Reduction of Output Capacitance for DAB DC-DC Converters in DC Microgrids by Shaping the Resistive Output Impedance

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***Abstract*—The reduction of output capacitance for Distributed Energy Resource (DER) converters in DC microgrids is expected, for the purpose of saving cost, decreasing system weight and size, and facilitating the short-circuit fault isolation. However, the decrease of output capacitance leads to the increase of output voltage spike/dip during load changes, and the output voltage may go out of the acceptable range during transient. From this point of view, the resistive output impedance is a better design solution for DER converters than non-resistive solutions, because it allows a larger voltage spike/sag and thus enables the use of smaller output capacitance. This paper proposed a design methodology for droop-controlled Dual Active Bridge (DAB) dc-dc converters, so that the resistive output impedance can be achieved. This design approach consists of the selection of output capacitance and the design of droop controller. Besides, for converters with small output capacitance, the output voltage presents high switching ripple. In such a case, the traditional single sampling technique causes a steady-state error between the averaged output voltage and the sampled one, impacting on the output impedance. This issue is addressed in this paper by a hybrid sampling method which combines the instantaneous value and the well-filtered value of the output voltage. Finally, the proposed design method with the hybrid sampling method is verified by experimental results.**

***Index Terms*—DAB converters, droop control, design guideline, resistive output impedance, output capacitance reduction.**

I. Introduction

DC microgrid is a collection of different kinds of Distributed Energy Resources (DERs), which include distributed generations and energy storage systems, and customer loads [1]. The typical layout of a standalone dc microgrid is shown in Fig. 1. Power electronic converters serve as the interfaces between DERs and the common dc bus. Droop control is widely adopted as the primary control strategy for DER converters, since it ensures automatic load distribution among parallel converters [2]. With droop control employed, the common dc bus voltage conveys the information of load condition, that is, the dc bus voltage decreases as the load power increases. In order to have a reliable dc bus voltage, literatures tend to install bulky output capacitance at the output ports of DER converters, leading to the increase of cost, converter weight and size. Meanwhile, large output capacitance means a great amount of energy stored on the dc bus. In case of a short-circuit fault, high fault current can be generated, making fault isolation more difficult [3]. Therefore, it is essential to reduce the output capacitance of DER converters.

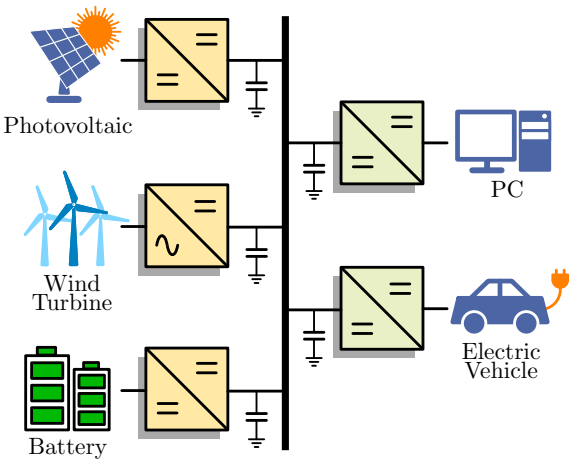

Fig. 1. Typical layout of a dc microgrid.

One of the constraints to reduce DER converter's output capacitance is the voltage tolerance range. The output voltage should be always maintained inside this acceptable range. Assuming the same dynamic response speed of the output voltage control loop, the voltage spike/sag during load changes increases with the decrease of the output capacitance. Hence, the minimum output capacitance is determined by the maximum allowable voltage spike/sag. Fig. 2(a) shows the typical non-resistive output impedance of droop-controlled DER converters and the corresponding dynamic output voltage waveform during transient. As can be seen, the allowable

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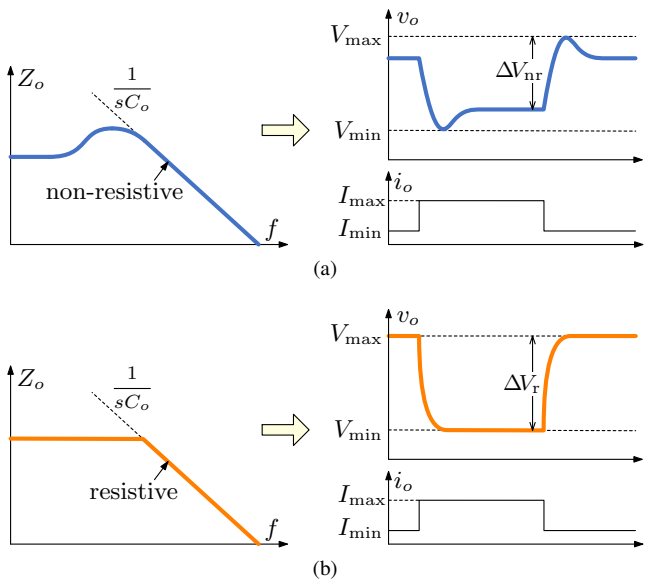


Fig. 2. Different output impedance of droop-controlled DER converters and corresponding dynamic output voltage waveforms during load changes. (a) Non-resistive output impedance; (b) Resistive output impedance. Resistive output impedance allows a larger voltage spike/dip than the non-resistive case ($\Delta V_{\rm r} > \Delta V_{\rm nr}$). Consequently, DER converters with resistive output impedance could use a smaller output capacitance.

voltage spike/dip $\Delta V_{\rm nr}$ makes use of part of the tolerance range. On the other hand, if the output impedance is designed to be resistive, as depicted in Fig. 2(b), the output voltage spike/dip $\Delta V_{\rm r}$ takes advantage of the full tolerance band. Apparently, since $\Delta V_{\rm r}$ is larger than $\Delta V_{\rm nr}$, resistive output impedance is the optimal design for the reduction of output capacitance.

The techniques for shaping the resistive output impedance have been deeply studied in the applications of Voltage Regulator Modules (VRM) used for powering microprocessors [4]–[7]. These research works cover many aspects, such as the design of the critical inductance, the output capacitance, and the voltage loop compensator. Moreover, a design guideline for droop-controlled DER converters is also presented in [8] to accomplish resistive output impedance, including the selection of output capacitance and the design of droop coefficient. However, the above mentioned literatures mainly focus on the basic dc-dc converters like buck converter and boost converter, with little attention paid to other converter topologies. For example, Dual Active Bridge (DAB) dc-dc converters are adopted in many applications like electric vehicles and energy storage systems where electrical isolation and high input-output voltage ratio are required [9], [10].

This paper applies the technique proposed in [8] to DAB droop-controlled converters. The output capacitance of DAB converters is reduced by shaping the resistive output impedance. The main contributions of this paper can be summarized as: (1) the design methodology for DAB converters is proposed, so that resistive output impedance can be achieved; (2) the feedback signal of the output voltage combines the instantaneous value and the filtered value, avoiding the steady-state sampling error. The rest of this paper is organized as follows. Section II presents the design guideline for DAB converters, including the selection of output capacitance and the design of droop controller. Section III analyzes the dc error existing voltage sampling and introduces the hybrid sampling method. Finally, Section IV shows the experimental results to validate the effectiveness of the proposed design methodology.

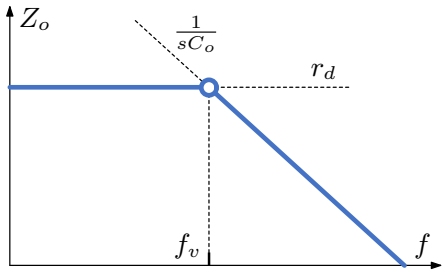


Fig. 3. Necessary output capacitance to achieve the resistive output impedance.

II. Design of DAB Converters

This section presents the design guideline for droop-controlled DAB converters to attain resistive output impedance, including the selection criterion of output capacitance and the design of droop controller.

A. Selection of output capacitance

The approximated relationship of the output capacitance, the voltage spike/dip and the voltage loop bandwidth is revealed herein, for the purpose of finding the necessary output capacitance to shape the resistive output impedance.

The accurate expression of the output impedance Z_o of a droop-controlled DAB converter is complicated. Since the target is to obtain an initial value of the output capacitance, which is not required to be highly precise, the simplified shape of Z_o is considered. Below the voltage control bandwidth, that is, $f < f_v$, Z_o can be effectively shaped to be resistive and be equal to the dc droop coefficient r_d by voltage control loop. Above the voltage control bandwidth, that is, $f > f_v$, Z_o is out of control and is dominated by the open-loop output impedance, which exhibits the characteristic of the output capacitance. In such a case, if the output capacitance is chosen at such a value that $1/sC_o$ intersects with r_d at f_v, the overall output impedance would meet the design requirement, as shown in Fig. 3. Further, the necessary output capacitance C_o can be expressed as:

$$C_o = \frac{1}{2\pi \cdot r_d \cdot f_v} \tag{1}$$

It is worth mentioning that the output capacitance obtained from (1) is only an initial estimation, it can be adjusted accordingly during the design process.

B. Design of droop controller

The design of droop controller for DAB converters is investigated herein. The idea is straightforward. Firstly, the small-signal model of a DAB converter is derived and the transfer function of the output impedance $Z_o(s)$ is deduced. Then, by assuming that $Z_o(s)$ equals r_d, the required control parameters can be found.

The control scheme of a droop-controlled DAB converter are shown in Fig. 4. The droop controller consists of a voltage loop and a droop loop. $G_v(s)$ is the voltage regulator, which usually employs PI to achieve zero steady-state error. The droop function can be expressed as below:

$$v_o^* = V_0 - i_o \cdot Z_d(s) \tag{2}$$

where V_0 is the voltage set point under no-load condition and $Z_d(s)$ is the frequency-dependent droop coefficient, which has a dc value of r_d. Single-phase-shift modulation is adopted herein. The key waveforms of the DAB converter are presented in Fig. 5. The bridge output voltages v_p and v_s are square waves with duty cycle fixed at 50%, and the phase shift ϕ between them is adjusted for power transfer. Different small-signal models are developed for DAB converters, covering both continuous-time [11], [12] and discrete-time models [13]. In this paper, the reduced-order continuous-time model is considered [11], since it is simple and provides enough accuracy at the frequency range that is well below the switching frequency.

The output power P_o of the DAB converter shown in Fig. 4 can be calculated as:

$$P_o = \frac{nV_{in}V_o\phi(\pi - |\phi|)}{2\pi^2 f_s L}, \quad -\frac{\pi}{2} < \phi < \frac{\pi}{2} \tag{3}$$

where f_s is the switching frequency and the other symbols can be found in Fig. 4. Assuming that the output voltage v_o is constant, then the bridge output current i_b can be expressed as:

$$i_b = \frac{nV_{in}\phi(\pi - |\phi|)}{2\pi^2 f_s L} \tag{4}$$

By linearizing (4) around a steady-state operation point, the transfer function $G_{i\phi}(s)$ from control to output current can be deduced as:

$$G_{i\phi} = \frac{\hat{i}_b}{\hat{\phi}} = \frac{nV_{in}(\pi - 2|\Phi|)}{2\pi^2 f_s L} \tag{5}$$

where Φ is the steady-state phase shift. Based on (5), the block diagram of the small-signal model of the DAB converter is illustrated in Fig. 6, where $G_{delay}(s)$ is the control delay including the computation time and the modulation delay. Further, the output impedance $Z_o(s)$ can be derived from this model:

$$Z_o(s) = Z_d(s)T_{vCL}(s) + \frac{1}{sC_o}\frac{1}{1 + T_{vOL}(s)} \tag{6}$$

where $T_{vOL}(s)$ and $T_{vCL}(s)$ are open-loop and closed-loop transfer functions of the voltage loop, respectively:

$$T_{vOL}(s) = \frac{G_v(s)G_{delay}(s)G_{i\phi}}{sC_o} \tag{7}$$

TABLE I
DAB CONVERTER PARAMETERS

Parameter	Symbol	Value
Input voltage	V_{in}	$48\,\mathrm{V}$
Nominal bus voltage	V_o	$380\,\mathrm{V}$
Nominal Power	P_n	$1.5\,\mathrm{kW}$
Inductance	L	$160\,\mu\mathrm{H}$
Output capacitance	C_o	$12\,\mu\mathrm{F}$
Switching frequency	f_s	$60\,\mathrm{kHz}$
DC droop coefficient	r_d	$5.07\,\mathrm{V/A}$
Voltage regulator	$G_v(s)$	$0.079+67.7/s$
Droop coefficient	$Z_d(s)$	$0.15\times\frac{s+2.9\times10^4}{s+858}$

$$T_{vCL}(s) = T_{vOL}(s)/[1 + T_{vOL}(s)] \tag{8}$$

To achieve resistive output impedance, there should be:

$$Z_o(s) = r_d \tag{9}$$

By combining (6) and (9), $Z_d(s)$ can be solved as:

$$Z_d(s) = \frac{r_d}{T_{vCL}(s)} - \frac{1}{sC_o}\frac{1}{T_{vOL}(s)} \tag{10}$$

Within the voltage control bandwidth f_v, $T_{vCL}(s)$ and $G_{delay}(s)$ can be approximated as unit gains. Finally, the required $Z_d(s)$ to accomplish the resistive output impedance can be expressed as:

$$Z_d(j\omega) = r_d - \frac{1}{G_{i\phi}G_v(j\omega)}, \quad \omega < 2\pi f_v \tag{11}$$

To numerically verify the effectiveness of the proposed design method, parameters of the DAB converter are given in Table I. The tolerance band of the output voltage is from $360\,\mathrm{V}$ to $400\,\mathrm{V}$, and the resulted dc droop coefficient r_d equals $5.07\,\mathrm{V/A}$. The voltage loop bandwidth f_v is designed at $3\,\mathrm{kHz}$, which is $1/20$ of the switching frequency. According to (1), the output capacitance is selected to be $12\,\mu\mathrm{F}$. Based on these system parameters, the output impedance of the DAB converter is drawn in Fig. 7. In the traditional way (i.e., $Z_d(s)$ is designed as a constant), the resulted $Z_o(s)$ show higher magnitude than r_d. On the contrary, after implementing the proposed $Z_d(s)$, the resistive output impedance is achieved, validating the feasibility of the proposed design approach.

In summary, there are three steps in the design process of a DAB converter to achieve resistive output impedance. (1) The voltage control bandwidth f_v can be estimated according to the switching frequency and the control delay. The dc droop coefficient r_d can be calculated based on the voltage tolerance range and the converter's nominal output current. Following (1), the output capacitance can be designed. (2) The voltage loop bandwidth should be designed at the estimated value by choosing a suitable regulator $G_v(s)$. (3) The droop coefficient $Z_d(s)$ should be derived from (11). In the end of the design process, it is necessary to perform a final check of the resulted output impedance.

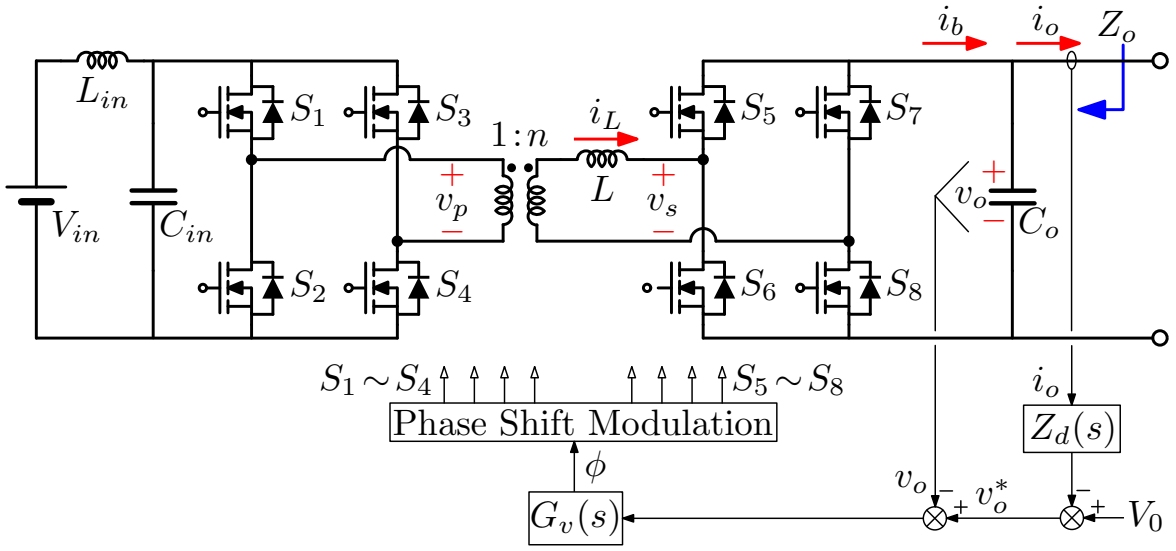


Fig. 4. Control scheme of a droop-controlled DAB converter.

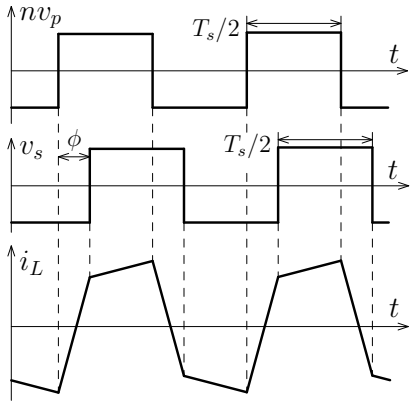


Fig. 5. The key waveforms of the DAB converter with single-phase-shift modulation implemented.

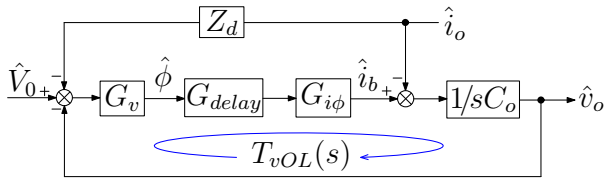


Fig. 6. Small-signal model of the DAB converter.

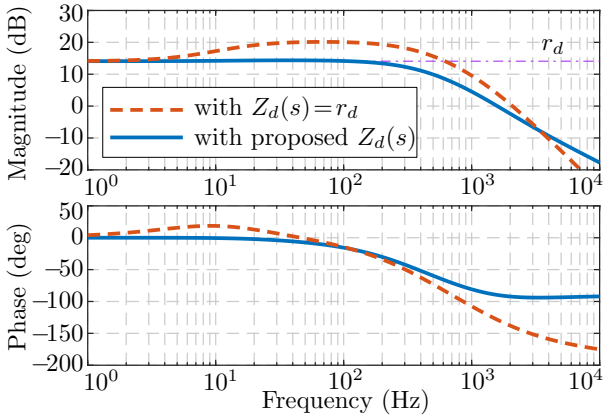


Fig. 7. Output impedance of the DAB converter with the traditional and proposed design methods. The resistive output impedance is achieved with the proposed design method.

III. Hybrid Sampling Method

Although the reduction of output capacitance shows benefits in the aspects of system weight, size, cost, and fault isolation, it inevitably brings the switching ripple on the output voltage to a higher level. Meanwhile, the output voltage is not sampled at middle points, so the increase of the switching ripple causes a larger steady-state error between the sampled output voltage and the average value, as shown in Fig. 8. What is worse, this error varies with the load condition due to the change of switching ripple. As a consequence, the actual output impedance is different from expectation, especially at low frequency.

To overcome this problem, a hybrid sampling method is implemented in this paper. The scheme of this sampling technique is displayed in Fig. 9. As can be seen, the output voltage is filtered by a physical low-pass filter to obtain its averaged value in steady state. Both the instantaneous value and the filtered value are sampled by ADC with a sampling frequency equal to the switching frequency. Inside the micro-controller, the instantaneous value is filtered by a digital high-pass filter. Afterwards, the feedback voltage signal $v_{\rm fb}$ is the sum of the two filtered signals.

The advantage of this sampling technique is discussed as follows. At high frequency, $v_{\rm fb}$ preserves the characteristic of the instantaneous voltage without introducing phase delay. Hence, the voltage loop bandwidth can be designed at a high frequency as usual. On the other hand, at low frequency, $v_{\rm fb}$ holds the averaged value since the switching ripple is

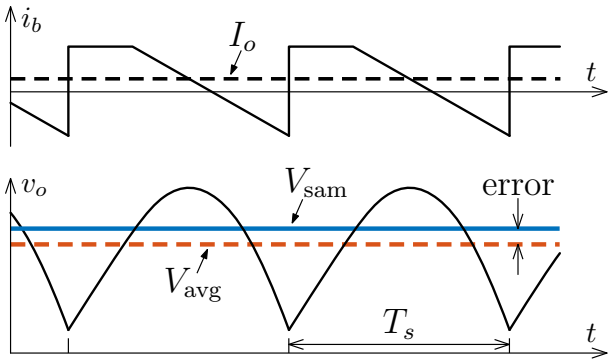


Fig. 8. The steady-state error between the sampled output voltage V_{sam} and the averaged one V_{avg}.

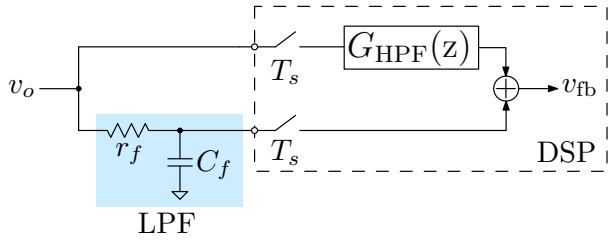


Fig. 9. The hybrid sample method. The feedback voltage signal makes use of the instantaneous voltage at high frequency and the filtered voltage at low frequency. By doing so, the dc sampling error can be compensated.

eliminated by the low-pass filter. In this case, the output impedance at low frequency can be corrected to the desired value.

IV. Experimental Results

To validate the proposed design method, a DAB converter is built up. The circuit diagram can be found in Fig. 4 and the picture of this converter is shown in Fig. 10. The system parameters are the same as those reported in Table I.

A. Output impedance measurement

In this test, the output impedance of the DAB converter is measured experimentally. The output current perturbations are generated by switching a part of the load at different

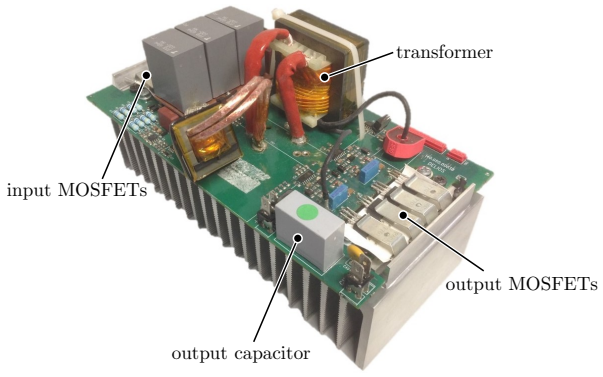


Fig. 10. Picture of the DAB converter prototype.

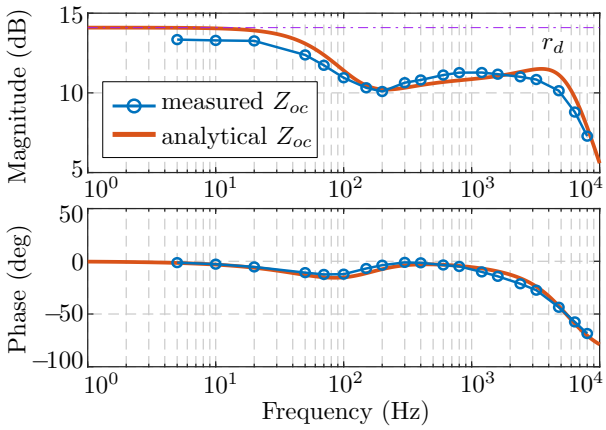


Fig. 11. The measured and theoretical output impedance of the DAB converter, with the proposed design method.

frequencies. The output current and the output voltage are acquired by the oscilloscope. By performing FFT on the waveforms, the real output impedance can be obtained.

With the proposed design method, the real output impedance is measured. Fig. 11 gives the comparison between the measured and the theoretical output impedance. A good match can be found between them at medium and high frequency. It should be noted that the measurement result is slightly lower than the analytical one at low frequency. This is because the voltage sensing has dc offset due to the influence of the switching ripple. The overall magnitude of the measured output impedance is lower than r_d, satisfying the design requirement.

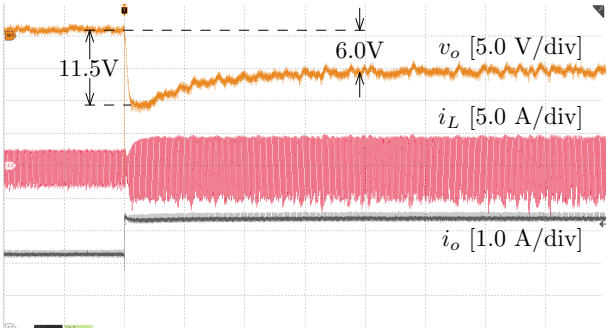
B. Voltage variations under load changes

The experiments under load step changes are carried out to find out the output voltage behavior. Fig. 12 presents the experimental results with the droop controller designed in the traditional way. As seen in Fig. 12(a), the output voltage shows a large undershoot of $11.5\,\text{V}$ in case of load step up. This voltage sag is actually almost two times of the static voltage drop due to droop function. Similar results can be found in Fig. 12(b) when the load steps down.

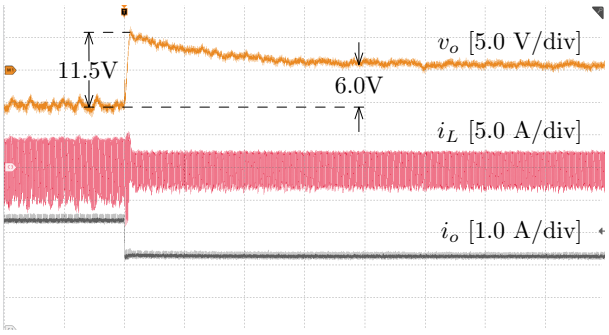
Subsequently, the droop coefficient $Z_d(s)$ is designed according to (11). Under the same load steps, the output voltage is tightly regulated inside the tolerance range, as shown in Fig. 13. Therefore, the effectiveness of the proposed design method is confirmed.

V. Conclusion

This paper proposed a design approach for droop-controlled DAB dc-dc converters in DC microgrids. The design target is to shape the resistive output impedance so as to reduce the output capacitance. Specifically, this design approach involves two parts. The first part is that the output capacitance should be selected according to the dc droop coefficient and the voltage control bandwidth. The second part is that the droop coefficient should be designed as a frequency-dependent term instead of a constant. In addition, the reduction of output

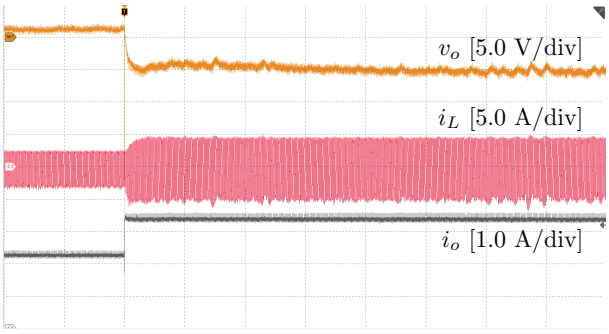


(a) 400 W load step up

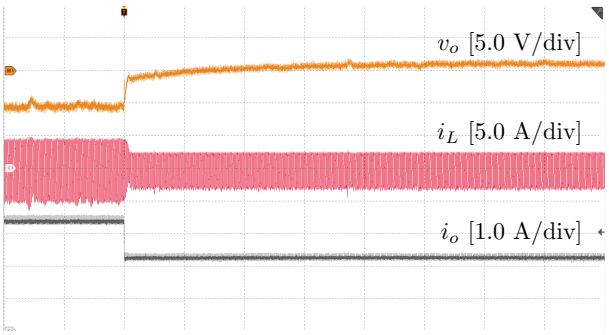


(b) 400 W load step down

Fig. 12. Experimental results under load step changes, with DAB converters designed in the traditional way. v_{bus} offset: 370 V. Time: 1 ms/div.



(a) 400 W load step up



(b) 400 W load step down

Fig. 13. Experimental results under load step changes, with DAB converters designed in the proposed way. v_{bus} offset: 370 V. Time: 1 ms/div.

capacitance leads to the increase of the switching ripple on the output voltage. Consequently, the error between the sampled voltage and the average voltage rises and the output impedance deviates from the expectation. This issue is addressed by the hybrid sampling technique which takes into account both the instantaneous voltage and the filtered voltage. Experimental results shows that the resistive output impedance is achieved in DAB converters, verifying the feasibility of the proposed design method and the hybrid sampling method.

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