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CICLO XXII

Analysis and Design of Injection-Locked Building Blocks for RF Frequency Generation in Ultra-Scaled CMOS Technologies

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Scuola di Dottorato di Ricerca in Ingegneria dell'Informazione
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Contents

Abstract

This work presents the analysis and the design of injection-locked building blocks for RF frequency generation in ultra scaled CMOS technologies. The injection locked mechanism is analyzed and employed both in the sub-harmonic injection locking version and in the super-harmonic injection locking version.

In the former case sub-harmonic injection locking is employed to generate the fast-hopping carriers required in UWB systems for WiMedia band ♯6 (i.e. from 15.3 GHz to 17.4 GHz). The work is supported by analysis of the LC oscillator in presence of a multi-tone synchronization signal and analysis of the hopping time. Measurement results of a 90 nm CMOS prototype demonstrate the feasibility of the proposed solution, achieving the lowest power and area consumption with respect to the state of the art.

In the latter case, super-harmonic injection locking is employed to a ring oscillator to realize a very compact, wideband divider topology that features low power consumption. A first test chip containing a divide-by-2 divider was realized in a 65 nm CMOS process. Measurements demonstrate a 2 to 16 GHz locking range, achieved with the lowest power and area consumptions among the state of the art solutions. In particular, the power consumption is 2 mW while the area consumption is only 130 μm^2.

The same divider topology is then extended to realize a divide-by-4 divider. The divider was implemented in a 65 nm CMOS process, together with a LC VCO operating at 8 times the GSM frequency range. The combination VCO + divider was implemented to generate a low power, low area local oscillator for the GSM standard. The figure of merit of the system VCO + divider is comparable with the state-of-the-art, despite the additional power consumption due to the divider. Moreover, the silicon area of the proposed work is remarkably smaller (0.06 mm^2).

Sommario

Questa tesi descrive l'analisi e la progettazione di blocchi circuitali per la generazione di segnali a radio frequenza in tecnologie CMOS ultrascalate, basati sul meccanismo dell' "*injection locking*". All'intenro della tesi il meccanismo di injection locking viene analizzato ed utilizzato sia nella sua variante di "*sub-harmonic injection locking*", sia nella variante di *super-harmonic injection locking*".

Nel primo caso il meccanismo di *sub-harmonic injection locking* viene applicato ad un oscillatore LC per generare le portanti "fast-hopping"della banda ♯6 dello standard UWB WiMedia (i.e. da 15.3 GHz a 17.4 GHz). Il lavoro é stato accompagnato da uno studio teorico della risposta dell'oscillatore LC in presenza di un segnale di sincronizzazione multitono e dallo studio del transitorio di hopping. I risultati delle misure effetuate su un prototipo realizzato in un processo CMOS a 90 nm hanno dimostrato la fattibilitá della soluzione proposta, candidandola come la migliore soluzione, fra quelle presenti allo stato dell'arte, in termini di consumi di potenza e area.

In meccanismo di *super-harmonic injection locking* é stato invece applicato ad un *ring oscillator* per realizzare in forma estremamente compatta una nuova topologia di divisori di frequenza a larghissima banda e basso consumo di potenza. Un primo test chip contenente un divisore per 2 é stato realizzato in un processo CMOS a 65 nm per dimostrare la fattibilitá della topologia proposta. Le misure hanno evidenziato un locking range da 2 a 16 GHz, ottenuto con i piú bassi consumi di potenza (2 mW) e area (130 μm^2) fra quelli dello stato dell'arte.

In seguito la stessa topologia di divisore é stata estesa per realizzare un divisore per 4. Il divisore é stato implementato in un processo CMOS a 65 nm, assime ad un VCO LC operante a 8 volte il range di frequenze GSM, per generare in forma compatta e a basso consumo di potenza un oscillatore locale conforme allo standard GSM. La figura di merito del sistema oscillatore + divisore risulta comparabile con quelle dello stato dell'arte, nonostante il consumo di potenza addizionale dovuto al divisore, ma con un consumo di area, pari 0.06 mm^2, sensibilmente inferiore.

Introduction

As multi-standard multi-band systems emerge in today wireless market, one of the most critical blocks to realize is the frequency synthesizer, that must operate over a wide range of frequencies with low power consumption. Moreover the constant increase level of integration of different systems in a single chip asks for low area solutions, with a preference for inductorless one. In this thesis we propose the use of injection locking as an efficient way to realize low power, low area building blocks for RF frequency generation in ultra-scaled CMOS technologies. In particular we focused on two points of particular interest: the design of an efficient local oscillator (LO) generation for high data rate WiMedia ultra-wideband (UWB) systems, and the design of a wide band, inductorless frequency divider.

The WiMedia Alliance proposed to channelize the UWB available spectrum from 3.1 to 10.6 GHz into 14 sub-bands. The channel center frequencies are at $f_c = 2904 + 528 \cdot n_b$ [MHz], where $n_b = 1, 2, ...14$, that is at odd harmonics of 264 MHz. The generation of the WiMedia UWB carriers entails several issues. A wide span of frequencies is to be synthesized while ensuring a fast hopping and phase coherence capability. The required ability of hopping from one LO frequency to the other within 9 ns prevents the use of a conventional approach based on a single wide-band PLL. Single-sideband (SSB) mixers can be used to offset a fixed frequency to simultaneously generate the required carriers which are dynamically selected by a multiplexer. This approach, however, in CMOS requires a huge power consumption to achieve low spurious. Another possibility is to use an array of PLLs, leading to a large area. In this work, we propose a completely different approach based on sub-harmonic injection locking [1]. An *LC* oscillator, operated at twice the desired frequency to avoid TX frequency pulling, is injection locked to the k^{th} harmonic of a 528-MHz reference to generate the carriers for WiMedia group ♯6 (i.e. from 15.3 to 17.4 GHz). Measurement results in 90-nm CMOS clearly show the required performance, while having lowest area and power.

Frequency dividers are largely employed in frequency synthesis and generation of quadrature phases. They are usually designed as clocked digital circuits, due to the ro-

bustness of this approach. However, a pure digital design suffers of the increase of power consumption with the frequency of operation. An alternative approach are injection-locked circuits. There are two main drawbacks in injection-locked dividers: they are often made of area-hungry LC oscillators to operate at higher frequencies; the locking range of the divider is usually quite limited. In this work, we present a divider circuit that addresses both issues by applying direct injection locking to a ring oscillator-based topology [2]. The design is ultimately based on digital gates, hence it benefits from technology scaling, while it is lower power than purely clocked digital circuits, as the divider circuitry switches at the output frequency rate.

A first design was intended to study the behavior and the performance of divider. Experimental results of a divide-by-two divider realized in a 65-nm CMOS process demonstrated a very compact circuit with a locking range from 2 to 16-GHz and a 2-mW power consumption. Then, we decide to employ this divider topology to realize a possible solution to simultaneously reduce area and power consumption, and improve the phase noise in LC local oscillator. The idea is to employ a higher frequency VCO followed by a frequency division system, as going to higher frequencies leads to smaller, reduced footprint, and often higher-Q, inductors. However, this solution can be attractive only if the system that brings back the frequency to the desired value consumes a negligible amount of area and power with respect to the oscillator. Then, the new divider circuit we proposed becomes the natural candidate for this kind of applications because it occupies a tiny silicon area, and it achieves a wide locking range with small power consumption. The effectiveness of this approach is demonstrate in the case of a GSM frequency synthesizer [3]. We designed an LC VCO operating at eight times the frequencies needed in GSM systems, followed by a divider divide-by-four frequency divider of the same topology of the divide-by-two divider. The chip was implemented in a 65-nm digital CMOS technology with a thick top metal layer and a standard 1.2 V supply. The phase noise at the divider output meets the GSM specifications without requiring any thick-oxide or lowthreshold voltage device, nor any dedicated supply voltage.

Chapter 1 of the thesis contains an introduction to the LC tanks, focused on the quality factor calculation and on the inductor modeling. A thorough analysis of the switched capacitor banks quality factor is carried out, demonstrating that the contribution of the switched capacitances in off state strongly affects the quality factor of the capacitor bank, and thus of the tank, increasing it. In succession a wide band lump components inductor model is presented, together with useful guidelines to guide the designer through the fitting of the model. Chapter 2 is the theoretical core of the thesis. Injection locking is deeply investigate both on LC and ring oscillators, providing the basics and the structure of the

design activity presented in the subsequent chapters. The design and the measurement results of the sub-harmonic injection locking LC oscillator for the UWB fast hopping frequency generation are presented in Chapter 3. Chapter 4 presents the design and the measurements results of the divide-by-two frequency divider, while the design and the measurements results of the local oscillator for the GSM standard are shown in Chapter 5.

Apendix A reports the design and the post-layout simulation results of VCOs and frequency divider for a step-frequency radar (SFR) for breast cancer detection. Two VCOs were designed, as well as a divide-by-four and a programmable divide-by-N frequency divider. We prefer to put this work in the appendix because the VCOs and the divide-by-four divider are of the same topology as the VCO and the divider presented in Chapter 5, then it does not add any new topic to the research work.

Part I

Analysis

Chapter 1

LC tanks

Nowadays, wireless communications ask for broadband or multiband systems that operate at always increasing frequencies. In such a scenario, one of the most challenging block to design is the voltage-controlled oscillator (VCO) [4–7], which must feature a wide tuning range, while meeting the phase noise requirements, and keeping the power consumption low. The performance of *LC* VCOs is strongly related to the tank features, so that most of the efforts in the VCO design are focused on the optimization of the tank. In this chapter we take into consideration two different aspects of the LC tanks: the optimization of the switch capacitors in the capacitor bank based tanks, and the modeling of the tank inductor.

1.1 Quality factor of thank with switched capacitor banks

1.1.1 Introduction

Many works in the literature focused on the analysis of the LC tanks, showing that a compromise between phase noise and tuning range is always necessary (e.g. [5–8]). Capacitor bank based tanks not only have been demonstrated to be the most suitable solution to achieve the best compromise between low phase noise and large tuning range, but they also achieve low tuning sensitivity, as they require small varactors to get continuous tuning [5, 6]. To achieve even larger tuning ranges, different solutions based on multi-mode or variable inductor tank have been proposed [9–12]. Nevertheless, to work properly, and to achieve the best performance, these solutions must be combined with a carefully designed capacitor bank. An accurate analysis of the capacitor bank is thus necessary

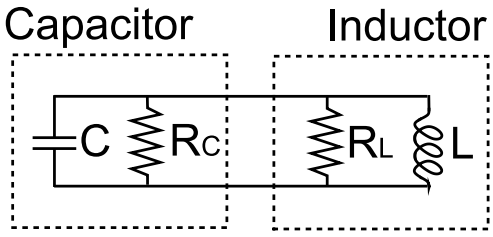


Figure 1.1 Parallel LC tank.

for the design of any VCO, since the impact of the capacitor quality factor on the overall tank quality factor is larger and larger as the frequency of operation increases.

1.1.2 Quality factor definition and computation

For a complex impedance Z, the quality factor is defined as the absolute value of the ratio of the reactance to the resistance (dually, for a complex admittance Y it is the absolute value of the ratio of the susceptance to the conductance):

$$Q = \left| \frac{\Im[Z]}{\Re[Z]} \right| = \left| \frac{\Im[Y]}{\Re[Y]} \right|. \tag{1.1}$$

As common sense would suggest, the higher the reactance (or susceptance) the higher the quality factor while the higher the resistance (or conductance) the lower the quality factor. Hence, to find the quality factor of any one-port network, we first have to calculate the equivalent impedance (or admittance) of the network and then apply (1.1). In Tab. 1.1, general expressions to easily and quickly calculate the quality factor of commonly used one-port networks, as well as some specific cases of particular interest, are reported. These results are very useful and allow the designer to immediately calculate the quality factor of many practically encountered complex networks.

Different from impedance, the quality factor of a LC tank is defined as the ratio between the energy stored and the average power dissipated per oscillation cycle:

$$Q_T = \omega_0 \frac{\text{Energy stored}}{\text{Average power dissipated}}. \tag{1.2}$$

where $\omega_0 = 1/\sqrt{LC}$ is the tank resonance frequency. To get more insight on this definition, let calculate the quality factor of the parallel LC tank drawn in Fig. 1.1 where both capacitor and inductor have losses. Let $V(t) = V_{pk}cos(\omega_0 t + \psi)$ the voltage across the tank. The energy E_T stored in the tank is:

$$E_T = \frac{1}{2} C V_{pk}^2 \tag{1.3}$$

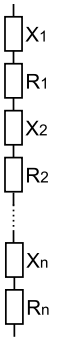
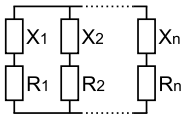
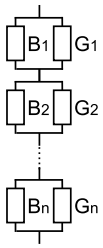
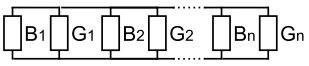
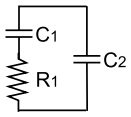
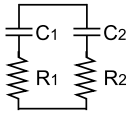
Configuration	Equivalent quality factor
	$Q_{eq1} = \left(\frac{1}{Q_1 \frac{X_S}{\lvert X_1 \rvert}} + \frac{1}{Q_2 \frac{X_S}{\lvert X_2 \rvert}} + \ldots + \frac{1}{Q_n \frac{X_S}{\lvert X_n \rvert}} \right)^{-1}$ $Q_i = \frac{\lvert Xi \rvert}{R_i}$ $X_S = X_1 + X_2 + \ldots + X_n$
	$Q^*_{eq2} \approx \left(\frac{1}{Q_1 \frac{\lvert X_1 \rvert}{X_P}} + \frac{1}{Q_2 \frac{\lvert X_2 \rvert}{X_P}} + \ldots + \frac{1}{Q_n \frac{\lvert X_n \rvert}{X_P}} \right)^{-1}$ $Q_i = \frac{\lvert Xi \rvert}{R_i}$ $X_P = \left(\frac{1}{X_1} + \frac{1}{X_2} + \ldots + \frac{1}{X_n} \right)^{-1}$
	$Q^*_{eq3} \approx \left(\frac{1}{Q_1 \frac{\lvert B_1 \rvert}{B_S}} + \frac{1}{Q_2 \frac{\lvert B_2 \rvert}{B_S}} + \ldots + \frac{1}{Q_n \frac{\lvert B_n \rvert}{B_S}} \right)^{-1}$ $Q_i = \frac{\lvert Bi \rvert}{G_i}$ $B_S = \left(\frac{1}{B_1} + \frac{1}{B_2} + \ldots + \frac{1}{B_n} \right)^{-1}$
	$Q_{eq4} = \left(\frac{1}{Q_1 \frac{B_P}{\lvert B_1 \rvert}} + \frac{1}{Q_2 \frac{B_P}{\lvert B_2 \rvert}} + \ldots + \frac{1}{Q_n \frac{B_P}{\lvert B_n \rvert}} \right)^{-1}$ $Q_i = \frac{\lvert Bi \rvert}{G_i}$ $B_P = B_1 + B_2 + \ldots + B_n$
	$Q_1 = \frac{1}{\omega R_1 C_1} \qquad Q_2 = \infty$ $Q_{eq5} \approx Q_1 \left(1 + \frac{C_2}{C_1} \right) > Q_1$
	$Q_1 = \frac{1}{\omega R_1 C_1} \qquad Q_2 = \frac{1}{\omega R_2 C_2}$ $Q_{eq6} = \left(\frac{1}{Q_1 \left(1 + \frac{C_2}{C_1} \right)} + \frac{1}{Q_2 \left(1 + \frac{C_1}{C_2} \right)} \right)^{-1}$
* assuming $Q_i \gg 1$	

Table 1.1 Equivalent quality factor of series and parallel combinations of complex impedances

while the power dissipated is:

$$P_T = \frac{V_{pk}^2}{2R_P} \tag{1.4}$$

where:

$$R_P = \frac{R_C R_L}{R_C + R_L} \tag{1.5}$$

is the equivalent tank parallel resistance. From (1.2) the tank quality factor reads as:

$$Q_T = \omega_0 \frac{E_T}{P_T} = \omega_0 C R_P = \sqrt{\frac{C}{L}} R_P \tag{1.6}$$

Let now find a way to derive Q_T starting from the inductor and the capacitor quality factors. Based on (1.1) the capacitor and inductor quality factor are respectively:

$$Q_C = \omega_0 C R_C \tag{1.7}$$

and

$$Q_L = \frac{R_L}{\omega_0 L} \tag{1.8}$$

Recasting (1.7) and (1.8) and making use of (1.5), we can express R_P as:

$$R_P = \frac{\frac{Q_C}{\omega_0 C} \cdot Q_L \omega_0 L}{\frac{Q_C}{\omega_0 C} + Q_L \omega_0 L} = \sqrt{\frac{L}{C}} \frac{Q_C Q_L}{Q_C + Q_L} \tag{1.9}$$

Combining (1.9) with (1.6), the tank quality factor can be written as:

$$Q_T = \frac{Q_C Q_L}{Q_C + Q_L} \tag{1.10}$$

that is the parallel combination of the capacitance and the inductance quality factors.

It can be proved (and it is a well known result) that this is a general result, and that the quality factor of any LC tank is equal to the parallel combination of the quality factors of the inductance and the capacitance that make up the resonant circuit. As a consequence, once we have the two quality factors Q_L and Q_C is very easy to calculate Q_T. Note that, as (1.1) evaluates zero when applied to resonators at the resonance frequency, the results in Tab. 1.1 must be used with care, when applied to the computation of Q_T. Basically, they have to be applied to networks with only one type of reactive behavior (capacitive or inductive); then, once Q_L and Q_C are derived, the aforementioned parallel combination of the two can be computed.

As we can notice looking to (1.7) and (1.8), while the quality factor of the inductor is growing with frequency, the capacitor one is decreasing with it. Since the quality factor of the tank is the parallel combination of the two quality factors, the growing the frequency, the more the capacitor quality factor limits the tank performance.

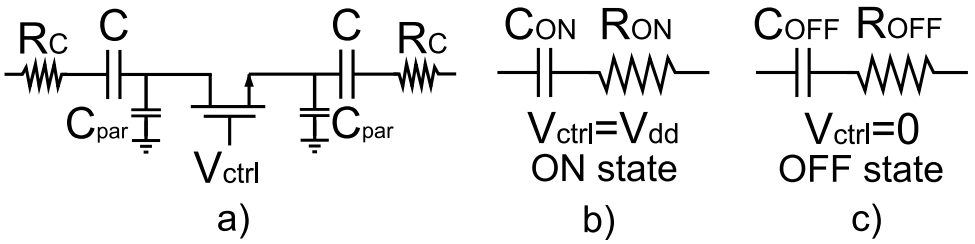


Figure 1.2 (a) Simplified schematic of a unit switched capacitance. (b) Equivalent model in the on state. (c) Equivalent model in the off state.

1.1.3 Capacitor bank quality factor

Consider the simplified schematic of a unit switched capacitance of the capacitor bank, drawn in Fig. 1.2(a). R_C is the parasitic resistance of the capacitance C, while $C_{\rm par}$ is the parasitic capacitance at each switch terminal. Depending on the gate voltage $V_{\rm ctrl}$, the transistor can be either in the on or in the off state. When $V_{\rm ctrl} = V_{\rm dd}$, the switch is turned on, becoming equivalent to a resistance $R_{\rm sw}$ in series to the capacitances C. According to equivalent model reported in Fig.1.2(b) the quality factor $Q_{\rm on}$ of the unit switched capacitance in the on state is:

$$Q_{\rm on}(\omega) = \frac{1}{\omega R_{\rm on} C_{\rm on}}, \tag{1.11}$$

where $C_{\rm on} \approx C/2$ and $R_{\rm on} = R_{\rm sw} + 2R_C \approx R_{\rm sw}$ is basically equal to the resistance of the MOS switch. When $V_{\rm ctrl} = 0$, the switch is turned off, that is it behaves like an open circuit. The equivalent model of the switched capacitance is sketched in Fig.1.2(c) and its quality factor $Q_{\rm off}$ is given by:

$$Q_{\rm off}(\omega) = \frac{1}{\omega R_{\rm off} C_{\rm off}}, \tag{1.12}$$

where $C_{\rm off} = CC_{\rm par}/(C + C_{\rm par})$ is the series connection of C and the parasitic capacitance of the switch $C_{\rm par}$, and $R_{\rm off} = 2R_C$ represents the losses of the capacitances C. Both the quality factors are in inverse proportion to the frequency and the series resistance. Moreover, it is important to notice that, since $R_{\rm off}$ is only due to the capacitor losses, for any frequency $Q_{\rm off} > Q_{\rm on}$, as shown in Fig. 1.3. The values of $C_{\rm on} = 44\,{\rm fF}$, $C_{\rm off} = 13\,{\rm fF}$, $Q_{\rm on} = 16$, and $Q_{\rm off} = 40$ (at 20 GHz) are obtained from a schematic simulation of a switched capacitance made of two 87 fF MIM capacitors connected by a $54\,\mu{\rm m}/60\,{\rm nm}$ nMOS switch.

Let us consider a capacitor bank realised by connecting in parallel N identical switched capacitances, $N_{\rm on}$ of them in the on state and $N_{\rm off} = N - N_{\rm on}$ of them in the off state.

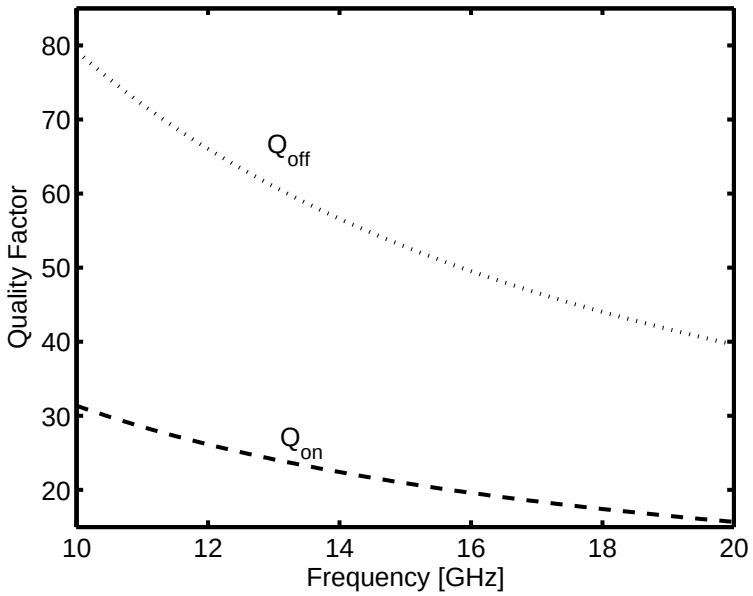


Figure 1.3 Quality factor of the unit capacitance in the on state (Q_{on}) and in the off state (Q_{off}). The values of $C_{\text{on}} = 44\,\text{fF}$, $C_{\text{off}} = 13\,\text{fF}$, $Q_{\text{on}} = 16$, and $Q_{\text{off}} = 40$ (at 20 GHz) are obtained from a schematic simulation of a switched capacitance made of two 87 fF MIM capacitors connected by a $54\,\mu\text{m}/60\,\text{nm}$ nMOS switch.

We can represent all the switched capacitances in the on state with one capacitance $C_1 = N_{\text{on}}C_{\text{on}}$ of quality factor $Q_1 = Q_{\text{on}}$, and all the switched capacitances in the off state with one capacitance $C_2 = N_{\text{off}}C_{\text{off}}$ of quality factor $Q_2 = Q_{\text{off}}$. Note that this is true even in the more general case where each switched capacitance has a different value, as long as they are designed in such a way that the quality factor is the same for all the capacitances. The quality factor of the capacitor bank, Q_{CB}, can be calculated substituting C_1, C_2, Q_1, and Q_2 into the expression of Q_{eq6} reported in Tab. 1.1:

$$\begin{aligned} Q_{\text{CB}} &= \left(\frac{1}{Q_{\text{on}}\left(1+\frac{C_2}{C_1}\right)} + \frac{1}{Q_{\text{off}}\left(1+\frac{C_1}{C_2}\right)} \right)^{-1} \\ &= \left(\frac{1}{Q_{\text{on}}\left(1+\frac{N_{\text{off}}C_{\text{off}}}{N_{\text{on}}C_{\text{on}}}\right)} + \frac{1}{Q_{\text{off}}\left(1+\frac{N_{\text{on}}C_{\text{on}}}{N_{\text{off}}C_{\text{off}}}\right)} \right)^{-1} \end{aligned} \tag{1.13}$$

Solving for N_{on} we obtain:

$$Q_{\text{CB}} = Q_{\text{off}} \frac{N + N_{\text{on}}(\beta - 1)}{N + N_{\text{on}}(\beta \cdot \gamma - 1)}, \tag{1.14}$$

where $\beta = C_{\text{on}}/C_{\text{off}}$, and $\gamma = Q_{\text{off}}/Q_{\text{on}}$.

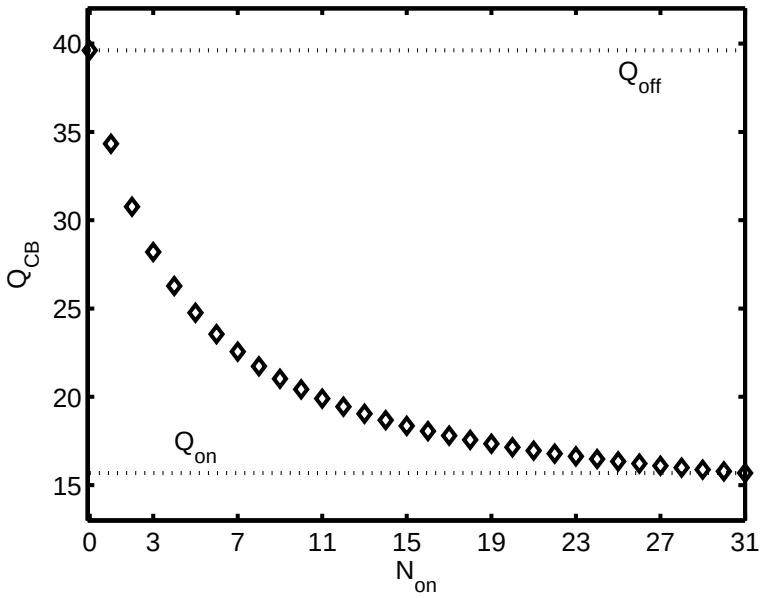


Figure 1.4 Quality factor of the capacitor bank at 20 GHz as a function of N_{on} ($N = 31$, $Q_{\text{on}} = 16$ at $20GHz$, $C_{\text{on}} = 44fF$, $\beta = 3.4$, $\gamma = 2.5$).

As expected, for $N_{\text{on}} = 0$ the quality factor is equal to Q_{off}, while for $N_{\text{on}} = N$ it is equal to $Q_{\text{off}}/\gamma = Q_{\text{on}}$. Fig. 1.4 shows the value of Q_{CB} as a function of N_{on} at a frequency of 20 GHz. Obviously, the analysis carried out so far is not exhaustive, because it does not take into account the change in the tank resonance frequency with N_{on}. The resonance frequency is given by:

$$\begin{aligned}\omega =& \frac{1}{\sqrt{L\left(C_p + N_{\text{on}}C_{\text{on}} + N_{\text{off}}C_{\text{off}}\right)}} \\ =& \frac{1}{\sqrt{LC_p + LC_{\text{off}}\left(N + N_{\text{on}}\left(\beta - 1\right)\right)}},\end{aligned} \tag{1.15}$$

where L is the tank inductance and C_p is the tank fixed capacitance. Recasting (1.15), we express N_{on} as a function of the frequency ω:

$$N_{\text{on}}\left(\omega\right) = \left(\frac{1}{LC_{\text{off}}\omega^2} - \frac{Cp}{C_{\text{off}}} - N\right)\frac{1}{\beta - 1} \tag{1.16}$$

Replacing (1.16) it into (1.14) we derive:

$$Q_{\text{CB}}\left(\omega\right) = \frac{\gamma\left(\beta - 1\right)}{R_{\text{on}}C_{\text{on}}} \cdot \frac{1 - LC_p\omega^2}{\omega\left(\beta \cdot \gamma - 1\right) + \omega^3 L\left[NC_{\text{off}}\beta\left(1 - \gamma\right) - C_p\left(\beta \cdot \gamma - 1\right)\right]} \tag{1.17}$$

A plot of (1.17), compared to the quality factor Q_{on} of the unit switched capacitance in the on state, is illustrated in Fig. 1.5 in the case of $L = 100\,\text{pH}$ and $C_p = 200\,\text{fF}$. The

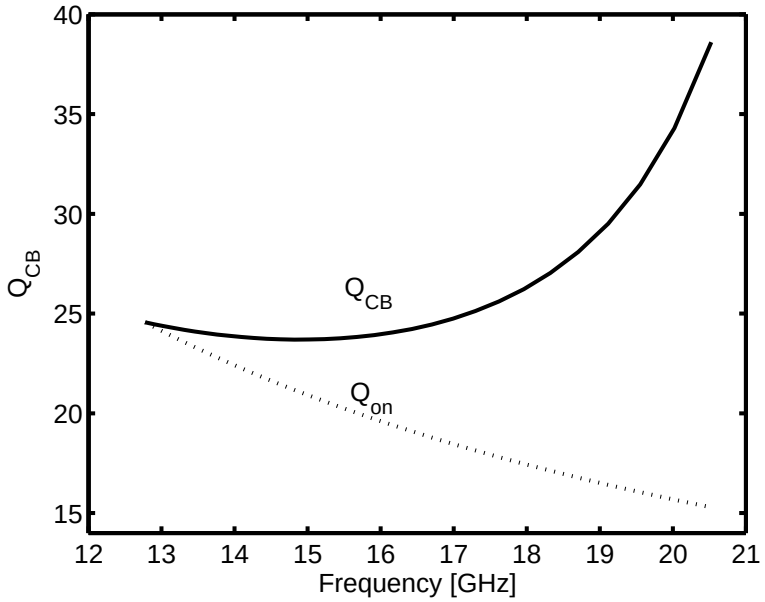


Figure 1.5 Quality factor of the capacitor bank ($Q_{\rm CB}$) and of a unit switched capacitance in the on state ($Q_{\rm on}$) as a function of frequency ($N = 31$, $Q_{\rm on} = 16$ at 20,GHz, $C_{\rm on} = 44\,{\rm fF}$, $\beta = 3.4$, $\gamma = 2.5$, $L = 100\,{\rm pH}$, $Cp = 200\,{\rm fF}$).

frequency range has been calculated varying $N_{\rm on}$ from 0 to N in (1.15). As opposed to what one could expect, the capacitor bank quality factor increases with the frequency (even if not monotonically) and $Q_{\rm CB}\left(f_{\rm max}\right) \gg Q_{\rm on}\left(f_{\rm max}\right)$.

Fig. 1.6 illustrates the quality factor of the capacitor bank for different values of C_p. As expected, the smaller the fixed capacitance, the smaller the minimum quality factor because for a given $N_{\rm on}$ the tank resonance frequency increases, consequently reducing both $Q_{\rm on}$ and $Q_{\rm off}$.

The minimum quality factor of the capacitor bank in the worst case ($C_p = 0$) is derived setting its derivative with respect to the frequency ω to zero:

$$\frac{dQ_{\rm CB}}{d\omega} = 0 \;\Rightarrow\; 3\omega^2\left[\beta N L C_{\rm off}\left(\gamma - 1\right)\right] = \beta\cdot\gamma - 1, \tag{1.18}$$

that gives

$$f_{Q\rm min} = \frac{\omega_{\rm max}}{2\pi}\sqrt{\frac{\beta\cdot\gamma - 1}{3\beta\left(\gamma - 1\right)}}, \tag{1.19}$$

where $\omega_{\rm max} = 1/\sqrt{LNC_{\rm off}}$.

When $N_{\rm on} = N$ the tank resonates at the minimum frequency $f_{\rm min}$ and $Q_{\rm CB}$ is equal to $Q_{\rm on}\left(f_{\rm min}\right)$. Increasing the frequency (decreasing $N_{\rm on}$) the quality factor first decreases

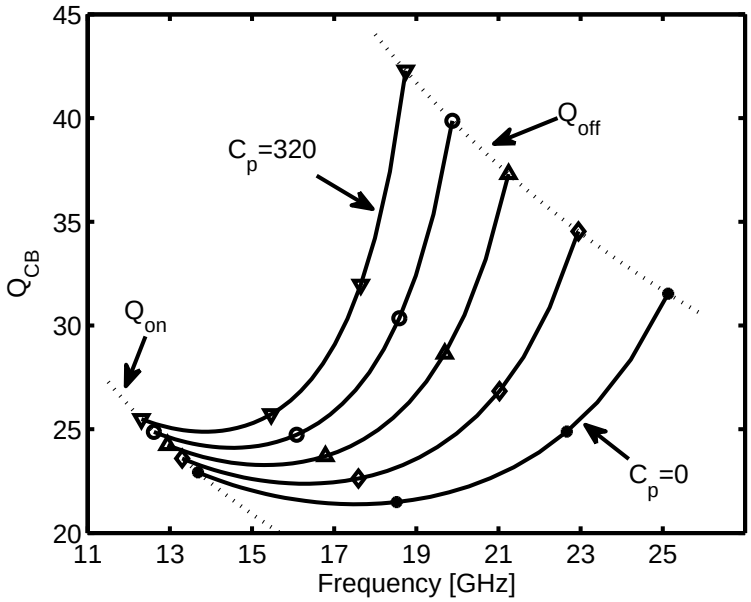


Figure 1.6 Q_{CB} varing the tank fixed capacitance $C_p : \nabla = 320fF$, $\circ = 240fF$, $\triangle = 160fF$, $\diamond = 80fF$, $* = 0fF$ ($N = 31$, $Q_{\mathrm{on}} = 15.62$ at 20 GHz, $C_{\mathrm{on}} = 44$ fF, $\beta = 3.4$, $\gamma = 2.5$, $L = 100$ pH).

reaching its minimum value at frequency $f_{Q\mathrm{min}}$, then it increases to its maximum value $Q_{\mathrm{off}}(f_{\mathrm{max}})$ achieved at the maximum frequency f_{max} ($N_{\mathrm{on}} = 0$). If $f_{Q\mathrm{min}} < f_{\mathrm{min}}$, Q_{CB} grows monotonically. Considering the case $C_p = 0$, the condition $f_{Q\mathrm{min}} < f_{\mathrm{min}}$ results in:

$$\beta < 3 - \frac{2}{\gamma} < 3. \tag{1.20}$$

Since in almost all applications $\beta \geq 3$, we can assume that (1.20) is never satisfied, and that Q_{CB} has the frequency behavior illustrated in Fig. 1.6.

1.1.4 Tank quality factor

Since the capacitive part of the tank is composed by both the bank capacitance C_{CB} and the fixed capacitance C_p, we must include the contribution of the latter in the computation of the quality factor. The quality factor of the capacitive part of the tank is therefore:

$$Q_C(\omega) = \left[\frac{1}{Q_{\mathrm{CB}}(\omega)\left(1 + \frac{C_p}{C_{\mathrm{CB}}}\right)} + \frac{1}{Q_p(\omega)\left(1 + \frac{C_{\mathrm{CB}}}{C_p}\right)} \right]^{-1}, \tag{1.21}$$

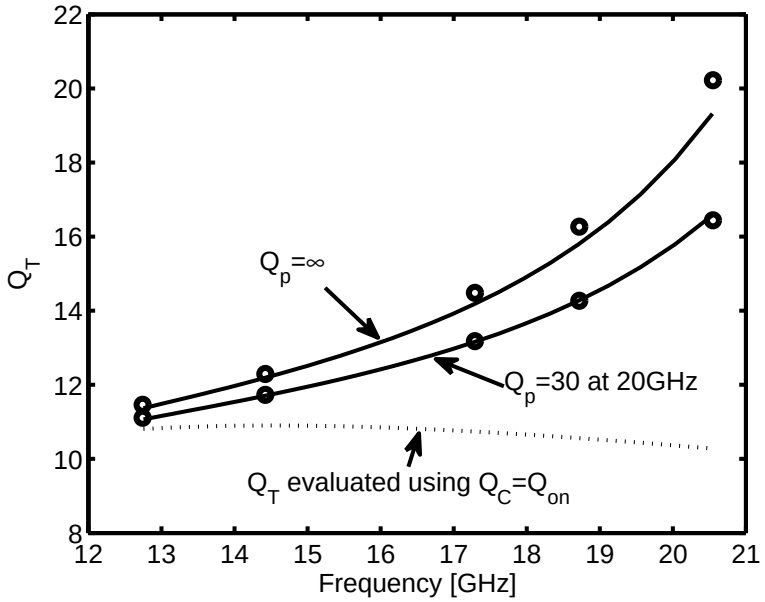


Figure 1.7 Tank quality factor calculated for two different value of Q_p (solid line). Circles are schematic simulation results. Dashed line refers to the assumption $Q_C = Q_{\text{on}}$ ($N = 31$, $Q_{\text{on}} = 16$ at 20 GHz, $C_{\text{on}} = 44\,\text{fF}$, $\beta = 3.4$, $\gamma = 2.5$, $L = 100\,\text{pH}$, $Q_L = 30$ at 20, $C_p = 200\,\text{fF}$).

where Q_p is the quality factor of the fixed capacitance. The tank quality factor is :

$$Q_T(\omega) = \left[\frac{1}{Q_C(\omega)} + \frac{1}{Q_L(\omega)}\right]^{-1}, \tag{1.22}$$

where $Q_L(\omega) \approx \omega L/R_L$ is the inductance quality factor, R_L is the inductance series resistance, and ω is given by (1.15).

Fig. 1.7 compares the theoretical and simulated tank quality factor in the case Q_L is 30 at 20 GHz for two different values of Q_p: $Q_p = \infty$ and $Q_p = 30$ (at 20 GHz). The capacitor bank is composed by 16 identical switched capacitances, binary weighted by 4 control bits. There is a very good agreement between schematic simulations and the presented theory.

Previous work evaluated the tank quality factor assuming that the quality factor of the capacitive part (Q_C) was equal to Q_{on} (dashed line in Fig.1.7). This results in an underestimation of Q_T, especially at the higher end of the tuning range. The new results show instead that there is some additional headroom in the design of the capacitor bank. For a target Q_T, and for a given technology, smaller transistors may be employed as switches, reducing the parasitic capacitances, and thus achieving a wider tuning range.

In other words, one must design the capacitor bank for a target Q_{on} evaluating it at f_{min}, and not at f_{max}, as traditionally done, and as intuition would point to.

1.2 Inductor modelling

In the previously section we see that the design of high frequency, wide tuning range VCOs needs to be accomplished with a careful design of the capacitor bank to obtain the maximum tuning range with the minimum amount of parasitic capacitance. Nevertheless we must keep in mind that the best performance is achieved only if even the inductor is also carefully designed: the smaller the inductor the bigger the tuning range and the lower the phase noise, but the higher the consumption. The design and the optimization of the inductor is out of the purpose of this work. At the contrary we are more interested in presenting of an equivalent lump components model for the inductor that fits the electromagnetic (EM) simulation of the inductor over a wide range of frequency. In the following we first explain how the model was derived, then we try to give some guidelines for the fitting in order to give to the reader some practical advices.

1.2.1 Introduction

The need of simulating high frequency, wide tuning range oscillators introduces the problem of the inductor modeling. The wide tuning range prevents the use of a simple narrowband model and the high operating frequencies ask to take into account all the parasitic effects of the inductor. The design of the inductor is usually done by an EM simulator. Its inputs are the inductor shape and the technology parameters of the substrate stack, while its output is a $n-$port representation of the inductor[1]. The simulation is run over frequency so that the characterization of the inductor that we posses at the end of the simulation is very accurate and wideband. Nevertheless the results cannot be directly used in schematic level simulations solved in the time domain, because of accuracy and convergence problems. The solution is to build an equivalent lumped components model of the inductor, to fit it with the EM simulations results, and to use it in the schematic level simulations.

[1]Most of the time the results are given in the form of scatter ($s-$) parameters. Anyway all the n-ports representations are equivalent and it is always possible to change from one representation to the other, depending on which one is the most suitable.

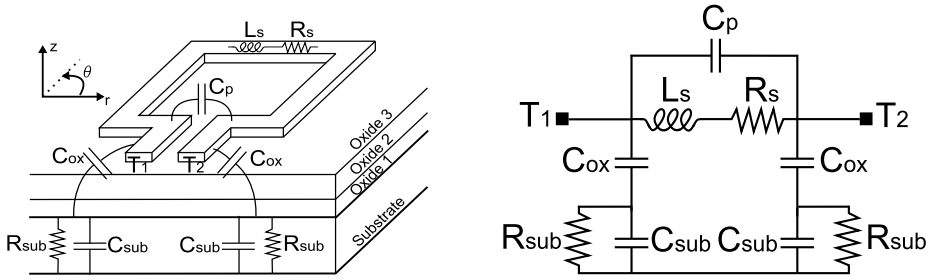


Figure 1.8 (a) Integrated inductor cross section. (b) Six components equivalent π model.

1.2.2 Model derivation

Consider the cross section of a general inductor drawn in fig. 1.8(a) and its six elements π model sketched in fig. 1.8(b). L_s an R_s are respectively the inductance and the series resistance value of the inductor while C_p is the parasitic capacitance between turns and/or between different segments of a turn. The chip substrate introduces other parasitic elements, usually not present in off chip inductor: C_{ox}, that is the capacitance of the dielectric between the top of the substrate and the inductor, and R_{sub} and C_{sub}, that are respectively the losses and the parasitic capacitance of the silicon substrate. On one hand the 6 elements π model results very simple and the value of each component sketched in fig. 1.8(b) can be quickly derived from the EM simulation. On the other hand, because of its simplicity, it is narrowband.

Let consider for instance the resistance of the metal strip that make up the inductor. This is mainly due to two different physic aspects: the finite conductivity of the metal, and the skin effect. The further contribution is constant with frequency, while the latter is frequency dependant and it is relevant only at high frequency. However, because of the growing of the operating frequency it cannot be neglected in the model. Nevertheless both contributions are modeled together by meaning of R_s, that is frequency invariant, preventing the model to fit the series resistance of the metal strip over a wide range of frequencies.

This simple example suggests that in order to build a very wide-band model of the inductor we have to:

- individuate and model all the physic phenomena present in a IC inductor;
- separate the frequency independent phenomena form the frequency dependant ones, even when they results in the same effect (e.g. both finite conductivity and skin

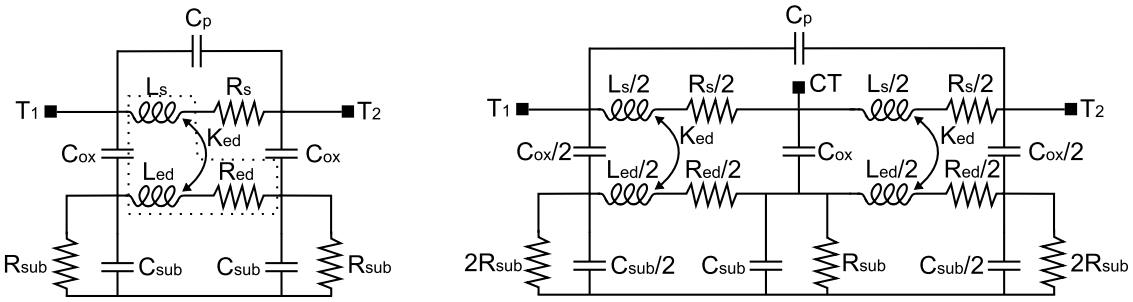


Figure 1.9 a) Single π substrate-coupled inductor model reported in [13]. b) Double π substrate-coupled model that takes into account the central tap terminal of the inductor (T_3).

effect result in a series resistance greater than zero);

- take into account the frequency dependant nature of the latter in the model.

Many works in the literature have already explained which are the major parasitic effects present in the integrated inductors. In the following we just limit to summarized them [13]:

1. the current does not flow uniformly in wiring because of skin and proximity effects, increasing the resistance with increasing frequency;

2. when the current flowing in wiring becomes less uniform with increasing frequency, inductance decreases;

3. in the case of a low-resistivity substrate, at high frequencies a large current flows in the substrate due to capacitive coupling between the wiring and the substrate. Moreover, an eddy current also flows in the substrate due to the magnetic coupling between it and the inductor.

The simple 6 elements π model already models the capacitance coupling between inductor and substrate but it does not consider the presence of currents flowing on the surface of the substrate. Those currents can be either magnetic or capacitive. To catch both the phenomena, the model was modified adding the substrate network drawn inside the dashed line in fig. 1.9(a) [13]. Here R_s and L_s represent respectively the resistance, and the inductance of the inductor at low frequency, R_{ed} and L_{ed} denote the substrate resistance and inductance, and K_{ed} is the coupling coefficient between L_s and L_{ed}. Then, to model inductors with a central tap terminal (CT), the model has been transformed to

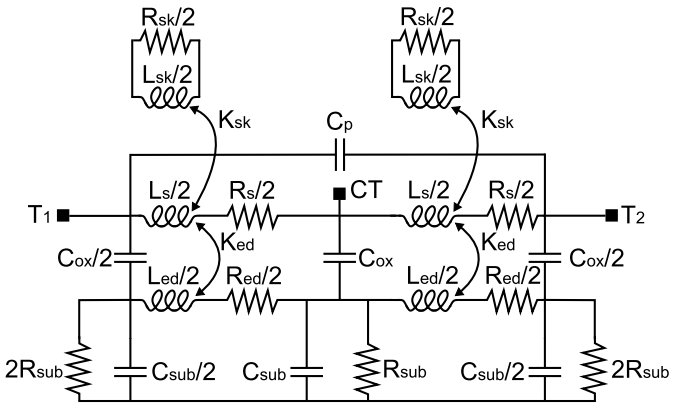


Figure 1.10 The completed broadband lumped components model of an IC inductor.

the double π model of fig. 1.9(b), that is even more beneficial because it better represents the distribute nature of the parasitics. The model was derived assuming that the inductor is symmetrical with respect to the central tap. As a consequence L_s, R_s, L_{ed},and R_{ed} were replaced with the series of two components whose value is half the original one, and the shunt impedance connected between the central tap and ground is the parallel combination of the two shunt impedances connected to the other two terminals of the inductor. The only parasitic effects left to model are the skin and proximity effects of the wiring. To take them into account the model has been completed by adding the two current loops made by $L_{sk}/2$ and $R_{sk}/2$ [14], as shown in fig. 1.10. Another common way to model the skin and proximity effects is to add a series LR network in shunt to the resistance R_s [15] [16]. We preferred to do not use this solution because, for the inductor we had to model[2], it resulted less accurate than the solution with the current loops. Nevertheless, this does not exclude that the solutions might be better for other inductors, and we suggest to try it if the current loop solutions does not give a satisfactory result.

Then, the model of fig. 1.10 is a very accurate, broad-band model for integrated inductor, that take into account all the parasitics effects. Moreover, for each component of the model, we exactly know which particular physic aspect it represents, that is a very useful knowledge for the next step: the fitting of the model with the EM simulations results[3].

[2]single turn inductor with diameter smaller than $200\mu m$.

[3]The EM simulator gives a scatter (s-) parameters representation of the inductor. Nevertheless we will refer to the impedance (z-) or the admittance (y-) parameter representation because they give more insight on the physic aspects of the inductor. Anyway is trivial to convert the scatter representation to either impedance or admittance representation and many EM simulators already include this function, so that they can do the transformation automatically.

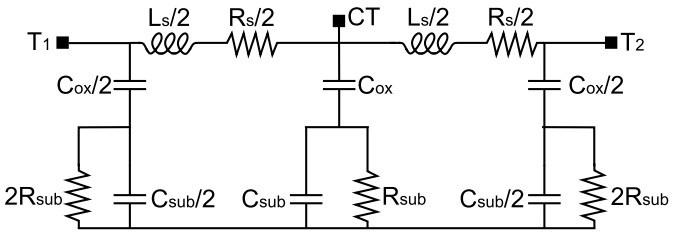


Figure 1.11 Low frequencies simplified model of the inductor for the derivation of L_s and R_s.

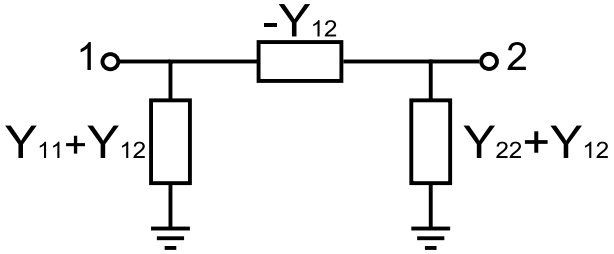


Figure 1.12 π representation of a 2-port network.

1.2.3 Model Fitting

Let focus our attentions at very low frequencies, where the the contribution of C_p, the skin effect, and the eddy currents are negligible. The equivalent model can be simplified as shown in Fig. 1.11. At those frequencies the module of the shunt impedances connected between T_1, T_2, CT, and ground are much bigger than the series impedance connected between T_1 and T_2. Then, referring to the π representation of the 2-ports network sketch in Fig. 1.12 we can affirm that [17]:

$$L_s = \mathrm{Im}\left[\frac{-1/Y_{12}(\omega)}{\omega}\right] \tag{1.23}$$

$$R_s = \mathrm{Re}\left[-1/Y_{12}(\omega)\right] \tag{1.24}$$

where 1.23 and 1.24 are evaluated at the lowest frequency available from the EM simulations data (idealy at DC). Similar considerations can be obtained for the shunt impedances, by computing the z-parameters. In fact, at low frequencies we can assume that C_p and C_{sub} are open circuits, L_s is a short, R_s is negligible with respect to R_{sub}, and that the magnetic and the capacitive currents flowing in the substrate are negligible. Under this assumptions, Z_{11} is as sketched in fig. 1.13 and C_{ox} and R_{sub} can be computed as:

$$C_{ox} = -\frac{1}{2}\frac{1}{\omega \mathrm{Im}\left[Z_{11}(\omega)\right]} \tag{1.25}$$

$$R_{sub} = 2\mathrm{Re}\left[Z_{11}(\omega)\right] \tag{1.26}$$

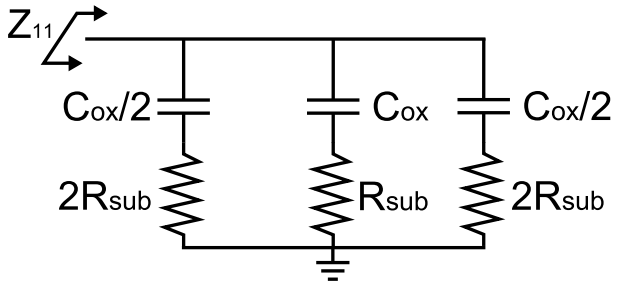


Figure 1.13 Low frequencies simplified model of the inductor for the derivation of C_{ox} and R_{sub}.

Again 1.25 and 1.26 are evaluated at the lowest frequency available from the EM simulations data, in order to make valid the assumption that we mentioned.

To complete the fitting of the model we still need to find the right value of C_{sub}, L_{ed}, R_{ed}, k_{ed}, L_{sk}, R_{sk}, k_{sk}, and C_p. Unfortunately, those values cannot be derived from simply assumptions as we did for L_s, R_s, C_{ox}, and R_{sub}, and we have to use some fitting tool to derive them.

Fitting with ADS Optimizer

A good solution is to use the ADS optimizer tool, based on the nominal optimization component OPTIM. What the nominal optimization does, is to modify the value of a set of optimization variables to try to reach predefined goals. In our case the optimization variables are C_{sub}, L_{ed}, R_{ed}, k_{ed}, L_{sk}, R_{sk}, k_{sk}, and C_p, while the goal is to obtain an equivalent lumped model that matches in the best way is possible, and over the lager range of frequency is possible, the EM simulation results. The more important parameters of the OPTIM component are:

- OptVar: defines the variables to use for the optimization;
- OptGoal: defines the optimization goals;
- optimization Type: defines the algorithm to use to perform the optimization;
- Number of iterations: maximum number of iterations that the optimization engine is allowed to run. If this limit is reached, the simulation will stop, regardless whether the goal function is reached or not.

Variables and goals are defined in appropriate components called VAR and GOAL respectively. The more important parameters for a variable are:

- variable value: the defaul value of the variable;
- the optimization tab: here is possible to enable the variable for the optimization as well as define the minimum and maximum value it can assume during the optimization process.

For a goal the more important parameters are:

- Expr: it is the function that we want to optimize (In the following when we refer to a goal, we implicitly refer to its function);
- Min and Max: they are respectively the minimum and maximum acceptable values for Expr;
- RangeVar: it is the independent variable. We want to match the model with the EM simulation over frequency, so in our case the independent variable will be the frequency.
- RangeMin and RangeMax: they define inside which range of the independent variable, (inside which range of frequency in our case), the goal must be reached.

To fix the idea let refer to Fig. 1.14, that reports the schematic used for the first step of the fitting procedure that will be describe in the following. On the right side of the figure there is the inductor model, loaded with two ports: port-3 and port-4. The value of each component in the schematic is defined with a variable contained in VAR. The S2P component contains the EM simulation result of the inductor and it is terminated to two other ports: port-1 and port-2. S-PARAMETERS defines the type of simulation to run, that is a scatter parameter simulation, as the EM simulation was. SWEEP PLAN defines the range of frequency where performing the simulation. It has been set to contain exactly the same frequency points than the EM simulation. The two GOAL components $C_{sub-goal1}$ and $C_{sub-goal2}$ define the goals: $\left(1-\frac{\mathrm{Im}[Z_{11}]}{\mathrm{Im}[Z_{33}]}\right)$ and $\left(1-\frac{\mathrm{Re}[Z_{11}]}{\mathrm{Re}[Z_{33}]}\right)$, respectively. Their Min and Max parameters are $-1e-3$ and $1e3$, while the RangeVar is set to be equal to the whole frequency range defined in SWEEP PLAN. In OPTIM we set C_{sub} as OptVar, and $C_{sub-goal1}$ and $C_{sub-goal2}$ as OptGoals. When we start the simulation OPTIM will try to modify the value of the variable C_{sub} inside its range of variation to make the value of the two goal expressions to lie inside their [Min, Max] range. This is obtained when $\mathrm{Im}[Z_{11}] \approx \mathrm{Im}[Z_{33}]$ and $\mathrm{Re}[Z_{11}] \approx \mathrm{Re}[Z_{33}]$. That means that the optimization procedure will try to modify the value of C_{sub} to match, over the whole range of frequency, the real and the imaginary part of the impedance Z_{11} of the lumped model with the real and the imaginary part of Z_{11} obtained from the EM simulation.

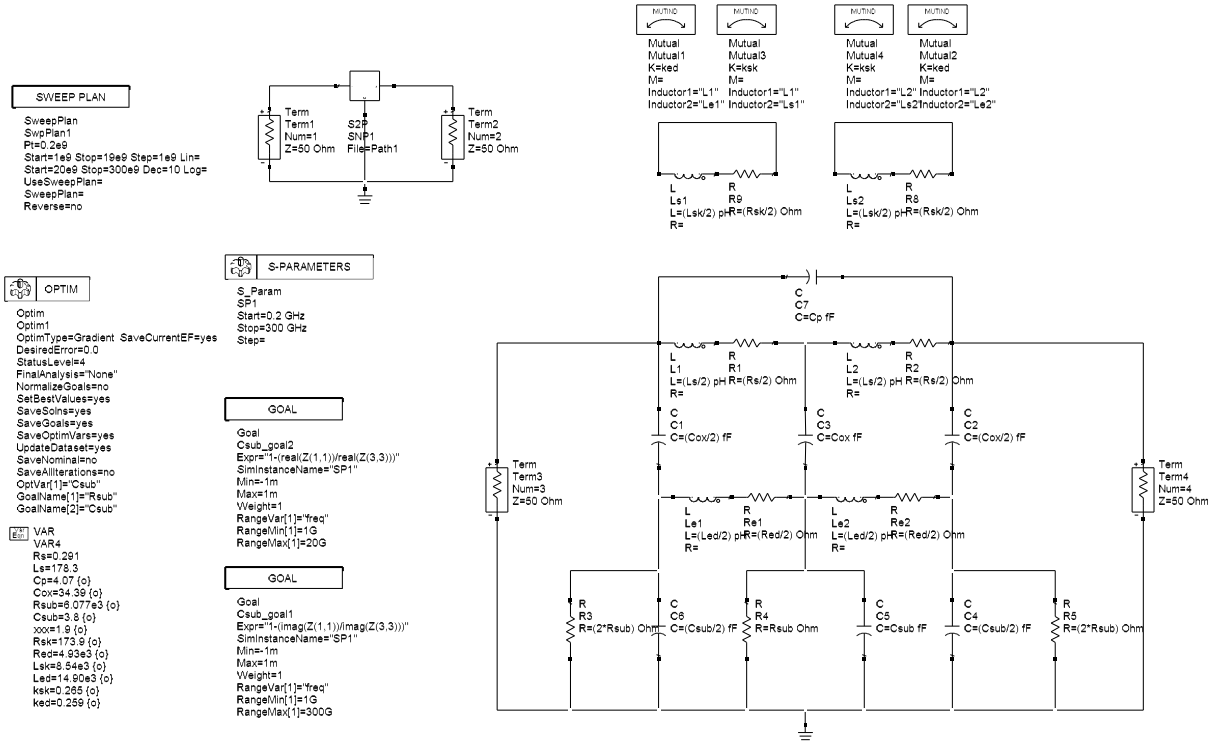


Figure 1.14 Example of a ADS OPTIM setup.

In the follow I tried to summarize the steps to follow to accomplish the fitting of the model. Nevertheless, before proceeding I would highlight that is impossible to write a general procedure valid for any inductor, and the following steps should be interpret as a guideline based on my personal experience[4]. However I think that this work could be very useful for anyone that has to model an inductor, helping him to save lots of time.

The first parameter to fit is the substrate capacitance C_{sub} because it is sufficiently independent from all the other components. Then it can be accurately fitted even though the others components are not optimized yet. To fit it we have to:

- Set $L_{ed} = L_{sk} = L_s$, $R_{ed} = R_{sk} = R_s$, $k_{ed} = k_{sk} = 0.5$;
- set a reasonable value for C_p in order to obtain a resonant frequency close to the one given by the EM simulation;
- instantiate two goals components $C_{sub-goal1}$ and $C_{sub-goal2}$, with optimization functions:

$$1 - \frac{\mathrm{Im}[Z_{11}]}{\mathrm{Im}[Z_{33}]} \tag{1.27}$$

[4]I had to model different single turn inductors, with external diameter smaller than $200\mu m$

and

$$1 - \frac{\mathrm{Re}[Z_{11}]}{\mathrm{Re}[Z_{33}]} \tag{1.28}$$

respectively. Set the range of frequency to be coincident to the whole range of frequency of the EM simulation, and Min $= -1e-3$, Max $= 1e-3$;

- in the OPTIM component, set C_{sub} as OptVar, and $C_{sub-goal1}$ and $C_{sub-goal2}$ as OptGoals;
- run a simulation using Gradient as optimization Type;
- in the same chart, plot Im $\left[\frac{-1/Y_{12}(\omega)}{\omega}\right]$, and Im $\left[\frac{-1/Y_{34}(\omega)}{\omega}\right]$ and recursively simulate, manually adjusting the value of C_p until the resonance frequencies between model and EM simulation are similar.

Following these first step we obtain the right value of C_{sub} and a coarse value of C_p. The next step is to determinate a coarse value for L_{ed}, R_{ed}, k_{ed}, L_{sk}, R_{sk}, and k_{sk}. All these components directly impact the series inductance and resistance values of the inductor and, as a consequence, its quality factor. Then:

- define three goal components: L_{s-goal}, R_{s-goal}, and Q_{goal}, whose optimization function are respectively:

$$1 - \frac{\mathrm{Im}[Z_{11} + Z_{22} - 2Z_{12}]}{\mathrm{Im}[Z_{33} + Z_{44} - 2Z_{34}]} \tag{1.29}$$

$$1 - \frac{\mathrm{Re}[Z_{11} + Z_{22} - 2Z_{12}]}{\mathrm{Re}[Z_{33} + Z_{44} - 2Z_{34}]} \tag{1.30}$$

$$1 - \frac{\mathrm{Im}[Z_{11} + Z_{22} - 2Z_{12}]}{\mathrm{Im}[Z_{33} + Z_{44} - 2Z_{34}]} \cdot \frac{\mathrm{Re}[Z_{33} + Z_{44} - 2Z_{34}]}{\mathrm{Im}[Z_{11} + Z_{22} - 2Z_{12}]} \tag{1.31}$$

- Set the range of frequency to be coincident to the whole range of frequency of the EM simulation, and Min $= -1e-3$, Max $= 1e-3$;
- in the OPTIM component, set L_{ed}, R_{ed}, k_{ed}, L_{sk}, R_{sk}, and k_{sk} as OptVar, and L_{s-goal}, R_{s-goal}, and Q_{goal} as OptGoals;
- set a range of variation of at least three decades for the variables L_{ed}, R_{ed}, k_{ed}, L_{sk}, R_{sk}, and k_{sk}.
- run a simulation using Gradient as optimization Type

- in three different plots compare the value of $\frac{\mathrm{Im}[Z_{11}+Z_{22}-2Z_{12}]}{\omega}$ with $\frac{\mathrm{Im}[Z_{33}+Z_{44}-2Z_{34}]}{\omega}$, the value of $\frac{\mathrm{Re}[Z_{11}+Z_{22}-2Z_{12}]}{\omega}$ with $\frac{\mathrm{Re}[Z_{33}+Z_{44}-2Z_{34}]}{\omega}$, and the value of $\frac{\mathrm{Im}[Z_{11}+Z_{22}-2Z_{12}]}{\mathrm{Re}[Z_{11}+Z_{22}-2Z_{12}]}$ with $\frac{\mathrm{Im}[Z_{33}+Z_{44}-2Z_{34}]}{\mathrm{Re}[Z_{33}+Z_{44}-2Z_{34}]}$.

- recursively simulate. At the end of each simulation use the final value of the variables as initial value of the next simulation.

- sometime the optimization can diverge. To prevent this always check the curves in the plots and manually adjust the range of variation of the variable if they start to diverge. Once in a while, performing simulations with Random as optimization Type can help too. Remember that in this step we just want to obtain a coarse fitting. So, once the curves are quite similar, we can proceed with the next step.

In the next step we try to perform the fine fitting for all the variable, but k_{sk}. Remember that k_{sk} is used in the network that simulate the skin effect. Then we can already expect that the fitting will not be good in the range of frequency where the skin effect is preponderant.

- In the OPTIM component, from the list of variable already set in the previous step, add C_p and remove k_{sk};

- look at the curves in the three plots we created before. Identify the range of frequency where the curves match less (usually this happens at the points where the derivative is higher);

- add new goals with the same functions defined in (1.29)-(1.31) but set their range of frequency only around the frequencies where the curves match less. This is just a general advice because it is impossible to know *a priori* the exact range of frequencies for the new goals. Sometime it is better to define a goal for every point where the curves are far each other. Other time it is better to gather two or more points inside one goal defined in a larger range of frequencies. Nevertheless it is sufficient to run just few simulations to understand if the range of frequency chosen for the new goals was right or not;

- keep simulating recursively. After each simulation use the final value of the variables as initial value for the next simulation. To obtain better result try to reduce the value of Min and Max of the goals but it is a good rule to do not use value smaller than $1e-6$ in absolute value.

The very last step is to find the final value for k_{sk}:

- in the OPTIM component, set only L_{sk}, R_{sk}, and k_{sk} as OptVar;
- recursively simulate using the same goal defined in the previously set of instruction;
- if is difficult to obtain a good agreement between the curves add some goals defined in the range of frequencies where the skin effect is bigger.

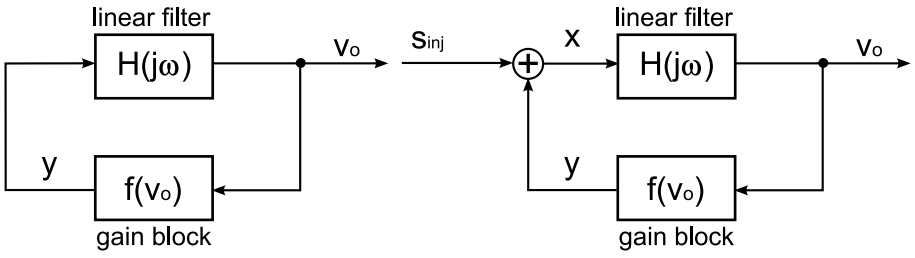
Chapter 2

Injection Locking Oscillators

Oscillator injection locking is a well know and deeply studied phenomenon. When an external signal is applied to an oscillator, the latter stops to be an autonomous circuit and synchronizes to the external signal. The conditions under which this happens have been investigated by Adler in 1946 [18], and since then by many other authors, more recently in [19–22].

2.1 Introduction

Consider the conceptual block of a free-running oscillator shown in Fig. 2.1(a): it consist of a gain block $f(v_0)$ and a linear filter $h(t)$. The Barkausen's amplitude and phase criterions define the conditions under which the oscillation can be sustained at a given



(a) (b)

Figure 2.1 (a) Block diagram of a free-running oscillator. (b Block diagram of an injection locked oscillator.

frequency ω. Those conditions are respectively:

$$|F(\omega')H(\omega)| = 1 \tag{2.1}$$

$$\angle F(\omega')H(\omega) = 2\pi \tag{2.2}$$

where $F(\omega)$ and $H(\omega)$ are the transfer function of the filter and the gain block respectively. Suppose that the gain block is capable to set its gain in such a way that (2.1) can be satisfy at any frequency, then oscillation happens at the frequency ω_0 where the phase of the filter satisfies (2.2). ω_0 is the oscillator natural frequency, that is the oscillation frequency of the oscillator when any external signal is applied to it.

Consider now the case drawn in Fig. 2.1(b) where an external signal s_{inj} at frequency ω_{inj} is applied to the oscillator. The signal X that feeds the linear filter is the vector sum of the feedback signal Y and the injection signal s_{inj}. Then the total phase shift across the loop at ω_0 is not any longer 2π, because of the extra phase shift introduced by s_{inj}, and the oscillation cannot be sustained at that frequency. However, under particular conditions the phase response of the filter at the frequency ω_{inj} compensates this extra phase shift and the Barkhausen's phase criterion is satisfied at ω_{inj}, instead of ω_0. We say that the oscillator is injection locked by s_{inj} and its oscillation frequency moves from the natural frequency ω_0 to the injection frequency ω_{inj} [18, 20]. The range of frequencies $\omega_0 \pm \omega_L$ where synchronization occurs defines the locking range of the oscillator. ω_L depends on the strength of the injecting signal s_{inj}, and on how much the filer is selective, and usally results in a small fraction of ω_0. If ω_{inj} lies outside the locking range, we say that the oscillator is injection pulled and spurious tones at frequencies $\omega_{\text{inj}} \pm k\omega_b$[1], $\omega_b = \sqrt{(\omega_0 - \omega_{\text{inj}})^2 - \omega_L^2}$, appear at the output of the oscillator [20].

If we assume that the oscillator can bear the presence of harmonics, the concept of injection locking can be further exploited. It is enough to assume that the synchronization signal is either a harmonic of the external signal, or the result of the mixing between the external signal and a harmonic of the oscillator output. In the former case we say that the oscillator is sub-harmonic injection locked, in the latter we say that it is super-harmonic injection locked.

- *Sub-harmonic injection locking:*

  Consider the case shown in Fig. 2.2(a) where the external tone s_i at frequency ω_i is processed by a non linear block g before being applied to the oscillator. The output

[1]The sign of the sum is positive if $\omega_{\text{inj}} < \omega_0 - \omega_L$, negative if $\omega_{\text{inj}} > \omega_0 + \omega_L$.

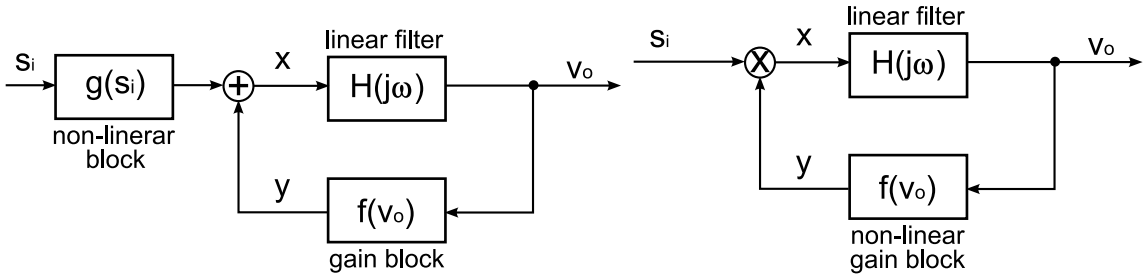


Figure 2.2 (a) block diagram of a sub-harmonic injection locked oscillator. (b) Block diagram of super-harmonic injection locked oscillator.

of the non-linear block can be express as polynomial series of the form:

$$g(s_i) = \sum_{k=0}^{\infty} b_k s_i^k \tag{2.3}$$

and contains tones at frequencies $k\omega_i$. Assume that $\omega_i \ll \omega_0$, and that the filter suppresses all the frequencies far from ω_0. If for some integer k, $k\omega_i$ lies inside the locking range $\omega_0 \pm \omega_L$, then the oscillator locks to the frequency $\omega_{\text{inj}} = k\omega_i$. We say that it is sub-harmonic injection locked and it acts as a frequency multiplier, since the oscillation frequency is k-times the synchronization frequency.

- *Super-harmonic injection locking:*

  Consider now the complementary case where $\omega_0 \ll \omega_i$ and suppose that the non-linear element is the gain block $f(v_0)$, as illustrated in Fig. 2.2(b) . Similar to what we did for $g(s_i)$, we express $f(v_0)$ as polynomial series of the form:

$$f(v_0) = \sum_{k=0}^{\infty} a_k v_0^k \tag{2.4}$$

  The output of the mixer reads as:

$$s_i \cdot f(v_0) = s_i \cdot \sum_{k=0}^{\infty} a_k v_0^k \tag{2.5}$$

  and contains tones at frequencies $|\omega_i \pm k\omega_0|$. If for some integer k, $|\omega_i \pm k\omega_0|$ lies inside the locking range $\omega_0 \pm \omega_L$, then the oscillator will lock at the frequency $\omega_{\text{inj}} = \omega_i / |1 \mp k|$. We say that the oscillator is super-harmonic injection locked and it acts as a frequency divider. To fix the idea suppose the synchronization signal frequency is $\omega_i = 4\omega_{\text{inj}}$ and that $|\omega_{\text{inj}} - \omega_0| < \omega_L$. Then both 3^{rd} and 5^{th} harmonic

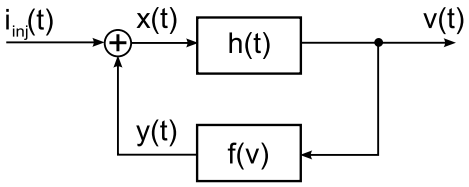


Figure 2.3 Conceptual block diagram of an injection locked oscillator.

of v_0 produce a term at frequency ω_{inj} at the output of the mixer, that locks the oscillator at the frequency $\omega_{\text{inj}} = \omega_i/4$.

In the following of the chapter the mechanism of injection locking will be deeply investigate both for LC and ring oscillators. For the LC oscillator we investigated the locking transient and the response of the system in presence of a multi-tones synchronization signal, while for the ring oscillator we first derived the locking range expression, then we analyzed the injection locking mechanism when the oscillator is super-harmonic injection locked and it behaves as a frequency divider.

2.2 LC oscillators under injection locking

2.2.1 Locking range derivation

The LC injection locked oscillator can be modeled as a feedback system where the forward path is linear and represents the LC tank impedance, while the feedback path is highly non-linear, and it represents the active element (e.g. a transconductor) characteristics, as sketched in Fig. 2.3. When the oscillator is locked, the signals are described in the time domain as:

$$i_{\text{inj}}(t) = A_i e^{j(\omega_i t + \Psi)} \tag{2.6}$$

$$v(t) = A_v e^{j\omega_{\text{inj}} t} \tag{2.7}$$

$$y(t) = f(v(t)) \tag{2.8}$$

$$x(t) = i_{\text{inj}}(t) + y(t) \tag{2.9}$$

where $i_{\text{inj}}(t)$ and $v(t)$ are the synchronization signal (a current) and the oscillator output voltage, respectively, $y(t)$ is the current output by the non-linear active element, and $x(t)$ is the total current injected in the tank. Ψ is the static phase difference between the input and the output in steady state. Under the hypothesis of hard switching of the active element, $f(v)$ is a non-linear function totally insensitive to the amplitude of $v(t)$ [19]. As

a consequence, $y(t)$ is written as

$$y(t) = I_1 e^{j\omega_{\text{inj}}t} + \tilde{y}(t), \tag{2.10}$$

where I_1 is the amplitude of the first harmonic of the current waveform $y(t)$ and $\tilde{y}(t)$ is the higher frequency content. Calling $h(t)$ the impulse response of the LC tank, $v(t)$ and $x(t)$ are linked by the convolution:

$$v(t) = h * x(t). \tag{2.11}$$

In the frequency domain, (2.11) is rewritten using harmonic balance as

$$A_v e^{j\omega_{\text{inj}}t} = H_{\omega_{\text{inj}}} e^{j\alpha_{\omega_{\text{inj}}}} (A_i e^{j\Psi} + I_1) e^{j\omega_{\text{inj}}t}, \tag{2.12}$$

where

$$H_{\omega_{\text{inj}}} \approx \frac{R}{\sqrt{1 + 4Q^2 \left(\frac{\omega_{\text{inj}} - \omega_0}{\omega_0}\right)^2}} \tag{2.13}$$

and

$$\alpha_{\omega_{\text{inj}}} \approx -\arctan\left(\frac{2Q(\omega_{\text{inj}} - \omega_0)}{\omega_0}\right) \tag{2.14}$$

are the magnitude and the phase, respectively, of the tank frequency response $H(\omega_{\text{inj}})$. Multiplying both sides of (2.12) by $e^{-j(\omega_{\text{inj}}t + \alpha_{\omega_{\text{inj}}})}$, setting $\phi_0 = -\alpha_{\omega_{\text{inj}}}$, and separating real and imaginary parts we write

$$A_v \cos(\phi_0) = H_{\omega_{\text{inj}}} (A_i \cos\Psi + I_1) \tag{2.15}$$

$$A_v \sin(\phi_0) = H_{\omega_{\text{inj}}} A_i \sin\Psi, \tag{2.16}$$

that are solved to get:

$$\cos\Psi = -\left(\frac{I_1}{A_i}\right)\sin^2\phi_0 \pm \cos\phi_0 \sqrt{1 - \left(\frac{I_1}{A_i}\right)^2 \sin^2\phi_0} \tag{2.17}$$

$$A_v = H_{\omega_{\text{inj}}} \left(I_1 \cos\phi_0 \pm A_i \sqrt{1 - \left(\frac{I_1}{A_i}\right)^2 \sin^2\phi_0} \right) \tag{2.18}$$

As discussed in [19], only one of the two modes of operation described by (2.17) and (2.18) is stable, namely the one corresponding to smaller angle Ψ and larger amplitude A_v. Notice that (2.17) and (2.18) are only valid for

$$|\sin\phi_0| \leq \frac{A_i}{I_1} \tag{2.19}$$

where the equality condition sets the maximum deviation of the injected frequency from the tank natural frequency for the lock to occur, that is the so-called locking range. Approximating

$$\phi_0 \approx \tan\phi_0 \approx \frac{2Q(\omega_{\text{inj}} - \omega_0)}{\omega_0}, \tag{2.20}$$

the unilateral locking range ω_L is finally derived combining (2.14) and (2.19) as [20]:

$$\omega_L = \max_{\omega_{\text{inj}}} |\omega_{\text{inj}} - \omega_0| = \frac{\omega_0}{2Q}\frac{A_i}{I_1}\frac{1}{\sqrt{1 - \left(\frac{A_i}{I_1}\right)^2}}. \tag{2.21}$$

When normalized to ω_0 equation (2.21) clearly shows that the locking range results proportional to the ratio A_i/I_1 and inversely proportional to the quality factor Q of the oscillator, i.e. to increase the locking range of the oscillator we have to increase either the strength of the injection signal or the band of the LC filter.

2.2.2 Spurious tones

The operation of an oscillator subject to the injection of a signal laying outside the locking range has been analyzed in [18, 20], and the rise of spurious tones in quasi-lock and fast beat conditions has been described. In our analysis, however, we want to investigate the response of the oscillator in presence of spurious tones of synchronization signal. To do so we follow a perturbative approach, assuming that the spurious tones that arise on the oscillator output can be regarded as amplitude ($a_v(t)$) and phase ($\phi_v(t)$) modulation of the locked oscillation. Moreover, we assume that the modulation indexes are low enough such that:

$$\begin{aligned} v(t) &= A_v(1 + a_v(t))e^{j(\omega_{\text{inj}}t + \phi_v(t))} \\ &\approx A_v[1 + a_v(t) + j\phi_v(t)]e^{j(\omega_{\text{inj}}t)}. \end{aligned} \tag{2.22}$$

As discussed in Sec. 2.2.1 the feedback element suppresses any amplitude modulation. However, it is sensitive to the phase modulation of $v(t)$, which is transferred to $y(t)$. Without lack of generality, the spurious tones of the injection signal can be seen as multi-tone SSB modulation of the desired one:

$$x(t) = A_i[1 + b_i(t) + jb_q(t)]e^{j(\omega_{\text{inj}}t + \Psi)} \tag{2.23}$$

where $b_i(t)$ and $b_q(t)$ are real in-phase and quadrature base-band components representing the undesired tones in the synchronization signal. To gain insight into (2.23), recall that to represent, for example, a spur with the same amplitude of the tone that locks the

oscillator, lying at a frequency offset ω_m from it, we must set $b_i(t) = \cos(\omega_m t)$ and $b_q(t) = \sin(\omega_m t)$. The total tank current is than express by:

$$x(t) \approx A_i[1 + b_i(t) + jb_q(t)]e^{j(\omega_{\text{inj}}t+\Psi)} + I_1[1 + j\phi_v(t)]e^{j(\omega_{\text{inj}}t)}. \tag{2.24}$$

Since we are mainly interested in the spectrum of $v(t)$, we switch to the frequency domain to exploit the fact that (2.11) simply reads as

$$V(f_i + f_m) = H(f_i + f_m) \cdot X(f_i + f_m). \tag{2.25}$$

Moreover, we consider the complex envelopes of the signals (in particular $H_C(f_m) = H(f_i + f_m)$) and we make use of the symmetries of the Fourier transform[2] to recast (2.25) for any frequency offset $|f_m| > 0$ from the locked oscillation frequency f_i as

$$\begin{aligned} &A_v[A_{ve}(f_m) + jA_{vo}(f_m) + j\Phi_{ve}(f_m) - \Phi_{vo}(f_m)] = \\ &= H_C(f_m)\left\{A_i[B_{ie}(f_m) + jB_{io}(f_m) + jB_{qe}(f_m) - B_{qo}(f_m)]e^{j\Psi}\right. \\ &\quad \left. + I_1[j\Phi_{ve}(f_m) - \Phi_{vo}(f_m)]\right\}, \end{aligned} \tag{2.26}$$

where A_{ve} and B_{ie} are the Fourier transforms of the even-symmetry components of $a_v(t)$ and $b_i(t)$, respectively, while jA_{vo} and jB_{io} refer to the transforms of the odd-symmetry components. Similarly, Φ_{ve}, B_{qe}, and $j\Phi_{vo}$, jB_{qo} are the Fourier transforms of the even- and odd-symmetry components of $\phi_v(t)$ and $b_q(t)$. Evaluated at $-f_m$ (2.26) reads as

$$\begin{aligned} &A_v[A_{ve}(f_m) - jA_{vo}(f_m) + j\Phi_{ve}(f_m) + \Phi_{vo}(f_m)] = \\ &= H_C(-f_m)\left\{A_i[B_{ie}(f_m) - jB_{io}(f_m) + jB_{qe}(f_m) + B_{qo}(f_m)]e^{j\Psi}\right. \\ &\quad \left. + I_1[j\Phi_{ve}(f_m) + \Phi_{vo}(f_m)]\right\}. \end{aligned} \tag{2.27}$$

For each offset frequency $|f_m|$, (2.26) and (2.27) are two linearly independent complex equations in four real unknowns. Taking the sum and difference of (2.26) and (2.27), and separating real and imaginary parts, we define a linear system in the form:

$$\mathbf{A}\begin{bmatrix}\Phi_{ve}\\ \Phi_{vo}\\ A_{ve}\\ A_{vo}\end{bmatrix} = \mathbf{B}\begin{bmatrix}B_{qe}\\ B_{qo}\\ B_{ie}\\ B_{io}\end{bmatrix} \tag{2.28}$$

[2]The time-domain signal is decomposed into even-symmetry and odd-symmetry parts; the Fourier transform of the even part is real and even, while the transform of the odd part is pure imaginary and odd.

being

$$\mathbf{A} = \begin{bmatrix} I_1\Im\{\Sigma_H\} & I_1\Re\{\Delta_H\} & 2A_v & 0 \\ 2A_v - I_1\Re\{\Sigma_H\} & I_1\Im\{\Delta_H\} & 0 & 0 \\ I_1\Im\{\Delta_H\} & -2A_v + I_1\Re\{\Sigma_H\} & 0 & 0 \\ -I_1\Re\{\Delta_H\} & I_1\Im\{\Sigma_H\} & 0 & 2A_v \end{bmatrix}, \tag{2.29}$$

and

$$\mathbf{B} = A_i \begin{bmatrix} b_{11} & -b_{41} & b_{21} & b_{31} \\ b_{21} & b_{31} & -b_{11} & b_{41} \\ b_{31} & -b_{21} & b_{41} & b_{11} \\ b_{41} & b_{11} & -b_{31} & b_{21} \end{bmatrix}, \tag{2.30}$$

where

$$b_{11} = -\cos\Psi \cdot \Im\{\Sigma_H\} - \sin\Psi \cdot \Re\{\Sigma_H\} \tag{2.31}$$
$$b_{21} = \cos\Psi \cdot \Re\{\Sigma_H\} - \sin\Psi \cdot \Im\{\Sigma_H\} \tag{2.32}$$
$$b_{31} = -\cos\Psi \cdot \Im\{\Delta_H\} - \sin\Psi \cdot \Re\{\Delta_H\} \tag{2.33}$$
$$b_{41} = \cos\Psi \cdot \Re\{\Delta_H\} - \sin\Psi \cdot \Im\{\Delta_H\} \tag{2.34}$$

and $\Sigma_H = H_C(f_m) + H_C(-f_m)$, $\Delta_H = H_C(f_m) - H_C(-f_m)$.

Inverting $\mathbf{A}$ we get:

$$\mathbf{A}^{-1} = \frac{1}{\det\mathbf{A}} \begin{bmatrix} 0 & a & b & 0 \\ 0 & b & -a & 0 \\ c & d & e & 0 \\ 0 & e & -d & c \end{bmatrix}, \tag{2.35}$$

where

$$\det\mathbf{A} = -4A_v^2[(2A_v - I_1\Re\{\Sigma_H\})^2 + I_1^2(\Im\{\Delta_H\})^2] \tag{2.36}$$
$$a = 4A_v^2(-2A_v + I_1\Re\{\Sigma_H\}) \tag{2.37}$$
$$b = -4A_v^2 I_1\Im\{\Delta_H\} \tag{2.38}$$
$$c = -2A_v[(2A_v - I_1\Re\{\Sigma_H\})^2 + I_1^2(\Im\{\Delta_H\})^2] \tag{2.39}$$
$$d = 2A_v[(2A_v - I_1\Re\{\Sigma_H\})I_1\Im\{\Sigma_H\} + I_1^2\Re\{\Delta_H\}\Im\{\Delta_H\}] \tag{2.40}$$
$$e = 2A_v[I_1^2\Im\{\Sigma_H\}\Im\{\Delta_H\} - I_1\Re\{\Delta_H\}(2A_v - I_1\Re\{\Sigma_H\})] \tag{2.41}$$

The important thing of the foregoing calculation is that, by using (2.30) and (2.35),

one can easily see that $\mathbf{M} = \mathbf{A}^{-1}\mathbf{B}$ has the following form:

$$\mathbf{M} = \begin{bmatrix} m_{11} & m_{12} & m_{13} & m_{14} \\ -m_{12} & m_{11} & -m_{14} & m_{13} \\ m_{31} & m_{32} & m_{33} & m_{34} \\ -m_{32} & m_{31} & -m_{34} & m_{33} \end{bmatrix} \tag{2.42}$$

As a consequence, we can recast (2.28) into:

$$\begin{bmatrix} \Phi_{ve} + j\Phi_{vo} \\ A_{ve} + jA_{vo} \end{bmatrix} = \underbrace{\begin{bmatrix} T_{\text{PM-Q}} & T_{\text{PM-I}} \\ T_{\text{AM-Q}} & T_{\text{AM-I}} \end{bmatrix}}_{\mathbf{T}} \begin{bmatrix} B_{qe} + jB_{qo} \\ B_{ie} + jB_{io} \end{bmatrix} \tag{2.43}$$

where the entries of the 2×2 matrix $\mathbf{T}$ are the input-output modulation transfer functions.

To gain insight in the understanding of the spurs response of the system we now present a simplify analysis of (2.42) in the case of a single spur tone, and $\omega_{\text{inj}} \approx \omega_0$, under two different hypothesis. The first is that the spur lies far from the LC filter band, that is $\omega_m \gg \frac{\omega_0}{2Q}$, the second is that the spur lies inside the band of the LC tank, that is $\omega_m \ll \frac{\omega_0}{2Q}$.

Out-of-band modulating signal

If we can assume that $2\pi f_m \gg \frac{\omega_0}{2Q}$ and $\omega_{\text{inj}} \approx \omega_0$, then $\Sigma_H = 0$, $\Delta_H \approx -j2\frac{R\omega_0}{2Q\omega_m} = -j2R\delta_H$,

$$\mathbf{A}^{-1} = \frac{-1}{2A_v^2\left[A_v^2 + I_1^2R^2\delta_H^2\right]} \cdot \cdot \begin{bmatrix} 0 & -A_v^3 & A_v^2I_1R\delta_H & 0 \\ 0 & A_v^2I_1R\delta_H & A_v^3 & 0 \\ -A_v\left[A_v^2 + I_1^2R^2\delta_H^2\right] & 0 & 0 & 0 \\ 0 & 0 & 0 & -A_v\left[A_v^2 + I_1^2R^2\delta_H^2\right] \end{bmatrix} \tag{2.44}$$

and

$$\mathbf{B} = A_i \begin{bmatrix} 0 & 0 & 0 & 2R\delta_H \\ 0 & 2R\delta_H & 0 & 0 \\ 2R\delta_H & 0 & 0 & 0 \\ 0 & 0 & -2R\delta_H & 0 \end{bmatrix} \tag{2.45}$$

As a consequence,

$$\mathbf{M} = \begin{bmatrix} -\frac{I_1 A_i R^2 \delta_H^2}{A_v^2 + I_1^2 R^2 \delta_H^2} & \frac{A_v A_i R \delta_H}{A_v^2 + I_1^2 R^2 \delta_H^2} & 0 & 0 \\ -\frac{A_v A_i R \delta_H}{A_v^2 + I_1^2 R^2 \delta_H^2} & -\frac{I_1 A_i R^2 \delta_H^2}{A_v^2 + I_1^2 R^2 \delta_H^2} & 0 & 0 \\ 0 & 0 & 0 & \frac{A_i R \delta_H}{A_v} \\ 0 & 0 & -\frac{A_i R \delta_H}{A_v} & 0 \end{bmatrix} \tag{2.46}$$

that can be recast as

$$\mathbf{M} \approx \frac{A_i}{I_1} \begin{bmatrix} -\alpha^2 & \alpha & 0 & 0 \\ -\alpha & -\alpha^2 & 0 & 0 \\ 0 & 0 & 0 & \alpha \\ 0 & 0 & -\alpha & 0 \end{bmatrix}. \tag{2.47}$$

where

$$\alpha = \frac{1}{1 + \frac{A_i}{I_1}} \cdot \frac{\omega_0}{2Q\omega_m}. \tag{2.48}$$

Now, if the synchronization signal is made of the desired harmonic plus a spurious tone both with equal amplitude, we have, for example, $B_{qe}(\pm\omega_m) = 0$, $B_{qo}(\pm\omega_m) = \mp 0.5$, $B_{ie}(\pm\omega_m) = 0.5$, and $B_{io}(\pm\omega_m) = 0$. Equation (2.47) shows that all the spurious output modulation is proportional to A_i/I_1, meaning that the lower the amplitude of the synchronization signal, the lower the output spurious tones. It also says that the SSB modulation is transferred to $v(t)$ as SSB modulation[3], the side-band being attenuated by the resonator normalized transfer function $\omega_0/(2Q\omega_m)$, and phase-shifted by 90°. Moreover, $v(t)$ shows an additional phase modulation, which arises from the diagonal elements of $\mathbf{M}$, and results in symmetric side-bands with lower amplitude. The lower side-band (LSB) is smaller than the upper side-band (USB), the difference getting larger and larger as $|\omega_m|$ increases.

[3]Under the assumption of low AM and PM modulation indexes made in (2.22), $a_v(t)$ and $\phi_v(t)$ may also be regarded as base-band quadrature components of a SSB modulation.

In-band modulating signal

In this case we assume $2\pi f_m \ll \frac{\omega_0}{2Q}$, $\omega_{\text{inj}} \approx \omega_0$. With these symplifying hypothesis, $\Sigma_H \approx 2R$, $\Delta_H \approx 0$, $A_v \approx (A_i + I_1)R$

$$\mathbf{A}^{-1} = \frac{-1}{2A_v^2(A_v - I_1R)^2} \cdot \cdot \begin{bmatrix} 0 & -A_v^2(A_v - I_1R) & 0 & 0 \\ 0 & 0 & A_v^2(A_v - I_1R) & 0 \\ -A_v(A_v - I_1R)^2 & 0 & 0 & 0 \\ 0 & 0 & 0 & -A_v(A_v - I_1R)^2 \end{bmatrix} \tag{2.49}$$

and

$$\mathbf{B} = A_i \begin{bmatrix} 0 & 0 & 2R & 0 \\ 2R & 0 & 0 & 0 \\ 0 & -2R & 0 & 0 \\ 0 & 0 & 0 & 2R \end{bmatrix} \tag{2.50}$$

As a consequence,

$$\mathbf{M} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1-\gamma & 0 \\ 0 & 0 & 0 & 1-\gamma \end{bmatrix} \tag{2.51}$$

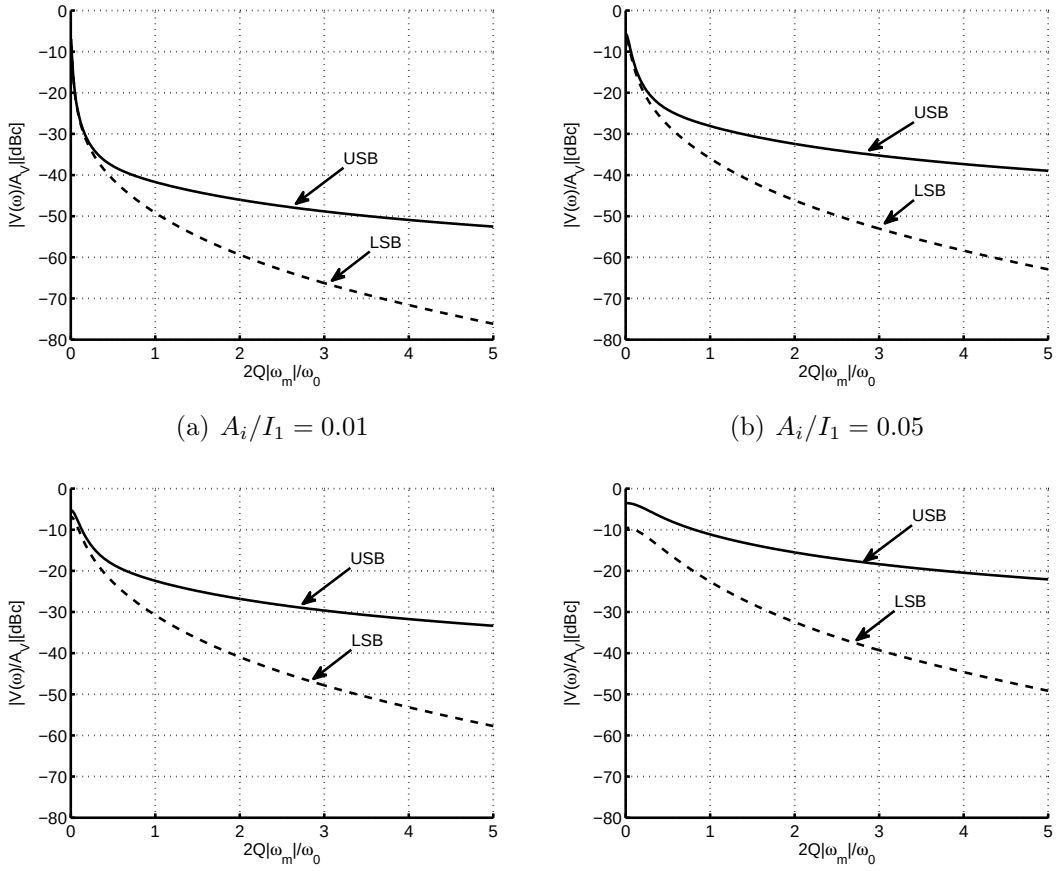
where

$$\gamma = \frac{1}{1 + A_i/I_1}. \tag{2.52}$$

The quadrature component of the input modulation is is always transferred to the phase modulation of the output with a unit transfer function. At the contrary, the in-phase modulation is transferred to the amplitude modulation of the output with a transfer function that depends on the ratio A_i/I_1. In particular if $A_i/I_1 \ll 1$, $\gamma \approx 1$ and the in-phase modulation is suppressed. Under the assumption of low AM and PM modulation indexes, this means that when $A_i/I_1 \ll 1$ the SSB modulation is transferred to $v(t)$ as double side band (DSB) modulation. A more interesting way to see the same result is assuming that also the input signal is modulated with a low modulation index:

$$i_{\text{inj}}(t) = A_i(1 + b_i(t) + jb_q(t))e^{j(\omega_{\text{inj}}t+\Psi)} \approx A_i(1 + b_i(t))e^{j(\omega_{\text{inj}}t+b_q(t)+\Psi)} \tag{2.53}$$

In this contest (2.51) shows that only the phase modulation of the input is transfer to the phase modulation of the output, with unit transfer function. This also explain why the phase noise of an injection locked oscillators is equal to the phase noise of the input signal inside the locking range of the oscillator.



(a) $A_i/I_1 = 0.01$ (b) $A_i/I_1 = 0.05$

(c) $A_i/I_1 = 0.1$ (d) $A_i/I_1 = 0.5$

Figure 2.4 Normalised side-bands of $|V(\omega)|$ at ω_m (USB) and $-\omega_m$ (LSB) frequency offset, generated by a single tone input at $+\omega_m$ offset.

Simulation results

In order to achieve a complete picture of the response of an injection locked oscillator in presence of spurious tones of the injecting signal, we present the results of some matlab simulations carried out using the exact formula for $\mathbf{M}$. We first analyze the case of a single SSB modulation of the input.

Fig. 2.4 illustrate the normalized side-bands of $|V(\omega)|$ at $\pm\omega_m$ frequency offset, generate by a single tone input at $+\omega_m$ offset. Simulations confirm that for $2\pi f_m \ll \frac{\omega_0}{2Q}$, the lower the ratio A_i/I_1 the more the in-phase modulation of the input is attenuated, and the more the SSB modulation is transferred to $v(t)$ as double side band (DSB) modulation. Equivalent, under the small modulation indexes approximation, the smaller the ratio A_i/I_1 the greater the AM modulation of the input is attenuated. Simulations also

confirm that, for $2\pi f_m \gg \frac{\omega_0}{2Q}$, all the spurious output modulation is proportional to A_i/I_1 meaning that, the lower the amplitude of the synchronization signal, the lower the output spurious tones. Moreover the lower side-band (LSB) is smaller than the upper side-band (USB), the difference getting larger and larger as $|\omega_m|$ increases.

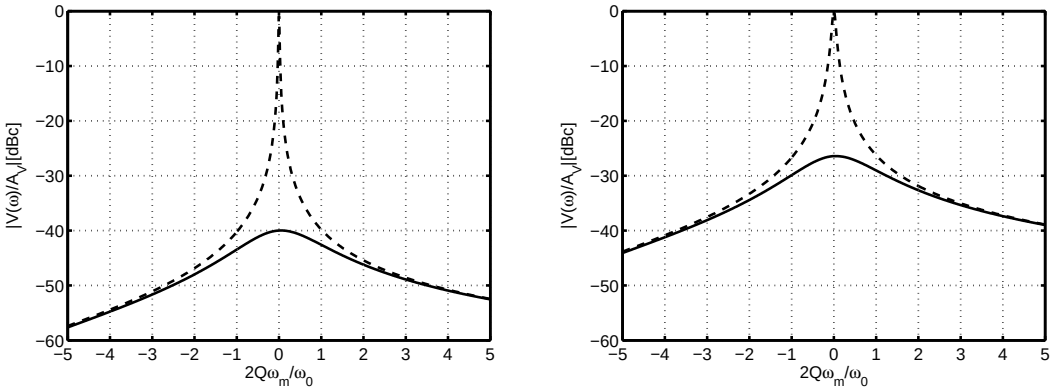
The case of a multi spurious tones is addressed by means of superposition, since the problem has been linearized, as shown by (2.28). In particular, the presence of two tones at $\pm\omega_m$ offset is of interest. More specifically, it is worth to consider the case the tones are represented by an in-phase base-band equivalent only ($b_q(t) = 0$), or by a quadrature base-band equivalent only ($b_i(t) = 0$). Considering the following equivalence:

$$\begin{aligned} A_{\text{lsb}}e^{j(\omega_{\text{inj}}-\omega_m)t} + A_i e^{j\omega_{\text{inj}}t} + A_{\text{usb}}e^{j(\omega_{\text{inj}}+\omega_m)t} = \\ = A_i e^{j\omega_{\text{inj}}t}\left[1 + \frac{A_{\text{usb}} + A_{\text{lsb}}}{A_i}\cos(\omega_m t) + j\frac{A_{\text{usb}} - A_{\text{lsb}}}{A_i}\sin(\omega_m t)\right] \end{aligned} \tag{2.54}$$

the former case arises when the two tones are in-phase, the latter when they are out-of-phase. Figure 2.5 shows the resulting output spectrum. For $\omega_m \gg \frac{\omega_0}{2Q}$ there is basically no difference between the two curves and all the spurious output modulation is proportional to A_i/I_1. On the other hands, for $\omega_L < \omega_m < \omega_0/(2Q)$, the case of out-of-phase input tones results in higher output side-bands. Such a behavior is readily explained by observing that $T_{33} = T_{44} = 0$.

So far, we assumed $\omega_{\text{inj}} - \omega_0 = \Delta\omega_0 \approx 0$. As ω_{inj} moves away from the tank natural frequency, the behavior of the system changes depending on the case the two tones are in-phase or out-of-phase. In the former case, illustrated in Fig. 2.6, as $\Delta\omega_0$ is increased the USB increases, becoming closer and closer to the USB of the two out-of-phase input tones case, while the LSB decreases. In the latter case, illustrated in Fig. 2.7, as $\Delta\omega_0$ is increased the USB decreases , while the LSB does not changes appreciably. For both the cases symmetrical results are obtained if $\Delta\omega_0$ is made negative.

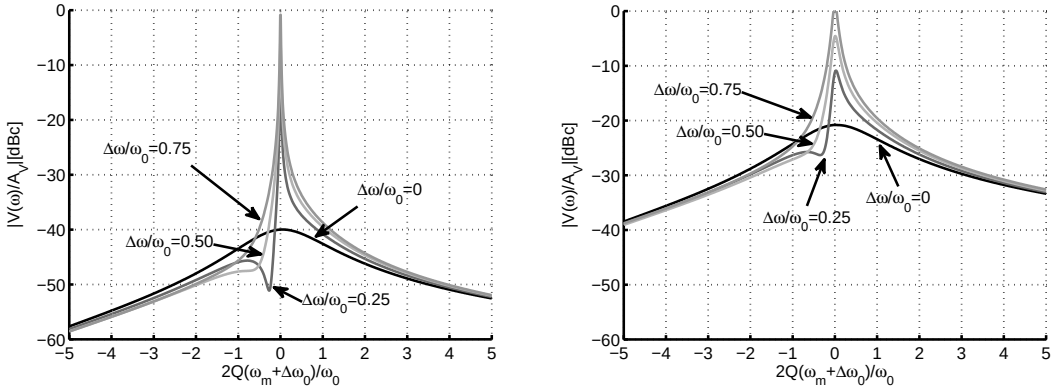
Summarizing, the analysis demonstrates while in the case of a single spurs is quite simple to predict the response of the system, this is not true in the case of multi spurious tones because the response can vary a lot depending on the relative phase between the tones. Nevertheless we can affirm that, at least at the first order, the case of out-of-phase multi tones with $\Delta\omega_0 = 0$ fix an upper limit condition. In general we can conclude that for a given relative signal level A_i/I_1, one can pursue two strategies to keep the spurious tones at the output of the oscillator low: on one hand one can rely on a highly selective, high-Q LC tank. Alternately, one can adopt countermeasures to attenuate the undesired harmonics directly at the source.



(a) $A_i/I_1 = 0.01$ (b) $A_i/I_1 = 0.05$

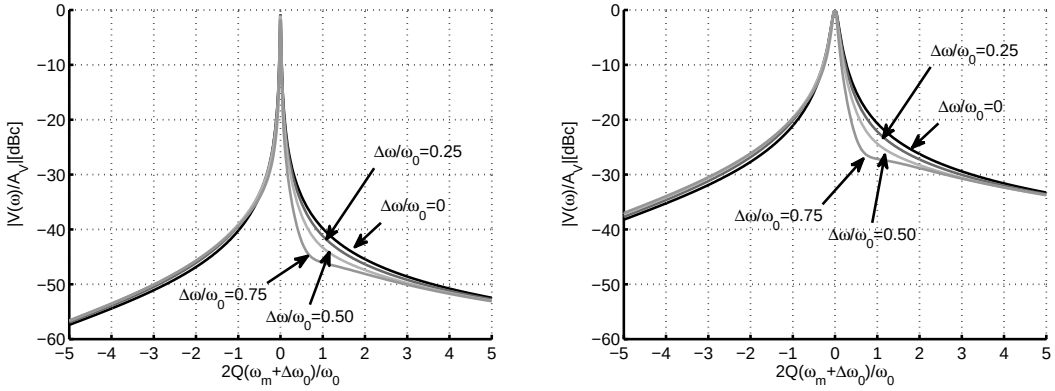
(c) $A_i/I_1 = 0.1$ (d) $A_i/I_1 = 0.5$

Figure 2.5 Normalized spectrum of $|V(\omega)|$ generated by two spurs tones of equal amplitude, at frequency offset $+\omega_m$ and $-\omega_m$. Continuous lines refer to the case the two tones are in-phase, dashed lines refer to the case the two tones are out-of-pahse.



(a) $A_i/I_1 = 0.01$ (b) $A_i/I_1 = 0.1$

Figure 2.6 Normalised spectrum of $|V(\omega)|$ generated by two in-phase tones of equal amplitude at frequency offset $+\omega_m$ and $-\omega_m$, for different values of $\Delta\omega_0$



(a) $A_i/I_1 = 0.01$ (b) $A_i/I_1 = 0.1$

Figure 2.7 Normalized spectrum of $|V(\omega)|$ generated by two out-of-phase tones of equal amplitude at frequency offset $+\omega_m$ and $-\omega_m$, for different values of $\Delta\omega_0$

2.2.3 Locking time

Phase transient

To study the locking transient of an injection locked LC oscillator we start form the Adler's equation [18]:

$$\frac{d\psi}{dt} = -\omega_L \left(\sin\alpha - K\right) \tag{2.55}$$

where ψ is the instantaneous phase difference between the synchronization signal and the output voltage of the oscillator and

$$K = (\omega_0 - \omega_{\text{inj}})/\omega_L = \Delta\omega_0/\omega_L \tag{2.56}$$

It is worthwhile to notice that: $K = 0$ if the frequency of the injection signal is equal to the tank natural frequency, $|K| < 1$ if the locking condition is staisfied, and $|K| > 1$ if the locking condition is not staisfied. The expression of ψ as a function of time is then obtained integrating (2.55). Let consider separately the case $K = 0$ from the case $K \neq 0$

- $K = 0$:
  (2.55) can be recast as:
  $$\frac{d\psi}{\sin\psi} = -\omega_L dt \tag{2.57}$$
  that integrated yields
  $$\psi(t) = 2\arctan\left[e^{-\omega_L\left(t-t_0-t'_{K=0}\right)}\right]\text{sign}\left(\psi_0\right) \tag{2.58}$$
  where t_0 is the initial time, ψ_0 id the initial phase difference between the injected signal and the oscillator voltage, and
  $$t'_{K=0} = \frac{1}{\omega_L}\ln\left|\tan\left(\frac{\psi_0}{2}\right)\right| \tag{2.59}$$
  is an integration constant.

- $K \neq 0$:
  (2.55) can be recast as:
  $$\frac{d\psi}{-\omega_L(\sin\psi - K)} = dt \tag{2.60}$$
  that integrated yields
  $$\psi(t) = 2\arctan\left[\frac{1+\sqrt{K^2-1}}{K}\tan\left(\frac{\omega_L\left(t-t_0-t'_{K\neq 0}\right)}{2}\sqrt{K^2-1}\right)\right] \tag{2.61}$$

where t_0 is the initial time, ψ_0 is the initial phase difference between the injected signal and the oscillator voltage, and

$$t'_{K\neq 0} = -\frac{2}{\omega_L\sqrt{K^2-1}}\arctan\left(\frac{K\tan\left(\frac{\psi_0}{2}\right)-1}{\sqrt{K^2-1}}\right) \tag{2.62}$$

is an integration constant. Of course, since we are interested in finding the locking time transient, the locking condition must be satisfied. That means that $|K| < 1$ and the sqare root term $\sqrt{K^2-1}$ becomes negative. As a consequence (2.61) can be rewrite as:

– if: $\sin\psi_0 > K$ for $K > 0$ or $\sin\psi_0 < K$ for $K < 0$:

$$\psi(t) = 2\arctan\left[\frac{1}{K} - \frac{\sqrt{1-K^2}}{K}\tanh\left(\frac{\omega_L(t-t_0-t'_A)}{2}\sqrt{1-K^2}\right)\right] \tag{2.63}$$

$$t'_A = \frac{2}{\omega_L\sqrt{1-K^2}}\tanh^{-1}\left(\frac{K\tan\left(\frac{\psi_0}{2}\right)-1}{\sqrt{1-K^2}}\right) \tag{2.64}$$

– if: $\sin\psi_0 < K$ for $K > 0$ or $\sin\psi_0 > K$ for $K < 0$:

$$\psi(t) = 2\arctan\left[\frac{1}{K} - \frac{\sqrt{1-K^2}}{K}\coth\left(\frac{\omega_L(t-t_0-t'_B)}{2}\sqrt{1-K^2}\right)\right] \tag{2.65}$$

$$t'_B = \frac{2}{\omega_L\sqrt{1-K^2}}\coth^{-1}\left(\frac{K\tan\left(\frac{\psi_0}{2}\right)-1}{\sqrt{1-K^2}}\right) \tag{2.66}$$

Frequency transient

In almost all the situations, more than in the phase transient we are interested on the frequency transient. The difference in instantaneous frequency between the reference and the output is then evaluated derivating the phase transient expressions (2.58), (2.63), and (2.65) and results:

$$\Delta\omega(t) = \frac{d\psi}{dt} = \begin{cases} \frac{-\omega_L\cdot\mathrm{sign}[\tan(\psi_0/2)]}{\cosh(X)} & \text{for } K = 0 \\ \frac{-\omega_L(1-K^2)K}{K^2\pm[\cosh(X)-\sqrt{1-K^2}\sinh(X)]} & \text{for } K \neq 0 \end{cases} \tag{2.67}$$

where

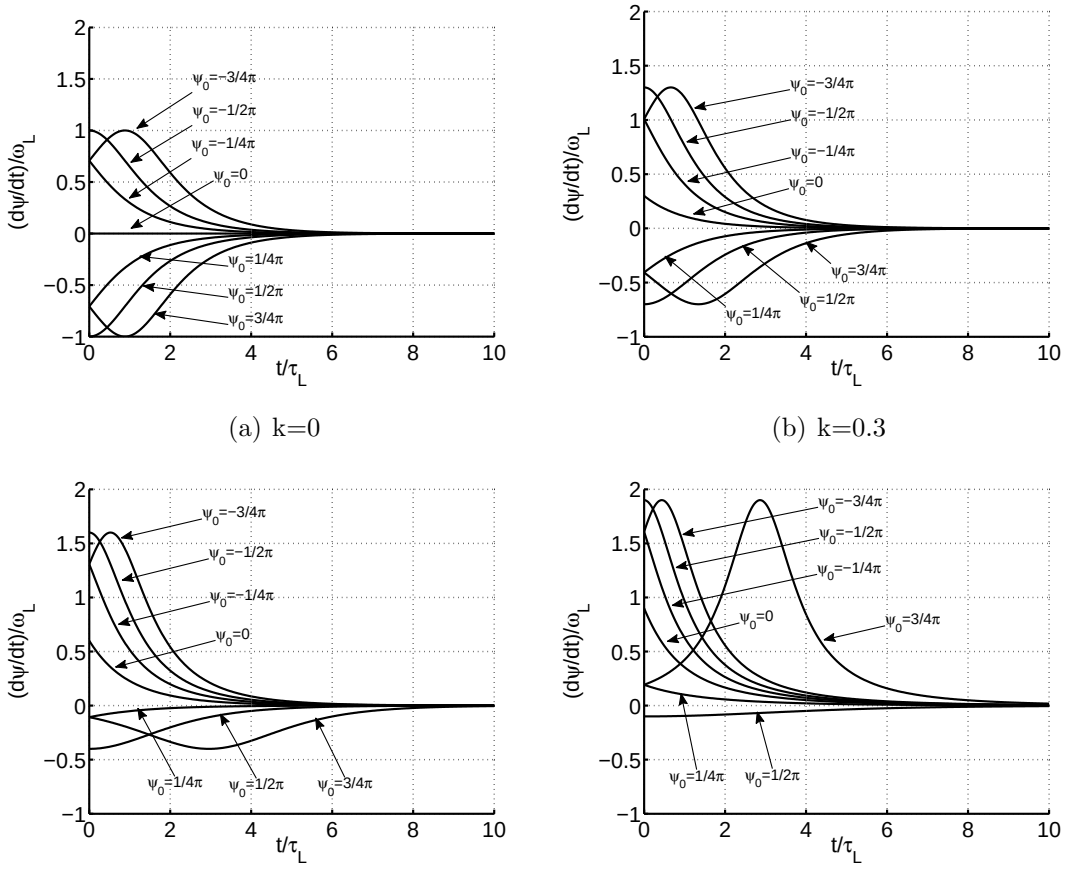
$$X = \omega_L(t-t_0-t')\sqrt{1-K^2} \tag{2.68}$$

and

$$t' = \begin{cases} t'_{k=0} & \text{if } K = 0 \\ t'_A & \text{if and } \sin\psi_0 > K \text{ for } K > 0 \text{ or } \sin\psi_0 < K \text{ for } K < 0 \\ t'_B & \text{otherwise} \end{cases} \tag{2.69}$$

is an integration constant, and the sign in the denominator of (2.67) for $K \neq 0$ is positive if $\sin\psi_0 > K$ for $K > 0$ or $\sin\psi_0 < K$ for $K < 0$, negative otherwise.

Equation (2.67) is plotted in Fig. 2.8 as a function of time for several values of ψ_0 and of K. We observe that in general the frequency transient is not monotonic and that the



(a) k=0 (b) k=0.3

(c) k=0.6 (d) k=0.9

Figure 2.8 Frequency transient of an injection locked LC oscillator for several values of $K = \Delta\omega_0/\omega_L$ and initial phase difference ψ_0 between the injection signal and the oscillator voltage

initial phase difference ψ_0 plays a significant role in determining the locking time. For a given value of K, the worst case condition is occurs when ψ_0 approaches $-\pi$ (dually for negative value of K the worst case condition occurs when ψ_0 approaches π), while among all the K values, the worst case condition is reached when K approaches the unit (i.e when we are approaching the locking range edge). In any case locking is reached within some multiples of $\tau_L = 1/\omega_L$. In fact, (2.67) reduces to a decaying exponential with characteristic time constant τ_L for $t \gg t_0 + t'$.

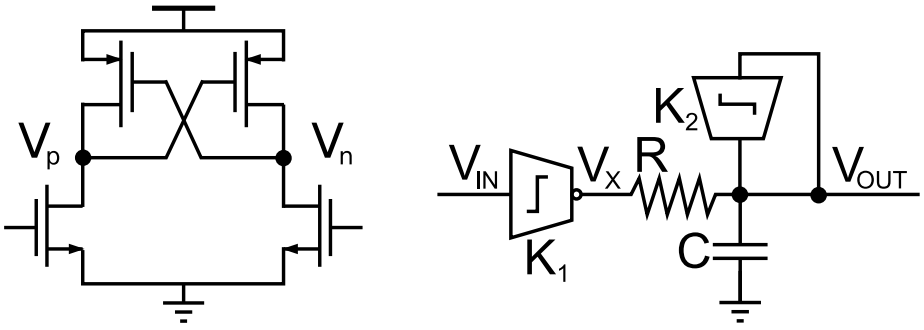
2.3 Ring oscillators under injection locking

Electronics oscillators can be divided in two main types: harmonic oscillators and relaxation oscillators. A Harmonic oscillator is made by a feedback loop where the forward path is represented by a resonant element (e.g. a LC filter), and the feedback path is an amplifier. When the power supply of the amplifier is first switched on, the amplifier's output consists only of noise. The noise travels around the loop, being filtered and re-amplified until it increasingly resembles the desired signal. The frequency of oscillation is set by the resonant frequency of the filter. At the contrary a relaxation oscillator continuously dissipates its internal energy. Each time the system reaches some threshold sufficiently close to its equilibrium, a mechanism disturbs it with additional energy. The oscillator's behavior is characterized by long periods of dissipation followed by short impulses. The period of the oscillations is set by the time it takes for the system to relax from each disturbed state to the threshold that triggers the next disturbance.

While LC oscillators are harmonics, ring oscillators belong to the relaxation family. Under this a point of view it looks more reasonable to study the behavior of an injection locked ring oscillator in the time domain, rather than in the frequency domain (as we did for the LC oscillator). In the following we present a pseudo-differential inverter made ring oscillator. First we derive an expression for the locking range of the oscillator, then we exploit the use of direct injection locking to realize a frequency divider.

2.3.1 Ring oscillator behavioral model

Fig. 2.9(a) shows the circuit implementation of a single delay cell of the ring oscillator, while the corresponding behavioral model we developed is depicted in Fig. 2.9(b). The cell is a differential CMOS inverter made of a nMOS pair loaded by two pMOS transistors in positive feedback. When the differential input commutates, one branch acts as a ratioed logic until the pMOS cross-coupled pair turns on and the gate latches to the final configuration. The equivalent model mimics the behavior of the delay cell as follows. The nMOS differential pair, described by the non-linear element K_1, is assumed to hard-switch as the input signal $V_{\mathrm{IN}}(t)$ crosses a threshold, set to zero for convenience. Next, the particular output node of the differential cell which was previously at the high logic level is pulled down. This is described by an RC network driven by $V_X = \pm V_O$. Finally, when the output signal $V_{\mathrm{OUT}}(t)$ crosses the zero-threshold, the non-linear element K_2 that represents the pMOS pair kicks in, instantaneously saturating the output voltage to



(a) (b)

Figure 2.9 (a) Circuit implementation of the delay cell. (b) Behavioral model of the delay cell.

its final value $(\pm V_O)$[4]. The propagation time t_p of the delay cell is thus set by the time $V_{\rm OUT}(t)$ takes to reach the zero level from an initial value of $\pm V_O$:

$$t_p = \ln(2)RC. \tag{2.70}$$

The transient behavior of the equivalent model is exemplified in Fig. 2.10 for a low-to-high transition of the input. When the input signal crosses the zero, K_1 responds switching V_X to $-V_O$ and the capacitance C is discharged. Consequently, $V_{\rm OUT}(t)$ evolves in an exponential fashion until it reaches the threshold voltage of K_2, i.e. the zero level. At this point, K_2 instantaneously pulls the output voltage to the final value $-V_O$. Note that in practice the switching of the pMOS pair will take a finite amount of time. However, this does not limit the proposed behavioral model, as the rise/fall time of K_2 can be easily taken into account by adjusting the RC time constant in (2.70) such that the overall propagation time t_p fits the circuit-level simulation or the measurement.

Let us now consider a ring oscillator made of a chain of N delay cells. The number of inverting stages can be even or odd, provided that there is cross-connection in the feedback path in the first case. In both cases, the period T_0 of oscillation is determined by the propagation time of a signal transition through the complete chain, that is the free running frequency of the ring oscillator is expressed by

$$f_0 = \frac{1}{T_0} = \frac{1}{2Nt_p} = \frac{1}{2N\ln(2)RC} \tag{2.71}$$

Notice that for this formulation of f_0 to be valid, the role of K_2 in the behavioral model (i.e. the role of the pMOS positive feedback) is crucial. Without K_2 (i.e. without the

[4] K_2 is modeled as an impulsive current source triggered at the zero-threshold crossings, that is $K_2(t) = \sum_k (-1)^k C V_O \delta(t - t_p - kT_0/2)$.

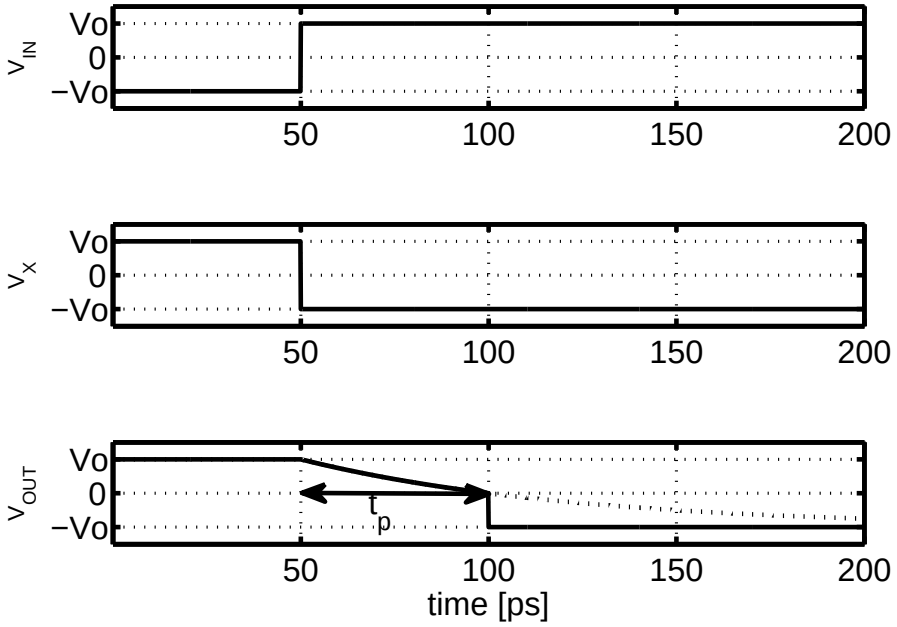


Figure 2.10 Switching of the delay cell: voltages in the behavioral model.

pMOS positive feedback), there would be an additional constraint setting the amplitude of oscillation. As described in [23], where they consider ring oscillators made by unit cells without the positive feedback load, the output voltage must show symmetric peaks with respect to the switching threshold of K_1. For a ring oscillator with two stages, as the one used in this work, the non-linear analysis in [23] predicts an amplitude equal to zero, from which stems the motivation for the presented model, where the amplitude is set by K_2 to V_O.

To fix the idea let consider the behavioral simulations reported in Fig. 2.11. They compare the voltage at the output of an unit cell of a two stages oscillator, in the case we include or not K_2 in the model. The propagation time t_p does not changes between the two cases since it only depends on the RC network, that is the same in both the simulations. Nevertheless, when K_2 is included in the model at the instant t_p the output voltage is forced to its final value, while when K_2 is not included, the output voltage keep evolving exponentially for half a period of oscillation: $T_0/2 = Nt_p$. If, as in this example, the number of stages of the ring is too small, the voltage does not reach the final value within half a period of oscillation and the amplitude of oscillation decreases, period after period, to zero.

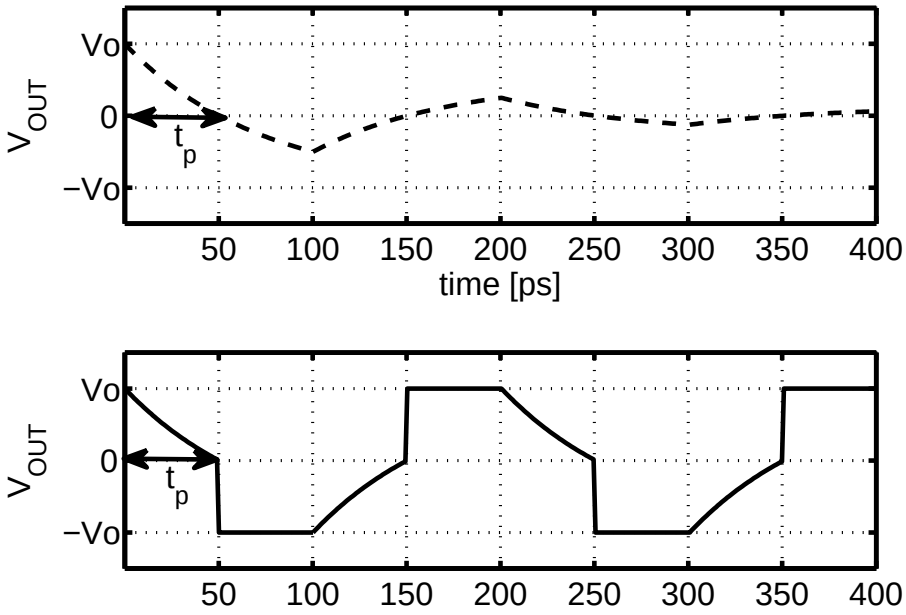


Figure 2.11 Effect of K_2: behavioral model simulations of a two stages ring oscillator in the case we include (solid line) or do not include (dashed line) K_2.

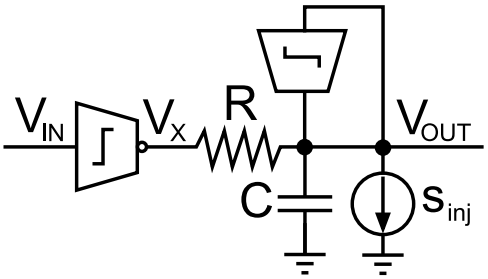


Figure 2.12 Behavioral model of the delay cell under injection-locking.

2.3.2 Locking range derivation

The behavioral model is instrumental to investigate the operation of the ring oscillator under injection locking. The injected signal is included in the behavioral model through the current source

$$s_{\text{inj}}(t) = I_{\text{inj}} \cos(\omega_{\text{inj}} t + \varphi), \tag{2.72}$$

as shown in Fig. 2.12. Moreover the model is derived assuming a multi-phase multi input injection scheme [24, 25]. This means that the phase of the injected signal changes among the different cells composing the ring, in order to guarantee that the relative phase difference between the injected signal $s_{\text{inj}}(t)$ and the output signal $V_{\text{OUT}}(t)$ is the same for all the cells. Under this assumption we can reduce the analysis of the ring to the analysis of the voltage and the current forms of a single cell, being all the others a time shifted version of the selected one.

The effect of the synchronization signal on every delay cell of the ring oscillator is to change the cell propagation time such that the period of oscillation of the ring matches the period of $s_{\text{inj}}(t)$. As a consequence, the propagation time t'_p under injection locking becomes:

$$t'_p = \frac{1}{2N f_{\text{inj}}} = \frac{\pi}{N\omega_{\text{inj}}} \tag{2.73}$$

Without loss of generality, we suppose that a low-to-high transition of the input signal occurs at the time $t = 0$. $V_{\text{OUT}}(t)$ read as:

$$V_{\text{OUT}}(t) = V_O - 2V_O(1 - e^{-\frac{t}{RC}}) - s_{\text{inj}}(t)\frac{R}{1 + j\omega_{\text{inj}}RC} \tag{2.74}$$

Moreover, by the definition of propagation time, we can write:

$$\begin{gathered} V_{\text{OUT}}(t'_p) = 0 \\ V_O - 2V_O(1 - e^{-\frac{t'_p}{RC}}) - \frac{I_{\text{inj}}R}{\sqrt{1 + (\omega_{\text{inj}}RC)^2}} \cos(\omega_{\text{inj}} t'_p + \varphi - \alpha) = 0 \end{gathered} \tag{2.75}$$

where $\alpha = \arctan(\omega_{\text{inj}} RC)$.

Making use of (2.71) and solving (2.75) for φ we obtain:

$$\varphi = \alpha - \frac{\pi}{N} + \arccos\left[\left(2e^{-\frac{\ln 2}{\xi}} - 1\right)\frac{1}{\varepsilon}\sqrt{1+\xi^2\left(\frac{\pi}{N\ln 2}\right)^2}\right] \tag{2.76}$$

where

$$\xi = \frac{\omega_{\text{inj}}}{\omega_0} \tag{2.77}$$

$$\varepsilon = \frac{I_{\text{inj}} R}{V_O} \tag{2.78}$$

The argument of the arccosine function must be limited between -1 and 1, this requirement yielding the locking range in the form of the following implicit formulation:

$$\left|2^{\frac{\xi-1}{\xi}} - 1\right| \sqrt{1+\xi^2\left(\frac{\pi}{N\ln 2}\right)^2} \leq \varepsilon. \tag{2.79}$$

For $\varepsilon = 0$, i.e. for $I_{\text{inj}} = 0$, (2.79) holds true only for $\xi = 1$, that is the ring oscillates at its free running frequency. Increasing ε, i.e. increasing the amplitude of the injection signal I_{inj}, the range of values of ξ satisfying (2.79), that is the locking range, increases as well. Solving (2.79) numerically, one can plot the locking range extrema ξ_L and ξ_H as a function of ε for several values of N, as shown in Fig. 2.13. The increase of the locking range with the number of stages observed in Fig. 2.13 is due to the multi-phase multi input injection scheme we assumed, that implies an increase of the overall strength of the injection signal as N increases. Notice that increasing too much the number of stages may be unpractical due to the requirement of a multi-phase signal.

Fig 2.14 shows the behavioral model of a minimum two stages ring we made and simulated in spectre. The time constant RC has been chosen so that the free running oscillation frequency is 5 GHz, while the injection signals have been phase shifted by $-\pi/2$ to ensure a multi-phase multi input injection scheme. Fig 2.15 compares the voltage at the output V_{OUT1} of the first cell between the free-running case and injection locked case. Two different injection locking conditions have been reported. In the first the frequency of the injection signal is smaller than the free-running frequency ($\varepsilon = 0.3$, $\xi = 0.8$), while in the second it is greater($\varepsilon = 0.3$, $\xi = 1.2$). As we expected, the presence of the injection signal modifies the charge and discharge of the RC network so the the resulting propagation time satisfy (2.73). Table 2.1 compares the normalized locking range, defined as $\xi_L - \xi_H$, predicted by (2.79) with the simulated one showing a good agreement between the two cases as a confirmation of the developed theory.

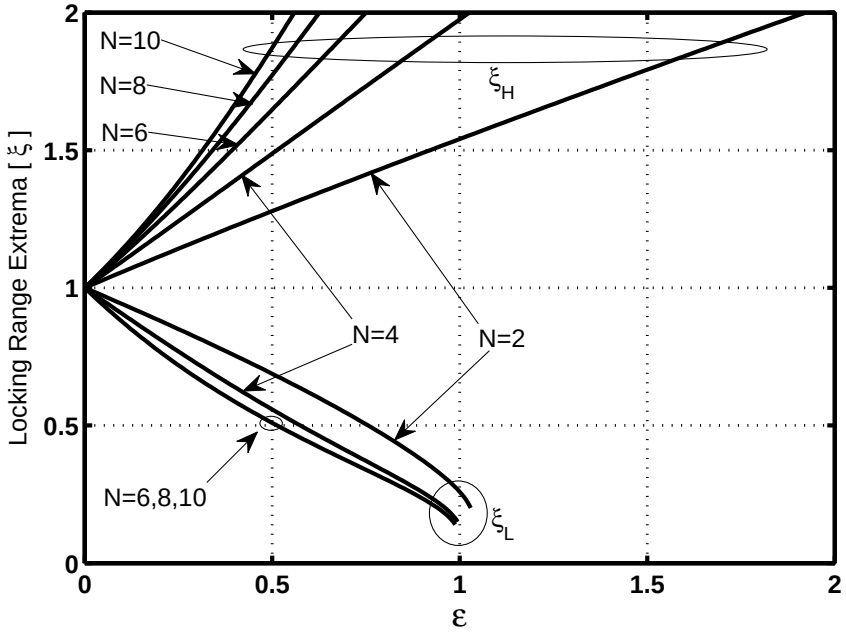


Figure 2.13 Normalized locking range extrema ξ_L and ξ_H of the N-stage ring oscillator.

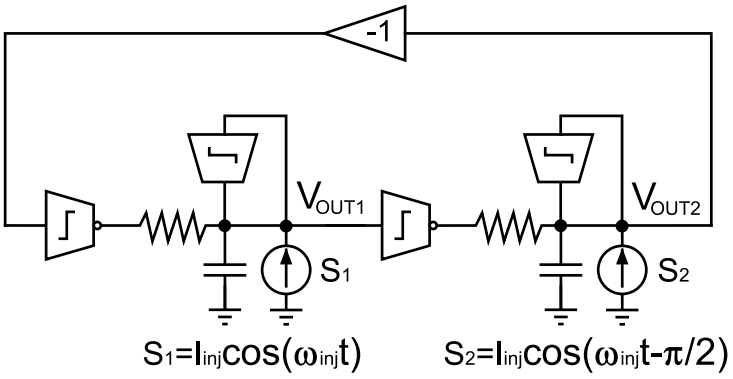


Figure 2.14 Behavioral model of the delay cell under injection-locking.

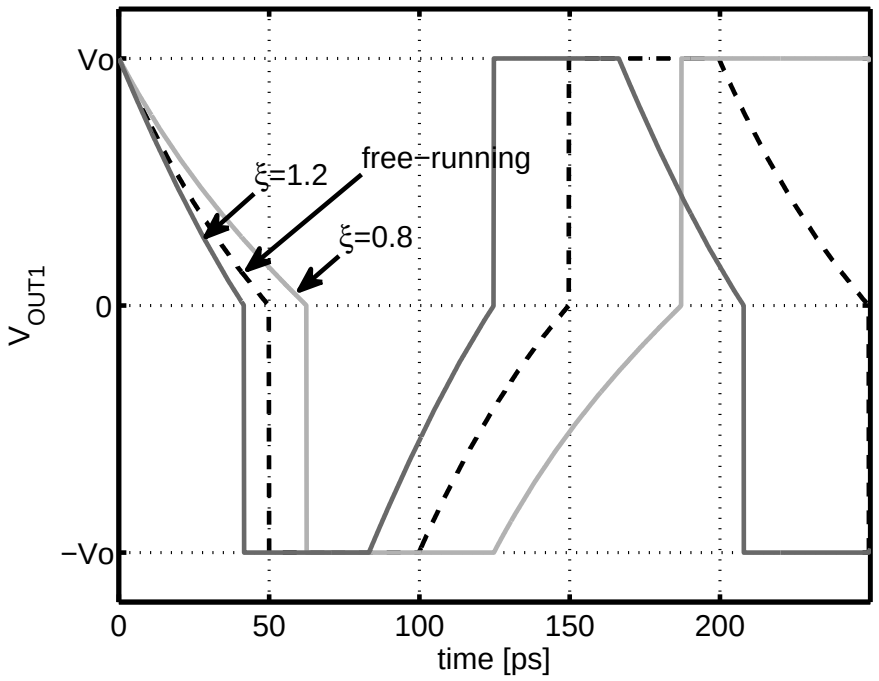


Figure 2.15 Transient simulation of the behavioral model of the ring under tree different conditions: free running (dashed line), injection locked by a signal whose frequency is greater than the free running one (dark line), and injection locked by a signal whose frequency is smaller than the free running one (light line).

ε	$\xi_L - \xi_H$	
	predicted by 2.79	simulated
0.1	0.1165	0.1284
0.2	0.2335	0.2574
0.5	0.5910	0.6470
0.8	0.9737	1.0527
0.8	1.1152	1.1994
1.0	1.2817	1.3686

Table 2.1 Comparison between the normalized locking range $\xi_L - \xi_H$ predicted by 2.79 and simulated with the behavior model of figure 2.14.

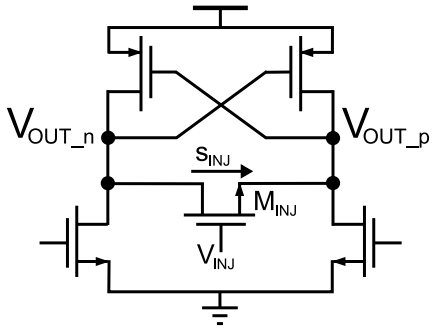


Figure 2.16 Schematic of the delay cell with direct injection device.

2.3.3 Direct injection locking as frequency divider

So far we derived the expression for the locking range of the ring assuming that a current s_{inj} was provided at the output of each unit cell of the ring. In the following we explain how to actually provide such a current and we demonstrate how this mechanism implicitly realizes a frequency divider.

Consider the schematic drawn in Fig. 2.16 where the circuit implementation of the delay cell is completed with the nMOS injection transistor M_{inj}. The divider operation is based on the super-harmonic injection locking phenomenon, which, to take place, requires some mixing to occur in the circuit [20–22, 26]. The injection signal must mix to the harmonics of the ring oscillator output waveform such that a tone is generated at a frequency close to the ring oscillator free running frequency. As will be clear from the following text, the transistors M_{inj} act as current commutating mixers, generating the required synchronization tone. Then, the way this tone will injection locked the oscillator, has been deeply investigate in Sec. 2.3.2 and expressed by (2.79).

In order to analyse the operation of the circuit under injection-locking, we write the voltages in the circuit as:

$$V_{\text{p}}(t) = V_Q + \frac{V_{\text{out}}(t)}{2} \tag{2.80}$$

$$V_{\text{n}}(t) = V_Q - \frac{V_{\text{out}}(t)}{2} \tag{2.81}$$

$$V_g(t) = V_{\text{CM}} + V_{\text{inj}}(t) = V_{\text{CM}} + V_{\text{inj}}\cos(\omega_h t + \varphi) \tag{2.82}$$

where $\omega_h = k \cdot \omega_{\text{inj}} \approx k \cdot \omega_0$. As a consequence of the ac large-signal differential output voltage, the source and drain terminals of M_{inj} swap every semiperiod, and the drain-source voltage is written as

$$V_{\text{ds}}(t) = |V_{\text{out}}(t)|, \tag{2.83}$$

while the gate-source voltage reads as

$$V_{\mathrm{gs}}(t) = V_{\mathrm{CM}} - V_Q + V_{\mathrm{inj}} \cos(\omega_h t + \varphi) + \left| \frac{V_{\mathrm{out}}(t)}{2} \right|. \tag{2.84}$$

The transistor M_{inj} is on when $V_{\mathrm{gs}}(t) - V_{t,n} > 0$:

$$V_B + V_{\mathrm{inj}} \cos(\omega_h t + \varphi) > - \left| \frac{V_{\mathrm{out}}(t)}{2} \right| \tag{2.85}$$

where $V_B = V_{\mathrm{CM}} - V_Q - V_{t,n}$ and $V_{t,n}$ is the nMOS threshold voltage. Furthermore, it is in triode region when the condition $V_{\mathrm{gs}}(t) - V_{t,n} > V_{\mathrm{ds}}(t)$:

$$V_B + V_{\mathrm{inj}} \cos(\omega_h t + \varphi) > \left| \frac{V_{\mathrm{out}}(t)}{2} \right| \tag{2.86}$$

is also satisfied. For convenience we define $D_{\mathrm{ON}}(t)$ and $D_T(t)$, which are equal to 1 when M_{inj} is on, or in the triode region, respectively, and equal to 0 elsewhere. Clearly, the condition when M_{inj} is in saturation is given by $D_S(t) = D_{\mathrm{ON}}(t) - D_T(t)$. As a consequence, we write the injection signal as

$$s_{\mathrm{inj}}(t) = \left[I_{ds,T}(t) \cdot D_T(t) + I_{ds,S}(t) \cdot D_S(t) \right] \mathrm{sign}\left[V_{\mathrm{out}}(t) \right] \tag{2.87}$$

where $I_{ds,T}(t)$ and $I_{ds,S}(t)$ are the expressions of the drain-source current of of M_{inj} in triode and saturation region, respectively. The multiplication by $\mathrm{sign}\left[V_{\mathrm{out}}(t)\right]$ takes into account the fact that the source and drain terminals of M_{inj} swap every semiperiod. Employing the long channel model for the MOS transistor, we define:

$$\begin{aligned} I_{d,T}(t) &= I_{ds,T}(t) \cdot \mathrm{sign}\left[V_{\mathrm{out}}(t)\right] \\ &= \beta \left[\left(V_B + V_{\mathrm{inj}}(t) + \frac{|V_{\mathrm{out}}(t)|}{2} \right) |V_{\mathrm{out}}(t)| - \frac{V_{\mathrm{out}}(t)^2}{2} \right] \cdot \mathrm{sign}\left[V_{\mathrm{out}}(t)\right] \\ &= \beta V_{\mathrm{inj}}(t) V_{\mathrm{out}}(t) + \frac{\beta}{2} V_B V_{\mathrm{out}}(t) \end{aligned} \tag{2.88}$$

and

$$\begin{aligned} I_{d,S}(t) &= I_{ds,S}(t) \cdot \mathrm{sign}\left[V_{\mathrm{out}}(t) V\right] \\ &= \frac{\beta}{2} \left(V_B + V_{\mathrm{inj}}(t) + \frac{|V_{\mathrm{out}}(t)|}{2} \right)^2 \cdot \mathrm{sign}\left[V_{\mathrm{out}}(t)\right] \\ &= \frac{\beta}{2} V_{\mathrm{inj}}(t) V_{\mathrm{out}}(t) + \beta V_B V_{\mathrm{inj}}(t) \cdot \mathrm{sign}[V_{\mathrm{out}}(t)] \\ &\quad + \frac{\beta}{2} V_B V_{\mathrm{out}}(t) \\ &\quad + \frac{\beta}{2} \left[V_B^2 + V_{\mathrm{inj}}^2(t) + \frac{V_{\mathrm{out}}^2(t)}{4} \right] \cdot \mathrm{sign}[V_{\mathrm{out}}(t)] \end{aligned} \tag{2.89}$$

where we make use of the identity: $|V_{\text{out}}| = V_{\text{out}} \cdot \text{sign}\,[V_{\text{out}}(t)]$. Approximating $V_{\text{out}}(t)$ as a square wave with amplitude V_O, $D_{\text{ON}}(t)$ and $D_T(t)$ are rectangular waves with duration $d_{\text{ON}} \cdot T_h$, and $d_T \cdot T_h$, respectively, and period $T_h = 2\pi/\omega_h$, whose Fourier series are:

$$\begin{aligned} D_{\text{ON}}(t) &= \sum_{k=-\infty}^{+\infty} d_{\text{ON}}\,\text{sinc}(k d_{\text{ON}})\, e^{jk(\omega_h t+\varphi)} \\ &= \sum_{k=-\infty}^{+\infty} \mathcal{D}_{\text{ON},k}\, e^{jk(\omega_h t+\varphi)} \end{aligned} \tag{2.90}$$

where

$$d_{\text{ON}} = \frac{1}{\pi}\arccos\left(-\frac{V_O}{2V_{\text{inj}}} - \frac{V_B}{V_{\text{inj}}}\right) \tag{2.91}$$

and

$$\begin{aligned} D_{\text{T}}(t) &= \sum_{k=-\infty}^{+\infty} d_{\text{T}}\,\text{sinc}(k d_{\text{T}})\, e^{jk(\omega_h t+\varphi)} \\ &= \sum_{k=-\infty}^{+\infty} \mathcal{D}_{\text{T},k}\, e^{jk(\omega_h t+\varphi)} \end{aligned} \tag{2.92}$$

where

$$d_T = \frac{1}{\pi}\arccos\left(\frac{V_O}{2V_{\text{inj}}} - \frac{V_B}{V_{\text{inj}}}\right) \tag{2.93}$$

Consequently, $D_S(t) = \sum_k \mathcal{D}_{S,k} e^{jk\omega_h t}$, with $\mathcal{D}_{S,k} = \mathcal{D}_{\text{ON},k} - \mathcal{D}_{T,k}$. The injection signal can then be writen as:

$$s_{\text{inj}}(t) = I_{d,T}(t) \cdot D_T(t) + I_{d,S}(t) \cdot D_S(t) \tag{2.94}$$

From (2.94), (2.88) and (2.89), it is clear that there are two different mechanisms enabling the mixing between $V_{\text{inj}}(t)$ and $V_{\text{out}}(t)$, then generating harmonics at frequencies $\omega_h \pm \omega_0$. One is the *direct* multiplication of the two signals. The other is an *indirect* mixing effect, due to the multiplication of $I_{d,T}(t)$ and $I_{d,S}(t)$ by $D_T(t)$ and $D_S(t)$, respectively. The synchronization signal can be written as:

$$s_{\text{inj}}(t) = I_{\text{inj}}\cos(\omega_{\text{inj}} t + \varphi) + \tilde{s}_{\text{inj}}(t) \tag{2.95}$$

where $\tilde{s}_{\text{inj}}(t)$ contains the spectral components of $s_{\text{inj}}(t)$ at frequencies other than ω_{inj}. Then the signal $I_{\text{inj}}\cos(\omega_{\text{inj}} t + \varphi)$ will lock the oscillator in the way we analysed in the Sec. 2.3.2. The exact expression for I_{inj} depends on the actual implementation, i.e. in the actual division factor. In chapters 4 and 5 we will derive the exact amplitude of I_{inj} on the case of $\omega_h = 2\omega_{\text{inj}}$ and $\omega_h = 4\omega_{\text{inj}}$ respectively.

Part II

Design

Chapter 3

UWB Fast-Hopping Frequency Generation Based on Sub-Harmonic Injection Locking

Sub-harmonic injection locking is employed to generate the fast-hopping carriers required in UWB systems for WiMedia. A very small area 90 nm CMOS prototype synthesizes the frequencies of band group #6 with a hop time shorter than 4 ns. It occupies 0.074 mm^2 and draws 30 mA from a 1.2 V supply. Phase noise at 8.71 GHz is -112 dBc at 1 MHz offset.

3.1 Introduction

One of the key challenges for high data rate WiMedia Ultra-Wideband (UWB) systems is to design an efficient local oscillator (LO) generation. On one hand it must fulfill the stringent requirements (multiple LO frequencies, spurious, settling time, in-phase/quadrature (I/Q) imbalance), and on the other hand it should yield minimized power consumption, area and complexity.

The LO generation in a UWB system shows peculiar features. The WiMedia Alliance proposed to channelize the UWB available spectrum from 3.1-GHz to 10.6-GHz into 14 sub-bands and to exploit OFDM modulation [27]. The channel center frequencies are at

$$f_c = 2904 + 528 \cdot n_b \text{ [MHz]}, \quad n_b = 1, \ldots, 14, \tag{3.1}$$

that is at odd harmonics of 264-MHz. The sub-bands are allocated in 6 groups, as sketched in Fig. 3.1. Within each group fast frequency hopping is employed to allow for

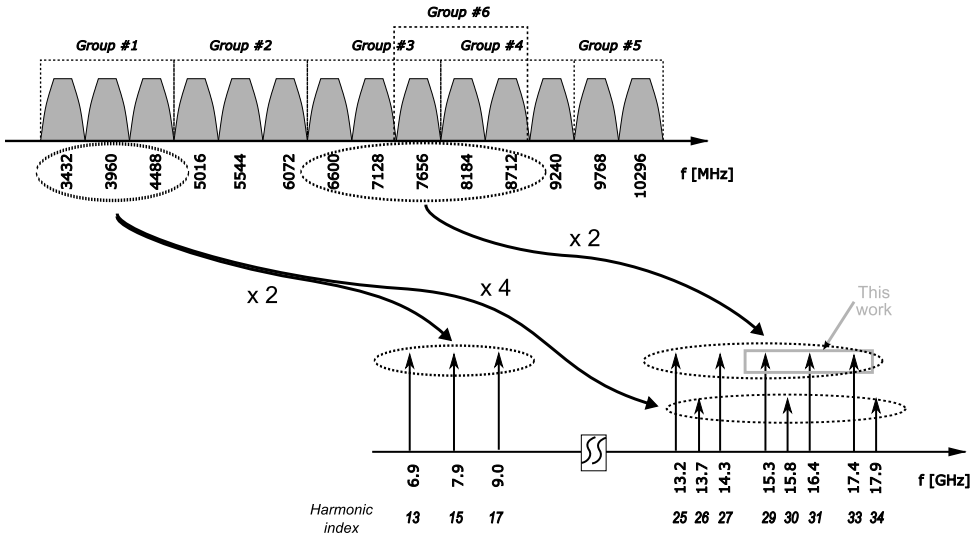


Figure 3.1 Frequency plan of the proposed system.

time-frequency coding. The generation of the carriers entails several issues. A wide span of frequencies is to be synthesized while ensuring a fast hopping capability. Transmitter (TX) EVM specifications call for a moderate (-106-dBc/Hz at 1-MHz offset) phase noise performance, while the transmit PSD mask requires the spur level to be less than -20-dBc in adjacent sub-bands [27].

Various different UWB LO concepts have already been proposed [28–31], but none of them seems to give a clear advantage over the other. The required ability of hopping from one LO frequency to the other within 9-ns [27] prevents the use of a conventional approach based on a single wideband PLL. Single-sideband (SSB) mixers can be used to offset a fixed frequency to simultaneously generate the required carriers which are dynamically selected by a multiplexer [29, 30]. This approach, however, in CMOS requires a huge power consumption to achieve low spurious. Another possibility is to use an array of PLLs [28, 31], leading to a large area. In this work we propose a completely different approach using sub-harmonic injection locking. Measurement results in 90-nm CMOS clearly show the required performance, while having lowest area and power.

3.2 Sub-harmonic injection locking concept and design constraints

The block diagram is depicted in Fig. 3.2. An *LC* oscillator, operated at twice the desired

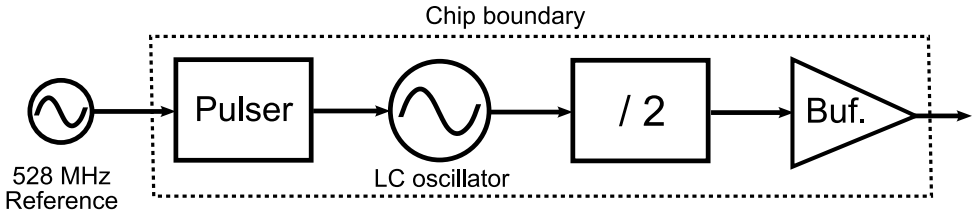


Figure 3.2 Block diagram of the proposed system.

frequency to avoid TX frequency pulling, is injection locked to the k-th harmonic of a 528-MHz reference. This basically allows to generate all 14 LO frequencies required by WiMedia. The oscillator is followed by a divide-by-2 circuit to generate the desired frequency as well as quadrature phases. The locking range is narrower than the reference frequency to guarantee a unique locking condition. Changing the natural frequency of the LC tank, the oscillator locks to another harmonic, corresponding to a different UWB channel frequency. For example, the harmonics corresponding to the UWB channels for band groups #1, #3, and #6 are shown in Fig. 3.1. One can also lock the oscillator at 4 times the frequencies of band group #1. As a consequence, only one oscillator with 30% tuning range can cover all band groups.

3.2.1 Lockign range constraints

As we introduced in Sec. 2.1 sub harmonic injection locking is a particular form of injection locking where the synchronization signal is at a frequency ω_i much smaller than oscillator natural frequency ω_0. Then, to ensure the lock condition to occurs, the synchronization signal must be processed by a non liner block that enriches its harmonic content to the point that one of the generating harmonic falls within the locking range, that is a small frequency interval around ω_0. Contrary to the normal solutions, where the harmonic that locks the oscillator is in the order of some units, in our case we want to lock up to the 33^{rd} harmonic of the synchronization signal, with some obvious complications, first of all the fact that non linearity must generate harmonics up to the 33^{rd}. This can be solved choosing a pulser as non linearity, because it generates infinite harmonics with equal amplitude at the multiple of the synchronization signal frequency. Of course an ideal pulser is impossible to realize and the best we can do is to generate a square wave-form with a duty cycle the smaller the possible. The fact we want to lock up to such a higher harmonic also introduces another problem. In normal solution the frequency distance between two consecutive harmonics of the synchronization signal is big enough to avoid

the risk that two or more harmonics lie inside the locking range. In our case, however, the frequency distance between two consecutive harmonics of the synchronization signal result in a small percentage of the oscillation frequency and the condition that only just a harmonic lies inside the locking range must be verified. The study of an LC oscillator under injection locking has already been faced in Sec. 2.2.1 and the unilateral locking range ω_L has been proved to be:

$$\omega_L = \frac{\omega_0}{2Q}\frac{A_i}{I_1}\frac{1}{\sqrt{1-\left(\frac{A_i}{I_1}\right)^2}}. \tag{3.2}$$

where A_i is now the amplitude of the $k-th$ harmonic of the synchronization signal at the frequency $\omega_{\text{inj}} = k\omega_i$, that actually locks the oscillator, and I_1 is the first harmonic of the current generated by the active element of the VCO. The condition that just a harmonic lies inside the locking range is verified when $2\omega_L$ is smaller than the reference frequency. In the design prospective (3.2) shows that the locking range is smaller than the bandwidth of the LC resonator by a factor that depends on the relative strength of the injected signal. As a consequence, for a given tank one can ensure correct and robust operation by controlling the strength of the injected signal. Changing the tank natural frequency, e.g. by acting on the resonator capacitance, one can bring it closer to another reference's harmonic. Then, the oscillator will lock to it. Selecting the reference frequency to be equal to the UWB channel spacing allows us to synthesize all the required UWB carriers. Capacitance variation can be accomplished by using varactors or capacitor banks. In the former case, an analog control is required. In the latter, a narrow locking range results in a requirement for high frequency/capacitance resolution, which seems anyway a simpler issue to deal with compared to a continuous control. In summary, the call for reliable operation of the sub-harmonic injection locked oscillator translates into the request of a capacitor bank controlled by a digital word with lots of bits.

3.2.2 Spurious tones

In typical application the harmonic of the synchronization signal that do not lock the oscillator lie far from ω_0 so that we can assume that they are removed by the filter. This is not true in our case and the analysis of the system in presence of a multi-tones synchronization signal must be developed. However, we can arrange this problem into the analysis of the spurs developed in Sec. 2.2.2. It is enough to interpret the tone that actually locks the oscillator as the desired one, and all the other harmonics as spurs, then the analysis does not changes. The analysis showed that there are two ways to keep the

spurious tones low: one is to implement a high selective, high-Q LC tank, the other is ti attenuate the undesired harmonics directly at the source. Since the quality factor of the tank cannot be chosen arbitrarily because it also impact other design aspects (e.g. the locking range and the power consumption) in our case we have chosen to follow the latter way, acting on the pulser to conveniently engineer the pulse waveform, as discussed in Sec. 3.3.

3.2.3 Hopping time

The time the oscillator takes to stabilize after the tank capacitance is changed is of extreme importance in UWB systems, as discussed in Sec. 3.1. There are two mechanisms that determine the transient. The first is the change of the tank natural frequency and the settling of a new oscillation mode. The second is, of course, the locking process to another reference's harmonic. The former is like the oscillator's startup. If at a given time t' we change the capacitance, oscillations will build up at the new natural frequency ω_0' having as initial condition the oscillator's state at t'. The actual transient depends on the characteristics of the non-linear feedback element. However, the system approximately settles with a characteristic time constant $\tau_0 = 2Q/\omega_0'$. The latter has been analyzed in Sec. 2.2.3, where we concluded that the locking is reached within some multiples of $\tau_L = 1/\omega_L$.

Comparing the two mechanisms we observe that the response of the oscillator to a change in the resonator natural frequency is a fast process compared to the locking transient, as the locking range is only a fraction of the tank bandwidth. This may be interpreted as the injection locking limits the ability of the system to fast frequency hop and that a wide locking range is required. Instead, it must be observed that while the change in the tank capacitance results in a considerable frequency jump $(\omega_i - \omega_0')$, the locking process only corrects for a minor frequency error $(\omega_i' - \omega_0')$, which in our case is on the order of 0.6 % of ω_0'. Thus, the locking process scarcely contributes to the overall settling time, as the dynamic frequency error is mainly set by the tank properties. This is the more true the closer the new tank center frequency ω_0' is to the new locked frequency ω_i'. The bottom line is that fast hopping is achievable in an injection locked oscillator with a moderate-Q tank and high frequency resolution.

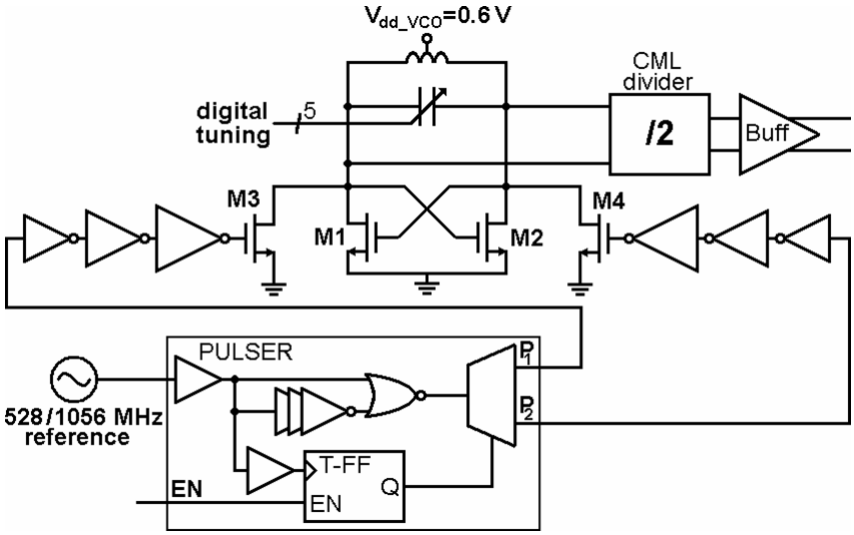


Figure 3.3 Simplified schematic of the implemented system.

3.3 Circuit design

In order to prove the concept proposed in Sec. 3.2, we focused on the generation of carriers for WiMedia band group #6. In fact, that portion of the spectrum shows the most stringent challenges, as the highest harmonic indexes among the band groups of commercial interest are involved. A simplified schematic of the implemented circuit is shown in Fig. 3.3. The sub-harmonic injection locked *LC* oscillator is followed by a conventional divide-by-2 CML divider. Output buffers are included for measurement purposes only.

The oscillator core is made of an *LC* tank and a cross-coupled nMOS differential pair. A single-turn 140-pH inductor is employed. Its center tap is connected to a dedicated 0.6 V supply to prevent any oscillator node to exceed the 1.2 V supply voltage of the employed technology.

As discussed in Sec. 3.2.3, a moderate tank quality factor associated to the capability of high frequency resolution allows for fast frequency hopping. A 5-bit binary weighted capacitor bank is used to tune the tank frequency. This makes the system a Digitally-controlled Injection Locked Oscillator (DILO). The two least significant bits are implemented by means of back-to-back connected MOS varactors, while the three most significant bits are made of switched metal-oxide-metal (MOM) finger capacitors for their higher Q. The switch arrangement turned out to be critical to achieve fast frequency hopping. A standard nMOS switch M_{sw} is sketched in Fig. 3.4(a). When the switch is opened

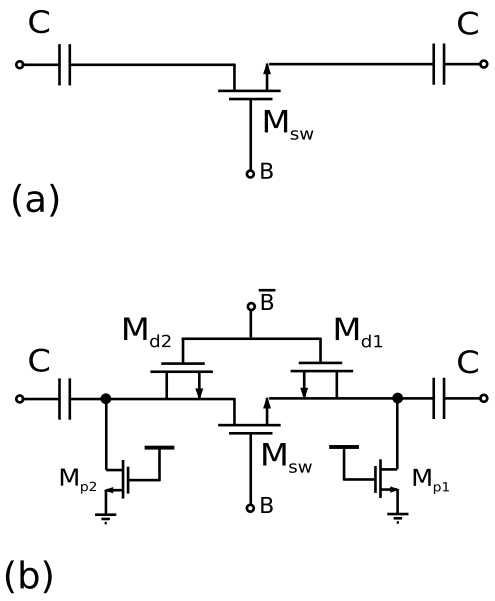


Figure 3.4 Unit element of the capacitor bank: (a) standard switch configuration; (b) improved switch configuration.

and the capacitors C disconnected from the tank, the nMOS channel charge is ejected out of the drain and source terminals. Since the latter are at high impedance the corresponding node voltages experience slow transients as they are discharged to the supplies. As a consequence, the switch parasitic drain-to-bulk and source-to-bulk capacitances slowly change as well. In turn, the residual contribution of the disconnected capacitances to the overall tank capacitance changes with time modulating the tank natural frequency and, eventually, slowing the oscillator frequency hop. To address this issue we added dummy switches M_{d1} and M_{d2} as shown in Fig. 3.4(b). They feature half the width of $M_{\rm sw}$, and they are controlled by a complementary signal compared to $M_{\rm sw}$. Moreover, we added minimum size transistors M_{p1} and M_{p2} that act as pull-downs. They ensure the dc level of the switch terminals be ground such that both the actual and dummy switches can be effectively turned on and off. Ac-wise M_{p1} and M_{p2} show high on-resistance and do not significantly affect the tank operation. The unit capacitance of the capacitor bank is as low as $C = 12.5$ fF. At power-up for each sub-band a control word is searched and stored such that the oscillation frequency matches the desired UWB sub-band.

Injection locking is enabled by a frequency reference driving a pulser which controls the injection devices (M_3 and M_4 in Fig. 3.3). The size of the injection devices sets the amplitude of the current pulses flowing into the tank and thus controls both the locking range and the level of the output spurious tones. We designed two versions of the

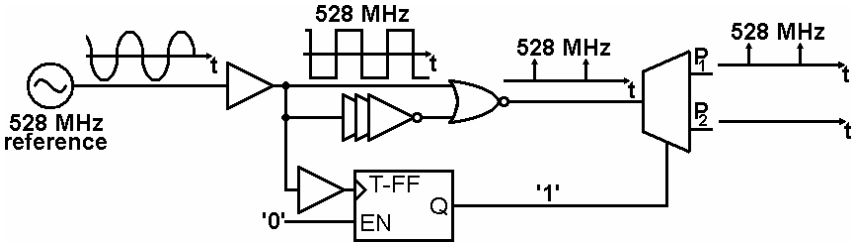


Figure 3.5 Pulser operation in "single" mode.

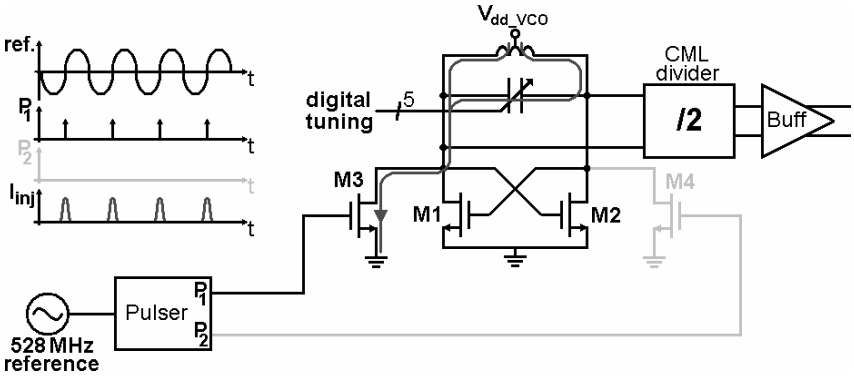


Figure 3.6 Injected current in in "single" mode.

DILO system. Wider injection devices, namely $W = 120\,\mu$m, are used in DILO-L, while $80\,\mu$m wide transistors are employed in DILO-S. The trade-off between locking range and spurious amplitude can consequently be experimentally assessed.

The pulser is made of complementary static digital gates. It forms approximately rectangular pulses with a sinc-like spectrum. The design aims at minimizing the pulse width such that all the harmonics of interest lie within the same sinc lobe, and they have approximately the same amplitude. Moreover, being within the same sinc lobe they are all in-phase, a convenient feature as shown by Fig. 2.5. As discussed in Sec. 2.2.2, appropriate shaping of the pulse waveform helps reducing the spurious tones in the oscillator output voltage. Therefore, we implemented two possible modes of operation for the pulser, which are detailed in the following.

3.3.1 "Single" mode of operation

The operation of the pulser in "single" mode is illustrated in Fig. 3.5. The pulser is driven by a 528-MHz reference and the toggle flip-flop (T-FF) is disabled. As a consequence, the pulser output P_2 is always off. Conversely, at P_1 pulses at 528-MHz rate are output, which

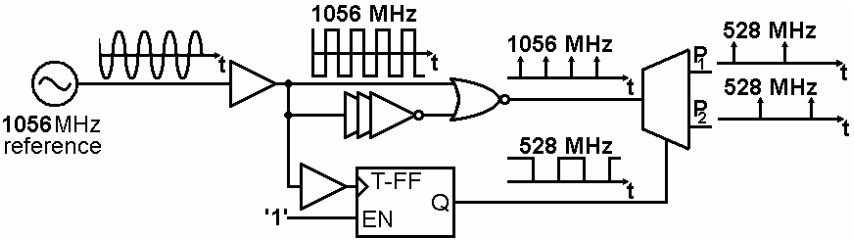


Figure 3.7 Pulser operation in "toggle" mode.

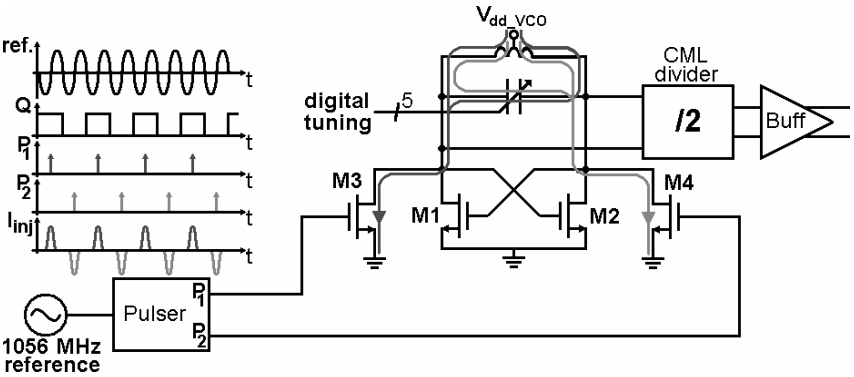


Figure 3.8 Injected current in in "toggle" mode.

activate only one device (M_3) while the transistor M_4 is never turned on. As sketched in Fig. 3.6, the injected current flows into the tank only in one direction. Thus, $i_{\text{inj}}(t)$ has both odd and even harmonics of 528-MHz.

3.3.2 "Toggle" mode of operation

In "togle" mode, pulses at 1056-MHz rate are generated, as shown in Fig. 3.7. As the T-FF is enabled, however, they are alternately fed to P_1 and P_2 such that at each output the pulse rate is only 528-MHz. The generated pulses activate M_3 and M_4 alternately, resulting in current pulses with opposite polarities. As a consequence, a 528-MHz odd-symmetry current wave with a rich harmonic content, shown in Fig. 3.8, is injected into the tank. The amplitude of each odd harmonic is effectively doubled, while even harmonics are theoretically suppressed. This results in doubled locking range. Moreover, the spurious tones in the adjacent UWB channels are canceled.

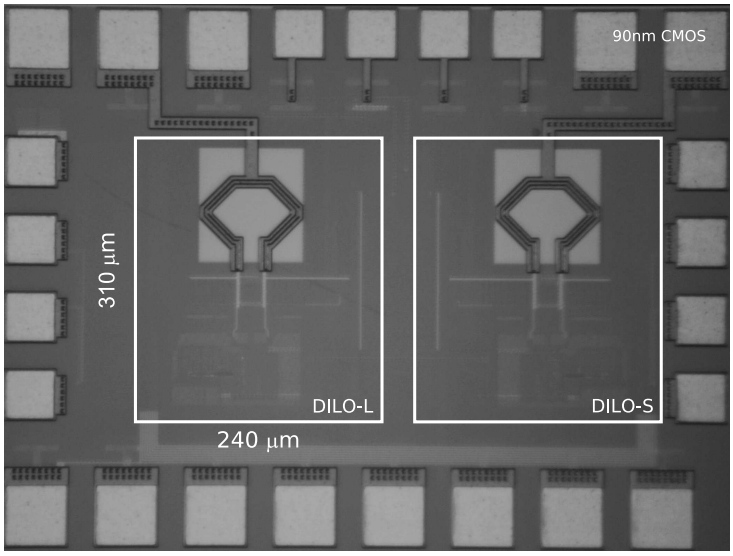


Figure 3.9 Chip micrograph.

3.4 Measurement results

Prototypes of the designed circuit are implemented in a digital 90nm CMOS technology and assembled in chip-on-board fashion for testing. A micrograph of the chip is shown in Fig. 3.9. Within the same pad ring two versions of the circuit are laid out, DILO-L and DILO-S, as previously discussed. In any case, the active area is only 0.074-mm^2.

Figure 3.10 shows the measured output spectrum of DILO-L for each frequency of band group #6, normalized to the carrier amplitude. The system is operated in "toggle" mode. The worst case spur is lower than −19 dBc, −30 dBc, and −38 dBc in sub-bands #9, #10, and #11, respectively. Notice the worst spurs are those at 528-MHz offset from the carrier, which are supposed to be canceled by the "toggle" operation. Mismatches in the buffers driving M_3 and M_4 cause their limited suppression. As a consequence, a more accurate layout is expected to improve the DILO performance, in particular at 7.66-GHz. "Toggle" operation is anyway effective. Measurements on DILO-L at 8.71-GHz in "single" mode show a 9-dB degradation of the spur level at 528MHz offset compared to "toggle" mode. Smaller injection devices result in lower amplitude of the reference's harmonics and thus lower spurs. Measurements on DILO-S at 8.71-GHz show −38 dBc and −48 dBc spurs at 528-MHz offset in "single" and "togle" mode, respectively. This however comes at the price of a reduction of the locking range from about 100-MHz in DILO-L to about 30-MHz in DILO-S.

Phase noise measurements carried out at 8.71-GHz show the typical behavior of in-

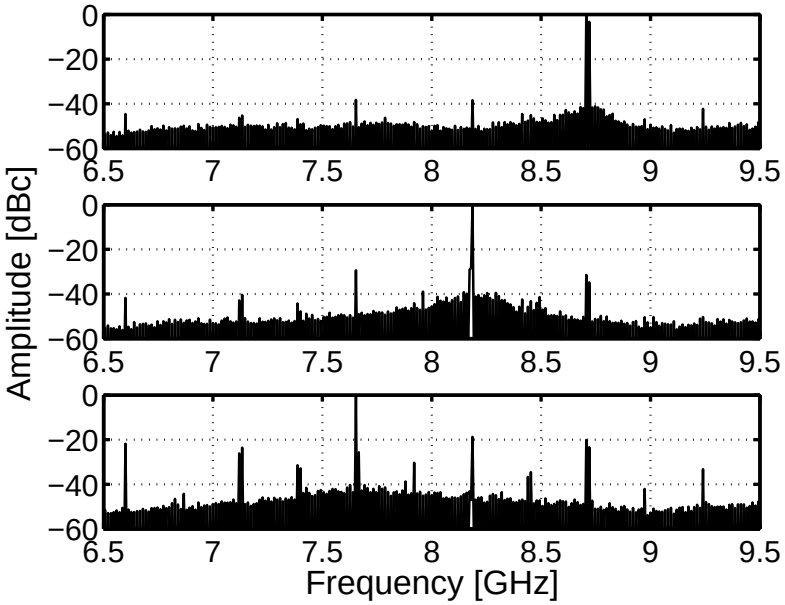


Figure 3.10 Measured spectrum of DILO-L for all frequency of band group #6.

jection locked systems. For offset frequencies in the locking range, the phase noise of the locked oscillator, shown in Fig. 3.11, tracks the reference's one scaled by a factor equal to the square of the frequency ratio, in this case 24-dB. In free running, the phase noise is -94 dBc/Hz at 1-MHz offset, while under injection locking it improves to -112 dBc/Hz at the same offset.

In Fig. 3.12, the setup for the measurement of the hopping time is illustrated. A hop from 7.66 GHz to 8.71 GHz is triggered by a change in the digital control word of the capacitor bank. The DILO-L output signal is downconverted using an external mixer and a 7-GHz oscillator to 0.66-GHz and 1.71-GHz, respectively, such that it lies well into the 8-GHz oscilloscope bandwidth. The acquired time-domain waveform is shown in Fig. 3.13. Evaluating the transient by looking at the waveform envelope as usually done in the literature is a quite problematic approach. In our case, the frequency hop seems almost instantaneous in Fig. 3.13. Thus, we evaluated the spectrogram of the measured wave. The result, reported in Fig. 3.14, clearly points out that the hopping time is shorter than 4 ns. The performance of the proposed LO generation system is summarized and compared to other designs in Tab. 3.1. The power consumption (30 mA from 1.2 V supply) is dominated by the VCO/Divider combination designed to achieve an I/Q phase imbalance of 1°.

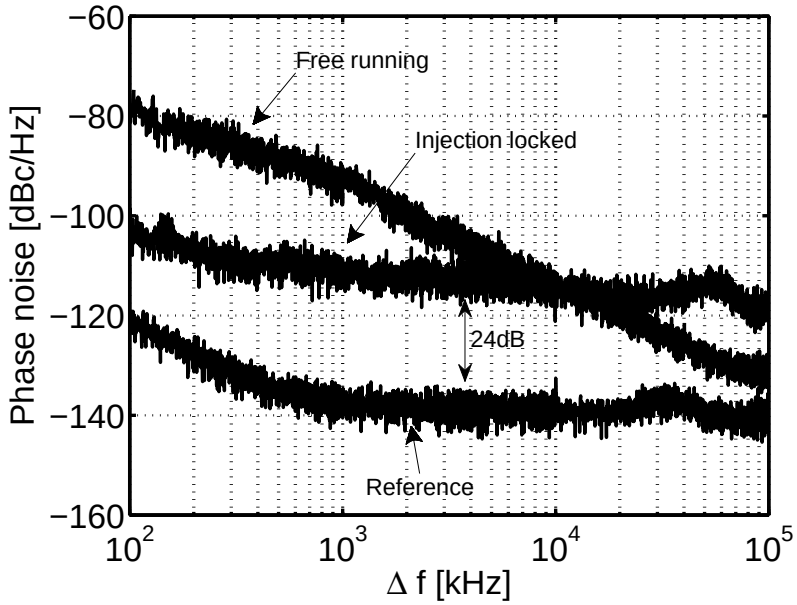


Figure 3.11 Measured phase noise of DILO-L at 8.71 GHz in free running and under locking condition. The phase noise of the 1056 MHz reference is also shown. Measurements carried out with Agilent E4448A spectrum analyzer.

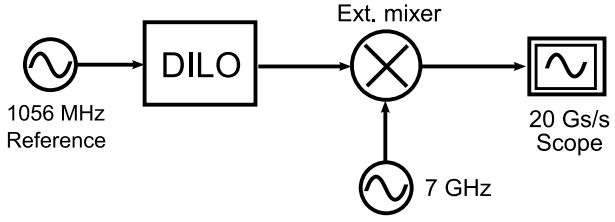


Figure 3.12 Setup for the hopping time measurement.

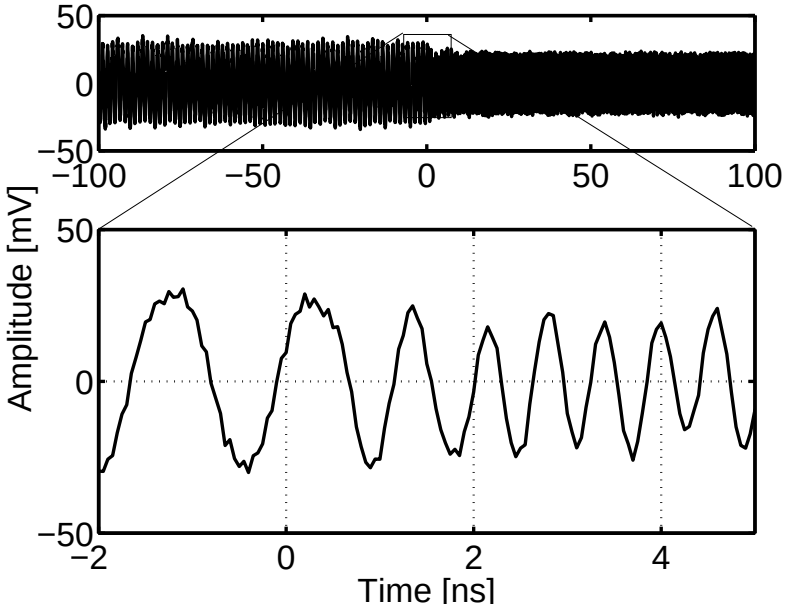


Figure 3.13 Time domain waveform of the frequency hop from 7.66 GHz to 8.71 GHz of DILO-L.

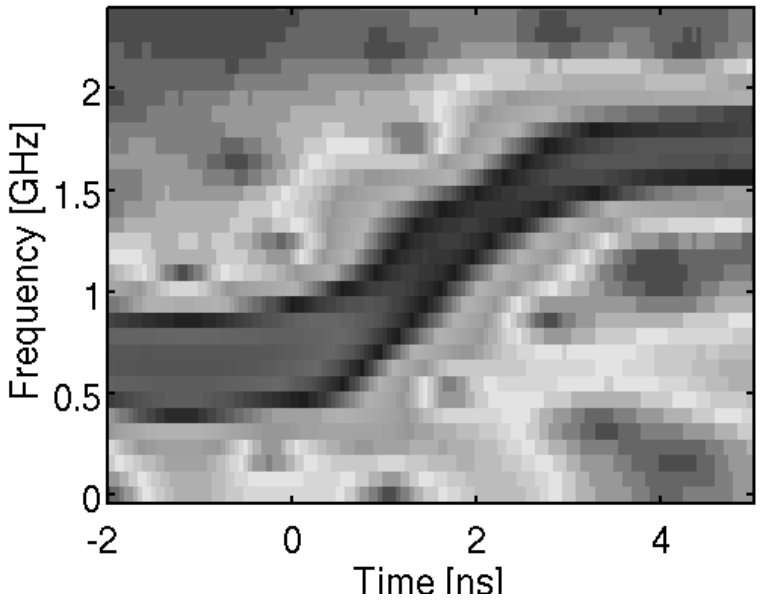


Figure 3.14 Spectrogram of the frequency hop from 7.66 GHz to 8.71 GHz of DILO-L.

	[28]	[29]	[30]	[31]	This work
Tech [μm]	0.13	0.18	0.13	0.13	0.09
Band group	#1	#1...#14	#1	#1, #3	#6
Area [mm^2]	N/A	1.52	1.2	1.9	0.074
P_{DC} [mW]	45	162	186	39	36†
Spur level [dBc]	<-27	<-35	<-18	<-28	-38...-19
$\mathcal{L}$(1MHz) [dBc/Hz]	-104	N/A	-100	-101	-112
Hop time [ns]	N/A	<3	<2	<2	<4

$^{\dagger}P_{\mathrm{DC}} = 1.2\,\mathrm{V} \cdot (17\,\mathrm{mA}\ [\mathrm{VCO}] + 12\,\mathrm{mA}\ [\mathrm{Divider}] + 1\,\mathrm{mA}\ [\mathrm{Pulser}, M_3, M_4])$

Table 3.1 Summary of measured performance and comparison to other UWB LO generation systems.

3.5 Conclusions

The use of sub-harmonic injection locking is demonstrated to be an elegant low-power low area solution to generate the fast-hopping carriers required in multi-band UWB systems. A very small area 0.074 mm^2 chip prototype in 90 nm CMOS synthesizes the frequencies of band group #6 with a hop time shorter than 4 ns. Power consumption, including IQ-generation, is 30 mA from a 1.2 V supply. Phase noise at 8.71 GHz is -112 dBc/Hz at 1 MHz offset. The obtained results point out that the proposed solution is a promising option for the implementation of WiMedia systems.

Chapter 4

An integrated divide-by-two direct injection locking frequency divider for bands S through K_u

Direct injection locking is applied to a ring oscillator topology to design a wideband divide-by-two frequency divider circuit with a locking range covering bands S through K_u, namely input frequencies from 2 to 16-GHz. Prototypes implemented in a digital 65-nm CMOS technology draw 1.6-mA from a 1.2-V supply. Since the design is inductorless, the divider area is as low as 130-μm^2. The output phase noise tracks the reference's one with the expected 6-dB difference over the entire range of operation frequencies.

4.1 Introduction

As multi-standard multi-band systems emerge in today wireless market, there is an increasing demand for broadband building blocks, capable of operating over a wide range of frequencies with low power consumption. However, the constant increase of the operation frequencies contrasts with the call for low power devices. Frequency dividers are largely employed in frequency synthesis and generation of quadrature phases. They are usually designed as clocked digital circuits, due to the robustness of this approach. However, a pure digital design suffers of the increase of power consumption with the frequency of operation. An alternative approach is injection-locked circuits [21–26, 32–37]. Harmonic or ring oscillators are synchronized by a reference signal at a frequency close to an integer multiple k of their oscillation frequency ω_0. In this way, frequency division is achieved. There are two main drawbacks in injection-locked dividers [21, 22, 26, 32, 33]: They are

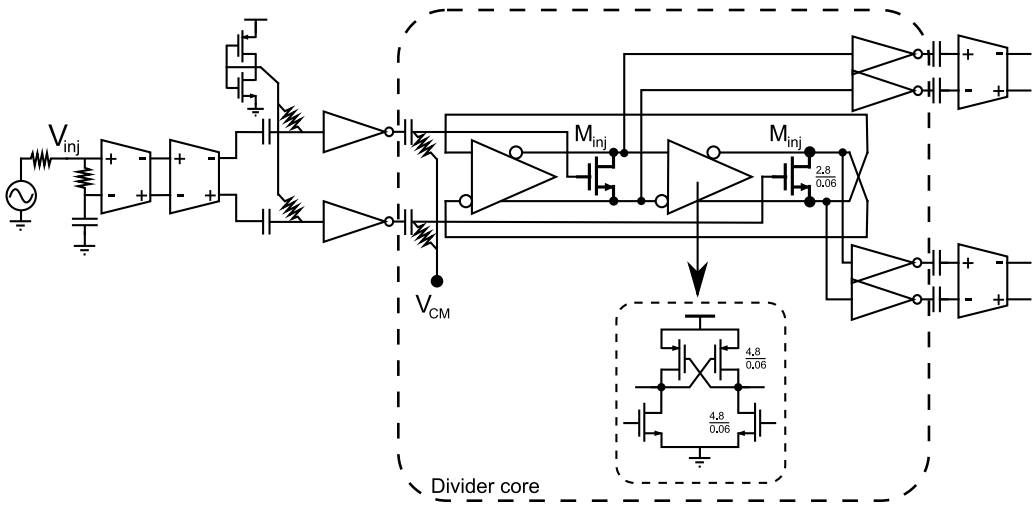


Figure 4.1 Schematic of the proposed circuit.

often made of area-hungry LC oscillators to operate at higher frequencies; The frequency to be divided should not be too different from $k \cdot \omega_0$, that is the locking range of the divider is usually quite limited.

In this work, we present a divide-by-two circuit that addresses both issues by applying direct injection locking [32] to a ring oscillator-based topology. The design is ultimately based on digital gates, hence it benefits from technology scaling, while it is lower power than purely clocked digital circuits, as the divider circuitry switches at the output frequency rate. The experimental results show a very compact circuit with a three-octave locking range and a 2-mW power consumption. The proposed circuit is not tailored for a specific application. It can be used for frequency generation in any system operating in bands S, C, X, or K_u (e.g. WLAN, Bluetooth, WiMAX, UWB, radars, etc.), as it accepts any input signal in the frequency range from 2 to 16-GHz. Moreover, due to its low power consumption, it may enable the use of higher-frequency smaller-area oscillators in cellular systems (or any other system in the low-GHz range) by operating as a prescaler.

4.2 Divider architecture and analysis

The proposed divider is depicted in Fig. 4.1, where the divider core solution is the one presented in Sec. 2.3. The number of stages N has been chosen to be equal to two in order to satisfy the multi-phase multiple input scheme, and enhance the locking range [24, 25], in presence of a differential injection signal. This fits well the case when the input signal is generated by an integrated VCO, which commonly features a differential topology.

The general expression for the injection signal has been already calculated in chapter 2 and expressed by (2.94), and (2.95). Here we derive a more detailed expression for $I_{\rm inj}$ for the particular case of a divider by two under the hypothesis that the output signal is a square wave with amplitude V_0. In this condition we make use of the identities:

$$\text{sign}\left[V_{\rm out}(t)\right] = V_{\rm out}(t)/V_0 \tag{4.1}$$

$$V_{\rm out}(t)^2 = V_0^2 \tag{4.2}$$

to rewrite (2.89) as:

$$\begin{aligned} I_{d,S}(t) = & \frac{\beta}{2}\left[1+\frac{2V_B}{V_0}\right]V_{\rm inj}(t)V_{\rm out}(t) \\ & + \frac{\beta}{2}\left[1+\frac{V_B}{V_0}\right]V_B V_{\rm out}(t) + \frac{\beta}{4}\left[\frac{V_{\rm inj}^2}{V_0}+\frac{V_0}{2}\right]V_{\rm out}(t) \\ & + \frac{\beta}{4}\frac{V_{\rm inj}^2}{V_0}\cos(2\omega_h t + 2\psi) \end{aligned} \tag{4.3}$$

Then to calculate the exact expression of $I_{\rm inj}$ we should replace (4.3) and (2.88) into (2.94), and take into account all the mixing products among $I_{d,T}(t)$ and $\mathcal{D}_{{\rm T},k}$, and $I_{d,S}(t)$ and $\mathcal{D}_{{\rm S},k}$ that generate tones at the frequency $\omega_{\rm inj} = \omega_h/2$. Neglecting for simplicity all the Fourier coefficients of $\mathcal{D}_{{\rm T},k}$, and $\mathcal{D}_{{\rm S},k}$ for $k > 1$, and taking into account only the first harmonic of Vout(t), we obtain:

$$\begin{aligned} I_{\rm inj} = & \frac{\beta}{\pi}V_{\rm inj}V_O\left(d_{\rm ON}+d_T+\frac{2V_B}{V_O}\mathcal{D}_{S,0}\right)+\frac{3\beta}{2\pi}V_{\rm inj}^2\mathcal{D}_{S,1} \\ & + \frac{\beta}{\pi}V_O^2\left(\frac{\mathcal{D}_{S,1}}{4}+\frac{V_B}{V_O}\mathcal{D}_{{\rm ON},1}+\frac{V_B^2}{V_O^2}\mathcal{D}_{S,1}\right) \end{aligned} \tag{4.4}$$

Some simplifications can be carried out analysing the results report in Fig. 4.2. They show the values assumed by $d_{\rm ON}$, d_T, and $d_S = d_{\rm ON} - d_T$, for different values of V_B/V_0 and $V_{\rm inj}/V_0$. Notice that, assuming $V_O = V_{DD}$, $V_Q = V_{DD}/2$ and $V_{t,n} = V_{DD}/4$, the maximum possible value for V_B/V_O is 0.25, if $V_{\rm CM}$ cannot exceed V_{DD}, or even lower, if the threshold voltage of the nMOS device is higher (e.g. because of the body effect, or in low-power technologies). As a consequence we can assume that $M_{\rm inj}$ is never in triode in pracice, that is:

$$\frac{V_B}{V_O} < \frac{1}{2} - \frac{V_{\rm inj}}{V_O}. \tag{4.5}$$

In this case, $d_T = 0$ and $\mathcal{D}_{S,k} = \mathcal{D}_{{\rm ON},k}$. Moreover, Fig. 4.2(a) tells us that we can also assume that injection transistor is on only part of the time, i.e. for

$$-\left(\frac{1}{2}+\frac{V_{\rm inj}}{V_O}\right) < \frac{V_B}{V_O} < -\left(\frac{1}{2}-\frac{V_{\rm inj}}{V_O}\right), \tag{4.6}$$

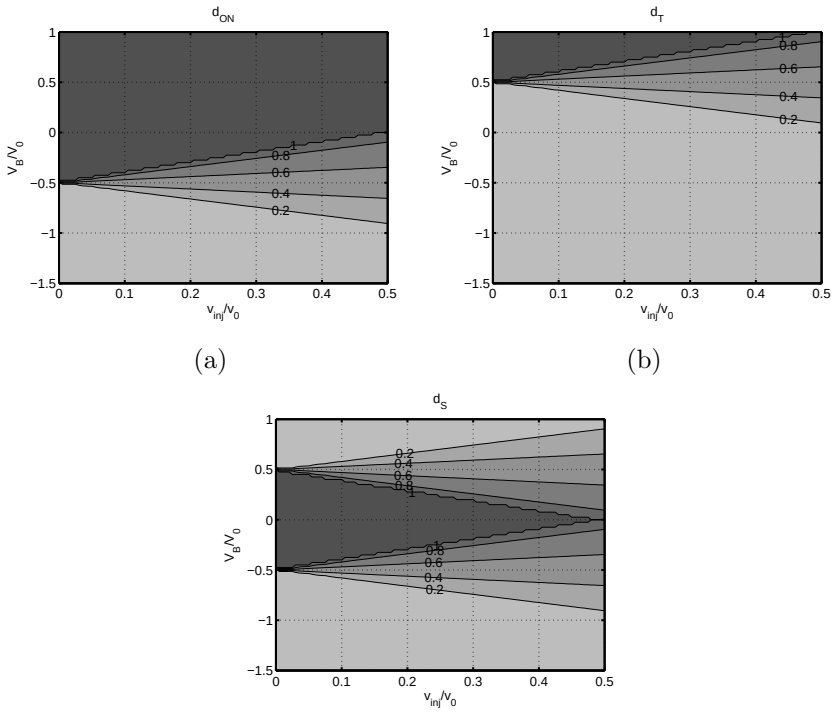


Figure 4.2 Values assumed by d_{ON}, d_T, and $d_S = d_{\mathrm{ON}} - d_T$, for different values of V_B/V_0 and V_{inj}/V_0.

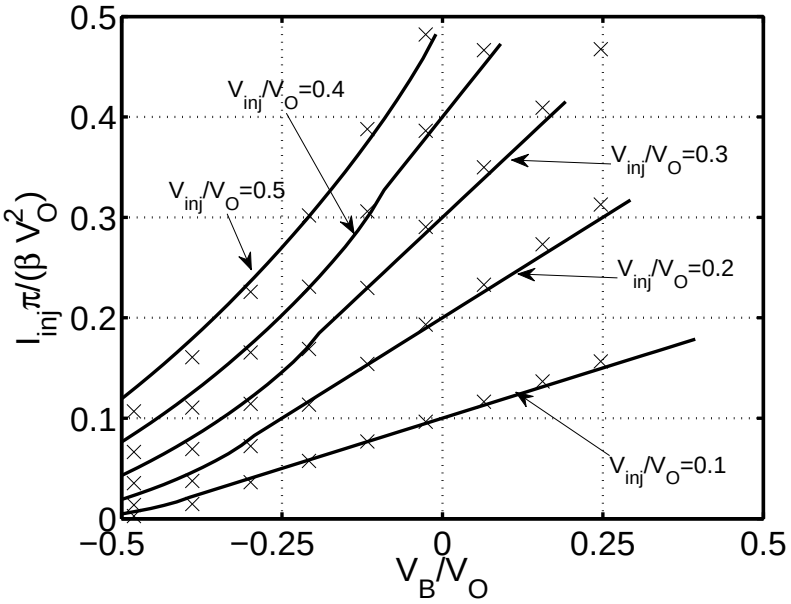


Figure 4.3 Normalized amplitude of the injection signal: theory (solid line) and transistor-level simulations (crosses).

Under this condition the last term of (4.4) turns out to be egligible and equation (4.4) can be simplified as:

$$I_{\text{inj}} \approx \frac{\beta}{\pi} V_O^2 \left[\frac{V_{\text{inj}}}{V_O} \left(1 + \frac{2V_B}{V_O} \right) d_{\text{on}} + \frac{3}{2} \frac{V_{\text{inj}}^2}{V_O^2} d_{\text{on}} \text{sinc}(d_{\text{on}}) \right] \tag{4.7}$$

Equation (4.7) shows that an injection device with a larger form factor, as well as a larger amplitude of the injection signal V_{inj} result in a larger locking range. Moreover, (4.7) points out that the bias conditions of M_{inj} also play an important role in determining the locking range.

In Fig. 4.3, the normalized injection amplitude $I_{\text{inj}}\pi/(\beta V_O^2)$ is plotted in solid line when (4.7) is valid, namely when the injection device never operates in triode. Transistor-level simulations with devices that follow the long-channel model (as assumed in the calculation) are also reported in Fig. 4.3 as crosses to validate the analysis. Quite good agreement is observed.

For higher values of V_B/V_O than shown in Fig. 4.3, M_{inj} is in triode part of the time, and the simulated curves flatten out, saturating to the limit value given by (4.8) for large V_B/V_O values. Short-channel effects result in a decrease of the injection amplitude, all the other parameters being the same. However, the trends described in Fig. 4.3 are

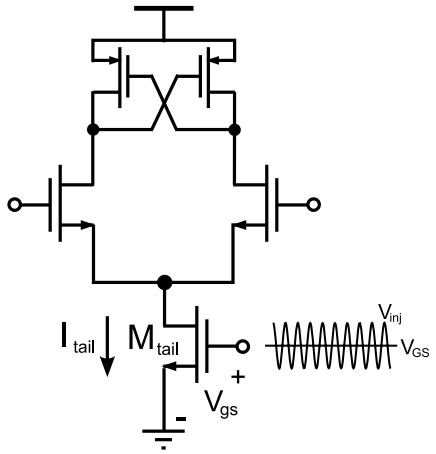


Figure 4.4 Schematic of the delay cell with tail injection device.

unaffected. From Fig. 4.3 it is clear that a large $V_{\rm inj}$ is not ultimately important, as a smaller amplitude of the injection signal can be compensated by an increase of V_B.

Notice that the limit condition for large values of V_B/V_O is that $M_{\rm inj}$ is always on and always in triode. As a consequence $\mathcal{D}_{S,1} = \mathcal{D}_{\rm ON,1} = 0$, and this condition gives an upper bound to $I_{\rm inj}$ for a given $V_{\rm inj}$:

$$I_{\rm inj} = \frac{2\beta}{\pi} V_{\rm inj} V_O. \tag{4.8}$$

4.2.1 Comparison with other injection techniques

It is interesting to compare the direct injection mechanisms described in the previous section and other schemes used in the literature. Focusing on the context of divide-by-two circuits based on ring oscillators and superharmonic injection locking, a commonly used technique is to inject the synchronization signal using the tail current generator of a differential amplifier employed as the delay cell (see Fig. 4.4) [24, 25, 35]. A signal of amplitude $V_{\rm inj}$ and frequency ω_h is superimposed to the dc gate-source voltage $V_{\rm GS}$ of the tail device $M_{\rm tail}$. The amplitude of the injection current flowing at frequency $\omega_{\rm inj}$ into the differential load is

$$I_{\rm inj,A} = \frac{2\beta}{\pi} V_{\rm ov} V_{\rm inj} \tag{4.9}$$

where $V_{\rm ov} = V_{\rm GS} - V_{t,n}$, and long-channel behavior is considered for simplicity. Comparing (4.8) and (4.9), and assuming $V_Q = V_O/2$, gives

$$\frac{I_{\rm inj}}{I_{\rm inj,A}} \approx \frac{V_{\rm CM} - V_{t,n}}{V_{\rm ov}} \tag{4.10}$$

which points out an advantage in the direct injection scheme since V_{CM} can be as large as V_{DD}, while V_{ov} is limited to guarantee that the tail device is always in saturation.

Another possibility is to drive M_{tail} in such a way that its drain current is a square wave commutating between 0 and $2I_B$ and frequency ω_h, I_B being the desired dc bias current for the delay cell. In this situation, (4.9) becomes

$$I_{\mathrm{inj,B}} = \frac{8}{\pi^2} I_B \tag{4.11}$$

and (4.10) turns into

$$\frac{I_{\mathrm{inj}}}{I_{\mathrm{inj,B}}} \approx \frac{\pi}{4} \frac{\beta(V_{\mathrm{CM}} - V_{t,n}) V_{\mathrm{inj}}}{I_B}, \tag{4.12}$$

suggesting that the two approaches may yield the same amount of injection signal for a sufficiently large I_B. However, in the case of tail injection in square wave regime, the relative injection level ε is fixed, since the amplitude of injection and the amplitude of oscillation are both proportional to I_B. On the other hand, in the direct injection scheme, ε is not limited by any fundamental constraint. One can select large V_{CM} and V_{inj} values without significantly affecting the operation of the ring oscillator, and without a large additional power consumption.

4.3 Circuit-level design

The ratio between the pMOS and nMOS devices of the delay cell of the ring is chosen to minimize the propagation time. As already mentioned in Sec. 2.3.1, the commutation of the gate takes place in two phases. At first, one branch is off, while the other one acts as a ratioed logic experiencing a high-to-low commutation. For this phase to be fast, large nMOS devices compared to the pMOS loads are beneficial. However, as soon as the voltage of the discharging node drops below $V_{DD} - |V_{t,p}|$, where $V_{t,p}$ is the pMOS threshold voltage, the cross-coupled pair turns on. The second phase is thus dominated by the latching transient for which large pMOS devices are required. The result is that the optimal condition is when the pMOS and nMOS transistor are sized approximately equal. The absolute dimensions of the devices ($W = 4.8\,\mu$m, $L = 0.06\,\mu$m) are selected as a compromise between power consumption, capability of driving loading capacitances, and matching between devices.

Large widths of M_{inj} result in a broad locking range as discussed in the previous section. The locking range obtained in simulation for different transistor widths is plotted in Fig. 4.5 for several values of V_{CM} and $V_{\mathrm{inj}} = 0.3$ V. The channel length is kept to the minimum allowed by the technology to minimize the capacitive parasitics. The simulation

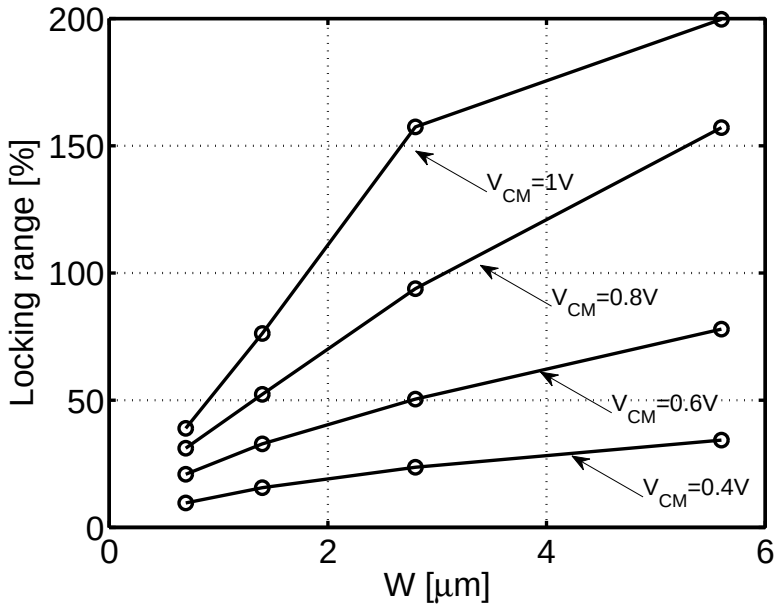


Figure 4.5 Simulated locking range vs. width of the injection device for different $V_{\rm CM}$ values and $V_{\rm inj} = 0.3$ V.

results confirm the outcome of the developed theory, predicting increased locking range for wider devices and for a higher dc gate voltage of $M_{\rm inj}$. As a trade-off between wide locking range and high frequencies of operation[1], in the design a width of $W = 2.8\,\mu$m has been selected for the injection devices.

In Fig. 4.6, the transistor-level simulation results are recast to yield the relative injection level ε at the edges of the locking range, expressed in terms of relative frequency ξ. The simulation data points refer to several widths of $M_{\rm inj}$ and values of $V_{\rm CM}$. The theoretical limit value of ε obtained evaluating (2.79) at equality is also plotted in Fig. 4.6 in solid line. There is quite an agreement between circuit-level simulations and analytical calculations, confirming the validity of the development carried out in Sec. 4.2.

Static CMOS inverters complete the design of the divider core. They are employed as buffers at each of the four ring oscillator nodes, as sketched in Fig 4.1.

In order to allow for testing, buffering stages have been designed to feed the divider and to drive the measurement equipment. The single-ended off-chip synchronization signal is converted into differential form by a resistively-loaded differential amplifier. A second identical stage removes the common-mode signal, while static CMOS inverters drive the injection devices. Ac-coupling between the differential amplifiers and the inverters allow

[1]The larger $M_{\rm inj}$, the bigger the parasitic capacitance.

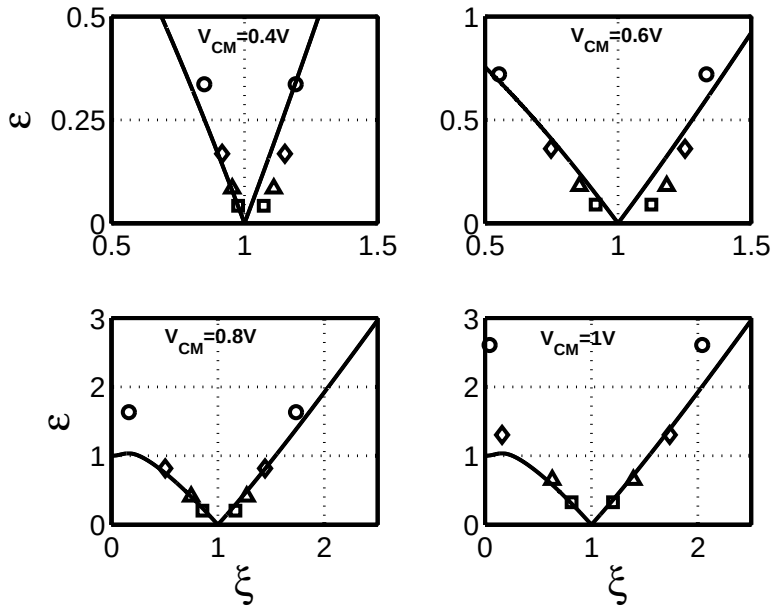


Figure 4.6 Simulated and calculated (solid line) relative injection amplitude for different widths of the injection device: $W = 0.7\,\mu$m (□), $W = 1.4\,\mu$m (△), $W = 2.8\,\mu$m (◇), and $W = 5.6\,\mu$m (○).

to bias the latter at their switching threshold. Due to the limited swing provided by the hard-switched differential amplifiers the CMOS inverters act more as amplifiers than digital gates. As a result, the differential signal provided to the injection devices is, depending on frequency, in the range of 300 to 600 mV, an amplitude easily achieved by integrated VCOs, even in low-supply-voltage technologies. The synchronization signal common-mode voltage (V_{CM}) can be independently set, as the CMOS inverters are ac-coupled to the gates of M_A and M_B. This is very important: To get a large locking range it is not ultimately essential to feed a large differential signal to the injection devices, but to realize a large modulation of their conductance at the synchronization signal rate. As a consequence, adjusting the common-mode voltage allows to compensate for the limited input signal swing. At the output, ac-coupled CML inverters are used to drive the measurement equipment.

4.4 Measurement results

Prototypes of the proposed design have been implemented in a low-power digital 65-nm CMOS technology and assembled in chip-on-board fashion for testing. A micrograph of

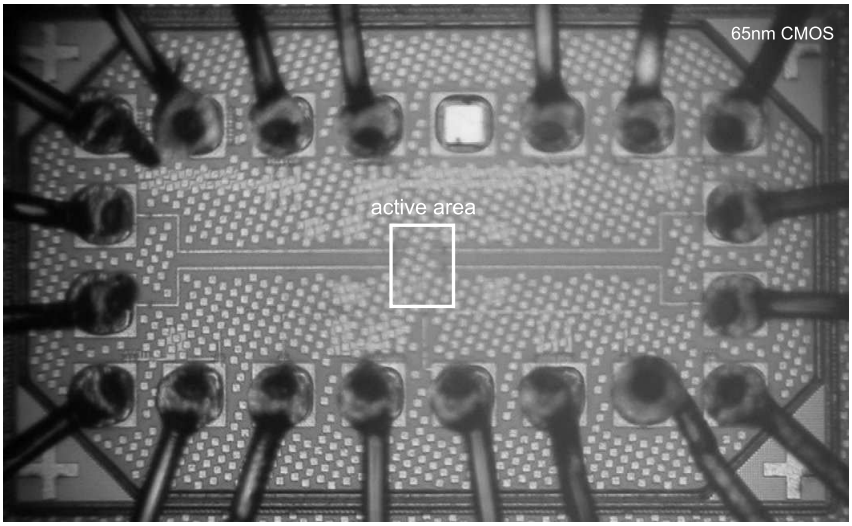


Figure 4.7 Chip micrograph.

the chip is shown in Fig. 4.7. The die is largely pad-dominated. The overall active area is just 0.006-mm^2, while the actual divider core takes as low as 130-μm^2.

The injection-locked divide-by-two operation is effective over a large range of frequencies, almost one decade. Figure 4.8 shows the input referred locking range for several values of V_{CM}. Clearly, an adequate value of the common-mode voltage is essential to achieve a large locking range, although more than 100% locking range is achieved for any value of V_{CM} higher than half the 1.2 V supply voltage. The largest observed locking range spans from 1.8 to 16.4 GHz at $V_{\mathrm{CM}} = 1$ V.

The measured input referred locking range extrema ($f_{h,H}$ and $f_{h,L}$) are compared in Fig. 4.9 with the predictions of the simulation and the theory developed in Sec. 4.2. We observe a quite good agreement between the estimated and the measured $f_{h,H}$ data, while there are larger discrepancies with regards to the lower frequency edge. Both the theory and the simulations yield more conservative results compared to the measurements.

The free-running oscillation frequency of the ring oscillator is 4.6 GHz. The output spectrum in this case is shown in Fig. 4.10, as well as in the case the divider is locked. The ring oscillator noise skirts are largely suppressed under injection locking.

Figure 4.11 shows the divider phase noise under locking condition measured at an input frequency of 16 GHz, that is in the worst case, at the top edge of the locking range. The phase noise of the synchronization signal is also reported for comparison. The 6-dB difference between input and output phase noise spectra confirms that the divider operates as expected. At large offsets ($\Delta f > 200$ kHz), the measurement setup

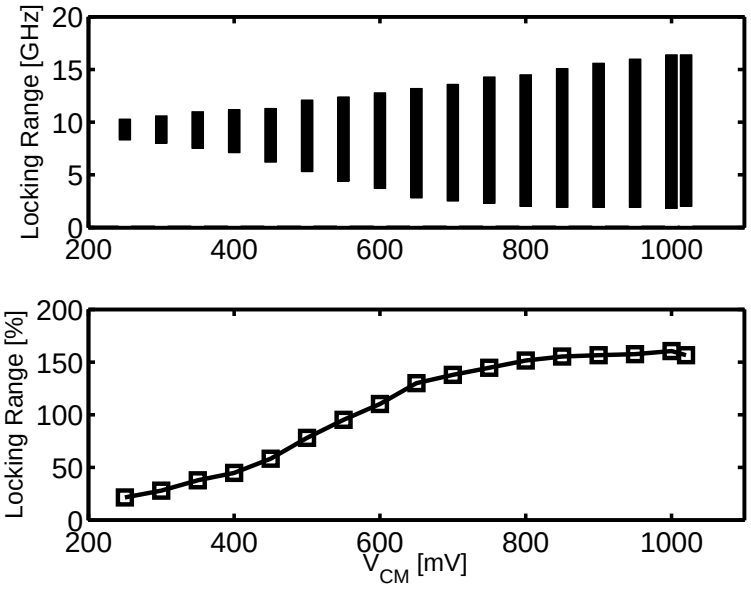


Figure 4.8 Measured locking range for several values of the input common mode voltage.

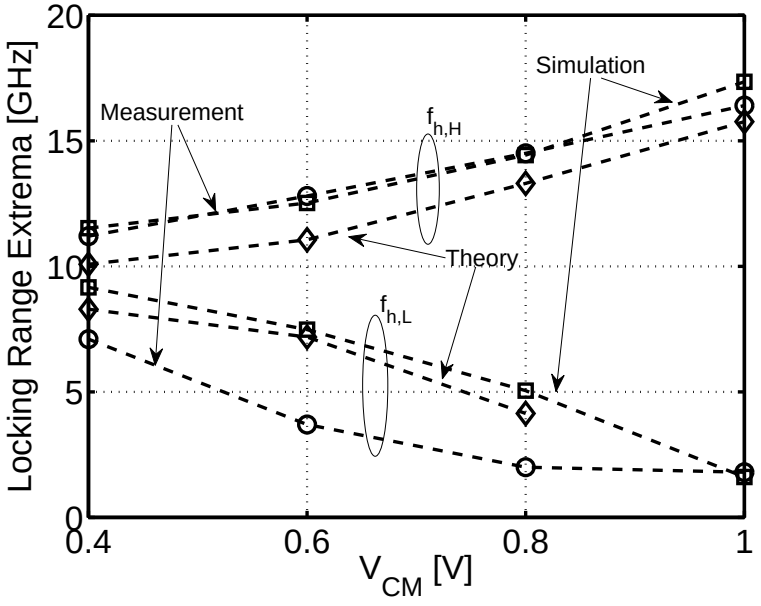


Figure 4.9 Input referred locking range extrema: comparison of measurement (∘), simulation (□) and theory (⋄).

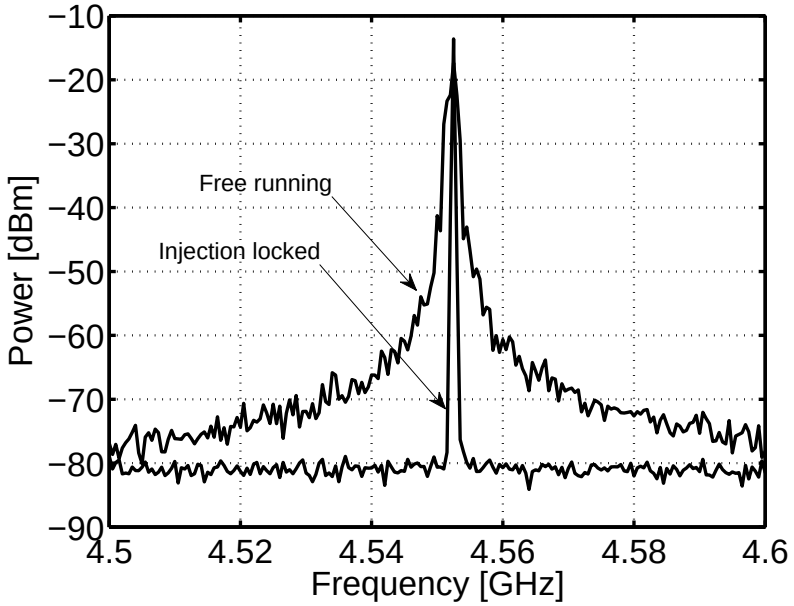


Figure 4.10 Measured divider spectrum in free running and under injection locking.

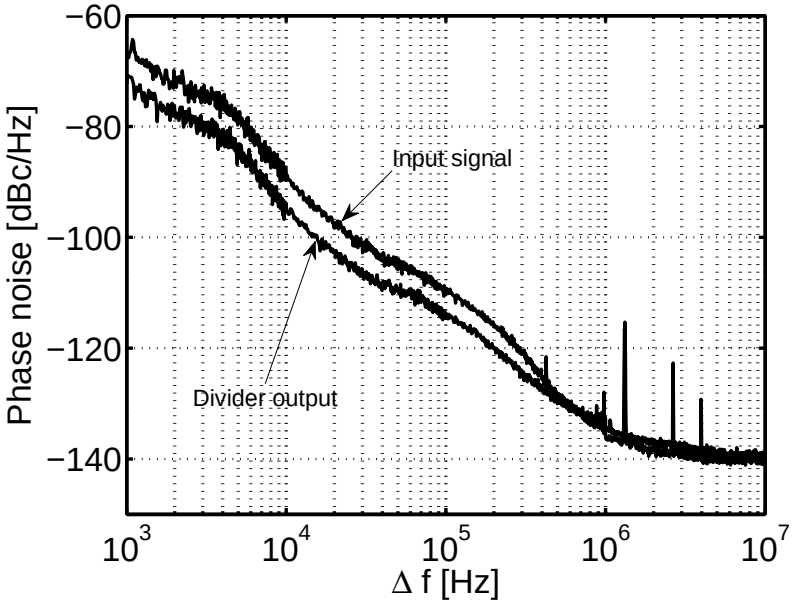


Figure 4.11 Measured phase noise of the locked divider and of the input signal at an input frequency of 16 GHz.

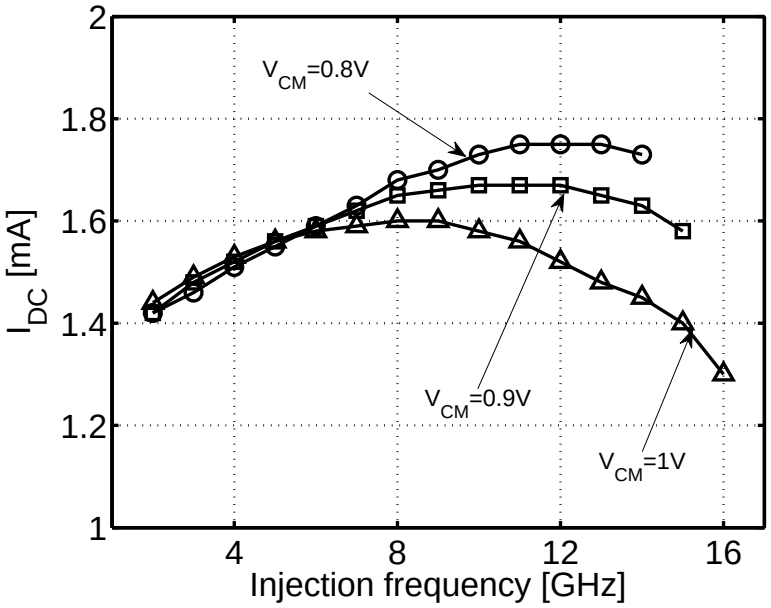


Figure 4.12 Measured dc current consumption of the divider vs. input frequency.

noise floor is observed. The spurious tones observed for $\Delta f > 1$ MHz are due to the measurement setup, as they also show up during the measurement of the phase noise of the input signal, i.e. when connecting the Agilent E8257D signal source directly to the Agilent E4407B spectrum analyzer.

The dc current drawn by the divider core at several input frequencies and for few values of V_{CM} is shown in Fig. 4.12. As the ring oscillator is basically a digital circuit, one would expect the current consumption to increase with the frequency, as opposed to the quite flat curves plotted in Fig. 4.12. In the presented design, the divider operates in an almost class-A fashion, which explains the observed current consumption. In any case the power consumption is lower than 2.1 mW. Varying the 1.2 V supply voltage by $\pm 10\%$ changes the free-running frequency of the ring oscillator. The locking range results shifted in frequency, but not changed in relative terms: It does not depart from the 160% measured in nominal conditions, as shown in Tab. 4.1.

In Tab. 4.2, the performance of the reported design is summarized and compared to other divide-by-two circuits based on injection-locked ring oscillators. With the exception of [25], our work clearly achieves a much wider locking range, using the smallest amount of area, and featuring the lowest power consumption. The work reported in [25], however, operates at much lower frequencies compared to our design, which has the potential to achieve an even broader locking range if tailored for the bottom end of the frequency

V_{DD} [V]	$f_{\min}$ [GHz]	$f_{\max}$ [GHz]
1.2	1.8	16.4
1.08	1.5	13.5
1.32	2.5	17.1

Table 4.1 Measured locking range vs. supply voltage.

	[24]	[35]	[36]	[37]	[25]	[34]	This work
Tech [nm]	180	130	180	130	130	180	65
Area [μm^2]	3000	1944	N/A	N/A	N/A	6700	130
V_{DD} [V]	1.8	1.2	1.8	2	N/A	1.8	1.2
$P_{\rm DC}$ [mW]	24	3.6	17.6	10.4	N/A‡	6.8	2
Lock range [GHz]	13-25†	11–15	1.95–5.5†	4–6	0.05–1.65	2.3–4.3	1.8–16.4
Lock range [%]	63†	31	95†	40	188	63	160

†Frequency range achieved over multiple bands by means of tuning.

‡Current consumption is 250 μA, supply voltage not reported.

Table 4.2 Summary of measured performance and comparison with the state-of-the-art.

spectrum, as shown in Fig. 4.5 and discussed in Sec. 4.3.

4.5 Conclusions

Direct injection locking applied to a non-harmonic oscillator proves in this paper to be a viable technique for the design of broadband low power frequency dividers. The use of an injection device, $M_{\rm inj}$, connected directly across the output terminals of the oscillator enables large locking ranges, since the injection mechanism results in large injection signals, and at the same time it does not at first order affect the oscillation amplitude. The proposed topology lends itself nicely to technology scaling, as it is ultimately built around logic gates. The designed prototypes, implemented in a low-power digital 65-nm CMOS technology, verify this statement: Experiments report a 2 to 16-GHz locking range, achieved with a 2-mW power consumption from a 1.2 V supply. The inductorless design occupies only 130-μm^2. The phase noise measured at the output of the divider tracks the reference's one with the theoretical 6-dB offset over the entire range of operation

frequencies.

Chapter 5

A 0.06 mm^2 11 mW local oscillator for the GSM standard in 65 nm CMOS

A GSM-compliant local oscillator consuming a tiny die area of only 0.06 mm^2 and drawing 9 mA from a 1.2 V supply has been designed in a 65-nm CMOS process using thin-oxide devices only. The system is made of a 13 to 15 GHz *LC* VCO followed by a divide-by-four injection-locked frequency divider. The divider employs a ring oscillator-based topology leading to a two octave locking range with limited area and power consumption. The phase noise at the output of the system is below -133 dBc/Hz at 3 MHz offset over the tuning range.

5.1 Introduction

While technology scaling helps reducing the area occupation, and thus the cost, for almost all kind of circuits, this is not true for those employing inductors, explaining the increasing interest for the inductorless systems. However, in some applications an inductorless approach is not viable to meet the system specifications. A noteworthy example is the GSM frequency synthesizer, where the strict phase noise requirements prevent the use of ring oscillators instead of *LC* VCOs. High-performance high-Q inductors tend to be bulky, and to consume a large amount of increasingly expensive silicon real estate. Further difficulties in satisfying the phase noise constraints come from the reduction of the supply voltage due to technology scaling, that results in smaller oscillation amplitudes. Highly pure oscillators would instead benefit of large oscillation voltages. Low supply

voltages are, however, only part of the problem, as circuits with LC tanks may swing over the supply. The standard thin oxide devices that usually come with the ultra-scaled digital CMOS technologies, on the other hand, are not designed to operate at such large voltages, so that high-swing oscillators call for the use of thick-oxide devices, a technology option that may be costly in terms of transistor parasitics.

One possible solution to simultaneously reduce the area consumption and improve the phase noise is to employ a higher frequency VCO followed by a frequency division system, as going to higher frequencies leads to smaller, reduced footprint, and often higher-Q, inductors [38]. However, this solution can be attractive only if the system that brings back the frequency to the desired value consumes a negligible amount of area and power with respect to the oscillator. Moreover, the phase-noise performance at the output of the divider should be compliant to the system specifications, and the divider should not impair it.

In this paper, we investigate the feasibility of designing a low-area low-power oscillator for GSM systems using standard supply voltages, and regular threshold-voltage standard thin-oxide devices only. We designed an LC VCO operating at eight times the frequencies needed in GSM systems, followed by an injection-locked divide-by-four frequency divider featuring a broad locking range. The divider is based on a ring oscillator. It does not require any inductor, it occupies a tiny silicon area, and it achieves a locking range in excess of two octaves while burning a fraction of the power of the VCO. The chip has been implemented in a 65-nm digital CMOS technology with a thick top metal layer and a standard 1.2 V supply. The phase noise at the divider output meets the GSM specifications without requiring any thick-oxide or low-threshold voltage device, nor any dedicated supply voltage.

5.2 System requirements and architecture

A frequency synthesizer suitable for all GSM systems is required to generate quite a wide range of carriers, as the GSM standard operates on many different portions of the spectrum. In the sketch in Fig. 5.1, the various uplink and downlink bands used by GSM850 and GSM900 are lumped together, as well as the frequencies for DCS1800 and PCS1900. From Fig 5.1, it is clear that a single high frequency oscillator spanning the spectrum from 13 to 16 GHz, along with a suitable set of frequency dividers, is sufficient to generate all the required carriers. It is well known that the oscillators for the GSM systems must feature high spectrum purity (see e.g. [39, 40]). The phase noise specifications are primarily set by the worst case blocker scenario for the receiver signal path, and by

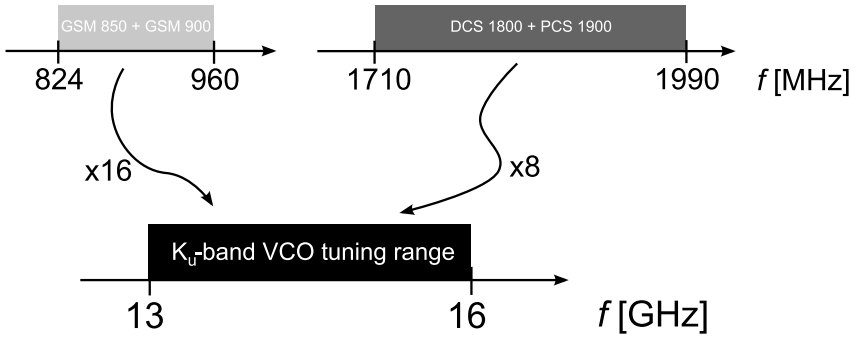


Figure 5.1 GSM bands.

Δf [MHz]	$\mathcal{L}(\Delta f)$ [dBc/Hz]	Set by
0.2	-59	GSM RX
0.4	-91	GSM RX
0.6	-110	DCS RX
1.6	-116	GSM RX
3	-127	DCS RX
6	-118	GSM TX
20	-150	GSM TX

Table 5.1 GSM phase noise requirements referred to a 3.6 GHz carrier.

limits on the out-of-band leakage for the transmitter. In Tab. 5.1, the set of the worst case phase noise specifications [39, 40] are reported for the different frequency offsets of interest, referred to a 3.6 GHz carrier.

The local oscillator (LO) implementation we propose in this work is based on a compact LC oscillator operating in the so-called K_u-band, from 13 to 16 GHz, ac-coupled to the input of an injection-locked inductorless divide-by-four prescaler. The LO architecture is reported in Fig 5.2. The divider outputs are buffered by two single-ended chains of static inverters sized to drive the 50 Ω load of the measurement setup. The buffers are only needed for testing purposes. In a GSM system, at least another divide-by-two stage is required to generate the actual carrier frequencies, as well as quadrature phases. Such an additional building block is out of the scope of this work.

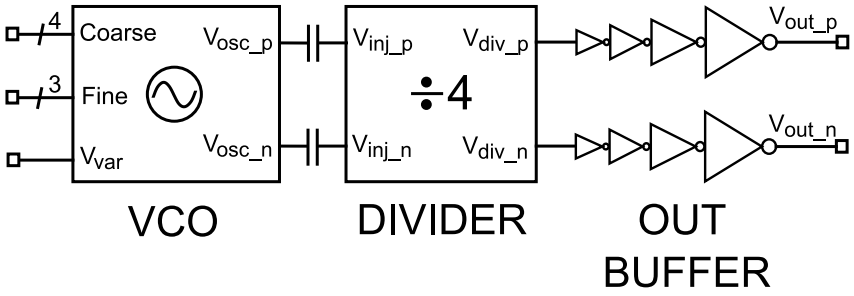


Figure 5.2 Block diagram of the implemented GSM local oscillator system.

5.3 Design of the K_u-band VCO

5.3.1 VCO topology and biasing scheme

The VCO is based on the well known differential *LC* topology with a cross-coupled nMOS pair, but it features a slightly modified biasing scheme [41]. As shown in Fig. 5.3, the bias current source is based on pMOS devices, and it is connected to the inductor center tap, as opposed to the source of the devices of the differential pair. As a consequence, the center tap of the inductor sits at a dc-voltage of about $V_{\rm dd}/2$. This scheme allows to achieve a large differential output voltage swing (almost 1.2 V zero-peak) without the need of a dedicated supply voltage. Moreover, the parasitic capacitance at the inductor central tap is not critical, and it can be conveniently used to filter out the high frequency noise contribution of the current source, avoiding its frequency downconversion and translation into phase noise.

Since at first order the parasitic capacitance of the pMOS tail device does not have any negative impact on the performance of the oscillator, a longer channel length can be selected for the pMOS transistors of the current mirror, thus reducing the flicker noise produced by the bias network. Moreover, as the voltage at the inductor central tap sits at the gate-source dc voltage of the nMOS devices, M_3 enjoys a large drain-source voltage (roughly $V_{\rm dd}/2$), and it is easily well in saturation during the entire oscillation cycle.

The dimension of the cross-coupled nMOS devices M_1 and M_2 has been selected based on oscillation start-up requirements at the lowest frequency of the tuning range, which is the worst case.

It is worthwhile to notice that in the designed circuit none of the node voltages exceeds 1.35 V (i.e. $V_{\rm dd} + 10\%$). As such, only thin-oxide devices are required, while achieving large output voltage swings.

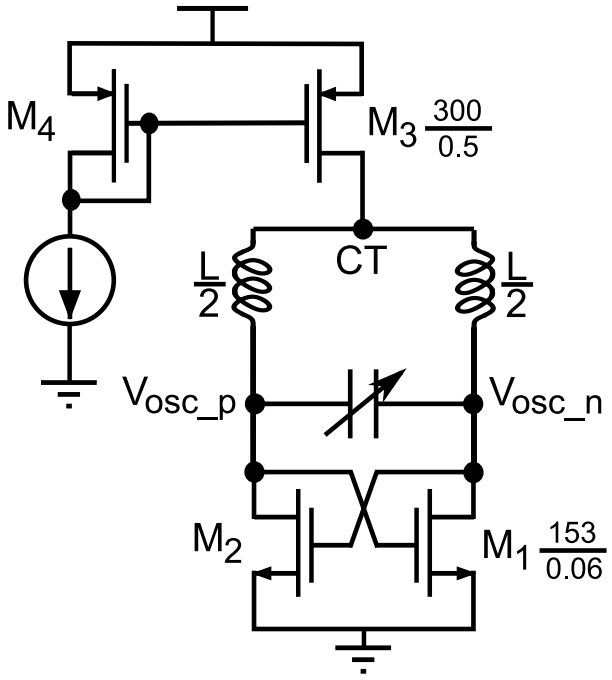


Figure 5.3 Schematic of the *LC* VCO.

5.3.2 Tank optimization and modeling

The design of the inductor is one of the main challenges in the design of VCOs. The inductance value has to be chosen as a compromise between power consumption, achievable tuning range, area consumption, and phase noise. To maximize the inductance per area ratio an octagonal shape has been chosen, while to maximize the quality factor the two top layers of the metal stack have been used connected together by many vias. Two single-turn inductors were designed to meet the stringent GSM phase noise requirements. The two coils feature 100 pH and 150 pH inductance. As a consequence, two VCO versions are designed with different tank elements out of the same basic topology (see Sec. 5.3.1); they are tailored for different bias current levels. The inductors were simulated using an electro-magnetic (EM) tool. Simulation results for the 100 pH coil, shown in Fig. 5.4 in solid line, indicate that the quality factor is in excess of 20 in the range of frequencies of interest. The performance of the 150 pH inductor is quite similar.

To perform time-domain simulations of the designed VCO, a lumped model of the inductor, reported in Fig. 5.5, was derived following the guidelines described in Sec. 1.2. In the following we just briefly summarize its characteristics, sending the reader to Sec. 1.2 for a complete description of the model and of the fitting of the components. The model was derived assuming the inductor is symmetrical, then the shunt impedance connected be-

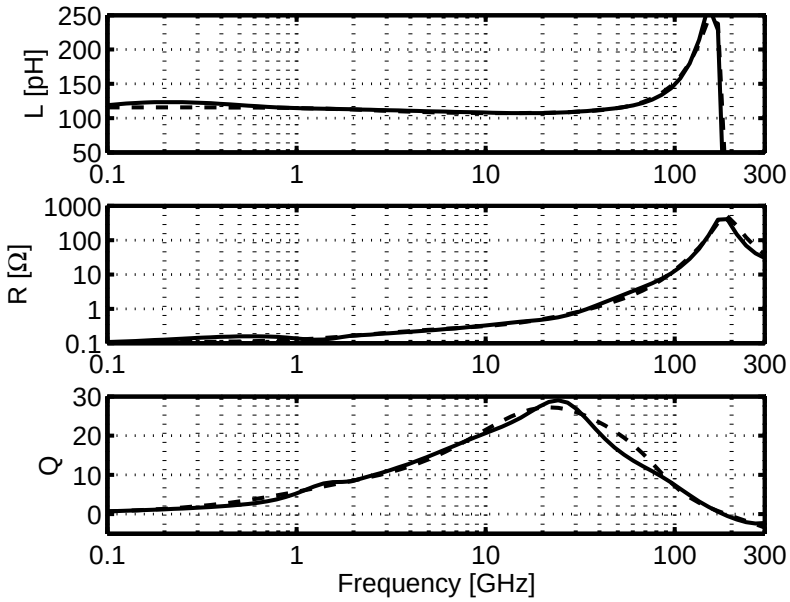


Figure 5.4 EM simulations of the 100 pH inductor (solid line) as well as frequency response of the equivalent lumped model (dashed line).

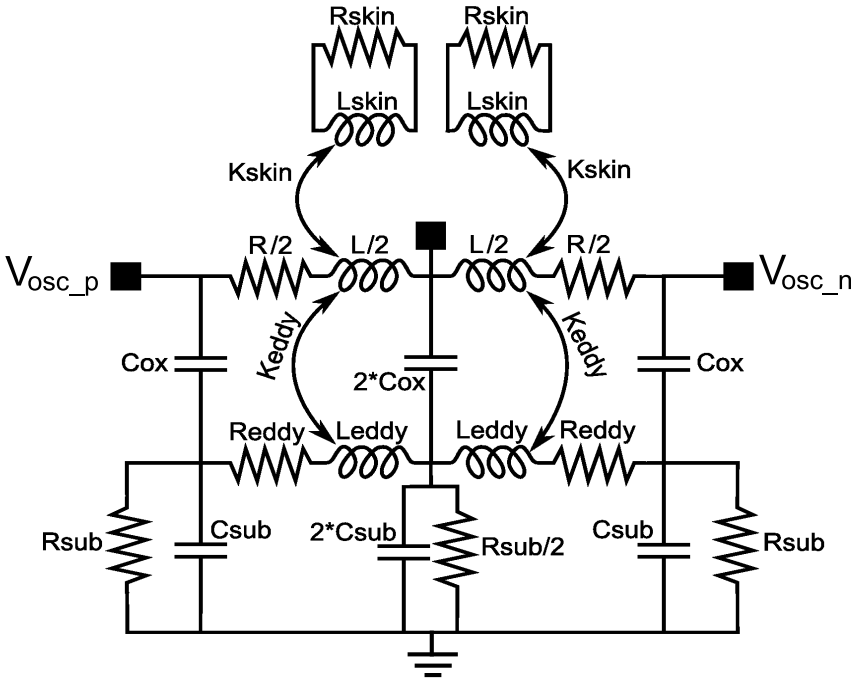


Figure 5.5 Schematic of the wideband lumped model of the inductor.

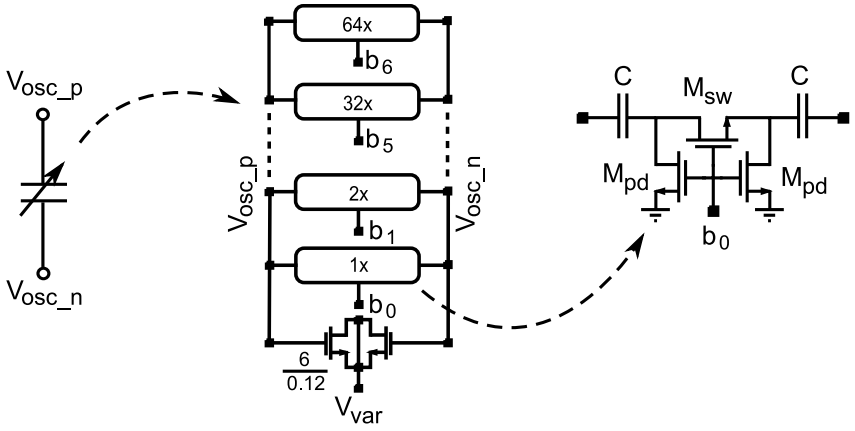


Figure 5.6 Arrangement of the varactor and the capacitor bank.

tween the central tap and ground is the parallel combination of the two shunt impedances connected to the other two terminals of the inductor. The skin effect was modeled using the transformer loop made of the resistor R_{skin} and the inductor L_{skin}, which is coupled to $L/2$. It results in an increase of the inductance and of the trace resistance at higher frequencies. The substrate coupled network made of the inductor L_{eddy} and the resistor R_{eddy} models the eddy currents, taking care of the losses generated in both the horizontal and vertical directions. On the one hand, the complexity of the presented model requires more efforts in extracting the values of the model parameters from the EM simulation data. On the other hand, it provides a very wide-band matching between the EM simulation and the lumped model frequency response, as shown in Fig. 5.4.

The tank capacitance is divided in a 7-bit capacitor bank plus a small varactor to allow for continuous frequency tuning, as shown in Fig. 5.6. With respect to using only varactors, this arrangement limits the AM to PM noise conversion. The varactor size has been chosen to guarantee overlap among all the sub-bands. The four most significant bits implement a coarse tuning, while the three least significant bits are for fine tuning. In any case, they all result from binary weighting an array of 127 switched capacitor unit-cells (see Fig. 5.6). The width of the transistor $M_{\rm sw}$ has been chosen as a compromise between the quality factor of the capacitor bank, Q_C, and the tuning range. The larger the switch, the higher the quality factor, but the lower the on/off capacitance ratio of the switched capacitor unit-cell. The pull-down transistors $M_{\rm pd}$ only have to set the dc voltage at the drain and at the source of $M_{\rm sw}$ to ensure it turns on appropriately. They are designed with minimum channel width, and longer than minimum length.

It is worthwhile to notice that, as we pointed out in Sec. 1.1, the quality factor Q_C

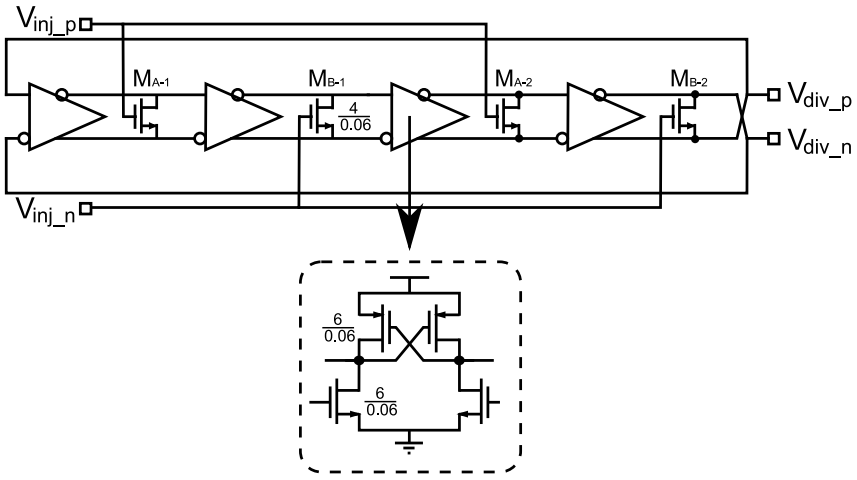


Figure 5.7 Schematic of the injection-locked divide-by-four frequency divider.

is strongly affected by the (parasitic) contribution of the switched capacitances in the off state, especially at the higher end of the tuning range. Usually, when designing the capacitor bank, the designer is used to consider only the quality factor of the unit cells in the on state for the computation of the capacitor bank quality factor. In such a case the quality factor result to decrease with frequency and the unit cell is designed to meet the quality factor specifications at the highest border of the tuning range. At the contrary, as we demonstrated in Sec. 1.1, taking into account the contribution of the switched capacitances in the off state the quality factor increases with frequency and the unit cell can be designed to meet the quality factor specifications at the highest border of the tuning range. This gives some additional headroom in the design of the capacitor bank. For a target tank quality factor Q_T, and for a given technology, smaller transistors may be employed as switches, reducing the parasitic capacitances, and thus achieving a wider tuning range. Figure 1.7 compares the values of Q_T predicted by (1.22) (plotted in solid line) to circuit-level simulations (circles), showing very good agreement.

5.4 Inductorless injection-locked divide-by-four frequency divider

The divide-by-four injection-locked frequency divider is of the same topology analysed in Sec. 2.3 and implemented as divide-by-two in Chapter 4. Although, in this case the divider is built around a four stage ring oscillator, as sketched in Fig 5.7. To this regard, it is worth to notice that the choice of four stages in the ring oscillator is not mandatory, as

any other number of delay cells would in principle be adequate. However, this particular choice results in the requirement of a sequence of phases spaced by steps equal to π to implement the multiple input scheme [24, 25], which is very convenient, as differential signals are readily available at the VCO output.

The injection signal is in the form of (2.95):

$$s_{\text{inj}}(t) = I_{\text{inj}} \cos(\omega_{\text{inj}} t + \varphi) + \tilde{s}_{\text{inj}}(t) \tag{5.1}$$

where now $\omega_{\text{inj}} = \omega_h/4$, and ω_h is the frequency of the injection signal. The analysis to derive the amplitude of I_{inj} is the same as reported in Chapter 4, with the only difference that in this case the harmonics of the output voltage that cause beating tones at ω_{inj} are the 3^{rd} and the 5^{th}. As a consequence the analysis will not be repeated and we only report the final value of the upper bound for I_{inj} derived in (4.8):

$$I_{d,\omega_{\text{inj}}} = \frac{4\beta}{15\pi}(V_{\text{CM}} - V_{t,n})V_{\text{inj}}, \tag{5.2}$$

It has been calculated in the same way as (4.8), but considering the 3^{rd} and the 5^{th} coefficient of the Fourier series of $D_T(t)$ and $D_S(t)$. All the consideration remains the same as the divider by two. Injection device with a larger form factor, as well as a larger amplitude of the injection signal V_{inj} result in a larger locking range. Moreover, (4.7) points out that the bias conditions of M_{inj} also play an important role in determining the locking range, as a smaller amplitude of the injection signal can be compensated by an increase of V_B.

Figure 5.8 shows the simulated locking range of the implemented divider for several values of V_{inj} (the peak-to-peak amplitude is annotated in the plot), and V_{CM} =0.8 V. For the amplitudes of the input signal we expect to get from the VCO across its tuning range (from 0.8 to 1.2 V), the locking range of the divider covers more than two octaves of the input frequency without requiring any calibration nor tuning. In particular, for a rail-to-rail input signal the locking range spans from 3 to 17.7 GHz, which is quite a remarkable result.

The area occupation of the divider is only 9×23 μm^2. The small dimensions of the divider, combined with its broad locking range, and the limited power consumption (2.4 mW) enable the use of the compact K_u-band VCO discussed in Sec. 5.3 for the generation of the GSM carriers. Moreover, since the divider is ultimately based on digital gates, it benefits from the technology scaling, while it is lower power than purely clocked digital circuits, as the divider circuitry switches at the output frequency rate.

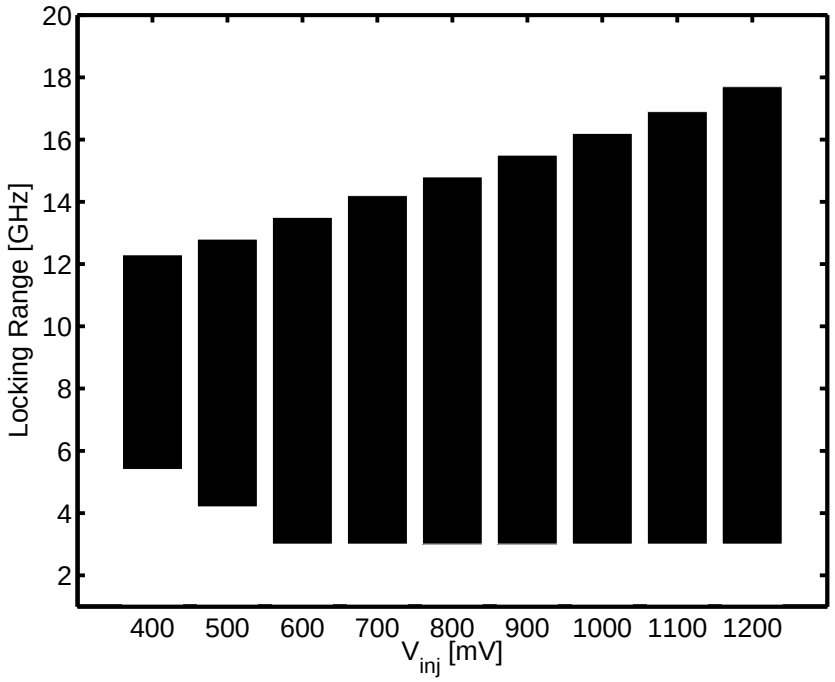


Figure 5.8 Simulated frequency divider locking range for V_{CM} =0.8 V and several values of V_{inj} (peak-to-peak amplitude is annotated in the plot).

5.5 Measurement results

The designed system was implemented in a digital 65 nm low-power CMOS process with a thick top metal layer, and a 1.2 V supply voltage. Only thin-oxide devices with standard threshold voltage were employed throughout the design. Two versions of the VCO were implemented, one featuring a 100 pH inductor, the other featuring a 150 pH inductor. Both VCOs were followed by the same divider circuit and testing buffers. The silicon active area occupied by the VCO, the divider, and the buffers is as small as 0.21 × 0.28 mm^2 for the version with the 100 pH inductor, and slightly larger, 0.21 × 0.3 mm^2, for the version with the 150 pH coil. A microphotograph of the die featuring the 100 pH inductor is shown in Fig. 5.9. The circuits draw a total current of 9 mA: 7 mA are drawn by the oscillator, and 2 mA by the divider. In the case of the VCO with the larger inductor, the VCO current can be reduced to 4 mA at the higher end of the tuning range without any phase noise penalty.

The measured tuning range, at the output of the divider, spans from 3.2 to 3.75 GHz for the design with the 100 pH inductor. The 16 tuning sub-bands resulting from the 4-bit coarse tuning are shown in Fig. 5.10. They clearly overlap. The tuning range is

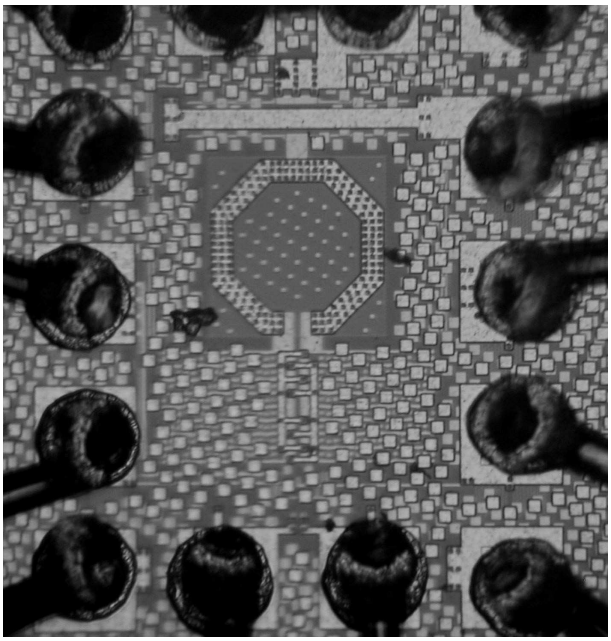


Figure 5.9 Chip microphotograph of the design with the 100 pH inductor. Active area is only 0.06 mm^2.

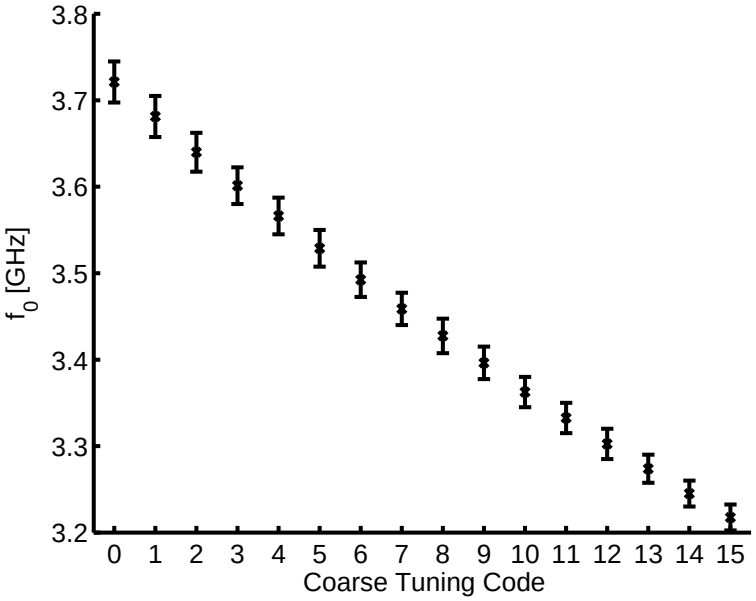


Figure 5.10 Measured coarse tuning sub-bands for the design with the 100 pH inductor.

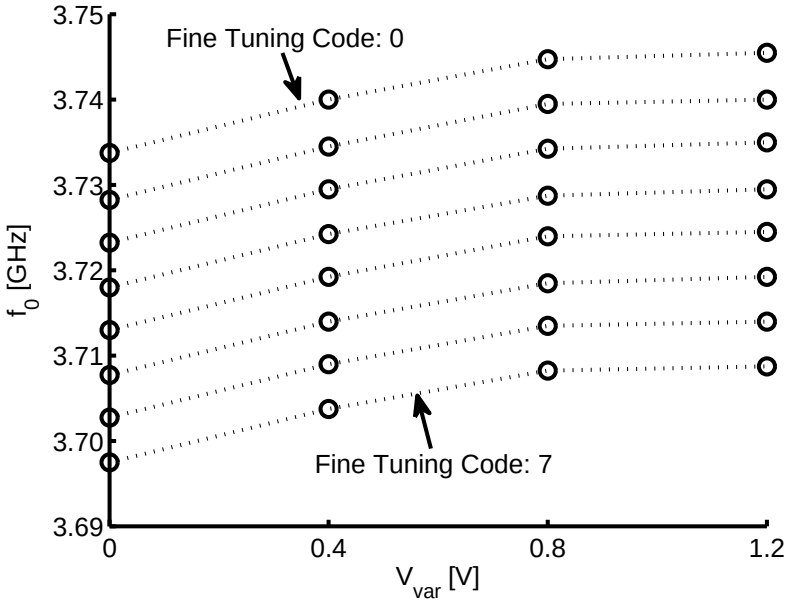


Figure 5.11 Measured oscillation frequencies for the design with the 100 pH inductor: fine tuning at the higher coarse tuning sub-band.

wide enough to cover almost every GSM band, although a redesign is required to expand the tuning range at the higher side and fully cover the downlink PCS channels. The observed discrepancy between the measurements and the design target was tracked back to a decrease of the $C_{\text{on}}/C_{\text{off}}$ ratio in the actual prototypes compared to the simulation results.

To illustrate the 3-bit fine tuning and the varactor operation in the implementation with the 100 pH inductor, the 8 fine tuning sub-bands are shown in Fig. 5.11 for the higher frequency coarse tuning, which is the worst case. Sweeping the control voltage of the varactor from 0 V to 1.2 V one can cover almost two fine tuning sub-bands, ensuring continuous tuning over the entire frequency range.

The use of the 150 pH inductor resulted in some additional parasitic capacitance, that was not accounted for in the design phase. This leads to a some 200 MHz frequency shift in the measured tuning range, which, in this case, spans from 3 to 3.5 GHz at the divider output. Figure 5.12 shows the coarse frequency tuning, while Fig. 5.13 illustrates the fine frequency tuning of the design with the 150 pH inductor.

As in the version with the 100 pH inductor, the entire tuning range can be continuously scanned by acting on the digital coarse and fine codes, as well as on the varactor control voltage without any gap.

A frequency-pushing measurement was performed varying the oscillator supply voltage

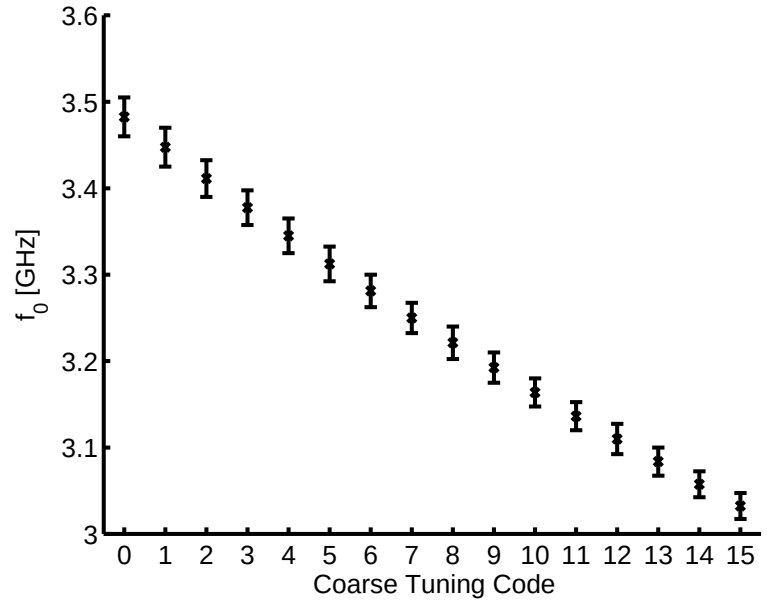


Figure 5.12 Measured coarse tuning sub-bands for the design with the 150 pH inductor.

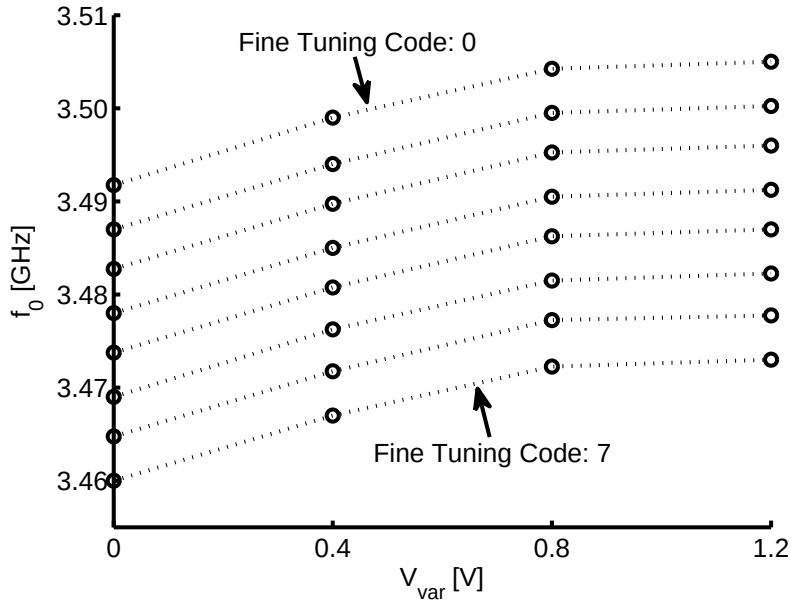


Figure 5.13 Measured oscillation frequencies for the design with the 150 pH inductor: fine tuning at the higher coarse tuning sub-band.

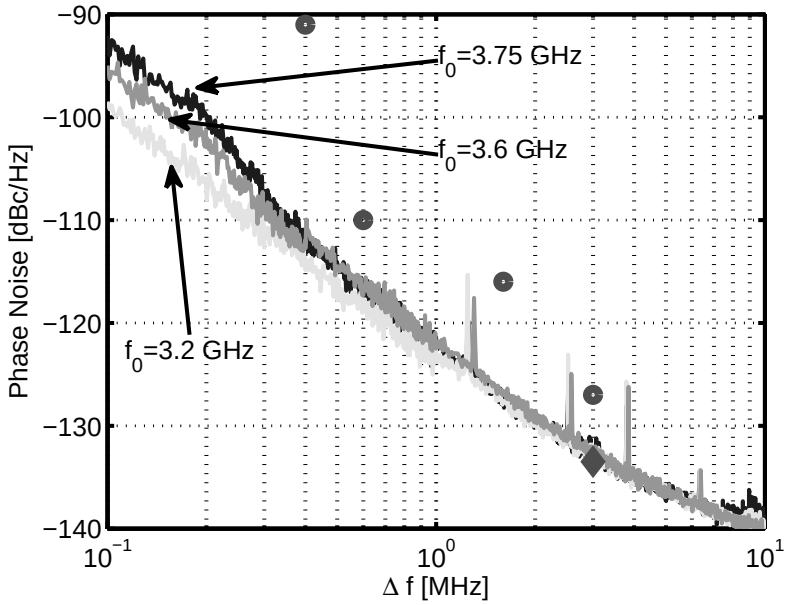


Figure 5.14 Measured phase noise at the two edges of the tuning range and at 3.6 GHz for the design with the 100 pH inductor. Dots indicate the GSM requirements. The diamond is the requirement at 20 MHz offset, referred back to the 3 MHz offset.

at constant bias current. For both designs, the resulting sensitivity is 3 MHz/V, and 20 MHz/V at the low-end and the high-end of the tuning range, respectively.

The phase noise was measured at the two edges of the tuning range, and at 3.6 GHz. The results are plotted in Fig. 5.14 for the implementation with the 100 pH inductor. For the 3.6 GHz carrier the phase noise is -95, -117, -122, -133 dBc/Hz for 0.1, 0.6, 1, and 3 MHz frequency offsets, respectively. The dots and the diamond represents the GSM requirements [39, 42], referred to 3.6 GHz. The diamond is the requirement at 20 MHz offset referred to 3 MHz offset. Our system clearly meets all the GSM phase noise specifications with quite a margin, with the exception of the requirement at 20 MHz offset, where it is just on target. As a consequence, further phase noise improvements are required to allow for some robustness of the design. However, note that the specification at 20 MHz offset is set assuming no attenuation in the TX path at the RX frequencies [39]. Any additional filtering would therefore relax the required far-off phase noise performance.

The phase noise of the two versions of the implemented prototypes is compared at the higher and lower ends of the tuning range in Figs. 5.15 and 5.16, respectively. Clearly, the designs show almost the same phase noise performance. Nevertheless, as a result of the use of a larger inductor, a lower bias current can be employed in the VCO with the

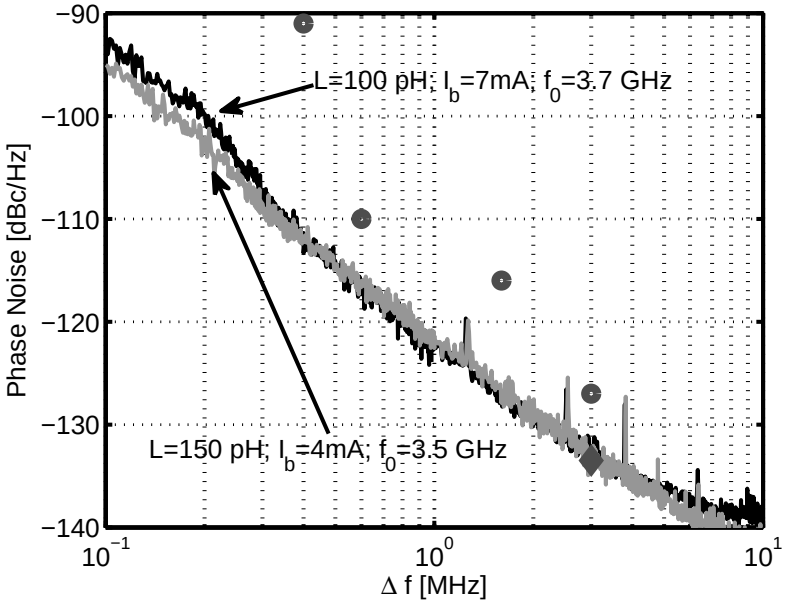


Figure 5.15 Measured phase noise at the lower frequency of oscillation for both implemented designs. Dots indicate the GSM requirements. The diamond is the requirement at 20 MHz offset, referred back to the 3 MHz offset.

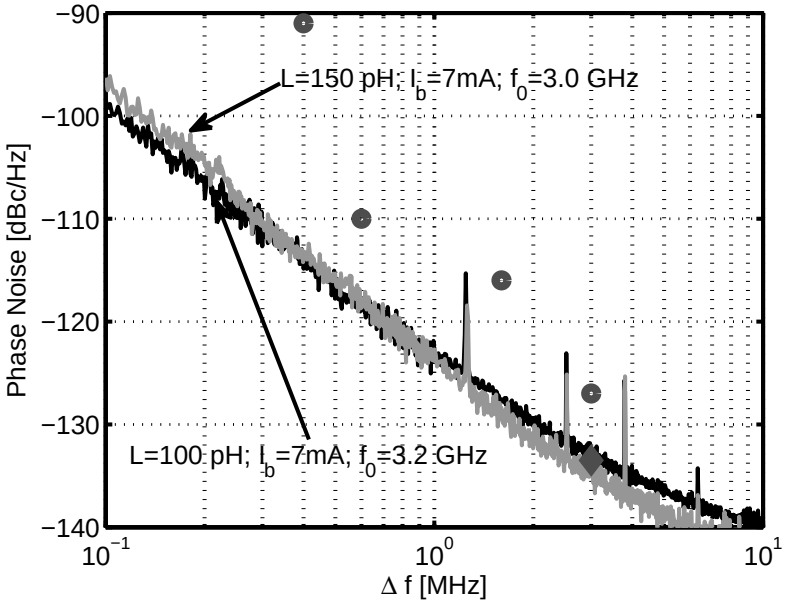


Figure 5.16 Measured phase noise at the higher frequency of oscillation for both implemented designs. Dots indicate the GSM requirements. The diamond is the requirement at 20 MHz offset, referred back to the 3 MHz offset.

Technology	65 nm digital CMOS
Active area	0.06 mm^2
Supply voltage	1.2 V
VCO current	7 mA
Divider current	2 mA
Total power (VC0 + divider)	11 mW
Tuning range	3.2–3.75 GHz
Tuning sensitivity (K_{VCO})	$\leq$ 14 MHz/V
Pushing	$\leq$ 20 MHz/V
$\mathcal{L}(f_0$=3.6 GHz, Δf=100 kHz)	-95 dBc/Hz
$\mathcal{L}(f_0$=3.6 GHz, Δf=600 kHz)	-117 dBc/Hz
$\mathcal{L}(f_0$=3.6 GHz, Δf=1 MHz)	-122 dBc/Hz
$\mathcal{L}(f_0$=3.6 GHz, Δf=3 MHz)	-133 dBc/Hz

Table 5.2 Performance summary.

150 pH inductor, without any penalty. The lower power dissipation, however, comes at the price of larger parasitics that cause the observed shift in the oscillation frequency. The bottom line is that all the conventional trade-offs that are typical of the VCO design at lower frequencies are still there in the proposed circuits, emphasizing that going to higher frequencies does not shrink the design space.

Table 5.2 summarizes the performance of the designed system, as obtained in the version with the 100 pH inductor. In addition to the measurement data previously discussed, the sensitivity of the oscillation frequency to the varactor control voltage, that is the parameter often labeled as K_{VCO}, is reported. It is measured to be less than 14 MHz/V.

Table 5.3 compares our circuit with other GSM oscillators using the following figure-of-merit (FOM) [43]:

$$FOM = 10\log\left[\frac{k_B T}{P_{\mathrm{DC}}}\left(\frac{f_0}{\Delta f}\right)^2\right] - \mathcal{L}(\Delta f), \tag{5.3}$$

where P_{DC} is the oscillator power consumption, f_0 is the oscillation frequency, $\mathcal{L}(\Delta f)$ is the phase noise, and Δf is the offset from the carrier. Our circuit shows a FOM comparable with the state-of-the-art, despite the additional power consumption due to the divider. Moreover, the silicon area of the proposed work is remarkably smaller.

VCO	Tech. [μm]	FOM [dB]	Frequency [GHz]	Area [mm^2]
[41]	0.7	3.8	1.8	0.563
[42]	0.25	9.22	1.82	N/A
[44]	0.25	11.5	1.8	1.05
[39]	0.35	14.9	0.915	3.57
[5]	0.18	11	1.8	1.7
[4]	0.13	22	4.9	N/A
[This]	0.065	10.4	3.6	0.06

Table 5.3 Performance comparison.

5.6 Conclusions

This work demonstrates the possibility of implementing a GSM oscillator that only needs 0.06 mm^2 of silicon area, and that does not require any special device, nor any dedicated power supply. This result is achieved by combining a K_u-band VCO and an injection-locked frequency divider based on a ring oscillator. The VCO operates at 15 GHz. It has been designed as a modified version of the standard nMOS cross-coupled pair differential oscillator in order to maximize the output voltage swing and to reduce the flicker noise. The divider consumes an area of only 9×23 μm^2, that is only the 0.35% of the entire silicon active area. In this way, the area occupation is limited by the area of a circuit that works at a much higher frequency than the desired one, allowing for the use of a smaller inductor. The designed chip, implemented in a 65 nm CMOS technology, consumes 11 mW of power, while satisfying the stringent phase noise requirements of the GSM standard. The measured phase noise is -133 dBc/Hz at 3 MHz offset from a 3.6 GHz carrier.

Conclusions

In this thesis we propose the use of injection locking as an efficient way to realize low power, low area building blocks for RF frequency generation in ultra-scaled CMOS technologies.

A thourough analysis of both *LC* and ring oscillations under injection locking was carried out. In *LC* oscillator we investigate the response of the oscillator in presence of a multi-tone synchronization signal and we derived an analytical expression to evaluate the locking transient. In ring oscillator we developed a behavioral model that allows to capture the operation of the oscillator and single out the mechanisms of the super-harmonic injection locking. Then, the analysis results have been used to established the guide-lines and the trade-offs in the design part of the thesis.

The use of sub-harmonic injection locking as promising option to generate the fast-hopping carriers required in multi-band UWB systems is demonstrated. A very small area 0.074 mm^2 chip prototyped in 90 nm CMOS synthesizes the frequencies of band group ♯6 with a hop time shorter than 4 ns. Power consumption, including IQ-generation, is 30 mA from a 1.2 V supply. Phase noise at 8.71 GHz is -112 dBc/Hz at 1 MHz offset.

The use of direct injection locking applied to a ring oscillator has been proved to be a viable technique for the design of broadband low power frequency dividers. A divide-by-two divider prototype, was implemented in a low-power digital 65-nm CMOS technology. Experiments report a 2 to 16-GHz locking range, achieved with a 2-mWpower consumption from a 1.2 V supply. The inductorless design occupies only 130-m2. The phase noise measured at the output of the divider tracks the references one with the theoretical 6-dB offset over the entire range of operation frequencies.

Moreover we demonstrated the possibility of implementing a GSM oscillator that only needs 0.06 mm2 of silicon area, and that does not require any special device, nor any dedicated power supply. This result is achieved by combining a VCO at 15 GHz and with the injection-locked frequency divider. The VCO has been designed as a modified version of the standard nMOS cross-coupled pair differential oscillator in order to maximize the output voltage swing and to reduce the flicker noise. The divider consumes an area of only 9×23 mm^2, that is only the 0.35% of the entire silicon active area. In this way, the

area occupation is limited by the area of a circuit that works at a much higher frequency than the desired one, allowing for the use of a smaller inductor. The designed chip, implemented in a 65 nm CMOS technology, consumes 11 mW of power, while satisfying the stringent phase noise requirements of the GSM standard. The measured phase noise is -133 dBc/Hz at 3 MHz offset from a 3.6 GHz carrier.

Appendix A

Building Blocks For Step Frequency Radar

A.1 Introduction

Breast cancer is the most common cancer among American women, except for skin cancers and it is the second leading cause of cancer death in women, exceeded only by lung cancer [45]. The current method of detection is mammography, which involves X-ray imaging of a compressed breast. Although mammography is the gold standard, concerns related to the false-positive and false-negative rates exist. Further, it requires uncomfortable or painful breast compression, and exposure to low levels of ionizing radiation. Other modalities such as ultrasound and magnetic resonance imaging (MRI) are either less effective or too costly.

One of the promising alternatives is the microwave breast cancer detection that relies on differences in electrical properties between malignant and fatty tissues. Hagness et al. [46] proposed a radar-based microwave breast imaging method, that relies on differences in electrical properties between malignant and fatty tissues to transmits a low-power UWB signal into the breast and records the backscatter.

An UWB microwave radar technique for breast cancer detection involves transmitting a short duration pulse and receiving an echo signal for different locations of a probe antenna (or for a fixed location of a switched beam array antenna). In practice, such pulse can be produced using a step-frequency pulse synthesis technique. In this technique measurements are carried at equidistant frequencies over a large band, and their time/space domain equivalent is obtained using an Inverse FFT (IFFT). By combining the received signals for various locations of the probe antenna, an image is created.

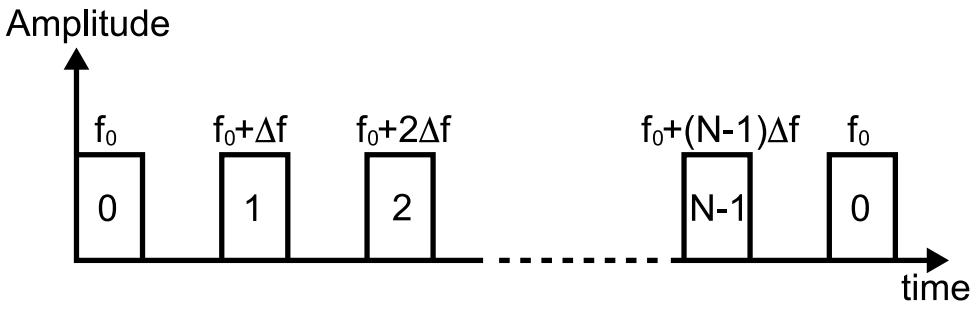


Figure A.1 Waveform of the step frequency radar.

In the last period of my Ph.D. I worked on the design of some blocks of a step-frequency radar (SFR) for breast cancer detection, more in particular in the design of the VCOs and the frequency dividers of the PLL. In the following we present the design of those blocks. However, since the design of the whole radar system requires the work of different people and takes some time, the chip has not been taped-out jet and we possess only post layout simulation results. The design was realized in a 65 nm technology, with a 1.2 voltage supply.

A.2 Step-Frequency radar introduction

A SFR transmits sequences of N pulses at fixed repetition frequency but a different radar frequency. A picture of the step frequency waveform is shown in Fig. A.1. Each pulse in the sequence has the same pulse width but different carrier frequency. The carrier frequency of the pulse is linearly increased from pulse to pulse by a fixed increment Δf. Then for the k^{th} transmitted pulse in the sequence, with $k = 0, 1, ...N-1$, the carrier frequency is given by:

$$f_k = f_0 + k\Delta f \tag{A.1}$$

If the transmitted pulse signal for the k^{th} pulse is:

$$s_t(t) = A_t cos\left(2\pi f_k t\right) \tag{A.2}$$

then the target signal received after a delay of $\tau = 2R\sqrt{\varepsilon_r}/c$ is given by:

$$s_r(t) = A_r cos\left[2\pi f_k\left(t - \frac{2R\sqrt{\varepsilon_r}}{c}\right)\right] \tag{A.3}$$

where R is the range of the target, ε_r is the relative dielectric constant of the medium, and c is the velocity of light.

Assuming a quadrature direct conversion topology on the receiver side, the signal at the output of the mixer is:

$$S(t) = I(t) + iQ(t) \tag{A.4}$$

where

$$\begin{aligned} I(t) &= A cos(\Psi f_k) \\ Q(t) &= A sin(\Psi f_k) \end{aligned} \tag{A.5}$$

and

$$\Psi = \frac{-4\pi R\sqrt{\epsilon_r}}{c} \tag{A.6}$$

Both $I(t)$ and $Q(t)$ depend only on the transmitted frequency f_k, not on the time t, so in the following they will express as a function of f_k:

$$\begin{aligned} I(f_k) &= A cos(\Psi f_k) \\ Q(f_k) &= A sin(\Psi f_k) \end{aligned} \tag{A.7}$$

and

$$S(f_k) = I(f_k) + iQ(f_k) \tag{A.8}$$

Equations (A.7) and (A.8) say that in the frequency domain the downconverted signal is a complex tones whose periodicity is given by Ψ. Antitransforming $S(f_k)$ by meaning of IFFT is possible to extract the values of Ψ,then the range R. It can be proved that in presence of L targets at ranges $R_1, R_2, ...R_L$, the downconverted signal is the sum of L complex tones with periodicity: $\Psi_1, \Psi_2, ...\Psi_L$, with $\Psi_i = -4\pi R_i\sqrt{\epsilon_r}/c$. Then, by meaning of IFFT it is still possible to extract the range of each target.

Consider for a moment a discrete time system. The inverse of the sampling time t_S is proportional to the maximum frequency that can be observed without having aliasing, while the inverse of the product $N_S t_S$, where N_S is the number of observed samples, is proportional to the minimum frequency resolution that can be appreciate. Dually, in a SFR the inverse of the step frequency Δf is proportional to the maximum unambiguous range R_u, while the inverse of the product $B_{tot} = N\Delta f$, that is the total equivalent bandwidth of radar, is proportional to the range resolution Δ_R. More in detail:

$$R_u = \frac{c}{2\Delta f\sqrt{\varepsilon_r}} \tag{A.9}$$

$$\Delta_R = \frac{c}{2N\Delta f\sqrt{\varepsilon_r}} = \frac{c}{2B_{tot}\sqrt{\varepsilon_r}} \tag{A.10}$$

If a target range is larger than R_u, then all scatters falling outside the unambiguous range window will fold over and appear in the synthesized profile. If two or more target ranges are closer than Δ_R, then the target will not detect as distinct objects.

The dynamic range of the radar is limited by many factors as: receiver dynamic range, ADC dynamic range, IQ imbalance, etc... On a VCO design prospective, the dynamic range is limited by the phase noise of the VCO [47]. In presence of phase noise, the phase $\vartheta(t)$ of the base band signal at the output of the mixer is given by:

$$\vartheta(t) = \Psi f_k + \Phi_c(t) \tag{A.11}$$

where $\Phi_c(t)$ is the cumulative phase noise:

$$\Phi_c(t) = \Phi_N(t+\tau) - \Phi_N(t) \tag{A.12}$$

where $\Phi_N(t)$ is the instantaneous phase noise of the carrier at time t. Then the measured phase as the result of this will deviate from the ideal value, leading to a noisy background disturbance.

A.3 System requirements and architecture

System analysis consideration defined the following project parameters:

- $f_0 = 2.8$ GHz
- $\Delta f = 400$ MHz
- $B_{tot} = N\Delta f = 15.2$ GHz
- Phase noise at 1 MHz offset from the carrier: $\mathcal{L}(1\text{MHz}) < -105$ dBc/Hz

The frequencies that must be synthesized range from f_0 to $f_0 + B_{tot}$: from 2.8 to 18 GHz, that is more than 2 octaves. The idea to cover such a huge range of frequency is to synthesize with a single PLL the highest octave of the required tuning range, then to derive all the other frequencies dividing by 2 or 4 the PLL output. The block diagram of the frequency synthesizer is sketch in Fig. A.2. The PLL reference is 100 MHz, and it has been chosen by other system constraints related to the maximum allowable settling time of the PLL. The frequency divider that closes the PLL loop is made by two different dividers: a fix divide by four prescaler, and a programmable divide by N divider. Of course a single VCO that operates up to 18 GHz performing a phase noise of -105 dBc/Hz at 1 MHz offset from the carrier, cannot have a tuning range of an octave. Then we decided to split the tuning range in two sections, and cover each of them with a different VCO.

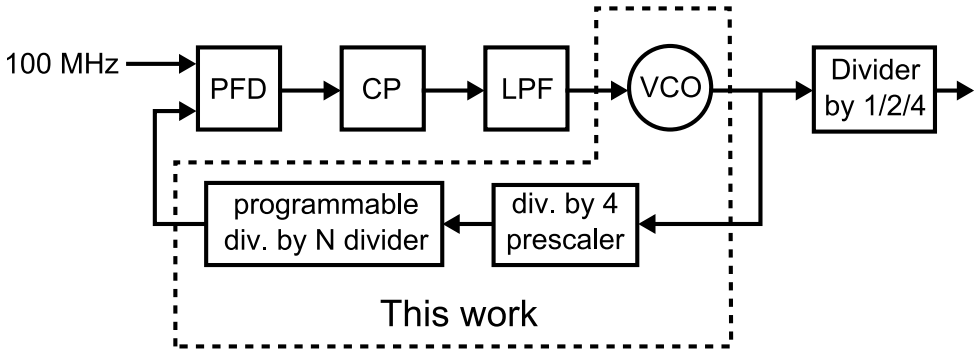


Figure A.2 Block diagram of the frequency synthesizer.

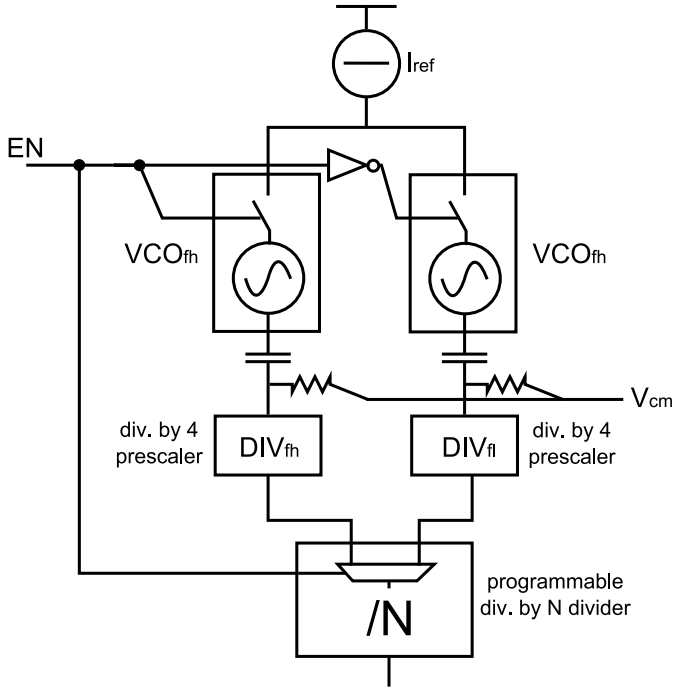


Figure A.3 Block diagram of the blocks presented in this work.

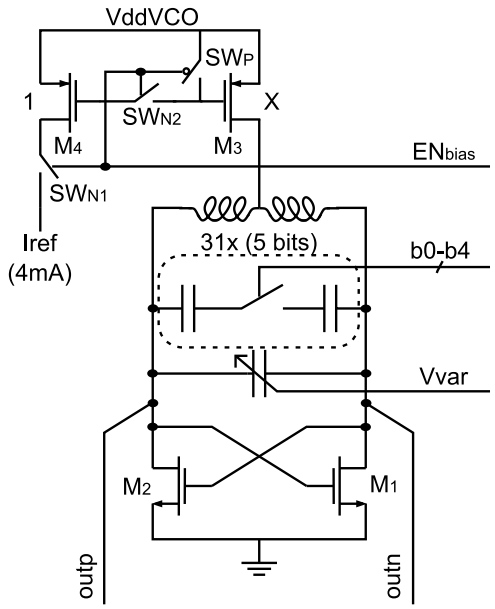


Figure A.4 Schematic of the VCOs.

Fig. A.3 shows more in detail the actual implementation of the blocks inside the dashed line of Fig. A.2. Each VCO is AC coupled to its own divide by four prescaler. This solution has been preferred to the one where both the VCOs share the same prescaler because it allows to place the prescalers the closer the possible to the VCO output, then to route a signal at a much lower frequency to the programmable divider. The signal EN controls which VCO to turn on. When EN is high the VCO_{fh}, that is the VCO that covers the higher part of the tuning range, is turned on and the VCO_{fl}, that he VCO that covers the lower part of the tuning range, is turned off. At the contrary when EN is low the VCO_{fh} is turned off, and the VCO_{fl} is turned on. Moreover EN controls which prescaler is multiplexed to the programmable divider input.

A.4 VCOs design

Both VCOs are based on the same topology shown in Fig. A.4, that is the same as the one presented in Chap. 5. The reference current I_{ref} is shared by both VCOs. In order to allow to turn on just one VCO at a time, control switches have been introduced in the bias network. When the EN_{bias} signal is high, both switches SW_{N1} and SW_{N2} are closed and the switch SW_P is opened. The reference current I_{ref} is correctly mirrored with a ratio $1 : X$ to the VCO's inductor central tap, and the VCO is turned on. The mirror

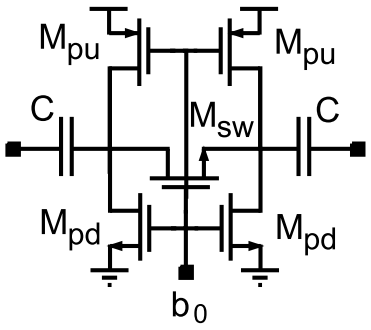


Figure A.5 Schematic unit cell capacitance of the capacitor bank.

ratio X values 3.5 for VCO_{fl}, and 5 for VCO_{fh}. At the contrary, when EN_{bias} is low, both switches SW_{N1} and SW_{N2} are opened while the switch SW_P is closed, forcing the transistor M_3 in the off state, and the VCO to be turned off. The size of the transistor M_1 and M_2 is $150/0.06\mu m$ for both VCOs.

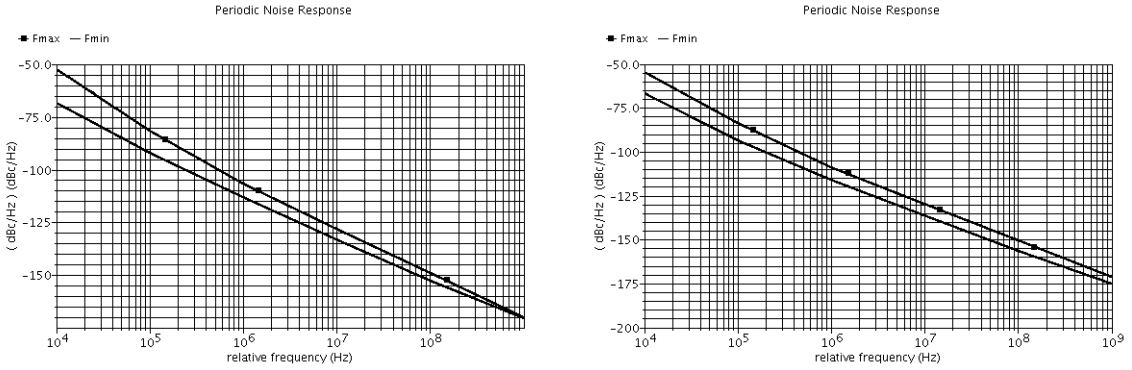
Both VCO inductors are single-turn inductors with octagonal shape. The coil for VCO_{fh} features 180 pH inductance, while the one for VCO_{fl} features 350 pH inductance. As for the GSM VCO's inductor, they were first designed using an EM simulator, then a lump model was derived, in order to perform time domain simulations. The model is the same as the one in Fig. 5.5, and it was fitted using the guidelines described in Sec. 1.2.

The tank capacitance is divided in a 5-bits capacitor bank plus a varactor to allow for continuous frequency tuning. The unit cell capacitance of the capacitor bank differs a little from the one of Fig. 5.6 for the presence of the pull-up pMOS transistors $M_{\rm pu}$, as shown in Fig. A.5. When the cell is in the off state, they force the dc voltage at the drain and at the source of $M_{\rm sw}$ to $V_{\rm dd}$. In this way the drain-bulk and source-bulk parasitic capacitances of $M_{\rm sw}$ are minimized and a larger C_{on}/C_{off} ratio of the unit cell can be achieved, ensuring a larger tuning range. Of course this is true only if the parasitic capacitance introduce by $M_{\rm pu}$ is small, and its output resistance is big enough to not affect the tank operation. For these reasons they were designed with minimum channel width, and longer then minimum length. A post layout simulation of the wiring of the capacitor bank was performed with an electromagnetic tool to take into account the extra parasitic inductance of the wiring. Moreover we checked that the varactor was large enough to cover the difference in parasitic inductance due to the different positions of the unit cells inside the capacitor bank layout, and ensure overlap between any two consecutive capacitor bank control words.

Post layout simulation of the tuning range as well as the values of the phase noise at 1 MHz offset from the carrier at the two edges of the tuning range are reported in

	F_{max}		F_{min}	
	Freq. [GHz]	P.N. @ 1MHz [dBc]	Freq. [GHz]	P.N. @ 1MHz [dBc]
VCO_{fl}	9.779	-115.8	14.64	-108.5
VCO_{fl}	13.86	-112.9	20.95	-106.9

Table A.1 VCOs tuning range and phase noise.



(a) (b)

Figure A.6 (a) Phase noise of VCO_{fh} at the two edges of its tuning range. (b) Phase noise of VCO_{fl} at the two edges of its tuning range.

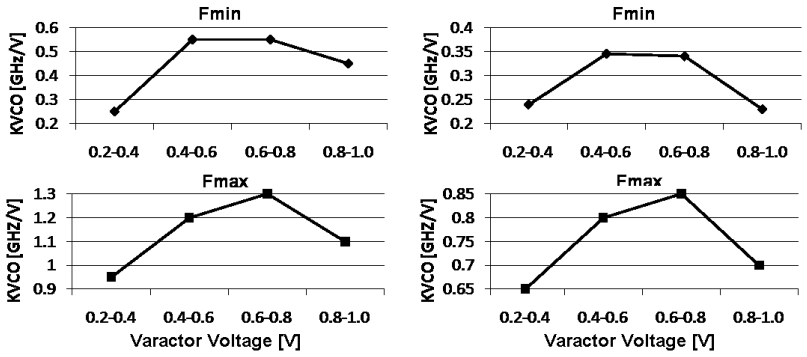
Tab. A.1 for both the VCOs. The completed plots of the phase noise at the two edges of the tuning range are shown in Fig. A.6(a) and Fig. A.6(b) for VCO_{fh}, and VCO_{fl} respectively. The highest edge of the tuning range is greater than 18 GHz in order to have margin with respect to the presence of extra parasitic capacitance not taken into account in the simulation and PVT variation. Fig. A.7(a) and Fig. A.7(b) shown the variation of K_{vco} within the varactor control voltage range (from 0.2V to 1V), due to the non linear C-V characteristic of the varactor.

A.5 Divider design

In a PLL, the input reference frequency and the output frequency are related by the division factor N of the divider in the feedback path of the PLL loop:

$$f_{out} = N f_{ref} \tag{A.13}$$

where f_{out} is the PLL output frequency, f_{ref} is the PLL reference frequency, and N is the division factor of the divider. Let consider only integer PLL (i.e. the division factor



(a) (b)

Figure A.7 (a) K_{VCO} of VCO_{fh} at the two edges of its tuning range. (b) K_{VCO} of VCO_{fl} at the two edges of its tuning range.

N is integer). The reference frequency f_{ref} defines which is the minimum frequency step at the PLL output. In our case the reference frequency is 100 MHz while the minimum step of frequency required at the PLL output is 400 MHz, that is four time f_{ref}. Then we preferred to realize the PLL divider as the series of two dividers: a fix divide by four prescaler and a programmable divide by N divider, as shown in Fig. A.2. In this case the relationship between output and reference frequencies is:

$$f_{ref} = \left(\frac{f_{out}}{4}\right)\frac{1}{N} \Rightarrow f_{out} = N\,(4f_{ref}) \tag{A.14}$$

From A.14 is clear that this solution allows a minimum frequency step of 400 MHz, introducing some practical advantages. In fact now the input frequency of the programmable divider is four times smaller than in absence of prescaler. This allows to realize the programmable divider using CMOS logic, and, if the prescaler is place close to the VCO, to route to the prescaler output, not the VCO output, with obvious advantages due the lower frequency of the former.

A.5.1 Prescaler

The prescaler is the same as the divider by four presented in Chap. 5, and shown in Fig.5.7. Two prescalers DIV_{fh} and DIV_{fl} were realized. The former is connected to VCO_{fh}, the latter to VCO_{fl}. The size of the injection transistor M_{inj} is the same for both prescalers and values 5/0.06 μm. At the contrary, the size of the transistors that make the ring core change between the two prescalers, in order to better centre the free

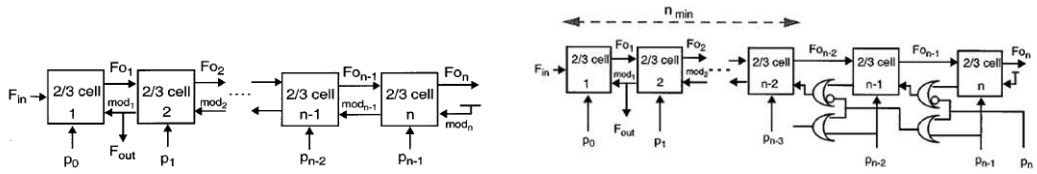


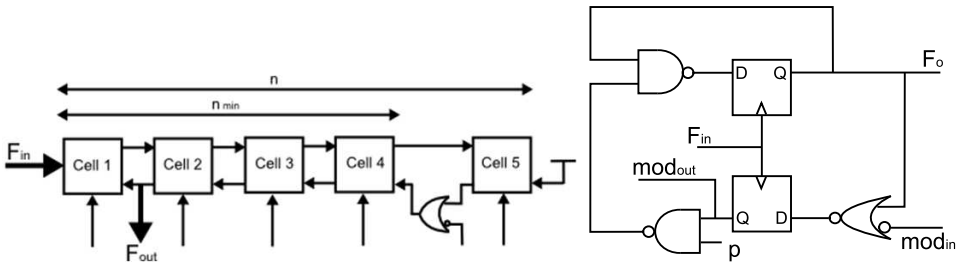
Figure A.8 Programmable prescaler. (a) Basic architecture. (b) With extended division range.

running frequency of the two ring oscillators with the two VCO tuning ranges. In any case the size of the nMOSs is equal to the size of the pMOSs and value 5/0.06 μm, and 5/0.08 μm for DIV_{fh} and DIV_{fl} respectively. Post layout simulations of the prescalers confirmed that they work properly over process and corner variation if the common mode voltage V_{cm} is in the range $700 - 800$ mV.

A.5.2 Programmable divider

The programmable divider is based on the dual modulus architecture of Fig. A.8(a) [48]. It consist of a modular structure based on a chain of 2/3 divider cells connected like a ripple counter. The programmable divider operates as follows. Once in a division period, the last cell on the chain generates the signal mod_{n-1}. This signal then propagates "up" the chain, being reclocked by each cell along the way. An active mod signal enables a cell to divide by 3 (once in a division cycle), provided that its programming input p is set to 1. Division by 3 adds one extra period of each cell's input signal to the period of the output signal.

It can be proved [48] that all integer division ratios ranging from 2^n (if all $p_n = 0$) to $2^{n+1} - 1$ (if all $p_n = 1$) can be realized. The division range is thus rather limited, amounting to roughly a factor two between maximum and minimum division ratios (an octave). This is not enough for our application since the sum of the two VCOs tuning ranges is more than one octave. [48] proposed a way to extend the tuning range based on the schematic of Fig. A.8(b). The idea is that deliberately setting the *mod* input of a certain 2/3 cell to the active level overrules the influence of all cells to the right of that cell. The divider chain behaves as if it has been shortened form n to n_{min} cells, where n_{min} is the number of divider cells that are effectively influencing the division cycle. Only a few extra OR gates are required to adapt n_{min} to the programmed division word, as depicted on the right side of Fig. A.8(b). With the additional logic the division ratio ranging from



(a) (b)

Figure A.9 (a) Schematic of the implemented prescaler. (b) Schematic of the 2/3 cell.

$2^{n_{min}}$ (if all $p_n = 0$) to $2^{n+1} - 1$ (if all $p_n = 1$). As a consequence the minimum and maximum division ratios can be set independently, by choice of n_{min} and n respectively. By choosing $n = 5$ and $n_{min} = 4$ the division factor N ranges between $N_{min} = 16$ and $N_{max} = 63$. That means that the divider can cover any VCO frequency in the range: $[4f_{ref}N_{min}$ - $4f_{ref}N_{max}] = [6.4$ GHz - 25.2 GHz], that is large enough to contain both the VCO tuning ranges.

The final schematic of the programmable divider is illustrate in Fig. A.9(a). A multiplexer was added at the input of the divider to choose among the two prescaler output, depending on which VCO is turned on. It was realized using CMOS static logic. The schematic of each 2/3 cell is shown in Fig. A.9(b). The D-FF was realized in TSPC CMOS logic while the logic gates outside the D-FF were realized in static CMOS logic. The schematic of the 2/3 cell is slightly different with respect to the one presented in [48], in order to realize the same logic without having complementary signals (e.g. Q and $\overline{Q}$). This is because in [48] they used CML logic to realize the 2/3 cell, then the complementary signal was for free. At the contrary we used CMOS logic, then we should add an inverter in the signal path to make the complementary signal, causing the cell to operate at lower frequencies. Post layout simulations confirmed the functionality of the programmable divider up to 6 GHz over process and corner variations, with a maximum power consumption of 0.63 mA.

At the moment I designed the programmable divider the choice of using a 100 MHz reference for the PLL was still under investigation. The other possible solution was to use a 25 MHz reference to obtain a step frequency Δf of 100 MHz, maintaining an integer PLL structure. Thanks to the modularity of the proposed divider solution it is very simple to adapt the divider to this new scenario. In fact it is enough to add two 2/3 unit cells at the right side of Cell 4, as illustrate in Fig. A.10 to obtain a new division chain whose

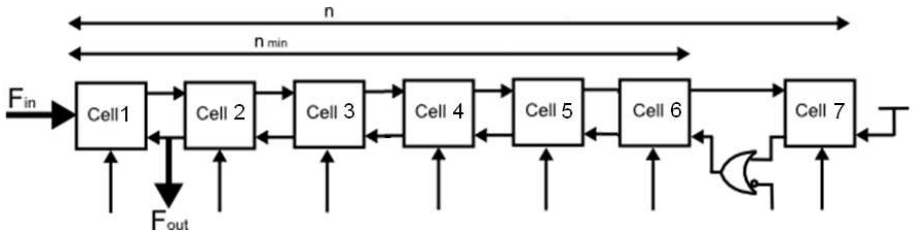


Figure A.10 Schematic of a possible prescaler in the case the reference signal is at 25 MHz.

parameter n and n_{min} values 7 and 6 respectively. As a consequence the new division factor N ranges between $N_{min} = 64$ and $N_{max} = 255$. With a 25 MHz reference it allows to cover a frequency range from 6.4 to 25.5 GHz at the PLL output, that is larger than the required for our applications. Moreover since the structure is characterized by the absence of long delay loops, as feedback lines are only present between adjacent cells, the maximum frequency of operation of each single cell decreases as one moves right the chain. Then, since we add new cells at the right end of the chain, while the frequency range at the input of the divider remains constant, the functionality of the new divider is still satisfy.

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