Università
degli Studi
di Padova

Sede Amministrativa: Università degli Studi di Padova

Dipartimento di Tecnica e Gestione dei Sistemi Industriali

Scuola di Dottorato di Ricerca in Ingegneria Meccatronica e dell'Innovazione Meccanica del Prodotto
Indirizzo: Meccatronica
Ciclo: XXXII

Advanced Controllers of Power Electronic Converters in DC Microgrids

Direttore della Scuola: Ch.mo Prof. Daria Battini
Coordinatore di Indirizzo: Ch.mo Prof. Daria Battini
Supervisore: Ch.mo Prof. Paolo Mattavelli

Dottorando: Guangyuan Liu

Contents

List of Acronyms

AC	Alternating Current
ADC	Anolog-to-Digital Converter
CAN	Controller Area Network
DAB	Dual Active Bridge
DAC	Digital-to-Anolog Converter
DC	Direct Current
DER	Distributed Energy Resource
DG	Distributed Generator
DPWM	Digital Pulse Width Modulation
DSP	Digital Signal Processor
ESS	Energy Storage System
EV	Electric Vehicle
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
IGBT	Insulated Gate Bipolar Transistor
LBC	Low-Bandwidth Communication

LED	Light Emitting Diode
MPPT	Maximum Power Point Tracking
PCC	Point of Common Coupling
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PR	Proportional-Resonant
PV	Photovoltaic
RHP	Right-Half-Plane
RMS	Root Mean Square
SFRA	Software Frequency Response Analyzer
SoC	State-of-Charge

List of Figures

List of Tables

Abstract

To cope with the pressure of climate change and depletion of fossil fuels, distributed power generation based on sustainable and green resources, such as photovoltaic and wind, have been exploited over the past decades. High penetration of renewable energy sources challenges the normal operation of traditional power grids, due to their characteristics of intermittence and uncertainty. To address this issue, an effective way is to aggregate distributed generators, energy storage systems, and customer loads together, as a single entity, that is, the so-called *microgrids*. Every microgrid is a fully dispatchable unit for grid operators, relieving the strains brought by renewable energy sources. Also, microgrids are able to provide reliable power for customer loads by supporting autonomous operation. Distributed energy resources are linked to microgrids by means of power electronic converters. As most of resources and future appliances are DC in nature, DC microgrids are more appealing than their AC counterparts. They can potentially achieve higher energy conversion efficiency and lower system costs, mainly by minimizing the number of DC-AC and AC-DC power conversion stages.

Droop control is a common decentralized solution to implement primary level control. With the droop control method, DC bus voltage is employed to convey the loading condition of DC microgrids, and load power can be automatically allocated among parallel resource converters. This dissertation focuses on performance improvement of droop-controlled converters, mainly in the following three aspects: *i)* reduction of DC bus capacitance while maintaining tight DC bus voltage regulation; *ii)* suppression of second-order harmonic current flowing into distributed energy resources; *iii)* smooth transfer from power flow control to droop control, allowing DC microgrids to seamlessly disconnect from upstream grids.

The first aspect: one of the constrains to reduce DC bus capacitance is the voltage surges and sags during load changes. From this point of view, resistive output impedance is a better design option than non-resistive output impedance for resource converters. This is because, given a certain output voltage tolerance band, resistive output impedance allows larger voltage dynamic variations, so that smaller output capacitance can be used. A systematical design approach, including the selection criteria of output capacitance and the design of droop coefficient, is proposed, covering both non-isolated (buck, boost, etc.) and isolated (dual active bridge) DC-DC converters. Following this design method, resistive output impedance can be effectively obtained. On the other hand, hysteresis control is another way to further reduce output capacitance, since it features faster dynamic response than classical PID control. Herein, hysteresis controller is implemented on digital signal processors instead of field programmable gate arrays. The implementation details, including the generation of driving signals for power switches and the effect of non-negligible computation time, are presented.

The second aspect: second-order harmonic power is an unavoidable issue in DC microgrids with single-phase inverters/rectifiers. Since droop-controlled converters usually show low output impedance at twice the line frequency, second-order harmonic power can flow into resource sides of converters. In some application like fuel cells, such harmonic current ripples can shorten device lifetime. To prevent the diffusion of second-order harmonic power, this dissertation studies the adoption of notch filter and resonant regulator in control loops. Although these two methods could mitigate second-order harmonic current, they deteriorate the stability performance of converters. In such a case, modified notch filter and modified resonant regulator are proposed to overcome the shortcoming of the traditional schemes. A comparative study is carried out to highlight the advantages of the proposed filter and regulator.

The third aspect: there are two limitations of the traditional droop control: one limitation is that the output power of droop-controlled converters is determined by load condition, and the other one is that the power sharing performance of droop control degrades with the presence of interconnecting cable impedance. To enhance the power flexibility and accuracy, a power-based droop controller, which unifies power flow control and droop control,

is proposed for resource converters. When grid-interfacing converters impose the DC bus voltage, resource converters could operate with power flow control. When grid-interfacing converters fail, resource converters could work with droop control to stabilize the system. Importantly, the switch from power flow control to droop control can be automatically accomplished without communication or detection schemes. The operation principle, the design criteria, and the power sharing performance of the proposed controller are analyzed comprehensively.

All of the above-mentioned proposals are verified by relevant experimental results performing on different laboratory-scale DC microgrid prototypes.

Acknowledgments

First of all, I wish to express my sincere gratitude to my supervisor Prof. Paolo Mattavelli. In the past three years, he is continuously giving me kind supports, not only for my research activities, but also for my life living in Italy. During our technical discussions, he shows adequate patience in guiding me through research challenges. His knowledge in power electronics and his enthusiasm for work inspire me to overcome obstacles in my study. More importantly, the way that he gets along with students deeply impresses me and motivates me to improve myself. It has been such a great pleasure for me to work with him and to learn from him.

I would like to thank the researcher and my dear friend Tommaso Caldognetto. He is always ready to answer my questions, to help me in simulations and experiments, and to introduce corrections for papers. Without his help, my Ph.D. study would have been much tougher, especially in its early stages. I am so grateful to him.

Special thanks go to my colleagues and dear friends, Aram Khodamoradi, Hossein Abedini, and Andrea Petucco. We had many cooperations in various research projects and their professional expertise has taught me a lot. Outside of university, I am truly touched by the warm help they provided for me and by their positive and active attitude towards life. I sincerely appreciate them for inviting me to many outdoor activities and parties, in which I enjoyed myself very much.

Special thanks go to my dear friends, Qing Liu, Weijian Han, Qi Xiao, Fei Deng, and Huiting Huang. Qing and Weijian have been my fellows since the start of my Ph.D. study and I could share many academic experiences, life confusions, and encouragement with them. Qi kept me company during his stay in University of Padova. The pleasant talks with him relieved my stress and anxiety to a large extent. Fei is my labmate in Vicenza and I have daily interesting lunchtime talks with him. Huiting has a broad knowledge and brings plenty of colorful topics into our chats. Thanks to these cute friends, my life living abroad is no longer lonely nor boring.

I wish to thank Prof. Paolo Magnone for his valuable comments and suggestions on my presentations and papers. I would like to thank Roberto Losco for his efforts in constructing experimental testbeds. My gratitude also goes to my labmates Fabio Tinazzi and Ludovico Ortombina for inviting me to events and for their kind help in university affairs.

In the end, I want to thank my father Zhouli Liu and my mother Yunxia Chen, for their unconditional love and for supporting me in studying abroad. I love you forever.

Guangyuan Liu
September 2019, Vicenza, Italy

Chapter 1

Introduction

Centering on micrigrids, this chapter gives a brief introduction for the background from three aspects: motivation for microgrids, microgrid architecture, and microgrid control. In the end, the challenges and objectives of this dissertation are outlined.

1.1 Motivation for microgrids

Energy is the foundation for the development of modern society. With the rapid growth of economy, the energy demand is continuously increasing. In 2018, the world consumed more than $160{,}000\,\mathrm{TWh}$ of primary energy [1]. The current energy system heavily relies on fossil fuels, including coal, oil, and natural gas. They account for 84.7% of the total energy consumption.

The use of such a huge amount of fossil fuels gives rise to two critical issues: energy crisis and climate change. From the perspective of energy crisis, fossil fuels are non-renewable resources and their reverses are limited. Fig. 1-1 shows the consumption of fossil fuels from 1965 to 2018 [1]. The consumption reaches $136{,}000\,\mathrm{TWh}$ in 2018 and grows by 2.4% compared to the data of 2017. Evidently, the depletion of fossil fuels is escalating. On the other hand, fossil fuels have considerable environmental effects. They are major contributors for global warming, since their combustion releases greenhouse-gases like carbon dioxide. For the decade from 2006 to 2015, the global mean surface temperature is $0.87°\mathrm{C}$ higher than the average over the 1850-1900 period [2]. Due to climate change, sea

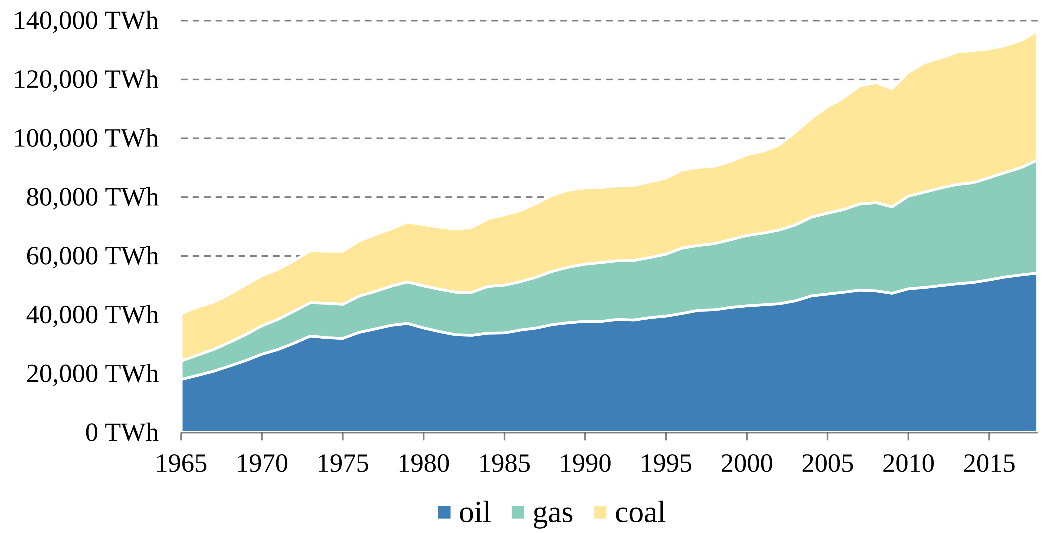


Figure 1-1: Consumption of fossil fuels from 1965 to 2018 [1].

levels continue to rise and extreme weather events become stronger and more intensive [3]. Driven by these two concerns, all countries endeavor to reduce the reliance on fossil fuels by exploiting renewable resources that are recognized to be sustainable and clean .

Propelled by government policies, Distributed Generators (DGs), such as photovoltaics (PVs) and wind turbines, have seen a vigorous development in recent years. Fig. 1-2 depicts the new annual installations of PVs and wind turbines all around the world [1]. Over the past decade, the average rate of new installation of wind turbine is $45\,\mathrm{GW}$ per year. Whereas, in the same period, photovoltaic shows an exponential growth, and its new installed capacity reaches $95\,\mathrm{GW}$ in 2018. The share of renewables (excluding hydroelectric) in electricity generation mix goes up from 8.4% in 2017 to 9.3% in 2018. Particularly, in Germany, renewable energy contributes to 32.2% of state's electricity production.

However, the development of traditional electrical power systems is not keeping pace with renewable energy. High penetration of DGs has significant influences the operation of power grids [4–8]. One of the challenges stems from the variability of renewable resources. The output power of PVs and wind turbines can face a sudden drop if cloud shadows pass across PV panels and wind speed slows down. This intermittence causes fluctuations in grid voltage and frequency especially with a high level of penetration, enforcing grid operators to provide more sophisticated grid regulation services. Moreover, the uncertainty of sunlight and wind makes it difficult to forecast power generation and further aggravates the

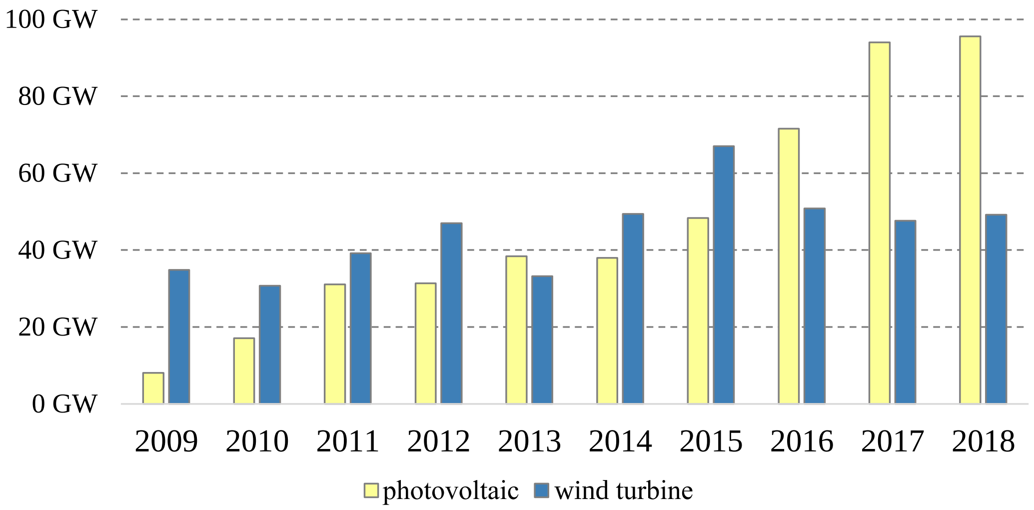


Figure 1-2: New annual installations of PV and wind turbine in the past decade [1].

situation. Another challenge is due to the fact that DGs deliver power to grids. When connected to existing distribution grids, DGs change the radial power flow of power systems and introduce reverse power flow. This behavior could eventually result in more complex power system protection.

Microgrids have been a promising solution to tackle the challenges posed by high penetration of DGs [9–11]. The components of microgrids include DGs, Energy Storage Systems (ESSs), and local customer loads. Also, microgrids are usually linked to upstreams grids (e.g., the utility). ESSs, such as lithium-ion batteries and super-capacitors, are utilized to smooth the output power of DGs [12, 13]. As bi-directional devices, ESSs can charge/discharge when the power generation of DGs is higher/lower than load demand. Thanks to the presence of ESSs, microgrids are able to function well either with upstream grids connected or disconnected [14, 15]. Microgrids bring benefits for both grid operators and customer loads [16, 17]. From grid's point of view, microgrids become fully-dispatchable units, alleviating the concerns for integrating DGs. From load's perspective, microgrids can provide more reliable electricity by supporting standalone operation, improve the power quality, and potentially reduce the energy cost.

Being an appealing network structure, microgrids have been receiving more and more attention, and there are many studies in this topic. In the following two sections of this chapter, the architectures and control of microgrids will be introduced.

1.2 Microgrid architectures

Microgrids comprise four main elements: DGs, ESSs, upstream grids, and customer loads. Within a microgrid, these four types of units are connected to common power bus(es) through power electronic converters. In general, according to the type of common bus(es), the microgrid architectures fall into three categories: AC, DC, and hybrid AC/DC microgrids.

1.2.1 AC microgrids

Nowadays, most of existing transmission and distribution power systems are designed for AC power, equipped with highly developed protection mechanism. Many commercial appliances and devices are manufactured with AC plugs, as well. In this context, AC microgrids are the commonly used configuration to take full advantage of the current infrastructure [11, 18–21].

Fig. 1-3 shows the typical layout of AC microgrid. For DGs and ESSs that based on DC power, such as PVs and Lithium-ion batteries, they are linked to AC bus by DC-AC converters. In some cases, these DC-AC converters employ two-stage topologies. The first stage is a DC-DC converter used to, for instance, boost the DC output voltage, and the second stage is a DC-AC inverter to complete the conversion from DC to AC power [22,23]. Even for DGs with AC output (e.g., wind turbines), direct connection from their output to AC bus is not feasible due to the difference of frequency, and AC-DC-AC interfacing converters are required. For AC loads like washing machines and refrigerators, they use DC power for motor drive, so additional AC-DC rectifiers are necessary. For Electric Vehicles (EVs), a typical adopted circuit for on-board charger is two-stage AC-DC-DC converters. The first stage can be a Power Factor Correction (PFC) converter to adjust the power factor to be as close to unity as possible, and the second stage can be an isolated DC-DC converter, for example, a LLC resonant converter which features high conversion efficiency in a wide operation range [24,25]. Through the description above, it is clear that two-stage converters are widely used for integrating various DGs, ESSs, and loads in AC microgrids. On the other hand, the connection with the utility is rather simple: only a breaker is needed at the

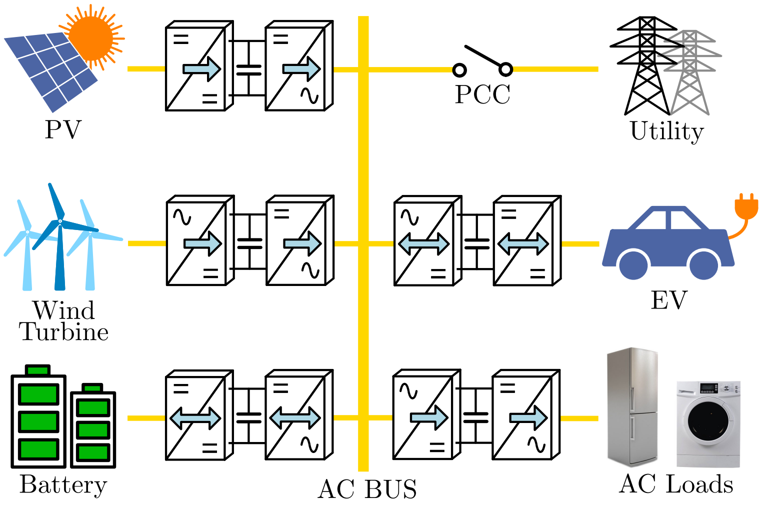


Figure 1-3: Typical layout of AC microgrid.

Point of Common Coupling (PCC).

Numerous pilot AC microgrids have been constructed all over the world in the past 20 years. Some examples are introduced as below:

- Kythnos island Microgrid, Greece, has been operating since 2001 to electrify 12 houses. This $400\,\mathrm{V}$ AC system has $11\,\mathrm{kW}$ PV arrays, $76.8\,\mathrm{kWh}$ lead-acid battery banks, and a $9\,\mathrm{kVA}$ back-up diesel generator [26].

- Miyako island microgrid, Japan, has been operating since 2010. The system is composed of $4\,\mathrm{MW}$ PV arrays, $4.2\,\mathrm{MW}$ wind turbines, $4\,\mathrm{MW}$ sodium-sulfur (NaS) batteries, and $100\,\mathrm{kW}$ lithium-ion batteries [27].

- Bronsbergen Holiday Park microgrid is the first microgrid in the Netherlands. Two battery banks and $315\,\mathrm{kW}$ PV arrays are connected to a $400\,\mathrm{V}$ AC bus [28].

1.2.2 DC microgrids

Many DGs (e.g., PVs, fuel cells), ESSs (e.g., lithium-ion batteries, super-capacitors), and today's loads (e.g., EVs) are dc in nature. Form this point of view, DC microgrids are more compatible than their AC counterparts [29–33]. Fig. 1-4 shows the typical layout of DC microgrids. Compared to the layout of AC microgrids shown in Fig. 1-3, a major distinction

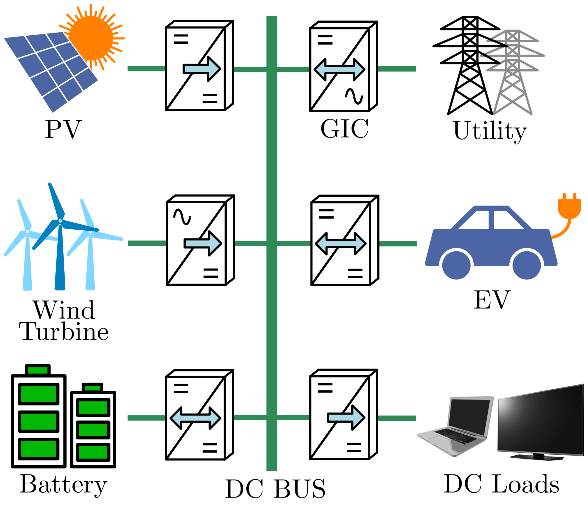


Figure 1-4: Typical layout of DC microgrid.

is the reduction of the number of DC-AC and AC-DC conversion stages. Thanks to this change, system investment and energy can be saved. However, an extra Grid-Interfacing Converter (GIC) is installed to tie DC microgrids with the upstream grid, which can be the utility or a higher level microgrid. The merits of DC microgrids are also reflected in the aspect of control. Issues like reactive power, frequency, harmonics, and synchronization are eliminated, resulting in much simpler control strategies.

The technology of DC microgrids has been applied to buildings and data centers. Some examples are reported as follows.

- ABB developed a $1\,\mathrm{MW}$ DC distribution system for a data center in Zurich-West, Switzerland, in 2012. Power is generated from a central AC-DC rectifier and is delivered to servers along a $\pm 200\,\mathrm{V}$ DC bus. Compared to the conventional AC architecture, this project is proven to save 10% of energy, 15% of investment, and 25% of space [34].

- In Xiang'an campus of Xiamen University, China, a $380\,\mathrm{V}$ DC microgrid based on a $150\,\mathrm{kW}$ rooftop PV system has been built up in 2014, supplying electricity to $30\,\mathrm{kW}$ air conditioners, $20\,\mathrm{kW}$ Light Emitting Diodes (LEDs), and $40\,\mathrm{kW}$ EV charging stations [35].

- In Lingshed village, India, 14 solar-based DC microgrids were established in 2015.

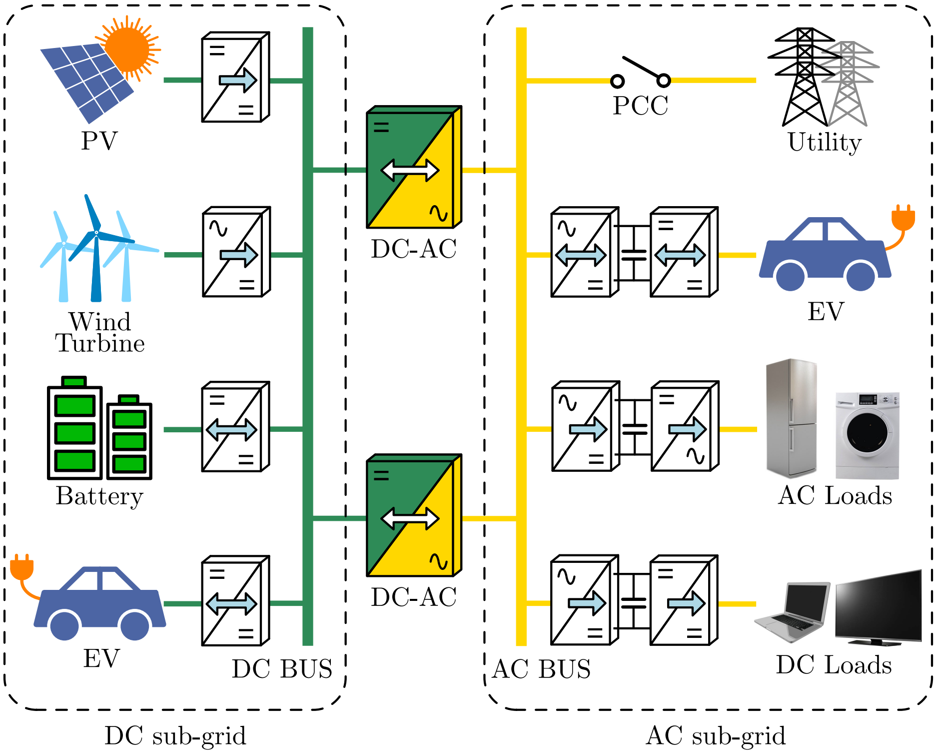


Figure 1-5: Typical layout of hybrid AC/DC microgrid.

Each microgrid comprises a 250 W PV panel, a pair of 12 V lead-acid batteries, and thirty 3 W LED lightbulbs. Thousands of (or even more) similar projects have been conducted in India to bring electricity to rural places [36].

1.2.3 Hybrid AC/DC microgrids

Hybrid AC/DC microgrids, which contain both DC sub-grids and AC sub-grids, are a compromise solution between AC microgrids and DC microgrids [37–41]. The typical layout of hybrid AC/DC microgrid is shown in Fig. 1-5. The utility and existing loads that are adapted to AC power can be connected to AC bus. Newly-built equipments can be connected to DC bus. AC bus and DC bus are interlinked by bi-directional DC-AC converters. The introduction of hybrid AC/DC microgrids facilitates the integration of DC technology with the present AC world, speeding up commercial applications of DC microgrids.

There are already some successful implementations of hybrid AC/DC microgrids, in fields of transportation and residence.

- Civil airplanes are stepping into the age of More Electric Aircrafts (MEAs). The electrical system of Boeing 787 is actually a hybrid AC/DC microgrid. A main $230\,\mathrm{V}$ AC distribution system conveys the power from six generators with a total capacity of $1450\,\mathrm{kVA}$ to three sub-systems, which are a $115\,\mathrm{V}$ AC system, a $\pm 270\,\mathrm{V}$ DC system, and a $28\,\mathrm{V}$ DC system. This configuration eliminates pneumatic bleed system, saves weight, and lowers maintenance costs [42].
- In Kaishan island, Jiangsu, Chian, a hybrid AC/DC microgrid has been set up to provide electricity for inhabitants. The system has a three-phase $380\,\mathrm{V}$ AC bus and a $750\,\mathrm{V}$ DC bus. $110\,\mathrm{kW}$ PV arrays, $30\,\mathrm{kW}$ wind turbines, and $660\,\mathrm{kW}$ batteries are connected to the DC bus. All customer loads and a $50\,\mathrm{kW}$ diesel engine are connected to the AC bus. The connection between the DC bus and the AC bus is accomplished by two centralized DC-AC converters [43].

In summary, DC microgrids, as well as DC sub-grids in hybrid AC/DC microgrids, are envisioned to play a vital role in future power distribution systems. Hence, they are selected as the research topic of this dissertation.

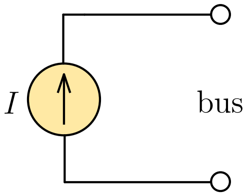
1.3 Microgrid control

Form the perspective of grid operators, GICs and interfacing power converters for DGs and ESSs are the foundation of DC microgrids. Proper control strategies are essential for the coordinated operation of these components. This section reviews the control for DC microgrids from microgrid level and from converter level. Microgrid-level control strategies aim at defining the role of each converter in microgrids, while converter-level control methods ensure that every converter acts as the predefined role.

1.3.1 Converter roles

Before going into the detail of DC microgrid control, it is necessary to firstly introduce the roles of converters in microgrids, that is, grid-forming converters, grid-following converters, and grid-supporting converters [18, 44].

(a) grid-forming converter (b) grid-supporting converter



(c) grid-following converter

Figure 1-6: Ideal representations of three types of converters in DC microgrids.

Grid-forming converters

Grid-forming converters are controlled as constant voltage sources, as shown in Fig. 1-6(a), so that they are able to maintain DC bus voltage at a certain level. They are responsible for power balance within microgrids, delivering power deficit to microgrids and absorbing power surplus from microgrids. Usually, one DC bus only allows the connection of one grid-forming converter. This is because grid-forming converters feature zero steady-state output (DC bus side) impedance. Hence, power sharing among parallel grid-forming converters is determined by parasitic parameters like sensing errors and cable resistance, which brings uncertainty for system operation.

Grid-supporting converters

A grid-supporting converter is basically a current-controlled or power-controlled voltage source. It can be ideally represented by a constant voltage source in series with a virtual output resistor, as shown in Fig. 1-6(b). Grid-supporting converters participate in DC bus voltage regulation. Due to the presence of virtual output resistors, DC bus voltage varies in a particular range instead of staying constant. Compared to grid-forming converters, grid-supporting converters can be safely connected in parallel, and power sharing depends on virtual output resistors.

Grid-following converters

Grid-following converters behave like current or power sources, as shown in Fig. 1-6(c), injecting power into microgrids without caring about DC bus voltage. Multiple grid-following converters can present in one DC microgrid. However, grid-following converters cannot work independently in a DC microgrid. At least one grid-forming or grid-supporting converter is needed to regulate the DC bus voltage.

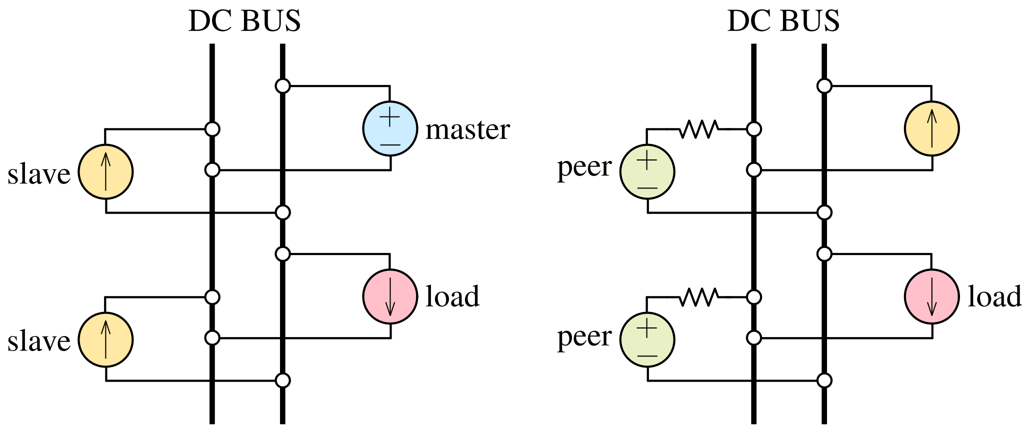
1.3.2 Microgrid-level control

Microgrid-level control defines the role of each converter in DC microgrids. There are two common control strategies, master-slave control and peer-to-peer control.

Master-slave control

Master-slave control for DC microgrids is the result of imitating the operation of grid-connected AC microgrids. For an AC microgrid tied with the utility, its AC bus voltage is dominated by the utility, and the other components in microgrid are only responsible for their own output power [45]. Similarly, for a DC microgrid in master-slave control mode, one converter acts as a master, that is, a grid-forming converter, to impose the DC bus voltage, and the other converters act as slaves, that is, grid-following converters [46, 47]. The concept of this control strategy is illustrated in Fig. 1-7(a).

The master converter maintains power balance within a DC microgrid. If power generation is higher than demand, the master converter absorbs the surplus power from the microgrid. If power generation is lower than demand, it injects power into the microgrid to compensate the power shortage. In this context, the master converter is expected to support bi-directional power flow and to have relatively larger capacity than other components in the microgrid. The GIC and ESS converters may fulfill the two requirements, and they can be considered as the candidate for the master converter. DG converters are usually configured as slave converters to operate with Maximum Power Point Tracking (MPPT)



(a) master-slave control (b) peer-to-peer control

Figure 1-7: Microgrid-level control strategies for DC microgrids.

algorithm [48], achieving a good harvest of energy.

This control strategy is simple and is easy to implement. Moreover, as slave converters operate with power flow control, accurate power sharing among them can be attained. However, the master-slave control suffers from a single point of failure. If a fault occured in the master converter, the DC bus voltage loses control and the entire DC microgrid collapses. In order to prevent this from happening, one of the slave converters should change to the master as soon as the original master converter fails. To this end, high-bandwidth communication or precise detection schemes must be adopted in DC microgrids, which complicates the design and decreases the system reliability.

The master-slave control is suitable for a small-scale DC microgrid, where a converter with dominant power capacity can be found. This control strategy has been tested in practical systems. For instance, in the DC sub-grid of Kaishan Island (see the second case in Section 1.2.3), one of the two battery converters is designated as the master converter to control the DC bus voltage.

Peer-to-peer control

In peer-to-peer control strategy, a part (or all) of converters are involved in microgrid power balancing and DC bus voltge regulation, with equal position [49, 50]. These converters can be configured as grid-supporting devices, while the other converters are configured as grid-following devices. There is not any grid-forming converter in this control mode. The concept of this control strategy is illustrated in Fig. 1-7(b).

Typically, stable resources like the GIC and ESS converters can be selected as grid-supporting converters. DG converters can choose to participate in voltage regulation or to stay in MPPT mode to maximize the generation of green energy.

The peer-to-peer control strategy features automatic power sharing among grid-supporting converters. By adjusting virtual output resistors of grid-supporting converters, proportional power sharing can be accomplished [51–53]. Furthermore, since the regulation of DC bus voltage relies on a couple of converters, the system reliability is significantly improved in comparison with the case with master-slave control. Nevertheless, the benefits are introduced at the expense of control flexibility, because the output power of grid-supporting converters is determined by load power not by their decisions. For example, ESS converters cannot freely decide to charge or discharge on the basis on the State-of-Charge (SoC).

According to the characteristics of peer-to-peer control, it is fit for a large-scale DC microgrid, where there is not any converter overwhelming the others in terms of power capacity.

1.3.3 Converter-level control

Taken the role assigned by microgrid-level control, one converter needs converter-level control to execute the tasks in a desired way. In order to manage these tasks, the hierarchical control structure is usually employed [37, 54–56].

The scheme of hierarchical converter-level control for DC mcirogrids is shown in Fig. 1-8. It includes primary, secondary, and tertiary control levels, corresponding to different control tasks.

- Primary control makes use of local information of converters [57]. It is responsible for local current, voltage, and power regulations, as well as other functions that only rely on local information. The time scale of primary control is at the level of microseconds and milliseconds.

- Secondary control has access to information of elements within DC microgrids

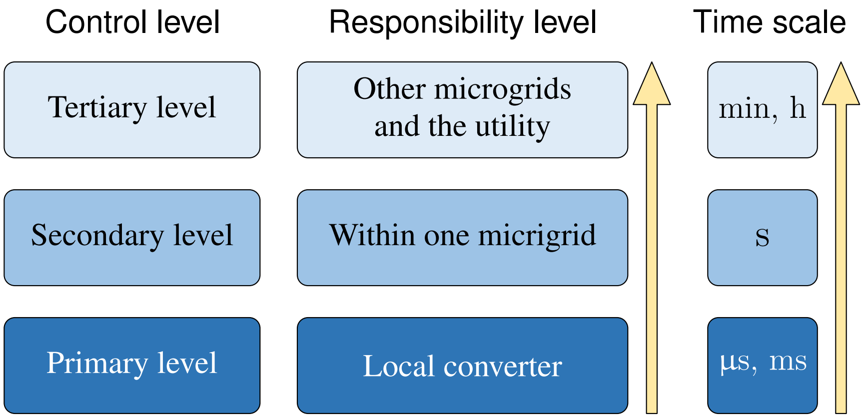


Figure 1-8: Hierarchical converter-level control for DC microgrids.

through communication link, so it could achieve global regulation targets, such as DC bus voltage restoration and load distribution enhancement [58–61]. Since communication with other devices takes time, the response time of secondary control is usually at the level of seconds.

- Tertiary control shares information with other microgrids and the utility [58, 62]. Its main objective is to guarantee the economic and optimal operation of DC microgrids by regulating the power exchange with other grids. The time scale of tertiary control is at the level of minutes and hours.

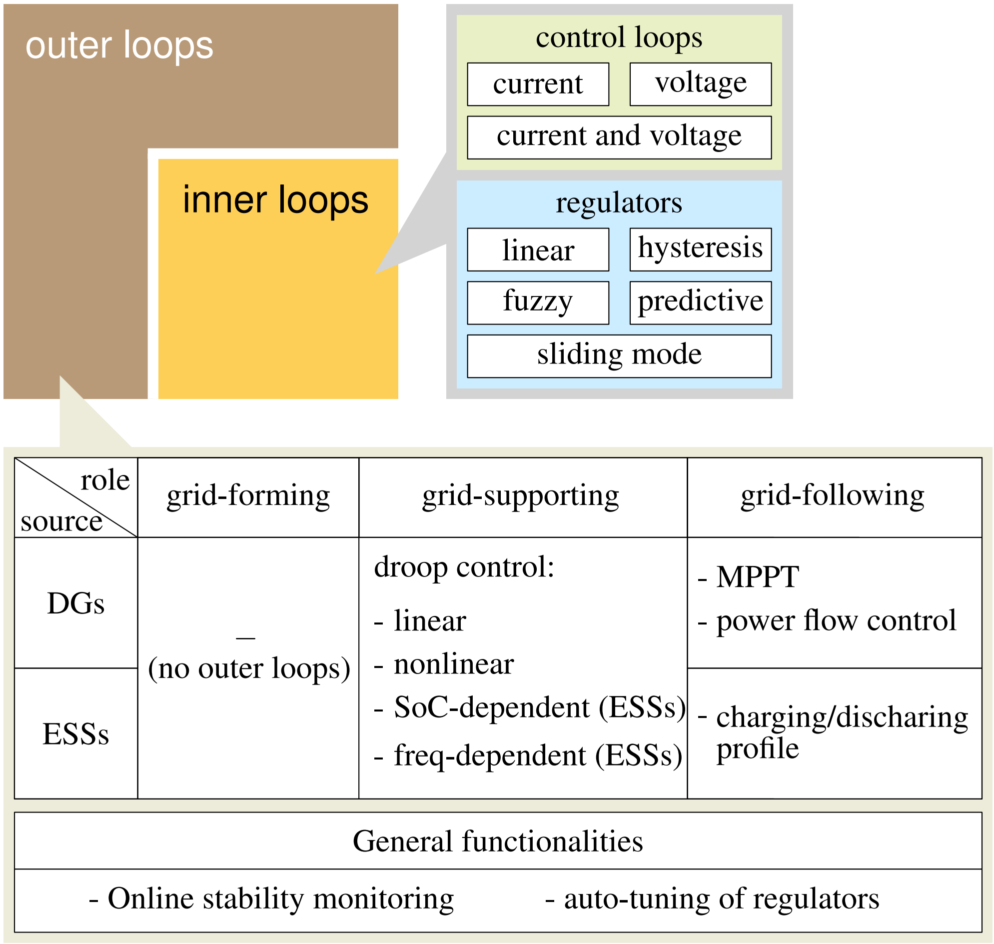
Primary control maintains mandatory functionalities of power converters, laying the foundation of this well-ordered hierarchical structure. Fig. 1-9 gives an overview of primary control techniques. As can be seen, primary control has inner control loop(s) to implement current/voltage regulations and outer control loop(s) to undertake other functionalities. The details of primary control for DC-DC converters are reviewed below.

Inner control loops of primary control

Inner control loops are the base of primary control. They have different configurations in terms of control loops and regulators.

Control loops

The common state variables used for feedback signals are the inductor current and the out-

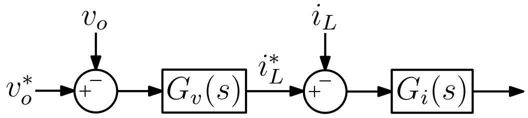


role / source	grid-forming	grid-supporting	grid-following
DGs	– (no outer loops)	droop control: - linear - nonlinear - SoC-dependent (ESSs) - freq-dependent (ESSs)	- MPPT - power flow control
ESSs			- charging/discharing profile

General functionalities	
- Online stability monitoring	- auto-tuning of regulators

Figure 1-9: Primary control techniques for DC-DC converters in DC microgrids.

(a) single current loop (b) single voltage loop



(c) cascaded voltage and current loops

Figure 1-10: Three typical forms of inner control loops.

put voltage. According to feedback signals, there are three typical control structures: single current loop, single voltage loop, and cascaded voltage and current loops, as presented in Fig. 1-10.

Single current loop takes the error between the current reference i_L^* and the current feedback i_L as the input of the current regulator $G_i(s)$ [63]. Depending on the operation principle of converter and the type of regulator, the output of $G_i(s)$ can be modulation signals like duty cycle, phase shift, and frequency, or it can also be gate driving signals for power switches. This structure is usually found in grid-following converters, which are controlled as current/power sources.

Single voltage loop calculates the error between the voltage reference v_o^* and the voltage feedback v_o and sends it into the voltage regulator $G_v(s)$ [64]. The output of $G_v(s)$ can either be modulation signals or gate driving signals. Single voltage loop is compatible with all types of converter circuits and regulators, and it is usually used in grid-forming and grid-supporting converters, which are assigned with the task of voltage regulation.

Cascaded voltage and current loops employs one voltage control loop to generate current reference i_L^* and one current control loop to produce modulation signals or gate driving signals [65]. It is usually adopted by grid-forming and grid-supporting converters. Compared to single voltage loop, the cascaded form can simply achieve current limitation. However, this cascaded structure cannot be applied with converters that do not possess dc inductor current, like Dual Active Bridge (DAB) converters. In addition, the voltage regulator $G_v(s)$ does not support regulators that directly produce gate driving signals, for example, hysteresis controllers.

Regulators

The current and voltage regulators used in inner control loops have different shapes. As listed in Fig. 1-9, there are linear control, hysteresis control, predictive control, fuzzy control, sliding mode control, and other control schemes. Among them, the most established ones, that is, linear control and hysteresis control, are introduced as follows.

Linear control is the most popular control technique and has been widely used in various control loops at different control levels. It features good control performances, robustness to perturbations, and easy implementation. Linear controllers include Proportional-Integral (PI) controller, Proportional-Integral-Derivative (PID) controller, Proportional-Resonant (PR) controller, etc.

In general, for a PI controller, the proportional gain K_p is used to tune the bandwidths of control loops, and the integrator K_i/s can achieve zero steady-state error. However, PI controller brings lagging phase for control loops. In order to increase the phase margin of control loops and to enhance system stability, a derivative term $K_d \cdot s$ can be added, resulting in a PID controller. It is able to provide up to $90°$ leading phase to control loops. A typical application of PID control is for a buck converter with single voltage loop, where PID control allows voltage loop bandwidth to be higher than the LC resonant frequency, which is not achievable with PI control.

With PI and PID control, only dc error signals converge to zero in steady state. In this case, PR control, as presented in (1.1), is used to regulate other frequency components to zero [66, 67]. The resonant term shows high magnitude peak at the center frequency ω_r. The width of the peak can be enlarged by increasing ω_b, improving the tolerance level to frequency variations.

$$G_{\mathrm{PR}}(s) = K_p + K_r \frac{2\omega_b s}{s^2 + 2\omega_b s + \omega_r^2} \tag{1.1}$$

Hysteresis control is also known as bang-bang control. The control target is to restrict an input signal within a hysteresis band [68]. The operation principle of conventional hysteresis control is illustrated in Fig. 1-11. When the input signal $in_1(t)$ hits the upper/lower

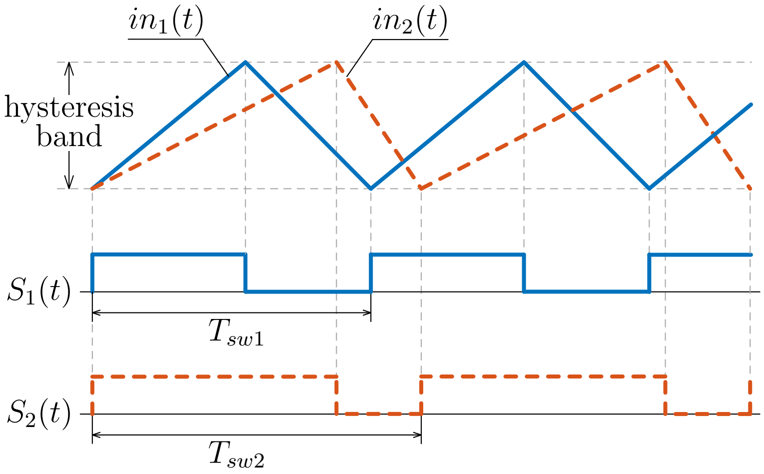


Figure 1-11: Operation principle of conventional hysteresis control. Switching frequency varies in different operation conditions.

bound, the switching signal $S_1(t)$ toggles its state, so that $in_1(t)$ would develop toward the opposite direction and stay inside the hysteresis band.

The main merit of hysteresis control is its extremely fast dynamic response. The switching state is immediately changed once the input signal goes out of the hysteresis band, with negligible time delay (true in analog implementations). Unfortunately, the major drawback of traditional hysteresis control is that the switching frequency is not fixed. For instance, $in_1(t)$ and $in_2(t)$ are input signals in different operation conditions, as shown in Fig. 1-11. Slew rates of them are different, leading to the variation of switching frequency. Besides, conventional hysteresis control requires relatively large switching ripples on the input signal, which makes it difficult to implement in voltage control loops.

To address these two issues, voltage-mode hysteresis control with frequency stabilization was proposed in [69, 70]. Its operation principle is shown in Fig. 1-12. Instead of acting on the voltage ripple, a ramp signal $R(t)$ is generated according to the switching state. By adjusting β_r, that is, the relative position between $R(t)$ and the input signal $in(t)$, duty cycle can be changed and $in(t)$ can be regulated to the reference value. Importantly, since the total height, which equals 2β, and slew rate of $R(t)$ are constant, the switching frequency is stabilized in steady states. It is worth mentioning that, while Ref [69] implements this controller in an architecture of mixed-signal, Ref [70] moves to a fully digital control plant.

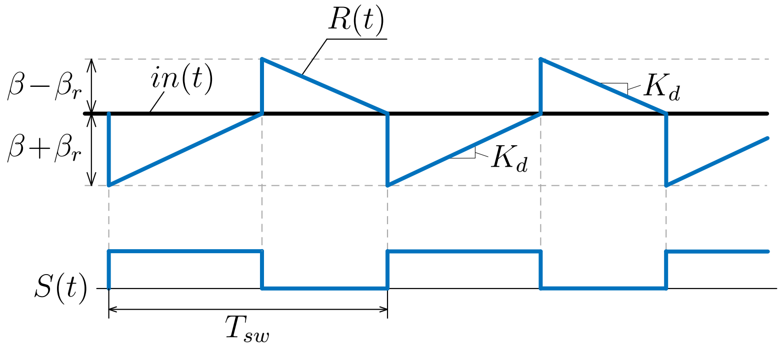


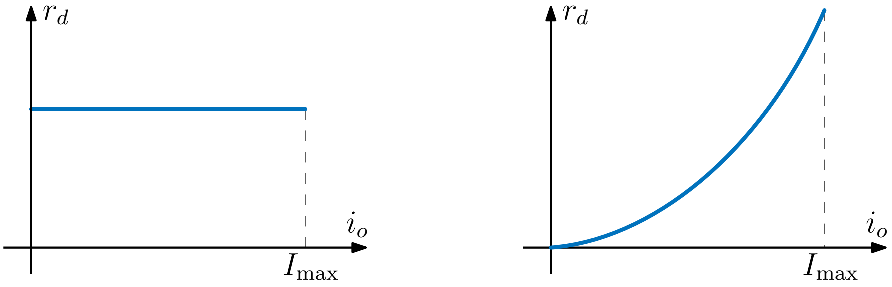
Figure 1-12: Voltage-mode hysteresis control.

Outer control loops of primary control

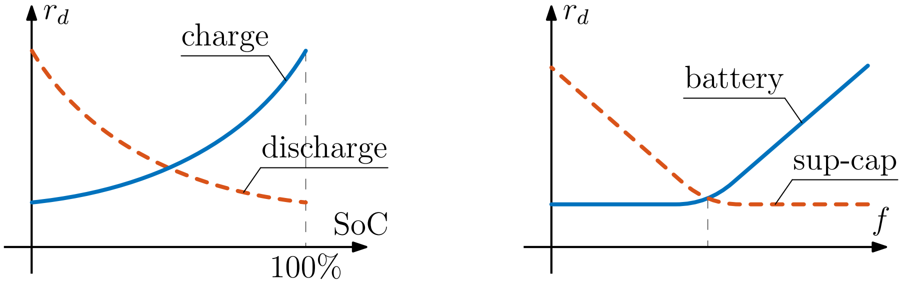
Outer control loops are installed on top of inner control loops, in order to accomplish various control missions. As reported in Fig. 1-9, potential control functionality include the general ones that can be applied to any converter, and the particular ones that depend on the role of converter and the type of source.

General control functionalities do not take into account of the converter role and the front-end source type. Online stability monitoring and adaptive tuning of regulators belong in this category. Online stability monitoring techniques cope with the varying microgrid environment by continuously identifying the stability performance of other control loops [71, 72]. Auto-tuning methods adjust regulator parameters online, for the purpose of maintaining desired dynamic performance [73–75].

Particular control functionalities consider the features of diverse converter roles and resources. Grid-forming converters are controlled as constant voltage sources, so that no outer control loops are required unless there is a need to change voltage references. As for grid-following converters, DGs can employ functionalities like MPPT [48] and constant power flow control, while ESSs can work on predefined charging/discharging profiles. Grid-supporting converters usually use droop control strategies to emulate virtual output resistor. Different design criteria are proposed for the virtual resistor: linear, nonlinear, SoC-dependent, frequency-dependent, etc. The last two shapes of droop coefficient are specifically for ESS applications. More discussions about droop control are presented as follows.



(a) linear droop (b) nonlinear droop



(c) SoC-dependent droop (d) frequency-dependent droop

Figure 1-13: Different shapes of the virtual resistor in droop control.

Droop control

Droop control is becoming a standard decentralized solution to underline the power sharing among parallel converters. Its operation principle is that the output voltage droops with the increase of the output current. This behavior is exactly like inserting a virtual resistor at the output port. As already stated in Section 1.3.2, ideally, power sharing among parallel droop-controlled converters is only determined by the ratio of their virtual output resistors.

Different virtual resistors have been reported in the literature: linear, nonlinear, SoC-dependent, and frequency-dependent, as shown in Fig. 1-13.

- Linear droop is the traditional design, in which the virtual resistor r_d is constant, as shown in Fig. 1-13(a), and the output voltage has a linear relationship with the output current. However, if the interconnecting cable impedance is comparable to r_d, the power sharing performance of linear droop deteriorates.

- Nonlinear droop is proposed to overcome the defect of linear droop [76, 77]. With nonlinear droop, r_d increases together with the output current, as shown in Fig. 1-

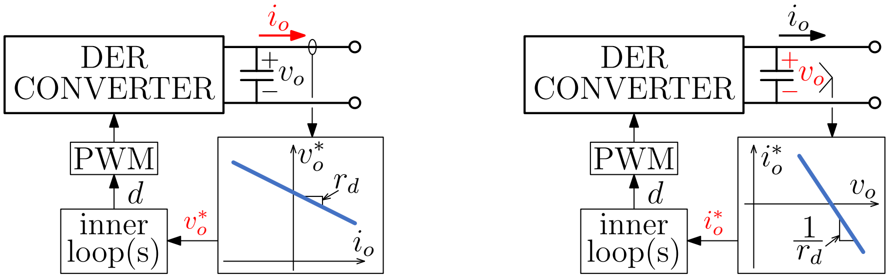
13(b). If the voltage drop at nominal current is maintained the same, r_d would be lower than the linear value at light load and be higher at heavy load. Consequently, the power sharing performance is enhanced at heavy load.

- SoC-dependent droop is proposed to balance SoC of multiple ESSs [56, 59]. As can be seen in Fig. 1-13(c), in charing mode, ESSs with higher SoC own larger r_d. On the contrary, in discharging mode, ESSs with higher SoC have smaller r_d. Therefore, ESS with higher SoC would deliver more power in discharging mode, and absorb less power in charging mode. After a couple of cycles of charging and discharging, SoC of multiple ESSs would be equal.

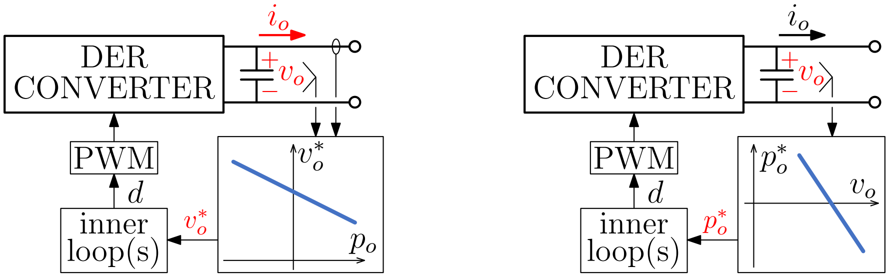
- Frequency-dependent aims to address the dynamic power distribution among ESSs with different features [78, 79]. For example, in a hybrid ESS configuration with super-capacitors and batteries, super-capacitors are expected to supply transient power demand and batteries only respond to static power demand. To this end, r_d for super-capacitors is designed to be high at low frequency and be low at high frequency, while r_d for batteries is designed to be low at low frequency and be high at high frequency, as depicted in Fig. 1-13(d).

Moreover, the implementation of droop control strategy can be categorized into four types, the voltage-current (*V-I*) droop, the current-voltage (*I-V*) droop, the voltage-power (*V-P*) droop, and the power-voltage (*P-V*) droop [80–82]. The control schemes of these four implementations are displayed in Fig. 1-14. The *V-I* and *I-V* droop methods work on the relationship between the output voltage and the output current, whereas the *V-P* and *P-V* droop methods work on the relationship between the output voltage and the output power. The *V-I* and *V-P* droop approaches generate the output voltage reference v_o^* based on the sampled output current i_o and the output power p_o, respectively. On the other hand, according to the measured output voltage v_o, the *I-V* and *P-V* droop methods calculate the output current reference i_o^* and the output power reference p_o^*, respectively.

According to the reference generated by droop control, different inner loops should be considered. For the *V-I* and *V-P* droop with v_o^*, single voltage loop and cascaded voltage and current loops can be the candidates. For the *I-V* droop with i_o^*, single output current



(a) *V-I* droop (b) *I-V* droop



(c) *V-P* droop (d) *P-V* droop

Figure 1-14: Different implementations of droop control.

loop, whose design methodology is not straightforward, should be adopted. Nevertheless, for converters with LC output filter, like buck converters, the single output current loop can be substituted by a single inductor current loop to ease the design, because the inductor current equals the output current in steady state. For the *P*-*V* droop with p_o^*, firstly i_o^* or v_o^* can be calculated based on the measured v_o or i_o, and then, corresponding inner loops can be selected.

1.4 Challenges and research objectives

In this chapter, microgrids are reviewed from different scenarios, including architecture and control, in order to build up a concise picture for readers. It is shown that primary control maintains the basic operation of converters in DC microgrids, so it is of paramount importance to have well-designed primary control to ensure stable operation of entire microgrids. This dissertation investigates several aspects about primary control for resource converters in DC microgrids, with a special focus on droop control.

1.4.1 Reduction of DC bus capacitance

Challenge: Having a certain amount of capacitors installed on DC bus in DC microgrids is a must to provide transient power and to stabilize the DC bus voltage. However, massive DC bus capacitance not only increases the investment, but also complicates fault protection. This is because, during short-circuit faults, the larger the DC bus capacitance, the higher the fault current. Therefore, the DC bus capacitance is expected to be as low as possible, under the condition that the DC bus voltage is maintained in the acceptable range during transient.

Objective: Improving the design of droop control for DC-DC resource converters, so that their output capacitance can be reduced while the output voltage is kept in the tolerance band during load changes.

1.4.2 Mitigation of second-order harmonic current

Challenge: Second-order harmonic power can be introduced into DC microgrids by either single-phase converters or three-phase converters with unbalanced three-phase voltages. As droop-controlled DC-DC converters usually show low output impedance at twice the line frequency, considerable second-order harmonic power would flow into DC-DC converters. This current ripple is generally not wanted, because it may decrease energy conversion efficiency and reduce the lifetime of front-end devices like fuel cells. Appropriate control actions must be taken to eliminate second-order harmonic current ripples.

Objective: Exploring the control approaches that can be simply integrated with droop controllers, for the sake of mitigating second-order harmonic current. Meanwhile, these control methods should not sacrifice other system performances like stability.

1.4.3 Seamless disconnection from upstream grids

Challenge: DC microgrids are usually connected to upstream grids to sell surplus power and to obtain power support. Microgrids may have master-slave control in grid-connected mode and peer-to-peer control in islanded mode, so as to combine the advantages of these two control strategies. In this context, when microgrids are disconnected from upstream grids, a part of converters need to change from grid-following converters to grid-supporting converters. Proper mode transition mechanism should be applied to those converters to guarantee stable operation.

Objective: Developing a unified controller for DC-DC resource converters in DC microgrids. This controller should operate with power flow control in grid-connected mode, and operate with droop control in islanded mode. Importantly, the mode transfer is expected to be done in an automatic way without any communication or islanding detection schemes.

1.5 Dissertation outline

In Chapter 2, a design method for general droop-controlled DC-DC converters in DC microgrids is introduced to reduce the output capacitance by shaping resistive output impedance. The design approach includes the selection criteria of output capacitance and the design of droop control parameters. Besides, hysteresis control is also exploited to extend the voltage loop bandwidth, so that the output capacitance can be further decreased.

In Chapter 3, a modified notch filter and a modified resonant regulator are presented. They can be easily inserted into existing droop controllers to prevent second-order harmonic current from flowing into DC-DC converters, without deteriorating the stability performances.

In Chapter 4, a power-based droop controller is proposed for DC-DC converters to enabling automatic transition from grid-following mode to grid-supporting mode. As a result, DC microgrids could achieve seamless disconnection from upstream grids.

In the end, Chapter 5 summarizes the main conclusions of the research work.

1.6 List of publications

Journal papers

J.1 **G. Liu**, T. Caldognetto, P. Mattavelli and P. Magnone, ”Power-Based Droop Control in DC Microgrids Enabling Seamless Disconnection From Upstream Grids,” in *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2039-2051, March 2019.

J.2 **G. Liu**, T. Caldognetto, P. Mattavelli and P. Magnone, ”Suppression of Second-Order Harmonic Current for Droop-Controlled Distributed Energy Resource Converters in DC Microgrids,” in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 1, pp. 358-368, Jan. 2020.

J.3 A. Khodamoradi, **G. Liu**, P. Mattavelli, T. Caldognetto and P. Magnone, ”Analysis of an Online Stability Monitoring Approach for DC Microgrid Power Converters,” in *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4794-4806, May 2019.

Conference papers

C.1 **G. Liu**, T. Caldognetto and P. Mattavelli, ”Power-based droop control in DC microgrids enabling seamless disconnection from AC grids,” *2017 IEEE Second International Conference on DC Microgrids (ICDCM)*, Nuremburg, 2017, pp. 523-528.

C.2 **G. Liu**, T. Caldognetto, P. Mattavelli and P. Magnone, ”Power sharing analysis of power-based droop control for DC microgrids considering cable impedances,” *2017 19th European Conference on Power Electronics and Applications (EPE’17 ECCE Europe)*, Warsaw, 2017, pp. P.1-P.10.

C.3 **G. Liu**, T. Caldognetto, P. Mattavelli and P. Magnone, ”Power-based droop control suppressing the effect of bus voltage harmonics for DC microgrids,” *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 4113-4120.

C.4 **G. Liu**, A. Khodamoradi, P. Mattavelli, T. Caldognetto and P. Magnone, ”Plug and Play DC-DC Converters for Smart DC Nanogrids with Advanced Control Ancillary Services,” *2018 IEEE 23rd International Workshop on Computer Aided Modeling and Design of Communication Links and Networks (CAMAD)*, Barcelona, 2018, pp. 1-6.

C.5 **G. Liu**, P. Mattavelli and S. Saggini, ”Design of Droop Controllers for Converters in DC Microgrids Towards Reducing Bus Capacitance,” *2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, Riga, 2018, pp. P.1-P.10.

C.6 **G. Liu**, P. Mattavelli, S. Pistollato and A. Petucco, ”Reduction of Output Capacitance for DAB DC-DC Converters in DC Microgrids by Shaping Resistive Output Impedance,” *2019 AEIT International Annual Conference (AEIT)*, Florence, 2019, to be published.

C.7 **G. Liu** and P. Mattavelli, ”Hysteresis Droop Controller with One Sample Delay for DC-DC Converters in DC Microgrids,” *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, 2019, to be published.

C.8 A. Khodamoradi, **G. Liu**, P. Mattavelli, T. Caldognetto and P. Magnone, ”On-line stability monitoring for power converters in DC microgrids,” *2017 IEEE Second International Conference on DC Microgrids (ICDCM)*, Nuremburg, 2017, pp. 302-308.

C.9 A. Khodamoradi, **G. Liu** and P. Mattavelli, ”Auto-Tuning of DC Microgrid Power Converters Based on a Constant Frequency Injection,” *2019 21th European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)*, Genova, 2019, to be published.

Chapter 2

Reduction of Output Capacitance by Shaping Resistive Output Impedance

In general, reduction of output capacitance for DER DC-DC converters in DC microgrids is expected, for the purpose of saving cost, decreasing system weight and size, and facilitating the short-circuit fault isolation. However, the decrease of output capacitance leads to the increase of output voltage spike/dip during load changes, and the output voltage may go out of the acceptable range during transient. From this point of view, resistive output impedance is a better design solution for DER converters than non-resistive solutions, because it allows a larger voltage spike/dip and thus enables the use of smaller output capacitance.

This chapter proposes a design methodology, which consists of the selection of output capacitance and the design of droop controller, for droop-controlled DC-DC converters, so that resistive output impedance can be achieved. This design approach is applied on not only non-isolated topologies like buck and boost converters, but also on isolated topologies like DAB converters.

This chapter also investigates the digital implementation of hysteresis control for the purpose of further reducing the output capacitance. As stated in Section 1.3.3, hysteresis control eliminating the modulation delay by removing the modulator. In addition, the hysteretic nature allows nonlinear switching actions during transient, speeding up the dynamic response. Consequently, compared to PID controllers, smaller output capacitance can be used without concerns of overvoltage and undervoltage. Hysteresis control is typically implemented on Field Programmable Gate Arrays (FPGAs). Differently, this work focuses on Digital Signal Processors (DSPs) implementation, as DSPs are more often used than FPGAs in commercial products, for example, PV inverters.

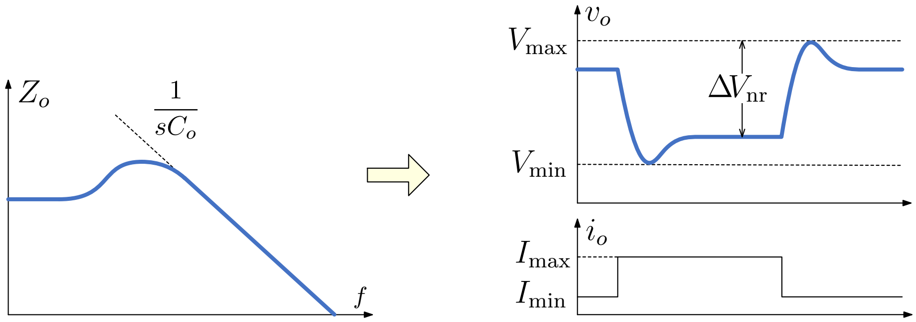
2.1 State-of-the-art

Droop control is a decentralized control strategy widely used in DC microgrids, allowing proportional power sharing among parallel DER converters without communication. Based on droop control, the static DC bus voltage varies in an allowable range according to load conditions, that is, the bus voltage stays at a high level with light load while it stays at a low level with heavy load. In order to supply a reliable bus voltage to customer loads, it is essential to attain tight DC bus voltage regulation when facing load variations.

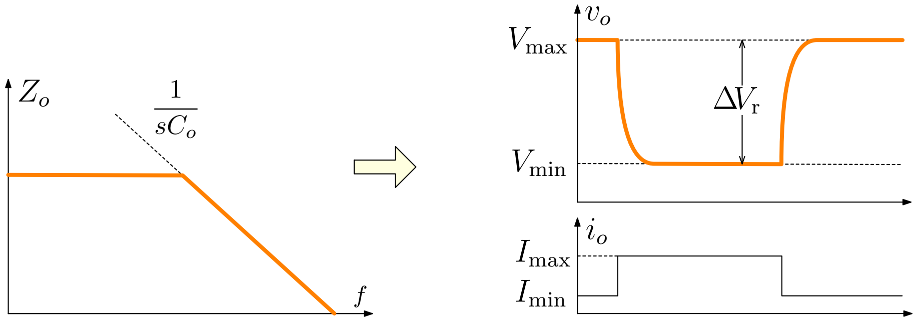
Given a certain voltage acceptable range, Fig. 2-1 displays different shapes of output impedance and corresponding dynamic output voltage waveforms during load changes. Fig. 2-1(a) shows the case of non-resistive output impedance. As can be seen, the allowable voltage spike/dip ΔV_{nr} makes use of part of the tolerance range. On the other hand, if the output impedance is designed to be resistive, as depicted in Fig. 2-1(b), the output voltage spike/dip ΔV_{r} takes advantage of the full tolerance band. Apparently, since ΔV_{r} is larger than ΔV_{nr}, resistive output impedance is the optimal design from the point of output capacitance reduction.

2.1.1 Output impedance shaping

To suppress the magnitude of output impedance, a straightforward solution is to choose relatively bulky output capacitors for DER converters [83]. By doing so, the DC bus voltage is so stiff that the bus voltage sags and surges during load changes are small enough or even negligible. Obviously, large output capacitance increases the system weight and size, which is critical in applications like aircrafts and ships [84]. Also, massive output capacitance means a great amount of energy stored on the bus. In case of a DC bus short-circuit fault, a high fault current can be generated, which makes fault isolation difficult [85,86]. Therefore,



(a) non-resistive output impedance



(b) resistive output impedance

Figure 2-1: Different output impedance of droop-controlled DER converters and corresponding dynamic output voltage waveforms during load changes.

it is necessary to reduce the output capacitance of DER converters.

Besides of hardware modifications, resistive output impedance can be also shaped by means of control solutions. In [87] and [88], an additional output voltage feedback path is added for the voltage control loop according to Mason's gain formula, so that the output impedance can be effectively shaped while preserving the voltage loop bandwidth. Moreover, voltage regulator modules, which are power supplies for microprocessors and are mainly buck converters, are designed to have almost constant output impedance by means of tuning the parameters of voltage regulators [89–91]. In addition, the so-called virtual-capacitor control, which is also named as integral droop control or virtual inertia control, is capable of providing virtual output capacitance for converters, thus diminishing the peak of output impedance [78, 79, 92–96]. The virtual-capacitor control is basically realized by an output current feedback path through an integral gain. The functions of this approach include mitigating the harmonics in output currents/voltages of inverters [93, 94], enhancing the system damping and stability [95], and smoothing the output power flow of devices like batteries [78, 79, 96]. Combing the concept of virtual-capacitor control, an admittance-type droop controller is proposed in [97], achieving resistive-capacitive output impedance. However, this controller is developed for specific converters with LC output filters (like buck converters). Also, the design of virtual capacitance and the selection criterion for the physical output capacitance are still missing.

2.1.2 Hysteresis control

DC bus voltage spikes or dips in case of load changes is related to the dynamic response speed of the voltage control loop. Since the voltage control loop enforces the output voltage to track its reference value, so a faster response of the voltage loop ensures a smaller voltage deviation. Hence, for a given voltage tolerance band, pushing the voltage control bandwidth facilitates the reduction of the output capacitance. However, with typical single-sampled PID controllers, the control bandwidth is limited by the control delay introduced by the computation time and the Digital Pulse Width Modulation (DPWM) modulator [68]. For example, considering a computation time of one switching period and the triangular carrier-based PWM, the control loop would have a total time delay of one and a half of the switching cycle, which causes about $-54°$ phase lag at $1/10$ of the switching frequency.

To reduce the time delay in control loops, a possible way is to adopt the oversampling technique, in which, the signals are acquired for multiple times in one switching period [68, 98, 99]. By doing so, the computation time and the modulation delay can be significantly lowered to a fraction of the original value. The oversampling technique are applied to different types of control solutions, including, but not restricted to, oversampled PID control, hysteresis control [70], sliding mode control [100], and finite-control-set model predictive control [101]. The oversampled PID control is directly developed from the single-sampled one, and it features easy design and application. On the other hand, the other three control methods are nonlinear solutions that are expected to advance the linear PID controller in aspects like dynamic response. This is partially because that they operate without modulators, thus, totally eliminating the modulation delay. In this chapter, hysteresis control, whose basics are introduced in Section 1.3.3, is considered and applied to droop-controlled DER converters.

Hysteresis control is usually implemented on FPGAs to guarantee an acceptable computation time, since analog-to-digital conversions of sampled signals and relevant data post-processing must be completed within sampling intervals. Nowadays, DSPs are becoming more and more powerful, showing potential capability to handle the time-critical calculation tasks. DSPs are highly integrated with various peripherals and are, in general, cheaper than FPGAs. Nevertheless, the use of DSP inevitably introduces additional computation time and increases the control delay.

2.2 Selection of output capacitance

This section provides an initial estimation value for the output capacitance to achieve resistive output impedance, by investigating the effect of the output capacitance on the output impedance.

In order to choose a reasonable output capacitance, the simplified shape of output impedance $Z_{oc}(s)$ is studied. Fig. 2-2(a) presents the diagram of $Z_{oc}(s)$ with inadequate output capacitance. The structure of $Z_{oc}(s)$ can be roughly divided into three parts. Well below the output voltage control bandwidth f_v, $Z_{oc}(s)$ can be shaped to be droop resistance r_d by means of control methods [102]. When the frequency approaches the control bandwidth, $Z_{oc}(s)$ becomes closer to the open-loop output impedance, and its magnitude rises gradually until dominated by $1/sC_o$ at high frequency. As can be observed, $Z_{oc}(s)$ is lower than r_d again when the frequency is over f_{int}, which is the intersection frequency of $1/sC_o$ and r_d:

$$f_{\text{int}} = 1/(2\pi \cdot C_o \cdot r_d) \tag{2.1}$$

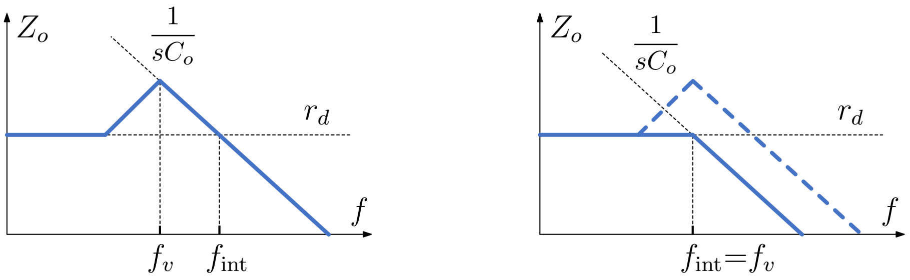
To have resistive-capacitive output impedance, the output capacitance should be selected in such a way that f_{int} matches f_v, as illustrated in Fig. 2-2(b). Thus, the value of the output capacitance C_o can be expressed as:

$$C_o = 1/(2\pi \cdot r_d \cdot f_v) \tag{2.2}$$

This equation is easy to understand. For a converter with a certain power capacity, a smaller r_d means a narrower voltage tolerance band, which, in turn, requires larger C_o or faster control response (i.e., higher f_v). In practical design, the voltage control bandwidth f_v can be firstly estimated according to system parameters such as the switching frequency and the control delay. Afterwards, the output capacitance C_o can be calculated by (2.2). It should be noticed that the output capacitance is obtained based on the simplified output impedance and is not highly accurate, so it can be adjusted accordingly in the following design procedures. Nevertheless, it could still facilitate the design process.

2.3 Case of non-isolated DC-DC converters

This section firstly derives the small-signal model of a generalized droop-controlled non-isolated DC-DC converter to obtain the output impedance. Secondly, the design method for droop controllers is introduced to attain resistive-capacitive output impedance. Then, the simplified version of this design method is presented, so that it is independent of converter topologies. Finally, the proposed design method is validated by experimental results



(a) inadequate C_o (b) optimal C_o

Figure 2-2: Simplified diagram of the output impedance of droop-controlled converters to select proper output capacitance.

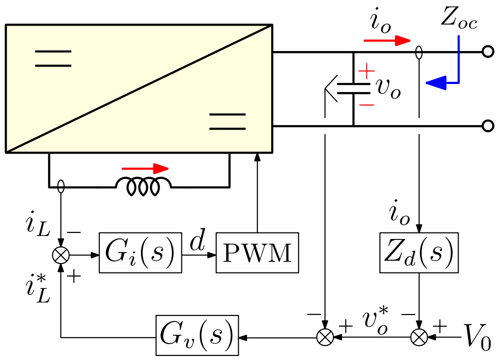


Figure 2-3: The control scheme of a generalized droop-controlled non-isolated DC-DC converter.

referring to a buck-based and a boost-based DC microgrid prototype.

2.3.1 Derivation of small-signal model

The control scheme of a generalized droop-controlled non-isolated DC-DC converter is shown in Fig. 2-3. The droop controller consists of cascaded voltage and current inner loops, and a droop loop. $G_i(s)$ is the current regulator and $G_v(s)$ is the voltage regulator. The implementation of droop control can be categorized into four types, as described in Section 1.3.3, *V-I* droop, *I-V* droop, *V-P* droop, and *P-V* droop. Herein, the design methodology the *V-I* droop approach is analyzed. The droop function is expressed as:

$$v_o^* = V_0 - i_o \cdot Z_d(s) \tag{2.3}$$

where v_o^* is the output voltage reference, V_0 is the output voltage set point under no load condition, i_o is the output current, and $Z_d(s)$ is the generalized droop impedance.

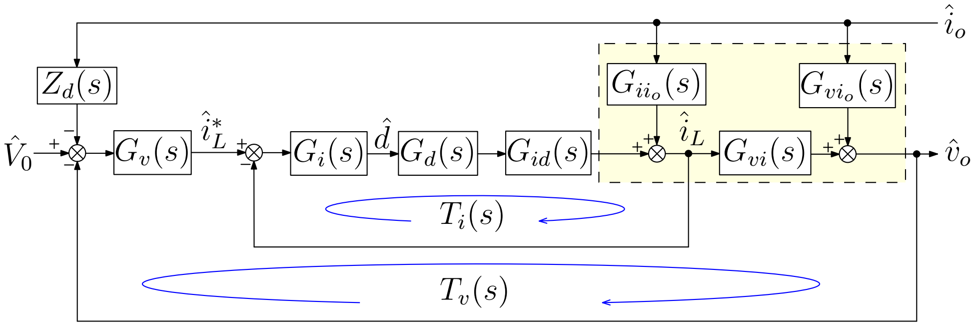


Figure 2-4: The linearized model of the converter shown in Fig. 2-3.

The small-signal model of the droop-controlled converter is derived. Under an operation condition, the power stage of this converter can be linearized as:

$$\hat{i}_L = G_{id}(s) \cdot \hat{d} + G_{ii_o}(s) \cdot \hat{i}_o \tag{2.4}$$

$$\hat{v}_o = G_{vd}(s) \cdot \hat{d} - Z_{oo}(s) \cdot \hat{i}_o \tag{2.5}$$

where the diacritic mark ˆ indicates the AC small-signal, $G_{id}(s)$ is the transfer function from $\hat{d}$ to $\hat{i}_L$, $G_{ii_o}(s)$ is the transfer function from $\hat{i}_o$ to $\hat{i}_L$, $G_{vd}(s)$ is the transfer function from $\hat{d}$ to $\hat{v}_o$, $Z_{oo}(s)$ is the open-loop output impedance, and $G_d(s)$ is the control delay caused by computation and DPWM. By combining equation (2.4) and (2.5) and canceling the variable $\hat{d}$, following equation is obtained:

$$\hat{v}_o = \frac{G_{vd}(s)}{G_{id}(s)} \cdot \hat{i}_L + \left[-Z_{oo}(s) - \frac{G_{vd}(s) G_{ii_o}(s)}{G_{id}(s)} \right] \cdot \hat{i}_o = G_{vi}(s) \cdot \hat{i}_L + G_{vi_o}(s) \cdot \hat{i}_o \tag{2.6}$$

Finally, the power stage can be represented by (2.4) and (2.6). The resulted linearized control block diagram of the droop-controlled converter is displayed in Fig. 2-4.

For the current loop, its open-loop transfer function $T_i(s)$ and its closed-loop transfer function $T_{iCL}(s)$ are given as:

$$T_i(s) = G_i(s) \cdot G_d(s) \cdot G_{id}(s) \tag{2.7}$$

$$T_{iCL}(s) = T_i(s)/[1 + T_i(s)] \tag{2.8}$$

For the voltage loop, its open-loop transfer function $T_v(s)$ and its closed-loop transfer function $T_{vCL}(s)$ are given as:

$$T_v(s) = G_v(s) \cdot T_{iCL}(s) \cdot G_{vi}(s) \tag{2.9}$$

$$T_{vCL}(s) = T_v(s)/[1 + T_v(s)] \tag{2.10}$$

With the current loop, the voltage loop, and the droop loop closed, the output impedance $Z_{oc}(s)$ can be deduced as:

$$Z_{oc}(s) = -\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{V}_0=0} = \frac{Z_d(s)T_v(s) - G_{ii_o}(s)G_{vi}(s)/[1+T_i(s)] - G_{vi_o}(s)}{1 + T_v(s)} \tag{2.11}$$

Since the open-loop output impedance $Z_{oo}(s)$ can be expressed as:

$$Z_{oo}(s) = -\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{d}=0} = -G_{vi_o}(s) - G_{ii_o}(s)G_{vi}(s) \tag{2.12}$$

(2.11) can be rewritten as:

$$\begin{aligned} Z_{oc}(s) &= Z_d(s)T_{vCL}(s) + \frac{Z_{oo}(s) + G_{ii_o}(s)G_{vi}(s)T_{iCL}(s)}{1 + T_v(s)} \\ &= Z_{oo}(s)[1 - T_{vCL}(s)] + [Z_d(s) + G_{ii_o}(s)/G_v(s)]\, T_{vCL}(s) \end{aligned} \tag{2.13}$$

2.3.2 Resistive output impedance shaping

The design method to achieve resistive output impedance is straightforward. The output impedance $Z_{oc}(s)$ can be regarded as a function of $Z_d(s)$. By solving the equation that $Z_{oc}(s) = r_d$ (r_d is the droop resistance), $Z_d(s)$ can be deduced. According to (2.13), the droop impedance $Z_d(s)$ should be designed as:

$$Z_d(s) = r_d/T_{vCL}(s) - Z_{oo}(s)/T_v(s) - G_{ii_o}(s)/G_v(s) \tag{2.14}$$

Within the voltage control bandwidth ω_v (i.e., $\omega < \omega_v$), $T_{vCL}(j\omega)$ and $T_{iCL}(j\omega)$ can be approximately considered as unit gains. Hence, combining (2.9) and (2.12), (2.14) can be simplified as:

$$\begin{aligned}Z_d(j\omega) &\approx r_d + \frac{G_{vi_o}(j\omega)+G_{ii_o}(j\omega)G_{vi}(j\omega)}{G_v(j\omega)G_{vi}(j\omega)} - \frac{G_{ii_o}(j\omega)}{G_v(j\omega)} \\ &= r_d + \frac{G_{vi_o}(j\omega)}{G_v(j\omega)G_{vi}(j\omega)}, \quad \omega < \omega_v\end{aligned} \tag{2.15}$$

It can be found that $Z_d(s)$ is related not only to r_d, but also to $G_{vi_o}(s)$, $G_{vi}(s)$ and $G_v(s)$. It suggests that $Z_d(s)$ depends on the topology of DER converters because of the presence of $G_{vi_o}(s)$ and $G_{vi}(s)$.

To numerically verify the feasibility of the proposed design method, two representative examples of DC-DC converters are studied herein: a buck-type converter and a boost-type converter. It should be noted that this design method is generic and it can be also applied to other converters like buck-boost, Cuk, Sepic, and Zeta.

Buck-type converter

The control scheme of a buck-type droop-controlled DER converter is shown in Fig. 2-5. Under an operation point, the linearized equations of the buck converter are given as:

$$sL \cdot \hat{i}_L = V_{in} \cdot \hat{d} - \hat{v}_o \tag{2.16}$$

$$sC_o \cdot \hat{v}_o = \hat{i}_L - \hat{i}_o \tag{2.17}$$

Then, by combining (2.16) and (2.17), the state variables $\hat{i}_L$ and $\hat{v}_o$ can be expressed as:

$$\hat{i}_L = \underbrace{\frac{sC_oV_{in}}{s^2LC_o+1}}_{G_{id}(s)} \cdot \hat{d} + \underbrace{\frac{1}{s^2LC_o+1}}_{G_{ii_o}(s)} \cdot \hat{i}_o \tag{2.18}$$

$$\hat{v}_o = \underbrace{\frac{1}{sC_o}}_{G_{vi}(s)} \cdot \hat{i}_L + \underbrace{\left(-\frac{1}{sC_o}\right)}_{G_{vi_o}(s)} \cdot \hat{i}_o \tag{2.19}$$

The entire block diagram of the linearized droop-controlled buck converter is displayed in Fig. 2-4.

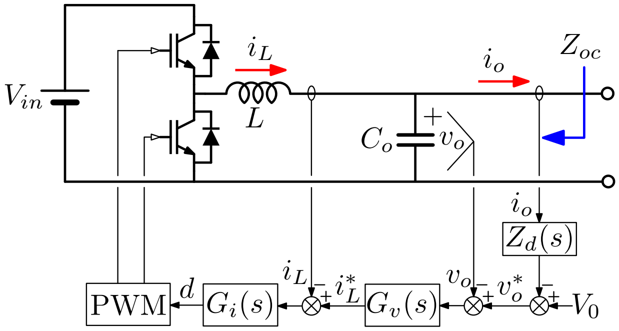


Figure 2-5: Control scheme of an example buck-type droop-controlled converter.

The system parameters used in this example are: $V_{in} = 380\,\mathrm{V}$, $V_o = 200\,\mathrm{V}$, $P_n = 3\,\mathrm{kW}$, $L = 1.6\,\mathrm{mH}$, $C_o = 200\,\mu\mathrm{F}$, $f_s = 12.5\,\mathrm{kHz}$, $r_d = 1.33\,\mathrm{V/A}$. As discussed in Section 2.2, the output capacitance C_o can be selected based on the voltage control bandwidth f_v and the droop resistance r_d. For example, f_v herein is expected to be $600\,\mathrm{Hz}$, which is $1/20$ of the switch frequency f_s, thus C_o is calculated as $200\,\mu\mathrm{F}$ according to (2.2). Based on these parameters, the current loop $T_i(s)$ [see (2.7)] and the voltage loop $T_v(s)$ [see (2.9)] are designed to have zero crossings at $1.2\,\mathrm{kHz}$ and $600\,\mathrm{Hz}$, respectively. It is worth mentioning that the voltage control bandwidth is exactly designed at its expected value. As for the droop loop, the design of $Z_d(s)$ follows (2.15), resulting in:

$$Z_d(s) = r_d - 1/G_v(s) \tag{2.20}$$

The bode diagram of $Z_{oc}(s)$ is plotted in Fig. 2-6, with $Z_d(s)$ designed in the conventional way [i.e., $Z_d(s) = r_d$] and in the proposed way [see (2.20)]. As can be seen, in both cases, $Z_{oc}(s)$ is equal to r_d at low frequency. However, with $Z_d(s)$ being r_d, $Z_{oc}(s)$ shows high magnitude, which is about 1.9 times of r_d, in medium frequency range. This output impedance actually suggests an output voltage overshoot/undershoot of $90\,\%$. To restrict the voltage fluctuation to a lower level, for instance, $10\,\%$, the output capacitance should be approximately increased to 9 times of the original value, that is, $1.8\,\mathrm{mF}$. Whereas, with the proposed $Z_d(s)$ implemented, $Z_{oc}(s)$ is nearly constant until $1\,\mathrm{kHz}$. Above this frequency, $Z_{oc}(s)$ is dominated by the output capacitance. As a result, the design target is achieved.

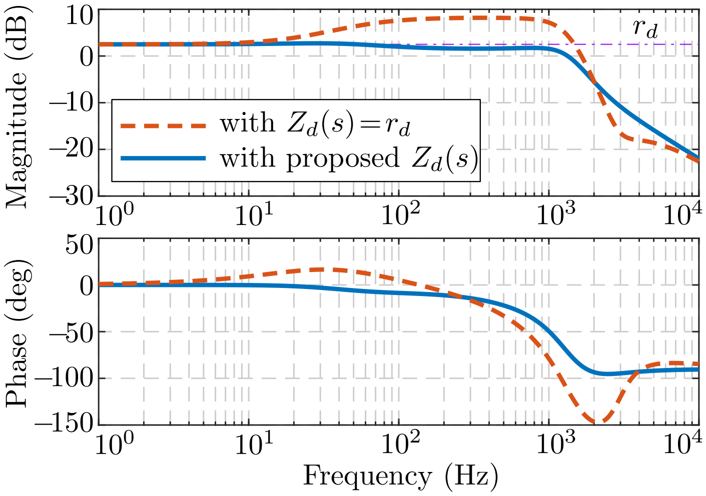


Figure 2-6: Bode diagram of the output impedance $Z_{oc}(s)$ of the buck-type droop-controlled converter shown in Fig. 2-5, using different design methods.

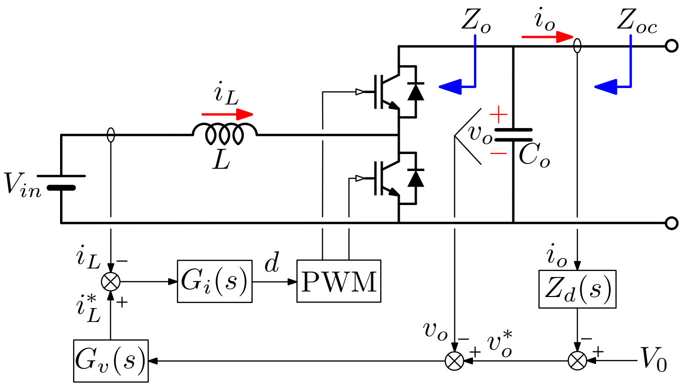


Figure 2-7: Control scheme of an example boost-type droop-controlled converter.

Boost-type converter

The Buck converter is a specific case because its small-signal model is not influenced by the operation point. Differently, for many other converters, their small-signal models change with the operation point. From this perspective, this paper aims to verify the feasibility of the proposed design method for this kind of converter by providing an example of boost converters. The control scheme of an boost-type converter is shown in Fig. 2-7. Under an operation point, the circuit of the boost converter can be linearized as follows:

$$sL \cdot \hat{i}_L = -(1 - D_p) \cdot \hat{v}_o + V_{op} \cdot \hat{d} \tag{2.21}$$

$$sC_o \cdot \hat{v}_o = (1 - D_p) \cdot \hat{i}_L - I_{Lp} \cdot \hat{d} - \hat{i}_o \tag{2.22}$$

where V_{op} is the static output voltage, I_{Lp} is the static inductor current, and D_p is the static duty cycle. In steady state, the input voltage V_{in} equals $(1-D_p)\cdot V_{op}$, and the static output current I_{op} equals $(1-D_p)\cdot I_{Lp}$. Then, by combining (2.21) and (2.22), the state variables $\hat{i}_L$ and $\hat{v}_o$ can be expressed as:

$$\hat{i}_L = \underbrace{\frac{sC_oV_{op}+I_{op}}{s^2LC_o+(1-D_p)^2}}_{G_{id}(s)} \cdot \hat{d} + \underbrace{\frac{1-D_p}{s^2LC_o+(1-D_p)^2}}_{G_{ii_o}(s)} \cdot \hat{i}_o \tag{2.23}$$

$$\hat{v}_o = \underbrace{\frac{-sLI_{Lp}+V_{in}}{sC_oV_{op}+I_{op}}}_{G_{vi}(s)} \cdot \hat{i}_L + \underbrace{\frac{-V_{op}}{sC_oV_{op}+I_{op}}}_{G_{vi_o}(s)} \cdot \hat{i}_o \tag{2.24}$$

For the complete block diagram of the linearized droop-controlled boost converter, one can refer to Fig. 2-4.

The system parameters are listed as follows: $V_{in} = 200\,\mathrm{V}$, $V_o = 380\,\mathrm{V}$, $P_n = 3\,\mathrm{kW}$, $L = 1.6\,\mathrm{mH}$, $C_o = 160\,\mu\mathrm{F}$, $f_s = 12.5\,\mathrm{kHz}$, $r_d = 2.53\,\mathrm{V/A}$. The voltage loop bandwidth f_v is expected to be $400\,\mathrm{Hz}$, and C_o is calculated as $160\,\mu\mathrm{F}$ according to (2.2). Based on these parameters, the current loop $T_i(s)$ [see (2.7)] and the voltage loop $T_v(s)$ [see (2.9)] are designed to have zero crossings at $1.2\,\mathrm{kHz}$ and $400\,\mathrm{Hz}$, respectively. Afterwards, following (2.15) and neglecting the Right-Half-Plane (RHP) pole introduced by $G_{vi}(s)$ since it is not causal, the droop impedance $Z_d(s)$ of the boost-type DER converter can be expressed as:

$$Z_d(s) = r_d - 1/[(1-D_p)G_v(s)] \tag{2.25}$$

The bode diagram of $Z_{oc}(s)$ is plotted in Fig. 2-8, with $Z_d(s)$ designed in the conventional way [i.e., $Z_d(s) = r_d$] and in the proposed way [see (2.25)]. When $Z_d(s)$ is designed as a pure resistance, $Z_{oc}(s)$ is greater than r_d from $10\,\mathrm{Hz}$ to $1\,\mathrm{kHz}$. Remarkably, with the proposed $Z_d(s)$, $Z_{oc}(s)$ is almost resistive at low frequency, satisfying the design requirement.

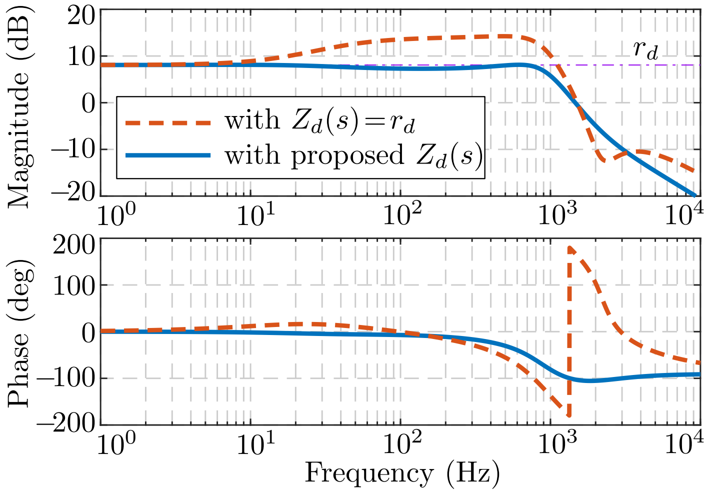


Figure 2-8: Bode diagram of the output impedance $Z_{oc}(s)$ of the boost-type droop-controlled converter shown in Fig. 2-7, using different design methods.

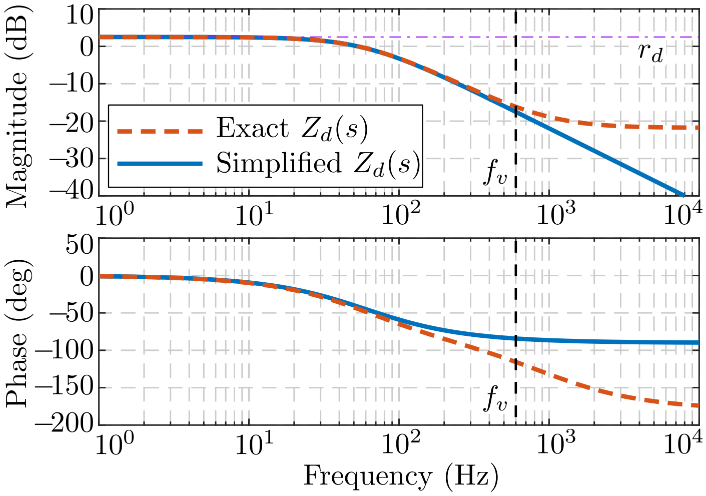
2.3.3 Simplification of the design method

When the proposed droop impedance $Z_d(s)$ shown in (2.15) is applied to a generalized droop-controlled converter, the transfer function $G_{vi_o}(s)$ and $G_{vi}(s)$ should be calculated for every kind of the converter topology. Although the calculation may not bring too much difficulty, a concise droop impedance $Z_d(s)$, which is independent of converter topologies, is still more appreciated.

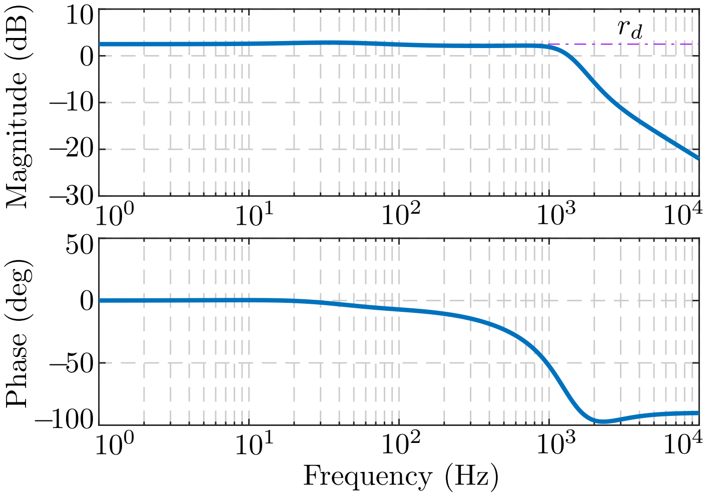
Fig. 2-9(a) depicts bode diagram of the droop impedance $Z_d(s)$ implemented in the example of buck-type converter. In fact, as the droop controller is only responsible for the output impedance up to the voltage control bandwidth f_v, the design of $Z_d(s)$ can be simplified as long as it is precise until f_v. Therefore, in this example, by performing curve fitting, the simplified version of the proposed $Z_d(s)$ is introduced as follows:

$$Z_d(s) = \frac{r_d}{s/\omega_{\mathrm{zv}} + 1} \tag{2.26}$$

where ω_{zv} is the zero of the voltage regulator $G_v(s)$. Fig. 2-9(a) also compares the exact $Z_d(s)$ defined in (2.20) and its simplified version (2.26). Clearly, within the voltage loop bandwidth, the difference between the exact and its simplified version is minor. With the simplified $Z_d(s)$ adopted, Fig. 2-9(b) shows the bode diagram of the corresponding output impedance $Z_{oc}(s)$. As expected, $Z_{oc}(s)$ is nearly resistive in the low and medium frequency



(a) Simplification of the droop impedance $Z_d(s)$



(b) Resulted output impedance with simplified deisgn method.

Figure 2-9: Simplification of the design for the buck-type converter.

range, presenting a satisfactory shape.

Similarly, for the boost-type converter, the proposed exact $Z_d(s)$ defined in (2.25) and its simplified version, which is expressed by (2.26), are shown in Fig. 2-10(a). It can be seen that the exact $Z_d(s)$ and its simplified form have a close shape. Consequently, the corresponding output impedance $Z_{oc}(s)$ presented in Fig. 2-10(b) is resistive at low frequency, verifying the effectiveness of the simplified design method.

Most importantly, the simplified $Z_d(s)$ is uniform for both buck-type and boost-type converters and is only related to the control parameters, so it can be easily extended to DER converters with different topologies.

In summary, for a droop-controlled DER converter shown in Fig. 2-3, in order to obtain resistive output impedance, the design should follow the steps below.

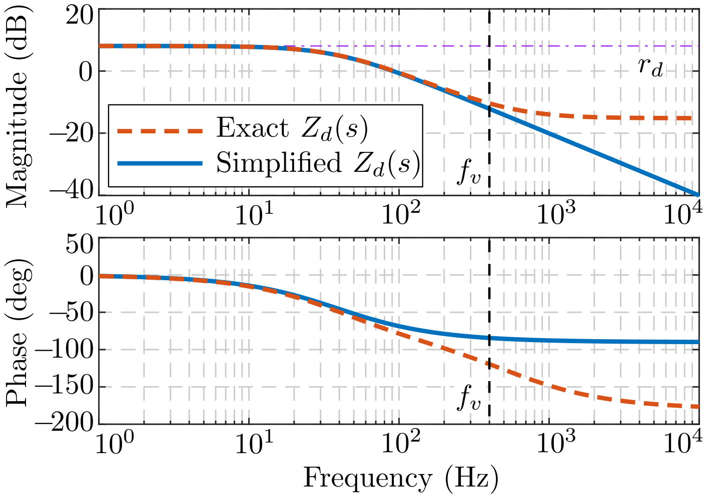
- In the beginning, taking account of control parameters like the switching frequency and the control delay (including computation time and PWM delay), a reasonable voltage control bandwidth f_v can be set;

- At the converter circuit level, based on the predicted f_v, the output capacitance C_o is selected according to (2.2);

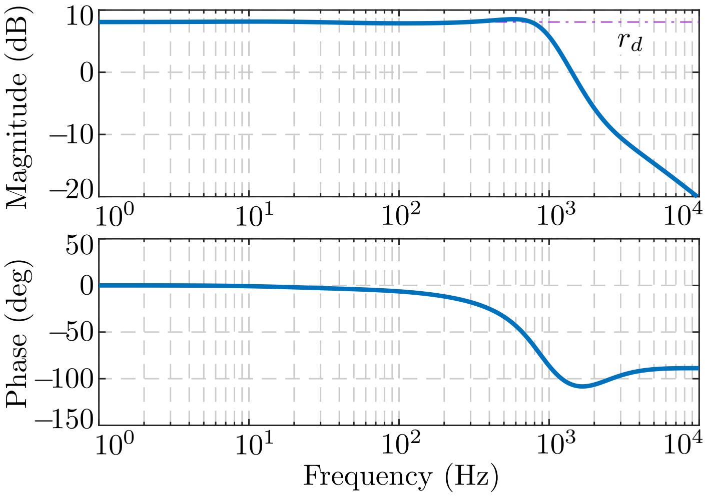
- Then, at the controller level, the current regulator $G_i(s)$ and the voltage regulator $G_v(s)$ can be designed on the basis of the current loop gain $T_i(s)$ and the voltage loop gain $T_v(s)$, respectively. The current control bandwidth can be set at, for example, $1/10$ of the switching frequency, and the voltage control bandwidth can be set at the expected value f_v;

- The droop loop is installed on the top inner current and voltage loops. The proposed droop impedance $Z_d(s)$ can be derived from (2.15) and further simplified by performing curve fitting.

In the end, it is necessary to perform an overall check of the resulted closed-loop output impedance by analytical expressions or by simulation results.



(a) Simplification of the droop impedance $Z_d(s)$



(b) Resulted output impedance with simplified deisgn method.

Figure 2-10: Simplification of the design for the boost-type converter.

2.3.4 Experimental verification

Laboratory-scale DC microgrid prototypes are set up to experimentally verify the performance of the proposed design method.

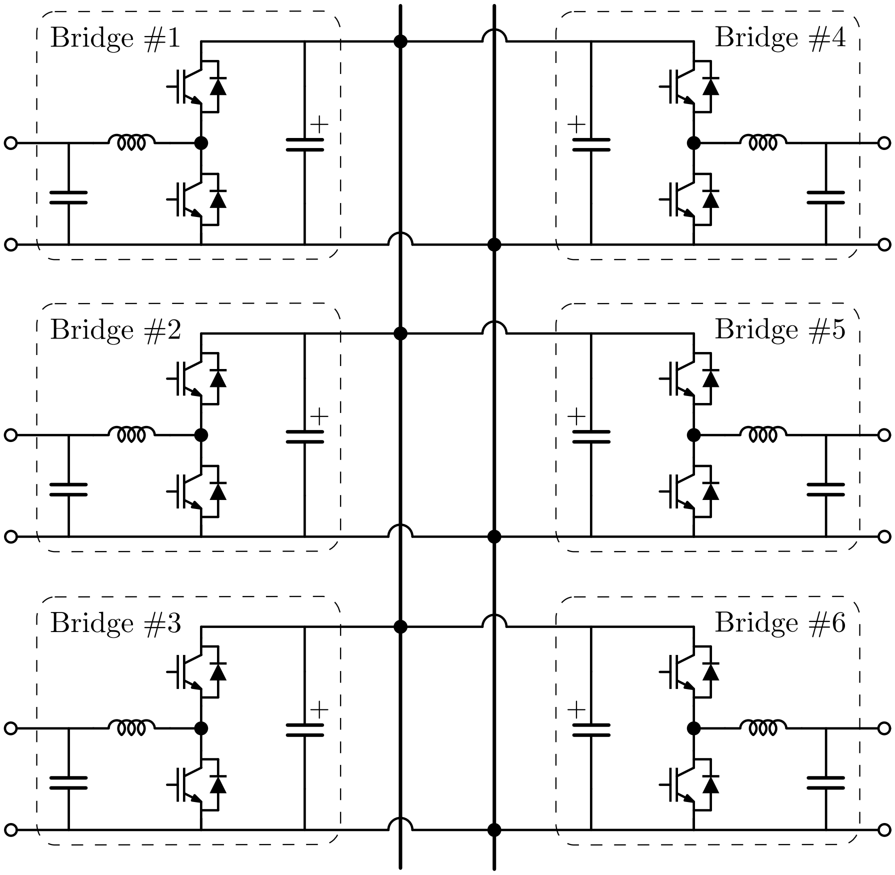
Verification on buck converters

One prototype is composed of six half-bridges and can be flexibly reconfigured. The entire plant employs one DSP (TMS320F2810) to control all of the six bridges. The circuit diagram and picture of this prototype are presented in Fig. 2-11. In this test, three bridges are connected to an external common DC bus to form a DC micorgrid prototype, as shown in Fig. 2-12. Each bridge is regarded as a bi-directional buck converter. Constant power load, which is a typical scenario of microgrids, is also considered and is emulated by DC electronic load. The system parameters are reported in Table 2.1.

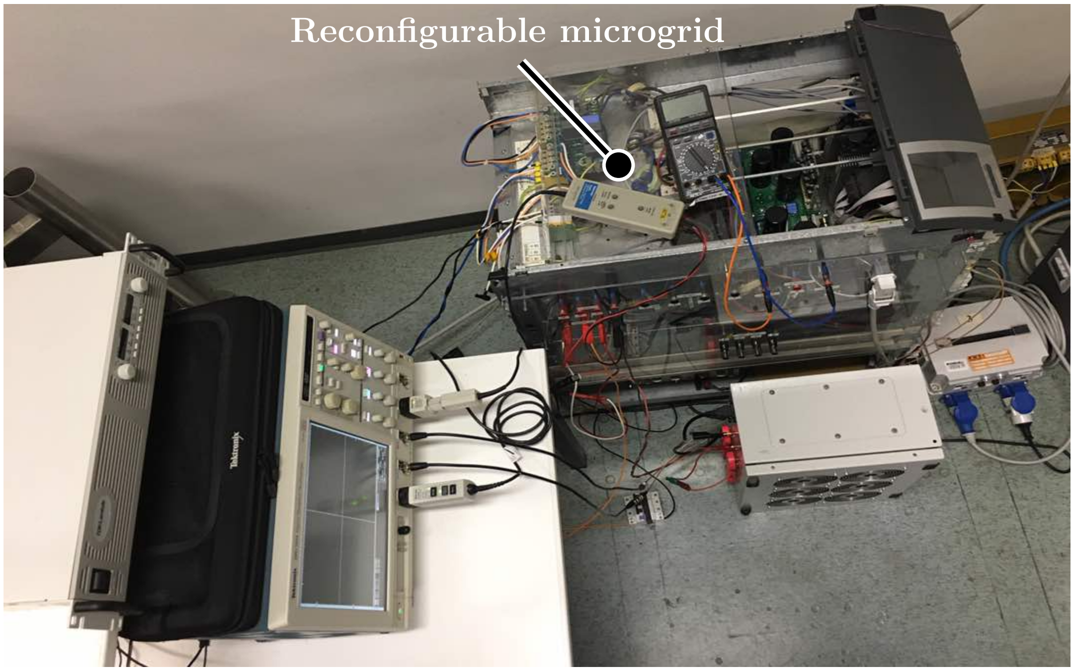
The control structure of every buck-type DER converter is shown in Fig. 2-5. Specifically, in the experimental implementation, the inductor current, which equals the output current in steady state, is taken as the feedback signal in the droop loop. In terms of the design of droop controller, considering that the switching frequency f_s is $12.5\,\mathrm{kHz}$ and the control delay is one switching cycle, the voltage control bandwidth is estimated at $600\,\mathrm{Hz}$, that is, around $1/20$ of f_s. Following the design procedure, the output capacitance is selected as $200\,\mu\mathrm{F}$ according to (2.2). The current control bandwidth and the voltage control bandwidth are designed at $1.2\,\mathrm{kHz}$ and $600\,\mathrm{Hz}$, respectively.

Output impedance measurement

The actual output impedance of one buck converter is experimentally measured by frequency sweep. Under an steady-state operation point, another converter injects sinusoidal small-signal perturbations into the DC microgrid. At injection frequency that is close to half of the switching frequency, although the perturbation signal is almost square wave instead of sinusoidal wave, it still contains corresponding frequency component. Meanwhile, the converter under measurement collects its output current and output voltage signals. Finally, the output impedance of the converter can be calculated by performing the Fast



(a) Circuit diagram



(b) Picture

Figure 2-11: Circuit diagram and picture of the reconfigurable prototype.

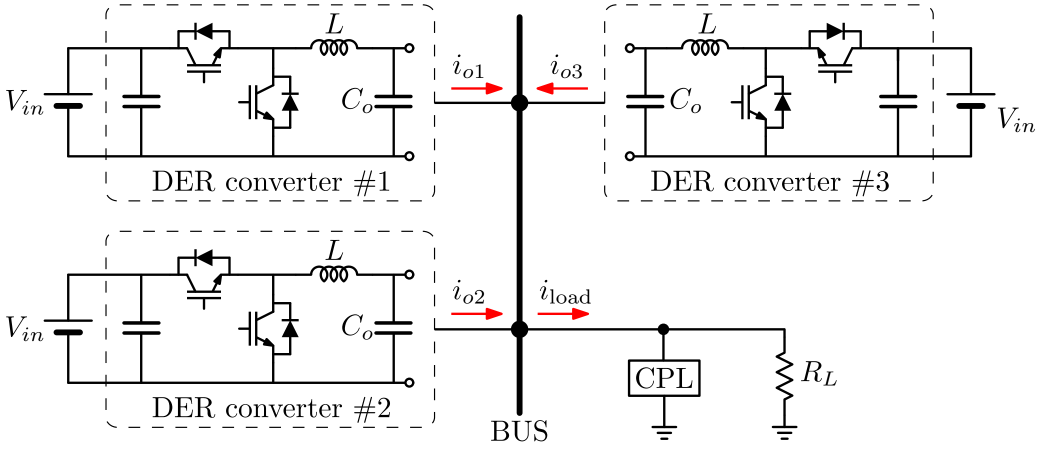


Figure 2-12: DC microgrid prototype based on buck converters.

Table 2.1: Parameters of the system shown in Fig. 2-12

Parameter	Symbol	Value
Input voltage	V_{in}	380 V
Nominal bus voltage	V_o	200 V
Nominal Power	P_n	3 kW
Inductance	L	1.6 mH
Output capacitance	C_o	200 µF
Switching frequency	f_s	12.5 kHz
Droop resistance	r_d	1.33 V/A
Current regulator	$G_i(s)$	$0.03 + 5.7/s$
Voltage regulator	$G_v(s)$	$0.7 + 267/s$

Fourier Transform (FFT) on the collected data. The output impedance measurement can be automatically completed by the Software Frequency Response Analyzer (SFRA) functions embedded in the Texas Instruments digital controllers [103]. One thing to be noted is that the amplitude of perturbation should be set at such a level that the operation point is not significantly changed. In the following measurements, the amplitude of voltage perturbation is $1\,\mathrm{V}$ which is 0.26% of the nominal bus voltage.

Fig. 2-13 shows the measured output impedance with different design principles. The actual output impedance is marked by a series of circles from $10\,\mathrm{Hz}$ to $5\,\mathrm{kHz}$, and the analytical output impedance is represented by the solid line. As can be seen, the measured output impedances almost follow the analytical ones up to half of the switching frequency, proving the accuracy of the modeled output impedances.

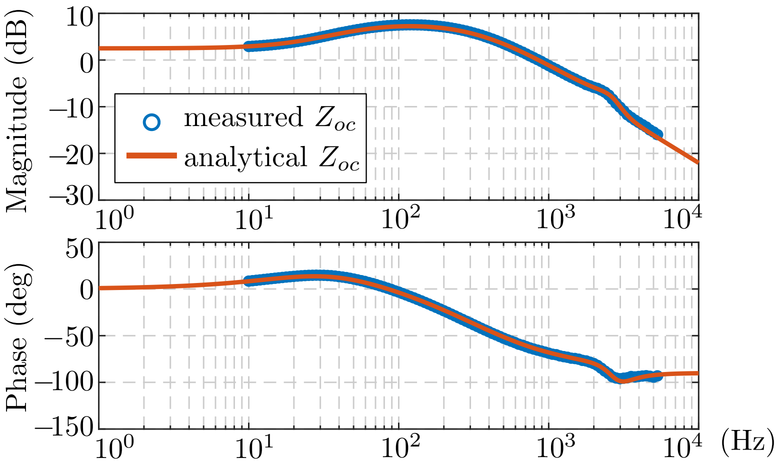
Moreover, with $Z_d(s)$ being r_d, $Z_{oc}(s)$ has higher magnitude than r_d until $600\,\mathrm{Hz}$, as shown in Fig. 2-13(a). In contrast, if $Z_d(s)$ is designed in the form of (2.15), the magnitude of the resulted $Z_{oc}(s)$ is successfully suppressed, presenting resistive characteristics at low and medium frequency, as displayed in Fig. 2-13(b). Similarly, with the simplified $Z_d(s)$ [see (2.26)], resistive-capacitive output impedance is also obtained, as presented in Fig. 2-13(c).

Voltage variations under load changes

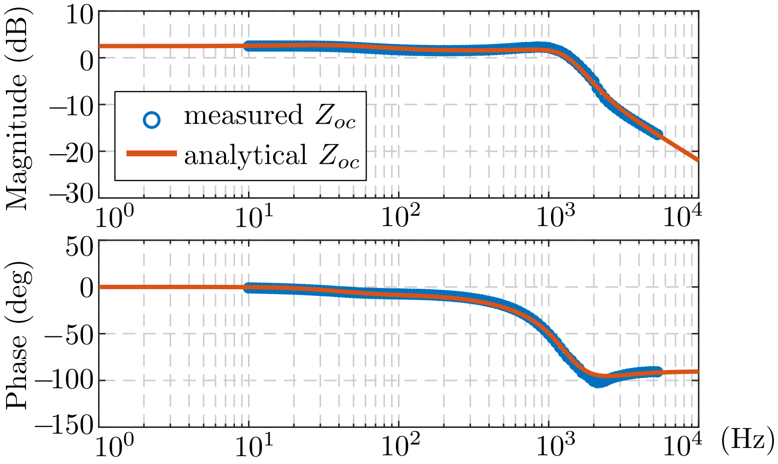
In this test, the DC bus voltage variations under load changes are evaluated. Fig. 2-14(a) shows the dynamic experimental results under a constant power load step, with the droop controller designed in the conventional way (i.e., $Z_d(s) = r_d$). As can be seen from Fig 2-14(a), when the load steps up, the bus voltage presents a significant sag of $5.5\,\mathrm{V}$ during transient. Compared to the $2.9\,\mathrm{V}$ steady-state voltage change, which is caused by the droop function, the dynamic voltage variation is almost doubled.

Fig. 2-14(b) depicts the experimental results under the same load change, with the droop controller designed in the proposed way [i.e., $Z_d(s)$ follows (2.15)]. Remarkably, the bus voltage undershoot and overshoot are successfully eliminated, verifying the feasibility of the proposed design method.

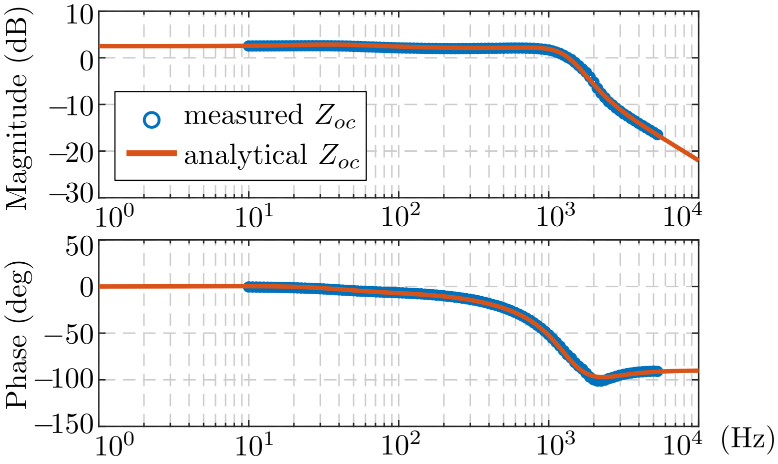
Fig. 2-14(c) displays the experimental results under the same load changes, with the



(a) $Z_d(s)$ is designed as r_d

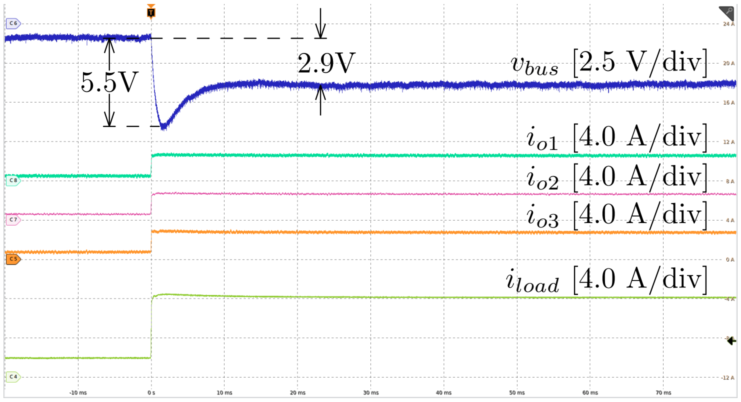


(b) $Z_d(s)$ is designed in the proposed way

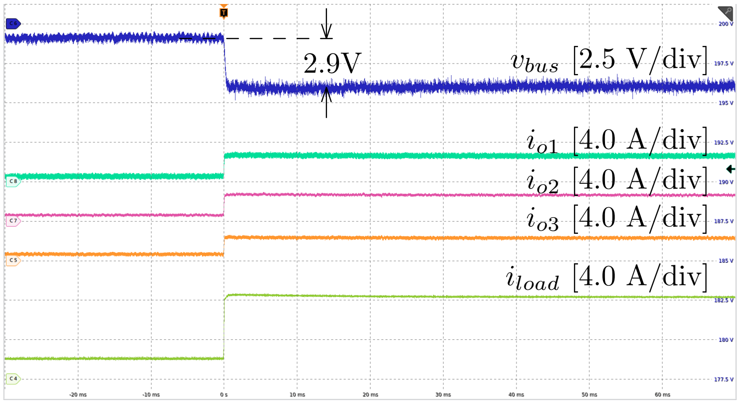


(c) $Z_d(s)$ is designed in the simplified way

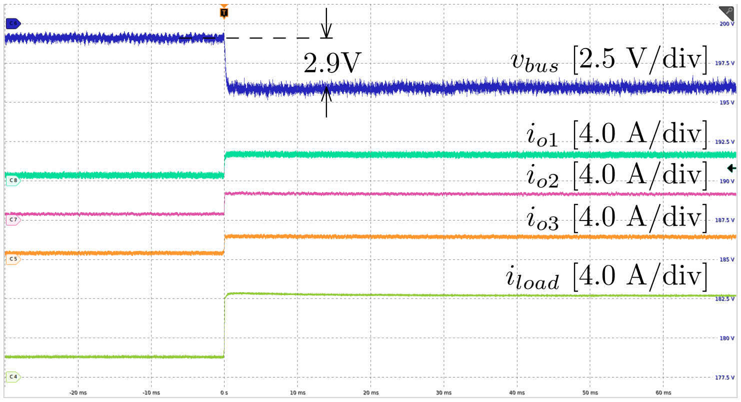
Figure 2-13: The measured and theoretical output impedance $Z_{oc}(s)$ of one buck-type droop-controlled converter, with droop controllers designed in different ways.



(a) $Z_d(s)$ is designed as r_d



(b) $Z_d(s)$ is designed in the proposed way



(c) $Z_d(s)$ is designed in the simplified way

Figure 2-14: Experimental results under a $1.2\,\mathrm{kW}$ step up of constant power load in the buck-based microgrid, with droop controllers designed in different ways. v_{bus} offset: $200\,\mathrm{V}$. Time: $10\,\mathrm{ms/div}$.

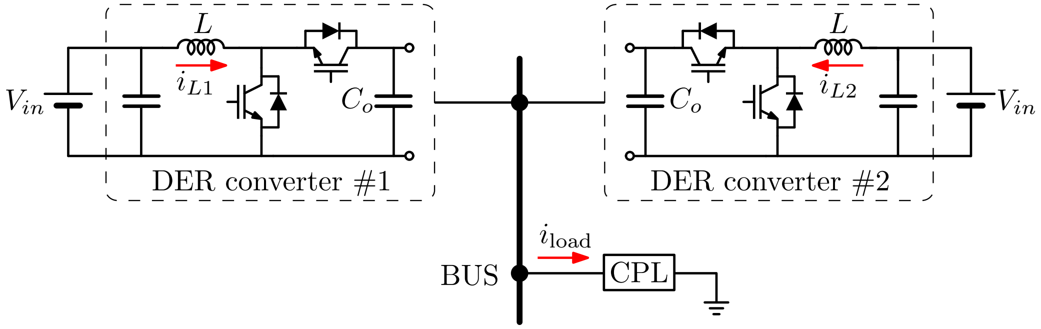


Figure 2-15: DC microgrid prototype based on boost converters.

droop controller designed in the simplified way [i.e., $Z_d(s)$ follows (2.26)]. Notably, the bus voltage is tightly regulated. Thus, the effectiveness of the simplified design method is also validated.

Verification on boost converters

The proposed design approach is also applied to the other DC microgrid prototype, which includes two boost converters, as shown in Fig. 2-15. More details of this prototype can be found in Appendix A. The system parameters are reported in Table 2.2. The control structure of every boost converter is shown in Fig. 2-7. As for the design of droop controller, since the switching frequency f_s is $20\,\text{kHz}$ and the control delay is one switching cycle, the voltage control bandwidth is predicted at $550\,\text{Hz}$ in this test. Subsequently, the output capacitance is chosen as $130\,\mu\text{F}$ according to (2.2). The current control bandwidth and the voltage control bandwidth are designed at $2\,\text{kHz}$ and $550\,\text{Hz}$, respectively.

Output impedance measurement

The output impedance $Z_{oc}(s)$ of one boost-type droop-controlled converter is experimentally measured using SFRA. Fig. 2-16 shows the measurement results with different design strategies. With the traditional design [$Z_d(s) = r_d$], $Z_{oc}(s)$ shows higher magnitude than r_d at medium frequency, as shown in Fig. 2-16(a). Whereas, if either the proposed design [refer to (2.15)] or the simplified design [refer to (2.26)] is applied, $Z_{oc}(s)$ is shaped to be resistive at low and medium frequency and to be capacitive at high frequency, as depicted in Fig. 2-16(b) and Fig. 2-16(c), respectively.

Table 2.2: Parameters of the system shown in Fig. 2-15

Parameter	Symbol	Value
Input voltage	V_{in}	$200\,\mathrm{V}$
Nominal bus voltage	V_o	$380\,\mathrm{V}$
Nominal Power	P_n	$3\,\mathrm{kW}$
Inductance	L	$1.0\,\mathrm{mH}$
Output capacitance	C_o	$130\,\mu\mathrm{F}$
Switching frequency	f_s	$20\,\mathrm{kHz}$
Droop resistance	r_d	$2.53\,\mathrm{V/A}$
Current regulator	$G_i(s)$	$0.034 + 32/s$
Voltage regulator	$G_v(s)$	$0.75 + 77/s$

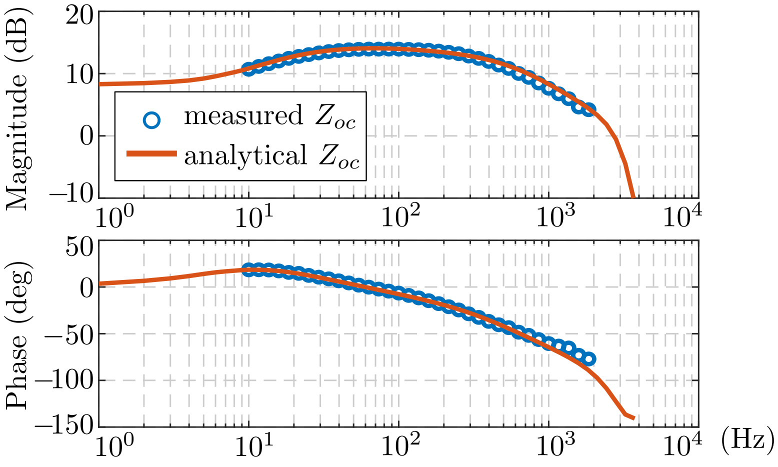
Voltage variations under load changes

Furthermore, the dynamic experiments under load changes are carried out, as shown in Fig. 2-17. With the traditional design, the DC bus voltage shows an unexpected dip of $6.5\,\mathrm{V}$ during transient, while the voltage change in steady state is only $4\,\mathrm{V}$, as shown in Fig. 2-17(a). Differently, Fig. 2-17(b) shows the case of adopting the proposed design. Notably, the DC bus voltage moves to the new level without any undershoot, demonstrating the advantage of the proposed design method. Similar results are obtained with the simplified design method, as presented in Fig. 2-17(c).

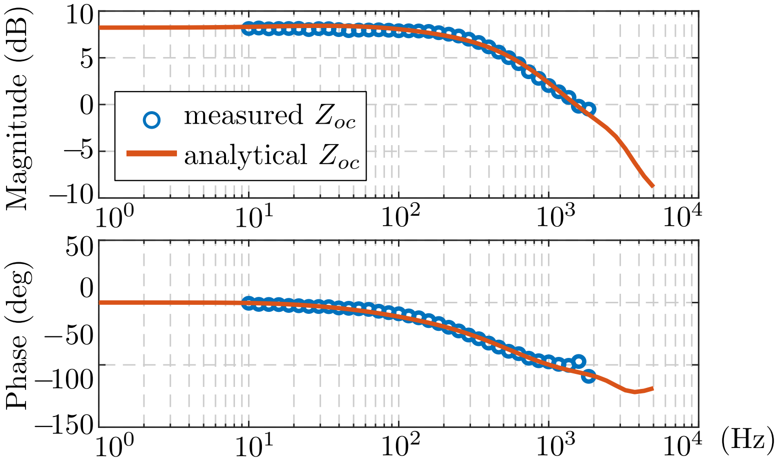
2.4 Case of isolated DC-DC converters

The proposed output impedance shaping approach can be also applied to isolated DC-DC converters. The control schemes of these converters are usually different from the one shown in Fig. 2-3. Thus, further analyses should be conducted. Herein, DAB DC-DC converters are taken as an example to demonstrate the concept, since they are adopted in many applications like electric vehicles and energy storage systems where electrical isolation and high input-output voltage ratio are required [104].

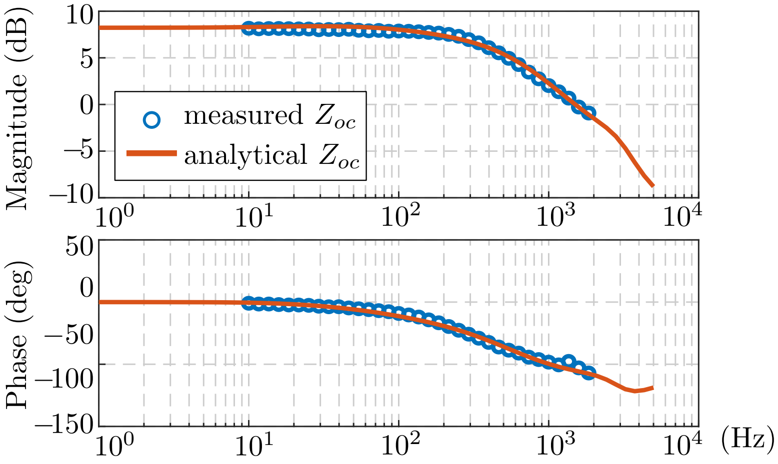
This section firstly derives the small-signal model of a DAB converter to calculate the



(a) $Z_d(s)$ is designed as r_d

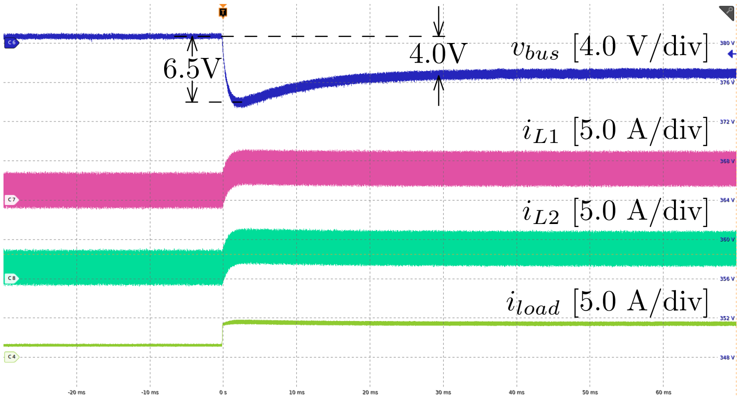


(b) $Z_d(s)$ is designed in the proposed way

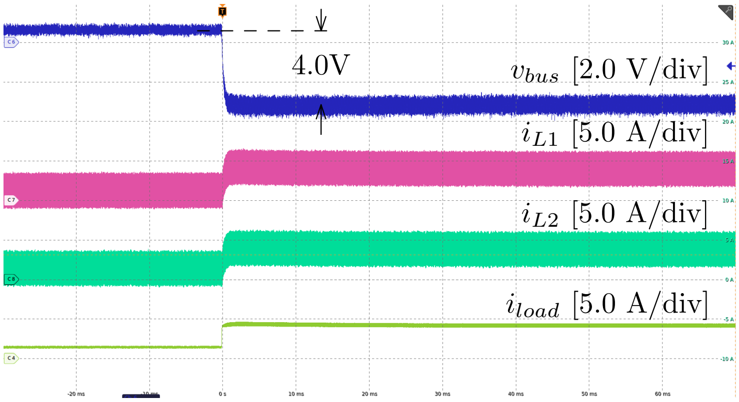


(c) $Z_d(s)$ is designed in the simplified way

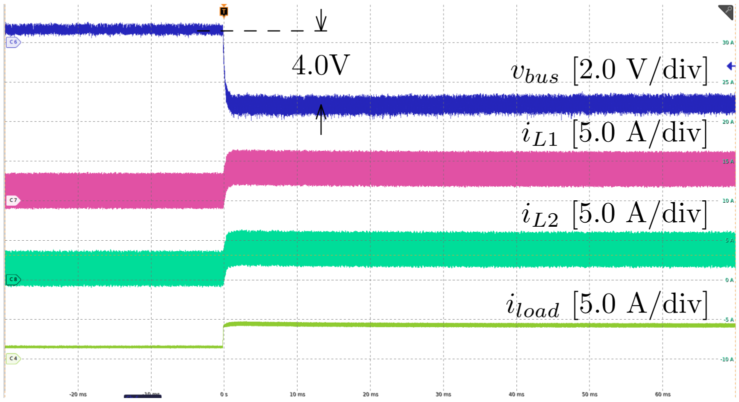
Figure 2-16: The measured and theoretical output impedance $Z_{oc}(s)$ of one boost-type droop-controlled converter, with droop controllers designed in different ways.



(a) $Z_d(s)$ is designed as r_d



(b) $Z_d(s)$ is designed in the proposed way



(c) $Z_d(s)$ is designed in the simplified way

Figure 2-17: Experimental results under a 600 W step up of constant power load in the boost-based microgrid, with droop controllers designed in different ways. v_{bus} offset: 380 V. Time: 10 ms/div.

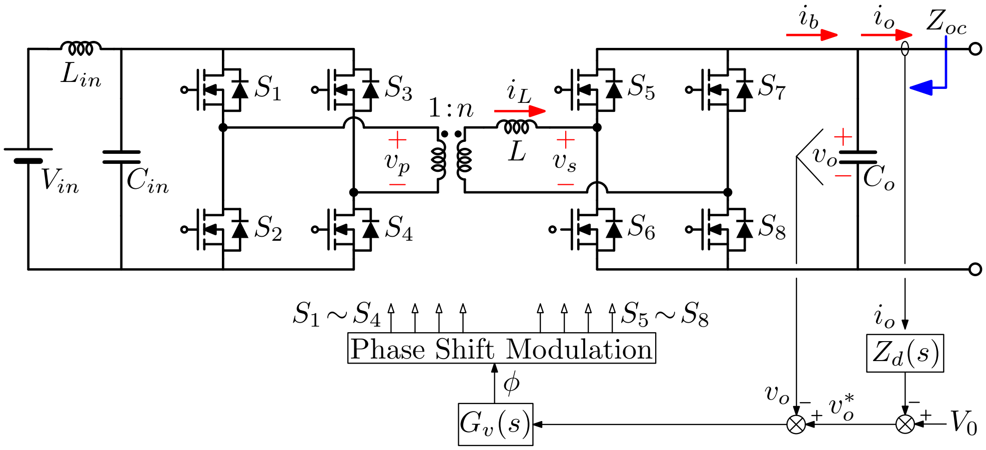


Figure 2-18: Control scheme of a droop-controlled DAB converter.

output impedance. Then, the output impedance is shaped to be resistive by adjusting the droop control parameters. In the end, experimental results are reported to show the effectiveness of the proposed design method.

2.4.1 Derivation of small-signal model

The control scheme of a droop-controlled DAB converter are shown in Fig. 2-18. The droop controller consists of a voltage loop and a droop loop. $G_v(s)$ is the voltage regulator, which usually employs PI to achieve zero steady-state error. The *V-I* droop is considered, and its function is expressed as:

$$v_o^* = V_0 - i_o \cdot Z_d(s) \tag{2.27}$$

where V_0 is the voltage set point under no-load condition and $Z_d(s)$ is the frequency-dependent droop coefficient, which has a DC value of r_d. Single-phase-shift modulation is adopted herein. The key waveforms of the DAB converter are presented in Fig. 2-19. The bridge output voltages v_p and v_s are square waves with duty cycle fixed at 50%, and the phase shift ϕ between them is adjusted for power transfer.

Different small-signal models are developed for DAB converters, covering both continuous-time [105, 106] and discrete-time models [107]. In this paper, the reduced-order continuous-time model is considered [105], since it is simple and provides enough

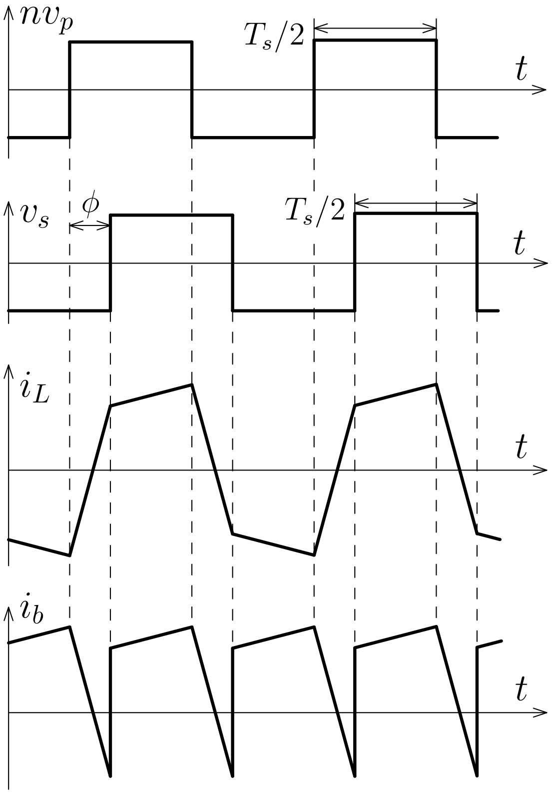


Figure 2-19: The key waveforms of the DAB converter with single-phase-shift modulation.

accuracy at the frequency range that is well below the switching frequency.

The steady-state output power P_o of the DAB converter shown in Fig. 2-18 can be calculated as:

$$P_o = V_o I_b = \frac{nV_{in}V_o\Phi(\pi - |\Phi|)}{2\pi^2 f_s L}, \quad -\frac{\pi}{2} < \phi < \frac{\pi}{2} \tag{2.28}$$

where f_s is the switching frequency, Φ is the steady-state phase shift, and the other symbols can be found in Fig. 2-18. Then, the bridge output current I_b can be expressed as:

$$I_b = \frac{nV_{in}\Phi(\pi - |\Phi|)}{2\pi^2 f_s L} \tag{2.29}$$

By linearizing (2.29) around a steady-state operation point, the transfer function $G_{i\phi}(s)$ from control to output current can be deduced as:

$$G_{i\phi}(s) = \frac{\hat{i}_b}{\hat{\phi}} = \frac{nV_{in}(\pi - 2|\Phi|)}{2\pi^2 f_s L} \tag{2.30}$$

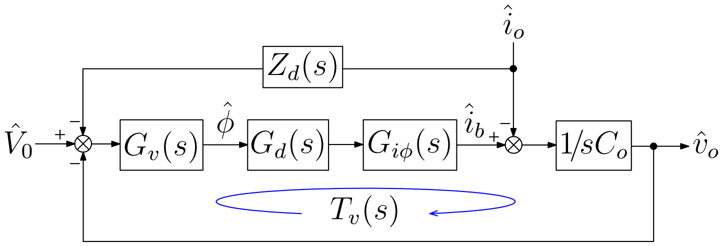


Figure 2-20: Small-signal model of the DAB converter.

Based on (2.30), the block diagram of the small-signal model of the DAB converter is illustrated in Fig. 2-20, where $G_d(s)$ is the control delay including the computation time and the modulation delay. Further, the output impedance $Z_{oc}(s)$ can be derived from this model:

$$Z_{oc}(s) = Z_d(s)T_{vCL}(s) + \frac{1}{sC_o} \cdot \frac{1}{1 + T_v(s)} \tag{2.31}$$

where $T_v(s)$ and $T_{vCL}(s)$ are open-loop and closed-loop transfer functions of the voltage loop, respectively:

$$T_v(s) = \frac{G_v(s)G_d(s)G_{i\phi}(s)}{sC_o} \tag{2.32}$$

$$T_{vCL}(s) = T_v(s)/[1 + T_v(s)] \tag{2.33}$$

To verify the accuracy of the obtained small-signal model, the voltage loop gain $T_v(s)$ is experimentally measured. Fig. 2-21 displays the comparison between the theoretical and experimental results. Clearly, the small-signal model established in this section shows enough accuracy in the frequency range that is well below the switching frequency.

2.4.2 Resistive output impedance shaping

To achieve resistive output impedance, there should be:

$$Z_{oc}(s) = r_d \tag{2.34}$$

By combining (2.31) and (2.34), $Z_d(s)$ can be solved as:

$$Z_d(s) = \frac{r_d}{T_{vCL}(s)} - \frac{1}{sC_o}\frac{1}{T_v(s)} \tag{2.35}$$

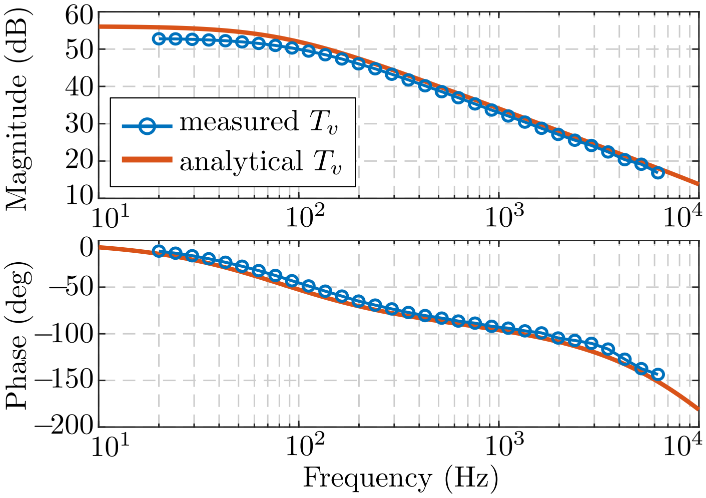


Figure 2-21: Theoretical and experimentally measured voltage loop gains of the DAB converter.

Table 2.3: Parameters of the DAB Converter shown in Fig. 2-18

Parameter	Symbol	Value
Input voltage	V_{in}	48 V
Nominal bus voltage	V_o	380 V
Nominal Power	P_n	1.5 kW
Inductance	L	186 µH
Output capacitance	C_o	12 µF
Switching frequency	f_s	60 kHz
Voltage regulator	$G_v(s)$	$0.13 + 90/s$
Droop resistance	$r_d(s)$	$5.06\,\mathrm{V/A}$

Within the voltage control bandwidth f_v, $T_{vCL}(s)$ and $G_d(s)$ can be approximated as unit gains. Finally, the required $Z_d(s)$ to accomplish resistive output impedance can be expressed as:

$$Z_d(j\omega) = r_d - \frac{1}{G_{i\phi}(j\omega)G_v(j\omega)}, \quad \omega < 2\pi f_v \tag{2.36}$$

To numerically verify the effectiveness of the proposed design method, parameters of the DAB converter are given in Table 2.3. The tolerance band of the output voltage is from $360\,\mathrm{V}$ to $400\,\mathrm{V}$, and the resulted DC droop coefficient r_d equals $5.06\,\mathrm{V/A}$. The voltage loop bandwidth f_v is designed at $3\,\mathrm{kHz}$, which is $1/20$ of the switching frequency. According

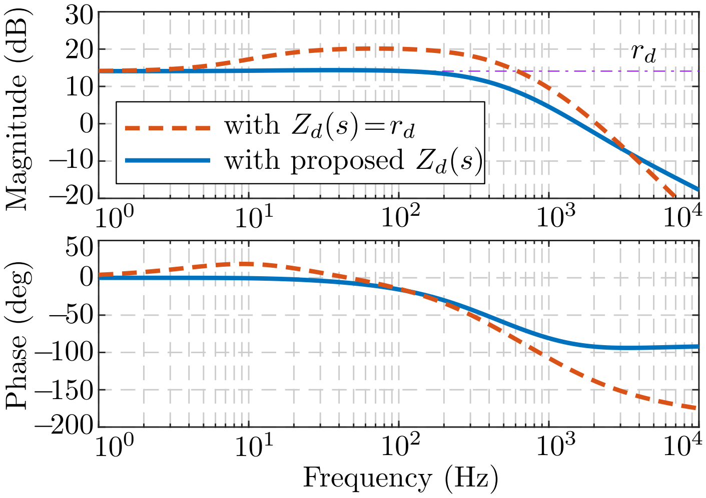


Figure 2-22: Output impedance of the DAB converter with the traditional and proposed design methods.

to (2.2), the output capacitance is selected to be $12\,\mu\mathrm{F}$. Based on these system parameters, the output impedance of the DAB converter is drawn in Fig. 2-22. In the traditional design way [i.e., $Z_d(s) = r_d$], the magnitude of the resulted $Z_{oc}(s)$ is about $6\,\mathrm{dB}$ higher than r_d from $20\,\mathrm{Hz}$ to $200\,\mathrm{Hz}$. On the contrary, after implementing the proposed design method (i.e., $Z_d(s)$ follows (2.36)), resistive output impedance is achieved.

In summary, there are three steps in the design process of a DAB converter to achieve resistive output impedance.

- The voltage control bandwidth f_v can be estimated according to the switching frequency and the control delay. The DC droop coefficient r_d can be calculated based on the voltage tolerance range and the converter's nominal output current. Following (2.2), the output capacitance can be designed.
- The voltage loop bandwidth should be designed at the estimated value by choosing proper gains for the voltage regulator $G_v(s)$.
- The droop coefficient $Z_d(s)$ should be derived from (2.36).

In the end of the design process, it is necessary to perform a final check of the resulted output impedance.

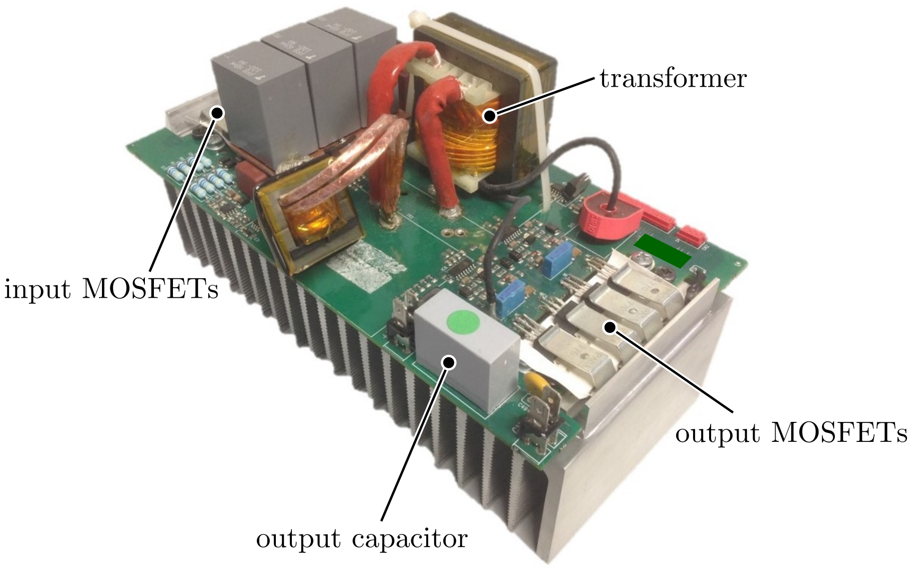


Figure 2-23: Picture of the DAB converter prototype.

2.4.3 Experimental verification

To validate the proposed design method, a DAB converter is built up. The circuit diagram can be found in Fig. 2-18 and the picture of this converter is shown in Fig. 2-23. The system parameters are the same as those reported in Table 2.3.

Output impedance measurement

In this test, the output impedance of the DAB converter is measured experimentally. The circuit diagram of the impedance measurement is presented in Fig. 2-24. The output current perturbations are generated by switching a part of the load at different frequencies. The output current and the output voltage are acquired by the oscilloscope. By performing FFT on the waveforms, the real output impedance can be obtained.

With the proposed design method, the real output impedance is measured. Fig. 2-25 gives the comparison between the measured and the theoretical output impedance. A good match can be found between them at medium and high frequency. It should be noted that the measurement result is slightly lower (around $1\,\mathrm{dB}$) than the analytical one at low frequency. This is because the voltage sensing error due to the switching ripple is not constant. Instead, it changes with the output power. The overall magnitude of the measured output impedance is lower than r_d, satisfying the design requirement.

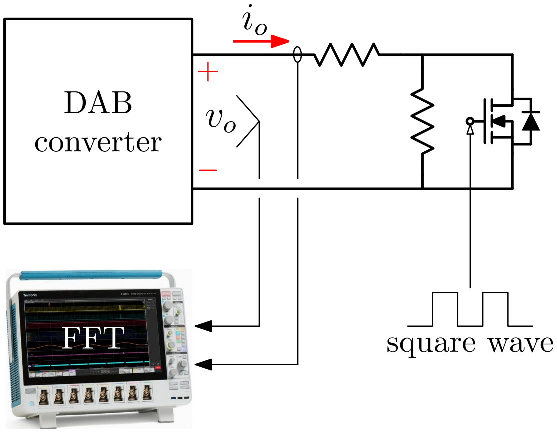


Figure 2-24: Circuit diagram of the impedance measurement.

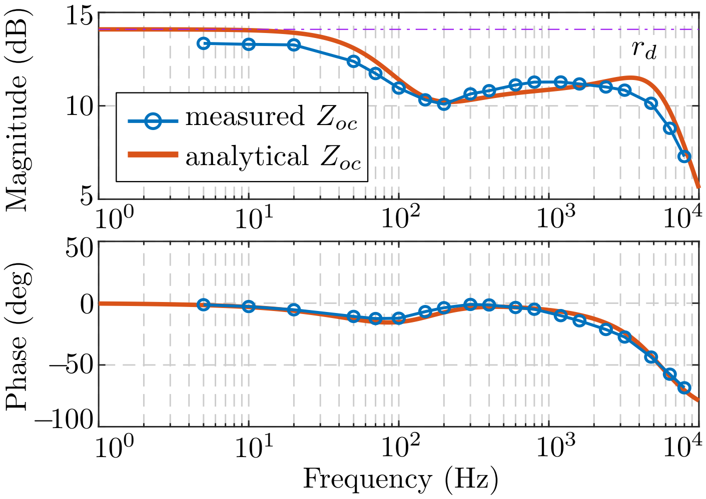
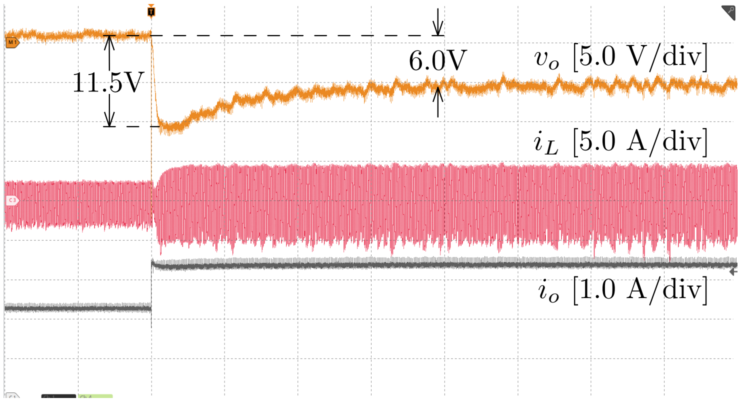
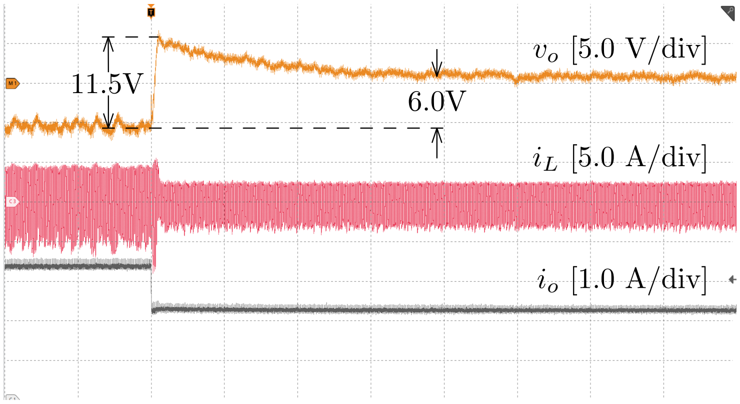


Figure 2-25: The measured and theoretical output impedance of the DAB converter, with the proposed design method.



(a) 400 W load step up



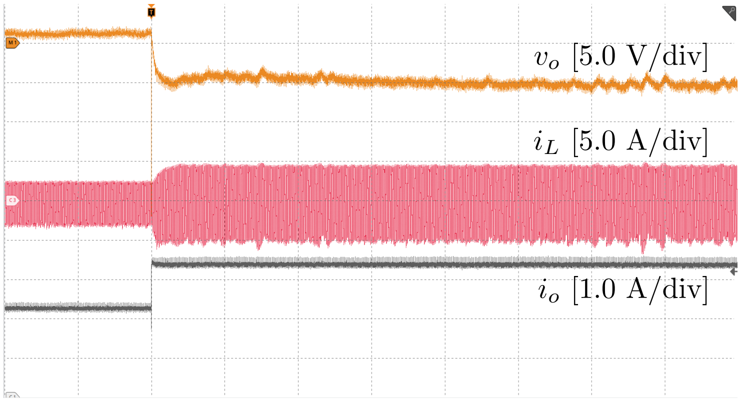
(b) 400 W load step down

Figure 2-26: Experimental results under load step changes, with DAB converters designed in the traditional way. v_{bus} offset: $370\,\mathrm{V}$. Time: $1\,\mathrm{ms/div}$.

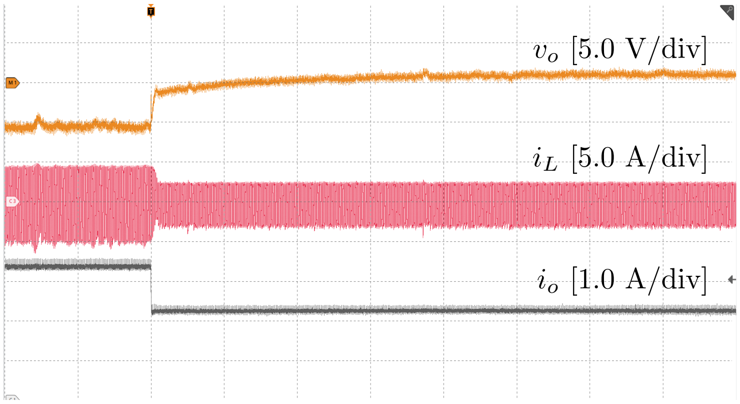
Voltage variations under load changes

The experiments under load step changes are carried out to find out the output voltage behavior. Fig. 2-26 presents the experimental results with the droop controller designed in the traditional way [i.e., $Z_d(s) = r_d$]. As seen in Fig. 2-26(a), the output voltage shows a large undershoot of $11.5\,\mathrm{V}$ in case of load step up. This voltage sag is actually almost two times of the static voltage drop due to droop function. Similar results can be found in Fig. 2-26(b) when the load steps down.

Subsequently, the droop coefficient $Z_d(s)$ is designed according to (2.36). Under the same load steps, the output voltage is tightly regulated inside the tolerance range, as shown in Fig. 2-27. Therefore, the effectiveness of the proposed design method is confirmed.



(a) 400 W load step up



(b) 400 W load step down

Figure 2-27: Experimental results under load step changes, with DAB converters designed in the proposed way. v_{bus} offset: 370 V. Time: 1 ms/div.

2.5 Implementation of hysteresis control

In Section 2.3 and Section 2.4, the inner control loops only employ traditional linear controllers. As discussed in Section 2.1.2, hysteresis control is a nonlinear technique and removes the modulator, featuring fast dynamic response. In this context, this section aims to exploit the advantages of hysteresis control to further reduce the output capacitance.

This section firstly gives a brief introduction for the structure of the hysteresis controller. Then, the implementation on a DSP-based control plant is discussed, as well as the effect of the induced one-sampling-period delay on the converter's stability. Finally, simulation and experimental results referring to a $3\,\mathrm{kW}$ boost converter are reported to demonstrate the performances of the hysteresis controller.

2.5.1 Hysteresis control structure

The control scheme of the hysteresis droop controller is presented in Fig. 2-28. It consists of two loops, an inner voltage control loop and an external droop control loop. The voltage loop regulates the output voltage v_o to track its reference v_o^*. A first-order low-pass filter LPFv is used to attenuate high-frequency noises. On top of the voltage loop, the droop loop is added to adjust the voltage reference v_o^* according to the output current i_o, achieving the droop function:

$$v_o^* = V_0 - i_o \cdot r_d \cdot G_{\mathrm{Li}}(s) \tag{2.37}$$

where V_0 is the voltage set point under no-load condition, r_d is the droop resistance, and $G_{\mathrm{Li}}(s)$ is a first-order low-pass filter to slow down the rate of change of v_o^*.

The hysteresis regulator, as shown in Fig. 2-28, distinguishes the hysteresis technique from others. It is constructed on the basis of a hysteretic differentiator and a PI controller. These two elements are responsible for instant actions and zero steady-state error, respectively. More details about these two components are discussed below.

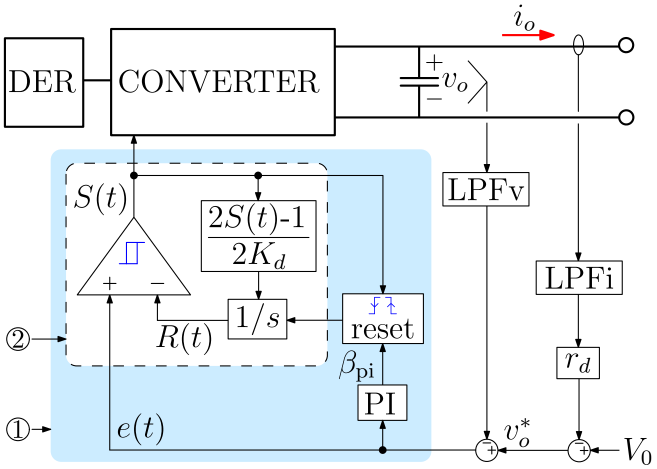


Figure 2-28: Control scheme of the hysteresis droop controller. ① The hysteresis regulator; ② The hysteretic differentiator.

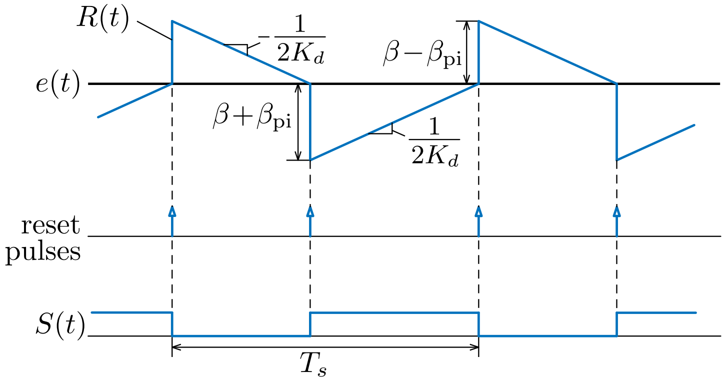


Figure 2-29: Operation principle of the hysteresis droop controller.

Hysteretic differentiator

The hysteretic differentiator, which is composed of a comparator and an integrator, is the heart of the proposed control method, as illustrated in the dashed area in Fig. 2-28. In the sense of small-signal, this hysteretic differentiator emulates the behavior of a derivative term, providing leading phase for the voltage loop gain and ensuring fast dynamic response.

The relevant waveforms are displayed in Fig. 2-29 to show the operation principle. The switching signal $S(t)$ is generated by comparing the error signal $e(t)$ and the ramp state

$R(t)$, and it has two possible states, 0 and 1.

$$S(t) = \begin{cases} 0, & \text{if } e(t) < R(t) \\ 1, & \text{else} \end{cases} \tag{2.38}$$

In terms of $R(t)$, it is ramped down at a slope of $-1/2K_d$ when $S(t) = 0$. Whereas, it is ramped up at a slope of $1/2K_d$ when $S(t) = 1$. At the moment that $R(t)$ crosses $e(t)$, $R(t)$ is reset. The reason to implement this reset action will be explained later. By choosing proper control parameters, $R(t)$ would oscillate around $e(t)$ within a certain hysteresis band, as can be seen in Fig. 2-29.

A simplified small-signal model of the hysteretic differentiator is derived as below. Let us approximately assume that $e(t)$ has the same average value as $R(t)$, which is a common supposition in the analysis of hysteresis loops. Then, there is:

$$\hat{e}(s) \approx \hat{R}(s) = \frac{\hat{S}(s)}{sK_d} \quad \Rightarrow \quad \hat{S}(s) \approx \hat{e}(s) \cdot sK_d \tag{2.39}$$

It is clear that the hysteretic differentiator behaves like a traditional differentiator from small signal point of view. On the other hand, in case of large-signal variations, the hysteretic differentiator shows instant actions once $e(t)$ crosses $R(t)$, improving the transient response.

This hysteretic differentiator also stabilizes the switching frequency, which is accomplished by the *reset* block in Fig. 2-28. When a rising edge is detected in $S(t)$, $R(t)$ is reset downward by $\beta + \beta_{\text{pi}}$, where β is a constant value and β_{pi} is the output of the PI controller. On the other hand, when a falling edge is detected in $S(t)$, $R(t)$ is reset upward by $\beta - \beta_{\text{pi}}$. Therefore, the switching frequency is only decided by the total hysteresis window height, which is equal to 2β, and the slope of $R(t)$, which is equal to $1/2K_d$. As a consequence, the switching frequency is fixed in steady state and can be expressed as:

$$f_s = 1/(4\beta K_d) \tag{2.40}$$

It should be noticed that, (2.40) is based on the condition that $e(t)$ and β_{pi} have negligible

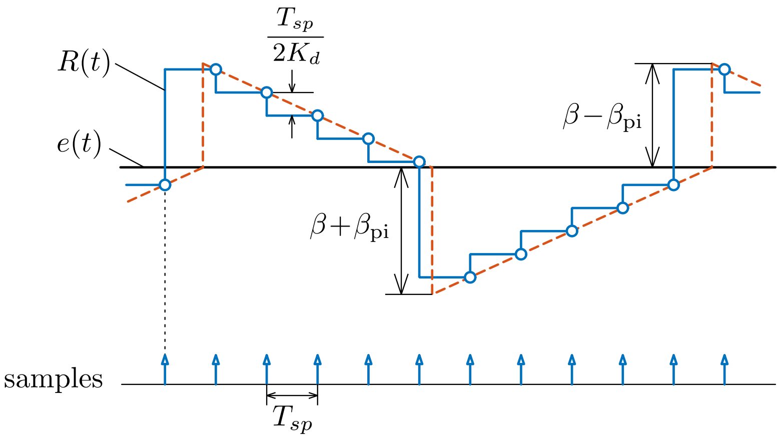


Figure 2-30: Operation principle of the hysteresis droop controller in DSP implementation.

variations in one switching cycle. Otherwise, this equation no longer holds.

PI controller

A PI controller is adopted here to force the output voltage v_o to follow its reference value v_o^* in steady state. Its output β_{pi} is used to adjust the relative position of $R(t)$ and $e(t)$. For example, considering the case that v_o is smaller than v_o^*, so $e(t)$ is larger than zero. Then, under the function of the PI controller, β_{pi} increases. The position of $R(t)$ moves downward compared to the position of $e(t)$, which means that more time is allocated to the switching state $S(t)=1$. In such a case, v_o increases until reaching v_o^*.

2.5.2 DSP implementation

The operation waveforms shown in Fig. 2-29 can only be realized in analog implementation. When migrated to digital platform, the operation principle changes.

A marked difference between analog and digital implementation is that the sampling frequency in digital implementation is finite and limited by the analog-to-digital conversion time and the computation time. Especially, when applied to DSP-based control system, computation takes a significant amount of time. Fig. 2-30 depicts the key waveforms of the digital hysteresis droop controller. As can be seen, $R(t)$ becomes a series of discrete points instead of a smooth curve. Importantly, $R(t)$ should be updated in a way that every point is located on the continuous curve, so that the digital controller's behavior exactly follows

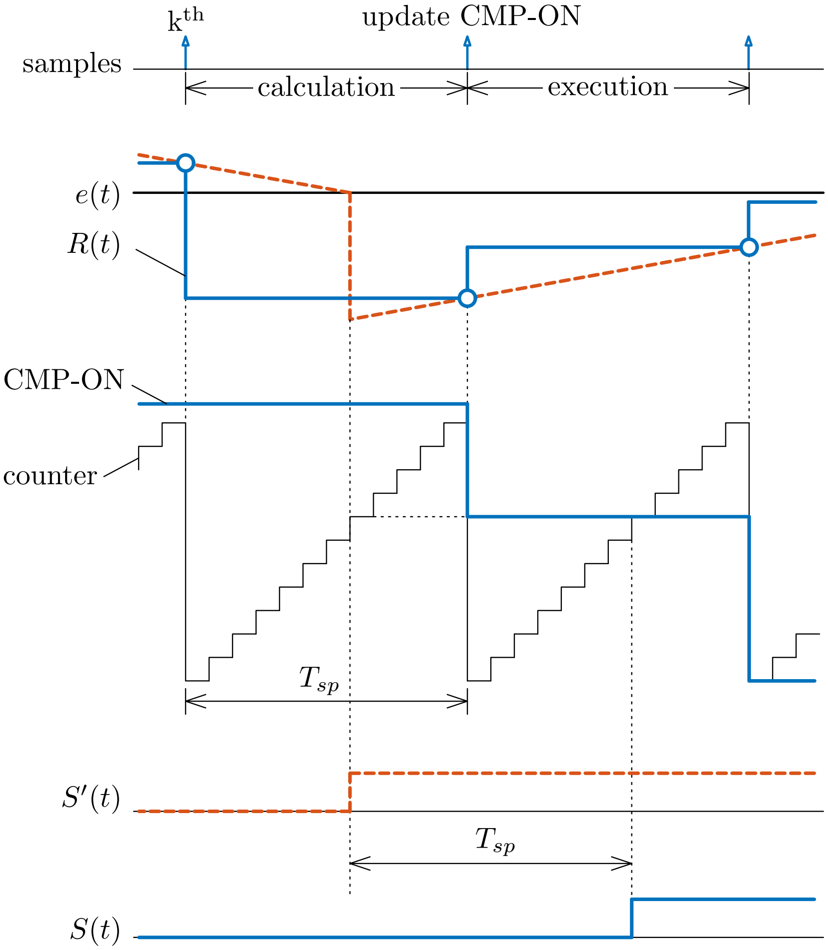


Figure 2-31: The switching signal $S(t)$ is generated by comparing a counter clocked at the system frequency and a variable CPM-ON.

the analog one.

Another phenomenon which should be noticed is that the DSP implementation induces non-negligible calculation time. The switching actions of hysteresis control are directly decided by the controller without any modulator. However, the controller operates at the sampling frequency f_{sp}, which is only several times of the switching frequency f_s. Thus, if the switching actions is synchronized with the sampling instants, the resolution of the resulted duty cycle is too low. For example, in the case that f_{sp} is 10 times of f_s, the synchronized duty cycle has a resolution of $10\,\%$. To solve this problem, a counter clocked at the system frequency is generated inside DSP, and it is exploited to trigger the sampling and to increase the resolution, as shown in Fig. 2-31. At the k$^{\mathrm{th}}$ instant, the voltage and current are acquired and processed in the following sampling period. The moment when $R(t)$

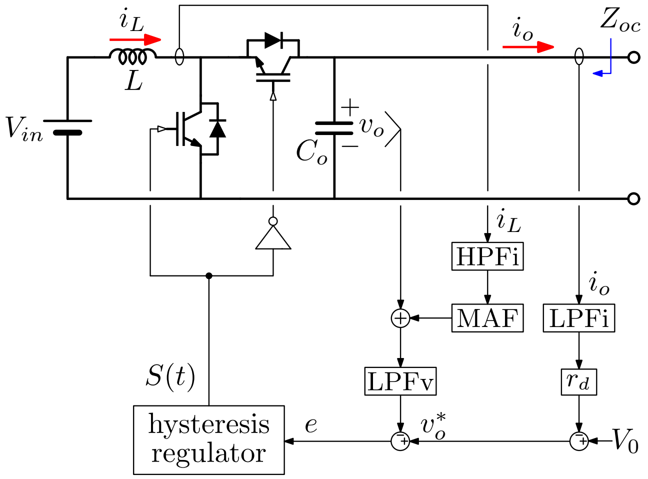


Figure 2-32: The boost DC-DC converter with the hysteresis droop controller. The structure of the hysteresis regulator can be found in Fig. 2-28.

crosses $e(t)$ is predicted, and the required compare value CMP-ON is calculated so that it intersects with the counter at the same moment. Then, at the $(\mathrm{k}+1)^{\mathrm{th}}$ instant, CMP-ON is updated and the switching state is changed in the following sampling period. Inevitably, the real switching signal $S(t)$ shows one-sampling-period delay compared with the ideal signal $S'(t)$.

2.5.3 Simulation results

To verify the effectiveness of the hysteresis droop controller, a model of boost DC-DC converter is built in MATLAB/SIMULINK. The control scheme is presented in Fig. 2-32. Compared to the control structure in Fig. 2-28, the model considered in simulation takes the inductor current i_L as an additional feedback signal. This is a particular modification only for the boost converter to suppress the effect of the RHP zero. A high-pass filter HPFi and a moving average filter MAF are inserted into the feedback path of i_L to remove the DC component and the switching ripple, respectively. The system parameters are reported in Table 2.4. The nominal power is $3\,\mathrm{kW}$ and the output capacitance is only $50\,\mu\mathrm{F}$. The acceptable range for the output voltage is from $360\,\mathrm{V}$ to $400\,\mathrm{V}$. The nominal switching frequency f_s is $20\,\mathrm{kHz}$ and the sampling frequency f_{sp} is fixed at $200\,\mathrm{kHz}$, which is 10 times more than f_s.

Table 2.4: Parameters of the hysteresis-based converter

Parameter	Symbol	Value
Input voltage	V_{in}	$200\,\mathrm{V}$
Nominal output voltage	V_o	$380\,\mathrm{V}$
Nominal Power	P_n	$3.0\,\mathrm{kW}$
Inductance	L	$1.0\,\mathrm{mH}$
Output capacitance	C_o	$50\,\mu\mathrm{F}$
Switching frequency	f_s	$20\,\mathrm{kHz}$
Sampling frequency	f_{sp}	$200\,\mathrm{kHz}$
Droop resistance	r_d	$2.53\,\mathrm{V/A}$
Cutoff frequency of LPFi	ω_{Li}	$2\pi \cdot 100\,\mathrm{rad/s}$
Cutoff frequency of HPFi	ω_{Hi}	$2\pi \cdot 300\,\mathrm{rad/s}$
Cutoff frequency of MAF	ω_{M}	$2\pi \cdot 20000\,\mathrm{rad/s}$
Cutoff frequency of LPFv	ω_{Lv}	$2\pi \cdot 20000\,\mathrm{rad/s}$
Proportional gain of PI	K_p	0.35
Integral gain of PI	K_i	0.0015
Ramp slope	K_d	0.45
Hysteresis window height	β	5.56

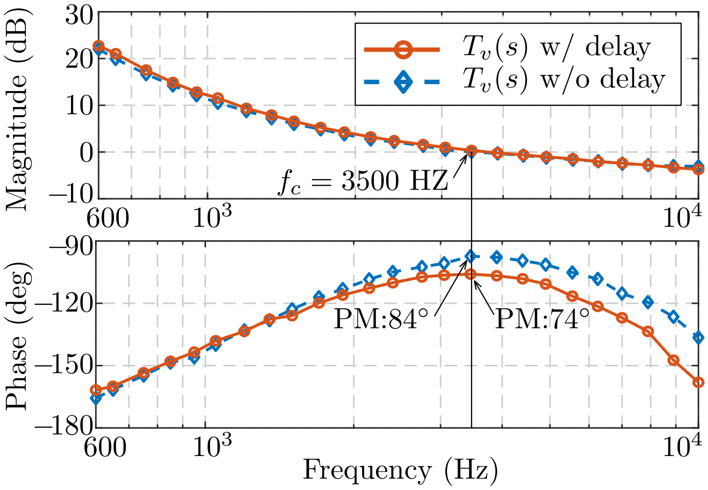


Figure 2-33: The voltage loop gain $T_v(s)$, with and without the one-sampling-period delay.

Effect of one-sampling-period delay

The effect of the one-sampling-period delay introduced by the DSP implementation is studied herein, by evaluating the voltage loop gain $T_v(s)$, which is expressed as:

$$T_v(s) = \frac{G_{\text{Lv}}(s) \cdot \hat{v}_o + G_{\text{Lv}}(s) G_{\text{Hi}}(s) G_{\text{M}}(s) \cdot \hat{i}_L + G_{\text{Li}}(s) r_d \cdot \hat{i}_o}{\hat{e}} \tag{2.41}$$

where e is the error signal marked in Fig. 2-32. The frequency response of $T_v(s)$ is measured in simulation by injecting small-signal sinusoidal perturbations at different frequency points. The loop gains with and without the one-sampling-period delay are both evaluated. The measurement results are shown in Fig. 2-33. The voltage loop has a crossover frequency of $3.5\,\text{kHz}$, which is around $1/6$ of the switching frequency. Although the time delay introduced by the DSP implementation brings a lagging phase of $-10°$, the phase margin is still as large as $74°$. Therefore, from the point of view of small-signal stability, the influence of the one-sampling-period delay is acceptable.

Output impedance measurement

The output impedance Z_{oc} of the boost DC-DC converter with the hysteresis droop controller is measured in simulation, by stimulating the system at different frequency points. The measurement result is shown in Fig. 2-34. A magnitude valley appears around $200\,\text{Hz}$.

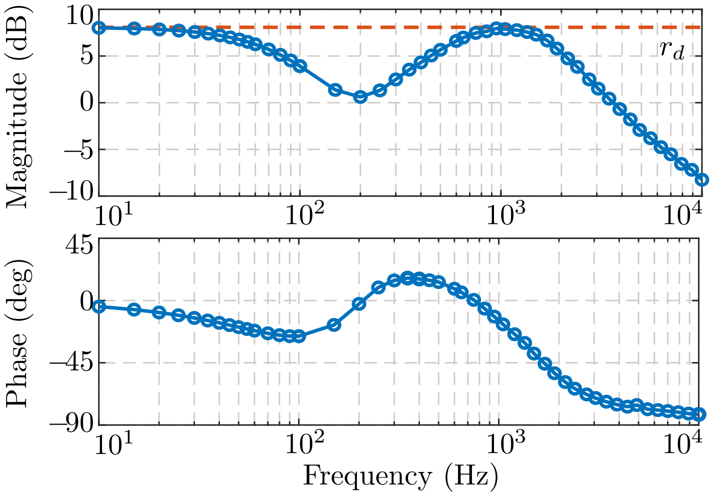


Figure 2-34: Simulated output impedance Z_{oc} of the boost converter with the hysteresis droop controller.

Below this frequency, v_o follows its reference v_o^*, and Z_{oc} is dominated by the droop function. The overall magnitude of Z_{oc} is equal to or lower than the droop resistance r_d in full frequency range. Hence, from small-signal perspective, the output voltage stays within the allowable range when facing a load change.

Steady-state simulation result

The steady-state waveforms under nominal load are presented in Fig. 2-35. The output voltage v_o is stably regulated and shows a switching ripple of $3\,\mathrm{V}$, which is about 0.8% of the nominal value. The inductor current i_L has a switching ripple of $4\,\mathrm{A}$, accounting for 30% of the nominal value. Due to these switching ripples, the error signal $e(t)$ is not constant in steady-state and presents switching-frequency fluctuation, which is about 15% of the ramp height. Regardless of the switching ripple in $e(t)$, the switching signal $S(t)$ still has a constant duty cycle. However, the actual switching frequency is affected and is 1.1 times as much as the nominal value. In order not to further amplify the switching ripple, the derivative gain (i.e., the ramp slope K_d) cannot be increased any more. It is worth mentioning that the nominal load condition is the worst case, because v_o has the largest switching ripple.

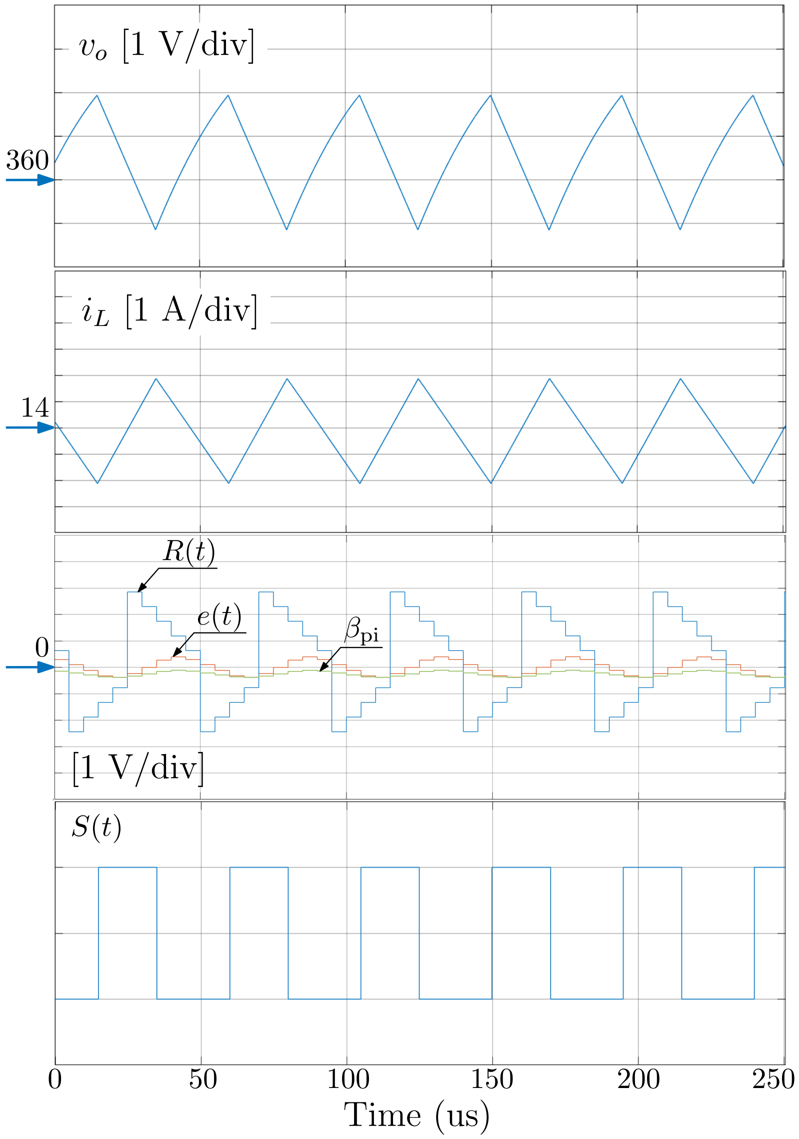


Figure 2-35: Steady-state simulation result of the boost converter with the hysteresis droop controller.

2.5.4 Experimental results

To experimentally demonstrating the dynamic performance of the hysteresis droop controller, the $3\,\mathrm{kW}$ boost DC-DC converter shown in Fig. 2-15 is utilized. The control scheme is the same as Fig. 2-32. The system parameters are listed in Table 2.4. The DSP utilized in this prototype is TMS320F28379D, with a system clock frequency of $200\,\mathrm{MHz}$.

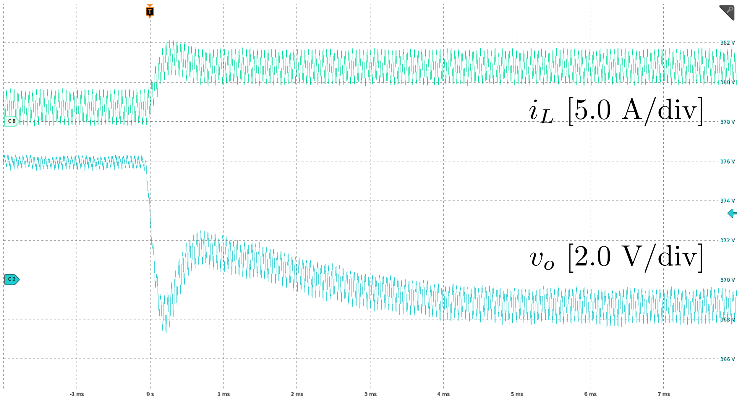
The dynamic experimental results, in case of load step up and step down, are depicted in Fig. 2-36(a) and Fig. 2-36(b), respectively. Notably, the output voltage drop during transient is not lower than the static drop, so v_o is strictly confined to the tolerance band, verifying the feasibility of the hysteresis droop controller. Moreover, in steady state, v_o and i_L present little fluctuations, which means that the proposed controller is not amplifying sample noises. This characteristic is obtained, in our case, by the low-pass filters, especially LPFv, used in the controller.

2.6 Summary

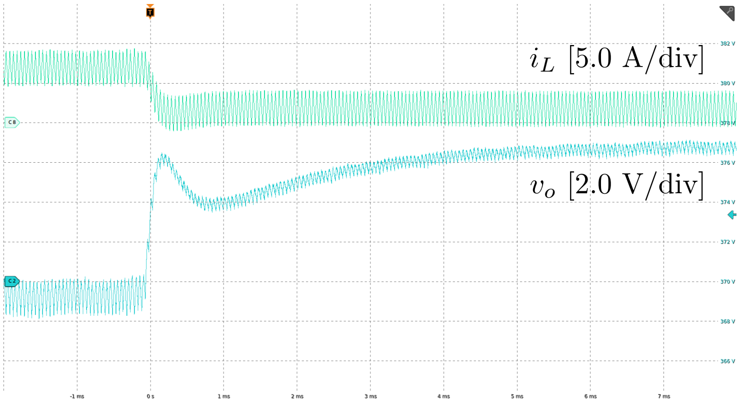
In this chapter, different control methods toward the reduction of DC bus capacitance are studied, from the perspectives of the design of droop control and the utilization of hysteresis control.

Firstly, the output capacitance of droop-controlled DC-DC converters in DC microgrids is reduced by shaping resistive output impedance. The output impedance shaping approach involves the selection criterion of output capacitance and the design of droop impedance. In particular, the output capacitance is chosen according to the voltage control bandwidth and the droop resistance, and the droop impedance is designed as a frequency-dependent term instead of a constant. Following this design methodology, resistive output impedance can be obtained on droop-controlled DC-DC converters. The effectiveness of the proposed design method has been verified by experimental results performed on buck-based and boost-based laboratory-scale DC microgrid prototypes.

Secondly, the digital application of the hysteresis droop controller on DER converters in DC mcirogrids is investigated. This controller removes the DPWM modulator used in the traditional PID controller, so the time delay in the voltage control loop is reduced. As



(a) 1 kW load step up



(b) 1 kW load step down

Figure 2-36: Dynamic experiment results of the boost converter with the hysteresis droop controller. v_o offset: $370\,\mathrm{V}$. Time: $1\,\mathrm{ms/div}$.

a consequence, the loop bandwidth can be further increased, for example, it is designed at $1/6$ of the switching frequency in this chapter. Moreover, the hysteresis controller features nonlinear behaviour in case of large-signal perturbations, speeding up the large-signal dynamic response. Thanks to these two advantages, a smaller output capacitance can be used while always keeping the output voltage within the tolerance band. This control method is implemented on a DSP-based $3\,\mathrm{kW}$ boost DC-DC converter with a sampling frequency of $200\,\mathrm{kHz}$. Although the DSP implementation brings one-sampling-period delay, it does not shows a significant influence on the small-signal stability. Simulation and experiment results validate the feasibility of the hysteresis controller.

Chapter 3

Suppression of second-order harmonic current

When DC microgrids are coupled with AC systems, second-order harmonics typically appear on the DC bus voltage, causing significant harmonic currents at the converters resource side. This chapter shows how to reduce such undesired currents by means of notch filters and resonant regulators included in the converters control loops. The main characteristics of the techniques in terms of harmonic attenuation and stability are systematically investigated.

This chapter is organized as follows. Section 3.1 reviews the existing approaches to suppress the second-order harmonic current ripples. Section 3.2 analyzes the issue of second-order harmonic current for a generic droop-controlled DC-DC converter. Section 3.3 investigates the method using a notch filter, focusing on the converter output impedance and stability. Section 3.4 introduces the modified notch filter and compares its performance with the notch filter; the design of the filter is reported in this section too. Section 3.5 and Section 3.6 briefly discusses the resonant regulator and the modified resonant regulator methods, respectively. Section 3.7 summarizes and compares the obtained results. Finally, Section 3.8 reports the experimental verification of the presented theoretical results and the methods.

3.1 State-of-the-art

DC microgrids can be linked to the AC utility mains or AC microgrids through GIC, to allow power balancing flexibility and energy trading [108, 109]. In a small-scale DC microgrid, a single-phase bidirectional converter can be used as GIC [110]. In this case, when the GIC operates at unity power factor, a second-order ripple inevitably appears in the DC bus voltage. This ripple also occurs with three-phase GIC under unbalanced voltages [111].

As described in Chapter 2, droop-controlled DER converters usually show low output impedance at twice the line frequency. In this case, the second-order bus voltage perturbation causes large current fluctuations flowing into the resource side of the converters. In some applications (e.g., fuel cells, batteries), the corresponding second-order harmonic current is detrimental, because it may shorten devices lifetime [112].

The issue of second-order harmonic current can be addressed by means of both hardware and control solutions. Hardware solutions, like increasing the bus capacitance [113], using different GIC topologies [114], and installing active power decoupling circuits [115–117], aim at eliminating the bus voltage harmonic ripple with hardware modifications. As a consequence, the second-order harmonic currents in DER converters are also reduced. It is worth mentioning that nonlinear control approaches are adopted in [116, 117]. While these nonlinear methods rely on the prior knowledge of the controlled system to obtain high performance, the linear ones, including the methods proposed in this paper, show the favorable feature of being more tolerant to the varying conditions that are typical of the addressed microgrid scenario. Moreover, without additional components, H-bridge rectifiers integrated with the active power decoupling function were proposed recently [118, 119]. In this converter, one half-bridge is responsible for active power transmission, while the other one is used for power decoupling. This converter serves as a good interface between 380 V DC microgrids and 110 V AC utility grid. However, interfacing with 230 V AC grids, a commonly used voltage level in Europe, would require DC bus voltages higher than 380 V (e.g., 500 V). Differently, techniques at the converters control level, which are addressed herein, allow to selectively mitigate harmonic currents at the resource side of DER converters in a flexible and effective way without requiring higher DC bus voltages or hardware modifications [120].

In [121], knowing the bus capacitance and the GIC output power, the bus voltage second-order ripple is calculated and then compensated by adding a ripple cancellation term on the duty cycle of the GIC. However, this method hardly supports the plug-and-play connection of converters, which makes the DC bus capacitance to vary unpredictably.

Second-order harmonic current suppression can be attained also by shaping the converters output impedance to be high at $2\omega_g$. To this end, the bandwidth of the output voltage loops can be set well below $2\omega_g$ [122], which though sacrifices the dynamic performance of the DER converters. In [123] the mean value of the bus voltage, rather than its instantaneous value, is calculated and taken as the feedback signal to eliminate the second-order harmonic in the voltage loops. For the same purpose, a notch filter based on the second-order generalized integrator (SOGI) is added in the output voltage feedback path in [124]. In these approaches, frequency-adaptive notch filters can be used to obtain more precise performances under fluctuating line frequency [125, 126], and multiple notch filters can be adopted to cope with multiple harmonic frequencies [127]. However, since notch filters introduce $-\pi/2$ phase lag around the characteristic frequency (i.e., $2\omega_g$), the bandwidth of the voltage loop is limited to be below $2\omega_g$ to avoid instability. In order to improve the dynamic performance of converters with low-bandwidth (less than $2\omega_g$) voltage loops, a load current feedforward path consisting of a notch filter is adopted in [128], and a virtual impedance in parallel with the DC bus capacitor is introduced in [120]. Both the load current feedforward method and the parallel virtual impedance method should be calculated based on the inverse of the converters transfer functions, which complicates the design.

In this chapter, four different methods for second-order harmonic currents reduction are discussed herein: adoption of a notch filter, a modified notch filter, a resonant regulator, and a modified resonant regulator. The implementations called *modified notch filter* and *modified resonant regulator* are proposed herein. The modified schemes can be simply inserted into high-bandwidth loops, without specific concerns about stability. Hence, the proposed approaches give an efficient way to tackle the second-order harmonic current issue and to achieve good dynamic performance, concurrently.

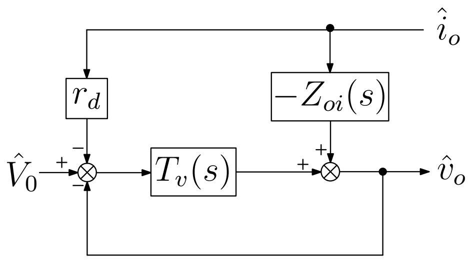


Figure 3-1: Equivalent transformation of the small-signal model shown in Fig.. 2-4.

3.2 Second-order harmonic current issue

For a generic droop-controlled DC-DC DER converter, its control scheme and small-signal model have been illustrated in Fig. 2-3 and Fig. 2-4, respectively. The small-signal model can be also restructured, as shown in Fig. 3-1. $T_v(s)$ is the open-loop transfer function of the voltage loop, and it is expressed as (2.9). $Z_{oi}(s)$ is the output impedance with only the current loop closed:

$$Z_{oi}(s) = -\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{i}_L^*=0} = -\left[G_{vi_o}(s) + \frac{G_{ii_o}(s)G_{vi}(s)}{1+T_i(s)}\right] \tag{3.1}$$

where $T_i(s)$ is the open-loop transfer function of the inductor current loop, and it is expressed as (2.7). Then, the output impedance with all the three loops closed $Z_{oc}(s)$, which is also given as (2.11), can be expressed as:

$$Z_{oc}(s) = -\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{V}_0=0} = \frac{Z_{oi}(s) + r_d \cdot T_v(s)}{1+T_v(s)} \tag{3.2}$$

Further, the output impedance excluding the output capacitance, $Z_o(s)$, can be derived by decoupling the output capacitance $1/sC_o$ from $Z_{oc}(s)$:

$$Z_o(s) = Z_{oc}(s)/\left[1 - sC_oZ_{oc}(s)\right] \tag{3.3}$$

To numerically present the issue of second-order harmonic current, the boost DER converter shown in Fig. 2-7 is taken as an example. The system parameters are: $V_{in} = 200\,\mathrm{V}$, $V_{bus} = 380\,\mathrm{V}$, $L = 0.5\,\mathrm{mH}$, $C_o = 220\,\mu\mathrm{F}$, $r_d = 0.76\,\mathrm{V/A}$. Fig. 3-2 shows the bode diagram of $Z_o(s)$. As can be seen, $|Z_o(s)|$ is about $4.8\,\mathrm{dB}$ (i.e., $1.7\,\Omega$) at twice the line fre-

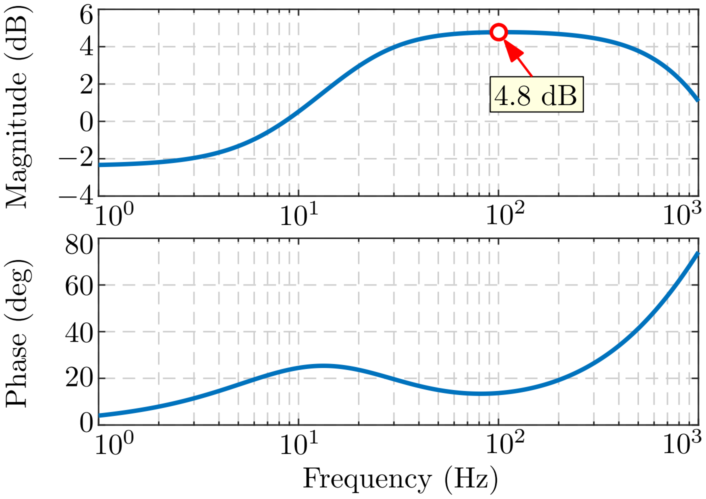


Figure 3-2: Bode diagram of the closed-loop output impedance $Z_o(s)$ in (3.3), excluding the output capacitance.

quency $2\omega_g$ (i.e., $100\,\mathrm{Hz}$), which means that even a relatively small second-order harmonic voltage ripple would lead to a large associated current flowing at the resource side of the converter. Actually, the output impedance at $2\omega_g$ can be as low as r_d, which would produce a higher second-order harmonic current.

3.3 Adoption of a notch filter

To mitigate the second-order harmonic current, a common way is to decrease the voltage loop gain at twice the line frequency, that is, to reduce the second-order fluctuations in the current reference i_L^*. A notch filter $G_{\mathrm{nf}}(s)$ can be adopted to this purpose:

$$G_{\mathrm{nf}}(s) = \frac{(s/\omega_c)^2 + 2\xi_1 \cdot s/\omega_c + 1}{(s/\omega_c)^2 + 2\xi_2 \cdot s/\omega_c + 1} \tag{3.4}$$

where ω_c is the center frequency of the notch, ξ_1 and ξ_2 are two coefficients related to the filter bandwidth and the notch depth. With the decrease of the ratio ξ_1/ξ_2, the notch at ω_c gets deeper (i.e., higher attenuation). The filter bandwidth becomes wider as ξ_1 decreases or ξ_2 increases. An instance of $G_{\mathrm{nf}}(s)$ is displayed in Fig. 3-3. The bandwidth of this notch filter is $100\,\mathrm{Hz}$ and the notch depth is $-60\,\mathrm{dB}$. By inserting $G_{\mathrm{nf}}(s)$ into the forward path of the voltage loop, that is, in series with the voltage regulator $G_v(s)$, the voltage loop gain at

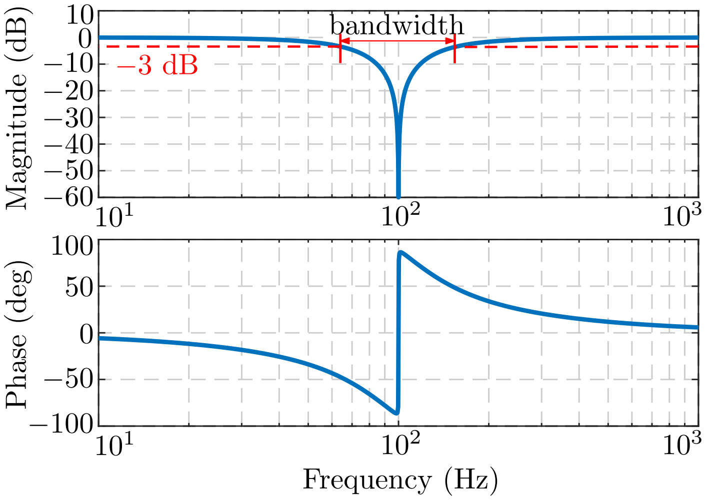


Figure 3-3: Bode diagram of a representative notch filter $G_{\mathrm{nf}}(s)$ in (3.4) using $\omega_c = 2\pi \cdot 100\,\mathrm{rad/s}$, $\xi_1 = 5.0 \times 10^{-4}$, and $\xi_2 = 5.0 \times 10^{-1}$.

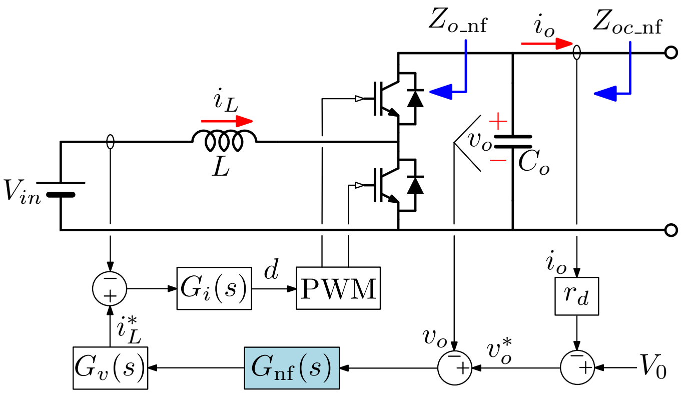


Figure 3-4: Control scheme of the second-order harmonic current provision by adopting a notch filter $G_{\mathrm{nf}}(s)$ [defined in (3.4)]. $G_{\mathrm{nf}}(s)$ can be replaced by the modified notch filter $G_{\mathrm{mnf}}(s)$ [defined in (3.9)].

ω_c can be reduced to a low level and i_L^* is free from the ripple at ω_c. The resulting control scheme adopting a notch filter is displayed in Fig. 3-4.

3.3.1 Output impedance

According to Fig. 3-4, the converter output impedance $Z_{oc\_\mathrm{nf}}(s)$ with $G_{\mathrm{nf}}(s)$ inserted is:

$$Z_{oc\_\mathrm{nf}}(s) = \frac{Z_{oi}(s) + r_d \cdot T_{v\_\mathrm{nf}}(s)}{1 + T_{v\_\mathrm{nf}}(s)} \tag{3.5}$$

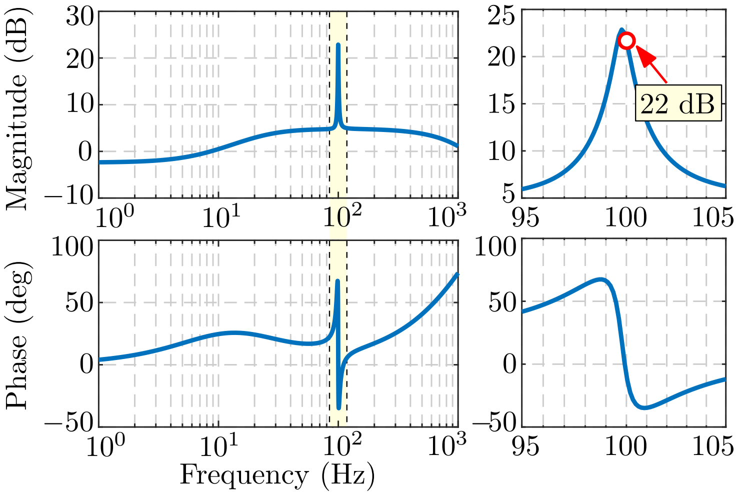


Figure 3-5: Bode diagram of the output impedance $Z_{o\_\mathrm{nf}}(s)$ [see (3.8)] resulting by adopting $G_{\mathrm{nf}}(s)$.

where $T_{v\_\mathrm{nf}}(s)$ is the open-loop transfer function of the voltage loop with $G_{\mathrm{nf}}(s)$ inserted:

$$T_{v\_\mathrm{nf}}(s) = T_v(s) \cdot G_{\mathrm{nf}}(s) \tag{3.6}$$

As $G_{\mathrm{nf}}(s)$ shows a high attenuation at $2\omega_g$, $|T_{v\_\mathrm{nf}}(j2\omega_g)|$ is small. Hence, $Z_{oc\_\mathrm{nf}}(j2\omega_g)$ can be approximated as:

$$Z_{oc\_\mathrm{nf}}(j2\omega_g) \approx Z_{oi}(j2\omega_g) \tag{3.7}$$

and $Z_{o\_\mathrm{nf}}(s)$ can be expressed as:

$$Z_{o\_\mathrm{nf}}(s) = Z_{oc\_\mathrm{nf}}(s) / \left[1 - sC_o Z_{oc\_\mathrm{nf}}(s)\right] \tag{3.8}$$

The bode diagram of $Z_{o\_\mathrm{nf}}(s)$ is displayed in Fig. 3-5. The notch filter $G_{\mathrm{nf}}(s)$ used here has a bandwidth of $10\,\mathrm{Hz}$ and a notch depth of $-60\,\mathrm{dB}$, with $\omega_c = 2\pi \cdot 100\,\mathrm{rad/s}$, $\xi_1 = 5.0 \times 10^{-5}$, and $\xi_2 = 5.0 \times 10^{-2}$. It can be noticed that $Z_{o\_\mathrm{nf}}(j2\omega_g)$ has a magnitude of $22\,\mathrm{dB}$ (i.e., $12.6\,\Omega$), which is 7.4 times $Z_o(j2\omega_g)$. Consequently, with $G_{\mathrm{nf}}(s)$, the second-order harmonic current is notably reduced.

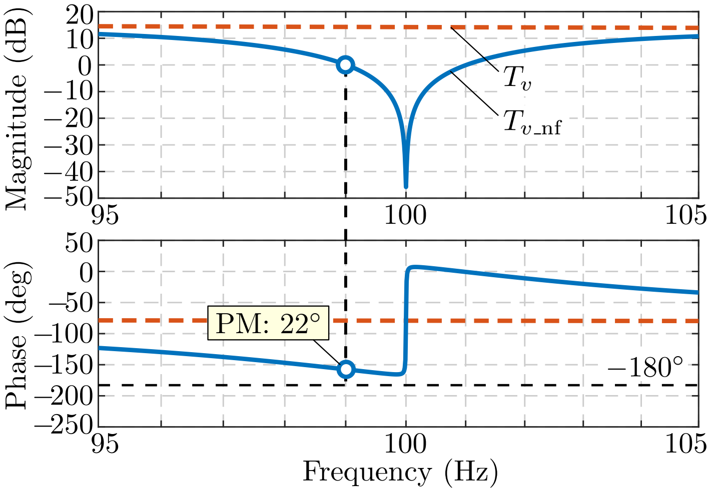


Figure 3-6: Impact of $G_{\mathrm{nf}}(s)$ on the stability: bode diagram of the open-loop transfer function of the voltage loop, with and without adopting $G_{\mathrm{nf}}(s)$.

3.3.2 Stability analysis

It should be noted that if the crossover frequency of the voltage loop is above $2\omega_g$, which is typically the case in practice, $G_{\mathrm{nf}}(s)$ brings two additional zero crossings: one below $2\omega_g$, the other above $2\omega_g$. Notably, $G_{\mathrm{nf}}(s)$ introduces large phase lags at frequencies below $2\omega_g$, reducing the phase margin at the corresponding zero crossing and weakening significantly the stability of the voltage loop. Fig. 3-6 shows the bode diagram of the open-loop transfer functions $T_{v\_\mathrm{nf}}(s)$ and $T_v(s)$ of the voltage loop. Without $G_{\mathrm{nf}}(s)$, $T_v(s)$ has a magnitude of $14\,\mathrm{dB}$ and a phase of -80° at $100\,\mathrm{Hz}$. By employing $G_{\mathrm{nf}}(s)$, $T_{v\_\mathrm{nf}}(s)$ has two additional zero crossing points around $100\,\mathrm{Hz}$. At the zero crossing below $100\,\mathrm{Hz}$, the phase margin drastically reduces to 22°. To maintain the system stability, the voltage control bandwidth should be redesigned to fall below $100\,\mathrm{Hz}$, resulting in a slow dynamic response.

3.4 Adoption of a modified notch filter

In order to concurrently achieve fast dynamic response and good stability margin, a modified notch filter $G_{\mathrm{mnf}}(s)$ is proposed herein in place of $G_{\mathrm{nf}}(s)$ in Fig. 3-4:

$$G_{\mathrm{mnf}}(s) = \frac{1}{\alpha^2}\frac{(s/\omega_c)^2 + 2\xi_1 \cdot s/\omega_c + 1}{\left[s/(\alpha\omega_c)\right]^2 + 2\xi_2 \cdot s/(\alpha\omega_c) + 1} \tag{3.9}$$

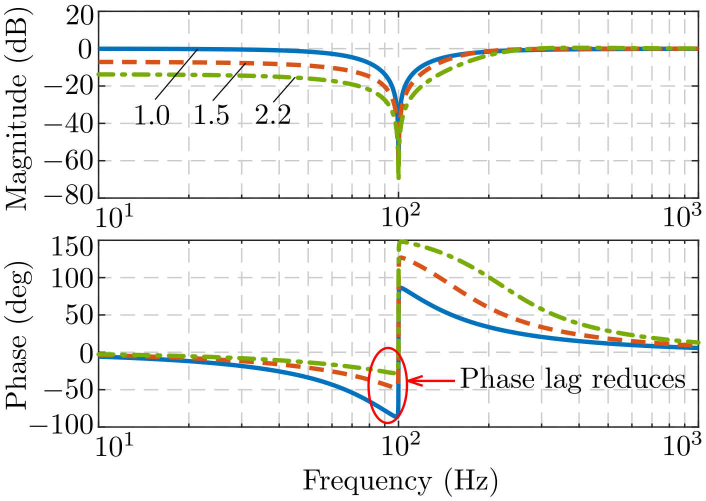


Figure 3-7: Bode diagram of the modified notch filter $G_{\mathrm{mnf}}(s)$ in (3.9) with different α, using $\omega_c = 2\pi \cdot 100\,\mathrm{rad/s}$, $\xi_1 = 5.0 \times 10^{-4}$, and $\xi_2 = 5.0 \times 10^{-1}$.

where α, which is larger than 1, is the deviation factor; if $\alpha = 1$, $G_{\mathrm{mnf}}(s)$ corresponds to $G_{\mathrm{nf}}(s)$. The bode diagram of $G_{\mathrm{mnf}}(s)$ with different values of α is displayed in Fig. 3-7. By increasing α, the two poles of $G_{\mathrm{mnf}}(s)$ move to higher frequencies. Consequently, the phase lag below ω_c reduces, while keeping a high attenuation at ω_c. The term $1/\alpha^2$ is used to correct the gains to 1 at high frequency, so that $G_{\mathrm{mnf}}(s)$ does not change the original crossover frequency of the voltage loop. However, by doing so, the static gain of $G_{\mathrm{mnf}}(s)$ is less than 1.

3.4.1 Stability improvement

To investigate the effect of $G_{\mathrm{mnf}}(s)$ on the converter stability, the open-loop transfer function $T_{v\_\mathrm{mnf}}(s)$ of the voltage loop with $G_{\mathrm{mnf}}(s)$ inserted is considered:

$$T_{v\_\mathrm{mnf}}(s) = T_v(s) \cdot G_{\mathrm{mnf}}(s) \tag{3.10}$$

The bode diagram of $T_{v\_\mathrm{mnf}}(s)$ is displayed in Fig. 3-8. The $G_{\mathrm{mnf}}(s)$ reported here have different α, but the other parameters are kept constant (i.e., $\omega_c = 2\pi \cdot 100\,\mathrm{rad/s}$, $\xi_1 = 5.0 \times 10^{-5}$, and $\xi_2 = 5.0 \times 10^{-2}$). Remarkably, the phase margin rises from 22° to 59°, with a light increase of α from 1.00 to 1.04, showing a significant stability improvement. Since the instability is avoided, the voltage control bandwidth can be kept at the original

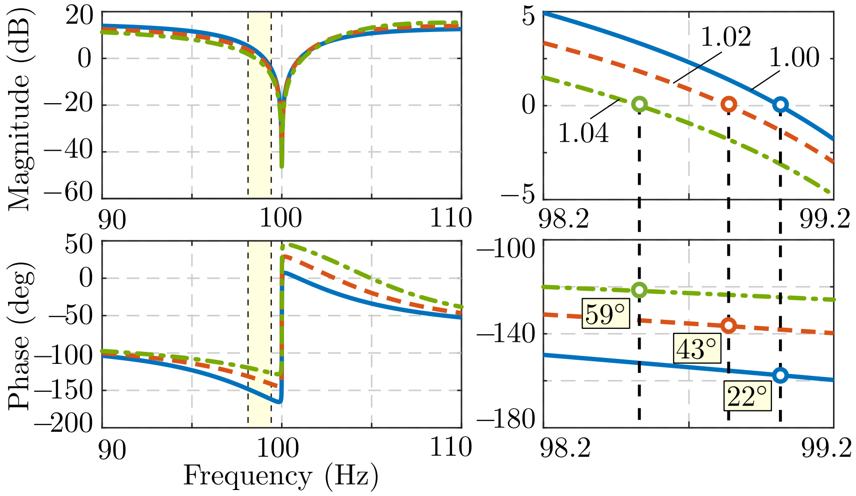


Figure 3-8: Stability improvement by using $G_{\mathrm{mnf}}(s)$ in (3.9) with different α: bode diagram of the open-loop transfer function $T_{v\_\mathrm{mnf}}(s)$ of the voltage loop.

value, that is, $650\,\mathrm{Hz}$. Compared to the case with the traditional notch filter, the converter dynamic response is much faster.

It is worth observing that the phase improvement induced by $G_{\mathrm{mnf}}(s)$ is determined only by the filter parameters, and it is not influenced by physical system variations. Clearly, to always ensure an adequate phase margin also in the presence of a wide range of operating conditions, $G_{\mathrm{mnf}}(s)$ should be designed by referring to the operation point showing the worst (i.e., minimum) phase at $2\omega_g$.

3.4.2 Output impedance

By replacing $G_{\mathrm{nf}}(s)$ with $G_{\mathrm{mnf}}(s)$ in Fig. 3-4, the output impedance $Z_{oc\_\mathrm{mnf}}(s)$ can be expressed as:

$$Z_{oc\_\mathrm{mnf}}(s) = \frac{Z_{oi}(s) + r_d \cdot T_{v\_\mathrm{mnf}}(s)}{1 + T_{v\_\mathrm{mnf}}(s)} \tag{3.11}$$

$Z_{o\_\mathrm{mnf}}(s)$ can be calculated by decoupling $1/sC_o$ from $Z_{oc\_\mathrm{mnf}}(s)$:

$$Z_{o\_\mathrm{mnf}}(s) = Z_{oc\_\mathrm{mnf}}(s) / \left[1 - sC_o Z_{oc\_\mathrm{mnf}}(s)\right] \tag{3.12}$$

The bode diagram of $Z_{o\_\mathrm{mnf}}(s)$ is shown in Fig. 3-9. $G_{\mathrm{mnf}}(s)$ adopted here uses $\alpha = 1.04$. Since $G_{\mathrm{mnf}}(s)$ also brings $|Z_{o\_\mathrm{mnf}}(j2\omega_g)|$ to $22\,\mathrm{dB}$ (i.e., $12.6\,\Omega$), it has the same

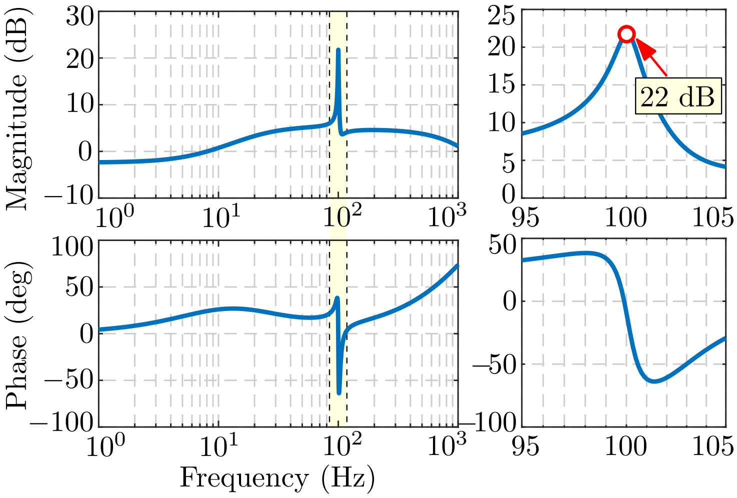


Figure 3-9: Bode diagram of the output impedance $Z_{o\_\mathrm{mnf}}(s)$ [see (3.12)] resulting by adopting $G_{\mathrm{mnf}}(s)$.

performance as $G_{\mathrm{nf}}(s)$ (see Fig. 3-5) in rejecting second-order harmonic current.

3.4.3 Filter design

A modified notch filter $G_{\mathrm{mnf}}(s)$ has four parameters: the center frequency ω_c, the deviation factor α, and the two coefficients ξ_1 and ξ_2. The first three parameters should be designed based on required attenuation and filter bandwidth. Particularly, in practical applications, the frequency of the second-order harmonic voltage depends on the, possibly varying, upstream grid frequency; therefore, a technique to adapt ω_c to the actual frequency of the second-order harmonic may be required. This adaptive feature can be attained by, for example, employing a phase locked loop to continuously monitor the bus voltage ripple frequency and changing ω_c accordingly. The deviation factor α is introduced in the proposed technique, and its selection criterion is discussed below.

The deviation factor α is utilized to increase the phase margin of the voltage loop. As compared to $G_{\mathrm{nf}}(s)$, $G_{\mathrm{mnf}}(s)$ gives a high phase gain at $2\omega_g$, and the phase gain reduces as the frequency strays from $2\omega_g$ (see Fig. 3-7). In different application cases, voltage loops with $G_{\mathrm{mnf}}(s)$ inserted may have different crossover frequencies around $2\omega_g$, so the phase margin improvements brought by $G_{\mathrm{mnf}}(s)$ differ from case to case. Fortunately, as long as the implemented $G_{\mathrm{mnf}}(s)$ has a narrow notch, the crossover frequency locates in the vicinity of $2\omega_g$ (see Fig. 3-8). In this case, the phase gain of $G_{\mathrm{mnf}}(s)$ at the crossover frequency is

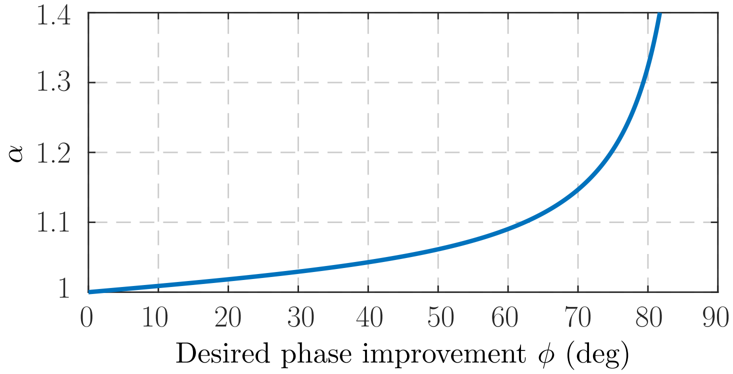


Figure 3-10: Relationship (3.14) between the desired phase improvement ϕ and α, using $\xi_2 = 5.0 \times 10^{-2}$.

approximately equal to the phase gain at $2\omega_g$, that is, $\angle G_{\mathrm{mnf}}(j2\omega_g)$. This estimation makes the selection of α independent from the specific application case, simplifying the design procedure. The phase gain of $G_{\mathrm{mnf}}(s)$ at $2\omega_g$ can be calculated as:

$$\angle G_{\mathrm{mnf}}(j2\omega_g) = \frac{\pi}{2} - \arctan\left(\frac{2\alpha\xi_2}{\alpha^2 - 1}\right) \tag{3.13}$$

The value of α for a desired phase gain ϕ ($0 < \phi < \pi/2$) is:

$$\alpha = \left(\xi_2 + \sqrt{{\xi_2}^2 + \tan^2\left(\frac{\pi}{2} - \phi\right)}\right) \Big/ \tan\left(\frac{\pi}{2} - \phi\right) \tag{3.14}$$

Fig. 3-10 displays the relationship between ϕ and α. Notably, the larger the required phase improvement, the larger the required value of α.

As an example, let us consider the choice of α to reach a phase margin of $60°$ in the case of Fig. 3-6, where the phase margin is displayed to decrease to $22°$ after inserting the notch filter. Being the necessary phase lead equal to $38°$, by referring to (3.14) or Fig. 3-10, it is possible to find that the desired phase margin improvement can be achieved if α is set to 1.04. In Fig. 3-8 the final result by employing a modified notch filter with $\alpha = 1.04$, showing an obtained phase margin of $59°$.

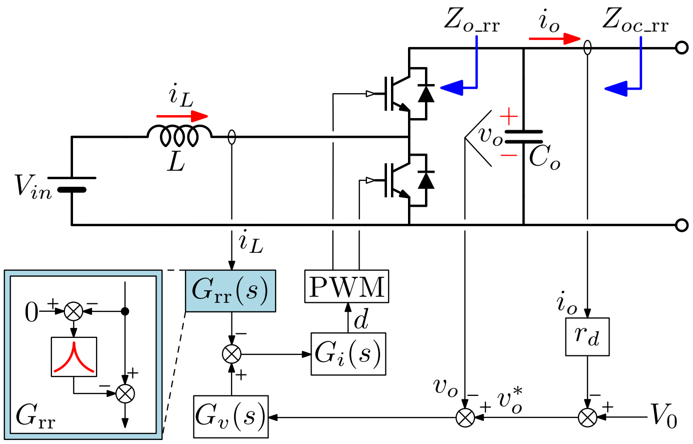


Figure 3-11: Second-order harmonic current provision by adopting a resonant regulator $G_{\mathrm{rr}}(s)$ [defined in (3.15)]. $G_{\mathrm{rr}}(s)$ can be replaced by the modified resonant regulator $G_{\mathrm{mrr}}(s)$ [defined in (3.20)].

3.5 Adoption of a resonant regulator

An alternative way to suppress the second-order harmonic current is to actively regulate it to a low level. The scheme in Fig. 3-11 gives a representation of this approach. $G_{\mathrm{rr}}(s)$ is a resonant regulator featuring a high gain at $2\omega_g$. $G_{\mathrm{rr}}(s)$ amplifies the error between 0 and i_l at $2\omega_g$, and its output is used to modify the inductor current reference i_{ref}. The higher the gain of $G_{\mathrm{rr}}(s)$ at $2\omega_g$, the smaller the second-order harmonic current. Particularly, if $G_{\mathrm{rr}}(s)$ has infinite gain at $2\omega_g$, the second-order harmonic current can be totally compensated. An instance of $G_{\mathrm{rr}}(s)$ is expressed as:

$$G_{\mathrm{rr}}(s) = \frac{\lambda_1 \cdot s/\omega_r}{(s/\omega_r)^2 + \lambda_2 \cdot s/\omega_r + 1} + 1 \tag{3.15}$$

where ω_r is the resonant frequency, λ_1 and λ_2 are two coefficients. The bode diagram of an example $G_{\mathrm{rr}}(s)$ is displayed in Fig. 3-12. A peak of $60\,\mathrm{dB}$ can be found at ω_r.

3.5.1 Output impedance

According to Fig. 3-11, the output impedance $Z_{oc\_\mathrm{rr}}(s)$ is calculated as:

$$Z_{oc\_\mathrm{rr}}(s) = \frac{-G_{vi_o}(s) - G_{ii_o}(s)G_{vi}(s)/[1 + T_{i\_\mathrm{rr}}(s)] + r_d T_{v\_\mathrm{rr}}(s)}{1 + T_{v\_\mathrm{rr}}(s)} \tag{3.16}$$

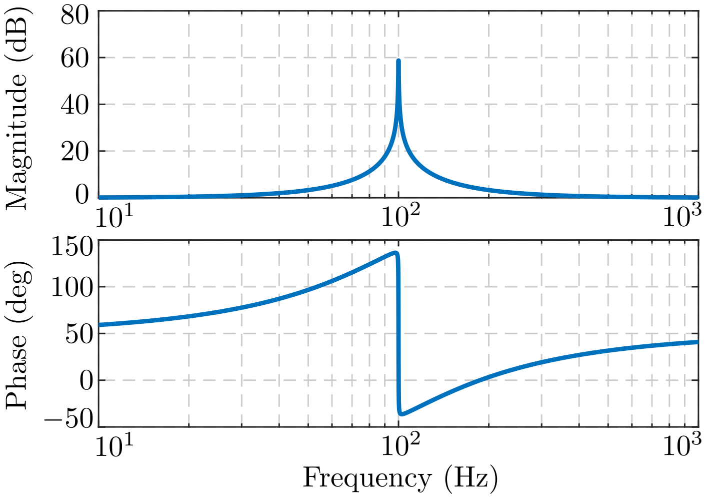


Figure 3-12: Bode diagram of the resonant regulator $G_{\mathrm{rr}}(s)$ in (3.15) using $\omega_r = 2\pi \cdot 100\,\mathrm{rad/s}$, $\lambda_1 = 1.6$, and $\lambda_2 = 1.6 \times 10^{-3}$.

where $T_{i\_\mathrm{rr}}(s)$ and $T_{v\_\mathrm{rr}}(s)$ are the open-loop transfer functions of the current loop and the voltage loop, respectively, with $G_{\mathrm{rr}}(s)$ adopted. They can be expressed as:

$$T_{i\_\mathrm{rr}}(s) = T_i(s)[1 + G_{\mathrm{rr}}(s)] \tag{3.17}$$

$$T_{v\_\mathrm{rr}}(s) = G_v(s) \cdot \frac{T_{i\_\mathrm{rr}}(s)}{[1 + T_{i\_\mathrm{rr}}(s)] \cdot [1 + G_{\mathrm{rr}}(s)]} \cdot G_{vi}(s) \tag{3.18}$$

Then, $Z_{o\_\mathrm{rr}}(s)$ can be derived by excluding the output capacitance.

$$Z_{o\_\mathrm{rr}}(s) = Z_{oc\_\mathrm{rr}}(s) / \left[1 - sC_o Z_{oc\_\mathrm{rr}}(s)\right] \tag{3.19}$$

Fig. 3-13 shows the bode diagram of $Z_{o\_\mathrm{rr}}(s)$. The $G_{\mathrm{rr}}(s)$ employed here uses $\omega_r = 2\pi \cdot 100\,\mathrm{rad/s}$, $\lambda_1 = 1.6 \times 10^{-1}$, and $\lambda_2 = 1.6 \times 10^{-4}$. At $2\omega_g$, $Z_{o\_\mathrm{rr}}(s)$ has a magnitude of $29\,\mathrm{dB}$ (i.e., $28.2\,\Omega$), indicating a high rejection of the second-order harmonic current ripple in the inductor current.

3.5.2 Stability analysis

Since $G_{\mathrm{rr}}(s)$ has a large magnitude at $2\omega_g$, $T_{v\_\mathrm{rr}}(s)$ presents a notch at $2\omega_g$ [see (3.18)]. In such a case, $G_{\mathrm{rr}}(s)$ gives rise to a stability problem. The bode diagram of $T_{v\_\mathrm{rr}}(s)$ is

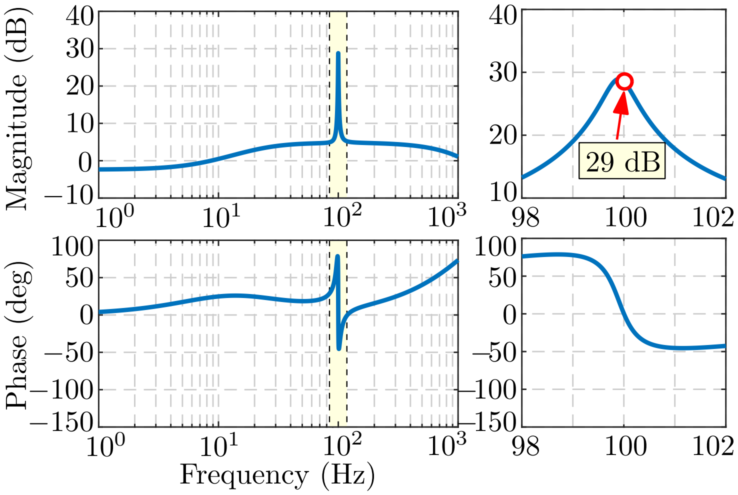


Figure 3-13: Bode diagram of the output impedance $Z_{o\_\mathrm{rr}}(s)$ resulting by adopting $G\_\mathrm{rr}(s)$.

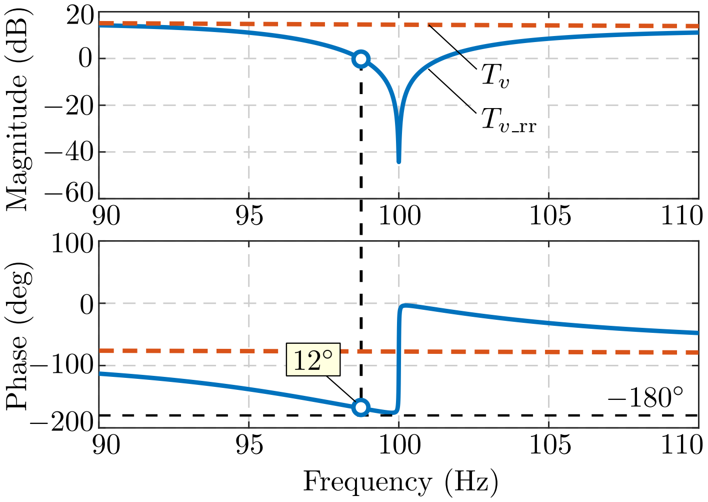


Figure 3-14: Impact of $G_{\mathrm{rr}}(s)$ on voltage loop stability: bode diagram of the open-loop transfer function of the voltage loop, with and without using $G_{\mathrm{rr}}(s)$.

depicted in Fig. 3-14, where the adopted $G_{\mathrm{rr}}(s)$ uses $\omega_r = 2\pi \cdot 100\,\mathrm{rad/s}$, $\lambda_1 = 1.6 \times 10^{-1}$, and $\lambda_2 = 1.6 \times 10^{-4}$. As can be seen, $T_{v\_\mathrm{rr}}(s)$ has two additional zero crossing points around $2\omega_g$. For the one at the frequency below $2\omega_g$, the phase margin is only $12\,^\circ$. Hence, the converter stability worsens considerably after inserting $G_{\mathrm{rr}}(s)$.

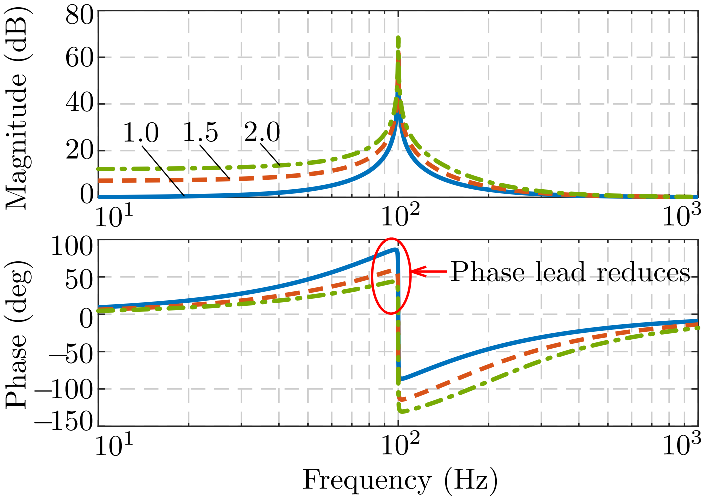


Figure 3-15: Bode diagram of the modified resonant regulator $G_{\text{mrr}}(s)$ with different β, using $\omega_r = 2\pi \cdot 100\,\text{rad/s}$, $\lambda_1 = 1.6$, and $\lambda_2 = 1.6 \times 10^{-3}$.

3.6 Adoption of a modified resonant regulator

To improve the stability margin, a modified resonant regulator $G_{\text{mrr}}(s)$ is proposed to replace the resonant regulator $G_{\text{rr}}(s)$ in Fig. 3-11. $G_{\text{mrr}}(s)$ is expressed as below:

$$G_{\text{mrr}}(s) = \beta^2 \frac{\left[s/(\beta\omega_r)\right]^2 + (\lambda_1 + \lambda_2) \cdot s/(\beta\omega_r) + 1}{(s/\omega_r)^2 + \lambda_2 \cdot s/\omega_r + 1} \tag{3.20}$$

where β is the deviation factor and is required to be larger than 1. It can be found that $G_{\text{mrr}}(s)$ is constructed in a way similar to $G_{\text{mnf}}(s)$. In the case that $\beta = 1$, $G_{\text{mrr}}(s)$ is equivalent to $(1+G_{rr}(s))$. The bode diagram of $G_{\text{mrr}}(s)$ with different β is shown in Fig 3-15. The zeros of $G_{\text{mrr}}(s)$ are moving to high frequencies by increasing β, so that the phase lead below $2\omega_g$ is reduced. To keep the original crossover frequencies of the current loop and the voltage loop, the gains at high frequencies are set to 1 by the term β^2. Moreover, since the static feedback gain of the current loop is β^2 instead of 1, current limitations, that is, the output of voltage regulator $G_v(s)$, should be changed correspondingly.

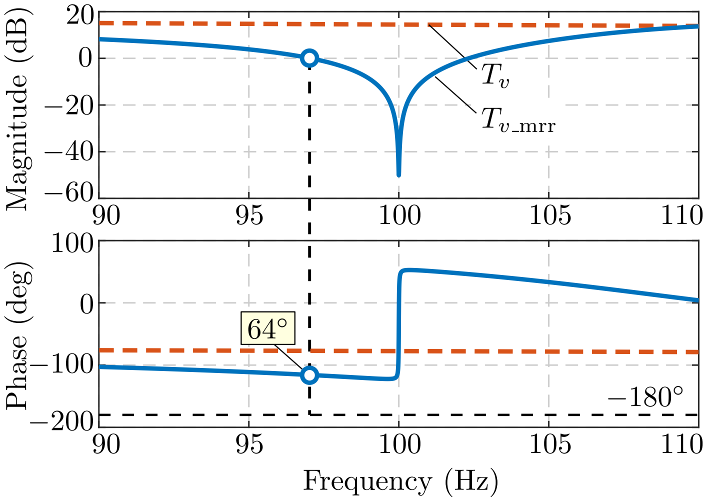


Figure 3-16: Stability improvement by using $G_{\mathrm{mrr}}(s)$ in (3.20): bode diagram of the open-loop transfer function $T_{v\_\mathrm{mrr}}(s)$ of the voltage loop.

3.6.1 Stability improvement

With $G_{\mathrm{mrr}}(s)$ adopted, the open-loop transfer function of voltage loop, $T_{v\_\mathrm{mrr}}(s)$, can be expressed as

$$T_{v\_\mathrm{mrr}}(s) = G_v(s) \cdot \frac{T_{i\_\mathrm{mrr}}(s)}{[1 + T_{i\_\mathrm{mrr}}(s)] \cdot G_{\mathrm{mrr}}(s)} \cdot G_{vi}(s) \tag{3.21}$$

where $T_{i\_\mathrm{mrr}}(s)$ is the open-loop transfer function of the current loop

$$T_{i\_\mathrm{mrr}}(s) = T_i(s) \cdot G_{\mathrm{mrr}}(s) \tag{3.22}$$

To evaluate the stability improvement brought by $G_{\mathrm{mrr}}(s)$, the bode diagram of $T_{v\_\mathrm{mrr}}(s)$ is shown in Fig. 3-16. The parameters of $G_{\mathrm{mrr}}(s)$ are: $\omega_r = 2\pi \cdot 100\,\mathrm{rad/s}$, $\lambda_1 = 1.6 \times 10^{-1}$, $\lambda_2 = 1.6 \times 10^{-4}$, and $\beta = 1.12$. It can be seen that the phase margin and, consequently, the system stability is significantly improved by adopting $G_{\mathrm{mrr}}(s)$.

3.6.2 Output impedance

The output impedance $Z_{oc\_\mathrm{mrr}}(s)$ can be further derived as:

$$Z_{oc\_\mathrm{mrr}}(s) = \frac{-G_{vi_o}(s) - G_{ii_o}(s)G_{vi}(s)/[1 + T_{i\_\mathrm{mrr}}(s)] + r_d T_{v\_\mathrm{mrr}}(s)}{1 + T_{v\_\mathrm{mrr}}(s)} \tag{3.23}$$

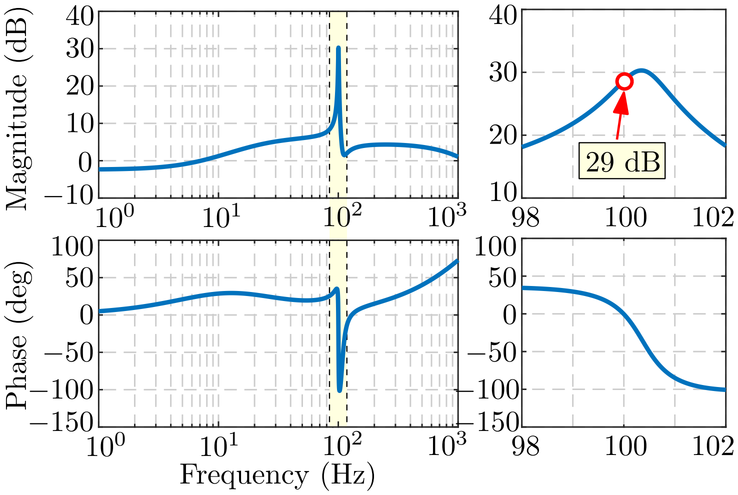


Figure 3-17: Bode diagram of the output impedance $Z_{o\_\mathrm{mrr}}(s)$ resulting by adopting $G_{\mathrm{mrr}}(s)$.

The output impedance without considering the output capacitance, $Z_{o\_\mathrm{mrr}}(s)$, can be expressed as:

$$Z_{o\_\mathrm{mrr}}(s) = Z_{oc\_\mathrm{mrr}}(s)/\left[1 - sC_o Z_{oc\_\mathrm{mrr}}(s)\right] \tag{3.24}$$

Fig. 3-17 depicts the bode diagram of $Z_{o\_\mathrm{mrr}}(s)$. $G_{\mathrm{mrr}}(s)$ adopted here uses $\omega_r = 2\pi \cdot 100\,\mathrm{rad/s}$, $\lambda_1 = 1.6 \times 10^{-1}$, $\lambda_2 = 1.6 \times 10^{-4}$, and $\beta = 1.12$. Similar to the result of using $G_{\mathrm{mrr}}(s)$, the magnitude at $2\omega_g$ is as high as $29\,\mathrm{dB}$, so the second-order harmonic current ripple in i_L is well removed.

3.6.3 Regulator design

It can be observed from (3.20) and (3.9) that $G_{\mathrm{mrr}}(s)$ resembles $G_{\mathrm{mnf}}(s)$ in terms of structure. Therefore, the design methodology of $G_{\mathrm{mnf}}(s)$ described in Sec. 3.4.3 can be adopted also to $G_{\mathrm{mrr}}(s)$. Since β is used to enhance the voltage loop stability, β should be chosen on the basis of the desired phase margin improvement. Note that $G_{\mathrm{mrr}}(s)$ introduces a phase lag in the current loop, which turns out to be a phase lead in the voltage loop. Actually, the phase margin improvement is roughly equal to the phase gain of $1/G_{\mathrm{mrr}}(j2\omega_g)$. In practice, in order to simplify the design process, β can be selected according to the phase change of

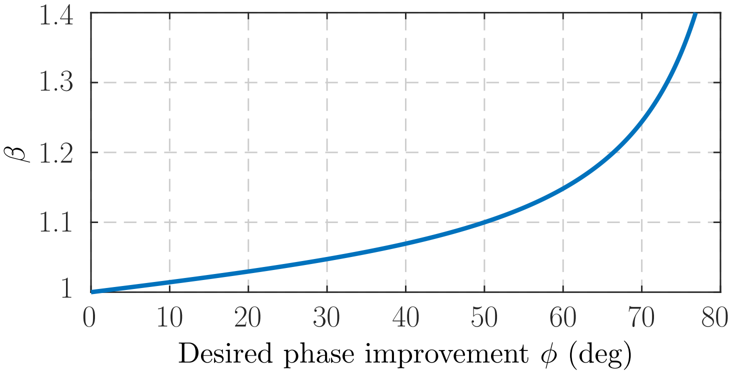


Figure 3-18: Relationship (3.25) between the desired phase improvement ϕ and β, using $\lambda_1 = 1.6 \times 10^{-1}$ and $\lambda_2 = 1.6 \times 10^{-4}$.

$1/G_{\mathrm{mrr}}(j2\omega_g)$, which can be expressed as:

$$\angle\left(1/G_{\mathrm{mrr}}(j2\omega_g)\right) = \frac{\pi}{2} - \arctan\left(\frac{\beta(\lambda_1 + \lambda_2)}{\beta^2 - 1}\right) \tag{3.25}$$

Fig. 3-18 displays the relationship between the desired phase improvement ϕ and β. Notably, for a phase improvement from $0°$ to $50°$, the value of β varies from 1 to 1.1.

3.7 Comparison

Table 3.1 summarizes the performances of the suppression methods analyzed in Section 3.3 to Section 3.6. The methods are compared by considering *i*) effectiveness in suppressing second-order harmonic currents and *ii*) impact on converter stability.

Regarding the reduction of the second-order harmonic current, the notch filter $G_{\mathrm{nf}}(s)$ and the modified notch filter $G_{\mathrm{mnf}}(s)$ are able to remove the second-order ripple in the current reference, whereas the approach using the resonant regulator $G_{\mathrm{rr}}(s)$ and the one employing the modified resonant regulator $G_{\mathrm{mrr}}(s)$ are capable of canceling the second-order ripple in the measured actual current. Hence, $G_{\mathrm{rr}}(s)$ and $G_{\mathrm{mrr}}(s)$ are expected to have better suppression performances than $G_{\mathrm{nf}}(s)$ and $G_{\mathrm{mnf}}(s)$.

Regarding the impact on converter stability, $G_{\mathrm{nf}}(s)$ and $G_{\mathrm{rr}}(s)$ drastically deteriorate the system stability if the voltage loop has a control bandwidth above $2\omega_g$. In contrast, $G_{\mathrm{mnf}}(s)$ and $G_{\mathrm{mrr}}(s)$ allow higher phase margins for the control system and, consequently,

Table 3.1: Comparison of harmonic current suppression methods

Method	Harmonic current suppression	Influence on converter stability
$G_{\mathrm{nf}}(s)$ in (3.4) and Fig. 3-4	good	easily cause instability
$G_{\mathrm{mnf}}(s)$ in (3.9) and Fig. 3-4	good	stability ensured
$G_{\mathrm{rr}}(s)$ in (3.15) and Fig. 3-11	excellent	easily cause instability
$G_{\mathrm{mrr}}(s)$ in (3.20) and Fig. 3-11	excellent	stability ensured

stable voltage control loops with wider control bandwidths.

3.8 Experimental results

The laboratory-scale experimental testbed represented in Fig. 3-19, constituted of one full-bridge GIC and three boost DER converters, is considered to evaluate the methods discussed herein. In fact, this testbed is developed from the configurable prototype shown in Fig. 2-11. Constant power load and resistive load are installed in the prototype. System parameters, unless otherwise specified, are reported in Table 3.2. The total bus capacitance C_b is the sum of all the capacitors connected to the DC bus. The input of the boost converters are connected to a DC source. The GIC and DER converters are controlled in droop, with the same droop coefficient r_d. The DC bus voltage ranges between $360\,\mathrm{V}$ and $400\,\mathrm{V}$. The bandwidths of the inductor current loop and the output voltage loop of DER converters are set to $1\,\mathrm{kHz}$ and $150\,\mathrm{Hz}$, respectively, without including notch filters or resonant controllers. These control parameters are reasonable and aligned with those found in other microgrid implementations [51, 129].

3.8.1 Operation with no harmonic suppression provisions

In this test, the GIC and DER #1 are in operation. A basic droop controller (see Fig. 2-7) is implemented on DER #1, without any second-order harmonic current suppression technique. The experimental result is given in Fig. 3-20. Due to the second-order power generated by the single-phase GIC, there is a second-order bus voltage ripple with a peak-

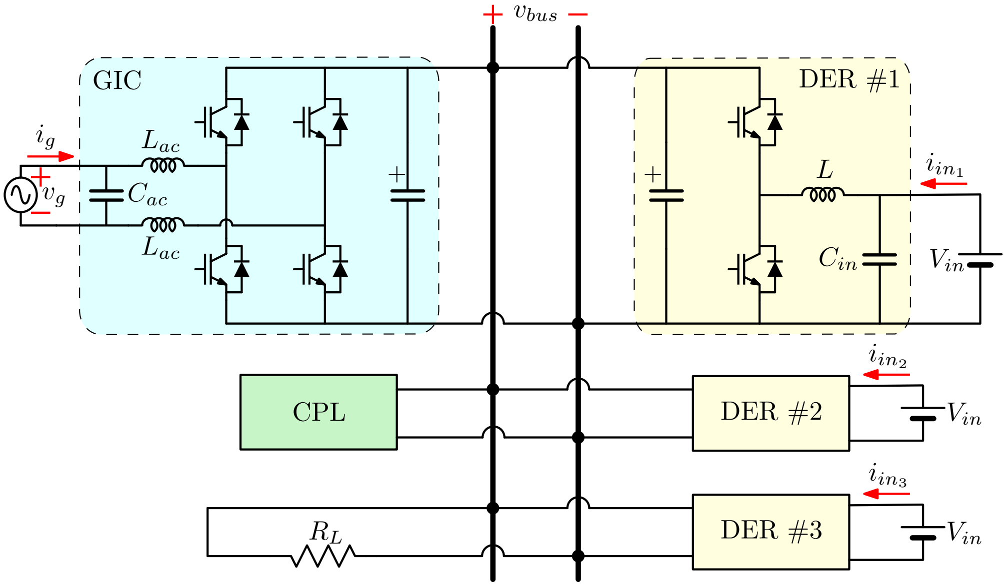


Figure 3-19: Schematic of the experimental testbed with a single-phase grid-connected converter.

Table 3.2: Parameters of the system shown in Fig. 3-19.

Parameter	Symbol	Value
Grid RMS voltage	V_g	$220\,\mathrm{V}$
Grid frequency	f_g	$50\,\mathrm{Hz}$
AC side inductance	L_{ac}	$1.6\,\mathrm{mH}$
AC side capacitance	C_{ac}	$20\,\mu\mathrm{F}$
Nominal bus voltage	V_{bus}	$380\,\mathrm{V}$
Total DC bus capacitance	C_b	$2.2\,\mathrm{mF}$
DER input voltage	V_{in}	$200\,\mathrm{V}$
Boost inductance	L	$1.6\,\mathrm{mH}$
DER input capacitance	C_{in}	$110\,\mu\mathrm{F}$
Switching frequency	f_s	$12.5\,\mathrm{kHz}$
Voltage set point	V_0	$380\,\mathrm{V}$
Droop coefficient	r_d	$0.76\,\mathrm{V/A}$
Current regulator	$G_i(s)$	$0.027 + 5/s$
Voltage regulator	$G_v(s)$	$3.7 + 103/s$

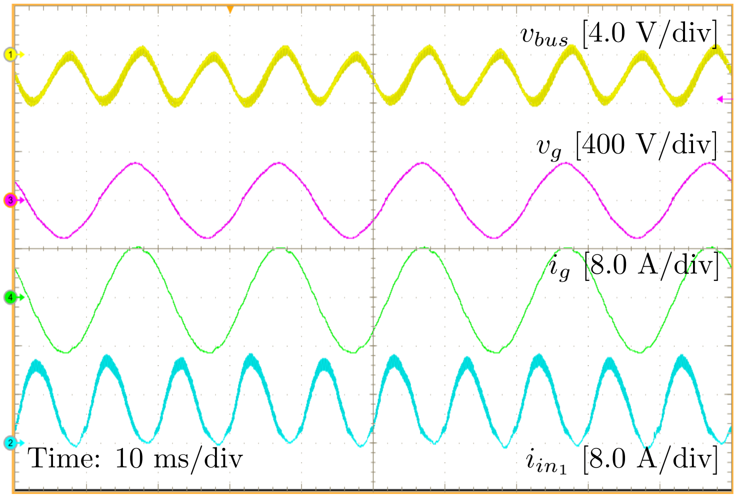


Figure 3-20: Steady-state experimental results without any second-order harmonic current suppression provision. v_{bus} offset: $380\,\mathrm{V}$.

to-peak value of about $4\,\mathrm{V}$. An associated current ripple with amplitude of about $6.7\,\mathrm{A}$ is measured in i_{in_1}. In this case, the second-order harmonic ripple amounts to about 27% the nominal value.

3.8.2 Evaluation of steady-state performances

The steady-state performances of the analyzed suppression methods are now considered.

Notch filters

A notch filter $G_{\mathrm{nf}}(s)$ and a modified notch filter $G_{\mathrm{mnf}}(s)$, with $\omega_c = 2\pi \cdot 100\,\mathrm{rad/s}$, $\xi_1 = 5.0 \times 10^{-5}$, $\xi_2 = 5.0 \times 10^{-2}$, and $\alpha = 1.06$, are included in the controller of DER #1, separately. The obtained results are shown in Fig. 3-21(a) and Fig. 3-21(b), respectively. Although v_{bus} shows a ripple with a peak-to-peak value of $5\,\mathrm{V}$, the corresponding ripple in i_{in_1} is effectively reduced.

Resonant regulators

The steady-state experimental results of the methods adopting the resonant regulator $G_{\mathrm{rr}}(s)$ and the modified resonant regulator $G_{\mathrm{mrr}}(s)$ are presented in Fig. 3-21(c) and Fig. 3-21(d), respectively. The implemented $G_{\mathrm{rr}}(s)$ and $G_{\mathrm{mrr}}(s)$ use $\omega_r = 2\pi \cdot 100\,\mathrm{rad/s}$, $\lambda_1 = 1.6 \times$

Table 3.3: Amplitude of Second-order Harmonic Current Ripple

Methods	No provision	$G_{\mathrm{nf}}(s)$	$G_{\mathrm{mnf}}(s)$	$G_{\mathrm{rr}}(s)$	$G_{\mathrm{mrr}}(s)$
Ripple	$6.75\,\mathrm{A}$	$0.11\,\mathrm{A}$	$0.14\,\mathrm{A}$	$0.03\,\mathrm{A}$	$0.01\,\mathrm{A}$

10^{-1}, $\lambda_2 = 1.6 \times 10^{-4}$, and $\beta = 1.06$. Notably, the second-order harmonic ripple in i_{in_1} is well eliminated.

The second-order harmonic component in the inductor current is also extracted by performing a discrete Fourier transform (DFT) over a time window of $2.5\,\mathrm{s}$ sampled at $200\,\mathrm{kS/s}$. The results are reported in Table 3.3. Compared to the cases using $G_{\mathrm{nf}}(s)$ or $G_{\mathrm{mnf}}(s)$, the current ripple is better rejected by solutions $G_{\mathrm{rr}}(s)$ or $G_{\mathrm{mrr}}(s)$. It should be also noticed that, as the inductor current has a DC component of $5.5\,\mathrm{A}$, the ripple differences between these four methods are relatively small.

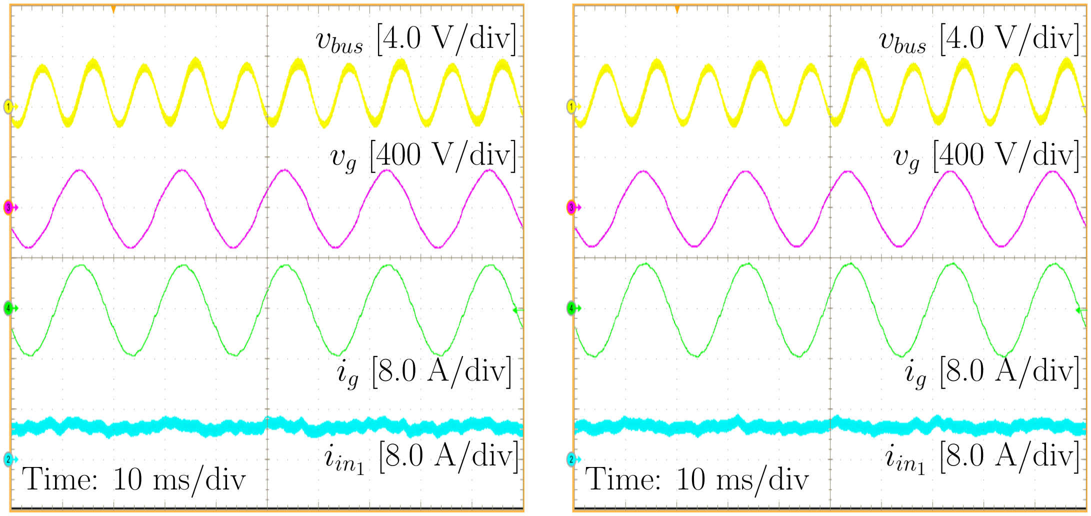
Fig. 3-21(a) to Fig. 3-21(d) display an increase in the bus voltage ripple when harmonic suppression methods are applied. This is due to the larger magnitude of $Z_o(s)$ at twice the line frequency attained by the suppression techniques, which prevents the DER converters from draining the second-order harmonic power affecting the DC bus.

3.8.3 Evaluation of stability performances

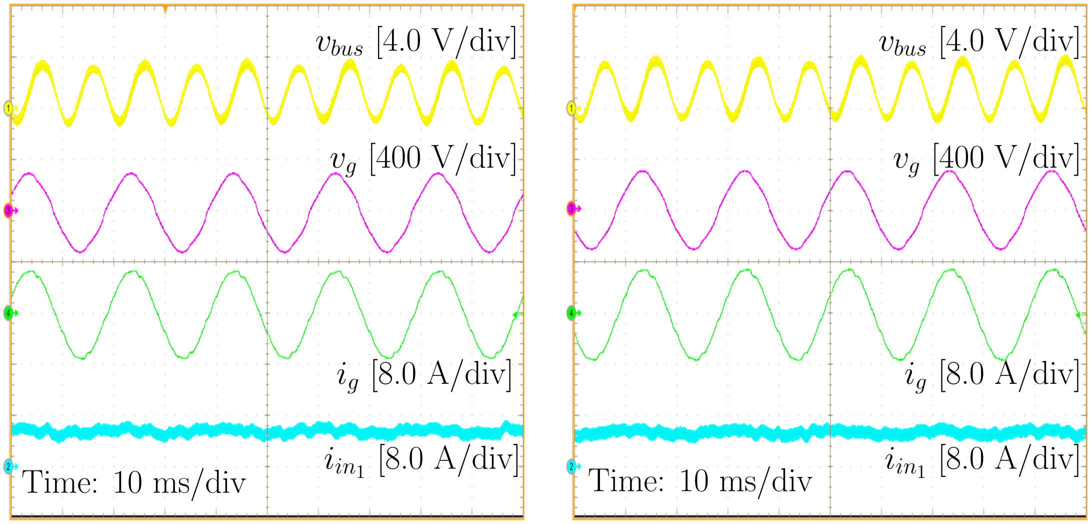
The dynamic processes of activating the second-order harmonic current suppression methods are now reported to show the stability performances of the considered approaches.

Notch filters

Fig. 3-22(a) shows the experimental result of activating $G_{\mathrm{nf}}(s)$. In the dynamic process, an oscillation can be observed in the bus voltage. Looking at the envelope, v_{bus} shows a peak of $1.9\,\mathrm{V}$ in the first oscillation cycle and reaches steady state after 3 cycles, which indicates poor a stability margin. Fig. 3-22(b) refers to the activation of $G_{\mathrm{mnf}}(s)$. As compared to $G_{\mathrm{nf}}(s)$, the bus voltage oscillation spike becomes smaller, indicating a better system stability, which shows the advantage of the proposed modified notch filter $G_{\mathrm{mnf}}(s)$.

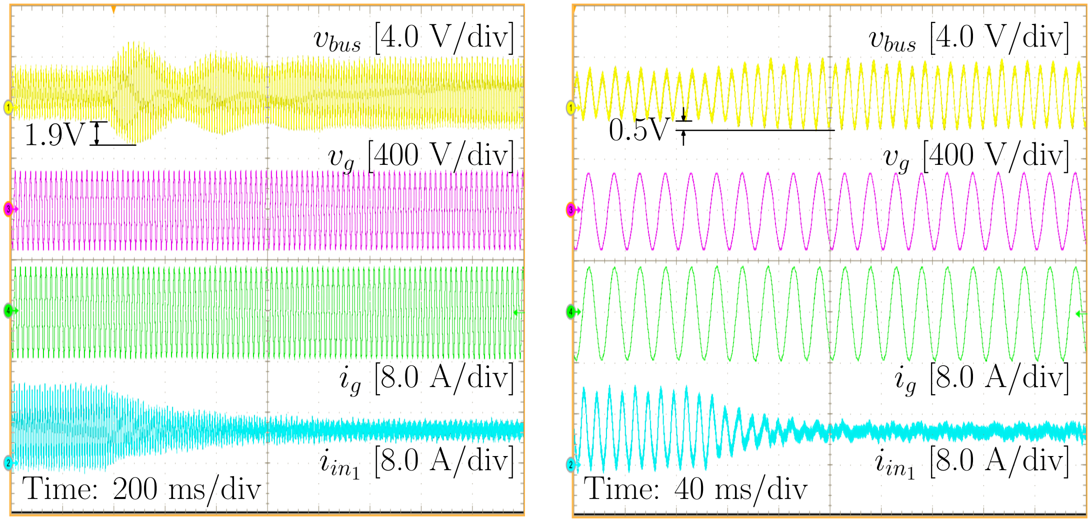


(a) $G_{\mathrm{nf}}(s)$ (b) $G_{\mathrm{mnf}}(s)$

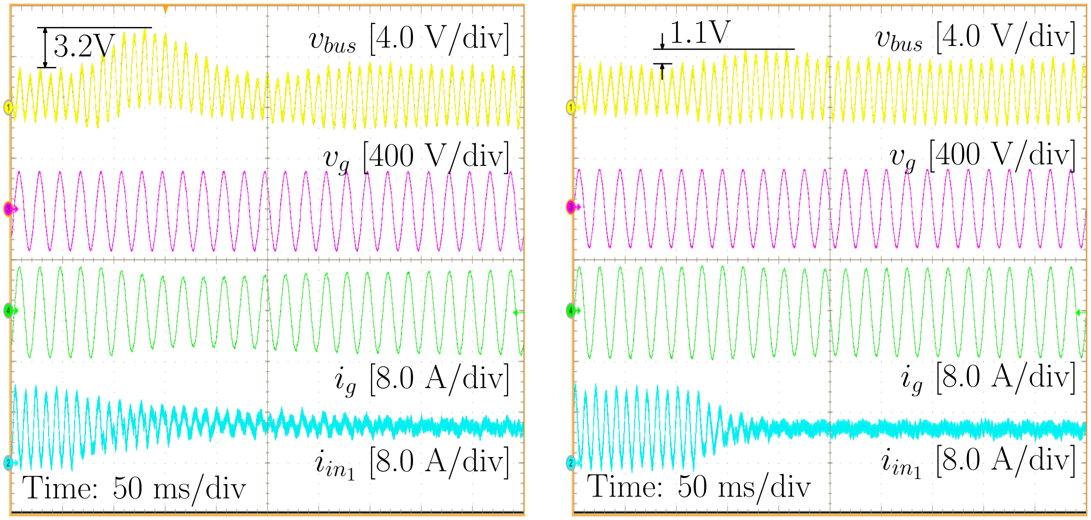


(c) $G_{\mathrm{rr}}(s)$ (d) $G_{\mathrm{mrr}}(s)$

Figure 3-21: Steady-state experimental results with different methods. v_{bus} offset: 380 V.



(a) $G_{\mathrm{nf}}(s)$ (b) $G_{\mathrm{mnf}}(s)$



(c) $G_{\mathrm{rr}}(s)$ (d) $G_{\mathrm{mrr}}(s)$

Figure 3-22: Dynamic experimental results of activating different filters and regulators. v_{bus} offset: 380 V.

Resonant regulators

Fig. 3-22(c) and Fig. 3-22(d) show the experimental results of activating $G_{\mathrm{rr}}(s)$ and $G_{\mathrm{mrr}}(s)$, respectively. After activating $G_{\mathrm{rr}}(s)$, v_{bus} shows an oscillation with an overshoot of $3.2\,\mathrm{V}$. Whereas, if $G_{\mathrm{mrr}}(s)$ is considered, the bus voltage oscillation overshoot reduces to $1.1\,\mathrm{V}$. This shows that the proposed modified resonant regulator $G_{\mathrm{mrr}}(s)$ is able to improve the system stability.

3.8.4 Evaluation of dynamic performances

The transient processes of load step are presented herein to assess the dynamic speed of DER converters with the modified approaches. In this test, the GIC and three DER converters are all activated. For the purpose of comparison, a low-bandwidth (corresponding to $50\,\mathrm{Hz}$ voltage loop bandwidth) voltage regulator, whose transfer function is $1.2 + 153/s$, is also implemented.

Notch filters

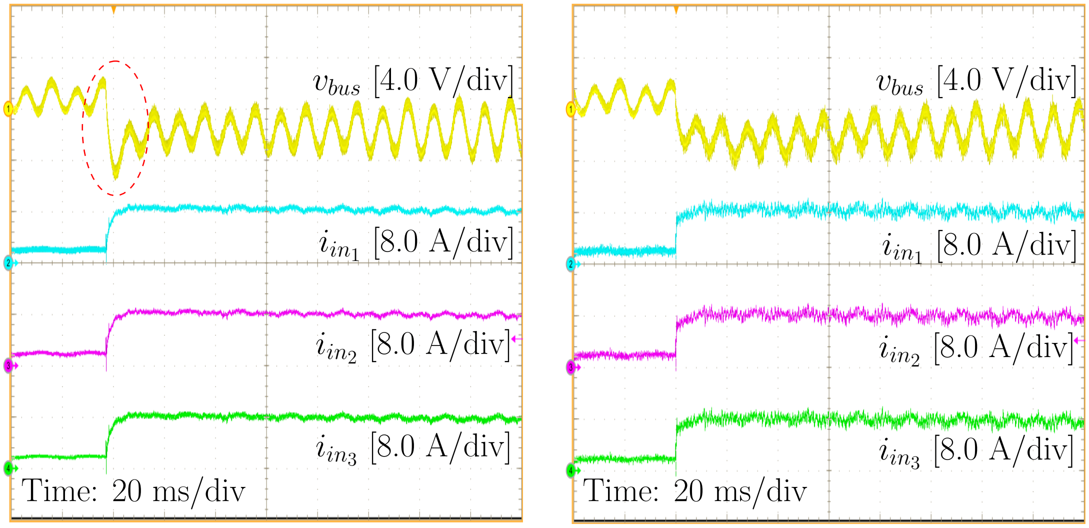
Fig. 3-23(a) shows the experimental result of load change, with the $50\,\mathrm{Hz}$ voltage regulator and $G_{\mathrm{mnf}}(s)$. Because of the low-bandwidth voltage loop, v_{bus} shows a significant drop during the transient. On the other hand, Fig. 3-23(b) shows the experimental result of the same load change, with the default $150\,\mathrm{Hz}$ voltage regulator and $G_{\mathrm{mnf}}(s)$. Thanks to the increase of the voltage control bandwidth, v_{bus} smoothly transit to the new steady state. Therefore, a high-bandwidth (over $2\omega_g$) voltage loop, which is the benefit brought by the proposed $G_{\mathrm{mnf}}(s)$, enables better dynamic performance and tighter DC bus voltage regulation.

Resonant regulators

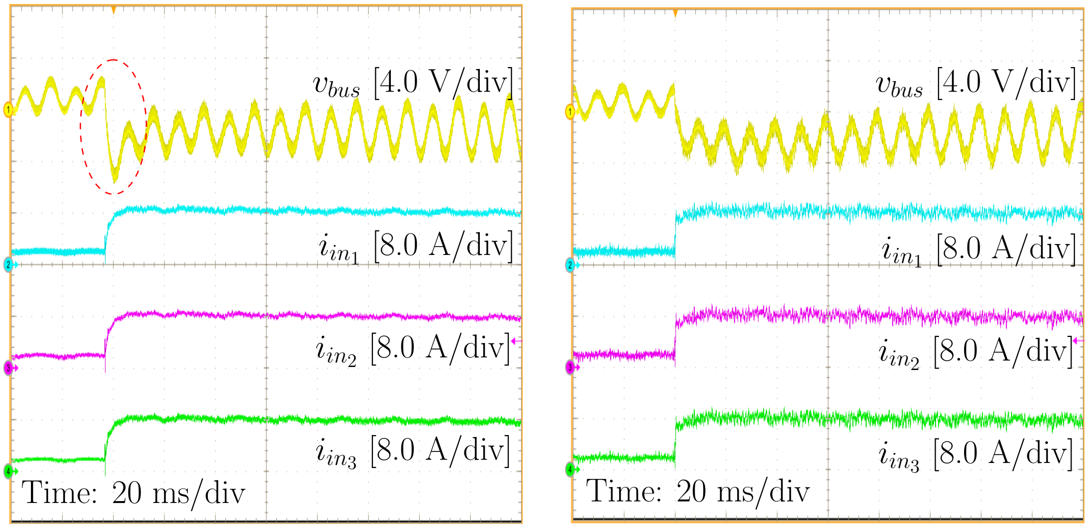
Fig. 3-23(c) and Fig. 3-23(d) report the experimental results about the dynamic speed with $G_{\mathrm{mrr}}(s)$ employed. Performing a load step in the DC microgrid, v_{bus} dips notably in Fig. 3-23(c), with the $50\,\mathrm{Hz}$ voltage regulator. On the contrary, the bus voltage drop is not observed with the $150\,\mathrm{Hz}$ voltage regulator in Fig. 3-23(d), validating the advantage of the proposed $G_{\mathrm{mrr}}(s)$.

3.9 Summary

This chapter presents four second-order harmonic current suppression methods for droop-controlled DER converters in DC microgrids coupled with AC power systems. The methods are based on the adoption of *a notch filter*, *a modified notch filter*, *a resonant regulator*, and *a modified resonant regulator*. They all allow converters connected to DC buses presenting a significant second-order harmonic voltage ripple to be free from corresponding current fluctuations at resource side. It is shown that, for the method adopting a notch filter and the one employing a resonant regulator, the voltage control bandwidth is limited to be below $2\omega_g$ to ensure stability, because these methods introduce large phase lags and high attenuation below $2\omega_g$ in the voltage control loop. Instead, in the case of the modified methods proposed in this paper, voltage control bandwidth can be designed to be above $2\omega_g$, while preserving stability and improving the converters dynamics. These four methods are verified experimentally on a prototype composed of three DER converters and one single-phase grid-interface converter.



(a) Low-bandwidth $G_v(s) + G_{\mathrm{mnf}}(s)$ (b) High-bandwidth $G_v(s) + G_{\mathrm{mnf}}(s)$



(a) Low-bandwidth $G_v(s) + G_{\mathrm{mrr}}(s)$ (b) High-bandwidth $G_v(s) + G_{\mathrm{mrr}}(s)$

Figure 3-23: Dynamic experimental results under load change. v_{bus} offset: 380 V.

Chapter 4

Seamless disconnection from upstream grids

Chapter 2 and Chapter 3 discusses the reduction of DC bus capacitance and the suppression of second-order harmonic current, respectively. Both of these two topics lie in the field of performance improvement for droop control. This chapter, however, focuses on the switch from power flow control to droop control. The goal is to allow DC microgrids:

- to operate with master-slave control if grid-interfacing converter works normally, taking advantage of the flexibility of power flow control;
- to work with peer-to-peer control if grid-interfacing converter fails, for the sake of reliability;
- to seamlessly transfer from grid-connected mode to islanded mode, when disconnecting from upstream grids.

This chapter is organized as follows. State-of-the-art is reviewed in Section 4.1. The control scheme of the proposed power-based droop control is introduced in Section 4.2. Then, the operation modes of a single DER converter considered individually and those of the whole microgrid are analyzed in Section 4.3. Section 4.4 discusses the controller design. The power sharing performance of the proposed control method is analyzed and compared with that of traditional droop control in Section 4.5. Finally, Section 4.6 reports the experimental results relevant to the steady-state and transient behaviors of the proposed control method, showing its feasibility and effectiveness.

4.1 State-of-the-art

As introduced in Section 1.3.3, with classical droop control, the power contributions from DER converters are determined by load power absorption. This behavior limits the power control flexibility at the output of DER converters and makes it difficult to apply power management strategies in which DER converters act as power sources [38, 130]. To address this problem, an additional power flow controller, operating in parallel with the droop controller, can be used [131]. In such a case, DER converters regulate their output power by means of the power flow controller when the bus voltage is imposed by the GIC, and they regulate the bus voltage by means of the droop controller when the GIC fails (e.g., due to faults or output power limitations). Unfortunately, switching between these two controllers usually requires time-critical communications between microgrid components or the implementation of bus voltage variations detection techniques, which increase system complexity and decrease reliability [41]. Similar issues, dealt with, for example, in [132–134], can be found in AC microgrids.

Power sharing is a key issue in DC microgrids due to the parallel operation of many DER converters. Although all the parallel converters share a common DC bus, the bus voltages at specific points of connection are not exactly the same because of the interconnection cable impedances. Indeed, load distribution within DC microgrids applying conventional droop control, with constant droop characteristics, is significantly affected by cable impedances [52]. For converters employing the *V-I* type droop method, since the droop coefficients can be approximately regarded as virtual output impedances [65], load distribution depends on the ratio between droop coefficients and cable impedances. With particular cable impedances, higher droop coefficients ensure better power sharing but result in wider bus voltage ranges. To cope with this trade-off, a nonlinear droop control method is presented in [76]. Under an equal voltage range, the droop coefficient is enlarged with the increase of the load power, attaining a more proportional power sharing under heavy loading conditions. In [135], Low-Bandwidth Communication (LBC) is used to restore the consequent voltage derivations. Hence, relatively larger droop coefficients can be selected with less concerns on bus voltage constrains. In [129], a small AC signal whose frequency is related to the bus voltage is injected onto the DC bus. Based on the signal frequency, which is uniform within the microgrid, the load can be distributed proportionally regardless of cable impedances. Active compensation of mismatch currents is another way to guarantee proportional power sharing. By considering the difference between the average output current and the actual converters output currents, a correction term can be added into the droop function through LBC, either to shift droop curves [30, 52, 136] or to adjust droop coefficients [137, 138]. Alternatively, for DER converters equipped with power flow controllers, the load can also be allocated in a proportional manner through LBC.

Aiming at achieving power flow control and enhancing system reliability, this chapter proposes a local power-based droop controller for DER converters by unifying the power flow controller and the droop controller. During normal operation, DERs track the given power references and the GIC imposes the bus voltage, while, during abnormal operation of the GIC, DERs ensure bus voltage regulation with droop control. The advantages of the proposed controller include *i)* regulation of DERs active power when the GIC is operating normally, accurately accomplishing specific power sharing configurations through LBC, regardless of cable impedances and loading conditions, *ii)* smooth transitions from power flow control to droop control in the event of the GIC inability in maintaining the bus voltage (e.g., due to power limitation or faults in the upstream grid), without using bus voltage variations detection schemes or communications with other microgrid elements.

4.2 Power-based droop controller

The power-based droop controller, which is designed for DER converters, is a combination of a droop controller and a power flow controller. Fig. 4-1 shows the scheme of this control approach, which mainly consists of three parts: inner voltage and current loops, droop loop, and power loop.

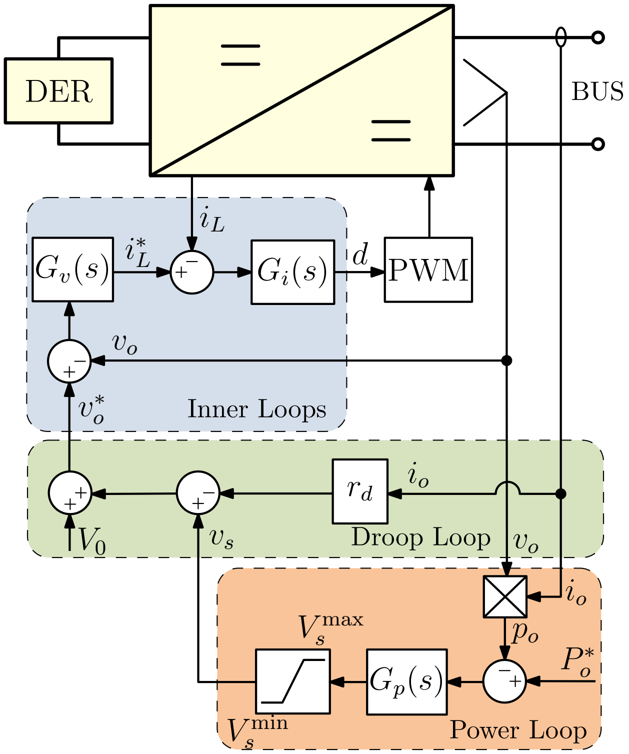


Figure 4-1: Scheme of the power-based droop control method.

Inner voltage and current loops

The inner voltage and current loops are the bases of the control structure. The inner voltage regulator $G_v(s)$ generates the current reference i_L^* by regulating the difference between the voltage reference v_o^* and the output voltage v_o. The current regulator $G_i(s)$ takes i_L^* and the inductor current i_L to produce the duty cycle d.

Droop loop

The *V-I* droop control is adopted herein. The voltage reference v_o^* is calculated as:

$$v_o^* = (V_0 + v_s) - r_d \cdot i_o \tag{4.1}$$

where V_0 is the voltage set point under no load condition, r_d is the droop resistance, v_s is the voltage offset determined by the power loop and i_o is the output current. In traditional droop control, v_s is zero. In the proposed solution, v_s is utilized to shift the droop curve upwards or downwards.

Power loop

Outside the droop loop, an external bounded power loop is added to track a given power reference P_{ref} which can be defined by a microgrid supervisor using non-critical communications. $G_p(s)$ is employed to regulate to zero the difference between the power reference P_{ref} and the output power p_o. The offset v_s is generated by $G_p(s)$ to shift the droop curve, enabling, in this way, power flow regulation:

$$v_s = (P_{\text{ref}} - p_o) \cdot G_p(s) \tag{4.2}$$

It should be noted that the upper and lower saturation levels of v_s, namely, $V_s^{\max}$ and $V_s^{\min}$, play a fundamental role in the controller. These two levels should be large enough to allow DER converters to reach their nominal power. On the other hand, once v_s is saturated, the proposed controller turns into a classical droop controller.

4.3 Operation modes

This section firstly describes the operation modes of a single DER converter. Then, the concept is extended to the microgrid level.

4.3.1 Operation modes of a single DER converter

From the standpoint of each individual DER converter, the operation modes can be classified into *power regulation mode* and *bus regulation mode*.

Power regulation mode

In power regulation mode, the DER converter exchanges the desired power P_{ref} with the microgrid, while other converters regulate the bus voltage. For example, Fig. 4-2 shows the operation principle of a DER converter in power regulation mode. Let us assume that the bus voltage is regulated at v_{o_A}, with v_{o_A} not necessarily equal to V_0. To achieve power flow control, the offset v_{s_A}, which is produced by the power regulator $G_p(s)$, is added to

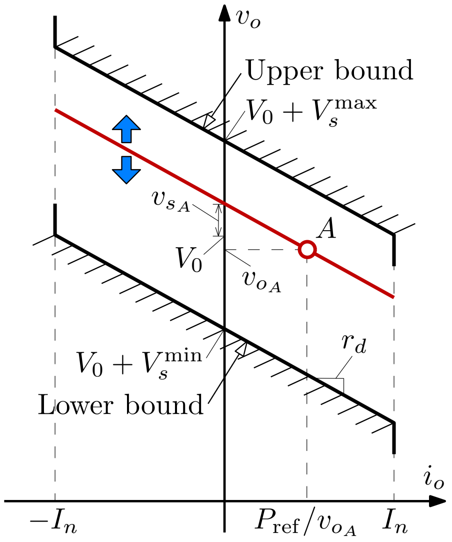


Figure 4-2: Operation principle of a DER converter in power regulation mode.

V_0. Then, the droop curve of the controller is shifted upwards by v_{s_A}, forcing the converter to operate at point A and to have an output current i_{o_A} equal to P_{ref}/v_{o_A}. Correspondingly, if the bus voltage stands at V_0, v_s is equal to $r_d \cdot P_{\text{ref}}/V_0$.

Bus regulation mode

in bus regulation mode, the DER converter contributes in ensuring bus voltage regulation. In this case, its output power p_o depends on load power demand and it is not equal, in general, to its given power reference P_{ref}. If p_o is larger than P_{ref}, the power regulator $G_p(s)$ saturates v_s at its lower level $V_s^{\min}$ and the droop curve leans against its lower bound. Conversely, if p_o is smaller than P_{ref}, v_s reaches its higher level $V_s^{\max}$ and the droop curve leans against its upper bound, as depicted in Fig. 4-3. The operation point of the DER converter stays on the lower or upper bound in a way that depends on the specific loading conditions. The resulting behavior at the converters output terminals is similar to that obtained with conventional droop control.

Transition mechanism

seamless transition from power regulation mode to bus regulation mode is an important feature of the proposed controller. This process actually consists in the transition of $G_p(s)$

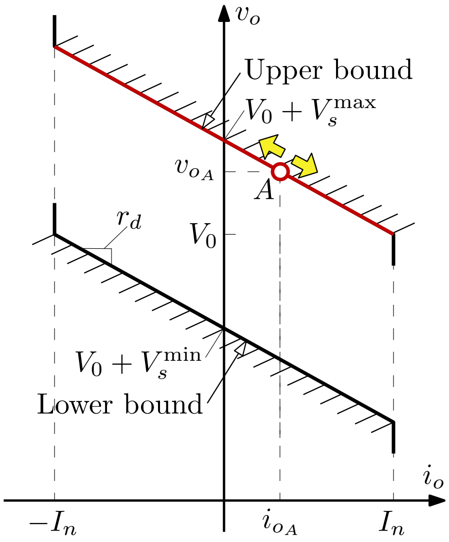


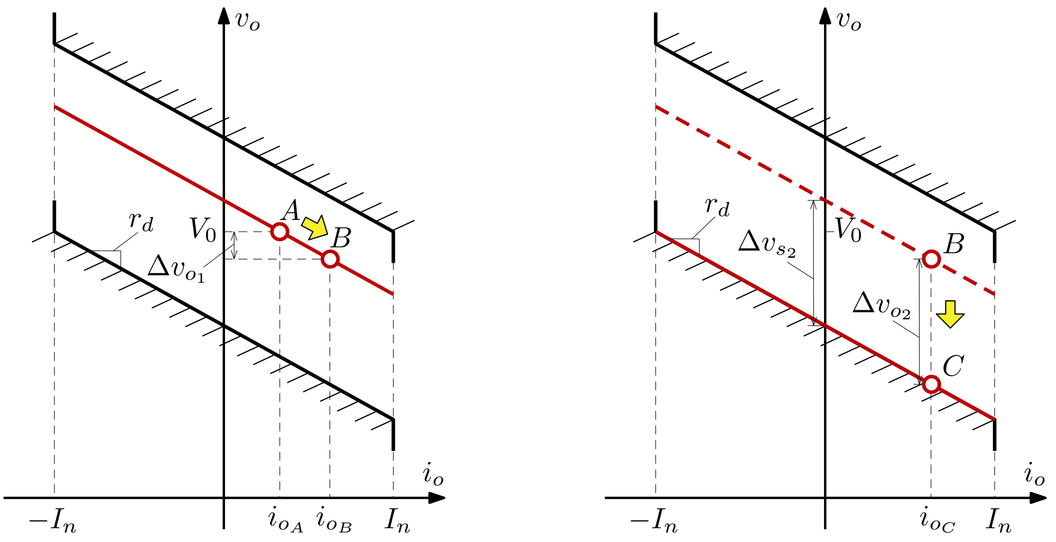
Figure 4-3: Operation principle of a DER converter in bus regulation mode.

from unsaturated state to saturated state. The following example is considered here to explain the principle of this operation. A DER converter switches from power regulation mode to bus regulation mode when the GIC stops the transfer of power from the upstream grid to the microgrid. This process can be divided into three stages, as presented in Fig. 4-4 and discussed in the following.

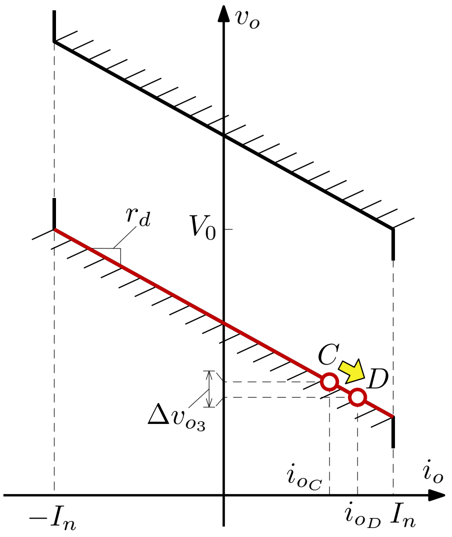
- Stage 1: assume the DER converter operating at a generic original operation point $A(V_0, i_{o_A})$, where i_{o_A} equals P_{ref}/V_0. After losing the support from the GIC, the lost power contribution from the GIC naturally redistributes to the droop controlled DER converter, which guarantees, in this way, the instantaneous power balance. Due to the control law (4.1) the bus voltage decreases and the operation point of the DER converter slides from A to B along the droop curve. As the outer power loop is usually designed to have a slower response than the droop loop, the effect of power loop, that is, the change of v_s, can be neglected in this stage. According to the control scheme, the following equation can be derived:

$$\varDelta v_{o_1} = -r_d \cdot (i_{o_B} - i_{o_A}) + \varDelta v_{s_1} \approx -r_d \cdot (i_{o_B} - \frac{P_{\text{ref}}}{V_0}) \tag{4.3}$$

where $\varDelta$ refers to changes of variables, the subscript 1 indicates the change occurring in the first stage and i_{o_B} is the output current at operation point B. Noticeably, in this



(a) stage 1: droop loop (b) stage 2: power loop



(c) stage 3: droop loop

Figure 4-4: Transition from power regulation mode to bus regulation mode.

stage, the output power p_o increases to compensate the lost contribution from the GIC and moves away from the power reference P_{ref}. Consequently, the error between p_o and P_{ref} becomes larger and v_s increases. On the contrary, the rate of change of v_o decreases as the power deficit reduces.

- Stage 2: once v_s changes at the same pace as v_o, the transition process steps into the second stage, where the power loop takes effect. The power regulator $G_p(s)$ completes the transition from the unsaturated state to the saturated state and the operation point of the DER converter moves from B to C. The variation of the bus voltage $\varDelta v_{o_2}$ can be expressed as:

$$\varDelta v_{o_2} = \varDelta v_{s_2} = V_s^{\min} - r_d \frac{P_{\text{ref}}}{V_0} \tag{4.4}$$

  where the subscript 2 indicates that the change occurs in the second stage. In this stage, the bus voltage deviates together with the droop curve and the output current approximately remains unchanged.

- Stage 3: the third stage begins when v_s hits its lower saturation level $V_s^{\min}$. The droop curve reaches its lower bound and the power regulator is inhibited. The bus voltage is then determined again by the droop loop and the operation point of the DER converter changes from C to D:

$$\varDelta v_{o_3} = -r_d \cdot (i_{o_D} - i_{o_C}) \tag{4.5}$$

  where the subscript 3 indicates that the change occurs in the third stage and i_{o_D} is the output current at operation point D. As can be seen, the bus voltage continues to decrease until the power balance is obtained. Finally, the microgrid enters another steady state.

4.3.2 Operation modes of microgrid

The operation of a DC microgrid with all the converters adopting the power-based droop controllers is now considered. The following operation modes can be identified.

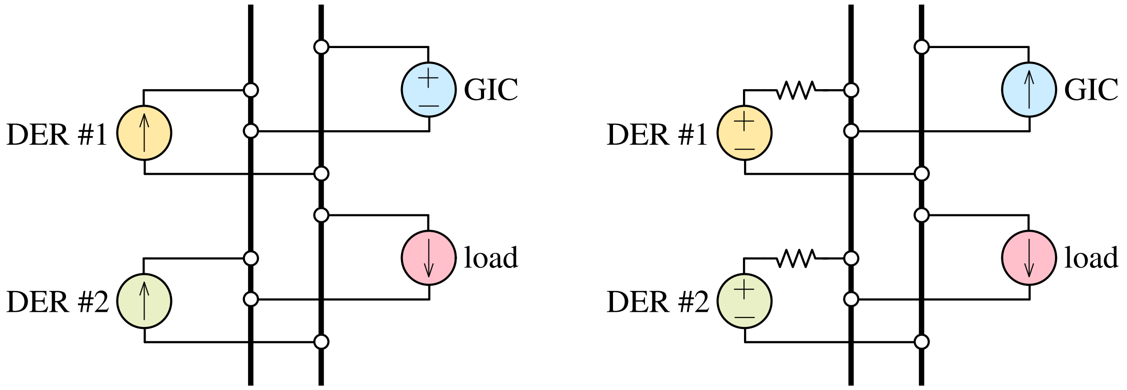
Mode I

In this mode, master-slave control strategy is adopted. The GIC compensates the power surplus or deficit within the microgrid through its connection with the upstream grid and maintains the bus voltage fixed at V_0, behaving as a grid-forming device. The DER converters operate in power regulation mode, tracking their own power references and behaving as grid-following devices. ESSs can be charged or discharged according to the desired targets and renewable energy resources can be operated at their maximum power points. The equivalent microgrid model is shown in Fig. 4-5(a).

Mode II

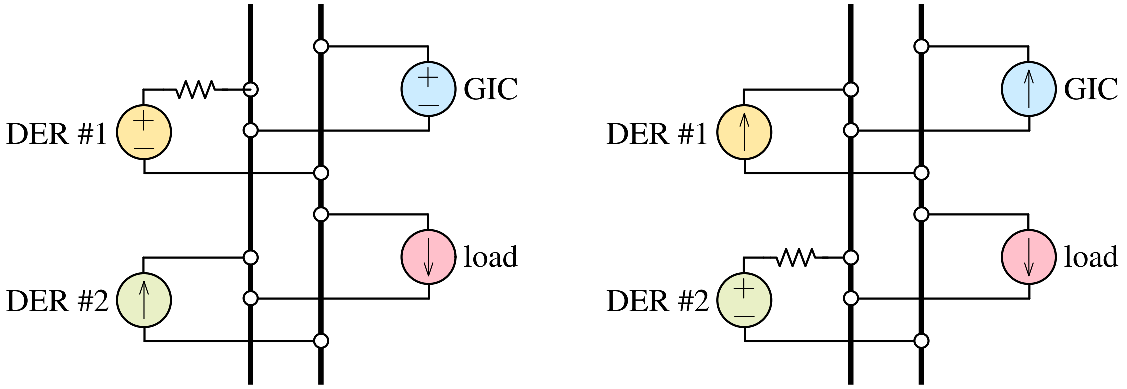
In this mode, peer-to-peer control strategy is employed. This mode occurs when the GIC is incapable of controlling the bus voltage. There are two possible causes for this mode: the upstream grid is unavailable or the required power flow exceeds the GIC availability (e.g., maximum converter's ratings). In these cases, the output power of the GIC is fixed, and it can be represented as a constant power source. Meanwhile, with power loop still activated, DER converters automatically reconfigure their operation status. For each DER converter, if the output power p_o is not equal to the power reference P_{ref}, the output of the power regulator $G_p(s)$ deviates and eventually saturates. In this condition, the droop curve is fixed at the upper or lower bound, and the converter works with droop control, operating in bus regulation mode to support the bus voltage. On the other hand, if p_o is equal to P_{ref}, the converter continues to operate in power regulation mode. It should be noted that, in practical cases, the sum of DER converters power references differs from the load power, thus, there is at least one DER converter operating in bus regulation mode.

To clearly explain the possible operation modes in *Mode II*, the example of a microgrid composed of two equal DER converters is now referred to. Let us assume $P_{\text{ref}_1} > P_{\text{ref}_2}$.



(a) mode I

(b) mode II, situation 1



(c) mode II, situation 2

(d) mode II, situation 3

Figure 4-5: Equivalent models of DC microgrid in different operation conditions.

The following situations can occur as a function of the load absorbed power P_L.

- Situation 1: Converter #1 and #2 are in bus regulation mode. Both of the droop curves of these two converters are saturated:
  - at the upper bound if:

$$P_{\text{ref}_1} > P_{\text{ref}_2} > \frac{P_L}{2} \tag{4.6}$$

  - at the lower bound if:

$$\frac{P_L}{2} > P_{\text{ref}_1} > P_{\text{ref}_2} \tag{4.7}$$

In this situation, the converters share the load equally if cable impedances are negligibly small. The equivalent microgrid model in this case is shown in Fig. 4-5(b). Since the lower and upper bounds of the droop curves are designed to have no intersections, the case that the droop curves of two converters are saturated at different bounds cannot happen (this aspect is specifically addresses in Section 4.4).

- Situation 2: Converter #1 is in bus regulation mode while converter #2 is in power regulation mode. Converter #2 tracks its power reference P_{ref_2} and converter #1 supplies the remaining power demand, that is, $P_L - P_{\mathrm{ref}_2}$. The droop curve of converter #1 is saturated at the upper bound. This situation occurs when:

  $$P_{\mathrm{ref}_1} > \frac{P_L}{2} > P_{\mathrm{ref}_2} \quad \& \quad P_{\mathrm{ref}_1} + P_{\mathrm{ref}_2} > P_L \tag{4.8}$$

  The equivalent microgrid model in this case is shown in Fig. 4-5(c).

- Situation 3: Converter #1 is in power regulation mode while converter #2 is in bus regulation mode. Similar to situation 2, the droop curve of converter #2 is saturated at the lower bound. The relationship between P_{ref_1}, P_{ref_2} and P_L in this situation can be expressed as:

  $$P_{\mathrm{ref}_1} > \frac{P_L}{2} > P_{\mathrm{ref}_2} \quad \& \quad P_{\mathrm{ref}_1} + P_{\mathrm{ref}_2} < P_L \tag{4.9}$$

  The equivalent microgrid model in this case is shown in Fig. 4-5(d).

It can be found that, the operation modes of DER converters are actually determined by factors like the load power, droop coefficients and power references. With the non-critical communication within the microgrid, appropriate power references can be chosen for DER converters to pursue specific operation situations.

4.4 Controller design

According to the operation principle, the controller design is presented in this section, with distributed cable impedances taken into consideration. The current regulator $G_i(s)$, the voltage regulator $G_v(s)$, and the power regulator $G_p(s)$ should be designed considering different operation modes [139]. The focus herein is, in particular, on the selection of

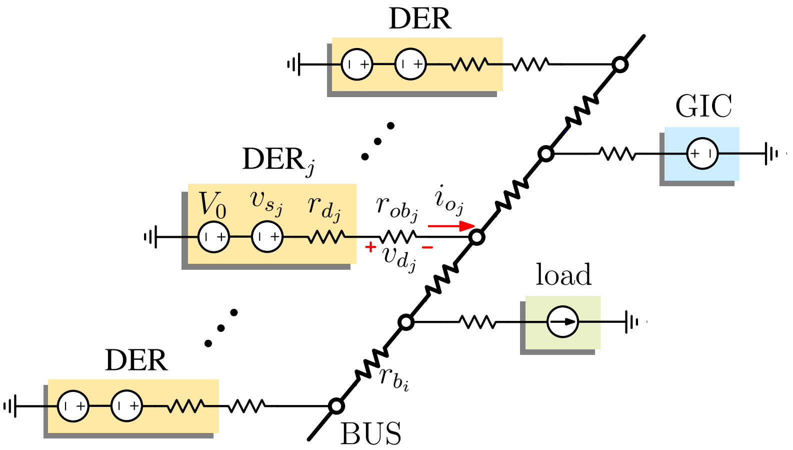


Figure 4-6: Equivalent model of a DC microgrid with cable impedance r_{ob} and r_b.

droop coefficient r_d and saturation levels of power regulator $G_p(s)$, $V_s^{\max}$ and $V_s^{\min}$, which is an aspect that deserves adequate investigation.

4.4.1 Current delivery capacity

When the microgrid is in *Mode I*, all DER converters operate in power regulation mode. In this condition, DER converters should be able to generate or absorb their nominal currents. For *V-I* type droop methods, the droop coefficients r_d can be regarded as virtual output resistance of DER converters, as shown in Fig. 4-6. In addition, the output-to-bus impedance r_{ob} of the cables that link DER converters to the DC bus can be considered as extra output impedance. Thus, for a DER converter, its total output impedance is $r_d + r_{ob}$ and its output voltage v_o can be expressed as

$$v_o = (V_0 + v_s) - (r_d + r_{ob}) \cdot i_o \tag{4.10}$$

This equivalent droop function is reported in Fig. 4-7. After considering the output-to-bus impedance r_{ob}, the droop curve shows a larger droop slope, resulting in an additional voltage drop v_d, which limits the actual current capacity that can be exploited. Besides, although the output voltage of the GIC is imposed at V_0, the bus voltage fluctuates from

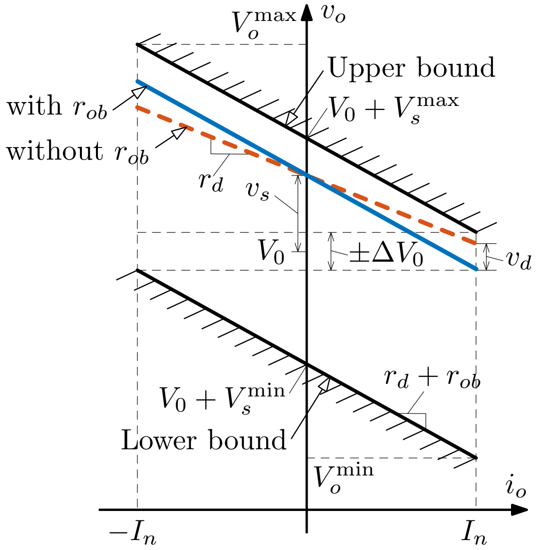


Figure 4-7: Equivalent droop function with cable impedance r_{ob}.

$V_0 - \mathit{\Delta} V_0$ to $V_0 + \mathit{\Delta} V_0$ due to distributed DC bus impedance r_b, that is

$$V_0 - \mathit{\Delta} V_0 \leqslant v_o \leqslant V_0 + \mathit{\Delta} V_0 \tag{4.11}$$

Then, by combining (4.10) and (4.11), the output current i_o of each DER converter can be shown as

$$\frac{v_s - \mathit{\Delta} V_0}{r_d + r_{ob}} \leqslant i_o \leqslant \frac{v_s + \mathit{\Delta} V_0}{r_d + r_{ob}} \tag{4.12}$$

It can be found that the output current range is determined by the range of variation of v_s, namely, from $V_s^{\min}$ to $V_s^{\max}$. To allow the exploitation of the full nominal current I_n of DER converters, that is, to allow the current i_o to assume all the values in the interval $[-I_n,\, I_n]$, the limitations of $V_s^{\max}$ and $V_s^{\min}$ should be defined as

$$\begin{cases} V_s^{\max} \geqslant I_n(r_d + r_{ob}) + \mathit{\Delta} V_0 \\ V_s^{\min} \leqslant -I_n(r_d + r_{ob}) - \mathit{\Delta} V_0 \end{cases} \tag{4.13}$$

The requirement of rated current capacity gives a lower limitation for $V_s^{\max}$ and an upper limitation for $V_s^{\min}$, respectively.

4.4.2 Bus voltage range

While in *Mode II* (i.e., autonomous mode), some DER converters operate in bus regulation mode and regulate the bus voltage. When these DER converters absorb the respective nominal current and their v_s are located at the upper saturation level $V_s^{\max}$, the highest output voltage $V_o^{\max}$ is obtained. Similarly, when the DER converters deliver nominal current and their v_s are located at the lower saturation level $V_s^{\min}$, the output voltage reaches its lowest level $V_o^{\min}$:

$$\begin{cases} V_o^{\max} = V_0 + V_s^{\max} + I_n(r_d + r_{ob}) \\ V_o^{\min} = V_0 + V_s^{\min} - I_n(r_d + r_{ob}) \end{cases} \tag{4.14}$$

If the acceptable bus voltage range is defined as $V_0 \pm \varDelta V_b$, then $V_o^{\max} \leqslant V_0 + \varDelta V_b$ and $V_o^{\min} \geqslant V_0 - \varDelta V_b$ must be satisfied. Accordingly, the limitations for $V_s^{\max}$ and $V_s^{\min}$ can be written as

$$\begin{cases} V_s^{\max} \leqslant \varDelta V_b - I_n(r_d + r_{ob}) \\ V_s^{\min} \geqslant \ -\varDelta V_b + I_n(r_d + r_{ob}) \end{cases} \tag{4.15}$$

The requirements on bus voltage range give an upper and a lower limitation, respectively, for $V_s^{\max}$ and $V_s^{\min}$.

4.4.3 Parameters selection

By combining (4.13) and (4.15), the available ranges of $V_s^{\max}$ and $V_s^{\min}$ can be found as

$$\begin{cases} I_n(r_d + r_{ob}) + \varDelta V_0 \leqslant V_s^{\max} \leqslant \varDelta V_b - I_n(r_d + r_{ob}) \\ -\varDelta V_b + I_n(r_d + r_{ob}) \leqslant V_s^{\min} \leqslant -I_n(r_d + r_{ob}) - \varDelta V_0 \end{cases} \tag{4.16}$$

According to (4.16), a restriction for r_d can be derived:

$$r_d \leqslant \frac{\varDelta V_b - \varDelta V_0 - 2I_n r_{ob}}{2I_n} \tag{4.17}$$

Since larger droop coefficient can bring benefits, such as higher power sharing accuracy, r_d should be chosen as large as possible. Additionally, for parallel DER converters, their droop coefficients should be inversely proportional to their nominal currents to attain a proportional load distribution. In this case, let us define a maximum acceptable voltage drop $V_d^{\max}$ on the output-to-bus cables r_{ob}. For any DER converter in the DC microgrid, it is required that the product of its rated current I_n and its output-to-bus cable impedance r_{ob} is less than $V_d^{\max}$. Then, the droop coefficient r_d can be selected as

$$r_d = \frac{\varDelta V_b - \varDelta V_0 - 2V_d^{\max}}{2I_n} \tag{4.18}$$

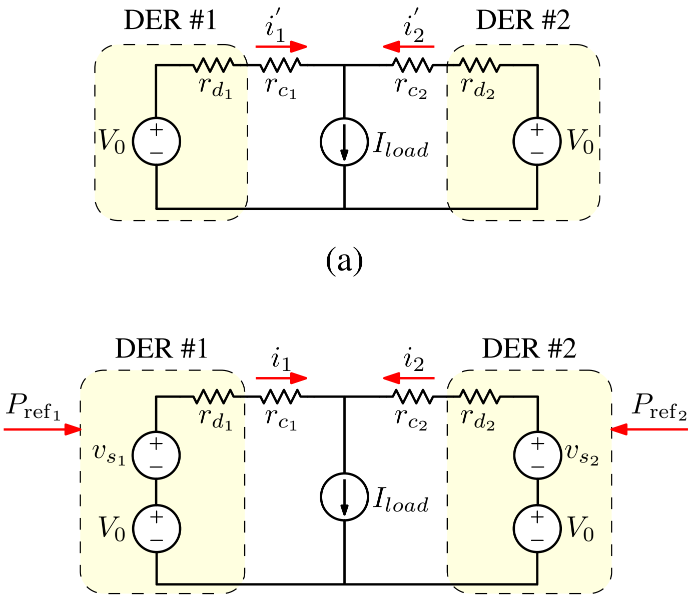
Further, $V_s^{\max}$ and $V_s^{\min}$ are set as

$$\begin{cases} V_s^{\max} = \dfrac{\varDelta V_b + \varDelta V_0 - 2V_d^{\max}}{2} \\ V_s^{\min} = -\dfrac{\varDelta V_b + \varDelta V_0 - 2V_d^{\max}}{2} \end{cases} \tag{4.19}$$

It can be seen that $V_s^{\max}$ and $V_s^{\min}$ are constants, so that all the DER converters share the same saturation levels. As a result, under no load condition, there is no circulating current among DER converters operating in bus regulation mode. It is also possible to find that the upper bounds do not intersect with the lower bounds at any voltage level, which means that DER converters operating in bus regulation mode must have droop curves saturated at the same level.

4.5 Power sharing performance

With the proposed controllers, when the microgrid is in *Mode I*, DER converters operate in power regulation mode. Through LBC, converters power references can be set in proportion to converters ratings. In this case, despite the existence of cable impedance, proportional power sharing can be accomplished precisely. However, when the DC microgrid operates in *Mode II*, power sharing accuracy degrades due to cable impedance. In the following, load distribution among parallel converters in the two operating modes is



(a)

(b)

Figure 4-8: Equivalent circuit of DC microgrids based on (a) traditional droop control; (b) power-based droop control.

discussed and compared with that of traditional droop control. A microgrid including two DER converters is considered in the comparison.

4.5.1 Traditional droop control

The equivalent circuit with DER converters employing droop controllers is shown in Fig. 4-8(a). The output currents $i_1^{'}$ and $i_2^{'}$ can be derived as

$$\begin{cases} i_1^{'} = \dfrac{r_{d_2} + r_{c_2}}{r_{d_1} + r_{c_1} + r_{d_2} + r_{c_2}} I_{load} \\ i_2^{'} = \dfrac{r_{d_1} + r_{c_1}}{r_{d_1} + r_{c_1} + r_{d_2} + r_{c_2}} I_{load} \end{cases} \tag{4.20}$$

where I_{load} is the load current and r_c is the cable impedance including the corresponding output-to-bus impedance r_{ob} and the bus impedance r_b. The mismatch $\varDelta i^{'}$ between the relative currents is defined as

$$\varDelta i^{'} = \frac{i_1^{'}}{I_{n_1}} - \frac{i_2^{'}}{I_{n_2}} = \frac{I_{load}}{I_{n_1} I_{n_2}} \frac{(r_{d_2} + r_{c_2}) I_{n_2} - (r_{d_1} + r_{c_1}) I_{n_1}}{r_{d_1} + r_{c_1} + r_{d_2} + r_{c_2}} \tag{4.21}$$

where I_{n_1} and I_{n_2} are the nominal output currents of converter #1 and #2, respectively. Only if $(r_{d_1} + r_{c_1})I_{n_1}$ equals $(r_{d_2} + r_{c_2})I_{n_2}$, there is no mismatch current and an exactly proportional load sharing is obtained.

4.5.2 Power-based droop control

When power-based droop controllers are used in DER converters, the equivalent circuit of the DC microgrid can be presented as in Fig. 4-8(b). The output of the power loop, v_s, can be regarded as an adjustable voltage source in series with the constant voltage source V_0.

The output currents, i_1 and i_2, of converter #1 and #2 can be calculated as

$$\begin{cases} i_1 = \dfrac{(r_{d_2} + r_{c_2})I_{load} + (v_{s_1} - v_{s_2})}{r_{d_1} + r_{c_1} + r_{d_2} + r_{c_2}} \\ i_2 = \dfrac{(r_{d_1} + r_{c_1})I_{load} - (v_{s_1} - v_{s_2})}{r_{d_1} + r_{c_1} + r_{d_2} + r_{c_2}} \end{cases} \tag{4.22}$$

the mismatch $\varDelta i$ of relative currents between these two converters results

$$\begin{aligned} \varDelta i &= \frac{i_1}{I_{n_1}} - \frac{i_2}{I_{n_2}} \\ &= \frac{I_{load}}{I_{n_1} I_{n_2}} \left[\frac{(r_{d_2} + r_{c_2})I_{n_2} - (r_{d_1} + r_{c_1})I_{n_1}}{r_{d_1} + r_{c_1} + r_{d_2} + r_{c_2}} + \frac{(v_{s_1} - v_{s_2})(I_{n_1} + I_{n_2})/I_{load}}{r_{d_1} + r_{c_1} + r_{d_2} + r_{c_2}} \right] \end{aligned} \tag{4.23}$$

4.5.3 Comparison of power sharing performance

A comparison of power sharing performance between the power-based droop control and the droop control is discussed here. Generally, the droop coefficient of a converter is inversely proportional to its nominal output current, that is, $r_{d_1} I_{n_1} = r_{d_2} I_{n_2}$. Hence, the ratio K_{mis} of $\varDelta i$ and $\varDelta i'$ is derived as

$$\begin{aligned} K_{mis} = \frac{\varDelta i}{\varDelta i'} &= 1 + \frac{(v_{s_1} - v_{s_2})(I_{n_1} + I_{n_2})}{(r_{d_2} + r_{c_2})I_{n_2} - (r_{d_1} + r_{c_1})I_{n_1}} \frac{1}{I_{load}} \\ &= 1 + \frac{(v_{s_1} - v_{s_2})(1/r_{d_1} + 1/r_{d_2})}{r_{c_2}/r_{d_2} - r_{c_1}/r_{d_1}} \frac{1}{I_{load}} \end{aligned} \tag{4.24}$$

If $|K_{mis}|$ is smaller than 1, the load is better distributed (i.e., in a way that is closer to the exact proportional sharing) with the power-based droop control. Otherwise, the traditional droop control method shows a better power sharing performance.

Since the saturation levels of v_{s_1} and v_{s_2} are the same, that is, $V_{s_1}^{\min} = V_{s_2}^{\min}$ and $V_{s_1}^{\max} = V_{s_2}^{\max}$, $|K_{mis}|$ is analyzed as follows.

1) $v_{s_1} = v_{s_2}$: it indicates the case that converter #1 and #2 are both in bus regulation mode. v_{s_1} and v_{s_2} are saturated at the same level, either the upper level or the lower one. $|K_{mis}|$ is equal to 1 in this case, traditional droop control and power-based droop control show the same power sharing accuracy.

2) $v_{s_1} \neq v_{s_2}$: it suggests the situation that one converter is in bus regulation mode while the other one is in power regulation mode. Therefore, the power loop brings additional uncertainty for power sharing.

If v_{s_1} is larger than v_{s_2}, there are two possible operation cases for these two converters. In the first case, converter #1 operates in bus regulation mode, with v_{s_1} saturated at the upper level, while converter #2 operates in power regulation mode. In the second one, converter #1 operates in power regulation mode, while converter #2 operates in bus regulation mode, with v_{s_2} saturated at the lower level. The indicator of power sharing performance, $|K_{mis}|$, is calculated as below:

- if $|(v_{s_1} - v_{s_2})(1/r_{d_1} + 1/r_{d_2})| < 2\,|(r_{c_2}/r_{d_2} - r_{c_1}/r_{d_1})I_{load}|$
  and $r_{c_2}/r_{d_2} < r_{c_1}/r_{d_1} \quad \Rightarrow \quad |K_{mis}| < 1$

- otherwise $\quad \Rightarrow \quad |K_{mis}| > 1$

If v_{s_1} is smaller than v_{s_2}, similarly, the power-based droop control attains a higher power sharing accuracy if $|(v_{s_1} - v_{s_2})(1/r_{d_1} + 1/r_{d_2})| < 2\,|(r_{c_2}/r_{d_2} - r_{c_1}/r_{d_1})I_{load}|$ and $r_{c_2}/r_{d_2} > r_{c_1}/r_{d_1}$.

In summary, when a DC microgrid is operating in *Mode I*, the power-based droop control method is able to distribute the load proportionally. When operating in *Mode II*, by coordinating DER converters' power references, the power-based droop control method is able to improve the load distribution among sources.

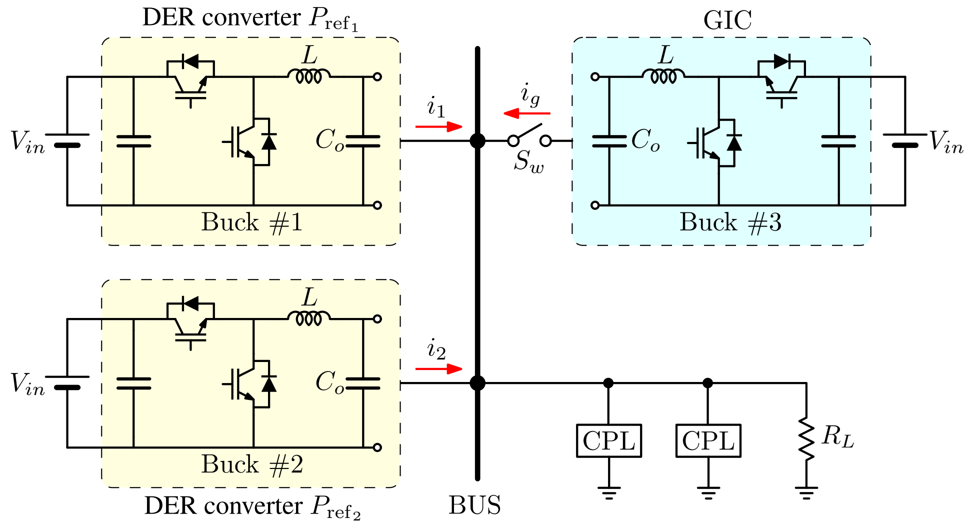


Figure 4-9: Schematic of the laboratory-scale DC microgrid.

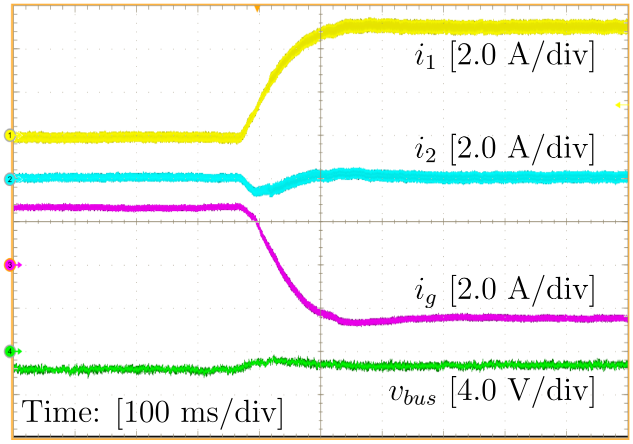
4.6 Experimental results

The actual operation of the proposed controller has been thoroughly tested by means of a laboratory-scale DC microgrid testbed, which is shown in Fig. 2-11. Herein, the testbed is configured as Fig. 4-9. It is composed of three parallel buck converters of $3\mathrm{kW}$ rated power, buck converter #1 and #2 play the role of DER converters and are controlled by the proposed power-based droop control, buck converter #3 plays the role of GIC. All the converters are powered by a DC power source. System parameters are listed in Table 4.1. Here, the acceptable bus voltage fluctuation is $\pm 15\%$ of the nominal value, that is $\pm \Delta V_b = \pm 30\,\mathrm{V}$, the maximum voltage drop V_d^{max} on the output-to-bus cable impedance r_{ob} is $5\,\mathrm{V}$, and the voltage drop ΔV_0 along the DC bus impedance r_b is neglected. According to (4.18) and (4.19), the droop coefficients for two DER converters are $0.67\,\mathrm{V/A}$, and the upper and lower saturation levels of $G_p(s)$ are $10\,\mathrm{V}$ and $-10\,\mathrm{V}$. The control bandwidths of the current loop, the voltage loop, and the power loop are designed at $1000\,\mathrm{Hz}$, $300\,\mathrm{Hz}$, and $3.5\,\mathrm{Hz}$, respectively.

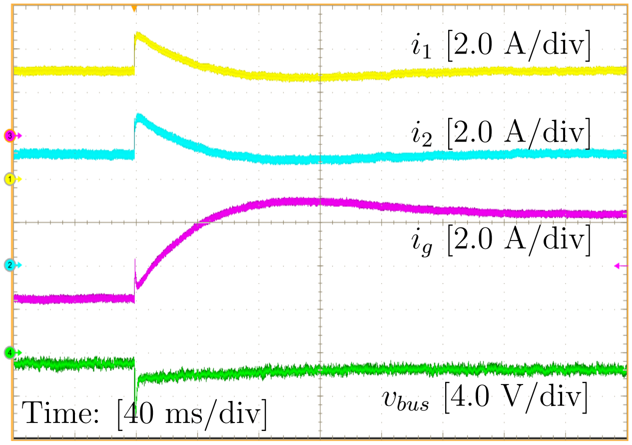
In the following, the basic functionality of the proposed control approach is firstly shown. Secondly, the achievable power sharing performance with cable impedance included is evaluated.

Table 4.1: Parameters of the system shown in Fig. 4-9

Parameter	Symbol	Value
	Converters	
Input voltage	V_{in}	$380\,\mathrm{V}$
Nominal bus voltage	V_{bus}	$200\,\mathrm{V}$
Nominal power	P_n	$3\,\mathrm{kW}$
Inductance	L_{in}	$1.6\,\mathrm{mH}$
Output capacitance	C_o	$110\,\mu\mathrm{F}$
Switching frequency	f_s	$12.5\,\mathrm{kHz}$
	Inner Current and Voltage Loops	
Current regulator	$G_i(s)$	$0.025 + 12.1/s$
Voltage regulator	$G_v(s)$	$0.16 + 395/s$
	Droop Loop	
Voltage set point	V_0	$200\,\mathrm{V}$
Droop coefficient	r_d	$0.67\,\mathrm{V/A}$
	Power Loop	
Upper saturation level	$V_s^{\max}$	$10\,\mathrm{V}$
Lower saturation level	$V_s^{\min}$	$-10\,\mathrm{V}$
Power regulator	$G_p(s)$	$0.067/s$



(a) P_{ref_1} step: $0\,\mathrm{kW} \rightarrow 1\,\mathrm{kW}$
condition: $P_{\mathrm{ref}_2} = 0\,\mathrm{kW}$, $R_L = 70\,\Omega$.



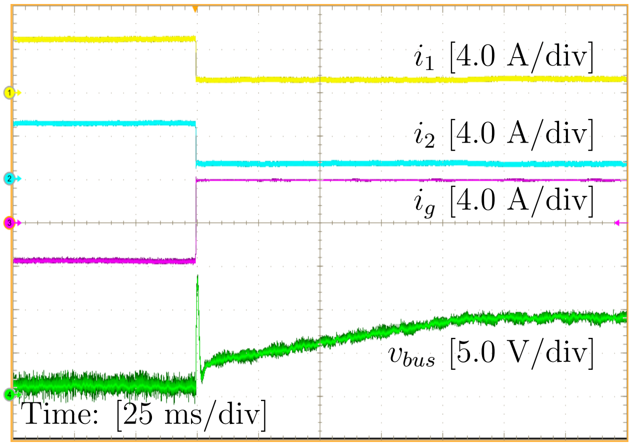
(b) load step: $70\,\Omega \rightarrow 30\,\Omega$
condition: $P_{\mathrm{ref}_1} = 1\,\mathrm{kW}$, $P_{\mathrm{ref}_2} = 1\,\mathrm{kW}$.

Figure 4-10: Dynamic experimental results in Mode I. v_{bus} offset: $200\,\mathrm{V}$.

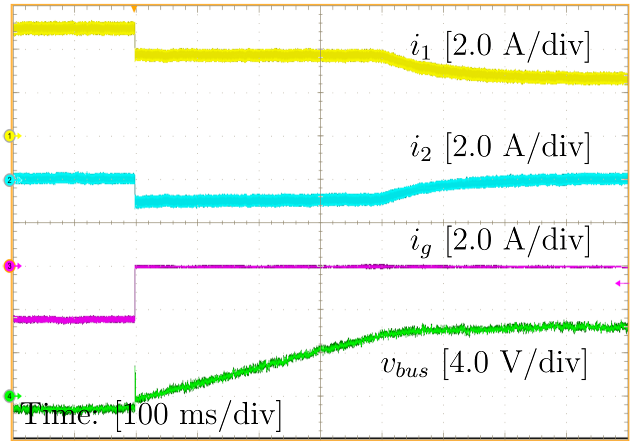
4.6.1 Basic functionality

The controller basic functionalities are evaluated while the microgrid operating in the two possible operation modes described in Section 4.3.

When the microgrid operates in *Mode I*, buck #1 and #2 operate in power regulation mode and the GIC dominates the bus voltage. A step change from $0\,\mathrm{kW}$ to $1\,\mathrm{kW}$ is applied to P_{ref_1}. The resulting dynamic performance is displayed in Fig. 4-10(a). The output current i_1 rises smoothly from $0\,\mathrm{A}$ to $5\,\mathrm{A}$, with the delivered output power correspondingly increasing up to $1\,\mathrm{kW}$. Accordingly, i_g reduces by $5\,\mathrm{A}$ to maintain the power balance. In



(a) condition: $P_{\text{ref}_1} = 1\,\text{kW}$, $P_{\text{ref}_2} = 1\,\text{kW}$, $R_L = 70\,\Omega$. i_g offset: $-4\,\text{A}$.

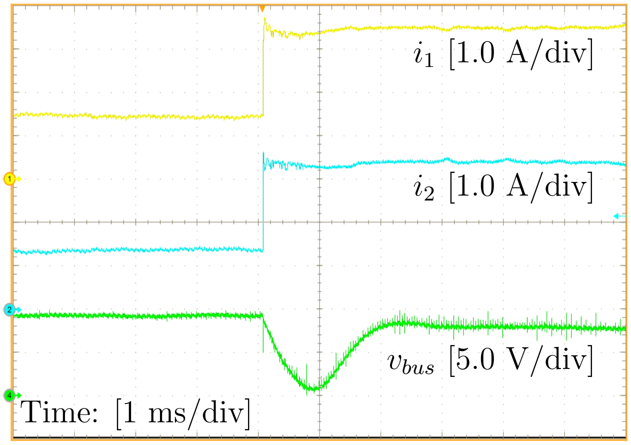


(b) condition: $P_{\text{ref}_1} = 1\,\text{kW}$, $P_{\text{ref}_2} = 0\,\text{kW}$, $R_L = 70\,\Omega$.

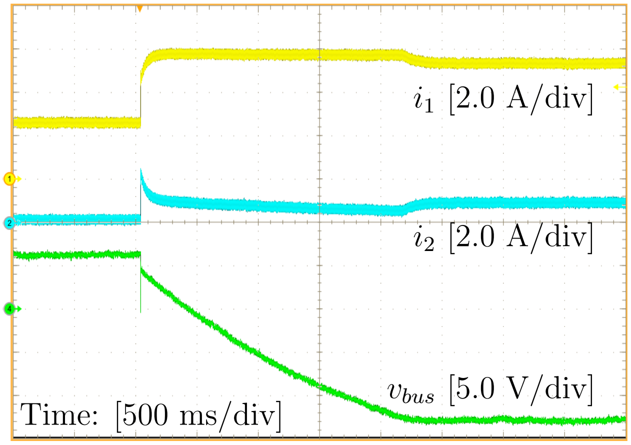
Figure 4-11: Transition from Mode I to Mode II: (a) situation 1; (b) situation 2. v_{bus} offset: 200 V.

the same operation case, the transient response with a load step from $70\,\Omega$ to $30\,\Omega$ is also shown in Fig. 4-10(b). The power deficit is compensated by the GIC, while buck #1 and #2 keep injecting their power references in steady-state.

The transition of the microgrid from *Mode I* to *Mode II* is performed by opening the switch S_w, that is, by disconnecting the GIC. As discussed in Section 4.3 and summarized in Fig. 4-5, under different situations of power references and loading conditions, different microgrid operations may establish during *Mode II*. The acquisitions displayed in Fig. 4-11(a) refer to microgrid operation in situation 1, with two DER converters operating in bus regulation mode. Whereas, Fig. 4-11(b) refers to a transition to *Mode II* in situation 2,



(a) condition: $P_{\mathrm{ref}_1} = 1\,\mathrm{kW}$, $P_{\mathrm{ref}_2} = 1\,\mathrm{kW}$.



(b) condition: $P_{\mathrm{ref}_1} = 1\,\mathrm{kW}$, $P_{\mathrm{ref}_2} = 0\,\mathrm{kW}$.

Figure 4-12: Dynamic experimental results of load step in Mode II: $70\,\Omega \rightarrow 30\,\Omega$. v_{bus} offset: $200\,\mathrm{V}$.

where buck #1 operates in bus regulation mode and buck #2 operates in power regulation mode. In both cases, the transition processes are achieved smoothly, which validates the effectiveness of the proposed control method.

Load step is implemented when the microgrid operates in *Mode II*. In Fig. 4-12(a), both DER converters operate in bus regulation mode before and after the load step. The total load power is increased by $800\,\mathrm{W}$ and each DER converter outputs $400\,\mathrm{W}$ more, that is, about $2\,\mathrm{A}$ of their currents. As a result, bus voltage decreases by $1.4\,\mathrm{V}$, due to the droop function. Besides, different power references and load steps may load to different microgrid states. As presented in Fig. 4-12(b), buck #1 switches from bus regulation mode to power

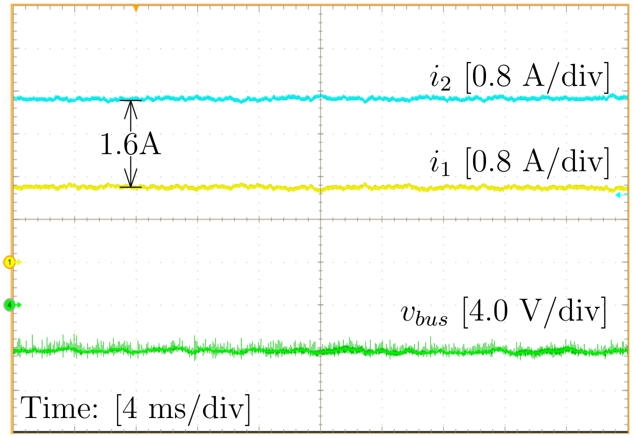


Figure 4-13: Power sharing performance of the traditional droop control, with $R_L = 30\,\Omega$. i_1 offset: $1\,\mathrm{A}$, i_2 offset: $1\,\mathrm{A}$, v_{bus} offset: $200\,\mathrm{V}$.

regulation mode, while buck #2 undergoes a reverse process during this transient.

4.6.2 Power sharing performance

A resistor r_b, with value $0.5\,\Omega$, is placed at the output terminal of buck #1 to emulate cable impedance. In this way, the power sharing performances of traditional droop control as compared to power-based droop control are evaluated.

With traditional droop control

in this test, converters #1 and #2 employ conventional droop controllers. Since these two converters have the same power rating, an equal load distribution is expected. However, due to bus impedance r_b, a mismatch current of $1.6\,\mathrm{A}$ can be observed in Fig. 4-13, with a load current of about $6.7\,\mathrm{A}$.

With power-based droop control

in this test, converters #1 and #2 employ the proposed power-based droop control. Fig. 4-14 shows the transient response with a step variation of the power reference P_{ref_1}, when the microgrid operates in *Mode I*. Since the bus voltage is imposed by the GI converter, converter #1 tracks its power reference precisely and the power sharing accuracy is preserved regardless of the bus impedance.

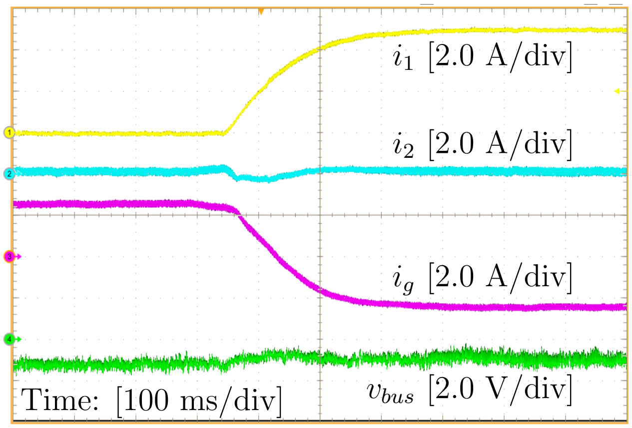
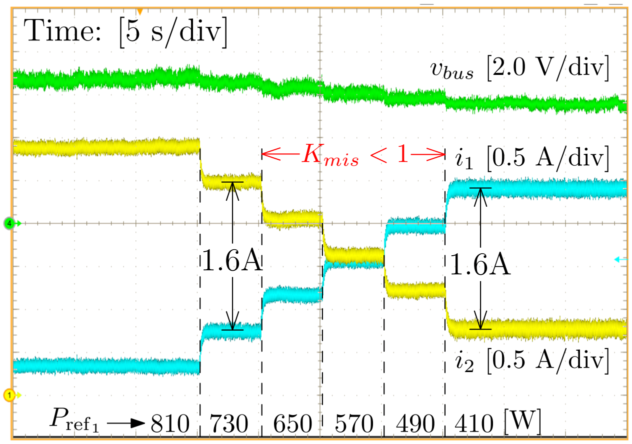


Figure 4-14: Power sharing performance of the proposed control method in Mode I, under P_{ref_1} step: $0\,\mathrm{kW} \rightarrow 1\,\mathrm{kW}$, with $P_{ref_2} = 0$ and $R_L = 70\,\Omega$. v_{bus} offset: $200\,\mathrm{V}$.

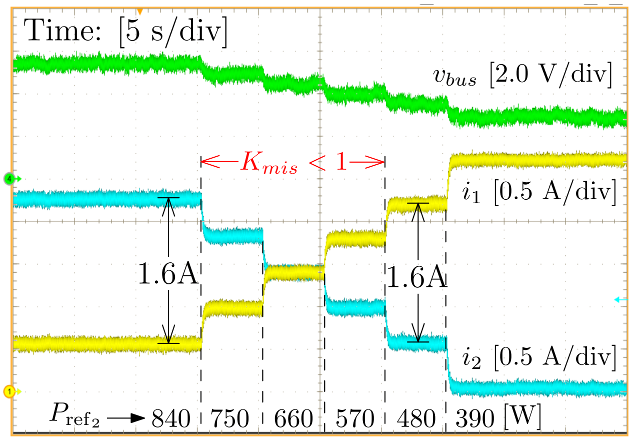
When the microgrid operates in *Mode II*, the power sharing performance is tested with different power references. Fig. 4-15(a) presents the result with converter #1 operating in power regulation mode and converter #2 operating in bus regulation mode. It can be seen that, by selecting proper power references, the mismatch current can be reduced or even totally eliminated. A similar result is obtained when converter #1 operates in bus regulation mode and converter #2 operates in power regulation mode, as shown in Fig. 4-15(b). As a consequence, compared to the traditional droop control method, power sharing accuracy is enhanced with the proposed approach.

4.7 Summary

This chapter presents a power-based droop controller for DER converters in DC microgrids that are connected to upstream grids by a GIC. During normal operation, the GIC imposes the bus voltage and the proposed controller allows DER converters to track given power references. If the GIC is not able (e.g., due to disconnection or faults) to provide bus voltage regulation, the proposed controller seamlessly transits to traditional droop controller, stabilizing the bus voltage. Moreover, by applying proper power references, the proposed control method allows better power sharing performances among parallel DER converters as compared to conventional droop control method. These features are attained by means of a bounded power loop on top of a traditional droop controller. In the paper, the design



(a) condition: $P_{\text{ref}_2} = 0\,\text{kW}$, $R_L = 30\,\Omega$.
i_1 and i_2 offset: 1.5 A, v_{bus} offset: 180 V.



(b) condition: $P_{\text{ref}_1} = 1.5\,\text{kW}$, $R_L = 30\,\Omega$.
i_1 and i_2 offset: 2 A, v_{bus} offset: 200 V.

Figure 4-15: Power sharing performance of the proposed control method in Mode II, with (a) different P_{ref_1} (W); (b) different P_{ref_2} (W).

criteria of the droop resistance and saturation levels of the power control loop are also discussed, satisfying the requirements of output current capacity and bus voltage regulation. Finally, the power-based droop control method has been implemented on a laboratory-scale DC microgrid testbed and its performance, in all the relevant operation modes, is experimentally verified and reported.

Chapter 5

Conclusions

This dissertation concentrates on the primary level control, particularly, droop control, for distributed energy resource converters in DC microgrids. The aim is to improve converter performances from three aspects by means of advanced control methods. The first aspect is about the reduction of converter output capacitance. The solutions studied herein include the improvement of design principle for droop-controlled converters and the utilization of hysteresis control. In the second aspect, the harmonic power coming from AC grid is suppressed at resource sides. This task is achieved by inserting a modified notch filter or resonant regulator in a droop controller. As for the third aspect, the investigation focuses on seamless disconnection of DC microgrids from upstream grids. A power-based droop controller is proposed to attain this goal.

1. A design approach is proposed for resource converters to achieve resistive output impedance, so that output capacitance can be reduced. The key point is to design the output capacitance, the voltage loop bandwidth, and the droop coefficient in a coordinated manner. The output capacitance should be selected according to the voltage loop bandwidth and the DC droop coefficient. The droop coefficient should be designed as a frequency-dependent term, which is related to the plant and other control parameters. This design guideline is applied to both non-isolated (buck and boost) and isolated (dual active bridge) DC-DC converters.

Hysteresis control is utilized to speed up the dynamic response of voltage loop. Compared to the case with PID control, smaller output capacitance is used while the output voltage is confined to the same acceptable range during transient. Hysteresis control is implemented in less-expensive digital signal processors with a sampling frequency of $200\,\mathrm{kHz}$, which is 10 times of the switching frequency. Although the implementation introduces one sampling period delay, the influence of this additional delay on the converter stability is acceptable.

2. Notch filter, modified notch filter, resonant regulator, and modified resonant regulator are employed in droop controllers. The first two filters are installed in voltage control loops and the last two regulators are added in current control loops. The performances of these four methods are compared in terms of output impedance and stability. All the approaches effectively increase converter output impedance at twice the line frequency. Notably, the proposed modified schemes overwhelm the traditional schemes by providing more stability margins. The design criteria for the proposed filter and regulator are discussed.

3. A power-based droop controller is proposed to enable seamless transition from power flow control to droop control. Based on this controller, the operation modes of a single converter and of a whole DC microgrids are described. Resource converters operate with power flow control when grid-interfacing converters impose DC bus voltage, and they regulate DC bus voltage with droop control when grid-interfacing converters are in abnormal conditions. The transfer from power flow control to droop control is achieved automatically, without communication or detection schemes. The power sharing performance between two converters are analyzed. The design guideline of the proposed controller is reported.

The scenarios outlined above are all supported and validated by experimental results referring to various laboratory-scale (several kilowatt) DC microgrid prototypes. Moreover, a DC microgrid prototype is built up from scratch. This prototype includes three boost converters and a central controller. The communication within this prototype is established by a $500\,\mathrm{kbps}$ CAN bus.

5.1 Future works

Within the area of this dissertation, there are still some gaps to fill.

1. This work only tests a set of parameters for the hysteresis-controlled droop converter.

The selection criteria of system parameters (e.g., the value of output capacitance, the slope of ramp, PI gains) should be further investigated. This study could be useful when this hysteresis control technique is applied to other power converters.

2. The modulation of DAB converters considered in this work only has one degree of freedom, i.e., the phase shift. In fact, many other modulation schemes have been proposed in literature, since they can potentially improve the converter performances, in terms of reactive power and soft-switching range. In such a case, output impedance shaping for DAB converters with other modulation schemes can be a worthwhile subject.

3. When considering cable impedance, nonlinear droop control could achieve more precise power sharing among parallel converters than linear droop control. How to obtain resistive output impedance for converters with nonlinear droop could be an interesting topic.

Appendix A

DC microgrid prototype

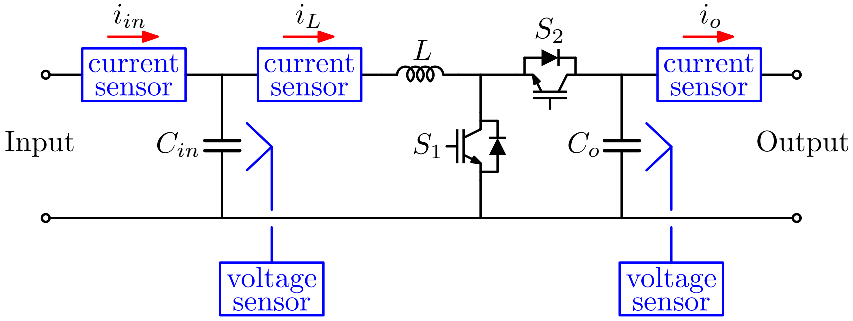
To experimentally verify the research proposals, a laboratory-scale DC microgrid prototype, which includes three boost DC-DC converters, is built from scratch. The target is to establish a general-purpose experimental platform for testing various control techniques in the scenario of DC microgrids. Since we have full access to every part of this prototype, the system parameters can be easily changed in case of needs, facilitating the current and future research studies. In the following, the structure of single boost converter and that of the entire DC microgrid will be introduced, respectively.

A.1 Single converter unit

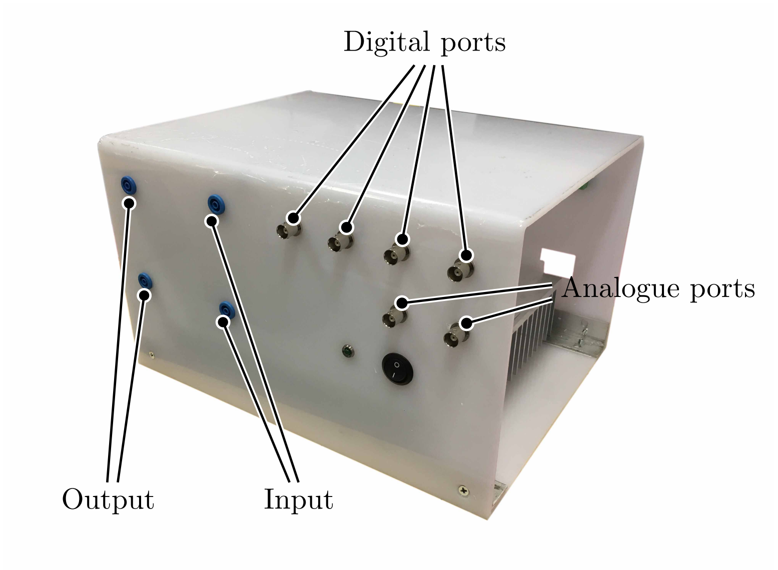
The power and sensing circuit diagram of one boost converter are shown in Fig. A-1(a). Besides, there are also some other major elements, such as protection circuits and the digital controller. The boost converter is boxed including all relevant components, and the picture is displayed in Fig. A-1(b).

A.1.1 Power circuit

The power circuit of the boost converter includes two power switches, one inductor, and input/output capacitors. The components are selected based on the system parameters. The nominal power of this converter is $3\,\mathrm{kW}$, the nominal input voltage is $200\,\mathrm{V}$, the nominal



(a) Circuit diagram



(b) Picture of the boost converter

Figure A-1: Circuit diagram and picture of the self-built boost converter.

output voltage is $380\,\mathrm{V}$, the nominal inductor current is $15\,\mathrm{A}$, and the nominal switching frequency is $20\,\mathrm{kHz}$.

Considering these parameters, the power switches use Insulated Gate Bipolar Transistors (IGBTs, IKW40N65ES5) from Infineon. The breakdown voltage of this IGBT is $650\,\mathrm{V}$ and the DC collector current can reach $40\,\mathrm{A}$.

The inductance is selected as $1\,\mathrm{mH}$, so that there is 30% switching ripple on the inductor current at nominal operating condition. The core for the inductor is the amorphous cut core (AMCU-40) from AMOGREENTECH. The air gap is designed as $1.5\,\mathrm{mm}$ at both columns, so that the A_L (inductance per turn) value has limited drop (less than 10%) with nominal DC bias current. The winding is made of 64 turns of litz wire with a cross section area of around $3.2\,\mathrm{mm}^2$ to support $15\,\mathrm{A}$ DC current.

The input and output capacitors use film capacitors. The input capacitance is $12\,\mu\mathrm{F}$ and the output capacitance is $24\,\mu\mathrm{F}$. Another $470\,\mathrm{nF}$ snubber capacitor is placed close to the power switches to form a short commutation loop. It is worth mentioning that one can freely install more capacitors on the input and output sides.

A.1.2 Sensing circuit

As shown in Fig. A-1(a), three current signals and two voltage signals are collected. The current transducers used in this prototype are CAS-25NP from LEM. This sensor supports maximum $25\,\mathrm{A}$ Root Mean Square (RMS) current and its measurement range is from $-85\,\mathrm{A}$ to $85\,\mathrm{A}$. The output of current sensors are sent to signal conditioning circuits to adjust the dc offset and the amplification gain. The signals after conditioning are sampled by Analog-to-Digital Converter (ADC) modules of the digital controller. The linear measurement range of the current sensing circuits (including current sensors and signal conditioning circuits) is from $-20\,\mathrm{A}$ to $20\,\mathrm{A}$.

The diagram of voltage sensing circuits is shown in Fig. A-2. The voltage signal is scaled down through resistors and is sent to an isolated amplifier (TLP7820). A dc offset voltage is connected to the other input of the amplifier, in order to locate the measurement range in a band surrounding the nominal voltage. The differential output of this amplifier

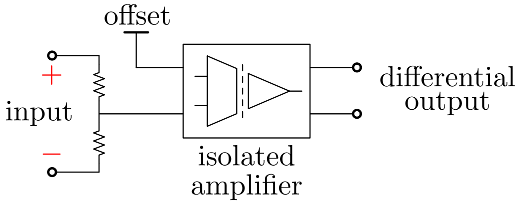


Figure A-2: Diagram of voltage sensing circuits.

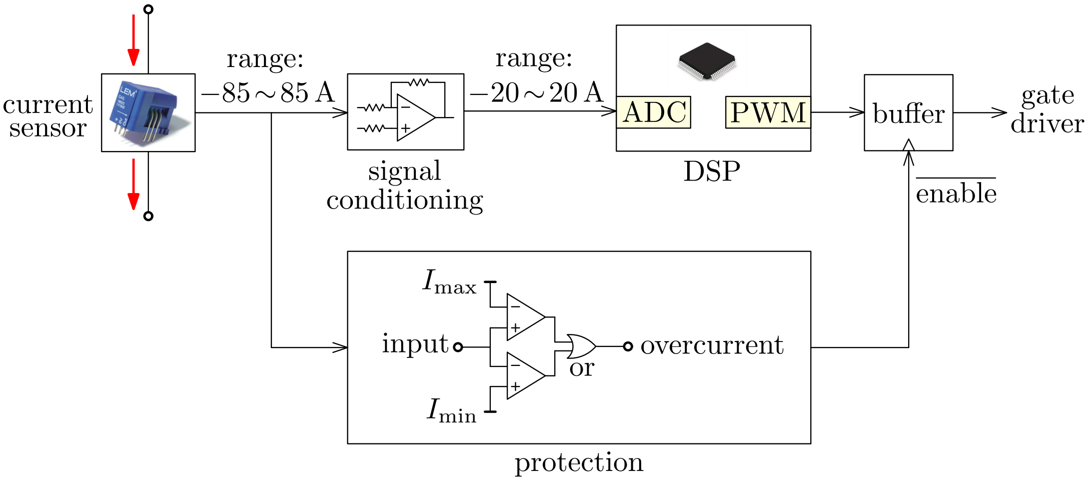


Figure A-3: Diagram of protection circuits.

is directly connected to ADC modules. In this prototype, the measurement range of input voltage is from 170 V to 230 V, and the measurement range of output voltage is from 335 V to 425 V.

A.1.3 Protection circuit

This prototype also includes hardware overcurrent protection circuits, as depicted in Fig. A-3. The protection circuits take the current signals produced by current sensors and compare these signals with upper/lower limits. Once the current signals exceed the limitations, the overcurrent flag is set and the PWM buffer is disabled. The maximum and minimum limitation levels can be changed by means of adjustable resistors.

A.1.4 Digital controller

The digital controller for the boost converter uses DSP TMS320F28379D from Texas Instruments. The CPU frequency of this dual-core DSP is 200 MHz. It also features a series

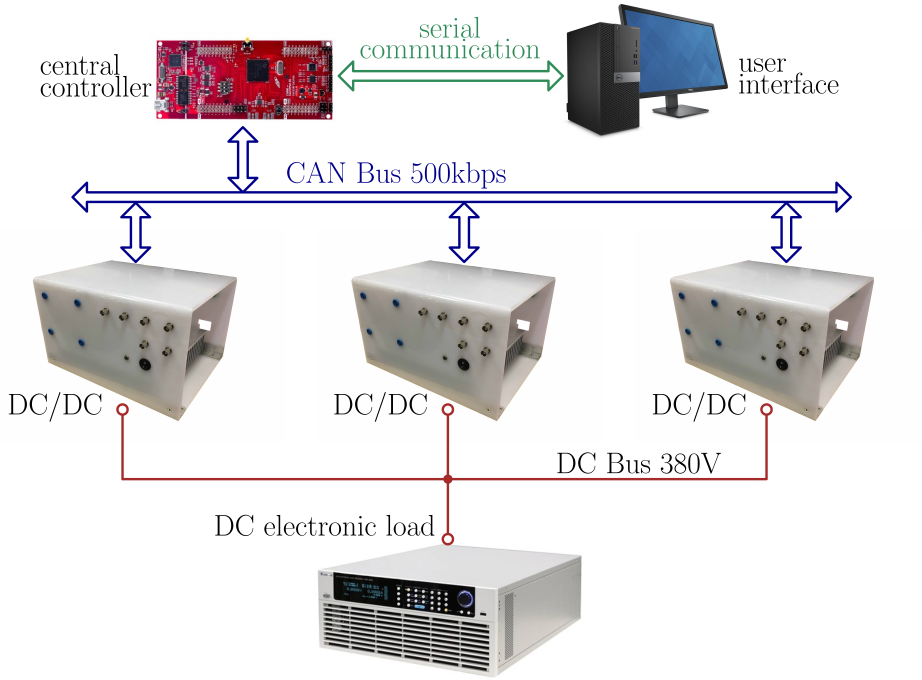


Figure A-4: Structure of entire DC microgrid prototype.

of built-in peripherals, like ADC, DAC, PWM, CAN bus, etc.

A.2 Entire prototype structure

The entire DC microgrid prototype, as illustrated in Fig. A-4, is composed of three boost converters described above, one central controller, and loads. The central controller is simply a DSP board (LAUNCHXL-F28379D). The communication link among converters and the central controller is established by a 500 kbps CAN bus. For the sake of user-friendly interface, there is also a serial communication link, between the central controller and a computer. Users could send commands to the central controller from the computer, and then, the commands are dispatched to converters. Thanks to the presence of communication link, it is possible to implement secondary-level and tertiary-level control techniques in this prototype.

Bibliography

[1] (2019) BP statistical review of world energy. [Online]. Available: http://www.bp.com/statisticalreview

[2] (2018) Intergovernmental Panel on Climate Change: global warming of 1.5°. [Online]. Available: https://report.ipcc.ch/sr15/pdf/sr15_spm_final.pdf

[3] The National Aeronautics and Space Administration (NASA): the effects of climate change. [Online]. Available: https://climate.nasa.gov/effects/

[4] D. Lew, R. Piwko, N. Miller, G. Jordan, K. Clark, and L. Freeman, "How do high levels of wind and solar impact the grid," *The Western Wind and Solar Integration Study National Renewable Energy Laboratory, Golden, CO*, 2010.

[5] L. Bird, M. Milligan, and D. Lew, "Integrating variable renewable energy: Challenges and solutions," National Renewable Energy Lab.(NREL), Golden, CO (United States), Tech. Rep., 2013.

[6] N. Nguyen and J. Mitra, "An analysis of the effects and dependency of wind power penetration on system frequency regulation," *IEEE Transactions on Sustainable Energy*, vol. 7, no. 1, pp. 354–363, Jan 2016.

[7] J. Conto, "Grid challenges on high penetration levels of wind power," in *2012 IEEE Power and Energy Society General Meeting*, July 2012, pp. 1–3.

[8] B. Wojszczyk and M. Brandao, "High penetration of distributed generation and its impact on electric grid performance - utility perspective," in *2011 IEEE PES Innovative Smart Grid Technologies*, Nov 2011, pp. 1–7.

[9] R. H. Lasseter, "Microgrids," in *2002 IEEE Power Engineering Society Winter Meeting. Conference Proceedings (Cat. No.02CH37309)*, vol. 1, Jan 2002, pp. 305–308 vol.1.

[10] N. Hatziargyriou, H. Asano, R. Iravani, and C. Marnay, "Microgrids," *IEEE Power and Energy Magazine*, vol. 5, no. 4, pp. 78–94, July 2007.

[11] F. Katiraei, R. Iravani, N. Hatziargyriou, and A. Dimeas, "Microgrids management," *IEEE Power and Energy Magazine*, vol. 6, no. 3, pp. 54–65, May 2008.

[12] S. X. Chen, H. B. Gooi, and M. Q. Wang, “Sizing of energy storage for microgrids,” *IEEE Transactions on Smart Grid*, vol. 3, no. 1, pp. 142–151, March 2012.

[13] J. M. Guerrero, P. C. Loh, T. Lee, and M. Chandorkar, “Advanced control architectures for intelligent microgrids-part II: Power quality, energy storage, and ac/dc microgrids,” *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1263–1270, April 2013.

[14] J. A. P. Lopes, C. L. Moreira, and A. G. Madureira, “Defining control strategies for microgrids islanded operation,” *IEEE Transactions on Power Systems*, vol. 21, no. 2, pp. 916–924, May 2006.

[15] B. Kroposki, R. Lasseter, T. Ise, S. Morozumi, S. Papathanassiou, and N. Hatziargyriou, “Making microgrids work,” *IEEE Power and Energy Magazine*, vol. 6, no. 3, pp. 40–53, May 2008.

[16] J. O. Dada, “Towards understanding the benefits and challenges of smart/micro-grid for electricity supply system in Nigeria,” *Renewable and Sustainable Energy Reviews*, vol. 38, pp. 1003–1014, 2014.

[17] D. T. Ton and M. A. Smith, “The US department of energy’s microgrid initiative,” *The Electricity Journal*, vol. 25, no. 8, pp. 84–94, 2012.

[18] J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodrguez, “Control of power converters in ac microgrids,” *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4734–4749, Nov 2012.

[19] F. Katiraei and M. R. Iravani, “Power management strategies for a microgrid with multiple distributed generation units,” *IEEE Transactions on Power Systems*, vol. 21, no. 4, pp. 1821–1831, Nov 2006.

[20] T. C. Green and M. Prodanović, “Control of inverter-based micro-grids,” *Electric power systems research*, vol. 77, no. 9, pp. 1204–1213, 2007.

[21] J. M. Guerrero, M. Chandorkar, T. Lee, and P. C. Loh, “Advanced control architectures for intelligent microgrids-part I: Decentralized and hierarchical control,” *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1254–1262, April 2013.

[22] H. Liu, P. C. Loh, X. Wang, Y. Yang, W. Wang, and D. Xu, “Droop control with improved disturbance adaption for a pv system with two power conversion stages,” *IEEE Transactions on Industrial Electronics*, vol. 63, no. 10, pp. 6073–6085, Oct 2016.

[23] T. Wu, C. Chang, L. Lin, and C. Kuo, “Power loss comparison of single- and two-stage grid-connected photovoltaic systems,” *IEEE Transactions on Energy Conversion*, vol. 26, no. 2, pp. 707–715, June 2011.

[24] B. Li, F. C. Lee, Q. Li, and Z. Liu, “Bi-directional on-board charger architecture and control for achieving ultra-high efficiency with wide battery voltage range,” in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 3688–3694.

[25] A. Khaligh and S. Dusmez, “Comprehensive topological analysis of conductive and inductive charging solutions for plug-in electric vehicles,” *IEEE Transactions on Vehicular Technology*, vol. 61, no. 8, pp. 3475–3489, Oct 2012.

[26] N. W. A. Lidula and A. D. Rajapakse, “Microgrids research: A review of experimental microgrids and test systems,” *Renewable and Sustainable Energy Reviews*, vol. 15, no. 1, pp. 186–202, 2011.

[27] M. Tamaki, S. Uehara, K. Takagi, and T. Ichikawa, “Demonstration results using miyako island mega-solar demonstration research facility,” in *PES T D 2012*, May 2012, pp. 1–4.

[28] S. Cobben, “Bronsbergen: The first micro-grid in the Netherlands,” in *Proceedings of the Kythnos 2008 Symposium on Microgrids*, 2008.

[29] D. Salomonsson, L. Soder, and A. Sannino, “An adaptive control system for a dc microgrid for data centers,” *IEEE Transactions on Industry Applications*, vol. 44, no. 6, pp. 1910–1917, Nov 2008.

[30] V. Nasirian, S. Moayedi, A. Davoudi, and F. L. Lewis, “Distributed cooperative control of dc microgrids,” *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2288–2303, April 2015.

[31] A. Kwasinski and C. N. Onwuchekwa, “Dynamic behavior and stabilization of dc microgrids with instantaneous constant-power loads,” *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 822–834, March 2011.

[32] H. Kakigano, Y. Miura, and T. Ise, “Low-voltage bipolar-type dc microgrid for super high quality distribution,” *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 3066–3075, Dec 2010.

[33] T. Dragicevic, X. Lu, J. C. Vasquez, and J. M. Guerrero, “DC microgrids-part II: A review of power architectures, applications, and standardization issues,” *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3528–3549, May 2016.

[34] A. Scharer, “DC for efficiency: Low voltage dc power infrastructure in data centers,” ABB, Tech. Rep.

[35] F. Zhang, C. Meng, Y. Yang, C. Sun, C. Ji, Y. Chen, W. Wei, H. Qiu, and G. Yang, “Advantages and challenges of dc microgrid for commercial building a case study from xiamen university dc microgrid,” in *2015 IEEE First International Conference on DC Microgrids (ICDCM)*, June 2015, pp. 355–358.

[36] J. Kumagai, “Lights for the enlightened,” *IEEE Spectrum*, vol. 53, no. 12, pp. 32–39, 2016.

[37] L. Che, M. Shahidehpour, A. Alabdulwahab, and Y. Al-Turki, “Hierarchical coordination of a community microgrid with ac and dc microgrids,” *IEEE Transactions on Smart Grid*, vol. 6, no. 6, pp. 3042–3051, Nov 2015.

[38] X. Liu, P. Wang, and P. C. Loh, “A hybrid ac/dc microgrid and its coordination control,” *IEEE Transactions on Smart Grid*, vol. 2, no. 2, pp. 278–286, June 2011.

[39] P. C. Loh, D. Li, Y. K. Chai, and F. Blaabjerg, “Autonomous operation of hybrid microgrid with ac and dc subgrids,” *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2214–2223, May 2013.

[40] N. Eghtedarpour and E. Farjah, “Power control and management in a hybrid ac/dc microgrid,” *IEEE Transactions on Smart Grid*, vol. 5, no. 3, pp. 1494–1505, May 2014.

[41] F. Nejabatkhah and Y. W. Li, “Overview of power management strategies of hybrid ac-dc microgrid,” *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7072–7089, Dec 2015.

[42] Y. Liu, J. Deng, C. Liu, and S. Li, “Energy optimization analysis of the more electric aircraft,” in *IOP Conference Series: Earth and Environmental Science*, vol. 113, no. 1. IOP Publishing, 2018, p. 012152.

[43] (2019) Kaishan island microgrid. [Online]. Available: http://www.chinawindenergy.com/news/gsdetail/1993

[44] T. Caldognetto, “Control of electronic power converters for low-voltage microgrids,” Ph.D. dissertation, University of Padova, 2016.

[45] T. Caldognetto and P. Tenti, “Microgrids operation based on master-slave cooperative control,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 4, pp. 1081–1088, Dec 2014.

[46] D. Velasco de la Fuente, C. L. Trujillo Rodrguez, G. Garcer, E. Figueres, and R. Ortega Gonzalez, “Photovoltaic power system with battery backup with grid-connection and islanded operation capabilities,” *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1571–1581, April 2013.

[47] D. Chen and L. Xu, “Autonomous dc voltage control of a dc microgrid with multiple slack terminals,” *IEEE Transactions on Power Systems*, vol. 27, no. 4, pp. 1897–1905, Nov 2012.

[48] B. Subudhi and R. Pradhan, “A comparative study on maximum power point tracking techniques for photovoltaic power systems,” *IEEE Transactions on Sustainable Energy*, vol. 4, no. 1, pp. 89–98, Jan 2013.

[49] F. Li, R. Li, and F. Zhou, *Microgrid technology and engineering application*. Elsevier, 2015.

[50] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla, “Hierarchical control of droop-controlled ac and dc microgridsa general approach toward standardization,” *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 158–172, Jan 2011.

[51] S. Augustine, M. K. Mishra, and N. Lakshminarasamma, “Adaptive droop control strategy for load sharing and circulating current minimization in low-voltage standalone dc microgrid,” *IEEE Transactions on Sustainable Energy*, vol. 6, no. 1, pp. 132–141, Jan 2015.

[52] X. Lu, J. M. Guerrero, K. Sun, and J. C. Vasquez, “An improved droop control method for dc microgrids based on low bandwidth communication with dc bus voltage restoration and enhanced current sharing accuracy,” *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1800–1812, April 2014.

[53] R. A. F. Ferreira, H. A. C. Braga, A. A. Ferreira, and P. G. Barbosa, “Analysis of voltage droop control method for dc microgrids with simulink: Modelling and simulation,” in *2012 10th IEEE/IAS International Conference on Industry Applications*, Nov 2012, pp. 1–6.

[54] L. Che and M. Shahidehpour, “Dc microgrids: Economic operation and enhancement of resilience by hierarchical control,” *IEEE Transactions on Smart Grid*, vol. 5, no. 5, pp. 2517–2526, Sep. 2014.

[55] L. Meng, Q. Shafiee, G. F. Trecate, H. Karimi, D. Fulwani, X. Lu, and J. M. Guerrero, “Review on control of dc microgrids and multiple microgrid clusters,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 3, pp. 928–948, Sep. 2017.

[56] Q. Shafiee, T. Dragicevic, J. C. Vasquez, and J. M. Guerrero, “Hierarchical control for multiple dc-microgrids clusters,” *IEEE Transactions on Energy Conversion*, vol. 29, no. 4, pp. 922–933, Dec 2014.

[57] G. Fei, K. Ren, C. Jun, and Y. Tao, “Primary and secondary control in dc microgrids: a review,” *Journal of Modern Power Systems and Clean Energy*, vol. 7, no. 2, pp. 227–242, 2019.

[58] L. Meng, T. Dragicevic, J. C. Vasquez, and J. M. Guerrero, “Tertiary and secondary control levels for efficiency optimization and system damping in droop controlled dc-dc converters,” *IEEE Transactions on Smart Grid*, vol. 6, no. 6, pp. 2615–2626, Nov 2015.

[59] X. Lu, K. Sun, J. M. Guerrero, J. C. Vasquez, and L. Huang, “State-of-charge balance using adaptive droop control for distributed energy storage systems in dc microgrid applications,” *IEEE Transactions on Industrial Electronics*, vol. 61, no. 6, pp. 2804–2815, June 2014.

[60] J. Xiao, P. Wang, and L. Setyawan, “Hierarchical control of hybrid energy storage system in dc microgrids,” *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4915–4924, Aug 2015.

[61] C. Jin, P. Wang, J. Xiao, Y. Tang, and F. H. Choo, “Implementation of hierarchical control in dc microgrids,” *IEEE Transactions on Industrial Electronics*, vol. 61, no. 8, pp. 4032–4042, Aug 2014.

[62] S. Moayedi and A. Davoudi, “Distributed tertiary control of dc microgrid clusters,” *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1717–1733, Feb 2016.

[63] H. Zhou, T. Bhattacharya, D. Tran, T. S. T. Siew, and A. M. Khambadkone, “Composite energy storage system involving battery and ultracapacitor with dynamic energy management in microgrid applications,” *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 923–930, March 2011.

[64] L. Guo, J. Y. Hung, and R. M. Nelms, “Evaluation of dsp-based pid and fuzzy controllers for dc-dc converters,” *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 2237–2248, June 2009.

[65] T. Dragicevic, X. Lu, J. C. Vasquez, and J. M. Guerrero, “DC microgrids-part I: A review of control strategies and stabilization techniques,” *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4876–4891, July 2016.

[66] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, “Proportional-resonant controllers and filters for grid-connected voltage-source converters,” *IEE Proceedings - Electric Power Applications*, vol. 153, no. 5, pp. 750–762, Sep. 2006.

[67] H. Qin and J. W. Kimball, “Closed-loop control of dc-dc dual active bridge converters driving single-phase inverters,” in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2012, pp. 173–179.

[68] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*. Morgan & Claypool, 2006.

[69] D. Trevisan, S. Saggini, and P. Mattavelli, “Hysteresis-based mixed-signal voltage-mode control for dc-dc converters,” in *2007 IEEE Power Electronics Specialists Conference*, June 2007, pp. 2664–2670.

[70] L. Corradini, E. Orietti, P. Mattavelli, and S. Saggini, “Digital hysteretic voltage-mode control for dc-dc converters based on asynchronous sampling,” *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 201–211, Jan 2009.

[71] J. Morroni, R. Zane, and D. Maksimovic, “An online stability margin monitor for digitally controlled switched-mode power supplies,” *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2639–2648, Nov 2009.

[72] A. Khodamoradi, G. Liu, P. Mattavelli, T. Caldognetto, and P. Magnone, “Analysis of an online stability monitoring approach for dc microgrid power converters,” *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4794–4806, May 2019.

[73] M. Shirazi, R. Zane, and D. Maksimovic, “An autotuning digital controller for dc-dc power converters based on online frequency-response measurement,” *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2578–2588, Nov 2009.

[74] W. Stefanutti, P. Mattavelli, S. Saggini, and M. Ghioni, “Autotuning of digitally controlled dc ndash;dc converters based on relay feedback,” *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 199–207, Jan 2007.

[75] L. Corradini, D. Maksimovic, P. Mattavelli, and R. Zane, *Digital control of high-frequency switched-mode power converters*. John Wiley & Sons, 2015.

[76] F. Chen, R. Burgos, D. Boroyevich, J. C. Vasquez, and J. M. Guerrero, “Investigation of nonlinear droop control in dc power distribution systems: Load sharing, voltage regulation, efficiency, and stability,” *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9404–9421, Oct 2019.

[77] A. Elrayyah, F. Cingoz, and Y. Sozer, “Construction of nonlinear droop relations to optimize islanded microgrid operation,” *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3404–3413, July 2015.

[78] Y. Gu, W. Li, and X. He, “Frequency-coordinating virtual impedance for autonomous power management of dc microgrid,” *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2328–2337, April 2015.

[79] Q. Xu, X. Hu, P. Wang, J. Xiao, P. Tu, C. Wen, and M. Y. Lee, “A decentralized dynamic power sharing strategy for hybrid energy storage system in autonomous dc microgrid,” *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 5930–5941, July 2017.

[80] F. Gao, S. Bozhko, A. Costabeber, C. Patel, P. Wheeler, C. I. Hill, and G. Asher, “Comparative stability analysis of droop control approaches in voltage-source-converter-based dc microgrids,” *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2395–2415, March 2017.

[81] Z. Jin, L. Meng, and J. M. Guerrero, “Comparative admittance-based analysis for different droop control approaches in dc microgrids,” in *IEEE Second International Conference on DC Microgrids (ICDCM)*, June 2017, pp. 515–522.

[82] H. Wang, M. Han, R. Han, J. M. Guerrero, and J. C. Vasquez, “A decentralized current-sharing controller endows fast transient response to parallel dc-dc converters,” *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4362–4372, May 2018.

[83] Y. Liu, T. C. Green, J. Wu, K. Rouzbehi, A. Raza, and D. Xu, "A new droop coefficient design method for accurate power-sharing in vsc-mtdc systems," *IEEE Access*, vol. 7, pp. 47 605–47 614, 2019.

[84] B. Sarlioglu and C. T. Morris, "More electric aircraft: Review, challenges, and opportunities for commercial transport aircraft," *IEEE Transactions on Transportation Electrification*, vol. 1, no. 1, pp. 54–64, June 2015.

[85] D. Salomonsson, L. Soder, and A. Sannino, "Protection of low-voltage dc microgrids," *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 1045–1053, July 2009.

[86] S. Beheshtaein, R. M. Cuzner, M. Forouzesh, M. Savaghebi, and J. M. Guerrero, "Dc microgrid protection: A comprehensive review," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2019.

[87] A. Aldhaheri and A. H. Etemadi, "Stabilization and performance preservation of dc-dc cascaded systems by diminishing output impedance magnitude," *IEEE Transactions on Industry Applications*, vol. 54, no. 2, pp. 1481–1489, March 2018.

[88] L. Cao, K. H. Loo, and Y. M. Lai, "Systematic derivation of a family of output-impedance shaping methods for power converters-a case study using fuel cell-battery-powered single-phase inverter system," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5854–5869, Oct 2015.

[89] K. Yao, M. Xu, Y. Meng, and F. C. Lee, "Design considerations for vrm transient response based on the output impedance," *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1270–1277, Nov 2003.

[90] M. Lee, D. Chen, K. Huang, C. Liu, and B. Tai, "Modeling and design for a novel adaptive voltage positioning (avp) scheme for multiphase vrms," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1733–1742, July 2008.

[91] A. Borrell, M. Castilla, J. Miret, J. Matas, and L. G. de Vicua, "Control design for multiphase synchronous buck converters based on exact constant resistive output impedance," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 11, pp. 4920–4929, Nov 2013.

[92] E. Unamuno and J. A. Barrena, "Design and small-signal stability analysis of a virtual-capacitor control for dc microgrids," in *European Conference on Power Electronics and Applications (ECCE Europe)*, Sept 2017, pp. P.1–P.10.

[93] X. Wang, Y. W. Li, F. Blaabjerg, and P. C. Loh, "Virtual-impedance-based control for voltage-source and current-source converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7019–7037, Dec 2015.

[94] Q. C. Zhong and Y. Zeng, "Control of inverters via a virtual capacitor to achieve capacitive output impedance," *IEEE Transactions on Power Electronics*, vol. 29, no. 10, pp. 5568–5578, Oct 2014.

[95] L. Guo, S. Zhang, X. Li, Y. W. Li, C. Wang, and Y. Feng, “Stability analysis and damping enhancement based on frequency-dependent virtual impedance for dc microgrids,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 338–350, March 2017.

[96] P. Lin, P. Wang, J. Xiao, J. Wang, C. Jin, and Y. Tang, “An integral droop for transient power allocation and output impedance shaping of hybrid energy storage system in dc microgrid,” *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6262–6277, July 2018.

[97] Z. Jin, L. Meng, R. Han, J. M. Guerrero, and J. C. Vasquez, “Admittance-type rc-mode droop control to introduce virtual inertia in dc microgrids,” in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 4107–4112.

[98] J. Bcker and O. Buchholz, “Can oversampling improve the dynamics of pwm controls?” in *2013 IEEE International Conference on Industrial Technology (ICIT)*, Feb 2013, pp. 1818–1824.

[99] L. Corradini and P. Mattavelli, “Modeling of multisampled pulse width modulators for digitally controlled dc-dc converters,” *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1839–1847, July 2008.

[100] S. Tan, Y. M. Lai, and C. K. Tse, “General design issues of sliding-mode controllers in dc-dc converters,” *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, pp. 1160–1174, March 2008.

[101] P. Cortes, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo, and J. Rodriguez, “Predictive control in power electronics and drives,” *IEEE Transactions on Industrial Electronics*, vol. 55, no. 12, pp. 4312–4324, Dec 2008.

[102] K. Yao, Y. Ren, and F. C. Lee, “Critical bandwidth for the load transient response of voltage regulator modules,” *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1454–1461, Nov 2004.

[103] (2019) Texas Instruments software frequency response analyzer (SFRA) library user’s guide. [Online]. Available: http://www.ti.com/tool/SFRA

[104] H. Bai and C. Mi, “Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge dc-dc converters using novel dual-phase-shift control,” *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 2905–2914, Nov 2008.

[105] H. Bai, Z. Nie, and C. C. Mi, “Experimental comparison of traditional phase-shift, dual-phase-shift, and model-based control of isolated bidirectional dc-dc converters,” *IEEE Transactions on Power Electronics*, vol. 25, no. 6, pp. 1444–1449, June 2010.

[106] H. Qin and J. W. Kimball, “Generalized average modeling of dual active bridge dc-dc converter,” *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 2078–2084, April 2012.

[107] F. Krismer and J. W. Kolar, “Accurate small-signal model for the digital control of an automotive bidirectional dual active bridge,” *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2756–2768, Dec 2009.

[108] Q. Jiang, M. Xue, and G. Geng, “Energy management of microgrid in grid-connected and stand-alone modes,” *IEEE Transactions on Power Systems*, vol. 28, no. 3, pp. 3380–3389, Aug 2013.

[109] J. Wang, C. Jin, and P. Wang, “A uniform control strategy for the interlinking converter in hierarchical controlled hybrid ac/dc microgrids,” *IEEE Transactions on Industrial Electronics*, vol. 65, no. 8, pp. 6188–6197, Aug 2018.

[110] T. F. Wu, K. H. Sun, C. L. Kuo, and C. H. Chang, “Predictive current controlled 5-kw single-phase bidirectional inverter with wide inductance variation for dc-microgrid applications,” *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 3076–3084, Dec 2010.

[111] X. Li, L. Guo, C. Wang, S. Zhang, Y. Rong, Y. Feng, and Y. Li, “Robust and autonomous dc bus voltage control and stability analysis for a dc microgrid,” in *IEEE International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, pp. 3708–3714.

[112] X. Li, W. Zhang, H. Li, R. Xie, M. Chen, G. Shen, and D. Xu, “Power management unit with its control for a three-phase fuel cell power system without large electrolytic capacitors,” *IEEE Transactions on Power Electronics*, vol. 26, no. 12, pp. 3766–3777, Dec 2011.

[113] M. E. Schenck, J.-S. Lai, and K. Stanton, “Fuel cell and power conditioning system interactions,” in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, vol. 1, March 2005, pp. 114–120 Vol. 1.

[114] D. Dong, I. Cvetkovic, D. Boroyevich, W. Zhang, R. Wang, and P. Mattavelli, “Grid-interface bidirectional converter for residential dc distribution systems-part one: High-density two-stage topology,” *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1655–1666, April 2013.

[115] M. A. Vitorino, L. F. S. Alves, R. Wang, and M. B. de Rossiter Corrła, “Low-frequency power decoupling in single-phase applications: A comprehensive overview,” *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 2892–2912, April 2017.

[116] H. Yuan, S. Li, W. Qi, S. Tan, and S. Hui, “On nonlinear control of single-phase converters with active power decoupling function,” *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5903–5915, June 2019.

[117] D. Neumayr, D. Bortis, and J. W. Kolar, “Ultra-compact power pulsation buffer for single-phase dc/ac converter systems,” in *IEEE International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, May 2016, pp. 2732–2741.

[118] Y. Tang and F. Blaabjerg, “A component-minimized single-phase active power decoupling circuit with reduced current stress to semiconductor switches,” *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 2905–2910, June 2015.

[119] S. Li, W. Qi, S. Tan, and S. Y. R. Hui, “Integration of an active filter and a single-phase ac/dc converter with reduced capacitance requirement and component count,” *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4121–4137, June 2016.

[120] L. Zhang, X. Ruan, and X. Ren, “Second-harmonic current reduction for two-stage inverter with boost-derived front-end converter: Control schemes and design considerations,” *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6361–6378, July 2018.

[121] J. M. Kwon, E. H. Kim, B. H. Kwon, and K. H. Nam, “High-efficiency fuel cell power conditioning system with input current ripple reduction,” *IEEE Transactions on Industrial Electronics*, vol. 56, no. 3, pp. 826–834, March 2009.

[122] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, “Overview of control and grid synchronization for distributed power generation systems,” *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1398–1409, Oct 2006.

[123] S. Eren, M. Pahlevani, A. Bakhshai, and P. Jain, “An adaptive droop dc-bus voltage controller for a grid-connected voltage source inverter with lcl filter,” *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 547–560, Feb 2015.

[124] L. Yang, Y. Chen, A. Luo, W. Wu, K. Huai, X. Zhou, L. Zhou, Q. Xu, and J. M. Guerrero, “Second ripple current suppression by two bandpass filters and current sharing method for energy storage converters in dc microgrid,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 3, pp. 1031–1044, Sept 2017.

[125] K. J. Lee, J. P. Lee, D. Shin, D. W. Yoo, and H. J. Kim, “A novel grid synchronization pll method based on adaptive low-pass notch filter for grid-connected pcs,” *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 292–301, Jan 2014.

[126] R. P. Venturini, P. Mattavelli, P. Zanchetta, and M. Sumner, “Adaptive selective compensation for variable frequency active power filters in more electrical aircraft,” *IEEE Transactions on Aerospace and Electronic Systems*, vol. 48, no. 2, pp. 1319–1328, April 2012.

[127] L. Corradini, P. Mattavelli, E. Tedeschi, and D. Trevisan, “High-bandwidth multisampled digitally controlled dc-dc converters using ripple compensation,” *IEEE Transactions on Industrial Electronics*, vol. 55, no. 4, pp. 1501–1508, April 2008.

[128] G. Zhu, X. Ruan, L. Zhang, and X. Wang, “On the reduction of second harmonic current and improvement of dynamic response for two-stage single-phase inverter,” *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 1028–1041, Feb 2015.

[129] S. Peyghami, H. Mokhtari, P. C. Loh, P. Davari, and F. Blaabjerg, “Distributed primary and secondary power sharing in a droop-controlled lvdc microgrid with merged ac and dc characteristics,” *IEEE Transactions on Smart Grid*, vol. 9, no. 3, pp. 2284–2294, May 2018.

[130] E. Rodriguez-Diaz, E. J. Palacios-Garcia, A. Anvari-Moghaddam, J. C. Vasquez, and J. M. Guerrero, “Real-time energy management system for a hybrid ac/dc residential microgrid,” in *2017 IEEE Second International Conference on DC Microgrids (ICDCM)*, June 2017, pp. 256–261.

[131] L. Xu and D. Chen, “Control and operation of a dc microgrid with variable generation and energy storage,” *IEEE Transactions on Power Delivery*, vol. 26, no. 4, pp. 2513–2522, Oct 2011.

[132] M. B. Delghavi and A. Yazdani, “A unified control strategy for electronically interfaced distributed energy resources,” *IEEE Transactions on Power Delivery*, vol. 27, no. 2, pp. 803–812, April 2012.

[133] J. Kim, J. M. Guerrero, P. Rodriguez, R. Teodorescu, and K. Nam, “Mode adaptive droop control with virtual output impedances for an inverter-based flexible ac microgrid,” *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 689–701, March 2011.

[134] S. Lissandron and P. Mattavelli, “A controller for the smooth transition from grid-connected to autonomous operation mode,” in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2014, pp. 4298–4305.

[135] S. Anand, B. G. Fernandes, and J. Guerrero, “Distributed control to ensure proportional load sharing and improve voltage regulation in low-voltage dc microgrids,” *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1900–1913, April 2013.

[136] D. H. Dam and H. H. Lee, “An adaptive power distributed control method to ensure proportional load power sharing in dc microgrid considering equivalent line impedances,” in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sept 2016, pp. 1–6.

[137] V. Nasirian, A. Davoudi, F. L. Lewis, and J. M. Guerrero, “Distributed adaptive droop control for dc distribution systems,” *IEEE Transactions on Energy Conversion*, vol. 29, no. 4, pp. 944–956, Dec 2014.

[138] P. Wang, X. Lu, X. Yang, W. Wang, and D. Xu, “An improved distributed secondary control method for dc microgrids with enhanced dynamic current sharing performance,” *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6658–6673, Sept 2016.

[139] D. Dong, T. Thacker, I. Cvetkovic, R. Burgos, D. Boroyevich, F. Wang, and G. Skutt, "Modes of operation and system-level control of single-phase bidirectional pwm converter for microgrid systems," *IEEE Transactions on Smart Grid*, vol. 3, no. 1, pp. 93–104, March 2012.