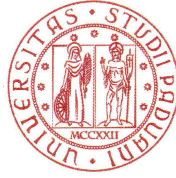

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DEGRADATION MECHANISMS OF DEVICES FOR OPTOELECTRONICS AND POWER ELECTRONICS BASED ON GALLIUM NITRIDE HETEROSTRUCTURES

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Abstract

Gallium Nitride is rapidly emerging as a promising material for electronic devices in various fields. Since it is a direct bandgap semiconductor it can be used for highly-efficient light emitting devices (Light Emitting Diodes and Laser Diodes) and the possibility of growing alloys containing Aluminum and Indium allow for the selection of the peak wavelength along the whole UV-green part of the radiation spectrum. Moreover, the high electron mobility, the ability of withstand high electric fields and the good thermal dissipation make GaN-based diodes and transistors devices with a good potential for high frequency and power applications. Before final products containing Gallium Nitride devices can permeate the international market, it is required to guarantee that they are reliable enough to have long lifetimes to appeal potential customers, and that their performance/cost relationship is superior compared to other competitors, at least in some specific fields of application. Aim of this thesis is to investigate the strong points of Gallium Nitrides by means of characterization and reliability tests on various different structures (LEDs, laser diodes, blocking diodes, HEMTs, GITs, MISs), in order to analyze the behavior of the material from different points of view.

Within this work is reported a detailed study of the gradual degradation of InGaN-based laser diodes and Light-Emitting Diodes submitted to electro-thermal stress. The purpose is to compare the behavior of the two devices by means of electro-optical measurements, electroluminescence characterization, near field emission measurements and Deep-Level Transient Spectroscopy (DLTS) investigation in order to give a deeper understanding of the mechanisms involved in LD degradation. Particular attention is given to the role of injection efficiency decrease and non-radiative recombination. The comparison of the degradation kinetics and an analysis of the degradation modes of the two device structures allowed a complete study of the phys-

ical mechanisms responsible for the degradation. It was found that the degradation of the devices can be ascribed to an increase of the defect density, which has a strong impact on non radiative recombination kinetics. The activation energy of the detected deep level is 0.35 - 0.45 eV. As an effect of combined electrical and thermal stress tests on commercially-available InGaN-based blue laser diodes, it has been found that sometimes there is an initial decrease of the threshold current, which is ascribed to the increase of the activation of p-type dopant, promoted by the temperature and the flow of minority carriers.

In order to investigate the effects of the creation of defects, two different commercial blue InGaN-based LEDs were submitted to 3 MeV proton irradiation at various fluencies (10^{11}, 10^{12} and 10^{13} p^+/cm^2). The degradation process was characterized by combined current-voltage (I - V), optical power-current (L - I) and capacitance-voltage (C - V) measurements, in order to investigate the changes induced by the irradiation and the recovery after annealing time at high temperature (150 ℃). The experimental data suggest the creation of non-radiative recombination centers near or into the active region of the LEDs, due to atomic displacement. This hypothesis is confirmed by the results of the recovery tests: the increase of the optical power and its correlation with the recovery of the forward current is consistent with the annealing of those defects.

Part of the activity on high electron mobility transistors was devoted to the realization of measurement setups in order to carry out novel characterization techniques. Were analyzed the advantages and limitations of the current-transient method used for the study of the deep levels in GaN-based high electron mobility transistors (HEMTs), by evaluating how the procedures adopted for measurement and data analysis can influence the results of the investigation. The choice of the measurement parameters (such as the voltage levels used to induce the trapping phenomena and monitor the current transients and the duration of the filling pulses) and of the analysis procedure (the method used for the extrapolation of the time constants of the processes) can influence the results of the drain current transient investigation and can provide information on the location of the trap levels responsible for current collapse. Moreover, was collected a database of defects described in more than

60 papers on GaN and its compounds, which can be used to extract information on the nature and origin of the traps in AlGaN/GaN HEMTs. Using this newly developed technique and other more common tests, several reliability and lifetime test were carried out on various structures, in order to gain a better understanding of their problematic aspects and possible improvements. One potential variation is the composition of the gate stack. Degradation tests were performed at Vgs = -5 V and increasing Vds levels on GaN HEMTs with different gate materials: Ni/Au/Ni, ITO and Ni/ITO. At each step of the stress experiment, the electrical and optical characteristics of the transistors were measured in order to analyze the degradation process. It was found that stress induces a permanent degradation of the gate diode, consisting in an increase in the leakage current. This change is due to the generation of parasitic conductive paths, as suggested by electroluminescence (EL) mapping, and devices based on ITO showed higher reliability. These data strongly support the hypothesis that the robustness is influenced by processing parameters and/or by the gate material, since all analyzed devices come from the same epitaxial wafer.

Other than varying the gate material, it is possible to add a p-type layer under the gate in order to achieve normally-off operation. This change produces a benefit in terms of performances, but can give birth to unusual trapping phenomena. It was carried out an extensive analysis of the time and field-dependent trapping processes that occur in GaN-based gate injection transistors exposed to high drain voltage levels. Results indicate that, even if the devices do not suffer from current collapse, continuous exposure to high drain voltages can induce a remarkable increase in the on-resistance (Ron). The increase in Ron can be recovered by leaving the device in rest conditions. Temperature-dependent analysis indicates that the activation energy of the detrapping process is equal to 0.47 eV. By time-resolved electroluminescence characterization, it is shown that this effect is related to the capture of electrons in the gate - drain access region. This is further confirmed by the fact that charge emission can be significantly accelerated through the injection of holes from the gate. A first-order model was developed to explain the time dependence of the trapping process. Using other deep levels characterization techniques, such as drain current transients, gate frequency sweeps and backgating, several other trap states were identified in

these devices. Their activation energies are 0.13, 0.14, 0.25, 0.47 and 0.51 eV.

During the accelerated lifetime tests of these devices, it was found a variation of the relative amplitude of the transconductance peaks, well correlated with the increase of the electroluminescence. This effect can be explained by the activation of the p-type dopant, a phenomenon which was detected also in laser diodes.

It is possible to develop diodes able to withstand very high reverse voltages using a similar structure, deprived of the gate region and with an additional Schottky diode (Natural superjunction). In this case, the activation energies of the detected deep levels were 0.35, 0.36, 0.44 and 0.47 eV. These values are very similar to the ones found in GITs, and this fact, along with the presence of the p-dopant activation in very different devices, confirms that it is useful to study different structures based on the same material in order to gain more knowledge on its performances, possibilities and reliability aspects.

Sommario

Il Nitruro di Gallio si sta rapidamente proponendo come un materiale promettente per dispositivi elettronici in vari campi applicativi. Dato che si tratta di un semiconduttore a *bandgap* diretto, può essere utilizzato per realizzare emettitori di radiazione luminosa altamente efficienti (LED e diodi laser), e la possibilità di realizzare leghe contenenti Alluminio e Indio permette di selezionare la lunghezza d'onda di picco all'interno dell'intervallo UV - verde dello spettro elettromagnetico. Prima che i prodotti finali basati su Nitruro di Gallio possano permeare il mercato internazionale, è necessario garantire che siano abbastanza affidabili da possedere lunghi tempi di vita ai fini di essere considerati da potenziali acquirenti, e che il loro rapporto prestazioni/costi sia superiore rispetto a quello dei dispositivi attualmente presenti nel mercato, almeno per alcune specifiche applicazioni. Lo scopo di questa tesi è analizzare i punti di forza dei materiali composti basati su Nitruro di Gallio tramite caratterizzazione e test affidabilistici su varie strutture differenti (LED, diodi laser, diodi bloccanti, HEMT, GIT, MIS), per comprendere il comportamento del materiale da diversi punti di vista.

In questo lavoro viene effettuato uno studio dettagliato del degrado graduale di LED e diodi laser in InGaN sottoposti a stress elettrotermici. lo scopo è di paragonare il comportamento delle due tipologie di dispositivi tramite caratterizzazione elettrica e ottica, elettroluminescenza, mappe di emissione in campo vicino e *Deep-Level Transient Spectroscopy* (DLTS), in modo da ottenere una comprensione profonda dei meccanismi di degrado che causano il calo di performance dei diodi laser. Un'attenzione particolare è rivolta al ruolo del calo dell'efficienza di iniezione e alla ricombinazione non-radiativa. Il confronto delle cinetiche di degrado e l'analisi del tipo di danno nelle due diverse strutture ha permesso uno studio completo dei meccanismi fisici responsabili del calo delle prestazioni. Il degrado dei dispositivi è stato attribuito ad

un aumento della concentrazione di difetti, che ha un forte impatto sulle cinetiche di ricombinazione non-radiativa. L'energia di attivazione del livello profondo rilevato è 0.35 - 0.45 eV. Come effetto dei test di vita accelerata elettrici e termici compiuti su diodi laser blu commerciali basati su InGaN, si è notato che a volte si ha un iniziale calo della corrente di soglia, dovuto all'aumento dell'attivazione del drogante di tipo p, promossa dalla temperatura e dal flusso di portatori minoritari.

Per comprendere gli effetti della creazione di difetti, due differenti tipologie di LED blu commerciali basati su InGaN sono stati sottoposti a irraggiamento tramite protoni con un'energia di 3 MeV a varie fluenze (10^{11}, 10^{12} and 10^{13} p^+/cm^2). Il processo di degrado è stato caratterizzato tramite misure corrente - tensione (I - V), potenza ottica - corrente (L - I) e capacità - tensione (C - V) combinate, per cercare di comprendere le modifiche indotte dall'irraggiamento e il recupero conseguente all'*annealing* ad alte temperature (150 ℃). I dati sperimentali suggeriscono la creazione di centri di ricombinazione non-radiativa vicino o all'interno della regione attiva dei LED, causati dallo spostamento di atomi. Questa ipotesi viene confermata dai risultati dei test di recupero: l'aumento della potenza ottica e la sua correlazione con il recupero della corrente diretta è consistente con l'*annealing* dei difetti.

Parte dell'attività sui transistor ad elevata mobilità elettronica è stata dedicata alla realizzazione di setup di misura che permettessero di utilizzare tecniche di caratterizzazione avanzata. Si sono analizzati i vantaggi e i limiti della metodologia dei transienti di corrente utilizzata per lo studio dei livelli profondi in HEMT basati su GaN, verificando in che modo diverse procedure adottate per la misurazione e l'analisi dei dati possano influenzare i risultati. La scelta dei parametri di misura (come i livelli di tensione utilizzati per indurre l'intrappolamento di carica e monitorare il transiente di corrente e la durata degli impulsi di *filling*) e della procedura di analisi (il metodo usato per l'estrapolazione delle costanti di tempo dei processi) può influenzare i risultati e può fornire informazioni sulla posizione degli stati trappola responsabili per il calo della corrente. Inoltre, è stato raccolto un database di difetti descritti in più di 60 articoli scientifici sul Nitruro di Gallio e i suoi composti, che può essere utilizzato per ottenere informazioni sulla natura e sull'origine delle trappole negli HEMT in AlGaN/GaN. Utilizzando questa tecnica innovativa e altri test

più comuni, sono stati condotti test affidabilistici e di tempo di vita su varie strutture, per ottenere una miglior comprensione delle loro problematiche e dei possibili miglioramenti. Una possibile variazione riguarda la composizione dello *stack* di gate. Sono stati condotti test di degrado a Vgs = -5 V e valori di Vds crescenti su HEMT in GaN con differenti materiali di gate: Ni/Au/Ni, ITO e Ni/ITO. Ad ogni passo dello stress sono state misurate le caratteristiche elettriche e ottiche dei transistor, per analizzare il processo di degrado. Si è trovato che lo stress causa un degrado permanente del diodo di gate, che consiste in un aumento della corrente di *leakage*. questo cambiamento è dovuto alla generazione di cammini conduttivi parassiti, come suggerito dalle misure di elettroluminescenza (EL), e dispositivi basati su ITO hanno mostrato un'affidabilità maggiore. Questi dati sostengono fortemente l'ipotesi che la robustezza è influenzata dai parametri di processo e/o dal materiale di gate, dato che tutti i dispositivi analizzati provengono dallo stesso wafer epitassiale.

Oltre a variare il materiale di gate, è possibile aggiungere uno strato di tipo p sotto il gate per ottenere un funzionamento *normally-off*. Questo cambiamento fornisce un incremento delle performance, ma può dar nascita a fenomeni di trapping particolari. Si è condotta un'accurata analisi dei processi di trapping dipendenti dal tempo e dal campo elettrico che si verificano nei transistor ad iniezione di corrente di gate (GIT) quando vengono sottoposti ad elevate tensioni di drain. I risultati indicano che, anche se i dispositivi non soffrono di cali di corrente per tempi brevi, l'esposizione continua a tensioni di drain elevate può indurre un aumento significativo della resistività in zona lineare (Ron). Il valore originario di Ron può essere recuperato lasciano il dispositivo a riposo. L'analisi della dipendenza dalla temperatura indica che l'energia di attivazione del processo di detrappolamento è pari a 0.47 eV. Tramite una caratterizzazione dell'elettroluminescenza risolta temporalmente, viene mostrato che questo effetto è correlato alla cattura di elettroni nella regione di accesso gate - drain. Questa interpretazione è inoltre confermata dal fatto che l'emissione della carica può essere significativamente accelerata attraverso l'iniezione di lacune dal gate. Un modello del primo ordine è stato sviluppato per spiegare la dipendenza dal tempo del processo di trapping. Utilizzando altre tecniche di caratterizzazione dei livelli profondi, come i transienti di corrente di drain, gli *sweep* di frequenza di gate e

il *backgating*, in questi dispositivi si sono identificati vari altri stati trappola. Le loro energie di attivazione sono 0.13, 0.14, 0.25, 0.47 e 0.51 eV.

Durante i test di vita accelerata di questi dispositivi, si è trovata una variazione dell'ampiezza relativa dei picchi di transconduttanza ben correlata con l'aumento dell'elettroluminescenza. Questo effetto può essere spiegato tramite l'attivazione del drogante p, un fenomeno che si è osservato anche nei diodi laser.

Utilizzando una struttura simile, è possibile realizzare diodi capaci di sopportare tensioni inverse molto elevate, rimuovendo la regione di gate e aggiungendo un diodo Schottky (Natural Superjunction). In questo caso, si sono rilevati livelli profondi di energia di attivazione 0.35, 0.36, 0.44 e 0.47 eV. Questi valori sono molto simili a quelli trovati nei GIT, e questo fatto, insieme alla presenza dell'ativazione del drogante p in dispositivi molto differenti tra loro, conferma l'utilità dello studio di differenti strutture basate sullo stesso materiale per ottenere una maggior conoscenza delle sue performance, possibilità e aspetti affidabilistici.

Introduction

The international market of the electronic devices is constantly looking for new technologies that can enhance its possible applicative fields, its energy consumption and its performances/cost ratio. A lot of attention has been drawn recently by the Gallium Nitride compounds system. Gallium Nitride is a direct bandgap semiconductor, so it can be used for the production of optoelectronic devices with an high power conversion efficiency from electrical to optical. Moreover, Aluminum and Indium can be used to form alloys with different energy gaps, which allows the tuning of the wavelength in the UV-green part of the electromagnetic spectrum and the creation of barriers for the electron and the holes. Gallium nitrides have an intrinsically high electron mobility, an high breakdown field and a very good thermal conductivity, and then can be used for the creation of highly reliable devices for radio frequency (RF) and high power applications.

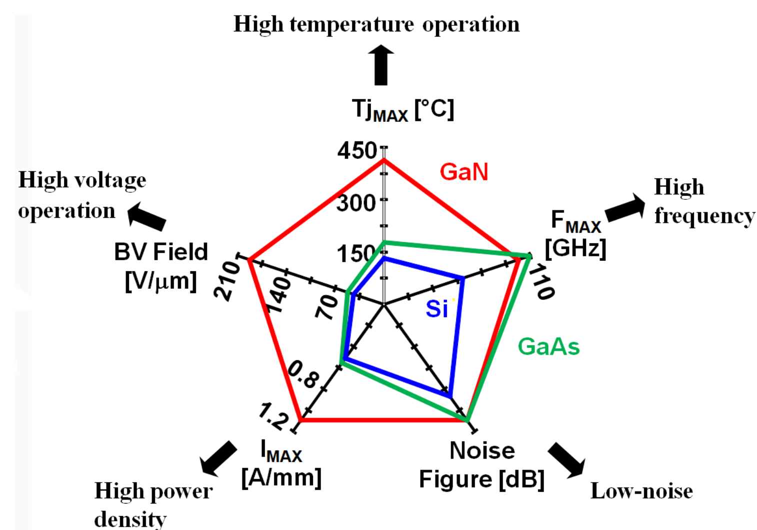


Figure 1: Comparison between the main physical parameters of Gallium Nitride and other semiconductor used for high-power and high-frequency electronics.

Given the large number of possible uses and different devices, it is useful to study the gallium nitrides at the material level, rather than at the device level, in order to share the knowledge acquired by means of very different characterization techniques on several peculiar structures. For this reason, in this thesis characterization and reliability tests have been carried out on LEDs, laser diodes, blocking diodes, HEMTs, GITs and MISs, and every one of this components has provided useful information for the comprehension of the behavior of Gallium Nitride compounds.

In order to give the reader all the information required to understand the experimental results and the general aim of the thesis, it has been structured as follows:

- *Chapter 1*: Here the Gallium Nitride system will be presented describing its nature and all the processes required to obtain a final device, such as the choice of the substrate, the various techniques that allow the growth of the GaN on it, the possible alloys with other chemical elements that can enhance its possible uses, the doping of the material, the design of the ohmic contacts, some useful intrinsic physical characteristics and the possible defect that can result from all these processes.

- *Chapter 2*: This chapter will review the basics of the optoelectronic devices, starting from their specific structure and production. The principles of the light emission process and of its efficiency will be described, along with the possible reliability issues, and will be covered some additional details on the difference between Light Emitting Diodes and Laser Diodes.

- *Chapter 3*: Similarly, a description of the functioning of an High Electron Mobility transistor will be provided, discussing the formation of the conductive channel, the gate leakage current, the trapping effects and the reliability aspects. Moreover, the structure and the basic operation of two novel devices (Gate Injection Transistor and Natural SuperJunction) analyzed through this thesis will be summarized.

- *Chapter 4*: In this chapter the reader will find an explanation of some characterization techniques used within this work, composed by their theoretical basis and their possible experimental results.

- *Chapter 5*: This part will report the experimental results of the tests carried out on optoelectronic devices. The effects induced by the irradiation with highly energetic protons will be analyzed, and the highlighted generation of defects will be found also in LEDs and LDs electro-thermally stressed during a split-wafer experiment. It will be provided experimental evidence of the additional dopant activation effect during the stress of commercial blue laser diodes.

- *Chapter 6*: This chapter covers the largest part of the research activity carried out during the Ph. D. It will be reported a comprehensive study of the trapping effects in Gate Injection Transistors, using different tests and in various conditions: a virtual gate effect caused by on-state trapping, the effect of the gate quiescent bias point on the current collapse, the identification of some deep levels using drain current transients, the newly-developed gate frequency sweeps employed to find out the performances of the devices in a real application and the use of backgating experiments to identify trap states located under the conductive channel. Once the defects have been described, it is possible to study the change of their concentration and the effects on the reliability of the devices during accelerated lifetime tests in both constant current and constant voltage condition, and during step-stress experiments in on- and off-state. The thermal resistance of the devices will be evaluated, since it is an important parameter that affects their robustness. In the latter part of the chapter, three different devices will be studied: the effect of the gate composition on the reliability of AlGaN/GaN HEMTs, the electrical and optical analysis of the trapping phenomena in Natural SuperJunctions and their degradation, and a possible issue that prevents the correct operation of Metal - Insulator - Semiconductor transistors.

Chapter 1

Main properties of Gallium Nitride

Gallium Nitride is a III/V compound semiconductor with direct bandgap. It is a widely-known material for optoelectronic devices and High Electron Mobility Transistor. The development of systems based on Gallium Nitride allowed for the production of light emitting diodes and laser diodes in the blue-green band and in the deep UV, and of transistors for high frequency operation and power electronics able to withstand high electric fields. Its very stable chemical structure and its high thermal conductivity ensure a good reliability in a wide field of application. The creation of alloys containing Aluminum and Indium enhances the possible uses: it is possible to have layers with different values of energy gap in order to create barriers or tune the emission wavelength and the refractive index.

The choice of the best substrate and growth process is not an easy task, due to lattice mismatch, defects, impurities and other secondary effects that can worsen the performances and reliability of the devices. The use of various chemical species for the doping of the material allows for a finer customization of the electrical and optical properties, but it introduces an aleatory process in the design and causes additional defects. Moreover, electrical contacts to the surrounding elements require band alignment in order to achieve ohmic behavior, and this adds another design condition and growth step. In the following we will discuss this problems and features.

1.1 Gallium Nitride crystals

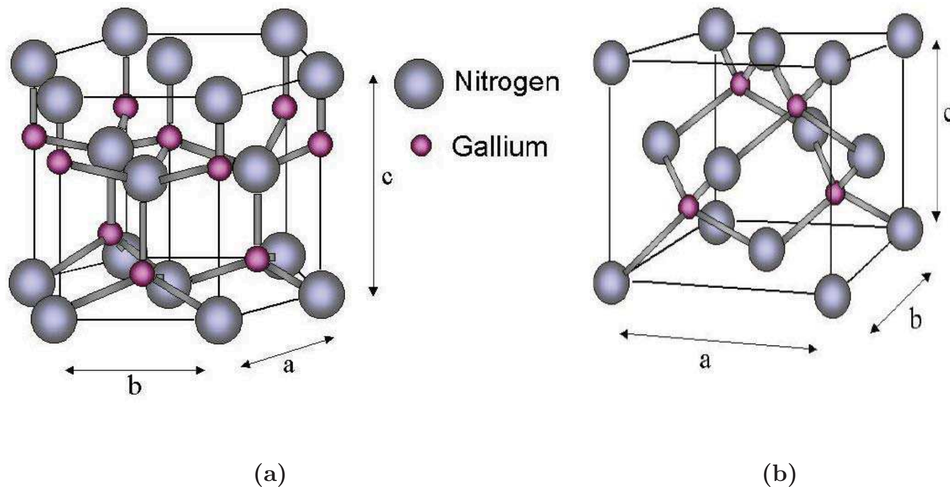
Even if the easiest structure that can be grown is the amorphous one, what we would like to obtain is a Gallium Nitride crystal. Crystals allow for the most isotropic

and spatially-invariant behavior (at least when we are taking into account lattice planes described by the same Miller indices), and for the best electrical and optical properties, thanks to their repetitive configuration.

Al-In-GaN compounds can take two different crystal structures, the wurtzite and the zincblende. In both cases the structure has tetrahedral coordination with a Gallium atom at the center, but the primitive unit cell is different. As a brief summary, we should remember that the cell could be fully described by two terns of numbers: the distances between the atoms in three directions that are a basis of the space (a, b, c) and the angles between these directions (α, β, γ), where γ is the angle $\widehat{ab}$ and so on.

- Zincblende has identical lattice vectors $a = b = c$ and orthogonal directions $\alpha = \beta = \gamma = 90°$. The unit cell follows the face-centered cubic bravais lattice, the vertices of the regular tetrahedron are occupied by the Nitrogen, whereas the Gallium links them together inside the cell.

- Wurtzite has $a = b \neq c$, $\alpha = \beta = 90°$ and $\gamma = 120°$. It has an hexagonal structure composed by successive layers of Gallium and Nitrogen along the c-axis.



(a) (b)

Figure 1.1: Visualization of wurtzite and zincblende structures

Figure 1.1 shows the pattern of the atoms in a wurtzite (a) and zincblende (b) crystal structure. The high binding energy of both structures is the reason for the

good stability of the Gallium Nitride, because it makes the formation of dislocations and lattice defects less likely.

The electrical and optical properties of a semiconductor are strongly dependent on its lattice structure, since the band diagram is a consequence of the formation of the molecular orbital, whose shape and energy comes from the characteristics of the original orbitals of each atom. As an example, in a first approximation the smaller the lattice vectors, the higher the energy gap. This can explain the relationship between energy gap and temperature: at higher temperatures the thermal vibration of the atoms is stronger, so we have a larger structure with smaller energy gap. The band structure of Gallium Nitride in the first Brillouin zone is reported in figure 1.2.

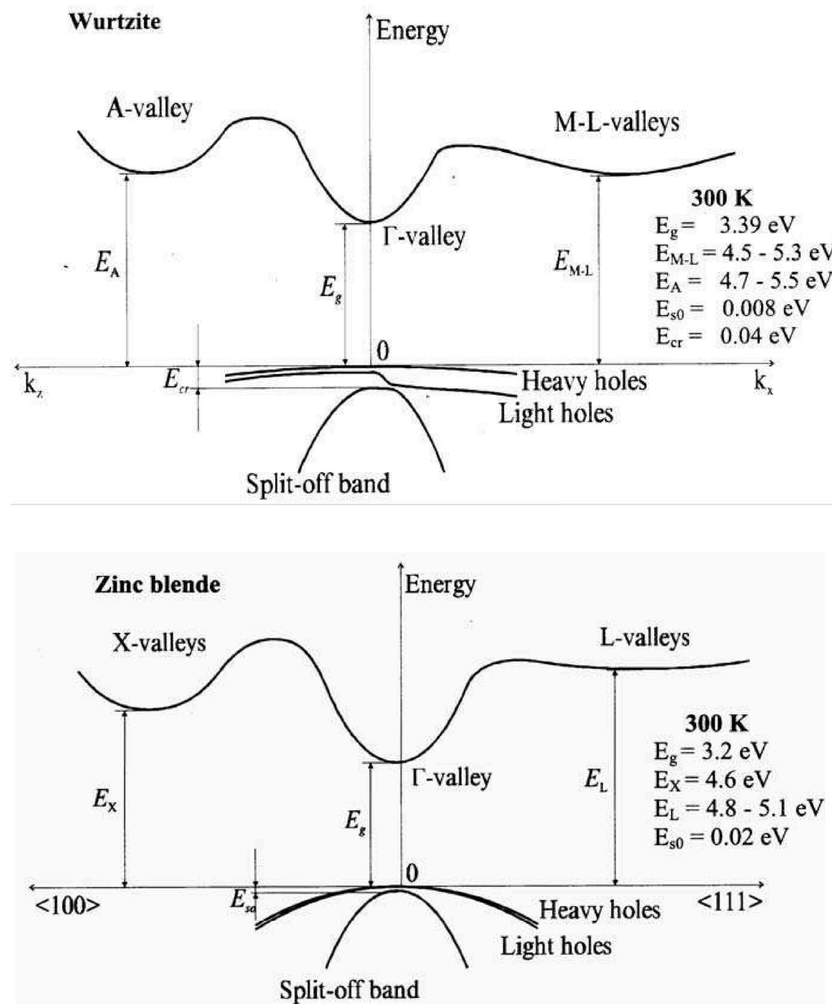


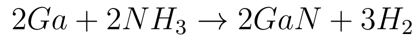
Figure 1.2: Wurtzite and zincblende band diagrams in the first Brillouin zone

For an electronic or optoelectronic device the most important transition is the fundamental one, i.e. from the maximum of the valence band to the minimum of the conduction band near the Γ-valley. The corresponding energy value of the prohibited gap is 3.504 eV, which gives a wavelength of 355 nm in the vacuum. Table 1.1 lists several important physical parameters for the Gallium Nitride and other materials used in the semiconductor technology.

Property (300°K)		Ge	Si	GaAs	GaP	GaN
Crystal structure	D = Diamond Z = Zincblende W = Wurtzite	D	D	Z	Z	W Z
Energy Gap	D = Direct I = Indirect	I	I	D	I	D
Lattice constants	$a_0 = b_0$ [Å] c_0 [Å]	5.64	5.43	5.65	5.45	3.19 4.52 5.19 4.52
Bandgap energy	$E_g\,[eV]$	0.66	1.12	1.42	2.26	3.39
Temperature dependence	$\frac{dE_g}{dT}\,[\times 10^{-4}\,\frac{eV}{^\circ K}]$	-3.7	-2.7	-5	-5.4	-6
Intrinsic carriers concentration	$n_i\,[cm^{-3}]$	$2 \cdot 10^{13}$	$1 \cdot 10^{10}$	$2 \cdot 10^{16}$	$1.6 \cdot 10^{10}$	$1.9 \cdot 10^{10}$
Electron mobility	$\mu_n\,[\frac{cm^2}{V \cdot s}]$	3900	1350	8500	110	2000
Hole mobility	$\mu_p\,[\frac{cm^2}{V \cdot s}]$	1900	450	400	75	30
Electron diffusion constant	$D_n\,[\frac{cm^2}{s}]$	101	39	220	2.9	39
Hole diffusion constant	$D_p\,[\frac{cm^2}{s}]$	49	12	10	2	0.75
Electron affinity	$\chi\,[V]$	4.0	4.05	4.07	≈ 4.3	4.1
Refractive index	n_{opt}	4.0	3.3	3.4	3.3	2.5
Breakdown field	$\epsilon_1\,[\times 10^5\,\frac{V}{cm}]$	0.8	3	3.5	≈ 10	33
Thermal conductivity	$k\,[\frac{W}{cm \cdot ^\circ K}]$	0.606	1.412	0.455	0.97	1.5

Table 1.1: Physical parameters of several semiconductors

Gallium Nitride was synthesized for the first time in 1928 by Johnson, using a chemical reaction between Gallium and Ammonia:



$$2Ga + 2NH_3 \rightarrow 2GaN + 3H_2$$

Maruska and Tietjien in 1969 were able to develop a more efficient technique of epitaxial growth using Gallium Chloride and Ammonia:

$$GaCl + NH_3 \rightarrow GaN + HCl + 3H_2$$

achieving good growth rates. Akasaki in 1986 was able to produce good quality GaN using buffer layers over a Sapphire substrate, and subsequently succeeded in activating the p-type dopants (Magnesium) using a technique called LEEBI (Low Energy Electron Beam Irradiation). All the requirements were met for the production of the first blue Light Emitting Diode based on a p-n junction (Amano 1989), but it was in 1994 that Nakamura was able to create a device with an efficiency high enough to be used in a real application, using for the first time a double heterostructure.

1.2 Substrates

One of the main problems in the growth of Gallium Nitride is the necessity of heteroepitaxy, which means that the epitaxial layer is grown as an overlayer on a different substrate [1]. This is a problem that Gallium Nitride shares with other compound semiconductors, which causes a great variability in the characteristics of the epitaxial film when different substrates are used. The number and type of dislocation and the lattice stress can vary greatly when materials with various lattice constants and thermal expansion coefficients are employed. In the following we will analyze the typical substrates for electronic and optoelectronic devices.

1.2.1 Sapphire (Al_2O_3)

Sapphire has been the first material used as a substrate for growth of Gallium Nitride. It has a low cost compared to other materials, an hexagonal structure such as wurtzite GaN and a good thermal and mechanical stability [2].

Among those advantages there is also a drawback: the mismatch between Sapphire and GaN (16% lattice mismatch and 39% thermal mismatch) causes a great number of defects during the growth and the temperature differences of the various processes. Figure 1.3 shows the different atomic structure at the interface, even if in a zone where

no defects propagate into the overlaying GaN. A method commonly used in order to mitigate this problem is the insertion of a buffer layer between the two materials, which gives a less abrupt transition. This process was developed by Akasaki and gave a great increase of the electron mobility, nearly by an order of magnitude, and a reduction equal to two orders of magnitude of the free carriers concentration in the GaN layer [3]. Moreover, Sapphire is an electrical insulator: the contacts must be placed on the upper surface of the device. This can be a problem for optoelectronic applications, since the contacts may screen part of the photons, and a smaller size of the contacts increases the effects of the current-crowding phenomenon, which will be described later.

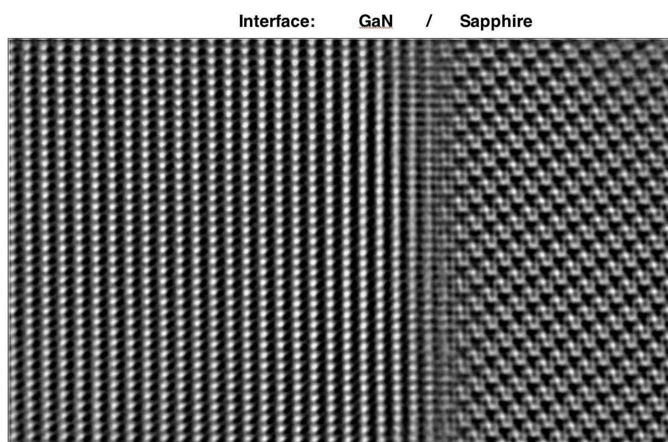


Figure 1.3: Interface and mismatch between GaN and Sapphire

1.2.2 Silicon Carbide (SiC)

Silicon Carbide has several characteristics that make it preferable and more performing than Sapphire:

- Lattice (3.5%) and thermal (3.2%) mismatches are lower, meaning that less defects are created during the various growth steps.
- The high electrical conductivity allows for smaller chip dimensions, easier an more economic to produce.
- The high thermal conductivity gives a better heat dissipation, increasing the performances, reliability and field of application (very high power electronics)

of the devices.

- The presence of preferential crystallographic directions for the splitting of the material produces easily very clean surfaces, with little roughness and low deviation from the ideal disposition of the atoms inside the lattice [4].

This material has also some drawbacks: Silicon Carbide has an high cost and requires very high fabrication temperatures [5].

Parameter	Sapphire Al_2O_3	Silicon Carbide $6H - SiC$
Symmetry	Hexagonal	Hexagonal
Lattice constant $a = b$	4.758 Å	3.08 Å
Lattice constant c	12.99 Å	15.12 Å
Density	$3.98\, g/mm^3$	$3.21\, g/mm^3$
Melting point	2050 ℃	2850 ℃
Specific heat capacity at 20℃	$0.16\, cal/g$	$0.16\, cal/g$
Heat capacity	$16.32\, cal/mol\,^\circ K$	$6.4\, cal/mol\,^\circ K$
Thermal conductivity	$0.412\, W/cm\,^\circ K$	$4.9\, W/cm\,^\circ K$
Coefficient of thermal expansion		
a	$7.5 \times 10^{-6}\,^\circ K^{-1}$	$4.68 \times 10^{-6}\,^\circ K^{-1}$
c	$8.5 \times 10^{-6}\,^\circ K^{-1}$	$4.2 \times 10^{-6}\,^\circ K^{-1}$
Density of defects at the interface	10^8–$10^{10}\, cm^{-2}$	10^8–$10^{10}\, cm^{-2}$

Table 1.2: Comparison between Sapphire and Silicon Carbide

1.2.3 Silicon (Si)

The use of Silicon substrates is the most cost-efficient solution: thanks to the great improvements in the fabrication of integrated circuits ant to its wide use, a Silicon wafer has typically a very high quality, good chemical and physical characteristics and a modest cost.

The better quality of Silicon crystals is offset by higher mismatches and by the formation of a superficial amorphous layer in the presence of Nitrogen. GaN layers grown on Silicon have an high defect concentration, so it is typically not used for optoelectronic devices (due to the increase of the non-radiative recombination). It is used more often as a substrate for electronics, because the higher number of defects is non as a critical factor as it is for light emitting devices.

1.2.4 Gallium Nitride (GaN)

As it should be obvious, a lot of the previous problems can be solved using homoepitaxy, i.e. growing the device on a substrate made by the same material.

This technique has a lot of critical aspects that make it difficult to obtain crystals of useful size. Better results have been achieved at the end of the 90s, using GaN produced through heteroepitaxy as a base for the subsequent homoepitaxial growth. The number of different variations that employ this principle is very high, but all of them suggest the use of a Hydrogen Vapour Phase Epitaxy, because it ensures a good speed.

Kelly et al. in '99 suggest a technique called *laser-induced liftoff* in order to separate the Gallium Nitride from the Sapphire [6]. This technique employs high power laser pulses through the Sapphire to thermally dissociate the interface and separate the materials (figure 1.4). The wafer they obtained was 275 μm thick and had a two inch diameter: a good result, suitable as a base for the subsequent growth.

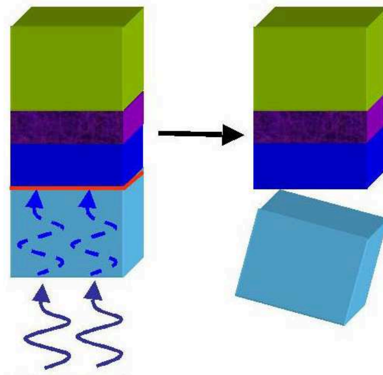


Figure 1.4: Laser-induced liftoff principle

Oshima et al. in 2003 presented another separation technique, the *void assisted separation* [1]. A GaN layer 300 nm thick is over a Sapphire substrate grown by Metal-Organic Vapor Phase Epitaxy. On this layer 20 nm of Titanium is deposited, and after a 30 minutes annealing in an atmosphere containing molecular Hydrogen and Nitrogen it creates a net-shaped layer of Titanium Nitride, where the holes are 20 - 30 nm wide. These holes lead to the formation, in the first moments of the later growth stage by HVPE of 300 nm Gallium Nitride, of GaN islands which subsequently merge to form a single layer. At the interface GaN/TiN/GaN, however, remain a number

of gaps, which allow to remove the GaN grown by HVPE through the application of a weak force. The layer of Gallium Nitride thus obtained has a low density of dislocations (5×10^6 cm^{-3}), since defects are blocked by the Titanium Nitride net.

The analysis of the wafers obtained with these techniques show that crystals of GaN have a good homogeneity and low residual stress, leading to having electrical and optical characteristics that differ little from the desired ones, and good reliability. Furthermore, the surface has less curvature than the one obtained on substrates of sapphire, making the subsequent fabrication steps easier.

1.3 Growth techniques

The manufacture of electronic devices typically involves some common steps: growth of different semiconductor layers, often different one from the another, over a suitable substrate, the cutting of the wafer, the realization of the contacts and encapsulation in a transparent plastic (in the case of light emitting devices) or other types of package (in the case of RF or power devices).

1.3.1 Hydrogen Vapour Phase Epitaxy (HVPE)

This was one of the first techniques used for the growth of GaN, and typically uses Sapphire substrates [7]. The atoms to be deposited, which must be in the gas phase as the name of the technique implies, come from very common materials: Ammonia (NH_3) for Nitrogen and a reaction between metallic gallium and hydrochloric acid (HCl) for the gallium. The room for the reaction is typically brought to a temperature of about 850 ℃, and the reaction takes place in an atmosphere of molecular Nitrogen or Hydrogen according to the equation:

$$GaCl(g) + NH_3(g) \longrightarrow GaN(s) + HCl(g) + H_2(g)$$

The growth rate that can be obtained is relatively high (30 - 130 μm/h) but the layers obtained have a lattice with a lot of defects, which led to the abandonment of this technique in the 80s. Lately this technique is coming back into favor because it allows to obtain thick layers of GaN to use as substrate for the homoepitaxial growth, without the GaN grown subsequently retains the large concentration of defects in the predecessor [8].

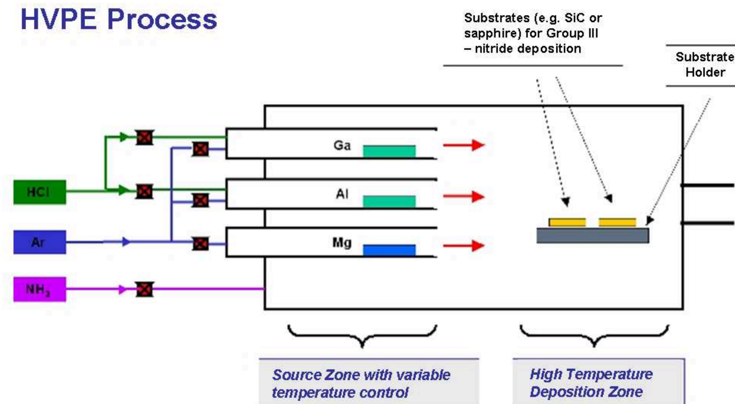


Figure 1.5: Basics of HVPE process

1.3.2 Epitaxial Lateral Overgrowth (ELO)

The basis of the technique *Epitaxial Lateral Overgrowth* is the HVPE technique, which provides a small amount of GaN (called "seed") over a Sapphire substrate (which will later be removed with laser-induced liftoff or taking advantage of the different thermal expansion coefficients of the interface). From the seed, the growth continues laterally creating a structure called the "wing".

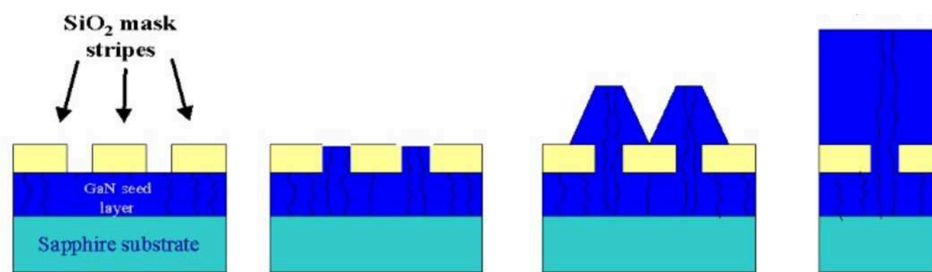


Figure 1.6: Use of seeds and growth of the wings

To speed up the growth a lot of seeds must be used, so in the resulting material defects are concentrated at the meeting point of two wings from different seeds, as well as in the seeds as intrinsic characteristic of the HVPE growth. The realization of the seeds takes advantage of masks of silicon oxide that select the region where the seed is grown, and are then removed along with the excess GaN [9].

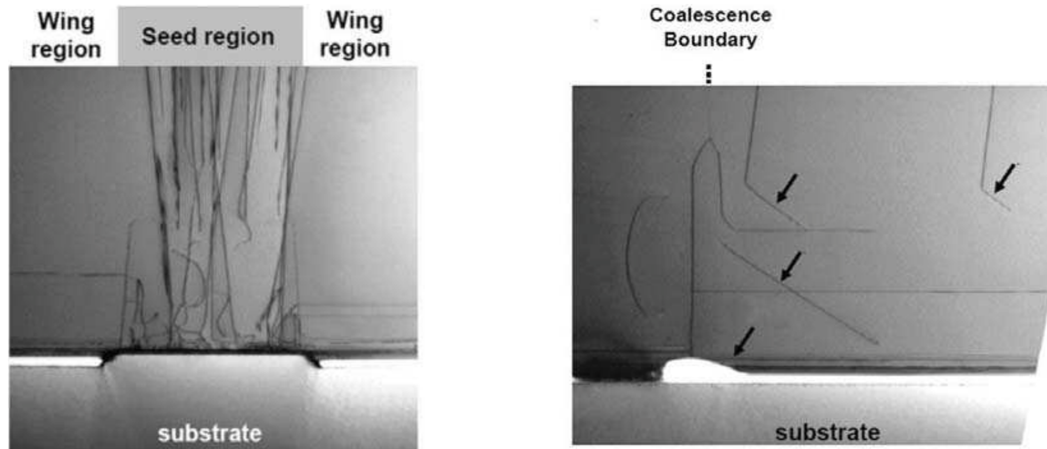


Figure 1.7: Electron microscope image showing the propagation of defects and meeting areas

1.3.3 Molecular Beam Epitaxy (MBE)

This technique is one of the most used for the growth of Nitrogen compounds , compounds of elements of the II-VI group and Silicon. Initially, in the growth of Gallium Nitride was it not possible to use molecular Nitrogen as a source, due to its high binding energy. It was used Ammonia (NH_3), which is another material quite common and inexpensive. Later it was possible to dissociate the N_2 by plasma sources (*Plasma assisted MBE*, PMBE). This step can take place before the Nitrogen reaches the substrate, thus allowing to adjust the temperature of growth independently of that required to break the bonds of the molecule of N_2. In the growth chamber the pressure must be kept very low, below 10^{-10} torr; Gallium is obtained via thermal evaporation, while the atomic Nitrogen is obtained in one of the ways described above and subsequently introduced into the chamber. Temperatures vary from a minimum of 600 ℃ to a maximum of 800 ℃, thus facilitating the introduction into the GaN of volatile elements such as Indium and Magnesium.

The (relatively) low growth temperatures allow to reduce the formation of lattice defects due to the thermal mismatch between the substrate and the layer of GaN grown on it. The low temperature, however, makes the growth of the GaN rather slow (50 nm/h). It is possible to increase the temperature to speed the growth, but this would lead to a surface of poor quality, a high concentration of free carriers or even a layer of semi-insulating GaN, due to the generation of compensating deep

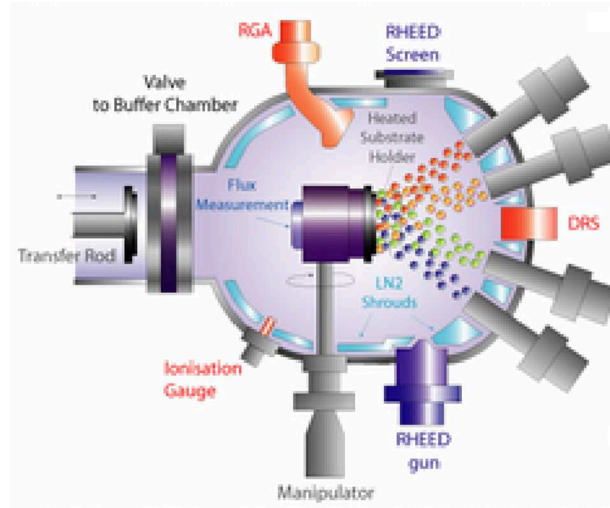


Figure 1.8: MBE growth chamber

levels. Summarizing, the advantages of this technique are:

- very simple reaction between elemental compounds readily obtainable;
- ability to constantly monitor the surface structure during growth;
- low unwanted doping level, using a low pressure;
- low growth temperatures;
- a better chance to have a good control of ultra-thin layers.

The heteroepitaxial growth by MBE of GaN on Sapphire or Silicon Carbide, however, fails to match the excellence of the electrical and optical characteristics obtained through another growth process, the *Metal-Organic Vapor Phase Epitaxy* (MOVPE). Anyway, using a first layer as a buffer grown by MOVPE, you can get good quality even through MBE [10]. Moreover, using a GaN substrate the quality of the layers grown by MBE exceeds that of the layers obtained by MOVPE.

Currently the main use of this technique lies in the easier growth of InGaN layers and layers of GaN doped with Magnesium, since, thanks to the low temperatures used, post-growth annealing treatments to reactivate acceptors are not necessary. Furthermore, the use of Nitrogen instead of Ammonia avoids bringing into contact the Magnesium, which acts as a dopant, with the Hydrogen, which could cause it to passivate and to create various complexes that act as deep levels.

1.3.4 Metal-Organic Chemical Vapour Deposition (MOCVD)

The MOCVD technique exploits the chemical reactions that occur at high temperature between the elements of the III-V group . While the reactants are in the gas phase, the products are in the solid phase and are deposited gradually on the substrate, thus allowing a gradual growth of the material controlled by the influx of the reactants. The choice of precursors for the elements that we want to depose falls on Trimethylgallium ($Ga(CH_3)_3$), Trimethylaluminum ($Al(CH_3)_3$), Trimethylindium ($In(CH_3)_3$) and Ammonia (NH_3); these materials are in fact relatively common or easy to produce, and allow to obtain as reaction products, in addition to the atoms to be deposited, other gaseous compounds that then can be easily removed from the growth region. The transport of various materials is via fluxes of molecular Nitrogen or Hydrogen [11]. To obtain good growth rates the temperatures must be maintained slightly higher compared to previous techniques: the substrate, placed on a graphite support, is initially heated to about 1100 ℃, to then be cooled to 450 ℃ for the growth of a buffer layer and subsequently got to about 1100 ℃ to speed the growth of GaN.

A slight modification was introduced by Nakamura, giving birth to the technique called *two-flow MOCVD* (TF-MOCVD) [12]. As the name suggests, two different gas flows are used: the first is sent in parallel and close to the substrate, carrying the reagents already described, while the second (composed of molecular Nitrogen and Hydrogen) flows from the top to the substrate with the task of distributing the reagents in a uniform manner and thus make the growth more homogeneous. The temperatures involved are essentially the same of the “base” version of the technique.

These techniques allows to obtain layers of good quality, with acceptable density of surface dislocations ($\approx 10^9$ cm^{-2}) and a decent growth rate. A problem not to be overlooked is the presence of Hydrogen in the reaction chamber, which we will see later have a passivating effect on Magnesium, as well as the difficulty of growing up with good quality thin layers contain Indium.

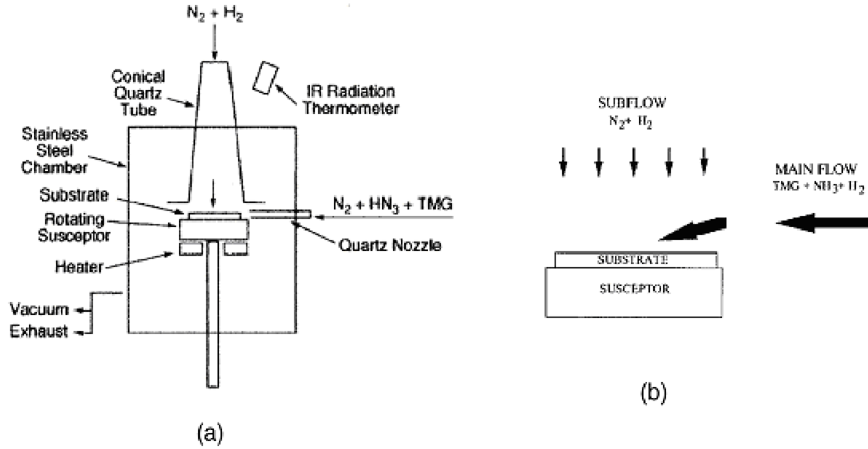


Figure 1.9: TF-MOCVD reactor (a) and diagram of the double flow (b)

1.3.5 Migration Enhanced Metal-Organic Chemical Vapour Deposition (MEMOCVD)

An improvement over the MOCVD technique has been recently developed by the company SETI (*Sensor Electronic Technology Inc.*) [13]. This new technique enables the growth of epitaxial layers AlN/GaN/InN and heterostructures with a good control over the thickness of the layers, and also allows to use lower temperatures than the MOCVD. The precursors used for Ga, Al, In, and N are again Trimethylgallium (TMGa), Trimethylaluminum (TMAl), Trimethylindium (TMIn) and Ammonia.

The principle of operation of MEMOCVD is similar to that of the *Pulsed Atomic Layer Epitaxy* (PALE), which deposits quaternary layers $Al_xIn_yGa_{1-x-y}N$ thanks to the repetition of pulses of the atoms to be deposited. While in PALE the duration of each pulse is fixed, the duration and shape of the pulses in MEMOCVD is optimized, and the pulses may overlap. MEMOCVD allows to achieve an high growth rate for the buffer layers with a reduction in the growth temperature (less than 150 °C) and an increase in the quality of the active zone.

1.4 GaN alloys

The construction of heterostructures and the choice of the wavelength of the radiation require the ability to modify the bandgap energy of the material, and this can be done by forming alloys with other materials with different electrical characteristics.

The main materials used in the GaN system are the Aluminum and Indium, because they allow to create high barriers and to extend the spectrum in a very wide range (from infrared to the far ultraviolet), forming at the same time very stable alloys with GaN.

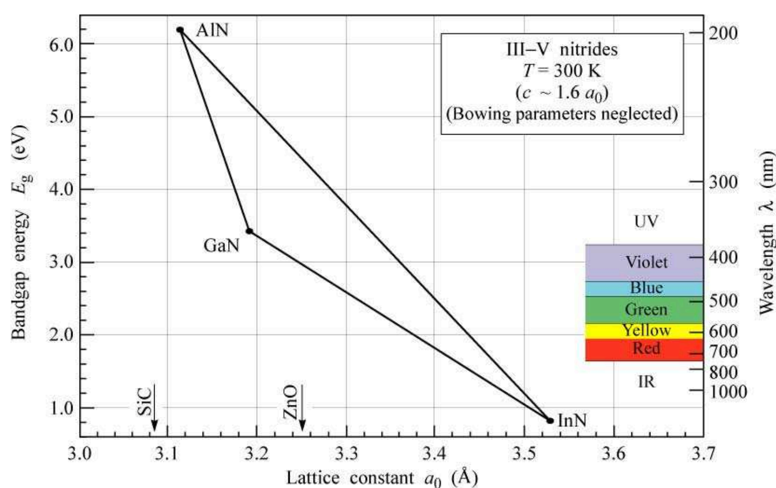


Figure 1.10: Variation of energy gap as a function of composition

1.4.1 Aluminum Nitride

The energy gap of Aluminum Nitride is 6.2 eV, so it is practically an insulator if the layer is too thick. However, if the fraction of Al is small, the alloy of AlGaN that is formed, possessing a bandgap greater than that of GaN, can be used as a barrier for the confinement of the carriers and consequently for the creation of gate barriers and quantum well structures.

Other positive features are the low lattice mismatch (2.4%) and the high melting point, which are the basis of the good characteristics and of the lattice stability already highlighted.

A critical issue for the AlN is in the moment of its deposition: the Aluminum is an extremely reactive material, so the deposition should be carried out in a controlled atmosphere (and in particular devoid of Oxygen) to avoid the formation of impurities which alter the electrical behavior and will reduce the reliability.

1.4.2 Indium Nitride

The Indium Nitride, as a counterpart of the Aluminum Nitride, instead has a very small energy gap, equivalent to about 0.7 - 0.8 eV [14]. The InGaN is therefore a good candidate to form the quantum well of a LED, with emission energies that vary with continuity, depending on the relative concentrations, between 3.44 and 0.8 eV (corresponding to wavelengths between red and near ultraviolet) [15].

Indium Nitride, however, presents an higher lattice mismatch (11%) and a relatively low dissociation temperature of Nitrogen and Indium (≈ 600 °K). This makes it difficult to create layers of InGaN with a good quality, which in fact are always made with concentrations of indium lower than 0.4 [16].

The Indium Nitride has the additional problem of growing spontaneously with a unintentional type-n doping, but in contrast to what happens for the GaN can be easily converted into a type-p doping by the addition of Magnesium. For all these reasons, the layers of InGaN typically have a high amount of defects, proportional to the concentration of indium [17], which increase trapping effects and reduce the radiative efficiency [18].

Property (300°K)	GaN	AlN	InN
Bandgap	$3.44\,eV$	$6.23\,eV$	$1.89\,eV$
dE_g/dT	$-6 \cdot 10^{-4}\,eV/{}^\circ K$	$-5.5 \cdot 10^{-4}\,eV/{}^\circ K$	$1.8 \cdot 10^{-4}\,eV/{}^\circ K$
Lattice constant a	$0.3189\,nm$	$0.3112\,nm$	$0.3548\,nm$
Lattice constant c	$0.5186\,nm$	$0.4982\,nm$	$0.5760\,nm$
Thermal conductivity	$1.3\,W/cm\,{}^\circ K$	$2.0\,W/cm\,{}^\circ K$	$0.8\,W/cm\,{}^\circ K$
Thermal expansion	$\frac{\Delta a}{a} = 5.59 \cdot 10^{-6}\,{}^\circ K^{-1}$ $\frac{\Delta c}{c} = 3.17 \cdot 10^{-6}\,{}^\circ K^{-1}$	$\frac{\Delta a}{a} = 4.2 \cdot 10^{-6}\,{}^\circ K^{-1}$ $\frac{\Delta c}{c} = 5.3 \cdot 10^{-6}\,{}^\circ K^{-1}$	$\frac{\Delta a}{a} = 3.8 \cdot 10^{-6}\,{}^\circ K^{-1}$ $\frac{\Delta c}{c} = 2.9 \cdot 10^{-6}\,{}^\circ K^{-1}$
Dielectric constant ϵ_0	9.5	8.5	15.3
Saturation velocity	$2.9 \cdot 10^7\,cm/s$	-	$4.2 \cdot 10^7\,cm/s$
Electron mobility	$9000\,cm^2/Vs$	$300\,cm^2/Vs$	$4400\,cm^2/Vs$
Melting point	2500 °C	3200 °C	550 °C

Table 1.3: Physical properties of the main III-V nitrides [10]

1.5 GaN doping

The doping processes of Gallium Nitride have some critical points derived from the inherent characteristics of the material, which make it difficult to get layers of good

quality both type-n and -p needed for the construction of electronic and optoelectronic devices.

1.5.1 n-type doping

The gallium nitride grows possessing an intrinsic n-type doping, independently on the deposition technique that instead varies the doping concentration (along with other process parameters such as the type of the substrate, the characteristics of the buffer layer and the post - growth processing). The cause of this intrinsic doping is still under investigation: some papers report that it results from defects in the crystal lattice, such as Nitrogen vacancies [12] [15], while others say that it originated from entrapment of Oxygen impurities in the crystal lattice [7] [19].

This intrinsic doping can not be used for a device, due to the absence of control on its concentration in the production phase, and therefore constitutes a problem for the realization of concentrations defined by the designer. Fortunately, by using the TF-MOCVD technique it is possible to obtain layers with very low concentrations of intrinsic doping. It is then possible to proceed to type-n doping with the implantation of Germanium or Silicon , which act as shallow donors within the forbidden gap. The dopant is entered in the reaction chamber in gaseous form (GeH_4 or SiH_4, respectively for Germanium or Silicon), and is reacted with the Trimethylgallium and Ammonia . Currently it is possible to reach concentrations of free carriers between 10^{17} and 10^{20} cm^{-3} [20], and using Silicon it is possible to obtain concentrations an order of magnitude higher than with the use of Germanium [12]. Having greater possibility of doping, the Silicon is the dopant that is routinely used.

1.5.2 p-type doping

As mentioned above, a major problem that has historically prevented the realization of GaN devices is the p-type doping. There was also the problem of compensating the intrinsic doping of the material, and then the high amounts of implanted dopants caused a number of lattice defects and a decrease in mobility that renders the material unusable for achieving efficient devices [21].

A first solution was proposed by Amano, who obtained the p-GaN by MOCVD,

using Magnesium as dopant and subjecting the layer to a LEEBI treatment (*Low Energy Electron Beam Irradiation*) [22]. This allowed him to obtain concentrations of holes up to 10^{17} cm^{-3}, while having minimum resistivity values of about 12 Ωcm [23]. The effect of LEEBI treatment was initially interpreted as follows: the interaction between the irradiated electrons and the crystal lattice allowed to move atoms of Magnesium from the interstitial positions they initially occupied to positions that were part of the lattice, resulting in their activation.

The next step was accomplished by Nakamura, who in 1992 succeeded in obtaining a layer of p-type GaN with good efficiency using post-growth annealing at 700 ℃ in an atmosphere of molecular Nitrogen [24]. A curious fact is that the process is reversible: if the layer thus obtained is subjected to a further annealing in NH_3 atmosphere the material returned to the high initial resistivity values. It was therefore suggested that doping was made difficult by the presence of Hydrogen atoms that bind with Magnesium passivating it (remember that, even if the molecular Hydrogen is chemically stable, the same is not true for Hydrogen ions, which in fact have been found able to form bonds with the Magnesium even at room temperature or slightly higher). This treatment made it possible to overcome some of the technical problems of the LEEBI technique. First, the treated layer of GaN was only the one within the depth of penetration of the electron beam in the crystal (approximately 0.2 μm), while with the annealing it is possible to obtain layers of good quality thick up to 4 μm. In addition, the real effect of the LEEBI technique is to break the bonds between the Hydrogen and the Magnesium with a reaction $MgH + MgH \rightarrow Mg + MgH_2$ and subsequently dissociate even the MgH_2 leaving the hydrogen inside the layer [23], this does not happen with the annealing that allows to expel the Hydrogen from the material.

Even the annealing, however, has its flaws. The high temperature at which the material must be brought in order to break the bonds between Magnesium and Hydrogen is typically detrimental (and in certain cases even destructive [25]) for the material, introducing a high number of lattice defects. Carrying out the annealing in an atmosphere of molecular Oxygen instead of Nitrogen, the temperature can be reduced (Hydrogen reacts with Oxygen to form water, which is removed preventing

Hydrogen to further interact with the material [26]), but we must also consider the interaction of the Oxygen with the grown layer and the substrate.

1.6 Ohmic contacts on GaN

The realization of low resistivity ohmic contacts on Gallium Nitride is an essential feature for the proper functioning of the devices. High resistivity would result in greater power dissipation on the contacts reducing the efficiency and increasing the heating, and there is also the possibility that the contact material migrates towards the junction short-circuiting the device. Furthermore, in optoelectronic devices the contacts must be transparent to the radiation emitted, in order to not reduce the efficiency of extraction.

1.6.1 n-type GaN

The realization of contacts on n-GaN begins with the implantation of Silicon and with a fast annealing, so as to create a layer of a heavily doped n-GaN ($10^{17} - 5 \times 10^{17}$ cm^{-3}) to encourage the tunnel effect; then the native oxide layer that is formed on the surface is deleted to improve the interface of the semiconductor with the metal via etching with Cl_2 [27]. Now it is possible to proceed with the growth of the contact (followed by a rapid annealing), which is typically composed of several layers of Titanium, Aluminum, Nickel and Gold. During the deposition of the contact can be generated reaction products such as TiAl and AuNi, which are not a problem and actually give a more solid contact.

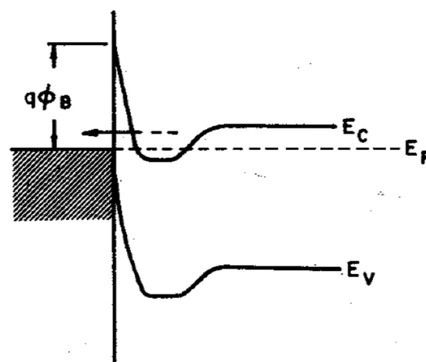


Figure 1.11: Ohmic contact on n-type material

1.6.2 p-type GaN

The contacts on p-type GaN are more problematic, as it is difficult to obtain low resistivity. This is due to the intrinsic characteristics of the band structure of GaN: possessing a high energy gap and high electron affinity, it is hard to find metals with work functions sufficient to achieve low height barriers, in addition, the free hole concentration in GaN is typically quite low, due to the depth in the bandgap of the acceptor level created by the Magnesium. Among the most used metals we have multilayer Nickel and Gold, Platinum and Tungsten in particular, which has excellent strength and stability at high temperatures. Indeed, after the deposition it is required an annealing phase, and a good resistance to temperature leads to a lower degradation of the final characteristics of the device. Clearly, as in the case of n-GaN , a surface treatment for the removal of oxides can greatly improve the charge transport [27].

1.7 Mobility and saturation velocity

One of the most attractive characteristics of the Gallium Nitride is its high electron mobility, as was reported in the table at page 4, which allows for high frequency operation. The mobility influences also the saturation velocity of the carriers, improving the overall characteristics of the devices. The mobility is strongly dependent on the temperature, as can be seen in figure 1.12. The initial increase at lower temperatures can be explained by the interaction of the carriers with the ionized impurities: when an higher thermal energy is possessed by the electrons it is easier for them to escape the coulombian potential of the ionized impurities. Otherwise, the scattering electron - phonon of the crystal lattice is more probable at high temperature due to the increased thermal agitation of the atoms of the crystal, and then in the second part of the figure the mobility drops.

Another aspect that can produce a reduction of the mobility is the concentration of the impurities inside the material, dopants included. For this reason, transistors based on Gallium Nitride are typically designed using heterojunctions, in order to create a conductive channel while avoiding doping. The value of the electron mobility causes an high saturation velocity. Figure 1.13 shows the drift velocity of electrons

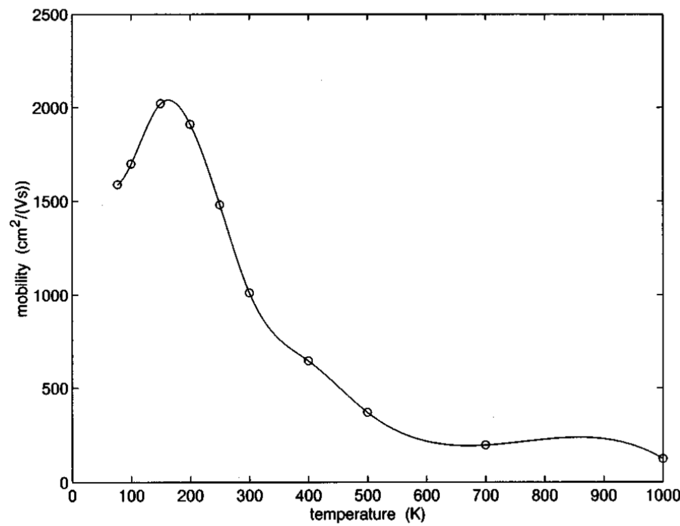


Figure 1.12: Mobility as a function of temperature [28].

in GaN as a function of the applied electric field and of the temperature. When the field is low, electrons are confined in the lower central valley (Γ-valley) of the conduction band, but when the field rises they can move to one of the lateral upper valleys (X, L, A, M-L, see figure 1.2). Since in these secondary valleys the effective mass of the electrons is higher, their mobility is lower, and this explains the negative differential velocity. Moreover, the drift velocity drops at higher temperatures, due to its relationship with mobility.

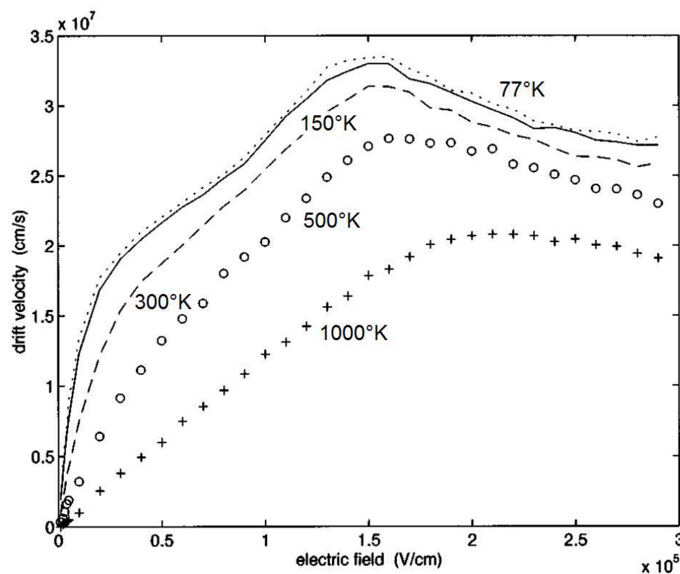


Figure 1.13: Drift velocity as a function of electric field and temperature [28].

In a RF application, in order to obtain high output currents both mobility and saturation velocity are required. Figure 1.14 compares the saturation velocities of various materials used for electronic devices. Gallium Nitride and its compounds possess a remarkable saturation velocity at high electric fields and the ability to withstand them, so they are good candidates for radio frequency devices with high performances.

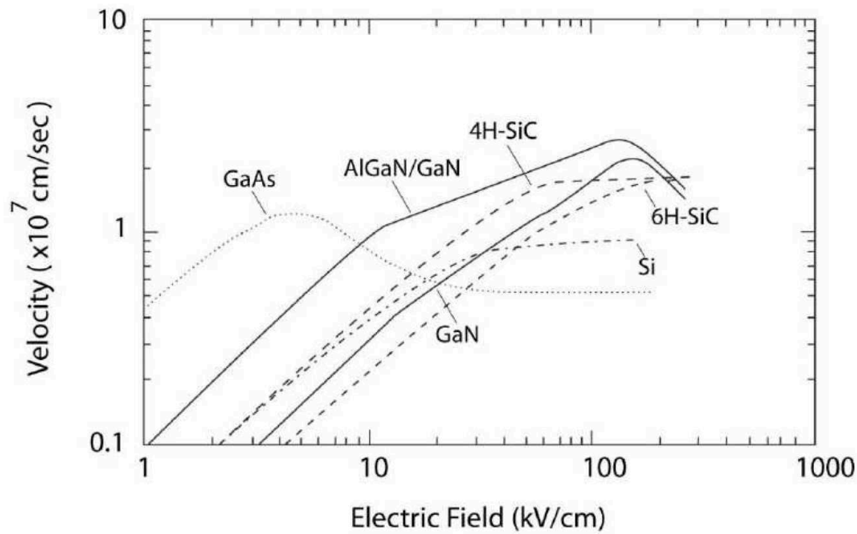


Figure 1.14: Drift velocity as a function of electric field and material [29].

1.8 Johnson's figure of merit

The Johnson's figure of merit is a parameter that can be used to evaluate the overall performances of a material. It is defined as the product between the maximum output electrical power P_{out} and the square of the cut-off frequency f_t

$$JFOM = f_t^2 P_{out} \tag{1.1}$$

The output power is given by

$$P_{out} = \frac{V_{max}^2}{Z_o} \tag{1.2}$$

Here, V_{max}^2 is the maximum output voltage on a generic load Z_o. If we assume that the its value is limited only by breakdown mechanisms, it can be expressed by

the product of the breakdown field E_{break} times the distance between the electrodes where it is applied, i. e. the channel length L_G

$$V_{max} = E_{break} L_G \tag{1.3}$$

Combining equations 1.2 and 1.3, we obtain

$$P_{out} = \frac{E_{break} L_G^2}{Z_o} \tag{1.4}$$

Now, to obtain the Johnson's figure of merit is necessary to evaluate f_t. We can use the derivation made by Brennan and Brown in [30] using a simple small signal equivalent model of the HEMT shown in figure 1.15.

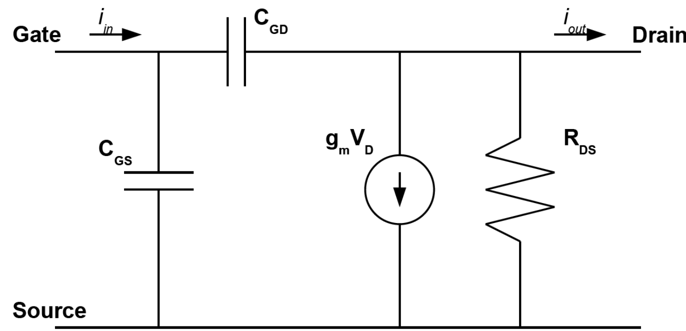


Figure 1.15: Small signal equivalent model of a HEMT [30].

From the basic theory of the electronic devices, we know that the transconductance g_m is defined as

$$g_m = \left.\frac{\delta I_D}{\delta V_G}\right|_{fixed\ V_D} \tag{1.5}$$

The cut-off frequency is defined as the frequency at which the short-circuit current gain of the device becomes unitary, i. e. when it can no longer amplify the input signal. Considering figure 1.15, when the output is short-circuited the small-signal input current i_{in} is given by

$$i_{in} = 2\pi f_t (C_{GD} + C_{GS}) v_G = 2\pi f_t C_G v_G \tag{1.6}$$

and the small-signal output current i_{out} by

$$i_{out} = g_m v_G \tag{1.7}$$

If we impose the same current at the input and at the output (i. e. an unitary gain), we can find the cut-off frequency

$$f_t = \frac{g_m}{2\pi C_G} \tag{1.8}$$

We can approximate C_G with the capacitance due to the 2DEG, obtaining

$$C_G \approx \frac{q n_s L_G W_G}{V_G - V_{th}} \tag{1.9}$$

where q is the electron charge, n_s the sheet charge, W_G the channel width, V_G the gate voltage and V_{th} the threshold voltage. If only the saturation velocity v_{sat} is considered, the drain current can be expressed as

$$I_D = q n_s v_{sat} W_G \tag{1.10}$$

If we substitute in this equation the value of n_s obtained from 1.9, we obtain

$$I_D = \frac{C_G (V_G - V_{th}) v_{sat}}{L_G} \tag{1.11}$$

We can then calculate g_m

$$g_m = \frac{\delta I_D}{\delta V_G} = \frac{C_G v_{sat}}{L_G} \tag{1.12}$$

and f_t

$$f_t = \frac{g_m}{2\pi C_G} = \frac{v_{sat}}{2\pi L_G} = \frac{1}{2\pi \tau_{tr}} \tag{1.13}$$

where τ_{tr} is the transit time of the electrons through the channel. We can then merge equations 1.1, 1.4 and 1.13 to obtain the final expression for Johnson's figure of merit

$$JFOM = \left(\frac{E_{break} v_{sat}}{2\pi}\right)^2 \left(\frac{1}{Z_o}\right) \tag{1.14}$$

Gallium Nitride is one of the most promising materials, with a JFOM of 625. It is 400 for SiC, 14.7 for InP, 7.8 for GaAs and 1 for Si.

1.9 Analysis of GaN defects

The main effect of the defects is the variation of the electrical and optical characteristics of the device. In fact, the defects break the regularity of the crystal lattice, which is the basis of the band theory that describes the electrical behavior of a material, and can lead to the formation of paths of different resistivity than the rest of the material and then a non-optimal distribution of the current in the device. Furthermore, the defects typically behave as deep levels able to capture and emit carriers, and as generation and non-radiative recombination centers, lowering the efficiency of power conversion from electrical to optical.

1.9.1 Lattice strains

The difference between the lattice constants of the substrate and of the grown material, combined with the different thermal expansion during the final stage of cooling, creates strains within the lattice, i.e. the bonds between the atoms that may be longer or shorter than usual. A change in the length of the link also implies a change in its energy, with consequent changes in the electrical transport and optic emission, and can lead to the breakage of the material.

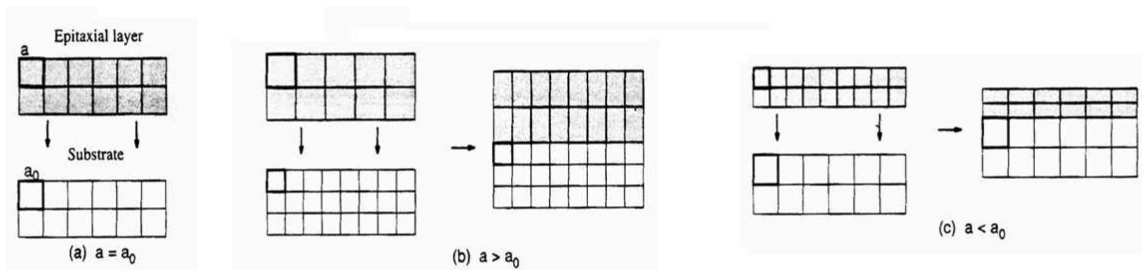


Figure 1.16: Lattice strains for different types of mismatch

1.9.2 Point defects

The point defects are defects that do not extend into the material but interest only a region confined to their position. There are may types of point defects, but in general they are combinations of presences or absences of atoms in positions that are and are not part of the crystal lattice.

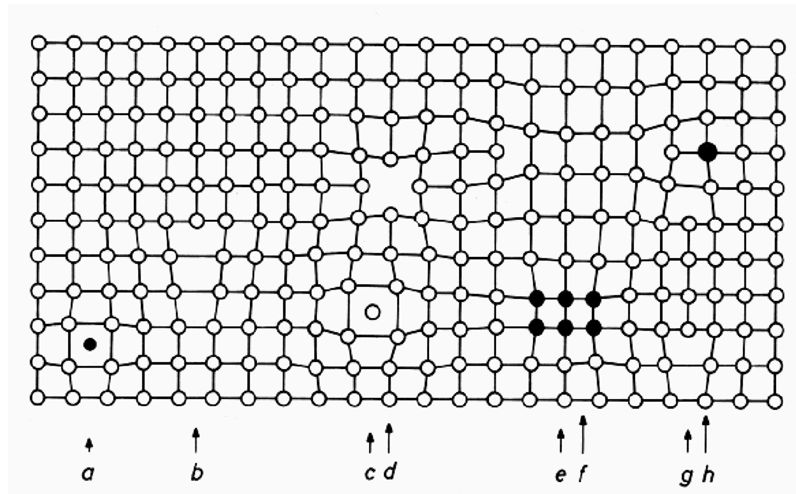


Figure 1.17: Exemplification of various types of defects. May be noticed impurities (a), interstitial atoms (c), vacancies (d) and substitutional impurities (h)

- **Vacancies** are positions that are part of the crystal lattice that should be occupied by a specific atom but they are not. In GaN typically are found vacancies of Nitrogen atoms, which have an effect similar to that of the Hydrogen in passivating the Magnesium, thus reducing the doping of the p-type GaN.

- **Interstitial defects** are atoms that occupy positions within the material not forming part of the crystal lattice, atoms that can be both the elements that compose the material or other elements (such as those present in the atmosphere of the growth chamber, or atoms that diffuse after the growth into the material from the common atmosphere). The electromagnetic field generated locally by the electrons of these atoms alters the electron clouds of the atoms that are part of the lattice, changing the shape and the energy of the bonds. As it is easy to imagine, atoms of small atomic number have a minor effect, both because they have a smaller number of electrons (and therefore less electromagnetic field sources) and because they have smaller dimensions (and thus a less extended influence). As an example of other possible effects due to interstitial atoms, think of what has been said about the passivating effect of Hydrogen on Magnesium.

- **Substitutional defects** are atoms of other elements that occupy positions in the crystal lattice. The effect of these defects typically depends on the type of

substitutional atom, in the case of GaN the most relevant are Hydrogen (for its aforementioned bond with Magnesium), Oxygen (which behaves as a shallow donor causing an unintended and uncontrolled n-type doping) and Carbon (which has an acceptor behavior [31]).

1.9.3 Stacking faults

The stacking faults appear in the presence of lattice mismatch: the lattice exhibits a spontaneous rearrangement of the atomic planes to minimize the residual stress within the material, with the result that the sequence of the atomic layers in some areas of the material can not be the desired one. The GaN is typically grown on materials with quite pronounced mismatch, and therefore the density of the stacking faults is high.

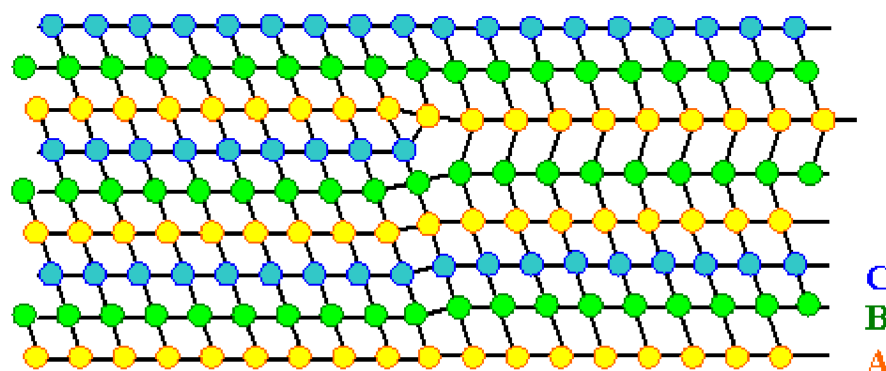


Figure 1.18: Example of stacking fault

The stacking faults have different characteristics depending on the reticular direction in which they are formed: for example, in the plane *c* in the vicinity of the substrate they prevent the initial growth of islands but generate defects which propagate vertically in the material. There are also other types: prismatic defects generated by planar stacking faults on the plane *c* that propagate in the lattice in the [0001] direction; the stacking mismatch boundaries; the inversion domain boundaries. Obviously, the GaN grown on substrates with lower mismatch (such as SiC and GaN) has a lower density of these defects.

The most important effect of the stacking faults is a localized variation in their position of the electrical characteristics of the material (in particular, the bandgap),

while it is not yet clear the relationship that binds them with the mobility of the carriers.

1.9.4 Dislocations

The dislocations are somehow similar to the stacking faults, because they are generated in the epitaxial layer in an attempt to relieve the tension in the material. The difference lies in the fact that there is not the absence of one of the atomic layers, but the relative translational motion of an entire block of material. Dislocations can be of different types depending on the way they are formed: perfect, partial, V-shaped and open core. The most common are the V-type, which take the form of an inverted hexagonal pyramid. The volume of material involved depends on the growth conditions and varies between 10 nm and 250 nm. Their high concentration is derived from the fact that they are typically formed in the interfaces between alloys of nitrides and therefore have a large density in the barriers and in the multiple quantum wells LEDs and laser diodes. Typical densities for GaN grown on Silicon Carbide substrates vary between 10^8 and 10^{10} dislocations/cm^2, while densities of 10^6 dislocations/cm^2 were obtained with the HVPE technique.

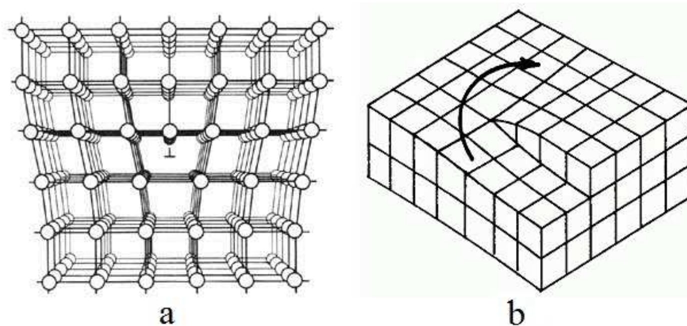


Figure 1.19: Edge (a) and screw (b) dislocation

A high concentration of dislocations has many deleterious effects on the devices. They are able to trap an high quantity of carriers, causing a great variation of the electrical properties in different operating conditions. They also act as non-radiative recombination centers, increasing the current loss and reducing the optical efficiency. They are privileged points for the mechanical breakage of the material and for the subsequent formation of interstitial defects, because of the deformed or not complete

bonds that are formed in these areas. For the reduction of the concentration of a dislocation a technique has proved very promising, the Epitaxial Lateral Overgrowth. To prevent a dislocation, which typically arises at the interface between GaN and the substrate, from propagating vertically, during the growth of the material thin layers of silicon oxide are created as described previously that make the growth lateral, allowing to obtain lower dislocation densities.

Chapter 2

Basics of LED and LD

2.1 Production

The ideal materials for the production of blue and DUV LEDs are alloys of GaN with Aluminum and Indium, which allow to obtain the desired energy gap while maintaining good characteristics of reliability and power dissipation and a not excessively high cost. Using InGaN we are able to achieve a minimum wavelength of about 380 nm, insufficient for some of the applications that will be described later, and the choice must then fall on AlGaN, even if it is a material harder to grow for the following reasons:

- in the devices based on InGaN the dislocations due to lattice mismatch have a lower effect on the performances;
- as described previously, in order to reduce the dislocations a buffer layer can be used; however, the increase of the thickness of the material increases its absorption, thus reducing the overall optical efficiency;
- the growth of massive AlGaN layers on a GaN buffer is still a problematic process at low temperatures.

2.1.1 Structure and production processes

A critical point in the design of LEDs is the choice of the sequence of the various layers and the direction of emission of radiation: the greater the number of layers after the active zone, the greater the absorption of the generated radiation. The

top-emitting structure presents a significant absorption in the layer of GaN of the p-type contact, while in bottom-emitting structures the low concentration of holes and the difficulty in obtaining a p-type ohmic contact requires a thick layer of p-GaN. The radiation does not pass through this contact but through the buffer layer and the substrate, which must then be transparent to the emitted wavelength. Sapphire substrates possess this characteristic, along with problems due to the mismatch (relaxed by the buffer layer) and to the poor thermal conductivity (of low interest for this type of structures).

In a typical bottom- emitting structure, shown schematically in figure 2.1, there is a layer of Aluminum Nitride grown on the Sapphire substrate to reduce the mismatch with the thick overlaying layer of AlGaN. Above the AlGaN is grown a structure called AlN-AlGaN superlattice, i.e. a periodic repetition of thin layers of these two materials, and then a layer of n-type AlGaN with the corresponding contacts to implement the side n of the device. Then, the active area of the device is grown with a heterostructure of multiple AlGaN quantum wells at different concentrations to obtain a good confinement of the carriers. Now we have to implement the side p, which is composed by a layer of p-AlGaN as electron blocking layer (EBL) and a subsequent layer of p-GaN to simplify the realization of the contact. The n-type doping is achieved using atoms of Silicon, while the p-type employs Magnesium. The contacts are made with multilayers of different materials: Titanium, Aluminum, Molybdenum and Gold on the n-side and Palladium and Gold on the p-side.

The presence of a large number of different layers proves critical in the production phase due to the lattice mismatch, and consequently due to the number of dislocations generated. We have already seen some techniques for the reduction of dislocations, such as the epitaxial lateral overgrowth, but in this case they are difficult to use: the Aluminum interacts strongly with the mask of Silicon Oxide typical of this technique. Other techniques that do not utilize masks are not used as they have been proved unsuitable to achieve the goal of growth of AlGaN with high Aluminum content to increase the optical efficiency.

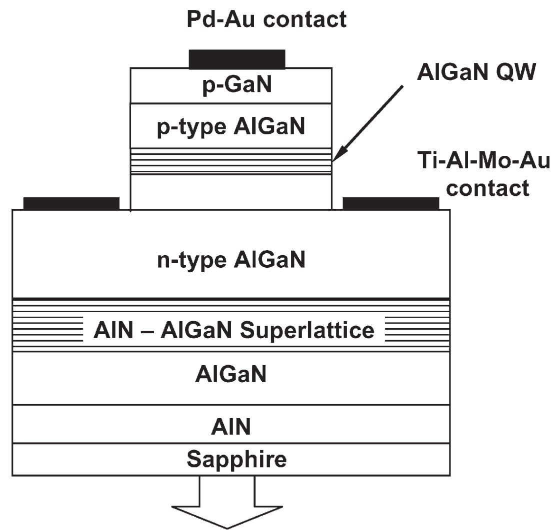


Figure 2.1: Schematic cross-section of a bottom-emitting LED

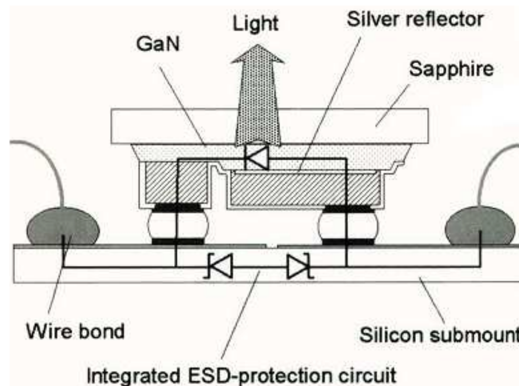


Figure 2.2: Flip-chip package

2.1.2 Flip-chip

The flip-chip technique is a method of mounting the LED on a package which allows to increase the extraction efficiency of the radiation. The chip produced with the bottom-emitting technique described before is reversed to allow the emission through the transparent Sapphire substrate, and not through the semitransparent contact electrode. In this way the absorption of the radiation is avoided, and also the darkening of a portion of the useful surface due to the bonding wires. The connections with the mounting base are made with a reflective metal in order to redirect towards the upper part the radiation that would otherwise be absorbed. Another advantage of these connections is that, thanks to the good electrical and thermal conductivity

typical of metals, it is possible to use circuits integrated in the base for protection against electrostatic discharges (ESD) that may be harmful to the device, as well as improve the dissipation of heat. Furthermore, another process called *roughening* can make less smooth the surface of the LED (in this case the substrate) to further improve the extraction efficiency of the radiation.

2.1.3 Other structures

The LEDs are fabricated also with other structures, three of which are illustrated in figure 2.3 [32].

The first structure has a layer of undoped GaN on which is grown a layer of n-GaN. The p-n zone is constituted by a super-lattice, and a layer of p-GaN forms the p-type contact. In the second structure we have a layer of undoped AlGaN grown on the substrate and a layer of n-AlGaN to form the n-type contact, i.e. the difference from the previous structure resides simply in the choice of materials. The third structure employs a second undoped AlGaN/GaN super-lattice instead of the AlGaN layer used in the second one, and an additional n-doped AlGaN/GaN super-lattice instead of the n-AlGaN.

A common feature of all these structures is the material used for the contacts, an alloy of Nickel and Gold on the p-side and of Titanium and Aluminum on the n-side. Each of these structures appears to be an improvement over the previous one: the layer of GaN used as buffer in the first structure causes an increase of the absorption and is then replaced by a layer of AlGaN in the second, which, however, leads to an increase the lattice mismatch with the substrate and therefore of dislocations, with the consequent preference for the super-lattice which allows to obtain a greater optical power.

2.2 Principles of operation

The structure that is common to all the LEDs is the p-n junction, whose band diagnam is depicted in figure 2.4. When this junction is forward biased, electrons and holes are injected into the region of recombination, where they release their energy emitting by electroluminescence a photon of energy corresponding to the energy gap

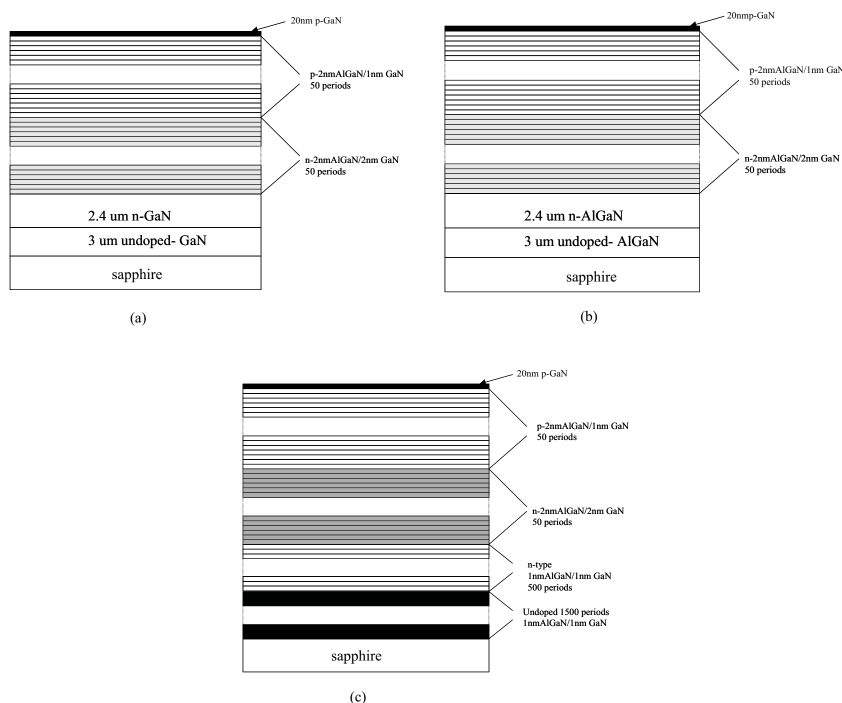


Figure 2.3: Examples of alternative LED structures

of the material [33].

2.2.1 Current-voltage relationship

From the electrical point of view, the LEDs are simply diodes, and can therefore be studied with the basic theory of the p-n junction [34]. To make the discussion more intuitive, we will use the following simplifications:

- abrupt junction: the concentration of donor (N_D) and acceptor (N_A) dopants is constant in the region of implantation and zero outside of it, with no gradual transition between different areas;
- the implanted dopants are supposed to be fully ionized, i. e., all of them contribute to the concentration of free electrons and holes (n=N_D, p=N_A);
- there is no compensation of the dopants due to defects and impurities.

In this case, in the vicinity of the metallurgical junction the electrons and holes diffuse to the other side (due to the concentration gradient), where they can meet carriers of the opposite type with which they recombine. As a result, a region of material around

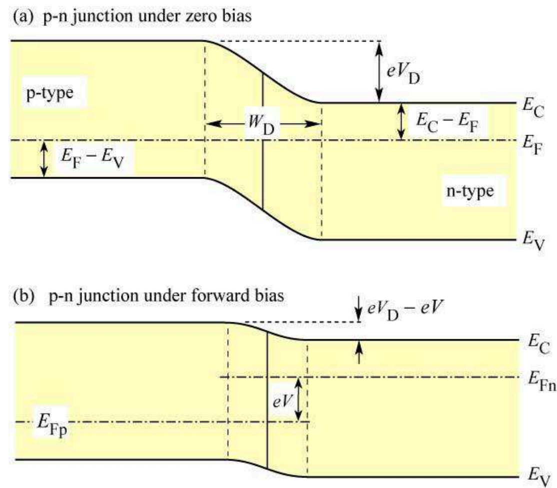


Figure 2.4: Band diagram of a p-n junction under zero and forward bias

the junction is completely emptied of carriers and is called depletion region. When an external bias is applied, the voltage falls mainly in the depletion region (which is more resistive due to the absence of free carriers), decreasing or increasing the potential barrier seen by the carriers respectively for forward and reverse bias. The analytical relationship that describes this behavior was developed by Shockley, and shows how the current tends to a saturation value in reverse operation and increases exponentially in forward bias.

The ideal characteristic degrades dramatically due to the parasitic resistances: typically a diode has a series resistance that models the resistance of the contacts and of the massive non-doped material, and a parallel resistance which models any resistive paths that make the current flow in areas different from the junction, such as damaged regions or surface imperfections. The series resistance takes effect mainly at high voltages: since the voltage drop over the diode and the resistor are added together, and the voltage on the resistance increases as the current increases, the overall characteristic shows a resistive (linear) behavior at high voltages. The parallel resistance is instead more influential at low voltages, when through it flows a current substantially higher than that of the diode, which is reflected in a linear characteristic in the usually flat area. All of these features are illustrated in Figure 2.5.

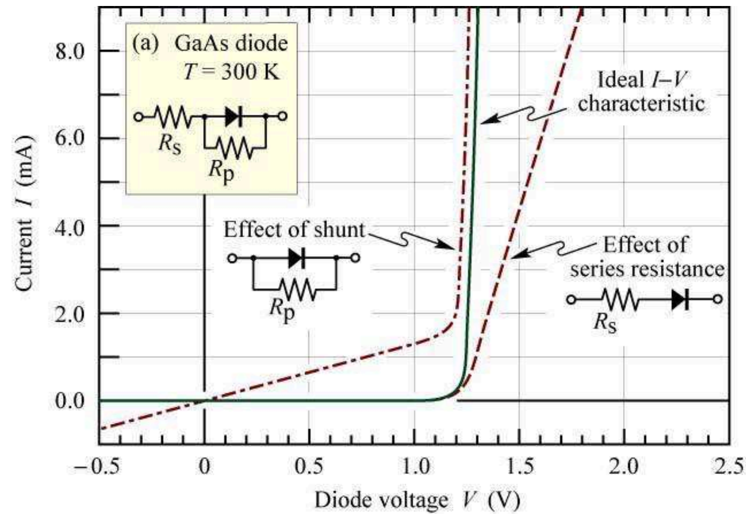


Figure 2.5: Changes in the I-V characteristic due to parasitic resistances

2.2.2 Radiative and non-radiative recombination

Electrons and holes in semiconductors can recombine in two ways: radiative, i. e. with the emission of a photon, or non-radiative, with the emission of phonons. To improve the efficiency of optoelectronic devices it is necessary to maximize this balance in favor of radiative recombination, and the study of the relationship involve writing equations that govern the evolution of the concentrations of excess carriers generated by the absorption of radiation or injection current.

Radiative recombination

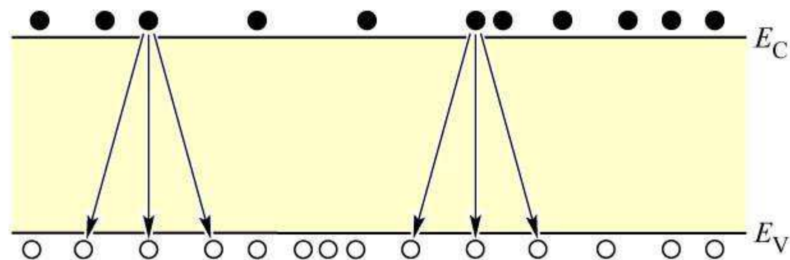


Figure 2.6: Diagram of the dependence of the recombination rate from the product np

The probability that an electron and a hole recombine is proportional to the concentration of electrons and holes, and given that both types of carriers are needed the recombination rate, i.e. the rate at which the number of carriers decreases,

will generally be proportional to the product of the two concentrations (Figure 2.6), according to the relationship

$$R = -\frac{dn}{dt} = -\frac{dp}{dt} = Bnp$$

This equation is the bimolecular rate equation, with a proportionality constant B called coefficient of bimolecular recombination. The evolution of the quantities described by this equation depends on the intensity of excitation. It is convenient to make explicit in the previous equation the dependence on the excess (Δn e Δp) and at equilibrium (n_0 e p_0) concentrations of electrons and holes as

$$R = B[n_0 + \Delta n(t)][p_0 + \Delta p(t)]$$

In low injection, i.e. when the concentration of the injected or photogenerated carriers is negligible compared to the concentration of free carriers ($\Delta n \ll n_0 + p_0$), the bimolecular rate equation can be rewritten, given $\Delta n(t) = \Delta p(t)$, as

$$R = Bn_i^2 + B(n_0 + p_0)\Delta n(t) = R_0 + R_e$$

where n_i is the intrinsic carrier concentration and R_0 and R_e are the recombination rate at equilibrium and in excess. The equation can be resolved to obtain the temporal evolution of the single species

$$\Delta n(t) = \Delta n_0 e^{-B(n_0+p_0)t}$$

with $\Delta n_0 = \Delta n(t = 0)$. This is an exponential decay with a carrier lifetime τ equal to

$$\tau = \frac{1}{B(n_0 + p_0)}$$

In the case of semiconductors with only one type of doping, in the previous equations remains only the term relative to the species of the dopant, leading to what are called monomolecular rate equations.

In high injection, injected or photogenerated carriers dominate over the free ones ($\Delta n \gg n_0 + p_0$) and the bimolecular rate equation becomes

$$\frac{d\Delta n(t)}{dt} = -B\Delta n^2$$

and a solution is

$$\Delta n(t) = \frac{1}{Bt + \Delta n_0^{-1}}$$

that represents a non-exponential decay, whose time constant

$$\tau(t) = t + \frac{1}{B\Delta n_0}$$

depends on the time. This expression also shows us how the lifetime of minority carriers increases with time, and at long times it is equal to the case of low injection, as it would be expected.

Non-radiative recombination

In the processes of non-radiative recombination, the energy possessed by the carriers is converted into vibrational energy transferred to the atoms of the lattice, i.e. phonons (Figure 2.7). This leads, with the extinction of the vibrational motions, to the dissipation of energy as heat, an unwanted event for devices that need to convert electrical power into optical power. The mechanisms and causes of this type of recombination are numerous and have been partially addressed in the part about defects. In particular, defects such as substitutions, vacancies and interstitial defects create allowed energy states inside the energy gap, called deep levels or trap states, which attract the carriers near them causing the non-radiative recombination. Another mechanism is that of the Auger recombination, in which the energy difference between the electron and hole that recombine is not emitted by a photon, but is given to another carrier, increasing its energy.

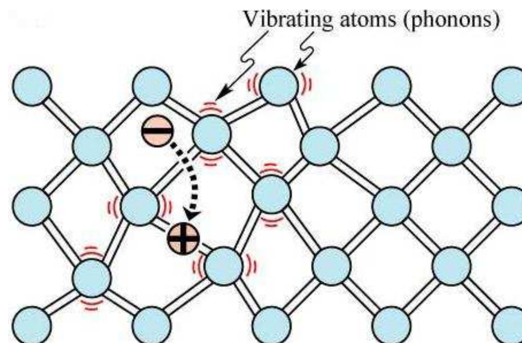


Figure 2.7: Picture of the non-radiative recombination

The recombination through deep levels has been studied extensively by Shockley, Read and Hall (it is often cited as SRH recombination). The rate of non-radiative recombination due to a concentration N_t of energy levels E_t is given by

$$R_{SRH} = \frac{p_0 \Delta n + n_0 \Delta p + \Delta n \Delta p}{(N_t v_p \sigma_p)^{-1}(n_0 + n_1 + \Delta n) + (N_t v_n \sigma_n)^{-1}(p_0 + p_1 + \Delta p)}$$

where v_n and v_p are the thermal speeds of electrons and holes, σ_n and σ_p the traps capture cross-section and n_1 and p_1 the concentrations of electrons and holes as if the Fermi level has energy E_t. The lifetime can be deduced from $R_{SRH} = \Delta n/\tau$ and is equal to

$$\frac{1}{\tau} = \frac{p_0 + n_0 + \Delta n}{(N_t v_p \sigma_p)^{-1}(n_0 + n_1 + \Delta n) + (N_t v_n \sigma_n)^{-1}(p_0 + p_1 + \Delta p)}$$

This result shows that the recombination rate is limited by the rate of capture of the minority carriers (as was intuitable, being less likely than the capture of majority carriers) and its temperature dependence: the decrease of the lifetime with increasing temperature allows us conclude that the SRH recombination causes a drop of the efficiency as the temperature increases.

Mixing the recombinations

Now that we have calculated the radiative (τ_r) and non-radiative (τ_{nr}) lifetime it is interesting to find an expression for the generic recombination lifetime within the material. Clearly, the total recombination rate should be given by the sum of the two rates, which leads us to obtain

$$\tau^{-1} = \tau_r^{-1} + \tau_{nr}^{-1}$$

The relative probability of having radiative recombination is given by the ratio between the probability of radiative recombination and the total probability of recombination. This expresses the internal quantum efficiency of the device, i.e. the ratio between the number of photons emitted and the number of electron - hole pairs which recombine.

$$\eta_{int} = \frac{\tau_r^{-1}}{\tau_r^{-1} + \tau_{nr}^{-1}}$$

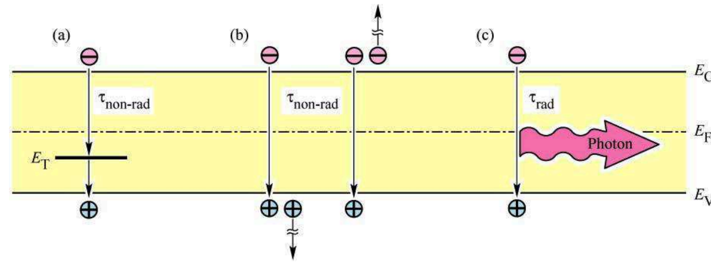


Figure 2.8: Summary of the main mechanisms of recombination: non-radiative through deep levels (a), Auger (b) and radiative (c)

2.2.3 Heterostructures

We have an heterostructure when a device uses two (or more) semiconductors with different energy gap and/or electron affinity. The use of heterostructures has numerous advantages for the realization of optoelectronic devices, but also some problems that should be carefully analyzed.

- First of all, heterostructures have the effect of confining carriers within the area made by the material with the smaller energy gap, so that the region in which the carriers recombine coincide with it and is no longer determined by the diffusion length of the carriers. This has the advantage of concentrating the carriers on a much smaller region, and from the equation of the bimolecular rate ($R = Bnp$) we can see how a higher concentration implies an increase of the rate of radiative recombination and a reduction of the radiative lifetime.

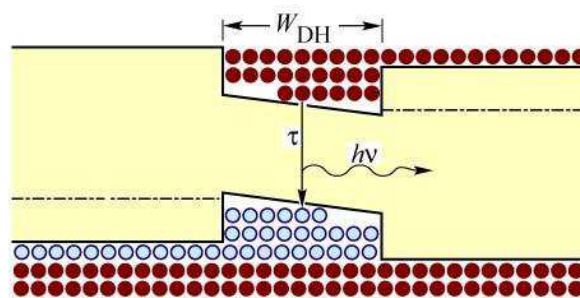


Figure 2.9: Carriers confinement inside a heterostructure

- Heterostructures can be used to confine the radiation in the best areas for its propagation thanks to changes of refractive index, and can be exploited to

improve the performances of contacts through special injection layer. They can also be exploited to reduce the lattice mismatch between different layers.

- One of the problems introduced by heterostructures is the potential barriers that can be created as a result of the transfer of the charges, resulting in an increase of the resistivity. This problem can be solved by using graded changes of composition (parabolic type) rather than abrupt (step), as illustrated in figure 2.10.

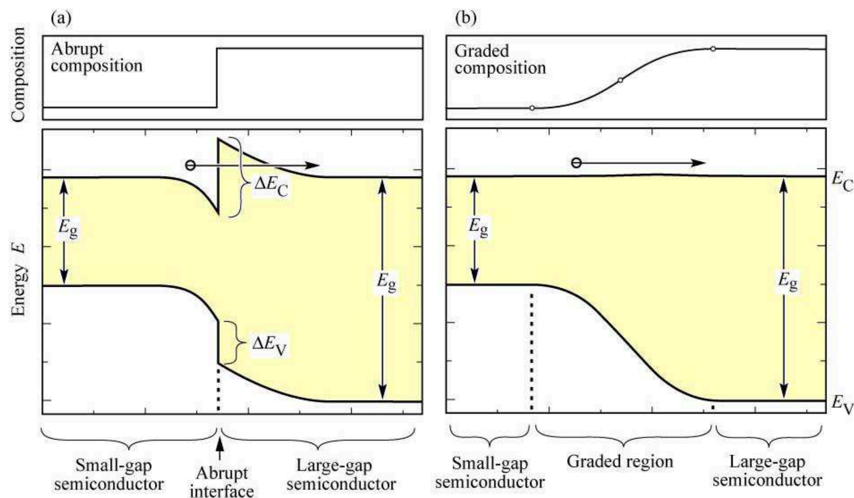


Figure 2.10: Decrease of the resistivity through graded composition

- A second problem comes directly from the high carrier concentration. For high concentrations increases the probability that part of the carriers are able to overcome the potential barrier that confines them, causing a leakage current that reduces the efficiency of the device (figure 2.11). This current increases exponentially with the temperature (i.e. with the thermal energy possessed by the carriers, which makes easier for them to overcome the barrier) and is therefore a critical factor at high temperatures in addition to the SRH recombination.

- A third loss mechanism occurs at high injection levels: the excess flow of carriers. Injection increases the carrier concentration within the potential wells, and with it the Fermi level. When this level is approaching the edge of the well a further increase of the current does not result in an increase of the carriers in the well (because it is “full”) but in a leakage current.

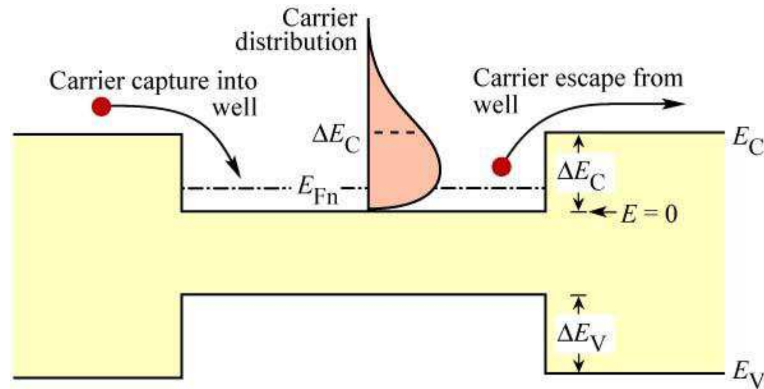


Figure 2.11: Leakage current as a function of carrier energy

- Given that many of the problems analyzed concern the escape of carriers from the potential wells, a solution can come from the same heterostructures. Frequently are grown layers to block the electrons and holes with too much energy with much higher barriers than those of the potential wells, preventing them to be drained from the contacts (see figure 2.12). Over time these carriers lose part of their energy, returning within the potential wells resulting in an increase in overall efficiency.

2.2.4 Optical properties and efficiency

Other than the electrical characteristics, to adequately characterize a device which purpose is the emission of radiation we can not ignore the optical characteristics. Some essential parameters that must be known in order to use these devices in real applications are the relationship between electrical and optical characteristics, the quality of the emitted radiation and how the behavior of the device changes with the external conditions.

Emission characteristics

The physical principle at the base of the LED is the spontaneous emission, which is different from the stimulated emission typical of laser diodes. The resulting spectrum is not monochromatic, as would be expected considering that all the photons have energy equal to the energy gap E_g, but has an energy distribution determined by the product of two contributions (see figure 2.13):

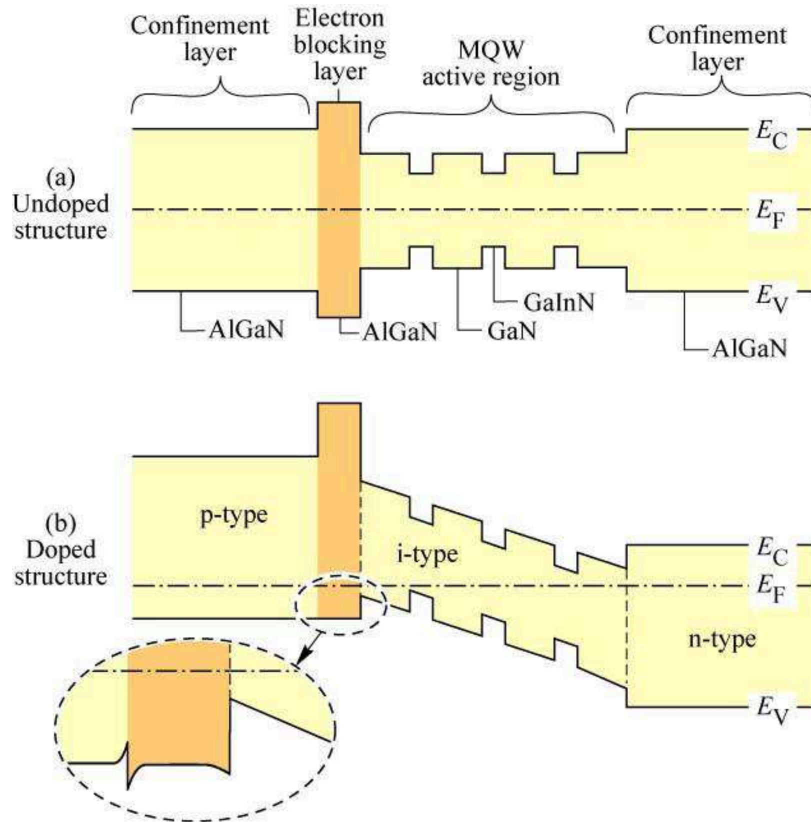


Figure 2.12: Electron blocking layer

- the density of energy states that can be occupied by carriers, proportional to $(E - E_g)^{1/2}$;
- the energy distribution of the carriers within the allowed bands, determined by the Boltzmann distribution and proportional to $\exp(-E/k_B T)$.

After analyzing the spectral distribution of the radiation emitted by the LEDs, it is common to investigate how this radiation is distributed spatially. The emission profile is strongly dependent on the surface topology of the LED, since the direction taken by the radiation must respect the Snell's law at the interface between the device and the external environment (whether it be air or a further encapsulation [35]). In the simplest case, that of an LED with planar surface, the profile of the emission follows a Lambertian profile, with a cosine dependence on the angle between the radiation and the normal.

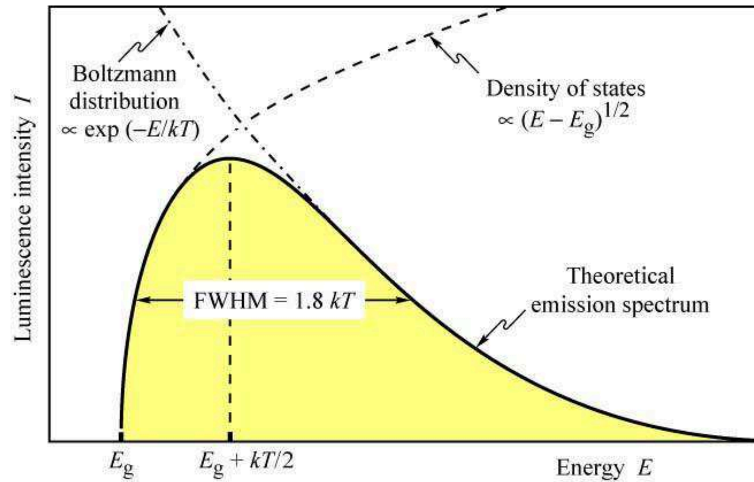


Figure 2.13: Contributions to the spectrum emitted by a LED

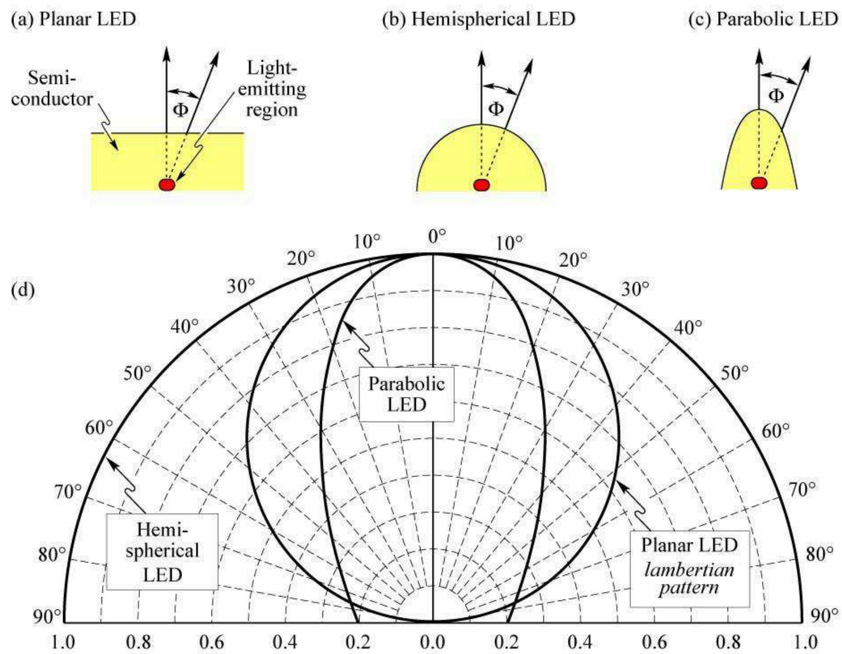


Figure 2.14: Emission profiles for various surface configurations

Efficiency

We have already seen, talking about the mixing of recombinations, the definition of internal quantum efficiency. However, this is not sufficient in order to fully characterize the performance of the devices, since the photons emitted by the active region must escape from the chip. The percentage of photons generated that is actually emitted gives birth to the extraction efficiency, defined as the ratio between the number of photons emitted in the surrounding space and those emitted from the semiconductor each second. Among the main causes that reduce the extraction efficiency there are the absorption by the contacts and the total internal reflection, which traps photons within the device. Note that it is difficult to have an extraction efficiency of more than 50% without the use of complex and expensive processes, which gives an idea of the central role of the extraction efficiency.

It is now possible to define the external quantum efficiency, given by the product of the internal and the extraction efficiency, in order to obtain a quantity that relates the number of electron-hole pairs with the number of useful photons produced. The final step is to define the power efficiency, i. e. the ratio between the emitted optical power and the electrical power absorbed by the device, which gives us the effective efficiency of conversion of power from electric to optic.

Temperature dependence

The intensity of the radiation emitted from an LED decreases with increasing temperature. This decline is due to several factors depending on the temperature, such as

- the non-radiative recombination due to deep levels;
- the recombination that occurs at the edges and on the external surfaces of the device;
- the spilling of carriers over the barriers made of heterostructures.

An experimental relationship that links the intensity to temperature is given by

$$I = I|_{300^\circ K} \exp - \frac{T - 300^\circ K}{T_1}$$

where T_1 is the characteristic temperature, which gives an indication on the strength of the dependence of the intensity on the temperature: high characteristic temperatures indicate a weak intensity variation with temperature.

2.3 Reliability

Some essential analyses that are performed on the LED concern their reliability, i.e. the variations that may occur in the device with the use that could jeopardize the proper functioning.

2.3.1 Catastrophic degradation

The catastrophic degradation is a type of degradation which may occur during the lifetime of a LED, sometimes even without premonitory signs. This degradation causes an irreparable decline in the characteristics of the device, which can be considered not working. The typical cause is the presence of defects within the material which, starting from the n-type area, also grow in the p-type area. Through these defects can also flow high currents, which may fuse the material and can in effect short-circuit the device preventing the distribution of current within the active area.

2.3.2 Gradual degradation

The gradual degradation is not destructive for the device, but it alters the characteristics worsening the optical and electrical behavior. This type of degradation typically causes a decrease of the optical power according to a decreasing exponential relationship in time, which then becomes linear with the continuation of the life of the device. The main causes of this degradation are the current through the active zone and the temperature increase generated by it [36], which lead to an increase in the number of defects and to their extension within the material. These defects lead to a variation of the rate of generation and radiative and non-radiative recombination, which thus leads to the modification of the optical properties, as well as to a possible increase of the tunneling current and to a variation of the distribution of the current within the active area, which influences also the electrical characteristics.

2.3.3 Kinetic energy of the electrons

The electrons, crossing the p-n area of the device, are accelerated by the electric field and can gain considerable kinetic energy. If they strike atoms of the lattice part of this energy is transferred, potentially causing the breakage of bonds both between Magnesium and Hydrogen (increasing the p-type doping)and between Gallium and Nitrogen (causing Nitrogen vacancies [36]). The increased activation of the Magnesium causes an increase of the optical power which then tends to reach a constant value, while the vacancies of Nitrogen lead to a slow decrease in the emission over a longer period of time.

2.3.4 Magnesium diffusion

GaN LEDs require a high concentration of Magnesium, which is used for the p-type doping, due to the intrinsic n-type doping and to the high activation energy of Magnesium. This can lead Magnesium to spread to other areas of the device, resulting in the formation of non-radiative recombination centers in the active region and a consequent decrease of the efficiency and of the emission [37].

2.3.5 Current crowding

Inside the chip the current distribution in the material is not uniform, because of the not perfect quality of the contacts and of the inhomogeneity of the material itself, which create paths of different resistance [34]. This causes the non-uniformity of the light emission and of the degradation, particularly in large or highly heterogeneous devices. In LEDs with Sapphire substrate this phenomenon is particularly intense, and causes a high current in the vicinity of the contacts (which, it must be remembered, are both made on the upper face) with a exponential decline with increasing distance from the region of proximity between the two. The effect is lower for substrates in Silicon Carbide.

One possible solution is to use semi-transparent layers below the p-type contact, but they tend to degrade rapidly and alter the electric transport and the extraction of radiation from the active region. A better technique is to distribute the current uniformly varying the geometry of the contacts (for example, with a contact shaped

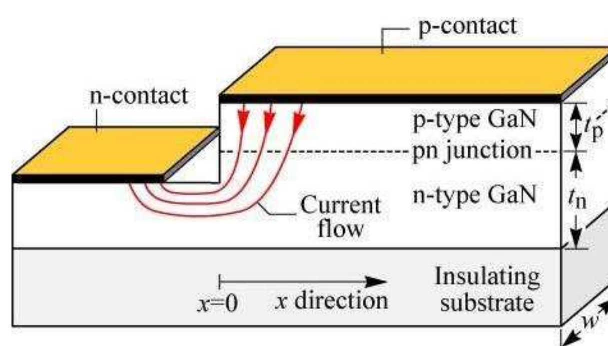


Figure 2.15: Current crowding effect

like a grid instead of a single point), a solution commonly used because the redistribution of the current causes an increased emission superior to the losses caused by the obscured surface percentage.

2.3.6 Electrostatic discharges (ESD)

LEDs, like all other electronic devices (and in particular those made of GaN), are very sensitive to electrostatic discharges. A probable cause is the large amount of lattice defects present in the crystal, which leads to the devices not able to withstand shocks exceeding 500 V (on Sapphire). Electrostatic discharge and excessive operating values achieved during longer abnormal events (electrical overstress EOS) are among the leading causes of malfunctioning of electronic devices. Even if different in their origin, these phenomena are typically handled jointly due to the remarkable similarity of the changes they create in the structure and in the electrical and optical characteristics of the devices. The purpose of this part is the discussion of the main effects arising from electrostatic discharges in laser diodes, with particular attention to the characteristic parameters of the operation of a laser (threshold current, slope efficiency, divergence angle of the beam, the spectral width of the emission) and to the changes in some indicators of the health status of the device (current - voltage relationship, optical power). Second, it will provide some examples of protection structures that allow to mitigate the harmful effects caused by the discharge events. The results reported in this first part refer to InP - based laser diodes with an active epitaxial layer composed of multiple InGaAsP quantum wells (MQW), grown by MOCVD. These devices have blocking layers realized in InP doped p-type and n-type,

while the metal contacts are composed of Au/Ti/Zn/Au or Au/Zn/Au to the p-side , and Au/Ge/Ni/Au to the n-side [38]. The discharges were carried out according to the **human body model** (HBM), with a resistance of 1.5 kΩ and a capacitance of 100 pF . The test consisted of a series of discharges at increasing voltage from 0.5 kV with a 0.25 kV step up to the value of failure, identified as the value that causes a variation in the threshold current greater than 3 mA , with typical values of threshold current for these devices equal to 6 - 8 mA. At each step the device was submitted to a single discharge in forward bias, reverse or a combination of the two (forward followed by reverse or vice versa). In figure 2.16 is shown a diagram of the structure of the laser and the principle diagram of the experimental setup for the implementation of the discharges.

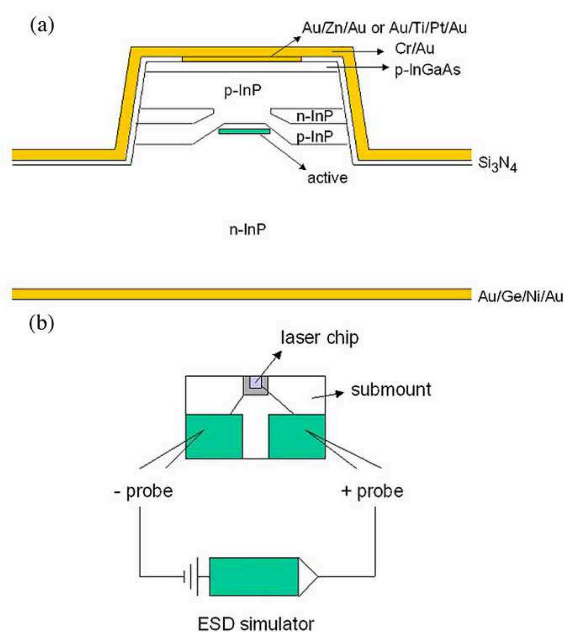


Figure 2.16: Structure of the laser under test (a) and basic diagram of the experimental setup (b) [38].

The most obvious change in the characteristics of laser diodes due to ESD events is found in the electrical - optical power characteristic. In figure 2.17 are shown the curves before and after a ESD stress in reverse bias at 4 kV. It can be seen that there is a significant increase of the threshold current (from 8 mA to approximately 28 mA) and a decrease in slope efficiency (from 0.43 to 0.31 mW/mA). Due to both these changes, there is a considerable decline of the optical output power at a given

current, but despite that the laser diode remains operational.

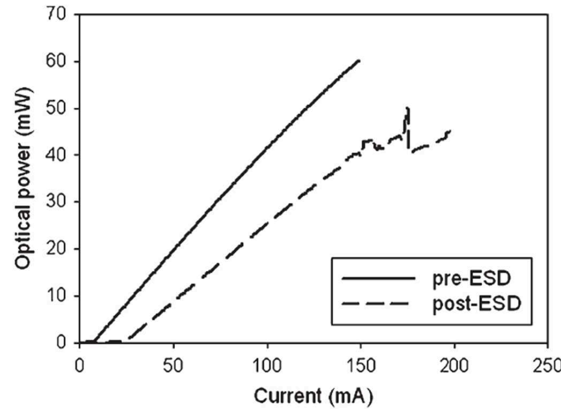


Figure 2.17: Relationship current - optical power of a laser diode submitted to 4 kV reverse ESD discharge [38].

For the description of the operation of a generic laser is very important also the spectral distribution of the emitted radiation, as a lower line width implies a better concentration of the input power to the wavelength of interest and a more precise choice of the frequency of the emitted radiation. In the literature are present analyses on lasers with a Fabry - Perot (FP) resonator and systems with distributed feedback (DFB), which have reacted differently to the applied discharges. Regarding the DFB lasers, before the stress they showed a very good rate of suppression of secondary modes (SMSR) which then dropped considerably after the discharge. Instead, in devices with a Fabry - Perot appeared a very strong ripple at all the wavelengths under analysis, even if the mechanisms behind this ripple are not yet well understood and can be related to the different electrical structure of the device. The spectra of some devices are shown in figure 2.18, together with the discharge conditions in reverse bias (for the DFB laser) and reverse - forward (for FP lasers) which have caused those changes.

In other cases, DFB devices similar to those just analyzed have shown a shift toward the blue of the emission, probably due to the passage of the peak emission from the main mode to a contiguous mode [39].

As in many other types of stress, the changes introduced in the crystal structure, with a consequent increase in the concentration of defects and therefore in the generation/recombination (G/R) current, make the current value reached by the device in

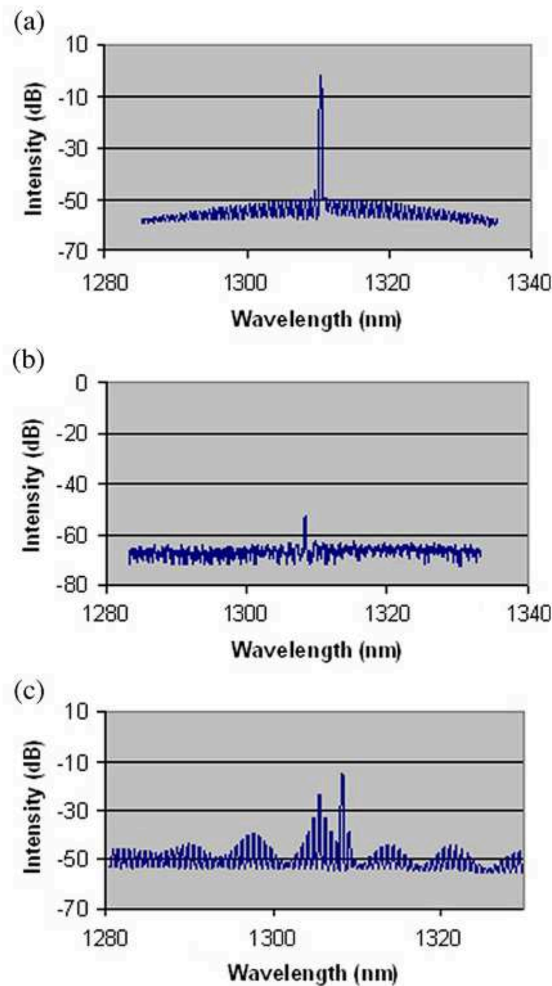


Figure 2.18: Spectra of different devices: (a) DFB, untreated; (b) DFB, stressed at 1.75 kV; (c) FP, stressed at 0.5 kV [38].

reverse bias a good parameter to assess the effects of stress. The lasers have shown two different behaviors: if the stress was not associated with a significant change (less than 5%) of the threshold current there is an increase of reverse current, which became much more intense in the case of devices that suffered a greater variation the threshold current. In both cases , the percentage variation of the reverse current proved to be about two orders of magnitude greater than the percentage change of the threshold current . Figure 2.19 shows (a) an example of a device that has not undergone a large variation of threshold current (10.2, 10 and 10.3 mA respectively for the untreated device, stressed at -2 kV and -2.75 kV) with a 285 % increase of the reverse current at the greater stress condition, and (b) a device with a significant

variation of the threshold current (from 8.7 to 12.6 mA, 46%) resulting in significant increase of the reverse current (3097 %) after a stress at -2.5 kV.

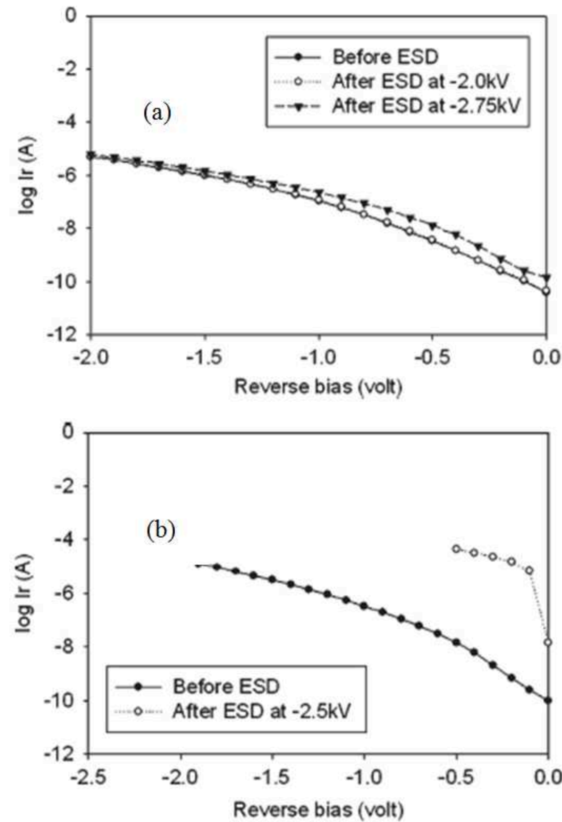


Figure 2.19: Reverse current - voltage relationship for two devices with (a) lower and (b) higher variation of the threshold current [38].

If until now we have mainly analyzed the effects produced by discharges in reverse bias, it is still interesting to see the effects of different polarities to try to understand the physical mechanisms that cause degradation. Figure 2.20 shows the statistical distribution of the failure voltages. The gray boxes enclose the results of 50 % of the devices, while the top and bottom edges represent respectively 75 % and 25 %. The line in the box indicates the mean of the population, the end of the vertical lines the minimum and maximum values and the separated points values that deviate much from the rest of the distribution, probably due to the devices grown with a particularly good or bad condition compared to the average.

Given the use of two different stacks of materials (Au/Ti/Zn/Au or Au/Zn/Au) for the contact of the p-side, in the literature are found also tests to verify the depen-

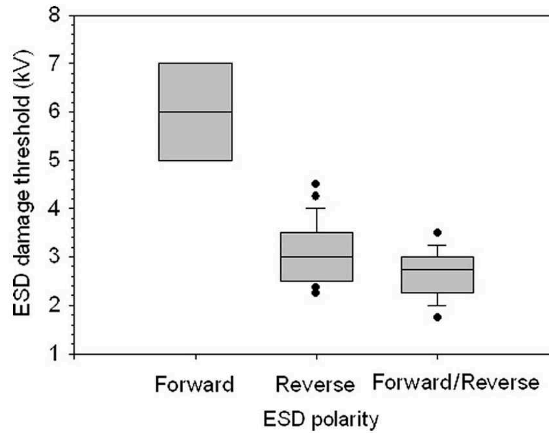


Figure 2.20: Distribution of the failure voltages at different polarities [38].

dence of the ESD robustness on the chemical composition of metal layers. Figure 2.21 summarizes the distribution of failure voltages of the devices tested (the percentage of broken devices below a certain voltage is shown in logarithmic scale). The two distributions are quite similar and do not allow to gain further information. It can be seen also that the breakdown voltages in the various bias conditions are compatible with the previously reported ones: these devices are most sensitive to alternating discharges in forward and reverse bias, in a lesser way to reverse pulses, and are relatively resistant to forward bias. The fact that the devices are more sensitive to shocks in reverse is probably due to an effect of avalanche breakdown, while in the case of succession of discharges in forward and reverse the lower robustness may be due to some kind of memory or cumulative effect, in a similar way to what occurs in integrated circuits [40, 41]. It is not reported a dependency on the order of the two directions of polarization.

A variation of the robustness has been reported as a function of the width of the contact (figure 2.22). Larger contact areas give birth to devices more resistant to electrostatic discharges (probably for the reduction of current crowding) but lead to a worst confinement of the current and to an increase of the parasitic capacitance, so the design of these devices requires careful evaluation of the specific performance and robustness [42].

During the stress of the devices are reported two different behaviors: in some cases there has been a gradual increase of the threshold current with the applied voltage of

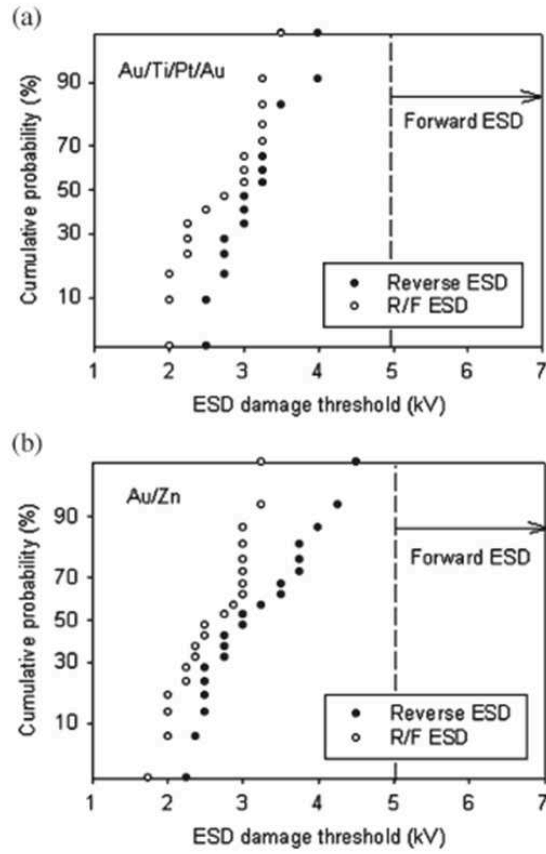


Figure 2.21: Cumulative percentage of failed devices for different p-side contact materials [38].

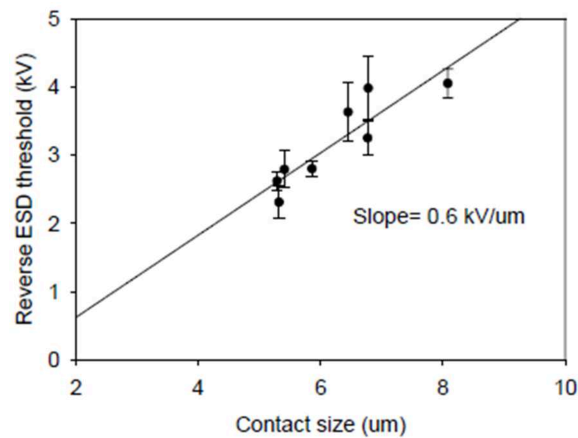


Figure 2.22: Reverse ESD failure voltage as a function of the contact size [42].

the discharges (soft), while in others the increase of the threshold current was very sharp once a critical value was reached (hard). Figure 2.23 shows an example of these kinetics, considering both the threshold current and the slope efficiency. It was also found a dependency between the frequency of the two mechanisms and the length of the laser cavity, as shown in figure 2.24: this trend can be explained by considering the flow of energy through the device. For shorter devices, at the same discharge level the flow of energy through the active zone is greater, with a consequent increase in the power dissipated locally and a higher probability of catastrophic degradation.

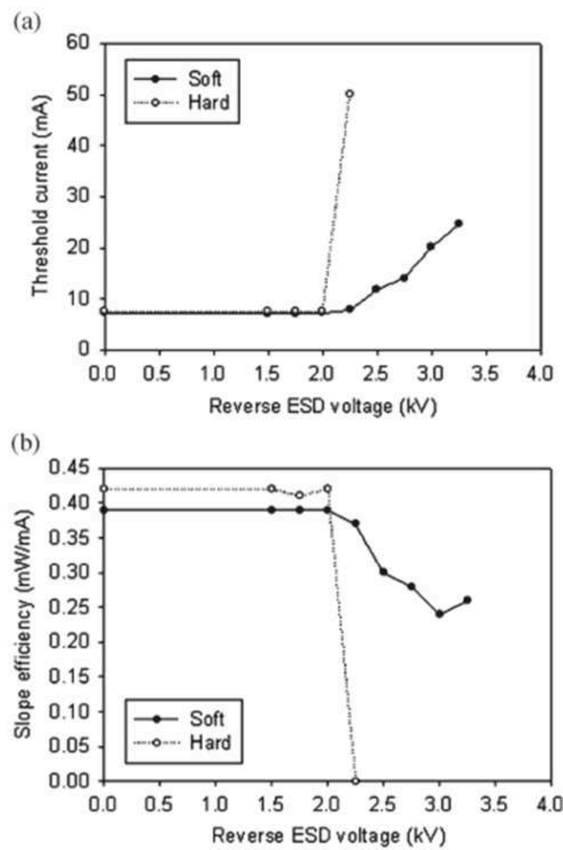


Figure 2.23: Example of typical degradation kinetics [38].

From measurements carried out by scanning electron microscopy (SEM) on the various devices, the main zones in which can be found changes in the structure of the laser are the facet of the active region, near the upper contact. This suggests that the damage has been caused by a phenomenon of current crowding, resulting in a strong local absorption due to surface recombination. In addition, it has been noticed

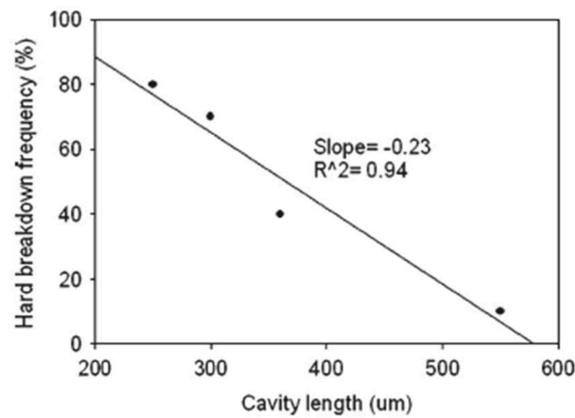


Figure 2.24: Dependence of the breakdown frequency on the cavity length [38].

damage to the facets more frequently in the devices affected by soft degradation (36 % vs 16 %), so it is assumed that a correlation exists between the two phenomena. Another group of diodes showed no obvious damage in these areas. The degradation may therefore be due to defects formed inside the active region, for example in correspondence of points with an unintentionally higher doping, of the interfaces of the heterostructure, of the edges of the device and of the lattice defects. On the length of the cavity also depends the failure voltage, following a proportional linear dependence (figure 2.25). As the length of the cavity increases from 250 μm to 750 μm, the average value of the breakdown voltage in reverse bias condition grows linearly from 2.25 kV to 7.65 kV. Since lasers with shorter cavity are typically used in applications that require high-speed response, special attention must be taken in the design of the protection structures in these cases, since the components used are inherently more sensitive [42].

The simplest protection structure against electrostatic discharges is composed by a diode placed in anti-parallel to the device, sized suitably in order to start conducting at the occurrence of a reverse discharge (we have to remember that these devices are intrinsically resistant to forward discharges) and thus avoid that all the current is circulated through the device to be protected. As this configuration may seem trivial, it has still a good efficacy which, combined with low cost and manufacturing simplicity, makes an acceptable compromise for most of the applications in which no greater robustness is required. In figure 2.26 we can see how, thanks to the protection diode, it is possible to more than double the failure voltage, significantly increasing

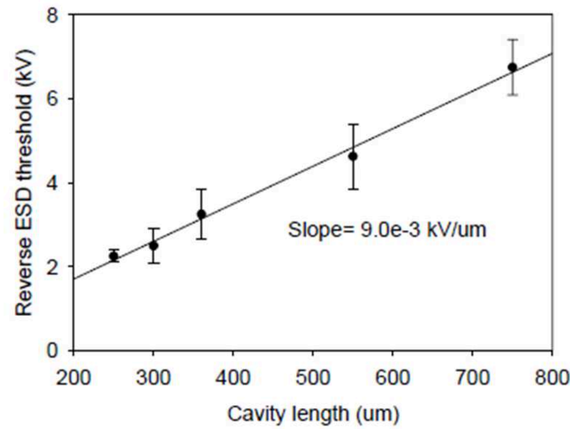


Figure 2.25: Dependence of the failure voltage on the cavity length [42].

the robustness of the device.

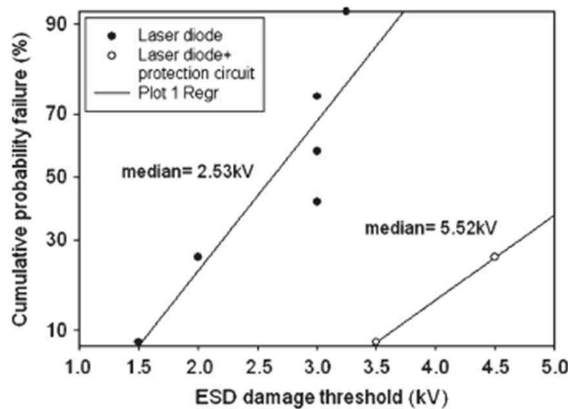


Figure 2.26: Failure cumulative probability of devices with and without protection diode [38].

Another method that can be used to improve the reliability of the laser does not require external circuitry and can be done during the growth of the diode: the facet passivation [43]. Inserting a thin (20 Å) layer of aluminum between the facets and the semiconductor is possible to reduce the oxidation and surface recombination, leading to an increased resistance to forward discharges (figure 2.27).

Other research groups have carried out detailed analyses of the spatial characteristics of the beams emitted from laser diodes subjected to ESD events, such as those discussed in [44] for top-emitting VCSEL diodes with distributed Bragg reflector (DBR) based on AlGaAs. The results reported in figure 2.28 show how the

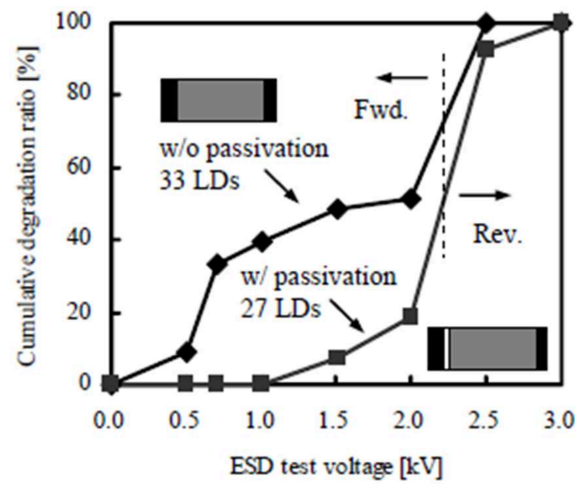
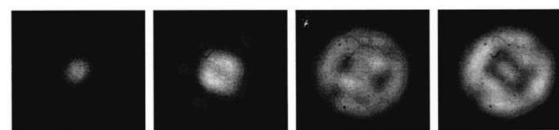


Figure 2.27: Increase of the failure voltage with facet passivation [43].

application of electrostatic discharges reduces the divergence of the beam detected in far-field zone, thus leading to an improvement of the device. This apparent contradiction can be explained by the variation in the number of modes that can oscillate in the cavity: compared to unstressed devices, the spot of the laser subjected to discharges do not exhibit higher-order "donut" modes around the main mode, leading to a reduction of the divergence.



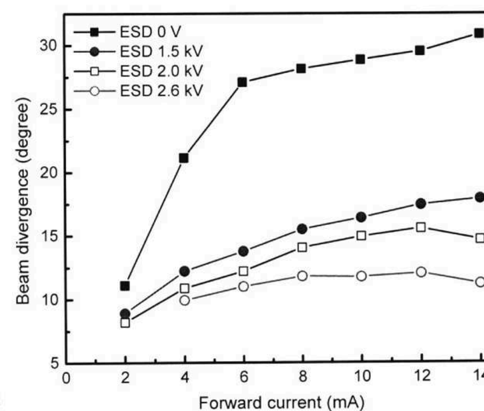


Figure 2.28: (a) far-field patterns at various currents (2, 4, 8, 12 mA) and (b) beam divergence [44].

These devices have also shown another curious effect, exemplified in figure 2.29 (the spectra are shifted along the axis of the intensity for clarity). If the spectra of virgin devices show several transverse modes oscillating in the cavity, at higher stress voltages the lasers show a weakening of the main mode but a strong suppression of the secondary modes, proportional to the order of the mode.

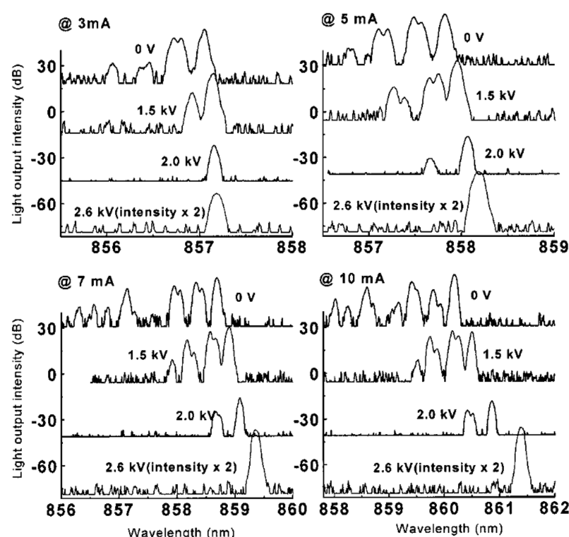


Figure 2.29: Spectra at various currents before and after a ESD stress [44].

The electrostatic discharges have shown an improvement in spectral characteristics and divergence, but the sharp drop in optical power, however, does not make it possible to exploit this behavior to improve the quality of the final products.

2.3.7 Early degradation

Although a large number of the degradation causes described above are thermally activated and more intense for higher current levels, there are other mechanisms of degradation that can occur at room temperature and for low current densities. We refer to all of these mechanisms with the name of early degradation, and typically they influence the optical behavior of the device without significantly changing the electrical characteristics. There have been reports of optical power drops up to 25% over 100 hours at low current.

2.4 From LEDs to laser diodes

The structure and principles of operation of a laser diode are very similar to those of an LED. The main differences are two: the operation based on stimulated emission (rather than on spontaneous emission) and the presence of mirrors or other methods to keep stable the radiation field within the active region (resonator).

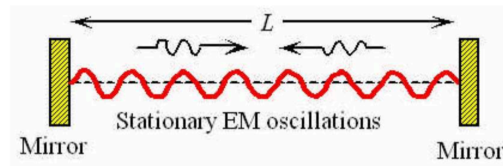


Figure 2.30: Schematic of a typical resonator

2.4.1 Stimulated emission

In the process of stimulated emission, an incident photon induces the excitation of an electron from a higher energy level to a lower level, with the emission of another photon. The salient point of this process is that the emitted photon has the same phase, direction, polarization and energy. This process continues, giving rise to a coherent radiation with characteristics of monochromaticity and power density that are impossible to achieve with classical methods.

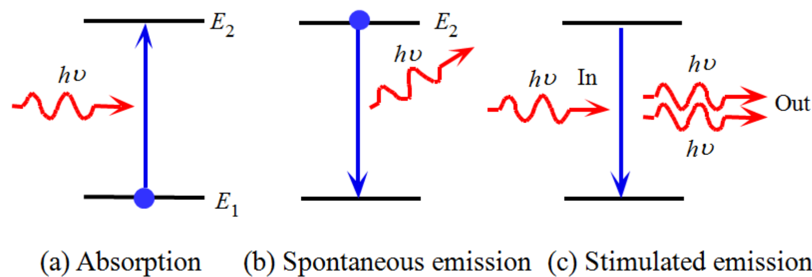


Figure 2.31: Absorption and emission processes

In order to obtain the laser radiation it is necessary to achieve the population inversion, i.e. a concentration of atoms in the higher energy level greater than the one in the lower energy level. The analytical relationships of the spontaneous emission and stimulated emission processes have been developed by Einstein. In a system with a density of atoms N_1 in the energy level E_1 and N_2 in the higher energy

level E_2 ($E_2 > E_1$), the rate of excitations from level E_1 to level E_2 stimulated by the absorption of a photon will be proportional to the number of atoms in the fundamental state N_1 and to the number of photons with sufficient energy to allow the excitation ($E_{ph} = h\nu > E_2 - E_1$)

$$R_{12} \approx B_{12} N_1 \rho(h\nu) \tag{2.1}$$

where $\rho(h\nu)$ is the energy density of photons per unit of frequency and B_{12} is called the Einstein coefficient B_{12}. The transitions from E_2 to E_1 may be due to spontaneous emission or stimulated emission, with a rate

$$R_{21} \approx A_{21} N_2 + B_{21} N_2 \rho(h\nu) \tag{2.2}$$

where A_{21} is called the Einstein coefficient A_{21} for the spontaneous emission. In order to calculate these coefficients we suppose to be at equilibrium, in order to have $R_{12} = R_{21}$. We can therefore apply the Boltzmann statistics and we obtain

$$\frac{N_2}{N_1} = \exp\left(-\frac{E_2 - E_1}{k_B T}\right) \tag{2.3}$$

where k_B is the Boltzmann constant and T the absolute temperature. The energy density as a function of frequency of the photons at equilibrium is given by Planck's law of the black body

$$\rho_{eq}(h\nu) = \frac{8\pi\nu^2}{c^3} \frac{h\nu}{\exp(\frac{h\nu}{k_B T}) - 1} \tag{2.4}$$

From the previous equations we obtain

$$B_{12} = B_{21} \qquad \text{e} \qquad \frac{A_{21}}{B_{21}} = \frac{8\pi h\nu^3}{c^3} \tag{2.5}$$

The relationship between stimulated emission and spontaneous emission is given by

$$\frac{R_{21,stim}}{R_{21,spon}} = \frac{B_{21} N_2 \rho(h\nu)}{A_{21} N_2} = \frac{B_{21} \rho(h\nu)}{A_{21}} \tag{2.6}$$

and using 2.5 we obtain

$$\frac{R_{21,stim}}{R_{21,spon}} = \frac{c^3}{8\pi h\nu^3}\rho(h\nu) \tag{2.7}$$

It is also important the value of the ratio between stimulated emission and absorption

$$\frac{R_{21,stim}}{R_{12}} = \frac{N_2}{N_1} \tag{2.8}$$

These two last equations show us that to increase the spontaneous emission it is required a high concentration of photons and therefore a good containment capacity of the cavity and a high pumping, while for more absorption we need to obtain a population inversion $N_2 > N_1$.

2.4.2 Conditions for oscillation

In order to keep the radiation field within the active region the presence of mirrors is not sufficient: other conditions are also necessary which are highly dependent on the geometry and type of the active material.

Optical gain coefficient

The optical gain coefficient g is defined as the change in the radiation power per unit of length. While the radiation travels inside the active material, we have both a gain due to the stimulated emission and a decrease due to absorption and losses. The optical power at each point is proportional to the concentration of coherent photons N_{ph} and to their energy $h\nu$. Photons travel with speed c/n, where n is the refractive index, and then in a time dt they cover a distance equal to $dx = (c/n)dt$. The optical gain coefficient can then be expressed as

$$g = \frac{dP}{Pdx} = \frac{dN_{ph}}{N_{ph}dx} = \frac{n}{PcN_{ph}}\frac{dN_{ph}}{dt} \tag{2.9}$$

From the theory of stimulated emission, the rate of stimulated emission is given by

$$\frac{dN_{ph}}{dt} = N_2B_{21}\rho(h\nu) - N_1B_{21}\rho(h\nu) \tag{2.10}$$

The energy density $\rho(h\nu)$ can be expressed as a function of N_{ph} as

$$\rho(h\nu) \approx \frac{N_{ph}h\nu_0}{\Delta\nu} \tag{2.11}$$

where $\Delta\nu$ is the enlargement in frequency due to the Doppler effect, to the lifetime of the transitions, to the widening of the band edges and to other factors. Using the equations 2.9 and 2.11 you can get an expression for the optical gain coefficient at the center frequency ν_0

$$g(\nu_0) = (N_2 - N_1)\frac{B_{21}nh\nu_0}{c\Delta\nu} \tag{2.12}$$

Phase relationship and modes

Imagine an electromagnetic wave that propagates from the first face of the active medium, is reflected by the second and returns toward the first. The radiation field that arises is stable only if the phase shift in the radiation due to the go and back travel (round-trip) is an integer multiple of 2π. If $k = 2\pi/\lambda$ is the wave vector, its values are all and only the k_m that satisfy this rule, and therefore these are the values of the wave vector we can expect to be emitted from the cavity. Assuming that the refractive index n is constant and that the mirrors do not introduce phase shifts, we can write

$$nk_m(2L) = m(2\pi)$$

where L is the length of the cavity. This relationship results in a selection rule for the length of the cavity in order to obtain a radiation of the desired wavelength λ_m:

$$L = m\left(\frac{\lambda_m}{2n}\right)$$

Consequently, the possible stationary configurations of the electromagnetic field inside the cavity are strongly dependent on the shape of the cavity itself, on the way that the radiation takes, on the shape of the mirrors and on other obstacles in the cavity, as they must replicate after an entire round trip in the cavity. Each of these configurations is called **mode** of the cavity, or alternatively, given the typical orthogonality between electric and magnetic fields and the axis of the cavity,

transverse electric and magnetic modes (TEM). These modes are referred to, depending on their shape, with a pair of integers representing the number of nodes in the distribution of the field along two orthogonal transverse directions.

Gain and threshold current

In order to have a radiation field that is not extinguished in time it is necessary that the gain in the cavity in a round trip is at least unitary. This gain is influenced by many factors, such as the reflectivity R_1 and R_2 of the mirrors, the losses in the active material (γ) and the coefficient of optical gain (g). The initial power P_i after a round-trip $2L$ then becomes a final power

$$P_f = P_i R_1 R_2 exp[g(2L)]\exp[-\gamma(2L)]$$

The value of the optical gain coefficient which allows to meet this condition is called the threshold gain

$$g_{th} = \gamma + \frac{1}{2L}\ln\left(\frac{1}{R_1 R_2}\right)$$

Substituting in equation 2.12, we can calculate the value of the threshold population inversion

$$(N_2 - N_1)_{th} = g_{th}\frac{c\Delta\nu}{B_{21} n h \nu_0}$$

This relationship provides us with the regions of operation of the laser when the pumping varies. Until the pumping does not make the population inversion reach the threshold value, the supplied energy contributes only to the increase of the inversion. When the inversion reaches the threshold its value no longer increases, while the output power increases (figure 2.32).

However, the gain is an uncomfortable threshold parameter to work with when it comes to electronic devices; it would be much more useful to have a relationship as a function of the bias current. The gain is proportional to the carriers in excess of the value of transparency (i.e., the value of inversion such that the stimulated radiation emitted offsets exactly the absorption of the medium)

$$g \approx G(n - n_{th}) = G'\Gamma(n - n_{th})$$

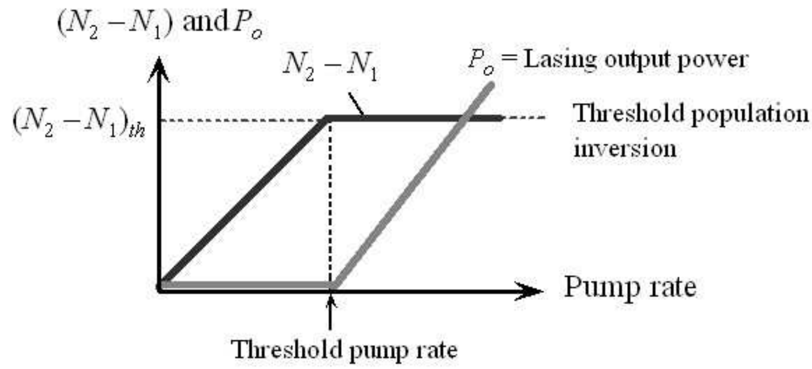


Figure 2.32: Population inversion and output optical power as a function of pumping

where G' is the portion of G due to the physical characteristics of the material, while Γ is the portion due to geometric factors. Remember also that the population will be proportional to the current $n \propto i$, then rewriting in the particular case of the threshold gain

$$g_{th} = G'\Gamma(ki - n_{th}) = \alpha_l + \frac{1}{2L}\ln\left(\frac{1}{R_1R_2}\right)$$

obtaining a threshold current equal to

$$I_{th} = \frac{1}{K}\left\{\frac{1}{G'\Gamma}\left[\alpha_l + \frac{1}{2L}\ln\left(\frac{1}{R_1R_2}\right)\right]\right\}$$

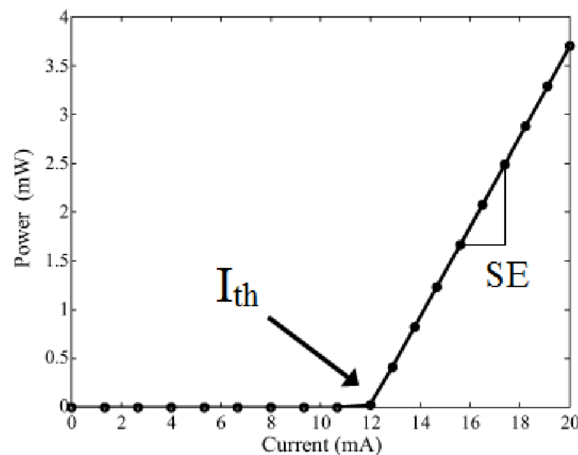


Figure 2.33: Ideal relationship optical power - current

Slope efficiency

The slope efficiency is a very important parameter for a laser diodes. It is typically obtained from the graph that relates the optical power emitted as a function of pumping: above the threshold, the graph tends to become a straight line, whose slope is the slope efficiency. The real curves are typically non-linear, typically showing a steep slope after the threshold, and a decrease of the slope at higher values due to increased losses and heating of the device at high power. The greater the slope efficiency, the greater the increase in output power caused by the same increase in the pumping, but high slope efficiency typically also involves a high threshold current. Consequently, the impact of these parameters should be carefully evaluated when designing a laser.

2.4.3 Structure

As just said, the quality of the laser depends on the intensity of the population inversion and on the density of photons in the cavity. Consequently, the laser diodes have a region as small as possible for the flow of the bias current, unlike the LEDs where we want to minimize the current crowding. The optical lateral containment is generally achieved through appropriate confinement layers with low refractive index in order to exploit the total internal reflection.

Multiple quantum wells

Lasers typically use, in order to have a thin active region, structures with multiple quantum wells (MQW). From the constructive point of view they are simply heterostructures of very reduced thickness, but inside them some very interesting quantum phenomena occur. First, in a quantum well (we suppose it has infinite energy depth and a rectangular shape for simplicity) the allowed energy levels are discretized, according to the relationship

$$E_n - E_c = \frac{h^2 n^2}{8 m_e^* d^2}$$

where E_n is the energy of the n-th level, E_c is the energy of the edge of the conduction band, n the quantum number, m_e^* the effective mass of the electrons and d

the width of the hole. In each of these quantized levels there is a two-dimensional electron gas, in which the density of states per unit of energy and volume is constant and is, for each level, greater than the one of a not quantized device. The electrons (and holes) are arranged mostly on the first available level, with well-defined energy. The charge density is greater, and the threshold current lower (by a factor of 50). When there are multiple quantum wells put together at a short distance, it establishes a phenomenon of quantum tunnel that leads to the creation of a continuum of quantized energy states in the active region. The quantization also leads to an increase in energy of the emitted photon, according to the relationship (as exemplified in figure 2.34)

$$E \approx E_{gw} + E_{e1} + E_{hh1}$$

and given the presence of discrete energy levels there is also a significant reduction in the width of the spectrum, because typically only the first of which is occupied.

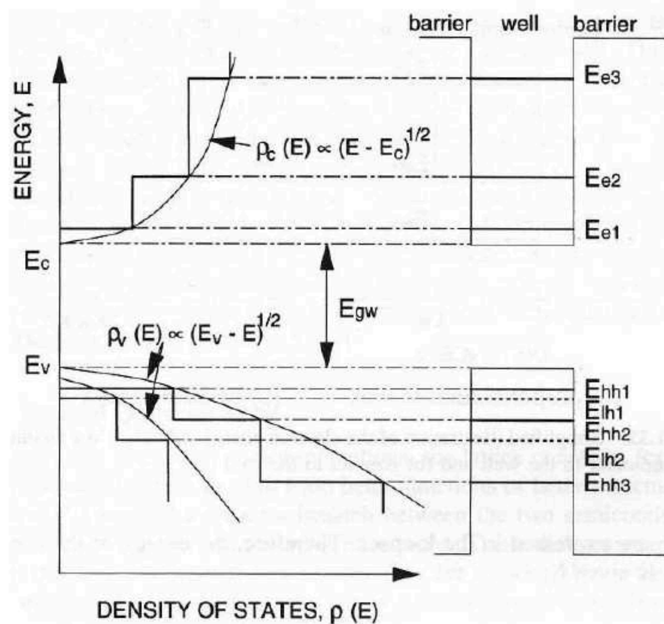


Figure 2.34: Band diagram of a quantum well

Gain guiding

In this type of devices the confinement of the current is obtained through a microstrip contact surface, which allows to reach high current densities in a small region.

The current density is greater in the region directly below the contact and less along the peripheral paths, and the optical gain follows its fluctuations. The main advantages of this structure are the reduction of the threshold current, due to the increase of the current density, and an easier coupling with waveguides (such as optical fibers), due to the smaller emission spot. The widths of the contacts may also be a few microns, giving rise to threshold currents in the order of tens of mA.

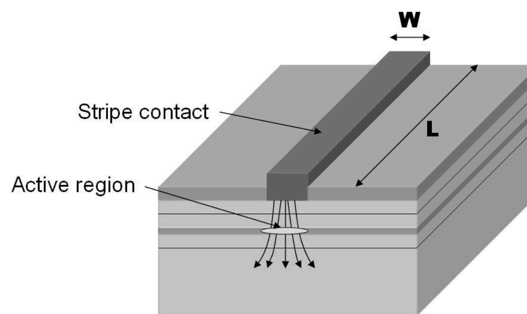


Figure 2.35: Struttura di un diodo laser *gain guided*

Index guiding

In these structures, the confinement is given not only by the contact, but also by special layers made at the edge of the active region. These layers have a lower refractive index in order to take advantage of the phenomenon of total internal reflection, ensuring the optical confinement of photons in the active region, with a consequent increase in the rate of stimulated emission and in the overall efficiency of the device. These structures, however, have also a disadvantage: the addition of layers of different materials in the proximity of the active region creates lattice mismatch, with all the problems already described, in the most important area of the device.

Distributed structures

The mirrors at the interfaces with the outside world are among the most critical parts of a laser diode, as evidenced by the fact that their reflectivity appears in almost all of the equations that characterize its operation. The mirrors can also be exploited to select the number and type of modes oscillating within the cavity, thus allowing (within certain limits) to determine the shape of the spot and the energy distribution

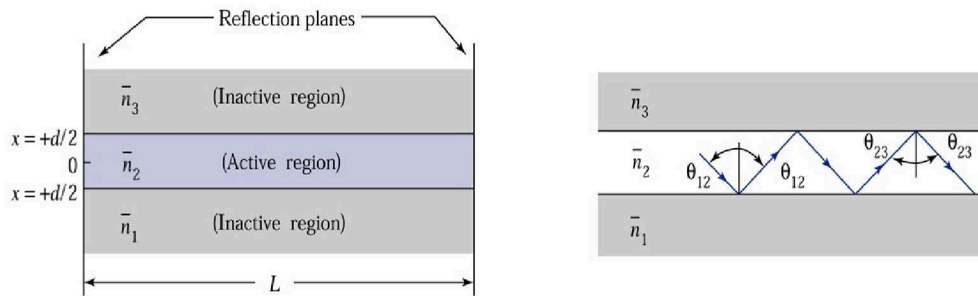


Figure 2.36: Confinement layers and total internal reflection in a index guided laser

in its interior. This result can be obtained in various ways.

- The easiest method is to insert an external mirror on which is prepared a diffraction grating: the wavelength of the radiation that returns within the active area (the edges of which are made of a suitable anti-reflective layer) is then selected by the angle between the grid and the axis of the cavity. This method is the simplest, but also the one that gives rise to higher power losses both for the efficiency of the grating and for the route taken from the edge of the active region to the grating. Moreover, the realization of this type of structure is typically expensive.

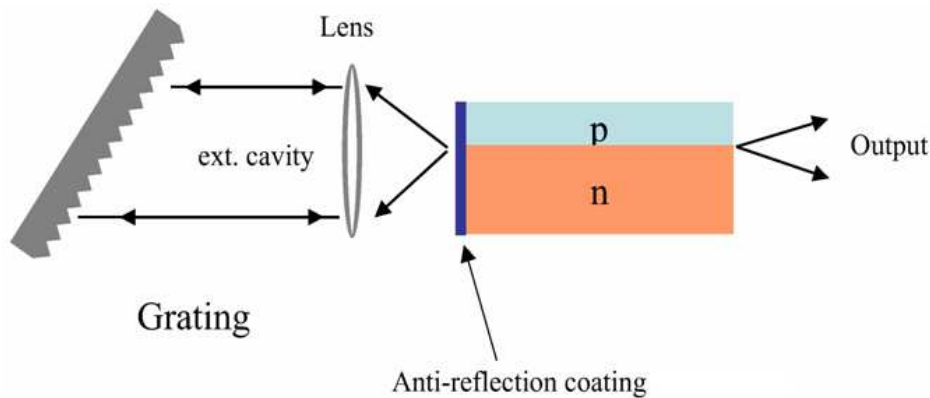


Figure 2.37: Structure with external diffraction grating

- A second method is to integrate a structure similar to the grating inside the chip at the edges of the active zone: the *distributed Bragg reflectors* (DBR). The operating principle is simple: every fold of the structure partially reflects the incident wave, and the superposition of all these waves originates the reflected

wave. In order to overlap constructively, the individual reflected waves must comply with the so-called Bragg's condition, i.e. the wavelength must be an integer multiple of the path difference $2a$. This allows to select the wavelengths λ_B (Bragg wavelengths)

$$\lambda_B = \frac{2an}{q}$$

where n is the refractive index of the dielectric which constitutes the Bragg reflector and q an integer called diffraction order. Consequently, the DBR has a high reflectivity for the various λ_B and low for the other wavelengths, allowing the establishment of a stable field of radiation only for the first ones. The specific wavelength can be selected using the curve of optical gain of the active medium.

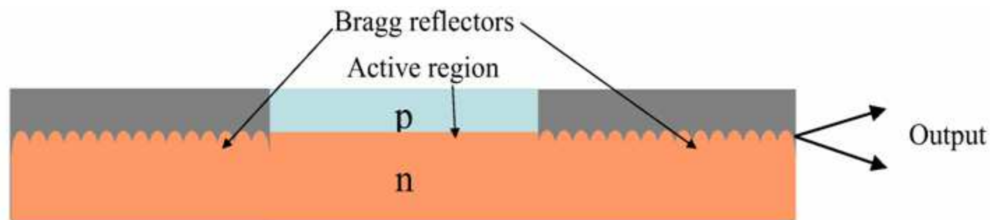


Figure 2.38: Distributed Bragg reflector

- The third method is to integrate the Bragg reflector within the active region, a technique called *distributed feedback* (DFB). In this case the operation is no longer determined by the simple constructive interference of the waves: indeed, along the optical path change both the gain and the index of refraction. The waves partially reflected from the folds of the structure are also partially amplified and have a different phase than the traveling waves. The problem is then to find the conditions for constructive interference between waves with different amplitudes and phases. The calculation is long and complex and gives as a result the relationship

$$\lambda_{osc} = \lambda_B \pm \frac{1}{2nL}\lambda_B^2(m+1)$$

where λ_{osc} is the wavelength that oscillates in the cavity, n the index of refraction of the material forming the folds, L the length of the corrugated area and m an integer. The first obvious conclusion is that the possible wavelengths do not coincide with the wavelength of Bragg. In addition. in these structure the threshold gain is proportional to $1/m^2$, thus leading to the selection of only the modes with low m (in real devices, the only modes with sufficient gain are those with $m = \pm 1$). The selection of the wavelength is very accurate as to give typically lines amplitude of about 0.1 nm. In contrast to the DBR devices, DFB devices are simpler to build and have less losses, and thus a lower threshold current.

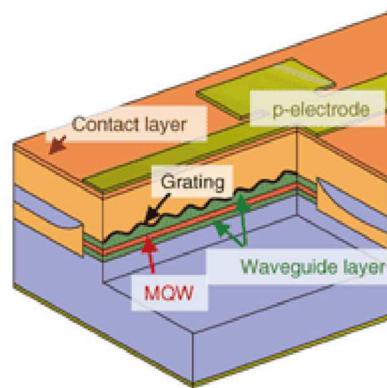


Figure 2.39: Distributed feedback structure

2.4.4 Reliability

Apart from what has been said previously in section 2.3 for LEDs, laser diodes have some additional reliability issues because due to their peculiar structure.

Catastrophic damage to the mirrors

The presence of mirrors at the edges of the cavity causes some reliability issues. The non-radiative recombination that occurs at the interface with the mirrors causes a local increase in temperature, due to the energy that is transferred to the crystal lattice. This increase in temperature causes a decrease of the energy gap, thus increasing the absorption and the temperature with a positive feedback. The increase in temperature can significantly degrade the faces of the mirrors or even cause it to

melt. This issue is currently under investigation by several research groups, as it constitutes one of the main problems that limit the reliability of the devices.

- Tang et al. have made studies on the temperature reached by the mirrors using experimental analyzes carried out with Raman spectroscopy [45].
- Henry et al. report evidences that the beginning of thermal degradation happens at temperatures between 120 ℃ and 140 ℃ [46].
- Menzel et al. show how the temperature of the mirrors is dependent on the rate of non-radiative recombination at the surface, and that this temperature increase occurs within a radius of about 1 μm, leaving relatively "cold" the rest of the cavity [47].
- Chen et al. indicate a relationship between the length and thickness of the active zone and the degradation, for both heterostructures and MQW. The decrease in light absorption in the MQW reduces the photogeneration of carriers, increasing the transparency of the mirrors and reducing the temperature rise compared to heterostructures [48].
- Houle et al. studied the changes in chemical composition of the surface of the mirrors. This composition is quite variable even for devices produced and never biased, and changes considerably even in the early stages of operation. In particular, they noted that the merging of the interfaces has not taken place in all devices that have suffered catastrophic damage to the mirrors, and that the greater oxidation of the interfaces is not necessarily related to this type of damage [49].

Catastrophic optical damage

This type of problem has been described and analyzed by Magistrali et al. [50]. This group has observed a decline in the power emitted before there was any visible degradation of the optical cavity, with a subsequent very quick degradation. Analysis carried out with the transmission electron microscope (TEM) showed a dense network of dislocations within the active region, associated with dislocations within the adjacent layers. The suggested explanation is the slow propagation of dislocations within

the material due to non-radiative recombination. When these dislocations reach the MQW their propagation becomes very rapid due to the high current density, causing a rapid decline of the performances of the device.

Chapter 3

High Electron Mobility Transistors

High Electron mobility transistors can be used as switches for power electronics applications and as amplifiers in radio frequency circuits. This wide field is partially explained by the good physical characteristics of the Gallium Nitride described in the previous chapter, but the structure and the operating principles of the transistor have a relevant role in the exploitation of the material possibilities and than have to be carefully described and designed.

3.1 Conductive channel

The channel is the most important part of the device, since it directly affects its resistivity, the maximum output current, the withstood power dissipation, the sustained off-state voltage and the amplification. The formation of the channel make use of the specific spontaneous polarization of the Gallium Nitride and of the piezoelectric polarization induced by the AlGaN barrier to create a two dimensional electron gas (2DEG) with an high sheet carrier density.

3.1.1 Spontaneous polarization

The spontaneous polarization is the polarization in the material when no external strain is applied, and it can be very large for wurtzite GaN crystals, where its typical value is $P_{sp} = -2.9 \times 10^{-6}$ C/cm^2. The different electronegativity of the atoms (Ga: 1.756, N: 3.066) in the lattice causes a non-uniform distribution of the bonding electrons inside the material, resulting in the concentration of the bonding electrons nearer to the Nitrogen, which behaves as anion, while the Gallium is the corresponding

cation. A polarization vector forms inside the material, with positive direction from the cation to the anion along the c axis. Figure 3.1 reports a representation of this process, in our case the cation M is a Gallium atom (or an Aluminum atom for $Al_xGa_{1-x}N$).

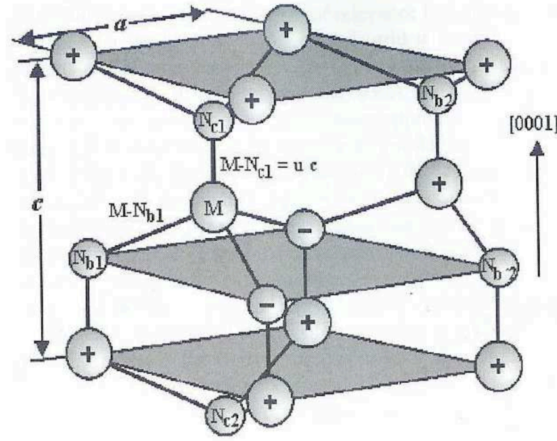


Figure 3.1: Creation of the spontaneous polarization vector inside a MN wurtzite crystal with lattice constants a and c.

3.1.2 Piezoelectric polarization

Besides the spontaneous polarization, also a piezoelectric polarization exists when the material is submitted to external tensile or compressive strain (see page 25). In an heterostructure, the strain is caused by the different lattice constants of the various materials, which give a complex situation after the pseudomorphic growth (see figure 3.2).

The piezoelectric polarization P_{pe} is related to the strain tensor ϵ_{ij} by the piezoelectric coefficients e_{ijk} as

$$P_{pe} = e_{ijk}\epsilon_{ij}$$

In a wurtzite crystal, the elastic tensor C depends only on five linearly independent elastic constants [52]

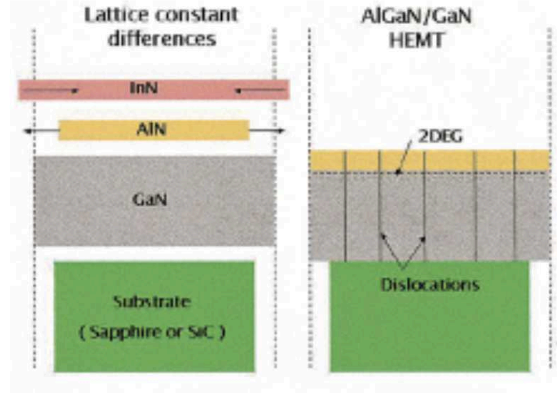


Figure 3.2: Strain created by the different lattice constants after pseudomorphic growth [51].

$$C = \begin{bmatrix} C_{11} & C_{12} & C_{13} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{13} & 0 & 0 & 0 \\ C_{13} & C_{13} & C_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{44} \end{bmatrix}$$

Only two of the components of the piezoelectric tensor are related to the piezoelectric polarization along the c axis:

$$P_{pe} = e_{33}\epsilon_z + e_{31}(\epsilon_x + \epsilon_y)$$

where $\epsilon_z = (c - c_0)/c_0$ is the strain along the c axis, $\epsilon_x = \epsilon_y = (a - a_0)/a_0$ are the strains between the planes and e_{31}, e_{33} the piezoelectric coefficients. Since the relationship between the lattice constants is given by

$$\frac{c - c_0}{c_0} = -2\frac{C_{13}}{C_{33}}\frac{a - a_0}{a_0}$$

the piezoelectric polarization can be expressed as

$$P_{pe} = 2\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right)$$

The strength and the direction of the spontaneous and piezoelectric polarization vectors of every material depends on the substrate, the growth orientation, the nature of the surface (Ga-face or N-face), the thickness (which influences only the magnitude) and the strain type (tensile or compressive). Since for AlGaN

$$e_{31} - e_{33}\frac{C_{13}}{C_{33}} < 0$$

the piezoelectric polarization is negative for a tensile strain and positive for a compressive strain of the AlGaN barrier, and if we take into account figure 3.2 we can conclude that structures with an AlGaN layer over a GaN substrate have a total polarization equal to the sum of the two terms

$$P = P_{sp} + P_{pe}$$

The polarization constants increase from GaN towards AlN, and then the total polarization of the strained AlGaN layer is greater than the one of the more relaxed GaN buffer

$$|P(\text{AlGaN})| > |P(\text{GaN})|$$

Both the polarization vectors in AlGaN and in GaN are directed from the Nitrogen atom to the nearest cation (Ga or Al), so the net polarization is directed along the c axis and points towards the substrate for Ga-face and towards the surface for N-face materials (see figure 3.3).

3.1.3 2DEG formation

The formation of the channel is caused by the presence of the polarization fields. Figure 3.4 reports the effect of the polarizations on the conduction band diagram, and the large zone under the Fermi level which is filled by electrons is strongly reduced or vanishes if the polarization is removed. The charge density induced by the polarization is given by

$$\rho_p = -\nabla \bullet P$$

If the charge is positive, free electrons will move to compensate this charge, resulting in the creation of a conductive two dimensional electron gas at the heterointerface. Then, the most favorable case is AlGaN on top of a Ga-face GaN buffer, which gives the highest sheet charge density. The electron concentration n_s in an undoped AlGaN/GaN heterojunction can be calculated as

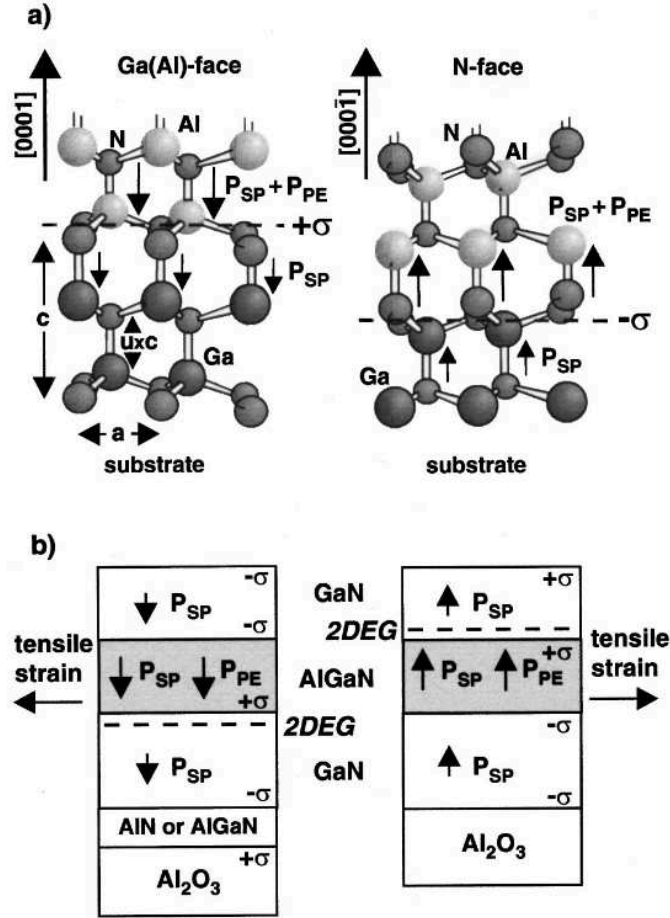


Figure 3.3: (a) Crystal structure and polarization of pseudomorphic AlN/GaN heterostructures with Ga(Al)-face or N-face structure. (b) Polarization in pseudomorphic GaN/AlGaN/GaN heterostructures with Ga-face or N-face polarity [53].

$$n_s(x) = \frac{\sigma(x)}{q} - \left(\frac{\epsilon_0 \epsilon(x)}{t_{AlGaN} q^2}\right) [q\phi_B(x) + E_F(x) - \Delta E_C(x)]$$

where x is the $Al_xGa_{1-x}N$ molar fraction, ϵ the relative dielectric constant, t_{AlGaN} the thickness of the AlGaN layer, ϕ_B the Schottky barrier height of the gate contact, E_F the Fermi level and ΔE_C the conduction band discontinuity. We can see that an increase of the Schottky barrier and a decrease of the thickness of the barrier layer have a negative impact on the charge density, which is entirely composed by the polarization charge. In this equation the dependence of σ on x has been highlighted, since the piezoelectric polarization strongly depends on the molar fraction. The piezoelectric constants of the system are related by

$$e_{ij}(x) = [e_{ij}(AlN) - e_{ij}(GaN)]x + e_{ij}(GaN)$$

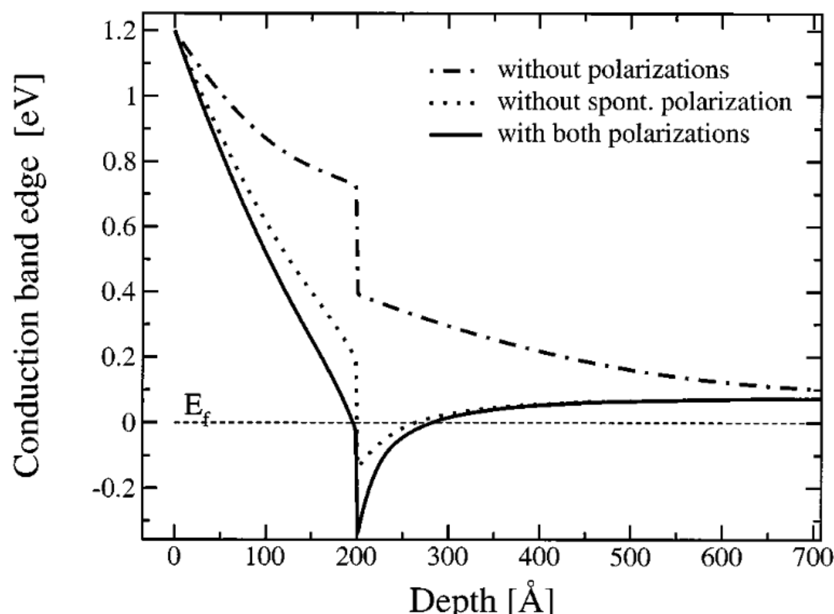


Figure 3.4: Conduction band edge with and without polarizations [54].

Ambacher et al. [53] have extensively studied this situation, and they found that the variation of $e_{31}(x)$ is very small, while $e_{33}(x)$ increases strongly with the Aluminum concentration (see figure 3.5).

Moreover, the relationship between the spontaneous polarization and the Aluminum content was found to follow the equation

$$P^{sp}_{AlGaN}(x) = -0.090x - 0.034(1-x) + 0.021x(1-x) \quad \left[\frac{\mathrm{C}}{\mathrm{m}^2}\right]$$

The positive effect of an increased Aluminum content is not constant: for values of x higher than 0.4 the AlGaN layer becomes an insulator, and also gives birth to a more defective material with an increased scattering and then reduced mobility. It is necessary to accurately design the values of the molar fraction and of the barrier thickness in order to obtain the best performances. Figure 3.6 reports the 2DEG carrier density as a function of x for different AlGaN thicknesses. The solid line is the curve of the critical thickness, i. e. the ideal thickness of the fully-strained layer.

We have analyzed the effect of several parameters on the sheet density, but it is still not clear the origin of the charges that form the channel. The most supported hypothesis is that the electrons come from the surface trap states [56]. Below a certain thickness of the AlGaN layer the concentration of carriers is very low since

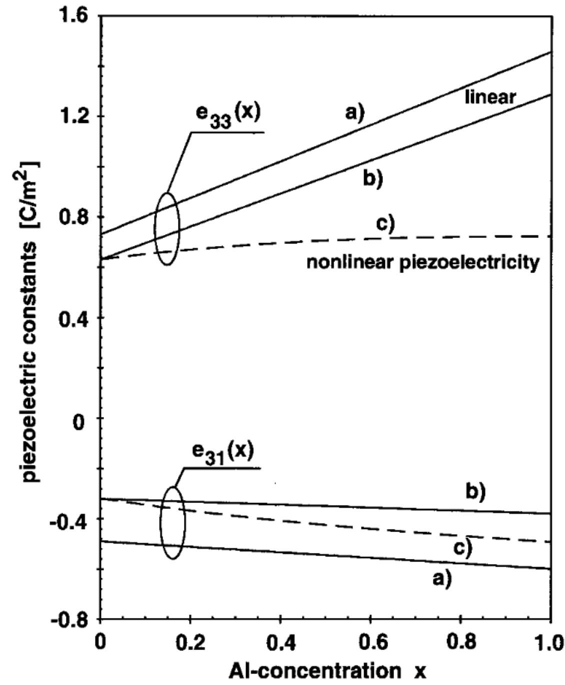


Figure 3.5: Piezoelectric constants as a function of Aluminum content in a Al-GaN/GaN structure [53].

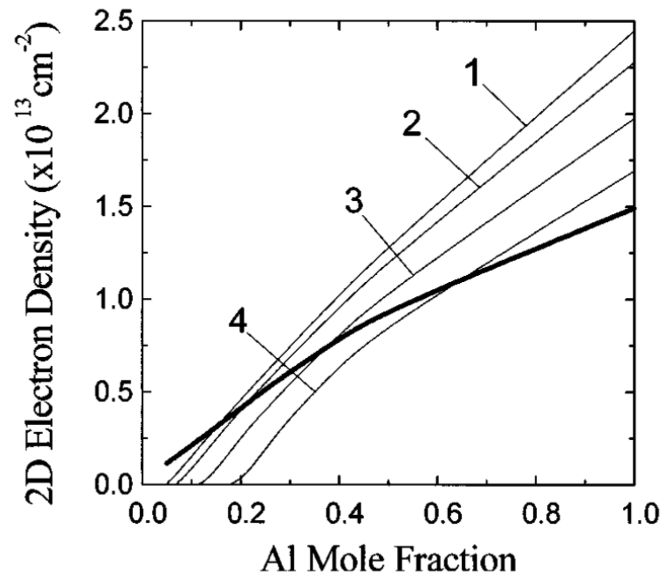


Figure 3.6: Electron sheet density induced by piezoelectric effect in heterostructures with different aluminum molar fraction and various AlGaN barrier layer thicknesses. 1: 30 nm; 2: 20 nm; 3: 10 nm; 4: 5 nm [55].

the surface trap energy level is below the Fermi level, and then the channel charge is confined inside the defective states. When the thickness is increased the channel density rises, since the traps move upside the Fermi level and donate their electrons to the heterointerface, and then reaches a saturation value, when all the surface levels are emptied. Figure 3.7 shows the band diagrams during this process and figure 3.8 the good correlation between this theoretical explanation and the experimental data.

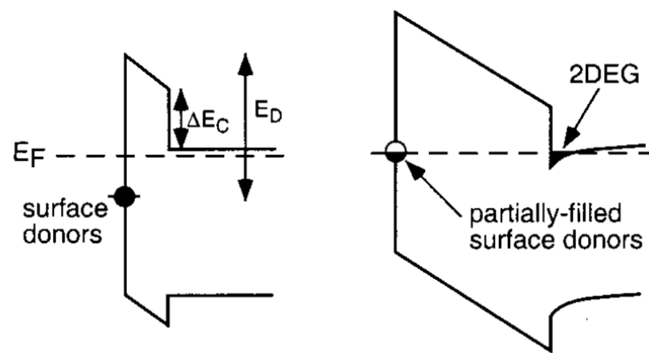


Figure 3.7: Band diagrams of the surface charge donor model of channel formation [56].

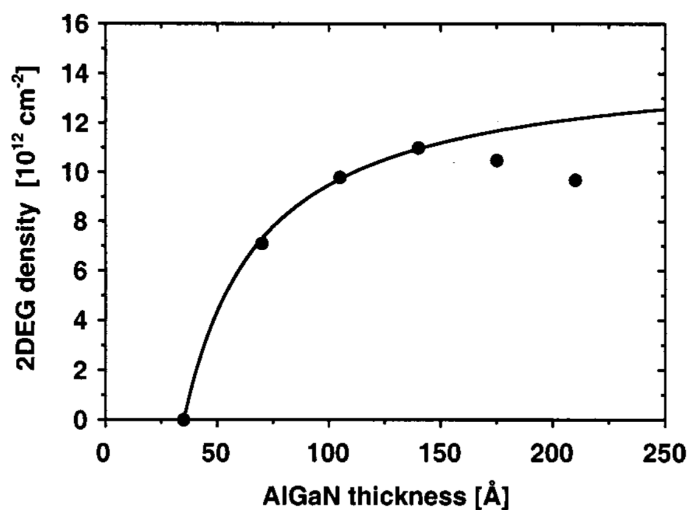


Figure 3.8: Channel density as a function of the barrier thickness: model and experimental data [56].

3.2 Schottky gate contact

The Schottky contact at the gate is a critical region for a HEMT, since it defines the leakage current and allows to deplete and create the conductive channel. If we consider the contributions to the total gate current, typically the thermoionic emission (TE) component prevails, which can be expressed as

$$J = A^*T^2\mathrm{exp}\left(-\frac{q\phi_B}{k_BT}\right)\left[\mathrm{exp}\left(\frac{qV}{nk_BT}\right)-1\right]$$

where A^* is the effective Richardson constant, T the absolute temperature, ϕ_B the barrier height and n the ideality factor. Anyway, it is necessary to take into account also the quantomechanical effects of reflection and tunneling through the barrier; in this case the carriers are emitted due to the applied electric field, and then the theory is called *Field Emission, FE* [57, 58], or *Thermoionic Field Emission, TFE* if the effect of the temperature is also considered [59, 60]. Without going into excessive detail with the long derivation, the current is given by

$$J = -J_s\mathrm{exp}\left\{\frac{qV}{E_0}\left[\frac{E_0}{k_BT}-\tanh\left(\frac{E_0}{k_BT}\right)\right]\right\}$$

where

$$J_s = A^*T\frac{\sqrt{\pi E_0}}{k_B}\left[q(V-V_n)+\frac{q\phi_B}{\cosh^2(E_0/k_BT)}\right]^{1/2}\mathrm{exp}\left[-\frac{q\phi_B}{\coth(E_0/k_BT)}\right]$$

and

$$E_0 = \frac{q\hbar}{2}\sqrt{\frac{N_D}{m^*E_s}}$$

We can now analyze in more detail what happens in an AlGaN/GaN HEMT. The most used metal for a Schottky contact are Ni, Pt, Mo, Ir, Au, Ag, Ni/Au and Pt/Au, and sometimes more complicate combinations such as Ni/Pt/Au, Ni/Au/Ni, ITO and Ni/ITO. It is useful to point out that, since the HEMT is a lateral device, also the current flows laterally on the surface or at the AlGaN/GaN interface. For this reason, the forward conduction can be easily explained using the TE theory, but the reverse current deviates from this study. Moreover, the TFE and FE theories are reliable only if the material is highly doped ($N_D > 10^{17}$), but this is not the case for a

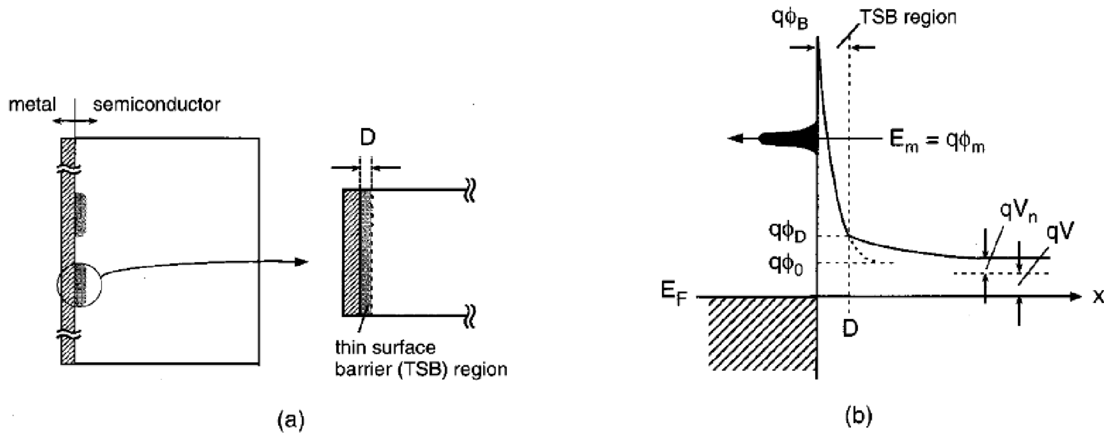


Figure 3.9: Schematic of the TSB model (a) and its band diagram (b) [64].

usual bulk [61, 62]. For this reason, the Thin Surface Barrier (TSB) model has been introduced [63]. Unintentional donors create a reduction of the Schottky barrier, and this explanation fits well the experimental data (see figure 3.9).

More detailed models have been developed in order to explain the high leakage current of AlGaN/GaN Schottky diodes, such as the *Trap-Assisted Tunneling* and the *Thermoionic Trap-Assisted Tunneling* [65]. Moreover, the *Poole-Frenkel* effect has been considered. The Poole-Frenkel effect describes the electrical conduction in an insulator as the hopping between localized states helped by an high electric field, which effectively lowers the barrier seen by the carriers [35]. The amount of this reduction, as seen in figure 3.10, is

$$\Delta_{q\phi} = \beta\sqrt{E}$$

where

$$\beta = \sqrt{\frac{q^3}{\pi\epsilon}}$$

is the Poole-Frenkel constant, E the applied electric field and ϵ the dielectric constant.

The current density contribution of this effect is given by

$$J \propto E\text{exp}\left[\frac{-q\left(\phi_B - \sqrt{qE/\pi\epsilon}\right)}{k_B T}\right]$$

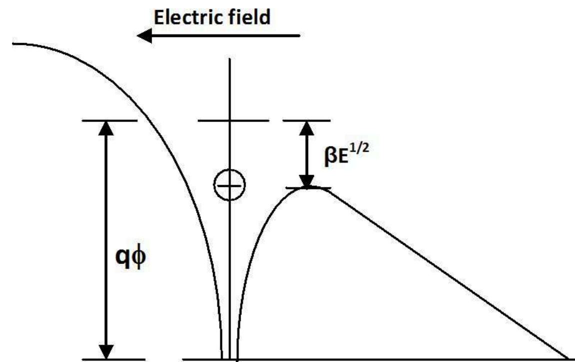


Figure 3.10: Poole-Frenkel barrier lowering [66].

The vertical conduction may be due to Poole-Frenkel emission through the AlGaN layer [67], while the lateral conduction to the same mechanism on the AlGaN surface [68]. Then, since defects act as localized states for the electrons, their concentration in directly related to the gate leakage current.

3.3 Trapping effects

The charge trapping is probably the most important mechanism that limits the performance of a HEMT. Defects are created by the growth of materials with a less than perfect lattice, by the interfaces between materials (included the surface) and by the typical operation of the device (see figure 3.11). Each defect acts as a deep level which can trap charge, reducing the dynamic response of the device and its steady - state output current, or increasing the on-resistance.

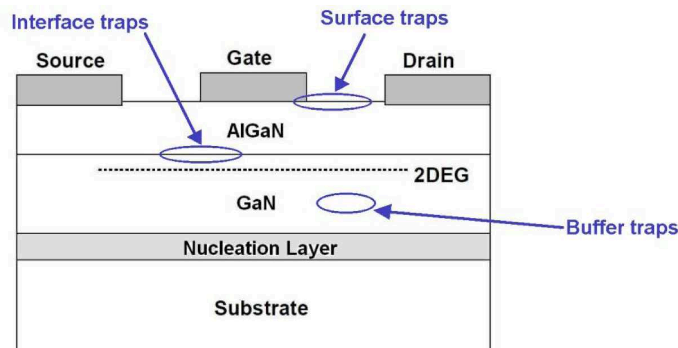


Figure 3.11: Some of the typical locations of defective states in an AlGaN/GaN HEMT.

Other common effects are the *kink* and the *current compression*. In the first case, we are referring to a variation of the ID-VD curve of the device induced by a relatively low trapping voltage, and a very low VD voltage is sufficient to bring the device back to its usual current values, so that the result on the output characteristic is the presence of a kink in the curve (see figure 3.12) [69].

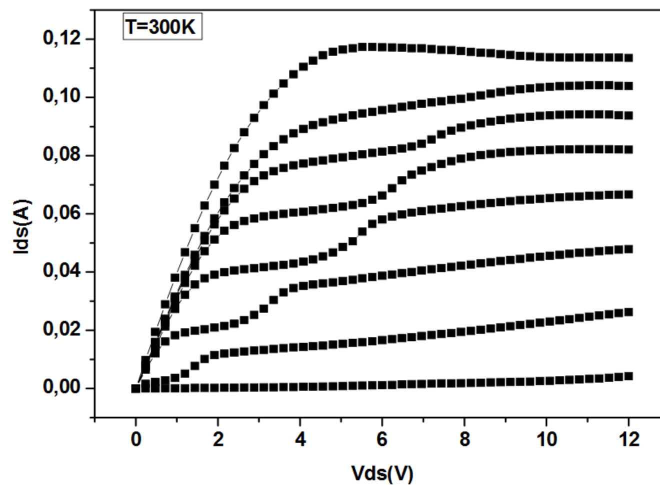


Figure 3.12: Typical output characteristic showing kink effect in an AlGaN/GaN HEMT [70].

The current compression is mainly due to the trapping of charge on the surface of the device, which can be assumed to be a natural donor. When high gate - drain electric fields are applied, these levels can be filled by electrons provided by the gate contact. There is then the formation of a region where the channel is partially controlled (i. e. depleted) by the fixed charge on the surface, which behaves as a *virtual gate*. This behavior is shown in figure 3.13.

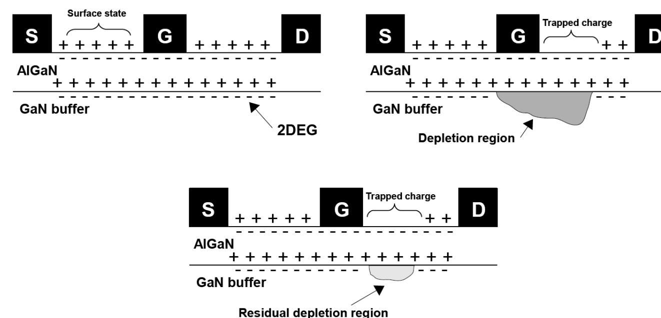


Figure 3.13: Formation and effect of the virtual gate.

In order to prevent this effect, it is possible to passivate the surface using a Silicon Nitride layer, as described in figure 3.14. This allows to remove at least a part of the dangling bonds, surface defects and foreign incorporated atoms, restoring most of the current.

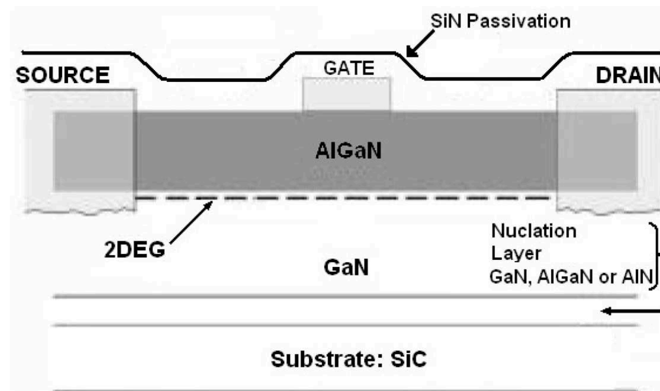


Figure 3.14: Passivating SiN layer.

Another design that helps reducing the trapping effects is the presence of a *field plate*, a conductive structure placed over the passivation and terminated (i. e. in electrical contact) towards the source or the gate. The effect of the field plate is to reduce the peak electric field at the gate edge, creating another smaller peak at the edge of the field plate (see figure 3.15). Since the trapped charge is composed by highly energetic electrons, a reduction of the maximum field causes a reduction of the maximum acceleration and then of the concentration of electrons that possess an energy high enough to be trapped.

A complete dissertation on the trapping mechanisms and effects would require many books and is outside the aim of this thesis, so only the two main mechanisms are presented here and in every section of the experimental results will be described the specific effect that takes place in that occurrence.

3.4 Reliability issues

The typical structure and operating principles of a HEMT has been extensively described. Given the high number of layers and critical regions, and the high bias levels and power dissipation these devices have to withstand, there are some effects

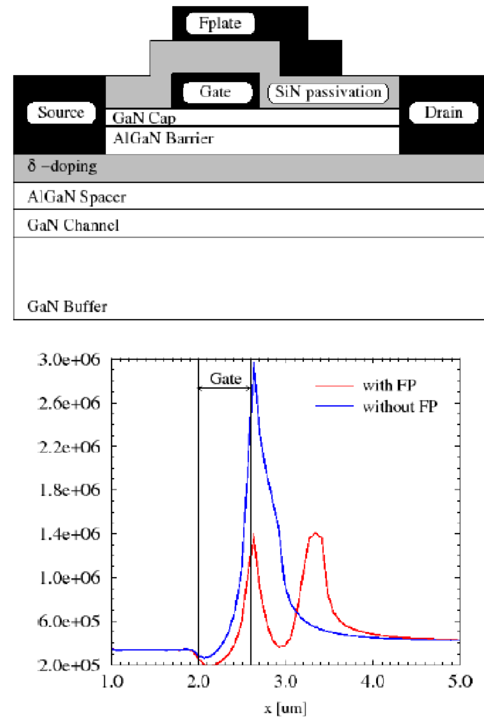


Figure 3.15: Field plate and its effect on the electric field distribution.

that can induce variations inside the device, causing a variation of its performances. These degradation aspects limit the reliability of the transistor, which is a critical parameter for real applications. Most of them are represented in figure 3.16.

The degradation mechanisms can be divided into three groups:

1. thermally-activated modifications of the structure: changes of the metal interconnects, of the ohmic contacts, of the gate metal and the delamination of the passivation;

2. effects caused by highly-energetic electrons, which include the trapping of the carriers in various regions of the device and the creation of defects due to the collision between the accelerated charges and the atoms of the lattice;

3. mechanisms related to the AlGaN/GaN structure, such as the degradation at the gate edge caused by an high electric field, the creation of defects due to high external electrical, thermal and tensile stimuli, and the source - drain punchthrough.

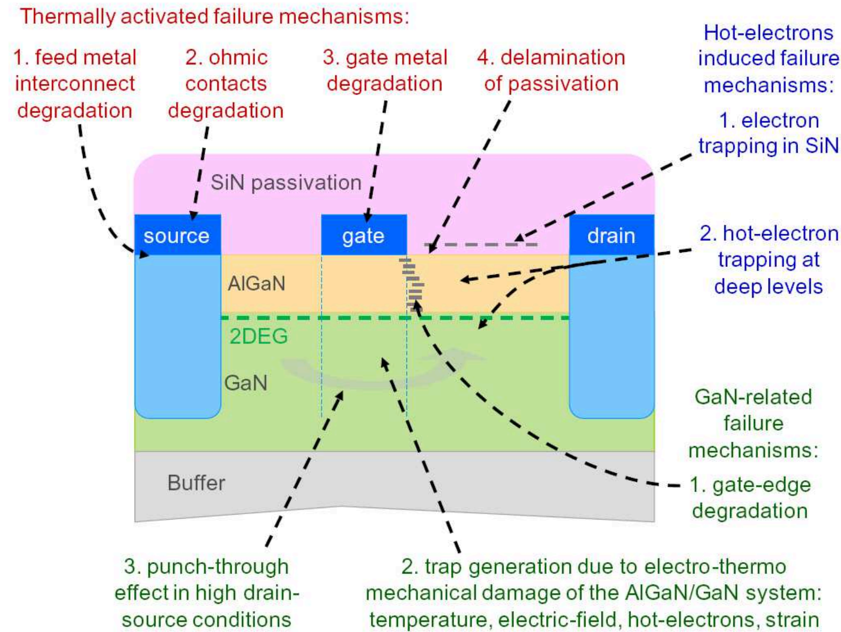


Figure 3.16: Summary of the critical reliability aspects for a GaN HEMT [71].

3.4.1 Gate-related mechanisms

The gate leakage current is one of the most critical aspects for the performances of a HEMT, since it affects the quantity of the charge modulated by the gate voltage and causes an unwanted power dissipation, which reduces the overall efficiency of the system. It is then important to study the physical degradation mechanisms that can change its value.

Contact degradation

The gate contacts are generally stable at high temperatures, but the interdiffusion of the metal inside the semiconductor or inside another metal of the gate stack can create defects, increased strain and contamination of the material, causing a variation of the electronic properties [72]. The main mechanisms reported in the literature are

- an increase of the gate leakage current and of the drain current, caused by the migration of Au atoms along the gate edges towards the AlGaN [73];
- an increase of the Schottky barrier height and a simultaneous decrease of the ideality factor, ascribed to the migration of Au [74, 75];

- a positive shift of the threshold voltage, caused by the migration of Au through the Ni towards the AlGaN [76];
- the increase of the gate leakage current due to the consumption of the Ni [77];
- a sudden degradation caused by the formation of NiSi between the Ni metal and the SiN passivation [78].

Failure mechanisms

A critical region for the reliability of a transistor is the gate edge, since the electric field has its highest value. Under this stress condition, a lot of defects can be created, which increase the gate leakage current due to the trap-assisted tunneling mechanism of electrons from the gate to the AlGaN barrier [79]. The specific reasons for the formation of defects are several:

- *Inverse piezoelectric effect*: given the strong spontaneous and piezoelectric polarization of GaN and AlGaN and the very high vertical electric field, the barrier layer is submitted to a significant tensile stress, even when no bias is applied (see figure 3.2). If a strong reverse bias is applied, the vertical electric field at the gate-drain edge increases abruptly, until the amount of induced strain is high enough to create lattice defects in the AlGaN, as shown in figure 3.17 [80].

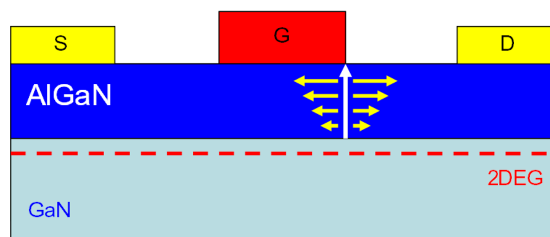


Figure 3.17: Piezoelectric tensile stress caused by an high electric field in the AlGaN barrier of a GaN HEMT [81].

- *Time-dependent AlGaN breakdown*: when a transistor is biased at a strong negative voltage for some time, initially the gate current drops due to the trapping of some electrons until a saturation value, then after some time the noise of the current increases and at the end the current exhibits a sharp variation. The

significant time of this processes are strongly dependent on the applied voltage value. This phenomenon can be explained by a mechanism similar to the time-dependent dielectric breakdown: the time-dependent AlGaN breakdown [77, 82]. The dynamic creation and destruction of defects is the responsible of the noisy current, until their percolation through the AlGaN creates a larger conductive path responsible for the sudden increase of the conductivity.

- *Surface oxidation*: reverse bias can induce the formation of oxide clusters at the gate edges due to an electrochemical reaction, and in correspondence with them several pits are formed that enhance the gate leakage current [83].

- *Pitting*: after a long DC stress at high temperature in on-state condition, on the devices is found a pit-shaped defect at the drain side of the gate edge in the barrier [84]. Moreover, sometimes a crack forms below the pit, and in many cases there was the presence of Oxygen in correspondence of these newly-created defects [85].

- *Forward gate current*: when a HEMT is operated at high VGS levels, the value of the forward current of the gate diode can reach a significant level. Since this current flows through the device during all its operating time (and not only for the short time required to measure its characteristics), over time there can be the creation of a significant amount of defects, which reduce its dynamic performances and further increase the flow of carriers [86].

3.4.2 Hot electrons

During stress tests in on-state at different gate voltage levels, it can be found a decrease of the drain current and an increase of the on-resistance which has a non-monotonic dependence on the gate voltage [71]. Since the time to failure (TTF) evaluated from these parameters is well correlated with the variation of the electroluminescence as a function of the gate voltage, it can be assumed that the two effects are caused by the same origin. The electroluminescence is caused by the bremsstrahlung of hot electrons, it can be concluded that the degradation itself strongly depends on the presence of hot electrons. This highly-accelerated carriers can move towards the

heterointerface, into the AlGaN barrier or even into the SiN passivation, and from this region they can't be drained anymore (at moderate voltage levels). This fixed trapped charge explains the decrease of the transistor performances.

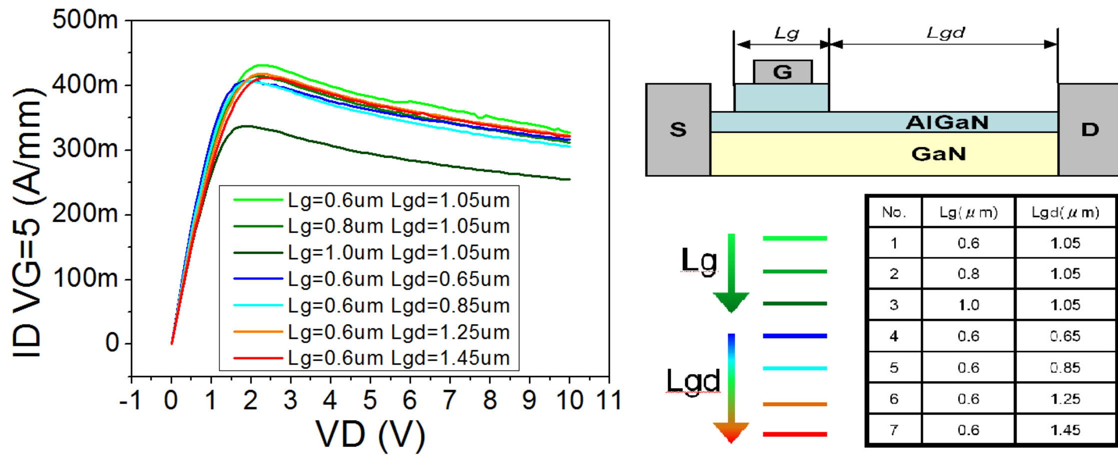
3.5 Gate Injection Transistors

High Electron Mobility Transistors (HEMTs) based on Gallium Nitride are promising devices for power and high frequency electronics. The mobility typical of AlGaN/GaN heterojunction allows for high frequency operation, and the possibility of driving GaN-HEMTs at high voltages makes these devices ideal for application in the power electronics field. The use of GaN HEMTs in power applications is still limited by their normally-on behavior, and by a number of reliability issues. Moreover, the use of high bias values can generate trapping phenomena, thus reducing the dynamic characteristics and the overall performance. Recently, a novel device structure was proposed, the Gate Injection Transistors (GITs) [87]. A GIT is in principle very similar to an HEMT, with a p-AlGaN layer under the gate metal contact. This p-doped region has the effect of rising the lower edge of the conduction band near the channel region, allowing normally-off operation. Moreover, when a gate voltage higher than the built-in voltage of the gate diode is applied, hole injection from the p-type region to the channel increases, resulting in conductivity modulation and higher drain current [87]. These transistors exhibit a good stability when an external drain field is applied, showing almost no current collapse.

One of the main parameters for a device used as a power electronics switch is its on-resistance: higher resistances increase the voltage drop across the transistor, resulting in additional dissipated power that reduces the overall efficiency of the circuit. GITs are able to carry high current densities while having a low resistivity. Figure 3.18 shows the typical output characteristics of those devices as a function of their dimension, and figure 3.19 confirms that the resistance is due to the total length of the path the current has to flow into and not to additional parasitic components, such as a not-perfect deposition of the ohmic contacts. The total length of the channel is equal to

$$L_{tot} = L_{gs} + L_g + L_{gd}$$

where L_{gs}, L_g and L_{gd} are, respectively, the gate - source spacing, the length of the p-AlGaN layer and the gate - drain distance. In figure 3.19 the contribution of $L_{gs} = 1$ μm is neglected, since it is the same for all the devices.



No.	Lg(μm)	Lgd(μm)
1	0.6	1.05
2	0.8	1.05
3	1.0	1.05
4	0.6	0.65
5	0.6	0.85
6	0.6	1.25
7	0.6	1.45

Figure 3.18: Output characteristic of a GIT as a function of the device dimensions.

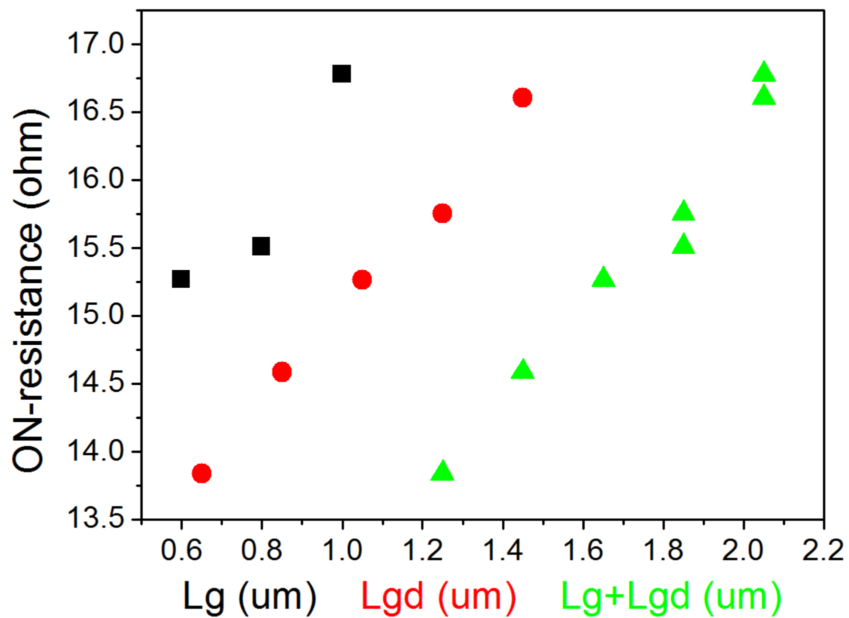


Figure 3.19: On-resistance of various GIT samples.

3.6 Natural SuperJunctions

Semiconductor junctions with a rectifying behavior are very important for all the devices that require blocking capabilities. In order to obtain the best performances from these elements, it is necessary to have both an high reverse breakdown voltage (which allows the device to withstand higher voltages) and a low on-resistance (to reduce its power dissipation). This is difficult to obtain with a common p-n junction: its breakdown voltage depends on the dopant concentration and on the thickness of the material, and is higher when they are respectively decreased and increased. However, in this case the resistance of the device sharply rises, because a lower dopant concentration gives less free carriers that can be moved by the electric field and because a thicker material is more resistive, since the resistivity is (theoretically) constant per unit of thickness. It can be used junctions based on Silicon Carbide, which has an higher breakdown field compared to Silicon, but the basic working principle of the junction is the same. in order to avoid this problem, it is necessary to rely on a completely different device.

Recently has been suggested an approach based on superjunctions, i. e. thin p and n layers vertically juxtaposed and laterally contacted. In this case, when the device is reverse biased the semiconductor is depleted of the free carriers, and only the positive fixed charges of donors in the n-type material and the negative fixed charges of acceptors in p-type material remain. The average charge density is null, since the negative charges are electrically compensated by the positive charges, and the breakdown voltage is increased. This explanation gives the expected results only if the dopant concentrations are perfectly equal, and this is impossible with the current technological processes. The Semiconductor Device Research Center, Semiconductor Company, Matsushita Electric Industrial Co., Ltd., of the Panasonic Corporation has developed a natural type of superjunction (Natural SuperJunction NSJ), based on the intrinsic polarization of the AlGaN/GaN stack. All the analyses in this thesis were carried out in close cooperation and on devices provided by the Semiconductor Device Research Center, so the basic description of the devices will follow what has been reported by Ishida et al. in [88].

The following description will consider the model of figure 3.20. When the device is

under zero bias, free charges e^- and h^+ are induced on the top and bottom surfaces by the polarization charge Pr^+ and Pr^-, to compensate their electric field. If an increasing reverse bias is applied, the free carrier slowly begin to deplete until only the polarization charge remains inside the device. In this case, the average charge is nearly zero, due to the almost perfect balance of the polarization charges. The absence of a net charge profile implies a constant electric field inside the semiconductor, and then a linear dependence of the breakdown voltage on the anode - cathode distance with no saturation, as confirmed by the experimental data of figure 3.21. When a forward bias is applied, the free charges induced are moved by the voltage, and given their high mobility and density it is possible to have very low on-resistances. The device structure just described is completely symmetric in the anode - cathode direction: in order to achieve a unidirectional behavior a Schottky diode is added at one of the electrodes, obtaining a Schottky Barrier Diode (SBD).

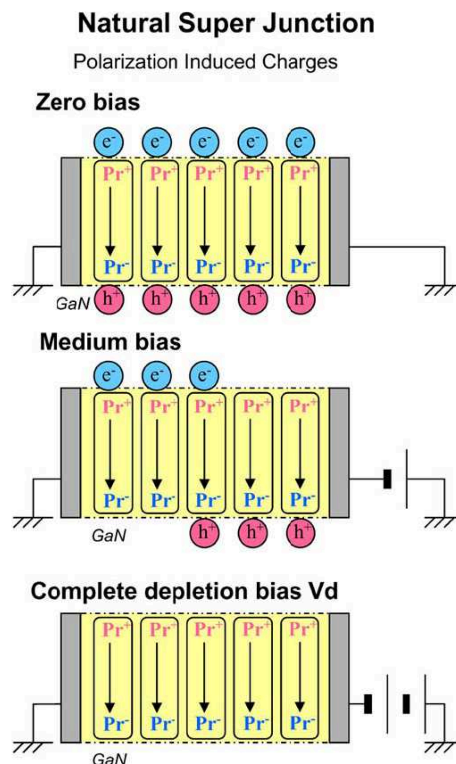


Figure 3.20: Model of a natural superjunction. e^-: free electron, h^+: free hole, Pr^+: positive polarization charge, Pr^-: negative polarization charge [88].

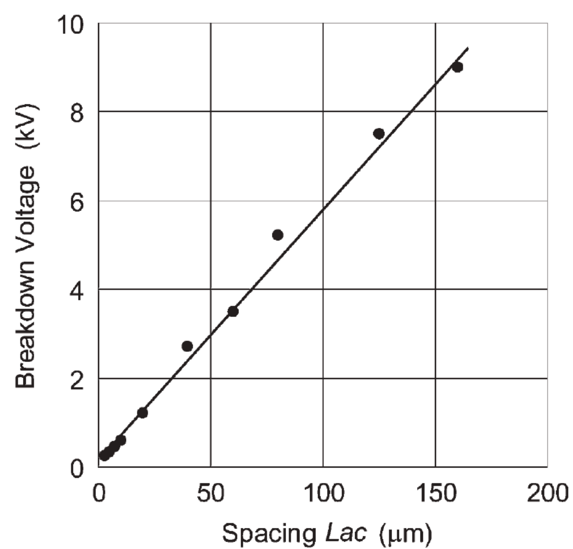


Figure 3.21: Measured breakdown voltages of AlGaN/GaN Schottky Barrier Diodes as a function of the anode - cathode distance (Lac). [88].

Chapter 4

Theory of measurements

4.1 Current - voltage relationship

These measurements consist on measuring the current that the device reaches for various applied voltages, and analyze their changes after the stress in order to understand what changes it has imposed on the component. In addition to what is described at page 35 , it is possible to carry out a more detailed analysis of the individual contributions to the final characteristic.

Diode forward bias

The application of a forward voltage at the terminals of the junction involves a bending of the band diagram, which causes the generation of a current due to the composition of the contributions of drift and diffusion of carriers. The behavior of a forward - biased junction is described by

$$I_F = A_{pn}(J_{diff} + J_{NR}) + A_{sur}J_{sur}$$

where A_{pn} is the area of the junction and A_{sur} the external surface. The current is composed by three different contributions:

- the diffusion current;
- the generation/recombination current;
- the superficial recombination current.

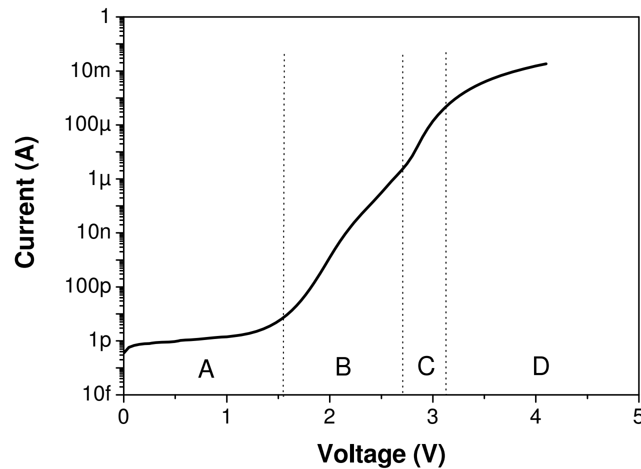


Figure 4.1: Contributions to the current of a diode

Figure 4.1 identifies four different regions, and each one is characterized by a different conductive mechanism:

- **region A**: at low voltages the surface recombination current dominates, its density is $J_{SUR} = J_{SO}[\exp(\frac{eV}{k_B T}) - 1]$, and is typically present only in compound semiconductors of group III - V;

- **region B**: it is called tunneling current of electrons, it is due to the tunneling of the carriers through the various layers of the heterostructure;

- **region C**: when the forward bias increases the diffusion current dominates $J_{diff} = A_{const} \exp(\frac{eV}{2k_B T})$;

- **region D**: when the current density becomes sufficiently high, there is a saturation of the current. This phenomenon is associated with the ohmic losses due to series resistance $I = \frac{\Delta V_D}{r_S}$, but it is still present even if the series resistance is negligible. In this case the concentration of minority carriers is similar to that of the majority ones, for which the current density is: $A_{const} \exp(\frac{eV}{2k_B T})$.

Diode reverse bias

Applying a significant reverse voltage at the junction, the reverse current follows a relationship given by the equation

$$I_R = A_{pn}(J_{s_0} + J_{NR} + A_{rsur}J_{RSUR})$$

This current can be considered almost constant to the saturation value J_{s_0}, even if it rises with the increase of the reverse voltage. This behavior is due to the high generation / recombination and surface phenomena.

4.2 Capacitance (C - f and C - V)

The measurement of the capacitance is a useful tool for understanding the mechanisms of recombination and distribution of the dopant in the device. This important information may be extracted thanks to two types of measurement, which will now be presented. The instrument used is a precision LCR meter, which is used to measure the impedance extracting magnitude and phase and then calculating the parameters using a model chosen by the user (any combination of capacitance or inductance with resistance or conductance, in our case capacity and conductance as shown in figure 4.2). The instrument can impose a selectable DC component and an AC component variable both in amplitude and frequency.

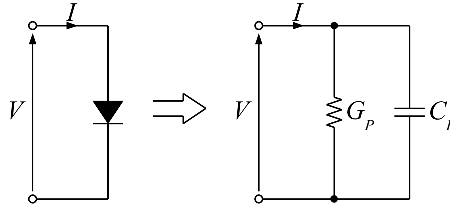


Figure 4.2: Equivalent model for the measurement of the capacitance

4.2.1 Capacitance - frequency

The measurement of the capacity as a function of frequency allow a study of the number and position of the deep levels inside the energy gap, and their possible variation during the lifetime of the device.

An explanation is given in the case of a $p^+ - n$ junction, in order to simplify the discussion, which is still extendable to the case of a generic junction. This junction has, when reverse - biased, a band diagram similar to the one shown in figure 4.3, where E_T is the energy level at which is located a generic acceptor deep level.

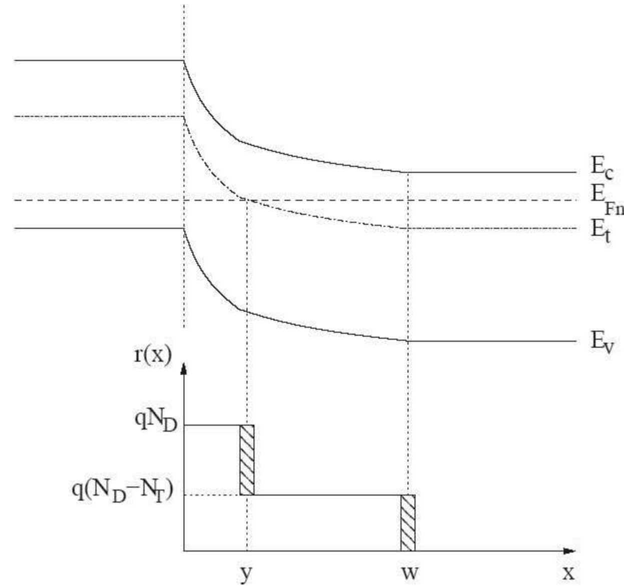


Figure 4.3: Band diagram and charge distribution of a reverse - biased p^+n junction

The dopant concentration at the side n is N_D. By studying the charge distribution in the junction it can be seen that in the range $x = [0 \div y]$ the charge density is equal to qN_D, the emission is dominant ($e_n^t \ll c_n n(y)$), and then the level is depleted of electrons. At $x = y$ the energy of the Fermi level and of the acceptor deep level overlap: the emission rate thus coincides with that of electron capture ($e_n^t = c_n n(y)$). But in the range $x = [y \div w]$ the phenomenon of capture prevails and the deep level is filled with electrons. The charge density thus has two components: on the left of y it is equal to qN_D, while on the right it is equal to $q(N_D - N_t)$. When it is applied a signal composed of a DC and an AC component, it can modulate both charges. The two charges, however, have a different behavior: at w the variations are considered to be instantaneous due to the high concentration of free electrons in the deep level, while the changes of the charge at y are limited by the rate of emission of the level. For frequencies lower than the emission rate of the trap level, the charge at both y and w is modulated and therefore the capacitance at low frequency is determined by the sum of both charges. However, since the emission and capture of electrons in the deep level is not instantaneous, at higher signal frequencies it is possible to have a condition of non-equilibrium: the free electrons can be trapped in the trap level or they can be injected into the conduction band with an increase of their energy. The

conductance increases due to the greater current flowing through the device. The value of the capacitance drops when a certain frequency is reached, as the trap level is no longer able to fill or empty of electrons quickly enough, then there is a reduction of the charge modulated in the junction. The capacitance then remains constant with the increase of the frequency, as none of the mechanisms described undergoes changes.

If there are multiple deep levels the value of capacitance has additional flexes. Therefore, studying the evolution of the capacitance as a function of frequency two regions ideally constants and a inflection point can be identified. Barbolla et al. [89] have studied this phenomenon and have observed that the peak of the G/f curve as a function of frequency is located at the point of bending of the $C - f$ measurement. Then, the frequency of the peak of G/f is the critical frequency of the trap level inside the bandgap.

4.2.2 Capacitance - Voltage

The measurement of capacitance as a function of voltage allows to identify the apparent doping profiles of the device, and then the modification of the charge distributions in the device over stress time.

When a diode is reverse biased, the space-charge region expands increasing the number of fixed ions in the lattice, forming a charge equal to:

$$Q = qN_D x_n = qN_A x_p$$

where N_D and N_A are the concentrations of donor and acceptor ions and x_n e x_p the depth of the space-charge region in the n and p side. Capacitance can then be calculated as

$$C = \frac{dQ}{dV_A} = qN_D \frac{dx_n}{dV_A} = qN_A \frac{dx_p}{dV_A}$$

Moreover, due to charge neutrality $x_p = (N_D/N_A)x_n$ and

$$x_d = x_n + x_p = \sqrt{\frac{2\epsilon}{q}(\frac{1}{N_A} + \frac{1}{N_D})(\phi_i - V_a)}$$

The junction capacitance for a small signal is given by

$$C = \left[\frac{q\epsilon}{2(\frac{1}{N_A} + \frac{1}{N_D})(\phi_i - V_a)} \right]^{1/2}$$

In the case in which the region p is doped more heavily than the region n ($N_A \gg N_D$), we have $x_p \ll x_n$, and then $x_d = x_n + x_p \approx x_n$. This is equivalent to saying that the depletion region extends almost entirely in the n region, so it is possible to estimate the doping profile of this region from the capacitance - voltage characteristic of the device. The doping profile under these assumptions is given by

$$N(x_n) = -\frac{2}{Aq\epsilon(\frac{d(\frac{1}{C^2})}{dV})}$$

where A is the area of the device. This is not the true doping profile but an apparent doping profile, since the approximation $N_A \gg N_D$ is not always verified, and then the space-charge region expands also in the p region. Consequently, the profile that we measure is originated from the composition of the two contributions.

4.3 Optical power - current relationship

This measurement allow us to obtain the relationship between the emitted optical power and the electrical power supplied, thereby resulting in an estimate of the overall efficiency of the device.

At equilibrium, the bimolecular rate equation in the presence of a density of current injected into the active region J can be written as

$$\frac{dn}{dt} = \frac{J}{qd} - (Bnp + AN_T n)$$

where d is the thickness of the active region, B the bimolecular recombination coefficient, A the coefficient of non-radiative recombination, N_T the density of defects and n and p the concentrations of electrons and holes in the active region. In high - injection condition, since $n \approx p \ll N_A, N_D$, this equation can be rewritten as

$$Bn^2 + AN_T n - \frac{J}{qd} = 0$$

This equation is different if the dominating mechanism is the radiative recombination ($AN_T n \ll Bn^2$) or the non-radiative recombination ($AN_T n \gg Bn^2$), obtaining

$$Bn^2 \approx \frac{J}{qd} \qquad \textit{and} \qquad AN_T n = \frac{J}{qd}$$

Since the light intensity is $L = Bn^2$, in the first case we have a dependency on the first power of the current, while in the second case, since $n \propto J$ implies $Bn^2 \propto J^2$, a second power dependence. This can be easily evaluated in a chart in log - log scale of the optical power as a function of the current: in fact a slope equal to one implies that we are in the first case, a slope equal to two in the second [90].

If there is the presence of an integrating sphere between the optical power meter and the device, the optical power (and with it the external quantum efficiency) measured is not absolute but relative, i. e. dependent on the response of the sphere: with different spheres different values would be obtained, but the relative trend of these values would be the same (a decrease of 10 % with a sphere corresponds to a decline of 10 % with another sphere). Considering efficiency, we must also remember that the value obtained is correct to within a multiplicative factor: formally, we should normalize the optical power with the energy of the emitted radiation quantum and divide the current for the electron charge to actually get a number of photons and a number of electrons.

Changes in the concentration of trap states can be evaluated thanks to the efficiency. The efficiency is given by the ratio between the radiative recombination rate and the total rate of recombination, i. e.

$$\eta \propto \frac{Bn^2}{An + Bn^2}$$

By inverting the relation, we obtain

$$\frac{1}{\eta} \propto \frac{An}{Bn^2} + 1 \qquad \text{e quindi} \qquad \frac{1}{\eta} - 1 \propto \frac{A}{Bn}$$

The ratio A/Bn is directly proportional to the concentration of trap states N_T, then from the measured efficiency, calculated as the ratio of the detected optical power and the electrical power supplied, it is possible to monitor the changes of this concentration, which in the literature has been reported to be proportional to $\sqrt{t}$.

4.4 Thermal characterization

The heating induced by the flow of current is a major cause of degradation of the devices. The high temperature reached during the operation causes a reduction of the efficiency of the devices, a variation of the spectral characteristics and a reduction of the expected lifetime, as many of the degradation mechanisms are thermally activated. In order to make a reliable estimate of the lifetime of a diode it is therefore necessary to be able to assess the temperature the junction reaches in standard operating conditions. This happens thanks to a relationship that describes the connection between the voltage drop across the device and its temperature, obtained by a characterization called *thermal maps*, and the estimate of the steady-state voltage of the device, thanks to the *transients* technique.

The relationship of the forward voltage of the diode V_f and the junction temperature T can be obtained using Shockley's equation, which relates the bias current to the temperature:

$$J_f = J_s \left[\exp\left(\frac{eV_f}{n_{ideal} kT} \right) - 1 \right] \tag{4.1}$$

where J_s is the saturation current density and n_{ideal} the diode ideality factor. The saturation current can be expressed as

$$J_s = e \left[\sqrt{\frac{D_n}{\tau_n}} \frac{n_i^2}{N_D} + \sqrt{\frac{D_p}{\tau_p}} \frac{n_i^2}{N_A} \right] \tag{4.2}$$

where D_n and D_p are the diffusion constants of electrons and holes and τ_n and τ_p are the lifetimes of the minority carriers. In this equation both the diffusion constants and the lifetimes are temperature dependent parameters. The diffusion constant decreases with temperature following a relationship like $T^{1/2}$. The average lifetime of the carriers may instead decrease (in the case of non-radiative recombination) or increase (in the case of the radiative recombination) with temperature. The concentration of free carriers can be considered independent on the temperature in the assumption that all the dopants are ionized.

The intrinsic carriers density n_i depends strongly on the temperature, following the relationship

$$n_i = \sqrt{N_C N_V} \exp\left(-\frac{E_g}{2kT}\right) \tag{4.3}$$

where N_C and N_V are respectively the effective densities of states at the edge of the conduction and valence band, and are equal to

$$N_C = 2\left(\frac{2\pi m_e kT}{h^2}\right)^{\frac{3}{2}} M_c \propto T^{\frac{3}{2}} \tag{4.4}$$

$$N_V = 2\left(\frac{2\pi m_h kT}{h^2}\right)^{\frac{3}{2}} M_c \propto T^{\frac{3}{2}} \tag{4.5}$$

where m_e and m_h are respectively the effective mass for electrons and holes, and M_c the number of minima of the conduction band.

From the equation 4.1, when to the diode is applied a forward bias $V_f \gg kT/e$, we have

$$J_f = J_s \exp\left(\frac{eV_f}{n_{ideal} kT}\right) \tag{4.6}$$

Isolating V_f, it is possible to evaluate the relationship between temperature and junction voltage as the derivative:

$$\frac{dV_f}{dT} = \frac{d}{dT}\left[\frac{n_{ideal} kT}{e} \ln\left(\frac{J_f}{J_s}\right)\right] \tag{4.7}$$

Substituting 4.2, 4.3, 4.4 and 4.5 in the equation 4.7 we obtain

$$\frac{dV_f}{dT} = \frac{eV_f - E_g}{eT} + \frac{1}{e}\frac{dE_g}{dT} - \frac{3k}{e} \tag{4.8}$$

This equation expresses the relationship between the junction temperature and the forward voltage across the diode. The equation is composed of the sum of three terms: the first term is due to the intrinsic carrier concentration, the second is instead originated from the temperature dependence of the energy gap, while the third term is derived from the parameters N_C and N_V, which are dependent on the temperature.

If the forward voltage imposed on the diode is similar to the built-in voltage, $V_f \approx V_{bi}$, and for a not degenerated dopant concentration, we can write

$$eV_f - E_g \approx kT \ln\left(\frac{N_D N_A}{n_i^2}\right) - kT \ln\left(\frac{N_C N_V}{n_i^2}\right) = kT \ln\left(\frac{N_D N_A}{N_C N_V}\right) \tag{4.9}$$

Moreover, the dependence of the energy gap on the temperature can be expressed using the Varshni law

$$E_g = E_0 - \frac{\alpha T^2}{\beta + T} \tag{4.10}$$

where α and β are the Varshni parameters. Substituting equation 4.9 and equation 4.10 in the equation 4.8 we obtain

$$\frac{dV_f}{dT} \approx kT \ln\left(\frac{N_D N_A}{N_C N_V}\right) - \frac{\alpha T(T + 2\beta)}{e(T + \beta)^2} - \frac{3k}{e} \tag{4.11}$$

The equation 4.11 is particularly useful to determine the relationship between the junction temperature and the forward voltage applied to the diode. Note that this expression represents a lower limit, since the junction voltage is always lower than the built-in voltage due to the non-zero resistivity of the neutral regions and of the contacts.

Now that we know the relationship between them, the voltage of the diode can be used to identify the junction temperature. This method consists of two measurements, a first calibration measurement (thermal map), and a measure that actually allows to trace the junction temperature (transient). In the calibration measurement, the device is brought to a known temperature using some external control (such as a thermal chamber or Peltier cell) and subsequently fed with a short current pulse, to avoid an excessive self-heating of the diode and then to be able to consider the junction temperature and that of the cell equal. The voltage across the diode is measured for different currents and for different temperatures, in order to establish a relationship between temperature and voltage. Experimental studies [91] show that the relation between V_f and T can be derived linearly or exponentially through the equations

$$V_f = A + BT_0 \qquad \text{o} \qquad V_f = A\exp(-\frac{T_0}{t_1}) + y_0$$

where T_0 is the temperature of the cell, while A, B and t_1 are the fit parameters. The same experiment is repeated at several current levels.

After the thermal map, the device is again brought to a known temperature, and a forward current is applied for a certain time in order to calculate the corresponding steady-state voltage across the device. The drop of the voltage follows an exponential law over time, so a steady-state value can be estimated more accurately thanks to another fit. Taking advantage of the calibration measurement, we can now calculate the junction temperature by

$$T_j = \frac{V_f - A}{B} \qquad \text{o} \qquad T_j = -t_1 \ln \frac{V_f - y_0}{A}$$

Now, knowing the values of T_j for different values of I, it is possible to plot the junction temperature as a function of the input electrical power. This relationship is approximately linear and the value of the slope of the line estimates the value of the thermal resistance of the device. The thermal resistance is defined as the increase in temperature caused by electrical power dissipation in the device

$$R_{th} = \frac{\Delta T}{P_{in}}$$

A similar process and several other techniques can be used also for the evaluation of the channel temperature of a HEMT. It is described in the relevant section at page 202.

4.5 Double pulse

The aim of the double pulse measure is to characterize the effect of the trapping on the characteristics of a transistor. Before the description of the technique, it is useful to recall the theoretical basis of the trapping and detrapping phenomena, which will be useful also for the comprehension of the subsequent section on drain current transients. We will consider a donor level, which has zero net charge when filled and is positive when ionized. At a given temperature, the total trap concentration is

$$N_T = N_T^+ + N_T^0$$

where N_T^+ is the concentration of empty (positive) traps and N_T^0 is the concentration of filled traps. Their variation over the time is given by

$$\frac{dN_T^0}{dt} = cN_T^+ - eN_T^0$$

where c and e are, respectively, the capture and emission rates. In a basic description the emission rate is not influenced by the bias point (this is not entirely correct, see for example the Poole-Frenkel effect at page 84), while the capture rate depends on the total concentration of free carriers, which is obviously related to the specific bias of the device. If we assume that all the traps are empty before the test, during the filling N_T^0 varies following the relationship

$$N_T^0(t) = \frac{c}{e+c} N_T[1 - exp(-(e+c)t_f)]$$

If the capture rate is high and the filling time t_f is long enough, it is possible to fill all the traps. If the capture is significantly faster than the emission, the initial condition right before the beginning of the detrapping phase is

$$N_T^0(t) = N_T[1 - exp(-ct_f)]$$

The concentration of empty traps during the detrapping is then given by the equation

$$N_T^0(t) = N_T[1 - exp(-ct_f)][exp(-et)]$$

The emission rate depends strongly on the temperature, following the relationship

$$e(T) = \gamma T^2 \sigma exp\left(\frac{E_a}{k_B T}\right)$$

where E_a is the *activation energy* and σ the *capture cross-section*, while γ groups several different constants and parameters:

$$\gamma = 2\sqrt{3} M_c (2\pi)^{3/2} k^2 m^* h^{-3}$$

The variation of $ln(\tau T^2)$ (where $\tau = 1/e$ is the *time constant* of the process) as a function of $1/T$ follows a linear dependence. These data are used to create the *Arrhenius plot*, the slope of the linear fit is the activation energy and from the intercept the capture cross-section can be evaluated.

The double pulse system is composed by two synchronized pulsers that fix the bias point of the device and by an oscilloscope that evaluates the current as the voltage drop over a known 50 Ω resistance. Using different gate and drain values, the transistor is submitted to a sweep of the drain voltage. At each point, the device is initially kept at a quiescent bias point in order to induce the trapping of the carriers, and then to a quick measure pulse used to check the response of the current. The width of this pulse is 1 μs and the duty cycle 1%, but different values can be chosen if necessity arises. The limited pulse ensures that the effects of the self-heating are prevented. An adequate choice of the quiescent bias points allows for the excitation of trapping in different regions of the device, while the choice of the sweep values leads to the ID - VD or ID - VG curves in the desired conditions. By means of the comparison of these curves at various quiescent bias points, it is possible to obtain information on the dynamic response of the device. The schematic pulse configuration and an example of the current response is given in figure 4.4 [92].

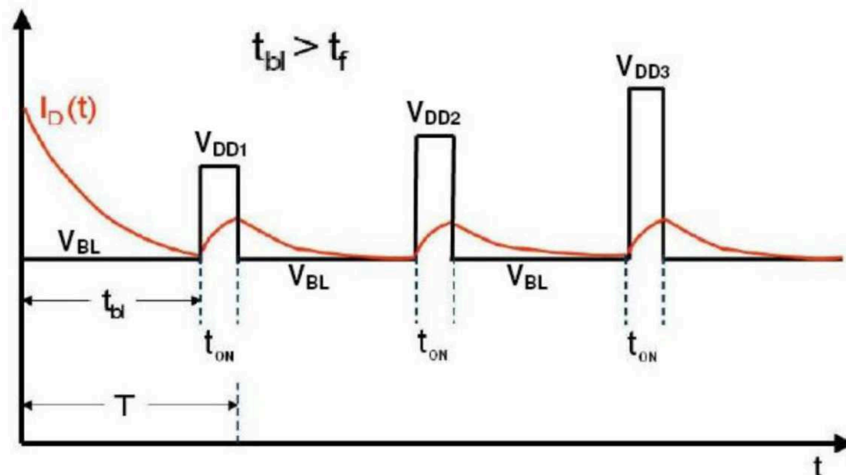


Figure 4.4: Pulse configuration and current response of the double pulse system.

It is useful to point out that at the gate terminal is placed a 50 Ω pass-through matching resistance, in order to avoid large oscillations and/or a slow response of the

gate voltage, and that the relative width of the gate and drain has to be accurately considered in order to avoid the simultaneous presence of a on-state gate voltage and of a high quiescent bias point drain voltage, which can destroy the device due to the excessive power dissipated.

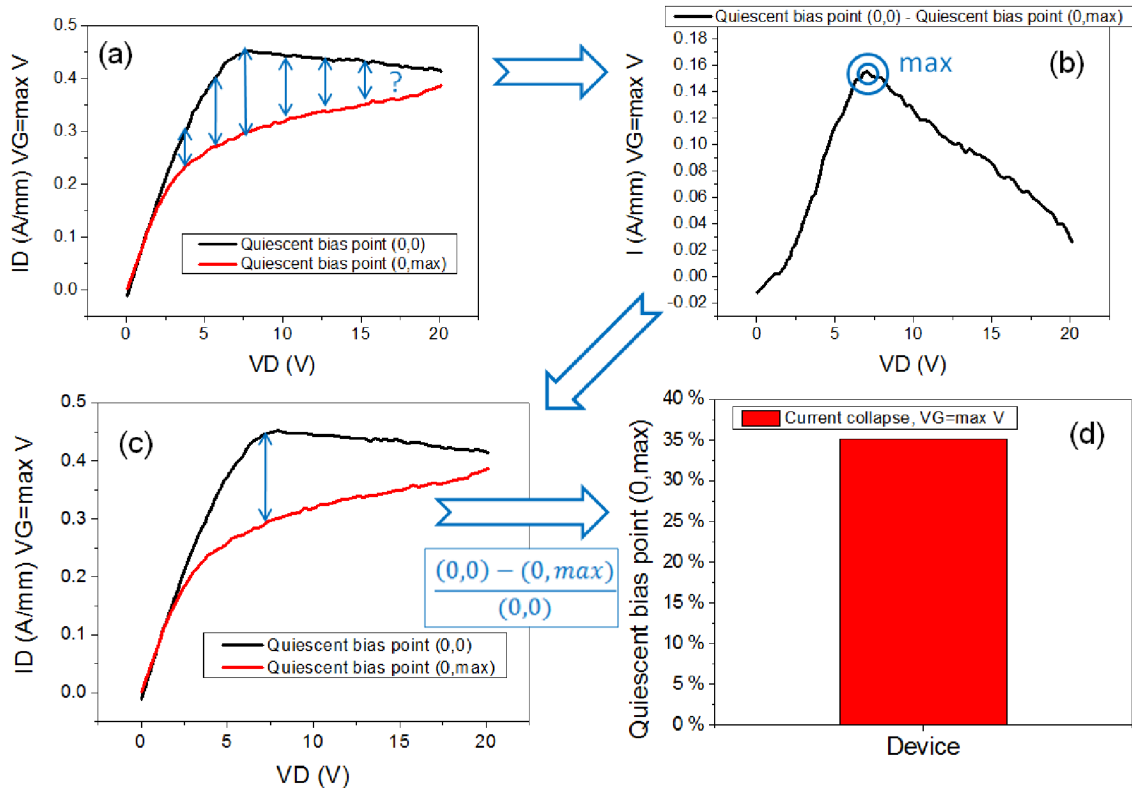


Figure 4.5: Definition and procedure for the calculation of the current collapse.

The comparison can be made easier defining the *current collapse*, the complete procedure is described in figure 4.5. If we consider, at the maximum measure gate voltage, the difference between the untrapped device and the curve obtained at the maximum quiescent bias point, it is not easy to define a comparison (a). The current collapse is typically defined as the percentage difference between the two curves at a given VD, but in this thesis it is used the *maximum* value of the current collapse, in order to analyze the most critical point of the characteristic. Once the maximum difference between the two curves and its corresponding VD has been identified (b), it is possible to check the curves for their current level at that drain value VD_{max} (c) and to calculate the current collapse percentage as

$$\frac{\mathrm{ID}(\mathrm{VD}_{max})|_{QBP=(0,0)} - \mathrm{ID}(\mathrm{VD}_{max})|_{QBP=(0,max)}}{\mathrm{ID}(\mathrm{VD}_{max})|_{QBP=(0,0)}}$$

This value can be used in graphs to compare different devices, measure conditions and stress steps (d).

4.6 Drain current transients

The drain current setup is composed by two pulsers that are able to concurrently set the gate and the drain voltage. The current flowing through the device is obtained reading with an oscilloscope the voltage signal at the output of a current probe, and a 100 Ω resistance is used in order to limit the high current output in case of the failure of the device. The pulsers are used to fill the traps during the quiescent bias phase, and to set the bias point during the subsequent measure phase. This way, it is possible to obtain the transient response to the filling in a wide time range (typically 1 μs - 100 s or more) with a good resolution, given by the chosen oscilloscope time base (up to the nanoseconds). The repetition of the measure with the same parameters at different temperatures allow for the extraction of the time constants as a function of the thermal energy, which can be used in an Arrhenius plot to evaluate the activation energy of the deep level and its capture cross-section. A drain current transient is typically faster than other techniques used for the activation energy estimation, such as current deep level transient spectroscopy (I-DLTS [93]), since it requires only a few temperatures to obtain the needed data, instead of a full sweep.

4.6.1 Bias points

The correct choice of the various bias point is crucial in this technique, since it allows to probe different areas of the device and to analyze the effect of the trapping in different operating conditions of the transistor. The matrix of the values to be fixed is composed by four element: the filling voltage and the measure voltage must be identified for both the gate and the drain terminal. As usual for the characterization of a transistor, the source is grounded. The quiescent bias point has to be chosen accurately in order to induce the desired trapping. It may be a high gate voltage and moderate drain voltage, if we want to analyze the on-state trapping (which

can be done also using a neutral filling bias and the adequate values during the measure phase), or a high drain voltage (up to hundreds of volts) at lower gate voltages to investigate the off-state trapping. Moreover, a critical approach requires the determination not only of the voltages during the filling phase, but also of the difference between them and the measure bias points. If there is only a large difference in the gate voltage it is possible to detect effects that happen in the region under the gate, while if the drain voltages have a large excursion and the gate bias only a small variation the trapping is caused mainly in the gate - drain access region. In addition to this reason, the measure voltage should be chosen to analyze the effect of the imposed trapping on different operating regions of the transistor, mainly the linear and saturation regimes.

4.6.2 Extrapolation of the time constants

Once the current transient in the desired conditions has been obtained, it is necessary to extrapolate correctly the time constants of the various processes. In the literature can be found some different methods:

- The multi-exponential fit tries to find a correspondence between the transient and the sum of some static exponential defined by the user [94]. This method has the lowest accuracy and causes artifacts, missing values and other problems, so it shouldn't be used for a rigorous analysis.

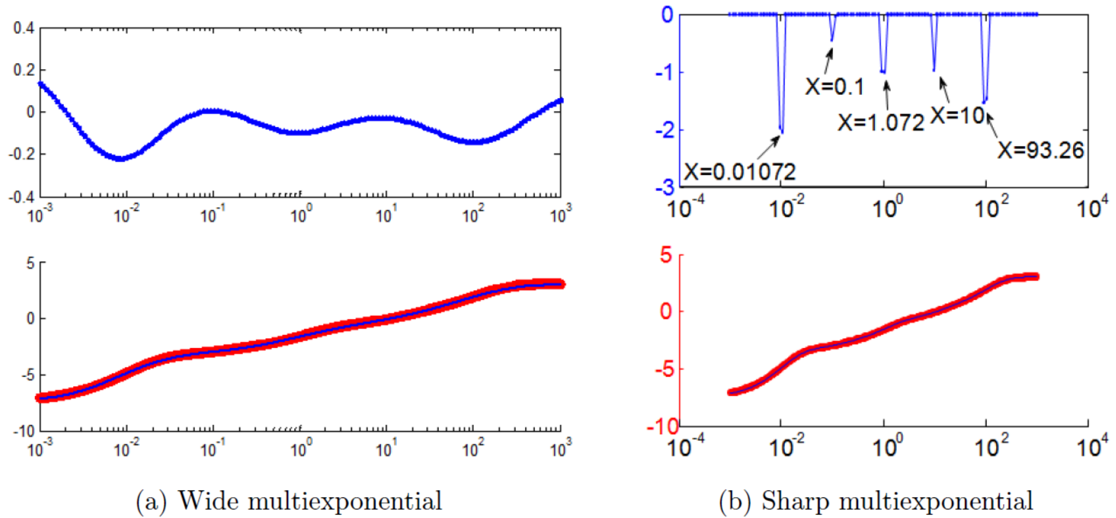
- The sharp multi-exponential fit employs an improved algorithm capable of finding the best match of the experimental data to a large sum of user-generated exponentials with fixed time constant. This fitting model gives the best precision and is apt to distinguish slight spectral differences (under the decade), but gives birth to artifacts when the transient behavior differs from the ideal sum of exponentials.

- The stretched exponential fit [95] permits to overcome this limitation by the use of a fixed number of unconstrained exponentials with a correction factor that takes into account the non-ideality, but causes a slight imprecision in the determination of the time constant and of the number of phenomena.

- The derivative of the current transient [96] is the easiest algorithm to implement and gives a good precision in the analysis of both ideal and stretched exponentials, but is not able to distinguish between two processes with similar time constants.

Each of this methods has its advantages and disadvantages. No one of them is able to give a good result in every case, so the choice should be made taking into account the actual shape of the transient under analysis. Figure 4.6 compares the results of the two different multiexponential algorithms on a test computer-generated transient: only the sharp one is able to correctly detect the time constants, while the more common analysis has not enough resolution and precision. Figure 4.7 reports the results of the algorithms on a experimental transient, highlighting the already discussed behavior.

$$y = 3 - 4e^{-t/0.01} - 0.5e^{-t/0.1} - 2e^{-t/1} - e^{-t/10} - 3e^{-t/100}$$



(a) Wide multiexponential (b) Sharp multiexponential

Figure 4.6: Comparison of the two multiexponential fit types.

4.6.3 Filling time dependence

The duration of the filling phase, called the *filling time*, can be used to obtain additional information on the physical structure of the defective state. While point defects can be filled in a very fast manner, extended defects (such as dislocations)

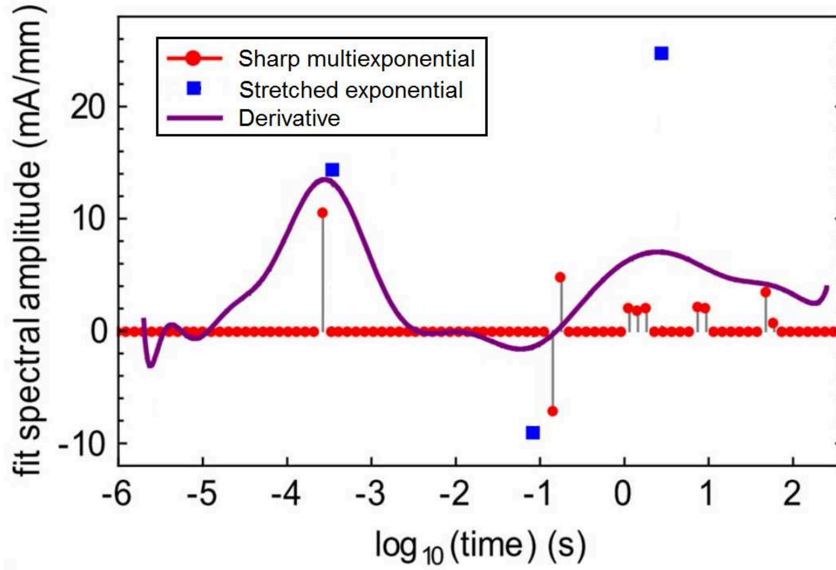


Figure 4.7: Comparison of the main fits for time constant extraction.

require a longer time to be completely filled. This is due to the build up of an electric field, created by the already trapped charge, that opposes the capture of other carriers inside the defect. The carrier capture has been found to depend logarithmically on the width of the filling pulse [97], following the equation

$$n_T(t_p) = \sigma_n \langle v_n \rangle n \tau N_T ln \left[1 + \left(\frac{t_p}{\tau} \right) \right]$$

where c_n is the capture probability, N_T the concentration of the defect and τ the capture time constant, which can be expressed, defining Φ_0 the time-dependent potential barrier for carrier trapping, as

$$\tau = \left(\frac{k_B T}{q \Phi_0} \right) \left(\frac{n_{T0}}{N_T} \right) \left(\frac{1}{\sigma_n \langle v_n \rangle n} \right)$$

Carrying out different transients at different filling times, it is possible to identify if a current variation is due to a point defect or to an extended defect: if the signal associated to a given time constant increases with the filling time there is the build-up of the charge inside an extended defective region, while if the signal is already at his maximum for a reduced filling duration there is the presence of a quickly-fillable point defect.

4.6.4 Arrhenius database

As a part of the research on the drain current transient, a database was collected from more than 60 published papers of deep levels and their corresponding signatures, which can be useful for the identification of the physical origin of the trap and its location. The database includes more than 370 deep levels, whose signatures are reported in figure 4.8.

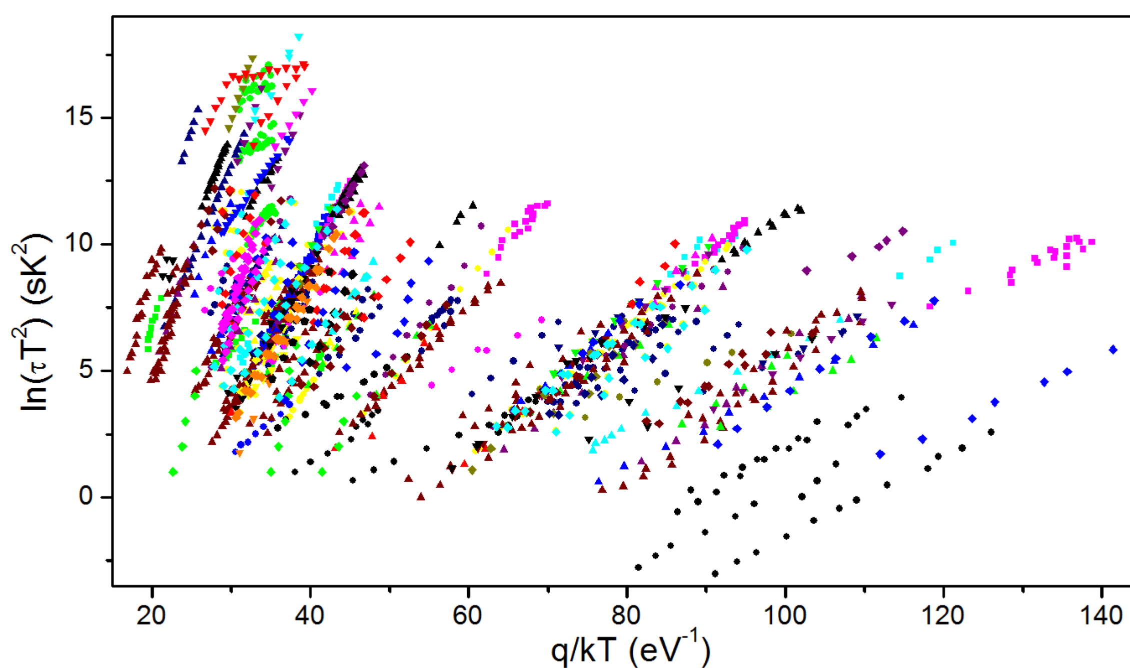


Figure 4.8: Signatures of the deep levels collected in the Arrhenius database.

Chapter 5

Optoelectronic devices

Part of this work was supported by the PRIN project "Dispositivi optoelettronici su nitruro di gallio per applicazioni avanzate: solid-state lighting, strumentazione biomedicale e data storage", coordinated by prof. Zanoni.

5.1 Radiation tests

Light emitting diodes are expected to find wide application in the lighting and automotive fields. Furthermore, these devices have demonstrated high efficiency and reliability, when used for the realization of displays, lamps and sterilization devices. In order to achieve a wide market penetration, it is important to optimize the reliability of InGaN-based LEDs, by understanding the physical mechanisms that limit the robustness of these devices.

Concerning space applications, it is necessary to analyze how the devices interact with the extreme ambient conditions typical of a space mission or a satellite environment. One of the most stringent requirements is the ability to withstand the flux of highly energetic particles, such as protons, without excessive damage. The effect of various proton fluences on GaAs LEDs and transistors has been widely investigated in the past [98, 99, 100]. However, over the last few years, GaN has emerged as a reference material for the realization of both visible and UV LEDs, and high power/high efficiency transistors. Gallium nitride has an intrinsically high robustness to electric fields and to high temperatures. However, before this material can be effectively adopted in space applications, it is important to study its robustness against harsh irradiation conditions. For this reason, within this section we present an extensive

analysis of the effects of proton irradiation on the electrical and optical properties of GaN-based LEDs.

It is useful to point out that, at the moment, there isn't a pushing request for lighting applications in space, leaving aside the intra-satellite communication that is typically well-handled by common GaAs infrared devices. Anyway, studying light emitting diodes can be useful to understand how the Gallium Nitride, as a material, behaves when used in space conditions. LEDs have a simpler structure than HEMTs and have a more mature technology and fabrication, so they are less prone to problems that can be due to a non-perfect growth and not to the material itself. Moreover, LEDs are better candidates than common p-n or Schottky diodes, since their higher output optical power and well-defined emission spectrum provides additional characteristics that can be monitored in order to understand the modifications induced by proton irradiation inside the material.

It is well known that when radiation interacts with a semiconductor, the collision between the highly energetic protons and the atoms could cause a permanent or reversible displacement from the original position in the crystal lattice. In LEDs, this atomic-level damage usually induces changes of the electrical and optical characteristics of the devices, due to the generation of defects that may act as non-radiative recombination centers. These modifications can be evaluated by means of current-voltage measurements (I - V), capacitance-voltage analysis (C - V) and optical power vs injected current (L - I) characterization.

The devices under test are commercially-available InGaN-based blue light emitting diodes, grown by two different manufacturers. In the following, we will refer to them as type A and type B. The type A devices have a sapphire substrate, a 460.32 nm average peak wavelength, a nominal 268 mW average optical power and a typical forward bias of 3.35 V. The type B samples have a silicon carbide substrate, a 462.4 nm average peak wavelength, a nominal 14.83 mW average optical power and a typical forward bias of 3.75 V. The LEDs are unpackaged, in order to avoid the absorption of the protons by the protective epoxy. The LEDs were placed on a Aluminum plate by means of a conductive silver epoxy glue. The I-V characterization was carried out by means of an Agilent E5263A semiconductor parameter analyzer. The maximum

reverse voltage was chosen to be -12 V, a value that gives a current high enough to be detected with precision but is not dangerous for this kind of technology. The maximum forward voltage was limited by the value of the maximum safe forward current provided by the manufacturers. The C-V data were measured by a HP 4284A precision LCR meter, that allows us to perform precise measurement of the modulus and the phase of the impedance, returning the value of inductance, capacitance and resistance following a selected model. In our case, the model that fits best the behavior of a LED is the parallel of capacitance and conductance. The evaluation of these parameters was carried out at two different small signal frequencies, 10 kHz and 1 MHz, in a voltage range equal to the one used to obtain the current-voltage relation. The relationship between the output optical power and the applied forward current has been evaluated biasing the device with a Keithley 2612 source-meter and collecting the spatially resolved emission with a cooled CCD camera Andor LUCA. The samples were irradiated at the INFN LNL center, using the 7 MeV CN Van de Graaf electrostatic accelerator. Were used 3 MeV protons and three different fluences: 10^{11} p^+/cm^2, 10^{13} p^+/cm^2 and 10^{14} p^+/cm^2.

5.1.1 Radiation effects

Diode characteristics

In figure 5.1 (a) are reported the current-voltage characteristics measured in the forward-bias region on a set of analyzed samples, irradiated with different fluences. As can be noticed the experimental data indicate that irradiation induced a shift of the I - V curves towards lower voltages: this effect was found to be stronger at the higher fluences. Results suggest that irradiation induced an increase in the concentration of defects within the active layer of the devices, with subsequent variation in the conductivity of the junction [101, 102]. After irradiation were detected also slight modifications in the reverse-current components: figure 5.1 (b) reports the difference between the reverse current (measured at -12 V) before and after irradiation at different fluence levels. As can be noticed, the reverse current exhibits a decrease, which is well correlated to the irradiation level. As reported in the papers cited above, this effect may be related to a change in the concentration of the carriers within the active

region, and/or to a variation in the mobility of the carriers.

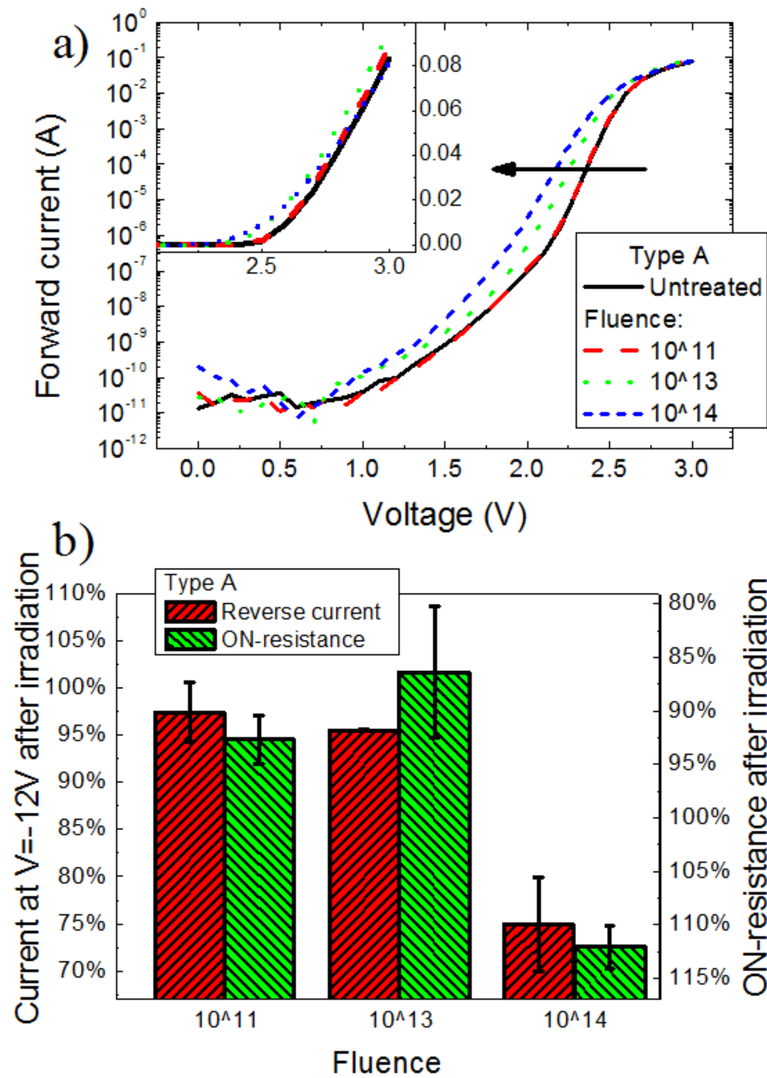


Figure 5.1: (a) Forward current of type A LEDs before and after 3 MeV proton irradiation at various fluences. (b) Decrease in the reverse current at V=-12V and increase of the series resistance in the type A samples after 3 MeV proton irradiation at different fluences.

A possible explanation of the behavior of the diode current as a whole could be the creation of defect-related energetic levels into the material bandgap. When the device is forward biased below the turn-on voltage, these new levels may enhance current conduction, possibly due to an increase in the generation/recombination or tunneling components. On the other hand, when the device is reverse biased the reduction of the current can be caused by a drop in the mobility of the material [101, 103]. When

the device is biased at a value higher than the turn-on voltage, where its behavior is dominated by resistive contributions, a slight increase of the series resistance has been found, shown in the inset of figure 5.1 (a), directly proportional to fluence, as found by other groups [104]. This drop of forward current is supposed to have the same origin as the decrease in reverse-current, i. e. a variation of the mobility of the material.

Optical power

The presence of defects already identified by I - V characterization has a deep impact on the output optical power. The increase in the non radiative recombination promoted by these centers causes a strong drop of the emission in the whole analyzed current range. Given a density of electrons injection, a growth of the ratio between non radiative and radiative recombinations means that less electron-hole pairs are able to produce light because most of the input power is lost via thermal dissipation. Figure 5.2 shows the change of the LED intensity at various injection currents and fluences. Even if a fluence of 10^{11} p^+/cm^2 is not high enough to create an appreciable decrease, more intense proton doses are able to cause the expected reduction. This result is consistent with the one reported in [105]: LEDs with a similar production technology and proton irradiation energy exhibit almost no lowering of their output up to 10^{12} p^+/cm^2, a value that seems to behave as a threshold causing a sudden and sharp degradation at higher fluences.

Moreover, spatially resolved measurements of the emission were carried out, in order to gain more information on the distribution of the damage. As can be seen in the false - colors figure 5.3 (intensity not in scale), the emission patterns do not show the formation of emissive clusters or dark holes: the damage is well diffused on the whole area: this result suggests that irradiation induces the generation of point defects, rather than of extended structural defects.

Capacitance variation

From the electrical and optical measurements we have identified the creation of deep levels that act as non-radiative recombination centers. In order to gain further insight on the variation of the performances of the irradiated samples, an analysis

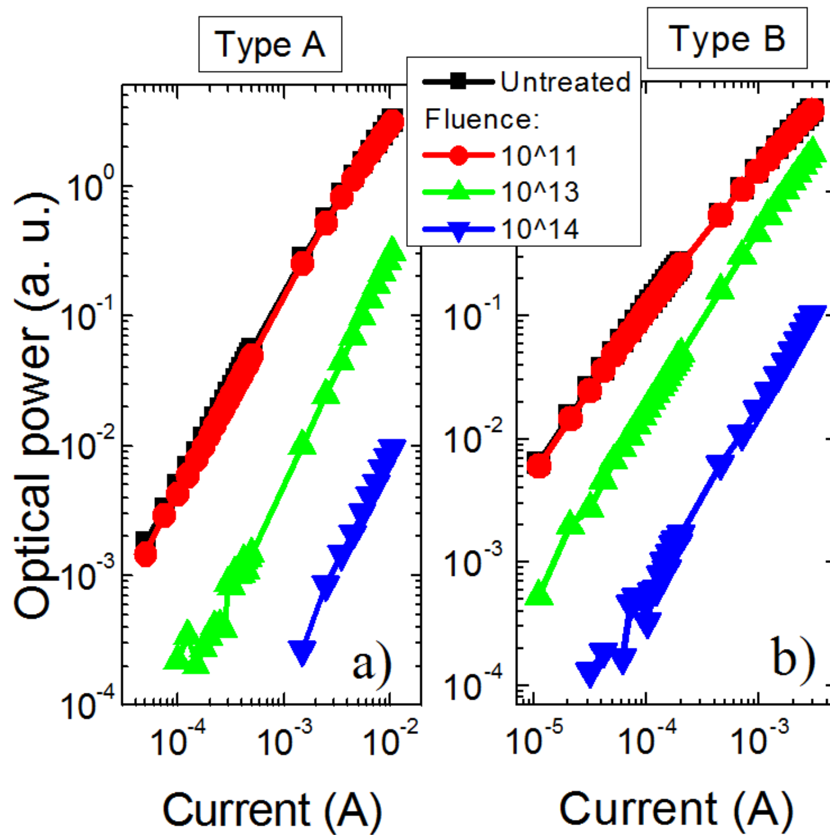


Figure 5.2: Output optical power as a function of injected current and 3 MeV proton fluence.

of the variation of the capacitance - voltage characteristics has been performed (see figure 5.4). As can be noticed, there is a drop of the capacitance value, directly proportional to the fluence. Since the capacitance is strongly determined by the amount of free charge present on the device, its variation is a strong indication of a change in the distribution of charge within device structure. The deviation from the untreated curve is more prominent at voltages near 1.5 V, where the conduction of the LED begins to increase (see figure 5.1). This is evidence that the creation of defects occurs close or into the active region, where it has the greatest impact on the electrical and optical behavior.

To further validate this hypothesis, the change in the diode ideality factor has been evaluated, which is strongly related to the presence of defect-related (or tunneling) current components. Its value increases at higher fluences, in accordance with the C-V data. Figure 5.5 show the relationship between the ideality factor and an estimate

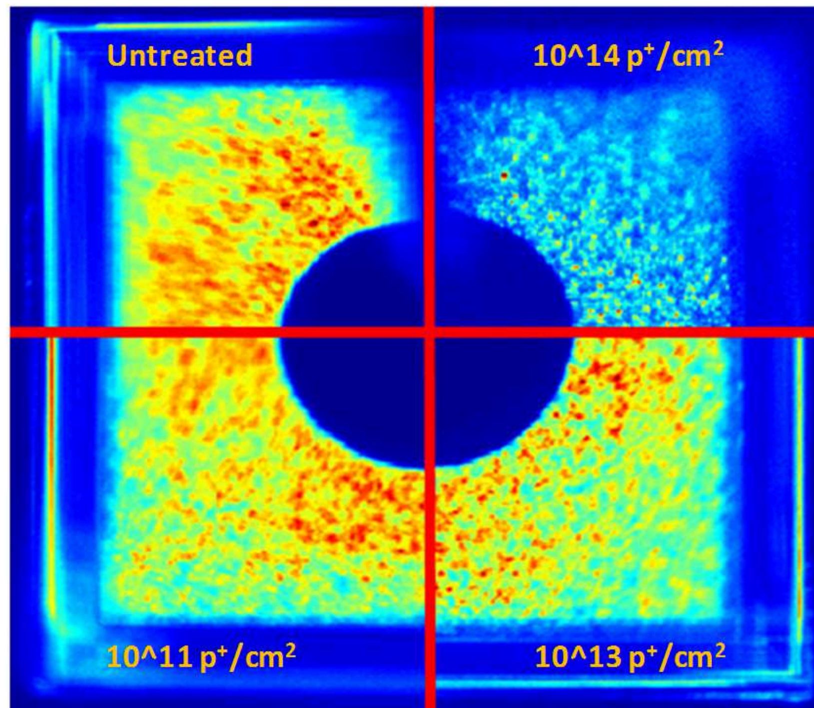


Figure 5.3: Electroluminescence map for type B LEDs (intensity not in scale). Bias current 3 mA.

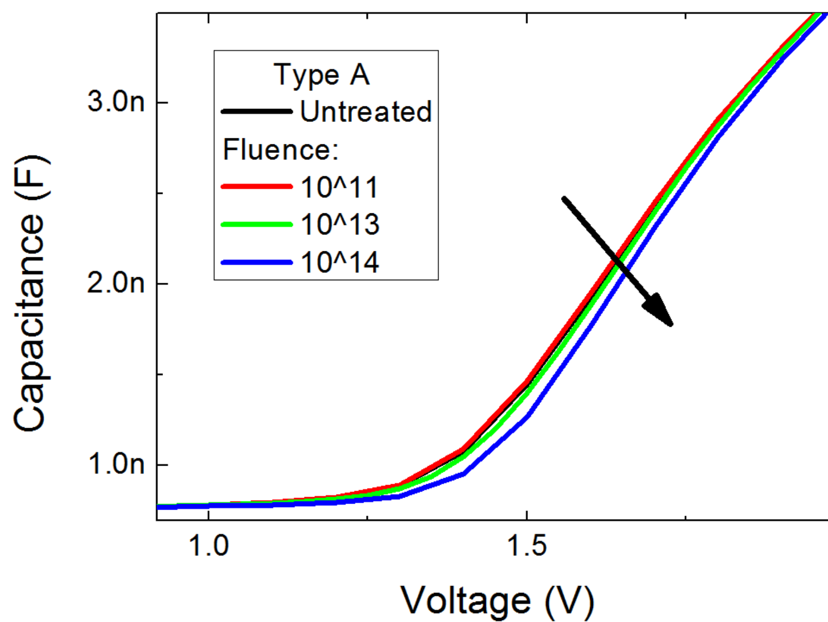


Figure 5.4: Variation of the bias-dependent capacitance before and after irradiation with various 3 MeV proton fluences for type A samples.

of the total junction charge, for both type A and type B devices, as a function of the residual optical power after the irradiation. The charge estimation was obtained integrating the capacitance at 10 kHz between -6 V and 2 V. In order to correlate the variation of the electrical characteristics with the optical ones, which are the quantities that are of interest the most for light emitting devices, a spectral analysis of the output radiation was carried out. There is an increase of the yellow - green parasitic emission band, which is commonly related to the presence of a energy level inside the bandgap. This defect-related allowed state creates another possible radiative recombination path with a lower transition energy, and gives birth to unwanted conversion of the injected electrical power to a parasitic spectral component. The yellow-green emission covers a wide range of wavelengths (500 - 650 nm) due to the non-homogeneous position of the defect level relative to the valence and conduction band edges, so we reported in figure 5.5 the increase of its peak value [106]. The good correlation between the three quantities suggests that the variation in the free-charge profile as a consequence of the creation of defects is responsible for the modification of the LED performance, and that the active region is the affected part of the diode that has the greatest impact on the overall functionality of the device after the irradiation test.

5.1.2 Recovery tests

The creation of defects should be recoverable by means of thermal annealing. The irradiated devices were submitted to recovery tests, carried out at 150 ℃ and no applied bias. At every step the electrical and optical characteristics were measured, in order to obtain the recovery kinetic. The results are summarized in figure 5.6, which reports the good correlation between the changes of three quantities related to the number of defects. It is shown that:

- the forward current above the turn-on voltage of the diode increases, due to the restoration of the mobility which dropped as a consequence of the irradiation (figure 5.1 (b));
- the reduction of the concentration of defects is highlighted also by the improvement of the output optical power at a fixed current value, since a lower number

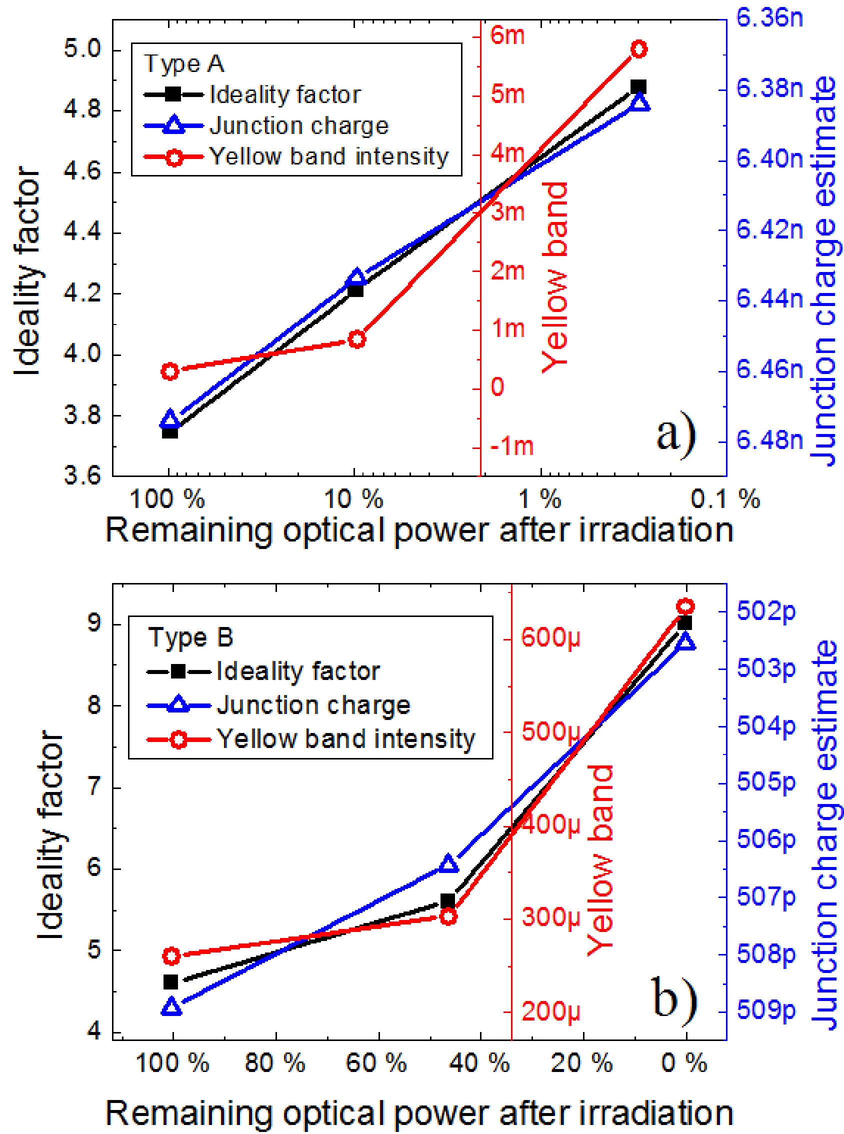


Figure 5.5: Correlation between diode ideality factor, 10 kHz capacitance integrated between -6 V and 2 V (proportional to the junction charge) and parasitic yellow-green emission, as a function of the variation of the optical power.

of defects gives less non-radiative recombination centers, and a more favorable ratio between light generation and non-emissive losses;

- there is a decrease of the current below the turn-on voltage, possibly due to lower generation/recombination (or tunneling) components, that are enhanced by a greater number of defects inside the device.

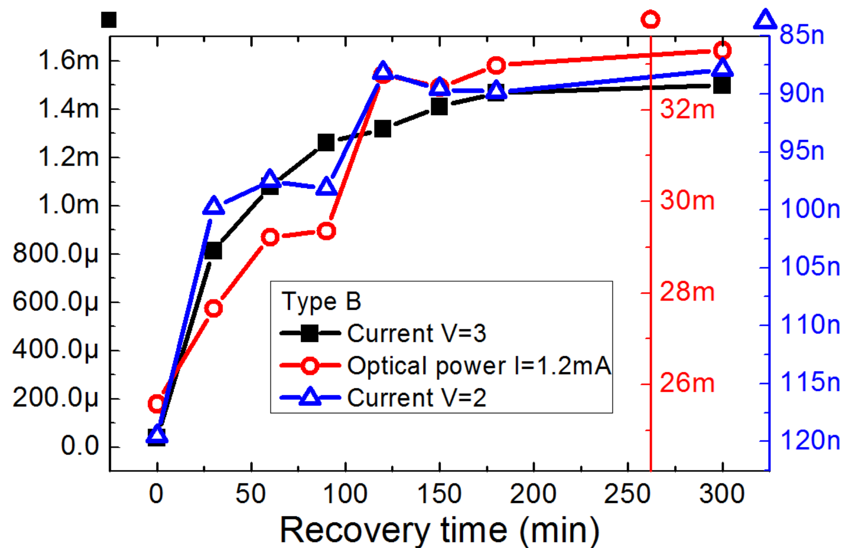


Figure 5.6: Recovery kinetics for Type B devices. Recovery carried out at 150 °C and no applied bias.

5.1.3 Conclusions

This part reports on the degradation of two different series of commercially-available InGaN LEDs submitted to proton irradiation at 3 MeV. The degradation process was characterized by combined current-voltage (I - V), optical power-current (L - I) and capacitance-voltage (C - V) measurements, carried out before and after irradiation at 10^{11}, 10^{12} and 10^{13} p/cm^2. It was found that exposure to higher fluences can cause:

- an increase in the forward current of the devices, in the series resistance and in the ideality factor, and a slight decrease of the reverse current;

- a strong drop of the optical power, evenly distributed over the whole surface;

- a good correlation between the diode ideality factor, the junction charge estimated by means of capacitance - voltage measurements and the parasitic yellow-green band intensity.

Those results are evidence for

- the creation of non-radiative recombination centers localized in the active region;
- a possible variation of electrical mobility.

The results are further validated by recovery tests, which show

- a gradual restoration of the electrical and optical performances of the devices.

5.2 LED-like structures

In this section are analyzed the physical mechanisms causing the degradation of InGaN-based Blu-ray laser diodes (LD) and LED structures (with the same epitaxial structure of laser diodes). The study was carried out on InGaN-based devices with a Multi Quantum Well (MQW) structure, emitting at 405 nm. A split-wafer experiment was designed as described in the following: part of the wafer was processed in order to obtain LDs, with cavity width and length equal to 1.5 μm and 600μm respectively. The remaining part of the wafer was processed in order to obtain LED samples (referred to as LED-like in the following) with the same epitaxial structure of the LDs, and an area of 75×200 cm^2. Devices were submitted to constant current stress at 4 kA/cm^2, with a case temperature equal to 75 ℃.

5.2.1 Optical measurements

During stress, the optical power of LED-like devices showed a remarkable decrease, more prominent at lower measuring current levels (figure 5.7). This kinetic indicates an increase in defect density within the active layer, that reduces the radiative recombination rate and consequently the luminescence. Stress was found to induce also an increase in the threshold current (I_{th}), following the square root of stress time, as reported in previous papers [107]. The slope efficiency showed only a slight decrease,

possibly related to an increase in mirror or internal losses, that cannot explain the observed threshold current increase. From the optical power measurement we have calculated the A/Bn ratio (related to the non-radiative recombination rate A) as follows:

$$\frac{1}{\eta} = \frac{1}{P_{out}} = \frac{A + Bn}{Bn} = \frac{A}{Bn} + 1$$

where η represents the external efficiency, P_{out} is the emitted optical power, A and B are the non-radiative and radiative recombination coefficients respectively. Figure 5.8 reports the temporal variations of these values, highlighting a strict correlation between I_{th} and A/Bn.

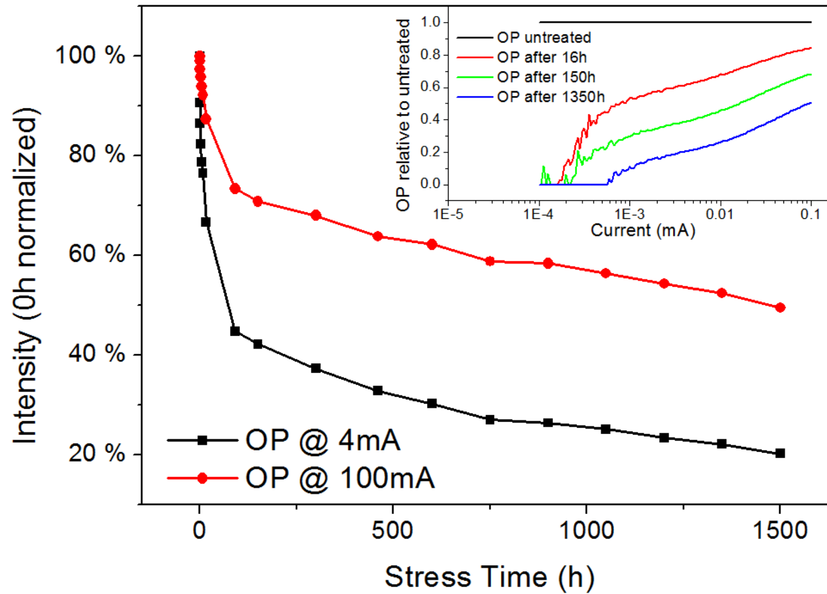


Figure 5.7: LED-like optical power measured at 25 ℃ during stress at 4 kA/cm^2 ,75 ℃ of a LED-like sample. Inset: normalized L-I characteristics measured during stress time on the same device.

5.2.2 Electrical measurements

The current - voltage curves of the LED-like samples for increasing stress times have been measured. Figure 5.9 indicates that stress induces an increase in the defect-related current components, which is well correlated with the optical power decrease, thus suggesting that stress induces an increase in the concentration of defects within the active region [108].

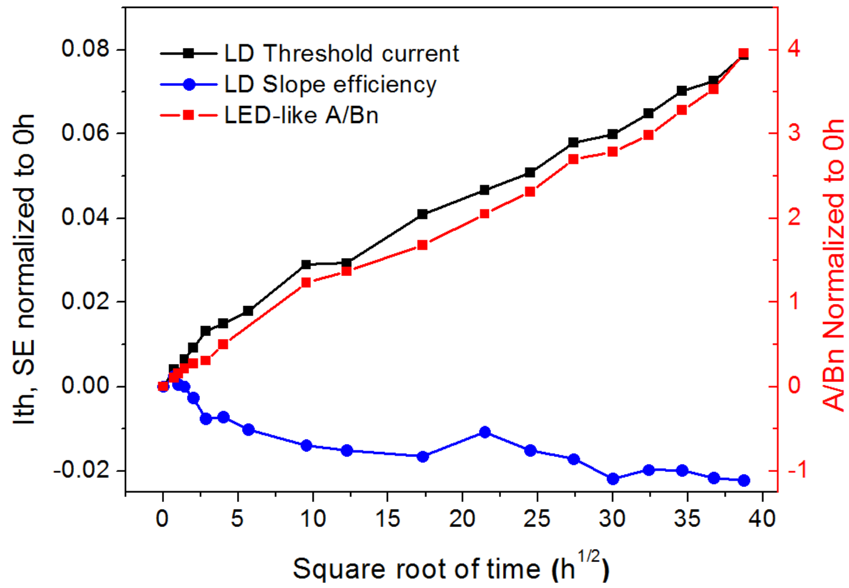


Figure 5.8: Degradation of the optical parameters of one of the analyzed LDs, submitted to stress at 25 °C, 4 kA/cm^2. Correlation with LED-like A/Bn parameter is also reported.

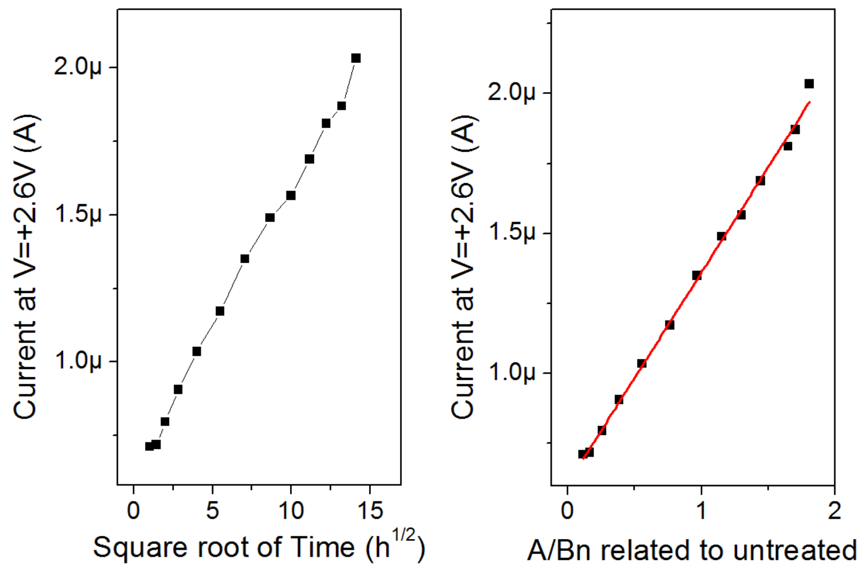


Figure 5.9: Defect-related current increase and correlation with A/Bn for LED-like structures stressed at 4 kA/cm^2, 75 °C.

5.2.3 Emission measurements

One of the mechanisms responsible for the decay of the optical performances is the current spreading from the active region to the outer parts of the device, causing a worsening of the optical confinement. From Figure 5.10 we can infer that no additional spreading becomes visible after stress, while the reduction in spot size is due to the decrease in optical power. This image was taken in near-field imaging, and is presented in logarithmic false-colors scale. In order to analyze defect-assisted recombination, were performed spectral measurements to obtain data on the typical yellow luminescence (YL) caused by Nitrogen vacancies in the crystal lattice. Figure 5.11 displays the results. The first ageing effect we can notice is the decrement in both the violet and yellow luminescence, and a smaller reduction in the YL (as shown by the inset). Moreover, during stress time no further parasitic emission band was generated. This result confirms that degradation is due to non-radiative effects, rather than to the generation of radiative/parasitic emission peaks.

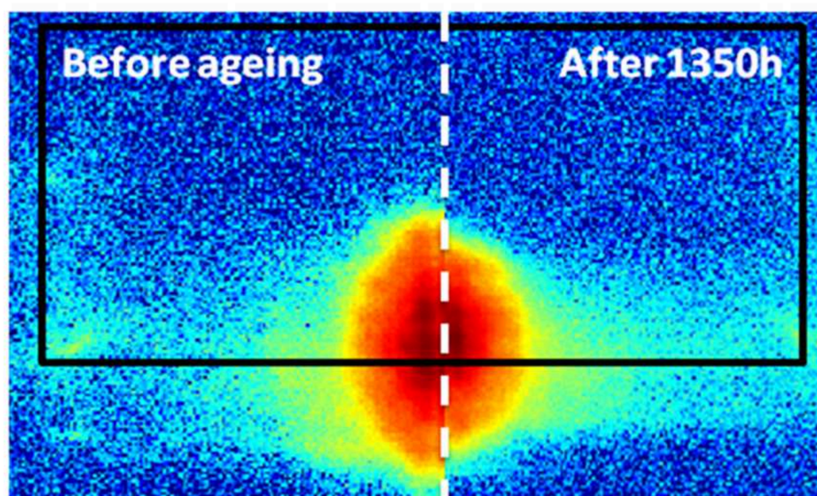


Figure 5.10: Near field emission microscopy map of one of the analyzed laser diodes, measured at 1 mA.

5.2.4 Characteristic temperature

The characteristic temperature (T_0) of the LD was analyzed with the aim of understanding the degradation mechanisms occurring in LDs (see [109]), thanks to

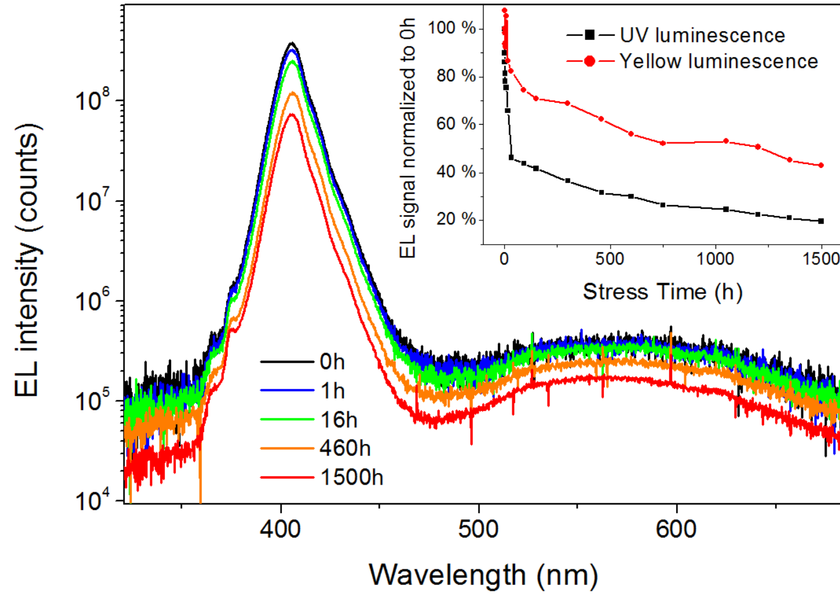


Figure 5.11: EL spectra at 25 ℃ (bias current = 4 mA) and kinetics of LED-like samples after stress at 4 kA/cm^2, 75 ℃.

the relationship with various parameters

$$\frac{1}{T_0} = \frac{1}{T_{tr}} + \frac{1}{T_{\eta_i}} + \frac{\alpha_i + \alpha_m}{\Gamma_{g0}} \frac{1}{T_{g0}} + \frac{\alpha_i}{\alpha_i + \alpha_m} \frac{1}{T_{\alpha_i}}$$

T_0 can be extrapolated from the formula $I_{th} = I_0 e^{T/T_0}$, as reported in figure 5.12 for increasing stress times. From the reported curves one can notice that the variation with aging consists only in a translation (due to the increase in I_{th} as seen in figure 5.8), with no variation of T_0. The stability of T_0 during degradation is due to the invariance of LD characteristic parameters (in particular the injection efficiency η_i), at least in the range of temperatures studied within this analysis.

5.2.5 Deep Level Transient Spectroscopy

The results point out that stress induces an increase in the concentration of defects within the active region of the devices. It is possible to carry out Capacitance Deep Level Transient Spectroscopy (C-DLTS) for the identification of the defect/impurity levels involved in the degradation of InGaN-based laser diodes. Due to the limited active area of the laser diodes (ridge area is $1.5 \times 600\ \mu\text{m}^2$), C-DLTS study was carried out on LED-like samples, which have the same epitaxial structure of the LDs but a

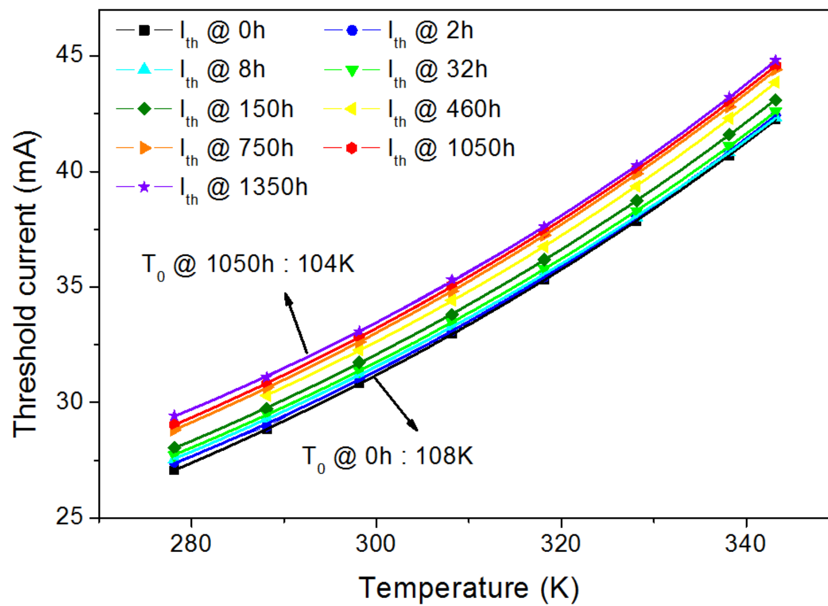


Figure 5.12: Characteristic temperature fits of LDs during stress at 4 kA/cm^2, 75 °C.

wider active surface (the area of the LED-like samples is 75 × 200 μm^2), resulting in an higher capacitance. The results obtained on LDs and LED-like samples can be compared since the two kinds of devices have similar degradation kinetics when stressed at similar current density and temperature levels, and have the same epitaxial structure. Before carrying out the C-DLTS analysis, the capacitive characteristics of the devices were simulated by means of a commercial 2D modeling tool (ISE-TCAD), in order to find out the levels of the filling and reverse pulses that must be used for the C-DLTS investigation. Results indicated that by using filling and reverse-bias of 2 V and -1 V respectively, we are able to effectively probe the entire active region, since the limit of the Space Charge Region (SCR) sweeps all its area during the C-DLTS test. These voltage levels are therefore suitable for analyzing the changes occurring in the active region as a consequence of the stress tests. Representative results of the simulations are summarized in figure 5.13, which reports the simulated band structure of one of the analyzed devices, the characteristics of the pulses used for the DLTS investigation, and the region investigated during the analysis [110].

In figure 5.14 are reported the results of the DLTS analysis obtained on one of the stressed samples during degradation time. Before stress, the signal of only one deep-level is detected: its peak is centered around 375 °K (black curve), and indicates

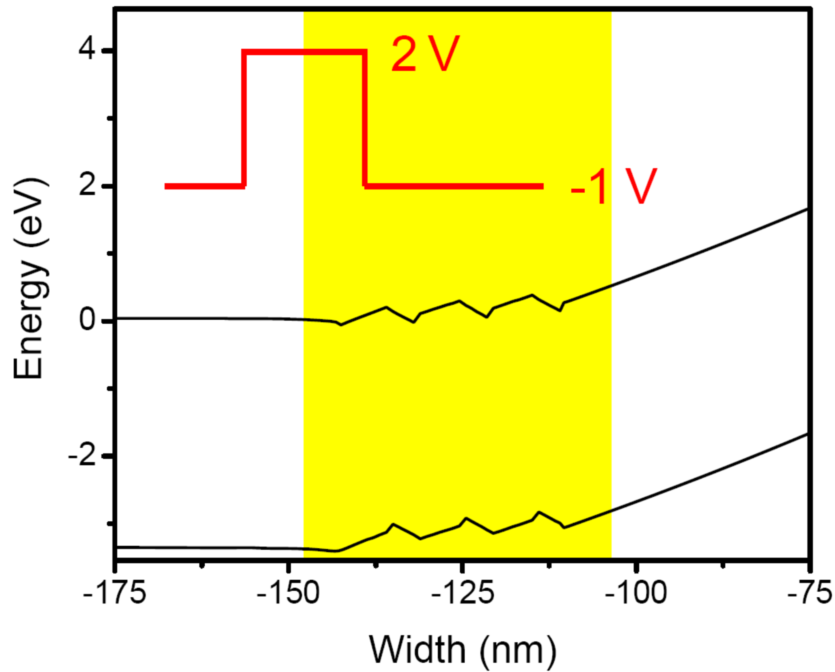


Figure 5.13: Simulated band diagrams of one of the analyzed devices. Inset: characteristics of the pulses used for DLTS analysis. Yellow area indicates the semiconductor region investigated using the adopted filling and reverse pulses.

the presence of an electron trap level, referred to as DL1 in the following.

The amplitude of this peak increases during stress time, indicating an increase in the concentration of DL1. Results indicate that the concentration of DL1 increases according to the square-root of stress time (figure 5.15), i. e. exactly with the same kinetics of the variation of Ith $(1/\eta - 1)$ of LDs submitted to constant current stress. The activation energy of this deep level is equal to 0.35 - 0.45 eV: the Arrhenius plot is reported in figure 5.16.

Results indicate that the Arrhenius plot of DL1 is very similar to that of level E2, which is often reported in the literature on bulk GaN layers (see for instance the Arrhenius plots reported in [111, 112]). Therefore, it is reasonable to think that DL1 and E2 have the same physical origin. Different explanations are suggested in the literature for level E2. This level can be related to:

- nitrogen antisite defects [111];
- to the residual magnesium concentration in GaN [113];

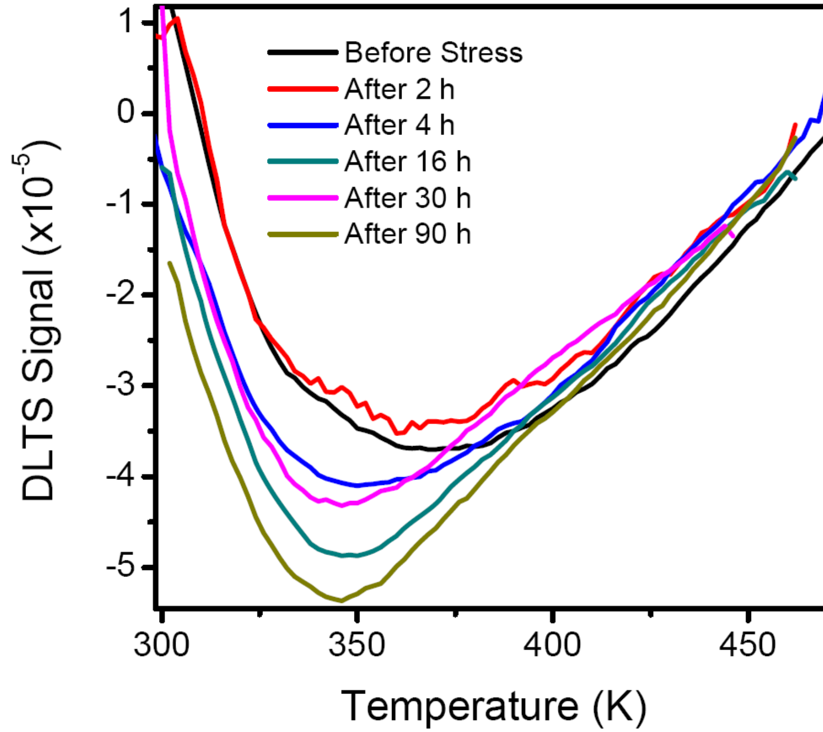


Figure 5.14: DLTS spectra measured at increasing stress times on one of the analyzed LED-like samples submitted to stress at 4 kA/cm^2, 75 °C.

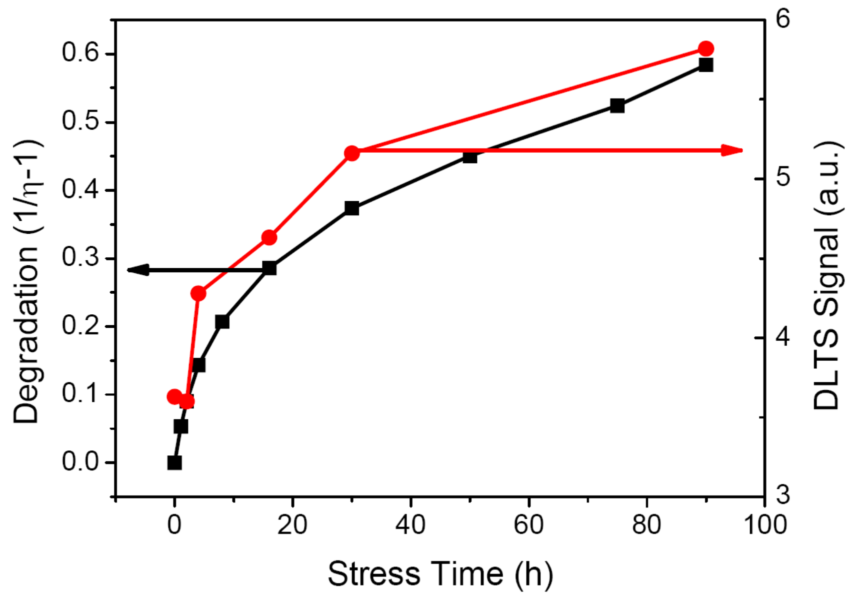


Figure 5.15: optical degradation and DLTS signal measured on one of the analyzed LED-like samples during stress at 4 kA/cm^2, 75 °C.

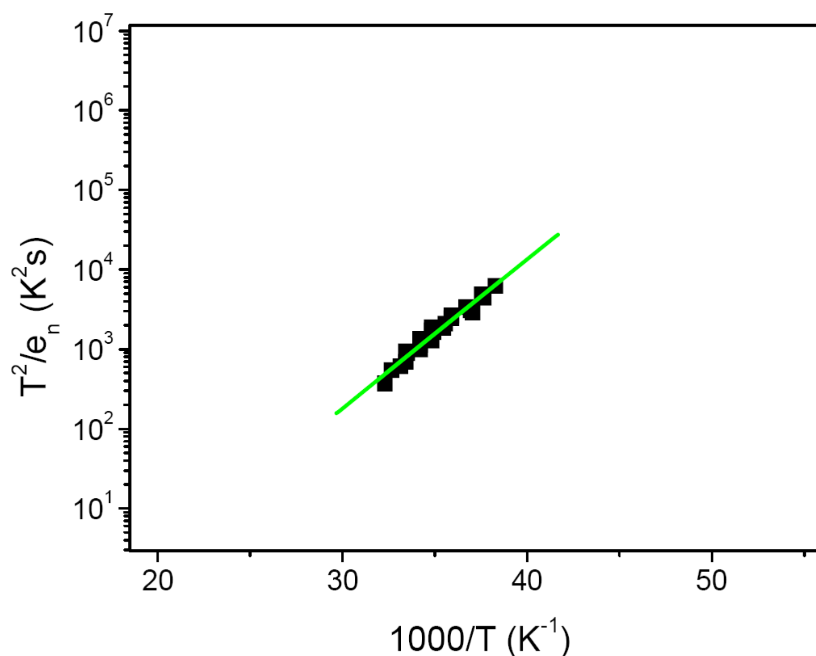


Figure 5.16: Arrhenius plot of level DL1.

- to foreign impurities, such as carbon [114];
- to vacancy-related point defects [112].

5.2.6 Conclusions

The purpose of this part is to describe the mechanisms causing InGaN laser degradation, with specific attention to defect concentration and injection efficiency. The experimental data, collected by means of electro-optical measurements, electroluminescence characterization, and near field emission measurements, provide experimental evidence for various effects:

- stress induces an increase in threshold current, according to the square root of stress time, and a decrease in sub-threshold emission;
- stress induces a slight variation in the slope efficiency of the LDs;
- during stress the output power of LED samples showed a significant decrease;
- the characteristic yellow luminescence signal decreased with a weaker dependence on stress time with respect to the main violet peak;

- LDs and LED-like samples degrade due to the same mechanism, as demonstrated by the analysis of the degradation kinetics.

We can deduce that:

- ageing causes an increase in defect density, therefore increasing the non-radiative recombination coefficient and lessening the output optical power;
- current confinement and injection efficiency do not significantly vary during stress time, causing only a minor decrease in slope efficiency;
- degradation is strongly correlated to the increase in the concentration of a trap level, located within the active region of the devices. The activation energy of this deep level is equal to 0.35 - 0.45 eV.

5.3 Laser diodes stress tests

Optoelectronic devices based on Gallium Nitride are rapidly emerging as excellent light sources for use in the lighting field, for optical data storage, for projection systems, and for optical signal transmission in the blue-green optical band. The creation of alloys containing Indium allows for the tuning of the peak wavelength, but still poses problems of reliability and lifetime in typical operating conditions. Current flow and joule heating are the main causes of degradation. The main mechanisms responsible for the decay of the performances are related to the creation of non-radiative recombination centers near the active region [115], induced by several causes, such as the formation of Nitrogen vacancies inside the active layer [116], the migration of defects towards the quantum wells [117, 118, 119] or the generation of point defects induced by Magnesium diffusion [120, 121]. In laser diodes, these driving forces play even a stronger role, due to the small dimensions of the active region, to the high optical power levels, and to the high current densities (which can be in excess of 10 kA/cm^2): the origin of accelerated degradation, mostly consisting in an increase in threshold current and decrease in slope efficiency, must be clearly identified. The aim of this work is to study the reliability of InGaN-based laser diodes and the physical mechanisms responsible for the changes of their performances under typical operating conditions [122].

The devices under test are commercially available blue InGaN-based Laser Diodes (LDs), with a typical output power of 100 mW and a peak wavelength of 405 nm at the nominal operating current of 120 mA. The average threshold current is 28 mA. The LDs are bonded in a standard TO 5.6 mm can package, that allows for a good thermal conductivity and ensures a good control over the chip temperature. Stress tests have been carried out at various currents (0, 20, 40, 60, 80, 100 mA) and temperatures (30, 45, 60, 75 ℃) using a Laser Diode Controller Alphaphotonics ILX Lightwave LDC-3916R. This LDC employs a Peltier temperature controller, which was used to fix the stress and measurement conditions, a precision current supply and a calibrated photodiode, to perform optical power measurements at a fixed and stable temperature (25 ℃ in our tests). This is very important given the strong dependence of the threshold current of a LD on the temperature discussed at page 131. At each step the main characteristics of the device have been measured:

- the voltage - current relationship, using a Semiconductor Parameter Analyzer HP 4155A, to obtain information on the variation of the conductivity of the devices;
- the output optical power at various bias currents, as previously described, from which the threshold current and slope efficiency can be calculated;
- the capacitance and conductance of the devices as a function of frequency and applied voltage, using a HP 4248A Precision LCR Meter, in order to understand how the charge distribution changes inside the LD.

5.3.1 Dopant activation

The analysis of the stress kinetics indicates the presence of two different mechanisms (figures 5.17 and 5.18), that induce an initial decrease and a subsequent increase of the threshold current. These two phenomena are visible during the entire span of our stress tests and act in conjunction to modify the electrical and optical parameters of the LDs. Luckily, the influence they have on the characteristics of the devices is strongly dependent on how much time has elapsed since the laser has been submitted to external stimuli. Therefore we can point out two different regions in the kinetics,

where one of these physical variations has a greater impact than the other, separated by a zone where they are comparable. In this section we analyze the first one, which is clearly identifiable up to nearly 32 hours of stress in our conditions.

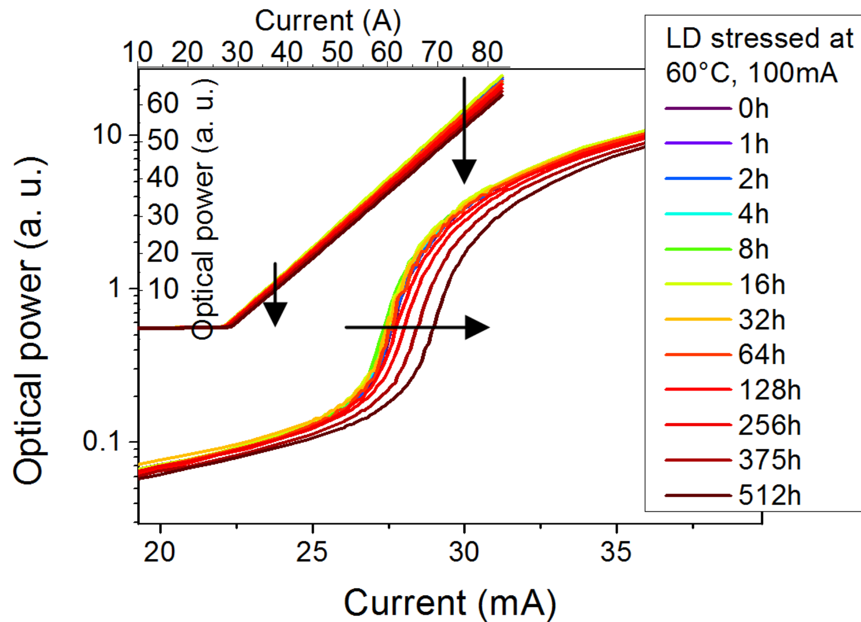


Figure 5.17: Output optical power versus bias current after various stress steps at 60 ℃, 100 mA.

Figure 5.17 reports the variation of the emitted optical power as a function of the injected current, while figure 5.18 reports the variation of threshold current measured during stress time. In the initial phase of the stress experiment, there is a significant improvement of the optical properties of the devices, mostly consisting in a decrease of the threshold current. As can be clearly seen, this variation exhibits almost no dependence on bias current, and is completely blocked when no electrons flow through the device and only temperature is applied as an external stress condition. Moreover, the effect is strongly promoted at higher temperatures (see figure 5.19, which reports the results of the first hours at different temperatures).

Based on previous literature reports [116, 123], this mechanism is attributed to the activation of the p-type dopant during the first steps of stress, induced by the flow of a high density of carriers within the active region of the devices. To understand this interpretation, we have to consider that after the growth of a p-type layer, only part of the Magnesium acceptor atoms are electrically active, due to the fact that

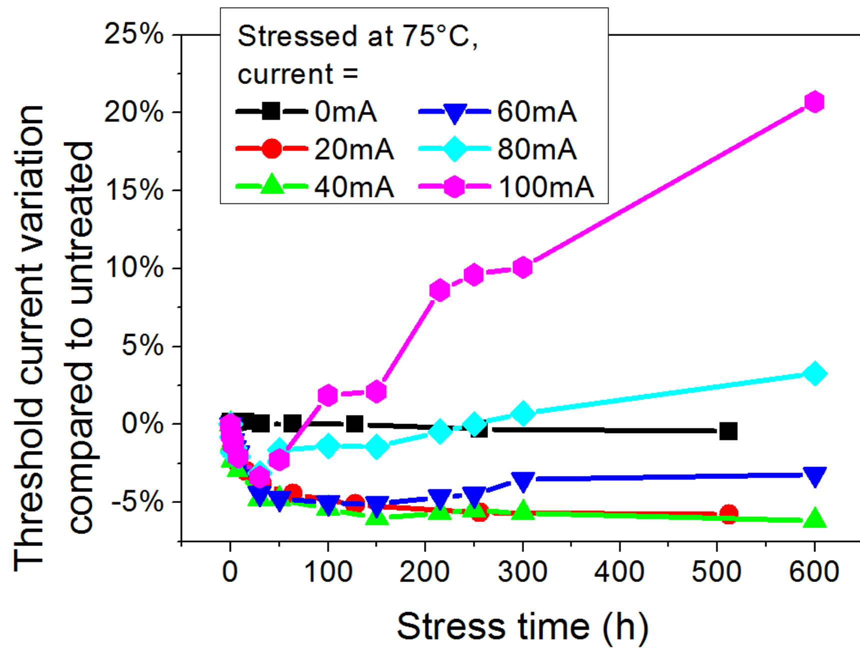


Figure 5.18: Effect of stress current on threshold current of LD stressed at 75 ℃.

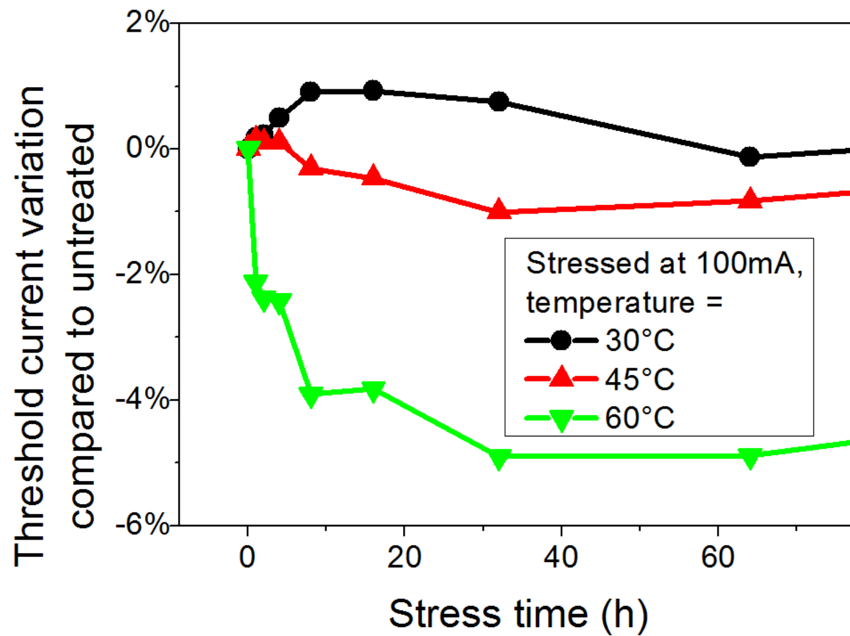


Figure 5.19: Variation of the threshold current during the first stress steps at 100 mA and various temperatures.

many Mg atoms are passivated by Hydrogen, through the formation of Mg-H bonds (where the Hydrogen is located at the Nitrogen anti-bonding site [124, 125]). To achieve a better activation of Mg, both high temperature annealing and low energy electron beam irradiation (LEEBI, [22, 126]) can be carried out. Even after these treatments, part of the Mg atoms can remain electrically inactive. The concentration of Magnesium and Hydrogen can be evaluated by means of Secondary Ion Mass Spectroscopy (SIMS) [127, 128]. The reduction of the threshold current described in figure 5.19 can be therefore ascribed to the partial re-activation of passivated Mg atoms, induced by the flow of highly energetic carriers [116]. A higher number of free holes in the p-GaN gives, at the same bias current, a larger ratio of positive carriers injected into the active region and a earlier increase of the emission. Figure 5.19 also shows how the variation of Ith is more prominent with the increase of the temperature, in agreement with the faster and greater activation. Moreover, as can be seen in figure 5.18, even stress currents as low as 20 mA are able to produce a change, whereas submitting the device only to different external temperatures (in the range tested in this paper) leaves the threshold current unaffected. This fact confirms the assumption of dopant activation.

Figure 5.20 shows that there exists a good correlation between various quantities that are influenced by an increased Magnesium activation:

- the threshold current decrease, which we have already extensively debated. A greater number of free holes gives an higher probability of radiative recombination when the same bias current is applied.

- the variation of the forward voltage of the laser diode. We find a decrease of its value measured at 27 mA (point chosen in order to check the voltage at a current value comparable to the threshold one). This behavior is in accordance with our explanation, since an higher activation of the dopant decreases the resistivity of the p-type layer.

- the drop of the conductance. In figure 5.20 is reported the variation of the conductance, evaluated at 10 kHz and 2.9 V. This value was chosen in order to investigate the change of the conductance when the barrier of the device

increases as a consequence of the higher p doping, which is more visible when the conductive mechanisms of the device are similar the most to the ideal one. This analysis was not possible from the current-voltage relationship since the difference between the various values was too small to be effectively estimated, whereas the impedance measurement, employing both the evaluation of the absolute value and of the phase difference between the voltage and current waveforms, is able to provide a more accurate reading. What we find is a decrease of the conductance, probably due to the increase in the voltage barrier as a consequence of the p-type dopant activation.

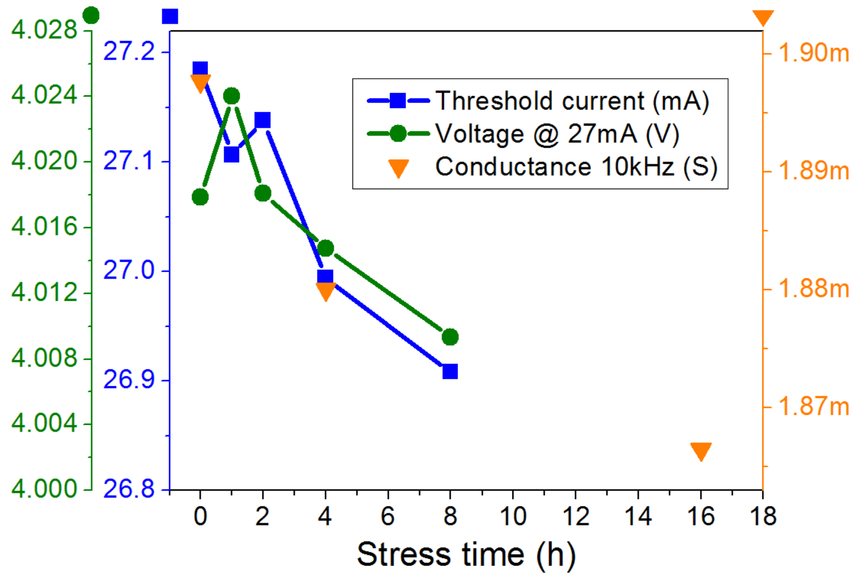


Figure 5.20: Correlation between the variation of threshold current, forward voltage and conductance at 2.9 V. Device stressed at 60 °C, 100 mA.

The possibility of an improvement of the ohmic contacts has not been considered, because its lower resistance could explain the behavior of the forward voltage, but is not consistent with the variation we see in threshold current and slope efficiency, that should be unaffected by its modifications. Since these quantities don't follow the ideal relationship, is it possible to have an improvement of the ohmic contact, but this effect has a lower impact on the characteristics of the device than the dopant activation.

The fact that stress induces an increase in the charge profile can be confirmed also by analyzing the changes of the capacitance when different voltages are applied.

The C - V profiles shown in figure 5.21 are strongly dependent on the charge that can be modulated by the probing AC small signal at a given DC bias, and their variation over stress time gives an indication on how the charge distribution and physical structure of the device evolve. The change of the total junction charge can be obtained integrating the capacitance over the voltage range where we have a variation of its value, 0 to 2 V in our case. In figure 5.22 we can see a clear increment of the carriers in coincidence with what we found in figure 5.19. The correspondence is not perfect because the influence of the concurrent generation of defects on the threshold current kinetic is stronger than on the junction charge.

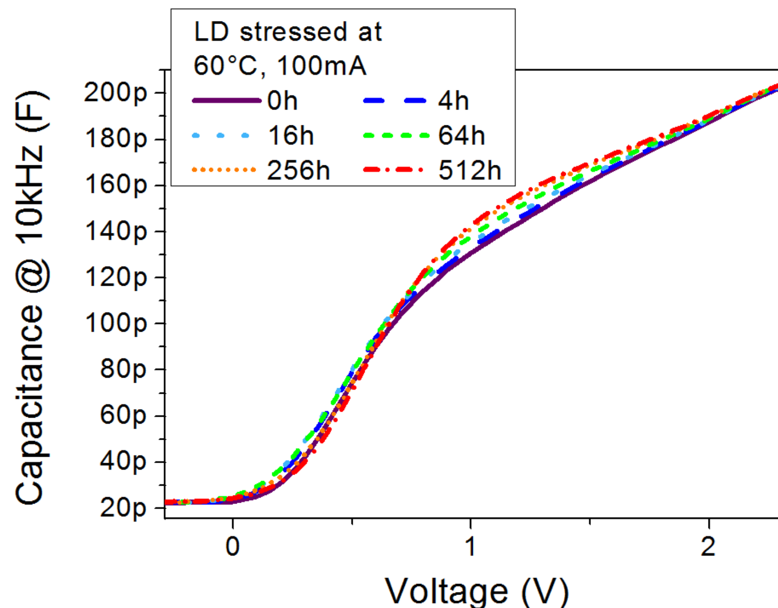


Figure 5.21: Capacitance variation during stress.

The activation of the p-type dopant is a phenomenon that is not always present in the lifetime of a device, since it is related to a partial annealing that comes from non completely refined growth conditions and post-processing. In order to gain other useful information that can confirm our assumption, it was verified that the decrease of the threshold current wasn't a recoverable effect in the temperature range under analysis. The electroluminescence spectra of the devices has also been measured and it was found found no appreciable shift of the peak wavelength or increase of the yellow parasitic emission. We can then assume that if defects are generated in this first region, their contribution to the optical characteristics of the devices is negligible.

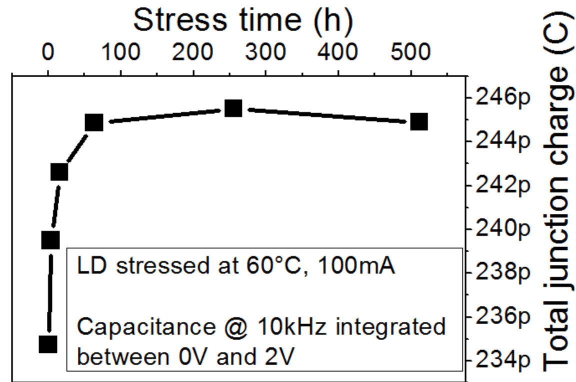


Figure 5.22: Junction charge variation during stress.

5.3.2 Creation of defects

In this section the second part of the degradation kinetics will be analyzed, which is dominated by an increase in the threshold current (figures 5.17 and 5.18). Based on previous literature reports [129, 130], this process is consistent with the generation of defects. They act as non-radiative recombination centers, lowering the ratio of carriers that are able to recombine radiatively an thus requiring an higher current in order to obtain the same light emission level. From the inset of figure 5.17 we can also notice a small decrease of the slope efficiency. Since this parameter is strongly correlated to coherent photon lifetime inside the cavity, given the fact that an increase of the non-radiative recombination means a decrease in carrier lifetime, this is another indication that stress induces the creation of defects that act as recombination centers and/or of the fact that stress induced changes in the reflectivity of the mirrors or of the injection efficiency. The main factors responsible for the degradation of GaN based optoelectronic devices have been extensively reported by several groups, and may be summarized as:

- deterioration of the ohmic contacts;
- generation of non-radiative recombination centers and deep levels;
- additional failure mechanisms leading to catastrophic damage and structural degradation, and to the formation of extended defects in the semiconductor.

Since the latter typically appears only at very high stress conditions, the long-term results of our lifetime tests can be explained by taking into account the first mechanisms.

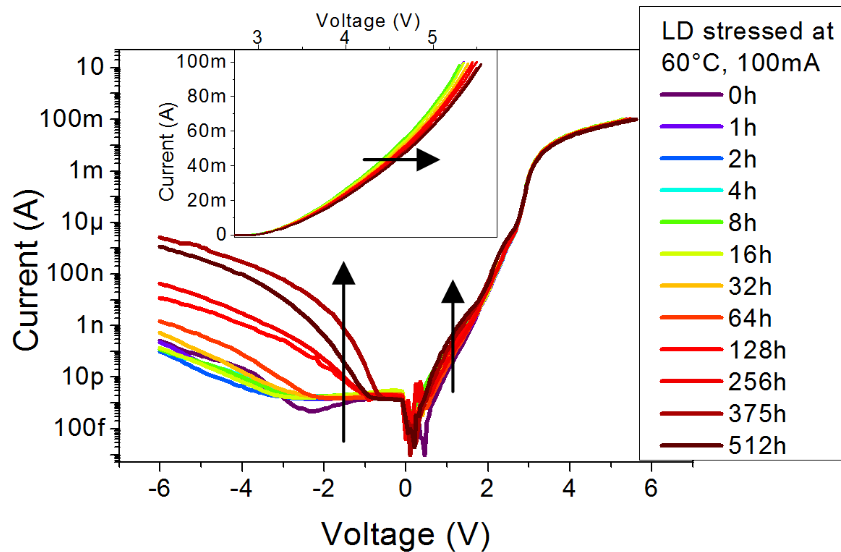


Figure 5.23: Current-voltage relationship of a Laser Diode stressed at 60 °C, 100 mA.

As can be seen in figure 5.23, after an initial slow degradation of the device, we have a strong increase of the reverse current and of the forward current below the turn-on voltage. This can be explained by the generation of defects, that in reverse bias increase leakage current by providing additional tunneling/recombination paths, and at low forward voltages act as current generation centers and promote carrier tunneling [35, 131]. The inset of figure 5.23 shows the variation of the current at higher voltage values. There is an increase of the series resistance of the device, mainly due to the degradation of the ohmic contacts. In order to confirm this interpretation, the variation of the threshold current at various stress temperatures (figure 5.24) and currents (figure 5.18) has been analyzed. The slope of the degradation increases at higher stress stimuli, and this is compatible with a faster generation of defects, as has already been reported by several groups. Moreover, from figure 5.18 we can see that the process responsible for the change of the threshold current requires both current and temperature in order to be activated, another fact that makes it congruous with the literature. Some paper report that the degradation kinetic of the threshold current follow a dependence on the stress time with a square-root law,

typical of most diffusive processes and usually ascribed to the diffusion of Magnesium along dislocations [106, 132]. In our case we have a great deviation from the square-root, more prominent at the lower temperatures, and the relationship seems to be linear as it is the case for generation of defects.

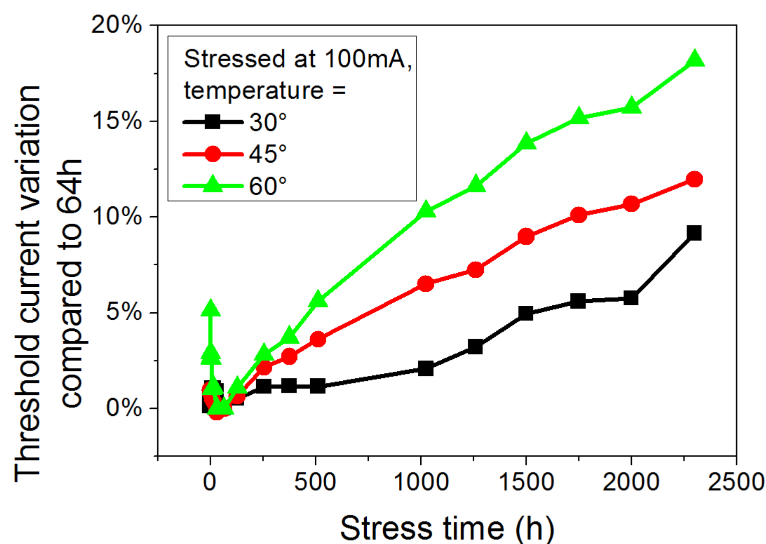


Figure 5.24: Effect of stress temperature on threshold current of LD stressed at 100 mA.

5.3.3 Conclusions

In this part have been analyzed the changes produced by accelerated lifetime tests, carried out at various temperature and bias conditions, on commercially available InGaN-based blue Laser Diodes. It is provided experimental evidence that the variation of the characteristics of the devices is due to two different mechanisms:

- an initial improvement of the performance of the devices, possibly due to an initial activation of the p-type dopant, promoted by the temperature and the flow of minority carriers;
- a long-term increase of the threshold current, due to the generation of defects inside the active region that act as non-radiative recombination centers.

These phenomena were identified by means of an extensive analysis of the main parameters of the laser diode, such as threshold current and slope efficiency, and by correlating electrical, optical and capacitive variations during the stress test.

Chapter 6

High frequency and power devices

6.1 Virtual gate

The aim of this part is to analyze how GIT structures react to high electric fields, by means of an extensive electrical and optical characterization. The gate region is composed by an intrinsic AlGaN layer, followed by a thick i-GaN zone (see figure 6.1). The formation of the 2DEG occurs at the interface between these two materials, and the AlGaN-GaN heterojunction prevents the injection of electron from the channel to the p-AlGaN. The GITs are grown on a Si substrate, with buffer layers composed of GaN/AlN multilayers over initial AlGaN/AlN layers. Devices are covered by a SiN Passivation. The transistors under analysis can be grouped into four types, with different gate - drain spacing (Lgd). The gate width is 100 μm and the gate - source distance (Lgs) is 1.5 μm. The various lengths combinations for the analyzed samples are summarized in table 6.1.

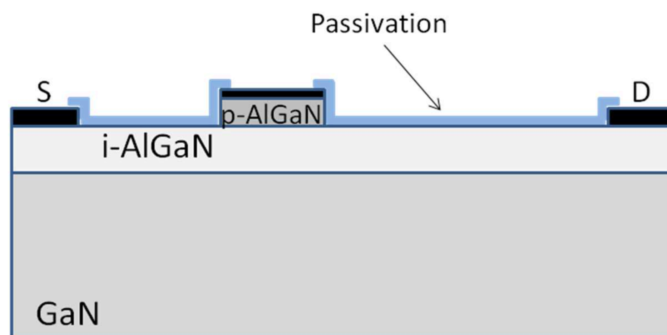


Figure 6.1: Schematic structure of the devices under test.

Sample	**Lgd** (μm)	**Lgs** (μm)
A	7.5	1.5
B	10	1.5
C	15	1.5
D	20	1.5

Table 6.1: Size of the devices under test (W = 100 μm).

6.1.1 Electrical characterization

In order to analyze the short-term trapping mechanisms occurring in the analyzed GITs, an extensive pulsed electrical characterization has been carried out, starting from different quiescent bias points (VG = 0 V, VD in the range 0 - 20 V). Measurements were performed using short (1 μs) pulses, while quiescent (trapping) bias was applied for 99 μs for each measurement point. Output characteristics were measured for VD levels in the range 0 - 20 V, and with VG levels in the range 1 - 3 V to prevent hole injection from the gate. During all these analyses the source was grounded. From the comparison between the various quiescent bias points, it is possible to evaluate the response of the drain current to the applied trapping voltage. Figure 6.2 reports representative output characteristics, measured starting from different quiescent bias points: GITs show almost no current collapse up to drain trapping voltages of 20 V. Measurements were obtained on devices of series A (see table 6.1).

To investigate the long-term trapping mechanisms, it was also performed a trapping experiment in on-state conditions. Charge trapping was induced by applying VG = 3 V, VD = 35 V for a period of 5 minutes, then devices were left unbiased to recover the effect of trapping. ID - VD characteristics were repeatedly measured before the test and during the following recovery time. As can be seen in figure 6.3, after 5 minutes at VG = 3 V, VD = 35 V devices showed a remarkable increase in on-resistance (see the decrease in drain current in the region VDS = 0 - 7 V). When the device is left unbiased, the current - voltage curve recovers its initial shape, suggesting that the observed degradation is due to a charge trapping mechanism.

Further details on the detrapping mechanism were obtained by measuring the variation of the time constant of the recovery process with temperature. The same experiment reported in figure 6.3 was repeated by varying device temperature from

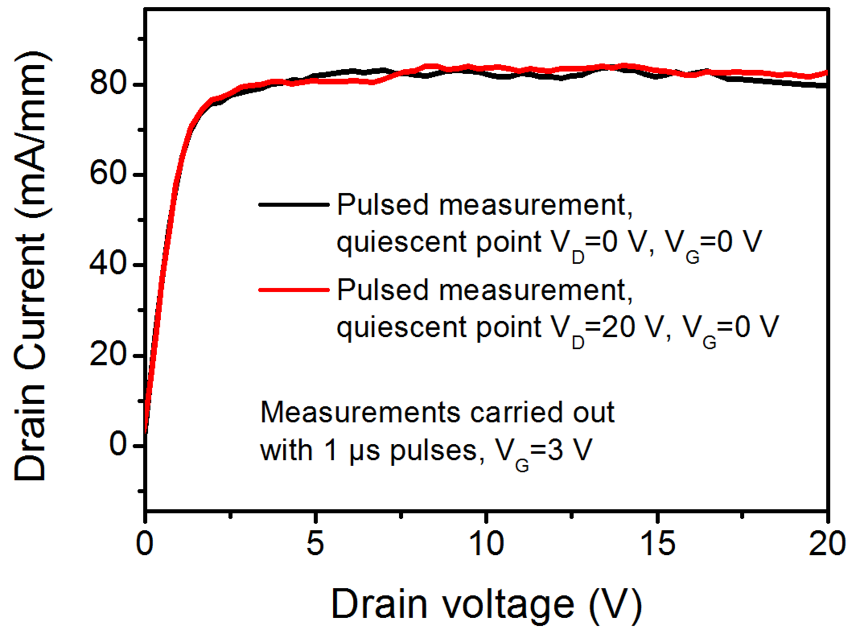


Figure 6.2: Pulsed characteristics of one of the analyzed samples, at different quiescent bias points (VG, VD).

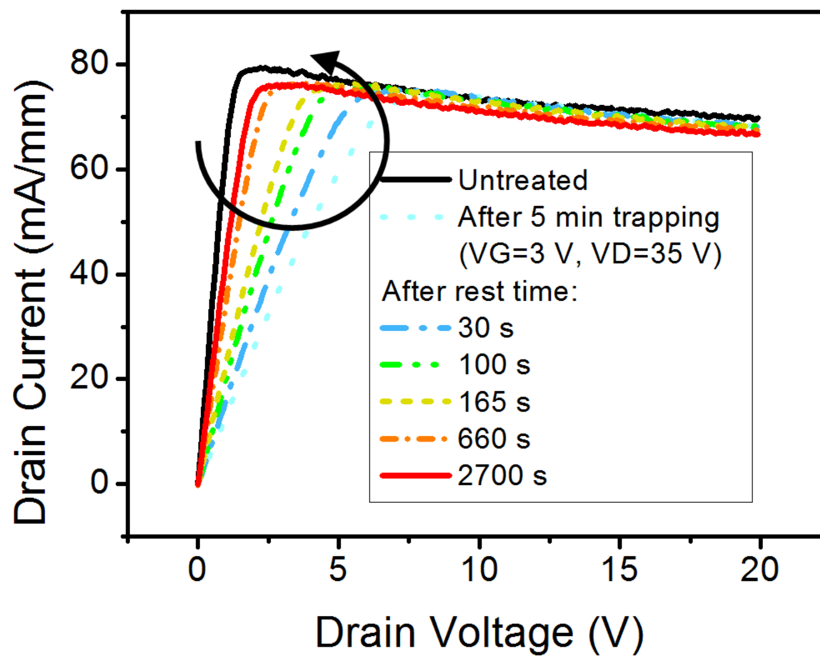


Figure 6.3: ID - VD characteristics over rest time, evaluated at VGS = 3 V.

15 °C to 52.5 °C (steps of 7.5 °C). The variation of the on-resistance, evaluated at VG = 3 V and VD = 1 V during the recovery test, is summarized in figure 6.4.

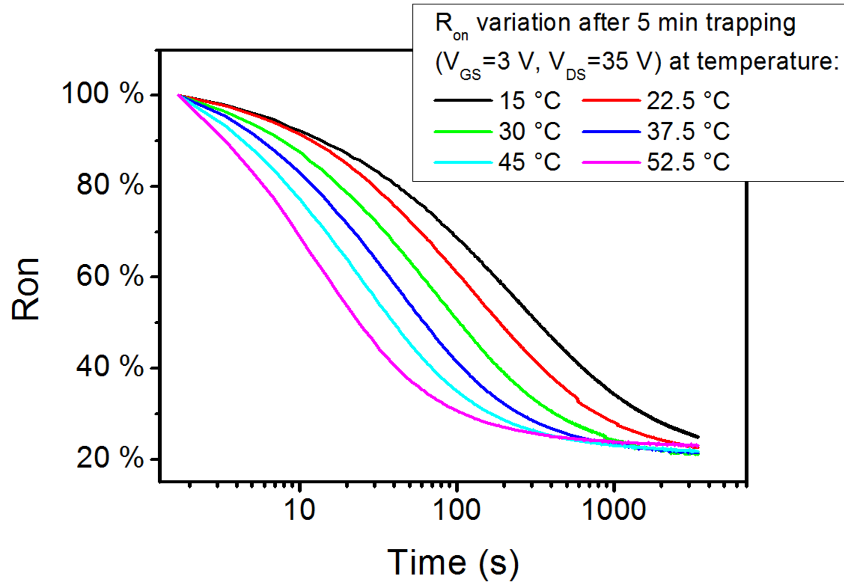


Figure 6.4: Variation of the on-resistance (VG = 3 V, VD = 1 V) over rest time at various external temperatures.

The kinetics of the current recovery are strongly influenced by temperature: de-trapping time decreases with increasing temperature. The activation energy of the detrapping process is 0.47 eV, as obtained from the Arrhenius plot of figure 6.5.

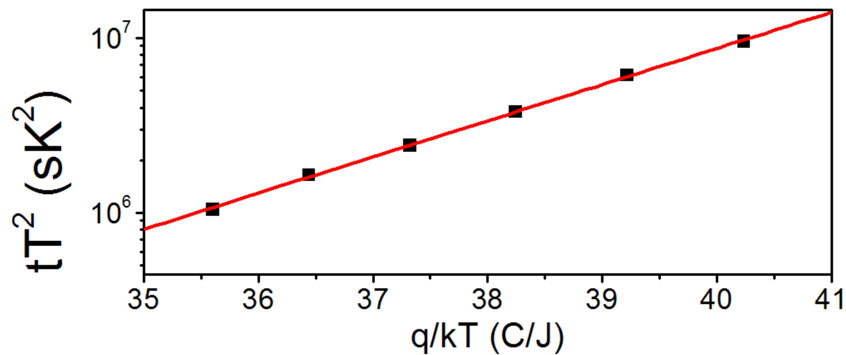


Figure 6.5: Arrhenius plot of the de-trapping process. Activation energy is 0.47 eV.

The structure of GITs is based on the use of a p-type AlGaN layer: by applying a positive voltage on the gate, holes can be injected towards the channel. The results indicated that, by injecting holes from the gate, the detrapping kinetics can

be significantly accelerated. In figure 6.6 it is reported the variation of on-resistance measured, after a trapping period of 5 minutes at VG = 3 V and VD = 35 V, by injecting different gate current densities. The time constant of the detrapping mechanism exhibits a linear dependence on the injected gate current density (see the inset of figure 6.6). This effect could be explained by taking into account two different mechanisms: the recall of trapped electrons towards the positive voltage of the gate, and/or the recombination between the trapped electrons and the injected holes.

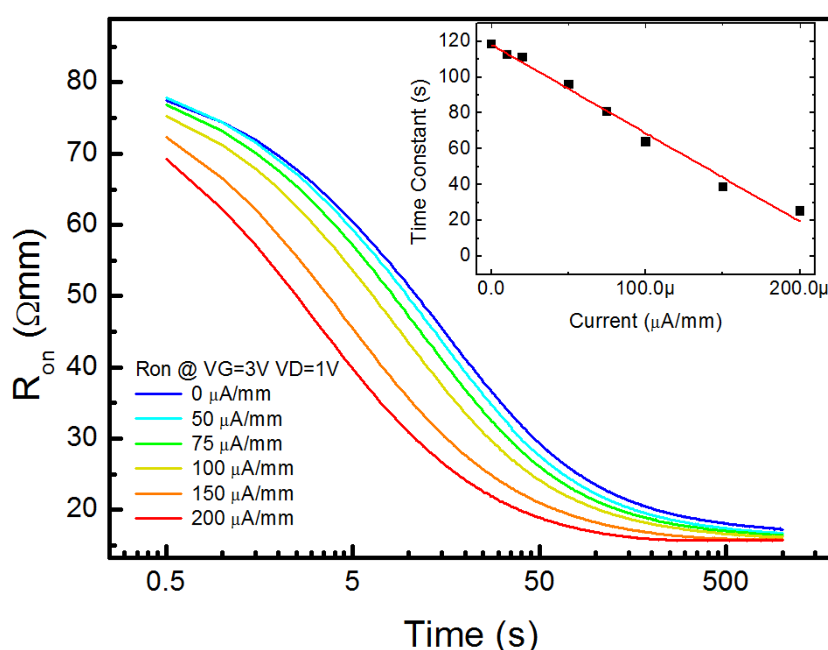


Figure 6.6: variation of the ON-resistance (VG = 3 V, VD = 1 V) over rest time at various injection currents.

6.1.2 Optical characterization

After this extensive investigation of the mechanisms responsible of the de-trapping phenomenon in various conditions, time- and spatially-resolved electroluminescence measurements were performed to achieve a better understanding of the origin and dependencies of the trapping. The devices were kept at a constant VG = 3 V for 5 minutes, and in the meanwhile their emission was repeatedly monitored. The experiment was repeated at various VD levels (from 30 V to 60 V, step 5 V) for each of the four types of transistors (see table 6.1). Generally, a GaN-based HEMT

emits light due to intraband transitions of highly-energetic electrons, and shows a luminescence peak where the electric field is maximum. This usually occurs at the drain edge of the gate [95]. The spectrum of the light emitted by a GIT in these bias conditions has a maxwellian shape (see typical spectra in figure 6.7), further confirming the hypothesis of an emission caused by the hot electrons generated in high electric field regions of the device [133].

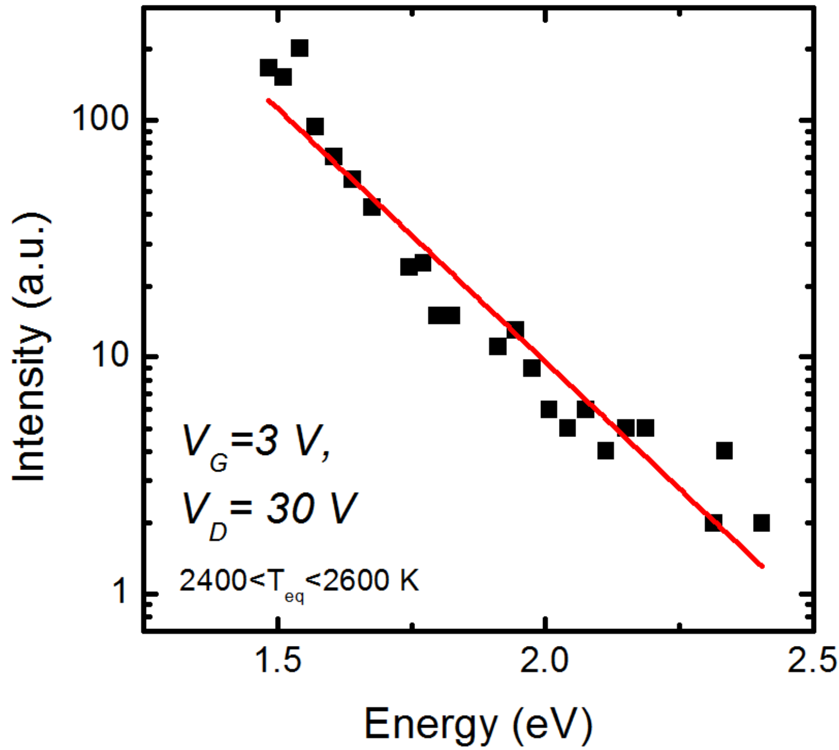


Figure 6.7: Maxwellian shape of the EL spectrum measured at VG = 3 V and VD = 30 V.

In Gate Injection Transistors we have found a shift of the EL from the gate to the drain contact over trapping time, reported in figure 6.8. At the beginning of the trapping period, EL signal is localized at the edge of the gate, towards the drain. After a certain interval t_d, a rapid increase in the luminescence signal occurs close to the drain pad. The delay time t_d was found to be strongly dependent on the electric field between the gate and the drain (see figure 6.9 (a)). In fact, when the trapping voltage increases, the delay time before the onset of the drain luminescence becomes progressively smaller, thus suggesting an inversely - dependent relationship with the

applied potential. Furthermore, as indicated in figure 6.9 (b), t_d is linearly dependent on the gate-drain distance, and this result confirms that the trapping process is field - dependent.

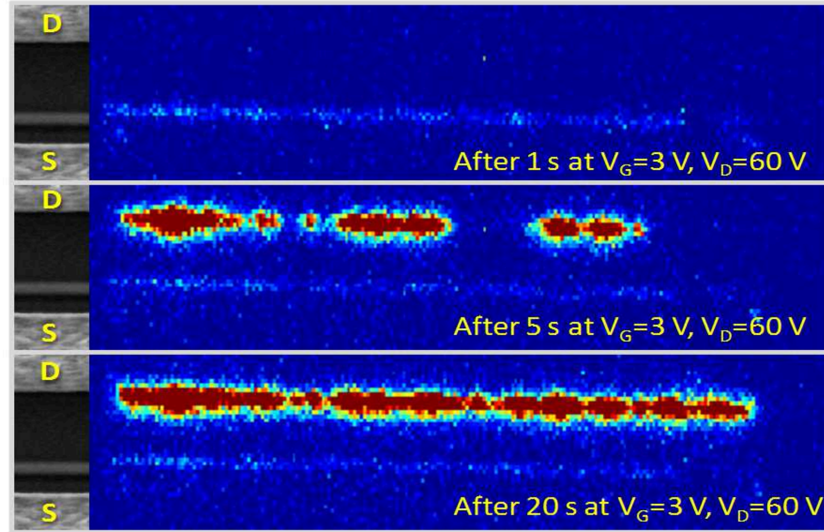


Figure 6.8: Electroluminescence variation during 5 minutes trapping at VG = 3 V, VD = 60 V.

Results suggest that the trapping of negative charge within the gate - drain access region can be responsible of a virtual-gate effect, with subsequent increase in on-resistance. Moreover, the formation of a virtual gate can explain the observed shift of the EL peak, according to the following model: at high drain voltages, accelerated electrons can be trapped in the gate - drain access region. As the trapped charge increases, the peak of the electric field at the drain side of the gate becomes smaller, resulting in a lower acceleration of the electrons, and in a decrease in the EL signal. After a delay time t_d, a "critical" amount of charge is accumulated and trapped in the gate - drain access region, and this generates a virtual gate, with subsequent shift of the luminescence peak towards the drain. The dependence of t_d on the applied voltage can be modeled by considering the lucky-electron approximation. The number of carriers injected towards the gate - drain access region at a given current level can be expressed as

$$\frac{I_{inj}}{ID} \approx e^{-\frac{\varphi}{q\lambda E}}$$

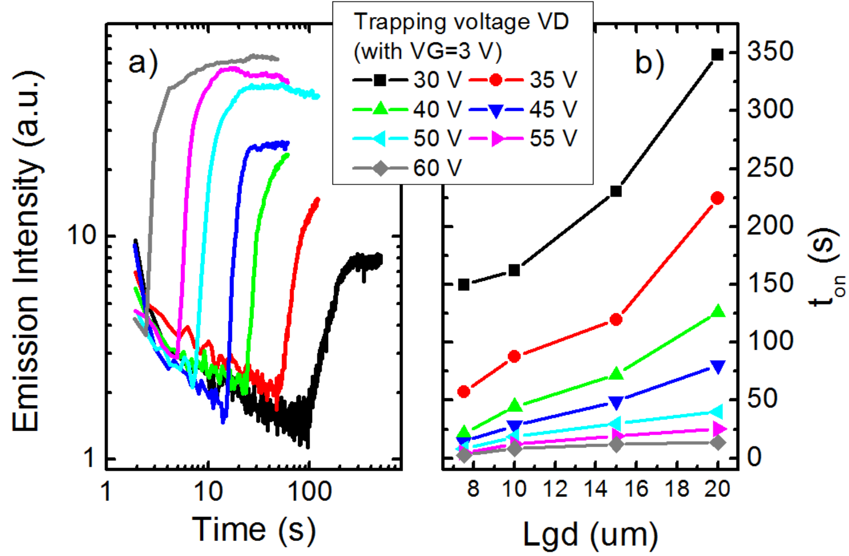


Figure 6.9: Dependence of the delay time on a) applied voltage and b) gate - drain distance.

where I_{inj} and ID are, respectively, the injected current and the drain current, φ is the potential barrier, q the electron charge, λ the mean free path and E the accelerating electric field in the gate - drain direction. The time required to build up enough charge to observe the onset of the drain luminescence, using the previous equation, follows the relationship with the drain voltage

$$t_d \approx e^{\frac{\varphi}{q\lambda E}}$$

in good agreement with the experimental data (figure 6.10).

The samples analyzed were not optimized with respect to trapping: they were test structures, fabricated with the specific aim of studying high-voltage trapping phenomena. The trapping problems detected were eliminated through the improvement of the crystal quality and the processing. This allowed to fabricate improved device structures which can withstand a VD level of 100 V in on-state, without showing any trapping effect.

6.1.3 Conclusions

This part presents a study of long-term trapping processes that occur in AlGaN/GaN transistors with p-type gate at high voltage levels. By means of pulsed

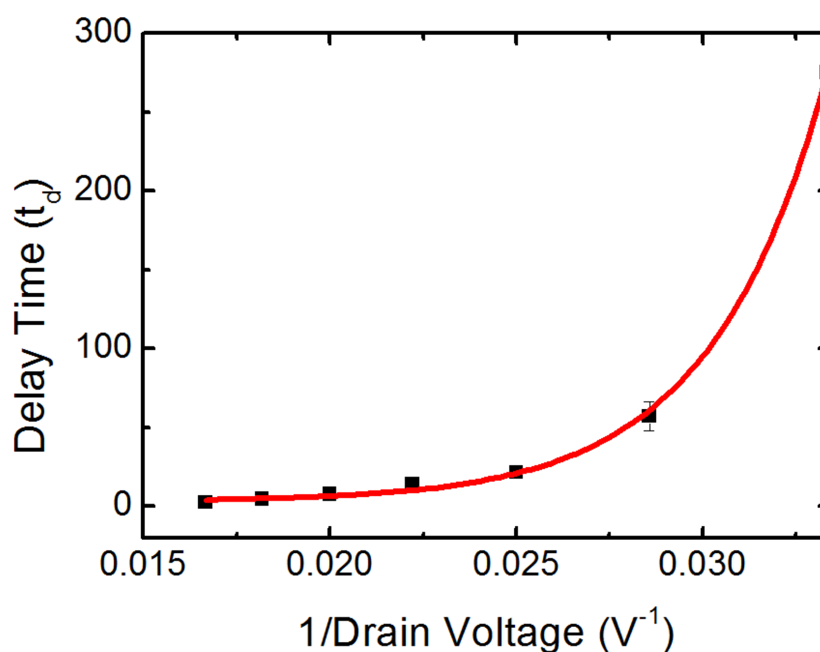


Figure 6.10: Model for the extrapolation of the delay time.

and DC electrical measurements and space- and time- resolved electroluminescence maps, the trapping and recovery kinetics of the devices under different bias regimes were analyzed. Results indicate that:

- while GITs have a negligible current collapse, long-term (ON-state) operation can induce a remarkable increase in the ON-resistance;
- this increase is not permanent: the initial conditions can be recovered after a rest period. Recovery kinetics are accelerated at high temperature levels, or by injecting a hole current through the gate;
- as a consequence of trapping, the peak of the electric field, detected by means of electroluminescence measurements, moves towards the drain;
- the onset of drain luminescence strongly depends on the applied voltage and on the gate - drain distance.

A first-order model based on the lucky-electron approximation explains with good confidence levels the trapping mechanism.

6.2 Current collapse and gate quiescent bias point

The double pulse technique is one of the basic tests that can be carried out on a device to evaluate its dynamic performances and the effects of trapping (see page 107). Even if the detection of a deep level and the elementary characterization are outside the more detailed aim of a Ph. D. thesis, an interesting aspect has been found and will be described. Various double pulse experiments were carried out at an high drain quiescent bias point voltage (VD QBP = 30 V) and an increasing gate voltage (VG QBP from 0 V to 0 1 V, step 0.2 V). The devices under test were PD10 GITs, the length of the p-type AlGaN along the direction of the current flow was Lg = 0.6 μm, and the gate - drain distance Lgd =1.45 μm (see figure 3.18). It was found an increase of the on-resistance directly proportional to the gate voltage during the quiescent bias phase (see figure 6.11). This effect suggests that the devices are affected by on-state trapping, visible even when the trapping voltage at the gate is low if the drain voltage is high.

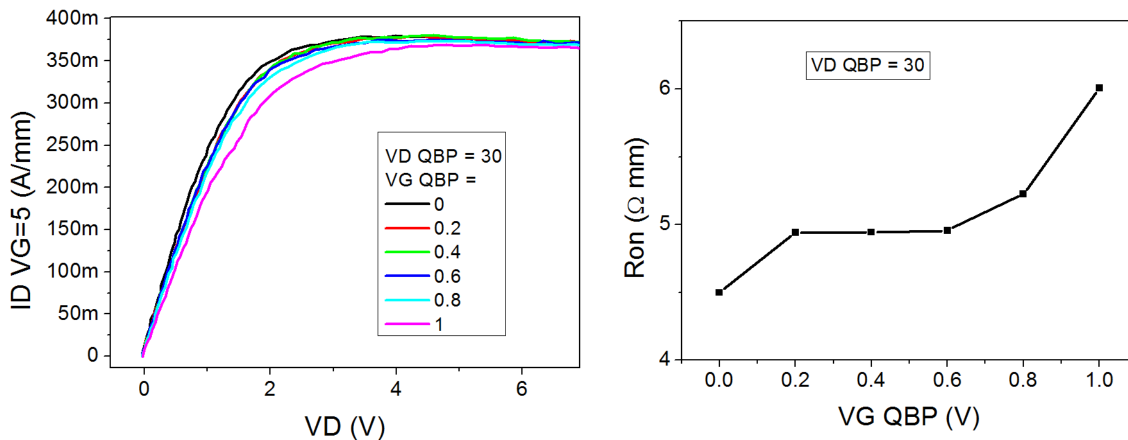


Figure 6.11: Ron variation as a function of the gate voltage during the quiescent bias phase. VD QBP = 30 V.

In order to validate this hypothesis, the on-state trapping was checked up to VG QBP = 3 V but at a lower VD QBP (0, 5, 10 V), since it was necessary to prevent the degradation of the device. Moreover, these drain values are more similar to the usual on-state bias of the devices. The curves in figure 6.12 confirm the assumption: when the VD QBP is increased, the ID-VD relationship up to VG QBP = 1.5 V remains unchanged, while at higher gate quiescent bias point voltages (and then at

stronger on-state condition during the trapping phase) there is an evident collapse of the drain current due to the accumulation of more trapped charge.

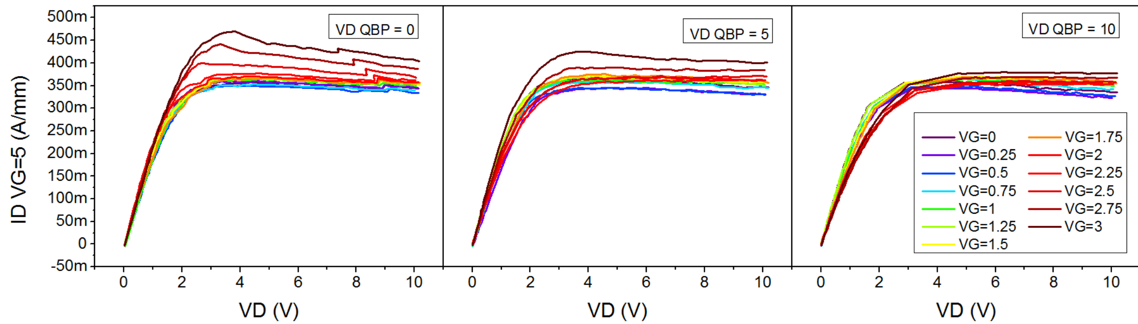


Figure 6.12: Current collapse as a function of the gate voltage during the quiescent bias phase. VD QBP = 0, 5, 10 V.

It can be noticed that, even if the presence of both an high drain and gate voltage during the quiescent bias phase has a detrimental effect on the on-resistance, the current collapse in the saturation region is mitigated by a very high VG QBP. This twofold behavior can be explained taking into account the specific structure of a Gate Injection Transistor described in figure 6.13, which also highlights the regions were take place the two different effects that will be described.

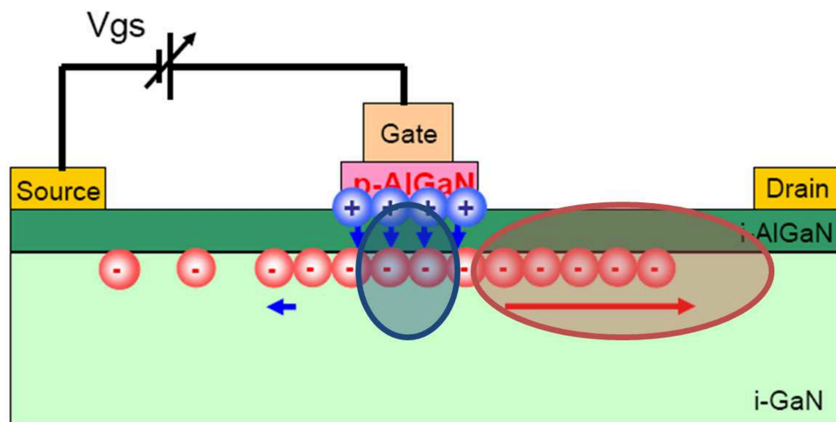


Figure 6.13: Schematic structure of a GIT. The regions where occur different trapping mechanisms are highlighted.

- Saturation region (blue): at higher VGs, the hole injection under the gate increases, and the trapping in this region is lowered. This has a positive effect

on the threshold voltage, which gives an increased saturation current. In figure 6.14 (a) is reported the relationship between the saturation current and the VG QBP, and the good correlation between the detrapping and the gate current (an effect that was also previously described in other devices at page 150).

- Linear region (red): at higher VGs, the electron density inside the channel is enhanced. This gives more trapping in the gate - drain (and gate - source) region, worsening the ON-resistance. The relationship between the on-resistance and the VG QBP is shown in figure 6.14 (b), along the correlation between its value and the drain current responsible of the filling of the traps. The positive effect of hole injection could be seen also on the on-resistance at very high VGs, where its value drops.

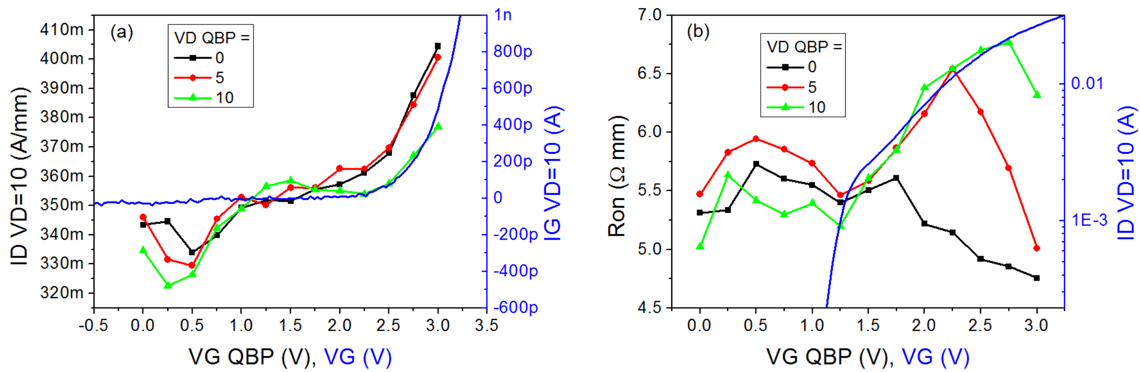


Figure 6.14: IDss and Ron variation as a function of the gate voltage during the quiescent bias phase. VD QBP = 0, 5, 10 V, and their correlation with the gate and drain currents.

6.3 Drain current transients

The drain current transients technique, described in great detail at page 111, can be used to extract the activation energy of the trapping and detrapping processes present inside the device, which can be used, in comparison with other values reported in the literature, to identify the physical mechanism responsible for the current collapse. These tests have been carried out on PD8 or newer devices, since they are the transistor with the better dynamic performances.

PD8

In saturation region, after an initial transient due to the response of the experimental setup, one emission process has been identified. Its time constant at different temperatures was extracted in order to calculate its activation energy, which was found to be 0.14 eV. The gate - drain distance of the device was Lgd = 10 μm.

The on-resistance was also analyzed. In linear region one emission process has been clearly identified. The time constant of this process is nearly temperature - independent (in the temperature range under analysis). Figure 6.15 shows the transients and the corresponding time constant spectra, while figure 6.16 reports the Arrhenius plots of the two processes. In both cases the filling condition was Vgs = 0 V and Vds = 60 V.

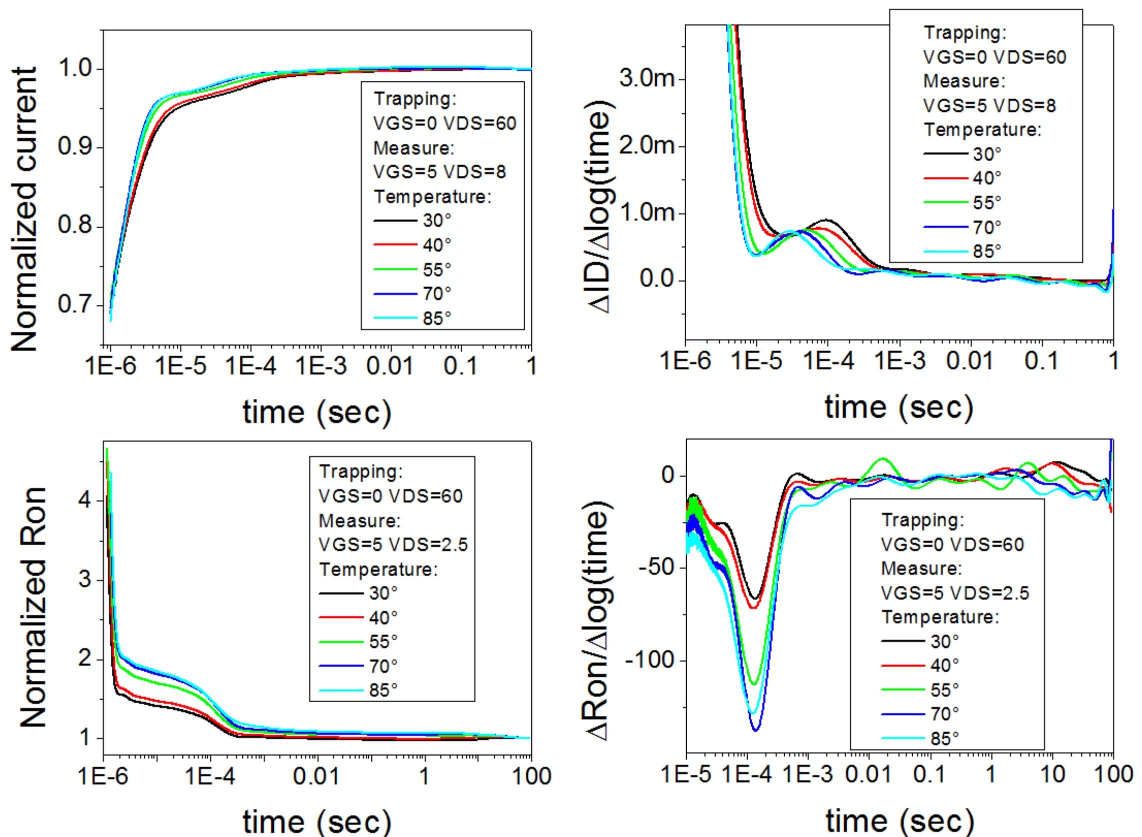


Figure 6.15: Drain current transients and time constant spectra in saturation and linear region for a PD8 device.

In figure 6.17, these Arrhenius plots are compared to other deep levels reported

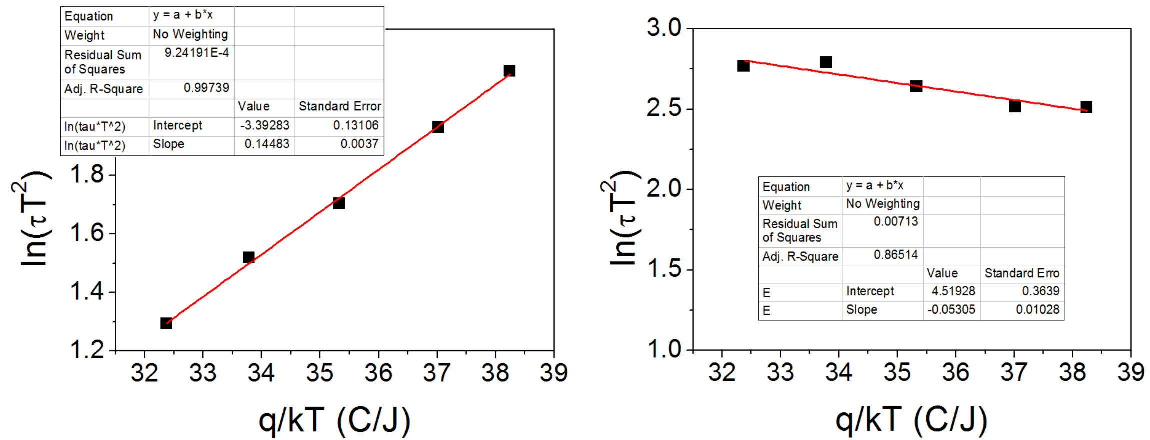


Figure 6.16: Arrhenius plots in saturation and linear region for a PD8 device.

in the literature. There is a good agreement with the data reported by Polyakov et al. [134] on various p-AlGaN and p-GaN bulks. It has to be remembered that the devices under test employ a p-AlGaN layer under the gate.

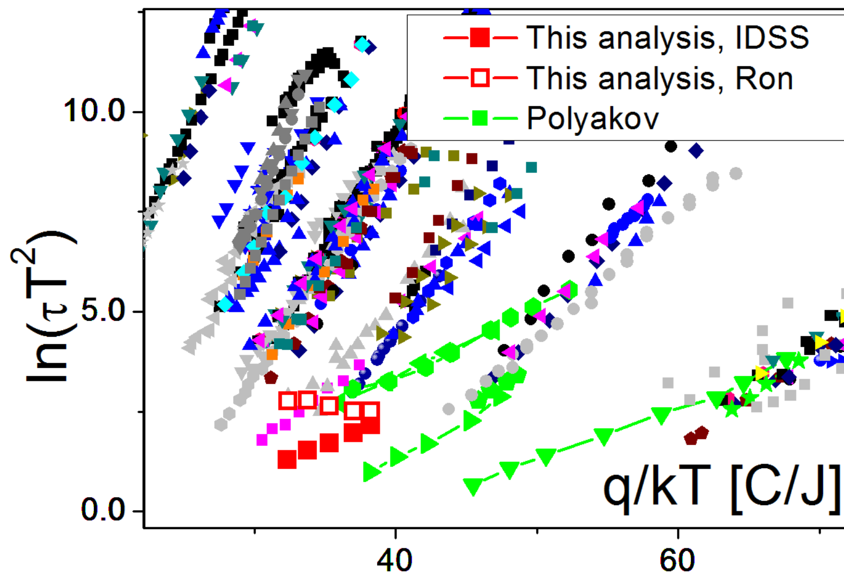


Figure 6.17: Comparison of the Arrhenius plots with the ones reported in the literature, PD8 device.

PD10

When the same analysis was carried out on PD10 devices, it was found a combined emission and capture process visible at short times (see figure 6.18). Since those

processes vanish at higher negative gate trapping voltages, the following analysis was performed in this condition (filling Vds = 10, Vgs = -10) in order to isolate the emission at nearly 0.1 seconds. The dimensions of the device under test were Lg = 0.6 μm and Lgd = 1.45 μm, using the conventions defined in figure 3.18.

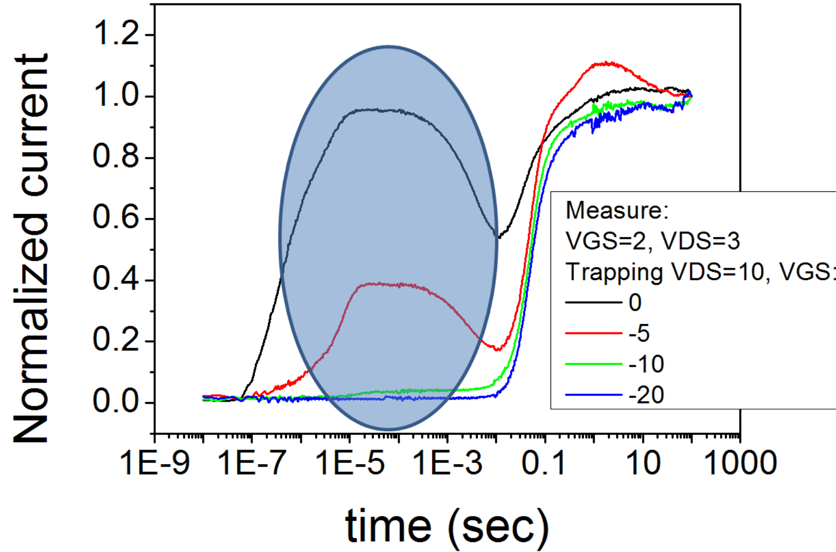


Figure 6.18: Drain current transients in saturation region of a PD10 device at various filling Vgs levels.

In saturation region and linear region one emission process has been identified. In the first case the activation energy was 0.13 eV, while the second process was not thermally activated. Figure 6.19 shows the transients and the corresponding time constant spectra, while figure 6.20 reports the Arrhenius plots of the two processes.

Figure 6.21 reports these data along the ones found by Polyakov et al.

6.4 Gate Frequency Sweeps

Gate Injection transistors exhibit a good stability when an external drain field is applied, showing almost no current collapse up to moderate drain voltage levels in both off-state and on-state conditions [135]. At higher drain voltages, trapping phenomena may take place, mainly due to hot electrons [136] or lucky electrons [137]. The trapped charge may adversely affect the performances of the device, increasing its on-resistance and thus the electrical power lost by dissipation when it is operated

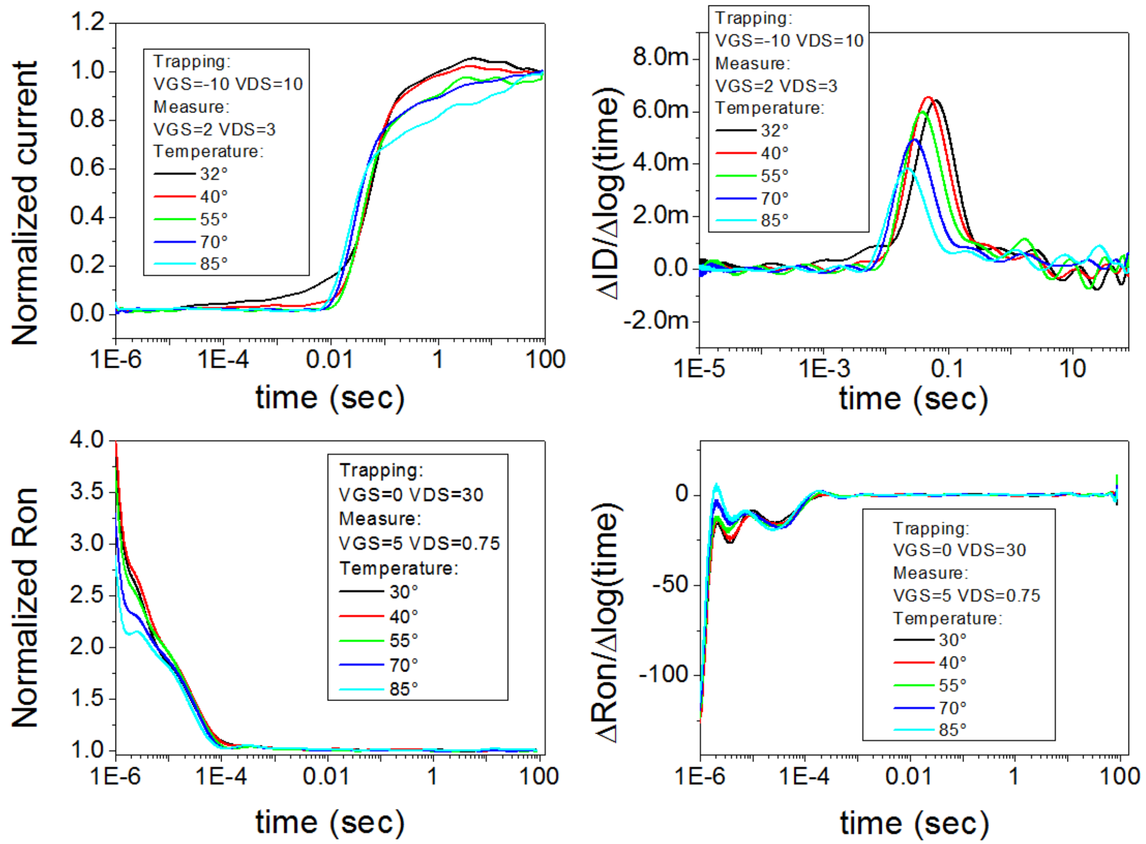


Figure 6.19: Drain current transients and time constant spectra in saturation and linear region for a PD10 device.

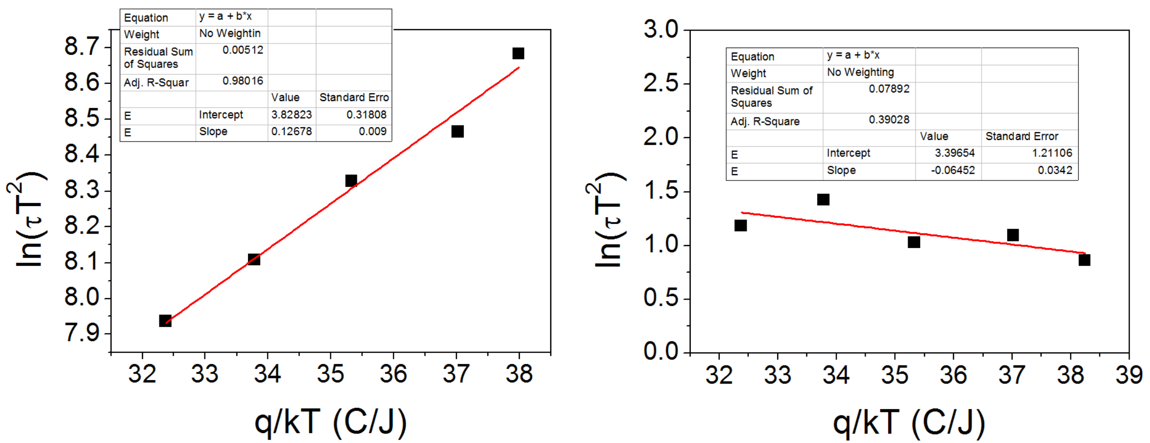


Figure 6.20: Arrhenius plots in saturation and linear region for a PD10 device.

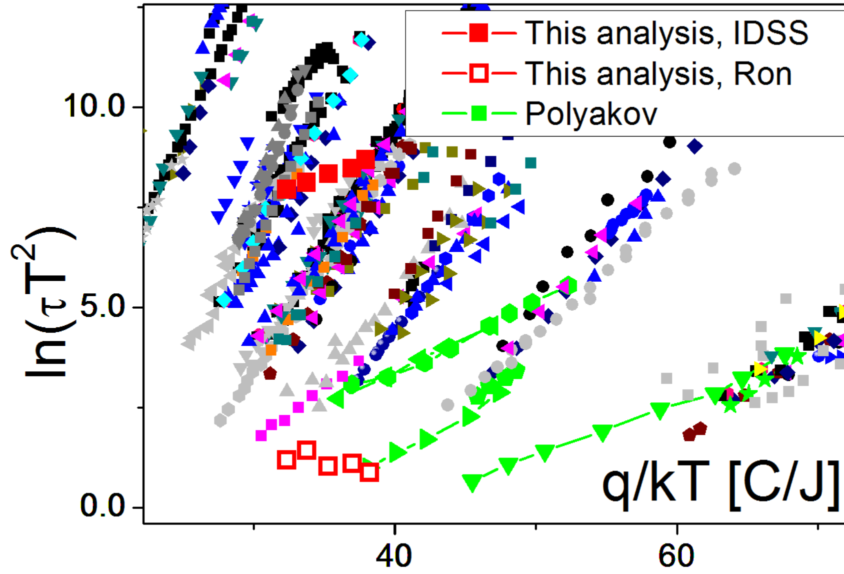


Figure 6.21: Comparison of the Arrhenius plots with the ones reported in the literature, PD10 device.

as a power switch. Several techniques have been suggested in order to evaluate the effect of the trapping on the characteristics of the devices, such as drain current deep level transient spectroscopy (I-DLTS) [138], double pulse measurements [92] and drain current transients [94, 139, 140]. These techniques can be used in order to obtain an extensive knowledge of the trap response and to extract the activation energy of the deep level, but they don't give any indication on how the device will perform in a practical switching application [141]. In this section a different test will be presented, the Gate Frequency Sweep (GFS), which can be used to evaluate the effect of high voltage trapping in a real operating scenario and to give an estimation of the activation energy of the detrapping process.

6.4.1 The technique

A gate frequency sweep consists on applying a square wave (duty cycle 50 %) to both the gate and drain terminal while the source and the substrate are grounded, until the device reaches its steady-state. In the first half of the square wave the device is biased in a filling condition which can be chosen considering the typical application of the device; in our case we have a power switching device that should be able to withstand an high drain voltage in off-state operation, so VG = 0 V and VD = 40 V

was chosen. The second half of the square wave is the measurement phase we have to carry out in order to evaluate the effect of the trapping condition on the performances of the device when used in a typical operating regime, so the transistor was biased in its linear region at VG = 5 V and VD = 3 V and its current at the end of the square wave was obtained with an oscilloscope as the voltage drop over a known resistance. This bias pattern is repeated at various frequencies up to 5 MHz. Figure 6.22 a) shows some measurement pulses which can be obtained with this technique. The corresponding current value is influenced by all the trapping and de-trapping processes inside the device, and its specific figure is determined by the relationship between the various time constants. Figure 6.22 b) reports the results of tests carried out at different temperatures. It is clearly visible a decrement of the drain current that is dependent on the bias frequency, due to the different weight that the filling and the measure part have when the device is biased for shorter periods of time. This effect is more prominent at lower temperatures because an higher temperature promotes the detrapping process, mitigating the effect of the same filling voltage and then reducing the current drop.

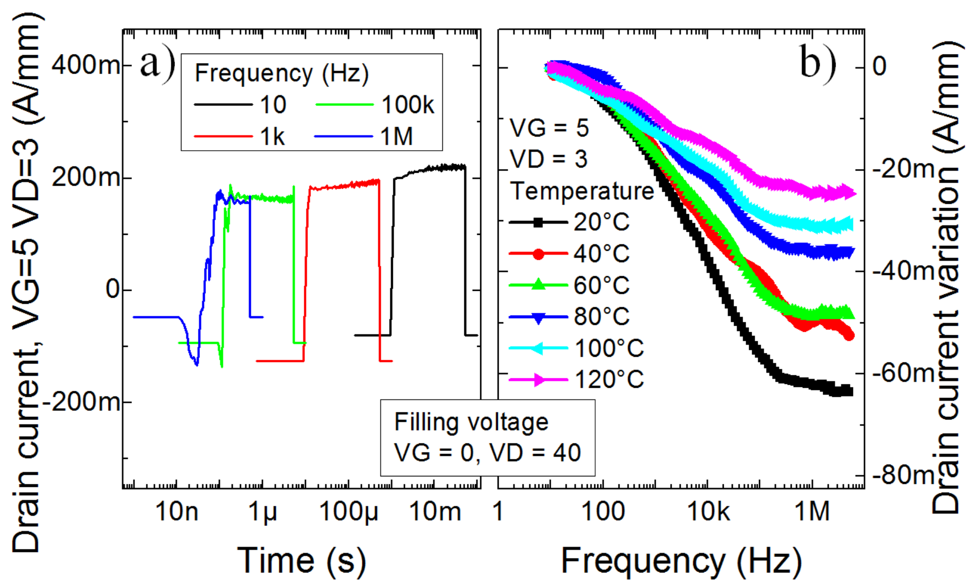


Figure 6.22: After a filling voltage of VG = 0 V and VD = 40 V (source grounded), figure shows a) some of the recorded current responses and b) the variation of the drain current as a function of the square wave frequency at different temperatures. Values measured at VG = 5 V and VD = 3 V.

The current variation at high frequency is not caused by the limited bandwidth of the experimental setup. It is an effect of the increased quantity of trapped charge when an high drain voltage is applied during the filling phase. This assumption is confirmed by figure 6.23, which reports the comparison between a double pulse measurement and a gate frequency sweep test. In figure 6.23 a), the drain current in the linear region of the characteristic is strongly influenced by the increased drain filling voltage, which has a negative effect on the switching performances of the device. As a matter of fact, this behavior is detected by the switching tests carried out during the gate frequency sweep (figure 6.23 b)). When the frequency increases, the drop of the drain current is more prominent when the device has to sustain an higher source-drain voltage during its filling phase.

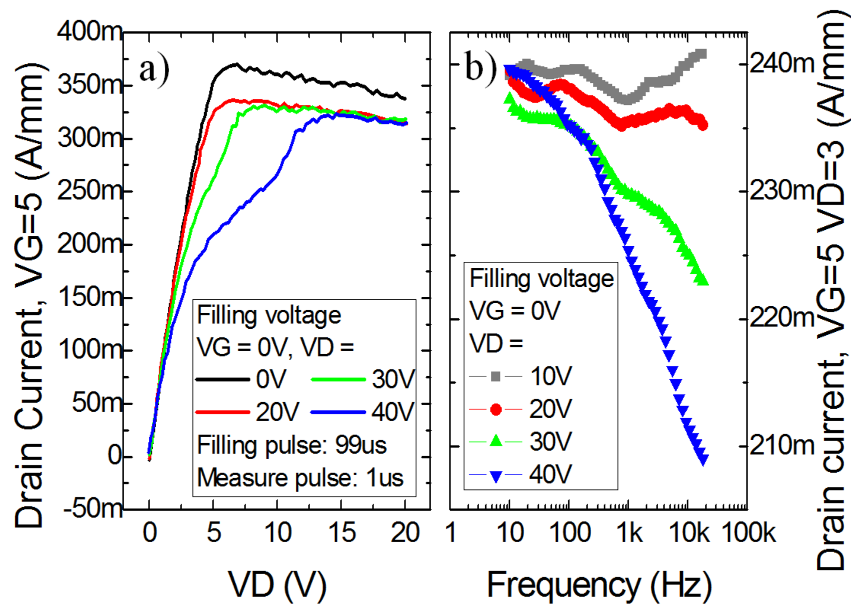


Figure 6.23: Comparison between a) the double pulse response and b) the drain current evaluated during a gate frequency sweep, as a function of the applied drain filling voltage (gate filling voltage = 0 V). The effect of the trapping highlighted by the double pulse test confirms the current variation detected by the GFSs.

The current levels detected by the two different tests are not exactly the same, due to the different duration of the filling and measure phases. The double pulse test is used to detect the effect of the trapping, so it employs a relatively long filling time in order to produce a sensible variation of the characteristics; in our case the filling time and the measure time were respectively 99 μs and 1 μs (1 % duty cycle).

On the other side, the gate frequency sweep has been developed to evaluate the performance of the device in a real switching application, so a 50 % duty cycle is used and the correspondent filling and measure times are equal to half the period of the applied square wave, which means they are not constant but dependent on the measure frequency.

6.4.2 Comparison with other tests

The different duration of the phases is present also when these two techniques are compared to the drain current transients, which typically employ a longer and constant filling time in order to ensure a completely-trapped state and the same initial conditions during the test. The length of the phases has a great influence on results and has to be taken into account, since it can lead to a over- or under-estimation of the device's performances. In the following are described the outcomes of the comparison tests carried out, which are summarized in figure 6.24.

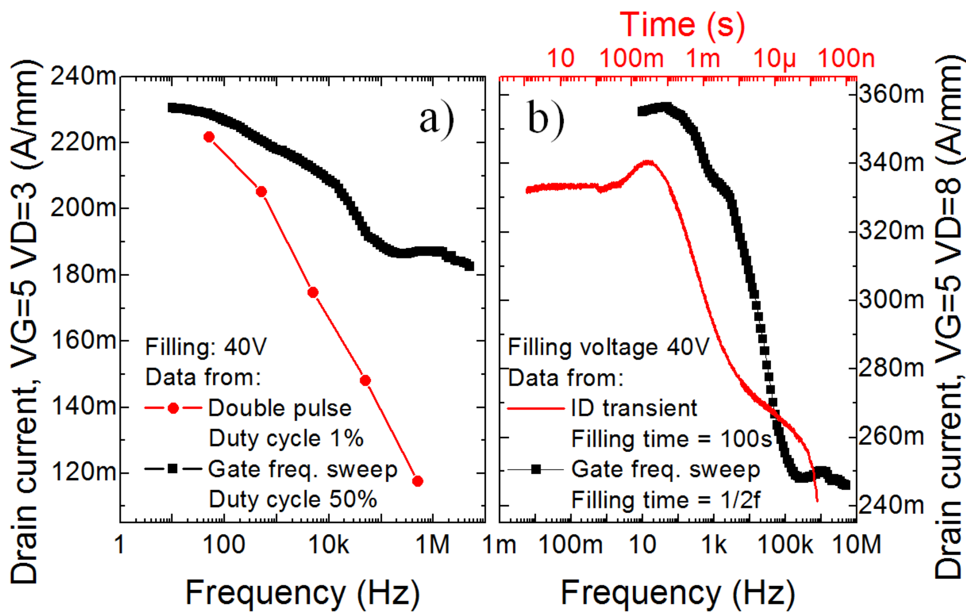


Figure 6.24: Results of the comparison tests carried out with a filling voltage of 0 V at the gate terminal and 40 V at the drain terminal (source grounded) between gate frequency sweeps and a) double pulse characterization, measure VG = 5 V and VD = 3 V or b) drain current transients, measure VG = 5 V and VD = 8 V.

Since the main difference between the double pulse test and the gate frequency sweep is the duty cycle of the applied wave, we have performed a double pulse ex-

periment at different pulse widths and constant duty cycle. The results and the corresponding gate frequency sweep are reported in figure 6.24 a), measured at Vgs = 5 V and Vds = 3 V after a filling bias point Vgs = 0 V and Vds = 40 V. The equivalent frequency of the double pulse has been chosen as half the reciprocal of the pulse width, in order to ensure that points reported in the figure at the same frequency have been measured after the same time has elapsed from the beginning of the measure phase. As can be clearly seen in the figure, the current evaluated by the double pulse is lower than the current from the gate frequency sweep, due to the higher filling time. In a real application, the device will actually have better performances than the values detected by the double pulse test, which in this case underestimates the characteristics of the transistor.

In figure 6.24 b) we can see the comparison between a gate frequency sweep and a drain current transient. The filling bias is the same of the previous experiment, and the device is measured at Vgs = 5 V and Vds = 8 V. In this case the main difference is the filling time, which is constant during the drain current transient (100 s) and varies during the gate frequency sweep: the constant 50 % duty cycle gives a filling time equal to half the reciprocal of the applied square wave frequency. The equivalent frequency of the drain current transient has been chosen according to the same considerations of the previous case, and the figure reports also the equivalent time value for a better understanding of the transient. The overall shape of the sweep is confirmed by the transient, which in turn gives an incorrect estimate of the current flowing through the device under test when used for a switching application due to the long filling period. Moreover, it is difficult to obtain a precise current value at very short times using the drain current transient technique, which typically suffers from a limited bandwidth, whereas the suggested setup allow for a stable output after tens of nanoseconds (see figure 6.22) and an error lower than 1 %, as verified during tests on HEMTs for GHz-band applications (not shown).

6.4.3 Extraction of the activation energy

From the gate frequency sweeps at different temperatures reported in figure 6.22 b) it is possible to obtain the activation energy of the deep level, which was found equal

to 0.25 ± 0.02 eV. The experimental data are reported in figure 6.25, among other deep levels reported in the literature. We have found a good concordance with the data reported in a paper by Polyakov et al. [134]. In that paper the authors report several deep levels found during the analysis of different p-$(Al_x)Ga_{1-x}N$ materials grown on various buffers, as a function of the thickness of the aluminum mole fraction x. Those levels are ascribed to the ionization energy of the magnesium, the element that is typically used in GaN and its alloys as an acceptor in order to obtain p-type conductivity. Since the devices under test employ a p-AlGaN layer under the gate in order to achieve normally-off operation, this is likely to be the location of the deep level responsible for the variation of the performances.

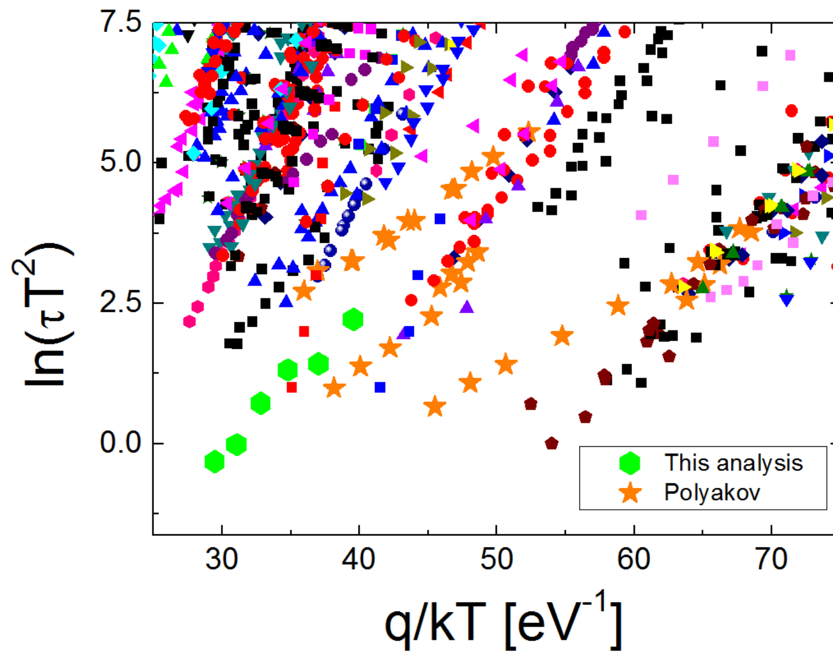


Figure 6.25: Arrhenius plot of the detected deep level among other levels reported in the literature. Highlighted is the relevant paper by Polyakov et al., which reports plots of other deep levels that have been found in p-type GaN alloys.

This hypothesis can be validated by gate frequency sweeps carried out on newer devices with improved epitaxial quality. Figure 6.26 shows the comparison, at a temperature of 40 °C, between the data of figure 6.22 b) and the same test on a upgraded transistor. The current drop at higher frequencies which was originated by the trapping of carriers in the deep level previously detected is not visible, and the same result holds true at different temperatures. The enhancement of the epitaxy

was sufficient for reducing the concentration of the trap states up to a level where the device is not influenced by their presence, and this behavior is consistent with an allowed energy level inside the bandgap situated in the p-AlGaN layer.

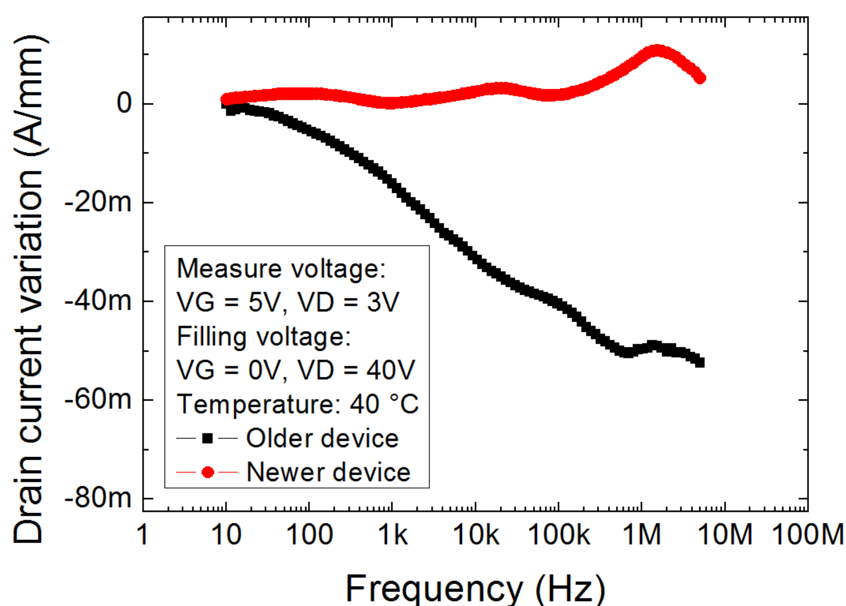


Figure 6.26: Improvement of the characteristics between older and newer devices with improved epitaxial quality. The influence of the deep level responsible for the drop of the current at higher frequencies was successfully reduced below the detection limit.

6.4.4 Conclusions

In summary, in this part we have reported the variation of the performances of a Gate Injection Transistor when used in a real operating condition, as a function of the working frequency. A new type of test, the gate frequency sweep, was suggested to achieve a better understanding of the actual current levels the device will reach in the final application, and this novel experiment was compared to other typical setups, the double pulse and the drain current transient. A deep level at 0.25 ± 0.02 eV, which is likely to be located into the p-AlGaN layer under the gate contact. Newer devices with better epitaxial quality are not affected by its presence.

6.5 Backgating

Backgating measurements are carried out in order to investigate the trapping effects (majority and minority traps) in the device as a response to different substrate biases [142]. Drain current transients are monitored after switching the bulk voltage from ground to negative (or positive) values. The current exhibits an increase when the majority traps are emptied, a decrease when they are filled again. Referring to the band diagram of figure 6.27, when the bulk is biases at a negative voltage V_{BG} the corresponding region of the band diagram rises, causing an overall decrease of the voltage in the substrate up to the channel of the transistor, since the most of the voltage drops in the region near the channel in the direction of the substrate [143]. Since there is this variation, the current suddenly decreases due to the depletion of the channel caused by the local raise of the conduction band. The traps that before were at a lower energy level (and then were filled) start slowly to empty, and the drain current begins to increase thanks to the lower concentration of fixed trapped charge near the channel that causes its depletion.

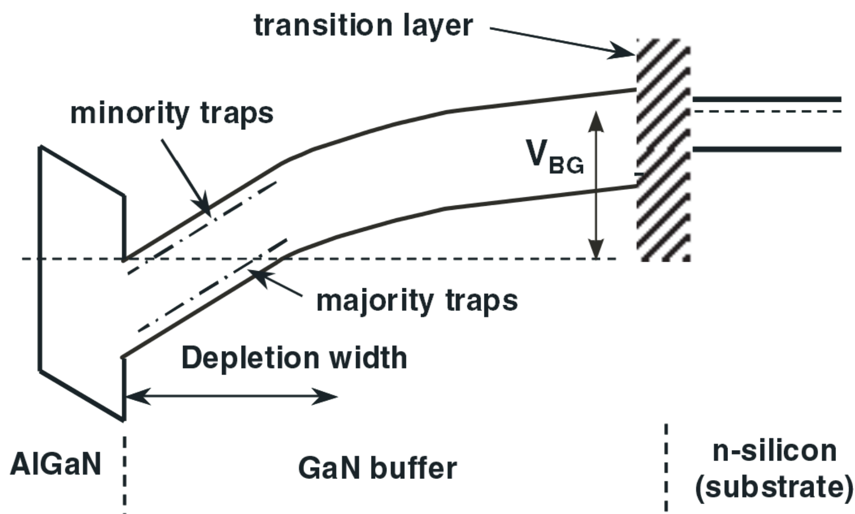


Figure 6.27: Band bending due to backgating [142].

Several experiments were carried out in order to understand the effect of the substrate bias on the performances of the device, and to identify trap states that would be otherwise difficult to detect. The first one was used to find out if a backgating effect exists in the devices under test and which were the best conditions for the

subsequent analysis. The bias values of the test, which was performed following the ideas presented in [142], are summarized in figure 6.28. After 60 second in on-state condition (VG = 5 V, VD = 2 V, source grounded) and no bulk bias, at t = 0 several positive or negative substrate voltages were applied for 500 seconds, and the corresponding drain and gate current transient were recorded. They are reported in figure 6.29. We can see that, when a positive backgating voltage is applied (blue region), there is an initial increase of the drain current due to the bias, followed by a decrease caused by the filling of the traps. Complementarily, when the voltage is negative (red region), at t = 0 the drain current has a lower value and a subsequent increase given by the emission from the traps. If we consider the gate current, we can see that its shape is not easy to understand: this is probably due to the detrapping effect associated with the injection of holes from the gate (see the section about the virtual gate effect reduction when current is injected from the gate at page 150). In order to minimize this effect, all the following experiments have been carried out at VG = 2 V. Moreover, the two phases have been inverted: in the first one the bulk voltage is applied to perturb the device, while in the second one the substrate is kept grounded, so it is possible to have detrapping current transient not influenced by the simultaneous presence of its bias.

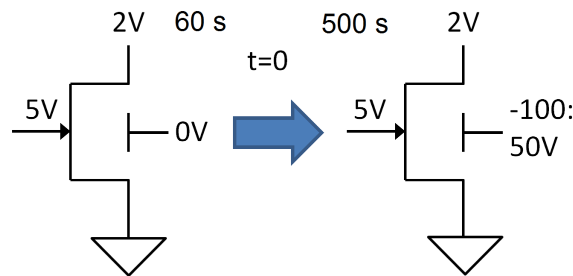


Figure 6.28: Test conditions for detecting the presence of backgating.

In the first experiment the effect of a positive backgating voltage was investigated, the test conditions are described in figure 6.30. The results reported in figure 6.31 detect no evident effect on the currents flowing through the device. the initial decrease of the drain current at lower V_{BG}s is caused by the on-state trapping of states that are filled also at higher V_{BG}, and the gate current is already at its steady-state value.

A different behavior is caused by a negative backgating voltage, as highlighted in

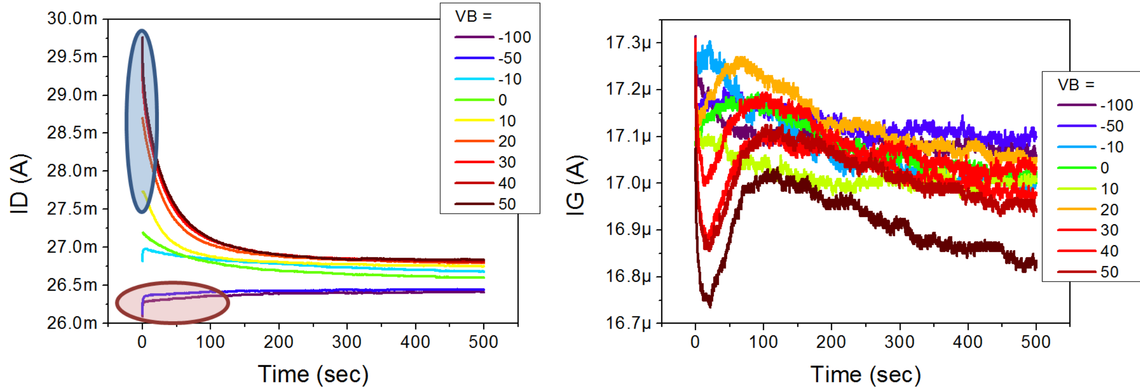


Figure 6.29: Result of the test for detecting the presence of backgating.

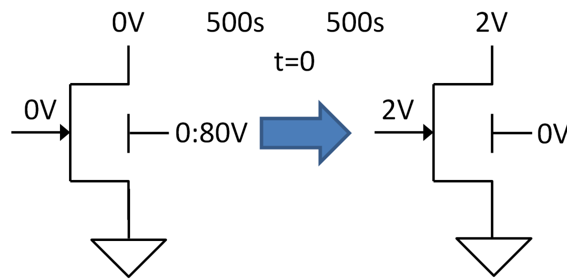


Figure 6.30: Test conditions for positive backgating experiment.

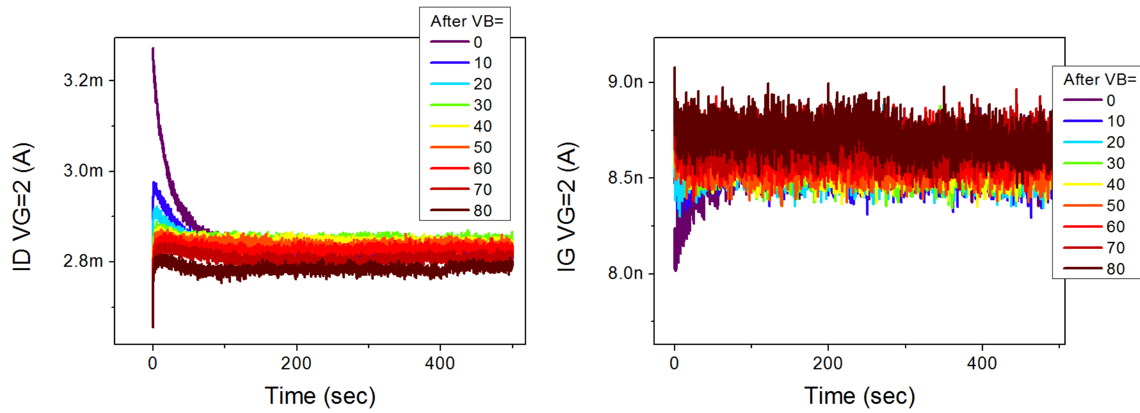


Figure 6.31: Result of the positive backgating experiment.

the subsequent test (conditions in figure 6.32). Figure 6.33 shows a strong decrease of the drain current due to the re-filling of the traps, emptied during the 500 seconds at $V_{BG} < 0$. The lower the bulk voltage the slower the decrease, since the emission is deeper and affects a larger area of the device. Moreover, the gate current reaches its steady-state value more slowly after lower V_{BG}s, an effect that is caused by the longer transitory phase.

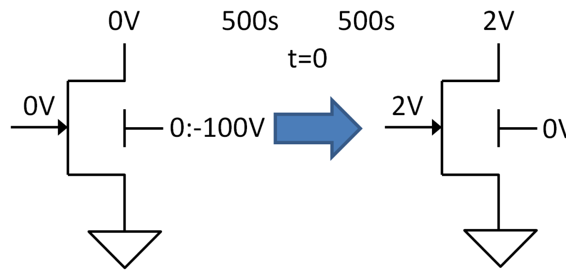


Figure 6.32: Test conditions for negative backgating experiment.

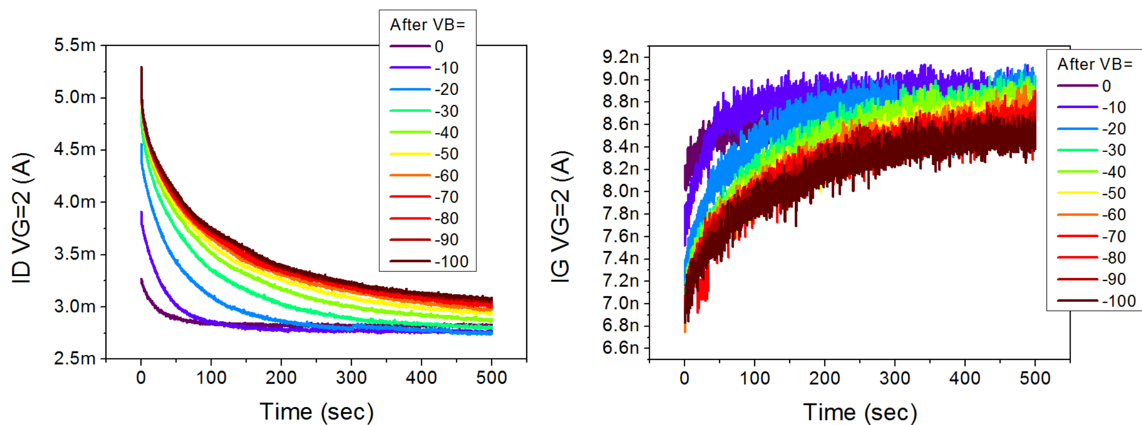


Figure 6.33: Result of the negative backgating experiment.

To find out which region of the device is affected by the trapping and detrapping, the second part of the experiment has been modified: instead of recording the current transients, a quick measurement of the ID - VD (see figure 6.34 (a)) and ID - VG (see figure 6.34 (b)) curve was carried out in order to evaluate the variation of the on-resistance and of the threshold voltage. The results are reported in figure 6.35: a negative V_{BG} = -40 V is enough to produce a strong improvement of the on-resistance, but causes also a reduction of the threshold voltage. Over rest time,

the characteristics slowly return to the same value they had before the test: the backgating voltage doesn't cause a permanent degradation of the device.

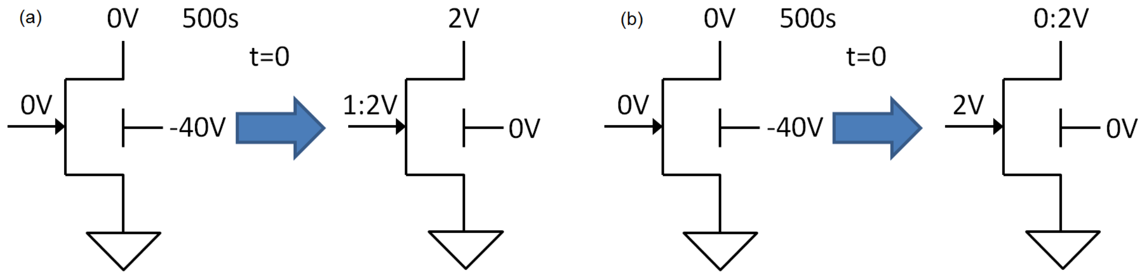


Figure 6.34: Test conditions for (a) Vth and (b) Ron backgating experiment.

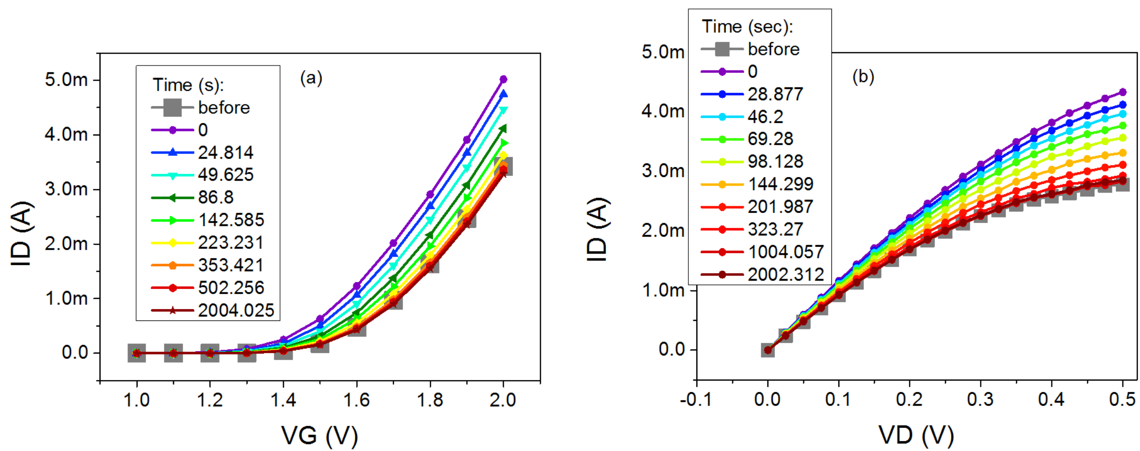


Figure 6.35: Result of the (a) Vth and (b) Ron backgating experiment.

In figure 6.36 the variation of the estimated Ron and Vth are compared as a function of the time after the turn-off of the bulk voltage. The two kinetics are well correlated and are described by similar time constants, so it is possible to say that the defect responsible for the change of the performances is located inside the whole material.

Thanks to the good level of detail of these transient, and to the fact that they are not influenced by the presence of a substrate bias, it is possible to repeat these experiments at various temperatures in order to find the activation energy of the process. The chosen bias values and temperature range are summarized in figure 6.37, while the results are shown in figure 6.38 (a). The temperature accelerates the drain current transient, due to the faster trapping of the carriers. With those data

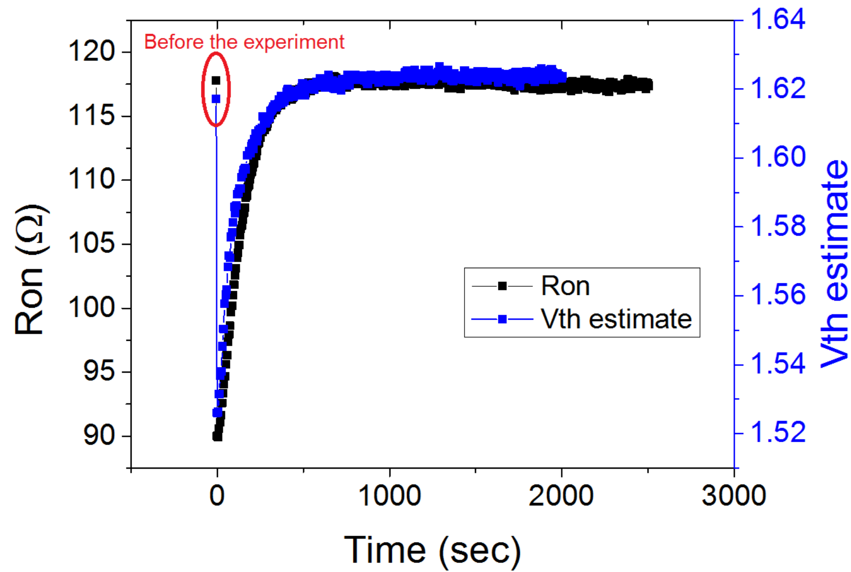


Figure 6.36: Comparison between the results of the Vth and Ron backgating experiment.

it is possible to create the Arrhenius plot of the process, reported in figure 6.38 (b), which was found to have an activation energy of 0.51 eV.

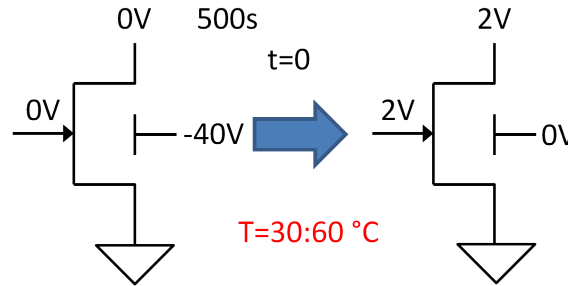


Figure 6.37: Test conditions for the temperature backgating experiment.

The Arrhenius plot can be compared with other data reported in the literature (see figure 6.39). While Tanaka et al. [144] and Meneghini et al. [135] were probably able to detect this same level in GITs, they couldn't distinguish if it was located in the barrier or in the bulk nearby the channel, a differentiation that is possible to have using backgating experiments. In the figure are highlighted also other results obtained by Marso et al. [145] using the backgating technique and by Honda et al. [146] on carbon-doped n-GaN, which may be the possible origin of this defect.

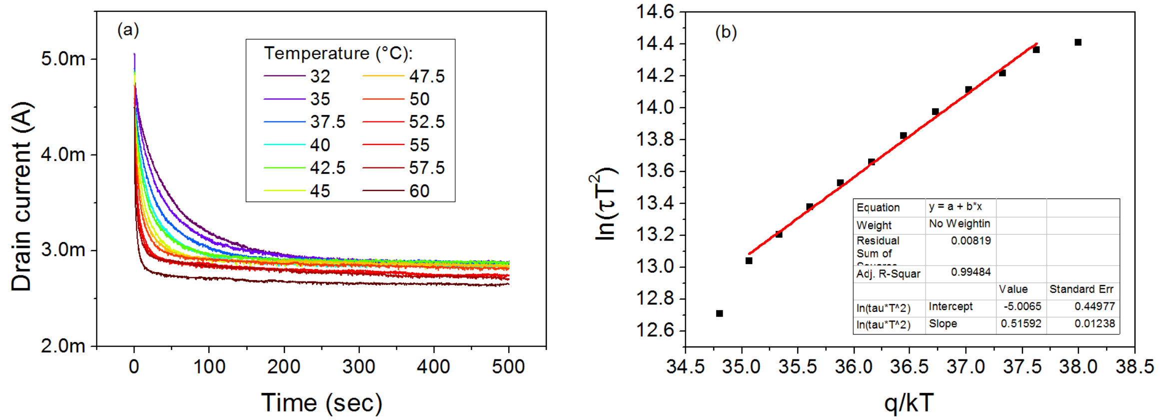


Figure 6.38: Result of the temperature backgating experiment (a) and corresponding Arrhenius plot (b).

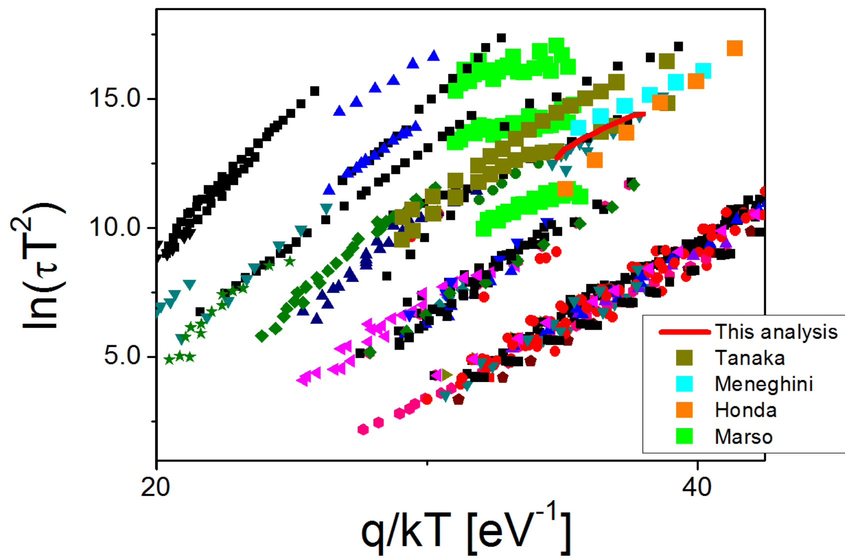


Figure 6.39: Comparison between relevant papers.

6.6 Constant bias stresses

Previous tests have highlighted the most important cause for the degradation of GITs during their typical operation: the reliability of the gate - source diode. This problem comes from the intrinsic structure of this transistors, which are able to inject moderate currents from the gate to the channel when in on-state condition. The majority of the carriers flow to the source, since this is the region of the device with the lowest potential. In order to check if the problem was solved with the newer iterations of the technological process, several stresses were carried out on the gate - source diode, both in constant current and constant voltage condition.

6.6.1 Constant current stress

The samples under test were Gate Injection Transistors of different families (PD4-5-6-7-8). The gate-drain distance of the chosen devices is 7.5 μm. Was applied a constant gate current IG = 1 mA (10 mA/mm) with drain floating and source grounded for up to 250 minutes. After each stress step, a complete characterization of the device was carried out. Figure 6.40 reports the typical modifications of the gate diode of tested devices over stress time. The results are aggregated in figure 6.41 for easier comparison. Newer devices are found to have an increase of the reverse current of the gate diode which is orders of magnitude different from the older devices, and this stability can vastly improve the reliability of the transistors during their typical operation.

A very interesting effect has been found in some of the older devices during the stress: the activation of the p-type dopant. Since this is an effect that has been pointed out also in the characterization of the optoelectronic devices (see the part about the dopant activation in laser diodes at page 137), it confirms the assumption that is important to study a material in all its possible application (and not focusing only one specific device type), because we can gain useful information in a field thanks to the results obtained in another one. As has already been said in the cited part, Mg atoms may remain in an interstitial unactivated position inside the lattice, and become activated moving in a substitutional position due to the flow of minority carriers. If we consider the second peak of the transconductance, labeled as P2 in

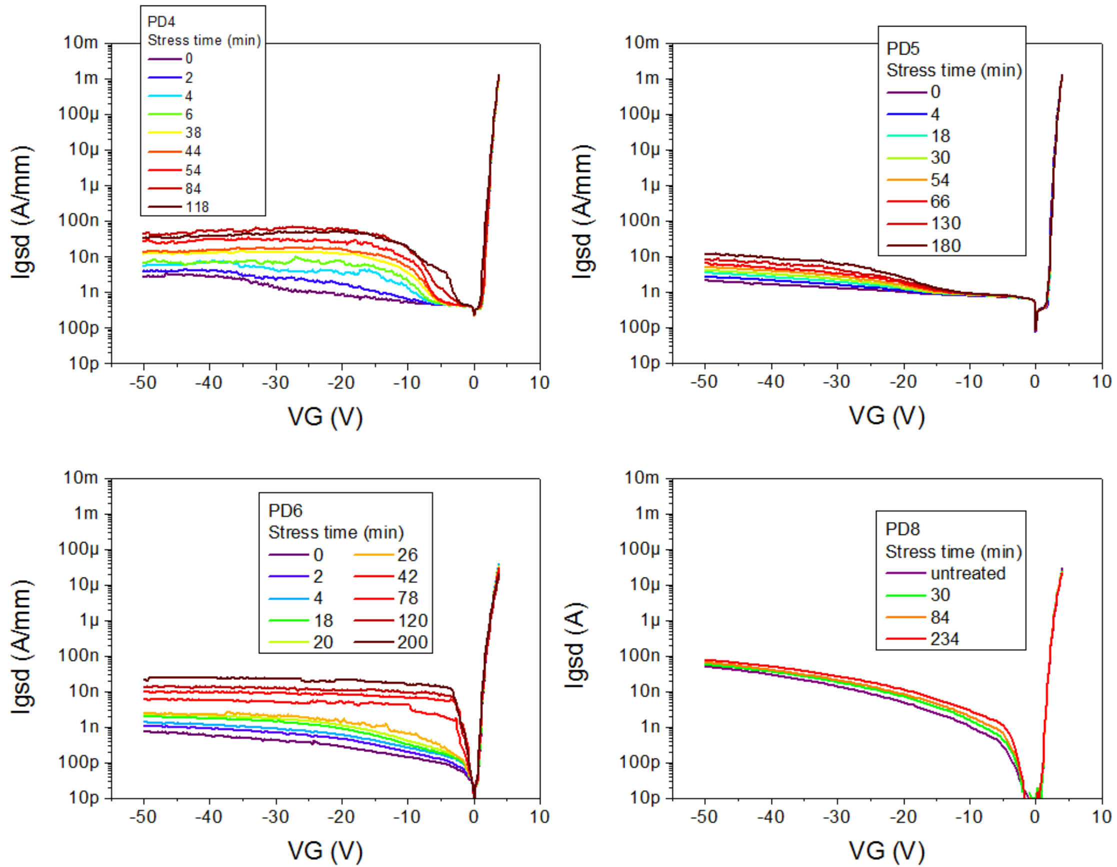


Figure 6.40: Gate diode variation over constant current stress time.

figure 6.42 (a), we know that it is a consequence of the hole injection from the p-type layer to the channel, so its magnitude is an indication of the quantity of holes present in the p-AlGaN that are subsequently injected into the channel. The increase of the second transconductance peak reported in the figure can then be caused by an increased p-type dopant activation. This hypothesis is confirmed by the relationship highlighted in figure 6.42 (b) between two parameters:

- the ratio between the amplitude of the transconductance peak related to the hole injection and of the main transconductance peak. This ratio is necessary in order to (somehow) take into account the fact that the modifications of P2 can also be due to the degradation of the transistor (which affects also P1) and not only to the increased hole concentration;

- the electroluminescence of the forward-biased gate diode. It is important to

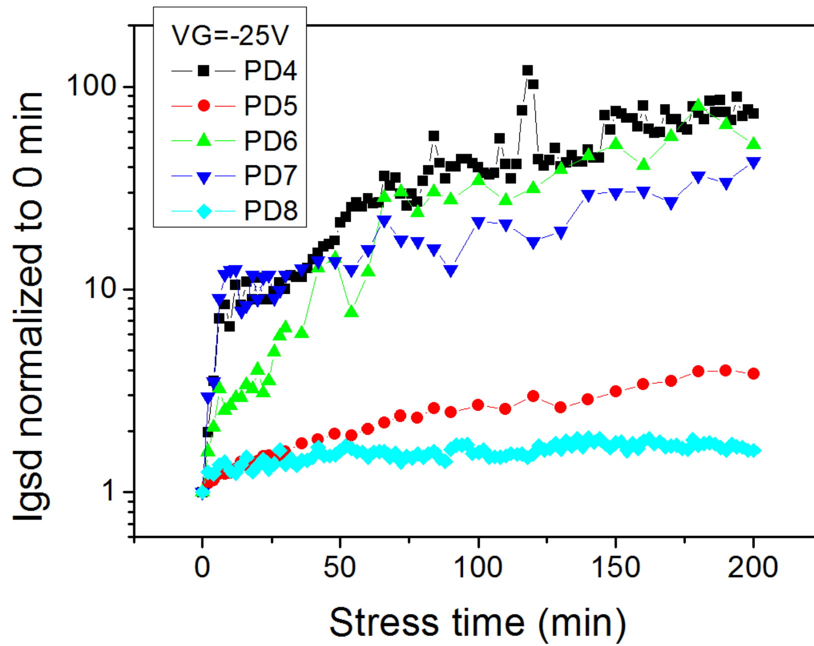


Figure 6.41: Comparison of the gate diode degradation between different devices, constant current stress.

point out that the emission of light in this condition is due to the band to band recombination of the holes injected by the gate with the electrons of the channel [147].

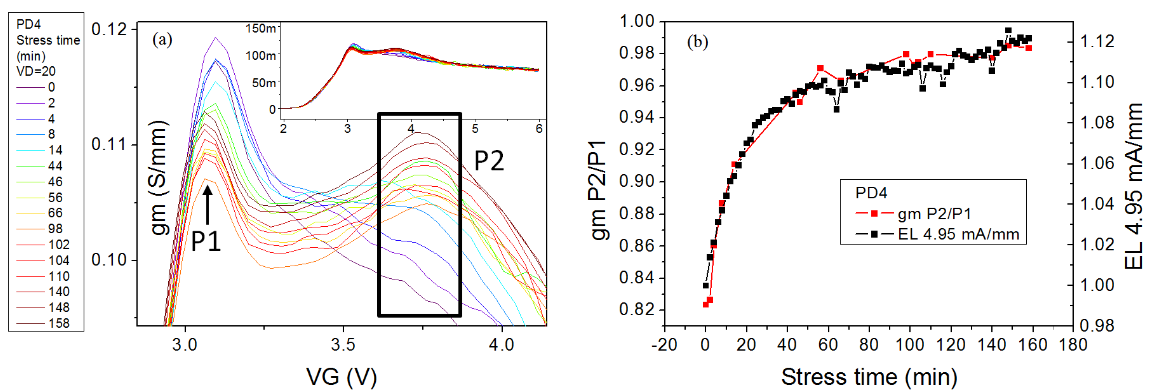


Figure 6.42: Variation of the transconductance peaks (a) and the correlation of their ratio with the electroluminescence (b) over stress time.

It is important to point out that, in figure 6.41, devices from an intermediate family (PD5) were found to have a lower degradation compared to newer devices (such as PD6 and PD7). this is due to the peculiar composition of the gate stack,

which allows a lower gate voltage at the same stress current. The voltages reached by the devices during the stress are reported in figure 6.43. In order to have a fair comparison between different iterations of the technological process, constant voltage stresses have been carried out.

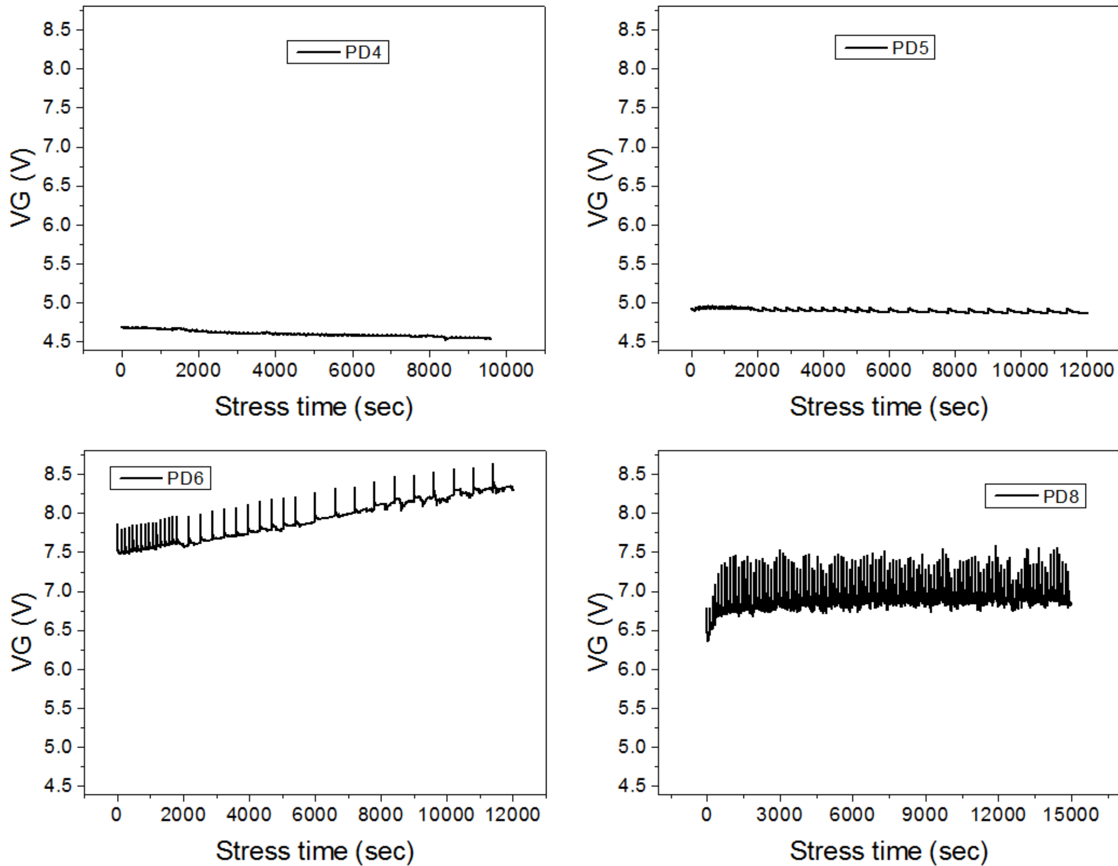


Figure 6.43: Gate voltage during constant current stress time.

6.6.2 Constant voltage stress

In this case, the devices under test have the same characteristics and dimensions of the previous experiment, and they were submitted to a constant VGS = 5 V while the drain was kept floating. The typical gate diodes are shown in figure 6.44, and their comparison in figure 6.45. In this case the increase of the reliability due to the improvements of the technological process is clearly visible and not biased by the different conductivities of the gate stacks.

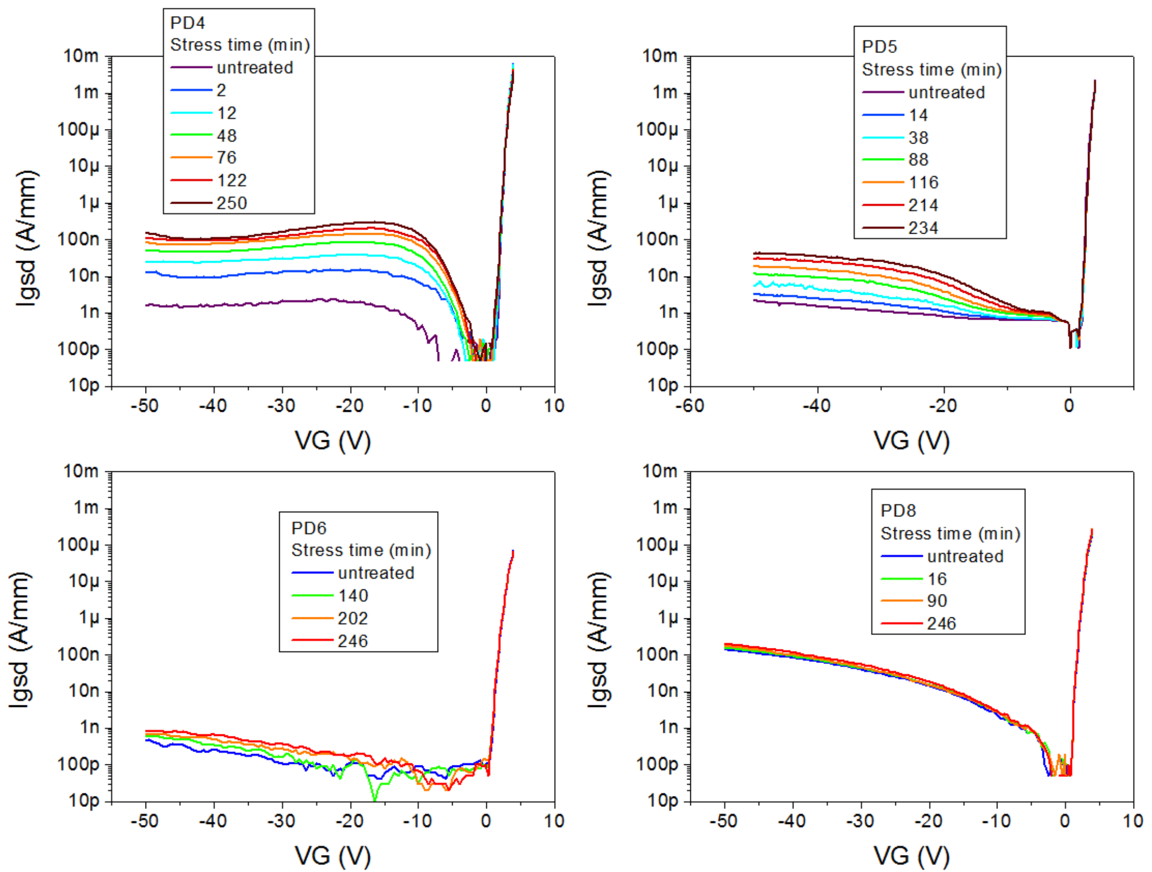


Figure 6.44: Gate diode variation over constant voltage stress time.

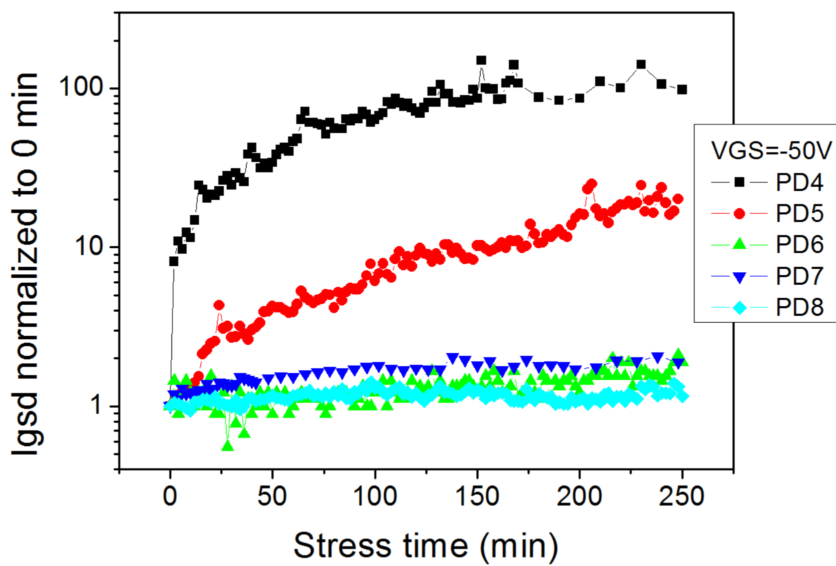


Figure 6.45: Comparison of the gate diode degradation between different devices, constant voltage stress.

An effect that has been found during this stresses on older devices is a strong variation of the evaluated threshold voltage, estimated as the gate voltage that produces a drain current equal to 1 mA/mm at VD = 10 V (i. e. from the ID-VG curve), while the threshold voltage remains very stable for the newer devices (see figure 6.46 (b)). This is due to a strong increase of the sub-threshold current, reported in figure 6.46 (a) with the current limit for the threshold voltage estimation.

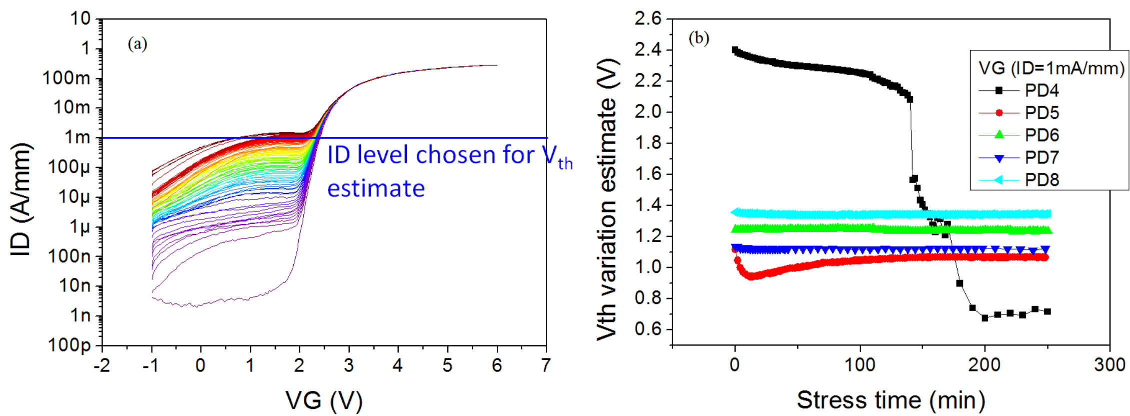


Figure 6.46: Subthreshold current variation (a) and its effect on the estimate of the threshold voltage over constant voltage stress time (b).

6.7 Breakdown and field plates

Gate injection transistor are able to withstand very high breakdown voltages (up to 800V, [87]), suitable for high power electronics. For this reason it is necessary to have a deep understanding of which kind of mechanisms could limit the performances and the reliability of those devices when submitted to high gate - drain and source - drain electric fields. Their dynamic characteristics, as said at page 87 can be further improved through the adoption of a field plate (FP, see figure 6.47) [148]. This design reduces the electric field peak, thus reducing trapping phenomena and current collapse. The aim of this part is to analyze how GIT structures react to high electric fields: the study is based on pulsed electrical characterization and breakdown tests. The typical structure of these samples employs a p-AlGaN layer under the gate, to lift the potential at the interface with the active region providing a normally-off operation. Moreover, the injection of holes from this layer at high gate voltages

enables conductivity modulation, increasing the maximum drain current [87]. The gate region is composed by an intrinsic AlGaN layer, followed by a thick i-GaN zone (see figure 6.47 (a)). The formation of the 2DEG occurs at the interface between these two materials, and the AlGaN-GaN heterojunction prevents the injection of electron from the channel to the p-AlGaN. The GITs are grown on a Si substrate, with buffer layers composed of GaN/AlN multilayers over initial AlGaN/AlN layers. The transistors under analysis can be grouped into two main categories: (a) without and (b) with field plate (see figure 6.47). The gate width is 100 μm and the gate - source spacing is 1.5 μm for both structures. Were studied devices with several gate-drain distances (Lgd) and no field plate, and devices with fixed Lgd = 10 μm and different field plate lengths (Lsfp). The various lengths combinations for the analyzed samples are summarized in table 6.2.

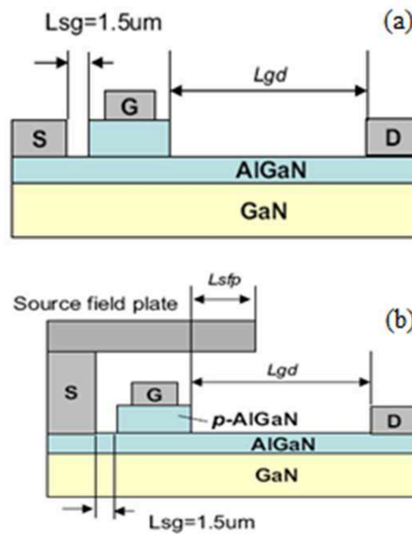


Figure 6.47: Structure of the devices under test, without (a) and with (b) field plate.

6.7.1 Electrical characterization

In order to analyze the response of the devices to trapping mechanisms, an extensive pulsed electrical characterization was carried out, starting from different quiescent bias points (VGS = 0 V, VDS in the range 20 - 30 V). Measurements were performed using short (1 μs) pulses, while quiescent (trapping) bias was applied for 99 μs for each measurement point. Output characteristics were measured for VDS

Sample	**Lgd** (μm)	**Lsfp** (μm)
A	2	0
B	5	0
C	7.5	0
D	10	0
E	10	3
F	10	5

Table 6.2: Size of the devices under test. For all devices W = 100 μm and Lsg = 1.5 μm.

levels in the range 0 - 20 V, and with VGS levels in the range 1 - 6 V. From the comparison between the various quiescent bias points, it is possible to evaluate the response of the drain current to the applied trapping voltage. The current collapse can be calculated as

$$CC = \frac{ID_{(0,0)}VD^* - ID_{(0,QBPmax)}VD^*}{ID_{(0,0)}VD^*}$$

where $QBPmax$ is the maximum quiescent bias point (30 V), $ID_{(a,b)}(V)$ is the drain current evaluated at the quiescent bias point (VGS = a, VDS = b) and pulse bias (VGS = 6 V, VDS = V), VD^* is the drain - source voltage that maximizes the numerator.

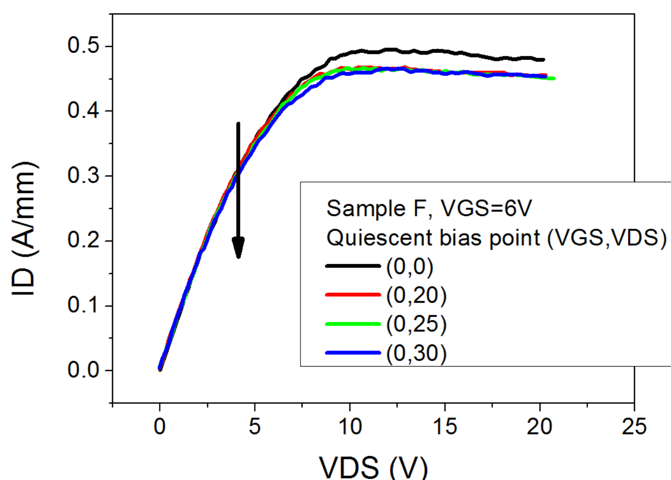


Figure 6.48: Pulsed output curves (pulse width: 1 μs, duty cycle 1%) of a device with Lgd =10 μm and Lsfp = 5 μm under different quiescent bias points, at VGS = 6 V.

Figure 6.48 reports representative output characteristics, measured starting from different quiescent bias points. Measurements were obtained on devices of series F

(see table 6.2 for details on device structure). GITs show almost no current collapse up to drain trapping voltages of 30 V, only a decrease in the current saturation value due to a slight threshold shift (not shown). The comparison between the various structures (no field plate, short field plate and long field plate) is reported in figure 6.49, by means of a comparison of their current collapse values. Longer field plates allow a reduction of the current collapse, thanks to the decreased peak electric field and the subsequently reduced trapping.

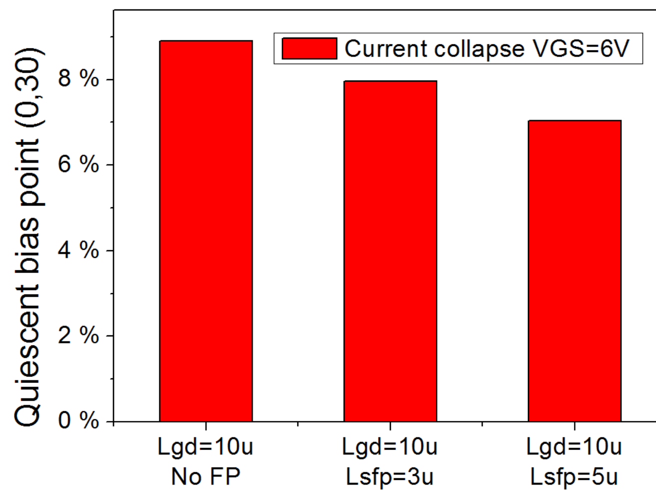


Figure 6.49: Maximum current collapse at quiescent bias point VGS = 0 V, VDS = 30 V, evaluated at VGS = 6 V. Comparison between three different structures: without field-plate, short field plate (3 μm), long field plate (5 μm).

6.7.2 Stress tests

To obtain additional knowledge on the mechanisms related to high drain-source fields in off-state condition, the devices were submitted to step-stress with high gate-drain voltage levels. With VGS fixed at 0 V (off-state) and the source terminal grounded, the transistors were kept at a constant VDS for 10 minutes. The VDS value was then increased, from 300 V until catastrophic breakdown with steps of 50 V (from 100 V, step 25 V for type A). After each step the gate diode, output characteristics and transconductance were measured to monitor the degradation of the samples. In figure 6.50 are shown the typical degradation kinetics of one of the analyzed GITs submitted to the step-stress experiment. At each stage, drain current

increases both due to the variation in the stress voltage level, and to a degradation of the gate - drain diode (see also figure 6.51). It is worth noticing that the noise superimposed to drain current increases during stress time: this is usually considered as a signature of the generation of defects under or close to the gate (see page 90).

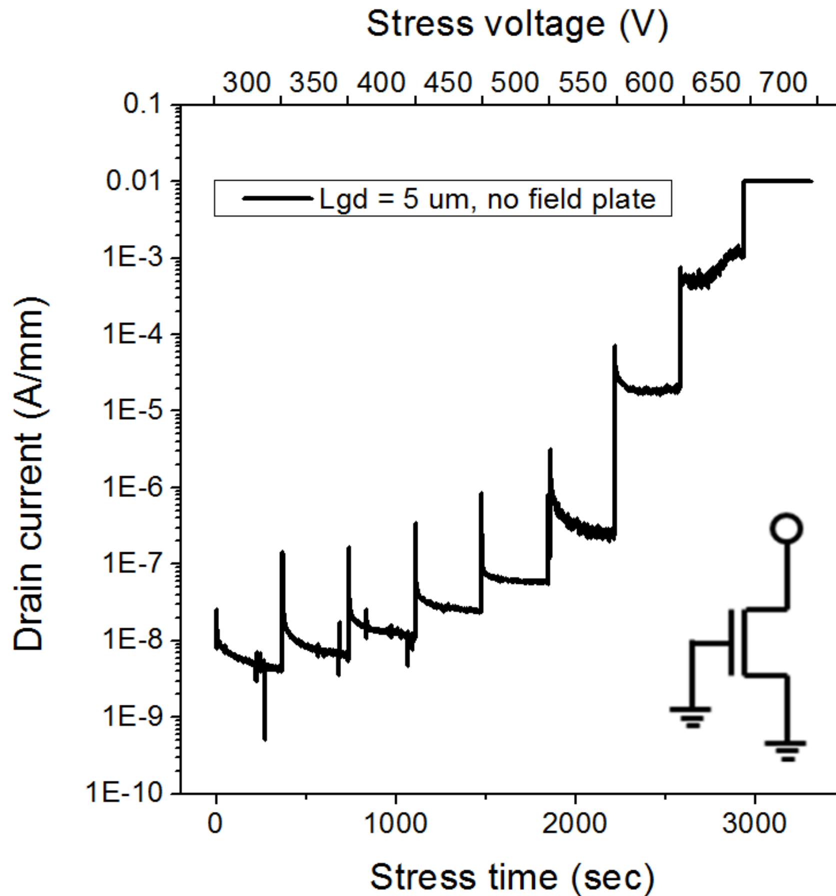


Figure 6.50: Drain current increase over stress time consequent to the applied stress voltage, source and gate grounded. Sample type B.

In figure 6.51 is reported the current - voltage characteristics measured at the gate - drain diode before and during the stress of the same device. Stress induces a significant increase in the gate leakage current, indicating the generation of parasitic leakage paths, generated by the high applied electric field. It is worth noticing that the leakage current increase occurs only after the 600 V stage of the step-stress experiments: this indicate that GITs with a Lgd of 5 μm can withstand a gate-drain voltage of 600 V without showing any significant degradation.

The effects of stress are visible also in the drain current vs gate voltage charac-

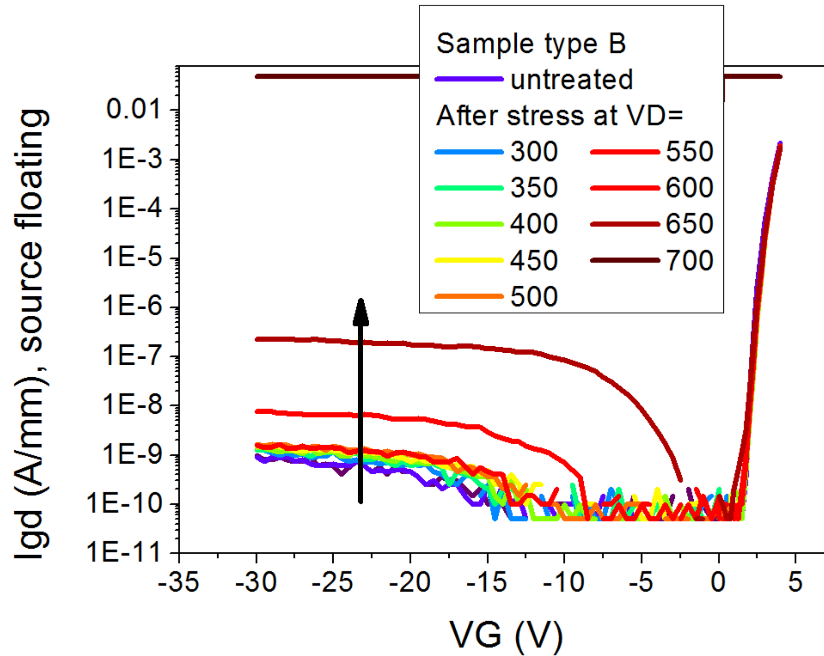


Figure 6.51: Current-voltage curve of the gate-drain diode (source floating) after each stress step. Type B transistor.

teristics (see, in figure 6.52, the curves measured with VDS = 20 V). The increase of the current at lower VG levels follows the one reported about the gate diode and is explained by the same phenomenon. The threshold voltage remains stable during the stress test, confirming the stability of the gate injection transistor structure even at very high electric fields.

6.7.3 Electroluminescence maps

As can be seen in figure 6.54, the formation of defects over the stressed region can also be inferred from near-field spatially-resolved electroluminescence maps. It was found an increase over stress time of the number of emitting spots and of the intensity of the luminescence, produced by the strong electric field localized where the defect concentration is higher.

6.7.4 Failure voltage

To summarize the results of the breakdown tests, it is useful to analyze the relationship between the catastrophic failure voltage and the gate-drain distance for

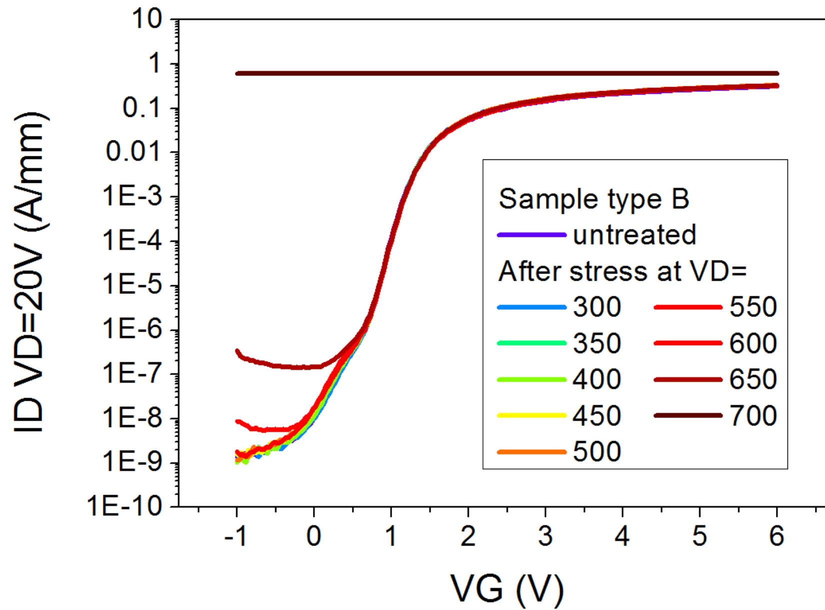


Figure 6.52: Relationship between drain current and applied gate voltage at VD = 20 V and VS = 0 V after each stress step. Sample type B.

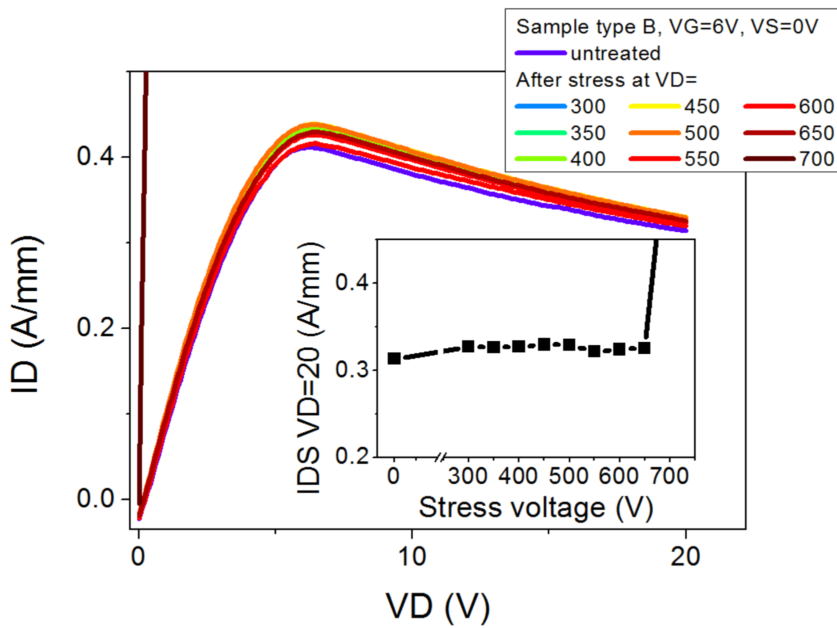


Figure 6.53: Drain current as a function of the drain - source voltage, measured at VGS = 6 V after each stress step. The inset reports the variation at VDS = 20 V.

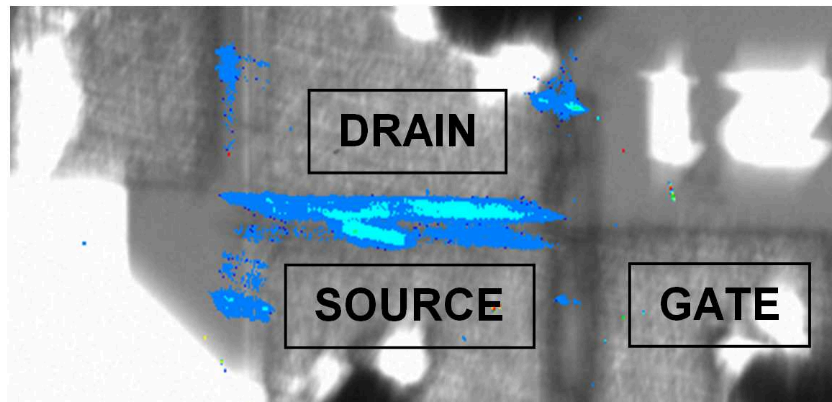


Figure 6.54: False colors electroluminescence map of a device under stress at VDS = 800 V, VGS = 0 V. No perfect focalization due to insulation using Fluorinert.

devices without field plate, and with field plate (also as a function of the spacing between field plate and drain (Lfpd). Figure 6.55 reports the results of this analysis. Results demonstrate that GITs with a Lgd of 10 μm can withstand a voltage of 1100 V without showing any degradation. Power electronics typically employs devices with large size, due to the higher power they are able to withstand, so GITs are good candidates for this field of applications. A linear relation between gate - drain spacing and breakdown voltage is found for the analyzed devices. Moreover, the presence of a field plate doesn't seem to lower the robustness of the transistor: the comparison is done between samples (without field plate) with the gate-drain distance equal to the spacing between field plate and drain (for devices with field plate). This behavior seems to disagree with the typical idea that the presence of a field plate increases the performances and the reliability of a device thanks to the reduction of the peak electric field ([149, 150]). The reduction of the breakdown voltage with longer field plates has already been identified by other groups ([151, 152]), even if this relationship and the underlying cause has not always been clearly stated.

6.7.5 Conclusions

To summarize, by means of pulsed electrical measurements and breakdown tests, the performance and reliability of devices with various gate - drain spacing and field plate lengths were analyzed, finding that:

- before stress, trapping is very small and the use of a field plate effectively

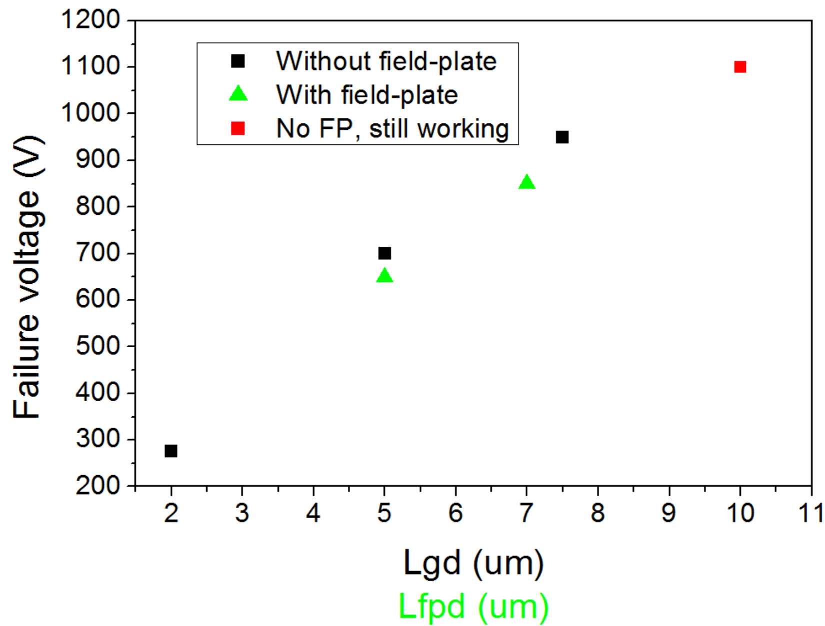


Figure 6.55: Catastrophic failure voltage as a function of the distance between gate and drain (for devices without field plate) or between field plate edge and drain (for devices with field plate). Stress performed on drain terminal, source and gate grounded (off-state) for 10 minutes each step.

reduces the current collapse due to trapping;

- the off-state stress causes an increase of the concentration of defects in the region close to the gate, resulting in higher gate leakage components, and in an increased noise superimposed to the gate current;
- there is a critical stress voltage, that triggers the catastrophic breakdown of the device, due to the very high applied field.

Breakdown voltage is found to have a linear dependence on the gate - drain spacing. For devices with field plate, a similar dependence is found for the spacing between field plate and drain. Devices with a gate - drain spacing of 10 μm can withstand a stress voltage level of 1100 V, without any catastrophic failure. Thanks to a field plate configuration it is possible to reduce the trapping effects responsible of the current collapse, achieving better static and dynamic performances. Moreover, the addition of a source field plate has no evident negative effect on the reliability of the transistor respect to devices with similar maximum electric fields. All these results

suggest that GITs are suitable for high power electronics applications, and that their performances can still be enhanced by smart design without being detrimental to their best operating features.

6.8 Step-stresses

This part will describe only the results of the on-state step-stresses on GITs. An example of off-state step stress has already been given in the part about breakdown and field plates (the previous section at page 182) for devices of one of the first iterations of the technological process (PD5). Anyway, newer devices have shown similar performances in terms of degradation and reliability (see figure 6.56). Step-stresses are typically useful to find out if a critical voltage for the degradation exists, if the degradation is gradual or abrupt and to find out what changes are induced by an increasing bias. The experiment consists on fixing the bias voltage (or current) on all but one terminal of the device, and on increasing its bias value up to a chosen point or to the catastrophic failure of the device. In this case, the source was grounded and the gate kept at 6 V, on-state value for the devices under test, while the drain voltage was increased from 10 V with a 5 V step until device failure. The duration of each step was 120 seconds, and at each step the main characteristics of the devices were checked. All the devices under test have Lgd = 10 μm.

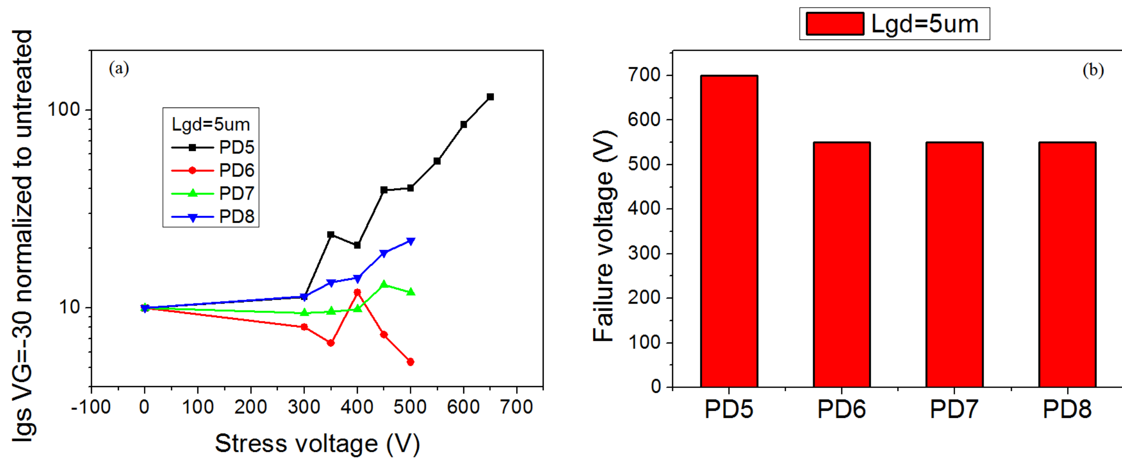


Figure 6.56: Results of the off-state step-stresses: (a) reverse gate diode current and (b) failure voltage of devices with the same dimensions (Lgd = 5 μm) belonging to different iterations of the technological process.

6.8.1 Degradation kinetics

For this analysis the gate diode current will be used as a comparison element between the different iterations of the technological process, since this is a critical design point for a HEMT and in particular for a Gate Injection Transistor, due to the high values that its current can reach during the operation. Figures 6.57 and 6.58 report some of the results on a, respectively, older (PD5) and newer (PD8) device:

- the drain current during the stress;
- the gate current during the stress;
- the overall shape of the diode characteristic at the various steps;
- its kinetic evaluated at VG = -10 V.

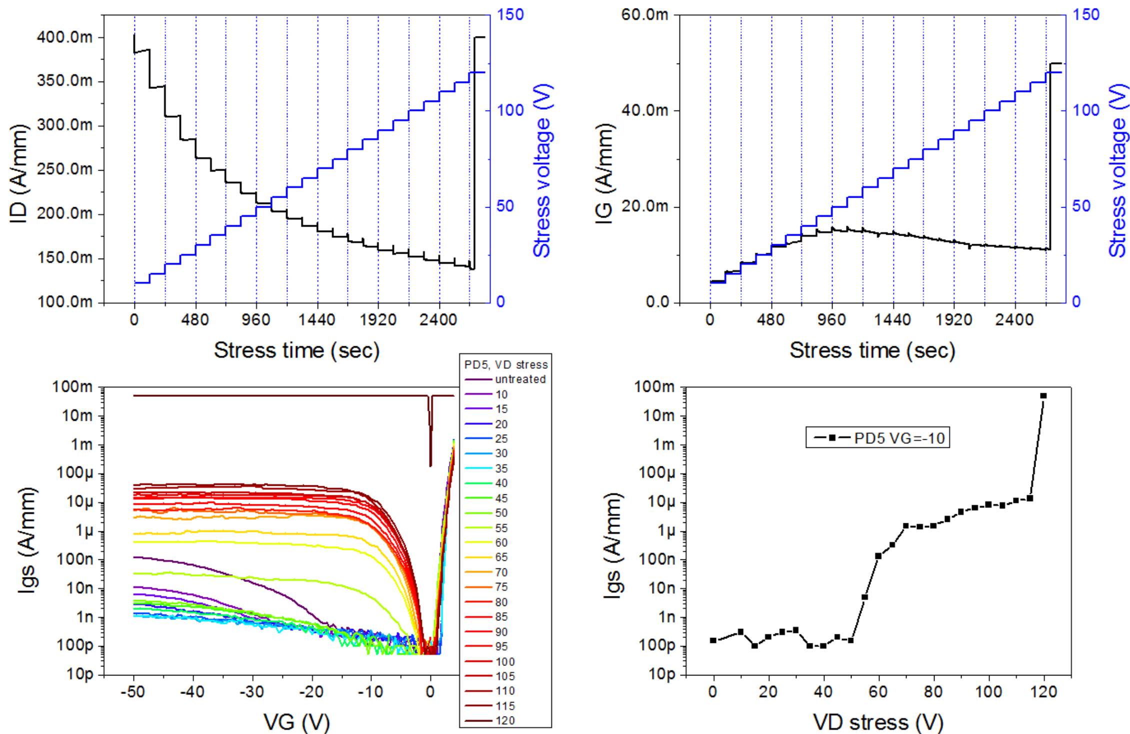


Figure 6.57: Results of the on-state step-stress of a older device.

The drain current decreases during the stress due to the increased drain voltage, which causes higher on-state trapping and higher power dissipation. The reverse current of the gate diode grows, an effect that is caused by the damages induced in the

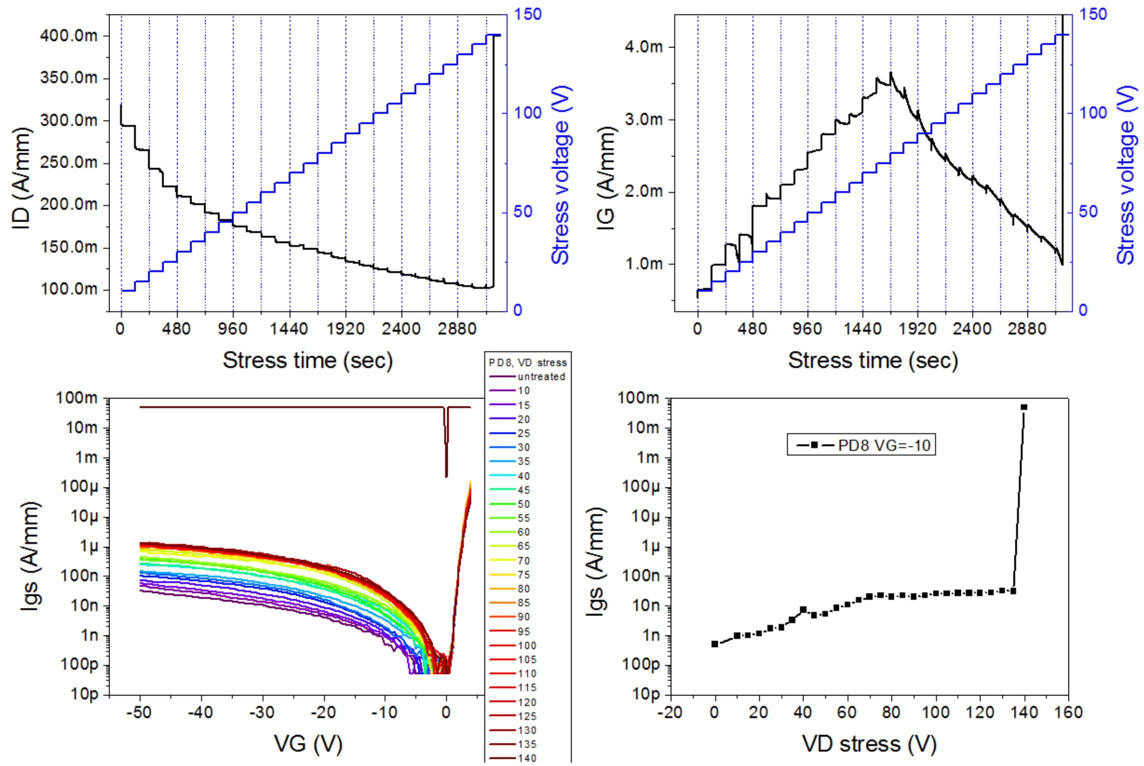


Figure 6.58: Results of the on-state step-stress of a newer device.

lattice of the device by the gate - drain field and by the flow of highly energetic carriers into the channel. These defects behave as parasitic conductive paths, enhancing the leakage current. As can be seen comparing the graphs, newer devices are affected by a reduced swing of the current between the untreated and the before - failure curve, and have a lower absolute value of the current before the catastrophic deterioration. A more extensive comparison between the different iterations of the technological process is reported in figure 6.59, where are described also the results on devices with different field-plate lengths (Lsfp is the distance between the edge of the p-AlGaN ant the edge of the field-plate, see figure 6.47). The use of a field-plate seems to reduce the degradation of the gate diode, but causes a lower catastrophic voltage, probably due to the lower distance between its edge and the drain electrode. Newer devices have a lower degradation, which confirm the improvements of the growth of the devices, and an higher failure voltage.

In the case of devices older than the ones tested in this thesis, the degradation was found to be dependent on the power dissipated by the device, rather than on the

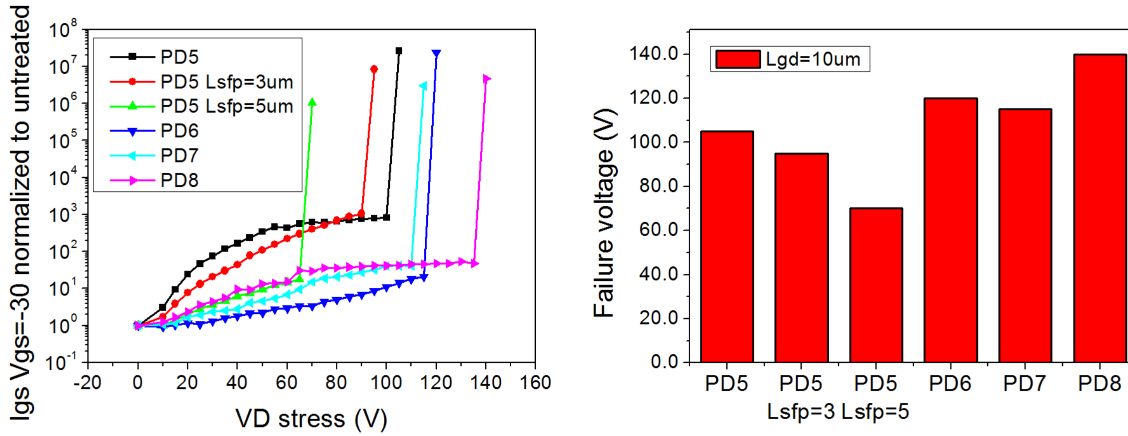


Figure 6.59: Comparison of the results of on-state step-stresses on different device families.

imposed voltage. In order to check this possibility, the same experiment was carried out on one of the older devices (PD5) not at the open air but inside Fluorinert, an electrical insulator with better characteristics of thermal transport. The thermal conductivity of the common air is 0.0257 W/m°C, while the Fluorinert one is 0.066 W/m°C. As can be seen in figure 6.60, Fluorinert causes an increase of the failure voltage, which ranges from the 105 V of the older devices to the 140 V of the newer ones. But when the dissipated power is taken into account, we can see that all the devices fail in a very limited power range (maximum variation ± 2 %), while the better thermal conduction provided by the Fluorinert gives an increase near to 20 %. Then, failure seems to be related to power dissipation rather than to the applied voltage.

6.8.2 Pulsed response

Since the creation of defects has been identified as a possible cause of the degradation of the devices, pulsed characterization has been carried out in order to detect this increase of the concentration of defects. Every 30 V increase of the stress voltage, a complete ID - VD analysis was performed on the device at different drain quiescent bias points, up to 100 V, in off-state condition (VG = 0 V). In this case, the curve was detected after 2.5 μs of a 5 μs measure pulse, and the filling pulse was 500 μs long. As can be seen in figure 6.61, the current collapse increases during the stress, an

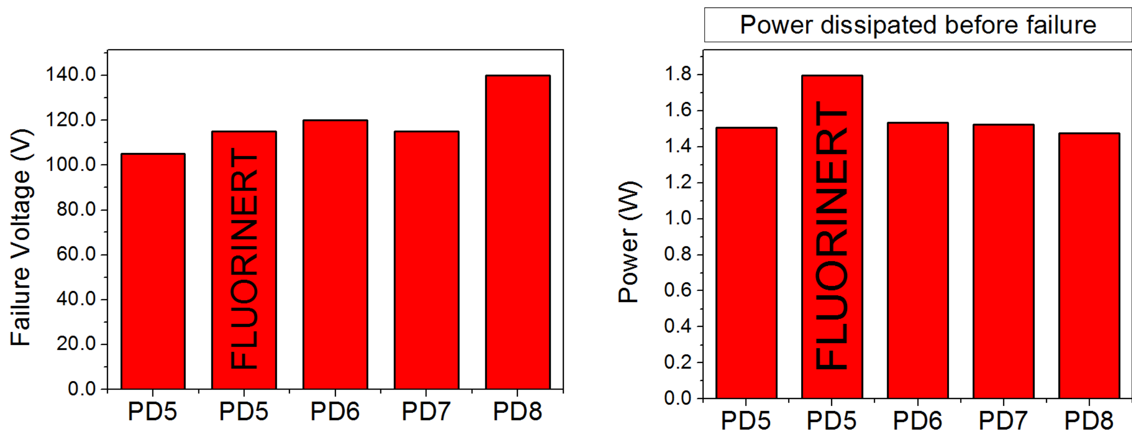


Figure 6.60: Dependence of failure on voltage and dissipated power.

indication of the higher number of defects present inside the device, which reduce the dynamic performances of the transistor. The same behavior was difficult to detect in the case of newer devices, since the very low current dispersion make it difficult to identify a reliable trend (figure 6.62).

The comparison between the maximum current collapses at the various steps is reported in figure 6.63 for both devices. In the case of older transistor there is an increase of nearly 25 % of its value, while for PD8 the variation is ± 4 %, a very low value that confirms the difficulty of obtaining a monotonic trend (given the limited sensitivity of the experimental setup), but testifies the good quality of the devices: they are not influenced by a significative reduction of the dynamic performances even after being stressed at a drain voltage of 120 V (a value that is often enough to cause the catastrophic failure of other devices in **off-state**) in **on-state**.

6.8.3 PD10

Since PD10 devices have a gate - drain distance that is one order of magnitude lower than the previous iterations of the technological process due to a steep scaling, their performances and reliability when submitted to a step-stress experiment are not comparable to the older transistors, and the results obtained are presented in a separate section.

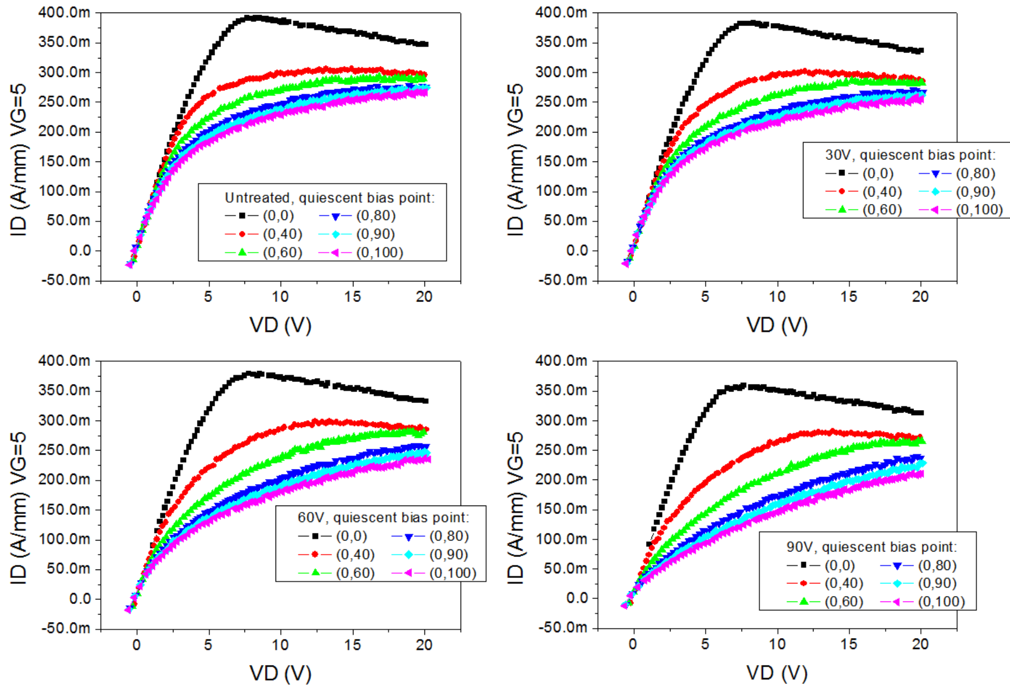


Figure 6.61: Dynamic performances of a PD5 device over stress voltage.

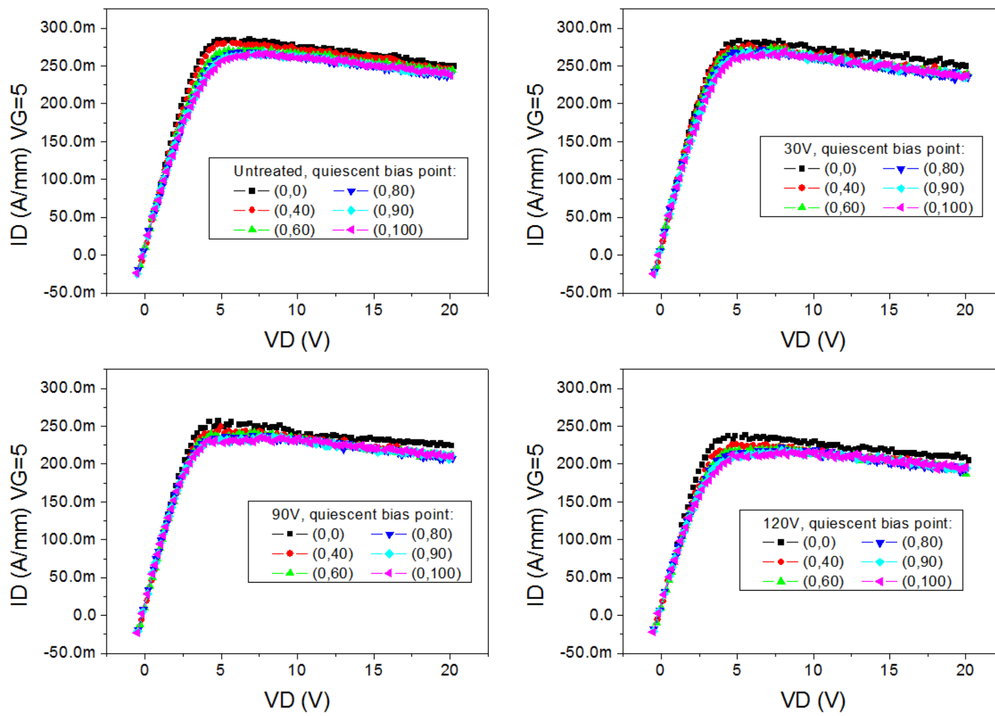


Figure 6.62: Dynamic performances of a PD8 device over stress voltage.

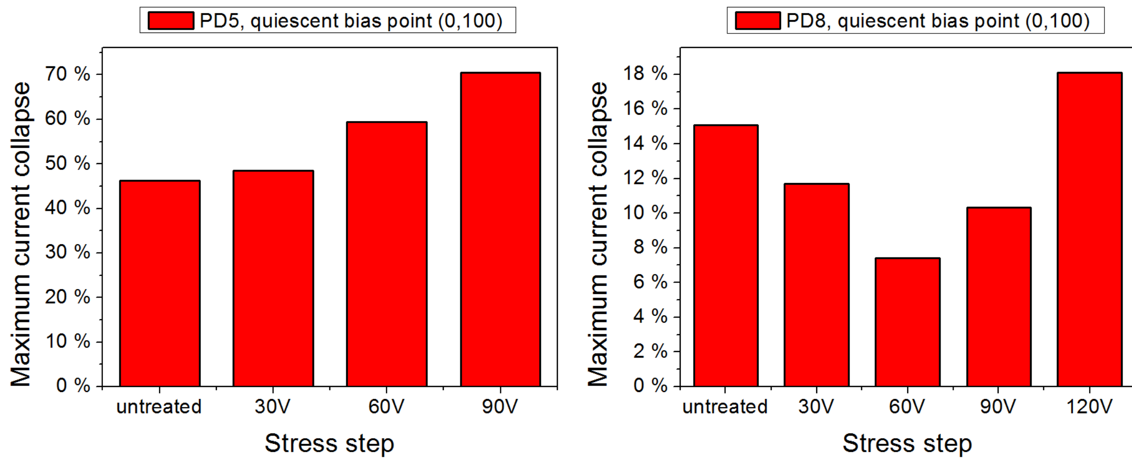


Figure 6.63: Comparison of the maximum current collapse over stress voltage.

Off-state

The good robustness typical of GITs when an high drain voltage is applied is confirmed by the results of the off-state step-stress. A device with Lg = 0.6 μm, Lgd = 1.05 μm (see figure 3.18) was submitted to a step-stress experiment in off-state conditions (VG=0) and increasing drain voltages from 12 V up to the catastrophic failure. The duration of each step was 600 seconds and dc characteristics were measured after each stage of the step-stress experiment. In figure 6.64 we can see that the device exhibits almost no degradation until the catastrophic breakdown, which occurs at Vgd = 100 V. For a device with a gate - drain distance of 1.05 μm, this is an outstanding performance.

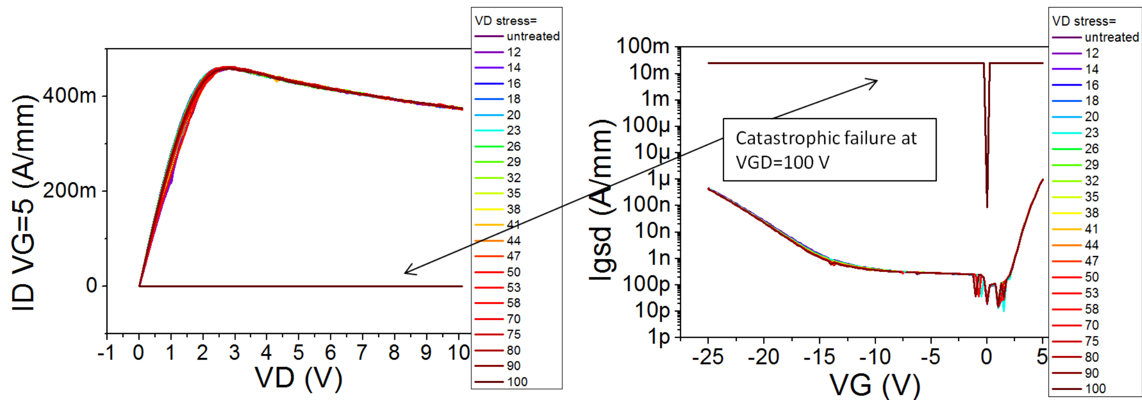


Figure 6.64: Results of the off-state step-stress on a PD10 device.

On-state

As discussed at page 6.6, the most critical part of a GIT is the gate - source diode. In order to investigate its degradation, the on-state step-stresses were carried out at a fixed drain voltage (Vds = 7, 12, 21, 30 V) and increasing gate voltage from 3 V to failure with a 0.25 V step. The duration of the step was 120 seconds and each of the analyzed devices had the same dimensions (Lg = 0.6 μm, Lgd = 1.05 μm, see figure 3.18). The typical results of this test are reported in figure 6.65 for Vds = 7 V.

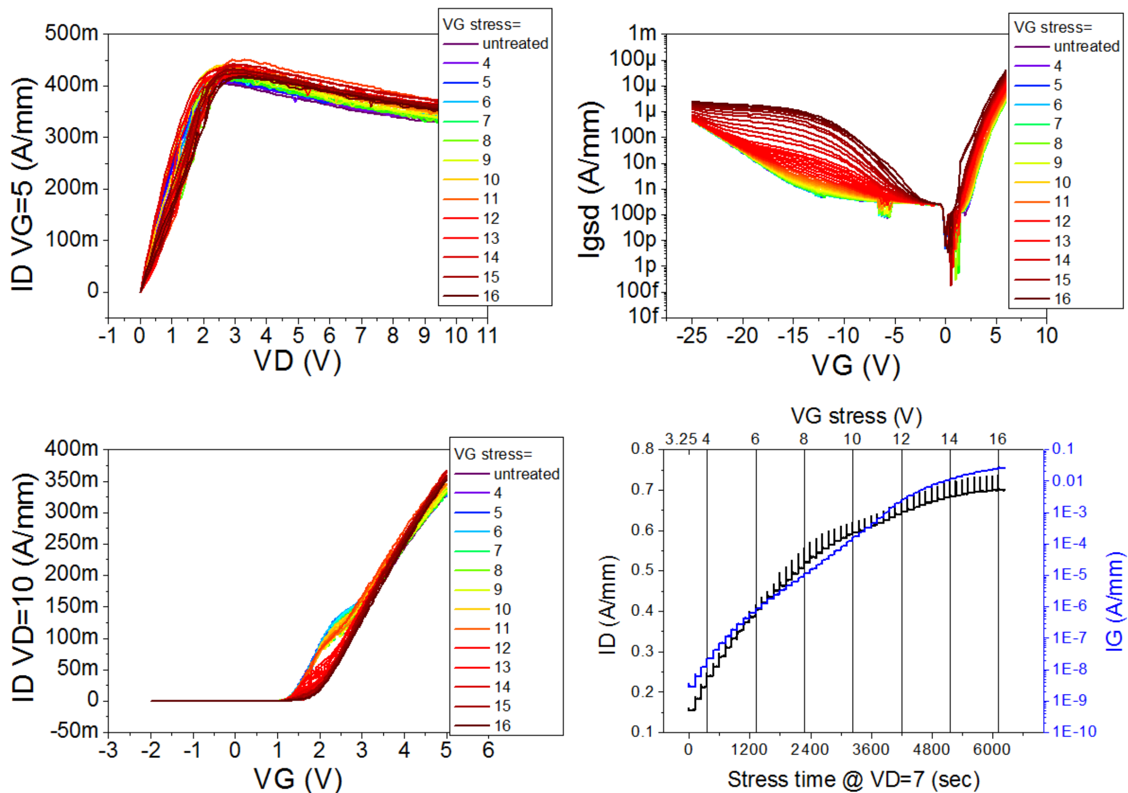


Figure 6.65: Results of the on-state step-stress (Vds = 7 V) on a PD10 device.

There is no gradual degradation of the gate diode and of the transistor up to very high gate voltages (Vgs = 9 V, a value 4 V higher than the expected operating one). The device was still working after being stressed at Vgs = 16 V. The same happens at the stress Vds = 12 V: before catastrophic failure (which occurs at Vgs = 8 V), there is not even a slight modification of the gate diode and of the transistor characteristics. The device stresses at Vds = 21 V failed at Vgs = 4.5 V, while the one stressed at Vds = 30 V ceased its functioning at Vgs = 3 V, a value substantially lower than in

the previous cases, probably due to the increased power dissipation at higher Vds. A common occurrence in all the tests is that the electroluminescence signal seems to be focused at the edges of the gate, as reported in figure 6.66 for a device stressed at Vds = 12 V and 21 V. The position of the electroluminescence peak may be related to the presence of a metal line that connects the two ends of the gate finger, as can be seen in a picture of the device (figure 6.67).

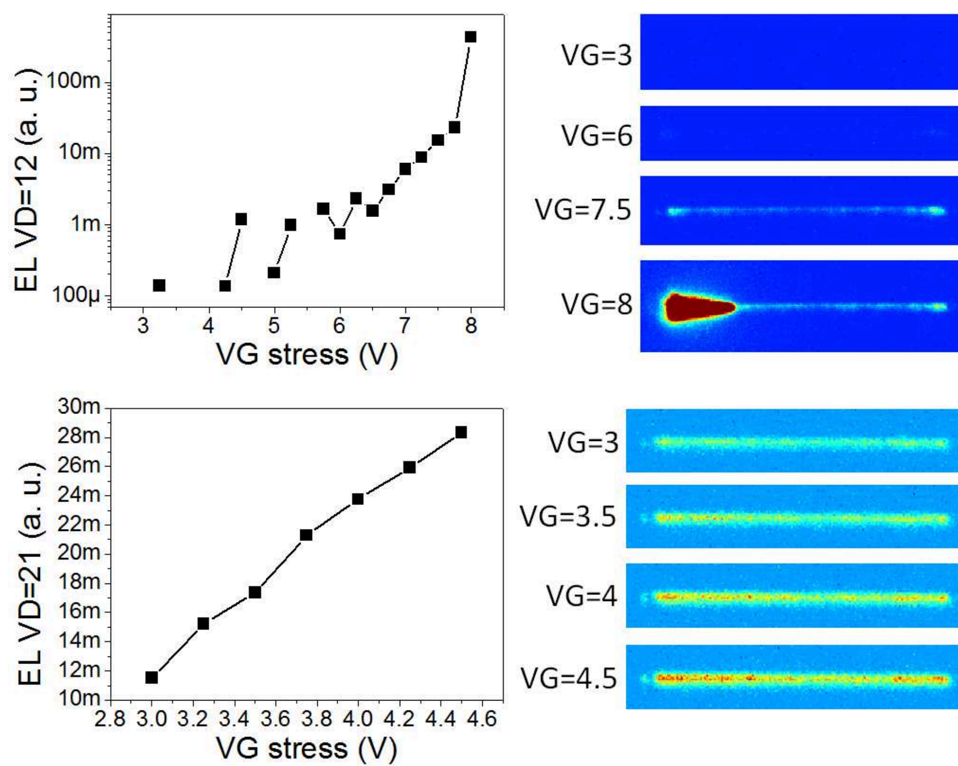


Figure 6.66: Electroluminescence of two devices stressed at Vds = 12 V and 21 V.

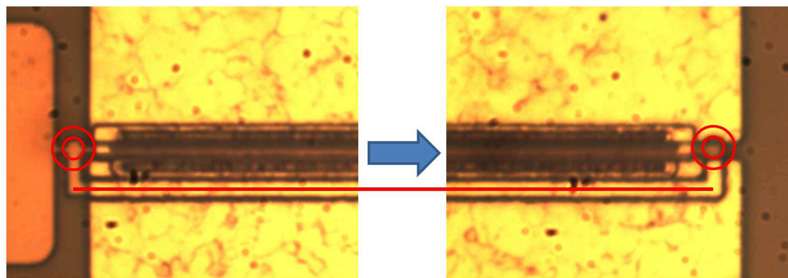


Figure 6.67: Picture of the structure of a PD10 device. Highlighted is the metal line that connects the two ends of the gate finger.

It has been reported in the previous section that failure seems to be related to power dissipation rather than to the applied voltage. The graph of figure 6.68 summarizes, for each tested drain voltage:

- the gate voltage of the catastrophic failure;
- the drain current reached before the failure;
- the power dissipation before the failure.

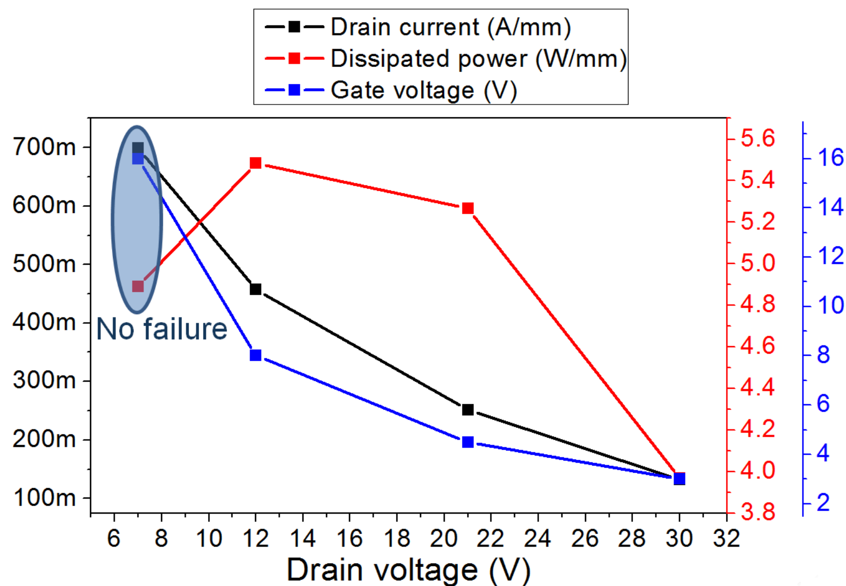


Figure 6.68: Summary of the results of the on-state step-stress on PD10 devices.

Power limit tests

In order to obtain other data about the power dissipation of the devices at the various bias conditions, power limit tests were carried out on the same devices of the previous tests (Lg = 0.6 μm, Lgd = 1.05 μm). At various gate voltages (Vgs =3, 4, 6, 8 V) was obtained the Ids versus Vds curve up to the Vds value that gives a 3.25 W/mm power dissipation measuring the spatially-resolved EL map at each (Vgs, Vds) bias point. The graphs in figure 6.69 summarize the results of this test, and in addition report the values of catastrophic failure from the step-stress tests. This data make it possible to identify the (Vgs, Vds) region where it's safe to operate these devices.

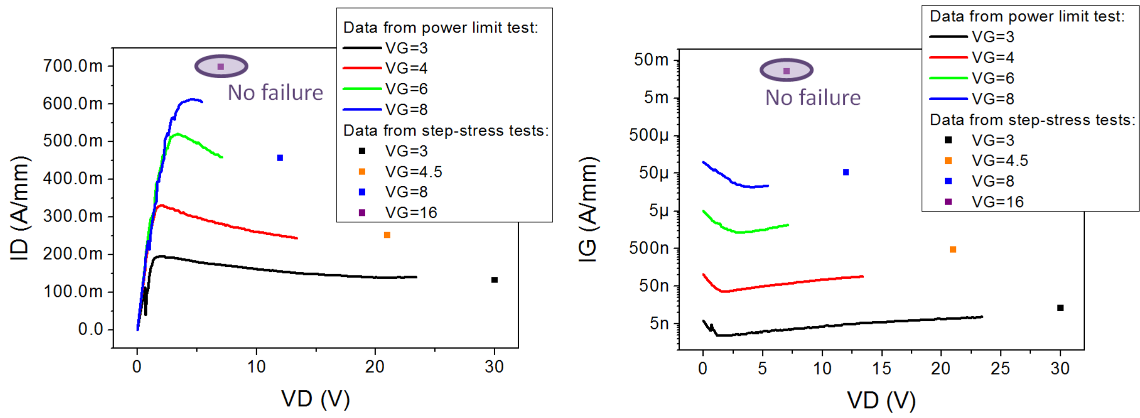


Figure 6.69: Summary of the electrical results of the power limit test on PD10 devices.

The electroluminescence seems to be focused at the ends of the gate finger, as it was during the previous on-state step-stresses. The origin of the measured emission is due to different reasons:

- at high Vgs, we have injection of holes from the p-gate to the channel (rich of electrons); the two carriers recombine generating a photon;
- at low Vgs, we have emission of light at high Vds, caused by the bremsstrahlung of hot electrons.

Figure 6.70 reports the total radiation emitted by the devices at different Vds and Vgs, along with some typical electroluminescence maps and with the curves of the power dissipated during the test.

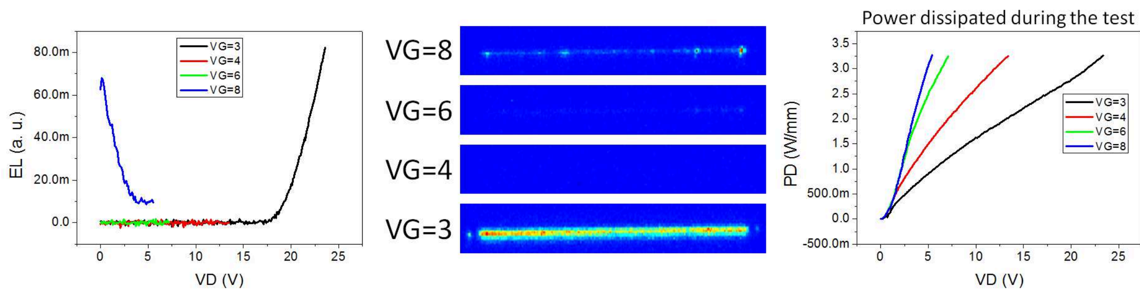


Figure 6.70: Summary of the optical results of the power limit test on PD10 devices and of the power dissipated by the devices at various bias conditions.

6.9 Thermal resistance

The channel temperature is one of the most important operating parameters for a GaN High Electron Mobility Transistor. The reasons are several:

- the temperature strongly affects the performances of the device, since the charge transport is strongly temperature-dependent. The mobility and the saturation velocity of electrons are a function of temperature, and their high values are one of the most important reasons to grow devices based on Gallium Nitride, so their variation with the operating temperature has to be taken into account;
- high temperatures give birth to highly energetic phonons, and strong vibrations of the lattice may cause damage to the crystal and a degradation or premature failure of the device;
- most of the failure prediction models require accelerated lifetime tests at channel temperatures higher than the nominal one.

Then, it is necessary to have an accurate estimate of the channel temperature during the normal operation of the device at the nominal bias (for the first two reasons) and at higher biases and/or external temperatures (for the third one). In a first approximation, it can be expressed as

$$T_{chan} = T_{amb} + R_{th} P_D$$

where T_{amb} is the external temperature, P_D the dissipated power and R_{th} a parameter called *thermal resistance*. It is enough to measure the thermal resistance (channel to ambient) of the device to evaluate the channel temperature in all the previously-mentioned conditions.

6.9.1 Pulsed technique

There are several approaches that can be used to evaluate the thermal resistance, each one with its strong points and drawbacks: optical, through micro-Raman [153] or IR cameras [154], physical [155] or electrical [156, 157]. The method that has been employed is the pulsed one [158]. In the first part of this technique, pulsed ID - VD

are carried out in order to find the dependence of a thermally-sensible parameter (on-resistance or saturation current) on the quiescent bias point temperature or the quiescent bias point dissipated electrical power. From the relationship between this parameter and the temperature or the power it is possible to evaluate the dependence of the channel temperature on the power dissipation. The slope of their relationship is the thermal resistance.

6.9.2 Experimental results

The measure was repeated on several GIT samples of different iterations of the technological processes, in order to obtain the average value of the thermal resistance. Figure 6.71 reports the results of the pulsed measurements as a function of the dissipated power (a) and of the external temperature (b). From those have been extrapolated the kinetics and the linear relationships of the two temperature sensible parameters, on-resistance (a) and saturation current (b), as shown in figure 6.72. Those values are then aggregated in order to obtain the relationship between temperature and dissipated power, whose slope is the thermal resistance (figure 6.73).

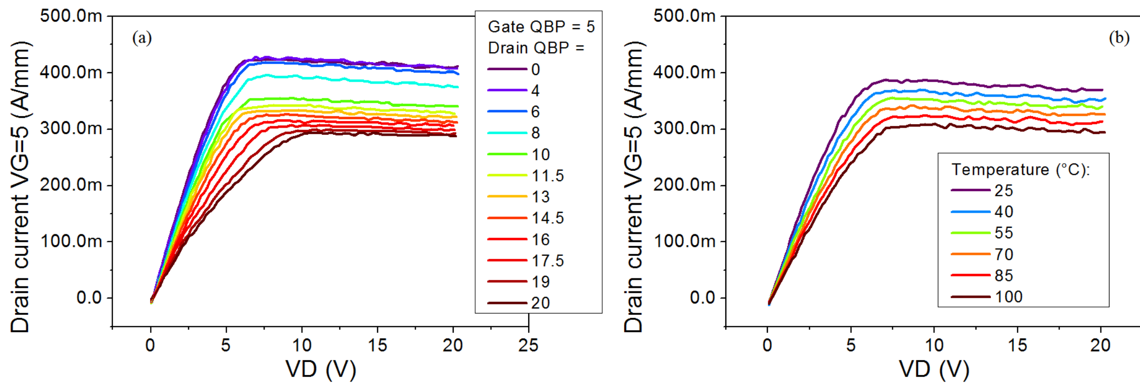


Figure 6.71: Pulsed calibration maps at different (a) dissipated power and (b) temperatures.

Figures 6.74, 6.75 and 6.76 report the same results on an improved device. In both cases the thermal resistance was found to be ≈ 20 °K mm/W. Since the improvement consisted mostly on a better epitaxy, and given that the largest part of the heat is dissipated through the substrate (which then affects the most the thermal resistance), the experimental results are consistent with the variations in the structure.

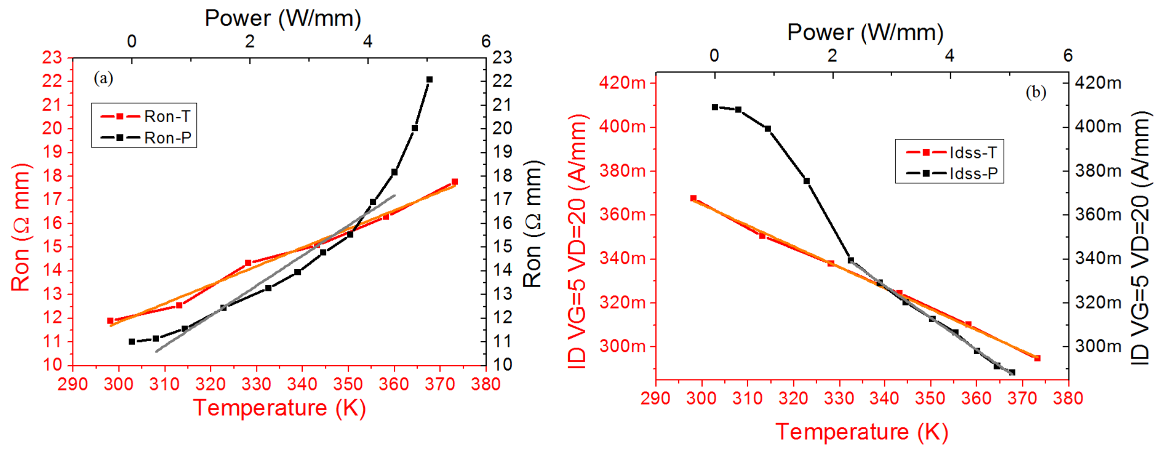


Figure 6.72: Relationship between the temperature sensible parameter on-resistance (a) and saturation current (b) and the external temperature or dissipated power.

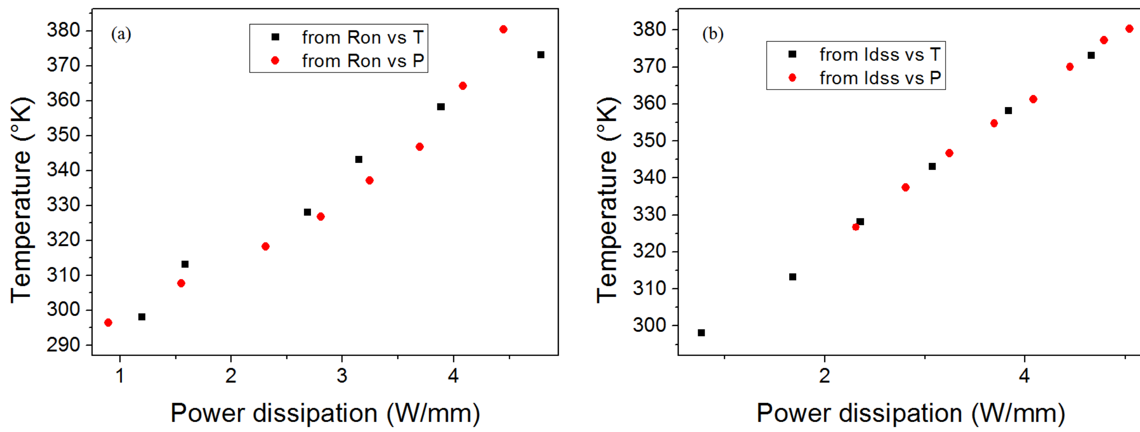


Figure 6.73: Extrapolation of the thermal resistance.

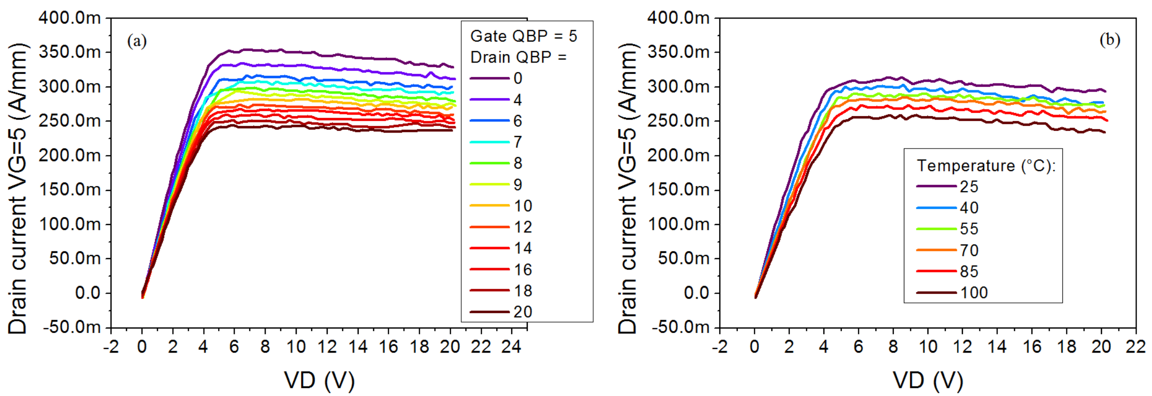


Figure 6.74: Pulsed calibration maps at different (a) dissipated power and (b) temperatures for an improved device.

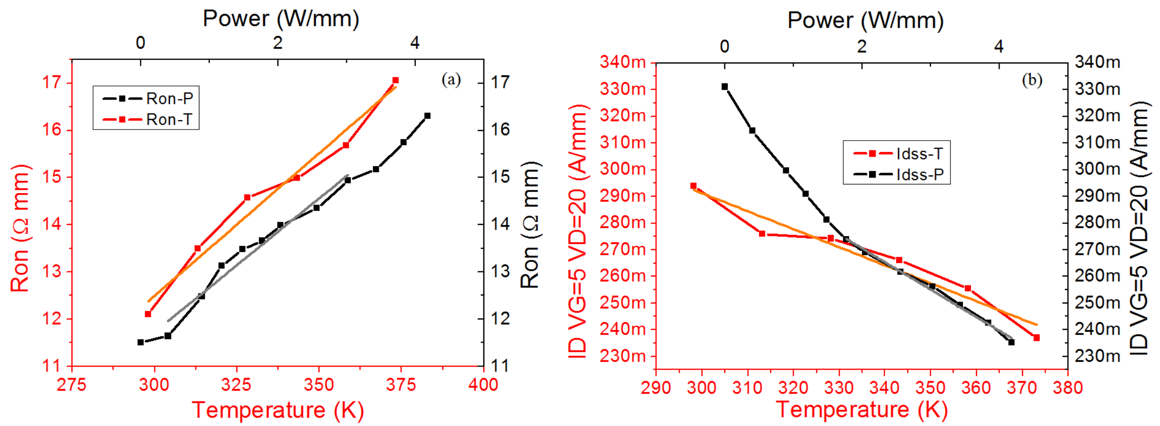


Figure 6.75: Relationship between the temperature sensible parameter on-resistance (a) and saturation current (b) and the external temperature or dissipated power for an improved device.

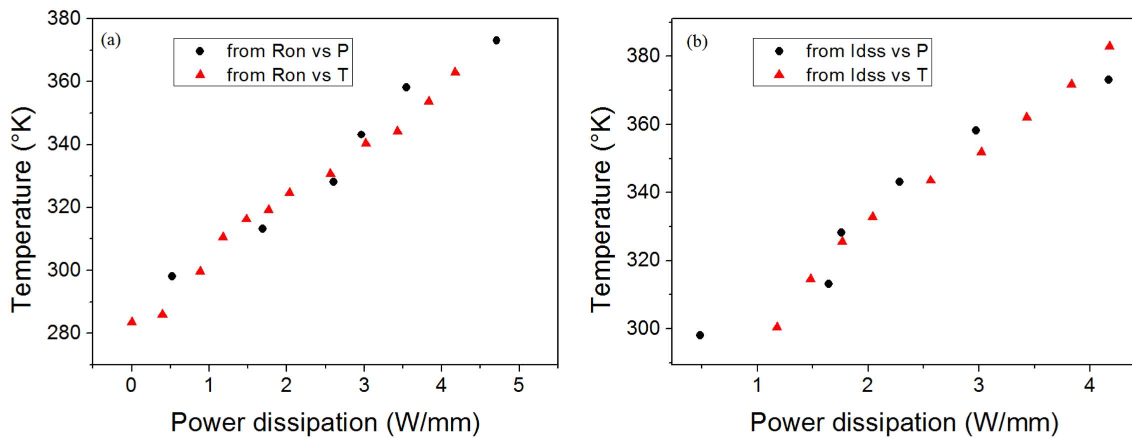


Figure 6.76: Extrapolation of the thermal resistance for an improved device.

6.10 Gate materials

This section reports the results of degradation tests performed on GaN HEMTs with different gate materials: Ni/Au/Ni, ITO and Ni/ITO, in order to study the sensitivity to high gate-drain electric fields. The devices under test are Ga-face HEMTs with different gate metal stacks (Nickel/Gold/Nickel, Indium Tin Oxide and Nickel/Indium Tin Oxide), provided by University of California at Santa Barbara. All the analyzed devices come from the same wafer, i. e. have exactly the same epitaxial parameters. The only difference is in gate material and processing. These transistors are composed by two equivalent gate fingers, 0.7 × 50 μm each. The

gate-source and gate-drain spacing is, respectively, 0.3 μm and 1 μm. One of the fingers was submitted to step-stress tests at Vgs = -5 V (off-state value for these devices) and increasing Vds levels from 10 V for two minutes, increasing Vds by 2 V until failure. At each step electrical and optical measurements were performed: are analyzed the gate diode, probed at Vgs from 10 V to 1.5 V at Vds = 0 V, and the near-field electroluminescence maps, evaluated at Vgs = 10 V and Vds = 0 V. Under the adopted stress conditions, devices are in off-state: only a negligible current flows through the channel, while the gate-drain diode is submitted to high reverse voltage. During the tests, the gate-source diode is kept at a constant Vgs = -5 V, a value that is too low to cause a variation in its performances. By monitoring the gate diode after each stress step, we can describe how the applied electric field influences the insulation between the gate and the channel region. The obtained data, reported in figure 6.77 for a Ni/ITO device, point out the presence of a critical voltage, a peculiar value of polarization responsible for a steep increase of the leakage current [80].

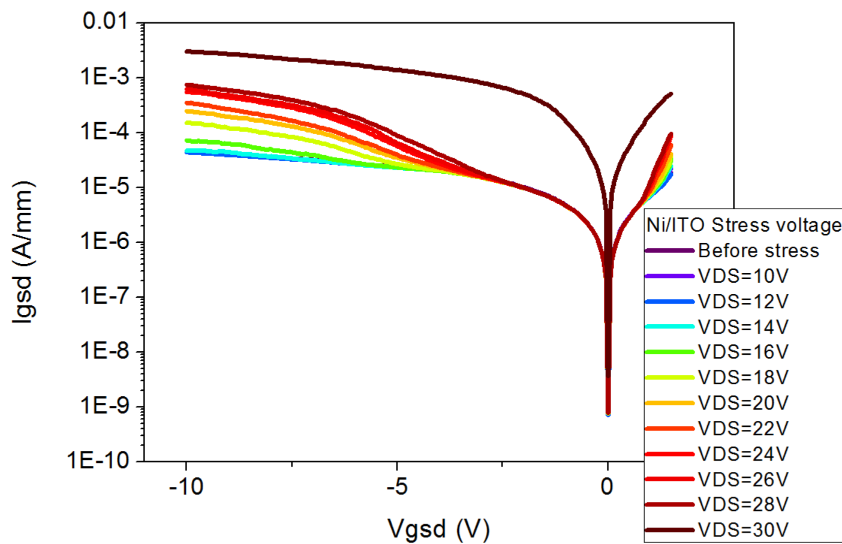


Figure 6.77: Variation of the gate diode current - voltage relationship over off-state stress (Vgs = -5V) and various Vds applied for 2 minutes.

A better description of the degradation process can be obtained through the analysis of the near-field electroluminescence maps. In figure 6.78 we can see the formation of emitting "hot spots" at the gate edge, localized where the leakage current is higher [159]. Reverse-bias degradation is usually ascribed to converse piezoelectric effect

[160], i. e. to a process which is strongly dependent on the epitaxial properties of the devices (in particular on the thickness and Aluminum content of the AlGaN layer).

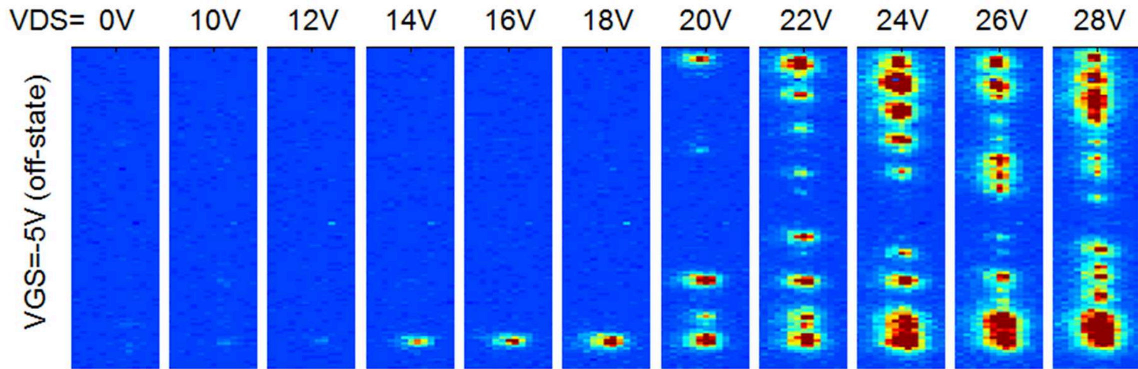


Figure 6.78: Spatially-resolved EL maps of a Ni/ITO HEMT stressed at Vgs = -5 V and increasing Vds for 2 minutes. Images were taken at Vgsd = -10 V.

Remarkably, the comparison between devices with different metal stacks (and the same epitaxy) indicates that samples with Ni/Au/Ni, ITO and Ni/ITO gates have different leakage currents and critical voltages for catastrophic breakdown (see figure 6.79). Devices based on Indium Tin Oxide showed high robustness and a slow degradation, whereas gates containing gold caused a steep increase in the reverse current even at low stress voltages. This result suggests that reverse-bias degradation of HEMTs cannot be solely ascribed to an epitaxy-dependent mechanism: the choice of the gate material and of the processing conditions may significantly influence the degradation of GaN HEMTs.

To summarize, This section reports the results of degradation tests performed at Vgs = -5 V and increasing Vds levels (and so gate - drain electric fields) on Ga-face GaN HEMTs with different gate materials: Ni/Au/Ni, ITO and Ni/ITO. At each step of the stress experiment, the electrical and optical characteristics of the transistors were measured to analyze the degradation process. It is found that

- stress induces a permanent degradation of the gate diode, consisting in an increase in the leakage current;

- this change is due to the generation of parasitic conductive paths, as suggested by electroluminescence (EL) mapping;

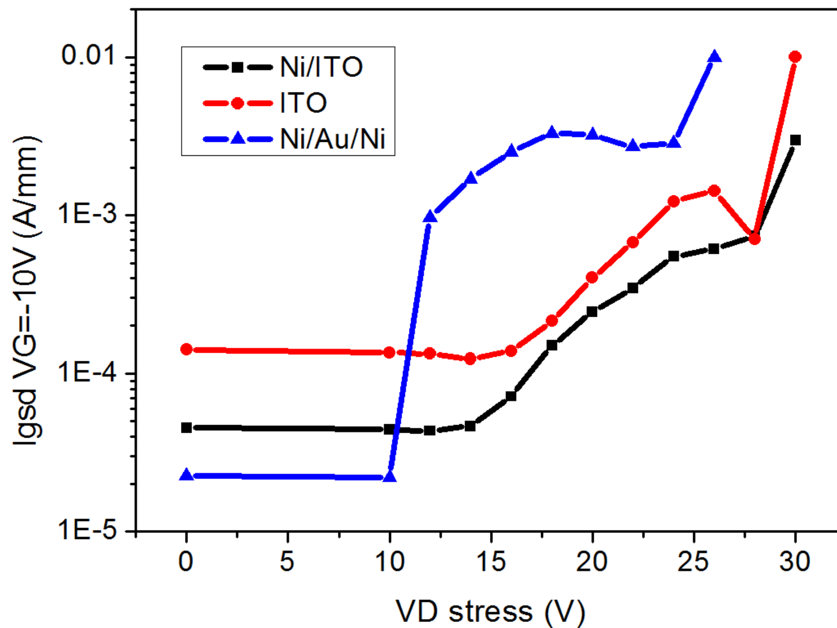


Figure 6.79: Reverse current increase for different gate materials, during reverse-bias (Vgs = -5 V, increasing Vds, duration 2 minutes) stress tests.

- the onset voltage of the degradation (critical voltage) can be strongly influenced by processing parameters, and devices based on ITO showed higher reliability.

These data strongly support the hypothesis that the robustness is influenced by processing parameters and/or by the gate material, since all analyzed devices come from the same epitaxial wafer. Dependence on the gate stack of the EL further suggests that gate material plays an important role in the deterioration of the device.

6.11 Natural superjunctions

A general description of the structure and of the operating principles of the natural superjunctions can be found in the relevant section at page 94. The outstanding performances of those devices have to be validated by analyses of their response to very high electric fields (as it is the case for devices used in power electronics) and of their reliability during typical operation. The devices under test belong to two subsequent iterations of the technological process, respectively DD1 and DD2.

6.11.1 Trapping phenomena

Trapping analysis

The devices, after a period at high reverse bias, show a decrease of the forward current due to trapping effects. The measurement of the diode current was performed by quick voltage pulses in order to avoid detrapping caused by biasing and power dissipation. To obtain a deeper understanding of the trapping mechanism, it was performed the following experiment on a device with an anode - cathode distance Lac = 10 μm. The device underwent a repetition of two measurements: a 5 seconds trapping period at anode voltage VA = -100 V (cathode - grounded, CG) and a quick check of the forward-bias I - V curve, from 0.5 V to 3 V, step 0.5 V. During all the tests the substrate was grounded. The results are reported in figure 6.80: there is a very strong decrease of the forward current, caused by the increase of the resistivity due to the depletion of the conductive "channel" induced by the trapped charge.

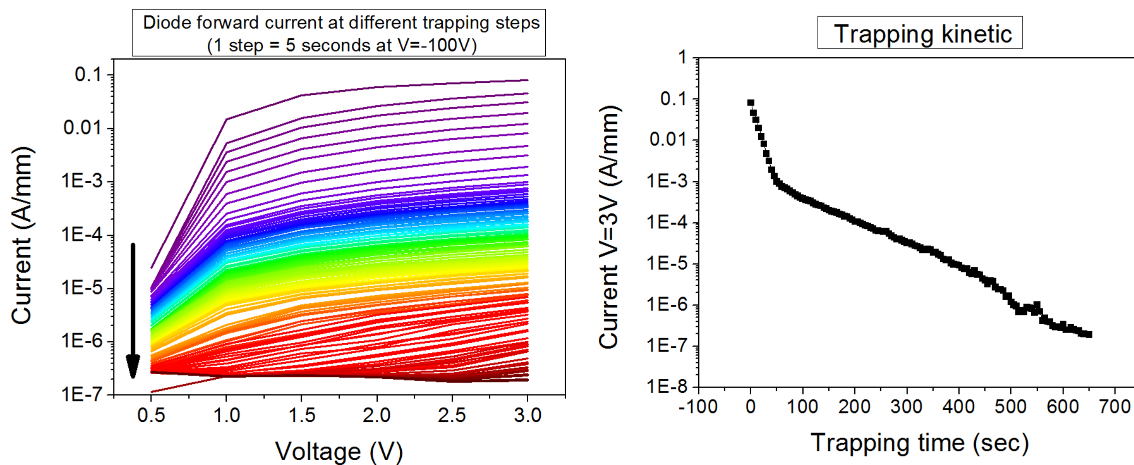


Figure 6.80: Variation of the forward - bias characteristic of a DD1 diode submitted to trapping. Cathode - grounded (CG) condition.

These devices employ a Schottky diode on the anode contact, so their behavior is highly non-symmetric. In order to gain other useful information, the same experiment was repeated also in anode - grounded (AG) condition. In this case, the trapping cathode voltage VC was chosen equal to 100 V. The opposite polarity is necessary in order to keep the device reverse-biased. The results reported in figure 6.81 highlight a trapping effect that is five orders of magnitude lower that in the CG condition.

Since trapping is more prominent in the cathode - grounded configuration, in which a negative potential is applied between anode and substrate, with respect to the anode grounded condition, this result suggests that the decrease in diode current is related to vertical charge trapping mechanisms.

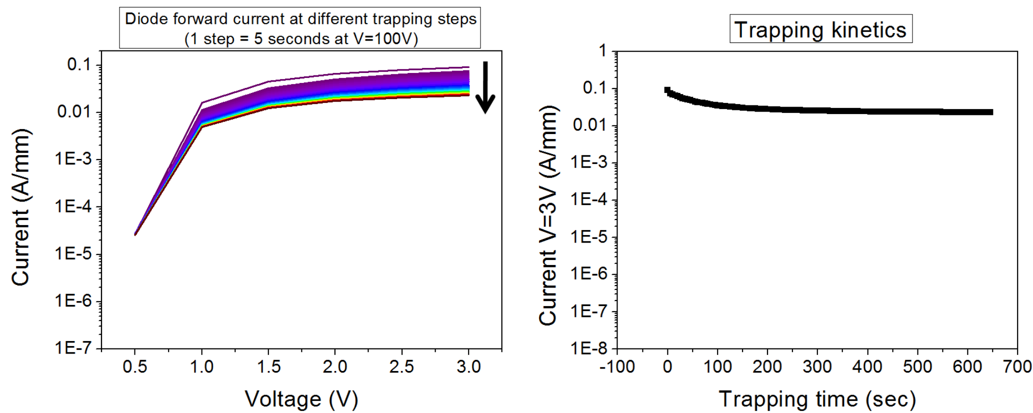


Figure 6.81: Variation of the forward - bias characteristic of a DD1 diode submitted to trapping. Anode - grounded (AG) condition.

The same measurements was carried out on the DD2 family (Lac = 10 μm, same as for DD1), adapting the parameters to the different characteristics of the device: a 0.5 seconds trapping period at VA = - 100 V (CG, same trapping voltage as DD1), and then a quick check of the forward current, from 0.25 V to 2 V, step 0.25 V. The same experiment was performed also in anode - grounded condition, at VC = 100 V. The results are shown respectively in figure 6.82 and 6.83.

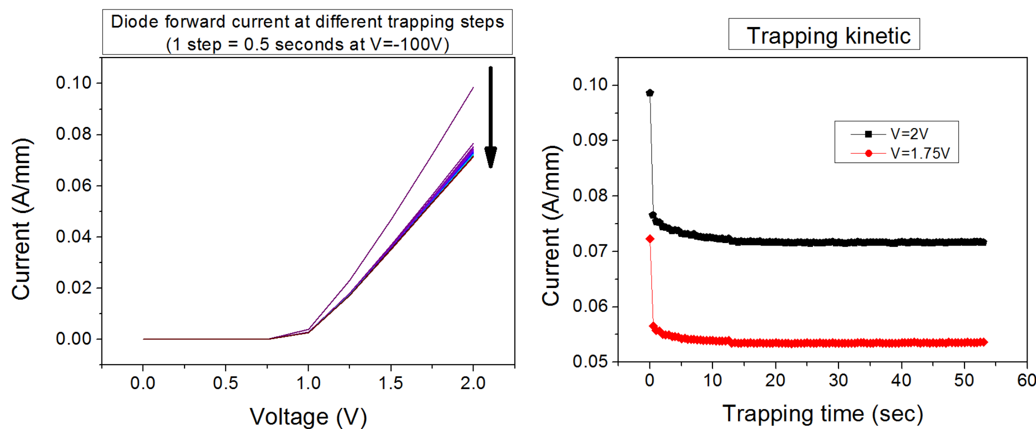


Figure 6.82: Variation of the forward - bias characteristic of a DD2 diode submitted to trapping. Cathode - grounded (CG) condition.

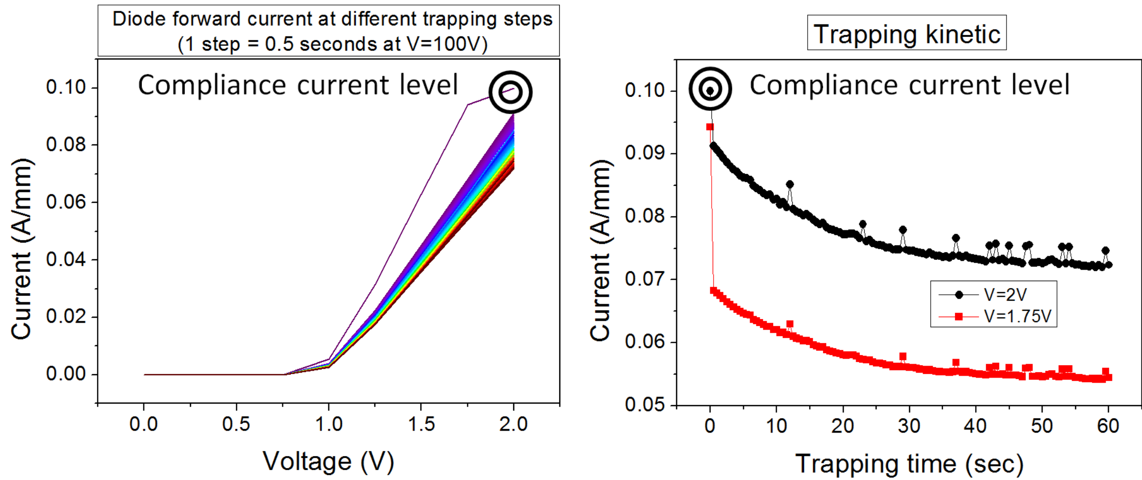


Figure 6.83: Variation of the forward - bias characteristic of a DD2 diode submitted to trapping. Anode - grounded (AG) condition.

It can be noticed a strong difference between the first (untrapped) characteristic in the two experiment, which have been carried out at the same conditions. In the second test the current even reaches its compliance value. What has changed in the second case is the initial condition: in order to achieve a complete detrapping after the previous experiment, the device was kept for some time under the light of the probe lamp. The DD2 family exhibits an intrinsic trapping. The device, after an extended rest time, is found at an intermediate condition between the completely detrapped and fully trapped state (see figure 6.84).

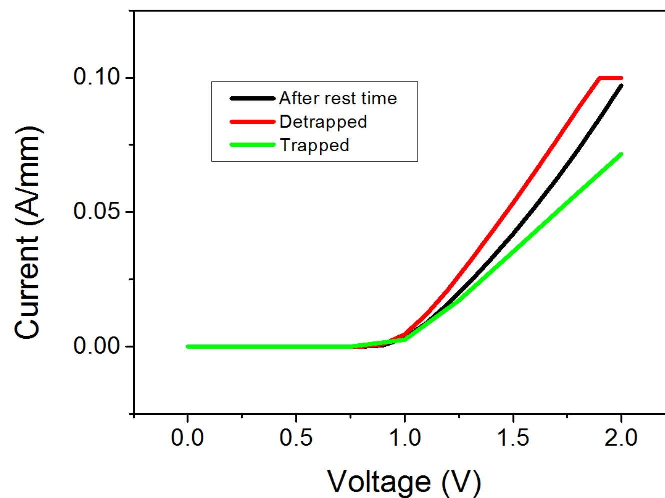


Figure 6.84: Detection of the intrinsic trapping in a DD2 device.

Testing DD2 devices using a sampling technique to avoid the detrapping effect of biasing is not possible. Due to the intrinsic trapping, this kind of device traps charge between the samples, thus distorting the kinetic. Figure 6.85 shows the effects of the intrinsic trapping during a detrapping current transient. After an initial detrapping part (yellow) where the device behaves as expected, the current decreases due to the intrinsic trapping (red). Since the time constants of the two processes are different (or the two processes are related to charge trapped in different regions of the device), the detrapping continues with a noisy behavior due to the intrinsic trapping between the non-perfectly even spaced samples of the transient (green). If the wait time between the samples is increased, there is another decrease of the current, as it was in the red region, caused by the increased time available between the samples for the intrinsic trapping (blue). Then, using a sampled characterization causes a strong distortion of the transient and a great amount of noise superimposed to the curve. This hypothesis is further confirmed by the detrapping kinetic under monochromatic light that will be reported in figure 6.89. Under more energetic photons the device releases all the trapped charges, thus reaching a current level that is higher than the value measured after a rest period under no illumination.

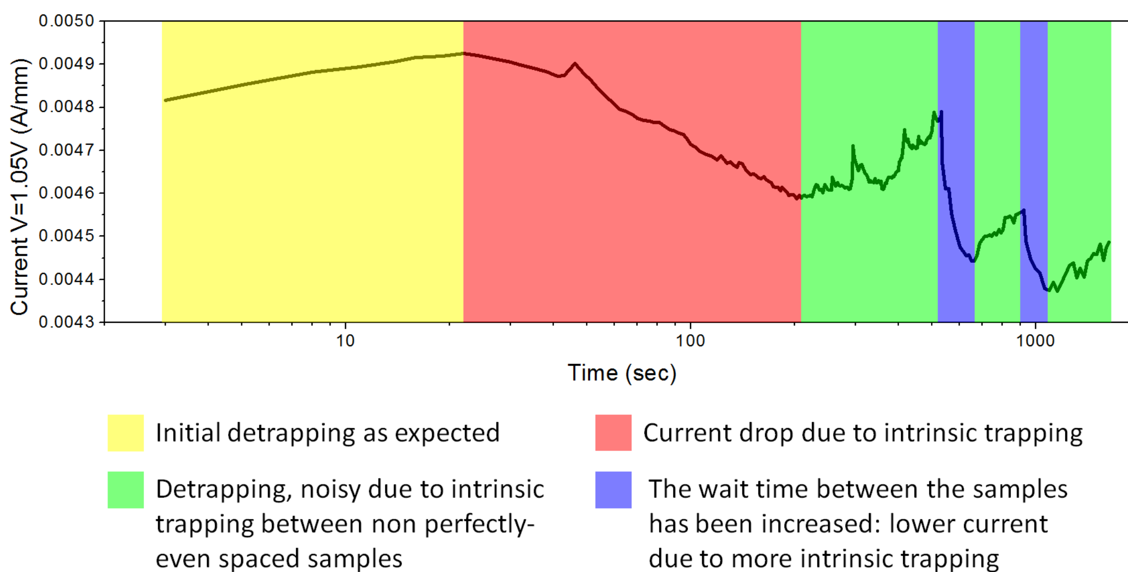


Figure 6.85: Current transient of a DD2 device showing intrinsic trapping effects.

Detrapping analysis

Some additional test were carried out to analyze the recovery of the current during the detrapping process. After an initial trapping time (120 seconds at VA = -100 V), the diode current was continuously monitored for an extended period of time. During this phase the diode was kept at a constant voltage, whose value was chosen as the value that produces, in the device without trapping, a current of 10 mA/mm (DD1: 0.91 V, DD2: 1.05 V). The same experiment was performed also in anode - grounded condition (VC = 100 V). The graph in figure 6.86 summarizes the difference between the cathode - grounded and anode - grounded conditions. The detrapping kinetics are faster in the cathode - grounded condition, which confirms the probable presence of a trapping mechanism related to the vertical voltage. Moreover, the detrapping is slower for DD2 devices even if the amount of current collapse is lower: this is probably another experimental evidence of the presence of intrinsic trapping in these devices, which is concurrent with the detrapping and slows it down.

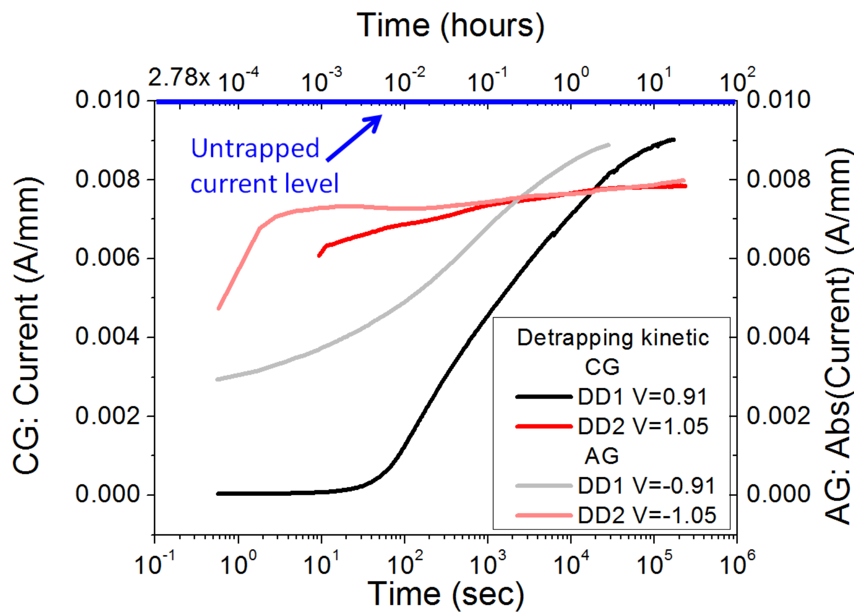


Figure 6.86: Detrapping transients of natural superjunctions.

To gain further insight on the traps responsible of the current drop, the test was repeated under monochromatic light of various energies. As can be seen in figure 6.87 for the cathode - grounded condition and figure 6.88 for the anode - grounded, the detrapping transients are strongly accelerated by higher photon energies.

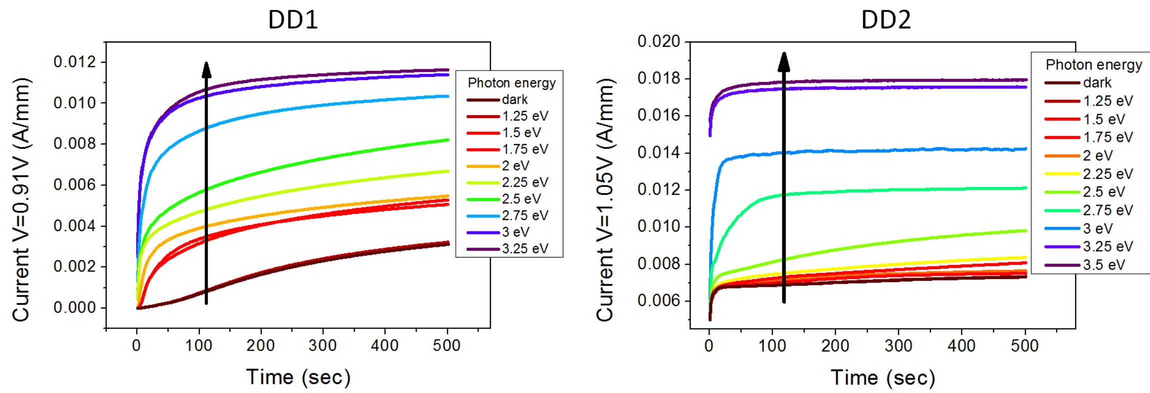


Figure 6.87: Detrapping transients under monochromatic light, cathode - grounded.

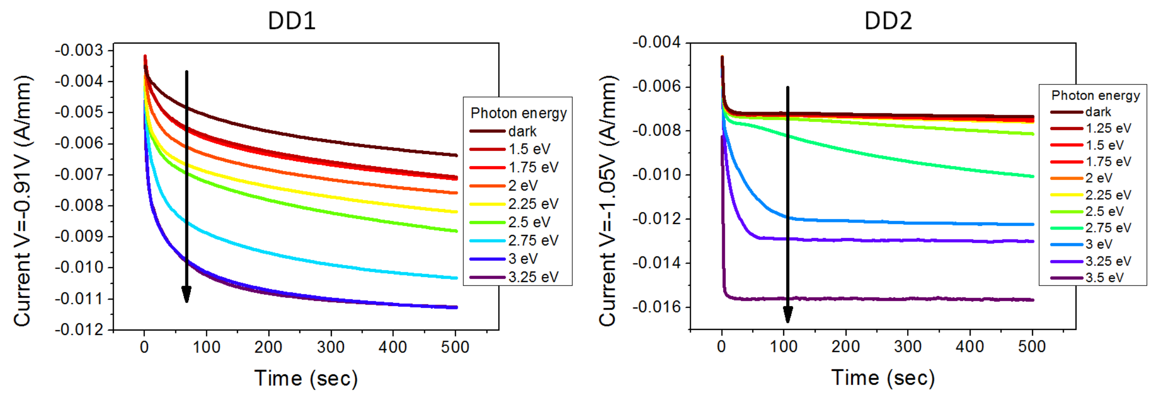


Figure 6.88: Detrapping transients under monochromatic light, anode - grounded.

The following graph (figure 6.89) summarizes the difference between the cathode-grounded and anode-grounded conditions for both device types. In this plot, the "dark" condition was reported as having a photon energy of 0 eV. In this case it is possible to see how there is an intrinsic trapping in DD2 devices, since the final current level is higher than the initial untrapped level. This is not an effect of carrier generation due to the light: it is not present in DD1 devices and begins to reach a saturation value at 3.25 eV.

The last analysis that has been carried out is the variation of the detrapping transients at different external temperatures, in order to evaluate the different time constants and to extrapolate the activation energy from the Arrhenius plot. An additional effect that has been found is the increased detrapping speed caused by the applied measure bias of the transient (see figure 6.90), so for DD1 devices the values were recorded sampling the transient to minimize the effect. The same analysis was

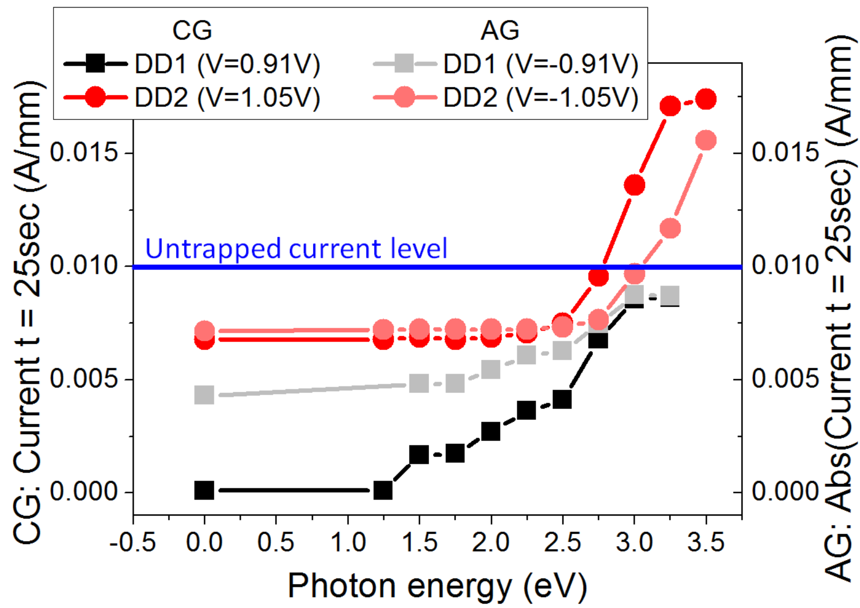


Figure 6.89: Comparison of the detrapping transients under monochromatic light.

not possible for DD2 due to their intrinsic trapping that perturbs the shape of the transient when the device is left unbiased for some time between the samples (figure 6.85).

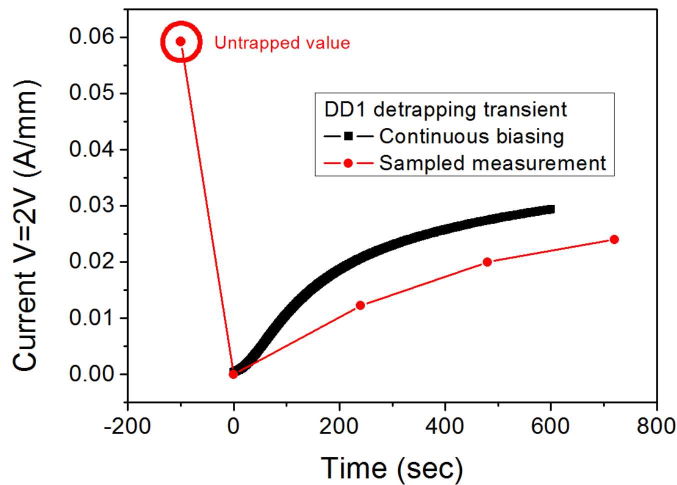


Figure 6.90: Comparison between continuous and sampled detrapping transients.

The detrapping transients of a DD1 device are summarized in figure 6.91 for both cathode - grounded and anode - grounded condition, while figure 6.92 reports the time constant spectra and the Arrhenius plot. The found activation energies were respectively 0.47 eV (CG) and 0.36 eV (AG).

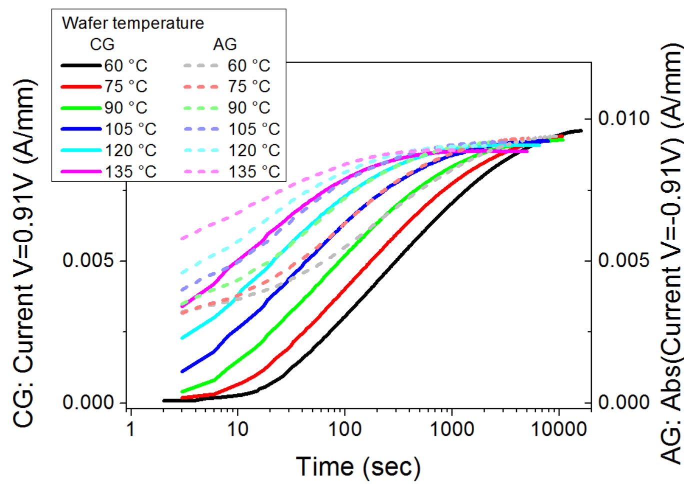


Figure 6.91: CG and AG detrapping transients at various temperatures, DD1 device.

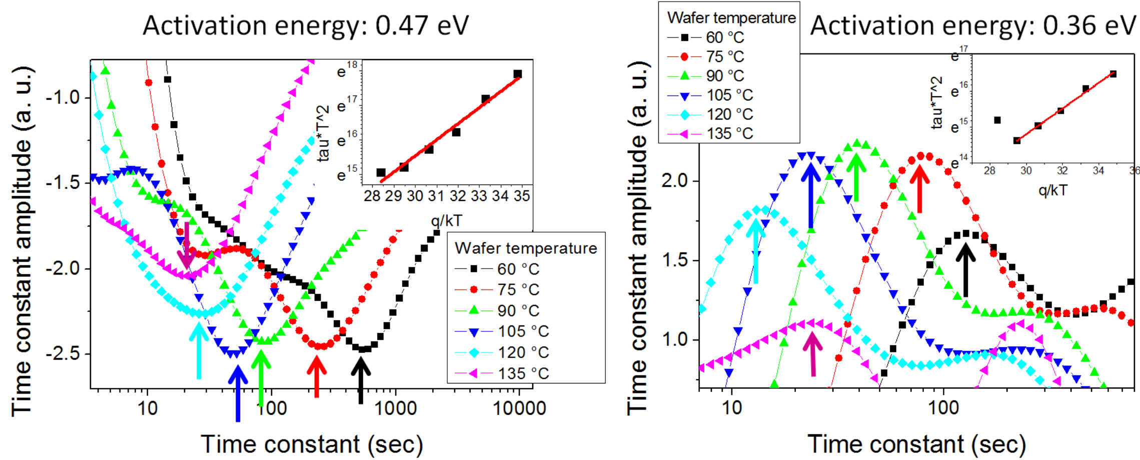


Figure 6.92: Time constant spectra and Arrhenius plot, DD1 devices.

The same data for a DD2 device are reported in figure 6.93 and 6.94. As said before, the only experimental difference with DD1 devices is that the transients are continuous and not sampled. The found activation energies were respectively 0.44 eV (CG) and 0.35 eV (AG). Those values are nearly identical to the ones reported for DD1 devices, so the defects responsible for the variation of the performances are probably the same for both the iterations of the technological process. If the causes of the current collapse are the same but DD2 devices are affected by a lower trapping intensity, the different design choices and the improvements made on DD2 proved to be effective.

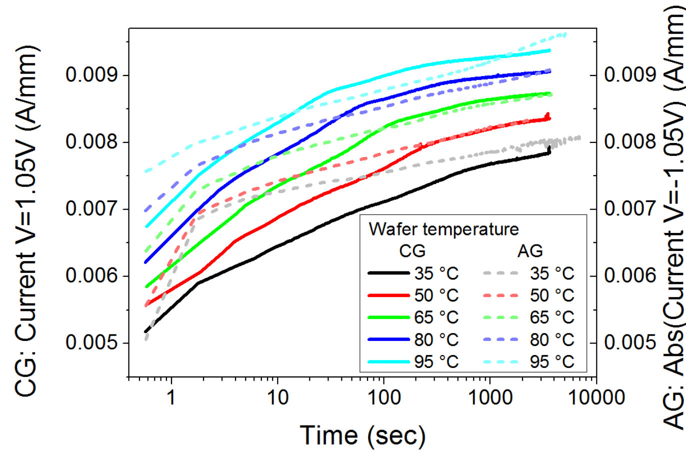


Figure 6.93: CG and AG detrapping transients at various temperatures, DD2 device.

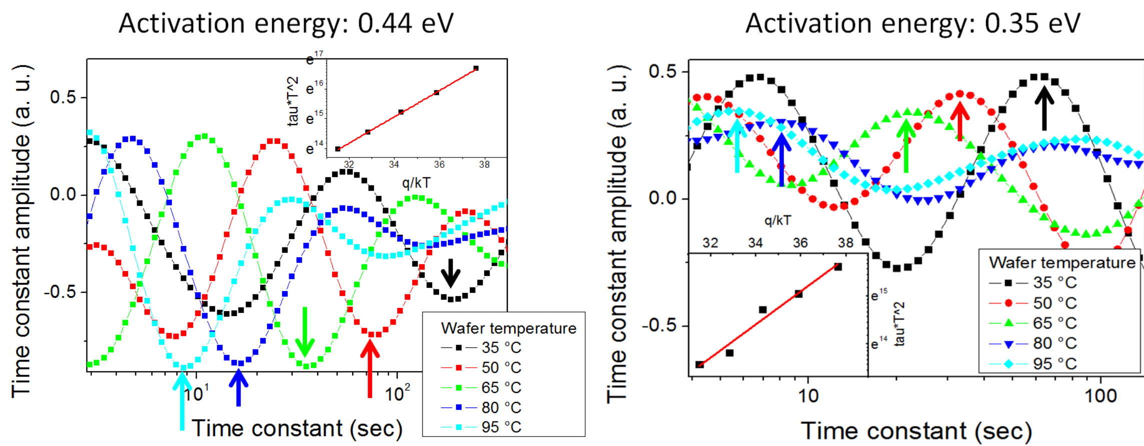


Figure 6.94: Time constant spectra and Arrhenius plot, DD2 devices.

6.11.2 Stresses

As seen in the previous section, the behavior of the substrate has a great impact in the performances of those devices. In order to gain the better knowledge about the physical modification associated with the degradation, each DC characterization was composed by an anode - cathode diode (Iac), an anode - substrate diode (Ias) and a cathode - substrate diode (Ics). The first experiment was a current - driven step-stress, carried out in order to find out the values that cause the degradation of the device to be used for the subsequent constant current stresses. The device tested has a anode - cathode distance Lac $= 20\ \mu$m, during the stress the substrate was grounded, the conditions are summarized in figure 6.95.

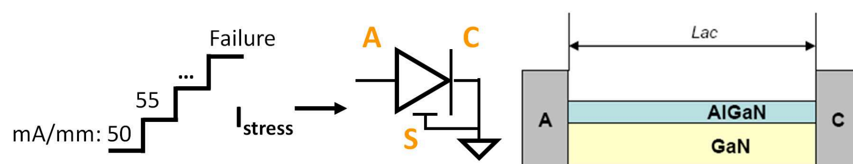


Figure 6.95: Test conditions of the step-stress experiment.

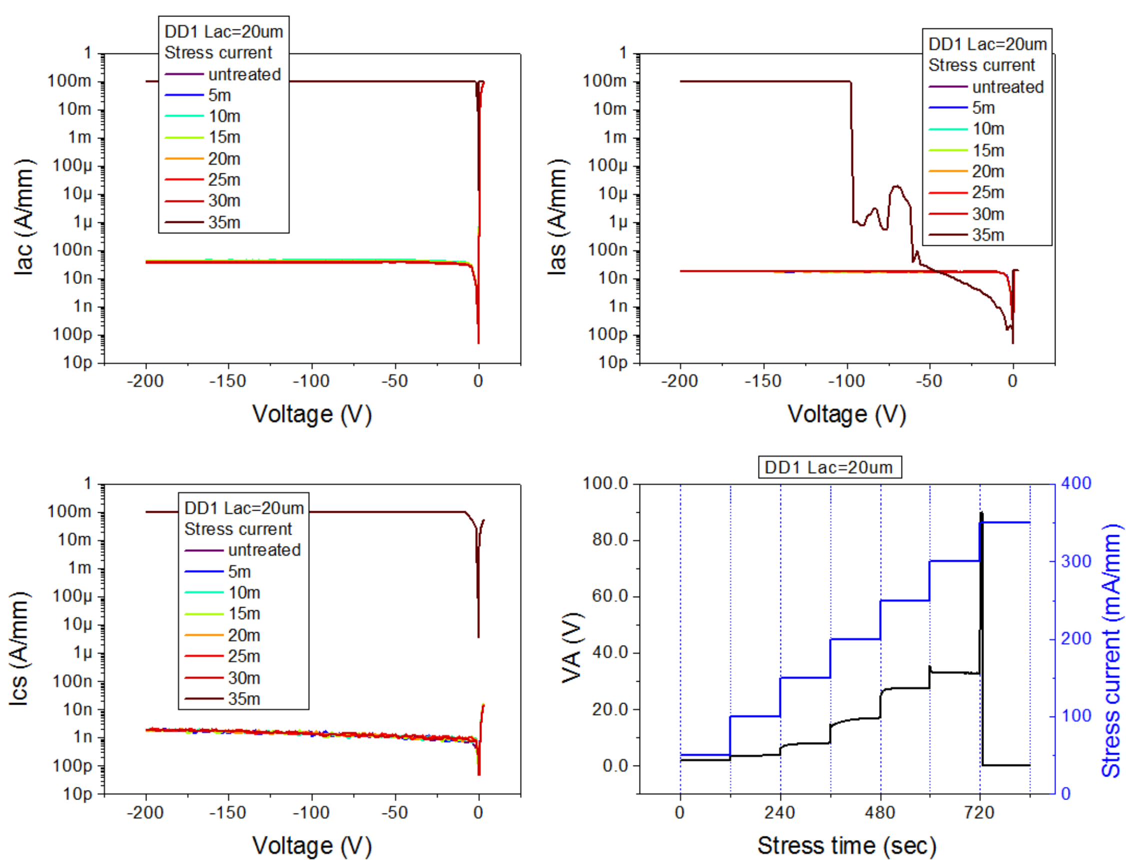


Figure 6.96: Results of the step-stress experiment.

Figure 6.96 shows that there is no gradual degradation of the device, which fails catastrophically at 350 mA/mm (the W of the device is 100 μm). Since the anode voltage VA reaches very high values during the operation, it is possible that the failure happens due to the power dissipated by the device. Anyway, the devices are able to withstand high power dissipation: the diode held 9.9 W/mm (300 mA/mm) and failed at 16.8 W/mm (350 mA/mm). The constant current stresses were then carried out on shorter devices (Lac = 5 μm), which have a lower resistivity and then dissipate less power. This is probably the correct interpretation, considering the results of figures 6.97 and 6.98, which report respectively the change of the characteristics of the device stressed at 300 and 350 mA/mm. The higher value caused the degradation of the device but not its catastrophic failure, as it was during the step-stress. Moreover, the lower value hasn't caused any degradation up to 8000 seconds. It is important to point out that the desired operating current for these devices is 100 mA/mm, than, considering the results of this test, it is probably possible to increase the expectations on their performances.

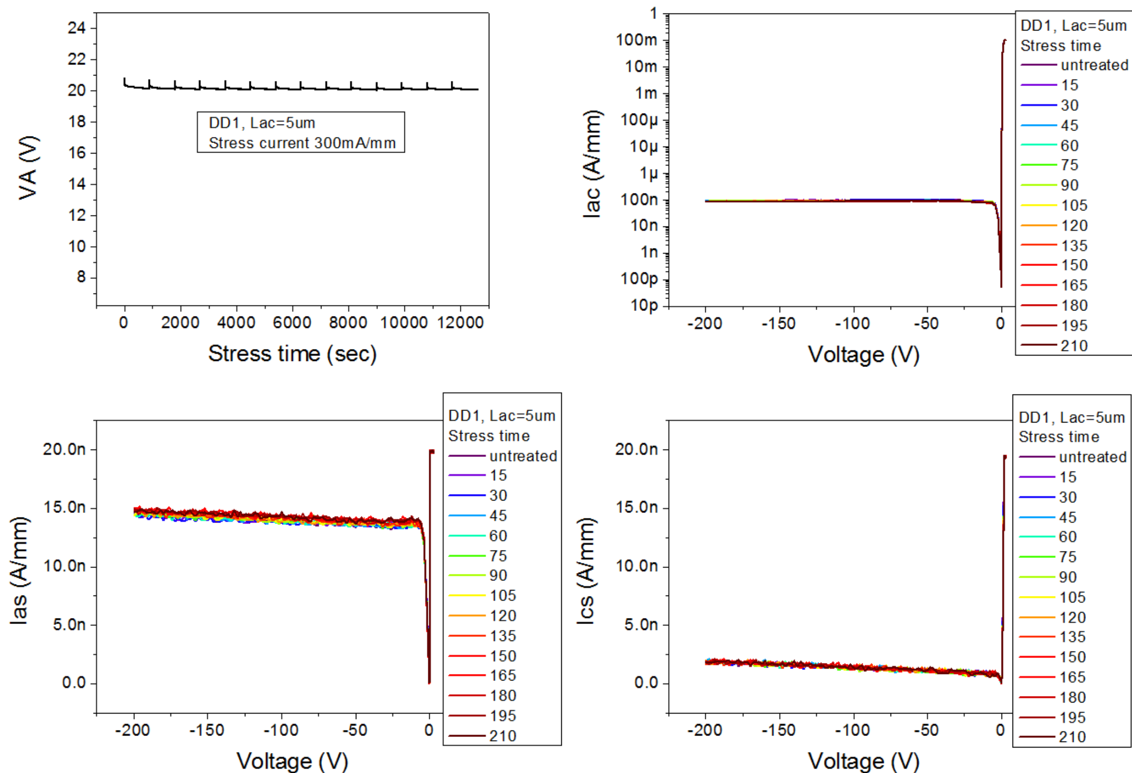


Figure 6.97: Constant current stress at 300 mA/mm.

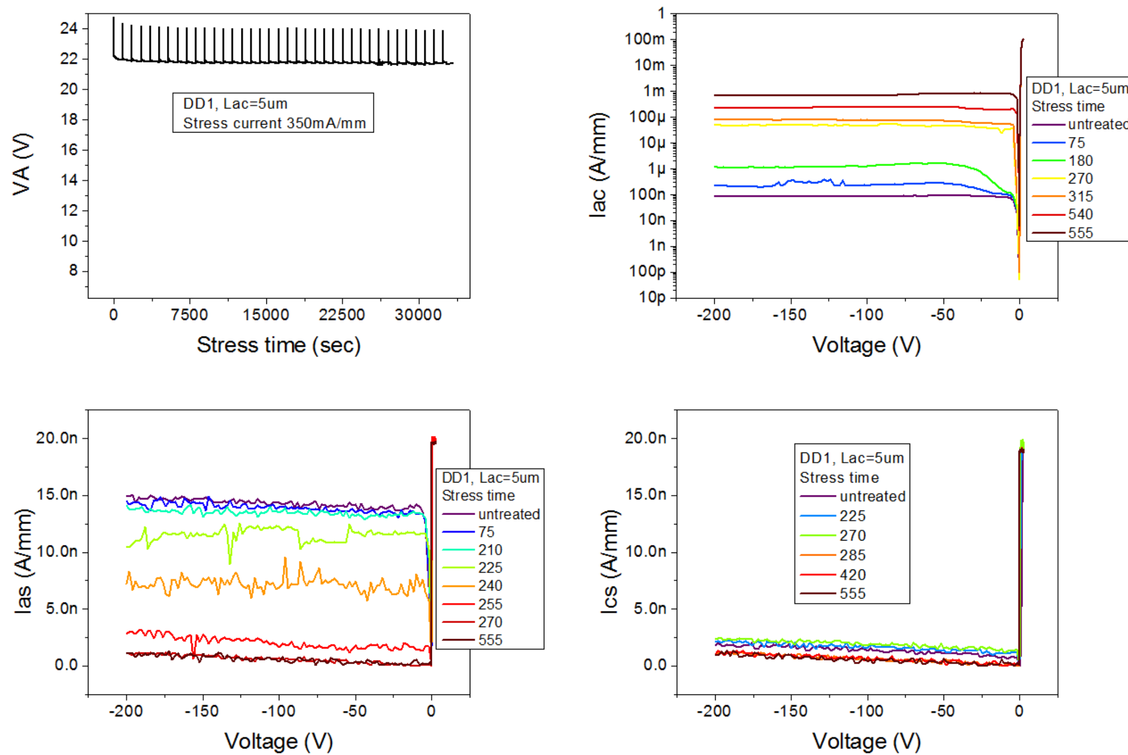


Figure 6.98: Constant current stress at 350 mA/mm.

Figure 6.99 reports the variation of the various currents during the stress. Stressed at 350 mA/mm (7.7 W/mm), the diode reverse current increases with no decrease of the forward-bias performances. Moreover, it was found a possible relationship with the degradation of the diodes towards the substrate.

6.12 Metal - Insulator - Semiconductor transistors

The performances of a HEMT are still limited by two issues: the high electric fields under the gate, which can lead to the premature breakdown of the device, and the leakage current through the gate, which gives an unwanted power dissipation and can fill some trap levels. A possible solution consists in the use of an insulating layer under the gate (typically an oxide or an extension of the passivation), which can lower the gate current due to the increase of the barrier and allows for the reduction of the peak electric field [161]. Moreover, the insulator has been found to improve the performances of the device when trapping effects and dynamic performances are taken into account [138, 162]. These devices are called Metal - Insulator - Semiconductor

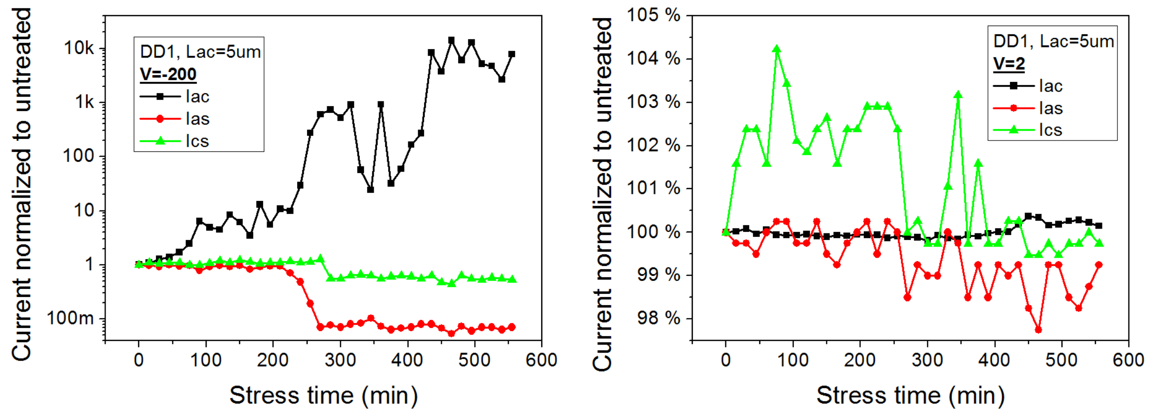


Figure 6.99: Variation kinetics of various currents: anode - cathode (Iac), anode - substrate (Ias) and cathode - substrate (Ics).

transistors (MIS).

The devices under test probably suffer from a non-perfect deposition of the insulating passivation layer. As can be seen in figure 6.100, after some measurements showing the expected device behavior, they exhibit a gate - channel short or anomalous values of the gate current, appearing abruptly at high reverse gate bias. Subsequent measurements take the device back to the usual values, with no further abnormal functioning. This can be explained by the probable creation of conductive paths through the insulator, which can short-circuit the gate - channel region. Since those are parasitic and unstable regions, the current flow can destroy them, bringing the device back to its usual operating behavior.

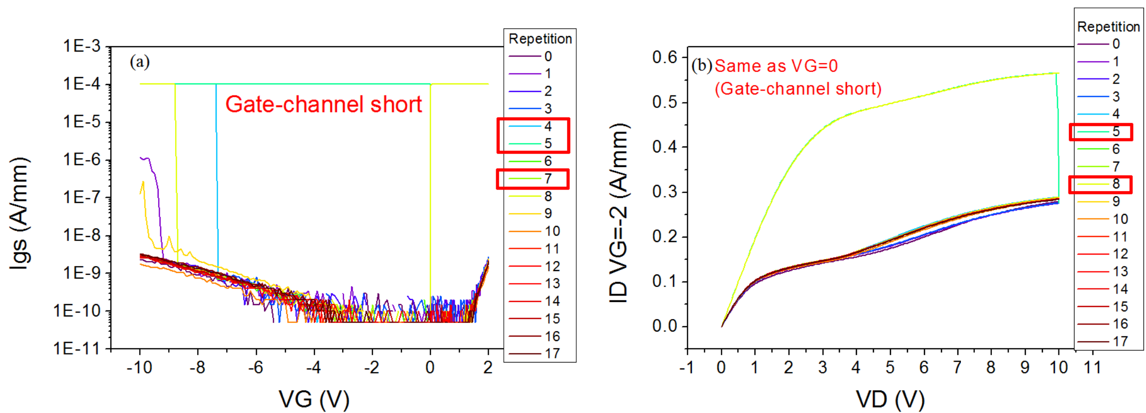


Figure 6.100: Repeated (a) gate diode and (b) output characteristic of a MIS showing abnormal behavior.

Conclusions

Within this work has been presented an extensive discussion on the characterization and reliability aspects of devices for optoelectronics and power electronics applications.

The tests carried out on Light Emitting Diodes and Laser Diodes have shown various effects.

- The irradiation with highly-energetic protons and electro-thermal accelerated lifetime tests cause lattice damage and creation of defects. An higher number of defects gives a decrease of the overall mobility of the material, and an enhanced generation/recombination and/or tunneling current components. Moreover, the defects act as non-radiative recombination centers, producing a drop of the output optical power and (in LDs) an increase of the threshold current.

- The degradation kinetic is dependent on the square root of the stress time, as in the case of a diffusive process, and by means of DLTS it is possible to extract the activation energy of the deep level that causes the drop of the characteristics. The activation energies can be compared with other reports in the literature to gain further insight on the physical cause of the defect.

- Annealing carried out at high temperature (150 °C) is able to restore some atoms in their original position in the lattice, repairing some of the damage and recovering part of the original performances.

- During the stress, it is possible to have an initial improvement of the devices, due to the activation of the p-type dopant. Residual Mg atoms in an interstitial position are moved to a substitutional position thanks to the flow of minority carriers and to the effect of temperature.

A large part of the research activity has been carried out on different aspects of devices for power electronics.

1. Trapping

   - The trapping can occur in both on-state and off-state condition, and its possible effects are the variation of the on-resistance, a modification of the threshold voltage or the creation of a virtual gate. It presence is strongly dependent on eventual filling currents and on the average or peak electric field.
   - The recovery from the trapping can be significantly accelerated by an external temperature, by the illumination with highly energetic photons or by other device-specific effects (gate current injection in GITs). From the temperature - dependent measures it is possible to extract the activation energy of the deep levels involved in the trapping/detrapping mechanism, with an accurate use of the drain current transients technique.
   - Double pulse and drain current transients techniques are not able to give an accurate representation of the behavior of the device in a real application, which is possible to obtain using the gate frequency sweeps.
   - The effect of the substrate voltage has to be accurately considered, since it can cause a great variation of the trapping mechanisms inside the device and a non accurate estimate of the methods to be used for its reduction.

2. Reliability

   - Accelerated lifetime tests can induce the creation of defects in various regions of the device, decreasing its performances. By means of an accurate electrical and optical characterization it is possible to locate the most critical parts.
   - Step-stresses can give information on the maximum operating condition of the devices and useful indications on how to improve them. It is possible to track the increase of the defects during the test and to analyze the effect of the field plates on the dynamic response and the reliability.

3. Additional effects

    - The thermal resistance is a critical parameter for the devices, since it can limit their reliability due to poor thermal conduction of the high power dissipated.
    - The robustness is influenced by the quality of the processing, other than the quality of the epitaxy, and/or by the different composition of the gate stack.
    - The deposition of the passivation has to be accurately planned in order to ensure a good insulation and passivating effect.

The presence of the p-type dopant activation both in GITs and in LDs, and the very similar values of the activation energies in different devices and structures confirm that it is important to obtain all the possible information on a material from different points of view and characterization techniques in order to gain a comprehensive knowledge of its behavior, its limits and its possible improvements.

List of Publications

Journals

[1] M. Meneghini, C De Santi, N. Trivellin, K. Orita, S. Takigawa, T. Tanaka, D. Ueda, G. Meneghesso, E. Zanoni, "Investigation of the deep level involved in InGaN laser degradation by deep level transient spectroscopy", *Applied Physics Letters*, 99, 9, 093506-093506-3, 08/2011, doi:10.1063/1.3626280.

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Acronyms

AG	Anode Grounded
AlGaN	Aluminum and Gallium Nitride
AlInGaN	Aluminum, Indium and Gallium Nitride
AlN	Aluminum Nitride
CG	Cathode Grounded
DBR	Distributed Bragg Reflector
DFB	Distributed Feedback
DLTS	Deep Level Transient Spectroscopy
DNA	DNA
DUV	DUV
EBL	Electron Blocking Layer
ELO	Epitaxial Lateral Overgrowth
ESD	ElectroStatic Discharge
FP	Fabry - Perot
	Field Plate
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GFP	Green Fluorescent Protein
GFS	Gate Frequency Sweep

GIT	Gate Injection Transistor
GPIB	General Purpose Interface Bus
HCl	HydroChloric acid
HEMT	High Electron Mobility Transistor
HVPE	Hydrogen Vapour Phase Epitaxy
IEEE	Institute of Electrical and Electronics Engineers
InGaN	Indium and Gallium Nitride
InN	Indium Nitride
InP	Indium Phosphide
ITO	Indium Tin Oxide
JFOM	Johnson's Figure Of Merit
LD	Laser Diode
LED	Light Emitting Diode
LEEBI	Low Energy Electron Beam Irradiation
LL	Laser-like
MBE	Molecular Beam Epitaxy
MEMOCVD	Migration Enhanced Metal-Organic Chemical Vapour Deposition
MIS	Metal - Insulator - Semiconductor transistors
MOCVD	Metal-Organic Chemical Vapour Deposition
MOVPE	Metal-Organic Vapor Phase Epitaxy
MQW	Multiple Quantum Well
NSJ	Natural SuperJunction
PALE	Pulsed Atomic Layer Epitaxy
PMBE	Plasma assisted MBE

QBP	Quiescent Bias Point
SEM	Scanning Electron Microscopy
SETI	Sensor Electronic Technology, Inc.
SiC	Silicon Carbide
SMSR	Secondary Modes Suppression Rate
SRH	Shockley, Read and Hall recombination
TEM	Transmission Electron Microscopy
	Transverse Electric and Magnetic modes
TF-MOCVD	Two-Flow MOCVD
UV	UV
2DEG	Two Dimensional Electron Gas

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