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**Characterization, modeling and reliability
of RF MEMS Switches and Photovoltaic Silicon Solar Cells**

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Abstract

The main goal of this thesis is the failure and reliability investigation of RF-MEMS switches and photovoltaic solar cells. For technical developer people the reliability issue is often consider a secondary problem in electronic devices since it is not considered an important factor in the production chain. This concept is changing is the last years because reliability studies are considered an important technological step to improve the production process. This fact is confirmed by the investments that companies adopt to test their products. In the particular case of this thesis, we can easily mention the solar cell production line where the cells are subjected to reliability tests that extrapolate the efficiency and the fill factor in order to study the performances and to consequently improve the production process.

Concerning RF MEMS

Wireless communication systems for space applications require electronic components with a high level of reliability, a low power consumption and they should be as small as possible in order to be better integrated in satellites. Radio Frequency Micro Electro Mechanical System (RF-MEMS) can be considered one of the best candidates to comply with previous requirements and, under certain conditions, they can completely replace an entire solid state circuit [1]. RF-MEM devices in general are characterized by a good miniaturization, an easily integration in a standard solid state circuit, an almost zero power consumption, a good RF linearity and a high quality factor Q [2].

Concerning RF-MEMS switches RF performances, they exhibit a very low insertion loss, lower than 0.1 dBm up to 60 GHz and, at the same time, a good isolation, more than 20 dBm. From an electrical and mechanical point of view the power consumption of these switches is close to zero because of an “on-state” current around pA and they are almost unaffected by high level of acceleration or deceleration because of their mass that is extremely small. The possibility to integrate the production of these devices in the standard foundry silicon pro-

cesses and their integration with mature semiconductor technology are a great advantage for their spread making possible to produce them in an easy and cheap way.

Over the last 10 years important developments on MEMS switches have been done all over the world. As a matter of fact, these switches are quite attractive since they combine excellent RF performances and low power consumption of mechanical switches with the small size and low weight of semiconductor devices. However, the appearance of MEMS switches on the market has been hindered by the need for specific packaging [3] as well as by reliability issues [4]. Reliability is a major issue for any satellite since it is almost impossible to envisage any repair work once the spacecraft has been launched. Hence, reliability is a key driver when designing any RF equipment. If we consider a RF-MEMS switch, we have to guarantee that his electromechanical performances will be the same after an intensive usage in harsh environment, for instance after millions or billions of cycles and after the exposure to different kind of radiations. In case of their application in a redundancy scheme, they have to be completely operative even after a long period of activity or inactivity.

The aim of this thesis is to perform an electrical characterization and several reliability tests on different kind of RF-MEMS switches in order to analyze which are the weaknesses and the strengths of this new technology. Electrical characterizations have been done using two different measurement systems. The first, based on a vector network analyzer and a power supply, has been used to test the RF performances of the devices and to extract the actuation and deactuation voltages. The second set up, based on the internal RF signal generator of the VNA, an 8-GHz digital signal oscilloscope and a profilometer (polytec MSA 500), has been used to characterize the electrical performances like actuation time, release delay and dynamic performances.

Cycling stress, one of the most common test used to understand the robustness of this kind of devices, has been performed on different topologies of switch in order to better understand how some parameters of the RF MEMS switch, such as the shape of the beams or the actuation voltage, impact on the reliability of the device. Furthermore, the influence of continuous actuation stress on the reliability of dielectric-less switches has been investigated, comparing different designs and studying the variation of the main electrical parameters induced by the stress and the successive recovery phase.

Concerning PV solar cells

A solar cell, or photovoltaic cell, is an electrical device that converts the

energy of light directly into electricity by the photovoltaic effect. The operation of a photovoltaic (PV) cell requires 3 basic attributes: (i) the absorption of light, generating either electron-hole pairs or excitons, (ii) the separation of charge carriers of opposite types and (iii) the extraction of those carriers to an external circuit [5].

Over the last decades, many research groups have tried to improve the conversion processes in order to increase the efficiency of solar cells and to reduce the parasitic effects that limit the energy conversion. This has generated a real challenge to the best conversion efficiency. The average efficiency of multicrystalline silicon solar cells at the beginning of 2014 was about 16% but in research labs different solar cells have exceeded the 20% [6] with records over 24% [7]. The continuous growth of the solar cells efficiency has been achieved thanks to the reliability study of the single cells and to the degradation analysis of the real photovoltaic systems. These studies have revealed the critical points of PV solar cells and have led to a constant improvement of the production processes.

The aim of this thesis is the study of the reliability problems related to a single solar cell and to a string of solar cells subjected to different illumination conditions. Different characterization procedures have been developed in order to study the failure mechanisms and to study the weaknesses and the strengths of the technology. Four types of measurement set-ups have been utilized: (i) the first system is able to extract the IV curves in dark and light conditions. This simple measurement procedure has to be opportunely calibrated in order to obtain right results in term of efficiency and fill factor. (ii) The second system extracts the thermographic image of a single solar cell. It can be used to analyze hot spot and other failure mechanisms in the silicon structure. (iii) The third system extracts the electroluminescence and the photoluminescence of a single solar cell. It is able to extract and analyze the defects in the crystalline structure of the materials. (iv) The fourth is the LOANA system: a commercial tool able to extract the External Quantum Efficiency and the Internal Quantum Efficiency with the measurement of the reflectance [8].

All these characterization procedures have been utilized to study the evolution of the failure mechanisms when a single solar cell is subjected to reverse biasing stresses. The study of the catastrophic degradation of solar cells submitted to reverse current stress is of crucial importance since the failure can lead to the rapid increase of the temperature with a consequent risk of fire and to the breaking of the entire PV system. This particular situation can occur when the PV system is not uniformly illuminated and the solar cells of the system

present not uniform shunt resistance. Additional studies have been performed in the modelization of a solar cell with the two diode model. The study and modeling of solar cells allows to obtain right results in term of efficiency and fill factor extrapolation. Moreover, the modelization allows the study of string of solar cells working in particular conditions in which the illumination level is not uniform in a whole panel. The simulations allows to predict the dangerous situations and to design appropriate prevention systems.

Sommario

Lo scopo principale di questa tesi è investigare i meccanismi di rottura e l'affidabilità di interruttori RF MEMS e celle solari. I problemi affidabilistici sono spesso considerati dagli sviluppatori un problema secondario nei dispositivi elettronici dal momento che non sono considerati un fattore importante nella catena produttiva. Questo concetto sta cambiando negli ultimi anni visto che gli studi affidabilistici stanno diventando uno step tecnologico per migliorare i processi produttivi stessi. Questo fatto è confermato dagli innumerevoli investimenti che le aziende stanno elargendo per testare i loro prodotti. Nel caso particolare di questa tesi possiamo facilmente menzionare la linea produttiva di una cella solare dove le celle sono soggette a test di affidabilità che estrapolano l'efficienza e il fill factor. Questo permette di studiare le prestazioni delle celle e di conseguenza di migliorare il processo produttivo.

Interruttori RF MEMS

I sistemi di comunicazione Wireless per applicazioni spaziali richiedono componenti elettronici con un alto livello di affidabilità, un consumo di potenza basso e un'occupazione di spazio ridotta in modo da essere integrati in un satellite. Gli interruttori microelettromeccanici (RF-MEMS) possono essere considerati per sostituire i dispositivi meccanici attuali e, in determinate condizioni, possono sostituire un intero circuito a stato solido [1]. I dispositivi RF MEMS in generale sono caratterizzati da un'ottima miniaturizzazione, una buona capacità di integrazione nei circuiti a stato solido, un consumo di potenza quasi nullo, una buona linearità e un alto fattore di qualità Q [2].

Riguardo le prestazioni, gli interruttori RF MEMS presentano una bassa perdita per inserzione, minore di 0.1 dBm fino a 60 GHz e, allo stesso tempo, un buon isolamento, maggiore di 20 dBm. Dal punto di vista elettromeccanico il consumo di potenza è vicino allo zero a causa della corrente di "on-state" vicina ai picoAmpere. Inoltre questi dispositivi non risultano disturbati dagli alti livelli di accelerazione e decelerazione (a causa della loro massa molto piccola). La pos-

sibilità di integrare la produzione di questi dispositivi nei processi standard di lavorazione del silicio e l'integrazione con tecnologie al silicio ormai mature sono dei grandi vantaggi per la loro diffusione su larga scala e per l'abbattimento dei costi di produzione.

Negli ultimi dieci anni molti miglioramenti sono stati fatti sugli switch MEMS da vari gruppi di ricerca. Gli switch RF MEMS stanno diventando interessanti per le loro prestazioni RF, per il loro basso consumo di potenza, per le piccole dimensioni e basso peso. Nonostante le loro prestazioni, la diffusione sul mercato è stata rallentata per la necessità di package specifici [3] e per i loro problemi di affidabilità [4]. L'affidabilità dei dispositivi RF MEMS è un fattore predominante in applicazioni spaziali dal momento che risulta impossibile qualsiasi intervento di manutenzione una volta che il satellite è stato lanciato. Quindi per applicazioni spaziali l'affidabilità deve essere considerata un fattore dominante nella fase di progettazione di ogni switch MEMS. Infatti dobbiamo garantire che le sue proprietà elettromagnetiche rimangano le stesse dopo un periodo di utilizzo prolungato in ambiente ostile, per esempio dopo milioni o bilioni di cicli e dopo la continua esposizione a diversi tipo di radiazioni. In caso di utilizzo di switch MEMS in schemi di ridondanza, devono essere completamente funzionanti anche dopo un lungo periodo di attività o inattività (mesi o anni).

Lo scopo di questa tesi è di effettuare caratterizzazioni di tipo elettrico e diverse tipologie di stress di affidabilità su switch RF MEMS in modo da studiare la tipologia di dispositivo più promettente e robusta. La caratterizzazione elettrica è stata eseguita utilizzando due diversi sistemi di misura. Il primo, basato su un "Vector network analyzer" e alimentatori, è stato utilizzato per verificare le prestazioni RF dei dispositivi ed estrapolare le tensioni di attuazione e disattuazione dei singoli dispositivi. Il secondo sistema di misura, composto dal generatore interno del "Vector network analyzer", da un oscilloscopio digitale con banda di 8-GHz e un profilometro ottico (polytec MSA 500), è stato utilizzato per caratterizzare le prestazioni elettriche e meccaniche come il tempo di attuazione, il ritardo introdotto in fase di rilascio e le prestazioni dinamiche dei dispositivi.

Lo stress di tipo "Cycling", uno dei test di affidabilità più comuni usato per comprendere la robustezza dei dispositivi, è stato eseguito su differenti tipologie di dispositivi per comprendere come le caratteristiche intrinseche (per esempio la forma del ponte mobile) possano impattare sull'affidabilità dell'interruttore stesso. Oltre a stress di tipo "Cycling" si è studiato l'influenza di stress di attuazione prolungata sull'affidabilità di interruttori senza dielettrico, comparando

differenti design e studiando la variazione dei parametri elettrici indotti dallo stress prolungato e dalle successive fasi di rilassamento dei dispositivi.

Celle Solari

Una cella solare, o cella fotovoltaica, è un dispositivo elettronico che converte l'energia della luce direttamente in energia elettrica attraverso l'effetto fotovoltaico. Il funzionamento delle celle fotovoltaiche richiede 3 principi di base: (i) l'assorbimento della luce, generando coppie elettrone lacuna, (ii) la separazione delle cariche generate e (iii) l'estrazione di queste cariche attraverso un circuito esterno opportunamente dimensionato [5].

Nelle ultime decadi molti gruppi di ricerca hanno provato ad incrementare il processo di conversione in modo da aumentare l'efficienza delle celle solari e ridurre così gli effetti parassiti che limitano il processo di conversione dell'energia. Tutto questo ha generato una vera e propria corsa alla migliore cella fotovoltaica in termini di efficienza di conversione. L'efficienza media di una cella solare multicristallina all'inizio del 2014 era di circa il 16% ma in alcuni laboratori di ricerca molte celle solari superavano il limite del 20% [6] con record superiori al 24% [7]. La continua crescita dell'efficienza delle celle solari è stata possibile anche grazie agli studi affidabilistici sulla cella solare singola e agli studi eseguiti sui meccanismi di degrado dei sistemi fotovoltaici esistenti. Questi studi hanno permesso di identificare i punti critici delle celle solari e hanno portato ad un costante aumento di prestazione dei processi produttivi.

Lo scopo di questa tesi è lo studio dell'affidabilità delle singole celle fotovoltaiche e di stringhe di celle sottoposte a differenti livelli di illuminazione. Diverse procedure di caratterizzazione sono state sviluppate per studiare i meccanismi di rottura e per studiare i punti di forza e i punti deboli di questa tecnologia. Quattro diversi sistemi di misura sono stati utilizzati: (i) il primo sistema è in grado di estrapolare le curve corrente tensione al buio e in condizione di illuminazione di una singola cella fotovoltaica. Questo sistema di misura apparentemente semplice deve essere opportunamente calibrato in modo da ottenere risultati corretti in termine di efficienza e fill factor. (ii) Il secondo sistema di misura permette di estrarre l'immagine termografica di una singola cella fotovoltaica. Può essere utilizzato per analizzare la presenza di "hot spot" e altri meccanismi di rottura nella struttura cristallina della cella solare. (iii) Il terzo sistema permette di estrarre l'elettroluminescenza e la fotoluminescenza di una singola cella solare. Questo sistema permette di analizzare la presenza di difetti nella struttura cristallina della cella stessa. (iv) Il quarto sistema di misura è il sistema commerciale LOANA (PVTools): questo strumento permette di estrarre

l'efficienza quantica esterna e interna attraverso misure di riflettività [8].

Tutte questi sistemi di misura sono stati utilizzati per studiare l'evoluzione dei meccanismi di rottura quando una singola cella fotovoltaica viene sottoposta a stress in polarizzazione inversa. Lo studio della rottura catastrofica di una cella solare sottoposta a stress in polarizzazione inversa è di cruciale importanza dal momento che la rottura di una singola cella può portare ad un aumento repentino della temperatura con conseguente rischio di incendio e rottura dell'intero sistema fotovoltaico. Questa particolare situazione può accadere quando un pannello fotovoltaico non è illuminato in modo uniforme e le singole celle fotovoltaiche presentano resistenza di "shunt" non uniformi in un singolo pannello. Studi addizionali sono stati eseguiti nella modellizzazione di una singola cella solare con il modello a due diodi. Lo studio e la modellizzazione di una cella solare permette di ottenere risultati corretti in termini di efficienza e fill factor. Inoltre la modellizzazione permette lo studio di stringhe di celle solari che lavorano in particolari condizioni di illuminazione non uniformi all'interno di uno stesso pannello fotovoltaico. Le simulazioni permettono di predire situazioni potenzialmente dannose e quindi di prevedere opportuni circuiti di protezione.

Chapter 1

RF-MEMS Switches, Manufacturing and Design

1.1 MEMS Switch Fabrication Technologies

The fabrication process for RF MEMS switches implemented for the devices is a ten-mask process, and is a modified and improved version of an eight mask process based on surface micromachining techniques and standard CMOS type processing sequences that has been developed and stabilized during the last years at FBK-irst in order to get a stable technology platform.

In Fig. 1.1 a conceptual process cross section is shown, which summarizes all structural elements provided by the process. The basic elements, that allow

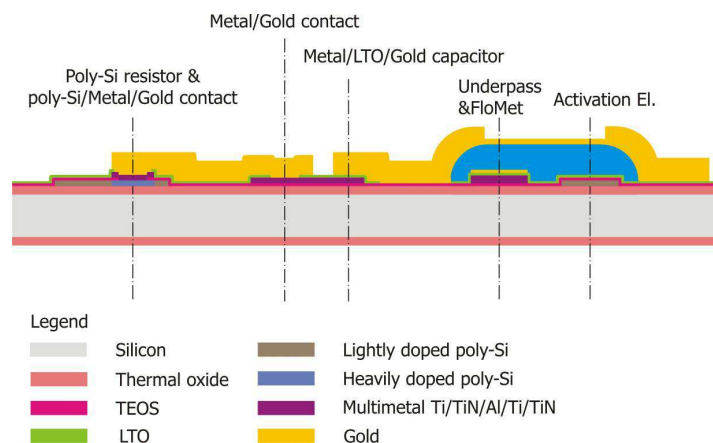


Figure 1.1: Conceptual cross-section of the basic device structures provided by the RF-switch process.

the fabrication of series and shunt type electrostatic actuated MEMS switches, are mobile metallic bridges, either clamped beams or cantilever beams, together with high resistive poly-silicon actuation pads and optional high value resistors and DC blocking capacitors. The air-bridges and movable bridges are realized without the need for a planarization step, utilizing two electrodeposited gold layers of different thickness which are also used for the realization of the coplanar waveguides. A third gold layer is used for the realization of low resistance metal-to-metal electro-mechanic contacts for series ohmic switches and floating electrodes for shunt switches.

The first batch fabricated for this project is the batch number 23 realized with this technology at FBK-irst and is therefore labelled RFS23. The flow of the base line fabrication process can be summarized in Fig. 1.2. The substrates for the switch process are p-type, $\langle 100 \rangle$, $500 \mu\text{m}$ thick, $5 \text{ k}\Omega\text{cm}$ high resistivity silicon wafers from TOPSIL. Some standard silicon wafers were added for the usual electro-mechanical in-house testing.

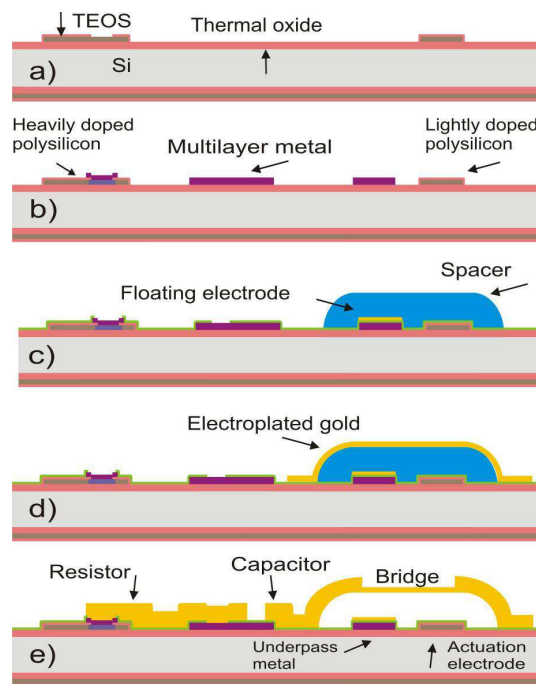


Figure 1.2: Schematic process flow of the 10 mask base line switch process.

a) As a first step alignment markers were etched on the wafers with a standard alignment mask. Then a 1000 nm thick thermal oxide was grown as an isolation layer. In order to reduce the fixed oxide charge the oxide was then annealed at 975°C in nitrogen for one hour. Next a 630 or 400 nm thick un-doped poly-silicon

layer was deposited by LPCVD at 620 °C and slightly doped with boron by ion implantation (BF_2 120 keV 6.2×10^{14} atoms/cm²). Then the area for heavy implant was defined and a second implantation was performed (BF_2 120 keV 5×10^{15} atoms/cm²). At this point the resistors and actuation electrodes were defined. The poly-silicon layer was selectively etched by a plasma etch process and the previous implanted boron was diffused at 925 °C for 1 hour in nitrogen, which normally provides a final sheet resistance for the poly-silicon of around 1700 Ω/\square for the lightly implanted regions and around 150 Ω/\square for the heavily implanted regions. Next a 300 nm thick silicon oxide layer was deposited from TEOS at 718 °C by a LPCVD process that provided the high isolation needed for the actuation electrodes. Contact holes were then defined and etched by a plasma process.

b) After photo mask ashing, the multilayer underpass metal was deposited by sputtering. First 30 nm of Ti and 50 nm thick TiN were deposited at 400 °C. Next a 410 nm thick Al 1%Si alloy and 60 nm thick Ti layers were deposited at room temperature. Finally an 80 nm thick capping layer of TiN was deposited at 300 °C to obtain a diffusion barrier between metal and gold. The total thickness of the multilayer was calculated in order to have the same height of the polysilicon, compensating the change of oxide thickness due to dry etching too. This metallization scheme provides at the same time a high conductive metal layer and a diffusion barrier for gold. The multilayer metal was then defined and dry etched.

c) Next the multilayer was covered with 100 nm of low temperature oxide (LTO). The vias in the LTO have been defined by masking and dry etching. The etch time has been calculated in order to remove the TiN capping of the multilayer metal and to expose the underlying aluminum layer. Immediately before the metallization steps the wafers underwent a vias cleaning step based on a dip in Aluminum-etch at room temperature, which removes the native oxide on the aluminum. Next a 5 nm thick Chromium adhesion layer followed by a 150 nm Gold layer were deposited by PVD. This Cr/Au layer was defined by lithography and wet etched. Main purpose of this layer is to cover with a noble metal the exposed electrical contacts of the series ohmic switches in order to provide low resistive electrical contacts. This layer can also be used to build a floating electrode for the shunt switches. In agreement with the design rule this layer has to cover all the vias, which allows to simplify the process flow and provides a more uniform and controlled via resistance. For lowest contact resistance values down to very low frequencies an anneal in nitrogen at 300 °C

for 30 min is then performed. The sacrificial layer for the definition of the air gap is then realised by a 3 μm thick patterned photo resist.

d) As a seed-layer for electrochemical Au deposition a 2.5/25/2 nm thick Cr/Au/Cr layer will be deposited by e-gun evaporation. The second Chromium layers acts as adhesion layer for the photoresist. The movable air bridges will be defined using a 5 μm thick positive resist. After an exposure to oxygen plasma at 80 °C and chromium layer removal a 1.8 μm thick gold layer will be selectively grown in a commercial gold cyanide bath (Aurolyte CN 200 from Atotech). The electroplating parameters have been chosen in order to achieve a uniform thickness and a smooth surface finish.

e) The first plating mask will then be removed with a solvent and the CPW lines and anchor posts for the movable air bridges will be defined with 5 μm thick positive resist. Again the wafers will be exposed to oxygen plasma at 80 °C and then a 3.5 μm thick gold layer will be selectively grown. The last plating mask and the seed layer will then be removed by wet etch. The seed layer removal will be completed by a second fast dip in Au-etch just after chromium etching in order to remove all possible residuals, followed by a 20 s dip in HF 0.8% to definitely clean the underlying oxide. At this point a sintering in nitrogen at 190 °C for 30 minutes will be performed in order to provide the gold layers with the appropriate tensile stress. In order to be diced the wafers will be coated with a 1.2 μm photoresist layer and pre-diced with the dicing saw, i.e. the wafers are diced about half way through. This allows handling the wafer still as a whole during the next step while the dies can be easily separated by breaking along the pre-diced scribe-lines. Finally the air bridges will be released with a modified plasma ashing process (typically 20 minutes at 200 °C, in steps of 5 minutes).

1.1.1 Modified Flomet and second Flomet

This splitting has been introduced with the purpose to increase the hardness on the contact material, that is, of the floating metal layer. For the same reason an additional flomet layer, made with the same material has been introduced above the spacer, as depicted in fig. 1.3.

The choice of the alternative material has been deeply investigated before the beginning of the fabrication cycle. Indentation measurements were performed on different samples, in order to determine the hardest material to be used. The general approach was to have a layered structure, with gold as main component, in order to preserve the useful chemical properties of this metal. The structure of the

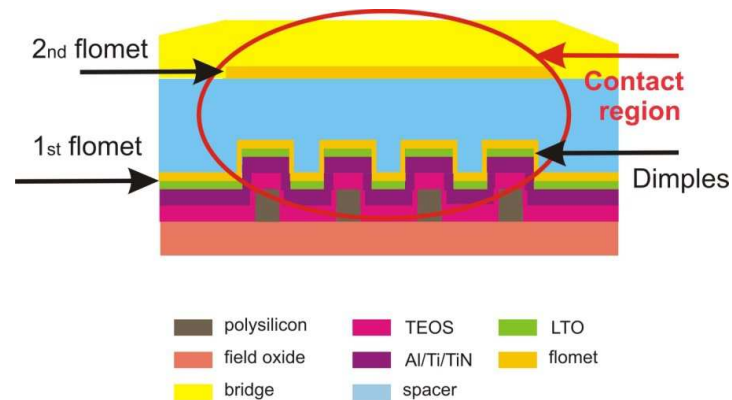


Figure 1.3: Structure of the contact region in ohmic switches with second floating metal.

multilayer is schematically depicted in Fig. 1.4. As alloying material chromium, palladium and platinum were tested. Chromium has been ruled out in spite of its good process compatibility because it was found that the increased hardness achieved by the layered structure was lost during the final release step, due to chromium oxidation. The final choice was platinum as alloying metal, because the increase of hardness was good especially after anneal, and the effect of final release was not relevant. An option that has not been explored is ruthenium as alloying metal. This last metal is very successful in increasing the hardness of the alloyed contact material, however this may not be enough to improve the real quality and reliability of the contact. In particular, in the literature, it is made clear that relevant percentages of alloying metal diminish the maximum number of cycles before the contact resistance starts to increase because of surface contamination. At low alloying concentration, ruthenium is not increasing hardness more than platinum. From our processing experience, we have also another reason to discard ruthenium as gold alloying material: all devices have necessarily to undergo the final plasma oxygen treatment to be released. This treatment is strongly oxidizing and few metals can survive it without being oxidized. The metal oxide is formed on the gold external surface, as a contaminating and insulating layer. From the metal we tested, chromium and palladium, when present in the multilayer material, are readily found on the gold external surface, but the same does not happen for platinum, because of its oxidation resistance. From its chemical properties it is very likely that ruthenium can build an insulating layer on the gold top, giving the same problems detected for palladium and chromium. On the other hand, a single platinum layer of 3 nm thickness cannot stop the

chromium adhesion layer diffusion, but strongly reduces the contact roughness after plasma ashing. Finally it should also be considered that the contact forces in microcontacts like those used in RF MEM switches are orders of magnitude lower than those present in macroscopic switches, which makes these devices particularly sensible to the oxidation of the contact surfaces.

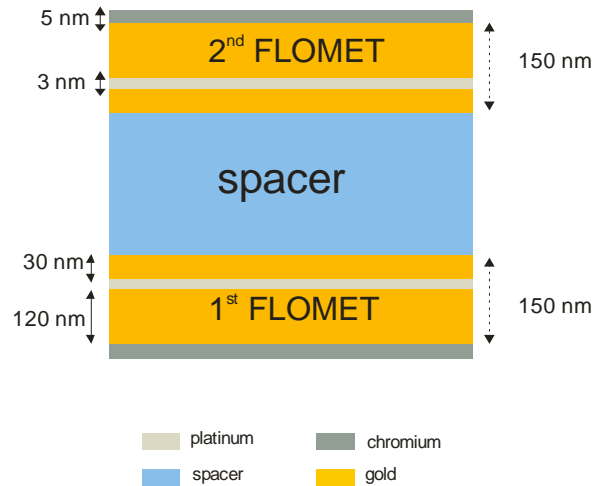


Figure 1.4: Structure of the multilayer dimples.

1.1.2 Low temperature release

This process variation has been developed during this fabrication cycle after a long study on test wafers with only the electromechanical gold part. The crucial point of this splitting is that keeping the release temperature sufficiently low, most of the unwanted mechanical deformations are avoided in the final suspended gold membrane. This happens because during the normal release process at 200 °C the difference in thermal expansion coefficients between gold and silicon produces deformations in the gold membrane that are not reversible when the structure comes back to ambient temperature. The low temperature release (at 90 °C) can avoid these deformations, leading to a very flat membrane. The drawback of this process is its extremely long time duration compared with the normal release, (5 to 6 hours instead of 20 minutes), because the asher etch rate is extremely sensitive to temperature. Other release temperatures, between 90 and 200 °C, have not been tested yet, but we are planning to do it in order to reach a satisfying compromise between planarity and release time.

1.2 Design of RF MEMS Switches

1.2.1 B type switch

The B-type switch is a shunt capacitive switch with enhanced C_{ON}/C_{OFF} ratio. It consists of a clamped-clamped membrane realized by using only the BRIDGE layer. A micrograph of the switch is reported in Fig. 1.5, and Table 1.1 reports the geometric dimensions of the device. The dielectric-less version of such a typology was investigated in accordance to the results from the reliability tests.

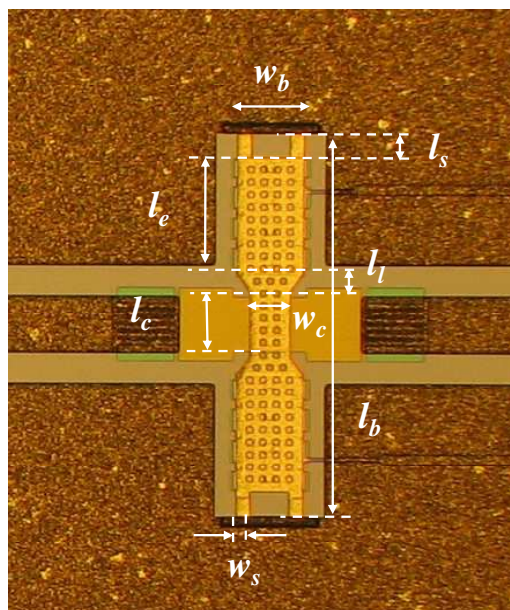


Figure 1.5: Micrograph of the RF MEMS capacitive switch (“B-type”) with enhanced capacitance ratio.

The electromechanical properties of such a device have been deeply analyzed by using ANSYS Multiphysics software. The settings used for the simulation are reported in Table 1.2. Pull-in simulations have been performed by using the electro-mechanical direct coupling elements TRANS126. The structural properties have been modeled by exploiting the multilayer functionalities of the 20-nodes SOLID186 structural elements. As a result, for a gold layer of thickness $t_b = 2\mu\text{m}$ and a residual stress of $\sigma_0 = 60\text{MPa}$, the simulated actuation voltage is 45 V, pretty much close to the average measured pull-in voltage.

The membrane results quite planar after the release process. However, it was observed a slight initial deformation in some samples, which actually does not affect significantly the electromechanical properties of the switches. Such a

Table 1.1: Geometrical dimensions of the B-type switch

Membrane length (l_b)	620 μm
Electrode length (l_e)	185 μm
Central membrane length (l_c)	110 μm
Lever length (l_l)	30 μm
Membrane width (w_b)	100 μm
Central membrane width (w_c)	60 μm
Spring length (w_l)	30 μm
Spring width (w_s)	15 μm
Membrane thickness (t_b)	2 μm

Table 1.2: Material properties and settings used for the finite element simulations in ANSYS.

Structural element type	SOLID186 Multilayer
Gold Young Modulus	75 GPa
Gold Poisson's ratio	0.42
Electromechanical element type	TRANS126
Contact element type (pillars)	CONTA174/TARGE170
Reference temperature	300 K
Residual Stress	60 MPa
Stress gradient	0-12 MPa/ μm

deformation is not present when the samples are released with a low temperature process, so it is due basically to the presence of a stress gradient.

Such a situation was reproduced by using finite element simulations. Fig. 1.6 a and b report the initial membrane deformation with or without the stress gradient Γ_s . When the stress gradient is applied, it is chosen equal to 12 MPa/ μm , which is the measured average value. Fig. 1.6 c reports instead the deformed membrane after the application of a bias voltage V_B equal to 60 V.

In some measured samples, the membrane remains stuck after the application of a high bias voltage (> 80 V). As it can be seen from Fig. 1.7 a, the stiction occurs on the bias electrode because of an electric short between the polysilicon pad and the gold bridge collapsed among the stoppers. The gap-distance simulation reported in Fig. 1.7 b is helpful to explain what probably occurs. For high bias voltage, the membrane is not ideally flat but its deformed shape slightly follows the pillars disposition. In addition, the process uncertainties can provide a pillar-

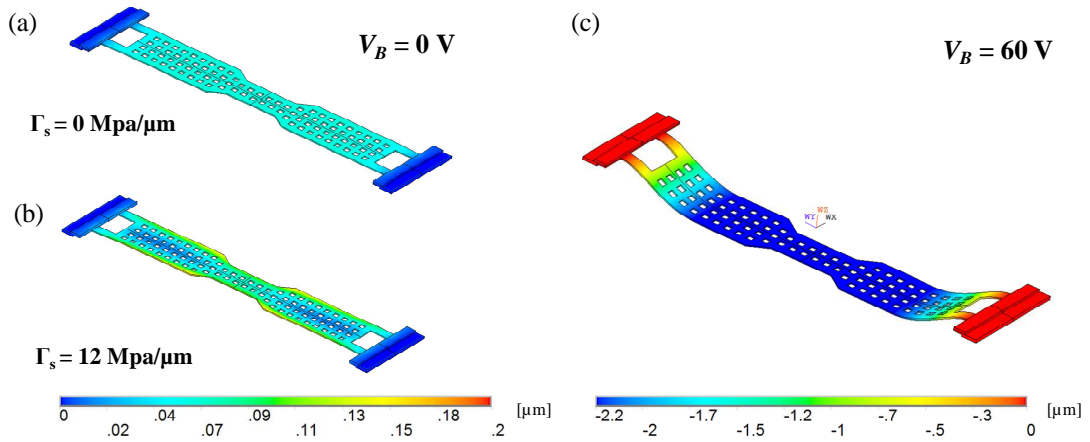


Figure 1.6: Finite element displacement solutions of the B-type capacitive switch : (a) at $V_B = 0$ V and no stress gradient, (b) at $V_B = 0$ V with a stress gradient of 12 MPa/ μ m and (c) at $V_B = 60$ V. After the actuation the membrane deformation is pretty similar with or without considering stress gradient, so only the case with no stress gradient is reported.

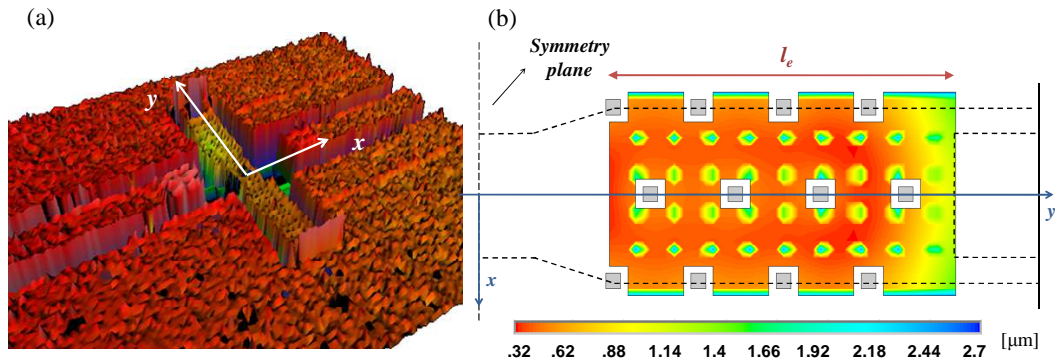


Figure 1.7: (a) Optical profiler image of a B-type switch stuck on the bias electrode (not-reversible stiction), and (b) simulated residual gap distance for $V_B = 60$ V.

electrode height difference which is lower than the nominal value of 550 nm set by design. Consequently, electric discharges can occur leading to the situation observed and reported in Fig. 1.7 a.

1.2.2 B OPT type switch

The B-type capacitive switch can be re-designed and optimized from both a electro-mechanical and RF point of view by exploiting the knowledge acquired

from measurements and FE modeling results. A preliminary consideration concerns the usage of the available gold layers. A frame of CPW layer can be designed in order to improve both the planarity of the membrane in its down state and avoid an excessive membrane deformation at high bias voltages. The CPW frame can be designed all over the length of the membrane except than the anchor springs. Since this solution affects the membrane stiffness, the anchor springs can be redesigned longer than they are in the current version in order to decrease the pull-in voltage. However, the design of the CPW frame can be critical in terms of the stress relaxation after the release. Thus the re-design will account for the following points:

- The membrane has to be as much flat as possible after the release and also after the actuation.
- The pull-in voltage does not have to exceed 50 V.
- The residual gap between the membrane and the bias electrode after the actuation has not remain close to the nominal value all over the electrode surface, even in case of very high bias voltages.

Fig. 1.8 shows the layout of the novel B-type switch and the corresponding electromechanical simulation for $V_B = 0$ V and 50 V, in case of a stress gradient equal to 12 MPa/ μm . Simulations were performed by using the same settings listed in Table 1.2. The planarity is slightly less than before. However, a full CPW frame or a different length of the CPW rows over the BRIDGE layer would have a worst effect on the planarity because of stress gradient induced by the not-uniform bi-layered cross-section. For this reason, the CPW rows length was chosen by using the Design-Of-Experiment (DOE) and Optimization tools available in ANSYS Workbench. As a result the actuation voltage is around 44 V. The stopping pillars are designed bigger than the ones in the previous version of switch, so the membrane bending among the stoppers is reduced. The geometry dimensions of the new design are listed in Table 1.3.

1.2.3 S type switch

The S-type switch is a series ohmic switch consisting of a clamped-clamped membrane and a couple of lateral “wings” used to establish the contact after the actuation. A micrograph of the manufactured device is depicted in Fig. 1.9 a, while in Table 1.4 the device dimensions are reported. The dielectric-less version

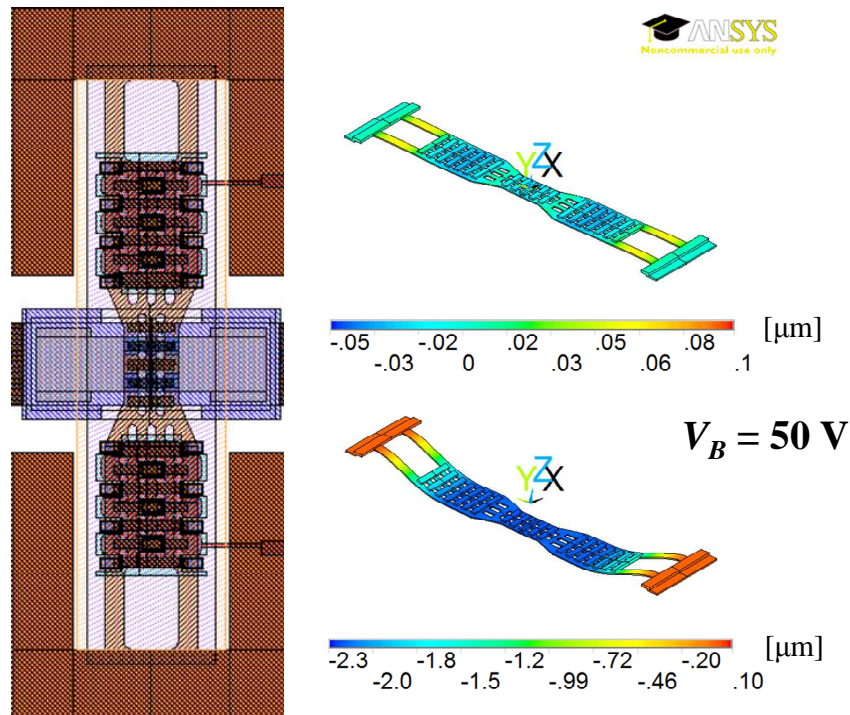


Figure 1.8: Optimized geometry of the B-type switch. As shown by the simulation, the planarity in case of stress gradient is largely increased.

Table 1.3: Geometrical dimensions of the optimized B-type switch

Membrane length (l_b)	620 μm
Electrode length (l_e)	135 μm
Central membrane length (l_c)	80 μm
Lever length (l_l)	50 μm
Membrane width (w_b)	100 μm
Central membrane width (w_c)	60 μm
Spring length (w_l)	90 μm
Spring width (w_s)	20 μm
Membrane thickness (t_b)	2 μm
CPW lateral frame length	80 μm
CPW central frame length	50 μm

of such a typology was investigated in accordance to the results from the reliability tests. The basic idea behind such a structure is the employment of the contact wings (which are basically clamped-free membranes) in order to provide

a contact force on a single dimple which mainly depends on the wing dimensions and deformation Δz and not on the bias voltage (Fig. 1.4 b).

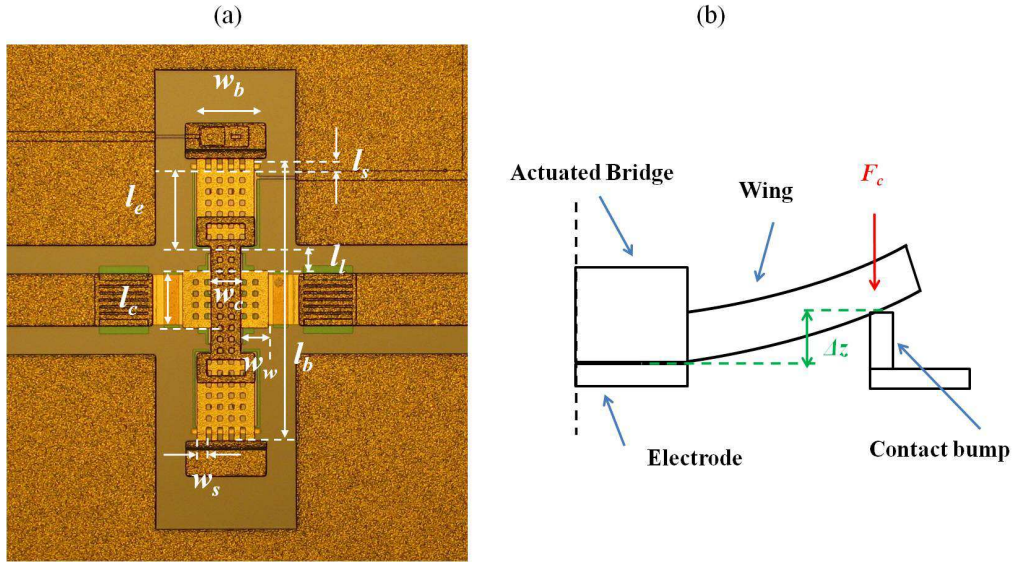


Figure 1.9: S-type ohmic switch : (a) micrograph, and (b) cross section of the contact wing when the switch is actuated.

Table 1.4: Geometrical dimension of the S-type switch

Membrane length (l_b)	500 μm
Electrode length (l_e)	130 μm
Central membrane length (l_c)	50 μm
Lever length (l_l)	45 μm
Membrane width (w_b)	100 μm
Central membrane width (w_c)	50 μm
Wing width	50 μm
Spring length (w_l)	25 μm
Spring width (w_s)	10 μm
Membrane thickness (t_b)	2 μm
Frame thickness (t_f)	3 μm

Finite element (FE) simulation have been performed by using ANSYS in order to reproduce the initial deformation and the contact force. The element types, material properties and settings parameters used for the simulations are the same listed in Table 1.2.

As a result of the structural simulation, after the application of a residual stress $\sigma_0 = 60$ MPa, the suspended membrane appears as reported in Fig. 1.10 a. Then when $V_B = 36$ V the wings touch the contact bumps (Fig. 1.10 b), and finally collapses over the stopping pillars when $V_B = 61$ V (Fig. 1.10 c). Thus there is a “transition region” where the contact force is not stable but changes with the bias voltage. To achieve a stable contact force only depending on wing geometry and displacement, high bias voltage is then needed. The bias voltage corresponding to the membrane collapse on the pillars, when the stable force is achieved, can be considered as the “real” pull-in voltage of the switch.

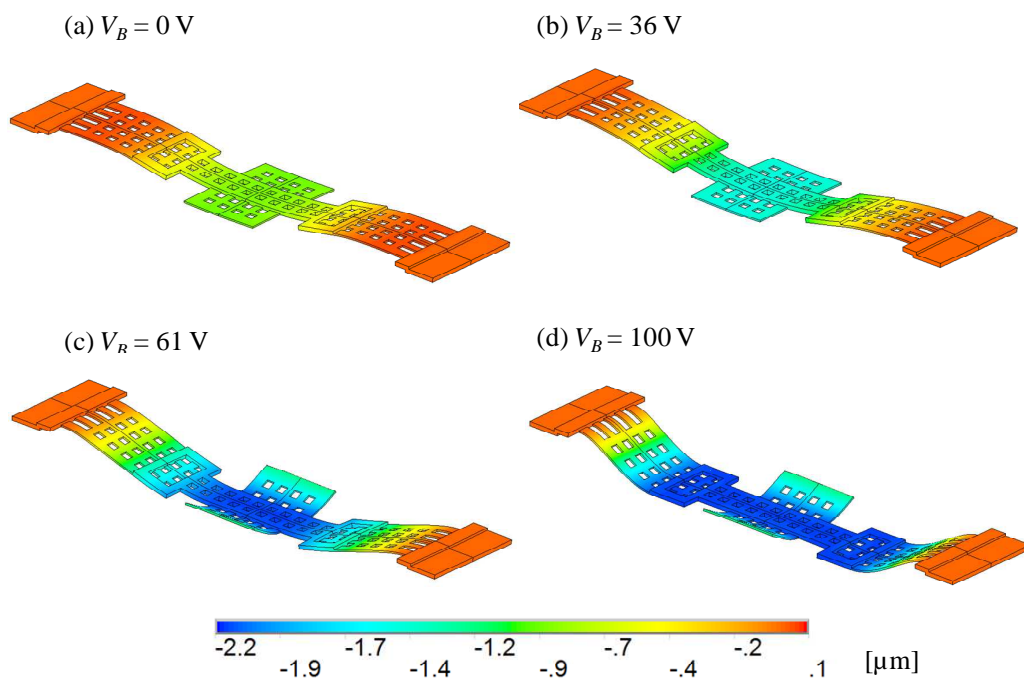


Figure 1.10: FE simulation results of the S-type switch : (a) at $V_B = 0$ V, after the application of a residual stress equal to 60 MPa, (b) at $V_B = 36$ V, when the wings touch the contact bumps, (c) at $V_B = 61$ V, when the air-bridge collapses over the stopping pillars, and (d) at $V_B = 100$ V.

Fig. 1.10 also shows that after the application of the initial stress the air bridge is significantly deformed. The initial deformation is confirmed by optical profiler characterization. In many switch samples the air gap under the wings is initially lower than the one under the anchor springs (typically around 0.9 - 1.3 μm depending on the gold thickness and stress conditions). FE simulations provide a wing z-displacement with respect to the anchor points of about 1.1 μm . This demonstrates that the thicker gold frame over the membrane can significantly

influence the overall bridge deformation, affecting in turn the expected pull-in voltage and also the bridge restoring force (in progress). Fig. 1.11 shows a comparison between the measured and simulated membrane profile along the air bridge length.

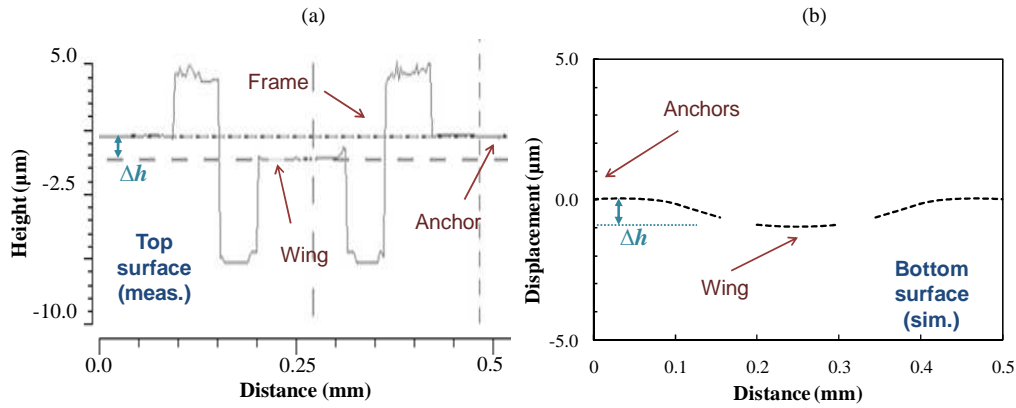


Figure 1.11: Profile of the S-type switch along the length l_b : (a) measurement from optical profiler (top surface), and (b) finite element simulation (bottom surface).

The usage of stopping pillars does not affect the initial deformation, but their height is important to evaluate the final contact force and consequently the contact resistance of the switch. For a nominal pillar height of $1.18 \mu\text{m}$ (TEOS+METAL+LTO+FLOMET) and a nominal contact dimple height of $1.81 \mu\text{m}$ (POLY+TEOS+METAL+LTO+FLOMET), the dimple-pillar height difference is equal to $\Delta z = 0.63 \mu\text{m}$. For a dimple-pillar distance of $37.5 \mu\text{m}$, which becomes the effective wing length, and if the 70% of the gold Young's modulus is considered, the theoretical contact force per dimple is around $20.5 \mu\text{N}$. A structural simulation including the contact element pairs CONTA174-TARGE170 has been performed in order to validate this value. As a result, the average contact force acting on a single dimple is $F_c = 20.2 \mu\text{N}$. The average value is considered since the contact force can be slightly different among each contact dimple, due to the initial deformation of the wing. The simulated contact pressure distribution on one single dimple is depicted in Fig. 1.12.

Another important aspect is the effect of stress gradient on the contact force. Stress gradient is usually ineffective on the electromechanical properties of a clamped-clamped membrane, but for S-type switches it can cause an initial upward bending of the contact wings. Fig. 1.13 reports the transversal profile of the S-type switch, showing clearly that the wings are not planar as expected. The

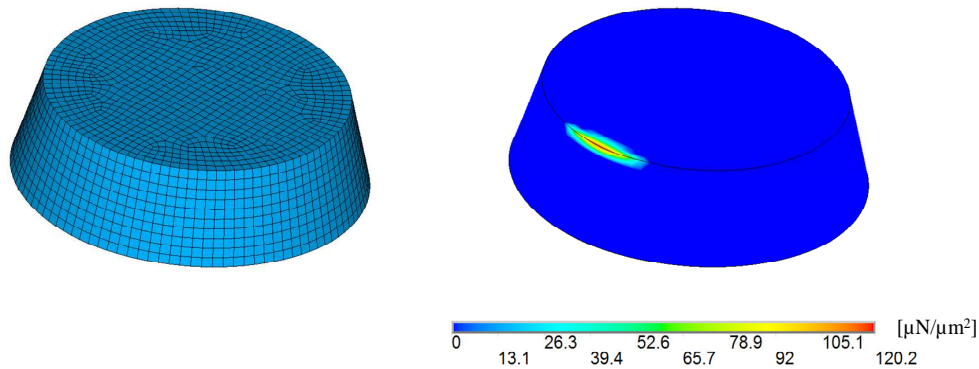


Figure 1.12: (a) FE model of the single contact bump, and (b) contact pressure at 70 V.

poor planarity is actually due to a combination of factors, such as the roughness of the gold surface (which is even higher at the edges of the structures), the planarization of the spacer (which is poorly effective when the layer underneath show significant height difference like in this case) and the stress gradient. ANSYS allows for the modeling of the stress gradient by exploiting the 20-nodes SOLID186 multilayer elements. The simulated profile corresponding to a stress gradient of $12 \text{ MPa}/\mu\text{m}$ is reported in Fig. 1.13 b. The resulting contact force is around $17.25 \mu\text{N}$, which is lower than the previous case. Consequently it seems clear that the presence of the stress gradient can reduce the contact force and then the switch contact resistance. Moreover, since the wings are closer to the RF line, the OFF state capacitance of the switch can be different. In addition, it is worth to observe that the stress gradient does not affect the first snap-down of the membrane, that is when the wings first come into contact with the bumps, as expected. However, the membrane collapses to the pillars (and then the contact force reaches its maximum value) at $V_B = 55 \text{ V}$, so a decrease of the “real” pull-in voltage, in the way defined before, is detected.

1.2.4 S OPT type switch

FE model suggest some actions to improve the electro-mechanical performances of the device. The CPW layer frame has to be re-designed in order to avoid the initial displacement. For example, the frame can be designed as a set of rows, parallel with respect to the RF line, avoiding any CPW layer the connection among them, as the ones used for the optimized B-type switch. This solution will prevent the membrane to deform after the stress relaxation of the CPW

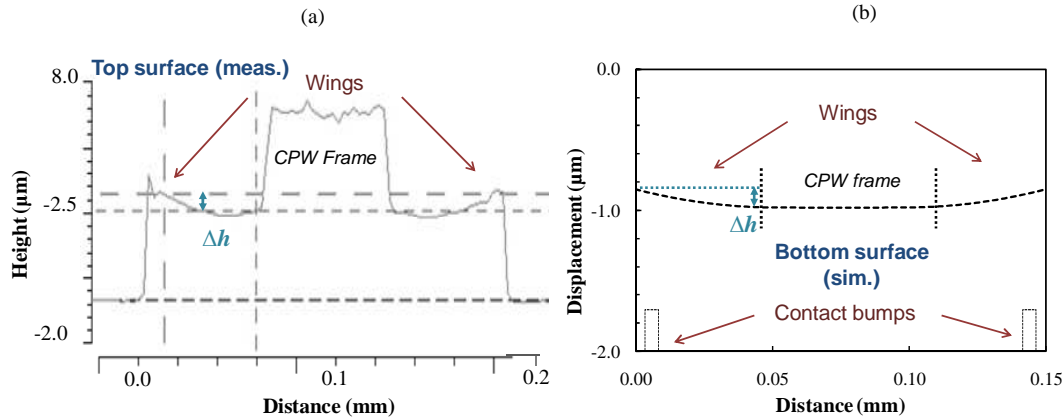


Figure 1.13: Transversal profile of the S-type switch : (a) measurement from optical profiler (top surface), and (b) FE simulation (bottom surface).

layer. In addition, a careful re-design of the contact wings is needed in order to both improve the contact force and reduce its sensitivity to the stress gradient. Fig. 1.14 depicts the FEM model of the new optimized design. The overall length of the switch is preserved, while the wing length is increased of $10 \mu\text{m}$. However, the width of central CPW frames is wider than the original design, and the springs length is increased from 25 to $45 \mu\text{m}$. As a result, the membrane is more planar than the previous case, with a maximum displacement of $0.12 \mu\text{m}$. The complete actuation of the membrane happens at 58 V , as shown in Fig. 1.15. Two contact dimples are used instead of five, along with a CPW reinforcement over the wings tip. As a result, the simulated contact force per dimple is equal to $100 \mu\text{N}$ (instead of $17 \mu\text{N}$ of the old version). Table 1.5 summarizes the new switch dimensions.

The mechanical optimization described above does not change significantly the overall dimensions of the membrane (length and width), so the RF performances in terms of return loss are not expected to change. However, a more planar membrane along with a higher contact force are expected to improve the isolation in OFF state and the insertion loss in ON state.

1.2.5 C type switch

The C-type switch is an ohmic series device consisting of a clamped-free or cantilever beam. The electromechanical properties of such a device resulted to be very sensitive to thickness and stress gradient variation, leading to a measured pull-in voltage from 30 to 80 V . A micrograph of the manufactured C-type switch

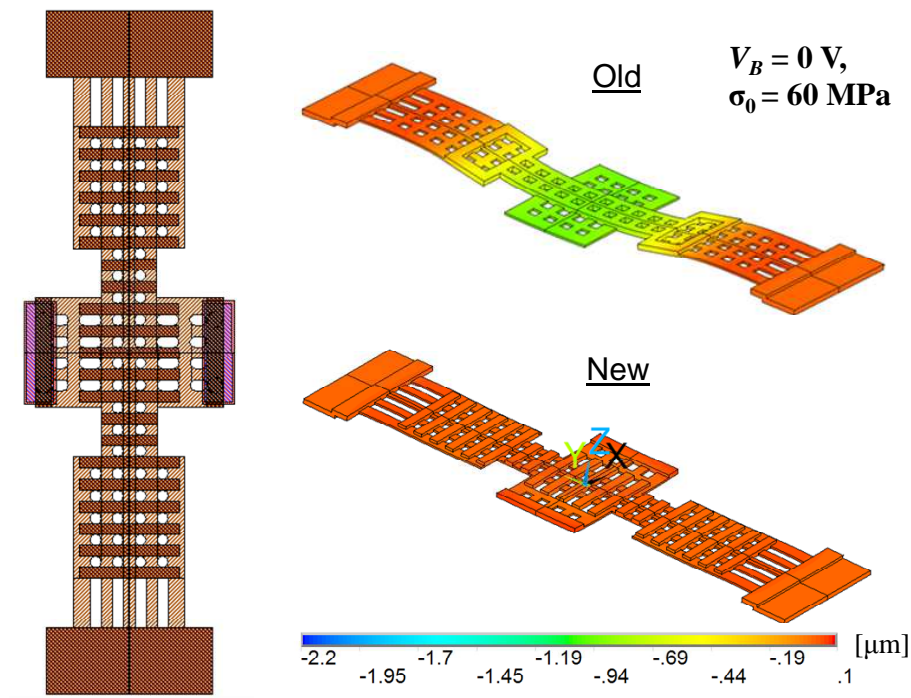


Figure 1.14: Layout of the optimized S-type switch and displacement comparison between old and new version at $V_B = 0\text{V}$ after the application of a 60 Ma residual stress.

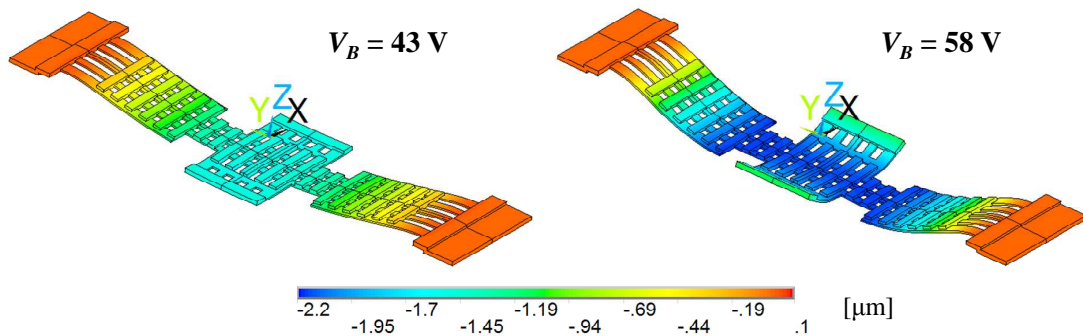


Figure 1.15: FE simulation results of the S-type switch: (a) at $V_B = 43\text{ V}$, when the wings touch the contact bumps, and (b) at $V_B = 58\text{ V}$, when the air-bridge collapses over the stopping pillars.

is shown in Fig. 1.16, while Table 1.6 reports the geometrical dimensions of the device.

FEM simulations have been performed by using the settings already listed in Table 1.2. As in the case of S-type switch, here the contact model assumes a

Table 1.5: Geometrical dimension of the S-type switch

Membrane length (l_b)	500 μm
Electrode length (l_e)	110 μm
Central membrane length (l_c)	50 μm
Lever length (l_l)	45 μm
Membrane width (w_b)	100 μm
Central membrane width (w_c)	50 μm
Wing width	60 μm
Spring length (w_l)	45 μm
Spring width (w_s)	10 μm
Membrane thickness (t_b)	2 μm
CPW Frame thickness (t_f)	3 μm
CPW Frame length 1	90 μm
CPW Frame length 2	50 μm

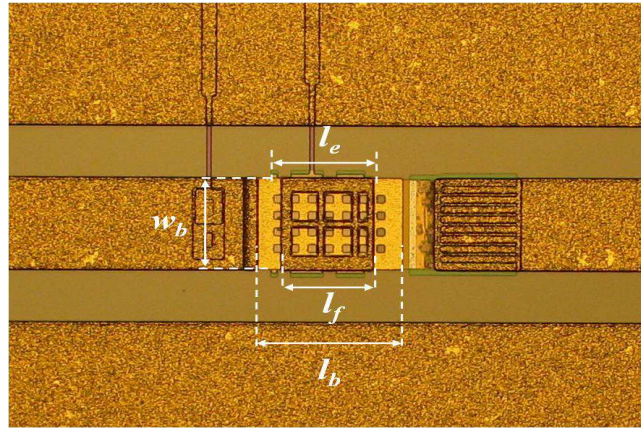


Figure 1.16: Micrograph of the C-type series switch.

Table 1.6: Geometrical dimensions of the C-type series switch

Membrane length (l_b)	170 μm
Electrode length (l_e)	120 μm
Frame length (l_c)	105 μm
Membrane width (w_b)	110 μm
Membrane thickness (t_b)	2 μm
Frame thickness (t_f)	3 μm

tremendous role in the evaluation of the switch performances. However, what is really important is the modeling of the stress gradient. Since the cantilever is a clamped-free membrane, actuation voltage and contact force are very sensitive to the presence of the stress gradient, which can induce a significant upward displacement (positive stress gradient) of the cantilever tip with respect to the contact dimple. Fig. 1.17 show the simulated displacement for $V_B = 0$ V and $V_B = 60$ V. A stress gradient of $12 \text{ MPa}/\mu\text{m}$ is again considered. The tip displacement reaches a maximum of $1.15 \mu\text{m}$. However, some measurements showed that the cantilever tip displacement can be even higher, which means that locally the stress gradient assumes even higher values.

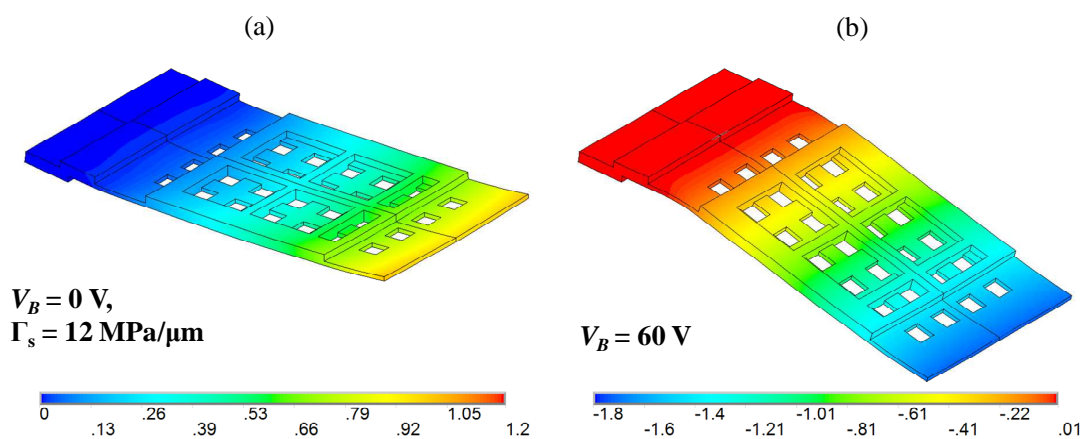


Figure 1.17: FE simulation results of the C-type switch : (a) at $V_B = 0$ V, with a stress gradient equal to $12 \text{ MPa}/\mu\text{m}$, and (b) at $V_B = 60$ V. The actuation occurs at 56 V.

If no stress gradient is present, the simulated pull-in voltage is around 44 V, which is in accordance with previous measurements performed on low-temperature released devices. The contact force per dimple is $1.4 \mu\text{N}$ at 60 V. For $\Gamma_s = 12 \text{ MPa}/\mu\text{m}$, the pull-in voltage is 56 V, whereas the contact force per dimple is $2.3 \mu\text{N}$ at 60 V. Fig. 1.18 a depicts the contact pressure distribution resulting from the last case. The variation of contact force as a function of stress gradient is difficult to evaluate since the contact is not stable after the actuation. In fact the cantilever anchor spring does not allow for a complete snap-down of the cantilever beam over the stopping pillars. In addition, in the case of stress gradient higher than zero, the cantilever tip is bended up, so the surface touching the contact dimple is larger than the case without stress gradient, as can be seen from Fig. 1.18 b.

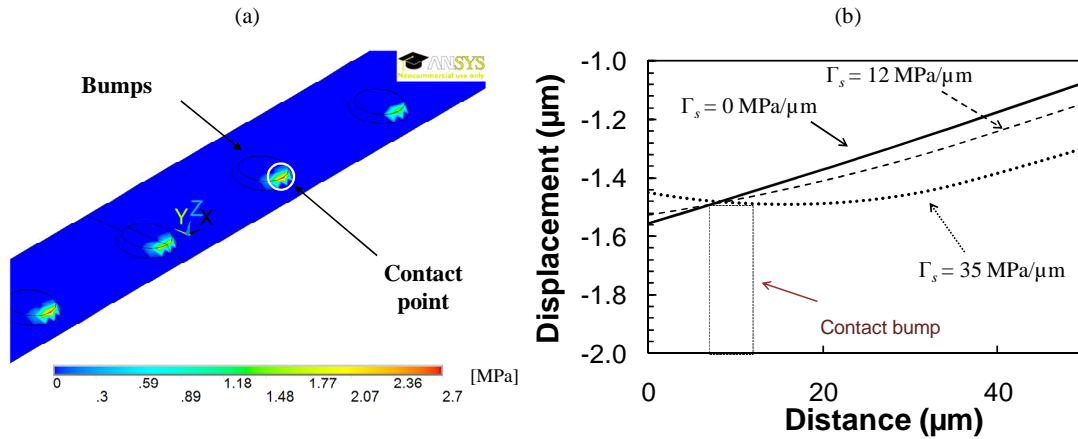


Figure 1.18: (a) Simulated contact pressure distribution, and (b) cantilever profile after the actuation with (dashed line) or without (solid lines) stress gradient.

1.2.6 C OPT type switch

The C-type switch can be redesigned and optimized in order to increase the contact force. For example, instead of a full anchor along the whole width of the beam, a couple of narrow anchor springs can be used to decrease the overall beam stiffness. This solution will allow the cantilever to fully collapse over the pillars, providing also a contact force which will depend only on the tip bending, as it is for S-type switch contact wings. A similar concept was previously fabricated and tested. It resulted in low actuation voltage but also low restoring force, showing many stiction problems. A new concept based on a double-actuation mechanism is proposed here. Actuation and restoring stiffness are optimized in order to minimize the tip displacement due to stress gradient and maximize the contact force. Fig. 1.19 depicts the FEM model of the new optimized design and the corresponding simulations at $V_B = 0, 30, 60$ V.

The long anchor springs allow for the employment of a double-cantilever structure: the overall membrane stiffness remains high enough to guarantee a good restoring force, but the internal cantilever facilitates the second actuation, providing a contact force per dimple which depends only by the tip bending stiffness in down state. Two contact dimples are employed in order to have a larger contact surface. However, the robustness of this solution under repeated actuation cycles should be investigated. The second pull-in voltage occurs at 50 V. The contact force per dimple at 60 V is 0.085 mN, which is much higher than the simulated contact force of the old version of the cantilever. Therefore a much lower and more stable contact resistance is expected. Fig. 1.20 depicts the final

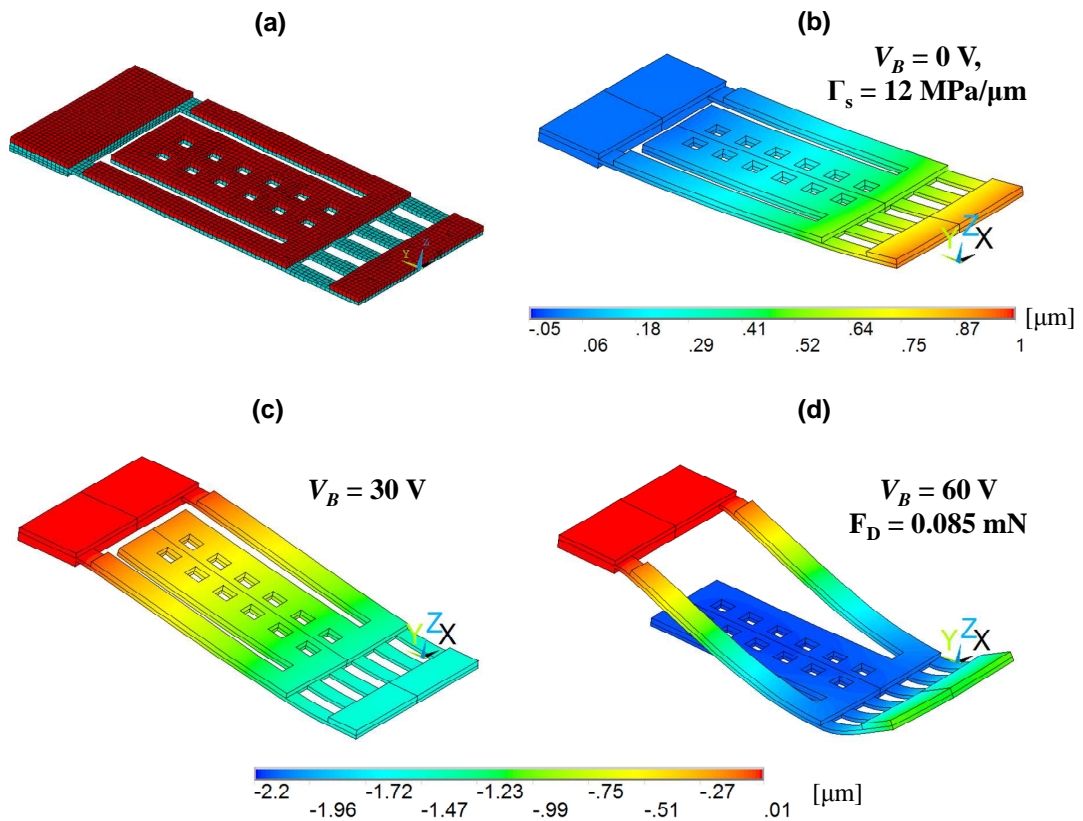


Figure 1.19: FE simulation results of the C-OPT switch : (a) Finite element model, (b) at $V_B = 0$ V, with a stress gradient equal to $12 \text{ MPa}/\mu\text{m}$, (c) at $V_B = 30$ V when the membrane touches the contact dimple, and (d) at $V_B = 60$ V. The actuation occurs at 50 V.

layout of the two versions of C-OPT switch. The only difference between the two switches is related to the actuation pad dimensions. In the second version the actuation pad has been designed larger to test the effect on the electric field distribution. Finally Table 1.7 reports the geometry dimensions of the membrane.

1.2.7 O type switch

The OAIR-type switch consists of a circular membrane anchored to the support by means of four long and narrow beams, placed at 90 degree among each other. It is a series device where the ohmic contact is established between the lateral side of the plate and two large contact pads. A micrograph of the device is depicted in Fig. 1.21, whereas Table 1.8 reports the main geometric dimensions. The device is dielectricless, but no stopping pillars are used. The direct contact between the

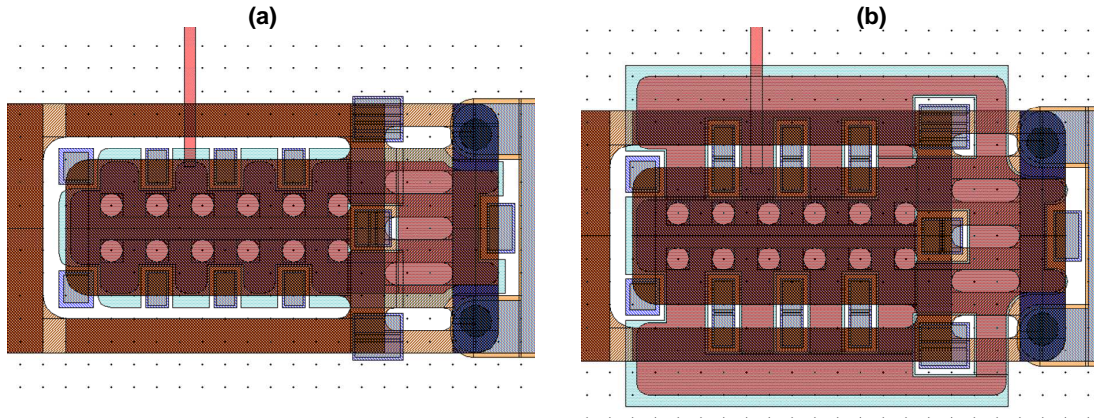


Figure 1.20: Final layout of the C-OPT type series switch: version 1 (a) with all the actuation electrode underneath the membrane, and version 2 (b) with a larger actuation electrode.

Table 1.7: Geometrical dimensions of the C-OPT series switch

Membrane length (l_b)	200 μm
Electrode length (l_e)	190 μm
Spring length (l_s)	135 μm
Frame length (l_c)	105 μm
Internal cant. length (l_{bi})	125 μm
Electrode width V1 (w_e)	60 μm
Electrode width V2 (w_e)	140 μm
Membrane width (w_b)	110 μm
Internal cant. width (w_{bi})	60 μm
Membrane thickness (t_b)	2 μm
Frame thickness (t_f)	3 μm

membrane and the bias electrode is supposed to be prevented by the contact pads. Finite element simulation have been performed by applying the settings already listed in Table 1.2.

Displacement results are reported in 1.22. The simulated actuation voltage is 38 V. The measured pull-in voltage in most of the switch was actually around 60 V. This difference is probably due to a different thickness of the gold layers characterizing the measured devices. In fact most of the OAIR-type devices were placed at the border of the wafers, since they were initially considered as a test structures. It is interesting to note that the initial displacement of the central

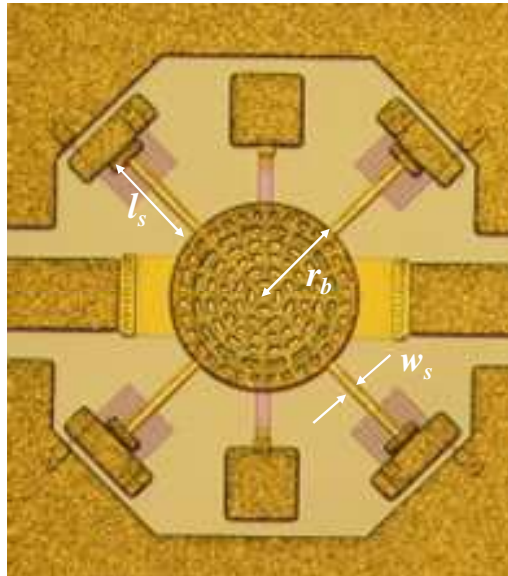


Figure 1.21: Micrograph of the OAIR-type series switch.

Table 1.8: Geometrical dimensions of the C-OPT series switch

Membrane Membrane radius (r_b)	135 μm
Spring length (l_s)	150 μm
Spring width (w_s)	10 μm
Membrane thickness (t_b)	2 μm
Frame thickness (t_f)	3 μm

point of the disk at 0 V is around 0.25 μm . If a stress gradient of 12 MPa/ μm is considered, the displacement reaches 0.5 μm . This means that a short between the two electrodes can easily happen. The simulated contact force at 60 V is 284 μN , which is a pretty high value. This partially confirms the reliability tests performed on the OAIR-type samples, which showed highly stable performances at the ON state. However no contact dimples are used (Fig. 1.23). Further investigation are on-going in order to understand the relevance of such a design difference.

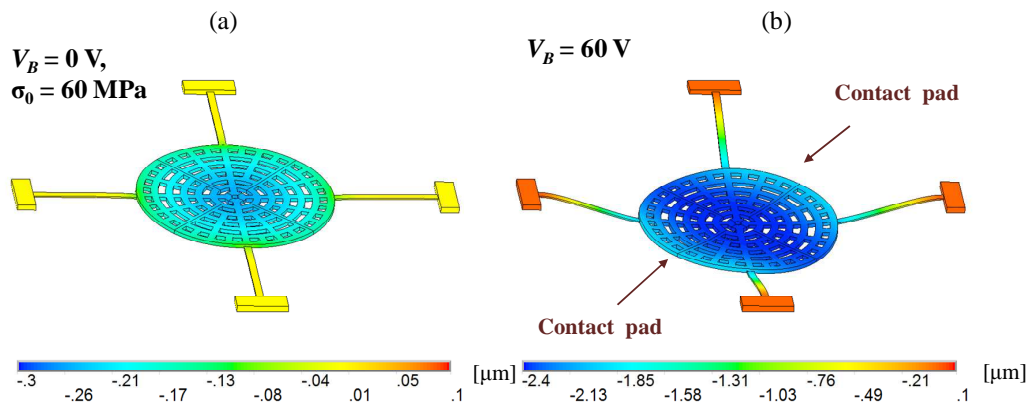


Figure 1.22: FE simulation results of the OAIR-type switch : (a) at $V_B = 0 \text{ V}$, with a residual stress equal to 60 MPa and no stress gradient, and (b) at $V_B = 60 \text{ V}$. The actuation occurs at 56 V.

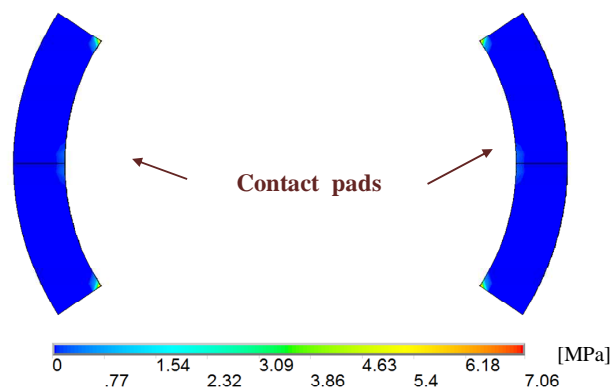


Figure 1.23: Contact pressure distribution on the contact pads at 60 V.

Chapter 2

RF MEMS Switches Operation

This chapter details the mechanical design of MEMS switches under electrostatic forces. Thermal actuation is not considered in this work because it is well covered in standard MEMS textbooks. Still, a lot of the material presented in this chapter is applicable for thermal or piezoelectric designs such as spring constant of fixed-fixed beams, critical stress issues, and hold-down voltage for MEMS switches [9].

2.1 Spring Constant of Fixed-Fixed Beams

The first step in understanding the mechanical operation of RF MEMS switches is to derive the spring constant of the fixed-fixed or cantilever beam. If the operation of the structure is limited to small deflections, as is the case for most RF MEMS devices, the mechanical behavior can be modeled using a linear spring constant, k (N/m). The deflection, Δg (m), of the fixed-fixed or cantilever beam for an external force, F (N), can then be obtained using $F = k\Delta g$.

Fixed-fixed beams are commonly used due to their relatively high spring constant and ease of manufacturing. The spring constant for the fixed-fixed beam can be modeled in two parts. One part, k' , is due to the stiffness of the bridge which accounts for the material characteristics such as Young's modulus, E (Pa), and the moment of inertia, I (m^4). The other part of the spring constant, k'' , is due to the biaxial residual stress, σ (Pa), within the beam and is a result of the fabrication process.

The expression for the spring constant of a fixed-fixed beam with a concentrated vertical load, P (N) in Fig. 2.1, is found from the deflection versus load position given by

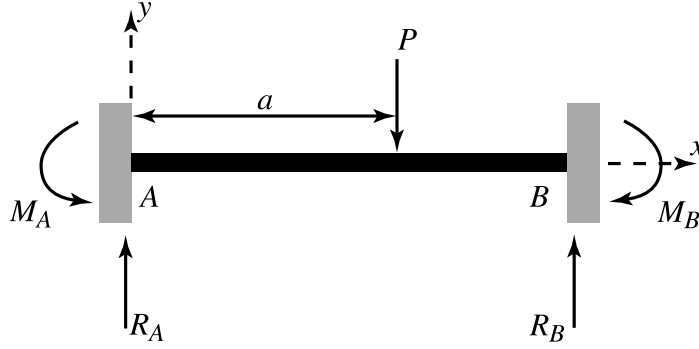


Figure 2.1: Fixed-fixed beam with concentrated vertical load P .

$$EI \frac{\partial^2 y}{\partial x^2} = M_A + R_A x \quad \text{per } x \leq a \quad (2.1)$$

$$y = \frac{M_A x^2}{2EI} + \frac{R_A x^3}{6EI} \quad \text{per } x \leq a$$

$$M_A = -\frac{Pa}{l^2}(l-a)^2$$

$$R_A = \frac{P}{l^3}(l-a)^2(l+2a)$$

where l is the length of the beam, M_A (Nm) is the reaction moment at the left end, and R_A (N) is the vertical reaction at the left end. The moment of inertia, I , for a rectangular cross section is given by $I = wt^3/12$, where w is the width and t is the thickness of the beam.

In MEMS applications, the load is typically distributed across the beam, and the deflection of the beam at the center is used to determine the spring constant. By substituting $x = l/2$ into Eq. 2.1, the deflection at the center is found for a concentrated load at point a . To find the deflection for a distributed load, the principle of superposition is used. For instance, in the case where the load is distributed across the entire beam, the deflection is found by evaluating the integral

$$y = \frac{2}{EI} \int_{\frac{l}{2}}^l \frac{\xi}{48} (l^3 - 6l^2a + 9la^2 - 4a^3) da \quad (2.2)$$

where ξ is the load per unit length so that the total load is $P = \xi l$, and the expressions for M_A and R_A have been substituted into Eq. 2.1. Since the structure is symmetric, the integral is evaluated from $l/2$ to l and multiplied by 2.

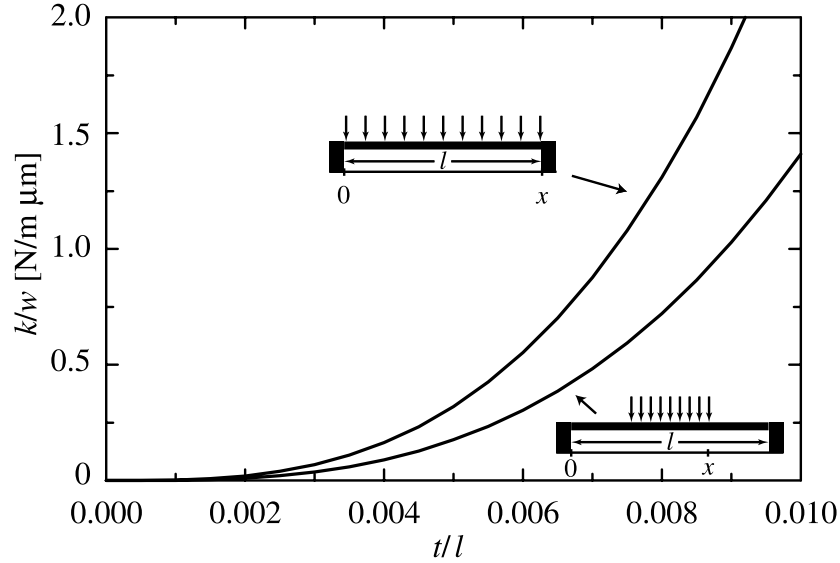


Figure 2.2: Spring constant (normalized with respect to the beam width w) versus t/l of a gold beam ($E = 80\text{GPa}$) where the force is distributed over the entire beam (k'_a) and over the center third of the beam ($k'_c, x = 2l/3$).

The spring constant is found to be

$$k'_a = -\frac{P}{y} = -\frac{\xi l}{y} = 32Ew \left(\frac{t}{l}\right)^3. \quad (2.3)$$

Figure 2.2 shows the variation of k'_a with $t = l$ for a gold beam ($E = 80\text{GPa}$). This figure is very similar for an aluminum beam, with the only difference being that $E = 69\text{GPa}$ for Al. Typical dimensions are beam lengths ranging from 200 to 500 μm and thicknesses ranging from 0.5 to 2 μm . Thus, a 300 μm -long gold beam with $t = 1\ \mu\text{m}$ and $w = 100\ \mu\text{m}$ has a spring constant of $k = 9,5\text{N/m}$. If the same beam is made of aluminum, the spring constant is 8.2 N/m. If the beam thickness is increased to 2 μm , the spring constant increases to 76 N/m and 65 N/m for gold and aluminum, respectively.

The force may be evenly distributed over the center portion of a fixed-fixed beam (Fig. 2.3). For this case, the integral in Eq. 2.2 should be evaluated with limits from $l/2$ to x . The general expression for this spring constant is

$$k'_c = 32Ew \left(\frac{t}{l}\right)^3 \frac{1}{8(x/l)^3 - 20(x/l)^2 + 14(x/l) - 1}. \quad (2.4)$$

Thus the spring constant for a concentrated load at the center of the beam is found when $x = l/2$, and for a load distributed over the entire beam when $x = l$,

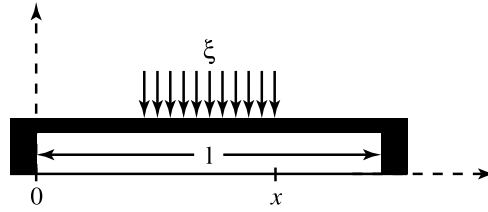


Figure 2.3: Fixed-fixed beam with the force, $P = \xi 2(x - l/2)$, evenly distributed about the center of the beam.

which results in Eq. 2.3. k'_c is plotted in Fig. 2.2 for a load distributed over the center third of the beam. As can be seen, concentrating the load more toward the center of the beam results in a lower spring constant than the case where the load is evenly distributed over the entire beam. The spring constant of the $300 \times 1 \times 100 - \mu m$ beam drops to 5.2 N/m for gold and 4.5 N/m for aluminum when the load is concentrated over the center third of the beam.

Another configuration is where the force is distributed at the ends of the beam, rather than in the center (Fig. 2.4). Here the spring constant is found by evaluating the integral in Eq. 2.2 from x to l . The result is

$$k'_e = 4Ew \left(\frac{t}{l} \right)^3 \frac{1}{(x/l)(1 - (x/l))^2}. \quad (2.5)$$

Figure 2.5 shows the calculated spring constant of a gold beam using Eqs. 2.4 and 2.5. Notice that the conditions $x/l = 1$ for k'_c and $x/l = 0.5$ for k'_e result in the same spring constant because they both represent the case where the force is distributed over the entire beam. As expected, concentrating the load toward the beam supports results in a much higher spring constant (and less movement for the same force) than having the load toward the center of the beam.

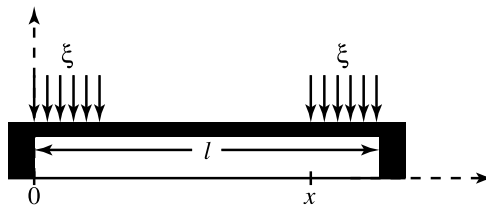


Figure 2.4: Fixed-fixed beam with the force, $P = \xi 2(l - x)$, evenly distributed along the ends of the beam.

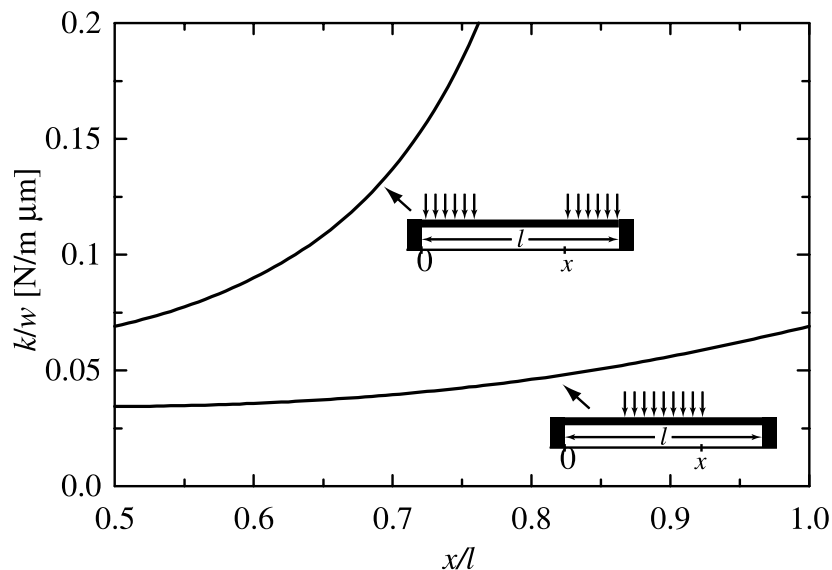


Figure 2.5: Spring constant (normalized with respect to the beam width w) of a gold beam with $t/l = 0,003$ where the force is distributed over the center (k'_c) and at the ends of the beam (k'_e).

2.1.1 Spring Constant Component due to Residual Stress

The part of the spring constant that is due to the biaxial residual stress within the beam is derived from modeling the beam as a stretched wire (Fig. 2.6). It should be noted that this model only applies for tensile stress. The biaxial residual stress, σ , results in a force, S [10],

$$S = \sigma(1 - \nu)tw \quad (2.6)$$

pulling on both ends of the beam, where ν is Poisson's ratio. When a vertical force (P) is applied, the beam is deflected by an amount, u , at the location of the applied force. This deflection stretches the beam, which increases the stress in the beam, and the force pulling on the ends increases to [11]

$$S + \frac{AE\Delta_1}{a} \text{ e } S + \frac{AE\Delta_2}{l-a} \quad (2.7)$$

where Δ_1 and Δ_2 are the lengths by which the beam is stretched on either side of the vertical load, P , and are given by

$$\Delta_1 = \sqrt{a^2 + u^2} - a \quad (2.8)$$

$$\Delta_2 = \sqrt{(l-a)^2 + u^2} - (l-a) \quad (2.9)$$

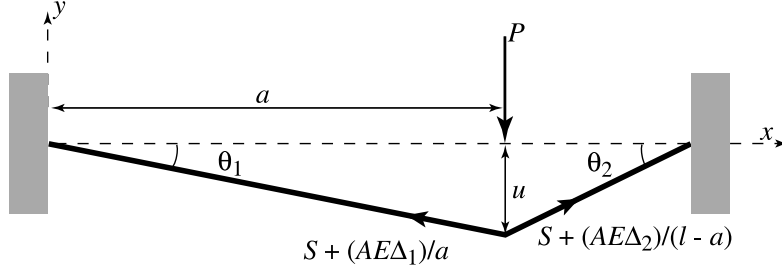


Figure 2.6: Beam modeled as a stretched wire with concentrated vertical load P .

By equating the applied force, P , with the forces in the beam projected onto the vertical direction and assuming a small deflection, the following equation can be found for u

$$u = \frac{Pa(l-a)}{Sl} \quad (2.10)$$

in which the additional force due to Δ_1 and Δ_2 has been neglected. From this equation, the deflection at the center of the beam ($x = l/2$) is found to be

$$y = -\frac{P}{2S}(l-a). \quad (2.11)$$

The deflection for a load distributed across the entire beam ($P = \xi l$) can now be found by evaluating the integral

$$y = -2 \int_{\frac{l}{2}}^l \frac{\xi}{2S}(l-a) da \quad (2.12)$$

where symmetry has been used in setting up the integral. The spring constant is found to be

$$k_a'' = -\frac{\xi l}{y} = \frac{8S}{l} = 8\sigma(1-v)w \left(\frac{t}{l}\right). \quad (2.13)$$

For the cases where the force is distributed over the beam and where the deflection is defined at the center of the beam ($x = l/2$), the spring constant due to the residual stress is

$$k_c'' = 8\sigma(1-v)w \left(\frac{t}{l}\right) \frac{1}{3-2(x/l)} \quad (2.14)$$

$$k_e'' = 4\sigma(1-v)w \left(\frac{t}{l}\right) \frac{1}{1-(x/l)}. \quad (2.15)$$

The total spring constant is the sum of the contributions from the beam stiffness and the biaxial residual stress; and for a load distributed across the entire beam, it is

$$k_a = k_a' + k_a'' = 32Ew \left(\frac{t}{l}\right)^3 + 8\sigma(1-v)w \left(\frac{t}{l}\right). \quad (2.16)$$

For a beam over a CPW line with the center conductor width being a third of the length of the beam with a force distributed above the center conductor, the total spring constant is found by adding the contributions from Eqs. 2.4 and 2.14 with $x = 2l/3$ and results in

$$k = 32Ew \left(\frac{t}{l}\right)^3 \left(\frac{27}{49}\right) + 8\sigma(1-\nu)w \left(\frac{t}{l}\right) \left(\frac{3}{5}\right). \quad (2.17)$$

Figure 2.7 shows the total spring constant using Eq. 2.17, for gold and aluminum beams for a residual stress of 0, 30, and 60 MPa. The spring constant for aluminum beams are very similar due to nearly equal Young's modulus and Poisson's ratio. For $l = 300 \mu\text{m}$ and $t = 0,5-1,5 \mu\text{m}$ ($t/l = 0,0015-0,0045$), the spring constant is dominated by the residual stress component (k'') for $\sigma > 10-20$ MPa.

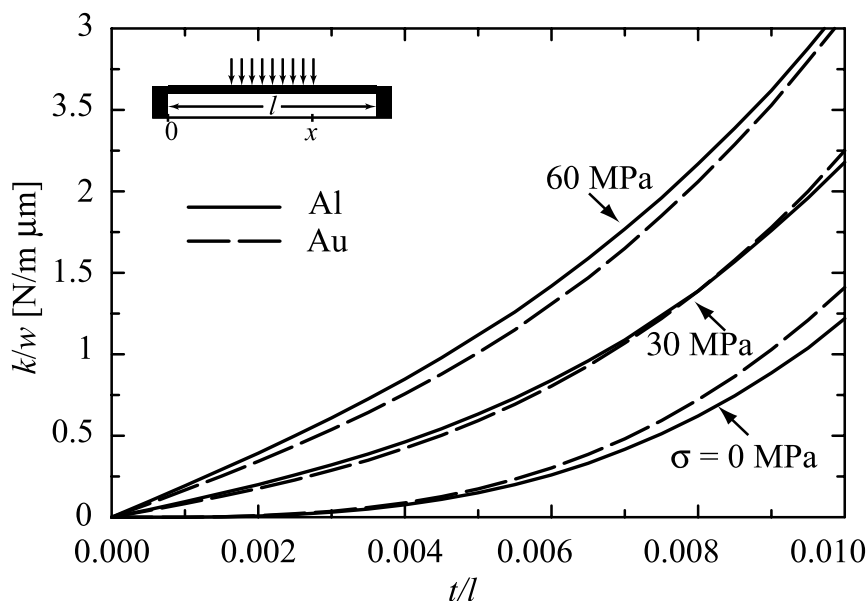


Figure 2.7: Spring constant (normalized with respect to the beam width w) of a gold and aluminum beam calculated using Eq. 2.17 versus residual stress in the beam.

2.2 Spring Constant of Low-k Beams

There are many variations of support beams that can be used to lower the effective spring constant of MEM devices. Some of the more commonly used support

variations are shown in Fig. 2.8, and the relevant equations for the spring constant are given below. Notice that these equations do not include the effect of the residual stress in the membrane layer.

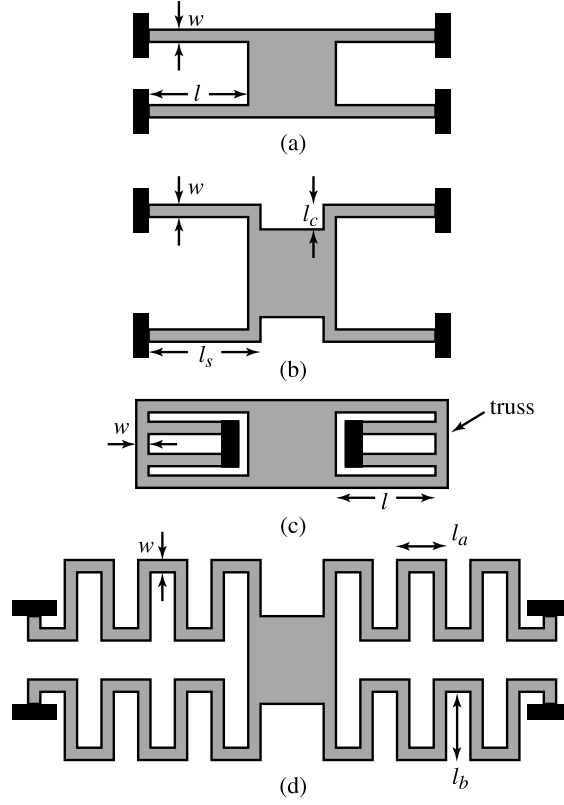


Figure 2.8: Various support beams used to reduce the spring constant. (a) Fixed-fixed flexures. (b) Crab-leg flexures. (c) Folded flexures. (d) Serpentine flexures.

$$(a) \quad k = 4Ew \left(\frac{t}{l} \right)^3 \quad (2.18)$$

$$(b) \quad k = \frac{4Ew \left(\frac{t}{l_c} \right)^3}{1 + \frac{l_s}{l_c} \left[\left(\frac{l_s}{l_c} \right)^2 + 12 \frac{1+\nu}{1+(w/t)^2} \right]} \approx 4Ew \left(\frac{t}{l_s} \right)^3 \quad \text{for } l_s \gg l_c \quad (2.19)$$

$$(c) \quad k \approx 2Ew \left(\frac{t}{l} \right)^3 \quad \text{for very stiff truss} \quad (2.20)$$

$$(d) \quad k \approx \frac{48GJ}{l_a^2 \left(\frac{GJ}{EI_x} l_a + l_b \right) n^3} \quad \text{for } n \gg \frac{3l_b}{\frac{GJ}{EI_x} l_a + l_b} \quad (2.21)$$

2.3 Spring Constant of Cantilever Beams

Cantilever beams are useful in many situations where it is inconvenient to fix both ends of the beam. An example is the in-line series switch where the input t-line becomes a cantilever beam whose free end hangs over the output t-line (Fig. 2.9). Another implementation is shown in Fig. 2.10 in which the actuation electrode is electrically isolated from the t-line through the use of a dielectric beam.

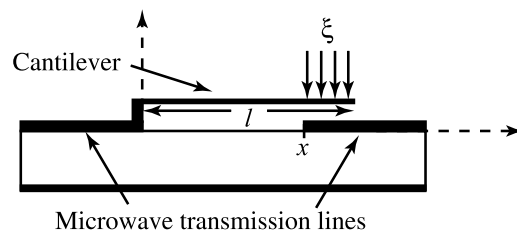


Figure 2.9: Example of a cantilever beam used as a series switch in a microstrip line.

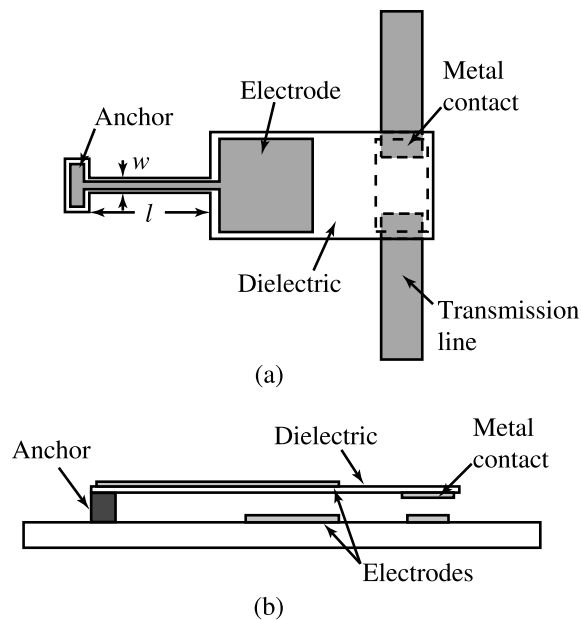


Figure 2.10: (a) Top and (b) side view of a cantilever beam with pull-down electrode and contact metal separated by a dielectric beam.

Since the cantilever beam is not fixed at one end, any residual stress within

the film is released and the spring constant does not contain a residual-stress component. Also, cantilever beams do not have any stretching component (k_s) due to the “free” condition at the tip of the beam. However, if there is a stress gradient over the cross section of the cantilever, then the beam will deflect upon release (see next Section regarding Beam curvature). In most cases this is an undesirable effect, but there are designs that use a built-in stress gradient to achieve a certain amount of deflection upon release [12]. The spring constant for a cantilever beam is derived the same way as the fixed-fixed beam. The spring constant due to a uniform force applied over the entire beam is given by

$$k_a = \frac{2Ew}{3} \left(\frac{t}{l} \right)^3 \quad (2.22)$$

whereas the spring constant for a force distributed from x to l on the beam, as shown in Fig. 2.9, is given by

$$k_c = 2Ew \left(\frac{t}{l} \right)^3 \frac{1 - (x/l)}{3 - 4(x/l)^3 + (x/l)^4}. \quad (2.23)$$

In many cases, the cantilever is fabricated using a thick silicon nitride or silicon dioxide (SiO_2) layer, with a Young’s modulus of around 210 GPa and 70 GPa, respectively. Figure 2.11 presents the spring constant of a gold and silicon nitride cantilever (SiN) using Eq. 2.23. By comparing Fig. 2.11 and Fig. 2.5, it is seen that the cantilever spring constant is much smaller than a fixed-fixed beam with the same t/l ratio. In fact, for the case of an evenly distributed load, the cantilever spring constant is 48 times smaller than that for the fixed-fixed beam. The spring constant for the cantilever shown in Fig. 2.10 can be approximated by assuming that the actuation electrode does not bend but provides a concentrated load at the end of the flexible beam of length l . This spring constant is found from Eq. 2.23 with $x = l$ and gives

$$k = 3 \frac{EI}{l^3} \quad (2.24)$$

where the Young’s modulus now must take into account the fact that the beam is formed from two different materials. Also, the beam no longer has a rectangular cross section, and so the moment of inertia, I , must be recalculated.

2.4 Beam Curvature Due to Stress Gradients

An unavoidable product of thin-film deposition is the presence of a stress gradient in the normal direction of fixed-fixed or cantilever beams. The stress gradient

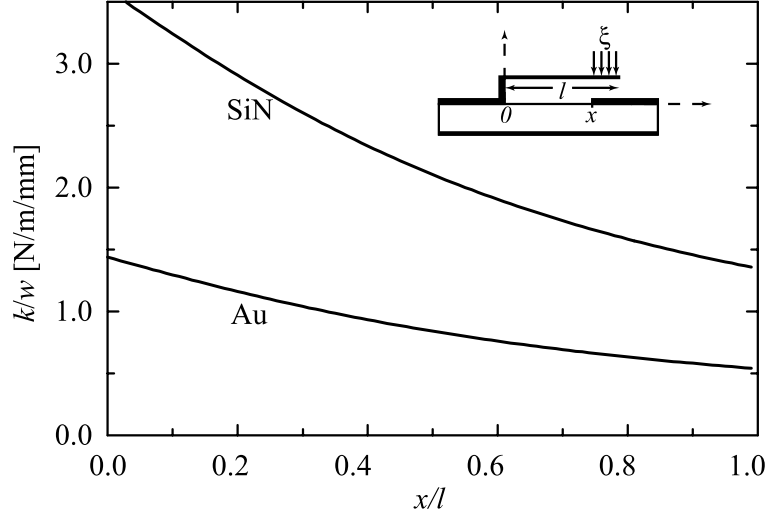


Figure 2.11: Spring constant (normalized with respect to the bridge width w) of a gold ($E = 80$ GPa) and *SiN* ($E = 210$ GPa) cantilever beam with $t/l = 0.01$ calculated using Eq. 2.23.

is due to the different deposition conditions encountered by the bottom and top layers of a uniform beam, or to the use of multiple layers each with a different residual stress component (SiN/Au/SiN). In most designs, it is important to reduce the stress gradient because it results in positive or negative beam curvature (Fig. 2.12). However, in some designs, the stress gradient is used to build a compact switch with a strong curvature component and a very low up-state capacitance [12].

The equivalent bending moment due to a stress gradient is

$$M = \int_{-(t/2)}^{t/2} wz\sigma(z)dz \quad (2.25)$$

where w is the width of the beam, z is in the thickness direction, and $\sigma(z)$ is the residual stress as a function of thickness. For a linear stress gradient, one can define the stress as

$$\sigma(z) = E\Gamma z \quad (2.26)$$

where Γ is a linear strain gradient. Using Eq. 2.25, Γ can be written as

$$\Gamma = \frac{12M}{Ewt^3} = \frac{M}{EI} \quad (2.27)$$

where I is the moment of inertia of a rectangular beam ($I = wt^3/12$). A moment applied at the endpoint of a cantilever with length l results in a deflection at the

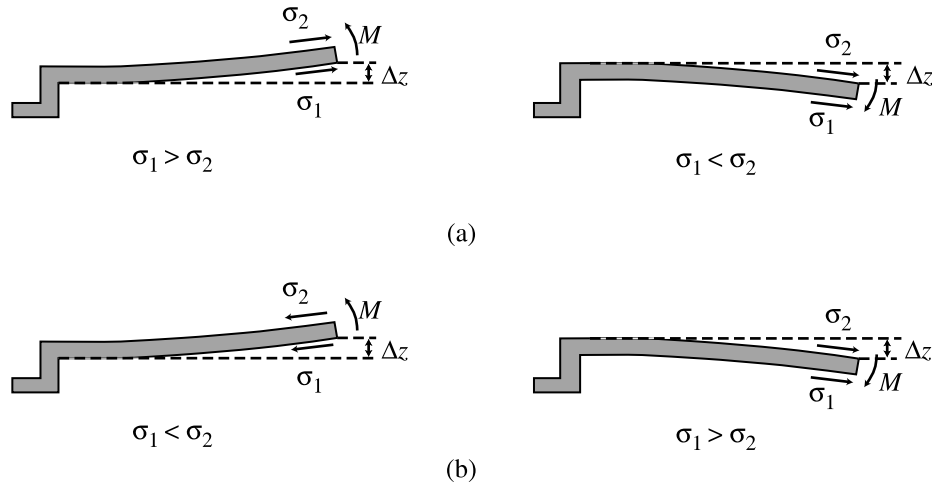


Figure 2.12: Effect of stress gradient on beam curvature for (a) compressive stress and (b) tensile stress.

tip of

$$\Delta z = \frac{Ml^2}{2EI} = \frac{\Gamma l^2}{2} \quad (2.28)$$

For the case of a two-layer beam with the same Young's modulus, a thickness of t_1 , t_2 , and a uniform residual stress per layer of s_1 , s_2 , respectively, the deflection at the tip of the beam is calculated using the equations above

$$\Delta z = \frac{3(\sigma_2 - \sigma_1)L^2}{4tE} \left[1 - \frac{(t_1 - t_2)^2}{t^2} \right] \quad (2.29)$$

where $t = t_1 + t_2$. If two different layers are used, then an approximate solution can still be obtained using the equivalent Young's modulus. A nitride-gold cantilever with $t_1 = 1.5 \mu\text{m}$, $t_2 = 0.5 \mu\text{m}$, $l = 150 \mu\text{m}$, $E_e = 160 \text{ GPa}$, results in $\pm 0.41 \mu\text{m}$ deflection at its tip for $\Delta\sigma = \pm 10 \text{ Mpa}$. This is not acceptable in most MEMS switch designs, and the stress difference between the top and bottom layers must be controlled to less than 5 Mpa.

2.5 Electrostatic Actuation

When a voltage is applied between a fixed-fixed or cantilever beam and the pull-down electrode, an electrostatic force is induced on the beam (Fig. 2.13). This is the well known electrostatic force which exists on the plates of a capacitor under an applied voltage [13]. In order to approximate this force, the beam over the pull-down electrode is modeled as a parallel-plate capacitor. Although the actual

capacitance is about 20-40 % larger due to fringing fields, the model provides a good understanding of how electrostatic actuation works.

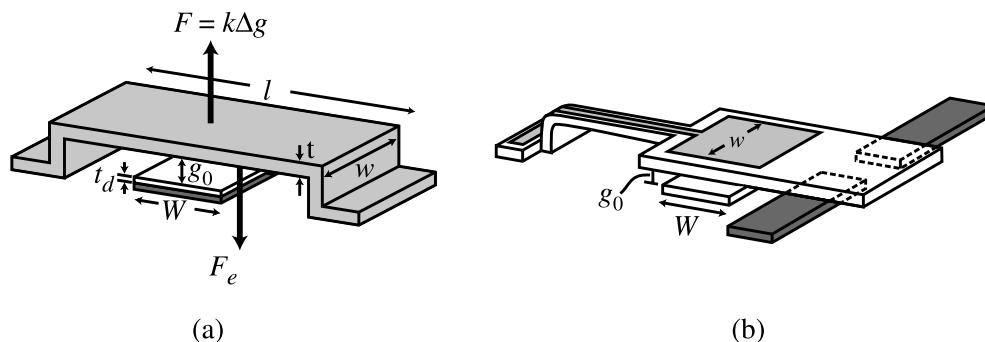


Figure 2.13: A MEMS fixed-fixed beam (a) and cantilever (b) with a pull-down electrode.

Given that the width of the beam is w and the width of the pull-down electrode is W ($A = Ww$), the parallel plate capacitance is

$$C = \frac{\varepsilon_0 A}{g} = \frac{\varepsilon_0 Ww}{g} \quad (2.30)$$

where g is the height of the beam above the electrode. The electrostatic force applied to the beam is found by considering the power delivered to a time-dependent capacitance and is given by

$$F_e = \frac{1}{2} V^2 \frac{dC(g)}{dg} = -\frac{1}{2} \frac{\varepsilon_0 Ww V^2}{g^2} \quad (2.31)$$

where V is the voltage applied between the beam and the electrode. Notice that the force is independent of the voltage polarity. Equating the applied electrostatic force with the mechanical restoring force due to the stiffness of the beam ($F = kx$), we find

$$\frac{1}{2} \frac{\varepsilon_0 Ww V^2}{g^2} = k(g_0 - g) \quad (2.32)$$

where g_0 is the zero-bias bridge height. Solving this equation for the voltage results in

$$V = \sqrt{\frac{2k}{\varepsilon_0 Ww} g^2 (g_0 - g)}. \quad (2.33)$$

The plot of the beam height versus applied voltage shows two possible beam positions for every applied voltage (Fig. 2.14). This is a result of the beam position

becoming unstable at $(2/3)g_0$, which is due to positive feedback in the electrostatic actuation. This can be understood by considering the electrostatic force in terms of the electric field applied to the beam [14], [15]

$$F_e = \frac{QE}{2} \quad (2.34)$$

where Q is the charge on the beam and $E = V/g$ is the electric field due to

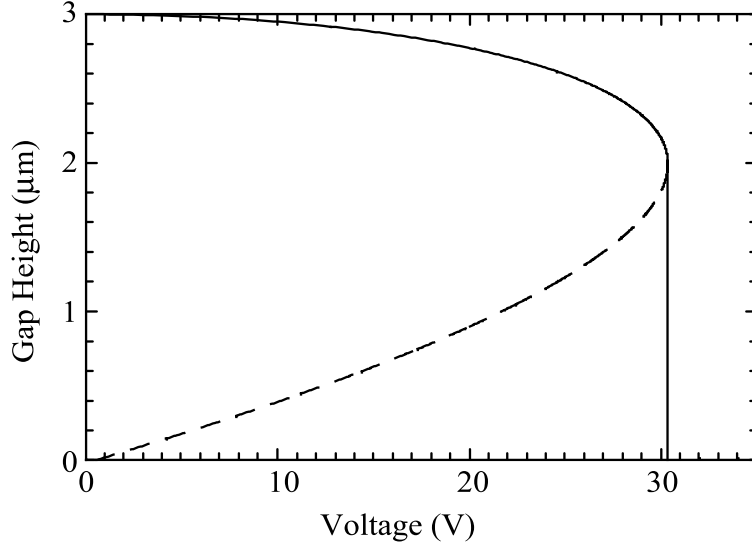


Figure 2.14: Beam height versus applied voltage with $W = 100 \mu\text{m}$, $w = 100 \mu\text{m}$, $g_0 = 3 \mu\text{m}$, and $k = 10 \text{ N/m}$. The pull-down voltage is 30 V. The dashed line represents the unstable portion of the height.

the applied voltage. When the constant voltage source (infinite charge pump) is increased, the force is increased due to an increase in the charge. Simultaneously the increased force decreases the beam height, which, in turn, increases the capacitance and thus the charge and the electric field. At $(2/3)g_0$, the increase in the electrostatic force is greater than the increase in the restoring force, resulting in (a) the beam position becoming unstable and (b) collapse of the beam to the down-state position. Notice that the equations above apply equally to fixed-fixed and cantilever beams. By taking the derivative of Eq. (2.33) with respect to the beam height and setting that to zero, the height at which the instability occurs is found to be exactly two-thirds the zero-bias beam height. Substituting this value back into Eq. (2.33), the “pull-down” voltage is found to be

$$V_p = V(2g_0/3) = \sqrt{\frac{8k}{27\epsilon_0 W w}} g_0^3. \quad (2.35)$$

It should be noted that although Eq. 2.35 shows a dependence on the beam width, w , the pull-down voltage is independent of the beam width since the spring constant, k , varies linearly with w (see Eq. 2.17). Figure 2.15 presents the pull-down voltage for a gold bridge with a residual stress of 0, 30, and 60 MPa, calculated using Eq. 2.35 and Eq. 2.17. A similar pull-down voltage is obtained for aluminum beams since they have nearly the same spring-constant values. Figure 2.16 shows the pull-down voltage versus beam height. It is seen that beams with $g \geq 3 \mu\text{m}$ and $\sigma \geq 30 \text{ MPa}$ result in a very large pull-down voltage.

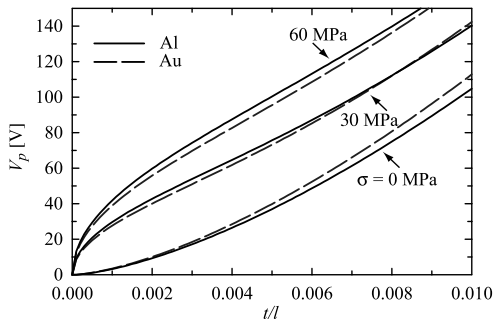


Figure 2.15: Pull-down voltage of gold and aluminum fixed-fixed beams versus t/l for $g_0 = 3 \mu\text{m}$ ($l = 300 \mu\text{m}$, $W = 100 \mu\text{m}$).

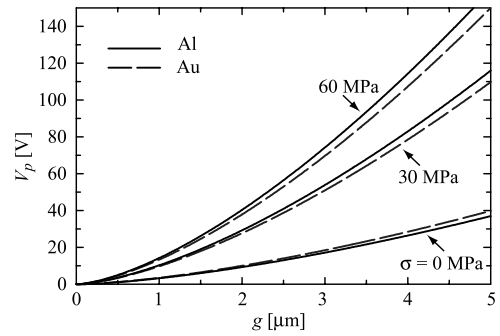


Figure 2.16: Pull-down voltage of gold and aluminum fixed-fixed beams versus gap for $l = 300 \mu\text{m}$, $W = 100 \mu\text{m}$, and $t = 1 \mu\text{m}$.

2.6 Linear Dynamic Analysis of MEMS Beams

The frequency response of a fixed-fixed or cantilever beam is useful for determining the switching time of the switch, the mechanical bandwidth over which it can be used, and the effect of thermal noise. The dynamic response is given by d'Alembert's principle and is [11]

$$m \frac{d^2x}{dt^2} + b \frac{dx}{dt} + kx = f_{ext} \quad (2.36)$$

where x is the bridge displacement, m is the bridge mass, b is the damping coefficient, k is the spring constant, and f_{ext} is an external force. By using Laplace transforms, the frequency response is found to be

$$\frac{X(j\omega)}{F(j\omega)} = \frac{1}{k} \left(\frac{1}{1 - (\omega/\omega_0)^2 + j\omega/(Q\omega_0)} \right) \quad (2.37)$$

where

$$\omega_0 = \sqrt{k/m}$$

$$Q = k/(\omega_0 b)$$

are the resonant frequency and the quality factor respectively. An important point to consider is the effective mass of the resonant mode, since only the central (or end) portion of the beam is moving. Modal analysis indicates that the effective mass is around 0.35-0.45 times the actual mass of the beam, and it depends on the size of the pull-down electrode, the thickness, and spring constant of the beam [16]. The mechanical resonant frequency of most electrostatic MEMS switches is 10-200 kHz.

Figure 2.17 shows the small-signal response of MEMS beams for $Q = 0.2, 1, 5$ and a resonant frequency of 50 kHz. The response at ω_0 is Q times the low-frequency response for all Q . $Q \geq 0.5$ results in a true second-order response; and for $Q = 0.2$ the response is dominated by the first-order pole at 10 kHz, thus behaving as a first-order system. In practice, it is advantageous to have a structure with $0.5 \leq Q \leq 2$. A $Q \leq 0.5$ results in a slow switching time, while a $Q \geq 2$ results in a long settling time when the switch is released.

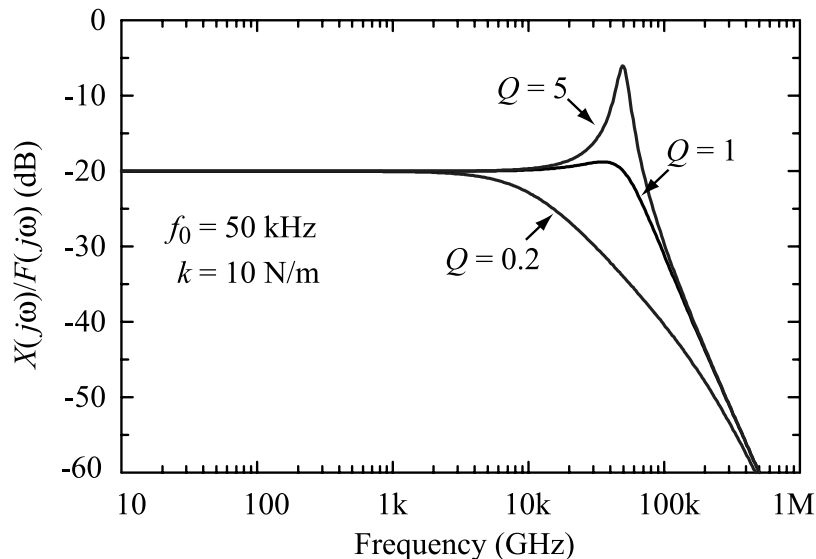


Figure 2.17: Relative frequency response of a beam with a resonant frequency of 50 kHz and $Q = 0.2, 1, 5$.

2.7 Gas Fundamentals

It is important to briefly review the fundamentals of gas motion because most of the damping in MEMS structures is given by squeeze film damping [17]. As the MEMS beam is actuated, the air (or gas) must be pushed from underneath the plate, and the air molecules undergo several collisions in the gap between the beam and the bottom electrode. There are several important numbers in fluid mechanics which must be considered because they represent the different regimes of fluid flow, and this has a direct effect on the damping coefficient of the MEMS beam. The mean-free path is the distance covered by a molecule in a gas between successive collisions and is given by

$$\lambda = \frac{1}{\sqrt{2}\pi N\sigma^2} \quad (2.38)$$

where σ is the diameter of the gas molecule and N is the number density of the gas [18] ($\rho = Nm_0$ where m_0 is the mass of a single molecule in the gas, and ρ is the gas density in kg/m³). The mean free path is 0.07-0.09 μm for most gases at standard pressure and temperature (STP is 25 °C, 101 kPa, or 760 torr). The mean free path at a pressure P_a is [18]

$$\lambda_a = \frac{P_0}{P_a}\lambda_0 \quad (2.39)$$

where λ_0 is the mean free path at a pressure P_0 . Notice that the mean free path at very low pressures (1 mtorr) is more than the typical gap in most MEMS structures. The Knudsen number is a measure of the viscosity of the gas (or fluid) under the MEMS beam and is given by [18]

$$K_n = \frac{\lambda}{g} \quad (2.40)$$

where g is the gap height. A very small Knudsen number means that there are many collisions in the gap and that the gas (or fluid) is viscous. When the gap height is on the order of the mean free path (large K_n), particle-wall interactions become important, reducing the flow resistance, or viscosity (μ), through a “slip effect” where particles can have fewer interactions before escaping. For $g \geq 1\mu\text{m}$, $K_n < 0.1$ at STP and the flow is assumed to be nearly viscous. The coefficient of viscosity, μ , is a measure of the resistance of a gas to changes in the transport of molecular momentum and is given by $\mu \simeq (\text{density})(\text{speed})(\text{length})$. The equation of viscosity is [18]

$$\mu = 0.1792\pi\rho\lambda\sqrt{2RT} \quad (2.41)$$

where R is the specific gas constant. An accurate equation for the viscosity for ideal and quasi-ideal gases such as air, nitrogen, and so on, was derived by Sutherland and is [18]

$$\mu = 1.2566 \times 10^{-6} \sqrt{T} \left(1 + \frac{\beta}{T}\right)^{-1} \text{ Kg/m}\cdot\text{s} \quad (2.42)$$

where $\beta = 110.33\text{K}$, T is in kelvin and the viscosity of ideal gases at STP is $1.845 \times 10^{-5} \text{ kg/ m s}$ (or $\text{Pa}\cdot\text{s}$). The viscosity is directly dependent on the pressure as seen by Eqs. 2.39 and 2.40. The viscosity does change with the Knudsen number, since a high Knudsen number means that the gas experiences very few collisions and that the flow is not viscous anymore. A well-known equation was derived by Veijola et al. [19]

$$\mu_e = \frac{\mu}{1 + 9.638K_n^{1.159}} \quad (2.43)$$

and is accurate to within $\pm 5\%$ for $0 \leq K_n \leq 880$. For $K_n = 0.026 - 0.08$, which corresponds to a gap height of $3 - 1 \mu\text{m}$, we find that $\mu_e = 0.87 - 0.66\mu$. Another parameter to consider is the non dimensional squeeze number, σ , defined by [20]-[21]

$$\sigma = \frac{12\mu_e l^2}{P_a g^2} \omega \quad (2.44)$$

where l is the characteristic length and ω is the applied mechanical frequency. For a circular membrane, $l = R$ and $l = w$ for a rectangle or square membrane, where w is the shortest dimension of the membrane. A low squeeze number ($\sigma \leq 3$) means that the gas escapes from the gap without compression. A high squeeze number means that the gas is trapped in the structure by its viscosity. Notice that the squeeze number increases with frequency; that is, at high mechanical frequencies, there is less time for the gas to escape and the flow becomes more viscous.

The main effect of a high squeeze number is the addition of a spring constant to the membrane structure. This spring constant converges to $k_a = P_a A/g$, where A is the area of the membrane, and should be added to the values derived in previous chapter to determine the correct resonant frequency of the MEMS structure. At low squeeze numbers, $k_a \simeq 0$. A membrane with $R = 100 \mu\text{m}$ and $g = 2 \mu\text{m}$ results in $\sigma = 21.6 \times 10^{-6} \omega$ and for $f = 10 \text{ kHz}$, $\sigma = 0.34$. However, at $f = 100 \text{ kHz}$, $\sigma = 3.4$, and one must take the k_a term into consideration if an accurate prediction of the resonant frequency is desired.

Equation 2.44 is derived for parallel plates with no holes, and where the gas

escapes from the sides. In the case of holes in the membrane, the distance l is defined as half the distance between the holes ($3 - 8 \mu\text{m}$); therefore the squeeze number is truly insignificant, even at $f = 100 \text{ kHz}$. It is for this reason that the squeeze number is not used in MEMS switch designs.

2.8 Damping Coefficient/Quality Factor

The quality factor of a beam is determined by several different variables such as the pressure, temperature, and intrinsic material dissipation. Because most RF MEMS devices are operated at atmospheric pressure, the quality factor is dominated by squeeze-film damping [17]. The equations below are valid for gaps as small as the mean-free path of the ambient gas.

The damping of a rectangular or circular parallel-plate geometries has been derived from a linearized form of the compressible Reynolds gas-film equation [17]-[20]

$$b = \frac{3}{2\pi} \frac{\mu A^2}{g_0^3} \quad (2.45)$$

where A is the area of the device. It is seen that the damping coefficient has a strong dependence on g_0 . One way to decrease the damping is to use holes in the top membrane. The effect of holes on the damping coefficient has been experimentally derived for circular structures and is [22]

$$b = \frac{12}{N\pi} \frac{\mu A^2}{g_0^3} \left(\frac{p}{2} - \frac{p^2}{8} - \frac{\ln(p)}{4} - \frac{3}{8} \right) \quad (2.46)$$

where N is the total number of the holes and p is the fraction of the open area on the plate.

An approximate formula for the quality factor ($Q = k/\omega_0 b$) of a cantilever beam is given by [23]

$$Q_{cant} = \frac{\sqrt{E\rho}t^2}{\mu(wl)^2} g_0^3 \quad (2.47)$$

where w and l are the width and length of the cantilever. A first-order approximation for the quality factor of a fixed-fixed beam is the Q of a cantilever beam of half its length [24]

$$Q_{ff} = \frac{\sqrt{E\rho}t^2}{\mu\left(\frac{wl}{2}\right)^2} g_0^3 \quad (2.48)$$

The quality factor for a gold fixed-fixed beam with dimensions of $l = 300 \mu\text{m}$, $w = 60 \mu\text{m}$, $t = 1 \mu\text{m}$, and $g_0 = 3 \mu\text{m}$ is $Q = 1.0$ using the effective viscosity

of air 2.43. The quality factor reduces to $Q = 0.2$ for $g = 1.5 \mu\text{m}$. The Q of Al beams is even smaller than Au beams due to the lower density of Al. It is therefore essential to use holes in the membrane, especially for low-height MEMS structures. At very low pressures, $\mu \simeq 0$ and the damping coefficient is limited by the dissipation in the beam anchors and by the interface granules in the beam itself. The Q of metal-based beams is 30 – 150 in vacuum, while polysilicon or siliconnitride beams yield a Q of 500 – 5,000 in vacuum. A high- Q structure will not affect the switching speed of the device if $Q \geq 3$. However, it has a large effect on the settling time of the switch when it is released from the down-state position.

2.8.1 Damping Variation Versus Height

As seen above, the damping is a strong function of the nominal gap height g_0 . To correct this equation for large displacements, Sadd and Stiffer [25] proposed the following multiplicative displacement function:

$$f_d = \left(1.1 - \left(\frac{x}{g_0} \right)^2 \right)^{-(3/2)} \quad (2.49)$$

Combining Eqs. 2.40, 2.43, and 2.49 yields the large displacement-compensated equation for the damping coefficient. The corresponding Q is

$$Q_e = Q \left(1.1 - \left(\frac{x}{g_0} \right)^2 \right)^{(3/2)} \left(1 + 9.638 \left(\frac{\lambda}{g} \right)^{1.159} \right) \quad (2.50)$$

where Q is the nominal small-displacement quality factor of the MEMS switch at $g = g_0$. This displacement-compensated equation is incorporated in the nonlinear dynamic model of next Section. Notice that an experimental factor of 1.1 instead of the theoretical factor of 1.0 is used in Eqs. 2.49 and 2.50. This results in $Q_e \neq 0$ for $x = g_0$ and a permissible solution when the beam touches the dielectric layer of the pull-down electrode. The pull-down simulations are nearly identical for both cases because the electrostatic force is very high as $g \rightarrow 0$. However, the release time is strongly affected by the choice of the experimental factor. The theoretical value of 1.0 results in $Q_e = 0$ ($b = \infty$) at $x = g_0$ and an infinite release time (the switch will not release).

2.9 Nonlinear dynamic analysis of MEMS Beams

The equations governing the simple 1-D nonlinear model can be readily solved with a nonlinear simultaneous differential equation solver such as *Mathematica* (Fig. 2.18). The voltage waveform V_s can be an arbitrary continuous function of time to allow investigation of phenomena such as pull-down, release, power handling, intermodulation, and source noise effects.

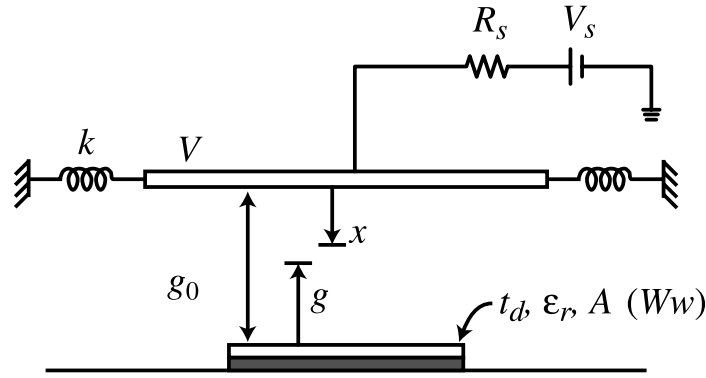


Figure 2.18: The 1-D MEMS beam model and its coordinate system.

The equations governing the 1-D model are

$$m \frac{d^2 x}{dt^2} + b \frac{dx}{dt} + kx + k_s x^3 = F_e + F_c \quad (2.51)$$

with

$$k = k' + k'' \quad (2.52)$$

where k' and k'' are the bending spring and residual-stress spring constants, and k_s is the stress-stiffening spring constant (stretching effect) and is only applicable to fixed-fixed beams. The damping factor is $b = k/\omega_0 Q$, and Q is displacement-dependent as shown in Eq. 2.50. The voltage on the switch is

$$V = V_s - i(t)R_s = V_s - \left(C \frac{dV}{dt} + V \frac{dC}{dt} \right) R_s \quad (2.53)$$

with

$$C = \frac{\epsilon_0 A}{g_0 + \frac{t_d}{\epsilon_r} - x} \quad (x = g_0 - g) \quad (2.54)$$

where the fringing capacitance has been neglected for now.

The external forces are

$$F_e = \frac{1}{2} \frac{\epsilon_0 A V^2}{(g_0 + t_d/\epsilon_r - x)^2} \quad (2.55)$$

$$F_c = \frac{C_1 A}{(g_0 - x)^3} - \frac{C_2 A}{(g - x)^{10}}. \quad (2.56)$$

where F_e is the electrostatic pull-down force, and F_c represents the attractive van der Waals forces (first component) and the repulsive nuclear contact forces (second component) between the metal and dielectric layers [26] -[27]. The constants $C_1 = 10^{-80}$ N m determines the surface energy due to the van der Waals attraction, and $C_2 = 10^{-75}$ N m⁸ determines the equilibrium distance from the surface (in this case, 58 Å). These numbers are a strong function of the microstructure of the surface and were chosen here to allow easy convergence of the numerical simulations. In general, surface interactions are very complex and cannot be modeled well by lumped 1-D models such as the one presented here.

The model in this chapter assumes that the movable beam is perfectly planar above the pull-down electrode and that the Q is given by Eq. 2.50 all the way down to $g = 0$. Both of these assumptions are not correct; and the current acceleration and values obtained using the simulations below should be taken as descriptive as $g \rightarrow 0$. Still, one can obtain a lot of information by studying the effect of Q , V_s , R_s , and so on, on the dynamic response of MEMS switches. Also, the model should agree well with experimental values up to $g \simeq 0.1$ μm, and therefore it should predict the switching mechanisms of series switches quite accurately (when no contact is made between the beam and the pull-down electrode). Of course, the model is not valid after impact because it is a simple 1-D model and does not take into account all the higher-order modes on the MEMS beam. The analysis applies equally well to fixed-fixed and cantilever beams. In the following sections, we will assume that the beam has the characteristics shown in Table 2.1 and is of the fixed-fixed type.

2.10 Switching and Release time calculations

2.10.1 Switching Time

The switching time is obtained using Eq. 2.51 and is defined when $x = g_0$. The voltage on the switch is constant ($R_s = 0$), and the damping factor is displacement-dependent [Eq. 2.50]. Figures 2.19 and 2.20 present the time-domain response for the gold and Al beams for different Q and applied voltages. It is seen that the switching time depends strongly on the applied voltage since the larger the voltage, the stronger the electrostatic force. There is also a substantial improvement from $Q = 0.2$ to $Q = 2$, but little improvement above $Q = 2$.

Table 2.1: Characteristics of the MEMS Beam for the Simulations

Parameter	Symbol	Value
Length	l	300 μm
Thickness	t	0.8 μm
Pull-down electrode length	W	100 μm
Bridge width	w	100 μm
Gap height	g_0	3 μm
Spring constant (Au and Al)	k	10 N/m
Residual stress (Au)	σ	9.5 MPa
k Components (Au)	k', k''	($k' = 2.67$ N/m, $k'' = 7.33$ N/m)
Density of Al	ρ_{Al}	2,700 kg/m ³
Density of Au	ρ_{Au}	19,320 kg/m ³
Effective mass	m_e	0.35(lwt) ρ
	$m_{eff, Al}$	22.7 nanogram
	$m_{eff, Au}$	162 nanogram
Mechanical resonance frequency (Al)	$f_{0, Al}$	106 kHz
Mechanical resonance frequency (Au)	$f_{0, Au}$	39.5 kHz

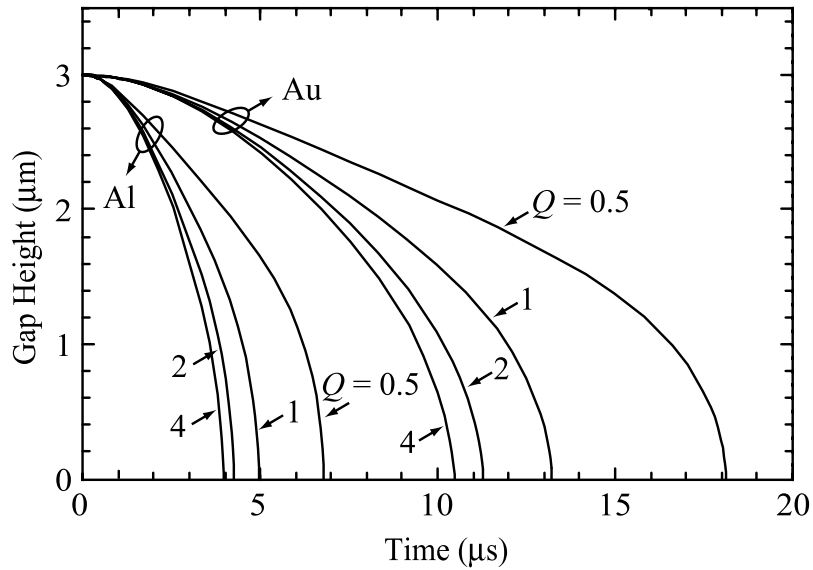


Figure 2.19: Pull-down simulations for the Au and Al beams of Table 2.1 for an applied voltage of 42V ($V_s = 1.4V_p$).

The switching times are very similar for the case of constant damping since the electrostatic force is quite large for a small gap height.

A closed-form solution for the switching time can be obtained for inertia-limited systems (acceleration limited)-that is, for beams with a small damping coefficient

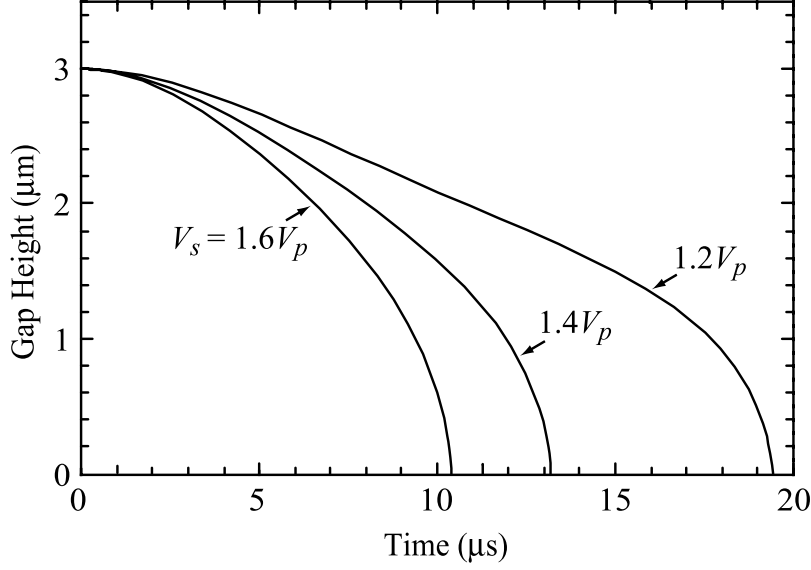


Figure 2.20: Pull-down simulations for the Au beam of Table 2.1 versus the applied voltage, and $Q = 1$.

and $Q \geq 2$. The equation of motion becomes ($b \simeq 0$)

$$m \frac{d^2 x}{dt^2} + kx = -\frac{1}{2} \frac{\varepsilon_0 A V^2}{g_0^2} \quad (2.57)$$

where the force is taken to be constant and equal to the initial applied force.

The solution is

$$t_s \simeq 3.67 \frac{V_p}{V_s \omega_0} \quad (2.58)$$

and $t_s = 10.6 \mu\text{s}$ and $4 \mu\text{s}$ for the Au and Al beams of Table 2.1 with $V_s = 1.4V_p$. It is seen that the closed-form value of t_s agrees well with the numerical modeling for $V_s \geq 1.3V_p$ and $Q \geq 2$ (Fig. 2.21). The above formula also agrees with measurements done by Barker [28]. In most cases, the applied voltage is $1.3-1.4V_p$ to result in a fast switching time at a reasonable voltage level. If the system is damping limited ($Q \leq 0.5$), then a similar equation can be derived, as was done by Castaner and Senturia [29]-[30] with the assumption of constant damping with gap height and neglecting the acceleration and spring component. The equation of motion becomes

$$b \frac{dx}{dt} = F_e \quad (2.59)$$

and can be solved with integral methods or estimated with difference methods.

The solution using integral methods and $F_e = (\varepsilon_0 w W V^2)/2g^2$ results in

$$t_s = \frac{2bg_0^3}{3\varepsilon_0 A V_s^2} \simeq \frac{9V_p^2}{4\omega_0 Q V_s^2} \quad V_s \gg V_p \quad (2.60)$$

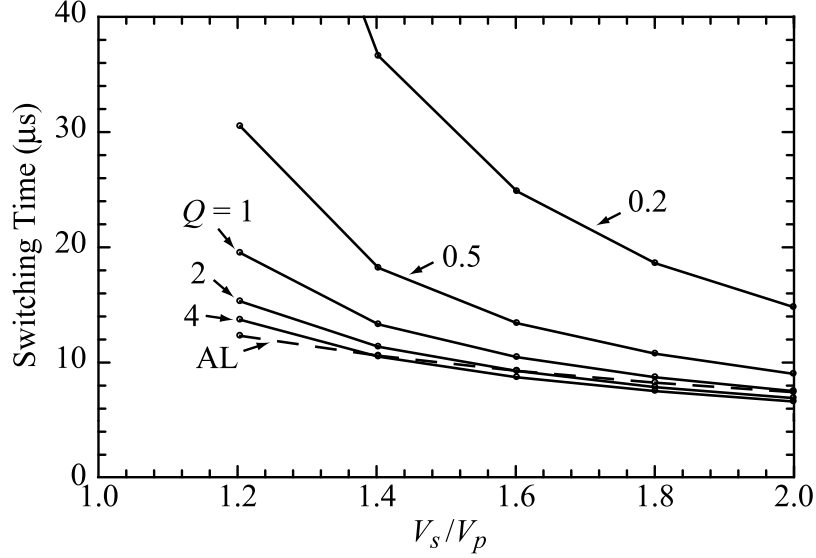


Figure 2.21: Simulated switching times for the Au beam given in Table 2.1. AL means acceleration-limited and is given by Eq. 2.58.

Another estimate can be made by assuming a constant F_e and a constant velocity approximation ($dx/dt = g_0/t_s$). This switching time estimate is given by

$$t_s = \frac{2bg_0^3}{\varepsilon_0 AV_s^2} \simeq \frac{27V_p^2}{4\omega_0 QV_s^2} \quad V_s \gg V_p \quad (2.61)$$

For the damping-limited case, Eq. 2.61 tends to overestimate the switching time and Eq. 2.60 tends to underestimate the switching time.

2.10.2 Release Time

The nonlinear dynamic analysis equation can also be used to model the release mechanism of the switch, and is done by setting $F_e = 0$. The restoring force is given by $kg_0 + k_s g_0^3$ and is 55 mN for the switch of Table 2.1. Figure 2.22 presents the release response for the Au beam and $Q = 0.5, 1, 2$. For $Q = 2$, the beam oscillates and while it does not make any contact with the t-line, it may modulate the power response on the t-line for tens of microseconds. The effect of the variable damping is much greater on the calculation of the release time since $F_e = 0$ and is dependent on the choice of the experimental factor of 1.1 [see Eq. 2.50]. A $Q \simeq 1$ is recommended for the best release response.

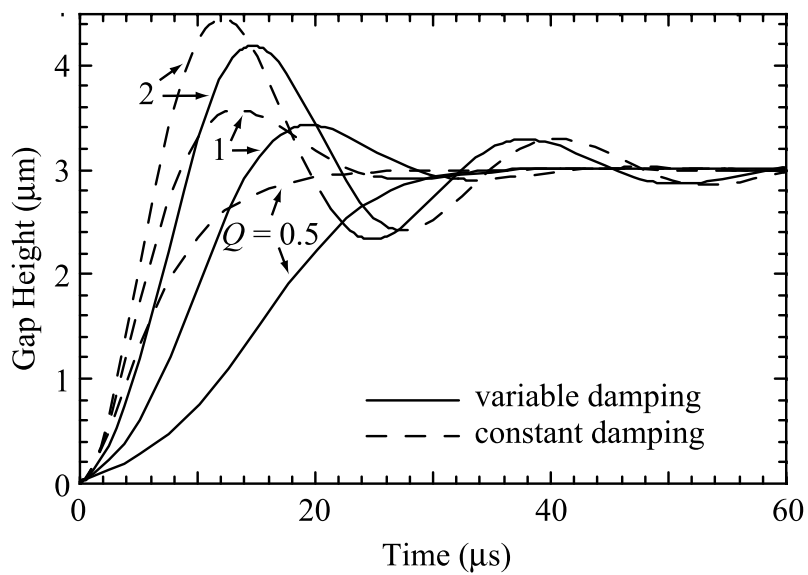


Figure 2.22: Release simulations for the Au beam of Table 2.1 with $Q = 0.5, 1, 2$ and a restoring force of 55 mN. Constant and variable Q cases are considered.

2.11 Charge trapping consideration

The charge trapping phenomenon is considered the most compromising problem for the reliability of RF-MEMS switches. In literature, we can find two dimensional electrostatic simulation that underline the structural points where the electrical field is maximum and so the points where the probability of charge trapping is potentially higher [31]. As it is shown in Fig. 2.23, the applied electrical field is higher in the air-gap between the bridge and the actuation electrode, but there are other areas into the substrate below where the estimated electrical field is higher than 50 MV/m; this can be sufficient to inject charge in the localized points of the substrate.

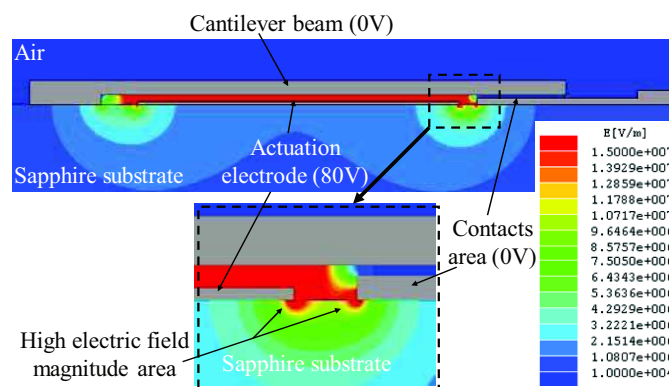


Figure 2.23: Maxwell EM simulations of a switch in the down state. Simulated electric field distribution in dielectricless switches under 60 V considering the switch in close state position.

The trapped or redistributed charge during the actuation process can lead to a shift of the actuation and release voltage. In the worst case the *stiction phenomenon* can occur. In fact, a uniform distributed charge inside the dielectric layer of the device can lead to a shift of the capacitance voltage curve (C - V) like shown in Fig. 2.24 [32].

In addition to lowering of the actuation voltage (pull-in voltage), the trapped charge also lowers the release voltage of the device (pull-out voltage); this effect can lead to a partial *stiction condition* or in the worst case to an irreversible sticking (Fig. 2.25).

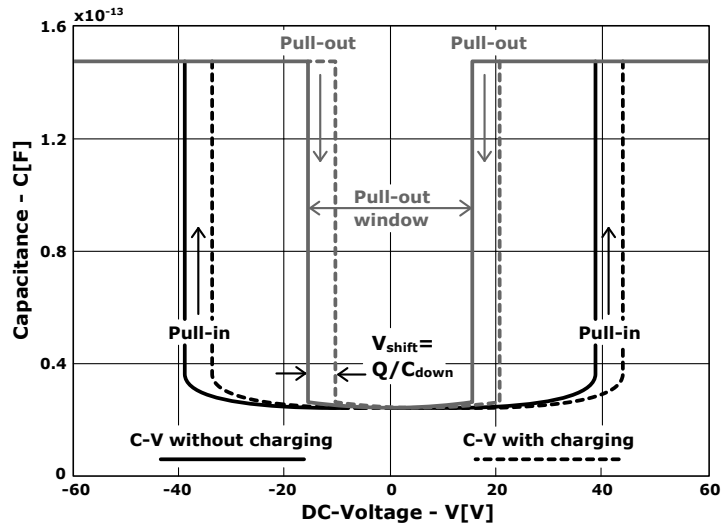


Figure 2.24: $C - V$ curve with an uniform charging (i.e. zero-variance).

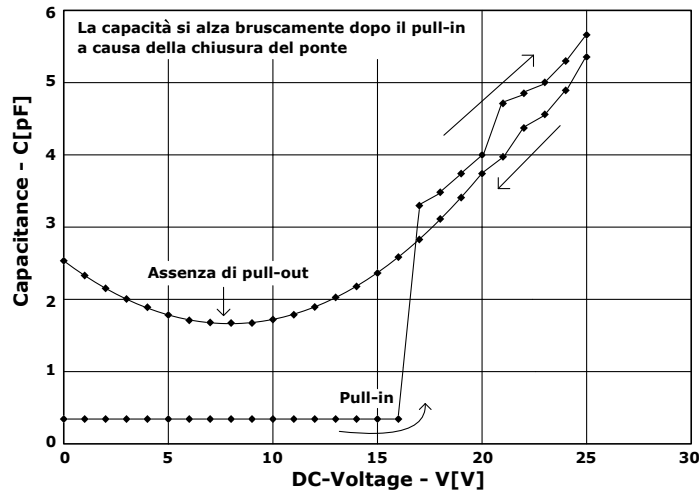


Figure 2.25: $C - V$ curve showing the stiction of a shunt switch.

2.12 Model of the parallel plate capacitor

In the following, it is presented the theoretical analysis of the parallel plate capacitor that permits to estimate the relationship between the accumulated charge in a dielectric layer and the effects on the actuation voltage of the device [33]. The model is based on a parallel plate capacitor in air, with a dielectric layer at the base of one of the two electrode (fixed electrode). The schematic view of the structure is visible in Fig. 2.26.

At the interface between the dielectric layer and the air, a parasitic charge surface density is present (symbol: σ_p). From this capacitor, a small portion of area

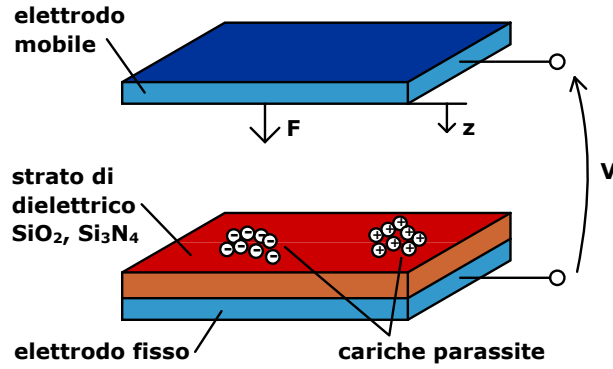


Figure 2.26: Parallel plate model.

(dA) shall be cut out. We assume that across this section σ_p as well as the fields in the dielectric and the air gap are considered to be homogeneous (Fig. 2.27). For the simplified model, it is now easy to calculate the influence of the parasitic charge surface density σ_p on the plate surface charge densities σ_1 and σ_2 and on the acting electrostatic force dF_{el} between the plate sections. Because of its ground connection and the assumption of a homogeneous field (i.e. no electrostatic interaction with adjacent sections) the capacitive section has to be electrostatically neutral, i.e.:

$$\sigma_1 + \sigma_2 + \sigma_p = 0. \tag{2.62}$$

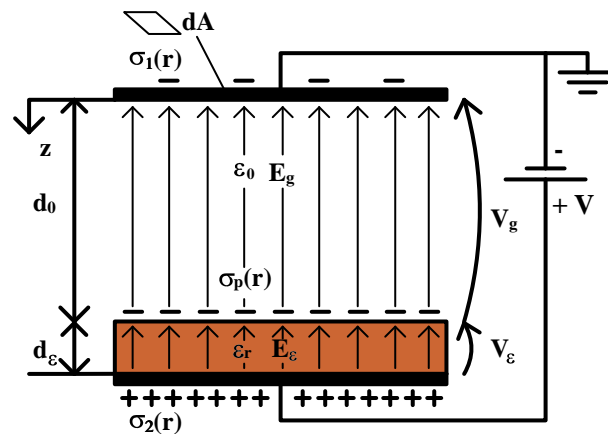


Figure 2.27: Model of a MEMS based on parallel plate capacitor (detail of electric field).

The space outside the arrangement is free of any field. Thus, according to the Gauss flux theorem we obtain for the field in the air gap:

$$E_g = \frac{D_g}{\varepsilon_0} = \frac{-dQ_1}{\varepsilon_0 dA} = -\frac{\sigma_1}{\varepsilon_0} \quad (2.63)$$

and for the field inside the dielectric:

$$E_\varepsilon = \frac{D_\varepsilon}{\varepsilon_r \varepsilon_0} = \frac{dQ_2}{\varepsilon_r \varepsilon_0 dA} = \frac{\sigma_2}{\varepsilon_r \varepsilon_0} = -\frac{\sigma_1 + \sigma_p}{\varepsilon_r \varepsilon_0} \quad (2.64)$$

where D_g e D_ε are the electric flux densities and dQ_1 e dQ_2 are the plate charges present in the section of the electrodes. The applied external voltage divides in the voltage presents on the dielectric layer plus the voltage presents in the air gap:

$$V = V_g + V_\varepsilon = E_g(d_0 - z) + E_\varepsilon d_\varepsilon = -\sigma_1 \frac{d_0 - z}{\varepsilon_0} - [\sigma_1 + \sigma_p] \frac{d_\varepsilon}{\varepsilon_r \varepsilon_0}. \quad (2.65)$$

Using the equations 2.62 - 2.65 one obtains the charge densities σ_1 e σ_2 :

$$\sigma_1 = -\frac{V + \sigma_p \frac{d_\varepsilon}{\varepsilon_r \varepsilon_0}}{\frac{d_0 - z}{\varepsilon_0} + \frac{d_\varepsilon}{\varepsilon_r \varepsilon_0}} = -C'V - \frac{\sigma_p}{\frac{C'_d}{C'_g} + 1} \quad (2.66)$$

and

$$\sigma_2 = -(\sigma_1 + \sigma_p) = -\frac{V - \sigma_p \frac{d_0 - z}{\varepsilon_0}}{\frac{d_0 - z}{\varepsilon_0} + \frac{d_\varepsilon}{\varepsilon_r \varepsilon_0}} = C'V - \frac{\sigma_p}{\frac{C'_g}{C'_d} + 1} \quad (2.67)$$

where $C'_g = \varepsilon_0/(d_0 - z)$ and $C'_d = (\varepsilon_r \varepsilon_0)/d_\varepsilon$ are respectively the capacitances of the air gap and dielectric layer per unit area, $C' = 1/[(d_0 - z)/\varepsilon_0 + d_0/(\varepsilon_r \varepsilon_0)]$ is the capacitance per unit area resulting from the C'_g and C'_d series arrangement. The equations 2.66 and 2.67 show that the parasitic charge σ_p generates additional voltage-independent charges on the electrodes:

$$-\frac{\sigma_p}{(C'_d/C'_g + 1)} \quad \text{and} \quad -\frac{\sigma_p}{(C'_g/C'_d + 1)}$$

The attracting force acting within the capacitance section dA can be expressed as:

$$dF_{el} = -\frac{E_g dQ_1}{2} = \frac{[\sigma_1]^2 dA}{2\varepsilon_0} = \frac{dA}{2\varepsilon_0} \left(\frac{V + \sigma_p \frac{d_\varepsilon}{\varepsilon_r \varepsilon_0}}{\frac{d_0 - z}{\varepsilon_0} + \frac{d_\varepsilon}{\varepsilon_r \varepsilon_0}} \right)^2 = \frac{[V - V_p]^2}{2} \frac{dC'}{dz} dA \quad (2.68)$$

For the whole capacitor, the force amounts to

$$F_{el} = \int_{(A)} dF_{el} = \frac{\varepsilon_0}{2} \int_{(A)} \left[\frac{V + \sigma_p \frac{d_\varepsilon}{\varepsilon_0 \varepsilon_r}}{(d_0 - z) + \frac{d_\varepsilon}{\varepsilon_r}} \right]^2 dA = \frac{dC'}{dz} \int_{(A)} \frac{[V - V_p]^2}{2} dA \quad (2.69)$$

where

$$V_p = \frac{-\sigma_p d_\varepsilon}{\varepsilon_r \varepsilon_0} = \frac{-\sigma_p}{C'_d} \quad (2.70)$$

is an offset voltage leading to a shift of the parabolic force vs. voltage curve within dA . Thus, sensors and actuators are subjected to an additional electrostatic force depending nonlinearly on the applied voltage and the displacement.

2.13 Pull-in/out voltages (parallel plate model)

Consider a fixed metal plate covered with a dielectric layer divided into two parts with equal areas 2.28 [34]. The two dielectric islands have uniform fixed surface charges of opposite sign ($+Q$, $-Q$). A movable metal plate is fastened with a spring above the dielectric layer. A dc voltage is applied across the two plates. The $+Q$, $-Q$ charges shift the local voltage-force characteristics by $+/- V_{shift}$, which are opposite quantities for the two dielectric islands.

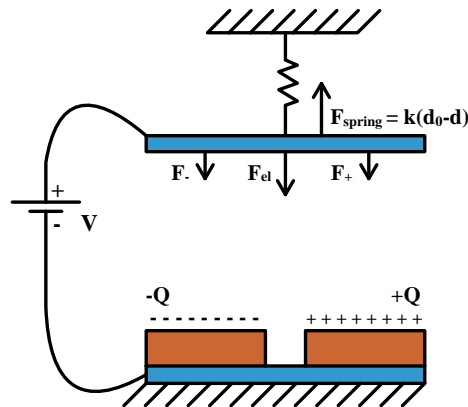


Figure 2.28: Mathematical model of the MEMS Switch charge trapping phenomenon.

Fig. 2.29 describes the electrostatic force F_{el} exerted on the top plate of Fig. 2.28 as a function of the applied voltage V and for a given and fixed position. As $F_{el}(V) = F_+(V) + F_-(V)$ and $F_\pm(V)$ define the red parabolas crossing at $V = 0$, $F_{el}(V)$ describes another narrower parabola in black centered on $V = 0$. It shows a simple force offset compared to the dashed characteristic, i.e., $F_{el_no_Q}$, which is obtained in the total absence of trapped charge. However, the top plate carries no net charge at $V = 0$; the charged dielectric islands induce on this plate charges of opposite polarity that produce this force offset $F_{el}(0)$.

Consider the setup in Fig. 2.30. A fixed metal plate of area A is covered with a

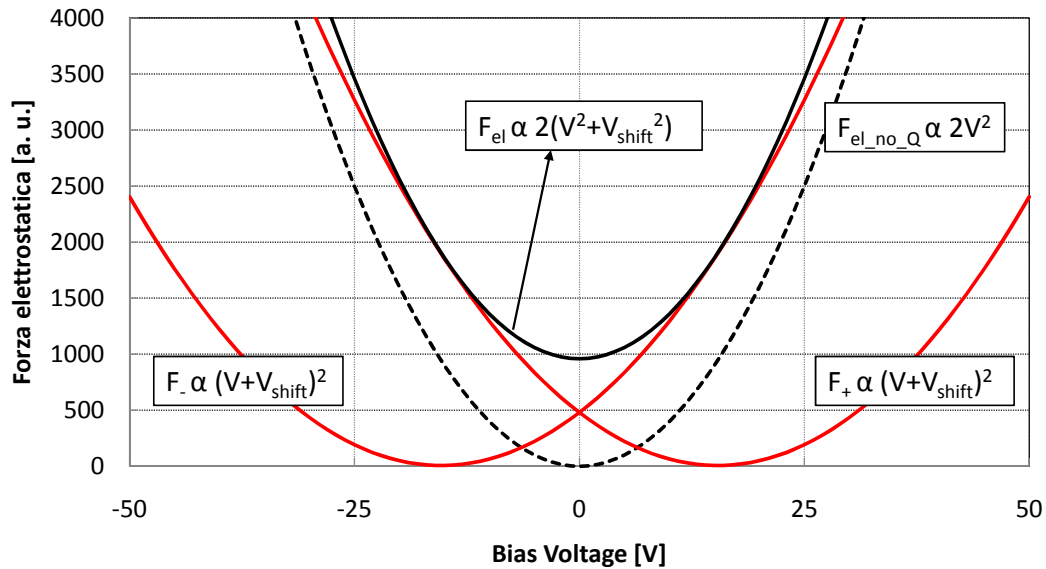


Figure 2.29: Description of the electrostatic force exerted on the moving plate at a given and fixed position as a function of the applied voltage V in the stiction mathematical model experiment of Fig. 2.28.

dielectric layer of thickness d_ε , dielectric constant ε_r , and volume charge density $\psi(x, y, z)$. A rigid movable metal plate is fastened with a spring k to a fixed wall above the dielectric layer at a rest position d_0 . A DC voltage source of amplitude V is applied to the two plates. The setup is placed in vacuum.

Using Gauss' law and assuming the electric field is everywhere aligned with the

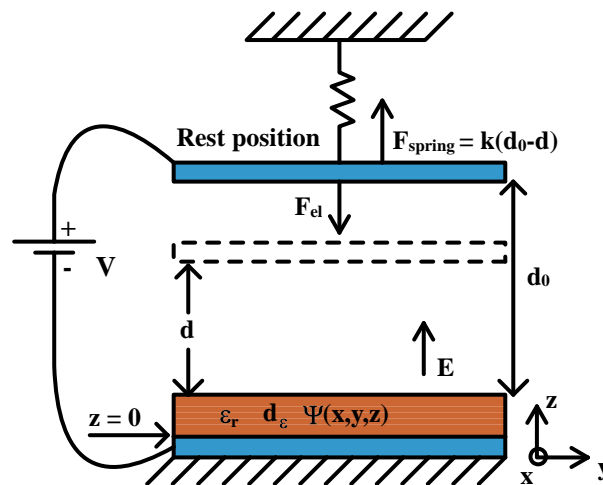


Figure 2.30: Model of a RF MEMS with distributed charging.

z-axis, F_{el} given by:

$$F_{el}(d) = \frac{\varepsilon_0}{2} \int_{(A)} \left[\frac{V - \frac{\psi_{eq}(x,y)d_\varepsilon}{\varepsilon_0\varepsilon_r}}{d + \frac{d_\varepsilon}{\varepsilon_r}} \right]^2 dx dy \quad (2.71)$$

where d is the gap spacing and

$$\psi_{eq}(x, y) = \int_0^{d_\varepsilon} \int_\alpha^{d_\varepsilon} \frac{\psi(x, y, z)}{d_\varepsilon} dz d\alpha \quad (2.72)$$

is the equivalent surface charge distribution defined as the surface charge distribution placed at $z = d_\varepsilon$ which produces the same electrostatic force as the actual $\psi(x, y, z)$. The formula just written is not in contrast with 2.69 since in Fig. 2.27 and 2.30 the reference for the applied voltage is reverse and also the position reference for z is opposite.

Note that a charge Q placed at the surface of the dielectric has an equivalent $Q_{eq} = Q$ while the same charge Q placed at the bottom of the dielectric has an equivalent $Q_{eq} = 0$. The stable and unstable electromechanical equilibrium positions of the movable plate are obtained by balancing $F_{el}(d)$ with the spring force $F_{spring} = k(d_0 - d)$ and are thus expressed by

$$V = \frac{\overline{\psi_{eq}}d_\varepsilon}{\varepsilon_0\varepsilon_r} \pm \sqrt{\frac{2k}{\varepsilon_0 A} (d_0 - d) \left(d + \frac{d_\varepsilon}{\varepsilon_r} \right)^2 - \frac{d_\varepsilon^2 \sigma^2(\psi_{eq})}{\varepsilon_0^2 \varepsilon_r^2}} \quad (2.73)$$

where $\overline{\psi_{eq}}$ and $\sigma^2(\psi_{eq})$ are the mean and variance of the equivalent surface charge distribution ($\psi_{eq}(x, y)$).

On the one hand, the mean equivalent charge results in a shift of the $d - V$ and $C - V$ curves, on the other hand, the variance of $\psi_{eq}(x, y)$ affects the shape of the actuation characteristics. The non-zero variance has the effect of a permanent force offset. Note for example that a non-zero variance forbids the rest position of the spring $d = d_0$ as an equilibrium position for the system.

The release voltage (*pull-out voltage*, V_{PO}), obtained from 2.73 with $d = 0$, is a parabolic function of the charge variance, given by

$$V_{PO} = \frac{\overline{\psi_{eq}}d_\varepsilon}{\varepsilon_0\varepsilon_r} \pm \sqrt{\frac{2kd_0d_\varepsilon^2}{\varepsilon_0\varepsilon_r^2 A} - \frac{d_\varepsilon^2 \sigma^2(\psi_{eq})}{\varepsilon_0^2 \varepsilon_r^2}} \quad (2.74)$$

Increasing the variance, the two symmetric V_{PO} shift towards each other, as shown in Fig. 2.31 and 2.32 in the case of a zero mean charge.

This phenomenon can bring to the failure of the switch due to stiction occurrence. The release voltage vanishes for a variance of $\psi_{eq}(x, y)$ independent of the

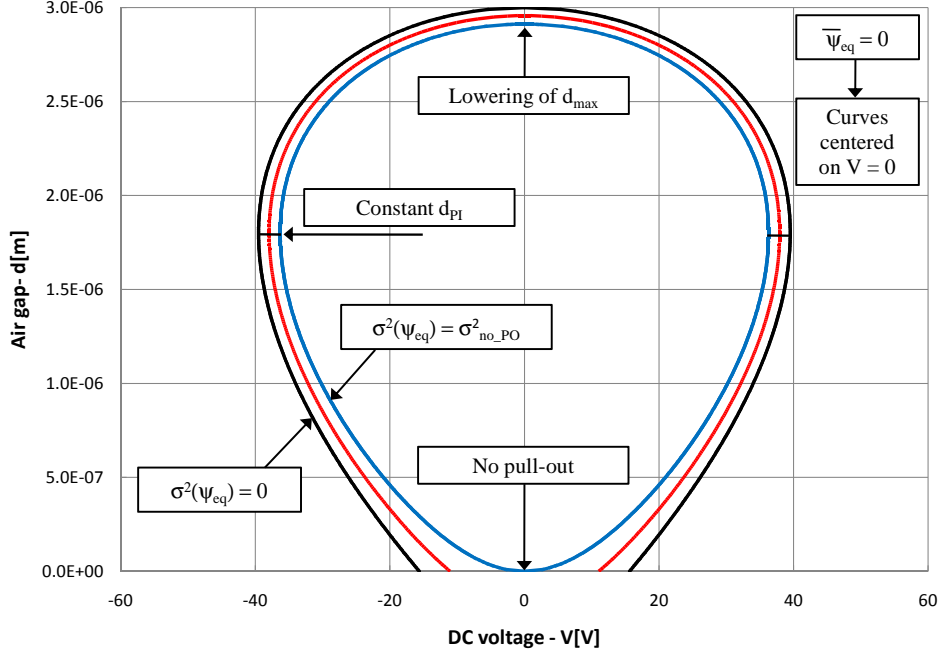


Figure 2.31: Simulated narrowing of the full $d - V$ curve increasing $\sigma^2(\psi_{eq})$ from 0 until $\sigma_{no_PO}^2$.

dielectric layer parameters and given by

$$\sigma_{no_PO}^2 = \frac{2kd_0\varepsilon_0}{A} \quad (2.75)$$

From 2.73 we can easily show that the gap spacing at pull-in d_{PI} is not affected by the charging and is still given by $(2d_0 - d_\varepsilon)/3$. V_{PI} is a function of the charging given by

$$V_{PI} = \frac{\overline{\psi_{eq}}d_\varepsilon}{\varepsilon_0\varepsilon_r} \pm \sqrt{\frac{8k}{27\varepsilon_0A} \left(d_0 + \frac{d_\varepsilon}{\varepsilon_r}\right)^3 - \frac{d_\varepsilon^2\sigma^2(\psi_{eq})}{\varepsilon_0^2\varepsilon_r^2}}. \quad (2.76)$$

V_{PI} can also disappear due to the variance $(\psi_{eq}(x, y))$. The critical variance for the pull-in is given by

$$\sigma_{no_PI}^2 = \frac{8k\varepsilon_0d_\varepsilon}{27A\varepsilon_r} \left(1 + \frac{\varepsilon_r d_0}{d_\varepsilon}\right)^3. \quad (2.77)$$

Fig. 2.33 and 2.34 show simulations equivalent to 2.31 and 2.32 increasing the variance from $\sigma_{no_PO}^2$ to $\sigma_{no_PI}^2$.

The whole $d - V$ e $C - V$ characteristics gradually vanish. As there is no more

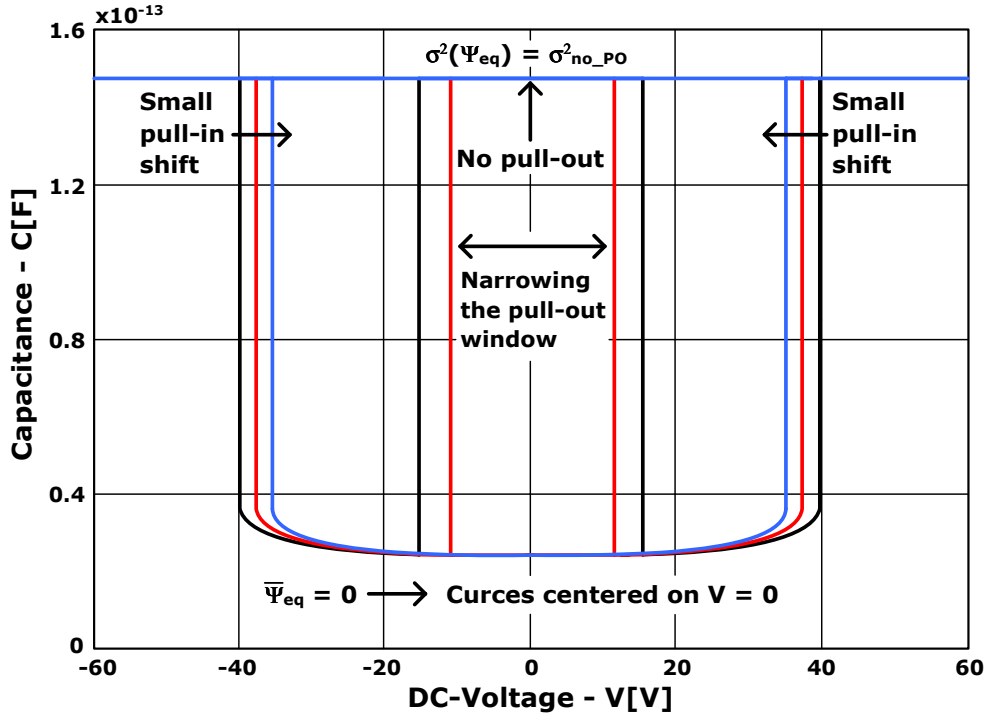


Figure 2.32: Simulated narrowing of the stable $C - V$ curve increasing $\sigma^2(\psi_{eq})$ from 0 until $\sigma_{no_PO}^2$.

stable position for the movable armature, the device fails by self-actuation due only to the variance of the equivalent surface distribution.

From the formulas, some considerations can be drawn:

1. As $V_{PO} < V_{PI}$ in absence of charge, V_{PO} disappears earlier than V_{PI} ;
2. Imposing $\sigma_{no_PO}^2 = \sigma_{no_PI}^2$ we get $d_\epsilon = 2\epsilon_r d_0$. This condition is equivalent to $V_{PI} = V_{PO}$;
3. A larger spring constant per unit area (k/A), a larger rest air gap (d_0), a thinner dielectric layer (d_ϵ) and a higher dielectric constant (ϵ_r) make a switching device less sensitive to the variance and mean of $\psi_{eq}(x, y)$.

We can say that the variation of $\psi_{eq}(x, y)$ can explain the stiction reversible phenomenon. For clarity the evolution of V_{PI} and V_{PO} as a function of the charging variance are plotted in Fig. 2.35. The V_{PO} curve intersects the zero point at $\sigma^2(\psi_{eq}) = \sigma_{no_PO}^2$.

Until now we have imputed the shift of the V_{PI} and V_{PO} to the variance of the

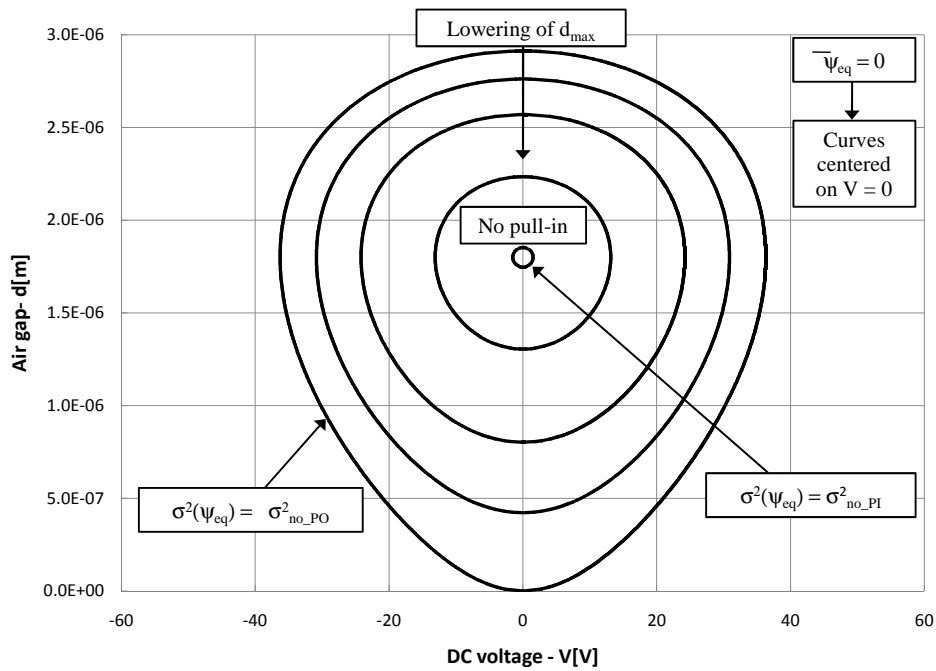


Figure 2.33: Simulated complete closure of the full $d - V$ curve increasing $\sigma^2(\psi_{eq})$ from $\sigma^2_{no_PO}$ until $\sigma^2_{no_PI}$.

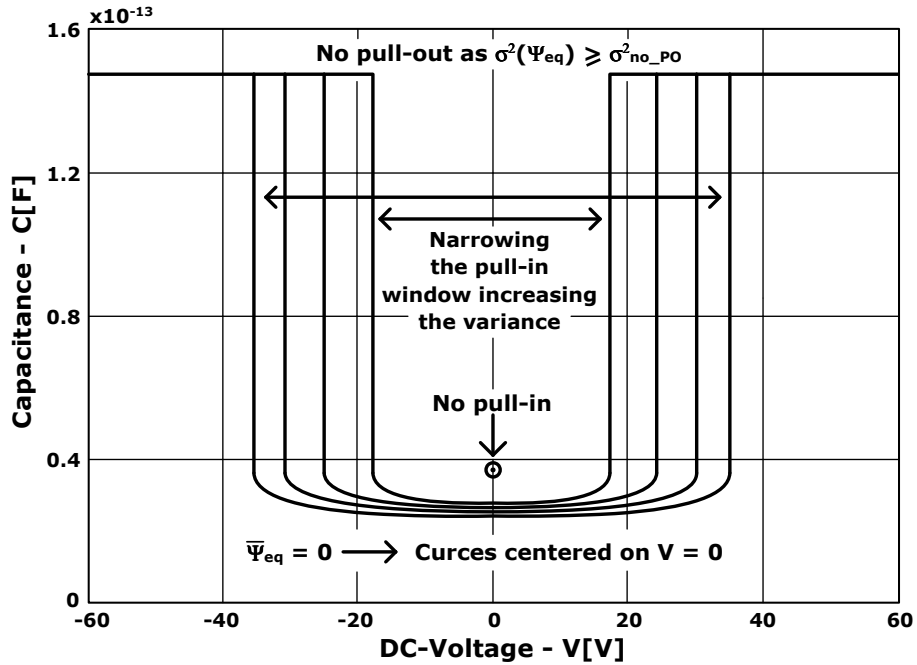


Figure 2.34: Simulated complete closure of the stable $C - V$ curve increasing $\sigma^2(\psi_{eq})$ from $\sigma^2_{no_PO}$ until $\sigma^2_{no_PI}$.

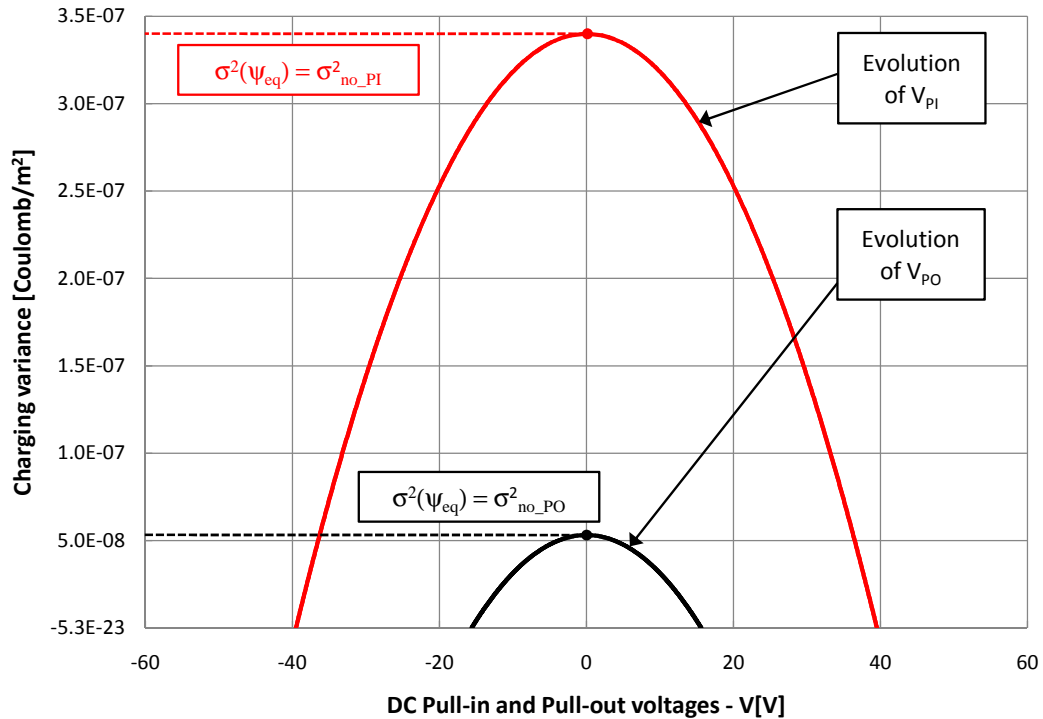


Figure 2.35: Evolution of V_{PI} and V_{PO} vs. $\sigma^2(\psi_{eq})$.

equivalent surface charge distribution, but we haven't analyze the causes that may lead to these changes.

Basically we can find two causes:

- The **fabrication process** is the first source of dielectric charging. The distributions of defects and traps imprinted in the dielectric layer during the processing are determining factors for the charging susceptibility and distribution.
- The **parasitic air gap** remaining upon closure of the device will lead to a distributed injection of charges and therefore a distributed charge in the dielectric. The model here presented assumed rigid plates. In practice however the movable plate deforms during its actuation so that d is also function of (x, y) . The varying gap in the deformed state leads to a varying electric field, which results in a variation in the induced charges. For a shunt switch, the maximal deflection occurs in the center of the bridge. The middle of the dielectric area feels more electromechanical stress. The dielectric thus charges more in the center than at the edges.

2.14 Pull-in/out voltages (nonflat model)

Consider the structure of Fig. 2.36 [34].

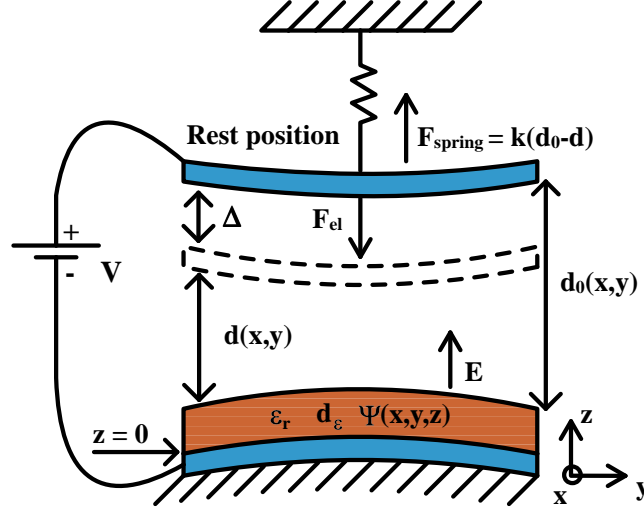


Figure 2.36: Model of a MEMS device with nonuniform trapped charge and air-gap distributions.

A fixed nonflat metal plate of area A is covered with a dielectric layer of uniform thickness d_ϵ , dielectric constant ϵ_r , and volume charge density $\psi(x, y, z)$. A rigid but nonflat movable metal plate is fastened with a linear spring k to a fixed wall above the dielectric layer at a rest position $d_0(x, y)$. A DC voltage source of amplitude V is applied to the two plates. The setup is placed in a vacuum. By using Gauss' law and assuming that the electric field is everywhere aligned with the z -axis, the electric field in the dielectric $E_\epsilon(x, y, \tau)$ is given by:

$$E_\epsilon(x, y, \tau) = \frac{E_{gap}(x, y)}{\epsilon_r} - \int_\tau^{d_\epsilon} \frac{\psi(x, y, z)}{\epsilon_0 \epsilon_r} dz \quad \text{per} \quad 0 < \tau < d_\epsilon \quad (2.78)$$

where $E_{gap}(x, y)$ is the field across the air gap, which is independent of z . Both fields are linked to V by:

$$V = - \int_0^{d_\epsilon} E_\epsilon(x, y, \tau) d\tau - (d_0(x, y) - \Delta) E_{gap}(x, y) \quad (2.79)$$

where $d_0(x, y)$ is the distributed gap spacing at the rest position of the anchoring spring, and Δ is the displacement of the moving electrode from this rest position. From 2.78 and 2.79, we isolate $E_{gap}(x, y)$ that we use to express the electrostatic force F_{el} as

$$F_{el}(\Delta) = \frac{1}{2\epsilon_0} \int_{Area} \alpha(x, y, \Delta)^2 \left[V - \frac{\psi_{eq}(x, y) d_\epsilon}{\epsilon_0 \epsilon_r} \right]^2 dx dy \quad (2.80)$$

where

$$\alpha(x, y, \Delta) = \frac{\varepsilon_0}{(d_0(x, y) - \Delta) + \frac{d_\varepsilon}{\varepsilon_r}} \quad (2.81)$$

is the capacitance distribution and

$$\psi_{eq}(x, y) = \int_0^{d_\varepsilon} \int_\chi^{d_\varepsilon} \frac{\psi(x, y, z)}{d_\varepsilon} dz d\chi \quad (2.82)$$

is an equivalent surface charge distribution. Placed at $z = d_\varepsilon$, $\psi_{eq}(x, y)$ produces the same electrostatic force as the actual $\psi(x, y, z)$. Note that a charge Q placed at the surface of the dielectric has an equivalent $Q_{eq} = Q$ while the same charge placed at the bottom of the dielectric has an equivalent $Q_{eq} = 0$. The equation 2.80 can be further reorganized to obtain the compact and elegant formulation

$$F_{el}(\Delta) = \frac{A}{2\varepsilon_0} [(V\mu_\alpha - \mu_\beta)^2 + V^2\sigma_\alpha^2 + \sigma_\beta^2 - 2V\text{cov}_{(\alpha,\beta)}] \quad (2.83)$$

where

$$\beta(x, y, \Delta) = \frac{d_\varepsilon}{\varepsilon_0\varepsilon_r} \psi_{eq}(x, y) \alpha(x, y) \quad (2.84)$$

is the charge distribution on the top electrode due to the charges trapped in the dielectric. Further, μ , σ^2 and cov denote the mean, variance, and covariance, respectively, of the $\alpha(x, y, \Delta)$ and $\beta(x, y, \Delta)$.

In the approximation of an ideal spring of spring constant k , the magnitude of the spring force exerted on the movable electrode is proportional to the displacement from the rest position and given by

$$F_{spring}(\Delta) = k(d_0(x, y) - d(x, y)) = k\Delta. \quad (2.85)$$

so that the equilibrium positions of the system are determined by equating 2.83 and 2.85 that finally reduce to

$$\frac{2\varepsilon_0 k \Delta}{A} = (V\mu_\alpha - \mu_\beta)^2 + V^2\sigma_\alpha^2 + \sigma_\beta^2 - 2V\text{cov}_{(\alpha,\beta)}. \quad (2.86)$$

We can find now five main general cases:

- **Uniform Equivalent Charge and Air-Gap Distributions**
- **Distributed Equivalent Charge and Uniform Air Gap**
- **Distributed Air Gap in the Absence of Equivalent Charge**
- **Distributed Air Gap and Uniform Equivalent Charge**
- **General Case, Distributed Equivalent Charge and Air Gap**

2.14.1 Uniform Equivalent Charge and Air-Gap Distributions

In this case

$$d_0(x, y) = d_0 \quad \text{and} \quad \psi_{eq}(x, y) = \psi_{eq} \quad (2.87)$$

and the electrostatic force simplifies to

$$F_{el} = \frac{A}{2\varepsilon_0} (V\mu_\alpha - \mu_\beta)^2 = \frac{A\varepsilon_0}{2} \left[\frac{1}{d_0 - \Delta + \frac{d_\varepsilon}{\varepsilon_r}} \right]^2 \left(V - \frac{\psi_{eq}d_\varepsilon}{\varepsilon_0\varepsilon_r} \right)^2. \quad (2.88)$$

The uniform equivalent charging condition translates in a constant shift in the voltage of the $F_{el} - V$. As this voltage shift is independent of the closure of the air-gap height, the profile of the $C - V$ actuation characteristic is not modified by the presence of the charges but is only shifted in voltage, as shown in Fig. 2.24 whit $Q = A\psi_{eq}$. As a result, the pull-in and pull-out voltages are given by

$$V_{PO} = \frac{\psi_{eq}d_\varepsilon}{\varepsilon_0\varepsilon_r} \pm \sqrt{\frac{2kd_0d_\varepsilon^2}{\varepsilon_0\varepsilon_r^2A}} \quad (2.89)$$

$$V_{PI} = \frac{\psi_{eq}d_\varepsilon}{\varepsilon_0\varepsilon_r} \pm \sqrt{\frac{8k}{27\varepsilon_0A} \left(d_0 + \frac{d_\varepsilon}{\varepsilon_r} \right)^3}. \quad (2.90)$$

A uniform equivalent charge distribution cannot explain the irreversible stiction failure of the electrostatic MEMS devices. The shift of the $C - V$ is nevertheless the main failure mechanism in the case of the unipolar actuation, where the bias voltage has always the same polarity.

2.14.2 Distributed Equivalent Charge and Uniform Air Gap

In this case

$$d_0(x, y) = d_0 \quad (2.91)$$

and the electrostatic force simplifies to

$$F_{el} = \frac{A}{2\varepsilon_0} [(V\mu_\alpha - \mu_\beta)^2 + \sigma_\beta^2] \quad (2.92)$$

$$F_{el} = \frac{A\varepsilon_0}{2} \left[\frac{1}{d_0 - \Delta + \frac{d_\varepsilon}{\varepsilon_r}} \right]^2 \left[\left(V - \frac{\overline{\psi_{eq}d_\varepsilon}}{\varepsilon_0\varepsilon_r} \right)^2 + \left(\frac{d_\varepsilon}{\varepsilon_0\varepsilon_r} \right)^2 \sigma^2(\psi_{eq}) \right]$$

where $\overline{\psi_{eq}}$ e $\sigma^2(\psi_{eq})$ are the mean and variance of the equivalent surface charge distribution ($\psi_{eq}(x, y)$).

The electromechanical equilibrium positions of the movable plate are obtained from 2.86 and are, thus, expressed by

$$V = \frac{\overline{\psi_{eq}}d_\varepsilon}{\varepsilon_0\varepsilon_r} \pm \sqrt{\frac{2k}{\varepsilon_0A}(d_0 - d) \left(d + \frac{d_\varepsilon}{\varepsilon_r}\right)^2 - \frac{d_\varepsilon^2\sigma^2(\psi_{eq})}{\varepsilon_0^2\varepsilon_r^2}}. \quad (2.93)$$

While the mean equivalent surface charge shifts the $C - V$ as a whole, like the uniform distribution did in the previous case, the variance $\psi_{eq}(x, y)$ affects the shape of the actuation characteristics. The nonzero variance has the effect of a force offset depending on the air-gap height but not on the polarity of the actuation voltage or on the sign of the trapped charges. Note, for example, that a nonzero variance forbids the rest position of the spring $d = d_0$ as an equilibrium position for the system. This case constitutes, thus, a generalization of our thought experiment where we had just considered a very specific charge distribution. The pull-out and pull-in voltages are given by

$$V_{PO} = \frac{\overline{\psi_{eq}}d_\varepsilon}{\varepsilon_0\varepsilon_r} \pm \sqrt{\frac{2kd_0d_\varepsilon^2}{\varepsilon_0\varepsilon_r^2A} - \frac{d_\varepsilon^2\sigma^2(\psi_{eq})}{\varepsilon_0^2\varepsilon_r^2}} \quad (2.94)$$

$$V_{PI} = \frac{\overline{\psi_{eq}}d_\varepsilon}{\varepsilon_0\varepsilon_r} \pm \sqrt{\frac{8k}{27\varepsilon_0A} \left(d_0 + \frac{d_\varepsilon}{\varepsilon_r}\right)^3 - \frac{d_\varepsilon^2\sigma^2(\psi_{eq})}{\varepsilon_0^2\varepsilon_r^2}}. \quad (2.95)$$

Increasing the variance of $\psi_{eq}(x, y)$, the two symmetric pull-in and pull-out voltages shift toward each other.

This is the equivalent case of the previous paragraph.

2.14.3 Distributed Air Gap in the Absence of Equivalent Charge

In this case

$$\psi_{eq}(x, y) = 0 \quad (2.96)$$

and the electrostatic force simplifies as

$$F_{el} = \frac{AV^2}{2\varepsilon_0} [\mu_\alpha^2 + \sigma_\alpha^2]. \quad (2.97)$$

This formula resembles the one derived in 2.92 in the special case where $\mu_\beta = 0$. The variance of the capacitance distribution, which is introduced by the nonuniform air gap in the capacitor, produces an offset of the electrostatic force. The

device of capacitance $A\mu_\alpha$ behaves, for what the actuation concerns, as another device, presenting a larger effective capacitance that is equal to $A\sqrt{\mu_\alpha^2 + \sigma_\alpha^2}$. All other things being equal, a MEMS capacitor with nonuniform capacitance distribution is, thus, more prompt to be actuated than a parallel-plate capacitor. As the electrostatic force offset is in this case proportional to the square of the bias voltage, the device will always fully reopen when a zero bias voltage is applied. From 2.97, the equilibrium locus cannot be generally expressed as in 2.93, in function of the displacement Δ , which is hidden in the mean and variance of the capacitance distribution α . However, 2.97 simplifies in the most general case to

$$V = \pm \sqrt{\frac{2\varepsilon_0 k(d_0(x, y) - d(x, y))/A}{\mu_\alpha^2 + \sigma_\alpha^2}} = \pm \sqrt{\frac{2\varepsilon_0 k\Delta/A}{\mu_\alpha^2 + \sigma_\alpha^2}} \quad (2.98)$$

2.14.4 Distributed Air Gap and Uniform Equivalent Charge

In this case

$$\psi_{eq}(x, y) = \psi_{eq} \quad (2.99)$$

and the electrostatic force simplifies as

$$F_{el} = \frac{A}{2\varepsilon_0} \left(V - \frac{\psi_{eq}d_\varepsilon}{\varepsilon_0\varepsilon_r} \right)^2 [\mu_\alpha^2 + \sigma_\alpha^2]. \quad (2.100)$$

The situation is almost the same as that presented in the previous section. The uniform charge distribution realizes once more a simple shift in voltage of the electrostatic force. The profile of the actuation characteristic is described by

$$V = \frac{\psi_{eq}d_\varepsilon}{\varepsilon_0\varepsilon_r} \pm \sqrt{\frac{2\varepsilon_0 k\Delta/A}{\mu_\alpha^2 + \sigma_\alpha^2}} \quad (2.101)$$

Comparing equation 2.98 with 2.101 it can be seen that the voltage is simply shifted of a constant factor. The two branches of the $C - V$ curve are symmetric. The device fully reopens at $V = \psi_{eq}d_\varepsilon/(\varepsilon_r\varepsilon_0)$.

2.14.5 General Case, Distributed Equivalent Charge and Air Gap

In this case the formula of the electrostatic force cannot be simplified. It is nevertheless obvious that the behavior of the device is more than a mix of the effects previously described. For a complete analysis of this case see [34].

Chapter 3

RF-MEMS, Experimental Set-Ups

The RF MEMS switches are 4 terminals devices: two rf ports for the radio frequency signal (RF_{IN} and RF_{OUT}) and two connection for the DC biasing (GND and V_{BIAS}) that permit the actuation of the switch (Fig. 3.1).

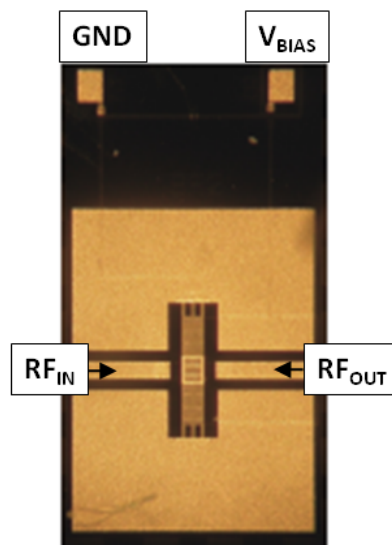


Figure 3.1: Simple illustration of the 4 terminals of an RF MEMS switch.

In order to characterize the performances of the devices, particular electrical LabView controlled measurement set-ups were build up. In the following the description of the different systems are reported:

- **RF and DC characterization Set Up (on wafer devices):** This system permits to extrapolate the classical hysteresis characterization of an RF

MEMS switch. The scattering parameters (S_{21} and S_{11}) are extracted as a function of the applied voltage (V_{BIAS}) for positive and negative biasing voltages.

- **Long Term actuation Set Up (on wafer devices):** This system permits to maintain the switches in down state for prolonged periods of time. During the stress procedure some characterization periods are inserted in order to monitor the performances of the switch under test.
- **Cycling Set Up (on wafer devices):** This system permits to obtain repetitive opening and closing of the switches. During the stress procedure some characterization periods are inserted in order to monitor the performances of the switch under test.
- **Dynamic measurement Set Up (Polytec MAS-500):** The system is a commercial profilometer able to extrapolate the dynamic mechanical response (displacement or velocity) of a membrane that is stimulated by an appropriate electrical signal. The system is used to compare the electrical characterization and the mechanical response. This set up is explained in the results (section: Dynamic measurement results (Polytec MAS-500)).
- **Long Term actuation Set Up (on package devices):** This system is an integrated measurement set up based on a microcontroller. It is able to maintain the switches in down state for prolonged periods of time. During the stress procedure some DC characterization periods appositely timed with the microcontroller are inserted in order to monitor the performances of the switch under test.

3.1 RF and DC characterization Set (on wafer devices)

A schematic representation of the electrical measurement system is presented in Fig. 3.2.

The instruments are:

- Vector Network Analyzer (VNA) 8753E used to generate the RF signal at the input port and to monitor the S-parameters (S_{21} and S_{11}).

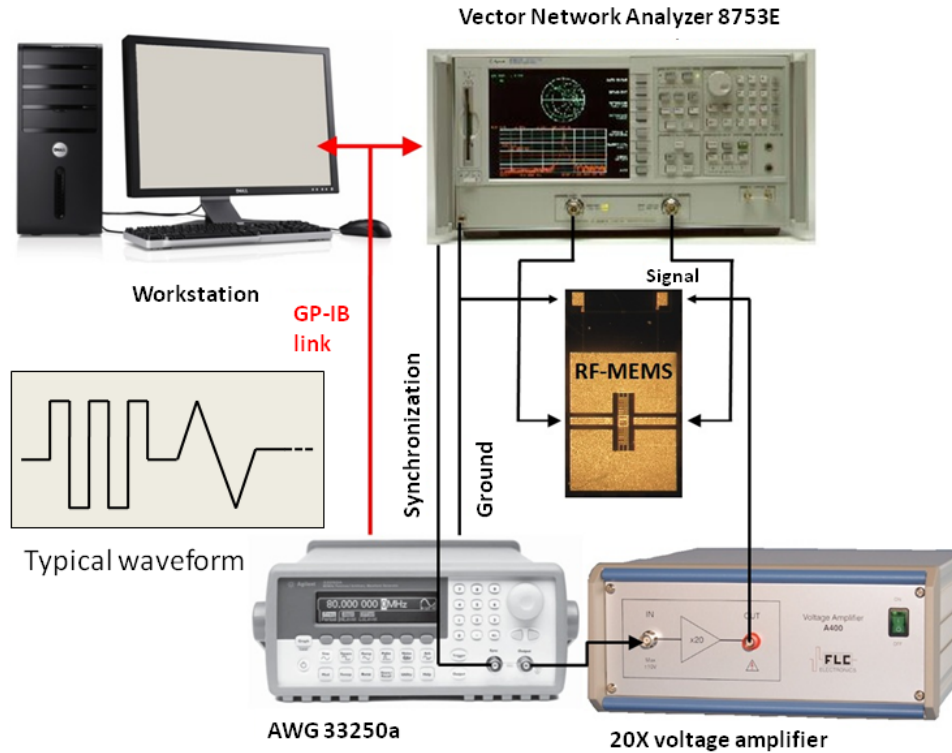


Figure 3.2: Schematic representation of the characterization system.

- Arbitrary Waveform Generator (AWG) Agilent 33250a used to generate the DC biasing waveform.
- Voltage Amplifier FLC 20X used to amplify the AWG voltage (± 5 V) to the biasing voltage of the switches (in the range of 40-80 V).
- Workstation with LabView used to synchronize the different instruments, acquire the data from the VNA and save the results.

The characterization procedure is described in the following: the VNA applies an RF signal at the input port of the switch under test (Frequency: 6 GHz, RF Power: 0 dBm), the RF out port of the switch is connected at the second port of the VNA in order to study the reflection parameter (S_{11}) and the transmission one (S_{21}). The AWG generates a positive staircase ramp from 0 to $+V_{MAX}$, a negative staircase ramp from $+V_{MAX}$ to $-V_{MAX}$ and finally a positive staircase ramp from $-V_{MAX}$ to 0 in 1 second. The VNA is oppositely synchronized with a trigger signal in order to monitor the S-parameters during the entire biasing period. Fig. 3.3 presents the result obtained on a representative switch: it can be seen the positive actuation voltage ($+V_{ACT}$), the positive release voltage

($+V_{REL}$), the negative actuation voltage ($-V_{ACT}$) and the negative release voltage ($-V_{REL}$). Moreover the transmission and reflection RF parameters in off and on state (respectively S_{11} and S_{21} at 0 volt and at V_{MAX}) can be extracted .

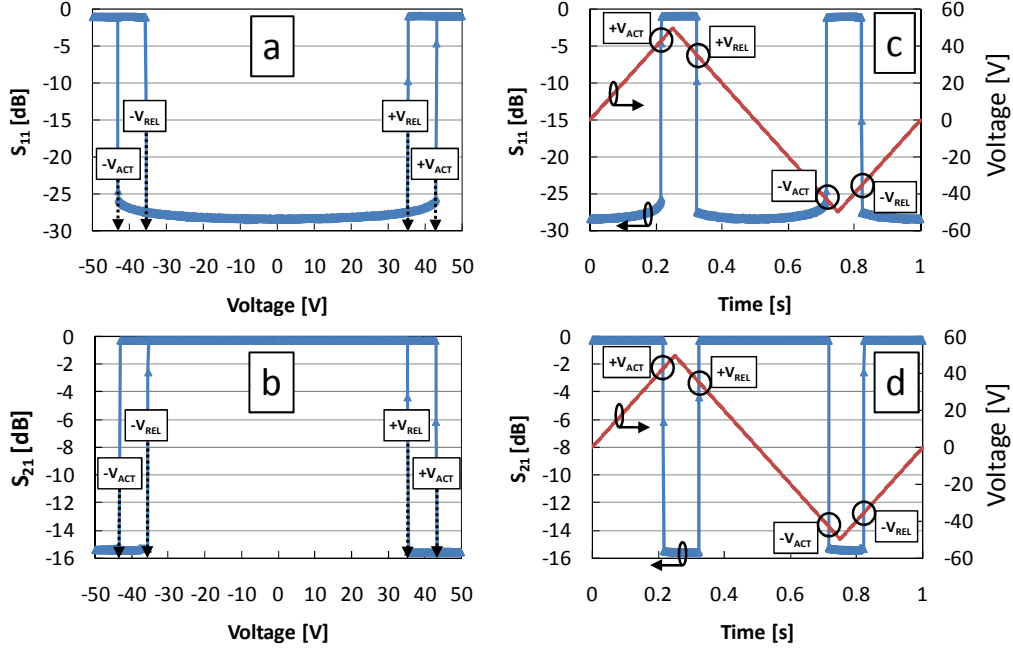


Figure 3.3: Extracted curves for a representative capacitive switch: (a) S_{11} vs applied voltage, (b) S_{21} vs applied voltage, (c) S_{11} vs characterization time and (d) S_{21} vs characterization time.

This kind of characterization highlights the hysteresis of the curves (Fig. 3.3 (a) and (b)): the positive actuation voltage is greater than the positive release voltage. The same can be seen for the negative actuation and release voltages. The difference is due to the minor electrostatic force required to maintain the membrane in down state respect to the same force required to bring the membrane in the low position.

The sketch of the LabView program can be seen in Fig. 3.4. The different parts are explained in the following: “Instruments” are the GP-IB addresses of the instruments, “AWG Parameters” are the settings for the Arbitrary Waveform Generator (“Signal” is set on “Ramp” that generates a triangular Waveform, “Low Voltage” and “High voltage DC” set the maximum and minimum output voltage values, “Period” sets the period of the waveform), “Save Data” is the path for the saving of the data, “Init_VNA” permits to load a particular calibration register of the VNA and to set the RF power and the frequency, “Sweep

number” permits to repeat the characterization for different times in sequence, finally on the right the two graphs “ S_{11} ” and “ S_{21} ” display the results of the characterization procedure.

The characterization procedure is typically repeated two times in sequence in order to investigate any deviation of the two, the RF frequency is set on 6 GHz (maximum of the VNA) and the RF power is set on 0 dBm. This value is sufficiently low to safeguard the contact during the closing and opening operations.

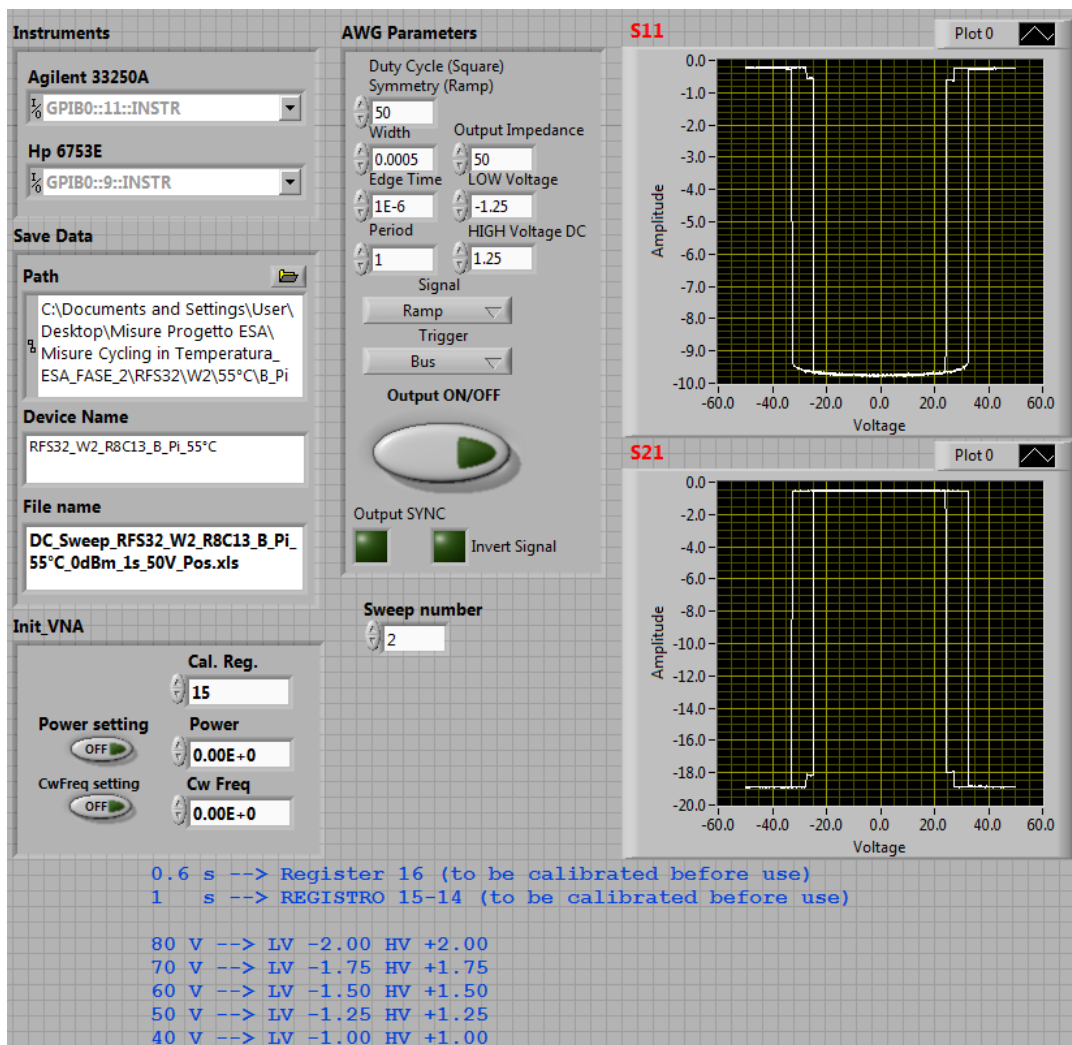


Figure 3.4: Sketch of the LabView program for the characterization system.

3.2 Long Term actuation Set Up (on wafer devices)

The schematic representation of the system is the same of Fig. 3.2. The devices were stressed in DC regime (applying a constant voltage to the actuation pad) and applying a 6 GHz, 0 dBm at the RF-input port. The evolution of the S-parameters during the stress was monitored, as well as the shift (if any) of the electromechanical parameters (V_{ACT+} , V_{REL+} , V_{ACT-} and V_{REL-}) after the stress (recovery phase at $V_{BIAS} = 0$ V) at selected time steps. A schematic representation of the adopted measurement timing is shown in Fig. 3.5. In order to study the influence of continuous actuation on switches, after each time step, a DC sweep was performed in order to investigate any deviation of the main electrical parameters (V_{ACT+} , V_{REL+} , V_{ACT-} and V_{REL-}) from the initial ones. Time steps duration were 10s, 20s, 30s, 50s, ..., and so on, and the applied voltage was $V_{BIAS} = V_{ACT+} + 5$ V. After the stress a relaxation period of some hours was performed. The relaxation period was introduced to analyze the discharge phenomena.

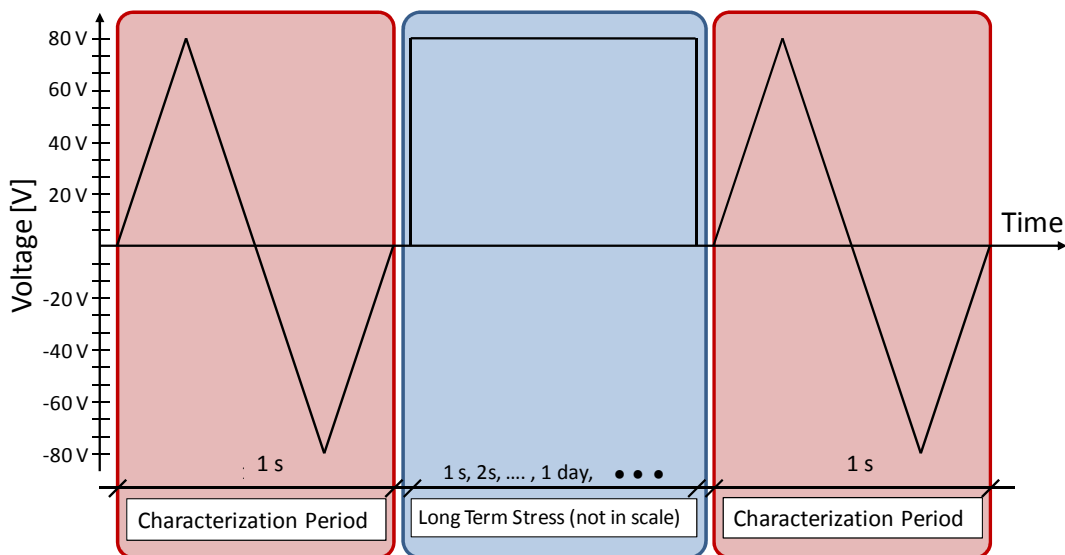


Figure 3.5: Schematic representation of the long term stress procedure timing.

The entire set up is automated and controlled via LabView in order to standardize the measurement procedure (Figure 3.6). The different parts are explained in the following: “Instruments” are the GP-IB addresses of the instruments, “AWG Parameters” are the settings for the Arbitrary Waveform Generator (“Signal” is

set on “Ramp” that generates a triangular Waveform, “Low Voltage” and “High voltage DC” set the maximum and minimum output voltage values, “Period” sets the period of the waveform), “DC Sweep” is the path for the saving of the data, “Init_VNA” permits to load a particular calibration register of the VNA and to set the RF power and the frequency, “Times2” sets the time steps of the prolonged actuation period, “PassoT2” sets the acquisition time step of the RF performances during the prolonged period (this permits to monitor the S-parameters also during the stress), “Stress voltage2” sets the voltage during the different steps (note that it can be also 0 for the recovery phase), “Sweep2” sets the number of characterization procedures that are performed at each step and finally the two graphs “ S_{11} ” and “ S_{21} ” display the results of the characterization procedure during the entire stress.

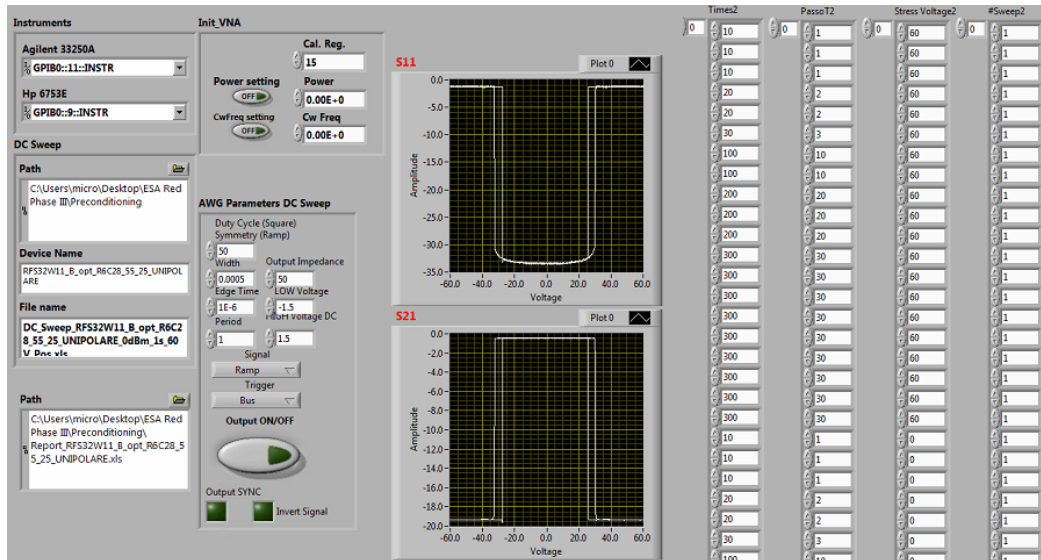


Figure 3.6: Sketch of the LabView program for the long term Set Up.

3.3 Cycling Set Up (on wafer devices)

The schematic representation of the system is the same of Fig. 3.2. The cycling setup is based on an Arbitrary waveform generator in order to properly shape the actuation bias voltage. During the stress, the RF performances and the electrical parameters were monitored in order to analyze the contact degradation and possible charge trapping during the cycling stress procedure (visible from the narrowing and/or the shifting of the release and actuation voltages). A schematic

representation of the adopted measurement timing is shown in Fig. 3.7. The set up was developed respect to the old set up [35] because the characterization phase is obtained with a staircase sweep that permits to monitoring also the actuation and the release voltages. This gives more information regarding the trapping of the device during the cycling stress.

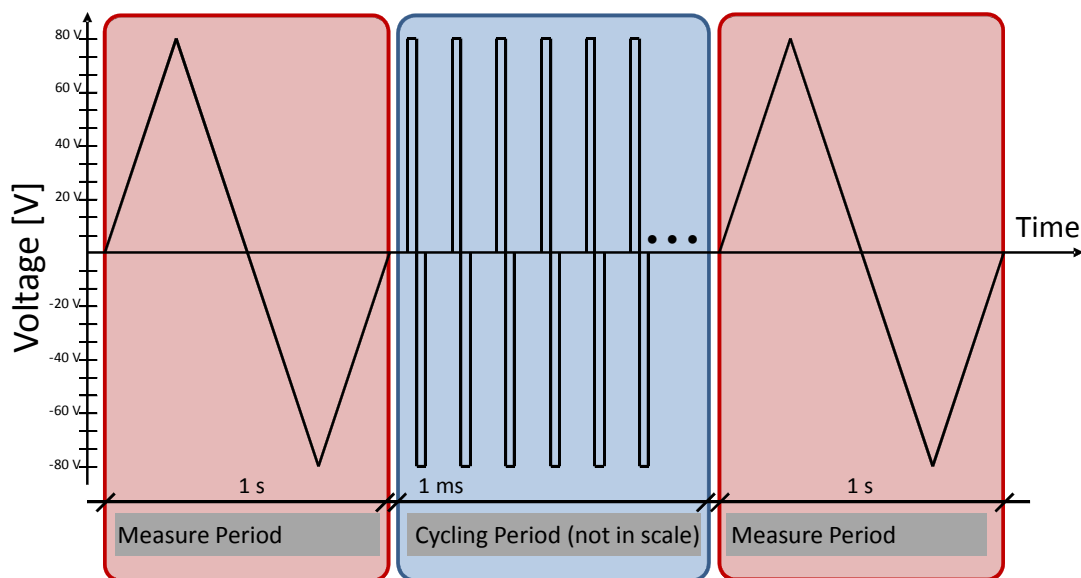


Figure 3.7: Schematic representation of the cycling stress procedure timing.

The entire set up is automated and controlled via LabView in order to standardize the measurement procedure (Figure 3.8). The different parts are explained in the following: “Instruments” are the GP-IB addresses of the instruments, “AWG Parameters” are the settings for the Arbitrary Waveform Generator used during the cycling steps (“Signal” is set on “User” and the waveform is acquired from “PATH FORMA D’ONDA”, “Low Voltage” and “High voltage DC” set the maximum and minimum output voltage values, “Period” sets the period of the waveform), “AWG Parameters DC Sweep” are the settings for the Arbitrary Waveform Generator used during the characterization procedures (“Signal” is set on “Ramp” that generates a triangular Waveform, “Low Voltage” and “High voltage DC” set the maximum and minimum output voltage values, “Period” sets the period of the waveform for the characterization), “DC Sweep” and “Path cycling” are the path for the saving of the data, “HOT-COLD” button permits to decide if the RF power is on or off during the cycling procedure, “Init_VNA” permits to load a particular calibration register of the VNA and to set the RF power and the frequency, “#CICLI” sets the number of cycles for each step of the prolonged

cycling procedure, “sweep” sets the number of characterization procedures that are performed at each step and finally the two graphs “ S_{11} ” and “ S_{21} ” display the results of the characterization procedure during the entire stress.

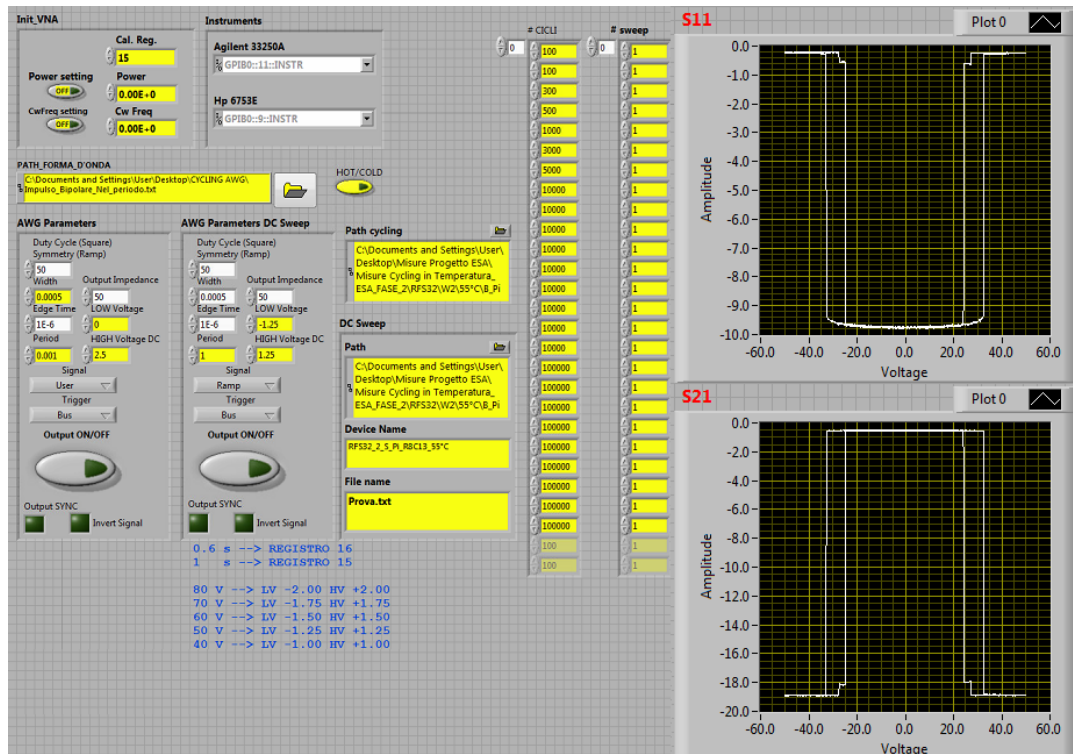


Figure 3.8: Sketch of the LabView program for the cycling measurement Set Up.

3.4 Long Term actuation Set Up (on package devices)

The measurement set up was appositely developed with the aim of optimizing the stress procedure. The stress procedure time line is presented in Figure 3.9: the devices are submitted to a time increasing fixed voltage stress.

After each time step a “characterization period” was performed in order to investigate any deviation of the main electrical parameters (V_{ACT+} , V_{REL+} , V_{ACT-} , V_{REL-}) from the initial ones. It is very important to maintain the time between “characterization period” and “long term stress period” as short as possible in order to have less impact on the charge detrapping phenomenon. With the aim of maintaining all these important restrictions we develop a microcontroller based

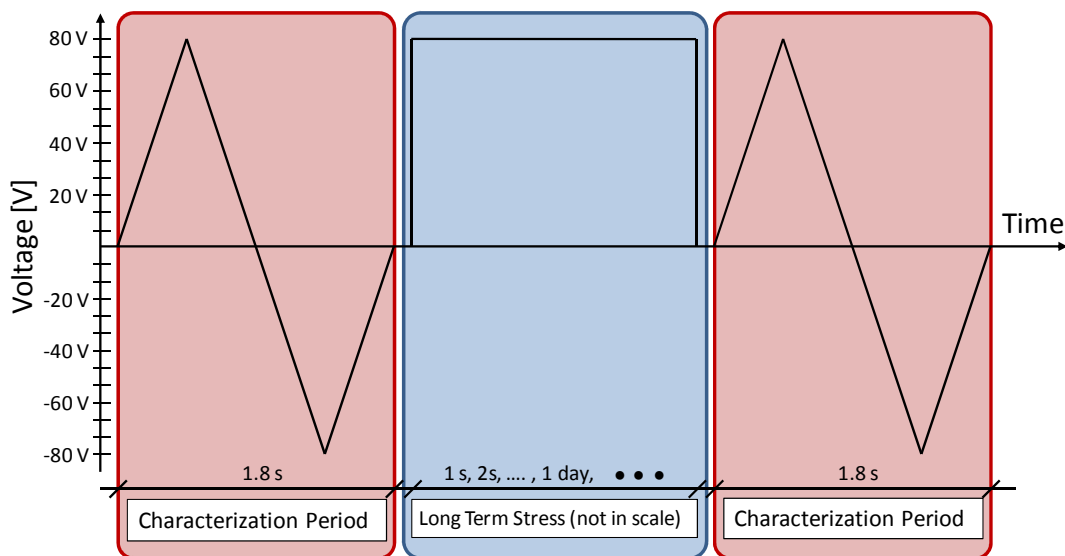


Figure 3.9: Schematic representation of the stress procedure timing.

board able to generate the triangular waveform during the “characterization period” and to stress the devices during the “long stress term period”. A schematic view of the circuit is shown in Figure 3.10. We can distinguish four different areas: the “ACTUATION” part that generates the signal able to actuate the devices, the “RF LINE” part that generates the signal for the RF input of the device, the “SENSING” part that monitors the aperture and the closure of the switch and finally the “DUT”.

The “ACTUATION” part is obtained from the series of the output port of the microcontroller that sends the digitally voltage to a DAC converter, this generates an analog voltage that is shifted and amplified by two consecutive operational amplifier in order to obtain a voltage of ± 100 V. The “RF LINE” part is obtained from the series of the output port of the microcontroller with a DAC converter and an operational amplifier obtaining a voltage of 0-5 V. The “SENSING” part is composed of two resistors that limit the current flow over the RF path of the devices and an ADC (internal to the microcontroller) that acquires the voltage at the input port of the device. The acquired voltage is imposed by the microcontroller in case of open device (we choose arbitrarily 3.8 V) while it is obtained from the resistive partitioning in case of close device (1.9 V).

The four parts of the board are synchronized by the microcontroller that generates the right signals for each part of the circuit. During the “characterization period” the microcontroller generates an opportune staircase waveform and for

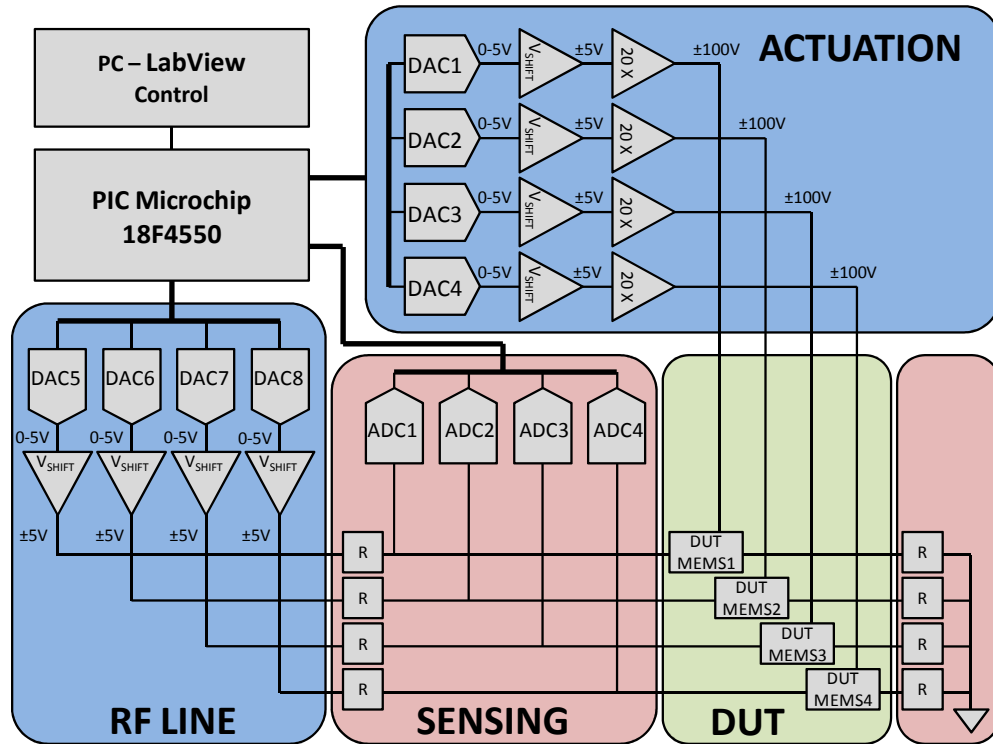


Figure 3.10: Schematic view of the PCB utilized to stress the devices.

each step acquires the information regarding the state of the switch (Figure 3.11). It can be seen that increasing the actuation voltage the ADC acquires 3.8 V whereas the device is open, after the actuation voltage (V_{ACT+}), the device goes into down position and the acquired voltage (1.9 V) is obtained from the partition over the two resistors. In the same way the positive release voltage, the negative actuation voltage and the negative release voltage can be extracted.

The velocity of the measurement set up can be seen from Figure 3.12 where we show two different DSO acquisitions of the biasing voltages and the relative ADC acquired signal. The measures are referred to two different velocity: 1.6 s and 3.2 s. This parameter can be varied from a minimum of 0.8 s to a maximum of 28.8 s by acting on the microcontroller programming. In this paragraph we consider a constant characterization time of 1.6 s that was considered sufficiently short to affect minimally the charge trapping phenomenon and long enough to not influence the dynamic mechanical response of the moving membrane.

With the acquired signal, we can reconstruct a graph like in Figure 3.13 where the positive and negative actuation and release voltages are easily visible. This is the classical hysteresis characteristic of a RF MEMS switch: increasing the voltage

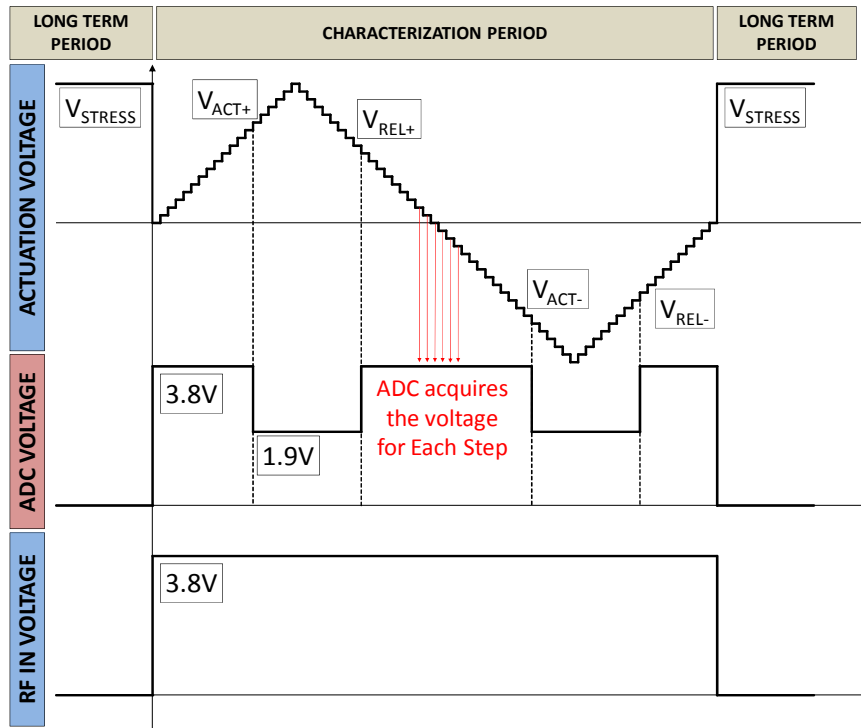


Figure 3.11: Schematic representation of the stress procedure.

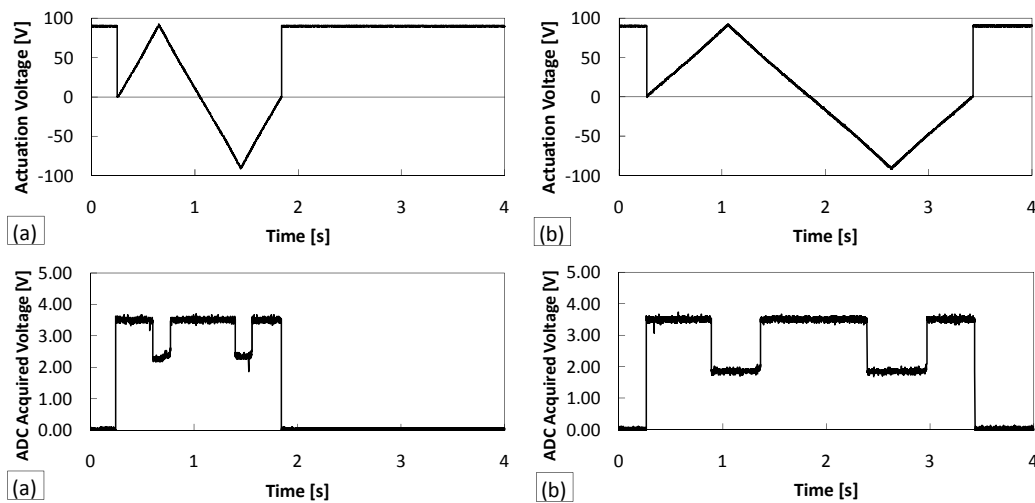


Figure 3.12: Biasing voltages acquired with a DSO during a measurement process for two velocities: (a) 1.6 seconds measurement process and (b) 3.2 seconds measurement process.

the positive actuation voltage is reached (point 1 in figure) and the switch goes in down position, then decreasing the voltage applied to the actuation pad, with

a certain hysteresis, the positive release voltage is reached (point 2 in figure) and the switch goes in up position. The same behavior is visible for negative voltages (points 3 and 4 in figure). It can be clearly noticed that the characterization is obtained monitoring the ADC acquired signal from the microcontroller.

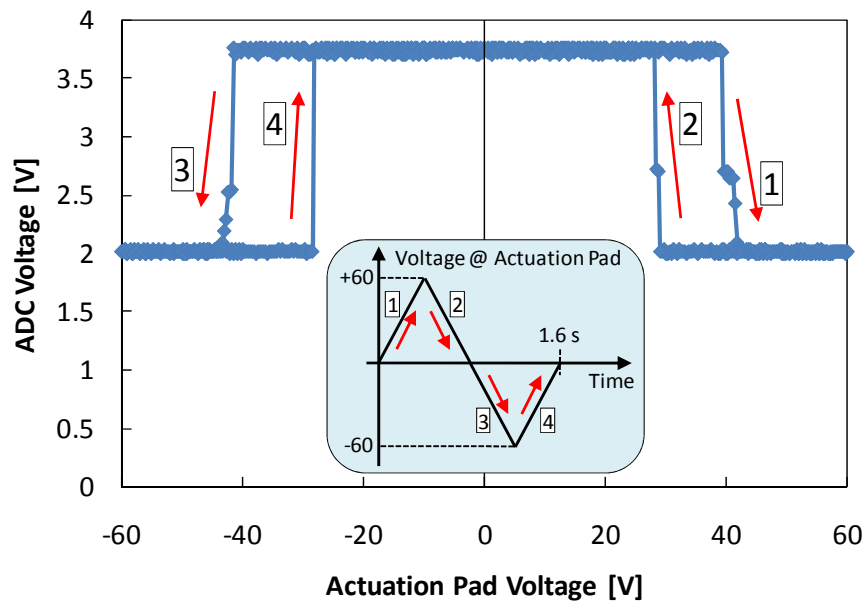


Figure 3.13: Hysteresis graph obtained with the PCB during the “characterization period”.

Chapter 4

RF-MEMS, Experimental Results

4.1 Long Term actuation results

4.1.1 Preliminary results: Clamped-Clamped device and Cantilever Device

The positive actuation and release voltages of two samples (Clamped-Clamped and cantilever), monitored during the stress, are visible in Fig. 4.1 and in Fig. 4.2. The stress times were 20 days for the Clamped-Clamped device and about two days for cantilever one. We use a power law fitting in order to extrapolate the stiction time [31]-[36]:

$$V_{REL+} = a \cdot t^b + c \quad (4.1)$$

We can see that the actuation voltage is minimally affected by the long term stresses (see Figures 4.1 and 4.2) while the release voltage is drastically decreased during the long actuation term period. This negatively affects the lifetime of the device and can bring to stiction occurrence. The phenomenon is reach after 51 hours of continuous biasing in cantilever configuration instead in Clamped-Clamped configuration the power law fitting estimates a stiction time of about 98 years.

The results are summarized in Table 4.1, 4.2, 4.3 and 4.4 for the two typologies respectively. The parameter c is related to the initial value of the release voltage (V_{REL+}) and it is not an important parameter to evaluate the robustness of the devices under test while b indicates the goodness to long term stresses because it

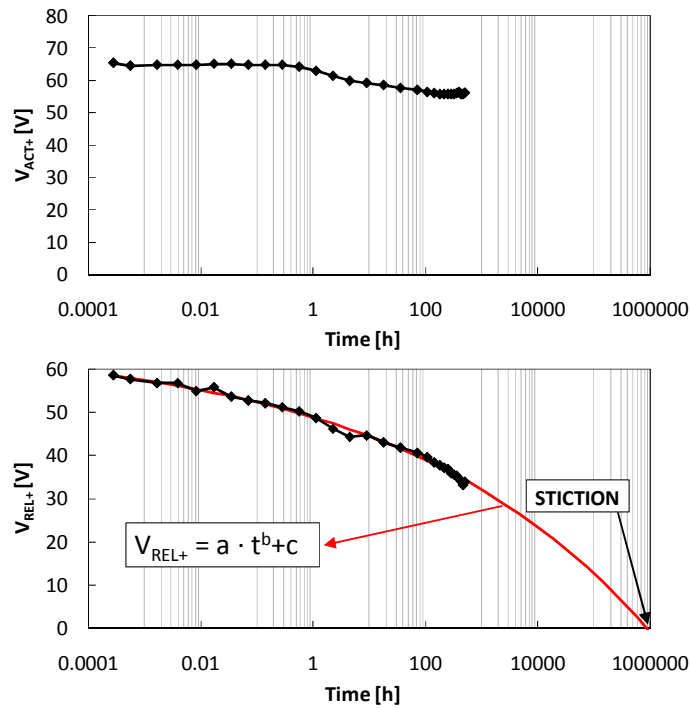


Figure 4.1: Evolution of V_{ACT+} and V_{REL+} about a Clamped-Clamped device.

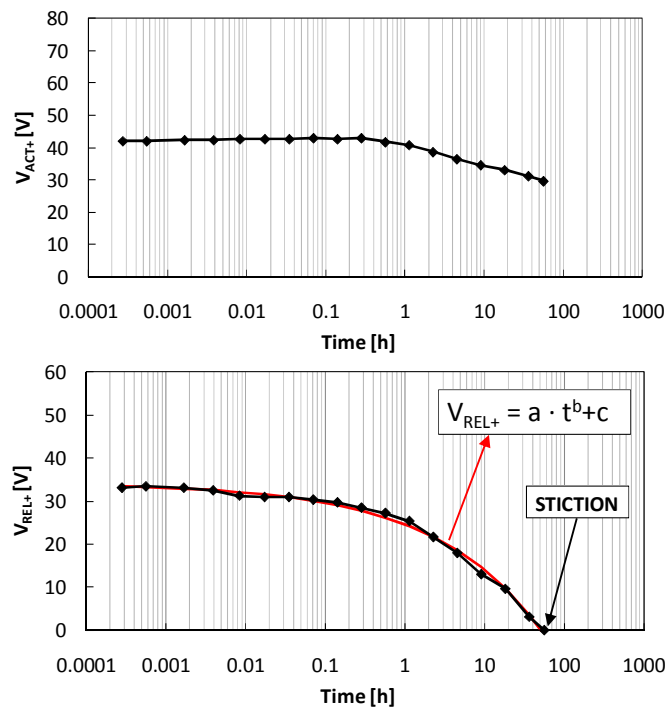


Figure 4.2: Evolution of V_{ACT+} and V_{REL+} about a Cantilever device.

is related to the slope of the curve: lower value of b is associated to a minor trend to shift of the actuation and release voltages. Clamped-Clamped design presents a b parameter that is one order of magnitude lower respect to cantilever design. The fitting goodness is guarantee by the R-square parameter that is close to one in both cases. The Clamped-Clamped configuration presents better results due to its design based on a major restoring force.

Table 4.1: Initial and final Experimental data about a Clamped-Clamped device.

Time [h]	V_{ACT+} [V]	V_{REL+} [V]	V_{ACT-} [V]	V_{REL-} [V]
0.01	65.43	58.60	-62.95	-56.13
509 (21 days)	59.22	35.97	-54.57	-32.26

Table 4.2: Extracted fitting parameters about the Clamped-Clamped configuration.

Fitting Parameters	a	b	c	R-Square	Estimated lifetime
Value	-17.54	0.09735	66.43	0.9944	98.7 years

Table 4.3: Initial and final Experimental data about a Cantilever device.

Time [h]	V_{ACT+} [V]	V_{REL+} [V]	V_{ACT-} [V]	V_{REL-} [V]
0.01	42.06	33.09	-32.47	-27.22
≈ 51	29.69	0	Stiction	Stiction

Table 4.4: Extracted fitting parameters about the Cantilever configuration.

Fitting Parameters	a	b	c	R-Square	Estimated lifetime
Value	-9.499	0.325	34.15	0.9954	51 hours

In order to identify the deviation of release and actuation voltages we carried out an analysis like in [37] where the effect of long term stresses is divides in narrowing and shifting of actuation and releases voltages. This kind of analysis allows us to better understand the entrapment mechanisms and mechanical degradation mechanisms. Let us define the difference between the positive and negative actuation and release voltages at the time step t_i respectively as:

$$\Delta V_{ACT}(t_i) = V_{ACT+}(t_i) - V_{ACT-}(t_i) \quad (4.2)$$

$$\Delta V_{REL}(t_i) = V_{REL+}(t_i) - V_{REL-}(t_i) \quad (4.3)$$

the narrowing of the actuation and release voltage windows can then be defined as:

$$\Delta V_{ACT_NAR}(t_i) = \Delta V_{ACT}(fresh) - \Delta V_{ACT}(t_i) \quad (4.4)$$

$$\Delta V_{REL_NAR}(t_i) = \Delta V_{REL}(fresh) - \Delta V_{REL}(t_i) \quad (4.5)$$

and the shifts of the center of symmetry of $\Delta V_{ACT}(t_i)$ and $\Delta V_{REL}(t_i)$ respectively as:

$$\Delta V_{ACT_SHIFT}(t_i) = \frac{V_{ACT+}(0) + V_{ACT-}(0)}{2} - \frac{V_{ACT+}(t_i) + V_{ACT-}(t_i)}{2} \quad (4.6)$$

$$\Delta V_{REL_SHIFT}(t_i) = \frac{V_{REL+}(0) + V_{REL-}(0)}{2} - \frac{V_{REL+}(t_i) + V_{REL-}(t_i)}{2} \quad (4.7)$$

The results presented in Fig. 4.3 and 4.4 show that narrowing is more relevant respect to shift both in the actuation voltage and release voltage analysis (shifting is around 2 volts maximum instead narrowing is respectively 18 volts maximum about actuation voltage and 55 volts maximum about release voltage).

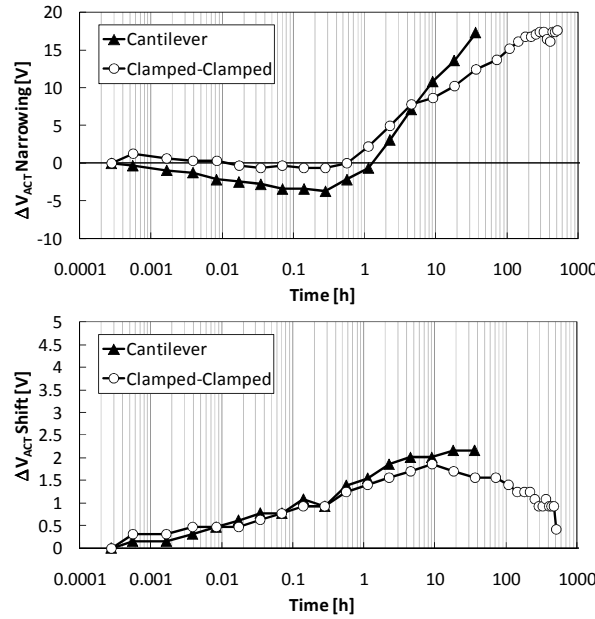


Figure 4.3: ΔV_{ACT} Narrowing and ΔV_{ACT} Shift of the two typologies.

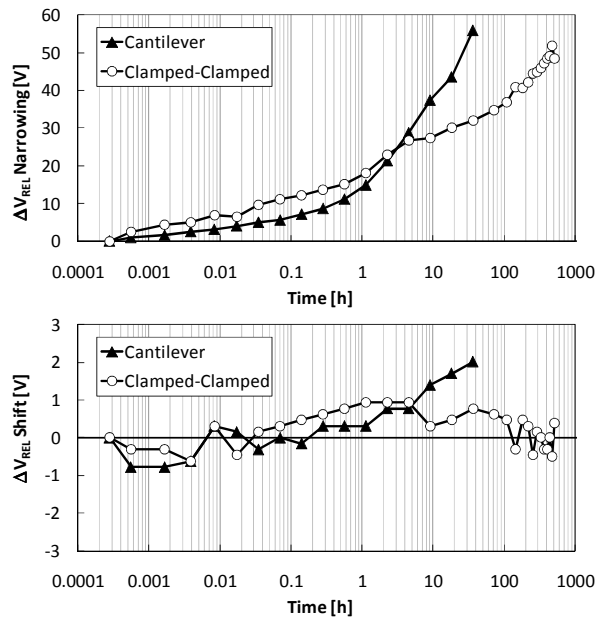


Figure 4.4: ΔV_{REL} Narrowing and ΔV_{REL} Shift of the two typologies.

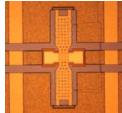
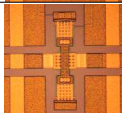
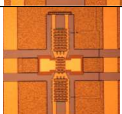
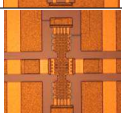

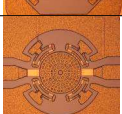
This is in accordance with the dielectric-less design. In fact the use of an oxide layer over the actuator is compatible with shifting [38] instead dielectric-less switches present major narrowing of both actuation and release voltages because the trapped charges are dislocated respect to the actuation structure [34]-[39] and the narrowing can be also related to mechanical phenomena. In this case the narrowing is the predominant effect respect to the shifting one. Results show that to obtain comparable narrowing of actuation and release voltages for both typologies, the stress time is one order of magnitude longer for Clamped-Clamped devices that are better candidates for long actuation periods.

4.1.2 Comparison of different Structures

The designs in table 4.5 have been selected as the most promising for additional reliability investigations.

The objective of the screening was the evaluation of the two device typologies to be used in the long term stress tests. To obtain this goal, samples of different typologies were subjected to 1 hour of continuous biasing, 1 hour of continuous recovery at 0 volts and another 1 hour of continuous biasing. Different stress conditions were selected: in particular two temperatures (25 and 55 °C) and two different actuation signals (Unipolar and Bipolar at 100 hertz and 50 percent

Table 4.5: Selected switch designs suitable for further characterization and long-term testing.

Device label	n. devices per wafer	Notes	Picture
B_pi	44	Capacitive	
S_pi	43	Ohmic	
B_opt	41	Capacitive	
S_opt	42	Ohmic	
O_pi	40	Ohmic	
Ω _opt	41	Ohmic	

duty cycle). So a total of 4 devices for each typology are stressed. The outcome is the selection of the two RF MEMS typologies to be packaged for the long term stresses.

The analysis was done by dividing the effects in narrowing and shifting like in the previous paragraph. The shifting considers a movement of the positive and negative release and actuation voltages in one direction while the narrowing considers a movement of the parameters one towards the other. The shifting and narrowing can be related to different failure mechanisms of the switches: in fact a change in the spring constant of the membrane k or a non-homogeneous charge trapping are expected to contribute to the narrowing while the mean of the charge trapping produces the shifting since it is related to the polarity of the trapped charge [34]-[40].

Fig. 4.5 shows the results obtained on a S_pi device. The different colors indicate the different temperatures and the different actuation biasing signals. We can see that narrowing is more relevant respect to shifting (in fact the maximum narrowing is about 12 volts while the maximum shifting is about 1 volt). Shifting is equal to zero for bipolar actuation signal and maximum 1.2 V for

unipolar stress. This means that charge trapping phenomenon is reduced respect to mechanical elastic and inelastic degradation mechanisms since charge trapping can be mainly related to shifting while mechanical effects can be related to the narrowing. The temperature produces a more pronounced reduction of the actuation voltage and of the narrowing; this can be explained with the fact that the mechanical contribution is widely influenced by the temperature. The green curve in the shifting presents an inversion in the final part of the stress period. This will be analyzed at the end of this paragraph.

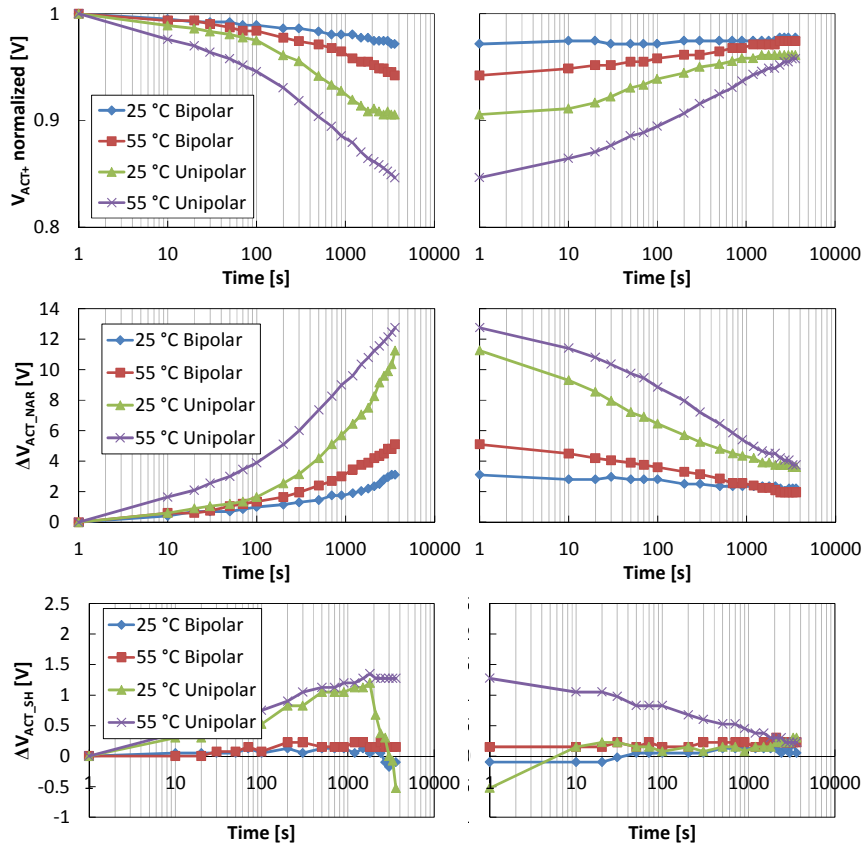


Figure 4.5: Evolution of the positive actuation voltage, narrowing and shifting during the stress procedure (1 hour stress, 1 hour recovery and 1 hour stress) at different temperatures of 4 different S_pi devices.

Results on S_pi devices:

- The unipolar stress produces a more pronounced reduction of the V_{ACT+} (green and violet curves). The effect is more pronounced at 55 °C: this confirms that the mechanical contribution is influenced by the temperature.
- The unipolar stress produces a more pronounced narrowing of the V_{ACT} (green and violet curves).
- The unipolar stress produces a shifting of the V_{ACT} of 1 V while the bipolar stress produces a shifting of 0 V. At 25 °C the unipolar stress presents a shifting that changes from 1 V to -0.6 V.
- The recovery is similar at 25 °C and 55 °C. The saturation recovery value at 25 °C and 55 °C is almost the same.

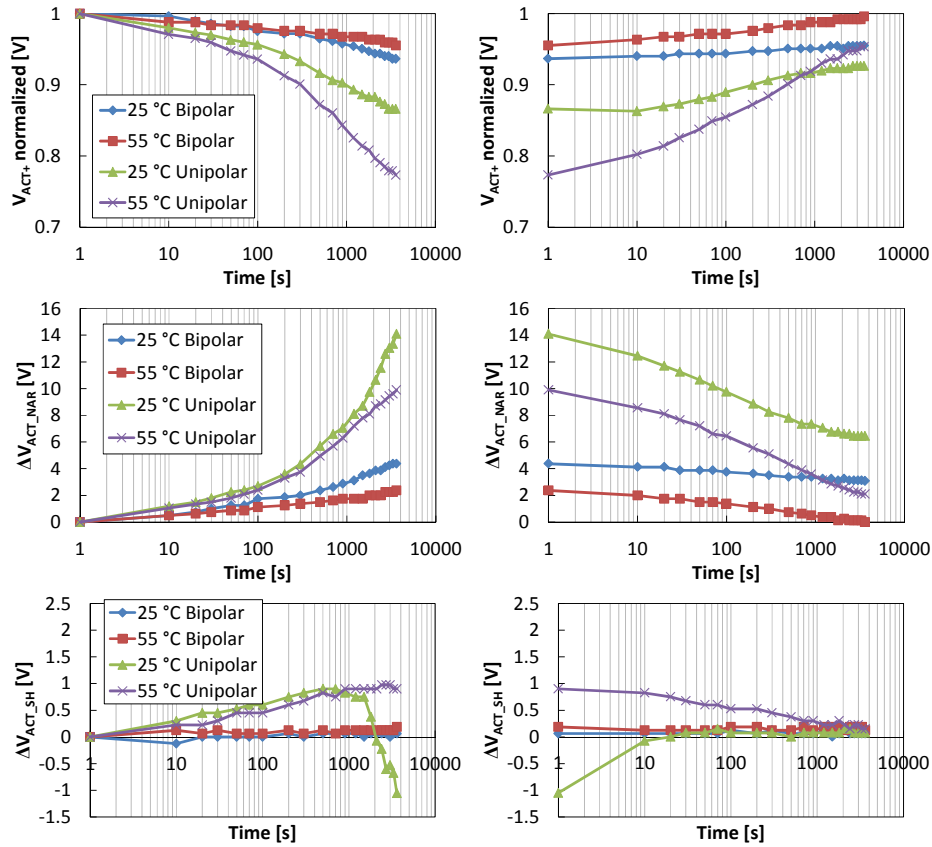


Figure 4.6: Evolution of the positive actuation voltage, narrowing and shifting during the stress procedure (1 hour stress, 1 hour recovery and 1 hour stress) at different temperatures of 4 different B_pi devices.

Fig. 4.6 presents the results obtained on a B_pi device.

Results on B_pi devices:

- The unipolar stress produces a more pronounced reduction of the V_{ACT+} (green and violet curves). The effect is more pronounced at 55 °C: this confirms that the mechanical contribution is influenced by the temperature.
- The unipolar stress produces a more pronounced narrowing of the V_{ACT} (green and violet curves).
- The unipolar stress produces a shifting of the V_{ACT} of 1 V while the bipolar stress produces a shifting of 0 V. At 25 °C the unipolar stress presents a shifting that changes from 1 V to -1 V.
- The recovery is facilitated at 55 °C: this confirms that the mechanical contribution is influenced by the temperature.

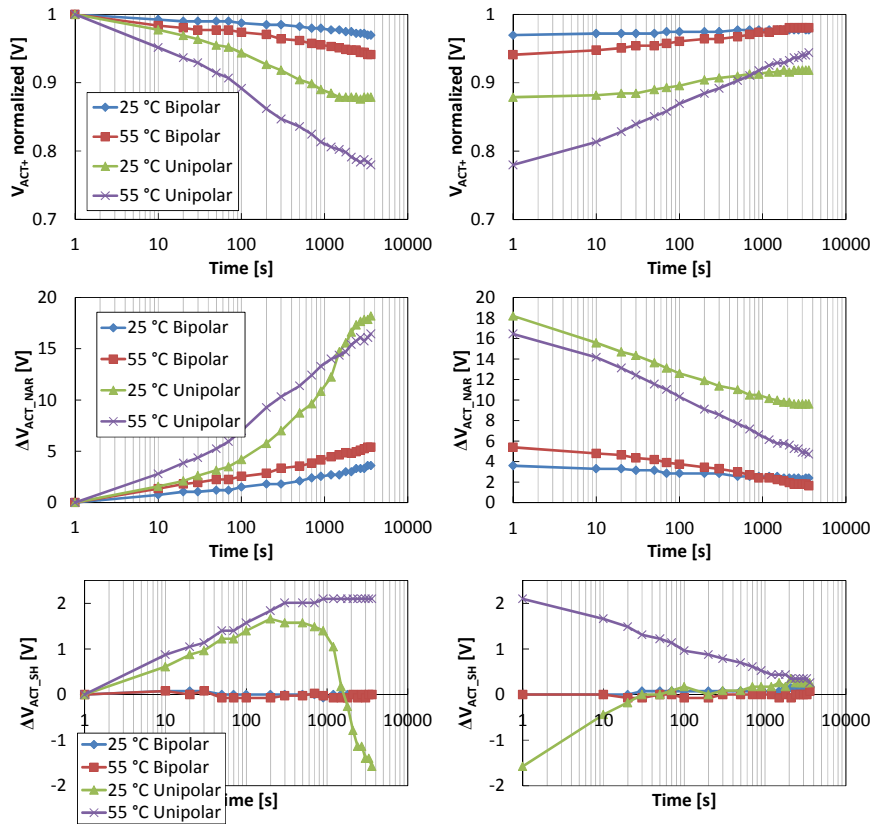


Figure 4.7: Evolution of the positive actuation voltage, narrowing and shifting during the stress procedure (1 hour stress, 1 hour recovery and 1 hour stress) at different temperatures of 4 different S_opt devices.

Fig. 4.7 presents the results obtained on a S_opt device.

Results on S_opt devices:

- The unipolar stress produces a more pronounced reduction of the V_{ACT+} (green and violet curves). The effect is more pronounced at 55 °C: this confirms that the mechanical contribution is influenced by the temperature.
- The unipolar stress produces a more pronounced narrowing of the V_{ACT} (green and violet curves).
- The unipolar stress produces a shifting of the V_{ACT} of 1.5/2 V while the bipolar stress produces a shifting of 0 V. At 25 °C the unipolar stress presents a shifting that changes from 1.5 V to -1.5 V.
- The recovery is facilitated at 55 °C: this confirms that the mechanical contribution is influenced by the temperature.

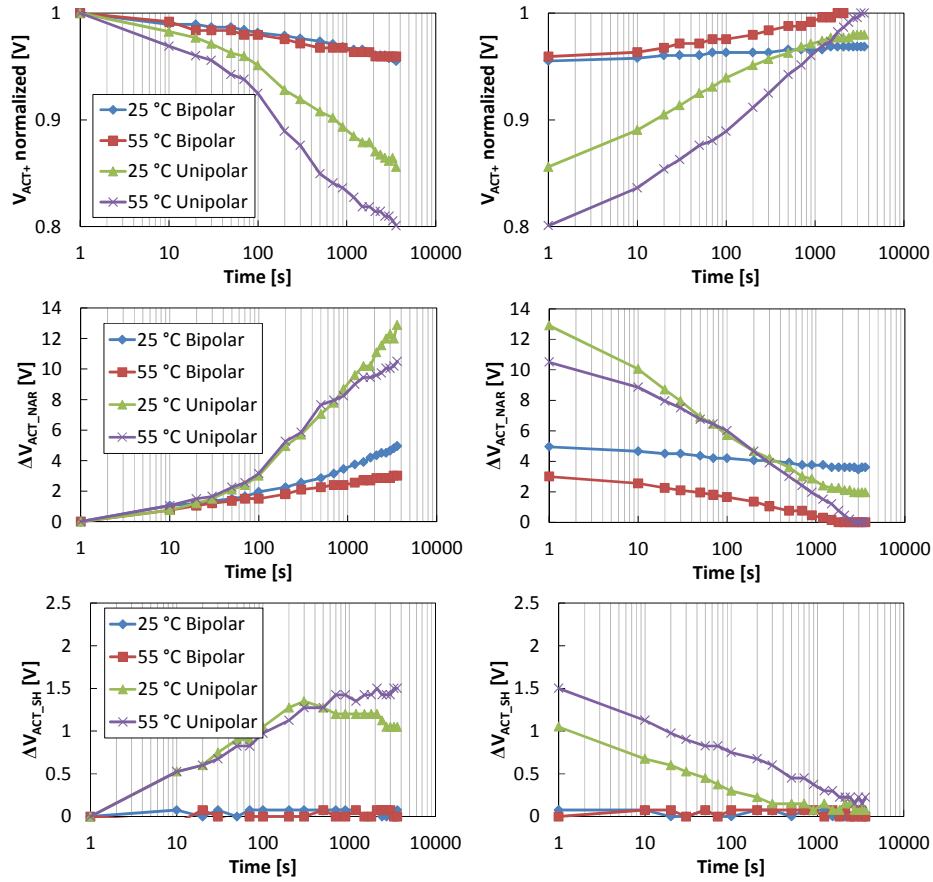


Figure 4.8: Evolution of the positive actuation voltage, narrowing and shifting during the stress procedure (1 hour stress, 1 hour recovery and 1 hour stress) at different temperatures of 4 different B_{opt} devices.

Fig. 4.8 presents the results obtained on a B_{opt} device.

Results on B_{opt} devices:

- The unipolar stress produces a more pronounced reduction of the V_{ACT+} (green and violet curves). The effect is more pronounced at 55 °C: this confirms that the mechanical contribution is influenced by the temperature.
- The unipolar stress produces a more pronounced narrowing of the V_{ACT} (green and violet curves).
- The unipolar stress produces a shifting of the V_{ACT} of 1/1.5 V while the bipolar stress produces a shifting of 0 V.
- The recovery is facilitated at 55 °C: this confirms that the mechanical contribution is influenced by the temperature.

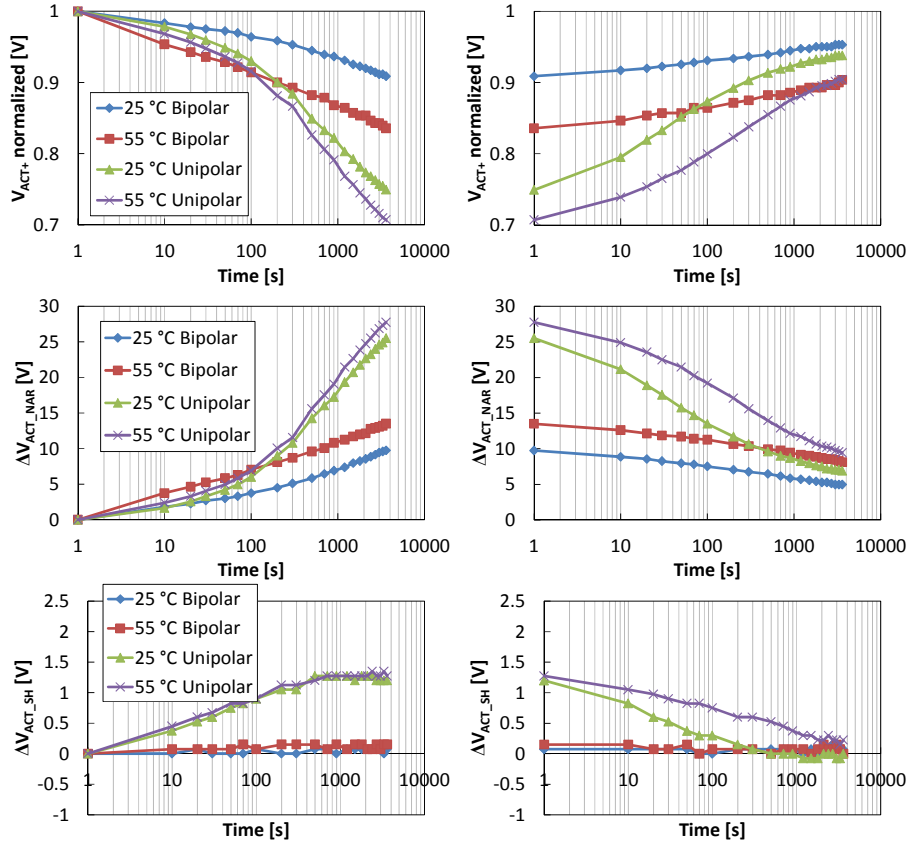


Figure 4.9: Evolution of the positive actuation voltage, narrowing and shifting during the stress procedure (1 hour stress, 1 hour recovery and 1 hour stress) at different temperatures of 4 different Ω_{opt} devices.

Fig. 4.9 presents the results obtained on a Ω_{opt} device.

Results on Ω_{opt} devices:

- The unipolar stress produces a more pronounced reduction of the V_{ACT+} (green and violet curves). The effect is more pronounced at 55 °C: this confirms that the mechanical contribution is influenced by the temperature.
- The unipolar stress produces a more pronounced narrowing of the V_{ACT} (green and violet curves).
- The unipolar stress produces a shifting of the V_{ACT} of 1/1.5 V while the bipolar stress produces a shifting near 0 V.
- The recovery is similar at 25 °C and 55 °C: this confirms that the mechanical contribution is marginally influenced by the temperature in such device.

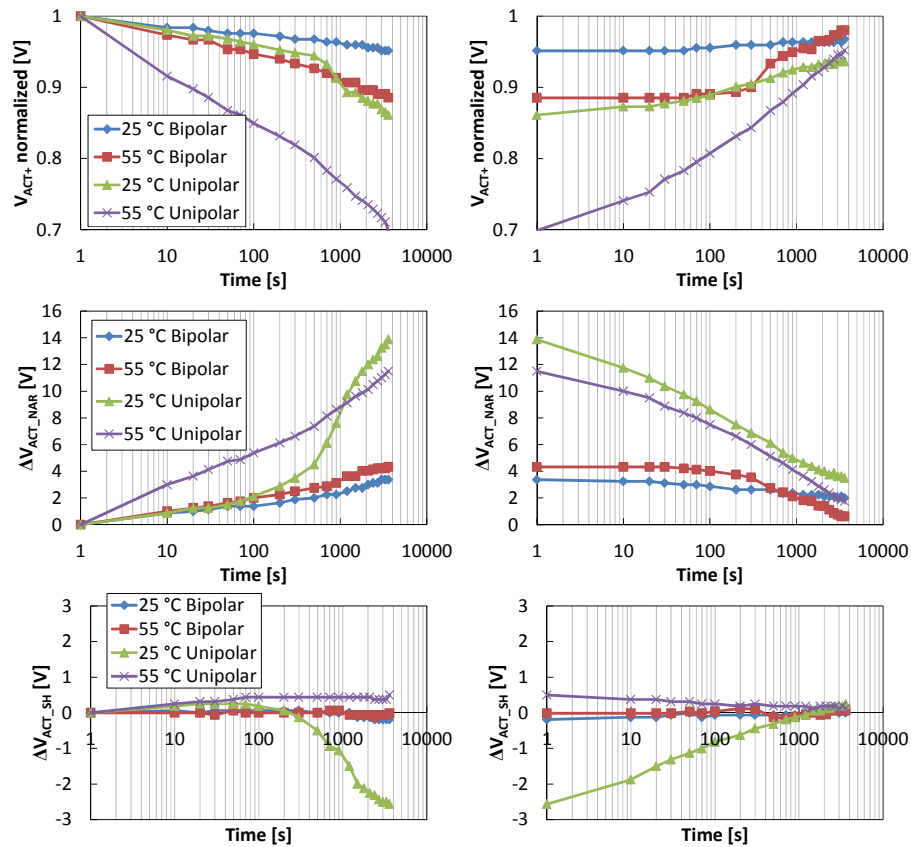


Figure 4.10: Evolution of the positive actuation voltage, narrowing and shifting during the stress procedure (1 hour stress, 1 hour recovery and 1 hour stress) at different temperatures of 4 different Oair devices.

Fig. 4.10 presents the results obtained on a Oair device.

Results on Oair devices:

- The unipolar stress produces a more pronounced reduction of the V_{ACT+} (green and violet curves). The effect is more pronounced at 55 °C: this confirms that the mechanical contribution is influenced by the temperature.
- The unipolar stress produces a more pronounced narrowing of the V_{ACT} (green and violet curves).
- The unipolar stress produces a shifting of the V_{ACT} of 0.5 V while the bipolar stress produces a shifting of 0 V. At 25 °C the unipolar stress presents a shifting that changes from 0.5 V to -2.5 V.
- The recovery is similar at 25 °C and 55 °C: this confirms that the mechanical contribution is marginally influenced by the temperature in such device.

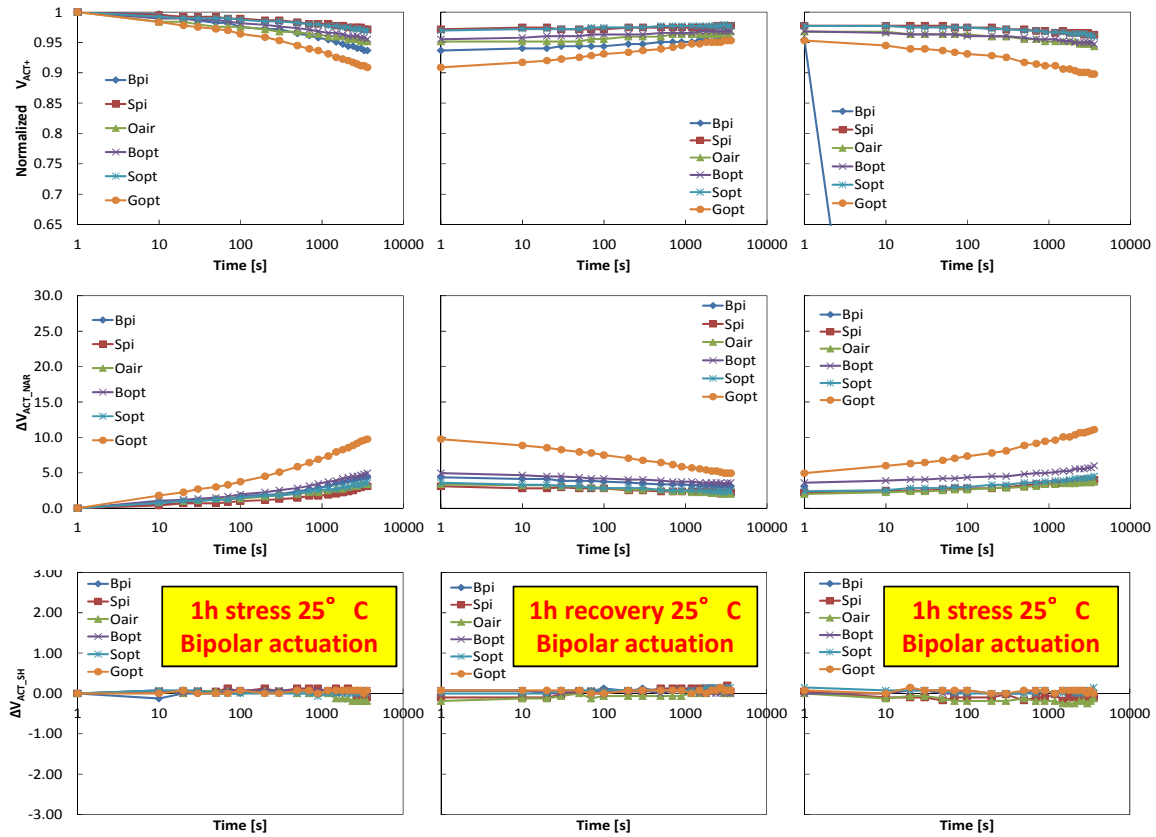


Figure 4.11: Comparison of the six different typologies with bipolar actuation at 25 °C.

Fig. 4.11 presents the comparison of the different typologies at 25 with bipolar actuation signal.

We can see that the normalized actuation voltage decreases during the stress and recovers during the 1 hour of recovery at 0 volts for all devices. At the same time the narrowing increases during the stress period and recovers during the 1 hour at 0 volts for all devices. It is interesting to note that the shifting remains zero with the bipolar actuation signal. This means that the charge trapping is reduced by the use of a bipolar actuation signal. Regarding the comparison of the different typologies we can see that the Ω _Opt typology presents the worst behavior in term of narrowing (see the orange curve, Gopt stands for Ω _Opt).

Fig. 4.12 presents the comparison of the different typologies at 25 with unipolar actuation signal.

A major increase in the narrowing was observed (red arrows): this is probably due to not uniform charge trapping inside the device. The shifting is now different from zero (black arrows): this is due to the mean of the charge trapped

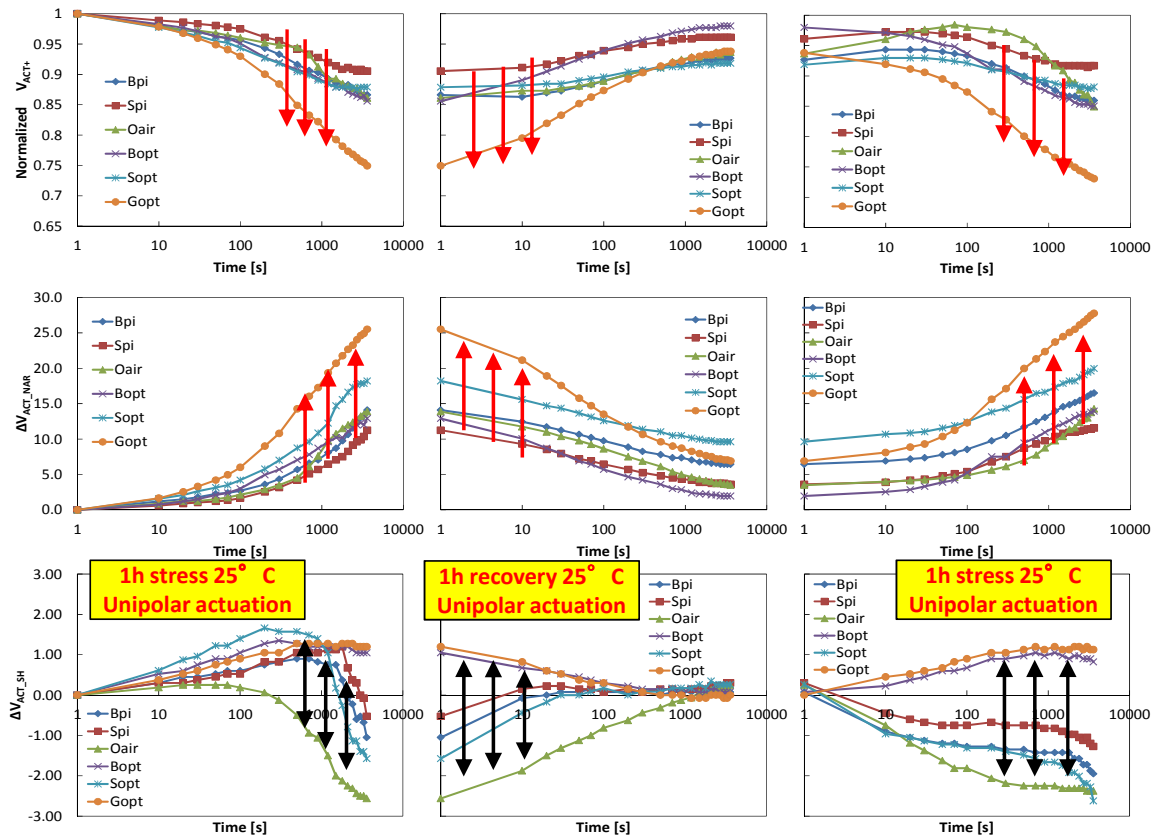


Figure 4.12: Comparison of the six different typologies with unipolar actuation at 25 °C.

that is different from zero. It can be noticed that the shifting is maximum 2 volts whereas the narrowing is maximum 25 volts. The conclusion is that the mechanical degradation is the dominant effect respect to electrical failure mechanism in long term stresses.

Fig. 4.13 presents the comparison of the different typologies at 55 with unipolar actuation signal.

At 55 °C there are major recovery capabilities (highlighted by the blue arrows): in fact during the recovery phase the curves go down more quickly respect to 25 °C. Another aspect to be highlighted is that the shifting now is only positive respect to the stresses with unipolar biasing at 25 °C where the shifting changes sign during the 1 hour stress (this effect is described at the end of this paragraph). At 55 °C the typology Oair and Ω _Opt are worse than the others typologies.

Fig. 4.14 presents the comparison of the different typologies at 55 with bipolar actuation signal.

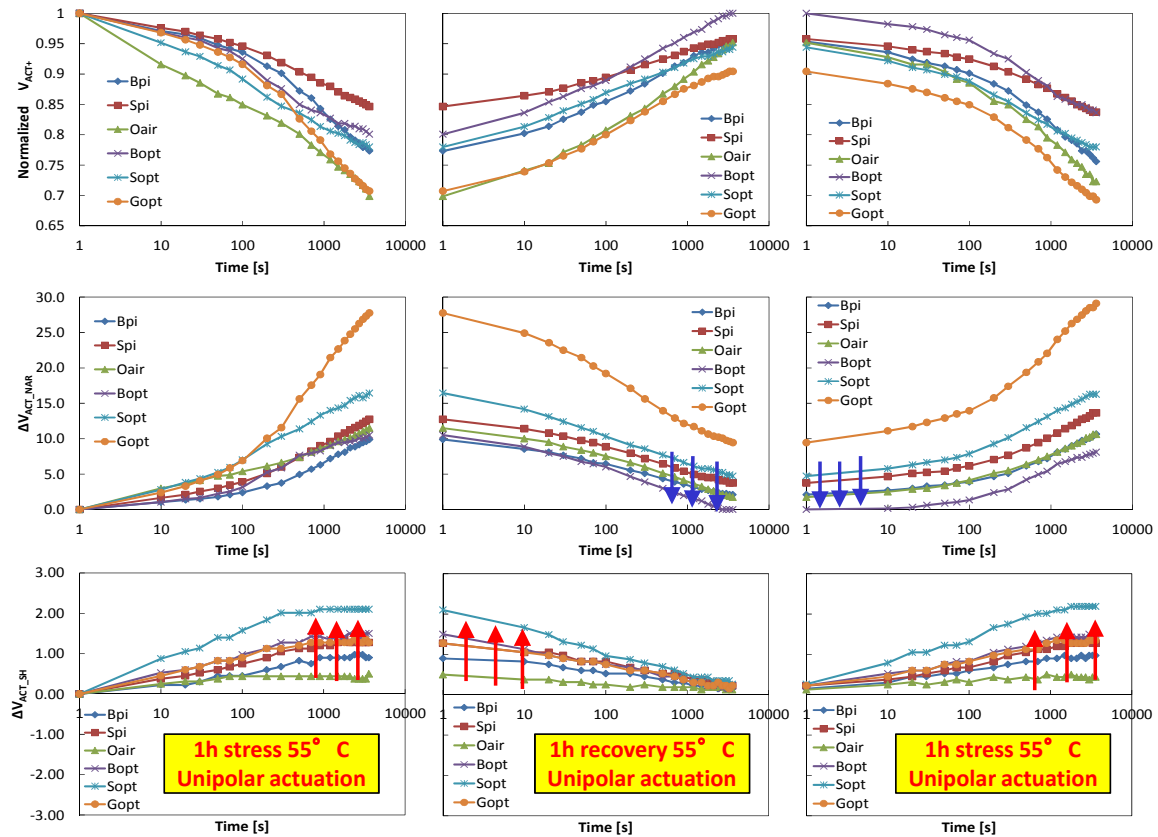


Figure 4.13: Comparison of the six different typologies with unipolar actuation at 55 °C.

We can see a minor normalized actuation voltage decrease, a minor increase in the narrowing (red arrows) and zero shifting during the stress and recovery phases since the actuation is bipolar: this means that the charge trapping is reduced. Another time Oair and Ω _Opt present the worst behavior.

Fig. 4.15 presents the shifting comparison of the unipolar stresses executed at 25 °C and 55 °C.

At 25 °C 4 typologies present an inversion of the shifting after 1000 seconds. The effect is probably due to the different charge trapping mechanisms that present different time constants and different activation temperature. The effect can also be due to the different trapping location or redistribution of the charge during the stress period. In fact during the long actuation period positive or negative charges can be injected into the oxide with a positive or negative net trapped charge (Fig. 4.16).

In general a positive shift results in a decrease of the actuation voltage: this means that a positive net charge is trapped into the device. On the contrary

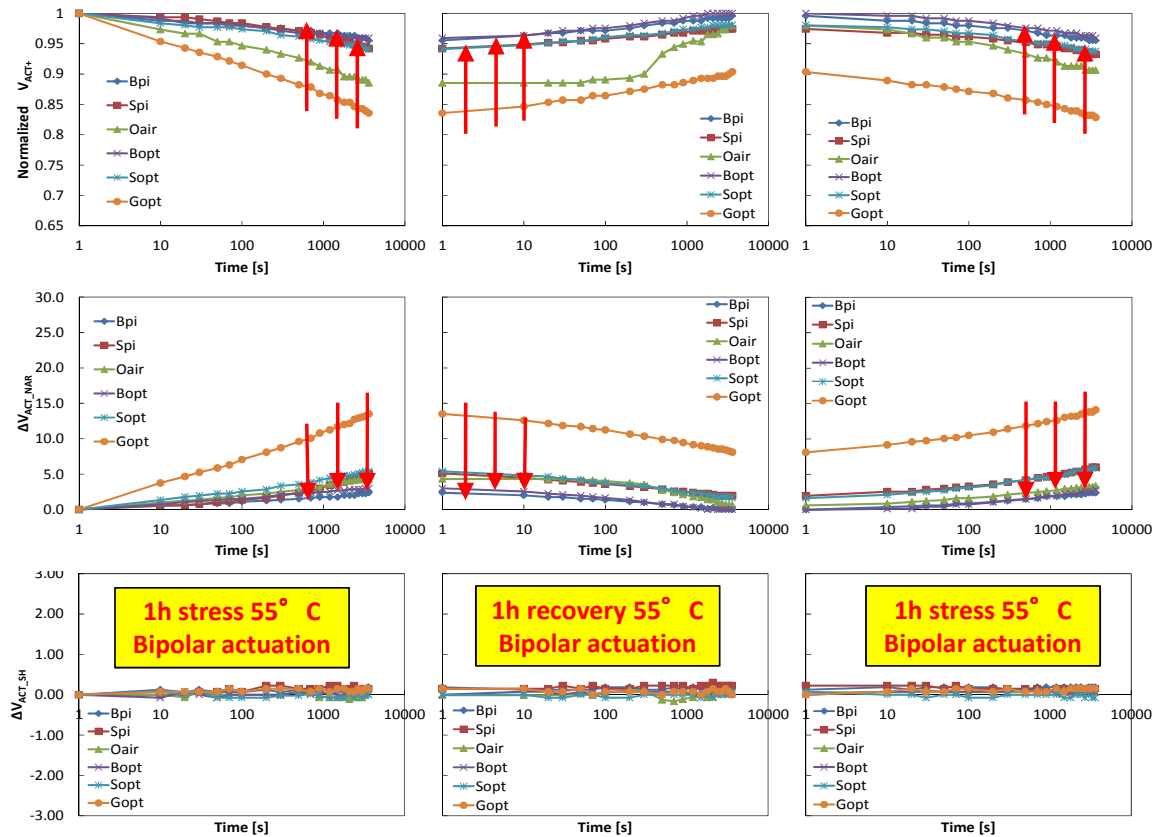


Figure 4.14: Comparison of the six different typologies with bipolar actuation at 55 °C.

a negative shift results in an increase of the actuation voltage: this means that a negative net charge is trapped into the device. So at different temperatures it is probable that different charges can be trapped into the device producing the results of Fig. 4.15. At 25 degrees in the first part positive charge trapping dominates, for long time negative charge trapping prevails and this produces the inversion of the curves. This is not visible at 55 degrees where only positive charge trapping are visible (at least up to 1 hour, we can say nothing for longer times). This is one possibility because another cause can be the different trapping location and so the redistribution of the trapped charge into the device during the stress period. This effect can be studied monitoring the current during the stress and recovery phases in order to see any deviation of the actuation pad current. This issue is currently under investigation.

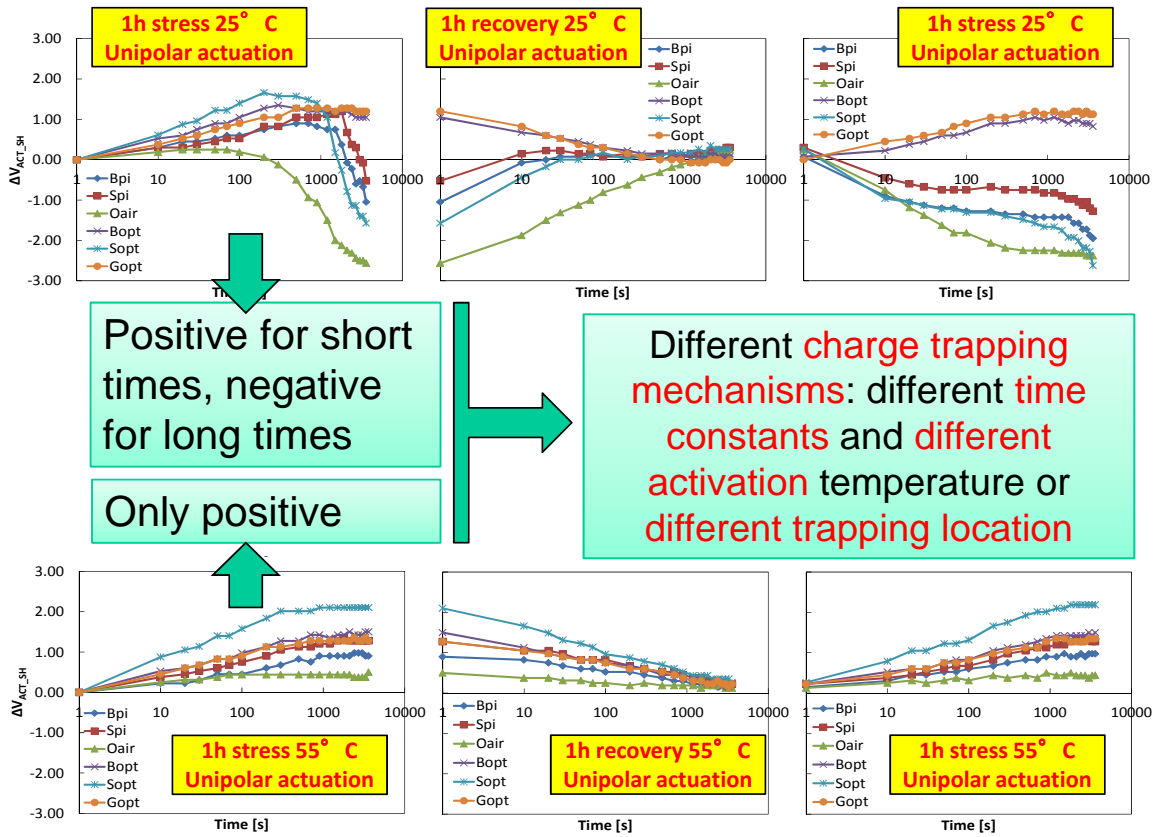


Figure 4.15: Comparison of the shifting for the six different typologies at 25 °C and at 55 °C.

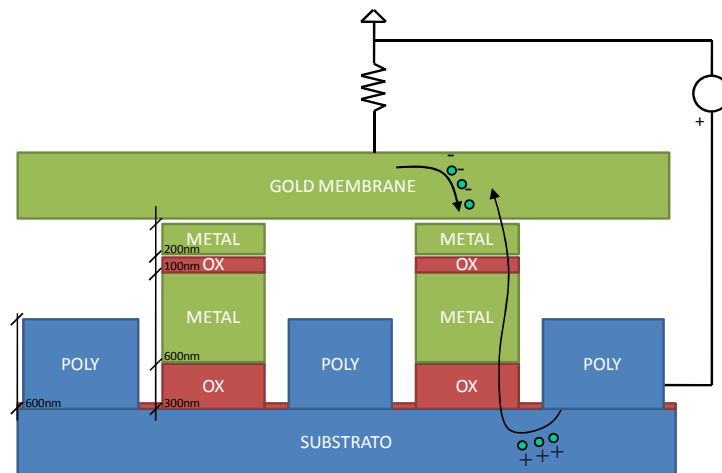


Figure 4.16: Scheme of the charge injection during the long term stress: positive or negative charge can be injected into the device.

4.1.3 Transient Evolution of Mechanical and Electrical Effects

The devices studied in this paragraph are cantilever ohmic switches (Fig. 4.17).

The actuation electrodes are in lightly doped polysilicon, whereas the mobile membrane and the coplanar waveguide are made of electrodeposited gold. This design is aimed at reducing charge trapping effects. The charge reduction is obtained removing the dielectric above the polysilicon electrode and including a few stoppers in the electrode area to prevent the contact between actuation electrode and mobile membrane.

The superposition of mechanical and charge trapping effects can lead to difficult interpretations of the actuation and release voltages shift during reliability tests. Fig. 4.18 presents this concepts in the classical hysteresis characterization plot of the transmission parameter versus the applied voltage to the actuation pad of an RF MEMS switch.

For this reason, narrowing and shifting of the hysteresis characterization curves during long actuation tests has been analyzed as reported in [41].

A change in the spring constant of the membrane k or more in general all mechanical modifications, together with non homogeneous charge trapping are expected to contribute to the narrowing parameters $\Delta V_{ACT,REL,NAR}$, of the switch. On the contrary the mean of the charge trapping, being polarity dependent, pro-

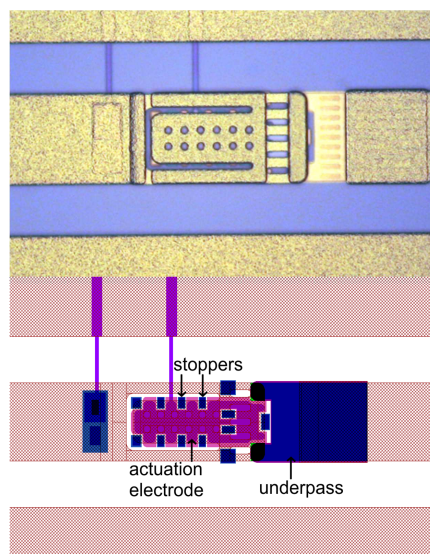


Figure 4.17: Manufactured devices (top) and device layout (bottom).

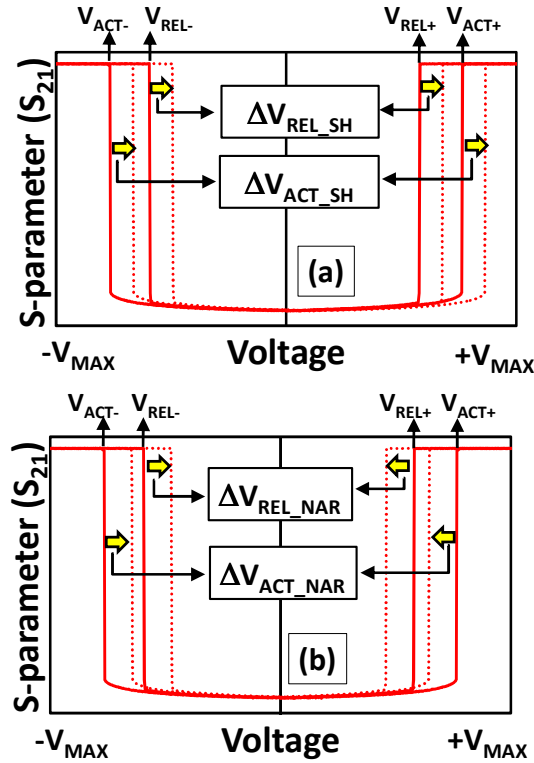


Figure 4.18: Shifting (a) and narrowing (b) of the classical hysteresis characterization curve of an RF MEMS switch.

duces the shifting $\Delta V_{ACT,REL,SH}$. We compare two types of long term stresses (Fig. 4.19): (i) with unipolar DC biasing (70 V) and (ii) bipolar biasing ($\pm 70V$, frequency = 100 Hz, duty cycle 50%) in order to highlight the mechanical effects respect to charge trapping. In bipolar biasing stress tests the biasing voltage is inverted quickly from + 70 V to - 70 V in order to prevent any deactuation of the device. The stress procedure is divided in 4 hours of continuous biasing and 20 hours of continuous recovery at 0 V. The entire biasing period is interrupted periodically to characterize the device. The whole characterization is 2-s long. The stress test is consecutively repeated for six times (three bipolar and three unipolar, in this order) in order to assess the stability of the degradation and to distinguish between transient and permanent effects.

In Fig. 4.20 we present the results of the continuous biasing procedure. During the first bipolar stress (curve # 1) a reduction of the V_{ACT+} , an increase of the $\Delta V_{ACT,NAR}$ are visible. $\Delta V_{ACT,SH}$ is equal to zero within the experimental error. This last observation implies that, for bipolar stresses, $2\Delta V_{ACT+} = \Delta V_{ACT,NAR}$, and therefore the time evolution of the two parameters is equivalent. During

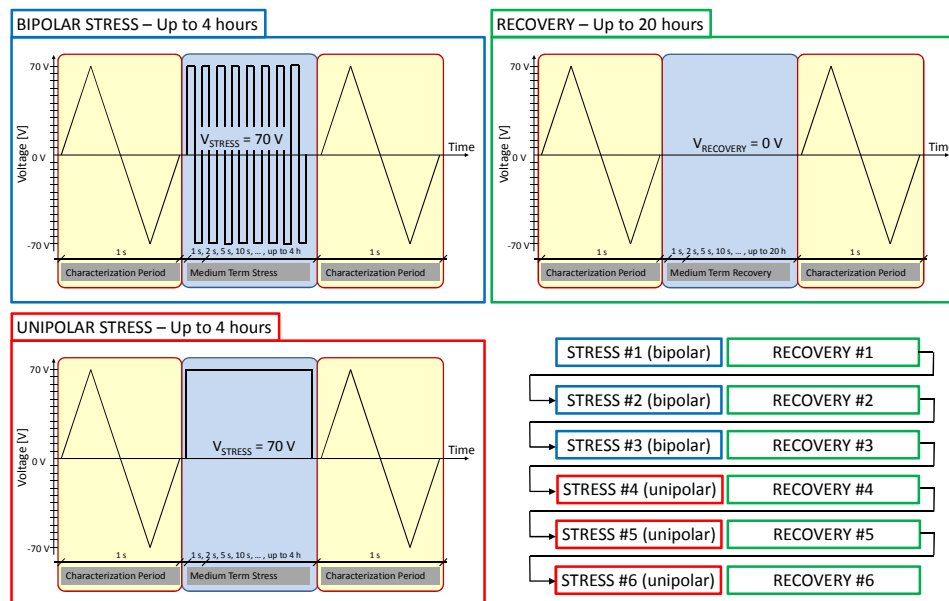


Figure 4.19: Scheme of the stress procedure: the stress test is consecutively repeated for six times (three bipolar and three unipolar, in this order).

the subsequent recovery phase the V_{ACT+} and ΔV_{ACT_NAR} partially recover. The second and third stresses and recovery phases (curves # 2 and # 3) are almost overlapping, indicating that a saturation is reached. These results (curves # 1, # 2 and # 3) can be explained with two different mechanisms: (i) the not recoverable part (see white arrows in Fig. 4.20a and 4.20c) is attributable to the mechanical permanent creep, while (ii) the recoverable part is ascribed to the viscoelastic recoverable mechanism. Due to the bipolar nature of the stress procedure no charge trapping is observed as confirmed by the absence of any ΔV_{ACT_SH} (see Fig. 4.20e, f).

The three unipolar stresses (curves # 4, # 5 and # 6), with respect to the bipolar technique, show an additional recoverable V_{ACT+} decrease and ΔV_{ACT_NAR} increase (see gray arrows in Fig. 4.20a, b, c, and d). At the same time, a significant ΔV_{ACT_SH} is observed (see black arrows in Fig. 4.20e and 4.20f) confirming the relevant effects of the charge trapping on both ΔV_{ACT_NAR} and ΔV_{ACT_SH} .

It can be noticed that the shifting (ΔV_{ACT_SH}) is significantly less than the narrowing (ΔV_{ACT_NAR}) even in unipolar stresses. Moreover, it is clear that the recoverable mechanical deformation has a different time evolution with respect to charge trapping. While the former keeps increasing with time, the latter seems to reach saturation. In fact, some sort of saturation is expected for charge trapping.

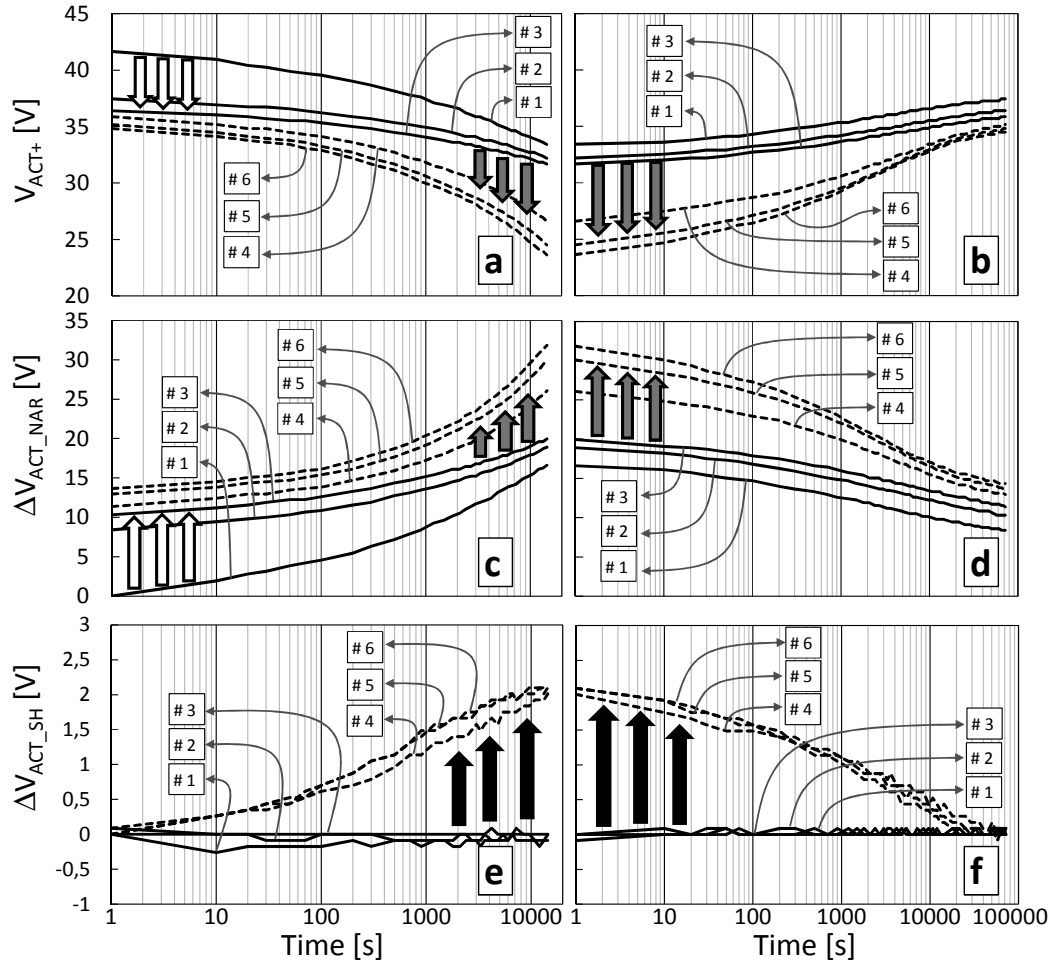


Figure 4.20: Evolution of the actuation voltage (a and b), narrowing of the actuation voltages (c and d) and shifting of the actuation voltages (e and f) during 3 consecutive long term stresses with bipolar biasing (solid lines on left graphs) and recovery phases (solid lines on right graphs) followed by 3 consecutive long term stresses with unipolar biasing (dashed lines on left graphs) and recovery phases (dashed lines on right graphs).

Charging in dielectrics is commonly modeled with a multiple exponential or a stretched exponential function [42]. Fig. 4.21 shows a stretched exponential fitting of ΔV_{ACT_SH} during the unipolar stress # 6 that is related to the charge trapping mechanism. The fitting law [43], [44] and the extracted fitting parameters are summarized in Table 4.6. From the fitting data the saturation value of $\Delta V_{ACT_SH} = 2.131$ V can be extracted and this value is very close to the last experimental point measured. This means that saturation of charge trapping is almost reached

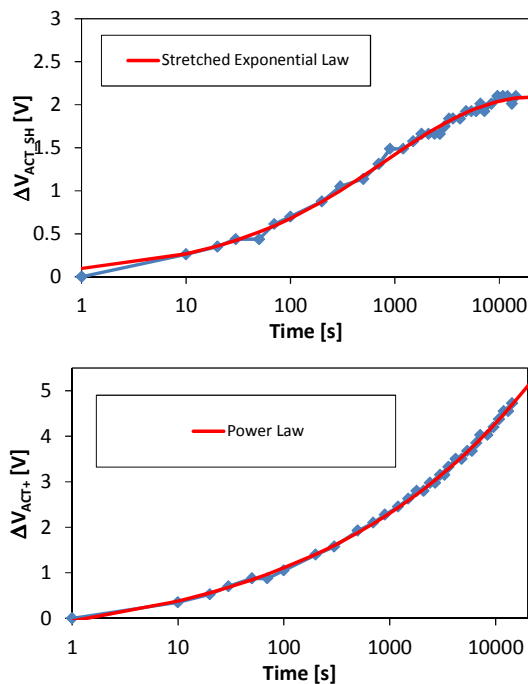


Figure 4.21: Fitting of $\Delta V_{ACT_{SH}}$ during unipolar stress # 6 (top) and ΔV_{ACT+} during bipolar stress # 3 (bottom).

after 4 hours, and therefore, at least for dielectric-less switches, it is very unlikely that charge trapping will ever be the main source of failure.

Table 4.6: Fitting Laws and Extracted Parameters

$$\Delta V_{ACT+} = b_1 \cdot t^{m_1} + c_1$$

$$\Delta V_{ACT_{SH}} = a_2 \cdot (1 - e^{-(t/\tau_2)^{n_2}})$$

Law	b_1	m_1	c_1	R^2
ΔV_{ACT+} power	0.6822	0.217	-0.748	0.99
	a_2	τ_2	n_2	
$\Delta V_{ACT_{SH}}$ stretched exponential	2.131	813.1	0.457	0.99

More complicated is the situation of the $\Delta V_{ACT_{NAR}}$, which is equivalent to ΔV_{ACT+} in bipolar stresses. This parameter identifies the mechanical component of actuation voltage variation. We know from a previous study [41] that narrowing continues to increase also after 20 days of continuous biasing. This is a signature of a different degradation mechanism with respect to charge trapping. A power law is a suitable fitting function for this curve. The fitting parameters obtained in this case are also reported in Table 4.6. It is evident that this degradation

mechanism will lead to switch failure if the biasing time is long enough, and the details of the calculation of the switch lifetime depend upon the failure criterion chosen. It is then clear that, for long-term actuation predictions in dielectric-less devices, the mechanical factor is more important than charge trapping, while in the short term both phenomena need to be taken into account.

4.1.4 Evaluation of a preconditioning procedure

At the light of the previous paragraph results, it is evident that a preconditioning procedure is needed in order to predict the lifetime of the devices. In fact we need to eliminate any permanent degradation before studying the transient degradation mechanism responsible of the failure. Regarding the preconditioning the objective is the identification of a standard procedure to be used before any use of the devices. The procedure is used to condition all the devices to the same starting point. The aim of this preconditioning is to remove all the devices with premature failures and to eliminate not reversible phenomena in the working devices (such as plastic deformation or mechanical not reversible phenomena). To obtain this objective we subjected 4 devices of the same typology (B_opt and S_opt) to four different long term stresses. The long term stress is divided in 6 phases of 1 hour stress and 1 hour recovery repeated in sequence. The first three phases are performed at 25 °C for the first device, at 40 °C for the second device, at 55 °C for the third device and at 70 °C for the fourth device, the second three phases are performed at 25 °C for all devices. In this way the influence of the temperature can be studied. The outcome of the preconditioning is the selection of the parameters (temperature, timing) for the initial conditioning procedure.

Fig. 4.22 presents the results obtained for the B_opt typology. The first stress at 25 °C presents a constant deviation respect to the following stresses (red arrows). This is due to the creep effect that is normally present in the first long actuation period. This part can't be recover in the subsequent stresses. At higher temperatures the creep effect seems to disappear (this is highlighted by the black circles where the different curves are overlapped). But reducing the temperature the creep effect reappears (visible from the black arrows). This effect is increased if the previous stresses (1 2 and 3) were performed at higher temperatures (this is visible from the length of the black arrows that grow with the temperature of the previous stresses).

Similar results are obtained for the S_opt typology (Fig. 4.23). In fact the first stress at 25 °C presents a constant deviation respect to the following stresses

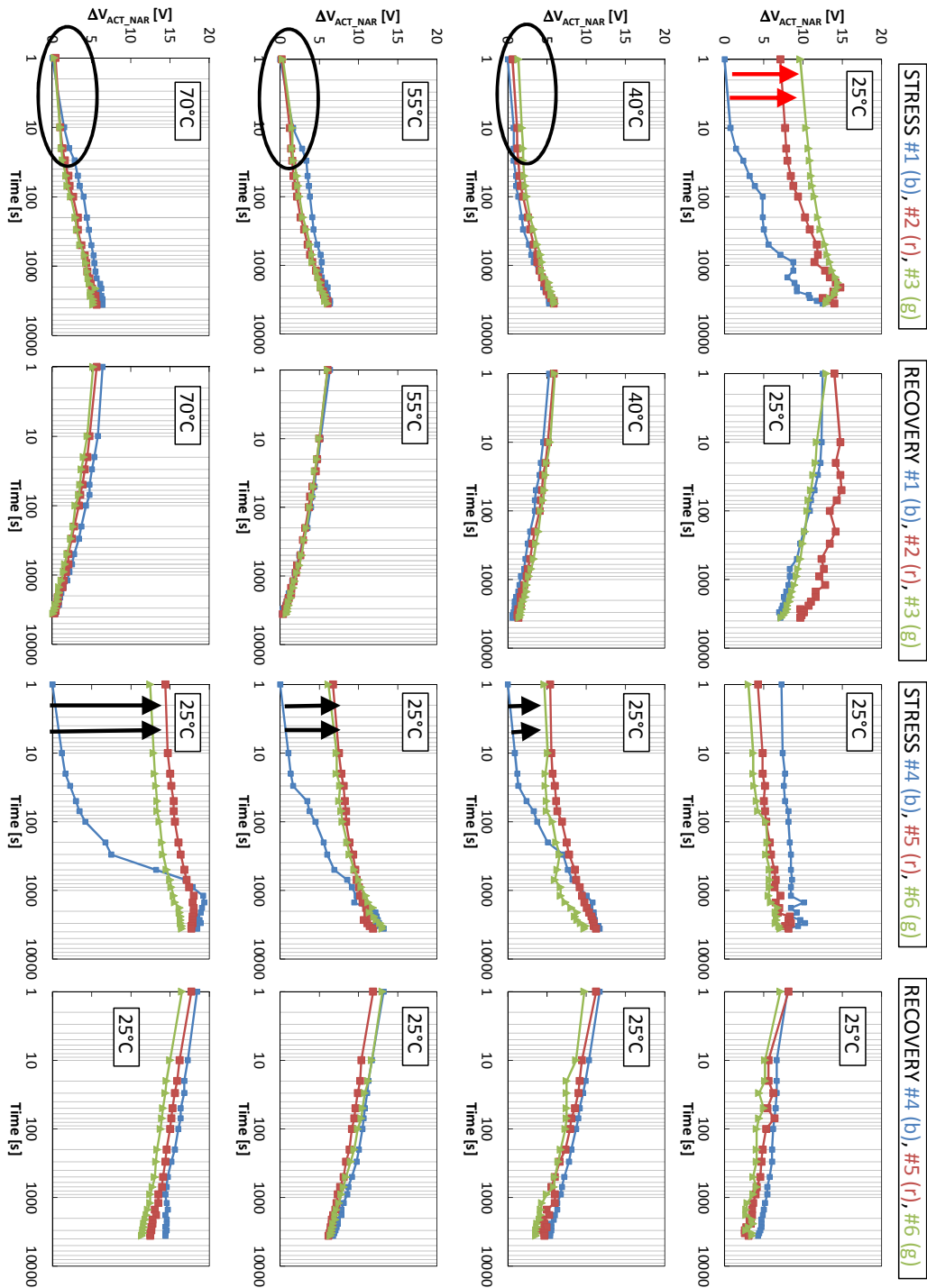


Figure 4.22: Study of the preconditioning for B_opt typology.

(red arrows). At higher temperatures the creep effect seems to disappear (this is highlighted by the black circles). At 70 °C the behavior seems to be different (blue circle). Also in this case reducing the temperature the creep effect reappears

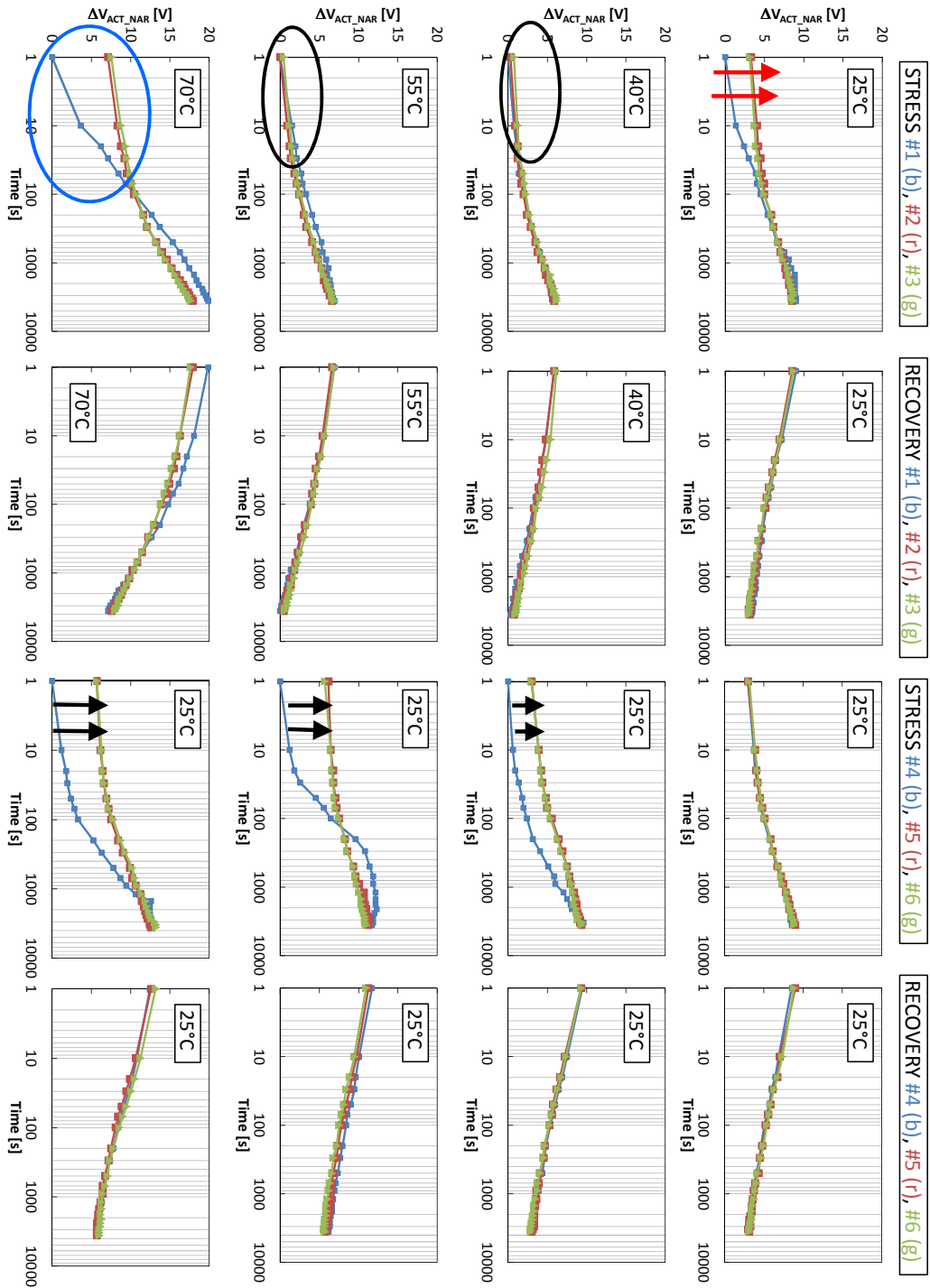


Figure 4.23: Study of the preconditioning for S_opt typology.

and the effect is increased if the previous stresses (1 2 and 3) were performed at higher temperatures (black arrows).

Results:

- The first stress at 25 °C presents a constant deviation (creep effect).
- At higher temperature the creep effect seems to disappear (circles): no deviation of the first three narrowing curves is observed at 40, 55 and 70 °C.
- Reducing the temperature at 25 °C after the higher temperature stresses the creep effect reappears in the stress #4.
- The effect is increased if the previous stresses (1, 2 and 3) were performed at higher temperatures.

At the light of the presented measures a simple procedure was selected for the preconditioning: First a stress of 1000 seconds at 70 °C followed by a recovery of 1000 seconds at 70 °C. Then a stress of 1000 seconds at 25 °C followed by a recovery of 1000 seconds at 25 °C.

The choice of 70 °C is intended to bring the device to the maximum operating temperature and then at 25 °C a second preconditioning is necessary since the creep reappears. The choice of 1000 seconds instead of 3600 seconds (1 hour) is intended to reduce the preconditioning time. In most cases after 1000 seconds stress time the 90% of the effect is reached (idem for the recovery phases).

This procedure has to be applied to each device before any long term stress and lifetime prediction. This permits to eliminate not reversible phenomena and to predict the real lifetime of the device under test.

4.2 Cycling results

The analysis of contact degradation in a not controlled atmosphere (air) at different temperatures in microstructures with electrostatic actuation is the main topic of this section [45]-[46]. Different types of devices are subjected to 1 million impact cycles at three different temperatures (25 °C, 40 °C and 55 °C). The electrical properties are shown and the results are explained: a major operating temperature lead to a more reliable contact because the membrane internal stress decreases with the temperature, lowering the restoring force of the switch. The use of modified floating metal in the fabrication of the devices can improve the reliability of the contact producing a significant improvement in the lifetime.

The contact degradation is a relevant issue in electrostatic actuated devices, where the degradation of the contact may bring to a significant reduction on the

electrical properties (i.e. insertion losses, return losses and isolation) and even to the mechanical failure of the device.

The full and comprehensive characterization of RF-MEMS requires several analysis approaches such as repetitive cyclic impact measurements at different frequencies, analysis at different temperatures, stress tests with different pulse shapes [47]-[48]. Contact degradation and charge trapping phenomena though, combined with the effects induced by these measurement methodologies, might lead to unclear or even counterintuitive results since different aspects combine together in a common outcome (i.e. mechanical and electrical effects).

The aim of this section is to explain the role of temperature on the cycling stress tests applied on different types of RF MEMS switches (i.e. standard contact procedure with pure evaporated gold and modified with a thin platinum layer). We aim to understand better the behavior of devices subjected to multiple impact stresses, which is always the ultimate goal. In particular, the effect of different plate temperature is considered. For each of these aspects we provide experimental results and their interpretation. We would like to emphasize that our primary purpose is not to draw conclusions about the absolute lifetime of the devices since the measures were performed in air but to investigate the effect of temperature on the contact and to better understand the issues related to the surface impact.

4.2.1 Devices description

This particular device was chosen for its specific design. While being a capacitive switch, the abrupt capacitance change which characterizes the switching behavior is provided by the electrical contact between small dimples on the underpass and the mobile membrane, with a contact structure which is more typical of ohmic switches. A picture of the manufactured device is reported in Figure 4.24 (a), while a scheme of the contact region is depicted in figure 4.24 (b).

The devices have been fabricated at FBK by employing a well-established process for RF-MEMS switches. The process flow, together with a detailed process description is deeply discussed in [49], and can be briefly summarized as follows: the switches were manufactured on high resistivity 525- μm thick and 4-inch wide silicon wafers. Actuation electrodes and connecting lines are made in lightly doped polysilicon. In order to reduce charging phenomena, the switch has no dielectric above the electrodes, with stopping pillars which prevent the contact between electrode and mobile membrane [49]. The underpass line is realized

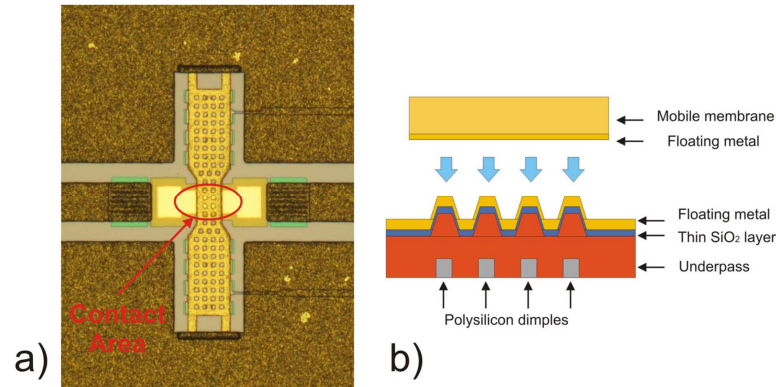


Figure 4.24: (a) Device micrograph, (b) Scheme of the contacting region.

in a sputtered multilayer metal composed by a 500 nm-thick aluminum layer sandwiched between two thin (about 80 nm) bi-layers of titanium and titanium nitride. Polysilicon dimples are included in the contact region of the underpass to improve the electrical contact, compensating typical shape irregularities due to technology. The contact region is covered with 100 nm of low temperature oxide and then with 150 nm of floating potential metal. In the device design presented in this paragraph, the role of the floating metal is to ensure a good electrical contact with the mobile membrane, which is made by a 2 μm thick electrodeposited gold, suspended over an air gap of 2.7 μm . The membrane is 620 μm long and 100 μm and 60 μm wide above the electrodes and the contact area respectively, as can be seen in Figure 4.24. The floating metal layer has been deposited in two different material variants: (i) by using pure evaporated gold and (ii) by means of a modified multilayer [50] composed of a thin (3 nm) platinum layer sandwiched between two thicker layers of gold with thicknesses of 120 nm (bottom) and 30 nm (top) of gold. Moreover, in the modified devices, the bottom part of the mobile membrane in the contacting region was also made with 150 nm of the same material, in order to have contacting surfaces with the same characteristics on both sides. In Figure 4.25 we show the evolution of S_{11} as a function of the bias voltage taken from a typical standard capacitive device, which clearly exhibits low losses and high isolation. The actuation voltage is about 43 V while the release voltage is close to 35 V. The DC bias voltage used in cycling tests has been chosen at 50 V in order to obtain a good actuation of the device. All the extracted parameters at 25 $^{\circ}\text{C}$ are reported in Table 4.7.

It is worth to remark that our primary target in this paragraph is to investigate the effect of temperature and different contact surface materials on the

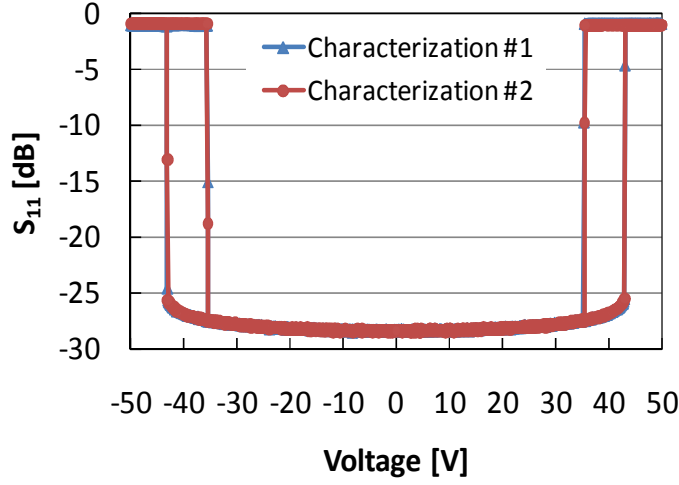


Figure 4.25: S_{11} evolution of a capacitive switch.

Table 4.7: Extracted parameters of the capacitive switch of fig. 4.25

DC Electrical Parameters	Symbol	Value (V)
Pull in positive voltage	V_{ACT+}	43
Pull out positive voltage	V_{REL+}	35
Pull in negative voltage	V_{ACT-}	-43
Pull out negative voltage	V_{REL-}	-35
RF Electrical Parameters	Symbol	Value (V)
S_{11} in off state	$S_{11} @ 0V$	-28.35
S_{11} in on state	$S_{11} @ V_{ACT+}$	-0.94
S_{21} in off state	$S_{21} @ 0V$	-0.23
S_{21} in on state	$S_{21} @ V_{ACT+}$	-15.59

cycling test. We are not interested, at moment, to evaluate the exact lifetime. Hence, for sake of simplicity we do not test the devices in nitrogen controlled atmosphere. All the measurements shown in this paragraph, have been done on wafer level, in air, at controlled temperature. This is the only reason for the relatively short lifetime observed in our tests (as we will show in the following).

After the preliminary characterization a cycling stress is carried out. We used a bipolar pulse with a period of 1 ms and a duty cycle of 0.2 accordingly with our previous work [51]. The total number of pulses is 10^6 . The RF Power forced during the cycling procedure was 0 dBm during the entire stress procedure. The characterization procedure and the experimental set up are described in the section dedicated to the description of the measurements set ups.

4.2.2 Experimental Results

Three capacitive devices for each temperature (25 °C, 40 °C and 55 °C) have been subjected to repetitive impact stress up to 1 million cycles using the above mentioned pulse. The evolution of $S_{11} @ +V_{MAX}$ and $S_{21} @ +V_{MAX}$ during the stress test obtained from the mean of the three devices are plotted in Figure 4.26.

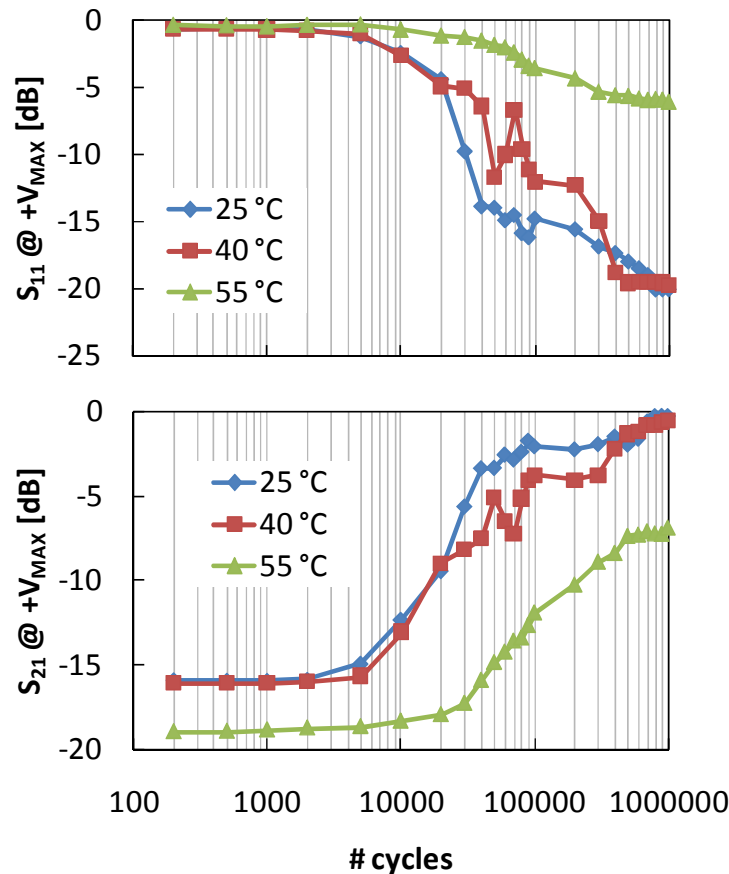


Figure 4.26: Evolution of $S_{11} @ +V_{MAX}$ and $S_{21} @ +V_{MAX}$ obtained from the mean of the nine different devices (three for each temperature).

From the results it is clear that increasing the number of cycles at 25 °C the $S_{11} @ +V_{MAX}$ decreases from -0.6 dB to -20 dB and $S_{21} @ +V_{MAX}$ increases from -16.2 dB to 0 dB. The effect is different increasing the temperature. In fact at 55 °C the final value is -6 dB regarding S_{11} and -8.5 dB regarding S_{21} . This fact can be explain with a more reliable contact during the characterization produced by the higher temperature. A first consideration can be carried out: the atmosphere (air in this work) is of fundamental importance for RF MEMS switches [52] since the degradation of the S-parameters results in 100K cycles. The hermetic package

can increase drastically the performances of the switches [53] and different results would have been obtained with N₂ controlled atmosphere or with hermetically packaged devices. Our primary purpose is not to draw conclusions about the absolute lifetime of the devices but to investigate the effect of temperature on the contact. A second consideration can be carried out regarding the RF Power: during the cycling procedure 0 dBm are forced in the input port of the device. The RF power can influence the lifetime of devices subjected to cycling stress tests. In fact it is known that increasing the RF power during hot switching the lifetime decreases [54] and the power can influence the mechanical reliability of the contact [55]. In this work 0 dBm level was selected in order to produce a light hot switching condition.

The evolution of the positive pull-in voltages extracted during the stress tests in the same way of the S parameters is shown in Figure 4.27.

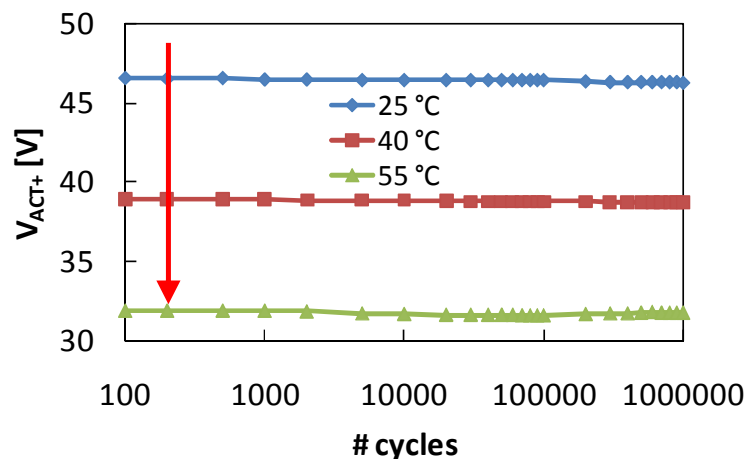


Figure 4.27: Evolution of positive pull in voltage extracted during the stress tests at different temperatures. Same results are extracted for negative pull in voltage and for release voltages.

The pull-in voltage remains practically constant during the entire stress. This confirms the small charge trapping during the stress test obtained combining a bipolar pulse during the cycling and a characterization as short as 1 second. Increasing the temperature of 15 °C results in a decrease of the actuation voltage of about 7 V (indicated by the arrow in Figure 4.27). This happens because the membrane internal stress decreases with the temperature, lowering the restoring force of the switch and thus decreasing the actuation voltage [56]. From Figure 4.27 we can conclude that the degradation of the electrical performances can be attributed only to the degradation of the contact and not to charge trapping

since no evident deviation of the pull in voltage is visible during the cycling stress test.

The results obtained in Figure 4.26 can be partially explained in the light of Figure 4.27. Being the bias voltage V_{MAX} the same for all the temperatures, this is barely 4 V above the actuation at 25 °C , but is 18 V above the actuation at 55 °C. It is then possible that the membrane shape and the force acting on the dimples are different at different temperatures, and the quality and the stability of the contact are known to improve sensibly when the contact force is higher.

Comparing the performances of devices with standard and modified floating metal, reported in Figure 4.28, it is evident that the modified material leads to better results in terms of contact performances. In fact, the insertion of a thin platinum layer in the gold above the dimples increases the contact hardness [50], increasing in turn its wear resistance.

Moreover, also the chemical resistance to oxidation of the modified material

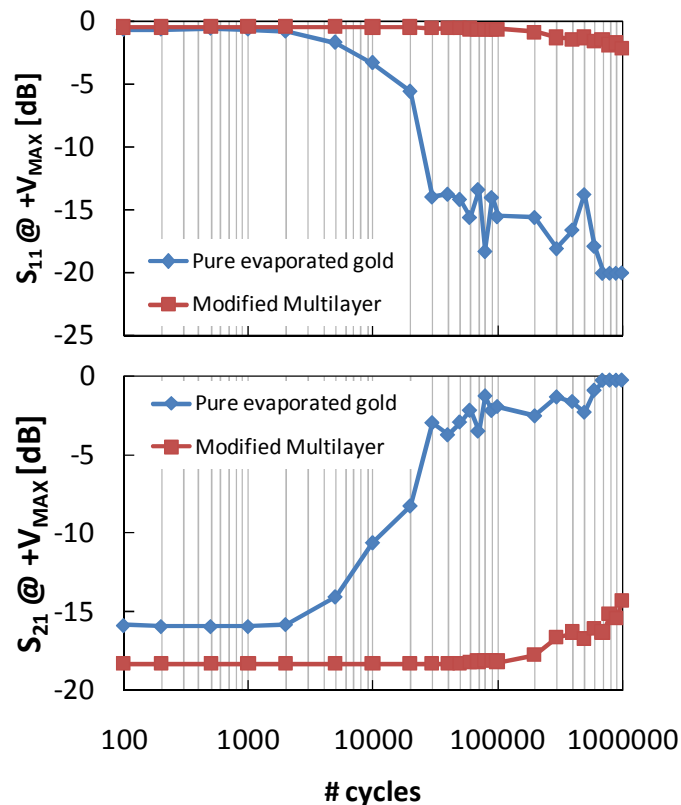


Figure 4.28: Evolution of $S_{11} @ +V_{MAX}$ and $S_{21} @ +V_{MAX}$ obtained from the mean of the six different devices (three with pure evaporated gold contact and three with modified multilayer contact).

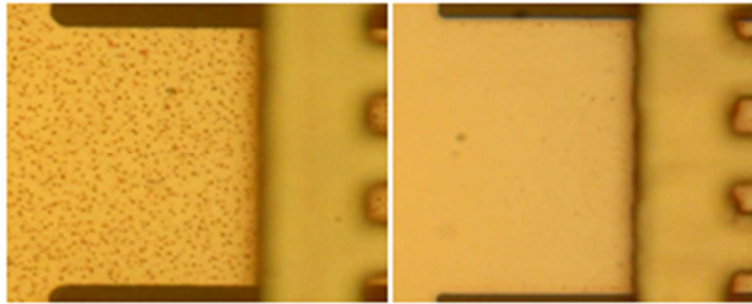


Figure 4.29: Contact region surface morphology (detail of Fig. 4.24) in the standard device (left) and in the modified contact material device (right). The small dots in the pure gold layer are due to the adhesion layer oxidation during oxygen plasma treatment during sample fabrication.

is improved, as shown in Figure 4.29, leading to a lower probability of chemical contamination of the contact. This results supports the general conclusion that the performance degradation detected after a relevant number of cycles is due primarily to contact consumption, chemical contamination or wear.

Further investigation have been done with SEM analysis (on different devices) in order to investigate the nature of the degradation. Figs. 4.30 and 4.31 show possible case of “purple plague”, an intermetallic compound of gold and aluminum ($AuAl_2$) with brittle mechanical behavior. Despite the origin of this intermetallic probably dates back to the fabrication process, the reduction in volume and the cavities originated in this region causes probably faster degradation of the material due to its lower mechanical strength. In the range of cycles number considered, the effects of surfaces degradation due to the impacts and to contact wear are largely limited to those regions where microfabrication features are already present. Here, the reduced material strength and the weakness of some features are probably responsible of surface topography variations and, consequently to changes in the electrical properties.

4.2.3 Conclusion of cycling

The results show a degradation of the contact increasing the number of the cycles with a consequent decreasing of the electrical S-parameters. During the stresses the pull in voltage remains practically constant indicating that no charge trapping occurs during the entire cycling procedure. The temperature can influence drastically the contact performances. At 55 °C the devices present better electri-

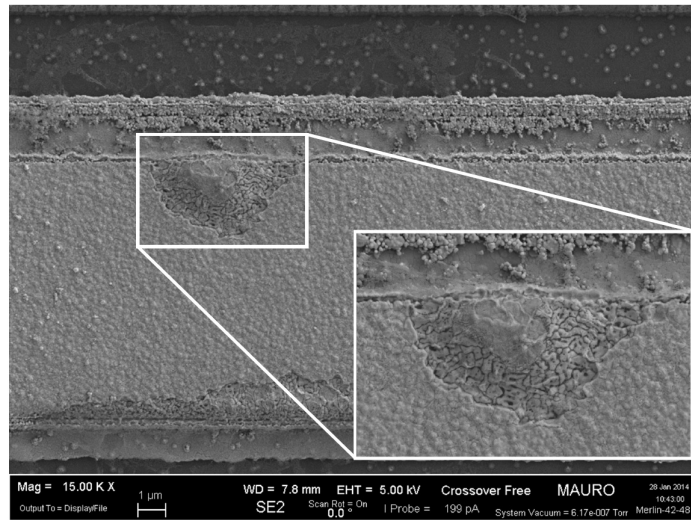


Figure 4.30: Detail of lower electrode after 1M cyclic stress test

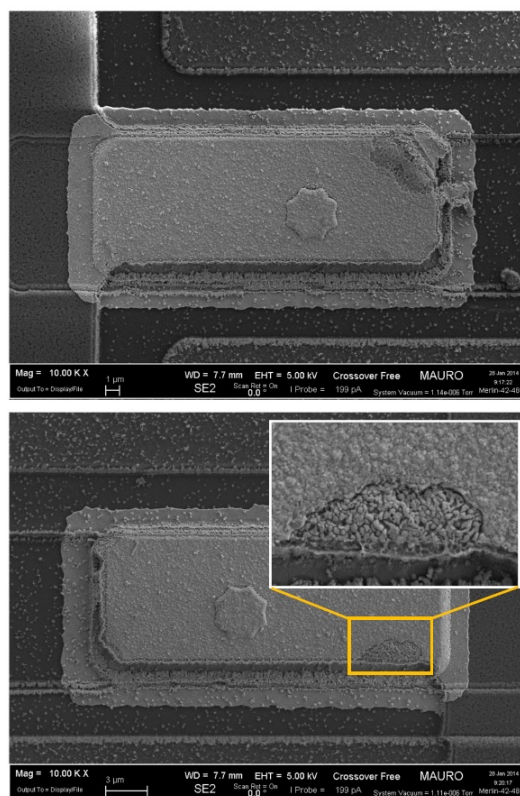


Figure 4.31: Detail of lower electrode after 100M cyclic stress test

cal performances indicating a more reliable contact. The use of a platinum layer can improve the performances of the contact. We show that standard devices present a significant degradation of the S-parameters after 10^4 cycles while the

modified contact presents good electrical performances at the end of 10^6 cycles. We remark that the measurements were done in a not controlled atmosphere and the concepts can be transposed in hermetically encapsulated RF MEMS switches. Further investigation will be done in future works regarding encapsulated devices in order to validate the concepts extracted in this paragraph.

4.3 Dynamic measurement results (Polytec MAS-500)

This section shows the potentialities of two characterization procedures on the electrical and mechanical characterizations of ohmic RF microelectromechanical systems (MEMS) switches [57]. The first is a “fast electrical” procedure that uses an electrical stimulus and monitor the RF signals at the input and output ports of the switch; the second is a “fast hybrid” procedure – electrical and mechanical – with an electrical input adopted to actuate the device and a mechanical measurement conducted with an optical profilometer which monitors the displacement and the velocity of the moving membrane when the input electrical signal is applied. Both systems are validated on cantilever and clamped-clamped resistive RF–MEMS switches. We developed these measurement procedures to speed up the measurement process and consequently to limit the charge trapping during the characterization process. In future analyses, the procedure will be systematically applied to investigate reliability issues when the switch is subjected to multiple impacts and long term actuation. The use of such procedures will permit to separate electrical and mechanical failure mechanisms.

RF–MEMS can be used in communication between satellites and wireless system on earth as well as between radar systems and adjustable antennas [58]. In these applications a fast switching time [1] and a response without bounces during the actuation phase are required, in order to avoid delays and false opening of the switches. For these reasons it is primarily important to characterize the dynamic behavior of switches both in the frequency [59] and in the time domain. Despite several works in literature devoted to RF–MEMS switches, they mainly address some design-related problems or the development of new structures. However less studies address the reliability, which remains an open and challenging issue for several applications. In this section we are proposing a novel approach that combines an electrical and a mechanical procedure for the dynamic characterization of RF–MEMS switches behavior.

Standard electrical and mechanical characterization procedures are not able to provide information regarding the robustness of microstructures considering both electrical and mechanical behaviors. These limitations are evident in the device reliability where the failure may derive from either electrical [31] or mechanical origin [60]-[61]. In order to solve this mismatch, one way is to combine different characterization methodologies (i.e. electrical and mechanical) and to provide the results to the designers to reduce the failure mechanisms. One example is the characterization of the impact velocity with electro-mechanical tests in combination with the characterization of the surface deterioration (two different problems that contribute to the contact degradation and that must be treated jointly).

The aim of the section is to show the potentialities of the two methodologies in the characterization of different types of RF-MEMS switch (i.e. cantilever and clamped-clamped) and to correlate the respective results. This procedure might be successfully employed also in more elaborated measurement systems and analyses, such as cycling stress systems [62] and long term stress systems [63].

The section is organized as follows: 1. We present the device which will be later used to validate and discuss the procedure. 2. We describe the combined electro-mechanical procedure. 3. We present some case studies of RF-MEMS switches characterization, using our combined techniques: the first is the extrapolation of the actuation and release voltages with high resolution and low impact in the charge distribution inside the device; the second is the analysis of the actuation time with details on the dynamic behavior and finally the rebounds can be analyzed in detail. All the analyses can be done with both the systems and we compare accurately the results in order to validate the respective conclusions.

4.3.1 Devices Description

We have considered two different types of ohmic series devices: cantilever and clamped-clamped. Two photos of the devices are presented in Fig. 4.32. The difference between the two types is the positioning of the moving membrane: for clamped-clamped configuration (a) the membrane is 90 degree rotated respect to the CPW (Coplanar Waveguide) while in cantilever configuration (b) the membrane is a prolongation of the CPW. For a detailed description of a clamped-clamped switch, please see [64].

The devices are manufactured by FBK-IRST (Trento, Italy). The technology

utilized for the fabrication of studied devices consists of an eight masks surface micromachining process. A brief view of the technological process is shown in Fig. 4.32 (c). A more detailed description is presented in [37] and in [65]. We analyze the behavior of both types, underlining the strengths and weaknesses of the two different configurations.

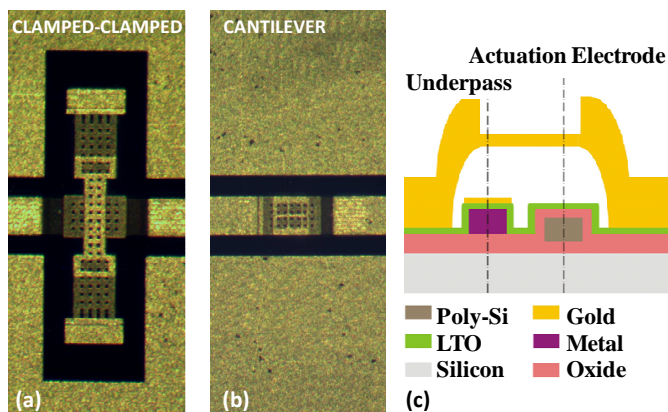


Figure 4.32: Photos of devices and technological process. (a) Clamped-clamped configuration, (b) cantilever configuration and (c) technological process scheme (section view).

4.3.2 Measurement Procedure Description

Fast Electrical Characterization Procedure In order to investigate the response of the devices during the characterization process, a dedicated measurement procedure was developed. Fig. 4.33 shows a simplified block diagram of the instruments and connections: a VNA (Vector Network Analyzer, HP 8753E) is used to generate the RF wave (6 GHz) which is applied to the device terminal $RF-IN$, the device terminal $RF-OUT$ is connected to a 8 GHz bandwidth oscilloscope (DSO, Tektronix TDS6804B) in order to measure the output signal from the RF-MEMS switch.

The fast actuation is obtained with an AWG (Arbitrary waveform generator, Agilent 33250A) that is able to generate a triangular waveform with a maximum frequency of 80 MHz. In order to actuate the MEMS device, a voltage amplifier (FLC Electronics A400) is connected in series between the AWG and the DUT, producing the 20X gain required to obtain the ± 100 V actuation voltage. The entire system is synchronized using a dedicated LabView software.

The AWG generates a triangular waveform and the DSO acquires the voltage

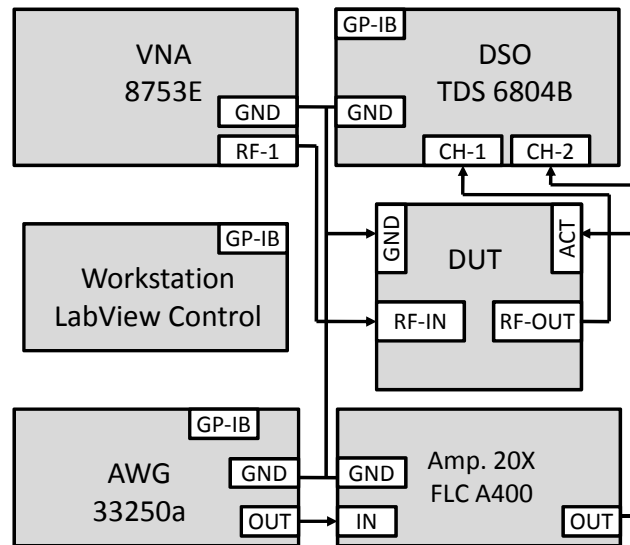


Figure 4.33: Schematic block diagram of the Fast electrical characterization procedure.

applied to the actuation pad and synchronously the RF voltage at the output port of the device. In this way it is possible to extrapolate the actuation and release voltages. The sweep duration can be varied from 1 ms to 10 s in order to study the actuation and release voltages on the sweep duration. Fig. 4.34 shows the data acquired from the DSO for a sweep time of 1 ms.

The following parameters can be extracted from this measurement: the positive actuation voltage, V_{ACT+} , the positive release voltage, V_{REL+} , the negative actuation voltage, V_{ACT-} , and the negative release voltage V_{REL-} . Noticeably, an hysteresis of approximately 5–10 V is observed between actuation and release for both positive and negative voltages. It is worth to remark that these parameters are obtained only monitoring the RF signal at the output port with the 8 GHz bandwidth oscilloscope. This technique greatly increased the voltage sweep velocity rather than to monitoring the RF signal with the secondary port of the VNA [37]. In fact, the VNA has a limited number of acquisition samples (several thousands), and plentys of measurements are needed in order to remove noise and to obtain accurate data. This increases the time needed for characterization. On the other hand the DSO can acquire as many as millions of samples. Hence, the DSO permits us to acquire enough accurate data with only one measurement, saving time.

Fast Hybrid Characterization Procedure The mechanical characterization procedure is schematically presented in Fig. 4.35. The micro system analyzer (Polytech MSA500) equipped with the controller OFV 5000 is used for the dynamic characterization with an AWG (Agilent 33250A) and a voltage amplifier (FLC Electronics A400) which is able to generate the appropriate actuation signal. The system is well suited for non-contact and non-destructive measurements of three-dimensional movements in microsystems. The MSA500 thereby measures out-of-plane movement using the microscope scanning vibrometer (MSV) on the basis of laser interferometry.

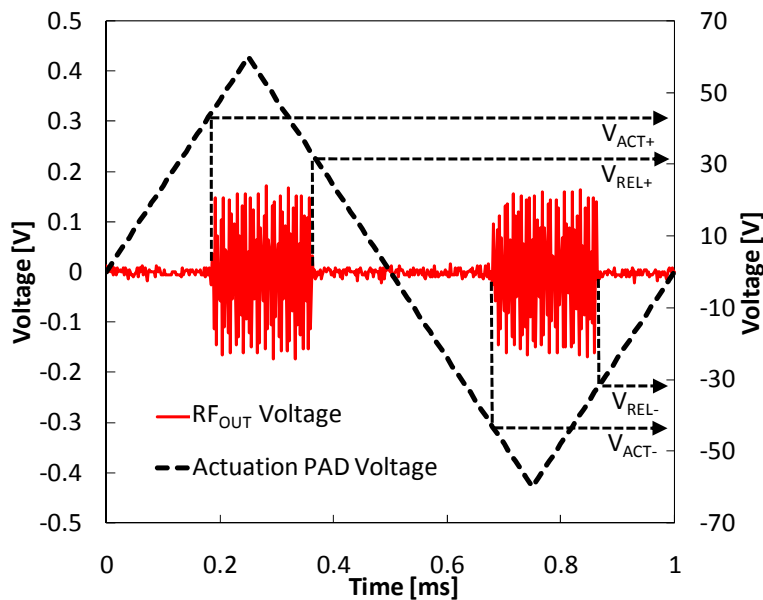


Figure 4.34: Acquired signals from DSO during a measurement process of 1 ms duration time.

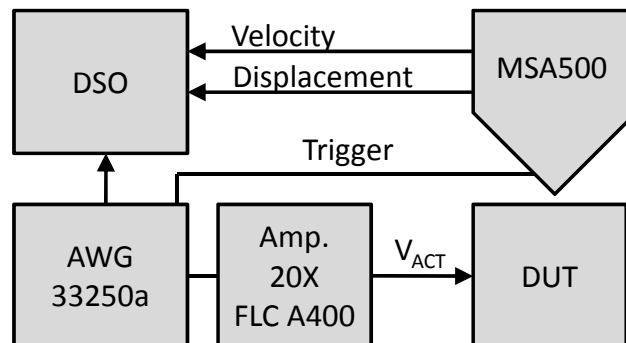


Figure 4.35: Schematic block diagram of the Fast hybrid characterization procedure.

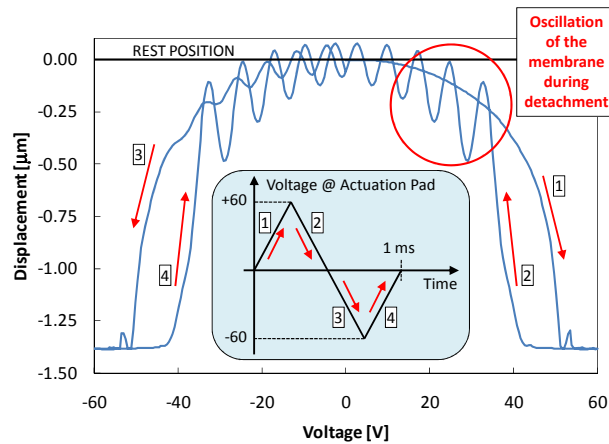


Figure 4.36: Measurement obtained with the MSA500 system. Displacement vs. Applied Voltage.

The MSV uses the principle of the heterodyne interferometer to acquire the characteristics of mechanical vibrations or transient motion processes. With this type of interferometer, a high-frequency carrier signal is generated on the photo detector with the help of a Bragg cell. To measure the vibration, the beam of a helium-neon laser is pointed at the vibrating object and scattered back from it. Velocity and displacement amplitude of a vibrating object generate a frequency or phase modulation of the laser light due to the Doppler effect. The velocity information is recovered from the frequency modulation of Doppler signal, while the displacement signal can be reconstructed from the phase modulation available at the same time. In addition, 3D topography measurements can also be made with the topography measurement system (TMS) to acquire the surface geometry of rough and also reflective structures. The TMS measurement is based on the principle of the white light interferometer; in this technique, the interferometer uses a light source with a large spectrum and thus low time coherence.

The results are shown in Fig. 4.36. A triangular voltage signal of 1 ms period is applied on the actuation pad and the displacement of the membrane is monitored. We can see that for positive voltage the cantilever starts from a stationary zero position, then when the membrane is detached, the natural oscillation of the membrane is visible (highlighted by the circle). These oscillations are visible because the total sweep time of the measurement process is comparable with the natural response of the cantilever. For negative voltage the behavior is similar but the residual oscillations of the membrane is visible also in the first part of the negative sweep due to the residual oscillation of the positive sweep.

4.3.3 Experimental Results and discussions

In this section we present the experimental results obtained using the two different measurement techniques for the dynamic characterization and the study of bounces. The results are divided into three parts: (i) we present the analysis of the actuation and release voltages with different velocities of the characterization process and the analysis of the charge trapping during the characterization phase. (ii) we analyze the actuation time (i. e. the time required for the closure of the switch) at different pulse voltage levels extracted using both characterization techniques. Finally (iii) we study the bounces when increasing voltage steps are applied to actuate the devices.

Actuation and release voltages analysis The extracted parameters obtained with different sweep times using the fast electrical characterization procedure are shown in Fig. 4.37 for a resistive switch.

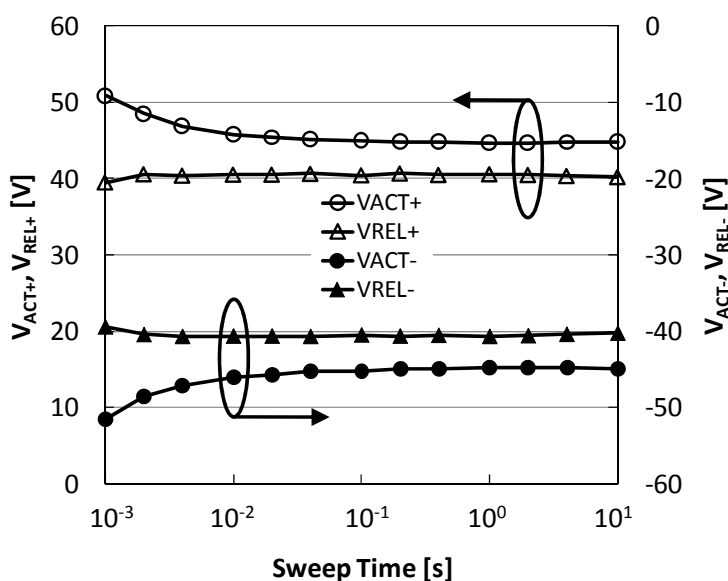


Figure 4.37: Actuation and release voltages vs. Sweep time of a series resistive RF MEMS switch.

It can be clearly noticed that reducing the sweep time below 10 ms, a significant increase, in absolute value, is observed in the actuation voltage. This shift can be related to the mechanical inertia of the devices: trying to quickly move the cantilever, the response could be delayed, showing an higher actuation voltage [66]-[67]. This phenomenon is completely reproducible, because the process is totally ascribed to the dynamic behavior. In fact, by repeating the entire

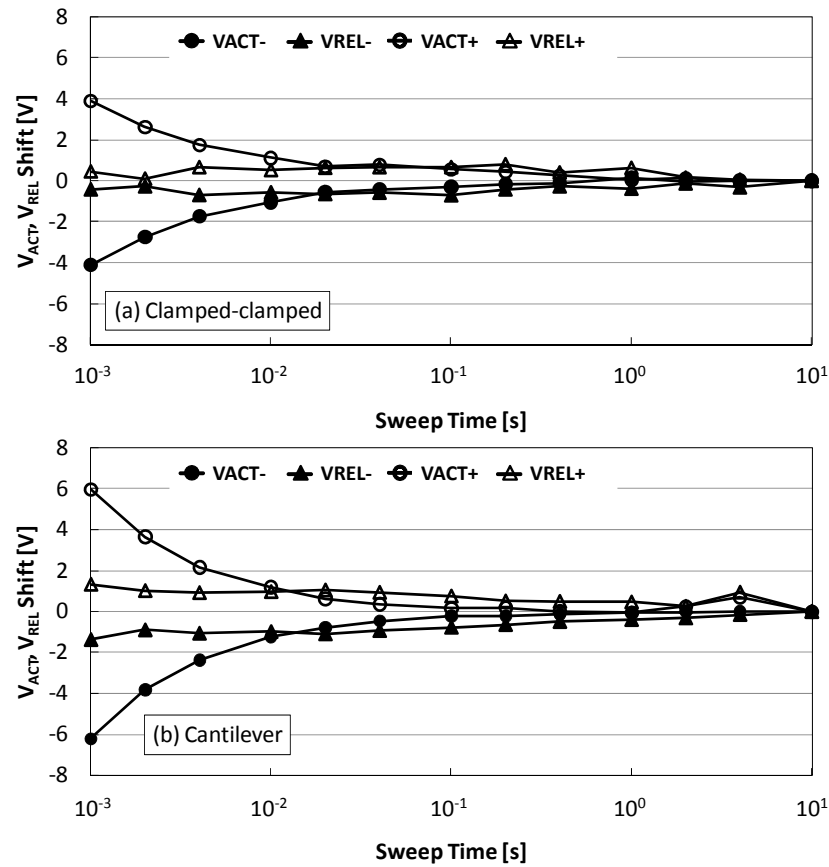


Figure 4.38: V_{ACT} and V_{REL} shift comparison about different structure design; (a) clamped-clamped configuration and (b) cantilever configuration.

experiment several times consecutively we obtained the same results indicating that charge trapping is not responsible for the observed shift.

Furthermore, the deviation of the release voltage is even less evident than the actuation voltage: the shift of the positive actuation voltage is over 6 V while the deviation of the positive release voltage is near 1 V.

Fig. 4.38 shows the shift of the actuation and release voltages obtained from the average of the measurements on three different devices for each type (clamped-clamped (a) and cantilever (b)) with the fast electrical characterization procedure. The shifts collapse to zero for high sweep times and increase (in absolute value) as the sweep time decreases. Noticeably, the shift is more pronounced for the actuation voltage rather than release voltage. This is in accordance with the mechanical inertia of the membrane: in fact the actuation point is reached after a deflection of the membrane (during which the inertia remarkably contributes delaying the actuation) while the detachment point happens immediately after a minimal movement of the bridge from the “down position”. Hence all the

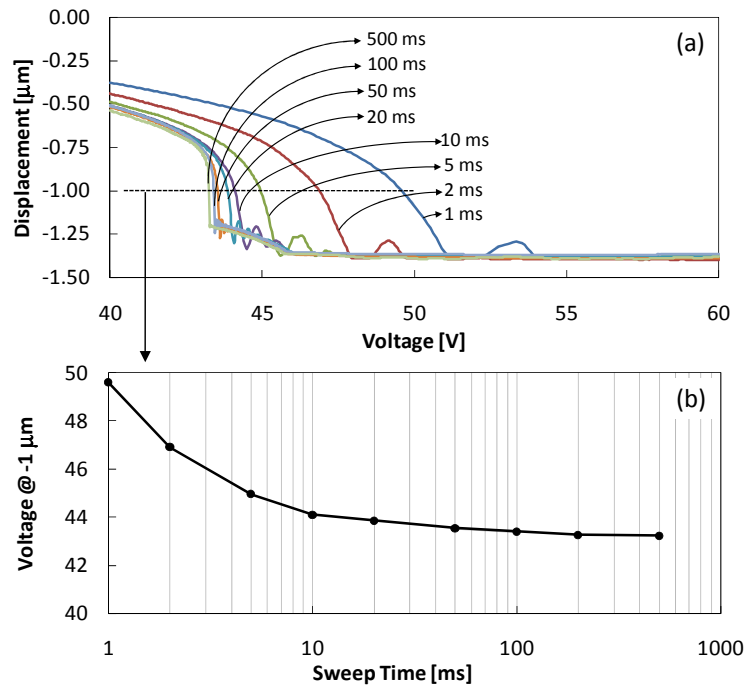


Figure 4.39: (a) Detail of the actuation point obtained with the hybrid measurement procedure with different sweep times on cantilever configuration and (b) Voltage at -1 micron vs. sweep time.

displacement (and the corresponding inertia effect) happened after the initial movement is irrelevant to the release voltage. The results are similar for both types but in cantilever configuration the shift of actuation voltage is larger than in clamped-clamped configuration due to the different mechanical conformation of the two designs.

The results can be obtained in similar way from the hybrid measurement procedure. The results are shown in Fig. 4.39 (a) for the cantilever typology. By increasing the sweep time from 1 ms to 500 ms the actuation voltage decreases (from about 51 V to 43 V). For sake of clarity we present in Fig. 4.39 (b) the evolution of the voltage required to reach a constant displacement of -1 μm . It can be seen that this voltage decreases through increasing the sweep time.

At this point a couple of consideration are worth to be done. First of all, it is well known from literature that a shift of the actuation voltage is correlated to the charge trapping phenomena [68]-[32]-[34], but this is not our case. In fact actuation and release voltages shift are mainly due to the inertia, being any degradation negligible. Besides inertia, also temperature may play a significant role [69]. In fact we cannot exclude that a localized temperature increase may

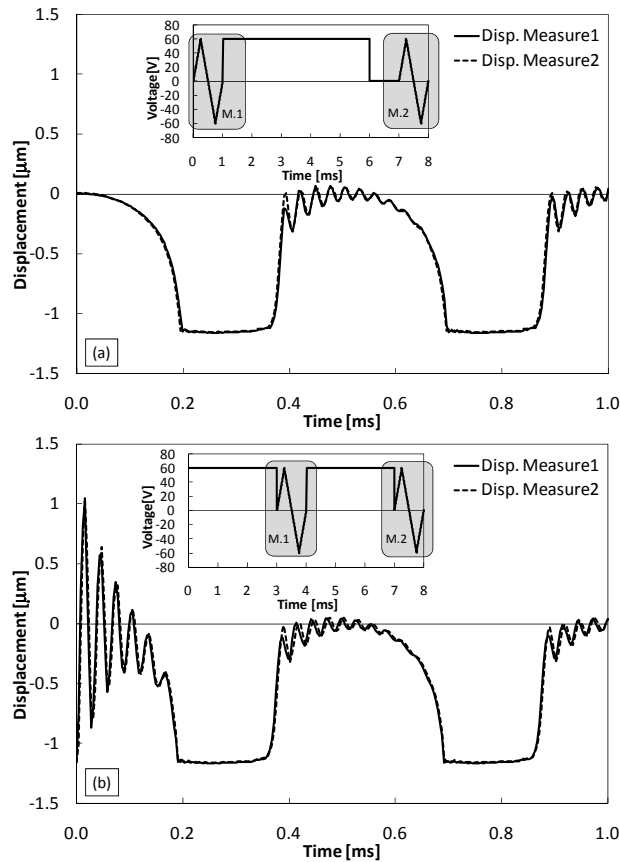


Figure 4.40: Displacement measurement vs. time repeated two times with two different positioning of the characterization procedure during a DC biasing period.

occur in the near neighbour of the anchors, which is the most stressed region of the cantilever, once the membrane is moved. At high frequency the localized heating can change the elastic modulus of the material and, in turn, can lead to a global variation of the mechanical structure stiffness.

In the experiment of Fig. 4.40 (a) we performed a measurement and we kept the device biased at 60 V for 5 ms to allow any possible fast charge trapping. Later on we applied a 0 V pulse to bring the switch in the release state and we reported the measurements before and immediately after the biasing period. In Fig. 4.40 (b) we reported the same procedure, but without the 0 V pulse. In this way the second measurement starts immediately after the 60 V bias period. We repeated 10 cycles, and we verified that they are perfectly overlapping each other. For sake of clarity in Fig. 4.40 (a) and Fig. 4.40 (b) we show only the first and the second cycle. In Fig. 4.40 (b) an initial oscillation of the membrane is visible because the measurement period starts after a biasing period while in Fig. 4.40 (a) this phenomenon is avoided inserting a zero voltage level before the

measurement period. In particular in Fig. 4.40 (b) there is no time between the actuation period and the next characterization phase to obtain the release of the eventual charge trapped. So if a fast charge trapping occurs, we would expect that the two measures do not overlap since charge trapping issue is associated with shifting of actuation and release voltages. Instead for both experiments we do not observe deviations of actuation and release voltages (displacement measure one and displacement measure two are practically overlapped) so we can conclude that the charge trapping phenomenon is avoided and no significant charge trapping occurs during a characterization period that is less than few milliseconds.

Actuation time analysis Fig. 4.41 presents the actuation time analysis about a cantilever switch. The device is actuated using a voltage pulse with an increasing level from 40 V to 100 V and a frequency of 100 Hz. We can see that under 60 V the device is not actuated, since the displacement presents an oscillating response (40 V and 50 V respectively). Over 60 V the switch goes into a low position and then with increasing voltage levels the actuation time decreases. The extracted actuation times are shown in Fig. 4.42 (b) (empty circles). The results are in agreement with [70] where the actuation time decreases not linearly with pulse voltage. The analysis has been made also with the fast electrical procedure obtaining the same results (empty triangles).

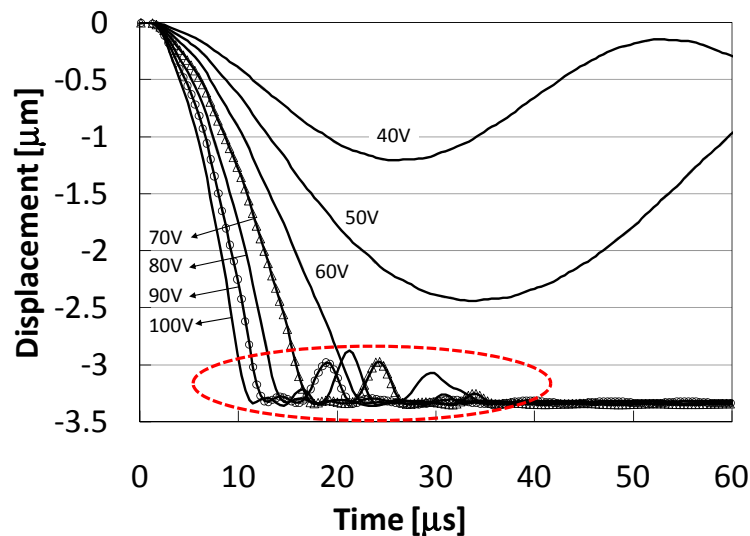


Figure 4.41: Displacement vs. Time for step pulse square voltage applied to actuation pad about a cantilever switch.

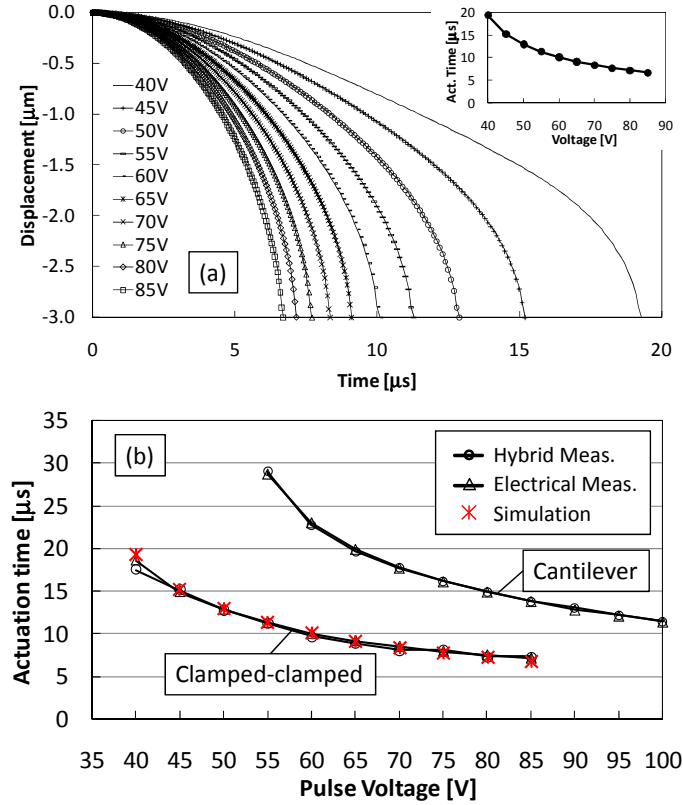


Figure 4.42: (a) Solution of equation (1) for a clamped-clamped device and (b) Actuation Time vs. Pulse voltage extracted with hybrid procedure and electrical procedure for both types of devices and simulation for clamped-clamped design.

The study of the actuation time can be made using the 1-D dynamic model expressed as:

$$m \frac{d^2x}{dt^2} + b \frac{dx}{dt} + kx = \frac{1}{2} \frac{\epsilon_0 AV^2}{(g_0 - x)^2} \quad (4.8)$$

where k is the spring constant, m is the effective mass, x is the position of the beam, A is the actuator area, V is the applied voltage, b is the damping coefficient and g_0 is the air gap. Fig. 4.42 (a) shows the solution of the differential equation with parameters:

- $m = 1.01799\text{e-}9$ [Kg]
- $b = 9.84944\text{e-}6$ [Kg/s]
- $k = 42.45$ [N/m]
- $A = 2.6561\text{e-}8$ [m²]

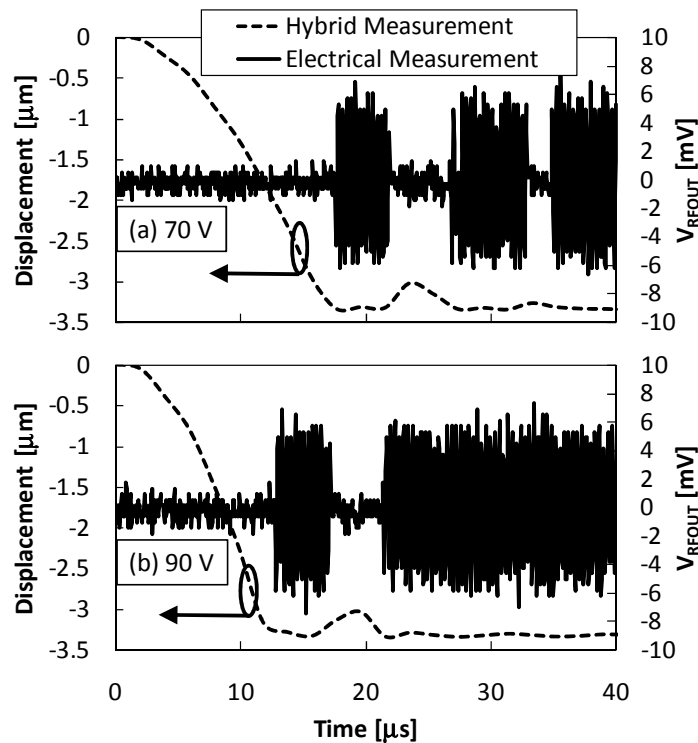


Figure 4.43: Comparison between electrical and hybrid measurements in rebounds observation of cantilever configuration.

- $V =$ from 40 to 85 [V]
- $g_0 = 3e-6$ [m]

that were extracted by topography and frequency response analyses of a clamped-clamped switch.

The experimental results about clamped-clamped configuration are presented in Fig. 4.42 (b) and are in agreement with simulation results. Clamped-clamped devices present an actuation time that is better than the cantilever configuration and also a lower actuation voltage (40 V versus 55 V).

Bounces analysis In Fig. 4.41 the closure process presents some rebounds that are visible just over the actuation voltage (highlighted with a dashed circle). This effect is much less visible for higher pulse voltages applied to the actuation pad. In fact with a voltage of 90 V only one bounce occurs (curve with open circles) while with an actuation signal of 70 V (curve with open triangles) there are two bounces. This is clearly visible from Fig. 4.43 where the mechanical displacements and the electrical output signals obtained with a 70 V pulse and

a 90 V pulse are compared. The effect of the bounces is to open and to close the device repetitively after the first closure. The electrical behavior (see V_{RFOUT} signal) is clearly due to bounces, in fact the points in which the electrical signal is down, correspond to the points where the membrane seems to detach (see dashed lines). This conclusion can be drawn from the comparison of the two different investigation procedures (i.e. fast electrical procedure and fast hybrid procedure).

4.3.4 Reliability evaluation with the developed procedures

From the data and discussions presented in previous section it is clear that this novel combined electro-mechanical analysis can be successfully implemented to improve the reliability study of RF–MEMS switches, collecting more accurate information. A couple of examples are discussed in the following.

First of all, the application of the developed systems is of particular interest in long term stress tests [37] where the device is maintained actuated for a long time and, at certain established moments is released to be characterized. In such stress test procedure the measurement process itself can influence the charge distribution and can lead to a wrong lifetime extrapolation. The characterization procedure described above is sufficiently reduced in time to prevent a considerable charge rearrangement but long enough to not influence the dynamic mechanical response of the membrane and to obtain accurate values of the actuation and release voltages. This permits to reduce appreciably the measurement–induced perturbation in the degradation kinetics.

The second example is represented by all these applications, where the number of openings/closures is high and the contact safeguard is of particular importance. In fact the repetitive rebounds of the moving membrane can lead to a preliminary failure of the device performances due to the large increment of the impacts. Moreover, if the device is switched on and off for many times in succession the number of impacts is drastically increased by bounces and this effect limits the lifetime of the device itself. With the developed measurement procedures a good estimation of the impacts can be done and the hybrid procedure can be used to analyze mechanical modifications of the membrane during the stress test (change of stiffness, mechanical cracks, stretching of the membrane), which cannot be done only with electrical measurements.

From the previous analysis we conclude that with a higher voltage the bounces are limited and the switching time is reduced. The problem of the high voltage

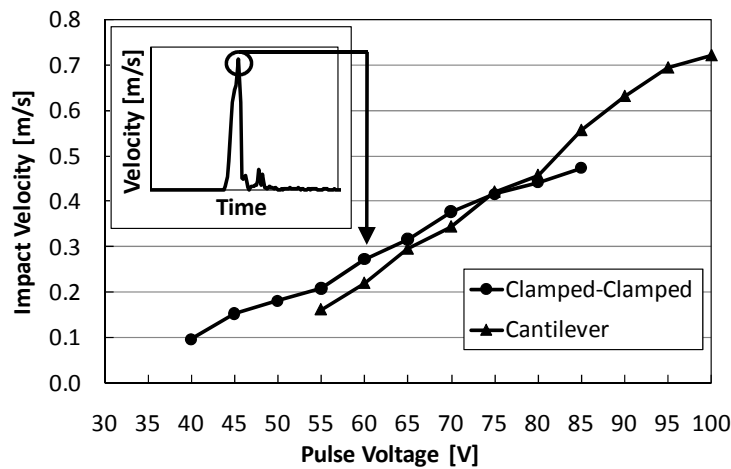


Figure 4.44: Impact Velocity vs. Pulse voltage extracted from mechanical measurement for both types of devices.

is the major impact force and so the higher degradation of the gold-gold contact [71]. This can be argued from Fig. 4.44 where we report the impact velocity as a function of the actuation pulse voltage amplitude.

The impact speed is increased the more the voltage is increased for both clamped-clamped and cantilever configurations. Both switches types present similar impact velocity values between 0.1 m/s and 0.7 m/s varying the actuation signal. In particular the impact velocity has a linear dependence with the applied voltage pulse. So with a higher voltage signal the bounces decrease but the impact velocity increases: the optimal balance has to be found in order to minimize the contact degradation during repetitive closures of the switch [48]-[47]. It is worth remarking, that the application of the procedures described in this paragraph is of great interest in the reliability field since it largely contributes to identify degradation modes and mechanisms (electrical and mechanical) and to estimate the lifetime of the studied electromechanical devices with better accuracy. One example is the correlation between the impact velocity and the on-state contact resistance variation. In fact, in long cycling operation the on resistance can be affected by the numerous impacts and its value can increase up to the point of making the device unusable [35]-[72]. Estimating the impact velocity, for different actuation voltages, operating conditions, MEMS structures, or materials, it may give further information about the origin of the degradation (contamination of surface, quality of contact area, etc) and it may give some suggestions, which can help to adopt the more suitable solutions to overcome the problem (improved packaging, addition of particular layers in the contact region, etc), improving

the device performance and reliability in the long term.

4.3.5 Conclusion of dynamic characterization

We present a novel RF-MEMS switches characterization approach which consists in the combination of the electrical and the mechanical measurement procedures based on the use of a high band oscilloscope and of the profilometer Polytech MSA500. The effectiveness of the systems was verified by testing two different types of resistive switches, obtaining results in term of release and actuation voltages extrapolation, actuation time analysis and study of bounces. Such results confirm that the characterization sweep time is of particular importance in reliability studies: from the stress tests point of view, one would like to keep the characterization time as short as possible provided that no artifacts are introduced in the extrapolation of the actuation and release voltages. Our developed procedures can be used to find the optimal characterization speed for each kind of device. A correlation between electrical and mechanical measurements was carried out with good results in term of investigation of bounces and intrinsic dynamic response of the devices. In reliability issues related to very fast on/off switching the use of the presented procedure is of particular importance. In fact, it permits the splitting of electrical and mechanical failure mechanisms. An example of the combination of the two measurement procedures is the relationship between the impact velocity and the number of bounces presented in Fig 4.44. An optimal actuation signal must be chosen in order to minimize the bounces and the impact velocity of the membrane and to obtain, in turn, a small degradation of the contact.

Chapter 5

PV-CELLS, Manufacturing and Design

Edmond Becquerel appears to have been the first to demonstrate the photovoltaic effect [73]-[74]. Working in his father's laboratory as a nineteen year old, he generated electricity by illuminating an electrode with different types of light, including sunlight (see the Figure 5.1). Best results were obtained with blue or ultraviolet light and when electrodes were coated with light sensitive material such as AgCl or AgBr. Although he usually used platinum electrodes, he also observed some response with silver electrodes. He subsequently found a use for the photovoltaic effect by developing an "actinograph" which was used to record the temperature of heated bodies by measuring the emitted light intensity [75].

The next significant photovoltaic development arose from the interest in the photoconductive effect in selenium. While investigating this effect, Adams and Day (1877) [76] noted an anomaly they thought could be explained by the generation of internal voltages. They investigated this anomaly more carefully using samples as shown in Figure 5.2. Heated platinum contacts were pushed into opposite ends of small cylinders of vitreous selenium. The objective of one experiment conducted by Adams and Day upon such specimens was to see 'whether it would be possible to start a current in the selenium merely by the action of light'.

The result was positive! This was the first demonstration of the photovoltaic effect in an all solid-state system. Adams and Day attributed the photogenerated currents to light induced crystallization of the outer layers of the selenium bar. Several decades were to pass before the development of physics allowed more insight into this process.

The next significant step forward came seven years later with the work of

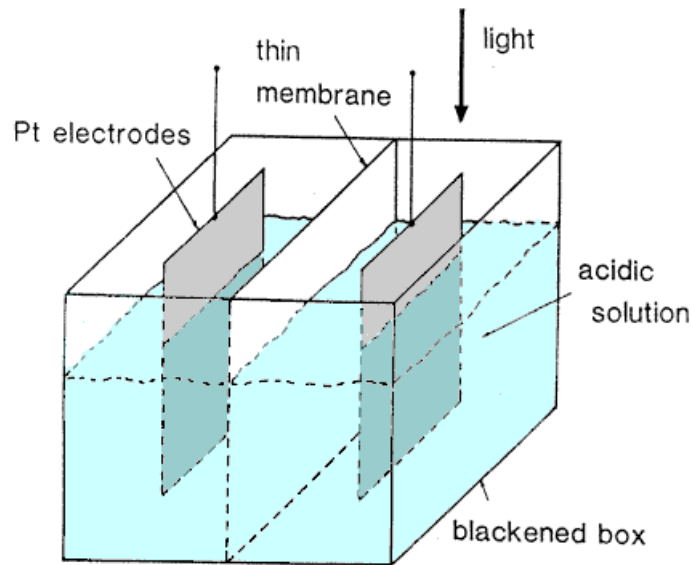


Figure 5.1: Diagram of apparatus described by Becquerel (1839).

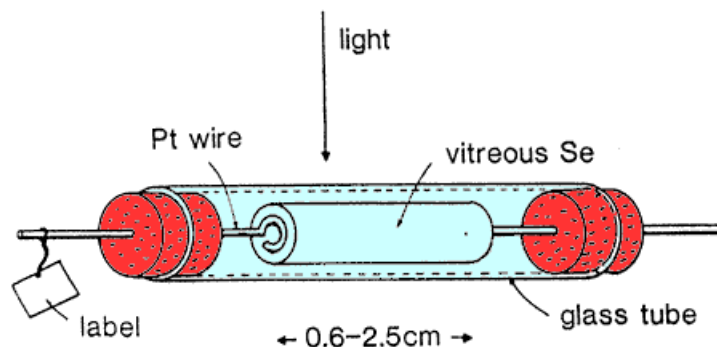


Figure 5.2: Sample geometry used by Adams and Day (1876) for the investigation of the photoelectric effects in selenium.

Fritts (1883) [77]. By compressing molten selenium between plates made from two different metals, Fritts was able to prepare thin Se films which adhered to one of the two plates, but not to the other. By pressing a gold leaf to the exposed selenium surface, he thereby prepared the first thin-film photovoltaic devices (Figure 5.3). These first thin-film devices were as large as 30 cm^2 in area.

He was also the first to recognize the enormous potential of photovoltaic devices. He saw that the devices could be fabricated at very low cost and noted that 'the current, if not wanted immediately, can either be "stored" where produced, in storage batteries... or transmitted... to a distance, and there used, or stored'.

It was, however, to be nearly fifty years before there was another significant

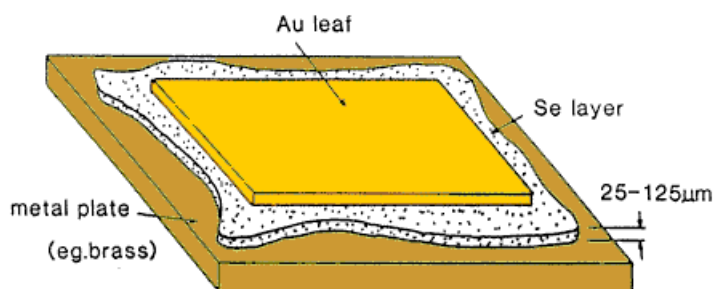


Figure 5.3: Thin-film selenium demonstrated by Fritts in 1883.

burst of activity in this area.

While studying photoconductive effects in cuprous oxide layers grown on copper, the rectifying action of the copper-cuprous oxide junction was discovered. This led to the development of large-area rectifiers, followed soon after by large-area photocells. Grondahl [78] describes the development of both copper-cuprous oxide rectifiers and photovoltaic cells.

The figure 5.4 shows the very simple structure used by the earlier cells based on the copper-cuprous oxide junction. A coil of Pb wire is used to give a grid contact to the illuminated surface of the cell. This approach was subsequently refined by sputtering the metal on the outer surface and removing a part of it so as 'to form a grid of any desired fineness'. These developments seem to have stimulated a great deal of activity in this area. Grondahl documents 38 publications dealing with copper-cuprous oxide photovoltaic cells over the period 1930-32.

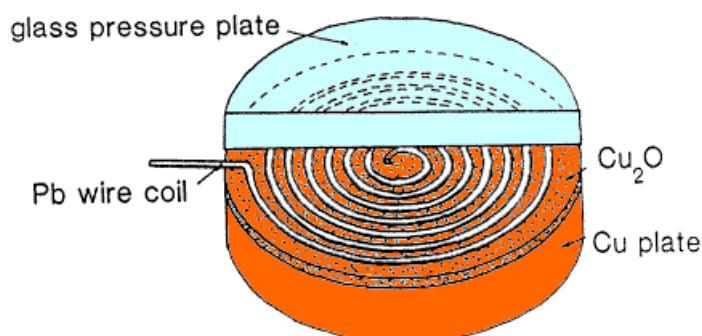


Figure 5.4: Early Grondahl-Geiger copper-cuprous oxide photovoltaic cell (circa 1927).

This activity also seems to have reawakened interest in selenium as a photovoltaic material. In particular, Bergmann [79] reported improved selenium de-

vices in 1931. These proved superior to the copper-based devices and became the commercially dominant product. In 1939, a thallosulphide cell of similar performance was also reported by Nix [80]. The structure of this device and of the most efficient selenium and copper-cuprous oxide devices took the form shown in the figure 5.5.

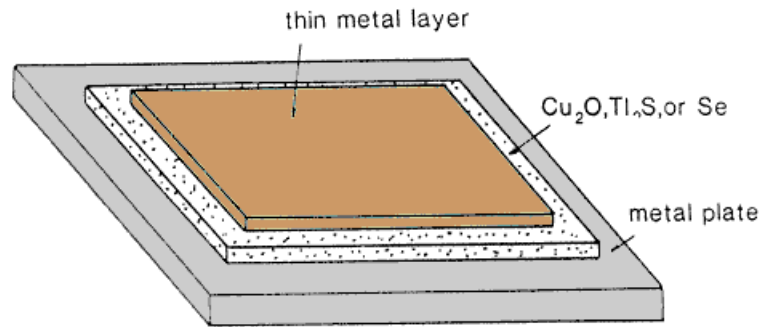


Figure 5.5: Structure of the most efficient photovoltaic devices developed during the 1930's.

At about the same time that selenium cells were under development in the 1930's, silicon was receiving increasing attention for its use in point-contact rectifiers. The rectifying properties of sharpened metal point contacts to various crystals had been known since at least 1874 [81]. In the early days of radio, such crystal rectifiers were the most commonly used detectors in radio receivers, but with the development of thermionic tubes, crystal rectifiers were replaced in all but ultra-high frequency applications. Tungsten points proved to be the most suitable material for making contact with silicon surfaces. Research into the purity of silicon also led to further understanding of its properties.

In studies of recrystallized melts of pure silicon prepared for this purpose, Ohl [82] discovered the presence of a well-defined barrier in ingots grown from commercially available, high-purity silicon (Figure 5.6).

In 1941, before even this limited understanding of dopants, silicon photovoltaic devices based on these natural junctions were described [82]. In the figure 5.6, (a) shows the naturally grown junction in a cast ingot of silicon. Ingots were produced from acid-leached metallurgical-grade silicon which were cooled from the top after melting. Cells were prepared by cutting from the ingot as indicated in (a). Alternatively, devices could be cut parallel to the junction as shown in (c).

This natural barrier was first found in rods cut from ingots for resistivity measurements. The rods showed good photovoltaic response, were found to have

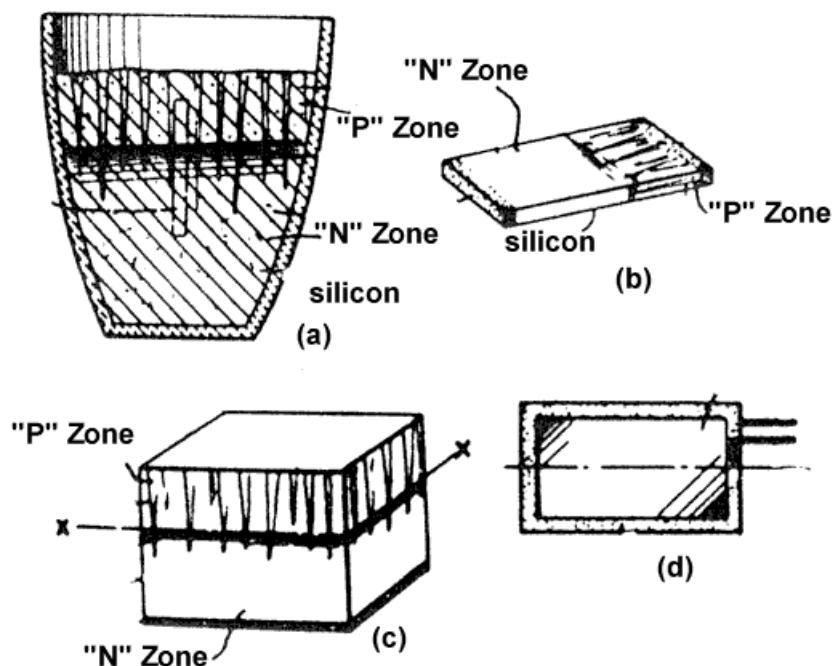


Figure 5.6: a) Cast ingot showing natural junction formed by impurity segregation during melting; (b) photovoltaic device cut perpendicular to junction; (c) device cut parallel to junction; (d) top surface of device cut parallel to junction.

a high thermoelectric coefficient, and had good rectifying properties. One end of the rod developed a negative potential when illuminated or heated and had to be biased negatively in order to show low resistance to current flow across the barrier or across a point contact to this material. Material with these properties became known as negative- or n-type silicon, and material of the opposite type was named positive-, or p-type. Subsequently the role of donor and acceptor impurities in producing these properties was shown.

Although these devices performed similarly to the thin-film devices then available, the preparation method did not obviously lend itself to convenient manufacture. However, it was clear that if a suitable method could be found to activate large areas of silicon surface uniformly, competitive cells could be made. In 1952, improved silicon solar cells were reported by Kingsbury and Ohl [83] using purer silicon to prevent growth junction formation and the ion bombardment of the surface to form the rectifying junction.

Meanwhile, development of crystal growth techniques and techniques for forming junctions by diffusion resulted in the announcement of the first modern silicon cell in 1954 by Chapin, Fuller and Pearson [84]. These cells had the

dual rear contact structure of the figure 5.7 and had an efficiency of 6%, about 15 times that of earlier devices, opening the first real prospects for power generation using photovoltaics. Considerable interest was aroused. However, given the immaturity of the silicon preparation industry, it soon became apparent that the initial enthusiasm was premature. Nevertheless, the cells proved suitable for space use and this formed their major application until the early 1970's.

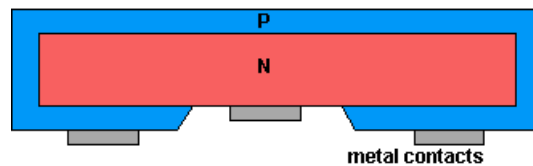


Figure 5.7: Early silicon solar cell structure.

5.1 Cell Fabrication Technologies

5.1.1 Screen Printed Solar Cells

Screen-printed solar cells were first developed in the 1970's. As such, they are the best established, most mature solar cell fabrication technology, and screen-printed solar cells currently dominate the market for terrestrial photovoltaic modules. The key advantage of screen-printing is the relative simplicity of the process. There are a variety of processes for manufacturing screen-printed solar cells. The production technique given in the Figures 5.8, 5.9 and 5.10 is one of the simplest techniques and has since been improved upon by many manufacturers and research laboratories.

There are many variations to the scheme shown above which give higher efficiencies, lower costs or both. Some techniques have already been introduced into commercial production while others are making progress from the labs to the production lines.

1. Phosphorous Diffusion

Screen-printed solar cells typically use a simple homogeneous diffusion to form the emitter where the doping is the same beneath the metal contacts and between the fingers. To maintain low contact resistance, a high surface concentration of phosphorous is required below the screen-printed contact. However, the high surface concentration of phosphorous produces a “dead

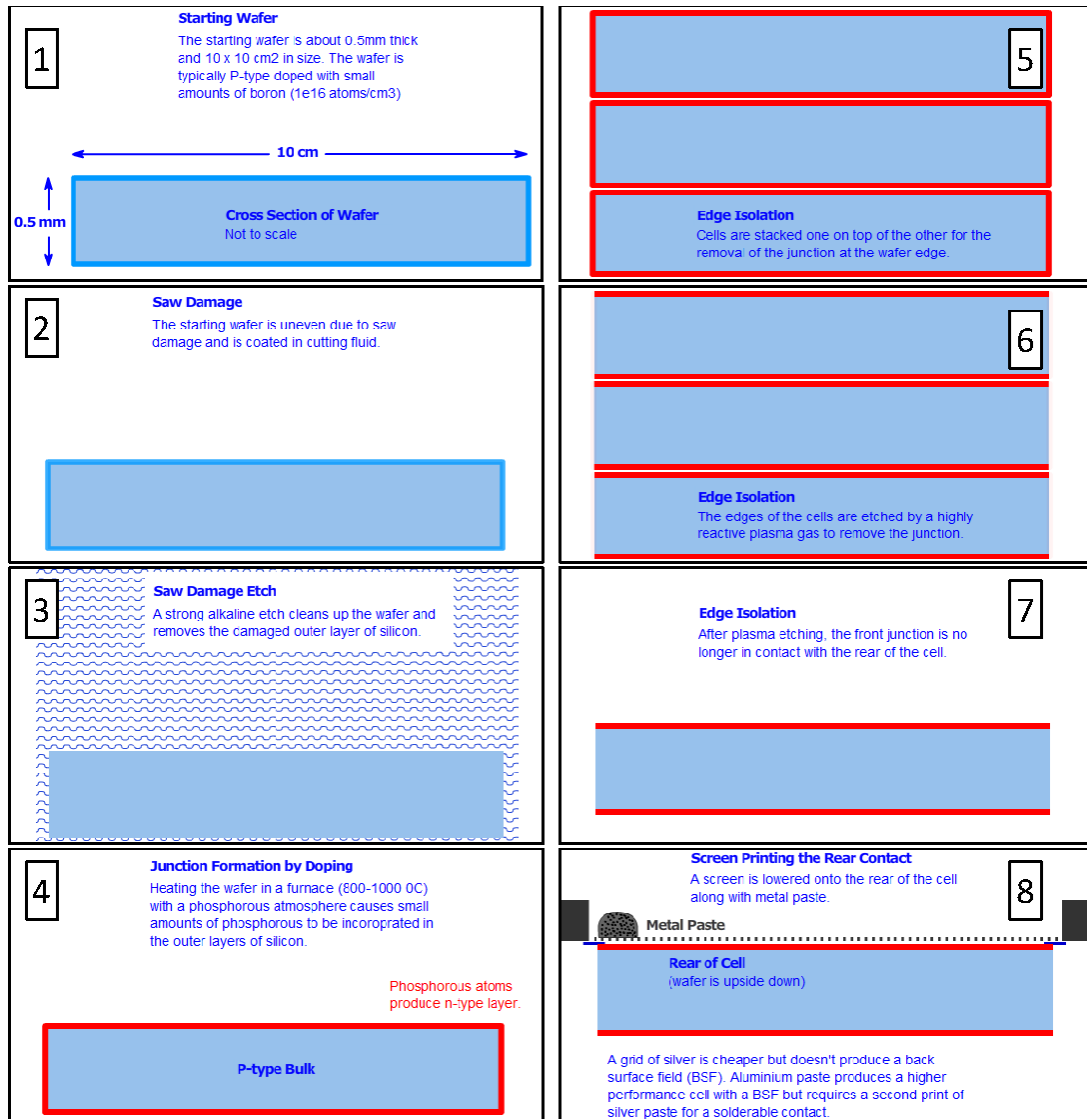


Figure 5.8: A basic technique for fabricating screen printed solar cells (1).

layer” that reduces the cell blue response. Newer cell designs can contact shallower emitters, thus improving the cell blue response. Selective emitters with higher doping below the metal contacts have also been proposed [85], [86] - but none have yet been introduced into commercial production.

2. Surface Texturing to Reduce Reflection

Wafers cut from a single crystal of silicon (monocrystalline material) are easily textured to reduce reflection by etching pyramids on the wafer surface with a chemical solution. While such etching is ideal for monocrystalline CZ wafers, it relies on the correct crystal orientation, and so is only marginally

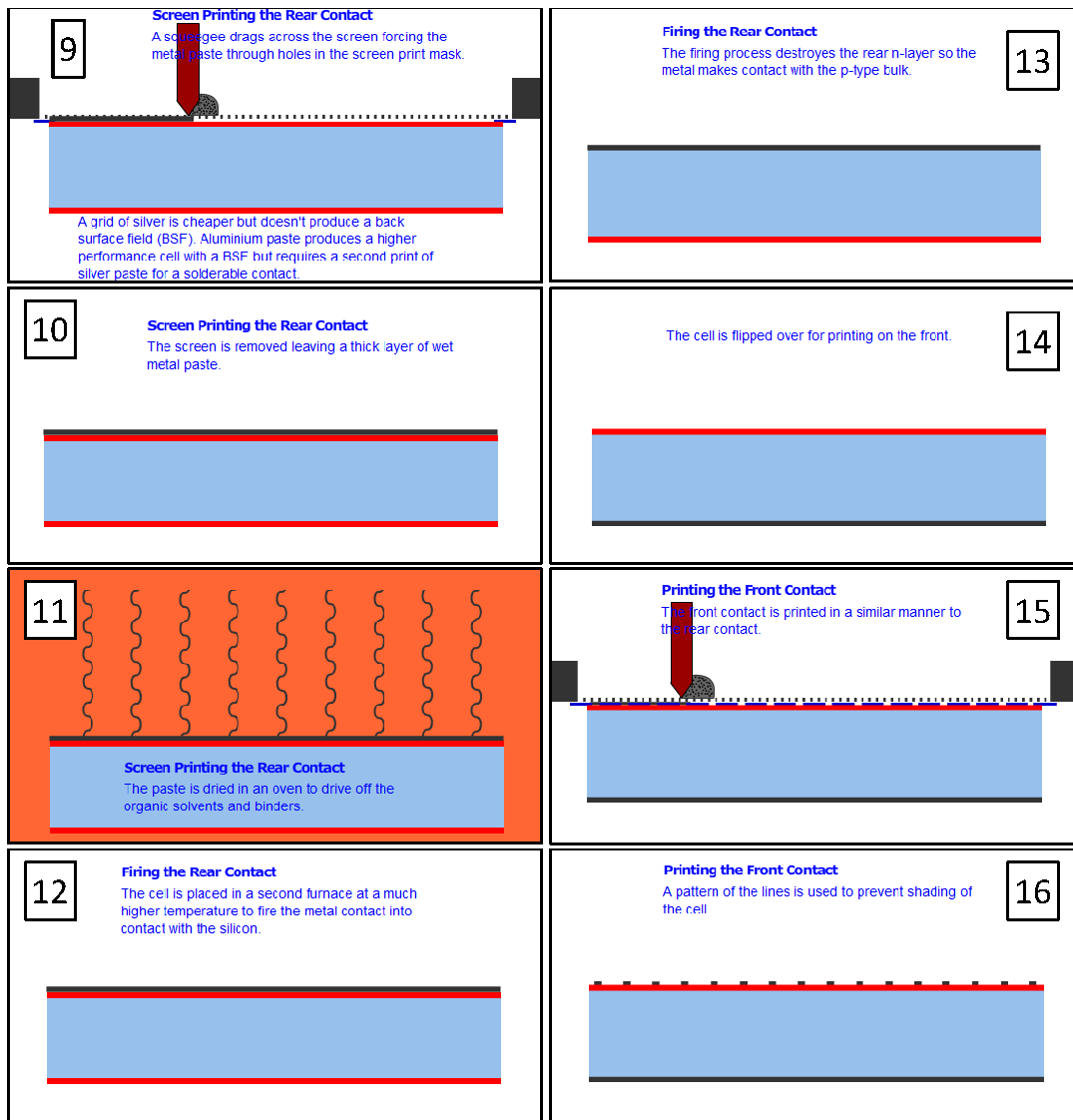


Figure 5.9: A basic technique for fabricating screen printed solar cells (2).

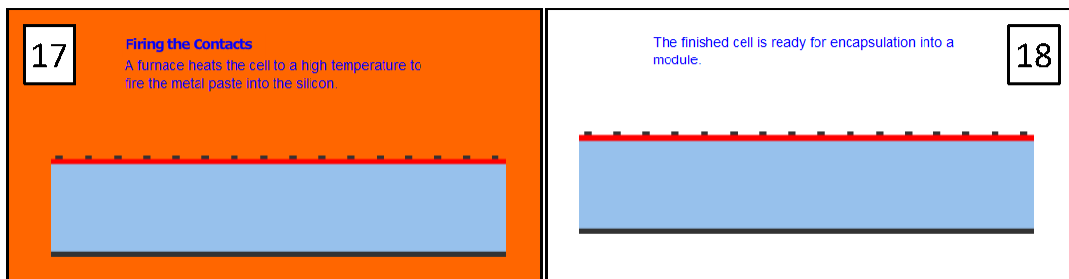


Figure 5.10: A basic technique for fabricating screen printed solar cells (3).

effective on the randomly orientated grains of multicrystalline material. Various schemes have been proposed to texture multicrystalline materials by using one of the following processes:

- (a) mechanical texturing of the wafer surface with cutting tools or lasers [87], [88], [89];
- (b) isotropic chemical etching based on defects rather than crystal orientation [90];
- (c) isotropic chemical etching in combination with a photolithographic mask [91], [92];
- (d) plasma etching [93].

3. Antireflection Coatings and Fire Through Contacts

Antireflection coatings are particularly beneficial for multicrystalline material that cannot be easily textured. Two common antireflection coatings are titanium dioxide (TiO_2) and silicon nitride (SiN_x). The coatings are applied through simple techniques like spraying or chemical vapour deposition. In addition to the optical benefits, dielectric coatings can also improve the electrical properties of the cell by surface passivation. By screen-printing over the antireflection coating with a paste containing cutting agents, the metal contacts can fire through the antireflection coating and bond to the underlying silicon. This process is very simple and has the added advantage of contacting shallower emitters [94].

4. Edge Isolation

There are various techniques for edge isolation such as plasma etching, laser cutting, or masking the border to prevent a diffusion from occurring around the edge in the first place.

5. Rear Contact

A full aluminium layer printed on the rear on the cell, with subsequent alloying through firing, produces a back surface field (BSF) and improves the cell bulk through gettering. However, the aluminium is expensive and a second print of Al/Ag is required for solderable contact. In most production, the rear contact is simply made using a Al/Ag grid printed in a single step.

6. Substrate

Screen-printing has been used on a variety of substrates. The simplicity of the sequence makes screen-printing ideal for poorer quality substrates such as multicrystalline material as well as CZ. The general trend is to move to larger size substrates - up to $15 \times 15 \text{ cm}^2$ for multicrystalline materials and wafers as thin as $200 \mu\text{m}$.

5.1.2 Buried Contact Solar Cells

The buried contact solar cell is a high efficiency commercial solar cell technology based on a plated metal contact inside a laser-formed groove. The buried contact technology overcomes many of the disadvantages associated with screen-printed contacts and this allows buried contact solar cell to have performance up to 25 % better than commercial screen-printed solar cells. A schematic of a buried contact solar cell is shown in the figure 5.11.

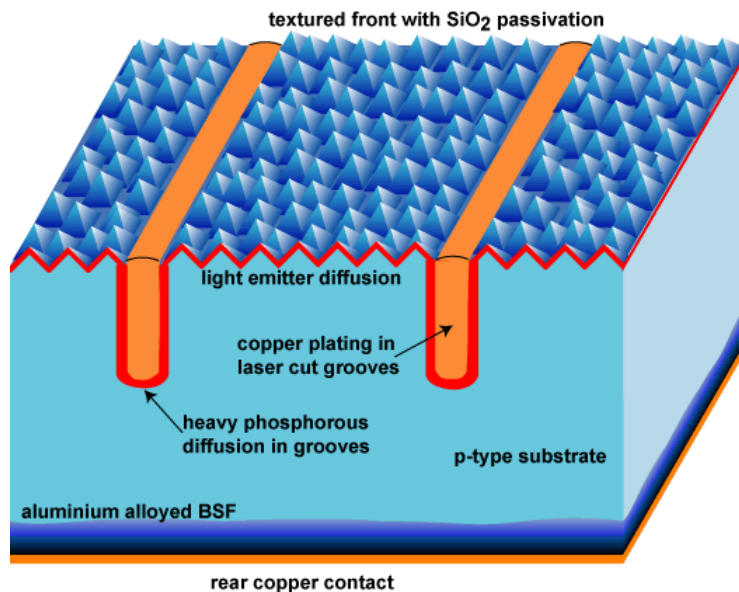


Figure 5.11: Cross-section of Laser Grooved, Buried Contact Solar Cell.

A key high efficiency feature of the buried contact solar cell is that the metal is buried in a laser-formed groove inside the silicon solar cell (Figure 5.12). This allows for a large metal height-to-width aspect ratio. A large metal contact aspect ratio in turn allows a large volume of metal to be used in the contact finger, without having a wide strip of metal on the top surface. Therefore, a high metal aspect ratio allows a large number of closely spaced metal fingers, while still retaining a high transparency. For example, on a large area device, a screen

printed solar cell may have shading losses as high as 10 to 15%, while in a buried contact structure, the shading losses will only be 2 to 3%. These lower shading losses allow low reflection and therefore higher short-circuit currents.

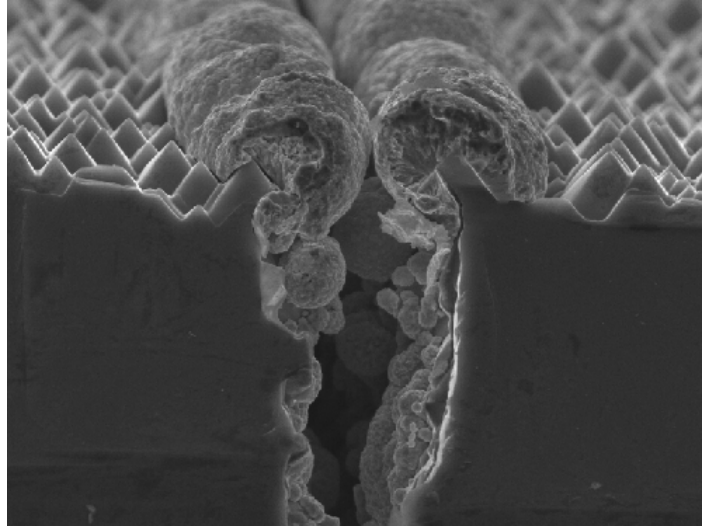


Figure 5.12: Cross section of a partially plated laser groove.

In addition to good reflection properties, the buried contact technology also allows low parasitic resistance losses due to its high metal aspect ratio, its fine finger spacing and its plated metal for the contacts. The emitter resistance is reduced in a buried contact solar cell since a narrower finger spacing dramatically reduces the emitter resistance losses. The metal grid resistance is also low since the finger resistance is reduced by the large volume of metal in the grooves and by the use of copper, which has a lower resistivity than the metal paste used in screen printing. As well, the contact resistance of a buried contact solar cell is lower than that in screen printed solar cells due to the formation of a nickel silicide at the semiconductor-metal interface and the large metal-silicon contact area. Overall, these reduced resistive losses allow large area solar cells with high FFs.

When compared to a screen-printed cell, the metallization scheme of a buried contact solar cell also improves the cell's emitter. To minimize resistive losses, the emitter region of a screen-printed solar cell is very heavily doped and results in a "dead" layer at the surface of the solar cell. Since emitter losses are low in a buried contact structure, the emitter doping can be optimized for high open-circuit voltages and short-circuit currents. Furthermore, a buried contact structure includes a self-aligned, selective emitter, which thereby reduces the

contact recombination and also contributes to high open-circuit voltages.

The efficiency advantages of buried contact technology provide significant cost and performance benefits. In terms of \$/W, the cost of a buried contact solar cell is the same as a screen-printed solar cell [95]. However, due to the inclusion of certain area-related costs as well as fixed costs in a PV system, a higher efficiency solar cell technology results in lower cost electricity. An additional advantage of buried contact technology is that it can be used for concentrator systems [96].

The production sequence for laser grooved buried contact solar cells is shown in the Figures 5.13 and 5.14.

5.1.3 High Efficiency Solar Cells

High efficiency cells cost considerably more to produce than standard silicon cells and are typically used in solar cars or space applications.

Some of the techniques and design features used in the laboratory fabrication of silicon solar cells, to produce the highest possible efficiencies include:

1. lightly phosphorus diffused emitters, to minimise recombination losses and avoid the existence of a “dead layer” at the cell surface;
2. closely spaced metal lines, to minimise emitter lateral resistive power losses;
3. very fine metal lines, typically less than 20 μm wide, to minimise shading losses;
4. polished or lapped surfaces to allow top metal grid patterning via photolithography;
5. small area devices and good metal conductivities, to minimise resistive losses in the metal grid;
6. low metal contact areas and heavy doping at the surface of the silicon beneath the metal contact to minimise recombination;
7. use of elaborate metallization schemes, such as titanium/palladium/silver, that give very low contact resistances;
8. good rear surface passivation, to reduce recombination;
9. use of anti-reflection coatings, which can reduce surface reflection from 30% to well below 10%.

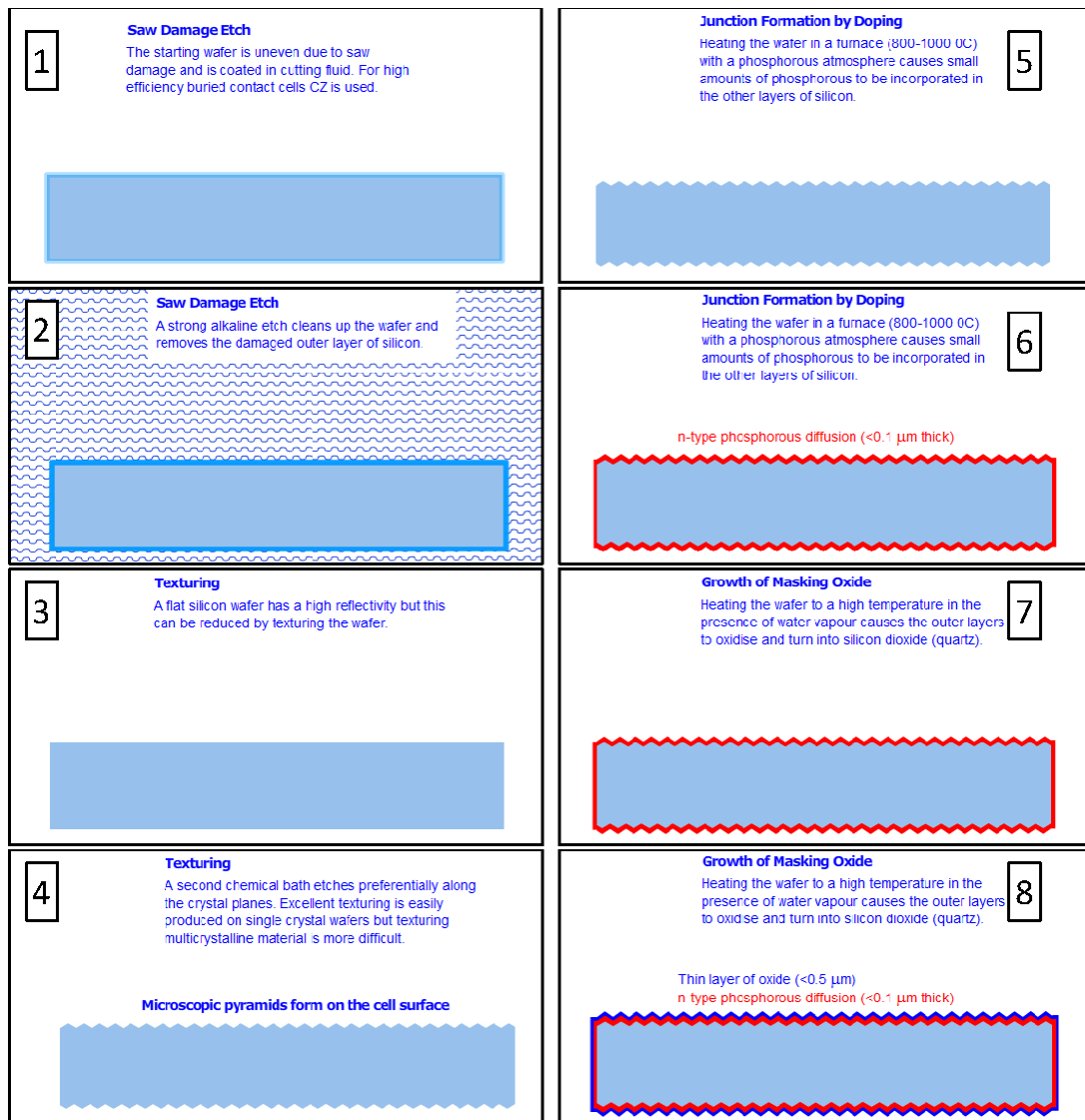


Figure 5.13: Figure showing the manufacture of a buried contact solar cell. The cell thickness is greatly enlarged for clarity. (1)

A number of cell designs exist which incorporate advanced laboratory features. Two approaches that have been used by niche markets such as solar cars are the PERL cells produced at University of New South Wales, and the rear-contact cells developed at Stanford University and SunPower.

PERL Solar Cells

The passivated emitter with rear locally diffused (PERL) cell uses micro-electronic techniques to produce cells with efficiencies approaching 25% under the standard

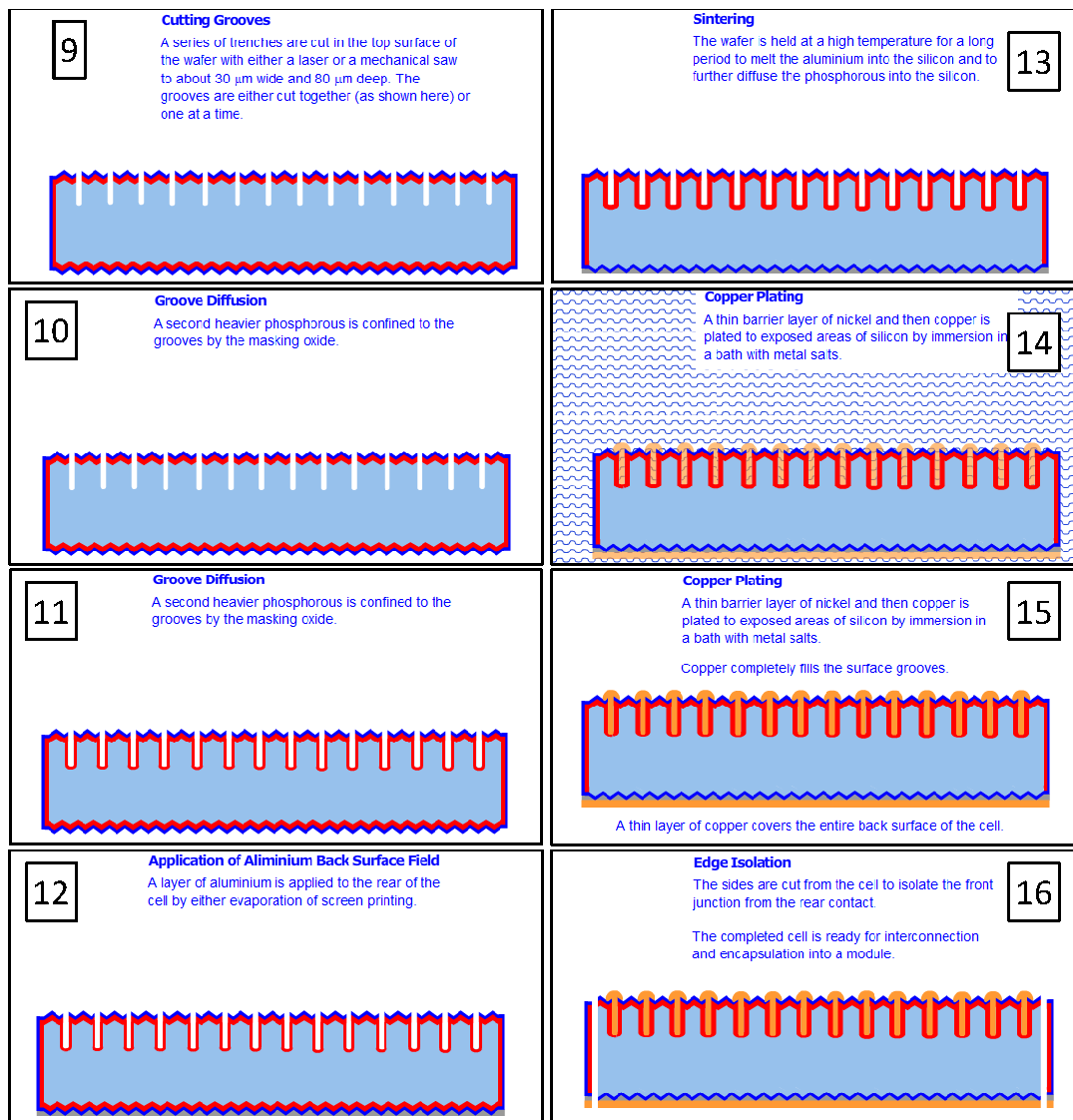


Figure 5.14: Figure showing the manufacture of a buried contact solar cell. The cell thickness is greatly enlarged for clarity. (2)

AM1.5 spectrum. The passivated emitter refers to the high quality oxide at the front surface that significantly lowers the number of carriers recombining at the surface. The rear is *locally diffused* only at the metal contacts to minimise recombination at the rear while maintaining good electrical contact (Figures 5.15 and 5.16).

While expensive to fabricate, it is possible to produce cells with very high efficiencies. A cell for a solar car had the following characteristics (Figure 5.17):

- Area: 22 cm^2

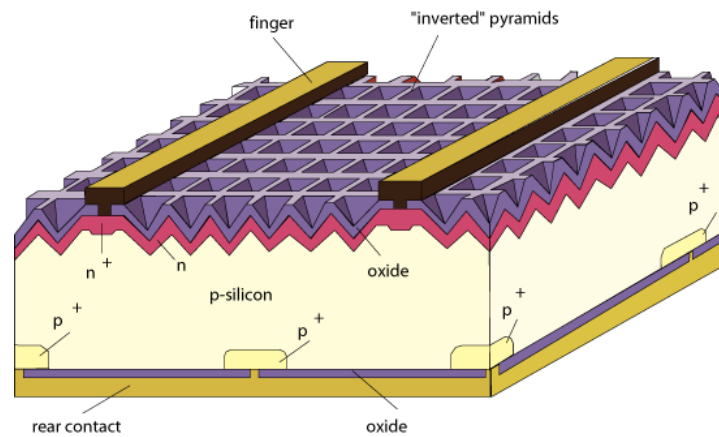


Figure 5.15: Schematic of high efficiency laboratory cell.

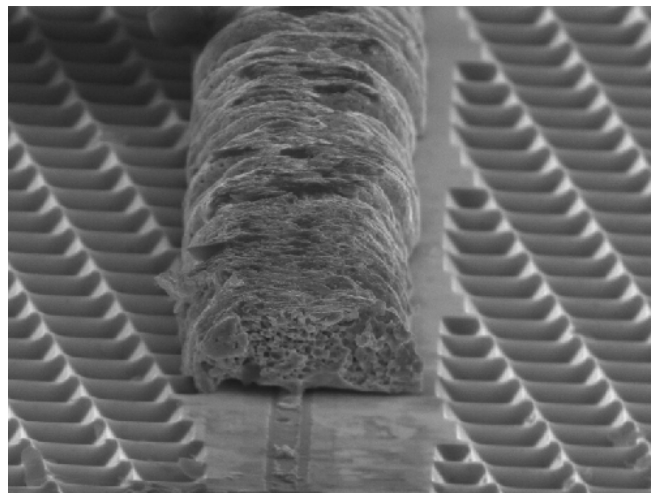


Figure 5.16: Electron microscope image of the top surface of a PERL Cell showing a broken electroplated finger. The total finger width is less than $20 \mu m$ and the contact width is $> 3 \mu m$.

- Efficiency: 23.5%
- V_{OC} : 703 mV
- I_{SC} : 914 mA
- J_{SC} : 41.3 mA
- V_{MP} : 600 mV
- I_{MP} : 868 mA
- FF : 0.81

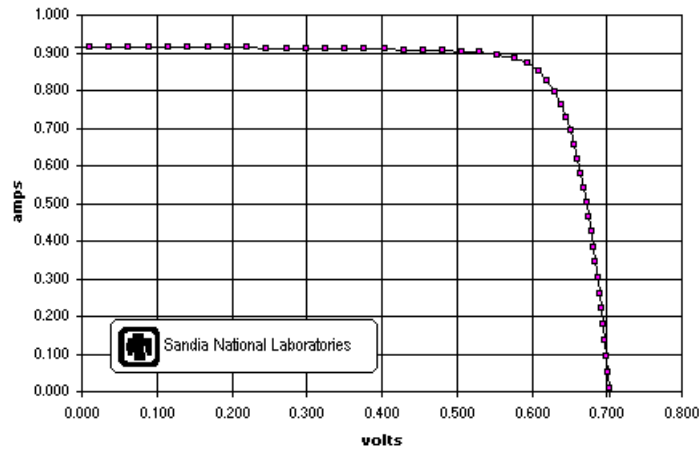


Figure 5.17: IV curve for a solar car cell.

5.1.4 Rear Contact Solar Cells

Rear contact solar cells achieve potentially higher efficiency by moving all or part of the front contact grids to the rear of the device. The higher efficiency potentially results from the reduced shading on the front of the cell and is especially useful in high current cells such as concentrators or large areas. There are several configurations.

Interdigitated back contact solar cells (IBC)

Rear contact solar cells eliminate shading losses altogether by putting both contacts on the rear of the cell (Figure 5.18). By using a thin solar cell made from high quality material, electron-hole pairs generated by light that is absorbed at the front surface can still be collected at the rear of the cell [97]. Such cells are especially useful in concentrator applications where the effect of cell series resistance is greater.

An additional benefit is that cells with both contacts on the rear are easier to interconnect and can be placed closer together in the module since there is no need for a space between the cells.

Metalization wrap through (MWT)

One possible way of increasing the conversion efficiency is to consider the MWT solar cell designs which, compared to conventional cells, requires only a couple of steps more in the manufacturing process and the use of a laser. Through this technology it has been demonstrated an absolute increase in the efficiency of

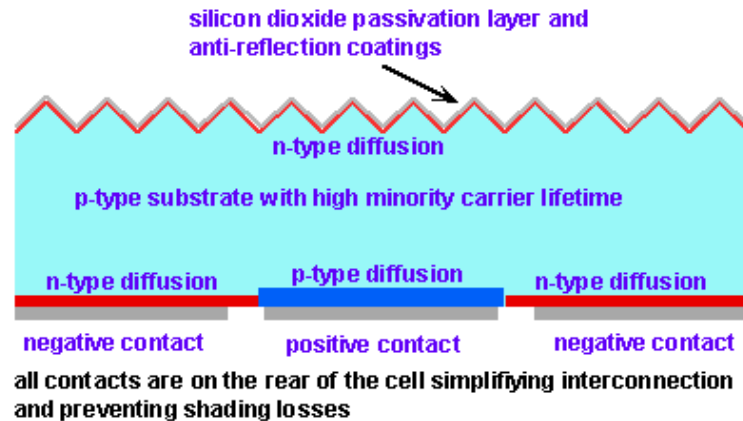


Figure 5.18: Back Contact Solar Cell as used in commercial production.

about 0.5% at 1 sun [98]; a section of this type of cell is reported in Figure 5.19, where we note the main feature of this model: both polarity (n and p contacts) are located in the rear of the cell. In addition, the electrical isolation between the two contacts is obtained by a diffusion barrier exactly located between the two opposite poles. An evolution of the MWT design are the so-called MWT-PERC

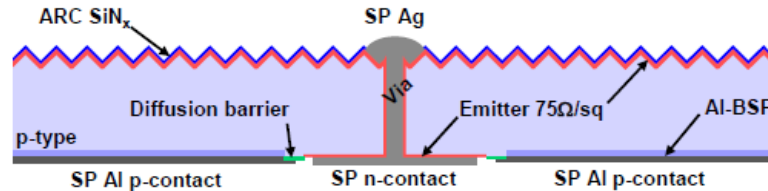


Figure 5.19: Section of a MWT solar cell.

(figure 5.20), which combines the two types of cells, entering further processing to the back of the cell to improve their characteristics. The implementation of the back surface passivation in combination with an optimized internal structure increases the cell efficiency, especially if thinner wafers are utilized. The gain of the PERC cells compared to standard cells is already been considered and confirmed [99].

5.2 Design of Silicon Solar Cell

Solar cell design involves specifying the parameters of a solar cell structure in order to maximize efficiency, given a certain set of constraints. These constraints will be defined by the working environment in which solar cells are produced. For

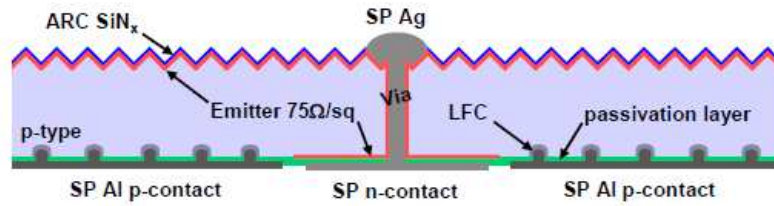


Figure 5.20: Section of a MWT-PERC solar cell.

example in a commercial environment where the objective is to produce a competitively priced solar cell, the cost of fabricating a particular solar cell structure must be taken into consideration. However, in a research environment where the objective is to produce a highly efficient laboratory-type cell, maximizing efficiency rather than cost, is the main consideration.

The theoretical efficiency for photovoltaic conversion is in excess of 86.8% [100]. However, the 86.8% figure uses detailed balance calculations and does not describe device implementation. For silicon solar cells, a more realistic efficiency under one sun operation is about 29% [101]. The maximum efficiency measured for a silicon solar cell was 24.7% under AM1.5G at the end of the last century (Figure 5.21). The difference between the high theoretical efficiencies and the efficiencies measured from terrestrial solar cells is due mainly to two factors. The first is that the theoretical maximum efficiency predictions assume that energy from each photon is optimally used, that there are no unabsorbed photons and that each photon is absorbed in a material which has a band gap equal to the photon energy. This is achieved in theory by modeling an infinite stack of solar cells of different band gap materials, each absorbing only the photons which correspond exactly to its band gap.

The second factor is that the high theoretical efficiency predictions assume a high concentration ratio. Assuming that temperature and resistive effects do not dominate in a concentrator solar cell, increasing the light intensity proportionally increases the short-circuit current. Since the open-circuit voltage (V_{OC}) also depends on the short-circuit current, V_{OC} increases logarithmically with light level. Furthermore, since the maximum fill factor (FF) increases with V_{OC} , the maximum possible FF also increases with concentration. The extra V_{OC} and FF increases with concentration which allows concentrators to achieve higher efficiencies.

In designing such single junction solar cells, the principles for maximizing cell efficiency are:

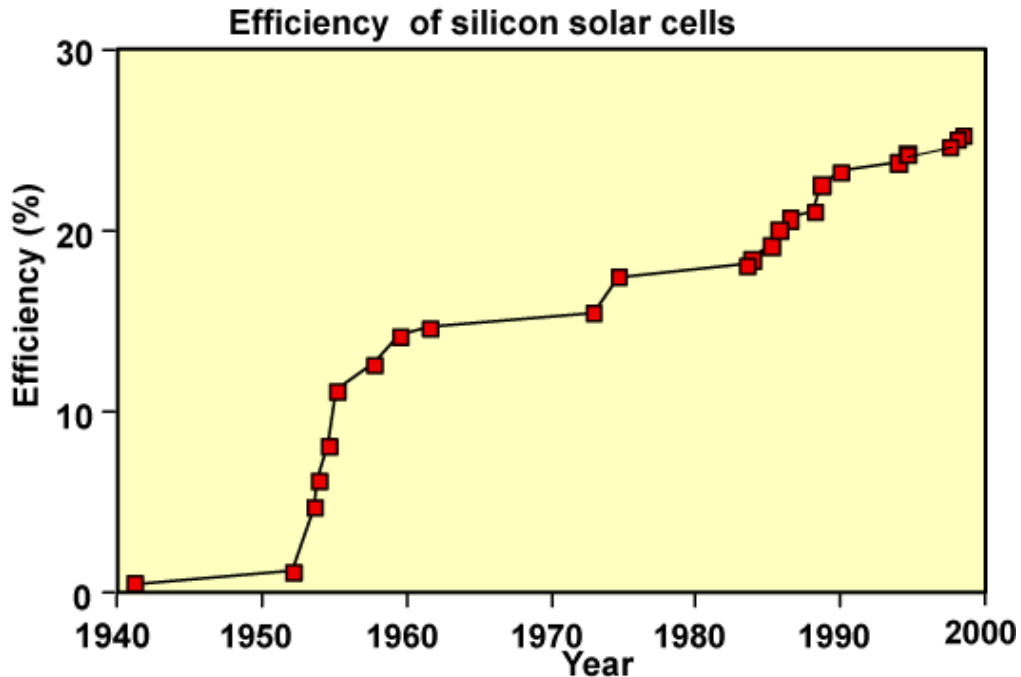


Figure 5.21: Evolution of silicon solar cell efficiency.

- increasing the amount of light collected by the cell that is turned into carriers;
- increasing the collection of light-generated carriers by the p-n junction;
- minimising the forward bias dark current;
- extracting the current from the cell without resistive losses.

5.2.1 Optical Properties

Optical Losses

Optical losses chiefly effect the power from a solar cell by lowering the short-circuit current. Optical losses consist of light which could have generated an electron-hole pair, but does not, because the light is reflected from the front surface, or because it is not absorbed in the solar cell (Figure 5.22). For the most common semiconductor solar cells, the entire visible spectrum (350 - 780 nm) has enough energy to create electron-hole pairs and therefore all visible light would ideally be absorbed.

There are a number of ways to reduce the optical losses:

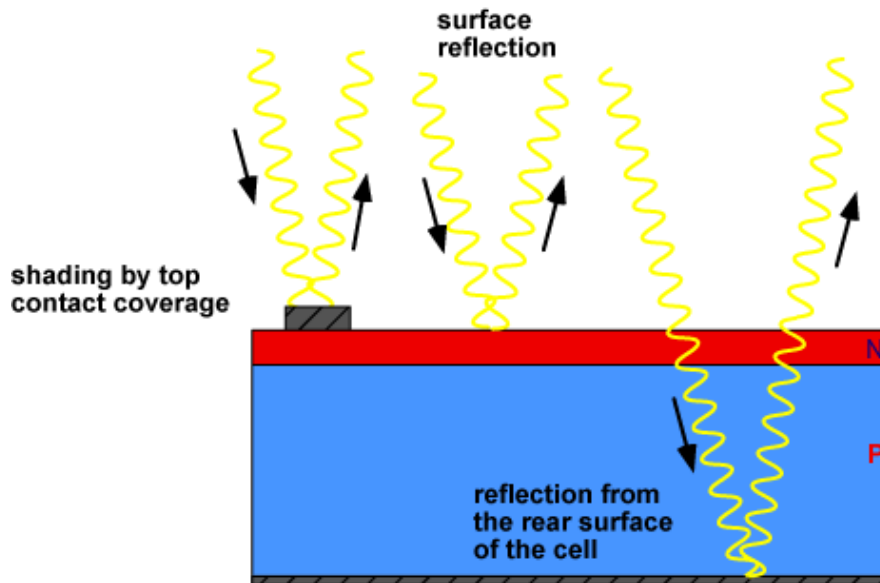


Figure 5.22: Sources of optical loss in a solar cell.

- Top contact coverage of the cell surface can be minimized (although this may result in increased series resistance). This is discussed in more detail in Series Resistance;
- Anti-reflection coatings can be used on the top surface of the cell;
- Reflection can be reduced by surface texturing;
- The solar cell can be made thicker to increase absorption (although light that is absorbed more than a diffusion length from the junction has a low collection probability and will not contribute to the short circuit current);
- The optical path length in the solar cell may be increased by a combination of surface texturing and light trapping.

The reflection of a silicon surface is over 30% due to its high refractive index. The reflectivity, R , between two materials of different refractive indices is determined by:

$$R = \left(\frac{n_0 - n_{Si}}{n_0 + n_{Si}} \right)^2 \quad (5.1)$$

where n_0 is the refractive index of the surroundings and n_{Si} is the complex refractive index of silicon. For an unencapsulated cell $n_0 = 1$. For an encapsulated cell $n_0 = 1.5$. The refractive index of silicon changes with wavelength.

Anti-Reflection Coatings

Bare silicon has a high surface reflection of over 30%. The reflection is reduced by texturing and and by applying anti-reflection coatings (ARC) to the surface [102]. Anti-reflection coatings on solar cells are similar to those used on other optical equipment such as camera lenses. They consist of a thin layer of dielectric material, with a specially chosen thickness so that interference effects in the coating cause the wave reflected from the anti-reflection coating top surface to be out of phase with the wave reflected from the semiconductor surfaces. These out-of-phase reflected waves destructively interfere with one another, resulting in zero net reflected energy (Figure 5.23). In addition to anti-reflection coatings, interference effects are also commonly encountered when a thin layer of oil on water produces rainbow-like bands of color.

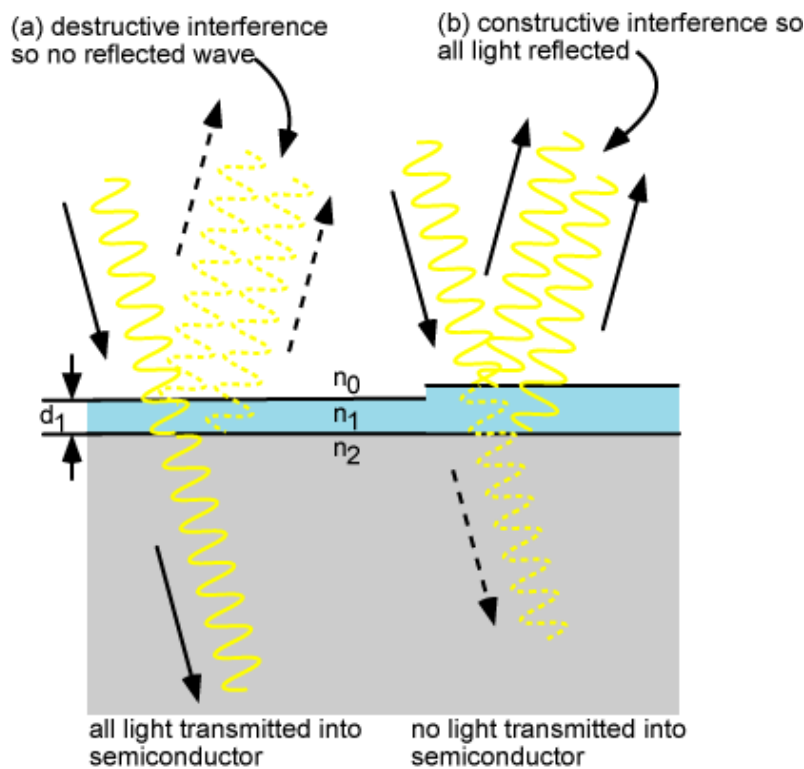


Figure 5.23: Use of a quarter wavelength anti-reflection coating to counter surface reflection.

The thickness of the anti-reflection coating is chosen so that the wavelength in the dielectric material is one quarter the wavelength of the incoming wave. For a quarter wavelength anti-reflection coating of a transparent material with a refractive index n_1 and light incident on the coating with a free-space wavelength

λ_0 , the thickness d_1 which causes minimum reflection is calculated by:

$$d_1 = \frac{\lambda_0}{4n_1} \quad (5.2)$$

Reflection is further minimized if the refractive index of the anti-reflection coating is the geometric mean of that of the materials on either side; that is, glass or air and the semiconductor. This is expressed by:

$$n_1 = \sqrt{n_0 n_2} \quad (5.3)$$

For the reflectance at normal incidence we define a series of parameters: r_1 , r_2 , and θ . The surrounding region has a refractive index of n_0 , the ARC has a refractive index of n_1 and a thickness of t_1 , and the silicon has a refractive index of n_2 .

$$r_1 = \frac{n_0 - n_1}{n_0 + n_1} \quad (5.4)$$

$$r_2 = \frac{n_1 - n_2}{n_1 + n_2} \quad (5.5)$$

$$\theta = \frac{2\pi n_1 t_1}{\lambda} \quad (5.6)$$

For a single layer ARC on a substrate the reflectivity is:

$$R = |r^2| = \frac{r_1^2 + r_2^2 + 2r_1 r_2 \cos(2\theta)}{1 + r_1^2 r_2^2 + 2r_1 r_2 \cos(2\theta)} \quad (5.7)$$

An example is shown in Figure 5.24.

While the reflection for a given thickness, index of refraction, and wavelength can be reduced to zero using the equations above, the index of refraction is dependent on wavelength and so zero reflection occurs only at a single wavelength. For photovoltaic applications, the refractive index, and thickness are chosen in order to minimize reflection for a wavelength of $0.6\mu\text{m}$. This wavelength is chosen since it is close to the peak power of the solar spectrum (Figure 5.25).

Double Layer Anti Reflection Coatings

A further reduction in reflectivity is achieved through a double layer anti-reflection coating (DLARC)(Figure 5.26). Popular DLARC coatings are zinc sulfide (ZnS) with magnesium flouride (MgF) or layers of silicon nitride with varying refractive index. However, this is usually too expensive for most commercial solar cells.

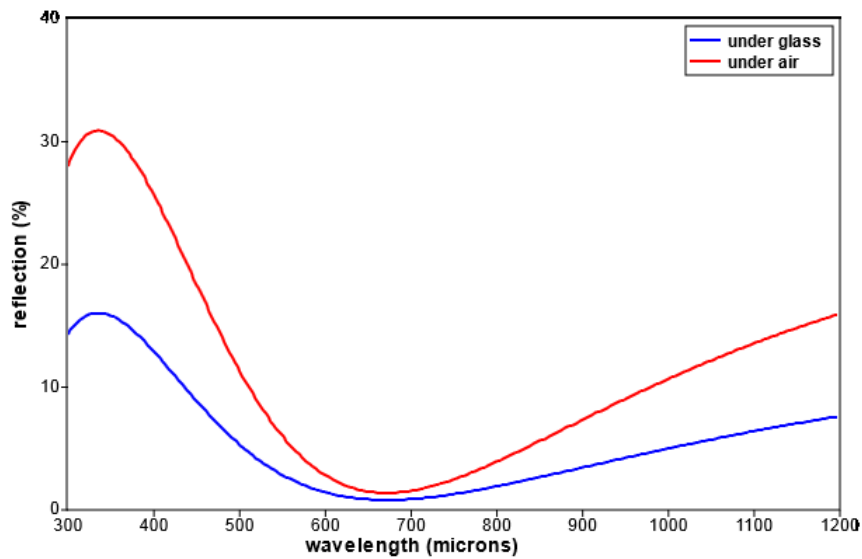


Figure 5.24: Effect of a single layer anti-reflection coating on silicon ($n = 2.1$ and $t_1 = 80nm$). For simplicity this simulation assumes a constant refractive index for silicon at 3.5.

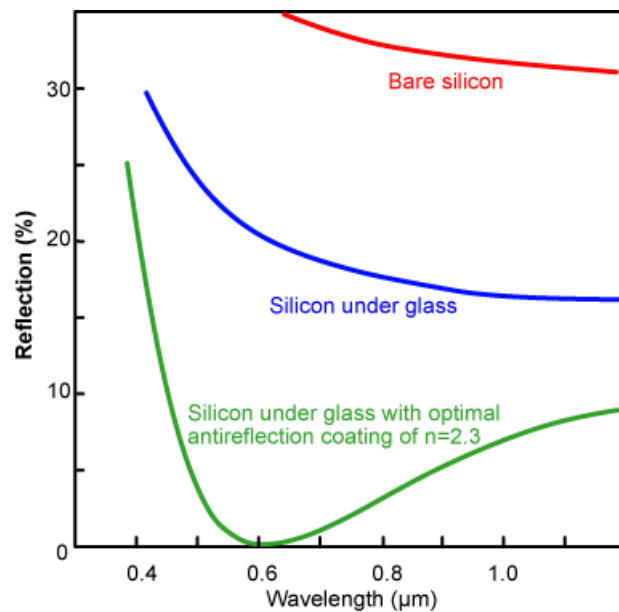


Figure 5.25: Comparison of surface reflection from a silicon solar cell, with and without a typical anti-reflection coating.

The equations for multiple anti-reflection coatings are more complicated than that for a single layer [103]. First we define a series of parameters: r_1 , r_2 , r_3 , θ_1 and θ_2 . As in the diagram above, the surrounding region has a refractive index

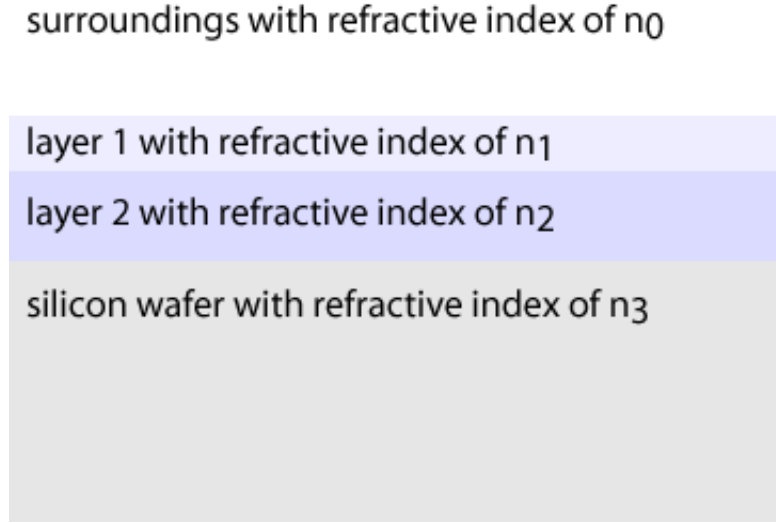


Figure 5.26: Double layer anti-reflection film on silicon wafer. The layers are usually deposited on a textured substrate to decrease the reflectivity further.

of n_0 , the next layer has a refractive index of n_1 and a thickness of t_1 , the layer immediately above the silicon has a refractive index of n_2 and a thickness of t_2 and the silicon has a refractive index of n_3 .

$$r_1 = \frac{n_0 - n_1}{n_0 + n_1} \quad (5.8)$$

$$r_2 = \frac{n_1 - n_2}{n_1 + n_2} \quad (5.9)$$

$$r_3 = \frac{n_2 - n_3}{n_2 + n_3} \quad (5.10)$$

$$\theta_1 = \frac{2\pi n_1 t_1}{\lambda} \quad (5.11)$$

$$\theta_2 = \frac{2\pi n_2 t_2}{\lambda} \quad (5.12)$$

The reflectivity is then calculated from the above parameters using the following formula:

$$R = |r^2| = \frac{r_1^2 + r_2^2 + r_3^2 + r_1^2 r_2^2 r_3^2 + 2r_1 r_2 (1 + r_3^2) \cos(2\theta_1) + 2r_2 r_3 (1 + r_1^2) \cos(2\theta_2) + 2r_1 r_3 \cos(2(\theta_1 + \theta_2)) + 2r_1 r_2 r_3 \cos(2(\theta_1 - \theta_2))}{1 + r_1^2 r_2^2 + r_1^2 r_3^2 + r_2^2 r_3^2 + 2r_1 r_2 (1 + r_3^2) \cos(2\theta_1) + 2r_2 r_3 (1 + r_1^2) \cos(2\theta_2) + 2r_1 r_3 \cos(2(\theta_1 + \theta_2)) + 2r_1 r_2 r_3 \cos(2(\theta_1 - \theta_2))} \quad (5.13)$$

The Figure 5.27 simulates a double layer antireflection coating. By adjusting the refractive index and thickness of the two layers it is possible to produce two minima and a overall reflectance of less than 3%.

Further reductions in reflectivity can be achieved with stacks of coatings or by grading the index of the layers. In the optical industry stacks of over 10 layers

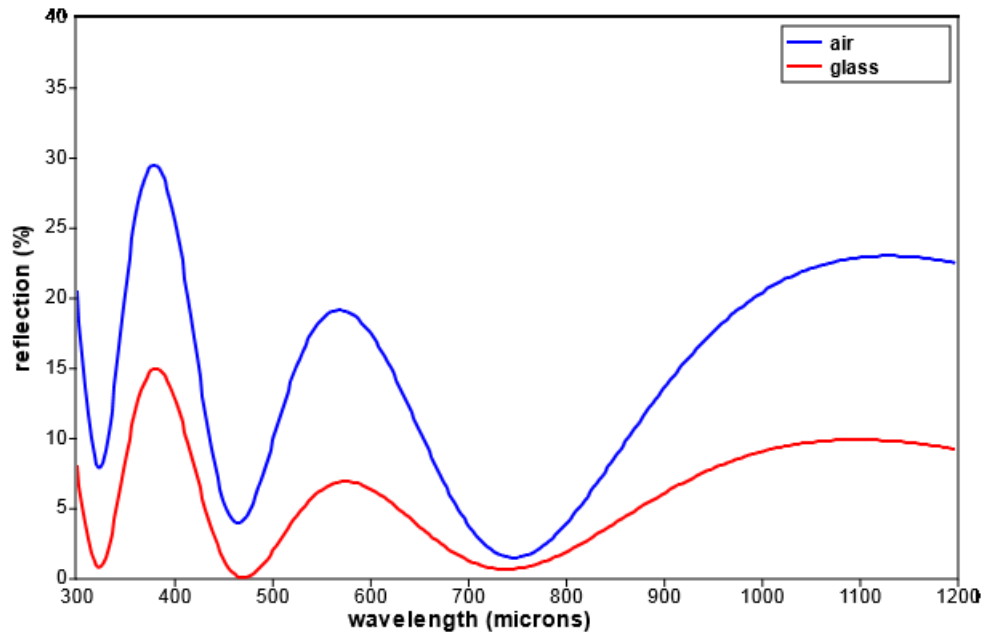


Figure 5.27: Effect of thickness and refractive index on a double layer anti-reflection coating (DLARC). Parameters: $n_1 = 2.1$, $t_1 = 80$ nm, $n_2 = 2.5$ and $t_2 = 160$ nm

are used for very low reflection losses in photographic equipment. However, the performance benefits of multiple layers are marginal. In most cases the real challenge is to incorporate the anti-reflection coatings in with the surface passivation layers.

OPAL2 [104] at pvlighthouse.com.au provides a simulator for multilayer stacks. It uses concepts similar to what is presented on these pages but has much more complete mathematical models including the effect of refractive index as a function of wavelength.

Surface Texturing

Surface texturing, either in combination with an anti-reflection coating or by itself, can also be used to minimise reflection (Figure 5.28). Any “roughening” of the surface reduces reflection by increasing the chances of reflected light bouncing back onto the surface, rather than out to the surrounding air [105].

Surface texturing can be accomplished in a number of ways. A single crystalline substrate can be textured by etching along the faces of the crystal planes. The crystalline structure of silicon results in a surface made up of pyramids if the surface is appropriately aligned with respect to the internal atoms. One such

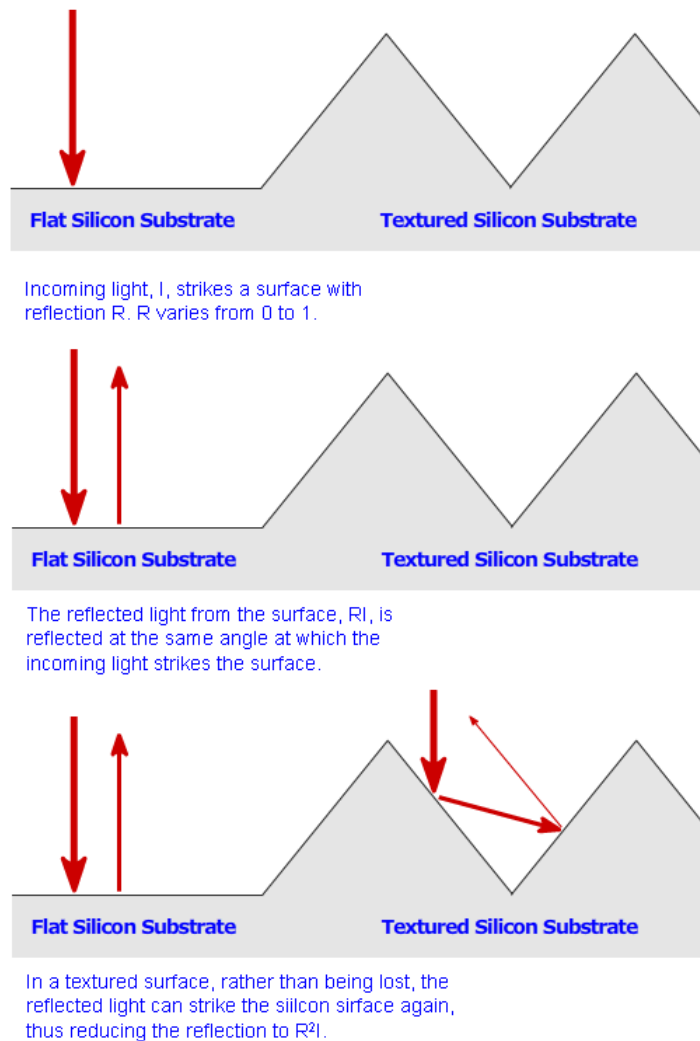


Figure 5.28: Effect of texturing: the light reflected is minimized by multiple scattering.

pyramid is illustrated in the Figure 5.29. An electron microscope photograph of a textured silicon surface is shown in the Figure 5.30. This type of texturing is called “random pyramid” texture [106], and is commonly used in industry for single crystalline wafers.

Another type of surface texturing used is known as “inverted pyramid” texturing [107] and [108]. Using this texturing scheme, the pyramids are etched down into the silicon surface rather than etched pointing upwards from the surface. A photograph of such a textured surface is shown in Figure 5.31.

For multicrystalline wafers, only a small fraction of the surface will have the required orientation of $\langle 111 \rangle$ and consequently these techniques are less effec-

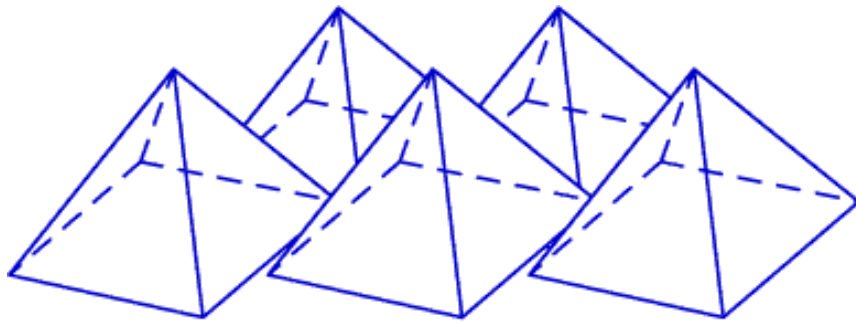


Figure 5.29: A square based pyramid which forms the surface of an appropriately textured crystalline silicon solar cell.

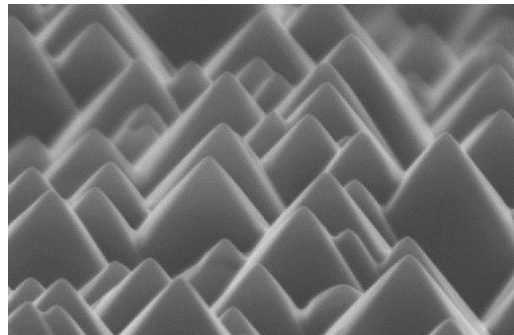


Figure 5.30: Scanning electron microscope photograph of a textured silicon surface. Image Courtesy of The School of Photovoltaic & Renewable Energy Engineering, University of New South Wales.

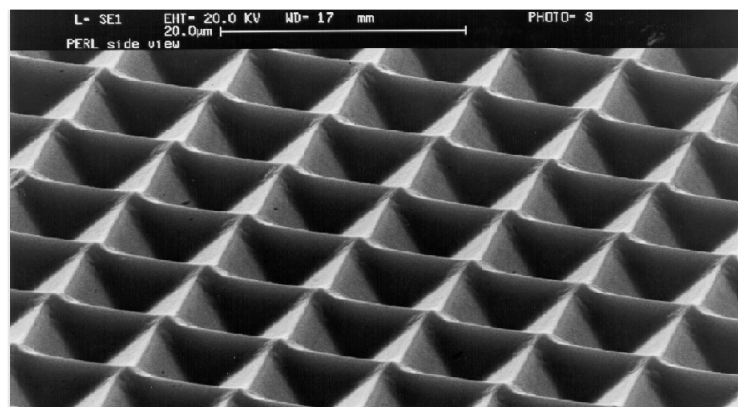


Figure 5.31: Scanning electron microscope photograph of a textured silicon surface. Image Courtesy of The School of Photovoltaic & Renewable Energy Engineering, University of New South Wales.

tive on multicrystalline wafers. However, multicrystalline wafers can be textured using a photolithographic technique [109] as well as mechanically sculpting the front surface using dicing saws [110] or lasers [111] to cut the surface into an appropriate shape. A micrograph of a photolithographic texturing scheme is shown in Figure 5.32.

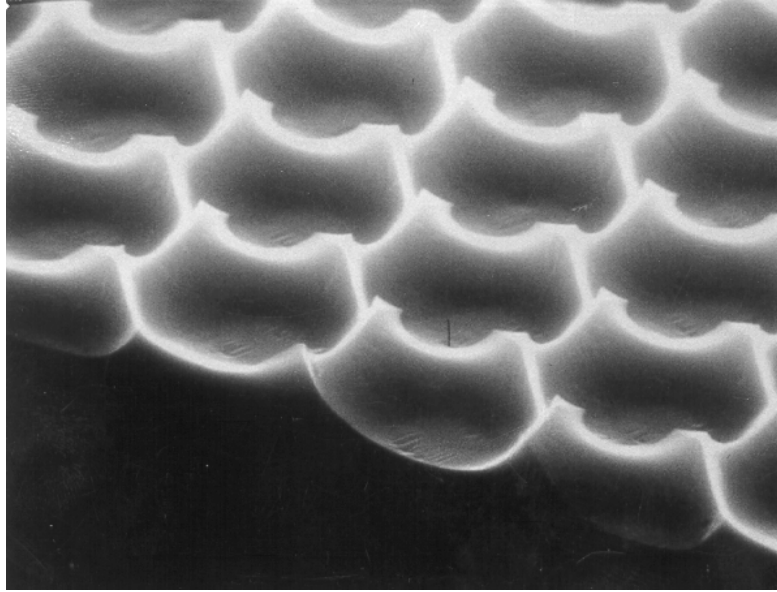


Figure 5.32: Scanning electron microscope photograph of a textured silicon surface. Image Courtesy of The School of Photovoltaic & Renewable Energy Engineering, University of New South Wales.

5.2.2 Reducing Recombination

Recombination Losses

Recombination losses effect both the current collection (and therefore the short-circuit current) as well as the forward bias injection current (and therefore the open-circuit voltage). Recombination is frequently classified according to the region of the cell in which it occurs. Typically, recombination at the surface (surface recombination) or in the bulk of the solar cell (bulk recombination) are the main areas of recombination. The depletion region is another area in which recombination can occur (depletion region recombination). Bulk and surface recombination are shown in the Figure 5.33.

In order for the p-n junction to be able to collect all of the light-generated carriers, both surface and bulk recombination must be minimised. In silicon solar

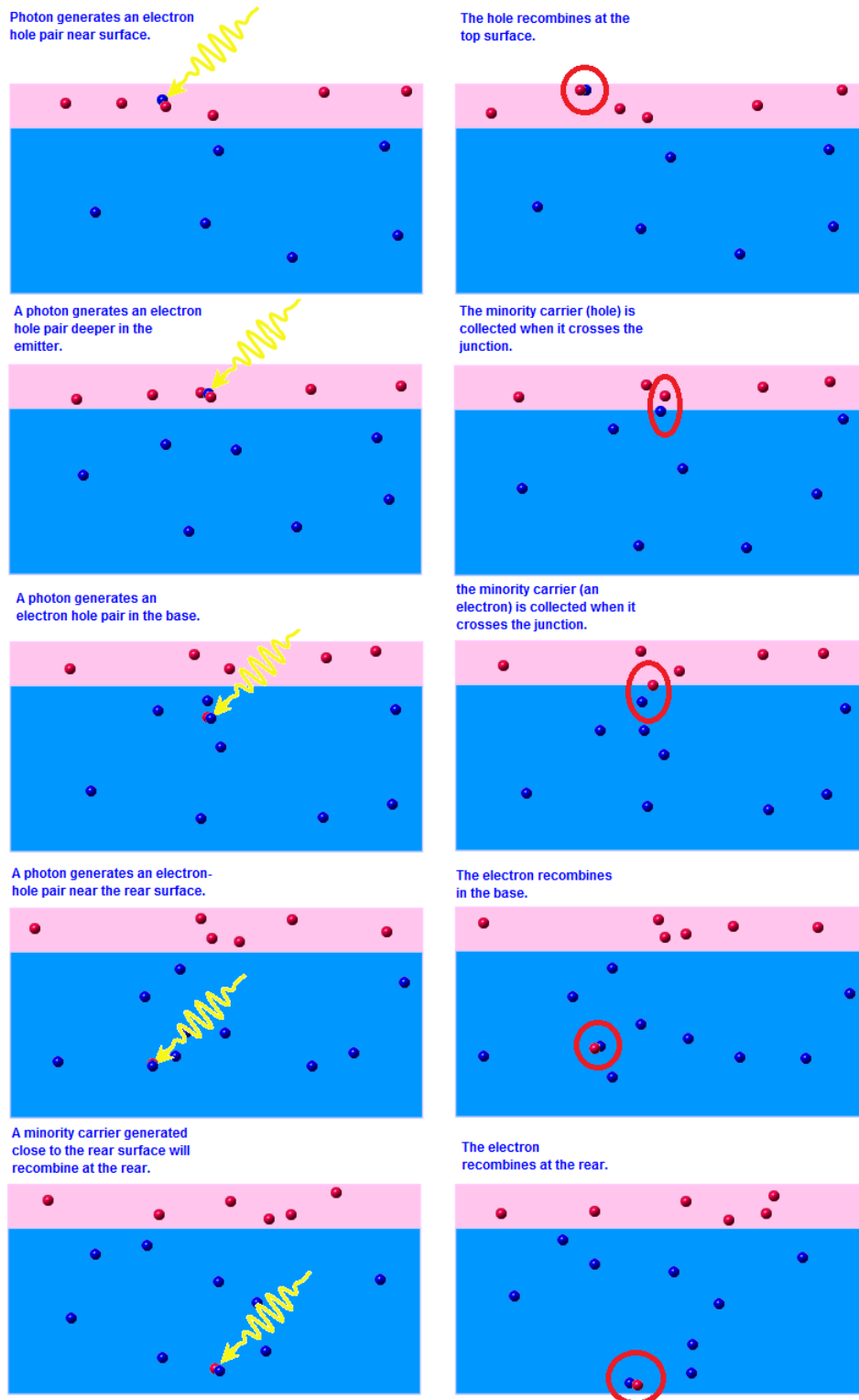


Figure 5.33: Types of recombination in silicon solar cell.

cells, the two conditions commonly required for such current collection are:

1. The carrier must be generated within a diffusion length of the junction, so that it will be able to diffuse to the junction before recombining;
2. In the case of a localized high recombination site (such as at an unpassivated surface or at a grain boundary in multicrystalline devices), the carrier must be generated closer to the junction than to the recombination site. For less severe localized recombination sites, (such as a passivated surface), carriers can be generated closer to the recombination site while still being able to diffuse to the junction and be collected without recombining.

The presence of localized recombination sites at both the front and the rear surfaces of a silicon solar cell means that photons of different energy will have different collection probabilities. Since blue light has a high absorption coefficient and is absorbed very close to the front surface, it is not likely to generate minority carriers that can be collected by the junction if the front surface is a site of high recombination. Similarly, a high rear surface recombination will primarily affect carriers generated by infrared light, which can generate carriers deep in the device. The quantum efficiency of a solar cell quantifies the effect of recombination on the light generation current. The quantum efficiency of a silicon solar cell is shown in Figure 5.34.

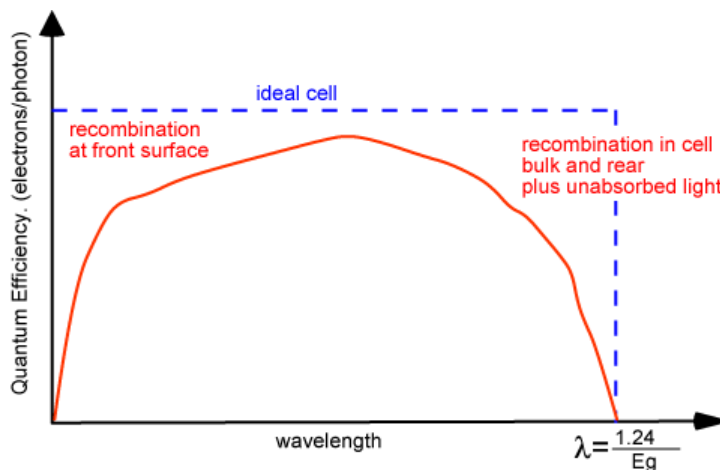


Figure 5.34: Typical quantum efficiency in an ideal and actual solar cell, illustrating the impact of optical and recombination losses.

The open-circuit voltage is the voltage at which the forward bias diffusion current is exactly equal to the short circuit current. The forward bias diffusion current is dependent on the amount recombination in a p-n junction and

increasing the recombination increases the forward bias current. Consequently, high recombination increases the forward bias diffusion current, which in turn reduces the open-circuit voltage. The material parameter which gives the recombination in forward bias is the diode saturation current. The recombination is controlled by the number of minority carriers at the junction edge, how fast they move away from the junction and how quickly they recombine. Consequently, the dark forward bias current, and hence the open-circuit voltage is affected by the following parameters:

1. *The number of minority carriers at the junction edge.* The number of minority carriers injected from the other side is simply the number of minority carriers in equilibrium multiplied by an exponential factor which depends on the voltage and the temperature. Therefore, minimising the equilibrium minority carrier concentration reduces recombination. Minimizing the equilibrium carrier concentration is achieved by **increasing the doping**;
2. *The diffusion length in the material.* A low diffusion length means that minority carriers disappear from the junction edge quickly due to recombination, thus allowing more carriers to cross and increasing the forward bias current. Consequently, to minimise recombination and achieve a high voltage, a **high diffusion length is required**. The diffusion length depends on the types of material, the processing history of the wafer and the doping in the wafer. High doping reduces the diffusion length, thus introducing a trade-off between maintaining a high diffusion length (which affects both the current and voltage) and achieving a high voltage;
3. *The presence of localized recombination sources within a diffusion length of the junction.* A high recombination source close to the junction (usually a surface or a grain boundary) will allow carriers to move to this recombination source very quickly and recombine, thus dramatically increasing the recombination current. The impact of surface recombination is reduced by **passivating the surfaces**.

The net effect of previous trade-offs is shown in the Figure 5.35.

Surface Recombination

Surface recombination can have a major impact both on the short-circuit current and on the open-circuit voltage. High recombination rates at the top surface have

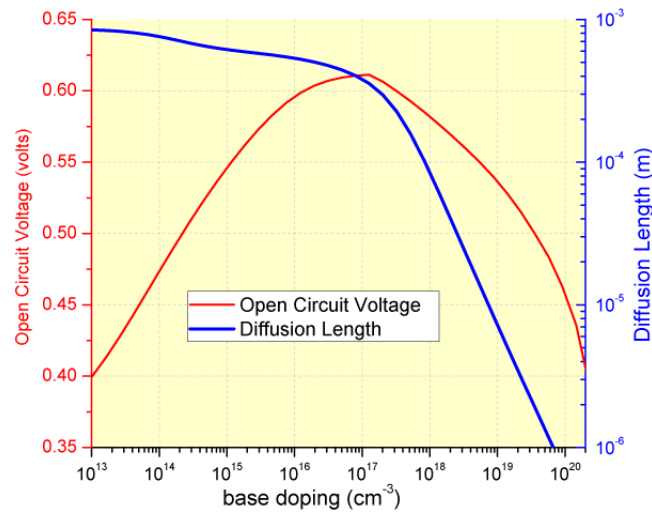


Figure 5.35: Effect of doping (N_D) on diffusion length and open-circuit voltage assuming well passivated surfaces.

a particularly detrimental impact on the short-circuit current since top surface also corresponds to the highest generation region of carriers in the solar cell. Lowering the high top surface recombination is typically accomplished by reducing the number of dangling silicon bonds at the top surface by using “passivating” layer on the top surface. The majority of the electronics industry relies on the use of a thermally grown silicon dioxide layer to passivate the surface due to the low defect states at the interface [112]. For commercial solar cells, dielectric layers such as silicon nitride are commonly used (Fig. 5.36).

Since the passivating layer for silicon solar cells is usually an insulator, any

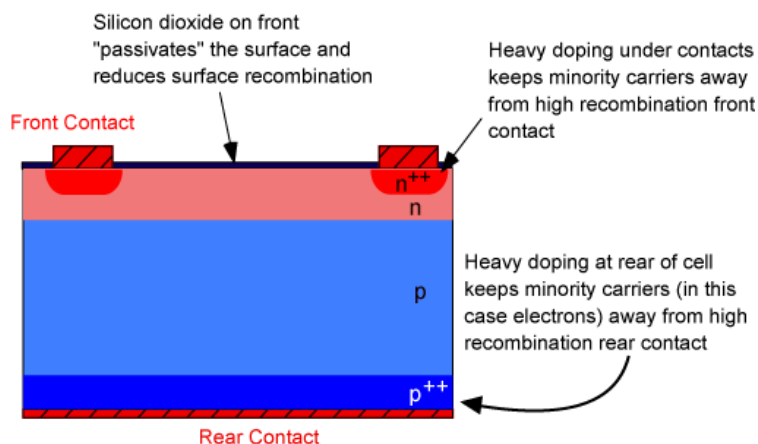


Figure 5.36: Techniques for reducing the impact of surface recombination.

region which has an ohmic metal contact cannot be passivated using silicon dioxide. Instead, under the top contacts the effect of the surface recombination can be minimized by increasing the doping. While typically such a high doping severely degrades the diffusion length, the contact regions do not participate in carrier generation and hence the impact on carrier collection is unimportant. In addition, in cases where a high recombination surface is close to the junction, the lowest recombination option is to increase the doping as high as possible.

Back Surface Field

A similar effect is employed at the rear surface to minimize the impact of rear surface recombination velocity on voltage and current if the rear surface is closer than a diffusion length to the junction. A “back surface field” (BSF) consists of a higher doped region at the rear surface of the solar cell (Figure 5.37). The interface between the high and low doped region behaves like a p-n junction and an electric field forms at the interface which introduces a barrier to minority carrier flow to the rear surface. The minority carrier concentration is thus maintained at higher levels in the bulk of the device and the BSF has a net effect of passivating the rear surface [113].

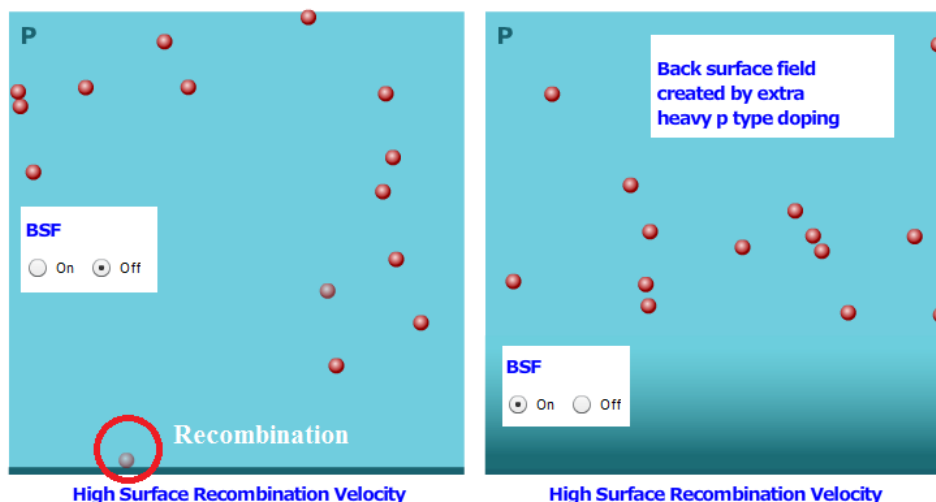


Figure 5.37: Techniques for reducing the impact of surface recombination.

5.2.3 Top Contact Design

Series Resistance

In addition to maximizing absorption and minimizing recombination, the final condition necessary to design a high efficiency solar cell is to minimize parasitic resistive losses. Both shunt and series resistance losses decrease the fill factor and efficiency of a solar cell. A detrimentally low shunt resistance is a processing defect rather than a design parameter. However, the series resistance, controlled by the top contact design and emitter resistance, needs to be carefully designed for each type and size of solar cell structure in order to optimize solar cell efficiency.

The series resistance of a solar cell consists of several components as shown in the Figure 5.38. Of these components, the emitter and top grid (consisting of the finger and busbar resistance) dominate the overall series resistance and are therefore most heavily optimized in solar cell design.

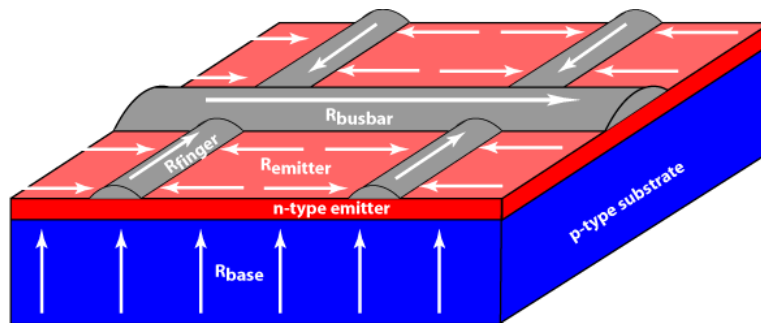


Figure 5.38: Resistive components and current flows in a solar cell.

The metallic top contacts are necessary to collect the current generated by a solar cell. “Busbars” are connected directly to the external leads, while “fingers” are finer areas of metallization which collect current for delivery to the busbars. The key design trade-off in top contact design is the balance between the increased resistive losses associated with a widely spaced grid and the increased reflection caused by a high fraction of metal coverage of the top surface (Figure 5.39).

Generated current typically flows perpendicular to the cell surface from the bulk of the cell and then laterally through the top doped layer until it is collected at a top surface contact.

The resistance and current of the base is assumed to be constant. The resistance to the current of the bulk component of the cell, or the “bulk resistance”, R_b , is defined as:

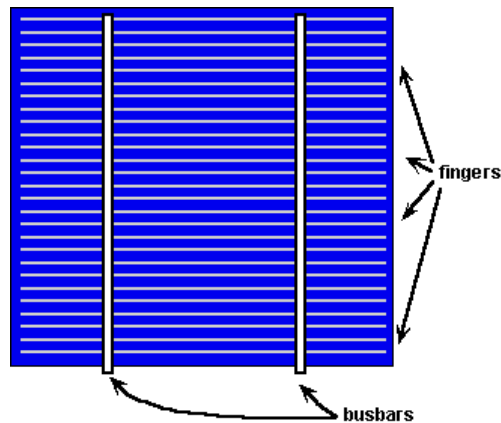


Figure 5.39: Top contact design in a solar cell. The busbars connect the fingers together and pass the generated current to the external electrical contacts.

$$R_b = \frac{\rho l}{A} = \frac{\rho_b W}{A} \quad (5.14)$$

taking into account the thickness of the material. Where: l = length of conducting (resistive) path. ρ_b = “bulk resistivity” (inverse of conductivity) of the bulk cell material (0.5 - 5.0 Ω cm for a typical silicon solar cell). A = cell area, and W = width of bulk region of cell.

Emitter Resistance

For the emitter layer, the resistivity as well as the thickness of the layer will often be unknown, making the resistance of the top layer difficult to calculate from the resistivity and thickness. However, a value known as the “sheet resistivity”, which depends on both the resistivity and the thickness, can be readily measured for the top surface n-type layer. For a uniformly doped layer, the sheet resistivity is defined as:

$$\rho_{\square} = \frac{\rho}{t} \quad (5.15)$$

where: ρ is the resistivity of the layer; and t is the thickness of the layer. The sheet resistivity is normally expressed as ohms/square or Ω/\square . The sheet resistivity of an emitter layer is typically measured with a four-point-probe.

Based on the sheet resistivity, the power loss due to the emitter resistance can be calculated as a function of finger spacing in the top contact. However, the distance that current flows in the emitter is not constant. Current can be collected from the base close to the finger and therefore has only a short distance

to flow to the finger or, alternatively, if the current enters the emitter between the fingers, then the length of the resistive path seen by such a carrier is half the grid spacing (Figure 5.40).

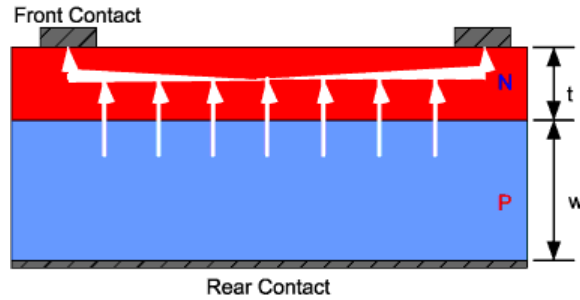


Figure 5.40: Idealised current flow from point of generation to external contact in a solar cell. The emitter is typically much thinner than shown in the diagram.

The incremental power loss in the section dy is given by:

$$dP_{\text{loss}} = I^2 dR \quad (5.16)$$

The differential resistance is given by:

$$dR = \frac{\rho}{b} dy \quad (5.17)$$

where: ρ is the sheet resistivity in Ω/\square , b is the distance along the finger and y the distance between two grid fingers as shown in Figure 5.41.

The current also depends on y and $I(y)$ is the lateral current flow, which is zero at the midpoint between grating lines and increases linearly to its maximum at the grating line, under uniform illumination. The equation for the current is:

$$I(y) = Jby \quad (5.18)$$

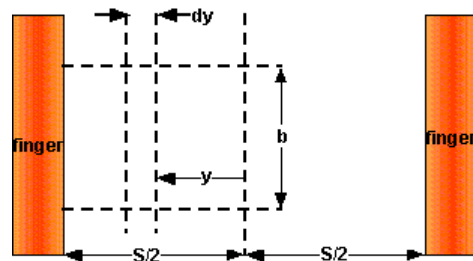


Figure 5.41: Dimensions needed for calculating power loss due to the lateral resistance of the top layer.

where: J is the current density, b is the distance along the finger and y the distance between two grid fingers. The total power loss is therefore:

$$P_{\text{loss}} = \int I(y)^2 dR = \int_0^{S/2} \frac{J^2 b^2 y^2 \rho_{\square} dy}{b} = \frac{J^2 b \rho_{\square} S^3}{24} \quad (5.19)$$

where S is the spacing between grid lines. At the maximum power point, the generated power is:

$$P_{\text{gen}} = J_{MP} b \frac{S}{2} V_{MP} \quad (5.20)$$

The fractional power loss is given by:

$$P_{\% \text{lost}} = \frac{P_{\text{loss}}}{P_{\text{gen}}} = \frac{\rho_{\square} S^2 J_{MP}}{12 V_{MP}} \quad (5.21)$$

Finger Resistance

To provide higher conductivity the top of a cell has a series of regularly spaced finger. While tapered fingers theoretically provide lower losses technology limitations mean that fingers are usually uniform in width. The resistive loss in a finger is calculated as below. Consider an element dx at a distance x from the end of the finger (Figure 5.42).

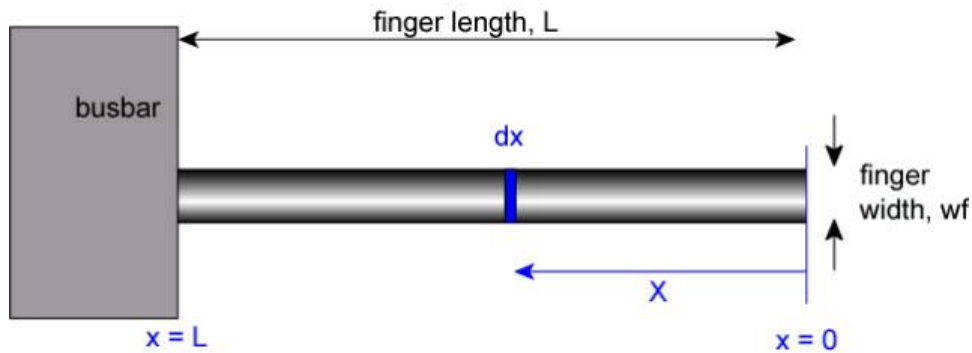


Figure 5.42: Calculation of the power loss in a single finger. The width is assumed constant and it is assumed that the current is uniformly generated and that it flows perpendicularly into the finger, i.e., no current flow directly into the busbar.

The current through the element dx is:

$$I(dx) = x J_{MP} S_f \quad (5.22)$$

where J_{MP} is the current at maximum power point and S_f is the finger spacing. The resistance of the element dx is:

$$R(dx) = \frac{dx\rho_f}{w_f d_f} \quad (5.23)$$

where w_f is the finger width, d_f is the finger depth (or height) and ρ_f is the effective resistivity of the metal.

The power loss in the element dx is:

$$RI^2 = \frac{dx\rho_f}{w_f d_f} (xJ_{MP}S_f)^2 \quad (5.24)$$

Integrating x from 0 to L gives the power loss in the finger:

$$\int_0^L \frac{(xJ_{MP}S_f)^2 \rho_f}{w_f d_f} dx = \frac{1}{3} L^3 J_{MP}^2 S_f^2 \frac{\rho_f}{w_f d_f} \quad (5.25)$$

Combining the equations for resistive losses allows use to determine the total power loss in the top contact grid. In Figure 5.43 the total power losses are shown for different finger spacing.

The parameters used are: Finger length: 50 mm, Emitter Sheet Resistivity: 100 Ω/\square , Metal Resistivity: $1.8 \times 10^{-8} \Omega m$, Finger Width: 100 μm and Finger Depth: 30 μm . For a typical cell type, say a screen printed cell, the metal resistivity will be fixed and the finger width is controlled by the screen size. Typical

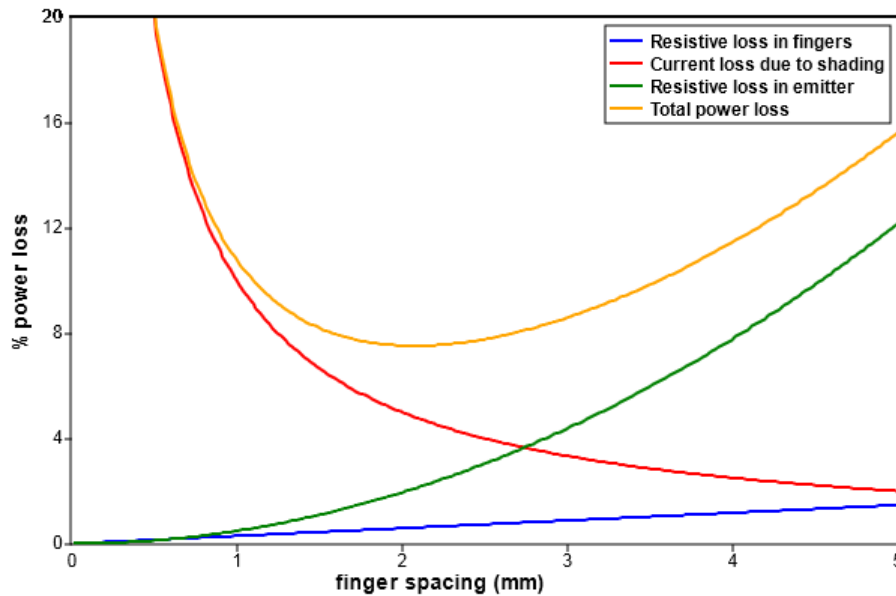


Figure 5.43: Total power and the optimum finger spacing.

values for the specific resistivity of silver are $3 \times 10^{-8} \Omega m$. For non-rectangular fingers the width is set to the actual width and an equivalent height is used to get the correct cross sectional area.

Metal Grid Pattern

The design of the top contact involves not only the minimization of the finger and busbar resistance, but the overall reduction of losses associated with the top contact. These include resistive losses in the emitter, resistive losses in the metal top contact and shading losses. The critical features of the top contact design which determine how the magnitude of these losses are the finger and busbar spacing, the metal height-to-width aspect ratio, the minimum metal line width and the resistivity of the metal. These are shown in the figure 5.44.

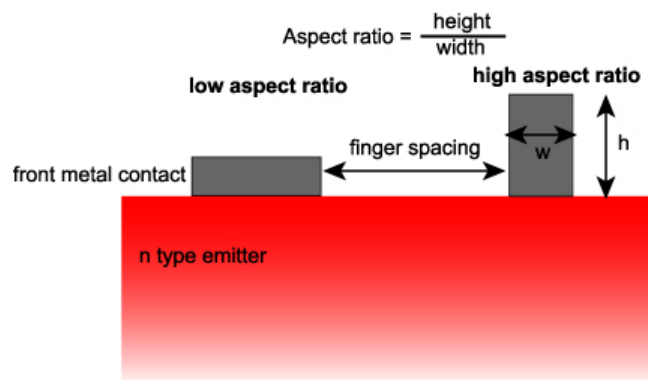


Figure 5.44: Key features of a top surface contacting scheme.

While a multitude of top contacting schemes exist, for practical reasons most top surface metallization patterns are relatively simple and highly symmetrical. A symmetrical contacting scheme can be broken down into unit cells and several broad design rules can be determined. It can be shown [114](Figure 5.45) that:

- The optimum width of the busbar, W_B , occurs when the resistive loss in the busbar equals its shading loss.
- A tapered busbar has lower losses than a busbar of constant width.
- The smaller the unit cell, the smaller finger width, W_F , and the smaller the finger spacings, S , the lower the losses.

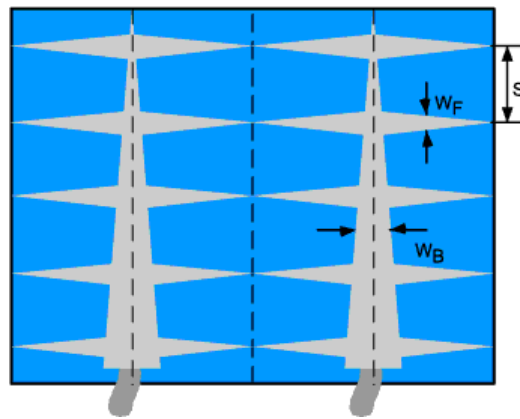


Figure 5.45: Schematic of a top contact design showing busbars and fingers.

Chapter 6

Solar Cell Operation

6.1 Ideal Solar Cells

6.1.1 Solar Cell Structure

A solar cell is an electronic device which directly converts sunlight into electricity. Light shining on the solar cell produces both a current and a voltage to generate electric power. This process requires firstly, a material in which the absorption of light raises an electron to a higher energy state, and secondly, the movement of this higher energy electron from the solar cell into an external circuit. The electron then dissipates its energy in the external circuit and returns to the solar cell. A variety of materials and processes can potentially satisfy the requirements for photovoltaic energy conversion, but in practice nearly all photovoltaic energy conversion uses semiconductor materials in the form of a p-n junction.

The basic steps in the operation of a solar cell are (Figure 6.1):

- the generation of light-generated carriers;
- the collection of the light-generated carries to generate a current;
- the generation of a large voltage across the solar cell;
- the dissipation of power in the load and in parasitic resistances.

The generation of current in a solar cell, known as the “light-generated current”, involves two key processes. The first process is the absorption of incident photons to create electron-hole pairs. Electron-hole pairs will be generated in the solar cell provided that the incident photon has an energy greater than that of the band gap. However, electrons (in the p-type material), and holes (in the

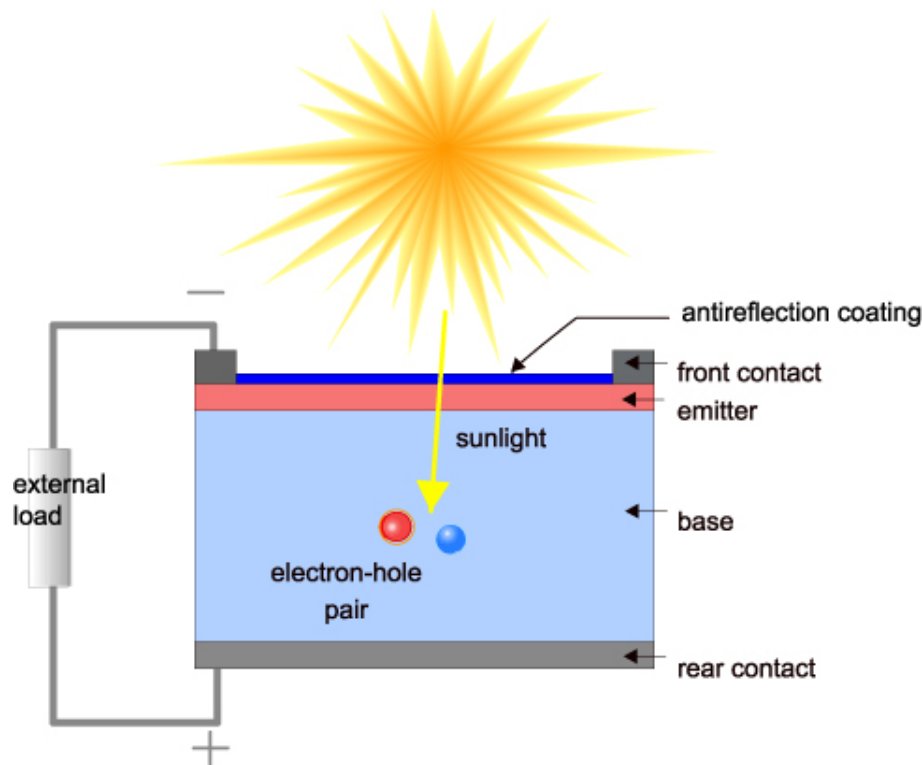


Figure 6.1: Cross section of a solar cell.

n-type material) are meta-stable and will only exist, on average, for a length of time equal to the minority carrier lifetime before they recombine. If the carrier recombines, then the light-generated electron-hole pair is lost and no current or power can be generated.

A second process, the collection of these carriers by the p-n junction, prevents this recombination by using a p-n junction to spatially separate the electron and the hole. The carriers are separated by the action of the electric field existing at the p-n junction. If the light-generated minority carrier reaches the p-n junction, it is swept across the junction by the electric field at the junction, where it is now a majority carrier. If the emitter and base of the solar cell are connected together (i.e., if the solar cell is short-circuited), then the light-generated carriers flow through the external circuit.

6.1.2 Collection Probability

The “collection probability” describes the probability that a carrier generated by light absorption in a certain region of the device will be collected by the p-n junction and therefore contribute to the light-generated current, but probability

depends on the distance that a light-generated carrier must travel compared to the diffusion length. Collection probability also depends on the surface properties of the device. The collection probability of carriers generated in the depletion region is unity as the electron-hole pair are quickly swept apart by the electric field and are collected. Away from the junction, the collection probability drops. If the carrier is generated more than a diffusion length away from the junction, then the collection probability of this carrier is quite low. Similarly, if the carrier is generated closer to a region such as a surface with higher recombination than the junction, then the carrier will recombine. The impact of surface passivation and diffusion length on collection probability is illustrated in Figure 6.2.

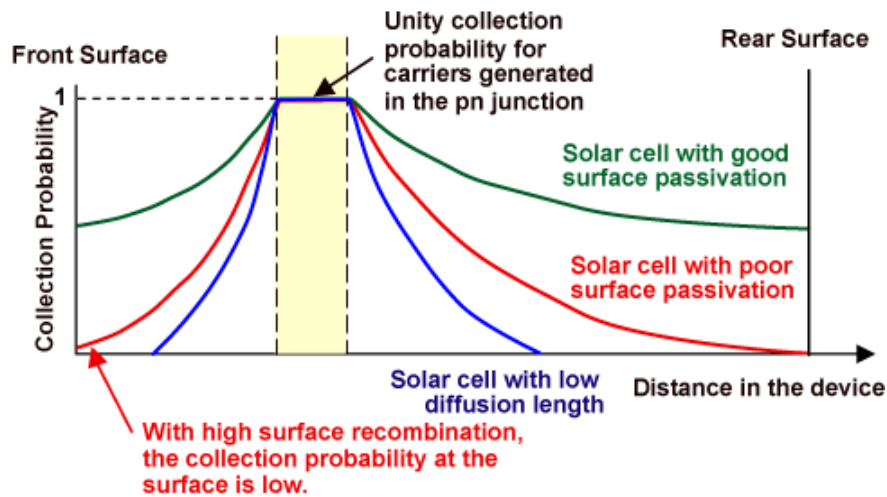


Figure 6.2: Collection probability.

The collection probability in conjunction with the generation rate in the solar cell determine the light-generated current from the solar cell (Figure 6.3). The light-generated current is the integration over the entire device thickness of the generation rate at a particular point in the device, multiplied by the collection probability at that point. The equation for the light-generated current density (J_L), with an arbitrary generation rate ($G(x)$) and collection probability ($CP(x)$), is shown below, as is the generation rate in silicon due to the AM1.5 solar spectrum:

$$J_L = q \int_0^W G(x) CP(x) dx = q \int_0^W \left[\int \alpha(\lambda) H_0 \exp(-\alpha(\lambda)x) d\lambda \right] CP(x) dx \quad (6.1)$$

where: q is the electronic charge; W is the thickness of the device; $\alpha(\lambda)$ is the

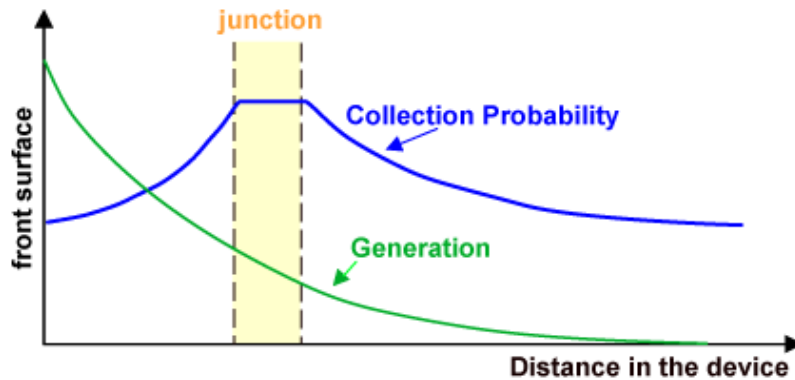


Figure 6.3: The light-generated current depends on the generation of carriers and the collection probability of these carriers.

absorption coefficient; H_0 is the number of photons at each wavelength.

A non-uniform collection probability will cause a spectral dependence in the light-generated current. For example, at the surfaces, the collection probability is lower than in the bulk. Comparing the generation rates for blue, green and infrared light, blue light is nearly completely absorbed in the first few tenths of a micron in silicon. Therefore, if the collection probability at the front surface is low, any blue light in the solar spectrum does not contribute to the light-generated current.

6.1.3 Quantum Efficiency

The “quantum efficiency” (Q.E.) is the ratio of the number of carriers collected by the solar cell to the number of photons of a given energy incident on the solar cell. The quantum efficiency may be given either as a function of wavelength or as energy. If all photons of a certain wavelength are absorbed and the resulting minority carriers are collected, then the quantum efficiency at that particular wavelength is unity. The quantum efficiency for photons with energy below the band gap is zero. A quantum efficiency curve for an ideal solar cell is shown in Figure 6.4.

While quantum efficiency ideally has the square shape shown above, the quantum efficiency for most solar cells is reduced due to recombination effects. The same mechanisms which affect the collection probability also affect the quantum efficiency. For example, front surface passivation affects carriers generated near the surface, and since blue light is absorbed very close to the surface, high front surface recombination will affect the “blue” portion of the quantum efficiency.

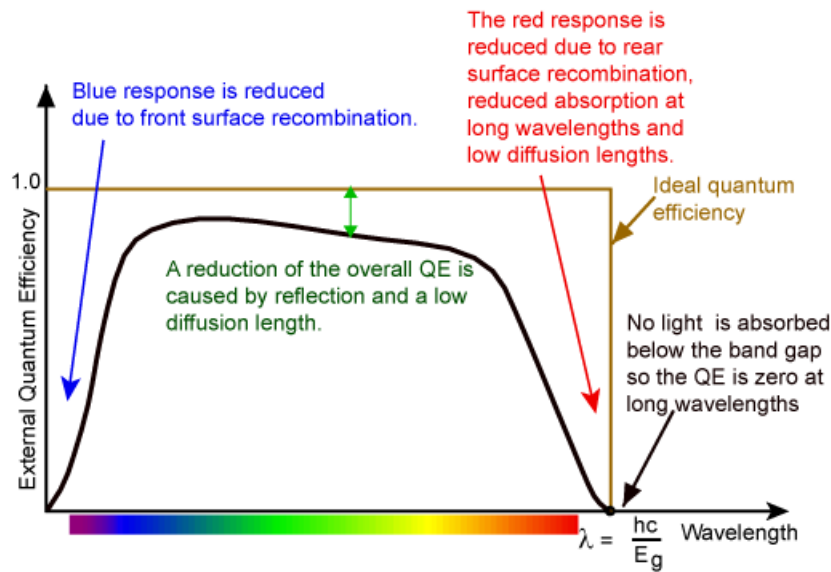


Figure 6.4: The quantum efficiency of a silicon solar cell. Quantum efficiency is usually not measured much below 350 nm as the power from the AM1.5 contained in such low wavelengths is low.

Similarly, green light is absorbed in the bulk of a solar cell and a low diffusion length will affect the collection probability from the solar cell bulk and reduce the quantum efficiency in the “green” portion of the spectrum. The quantum efficiency can be viewed as the collection probability due the generation profile of a single wavelength, integrated over the device thickness and normalized to the incident number of photons.

The “external” quantum efficiency (EQE) of a silicon solar cell includes the effect of optical losses such as transmission and reflection. However, it is often useful to look at the quantum efficiency of the light left after the reflected and transmitted light has been lost. “Internal” quantum efficiency (IQE) refers to the efficiency with which photons that are not reflected or transmitted out of the cell can generate collectable carriers. By measuring the reflection and transmission of a device, the external quantum efficiency curve can be corrected to obtain the internal quantum efficiency curve.

The Figure 6.5 shows the effect on surface recombination and diffusion length on the internal quantum efficiency of a solar cell with parameters:

- Emitter thickness: $1 \mu\text{m}$,
- Emitter diffusivity: $4 \text{ cm}^2\text{s}^{-1}$,

- Emitter diffusion length (L_p): $1 \mu m$,
- Front surface recombination velocity (S_p): 100 cm/s ,
- Base thickness: $300 \mu m$,
- Base diffusivity: $27 \text{ cm}^2\text{s}^{-1}$,
- Base diffusion length (L_n): $100 \mu m$,
- Rear surface recombination velocity (S_n): 100 cm/s .

For base diffusion lengths greater than the device thickness of $300 \mu m$ the rear surface recombination velocity has a large effect on QE. For low diffusion lengths recombination at the rear surface has no effect.

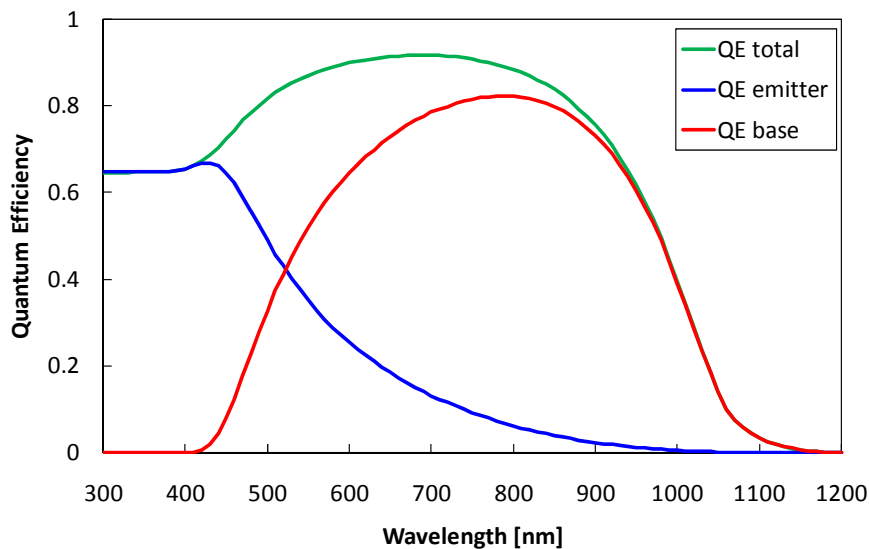


Figure 6.5: Internal quantum efficiency. L_p is the emitter diffusion length (μm), S_p is the front surface recombination velocity (cm/s), L_n is the base diffusion length (μm), S_n is the rear surface recombination velocity (cm/s).

6.1.4 Spectral Response

The spectral response is conceptually similar to the quantum efficiency. The quantum efficiency gives the number of electrons output by the solar cell compared to the number of photons incident on the device, while the spectral response is the ratio of the current generated by the solar cell to the power incident on the solar cell. A spectral response curve is shown in Figure 6.6.

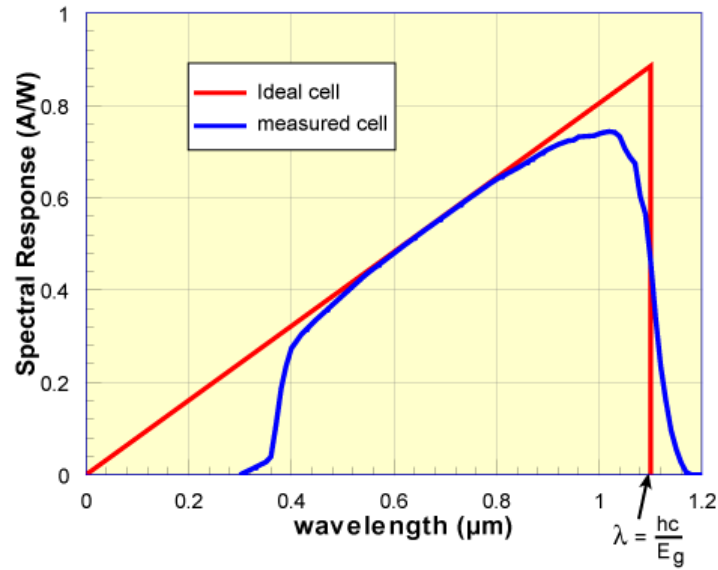


Figure 6.6: The spectral response of a silicon solar cell under glass. At short wavelengths below 400 nm the glass absorbs most of the light and the cell response is very low. At intermediate wavelengths the cell approaches the ideal. At long wavelengths the response fall back to zero. Silicon is an indirect band gap semiconductor so there is not a sharp cut off at the wavelength corresponding to the band gap ($E_g = 1.12\text{ eV}$).

The ideal spectral response is limited at long wavelengths by the inability of the semiconductor to absorb photons with energies below the band gap. This limit is the same as that encountered in quantum efficiency curves. However, unlike the square shape of QE curves, the spectral response decreases at small photon wavelengths. At these wavelengths, each photon has a large energy, and hence the ratio of photons to power is reduced. Any energy above the band gap energy is not utilized by the solar cell and instead goes to heating the solar cell. The inability to fully utilize the incident energy at high energies, and the inability to absorb low energies of light represents a significant power loss in solar cells consisting of a single p-n junction.

Spectral response is important since it is the spectral response that is measured from a solar cell, and from this the quantum efficiency is calculated. The quantum efficiency can be determined from the spectral response by replacing the power of the light at a particular wavelength with the photon flux for that wavelength. This gives:

$$SR = \frac{q\lambda}{hc}QE \quad (6.2)$$

Simplifying gives:

$$SR(A/W) = \frac{QE}{\lambda(nm)}1239.8 \quad (6.3)$$

or

$$SR(A/W) = \frac{QE}{\lambda(\mu m)}1.2398 \quad (6.4)$$

6.2 Solar Cell Parameters

6.2.1 IV Curve

The IV curve of a solar cell is the superposition of the IV curve of the solar cell diode in the dark with the light-generated current [115]. The light has the effect of shifting the IV curve down into the fourth quadrant where power can be extracted from the diode. Illuminating a cell adds to the normal “dark” currents in the diode so that the diode law becomes:

$$I = I_0 \cdot \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] - I_L \quad (6.5)$$

where I_L is the light generated current.

Figure 6.7 shows the effect of the light on the current voltage characteristics of a p-n junction.

The equation for the IV curve in the first quadrant is:

$$I = I_L - I_0 \cdot \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \quad (6.6)$$

The -1 term in the above equation can usually be neglected. The exponential term is usually $\gg 1$ except for voltages below $100mV$. Further, at low voltages the light generated current I_L dominates the I_0 term so the -1 term is not needed under illumination:

$$I = I_L - I_0 \cdot \left[\exp\left(\frac{qV}{nkT}\right) \right] \quad (6.7)$$

Several important parameters which are used to characterize solar cells are discussed in the following pages. The short-circuit current (I_{SC}), the open-circuit

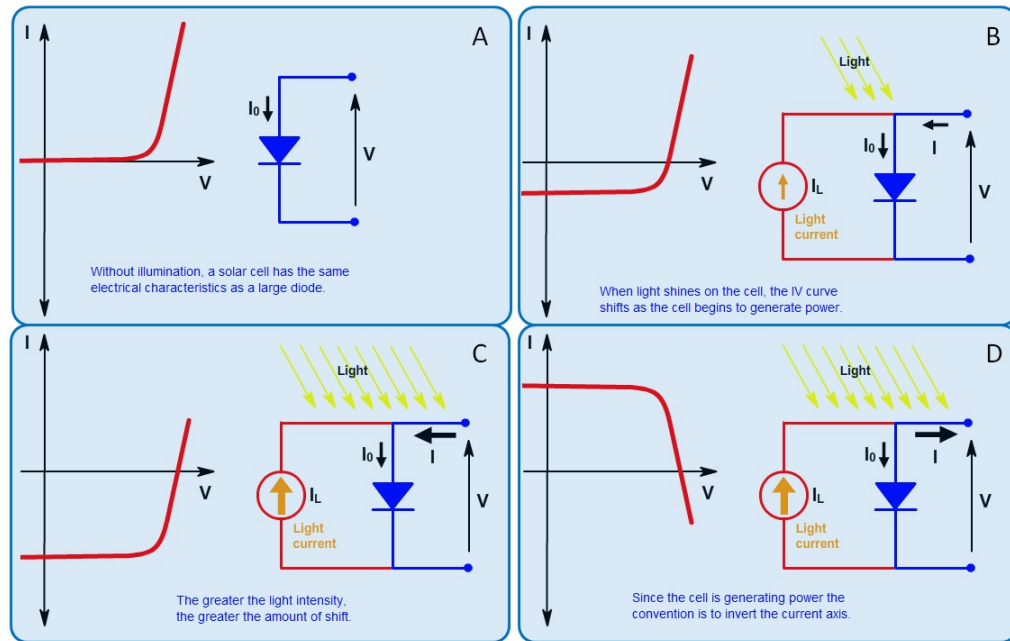


Figure 6.7: The effect of light on the current-voltage characteristics of a p-junction.

voltage (V_{OC}), the fill factor (FF) and the efficiency (η) are all parameters determined from the IV light curve.

6.2.2 Short Circuit Current

The short-circuit current is the current through the solar cell when the voltage across the solar cell is zero (i.e., when the solar cell is short circuited). Usually written as I_{SC} , the short-circuit current is shown on the IV curve in Figure 6.8.

The short-circuit current is due to the generation and collection of light-generated carriers. For an ideal solar cell at most moderate resistive loss mechanisms, the short-circuit current and the light-generated current are identical. Therefore, the short-circuit current is the largest current which may be drawn from the solar cell. The short-circuit current depends on a number of factors which are described below:

- **The area of the solar cell.** To remove the dependence of the solar cell area, it is more common to list the short-circuit current **density** (J_{SC} in mA/cm^2) rather than the short-circuit current.
- **The number of photons** (i.e., the power of the incident light source). I_{SC}

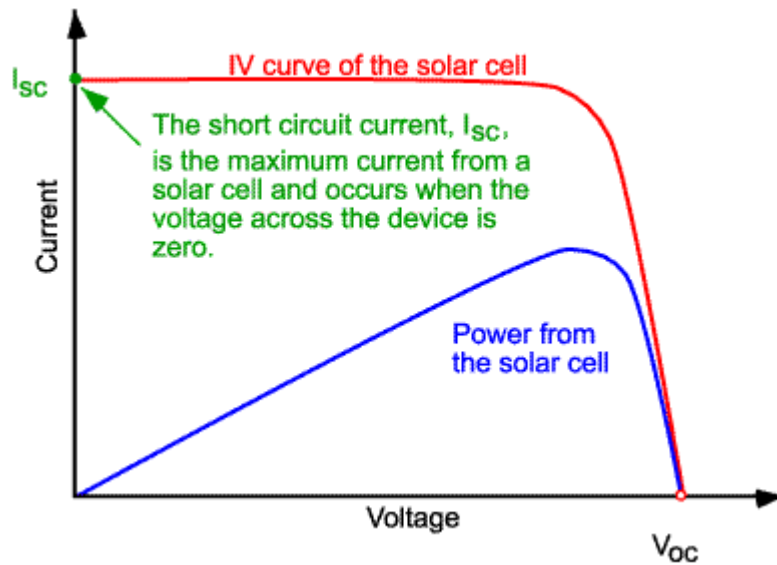


Figure 6.8: IV curve of a solar cell showing the short-circuit current.

from a solar cell is directly dependant on the light intensity as discussed in the paragraph Effect of Light Intensity.

- **The spectrum of the incident light.** For most solar cell measurement, the spectrum is standardized to the AM1.5 spectrum.
- **The optical properties** (absorption and reflection) of the solar cell.
- **The collection probability** of the solar cell, which depends chiefly on the surface passivation and the minority carrier lifetime in the base.

When comparing solar cells of the same material type, the most critical material parameter is the diffusion length and surface passivation. In a cell with perfectly passivated surface and uniform generation, the equation for the short-circuit current can be approximated as:

$$J_{SC} = qG(L_n + L_p) \quad (6.8)$$

where G is the generation rate, and L_n and L_p are the electron and hole diffusion lengths respectively. Although this equation makes several assumptions which are not true for the conditions encountered in most solar cells, the above equation nevertheless indicates that the short-circuit current depends strongly on the generation rate and the diffusion length.

Silicon solar cells under an AM1.5 spectrum have a maximum possible current of 45 mA/cm^2 (Figure 6.9). Laboratory devices have measured short-circuit

currents of over 42 mA/cm^2 , and commercial solar cell have short-circuit currents between about 28 mA/cm^2 and 35 mA/cm^2 .

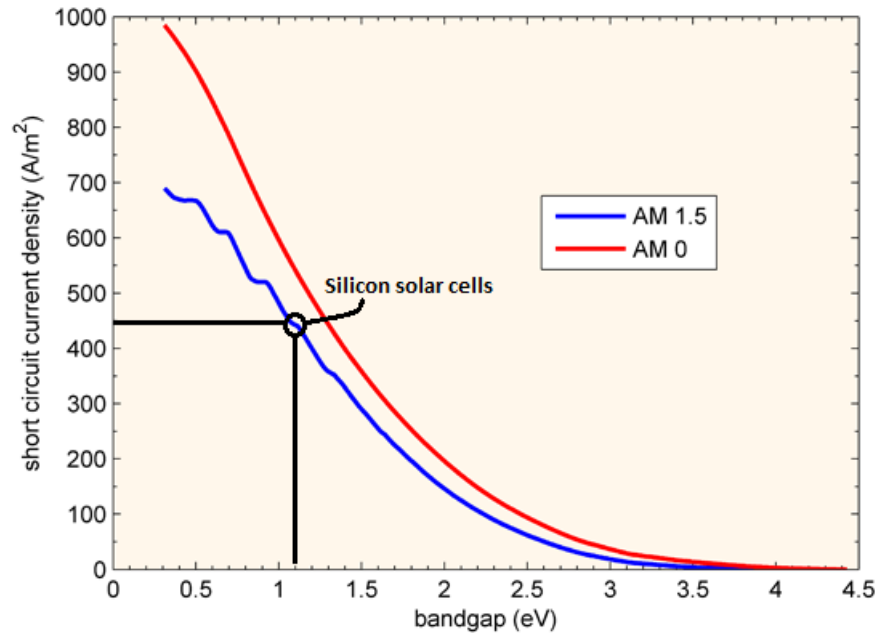


Figure 6.9: In an ideal device every photon above the bandgap gives one charge carrier in the external circuit so the the highest current is for the lowest bandgap.

Illuminated Current and Short Circuit Current (I_L or I_{SC} ?)

I_L is the light generated current inside the solar cell and is the correct term to use in the solar cell equation. At short circuit conditions the externally measured current is I_{SC} . Since I_{SC} is usually equal to I_L , the two are used interchangeably and for simplicity and the solar cell equation is written with I_{SC} in place of I_L . In the case of very high series resistance ($> 10 \Omega\text{cm}^2$) I_{SC} is less than I_L and writing the solar cell equation with I_{SC} is incorrect.

Another assumption is that the illumination current I_L is solely dependent on the incoming light and is independent of voltage across the cell. However, I_L varies with voltage in the case of drift-field solar cells and where carrier lifetime is a function of injection level such as defected multicrystalline materials.

6.2.3 Open Circuit Voltage

The open-circuit voltage, V_{OC} , is the maximum voltage available from a solar cell, and this occurs at zero current. The open-circuit voltage corresponds to the amount of forward bias on the solar cell due to the bias of the solar cell junction with the light-generated current. The open-circuit voltage is shown on the IV curve in Figure 6.10.

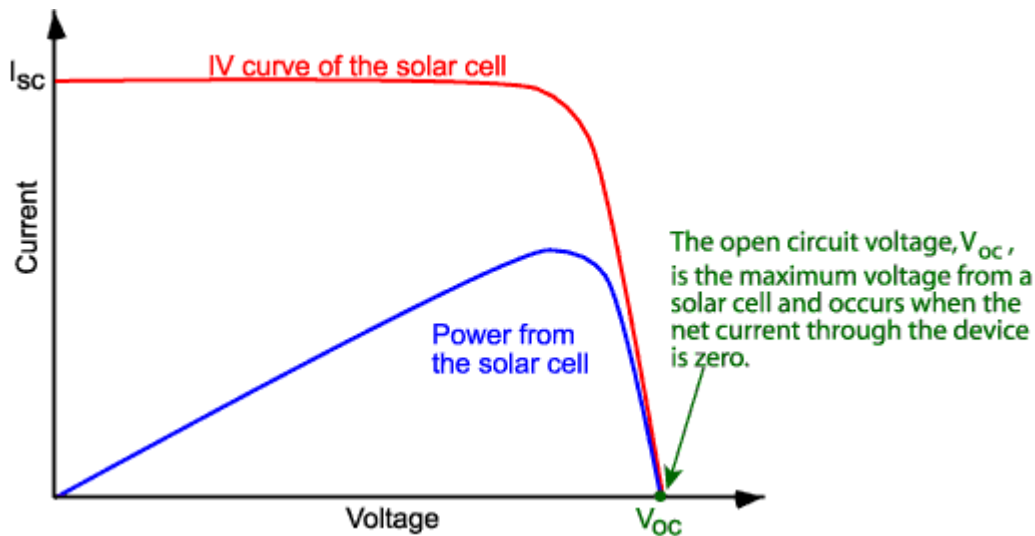


Figure 6.10: IV curve of a solar cell showing the open-circuit voltage.

An equation for V_{OC} is found by setting the net current equal to zero in the solar cell equation to give:

$$V_{OC} = \frac{nKT}{q} \ln \left(\frac{I_L}{I_0} + 1 \right) \quad (6.9)$$

The above equation shows that V_{OC} depends on the saturation current of the solar cell and the light-generated current. While I_{SC} typically has a small variation, the key effect is the saturation current, since this may vary by orders of magnitude. The saturation current, I_0 depends on recombination in the solar cell. Open-circuit voltage is then a measure of the amount of recombination in the device. Silicon solar cells on high quality single crystalline material have open-circuit voltages of up to 730 mV under one sun and AM1.5 conditions, while commercial devices on multicrystalline silicon typically have open-circuit voltages around 600 mV.

The V_{OC} can also be determined from the carrier concentration [116]:

$$V_{OC} = \frac{KT}{q} \ln \left(\frac{(N_A + \Delta n)\Delta n}{n_i^2} \right) \quad (6.10)$$

where kT/q is the thermal voltage, N_A is the doping concentration, Δn is the excess carrier concentration and n_i is the intrinsic carrier concentration. The determination of V_{OC} from the carrier concentration is also termed Implied V_{OC} .

V_{OC} as a Function of Bandgap, E_G

Where the short-circuit current (I_{SC}) decreases with increasing bandgap, the open-circuit voltage increases as the band gap increases. In an ideal device the V_{OC} is limited by radiative recombination and the analysis uses the principle of detailed balance to determine the minimum possible value for J_0 .

The minimum value of the diode saturation current is given by [117]:

$$J_0 = \frac{q}{k} \frac{15\sigma}{\pi^4} T^3 \int_u^\infty \frac{x^2}{e^x - 1} dx \quad (6.11)$$

where q is the electronic charge, σ is the Stefan-Boltzman constant, k is Boltmann constant, T is the temperature and

$$u = \frac{E_G}{kT} \quad (6.12)$$

Evaluating the integral in the above equation is quite complex. The Figure 6.11 uses the method outlined in [118].

The J_0 calculated above can be directly plugged into the standard solar cell equation given at the top of the page to determine the V_{OC} so long as the voltage is less than the band gap, as is the case under one sun illumination (Figure 6.12).

6.2.4 Fill Factor

The short-circuit current and the open-circuit voltage are the maximum current and voltage respectively from a solar cell. However, at both of these operating points, the power from the solar cell is zero. The “fill factor”, more commonly known by its abbreviation FF , is a parameter which, in conjunction with V_{OC} and I_{SC} , determines the maximum power from a solar cell. The FF is defined as the ratio of the maximum power from the solar cell to the product of V_{OC} and I_{SC} . Graphically, the FF is a measure of the “squareness” of the solar cell and is also the area of the largest rectangle which will fit in the IV curve. The FF is illustrated in Figure 6.13.

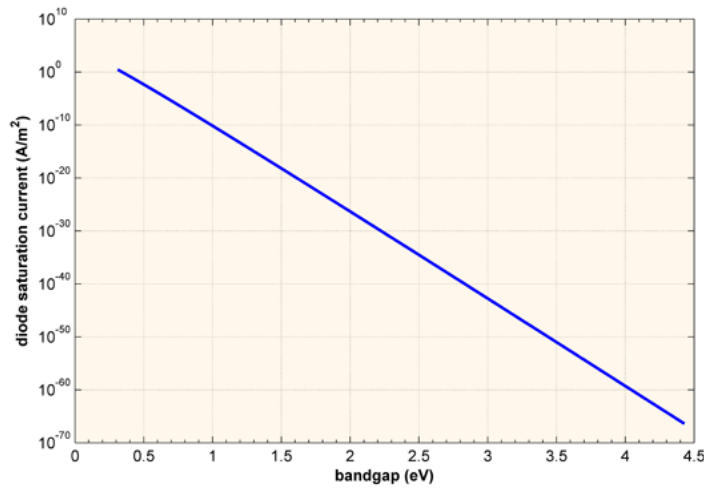


Figure 6.11: Diode saturation current as a function of band gap. The values are determined from detailed balance and place a limit on the open circuit voltage of a solar cell.

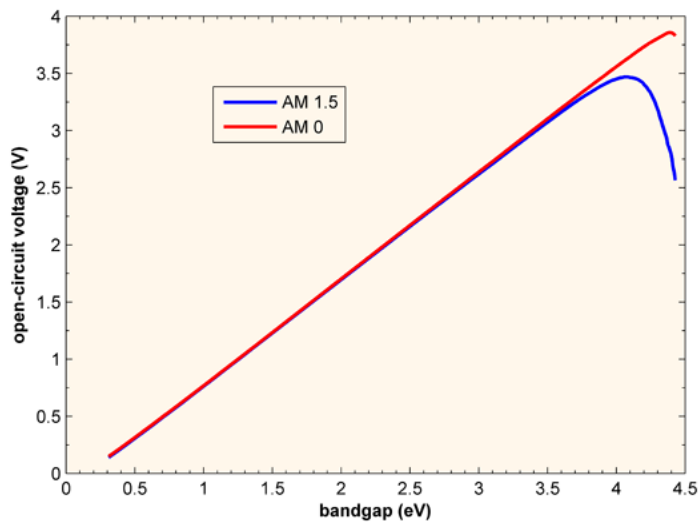


Figure 6.12: V_{OC} as function of bandgap for a cell with AM0 and AM1.5. The V_{OC} increases with bandgap as the recombination current falls. There is drop off in V_{OC} at very high band gaps due to the very low I_{SC} .

As FF is a measure of the “squareness” of the IV curve, a solar cell with a higher voltage has a larger possible FF since the “rounded” portion of the IV curve takes up less area. The maximum theoretical FF from a solar cell can be determined by differentiating the power from a solar cell with respect to voltage

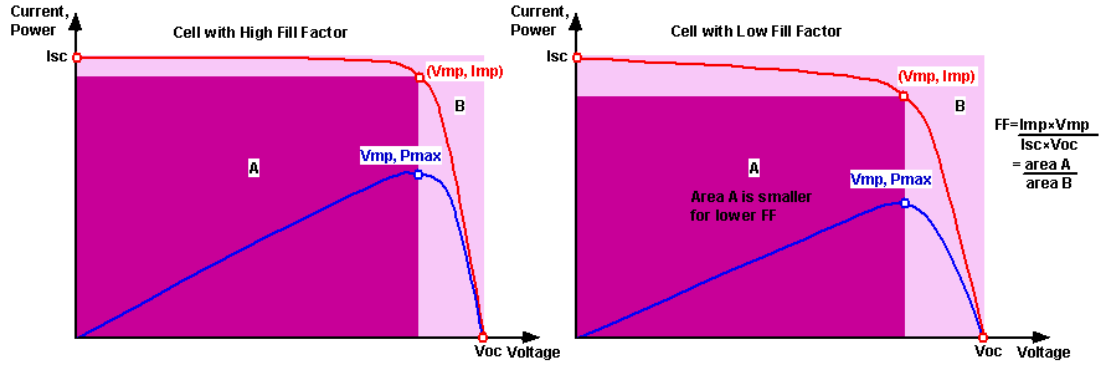


Figure 6.13: Graph of cell output current (red line) and power (blue line) as function of voltage. Also shown are the cell short-circuit current (I_{SC}) and open-circuit voltage (V_{OC}) points, as well as the maximum power point (V_{MP} , I_{MP}). Curve changes for a cell with low FF and a cell with high FF .

and finding where this is equal to zero. Hence:

$$\frac{d(IV)}{dV} = 0 \quad (6.13)$$

giving:

$$V_{MP} = V_{OC} - \frac{nkT}{q} \ln \left(\frac{V_{MP}}{nkT/q} + 1 \right) \quad (6.14)$$

However, the above technique does not yield a simple or closed form equation. The equation above only relates V_{OC} to V_{MP} , and extra equations are needed to find I_{MP} and FF . A more commonly used expression for the FF can be determined empirically as [119]:

$$FF = \frac{\overline{V_{OC}} - \ln(\overline{V_{OC}} + 0.72)}{\overline{V_{OC}} + 1} \quad (6.15)$$

where $\overline{V_{OC}}$ is defined as a normalized “ V_{OC} ”:

$$\overline{V_{OC}} = v_{oc} = \frac{q}{nkT} V_{OC} \quad (6.16)$$

The above equations show that a higher voltage will have a higher possible FF . However, large variations in open-circuit voltage within a given material system are relatively uncommon. For example, at one sun, the difference between the maximum open-circuit voltage measured for a silicon laboratory device and a typical commercial solar cell is about 120 mV, giving maximum FF 's respectively of 0.85 and 0.83. However, the variation in maximum FF can be significant for

solar cells made from different materials. For example, a GaAs solar cell may have a FF approaching 0.89.

The above equation also demonstrates the importance of the ideality factor, also known as the “n-factor” of a solar cell. The ideality factor is a measure of the junction quality and the type of recombination in a solar cell. For the simple recombination mechanisms, the n-factor has a value of 1. However, some recombination mechanisms, particularly if they are large, may introduce recombination mechanisms of 2. A high n-value not only degrades the FF , but since it will also usually signal high recombination, it gives low open-circuit voltages.

A key limitation in the equations described above is that they represent a maximum possible FF , although in practice the FF will be lower due to the presence of parasitic resistive losses, which are discussed in Effects of Parasitic Resistances. Therefore, the FF is most commonly determined from measurement of the IV curve and is defined as the maximum power divided by the product of I_{SC} and V_{OC} , i.e.:

$$FF = \frac{I_{MP} \times V_{MP}}{I_{SC} \times V_{OC}} \quad (6.17)$$

6.2.5 Efficiency

The efficiency is the most commonly used parameter to compare the performance of one solar cell to another. Efficiency is defined as the ratio of energy output from the solar cell to input energy from the sun. In addition to reflecting the performance of the solar cell itself, the efficiency depends on the spectrum and intensity of the incident sunlight and the temperature of the solar cell. Therefore, conditions under which efficiency is measured must be carefully controlled in order to compare the performance of one device to another. Terrestrial solar cells are measured under AM1.5 conditions and at a temperature of 25 °C. Solar cells intended for space use are measured under AM0 conditions. Recent top efficiency solar cell results are given in Table 6.1.

Table 6.1: Solar Cell Efficiency Records

Classification	Efficiency	Device Description	Area (cm^2)	V_{OC}	$J_{SC}(mA/cm^2)$	FF (%)
Cell (concentrator)	41.1 %	Triple-junction (Fraunhofer)	0.0509	2.867	$I_{SC} = 380.5mA$	87.2
Cell at one-sun	35.8 %	InGaP/GaAs/InGaAs (Sharp)	3.989	2.622	14.37	85
Silicon Cell (one-sun)	25.0 %	UNSW PERL	4.00	0.706	42.7	82.8
Module (concentrator)	27.0 %	Entech	34			
Module (one-sun)	22.7 %	UNSW PERL	778	5.6	3.93 (for module)	80.3
Module (production)	20.4 %	SunPower	16300	68.6	6.12 (for module)	79.1

The efficiency of a solar cell is determined as the fraction of incident power which is converted to electricity and is defined as:

$$P_{MAX} = V_{OC}I_{SC}FF \quad (6.18)$$

$$\eta = \frac{V_{OC}I_{SC}FF}{P_{IN}} \quad (6.19)$$

where V_{OC} is the open-circuit voltage, I_{SC} is the short-circuit current, FF is the fill factor and η is the efficiency.

The input power for efficiency calculations is $1 \text{ kW}/\text{m}^2$ or $100 \text{ mW}/\text{cm}^2$. Thus the input power for a $100 \times 100 \text{ mm}^2$ cell is 10 W and for a $156 \times 156 \text{ mm}^2$ cell is 24.3 W .

6.3 Resistive Effects

6.3.1 Characteristic Resistance

The characteristic resistance of a solar cell is the output resistance of the solar cell at its maximum power point. If the resistance of the load is equal to the characteristic resistance of the solar cell, then the maximum power is transferred to the load and the solar cell operates at its maximum power point. It is a useful parameter in solar cell analysis, particularly when examining the impact of parasitic loss mechanisms. The characteristic resistance is shown in the figure 6.14.

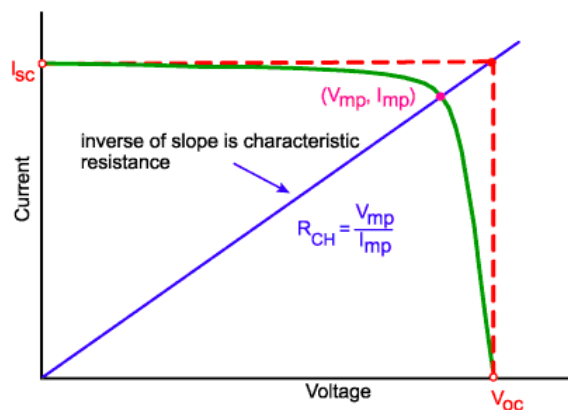


Figure 6.14: Characteristic Resistance of a solar cell.

The characteristic resistance of a solar cell is the inverse of the slope of the line, shown in the figure, which, after Green [120], can be given as:

$$R_{CH} = \frac{V_{MP}}{I_{MP}} \quad (6.20)$$

It can alternately be given as an approximation where:

$$R_{CH} = \frac{V_{OC}}{I_{SC}} \quad (6.21)$$

6.3.2 Effect of Parasitic Resistances

Resistive effects in solar cells reduce the efficiency of the solar cell by dissipating power in the resistances. The most common parasitic resistances are series resistance and shunt resistance. The inclusion of the series and shunt resistance on the solar cell model is shown in the figure 6.15.

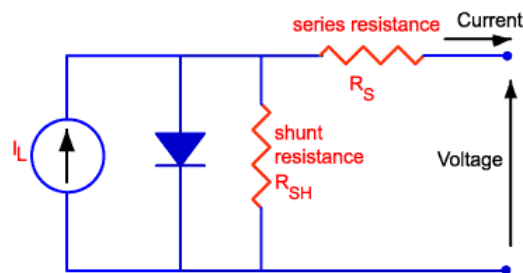


Figure 6.15: Parasitic series and shunt resistances in a solar cell circuit.

In most cases and for typical values of shunt and series resistance, the key impact of parasitic resistance is to reduce the fill factor. Both the magnitude and impact of series and shunt resistance depend on the geometry of the solar cell, at the operating point of the solar cell. Since the value of resistance will depend on the area of the solar cell, when comparing the series resistance of solar cells which may have different areas, a common unit for resistance is in Ωcm^2 . This area-normalized resistance results from replacing current with current density in Ohm's law as shown below:

$$R'(\Omega cm^2) = \frac{V}{J} \quad (6.22)$$

The effects of series and shunt resistances are described in the following pages.

Series Resistance

Series resistance (figure 6.16) in a solar cell has three causes: firstly, the movement of current through the emitter and base of the solar cell; secondly, the contact

resistance between the metal contact and the silicon; and finally the resistance of the top and rear metal contacts. The main impact of series resistance is to reduce the fill factor, although excessively high values may also reduce the short-circuit current.

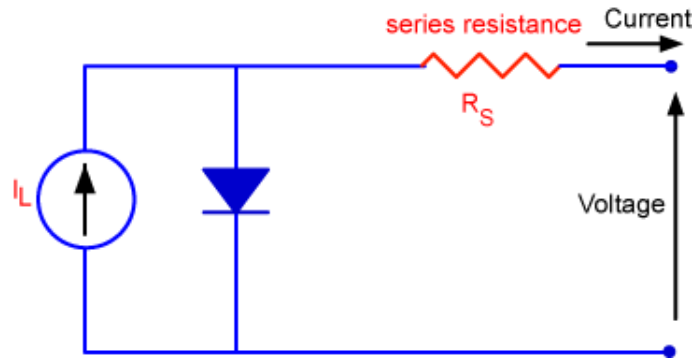


Figure 6.16: Schematic of a solar cell with series resistance.

The equation for a solar cell in presence of a series resistance is:

$$I = I_L - I_0 \exp \left[\frac{q(V + IR_S)}{nkT} \right] \quad (6.23)$$

where: I is the cell output current, I_L is the light generated current, V is the voltage across the cell terminals, T is the temperature, q and k are constants, n is the ideality factor, and R_S is the cell series resistance. The formula is an example of an implicit function due to the appearance of the current, I , on both sides of the equation and requires numerical methods to solve.

The effect of the series resistance on the IV curve is shown in figure 6.17. To generate the plot the voltage across the diode is varied thereby avoiding the need to solve an implicit equation.

Series resistance does not affect the solar cell at open-circuit voltage since the overall current flow through the solar cell, and therefore through the series resistance is zero. However, near the open-circuit voltage, the IV curve is strongly effected by the series resistance. A straight-forward method of estimating the series resistance from a solar cell is to find the slope of the IV curve at the open-circuit voltage point.

An equation for the FF as a function of series resistance can be determined by noting that for moderate values of series resistance, the maximum power may be approximated as the power in the absence of series resistance minus the power lost in the series resistance. The equation for the maximum power from a solar cell then becomes:

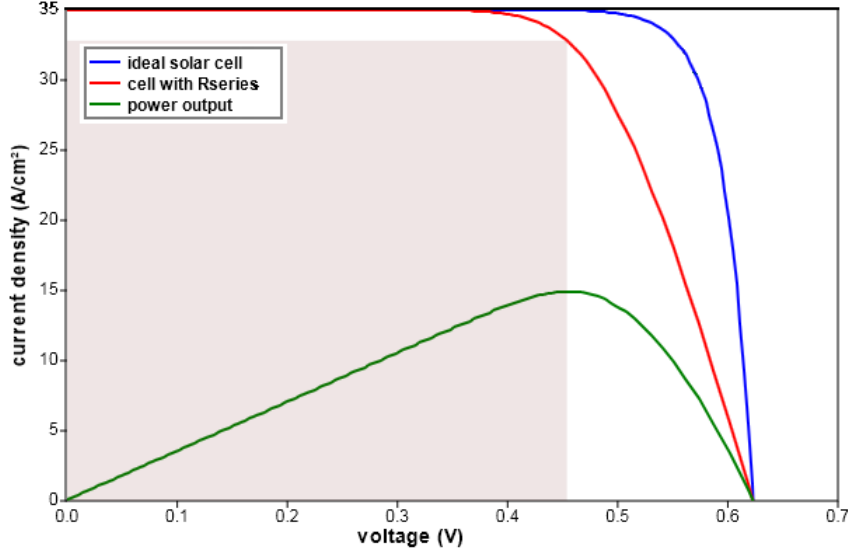


Figure 6.17: The effect of series resistance on fill factor. The series resistance is $3 \Omega\text{cm}^2$ (red curve). The area of the solar cell is 1 cm^2 so that the units of resistance can be either ω or ωcm^2 . The short circuit current (I_{SC}) is unaffected by the series resistance until it is very large.

$$P'_{MP} \approx V_{MP}I_{MP} - I_{MP}^2R_S = V_{MP}I_{MP} \left(1 - \frac{I_{MP}}{V_{MP}}R_S\right) = P_{MP} \left(1 - \frac{I_{SC}}{V_{OC}}R_S\right) \quad (6.24)$$

$$P'_{MP} = P_{MP} \left(1 - \frac{R_S}{R_{CH}}\right) \quad (6.25)$$

defining a normalized series resistance as:

$$r_s = \frac{R_S}{R_{CH}} \quad (6.26)$$

gives the following equation which approximates the effect of series resistance on the output power of a solar cell:

$$P'_{MP} = P_{MP}(1 - r_s) \quad (6.27)$$

Assuming that the open-circuit voltage and short-circuit current are not affected by the series resistance allows the impact of series resistance on FF to be determined as:

$$P'_{MP} = P_{MP}(1 - r_s)$$

$$V'_{OC}I'_{SC}FF' = V_{OC}I_{SC}FF(1 - r_s)$$

$$FF' = FF(1 - r_s) \quad (6.28)$$

In the above equation the fill factor which is not affected by series resistance is denoted by FF_0 and FF' is called FF_S . The equation then becomes:

$$FF_S = FF_0(1 - r_s) \quad (6.29)$$

An empirical equation, which is slightly more accurate for the relationship between FF_0 and FF_S is:

$$FF_S = FF_0(1 - 1.1r_s) + \frac{r_s^2}{5.4} \quad (6.30)$$

which is valid for $r_s < 0.4$ and $v_{oc} > 10$.

Typical values for area-normalized series resistance are between $0.5 \Omega cm^2$ for laboratory type solar cells and up to $0.65 \Omega cm^2$ for commercial solar cells.

Shunt Resistance

Significant power losses caused by the presence of a shunt resistance (figure 6.18), R_{SH} , are typically due to manufacturing defects, rather than poor solar cell design. Low shunt resistance causes power losses in solar cells by providing an alternate current path for the light-generated current. Such a diversion reduces the amount of current flowing through the solar cell junction and reduces the voltage from the solar cell. The effect of a shunt resistance is particularly severe at low light levels, since there will be less light-generated current. The loss of this current to the shunt therefore has a larger impact. In addition, at lower voltages where the effective resistance of the solar cell is high, the impact of a resistance in parallel is large.

The equation for a solar cell in presence of a shunt resistance is:

$$I = I_L - I_0 \exp \left[\frac{qV}{nkT} \right] - \frac{V}{R_{SH}} \quad (6.31)$$

where: I is the cell output current, I_L is the light generated current, V is the voltage across the cell terminals, T is the temperature, q and k are constants, n is the ideality factor, and R_{SH} is the cell shunt resistance.

The effect of a low shunt resistance is shown in the figure 6.19.

An estimate for the value of the shunt resistance of a solar cell can be determined from the slope of the IV curve near the short-circuit current point.

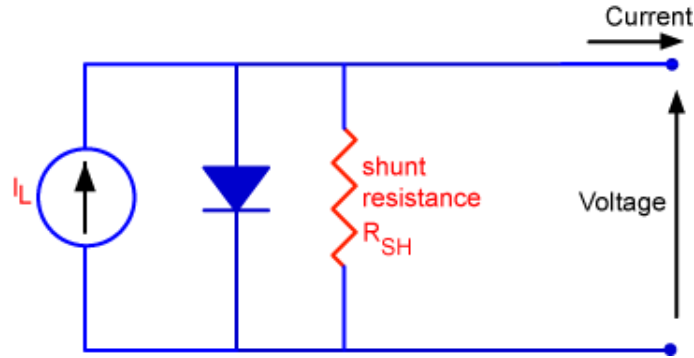


Figure 6.18: Schematic of a solar cell with shunt resistance.

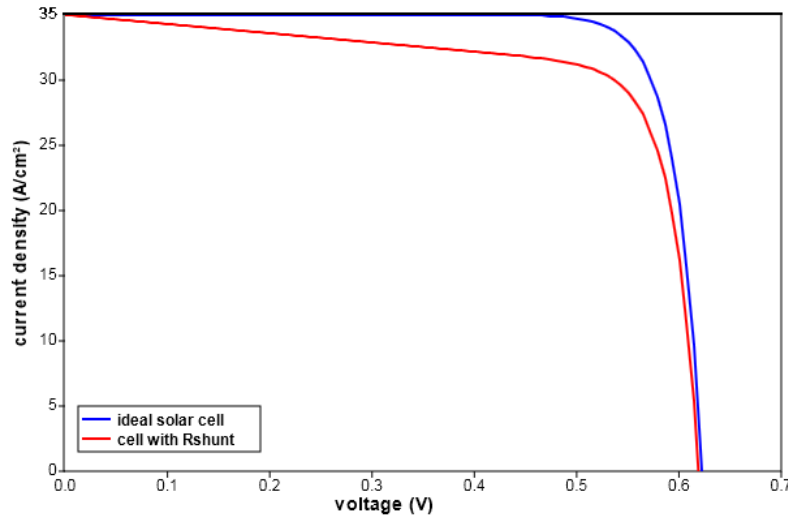


Figure 6.19: The effect of shunt resistance on fill factor in a solar cell. The cell series resistance is zero, temperature is 300 K, and I_0 is 10^{-12} A/cm^2 . The shunt resistance is $141 \text{ } \Omega\text{cm}^2$

The impact of the shunt resistance on the fill factor can be calculated in a manner similar to that used to find the impact of series resistance on fill factor. The maximum power may be approximated as the power in the absence of shunt resistance, minus the power lost in the shunt resistance. The equation for the maximum power from a solar cell then becomes:

$$P'_{MP} \approx V_{MP} I_{MP} - \frac{V_{MP}^2}{R_{SH}} = V_{MP} I_{MP} \left(1 - \frac{V_{MP}}{I_{MP}} \frac{1}{R_{SH}} \right) = P_{MP} \left(1 - \frac{V_{OC}}{I_{SC}} \frac{1}{R_{SH}} \right) \quad (6.32)$$

$$P'_{MP} = P_{MP} \left(1 - \frac{R_{CH}}{R_S} \right) \quad (6.33)$$

defining a normalized shunt resistance as:

$$r_{sh} = \frac{R_{SH}}{R_{CH}} \quad (6.34)$$

gives the following equation which approximates the effect of shunt resistance on the output power of a solar cell:

$$P'_{MP} = P_{MP} \left(1 - \frac{1}{r_{sh}} \right) \quad (6.35)$$

Assuming that the open-circuit voltage and short-circuit current are not affected by the shunt resistance allows the impact of series resistance on FF to be determined as:

$$\begin{aligned} P'_{MP} &= P_{MP} \left(1 - \frac{1}{r_{sh}} \right) \\ V'_{OC} I'_{SC} FF' &= V_{OC} I_{SC} FF \left(1 - \frac{1}{r_{sh}} \right) \\ FF' &= FF \left(1 - \frac{1}{r_{sh}} \right) \end{aligned} \quad (6.36)$$

In the above equation the fill factor which is not affected by shunt resistance is denoted by FF_0 and FF' is called FF_{SH} . The equation then becomes:

$$FF_{SH} = FF_0 \left(1 - \frac{1}{r_{sh}} \right) \quad (6.37)$$

An empirical equation, which is slightly more accurate for the relationship between FF_0 and FF_{SH} is:

$$FF_{SH} = FF_0 \left(1 - \frac{v_{oc} + 0.7 FF_0}{v_{oc} r_{sh}} \right) \quad (6.38)$$

which is valid for $r_s > 0.4$.

Typical values for area-normalized shunt resistance are in the $M\Omega cm^2$ range for laboratory type solar cells, and $1000 \Omega cm^2$ for commercial solar cells.

6.4 Others Effects

6.4.1 Impact of Both Series and Shunt Resistance

In the presence of both series and shunt resistances, the IV curve of the solar cell is given by:

$$I = I_L - I_0 \exp \left[\frac{q(V + IR_S)}{nkT} \right] - \frac{V + IR_S}{R_{SH}} \quad (6.39)$$

and the circuit diagram of the solar cell is given in figure 6.20.

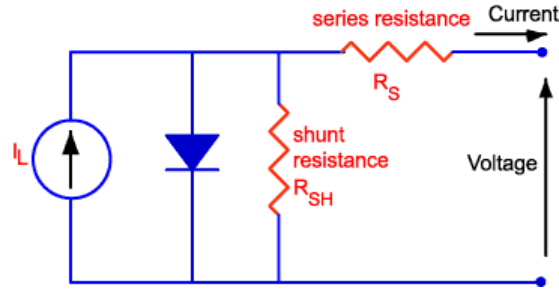


Figure 6.20: Parasitic series and shunt resistances in a solar cell circuit.

To combine the effect of both series and shunt resistances, the expression for FF_{SH} , derived above, can be used, with FF_0 replaced by FF_S ([121]). The overall equation then becomes:

$$FF_{SH} = FF_S \left(1 - \frac{v_{oc} + 0.7 FF_S}{v_{oc} r_{sh}} \right) \quad (6.40)$$

where FF_S is given by:

$$FF_S = FF_0(1 - 1.1r_s) + \frac{r_s^2}{5.4}$$

and by combining the above equations, the net equation for FF becomes:

$$FF = FF_0 \left\{ (1 - 1.1r_s) + \frac{r_s^2}{5.4} \right\} \left\{ 1 - \frac{v_{oc} + 0.7 FF_0}{v_{oc} r_{sh}} \left[(1 - 1.1r_s) + \frac{r_s^2}{5.4} \right] \right\} \quad (6.41)$$

Figure 6.21 shows the effect of both shunt and series resistances on the IV curve of a solar cell.

6.4.2 Effect of Temperature

Like all other semiconductor devices, solar cells are sensitive to temperature. Increases in temperature reduce the band gap of a semiconductor, thereby effecting most of the semiconductor material parameters. The decrease in the band gap of a semiconductor with increasing temperature can be viewed as increasing the energy of the electrons in the material. Lower energy is therefore needed to break

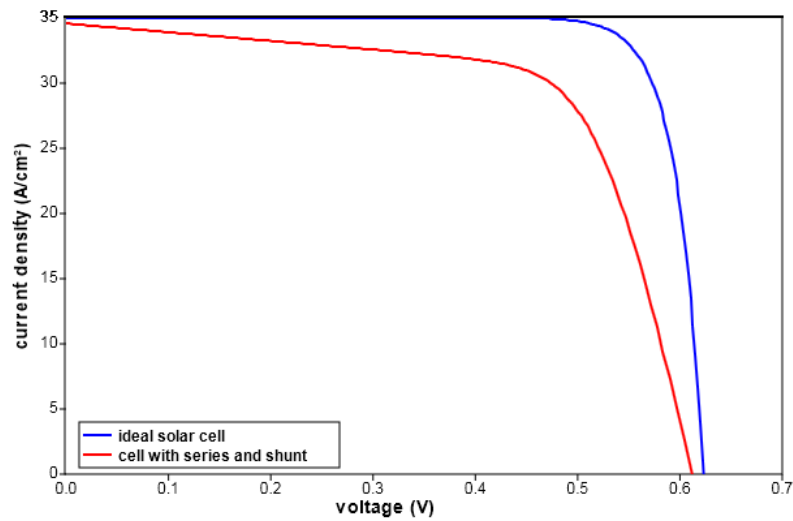


Figure 6.21: The effect of shunt and series resistances on the IV curve in a solar cell. Cell series resistance is $2 \Omega\text{cm}^2$ and the shunt resistance is $150 \Omega\text{cm}^2$.

the bond. In the bond model of a semiconductor band gap, reduction in the bond energy also reduces the band gap. Therefore increasing the temperature reduces the band gap.

In a solar cell, the parameter most affected by an increase in temperature is the open-circuit voltage. The impact of increasing temperature is shown in the figure 6.22.

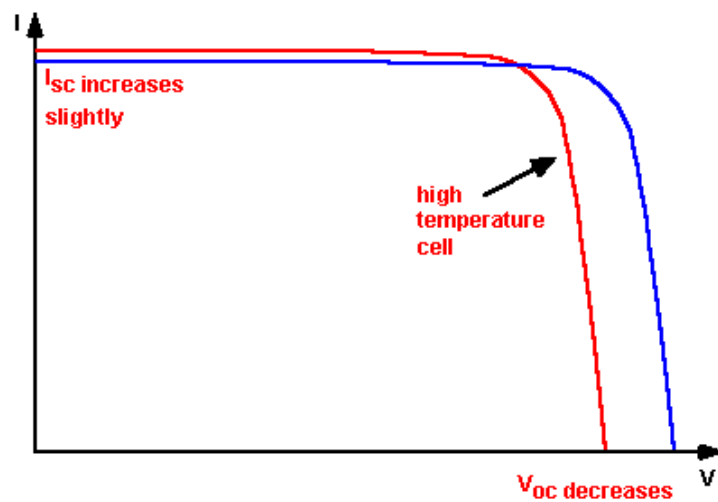


Figure 6.22: The effect of temperature on the IV characteristics of a solar cell.

The open-circuit voltage decreases with temperature because of the temperature dependence of I_0 . The equation for I_0 from one side of a p-n junction is

given by:

$$I_0 = qA \frac{Dn_i^2}{LN_D} \quad (6.42)$$

where: q is the electronic charge; D is the diffusivity of the minority carrier for silicon as a function of doping; L is the diffusion length of the minority carrier; N_D is the doping; and n_i is the intrinsic carrier concentration for silicon.

In the above equation, many of the parameters have some temperature dependence, but the most significant effect is due to the intrinsic carrier concentration, n_i . The intrinsic carrier concentration depends on the band gap energy (with lower band gaps giving a higher intrinsic carrier concentration), and on the energy which the carriers have (with higher temperatures giving higher intrinsic carrier concentrations). The equation for the intrinsic carrier concentration is:

$$n_i^2 = 4 \left(\frac{2\pi kT}{h^2} \right)^3 (m_e^* m_h^*)^{(3/2)} \exp \left(-\frac{E_{G0}}{kT} \right) = BT^3 \exp \left(-\frac{E_{G0}}{kT} \right) \quad (6.43)$$

where: T is the temperature; h and k are constants; m_e^* and m_h^* are the effective masses of electrons and holes respectively; E_{G0} is the band gap linearly extrapolated to absolute zero; and B is a constant which is essentially independent of temperature.

Substituting these equations back into the expression for I_0 , and assuming that the temperature dependencies of the other parameters can be neglected, gives:

$$I_0 = qA \frac{D}{LN_D} BT^3 \exp \left(-\frac{E_{G0}}{kT} \right) \approx B'T^\gamma \exp \left(-\frac{E_{G0}}{kT} \right) \quad (6.44)$$

where B' is a temperature independent constant. A constant γ , is used instead of the number 3 to incorporate the possible temperature dependencies of the other material parameters. For silicon solar cells near room temperature, I_0 approximately doubles for every 10 degrees increase in temperature.

The impact of I_0 on the open-circuit voltage can be calculated by substituting the equation for I_0 into the equation for V_{OC} as shown below:

$$\begin{aligned} V_{0C} &= \frac{kT}{q} \ln \left(\frac{I_{SC}}{I_0} \right) = \\ &= \frac{kT}{q} [\ln I_{SC} - \ln I_0] = \frac{kT}{q} \ln I_{SC} - \frac{kT}{q} \ln \left[B'T^\gamma \exp \left(-\frac{E_{G0}}{kT} \right) \right] = \end{aligned}$$

$$= \frac{kT}{q} \left(\ln I_{SC} - \ln B' - \gamma \ln T + \frac{qV_{G0}}{kT} \right) \quad (6.45)$$

where $E_{G0} = qV_{G0}$. Assuming that dV_{OC}/dT does not depend on dI_{SC}/dT , dV_{OC}/dT can be found as:

$$\frac{dV_{OC}}{dT} = \frac{V_{OC} - V_{G0}}{T} - \gamma \frac{k}{q} \quad (6.46)$$

The above equation shows that the temperature sensitivity of a solar cell depends on the open circuit voltage of the solar cell, with higher voltage solar cells being less affected by temperature. For silicon, E_{G0} is 1.2, and using γ as 3 gives a reduction in the open-circuit voltage of about 2.2 mV/°C:

$$\frac{dV_{OC}}{dT} = -\frac{V_{G0} - V_{OC} + \gamma \frac{kT}{q}}{T} \approx -2.2 \text{ mV}/^\circ\text{C for Si} \quad (6.47)$$

The short-circuit current, I_{SC} , increases slightly with temperature, since the band gap energy, E_G , decreases and more photons have enough energy to create e-h pairs. However, this is a small effect and the temperature dependence of the short-circuit current from a silicon solar cell is:

$$\frac{1}{I_{SC}} \frac{dI_{SC}}{dT} \approx 0.0006 \text{ per } ^\circ\text{C for Si} \quad (6.48)$$

The temperature dependency FF for silicon is approximated by the following equation:

$$\frac{1}{FF} \frac{dFF}{dT} \approx \left(\frac{1}{V_{OC}} \frac{dV_{OC}}{dT} - \frac{1}{T} \right) \approx -0.0015 \text{ per } ^\circ\text{C for Si} \quad (6.49)$$

The effect of temperature on the maximum power output, P_M , is:

$$P_{Mvar} = \frac{1}{P_M} \frac{dP_M}{dT} = \frac{1}{V_{OC}} \frac{dV_{OC}}{dT} + \frac{1}{FF} \frac{dFF}{dT} + \frac{1}{I_{SC}} \frac{dI_{SC}}{dT} \quad (6.50)$$

$$\frac{1}{P_M} \frac{dP_M}{dT} \approx -(0.004 \text{ to } 0.005) \text{ per } ^\circ\text{C for Si} \quad (6.51)$$

6.4.3 Effect of Light Intensity

Changing the light intensity incident on a solar cell changes all solar cell parameters, including the short-circuit current, the open-circuit voltage, the FF , the efficiency and the impact of series and shunt resistances (figure 6.23). The light intensity on a solar cell is called the number of suns, where 1 sun corresponds to standard illumination at AM1.5, or 1 kW/m². For example a system with 10

kW/m^2 incident on the solar cell would be operating at 10 suns, or at 10X. A PV module designed to operate under 1 sun conditions is called a “flat plate” module while those using concentrated sunlight are called “concentrators”.

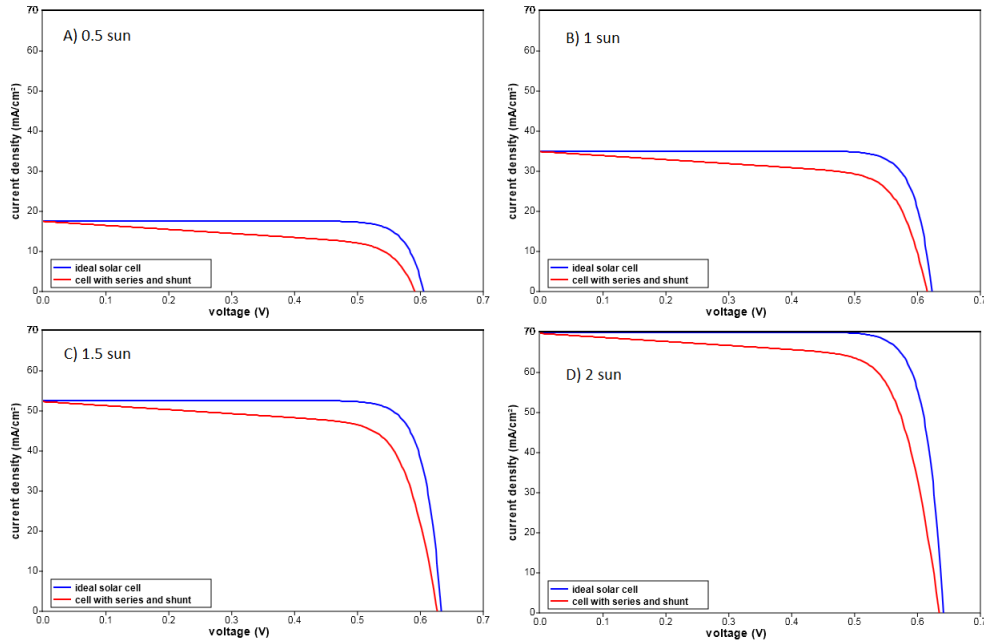


Figure 6.23: The effect of concentration on the IV characteristics of a solar cell. The series resistance has a greater effect on performance at high intensity and the shunt resistance has a greater effect on cell performance at low light intensity.

Concentrators

A concentrator is a solar cell designed to operate under illumination greater than 1 sun. The incident sunlight is focused or guided by optical elements such that a high intensity light beam shines on a small solar cell. Concentrators have several potential advantages, including a higher efficiency potential than a one-sun solar cell and the possibility of lower cost. The short-circuit current from a solar cell depends linearly on light intensity, such that a device operating under 10 suns would have 10 times the short-circuit current as the same device under one sun operation. However, this effect does not provide an efficiency increase, since the incident power also increases linearly with concentration. Instead, the efficiency benefits arise from the logarithmic dependence of the open-circuit voltage on short circuit. Therefore, under concentration, V_{OC} increases logarithmically with light intensity, as shown in the equation below:

$$V'_{OC} = \frac{nkT}{q} \ln \left(\frac{X I_{SC}}{I_0} \right) = \frac{nkT}{q} \left[\ln \left(\frac{I_{SC}}{I_0} \right) + \ln X \right] = V_{OC} + \frac{nkT}{q} \ln X \quad (6.52)$$

where X is the concentration of sunlight. From the equation above, a doubling of the light intensity ($X = 2$) causes a $18mV$ rise in V_{OC} . The cost of a concentrating PV system may be lower than a corresponding flat-plate PV system since only a small area of solar cells is needed.

The efficiency benefits of concentration may be reduced by increased losses in series resistance as the short-circuit current increases and also by the increased temperature operation of the solar cell. As losses due to short-circuit current depend on the square of the current, power loss due to series resistance increases as the square of the concentration.

Low Light Intensity

Solar cells experience daily variations in light intensity, with the incident power from the sun varying between 0 and $1 kW/m^2$. At low light levels, the effect of the shunt resistance becomes increasingly important. As the light intensity decreases, the bias point and current through the solar cell also decreases, and the equivalent resistance of the solar cell may begin to approach the shunt resistance. When these two resistances are similar, the fraction of the total current flowing through the shunt resistance increases, thereby increasing the fractional power loss due to shunt resistance. Consequently, under cloudy conditions, a solar cell with a high shunt resistance retains a greater fraction of its original power than a solar cell with a low shunt resistance [122].

6.4.4 Ideality Factor

The ideality factor of a diode is a measure of how closely the diode follows the ideal diode equation. The derivation of the simple diode equation uses certain assumption about the cell. In practice, there are second order effects so that the diode does not follow the simple diode equation and the ideality factor provides a way of describing them.

Recombination mechanisms

The ideal diode equation assumes that all the recombination occurs via band to band or recombination via traps in the bulk areas from the device (i.e. not

in the junction). Using that assumption the derivation produces the ideal diode equation below and the ideality factor, n , is equal to one.

$$I = I_L - I_0 \left[\exp \left(\frac{qV}{nkT} \right) - 1 \right] \quad (6.53)$$

However recombination does occur in other ways and in other areas of the device. These recombinations produce ideality factors that deviate from the ideal. Deriving the ideal diode equation by considering the number of carriers the need to come together during the process produces the results in the table 6.2.

Table 6.2: Ideality factor of non ideal solar cell

Recombination Type	Ideality factor	Description
SRH, band to band (low level injection)	1	Recombination limited by minority carrier
SRH, band to band (high level injection)	2	Recombination limited by both carrier types
Auger	2/3	Two majority and one minority carriers required for recombination
Depletion region (junction)	2	Two carriers limit recombination

Chapter 7

Experimental Set-Ups for Solar Cells

The characterization of standard silicon solar cells ($15.6 \text{ cm}^2 \times 15.6 \text{ cm}^2$ area) requires dedicated instrumentation since the current level and capacitance are different respect to standard microelectronic devices. The current level can easily exceed 8 A and the parasitic capacitance can be 1-5 μF .

The choice of dedicated instrumentation is of particular importance since the extracted parameters (efficiency, η and fill factor, FF) can be influenced by the measurement process. The high current level of a single solar cell introduces other problems if the measurement results have to be detailed in all the current ranges (from μA to Amps). Dedicated measurement set-ups were developed in order to resolve all these problems and to obtain right results not affected by the used instrumentation.

7.1 IV characterization Set Up

7.1.1 Dark IV curve

The extraction of the IV curve of a silicon solar cell requires a detailed reading of the current in all the ranges from μA to 9 Amps. The measurement are performed using a 4-wires technique in order to delete all the effects introduced by the interconnections. The selected instrument was the Keithley 2651A that can measure a single solar cell but also an entire module of 50 solar cells.

The extraction of a clean IV curve in all the current ranges was obtained dynamically allocating the current range of the instrument. A dedicated labView

program was developed to obtain this result. In Fig. 7.1 the sketch of the program is presented. The program allows to obtain the direct and the reverse characterization enabling the different panels. The direct and reverse curves can be divided in different steps (“Step Totali Diretta” and “Step Totali Inversa”) dynamically allocating the number of points for each step (“Punti”) and the Voltage and Current ranges (“Range V” and “Range I”). This increases the precision of the measure in all the current range. The program permits to set the delay time (“Delay Time Diretta” and “Delay Time Inversa”) that can be used to set the time before the measure of each point.

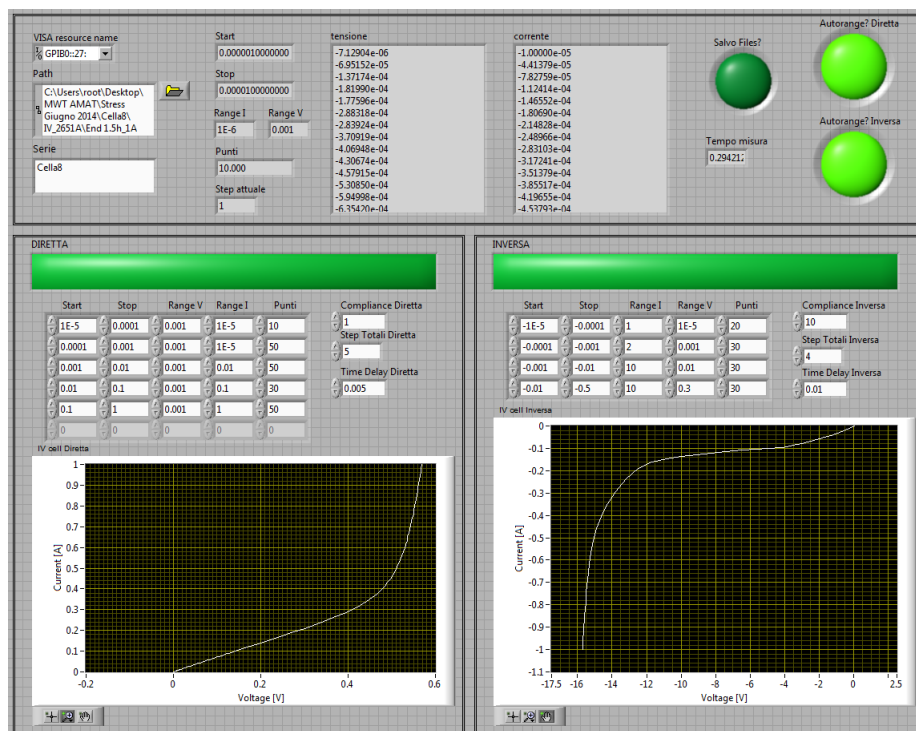


Figure 7.1: Picture of the LabView program developed to obtain the IV curve of a silicon solar cell.

An example of the extracted IV curve is presented in Fig. 7.2. The direct measure shows the great precision of the measure in all the current ranges: in this particular case from $1 \mu\text{A}$ to 10 Amps while the reverse measure shows the breakdown of the silicon diode that is near -13 Volts. The high capacitance of the solar cell lead to the result visible in the zoom of Fig. 7.2. Increasing the delay time the IV curve shifts down in the range of 0-0.1V. We selected a 5 ms delay time for the characterization in order to avoid all the capacitive effects visible in the measurements made with too short delay times.

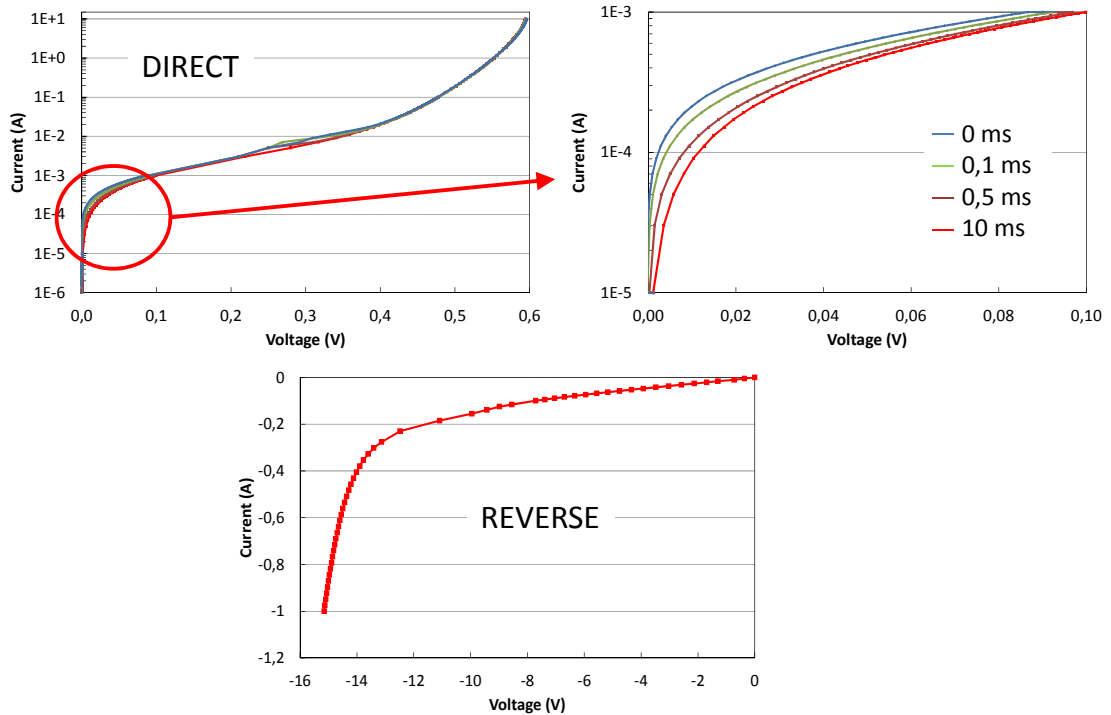


Figure 7.2: IV curves extracted using the 2651A and the developed LabView program.

7.1.2 Light IV curve

The light IV measurements are extracted using two different systems. The first is the Loana PV Tools commercial system and the second is a LED solar simulator developed in cooperation with Applied Materials SRL. In this paragraph I will simply explain the developed LabView program of the LED solar simulator and not the complete systems. You can refer to the respectively data sheet for more accurate description.

The system is composed of the LED solar simulator, the Keithley 2651A source meter and a thermal chuck used to maintain the solar cell to the 25 °C standard temperature. Fig. 7.3 shows the timing of the measure. The Keithley 2651A is set for the measure and then is placed in hold of the solar simulator trigger. The solar simulator is switched on and after the stabilization period (10 ms), it triggers the keithley 2651A that performs the measure of the IV under illumination. Since the stabilization of the LED lamp is guaranteed for 300 ms the sweep is repeated different time with different biasing of the cell in order to reconstruct the entire IV curve with a sufficient number of points.

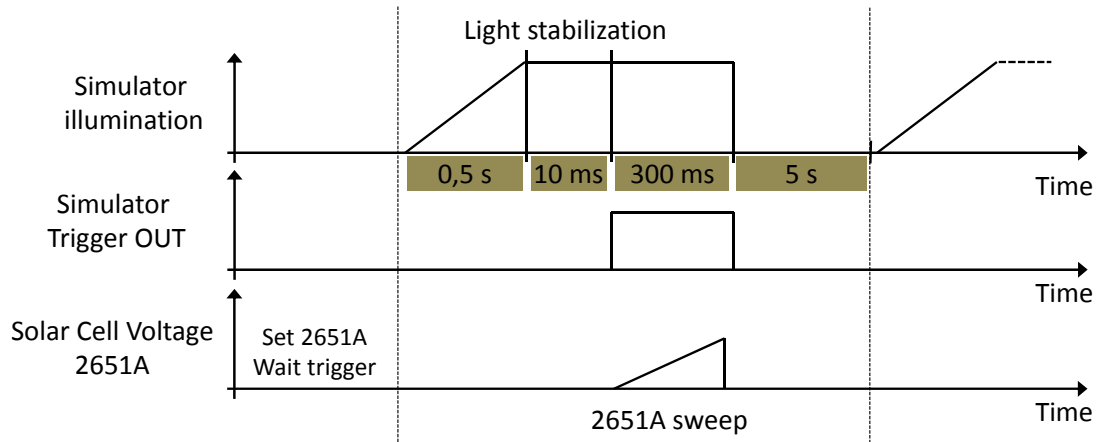


Figure 7.3: Timing of the light IV measure performed with the LED solar simulator.

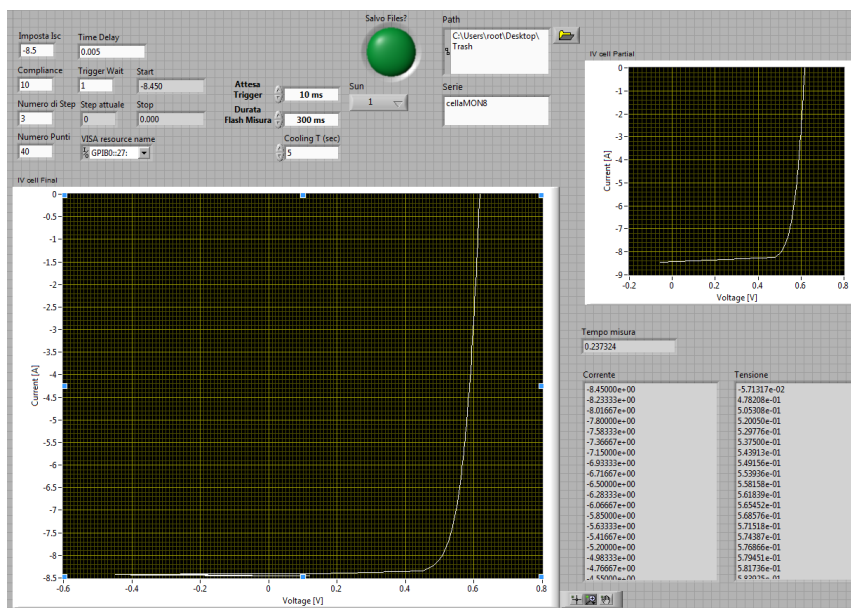


Figure 7.4: Picture of the LabView program developed to obtain the IV curve of a silicon solar cell under illumination.

A dedicated LabView program was developed in order to automate the different sequential measurements (Fig. 7.4). The program requires the I_{SC} value (“Imposta Isc”). The source meter is used like a current generator that forces the current into the solar cell and measures the voltage due to the high current value. The IV is divided in different flash steps (“Numero di Step”) as described above. For each step the 2651A is able to capture about 40 points (“Numero Punti”) remaining within the flash duration. After each flash a period of 5 seconds is

waited in order to cool down the entire system and to avoid any deviation of the solar cell temperature. The program shows the partial IV curve performed during the characterization (“IV Cell Partial”) and also the final reconstructed curve (“IV Cell Final”). Note that the delay time (“Time Delay”) is set to 5 ms as described in the previous paragraph. The LED solar simulator is able to set the illumination level that can be set with the control “Sun” from a value of 0.3 sun up to 1.2 sun.

7.2 Thermography Characterization Set Up

In order to evaluate the presence of hot spots in reverse bias, a dedicated measurement set up was build up. In conventional thermography setups, a dc bias is applied to the cell and a thermographic image is acquired. The use of dc bias can produce a detrimental effect on the results of thermography measurements, since - due to the long measurement times - heat can spread on the cell area, negatively affecting the spatial resolution of the measurement. We have realized a setup for “synchronous-pulsed” thermal characterization, that allows for a better spatial resolution, without the need of a more expensive Lock-in thermography system [123]. Fig. 7.5 shows a schematic block diagram of the measurement setup.

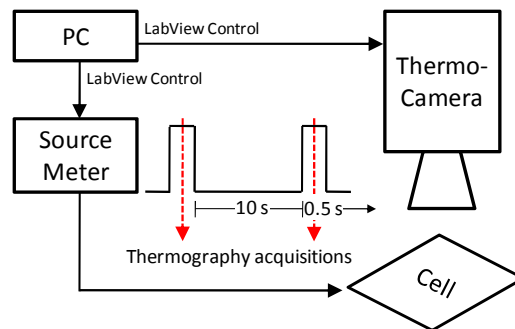


Figure 7.5: Schematic diagram of spatially resolved thermography measurement set up.

A 500 ms bias pulse is applied on the cell in reverse conditions and a spatially resolved thermography image is acquired immediately after the voltage has stabilized. Then a zero voltage is applied for about ten seconds, to cool down the cell, and then another measurement can be taken. The final image is obtained as the average of over ten images in order to reduce noise. This kind of measurement setup is used to reduce self-heating of the cell during the measurements, thus

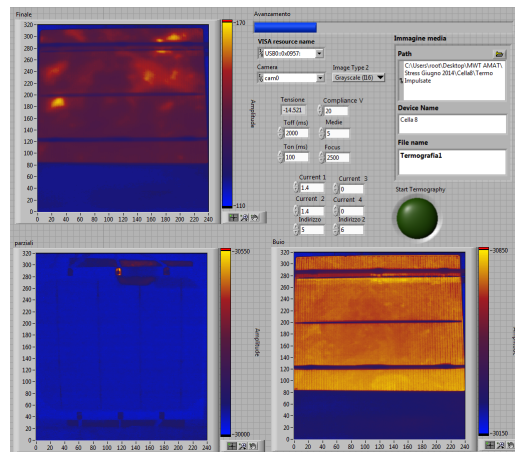


Figure 7.6: Picture of the LabView program developed to obtain the thermographic image of a solar cell.

increasing spatial resolution. The dedicated LabView program is visible in Fig. 7.6

7.3 Electroluminescence and Photoluminescence Characterization Set Up

The luminescence of a silicon solar cell can be detected using an InGaAs Camera with a spectral range of 950 nm - 1650 nm. In fact the emission of a silicon solar cell is near the silicon Energy Gap (1100 nm). The emission of possible defects (at longer wavelengths) can be identified using appropriate optical filters capable of eliminating the shorter wavelengths.

Electroluminescence (abbreviated as EL) is an optical phenomenon and electrical phenomenon in which a material emits light in response to the passage of an electric current or to a strong electric field. In silicon solar cells the EL can be extracted with a positive current of 5 A and over.

Fig. 7.7 (a) and (b) show the Electroluminescence obtained on a silicon solar cell with positive current of 5 A and 8 A respectively. The Electroluminescence signal can be related to the capabilities of the solar cell to emit light as a result of the passage of current. This process is exactly the reverse process of converting light energy into electrical energy. The EL permits to identify defects and all areas of the cell that are not reached by the current through the busbars.

Photoluminescence (abbreviated as PL) is light emission from any form of

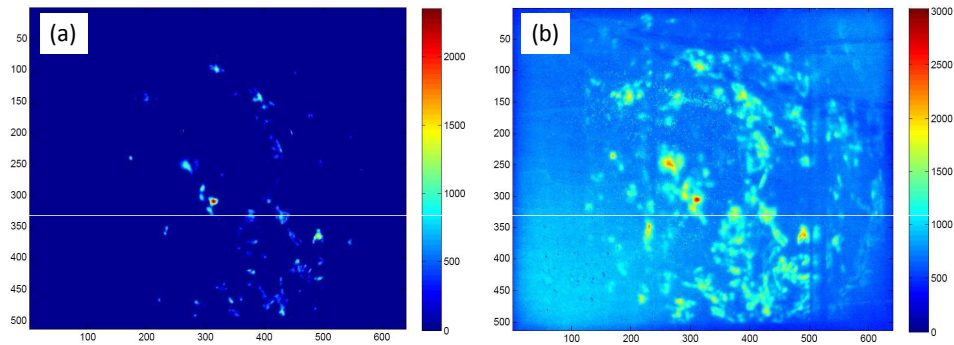


Figure 7.7: Electroluminescence images of a silicon solar cell with direct current of 5 A (a) and 8 A (b).

matter after the absorption of photons (electromagnetic radiation). It is one of many forms of luminescence (light emission) and is initiated by photoexcitation (excitation by photons), hence the prefix photo. Following excitation various relaxation processes typically occur in which other photons are re-radiated.

The PL in silicon solar cell is very difficult to obtain. A LED array was opportunely built in order to excite the silicon solar cell. The light stimulus was chosen at 850 nm in order to appropriately excite the cell within its absorption band. The emission can be observed above 1100 nm (band gap of silicon). To avoid the acquisition of the stimulus signal (850 nm), appropriate optical filters should be used, in order to isolate only the signal actually emitted from the photovoltaic cell. Since the emitted signal is very weak, three 1100 nm OD4 notch filters were used to filter the signal appropriately.

Fig. 7.8 (a) and 7.8 (b) show the PL signal obtained on a silicon solar cell with a current of 0.8 A on the LED array and 2 and 3 filters respectively with 1 second of aperture of the camera shutter. Fig. 7.8 (c) shows the PL signal with 0.8 A on the LED array and 3 filters with 2 second of aperture of the camera shutter. The PL signal can be related to the capabilities of each single point of the solar cell of converting the light absorbed energy into radiation energy. So it can be related to defectively of the solar cell without taking into account the spreading of the current since the stimulus is optical and not electrical.

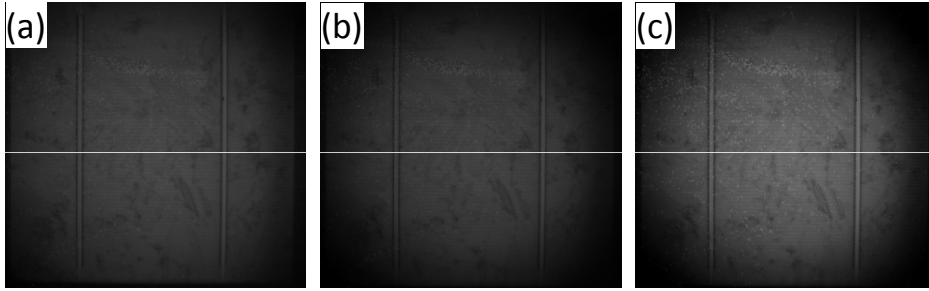


Figure 7.8: Photoluminescence images of a silicon solar cell with 0.8 A on the LED array, 2 filter and 1 second of aperture (a), 0.8 A on the LED array, 3 filter and 1 second of aperture (b) and 0.8 A on the LED array, 3 filter and 2 second of aperture (c).

7.4 External Quantum Efficiency and Reflectance (LOANA System)

The internal quantum efficiency (IQE) is not measured directly but calculated from:

- the external quantum efficiency (EQE)
- the integral reflectance (REFL)

The calculation is done with the program LASSIE and described in detail in the Lassie manual. This section only describes the measurement of EQE and REFL. The external quantum efficiency (EQE) is defined as the fraction of charge carriers collected per incident photon (ϕ_{in})

$$EQE(\lambda) = \frac{J_{SC}(\lambda)/q}{\phi_{in}(\lambda)} \quad (7.1)$$

and is determined by measuring the short circuit current response to illumination with monochromatic light.

The samples EQE_{sample} is determined relative to a reference sample with known EQE_{cal} . We use the term baseline for the measurement on the reference cell. The signals ($S_{Jsc,sample}$ and $S_{Jsc,cal}$) from baseline and sample measurement are divided by the signal from the monitor diode (S_{mon}) which corrects fluctuation in the light intensity between calibration and measurement. The sample's EQE is then calculated as

$$EQE_{sample}(\lambda) = EQE_{cal}(\lambda) \frac{S_{Jsc,sample}(\lambda)}{S_{Jsc,cal}(\lambda)} \frac{S_{mon,cal}(\lambda)}{S_{mon,sample}(\lambda)} \quad (7.2)$$

7.4 External Quantum Efficiency and Reflectance (LOANA System) 19

where:

- EQE_{sample} = desired EQE of the sample
- EQE_{cal} = given EQE of the internal reference cell
- $S_{Jsc,sample}$ = measured signal of the sample
- $S_{Jsc,cal}$ = measured signal of the internal reference cell
- $S_{mon,cal}$ = measured monitor signal of the internal reference cell
- $S_{mon,sample}$ = measured monitor signal of the sample

The integral reflectance comprises both the diffuse specular components and is also measured with monochromatic illumination and an integrating sphere. It is defined as the fraction of light reflected per incident photon.

Both EQE and reflectance are usually measured on an area of 20 mm x 20 mm (figure 7.9) or scanned on a area up to 156 mm x 156 mm. For special investigations the light can be focused to a approx. 1 mm x 3 mm spot. An

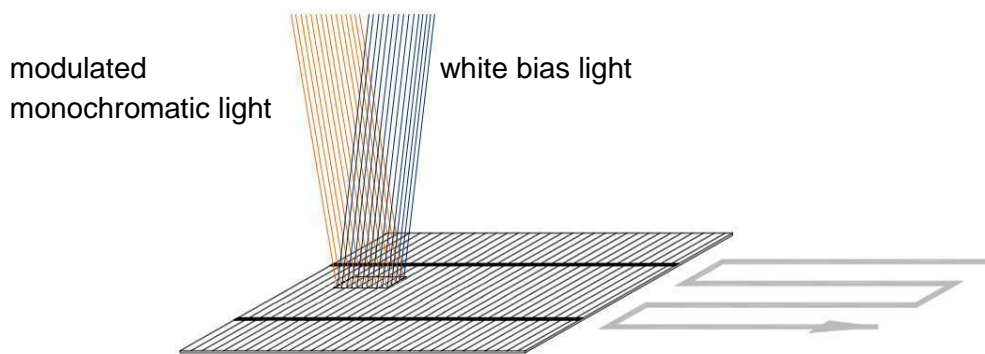


Figure 7.9: Example of EQE scan.

example of EQE is reported in figure 7.10

The reflectance spectrum is measured with help of an integrating sphere (figure 7.11). It has a diameter of 11 cm and its inside is coated with a diffuse reflecting $BaSO_4$ coating. The sphere is located in a distance of about 300 μm between the solar cell and the sample port. Monochromatic light enters the sphere through the input port and illuminates the solar cell over 20 mm x 20 mm. The reflected light is collected by the sphere and reflected internally until is finally measured by one of the two detectors (Si and Ge). To detect both the specularly and the diffusely reflected light the angle of incidence is tilted by 8 degrees. This

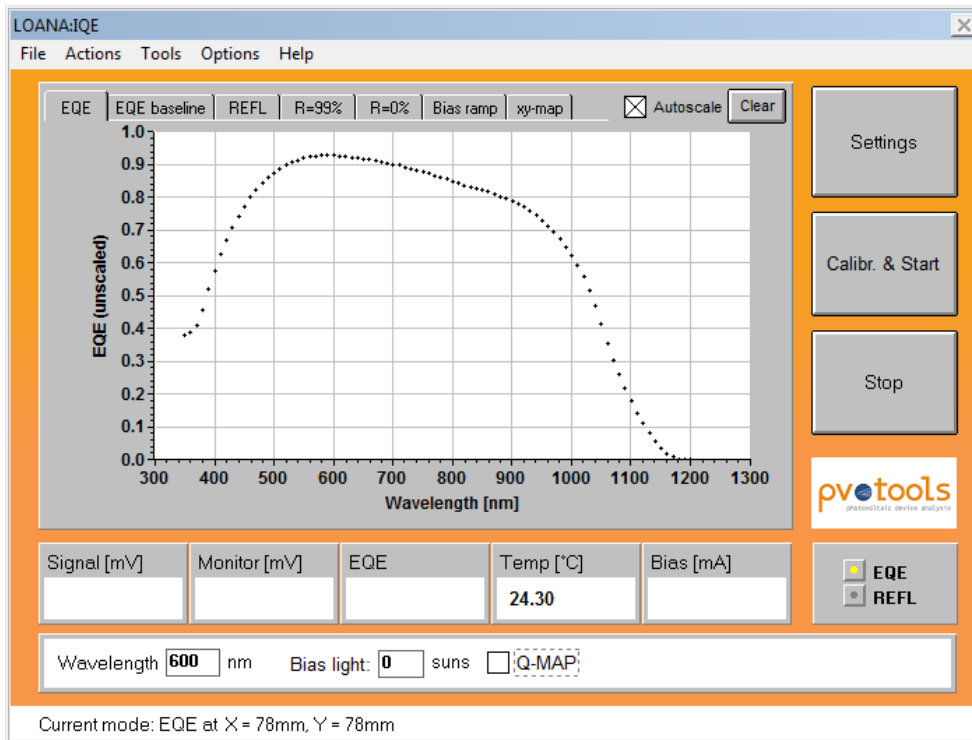


Figure 7.10: EQE example. Loana Panel.

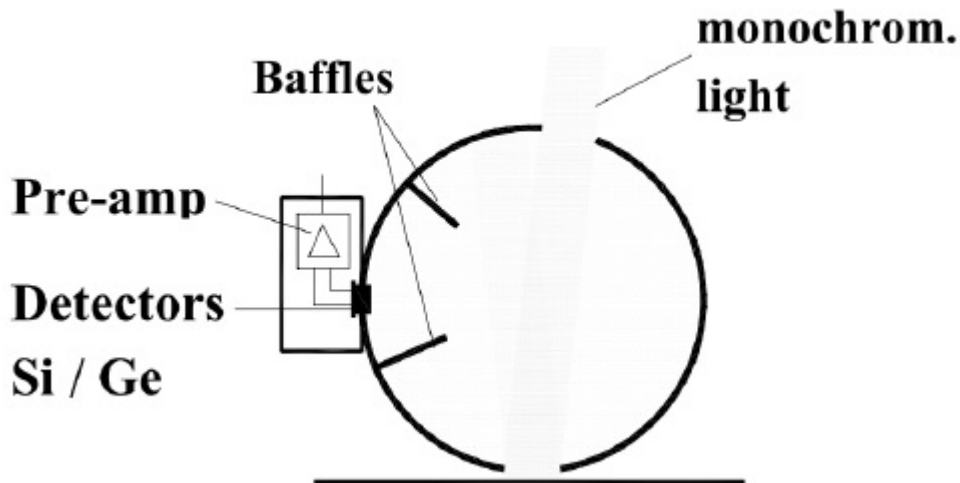


Figure 7.11: Integrating sphere

prevents the specular component from leaving the sphere through the input port. Internal baffles ensure, that the light that hits the detector has been reflected by the walls at least once (and at least twice for the specular component). Activat-

7.4 External Quantum Efficiency and Reflectance (LOANA System) 21

ing the reflectance mode moves the sphere automatically into position. Otherwise the sphere moves automatically into a parking position where a cover protects the sphere against dust. This position is 1 cm higher to prevent damages from the table movement. In order to measure the full area integral reflectance by scanning a distance around 300 μm between sample and integrating sphere must be maintained. Therefore not all of the reflected light is collected by the sphere. This signal loss is largely compensated when the same distance is used for the calibration and the sample measurement.

Chapter 8

PV-CELLS, Experimental Results

8.1 Effect of shunt resistance on the performance of mc-Silicon solar cells

In this paragraph we discuss the effect of shunt resistance on the electro-optical characteristics of multicrystalline silicon (mc-Si) solar cells at different illumination levels. The analysis is based on combined electro-optical characterization and thermographic measurements of solar cells with similar efficiencies, but with different shunt resistance levels. In order to understand how the shunt resistance can affect the performance of mc-Si solar cells, a special setup for J-V characterization at several illumination levels was developed. Results indicate that:

- A low shunt resistance is strongly correlated to the presence of hot spots, which can be identified by means of infrared thermography.
- Solar cells with different shunt resistance levels can show significantly different fill factors and efficiencies, particularly at low irradiation levels. This can strongly influence the reliability of modules at low illumination conditions.
- The electrical characteristics of mc-Si solar cells can be modeled with good results, by considering the equivalent two-diode electrical model and solving it by a circuit simulator like SPICE.

Despite the recent improvements in manufacturing technology, the fabrication of solar cells is complicated by a number of factors, including the presence of

crystallographic defects, material inhomogeneities, dislocations and microcracks [124]. These issues influence the electrical properties of the junction and lead to a degradation of the conversion efficiency. In multicrystalline silicon solar cells, the presence of defects causes the formation of parasitic shunting paths with low resistance [125]. These paths can be identified as hot spots in Infrared Thermographic Measurements, carried out on reverse-biased solar cells [123]. Another important open issue is the partial shading, or in general the non-uniform illumination level, of photovoltaic (PV) array [126], constituted by cells with different electrical characteristics. For this reason, it can be very useful to understand how shunt resistance can affect the properties of solar cells at varying irradiance levels [127]. Finally, the presence of a shunting path on a solar cell can affect the reliability of the cell itself, since it leads to a localized over-heating of the device. In order to investigate problems related to the presence of shunting paths, in this paragraph mc-Si solar cells with similar electrical parameters were analyzed, but with different shunt resistances, by studying their behavior at different light levels using the LED-based solar simulator. Moreover the two-diodes equivalent circuit model for the different cells was extracted. We show that this model provides a reliable fitting of the characteristics of the cells, with both high and low shunt resistance.

8.1.1 Experimental details and results

The cells have an area of 156 mm x 156 mm. In the following, the results obtained on three representative samples (referred to as “Cell A”, “B” and “C” in the paragraph) are reported, featuring low, intermediate and high shunt resistance, respectively. The main electrical parameters of these three cells are reported in Table 8.1. We made three typologies of measurements: (1) Dark I V characterization, (2) Thermographic characterization and (3) I V curves at different light levels using the LED-based solar simulator.

Dark I V characterization

Using a source meter we made a dark I V characterization of the three cells with different levels of shunting (see Fig. 8.1). In order to extrapolate a reliable I-V curves in solar cell with high shunt current components, it is important to adapt dynamically the current measurement range. This is necessary because the wide current range (from μ Ampere to Ampere) doesn't permit a good resolution for low values of current. The current adjustment method has produced good results for all the current range as shown in Fig. 8.1 for any kind of shunt

Table 8.1: Main parameters of analyzed sola cells at 1.18 sun.

CELL	V_{OC} [V]	I_{SC} [A]	E_{ff} [%]	FF [%]	V_{PW} [V]	I_{PW} [A]	P_W [W]	R_{SH} [Ω]
A	0.58	9.4	11.7	60.7	0.46	7.19	3.31	0.27
B	0.59	9.4	13.6	68.9	0.46	8.29	3.85	1.19
C	0.59	9.5	14.4	73.4	0.46	8.79	4.09	78.6

V_{OC} = Open circuit voltage [V]

I_{SC} = Short Circuit Current [A]

E_{ff} = Efficiency [%]

FF = Fill Factor [%]

V_{PW} = Voltage @ Maximum Power [V]

I_{PW} = Current @ Maximum Power [A]

P_W = Maximum Power [W]

R_{SH} = Shunt Resistance [Ω]

cell. The measurements were carried out with a four wire technique in order to minimize the effect of the parasitic impedance of the cables. The different shunt resistances of the cells are clearly recognizable in the reverse-bias region of the curves. Cell A has a low shunt resistance, hence, in reverse biasing condition, the characterization was stopped at -1 V in order to avoid a large current flow.

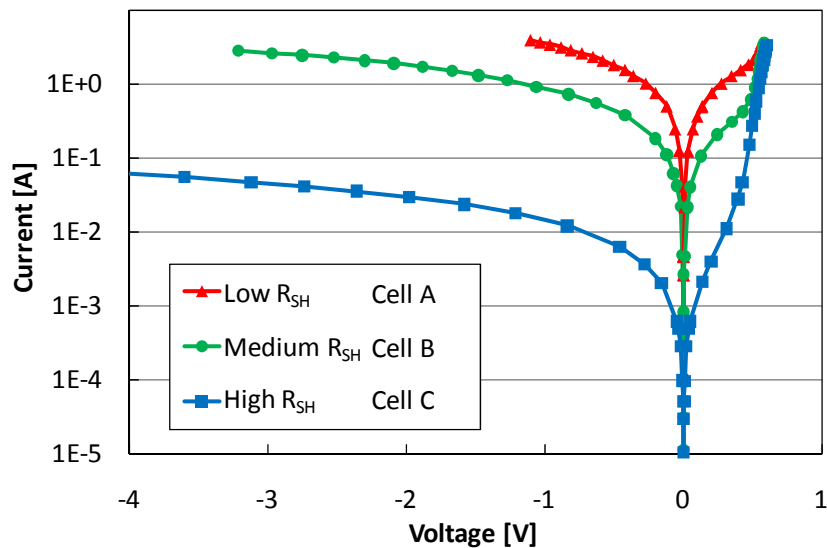


Figure 8.1: Dark I-V characteristics of the three solar cells.

Thermographic characterization

In Fig. 8.2 we report the spatially resolved thermography of two cells using the experimental set up explained in the measurement set up chapter. Cell A

presents a localized hot spot coinciding with the localized temperature increase, visible in the picture (about 25 °C). Cell C presents a diffused heating of one or two degrees, randomly distributed on device area, and this is in agreement with the higher value of the shunt resistance. The localized temperature increase (occurring at the hot spots) negatively influences the behavior of an entire PV system, in particular it can lead to a crack of the protection over the PV-module. For this reason it is important to prevent the formation of shunt paths during the fabrication process and then to prevent the biasing of the single cell in reverse conditions, which can result in the generation of hot spots. This condition can be present in shaded cells or in strings of cells with different native shunt resistance.

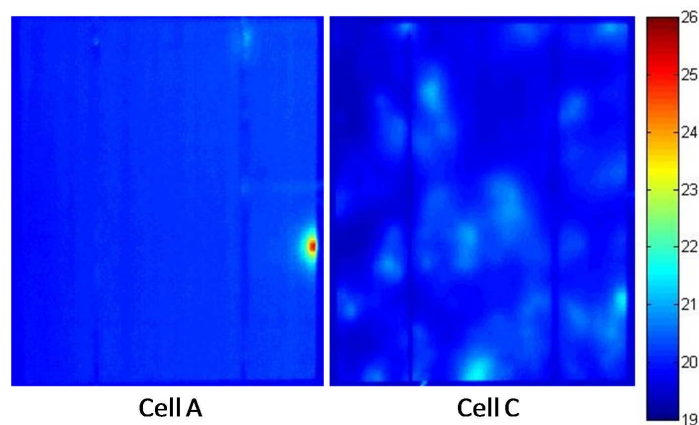


Figure 8.2: Synchronous-pulse thermography image of two analyzed cells.

I-V curves at different illumination levels

The LED-based solar simulator can produce an arbitrary illumination level between 0.2 and 1.2 sun, with class A for spectral shape, spatial uniformity, and temporal stability. Fig. 8.3 shows the I-V curves obtained by measuring the three cells at four different illumination levels. It is possible to see how the difference in the shunt resistance affects the parameters of the cells: lower shunt resistances correspond to lower current levels, for the same voltage.

Fig. 8.4 summarizes the effect of shunt resistance on the electrical performance of the cells at different illumination levels: while in cell C the fill factor is practically constant at different light levels, for cell A it steeply decreases with the illumination level. This problem can influence the performance of the single cell and the functionality of the entire PV module because in low illumination condition the shunt resistance leads to a degradation of the fill factor and hence of the

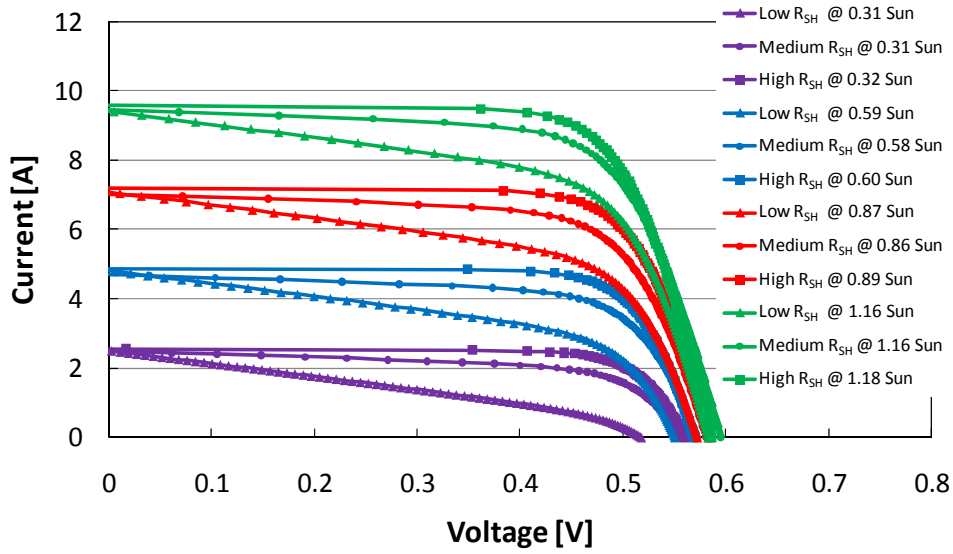


Figure 8.3: Illuminated I-V curves at different light levels using a LED-based solar simulator.

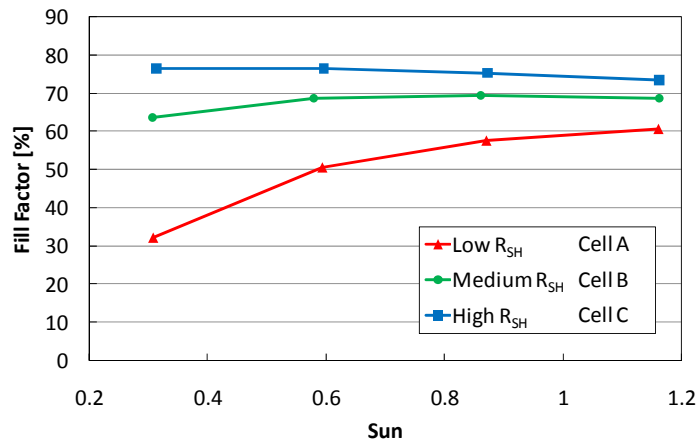


Figure 8.4: Fill Factor of the three cells at different levels of irradiance.

efficiency. Therefore the shunt resistance is a fundamental parameter to be considered in the “in-line” selection procedure of manufacturing production process.

8.1.2 Modeling of the solar cells

In order to provide a more detailed understanding of the impact of shunt resistance, we modeled the solar cell characteristics by means of the standard two-diodes equivalent circuit schematically shown in Fig. 8.5 [128].

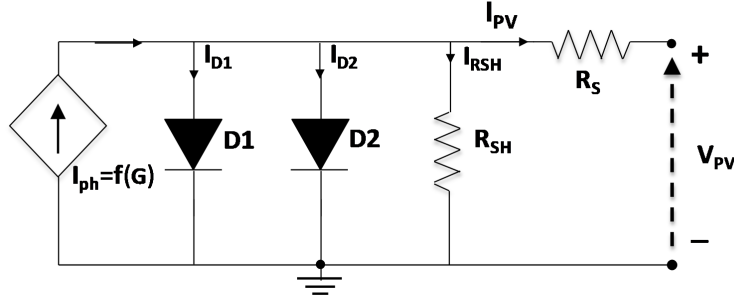


Figure 8.5: Two-diodes equivalent circuit of the solar cell.

The output current I_{PV} provided by the PV cell under illumination is given by:

$$I_{PV} = I_{ph} - I_{D1} - I_{D2} - I_{RSH} \quad (8.1)$$

The diodes D_1 and D_2 account for the recombination mechanisms in the PV cell. Particularly, the provided currents I_{D1} and I_{D2} are given as:

$$I_{D1} = I_{01} \left[\exp \left(\frac{V_{PV} - I_{PV} R_S}{\eta_1 V_T} \right) - 1 \right] \quad (8.2)$$

$$I_{D2} = I_{02} \left[\exp \left(\frac{V_{PV} - I_{PV} R_S}{\eta_2 V_T} \right) - 1 \right] \quad (8.3)$$

where η_1 , η_2 are the ideality factors and V_T is the thermal voltage. The current I_{RSH} represents the leakage current of the PV cell, which is accounted by the shunt resistance R_{SH} . The series resistance R_S models the voltage drop across the PV cell produced by the current I_{PV} . I_{ph} accounts for the photocurrent generated at different illumination levels, which is modeled with the function

$$f(G) = J_{ph0} \cdot A_{cell} \cdot G/G_0 \quad (8.4)$$

where G_0 is the solar irradiation at 1 sun (1000 W/m^2), J_{ph0} is the photocurrent density at 1 sun and A_{cell} is area of the cell. It is worth noting that the ratio G/G_0 represents the number of sun. LTSpice from Linear Technology Corporation was adopted to perform the circuit simulations of Fig. 8.5. The several components of the equivalent circuit, represented in Fig. 8.5, influence the dark I-V curve at different voltage level (see Fig. 8.6). For low forward voltage, the effect of the shunt resistance is typically dominant. By increasing the forward voltage, the contribute of the diodes D1 and D2 characterizes the behavior of

the solar cell. Finally, at very high forward voltage the series resistance limits the current through the cell. The dark I-V curves, generated with the equivalent circuit of Fig. 8.5 (considering $I_{ph} = 0$), are compared with experimental data in Fig. 8.6.

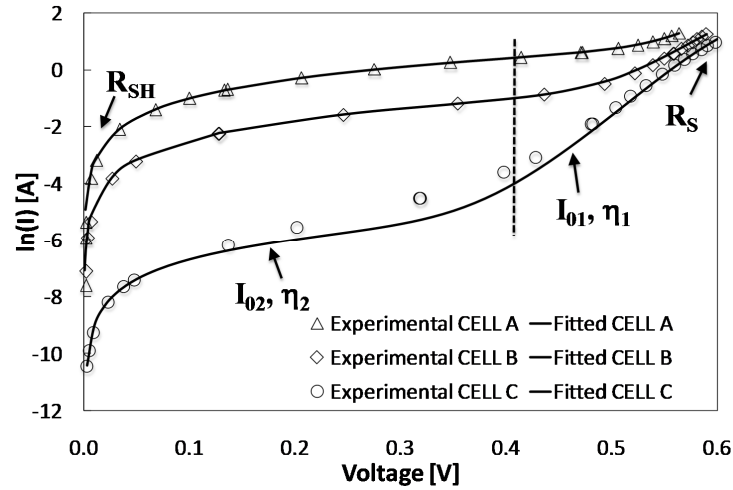


Figure 8.6: Comparison between experimental and modeled dark I-V.

The parameters extracted for each cell are reported in Table 8.2. Circuit simulations were performed as a function of the illumination level, according to 8.4 and to the parameters reported in Table 8.2. Table 8.3 summarizes the output electrical parameters of the solar cell at 1.18 sun. These results are in agreement with the experimental analysis reported in Table 8.1. Circuit simulations are also implemented in order to study the impact of the shunt resistance on the fill factor. In Fig. 8.7 we analyze the behavior of cell C for different value of the shunt resistance. The reduction of the shunt resistance leads to a reduction of the fill factor. Moreover, it is possible to observe that at lower illumination level we find a higher degradation of the fill factor when the shunt resistance is decreased.

Table 8.2: Parameters extracted from the experimental dark I-V curves.

CELL	J_{01} [A/cm ²]	η_1	J_{02} [A/cm ²]	η_2	R_{SH} [Ω]	R_S [Ω]
A	$2 \cdot 10^{-12}$	1	$1.7 \cdot 10^{-9}$	1.51	0.265	$4 \cdot 10^{-3}$
B	$1.99 \cdot 10^{-12}$	1	$2.15 \cdot 10^{-9}$	1.478	1.16	$3.75 \cdot 10^{-3}$
C	$1.15 \cdot 10^{-12}$	1	$1.1 \cdot 10^{-9}$	1.49	80	$6 \cdot 10^{-3}$

Table 8.3: Electrical output parameters obtained from the simulated solar cells under 1.18 sun.

CELL	V_{OC} [V]	I_{SC} [A]	E_{ff} [%]	FF [%]
A	0.58	9.4	11.7	60.8
B	0.59	9.4	14.06	71.6
C	0.59	9.5	14.2	72.8

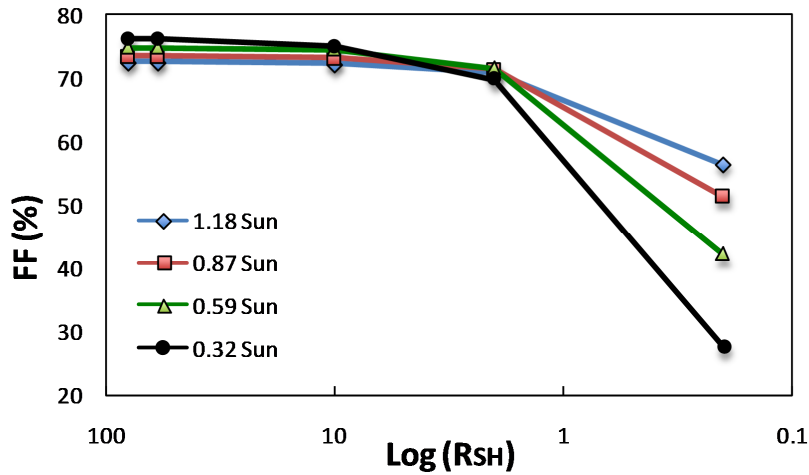


Figure 8.7: FF vs. R_{SH} as a function of the illumination level.

8.2 Simulation of string of cells: effect of shunt resistance of the performances

This paragraph presents an extensive study of how the presence of a solar cell with low shunt resistance can influence the performance and reliability of a solar panel [129]. The analysis is based on simulations, and provides the following results:

- The presence of a cell with low shunt resistance can significantly modify the efficiency of a panel;
- This effect is particularly prominent when the shunted cell is partially shaded: in this case, the shunt resistance of the cell represents a load for most of the power generated by the panel;
- Under these conditions, the shunted cell can significantly degrade: in fact, the (small-size) shunt paths are crossed by a high current density, generated by the other cells in the panel, thus reaching high temperature levels.

The study presents an extensive analysis of the behavior of a string constituted by the series connection of several (multi-crystalline) silicon solar cells, in which one of the cells has a low shunt resistance. It is also analyzed the case in which the shunted cell is totally or partially shadowed.

Simulations data are obtained by the two-diode model, whose theoretical background will be extensively discussed. The model is applied in its standard form for a solar cell with high shunt resistance and is revisited for a solar cell with very low shunt resistance. The application of the two diode model on high and low shunt resistance solar cells is very important since the shunt resistance of single solar cells can modify the performance of an entire module [130]. Results of simulations conducted on a string of 21 cells show that when in a module a low shunt resistance cell is partially shaded, the cell itself is crossed by high reverse current and the whole module results to be still functioning, generating a certain current. Since the reverse-biased cell is crossed by the photogenerated current thanks to the presence of the shunt resistance, a power dissipation can take place and is observed to be in the order of tens of Watts.

8.2.1 Two diode model for the simulation of solar cells

The main parameters of the analyzed solar cells were extrapolated from the I-V characteristics using the method described in [131]-[132]. According to theory, the dark I-V curve can be fitted with one-diode model or with the more complex two-diodes model and the main electrical parameters are extracted: series resistance (R_S), shunt resistance (R_{SH}), diodes ideality factors (η_1 and η_2) and saturation currents (I_{S1} and I_{S2}). The extraction of these parameters is of crucial importance, since they play an important role in the determination of the cell fill factor and efficiency. For instance, a substantial improvement of the solar cell performance is obtained by reducing the series resistance of the cells. An accurate estimation of the main cell parameters is therefore important for the optimization of cell performance, and for the definition of advanced processing and technological parameters. In the following we briefly summarize the procedure used for the extrapolation of the main cell parameters: the fitting procedure requires four consecutive linear regressions over the experimental data. The first is used to estimate the series resistance (R_S), the second provides the first diode contribution (I_{S1} and η_1), the third provides the shunt resistance (R_{SH}) and finally the fourth the second diode evaluation (I_{S2} and η_2). The linear regression is performed using the software MATLAB. The values extracted by the fitting

procedure are validated according to the following method: firstly the I-V curves of the devices under 1 sun illumination are calculated, on the basis of the parameters extrapolated from the dark I-V measurements, and then the calculated curves are compared to the experimental ones (obtained from light I-V curves), to verify the correspondence between calculated and measured data. Light I-V simulations are performed using the commercial software AIM-Spice. In Fig. 8.8 the standard two diode model is presented. When the cell is illuminated (Fig. 8.8 a), a photocurrent I_{PH} is generated, and the solar cell is modeled like a circuit with a current generator, two diodes, a shunt (R_{SH}) and a series resistance (R_S). When the cell is in dark, the generated photocurrent is zero and the cell is modeled only with two diodes and two resistors (Fig. 8.8 b).

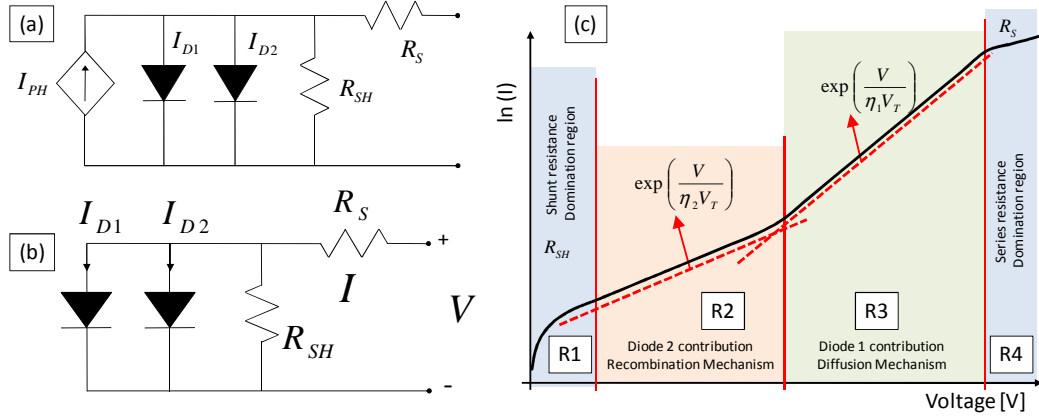


Figure 8.8: Electrical circuits for the (a) light and (b) dark cell modelization. The contributions of each diode and resistance can be identified into the dark current voltage characteristic (c).

The standard two diode fitting procedure is made by splitting the dark I-V curve into four regions [133]-[134] as in Fig. 8.8 c: the two on the right (marked with R3 and R4) are used to fit the first diode parameters (I_{S1} and η_1) and the series resistance, the one in the middle (marked with R2) is used for the second diode parameters (I_{S2} and η_2) responsible of the recombination mechanism and finally the leftmost (marked with R1) is dominated by the shunt resistance. The resulting equation in dark conditions (Fig 8.8 b) is given by:

$$I = I_{D1} + I_{D2} + I_{RSH} = I_{S1} \cdot \left(\exp \left(\frac{V - R_S I}{\eta_1 V_T} \right) - 1 \right) + I_{S2} \cdot \left(\exp \left(\frac{V - R_S I}{\eta_2 V_T} \right) - 1 \right) + \frac{V - R_S I}{R_{SH}} \quad (8.5)$$

For the parameters extraction, we separate the curve in four different parts (Fig. 8.8 c): in the first region ($V = 0 - 0.15$ V) the dark current is dominated

by the shunt resistance; in the second one ($V = 0.2 - 0.4$ V), the current is dominated by the recombination mechanism; in the third region ($V = 0.4 - 0.6$ V), diffusion mechanism dominates. From 0.6 V upwards, the series resistance is the main domination parameter.

The choice of the boundaries of the four regions strongly influences the procedure results. For this reason the results of the dark I-V fitting have to be validated a posteriori by light I-V comparison. The model gives reliable results when only the region R1 is affected by the shunt resistance, in this case the current in the regions R3 and R4 of the I-V curve can be modeled using the simplified equation:

$$I = I_{D1} = I_{S1} \cdot \left(\exp \left(\frac{V - R_S I}{\eta_1 V_T} \right) - 1 \right) \cong I_{S1} \cdot \left(\exp \left(\frac{V - R_S I}{\eta_1 V_T} \right) \right) \quad (8.6)$$

which takes into account only the contribution of the first diode and the series resistor, while the shunt effect is neglected. For shunt resistance values greater than 10-15 Ω , the curves are fitted using the procedure described in the following:

$$\ln(I) \cong \ln(I_{S1}) + \frac{V - R_S I}{\eta_1 V_T} \quad (8.7)$$

By taking a point (V_0, I_0) of the I-V curve, we can write the following relation:

$$\ln(I) - \ln(I_0) = \frac{V - R_S I}{\eta_1 V_T} - \frac{V_0 - R_S I_0}{\eta_1 V_T} \quad (8.8)$$

$$\ln(I) - \ln(I_0) = \frac{V - V_0}{\eta_1 V_T} - \frac{R_S}{\eta_1 V_T} (I - I_0) \quad (8.9)$$

$$\frac{\ln(I) - \ln(I_0)}{I - I_0} = \frac{V - V_0}{I - I_0} \frac{1}{\eta_1 V_T} - \frac{R_S}{\eta_1 V_T} \quad (8.10)$$

Taking

$$X = \frac{V - V_0}{I - I_0} \quad (8.11)$$

$$Y = \frac{\ln(I) - \ln(I_0)}{I - I_0} \quad (8.12)$$

We have a straight line:

$$Y = X \frac{1}{\eta_1 V_T} - \frac{R_S}{\eta_1 V_T} = mX + q \quad (8.13)$$

The linear regression of this straight line gives η_1 and R_S :

$$\eta_1 = \frac{1}{mV_T} \quad (8.14)$$

$$R_S = -q\eta_1 V_T \quad (8.15)$$

At this point, when we know R_S , the reverse saturation current (I_{S1}) is obtained by a second linear regression. This fitting gives also a new value of η_1 .

$$\ln(I) \cong \ln(I_{S1}) + \frac{V - R_S I}{\eta_1 V_T} \quad (8.16)$$

Taking

$$X_1 = V - R_S I \quad (8.17)$$

$$Y_1 = \ln(I) \quad (8.18)$$

We obtain a straight line:

$$Y_1 = X_1 \frac{1}{\eta_1 V_T} + \ln(I_{S1}) = m_1 X_1 + q_1 \quad (8.19)$$

From the linear regression of this curve we can obtain the new η_1 and the saturation current (I_{S1}):

$$\eta_1 = \frac{1}{m_1 V_T} \quad (8.20)$$

$$I_{S1} = \exp(q_1) \quad (8.21)$$

In order to extrapolate the second exponential contribution and the shunt resistance, we define:

$$V_C = V - R_S I \quad (8.22)$$

$$I_{D1} = I_{S1} \cdot \left(\exp \left(\frac{V - R_S I}{\eta_1 V_T} \right) \right) \quad (8.23)$$

The current I_{D1} has to be subtracted from the total current and we obtain the remaining current (I_R).

$$I_R = I - I_{D1} = I_{S2} \exp \left(\frac{V - R_S I}{\eta_2 V_T} \right) \quad (8.24)$$

$$\ln(I_R) = \ln(I_{S2}) + \frac{V - R_S I}{\eta_2 V_T} \quad (8.25)$$

$$\ln(I_R) = \ln(I_{S2}) + \frac{V_C}{\eta_2 V_T} \quad (8.26)$$

Taking

$$X_2 = V_C = V - R_S I \quad (8.27)$$

$$Y_2 = \ln(I_R) \quad (8.28)$$

We obtain a straight line:

$$Y_2 = X_2 \frac{1}{\eta_2 V_T} + \ln(I_{S2}) = m_2 X_2 + q_2 \quad (8.29)$$

The linear regression of this straight line gives η_2 and I_{S2} :

$$\eta_2 = \frac{1}{m_2 V_T} \quad (8.30)$$

$$I_{S2} = \exp(q_2) \quad (8.31)$$

At this point we can calculate R_{SH} with the following relation that derives directly from the initial equation:

$$R_{SH} = \left[\left(\frac{dI}{dV} \right)_{V \rightarrow 0} - I_{S1} \frac{1}{\eta_1 V_T} - I_{S2} \frac{1}{\eta_2 V_T} \right]^{-1} \quad (8.32)$$

If R_{SH} is comparable to dV/dI in the region used to determine I_{S2} and η_2 , then we fit the curve considering the introduction of R_{SH} and we can obtain the final value of I_{S2} and η_2 :

$$I_R^* = I - I_{D1} - I_{RSH} = I_R - \frac{V_C}{R_{SH}} = I_{S2} \exp\left(\frac{V - R_S I}{\eta_2 V_T}\right) \quad (8.33)$$

$$\ln(I_R^*) = \ln\left(I_R - \frac{V_C}{R_{SH}}\right) = \ln(I_{S2}) + \frac{V - R_S I}{\eta_2 V_T} \quad (8.34)$$

Taking

$$X_3 = V_C = V - R_S I \quad (8.35)$$

$$Y_3 = \ln(I_R^*) = \ln\left(I_R - \frac{V_C}{R_{SH}}\right) \quad (8.36)$$

We obtain a straight line:

$$Y_3 = X_3 \frac{1}{\eta_2 V_T} + \ln(I_{S2}) = m_3 X_3 + q_3 \quad (8.37)$$

The linear regression of this straight line gives η_2 and I_{S2} :

$$\eta_2 = \frac{1}{m_3 V_T} \quad (8.38)$$

$$I_{S2} = \exp(q_3) \quad (8.39)$$

Typical results are shown in Fig. 8.9 and Table 8.4 regarding the solar cell with high R_{SH} .

The method intrinsically presents some problems: in fact, the splitting of the I-V curve in four regions is correct as long as the different contributions of R_S , D_1 , D_2 and R_{SH} are considered to be limited in the region in which they are dominant. This assumption cannot be made if the shunt resistance is too low, because in this case it affects also the high part of the I-V curve. When the shunt

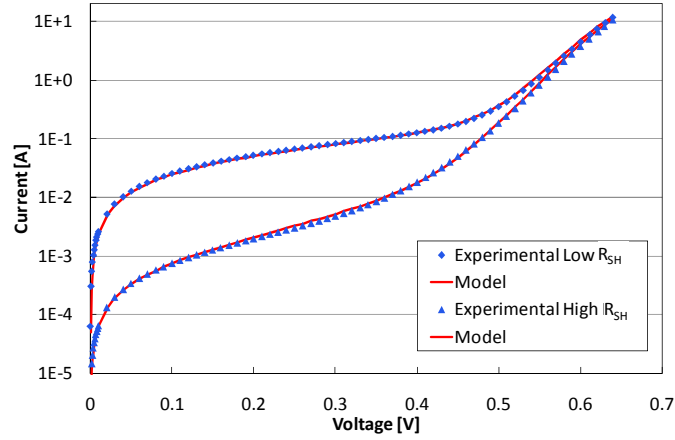


Figure 8.9: Dark I-V curves measured from two solar cells: one with shunt resistance of 4.127Ω and the second 231Ω . Experimental data were submitted to the model fitting and the simulation results are also reported.

Table 8.4: Data extracted from the two diode fitting procedure

Cell	I_{S1} [A]	η_1	I_{S2} [A]	η_2	R_S [Ω]	R_{SH} [Ω]
Low R_{SH}	6.10E-9	1.127	3.76E-4	3.720	1.61E-3	4.127
High R_{SH}	4.24E-9	1.116	1.68E-4	3.695	1.57E-3	231

resistance is drastically reduced (lower than $10\sim 15 \Omega$) the standard technique produces wrong results in term of approximation of the shunt resistance in the R3 and R4 regions. In this case the shunt resistance cannot be neglected and eq. 8.6 is modified to:

$$I = I_{S1} \cdot \left(\exp \left(\frac{V - R_S I}{\eta_1 V_T} \right) - 1 \right) + \left(\frac{V - R_S I}{R_{SH}} \right) \cong I_{S1} \cdot \left(\exp \left(\frac{V - R_S I}{\eta_1 V_T} \right) \right) + \left(\frac{V - R_S I}{R_{SH}} \right) \quad (8.40)$$

In this way the effects of the first diode, the series resistor and the shunt resistor are considered. The shunt resistance can be roughly estimated from the slope of the I-V curve in the low voltage region, and then is recalculated after the estimation of the two diode parameters.

The first step is a rough estimation of R_{SH} from the first part of the I-V curve:

$$R_{SH} \approx \left(\frac{dI}{dV} \right)_{V \rightarrow 0} \quad (8.41)$$

For $I \gg I_{S1}$ we can write for the high part of the I-V curve:

$$I = I_{S1} \cdot \left(\exp \left(\frac{V - R_S I}{\eta_1 V_T} \right) - 1 \right) + \left(\frac{V - R_S I}{R_{SH}} \right) \cong I_{S1} \cdot \left(\exp \left(\frac{V - R_S I}{\eta_1 V_T} \right) \right) + \left(\frac{V - R_S I}{R_{SH}} \right) \quad (8.42)$$

$$\ln \left(I - \frac{V - R_S I}{R_{SH}} \right) \cong \ln(I_{S1}) + \frac{V - R_S I}{\eta_1 V_T} \quad (8.43)$$

By taking a point (V_0, I_0) of the I-V curve, we can write the following relation:

$$\ln \left(I - \frac{V - R_S I}{R_{SH}} \right) - \ln \left(I_0 - \frac{V_0 - R_S I_0}{R_{SH}} \right) = \frac{V - R_S I}{\eta_1 V_T} - \frac{V_0 - R_S I_0}{\eta_1 V_T} \quad (8.44)$$

$$\ln \left(I - \frac{V - R_S I}{R_{SH}} \right) - \ln \left(I_0 - \frac{V_0 - R_S I_0}{R_{SH}} \right) = \frac{V - V_0}{\eta_1 V_T} - \frac{R_S}{\eta_1 V_T} (I - I_0) \quad (8.45)$$

$$\frac{\ln \left(I - \frac{V}{R_{SH}} \right) - \ln \left(I_0 - \frac{V_0}{R_{SH}} \right)}{I - I_0} = \frac{V - V_0}{I - I_0} \frac{1}{\eta_1 V_T} - \frac{R_S}{\eta_1 V_T} \quad (8.46)$$

In the last simplification the R_S contribution was deleted in the left part of the equation considering $R_S I$ low respect to V in the high part of the I-V curve.

Taking:

$$X = \frac{V - V_0}{I - I_0} \quad (8.47)$$

$$Y = \frac{\ln \left(I - \frac{V}{R_{SH}} \right) - \ln \left(I_0 - \frac{V_0}{R_{SH}} \right)}{I - I_0} \quad (8.48)$$

We have a straight line:

$$Y = X \frac{1}{\eta_1 V_T} - \frac{R_S}{\eta_1 V_T} = mX + q \quad (8.49)$$

The linear regression of this straight line gives η_1 and R_S .

$$\eta_1 = \frac{1}{m V_T} \quad (8.50)$$

$$R_S = -q \eta_1 V_T \quad (8.51)$$

At this point, when we know R_S , the reverse saturation current (I_{S1}) is obtained by a second linear regression. This fitting gives also a new value of η_1 .

$$\ln \left(I - \frac{V - R_S I}{R_{SH}} \right) \cong \ln(I_{S1}) + \frac{V - R_S I}{\eta_1 V_T} \quad (8.52)$$

Taking:

$$X_1 = V - I R_S \quad (8.53)$$

$$Y_1 = \ln \left(I - \frac{V - R_S I}{R_{SH}} \right) \quad (8.54)$$

We have a straight line:

$$Y_1 = X_1 \frac{1}{\eta_1 V_T} + \ln(I_{S1}) = m_1 X_1 + q_1 \quad (8.55)$$

From the linear regression of this curve we can obtain the new η_1 and the saturation current (I_{S1}):

$$\eta_1 = \frac{1}{m_1 V_T} \quad (8.56)$$

$$I_{S1} = \exp(q_1) \quad (8.57)$$

In order to extrapolate the second exponential contribution and the shunt resistance, we define:

$$V_C = V - I R_S \quad (8.58)$$

$$I_{D1} = I_{S1} \cdot \left(\exp \left(\frac{V - R_S I}{\eta_1 V_T} \right) \right) \quad (8.59)$$

The current I_{D1} has to be subtracted from the total current considering also the R_{SH} contribution and we obtain the remaining current (I_R).

$$I_R = I - I_{D1} - I_{RSH} = I - I_{D1} - \frac{V - R_S I}{R_{SH}} = I_{S2} \exp \left(\frac{V - R_S I}{\eta_2 V_T} \right) \quad (8.60)$$

$$\ln(I_R) = \ln(I_{S2}) + \frac{V - R_S I}{\eta_2 V_T} \quad (8.61)$$

$$\ln(I_R) = \ln(I_{S2}) + \frac{V_C}{\eta_2 V_T} \quad (8.62)$$

Taking

$$X_2 = V_C = V - I R_S \quad (8.63)$$

$$Y_2 = \ln(I_R) \quad (8.64)$$

We obtain a straight line:

$$Y_2 = X_2 \frac{1}{\eta_2 V_T} + \ln(I_{S2}) = m_2 X_2 + q_2 \quad (8.65)$$

From the linear regression of this curve we can obtain η_2 and the saturation current (I_{S2}):

$$\eta_2 = \frac{1}{m_2 V_T} \quad (8.66)$$

$$I_{S2} = \exp(q_2) \quad (8.67)$$

At this point we can calculate R_{SH} with the following relation that derives directly from the initial equation:

$$R_{SH} = \left[\left(\frac{dI}{dV} \right)_{V \rightarrow 0} - I_{S1} \frac{1}{\eta_1 V_T} - I_{S2} \frac{1}{\eta_2 V_T} \right]^{-1} \quad (8.68)$$

If R_{SH} is comparable to dV/dI in the region used to determine I_{S2} and η_2 , then we fit the curve considering the introduction of R_{SH} and we can obtain the final value of I_{S2} and η_2 :

$$I_R^* = I - I_{D1} - I_{RSH} = I_R - \frac{V_C}{R_{SH}} = I_{S2} \exp \left(\frac{V - R_S I}{\eta_2 V_T} \right) \quad (8.69)$$

$$\ln(I_R^*) = \ln \left(I_R - \frac{V_C}{R_{SH}} \right) = \ln(I_{S2}) + \frac{V - R_S I}{\eta_2 V_T} \quad (8.70)$$

Taking

$$X_3 = V_C = V - R_S I \quad (8.71)$$

$$Y_3 = \ln(I_R^*) = \ln \left(I_R - \frac{V_C}{R_{SH}} \right) \quad (8.72)$$

We obtain a straight line:

$$Y_3 = X_3 \frac{1}{\eta_2 V_T} + \ln(I_{S2}) = m_3 X_3 + q_3 \quad (8.73)$$

The linear regression of this straight line gives η_2 and I_{S2} :

$$\eta_2 = \frac{1}{m_3 V_T} \quad (8.74)$$

$$I_{S2} = \exp(q_3) \quad (8.75)$$

With this modified approach the influence of the shunt resistance is not neglected, and we obtain results shown in Fig. 8.9 and Table 8.4 regarding the cell with low shunt resistance. Results show that the different procedure does not affect the parameters related to diode 1 and the series resistance, but only the shunt resistance is drastically decreased from one cell to another. This is very important, since it confirms that the shunt resistance can also affect the high-voltage part of the I-V curve, and confirms that with this simple modification, a self-consistent method was found for a more reliable calculation and estimation of the shunt resistance, which is a fundamental parameter to be considered during the sorting of the solar cells.

The fitting parameters obtained in dark conditions are validated by simulations under illumination: they are inserted in the light model (Fig. 8.8 a) and the

simulated I-V light curves are compared with the experimental measurements under 1 sun illumination and 25 °C cell temperature. Fig. 8.10 shows the comparison between the experimental and simulation results, while Table 8.5 reports the parameters obtained from light I-V measurement (e.g. Fill Factor, efficiency, max power point) and from the previous two diode model simulation. The results and the matching are very good, and this is due to the modification of the standard procedure for the optimal fitting of a low shunt resistance cell measurement.

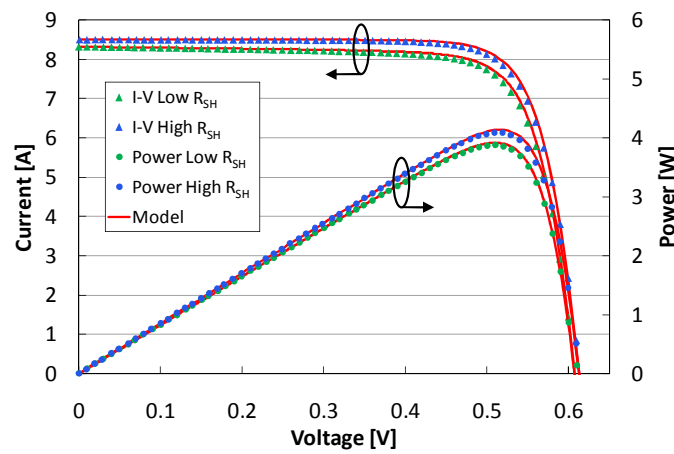


Figure 8.10: Light I-V curves obtained from two solar cells: one with shunt resistance of 4.127 Ω and the second 231 Ω . The experimental and simulation results are reported, and the generated power is also plotted.

Table 8.5: Comparison Between light I-V curves and AIM-Spice simulation

Cell	V_{OC} [V]	I_{SC} [A]	η	FF	V_{PW} [V]	I_{PW} [A]	P_W [W]
Low R_{SH} data	0.609	8.327	15.95	0.766	0.510	7.613	3.882
Low R_{SH} model	0.607	8.323	16.12	0.777	0.510	7.693	3.924
High R_{SH} data	0.609	8.514	16.80	0.788	0.509	8.024	4.088
High R_{SH} model	0.610	8.514	16.99	0.796	0.515	8.030	4.135

In order to find the temperature dependence of the fitting procedure we conducted dark I-V measurement over temperature (between 25 °C and 55 °C). The saturation current in AIM-Spice is modeled using the equation:

$$I_{Si} = I_{Si}(T_0) \cdot \left(\frac{T_1}{T_0}\right)^{\frac{XTI}{N}} \exp\left(\frac{E_G(T_1 - T_0)}{NkT_1T_0}\right) \quad (8.76)$$

where T_0 is the standard temperature (25 °C), T_1 is the operating temperature, k the Boltzmann constant, E_G is the energy gap, XTI is the saturation current temperature exponent and N the ideality factor. The experimental measurements allowed us to extrapolate the XTI parameter related to the two diodes (recombination mechanism and diffusion mechanism). The XTI parameters were found 4 and 6 for the diode 1 and 2, respectively. This is in accordance with the theoretical formulas [135]:

$$I_{S1} \propto T^3 \cdot \exp\left(\frac{-E_G}{\eta_1 kT}\right) \quad (8.77)$$

$$I_{S2} \propto T^{5/2} \cdot \exp\left(\frac{-E_G}{\eta_2 kT}\right) \quad (8.78)$$

The exponent XTI/N in Eq. 8.76 is then separately found for the two diodes of the cell model:

- in Eq. 8.77 it takes into account the diffusion mechanism (diode 1 with a ideality factor $1 = 1.20$) and its value is then $4/1.2=3.33$;
- in Eq. 8.78 it represents the recombination mechanism (diode 2 with an ideality factor $2 = 2.44$) and is then $6/2.44=2.46$.

The two ideality factors are calculated using the two diode model at standard temperature. These two results are in agreement with the theoretical temperature exponents also reported in Eqs. 8.77 and 8.78. After applying the two diode models (standard and modified) to different cells with high and low shunt resistance, simulation over a string of cells were carried out.

8.2.2 Study of a string of cells

The presence of a low shunt resistance (smaller than 10 Ohm) can significantly influence the characteristics and performance of the solar cells, especially when the cells operate in low illumination conditions, as demonstrated by preliminary studies [136]-[126]. An even more critical situation occurs when a shunted cell - located in a module constituted by several cells - is partially shaded: in this case the current that is photogenerated by the other cells reversely crosses the shadowed one. At this point the operation of the shadowed cell is strictly dependent from the value of its shunt resistance, that can itself vary when the cell is reverse-polarized [126]. To investigate how the presence of a shunted cell can impact the performance and electro-optical characteristics of a module, we

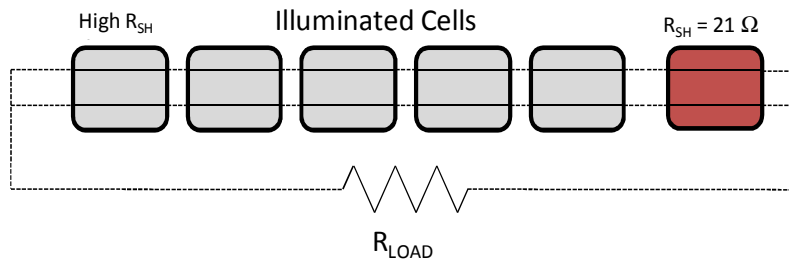


Figure 8.11: Six cells string. The cells are connected in series, the low shunt resistance cell is shaded and the shunt resistance is 21Ω .

conducted some experiments and simulations over a string of 6 cells connected in series and afterwards simulated the electrical characteristics of a string of 21 cells in which a low-shunt resistance cell is inserted.

6 Cells are then connected in series, 5 with high shunt resistance (between 142Ω and 274Ω) and one with low shunt resistance (21Ω) that is shaded (Fig. 8.11).

Fig. 8.12 shows the light and dark I-V curves of the cell with 21Ω shunt resistance and one of the solar cells with high shunt resistance.

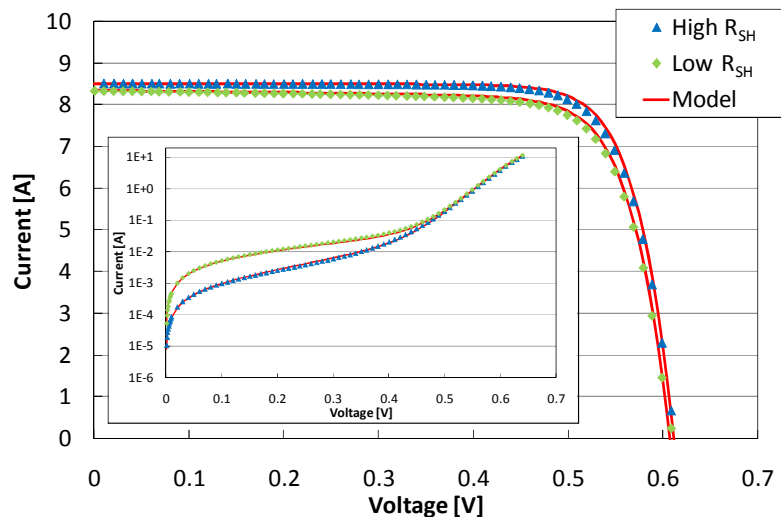


Figure 8.12: Light I-V curves obtained from two solar cells: one with shunt resistance of 21Ω (Low R_{SH}) and the second 208Ω (High R_{SH}). Inset: Dark I V curves of the same solar cells.

The outdoor measurements were conducted under a 760 W/m^2 illumination (light intensity was monitored with a pyranometer) and a temperature of 50°C (measured directly with a thermocouple on a lighted cell). The simulation

and the experimental results are shown in Fig. 8.13: the simulation are obtained changing the shunt resistance of the shaded cell from 5 Ω to 50 Ω .

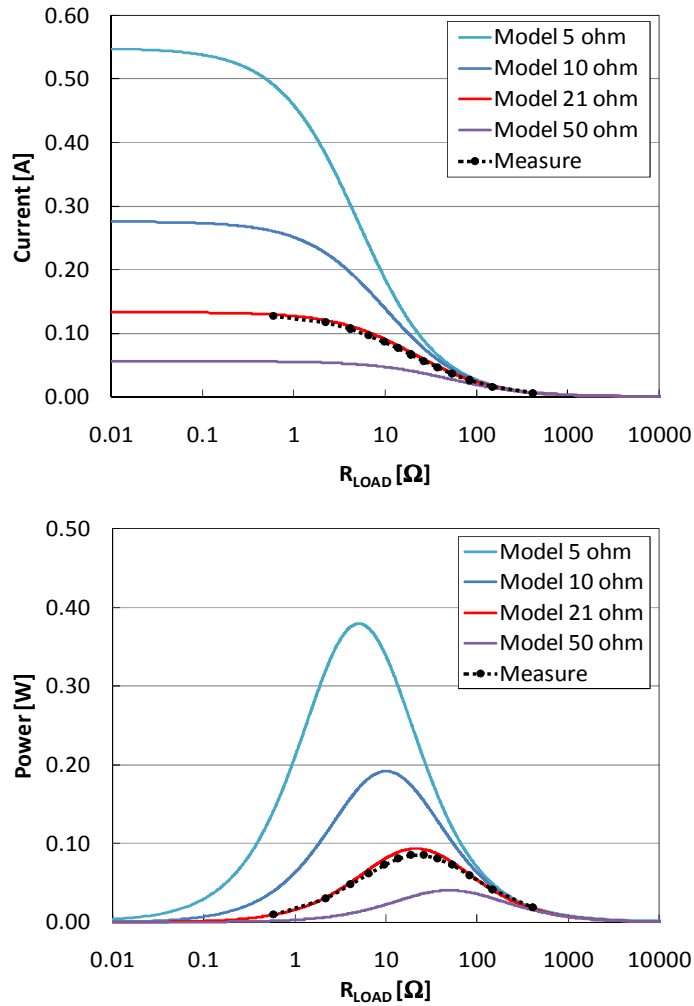


Figure 8.13: Six cells string simulation (varying the shunt resistance from 5 Ω to 50 Ω) and experimental results (shunt resistance: 21 Ω).

We can see that lowering the shunt resistance the external power and current are increased, and this is the evidence that the shaded low shunt resistance cell offers a path to the current generated by the lighted cells. The simulation results with a shunt resistance of 21 is in agreement with the experimental measure obtained directly from the real six cell string and this confirms the goodness of the model used to fit the I-V curve of the single cell and the temperature dependence correction. After this experiment we conducted some simulation over a twenty-one cells string: 20 with high shunt resistance (511 Ω) and one with a

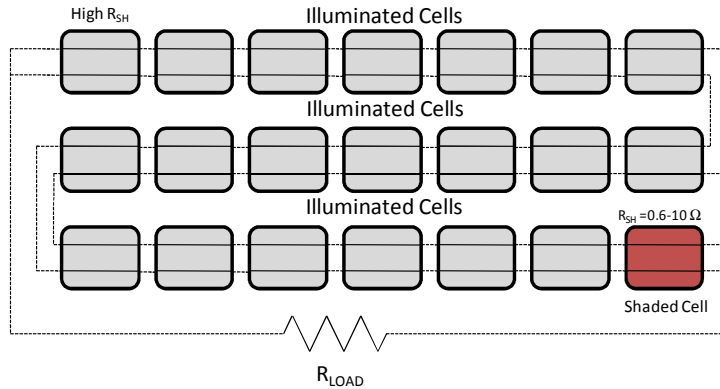


Figure 8.14: Twenty-one cells string. The cells are connected in series, the low shunt resistance cell is shaded and the resistance is varied from 0.6Ω to 10Ω .

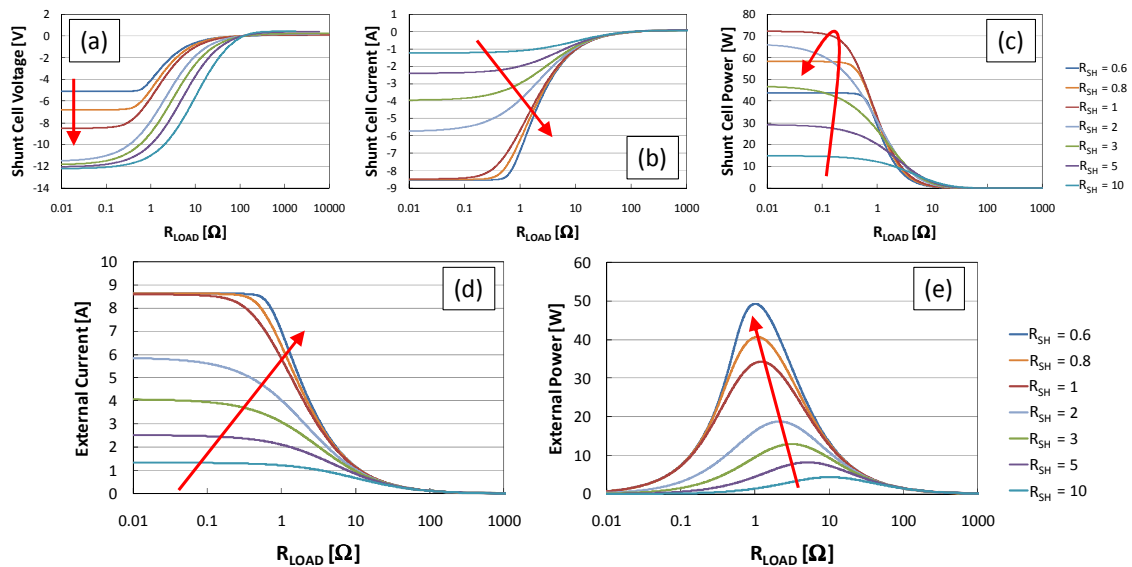


Figure 8.15: Electrical parameters of the shadowed cell, calculated for different R_{SH} values.

low shunt resistance (a sweep from 0.6Ω and 10Ω was done)(Fig. 8.14). We analyzed the case in which the low shunt resistance cell is shadowed.

The results of the simulation of 21 cells are presented in Fig. 8.15. Data indicate that as the shunt resistance of the shadowed cell is lowered, this cell behaves as a resistive load for the other (lit) cells: in fact the external power extracted by the series of 21 cells monotonically increases with the decrease of the shunt resistance (see Fig. 8.15 d and 8.15 e). The shunt resistance acts as a preferential path for the current generated by the other cells, and so it does

not allow the shutdown of the entire system. Figs. 8.15 a- 8.15 c summarize the voltage, current and power dissipation on the shunted cell, for varying values of the shunt resistance; as can be noticed, when the cell with low shunt resistance is shadowed, it is crossed by a high reverse current. The power dissipation on the shunted cell increases with decreasing shunt resistance, until a saturation is reached for $R_{SH} = 1$ (Fig. 8.15 c). The shadowed cell is biased in reverse condition, and the temperature can reach levels in excess of 100-200 °C [126], leading to the failure of the cell itself. The results described above indicate that when, in a module, a solar cell with low shunt resistance is shadowed, it can be crossed by a high reverse current. This may lead to a very high, localized power dissipation, eventually resulting in a catastrophic degradation of the cell. An experimental confirmation of the problems related to reverse-current stress of solar cells is given in next session.

8.3 Catastrophic degradation of standard solar cells submitted to reverse current stress

The ageing process was found to lead to a catastrophic failure of the solar cells, which takes place for sufficiently high reverse-current levels. The failure current was found to be different for the several cells analyzed in this thesis, depending on the initial shunt resistance of the cells, and on the preexistent position and distribution of the hot spots where leakage current is focused. Moreover, the hot spot position demonstrated to change significantly during the stress experiment, towards a stabilization in correspondence of a low-resistance shunting path. Representative data on the typical behavior are described in the following.

8.3.1 Reverse bias stresses description

Once the importance of the reverse bias stress is demonstrated in previous section, a certain number of cells are submitted to a reverse current stress. Reverse current levels are increased step by step in order to (i) monitor the cell behavior gradually and have a partial result regarding each low-level reverse current operation, and (ii) quickly reach critical currents for the cell actual degradation, thus achieving an accelerated ageing of the cell [137]. Different characterization methodologies are adopted during the stress procedure: before carrying out the stress tests, the main cell parameters were extracted by means of I-V measure-

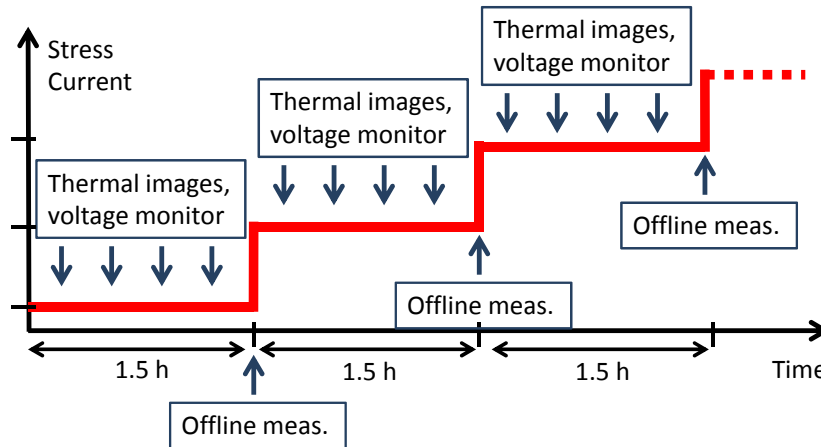


Figure 8.16: Schematic representation of the step stress procedure.

ments, both in dark condition and under illumination. Thermal characterization was carried out by means of a FLIR 320 Thermal camera using a pulsed technique [136], which allows one to increase the spatial resolution of the measurements. The degradation of the cells was induced by a step-stress strategy (Fig. 8.16): after each 90-minutes stress step at constant current, the stress level was increased. We started from relatively low current levels (1 A for this cell), reaching the critical current values that generated the permanent degradation, e.g. 4.6 A in this case.

Simulations of previous paragraph have demonstrated that such high current levels can easily be reached by solar cells with low shunt resistance in low illumination conditions. During the ageing tests, thermographic images were continuously acquired, with the aim of studying the contribution of the self-heating spots (hot spots) to current conduction and to the degradation process. Some samples were submitted to SEM analysis in correspondence of the shunt paths revealed by the thermal images, and this gave us additional and useful information on the hot spot conformation and material distribution caused by the high-temperature stress.

8.3.2 Thermo-optical degradation of the cells

The reverse current stress is structured into two stages: during the first stage at relatively low current level no degradation is observed, and the cell behaves normally once it cools down after the stress step. In this first part of the ageing all the changes induced by the stress experiment resulted to be fully reversible. In

the second stage, an irreversible deterioration of the shunt resistance is observed. This occurred for high enough current values, and leads to a sudden drop of the shunt resistance, hot spot area shrinkage and rising of the local power density and temperature. Once the cell is cooled down, the original shunt value cannot be recovered, and the cell failure is permanent. The critical reverse current value at which the failure is induced is strictly dependent by the shunt resistance presented by the cell before the stress beginning. More specifically, a dependence from the hot spot number, distribution and intensity is observed, and this is in accordance with previous studies [136]. Cells with higher shunt resistance values demonstrated hot spots more widely diffused and with lower peak temperatures, while a low shunt resistance, macroscopically extrapolated from the dark I-V measurement, is surely an index of a more concentrated and localized hot spot presence. This is reported in Fig. 8.17.

Note that the thermal images are obtained with a pulsed technique, so the maximum temperature is much lower than the same temperature reaches during the breaking. The stress experiment was conducted in both the cell types, and

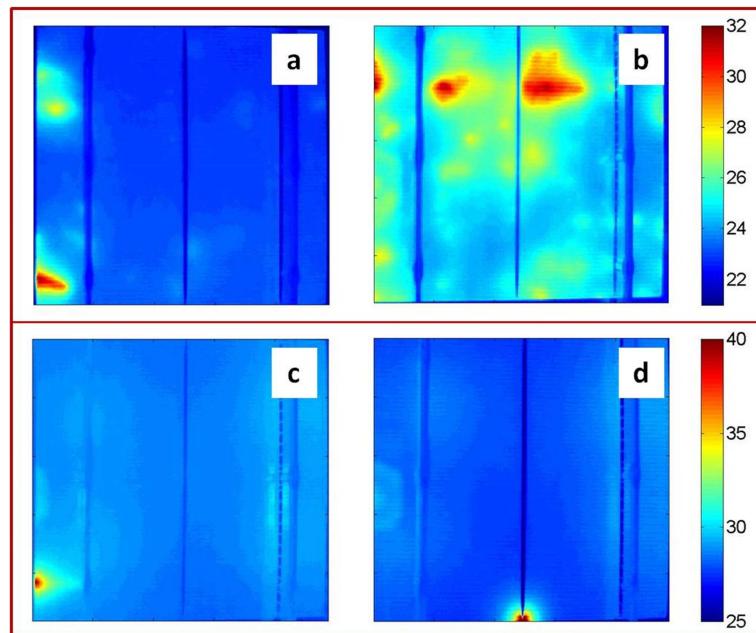


Figure 8.17: Pulsed thermal images relative to two cells with different R_{SH} values and hot spot distribution: (a) a cell with a localized hot spot and medium shunt resistance (243Ω), (b) another cell with a different hot spots distribution and high R_{SH} (380Ω). In (c), (d) the same cells are presented once failure were reached, after a stress at 4.6 A and 8.4 A respectively.

Fig. 8.17 also shows how the stress thermal results are analogous for the two. The main difference is the reverse current value in which the failure occurs, because in the case of a higher R_{SH} , very high reverse current levels (and thus high absorbed power) were reached before to effective degradation. The lowering of the shunt resistance obtained during the latter stage is confirmed by reverse dark I-V characterizations.

Thermal images were indeed taken during the stress procedure, so we are able to describe the hot spot evolution. These information are quite useful when observing the hot spot behavior during the failure: the spot showed a radical shrinkage and reached very high temperature levels, up to 180 °C, while the cell reverse voltage followed these dynamics.

To achieve a better description of the degradation process, we carried out a complete thermal characterization of the cells both during the execution of the stress test, and at the end of each stage of the step-stress experiment. Fig. 8.18 reports two thermal images of the cell, collected before and after the catastrophic failure.

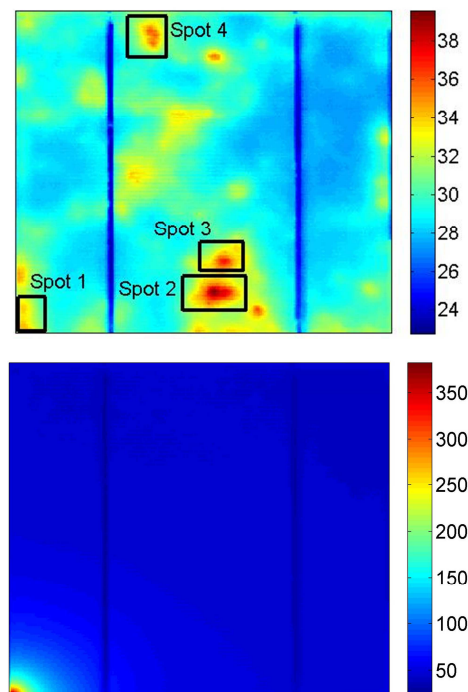


Figure 8.18: Thermal images taken before the stress beginning (top) and after the cell failure at -3.6A (bottom). At the top the three hot spots are still distinguishable, while in the bottom the failed path along Spot 1 prevails.

The first image was taken at the beginning of the stress, the second after the cell failure, that occurred at - 3.6 A. Before stress (Fig. 8.18, top), several hot spots indicate the presence of a number of leakage paths, that are responsible for reverse current conduction. Four of these spots have been highlighted and labeled as Spot 1-4 in Fig. 8.18, and their temperature were monitored along the whole stress procedure.

In Fig. 8.19 we report the temperature increase measured on these spots during the step-stress experiment: during stress time, all the hot spots increase in temperature, while the cell (reverse) voltage increases with stress current level. When failure occurs, Spot 1 shows a remarkable temperature increase, and becomes the dominant shunt path: as a consequence, the cell (reverse) voltage rapidly decreases (from -16 V to -2.5 V).

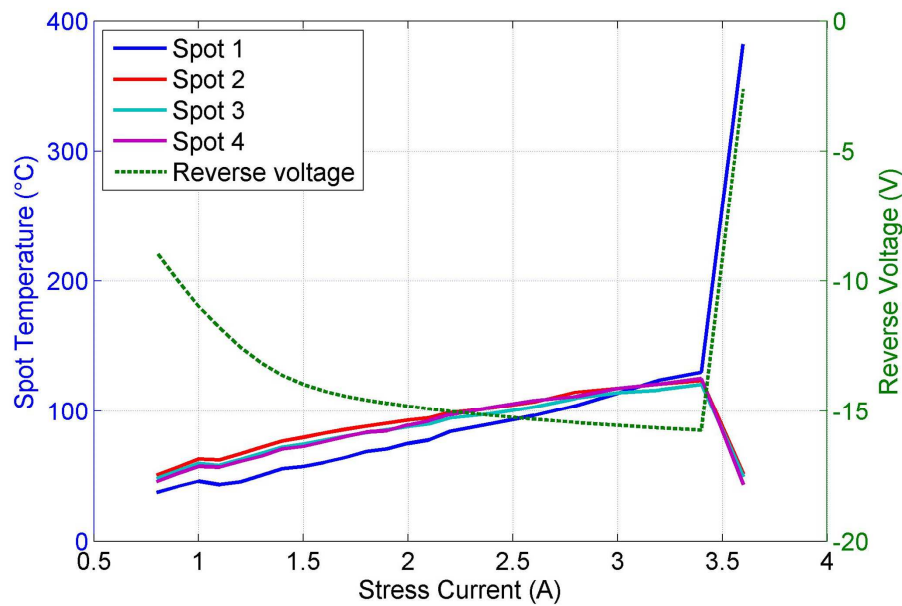


Figure 8.19: Temperature of the spots and cell voltage monitored during the stress process. Notice the higher temperature maintained by Spot 1 and its rapid increase while reaching critical current values.

Fig. 8.20 provides a detailed description of the last stage of the step-stress experiment (at -3.6 A), i.e. the step in which the failure occurs. During stress time, all the analyzed leaky regions increase in temperature: however Spot 1 shows the larger temperature increase, by reaching temperatures around 380 °C. This leads to a permanent degradation of the cell, due to the formation of a low-resistance shunt path in proximity of Spot 1, and to a sudden drop of cell voltage.

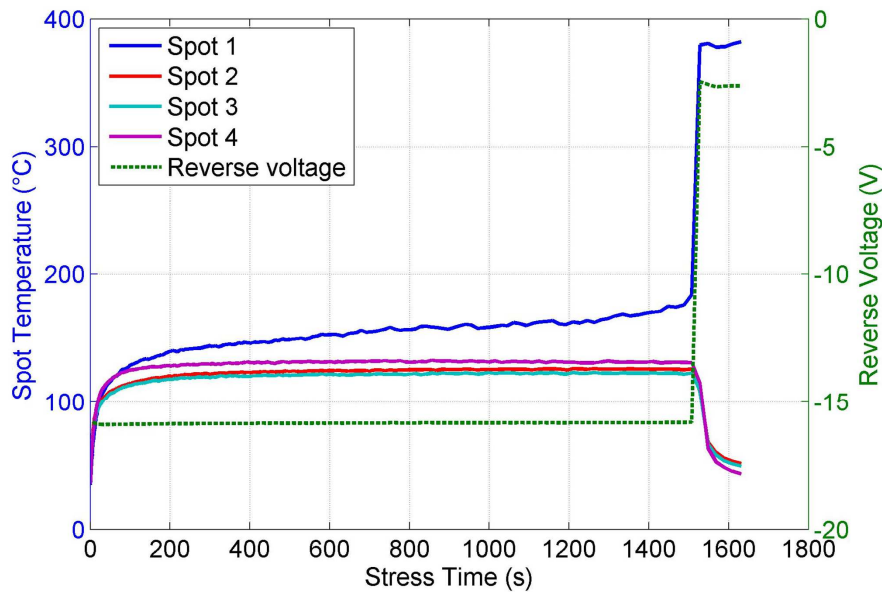


Figure 8.20: Plots of the spots temperature and cell voltage (dashed line) vs. time, during a -3.6 A stress. At the -3.6 A inverse current, the cell has broken, and it is evidenced by the fast increase of the Spot 1 temperature and voltage drop.

It is worth noticing that the power dissipation during reverse operation induced on the cell shunt resistance and observed at the breaking point is about $P_{rev} = 57.6$ W, which is even lower than the power that can be reversely-induced into a shaded cell encapsulated into a partially-shaded panel. In absence of bypass diodes integrated into the panel, indeed, all the current from the panel will cross the shaded cell, and in this way a power loss will be induced by the shaded cell into its shunt resistance. This would lead to a sudden and significant decrease of the total power output of the panel, and to a power dissipation on the shunt resistance that for a solar module with $I_{sc} = 8$ A and silicon solar cells with a breakdown voltage of approximately $V_{br} = 16$ V can reach values of $P_{rev} \approx 100$ W [138].

Up to date, the physical nature of these hotspots is not completely known, so in the following a deeper analysis of their creation and behavior during the reverse-bias operation and their area conformation is presented. The imaging of hot spots via thermal images investigations allowed to identify some preferential location for the hot spot before and after the stress experiment. Like in other studies [139], hot spot were often noticed in positions that have been submitted to a stronger stress during the fabrication process, i.e. under the fingers, busbars,

or along the edge isolations. Moreover, the hot spots are not fixed but they are subjected to change their position and temperature during the reverse bias stress. This variability is noticed in a significant number of cells, and indicates the strong dependence of hot spots from cell mechanical and material properties, that can be influenced by the local current flow and temperature levels. An example of these dynamics is presented in Fig. 8.21: for a cell stressed up to a current level of 7.7 A, the self-heating points shifted along the cell and deeply changed their position and temperature. The high temperature (> 250 °C) reached during the stress led in this case to a partial re-arrangement of the silicon material itself, and probably induced the generation and adjustment of the defects responsible of the shunt current conduction. This hypothesis is supported by the continuous change of the reverse voltage, also shown in Fig. 8.21, which indicates the variation of the shunt resistance.

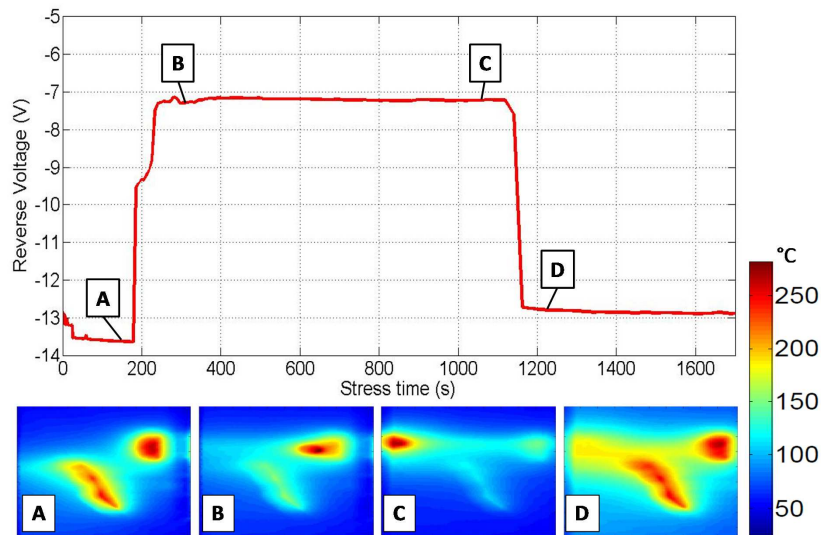


Figure 8.21: Plot of the cell voltage vs. stress time measured during a step conducted after 57 hours of stress and at a reverse bias of 7.7 A. The pictures at the bottom refer to a 3.4×2.0 cm² area thermographic images taken during the stress itself.

A detailed investigation of the area submitted to this high temperature heating is presented in Fig. 8.22, where some microscopic images of the principal heating spots are reported. In this case the hot spots happened to be right below the finger contacts, and this is proved by the finger aluminum alloy fusion imaged in A and B. The same alloy migration is shown in C, in this case the material is not coming from the fingers, but probably from the rear side of the cell: this

mechanism is currently under investigation. The high temperature reached in correspondence of the hot spots has a detrimental effect on the finger conditions and moreover on the mechanical integrity of the cell: sometimes after the stress the cell showed a structural breaking along the hot spots disposition, while on other samples it became very delicate and highly prone to cracks.

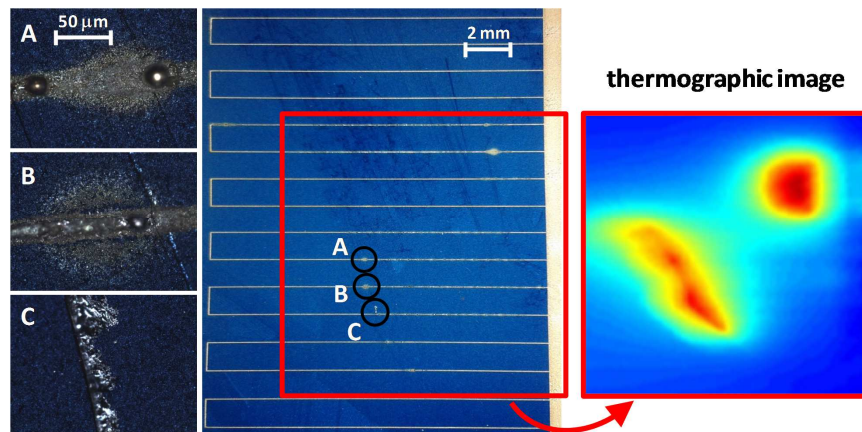


Figure 8.22: Microscopic images presenting the hotspots reported from the cell of Fig. 8.21. In A, B there is the damage induced by the high temperature, while in C is the material from the crack. For reference the spot position of the thermal image are reported.

The change in silicon morphology is confirmed also by the SEM picture of one of the failed regions reported in Fig. 8.23. The damage, located in correspondence of a pre-existing leaky region, is recognizable by the change in the silicon surface, which has been induced by the high temperatures reached by the cell during stress. In addition in Fig. 8.23 b a map of the presence of carbon is reported. Since the presence of carbon is not usual upon a silicon solar cell, and it is noticed to be present right over the hot-spot position, it can be an additional proof to the very high temperature and carbonization of the cell reached in that specific point. In Fig. 8.23 c a detailed SEM picture of the hotspot morphology is shown: in correspondence of the low shunt resistance is clearly visible a silicon defect and the formation of a small conductive path responsible for lowering of shunt resistance caused by the electrical stress. Incidentally, other works relate the presence of similar hot spot with the fabrication process. For instance, in [140] the hot spot creation is related to the separation of the diffused emitter from back contacts, whereas in [141] to the native defects in the materials. Probably, the stress-induced hot spots may originate from some small process-induced latent

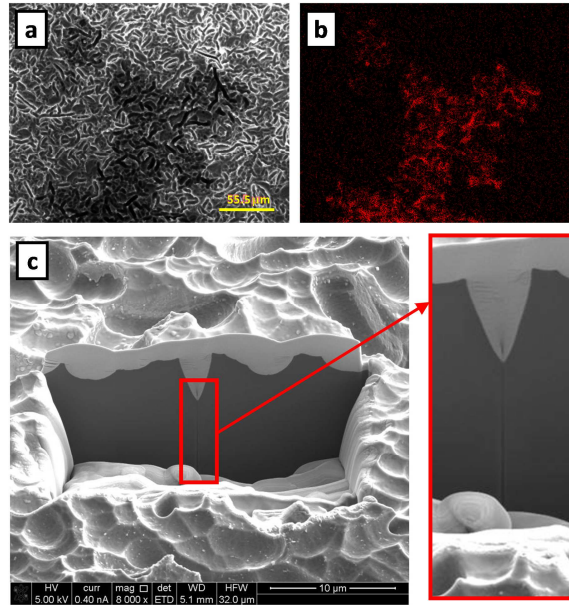


Figure 8.23: (a) SEM image taken in correspondence of the hotspot. It refers to a cell already stressed and failed, and the imaged area is where the current was concentrated. Thanks to a microanalysis on the same SEM measurement, in (b) the presence of carbon is reported. (c) SEM image taken after etching of silicon in correspondence of the hotspot. The low resistive signal path is clearly visible within the highlighted area.

defect, which is later depassivated during accelerated electrical stress.

8.3.3 Electrical degradation of the cells

Electrical measurements were performed after each stage of the step-stress experiment, both in dark and light conditions. Representative results are summarized in Fig. 8.24 and 8.25. The deep lowering of the shunt resistance induced strong changes both in the illuminated (Fig. 8.25 top) and dark reverse I-V curves (Fig. 8.25 bottom). Therefore also the main cell parameters (V_{OC} , I_{SC} , FF , efficiency) are affected by the R_{SH} decrease. In Fig. 8.24 we plot the variation of the main cell parameters during the step-stress experiment: each point represents the result of measurements taken after 90 min of stress at increasing reverse current. Shunt resistance suddenly dropped from 11Ω to 0.32Ω , thus determining a decrease in open-circuit voltage, efficiency (from 15.6 % to 12.1 %), and fill factor (FF). It is worth noticing that, in accordance with previous studies [136], the decrease in η and FF is more prominent at low illumination levels: lower shunt

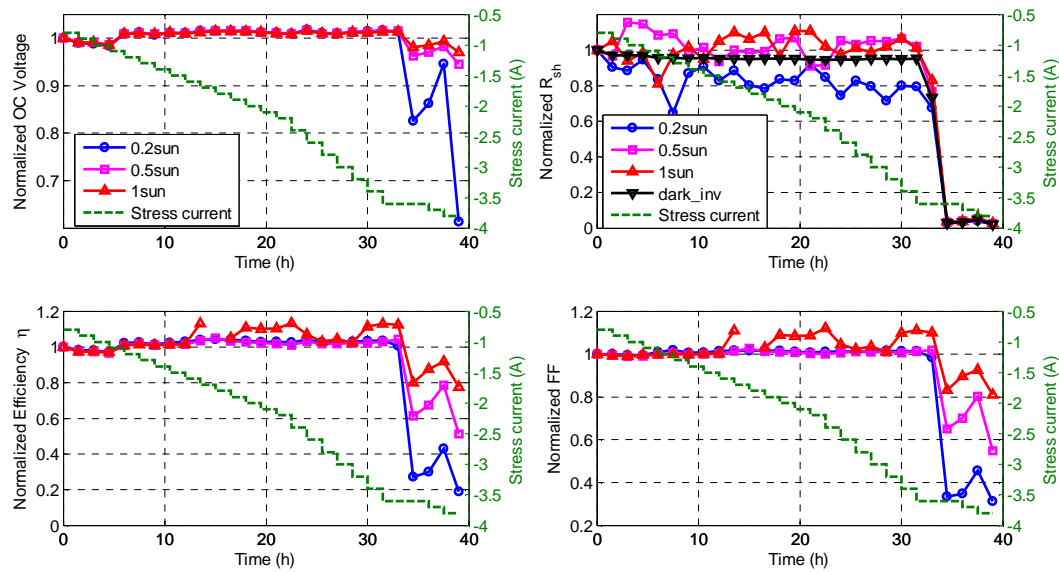


Figure 8.24: Normalized values for the shunt resistance and efficiency. Values are normalized to the first measurement conducted before the stress beginning.

resistance brings to a more relevant degradation of the fill factor and this can strongly influence the performance and reliability of PV cell.

8.3.4 The hot spot optical efficiency

The high temperature reached by the hot spot during the stress drastically influences its optical properties, by inducing a strong lowering of the local quantum efficiency in the heated area. In Fig. 8.26 a spatially resolved EQE measured at an optical wavelength of 1000 nm over the area of a hot spot is reported. In this case the hot spot reached values of about 400 °C after the failure, and the power dissipation was about $P_{\text{rev}} = 52$ W immediately before the failure. The shunt power dissipation and temperature values demonstrated to be quite similar for all the stress experiments conducted, and the temperature-induced damage is thus analogous for all the studied hot spots. From this image, it is clear that the quantum efficiency not only drops to almost 0% at the position of the weak spot, due to the small shunt resistance, but also it globally decreases in a wide region surrounding the leaky spot (as large as tens of millimeters) due to the high temperature increase. Additional EQE measurements were performed, in order to quantify the impact of the high temperature on the cell conversion efficiency. The EQE measurements were conducted exactly upon the area interested by the

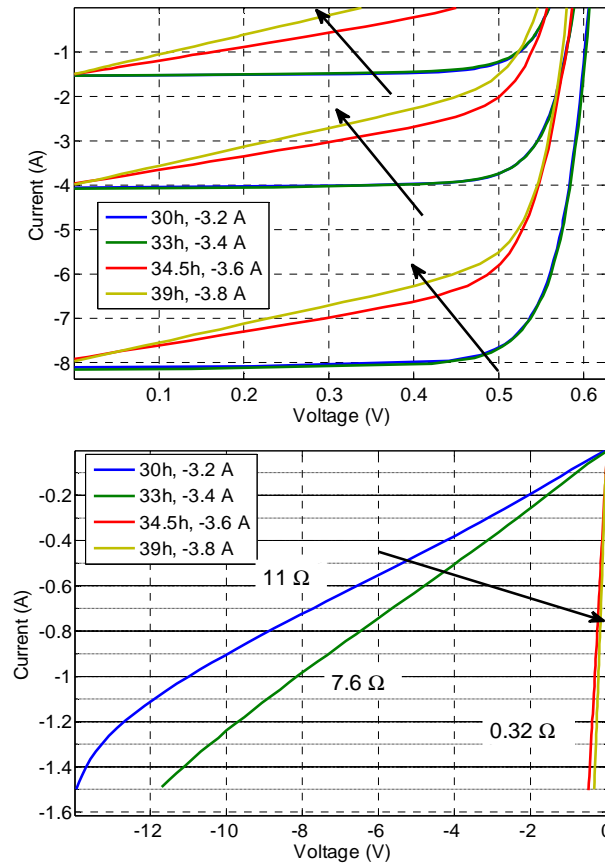


Figure 8.25: Illuminated IV measurements conducted after and before the catastrophic failure, at different conditions (0.2, 0.5 and 1 sun) and reverse bias dark IV characteristic. In evidence the lowering of the shunt resistance.

heating, after and before the breaking phenomenon, in this case after the step at -7.7 A and 7.8 A of the stress experiment. The results are reported in Fig. 8.27, from which is evident the lowering of the efficiency in the heated area.

8.3.5 Numerical simulation

The experimental data has been fitted within a two-diode model by means of Simulink MATLAB simulation, obtaining the main electrical values and their change prior and after the cell failure. The values found for a stressed cell are reported in Table 8.6, while the fitted and experimental data are in Fig. 8.28.

Fig. 8.28 shows that the simulation results are in optimal accordance with the experimental data, especially in the low-voltage region; this means that the estimated shunt resistance value (R_{sh}) is very reliable. The values reported here

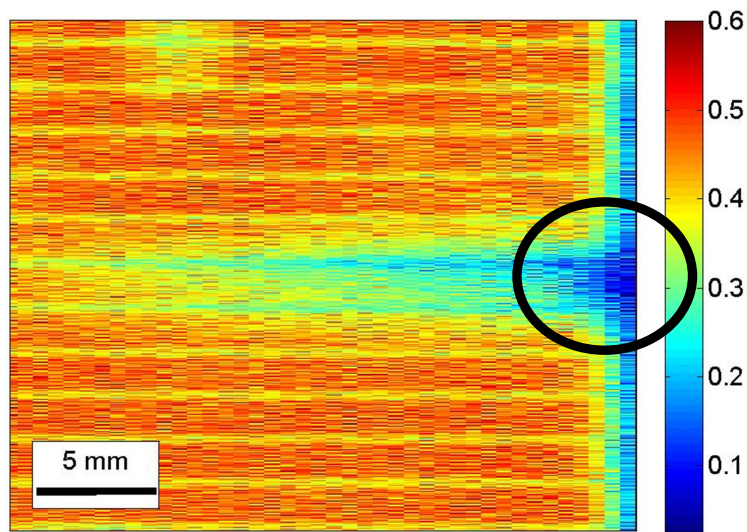


Figure 8.26: EQE spatially-resolved measurement, conducted over the hot spot in which happened the failure. The area is of $26 \times 20 \text{ mm}^2$ and the measurement was conducted with a light spot of $1 \times 2 \text{ mm}^2$ at a wavelength of 1000 nm . On the left side of the figure, the cell edge is imaged.

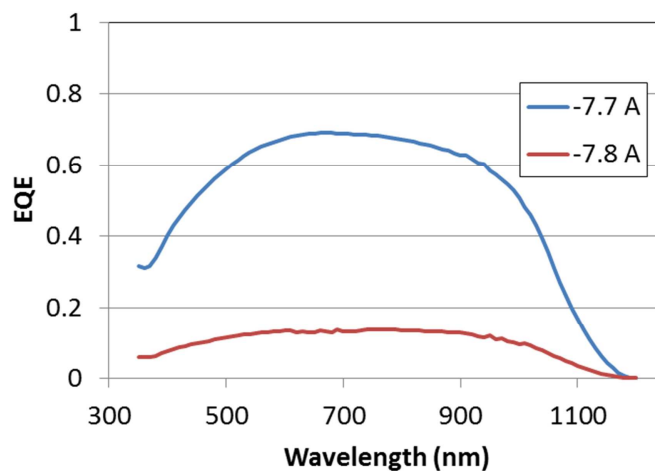


Figure 8.27: External Quantum Efficiency measured in correspondence of the area submitted to the high temperature, before and after the complete failure of the cell.

are relative for a different cell in respect to the one in Fig. 8.25, but the lowering of the shunt resistance value is again confirmed.

The resistance drop verified after the cell failure is then fully confirmed by the simulation, since the experimental data are fitted very well by the model.

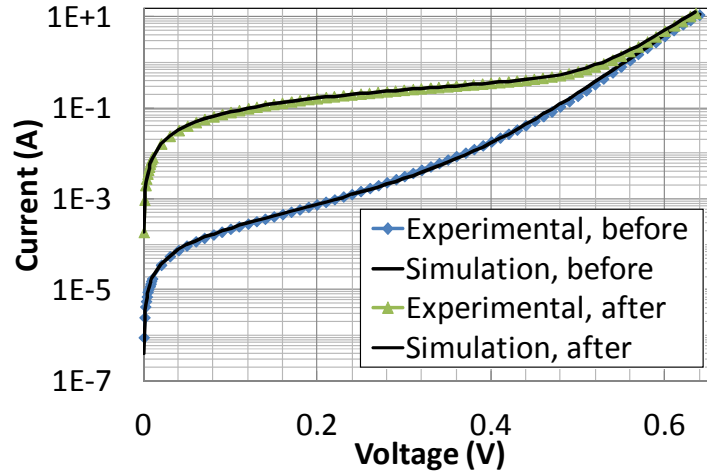


Figure 8.28: Curves relative to the cell dark IV before (green) and after (blue) the catastrophic failure. The experimental measurements (markers) and simulation results (solid lines) are reported.

Table 8.6: Results of the simulations

Param.	Before	After
J_{01} (A/cm ²)	1.15E-10	2.30E-10
η_1	1.24	1.28
J_{02} (A/cm ²)	1.21E-7	1.21E-7
η_2	2.73	2.73
R_{SH}	744	1.25
R_S	6.5E-4	3.2E-4

The influence of the shunt resistance value on the second diode characteristics can be surely neglected when the resistance is large, i.e. in the fitting of the data measured before the stress. This approximation cannot be assumed after the cell failure, because the low shunt resistance effects are observed to overcome the second diode characteristics and this surely results into a lower reliability of the diode features (J_{02} , η_2) found by the simulation. Because of this, these values were maintained the same for both the simulations, as reported in Table 8.6. This is done by considering the typical resistive behavior of the cell failure and the small area interested by the shunt, for there is no reason to suppose a changing of the recombination losses, due to hypothetical changes of the second diode characteristics.

Conclusion

RF MEMS

Despite the advantages offered by the RF-MEMS technology in terms of losses and sizes, the reliability of these devices still affects the complete expansion at the industrial level. RF-MEMS technology analyzed as part of this thesis has presented various reliability problems.

From the results obtained in this thesis, it can be seen that the resistive switches suffer from dielectric charging and mechanical relaxation and this affects their full use in radio frequency applications. Since this phenomenon leads to an instability in term of pull-in and pull-out voltages (the voltages tend to decrease with increasing biasing time), the phenomenon can also lead to failure of the device due to partial or permanent stiction. Considering the devices used in this thesis (e.g. Cantilever and Clamped-Clamped switches), it was also noted that Clamped-Clamped design presents better performance when long term stress are performed. In terms of long term stresses, to obtain devices with better characteristics, it is required a redesign of the devices considering the use of different materials (different from gold) and the use of different sizes for the mobile bridge. In particular the dimensions and spacings have to be optimized in order to minimize the mechanical relaxation due to the bridge bending during the prolonged actuation periods.

With regards to the cycling test, it was seen a progressive worsening of the scattering parameters increasing the number of cycles. This is due to a progressive degradation of the device during the stress test (probably of the contact between the gold in the bridge and the transmission line). The same phenomenon is confirmed by performing the cycling procedure at different temperatures. For

this type of tests, it has not been possible to give an exact estimation of the number cycles before breaking because of the uncontrolled atmosphere. In fact the lifetime is drastically influenced by the presence of inert atmosphere inside the package of the devices. However, the SEM analysis highlighted how the study of the gold-gold contact is of fundamental importance to obtain a life time of tens or hundreds of millions of cycles.

Finally the optical profilometer tests have allowed a detailed analysis of the actuation and release dynamics highlighting issues related to multiple rebounds in the actuation phase. It was also possible to monitor the impact speed of the mobile bridge during the actuation phase, a fundamental parameter to study the reliability of the contact itself after multiple cycling tests.

PV Solar CELLS

The solar cell technology can be considered mature in terms of robustness. The reliability studies are definitely aimed at improving the performance of the technology and at the analysis of specific conditions of use of the cells that can lead to breakage of the cells (shaded conditions or uneven illumination of an entire panel).

From the results obtained in this thesis, we can conclude how it is important to limit the presence of solar cells with low shunt resistance (less than 10 ohms) in panels that can be in condition of partial shading. In fact, the photogenerated current from the cells to the sun may lead to breakage of the cell in shadow with temperatures that can exceed 300 degrees. If the condition persists for an extended time, this could lead to rupture of the encapsulating materials with the consequent problem of fire of the photovoltaic panel.

The reliability study of a single photovoltaic cells subjected to stress in reverse bias conditions has highlighted how the break is not “soft” but of type “hard”, i.e., the cell continues to operate until abruptly one or more “hot spot” gives way under the current passage leading to the focusing of the current in a few square millimeters of silicon. Moreover the SEM analysis has highlighted the formation of shunt paths (filaments) responsible for the rupture of the photovoltaic cell. The reverse breaking current is not homogeneous in the solar cells unitized in

this thesis but is strongly dependent on the initial characteristics of the cell. It can vary from 2 A up to 5/6 A according to the initial distribution of the parasitic paths within the cell itself.

Within this thesis, we have developed algorithms in order to extrapolate the fundamental parameters of the solar cells (open circuit voltage, V_{OC} , short circuit current, I_{SC} , series resistance, R_S , shunt resistance, R_{SH} , fill factor, FF , efficiency, η , voltage at the maximum power point, V_{MP} , current at the maximum power point, I_{MP}). This allowed us to analyze in detail the evolution of the various parameters during the reverse bias stress and to understand the evolution over time of the “hot spot”. Moreover, these algorithms are very important in the production phase to obtain an accurate estimation of the goodness of the photovoltaic cells.

Finally, we have developed two optical systems (electroluminescence and photoluminescence systems). These have allowed a more accurate analysis of the failure mechanisms of photovoltaic cells by relating the optical images to the electrical parameters extracted during stress. The photoluminescence analyzes are of particular importance in the production phase as they allow measurements to be made before laying the contacts. This allows to determine the goodness of a photovoltaic cell even before the end of the production process with consequent saving of materials and production time.

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