UNIVERSITA' DI PADOVA FACOLTA' DI INGEGNERIA

Dipartimento di Ingegneria dell'Informazione

Scuola di Dottorato di Ricerca in Ingegneria dell'Informazione
Indirizzo: Ingegneria elettronica e delle telecomunicazioni

CICLO XXI

Stress, Overstress and Strain on AlGaN/GaN HEMT devices

Direttore della Scuola: Ch.mo Prof. Matteo Bertocco

Supervisore: Prof. Gaudenzio Meneghesso

Dottorando: Francesca Danesin

Index

Prefazione

I sistemi di comunicazione di ultima generazione, basati su amplificatori che operano a frequenze tra gli 1 ed i 40 GHz, necessitano di prestazioni rf sempre più spinte per quel che riguarda la potenza, l'efficienza, la linearità ed il basso costo. I semiconduttori basati sul Silicio (Si) o sull' Arseniuro di Gallio (GaAs) che sono abitualmente utilizzati per la costruzione di sistemi di comunicazione non sono in grado di soddisfare la domanda continua e crescente di prestazioni di potenza alle microonde. Questo tipo di dispositivi sono vicini al limite delle proprie prestazioni, lavorano con bassa efficienza e richiedono sistemi di raffreddamento di grandi dimensioni. I dispositivi basati su Nitruro di Gallio stanno quindi diventando interessanti per un gran numero di applicazioni: dalla optoelettronica all' elettronica di potenza. In particolare i transistor ad alta mobilità elettronica (HEMT) si sono rivelati promettenti per gli amplificatori a microonde ma la loro stabilità e affidabilità sono ancora uno dei problemi da risolvere per ottenere un prodotto commercializzabile e pronto per il mercato.

All'inizio di questa tesi saranno discusse le qualità dei dispositivi basati su GaN e verrà introdotto il progetto europeo Korrigan.

Il capitolo 2 tratterà di diversi test per valutare l'affidabilità a breve e lungo termine di dispositivi HEMT.

Nel capitolo 3 verrà discusso uno storage termico alla temperature di 300°C della durata di 2000 ore. Sarà identificato un nuovo meccanismo di guasto proprio dei GaN HEMT e verrà proposta una soluzione per prevenire problemi e rotture della passivazione.

Il capitolo 4 tratterà di esperimenti effettuati tramite stress inversi. I risultati ottenuti mostreranno che la scarsa qualità del materiale epitassiale può contribuire al degrado delle proprietà di un GaN HEMT.

Nel capitolo 5 verranno alla fine analizzate le proprietà di breakdown di dispositivi basati su Nitruro di Gallio. Sono stati svolti esperimenti a due e tre terminali, misure TLP e con il modello HBM.

Abstract

Defence radar and wireless communication systems have a drastic need for increased rf performance for high power, high efficiency, high linearity and low-cost monolithic amplifiers operating in the 1-40 GHz frequency range. Semiconductor devices based on Silicon (Si) or Gallium Arsenide (GaAs) are currently used for the fabrication of communication systems but they are not able to deal with the continuous increase in demand for microwave power performances: those devices are very close to their limit, working with a poor efficiency and requiring large cooling systems. Therefore Gallium nitride-based devices are becoming extremely attractive for a wide range of applications, from optoelectronics to power electronics. In particular, High Electron Mobility Transistors (HEMT) are emerging as a key technology for rf and microwave amplifiers, but their stability and reliability is still one of the main issue that has to be solved in order to achieve production level quality devices.

In the beginning the advantages of GaN-based devices will be briefly discussed and the European project Korrigan will be introduced.

Chapter 2 will deal with short and long term reliability tests performed on different wafers to study the influence of different bias point on HEMT degradation.

In Chapter 3 a thermal storage performed for 2000 hours at 300°C will be discussed. A new failure mechanism on GaN HEMTs will be identified and an improved passivation deposition process will be developed to prevent problem with passivation.

Chapter 4 will be focused on reverse-bias step stress experiments. Results obtained show that the epitaxial material contributes to enhance reverse-bias degradation of GaN HEMTs.

In Chapter 5 the characterization of the breakdown properties of the GaN-based devices has eventually been analyzed. We have performed two terminal and three terminal breakdown, TLP and the HBM model measurements.

Chapter 6 will summarize the results obtained.

Publications

1) A.Sozza, C. Dua, N. Sarazin, E. Morvan, S.L. Delage, F. Rampazzo, A. Tazzoli, **F. Danesin**, G.Meneghesso, E. Zanoni, A. Curutchet, N. Malbert and N. Labat, "*Traps characterization in Si-doped GaN/AlGaN/GaN HEMT on SiC by means of low frequency techniques*", HETECH 2005-14th International Workshop on Heterostructure Technology

2) A.Sozza, C. Dua, E. Morvan, M. A. di Forte-Poisson, S. Delage, F. Rampazzo, A. Tazzoli, **F. Danesin**, G. Meneghesso, E. Zanoni, A. Curutchet, N. Malbert , N. Labat, B. Grimber and J.-C. De Jaeger, "*Evidence of traps creation in GaN/AlGaN/GaN HEMTs after a 3000 hour on-state and off-state hot electron stress*", Accepted at IEDM 2005, 2005 IEEE International Electron Devices Meeting –Washington, 5-7 December

3) **F.Danesin**, F.Zanon. S.Gerardin, F.Rampazzo, G.Meneghesso, E.Zanoni, A.Paccagnella, "*Degradation induced by 2-MeV Alpha Particles on AlGaN/GaN High Electron Mobility Transistors*" Microelectronic Reliability, Vol. 46, n. 9-11, pp. 1750-1753

4) F. Zanon, **F. Danesin**, S. Gerardin, F. Rampazzo, G. Meneghesso, E. Zanoni, and A. Paccagnella, "*Impact of 2-MeV Alpha Irradiation on AlGaN/GaN High Electron Mobility Transistors*", WOCSDICE 2006-30th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe

5) F. Zanon, **F. Danesin**, G. Montanari, G. Meneghesso, and E. Zanoni "*Investigation on charge trapping phenomena leading to kink effect on AlGaN/GaN HEMTs*", WOCSDICE 2007- 31th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe

6) A. Tazzoli, **F. Danesin**, C. Ongaro, F. Rampazzo, F. Zanon, E. Zanon,and G. Meneghesso *"High Voltage Electrical Characterization of Field-Plate Gate HEMT Devices"*, HETECH 2007-16th European Workshop on Heterostructure Technology

7) M. Faqir, G. Verzellesi, F. Fantini, A. Cavallini, A. Castaldini, **F. Danesin**, G. Meneghesso,and E. Zanoni *"Interpretation of Buffer-Trap Effects in AlGaN-GaN HEMTs",* HETECH 2007-16th European Workshop on Heterostructure Technology

8) A.Tazzoli, **F. Danesin**, E. Zanoni, G. Meneghesso "*ESD Robustness of AlGaN/GaN HEMT Devices*", accepted for oral presentation at the 29th Electrical Overstress/Electrostatic Discharge Symposium Proc., EOS/ESD 2007.

9) M. Faqir, G. Verzellesi, F. Fantini, **F. Danesin** , F. Rampazzo , G. Meneghesso, E. Zanoni, A. Cavallini, A. Castaldini, N. Labat, A. Touboul, C. Dua *"Characterization and Analysis of Trap-Related Effects in AlGaN-GaN HEMTs",* ESREF 2007

10) E. Zanoni, G. Meneghesso, G. Verzellesi, **F. Danesin**, M. Meneghini, F. Rampazzo, A. Tazzoli, F. Zanon, *"A review of failure modes and mechanisms of GaN-based HEMT's"*, invited paper at the 2007 IEEE International Electron Device Meeting, IEDM 2007

11) G. Meneghesso, G. Verzellesi, **F. Danesin**, M. Meneghini, F. Rampazzo, A. Tazzoli, F. Zanon, E. Zanoni, "*Degradation of GaN HEMT at high drain voltages"* , ISMOT 2008

12) **F. Danesin**, A, Tazzoli, F. Zanon, G. Meneghesso, E. Zanoni, A. Cetronio, C. Lanzieri, S. Lavanga, M. Peroni, and P. Romanini "*Thermal Storage Effects on AlGaN/GaN HEMT*", Microelectronic Reliability, Vol. 48, n. 8-9, pp. 1361-1365

13) A. Tazzoli, F. Zanon, **F. Danesin**, E. Zanoni, G. Meneghesso, "*Electrical Characterization and Reliability Study of HEMTs on Composite Substrates under High Electric Fields*", Microelectronic Reliability, Vol. 48, n. 8-9, pp. 1361-1365

14) F. Zanon, **F. Danesin**, A. Tazzoli, G. Montanari, A. Chini, J. Thorpe, C. Gaquière, G. Meneghesso, and E. Zanoni "*High power performances of GaN HEMT on SopSiC substrate*", 32nd Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe, WOCSDICE 2008

15) **F. Danesin**, A. Tazzoli, F. Zanon, G. Meneghesso, E. Zanoni, A. Cetronio, C. Lanzieri, S. Lavanga, M. Peroni, and P. Romanini, "*Correlation between traps location and dispersion effects in AlGaN/GaN HEMTs*", HETECH 2008-17th European Workshop on Heterostructure Technology

16) F. Zanon, N. Ronchi, **F. Danesin**, P. Bove, R. Langer, J. Thorpe, A. Stocco, and G. Meneghesso "An investigation of reliability on hybrid substrates GaN-HEMTs", HETECH 2008-17th European Heterostructure Technology Workshop

17) Meneghesso, G.; Verzellesi, G.; **Danesin, F**.; Rampazzo, F.; Zanon, F.; Tazzoli, A.; Meneghini, M.; Zanoni, E. "*Reliability of GaN High-Electron-Mobility Transistors: State of the Art and Perspectives*" , IEEE Transactions on Device and Materials Reliability, Vol. 8, Issue 2, June 2008 Pages:332–343

18) Faqir, M.; Verzellesi, G.; Chini, A.; Fantini, F.; **Danesin, F**.; Meneghesso, G.; Zanoni, E.; Dua, C.,"*Mechanisms of RF Current Collapse in AlGaN–GaN High Electron Mobility Transistors*", ,IEEE Transactions on Device and Materials Reliability, Vol. 8, Issue 2, June 2008 Pages:240–247

19) F. Zanon, **F. Danesin**, A. Tazzoli, M. Meneghini, N. Ronchi, A. Chini, P. Bove, E. Zanoni, and G. Meneghesso "*Reliability aspects of GaN-HEMTs on composite substrates*", invited paper at the 7th International Conference on Advanced Semiconductor Devices and Microsystems, ASDAM 2008

20) G. Meneghesso, **F. Danesin**, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni "*Light emission in GaN HEMTs: a powerful characterization and reliability tool*", invited paper at the International Workshop on Nitride semiconductor, IWN 2008

21) G. Verzellesi, M. Faqir, A. Chini, F. Fantini, G. Meneghesso, E. Zanoni, **F. Danesin**, F. Zanon, F. Rampazzo, F.A. Marino, A. Cavallini, A. Castaldini, "False Surface-Trap Signature Induced by Buffer Traps in AlGaN-GaN HEMT", IRPS 2009

1. Gallium Nitride devices

1.1 Introduction

Defence radar and communication systems as well as wireless communication systems have a drastic need for increased rf performance and particularly for high power, high efficiency, high linearity and low-cost monolithic amplifiers operating in the 1-40 GHz frequency range. Mainstream III-V solid-state technology, mainly GaAs and more recently SiGe devices, and alternative solutions such as vacuum tubes, fall short of satisfying these requirements simultaneously. Therefore there is an increased interest in newer wide band-gap materials, which can potentially fulfil these requirements thanks to superior inherent material properties including high breakdown electric field, high electron mobility and saturation carrier velocity, and high thermal conductivity. The higher breakdown electric field allows operation at higher voltages, which means that for the same power level, much higher matching

impedances, lower power recombination losses in multi-transistor amplifiers and better energy efficiencies at lower circuit complexity will be possible. The intrinsic high thermal stability of the material should allow operation at higher temperatures, requiring less stringent (and less expensive) thermal management solutions for the packaging of high power amplifiers. Also thanks to the very high power-density of GaN devices, there is a real necessity to evaluate the technology reliability and to explore packaging and heat sink solutions, which will provide optimum thermal management. During the past decade, GaN HEMT technology has attracted considerable interest and rapid and impressive progress has been made mainly in the US and Japan in the development of GaN materials and GaN-based processes and devices [1-3]. The GaN semiconductor materials show a large potential for high power amplification at microwave and millimetre-wave frequencies [4-6]. Adequate MMIC integration technologies are now available on different types on substrates [7-9]. Also, GaN power HEMTs should ultimately show very high reliability due to the chemical inertness of the material and very high robustness and low sensitivity to space radiation, due to the large breakdown field and temperature stability.

1.2 GaN HEMT reliability issues

In the last years, GaN HEMTs have been subject to various optimization processes, starting from the material properties, to the control of surface and buffer properties aimed at reducing transient phenomena, the "current collapse" problems and electrical degradation. A better control of short-channel effects, gate current, and degradation phenomena at high electric fields, together with the development of suitable structures for the menagement of the electric field (using T-shaped and Γ-shaped gates and field-plates) have lead to the progressive increase of the operation drain voltage from 12 to 24 and 48 V even if many issues remain open for there devices. Parametric and gradual degradation (decrease in I_{DSS} and g_m, increase in gate-lag effects) are not accelerated by the electric field only; in fact the most dangerous conditions for device reliability occur when both channel current and a fairly high electric field are present in the device, i.e., it is required the presence of hot electrons.

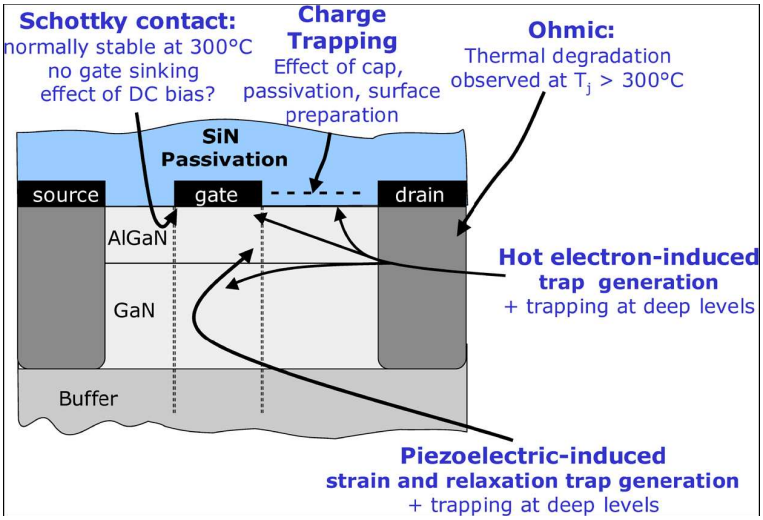


Figure 1.1 GaN HEMT problems

Hot electrons may be trapped on the device surface, in the AlGaN or in the buffer, giving rise to reversible degradation of I_{DSS} and g_m; they can also generate traps, thus promoting further charge trapping, see Fig. 1.1. Several authors have reported their results in the literature; main features can be summarized as follows.

The degradation involves the surface of the AlGaN: Kelvin probe experiments show changes in the surface potential of the gate-drain region, with accumulation of negative charge [11]. Passivation of the device surface with SiN has a healthy effect on hot-electron degradation; it is not clear, however, whether this beneficial effect is due to reduction of surface deep levels or to the passivation of traps induced by hydrogen indiffusion, associated with PECVD SiN deposition [11], [12]; reliability is improved if a low-power NH_3 plasma treatment is adopted before depositing the SiN passivation layer [13]. The authors in [14] speculate that the NH_3 treatment may either improve the resistance to hot-electron damage through the strengthening of bonds in the material or reduce the effects of hot-electron damage through the incorporation of hydrogen which would passivate traps.

Jha *et al.* [15] have studied the influence of gate recess depth, formed by reactive ion etching, on hot-electron degradation in GaN HEMTs; they concluded that a drastic increase in the interface trap density at the AlGaN/GaN heterointerface resulted from the hot-electron stressing experiment. Another mechanism induces an early degradation of I_{DSS}: the larger the recess, the faster the degradation.

Noise measurements were adopted by Valizadeh and Pavlidis [16] in order to study the effect of DC and rf stress on AlGaN/GaN HEMTs: They concluded that hot-electron trapping is responsible for the observed degradation in both DC and rf tests. Coffie *et al.* [17] observed a negative activation energy for the degradation of output power in the junction temperature range −55 ◦C to 205 ◦C and concluded

that hot carrier induced degradation is the dominant degradation mechanism. It should be stressed, however, that there is no agreement on this topic in the literature, and that many authors have reported thermally activated degradation of GaN HEMTs, with positive activation energies ≈1.05–2.0 eV [10], [18]–[22].

Due to the differences in the device's structure and technologies, as well as in accelerated testing conditions and failure criteria, a comparison of the results of the experiments reported in literature is extremely difficult. Most of the above quoted papers, however, report gradual degradation of I_{DSS} and g_m, generation of deep levels and increase in gate-lag or current collapse phenomena compatible with the hot-electron failure mechanism.

In addition to the experiments described above, there are several works which describe failure modes which cannot be explained in the framework of hot electron-induced degradation, at least if only channel electrons are considered. Since significant changes in device electrical parameters and increase in transient effects have been observed after OFF-state accelerated tests with negligible channel current, many authors have proposed the existence of a failure mechanism accelerated by the electric field only, resulting in trap generation and charge trapping, with consequent decrease in I_{DSS}, g_m, and increase in the drain resistance R_D, and in the gate leakage current. A specific hypothesis has been recently formulated by Joh and del Alamo [23], [24]; according to the proposed mechanism, the electric field in the gate-drain region would increase the strain in the AlGaN/GaN heterojunction ("inverse piezoelectric effect") eventually resulting in strain relaxation and crystallographic defect formation. This would compromise carrier transport properties and electron concentration in the access region, thus increasing *R*D and reducing *g*m; gate leakage current would then increase due to the enhanced trap-assisted tunneling and hopping phenomena in the AlGaN. The increase in strain has been experimentally evaluated by means of micro-Raman spectroscopy by Sarua *et al.* [25]. Moreover, several authors have suggested that reduced strain in the AlGaN barrier leads to improved device reliability [26]–[28], while other authors have found a dependence of the time to failure on the substrate and epitaxial material quality [10]. Finally, this failure mechanism would be thermally activated with a positive activation energy (which is inconsistent with the channel hot-electron degradation mechanism), which has been actually observed by many authors. Joh and del Alamo [24] have found that there is a critical gate-drain voltage which triggers this effect, around $V_{GD} \approx 20-30$ V for the tested devices. The inverse piezoelectric effect and the preexisting strain of the AlGaN/GaN structure certainly have a negative influence on device reliability. This is one of the reasons motivating research on InAlN as barrier layer, where piezoelectric effect is not

present. InAlN/GaN HEMTs have already demonstrated high breakdown voltage, low leakage current, and high-temperature operation [29]. Other mechanisms may contribute to compromise the reliability of GaN devices biased in OFF-state at very high drain-gate voltages: 1) Electrons, injected from the gate electrode into the GaN due to trap assisted tunneling, can reach very high energies, damage the semiconductor surface and interfaces and induce traps [30]; 2) as the electric field is increased, vertical breakdown of the AlGaN layer can occur, as in the dielectric of a MOSFET structure, thus creating a damaged path between the gate and the GaN. EL microscopy can be very useful in detecting localized breakdown effects and evaluating degradation mechanisms in OFF-state. We carried out several step-stress experiments by reverse biasing the gate Schottky junction with drain and source contacts short circuited (*V*DS = 0 V) [24]. Gate voltage was decreased from −10 to −40 V in −5 V steps, with a duration of 2 min each. Since the gate-source distance is usually shorter than the gate-drain one, a larger stress is imposed on the gate-source junction with respect to the gate-drain one. As a consequence, breakdown (or localized strain-relaxation) occurs at the source edge. Localized damage points are created, inducing sudden "jumps" in the source current; each "jump" corresponds to the creation of a new breakdown point and is followed by a subsequent decrease in the source current, possibly due to trapping in the generated deep levels, which decreases locally the electric field and/or reduces the number of available traps for tunneling. Another remarkable feature is that the degradation does not proceed by enlarging the already damaged points, but by creating new ones. Very similar results have been shown by Inoue *et al.* [22], who suggested that sudden degradationoccurs due to preexisting current paths which fail under reverse bias test. Devices selected between samples that initially have a low current show indeed a longer lifetime with respect to high leakage HEMTs.

Excellent reliability values (MTTF = 106 h at *Tj* = 180 ◦C,[4]) have been recently announced for high-power devices operating at the low-frequency end of AlGaN/GaN HEMTs applications (*f* < 3.5 GHz). Devices operating at higher frequencies still suffer from reliability problems and require further improvements. In general, a better understanding of failure mechanisms of GaN HEMTs is urgently needed for the full exploitation of the capabilities of these devices. Results presented here have demonstrated that at moderate *V*DS bias, a parametric degradation occurs, due to the generation of deep levels in the gate-drain access region, with features similar to those attributed to hot-electron degradation in GaAs FETs. At high V_{GD}, in particular in pinch-off conditions, new failure mechanisms are triggered, leading to an increase in gate leakage current, and correlated with localized defect creation.

1.3 Korrigan project

KORRIGAN project, launched in 2005 to accelerate the development of independent GaN HEMT foundries in Europe, addresses several key research areas such as materials, processing, reliability, thermal management and advanced packaging solutions. The benefits of GaN technology will be evaluated at system level with the fabrication of circuit, MMIC and module demonstrators. The project is supported by the MOD of seven nations and is primarily dedicated to defence applications. The KORRIGAN consortium consists of major European system houses and research laboratories, under the lead of Thales Airborne Systems, providing all the necessary competence for the establishment of the future GaN HEMT supply chain.

KORRIGAN is a large-scale European joint Research and Technology Project aiming at the development of microelectronics components. Seven nations are contributing to KORRIGAN: France also acting as the MOD management group, Italy, The Netherlands, Germany, Spain, Sweden and the United Kingdom. The KORRIGAN consortium, placed under the lead of Thales Airborne Systems (France), consists of 29 partners from the 7 contributing nations providing all the necessary competence in all key areas dedicated to semiconductor technologies such as substrate growth, device processing, circuit design and modelling, circuit packaging and integration. Also, in order to increase the project efficiency, the KORRIGAN consortium will share a very large number of test equipment, as well as characterisation and evaluation means. The main objective of KORRIGAN is to develop a stand alone European supply chain and capability for GaN HEMT technology which will provide all major European defence industries with reliable state-of-the-art GaN foundries services.

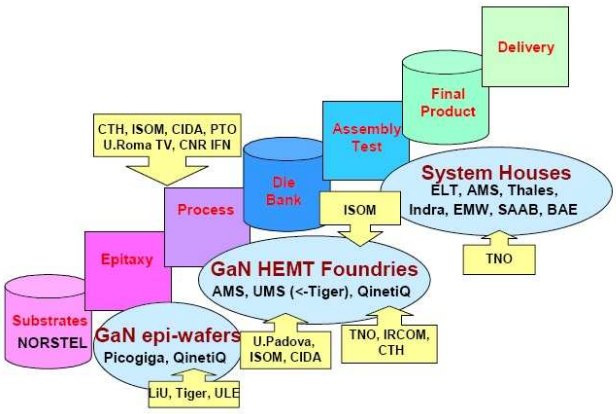


Figure 1.2 Supply chain for GaN HEMT process

For that purpose, there are four major technical objectives:

- To establish a European supply chain for the manufacture of GaN HEMT devices and MMICs.
- To assess the reliability and reproducibility of existing GaN device technologies within Europe in order to identify preferred processing options.
- To demonstrate the technology and the supply chain through the fabrication and testing of selected demonstrators for key S-band, X-band and wide-band applications.
- To evaluate the benefit of the technology at system level.

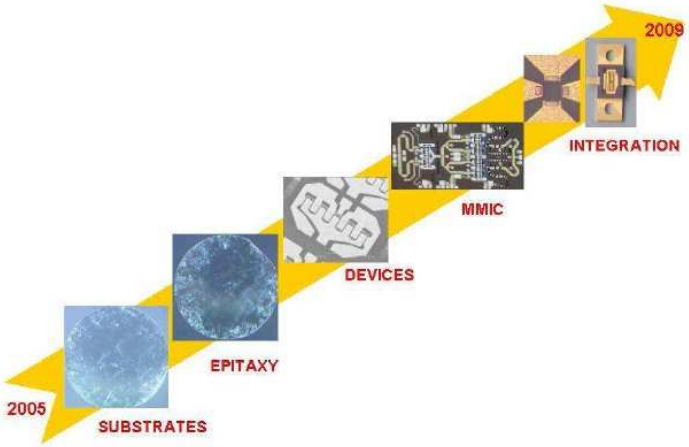


Figure 1.3 GaN HEMT technology development roadmap.

In order to successfully achieve the project goals and enable the development of leading GaN technology at the horizon of 2009, an integrated methodology has been setup and the project has been organised into 4 subprojects dedicated to materials, device and circuit processing technologies, reliability evaluation, thermal management and packaging solutions. Several demonstrators will be designed to validate GaN technology for various applications: S-band HPA, X-band and wideband HPA, LNA and switches. Materials Wideband gap semiconductor substrates will provide the foundation for the GaN HEMT technology. Silicon Carbide (SiC), Sapphire and Silicon materials will be considered, with a stronger focus on the growth of bulk crystal of SiC subtrates using HTCVD techniques. Substrate diameter expansion will be a key issue to ensure the economic maturation and to guarantee cost-effective industrial access to the technology. Also for each material, several types of epitaxial growth using both MBE and MOCVD techniques will be studied and characterised using a common approach.

The development activities will aim at establishing the access to a global manufacturing process of GaN HEMT devices and MMICs on SiC, Silicon and

Sapphire substrates. The work packages will cover the development of main technological aspects of circuit manufacturing including: generic technologies for active devices and passive circuits; design and manufacturing of devices; design and manufacturing of MMICs; and extraction of models from DC-RF characterisation. A common PCM will be exploited.

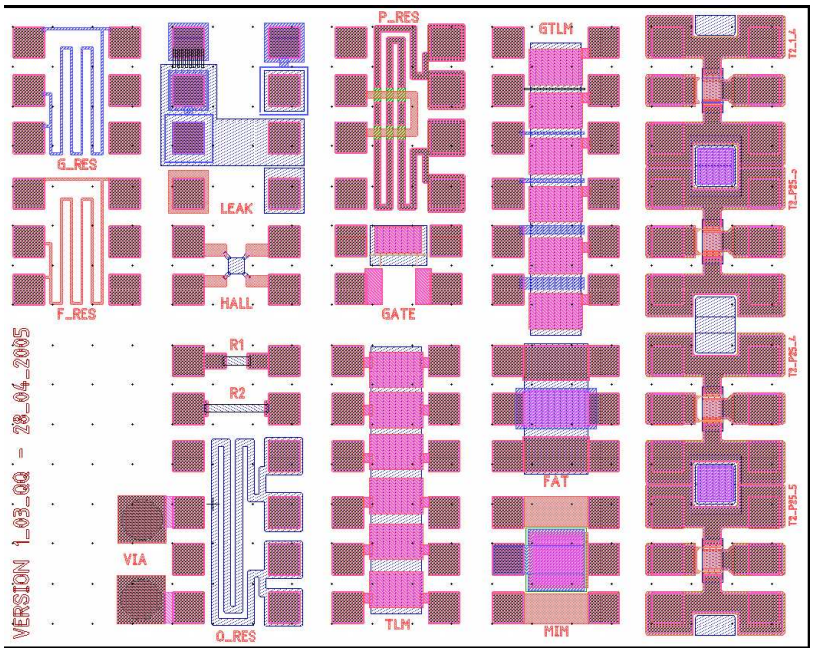


Figure 1.4 Korrigan PCM

The work is focused on the assessment of GaN technology regarding reliability aspects. Work packages will include: the study of parasitic effects, such as current collapse, which result from trapping effects occuring in the substrate; the systematic evaluation of the long-term reliability of GaN HEMT devices and passives; the identification and understanding of failure mechanisms based of the analysis of failed devices; and the evaluation of device robustness to extreme operating regime.

The objective of this subproject is to develop the suitable thermal environment for the use and integration of GaN power devices if current systems. The work will address the following issues: the design of optimised thermal cells and the improvement of heat sinking efficiency by reducing the device thermal resistance; the study of advanced assembly solutions and power packages; the simulation of the thermal environment of devices and circuits.

The KORRIGAN consortium is the largest organisation ever established in Europe for research in the field of microelectronics. The success of the project will be guaranteed by a very high degree of cooperation between partners relying on the use of common test plans, PCM and design strategies, and on the sharing of

characterisation equipment. Such a large-scale project anticipates the future EDA organisation of research in Europe.

1.4 References

[1] R.J. Trew, "SiC and GaN transistors: Is there one winner for microwave power applications?," Proceedings of the IEEE, vol. 90, no 6, pp.1032-47, June 2002.

[2] U.K. Mishra, et al., "AlGaN/GaN HEMTs: An overview of device operation and applications," Proceedings of the IEEE, vol. 90, no 6, pp. 1022-31, June 2002.

[3] M. Rosker, "Wide bandgap semiconductor devices and MMICs: a DARPA perspective," 2005 International Conference on Compound Semiconductor Manufacturing Technologies (GaAs MANTECH) Digest, 2005.

[4] Y.F. WU, et al., "30-W/mm GaN HEMTs by field plate optimization," IEEE Electron Device Letters, vol. 25, no 3, pp. 117- 119, March 2004.

[5] Y. Okamoto, et al., "179W recessed-gate AlGaN/GaN heterojunction FET with field-modulating plate," Electronics Letters, vol. 40, issue 10, pp. 629-631, May 2004.

[6] A. Wakejima, et al., "280W output power single-ended amplifier using single-die GaN-FET for W-CDMA cellular base stations," Electronics Letters, vol. 41, no 18, pp. 1004-05, September 2005.

[7] W. Nagy, et al., "150W GaN-on-Si RF power transistor," IEEE MTT-S International Microwave Symposium Digest, Los Angeles, June 2005.

[8] D.M. Fanning, et al., "25W X-band GaN on Si MMIC," 2005 International Conference on Compound Semiconductor Manufacturing Technologies (GaAs MANTECH) Digest, 2005.

[9] M. Nishijima, et al., "A K-band AlGaN/GaN HFET MMIC Amplifier on Sapphire using novel superlattice cap layer," IEEE MTT-S International Microwave Symposium Digest, Los Angeles, XXXX.

[10] Y. C. Chou, D. Leung, I. Smorchkova, M. Wojtowicz, R. Grundbacher, L. Callejo, Q. Kan, R. Lai, P. H. Liu, D. Eng, and A. Oki, "Degradation of AlGaN/GaN HEMTs under elevated temperature lifetesting," *Microelectron. Reliab.*, vol. 44, no. 7, pp. 1033–1038, Jul. 2004.

[11] G. Koley, V. Tilak, L. F. Eastman, and M. G. Spencer, "Slow transients observed in AlGaN/GaN HFETs: Effects of SiNzx passivation and UV illumination," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 886–893, Apr. 2003.

[12] J. A. Mittereder, S. C. Binari, P. B. Klein, J. A. Roussos, D. S. Katzer, D. F. Storm, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Current collapse induced

in AlGaN/GaN high-electron-mobility transistors by bias stress," *Appl. Phys. Lett.*, vol. 83, no. 8, pp. 1650–1652, 2003.

[13] T. Kunii, M. Totsuka, Y. Kamo, Y. Yamamoto, H. Takeuchi, Y. Shimada, T. Shiga, H. Minami, T. Kitano, S. Miyakuni, S. Nakatsuka, A. Inoue, T. Oku, T. Nanjo, T. Oishi, T. Ishukawa, and Y. Matsuda, "A high reliability GaN HEMT with SiN passivation by Cat-CVD," in *Proc. IEEE CSIC Symp.*, 2004, pp. 197–200.

[14] A. P. Edwards, J. A. Mittereder, S. C. Binari, D. Scott Katzer, D. F. Storm, and J. A. Roussos, "Improved reliability of AlGaN/GaN HEMTs using an NH3 plasma treatment prior to SiN passivation," *IEEE Electron Device Lett.*, vol. 26, no. 4, pp. 225–227, Apr. 2005.

[15] S. K. Jha, B. H. Leung, C. Surya, H. Schweizer, and H. Pilkhuhn, "Studies of hot-electron degradation in GaN HEMTs with varying gate recess depths," in *Proc. COMMAD*, 2004, pp. 33–36.

[16] P. Valizadeh and D. Pavlidis, "Effects of rf and DC stress on AlGaN/GaN MODFETs: A low-frequency noise-based investigation," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 555–563, Sep. 2005.

[17] R. Coffie, Y. Chen, I. P. Smorchkova, B. Heying, V. Gambin, W. Sutton, Y. C. Chou, W. B. Luo, M. Wojtowicz, and A. Oki, "Temperature and voltage dependent rf degradation study in AlGaN/GaN HEMTs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2007, pp. 568–569.

[18] E. L. Piner, S. Singhal, P. Rajagopal, R. Therrien, J. C. Roberts, T. Li, A. W. Hanson, J. W. Johnson, I. C. Kizilyalli, and K. J. Linthicum, "Device degradation phenomena in GaN HFET technology: Status, mechanisms, and opportunities," in *IEDM Tech. Dig.*, 2006, pp. 1–4.

[19] A. M. Conway, M. Chen, P. Hashimoto, P. J. Willadsen, and M. Micovic, "Accelerated rf life testing of GaN HFETs," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2007, pp. 472–475.

[20] S. Singhal, J. C. Roberts, P. Rajagopal, T. Li, A. W. Hansen, R. Therrien, J. W. Johnson, I. C. Kizilyalli, and K. J. Linthicum, "GaN-on-Si failure mechanisms and reliability improvements," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2006, pp. 95–98.

[21] P. Saunier, C. Lee, A. Balistreri, D. Dumka, J. Jimenez, H. Q. Tserng, M. Y. Kao, P. C. Chao, A. Souzis, I. Eliashevich, S. Guo, J. del Alamo, J. Joh, and M. Shur, "Progress in GaN performance and reliability'' *Proc. Device Res. Conf.*, 2007, pp. 35–36.

[22] Y. Inoue, S. Masuda, M. Kanamura, T. Ohki, K. Makiyama, N. Okamoto, K. Imanishi, T. Kikkawa, N. Hara, H. Shigematsu, and K. Joshin, "Degradation-mode analysis for highly reliable GaN HEMT," in *IEEE MTT-S Int. Microw. Symp.*, 2007, pp. 639–642.

[23] J. Joh and J. A. del Alamo, "Mechanisms for electrical degradation of GaN high electron mobility transistors," in *IEDM Tech. Dig.*, 2006, pp. 415–418.
[24] J. Joh and J. A. del Alamo, "Gate current degradation mechanisms of GaN high electron mobility transistors," in *IEDM Tech. Dig.*, 2007, pp. 385–388.
[25] A. Sarua, H. Ji, M. Kuball, M. J. Uren, T. Martin, K. J. Nash, K. P. Hilton, and R. S. Balmer, "Piezoelectric strain in AlGaN/GaN heterostructure field-effect transistors under bias," *Appl. Phys. Lett.*, vol. 88, no. 10, p. 103 502, Mar. 2006.
[26] C. Lee, L. Witkowski, H.-Q. Tserng, P. Saunier, R. Birkhahn, D. Olson, G. Munns, S. Guo, and B. Albert, "Effects of AlGaN/GaN HEMT structure on rf reliability," *Electron. Lett.*, vol. 41, no. 3, pp. 155–157, Feb. 2005.
[27] D. W. Gotthold, S. P. Guo, R. Birkhahn, and B. Albert, "Time-dependent degradation of AlGaN/GaN heterostructures grown on silicon carbide," *J. Electron. Mat.*, vol. 33, no. 5, pp. 408–411, May 2004.
[28] P. Valizadeh and D. Pavlidis, "Investigation of the impact of Al mole-fraction on the consequences of rf stress on Al*x*Ga1−*x*N/GaN MODFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 1933–1939, Sept. 2005.
[29] F. Medjdoub, J. F. Carlin, M. Gonschorek, E. Feltin, M. A. Py, D. Ducatteau, C. Gaquière, N. Grandjean, and E. Kohn, "Can InAlN/GaN be an alternative to high power / high temperature AlGaN/GaN devices?" in *IEDM Tech. Dig.*, 2006, pp. 1–4.
[30] D. Kumar Sahoo, R.K. Lal, H. Kim, V. Tilak, and L. F. Eastman, "High-field effects in silicon nitride passivated GaN MODFETs," *IEEE Trans.Electron Devices*, vol. 50, no. 5, pp. 1163–1170, May 2003.

2. DC life test

2.1 Introduction

Material quality and reliability issues are the key points for the industrial application of GaN-HEMTs that have demonstrated superb rf power performances [1-3], but are still subject to various degradation mechanisms when they operate at high electric fields and/or high channel temperatures [4-5]. Degradation induced by hot carriers and strain enhancement due to piezoelectric effect at high electric field, followed by relaxation consequent to defect creation, are two important mechanisms resulting in the generation of deep levels. In this chapter are presented the results of several accelerated tests carried out on various GaN-HEMT technologies. Main findings can be summarized as follows: at low V_{DS} values (~ 20 V), moderate degradation occurs, and a remarkable correlation exists between life tests bias points and the failure modes, possibly related to the different location of the damage along the channel, as shown by 2D device simulations; for V_{DS} > 20 V, even in pinch-off conditions, damage of the metal/semiconductor interface occurs at the drain edge in localized points corresponding to defects or strained areas, where gate current density is enhanced due to localized injection.

2.2 Long term DC life test in AEC1148

2.2.1 Test description

24 transistors from wafer AEC1148 with W_G = 8x75µm, L_G=0.25µm were selected to be put under DC test by 3-5Labs. The devices have been characterized before and after the stress in DC, frequency and transient regime. During the accelerated test 7 bias points (see Figure 2.1 and Table 2.1) were used. These bias points were chosen to study the ageing of the devices under classical bias conditions i.e. on-state, off-state and class A. We also aimed at enhancing possible hot carrier degradation that is why 3 different levels of drain current (0mA, 30mA and 250mA) were used at the same drain voltage (25V), corresponding respectively to the bias points C, D and E on
Figure 2.1.

The junction temperature was kept constant at 175°C and targeted to remain constant whatever the bias conditions. The test was performed in 9 steps with durations 2h, 4h, 8h, 24h, 43h, 159h, 180h, 590h and finally 1072h, leading to a cumulated time of 2082 hours. The test was concluded without catastrophic failure observed out of the 24 devices under test.

The bias points were presented on
Figure 2.1. The following test conditions have been applied:

- For bias points A and F, V_{DS} is adjusted to keep the dissipated power constant at the targeted value with V_{GS}=0V; the gate current is close to 0 µA.
- For bias points B, D and E, V_{DS} is set at the targeted value and the drain current is kept constant by an automatic control of the gate voltage in order to keep the dissipated power constant.
- Finally in the pinch-off mode, points C and G, V_{DS} and V_{GS} are constant

The test results can be summarized by rating bias point in order of severity as follows:

- it appears that the most stressful conditions (with up to 50% decrease in I_{DSS}) are those close to "class A" (bias point B and E) where there is a rather high electric field and a high density of current.
- The on-state conditions A and F, highest current density and lower electric field look the less stressful. The I_{DSS} decreases of less than 10% with almost no variation of the transconductance.

- Bias conditions with higher electric fields with no or little current, pinch-off conditions, are somewhere in between with about 15% decrease of the I_{DSS} and gm peak.

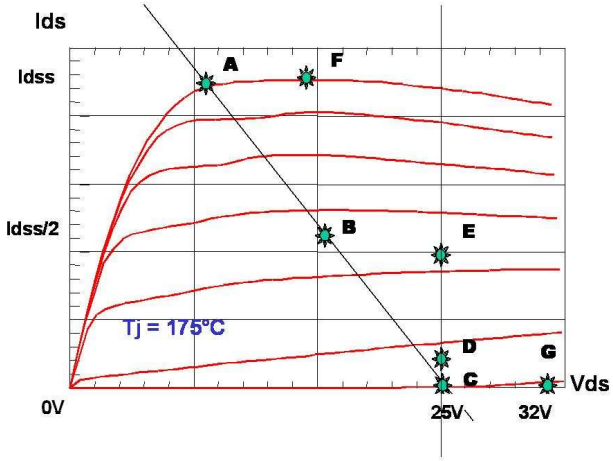


Figure 2.1 : Sketch of the output characteristics with the seven bias conditions

Condition	A	B	C	D	E	F	G
V_{DS} (V)	6	15.5	25	25	25	10.4	32
I_{DS} (mA)	600	300	0	30	250	600	0
P_D (W/mm)	6	7.75	0	1.25	10.4	10.4	0
V_{GS} (V)	0	-3	-8	-5.5	-3.8	0	-9
Tj (°C)	175	175	175	175	175	175	175

Table 2.1 Detailed initial bias conditions of the AEC1148 DC life test

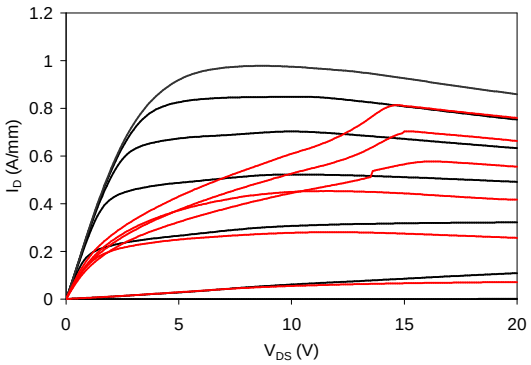
2.1.1. Failure analysis: DC degradation

Following the results previously reported we focussed our detailed analysis on the comparison of the main DC characteristics of the three main degradation points: A, B, C. In the following figures : Figure 2.2, Figure 2.3 and Figure 2.4, the I-V curves (diode, Id vs Vds output characteristics, trancharacteristics gm, and sub-threshold current characteristics), before and after stress, in the A, B, and C points

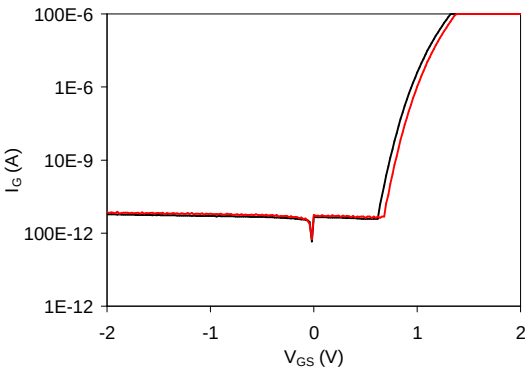
respectively are reported for some representative samples. The following consideration can be drawn by comparing the degradation modes:

1. Bias point A: devices stressed in the A bias point show a large degradation of the output I-V characteristics (Figure 2.2 A) which is not reflected in other curves (Figure 2.2 C, D), since no significant degradation of g_m, V_{TH} and diode characteristics are observed. This anomalous phenomenon will be explained later (see Paragraph. 0 and
2. Figure 2.1). It looks like the stress point A does not present any significant degradation (not considering Figure 2.2 A) both in the Schottky gate leakage current (see Figure 2.2 B) or in the drain current (see Figure 2.2 C and D) or in the sub-threshold current (see Figure 2.2 E). Finally no significant increase in dispersion phenomena is observed using gate-lag measurements (Figure 2.2 F).
3. Bias point B**:** shows a strong degradation of the output I-V characteristics (see Figure 2.3 A) that is correlated with the other curves (Figure 2.3 C, D). This stress point B presents large degradation of the Schottky gate contact that becomes almost ohmic (see Figure 2.3 B), large degradation of the drain current (see Figure 2.3 A, C and D) and in the sub-threshold current (see Figure 2.3 E). The decrease of the drain current is mainly correlated with a decrease of the g_m peak rather than with a threshold voltage shift. Finally the gate-lag curve shows a large decrease of the drain current (in line with is Figure 2.3 A) but no large transient are observed. These results indicate that generation of new traps is not the main degradation mechanisms. Charge trapping in the access regions and/or of degradation of electron mobility (due to charge trapping in the channel nearby) can better explain the observed degradation modes.
4. Bias Point C**:** shows a degradation that in general is intermediate between the one observed in the bias point A and B. In this condition, large electric field is applied to the device, but almost zero current is present. The Schottky diode is largely degraded (Figure 2.4 B). Differently from the stress bias point B the drain current reduction observed in Figure 2.4 A is mainly related to a threshold voltage shift (see Figure 2.4 C, D) rather than to a transconductance reduction. Similarly to the bias point B, the gate-lag curve shows a decrease of the drain current (in line with Figure 2.4 A) but no slow transients are observed. In this type of stress we have observed the larger shift of the threshold voltage, possibly due to the large reverse bias of the gate Schottky diode of this bias point.

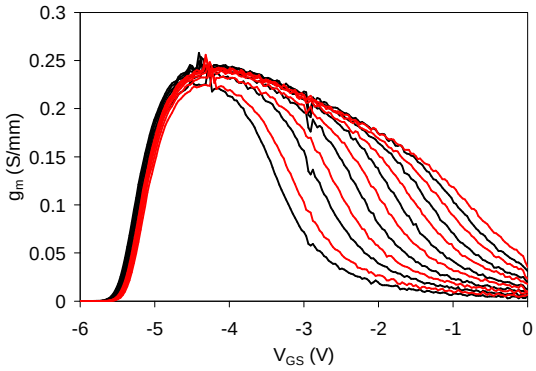
bias point A (device 27)



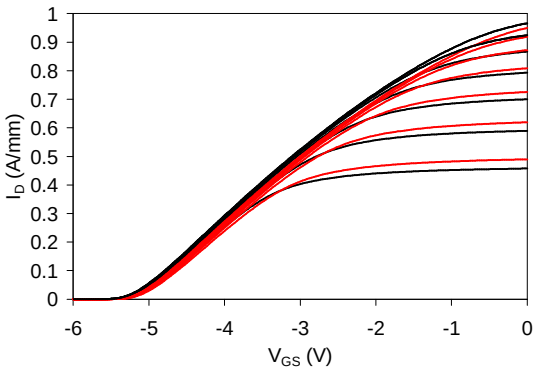
(A)



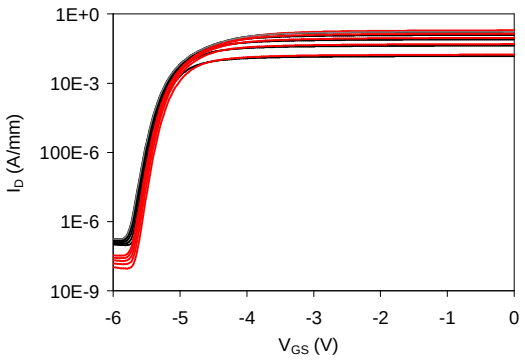
(B)



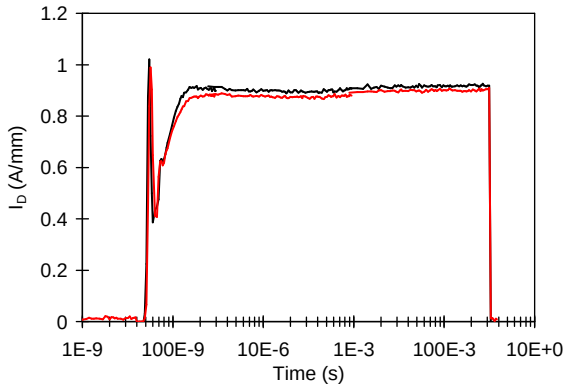
(C)



(D)



(E)

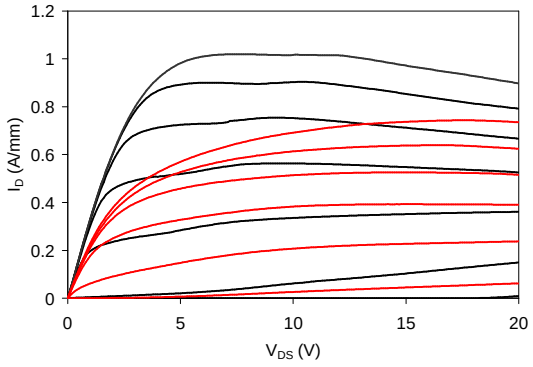


(F)

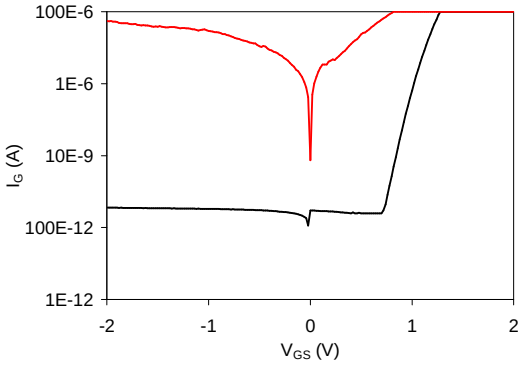
Figure 2.2. I_D vs V_{DS} output characteristics (A), diode (B), trans-characteristic g_m (C & D), sub-threshold current characteristics (E) and gate-lag measurements before (black lines) and after (red lines) the long term stress (2082 hrs) of device #27 stressed in the A bias point (see Figure 2.1 and Table 2.1)

Condition	A	B	C	D	E	F	G
V_{DS} (V)	6	15.5	25	25	25	10.4	32
I_{DS} (mA)	600	300	0	30	250	600	0
P_D (W/mm)	6	7.75	0	1.25	10.4	10.4	0
V_{GS} (V)	0	-3	-8	-5.5	-3.8	0	-9
Tj (°C)	175	175	175	175	175	175	175

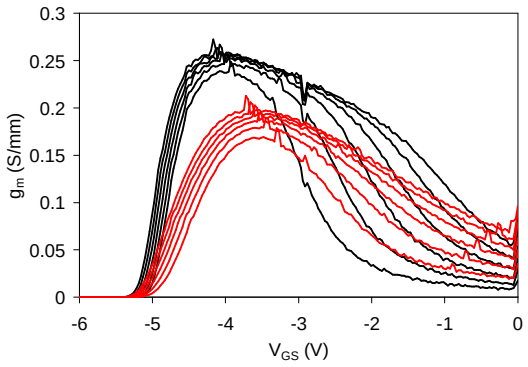
bias point B (device 29)



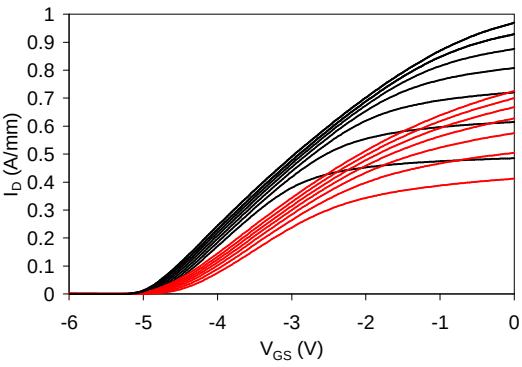
(A)



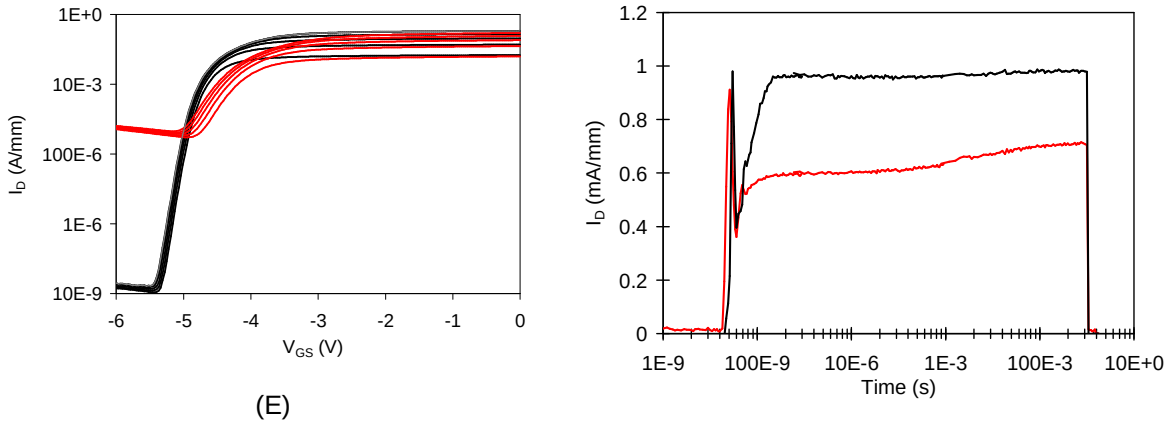
(B)



(C)



(D)

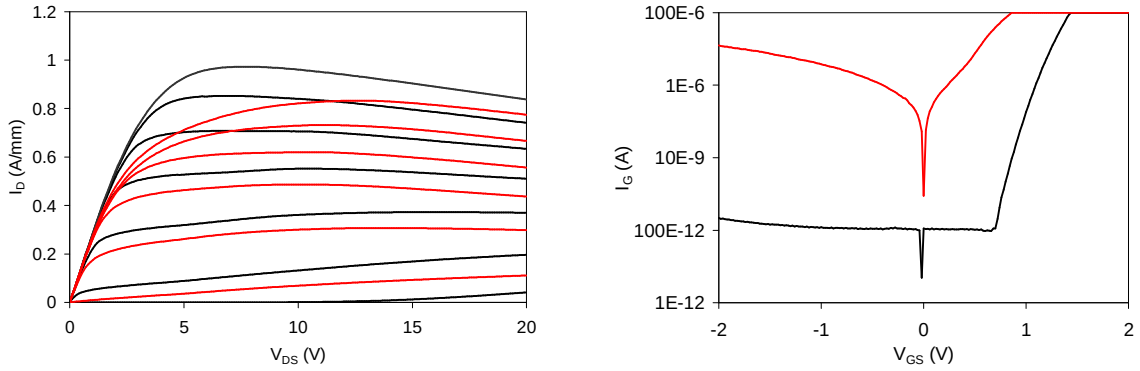


(E) (F)

Figure 2.3 I_D vs V_{DS} output characteristics (A), diode (B), trans-characteristic g_m (C & D), sub-threshold current characteristics (E) and gate-lag measurements before (black lines) and after (red lines) the long term stress (2082 hrs) of device #29 stressed in the B bias point (see Figure 2.1 and Table **2.1**)

Condition	**A**	**B**	**C**	**D**	**E**	**F**	**G**
V_{DS} (V)	6	15.5	25	25	25	10.4	32
I_{DS} (mA)	600	300	0	30	250	600	0
P_D (W/mm)	6	7.75	0	1.25	10.4	10.4	0
V_{GS} (V)	0	-3	-8	-5.5	-3.8	0	-9
Tj (°C)	175	175	175	175	175	175	175

bias point C (device 16)



(A) (B)

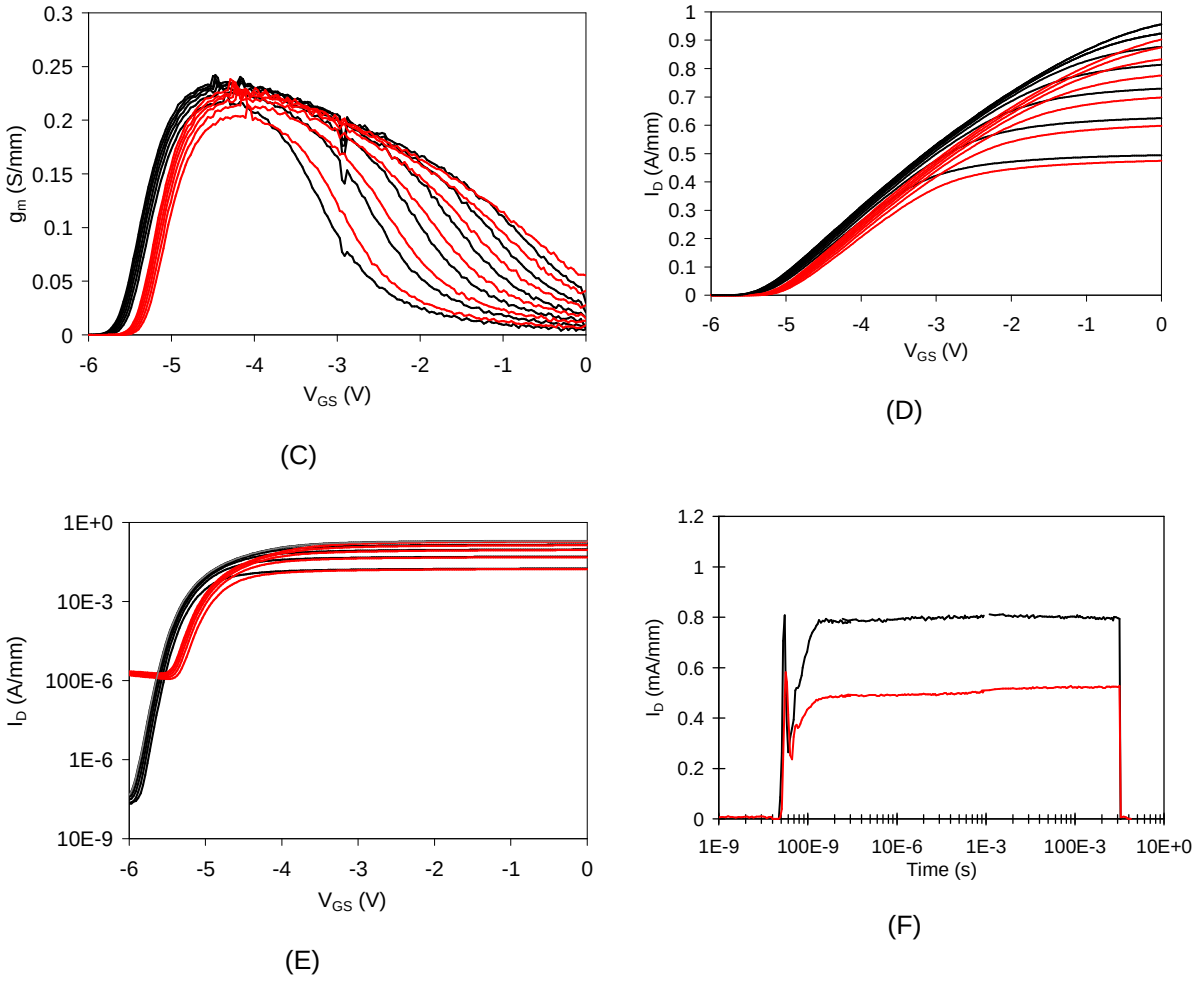


Figure 2.4 I_D vs V_{DS} output characteristics (A), diode (B), trans-characteristic g_m (C & D), sub-threshold current characteristics (E) and gate-lag measurements before (black lines) and after (red lines) the long term stress (2082 hrs) of device #16 stressed in the C bias point (see Figure 2.1 and **Table 2.1**)

Condition	A	B	C	D	E	F	G
V_{DS} (V)	6	15.5	25	25	25	10.4	32
I_{DS} (mA)	600	300	0	30	250	600	0
P_D (W/mm)	6	7.75	0	1.25	10.4	10.4	0
V_{GS} (V)	0	-3	-8	-5.5	-3.8	0	-9
Tj (°C)	175	175	175	175	175	175	175

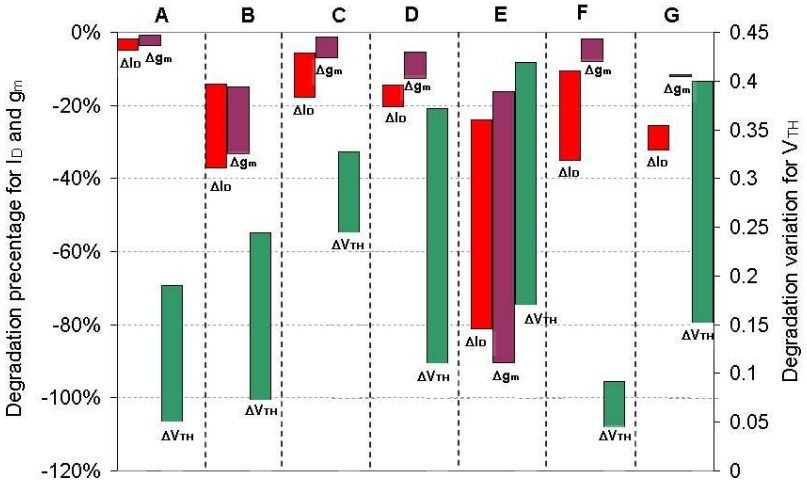


Figure 2.5 Summary of the variations of the main parameters (I_{DS} at V_{DS}=10V, g_{mpeak} at V_{DS}=10V and V_{TH} at V_{DS}=10V) observed after the 2080 hour stress test for all bias points.

2.1.2. Failure analysis: trapping phenomena

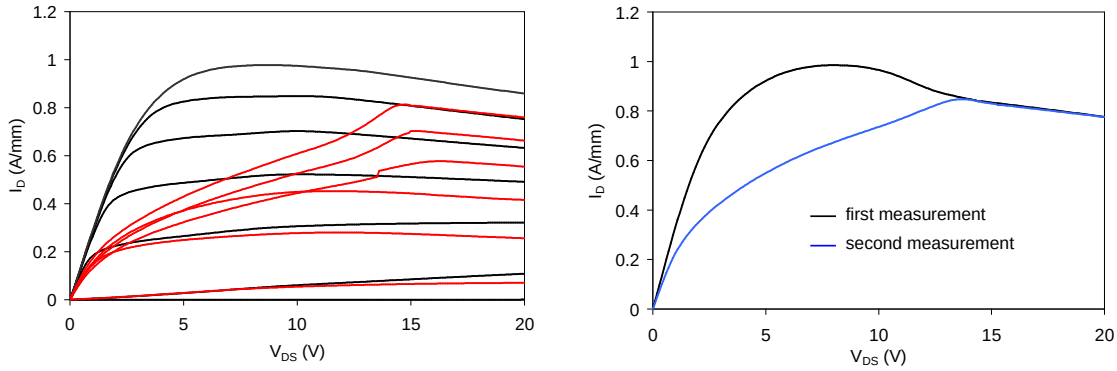
The characteristics of device 27, stressed in bias point A, before and after stress (presented in Figure 2.2) and reported again in Figure 2.6 A for a better readability, present an unclear situation as already highlighted. In this paragraph we clearly explain the origin of this anomalous behaviour.

In Figure 2.6 B we report the results of two measurements made in succession (just two repeated measurements in the same conditions, V_{GS}=0V and V_{DS} sweeping from V_{DS} = 0 V to V_{DS} = 20V). Clearly the second measurement is remarkably collapsed due to the first measurements. we can attribute this phenomena to negative charge trapping which generates a large reduction of the drain current at low V_{DS}. It is also speculated that during the first measurements the trapping starts roughly beyond the V_{DS} = 10 V where an anomalous drop is observed (see Figure 2.6 B, first measurement).

In order to better understand this trapping phenomena, we have carried out a number of repeated measurements as reported in the following lines. These experiments were carried out in order to identify at which voltage the trapping take

Device 27 After stress in bias point A

place.

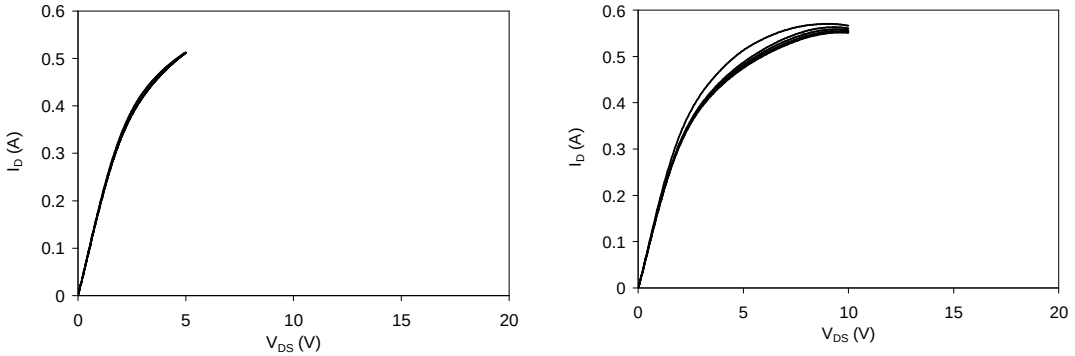


(A) (B)

Figure 2.6 (A) I_{DS} vs V_{DS} curves before and after stress of device #27. (B) Two repeated I_{DS} vd V_{DS} curves (at V_{GS}=0V) of device #27, black: first measurement, and blue: second measurement .

To this aim, we carried out repeated measurements (at fixed V_{GS}=0V) sweeping the V_{DS} values from 0V to different final values (5V, 10 V, 15V and 20V), see Figure 2.7 and Figure 2.8.

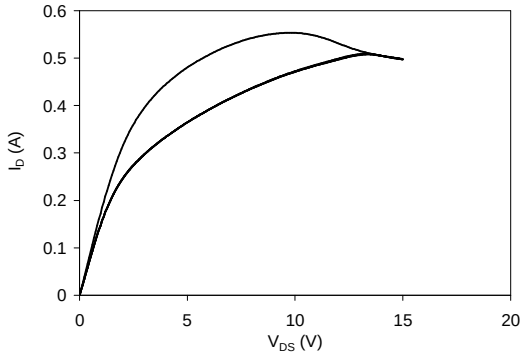
Repeated measurements (at V_{GS}=0V) up to 5V do not present any collapse (see Figure 2.7 A); while repeated measurements up to 10V start to show a small collapse (see Figure 2.7 B), repeated measurements up to 15V show a large collapse (see Figure 2.7 C). Repeated measurements up to 20 V shows the largest current collapse, see Figure 2.8. Finally the drain current slowly recovers to a value close to its initial value if the device is kept unbiased for a sufficiently long time (180 minutes), see Figure 2.9.



(A) (B)

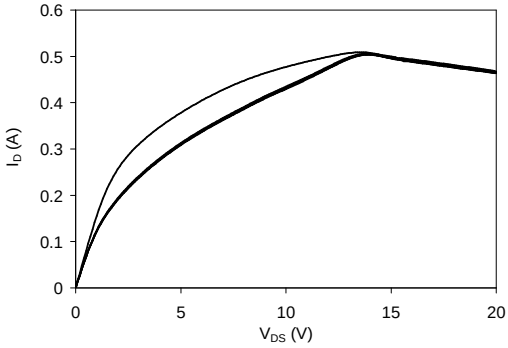
Five repeated measurements at V_{GS} = 0V up to 5 V.

Five repeated measurements at V_{GS} = 0V up to 10 V.



(C)

Five repeated measurements at V_{GS} = 0V up to 15 V.



(D)

Five repeated measurements at V_{GS} = 0V up to 20 V.

Figure 2.7 Repeated measurements with different final V_{DS} values in dev.27 stressed in bias point A.

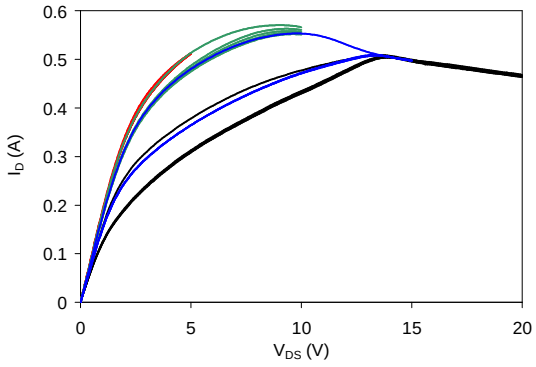


Figure 2.8 Succession of the curves shown in previous figures.

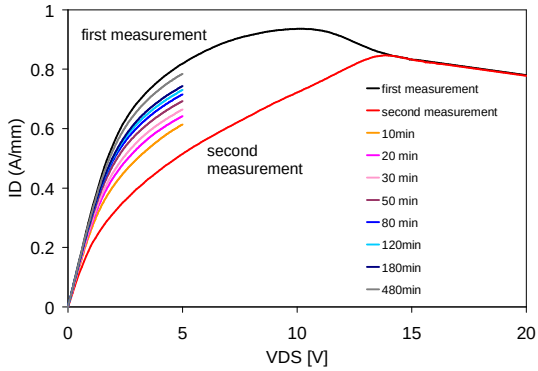


Figure 2.9 Two repeated measurements at V_{GS} =0V, with V_{DS} sweeping from 0 to V to 20 V. The other measurements at V_{GS} =0V, with V_{DS} sweeping from 0V to 5 V (to avoid further trapping) show I_{DS} recovery with time (device is kept unbiased at room temperature).

To try to localize where the trapping takes place, we have carried out the following experiment:

a) we chose the device 27 which was stressed at the bias point A. Then we stored it at room temperature without bias for a long time (more than one day) in order to be sure that the complete detrapping is achieved;

b) we measured the transconductance (I_D and g_m vs V_{GS}) at low V_{DS} values (1 V and 4.5 V) in order to avoid trapping during the measurements itself (as demonstrated in Figure 2.7 A);

c) We carried out two output I-V curves at V_{GS} =0V, V_{DS} sweeping from 0 V to 20 V reaching a trapped situation (see Figure 2.6 B);

d) we have re-measured the transconductance (I_D and g_m vs V_{GS}) at low V_{DS} values (1 V and 4.5 V)

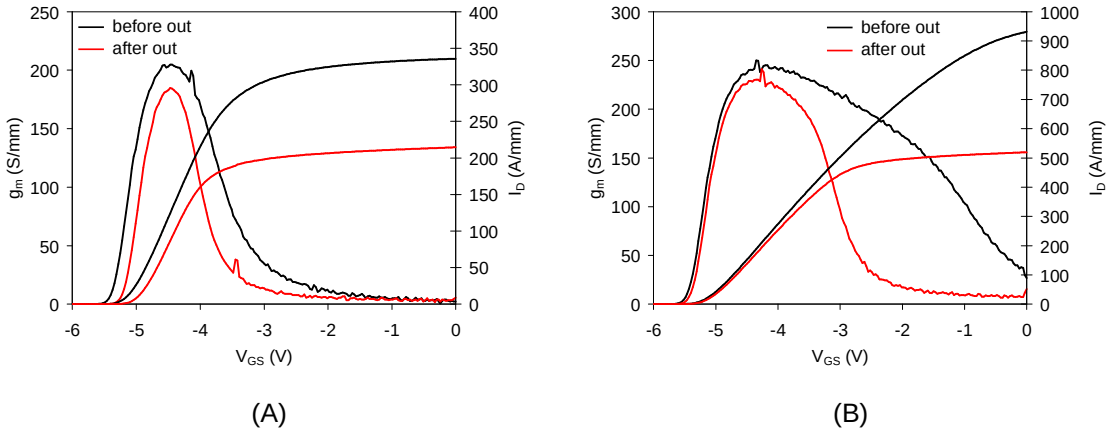


Figure 2.10 I_D and g_m vs V_{GS} transconductance curves measure at V_{DS} = 1 V (A) and at V_{DS} = 4.5 V (B) before (black lines) and after (red curves) two repeated measurements at Vgs=0V, with Vds sweeping from 0 to V to 20 V (same curves as in Figure 2.6B).

The results of this experiment is shown in Figure 2.10. As it can be seen, at low Vds values (Vds = 1V, see Figure 2.10 A) the Id decrease is correlated with a decreasing of the transconductance in all the Vgs range, possibly due to a carrier mobility degradation in the channel. At Vds values of 4.5 V (just below the saturation region, see Figure 2.10 B) a large drop of the Current and transconductance is observed ONLY in open channel condition. In general this degradation mode can be attributed to an increase of the parasitic drain resistance of the gate-to-drain access region; in particular the parasitic resistance increase should mainly take place close to the drain contact (far away from the gate contact). This degradation mechanism is consistent with the fact that the trapping takes place at Vds values larger that 10 V, when the saturation region is reached and high gate-to drain Electric Field are present, suggesting injection of hot

electrons in the gate-to-drain access region that will be trapped. This trap localization is confirmed by the fact that at high Vds values, no large collapse is observed (see Figure 2.6 B), since the channel (longitudinal) electric field is large and it masks the effects of the parasitic (vertical) electric field induced by the trapped charge.

To fully understand the "strange" measurements of devices stressed in "A" and "F" conditions it is also necessary to know the measurements orders; in fact the measurements are carried out with the following order:

1) Diode

2) g_{m1} (transconductance characteristics with Vds from 0.2 to 1.0 V)

3) g_{m2} (transconductance characteristics with Vds from 1.0 to .4.5 V)

4) g_{m3} (transconductance characteristics with Vds from 8 to 20 V)

5) Output characteristics (Vds from 0 to 20V and Vgs varying from -6V to 0V by 1V step).

Following all these consideration, now it becomes clear what happens during the measurements of devices stressed in A and F conditions:

i. Measurements of the gate Schottky diode do not generate any trapping;

ii. during "g_{m1}" and "g_{m2}" measurements devices will not reach bias values which lead to trapping, and hence they will not undergo any degradation

iii. during the Id vs Vds output measurements (which are carried out by stepping Vgs from closed channel to open channel conditions) trapping occurs during the measurement itself as Vds is swept beyond 10 V (with Vgs ≥ -4V).

The complete comparison between the behaviours of virgin and aged devices is summarized in Figure 2.11 where the pre_stress (virgin) curve and the two curves made after the stress are compared. Finally in Figure 2.12 we report the effect of light, having photon energy lower than the GaN energy gap, on the collapsed devices. As expected, light causes charge detrapping leading to a current recovery (green curve). This trapping mechanism was not observed in untreated devices.

A new failure mechanism has therefore been identified consisting in the generation of extremely slow traps, possibly located in the device access regions. The consequent decrease in drain current is significant only when the device is biased at Vds > 10V with Vgs > -4V. The devices which have been tested in points A and F are most affected by this failure mode possibly due to the simultaneous application of high current (1000 mA/mm) and high temperature. Nevertheless the other tested devices are also slightly affected, as shown in Figure 2.13 .

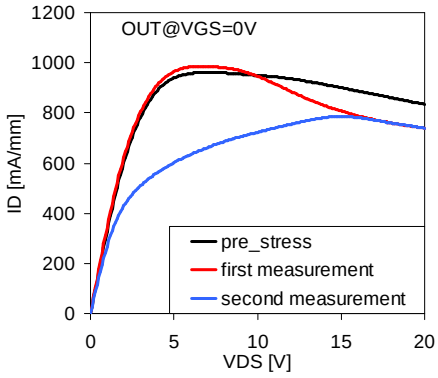


Figure 2.11 Id vs Vda curved (at Vgs=0V) in dev. #27 prior the stress (black line) and after the stress: Red line: first measure; Blue line: second measure.

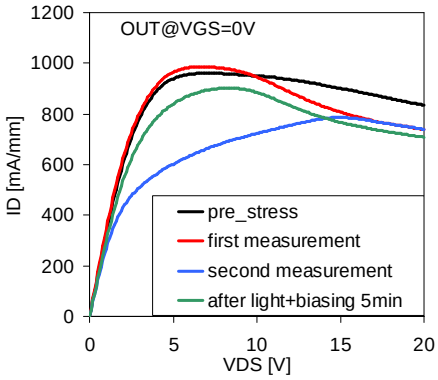


Figure 2.12 Same curves as Figure 2.11, with a subsequent measure carried out shining the device with light, having photon energy lower than the GaN energy gap

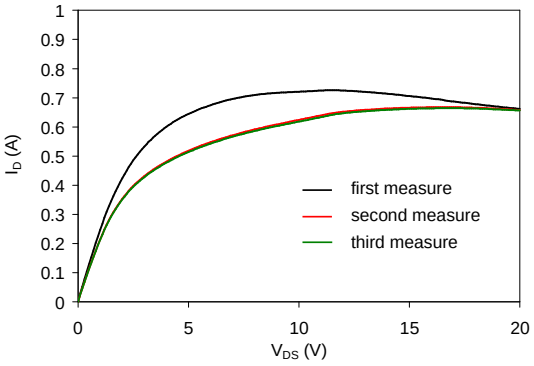


Figure 2.13 Three repeated Ids vd Vds curves (at Vgs=0V) of device #28 after the stress in the B bias point.

We have reported on Table 2.2 the main parameters degradations observed during the stress. It must be noted that for bias points A and F we have decided to use the "g_{m2}" curves and NOT the OUT curves to calculate the Id degradation. We must hence keep in mind that even if devices biased in Point A are not reported in Table 2.2 as presenting significant degradation, they are affected by the trapping/detrapping phenomena previously described. We will continue to investigate this phenomenon in the next period.

Bias condition	ΔI_D (%)	Δg_{mp} (%)	ΔV_T (mV)	Subthreshold	Trapping
A	5÷10%	2÷3 %	+150	no change	STRONG
B	25÷30%	30%	200	worse	Present
C	15%	5÷10%	250	worse	Present
D	15%	15%	350	worse	Present
E	50%	60%	??	worse	Present
F	10%	3÷5%	100	no change	STRONG
G	20%	10%	+250	worse	Present

Table 2.2 Main variations observed after the 2080 hour stress test.

Looking at the data reported on Table 2.2 we can draw the following considerations:

1) Point B and E are the most stressful conditions, followed by points in the close channel conditions (C, D and G) and those in open channel conditions are the less severe (again, apart the trapping phenomenon already discussed)
2) The open channel stress bias point leads to a trap-formation in the gate-to drain access region (close to the drain contact) that causes large reversible charge trapping. Trap formation in the gate-to-drain access region, promoted by the simultaneous presence of high temperature and high current is the possible explanation.
3) The largest Id decrease and degradation are observed in devices stressed in Points B and E. The devices tested in those conditions are mainly affected by a reduction of the transconductance peak (g_{m_peak}), due to trap formation and charges trapped permanently in the gate-to-drain access region,. Some devices tested in E conditions actually show an increase of gate-lag dispersion effects.
4) The Id decrease observed in the devices stressed in the close channel conditions (points C, D and G) is mainly due to a degradation of the gate Schottky barrier demonstrated by a threshold voltage shift.

The degradation modes and mechanisms can be grouped according to the various bias points chosen for the accelerated tests:

- The open channel stress bias points (A, F) are characterised by a low I_{DS}, g_m and V_{TH} degradation, and by the occurrence of remarkable trapping effects which are reversible.
- Maximum degradation occurs at the bias points B and E. The major part of the degradation is permanent and due to possible trap formation and charge trapping at the gate edge towards the drain contact.
- Finally, the degradation observed in the devices stressed in close channel conditions (points C,D and G) is mainly related to a degradation of the gate Schottky barrier.

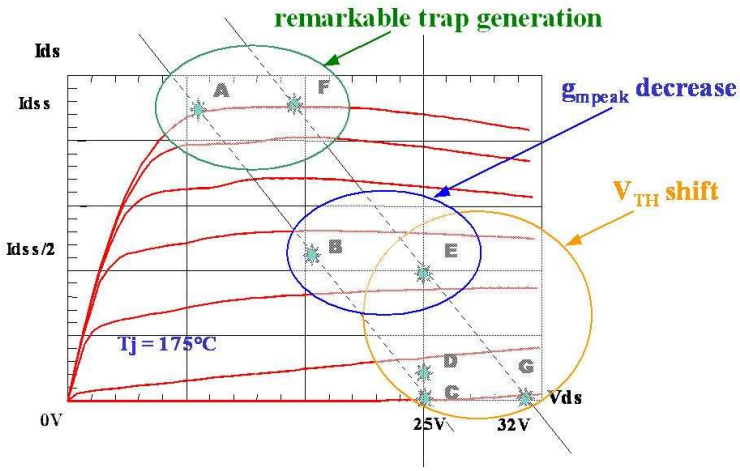


Figure 2.14 Sketch of the main degradation modes observed in devices stressed at the different bias points.

2.3 Short term DC stress on AMS04

Devices from wafer Selex AMS04 with L_G=0.5µm and W_G=200µm (gate without field-plate) have been tested at V_{DS}=20 V for different V_{GS} for 10 hours. These stress have induced a severe degradations on all tested transistors.
In "ON-state" (V_{DS}=20 V, V_{GS} = 0V) the drain current decrease varies from 17%, Figure 2.15, to 46%, the transconductance decrease in linear region reached 90%, Figure 2.16, and 25% in saturation region. Sub-threshold characteristics and sub-threshold slope were also affected, see Figure 2.18.

All devices tested in "ON-state" developed gate-lag transient effects to various extents, Figure 2.19 and a relatively moderate increase in gate forward and reverse current was observed only in 2 (out of 8) devices.

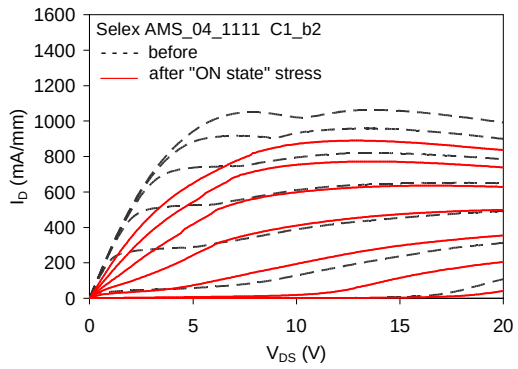


Figure 2.15: Drain current output characteristics of the AMS_04_1111 sample C1b2 before and after a 10 hours "ON-state" stress at V_{DS} = 20 V, V_{GS} = 0 V.

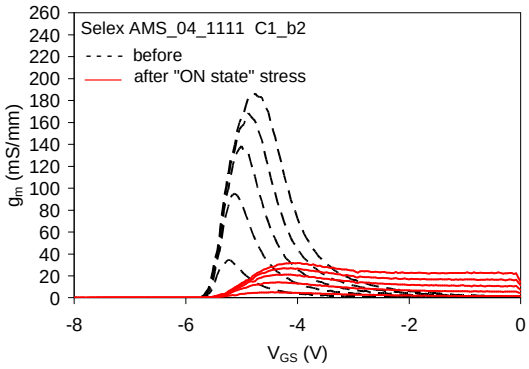


Figure 2.16: Transconductance g_m as a function of V_{GS} at increasing V_{DS} from 0.1 to 0.9 V of the AMS_04_1111 sample C1b2 before and after a 10 hours "ON-state" stress at V_{DS} = 20 V, V_{GS} = 0 V.

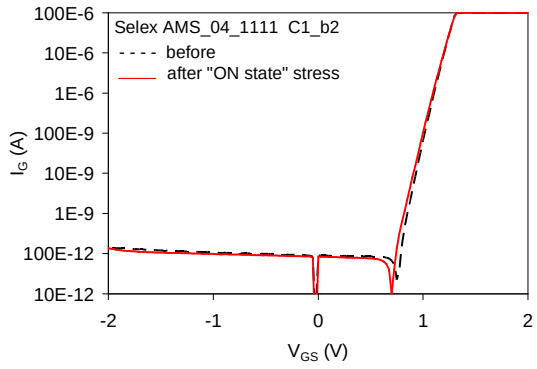


Figure 2.17: I-V characteristics of the gate-source Schottky diode of the AMS_04_1111 sample C1b2 before and after a 10 hours "ON-state" stress at V_{DS} = 20 V, V_{GS} = 0 V.

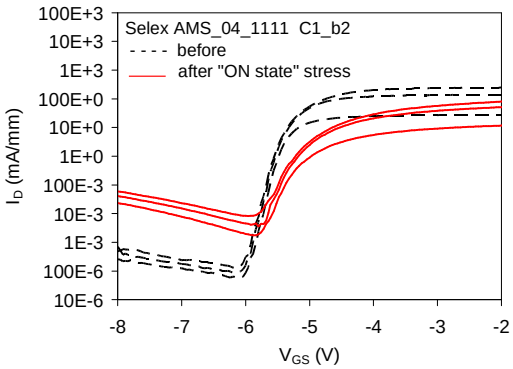


Figure 2.18: Sub-threshold drain current characteristics log(I_D) vs V_{GS} at increasing V_{DS} from 100 mV to 900 mV of the AMS_04_1111 sample C1b2 before and after a 10 hours "ON-state" stress at V_{DS} = 20 V, V_{GS} = 0 V.

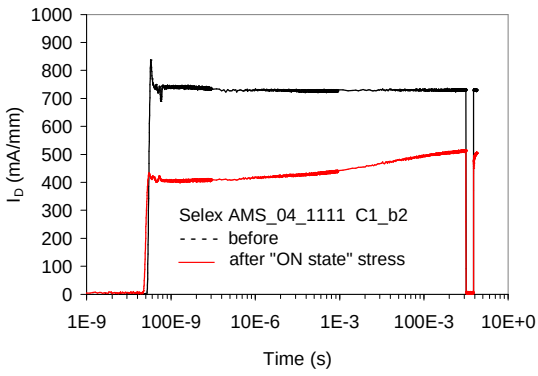


Figure 2.19: Drain current transient during a gate-lag experiment (V_{DD}=10 V, V_{GSoff} = - 9 V) of the AMS_04_1111 sample C1b2 before and after a 10 hours "ON-state" stress at V_{DS} = 20 V, V_{GS} = 0 V.

On the contrary, "SEMI-ON" tests caused a radical change in the I-V characteristics of the gate Schottky diode in all the tested devices, Figure 2.21. Transconductance dropped significantly, Figure 2.20. Rather surprisingly, no increase in gate-lag effects was found,

Figure 2.22.

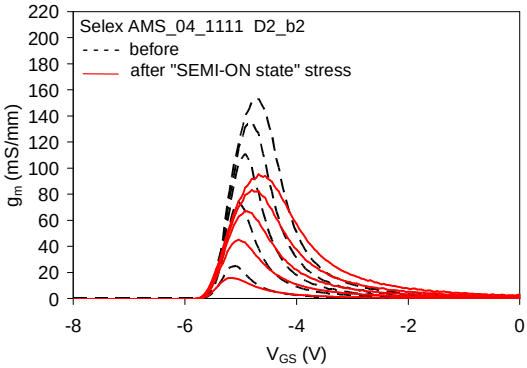


Figure 2.20: Transconductance g_m as a function of V_{GS} at increasing V_{DS} from 0.1 to 0.9 V of the AMS_04_1111 sample D2b2 before and after a 10 hours "SEMI-ON" stress at V_{DS} = 20 V, V_{GS} = -5.5 V.

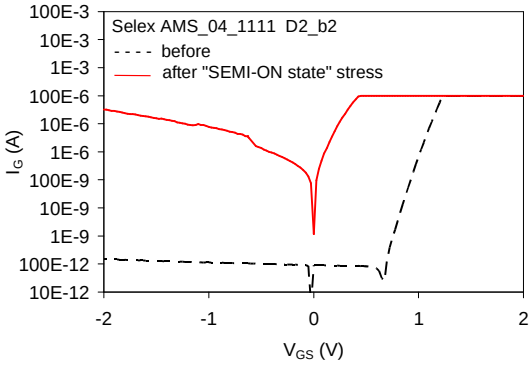


Figure 2.21: I-V characteristics of the gate-source Schottky diode of the AMS_04_1111 sample D2b2 before and after a 10 hours "SEMI-ON" stress at V_{DS} = 20 V, V_{GS} = -5.5 V.

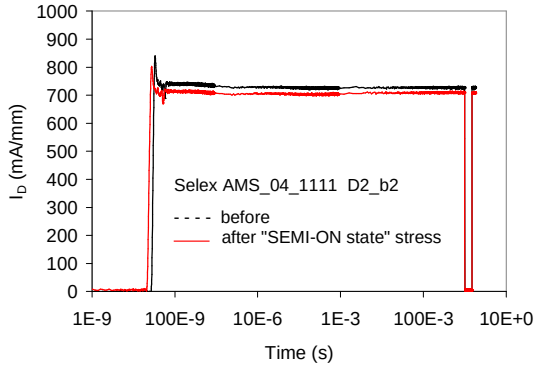


Figure 2.22: Drain current transient during a gate-lag experiment (V_{DD}=10 V, V_{GSoff} = - 9 V) of the AMS_04_1111 sample D2b2 before and after a 10 hours "SEMI-ON" stress at V_{DS} = 20 V, V_{GS} = -5.5 V.

Finally, "OFF-state" tests induced catastrophic changes in the gate I-V characteristics of all the tested devices, Figure 2.23. Transconductance decreases were observed in all devices. Only one device showed a remarkable increase in $|V_{TH}|$, Figure 2.24. The decrease in transconductance is sometimes accompanied by a slow drain current response, Figure 2.25 and Figure 2.26, but there is no

correlation between the two effects, since transconductance degradation is present also in devices completely free from gate-lag effects, Figure 2.27 and Figure 2.28.

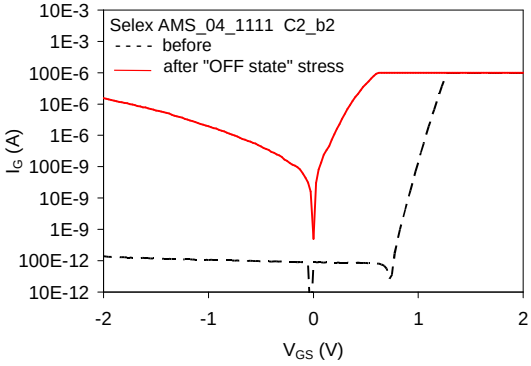


Figure 2.23: I-V characteristics of the gate-source Schottky diode of the AMS_04_1111 sample C2b2 before and after a 10 hours "OFF-state" stress at V_{DS} =20 V, V_{GS}=-7.5 V.

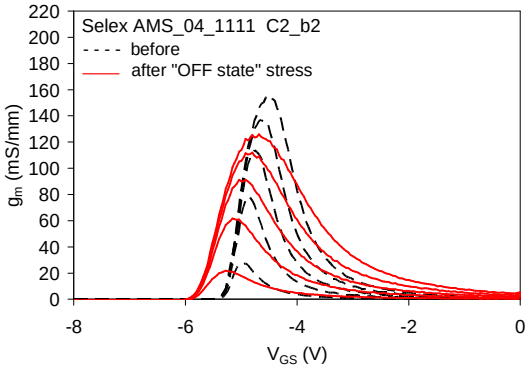


Figure 2.24: Transconductance g_m as a function of V_{GS} at increasing V_{DS} from 0.1 to 0.9 V of the AMS_04_1111 sample C2b2 before and after a 10 hours "OFF-state" stress at V_{DS} =20 V, V_{GS}=-7.5 V.

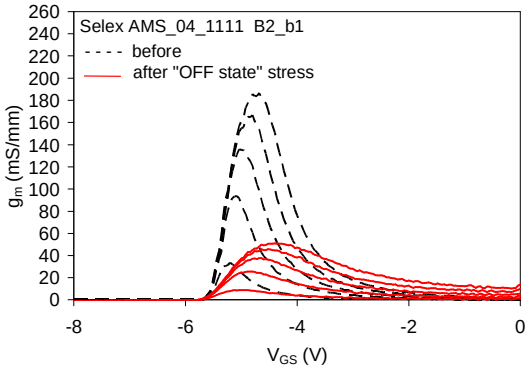


Figure 2.25: Transconductance g_m as a function of V_{GS} at increasing V_{DS} from 0.1 to 0.9 V of the AMS_04_1111 sample B2b1 before and after a 10 hours "OFF-state" stress at V_{DS} =20 V, V_{GS}=-7.5 V.

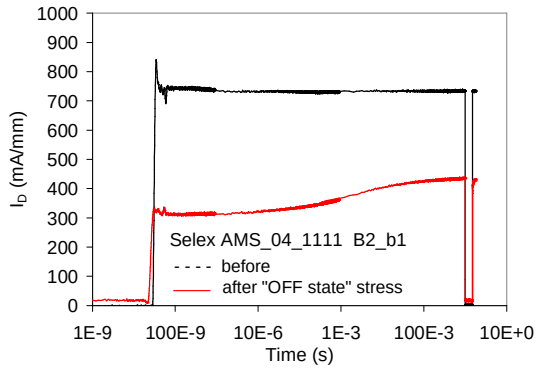


Figure 2.26: Drain current transient during a gate-lag experiment (V_{DD}=10 V, V_{GSoff} = - 9 V) of the AMS_04_1111 sample B2b1 before and after a 10 hours "OFF-state" stress at V_{DS} =20 V, V_{GS}=-7.5 V.

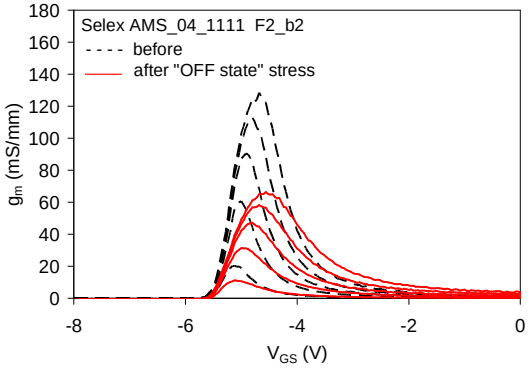


Figure 2.27: Transconductance g_m as a function of V_{GS} at increasing V_{DS} from 0.1 to

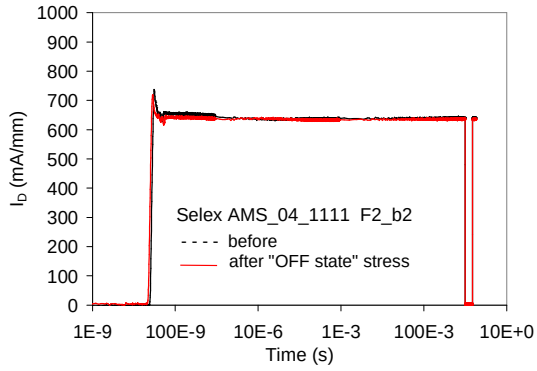


Figure 2.28: Drain current transient during a gate-lag experiment (V_{DD}=10 V, V_{GSoff} = - 9

0.9 V of the AMS_04_1111 sample F2b2 before and after a 10 hours "OFF-state" stress at V_{DS} =20 V, V_{GS}=-7.5 V.

V) of the AMS_04_1111 sample F2b2 before and after a 10 hours "OFF-state" stress at V_{DS} =20 V, V_{GS}=-7.5 V.

I_{DSS} degradation is more pronounced for the "ON-state" and "SEMI-ON" stress, Figure 2.29; $g_{m\text{-}peak}$ is more affected by "ON-state" stress, with an average decrease of more than 80% in 10 hours, Figure 2.30. $|V_{TH}|$ sharply increases during "ON-state" tests only, Figure 2.33. Finally, both "OFF-state" and "SEMI-ON" tests strongly increase the gate leakage current, with an increase in $I_{G\text{-}ON}$ of five order of magnitude and a x1000 increase in $I_{G\text{-}OFF}$, Figure 2.31 and Figure 2.32 respectively.

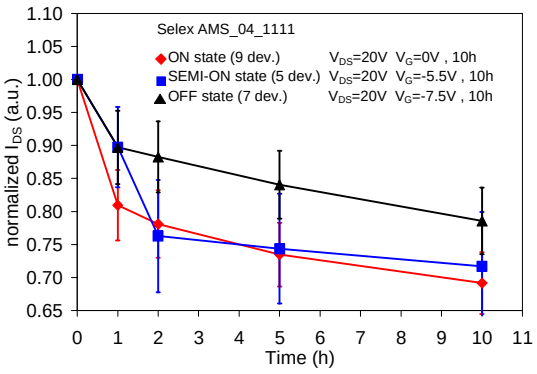


Figure 2.29: Graphics of I_{DSS} measured during "ON-state", "OFF-state" and "SEMI-ON state" stress. Error bars represent the related mean error.

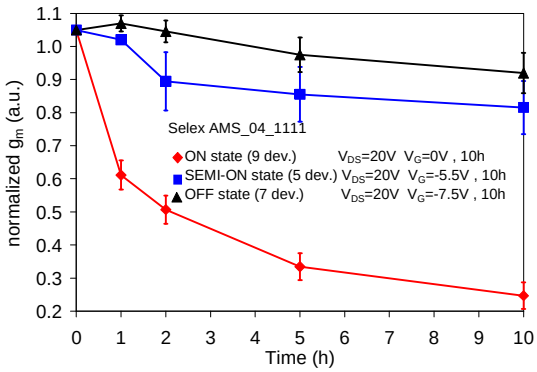


Figure 2.30: Graphics of g_{mpeak} measured during "ON-state", "OFF-state" and "SEMI-ON state" stress. Error bars represent the related mean error.

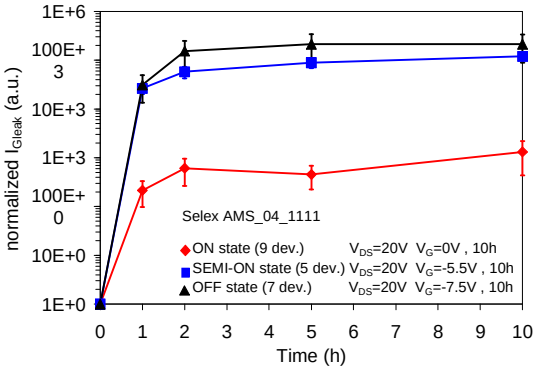


Figure 2.31: Graphics of $I_{Gleak\text{-}on}$, measured during "ON-state", "OFF-state" and "SEMI-ON state" stress. Error bars represent the related mean error.

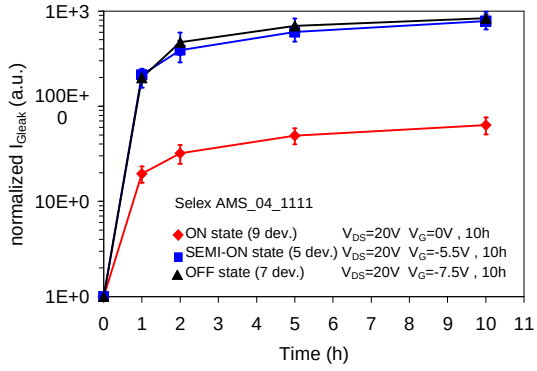


Figure 2.32: Graphics of $I_{Gleak\text{-}off}$ measured during "ON-state", "OFF-state" and "SEMI-ON state" stress. Error bars represent the related mean error.

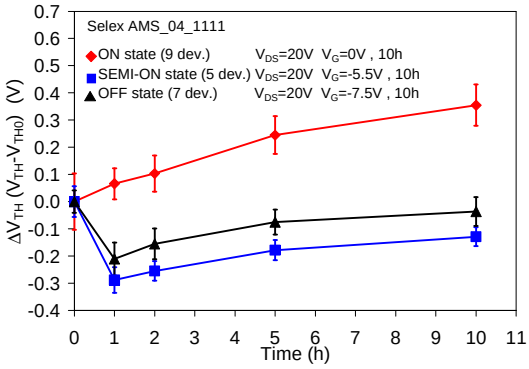


Figure 2.33: Graphics of ΔV_{TH} measured during "ON-state", "OFF-state" and "SEMI-ON state" stress. Error bars represent the related mean error; $\Delta V_{TH}=(V_{TH}-V_{TH0})$, therefore a positive increase means that the threshold voltage shift towards more positive values.

During "ON-state" tests of AMS04 devices, threshold voltage shifts (decreasing $|V_{TH}|$) are observed, to various extent, in all tested devices. This failure mode can not be due to surface effect, but should involve the device volume under the gate; it is not due to changes in the barrier height of the gate Schottky diode, since the I-V characteristics of that diode remain unchanged or suggest a decrease in barrier height, rather than a decrease. Negative charge trapping at the AlGaN/GaN interface, or within the AlGaN, or in the buffer itself may be responsible for this failure mode. Trapping would in this case take place at new deep levels, since generation of defects or traps seems to be involved, as shown by the increase of gate-lag effects in degraded devices, see Figure 2.19: Drain current transient during a gate-lag experiment (V_{DD}=10 V, V_{GSoff} = - 9 V) of the AMS_04_1111 sample C1b2 before and after a 10 hours "ON-state" stress at V_{DS} = 20 V, V_{GS} = 0 V.

The dominant failure mode consequent to "SEMI-ON" and "OFF-state" tests was the decrease in the maximum of transconductance, see Figure 2.24 and Figure 2.25. Threshold voltage is generally unchanged with a slight tendency to $|V_{TH}|$ increase in "OFF-state" samples. Development of drain current transient effects during gate-lag experiments is frequently observed, but is not always directly correlated with the I_{DSS} and g_m decrease. This failure mode suggests an increase in parasitic series resistances in the HEMT structure, consequent to negative charge accumulation in the gate-to-drain access region over or below the device channel. At the same time, generation of new deep levels may be involved, as demonstrated by gate-lag experiments, Figure 2.26, possibly consequent to hot-electron injection, or strain relaxation of the AlGaN layer (consequent to piezo-electric effects related with electric field, maximum during "OFF-state" tests). I_{DSS} and g_m degradation is faster during "SEMI-ON" accelerated tests; however, it is almost impossible to distinguish between the two mechanisms (or to rule out the presence of alternative mechanisms) in consequence of the reduced number of tested samples available. One should be aware, for instance, that testing in "OFF-state" conditions at high V_{DS} (> 20 V) often induces carrier injection at hot spots or preferential breakdown

points, which then become a source of high energetic carriers, thus explaining the early degradation.

2.4 Conclusion

For ACE1148 devices we can draw the following considerations: Point B and E are the most stressful conditions, followed by points in the close channel conditions (C, D and G) and those in open channel conditions. Open channel stress bias point leads to a trap-formation in the gate-to drain access region (close to the drain contact) that causes large reversible charge trapping. The degradation modes and mechanisms can be grouped according to the various bias points chosen for the accelerated tests: the open channel stress bias points (A, F) are characterised by a low I_{DS}, g_m and V_{TH} degradation, and by the occurrence of remarkable trapping effects which are reversible; maximum degradation occurs at the bias points B and E. The major part of the degradation is permanent and due to possible trap formation and charge trapping at the gate edge towards the drain contact. The degradation observed in the devices stressed in close channel conditions (points C,D and G) is mainly related to a degradation of the gate Schottky barrier.

In AMS04 the main degradation mechanisms in the "ON-state" stress are drain current and transconductance decrease and threshold voltage shifts, this phenomea can not be due to surface effect, but should involve the device volume under the gate. The dominant failure mode consequent to "SEMI-ON " and "OFF-state" tests was the decrease in the maximum of transconductance, whereas the threshold voltage is generally unchanged. Development of drain current transient effects during gate-lag experiments is frequently observed, but is not always directly correlated with the I_{DSS} and g_m decrease.

2.5 References

[1] Y.F. Wu et al., Electron Devices Meeting, 2006.

[2] S. Nakajima et al., Proc. WOCSDICE 2007;

[3] E. L.Piner, Proc. WOCSDICE 2007;

[4] G. Meneghesso et al., IEEE Trans. El. Dev. 53 (12) 2932, 2006;

[5] R. Coffie et al., IEEE Proc. Int. Rel. Phys . Symp. 2007, p. 568; [6] J. Joh, J. del Alamo, " IEEE IEDM TEch. Digest 2006.

3.Thermal Storage

3.1 Introduction

Great efforts are being dedicated to understand long-term degradation effects and failure mechanisms to improve GaN HEMT device reliability [1]. Device aging may enhance trapping effects by generating new defects through several physical mechanisms [2], [3], and [4]. Trapping phenomena may induce the current-collapse effect [5], which consists in a decrease of drain current measured in pulsed conditions with respect to the DC value. The current collapse related to surface traps can be solved by adopting suitable surface passivations [6, 7]. The long-term passivation reliability has became a really important issue.

In the following pages a detailed characterization of GaN/AlGaN/GaN HEMT grown on SiC and Sapphire submitted to 2,000 hours test at 300 °C without bias is presented. After thermal storage, devices belonging to SiC wafers present a dramatic enhancement of the current collapse effect due to surface trapping. The current collapse is not evident when the devices are measured in DC conditions. The observed degradation mode has been attributed to a passivation delamination with a consequent generation of surface traps. This reliability problem has been solved by adopting an adequate modification of the passivation_technology. The

effects of the thermal storage on the devices belonging to the Sapphire wafer were studied in relation of the form of the gate. Mainly no difference has been found for I-gate or Γ-gate with two different field-plate lengths.

3.2 Device description

SLX19 has been grown by MBE on a 2-inch SiC substrate. A 1.7 μm GaN buffer layer has been grown on this substrate followed by an AlGaN barrier (21 nm) and a GaN cap (1 nm) layer. GaN HEMT fabrication has been completed by Ohmic contact (Ti/Al/Ni/Au) and Schottky gate electrode formation (Ni/Au) on the semiconductor surface. The gate electrode fabrication has been optimized to provide both high rf gain and high breakdown voltage, through the Field-plate effect provided by the "Γ" shape section of the gate metallization, having a footprint length of L_G = 0.25 μm and a 0.2 μm head overhang toward the drain contact [8]. Devices have been passivated with 400 nm SiN deposition on the wafer surface, by using Plasma Enhanced Chemical Vapor Deposition (PECVD). Total SiN 400 nm thickness has been deposited in different phases: one 70 nm thick layer before Gate definition, further 80 nm before Ti/Pt/Au metallization and the rest before thick Au layer definition.

SLX25 has been grown by MOCVD on a 2-inch SiC substrate, the contact definition and the passivation deposition were the same as SLX19. This wafer presents a 1.9 μm Fe doped GaN buffer and an AlGaN barrier of 25 nm.

SLX15 has been grown by MOCVD on a 2-inch Sapphire substrate, the gate were fabricated using Stepper I-Gate technology for L_G=0.5μm and EBL Γ-Gate technology for L_G=0.25μm, two different lengths of drain overhang (field plate) for Γ-Gate are present: L_{FP}=0.2μm and L_{FP}=0.4μm. Devices have been passivated with 400 nm SiN deposition as SLX19 and SLX25. This wafer presents a 1.2 μm GaN buffer and an AlGaN barrier of 26 nm with Al fraction of 0.26.

The characteristics of the three tested wafers are summarized in Tab 1. The wafers were cut in several parts: for each wafer one was submitted to the thermal storage, whereas another part was kept untreated for reference. The devices were characterized with different techniques before and after the storage. First of all, a complete DC electrical characterization has been carried out using an HP 4142 parameter analyzer under dark-light condition.

		SLX19	SLX25	SLX15
Passivation	**material** **thickness/type** **thickness/type** **total thick.**	SiN 150nm/type "A 250nm/type"B" 400 nm	SiN 150nm/type "A 250nm/type"B" 400 nm	SiN 150nm/type "A 250nm/type"B" 400 nm
Gan (cap)		1 nm	no	no
AlGaN	**thickness** **Si-doped** **Al %**	21 nm no 23%	25 nm no 28%	26 nm no 26%
GaN	**thickness** **Fe**	1700 nm no	1900 nm yes	1200 nm no
Epi supplyer		Picogiga	QinetiQ	QinetiQ
Substrate		SiC (Norstel)	SiC (Norstel)	Sapphire
Gate	L_G **gate** L_{FP}	0.25 Γ 0.2	0.25 Γ 0.2	0.5, 0.25 Γ and I 0.2, 0.4

Tab 1 : Wafer structure for the wafers submitted to thermal storage stress

Trapping effects and current collapse phenomena , that strongly impact on the reliability of HEMT devices [9], have been characterized either by means of a DIVA-like double-pulser setup (controlling voltage pulses applied to both the gate and to the drain, i.e. allowing one to pulse the devices starting from an arbitrary V_{GS}, V_{DS} baseline) and by a "gate-single-pulser" setup where the gate is pulsed while the drain is connected through a drain resistance to the supply voltage V_{DD}.

When the devices where measured by means of the double-pulser setup two baseline bias conditions (V_{GBL},V_{DBL}) have been adopted:

(i), (V_{GBL},V_{DBL}) = (0 V, 0 V) - This is considered the reference baseline, since this bias condition do not induce charge trapping during the biasing itself, and hence no current collapse is observed on the I-V curves;

(ii) (V_{GBL},V_{DBL}) = (-8 V, 20 V) – This is considered the most critical bias point for charge trapping, since the negative gate bias and at the same time high drain voltage highly enhance the charge injection.

When the "gate-single-pulser" setup was adopted, the V_{DD} was fixed at 20 V and the gate was pulsed from -8 V to 0 V, reproducing a situation very closed to the (ii) (V_{GBL},V_{DBL}) = (-8 V, 20 V) of the Diva-like measurements.

For wafer SLX19 we have also adopted a 100 ns Transmission Line Pulser (TLP-TDR) measurement [10], in order to study the breakdown behaviour of the transistors at high voltage and high current regimes limiting the self heating effects as much as possible.

3.3 DC measurements

For SLX19 wafer the complete DC characterization performed before and after the thermal storage (2,000 hours, 300 °C) shows a moderate degradation of the main parameters all over the wafer of the devices after the storage. Over fifty devices of the thermally treated wafer portion, and about twenty of the untreated part were measured. The mean value of the drain current measured either in linear (V_{DS} = 2 V) or in saturation region (V_{DS} = 10 V) shows a decrease of about the 20 % (see Figure 3.1 as an example of the output characteristics), whereas the mean value of the transconductance peak measured in linear region (V_{DS} = 0.1 – 1 V) is reduced by 25 %, see Figure 3.2. Gate leakage current decreases fairly (not shown), and the threshold voltage seems to be unaffected by the storage, as can be seen in Figure 3.2.

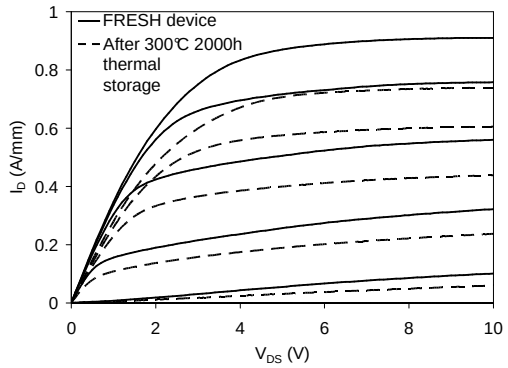


Figure 3.1 Typical output DC characteristics before and after the thermal storage for V_{GS} from -6 V to 0 V, step 1 V for SLX19 wafer

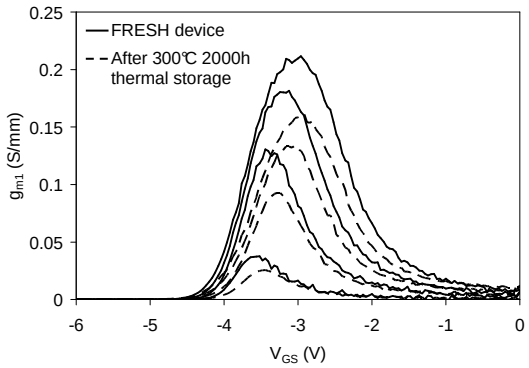


Figure 3.2 Typical transconductance before and after the thermal storage for V_{DS} from 0.1 V to 1 V step 0.3 for SLX19 wafer

Differently from what observed in the SLX19, in the SLX25 wafer the significant decrease of the drain current devices channel resistances, associated to a significant shift of the threshold voltages to positive values suggests that the observed problem is not related exclusively to the processing technology (virtually the same for both the wafers) but to the material properties (coming from two different epitaxial sources) and/or the combination of the fabrication with the substrate. Wafer SLX15 presents a moderate degradation of DC parameters and no threshold voltage shift. The gate current leakage decrease present in all wafers can be associated to a stabilization of the Metal-Semiconductor Schottky junction induced by the thermal storage. This suggests that an additional thermal treatment after the gate metal deposition could improve the stabilization of the device

characteristics. DC characteristics for all tested wafers are summarized in figures from Figure 3.3 to Figure 3.8, for a better readability the data are normalized to the value before the storage.

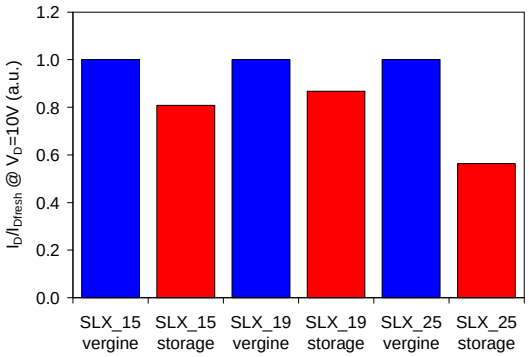


Figure 3.3 Normalized drain current at V_{DS}=10V for fresh and stressed devices on SLX15,SLX19 and SLX25

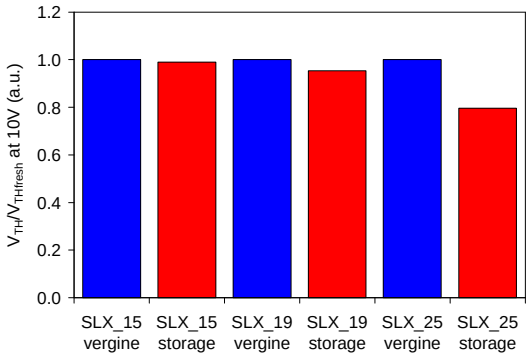


Figure 3.4 Normalized threshold voltage at V_{DS}=10V for fresh and stressed devices on SLX15,SLX19 and SLX25

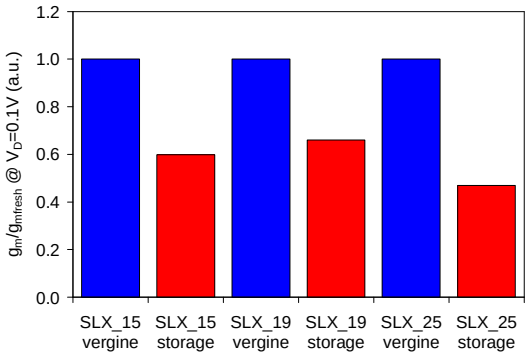


Figure 3.5 Normalized transconductance at V_{DS}=0.1V for fresh and stressed devices on SLX15,SLX19 and SLX25

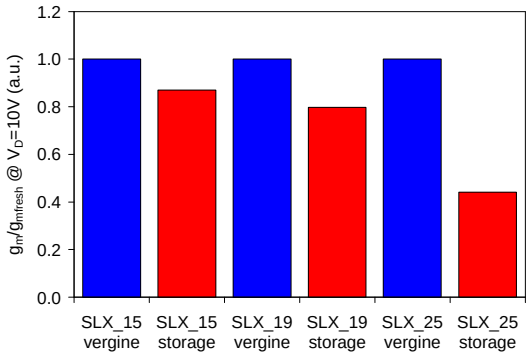


Figure 3.6 Normalized transconductance at V_{DS}=10V for fresh and stressed devices on SLX15,SLX19 and SLX25

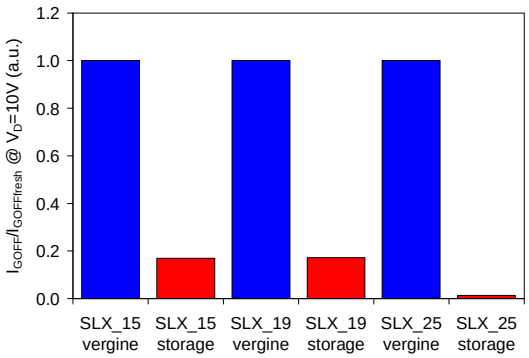


Figure 3.7 Normalized leakage current at V_{DS}=10V, V_{GS}=-Vp for fresh and stressed devices on SLX15,SLX19 and SLX25

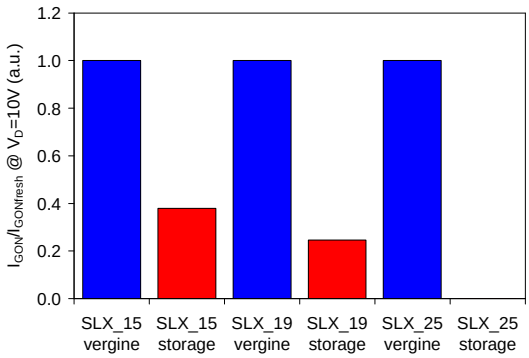


Figure 3.8 Normalized leakage current at V_{DS}=10V, V_{GS}=0V for fresh and stressed devices on SLX15,SLX19 and SLX25

The differences between different gate topology devices on SLX15 wafer after the thermal storage shows that the different technologies have a comparable reliability (see figures from Figure 3.9 to Figure 3.14) excluding the gate leakage current.

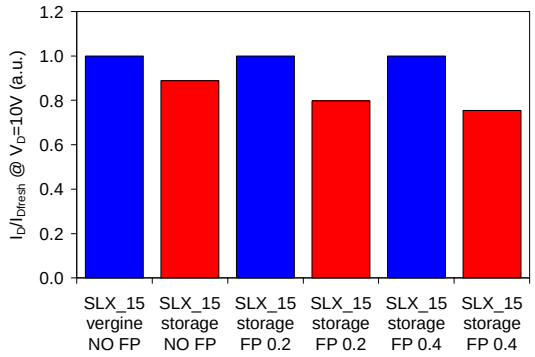


Figure 3.9 Normalized drain current at V_{DS}=10V for fresh and stressed devices without and with different L_{FP}

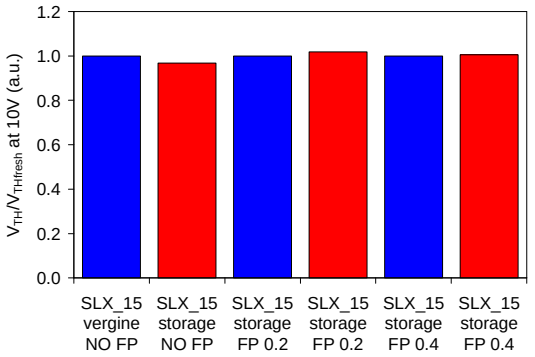


Figure 3.10 Normalized threshold voltage at V_{DS}=10V for fresh and stressed devices without and with different L_{FP}

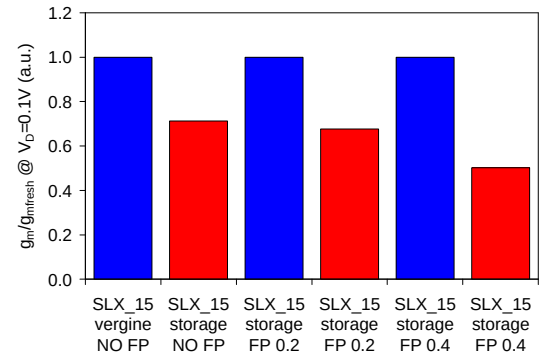


Figure 3.11 Normalized transconductance at V_{DS}=0.1V for fresh and stressed devices without and with different L_{FP}

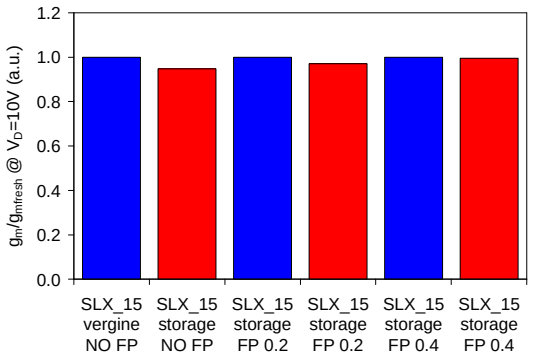


Figure 3.12 Normalized transconductance at V_{DS}=10V for fresh and stressed devices without and with different L_{FP}

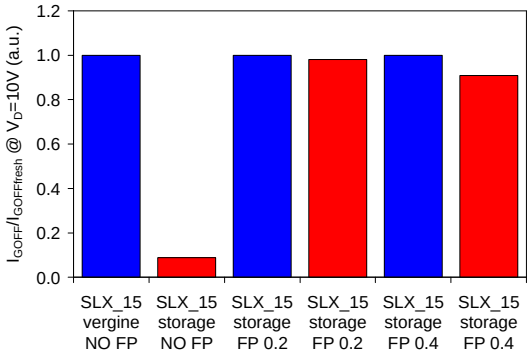


Figure 3.13 Normalized leakage current at V_{DS}=10V, V_{GS}=-Vp for fresh and stressed

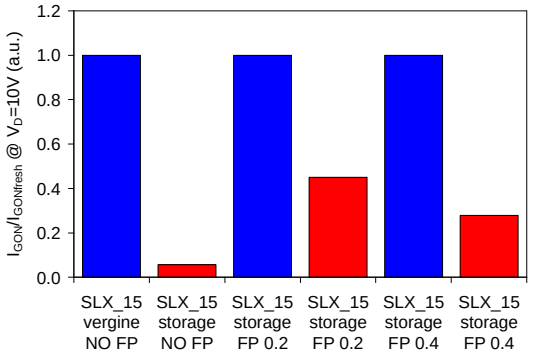


Figure 3.14 Normalized leakage current at V_{DS}=10V, V_{GS}=0V for fresh and stressed

devices without and with different L_{FP}

devices without and with different L_{FP}

The IG current in the I-gate structure seems to decrease more than in the other structures, see Figure 3.13 and Figure 3.14.

3.4 Double-Pulse measurements

The slump ratio (S.R.), measured through DIVA-like measurements, defined as the ratio between the IDSS measured at V_G = 0 V and V_D = 10 V of curves with the baseline (-V_P, 20 V) and those with the baseline (0 V, 0 V), is recognized in literature as a good indicator of trapping phenomena [11], [12]: the higher the S.R. value (with 1 as the maximum value) the lower the trapping phenomena. For SLX19 the S.R. measurement highlights a strong difference between fresh and thermally treated device as it can be seen in Figure 3.15 and Figure 3.16. Clearly, the curves corresponding to the (0 V, 0 V) baseline condition (black diamonds in Figure 3.15 and Figure 3.16) are not affected by trapping effects either in fresh or treated device, i.e. the transistor reaches the same value of drain current before and after the stress. The situation is completely different when the measurements are carried out with (-8 V, 20 V) baseline condition (open squares). Regarding fresh devices, only a slight current collapse is observed, leading to a S.R. value of about 0.8, whereas stressed devices show strong trapping phenomena (see open square in Figure 3.16), leading to a S.R. value lower than 0.1.

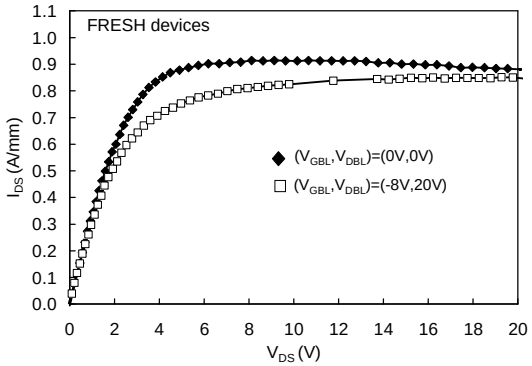


Figure 3.15 Typical DIVA-like I_D - V_D measurement for a fresh device for two different base-line, namely (0 V, 0 V) and (-8 V, 20 V) for SLX19 wafer

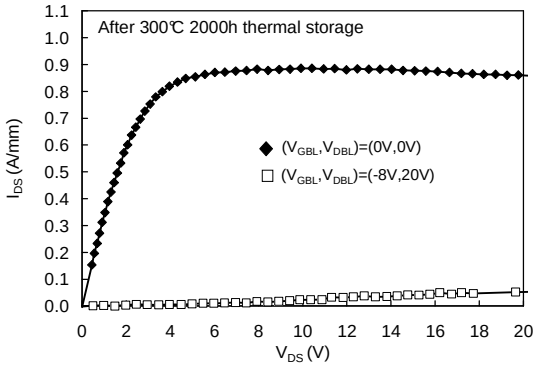


Figure 3.16 Typical DIVA-like I_D - V_D measurement for a storage device for two different base-line, namely (0 V, 0 V) and (-8 V, 20 V) for SLX19 wafer

The DIVA-like drain current (I_D) curves as a function of the gate voltage (V_{GS}) measured in untreated and treated devices are presented in Figure 3.17 and Figure 3.18 respectively. In Figure 3.18 we compare the curve at baseline (0 V, 0 V), with the one at baseline (-8 V, 20 V), the latter being magnified by a factor of ten.
Again, we can observe a large collapse on the devices after storage when measured with the (-8 V, 20 V) baseline.

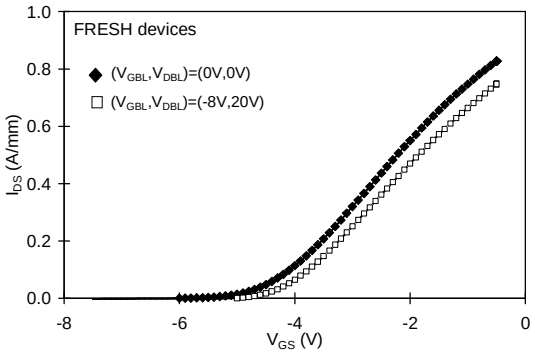


Figure 3.17 DIVA-like I_D - V_G measurement for a fresh device for two different base-line, namely (0V, 0V) and (-8V, 20V) for SLX19 wafer

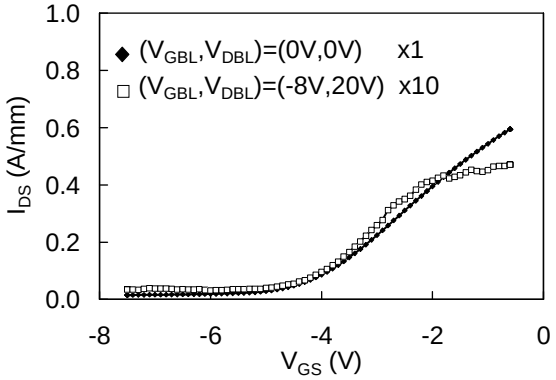


Figure 3.18 DIVA-like I_D - V_G measurement for a storage device for two different base-line, namely (0 V, 0 V) and (-8 V, 20 V) for SLX19 wafer. The baseline (-8 V, 20 V) is magnified by ten times

From this comparison, it is possible to notice that the current collapse in SLX19 is not due to a threshold voltage shift, but only to a decrease of the transconductance peak. This result suggests that the current collapse is correlated with an increase of the series resistance possibly induced by surface trapping.

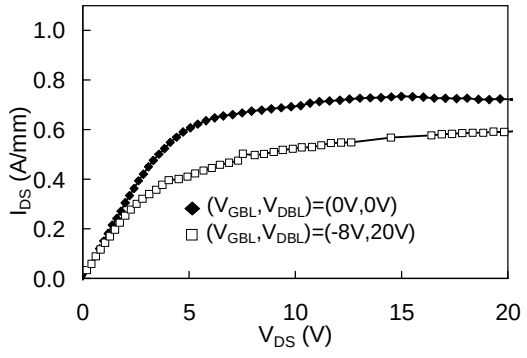


Figure 3.19 Typical DIVA-like I_D - V_D measurement for a fresh device for two different base-line, namely (0 V, 0 V) and (-8 V, 20 V) for SLX25 wafer

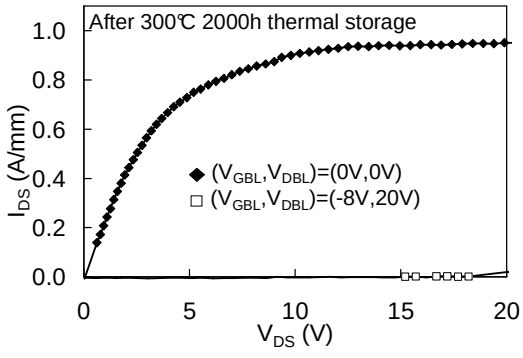


Figure 3.20 Typical DIVA-like I_D - V_D measurement for a storage device for two different base-line, namely (0 V, 0 V) and (-8 V, 20 V) for SLX25 wafer

For SLX25 wafer the current collapse before the stress was 0.75 whereas after the thermal storage is nearly zero (see Figure 3.19 and Figure 3.20). In these devices, on the contrary of SLX19, a strong threshold voltage shift of about 2V after the thermal storage is present, as can be seen from Figure 3.21 and Figure 3.22.

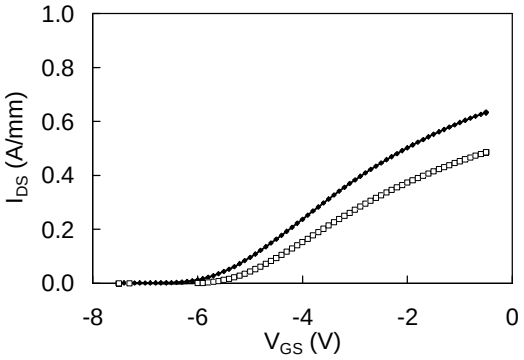


Figure 3.21 DIVA-like I_D - V_G measurement for a fresh device for two different base-line, namely (0V, 0V) and (-8V, 20V) for SLX25 wafer

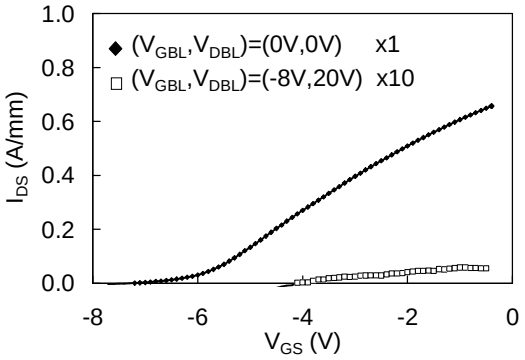


Figure 3.22 DIVA-like I_D - V_G measurement for a storage device for two different base-line, namely (0 V, 0 V) and (-8 V, 20 V) for SLX25 wafer. The baseline (-8 V, 20 V) is magnified by ten times

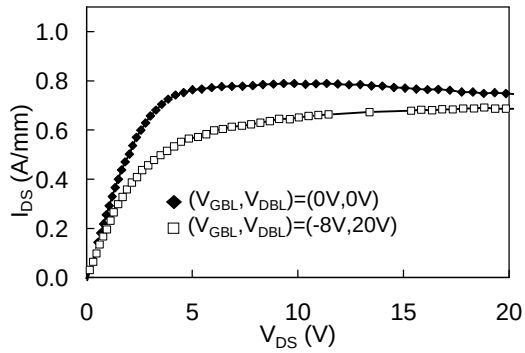


Figure 3.23 Typical DIVA-like I_D - V_D measurement for a fresh device for two different base-line, namely (0 V, 0 V) and (-8 V, 20 V) for a SLX15 device with L_{FP}=0.2um

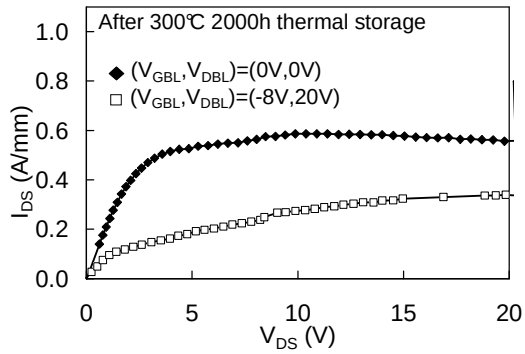


Figure 3.24 Typical DIVA-like I_D - V_D measurement for a storage device for two different base-line, namely (0 V, 0 V) and (-8 V, 20 V) for a SLX15 device with L_{FP}=0.2um

Figure 3.25 summarize the S.R. for the three fresh wafers and the three wafers submitted to the thermal storage.

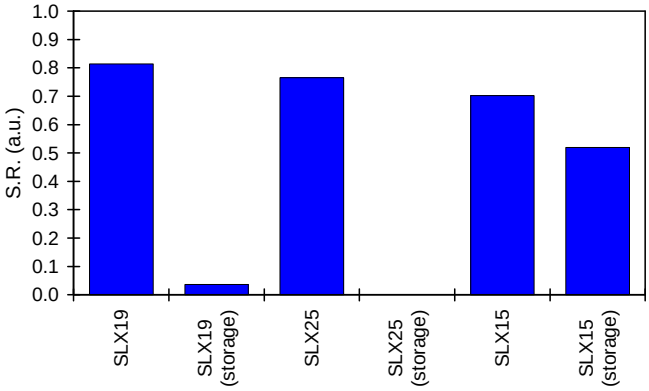


Figure 3.25 S.R. for the three fresh wafers and the three wafers submitted to the thermal storage

3.5 Breakdown characterization for SLX19

Breakdown measurements, by means of the TLP tester, have been carried out on fresh and treated devices, in order to study the effect of the high temperature storage stress on the device breakdown properties. Figure 8 shows the breakdown characteristics of devices with three different gate width (100 μm, 300 μm, and 2400 μm) before and after the thermal storage at 300 °C. TLP curves of Figure 3.26 were obtained keeping the gate and drain voltage constant to 0 V (similar to the a quiescent bias point (0 V, 0 V) of the DIVA-like setup) and then pulsing the drain to the final value. It can be seen that no trapping effects, and no difference between treated or untreated devices (for all the gate width) are evident, in good agreement with the DIVA-like measurements (see Figure 3.15 and Figure 3.16with the (0 V,0 V) baseline). We have also carried out breakdown measurements varying the gate voltage (starting from V_{GS} = -5 V, up to V_{GS} = 0 V), see Figure 3.27, on a device after the thermal storage with a gate width of 1200 μm.

As it can be seen, a breakdown voltage value of about 150 V is present in OFF-State condition (V_{GS} = -5 V) while this value decreases to about 100 V in ON-state condition (V_{GS} = 0 V). This result addresses that the breakdown condition is not driven by the electric field (that is higher in OFF-state condition).

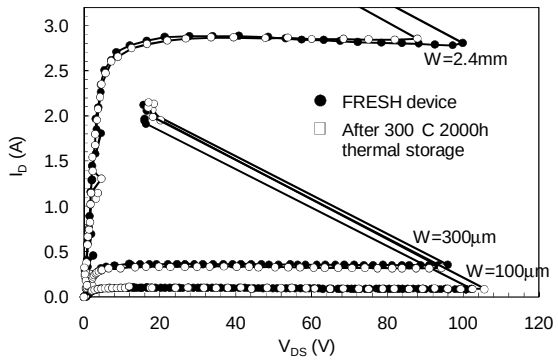


Figure 3.26 TLP measurements for both fresh and thermal treated devices. The pulse is applied between drain and source, with gate grounded

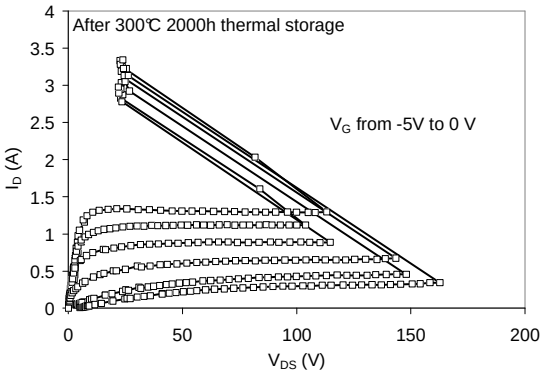


Figure 3.27 TLP measurements for thermally treated devices with W = 1200 □m for V_{GS} from -5 V to 0 V

From this result one could consider that the breakdown condition is reached by the combination of high current density (leading to a high power dissipation), and the high electric field between gate and drain. However, another possible interpretation could be that the breakdown voltage increases when the gate is more negative biased because the charge trapping is present. In fact, when the gate is negatively biased, charge trapping in the access regions is strongly enhanced leading to a large reduction of the electric field and hence to the breakdown walkout effect.

3.6 Failure mechanism

Pulsed measurements have highlighted a strong enhancement of trapping effects, suggesting that the damage could be located at the device surface. We suppose that these superficial traps are neutral if the devices are kept at (V_{DBL}, V_{GBL}) = (0 V, 0 V) in both DIVA-like and TLP measurements. On the contrary, under (V_{GBL}, V_{DBL}) = (-8 V, 20 V) bias condition, a large amount of charge is trapped on the surface, and this dramatically affects transistor performances, with a heavy decrease of the GaN HEMT current. It is believed that traps are only located at the surface access region, since no threshold voltage shift was observed in the collapsed devices.

In order to obtain some physical degradation mechanisms, we have carried out an optical inspection. Thanks to this we have noticed the presence of a severe passivation damages, in the wafer portion submitted to the thermal storage. All over the wafer submitted to the storage, cracks and loss of adhesion were

observed. Figure 3.28 and Figure 3.29 show these cracks near the active region of transistors.

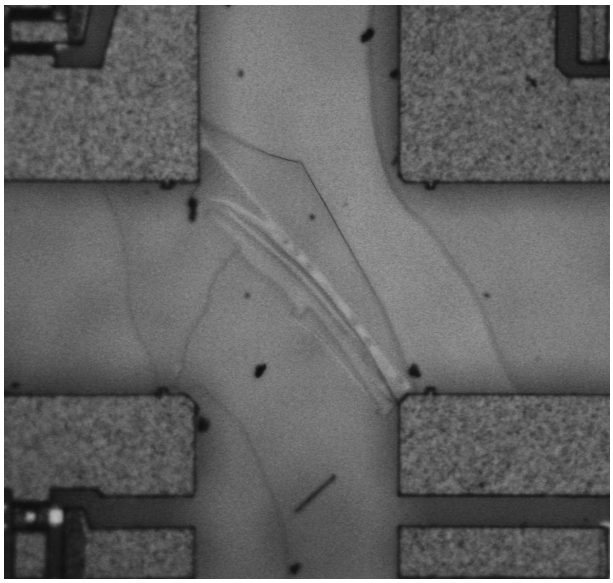


Figure 3.28 Photo of passivation layer damage in the wafer area between four different devices

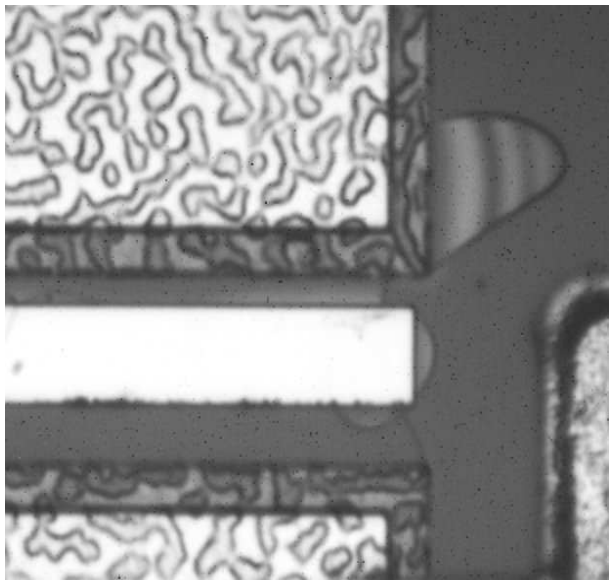


Figure 3.29 Photo of passivation layer damage in a HEMT device without air-bridge structure

3.7 Solution

In order to solve this problem, different passivation processes have been studied, and an in situ NH_3/N_2 mixture (1:50) surface plasma exposure before passivation deposition has then been identified as the best cleaning procedure solution to improve its adhesion. A new wafer has then been processed by using the identical epitaxial structure of the previous one, and thin film processing adding plasma clean procedure before each SiN deposition was used to fix the observed issues. Up to now, a 500 hours thermal storage at 300 °C has been carried out, and no degradation neither on DC nor on rf performances have been identified, see Figure 3.30.

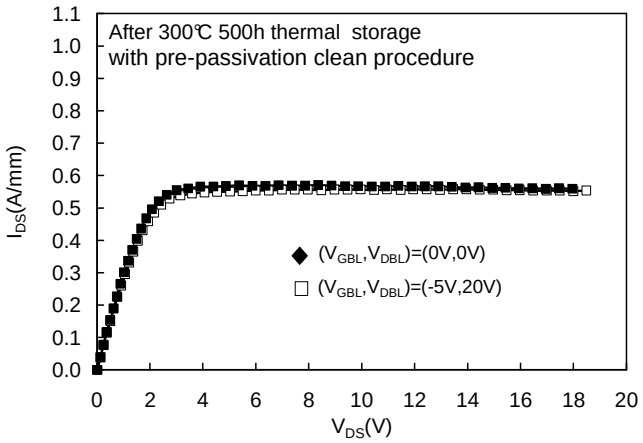


Figure 3.30 DIVA measurement for a device with pre-passivation clean procedure for two different baseline values, namely (0 V, 0 V) and (-5 V, 20 V)

3.8 Conclusion

We have identified a new failure mechanism on GaN HEMTs, observed after long thermal storage tests at high temperature (300 °C). DC measurements have shown a slight degradation of the devices current value, no threshold voltage shift, but a severe degradation was identified in pulsed and low-frequency measurements. The main failure mode was an enhancement of trapping effects that took place on the device surface access regions, more precisely at the interface between the AlGaN layer and the SiN passivation.

Failure analysis demonstrated that a loss of adhesion of the passivating layers was responsible for the observed trap reactivation. An improved passivation deposition process was then developed, including a surface cleaning procedure aimed to preventing passivation detaching. Devices fabricated using this new procedure have not shown any enhancement of trapping effects up to 500 hours of stress at 300°C.

3.9 References

[1] U. K. Mishra, et al., "AlGan/Gan HEMTs – An overview of device operation and applications", Proc. IEEE, v. 90, n. 6, June 2002.

[2] G. Meneghesso, et al., "Hot-electron-stress degradation in unpassivated GaN/AlGaN/GaN HEMTS on SiC, Proc. IRPS, pp. 415-422, April 2005.
[3] A. Sozza, et al., "Evidence of Traps Creation in GaN/AlGaN/GaN HEMTs After a 3000 Hour On-state and Off-state Hot-electron Stress", IEDM, December 2005.
[4] J. Joh, et al., "Mechanisms for Electrical Degradation of GaN High-Electron Mobility Transistors", IEDM, December 2006.
[5] G. Meneghesso, et al., "Surface-related drain–current dispersion effects in AlGaN-GaN HEMTs", IEEE Trans. Electron Devices, vol. 51, no. 10, pp. 1554–1561, Oct. 2004.
[6] S. Arulkumaran, et al., "Current collapse-free i-GaN/AlGaN/GaN high-electron-mobility transistors with and without surface passivation", Applied Physics Letter, vol.85 no. 23, December 2004.
[7] V. Tilak, et al., "Effect of Passivation on AlGaN/GaN HEMT device performance", ISCS, pp.357-363, October 2000.
[8] P. Romanini, et al., "Very High Performance GaN HEMT devices by Optimized Buffer and Field Plate Technology", European Microwave Integrated Circuits Conference, Manchester (UK) 10-13 Sept. 2006.
[9] G. Meneghesso, et al., "Current Collapse and High-Electric-Field Reliability of Unpassivated GaN/AlGaN/GaN HEMTs", IEEE Transaction on Electron Devices, issue 12, Dec. 2006, pp. 2932-2941.
[10] A. Amerasekera, et al., "ESD in Silicon Integrated Circuits", 2nd Edition, Chichester, England: John Wiley and Sons, 2002.
[11] G. Meneghesso et al., IEEE Trans. on Electron Devices, Vol. 51, No. 10, pp. 1554-1561, October 2004.
[12] G. Verzellesi, et al., Microelectronics Reliability, Vol. 45, pp. 1585-1592, 2005.
[13] A. Tazzoli, et al., "ESD Robustness of AlGaN/GaN HEMT Devices", Proc. of 29th Electrical Overstress/Electrostatic Discharge Symposium Proc., EOS/ESD 2007, pp. 264-272, Anaheim, California, USA, September 16-20, 2007.

4.Reverse bias step stress

4.1 Introduction

Degradation induced by high electric field can significantly affect the reliability of GaN-based HEMT's [1-5]. One of the key issue is the correlation of substrate and epitaxial material quality with GaN HEMT failure mechanisms, and the identification of the role of intrinsic (hot electrons, reverse piezoelectric effect) and extrinsic (defects-related) mechanisms in determining time to failure.

In several works are described failure modes which cannot be explained with hot electron-induced degradation, at least if only channel electrons are considered. Since significant changes in device electrical parameters and increase in transient effects have been observed after OFF-state accelerated tests with negligible channel current, many authors have proposed the existence of a failure mechanism accelerated by the electric field only, resulting in charge trapping and traps creation. A specific hypothesis has been recently formulated by Joh and del Alamo [4], [5]; according to the proposed mechanism, the electric field in the gate-drain region would increase the strain in the AlGaN/GaN heterojunction resulting in strain relaxation and crystallographic defect formation. The inverse piezoelectric effect

and the preexisting strain of the AlGaN/GaN structure certainly have a negative influence on device reliability. Other mechanisms may contribute to compromise the reliability of GaN devices biased in OFF-state at very high drain-gate voltages: 1) Electrons, injected from the gate electrode into the GaN due to trap assisted tunneling, can reach very high energies, damage the semiconductor surface and interfaces and induce traps [7]; 2) as the electric field is increased, vertical breakdown of the AlGaN layer can occur creating a damaged path between the gate and the GaN. EL microscopy can be very useful in detecting localized breakdown effects and evaluating degradation mechanisms in OFF-state.

In this chapter we present the results of an experiment carried out on HEMT test structures, which were submitted to a reverse-bias step stress up to -100 V. We show clear evidence of a dependence of reverse bias degradation on material quality, together with the first observation of breakdown walkout effects in GaN HEMTs.

4.2 Measurements

A set of AlGaN/GaN HEMT wafers was manufactured using a common fabrication process and device layout, and similar epitaxial structures were studied. Different suppliers for substrate and epitaxial layers were adopted, in order to compare the influence of material quality on device degradation (see Table 4.1 **Tested wafers with Selex processing.**and Table 4.2).

Wafer		SLX14	SLX15	SLX19	SLX34	SLX39	SLX46	SLX57	SLX0P
Gan cap		no	no	1 nm	no	no	yes		1 nm
AlGaN	thickness	25 nm	26 nm	21 nm	22 nm	25 nm	22 nm		20 nm
	Al %	23%	26%	23%	26%	28%	28%		23%
GaN	thickness	2000 nm	1200 nm	1700 nm	1500 nm	1900 nm			2000 nm
	Fe	no	no	no	no	yes			yes
Epi supplyer		Lecce	QinetiQ	Picogiga	Tiger	QinetiQ	Picogiga	Lecce	Cree
Substrate		Sapphire	Sapphire	SiC	SiC	SiC	SiC	SiC	SiC
Substrate supplier		Commercial	Commercial	Norstel	Cree	Cree	Cree	Norstel	Cree

Table 4.1 Tested wafers with Selex processing.

Wafer		Tinkerbell	Peterpan	Beast	AEC1303
Gan cap		no	no	no	no
AlGaN	thickness	28	28 nm	27 nm	22 nm
	Al %	25%	25%	30%	27%
GaN	thickness				1500 nm
	Fe	yes	yes	no	no
Epi supplyer		QinetiQ	QinetiQ	Tiger	Tiger
Substrate		SiC	SiC	SiC	SiC
Substrate supplier		Norstel	Cree	Cree	Cree

Table 4.2 Tested wafers with QinetiQ and TRT (only AEC1303) processing.

Eight different HEMT structures with Selex processing, three with QinetiQ processing and one with TRT processing have been tested; wafers epitaxial structures are described in Table 4.1 **Tested wafers with Selex processing.**and Table 4.2. All layers were grown by MOCVD, with the exception of SLX19 and SLX46, who adopted MBE; the AlGaN layer was undoped for all suppliers.

For devices in Table 4.1 (Selex processing) GaN HEMT fabrication has been completed by ohmic contact formation trough Ti/Al/Ni/Au deposition and subsequent rapid thermal processing, Schottky gate electrode formation using Ni/Au deposition, active device isolation by Fluorine ion implantation. Devices have been passivated with 400 nm SiN, deposited by Plasma Enhanced Chemical Vapor Deposition.

For devices in Table 4.2. (QinetiQ processing) Ti/Al/Pt/Au ohmic contact and Ni/Au Schottky gate electrode have been deposited. Devices have been passivated with SiN/SiO_2/SiN, deposited by PECVD. For TRT processing (see Table 4.2.wafer AEC1303) ohmic contact are made of Ti/Al/Ni/Au, Schottky of Mo/Au and the passivation is composed of SiO_2 and SiN.

Test structures having L_G = 5 μm, LDS = 15 μm, W =100μm were submitted to a reverse bias step stress test, keeping source and drain grounded and applying a negative bias to the gate, from -15 V to – 50 V in -5 V steps (120 s each); and then from -50 V to -100 V in -5 V steps. At the end of each step, device electrical characteristics and EL images of the devices were measured.

Reverse bias testing induces an increase in I_G which is correlated with the appearance of "hot spots" in the EL micrographs obtained by reverse biasing the gate Schottky junction with source and drain grounded. This behaviour was common to all wafers, but the increase took place at different reverse bias voltages for the various wafers. Double-pulse gate-lag measurements were carried out, and an increase in the current slump (demonstrating an increase in trap density) was verified. Despite the large increase in Ig, degradation of ID and gm is less than 10% and occurs gradually for all devices.

In the following pages the correlation between I_G and emission spots presence (emission measured each time at V_G=-10V, V_S=V_D=0V) during the stress are presented. First results to be presented are for Selex processing.

SLX14

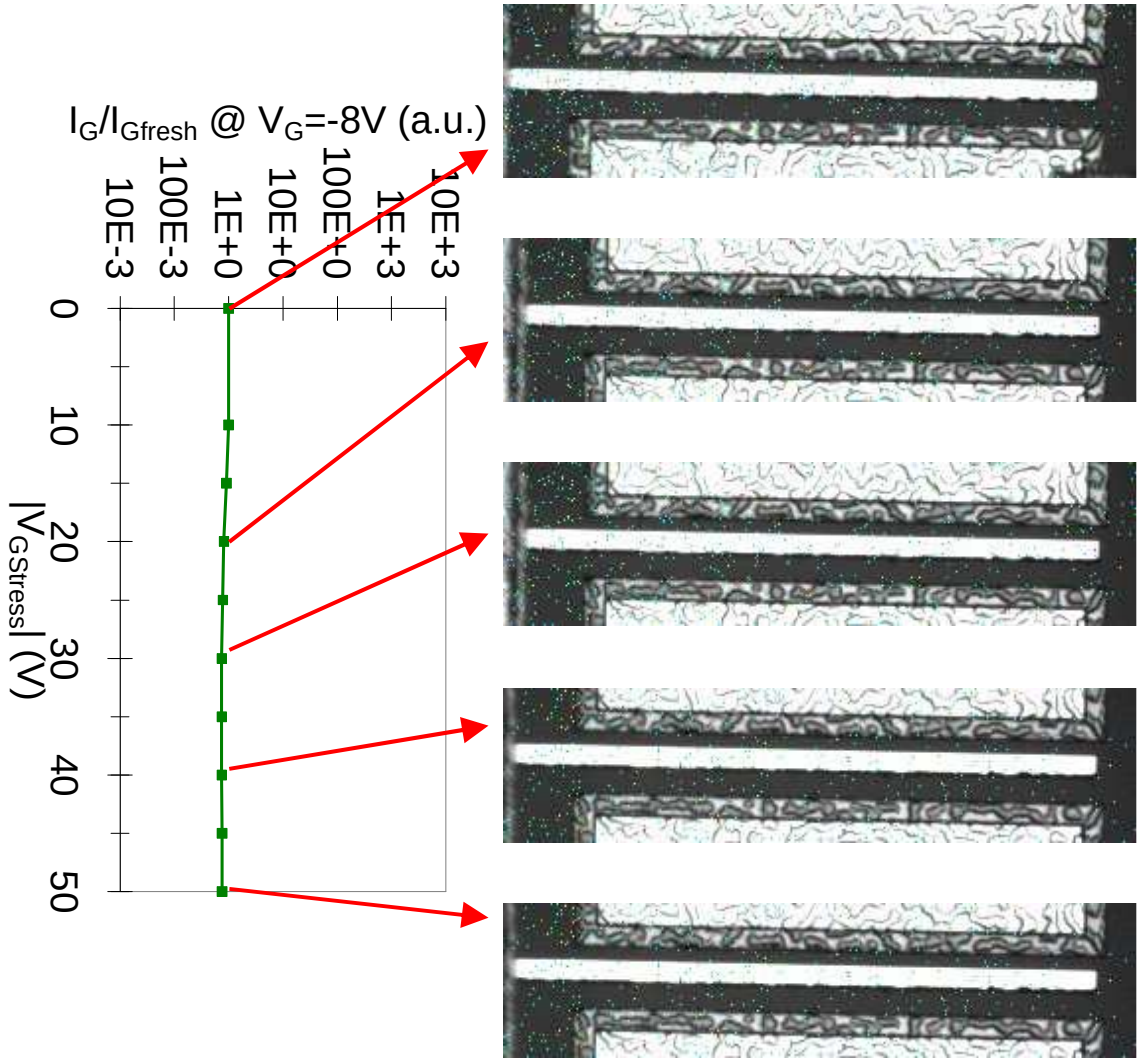


Figure 4.1 On the left Gate current VS Gate voltage bias during the stress. On the right emission images at different step of the stress.

SLX14 wafer show no increase of the Gate leakage current and no emission spots in the emission images. As can be seen from Figure 4.9 to Figure 4.18 Drain current and transconductance peak slightly decrease; the Source resistance increase at $V_{Gstress}$ = -30V.

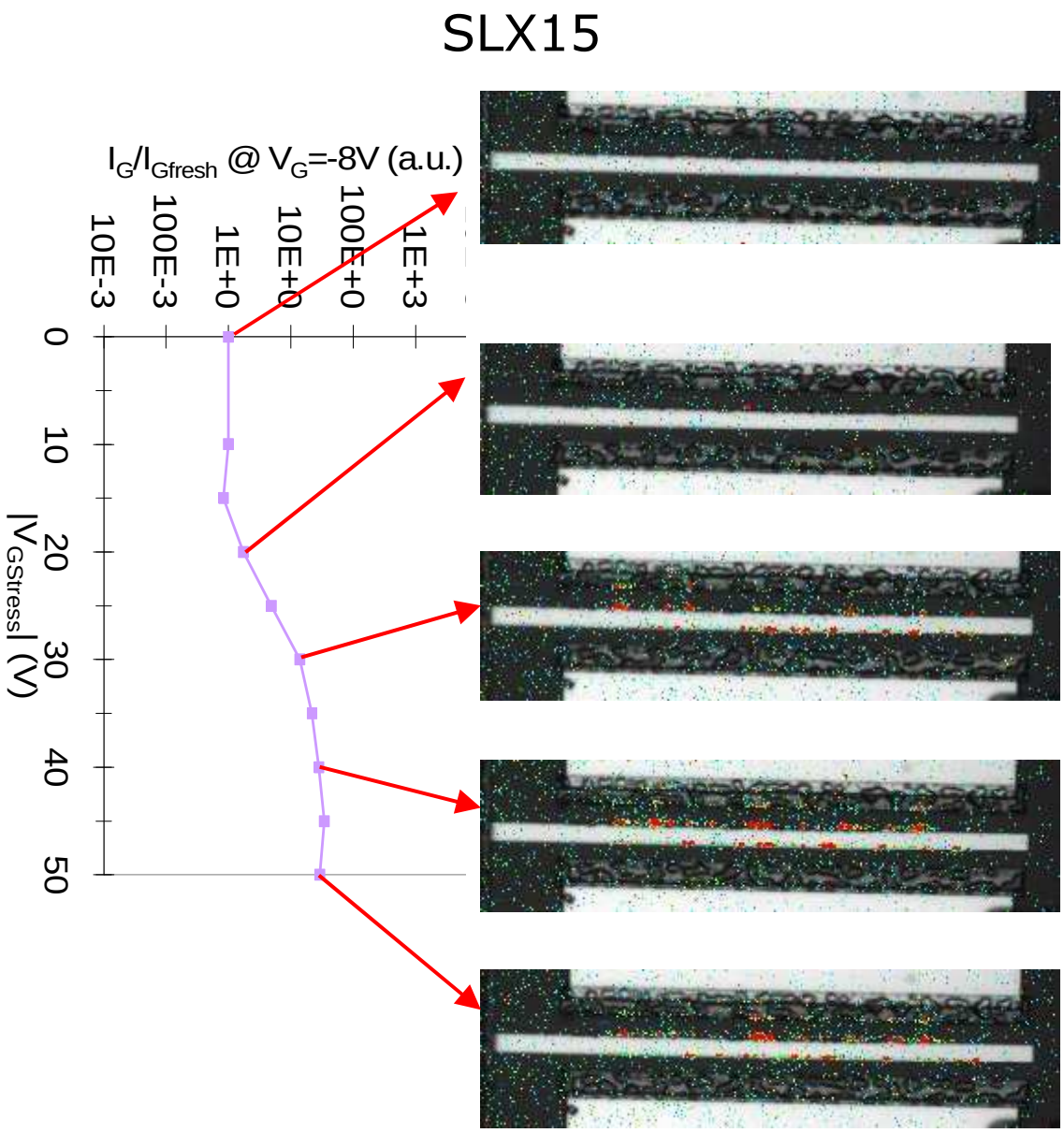


Figure 4.2 On the left Gate current VS Gate voltage bias during the stress. On the right emission images at different step of the stress.

SLX15 wafer show an increase of the Gate leakage current of more than one order of magnitude, emission spots appears in the emission images as the leakage current increases. The threshold for this device is $V_{Gstress}$ = -20V, in fact after 120s at $V_{Gstress}$ = -20V a tiny spot appears, after $V_{Gstress}$ = -35V Gate current becames constant and no more degradation in the emission image is found. As can be seen from Figure 4.9 to Figure 4.18 Drain current and transconductance decrease very slightly during the stress; Drain and Source resistance increase after the $V_{Gstress}$ = -20V step of stress.

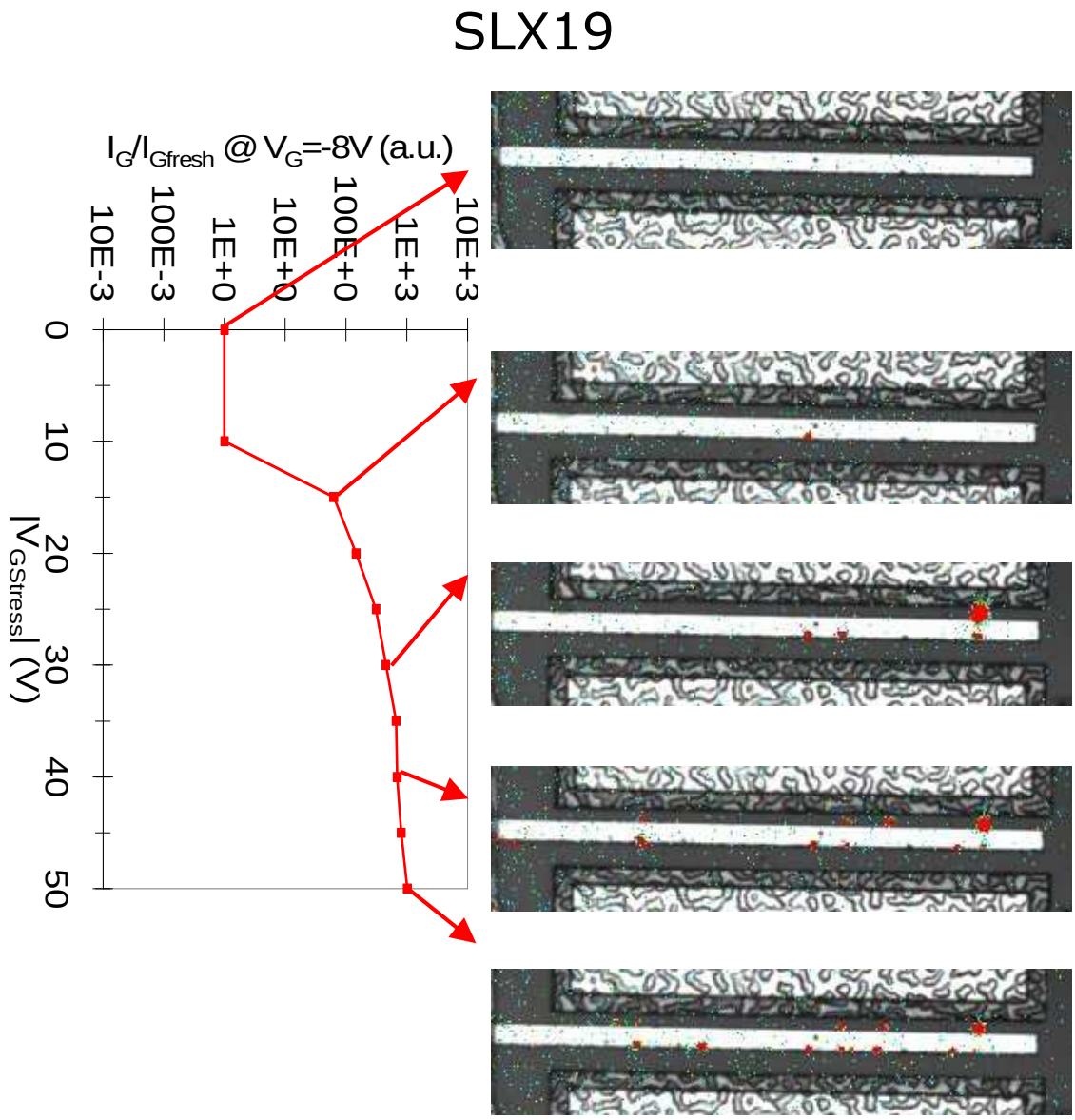


Figure 4.3 On the left Gate current VS Gate voltage bias during the stress. On the right emission images at different step of the stress.

SLX19 wafer show a strong increase of the Gate leakage current and emission spots appears as the leakage current increases.. The device presents a sudden I_G degradation (the threshold for this device is $V_{Gstress}$ = -15V) that increase during the stress: I_G at the end of the stress is three order of magnitude in respect to the IG of the fresh device. As can be seen from Figure 4.9 to Figure 4.18 Drain current and transconductance decrease very slightly during the stress; Drain resistance increase but at the end decrease whereas Source resistance is strongly increased.

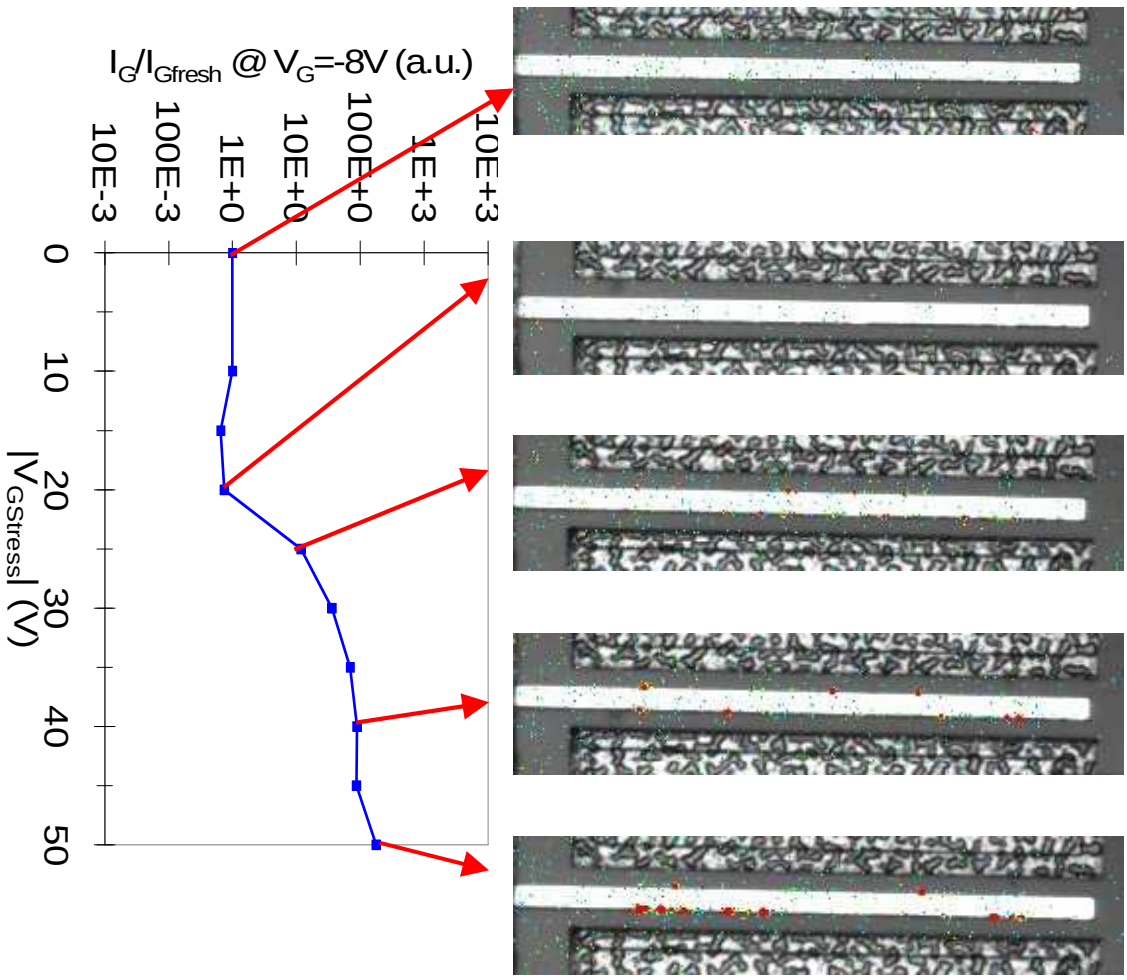


Figure 4.4 On the left Gate current VS Gate voltage bias during the stress. On the right emission images at different step of the stress.

SLX34 wafer show an increase of the Gate leakage current of two order of magnitude, emission spots appears in the emission images as the leakage current increases. The threshold for this device is $V_{Gstress}$ = -25V as can be seen comparing the emission after $V_{Gstress}$ = -20V and the one of the following step. From Figure 4.9 to Figure 4.18 Drain current, transconductance and Drain and Source resistance do not show any changes during the stress.

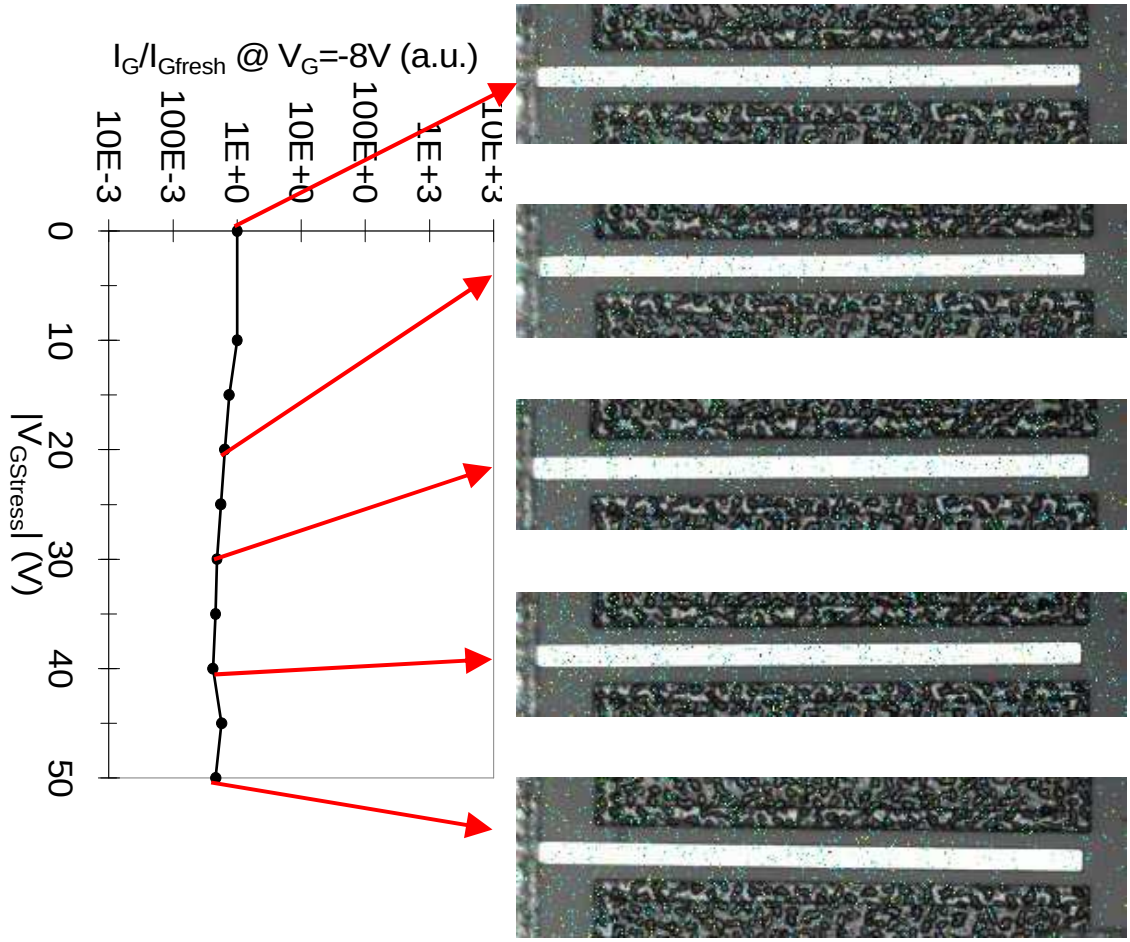


Figure 4.5 On the left Gate current VS Gate voltage bias during the stress. On the right emission images at different step of the stress.

SLX39 wafer show a slight decrease of the Gate leakage current and no emission spots appears. As can be seen from Figure 4.9 to Figure 4.18 Drain current and transconductance have little decrease and increase; Drain resistance increase whereas Source resistance is quite constant.

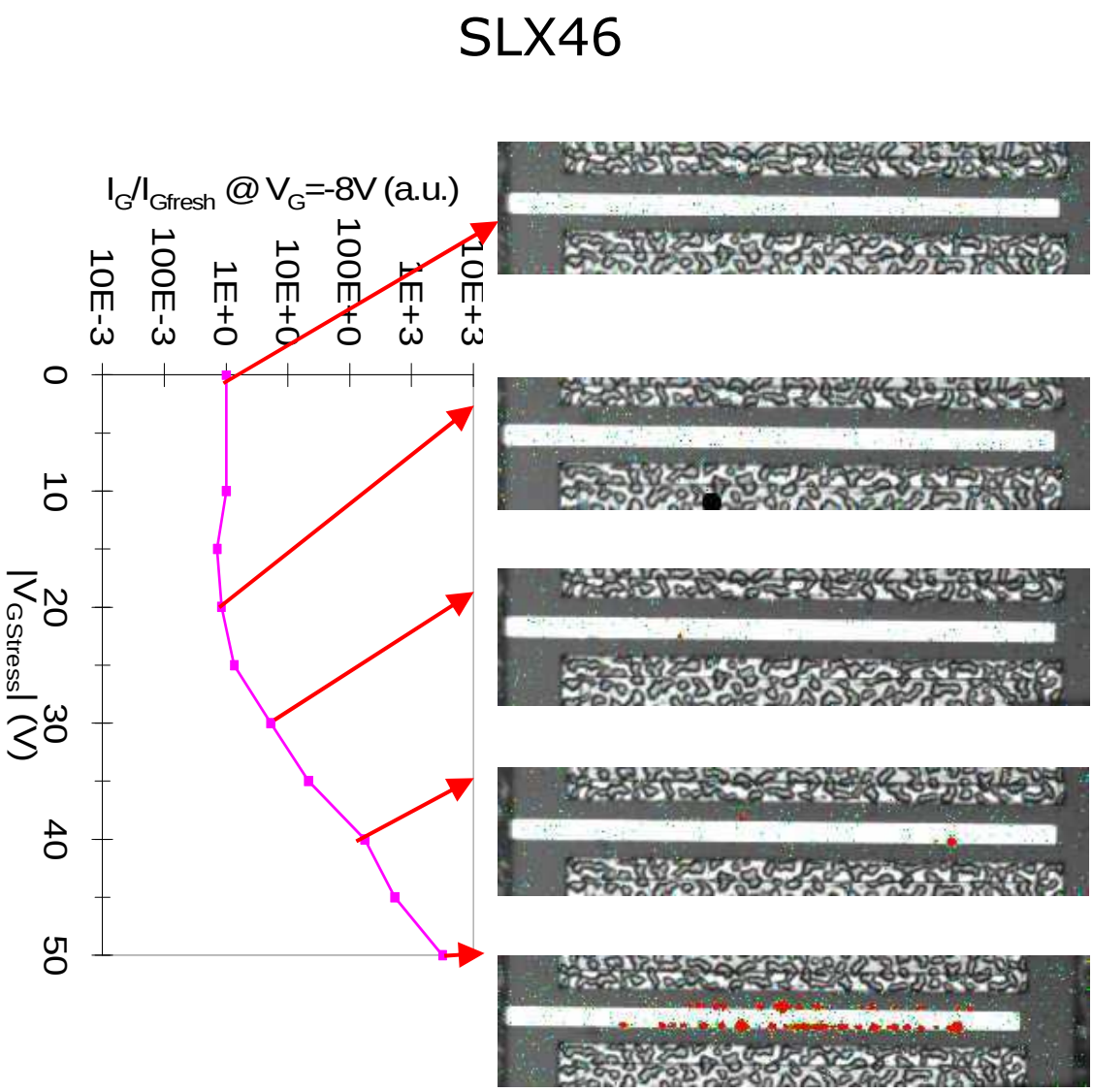


Figure 4.6 On the left Gate current VS Gate voltage bias during the stress. On the right emission images at different step of the stress.

SLX46 wafer show the strongest increase of the Gate leakage current in all Selex wafers. Emission spots clearly appears as the leakage current increases. The device presents a "soft" and not sudden I_G degradation (the threshold for this device is $V_{Gstress}$ = -35V); at the end of the stress I_G is four order of magnitude in respect to the I_G of the fresh device. As can be seen from Figure 4.9 to Figure 4.18 Drain current and transconductance increase during the stress; Drain resistance strongly decrease whereas Source resistance is increases.

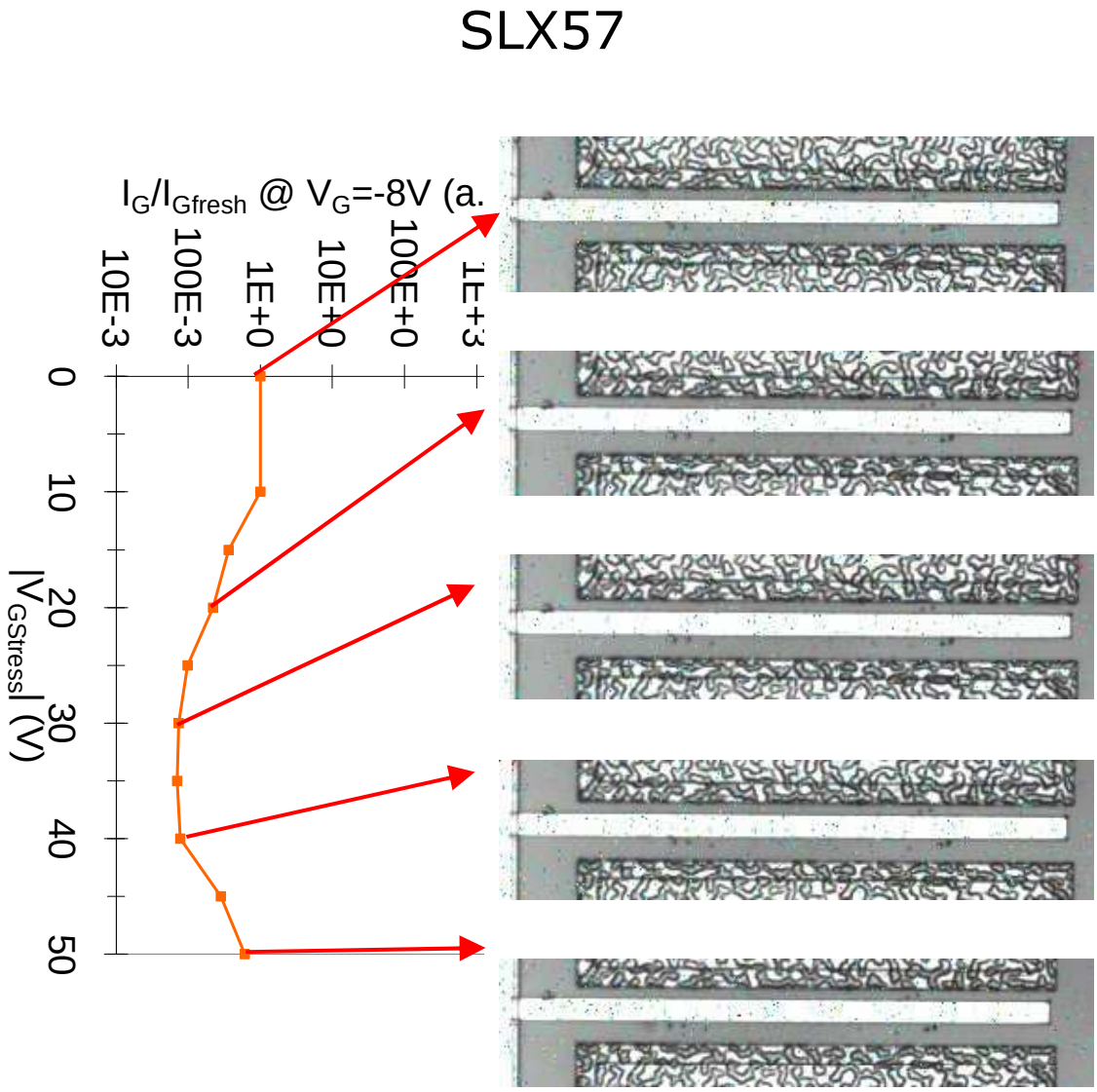


Figure 4.7 On the left Gate current VS Gate voltage bias during the stress. On the right emission images at different step of the stress.

SLX57 wafer show a slight decrease of the Gate leakage current up to $V_{Gstress}$ = -40V and no emission spots appears. As can be seen from Figure 4.9 to Figure 4.18 Drain current and transconductance have little increase; Drain and Source resistance are quite constant.

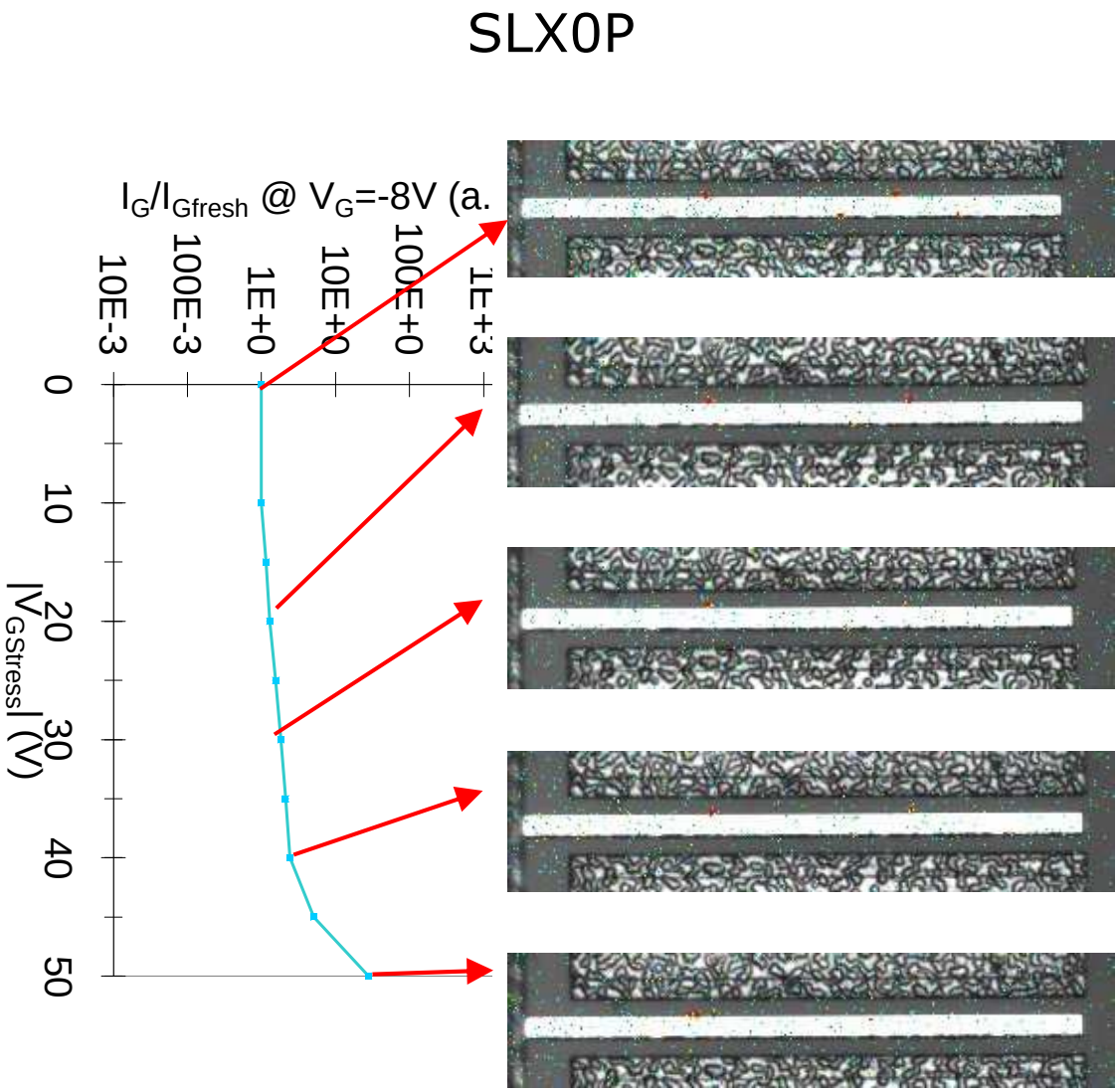


Figure 4.8 On the left Gate current VS Gate voltage bias during the stress. On the right emission images at different step of the stress.

SLX57 wafer show a slight increase of the Gate leakage current and no emission spots appears. As can be seen from Figure 4.9 to Figure 4.18 Drain current and transconductance have a strong increase due to a strong threshold voltage shift; Drain and Source resistance are quite constant.

Main results are:

(a) all devices show common failure modes, consisting in an increase of the reverse gate current, Ig, a (slight) decrease of drain saturation current, IDSS, and transconductance, gm

(b) as already observed in [1],[2], a "threshold" reverse voltage value for degradation exists; this threshold (as well as the amount of gate current increase) remarkably depends on the wafer quality, ranging from ~15 V to more than 100 V: devices belonging to the same wafer show similar threshold values;

(c) during tests, the increase in gate current occurs suddenly, and is correlated in all wafers with the growth of localized "hot spots", which can be detected by electroluminescence, EL, microscopy;

The parametric degradation of all the wafers with Selex processing are summarized from Figure 4.9 to Figure 4.12.

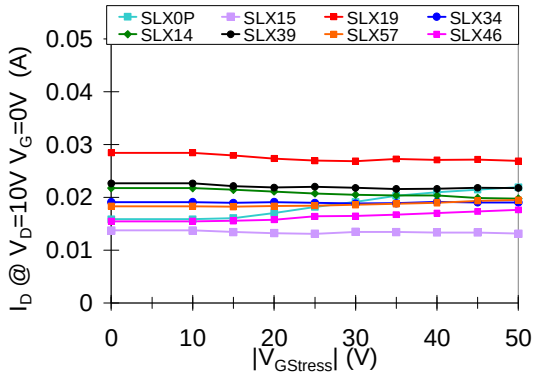


Figure 4.9 Drain current VS $V_{Gstress}$ for all tested wafers

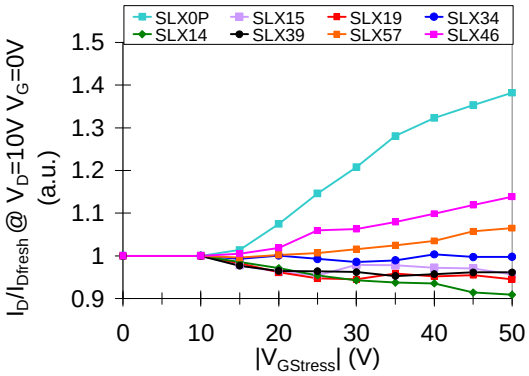


Figure 4.10 Normalized Drain current VS $V_{Gstress}$ for all tested wafers

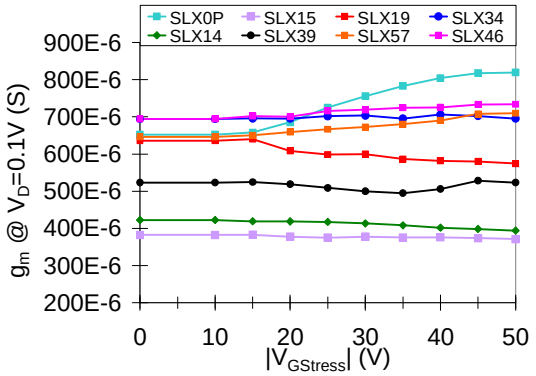


Figure 4.11 Transconductance peak at VD=0.1V VS $V_{Gstress}$ for all tested wafers

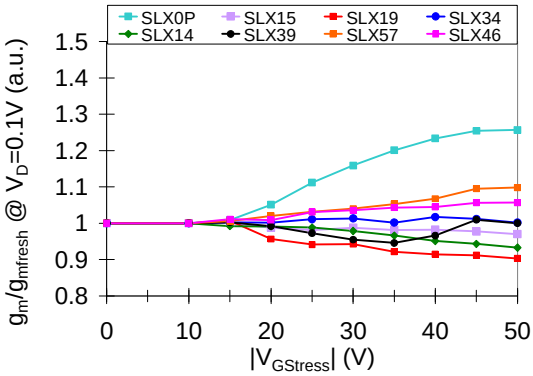


Figure 4.12 Normalized Transconductance VS $V_{Gstress}$ for all tested wafers

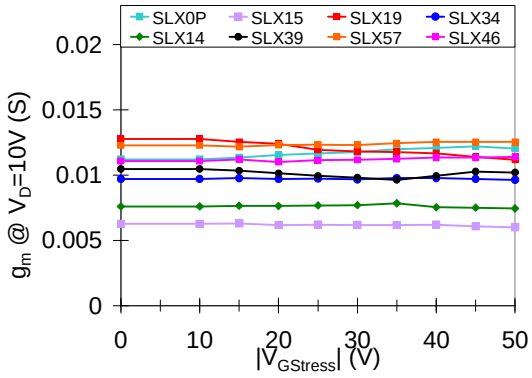


Figure 4.13 Transconductance peak at VD=10V VS $V_{Gstress}$ for all tested wafers

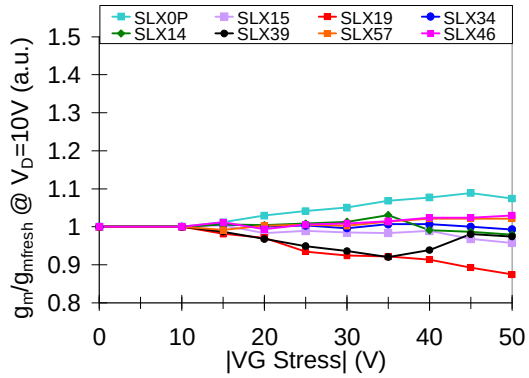


Figure 4.14 Normalized Transconductance peak at VD=10V VS $V_{Gstress}$ for all tested wafers

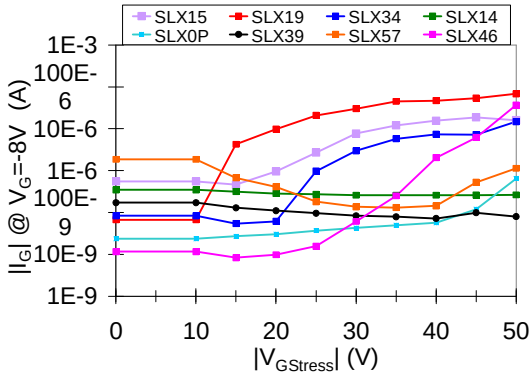


Figure 4.15 Gate leakage current at VG=-8V VS $V_{Gstress}$ for all tested wafers

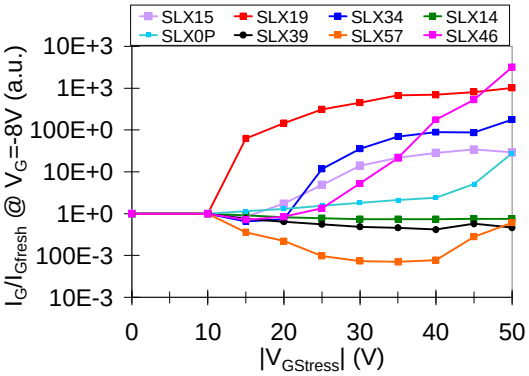


Figure 4.16 Normalized Gate leakage current at VG=-8V VS $V_{Gstress}$ for all tested wafers

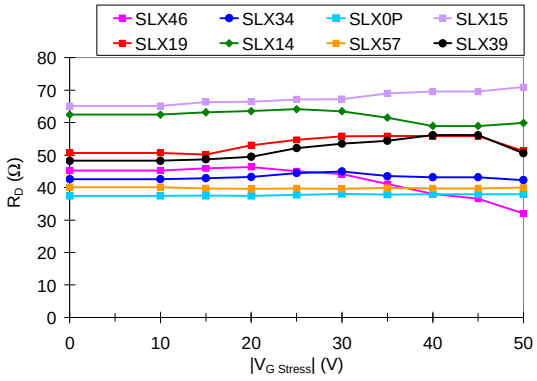


Figure 4.17 Drain resistance VS $V_{Gstress}$ for all tested wafers

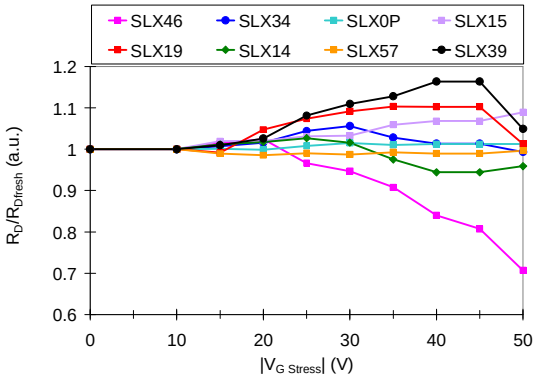


Figure 4.18 Normalized Drain resistance VS $V_{Gstress}$ for all tested wafers

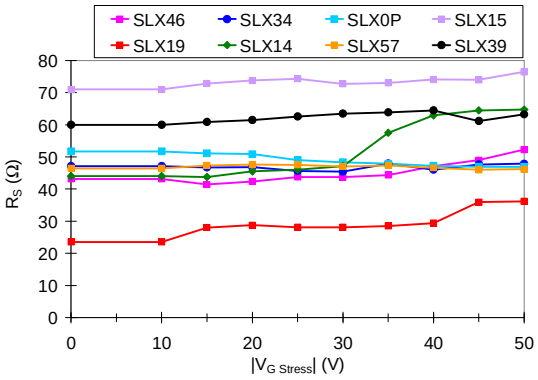


Figure 4.19 Source resistance VS $V_{Gstress}$ for all tested wafers

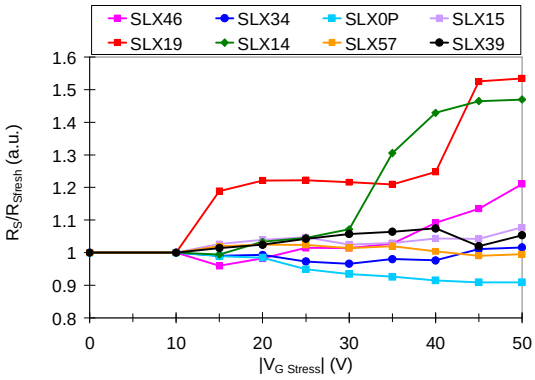


Figure 4.20 Normalized Source resistance VS $V_{Gstress}$ for all tested wafers

In the following pages the correlation between I_G and emission spots presence for QinetiQ (Beast, PeretPan, Tinkerbell) and TRT (AEC1303) wafers during the stress are presented.

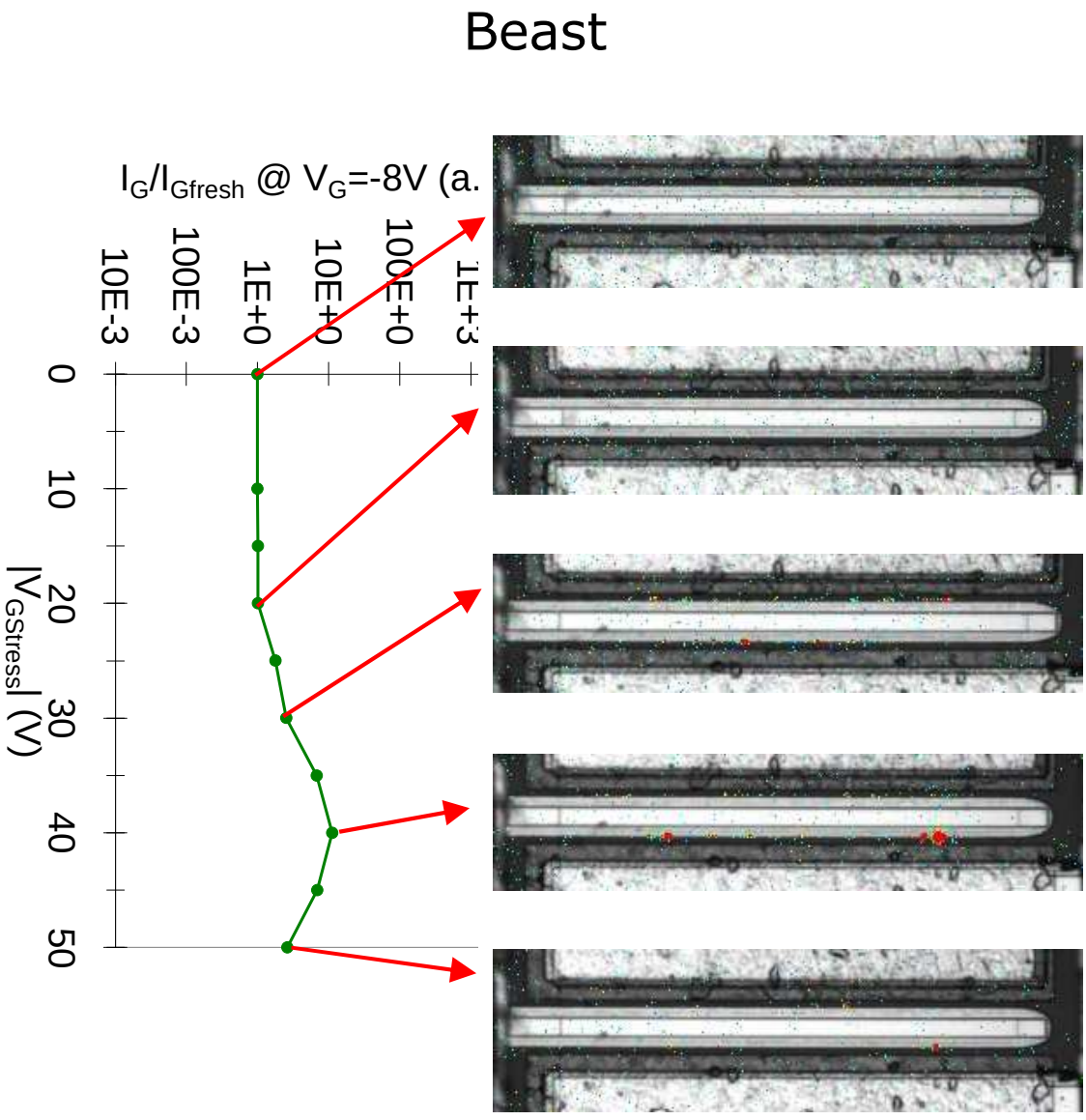


Figure 4.21 On the left Gate current VS Gate voltage bias during the stress. On the right emission images at different step of the stress.

Beast wafer show an increase of the Gate leakage current of one order of magnitude. Emission spots clearly appears as the leakage current increases and disappear as the I_G decrease. The device presents a "soft" degradation (the threshold for this device is $V_{Gstress}$ = -30V). As can be seen from Figure 4.25 to Figure 4.36 Drain current and transconductance decrease during the stress; Drain resistance decrease whereas Source resistance increases.

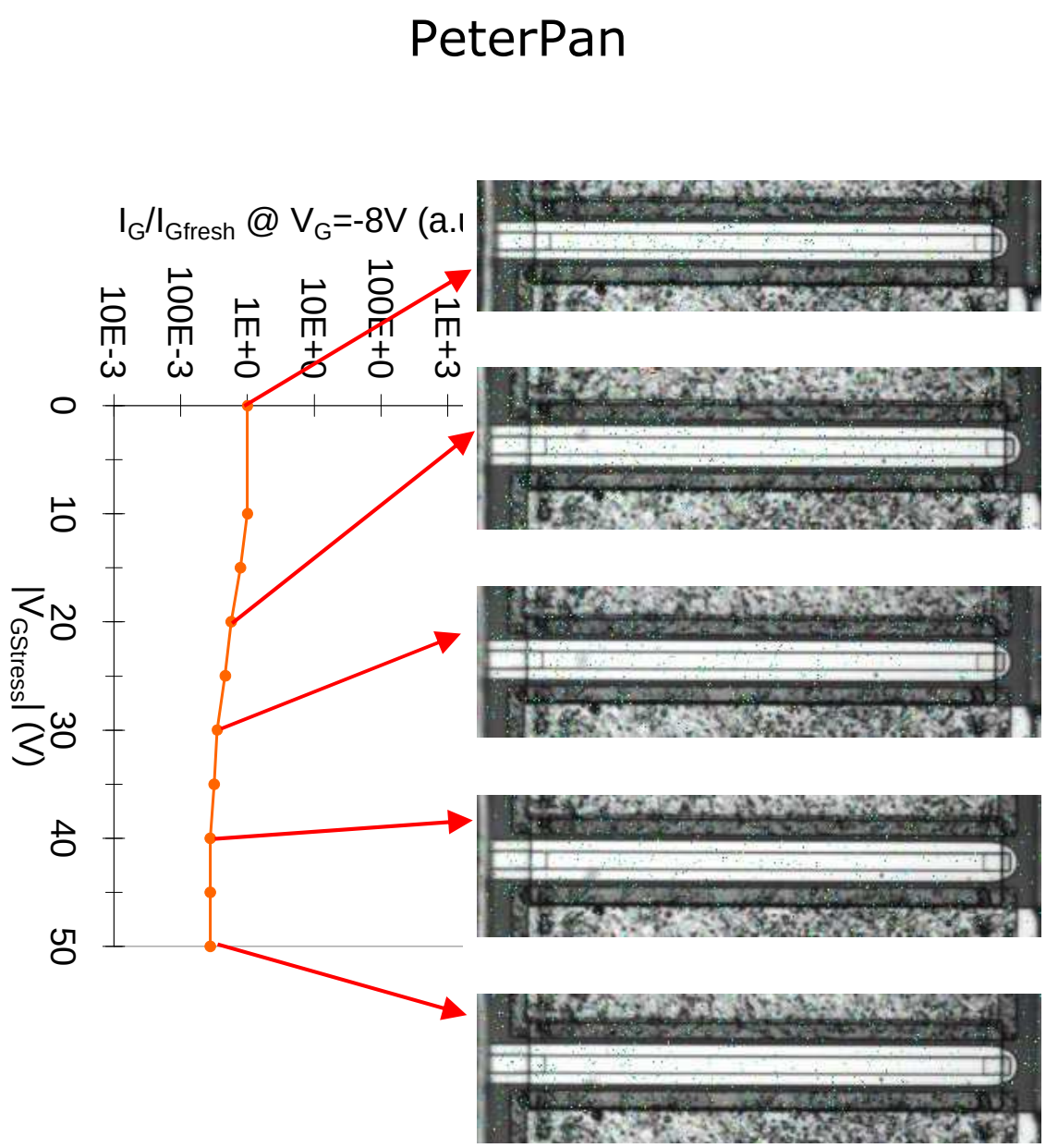


Figure 4.22 On the left Gate current VS Gate voltage bias during the stress. On the right emission images at different step of the stress.

PeterPan wafer show the strongest degradation of DC parameters all wafers. No emission spots appear and the leakage current is constant. As can be seen from Figure 4.25 to Figure 4.36 Drain current and transconductance decrease of about 80% during the stress; Drain and Source resistance increase of more than three times their initial values.

Tinkerbell

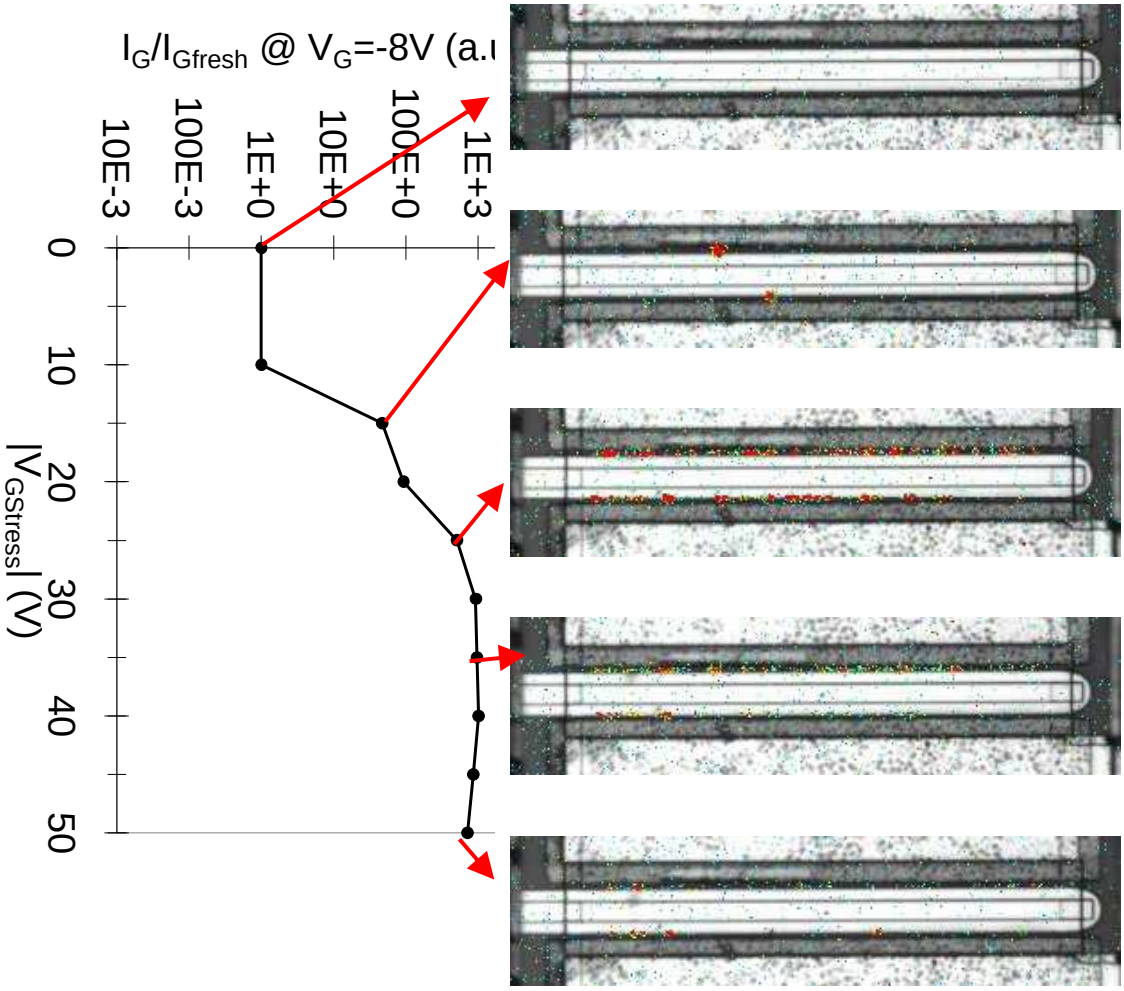


Figure 4.23 On the left Gate current VS Gate voltage bias during the stress. On the right emission images at different step of the stress.

Tinkerbell wafer show the strongest increase of the Gate leakage current in all QinetiQ wafers. Emission spots clearly appears as the leakage current increases. The device presents a sudden I_G degradation (the threshold is $V_{Gstress}$ = -15V); at the end of the stress I_G is three order of magnitude in respect to the I_G of the fresh device. As can be seen from Figure 4.25 to Figure 4.36 Drain current, transconductance ,Drain resistance and Source resistance do not change during the stress.

AEC1303

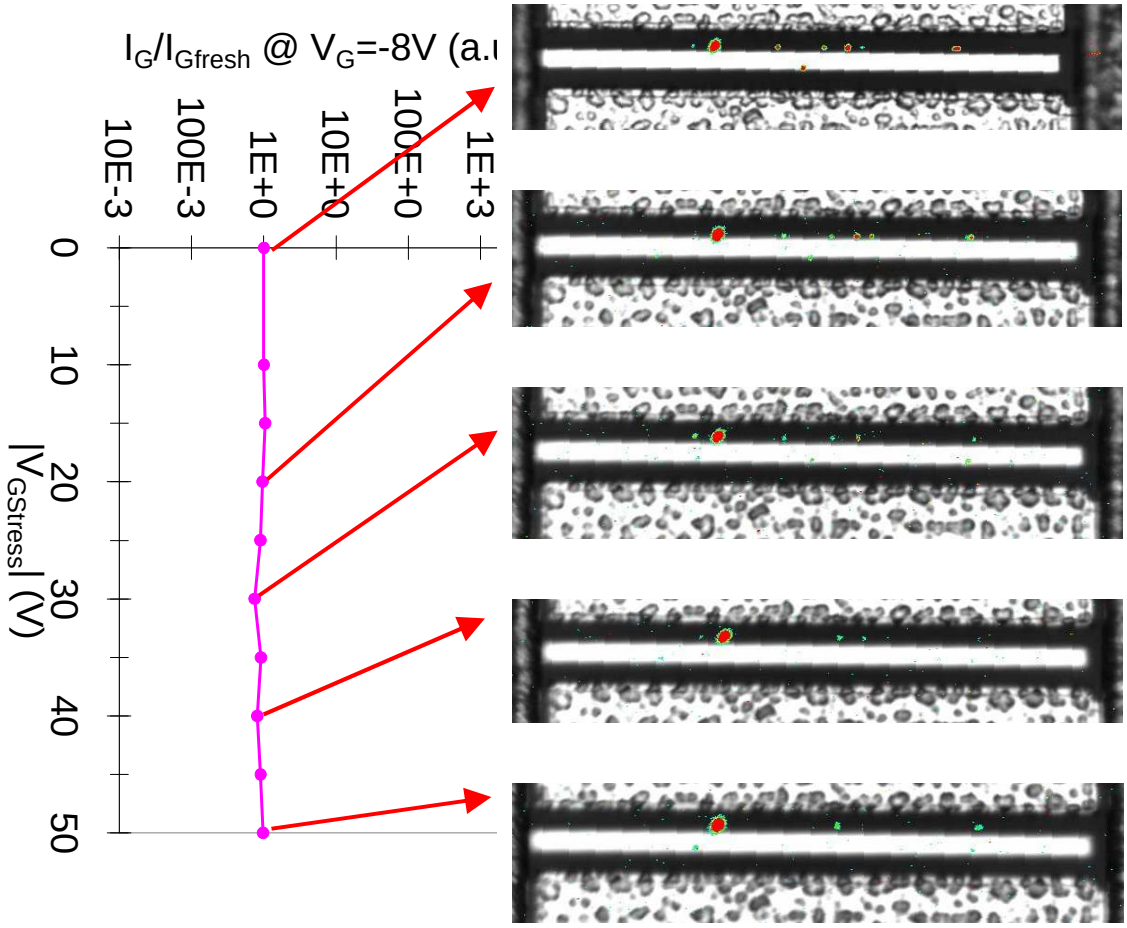


Figure 4.24 On the left Gate current VS Gate voltage bias during the stress. On the right emission images at different step of the stress.

In AEC1303 wafer the initial values of the gate leakage current was very high (from Figure 4.25 to Figure 4.36), all the gated-TLM tested present the same problem. This is due to the presence of a leakage path visible with emission in the fresh devices. During the stress only tiny spots appear and disappear. Drain current and transconductance decrease slightly whereas Drain resistance and Source resistance do not change during the stress.

Main results are:

(a) these group of devices show different failure modes: the first is like the one for Selex process devices, the other consists in a strong decrease of drain saturation current, I_{DSS}, and transconductance, gm whereas the reverse gate current, Ig, stays unchanged.

(b) In wafer AEC1303 no correlation between the growth of localized "hot spots", and increase of IG can be detected due to the already damaged fresh device.

The parametric degradation of all the wafers with QinetiQ and TRT processing are summarized from Figure 4.25 to Figure 4.36.

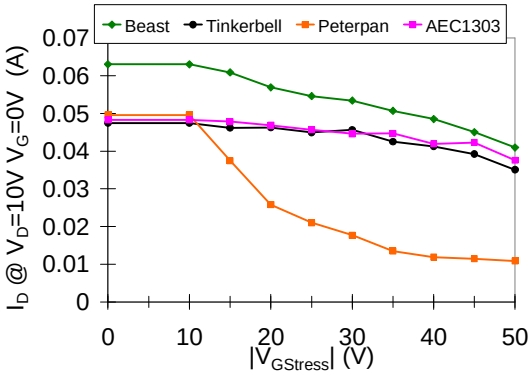


Figure 4.25 Drain current VS $V_{Gstress}$ for all tested wafers

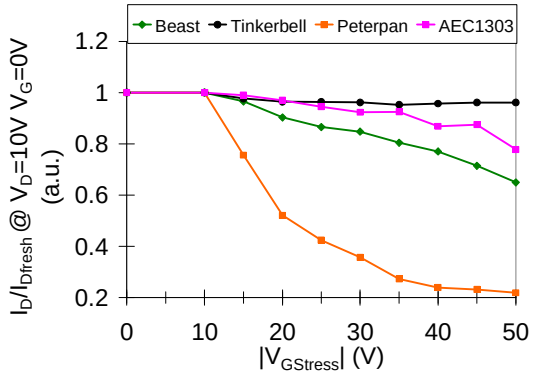


Figure 4.26 Normalized Drain current VS $V_{Gstress}$ for all tested wafers

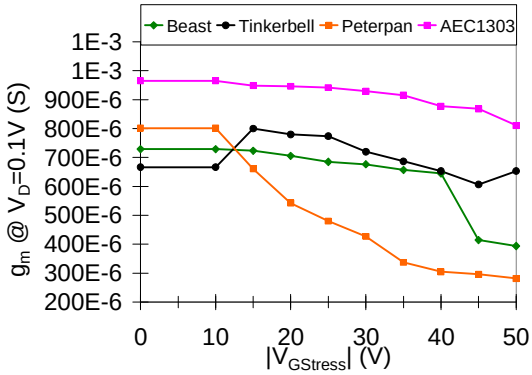


Figure 4.27 Transconductance peak at VD=0.1V VS $V_{Gstress}$ for all tested wafers

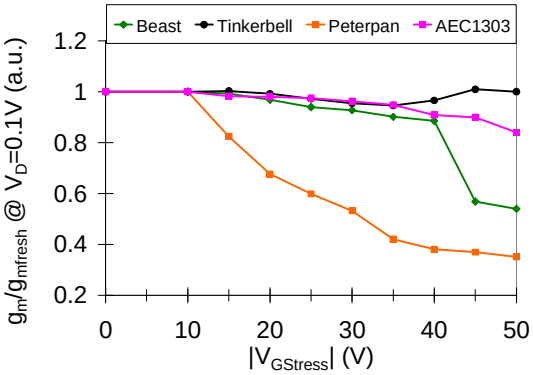


Figure 4.28 Normalized Transconductance VS $V_{Gstress}$ for all tested wafers

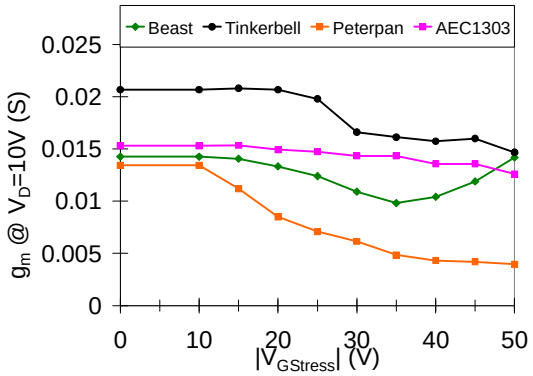


Figure 4.29 Transconductance peak at VD=10V VS $V_{Gstress}$ for all tested wafers

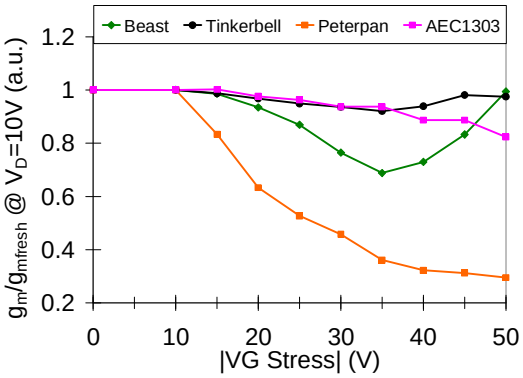


Figure 4.30 Normalized Transconductance peak at VD=10V VS $V_{Gstress}$ for all tested wafers

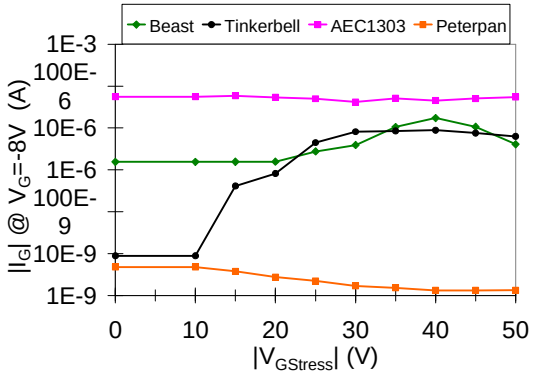


Figure 4.31 Gate leakage current at VG=-8V VS $V_{Gstress}$ for all tested wafers

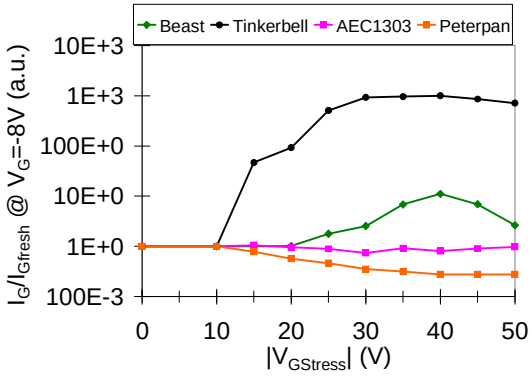


Figure 4.32 Normalized Gate leakage current at VG=-8V VS $V_{Gstress}$ for all tested wafers

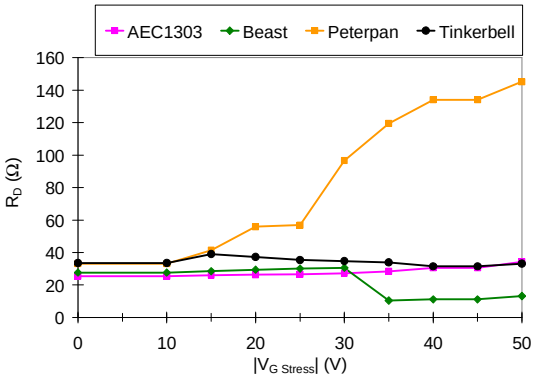


Figure 4.33 Drain resistance VS $V_{Gstress}$ for all tested wafers

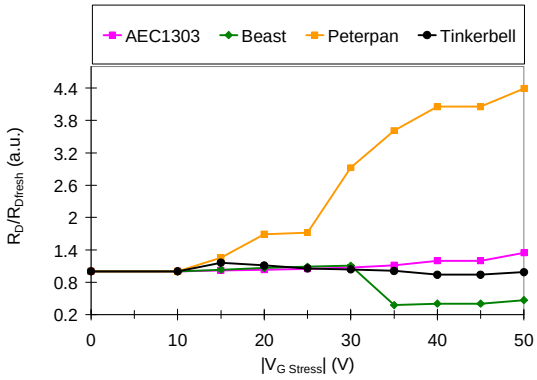


Figure 4.34 Normalized Drain resistance VS $V_{Gstress}$ for all tested wafers

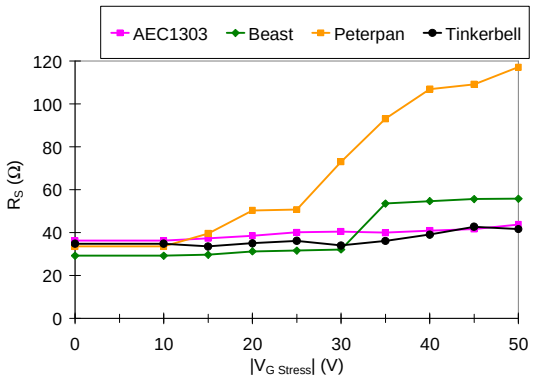


Figure 4.35 Source resistance VS $V_{Gstress}$ for all tested wafers

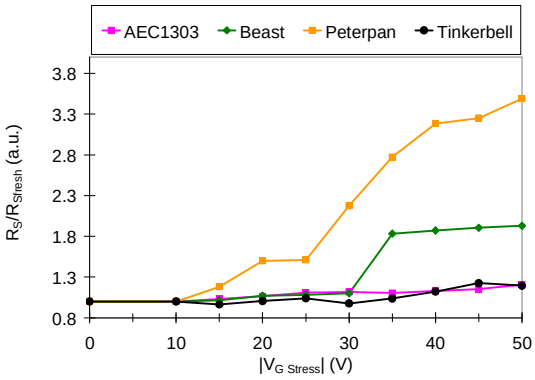


Figure 4.36 Normalized Source resistance VS $V_{Gstress}$ for all tested wafers

4.3 Double Pulse measurements

Double-pulse measurements are being carried out, and an increase in the current slump (demonstrating an increase in trap density) was verified, Figure 4.37. The amount of current collapse (or trap density) is correlated with the increase of gate leakage current observed in the five tested wafers.

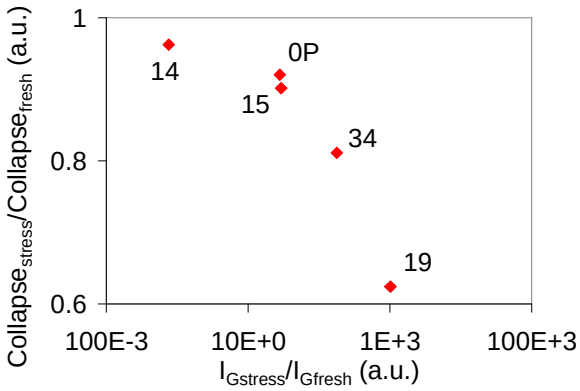


Figure 4.37 Double-pulse measurements on several Selex wafers

4.4 EBIC and SEM

On a device of wafer SLX34 submitted to reverse stress have been performed both EBIC and SEM analysis.

As can be seen from Figure 4.40 there is a correspondence between emission and EBIC measurement. The section indicated by the arrow is the one studied by SEM imaging.

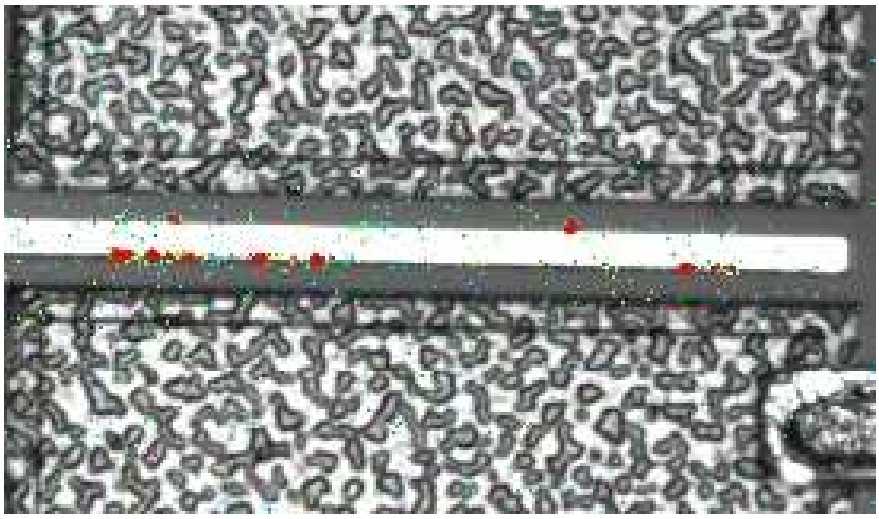


Figure 4.38 Emission image for $V_S = V_D = 0V$, $V_G = -10V$, t = 100 s after the step at $V_G = -50V$ for a SLX34 device.

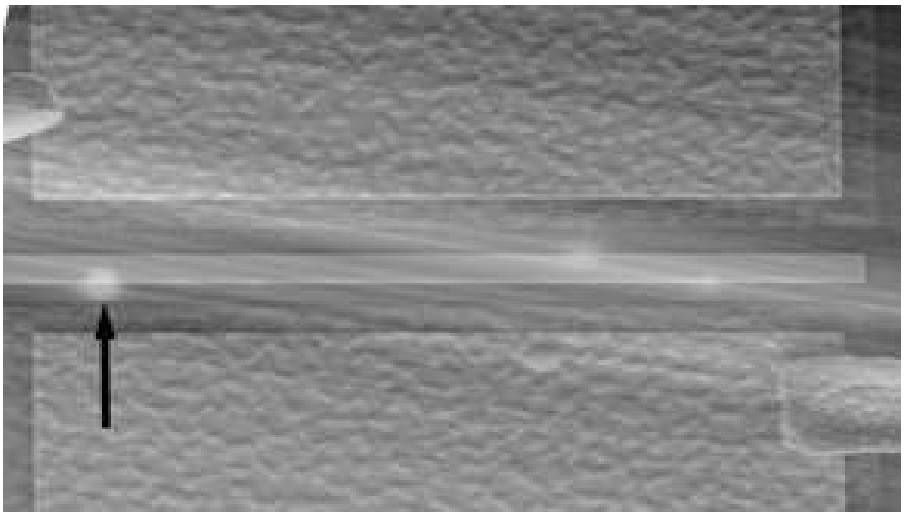


Figure 4.39 EBIC image image for $V_S = V_D = 0V$, $V_G = -4V$, t = 180 s after the step at $V_G = -50V$ for the same SLX34 device of Figure 4.38.

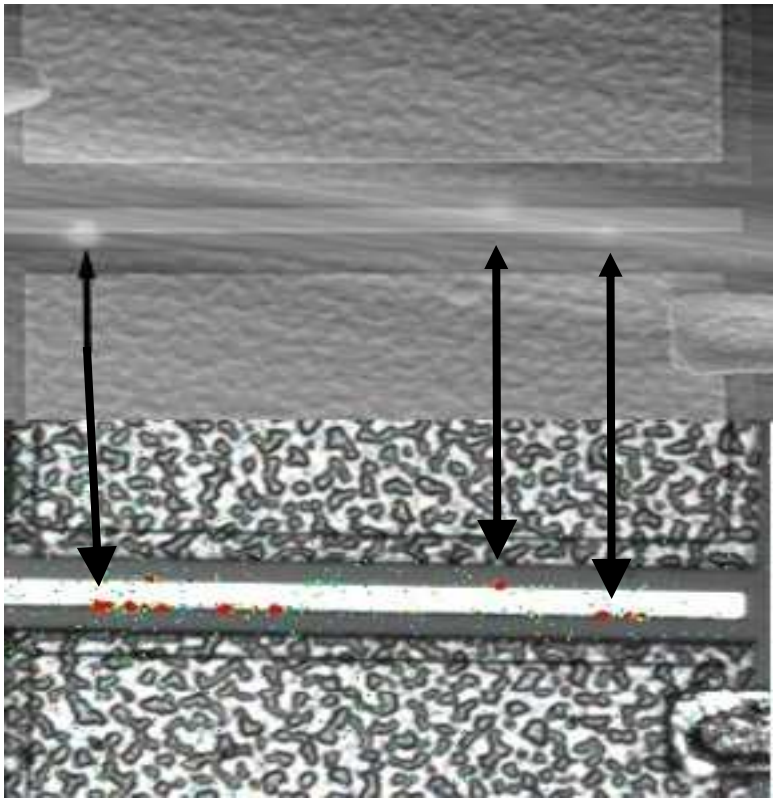


Figure 4.40 Correspondence between emission and EBIC spots.

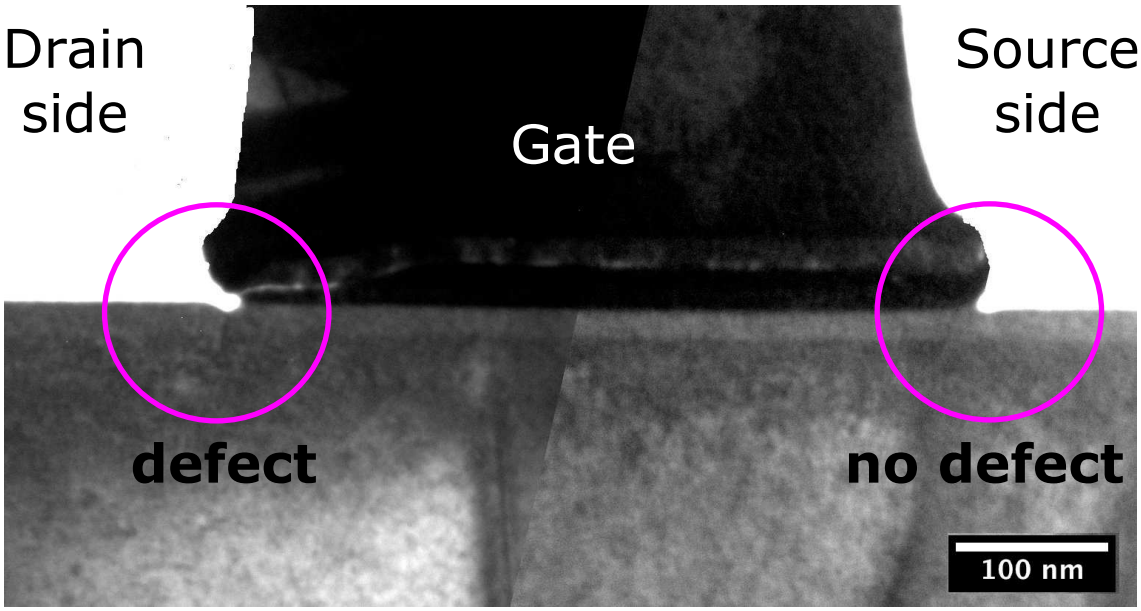


Figure 4.41 SEM section of the device in Figure 4.38. A damage in the AlGaN layer in the gate to drain region seems to be present, defects in GaN are also evident [9].

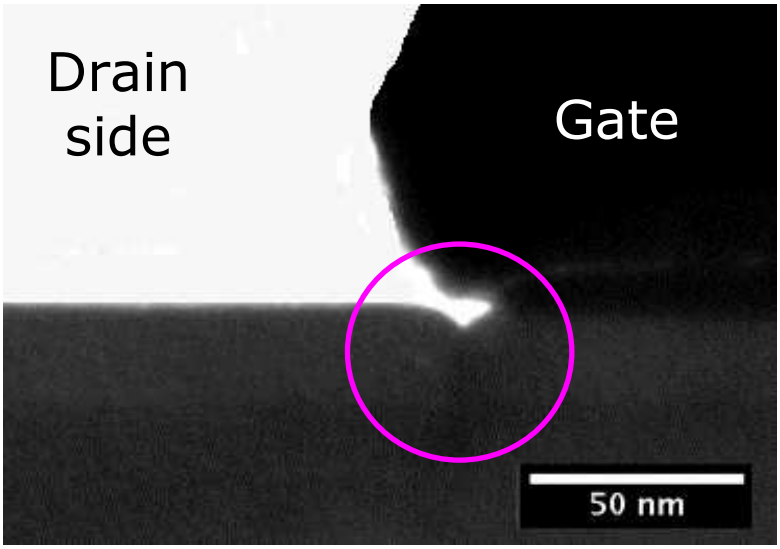


Figure 4.42 Magnification of the gate to drain side. It is possible to see a "V" shape defect that can be responsible of the emission and EBIC spot [9].

4.5 Breakdown walkout effect

On a wafer with no detectable degradation (SLX14) we performed at each step of stress not only the emission in OFF condition (V_S = V_D = 0V and V_G = -10V) but also in ON condition (V_S = 0V V_D = 20V and V_G = 0V). The gate voltage bias during the stress was from V_G = -15 V up to V_G = -100V. As can be seen in Figure 4.43 fresh devices had a stronger emission than the one after the stress up to V_G = -40V (Figure 4.44). The decrease of emission is confirmed also by Figure 4.45 and Figure 4.46, respectively the emissions after V_G = -60V and after V_G = -100V. The total photon count during the stress is summarized in Figure 4.47. We performed also TLP-TDR breakdown measurements (see Figure 4.48). The measurements show that the breakdown voltage of the fresh device is 170 V whereas the bd voltage of the one after the stress up to V_G = -100 V is 320V. This effect can possibly be attributed to the breakdown walkout effect.

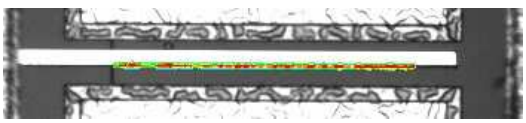


Figure 4.43 EMMI images obtained at V_S = 0V V_D = 20V and V_G = 0 V for the

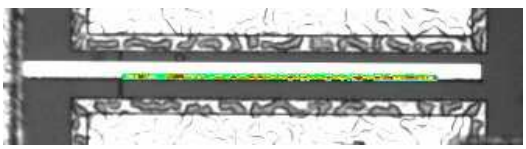


Figure 4.44 EMMI images obtained at V_S = 0V V_D = 20V and V_G = 0 V after the stress

fresh device fresh on wafer SLX_14.

Figure 4.45 EMMI images obtained at V_S = 0V V_D = 20V and V_G = 0 V after the stress up to V_G = -60V on wafer SLX_14.

up to V_G = -40V on wafer SLX_14.

Figure 4.46 EMMI images obtained at V_S = 0V V_D = 20V and V_G = 0 V after the stress up to V_G = -100V on wafer SLX_14.

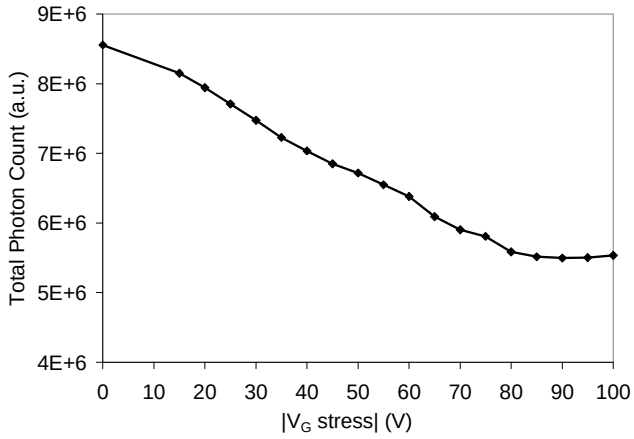


Figure 4.47 Total Photon Count obtained for V_S = 0V, V_D = 20 V and V_G = 0 V conditions during the stress with V_G from -15 V to -100 V

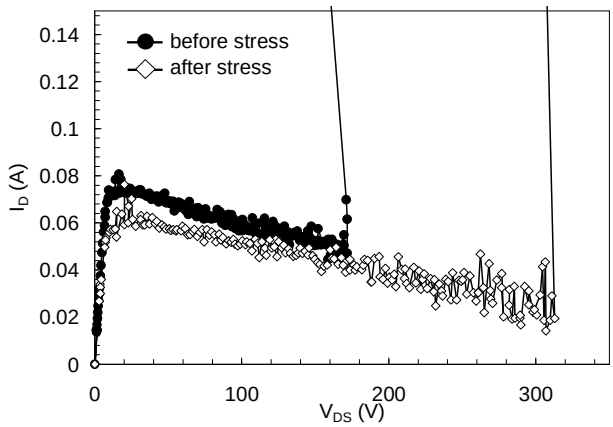


Figure 4.48 TLP-TDR measurement of a fresh device and of a stressed (up to V_G = -100V) device.

4.6 Conclusion

In the "on-state" EL images (VDS=20 V, VGS=0 V) of untreated and stressed devices, an evenly distributed emission is observed, without "hot spots", thus suggesting that localized defects have a limited influence on carrier transport in the device channel. A gradual decrease in the EL total photon count is measured. Following the model which attributes light emission to intraband transitions of highly energetic channel electrons [8], this corresponds to a decrease in the population and/or energy of hot carriers. This is confirmed by breakdown voltage (BV) measurements: untreated devices have a source-drain (gate floating) BV ≈180 V (measured using 100 ns pulses, Figure 4.48). After stress, BV increases up to 300 V due to the breakdown walkout effect: electrons trapped at the surface of the gate-drain region induce a change in the electric field profile and a decrease of the maximum electric field, thus increasing BV.

Experiments strongly suggest that the defectivity of the epitaxial material contributes to enhance reverse-bias degradation of GaN HEMTs; when a certain reverse voltage is reached, depending on defect density and energy position of deep levels, trap-assisted tunneling occurs, focusing the current into specific areas, eventually resulting in permanent localized degradation, with further generation of deep levels. A different (and gradual) mechanism consists in the trapping of electrons at the surface of the gate-drain region, which increases parasitic resistances, reduces I_D and g_m and induces breakdown walkout. The latter is a well-known failure mechanism of GaAs HEMT's, but has not been observed previously in GaN devices.

4.7 References

[1] U. K. Mishra, L. Shen, T. E. Kazior, Y.-F. Wu, "GaN-based rf power devices and amplifiers Proc. IEEE, vol. 96(2), pp. 287-305, 2008.

[2] R. Quay, "Gallium Nitride Electronics", Springer, Berlin 2008.

[3] Jungwoo Joh and Jesús A. del Alamo, "Critical voltage for electrical degradation of GaN high-electron mobility transistors", IEEE El. Dev. Lett., vol. 29(4), pp.287-289, 2008.

[4] J. Joh and J. A. del Alamo, "Mechanisms for electrical degradation of GaN high-electron mobility transistors," in IEDM Tech. Dig., 2006, pp. 415–418.

[5] J. Joh, L. Xia, and J. A. del Alamo, "Gate current degradation mechanisms of GaN high electron mobility transistors," in IEDM Tech. Dig., 2007, pp. 385–388.

[6] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, M. Meneghini, and E. Zanoni, "Reliability of GaN High-Electron-Mobility Transistors: state of the art and perspectives", IEEE Trans. on Dev. and Materials Reliability, vol. 8 (2), pp. 332-343, 2008.

[7] E. Zanoni, G. Meneghesso, G. Verzellesi, F. Danesin, M. Meneghini, F. Rampazzo, A. Tazzoli, F. Zanon, "A review of failure modes and mechanisms of GaN-based HEMTs", in IEDM Tech. Dig., 2007, pp. 381-384, 2007.

[8] N. Shigekawa, K. Shojima, T. Suemitsu, „Optical study of high-biased AlGaN/GaN High Electron Mobility Transistors", J. Appl. Phys, vol. 92, pp. 531-535, 2002.

[9] U. Chowdhury, J. L. Jimenez, C. Lee, E. Beam, P. Saunier, T. Balistreri, S.-Y. Park, T. Lee, J. Wang, M. J. Kim, J. Joh, and J. A. del Alamo, "TEM observations of crack- and pit-shaped defects in electrically degraded GaN HEMTs", IEEE El. Dev. Lett., vol. 29(10), pp. 1098-1100, 2008.

5.ESD characterization

5.1 Introduction

In GaAs based devices, hot carrier effects are usually evaluated by measuring the gate current due to collection of holes generated by impact-ionization [1]. The gate current I_G has also been used to derive field-acceleration laws for the failure time of AlGaAs/GaAs HEMTs submitted to hot electron tests at constant I_G [2]. According to Chynoweth's law [3], in an n-channel GaAs FET, the $|I_G|/I_D$ ratio is proportional to the αL_{eff} product, where α is the electron impact-ionization coefficient of the channel material, while L_{eff} is the extension of the channel region where impact ionization takes place [4]:

$$|I_G|/I_D \cong \alpha L_{eff}$$
$$\cong L_{eff} \exp(-1/\xi)$$
$$\cong L_{eff} \exp(-L_{eff}/(V_{DS} - V_{DSAT}))$$

Here ξ is the longitudinal electric field in the L_{eff} region and V_{DSAT} is the drain saturation voltage. According to this equation, by plotting $\ln(|I_G|/I_D)$ vs $1/(V_{DS} - V_{DSAT})$, a straight line is obtained.

Furthermore, in GaAs and InP HEMTs, a significant portion of the holes generated by impact ionization at the drain side travel towards the source, where they

accumulate and recombine with electrons, giving rise to the typical band-to-band emission at the source side of the HEMTs [5].

In wide bandgap semiconductor GaN HEMTs, the impact ionization is extremely low and hardly detectable. In fact, it has never been reported so far in literature either an evident "bell shaped" gate current (the "best" bell-shape reported can be seen in [6] and the leakage current is not negligible) as well as the band-to-band emission at the gate-to-source side of a GaN HEMT. Moreover, many parasitic effects contribute to I_G in these devices: for instance surface conductive paths between Gate and Drain. For these reasons, I_G is not a reliable predictor for hot carrier effects in GaN- HEMTs.

To overcome this problem, we used electroluminescence (EL) measurements as an alternative method to evaluate hot-carrier effects and their dependence on bias conditions. Electroluminescence in GaN HEMTs has been reported by various authors. Nakao [7] and Shigekawa [8], [9] showed that light emitted by GaN HEMTs can be due to intraband transitions of highly energetic electrons that acquire kinetic energy in the high field region of the channel.

In Figure 5-1(a) false colour image of the light emitted from a GaN HEMT (L_G=1 μm) biased at V_{GS}=0 V and V_{DS}=16 V is shown. An Hamamatsu PHEMOS-200 light emission microscope (EMMI) was used. Photons are homogeneously emitted without hot spots and, moreover, no emission is revealed on the gate-source side. In Figure 5-2 the total photon emission is presented for the same device together with the corresponding I_G. V_{DS} was kept varied from 8 V to 18 V, whereas V_{GS} was varied from pinch-off to open channel conditions. The "bell-shaped" behaviour is present only in the light emission but not in the I_G.

The "bell-shaped" behaviour can be explained as follow. When V_{GS} is smaller than the pinch-off value, the gate-drain voltage V_{GD} and the electric field are maximum, but there are no carriers in the channel, so that no light is emitted. When V_{GS} is increased over the pinch-off value, carriers start flowing in the channel and are "heated" by the high electric field in the gate-drain region. Correspondingly, light emission is detected and its intensity increases as V_{GS} is increased due to the larger primary electrons population in the channel, see Figure 5-2. At the same time, however, the Gate-Drain voltage and, consequently, the electric field, decrease as far as the V_{GS} is increased. Beyond a certain value of V_{GS}, therefore, electrons are less energetic, and the emitted light starts to decrease.

It is therefore clear that should be considered the correlation between hot carriers and light emission rather than any gate leakage current. Relying on this, instead of plotting the $|I_G|/I_D$ ratio (as in [10]) we substituted the EL intensity for $|I_G|$ and plotted the EL/I_D ratio as a function of $1/(V_{DS}-V_{DS,sat})$ (being $V_{DS,sat}=V_{GS}-V_{TH}$). As can

be seen in Figure 5-3, a straight line is obtained, thus confirming that the EL intensity is a good indicator of the presence of hot-electrons in the channel.

Figure 5-4(a) shows the electroluminescence image of a QinetiQ device biased at V_{DS} = 20 V, V_{GS} = 0 V, in on-state conditions. The emission is evenly distributed along the channel, without hot spots or current crowding effects and is due to channel hot electrons. Figure 5-4(b) shows the corresponding image close to pinch-off conditions, i.e. with V_{GS} = -6 V. In the latter case the presence of preferential emission sites is observed, possibly due to the contribution to electroluminescence of electrons injected from the gate into the channel. Due to the band discontinuities and to the large band bending corresponding to V_{GD} = -26 V, these electrons can acquire a large energy and give rise to photon emission.

Figure 5-5 shows the electroluminescence spectra respectively of a Thales device, a), and of a QinetiQ device, b), both in "on-state" conditions. When biased at high V_{DS}, devices have been found to emit light characterized by a continuous spectrum without remarkable features, which, for the tested devices in the 20 V - 30 V V_{DS} range, can be fitted by a Maxwellian distribution with equivalent temperatures in the 1500 - 3000 K range. No evidence of e/h recombination is found in these spectra (there is no band-to-band recombination peak corresponding to the energy gap of GaN or AlGaN); the EL intensity is generally small when compared to the corresponding signal of GaAs-based devices.

For what concerns hot-electron-induced degradation, therefore, the most dangerous bias conditions should therefore correspond, for a given V_{DS}, to "semi-on" conditions, close to the maximum of the EL vs. V_{GS} curve.

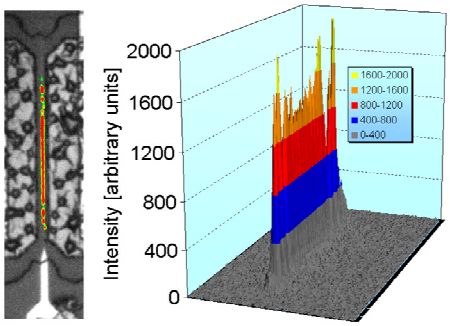


Figure 5-1 EL intensity at V_{GS}=0V, V_{DS}= 16 V.

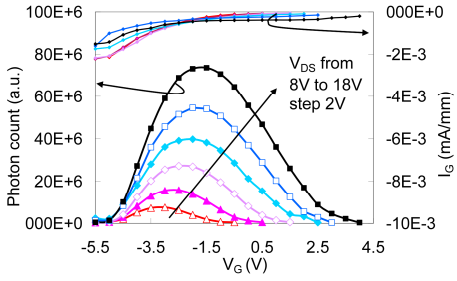


Figure 5-2 EL and I_G vs. V_{GS} at high V_{DS} (8 – 18 V).

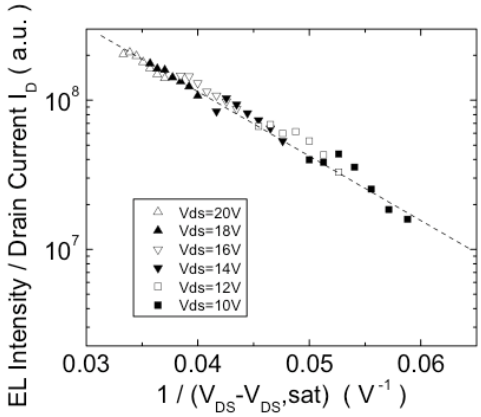


Figure 5-3 EL/I_D vs. $1/(V_{DS} - V_{DS,sat})$ for different V_{DS} values.

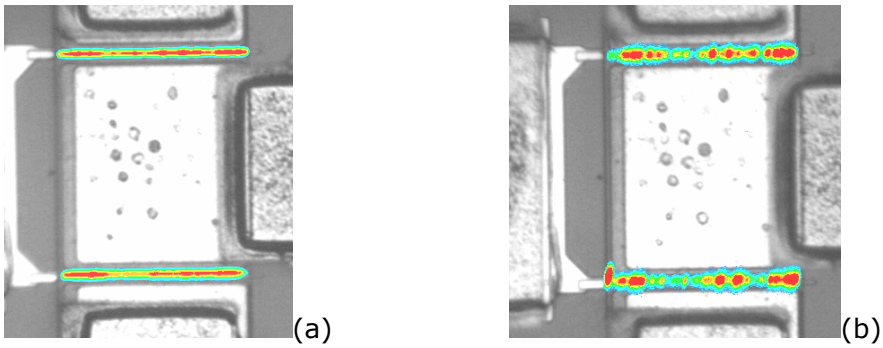


Figure 5-4a) electroluminescence micrograph of a QuinetiQ-Gibson device (EL intensity in false colours) in open channel conditions at V_{DS} = 20 V, V_{GS} = 0 V; b) EL micrograph of the same device close to pinch-off conditions, V_{DS} = 20V, V_{GS} = -6 V.

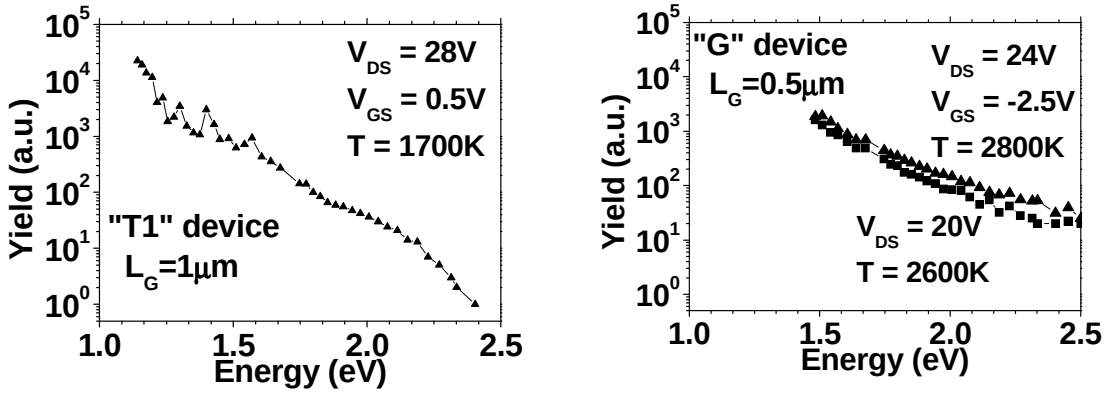


Figure 5-5a) electroluminescence spectrum of a ThalesAEC1024 device biased in open channel conditions at V_{DS}=20 V, V_{GS} =+0.5V. An equivalent temperature T=1700 K is derived by fitting the spectrum with Maxwellian distribution; b) EL spectrum of a HEMT device at V_{DS} = 20 V and 24 V, V_{GS} = -2.5 V. Equivalent temperature T = 2600 K.

Electrostatic discharge (ESD) and electrical overstress (EOS) events are an important issue also for GaN-based HEMT devices and very few data have been presented in literature regarding this aspect. J. Kuzmik et al. have demonstrated the capability of AlGaN/GaN HEMT devices to work in snapback regime, at low current level, without any degradation of the electrical characteristics [11-12] up to the failure point, a catastrophic failure was then observed, accompanied by filament formation. ESD events may change electrical characteristics (on-current, transconductance, and leakage current), and the reliability can be impaired by the migration of metals caused by the high electric field and high temperature under ESD stress.

In this chapter we report on the characterization of the breakdown properties of the GaN-based devices. We have carried out the analysis of two terminal breakdown properties of devices; Gate-to-Drain and Gate-to-Source breakdown values from 45 to 150 V has been found.

A three terminal breakdown evaluation has been carried out in pulsed condition (by means of a 100 ns pulser system developed ad hoc for this kind of investigation). Breakdown voltages in some devices are strongly dependent on gate bias (the more negative is the gate bias (lower current level) the higher is the breakdown voltage), while in other devices the breakdown is almost independent from the gate bias. Failure analysis revealed that two main failure mechanisms following the destructive breakdown characterization are present: GaN-lattice degradation (possibly related to a pre-existing crystal defect) and metal filamentation due to metal fusion.

Eventually we have also submitted the devices to Electrostatic Discharge evaluation using TLP (Gate-Source TLP stress and Gate-Drain TLP stress have been performed) and the HBM model. During Gate-Drain TLP stress (pulse applied between Drain and Source, Gate floating) we have monitored the V_{GS} waveforms and the I_{GS} current, in DC regime, after each TLP pulses. An important thing to be noticed is that a strong capacitive coupling between the Drain, Gate, and Source terminals is present, impairing the reliability of the Gate-Source Schottky diode. We also found out that the electrical parameter that can predict the device failure is the I_{GS}. Thus, we demonstrate that the traditional "leakage current" measurement, typical of a TLP system, is insufficient to reveal device degradation. The scaling of the failure current with the device width, both for Drain and Gate stresses, has been also investigated. We observed a completely different failure mode in Gate-Source TLP stress involving Gate metal line fusion.

5.2 Device description

In Table 5-1 the wafers on which breakdown and the ESD sensitivity have been studied are summarized.

Fab	Wafer	Sub.	Sub.Suppl.	Epitaxy	Al (nm)	Al (%)
Selex	AMS04	SiC	Cree	QinetiQ	25	26
Selex	AMS09	Sapphire	Commercial	QinetiQ	25	26
Selex	SLX15	Sapphire	Commercial	QinetiQ	26	26
Selex	SLX19	SiC	Norstel	Picogiga	23	28
Selex	SLX02	SiC	Cree	TRT	25	28
Selex	SLX25	SiC	Norstel	QinetiQ	25	28
QinetiQ	ATACAMA	SiC	Cree	QinetiQ	30	28
QinetiQ	GIBSON	SiC	Cree	QinetiQ	30	28
QinetiQ	RHODES	SiC	Cree	QinetiQ	27	28
QinetiQ	PETER PAN	SiC	Cree	QinetiQ	28	25
QinetiQ	TINKERBELL	SiC	Norstel	QinetiQ	28	25
QinetiQ	BEAST	SiC	Cree	TRT	27.5	30

Table 5-1 Devices submitted to Breakdown characterization.

5.3 Two terminal DC breakdown

In order to identify specific properties of the different epi-layers and mask processing and to characterize the breakdown behaviour of GaN-HEMT devices of Table 5-1 we have carried out a two-terminal DC breakdown, i.e. Gate-to-Drain and Gate-to-Source breakdown. Through some simple optical images, we have identified location and possible explanation of the observed breakdown.

Two terminal breakdown characterization is carried out biasing the Gate vs the Drain, keeping the source floating (GD) or biasing Gate vs the Source, keeping the drain floating (GS).

In Figure 5-6 we report the two terminal breakdown characterization of a representative sample of the SLX25 devices. More specifically, we report the G-S breakdown (a), and the G-D breakdown (b). Tested devices have W_G = 1 mm. The larger breakdown of the GD junction can clearly be attributed to the GD distance (2.05 um) that is larger than the GS distance (1.15 um).

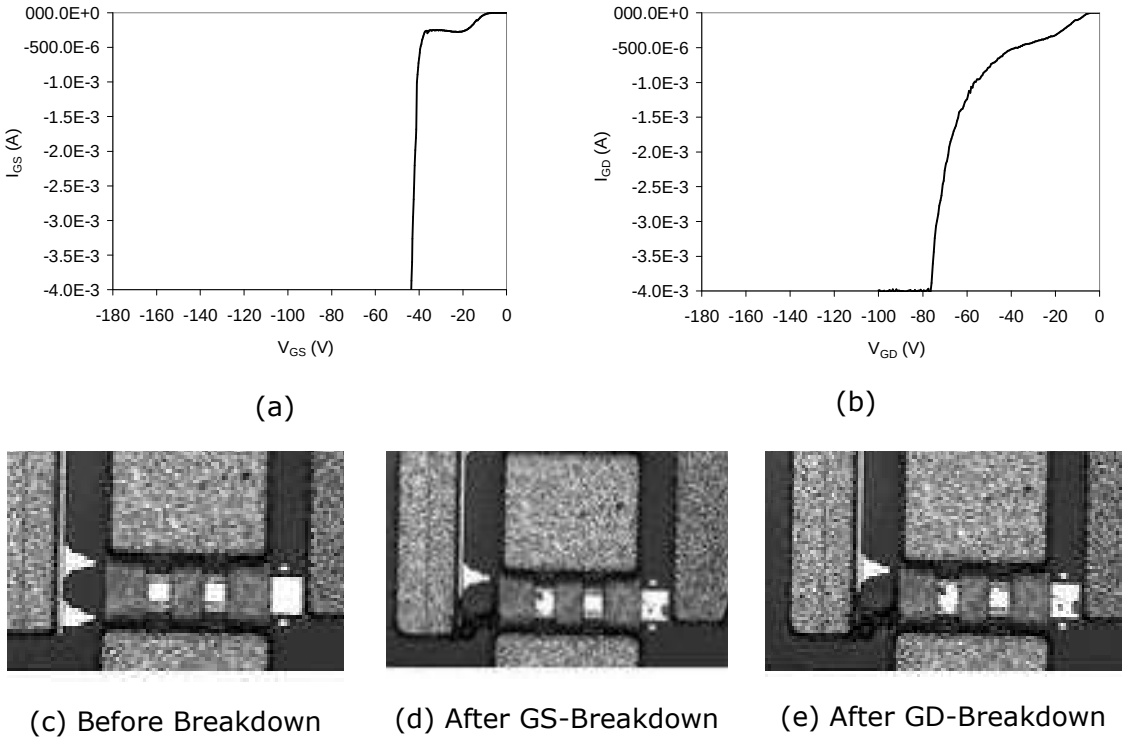
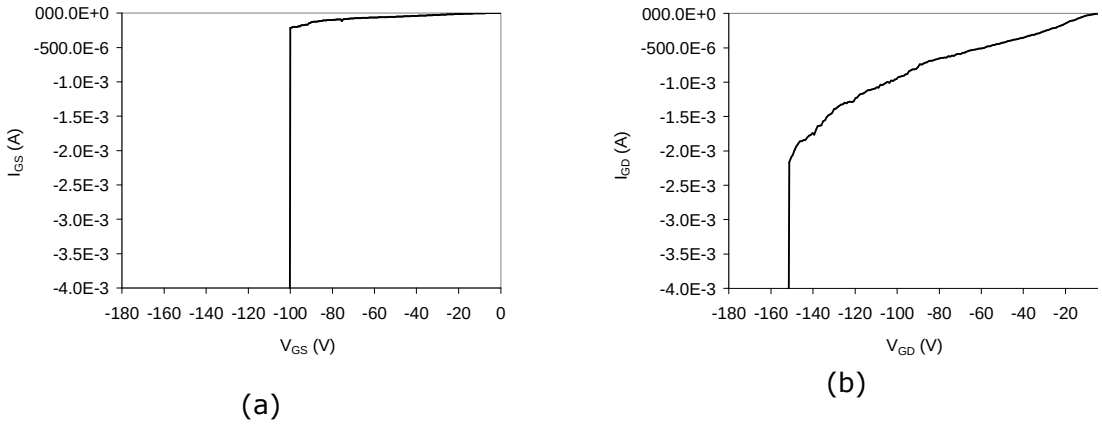
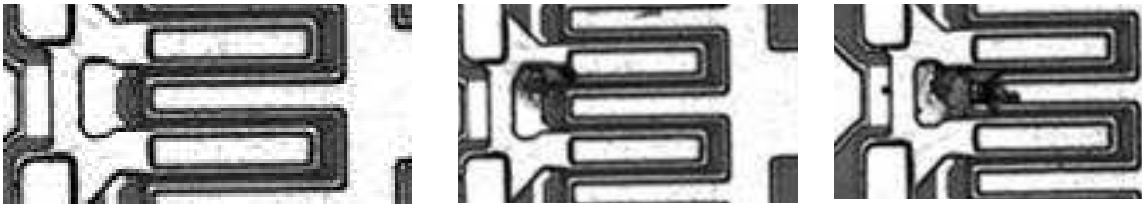


Figure 5-6(a) Gate to source and (b) Gate to Drain breakdown measurement in SLX25 device. Bottom figures refer to a fresh device (c), and to device after breakdown measurements (d,e)

In Figure 5-6 (a), (b) and (c) we report the optical images of the device area that is subjected to catastrophic failure after the breakdown measurement itself: (a)the device before the breakdown measurement, (b) the image after the GS breakdown measurement and finally (c) the image after the GD breakdown measurement. It can be observed that the device failure consists in the fusion (burning) of the Gate metal. We believe that GaN semiconductor is not subjected to degradation.
Figure 5-7 reports the same characterization for QinetiQ PeterPan devices.

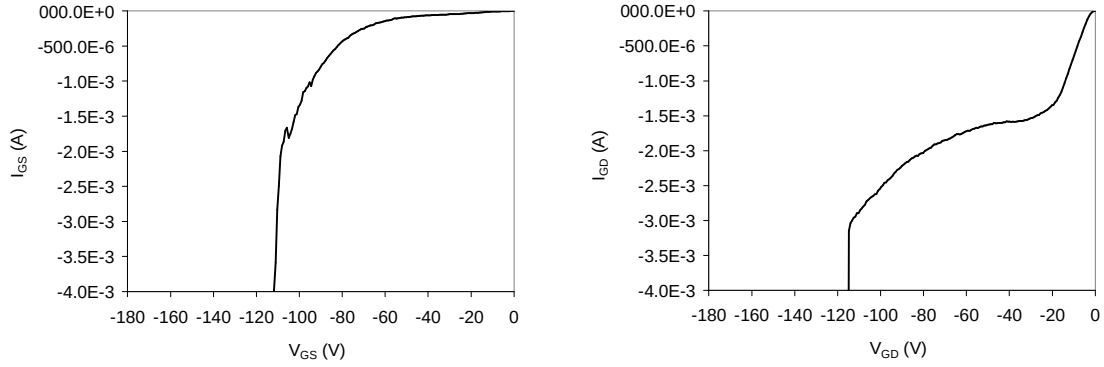




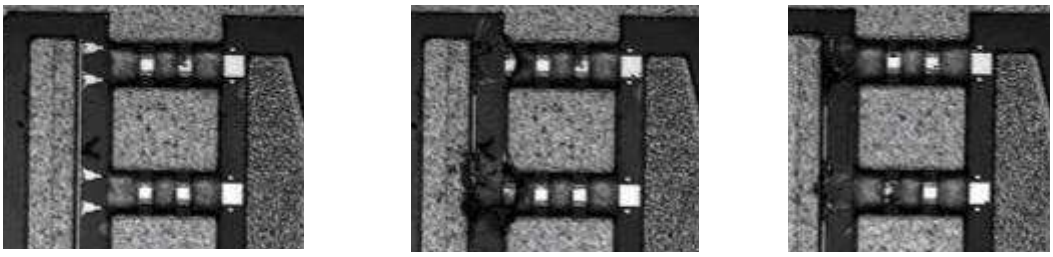
(c) Before Breakdown (d) After GS-Breakdown (e) After GD-Breakdown

Figure 5-7(a) Gate to source and (b) Gate to Drain breakdown measurement in PeterPan devices. Bottom figures refer to a virgin device (c), and to device after breakdown measurements (d,e).

In Figure 5-8 Selex SLX19 devices have been characterized in terms of breakdown after a thermal storage stress (300°C for 2000h).



(a) (b)



(c) Before Breakdown (d) After GS-Breakdown (e) After GD-Breakdown

Figure 5-8(a) Gate to source and (b) Gate to Drain breakdown measurement in SLX19 storage devices. Bottom figures refer to a virgin device (c), and to device after breakdown measurements (d,e).

1. Finally figures from Figure 5-9 to Figure 5-12 are reported the GD breakdown characterization for four different QinetiQ devices: Tinkerbell, Beast, PeterPan and Rhodes.

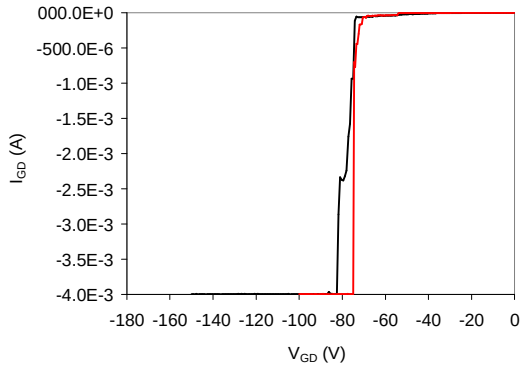


Figure 5-9 Gate-to-Drain two terminal Breakdown characterization for Tinkerbell devices.

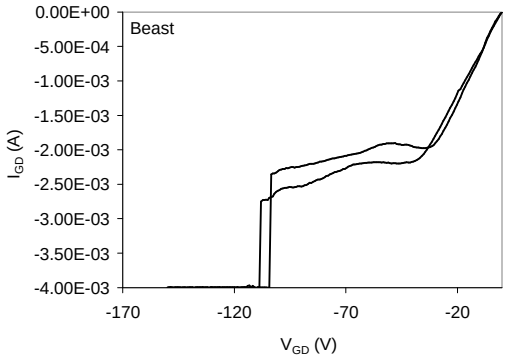


Figure 5-10 Gate-to-Drain two terminal Breakdown characterization for Beast devices.

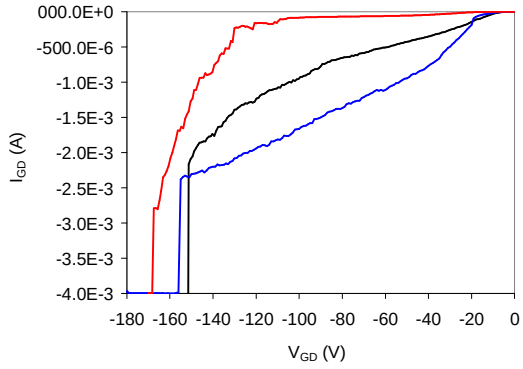


Figure 5-11 Gate-to-Drain two terminal Breakdown characterization for PeterPan devices.

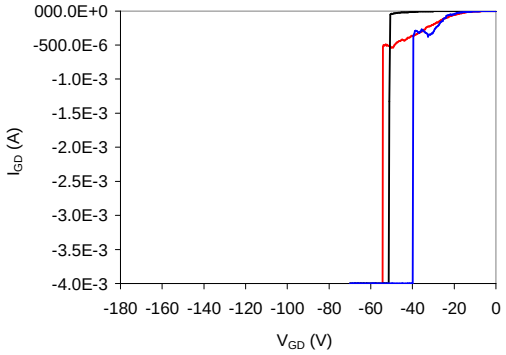


Figure 5-12 Gate-to-Drain two terminal Breakdown characterization for Rhodes devices.

Table 5-2 summarize the GD and GS two terminal breakdown measurements in all the tested devices.

Wafer	Sub.	Sub.Suppl.	Epitaxy	W (µm)	L (µm)	L_{GD} (µm)	L_{GS} (µm)	V_{BDGS}	V_{BDGD}
RHODES	SiC	Cree	QinetiQ	1000	-	-	-	-60	-55
PETER PAN	SiC	Cree	QinetiQ	1000	0.2	2.525	1.275	-100	-150
TINKERBELL	SiC	Norstel	QinetiQ	1000	0.2	2.525	1.275	-80	-80
BEAST	SiC	Cree	TRT	1000	0.2	2.525	1.275	-90	-110
SLX_25	SiC	Norstel	QinetiQ	1000	0.25	2.05	1.15	-45	-75
SLX_19storage	SiC	Norstel	Picogiga	1000	0.25	2.05	1.15	-110	-110

Table 5-2 Two terminal GD and GS Breakdown values on the tested devices.

The following consideration can be drawn:

- SLX25 present a very low breakdown value if compared to Tinkerbell devices that have the same substrate and epilayers.
- Peterpan has twice the breakdown voltage value of Tinkerbell. Both substrate and passivation layer can be responsible. The more "leaky" curves of the PeterPan devices, could suggest a strong influence of the passivation layer.

5.4 Pulsed breakdown characterization

5.4.1 Transmission Line Pulse set-up

Device behavior in high-voltage and high-current regimes was analyzed by means of a 100 ns Transmission Line Pulser. This is a common method used to generate square pulses of selectable duration and amplitude, based on the charging and discharging of the distributed capacitance of a transmission line. A schematic of the TLP system used is depicted in Figure 5-13.

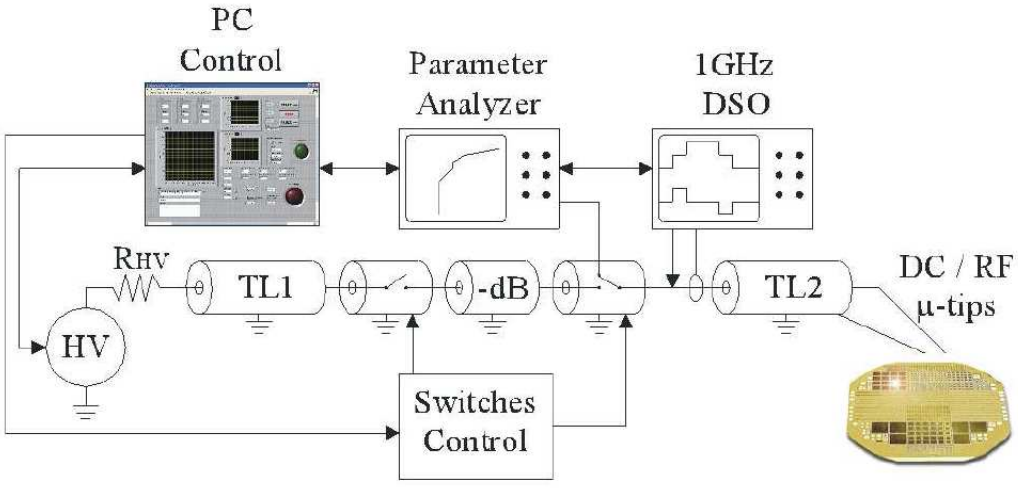


Figure 5-13 Schematic of the Time Domain Transmission TLP (overlapping waveforms).

For TLP-testing of integrated structures a high-voltage source is used to charge the distributed capacitance of the transmission line TL1 via a high-ohmic resistor, while the coaxial switch S1 is in open state. After the switch closes, the discharge of such

transmission line (TL1) into a resistive load (through TL2) produces a square pulse. The duration of the square pulse is equal to the length of the charged line divided by the velocity the signal propagates from the switch to the high-ohmic end of this line and back to the switch. As an example, 10m of the typical RG58 transmission line with a propagation velocity of 20 cm/ns generate a 100ns wide pulse. The amplitude of the voltage pulse V is determined by the pre-charge voltage V_0 and the voltage divider given by the impedances of the source Z_L and the load Z_S.
Based on the same philosophy, several kind of TLP systems can be made. Our setup is based on the Time Domain Reflectometer technique (TLP-TDR), with overlapping voltage and current waveforms. It is based on the fact that if an incident square pulse reaches the DUT at the end of a transmission line, it will be reflected depending on the impedance $Z_{DUT}(t)$ of the DUT relative to the impedance Z_0 of the transmission line:

$$V_{reflected}(t) = \frac{Z_{DUT}(t - t_{delay}) - Z_0}{Z_{DUT}(t - t_{delay}) + Z_0} \cdot V_{incident}(t - t_{delay})$$

This setup maintains the 50 Ω impedance from the generator to the device with minimum parasitic elements and pulse distortion. Figure 5-14 shows a detail of the behavior of the waveforms incident to and reflected from the DUT.

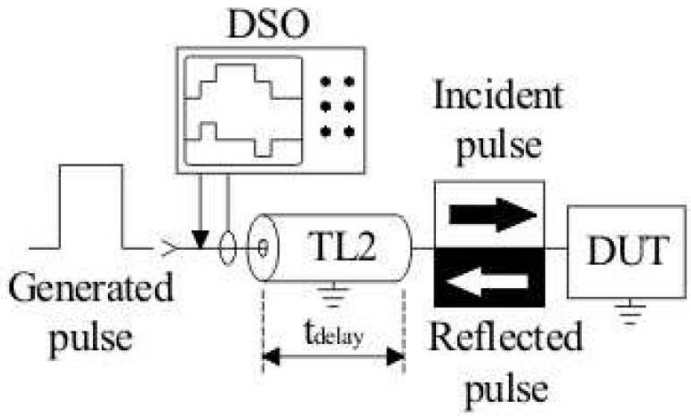


Figure 5-14 Detail of the behaviour of the waveforms incident to and reflected from the DUT (overlapping waveforms).

An example of the voltage waveforms at increasing pre-charge voltage values obtained with the TLP-TDR (overlapping) is reported in Figure 5-15.

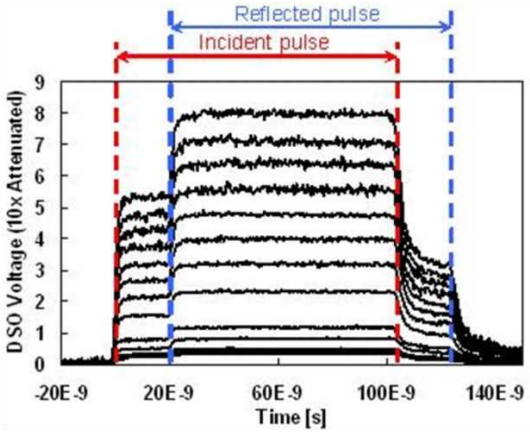


Figure 5-15 Voltage waveforms obtained with our setup at increasing pre-charge voltage values.

Increasing step by step the pre-charge voltage of the high voltage supply, it is possible to investigate the full I-V behavior of the DUT in a semi-static way.
In order to better investigate the behaviour of HEMT devices during the TLP tests, we have improved our traditional setup. The TLP system has been equipped with "ad-hoc" developed relays, in order to carry out a complete electrical DC characterization, and in particular the I-V measurement of the Gate-Source diode after each TLP pulse. In this way, by changing the circuit topology, the DC parameter analyzer is isolated from the TLP system and vice versa. These relays have been developed with a 50 Ω-matched layout on a PCB and characterized by means of a Vector Network Analyzer; optimum RF performances (very low insertion loss) have been achieved up to 3 GHz. The schematic of the modified TLP system and a photo of the developed relays mounted on the rf-tips is shown in Figure 5-16.

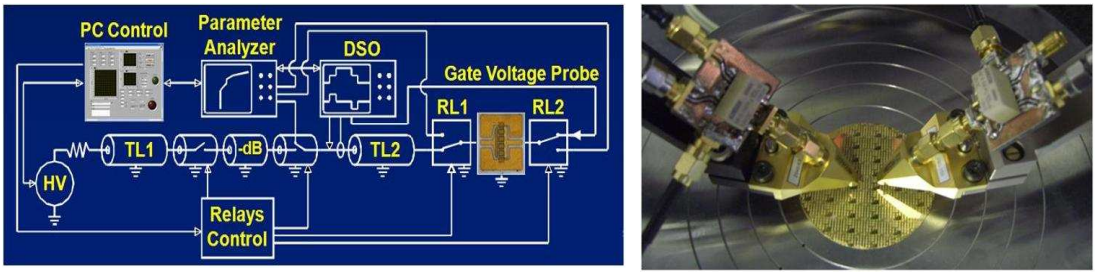


Figure 5-16 Schematic of the modified TLP system (left), and photo of the developed relays mounted on the rf-tips (right).

5.4.2 Three terminal pulsed breakdown characterization

The three terminal breakdown measurements have been carried out by biasing the Gate at a fixed voltage and pulsing the drain with with increasing amplitude. Drain current and voltage waveforms are then recorded at each pulse (as previously described) creating in this way the I-V curve. The pulses applied to the Drain have been increased up to the device breakdown. In Figure 5-17 we report the complete I-V characteristic (up to the breakdown) for a QinetiQ PeterPan device. It must be noted that eight devices were required for this measurement, since at the breakdown the device present a catastrophic failure (Drain-to-Source short circuit).
An important feature of this breakdown characterization is related to the dependence of the breakdown voltage as a function of the Gate voltage: the breakdown voltage increases as far as the Gate voltage decreases. As shown in Figure 5-17, the breakdown voltages change from about V_{DS} = 80 V in open-channel condition (V_{GS} = 0 V, -1 V) increasing up to 260 V near to the pinch-off (V_{GS} = -7 V). This trend can suggest that power dissipation and/or current density is playing an important role in determining the breakdown voltage. Iso-power curves are also depicted on Figure 5-17 and it can be observed however that the breakdown is not determined only by power dissipation.
This result clearly suggests that the observed device breakdown is not driven by the Gate-to-Drain electric field, since, in this case, a decreasing of the breakdown voltage should be observed at decreasing of the Gate voltage (Gate-to-Drain voltage increases at decreasing of V_{GS}). A combined mechanisms involving power dissipation, current density and electric field could be responsible of the observed results.
In Figure 5-18 we report the same three terminal breakdown measurements in a QinetiQ Rhodes device. The two following main observation can be drawn:

a) The breakdown value is much lower that the PeterPan devices, in line with the two terminal breakdown characterization;

b) Again the breakdown value increase at decreasing the gate voltage.

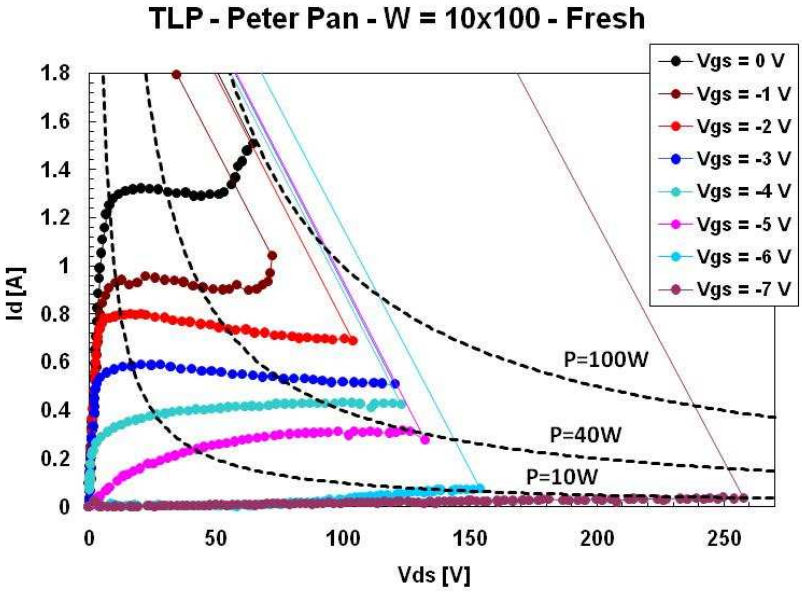


Figure 5-17 Three terminal pulsed (TLP) characterization in a QinetiQ PeterPan device.

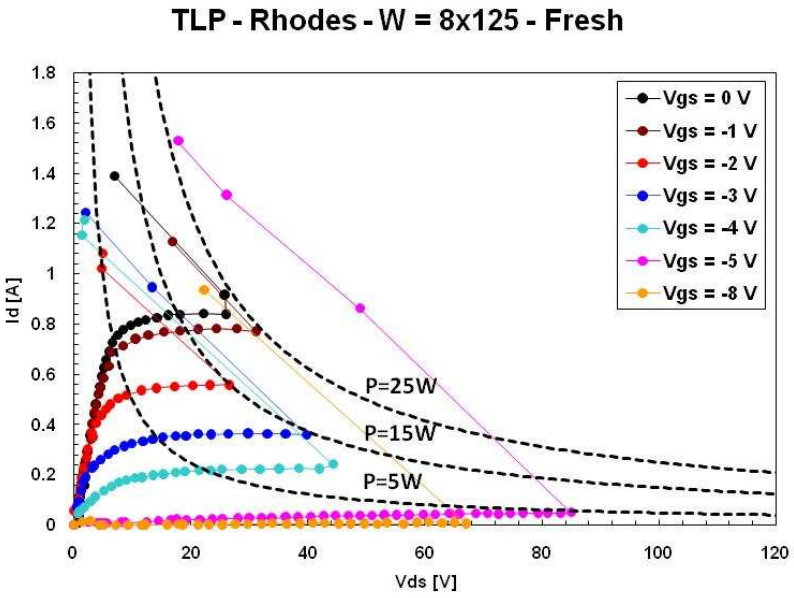


Figure 5-18 Three terminal pulsed (TLP) characterization in a QinetiQ Rhodes device.

Three terminal breakdown measurements have been carried out also on Selex-SI devices. In Figure 5-19 and Figure 5-20 we report the breakdown characterization in a Selex SLX25 device respectively for a 1.2 mm and a 1.0 mm periphery device.

The Main difference observed in these devices is the dependence of the breakdown voltage as a function of the Gate voltage. On these we did not observe a clear trend of the breakdown voltage with the Gate bias. The different breakdown values observed can be due to device variability.

However, it could be speculated that in these devices the breakdown decrease at decreasing the Gate voltage (consider V_{GS} = 0, -1, -3 and -5 V in Figure 5-19, and V_{GS}= 0, -1, -2, -6, and -8 V in Figure 5-20). In this case the breakdown could be related to the Gate-to-Drain electric field and not to any phenomena related to power dissipation and or current density.

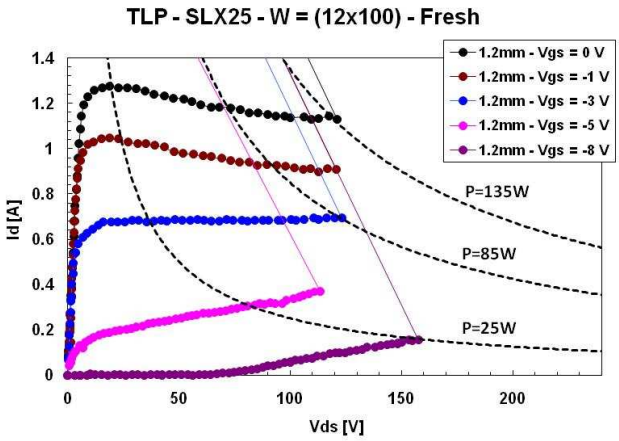


Figure 5-19 Three terminal pulsed (TLP) characterization in a SELEX-SI SLX25 device (W=1.2 mm).

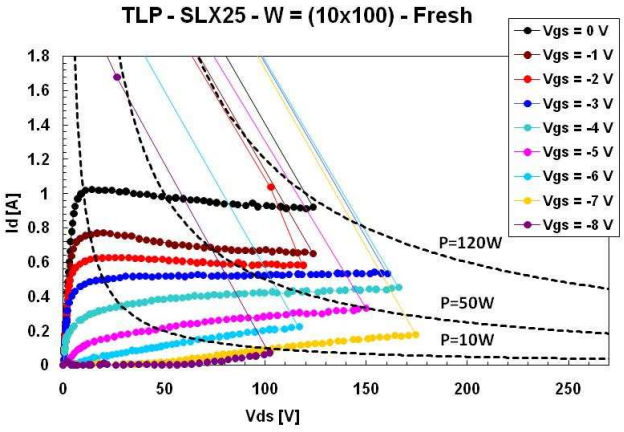


Figure 5-20 Three terminal pulsed (TLP) characterization in a SELEX-SI SLX25 device (W=1.0 mm).

5.4.3 Failure analysis after breakdown

Devices after breakdown characterization present a catastrophic damage that is generally represented by a Drain-to-Source short circuit. We have continuously monitored a SLX15 devices submitted to the breakdown characterization by means of optical and emission microscopy investigation.

It has been observed that the catastrophic failure of the GaN HEMT is mainly related to a Drain-to-Source filamentation formation due to metal fusion (see Figure 5-21). This failure mechanism is the most common event observed in the studied devices during the breakdown characterization. This metal fusion phenomena is strongly related to the metallization, geometry of the access region and to the device surface properties (passivation, recess profile, …).

Another important feature often observed in the studied devices is the appearance of a more limited (in area) damage of the Gate area of the devices, preceding the catastrophic failure (see damaged area at the centre of the bottom figure). This failure mechanisms is different frm the previous one and it can be possibly related to the damage of the crystal lattice of the GaN and / or AlGaN layers. This damage is likely to appear in correspondence of a previously present defect (dislocation).

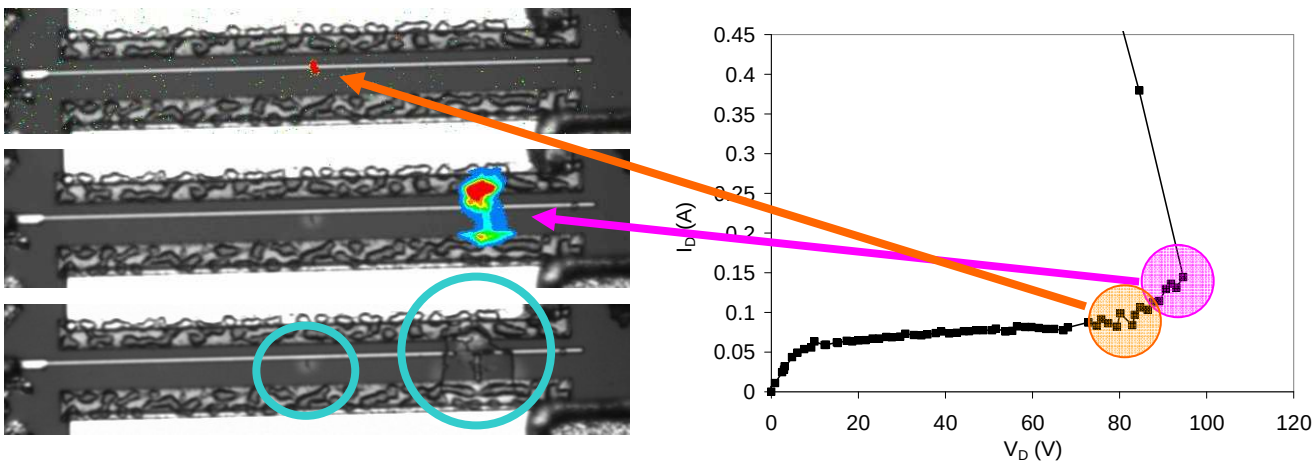


Figure 5-21 Optical and Emission Microscopy investigation after breakdown characterization in a SLX15 SELEX-SI device.

5.5 ESD sensitivity characterization

We have used a 100ns TDR-TLP system in order to test the ESD robustness of HEMT devices in two different configurations:
(a) positive voltage pulses applied to the Drain, with Source grounded, and Gate floating;
(b) positive voltage pulses applied to the Gate, with Source grounded, and Drain floating.
In this paper we will focus mainly on the study of the first configuration. Complete DC electrical characterization has been carried out with an HP 4142 parameter analyzer in order to investigate the DUT degradation, if any, at selected step during TLP stress.
During Drain to Source stress Drain current and voltage were monitored during the TLP stress; a 10MΩ probe, with low parasitic capacitance, was used to measure the Gate voltage waveform. We verified that the presence of the relays and the voltage probe do not affect the behaviour of the device submitted to test, nor alter results.
Emission based failure analysis has been carried out using a Hamamatsu PHEMOS-200 light emission microscope, equipped with a water-cooled CCD camera, in order to make measurements at -50°C to reduce the noise.

5.5.1 ESD Drain to Source TLP stress

The first configuration we have studied has been the TLP stress applied to the Drain, with Source grounded, and Gate floating. We think this case could be the most critical for the device, because it affects the whole device structure, and it could be a typical ESD event during device manufacturing or manipulation.
Figure 5-22 shows the IV-TLP curve of a HEMT device (W = 1mm) stressed in this configuration. Being the conductive channel already formed (the Gate is floating),

the device exhibits a typical $I_{DS}(V_{DS})$ transistor curve, until it reaches the snapback point (V_{DS} suddenly decreases with the increase of the I_{DS} at around 85V, 1.2A). In the first stage, we tried to use the traditional leakage current measurement used in TLP systems as failure criterion [13]. The leakage current measurement consists in the measure of the current flowing between the two tested pads (Drain vs. Source in this case) at a fixed voltage after each TLP pulse. Since the studied devices are normally on, a large current flows from the Drain to Source in this configuration. Hence, we measured the standard Drain to Source TLP leakage current at a low V_{DS} value (10mV), as reported in Figure 5-22. As it is possible to see in the Figure, this criterion (open diamonds) doesn't reveal any device degradation. In fact, the I_{DS} current remains practically unchanged even after the device failure.

In order to study which electrical parameters (if any) degrade during TLP stress, we have then made a complete DC electrical characterization at selected TLP steps. We have carried out the following measurements: the Gate-Source diode characterization, Output characteristics in on-state and in sub-threshold regime, trans-conductance, and trans-characteristics curves.

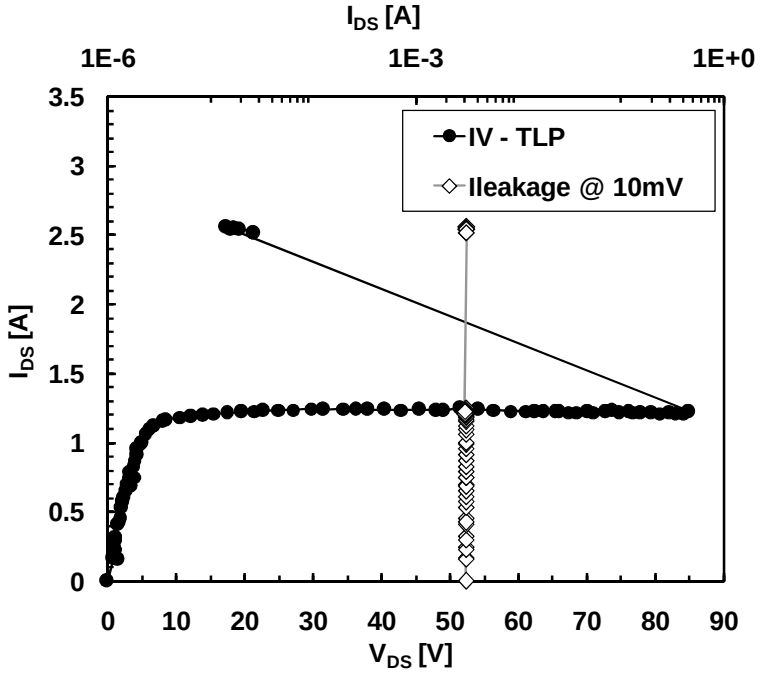


Figure 5-22 IV-TLP curve of a W=1mm HEMT stressed between Drain and Source, Gate floating. Ids measurements are reported with open diamonds, but they don't give any indication on the device degradation.

In Figure 5-23a), b), and 3) we report the comparison between the Output characteristics (I_{DS}-V_{DS}), the trans-conductance measurements (g_m), and the sub-

threshold current curves ($I_{D\text{-}SUB}$) of the W=1mm HEMT device previously reported in Figure 5-22, in its untreated device, and just before the failure. As shown in Figure 5-23a), b), characteristics exhibit practically no variation. In fact, we don't observe any threshold voltage shift, or significant series resistance increase, or decrease of the gain factor. On the contrary, as depicted in Figure 5-23 c), the $I_{D\text{-}SUB}$ exhibits an appreciable change at V_{GS} lower than -6V. This behaviour is typically symptomatic of the degradation of the Gate-Source and Gate-Drain Schottky diodes.

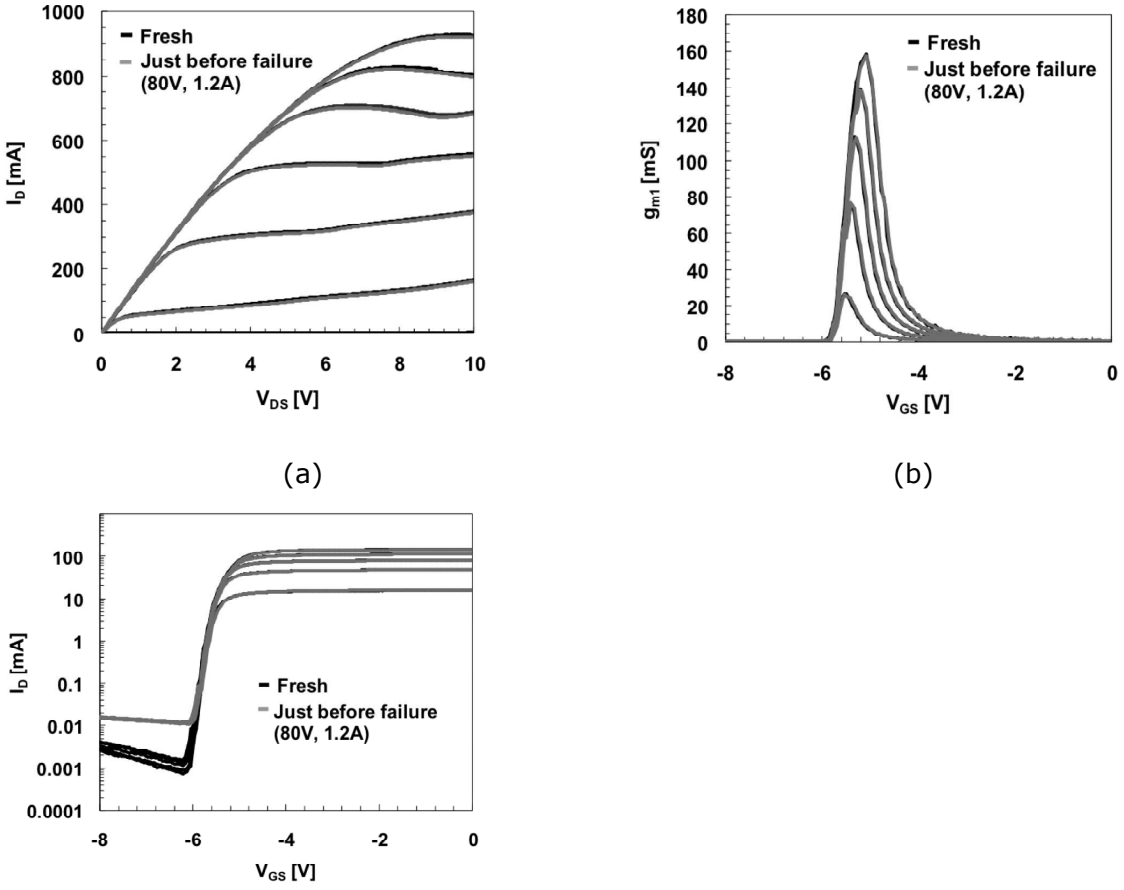


Figure 5-23 DC electrical characterizations of a HEMT device with W_G=1mm, L_G=0.5mm before and after a TLP stress. a) Output characteristics (Gate bias: -8V ≤ V_{GS} ≤ 0V, step 1V); b) Transconductance curves (Drain bias: 0.1V ≤ VDS ≤ 0.9V, step 0.2V); c) Subthreshold I_D, I_{D_SUB}, (Drain bias: 0.1V ≤ VDS ≤ 0.9V, step 0.2V).

In Figure 5-24 the evolutions of selected electrical parameters of the same W=1mm HEMT device (IV-TLP reported in Figure 5-22) during the TLP stress are shown. Parameters are: I_{DSAT} (V_{GS}=0V, V_{DS}=10V), $I_{D\text{-}SUB}$ (V_{GS}=-8V, V_{DS}=0.1V), and g_m peak (V_{DS}=0.1V), extracted at $V_{DS\text{-}TLP}$=0V (untreated), 30V, 50V, 80V, and after the failure. As it can be seen, all the investigated parameters remain practically unchanged, up to the V_{DS} value which induces the device failure.

The Gate-Source Schottky diode exhibits a heavy degradation during the TLP stress. Thank to this result, we have then decided to monitor the behaviour of the I_{GS}-V_{GS} curve (with V_{GS} varying from -2V up to 2V, limiting the current at 100mA, in order to not overstress the devices during the DC measurement) at each TLP stress.

Figure 5-25 the IV-TLP characteristic of a W=400mm device, using the I_{GS} current (measured at V_{GS} = -2V) as a failure criterion, is reported. As it is possible to notice, the I_{GS} indicates the device degradation during the TLP stress even before the snapback condition.

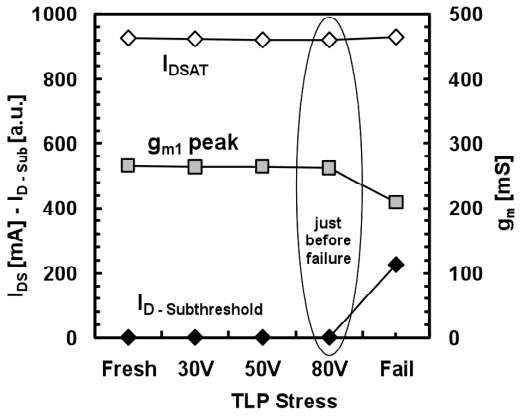


Figure 5-24 I_{DSAT} (V_{GS}=0V, V_{DS}=10V), $I_{D\text{-}SUB}$ (V_{GS}=-8V, V_{DS}=0.1V), and g_m peak (V_{DS}=0.1V) measured at selected step during the TLP stress. Measurements refer to the W=1mm HEMT device reported in Figure 5-22 and Figure 5-23. Electrical parameters exhibit substantial changes only after the failure has occurred. $I_{D\text{-}SUB}$ measurements have been multiplied by a factor of 100.

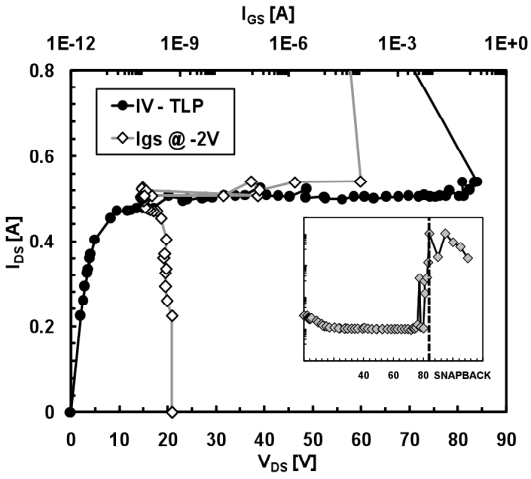


Figure 5-25 IV-TLP curve of a W=400mm HEMT stressed between Drain and Source, Gate floating. The I_{GS} measurement (at V_{GS} = -2V) after each TLP stress (open diamonds) gives indication on the device degradation even before the snapback point. The insert shows the evolution of the IGS current up to the snapback points.

The full evolution of the Gate-Source Schottky diode I_{GS}-V_{GS} is reported in Figure 5-26. Below 75V it doesn't exhibit any change, while after TLP stress larger than

75V at V_{DS}, the I_{GS} current starts to degrade. After the failure, in fact, the Gate-Source diode behaves like an ohmic contact.

The impact of the device width (W) on the ESD robustness was studied using devices with different dimension: W=100mm, 400mm, 1mm, 1.2mm, and 2.4mm. Figure 5-27 reports the comparison of the IV-TLP curves of devices with different width. All devices presents the failure between 80V to 110V.

As depicted in Figure 5-28, a very good scaling of the failure current has been observed with the device width.

The robustness scaling is not so obvious in GaN based devices. In fact, despite the already formed conducting channel, the presence of defects and dislocations in the material, as asserted in the introduction, could affect the uniform current distribution along the device width. This, in turn, could not give any scaling of the failure current.

In Figure 5-29 we report typical TDR-TLP voltage and current waveforms in the instant in which the failure occurs (see the point A in Figure 5-27). All tested devices have exhibited abrupt failures, with only a small deviation from the rectangular shape, caused by self-heating effects, before the failure.

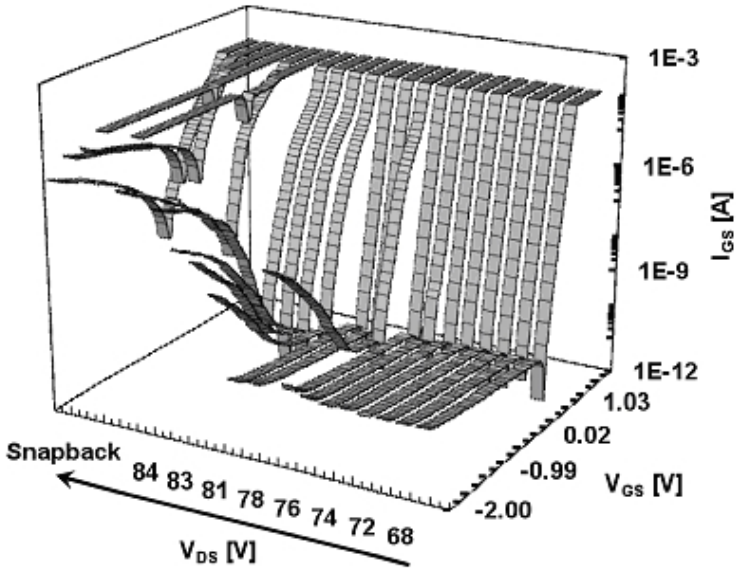


Figure 5-26 Evolution of the Gate-Source Schottky diode degradation during the TLP stress of the W=400μm depicted in Figure 5-25. I_{GS} has been measured at -2V ≤ V_{GS} ≤ 2V, with a 100μA compliance level. The arrow indicates the TLP evolution.

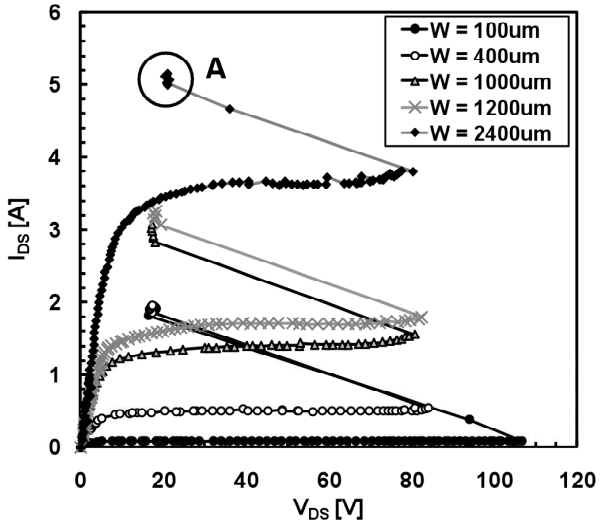


Figure 5-27 I_{DS} vs V_{DS} pulsed curves obtained pulsing the Drain vs. the Source (keeping the Gate floating) with the TLP pulser. Devices have widths starting from 100um up to 2400um.

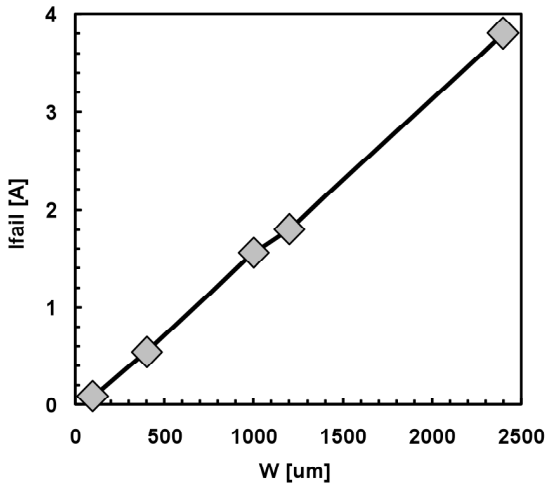


Figure 5-28 Optimum linear scaling of the failure current as a function of the device width of HEMT devices stressed between Drain and Source, Gate floating.

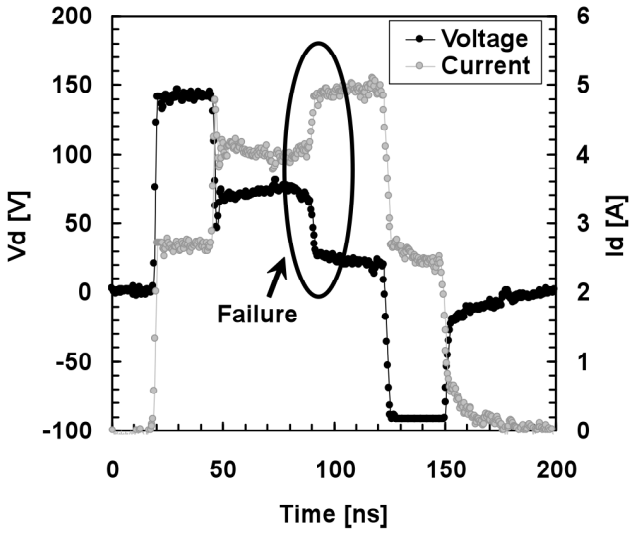


Figure 5-29: Typical abrupt impedance change shown by the voltage and current waveforms of the TLP when the failure point is reached (point A of Figure 5-27). The figure refers to the failure of the W=2.4mm device.

5.5.2 ESD Gate to Source TLP stress

Results from the TLP stress at the Gate with the Source grounded, and the Drain floating are reported in Figure 5-30. The inset demonstrates that even in this case a good scaling of the ESD robustness with the device width is observed up to a W=1.2mm. All 2.4mm tested devices deviate in the same way from the linear trend, sustaining a current of around 2A, suggesting that a Gate-metal fusion could be a possible explanation. In fact, it is possible to notice that the I-V curves exhibit the typical behaviour of a diode, biased in a very high forward current regime. The series resistance depends, as expected, on the width of the stressed devices. For high current values, the I-V curves tend to saturate, indicating the inability of the metal lines to bring the current.

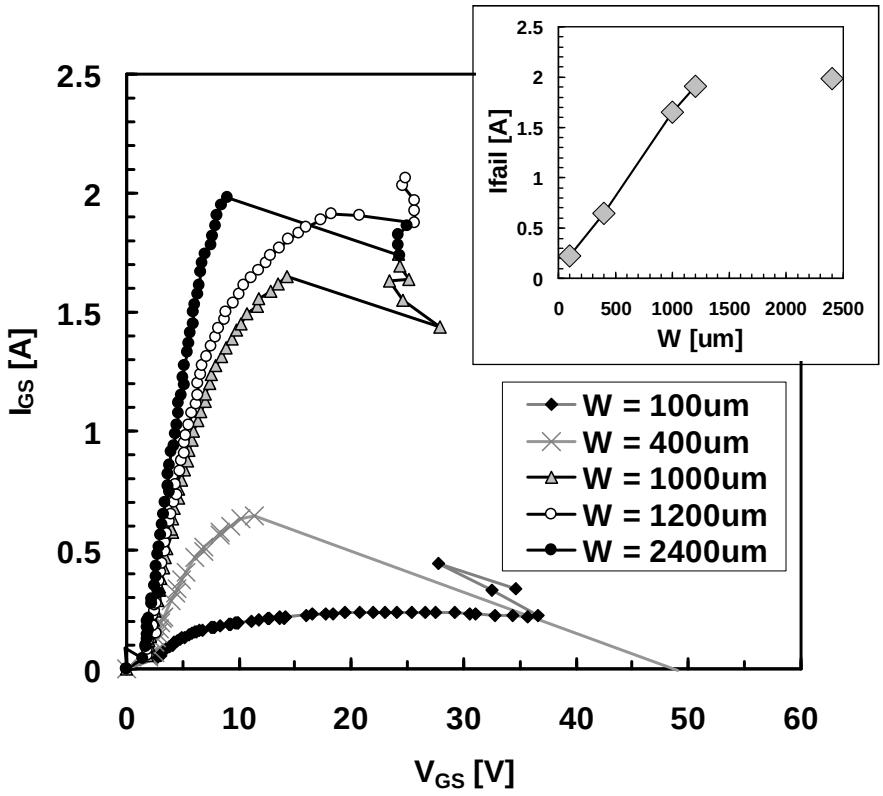


Figure 5-30 Gate vs Source (Drain floating) IV-TLP comparison of devices, with a width starting from 100um up to 2400um. The inset shows the optimum scaling with the device width of the failure current, with the exception of all 2.4mm tested devices.

5.5.3 ESD failure analysis

We have shown that applying the TLP stress to the Drain, with Source grounded, and Gate floating, a critical degradation of the Gate Schottky diode is observed, as previously reported in Figure 5-26. In order to explain this result we have studied the capacitive coupling between the Drain, Gate, and Source contacts during the TLP events.

Figure 5-31 shows a schematic representation of the parasitic capacitors between Gate and Drain (C_{GD}), and between Gate and Source (C_{GS}), and the intrinsic Gate-Drain and Gate-Source Schottky diodes. Using our extended TLP system, monitoring the Gate voltage during the TLP stress applied to the Drain, with the Gate floating, we have measured (relatively) high voltage values at the Gate contact. In fact, due to the fast rise time of the TLP system (below 1ns), the floating Gate can easily follow the Drain voltage, reaching high voltage values.

Figure 5-32 shows the increase of the floating Gate voltage with the increase of the V_{DS} applied by the TLP stress. Each point has been extracted making an average of the end part of the V_{GS} waveform, like traditional voltage and current values extraction.

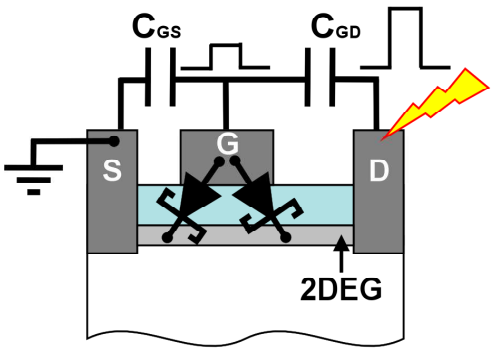


Figure 5-31 Schematic representation of the capacitive coupling between Drain-Gate-Source contacts and the intrinsic Gate-Drain and Gate-Source Schottky diodes.

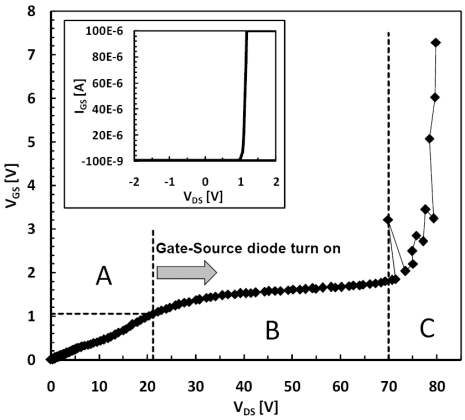


Figure 5-32 Coupled Gate voltage evolution as a function of the V_{DS} applied with the TLP system (TLP stress between Drain and Source, Gate floating). In the inset a typical IV characteristic of the Gate-Source diode is reported, exhibiting a V_{TH} voltage of around 1V. Device width W=1mm.

As shown in Figure 5-32, the behavior of the Gate voltage coupling can be divided in three different zones (indicated by A, B, and C). In the first zone, the V_{GS} increases practically in a linear way with the increase of the V_{DS} applied by the TLP system. When the V_{GS} reaches about 1V, the Gate-Source diode turns on (see the inset in Figure 5-32), draining a part of the current used to charge the capacitor divider C_{GD}-C_{GS}, and then reducing the voltage reached by the Gate. This condition is indicated by the change of slope in the zone B of Figure 5-32. In the zone (C) another failure occurs. Region (C) can possibly correspond to the formation of filaments between the Gate and Drain regions, bringing to an abrupt increase of the Gate voltage at every TLP pulse.

The main effect of the Gate-Source diode degradation is the Gate inability to pinch-off the channel, as reported in Figure 5-33. In fact, beyond some differences in the I-V curves for $-2V \leq V_{GS} \leq 0V$, all other curves are overlapped but very different from before the stress, meaning that the device is no more able to sustain an electric field sufficient to deplete the active region and pinch-off the channel. Other defects created along the TLP stress, either superficial or in the interface AlGaN/GaN, could also explain the change of the series resistance in the IV curves.

The filament formation can be confirmed by different optical and emission-based measurements. In Figure 5-34, emission images of a W=100mm device during the Drain vs Source, Gate floating, TLP stress is reported. The emission images are obtained biasing in DC regime the device, at V_{GD} = -6V, leaving the Source floating, and with an integration time of 30s. In the same Figure it is possible to see the formation and the evolution of light-spots on the edge of the Gate on the Drain side. The device didn't show any emission when untreated and biased in the same conditions. Spot emissions start to appear when V_{DS} is greater than 60V, increasing their size and number during the TLP stress up to the failure. The spatial position of emission spots remains quite unchanged.

Another confirmation is given by the emission images taken during the TLP stress. In fact, we have acquired an emission image at each TLP pulse, and no emission was seen just before the failure point. On the contrary, as shown in Figure 5-35, when the IV curve exhibits the transition to low impedance, a big spot appears where eventually a filament is found. The last confirm is simply given by the photo, taken with a 1000X magnification factor, shown in Figure 5-36. The highlighted region actually shows the filament between the Drain and the Gate region. Furthermore, successive TLP-emission measurements carried out after the failure haven't exhibited any light emission, because of the filament was already formed.

The same Figure also shows a burn of the Gate finger. This was due to successive DC measurements performed to study the electrical behavior of the tested device, but wasn't caused by the TLP stress.

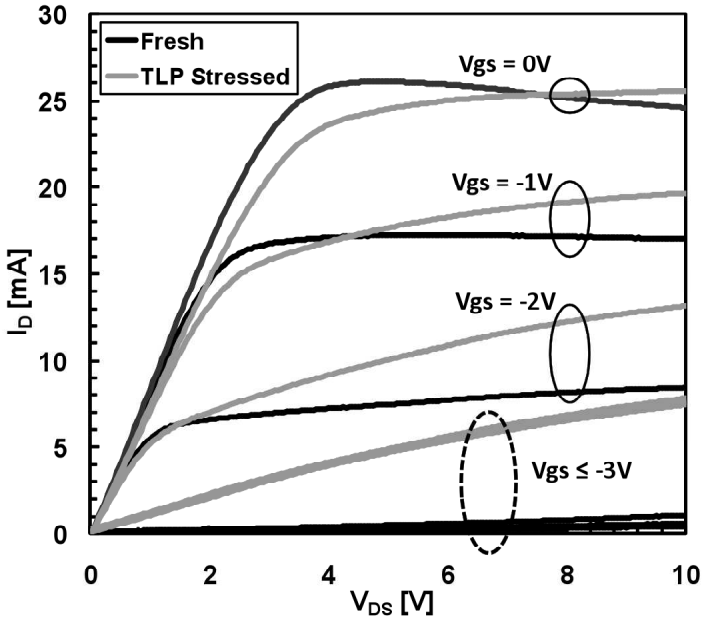


Figure 5-33 Comparison of the I_{DS}-V_{DS} characteristics between a fresh and a TLP stressed devices. Gate bias: -6V ≤ V_{GS} ≤ 0V, step 1V. The stressed device is no more able to pinch-off the channel (highlighted by the dotted oval).

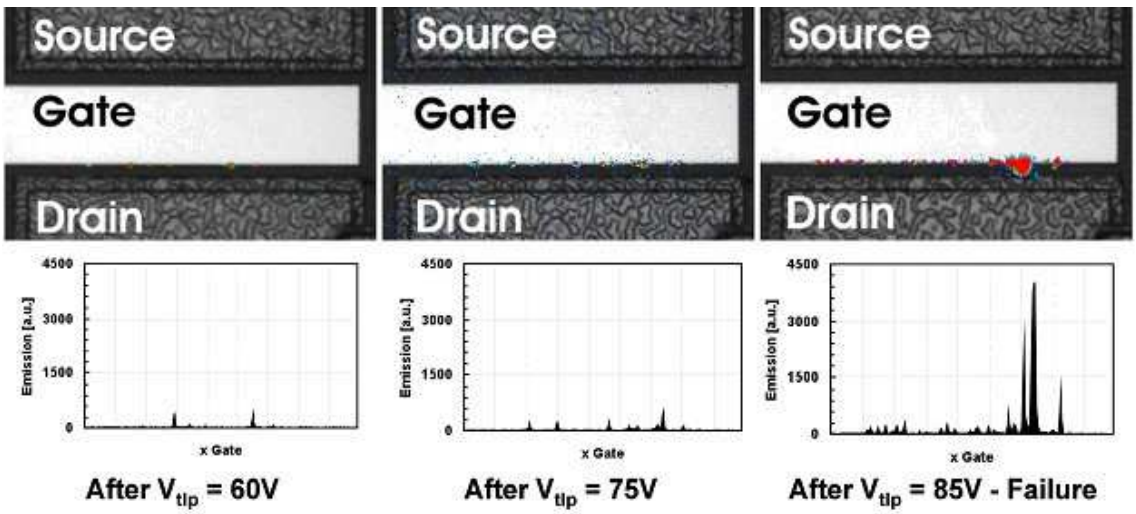


Figure 5-34 Emission images of the HEMT stressed device obtained by DC step biasing after selected TLP stress. Bias conditions: V_{GD}=-6V, Source floating, Integration time = 30s.

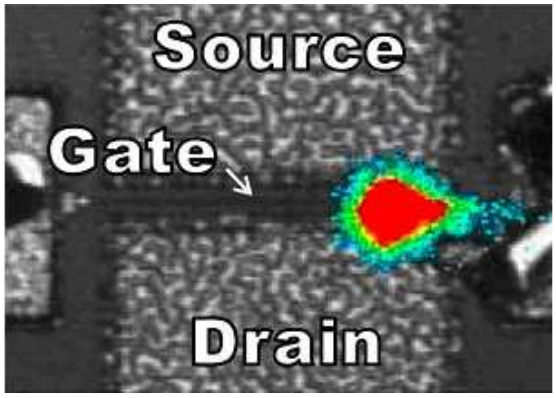


Figure 5-35. Sparkling emission during the destructive TLP pulse.

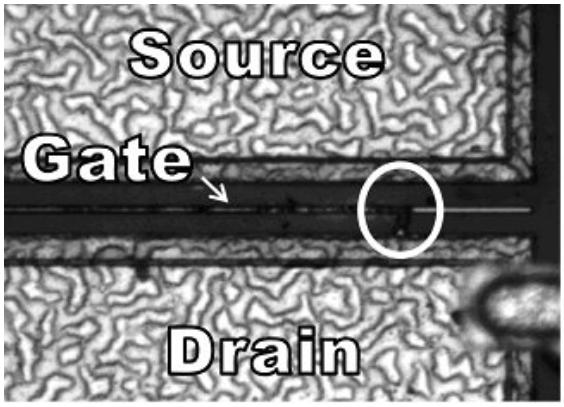


Figure 5-36: Typical filament, created between Drain and Gate regions, is highlighted in the circled zone. The burn of the gate finger was caused by successive DC measurements.

Regarding the Gate to Source TLP configuration (previously shown in Figure 5-30), we observed a completely different failure mode, due to the high-current condition reached by the Gate metal line during the TLP stress. IV curves and optical inspections suggest that a Gate metal-line fusion could be a possible explanation. In Figure 5-37 we report a photo taken with a metallographic microscope exhibiting the complete destruction of the Gate finger after the TLP stress.

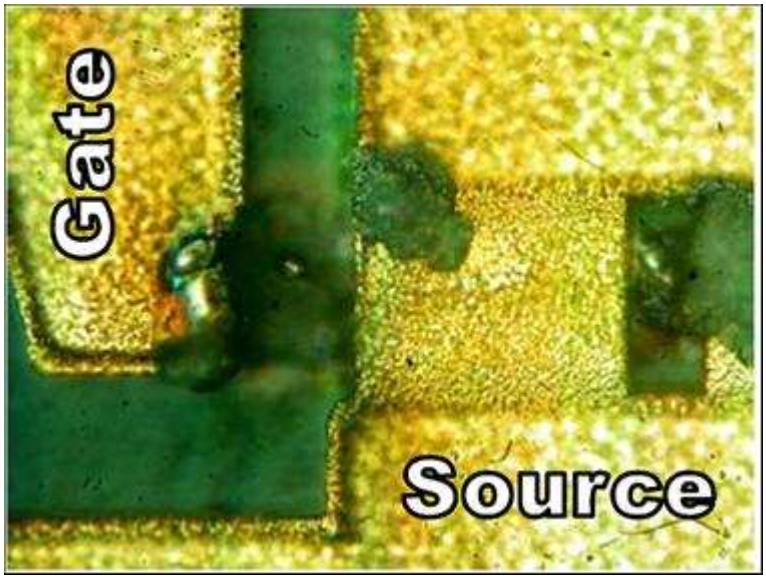


Figure 5-37: Metallographic microscope picture of a W=1mm HEMT stressed between the Gate and the Source. A complete destruction of the Gate finger is occurred, and also the Source bridge appears damaged.

5.5.4 Human Body Model characterization

We have started the investigation of the sensitivity of GaN HEMT devices in according to the Human Body Model (HBM). The HBM is the traditional ESD testing standard, originally defined in the MILSTD-883x method 3015.7. This standard defines the current waveform for the discharge of a 100 pF capacitor through a 1.5 kΩ resistor and a 0Ω load for different discharge voltages. In Figure 5-38 the schematic of the HBM test circuit is reported.

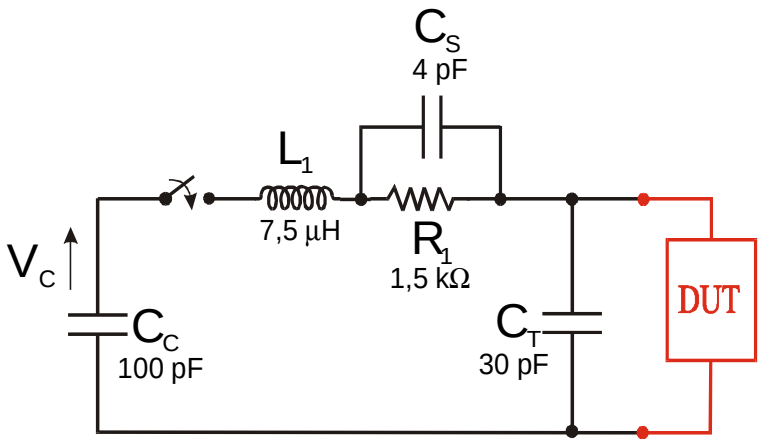


Figure 5-38: Human Body Model test circuit.

We have developed a HBM-like tester on wafer level, with the ability of recording both voltage and current waveforms. Preliminary results on the HBM stress performed at pre-charging voltage of 600, 800, 1000, and 1100V on a SLX15 Gated-TLM with L_G=20µm are shown in Figure 5-39 (voltage waveforms on right, current waveforms on left). It is possible to notice that the device fails at a pre-charge voltage of 1100V.

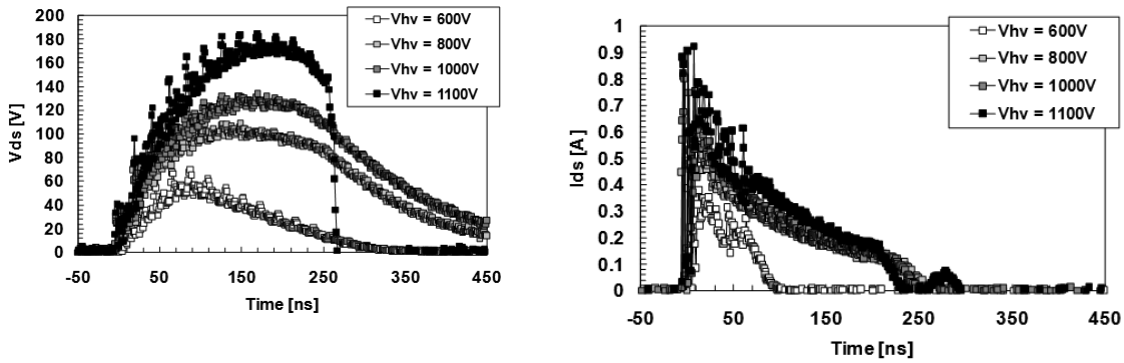


Figure 5-39: Voltage and current waveforms of the SLX15 Gated-TLM with L_G=20µm device stressed in according with the Human Body Model.

Preliminary failure analysis investigations have been performed by means of E-SEM technique. Like during TLP stress, filaments formation, fusion of metallization, and explosion of the passivation layer have been the most evident effects of the HBM stress. E-SEM photos of the damaged device are shown in Figure 5-40.

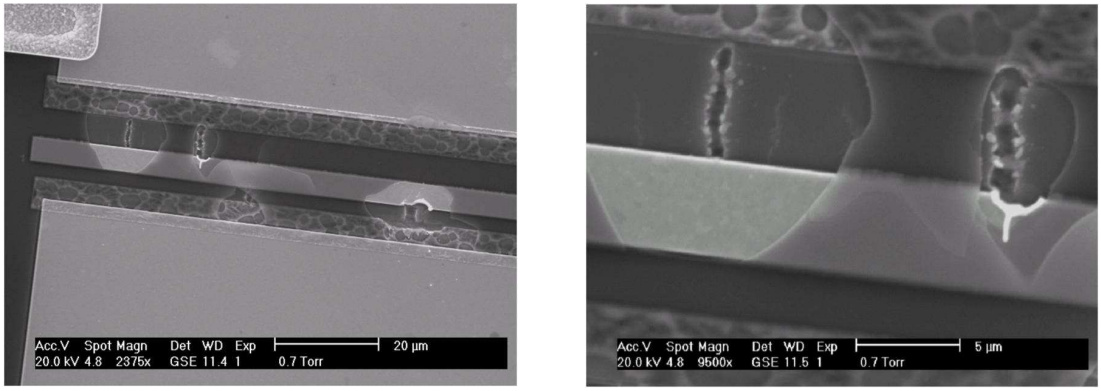


Figure 5-40: E-SEM images of the HBM stressed device.

5.6 Conclusion

ESD and EOS events are very important for GaN HEMT devices. ESD events have a strong influence on electrical characteristics and impair the reliability of the devices by high electric field and high temperature. Breakdown voltages in some devices are strongly dependent on gate bias, while in other devices the breakdown is almost independent from the gate bias. Failure analysis revealed that two main failure mechanisms following the destructive breakdown characterization are

present: GaN-lattice degradation (possibly related to a pre-existing crystal defect) and metal filamentation due to metal fusion.

Eventually we have also submitted the devices to Electrostatic Discharge evaluation using TLP and the HBM model. A strong capacitive coupling between the Drain, Gate, and Source terminals is present, impairing the reliability of the Gate-Source Schottky diode. The electrical parameter that can predict the device failure was found to be the I_{GS}. We observed a completely different failure mode in Gate-Source TLP stress involving Gate metal line fusion.

5.7 References

[1] C. Canali, A. Paccagnella, P. Pisoni, C. Tedesco, P. Telaroli and E. Zanoni, "Impact ionization phenomena in AlGaAs/GaAs HEMTs", IEEE Trans. on Electron Devices, vol. 38 (11), pp. 2571-2573, 1991.

[2] D. Dieci, G. Sozzi, R. Menozzi, E. Tediosi, C. Lanzieri, and C. Canali, "Electric-Field-Related Reliability of AlGaAs/GaAs Power HFETs: Bias Dependance and Correlation With Breakdown", IEEE Trans. on Electron Device, vol.48 (9), pp. 1929-1937, 2001.

[3] A.G. Chynoweth, Phys. Rev., 109, pp.1537-1540, 1958,

[4] K. Hui, et al. , IEEE Electron Device Lett., 11, pp.113-115, 1990.

[5] G. Meneghesso et al. IEEE Transd.on El. Devices, Vol.47, No.1, pp. 2-10, 2000.

[6] B. Brar et al. IEEE Lester Eastman Conference on High Performance Devices, pp. 487-491, 2002.

[7] T. Nakao, Y. Ohno, M. Akita, S. Kishimoto, K. Maezawa, and T. Mizutani, "Electroluminescence in AlGaN/GaN High Electron Mobility Transistors under High Bias Voltage", Jpn. J. Appl. Phy., vol.41 (1), pp.1990-1991, 2002.

[8] N. Shigekawa, K. Shiojima, T. Suemitsu, "Electroluminescence characterization of AIGaN/GaN High Electron Mobility Transistors", Appl. Phys. Lett., vol. 72 (8), pp. 1196-1198, 2001

[9] N. Shigekawa, K. Shiojima , T. Suemitsu "Optical Study ofhigh-biased AIGaNiGaN high-electron-mobility-transistors", J. Appl. Phys, vol. 92 (1), pp.531-535, 2002.

[10] A. Amerasekera, C. Duvvury, "ESD in Silicon Integrated Circuits", 2nd Edition, Chichester, England: John Wiley and Sons, 2002.

[11] J. Kuzmik, et al., "EOS in AlGan/Gan HEMTS: study of degradation processes", Solid State Electronics, n. 48, 2004, pp. 271-276.

[12] J. Kuzmik, et al., "Electrostatic discharge effects in AlGaN/GaN high-electron-mobility transistors", Appl. Phys. Lett., Vol. 83, No. 22, 1 December 2003, pp. 4655-4657.

[13] A. Amerasekera, C. Duvvury, "ESD in Silicon Integrated Circuits", 2nd Edition, Chichester, England: John Wiley and Sons, 2002.

6. Conclusion

A study of long term reliability has been performed on AEC1148 wafer in order to study the influence of different bias point on HEMT degradation. Devices stressed in "ON-state" show a large degradation of the output I-V characteristics which is not reflected in other curves; we can attribute this phenomena to negative charge trapping generating a large reduction of the drain current at low $V_{DS.}$ Devices tested in "SEMI_ON state" show a strong degradation of the output I-V characteristics: large degradation of the Schottky gate contact, of the drain current and in the sub-threshold current. In this case generation of new traps is not the main degradation mechanisms. In "OFF-state" devices show a degradation that in general is intermediate between the one observed in the other two bias point. Short term stresses on AMS04 wafer show that in "ON-state" a dramatic decrease of drain current and transconductance is present. All devices developed gate-lag transient effects to various extents and a moderate increase in gate forward and reverse current was observed only in some devices. In "SEMI-ON " and "OFF-state" tests is always present a decrease in the maximum of transconductance; development of drain current transient effects during gate-lag experiments is frequently observed. Devices long and short term reliability is actually still an important issue to be solved.

After a thermal storage performed for 2000 hours at 300°C a new failure mechanism on GaN HEMTs has been identified. DC measurements have shown a slight degradation of the devices current value, no threshold voltage shift, but a severe degradation was identified in pulsed and low-frequency measurements. The main failure mode was an enhancement of trapping effects that took place on the device surface access regions, more precisely at the interface between the AlGaN layer and the SiN passivation. Failure analysis demonstrated that a loss of adhesion of the passivating layers was responsible for the observed trap reactivation. An improved passivation deposition process was then developed, including a surface cleaning procedure aimed to preventing passivation detaching. Devices fabricated using this new procedure have not shown any enhancement of trapping effects up to 500 hours of stress at 300°C.

The reverse-bias step stress experiments strongly suggest that the defectivity of the epitaxial material contributes to enhance reverse-bias degradation of GaN HEMTs; when a certain reverse voltage is reached, depending on defect density and energy position of deep levels, trap-assisted tunneling occurs, focusing the current into specific areas, eventually resulting in permanent localized degradation, with

further generation of deep levels. A different and gradual mechanism consists in the trapping of electrons at the surface of the gate-drain region, which increases parasitic resistances, reduces I_D and g_m and induces breakdown walkout.

The characterization of the breakdown properties of the GaN-based devices has eventually been analyzed. We have carried out the analysis of two terminal and three terminal breakdown properties. Breakdown voltages in some devices are strongly dependent on gate bias , whereas in other devices the breakdown is almost independent from the gate bias. Failure analysis revealed that two main failure mechanisms following the destructive breakdown characterization are present: GaN-lattice degradation (possibly related to a pre-existing crystal defect) and metal filamentation due to metal fusion. We have submitted the devices to Electrostatic Discharge evaluation using TLP and the HBM model. A strong capacitive coupling between the Drain, Gate, and Source terminals has been found to be responsible of the impaired reliability of the Gate-Source Schottky diode in the Drain-Source TLP stress. The scaling of the failure current with the device width, both for Drain and Gate stresses, has been also investigated. We observed a completely different failure mode in Gate-Source TLP stress involving Gate metal line fusion.

Al mio cielo in una stanza