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Ph.D. THESIS

**Hybrid substrates employment for the  
development of Gallium Nitride HEMTs:  
study of reliability and failure modes**

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## REFERRED JOURNAL PAPERS

- F. Danesin, **F. Zanon**, S. Gerardin, F. Rampazzo, G. Meneghesso, E. Zanoni, and A. Paccagnella, “*Degradation induced by 2-MeV Alpha Particles on AlGaIn/GaN High Electron Mobility Transistors*” *Microelectronic Reliability*, Vol. 46, Issues 9-11, pp. 1750-1753
- G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, **F. Zanon**, A. Tazzoli, M. Meneghini, and E. Zanoni “*Reliability of GaN High-Electron-Mobility Transistors: State of the Art and Perspectives*”, *IEEE Transactions on Device and Materials Reliability*, Vol. 8, Issue 2, June 2008, pp. 332 – 343
- A. Tazzoli, G. Meneghesso, **F. Zanon**, F. Danesin, P. Bove, R. Langer, J. Thorpe, and E. Zanoni “*Electrical Characterization and Reliability Study of HEMTs on Composite Substrates under High Electric Fields*”, *Microelectronic Reliability*, Vol. 48, Issues 8-9, pp. 1370-1374
- F. Danesin, A. Tazzoli, **F. Zanon**, G. Meneghesso, E. Zanoni, A. Cetronio, C. Lanzieri, S. Lavanga, M. Peroni, and P. Romanini “*Thermal Storage Effects on AlGaIn/GaN HEMT*”, *Microelectronic Reliability*, Vol. 48, Issues 8-9, pp. 1361-1365

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- **F. Zanon**, F. Danesin, S. Gerardin, F. Rampazzo, G. Meneghesso, E. Zanoni, and A. Paccagnella, “*Impact of 2-MeV Alpha Irradiation*”

- on AlGaN/GaN High Electron Mobility Transistors*", 30<sup>th</sup> Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe, WOCSDICE 2006
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  - A. Tazzoli, F. Danesin, C. Ongaro, F. Rampazzo, **F. Zanon**, E. Zanon, and G. Meneghesso "*High Voltage Electrical Characterization of Field-Plate Gate HEMT Devices*" , 16<sup>th</sup> European Heterostructure Technology Workshop, HETECH 2007
  - E. Zanoni, G. Meneghesso, G. Verzellesi, F. Danesin, M. Meneghini, F. Rampazzo, A. Tazzoli, and **F. Zanon**, "*A review of failure modes and mechanisms of GaN-based HEMT's*", invited paper at the 2007 IEEE International Electron Device Meeting, IEDM 2007
  - G. Meneghesso, G. Verzellesi, F. Danesin, M. Meneghini, F. Rampazzo, A. Tazzoli, **F. Zanon**, and E. Zanoni "*Degradation of GaN HEMT at high drain voltages*", 11<sup>st</sup> International Symposium on Microwave and Optical Technology, ISMOT 2007
  - **F. Zanon**, F. Danesin, A. Tazzoli, G. Montanari, A. Chini, J. Thorpe, C. Gaquière, G. Meneghesso, and E. Zanoni "*High power performances of GaN HEMT on SopSiC substrate*", 32<sup>nd</sup> Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe, WOCSDICE 2008
  - G. Meneghesso, F. Danesin, F. Rampazzo, **F. Zanon**, A. Tazzoli, M. Meneghini, and E. Zanoni "*Light emission in GaN HEMTs: a powerful characterization and reliability tool*", invited paper at the International Workshop on Nitride semiconductor, IWN 2008

- **F. Zanon**, F. Danesin, A. Tazzoli, M. Meneghini, N. Ronchi, A. Chini, P. Bove, E. Zanoni, and G. Meneghesso “*Reliability aspects of GaN-HEMTs on composite substrates*”, invited paper at the 7<sup>th</sup> International Conference on Advanced Semiconductor Devices and Microsystems, ASDAM 2008
- **F. Zanon**, N. Ronchi, F. Danesin, P. Bove, R. Langer, J. Thorpe, A. Stocco, and G. Meneghesso “*An investigation of reliability on hybrid substrates GaN-HEMTs*”, 17<sup>th</sup> European Heterostructure Technology Workshop, HETECH 2008
- F. Danesin, A. Tazzoli, **F. Zanon**, G. Meneghesso, E. Zanoni, A. Cetronio, C. Lanzieri, S. Lavanga, M. Peroni, and P. Romanini “*Correlation between traps location and dispersion effects in AlGaIn/GaN HEMTs*”, 17<sup>th</sup> European Heterostructure Technology Workshop, HETECH 2008
- A. Chini, M. Esposito, M. Bonaiuti, G. Verzellesi, **F. Zanon**, E. Zanoni, and G. Meneghesso “*Influence of device self-heating on the activation energy extraction during current-DLTS measurement*”, 17<sup>th</sup> European Heterostructure Technology Workshop, HETECH 2008



## SOMMARIO

Questa tesi riassume il lavoro svolto relativo alla caratterizzazione statica, dinamica, affidabilistica, ai modi di guasto e agli effetti parassiti legati al funzionamento di transistor ad alta mobilità elettronica (High Electron Mobility Transistor - HEMT) basati su eterostruttura AlGaN/GaN.

La prima parte della tesi, in particolare, sintetizza l'attività di caratterizzazione elettrica e l'analisi affidabilistica effettuate su dispositivi cresciuti su substrati innovativi, come SopSiC e SiCopSiC, sviluppati all'interno del progetto europeo HYPHEN. Questi substrati sono realizzati tramite il trasferimento, su un wafer di carburo di silicio policristallino, di un sottile strato monocristallino di silicio (SopSiC) o carburo di silicio (SiCopSiC). I substrati ibridi sono stati studiati allo scopo di trovare un'alternativa funzionale e meno costosa rispetto al convenzionale SiC monocristallino, attualmente utilizzato come substrato preferenziale per la crescita di dispositivi su nitruro di gallio. Un'analisi delle caratteristiche statiche, impulsive e RF è stata effettuata su tutti i campioni ricevuti, oltre ad alcuni test per valutare le massime tensioni sostenibili dalle strutture (breakdown). Si è valutato dunque come questi dispositivi innovativi presentino performance (in termini di corrente di saturazione, massima trans conduttanza, correnti di perdita, tensione di soglia) in costante miglioramento, che stanno quindi raggiungendo quelle dei transistor cresciuti da più di 10 anni su SiC. Alcuni HEMT misurati mostrano caratteristiche in regime dinamico molto promettenti, con ottime prestazioni RF, mentre altri sono purtroppo affetti da fenomeni di dispersione in frequenza. Da un'attenta analisi si è però dimostrata la non diretta correlazione tra la presenza delle trappole responsabili di questi fenomeni dispersivi e l'utilizzo dei substrati ibridi, facendone invece ricadere la causa nei difetti superficiali. Questo risultato è molto importante, in quanto

esclude uno degli aspetti più critici previsti all'inizio del progetto: la formazione di trappole di tipo "bulk-related". L'affidabilità dei dispositivi cresciuti su substrato ibrido è stata valutata mediante una serie di test di ageing. Un'analisi preliminare è stata condotta tramite una serie di brevi "step-stress", con tensioni massime drain-source di 30 V, evidenziando un buon comportamento per quasi tutti i wafer misurati. Per i dispositivi più promettenti il test è stato prolungato fino ai 50 V, e sorprendentemente le principali caratteristiche elettriche sono rimaste pressoché invariate. È stato infine effettuato un test di vita accelerata su un wafer cresciuto su SopSiC, sia a canale aperto che a canale chiuso. Dopo 1000 ore di stress in condizione di canale aperto i dispositivi non hanno mostrato alcuna variazione nelle caratteristiche elettriche, mentre alla fine del test a canale chiuso si è notato un aumento della corrente di leakage.

La seconda parte della tesi analizza in dettaglio i fenomeni parassiti legati al funzionamento degli HEMT su nitruro di gallio. Questo studio è stato effettuato all'interno del progetto europeo KorriGaN, (**Key OR**ganisation for **R**esearch on **I**ntegrated circuit in **GaN** technology) su dispositivi cresciuti su SiC, in quanto tecnologia più matura. I risultati sono ad ogni modo estendibili ai dispositivi cresciuti su substrati ibridi. L'eventuale presenza di trappole superficiali è stata contrastata da tecniche di passivazione ottimali, permettendo funzionamenti in regime dinamico buoni, con cali di corrente in regime impulsivo rispetto alla condizione statica (current slump) mediamente del 20%. Una parte del lavoro è stata dedicata a valutare la dipendenza del collasso di corrente dal tipo di materiale, dall'utilizzo o meno del field-plate e dalle geometrie, dimostrando come il field-plate abbia un impatto migliorativo solo quando la concentrazione di trappole superficiali è sufficientemente alta. L'aspetto del KINK è stato poi studiato in modo approfondito, tramite analisi di dipendenza dalla geometria del dispositivo, misure in funzione della temperatura, misure di foto-corrente, Deep Level Transient Spectroscopy (DLTS) e catodoluminescenza (CL). Queste misure hanno evidenziato come il KINK sia molto probabilmente correlato alla presenza di livelli profondi nello strato di GaN, e correlato inoltre alla presenza di banda gialla nello spettro di catodoluminescenza.

## ABSTRACT

In this work the electrical characterization of AlGa<sub>N</sub>/Ga<sub>N</sub> High Electron Mobility Transistors (HEMTs) grown epitaxially on composite SiC<sub>0.5</sub>SiC<sub>0.5</sub>, SiC<sub>0.5</sub>SiC<sub>0.5</sub> and silicon substrate processed in the frame of the European HYPHEN project have been reported. A full set of electrical characterization, DC, Pulsed and RF has been carried out. Some preliminary breakdown measurements have been also carried out. By comparing to the state of the art device developed since more than 10 years Ga<sub>N</sub> on SiC to those of HYPHEN projects Ga<sub>N</sub> on hybrid substrate, the electrical performance observed are good well in line. The main DC parameters (Maximum drain current, maximum transconductance, gate leakage current, threshold voltage) are approaching values obtained in devices processed in more conventional substrates. Current collapse free transistors with promising RF performances have been obtained. Some other devices present current collapse, however the data analysis indicate that the mechanism responsible for the collapse seems not to be related to the bulk material, but more to the surface. This is a very important result because, if confirmed, it will rule out the most critical aspect that was forecast at the beginning of the project: bulk-related trap phenomena. The reliability aspects of hybrid substrates devices have been then investigated. A “short-term” step-stress plan with a maximum drain-to-source voltage of 30 V on several wafers has been carried out. No degradation has been observed in almost all tested devices but some devices exhibit remarkable degradation at relatively low  $V_{DS}$  voltages. On selected wafers, the step-stress test has been also extended up to  $V_{DS} = 50$  V and, surprisingly, devices exhibited very excellent reliability performances, showing no degradation.

A deep investigation of traps responsible of Ga<sub>N</sub> HEMTs parasitic effects has been reported in the second part of this work. This study has been performed on

AlGaIn/GaN devices grown on conventional SiC substrate in the frame of the European project KorriGaN (**Key OR**ganisation for **R**esearch on **I**ntegrated circuit in **GaN** technology), since the fabrication technology is more mature. By the way, the same considerations could be extended to composite substrate devices as well. In general, effective passivation of surface traps has been achieved, and good results have been achieved by KorriGaN wafers, with reduced decrease of the drain current during pulsed operation. Average current slump level is ~80% (ideal value is 100%). The dependence of the current collapse effects on material, field-plate and device geometry has been also studied, demonstrating that field plate has a strong effect on collapse only when a high density of surface traps is present. The study of the dependence of "KINK effect" on device geometry, together with measurements as a function of temperature, photocurrent spectroscopy, Deep Level Transient Spectroscopy (DLTS) and cathodoluminescence (CL) spectroscopy within a Scanning Electron Microscope (SEM) have shown that the kink effect is due to the presence of deep levels within the undoped GaN layer, possibly related with the observation of yellow luminescence in the CL spectra.

# INTRODUCTION

## 1.1 NITRIDE BASED DEVICES

In recent years, with the expansions of wireless communication market the research units' activity has put a lot of effort in microwave transistors development, with ever-increasing performances requirement. Wider bandwidth and improved efficiency are required for future generation portable phones, while satellite communication systems and TV broadcasting need amplifiers working at higher frequencies (up to 30 – 40 GHz) and higher power, in order to reduce the size of the terminal user antenna. Semiconductor devices based on silicon (Si) are already pushed closed to their limit, working with a poor efficiency and requiring very large cooling systems. Under these circumstances, a lot of activity has been invested in the development of compound semiconductor transistors and amplifiers. The main physical properties of the most adopted material are listed in Table 1.1. The Johnson's figure of merit (JM), calculated to compare the power-frequency limits of different materials [1] is also reported. This parameter permit to select which is the material preferable in terms of large breakdown voltage ( $E_{br}$ ) and high electron mobility ( $\mu_n$ ), required for high power and high frequency operations. Therefore, wide bandgap materials with higher JM, like SiC and GaN, are the best candidates for the above-mentioned applications. These two semiconductors present almost similar breakdown fields and saturation electron velocities, but the ability of gallium nitride to form heterostructures make it superior compared to silicon carbide. In fact, GaN can be widely adopted for the fabrication of **H**igh **E**lectron **M**obility **T**ransistors (**HEMTs**) whereas SiC can only be used to fabricate **M**etal **S**emiconductor **F**ield **E**ffect **T**ransistors (**MESFETs**). High carrier concentration ( $n_s$ ) and high electron mobility can be

achieved adopting a HEMT structure, due to reduced ionized impurity scattering. By combining high  $n_s$  and high  $\mu_n$ , it is possible to realize devices with high current densities and low channel resistances, which are key points for high frequency operation and power switching applications.

Table 1.1: material properties for various compound semiconductor materials.

	<b>Si</b>	<b>GaAs</b>	<b>4H-SiC</b>	<b>GaN</b>	<b>Diamond</b>
$E_g$ (eV)	1.1	1.42	3.26	3.39	5.45
$n_i$ (cm <sup>-3</sup> )	$1.5 \times 10^{10}$	$1.5 \times 10^6$	$8.2 \times 10^9$	$1.9 \times 10^{10}$	$1.6 \times 10^{27}$
$\epsilon_r$	11.8	13.1	10	9	5.5
$\mu_n$ (cm <sup>2</sup> /V s)	1350	8500	700	1200(bulk) 2000(2DEG)	1900
$v_{sat}$ (10 <sup>7</sup> cm/s)	1.0	1.0	2.0	2.5	2.7
$E_{br}$ (MV/cm)	0.3	0.4	3.0	3.3	5.6
$\Theta$ (W/cm K)	1.5	0.43	3.3-4.5	1.3	20
$JM = E_{br} v_{sat} / 2\pi$	1	2.7	20	27.5	50

Epitaxial growth of GaN HEMT devices usually takes place on three types of substrate: sapphire, silicon, and silicon carbide (SiC). The latter one is the preferred substrate due to its high thermal conductivity but, on the other hand, it is also the most expensive. In this thesis, innovative solutions based on two types of “composite substrates” obtained from variants of the Smart Cut™ technology developed by SOITEC [2] are presented. These solutions come from the European HYPHEN project (Hybrid Substrates for Competitive High Frequency Electronics), which has the aim to *develop and evaluate a new type of composite substrate based on Silicon and Silicon Carbide materials, able to provide a cost efficient solution that will leverage the use of advanced high power devices in wireless communication systems* [3]. This project develop and characterize the complete technology chain, from substrate manufacturing to device processing, relying on a European consortium composed of academic institutes (University of Padova DEI - Italy, Research Institute for Technical Physics and Material Science MFA - Hungary, Institute of Electron Technology IET – Poland, and Centre National de la Recherche Scientifique IEMN - France) and industrial partners (Norstel - Sweden, Picogiga International - France, United Monolithic Semiconductor UMS – Germany and Alcatel Thales III-V Lab - France).

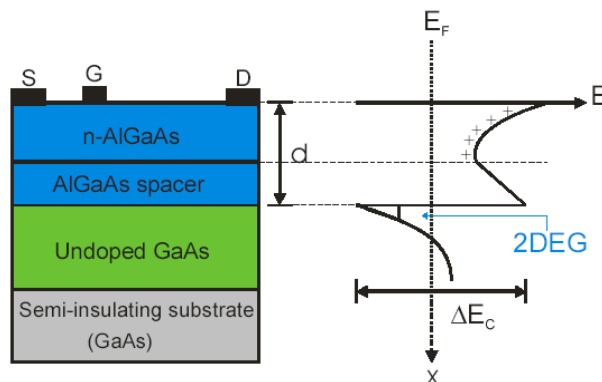
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These new composite substrates are both made of a thin single crystal layer transferred onto a thick polycrystalline silicon carbide base. The top single crystal layer is made of silicon for “**SopSiC**” substrates (**Silicon on polySiC**), and made of silicon carbide for “**SiCopSiC**” (**Silicon Carbide on polySiC**) substrates. By combining the high quality SiC single crystal top layer with the high thermal conductivity of inexpensive polycrystalline SiC, the use of SiCopSiC composite substrates is expected to significantly decrease the cost of the GaN HEMT structures grown on it, while keeping device performances almost similar to those obtained using bulk SiC substrates. On the other hand, the adoption of SopSiC composite substrates could improve the large volume application of composite substrates devices, since large seed silicon substrate for device manufacturing are available (4 or 6 inches), with the advantages offered by the improved thermal conductivity of the polySiC with respect to bulk silicon.

The successful experiments on modulation doped AlGaAs/GaAs heterostructures [4], which revealed the formation of a two-dimensional electron gas (2DEG) with enhanced electron mobility, have showed the way forward to the development of the first HEMT structure in 1980 [5]. Semiconductor heterostructures, defined as heterogeneous semiconductor structures built of two or more different semiconductors, is formed when a semiconductor material is grown with epitaxial techniques on the top of another semiconductor material. Earlier HEMTs adopted the AlGaAs/GaAs system, which was the most widely studied and the best understood hetero-junction system. In classic semiconductors, in order to increase the free carrier density, it is required to highly doping the structure with consequent impurities incorporation. Dopants create local lattice distortions, and then the scattering is increased with consequently electron and hole mobility decreasing. A HEMT device is based on a hetero-junction between a low  $E_g$  *channel layer* (i.e. GaAs) and a high  $E_g$  *barrier layer* (i.e. AlGaAs). The 2DEG conductive channel is formed at the hetero-interface, with the possibility of increasing the conductivity by barrier layer modulation doping, without suffering the mobility degradation effects due to the impurity scattering.

An example of structure schematic and band diagrams of an AlGaAs/GaAs HEMT are shown in Fig. 1.1. For a n-type doping of the barrier, the region in the barrier close to the interface will be depleted, and the corresponding electrons will accumulate in a so called *triangular quantum well*, in the channel layer close to the hetero-interface, forming the 2DEG. The most important feature is that these carriers have higher mobility in comparison to the bulk mobility in the active layer, since they are spatially separated from the ionized donors in the barrier layer [4]. Experimentally, the existence of the 2DEG can be evaluated by measuring the temperature dependence of the carrier mobility and carrier concentrations using low temperature Hall measurement. Results obtained by Hall measurements support the existence of this two dimensional electron gas by showing the temperature mobility invariability at temperatures below 100K, which is the characteristic temperature for the optical phonon scattering to be pronounced [6].

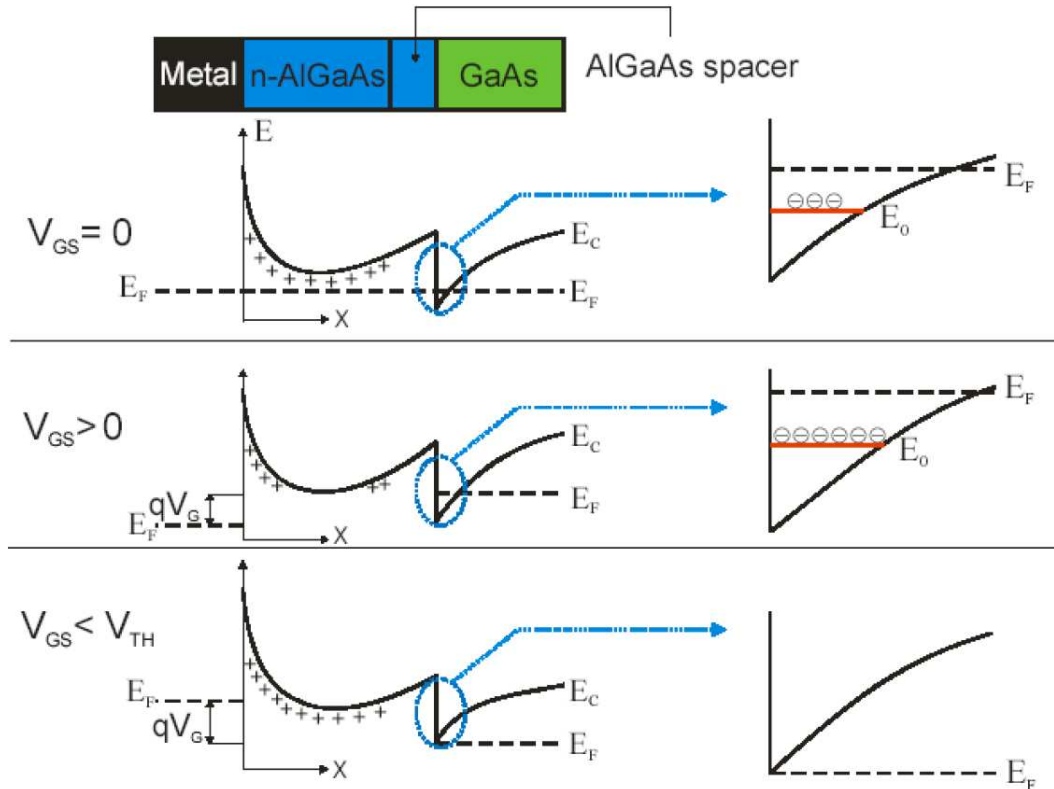
In a typical HEMT structure, the drain current is controlled by gate modulation of 2DEG density. When the gate contact is zero biased, the 2DEG is formed and the channel is open. The current can be increased by applying a positive voltage to the gate, which increases the 2DEG density and the current density in the conductive channel. However, when the gate voltage is below the threshold (or pinch-off) voltage, the channel is depleted, and the drain current approaches zero regardless of the drain bias. The mechanisms of current control under different



**Fig. 1.1:** schematic of an AlGaAs/GaAs HEMT and the corresponding conduction band diagram.

Location of the 2DEG is also shown [7].

gate biases are shown in Fig. 1.2.



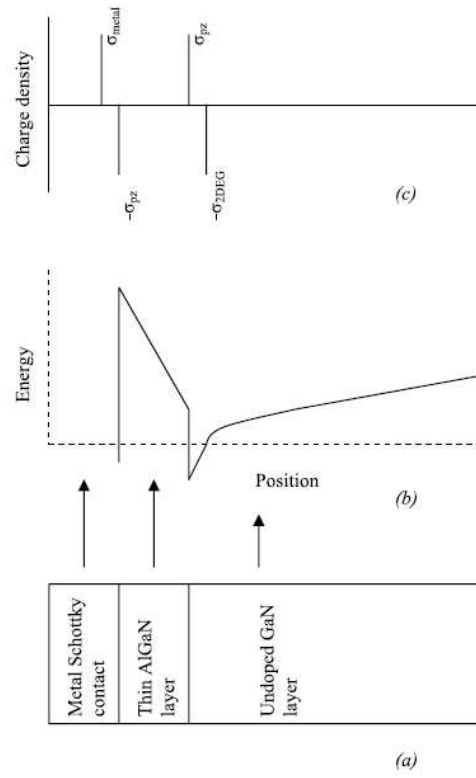
**Fig. 1.2:** conduction band diagrams and 2DEG populations of an AlGaAs/GaAs HEMT under different gate biases [7]

## 1.2 DEVELOPMENT OF GALLIUM NITRIDE HEMTS

As largely reported in literature, nitride semiconductors like AlN, GaN, InN and their alloys are very promising materials thanks to their potential application in electronic and optoelectronic devices [8]. Gallium nitride large bandgap, large field strength, high thermal conductivity and good electron mobility make it suitable for high voltage, high power and high frequency applications, as previously shown in Table 1.1. Furthermore, one of the unique properties of nitride semiconductors is the presence of strong polarization field within the crystal, which has heavy impact on electronic properties of GaN-based heterostructures [9]. This polarization electric field is two fold: *spontaneous polarization field* and *strain-induced piezoelectric field*.

When a thin semiconductor layer is epitaxially grown on the top of another semiconductor, with different lattice constants, the thin layer will grow with the lattice constant of the layer below. In this case the thin epitaxial layer becomes internally strained to accommodate the lattice constants mismatch. However, if the thickness of the thin layer exceeds an upper limit, the mismatch is accommodated by the formation of defects and dislocations near the interface rather than by the strain. A strained layer can exhibit a strained-induced piezoelectric field ( $P_{pz}$ ), which can be adopted to modify the carrier concentration near the hetero-junction layer with no doping. In a gallium nitride HEMT structure, the AlGaN barrier layer is strained on the top by a Schottky gate metal contact and on the bottom by the GaN buffer. The result is a polarization field which creates, at both interfaces, a polarization charge density ( $\sigma_{pz}$ ). As we can see in Fig. 1.3,  $\sigma_{pz}$  induces a compensating charge density at both metal/AlGaN and AlGaN/GaN interfaces. Notice that at this point the electron concentration in the GaN layer near the hetero-interface is significantly increased.

Another phenomenon that increases the carrier concentration at the hetero-interface in the absence of strain is the spontaneous polarization of GaN ( $P_{sp}$ ). The values of spontaneous polarization field in nitrides are quite large, and in the same order of magnitude as ferromagnetic crystals [10]. To increase the 2DEG concentration  $P_{sp}$  and  $P_{pz}$  must be aligned: in this way, the total polarization is the sum of the other two. The  $P_{sp}$  orientation in nitrides depends on crystal polarity, namely whether the cation sites (gallium) or the anion sites (nitrogen) are facing toward the sample surface [11]. If the crystal surface is a Ga-face  $P_{sp}$  points away from the surface to the substrate, see Fig. 1.4. In the case of a N-face  $P_{sp}$  the situation is inverted, see again Fig. 1.4. Almost all MOCVD grown nitrides are Ga-face, while MBE are usually N-face. Nevertheless, the polarity can be inverted by depositing a thin AlN *nucleation layer* prior to the growth of GaN.



**Fig. 1.3:** (a) device structure; (b) energy band diagram; (c) charge density [12]

The  $P_{\text{pz}}$  orientation depends on the type of strain: in compressive-strain  $P_{\text{pz}}$  and  $P_{\text{sp}}$  are opposed, in tensile-strain they are aligned [13] [14]. Since AlGaN layer grown on GaN is always in tensile-strain, the total polarization is:

$$P = P_{\text{pz}} + P_{\text{sp}}$$

Due to the presence of this strong polarization field across the AlGaN/GaN hetero-junction,  $n_s$  up to  $10^{13} \text{ cm}^{-2}$  can be achieved, without any doping [15]. There are several possible sources of electrons contributing to 2DEG accumulation: the GaN buffer layer, the AlGaN barrier layer, and the AlGaN surface states. Charges in the GaN buffer layer should be negative so that a potential well can be formed in the GaN side and the 2DEG confined. The transfer of electrons from the GaN buffer layer to the hetero-interface leaves behind positive charges and consequently potential barriers, so by any means electrons in the 2DEG cannot come from the GaN buffer layer. Similar to the case of AlGaAs/GaAs HEMTs, modulation doping in the AlGaN barrier layer positively

contributes to the formation of 2DEG. In any case, with undoped AlGaN a 2DEG density of  $10^{12} - 10^{13}$  can be achieved.

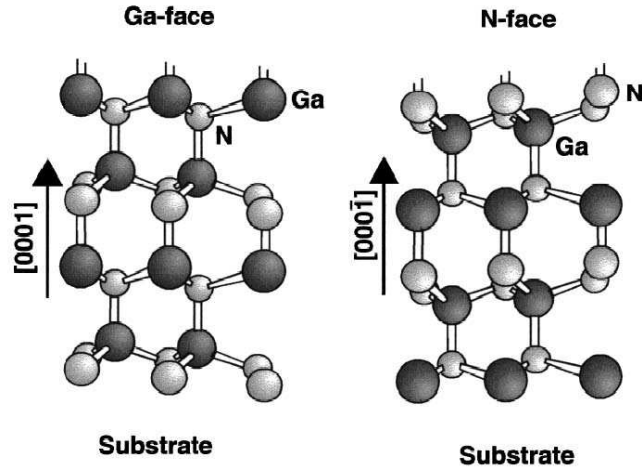
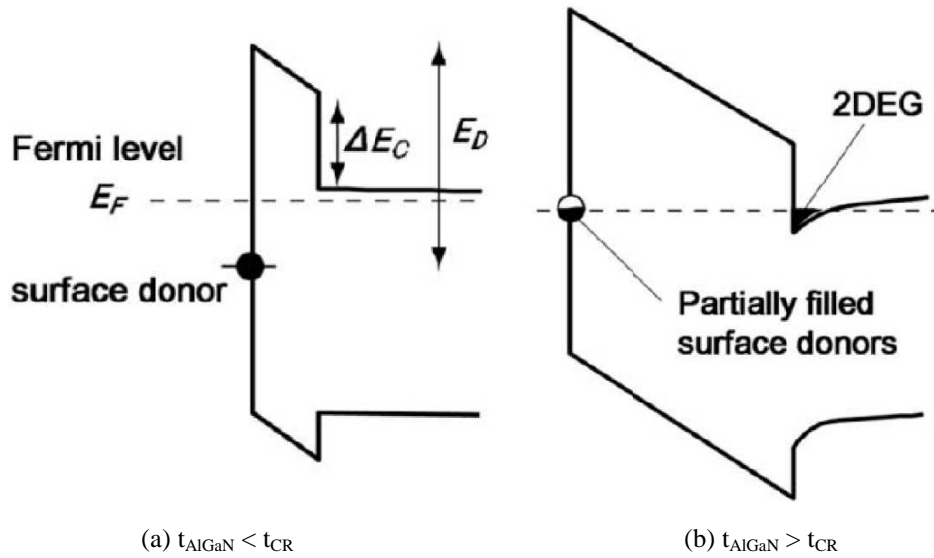


Fig. 1.4: Ga-face and N-face in wurtzite structure GaN [13]

*Ibbetson et al.* suggest that the surface states of the AlGaN layer are donor-like states, and when the strain-induced polarization field is sufficiently high to alter the band profile and the charge distribution, the electrons are attracted from the surface to the AlGaN/GaN hetero-interface forming the 2DEG [16]. A schematic representation of band profiles is shown in Fig. 1.5. If the AlGaN layer thickness is below the critical one ( $t_{CR}$ ), the surface donor states are still full and the 2DEG is not formed, see Fig. 1.5(a). On the other hand, if the layer thickness reaches and exceeds the  $t_{CR}$  the donor energy  $E_D$  is over the Fermi level  $E_F$  and electrons can migrate to the empty conduction band levels forming the electronic gas, see Fig. 1.5(b).

The  $n_s$  dependence in function of AlGaN thickness is plotted in Fig. 1.6: for little increment of barrier thickness over  $t_{CR}$  the charge density increases fast, then for greater increments it tends to saturate to a constant value. The diagram is the result of theoretical calculation (line) and experimental data (points) from the study of *Zhang et al.* [17].

The percentage of aluminium content in the AlGaN layer can also affect the sheet charge density of gallium nitride HEMT. By varying the aluminium

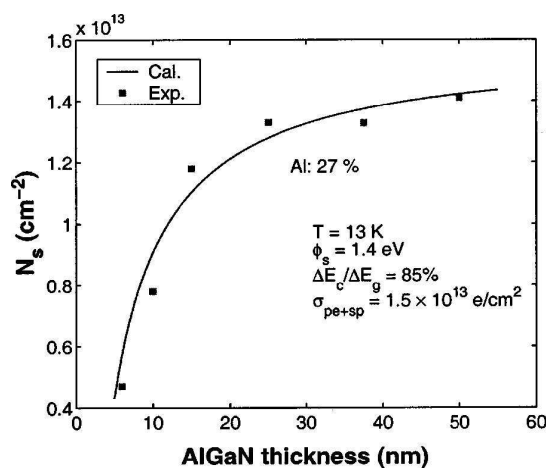


**Fig. 1.5:** schematic representation of band profiles with AlGaN layer thickness below (a) and above (b) critical thickness [16]

percentage  $x$  of the barrier layer  $\text{Al}_x\text{Ga}_{1-x}\text{N}$  it is possible to obtain energy gaps from 3.5 eV (like GaN,  $x = 0$ ) to 6.2 eV (like AlN,  $x = 1$ ). The critical thickness  $t_{\text{CR}}$  for an AlGaN/GaN hetero-structure can be obtained applying the following formula [16]:

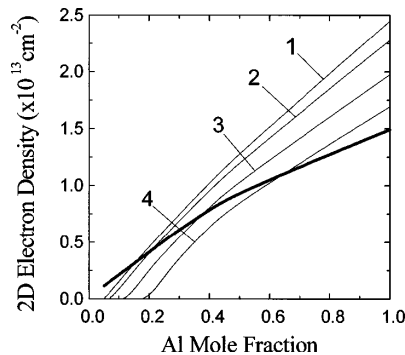
$$t_{\text{CR}} = \frac{(E_D - \Delta E_C)\epsilon}{q\sigma_{pz}}$$

It is clear how the conduction band discontinuity  $\Delta E_C$  (between GaN and



**Fig. 1.6:** two-dimensional sheet charge density as a function of AlGaN thickness [ronchi9].

AlGaN) strictly depends on AlGaN bandgap and hence on aluminium percentage. In addition, increasing the Al mole fraction, the piezoelectric effect increases and the charge sheet density grows. By the way, it must be remembered that highest  $n_s$  can not be reachable simply adopting higher Al content. If the aluminium percentage exceeds 40% then AlGaN becomes an insulating layer. Furthermore, the Al percentage negatively affects the upper limit of the AlGaN layer, beyond which lattice mismatch is accommodated by the formations of defects and dislocation at the hetero-interface (above mentioned). The electron density induced by piezoelectric effect in AlGaN/GaN heterostructures for different aluminum content is shown in Fig. 1.7 [18]; charge density increases with growth of Al content and layer thickness. Thicker line represents the charge density for a thickness equals to the upper limit, in this situation the AlGaN layer is fully strained (without relaxations).



**Fig. 1.7:** 2DEG density induced by piezoelectric effect in AlGaN/GaN heterostructures for different aluminum content and different AlGaN layer thickness: 1-30 nm; 2-20 nm; 3-10 nm; 4-5 nm. Thicker line represents the charge density for a thickness equals to the critical one as a function of Al content [18].

### 1.3 THE SUBSTRATE

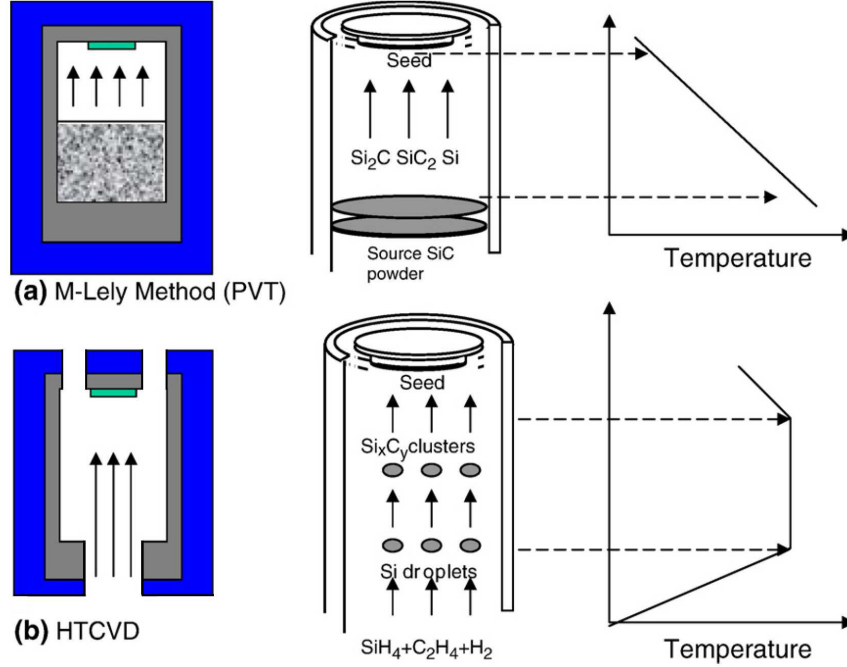
One of the main issues in the realization of GaN-based devices is the lack of native GaN substrate. In order to optimize the fabrication processes it is becoming necessary to produce high thermal conductivity, good lattice and thermal matched substrates. For these reasons, AlGaN/GaN HEMT devices are usually fabricated from epitaxial stacks on sapphire ( $\text{Al}_2\text{O}_3$ ), silicon carbide (SiC), and silicon (Si). The main properties of these materials are reported in Table 1.2.

Sapphire is usually adopted to produce high resistivity, low cost, and large area substrate. The main disadvantage is the poor thermal conductivity that makes HEMT-on-sapphire devices inappropriate for high power applications, in front of the self-heating effect. Furthermore, sapphire is ~15% [19] lattice mismatched with GaN, but this can be reduced adopting an AlN or GaN nucleation layer.

With the aim to reduce self-heating issues, the silicon carbide (SiC) was introduced in the middle of '90s. SiC has a higher thermal conductivity in respect to sapphire, and the lattice mismatch is only 3%. There are many forms, namely polytypes, in which the SiC crystallized (more than two hundreds). Generally, polytypes adopted for GaN epitaxial growth are 4H and 6H, where H indicates the hexagonal crystal symmetry and the number indicates the total of atomic layers in an elementary cell. Bulk SiC wafers are produced by two well-established growth processes: *modified Lely method* and *High Temperature Chemical Vapor Deposition* technique (HTCVD). The modified Lely method [20] is based on Physical Vapor Transport (PVT); a schematic representation of the process is shown in Fig. 1.8(a). In the growth chamber vapors from the sublimation of material sources, like SiC powder, condensate on a colder seed crystal. Temperature of sources, temperature gradient and pressure of the system are the parameters that control the growth rate. In HTCVD, shown on Fig. 1.8(b), the precursors are liberated in a vertical reaction chamber from the bottom, and carried to the top through a heating zone by an inert gas.

Here a seed crystal, kept in continuous rotating motion, is used for the growth of the bulk crystal substrate. This technique has some advantages than modified Lely method: the continuous supply of source materials, the relatively low cost of high purity gases and the control of the C/Si ratio. Both processes are available for the growth of monocrystalline and polycrystalline SiC, the only difference is in the seed crystal which establishes the kind of crystalline structure of the substrate; also poly-SiC not needs high control in fabrication process and slow growth rate, thanks to its polycrystalline nature. Mono-SiC wafers are available with maximum diameter of 3 inches, meaning a less throughput of devices per wafer, while poly-

SiC wafers reach 8 inches. Unfortunately, mono-SiC substrate is still very expensive, with low resistivity controllability and high dislocation density.



**Fig. 1.8:** growth processes for bulk single crystal SiC: (a) modified Lely method and (b) HTCVD [20].

Another candidate as GaN substrate is the silicon, that has larger lattice mismatch with GaN in respect to silicon carbide and sapphire, but it presents some interestingly characteristics. First, it is very cheap and growth processes are well known; second, it is available in high quality and large diameter wafers. Finally, Si-based and GaN-based devices can be realized on the same wafer.

Table 1.2: properties of different conventional substrates [19].

Property	Unit	Al <sub>2</sub> O <sub>3</sub>	6H-SiC	Si
Symmetry	-	hexagonal	hexagonal	cubic
Lattice constant a	Å	4.765	3.08	5.431
Lattice constant c	Å	12.982	15.117	-
Thermal conductivity	W/cm K	0.25	3.8	1.56
Lattice mismatch with GaN	%	15	3.1	17

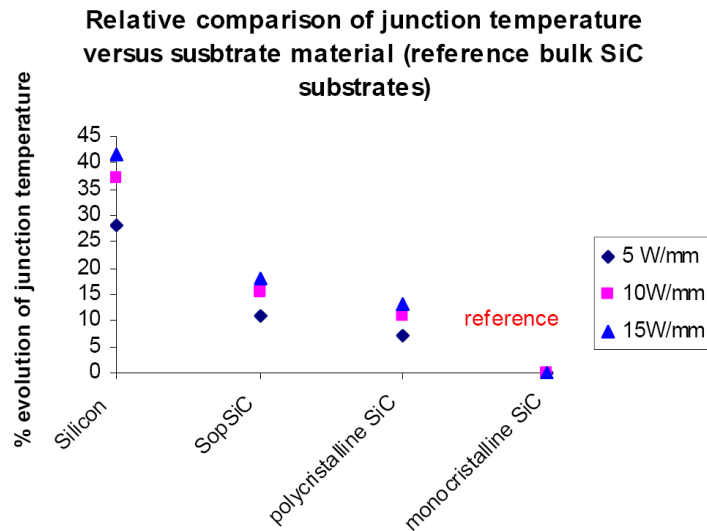
#### 1.4 COMPOSITE SUBSTRATES: HYPHEN PROJECT

The recent progress on substrate engineering has provided new technological approaches for GaN HEMT substrate realization. Two novel “hybrid substrates” have been developed in the frame of HYPHEN project, obtained from variants of the SOITEC SmartCut™ technology [2] [21]. These hybrid substrates consist in a thin layer of single crystal material supported by a thick layer of insulator or polycrystal material.

The SiCopSiC structure, for example, is formed by a thin film of monocrystalline SiC bonded onto an oxidized polycrystalline SiC wafer. Thanks to the multiple usages of high quality single crystal SiC used as seed layer, SiCopSiC allows to obtain high quality surfaces where growing GaN with contained lattice mismatch. Moreover, thanks to the high thermal conductivity of the inexpensive polycrystalline SiC, close to that one of mono-SiC (poly-SiC: 3.0 W/cm K, mono-SiC: 3.8 W/cm K), the global material cost would be significantly improved. Furthermore, the performances of GaN-based devices grown on SiCopSiC will be almost similar to the ones grown on bulk SiC substrate, in similar channel temperature conditions.

The SopSiC substrate is monocrystalline silicon bonded onto oxidized polycrystalline SiC. In this case, adopting Si as seed layer allows larger diameter substrates (4 or 6 inches) and in addition the thermal conductivity is significantly improved in respect to bulk silicon, thanks to the polycrystalline SiC substrate.

Thermal behaviors of a composite substrate have been simulated in order to investigate the effect of various parameters such as the thickness of the insulating intermediate layer, its nature, the thickness of the transferred silicon layer, and the power dissipated by the devices. A significant improvement in junction temperature increase (with the case at room temperature), is observed for SiCopSiC and SopSiC substrates compared to bulk silicon substrates. This is even more visible when the power level of the device is in the high range, see Fig. 1.9. This confirms that for nitride based devices the layer transfer-based composite substrates are very promising for high-performance, low-cost RF power applications.



**Fig. 1.9:** maximal computed junction temperature as a function of the substrate nature. The comparison is drawn for a range of power density to be dissipated from 5 to 15 W/mm.

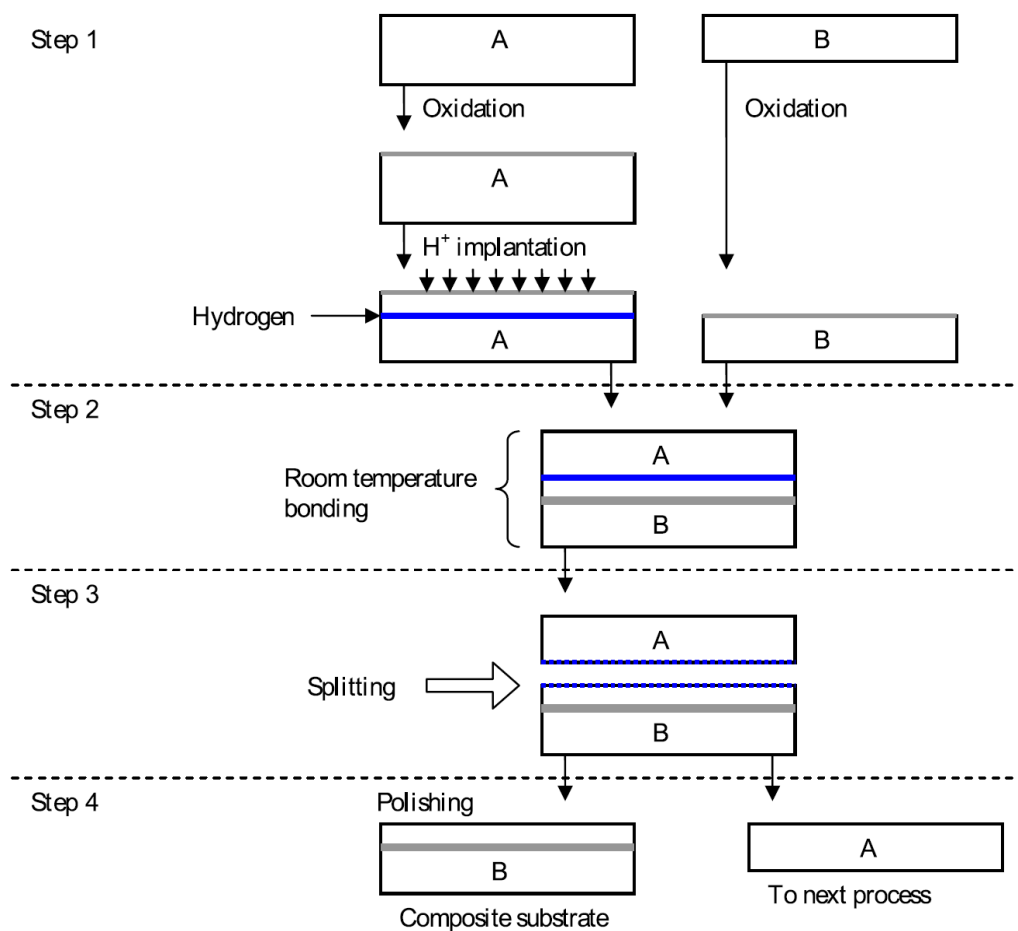
The fabrication technique adopted to produce composite substrates, sketched in Fig. 1.10, starts from two wafers that must be combined in a single wafer: the carrier and the seed. The first, called B on the diagram, in our case is a poly-SiC wafer that represent the base of the final compound substrate. The second, called A, can be single-crystal Si (for SopSiC) or single-crystal SiC (for SiCopSiC). The process consists in four fundamental steps:

1. The seed wafer is covered by thermal oxidation or chemical deposition with a  $\text{SiO}_2$  thin layer, and then exposed to a hydrogen ion implantation at room temperature. The implanted dose is approximately  $3.5 \times 10^{16} \div 1.0 \times 10^{17} \text{ cm}^{-2}$ . Ions form a thin layer with high density inside the wafer. The deep of this layer is defined by implantation energy ( $\sim 8 \text{ nm/keV}$ ). In addition, the surface of wafer B is covered by oxide.
2. Wafer A is pressed against wafer B to obtain a hydrophilic bonding at room temperature.
3. This step is divided in two annealing phases: the first at  $T \sim 500 \text{ }^\circ\text{C}$  and the second at  $T \sim 1100 \text{ }^\circ\text{C}$ . During the first annealing, the implanted ions create a thin layer of defects and micro cavities, which split the bonded wafer in

two parts. The second high temperature annealing is adopted to strengthen the bond between carrier and seed wafers.

4. In the final step, the top of the wafer (Si or SiC) is polished by a chemical-mechanical method in order to remove the surface roughness caused by splitting: a high-quality surface is important for the following epitaxial growth. Furthermore, residual of A wafer can be used for another process cycle.

5.



**Fig. 1.10:** four steps of SmartCut™ adopted process.

A section of this thesis is dedicated to the work performed in the frame of the European HYPHEN project. This project is divided in five workpackages (WP) [3]:

- **WP1 (Starting Materials)** aims at providing, characterizing and improving the material quality of the starting materials, then to reduce the material cost by increasing growth rate and diameter from 2" to 4", and finally to improve the growth yield.
- **WP2 (Composite Structure)** has four objectives:
  1. simulation about thermo-mechanical behavior related to the compound devices and starting materials;
  2. development of 4" silicon mature substrates and low cost perspectives;
  3. maintain the epitaxial layers quality resulting from a better lattice matching with the GaN family materials;
  4. development of an interactive characterization to qualify the various stages realized in the experiments.
- **WP3 (Epitaxy)** is the next decisive step in the validation of composite substrates. Three objectives have been identified:
  1. validate the epitaxy of III-N compounds on the composite substrates SopSiC and SiCopSiC;
  2. evaluate the crystal quality of the compound substrates;
  3. evaluate the composite substrates quality at the user's level, by providing GaAlN/GaN HEMT complete hetero-structures to be processed into test devices, which can be directly compared to devices on bulk single crystal substrates.
- **WP4 (Device Processing)** is necessary to get information on the composite substrate quality as seen from the device manufacturer's point of view. It is the next stage after the material characterization work performed in WP2 and WP3. One main goal of this work package has been set up the basis of a fabrication process adapted to the exploratory substrates.
- **WP5 (Assessment)** has the main goal to provide feedback information to the previous work packages: composite substrate fabrication in WP2, epitaxy in WP3, and wafer processing in WP4, in order to allow the

optimization of the fabrication process at each level. The focus has been put on the comparison between the characterization results obtained on reference wafers on silicon and SiC bulk substrates, *processed in the frame of other programs outside this project*, and composite substrates processed in WP4. As much as possible, we have tried to set up and validate methods for correlating the device electrical characteristics with the substrate material properties.

## 1.5 DESCRIPTION OF WORK

This work is divided in two macro section. In the first, the activity performed in the frame of HYPHEN project, related to the Assessment workpackage (WP5), has been described. The electrical characterization of GaN HEMT processed on composite SiCopSiC and SopSiC, by means of a full set of DC, pulsed, and RF measurement and a preliminary breakdown characterization has been carried out. Furthermore, the reliability aspect has been investigated by means of step-stress experiments. Finally, on devices that have shown negligible degradation a 1000 hours long term stress has been performed, resulting in very promising reliability performances.

A deep investigation of traps responsible of GaN HEMTs parasitic effects has been reported in the second part of this work. This study has been performed on AlGaIn/GaN devices grown on conventional SiC substrate in the frame of the European project KorriGaN (**Key OR**ganisation for **R**esearch on **I**ntegrated circuit in **GaN** technology), since the fabrication technology is more mature. By the way, the same considerations could be extended to composite substrate devices as well. The KorriGaN project has been launched in 2005 with the aim to accelerate the development of independent GaN HEMT foundries in Europe. The project addresses several key research areas such as materials, processing, reliability, thermal management and advanced packaging solutions. The benefits of GaN technology have be evaluated at system level with the fabrication of circuit, MMIC and module demonstrators. The project is supported by the ministry of defense (MOD) of seven nations and is primarily dedicated to defence

applications. The KorriGaN consortium consists of major European system houses and research laboratories, under the lead of Thales Airborne Systems, providing all the necessary competence for the establishment of the future GaN HEMT supply chain.

# **ELECTRICAL CHARACTERIZATION OF HYBRID SUBSTRATE DEVICES**

In this chapter, data concerning the detailed electrical characterisation of HYPHEN devices is reported. These characterisation results of devices fabricated on the composite substrates will be compared with those obtained on similar devices fabricated on reference epitaxial wafers on bulk single crystal Silicon or SiC substrates, processed in a similar way with the same mask set.

DC, Pulsed and RF characterisation has been carried out on the available test structures (mainly transistors) on material originating from workpackage 4 of the project. This data has enabled the mapping of many electrical characteristics for comparison with available material characteristics originating from other work-packages. Salient characteristics of the elementary microwave device such as the drain current, gate leakage, transconductance, current collapse as well as RF power and current gains have been analysed.

## **2.1 DEVICE DESCRIPTION**

As already mentioned in the Introduction chapter, hybrid substrate wafers studied in this work came from the European HYPHEN project. Two sets of devices, coming out from two production batches, have been received from partners (*United Monolithic Semiconductor UMS*, *Institut d'Electronique de Microélectronique et de Nanotechnologie IEMN*, and 3-5 Lab): a first batch (1<sup>st</sup>-batch) and a second batch (2<sup>nd</sup>-batch). Second batch wafers were realized after first batch realization and testing; hence an improvement of electrical characteristics is expected.

The tested wafers list, within information about epilayer and substrate supplier is reported in Table 2.1. Some devices processed on wafers grown on SiC are here adopted as REFERENCE (first 2 rows in Table 2.1). The others have been processed on composite SiCopSiC, SopSiC and silicon substrate developed within the HYPHEN Project.

**Table 2.1:** list of tested wafers (both BATCH 1 and BATCH 2 devices)

foundry	wafer	batch	epilayer		substrate
			reactor	supplier	
3-5 Labs	AEC1142	REF		TRT	SiC
	AEC1147	REF		TRT	SiC
UMS	AEC1333	1	MOCVD	TRT	SiCopSiC
	AEC1337	1	MOCVD	TRT	SiCopSiC
	L879	2	MBE	Picogiga	SopSiC
	L1053	2	MBE	Picogiga	Si
	L909	2	MBE	Picogiga	Si
	L1338	2	MBE	Picogiga	Si
IEMN	AEC1345	1	MOCVD	TIGER	SiCopSiC
	L895	1	MBE	Picogiga	SiCopSiC
	AEC1341	1	MOCVD	TRT	SiCopSiC
	LO-792	1	MBE	Picogiga	SopSiC
	LO-896	1	MBE	Picogiga	SiCopSiC
	LO-1055	2	MBE	Picogiga	SiCopSiC
	AEC1470	2	MOCVD	TRT	SiCopSiC
3-5 Lab	AEC1313	2	MOCVD	TRT	SiCopSiC

In Fig. 2.1 the main transistor peripheries are showed. Gate width ( $W_G$ ), gate length ( $L_G$ ), gate-to-drain spacing ( $L_{GD}$ ), and drain-to-source spacing ( $L_{DS}$ ) are defined. Since the gamma-shaped gate technology has been adopted for the processing of some devices, the gate drain overhang length ( $L_{SH}$ ) of a  $\Gamma$ -gate is also defined in Fig. 2.1(b). Unfortunately, not all geometrical data are available from wafer suppliers, and then some wafers not have a complete peripheries description. The available information about peripheries and layer structures are listed in Table 2.2 and Table 2.3.

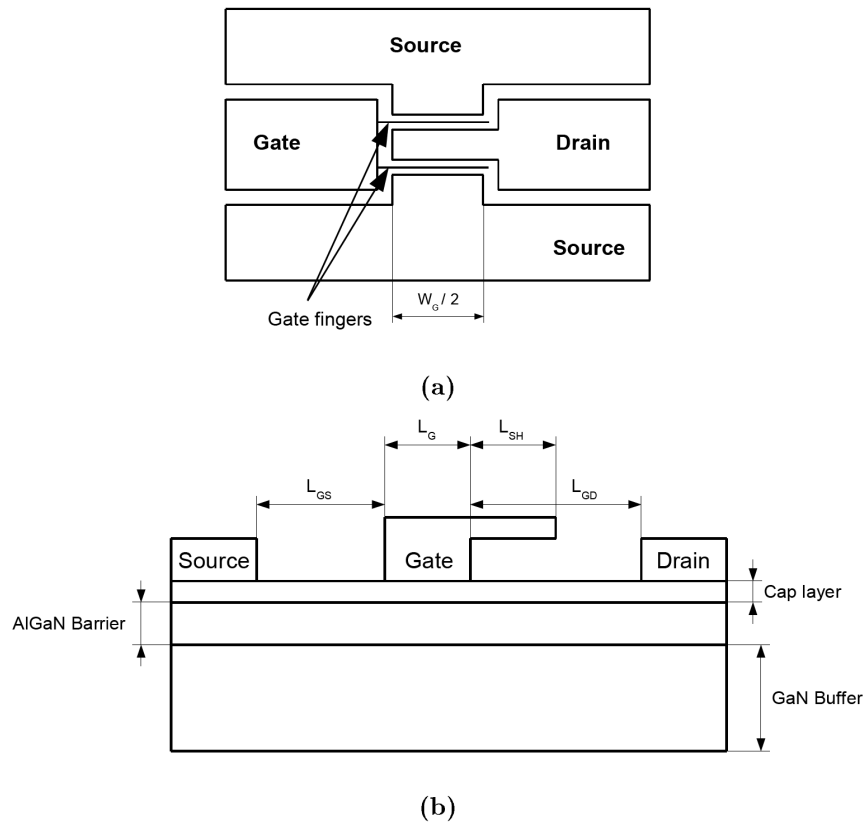


Fig. 2.1: transistor peripheries definition.

Table 2.2: layer structures of tested devices (some information is missing).

foundry	wafer	GaN	AlGaN		Cap	passivation	maskset
		( $\mu\text{m}$ )	(nm)	(%Al)	(nm)	(nm)	
3-5 Labs	AEC1142	1	25	27	no	(SiO <sub>2</sub> /SiN)	Sangha
	AEC1147	1	25	29	no		Sangha
UMS	AEC1333						Pytheas
	AEC1337						Pytheas
	L879	1.5	23	31	2	100+300 (SiN <sub>x</sub> )	Pizarro
	L1053	1.5	22	20	2		Pizarro
	L909						Pizarro
	L1338						Tasman
IEMN	AEC1345						Flash
	L895						Flash
	AEC1341						Flash
	LO-792						Flash
	LO-896					100/50 (SiO <sub>2</sub> /SiN)	Flash
	LO-1055	1.5	22	25	1	240 (Si <sub>3</sub> N <sub>4</sub> )	Koumal
	AEC1470	1.8	24	20	no	240 (Si <sub>3</sub> N <sub>4</sub> )	Koumal
3-5 Lab	AEC1313	1.15	25	24.3			Lynx

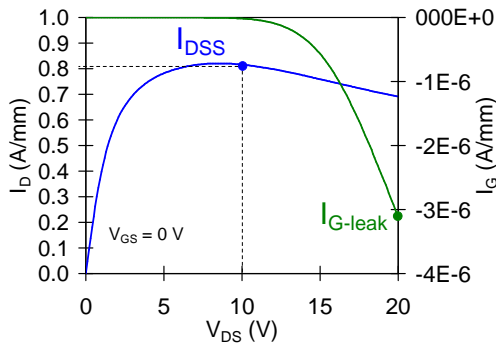
**Table 2.3:** maskset geometries (of measured devices).

maskset	$W_G$	$L_G$	$L_{GD}$	$L_{GS}$
	( $\mu\text{m}$ )	( $\mu\text{m}$ )	( $\mu\text{m}$ )	( $\mu\text{m}$ )
Sangha	200	0.25	3	1
Pytheas	80	0.5	2.5	1.25
			3.5	1
			1.75	1
Pizarro	100 – 320 - 480	0.3		
		0.5		
		0.7		
Flash	100 – 200 – 300 - 400	1		
		2		
		3		
Tasman	100 - 480	0.5		
Koumal	100 – 150 – 200 - 280	0.25	2	1
Lynx	150	0.25	2	1

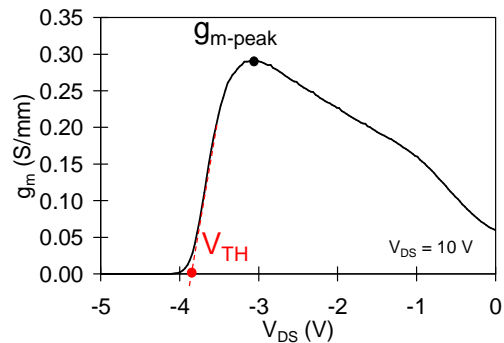
## 2.2 DC CHARACTERIZATION

A DC characterization has been performed on all received wafers, as a preliminary test, to check if transistors work correctly. Despite HEMT devices are designed to operate in power microwave circuits, the DC electrical characterization is the starting point to evaluate the electrical parameters and performances of such devices. Measurements have been carried out under dark-light conditions using an Agilent E5263A parameter analyzer, connected to a computer via GP-IB cable. A *virtual instrument* (VI) created with LabVIEW permits instrument control and data acquisition.

In order to compare static performances of tested devices, a set of parameters has been extracted from the static characterization, among other thing saturation drain current  $I_{DSS}$ , leakage current  $I_{G-leak}$ , transconductance  $g_{m-peak}$ , and threshold voltage  $V_{TH}$ . A definition of how these parameters have been extracted is presented in Fig. 2.2 and Fig. 2.3:



**Fig. 2.2:**  $I_{DSS}$  and  $I_{G-leak}$  definition



**Fig. 2.3:**  $g_{m-peak}$  and  $V_{TH}$  definition

A general comparison of these main DC parameters extracted from analyzed devices is reported on Fig. 2.4, Fig. 2.5, Fig. 2.6, and Fig. 2.7. In particular:

- Fig. 2.4 reports the saturated drain current density,  $I_{DSS}$  (A/mm), measured at  $V_{GS} = 0$  V.
- Fig. 2.5 reports the transconductance peak,  $g_{m-peak}$  (S/mm) measured at a drain to source voltage ( $V_{DS}$ ) of 10 V.

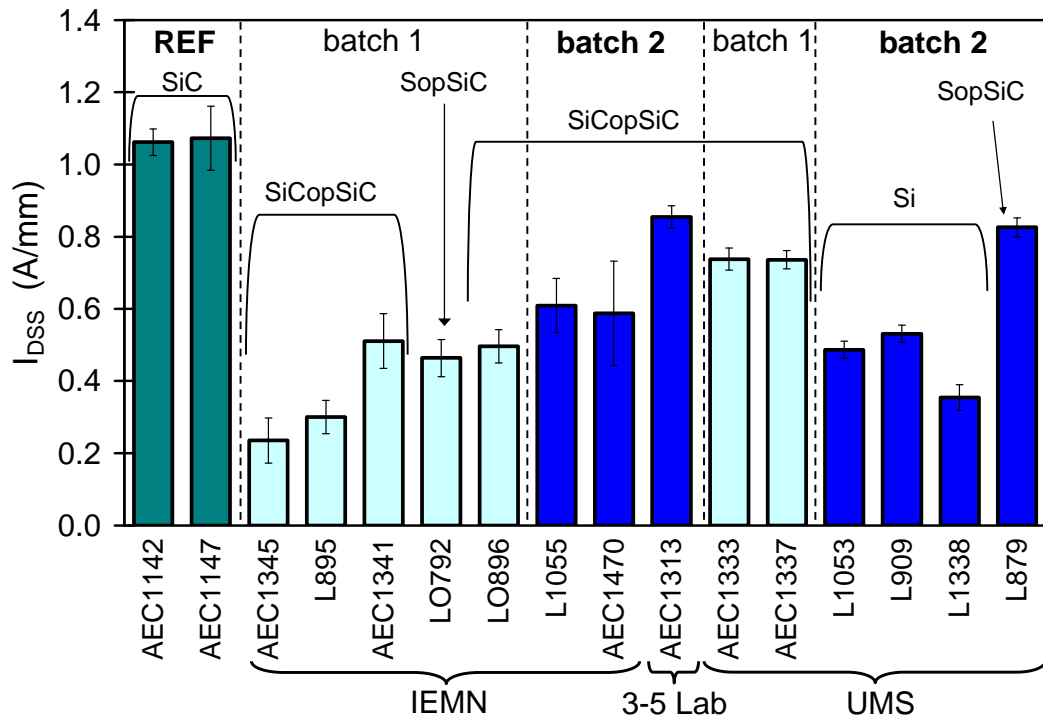
Fig. 2.6 reports the gate leakage current,  $I_{G\text{-leak}}$  (A/mm) measured at  $V_{DS} = 20$  V and  $V_{GS} = 0$  V.

Fig. 2.7 reports the threshold voltage  $V_{TH}$  measured at  $V_{DS} = 10$  V.

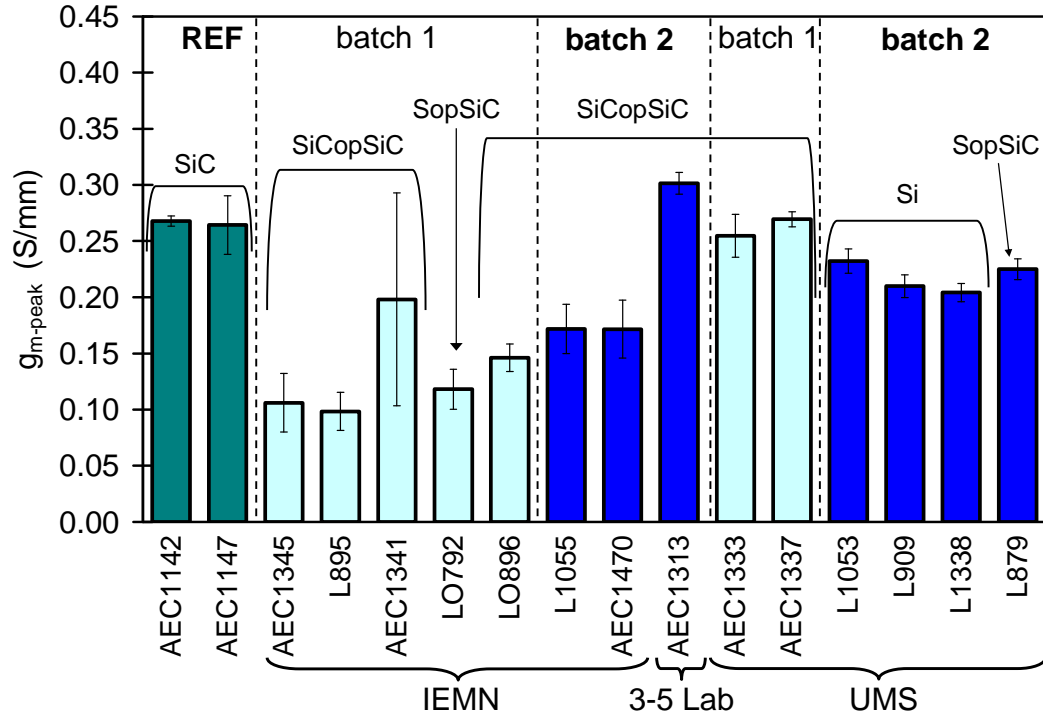
It must be clarify that each bar present in these figures represents the average value of at least five measured devices. Each mean value is also accompanied by the relatively error bar, which shows variability of the measurements carried out in the set of similar devices. Analyzing these DC measurements, we can observe that:

- 1) The saturated drain current density of the composite substrate devices developed in the 2<sup>nd</sup>-batch (see Fig. 2.4) have reached a value of about 0.80 - 0.85 A/mm (3-5 Lab AEC1313, UMS L879). This  $I_{DSS}$  value is approaching the value obtained by the reference SiC devices (around 1.1 A/mm). It is worth noticing that  $I_{DSS}$  for silicon substrate devices is limited to about 0.4 – 0.5 A/mm;
- 2) Very good levels of transconductance have been reached with 2<sup>nd</sup>-batch devices. At  $V_{DS} = 10$  V,  $g_m$  of 3-5 Lab AEC1313 devices is approximately 0.3 S/mm, that is well in line with the 0.26 – 0.27 S/mm of reference devices (see Fig. 2.5);
- 3) Concerning the gate leakage current, the devices processed by IEMN shows very low values (in general less than 100  $\mu$ A/mm measured at  $V_{GD} = -20$  V) while the devices developed by UMS show a larger gate leakage current (about 1 mA/mm). Devices processed by UMS still suffer from a relatively high gate leakage current (see Fig. 2.6);
- 4) The threshold voltage of the devices developed within HYPHEN is very uniform in the  $-3 \div -4$  Volts. The reference devices show in general a more negative  $V_{TH}$  ( $-5 \div -6$  Volts). It must be taken into account that reference wafers are characterized by a thicker AlGa<sub>0.2</sub>N layer in respect to HYPHEN devices (25 nm instead of 22 nm), that can explain the higher  $|V_{TH}|$  values (see Fig. 2.7).

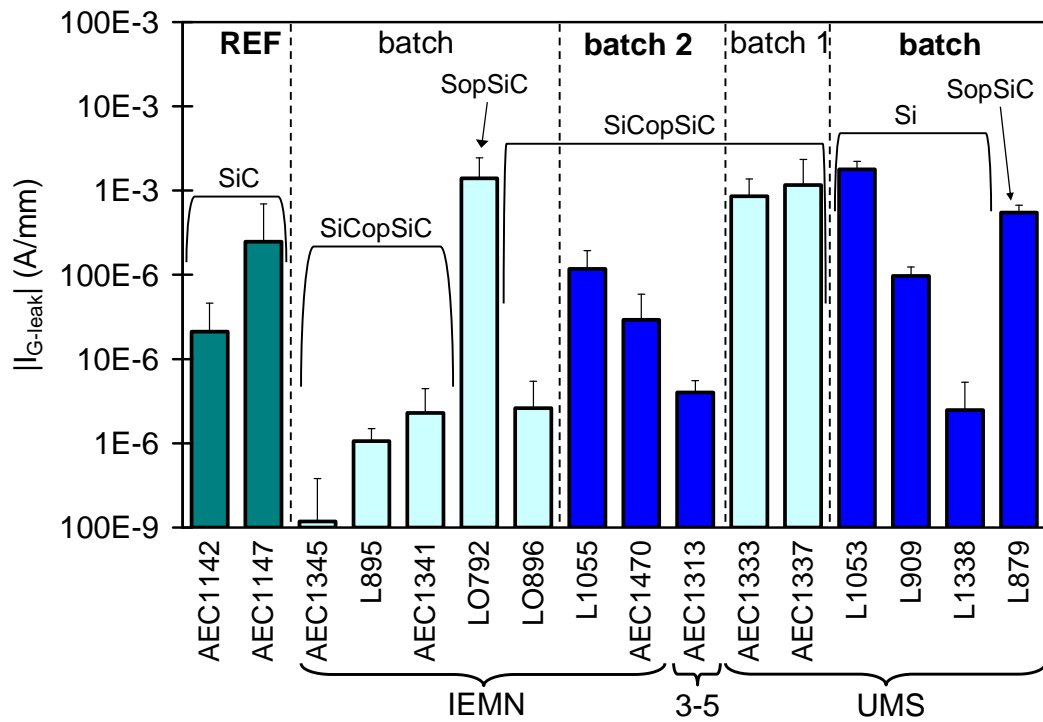
In Appendix I, a selected set of DC measurements carried out on some representative devices is reported as a reference.



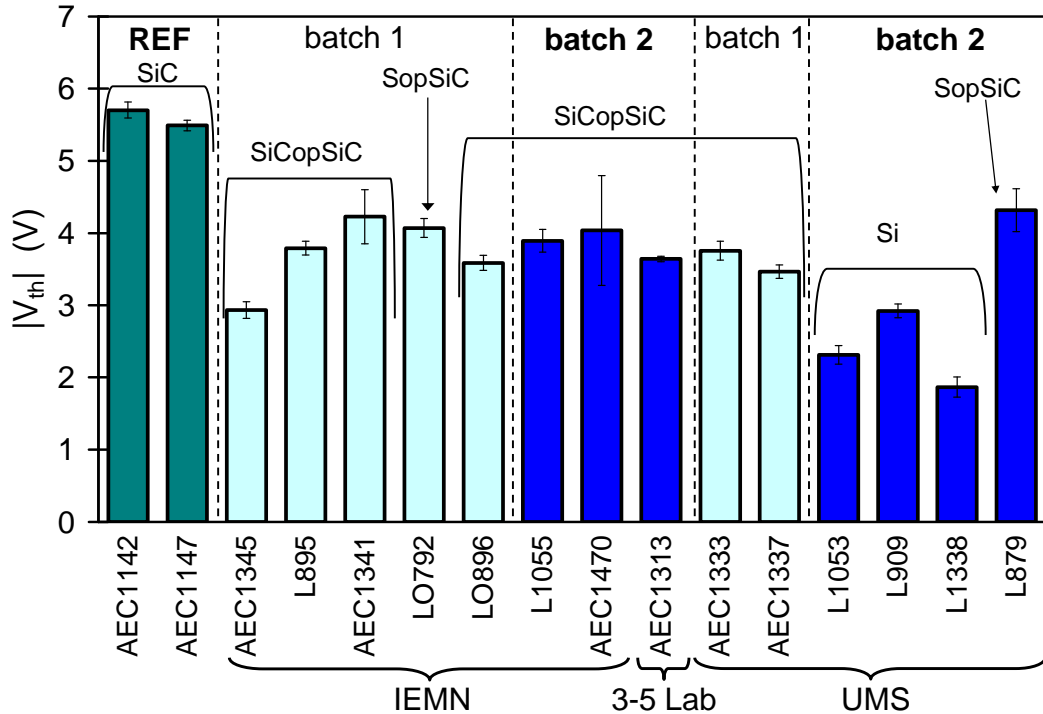
**Fig. 2.4:** saturated drain current ( $I_{DSS}$ ) measured at  $V_{DS} = 10$  V and  $V_{GS} = 0$  V, both for REFERENCE devices and for HYPHEN devices.



**Fig. 2.5:** transconductance peak ( $g_{m-peak}$ ) at  $V_{DS} = 10$  V both for REFERENCE devices and for HYPHEN devices.

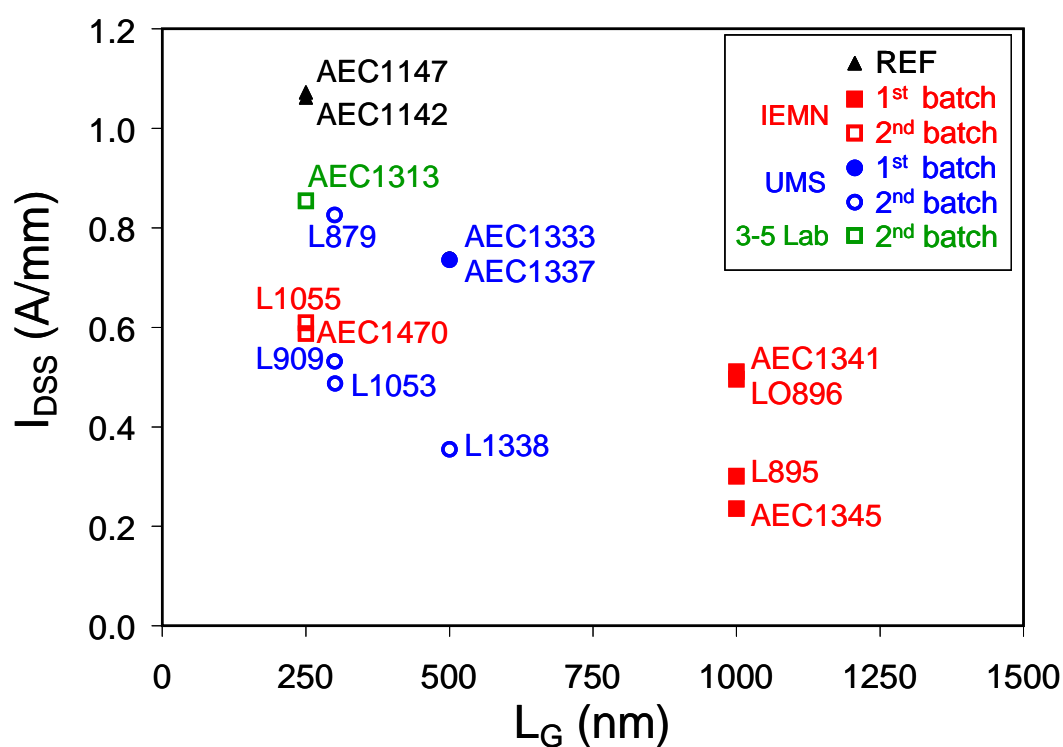


**Fig. 2.6:** absolute gate-leakage current ( $|I_{G-leak}|$ ) measured at  $V_{GD} = -20$  V both for REFERENCE devices and for HYPHEN devices.



**Fig. 2.7:** absolute threshold voltage ( $|V_{TH}|$ ) measured at  $V_{DS} = 10$  V both for REFERENCE devices and for HYPHEN devices.

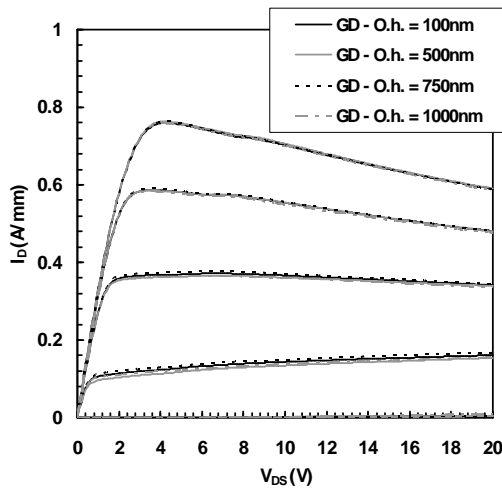
In order to correctly analyze data reported in previous figures, it must be carefully taken into account all the geometrical dimension and layer structures of the investigated devices. Here an example of how these parameters can affect the devices performances is reported: the gate length of the device is strongly affecting the maximum current density as well as the transconductance peak. Fig. 2.8 is clearly showing this aspect, and the scaling of the saturated drain current is present both in the reference devices as well as in the devices processed in the substrates developed within HYPHEN. This result suggests that the current level obtained in the devices processed on SiCopSiC substrate is well in line with the current level obtained in devices processed on reference substrates.



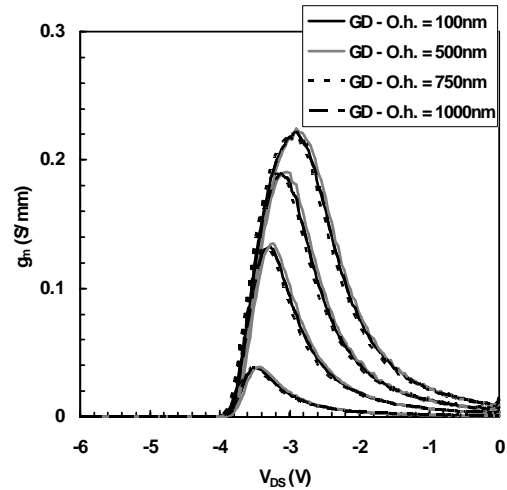
**Fig. 2.8:** maximum saturated drain current, measured at  $V_{DS}=10V$  and  $V_{GS}=0V$  plotted as a function of the device gate length both for REFERENCE devices and for HYPHEN devices.

### 2.2.1 Effect of different gate-drain head overhang

The impact of different gate-drain head overhang (GD-O.h.) on DC performances has been also analyzed. The comparison of the  $I_D$  vs  $V_{DS}$  curves extracted on SiCopSiC (UMS AEC1333) devices, with GD-O.h. from 100 nm to 1000 nm, is presented in Fig. 2.9a. Transconductance measurements in linear region (with  $V_{DS}$  from 100 mV to 1 V) of the same devices are reported in Fig. 2.9b. It is clear that different GD-O.h. lengths have almost no impact on the HEMT electrical parameters measured in DC regime. In chapter 2.3.4, it will be showed how, on the contrary, different GD-O.h. lengths can modify the electrical parameters under high electric field (with high  $V_{DS}$  values).



**Fig. 2.9:**  $I_D$  vs  $V_{DS}$  output characteristics at  $V_{GS}$  from  $-6$  V to  $0$  V (step  $1$  V) of SiCopSiC (UMS AEC1333) HEMTs with different gate-drain overhang lengths (100 nm, 500 nm, 750 nm, and 1000 nm).



**Fig. 2.10:**  $g_m$  measurements at  $V_{DS}$  from 100 mV to 1 V (step 300 mV) of SiCopSiC (UMS AEC1333) HEMTs with different gate-drain overhang lengths (100 nm, 500 nm, 750 nm, and 1000 nm).

## 2.3 DYNAMIC CHARACTERIZATION

The not yet established technological process could make GaN HEMTs prone to be affected by several factors that can impair both the performances and the reliability of such devices. For such reasons, DC regime measurements are often insufficient to characterize altogether device performances, whereas pulsed regime characterizations can offer more interesting results.

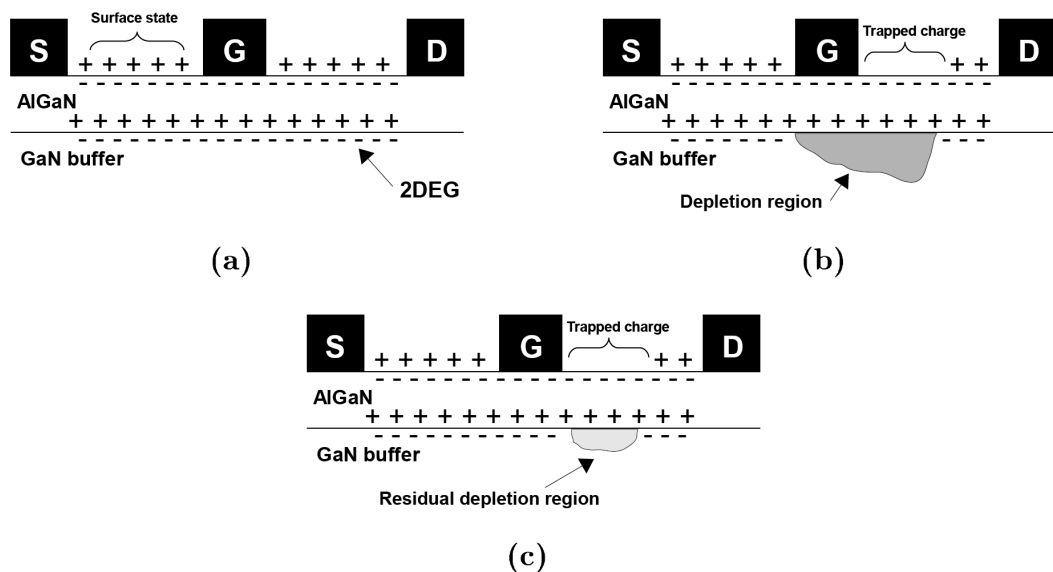
### 2.3.1 Trapping effects: current collapse

The *current collapse* is a large reduction of the device current, which arises when a large voltage RF signal is applied to the gate. If this reduction is observed when the device is pulsed from pinch-off condition to open-channel, then the device is likely experiencing trapping / de-trapping phenomena that are limiting its performance. This effect is detrimental for the RF power performances of HEMTs: the maximum available power results less than that expected from the DC characteristics. Various mechanisms and theories have been investigated in order to explain this effect, but surface traps are generally indicated as the origin of current collapse [22].

For better understanding how trapping and de-trapping of surface states works, a schematic representation of the phenomenon is showed in Fig. 2.19. In the on-state (Fig. 2.19a) the donor-like surface states are positively charged to balance the 2DEG formation; when the device is biased to off-state electrons from the gate are captured by empty surface states causing a decrease of sheet charge density and an extension of the depletion region under the gate (Fig. 2.19b). At the next turn-on (Fig. 2.19c) the drain current grows slowly, since 2DEG is not completely formed yet and the region between gate and source presents a high resistance (this effect is also called “*virtual gate*” in literature). In RF regime the current collapse is more evident: surface trapped electrons cannot be liberated since the long time constant involved in the de-trapping process [23]. In order to reduce the current collapse a passivation layer deposited on the surface can be applied with good results; also adopting field plate (FP) we can improve the RF current response.

The passivation layer, generally formed by silicon nitride ( $\text{Si}_3\text{N}_4$ ), works like a shield that prevents electrons from occupying the surface states; also silicon absorbed during deposition in the AlGaN barrier works like substitute of surface donors [24].

The field plate is a more complex configuration of the gate electrode: it consists in an extension of the gate over the gate-source and gate-drain regions (T-gate), or only over the gate-drain region ( $\Gamma$ -gate). The aim of field plate is to redistribute the electric field between gate and drain: this electric field is responsible of the current collapse since it pulls-out electrons from the gate, charges that are captured by the surface traps. In a traditional structure, the peak of the electric field is located at the edge of the gate, causing a high migration of electrons; with the FP the peak is split into two less intense peaks (one at the edge of the gate and one at the edge of FP) and the electric field results enough weak to not extract electrons from the gate [25].



**Fig. 2.11:** schematic representation of current collapse. (a) On-state: surface donors are positively charged. (b) Off-state: surface donors are electrically neutral because they have captured electrons. (c) On-state: the captured electrons are still causing a persistence of the depletion region.

### 2.3.2 DIVA-like measurements

Trapping effects and current collapse phenomena have been characterized on HYPHEN devices. Generally, the current collapse is no longer a big problem, in

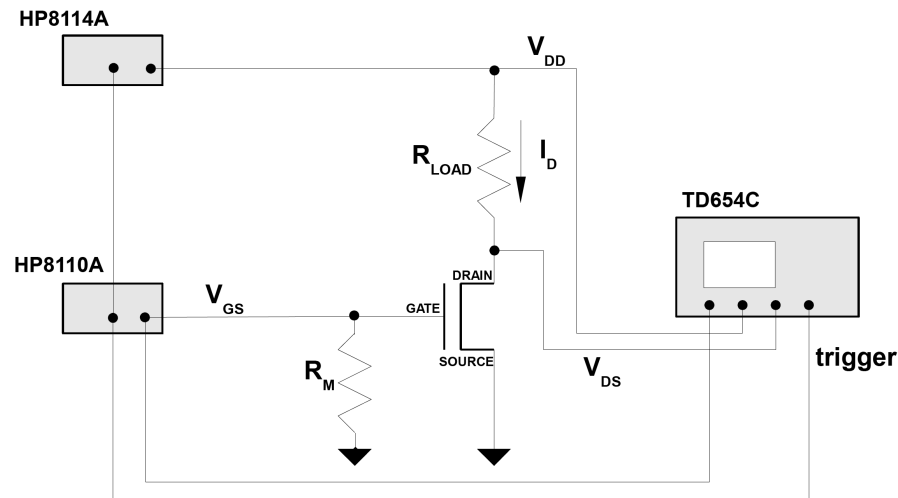
the devices growth on SiC or Al<sub>2</sub>O<sub>3</sub>, if an appropriate passivation layer is deposited on top of the device surface. However, the employment of composite substrates could induce large trap concentration in the different layers, leading to a worsening of the transient response of devices. Therefore, trapping phenomena could still be an issue. The aim of this section is to investigate the trapping phenomena in devices processed on SiCopSiC and SopSiC wafers and, possibly, identify if the adoption of these composite substrates can be responsible of current collapse phenomena formation.

### 2.3.2.1 Measurements setup

Pulsed  $I_D$ - $V_D$  and  $I_D$ - $V_G$  characteristics have been measured by means of a home-made version of the commercial DIVA system [26], to which we refer as DIVA-like system. This double pulser measurement bench comprised an HP8110A pulser, an HP8114A pulser, and a Tektronix TD654C DSO (500 MHz bandwidth, four channels). A LabVIEW interface has been developed to control all the instrumentations and to acquire the data. Measurement setup is shown in Fig. 2.12. The transistor is connected in class-A amplifier configuration with a 50  $\Omega$  resistance load ( $R_{LOAD}$ ). The gate signal ( $V_{GS}$ ) is supplied by HP8110A, also this signal is used as trigger input for HP8114 and for the oscilloscope allowing a perfect synchronization among instruments. The pulsed drain voltage ( $V_{DD}$ ) is supplied by the HP8114A pulser. The oscilloscope measures  $V_{GS}$ ,  $V_{DD}$  and  $V_{DS}$ , from this last measure we obtain the the drain current ( $I_D$ ) with the following equations:

$$I_D = \frac{V_{DD} - V_{DS}}{R_{LOAD}}$$

Pulse width and pulse period were set to 1  $\mu$ s and 100  $\mu$ s, respectively, while three quiescent bias points ( $V_{G\_bp}$ ,  $V_{D\_bp}$ ) were adopted: (0 V, 0 V), ( $V_P$ , 0 V), and ( $V_P$ , 20 V) ( $V_P$  represents a gate voltage lower than pinch-off voltage, i.e.  $V_P = V_{TH} - 1$  V). As largely reported in literature, comparing pulsed  $I_D$ - $V_D$  measurements obtained with a quiescent bias point such as ( $V_{G\_bp}$ ,  $V_{D\_bp}$ ) = (0 V, 0 V) with those obtained by using bias points where the device is held in pinch-off



**Fig. 2.12:** double-pulse measurement home-made setup.  $R_M$  is a resistance of  $50\ \Omega$  used for matching the HP8110A pulser output.

condition, large gate-drain voltages can be used in order to evaluate the presence of trapping phenomena.

### 2.3.2.2 Results

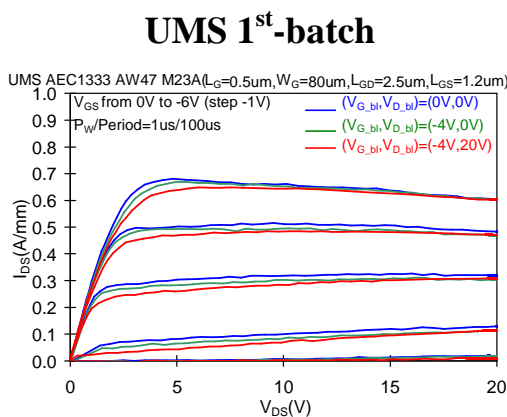
An intensive dynamic characterization on all received wafers, with a conspicuous number of tested devices, has been performed in order to correlate results with device fabrication steps (i.e. substrate, epitaxy, and process).

Pulsed  $I_D$  vs  $V_{DS}$  measurement for UMS AEC1333 (1<sup>st</sup>-batch) and UMS L879 (2<sup>nd</sup>-batch) devices are presented as representative samples in Fig. 2.13 and Fig. 2.14, respectively. A very small current collapse is present in UMS devices. These results are a good representation of the general situation for the devices processed at UMS, which in general are current collapse free.

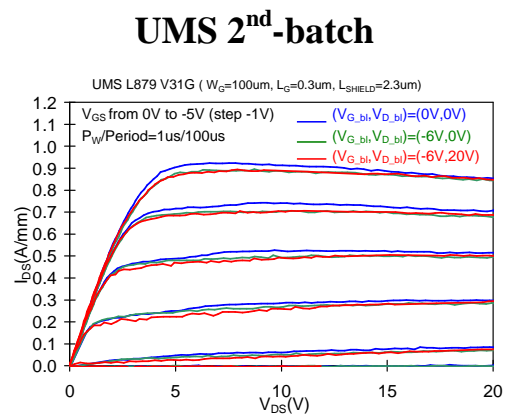
Devices processed in the 1<sup>st</sup>-batch at IEMN had presented very poor dynamic characteristics resulting in very large current collapse. On the other hand, the situation is getting better considering devices of the 2<sup>nd</sup>-batch, which present a rather good improved of the dynamic characteristics. This is clearly a consequence of process optimization and confirms that the composite substrate is not the main responsible of the observed current collapse. In order to clarify this

aspect, dynamic  $I_D$  vs  $V_{DS}$  of representative 1<sup>st</sup>-batch (L895) and 2<sup>nd</sup>-batch (AEC1470) samples are presented in Fig. 2.15 and Fig. 2.16, respectively.

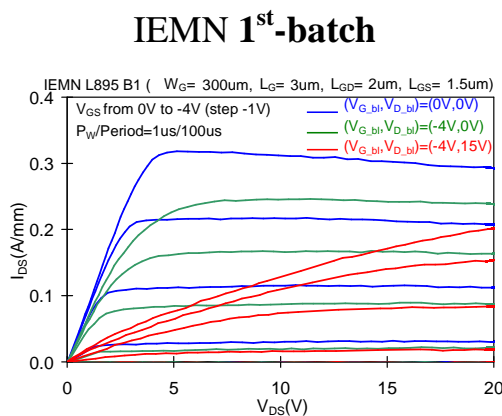
A wafer-by-wafer comparison of dynamic  $I_D$  vs  $V_{DS}$  is summarized in Fig. 2.17. For each wafer, a set of 5-10 devices was tested. Blue bars represent the reference current for each devices since the adopted baseline ( $V_{G\_bp}$ ,  $V_{D\_bp}$ ) = (0 V, 0 V) does not induce any charge trapping, hence these curves are current-collapse free; the green bars represent the collapse observed with the a Gate-Lag condition ( $V_{G\_bp}$ ,  $V_{D\_bp}$ ) = (- $V_P$ , 0 V); while the red bars represent the more severe



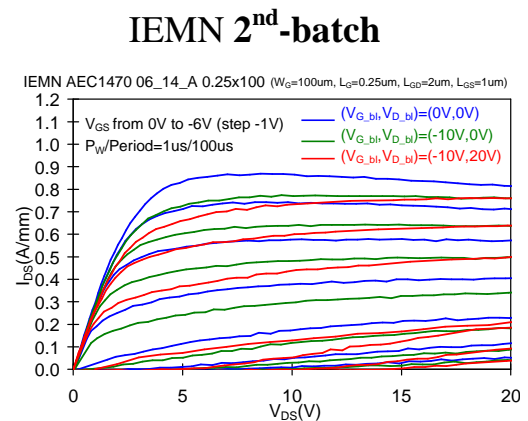
**Fig. 2.13:**  $I_D$  vs  $V_{DS}$  output curves measured in pulsed condition for **UMS AEC1333 AW47 M23A** device. Three different baseline are adopted: blue curve: ( $V_{G\_bl}$ ,  $V_{D\_bl}$ ) = (0 V, 0 V); green curve: ( $V_{G\_bl}$ ,  $V_{D\_bl}$ ) = (-4 V, 0 V); red curve: ( $V_{G\_bl}$ ,  $V_{D\_bl}$ ) = (-4 V, 20 V).



**Fig. 2.14:**  $I_D$  vs  $V_{DS}$  output curves measured in pulsed condition for **UMS L879 V31G** device. Three different baseline are adopted: blue curve: ( $V_{G\_bl}$ ,  $V_{D\_bl}$ ) = (0 V, 0 V); green curve: ( $V_{G\_bl}$ ,  $V_{D\_bl}$ ) = (-6 V, 0 V); red curve: ( $V_{G\_bl}$ ,  $V_{D\_bl}$ ) = (-6 V, 20 V).



**Fig. 2.15:**  $I_D$  vs  $V_{DS}$  output curves measured in pulsed condition for **IEMN L895 B1** device. Three different baseline are adopted: blue curve: ( $V_{G\_bl}$ ,  $V_{D\_bl}$ ) = (0 V, 0 V); green curve: ( $V_{G\_bl}$ ,  $V_{D\_bl}$ ) = (-4 V, 0 V); red curve: ( $V_{G\_bl}$ ,  $V_{D\_bl}$ ) = (-4 V, 15 V).



**Fig. 2.16:**  $I_D$  vs  $V_{DS}$  output curves measured in pulsed condition for **IEMN AEC1470 06\_14\_A** device. Three different baseline are adopted: blue curve: ( $V_{G\_bl}$ ,  $V_{D\_bl}$ ) = (0 V, 0 V); green curve: ( $V_{G\_bl}$ ,  $V_{D\_bl}$ ) = (-10 V, 0 V); red curve: ( $V_{G\_bl}$ ,  $V_{D\_bl}$ ) = (-10 V, 20 V).

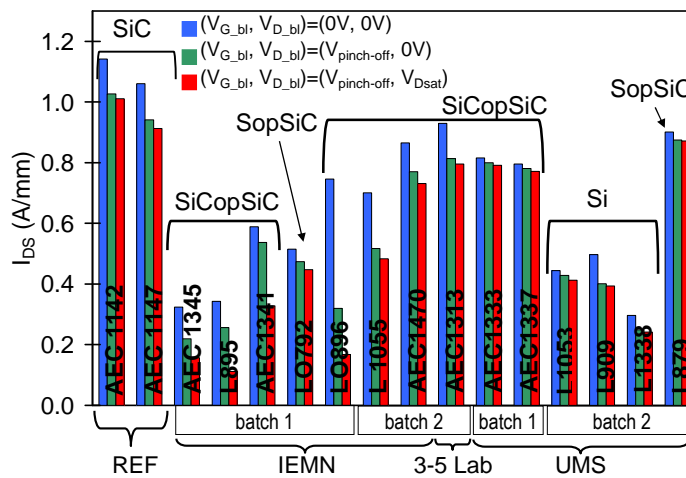
condition of Drain-Lag condition ( $V_{G\_bp}, V_{D\_bp}$ ) = ( $V_P, 20$  V).

In Fig. 2.17 some reference SiC-based devices developed within other European projects where GaN-devices are being developed (KorriGaN) have been also reported. Obviously, the ideal situation would be the case in which the bars are all at the same levels of the blue one (0 V, 0 V). In order to better appreciate the amount of current collapse the index of Slump Ratio (S.R.) has been calculated in tested wafers. S.R. is defined with the following formula:

$$S.R. = \frac{I_{DS0(V_P, 20)}}{I_{DS0(0, 0)}} \quad I_{DS0} = I_D \text{ at } V_G = 0V, V_D = 10V$$

The calculated S.R. are reported in Fig. 2.18: it is clear that UMS wafers are current collapse free. The improving on IEMN dynamic characteristics from 1<sup>st</sup>- to 2<sup>nd</sup>-batch is also clear. Considering all these data, current collapse should not be an issue in the devices adopting the SiCopSiC and SopSiC composite substrates.

Finally, the different drain current collapse behaviors on HYPHEN devices could be correlated with the gate leakage current. It may happen that the same cause, which is responsible for the high gate leakage current on the UMS wafers,



**Fig. 2.17:** pulsed characterizations for three different baselines. Blue bars represent the current levels without collapse (thanks to the appropriate baseline used).

is also responsible for the low drain lag effect on the same wafers. Gate leakage may help to discharge interface traps at (or close to) the semiconductor / insulator interface [27].

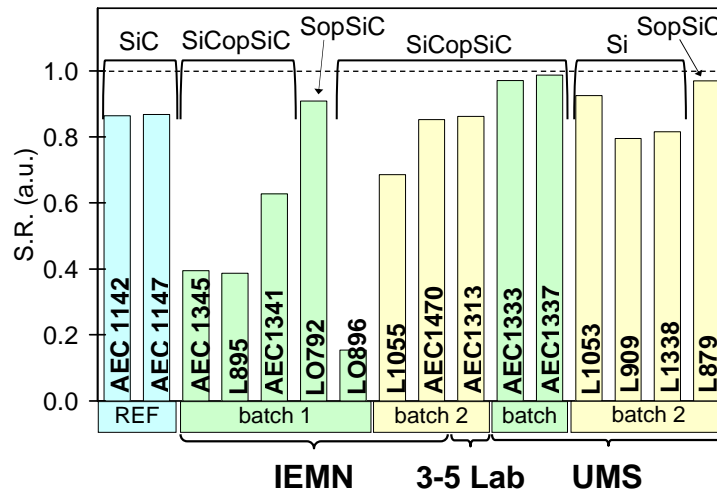
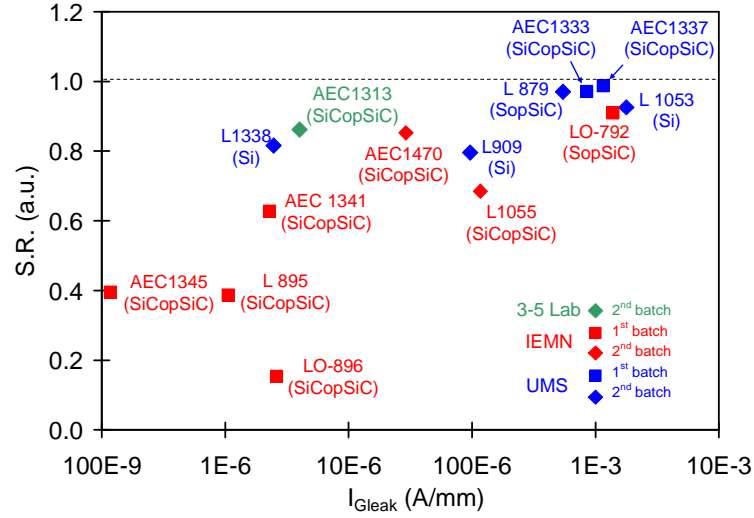


Fig. 2.18: Slump Ratio (S.R.) for measured devices.

UMS devices, that present very good dynamic characteristics, are unfortunately affected by a quite high gate leakage current, as well depicted in Fig. 2.19. Only the L1338 (silicon substrate) is characterized restricted leakage. On the contrary, IEMN 1<sup>st</sup>-batch devices present very low leakage current but with very poor dynamic performances.

The most promising result is represented by both 3-5 Lab AEC1313 and UMS L1338 wafers, that reached a pretty good dynamic behavior accompanied with a very low leakage current level (see Fig. 2.19). In particular, AEC1313 show the better trade off between the Slump Ratio (that is 0.86) and an  $I_{\text{Gleak}}$  current (in the order of  $4 \times 10^{-6}$  A/mm), and at the same time shows drain current values very similar to reference devices.

In Appendix II, a selected set of the dynamic measurements carried out on some representative devices are reported as a reference.



**Fig. 2.19:** correlation between the gate leakage current (x-axes) and the current collapse (SR, Y-axes) in the HYPHEN devices. UMS devices present very low current collapse ( $SR \approx 1$ ) but have, in except of L1338, a quite high gate leakage current ( $\approx 1$  mA/mm). IEMN 1<sup>st</sup>-batch devices have the opposite situation.

### 2.3.3 RF power measurements

As we have seen in the Introduction chapter, the HEMT, with its high current density and operation frequency, is an ideal candidate for microwave power amplifiers. Large-signal Figures Of Merit (FOMs) can be very useful for making preliminary judgments concerning active capabilities. FOMs of particular interest, such as  $P_{out}$  and PAE, are needed to evaluate microwave power performance of the device.

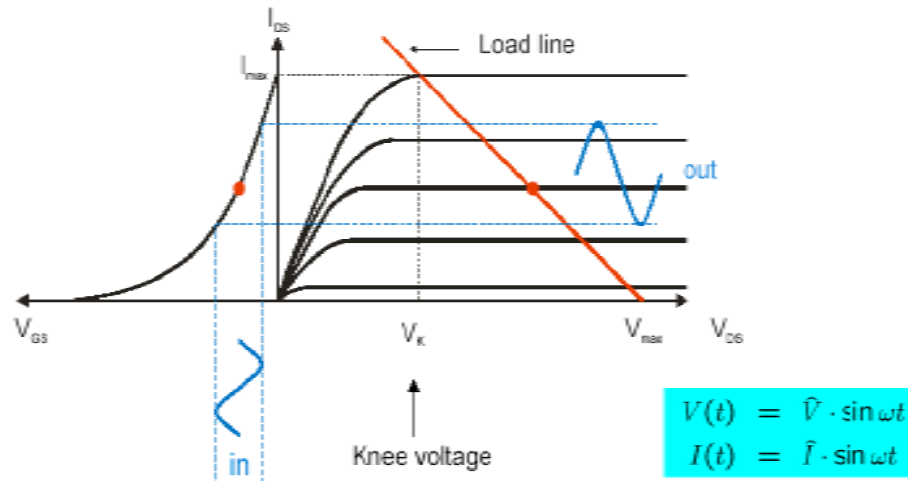
#### 2.3.3.1 Output Power and Power Added Efficiency

For class A operation (see Fig. 2.20), which is the most important class at microwave frequencies, the theoretical maximum output power  $P_{out-max}$  of a HEMT is given by:

$$P_{out-max} = \frac{1}{8} \frac{I_{max} - I_{min}}{V_{max} - V_k}$$

where  $I_{MAX}$  represent the maximum drain current,  $I_{MIN}$  is the minimum drain current due to gate-drain and/or source-drain leakage,  $BV_{DS}$  is the off-state breakdown voltage, and  $V_k$  is the knee voltage. This simple approximation is

graphically presented in Fig. 2.20 in which the HEMT is assumed to operate along its ideal load line, with an adequate large-signal gain.



**Fig. 2.20:** schematic representation of a HEMT operating in class A.

In addition to the  $P_{out}$ , the Power Added Efficiency (PAE) is also an important parameter, which is related to the device power gain for a class A power amplifier as follows:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \frac{P_{out}}{P_{DC}} \left( 1 - \frac{1}{G_a} \right) = \frac{1}{2} \left( 1 - \frac{1}{G_a} \right)$$

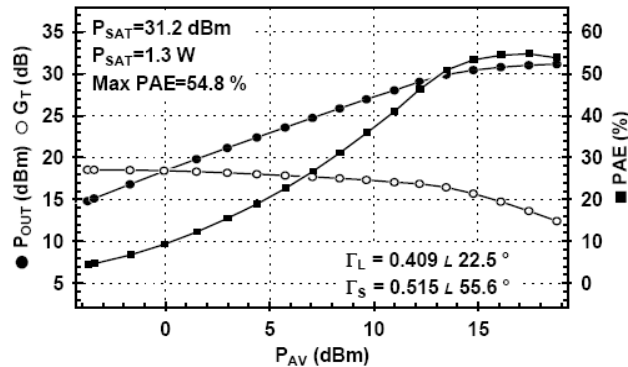
Thus in the lower frequency limit, in which  $1/G_a$  approaches 0, the PAE approaches 1/2 under class A operation.

### 2.3.3.2 Measurements

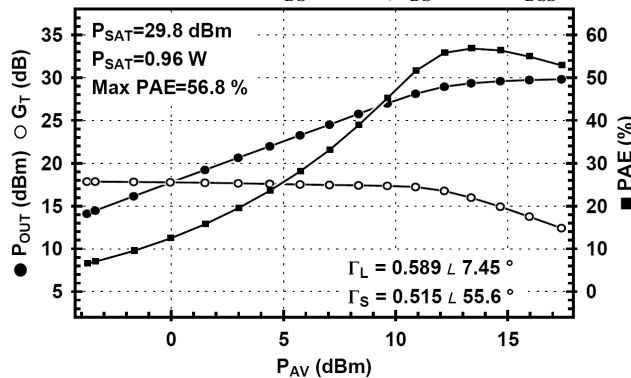
The very promising results obtained from pulsed characterization on 2<sup>nd</sup>-batch devices were confirmed also by RF power measurements, performed into laboratories of the *Università di Modena e Reggio Emilia*, where a Load-pull on wafer system is available. These measurements have been carried out at 2GHz by means of a Load-Pull System based on an Agilent PNA Vector Network Analyzer and a PAF Dragon Load-Pull System. Bias conditions were set to  $V_{DS} = 20$  V and  $I_{DS} = 10\% I_{DSS}$ . Devices belonging to UMS L879 (SopSiC substrate) yielded a continuous-wave power density of about 4 W/mm with peak power added efficiency (PAE) of 54.8%, as shown in Fig. 2.21. Observed performances are

quite remarkable, demonstrating the excellent power capabilities of composite substrate devices.

Devices belonging to UMS L1053 (silicon substrate) yielded a continuous-wave power density of about 3 W/mm with peak power added efficiency (PAE) of 56.8%, as shown in Fig. 2.22.

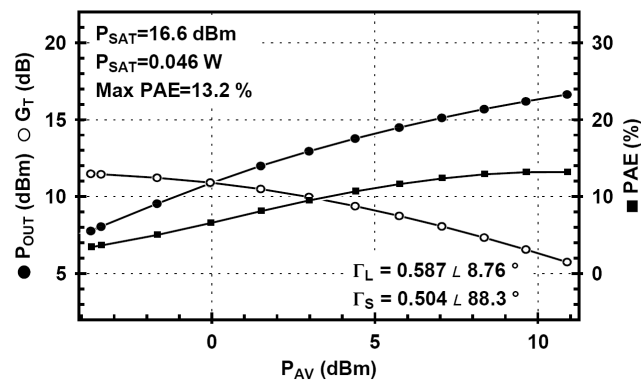


**Fig. 2.21:** RF power measurement at 2 GHz on a  $W_G = 320 \mu\text{m}$  UMS L879 (SopSiC substrate) device. A maximum saturated output power of 4 W/mm and a peak PAE of 54.8% were obtained. Bias conditions:  $V_{DS} = 20 \text{ V}$ ,  $I_{DS} = 10\% I_{DSS}$ .



**Fig. 2.22:** RF power measurement at 2 GHz on a  $W_G = 320 \mu\text{m}$  UMS L1053 (silicon substrate) device. A maximum saturated output power of 3 W/mm and a peak PAE of 56.8% were obtained. Bias conditions:  $V_{DS} = 20 \text{ V}$ ,  $I_{DS} = 10\% I_{DSS}$ .

Some devices that have shown very poor dynamic behavior, i.e. IEMN L895 (1<sup>st</sup>-batch SiCopSiC substrate) devices, were also measured. Obviously, since the DIVA-like characterization has demonstrated very low slump ratio values, the RF behavior is poor as well. In fact, these devices yielded a continuous-wave power density of about one order of magnitude lower with respect to previous ones (0.3 W/mm instead of 3-4 W/mm) with very low peak PAE of only 13.2%, as shown in Fig. 2.23.



**Fig. 2.23:** RF power measurement at 2 GHz on a  $W_G = 300 \mu\text{m}$  IEMN L895 (SiCopSiC 1<sup>st</sup>-batch substrate) device. A maximum saturated output power of 0.3 W/mm and a peak PAE of 13.2% were obtained. Bias conditions:  $V_{DS} = 15$  V,  $I_{DS} = 10\%$   $I_{DSS}$ .

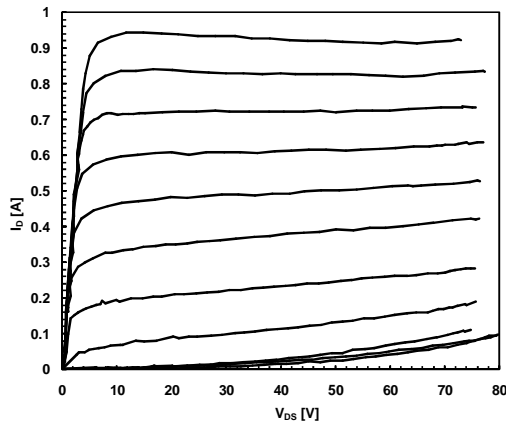
### 2.3.4 TLP measurements

As we have seen in chapter 2.2.1, different gate-drain overhang lengths have not influenced the DC performances of SiCopSiC UMS AEC1333 devices. On the same devices, a DIVA-like characterization has been performed as well. Even in this case, different GD-O.h. lengths have not influenced the devices behavior in pulsed regime with  $V_{DS}$  values below 20 V. On the contrary, we have seen that gate-drain head overhang length has a strong impact on the device behavior at higher electric field (with high  $V_{DS}$  values).

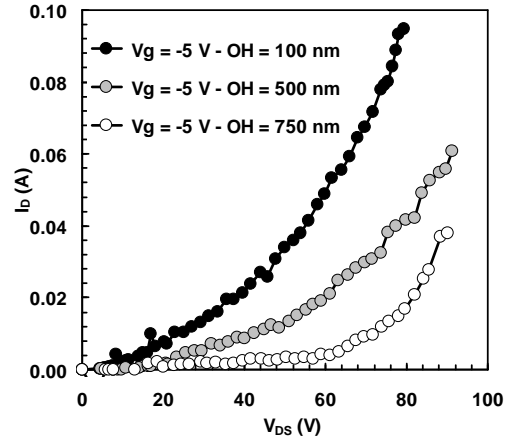
We have adopted a 100 ns Transmission Line Pulser (TLP-TDR) [28] in order to study the behavior of  $W_G = 1$  mm devices at high voltage and high current regimes. TLP technique is adopted as traditional method to evaluate the reliability of devices under ESD-like events, but it can also be adopted to characterize devices under high voltage and/or high current pulses. An ad hoc developed setup was employed in order to stabilize the applied gate voltage during the test, avoiding strong capacitive coupling between drain and gate induced by the fast-slope pulse.

The  $I_D$  vs  $V_{DS}$  characteristics of a 100 nm long gate-drain overhang SiCopSiC device (UMS AEC1333) with  $V_{DS}$  up to about 75 V are reported in Fig. 2.24. The device exhibits some short-channel effect, but, at  $V_{GS}$  near to the pinch-off voltage and  $V_{DS}$  higher than 30 V, output curves change their linear slope going to assume an exponential behavior. We have seen that this behavior is strongly gate-drain

head overhang length dependent. Fig. 2.25, shows  $I_D$  vs  $V_{DS}$  curves, measured at  $V_{GS} = -5$  V, of  $W_G = 1$  mm devices with GD-O.h. lengths respectively of 100 nm, 500 nm, and 750 nm.

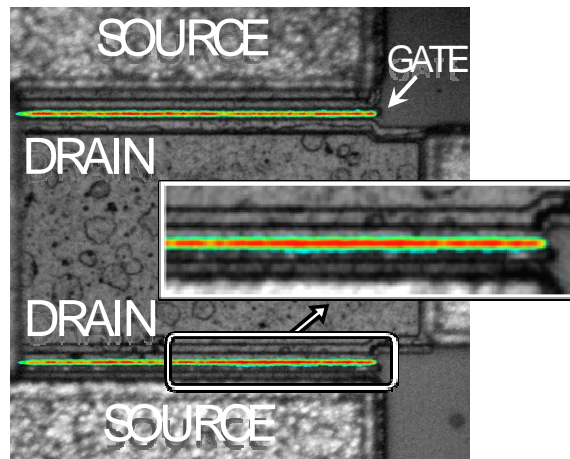


**Fig. 2.24:** I-V curves in 100 ns-TLP regime of a UMS AEC1333 SiCopSiC HEMT with  $W = 1$  mm, gate-drain head overhang length = 100 nm. Gate bias:  $0 \text{ V} \leq V_{GS} \leq 6.5 \text{ V}$ , step 0.5 V.



**Fig. 2.25:** I-V curves in 100 ns-TLP regime comparison with different GD O.h. lengths (100 nm, 500 nm, 750 nm). Device width  $W = 1$  mm.  $V_{GS} = -5$  V.

In order to better investigate this behavior, Emission Microscopy measurements (EMMI) have been performed on several devices, by means of a Hamamatsu PHEMOS-200 emission microscope. The emission image of a  $W_G =$



**Fig. 2.26:** emission image measured in pulsed regime (UMS AEC1333 - SiCopSiC). Bias conditions:  $V_{GS} = -3.5$  V,  $V_{DS} = 75$  V, pulse width = 100 ns, frequency = 10 kHz, 5 min long emission, magnification = 1000x. The inset shows a detail of the uniform emission between drain and gate.

1 mm device at high drain voltage value in pulsed regime condition ( $V_{GS} = -3.5$  V,  $V_{DS} = 75$  V, 100 ns long pulses, frequency = 10 kHz, 5 min long integration) is showed in Fig. 2.26. Emission analysis has shown a good current uniformity along the gate fingers, but at the same time, reveals itself to be not sufficient to explain the change of slope of the I–V curves.

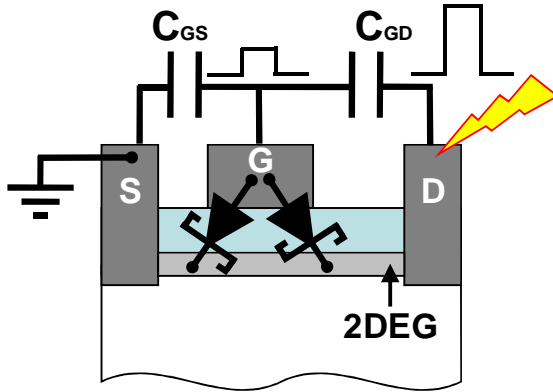
## 2.4 BREAKDOWN CHARACTERIZATION

The robustness of SiCopSiC and SopSiC devices under short pulses applied between Drain and Source, in floating Gate condition has been tested by means of a 100 ns Transmission Line Pulser (TLP-TDR). As already measured in our labs for HEMT devices grown on conventional substrates in 2007 [28], and demonstrated by these devices, the fast rise time of the TLP pulse applied to the Drain pad induces a strong capacitive coupling to the Gate contact.

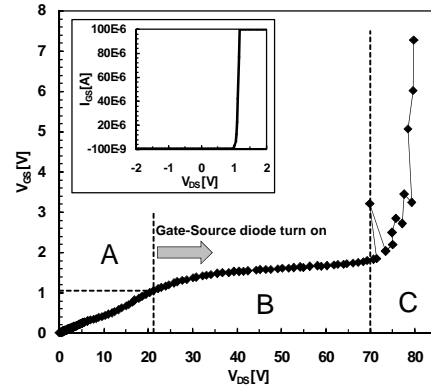
A schematic representation of the parasitic capacitors between gate and drain ( $C_{GD}$ ), and between gate and source ( $C_{GS}$ ), and the intrinsic gate-to-drain and Gate-to-Source Schottky diodes of a typical HEMT structure is presented in Fig. 2.27. Adopting an extended TLP system, Tazzoli et al. [28] have monitored the gate voltage during the TLP stress applied to the drain of a typical HEMT structure (SiC substrate), with the gate floating, and (relatively) high voltage values at the gate contact have been measured. In fact, due to the fast rise time of the TLP system (below 1 ns), the floating gate can easily follow the drain voltage, reaching high voltage values.

Fig. 2.28 shows the increase of the floating gate voltage with the increase of the  $V_{DS}$  applied by the TLP stress. Each point has been extracted making an average of the end part of the  $V_{GS}$  waveform, like traditional voltage and current values extraction. As shown in Fig. 2.28, the behavior of the gate voltage coupling can be divided in three different zones (indicated by A, B, and C). In the first zone, the  $V_{GS}$  increases practically in a linear way with the increase of the  $V_{DS}$  applied by the TLP system. When the  $V_{GS}$  reaches about 1 V, the gate-to-source diode turns on (see the insert in Fig. 2.28), draining a part of the current used to charge the capacitor divider  $C_{GD}$ - $C_{GS}$ , and then reducing the voltage reached by the gate. This condition is indicated by the change of slope in the zone B of Fig. 2.28. In the zone (C) another failure occurs. Region (C) can possibly correspond to

the formation of filaments between the gate and drain regions, bringing to an abrupt increase of the gate voltage at every TLP pulse. This coupling aspect is also demonstrated by the “floating gate”  $I_D$  vs  $V_{DS}$  curve reported in Fig. 2.29 for a UMS L879 SopSiC device.

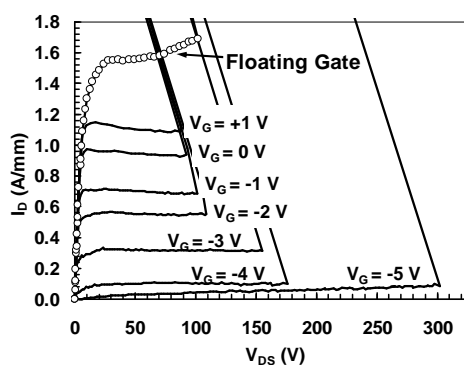


**Fig. 2.27:** Schematic representation of the capacitive coupling between Drain-Gate-Source contacts and the intrinsic Gate-Drain and Gate-Source Schottky diodes.

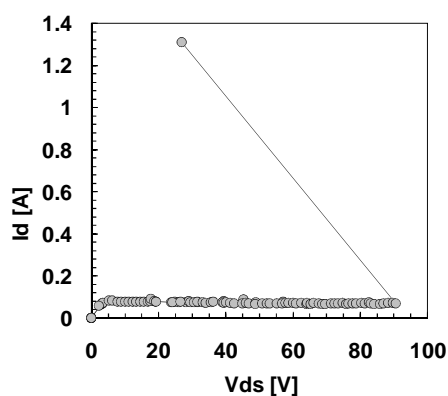


**Fig. 2.28:** Coupled Gate voltage evolution as a function of the  $V_{DS}$  applied with the TLP system (TLP stress between Drain and Source, Gate floating). In the insert, a typical I-V characteristic of the Gate-Source diode is reported, exhibiting a  $V_{TH}$  voltage of around 1V.  $W_G = 1$  mm.

We have made a complete breakdown investigation of devices realized on both the substrates. An example of a  $W_G = 80 \mu\text{m}$  UMS AEC1333 SiCopSiC HEMT is reported in Fig. 2.30. The breakdown condition is here reached at around (90 V, 0.1 A). The breakdown condition is always reached with an abrupt transition to a short circuit condition. Failure analysis has been carried out using optical inspection (see Fig. 2.31) and emission-microscope analysis (see Fig. 2.32), highlighting a filament formation between drain and gate contacts when the breakdown condition is reached. The filament formation is typically followed by the blow up of the zone around the failure. Despite the presence of the air-bridge, it is possible to see in Fig. 2.32 the emission hot spot in correspondence of the filament. Full optical accessible devices have been tested as well, obtaining similar results. These results are comparable to the ESD robustness exhibited by those obtained in SiC and Sapphire based devices (equal width/length HEMT devices processed in the frame of other programs outside this project). The failure

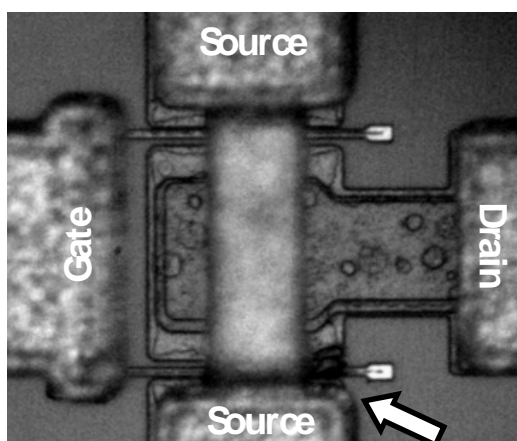


**Fig. 2.29:**  $I_D$  vs  $V_{DS}$  curves in 100 ns TLP regime to evaluate the breakdown points at different  $V_{GS}$ , and floating gate condition in a UMS L879 SopSiC device.  $W_G = 800 \mu\text{m}$ ,  $L_G = 0.5 \mu\text{m}$

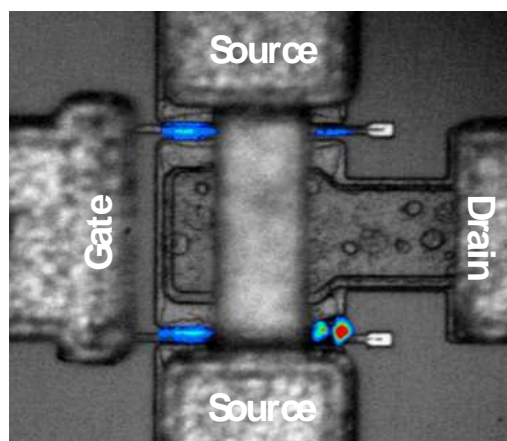


**Fig. 2.30:**  $I_D$  vs  $V_{DS}$  curves in 100 ns TLP regime under floating gate condition.  $W = 80 \mu\text{m}$ ,  $L_G = 0.5 \mu\text{m}$ , UMS AEC1333 SiCopSiC HEMT.

is reached with the formation of filament between drain and gate contacts in all tested samples, and the physical mechanism is currently under investigation.



**Fig. 2.31:** optical microscope image of the device of Fig. 2.30 after the breakdown point was reached. The arrow indicates the damaged zone induced by the filament formation and the successive blow up.



**Fig. 2.32:** emission microscope image of the failed device of Fig. 2.30. Bias conditions:  $V_{GS} = -2 \text{ V}$ ,  $V_{DS} = 15 \text{ V}$ , 10 s long emission, Magnification = 1000x.



# **RELIABILITY OF HYBRID SUBSTRATE DEVICES**

As previously stated, thanks to the material properties, GaN HEMTs can operate at extremely high drain-source voltages. However, since GaN HEMTs already adopt sub-micrometer gate geometries, extremely high electric field values can be reached in the device active area in conventional planar structures that do not use field-plate or recessed-gate technologies. Consequently, charge carriers can reach very high energies (hot electrons), triggering degradation phenomena such as charge trapping, generation of defects and/or deep-level generation, and strain relaxation due to the reverse piezoelectric effect induced by high electric fields.

A section of this work has been dedicated to the study of reliability aspects of hybrid substrates devices. The main objective is to assess material quality through the evaluation of the long-term stability of the electrical and physical characteristics of GaN HEMT devices fabricated on the composite epitaxial substrates, as compared to similar devices made on single crystal substrates.

The two main issues we want to address are the following:

- Identify failure modes and mechanisms of GaN HEMTs developed within the HYPHEN project and correlate them with the different substrates and epitaxy techniques;
- Contribute to the identification of material and process optimization tracks for the improvement of device reliability.

With respect to the state-of-the-art, the main critical issues are:

1. Possible problems can be related with hot carrier injection into semi-insulating SiC substrates; possible different behaviours of SopSiC or SiCopSiC substrates;
2. Impurities present in large quantities in passivation layers or resulting from processing, such as hydrogen or fluorine can also have detrimental effects on device stability, thus requiring ad-hoc testing.

The devices have been submitted to various accelerated tests (on wafer and in package) including thermal storage, ageing under DC bias, hot electron testing. Failed devices will be submitted to failure analysis and results will be compared with data obtained during the material and device characterisation phases.

### **3.1 STEP-STRESS EXPERIMENTS**

#### **3.1.1 Step-stress at $V_{DS}$ up to 30 V**

The setting up of reliability tests on devices that are under development is not an easy task, and often can be a useless work. First of all the correct biasing point must be decided in order to obtain the maximum of information. Clearly, setting up either a too low bias point (leading to zero degradation) or a too high bias point (leading to sudden catastrophic degradation in all devices) can not provide valuable information.

With the aim of well identify the biasing point we have first make use of our heritage obtained in other projects that aim to the development of GaN based devices on SiC substrates (KorriGaN). We have considered devices with similar geometries to those developed within the HYPHEN Project (with a gate length  $L_G = 0.5 \mu\text{m}$ ) that have been submitted to short term stress (10 hrs) at  $V_{DS} = 20 \text{ V}$  and at different  $V_{GS}$  values:  $V_{GSon} = 0 \text{ V}$ ,  $V_{GSoff} = -7.5 \text{ V}$  and  $V_{GSsemi-on} = -5.5 \text{ V}$ .

In order to explain the main difference between these  $V_{GS}$  bias point, a brief summary of different effects is reported in the following:

- a) "ON-state" ( $V_{GSon} = 0 \text{ V}$ ): high drain current, moderately high electric fields, high dissipated power and high junction temperatures are simultaneously present;

- b) “OFF-state” ( $V_{GSoff} = -7.5$  V): the drain current and the dissipated power are close to zero, but the electric field between gate and drain is maximum;
- c) “SEMI-ON-state” ( $V_{GSsemi-on} = -5.5$  V): junction temperature is lower than the ON-state, but the gate to drain electric field is very high, thus allowing channel electrons to reach high energies.

The KorriGaN devices experienced degradation, as shown in Fig. 3.1. Many other reliability tests carried out within the KorriGaN project evidenced device degradations when device were biased around 20 - 30 V.

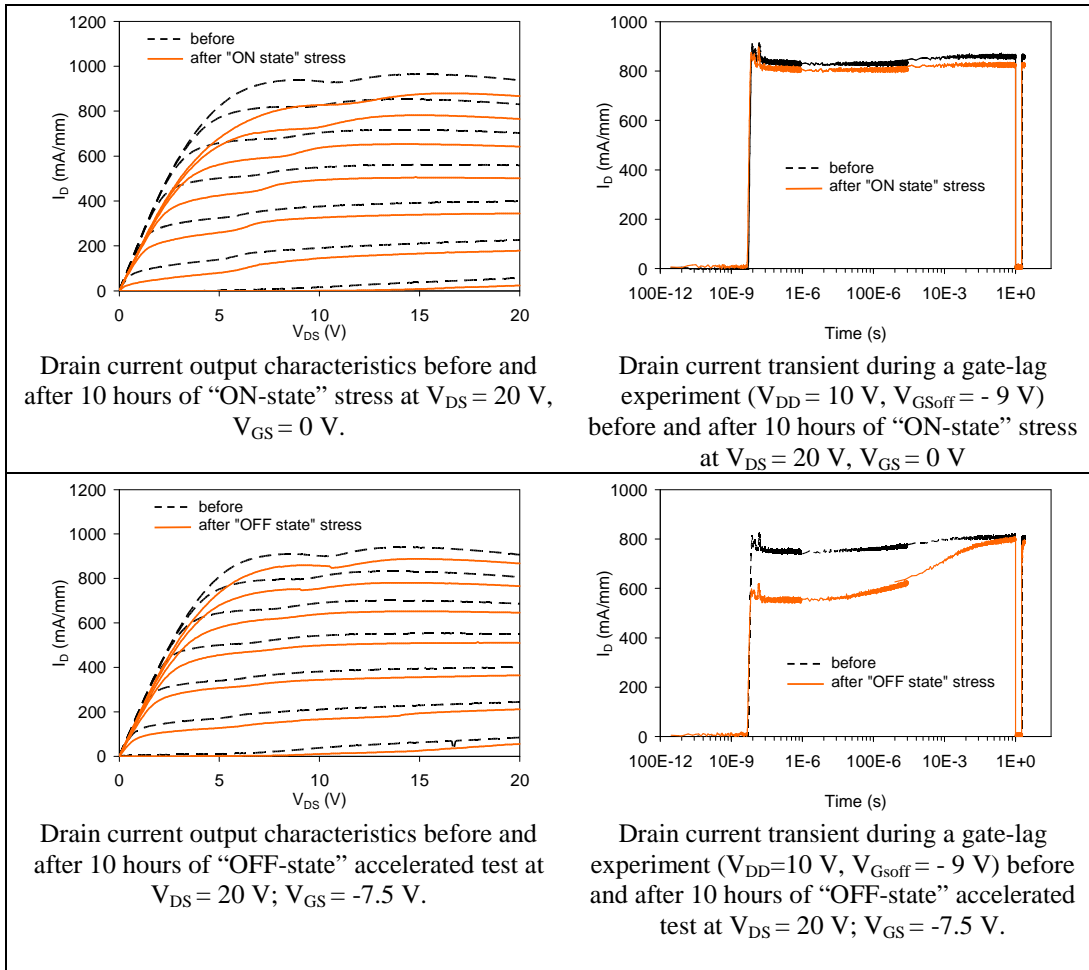
Having in mind that HYPHEN devices could have been more prone to degradation, due to the inherent nature of the composite substrates, “short-term” step-stress test with a maximum drain-to-source voltage of 40 V – 50 V has been carried out on such devices. The results coming out from this test has been adopted for the next “long-term” stress plan.

The step-stress has been organized as follow (see Fig. 3.2):

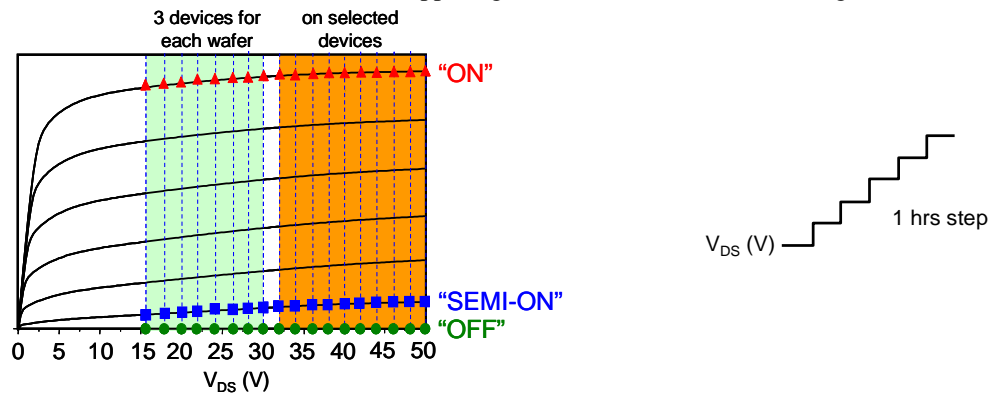
- i. Three gate bias have been adopted:
  - a.  $V_{GS} = 0$  V (ON-state);
  - b.  $V_{GS} = V_{th} - 1$  V (OFF-state);
  - c.  $V_{GS} = V_{th} + 1$  V (SEMI-ON-state).
- ii. For each gate bias, drain bias was stepped from  $V_{DS} = 16$  V to  $V_{DS} = 30$  V, with a  $V_{DS}$  step of 2 V and leaving the device biased for one hour at each  $V_{DS}$  step
- iii. The devices (at least three for each bias point) have been fully characterized at the end of each  $V_{DS}$  step.

Wafers subjected to step-stress with number of tested devices are shown in Table 3.1. Generally, no degradation has been observed during the step stress up to  $V_{DS} = 30$  V in the three  $V_{GS}$  condition on almost all the tested devices. Only UMS AEC1333, UMS AEC1337 and IEMN LO792 were affected by the stress showing large degradation. We have also observed that dynamic behaviour of devices after the stress is not modify either in devices showing degradation after the step stress

as well as in the devices that did not present degradation of the electrical DC characteristics.



**Fig. 3.1:** degradation observed in a KorriGaN GaN HEMT on SiC substrates submitted to two different stress test: a) “ON state” (upper figures) b) “OFF state” (bottom figures)



**Fig. 3.2:** schematic of the step-stress definition. All the devices reported in Table II have been submitted to the step-stress up to 30 V for the three gate bias: i) “ON” state:  $V_{GSon} = 0$  V; ii) “OFF” state:  $V_{GSoff} = V_{th} - 1$  V; iii) “SEMI-ON” state:  $V_{GSsemi-on} = V_{th} + 1$  V. Selected wafers/devices have been submitted to the step stress up to 50 V.

**Table 3.1:** wafer subjected to step-stress experiment ( $V_{DS}$  up to 30V).

Foundry	Wafer	Substrate	Number of tested devices		
			“ON state”	“SEMI-ON state”	“OFF state”
IEMN	L895	SiCopSiC	3 $W_G=100-300\mu\text{m}$ $L_G=1-3\mu\text{m}$	3 $W_G=100-400\mu\text{m}$ $L_G=1-2\mu\text{m}$	3 $W_G=100-300\mu\text{m}$ $L_G=1-3\mu\text{m}$
	LO792	SopSiC	3 $W_G=100\mu\text{m}$ $L_G=2-3\mu\text{m}$	3 $W_G=100\mu\text{m}$ $L_G=2-3\mu\text{m}$	3 $W_G=100\mu\text{m}$ $L_G=2-3\mu\text{m}$
	LO896	SiCopSiC	3 $W_G=100\mu\text{m}$ $L_G=1-3\mu\text{m}$	3 $W_G=100\mu\text{m}$ $L_G=1-3\mu\text{m}$	3 $W_G=100\mu\text{m}$ $L_G=1-2\mu\text{m}$
UMS	AEC1333	SiCopSiC	4 $W_G=80\mu\text{m}$ $L_G=0.5\mu\text{m}$	3 $W_G=80\mu\text{m}$ $L_G=0.5\mu\text{m}$	4 $W_G=80\mu\text{m}$ $L_G=0.5\mu\text{m}$
	AEC1337	SiCopSiC	3 $W_G=80\mu\text{m}$ $L_G=0.5\mu\text{m}$	2 $W_G=80\mu\text{m}$ $L_G=0.5\mu\text{m}$	2 $W_G=80\mu\text{m}$ $L_G=0.5\mu\text{m}$
	L879	SopSiC	3 $W_G=100\mu\text{m}$ $L_G=0.3-0.5\mu\text{m}$	3 $W_G=100\mu\text{m}$ $L_G=0.3-0.7\mu\text{m}$	4 $W_G=100\mu\text{m}$ $L_G=0.5-0.7\mu\text{m}$
	L1053	silicon	3 $W_G=100\mu\text{m}$ $L_G=0.3\mu\text{m}$	3 $W_G=100\mu\text{m}$ $L_G=0.3-0.5\mu\text{m}$	3 $W_G=100\mu\text{m}$ $L_G=0.3-0.7\mu\text{m}$
3-5 Lab	AEC1313	SiCopSiC	2 $W_G=150\mu\text{m}$ $L_G=0.25\mu\text{m}$	2 $W_G=150\mu\text{m}$ $L_G=0.25\mu\text{m}$	2 $W_G=150\mu\text{m}$ $L_G=0.25\mu\text{m}$

A detailed description of stress effects wafer-by-wafer is presented in the following.

**UMS AEC1333 and AEC 1337 (SiCopSiC substrate):** These devices, submitted to “ON state” test condition ( $V_{GS-ON} = 0$  V) presents a strong degradation of the electrical DC characteristics, see Fig. 3.3. Devices present degradation since the first hour of stress at relatively low  $V_{DS}$  (20 V). The degradation was not due to a threshold voltage shift. A degradation of about three orders of magnitude in the gate-to-source diode characteristics was also measured. Regarding the “OFF state” condition, we found that  $I_{DSS}$  present a limited degradation in the knee region while it remains quite unchanged in the other  $V_{DS}$  regions, see Fig. 3.4. Gate leakage currents largely degrade also in the “OFF state” stress, see Fig. 3.4, bottom right. Finally negligible variations in output characteristics were induced

also by “SEMI-ON state” step-stress, see Fig. 3.5. Again the gate leakage current is largely degraded after the stress.

**IEMN L895 (SiCopSiC substrate):** No DC degradations were found after stresses up to 30 V for the three gate bias: i) “ON” state:  $V_{GS-ON} = 0$  V; ii) “OFF” state:  $V_{GS-OFF} = -5$  V; iii) “SEMI-ON” state:  $V_{GS-SEMI-ON} = -3$  V, see Fig. 3.6, Fig. 3.7, and Fig. 3.8. The gate leakage currents remain practically unchanged after treatments. It should be highlighted that these devices were affected by remarkable current collapse (before the stress) as seen in Top-right graphs on Fig. 3.6, Fig. 3.7, and Fig. 3.8. However, it can also be noticed that no worsening of the collapse is seen after the stress. We can hence conclude that the stress did not affect both the static and dynamic I-V characteristics.

*Since the devices that we will analyze will present degradation characteristics similar to the two just described, in the following we will not report the detailed I-V characterization before and after stress. We will refer to Fig. 3.9 and to Table III that summarize the electrical degradation in the tested devices.*

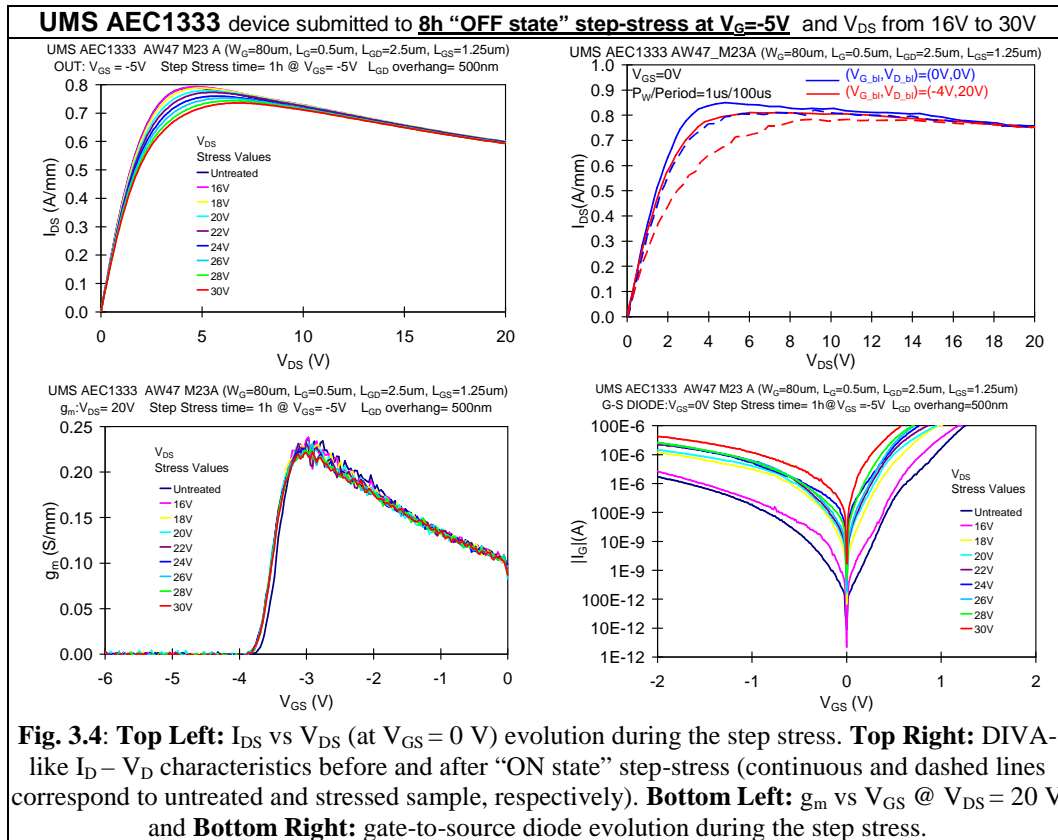
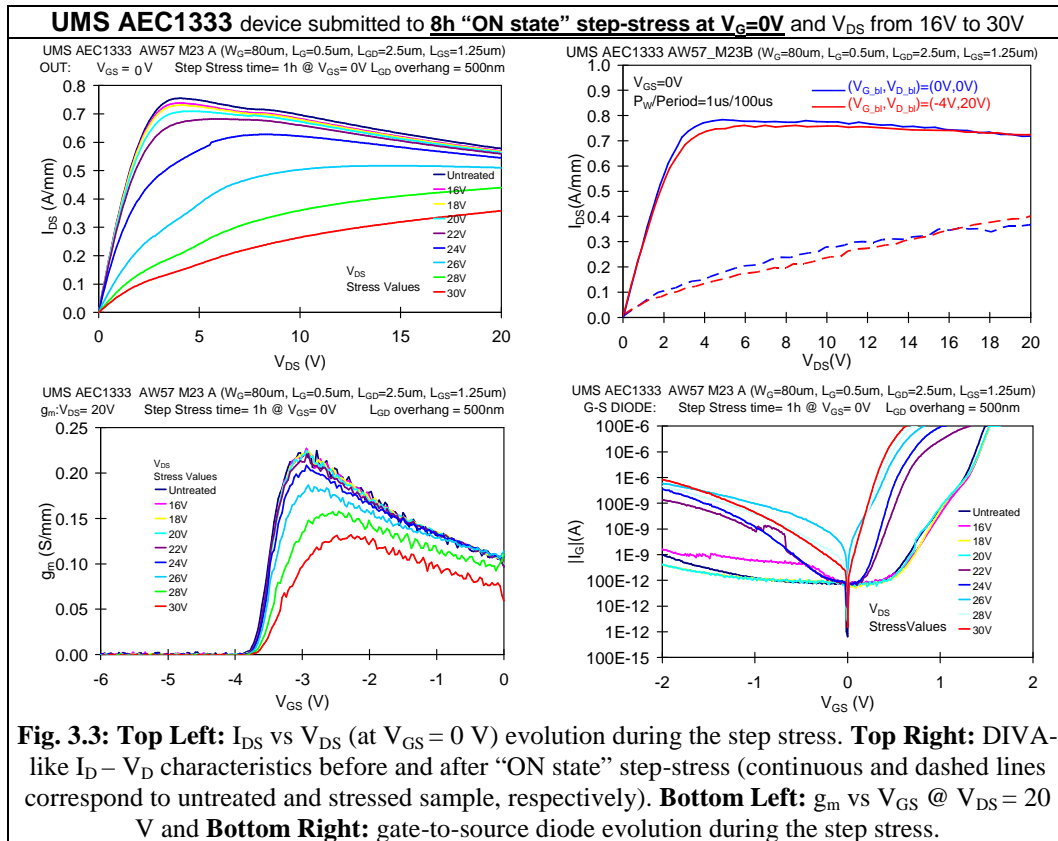
**UMS L879 (SopSiC substrate):** No significant ageing effects were found in terms of  $I_{DSS}$  and  $g_m$ . We must point out that some devices subjected to “ON state” step-stress failed when reaching  $V_{DS-step}$  of about 28÷30 V. Leakage currents were (in some cases) 2x – 3x times greater after stresses. In general a good stability has been observed.

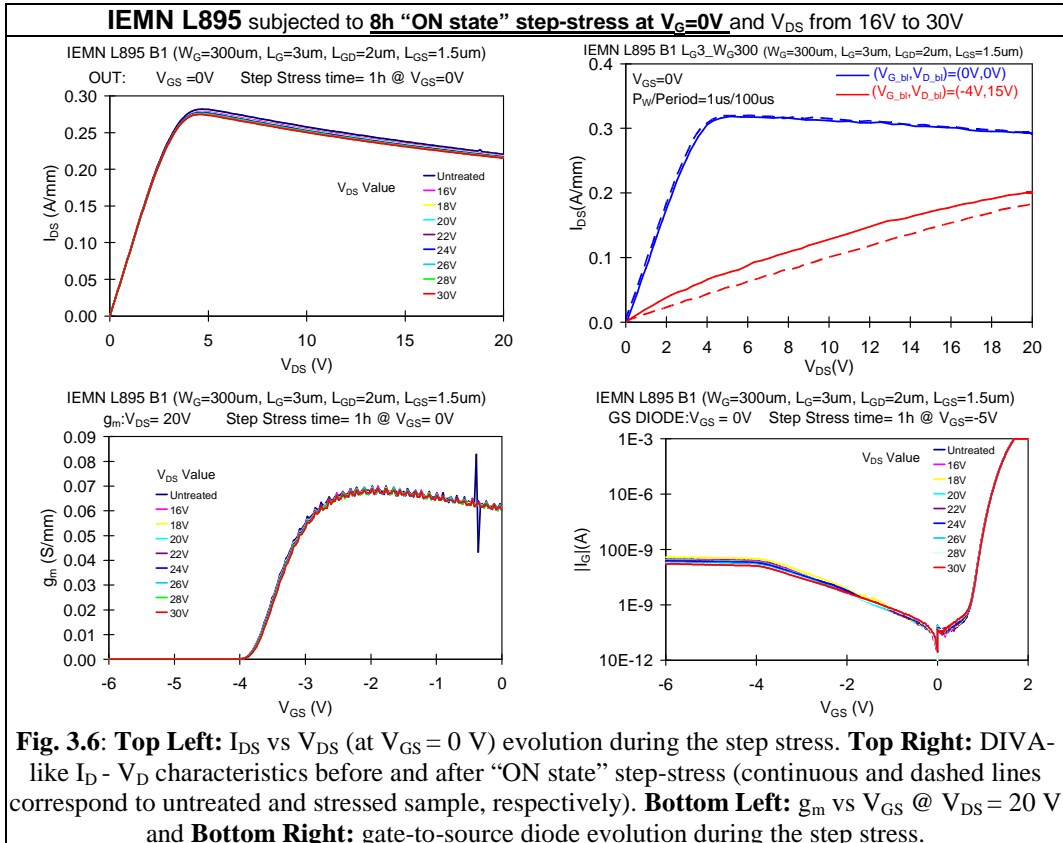
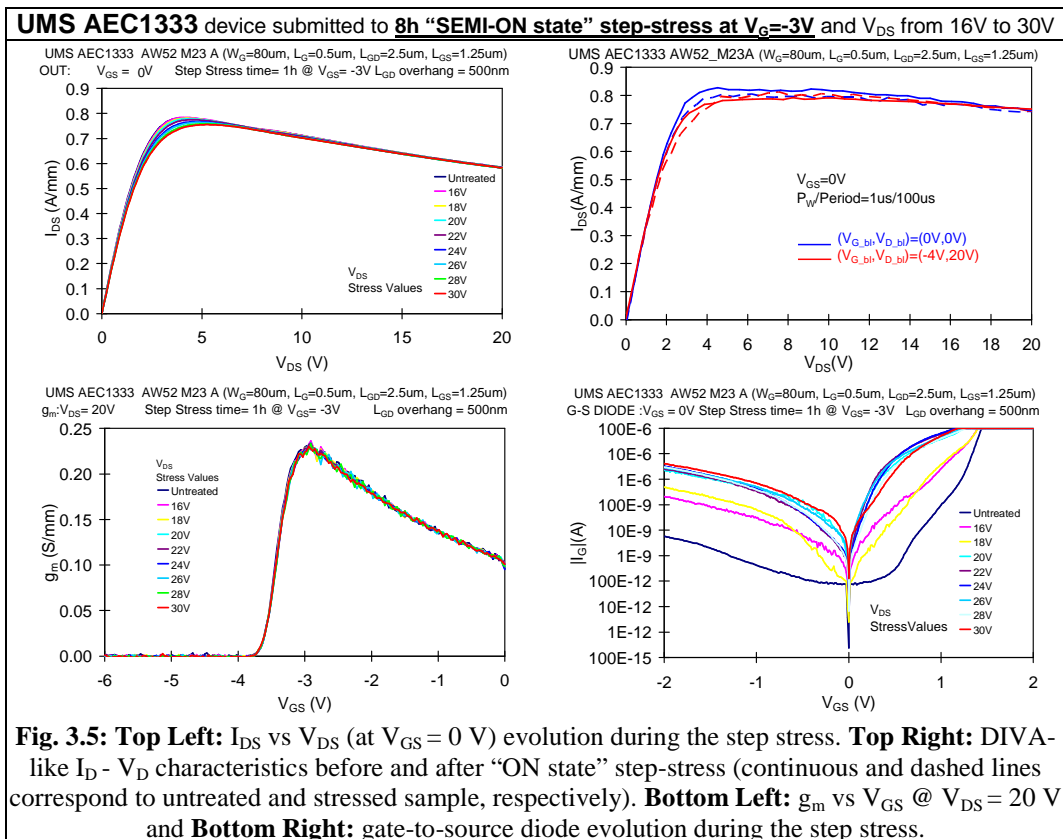
**UMS L1053 (silicon substrate):** Very good reliability performances. No degradations of any parameters were found for  $V_{DS}$  stress voltage up to 30 V.

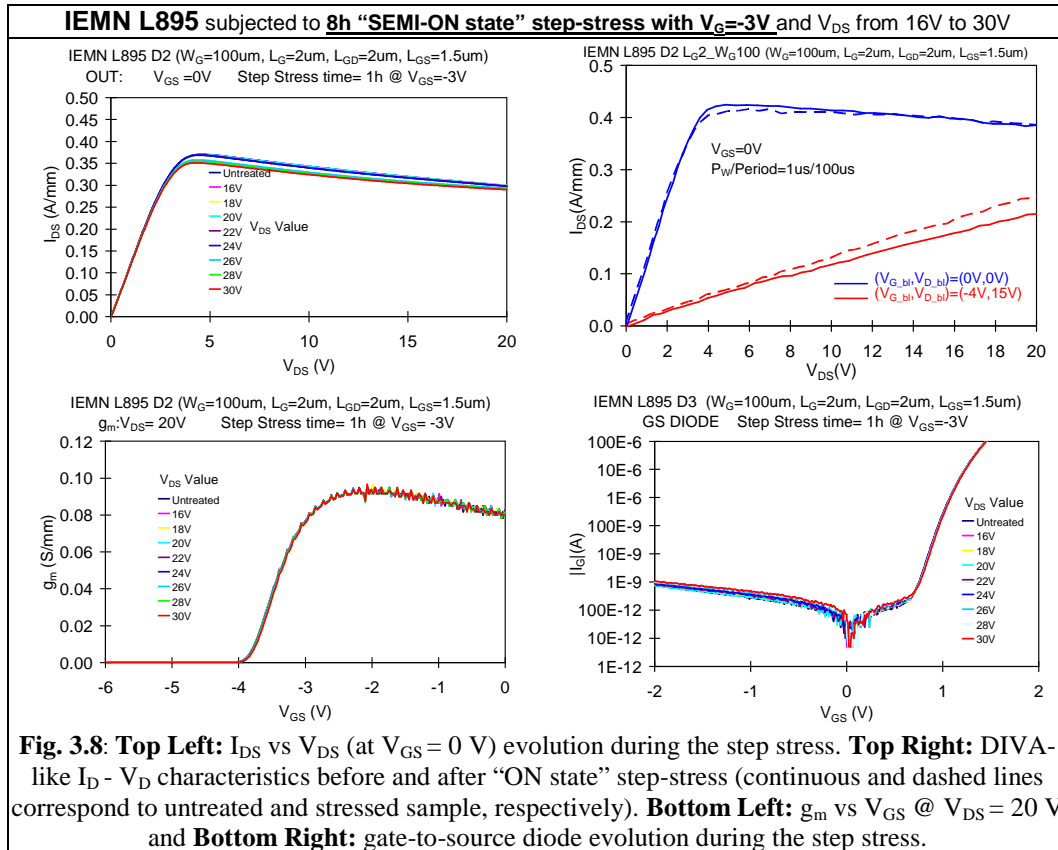
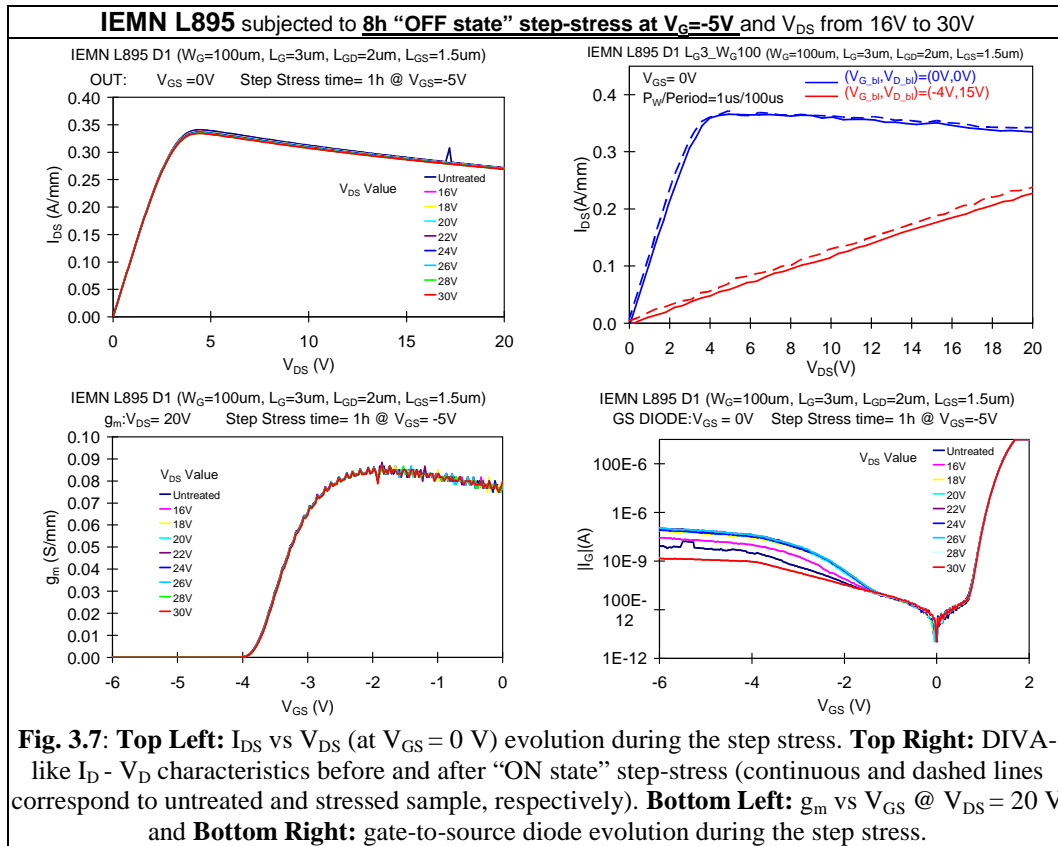
**IEMN LO792 (SopSiC substrate):** Remarkable decrease of  $I_{DS}$  (-50% at  $V_{DS} = 5$  V,  $V_G = 0$  V) after the “ON state” step-stress has been observed. The  $I_{DSS}$  degradation is not due to a threshold voltage shift and (surprisingly) no degradation of the Gate Schottky diode characteristics has been observed.

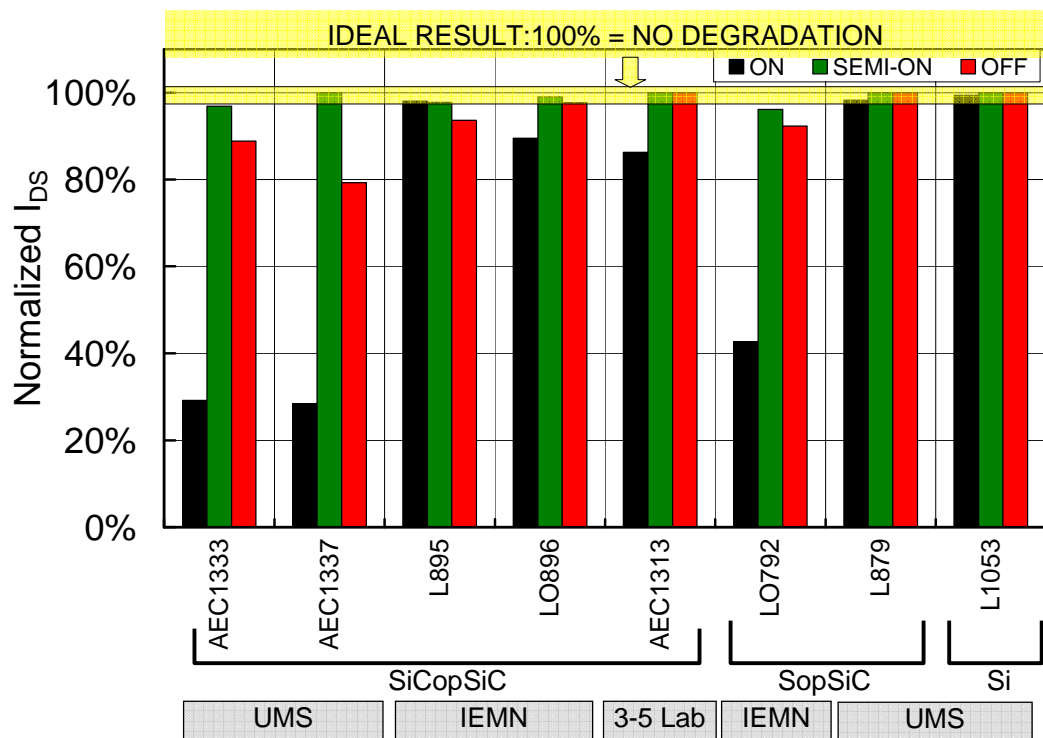
**IEMN LO896 (SiCopSiC substrate):** Only the “ON state” step-stress has caused an anyhow confined worsening in linear and knee regions of output characteristics (-10%  $I_{DS}$  at  $V_{DS} = 5$  V,  $V_G = 0$  V). No DC degradations were found related to “SEMI-ON state” or “OFF state” stresses.  $I_G$  leakage current remained practically unchanged during all the treatments.

**3-5 Lab AEC1313 (SiCopSiC substrate):** No significant ageing effects were found on devices submitted to “SEMI-ON-state” and “OFF-state”, showing a very good stability in these conditions. After “ON-state” stress a ~20%  $I_{DSS}$  reduction has been found.









**Fig. 3.9:** summary of the  $I_{DSS}$  degradation following the step-stress test up to  $V_{DS} = 30$  V for the three gate bias: i) “ON” state:  $V_{GSon} = 0$  V; ii) “OFF” state:  $V_{GSoff} = V_{th} - 1$  V; iii) “SEMI-ON” state:  $V_{GSsemi-on} = V_{th} + 1$  V.

**Table 3.2:** gate leakage variation after stress(measured at  $V_{DS} = 20$  V,  $V_{GS} = -6$  V)

Foundry	Wafer	Substrate	$I_{Gleak-OFF}$ ( $V_{DS} = 20$ V, $V_{GS} = -6$ V) variation before/after stresses		
			“ON state”	“SEMI-ON state”	“OFF state”
IEMN	L895	SiCopSiC	No Degradation		
	LO792	SopSiC			
	LO896	SiCopSiC			
UMS	AEC1333	SiCopSiC	Large Degradation		
	AEC1337	SiCopSiC			
	L879	SopSiC	Limited Degradation (x2-x3)		
	L1053	Si	No Degradation		

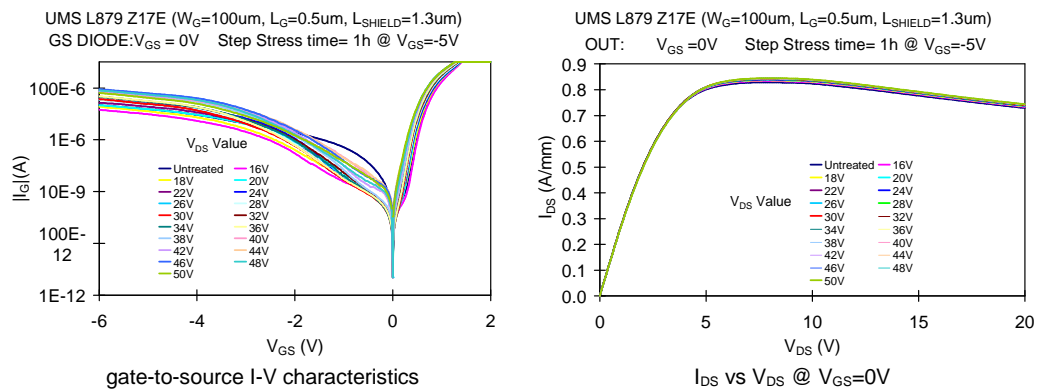
### 3.1.2 Step-stress at $V_{DS}$ up to 50 V

Step-stress experiment was **extended up to  $V_{DS} = 50$  V** for selected devices, in order to extract data regarding higher voltage conditions (see Fig. 3.2), and to definitely define bias conditions for following “long-term” stress tests. This test has been carried out on UMS L879 (SopSiC substrate), on UMS L1053 (silicon substrate), and on 3-5 Lab AEC1313 (SiCopSiC substrate) who have

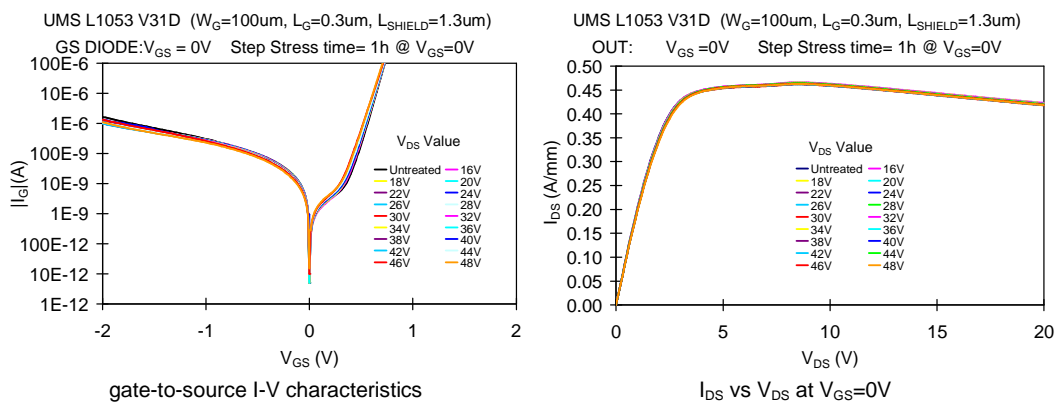
demonstrated very promising electrical characteristics and a fairly good robustness at once during the step-stress test with  $V_{DS}$  up to 30 V.

Although UMS L879 wafer has already failed in “ON state” step-stress at drain-to-source voltage of about 28 V – 30 V, the “SEMI-ON state” and the “OFF state” have been extended to  $V_{DS} = 50$  V. As an example, the gate Schottky characteristic and the  $I_D$  vs  $V_{DS}$  curve at  $V_{GS} = 0$  V, after each step of “OFF state” step-stress, are presented in Fig. 3.10. As can be seen, no significant variations in the main electrical characteristics have been induced by these stresses.

Surprisingly, no evidences of any significant degradation were found on UMS L1053 devices subjected to stresses up to  $V_{DS} = 50$  V in all conditions, demonstrating a very good reliability performance of these devices. It should be mentioned that, during “ON state” stress test L1053 devices failed at  $V_{DS} = 50$  V but no degradations were found up to  $V_{DS} = 48$  V, see Fig. 3.11. This can be easily



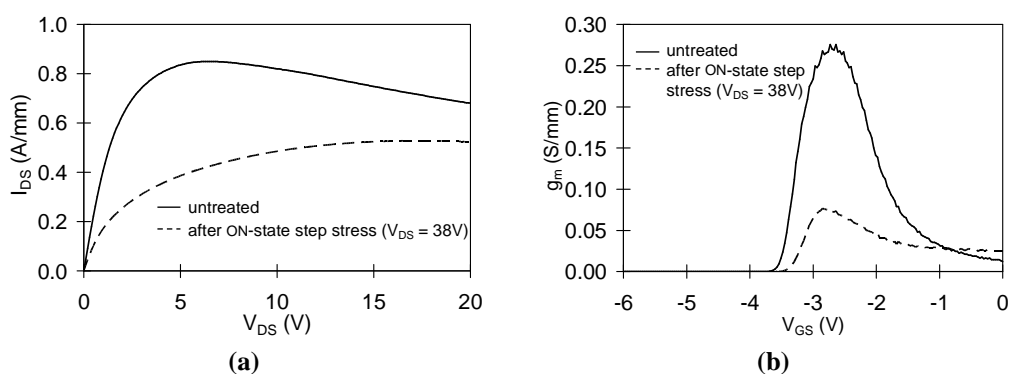
**Fig. 3.10:** UMS L879 Z17E ( $W_G=100\mu\text{m}$ ,  $L_G=0.5\mu\text{m}$ ,  $L_{SHIELD}=1.3\mu\text{m}$ ) subjected to **18h “OFF state”** step-stress with  $V_G=-5\text{V}$  and  $V_{DS}$  from 16V to 50V (2V step)



**Fig. 3.11:** UMS L1053 V31-D ( $W_G=100\mu\text{m}$ ,  $L_G=0.3\mu\text{m}$ ,  $L_{SHIELD}=1.3\mu\text{m}$ ) subjected to **17h “ON state”** step-stress with  $V_G=0\text{V}$  and  $V_{DS}$  from 16V to 48V (2V step). Device failed at  $V_{DS}=50\text{V}$ .

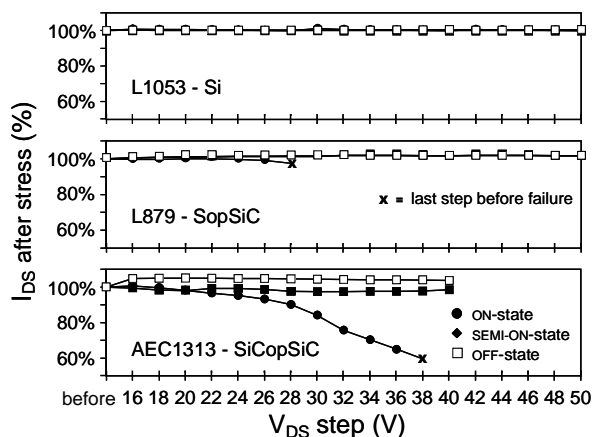
due to the very large power dissipation during the stress, since the junction temperature, during this test was not kept under control.

3-5 Lab AEC1313 devices stressed in “ON-state” also failed at  $V_{DS} = 38 - 40$  V. In this case, we have found a strong degradation of the DC characteristics just before the failure. The  $I_D - V_{DS}$  characteristic measured at  $V_G = 0$  V before and after the  $V_{DS} = 38$  V step of the “ON-state” step-stress is reported in Fig. 3.12(a). The  $g_m - V_G$  characteristics at  $V_{DS} = 1$  V are also reported in Fig. 3.12(b). As for the other two wafers, “SEMI-ON-state” and “OFF-state” step-stress, performed with a maximum drain-to-source voltage of 40 V, have not induced any degradation on AEC1313 devices.



**Fig. 3.12:** (a)  $I_D - V_{DS}$  characteristic at  $V_{GS} = 0$  V and (b)  $g_m - V_G$  characteristic at  $V_{DS} = 1$  V, before and after the  $V_{DS} = 38$  V step of the ON-state short-term step-stress at  $V_G = 0$  V. AEC1313 SiCopSiC devices.

The evolution of  $I_{DS}$ , measured at  $V_{DS} = 10$  V,  $V_G = 0$  V after each step and normalized to the correspondent virgin values, are summarized in Fig. 3.13.



**Fig. 3.13:** short-term step-stress results for UMS L879 (on the top), UMS L1053 (center), and 3-5 Lab AEC1313 (bottom). Evolution of  $I_D$  measured at  $V_{DS} = 10$  V,  $V_G = 0$  V after each step. The “x” represents the last step before failure.

### 3.2 LONG-TERM DC LIFE TEST

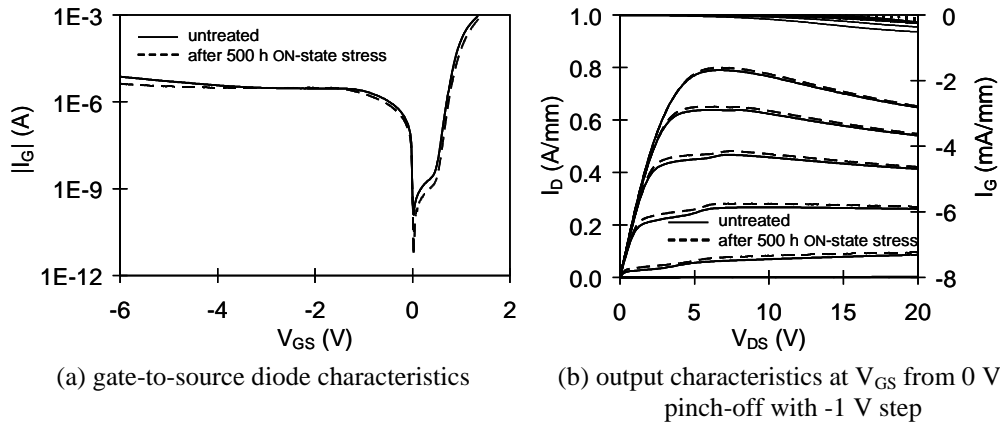
A set of 12  $W_G = 480 \mu\text{m}$  UMS L879 (SopSiC substrate) devices has been finally mounted on EGIDE packages, in order to perform a 1000 hours DC long-term life test. In this test, devices were submitted to an electrical stress combined with a thermal stress. Analyzing step-stress experiment results performed on the same wafer three electrical bias conditions have been selected, in collaboration with UMS: 1)  $I_D = I_{DSS} / 2$  at  $V_{DS} = 15 \text{ V}$  (ON-state); 2)  $I_D = I_{DSS} / 4$  at  $V_{DS} = 30 \text{ V}$  (SEMI-ON-state); 3)  $I_D = I_{DSS} / 16$  at  $V_{DS} = 40 \text{ V}$  (OFF-state). Junction temperature  $T_{\text{junction}}$  of devices during these life tests has been set to  $200 \text{ }^\circ\text{C}$  for both “ON-state” and “SEMI-ON-state”, while  $100 \text{ }^\circ\text{C}$  has been fixed for “OFF-state”. Taking the packaging effect into account,  $R_{\text{th}}$  values in the order of  $15 - 20 \text{ }^\circ\text{C/W}$  were extracted by means of a home-made thermal characterization. A burn-in test bench has been then adopted. This system permits to polarize a transistor at fixed voltages and/or current, and also to fix temperature of the baseplate on which transistors are accommodated. Thermal and electrical details relatively to the different DC life test conditions are reported in Table 3.3.

**Table 3.3:** adopted bias condition for long-term stress

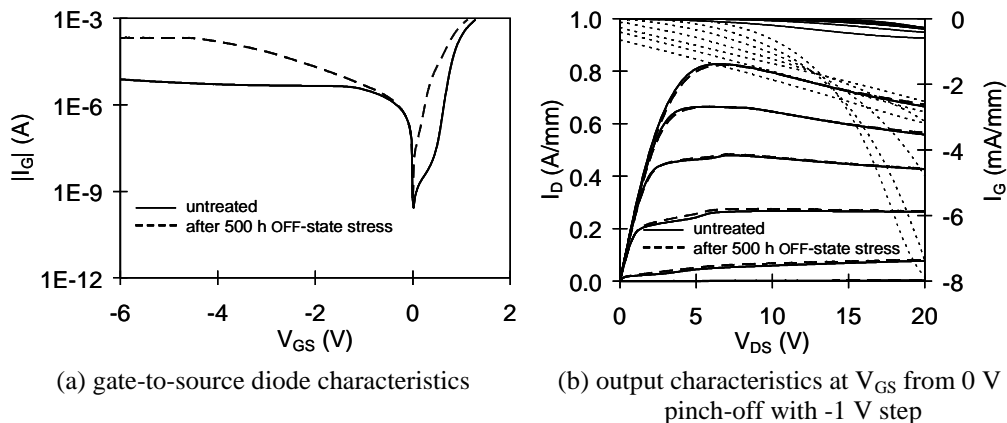
$I_{DSS}$ from PCM	$I_{DSS}$ for DUT	Ref	$V_{DS}$	$I_{DS}$	% of $I_{DSS}$	$P_{DISS}$	$R_{\text{th}}$	Baseplate temp	$T_{\text{junction}}$
(A/mm)	(A/mm)	///	(V)	(A)	(%)	(W)	( $^\circ\text{C/W}$ )	( $^\circ\text{C}$ )	( $^\circ\text{C}$ )
0.8	0.384	1)	15	0.195	50.781	2.925	20	140	198.5
		2)	30	0.0975	25.391	2.925	20	140	198.5
		3)	40	0.024	6.25	0.96	20	80	99.2

After 1000 h “ON-state” test no ageing effects were found, neither in the  $I_D - V_{DS}$  curves nor in the gate leakage characteristics, see Fig. 3.14. On the contrary, “OFF-state” test has caused a degradation of the gate Schottky diode characteristics, see Fig. 3.15(a), and of the gate leakage current level of about one order of magnitude, maintaining  $I_D - V_{DS}$  characteristics quite the same, see Fig. 3.15(b). This can be due to the large  $V_{GD}$  voltage during the “OFF-state” that, combined with the temperature effect, could affect the stability of the gate Schottky diode. The “SEMI-ON-state” condition, on the contrary, has caused

irreversible damage on the devices submitted to the test. This catastrophic failure of devices was happened at the beginning of the test, at ambient temperature ( $T_{AMB} = 23 \text{ }^\circ\text{C}$ ), just when the stress bias conditions have been applied.



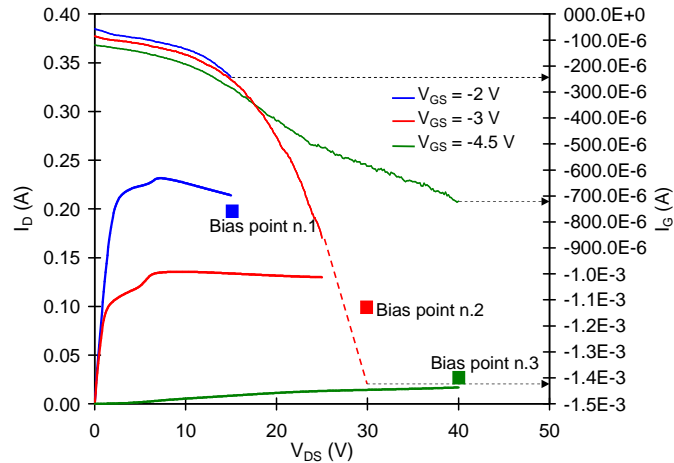
**Fig. 3.14:** DC characteristics, before and after 1000 h of ON-state DC life test at  $I_D = I_{DSS} / 2$  and  $V_{DS} = 16 \text{ V}$ . Junction temperature was kept at  $400 \text{ }^\circ\text{C}$  during the test. UMS L879 SopSiC  $480 \text{ } \mu\text{m}$  devices.



**Fig. 3.15:** DC characteristics, before and after 1000 h of OFF-state DC life test at  $I_D = I_{DSS} / 16$  and  $V_{DS} = 40 \text{ V}$ . Junction temperature was kept at  $200 \text{ }^\circ\text{C}$  during the test. UMS L879 SopSiC  $480 \text{ } \mu\text{m}$  devices.

A possible explanation of devices failure for “SEMI-ON-state” bias point can be found considering the high gate leakage current measured when devices are biased at high drain voltage. In Fig. 3.16 the DC characterization of a device realized at about room temperature is shown. The three squares represent the bias conditions selected for the stress test (blue, red and green are bias point (1), (2) and (3), respectively), while lines represent the  $I_D$  and the  $I_G$  measured near the stress bias condition. Device biased at  $V_{GS} = -2 \text{ V}$  shows low gate current because the drain voltage is limited at  $15 \text{ V}$ ; for higher  $V_D$  the gate current drastically increases:

ideally extending  $I_G$  with  $V_G = -3$  V and  $V_D$  up to 30 V (the dashed red line) it reaches -1.4 mA (about -3 mA/mm). This value could be very detrimental so that the device could not work properly. While at  $V_D = 40$  V and very low drain current ( $V_G = -4.5$  V) the gate leakage current stops at -0.7 mA (-1.5 mA/mm).



**Fig. 3.16:**  $I_D$  vs  $V_D$  and  $I_G$  vs  $V_D$  characteristics for three different  $V_G$  (blue line  $V_G = -2$  V; red line  $V_G = -3$  V; green line  $V_G = -4.5$  V). Stress bias conditions are also indicated in the figure.

These very good reliability results can be used to demonstrate that degradation mechanisms involved in composite substrate devices are not stronger than when using SiC monocrystalline substrate. All these data confirm that the layer transfer based composite substrates are very promising for high performance low-cost RF GaN HEMT structures for power applications.

# PARASITIC EFFECTS IN GAN HEMTS

The present chapter presents the results obtained within the "Parasitic effects" workpackage of the "Reliability" subproject of the KorriGaN project.

## 4.1 KORRIGAN PROJECT

### 4.1.1 Background

KorriGaN is a large-scale European joint Research and Technology Project performed within the EUROPA framework and targeting CEPA2 objectives aiming at the development of microelectronics components. Seven nations are contributing to KorriGaN: France also acting as the Ministry Of Defence management group, Italy, The Netherlands, Germany, Spain, Sweden and the United Kingdom. The KorriGaN consortium consists of 29 partners from the 7 contributing nations providing all the necessary competence in all key areas dedicated to semiconductor technologies such as substrate growth, device processing, circuit design and modeling, circuit packaging and integration.

### 4.1.2 Objectives

The main objective of KORRIGAN is to develop a stand alone European supply chain and capability for GaN HEMT technology which will provide all major European defence industries with reliable state-of-the-art GaN foundries services. For that purpose, there are four major technical objectives:

1. To establish a European supply chain for the manufacture of GaN HEMT devices and MMICs.
2. To assess the reliability and reproducibility of existing GaN device technologies within Europe in order to identify preferred processing options.

3. To demonstrate the technology and the supply chain through the fabrication and testing of selected demonstrators for key S-band, X-band and wide-band applications.
4. To evaluate the benefit of the technology at system level.

#### **4.1.3 Methodologies and work plan**

In order to successfully achieve the project goals and enable the development of leading GaN technology at the horizon of 2009, an integrated methodology has been setup and the project has been organized into 4 subprojects dedicated to materials, device and circuit processing technologies, reliability evaluation, thermal management and packaging solutions. Several demonstrators will be designed to validate GaN technology for various applications: S-band High Power Amplifiers (HPA), X-band and wideband HPA, Low Noise Amplifiers (LNA) and switches.

*A. Materials:* Wideband gap semiconductor substrates will provide the foundation for the GaN HEMT technology. Silicon Carbide (SiC), Sapphire and Silicon materials will be considered, with a stronger focus on the growth of bulk crystal of SiC substrates using High Temperature Chemical Vapor Deposition (HTCVD) techniques. Substrate diameter expansion will be a key issue to ensure the economic maturation and to guarantee cost-effective industrial access to the technology. Also for each material, several types of epitaxial growth using both Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD) techniques will be studied and characterized using a common approach.

*B. Processing:* The development activities will aim at establishing the access to a global manufacturing process of GaN HEMT devices and Microwave Monolithic Integrated Circuits (MMICs) on SiC, Silicon and Sapphire substrates. The work packages will cover the development of main technological aspects of circuit manufacturing including: generic technologies for active devices and passive circuits; design and manufacturing of devices; design and manufacturing

of MMICs; and extraction of models from DC-RF characterisation. A common PCM will be exploited.

*C. Reliability:* The work is focused on the assessment of GaN technology regarding reliability aspects. Work packages will include: the study of parasitic effects, such as current collapse, which result from trapping effects occurring in the substrate; the systematic evaluation of the long-term reliability of GaN HEMT devices and passives; the identification and understanding of failure mechanisms based on the analysis of failed devices; and the evaluation of device robustness to extreme operating regime.

*D. Thermal management and packaging:* The objective of this subproject is to develop the suitable thermal environment for the use and integration of GaN power devices in current systems. The work will address the following issues: the design of optimized thermal cells and the improvement of heat sinking efficiency by reducing the device thermal resistance; the study of advanced assembly solutions and power packages; the simulation of the thermal environment of devices and circuits.

#### **4.1.4 Parasitic effect evaluation**

The goal of "Parasitic effects" workpackage of the "Reliability" subproject of the KorriGaN project was the identification and study of the mechanisms leading to dispersion of the device electrical characteristics as a function of frequency, or to time-dependent anomalies in their I-V characteristics. Two main dispersion effects have been identified and characterized in KorriGaN, namely:

- (a) **“current slump” or “current collapse” effects**, i.e. a decrease of drain current which takes place when the device is pulsed between pinch-off (typically  $V_{DS} = 20$  V,  $V_{GS} = -8$  V) and open channel conditions, with respect to DC or to pulsed  $I_D - V_{DS}$  measurements carried out from the baseline with  $V_{DS} = 0$  V,  $V_{GS} = 0$  V. This current slump obviously reduces the RF power of the devices, and is usually attributed to trapping effects, which can take place at the device surface or within the epi layer

and its interfaces. The highest contribution to current slump usually comes from traps at the surface, as demonstrated by the fact that suitable passivation using SiN or SiO/SiN greatly improves current collapse. Most KorriGaN devices preserve at least 80% of their DC current in pulsed conditions).

- (b) **"kinks" in the I-V characteristics.** This effect consists in a sudden, but small, increase in the drain current, taking place during DC  $I_D$  vs  $V_{DS}$  measurements when a certain  $V_{DS\_kink}$  value is exceeded. This effect is due to extremely slow traps within the epitaxial layers and/or their interfaces, and is not related with the device surface. Independently from the process, devices adopting QinetiQ epitaxy are affected by the "kink" which, however, does not affect significantly power performances.

Exploitable results of the workpackage were the identification of structures, processes and technologies capable of reducing parasitic effects, the development of diagnostic techniques, the correlation between electrical characteristics and device performances and materials' properties. In the following, we will describe these results using the following outline: chapter 4.2 will analyze "current collapse" effects in the various KorriGaN technologies. The paragraph 4.2.1 will describe the experimental techniques adopted for the evaluation of current collapse, will present the results of dispersion measurements as a function of the choice of process, epitaxial layer growth, substrate type and supplier. A methodology for identifying the contributions of surface and epitaxial layer traps will be presented, and validated with the use of two-dimensional numerical device simulations. A circuit model has been developed, which allows one to evaluate the effects of parasitic phenomena on device performances. Results have been correlated with material properties, obtained using Capacitance vs Voltage (C(V)) measurements, Deep Level Transient Spectroscopy (DLTS), photocurrent measurements, cathode-luminescence spectroscopy. Chapter 4.3 summarizes the results of the characterization of the kink effect observed in all devices adopting QinetiQ epitaxy.

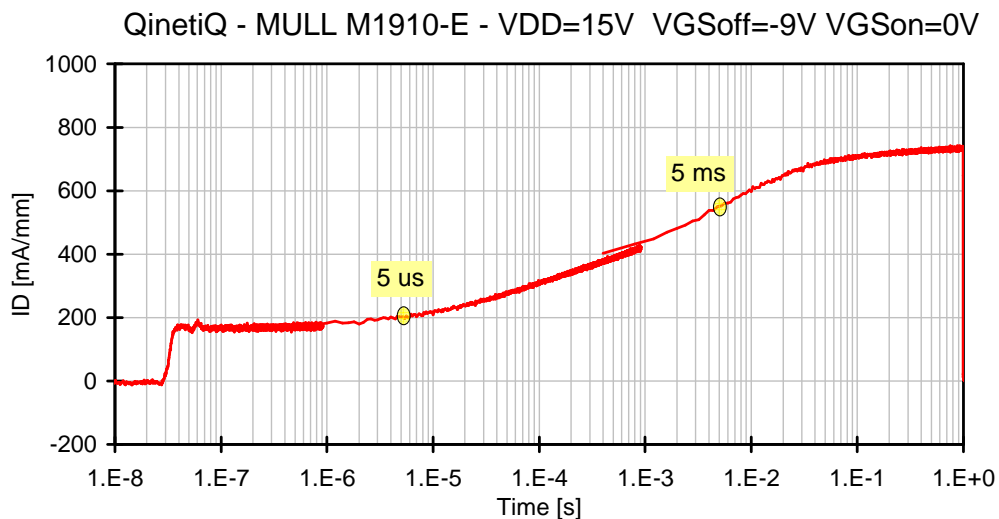
## 4.2 CURRENT COLLAPSE EFFECT

### 4.2.1 Experimental characterization methods

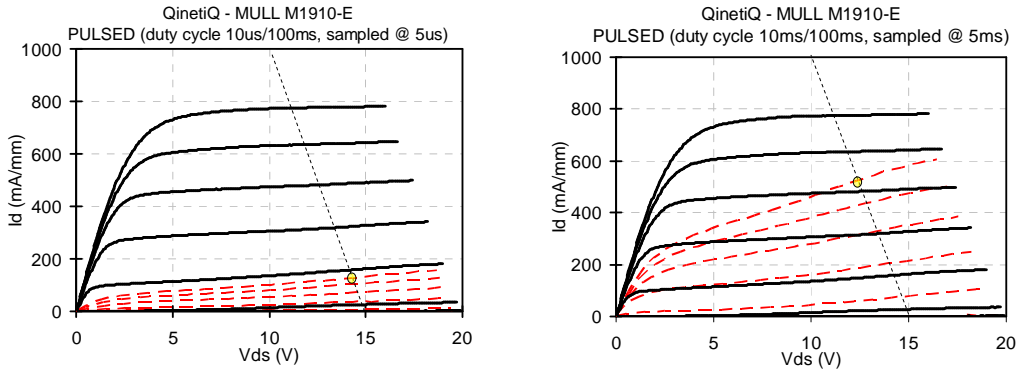
Dispersion effects have been characterized using different types of electrical measurements, including (i) "logarithmic" gate voltage pulses; (ii) double-pulse measurements, pulsing drain and gate voltages from arbitrary baseline values; and (iii) transconductance vs. frequency measurements.

#### 4.2.1.1 "Logarithmic pulse" measurements

In KorriGaN technologies, dispersion effects appear at low frequencies; as a consequence, very long voltage pulses are required in order to evaluate the duration of the turn-on transient. An automated measurement system merges the results obtained by applying a series of voltage pulses of different duration to the gate and allows one to evaluate the evolution of drain current up to 1 s after the application of the pulse, with a very good time resolution, see Fig. 4.1. Drain current vs voltage characteristics can be evaluated at different sampling times, Fig. 4.2, but comparison can be done only with DC characteristics, since only the gate voltage can be pulsed.



**Fig. 4.1:** gate-lag drain current "logarithmic pulse" of QinetiQ MULL HEMT processed with the Photolithography step.



**Fig. 4.2:** Output  $I_D$  vs  $V_{DS}$  curves,  $V_{GS}=0V$  to  $-6V$ , step  $-1V$ ,  $V_{GS}=0V$  are the top lines. **Solid black lines:** DC curves taken with short integration time mode; **Dash red lines:** Pulsed curves sampled at  $5\ \mu s$  (**left**) and  $5\ ms$  (**right**) after the gate turn-on pulse application.

#### 4.2.1.2 "Double-pulse" or "DIVA-like" measurements

More commonly, current collapse effects are evaluated using the "double-pulse" or "DIVA-like" system, already described in chapter 2.3.2.1. The transistor is turned on starting from an arbitrary quiescent point (or  $V_{GS}$ ,  $V_{DS}$  "baseline"), that is an important feature since the presence of traps always involves memory effects which may change the device pulsed behavior according to the adopted quiescent bias point. Pulse duration and duty cycle were chosen taking into account typical capture and emission times of the involved traps.

Slump ratio is defined by comparing two pulsed  $I_D$  vs  $V_{DS}$  characteristics, the "collapsed" I-V curve, measured starting from baseline  $V_{DS} \geq 0\ V$ ,  $V_{GS} \leq V_{pinch-off} = V_p$  (which injects negative charge on surface traps), and the "reference" curve, measured with baseline  $V_{GS} = V_{DS} = 0\ V$ . A "slump ratio" S.R. is then defined using the equation listed below; S.R. = 1 means no current collapse. A completely collapsed device has S.R. which tends to 0. A dynamic threshold voltage shift,  $\Delta V_{TH}$ , and a "transconductance slump",  $g_{m\_slump}$ , were also defined, as shown below. Threshold voltage  $V_{TH}$  was defined by extrapolating the  $I_D$  vs  $V_{GS}$  curves to measured at  $V_{DS} = 10\ V$  to  $I_D = 0\ mA$ ;  $g_{m\_max}(V_p, 20)$  corresponds to the maximum value of transconductance measured in pulsed conditions using a baseline with  $V_{GS} = V_p$ ,  $V_{DS} = 20\ V$ .

$$S.R. = \frac{I_{DS0}(V_p, 20)}{I_{DS0}(0, 0)}$$

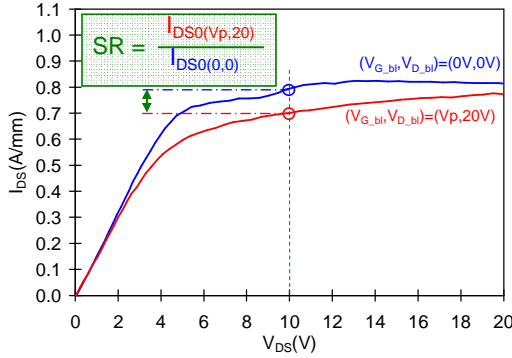
$$I_{DS0} = I_D \text{ at } V_G = 0V, V_D = 10V$$

$$\Delta V_{TH} = V_{TH}(V_p, 20) - V_{TH}(0, 0)$$

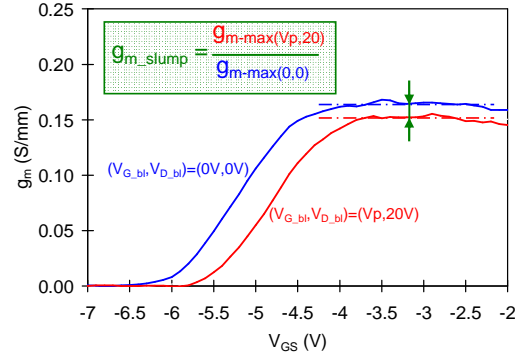
$$\text{at } V_D = 10V$$

$$g_{m\_slump} = \frac{g_{m\text{-max}}(V_p, 20)}{g_{m\text{-max}}(0, 0)}$$

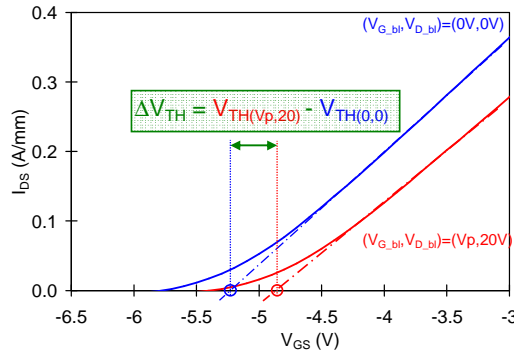
$$\text{at } V_D = 10V$$



**Fig. 4.3:** SR definition adopted in this work.



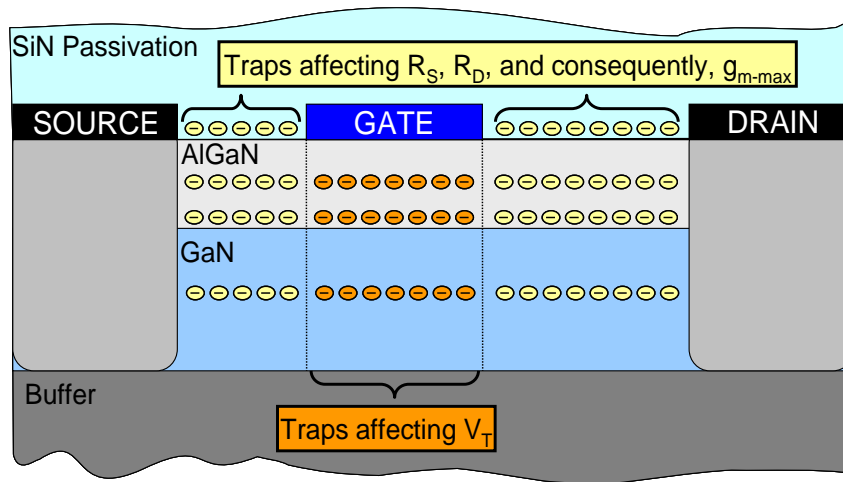
**Fig. 4.4:**  $g_{m\_slump}$  definition adopted in this work.



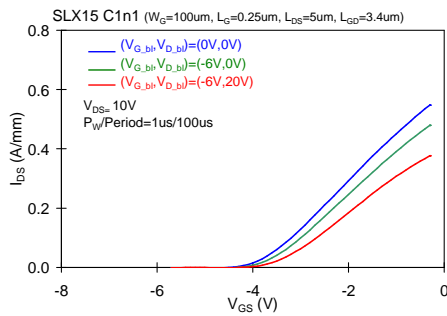
**Fig. 4.5:**  $\Delta V_{TH}$  definition adopted in this work.

The interest in the dynamic behaviour of  $V_{TH}$  and  $g_m$  is motivated by a simple consideration. Fig. 4.6 shows the schematic cross-section of an AlGaIn/GaN HEMT and identifies possible location of deep levels on the device surface and within the various epitaxial layers and their interfaces. Neglecting short-channel effects, we can assume that traps on the device surface will only affect source and drain parasitic resistances  $R_S$  and  $R_D$ , while traps located below the surface, within the various epitaxial layers, if homogeneously distributed along the device length and width, will influence both parasitic resistances and device threshold voltage. An increase in parasitic resistances reduces drain current and transconductance,

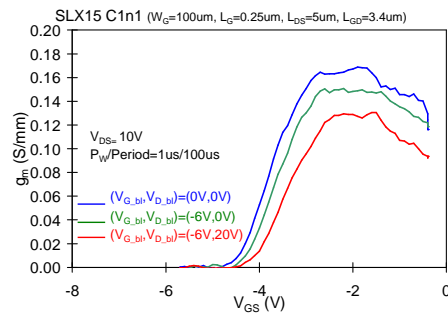
and has its maximum effect when the channel is fully open, i.e. at high values of  $V_{GS}$ , as shown in Fig. 4.7, Fig. 4.8, and Fig. 4.9 which refer to double-pulse measurements respectively of the  $I_D$  vs  $V_{GS}$ ,  $g_m$  vs  $V_{GS}$ , and  $I_D$  vs  $V_{DS}$  characteristics of a Selex SLX15 device. Since almost no shift in threshold voltage is observed, it seems reasonable to assume that the observed collapse effects are due, in these devices, to the effect of traps on the devices surface.



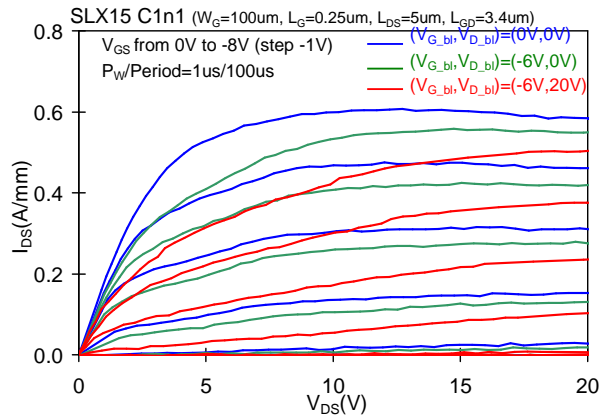
**Fig. 4.6:** schematic cross-section of an AlGaIn/GaN HEMT identifying the effect of traps.



**Fig. 4.7:** Double-pulse  $I_{DS}$ - $V_{GS}$  characteristics of a Selex SLX15 device ( $W_G=100\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{DS}=5\mu\text{m}$ ,  $L_{GD}=3.4\mu\text{m}$ ) measured with a  $100\mu\text{s}$  period, and a  $1\mu\text{s}$  pulse width ( $V_{GS}$  from  $0\text{V}$  to  $-6\text{V}$  step  $-1\text{V}$ ,  $V_{DS}$  from  $0$  to  $20\text{V}$ ). Different baseline values for  $V_{GS-bl}$ ,  $V_{DS-bl}$  have been adopted.

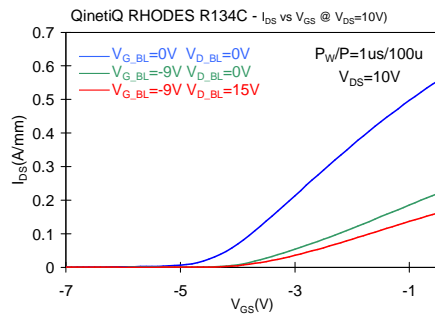


**Fig. 4.8:** Double-pulse transconductance characteristics  $g_m$  vs  $V_{GS}$  of a Selex SLX15 ( $W_G=100\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{DS}=5\mu\text{m}$ ,  $L_{GD}=3.4\mu\text{m}$ ) measured with a  $100\mu\text{s}$  period, and a  $1\mu\text{s}$  pulse width ( $V_{GS}$  from  $0\text{V}$  to  $-6\text{V}$  step  $-1\text{V}$ ,  $V_{DS}$  from  $0$  to  $20\text{V}$ ). Different baseline values for  $V_{GS-bl}$ ,  $V_{DS-bl}$  have been adopted.

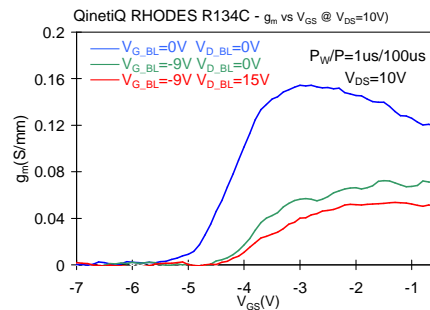


**Fig. 4.9:** Double-pulse  $I_{DS}$ - $V_{DS}$  characteristics of a Selex SLX15 ( $W_G=100\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{DS}=5\mu\text{m}$ ,  $L_{GD}=3.4\mu\text{m}$ ) measured with a  $100\mu\text{s}$  period, and a  $1\mu\text{s}$  pulse width ( $V_{GS}$  from  $0\text{V}$  to  $-6\text{V}$  step  $-1\text{V}$ ,  $V_{DS}$  from  $0$  to  $20\text{V}$ ). Different baseline values for  $V_{GS-bl}$ ,  $V_{DS-bl}$  have been adopted.

At high  $V_{DS}$  voltages, some detrapping may occur due to the high electric field, which also "masks" the electrostatic action of the traps; as a consequence, the current slump is maximum for  $V_{DS}$  values around the knee voltage, between the linear and the saturation region, see Fig. 4.9, and decrease at increasing  $V_{DS}$  in saturation.

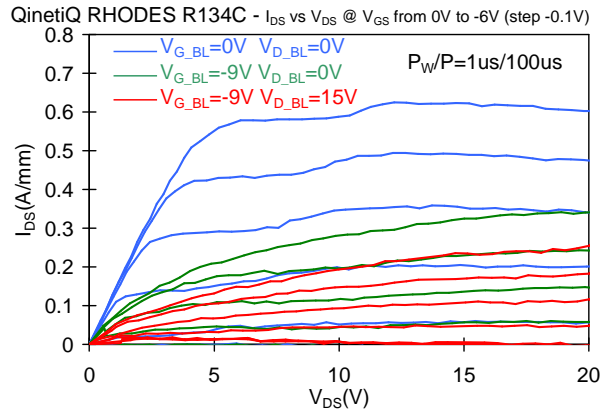


**Fig. 4.10:** Double-pulse  $I_{DS}$ - $V_{GS}$  characteristics of a QinetiQ RHODES device ( $W_G=100\mu\text{m}$ ,  $L_G=0.5\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.4\mu\text{m}$ ) measured with a  $100\mu\text{s}$  period, and a  $1\mu\text{s}$  pulse width ( $V_{GS}$  from  $0\text{V}$  to  $-6\text{V}$  step  $-1\text{V}$ ,  $V_{DS}$  from  $0$  to  $20\text{V}$ ). Different baseline values for  $V_{GS-bl}$ ,  $V_{DS-bl}$  have been adopted.



**Fig. 4.11:** Double-pulse transconductance characteristics  $g_m$  vs  $V_{GS}$  of a QinetiQ RHODES device ( $W_G=100\mu\text{m}$ ,  $L_G=0.5\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.4\mu\text{m}$ ) measured with a  $100\mu\text{s}$  period, and a  $1\mu\text{s}$  pulse width ( $V_{GS}$  from  $0\text{V}$  to  $-6\text{V}$  step  $-1\text{V}$ ,  $V_{DS}$  from  $0$  to  $20\text{V}$ ). Different baseline values for  $V_{GS-bl}$ ,  $V_{DS-bl}$  have been adopted.

When traps are present below the gate (i.e. within the epitaxial layers), a dynamic shift in the threshold voltage is observed, see Fig. 4.10 and Fig. 4.11; however, since source and drain access region are also affected by traps, the transconductance also decreases, so that the entire  $I_D$  vs  $V_{DS}$  is collapsed, see Fig. 4.12.



**Fig. 4.12:** Double-pulse  $I_{DS}$ - $V_{DS}$  characteristics of a QinetiQ RHODES device ( $W_G=100\mu\text{m}$ ,  $L_G=0.5\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.4\mu\text{m}$ ) measured with a 100  $\mu\text{s}$  period, and a 1  $\mu\text{s}$  pulse width ( $V_{GS}$  from 0V to -6V step -1V,  $V_{DS}$  from 0 to 20 V). Different baseline values for  $V_{GS-bl}$ ,  $V_{DS-bl}$  have been adopted.

#### 4.2.1.3 Analysis of dispersion effects by means of two-dimensional numerical device simulation

In order to validate our hypothesis on the influence of the location of traps on the dynamic behaviour of  $V_{TH}$  and  $g_m$ , we have carried out two-dimensional (2D) numerical device simulations using the commercial package DESSIS (Synopsis).

The simulated device structure includes a 1.2  $\mu\text{m}$  GaN bulk layer, capped by a 25 nm AlGaIn barrier, with  $x=0.26$ . The source-gate and gate-drain separations used are 1.13  $\mu\text{m}$  and 2.05  $\mu\text{m}$ , respectively, and the gate length is set to 0.52  $\mu\text{m}$ . Highly doped regions are created under the source-drain electrodes down to the GaN channel to emulate metal spikes and to control contact resistance. AlGaIn and GaN possess polarized wurtzite crystal structures, having dipoles across the crystal in the [0001] direction. In the absence of external fields, this macroscopic polarization includes spontaneous (pyroelectric) and strain-induced (piezoelectric) contributions. The primary effect of polarization is an interface charge due to

abrupt divergence in the polarization at the AlGaN–GaN heterointerface. To account for polarization charges at the AlGaN/GaN heterointerface were used explicit charges at heterointerface, where a large polarization divergence is present. The charge values are automatically computed during preprocessing of the input file by TCL script written by us. The computation uses Tcl scripting and follows the formulation by Ambacher *et al.* [2]. A partial strain relaxation would lead to a reduction of the polarization charges and, therefore, a DESSIS variable, strainRelax, is included to allow users to control the degree of required relaxation. In this simulations, strainRelax = 0.1. Acceptable values range from 0 to 1. In this work, it is assumed that GaN is fully relaxed and, therefore, its polarization vector contains only the spontaneous component,  $P_{sp}(GaN)$ . For AlGaN, in addition to the spontaneous component  $P_{sp}(AlGaN)$ , the piezopolarization component due to the strained AlGaN layer must be computed. GaN and AlN values and linear interpolation are adopted in the computation of all mole fraction–dependent piezoelectric and mechanical constants of AlGaN. The large polarization divergence at the AlGaN barrier surface would completely deplete the channel of electrons if not partially or completely compensated by positive charges [3]. It is still not clear whether the polarization charge is compensated by fixed charges or interface trap states. In this work, polarization change was partially compensated by deep, single-level trap states. Since anisotropy in dielectric constants plays a first-order role in the potential distribution in GaN HFET devices and, as a consequence, in the I–V characteristics, an anisotropic model for the dielectric constants was used in the simulations ( $\epsilon_{//} = 9.5$ ,  $\epsilon_{\perp} = 10.4$ ).

The aim of this simulation study is to verify the effect of traps on  $I_D$  vs  $V_{GS}$  device characteristics, without attempting any quantitative modeling of the device, only acceptor/electron, bulk, single-level traps have been included in the simulations. The density of traps in the GaN buffer was set to  $N_T = 1 \times 10^{17} \text{ cm}^{-3}$ , with a cross section of  $\sigma_T = 1 \times 10^{-15} \text{ cm}^{-2}$ ; they were positioned 0.5 eV from the conduction band. The density of interface fixed charge in the GaN/AlGaN and AlGaN/SiN interface was instead set to an initial concentration of  $N_{\text{GaN/AlGaN}} = 13.8 \times 10^{12} \text{ cm}^{-2}$  (resulting by the polarization theory) and  $N_{\text{SiN/AlGaN}} = -9.3 \times 10^{12}$

$\text{cm}^{-2}$ , respectively. Furthermore a concentration of  $N_T = 4.4 \times 10^{12} \text{ cm}^{-2}$  donor single-level traps, with a cross section of  $\sigma_T = 1 \times 10^{-15} \text{ cm}^{-2}$ , were positioned 0.1 eV from the conduction band in the GaN/AlGaN interface.

Fig. 4.13a shows typical dc drain-current  $I_D$  versus gate-source voltage  $V_{GS}$  characteristics measured at a drain-source voltage  $V_{DS}$  of 10 V of the undoped Selex AMS04 HEMTs superimposed to the device simulation results. Whereas Fig. 4.13b shows the respective  $g_m$  curve.

With the aim of evaluating the effects of deep levels, three different scenarios were taken into consideration, differing for the vertical position of the traps: a) at the SiN/AlGaN interface, only in the access regions; b) at the AlGaN/GaN interface, everywhere; c) within the AlGaN and GaN layers. Simulations have considered either fixed charge or traps with specific energy positions from the band edges and cross-sections.

- a) *Trap formation at SiN/AlGaN interface.* A negative charge at the device surface in the access regions (either fixed or due to traps) affects, as expected, the device current and transconductance without changing the threshold voltage, see Fig. 4.14. The SiN or the AlGaN surface acts as a "virtual Gate" whose voltage is determined by the trapped charge at AlGaN/SiN interface as proposed by [4] in order to explain current collapse. The presence of this virtual gate leads to an increase of the access resistances originating the "current collapse" in dynamic conditions. Moreover, at high  $V_{GS}$  values, drain current is controlled by the "virtual gate" and only when  $V_{GS}$  decreases below a certain value, which is determined by the concentration of surface traps, the "real gate" is able to modulate again  $I_D$ , since the depletion region under the gate prevails upon that in the access regions. When the "virtual gate" limits the current, the drain current remains nearly constant as a function of  $V_{GS}$ , leading to a transconductance drop.
- b) *Trap formation at GaN/AlGaN interface.* In this case a threshold shift is obtained, as it occurs in the case of a MOSFET with charge trapped in

the gate oxide (or at the Si/SiO<sub>2</sub> interface), see Fig. 4.15. It should be noticed that a transconductance drop is also present since the effect of the positive charge at the SiN/AlGa<sub>N</sub> interface on the channel is screened due to the AlGa<sub>N</sub>/Ga<sub>N</sub> interface charge.

- c) *Trap formation at GaN and AlGa<sub>N</sub> layers.* Bulk trap formation in the Ga<sub>N</sub> and AlGa<sub>N</sub> layers has the same effect observed in b), see Fig. 4.16.

In conclusion, device simulations have confirmed that, at least for fairly long gate-length devices, the observed threshold voltage shifts should be attributed to traps located within the epitaxial layers and their interfaces, while surface traps would not affect  $V_{TH}$ . Simulations therefore confirm that pulsed  $V_{TH}$  and  $g_m$  measurements represent a simple, yet effective, tool to identify possible trapping effects related with substrate quality or epitaxial layer growth. The results of the simulations can be applied also to the study of current collapse effects due to degradation.

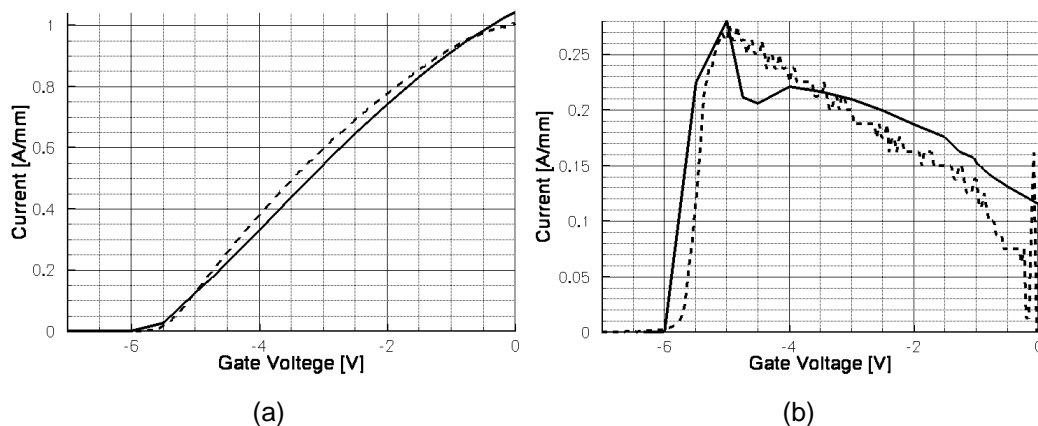


Fig. 4.13: Typical dc drain-current  $I_D$  versus gate-source voltage  $V_{GS}$  characteristics of Selex AMS04 measured at a drain-source voltage  $V_{DS}$  of 10 V of the undoped HEMTs studied superimposed to the device simulation results (a) and their corresponding transconductance (b).

--- Measure  
 — Fitting Simulation

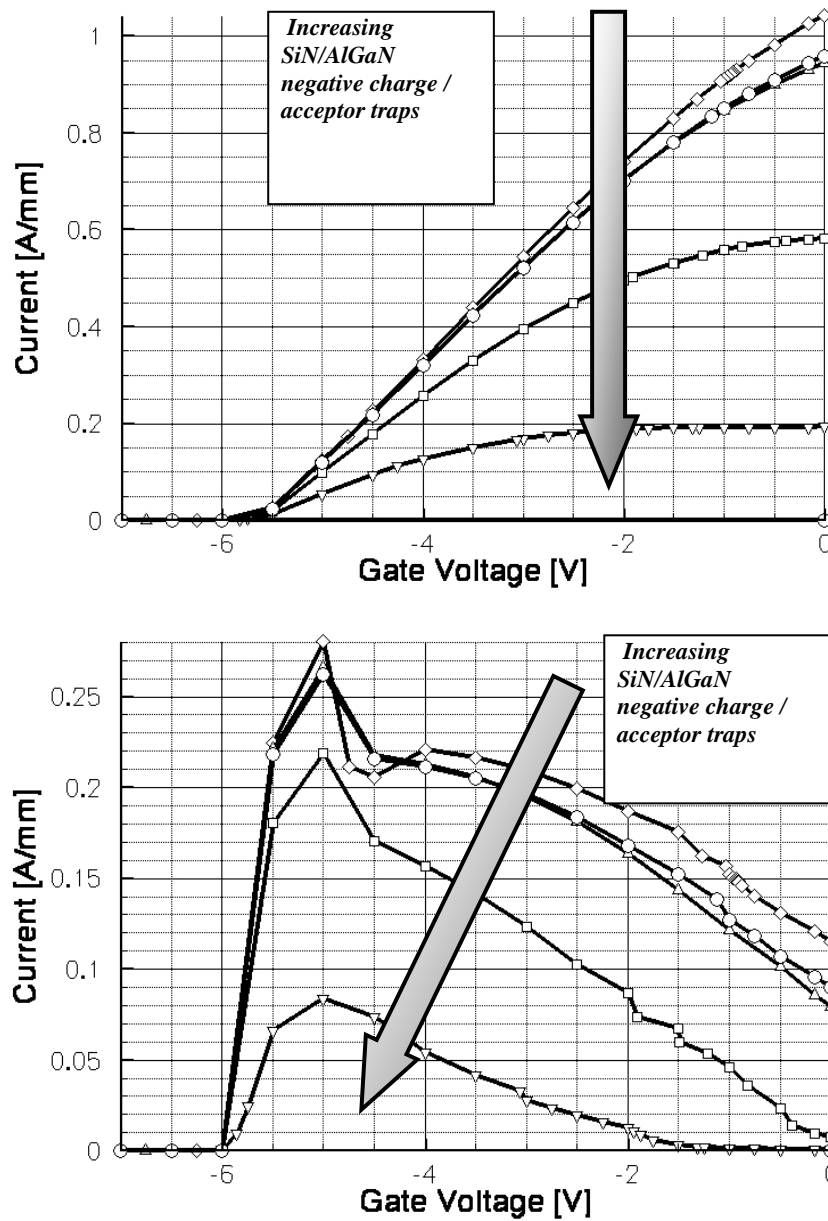


Fig. 4.14: Device simulation results of the dc drain-current  $I_D$  versus  $V_{GS}$  characteristics at  $V_{DS} = 10$  V of the undoped HEMTs studied obtained varying the charge/trap concentration at SiN/AlGaN interface.

- ◇— Fitting Simulation
- Simulation obtained added  $N_T = 3 \times 10^{12} \text{ cm}^{-2}$  of acceptor traps positioned 0.5 eV from the Valence band at SiN/AlGaN interface
- △— Simulation obtained added  $N_T = 5 \times 10^{12} \text{ cm}^{-2}$  of acceptor traps positioned 0.5 eV from the Valence band at SiN/AlGaN interface
- Simulation obtained added  $N_T = 3 \times 10^{12} \text{ cm}^{-2}$  negative fixed charge to SiN/AlGaN interface
- ▽— Simulation obtained added  $N_T = 6 \times 10^{12} \text{ cm}^{-2}$  negative fixed charge to SiN/AlGaN interface

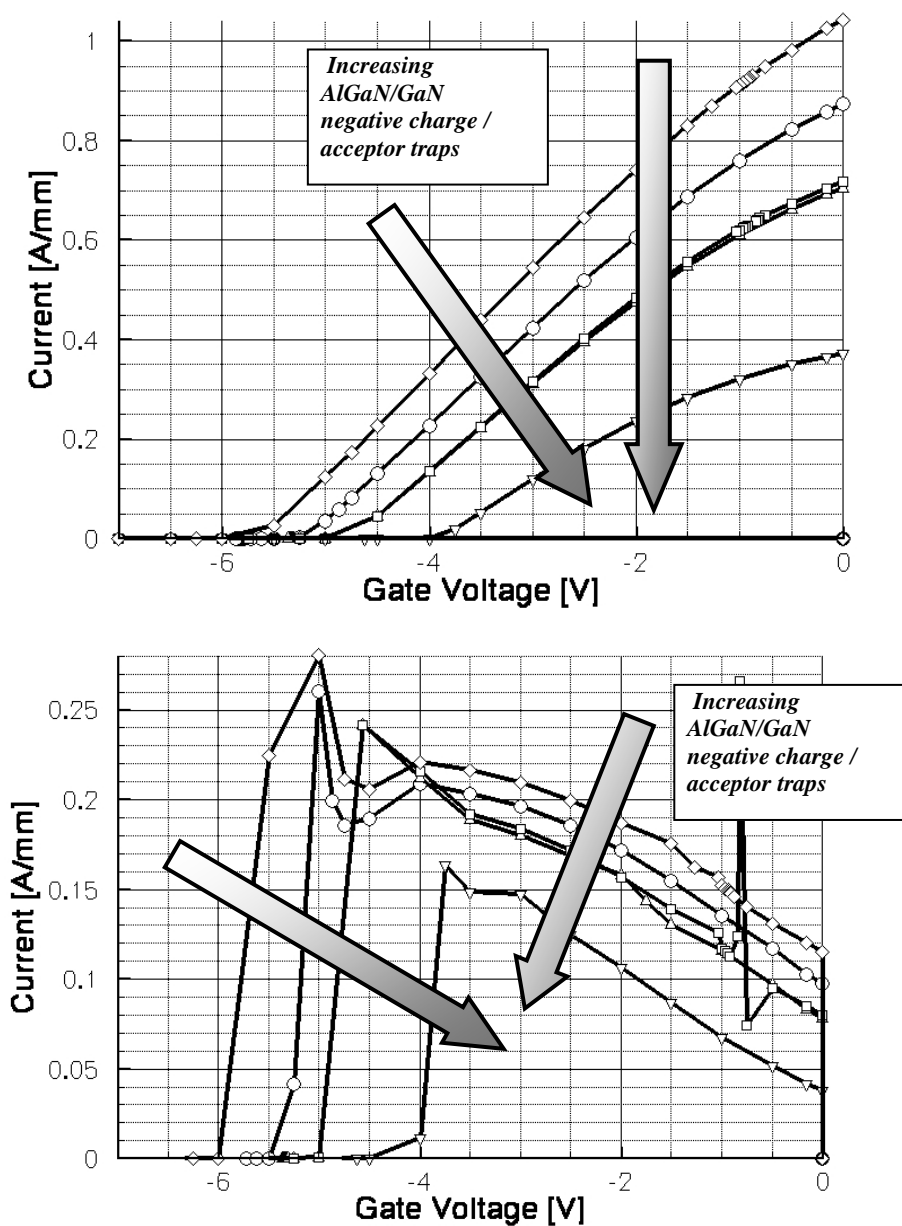







Fig. 4.15: Device simulation results of the dc drain-current  $I_D$  versus  $V_{GS}$  characteristics at  $V_{DS} = 10$  V of the undoped HEMTs studied obtained varying the trap concentration at GaN/AlGaN interface.

-  Fitting Simulation
-  Simulation obtained added  $N_T = 1 \times 10^{12} \text{ cm}^{-2}$  of acceptor traps positioned 0.5 eV from the Conduction band at GaN/AlGaN interface
-  Simulation obtained added  $N_T = 2 \times 10^{12} \text{ cm}^{-2}$  of acceptor traps positioned 0.5 eV from the Conduction band to GaN/AlGaN interface
-  Simulation obtained added  $N_T = 1 \times 10^{12} \text{ cm}^{-2}$  negative fixed charge to GaN/AlGaN interface
-  Simulation obtained added  $N_T = 2 \times 10^{12} \text{ cm}^{-2}$  negative fixed charge to GaN/AlGaN interface

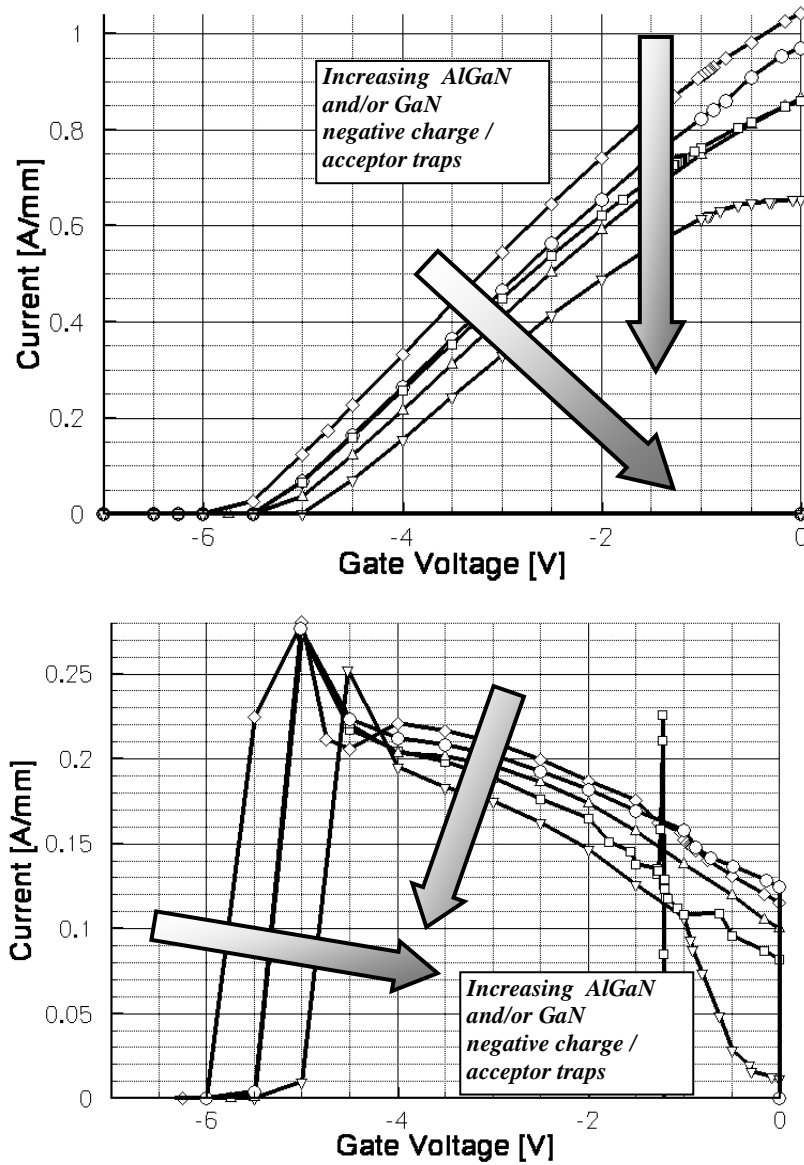
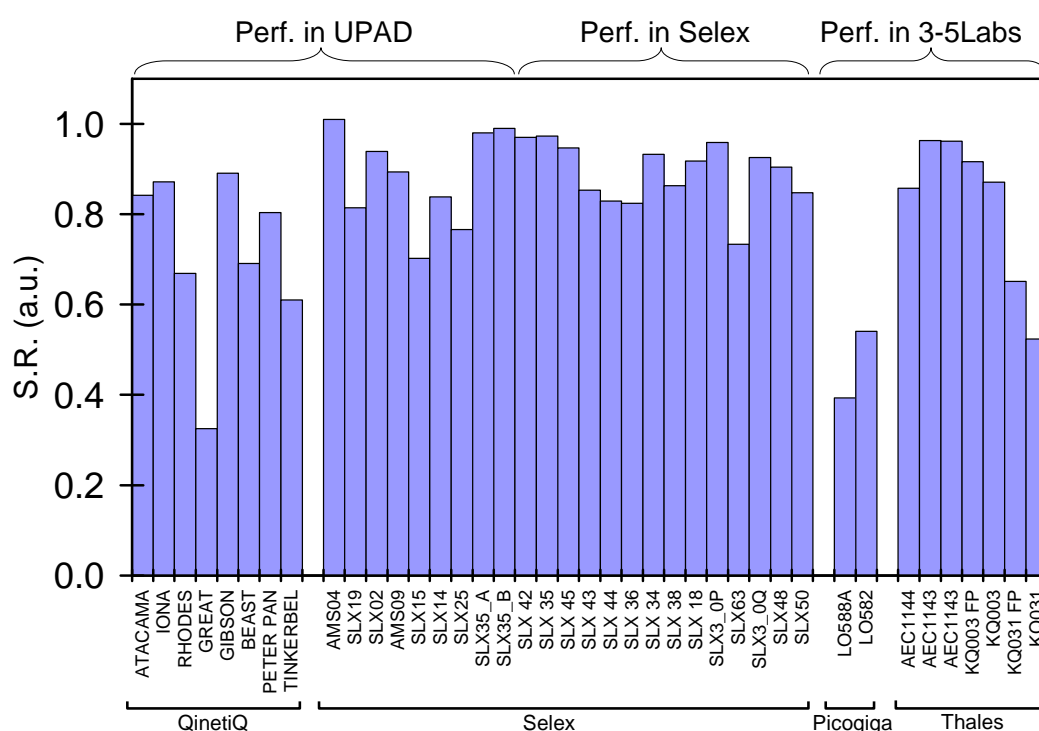


Fig. 4.16: Device simulation results of the dc drain-current  $I_D$  versus  $V_{GS}$  characteristics at  $V_{DS} = 10$  V of the undoped HEMTs studied obtained varying the trap concentration at GaN and AlGaN bulk.

- ◇— Fitting Simulation
- Simulation obtained added  $N_T = 5 \times 10^{17} \text{ cm}^{-2}$  of acceptor bulk traps positioned 1.5 eV from the Conduction band in the AlGaN barrier
- △— Simulation obtained added  $N_T = 1 \times 10^{17} \text{ cm}^{-2}$  of acceptor bulk traps positioned 0.5 eV from the Conduction band in the GaN buffer
- Simulation obtained added  $N_T = 5 \times 10^{17} \text{ cm}^{-2}$  negative fixed bulk charge to AlGaN barrier
- ▽— Simulation obtained added  $N_T = 1 \times 10^{17} \text{ cm}^{-2}$  negative fixed bulk charge to GaN buffer

## 4.2.2 Material and technology dependence of current collapse effects

Current slump has been characterized using the double-pulse, DIVA-like set-up in almost all wafers manufactured within KorriGaN. Fig. 4.17 summarizes the current slump, defined as described in paragraph 4.2.1.2, for a significant set of KorriGaN wafers. Measurements have been performed at University of Padova, Selex-SI, and 3-5 Labs. Characteristics of wafers submitted to double-pulse current collapse tests, within information about substrate and epi suppliers are reported in Table 4.1.



**Fig. 4.17:** Drain current slump ratio, measured adopting a baseline ( $V_{DS} = 20$  V,  $V_{GS} = -8$  V) in some of the KorriGaN wafers. Measurements have been performed at University of Padova, Selex-SI, and 3-5 Labs.

The highest contribution to current slump usually comes from traps at the surface, as demonstrated by the fact that suitable passivation using SiN or SiO/SiN greatly improves current collapse. Most KorriGaN devices preserve at least 80% of their DC current in pulsed conditions).

As demonstrated by the 2D device simulations presented in paragraph 4.2.1.3, if the traps responsible for dispersion are located on the device surface, they

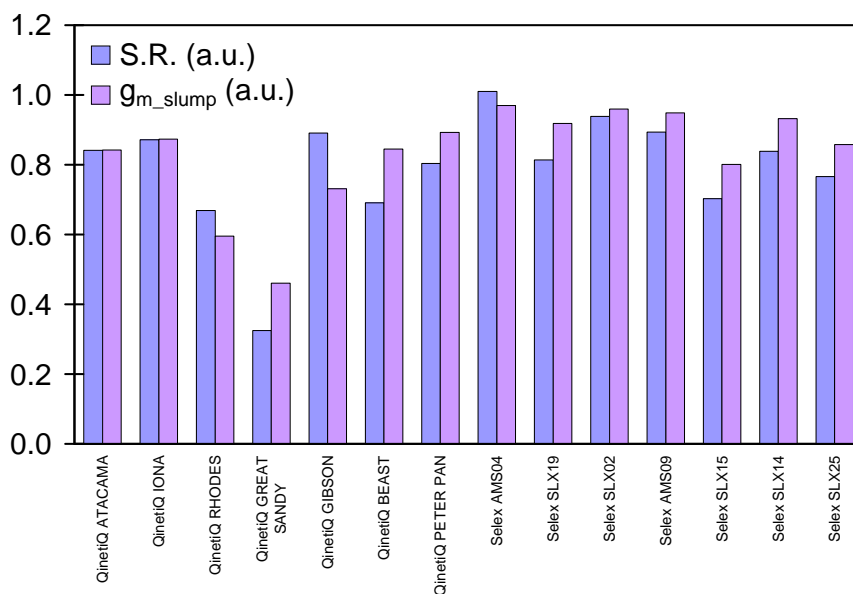
should have a reduced effect on the device threshold voltage, but they will affect the series resistances, and, as a consequence, the maximum value of transconductance  $g_{m\_max}$  (see Fig. 4.6).

**Table 4.1:** Characteristics of wafers submitted to double-pulse current collapse tests

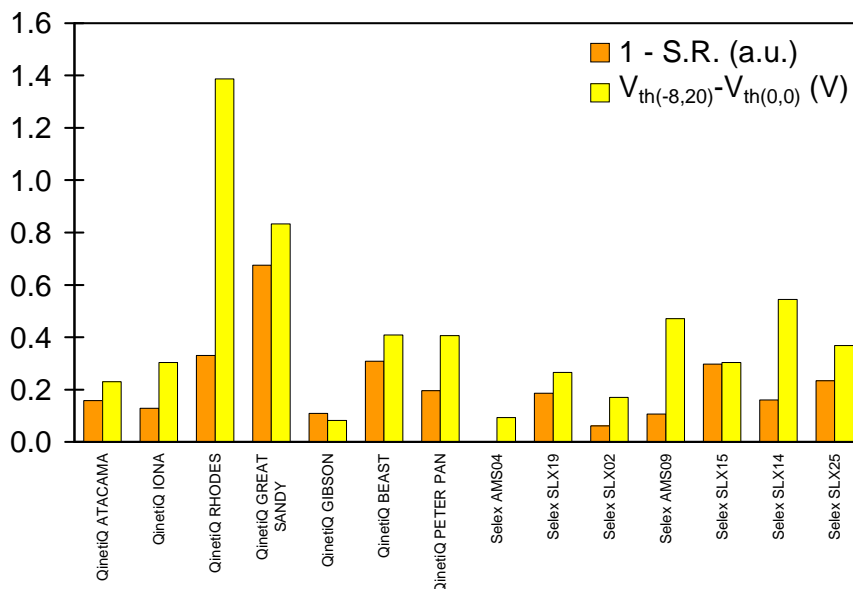
Foundry	Wafer name	substrate		epilayer supplier
			supplier	
QinetiQ	ATACAMA	SiC	Cree	QinetiQ
	IONA	SiC	Cree	Qinetiq
	RHODES	SiC	Cree	QinetiQ
	GREAT SANDY	SiC	Cree	TRT
	GIBSON	SiC	Cree	QinetiQ
	BEAST	SiC	Cree	TRT
	PETER PAN	SiC	Cree	QinetiQ
	TINKERBELL	SiC	Norstel	QinetiQ
Selex	AMS_04	SiC	Cree	QinetiQ
	SLX_19	SiC	Norstel	Picogiga
	SLX_02	SiC	Cree	TRT
	AMS_09	Sapphire	-	QinetiQ
	SLX_15	Sapphire	-	QinetiQ
	SLX_14	Sapphire	-	ULE
	SLX_25	SiC	Norstel	QinetiQ
	SLX_35	SiC	Cree	TRT
	SLX_42	SiC	Norstel	QinetiQ
	SLX_45	SiC	Cree	Picogiga
	SLX_43	SiC	Cree	Picogiga
	SLX_44	SiC	Cree	Picogiga
	SLX_36	SiC	Nostel	Picogiga
	SLX_34	SiC	Cree	TRT
	SLX_38	SiC	Nostel	QinetiQ
	SLX_18	SiC	Cree	TRT
	SLX_0P	SiC	Cree	Cree
	SLX_63	SiC	Cree	QinetiQ
	SLX_0Q	SiC	Cree	Cree
	SLX_48	SiC	Cree	Picogiga
SLX_50	SiC	Norstel	QinetiQ	
Picogiga	LO588A	-	-	-
	LO582	-	-	-
Thales	AEC1144	SiC	Cree	TRT
	AEC1143	SiC	Cree	TRT
	KQ003	SiC	Cree	QinetiQ
	KQ031	SiC	Norstel	QinetiQ

Fig. 4.18 shows the slump ratio of a significant set of KorriGaN wafers; the higher the slump ratio, the better is the device behavior. With few exceptions, the S.R. of tested wafers is close to 0.8. Current slump is closely correlated with transconductance slump, Fig. 4.18, as it was expected since  $I_D = g_m (V_{GS} - V_T)$ . There are a few wafers, however, which also show remarkable shifts in the threshold voltage, see Fig. 4.19, thus suggesting the presence of traps in the

epitaxial layers or at their interfaces. In Fig. 4.19 the value of  $(1 - S.R.)$  is plotted, so that better devices show at the same time lower values of  $(1 - S.R.)$  and of threshold voltage shift. The histogram plot reported in Fig. 4.18 and Fig. 4.19 show that wafer RHODES and GREAT SANDY are possibly affected by presence of traps in the epitaxial layers, resulting in remarkable  $V_{TH}$  shifts during pulsed measurements ( $\sim 1.4$  V and  $0.8$  V respectively).



**Fig. 4.18:** slump ratio S.R. and  $g_{m\_slump}$  of wafers measured at University of Padova.



**Fig. 4.19:**  $(1 - S.R.)$  and threshold voltage shift of wafers measured at University of Padova.

### 4.2.3 Dependence on gate-to-drain distance

In QinetiQ GIBSON and ATACAMA wafers, the dynamic shift in threshold voltage is very small, see Fig. 4.19; as a consequence the observed current slump should be attributed to an increase in series resistance due to negative charge trapping at the SiN/AlGa<sub>N</sub> interface in the access regions. This is confirmed by the experimental observation that dispersion increases at increasing the gate-drain distance  $L_{GD}$ , see Fig. 4.20.

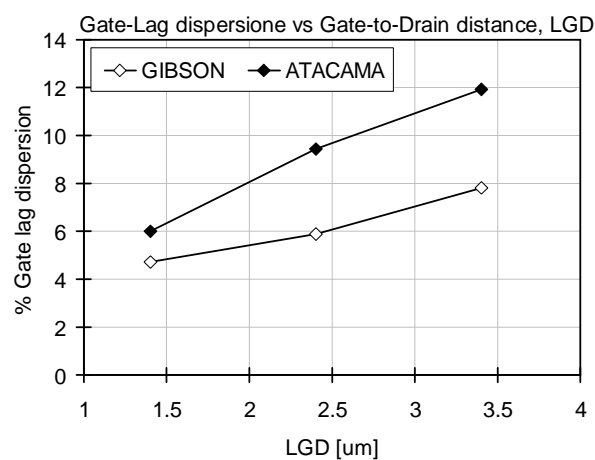


Fig. 4.20: Gate-lag dispersion as a function of the gate to drain distance in QinetiQ GIBSON and ATACAMA devices.

### 4.2.4 Anomalies in QinetiQ devices defined by photolithography

In general, moderate or low dispersion effects were detected by means of pulsed techniques, with some exceptions:

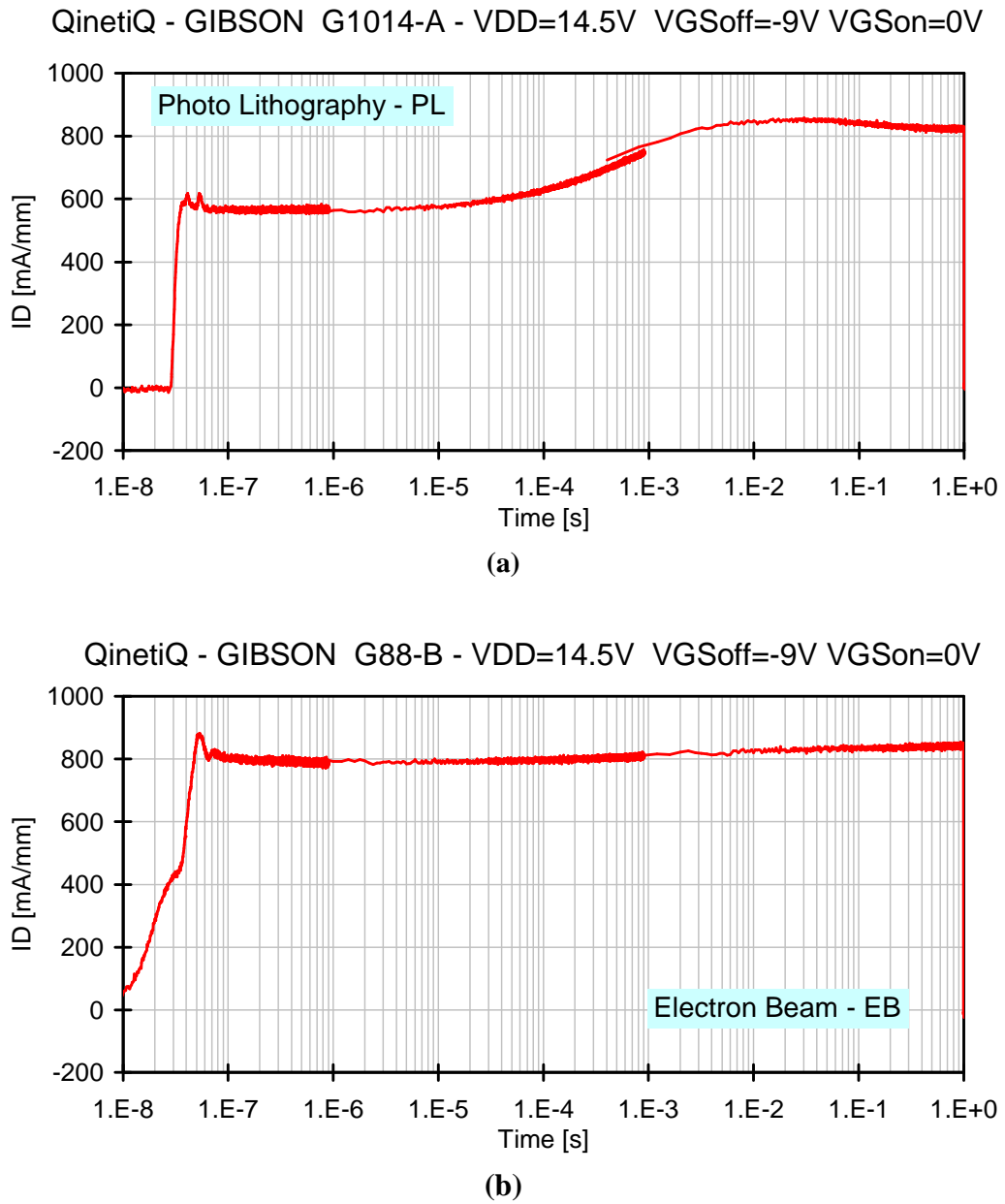
- (a) QinetiQ devices which have been fabricated using photolithography, even if they belong to different wafers, present remarkable dispersion effects; Table 4.2 compares the results of gate-lag characterization in QinetiQ devices (First rows); Fig. 4.21(a) and (b) compares the typical drain current pulse of a GIBSON device fabricated with e-beam lithography with those of a photolithography device;
- (b) QinetiQ MULL devices, either fabricated using photolithography or e-beam lithography, present significant dispersion effects, reaching 90% in case of photolithography. Fig. 4.22(a) shows the "logarithmic pulse" gate-

lag pulse of a QinetiQ MULL device fabricated using the photolithography process (a) and with the e-beam lithography (b). Fig. 4.1 shows the "logarithmic pulse" gate-lag pulse of a QinetiQ MULL device fabricated using e-beam lithography in which two time points have been highlighted: 5  $\mu$ s and 5ms. In Fig. 4.2, the I-V DC output characteristics obtained using HP4155 in the short integration time mode are compared with those sampled respectively after a 10  $\mu$ s/100 ms  $V_{GS}$  pulse, starting from  $V_{GS-off} = -9V$  to  $V_{GS-on} = 0V$ , at constant  $V_{DD} = 15 V$ , Fig. 4.2, left, or after 5 ms of a 10 ms-on/100 ms-off  $V_{GS}$  pulse with the same bias points, Fig. 4.2, right. Time dependent current collapse of I-V characteristics is clearly detected.

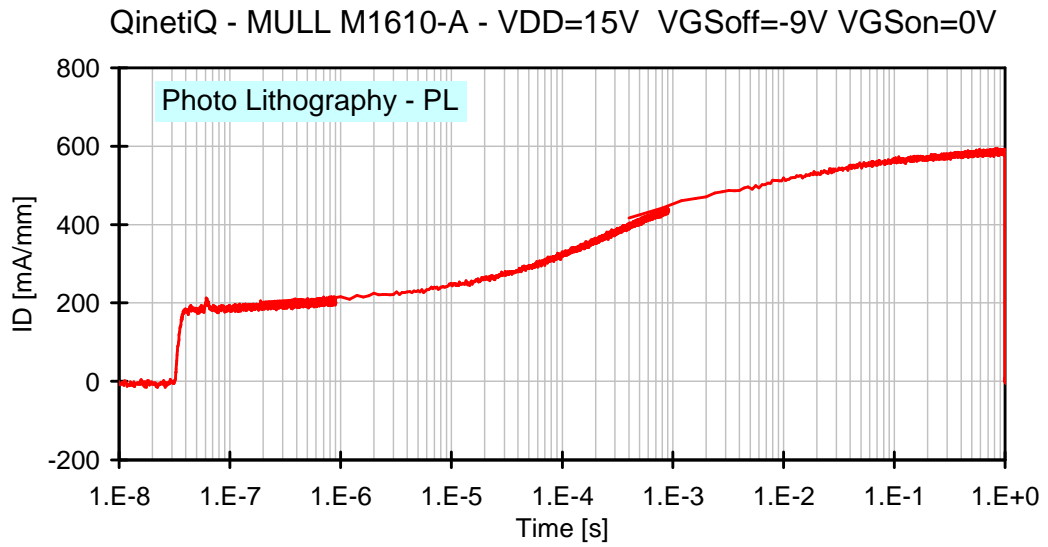
**Table 4.2:** dispersion in QinetiQ PL and EBL devices and in MULL devices with Okmetic substrate

Fab	Wafer name	PL/EB	epilayer supplier	substrate	substrate supplier	Measured devices	GATE-LAG DISPERSION	NOTE
QINETIQ	ATACAMA	PL	QinetiQ	SiC	Cree	7	MEDIUM (~25%)	
		EB				35	LOW (~10 %)	
	GIBSON	PL	QinetiQ	SiC	Cree	8	HIGH (~40%)	see Figure
		EB				40	LOW (<10 %)	see Figure
	IONA	PL	QinetiQ	SiC	Cree	6	MEDIUM (~30%)	
		EB				33	VERY LOW (< 5%)	
	MULL	PL	Tiger	SiC	Okmetic	13	VERY HIGH (~90%)	see Figure
		EB				41	VERY HIGH (~70%)	see Figure

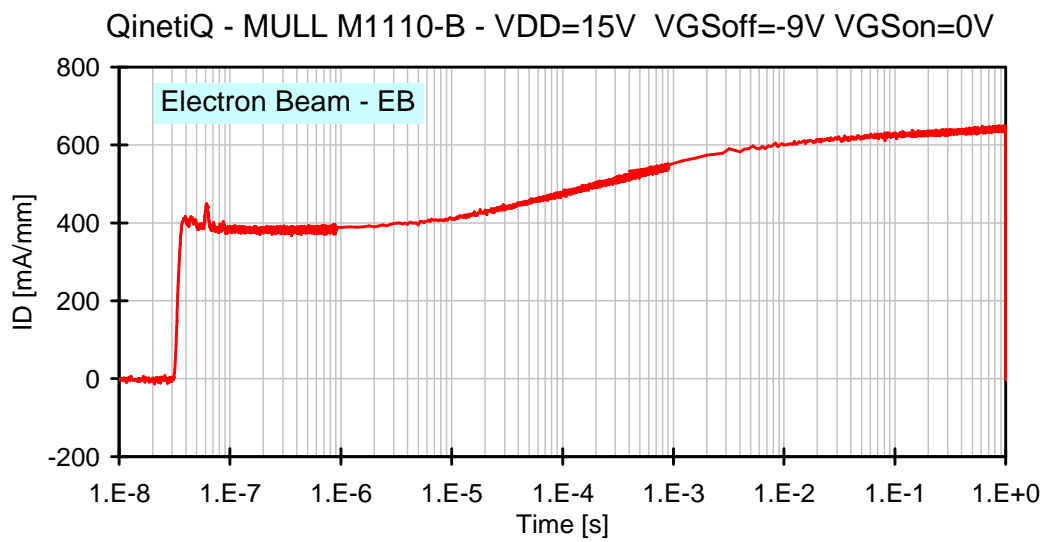
While dispersion in MULL devices, which present large dynamic shift of threshold voltage is possibly linked with a high density of deep levels in the Okmetic SiC substrate, the worsening of current collapse effects observed in PL devices with respect to EBL devices fabricated on the same wafer is certainly linked to specific process steps; surface damage or photo-resist residuals may be at the origin of the observed transient behaviour. Further information will be available after destructive failure analysis by cross-sectioning which will be carried out within WP4.4.



**Fig. 4.21:** gate-lag drain current "logarithmic pulse" of QinetiQ GIBSON HEMT processed with two different lithographic methods: (a) Photolithography; (b) Electron Beam lithography.



(a)



(b)

**Fig. 4.22:** gate-lag drain current "logarithmic pulse" of QinetiQ MULL HEMT processed with two different lithographic methods: (a) Photolithography; (b) Electron Beam lithography.

### 4.2.5 Transconductance dispersion as a function of frequency

Small-signal parameters characteristics of KorriGaN devices were also measured, in order to obtain a better understanding of the effects of the presence of bulk and surface deep levels on the circuit performances. Fig. 4.23 shows transconductance frequency dispersion measurements carried out at various temperatures from  $-40^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  in a QinetiQ MULL device biased at  $V_{GS} = 0$  V,  $V_{DS} = 2$  V using a gate sinusoidal signal with 50 mV amplitude. From the phase changes depicted in Fig. 4.24, an activation energy of 0.13 eV is obtained, as shown in the Arrhenius plot of Fig. 4.25.

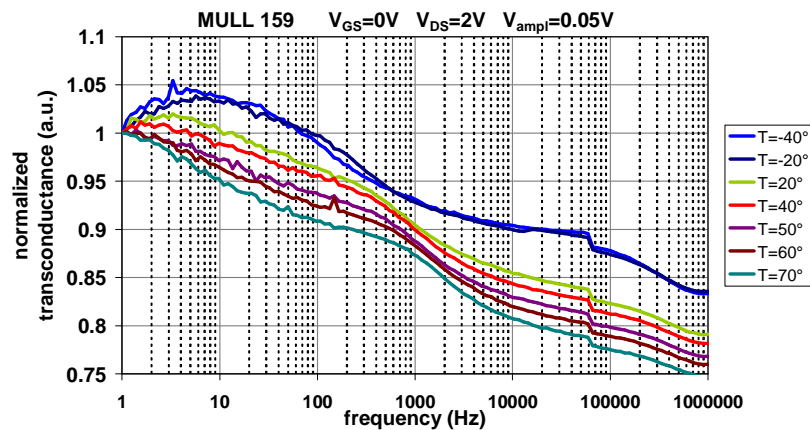


Fig. 4.23: transconductance frequency dispersion measured at different temperatures in QinetiQ MULL devices.

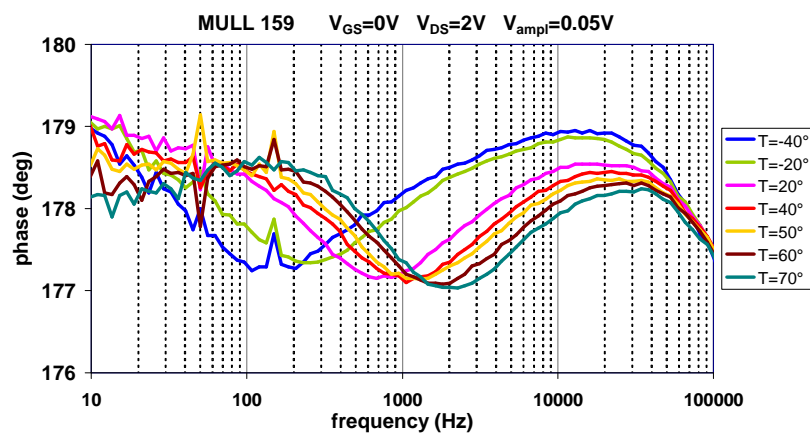
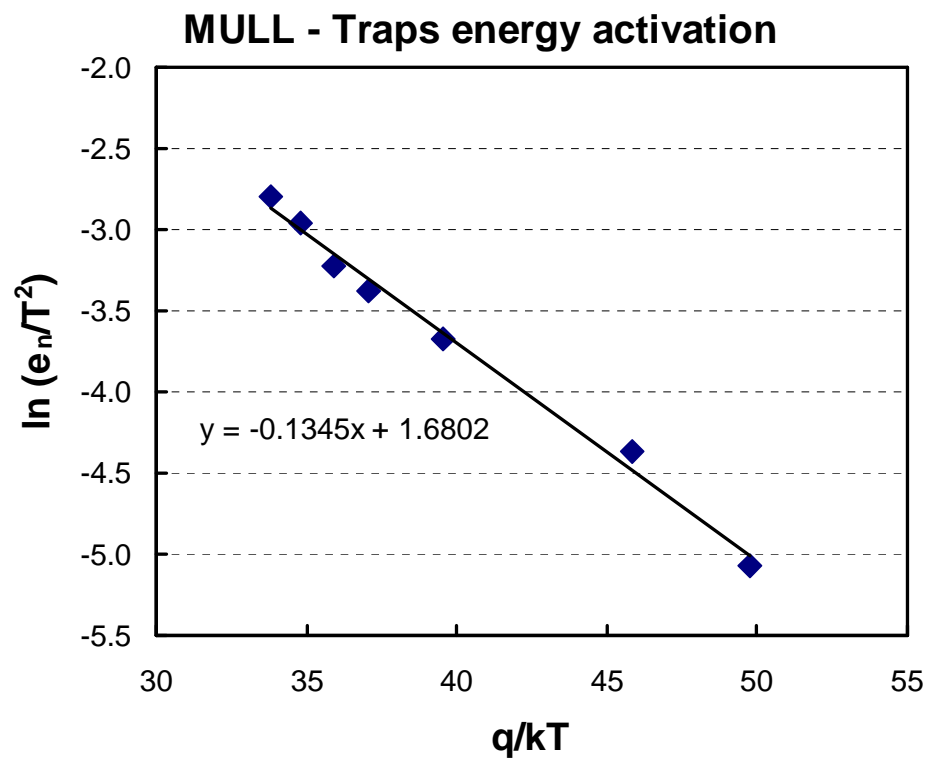


Fig. 4.24: phase shift frequency dispersion measured at different temperatures in QinetiQ MULL devices.



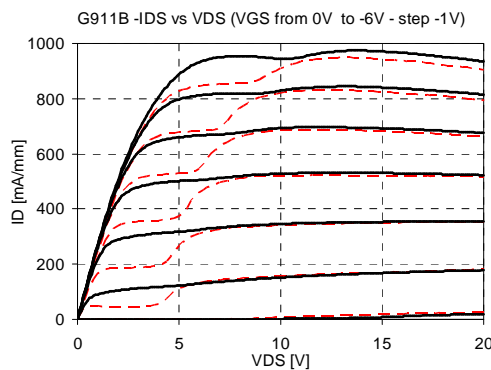
**Fig. 4.25:** activation energy extracted from the frequency phase shift of Fig. 4.24.

### 4.3 KINK EFFECTS

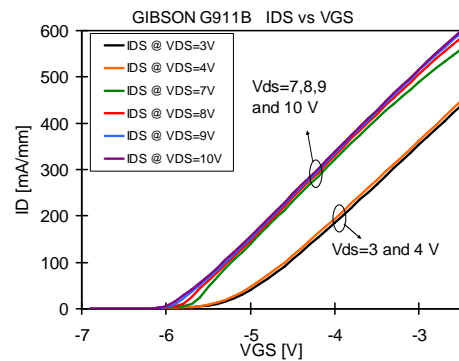
#### 4.3.1 Kink effect experimental characterization

The "kink" effect consists in a sudden, but small, increase in the drain current, taking place during DC  $I_D$  vs  $V_{DS}$  measurements when a certain  $V_{DS\_kink}$  value is exceeded. This effect is due to extremely slow traps within the epitaxial layers and/or their interfaces, and is not apparently related with the device surface. ISOM, QinetiQ and University of Padova intensively collaborated in the study of these parasitic phenomena. Main features of the kink effect may be summarized as follows:

- (a) in  $L_G = 0.6 \mu\text{m}$  HEMTs, the kink is observed only when long time constants and slow voltage sweeps were adopted, see Fig. 4.26;
- (b) the kink is due to a shift in the device threshold voltage: at  $V_{DS} < V_{DS\_kink}$ , the absolute value of the threshold voltage is smaller than at  $V_{DS} > V_{DS\_kink}$ , see Fig. 4.27;
- (c) independently from the process, devices adopting QinetiQ epitaxy are affected by the "kink" which, however, does not affect significantly power performances;



**Fig. 4.26:** output curve taken with short integration time mode (solid black line) and with long integration time mode (dashed red line).  $V_{GS}=0\text{V}$  are the top lines. QinetiQ GIBSON device.

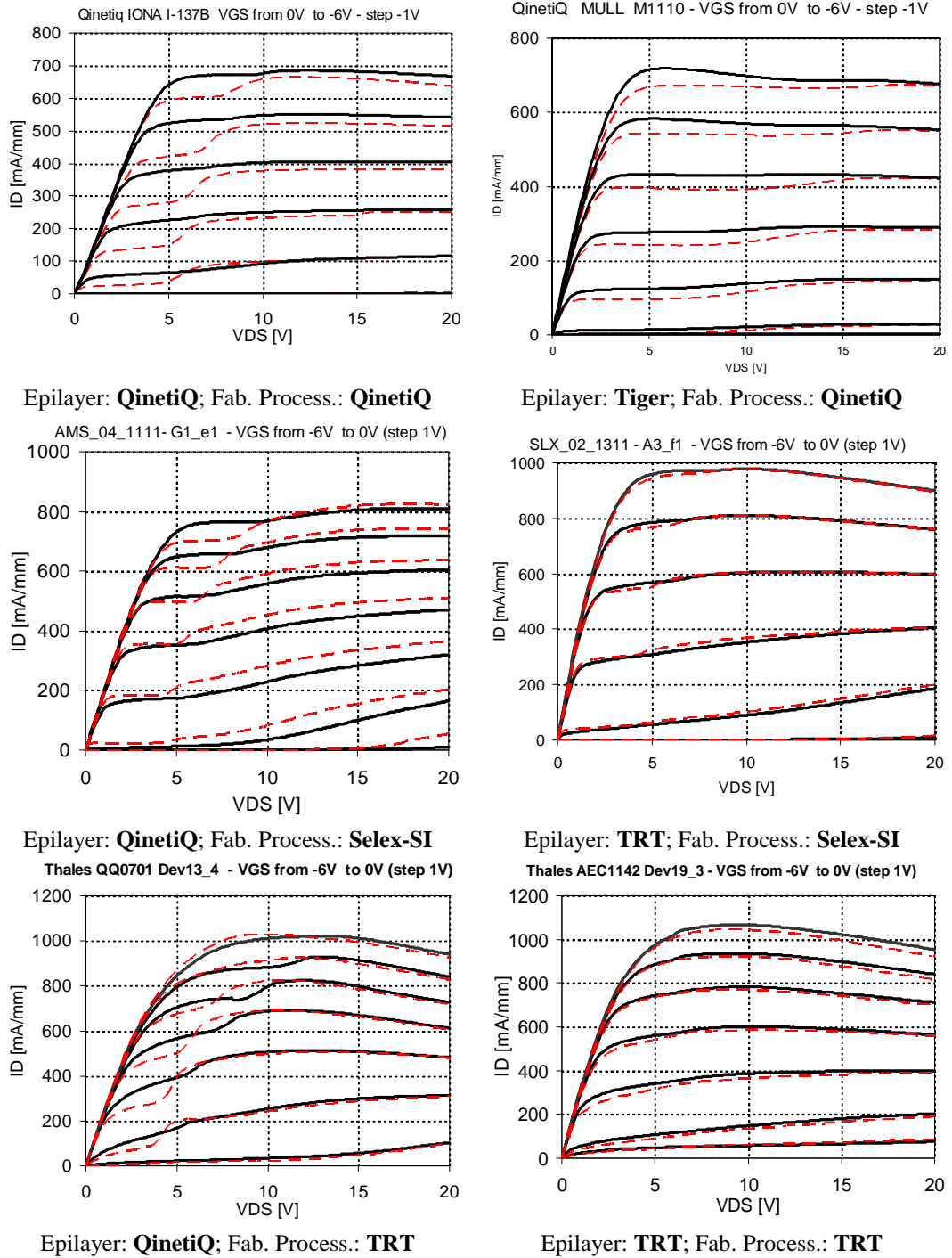


**Fig. 4.27:**  $I_D$  vs  $V_{GS}$  before (3 and 4  $V_{DS}$  values) and after (7-10 V  $V_{DS}$  values) the kink. The parallel shift of the  $I_{DS}$  curves after the kink is clearly due to a threshold voltage shift. QinetiQ GIBSON device.

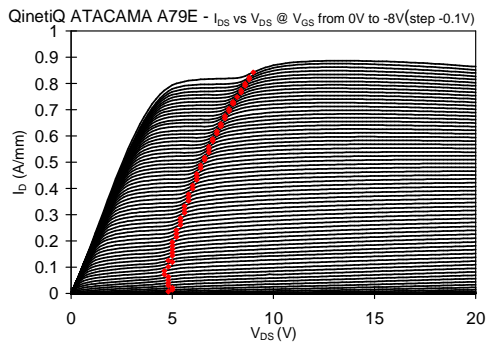
- (d) Table 4.3 and  $I_D$  characteristics from Fig. 4.28 to Fig. 4.33 compare different wafers from the point of view of the kink effects. Devices MULL with substrate SiC Okmetic and epi-layer TRT also show a small kink due to a threshold shift, but with significantly higher  $V_{DS\_kink}$  values, see Fig. 4.31 and Fig. 4.32. On the other hand, devices from wafer GREAT SANDY, fabricated by QinetiQ on TRT epitaxy and SiC Cree substrate within the same batch as ATACAMA and GIBSON, do not show the kink effect, see Fig. 4.33;
- (e) kink does not depend on the presence of passivation (it is present both before and after passivation) and on the presence of Fe in the GaN buffer layer;

**Table 4.3:** Presence of kink phenomena in the different studied devices. The devices with the kink effect have been highlighted by shading the cells. Clearly there is a correlation between presence of kink and epilayer supplier; all the epilayers coming from QinetiQ, even if processed in different site, present the kink phenomena. The I-V curved of some representative devices (highlighted in bold) have been plotted in Fig. 4.28.

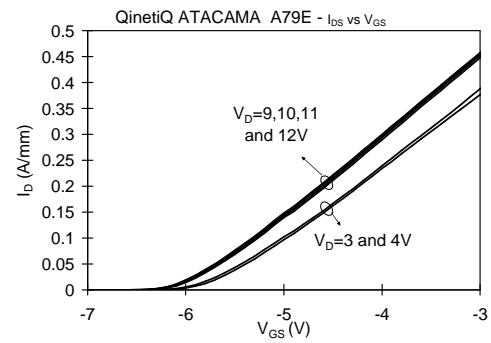
Fab	Wafer name	epilayer supplier	substrate	substrate supplier	KINK
<b>QINETIQ</b>	ATACAMA	QinetiQ	SiC	Cree	YES
	GIBSON	QinetiQ	SiC	Cree	YES
	<b>IONA</b>	<b>QinetiQ</b>	<b>SiC</b>	<b>Cree</b>	<b>YES</b>
	MULL	Tiger	SiC	Okmetic	NO
<b>SELEX</b>	AMS_00C_2623	Emcore	Sapphire		NO
	SLX_19_2212	Picogiga	SiC	Norstel	NO
	AMS_00A_2111	QinetiQ	SiC	Cree	YES
	AMS_00B_2121	QinetiQ	Sapphire	Cree	YES
	<b>AMS_04_1111</b>	<b>QinetiQ</b>	<b>SiC</b>	<b>Cree</b>	<b>YES</b>
	SLX_02_1311	TRT	SiC	Cree	NO
<b>THALES</b>	QQ0602	QinetiQ	SiC	Cree	YES
	<b>QQ0701</b>	<b>QinetiQ</b>	<b>SiC</b>	<b>Cree</b>	<b>YES</b>
	QQ0702	QinetiQ	SiC	Cree	YES
	AEC1148	Tiger	SiC	Okmetic	NO
	<b>AEC1142</b>	<b>TRT</b>	<b>SiC</b>	<b>Cree</b>	<b>NO</b>
	AEC1147	TRT	SiC	Cree	NO



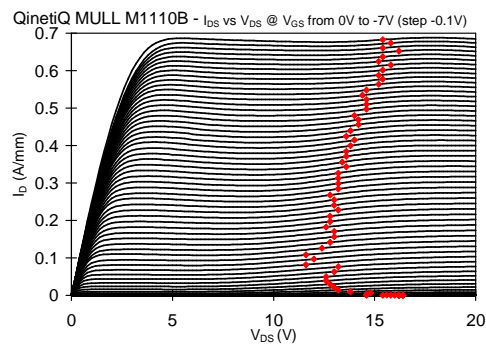
**Fig. 4.28:** output curve taken with short integration time mode (solid black line) and with long integration time mode (dashed red line).  $V_{GS} = 0$  V are the top lines.



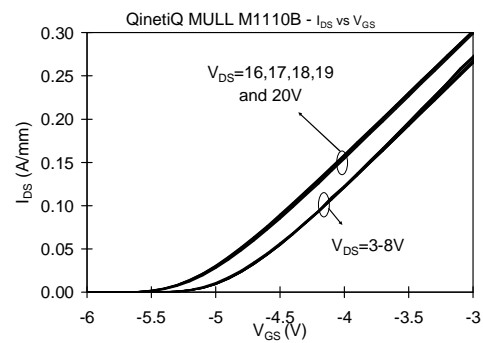
**Fig. 4.29:** Output characteristics with a small  $V_{GS}$  step. QinetiQ ATACAMA device. ( $W_G=100\mu\text{m}$ ,  $L_G=0.6\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.4\mu\text{m}$ ).



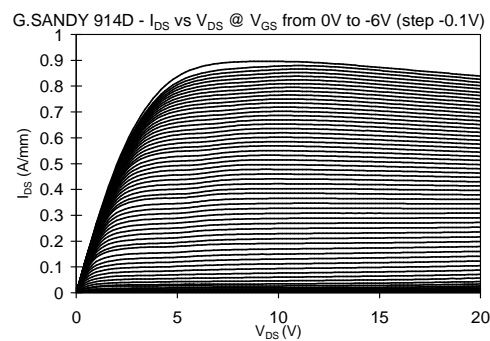
**Fig. 4.30:**  $I_D$  vs  $V_{GS}$  before ( $V_{DS} = 3$  and  $4\text{V}$ ) and after ( $V_{DS} = 9, 10, 11$  and  $12\text{V}$ ) the kink. The parallel shift of the  $I_D$  curves after the kink is clearly due to a threshold voltage shift. Same device of Fig. 4.29.



**Fig. 4.31:** Output characteristics with a small  $V_{GS}$  step. QinetiQ MULL device ( $W_G=100\mu\text{m}$ ,  $L_G=1\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.15\mu\text{m}$ ). OKMETIC substrate, epi TRT epi, QinetiQ processing..

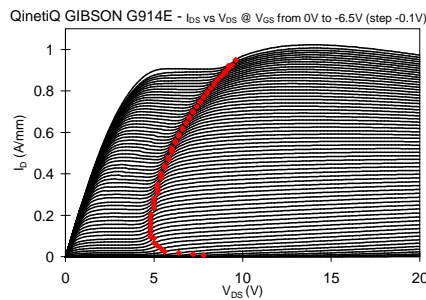


**Fig. 4.32:**  $I_D$  vs  $V_{GS}$  before ( $V_{DS} = 3-8\text{V}$ ) and after ( $V_{DS} = 16, 17, 18, 19$  and  $20\text{V}$ ) the kink. Same device of Fig. 4.31.

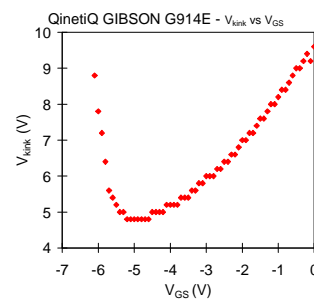


**Fig. 4.33:** output characteristics with a small  $V_{GS}$  step aimed at identifying “kinks” in the I-V characteristics. QinetiQ GREAT SANDY device ( $W_G=100\mu\text{m}$ ,  $L_G=0.6\mu\text{m}$ ,  $L_{DS}=5\mu\text{m}$ ,  $L_{GD}=3.4\mu\text{m}$ ).

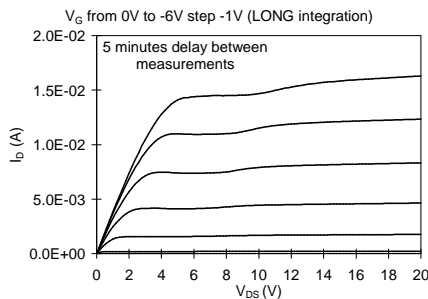
- (f) the  $V_{DS\_kink}$  value has a non-monotonic dependence on  $V_{GS}$ , see Fig. 4.34 and Fig. 4.35;
- (g) the kink is present also in the characteristics of long gate devices, see Fig. 4.36;  $V_{DS\_kink}$  does not change with the  $L_G$ , but the kink amplitude is lower in 50  $\mu\text{m}$  devices than in 100  $\mu\text{m}$  ones (see Fig. 4.36 and Fig. 4.37);
- (h) kink amplitude is lowered at increasing  $L_{GD}$ , see Fig. 4.38;
- (i) relevant memory effects contribute to hinder kink characterization: during repeated measurements, if  $V_{DS}$  exceeds  $V_{DS\_kink}$ , only the first curve will show a "kink" (i.e. if the device is biased at  $V_{DS} > V_{DS\_kink}$  this will temporarily remove the kink). The effect is recovered by keeping the device unbiased (at  $V_{GS}=V_{DS} = 0$  V) for at least 5 minutes, see Fig. 4.39 and Fig. 4.40;



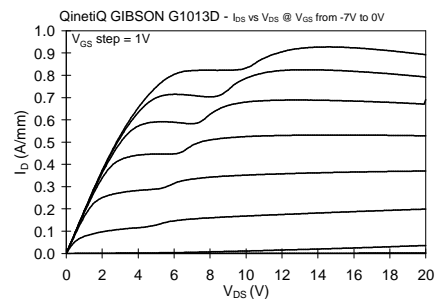
**Fig. 4.34:** output characteristics with a small  $V_{GS}$  step. Red diamonds correspond to the maximum of the output conductance in the kink region ( $V_{KINK}$ ). QinetiQ GIBSON device ( $W_G=100\mu\text{m}$ ,  $L_G=0.6\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.4\mu\text{m}$ ).



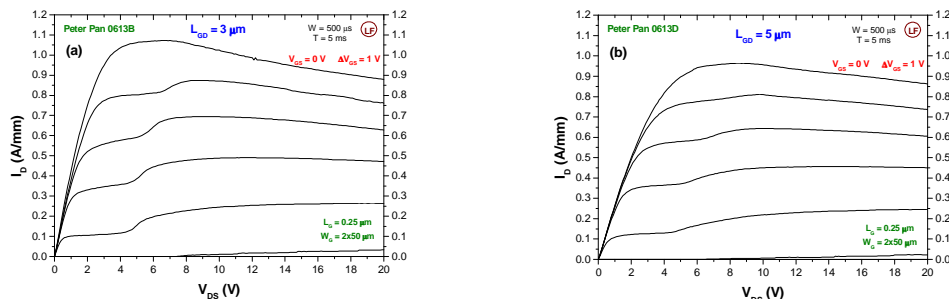
**Fig. 4.35:**  $V_{DS}$  values corresponding to maxima in output conductance ( $V_{KINK}$ ) vs  $V_{GS}$  (points identified in the previous figure). QinetiQ GIBSON device ( $W_G=100\mu\text{m}$ ,  $L_G=0.6\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.4\mu\text{m}$ ).



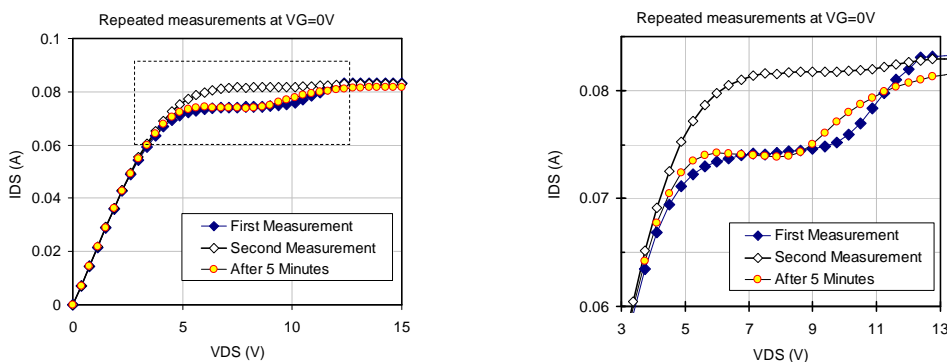
**Fig. 4.36:**  $I_D$ - $V_D$  of a GIBSON FATFET  $L_G= 50$   $\mu\text{m}$ ,  $W = 100\mu\text{m}$  device.



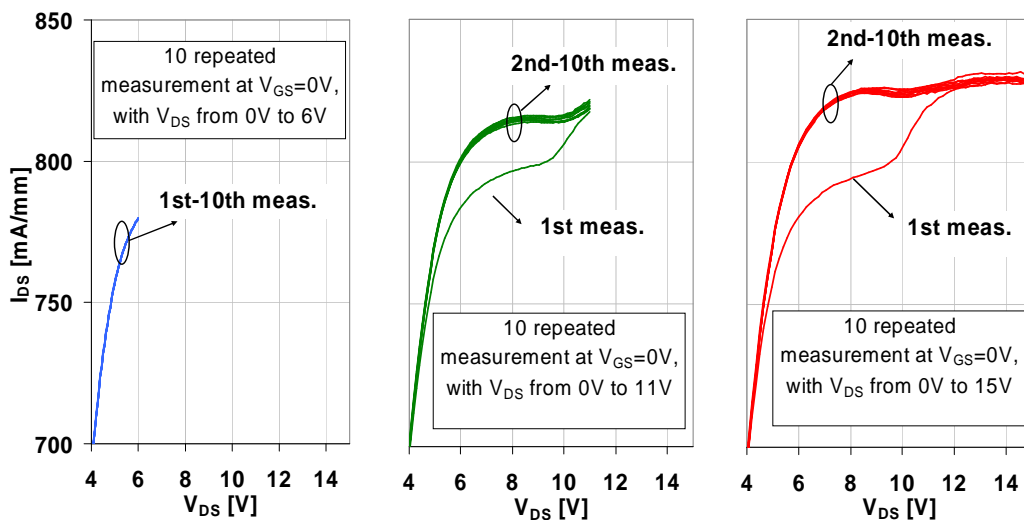
**Fig. 4.37:**  $I_D$ - $V_D$  of a  $L_G= 0.5$   $\mu\text{m}$ ,  $W=100\mu\text{m}$  GIBSON device.



**Fig. 4.38:**  $I_D$ - $V_{DS}$  measurements of QinetiQ PETER PAN transistors with  $L_{GD} = 3 \mu\text{m}$  (left) and  $L_{GD} = 5 \mu\text{m}$  (right). Pulsed measurements shown are equivalent to DC measurements for medium integration times.

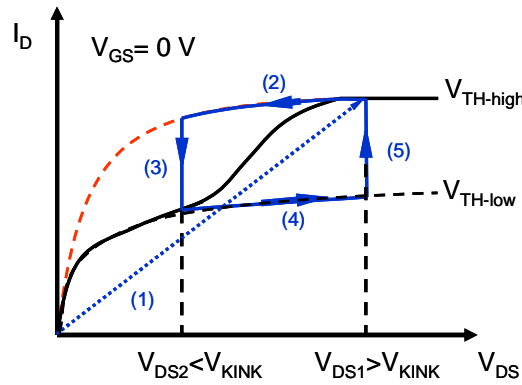


**Fig. 4.39:** repeated  $I_{DS}$  vs  $V_{DS}$  curves at Fixed  $V_{GS}=0V$ . Right measurements are the enlargement of the dashed box of the left figure. Measurements are taken with short integration time.

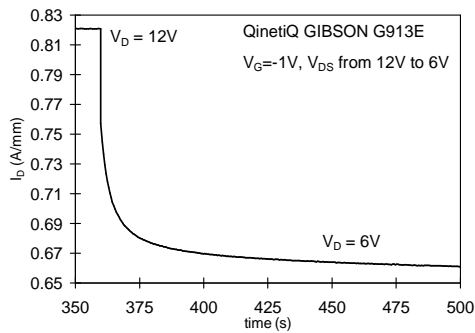


**Fig. 4.40:** same repeated (10 measurements)  $I_{DS}$  vs  $V_{DS}$  curves of previous figures with  $V_{GS}=0V$ .  $V_{DS}$  is swept from 0V to 6 V (blue curves, left figure), from 0 to 11 V (green curves, central figure), from 0 to 15 V (red curves, right figure). Measurements are taken with short integration time.

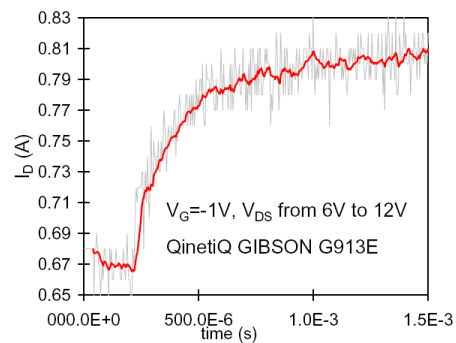
- (j) pulsed measurements of the kink effect have been carried out by switching  $V_{DS}$  from 0 V to  $V_{DS1} > V_{KINK}$  (1), and, after having reached equilibrium, from  $V_{DS1}$  to  $V_{DS2} < V_{KINK}$  (2), waiting for the transient (3), switching back  $V_{DS}$  from  $V_{DS2}$  to  $V_{DS1} > V_{KINK}$  and waiting for the transient (5), Fig. 4.41. Negative charge build-up takes place during transient (3), corresponding to a fast electron capture process, followed by an extremely slow transient (several s). During this transient drain current and the absolute value of threshold voltage decrease, Fig. 4.42. Detrapping or charge compensation takes place during transient (5), with typical times of the order of ms, drain current and threshold voltage recover, Fig. 4.43;



**Fig. 4.41:** ideal  $I_D$  vs  $V_{DS}$  characteristics showing I-V trajectories during a pulsed kink characterization.  $V_{GS}$  is kept at 0 V.  $V_{DS}$  is switched from 0 V to  $V_{DS1} > V_{KINK}$  (1), and, after having reached equilibrium from  $V_{DS1}$  to  $V_{DS2} < V_{KINK}$  and back. Negative charge build-up takes place during (3), and detrapping or compensation during (5).

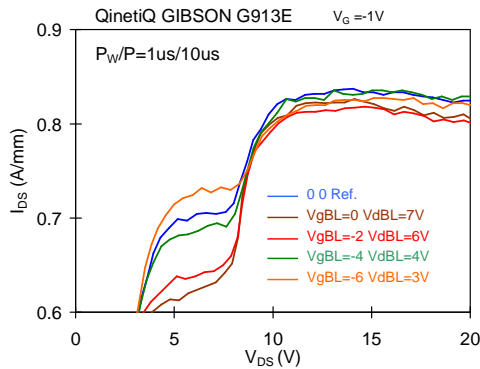


**Fig. 4.42:** Drain current transient corresponding to (3) in Fig. 4.41, i.e. during negative charge build-up. QinetiQ GIBSON device ( $W_G=100\mu\text{m}$ ,  $L_G=0.6\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.4\mu\text{m}$ ).

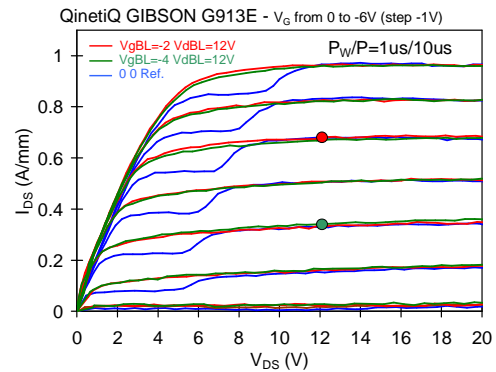


**Fig. 4.43:** Drain current transient corresponding to (5) in the Fig. 4.41, i.e. during detrapping or compensation. QinetiQ GIBSON device ( $W_G=100\mu\text{m}$ ,  $L_G=0.6\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.4\mu\text{m}$ ).

(k) the negative charge build-up leading to a decrease in  $I_D$  when  $V_{DS} < V_{DS\_kink}$  is enhanced when both channel electron and a high electric field are simultaneously present. Fig. 4.44 shows pulsed output characteristics obtained in a QinetiQ GIBSON device by varying the baseline values. It can be noticed that, even if negative charge build-up also occurs when the device is kept unbiased or in pinch-off conditions, maximum kink amplitude is observed for  $V_{GS-bl}=0$  V,  $V_{DS-bl}=7$  V, while the lowest amplitude corresponds to  $V_{GS-bl}=-6$  V,  $V_{DS-bl}=3$  V, which actually induces less kink than  $V_{GS-bl}=0$  V,  $V_{DS-bl}=0$  V despite the higher  $V_{GD}$  value. When  $V_{DS} > V_{kink}$  is used as baseline, negative charge compensation or detrapping takes place, and the kink disappears, see Fig. 4.45;



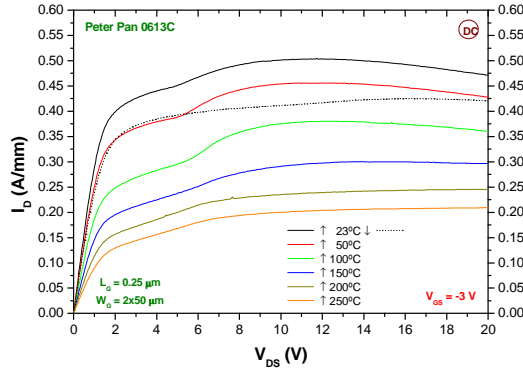
**Fig. 4.44:** double-pulse  $I_D$ - $V_{DS}$  characteristics of a QinetiQ GIBSON device ( $W_G=100\mu\text{m}$ ,  $L_G=0.6\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.4\mu\text{m}$ ) measured with a  $10\mu\text{s}$  period, and a  $1\mu\text{s}$  pulse width ( $V_{GS}=-1$  V,  $V_{DS}$  from 0 to 20 V). Different baseline values for  $V_{GS-bl}$ ,  $V_{DS-bl}$  have been adopted, choosing  $V_{DS-bl} < V_{KINK}$ . Negative charge build-up takes place and, as a consequence, kink amplitude, depends on baseline values.



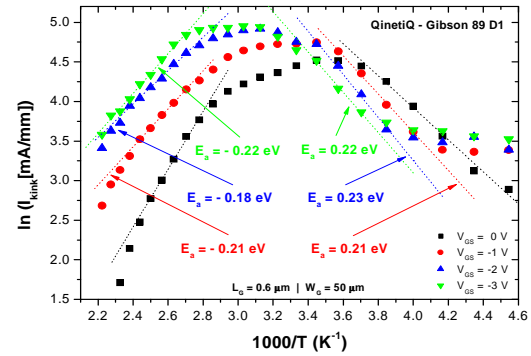
**Fig. 4.45:** double-pulse  $I_D$ - $V_{DS}$  characteristics of a QinetiQ GIBSON device ( $W_G=100\mu\text{m}$ ,  $L_G=0.6\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.4\mu\text{m}$ ) measured with a  $10\mu\text{s}$  period, and a  $1\mu\text{s}$  pulse width ( $V_{GS}$  from 0V to -6V step -1V,  $V_{DS}$  from 0 to 20 V). Different baseline values for  $V_{GS-bl}$ ,  $V_{DS-bl}$  have been adopted, choosing  $V_{DS-bl} > V_{KINK}$  (the  $V_{GS-bl} = 0$  V,  $V_{DS-bl} = 0$  V is also shown as a reference). As a result, negative charge detrapping or compensation takes place, and the kink disappears.

(l) the kink behaviour as a function of temperature is non-monotonic, so that the kink first increases at increasing the temperature, reaches a maximum amplitude around R.T., and then decreases again, see Fig. 4.46 and Fig. 4.47. Kink amplitude seems to be thermally activated, (for  $T < \text{R.T.}$ ) or

deactivated (for  $T > \text{R.T.}$ ), with activation energies ranging from 0.18 eV to 0.25 eV.



**Fig. 4.46:** evolution of the kink effect as devices are heated. The dotted line is obtained after the thermal cycle.

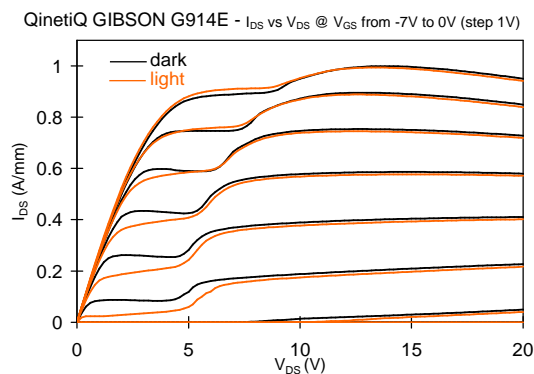


**Fig. 4.47:** evolution of the  $I_{\text{kink}}$  and its activation energies for the transistor 89D1 at  $V_{\text{GS}} = 0, -1, -2$  and  $-3$  V.

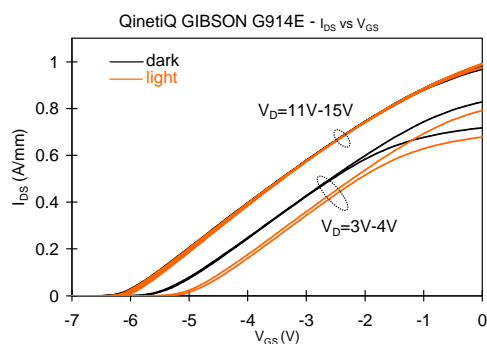
**Table 4.4:** Summary of the activation energies for some of the devices measured.

$V_{\text{GS}}$	$E_a (I_{\text{kink}})$					
	Gibson 87 C2 ( $L_G = 0.5 \mu\text{m}$ )		Gibson 89 D1 ( $L_G = 0.6 \mu\text{m}$ )		G 910 D ( $L_G = 0.6 \mu\text{m}$ )	G 99 B ( $L_G = 1 \mu\text{m}$ )
	LT	HT	LT	HT	HT	HT
0 V	0.22 eV	-0.16 eV	0.17 eV	-0.32 eV	-0.34 eV	-0.30 eV
-1 V	0.19 eV	-0.15 eV	0.21 eV	-0.21 eV	-0.32 eV	-0.32 eV
-2 V			0.23 eV	-0.18 eV	-0.19 eV	-0.29 eV
-3 V			0.22 eV	-0.22 eV	-0.11 eV	-0.13 eV

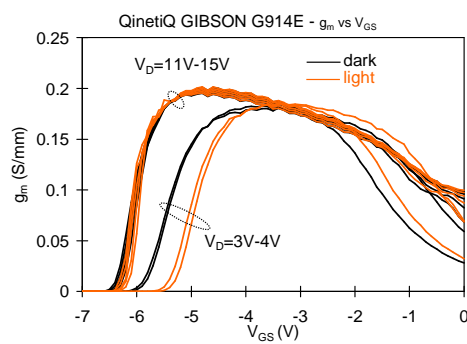
(m) rather surprisingly, if the device is illuminated using an incandescent lamp, the kink amplitude increases, see Fig. 4.48, Fig. 4.49, and Fig. 4.50. We have repeated the characterization using monochromatic light in the 0.8 eV – 3.32 eV energy range and measured the amplitude of the kink, see Fig. 4.51. A non-monotonic behaviour of the kink amplitude as a function of photon energies has been detected: kink is enhanced for  $E > 1$  eV approximately, and is lowered for  $E > 2$  eV. Fig. 4.52 shows kink amplitude as a function of  $V_{\text{GS}}$  with the device illuminated by radiation of different wavelengths. Fig. 4.53 clarifies the role of light in determining the kink amplitude: light having  $E < 2$  eV enhances trapping at  $V_{\text{DS}} < V_{\text{KINK}}$ , leading to a decrease in  $I_{\text{D}}$ ; for  $E > 2$  eV, electron detrapping is favoured, leading to an increase in  $I_{\text{D}}$  at  $V_{\text{DS}} < V_{\text{KINK}}$ .



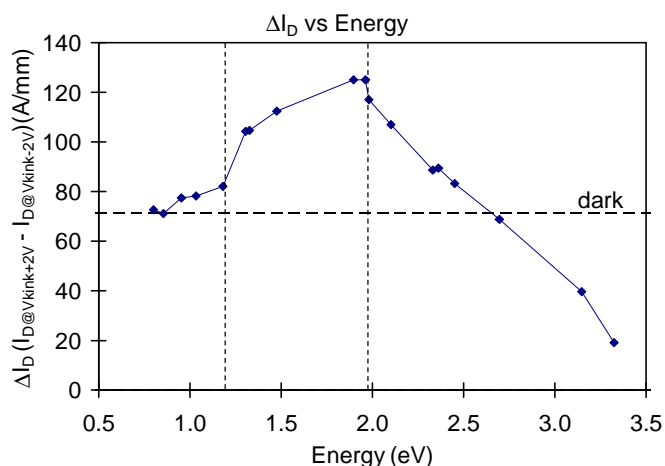
**Fig. 4.48:** output characteristics of a QinetiQ GIBSON device ( $W_G=100\mu\text{m}$ ,  $L_G=0.6\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.4\mu\text{m}$ ) measured in the dark (black) and under illumination (orange) using an incandescent lamp.



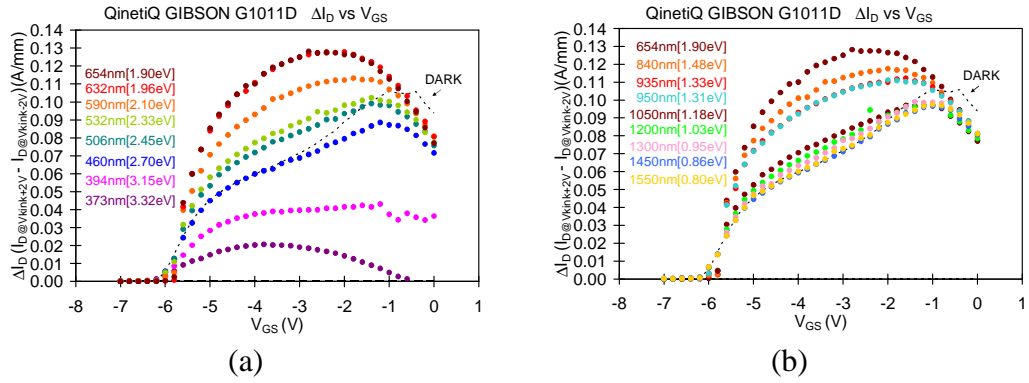
**Fig. 4.49:**  $I_D$  vs  $V_{GS}$  characteristics of a QinetiQ GIBSON device ( $W_G=100\mu\text{m}$ ,  $L_G=0.6\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.4\mu\text{m}$ ) measured in the dark (black) and under illumination (orange) using an incandescent lamp.



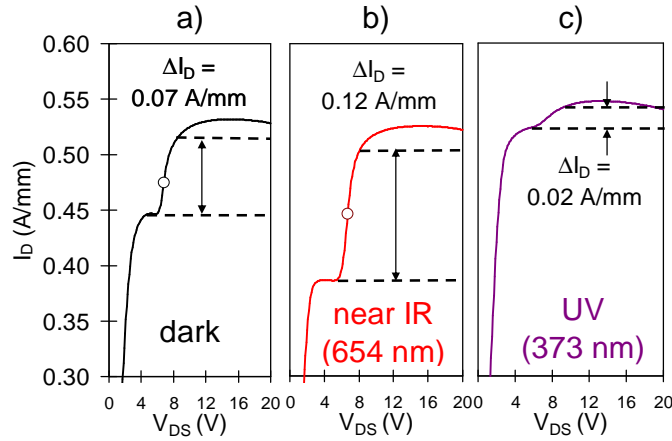
**Fig. 4.50:** transconductance  $g_m$  vs  $V_{GS}$  of a QinetiQ GIBSON device ( $W_G=100\mu\text{m}$ ,  $L_G=0.6\mu\text{m}$ ,  $L_{DS}=4\mu\text{m}$ ,  $L_{GD}=2.4\mu\text{m}$ ) measured in the dark (black) and under illumination (orange) using an incandescent lamp.



**Fig. 4.51:** kink amplitude VS monochromatic source energy. GIBSON G1011D device ( $W_G=100\mu\text{m}$ ,  $L_G=0.6\mu\text{m}$ ,  $L_{DS}=5\mu\text{m}$ ,  $L_{GD}=3.4\mu\text{m}$ ).



**Fig. 4.52:** kink amplitude VS  $V_{GS}$ . Device was subjected to different monochromatic source: (a) from 373 nm to 654 nm; (b) from 654 nm to 1550 nm. GIBSON device ( $W_G=100\mu m$ ,  $L_G=0.6\mu m$ ,  $L_{DS}=5\mu m$ ,  $L_{GD}=3.4\mu m$ ).



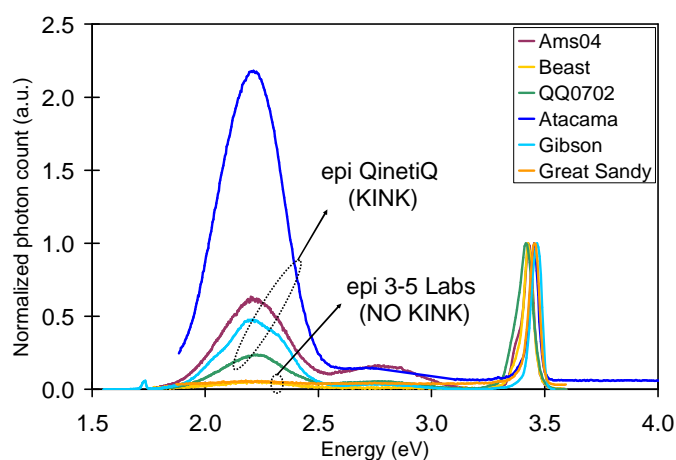
**Fig. 4.53:** enlargement of  $I_D - V_D$  at  $V_{GS} = -3 V$ . Measurements were performed in a) dark condition, and with devices illuminated by (b) 373 nm and (c) 654 nm continuous monochromatic light sources. The  $\Delta I_D$  values are reported. GIBSON G1011D device ( $W_G=100\mu m$ ,  $L_G=0.6\mu m$ ,  $L_{DS}=5\mu m$ ,  $L_{GD}=3.4\mu m$ ).

(n) finally, we have characterized different epilayers using cathodoluminescence (CL) in a Scanning Electron Microscope (SEM). Table 4.5 shows the list of the samples which have been submitted to analysis. During the analysis, we carefully controlled experimental conditions, keeping constant the electron beam accelerating energy (10 kV) and the beam current. Spectra were measured at  $T = 77 K$ . Six wafers have been tested, four having QinetiQ epitaxy, the remaining two adopting 3-5 Labs epitaxy. The four wafers marked in blue in the table have been independently processed by QinetiQ, III-V Labs and Selex foundries, and are affected by the kink, as verified by I-V DC measurements with long

time constants. All these wafers present a peak around 2.2 eV in the CL spectra, see Fig. 4.54, where the spectra have been renormalized taking as reference the amplitude of the GaN peak. The intensity of this "Yellow Luminescence" (YL) peak is almost undetectable in the other two wafers (Great Sandy and Beast), with 3-5 Labs epitaxy and QinetiQ processing, which do not show remarkable kinks in the I-V characteristics.

**Table 4.5:** List of substrates evaluated by cathodoluminescence in a Scanning Electron Microscope.

Wafer	Epitaxy	Process	KINK	Y.L.
ATACAMA	QinetiQ	QinetiQ	YES	YES
GIBSON	QinetiQ	QinetiQ	YES	YES
QQ0702	QinetiQ	3-5 Labs	YES	YES
AMS04	QinetiQ	Selex	YES	YES
GREAT SANDY	3-5 Labs	QinetiQ	NO	NO
BEAST	3-5 Labs	QinetiQ	NO	NO



**Fig. 4.54:** normalized cathodoluminescence spectra on Atacama, Great Sandy and Gibson wafers at 77 K. The three spectra are normalized respect the GaN peak at about 3.45 eV. The yellow luminescence peak is evident on Atacama and Gibson wafers (QinetiQ epitaxy), while it is negligible on Great Sandy wafer (TRT epitaxy).

### 4.3.2 Origin of the KINK effect

The experimental observations summarized in the last Section suggest that the kink is due to the presence of traps in the epitaxial layers under the gate. When electron trapping takes place, the negative charge shifts the device threshold

voltage towards more positive values, thus decreasing the drain current, as described at points (b), (c) and (k) of the previous section. Electron trapping takes place for  $V_{DS} < V_{DS\_kink}$ , or when the device is unbiased, see points (a), (b), (h); for  $V_{DS} > V_{DS\_kink}$ , electron detrapping or compensation occurs, thus restoring the nominal value of  $V_{TH}$ , see point (b). This effect is not governed by electric field; in fact,  $V_{DS\_kink}$  has a non-monotonic dependence on  $V_{GS}$ , see Fig. 4.34, which is typical of impact-ionization effects: close to the device pinch-off value,  $V_{DS\_kink}$  decreases at increasing  $V_{GS}$ , as more channel electrons are available; beyond a certain value of  $V_{GS}$ , however, the effect of the decrease in the electric field prevails; impact-ionization becomes less probable due to the lower electron energy, and  $V_{DS\_kink}$  increases again, see Fig. 4.34. In low energy bandgap devices, like GaAs-based or InP-based HEMTs, impact-ionization generated holes compensate the negative charge, thus originating the kink [29]; since in these devices we did not observe any sign of impact-ionization like light emission due to band-to-band recombination or increase in negative gate current, we think that energetic electrons may impact-ionize traps, thus reducing the trapped negative charge and inducing the kink [30]. Trapping does not occur instantaneously; moreover, it requires a certain electron energy in order to occur: 5 minutes at  $V_{DS} = V_{GS} = 0$  V are needed to build-up the negative charge required to generate the kink, but when drain voltage is dynamically switched from  $V_{DS} = 12$  to  $V_{DS} = 6$  V, ( $V_{GS} = -1$ ),  $I_D$  decreases from 0.82 to 0.75 A/mm due to trapping in  $\approx 1$   $\mu$ s, followed by a very long transient, extending over several tens of seconds. It seems that electrons should achieve a certain energy in order to interact with traps and get trapped; this process can be thermally activated (trapping occurs also at  $V_{DS} = V_{GS} = 0$  V), or can be promoted by providing energy to channel electrons through the electric field. Electron injection from the gate into the channel due to tunneling does not seem to be an efficient trapping mechanism. In fact, 10  $\mu$ s pulses at  $V_{GS} = -6$  V,  $V_{DS} = 3$  V produce less trapping than pulses at  $V_{GS} = 0$  V,  $V_{DS} = 0$  V, while trapping is greatly enhanced by pulsing at  $V_{GS} = 0$  V,  $V_{DS} = 7$  V, i.e. when energetic electrons are present in the channel, despite the lower  $V_{GD}$  value, see Fig. 4.44. As a consequence, trapping is less efficient and kink

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amplitude is reduced when  $L_{GS}$  and/or  $L_{GD}$  are increased, see Fig. 4.36 and Fig. 4.38. The behaviour of the kink effect as a function of temperature is consistent with the above described mechanisms: kink amplitude reaches a maximum around R.T.; if the temperature is decreased, less trapping occurs, and its amplitude decreases; if temperature is increased above R.T., both trapping and degradation of carrier transport properties contribute to decrease  $I_D$  and reduce kink amplitude, see Fig. 4.46 and Fig. 4.47. In order to study the properties of deep levels in these devices, we carried out photocurrent and cathodoluminescence experiments. Photocurrent measurements, Fig. 4.51 and Fig. 4.52, show that photons with energy  $E$  in the 0.85 eV to 2.0 eV enhance trapping effects (the pre-kink  $I_D$ , for  $V_{DS} < V_{DS\_kink}$ , is lower than in the dark), while when  $E > 2.0$  eV, detrapping is promoted (and the pre-kink current is enhanced). Cathodoluminescence spectra have been measured on ATACAMA, GIBSON and GREAT SANDY QinetiQ devices; HEMTs have been fabricated by QinetiQ on these three wafers using the same process batch; ATACAMA and GIBSON adopted QinetiQ epitaxy on Cree SiC; GREAT SANDY was based on TRT epitaxy. An intense yellow band peak (between 2.0 eV and 2.5 eV approximately) was detected in ATACAMA and GIBSON devices, which was practically undetectable in GREAT SANDY samples. Recent results [31]-[32]; concerning yellow luminescence in undoped GaN have proposed model similar to that reported in Fig. 4.55, which could be in agreement with our observations of the kink enhancement consequent to illumination. In fact, illumination with photons having energy  $E > 0.87$  eV could promote electron transitions from the valence band into the deep acceptor level  $A_D$  at  $E_V + 0.87$  eV; when approximately 2.0 eV are reached, electrons can be transferred to the deep donor level from where they can be easily removed by thermionic emission or tunneling. An explanation of the kink effect based on the interaction of a deep acceptor state with hole generation by impact-ionization has been already presented for AlGaAs/GaAs HEMTs (Verzellesi EDL Selex). In the case of the QinetiQ devices, a model based on a deep acceptor state coupled with direct trap impact-ionization could explain the observed features of the kink effect

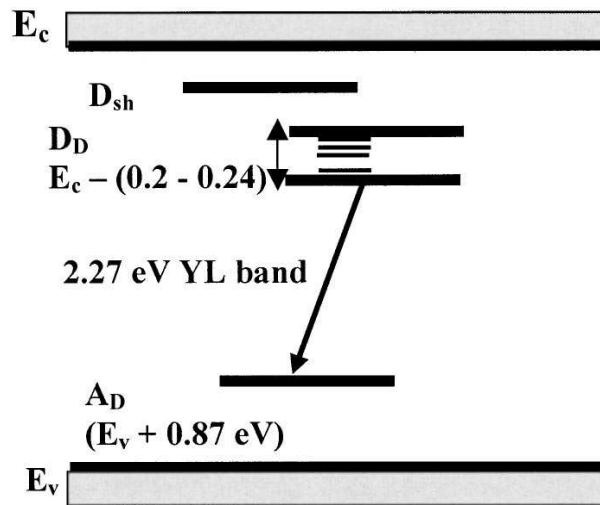


Fig. 4.55: Proposed model for the yellow luminescence transitions in undoped GaN.

### 4.3.3 Material evaluation by means of DLTS

Drain current Deep Level Transient Spectroscopy (DLTS) measurements have been carried out by applying a voltage pulse with a peak value of  $-4\text{V}$  to the gate of the device. The drain current transient after switching the gate voltage to  $-2\text{V}$  was measured by DLTS technique. The measurements were carried out by biasing the devices at  $V_{DS}$  values of  $5\text{V}$ . As can be seen in Fig. 4.56 the same hole-like trap was observed for SLX25 and SLX02 samples while two hole-like traps have been extracted for the sample Great Sandy. For the Great Sandy sample the trap at  $0.52\text{eV}$  was observed at  $V_{DS} = 5\text{V}$  as for the other two samples, while the traps at  $0.32\text{eV}$  was extracted at  $V_{DS} = 10\text{V}$ . DLTS measurements also showed the presence of electron-like traps whose Arrhenius plot are depicted in Fig. 4.57.

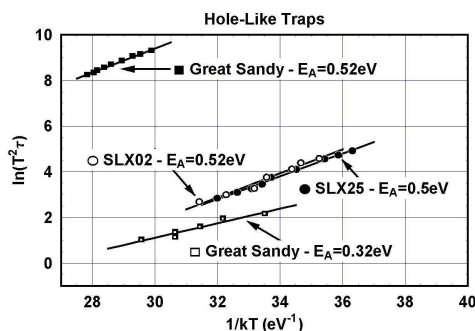


Fig. 4.56: Arrhenius plot of the hole-like traps observed during current-DLTS measurements.

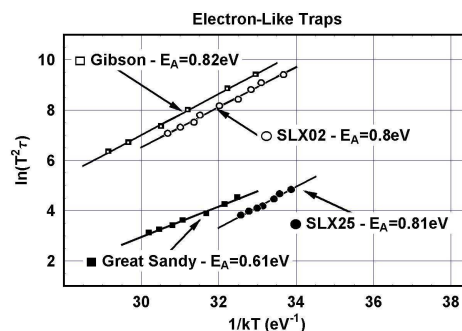


Fig. 4.57: Arrhenius plot of the electron-like traps observed during current-DLTS measurements.

# CONCLUSION

In this thesis results concerning the electrical characterization and reliability analysis of AlGaIn/GaN High Electron Mobility Transistor (HEMTs) grown epitaxially on composite SiCopSiC, SopSiC and silicon substrate processed in the frame of the European HYPHEN project have been reported. A full set of electrical characterization, DC, Pulsed and RF has been carried out. The obtained results are summarized in the follow:

## **Highlight:**

By comparing the results obtained in 1<sup>st</sup>-batch devices as well as the state of the art device to those of 2<sup>nd</sup>-batch HYPHEN devices (Si, SiCopSiC and SopSiC), the electrical performance observed are very well in line:

- a) the main DC parameters ( $I_{Dsat}$ ,  $g_{m-max}$ ,  $I_G$ ,  $V_{th}$ ) have improved with respect of 1<sup>st</sup>-batch devices and are pretty much approaching the values obtained in devices made processed in more conventional substrates (SiC, Sapphire);
- b) devices with reduced gate leakage current and limited current collapse have been obtained, providing a very good improvements with respect to 1<sup>st</sup>-batch;
- c) breakdown characterization demonstrate very promising values (beyond 100 V for SopSiC devices and about 90 V for SiCopSiC devices);
- d) excellent RF performances have been obtained: 4.5 W/mm power densities have been achieved on SopSiC devices representing a record for devices grown on non-SiC substrate.

## **Lowlight:**

- a) still some 2<sup>nd</sup>-batch devices present current collapse and relatively high current level, however the problem is much less severe than in 1<sup>st</sup>-batch;

- b) at very high bias condition, current collapse appears, however under these very severe conditions, also conventional devices grown on SiC substrate can be affected by current collapse.

Very promising reliability performances has been observed in almost all tested devices by means of a short-term step-stress experiment, showing good devices stability up to  $V_{DS} = 50$  V. Some SopSiC devices have been exposed to a 1000 hours long-term stress, showing no significant ageing effects. All these data confirm that the layer transfer based composite substrates are very promising for high performance low-cost RF GaN HEMT structures for power applications.

In the second half of this work, the results obtained within the "Parasitic effects" workpackage of the "Reliability" subproject of the KorriGaN project have been reported. The "current slump" or "current collapse" effect have been studied by means of double pulse experiments, adopting a custom-made set-up. The current collapse is a decrease of drain current which takes place when the device is pulsed between pinch-off (typically  $V_{DS} = 20$  V,  $V_{GS} = -8$  V) and open channel conditions with respect to DC or to pulsed  $I_D - V_{DS}$  measurements carried out from baseline ( $V_{DS} = 0$  V,  $V_{GS} = 0$  V). This current slump obviously reduces the RF power of the devices, and is usually attributed to trapping effects, which can take place at the device surface or within the epilayer and its interfaces. The highest contribution to current slump usually comes from traps at the surface, as demonstrated by the fact that suitable passivation using SiN or SiO/SiN greatly improves current collapse. Most KorriGaN devices preserve at least 80% of their DC current in pulsed conditions). The "kink" effect in the DC characteristics has been also studied. This phenomenon consists in a sudden, but reduced, increase in the drain current that take place during DC  $I_D$  vs  $V_{DS}$  measurements when a certain  $V_{DS\_kink}$  value is exceeded. The kink effect is due to extremely slow traps within the epitaxial layers and/or their interfaces, and is not apparently related with the device surface. Concerning KorriGaN devices, only wafers adopting a certain epitaxy (i.e. QinetiQ) are affected by the kink, independently from the fabrication process. A photo-current experiment have confirmed the above

mentioned statements, demonstrating that kink amplitude is strictly correlated with the wavelength of the monochromatic source that illuminated the devices. The study of the dependence of "KINK effect" on device geometry, together with measurements as a function of temperature, photocurrent spectroscopy, DLTS and cathodoluminescence spectroscopy within the adoption of a SEM have shown that kink effect is due to the presence of deep levels within the undoped GaN layer, possibly related with the observation of yellow luminescence in the CL spectra.



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# **APPENDIX I: SELECTED DC MEASUREMENTS FOR HYPHEN DEVICES**

In this appendix the DC characterizations of HYPHEN wafers are reported as reference. The diagrams about a representative device for each device are presented, in particular:

Reference:

- AEC1142
- AEC1147

IEMN:

- AEC1345
- L895
- AEC1341
- LO-792
- LO-896
- LO-1055
- AEC1470

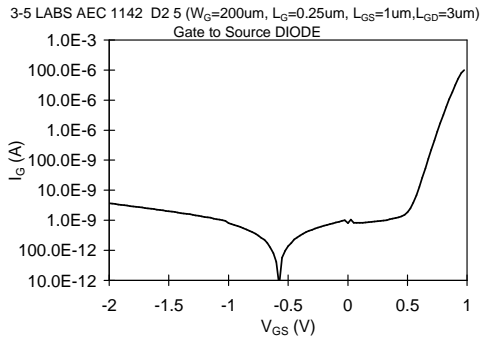
3-5 Labs:

- AEC1313

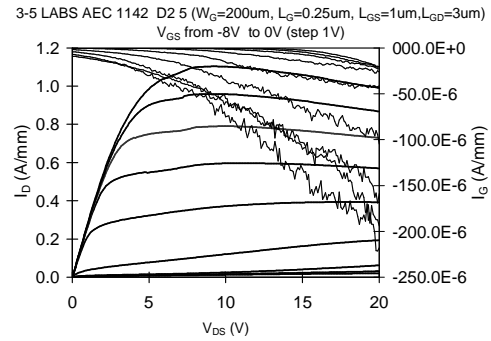
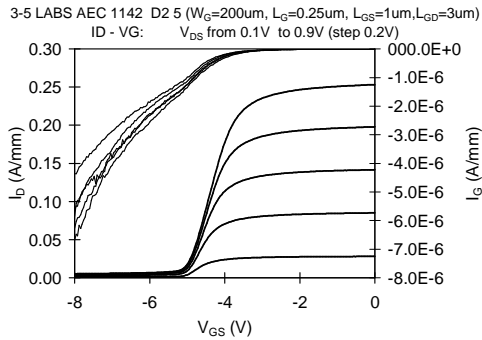
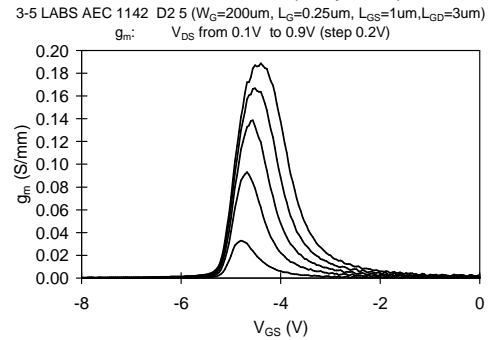
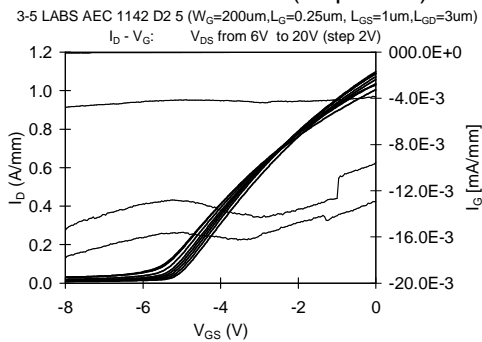
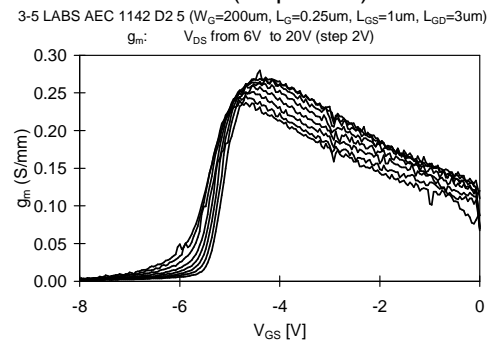
UMS:

- AEC1333
- AEC1337
- L1053
- L909
- L1338
- L879

### 3-5 Labs AEC1142 [REFERENCE SiC substrate] [ $W_G = 200 \mu\text{m}$ , $L_G = 0.25 \mu\text{m}$ , $L_{GS} = 1 \mu\text{m}$ , $L_{GD} = 3 \mu\text{m}$ ]

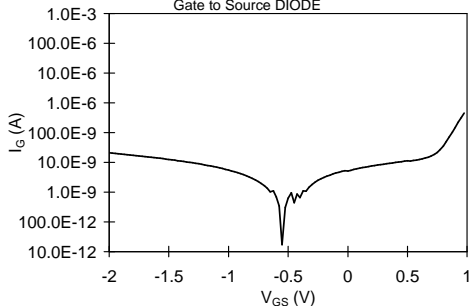


a) gate-to-source I-V characteristic

b)  $I_D$ - $V_{DS}$  and  $I_{GS}$ - $V_{DS}$  characteristic at  $V_{GS}$  from -8 V to 0 V (step 1 V)c)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 0.1 V to 0.9 V (step 0.2 V)d)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 0.1 V to 0.9 V (step 0.2 V)e)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 6 V to 20 V (step 2 V)f)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 6 V to 20 V (step 2 V)

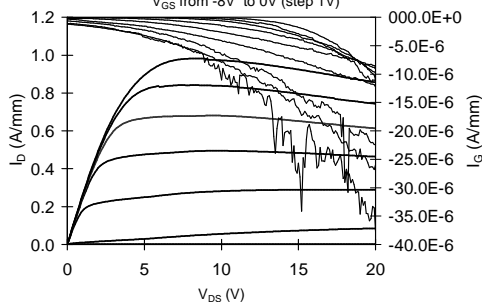
### 3-5 Labs AEC1147 [REFERENCE SiC substrate] [ $W_G = 200 \mu\text{m}$ , $L_G = 0.25 \mu\text{m}$ , $L_{GS} = 1 \mu\text{m}$ , $L_{GD} = 3 \mu\text{m}$ ]

3-5 LABS AEC 1147 C4 3 ( $W_G=200\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{GS}=1\mu\text{m}$ ,  $L_{GD}=3\mu\text{m}$ )  
Gate to Source DIODE



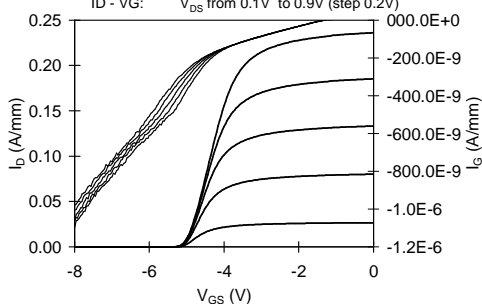
a) gate-to-source I-V characteristic

3-5 LABS AEC 1147 C4 3 ( $W_G=200\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{GS}=1\mu\text{m}$ ,  $L_{GD}=3\mu\text{m}$ )  
 $V_{GS}$  from -8V to 0V (step 1V)



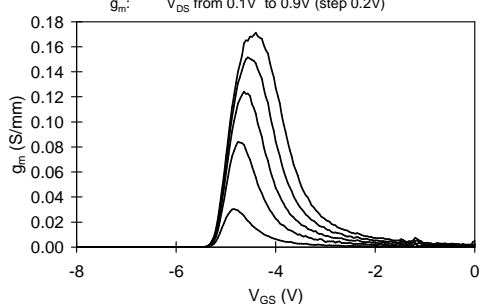
b)  $I_D$ - $V_{DS}$  and  $I_{GS}$ - $V_{DS}$  characteristic at  $V_{GS}$  from -8 V to 0 V (step 1 V)

3-5 LABS AEC 1147 C4 3 ( $W_G=200\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{GS}=1\mu\text{m}$ ,  $L_{GD}=3\mu\text{m}$ )  
ID - VG:  $V_{DS}$  from 0.1V to 0.9V (step 0.2V)



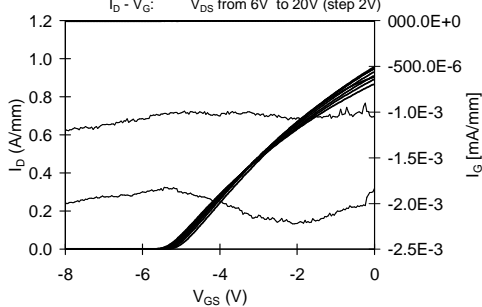
c)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 0.1 V to 0.9 V (step 0.2 V)

3-5 LABS AEC 1147 C4 3 ( $W_G=200\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{GS}=1\mu\text{m}$ ,  $L_{GD}=3\mu\text{m}$ )  
 $g_m$ :  $V_{DS}$  from 0.1V to 0.9V (step 0.2V)



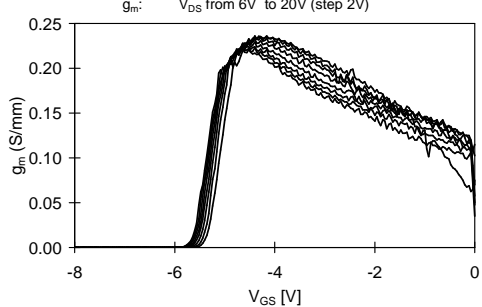
d)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 0.1 V to 0.9 V (step 0.2 V)

3-5 LABS AEC 1147 C4 3 ( $W_G=200\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{GS}=1\mu\text{m}$ ,  $L_{GD}=3\mu\text{m}$ )  
 $I_D$  -  $V_G$ :  $V_{DS}$  from 6V to 20V (step 2V)



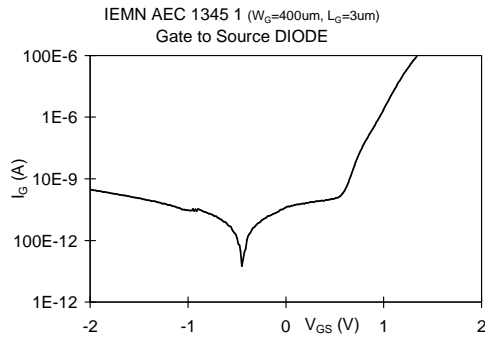
e)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 6 V to 20 V (step 2 V)

3-5 LABS AEC 1147 C4 3 ( $W_G=200\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{GS}=1\mu\text{m}$ ,  $L_{GD}=3\mu\text{m}$ )  
 $g_m$ :  $V_{DS}$  from 6V to 20V (step 2V)

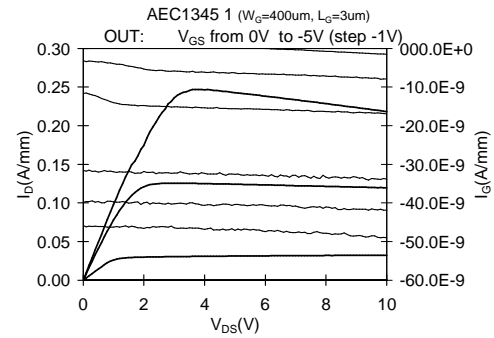
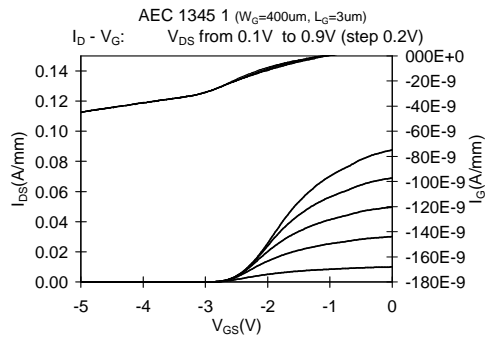
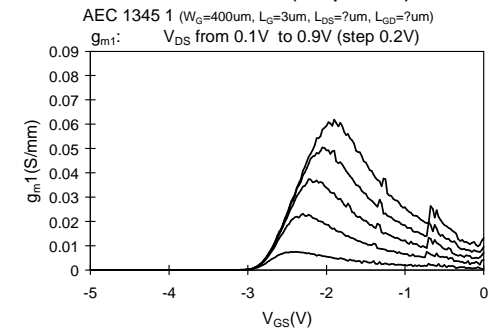
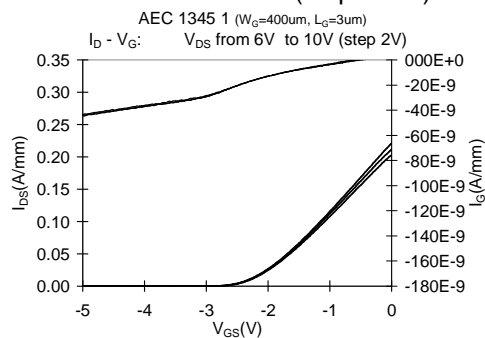
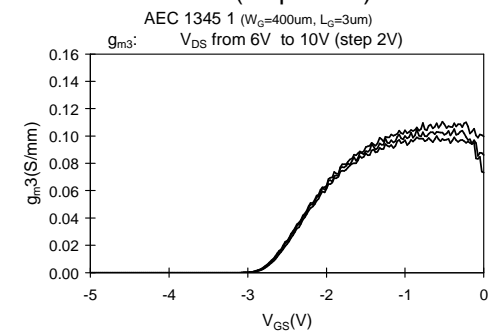


f)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 6 V to 20 V (step 2 V)

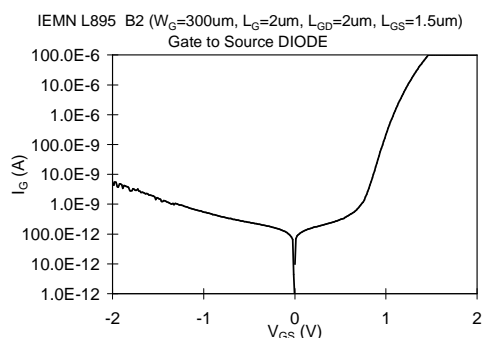
## IEMN AEC1345 [1<sup>st</sup>-batch SiCopSiC substrate] [ $W_G = 400 \mu\text{m}$ , $L_G = 3 \mu\text{m}$ ]



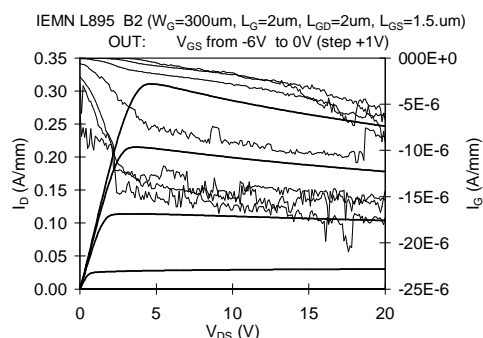
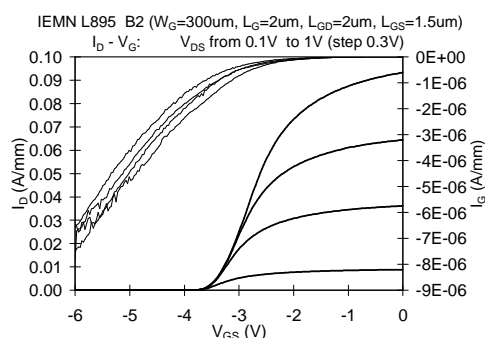
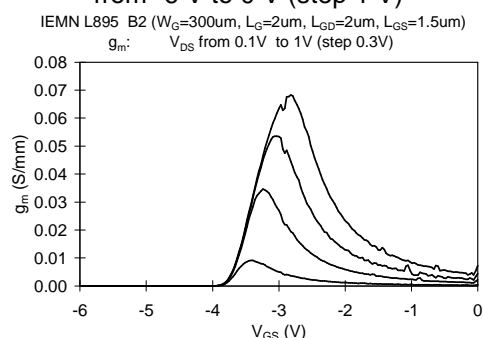
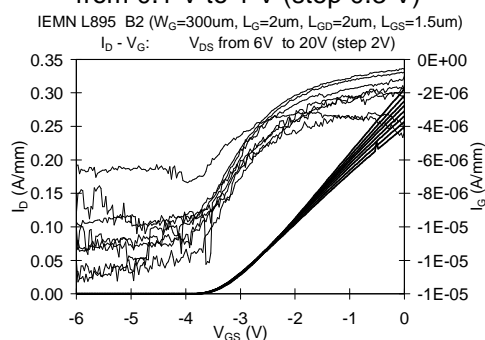
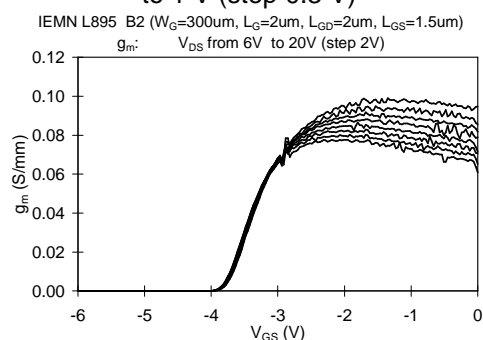
a) gate-to-source I-V characteristic

b)  $I_D$ - $V_{DS}$  and  $I_{GS}$ - $V_{DS}$  characteristic at  $V_{GS}$  from 0 V to -5 V (step -1 V)c)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 0.1 V to 0.9 V (step 0.2 V)d)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 0.1 V to 0.9 V (step 0.2 V)e)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 6 V to 10 V (step 2 V)f)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 6 V to 10 V (step 2 V)

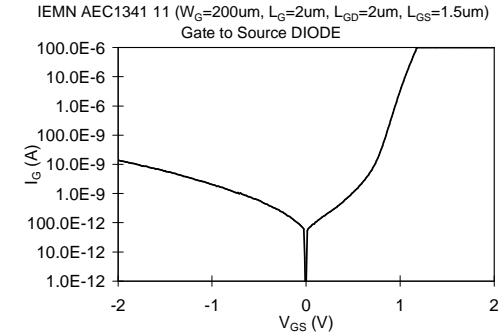
## IEMN L895 [1<sup>st</sup>-batch SiCopSiC substrate] [ $W_G = 300 \mu\text{m}$ , $L_G = 2 \mu\text{m}$ ]



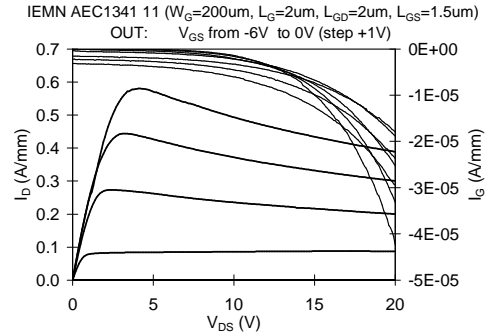
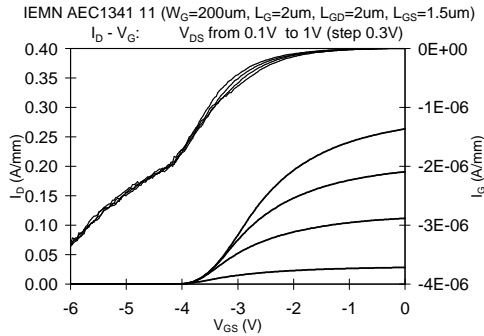
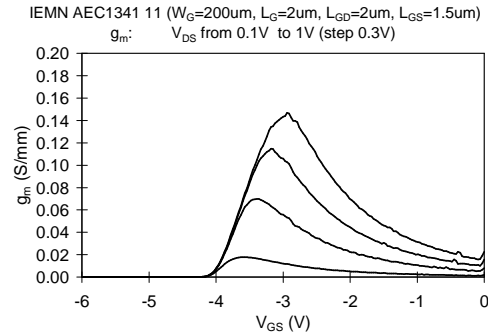
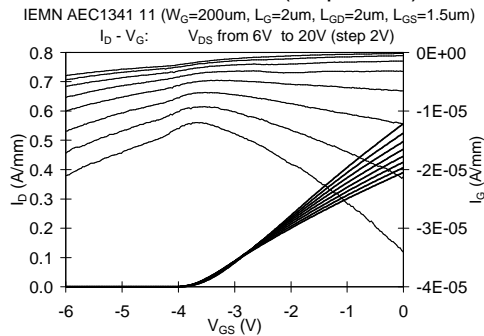
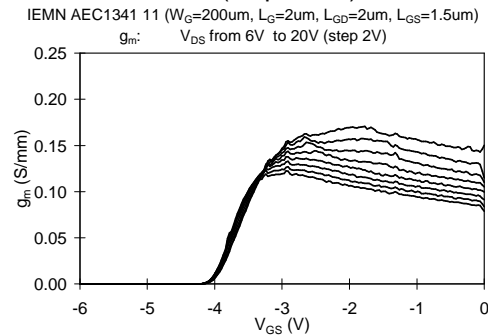
a) gate-to-source I-V characteristic

b)  $I_D$ - $V_{DS}$  and  $I_{GS}$ - $V_{DS}$  characteristic at  $V_{GS}$  from -6 V to 0 V (step 1 V)c)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)d)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)e)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 6 V to 10 V (step 2 V)f)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 6 V to 10 V (step 2 V)

## IEMN AEC1341 [1<sup>st</sup>-batch SiCopSiC substrate] [ $W_G = 200 \mu\text{m}$ , $L_G = 2 \mu\text{m}$ ]

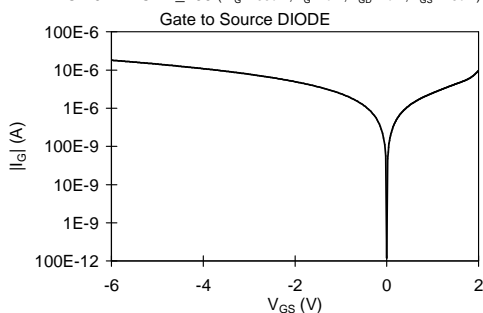


a) gate-to-source I-V characteristic

b)  $I_D$ - $V_{DS}$  and  $I_{GS}$ - $V_{DS}$  characteristic at  $V_{GS}$  from -6 V to 0 V (step 1 V)c)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)d)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)e)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 6 V to 10 V (step 2 V)f)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 6 V to 10 V (step 2 V)

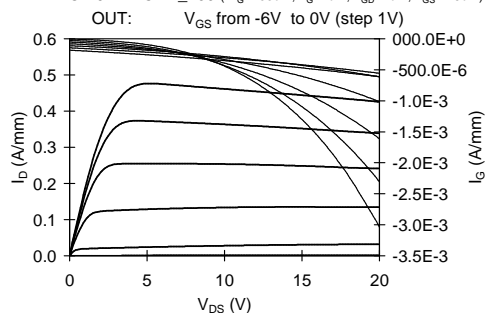
## IEMN LO-792 [1<sup>st</sup>-batch SopSiC substrate] [ $W_G = 100 \mu\text{m}$ , $L_G = 2 \mu\text{m}$ ]

IEMN LO-792 L2C1 2\_100 ( $W_G=100\mu\text{m}$ ,  $L_G=2\mu\text{m}$ ,  $L_{GD}=2\mu\text{m}$ ,  $L_{GS}=1.5\mu\text{m}$ )



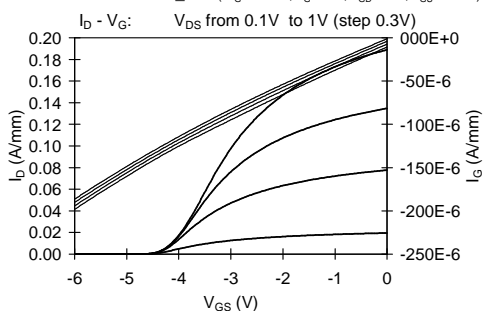
a) gate-to-source I-V characteristic

IEMN LO-792 L2C1 2\_100 ( $W_G=100\mu\text{m}$ ,  $L_G=2\mu\text{m}$ ,  $L_{GD}=2\mu\text{m}$ ,  $L_{GS}=1.5\mu\text{m}$ )



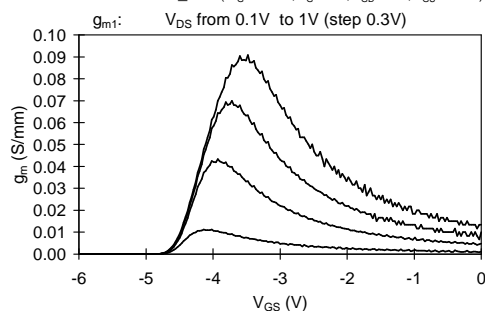
b)  $I_D$ - $V_{DS}$  and  $I_{GS}$ - $V_{DS}$  characteristic at  $V_{GS}$  from -6 V to 0 V (step 1 V)

IEMN LO-792 L2C1 2\_100 ( $W_G=100\mu\text{m}$ ,  $L_G=2\mu\text{m}$ ,  $L_{GD}=2\mu\text{m}$ ,  $L_{GS}=1.5\mu\text{m}$ )



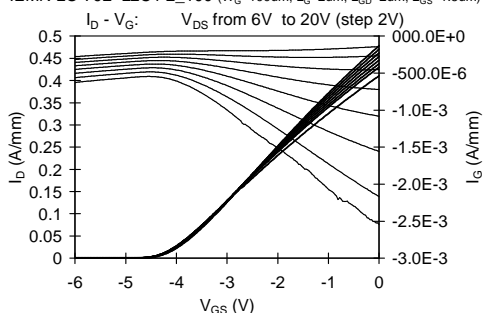
c)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)

IEMN LO-792 L2C1 2\_100 ( $W_G=100\mu\text{m}$ ,  $L_G=2\mu\text{m}$ ,  $L_{GD}=2\mu\text{m}$ ,  $L_{GS}=1.5\mu\text{m}$ )



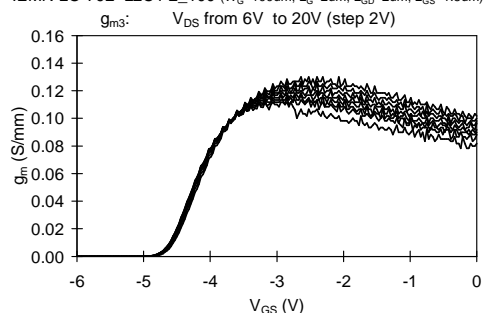
d)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)

IEMN LO-792 L2C1 2\_100 ( $W_G=100\mu\text{m}$ ,  $L_G=2\mu\text{m}$ ,  $L_{GD}=2\mu\text{m}$ ,  $L_{GS}=1.5\mu\text{m}$ )



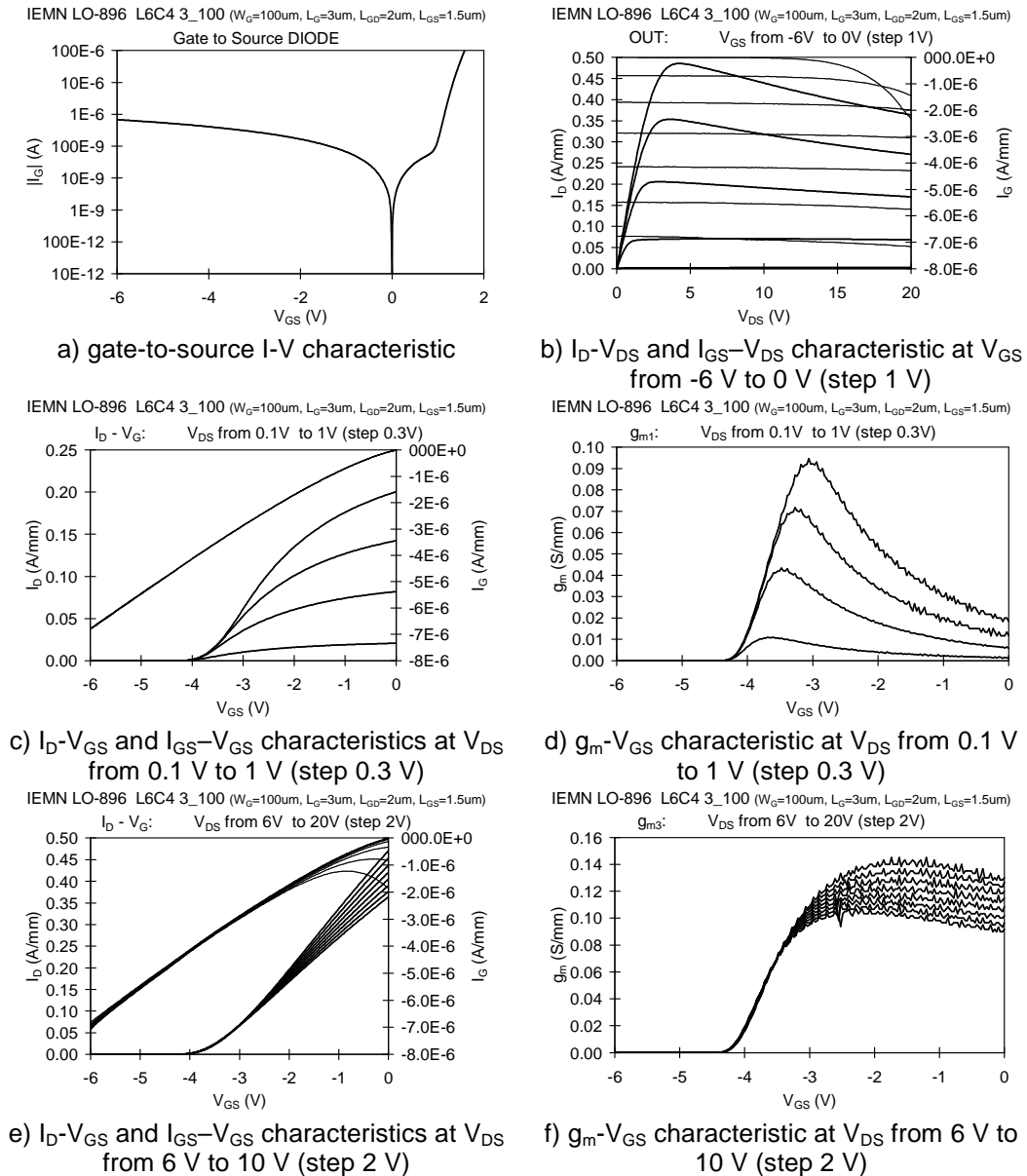
e)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 6 V to 10 V (step 2 V)

IEMN LO-792 L2C1 2\_100 ( $W_G=100\mu\text{m}$ ,  $L_G=2\mu\text{m}$ ,  $L_{GD}=2\mu\text{m}$ ,  $L_{GS}=1.5\mu\text{m}$ )

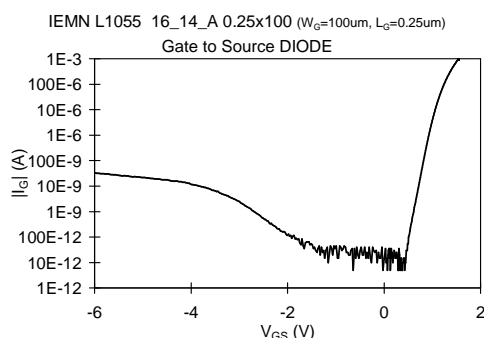


f)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 6 V to 10 V (step 2 V)

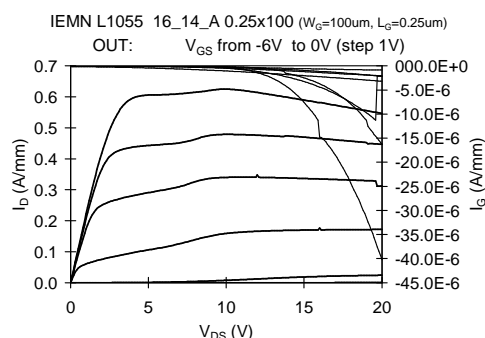
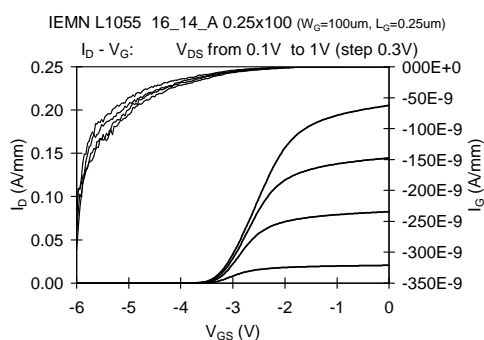
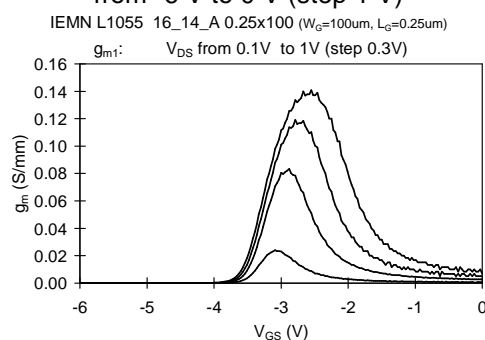
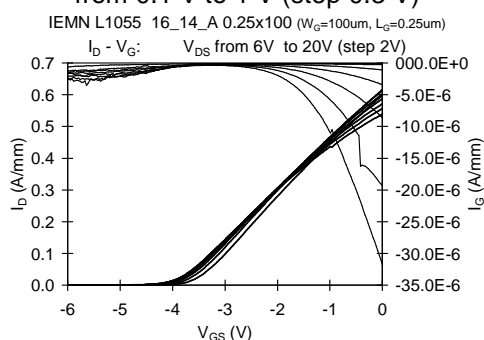
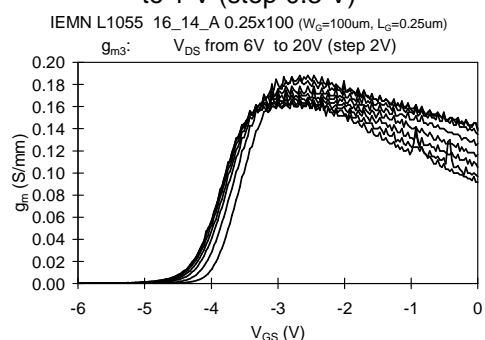
## IEMN LO-896 [1<sup>st</sup>-batch SiCopSiC substrate] [ $W_G = 100 \mu\text{m}$ , $L_G = 3 \mu\text{m}$ ]



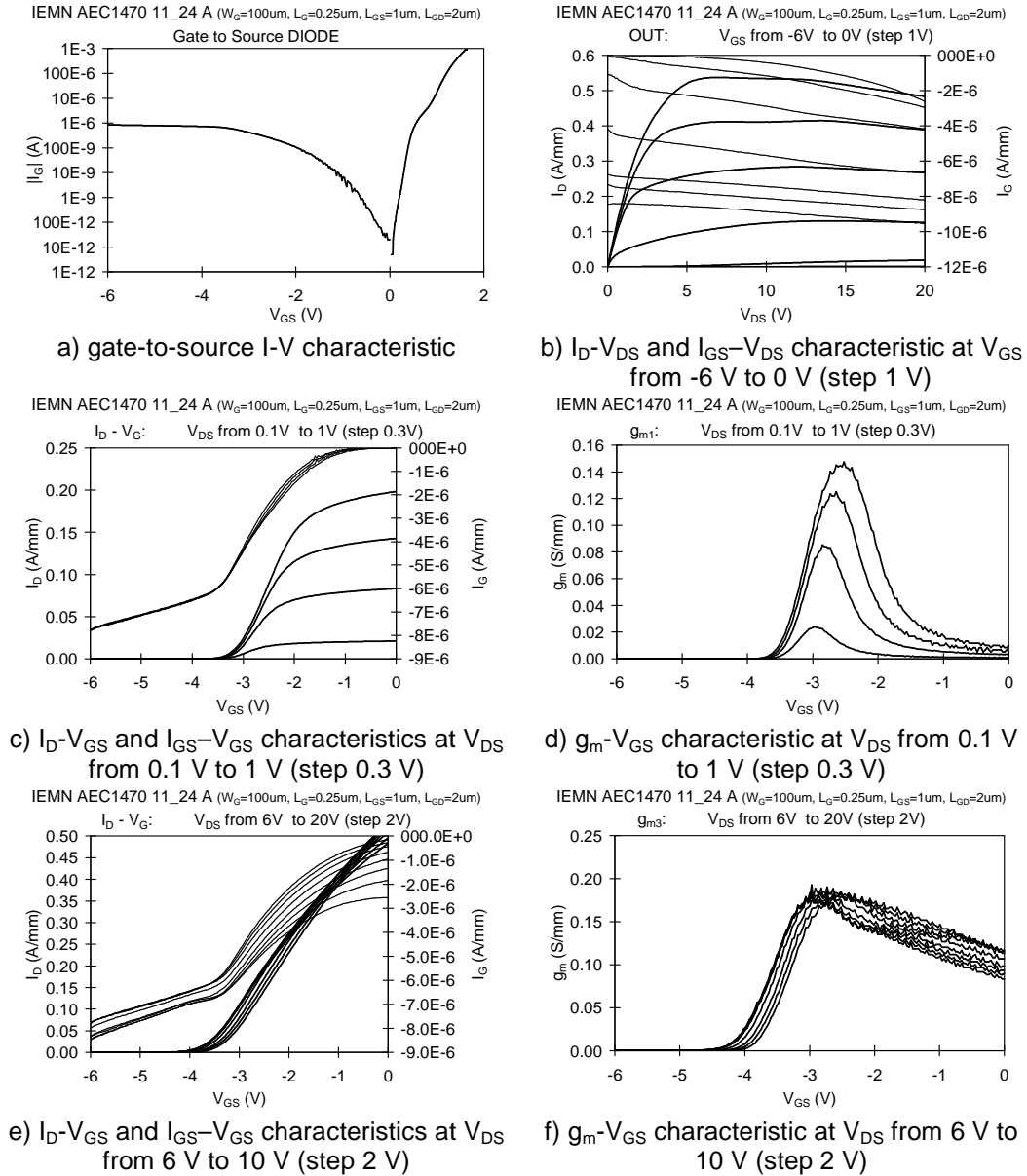
## IEMN L1055 [2<sup>nd</sup>-batch SiCopSiC substrate] [ $W_G = 100 \mu\text{m}$ , $L_G = 0.25 \mu\text{m}$ , $L_{GS} = 1 \mu\text{m}$ , $L_{GD} = 2 \mu\text{m}$ ]



a) gate-to-source I-V characteristic

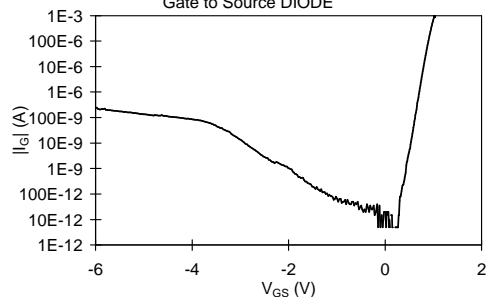
b)  $I_D$ - $V_{DS}$  and  $I_{GS}$ - $V_{DS}$  characteristic at  $V_{GS}$  from -6 V to 0 V (step 1 V)c)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)d)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)e)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 6 V to 10 V (step 2 V)f)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 6 V to 10 V (step 2 V)

## IEMN AEC1470 [2<sup>nd</sup>-batch SiCopSiC substrate] [ $W_G = 100 \mu\text{m}$ , $L_G = 0.25 \mu\text{m}$ , $L_{GS} = 1 \mu\text{m}$ , $L_{GD} = 2 \mu\text{m}$ ]



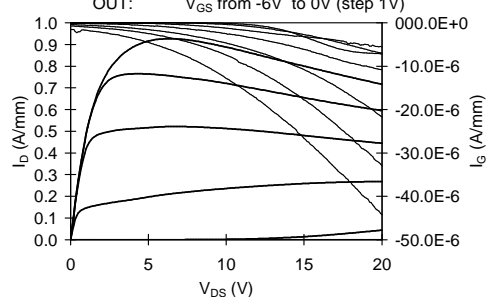
### 3-5 Labs AEC1313 [2<sup>nd</sup>-batch SiCopSiC substrate] [ $W_G = 150 \mu\text{m}$ , $L_G = 0.25 \mu\text{m}$ , $L_{GS} = 2 \mu\text{m}$ , $L_{GD} = 1 \mu\text{m}$ ]

IEMN AEC1313 23\_31\_C 0.25x150 ( $W_G=150\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{GD}=2\mu\text{m}$ ,  $L_{GD}=1\mu\text{m}$ )  
Gate to Source DIODE



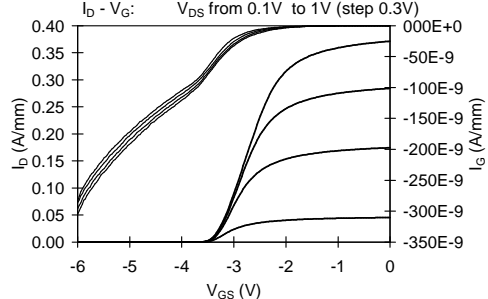
a) gate-to-source I-V characteristic

IEMN AEC1313 23\_31\_C 0.25x150 ( $W_G=150\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{GD}=2\mu\text{m}$ ,  $L_{GD}=1\mu\text{m}$ )  
OUT:  $V_{GS}$  from -6V to 0V (step 1V)



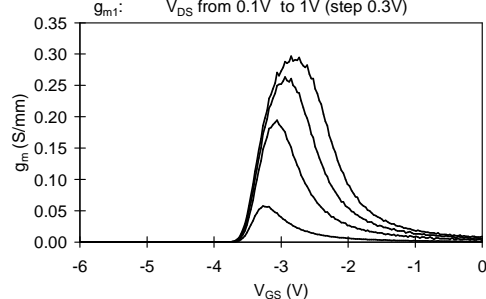
b)  $I_D$ - $V_{DS}$  and  $I_{GS}$ - $V_{DS}$  characteristic at  $V_{GS}$  from -6 V to 0 V (step 1 V)

IEMN AEC1313 23\_31\_C 0.25x150 ( $W_G=150\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{GD}=2\mu\text{m}$ ,  $L_{GD}=1\mu\text{m}$ )  
 $I_D - V_{GS}$ :  $V_{DS}$  from 0.1V to 1V (step 0.3V)



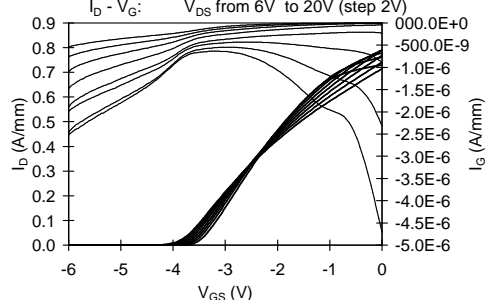
c)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)

IEMN AEC1313 23\_31\_C 0.25x150 ( $W_G=150\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{GD}=2\mu\text{m}$ ,  $L_{GD}=1\mu\text{m}$ )  
 $g_m$ :  $V_{DS}$  from 0.1V to 1V (step 0.3V)



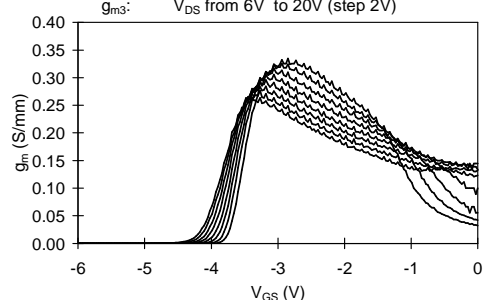
d)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)

IEMN AEC1313 23\_31\_C 0.25x150 ( $W_G=150\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{GD}=2\mu\text{m}$ ,  $L_{GD}=1\mu\text{m}$ )  
 $I_D - V_{GS}$ :  $V_{DS}$  from 6V to 20V (step 2V)



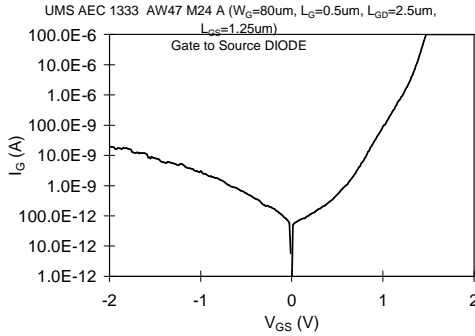
e)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 6 V to 10 V (step 2 V)

IEMN AEC1313 23\_31\_C 0.25x150 ( $W_G=150\mu\text{m}$ ,  $L_G=0.25\mu\text{m}$ ,  $L_{GD}=2\mu\text{m}$ ,  $L_{GD}=1\mu\text{m}$ )  
 $g_m$ :  $V_{DS}$  from 6V to 20V (step 2V)

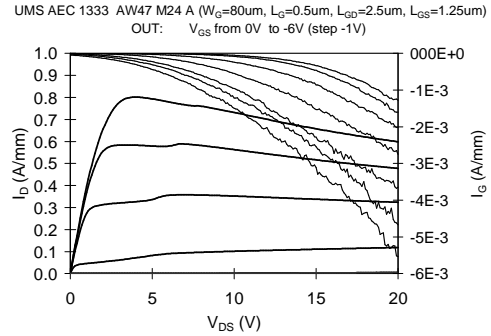
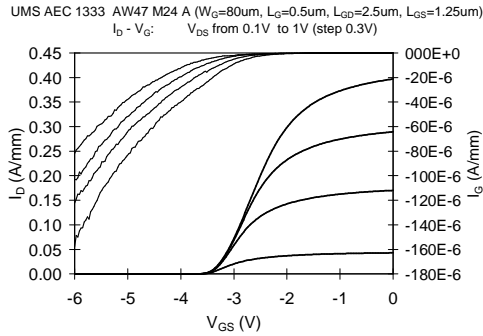
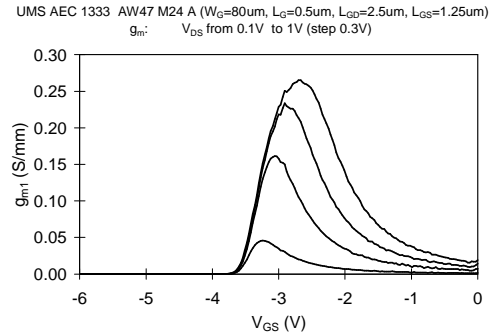
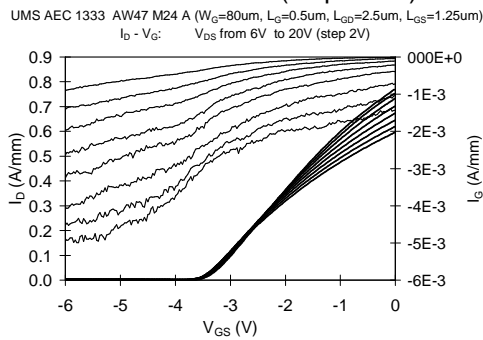
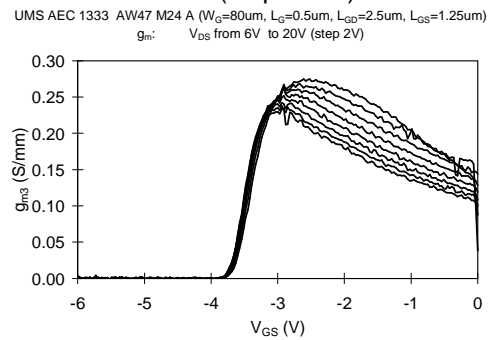


f)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 6 V to 10 V (step 2 V)

**UMS AEC1333 [1<sup>st</sup>-batch SiCopSiC substrate]**  
**[ $W_G = 80 \mu\text{m}$ ,  $L_G = 0.5 \mu\text{m}$ ,  $L_{GS} = 1.25 \mu\text{m}$ ,  $L_{GD} = 2.5 \mu\text{m}$ ]**

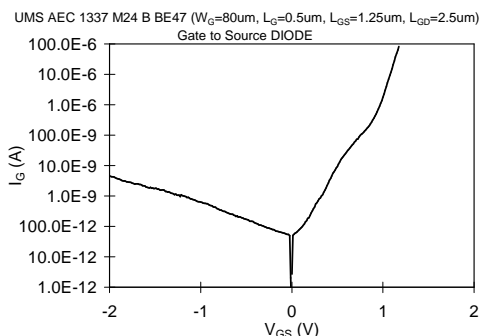


a) gate-to-source I-V characteristic

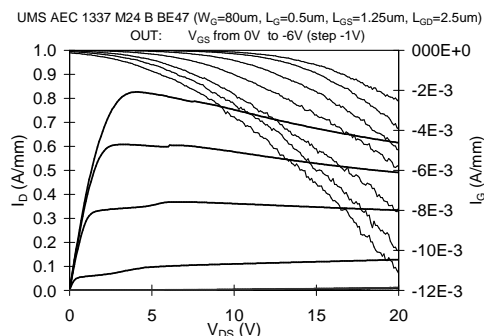
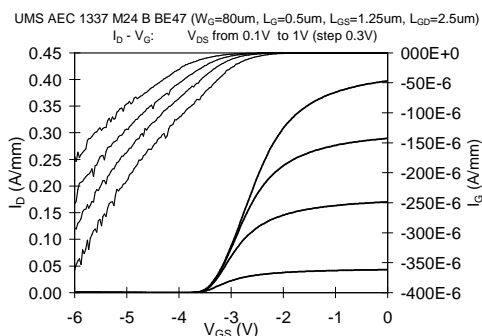
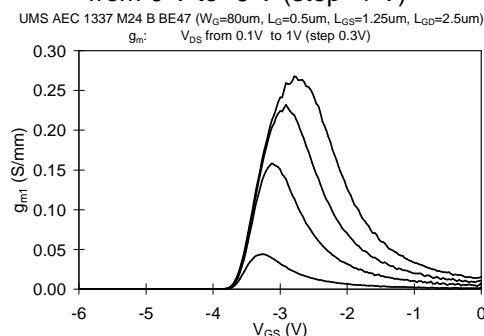
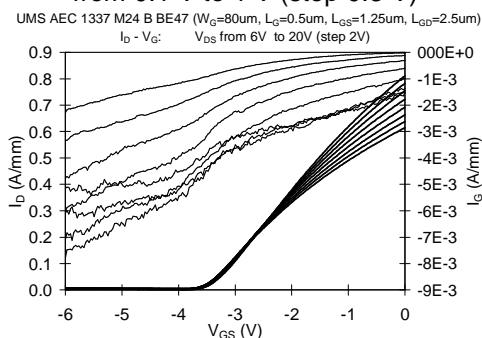
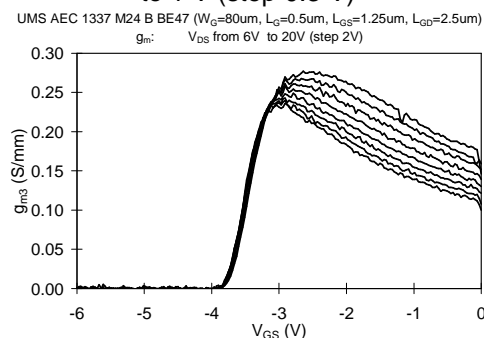
b)  $I_D$ - $V_{DS}$  and  $I_{GS}$ - $V_{DS}$  characteristic at  $V_{GS}$  from 0 V to -6 V (step -1 V)c)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)d)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)e)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 6 V to 10 V (step 2 V)f)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 6 V to 10 V (step 2 V)

## UMS AEC1337 [1<sup>st</sup>-batch SiCopSiC substrate]

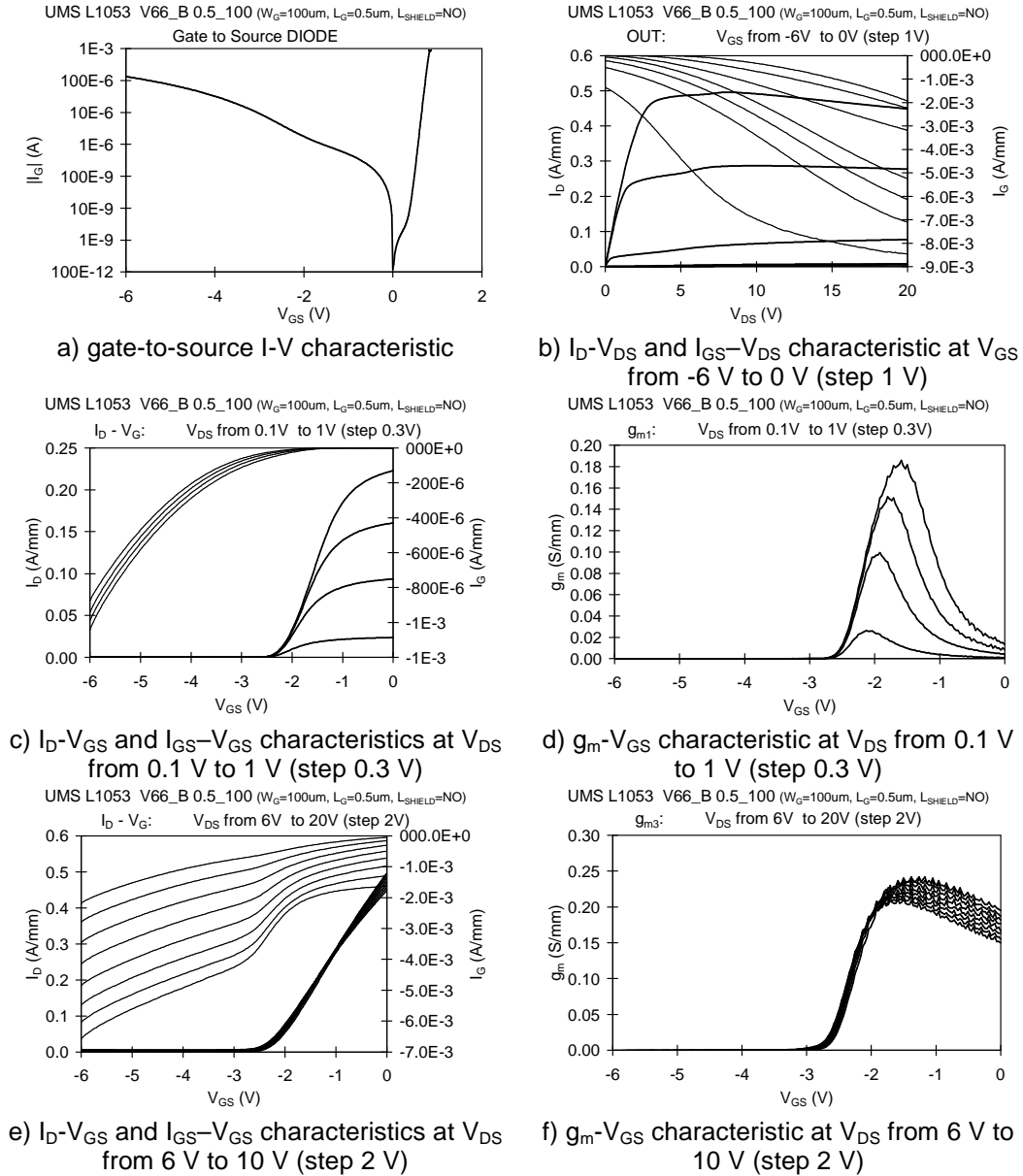
### [ $W_G = 80 \mu\text{m}$ , $L_G = 0.5 \mu\text{m}$ , $L_{GS} = 1.25 \mu\text{m}$ , $L_{GD} = 2.5 \mu\text{m}$ ]



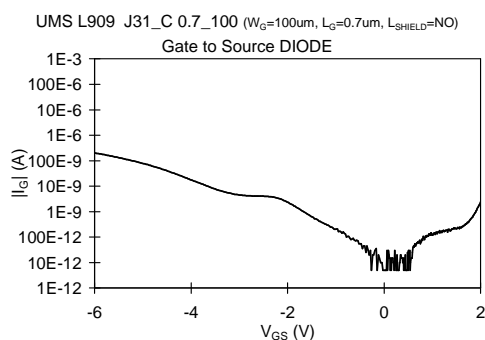
a) gate-to-source I-V characteristic

b)  $I_D$ - $V_{DS}$  and  $I_{GS}$ - $V_{DS}$  characteristic at  $V_{GS}$  from 0 V to -6 V (step -1 V)c)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)d)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)e)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 6 V to 10 V (step 2 V)f)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 6 V to 10 V (step 2 V)

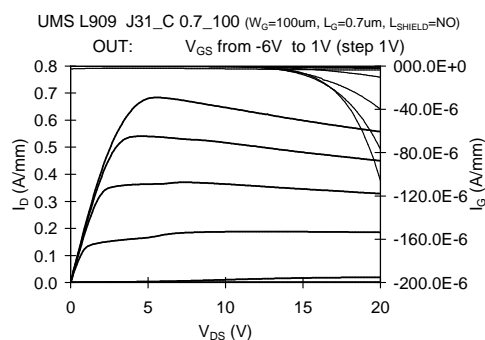
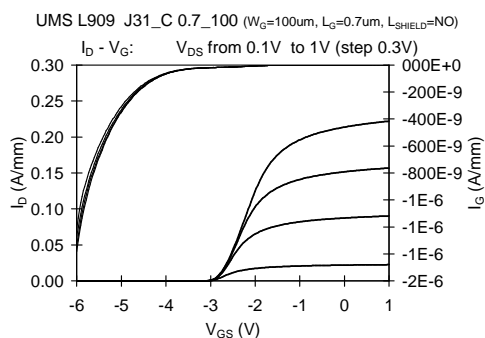
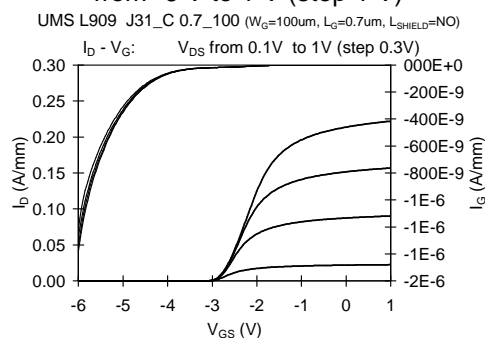
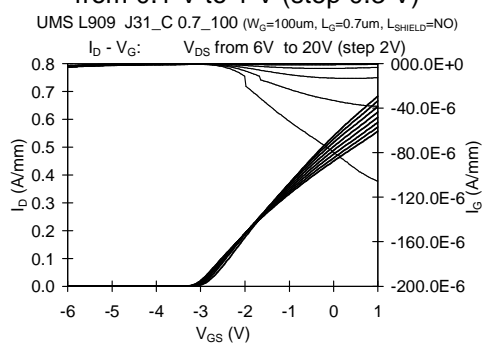
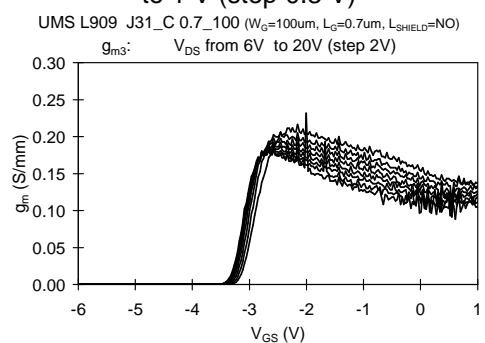
## UMS L1053 [2<sup>nd</sup>-batch Si substrate] [ $W_G = 100 \mu\text{m}$ , $L_G = 0.5 \mu\text{m}$ ]



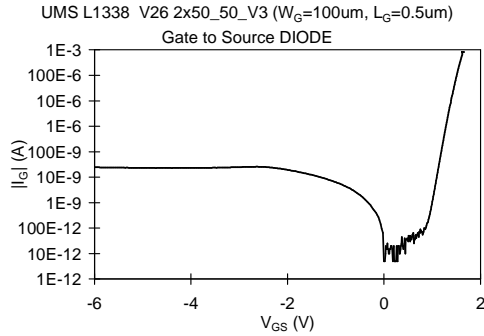
## UMS L909 [2<sup>nd</sup>-batch Si substrate] [ $W_G = 100 \mu\text{m}$ , $L_G = 0.7 \mu\text{m}$ ]



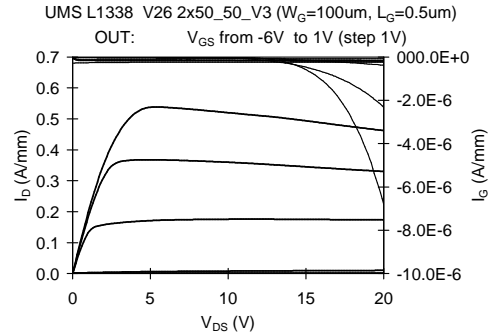
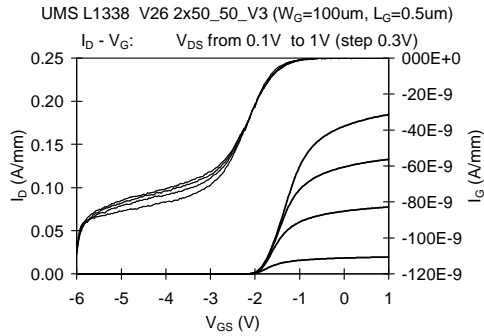
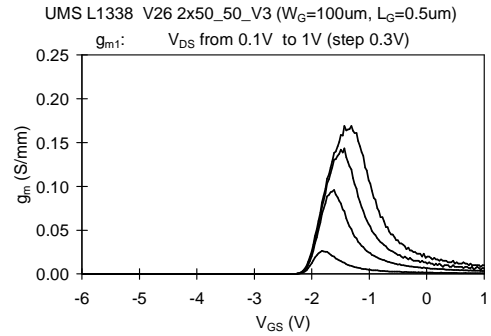
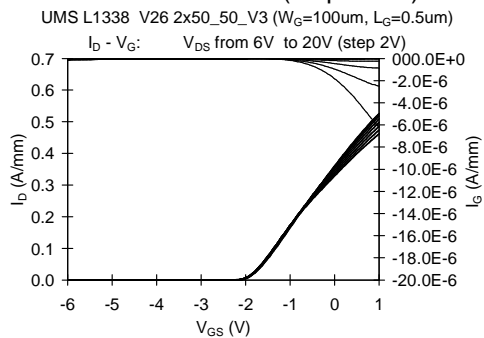
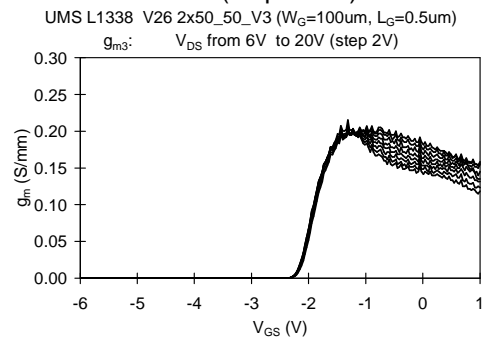
a) gate-to-source I-V characteristic

b)  $I_D$ - $V_{DS}$  and  $I_{GS}$ - $V_{DS}$  characteristic at  $V_{GS}$  from -6 V to 1 V (step 1 V)c)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)d)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)e)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 6 V to 10 V (step 2 V)f)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 6 V to 10 V (step 2 V)

## UMS L1338 [2<sup>nd</sup>-batch Si substrate] [ $W_G = 100 \mu\text{m}$ , $L_G = 0.5 \mu\text{m}$ ]

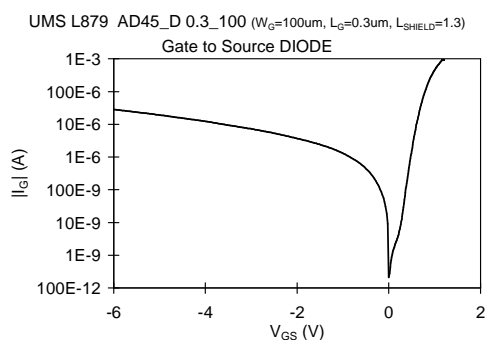


a) gate-to-source I-V characteristic

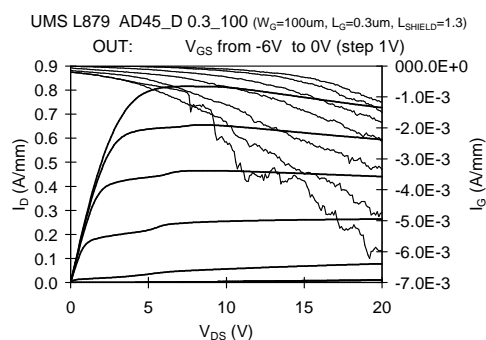
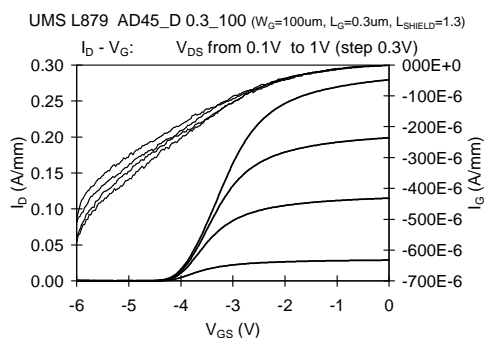
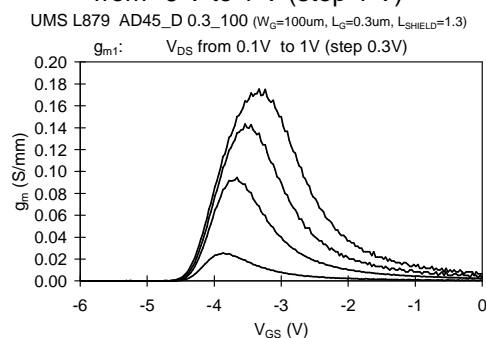
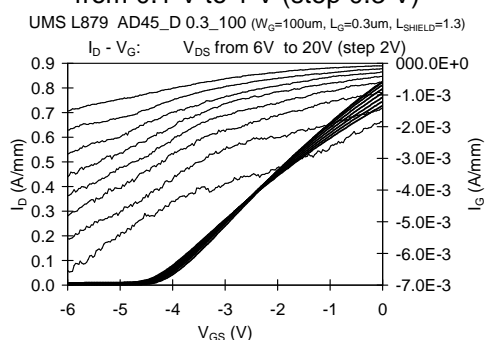
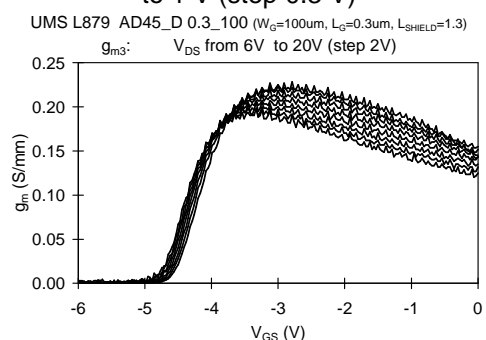
b)  $I_D$ - $V_{DS}$  and  $I_{GS}$ - $V_{DS}$  characteristic at  $V_{GS}$  from -6 V to 1 V (step 1 V)c)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)d)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)e)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 6 V to 20 V (step 2 V)f)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 6 V to 20 V (step 2 V)

## UMS L879 [2<sup>nd</sup>-batch SopSiC substrate]

### [ $W_G = 100 \mu\text{m}$ , $L_G = 0.3 \mu\text{m}$ , $L_{SH} = 1.3 \mu\text{m}$ ]



a) gate-to-source I-V characteristic

b)  $I_D$ - $V_{DS}$  and  $I_{GS}$ - $V_{DS}$  characteristic at  $V_{GS}$  from -6 V to 1 V (step 1 V)c)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)d)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 0.1 V to 1 V (step 0.3 V)e)  $I_D$ - $V_{GS}$  and  $I_{GS}$ - $V_{GS}$  characteristics at  $V_{DS}$  from 6 V to 20 V (step 2 V)f)  $g_m$ - $V_{GS}$  characteristic at  $V_{DS}$  from 6 V to 20 V (step 2 V)



## **APPENDIX II: SELECTED DYNAMIC MEASUREMENTS FOR HYPHEN DEVICES**

In this appendix the DIVA-like characterizations of HYPHEN wafers are reported as reference. The diagrams about a representative device for each device are presented, in particular:

Reference:

- AEC1142
- AEC1147

IEMN:

- AEC1345
- L895
- AEC1341
- LO-792
- LO-896
- LO-1055
- AEC1470

3-5 Labs:

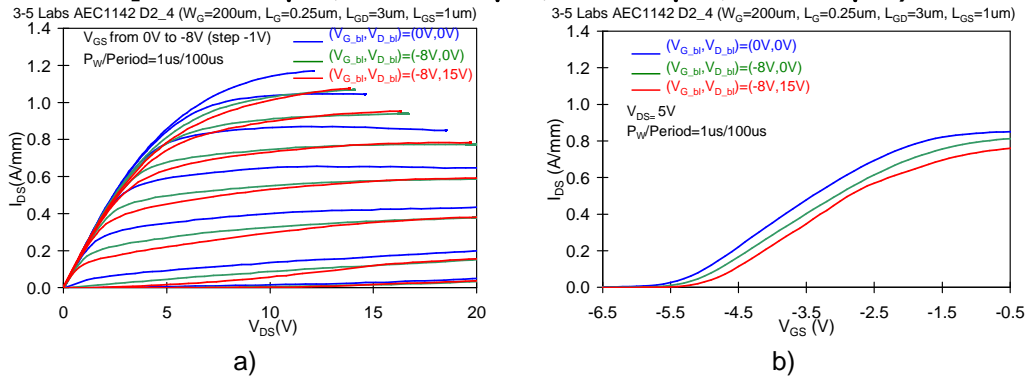
- AEC1313

UMS:

- AEC1333
- AEC1337
- L1053
- L909
- L1338
- L879

### 3-5 Labs AEC1142 [REFERENCE SiC substrate]

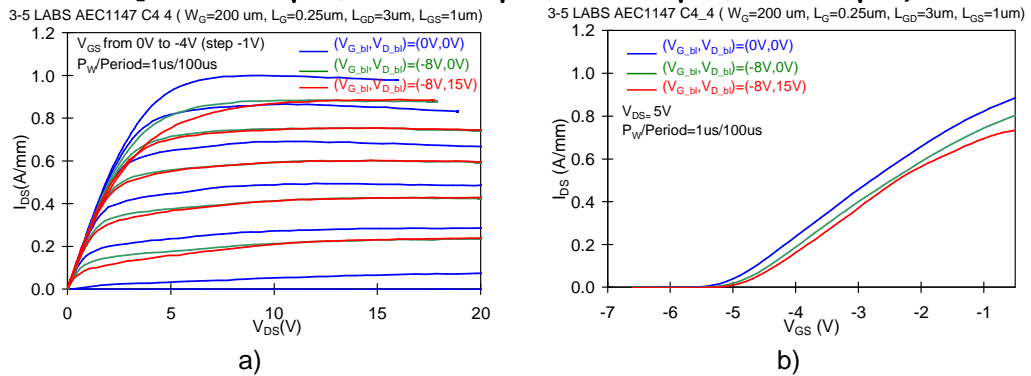
$[W_G = 200 \mu\text{m}, L_G = 0.25 \mu\text{m}, L_{GS} = 1 \mu\text{m}, L_{GD} = 3 \mu\text{m}]$



DIVA-like (a)  $I_D$ - $V_D$  characteristics at  $V_{GS}$  from 0 V to -8 V and (b)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 5$  V. Baseline:  $(V_{GS\_bl}, V_{DS\_bl})=(0 \text{ V}, 0 \text{ V})$ ,  $(-8 \text{ V}, 0 \text{ V})$  and  $(-8 \text{ V}, 15 \text{ V})$ .

### 3-5 Labs AEC1147 [REFERENCE SiC substrate]

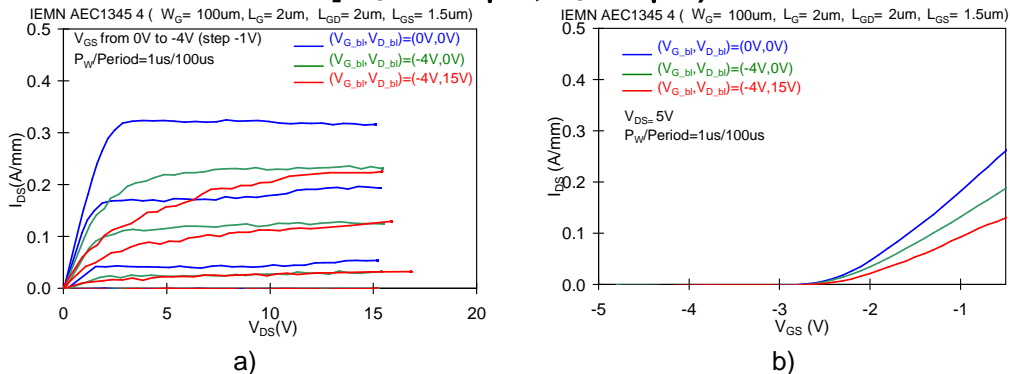
$[W_G = 200 \mu\text{m}, L_G = 0.25 \mu\text{m}, L_{GS} = 1 \mu\text{m}, L_{GD} = 3 \mu\text{m}]$



DIVA-like (a)  $I_D$ - $V_D$  characteristics at  $V_{GS}$  from 0 V to -8 V and (b)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 5$  V. Baseline:  $(V_{GS\_bl}, V_{DS\_bl})=(0 \text{ V}, 0 \text{ V})$ ,  $(-8 \text{ V}, 0 \text{ V})$  and  $(-8 \text{ V}, 15 \text{ V})$ .

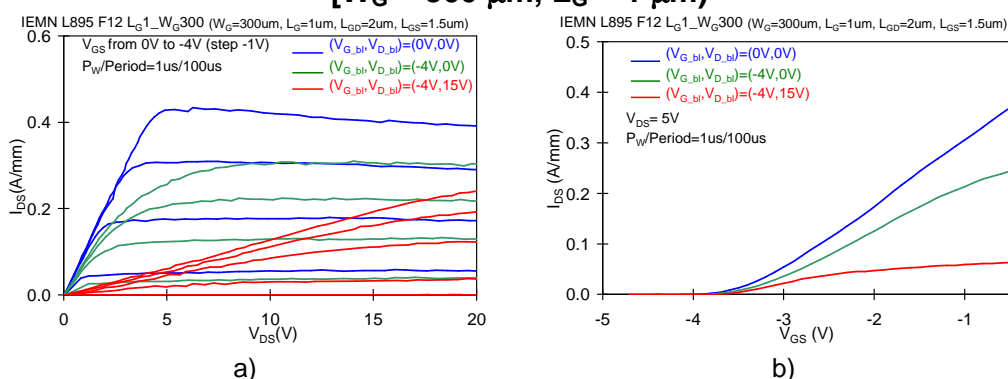
### IEMN AEC1345 [1<sup>st</sup>-batch SiCopSiC substrate]

$[W_G = 100 \mu\text{m}, L_G = 2 \mu\text{m}]$



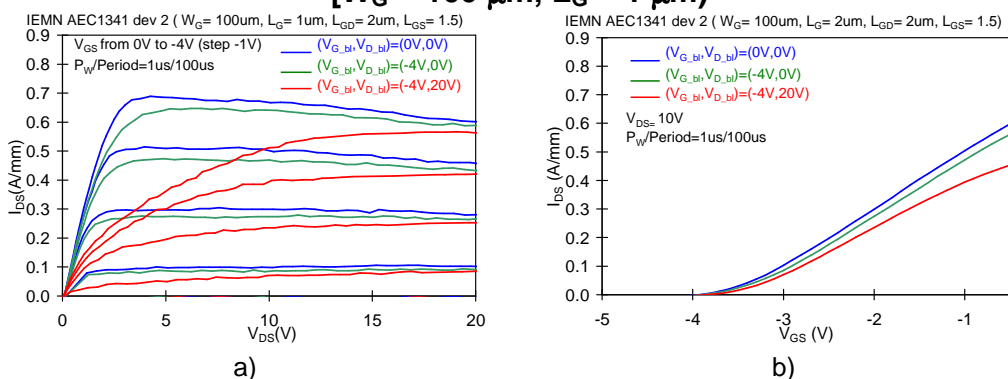
DIVA-like (a)  $I_D$ - $V_D$  characteristics at  $V_{GS}$  from 0 V to -8 V and (b)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 5$  V. Baseline:  $(V_{GS\_bl}, V_{DS\_bl})=(0 \text{ V}, 0 \text{ V})$ ,  $(-4 \text{ V}, 0 \text{ V})$  and  $(-4 \text{ V}, 15 \text{ V})$ .

## IEMN L895 [1<sup>st</sup>-batch SiCopSiC substrate] [ $W_G = 300 \mu\text{m}$ , $L_G = 1 \mu\text{m}$ ]



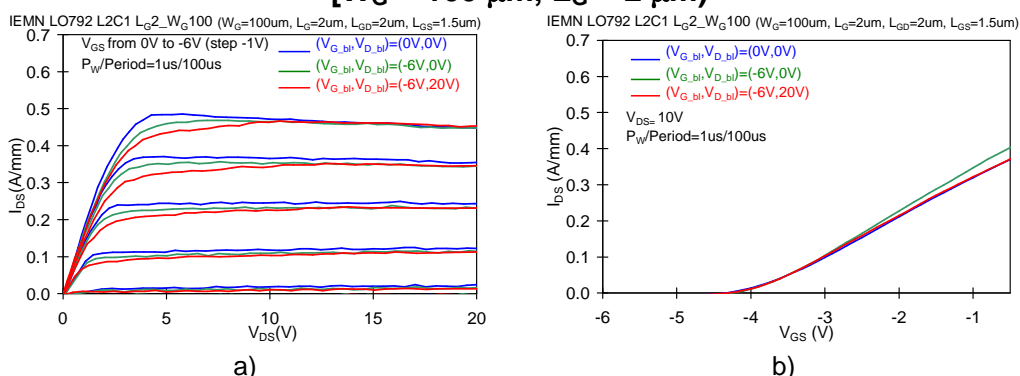
DIVA-like (a)  $I_D$ - $V_D$  characteristics at  $V_{GS}$  from 0 V to -8 V and (b)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 5$  V. Baseline:  $(V_{GS\_bl}, V_{DS\_bl})=(0$  V, 0 V), (-4 V, 0 V) and (-4 V, 15 V).

## IEMN AEC1341 [1<sup>st</sup>-batch SiCopSiC substrate] [ $W_G = 100 \mu\text{m}$ , $L_G = 1 \mu\text{m}$ ]



DIVA-like (a)  $I_D$ - $V_D$  characteristics at  $V_{GS}$  from 0 V to -8 V and (b)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 5$  V. Baseline:  $(V_{GS\_bl}, V_{DS\_bl})=(0$  V, 0 V), (-4 V, 0 V) and (-4 V, 20 V).

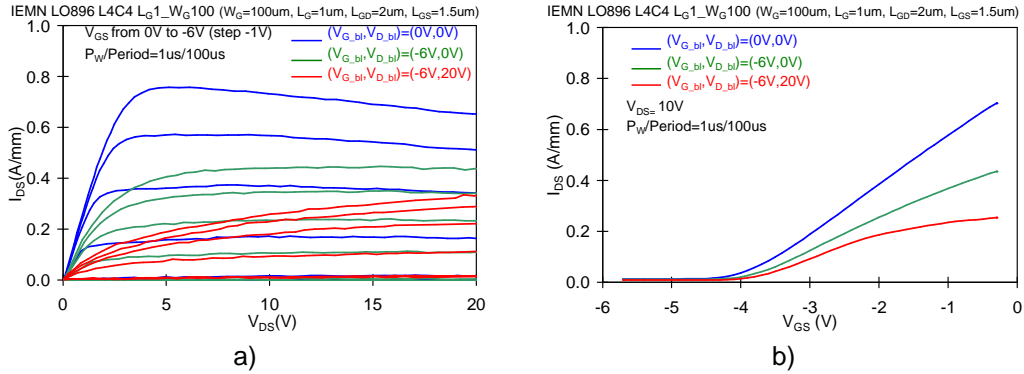
## IEMN LO-792 [1<sup>st</sup>-batch SopSiC substrate] [ $W_G = 100 \mu\text{m}$ , $L_G = 2 \mu\text{m}$ ]



DIVA-like (a)  $I_D$ - $V_D$  characteristics at  $V_{GS}$  from 0 V to -8 V and (b)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 5$  V. Baseline:  $(V_{GS\_bl}, V_{DS\_bl})=(0$  V, 0 V), (-6 V, 0 V) and (-6 V, 20 V).

## IEMN LO-896 [1<sup>st</sup>-batch SiCopSiC substrate]

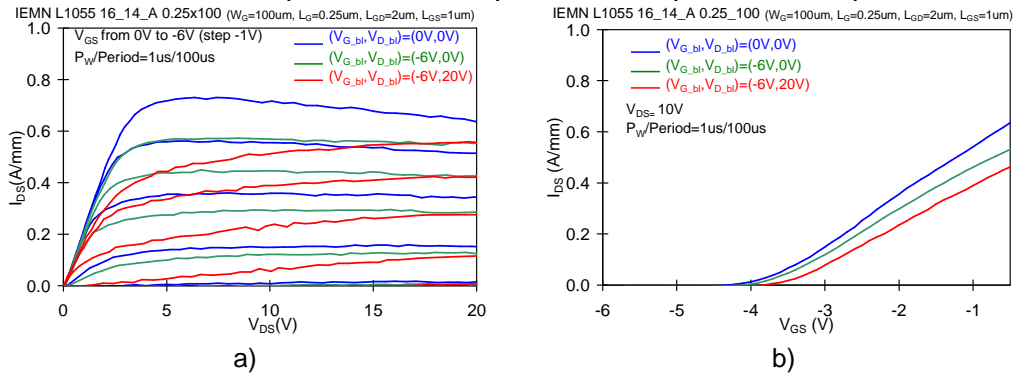
[ $W_G = 100 \mu\text{m}$ ,  $L_G = 1 \mu\text{m}$ ]



DIVA-like (a)  $I_D$ - $V_D$  characteristics at  $V_{GS}$  from 0 V to -8 V and (b)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 5$  V. Baseline: ( $V_{GS\_bl}$ ,  $V_{DS\_bl}$ )=(0 V, 0 V), (-6 V, 0 V) and (-6 V, 20 V).

## IEMN L1055 [2<sup>nd</sup>-batch SiCopSiC substrate]

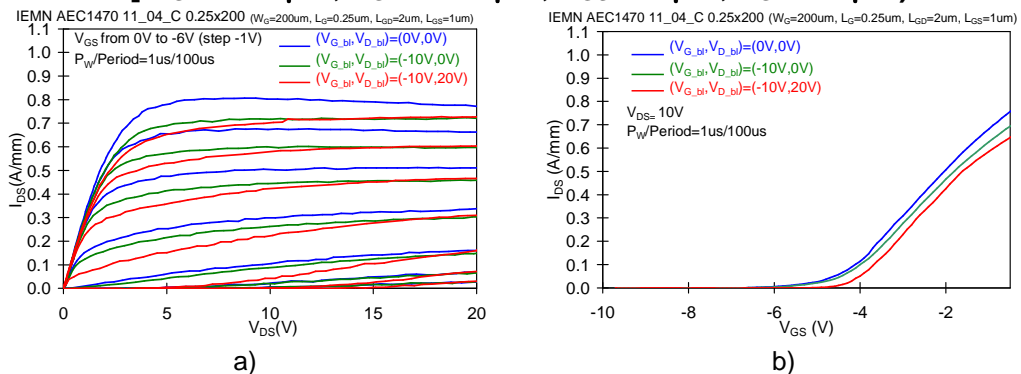
[ $W_G = 100 \mu\text{m}$ ,  $L_G = 0.25 \mu\text{m}$ ,  $L_{GS} = 1 \mu\text{m}$ ,  $L_{GD} = 2 \mu\text{m}$ ]



DIVA-like (a)  $I_D$ - $V_D$  characteristics at  $V_{GS}$  from 0 V to -8 V and (b)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 5$  V. Baseline: ( $V_{GS\_bl}$ ,  $V_{DS\_bl}$ )=(0 V, 0 V), (-6 V, 0 V) and (-6 V, 20 V).

## IEMN AEC1470 [2<sup>nd</sup>-batch SiCopSiC substrate]

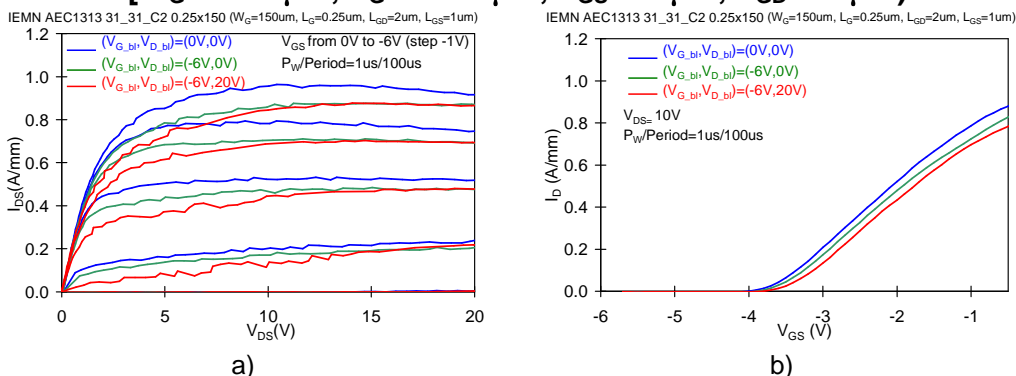
[ $W_G = 100 \mu\text{m}$ ,  $L_G = 0.25 \mu\text{m}$ ,  $L_{GS} = 1 \mu\text{m}$ ,  $L_{GD} = 2 \mu\text{m}$ ]



DIVA-like (a)  $I_D$ - $V_D$  characteristics at  $V_{GS}$  from 0 V to -8 V and (b)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 5$  V. Baseline: ( $V_{GS\_bl}$ ,  $V_{DS\_bl}$ )=(0 V, 0 V), (-10 V, 0 V) and (-10 V, 20 V).

### 3-5 Labs AEC1313 [2<sup>nd</sup>-batch SiCopSiC substrate]

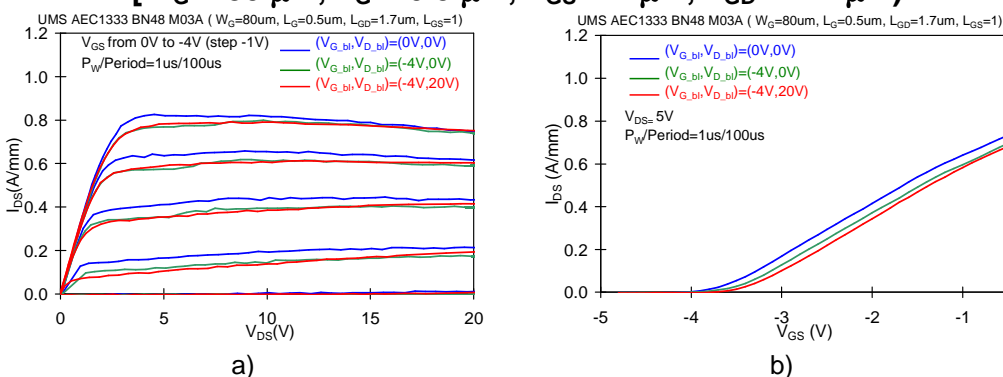
[ $W_G = 150 \mu\text{m}$ ,  $L_G = 0.25 \mu\text{m}$ ,  $L_{GS} = 2 \mu\text{m}$ ,  $L_{GD} = 1 \mu\text{m}$ ]



DIVA-like (a) I<sub>D</sub>-V<sub>D</sub> characteristics at V<sub>GS</sub> from 0 V to -8 V and (b) I<sub>D</sub>-V<sub>GS</sub> characteristics at V<sub>DS</sub> = 5 V. Baseline: (V<sub>GS,bl</sub>, V<sub>DS,bl</sub>) = (0 V, 0 V), (-6 V, 0 V) and (-6 V, 20 V).

### UMS AEC1333 [1<sup>st</sup>-batch SiCopSiC substrate]

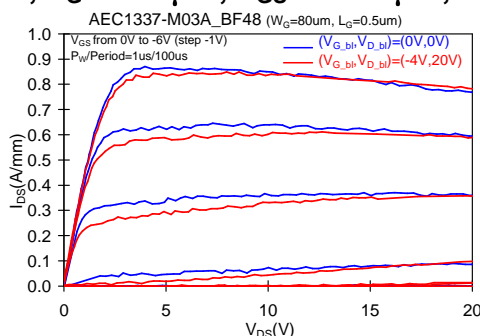
[ $W_G = 80 \mu\text{m}$ ,  $L_G = 0.5 \mu\text{m}$ ,  $L_{GS} = 1 \mu\text{m}$ ,  $L_{GD} = 1.7 \mu\text{m}$ ]



DIVA-like (a) I<sub>D</sub>-V<sub>D</sub> characteristics at V<sub>GS</sub> from 0 V to -8 V and (b) I<sub>D</sub>-V<sub>GS</sub> characteristics at V<sub>DS</sub> = 5 V. Baseline: (V<sub>GS,bl</sub>, V<sub>DS,bl</sub>) = (0 V, 0 V), (-4 V, 0 V) and (-4 V, 20 V).

### UMS AEC1337 [1<sup>st</sup>-batch SiCopSiC substrate]

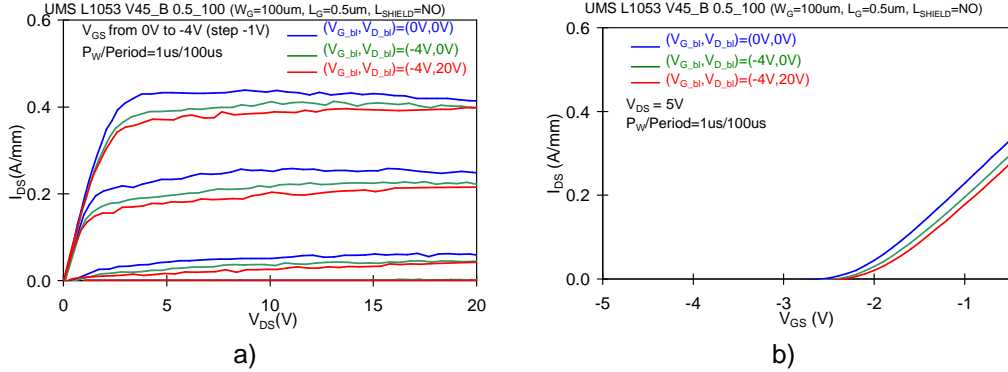
[ $W_G = 80 \mu\text{m}$ ,  $L_G = 0.5 \mu\text{m}$ ,  $L_{GS} = 1.25 \mu\text{m}$ ,  $L_{GD} = 2.5 \mu\text{m}$ ]



DIVA-like I<sub>D</sub>-V<sub>D</sub> characteristics at V<sub>GS</sub> from 0 V to -8 V. Baseline: (V<sub>GS,bl</sub>, V<sub>DS,bl</sub>) = (0 V, 0 V), (-6 V, 0 V) and (-6 V, 20 V).

## UMS L1053 [2<sup>nd</sup>-batch Si substrate]

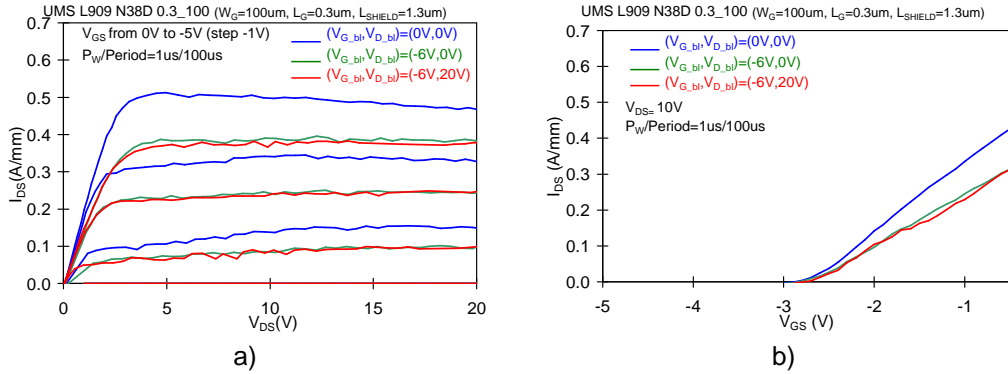
[ $W_G = 100 \mu\text{m}$ ,  $L_G = 0.5 \mu\text{m}$ ]



DIVA-like (a)  $I_D$ - $V_D$  characteristics at  $V_{GS}$  from 0 V to -8 V and (b)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 5$  V. Baseline: ( $V_{GS_{bl}}, V_{DS_{bl}}$ )=(0 V, 0 V), (-4 V, 0 V) and (-4 V, 20 V).

## UMS L909 [2<sup>nd</sup>-batch Si substrate]

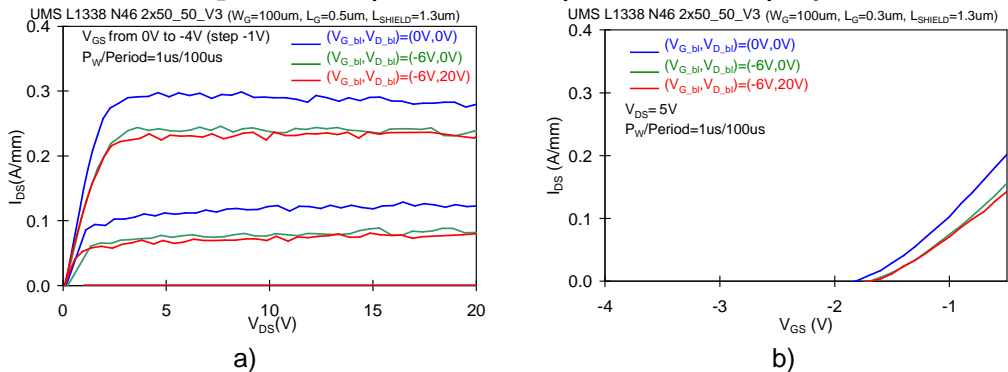
[ $W_G = 100 \mu\text{m}$ ,  $L_G = 0.3 \mu\text{m}$ ,  $L_{SH} = 1.3 \mu\text{m}$ ]



DIVA-like (a)  $I_D$ - $V_D$  characteristics at  $V_{GS}$  from 0 V to -8 V and (b)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 5$  V. Baseline: ( $V_{GS_{bl}}, V_{DS_{bl}}$ )=(0 V, 0 V), (-6 V, 0 V) and (-6 V, 20 V).

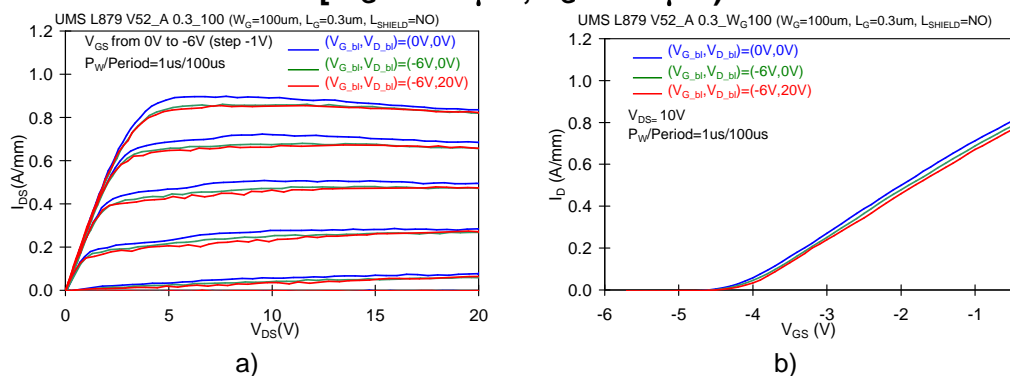
## UMS L1338 [2<sup>nd</sup>-batch Si substrate]

[ $W_G = 100 \mu\text{m}$ ,  $L_G = 0.5 \mu\text{m}$ ,  $L_{SH} = 1.3 \mu\text{m}$ ]



DIVA-like (a)  $I_D$ - $V_D$  characteristics at  $V_{GS}$  from 0 V to -8 V and (b)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 5$  V. Baseline: ( $V_{GS_{bl}}, V_{DS_{bl}}$ )=(0 V, 0 V), (-6 V, 0 V) and (-6 V, 20 V).

## UMS L879 [2<sup>nd</sup>-batch SopSiC substrate] [ $W_G = 100 \mu\text{m}$ , $L_G = 0.3 \mu\text{m}$ ]



DIVA-like (a)  $I_D$ - $V_D$  characteristics at  $V_{GS}$  from 0 V to -8 V and (b)  $I_D$ - $V_{GS}$  characteristics at  $V_{DS} = 5$  V. Baseline:  $(V_{GS\_bl}, V_{DS\_bl})=(0 \text{ V}, 0 \text{ V})$ ,  $(-6 \text{ V}, 0 \text{ V})$  and  $(-6 \text{ V}, 20 \text{ V})$ .