UNIVERSITÀ DEGLI STUDI DI PADOVA

DOCTORAL THESIS

Innovative Architecture of dc-dc Converters for High Efficiency Applications in Harsh Automotive Environment

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"Omnis cum in tenebris vita laboret"

T. L. Caro

Abstract

In the last years the strive for car emission reduction produced several changes in the automotive environment, which led to a significant increase of power electronics presence on cars. Linear dc-dc converters are being replaced by higher efficiency switching-mode power converters also in the standard 12 V-to-5 V application, while hybrid electric and full electric vehicles require bidirectional high power dc-dc converters for their powertrains. To decrease the car fuel consumption, a reduction of the copper cable weight is required. For these reasons car manufacturers propose to shift the battery voltage from 12 V to 48 V and to deliver this single bus throughout the car, while deriving all the required voltages locally. This scenario pushes for high step-down converters.

The goal of this thesis is to optimize the operation of automotive dc-dc switching converters through the use of digital regulators and controllers. As a general philosophy no additional devices are added to the power stage and the topology modulation degrees of freedom are exploited to regulate and optimize its operation. This research activity is conducted through a collaboration between the Power Electronics Group of the Department of Information Engineering (DEI) and Infineon Technologies Italia S.r.l.

In the first part the minimum *rms* current trajectory (MCT) for a high-power bidirectional series-resonant dual-half bridge (SR-DHB) is analytically calculated, approximated and implemented on a digital controller which makes the converter to act as an optimized building block driven by a power command.

Secondly the 12 V-to-5 V application is analyzed and a non-resonant dual half-bridge – also called non-inverting buck-boost – is selected. Its efficiency is optimized on-the-fly by measuring the input current while a low-complexity hardwired simplex algorithm acts on the modulation quantities to find the

highest efficiency point. This approach is robust against operating condition variation.

In the third chapter the SCTI converter topology is considered because of its increased duty cycle range and the zero voltage switching turn-on for all devices. The SCTI is a promising topology but suffers from a potential voltage spike during transient events, which poses a reliability issue for the converter. Both a snubber and a control solution are proposed. With the former a careful design is required taking into account several parasitics, which coul be challenging to be measured. For this reason a solution based on a finite state machine which only requires analog comparators is then proposed and developed. Since SCTI topology is not a wide-spread topology, there is a shortage of commercially available *ad-hoc* inductors. During a research period in Infineon Technologies A.G. under the supervision of prof. Pelz, the SCTI converter efficiency was studied and optimized by considering off-the-shelf inductors only. To perform this optimization, Cadence® simulations are run and machine learning algorithm are employed in order to have a good understanding of the converter efficiency on the full design space and providing preliminary inductor design guidelines.

Sommario

Negli ultimi anni l'adeguamento a normative europee sempre più severe in materia di emissioni di anidride carbonica ha portato ad un'evoluzione del settore automotive. Uno dei cambiamenti più rilevanti è l'incremento significativo di elettronica di potenza a bordo. I convertitori dc-dc lineari vengono gradualmente sostituiti da regolatori a commutazione che permettono di raggiungere efficienze più elevate. Lo sviluppo di veicoli ibridi o completamente elettrici ha inoltre richiesto la presenza di convertitori bidirezionali ad alta potenza. Avendo sempre in mente l'obiettivo di ridurre le emissioni, alcuni produttori di automobili stanno promuovendo l'adozione di un unico bus a 48 V, dal quale derivare localmente le tensioni richieste dai dispositivi a bordo per mezzo di convertitori dc-dc ad alto *step-down*. Dunque anche la batteria non è immune al cambiamento.

L'obiettivo di questa tesi è di ottimizzare i convertori dc-dc del settore automotive mediante l'impiego di controllori digitali. È stato evitato di aggiungere ulteriori dispositivi di potenza mentre si è agito sulle grandezze di modulazione (*duty-cycle* e sfasamenti) al fine di migliorare il funzionamento del convertitore. Questa attività di ricerca è stata possibile grazie alla collaborazione tra il gruppo di elettronica di potenza del dipartimento di ingegneria dell'informazione (DEI) dell'Università di Padova e Infineon Technologies Italia S.r.l..

La prima parte di questo lavoro si occupa delle traiettorie a minima corrente *rms* per il convertitore a doppio mezzo ponte risonante. L'espressione analitica è calcolata, semplificata e infine implementata per mezzo di un controllore digitale. In questo modo il convertitore può essere considerato come un modulo ottimizzato che riceve come segnale di controllo il valore di potenza.

In secondo luogo è stata considerata la conversione da 12 V a 5 V mediante

un convertitore a doppio mezzo ponte nella versione non risonante. In questo caso l'efficienza viene ottimizata mentre il convertitore è in funzionamento. La corrente di ingresso viene infatti misurata e l'algoritmo del simplesso agisce sul *duty-cycle* e lo sfasamento in modo da raggiungere il punto di massima efficienza. Questo approccio permette di ottenere un'ottimizzazione indipendente dal punto di lavoro e dal valore dei componenti, risultando quindi robusto anche in caso di invecchiamento dei dispositivi o variazioni di temperatura.

Nella terza parte della tesi è stata selezionata la topologia SCTI per via dell'aumento di duty cycle che permette e delle commutazioni a zero tensione per tutti e tre gli interruttori di potenza. La topologia SCTI è promettente ma alcuni transitori tendono ad innescare un elevato picco di tensione che risulta in un grave problema di affidabilità. Per questo motivo sono state sviluppate due soluzioni, una circuitale basata su un soppressore ad avvolgimento ausiliario ed una di controllo. Benché la prima dia buoni risultati, è necessario prestare sufficiente attenzione ai parassiti, specialmente le induttanze di dispersione. Per questo motivo è stata implementata una soluzione basata su una macchina a stati finiti che richiede esternamente solo due comparatori analogici. Il convertitore SCTI non è una topologia comunemente impiegata e di conseguenza non è possibile trovare induttori *ad hoc* in commercio. Per questa ragione l'efficienza del convertitore SCTI è stata successivamente analizzata e ottimizzata considerando solo componenti presenti a catalogo. Durante un periodo di ricerca presso Infineon Technologies A.G. a Monaco sotto la supervisione del prof. Pelz, sono state eseguite a questo fine simulazioni Cadence®predisposte anche grazie ad algoritmi di *machine learning* messi a disposizione dal gruppo di Monaco. Questo lavoro ha permesso di comprendere come l'efficienza del convertitore varia su tutto lo spazio di progetto e di ottenere delle linee guida per il progetto dell'induttore.

Acknowledgments

First I want to thank my supervisor prof. Luca Corradini, whose suggestions have been crucial for this work. His help has been there when it was needed most and his method and keen eye for detail was invaluable for the work done together. With him I wish to thank also prof. Giorgio Spiazzi, whose insight in converter topologies was from time to time simply illuminating and prof. Paolo Tenti, whose passionate lectures are basically the reason why I began to study power electronics (and to listen to opera music, but that's probably off-topic). I owe my thanks also to prof. Leopoldo Rossetto for his great help with analog electronics – even when more audio than work-related – and to prof. Simone Buso and Paolo Mattavelli for the quite useful discussions, which we had during these years.

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I would like to express my gratitude for the assistance given by Tommaso Caldognetto, Marco Stellini and Luca Scandola especially during my first steps as Ph.D. student. For all this time spent in the same laboratory, I wish to thank all my colleagues and especially Weijian Han for his great help with the series resonant converter project. His perseverance and tidiness are more than admirable. "Diciassei" thanks also to Hildo, whose "funsionamainiente"

life-style helped all of us to work in the lab, especially when things did not go as planned and it means almost always. Thanks also to my office and Ph.D. colleague Stefano and Eslam for his eternal optimism and kindness.

I owe my thanks to my parents, who always encouraged me and to my brothers Patrick and Mirko, who was always ready to give me a hand. Finally I wish to thank Sara

Quacum vitast

quasi sole illustrata

Contents

Chapter 1

Introduction

During the last decade, the production of cars and commercial vehicles showed a steady increase (Fig. 1.1), which was only briefly hindered in 2009 after the Great Recession. The number of motor vehicles is deeply bounded with the population growth Fig. 1.2a [2] which is not uniformly spread over the world regions. This growth – mainly due to emerging countries (e.g. China, Brazil and India) – reflects itself on the car production, as shown in Fig. 1.3. The importance of automotive market appears clear from the manufacturer revenue, which in 2016 reached a value over 1000 billions of U.S. dollars (Fig. 1.4). The shared opinion is that the growth in the automotive market is accelerating, while moving toward new directions. Four are the main forces which will lead the future automotive market [3], namely the car electrification, autonomous vehicles, shared mobility and connectivity.

Today more than 800 million cars are driven only in the United States,

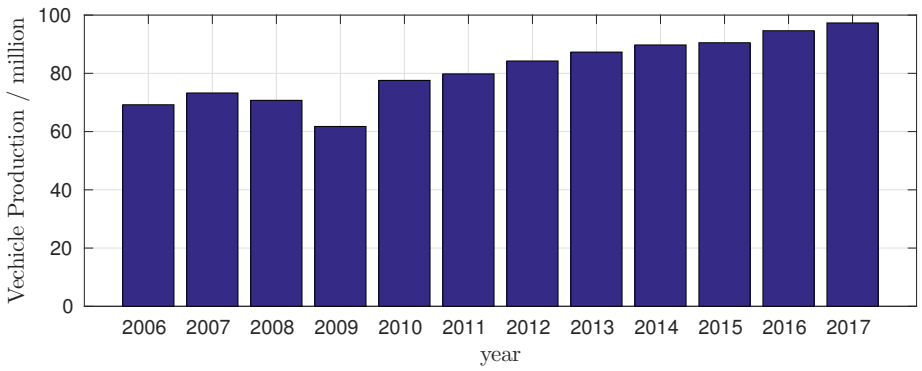
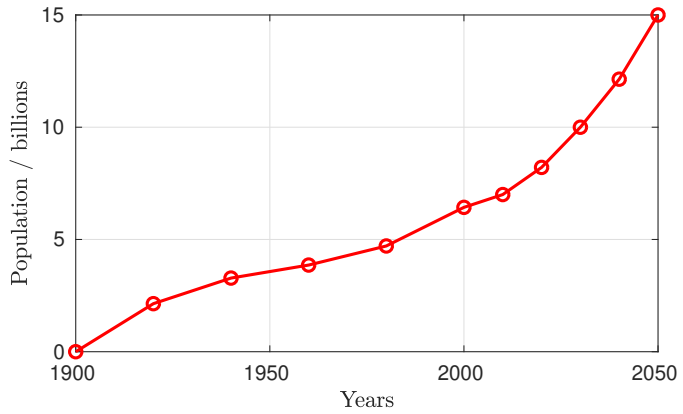
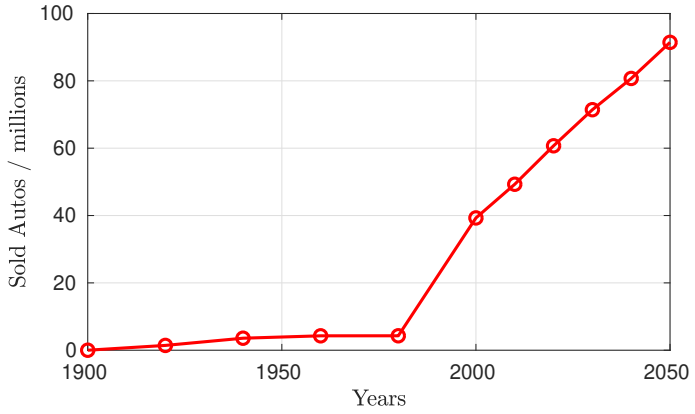


FIGURE 1.1: Car and commercial vehicle production from 2006 to 2017 [1]



(a)



(b)

FIGURE 1.2: Past and estimated population trend in billion (a) and million car passenger cars sold per year (b)

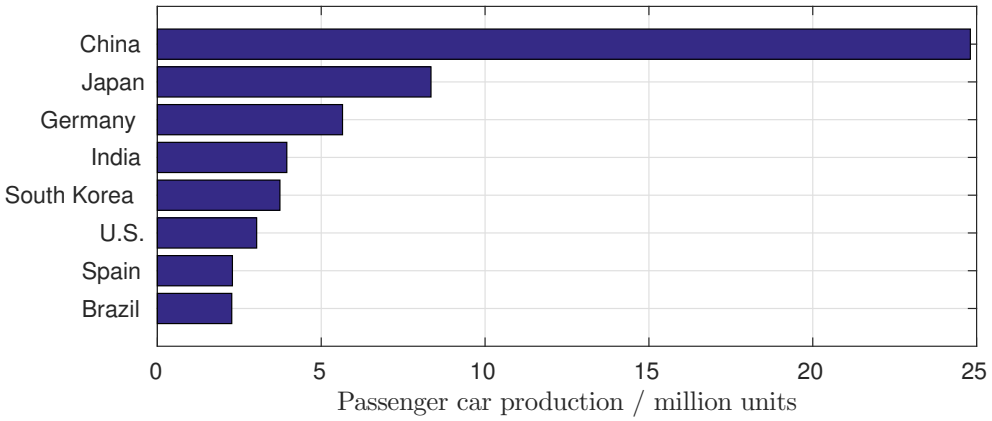


FIGURE 1.3: Car production in 2017 for selected countries (ordered by produced units [1]).

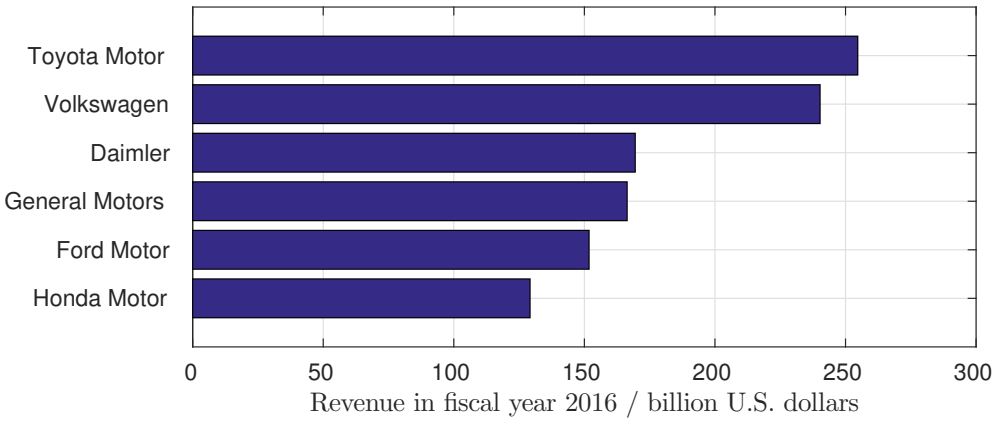


FIGURE 1.4: Revenue of the leading automotive manufacturers in 2016 [1].

leading to 85 million oil barrels consumed every day, a number which is increasing. Oil resources on Earth are limited and several researches indicate that they will end in about 40 years [2]. Emissions related to burning oil have also effects on the environment and health. Environmental concerns are related to carbon dioxide (CO_2) emissions, responsible for global temperature increase, which causes sea level increase and ecosystem instability. Fossil fuel powered vehicles produce also nitrogen oxides (NO_x) which pollute the air and have proven negative effects on human health. *Electrification* of cars can solve the aforementioned problems. Electrical engines are proved to be more efficient even with oil generated electricity. An electric car can travel for about 180 km with about 4 L of gasoline, compared to the about 60 km of an internal combustion engine (ICE) car. But electricity can also be produced through renewable sources, moving the personal transportation toward sustainability. Among the aforementioned advantages, full electric vehicles (EVs) can take advantage from the surplus of energy production in the grid during the night, helping also to solve the present storage capability shortage. So far the hinder to wide-spread adoption of full electric vehicles are the high cost related to high-capacity batteries and the limited driving range. To overcome these problems, hybrid electric vehicles (HEVs) have been developed. The conjunction of an electric drive with a combustion generator

overcomes the driving range limit, while providing the low fuel consumption typical of electrical powertrains. Since personal vehicles are mostly used for commuting, plug-in hybrid vehicles (PHEVs) have also been proposed. PHEV are equipped with a battery which can be plugged to the grid and which supports a limited driving range (e.g. 50 km), providing enough energy for daily city commutes. When the battery is depleted, PHEV vehicles operate as HEVs. But in the long run the convergence of stricter emission regulation, the drop of battery cost and the increase of the number of charging stations will push the adoption of fully electric vehicles (EVs). It is estimated that in 2030, the EVs share of new car sales will be between 10% and 50%. *autonomous vehicles* (AVs) do not encounter wide consumer and regulation acceptance yet, but advanced driver assistance systems (ADAS) are today a market reality and will lead AV future adoption. A probable scenario sees half of the vehicle sold in 2030 to be at least highly autonomous (NHTSA[1] level 3).

Especially in dense cities, lack of parking and traffic jams lead to increased interest in *shared mobility*, which both requires and emphasizes *connectivity*.

All these trends mean a steady increase in the silicon quantity and value on board, as clearly shown by the projections of the PWC[2] Semiconductor report (Fig. 1.5, [4])

Consumer and safety electronics require supplies whose static and dynamic specifications are strict, because of the sensitiveness of digital loads. Different supply voltages have to be derived from the common 12 V battery, which undergoes steep voltage variations during operation. Traditionally the supplies are obtained through linear dc-dc converters, which achieve tight and fast regulation of the output but show poor efficiency, which translates into increased emissions. In December 2015 196 countries signed the Paris Agreement, whose objective is to keep by 2020 the average temperature

[1] National Highway Traffic Safety Administration
[2] Price Waterhouse and Cooper.

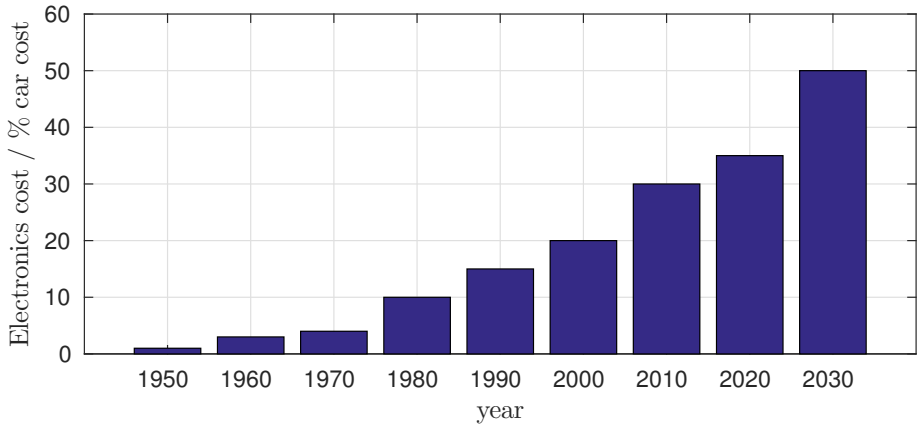


FIGURE 1.5: Automotive electronics cost as percentage of total car cost [4].

increase lower than 2 °C by strictly limiting the CO_2 emissions. To reduce emissions and fuel consumption, the automotive environment is experiencing a transition from linear dc-dc converter to switching converters, also for standard 12 V to 5 V application. This major change is pushing a pervasive use of power electronics in automotive scenario. Switching dc-dc converters reduced dramatically the heavy load power loss, but efficiency is usually lower at light load, hence the improvement of light load efficiency is a a topic of interest. The strive for CO_2 reduction pushed the development of hybrid-electric (HEV) and full electric (EV) vehicles, requiring more electric power demanding trains, which need bidirectional dc-dc converters for engine driving and regenerative braking. The higher electrical power in these new vehicle typologies is also suggesting the replacement of the 12 V battery with a higher voltage (48 V) solution. This new bus will start appearing in HEVs, where the current demand is greater than internal combustion engine vehicles (ICEV), but it will only assist the traditional 12 V battery and is not envisioned to replace it in the next future. So far the required supply voltages are obtained by dc-dc converters and delivered trough the car by means of copper cables. These copper cables have a wide cross section, because of the high current required by the loads. Hence they are heavy and costly, thus exerting negative influence on both car fuel consumption and price. For these

reasons car manufacturers proposed to deliver the 48 V bus only throughout the car and to derive locally all the required supply voltages. In this case a single smaller cross section wire is used, but high efficiency, high step-down converters are required (e.g. for microcontroller supplies) posing a stronger challenge for efficiency improvement. These motivations highlight the need of efficiency optimization for switching converters in automotive environment.

1.1 Efficiency Optimization

The main contributions to efficiency degradation in switched-mode power converters are switching and conduction losses and several works aim to improve the efficiency focusing on them separately. A way to reduce these loss source is by altering the converter power stage, by adding additional passive and active components. In [5] the switching losses of a full bridge converter have been reduced by increasing the operating region where the transistors switch on at zero v_{ds} voltage (Zero voltage switching, ZVS). This result has been obtained by adding two more inductors to the standard topology, thus increasing the circulating current. Large DC capacitors have also to be added leading to an increased hardware complexity. Full-bridge converter is also the topic of [6] which propose a hardware modification based on a energy recovery snubber, which mitigates switching losses and also helps reducing conduction losses. In [7] and [8] two active clamp snubbers are proposed for flyback converter which prevent the commutation spike caused by the leakage inductance but also achieve ZVS commutation for both primary and auxiliary switches. Snubbers can be designed to address single power switches as in [9] where an active snubber based on an inductor, a capacitor and a diode is designed to reduce the turn-off switching losses of an IGBT. In these cases, the addition of passive and active elements lets the converter to achieve ZVS/ZCS

and/or to reduce the conduction losses. The increased component count not only increases the price of the solution but can also lead to a reduced reliability.

The efficiency can be improved without auxiliary circuits, exploiting the degrees of freedom which are offered by the topology. In [10] the dead time duration is the degree of freedom which is optimized in a synchronous buck converter. Longer dead times lead to increased body diode conduction losses and reverse recovery, while shorter dead times can lead to simultaneous conduction of both transistors. Since a buck converter is considered, the optimization can be performed in a sensorless way, relying on the duty cycle information only, thus achieving higher efficiency without the addition of any extra element. The control layer has been modified without affecting the topology.

The same approach can be adopted for topologies which offer a higher number of degrees of freedom. The dual active bridge (DAB) converter consists of two full-bridges linked by a transformer. This converter is traditionally controlled by changing the phase shift between two 50% duty cycle voltage square waves imposed by the two full-bridges. But a full-bridge can also be modulated to obtain a three level PWM, thus increasing the number of degrees of freedom. In [11] the added pulse modulation to one bridge is exploited to increase the ZVS operating region. In [12] the series resonant dual active bridge (SR-DAB) degrees of freedom have been used to find the modulation strategy which minimizes the RMS inductor current value for a given output power. In [13], some auxiliary circuit elements are added increasing the degrees of freedom and ensuring ZVS for all switches over broad input and output voltage variation.

The DAB converter offers several degrees of freedom but requires a high number of switches. Another topology which provides many modulation quantities while needing four transistor only is the dual half bridge (DHB). This topology can be used when isolation is not required and bidirectional

step up and step down operation is desired. In [14] the switching instants are exploited to achieve ZVS turn on in every load condition.

The software based optimization can be divided into the *offline* and *online* approaches. In the former, the desired trajectory in the degrees of freedom space has to be previously evaluated for every load and transfer ratio condition as in [11,12,14,15]. Then the results have to be stored in look-up table or calculated on the fly. The *online* optimization approach is performed during the converter operation [10]. The main advantage of the online efficiency optimization is the small dependence on components value and operating condition, achieving robustness against aging and load change. The main disadvantage is the increased control complexity due to the less predictable dynamical behavior.

The last point is about the quantity to be optimized. In [11,12,14] only switching or conduction losses are optimized, while in [10] the overall efficiency is optimized, even if it has been made indirectly. In order to optimize the efficiency in more complex topology, the quantity which has to be minimized is the input current.

1.2 Digital Control of dc-dc Converters

Power electronics modeling is based on the continuous-time averaging analysis [16–18] and from the beginning linear analog controllers are used to regulate voltages or currents. Analog controller and pulse-width modulator require a small amount of analog building blocks and fast and precise linear controller can be easily implemented. For these reasons, integrated switch-mode power supply controllers have been industry standard for many decades. Digital control loops suffer from delay related to the digital pulse-width modulation and the A/D conversion time. Furthermore regulation

accuracy depend on A/D and DPWM resolution, which also play a major role in the limit cycling condition [19].

In high power applications, more complex power management system [20,21] and safety concerns pushed for an early adoption of digital controllers, whose cost and power consumption remains negligible with respect to the total system price and dissipation.

For low-to-medium switching-mode power supplies the adoption of digital controllers was slower. Switching frequencies in the hundreds of kilohertz to megahertz range and faster transient response hindered the employment of early digital controller implementations. Advantages in both technology and digital techniques made it possible the wide-spread adoption of digital controllers also in low-power converters. Technology improvement consists of increased processing capabilities and decreased cost for digital integrated-circuit processes and the introduction of CMOS processes with high-voltage extensions, which made possible the full power stage silicon and digital control single-chip integration. Improved techniques include hybrid counter/ring oscillator DPWM [22,23] which can achieve extremely small duty cycle resolution, keeping the clock frequency in the switching frequency order of magnitude and the windowed A/D converter [24], which permits the tight voltage regulation without a high-frequency high-resolution ADC. A secondary beneficial effect of the low-bit windowed A/D is that multiplication can be performed through a small look-up table (LUT) [25–27].

A second major push to digital controller adoption is represented by the development of non-linear control techniques, whose main benefit is the ability to precisely adjust the switching instants, which can lead to increased transient speed and converter efficiency. Even if non-linear control was developed also for analog [28] controller, digital regulators let more complex and efficient techniques to be employed [29,30], which cannot be easily implemented on their analog counterparts. An early example is the state trajectory control

law, proposed in [31], which let the desired steady-state condition be met in one single cycle. Many implementation of this concept followed when digital control became wide-adopted [32] and time-optimal control was since a main topic of switched-mode power supply control [32–35]. Also efficiency can be improved through digital control [10,36], which can be used to segment the power switches [37] but also to apply phase-shedding technique [38].

The main advantages of digital control is programmability and the interface compatibility power management systems, which are becoming more and more relevant also in low-power applications. For this reasons in this thesis digital control is employed. For each analyzed scenario, a two block digital system is considered, namely a PID digital regulator is implemented to regulate the output voltage, while a second block is used to optimize the efficiency of the converter (Chapters 2 and 3) or to improve its reliability 4.

1.3 Scope and Outline of the Thesis

The thesis focuses on the digital control of dc-dc converters for automotive applications and the goal is to control and improve efficiency without adding additional power devices to standard topologies. The approach followed in the thesis consists in analyzing the relations between the topology modulation quantities and the converter operation and losses in order to maximize efficiency through control. As mentioned in this thesis digital control is considered for its simple expansion capabilities. dc-dc converters are regulated by digital PID controller, while *ad hoc* finite state machines (FSM) or combinational circuits act on the modulation degrees of freedom in order to enhance performance of the converter. Performance includes losses (e.g. conduction losses), the total efficiency or voltage stresses. The digital controllers are implemented on FPGA for sake of simplicity, but their complexity is kept limited with the aim of integration (ASICs).

Bidirectional high power automotive application is discussed in chapter 2, where a digital control for a resonant dual half-bridge provides general conduction losses minimization. A simplified trajectory in the modulation quantities space is devised in order to code a controller which requires low computational power or low digital gates count. The main benefit is that these trajectories depend on the conversion ratio only, hence they are independent of the converter design and they are calculated once and for all in this chapter.

Chapter 3 deals with online efficiency optimization for a conventional 12 V to 5 V application. As mentioned linear dc-dc converters are recently being replaced by switching ones, thus leading to higher efficiency but also increased size. To address this problem, small inductors are required and this leads to higher current ripple and higher conduction and core losses. The dual half-bridge topology is considered and three modulation quantities taken into consideration. One of them is used to control the output voltage, while the other two are provided by a low-complexity simplex algorithm which is hardwired in a FPGA board. The algorithm senses the input current and acts on the two degrees of freedom in order to minimize the current absorbed by the converter. With controlled output voltage, it is equivalent to optimize the efficiency. With respect to an *offline* optimization, based on fixed trajectories, this approach is robust against operating condition variation. Moreover no accurate loss model is required, whose implementation is challenging because of the switching losses complex modeling.

As a mentioned approach to further reduce CO_2 emissions, car manufacturers propose to deliver a single 48 V bus throughout the car and to derive locally all the required supply voltages. This way only a small cross-section wire is required, thus leading to lower weight and cost, but high efficiency high step-down converters are needed. In chapter 4 the series capacitor tapped-inductor (SCTI) is selected for the 48 V to 1.5 V interface converter between the next generation 48 V bus and a microcontroller supply. SCTI

converter is a promising topology but it suffers from an issue, which is related to input voltage or duty cycle step and which leads to a non-negligible voltage spike. In this thesis a digital control is provided in order to prevent this spike to occur. This control technique is compared with a hardware solution, which consists in an auxiliary winding snubber, which is described later in the chapter. To adopt this topology in automotive environment, only commercial components should be used. SCTI requires a $n:1$ coupled inductor, whose commercial availability is limited. To address this problem an analysis of the converter losses has been carried out during a research period in Infineon A.G. in Munich (Germany). The preliminary results of this study are also presented in chapter 4.

Chapter 2

Series Resonant Dual Half-Bridge Conduction Losses Minimization

2.1 Introduction

Hybrid Electric and Full Electric vehicles power trains require high power bidirectional dc-dc converters to transfer power from battery to a voltage bus and vice versa. Moreover the power distribution system consists in multiple voltage domains [39,40] which have to be managed through dc-dc converters.

Bidirectional converters are not restricted to automotive application, they become building blocks in many energy management architectures [41]. Their use and coordination are key elements of future dc micro and nanogrids intended for residential or commercial use [42–47], and in other application-specific dc power distribution systems [48,49]. In all these cases the converter is controlled with a power signal which acts as reference for a control loop. The power command depends on the available resources or the required voltage or current regulation.

Isolation requirements and power processing levels drive the selection of the suitable topology for bidirectional power processing. High power (above kilowatt range) naturally leads to the dual active bridge (DAB) converter [50, 51]. It features reduced current stress, galvanic isolation and many modulation

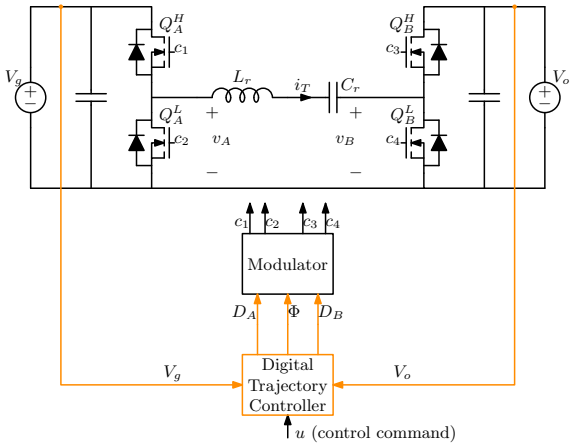
quantities which can be exploit to reduce losses or stresses. In [11, 52–54] advanced modulation strategies are disclosed in order to extend the zero voltage switching range or to reduce the conduction losses. Minimum-*rms* current modulation scheme is described in [55] where closed-form expression relates all the modulation quantities to the current for various power levels. In [56] a digital controller is employed to optimize the efficiency of a DAB converter at high switching frequency and low output current level. Also the *half*-bridge version has been subject to investigation and control-based optimization [14].

Replacing the reactive element (inductor or transformer) with a resonant tank, leads to the series-resonant converter (DBSRC), which has been deeply analyzed [12, 13, 57–61]. As for the DAB converter, the topology offers several modulation quantities, which can be exploit for optimzation purpose. The simplest and traditional modulation is the phase-shift modulation (PSM), where the two bridges produce a 50% duty cycle at the switching nodes and the phase-shift between these two square waves is used to control the output power in both sign and magnitude. A general analysis of this modulation strategy based on fundamental harmonic approximation [62] is disclosed in [59], where it is highlighted the ZVS operating range as a function of the output power.

More modulation quantities can be employed, thus obtaining control degrees of freedom, which can be used optimize a target value. In [12] a multi-angle phase shift modulation is proposed, in which the modulation degrees of freedom are used to minimize the *rms* tank current value. A closed-form solution to the minimization problem is proposed and the converter is forced to operate along the minimum current trajectories (MCT) in the modulation space. Dynamical small-signal modeling for this approach is address in [60], while a closed-loop implementation of the MCT-controlled DBSRC is presented in [61, 63].

For lower output power the *half*-bridge version of the DAB converter become of interest because of the reduced part count. The series-resonant dual half-bridge (SR-DHB Fig. 2.1a) is capable of bidirectional step-up and step-down operation. It avoids the transformer and the presence of the DC-blocking capacitor is of interest where first failure short circuit between the two voltage source should be avoided. With standard PSM sub-optimal efficiency is achieved by this topology at light load, where ZVS operation is lost and high reactive tank current leads to increased conduction losses. Efficiency drops quickly as the transfer ratio departs from unity.

To solve these issues, in this chapter the SR-DHB is combined with a low-complexity digital *trajectory controller*, thus forming an efficient power-controlled unit (Fig. 2.1a).



(a)

FIGURE 2.1: Trajectory-controlled SR-DHB bidirectional power unit operating between two dc voltages V_g and V_o

2.2 Phase-shift Modulation of Series-Resonant Converters

The standard modulation strategy employed with the SR-DHB is the phase-shift modulation. With this modulation the two bridges constituted by Q_A^H,Q_A^L

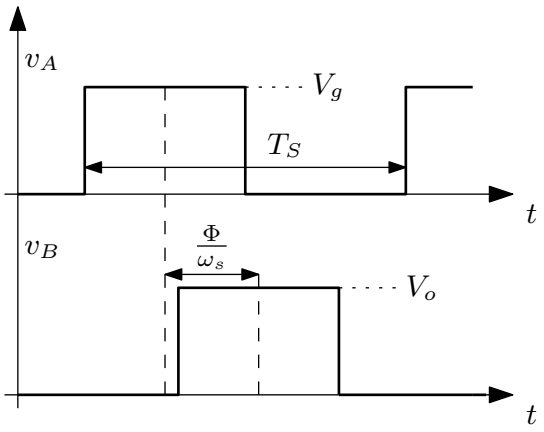


FIGURE 2.2: Phase-shift modulation (PSM).

and Q_B^H, Q_B^L are operated with a 50% duty cycle command (Fig. 2.2). Under the fundamental harmonic approximation (FHA, [62]) the output power can be expressed as

$$P_o = \frac{2}{M\pi^2}\frac{V_o^2}{|Z_T|}\sin(\phi) \tag{2.1}$$

where Z_T is the tank impedance evaluated at the switching angular frequency ω_s, i.e. $\jmath\omega_s L_r + \frac{1}{\jmath\omega_s C_r}$. For an ideal tank modulated above its resonant angular frequency ω_r, it can be also be expressed as

$$|Z_T| \triangleq Z_0\frac{1-r^2}{r}, \tag{2.2}$$

with

$$r \triangleq \frac{\omega_r}{\omega_s} < 1, \qquad Z_0 \triangleq \sqrt{\frac{L_r}{C_r}}. \tag{2.3}$$

The maximum output power which can be transferred is

$$P_{o,max} = \frac{2}{M\pi^2}\frac{V_o^2}{|Z_T|}. \tag{2.4}$$

The value of phase command ϕ required to transfer a power normalized power $P_{o,N} \triangleq P_o/P_{o,max}$ is obtained from (2.1):

$$\phi = \arcsin\left(P_{o,N}\right). \tag{2.5}$$

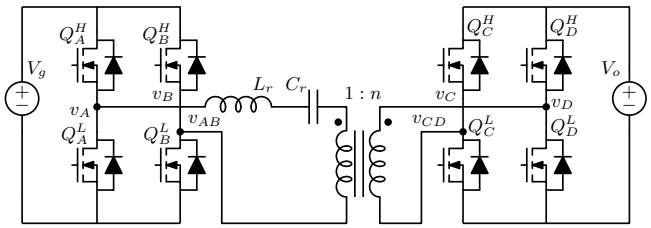


FIGURE 2.3: Series Resonant Full-Bridge Converter

Only the phase-shift ϕ is used, and there is only a value of ϕ which let a power $P_{o,N}$ to be transferred. In this case no optimization is possible.

2.3 Minimum Current Trajectories

If the duty cycles of the two legs D_A and D_B are controlled in addition to ϕ, a modulation strategy can be devised to optimize the efficiency while transferring the required output power. A main issue with resonant tank topologies is the circulating tank current at light load. To address this problem a minimum *rms* current trajectory (γ_{MCT}) can be calculated under the fundamental harmonic approximation.

2.3.1 Review of MCT in the Full-Bridge Series-Resonant Converter

Minimum conduction trajectory concept for series-resonant converters is first proposed in [12], where the modulation quantities are uniformly considered as phase shifts for series resonant full-bridge converter (SR-DAB) (Fig. 2.3). The four half-bridges voltages v_A, v_B, v_C, v_D are square waves, but the phase shifts between them $\phi_{AB}, \phi_{AD}, \phi_{BC}$ cause the transformer applied voltages v_{AB} and v_{CD} to have different duty cycles. The normalized output power under the fundamental harmonic approximation is for the SR-DAB

$$P_{o,N} = \sin\left(\frac{\phi_{AB}}{2}\right)\sin\left(\frac{\phi_{CD}}{2}\right)\sin\left(\phi_{AD} + \frac{\phi_{DC} - \phi_{AB}}{2}\right) \tag{2.6}$$

where $P_{o,N} \triangleq P_o / P_{o,max}$,

$$P_{o,max} = \frac{8}{n\pi^2} \frac{MV_g^2}{Z_0} \frac{r}{1-r^2},$$

$Z_0 = \sqrt{L_r/C_r}$ and $M = V_o/(nV_g)$. The MCT is defined as the trajectory over which the required power level is transferred with the minimum *rms* current value. The optimization is performed through Lagrange multiplier and the closed form solution is provided for both step-up and step-down application. In the case $M < 1$ the MCT lies on the $\phi_{DC}/2 = \pi/2$ plane. Depending on the power level, two expressions for the MCT are provided. For $P_{o,N} < \sqrt{1-M^2}$

$$\begin{cases} \phi_{AD} & = \frac{\phi_{AB}}{2} + \arctan\left(\frac{P_{o,N}}{M}\right) - \frac{\pi}{2} \\ \frac{\phi_{AB}}{2} & = \arcsin\left(\sqrt{M^2 + P_{o,N}^2}\right) \\ \frac{\phi_{DC}}{2} & = \frac{\pi}{2} \end{cases} \tag{2.7}$$

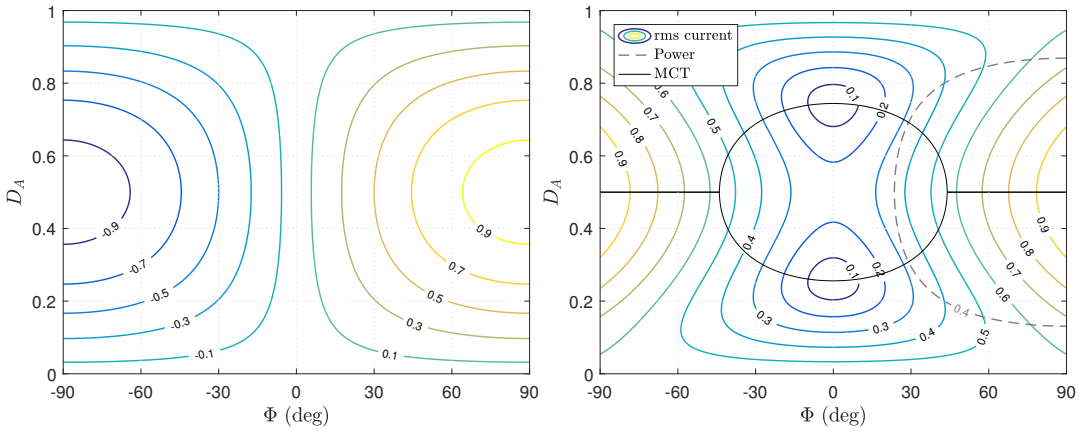
while for $P_{o,N} \geq \sqrt{1-M^2}$ the solution yields

$$\begin{cases} \phi_{AD} & = \arcsin(P_{o,N}) \\ \frac{\phi_{AB}}{2} & = \frac{\pi}{2} \\ \frac{\phi_{DC}}{2} & = \frac{\pi}{2}. \end{cases} \tag{2.8}$$

In this last case, only ϕ_{AD} is used to control the power, while ϕ_{AB} is kept constant.

2.3.2 Development of MCT in the Half-Bridge Series-Resonant Converter

In the case of the SR-DHB topology here studied, the modulation quantities of interest are the duty cycles D_A and D_B of the input and output leg, and



(a) (b)

FIGURE 2.4: The (D_A,Φ) plane ($D_B = 0.5$) for $M = 0.72$: (a) normalized output power contours $P_{o,N} = P_o/P_{o,max}$, and (b) normalized tank *rms* current $I_{T,N} = I_T/I_{T,max}$ and MCT together with a single power contour $P_{o,N} = 0.4$.

the phase shift Φ between them. In this case the computed trajectory can be directly implemented in a combined PSM+PWM modulator.

Under the FHA, the output power and tank *rms* current are expressed by

$$P_o = P_{o,max} \sin(\pi D_A) \sin(\pi D_B) \sin(\Phi), \tag{2.9}$$

$$I_T = \frac{\sqrt{2}V_o}{\pi M |Z_T|} \sqrt{\begin{aligned} &M^2 \sin^2(\pi D_B) + \\ &-2M \cos(\Phi) \sin(\pi D_A) \sin(\pi D_B) + \\ &\sin^2(\pi D_A) \end{aligned}} \tag{2.10}$$

Contours of positive and negative output power for the converter on $D_B = 0.5$ plane are represented in Fig. 2.4a. The *rms* current contours under the same condition are reported in Fig. 2.4b. The power and tank *rms* current are represented in normalized form, $I_{T,N} \triangleq I_T/I_{T,max}$ and $P_{o,N} = P_o/P_{o,max}$, where

$$I_{T,max} \triangleq \frac{\pi P_{o,max}}{\sqrt{2}V_o} \sqrt{1+M^2}, \tag{2.11}$$

and are respectively achieved at $(D_A = D_B = 0.5, \Phi = 90°)$ in the positive direction, and at $(D_A = D_B = 0.5, \Phi = -90°)$ in reverse processing mode.

According to (2.9) and to Fig. 2.4a, a given output power level $\tilde{P}_{o,N}$ can be achieved via infinite combinations of D_A, D_B and Φ, each corresponding to a different tank current waveform and thus different *rms* value and conduction losses. Among such combinations, those that minimize the tank *rms* current define the MCT. The objective to operate the converter on MCT is equivalently expressed by the constrained minimization problem as shown in (2.12).

$$\min_{D_A,D_B\in[0,1],\Phi\in[-\frac{\pi}{2},\frac{\pi}{2}]}\{I_{T,N}(D_A,D_B,\Phi)\},\quad \begin{cases} P_{o,N}(D_A,D_B,\Phi)=\tilde{P}_{o,N} \\ -P_{o,max,N}\le\tilde{P}_{o,N}\le P_{o,max,N}\end{cases} \tag{2.12}$$

Lagrange multiplier optimization has been employed, yielding the following results.

Step-Down Case

For step-down case, where $M<1$, the control space points which achieve the minimum *rms* current value for a given normalized output power lie on the $D_B=0.5$ plane and they are expressed by

$$\gamma_{MCT}:\begin{cases}\Phi=\arctan\left(\frac{P_{o,N}}{M}\right)\\ D_A=\frac{1}{\pi}\arcsin\left(\sqrt{P_{o,N}^2+M^2}\right)\\ D_B=0.5\end{cases} \tag{2.13}$$

when $|P_{o,N}|<\sqrt{1-M^2}$. On the other hand, the minimum current trajectory becomes a pure phase shift modulation when $|P_{o,N}|\ge\sqrt{1-M^2}$, i.e.

$$\gamma_{MCT}:\begin{cases}\Phi=\arcsin\left(P_{o,N}\right)\\ D_A=D_B=0.5\end{cases}. \tag{2.14}$$

The MCT coincides with the simple phase shift modulation (2.14) down to a certain normalized power level $|P_{o,N}| = \sqrt{1-M^2}$. Below such value, it becomes possible to maintain the tank current in phase with v_B by modulating the duty cycle D_A according to (2.13).

A fully equivalent minimum current trajectory can be found by selecting the complement of $D'_A \triangleq 1 - D_A$, as shown also in Fig. 2.4. The two branches merge and coincide with the PSM at $P_{o,N} = \sqrt{1-M^2}$. The MCT solution here described is graphically represented in Fig. 2.4b, which illustrates the MCT branches on the $D_B = 0.5$ plane for $M = 0.72$. Such value corresponds to the nominal voltage conversion ratio of the experimental prototype described in section 2.6. Under the MCT, the tank *rms* current can be expressed in normalized form as

$$I_{T,N} = \begin{cases} \dfrac{P_{o,N}}{\sqrt{1+M^2}}, & \text{if } |P_{o,N}| \leq \sqrt{1-M^2} \\ \dfrac{\sqrt{1+M^2-2M\sqrt{1-P_{o,N}}}}{\sqrt{1+M^2}}, & \text{otherwise} \end{cases} \tag{2.15}$$

From Fig. 2.4b it can be seen how the MCT circumvents the regions of elevated *rms* current, as opposed to the pure phase shift modulation. This is especially true in the light load region, where the use of the MCT is expected to yield the strongest advantages. The figure also highlights a specific power contour $P_{o,N} = 0.4$. Minimization of the tank *rms* current operated by the MCT at this particular power level can be directly verified by inspection.

The similarity between (2.7) with (2.13) and (2.8) with (2.14) becomes evident if the relation

$$\frac{\phi}{2\pi} = \frac{t}{T_s} \triangleq D \rightarrow \frac{\phi}{2} = \pi D$$

is considered for ϕ_{AB} and ϕ_{CD}, which actually represent duty cycle of the two

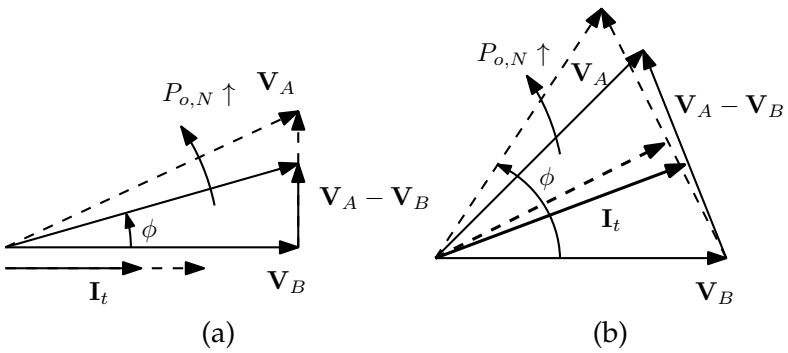


FIGURE 2.5: Phasor interpretation for (2.13) (a) and for (2.14) (b).

voltages applied to the transformer. For the SR-DAB converter MCT trajectories are useful when the input voltage has wide variation range, otherwise a suitable selection for n can provide minimun conduction and switching losses through simple PSM (2.8). On the other hand, the lack of transformer in the SR-DHB make the MCT trajectory important even in fixed input voltage applications. Note that in the step-up case $M > 1$ a completely symmetrical MCT solution is found on the $D_A = 0.5$ plane.

Phasor Interpretation of MCT

Physical reason for the change in the analytical expression of the MCT are disclosed in [12]. Minimum current operation corresponds to an output leg voltage v_B which has the maximum value (i.e. $D_B = 0.5$) and is in phase with the tank current. Since the current has a $\pi/2$ phase displacement with respect to the imposed tank voltage $v_A - v_B$, it means that v_A should increase its module, while sliding the perpendicular of $\mathbf{V}_B$. Thus the three phasors $\mathbf{V}_A, \mathbf{V}_B$ and $\mathbf{V}_A - \mathbf{V}_B$ describe a right triangle (2.5a). When $\mathbf{V}_A$ reaches its maximum value, the phasor has to departe from the perpendicular of $\mathbf{V}_B$ and the tank current start to have a phase displacement with it (Fig. 2.5b). Similarly can be discussed the case with $M > 1$, provided that the role of the two legs are exchanged.

2.3.3 Validation of the Fundamental Harmonic Approximation

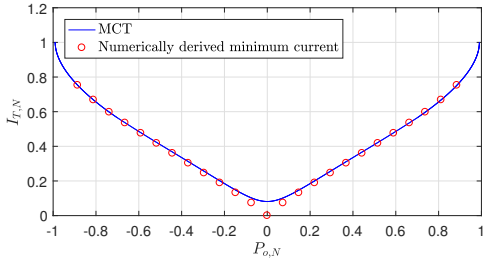
The validity of the FHA-based approach is demonstrated by comparing its expression with the global optimum solution of minimum *rms* current obtained considering ten harmonics. The numerical solutions are derived by numerically finding out all the combinations of modulation quantities (Φ, D_A ,D_B) corresponding to a given power level, and then calculating the *rms* current for each individual combination and determining the one corresponding to the lowest *rms* value.

When multiple harmonics are considered, the normalized tank *rms* current will depend on the frequency ratio r. In fact, in the fundamental harmonic approximation (FHA), the frequency ratio r only affects the amplitude of the tank current and when the *rms* current is normalized, the resulting expression is independent of r. On the other hand, when multiple harmonics are quadratically added to estimate the tank *rms* current, each individual harmonic amplitude depends on r, and normalization does not lead to dependence cancellation.

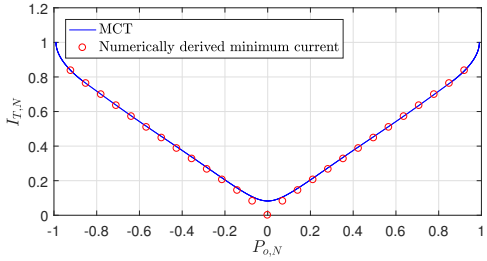
In this work the switching frequency f_s is kept constant, but r can change with different tank design, which brings different resonant frequency f_r. Here a resonant converter is studied, thus the r value is next to 1. The validity of the FHA heavily depends on its value and for this reason r range is assumed to lie in the range $0.8 \leq r \leq 0.95$ [57,59]. Note that lower values for r lead to non-resonant operation.

Fig. 2.6 reports the normalized tank *rms* current as a function of output power for different voltage conversion ratios ($M = 0.72$ and $M = 0.5$) and frequency ratios ($r = 0.85$ and $r = 0.95$). The actual minimum tank *rms* current, determined numerically, is compared with the *rms* current along the theoretical MCT derived using the FHA approach. Fig. 2.6 proves that the numerically calculated minimum-*rms* current is consistent with the one along

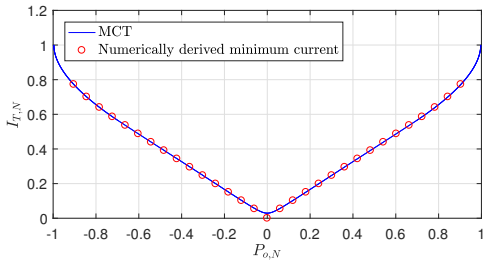
MCT, with minor deviations only appearing for power levels close to zero, where the duty cycle is lower and the number of harmonics increases.



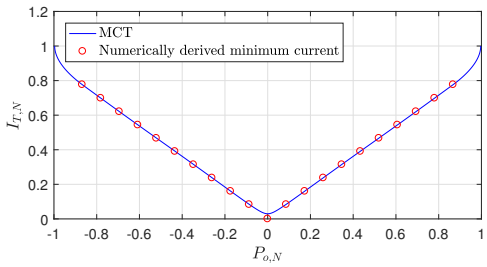
(a) $r = 0.85, M = 0.72$



(b) $r = 0.85, M = 0.5$



(c) $r = 0.95, M = 0.72$



(d) $r = 0.95, M = 0.5$

FIGURE 2.6: Comparison between the tank *rms* current evaluated along the MCT (solid line) and the actual minimum *rms* current derived numerically (dots), as a function of output power, for $r = 0.85$ and $r = 0.95$, and voltage conversion ratios $M = 0.72$ and $M = 0.5$.

2.4 Piecewise-Linear MCT Controller

Minimum current trajectory γ_{MCT} is a trigonometric function of the transfer ratio M. To implement directly (2.13) and (2.14) the evaluation of these expressions through power expansion or the use of large look-up tables (LUT) is required. In order to simplify the calculation of the γ_{MCT}, its linear approximation $\gamma_{PWL\text{-}MCT}$ (PWL-MCT) can be calculated. This formulation strongly reduces the complexity of the calculations, while eliminating the required LUT. Furthermore, the proposed PWL-MCT easily incorporates variations in the converter voltage conversion ratio as long as a digital estimate of M is available to the controller, e.g. via simple input/output voltage sensing.

The comparison of γ_{MCT} and the PWL-MCT is shown in Fig. 2.7, where three values for M are represented. For $P_{o,N} \geq \sqrt{1-M^2}$, i.e. when the MCT reduces to a pure phase shift modulation, the PWL-MCT, the MCT and the PSM all coincide. When $P_{o,N} \leq \sqrt{1-M^2}$ the PWL-MCT becomes a combination of a constant-D_A segment located at $D_A = D_{sat}$ at very light load, and a linear segment $D_A = D_0 + m\Phi$, defined by its slope m and its zero phase shift intercept D_0. The three parameters (D_{sat}, m, D_0) defining the PWL-MCT are determined numerically once and for all as a function of the transfer ratio $M$by minimizing the mean squared error ε between the true MCT and the PWL-MCT,

$$\varepsilon(D_{sat}, m, D_0) \triangleq \int_0^{\pi/2} |\gamma_{MCT}(\Phi) - \gamma_{PWL\text{-}MCT}(\Phi)|^2 d\Phi. \tag{2.16}$$

Since the MCT is only defined by M, quantities (D_{sat}, m, D_0) only depend on M. If the converter is to be operated over a range of voltage conversion ratios, three vectors $(D_{sat}(M), m(M), D_0(M))$ can be pre-calculated for the required M's. Such numerically-determined curves are depicted in Fig. 2.8. It is important to notice that, since these curves depend on the converter voltage conversion ratio M *only*, they are independent of the converter parameters.

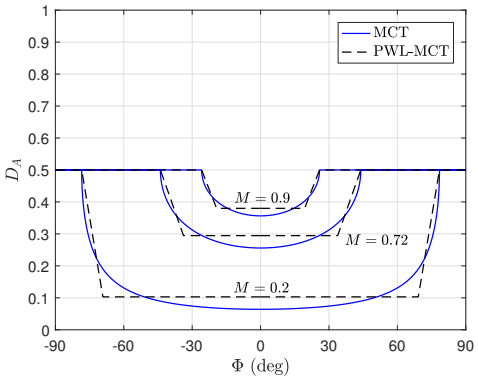


FIGURE 2.7: Proposed piecewise-linear approximation $\gamma_{PWL\text{-}MCT}$ of the true MCT γ_{MCT} for different values of M.

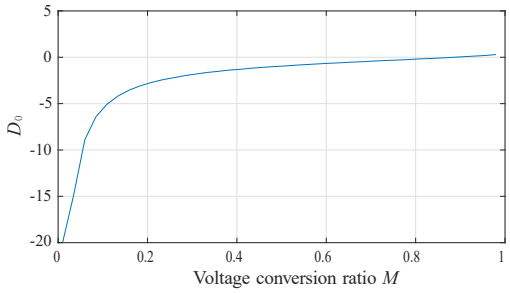
2.4.1 Implementation of the PWL-MCT

The block diagram of the proposed PWL-MCT controller which generates D_A as a function of Φ is depicted in Fig. 2.9. The power command u is provided externally by a controller and is directly transmitted to the phase shift, i.e. $\Phi = u$. At the same time, quantities $m\Phi + D_0$ and D_{sat} are evaluated, and the largest is assigned to D_A, i.e. $D_A = \max(m\Phi + D_0, D_{sat})$. As for M, the voltage conversion ratio is determined digitally by sensing the input and output voltages. Bidirectional converters are always equipped with input and output voltage sensing and therefore no additional hardware complexity is needed.

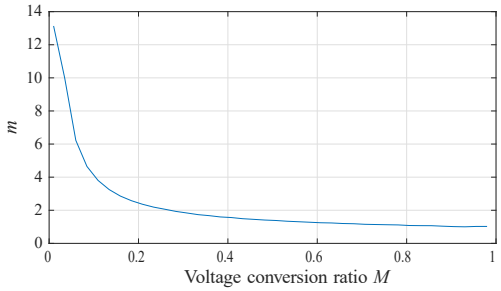
For the calculation of $D_{sat}(M)$, $m(M)$ and $D_0(M)$, as shown in Fig. 2.8 the three parameters show good linearity with respect to M in the range $0.4 \leq M \leq 1$ which covers almost all possible voltage conversion ratios in practical application. As a consequence, D_{sat}, m and D_0 can be expressed using linear fitting method based on the numerical results in Tab. 2.1,

$$\begin{aligned} D_0 &= -2.3442 + 2.6632M \\ m &= \ \ 1.9178 - 0.9820M \\ D_{sat} &= -0.0032 + 0.4276M \qquad M \in [0.4, 1] \end{aligned} \tag{2.17}$$

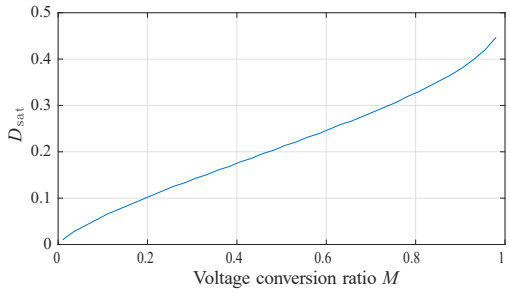
and the use of LUTs is entirely avoided. If wider voltage range is concerned



(a)



(b)



(c)

FIGURE 2.8: Numerically calculated parameters (D_{sat}, m, D_0) of the PWL-MCT trajectory as a function of the voltage conversion ratio M.

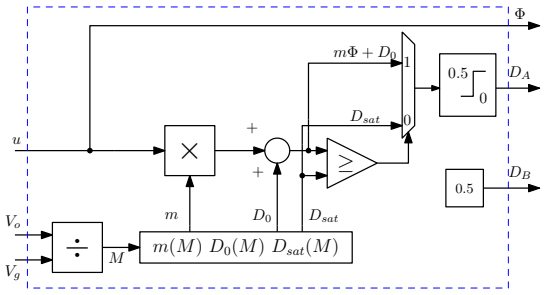


FIGURE 2.9: Proposed digital implementation of the PWL-MCT trajectory controller of Fig. 2.1a.

in the practical application, quadratic fitting or piecewise linear fitting can be used to achieve higher accuracy.

TABLE 2.1: PWL-MCT parameters evaluated at specific M's

M	D_0	m	D_{sat}
0.02	-20	13.217	0.018
0.05	-10.502	7.234	0.035
0.07	-7.64	5.424	0.045
0.1	-5.501	4.08	0.06
0.15	-3.77	3.007	0.083
0.2	-2.852	2.448	0.103
0.3	-1.877	1.877	0.141
0.4	-1.327	1.576	0.176
0.6	-0.671	1.263	0.246
0.8	-0.204	1.094	0.327
0.9	0.027	1.048	0.38
0.95	0.175	1.024	0.416

As it can be seen from Fig. 2.9, the proposed implementation only requires standard digital arithmetic functions, a strong simplification over a hypothetical implementation of the true MCT.

2.5 Switching Losses Along the PWL-MCT

Two major mechanisms of power dissipation are conduction and switching losses. While the use of the PWL-MCT trajectory reduces the former contribution, behavior of switching losses along the PWL-MCT requires a separate analysis.

A qualitative explanation is that since the PWL-MCT reduces the *rms* current value, it also reduces the amplitude of the tank current, thus decreasing the switched currents. Hence a beneficial side effect of the *rms* current optimization is a corresponding mitigation of residual hard-switching losses. It is interesting to notice, on the other hand, that forcing ZVS of all devices would *certainly* increase the overall circulating current and conduction losses. Similar considerations of *rms* current minimization are highlighted in [64] for Dual Active Half-Bridge Converters, also illustrating how a modulation strategy based on achieving ZVS of all devices can potentially lead to efficiency

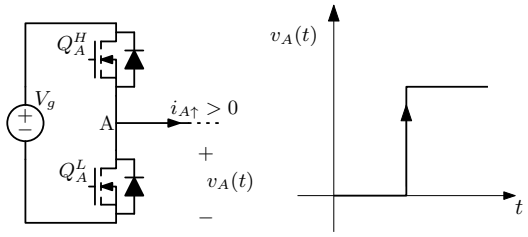


FIGURE 2.10: Low-to-high transition of the input leg A with positive switched current.

degradation due to excessive circulating current.

To prove quantitatively this point, a simplified analysis is carried out. Four switching instants are considered, namely the input leg low-to-high and high-to-low transitions, with the associated switched currents $i_{A\uparrow}$ and $i_{A\downarrow}$, and the output leg transitions associated with $i_{B\uparrow}$ and $i_{B\downarrow}$. Currents $i_{X\uparrow}$ and $i_{X\downarrow}$ associated with leg X are here defined as *outsourced* by the switching node.

Consider, for definiteness, the low-to-high transition of the input leg A sketched in Fig. 2.10. If the current $i_{A\uparrow}$ is positive as indicated in the figure, the inductor current flows through the lower MOSFET body diode during the dead time. Hence Q_A^L undergoes ZVS turn-off, while Q_A^H undergoes hard-switching (HS) turn-on. On the other hand, if $i_{A\uparrow} < 0$, Q_A^H undergoes ZVS turn-on while Q_A^L experiences HS turn-off. The first case ($i_{A\uparrow} > 0$) is associated to the power loss contribution $\frac{1}{2} f_s \tau_{on} V_g i_{A\uparrow}$ [65], while the second ($i_{A\uparrow} < 0$) to $\frac{1}{2} f_s \tau_{off} V_g |i_{A\uparrow}|$. Constants τ_{on} and τ_{off} respectively denote the turn-on and turn-off delays of the switches.

As for the high-to-low transition, the case $i_{A\downarrow} > 0$ leads to ZVS turn-on of Q_A^L and HS turn-off of Q_A^H, while $i_{A\downarrow} < 0$ corresponds to HS turn-on of Q_A^L and ZVS turn-off of Q_A^H. The first case leads to total power losses $\frac{1}{2} f_s \tau_{off} V_g i_{A\downarrow}$, while the second scenario to $\frac{1}{2} f_s \tau_{on} V_g |i_{A\downarrow}|$.

Since parasitic output capacitance of a MOSFET is known to strongly mitigate HS turn-off losses, only turn-on losses are considered. This allows to

express the total switching losses for leg A as

$$P_{sw,A} = \frac{1}{2}\tau_{on} f_s V_g \left(\max\left(i_{A\uparrow}, 0\right) + \left|\min\left(i_{A\downarrow}, 0\right)\right|\right). \tag{2.18}$$

By repeating the above reasoning for leg B, one has

$$P_{sw,B} = \frac{1}{2}\tau_{on} f_s V_o \left(\max\left(i_{B\uparrow}, 0\right) + \left|\min\left(i_{B\downarrow}, 0\right)\right|\right), \tag{2.19}$$

and by summing the contributions related to all four switching instants, the total switching loss is expressed as

$$\begin{aligned} P_{sw} = \;& P_{sw,A} + P_{sw,B} \\ = \;& \frac{1}{2}\tau_{on} f_s V_g \left(\max\left(i_{A\uparrow}, 0\right) + \left|\min\left(i_{A\downarrow}, 0\right)\right| + \right. \\ & \left. + M\left(\max\left(i_{B\uparrow}, 0\right) + \left|\min\left(i_{B\downarrow}, 0\right)\right|\right)\right) \quad . \end{aligned} \tag{2.20}$$

To numerically evaluate (2.20), the calculation of $i_{A\uparrow}$, $i_{A\downarrow}$, $i_{B\uparrow}$ and $i_{B\downarrow}$ is performed by considering multiple harmonics. Expression of the k^{th} tank current harmonic is

$$\begin{aligned} i_{T,k}(t) = & \frac{2V_g}{k\pi|Z_T|_k}\sin(k\pi D_A)\cos(k\omega_s t - k\pi D_A - \frac{\pi}{2}) \\ & - \frac{2V_o}{k\pi|Z_T|_k}\sin(k\pi D_B)\cos(k\omega_s t - k\pi D_A - k\phi - \frac{\pi}{2}) \end{aligned} \tag{2.21}$$

where,

$$|Z_T|_k = k\omega_s L_r - \frac{1}{k\omega_s C_r} = \sqrt{\frac{L_r}{C_r}}\left(\frac{k^2 - r^2}{kr}\right) \tag{2.22}$$

In order to gain insight on the switching losses contribution and independently of the devices, the switching losses are further normalized as

$$P_{sw,N} \triangleq \frac{P_{sw}}{\frac{1}{2}\tau_{on} f_s V_g I_{max}}, \tag{2.23}$$

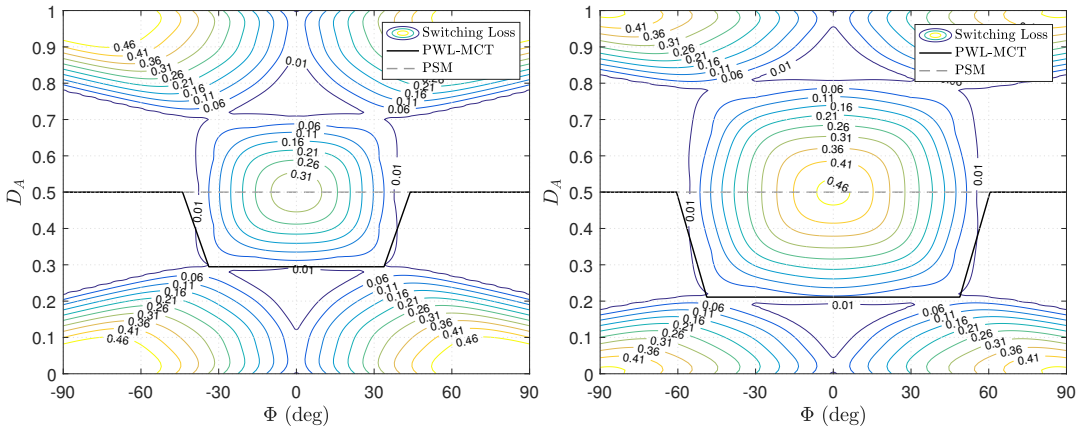


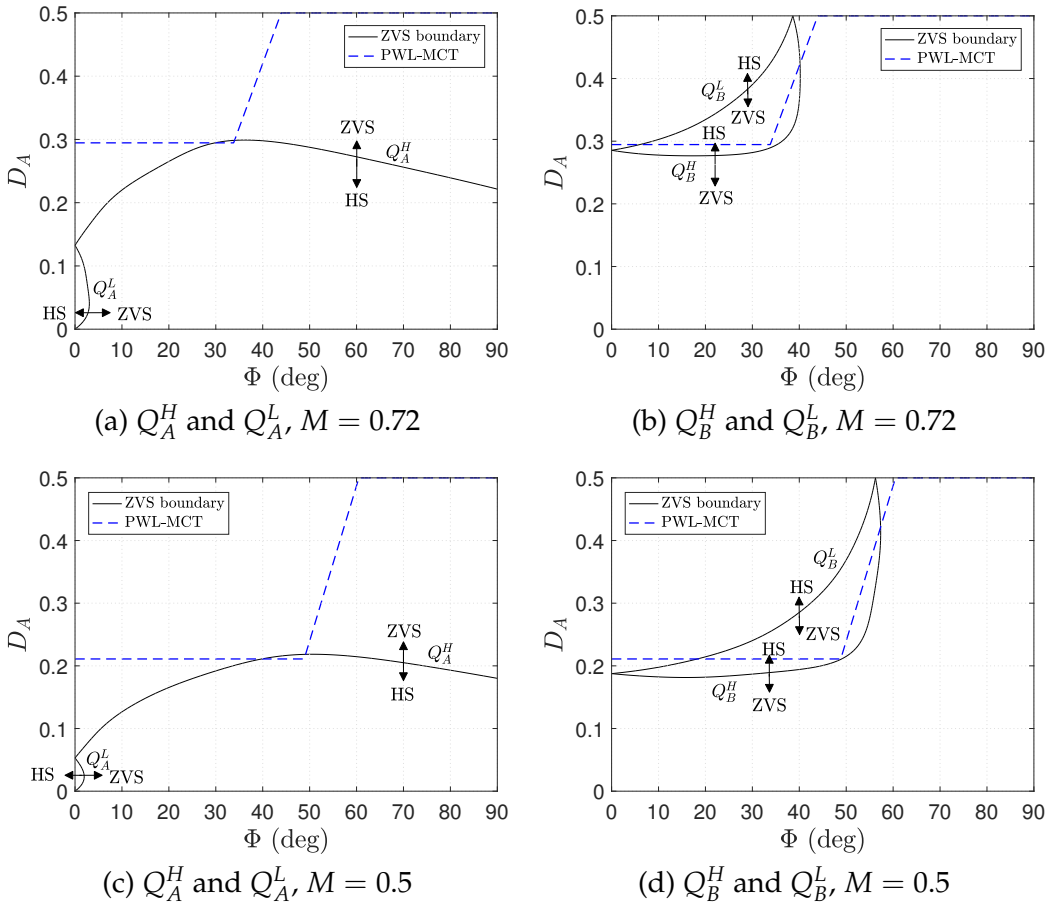
FIGURE 2.11: Contours of normalized switching losses $P_{sw,N}$ on the (D_A,Φ) plane ($D_B = 0.5$) for (a) $M = 0.72$ and (b) $M = 0.5$, with $r = 0.85$ and accounting for harmonics #1 through #10 of the tank current.

where

$$I_{max} \triangleq \sqrt{2} I_{T,max} \tag{2.24}$$

represents the full-power tank current amplitude under the FHA. Fig. 2.11 illustrates the contours of normalized switching losses based on (2.23) considering harmonics #1 through #10 on the $D_B = 0.5$ plane, and for two distinct values of M. The frequency ratio r used here is 0.85 corresponding to the parameter in experimental prototype. Although the switching losses contours change with the input voltage and conversion ratio M, it can be seen that the PWL-MCT is always located in a region of reduced switching losses. Based on Fig. 2.11, a strong mitigation of switching losses is expected along the PWL-MCT compared with PSM.

In order to investigate the switching behavior of each switch along PWL-MCT, ZVS and HS regions on $D_B = 0.5$ plane are determined using current-based ZVS method, i.e. the judgment of soft-switching only depends on the sign of tank current without considering the effects of parasitic switch capacitance [53, 59, 66]. Harmonics #1 through #10 are still superimposed here in order to derive accurate results. Fig. 2.12 shows ZVS and HS regions of all switches on $D_B = 0.5$ plane for $M = 0.72$ and $M = 0.5$ with $r = 0.85$. It



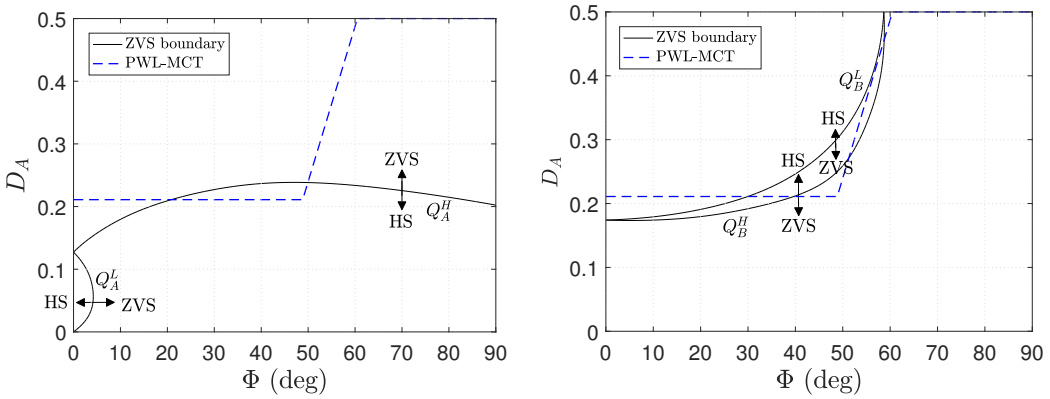
(a) Q_A^H and Q_A^L, $M = 0.72$ (b) Q_B^H and Q_B^L, $M = 0.72$

(c) Q_A^H and Q_A^L, $M = 0.5$ (d) Q_B^H and Q_B^L, $M = 0.5$

FIGURE 2.12: Zero voltage switching (ZVS) and hard switching (HS) regions of all switches on the (D_A,Φ) plane ($D_B = 0.5$) for (a)-(b) $M = 0.72$ and (c)-(d) $M = 0.5$, with $r = 0.85$.

can be seen that along PWL-MCT, the switches Q_A^H, Q_A^L and Q_B^L achieve ZVS for almost all the power range. For Q_B^H, although it operates in HS state at light and medium power levels, the switching losses are apparently mitigated compared with PSM due to the reduced tank current at switching instant.

Fig. 2.13 reports ZVS and HS regions on $D_B = 0.5$ plane for each switches for $M = 0.5$ with $r = 0.95$. Compared to the case $r = 0.85$ in Fig. 2.12c and Fig. 2.12d, it indicates that the ZVS regions of Q_A^H, Q_A^L and Q_B^L tend to narrow down with the increase of r. However, ZVS operation in a wide power range still can be achieved for these three switches. As for Q_B^H, lower switching losses are guaranteed due to the strongly reduced switched current. The analysis confirms that the developed PWL-MCT contributes to



(a) Q_A^H and Q_A^L, $r = 0.95$ (b) Q_B^H and Q_B^L, $r = 0.95$

FIGURE 2.13: Zero voltage switching (ZVS) and hard switching (HS) regions of all switches on the (D_A,Φ) plane ($D_B = 0.5$) for $M = 0.5$ and $r = 0.95$.

TABLE 2.2: Parameters of the experimental prototype

Input Voltage V_g	200 V
Output Voltage V_o	145 V
Maximum Output Power $P_{o_{max}}$	800 W
Switching frequency f_s	48.8 kHz
Resonant frequency f_r	41.3 kHz
Tank inductance L_r	66 µH
Tank capacitance C_r	225 nF
Output capacitance C_o	480 µF
MOSFETs	Infineon CoolMOS™ IPW60R160C6 (650 V, 23.8 A)

eliminate/reduce switching losses, and that these considerations apply quite generally to different resonant tank parameters.

2.6 Experimental Results

A 800 W, 200 V-to-145 V SR-DHB prototype is developed with the specifications listed in Tab. 2.2. In the experimental setup, a 5 kW power supply and a dc electronic load in constant voltage mode are used as V_g or V_o and both input and output power levels are measured. The modulator and the PWL-MCT trajectory controller are VHDL-coded and implemented on a commercial FPGA development board interfaced with the power stage. The power control

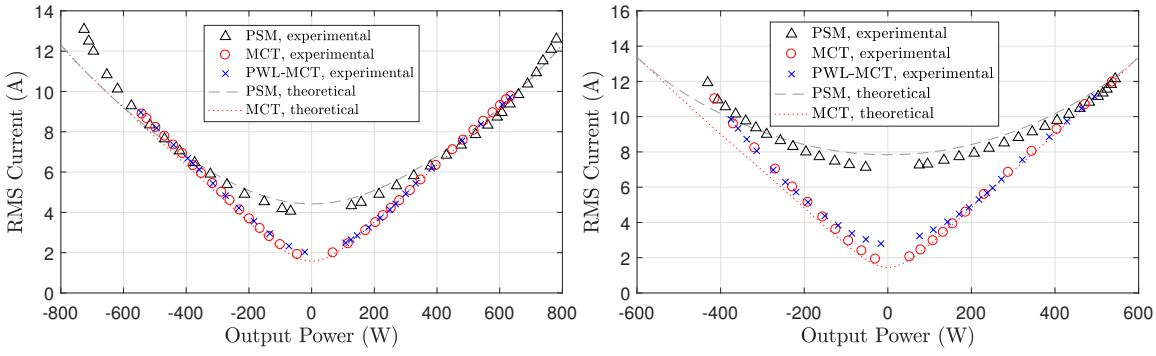
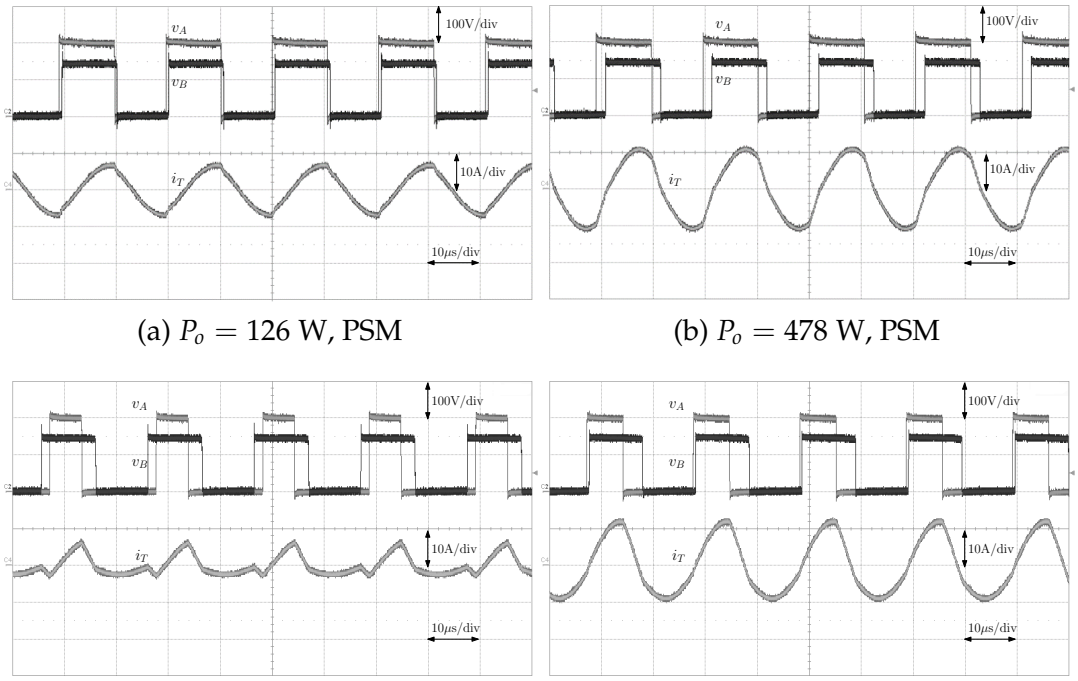


FIGURE 2.14: Experimental tank *rms* current as a function of the output power along PSM, MCT and PWL-MCT, for (a) $M \approx 0.72$, (b) $M = 0.5$.

command u and parameters m, D_{sat} and D_0 used by the PWL-MCT controller are manually entered via a PC-based console. The digital setup also allows a direct programming of both Φ and D_A in order to easily test operating points on the simple PSM trajectory or on the converter true MCT.

In a first test, the steady state *rms* tank current under PSM, MCT and PWL-MCT is measured for $M \approx 0.72$ ($V_g = 200$ V, $V_o = 145$ V) and $M = 0.5$ ($V_g = 200$ V, $V_o = 100$ V) and respectively reported in Fig. 2.14a and 2.14b. The *rms* current along both MCT and PWL-MCT is evidently decreased in the light power condition with respect to PSM. Although minor differences can be observed in very light load due to the approximation error, the experimental results still strongly indicate good consistency between MCT and PWL-MCT. At the same time, it shows that the experimental results well agree with the theoretical analysis along MCT and PSM for at light and medium power levels.

Fig. 2.15 and Fig. 2.16 exemplify the steady-state waveforms of the tank current and the switching node voltages on both PSM and PWL-MCT for different power levels and voltage conversion ratios. It can be seen that the circulating current is significantly reduced when the converter operating on PWL-MCT, especially at light load. For instance, in Fig. 2.15a, the tank *rms* current with PSM amounts to approximately 4.33 A, while it reduces to



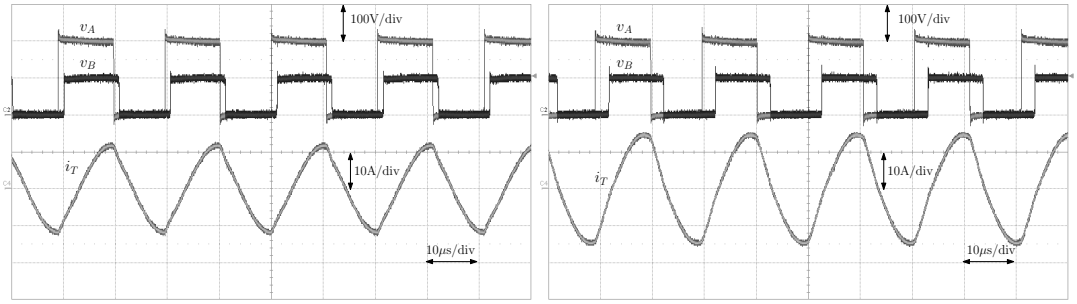
(a) $P_o = 126$ W, PSM (b) $P_o = 478$ W, PSM

(c) $P_o = 126$ W, PWL-MCT (d) $P_o = 478$ W, PWL-MCT

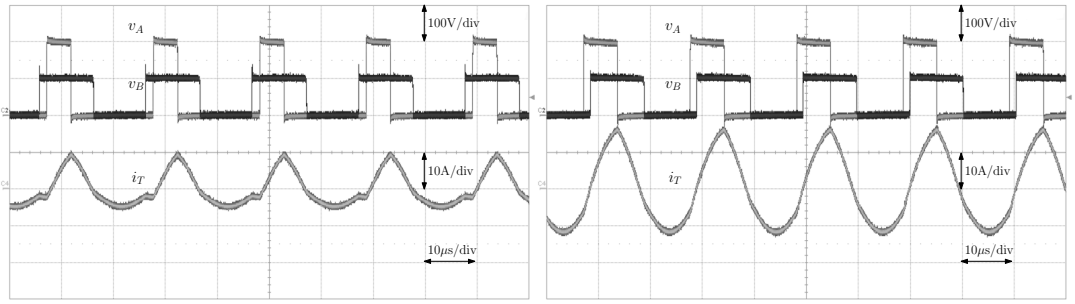
FIGURE 2.15: Tank current and switching node voltages at $M \approx 0.72$ ($V_g = 200$ V, $V_o = 145$ V) for $P_o = 126$ W and $P_o = 478$ W: (a)-(b) phase shift modulation, and (c)-(d) proposed PWL-MCT approach. Time scale 10 μs/div; voltage scale 100 V/div; current scale 10 A/div.

2.44 A on the PWL-MCT as shown in Fig. 2.15c. Notice that, as anticipated in section 2.5, the strong reduction in the *rms* current has the beneficial side effect of reducing the instantaneous current at the switching instants, mitigating hard-switching transition losses. In Fig. 2.16a, for instance, severe hard-switching occurs at both low-to-high and high-to-low transitions of leg B. In Fig. 2.16c, on the other hand, rising transition of v_B occurs at a tank current close to zero, while the falling transition occurs at a negative tank current, therefore only a mild hard-switching transient is observed.

Detailed switching behavior on the PWL-MCT are tested at operating point ($D_A = 0.295, \Phi = 20°$) at a power level of 300 W and $M \approx 0.72$ ($V_g = 200$ V, $V_o = 145$ V). Fig. 2.17 reports the switching nodes and gate-to-source voltages together with tank current for each switch. It can be seen that ZVS turn-on is achieved for Q_A^H, Q_A^L and Q_B^L. As for Q_B^H, Fig.2.17c illustrates how the



(a) $P_o = 170$ W, PSM (b) $P_o = 431$ W, PSM

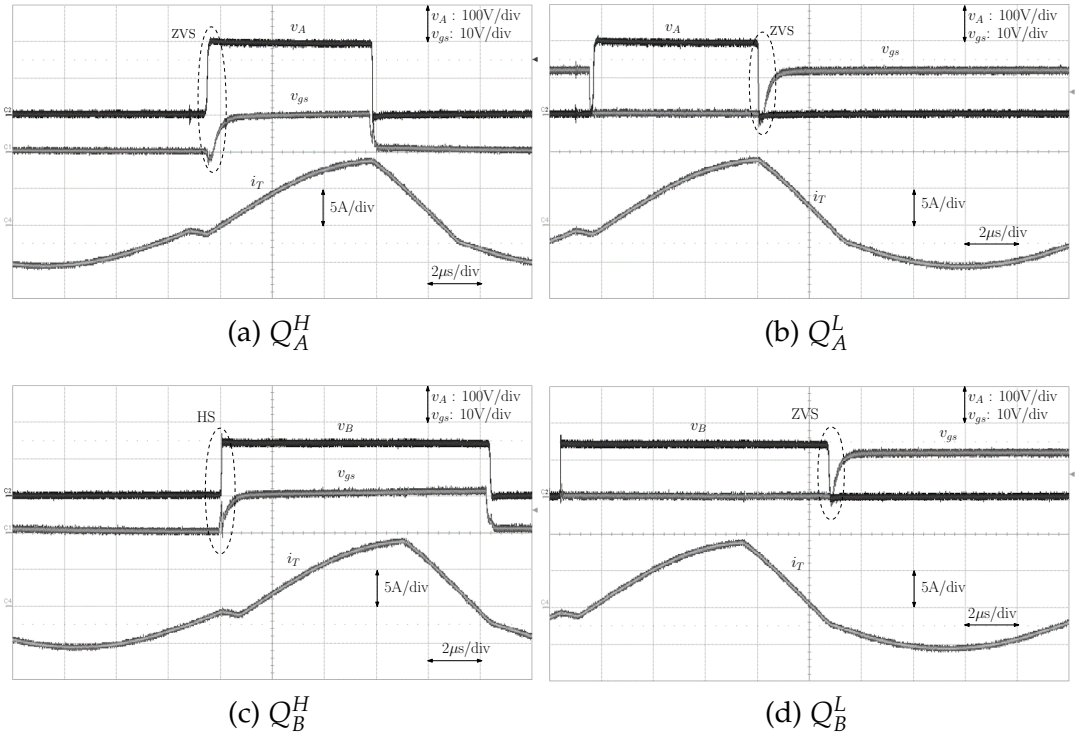


(c) $P_o = 170$ W, PWL-MCT (d) $P_o = 431$ W, PWL-MCT

FIGURE 2.16: Tank current and switching node voltages at $M = 0.5$ ($V_g = 200$ V, $V_o = 100$ V) for $P_o = 170$ W and $P_o = 431$ W: (a)-(b) phase shift modulation, and (c)-(d) proposed PWL-MCT approach. Time scale 10 μs/div; voltage scale 100 V/div; current scale 10 A/div.

corresponding switched current at the turn-on instant is close to zero, strongly mitigating the hard switching transition losses. Such experimental results are entirely consistent with the discussion developed in section 2.5 and with the corresponding plots of Fig. 2.12.

Efficiency tests along PSM, MCT and PWL-MCT are experimentally performed at the nominal voltage conversion ratio $M \approx 0.72$ ($V_g = 200$ V, $V_o = 145$ V) and $M = 0.5$ ($V_g = 200$ V, $V_o = 100$ V). Experimental test points are taken in both forward and reverse power flow, and are depicted in Fig. 2.18a and Fig. 2.18b for the various trajectories. The experimental efficiencies as a function of the output power are compared in Fig. 2.18c and 2.18d and the corresponding power losses are reported in Fig. 2.18e and 2.18f: effectiveness of the PWL-MCT approach is confirmed by the marked efficiency improvement and reduced power loss visible in the light and medium load.



(a) Q_A^H (b) Q_A^L

(c) Q_B^H (d) Q_B^L

FIGURE 2.17: Switching nodes and gate-to-source voltages and tank current at $M \approx 0.72$ ($V_g = 200$ V, $V_o = 145$ V) and for $P_o = 300$ W along the PWL-MCT trajectory. Time scale 2 μs/div; voltage scale: switching node 100 V/div, gate-to-source 10 V/div; current scale 5 A/div.

Although some degree of efficiency drop on the PWL-MCT is seen at very light load compared with MCT, the efficiency is still strongly enhanced compared with PSM. The beneficial effect of PWL-MCT control on total power losses is explicitly illustrated in Fig. 2.18e and 2.18f for the two considered cases $M = 0.72$ and $M = 0.5$: as seen in the comparison with PSM, the proposed PWL-MCT trajectory controller based on *rms* current minimization allows power losses to scale with the load and approach zero as the load decreases. From Fig. 2.18f, for instance, the total power saving approaches or exceeds 70 W in the $|P_o| < 200$ W power range.

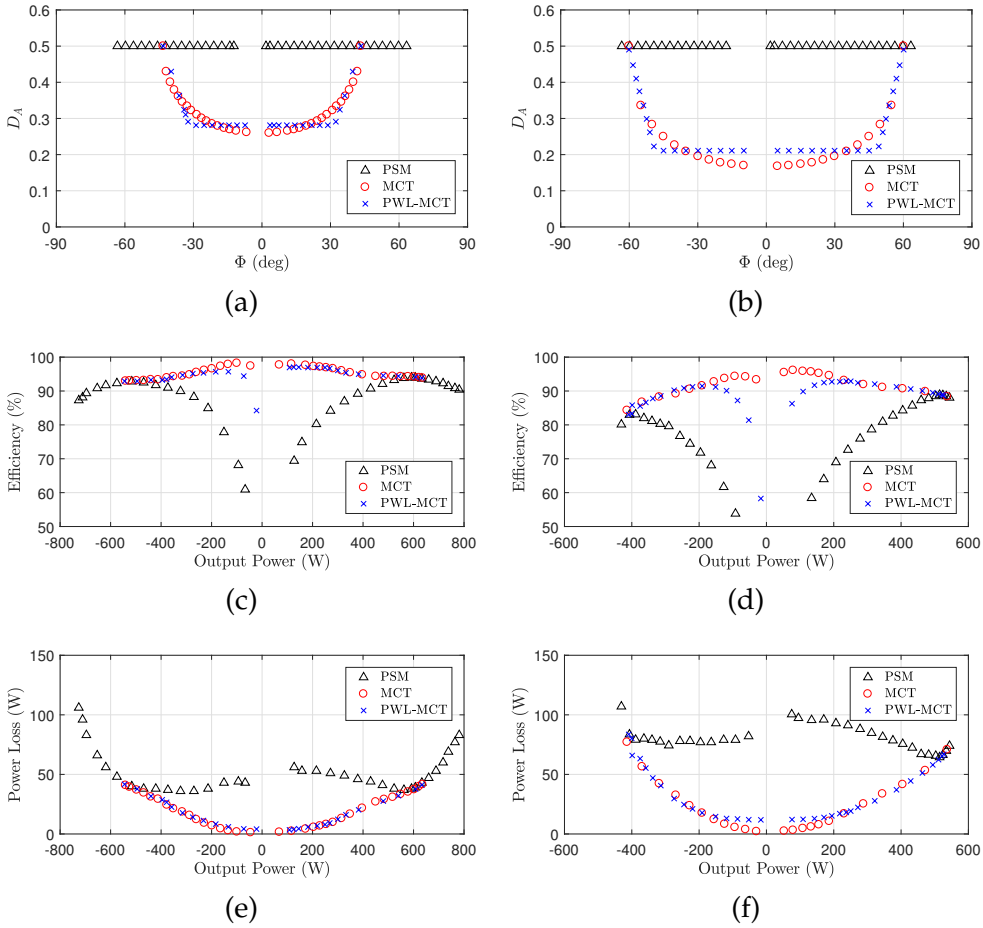


FIGURE 2.18: (Top) Experimental test points in the (D_A,Φ) plane, (middle) corresponding experimental efficiency and (bottom) power losses, for (a)-(c)-(e) $M \approx 0.72$ and (b)-(d)-(f) $M = 0.5$.

2.7 Conclusion and Summary of Contribution

Bidirectional power transfer is a main topic of automotive power conversion. Dual-half bridge converters are of interest because of their reduce component size, while resonant power processors achieve ZVS over a wide range. Moreover the series capacitor acts as first failure short circuit prevention. The main drawback of resonant converters are the conduction losses, which usually are higher with respect to the non-resonant counterpart. Conduction losses optimization is a known topic for full-bridge converters, where modulation degrees of freedom are exploited.

In this work a low-complexity trajectory controller for reduced conduction losses is proposed for SR-DHB converter topologies. The proposed modulation approximates the minimum current trajectory of the converter with a piecewise-linear one, achieving a near-optimal minimization of the tank *rms* current at any power level. The proposed implementation makes use of standard digital arithmetic operations, and can be realized either on low-cost microcontrollers, or inside custom-designed integrated circuits, depending on the application requirements. Furthermore, the proposed controller can be formulated independently of the resonant converter passive parameters, resulting in a robust approach of broad applicability for the topology under consideration. The technique also easily accommodates for wide-range variations of the converter voltage conversion ratio, which can be handled via input/output voltage sensing.

The main improvement with respect to PSM is achieved at intermediate-to-light load: at 100 W the efficiency increases from 68% to almost 90%. Even if the peak current is not predicted very well by the first harmonic only, the RMS value can be approximated quite well through the FHA, especially at heavy load. There is a small difference located at low $P_{o,N}$, where the THD value is very high because of the small D_A value.

Chapter 3

Online Efficiency Optimization of Dual Half-Bridge Converter

3.1 Introduction

As mentioned switching dc-dc converters are replacing the linear one also in the conventional 12 V-to-5 V application. Switching converters yield higher heavy load efficiency, but at light-load linear converters still can be preferable. The main idea developed in this chapter is to increase the efficiency by acting on modulation degrees of freedom during converter operation. In this way the optimization is obtained regardless the operating point or the component value. The dual half bridge topology (DHB, Fig.3.1, [67]) requires four switches and offers at least three degrees of freedom: the duty cycle of the leg A, D_A, the duty cycle of the leg B, D_B, and the phase shift Φ between the switching node voltages. Automotive point of load converters require integrated solution and small-valued inductors, thus motivating the selection of this topology.

The DHB converter is based on two half bridges linked by an impedance which can be an inductor or a resonant tank, i.e. the non resonant DHB (NR-DHB) and the series resonant DHB (SR-DHB), described in details in chapter 2. The main difference between these two versions of the DHB converter is the average impedance current, which is zero in the SR-DHB.

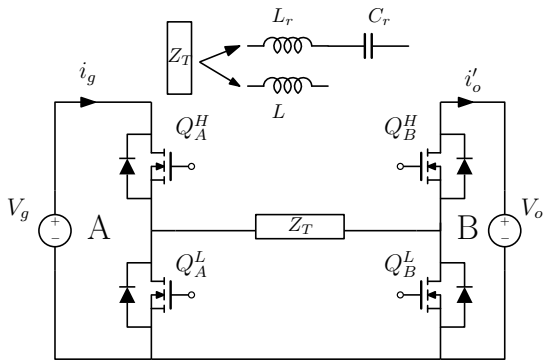


FIGURE 3.1: General Dual Half Bridge (DHB) Topology

TABLE 3.1: Parameters of the DHB Case Study

Switching frequency f_s	196 kHz
Input Voltage V_g	12 V
Output Voltage V_o	5 V
Inductance L	1.96 µH
Output Capacitance C_o	110 µF
Inductor Parasitic Resistance R_L	196 mΩ
MOSFET Parasitic Resistance $R_{ds,on}$	3.6 mΩ
Maximum Output Current $I_{o_{max}}$	2 A

This chapter is the continuation of the work made by Luca Scandola during a joint Ph.D. program between the University of Padova and Infineon Technologies S.r.l.. His results [68] has been extended and presented at the Workshop on Control and Modeling for Power Electronics [69].

3.1.1 Modulation Techniques in the Converter Optimization Plane

With two independently controlled half-bridges, the DHB topology offers several degrees of freedom to be exploited for modulation purposes. Fig. 3.2, for instance, exemplifies the use of the duty cycle D_A and D_B of the two legs and the mutual phase shift ϕ as three possible modulation variables. Note that the conversion ratio of the converter is $M = D_A/D_B$ and does not depend on ϕ. In the control strategy here considered, duty cycle D_A is used to regulate the output voltage, whereas D_B and ϕ become degrees

of freedom used to improve efficiency, as depicted in Fig. 3.4. The (D_B, ϕ) space therefore represents the *optimization plane* available to the controller to optimize efficiency. Objective of this section is to discuss the converter efficiency over the optimization plane. For this reason both experimental and approximate numerical results are reported and discussed in order to gain insight on the efficiency behavior of the DHB converter.

For a given power level P_o, any (D_B, ϕ) combination is allowed: different (D_B, ϕ) combinations provide the same output power but with a different inductor current waveform and hence a different efficiency. More precisely, according to the relative positions of the gate driving signals of legs A and B, the optimization plane (D_B, ϕ) can be divided into the five regions illustrated in Fig. 3.3, with a distinct inductor current waveform corresponding to each region. The example waveforms in Fig. 3.2, for instance, refer to region R_3. Furthermore, it is easy to see that the boundary line equations depend on the transfer ratio M only, and are defined by the four equations reported in Fig. 3.3. The power converter *efficiency contours*, i.e. curves of constant efficiency, are reported on the optimization plane in Fig. 3.5a and 3.5b for $P_o = 2.1$ W and 6.6 W respectively. Such plots have been experimentally determined by measuring the efficiency at various (D_B, ϕ) combinations while maintaining the output voltage fixed at 5 V.

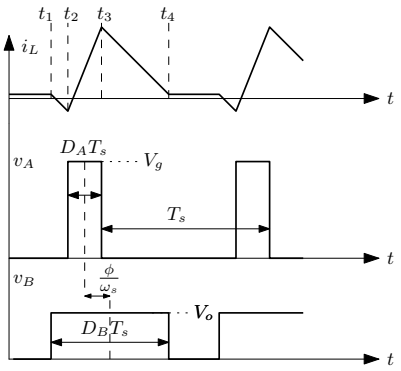


FIGURE 3.2: Example of switching node voltages and inductor current for a generic (D_A, D_B, ϕ) combination.

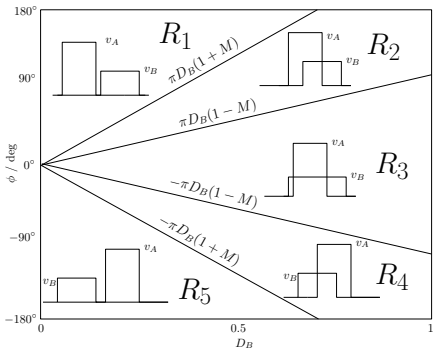


FIGURE 3.3: Modulation regions in the optimization plane.

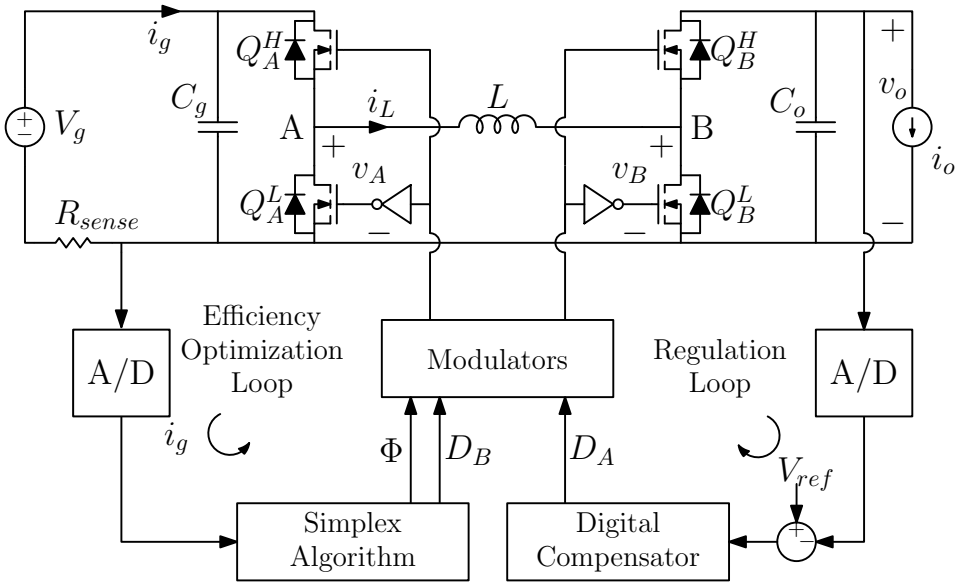


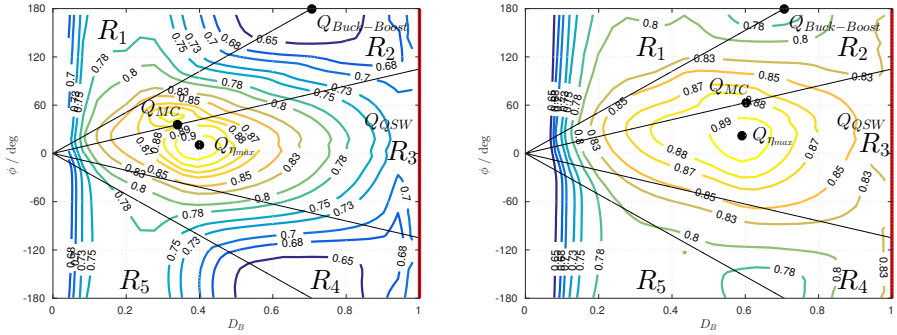
FIGURE 3.4: Dual Active Bridge converter with the proposed two-dimensional online efficiency optimization loop.

Each power level generates a different pattern of efficiency contours on the optimization plane.

Furthermore, the efficiency maximum point $Q_{\eta max}$ occurs inside region R_3, in which the inductor current waveform resembles the one depicted in Fig. 3.2.

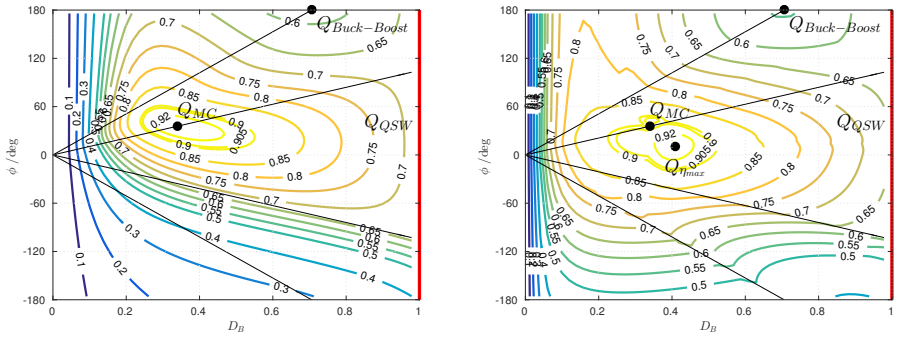
Simplified Model for Efficiency Calculations

A simplified numerical model for the converter losses is adopted in the following to interpret the efficiency patterns but no preliminary efficiency characterization is required by the simplex-based optimization approach which will be



(a) (b)

FIGURE 3.5: Experimental efficiency contours on the optimization plane for $P_o = 2.1$ W (a) and $P_o = 6.6$ W (b).



(a) (b)

FIGURE 3.6: Numerically estimated efficiency contours on the optimization plane for $P_o = 2.1$ W with the approximated efficiency model: (a) conduction losses only, and (b) by incorporating switching losses.

described in section 3.1.2. The efficiency contours and efficiency model are here only reported as a support to the conceptual justification of the method.

In the model, conduction losses are simply described by a single parasitic resistance $R_{par} \triangleq R_L + 2R_{ds,on}$ placed in series with the DHB inductor, which accounts for both the parasitic inductor resistance and the transistors on-resistance $R_{ds,on}$. To produce the efficiency contour of a given P_o, the inductor *rms* current is calculated for each (D_B, ϕ) and multiplied by R_{par}. The constant efficiency contours resulting from conduction losses only is illustrated in Fig. 3.6a for $P_o = 2.1$ W.

To further refine the model, an approximate account of the switching losses

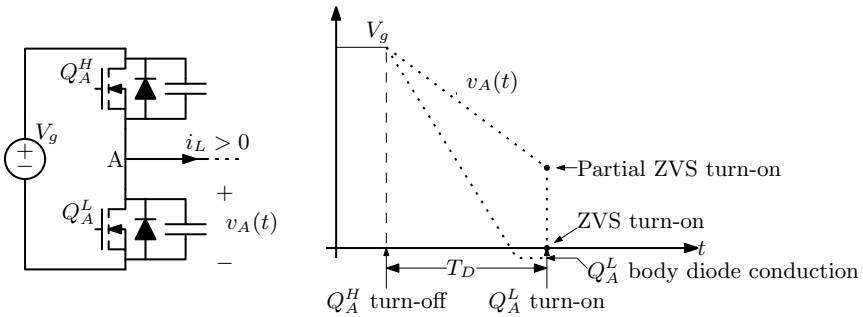


FIGURE 3.7: Switching loss mechanisms accounted by the approximate numerical model: partial ZVS turn-on and body diode conduction loss at full ZVS turn-on (Q_A^L turn-on example).

is also included, based on the modeling framework discussed in [70]. In [70] the switching losses due to the devices output capacitances of the single leg are modeled under no load condition – i.e. zero commutated current – and only hard switching is considered as an additional loss mechanism. This model has been extended by numerically including *partial* zero voltage switching losses and diode forward conduction losses. In reference to Fig. 3.7, which exemplifies the situation relative to Q_A^L turn-on after a dead time T_D, the two contributions can be described as follows:

- Partial ZVS losses arise when zero voltage is not fully achieved at the device turn-on due to an incomplete transition of the switching node voltage during the dead time. Such condition causes a partial energy loss at device turn-on, which depends on the value of the switching node voltage at the device turn-on instant, and which can be accounted for in an approximate fashion by extending the metodology disclosed in [70].

- The second contribution simply accounts for the body diode conduction losses occurring in transitions involving full-ZVS turn-on and a consequent generation of a free-wheeling subinterval within the dead time.

In the numerical model, the inductor current value at the switching instants t_1, t_2, t_3, t_4 (Fig. 3.2) is evaluated. Depending on sign and magnitude of the current, losses due to hard switching, partial zero voltage switching or body diode conduction are evaluated.

The efficiency contour predicted by the model is shown in Fig. 3.6b for $P_o = 2.1$ W. Comparison with Fig. 3.5a, which refers to the same power level, reveals that efficiency contours in region R_3, and in particular the maximum efficiency point position, are rather well approximated. On the other hand, the model accuracy is limited where hard switching with high inductor current occurs. The remaining subsection have the purpose of discussing a few relevant modulation techniques which can be identified in the (D_B, ϕ) optimization plane, and relate them to the experimental and numerical efficiency contours reported in Fig. 3.5 and 3.6.

Buck-Boost Modulation

In the Buck-Boost modulation the DHB converter is treated as a non-inverting Buck-Boost topology, and the two legs are driven in a complementary way so that $D_B = 1 - D_A$ and $\phi = \pi$. The voltage conversion ratio becomes $M = D_A/(1 - D_A)$, hence $D_B = 1/(1 + M)$, which evaluates to $\simeq 0.71$ in the case study here considered. The corresponding point in the (D_B, ϕ) optimization plane is denoted in Fig. 3.5 as $Q_{Buck\text{-}Boost}$ and is located on the boundary between regions R_1 and R_2 at $\phi = \pi$.

Quasi Square Wave (QSW) Buck Modulation

A DHB converter using a low-inductance design can also be controlled so as to emulate a Quasi Square Wave (QSW) Buck by modulating leg A while keeping leg B fixed at $D_B = 1$. In Fig. 3.5a this modulation is represented by the vertical segment Q_{QSW} defined by $D_B = 1$: Since $v_B(t)$ is constant, the value of ϕ becomes irrelevant and all the $D_B = 1$ points correspond to the

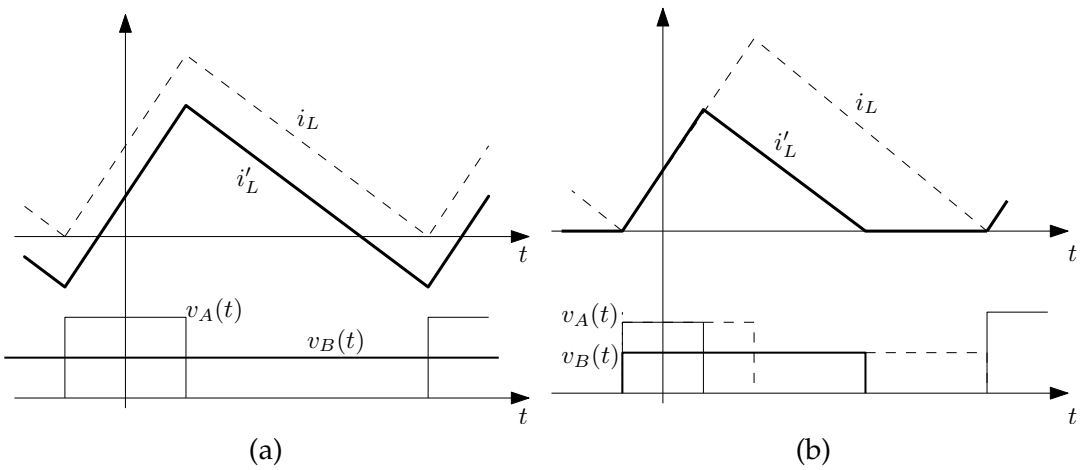


FIGURE 3.8: Inductor current waveforms in heavy and light-load: (a) QSW Buck modulation and (b) minimum current modulation.

same physical situation. The inductor current waveform in QSW Buck mode is shown in Fig. 3.8a. As long as the inductor current remains negative at its valley point, ZVS turn-on of both Q_A^H and Q_A^L is achieved, which is the major advantage of the QSW modulation.

This type of modulation, in which one of the DHB legs does not switch, is only useful in those situations where expected input voltage variations are large enough to induce both step-down and step-up scenarios. In this case the QSW modulation can alternatively be applied to the output leg (the Buck mode just described) or to the input leg (Boost mode), according to the input voltage level.

In synchronous Buck converters, QSW modulation is known to be an extremely heavy-load efficient modulation technique due to the reduced switching losses. When adopted in DHB converters, QSW modulation will result in a somewhat smaller efficiency because of the additional conduction losses due to Q_B^H being permanently on.

The efficiency of this modulation strategy is nonetheless typically higher than the simple Buck-Boost mode. This fact is confirmed by the experimental results of Fig. 3.5a and by the numerical prediction of Fig. 3.6a and 3.6b.

Notice, on the other hand, that the efficiency in QSW mode remains

nonetheless quite smaller than the maximum efficiency point. This is especially true in light load operation, where the advantage of reduced switching losses due to the ZVS mechanism is largely offset by the increasing weight of the conduction losses associated with the large inductor current ripple.

Minimum-Current Modulation (MCM)

A different strategy is to choose (D_B, ϕ) in order to minimize the circulating *rms* current through the inductor. Intuitively speaking, the minimum-current waveform minimizes the amount of *circulating current*, i.e. current flowing through the inductor but not delivered to the load. It can be verified that the waveform depicted in Fig. 3.8b satisfies such constraint with zero circulating current, and therefore represents the minimum current waveform.

The above considerations can be proven analytically. More specifically it can be shown that, for

$$P_o < P_{o,max} \triangleq \frac{V_o^2}{2 f_s L}(1 - M), \tag{3.1}$$

the (D_B, ϕ) operating point which minimizes the *rms* inductor always lies on the boundary between regions R_2 and R_3,

$$\phi = \pi D_B (1 - M), \tag{3.2}$$

and is given by

$$\begin{aligned} D_{B_{rms,min}} &= \sqrt{P_N} \\ \phi_{rms,min} &= \pi \left(1 - M\right) \sqrt{P_N}, \end{aligned} \tag{3.3}$$

where $P_N = P_o / P_{o,max}$ is the normalized output power. This is confirmed by Fig. 3.6a, in which the efficiency peak, when calculated using the simplified efficiency model and neglecting switching losses contributions, indeed lies on the boundary line.

As suggested by (3.3) and by Fig. 3.5, the minimum current point moves towards the $D_B = 1$ boundary of the optimization plane as the power level increases, reaching $D_B = 1$ for $P_o = P_{o,max}$. From this point on the converter operates in QSW mode ($D_B = 1$), and no degrees of freedom are left to further optimize the inductor *rms* current, which is solely determined by the power level. In the prototype characterized by the values of Tab. 3.1, $P_{o,max} \approx 18.6$ W and such limit lies above the converter nominal power rating.

Discussion

The true efficiency peak of the power converter, as determined experimentally in Fig. 3.5 and numerically predicted in Fig. 3.6b using an approximate model, is not achieved by any of the modulation strategies outlined so far. Among these, the minimum current modulation is certainly the one which better approximates the maximum efficiency point. Nonetheless, the true efficiency peak is not located on the minimum inductor *rms* current line because maximum efficiency is necessarily achieved through a balance of conduction and switching losses, while the MCM modulation outlined in section 3.1.1 only minimizes the former contribution.

Predicting the complex balance between conduction and switching losses at the maximum efficiency point would require a very accurate model of the switching mechanism, and/or a preliminary characterization of the power converter efficiency for a significant set of output power levels. Furthermore, an implementation of any optimization algorithm based on analytical models would necessarily involve large look-up tables to be pre-stored, if simplified trajectories cannot be found.

For these reasons, the approach followed in this work is an adaptive one, in which an online search on the (D_B, ϕ) plane is undertaken dynamically using an online optimization algorithm known as *simplex*. By restricting the simplex search to region R_3 only, the existence of a single maximum efficiency point is

guaranteed. Furthermore, such algorithm does not require any preliminary efficiency characterization of the power converter nor the development of accurate switching losses models.

3.1.2 Simplex Algorithm for Online Efficiency Optimization

The simplex method was first introduced in [71] as an algorithm used to find the minimum of a mathematical function of n variables without involving the calculation of derivatives. More recently, the simplex algorithm has been employed as a two-dimensional MPPT tracking system in energy harvesting scenarios [72].

The approach is based on the evaluation of the function to be minimized in $n+1$ points of its domain, i.e. a n-dimensional simplex. According to the value assumed by the function, a new simplex point is chosen, the function is there re-evaluated and the simplex updated accordingly.

The simplex algorithm is here implemented digitally as a finite state machine (FSM). The input of the FSM is the DHB input current I_g and its output a point (D_B, ϕ) in the optimization plane. In this two-dimensional minimization problem, the simplex is a triangle. The set point (D_B, ϕ) given by the FSM, along with D_A provided by the output voltage regulator, are fed to the modulator which produces the gate commands, as shown in Fig. 3.4. In Fig. 3.9 the flowchart of the algorithm is sketched. The FSM is clocked with a period long enough to guarantee that the converter reaches its steady-state before the next clock event.

Algorithm Description

At the beginning of each cycle the simplex is defined by three points $Q_1 = (D_{B_1}, \phi_1)$, $Q_2 = (D_{B_2}, \phi_2)$, $Q_3 = (D_{B_3}, \phi_3)$. Each cycle starts by measuring I_g at each point. Next, the three measured points are then classified as Q_{best},

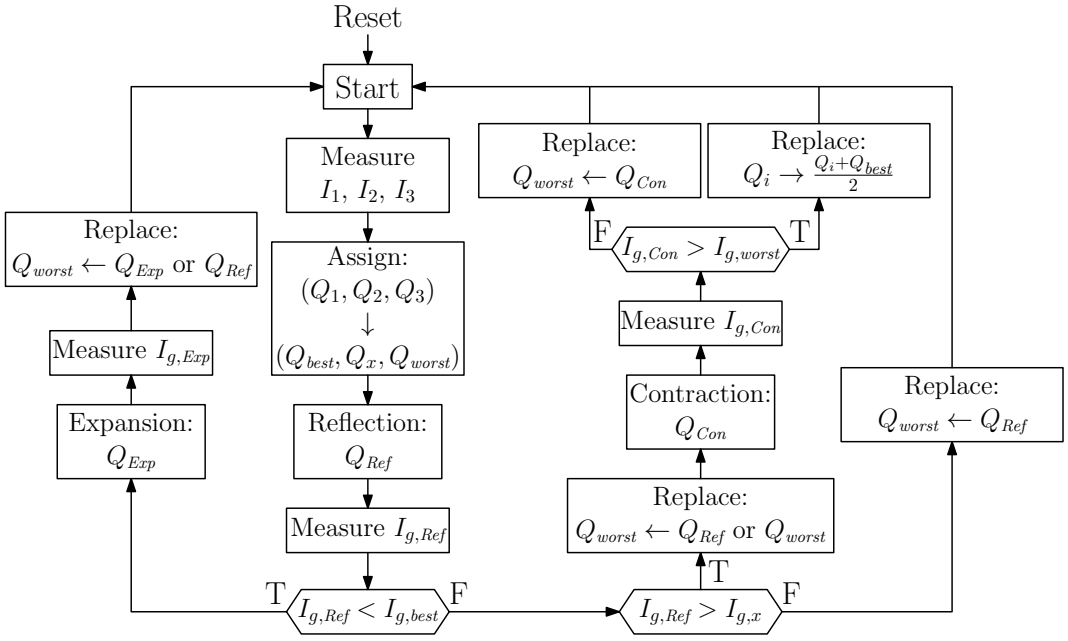


FIGURE 3.9: Flowchart of the simplex algorithm employed for efficiency optimization

associated with the minimum input current $I_{g,best}$, Q_{worst}, associated to the highest input current $I_{g,worst}$, and Q_x indicating the remaining point associated to the intermediate current $I_{g,x}$. Furthermore, the *centroid* $\bar{Q}$ of Q_{best} and Q_x is evaluated as $\bar{Q} \triangleq (Q_{best} + Q_x)/2$.

The simplex algorithm revolves around three types of manipulation of the simplex triangle: *reflection*, *expansion* and *contraction*. At each cycle, after the three operating points are measured and classified, the algorithm enters the *reflection* state:

Reflection

A new point Q_{Ref} is calculated by reflecting Q_{worst} with respect to $\bar{Q}$ through the operation

$$Q_{Ref} = 2\bar{Q} - Q_{worst}. \tag{3.4}$$

Next, current $I_{g,Ref}$ is sampled and evaluated. If $I_{g,Ref} < I_{g,best}$ the direction of the reflection is heading towards a higher efficiency region, and an *expansion* is performed next. If $I_{g,Ref} > I_{g,x}$, a *contraction* operation is performed. Otherwise, the simplex point corresponding to Q_{worst} is discarded and replaced with Q_{Ref},

and the measurement of the current associated with the simplex vertices is reiterated.

Expansion

If the reflection has produced a new minimum, a new point Q_{Exp} is calculated as

$$Q_{Exp} = 2Q_{Ref} + \bar{Q}. \tag{3.5}$$

Next, simplex point corresponding to Q_{worst} is discarded and replaced by either Q_{Exp} or Q_{Ref}, according to whether $I_{g,Exp}$ is smaller or larger than $I_{g,Ref}$. In other words, the highest efficiency point between Q_{Exp} or Q_{Ref} is chosen to substitute Q_{worst}. At this point the simplex cycle restarts.

Contraction

If $I_{g,Ref} > I_{g,x}$, point Q_{worst} is first reassigned as the best among Q_{worst} and Q_{Ref}. Next, a new point Q_{Con} is calculated as

$$Q_{Con} = \frac{1}{2}Q_{worst} + \frac{1}{2}\bar{Q} \tag{3.6}$$

and the current $I_{g,Con}$ is measured. If $I_{g,Con} < I_{g,worst}$, then the simplex point corresponding to Q_{worst} is discarded and replaced by Q_{Con}. If, on the other hand, $I_{g,Con} > I_{g,worst}$, the dimension of the simplex is reduced by replacing all its points Q_i by $(Q_i + Q_{best})/2$. This step is performed because such condition probably indicates the existence of an efficiency peak inside the simplex area. At the end of the contraction step, the simplex cycle restarts.

3.1.3 Experimental Results

A DHB converter with specification reported in Tab. 3.1 is prototyped and experimentally tested. Both the digital compensator and the simplex-based optimizer are VHDL-coded into a hardwired digital controller. An Altera Cyclone-II FPGA commercial development board is chosen as the digital

control platform. The total number of FPGA logic elements required by the design is about 4,900. The DHB converter employs Infineon OptiMOS®3 IPD036N04L-G power MOSFETs and a SMT inductor by Coilcraft of the DO3361P series. The inductor parasitic resistance R_L indicated in Tab. 3.1 includes the contribution of the winding ac resistance, separately measured at a test frequency of 196 kHz.

The compensation is implemented by a digital PID regulator designed to achieve a crossover frequency in the range of a few kHz over the majority of the (D_B, ϕ) range spanned by the simplex search. As for the simplex FSM, it is clocked at about 24 Hz, which is also the sampling frequency of the input current. Observe that, although a dedicated A/D converter is employed in the prototype, sampling of I_g can easily be time-multiplexed with that of the output voltage, therefore employing a single A/D converter for both voltage and current sensing.

To exemplify the simplex operation, consider Fig. 3.10. The simplex is initialized at operating points Q_1-Q_3, and the simplex FSM is successively enabled. The initial simplex points are intentionally selected far away from the efficiency optimum in order to assess the robustness of the simplex convergence process. Initial efficiency at Q_1 is $\eta(Q_1) = 71.8\%$, while the converter power level is 2.1 W.

Switching nodes and inductor current waveform are shown in Fig. 3.11a and Fig. 3.11b respectively before and after the optimization process. The final operating point $Q_{\eta max}$, also reported in Fig. 3.10, is correctly located at the efficiency peak with $\eta(Q_{\eta max}) = 90.9\%$. Notice that in Fig. 3.11b soft switching at turn-on is only achieved for devices Q_A^H, Q_A^L and Q_B^H, whereas turn-on of Q_B^L undergoes a hard transition: The optimization process inherently converges to the best balance between conduction and switching losses. An AC-coupled acquisition of the output voltage during the simplex optimization is shown in Fig. 3.12, while Fig. 3.13 reports the experimental input current, as acquired by

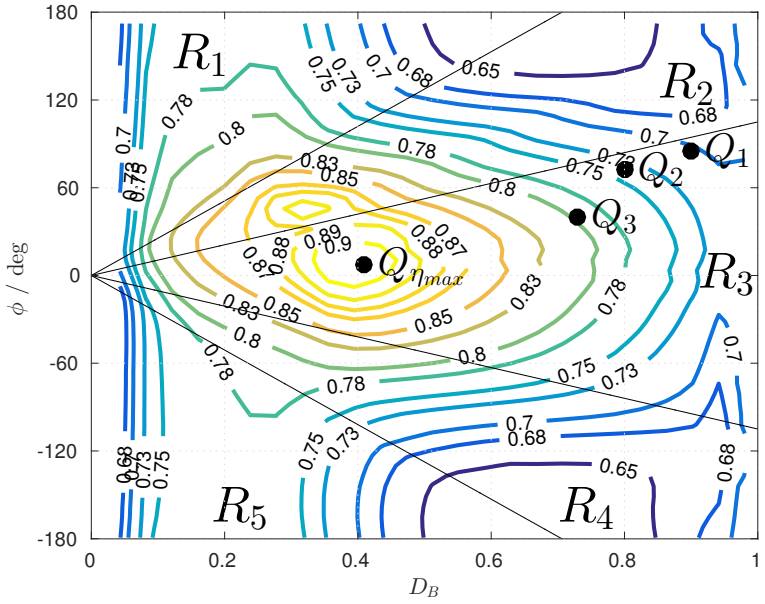
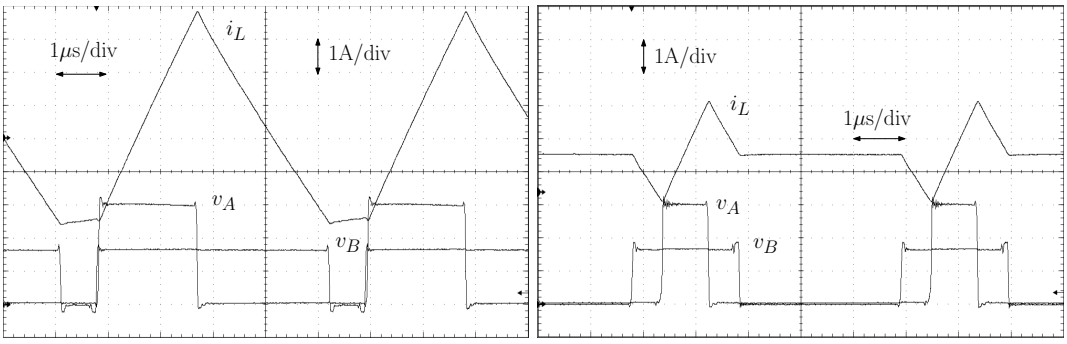


FIGURE 3.10: Simplex algorithm starting and ending points superimposed to the experimental efficiency contours for $P_o = 2.1$ W.



(a) (b)

FIGURE 3.11: Experimental converter waveforms (a) before optimization (point Q_1) and (b) after optimization (Point $Q_{\eta,max}$).

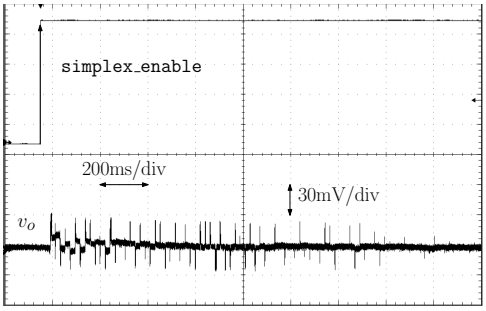


FIGURE 3.12: Experimental converter output voltage during simplex optimization, $P_o = 2.1$ W. Initial and end points are reported in Fig. 3.10.

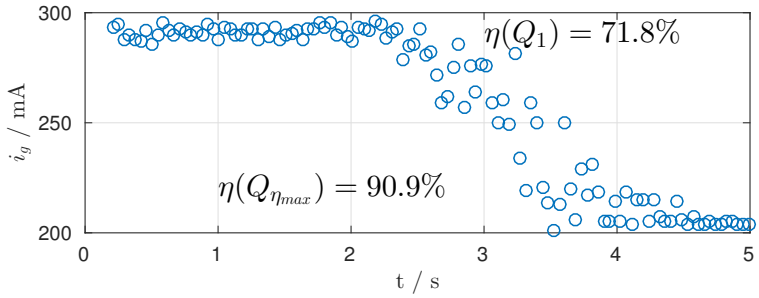


FIGURE 3.13: Experimental A/D converted input current during simplex optimization for $P_o = 2.1$ W.

the A/D converter and reconverted in mA, during the same optimization process. The output voltage perturbation due to the simplex operation is limited to a few tens of millivolts around the regulated value while the input current is minimized to the optimum value. Specific provisions undertaken to limit the sensitivity of the output voltage against simplex-induced disturbances are reported in section 3.1.5.

Fig. 3.14 reports the experimental converter efficiency of the simplex-optimized converter in comparison with the same topology modulated using the QSW Buck modulation discussed in section 3.1.1. Efficiency measurements do not include gate driving losses. The online optimization approach maintains the converter efficiency almost flat over the entire operating range. The QSW Buck modulation mode, on the other hand, leads to high efficiency in heavy load conditions, while a degraded efficiency is achieved at intermediate and light load levels because of the fixed inductor current shape and the consequent increasing weight of ripple-induced conduction losses. On

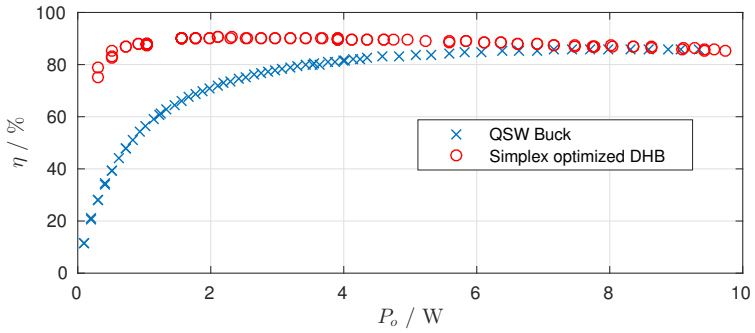


FIGURE 3.14: Experimental efficiency: comparison between simplex-optimized efficiency and QSW Buck modulation.

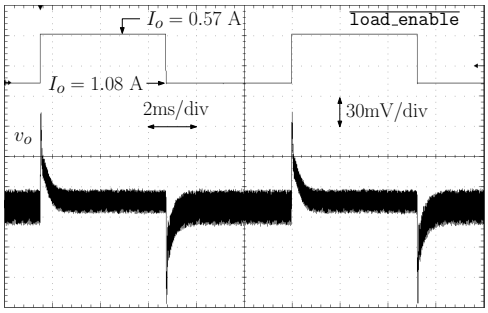


FIGURE 3.15: Experimental response to 0.57 A→1.08 A periodic load step variations with the simplex optimization enabled.

the other hand, the simplex approach reshapes the current and tracks the maximum efficiency point over the entire operating range.

The measured closed-loop transient response of the converter to a 0.57 A $\rightarrow$ 1.08 A $\rightarrow$0.57 A sequence of load step variations with the simplex optimization enabled is illustrated in Fig. 3.15. The closed-loop dynamic behavior is compatible with the designed bandwidth and phase margin, and the simplex optimization loop does not compromise the load regulation dynamics.

To assess the robustness of the algorithm in converging to the peak efficiency point, a random set of initial simplexes is generated in region R_3, and the simplex convergence checked. Initial simplex choices and the points reached two seconds after the simplex FSM is enabled are shown in Fig. 3.16, confirming that the algorithm is consistently capable of reaching the maximum efficiency region.

The following concluding sections discuss specific provisions that have

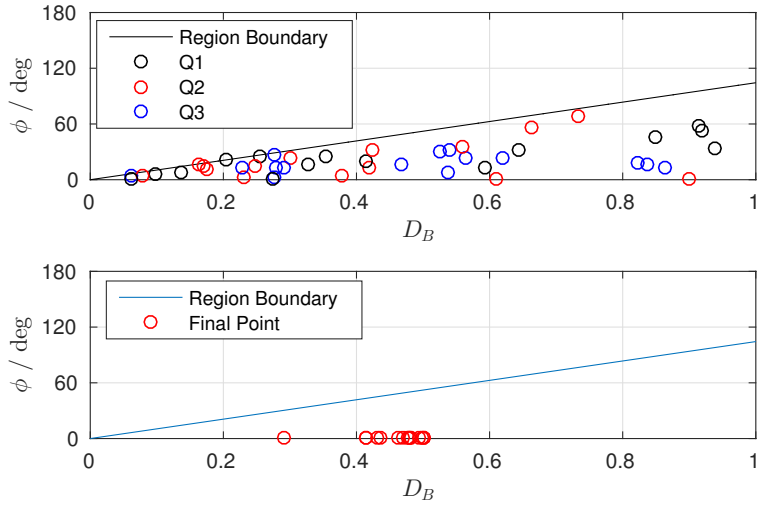


FIGURE 3.16: (top) Starting and (bottom) ending points of the simplex algorithm for $P_o = 3$ W.

been undertaken to guarantee the simplex algorithm convergence and robustness of operation.

3.1.4 Constraints on the Search Region

Since the maximum is known to be on the upper part of region R_3, the algorithm should be forced to converge there: without any restriction, the algorithm can in fact potentially converge to any other efficiency peak, e.g. the relative maximum present in region R_2 and visible in Fig. 3.5a.

To force the convergence in R_3, a combinational network checks if the point (D_B, ϕ) is outside of region R_3, and doubles the measured current value if such condition is verified. The effect of this provision is to fictitiously decrease the measured efficiency outside region R_3 and force the simplex search to bounce off its boundaries and never escape such region.

3.1.5 Output Voltage Disturbance Reduction

During optimization, rapid changes in (D_B, ϕ) imposed by the simplex FSM would induce disturbances on the output voltage. To avoid this, the (D_B, ϕ)

command output by the simplex algorithm is forced to slowly ramp to the new values at each update. The step of the staircase is chosen to cause a negligible overshoot in the output voltage. Note the spike amplitude will be different depending on the operating point. The sampling period of the staircase is selected to be slightly shorter than four times the worst-case closed-loop time constant, thus assuring the voltage reaches almost its steady state value after each step. The simplex FSM clock is calculated in order to let the staircase to achieve 50% D_B and ϕ swing in the worst case condition.

3.1.6 Single Point Collapse Prevention

Since the (D_B, ϕ) plane is discrete because of its digital representation in the controller, the vertices of the simplex may collapse into a *single* point after certain contractions. This occurrence mut be prevented, since the simplex algorithm would be unable to further expand or move the simplex after a collapse event. After the contraction, the condition $Q_1 = Q_2 = Q_3 = (D_B^*, \phi^*)$ is checked and, if verified, the simplex is enlarged by selecting three new points in close proximity of (D_B^*, ϕ^*). The increase is obtain by adding or subtracting 2 LSB's to the respective bit representation of $D_{B_{1,2,3}}$ and $\phi_{1,2,3}$.

This provision forces the simplex algorithm to reach a steady-state limit cycle after convergence, consisting of a periodic cycle between points Q_1, Q_2, Q_3 and Q_{Ref}. Nonetheless, these points are sufficiently close to each other not to compromise the output voltage regulation.

3.2 Conclusion and Summary of Contributions

Switching dc-dc converters offer higher efficiency with respect to the linear converters at heavy-load. To improve light-load behavior the NR-DHB topology is selected and its modulation degrees of freedom are exploited to increase the efficiency. Instead of calculating the highest efficiency trajectory,

an adaptive online efficiency optimizer is devised. In the proposed approach the input current is measured and the two modulation quantities D_B and ϕ are changed on-the-fly to minimize i_g. The major advantage of this method is that the optimization does not depend on the characterization of the converter efficiency, avoiding the complex modeling of switching losses. Moreover the approach is robust against operating point variation and component aging. The proposed technique requires a low-gate-count finite state machine, while the input current can be sampled a very low rate.

Chapter 4

Single Stage Microcontroller Supply from 48 V Bus

4.1 Introduction

The development of hybrid and full electric vehicles is leading to an increase in the electric power on cars. So far the required supply voltages are derived from the 12 V battery through dc-dc converter and delivered through copper cables throughout the car. Supply voltages includes the conventional 5 V and 3.3 V, but also lower microcontroller supply level (i.e. 1.5 V or less). The low voltage means the need of a wide cross-section wire, and this has a negative effect on both car price and fuel consumption. For these reasons car manufacturers propose to shift the battery voltage to 48 V [73], to deliver this single voltage bus through the car and to obtain all the required voltages locally by means of high step-down dc-dc converter. In this new scenario a single small cross-section wire is needed, but high efficiency high step-down converter are required.

In this work the 48 V to 1.5 V scenario is considered, where the transfer ratio is about 3.1%. In section 4.2 some promising topology are compared and the series resonant tapped inductor (SCTI) converter is selected. The steady state analysis SCTI is described in section 4.3, where a transient issue

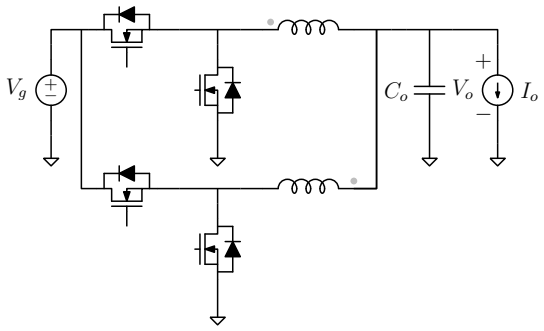
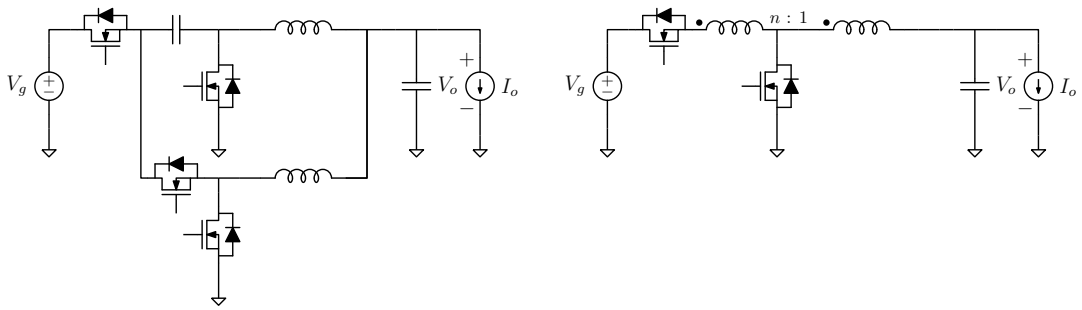


FIGURE 4.1: Interleaved buck converter, with the optional coupling shown in gray.

is highlighted, while its operation is compared with the tapped-inductor buck converter (TIB) one in section 4.4.2. The analytical study of the transient issue is presented in section 4.5 and a hardware and a software solution are disclosed in sections 5.2 and 5.3 respectively.

4.2 Topology Selection

Step down applications usually lead to the buck topology because of its low component count and high efficiency. The hard turn-on switching can be mitigated through quasi square wave [74] or quasi-resonant operation [75]. In case of high current demand, interleaving can be included ([76],Fig. 4.1), which also improved the transient response. To reduce the output ripple and the core number demands, coupled inductor can also be used [77]. But the buck topology has a duty ratio D equals to the transfer ratio $M \triangleq V_o/V_g$ and it is a main drawback regarding high step down conversion. For the application taken under consideration the required duty cycle is $D = M \simeq 3.1\%$, thus making challenging to produce a precise on-time at high frequency. To increase the step-down action, two main strategies have been developed. The first is to add a switched capacitor cell in order to reduce the effective input voltage, the second is to replace the inductor with a tapped inductor. The first strategy leads to the series capacitor buck (SBC) [78, 79], Fig. 4.2a,



(a) (b)

FIGURE 4.2: High step down topologies: series capacitor buck converter (a) and tapped-inductor converter (b).

while the second to the tapped-inductor buck converter [80], Fig. 4.2b

4.2.1 Series Capacitor Buck Converter

The SBC combines a switched capacitor cell with an inductor based converter, in this way the former performs the conversion, while the latter finely regulates the output. Zero voltage switching for all devices is achieved and the series capacitor acts as a DC voltage source of $V_g/2$, thus halving the voltage stress during commutation and reducing both turn on and turn off losses. Moreover the current ripple is reduced and it is equivalent to a four phase buck converter, thus reducing conduction and core losses and current balancing between phases is automatically achieved. A minor problem at light load – inductor current reversal – is addressed in [81], where an uneven phase interleaving is proposed. The small signal model and optimal state-space trajectory for this converter have been studied [82] and the SBC converters are now suitable replacements for Buck converters in 12 V to 1.x V applications, including integrated solutions [83]. However SBC topology requires four switches and two cores and its main drawback is that the duty cycle is only doubled, thus limiting its step-down action.

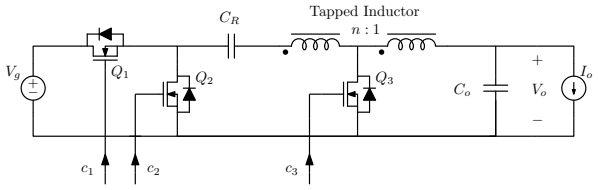


FIGURE 4.3: Series Resonant Tapped-Inductor (SCTI) Converter.

4.2.2 Tapped-Inductor Converter

If the inductor of the buck converter is replaced with a tapped inductor, the topology in Fig. 4.2b is obtained. Because of this modification, the conversion ratio modifies [84] in

$$M = \frac{D}{D + n(1 - D)} \tag{4.1}$$

which for small D means $M = D/n$. The duty ratio is increased by almost a factor of n. Moreover the taped inductor requires a single core, hence the footprint does not increase significantly. The upper mosfet undergoes hard switching turn-on, and it represents an issue for high frequency operation. Even if switching losses can be mitigated through suitable modulation [85], ZVS cannot be guaranteed for the full load range. The main drawback is represented by the voltage spike which affects the turn-off of the upper MOSFET, which is caused by the leakage inductance. Several clamping circuits have been proposed to reduce the voltage overshoot [86, 87] or to recover leakage inductance energy to power gate drivers [88]. However, these provisions come at the cost of a larger bill of material and of an increased complexity in the topology.

4.2.3 Series Capacitor Tapped-Inductor Converter

The series capacitor tapped inductor (SCTI) converter – illustrated in Fig. 4.3 – is a promising topology for high step-down, high frequency application, which brings a significant increase of the operating duty cycle. SCTI features a single-core tapped-inductor and with respect to TIB it needs an additional

switch and capacitor. The two input switches are controlled as an half bridge, i.e. they have complementary driving signals and a small dead time between them, while the mosfet Q_3 is driven with Q_2. The mosfet drivers can be standard bootstrapped half-bridge drivers.

SCTI converter can be designed to have quasi-resonant or piecewise linear operation. In both cases the series capacitor C_R forces the primary winding current to have zero average value, achieving ZVS turn-on for the two input power devices, while the third mosfet Q_3 exhibits zero current switching (ZCS) turn-on.

In the quasi-resonant design [89, 90] resonance period of capacitor and leakage inductance is next to the switching period. During off-time currents have a sinusoidal shape, while during on-time the current is linear. In this operation mode, the current i_{Q3} can change sign during the off-time. A small capacitor can be employed but to have optimal switching a fixed off-time control must be used. It results in a non-constant frequency operation, which is normally avoided in automotive application for EMI interferences.

The piecewise linear operation [91–95] requires a resonant period higher than several switching periods in order to have linear current shape also during the off-phase. The main advantage however is the possibility to operate under constant frequency PWM modulation, which simplifies the control. Overall, the reduced switching losses, increased duty cycle and the single magnetic core structure make the SCTI topology attractive for high-frequency operation, integration and large step-down applications.

One rather severe drawback of this converter, on the other hand, is the large voltage spike appearing across Q_3 as a result of hard turn-off of the switch during *transient* events, which strongly compromises the reliability of the converter and limits its attractiveness [96]. To solve this issue hardware or software based solutions can be proposed. The first includes snubbers and clamp and will be described in section 5.2, while the latter is disclosed in

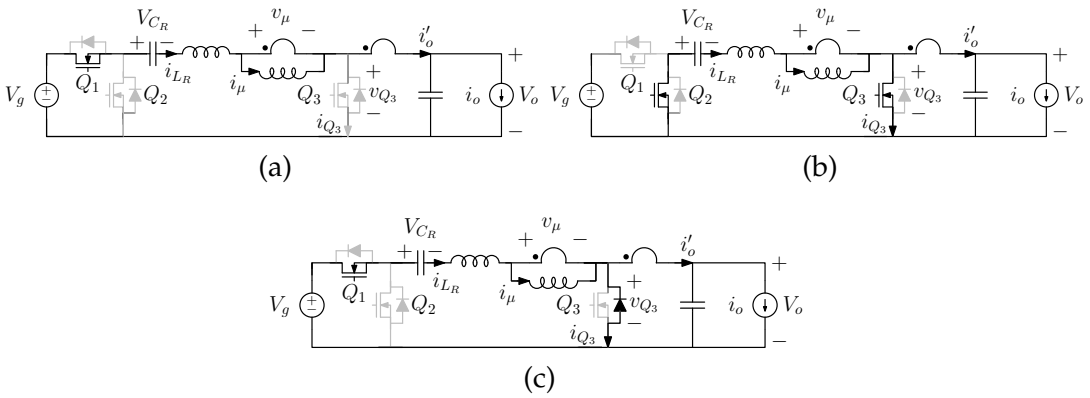


FIGURE 4.4: SCTI during (a) ON-phase, (b) OFF-phase, and (c) free-wheeling phase.

section 5.3.

4.3 Steady-State Analysis

The steady state analysis of the SCTI converter for non-resonant operation is here outlined. Q_1 and Q_2 are complementary driven, while Q_2 and Q_3 are driven together. The capacitor C_R is designed in order to have zero ripple and the DC voltage across it can be found by inspection to be equal to $DV_g - V_o$. The coupled inductor is modeled as an ideal transformer with a magnetizing inductance and a primary leakage inductance. Because of C_r the average leakage inductance current is zero, which forces the average magnetizing inductance current to be I_o/n.

SCTI converter has three topological states, namely on-state, off-state and freewheeling-state, which are shown in Fig. 4.4. The following analysis is based on small ripple approximation of the capacitor voltages and the volt-second balance approach [65]. Time-varying values are represented by small letters (e.g. v_μ), constant and DC values by capital letters (e.g. V_g or V_o), while values averaged on a switching period are distinguished by an horizontal bar (e.g. $\bar{i}_R$). Small ripple approximation on capacitors means $v_{C_R} = \bar{v}_{C_R} = V_{C_R}$ and $v_o = \bar{v}_o = V_o$.

4.3.1 On-State

During the on-state, the upper mosfet Q_1 is on, while Q_2 and Q_3 are off (Fig. 4.4a). The secondary current is equal to C_R current i_R, and thus the two inductor currents are liked

$$(n+1)i_R = ni_\mu$$

and they do not describe two independent state variables. A qualitative sketch of the converter waveforms are shown in Fig. 4.5. The voltages applied to the inductors are

$$\begin{aligned} V_{\mu,\text{on}} &= \frac{n(n+1)}{(n+1)^2+n^2\lambda}(V_g - V_{C_R} - V_o) \\ V_{R,\text{on}} &= \frac{n^2\lambda}{(n+1)^2+n^2\lambda}(V_g - V_{C_R} - V_o) \end{aligned} \tag{4.2}$$

The inductance currents increase, charging the capacitor C_r, which sees and equivalent inductance equal to

$$L_{on} = L_R + L_\mu \frac{(n+1)^2}{n^2}$$

Eq. (4.3.1) shows that the equivalent on-time inductance is higher than L_R and even in resonant mode, the capacitor current is linear during on-time.

4.3.2 Off-State

When Q_1 is opened and Q_2 and Q_3 are closed (Fig. 4.4b), the converter enters the off-phase. Since current can flow in Q_3, i_R and i_μ are no longer related and become independent quantities. The secondary voltage experiences a voltage equal to V_o, clamping the $v_\mu = nV_o$. Now C_R sees dinamically only

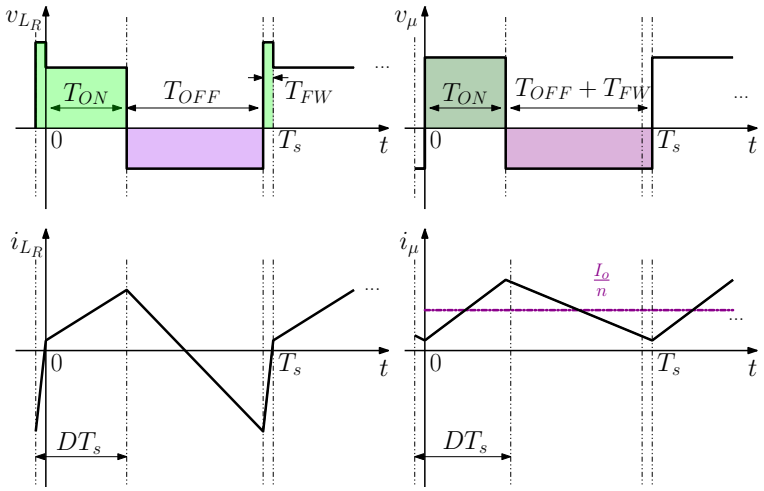


FIGURE 4.5: Qualitative steady-state plots of voltages and currents associated with the magnetizing and leakage inductances.

inductance L_R. The two inductance voltages are

$$\begin{aligned} V_{\mu,\text{off}} &= nV_o \\ V_{R,\text{off}} &= -V_{C_R} - nV_o. \end{aligned} \tag{4.3}$$

In *steady state*, the current which flows through Q_3 decreases and becomes negative. Current i_{Q3} can always be expressed as a linear combination of the inductance currents i_R and i_μ

$$i_{Q3} = (n+1)i_R - ni_\mu.$$

For this reason current i_{Q3} cannot undergo a sudden change.

4.3.3 Freewheeling-State

When Q_1 is closed and Q_2 and Q_3 are open, the converter cannot return immediately to the on-state because current i_{Q3} has reached a negative value, therefore a small interval is required in order to return this current to zero. Since the current i_{Q3} is negative in *steady-state*, it can flow through the body diode of Q_3, as shown in Fig. 4.4c. Note that if the current were positive,

opening MOSFET Q_3 causes a sudden change in and inductor current and thus a voltage spike, which is a reliability issue for this topology and it will be discussed in section 4.5. During freewheeling-state the voltage across v_μ remains nV_o, while the voltage across i_R is V_g higher with respect to the off-phase one:

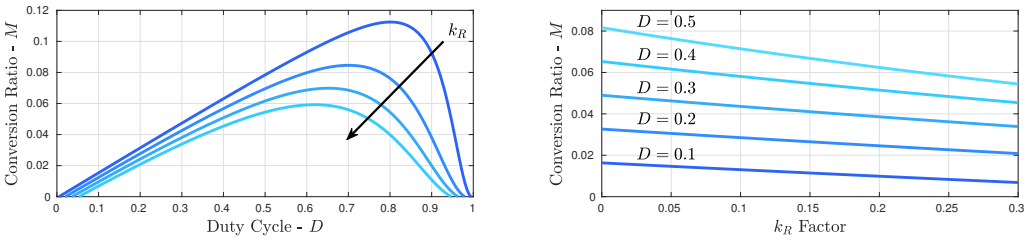
$$\begin{aligned} V_{\mu,\text{fw}} &= nV_o \\ V_{R,\text{fw}} &= V_g - V_{C_R} - nV_o. \end{aligned}$$

Since in this application $V_g >> V_o$, it means that during the freewheeling phase the current slope is significantly steeper than the one in off-phase. The current i_{Q3} moves quickly to zero and the freewheeling phase is short in time, but this topological state cannot be neglected because the current variation is relevant.

4.3.4 Voltage Conversion Ratio

Even if the duration of T_{FW} is short, the approximation $T_{FW} \simeq 0$ cannot be used to estimate the voltage conversion ratio, current stress or conduction losses. Note that the freewheeling time is a reduction of the on-time imposed by the controller, i.e. $D_{\text{on}} + D_{\text{fw}} = D$. Applying the volt second balance, and calling $D_{\text{on}} \triangleq T_{\text{on}}/T_s$, $D_{\text{off}} \triangleq T_{\text{off}}/T_s$ and $D_{\text{fw}} \triangleq T_{\text{fw}}/T_s$ yields:

$$\begin{cases} D_{\text{on}} V_{R,\text{on}} + D_{\text{off}} V_{R,\text{off}} + D_{\text{fw}} V_{R,\text{fw}} = 0 \\ D_{\text{on}} V_{\mu,\text{on}} + D_{\text{off}} V_{\mu,\text{off}} + D_{\text{fw}} V_{\mu,\text{fw}} = 0 \\ D_{\text{on}} + D_{\text{fw}} = D \end{cases} \tag{4.4}$$



(a) (b)

FIGURE 4.6: Voltage conversion ratio M as a function (a) of the duty cycle, and (b) of k_R factor.

where $V_{R,\text{on,off,fw}}$ and $V_{\mu,\text{on,off,fw}}$ are given by (4.2),(4.3) and (4.4). From (4.4) the voltage conversion ratio M is calculated:

$$M(D,k_R) = \frac{D}{n+1}\frac{1}{1+\lambda\left(\frac{n}{n+1}\right)^2}\frac{(1-D)^2(n+1)-(1/D-1)k_R}{(1-D)^2(n+1)+k_R}, \tag{4.5}$$

where

$$k_R \triangleq \frac{2f_s L_R\, I_o}{V_g}$$
$$\lambda \triangleq \frac{L_R}{L_\mu}.$$

Eq. (4.5) is sketched in Fig. 4.6a for different values of the parameter k_R. The conversion ratio versus k_R is illustrated In Fig. 4.6b for different values of D. With $k_R = 0$, i.e. in open circuit operation, (4.5) becomes:

$$M_0 \triangleq M(D,0) = \frac{D}{n+1}\frac{1}{1+\lambda\left(\frac{n}{n+1}\right)^2}, \tag{4.6}$$

which exhibits a linear dependence on D. The conversion ratio decreases with increasing output current, thus $M \leq M_0$ for all $I_o \neq 0$.

Approximation $M \approx M_0$ is valid at low currents, when the freewheeling time is short enough to be negligible in the analysis. In this limit the sub-topology corresponding to freewheeling time disappears and the SCTI

practically operates across the ON and OFF topological states only. During the on-time the source energy is stored in magnetizing inductance, and released to the output stage during off-time. Eq. (4.5) further approximates into

$$M_0 \approx \frac{D}{n+1} \tag{4.7}$$

as long as

$$\lambda \ll \left(\frac{n+1}{n}\right)^2, \tag{4.8}$$

i.e. as long as $L_R \ll L_\mu$, a condition which is easily met in practice. Eq. (4.7) shows a linear dependence with the duty cycle D. The system (4.4) gives also the duration of the three topological states:

$$D_{\text{on}} = \frac{1}{1+\frac{M_0}{M}\left(\frac{1}{D}-1\right)} \tag{4.9}$$

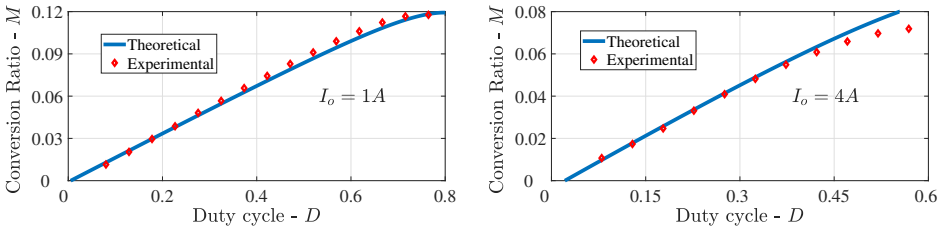
$$D_{\text{off}} = (1-D) \tag{4.10}$$

$$D_{\text{fw}} = D - D_{\text{on}}. \tag{4.11}$$

When $I_o = 0$ then $k_R = 0$ and $M = M_0$, hence (4.9) simplifies in $D_{\text{on}} = D$ and $D_{\text{fw}} = 0$. These equations can be used in conjunction with the expressions in Fig. 4.5 to predict the current peaks or the conduction losses of the body diode.

4.3.5 Experimental Results

In order to verify the relation (4.5), steady-state measurements are carried out on the prototype. In Fig. 4.7 a comparison between the theoretical and measured voltage conversion ratio is reported for two distinct load current levels, namely $I_o = 1$ A in Fig. 4.7a and $I_o = 4$ A in Fig. 4.7b. The comparison fully confirms the accuracy of the analysis disclosed previously, which in turn is an extension of previously reported results for the SCTI topology.



(a) (b)

FIGURE 4.7: Theoretical (solid line) vs. experimental (dots) voltage conversion ratio for (a) $I_o = 1$ A and (b) $I_o = 4$ A.

4.4 MOSFET Commutations

Because of C_R, input mosfet experiences ZVS commutation, but turn-on of Q_3 requires a few remarks. ZVS condition for Q_3 is obtained if $i_{Q_3}(T_{\text{OFF}}) < 0$, which occurs if and only if the slope of i_{Q_3} is negative during the off-time. The steady-state condition for soft switching can therefore be written as

$$\left.\frac{\mathrm{d}i_{Q_3}}{\mathrm{d}t}\right|_{t=T_{ON}} = (n+1)\frac{V_{L_R}}{L_R} - n\frac{V_\mu}{L_\mu} \leq 0. \tag{4.12}$$

By solving (4.12) with respect to V_{C_R}, condition for ZVS turn-off of Q_3 becomes

$$v_{C_R} > n\left(1 + \frac{\lambda n}{n+1}\right) M V_g. \tag{4.13}$$

In order to prove (4.13), consider first that, in steady-state, the following equations hold,

$$\begin{aligned} V_{C_R} &= DV_g - V_o \\ M_0 &> M. \end{aligned} \tag{4.14}$$

Using the above results in (4.13), the following chain of inequalities can be written,

$$\begin{aligned} &DV_g - V_o\,(I_o > 0) > \\ &DV_g - V_o(I_o = 0) = n\left(1+\lambda\frac{n}{n+1}\right)M_0 V_g > \\ &\qquad\qquad n\left(1+\lambda\frac{n}{n+1}\right)MV_g, \end{aligned} \tag{4.15}$$

where the central equality is easily proved,

$$\begin{aligned} &DV_g - V_o\,(I_o = 0) = \\ &\left[(n+1)\left(1+\lambda\left(\frac{n}{n+1}\right)^2\right)-1\right]M_0 V_g \\ =&n\left(1+\lambda\frac{n}{n+1}\right)M_0 V_g \end{aligned} \tag{4.16}$$

Therefore the ZVS turn-off condition for Q_3 expressed by (4.13) is always verified in steady-state.

4.4.1 Steady-state voltage ringing across Q_3

If the output current is not negligible, the freewheeling time sub-topology follows the off-time sub-topology, and a voltage ringing appears at drain node of Q_3 at the end of such phase. This phenomenon is similar to what occurs in a buck converter working in DCM [65, 97, 98]. The waveform corresponding to the steady-state operation are sketched in Fig. 4.8. After the ringing V_{Q3} reaches the value

$$V_{Q3,\text{on}} \;=\; V_o + \frac{V_g(1-D)}{n+1}\frac{1}{1+\left(\frac{n}{n+1}\right)^2\lambda}. \tag{4.17}$$

This type of *steady-state* ringing does not pose a reliability issue as long as the voltage rating of Q_3 is adequate. As discussed in section 4.5, on the other

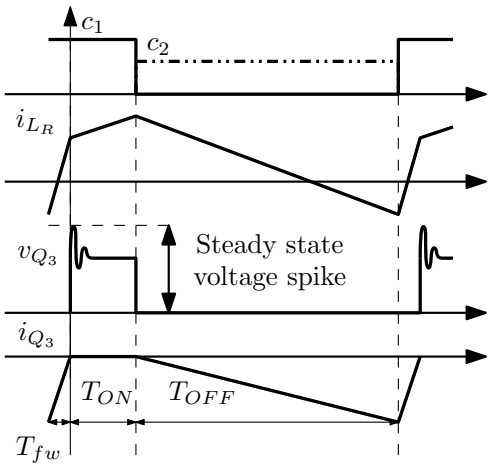


FIGURE 4.8: Steady-state waveforms including the steady-state voltage ringing across Q_3

hand, a much more severe voltage spike across Q_3 can occur during *transient* conditions in which Q_3 turns-off at positive drain-to-source currents.

4.4.2 Comparison with TIB Topology

SCTI and TIB topology have both high step-down capability and require a single-core tapped-inductor. To compare their operation a practical case of a 40 V to 100 V input voltage, 1.5 V output voltage is considered. For both converters a winding ratio of $n = 5$ is used.

A standard buck converter would operate at $D = M \simeq 1.5\% - 3.8\%$, which is challenging to be generated, especially at high frequency. On the other hand TIB voltage conversion ratio can be expressed as

$$M_{\text{TIB}} = \frac{D}{D + (1 - D)n} \simeq \frac{D}{n} \text{ small } D \tag{4.18}$$

thus requiring $D \simeq 7\% - 16\%$, while SCTI in the same condition requires $D \simeq 10\% - 24\%$ using (4.7). Both topologies offer a duty cycle expansion, which is slightly higher in SCTI, especially with lower value of winding ratio n.

Neglecting snubber circuits, TIB converter requires only two switches, with the upper mosfet undergoing hard switching turn-on and turn-off with continuous conduction mode. ZVS turn-on can be achieved with an intentionally small magnetizing inductance design [85] which on the other hand increases the conduction losses, or with resonant transitions [99]. The main drawback of TIB is the turn-off of the main switch, which forces a sudden change in the primary leakage inductance, leading to a high voltage spike. For this reason, clamp circuits are required [86], increasing the topology complexity and adding silicon devices. In SCTI the introduction of the series capacitor C_R forces the average input bridge current to be zero, thus achieving ZVS turn-on for both Q_1 and Q_2. Also Q_3 experiences in steady state ZVS commutation, and since i_{Q3} is linear combination of inductor currents, it starts decreasing slowly during turn-off, which leads to ZCS turn on.

4.5 Overvoltage Phenomenon During Transient Events

ZVS turn-on of Q_3 always occurs in steady state condition, but transient events may force i_{Q3} to be positive at turn-off, thus leading to a voltage spike.

Transients can be induced by input voltage of duty cycle steps and the resulting current waveform with positive slope is shown in Fig. 4.9

Eq. (4.14) can no longer be satisfied after a sudden decrease of V_g or D, as it becomes clear after rearranging the mentioned inequality as

$$V_g D \geq n V_o \left(1 + \frac{\lambda}{n+1} V_o\right)$$

and considering that V_{CR} dynamic response is faster than the one of V_o. This causes a hard turn-off of Q_3 which leads to a severe voltage spike at the drain of Q_3. The reason for such severe voltage spike is the resonance between the

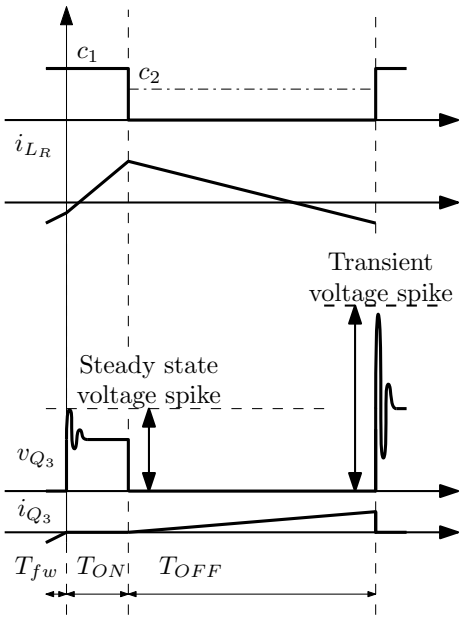


FIGURE 4.9: Converter waveforms during a spike-inducing transient event.

device output parasitic capacitance and inductances L_R and L_μ, excited by the sudden variation in the inductive currents i_{L_R} and i_{L_μ}. The voltage spike is only limited by the characteristic impedance Z_o of the parasitic resonant circuit: with a hypothetical ideal device having zero output capacitance, turn-off of Q_3 at positive drain-to-source current would cause inductive currents i_{L_R} and i_{L_μ} to undergo an abrupt discontinuity, causing the resulting voltage spike to have infinite amplitude.

4.5.1 Analysis of the over-voltage event at Q_3 turn-off

Fig. 5.3a illustrates the circuit model used in the following to analyze the over-voltage event occurring when Q_3 turns-off at positive current during a transient condition.

In the circuit model, capacitor C_R is approximated by a short-circuit during the spike event, and only its initial condition $V_{C_R} = DV_g - V_o$ is retained, corresponding to the dc value of v_{C_R}. This choice is consistent with the small-ripple approximation hypothesis made at the beginning of our analysis. The same considerations can be made for output capacitance. The ideal turn-on

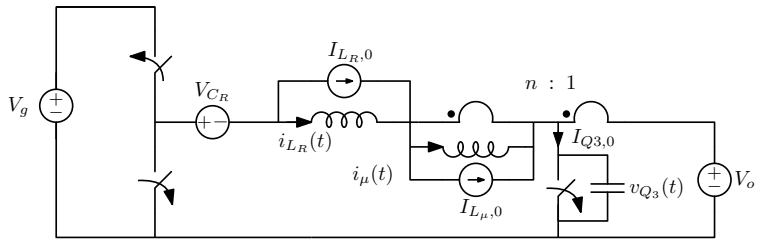


FIGURE 4.10: Circuit model used for transient analysis of the over-voltage event across Q_3.

and turn-off of Q_1 and Q_2 respectively can be analytically modeled by a step function $\mathcal{H}(t)V_g$, when $\mathcal{H}(t)$ is the unit step function. To obtaining a rough estimate of the voltage spike across Q_3, no lossy elements are included in the model.

Current $I_{Q3,0}$ represents the current through Q_3 at the device turn-off instant, and is related to the initial conditions $I_{L_R,0}$ and $I_{L_\mu,0}$ on the leakage and magnetizing inductance by

$$I_{Q3,0} = (1+n)I_{L_R,0} - nI_{L_\mu,0}. \tag{4.19}$$

By solving the evolution of the circuit in Fig. 5.3a, the voltage $v_{Q_3}(t)$ and current i_{Q3} can be written as

$$\begin{cases} v_{Q_3}(t) = V_{Q3,\text{on}} - V_{Q3,\text{on}}\cos(\omega_0 t) + Z_0 I_{Q3,0}\sin(\omega_0 t) \\ i_{Q_3}(t) = I_{Q3,0}\cos(\omega_0 t) + \frac{V_{Q3,\text{on}}}{Z_0}\sin(\omega_0 t) \end{cases} \tag{4.20}$$

where

$$\begin{aligned} \omega_0 &\triangleq \frac{1}{\sqrt{C_{Q3}L_{\text{eq}}}} \\ Z_0 &\triangleq \sqrt{\frac{L_{\text{eq}}}{C_{Q3}}} \\ L_{\text{eq}} &\triangleq \frac{L_R}{(n+1)^2} \parallel \frac{L_\mu}{n^2} \end{aligned} \tag{4.21}$$

TABLE 4.1: Parameters of the case study SCTI converter.

Nominal input Voltage V_g	48 V
Input voltage range	40 V-90 V
Output voltage V_o	1.5 V
Output current I_o	4 A
Switching frequency f_s	195.3 kHz
Tapped inductor turns ratio n	5
Leakage Inductance	2.6 µH
Magnetizing Inductance	16 µH
Series capacitance C_R	3 x 33 µF
Output capacitance C_o	174 µF
V_g sensing attenuation factor α	0.047
v_{Q_3} sensing attenuation factor β	0.18

and $V_{Q3,\text{on}}$ is given by (4.17). The voltage peak at the drain of Q_3 can be expressed as

$$V_{Q_3MAX} = V_{Q3,\text{on}} \left(1 + \sqrt{1 + \left(\frac{Z_0 I_{Q3,0}}{V_{Q3,\text{on}}} \right)^2} \right) \tag{4.22}$$

This peak depends on the operating point (V_g, D, I_o), on the initial condition $I_{Q3,0}$, on the capacitance C_{Q_3} and on tapped inductor parameters (λ, n, L_R). Notice that, as anticipated, the larger the characteristic impedance Z_0 of the resonant circuit is, the larger the spike.

Voltage spike V_{Q_3MAX} is reported in Fig. 4.11 as a function of the drain-to-source current i_{Q_3} and for the reference values summarized in Tab. 4.1. In the plot, a parasitic capacitance $C_{Q_3} \approx 0.1$ nF is assumed. As expected, the voltage spike is more and more severe as the leakage-to-magnetizing inductance ratio $\lambda \triangleq L_R / L_\mu$ increases. The transient over-voltage issue here briefly outline represents a strong reliability limitation of the synchronous SCTI converter.

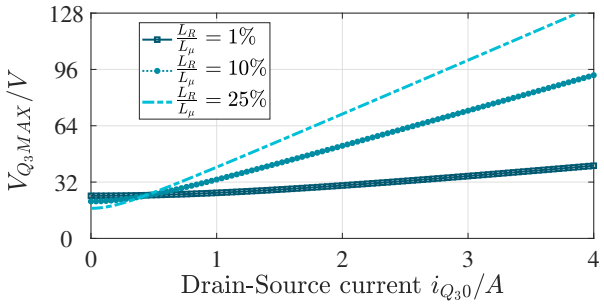


FIGURE 4.11: Estimated voltage spike across Q_3 with respect to the drain-to-source current i_{Q_30} at the turn-off instant.

TABLE 4.2: List of Constraints

Maximum Input Voltage	$V_{g,max}$	72 V
Output Voltage	V_o	0.9 V
Static V_o Precision	$\delta V_{o,s}$	1%
Dynamic V_o Range	$\delta V_{o,d}$	5%
Settling Time	T_{set}	20 µs

4.6 Efficiency Optimization with Commercial Inductors

The efficiency optimization of SCTI topology requires custom inductor design, but since this topology is not a common choice, no *ad-hoc* magnetic parts are commercially available yet. In this case the converter parameters should be adapted to commercial available inductors in order improve its operation. During a research period at Infineon Technologies A.G. (Munich) under the supervision of Prof. Georg Pelz, the 48 V bus to 0.9 V microcontroller core supply interface converter application has been studied. Static and dynamic specifications are given in Tab. 4.2.

4.6.1 Design Parameters

SCTI design requires the selection of inductor parameters, capacitance values, the switching frequency and the MOSFET areas.

TABLE 4.3: Commercial Inductors

Name	L_μ/μH	n	$\lambda = L_R/L_\mu/\%$	$R_{s,p}/\text{m}\Omega$	$R_{s,s}/\text{m}\Omega$
LPR5030	199	10	10.3	2500	60
TA7609	32	4	3	105	33
Lab Made	15.6	5	15.4	160	17

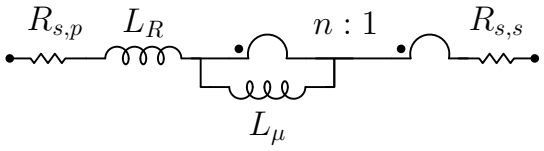


FIGURE 4.12: Inductor model from Tab. 4.3.

Inductor parameters are several and their electrical quantities are related on physical dimension in an analytically complex way. On the other side as mentioned only commercial inductors will be employed, thus no magnetic optimization is further considered. A separate optimization has to be performed separately for each selected inductor. In order to obtain small ripple across the capacitors, C_R and C_o should be designed with a ripple constraint in mind. Known the inductor and the frequency, the capacitance value is calculated as in (5.18). Larger capacitors do not improve the converter operation, as long as a piecewise linear behavior is obtained. On the contrary switching frequency f_s and MOSFET area values can be varied and have a significant role in the power losses. Thus they become part of the optimization problem which can be stated as

$$\arg\max \eta(f_s, A_1, A_2, A_3) \tag{4.23}$$

where η is the efficiency and A_1, A_2 and A_3 are the MOSFET areas.

The optimization has to be performed under the constraints which are listed in Tab. 4.2, together with the maximum voltage and current stresses for the MOSFETs and it consists in performing a separate optimization for each commercial inductor under consideration (Tab.4.3). The values mentioned in Tab. 4.3 refer to the inductor model in Fig. 4.12.

Degrees of Freedom Limits

In the following the efficiency is considered as a four dimensional function $\eta(\mathbf{x})$ where $\mathbf{x} = \begin{bmatrix} f_s & A_1 & A_2 & A_3 \end{bmatrix}$. In this section the boundaries of the $\mathbf{x}$ space are discussed.

The dynamical response of the controller depends on the switching frequency, hence its minimum value has to be calculated from the required settling time T_{set}. With the approximation

$$T_{\text{set}} \simeq \frac{0.36}{f_c} \simeq \frac{0.36}{f_s/10}$$

the conservative minimum switching frequency $f_{s,min} = 200$ kHz is found. Also the conversion ratio depends from the switching frequency and (4.5) with Fig. 4.6a highlight that M decreases with increasing k_R, i.e. with increasing switching frequency. Given the inductor parameters, a frequency is calculated over which the minimum transfer ratio $M_{\text{min}} = V_{o,min}/V_{g,max}$ cannot be achieved. This value if different for each inductor.

The minimum MOSFET area depends on the current the device should carry. From the area depends the on-resistance which causes a voltage drop when current flows. It is mandatory that the MOSFET stays in linear region:

$$V_{GS} - V_{th} \geq V_{DS,max} = R_{ON} I_{max} = \frac{k_W}{W_{min} L_{min}} I_{max} \tag{4.24}$$

where I_{max} is the maximum worst-case current which flows in the device and k_W is a factor which relates area and on-resistance and it is technology dependent. The channel length is kept to the minimum possible value $L = L_{min}$, while from (4.24) W_{min} can be calculated. To compare the MOSFETs from different voltage rating classes, the ratio

$$\frac{I_{max}}{W_{min}} = \frac{L_{min}(V_{GS} - V_{th})}{k_W} \tag{4.25}$$

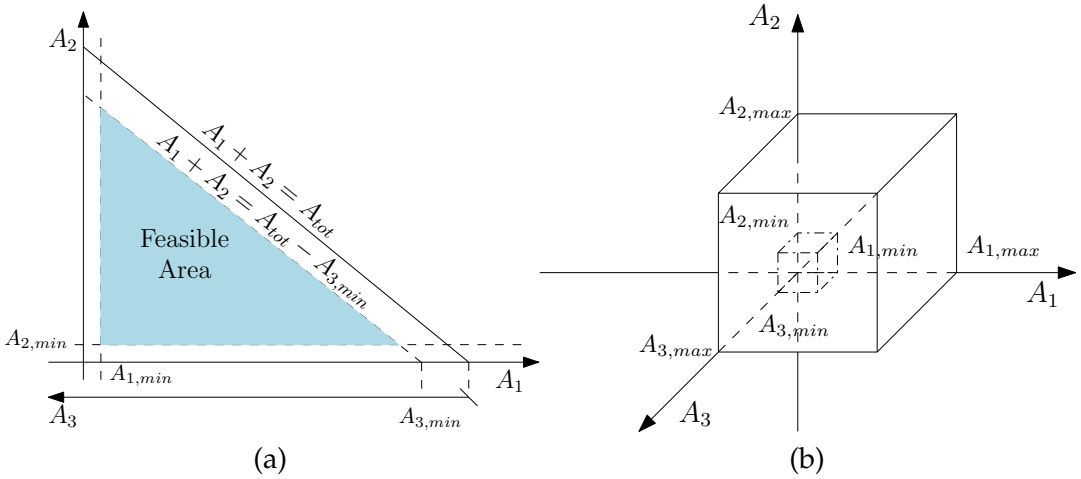


FIGURE 4.13: Feasible region with a total area constraint (a) and with a single area constraint (b).

is considered for the available technologies. High I_{max}/W_{min} means that a small area is capable of carrying high current. As far as the maximum area is concerned, no *intrinsic* limit exists. Two approaches can be followed, the first being limiting the total area $A_{TOT} = A_1 + A_2 + A_3$, while the second is limiting each area separately. To the first case refers Fig. 4.13a. Since the total area is fixed, the A_1, A_2 and A_3 space reduces to a surface. For each $\bar{A}_3 \in [A_{3,min}, A_{tot} - A_{1,min} - A_{2,min}]$ the feasible values for A_1 and A_2 lie on the line $A_2 = A_{tot} - \bar{A}_3 - A_1$. For this reason the value of A_3 can be read on an additional axis which starts from the intersection of the A_1 axis with the line $A_2 = A_{tot} - A_1$. Including the minimum value for A_1, A_2 and A_3 given by (4.25) leads to the light-blue triangle depicted in Fig. 4.13a. If separate constraints for each MOSFET are considered, the A_1, A_2 and A_3 feasible space is contained between two cuboids whose edge has $A_{min}^{1,2,3}$ and $A_{max}^{1,2,3}$ values respectively (Fig. 4.13b). If no strict total area constraint is known, it is of interest to select the second approach. In this way it is possible to see how the efficiency changes also as a function of the total area. In the following, constraints for separate areas are considered.

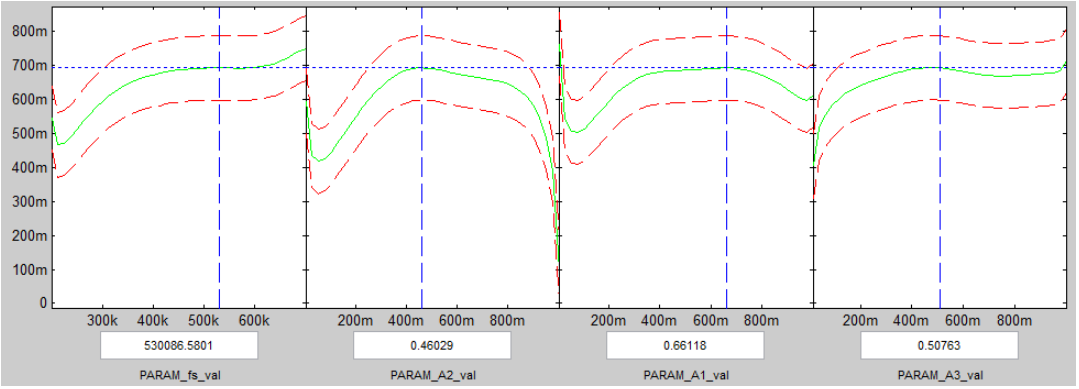


FIGURE 4.14: Metamodel representation for LPR5030 inductor.

Optimization Procedure

For each inductor a separate optimization loop is performed. A Cadence® simulation is employed on several **x** points, the efficiency is measured and the steady state specifications are verified. If the design described by **x** complies with the steady state specifications, the point is considered valid. The next step consists in performing a multi-dimensional regression in order to obtain a continuous function approximation of the efficiency. This approach is called metamodel [100, 101].

Metamodel

The word *metamodel* means model of a model, and in fact the experimental or simulation measurements are sampled and regressed to provide a continuous function of the parameter of interest, which already define a model for the physical world.

Usually the design optimization consists in selecting *a priori* the most influential factors and to optimizing one of them at a time by keeping the others constant. The drawback is that non-linear behavior is common and the separate effects of each parameter cannot be superimposed. The design methodology proposed by the group of prof. Pelz is based on the simultaneous variation of all parameters and on a successive regression. Fig. 4.14 is a screen

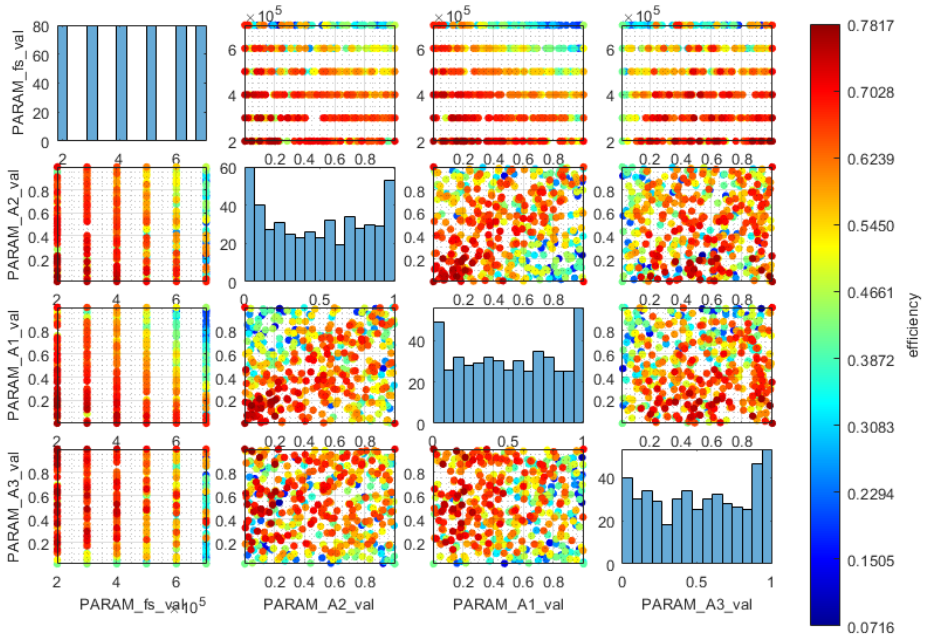
shot of the interactive metamodel representation. It consists in four plots – one for each parameter, here f_s, A_1, A_2, A_3 – showing the target parameter (efficiency in this case) when moving along the four directions i.e. varying one parameter keeping the others constant. It is possible to select a point in one of the graphs and the other update consequently.

The advantage of this approach is that it is possible not only to know where the maximum or minimum of the target function is, but also how the region next to the peak point is. For this goal best results are obtained with a weighted random point sample in the function space: Points next to the peak have higher probability to be sampled. In this way the high-efficiency region is well known, but there are not unknown regions which could hide other minima or maxima.

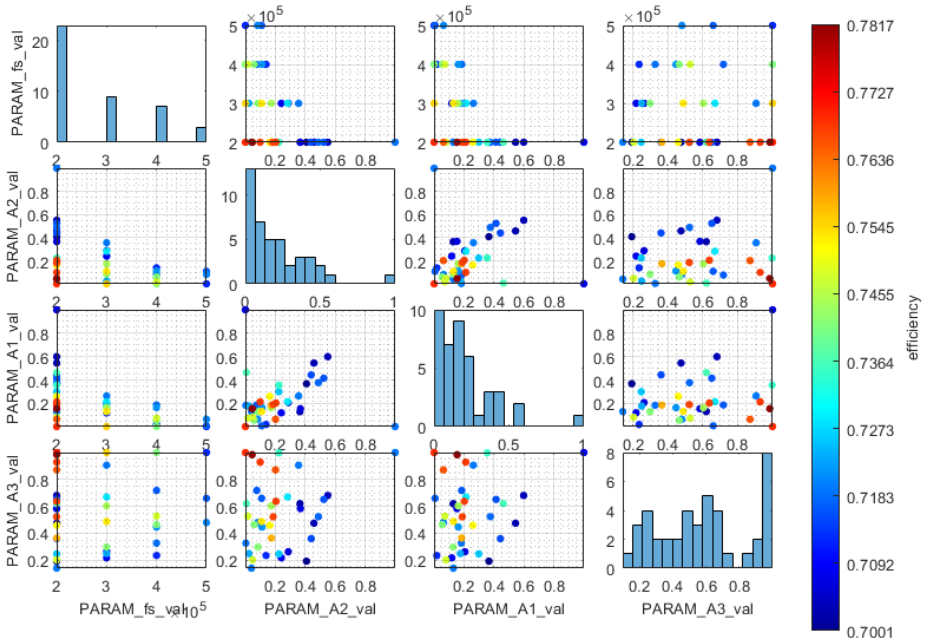
In Fig. 4.15 the four parameters are shown both in horizontal and vertical axis. When two different parameter cross, the scatter plot of the converter efficiency is represented through a color code. On the other hand the plots on the diagonal show histograms, which visualize the sampled values for the parameter. An ideal uniform distribution corresponds to a flat histogram. The frequency histogram in the upper left corner highlights that the frequency values start from 200 kHz and reach 700 kHz with 100 kHz steps. The other three parameters are sampled randomly with an uniform distribution between the limits considered previously. This plot highlights that for LPR5030 inductor the highest efficiency is obtained with the minimum frequency, while the MOSFETs areas A_1 and A_2 should be kept equal.

Comparison Results

The power loss breakdown (Fig. 4.16) suggests some preliminary conclusions about the inductor design. The LPR5030 has a very significant primary parasitic resistance (2500 mΩ) and a reasonable secondary one, but only the 13% of the total losses refers to the former (Fig. 4.16a). The 58% are due to the



(a)



(b)

FIGURE 4.15: Scatter plot of efficiency as a function of every couple of parameters (a) and the same plot limited to efficiency $\eta > 70\%$.

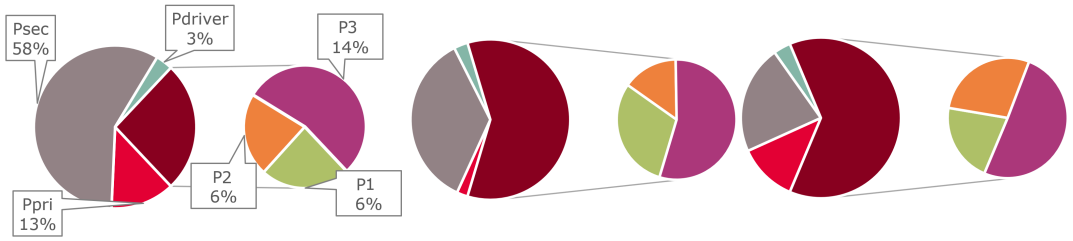


FIGURE 4.16: Power loss breakdown for LPR5030 (a), TA7609 (b) and the hand made inductors (c).

60 mΩ $R_{s,s}$ and the highest efficiency is $\eta_{\max} = 78.2\%$. Only in this high winding ratio inductor ($n = 10$) the inductor losses are higher than the losses located in the silicon. In the TA7609, where the primary winding resistance has a more reasonable value ($R_{s,p} = 105$ mΩ) the losses associated with it are negligible. With $n = 4$ the silicon losses are predominant, while the maximum efficiency increased to 84%. Similar considerations hold for the third inductor (Fig. 4.16c), but here the reduced $R_{s,p}$ leads to a more balanced contribution between primary and secondary winding losses.

Primary parasitic resistance plays a negligible role in the total loss and this is due to the zero average current of the primary winding. On the other hand, the secondary parasitic resistance experiences an average current equal to the output current. For this reason it causes a major loss contribution even if its value is much lower than the primary winding resistance. A last conclusion can be drawn about the winding ratio n whose high values moves the losses from silicon to the inductor.

Commercially available coupled-inductors usually have winding ratio $n = 1$. Only the flyback transformer, which usually has $n > 1$, can be successfully employed in the SCTI converter. However in flyback transformer design both primary and secondary resistances should be kept small, because non-negligible average current flows in both windings. To optimize SCTI a different inductor design is required: n should be the greatest possible within the conversion ratio constraint and the secondary parasitic resistance should

be minimize, while greater primary parasitic resistance is allowed.

4.7 Conclusion and Summary of Contributions

The SCTI converter is a promising topology for high step-down application. The tapped-inductor increases the duty cycle value and the series capacitor lets ZVS turn-on to be achieved for both input MOSFETs. Thus high efficiency at high switching rate can be obtained. In contrast to the TIB converter, no steady-state voltage spike is caused by the leakage inductance and snubbers are not required. The main drawback for SCTI topology arises during transient events, when the ZVS turn-off of Q_3 is lost. In this case a large voltage spike appears, posing a reliability issue. The first contribution of this work is to have identified an overvoltage induce by transient event. The cause of the overvoltage spike is found to be Q_3 current discontinuity and an analytical expression of its peak value is provided. In the second place the optimization of the SCTI topology using commercial available components has been performed during a research period by Infineon Technologies A.G. (Munich) under the supervision of prof. Pelz. The optimization has been carried out through Cadence®simulations, controller by machine learning algorithms provided by the hosting group. The effect of the SCTI components on the efficiency has been studied and design guides for the coupled-inductor have been devised.

Chapter 5

Solutions to the Transient-Induced Overvoltage

5.1 Introduction

In the previous chapter the overvoltage which can be induced by transient events has been highlighted and studied analytically. Since this poses a reliability issue, two solutions are proposed in this chapter: a *hardware* and a *software* solution. The snubber-based solution requires an auxiliary winding, which is wound on the same core of the coupled-inductor. The software-based solution consists in two analog comparators, used to test two separate conditions and a simple finite state machine, which has only three states.

5.2 Snubber-Based Solution

The traditional way to handle voltage spike issue is by adding a snubber. Snubbers which do not include resistive elements are called loss-less snubbers. A zener based snubber is proposed in [92], but the commercially available zener voltages are few and it limits the winding ratio selection. An active clamp is proposed in [102], which requires an additional controlled MOSFET and capacitor. Another feasible solution is based on an auxiliary winding snubber, depicted in Fig. 5.1. This snubber can be wound on the coupled

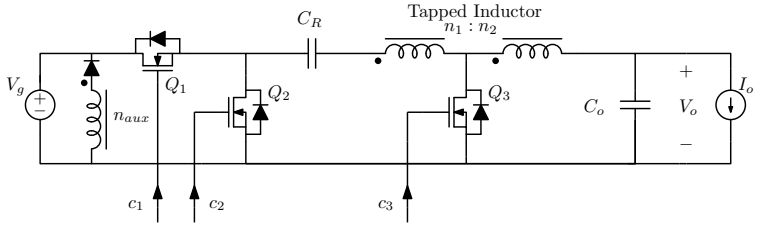


FIGURE 5.1: Auxiliary winding based loss-less snubber.

inductor core, thus without negatively influencing the total converter size. Moreover the auxiliary winding turns ratio does not have implicit constraints as for the zener. The snubber can be designed in order to clamp the voltage spike either during transients only, or to operate on a steady-state basis to also remove the static ringing.

5.2.1 Snubber Ideal Operation

The snubber is employed to prevent the voltage v_{Q3} from exceeding the voltage rating of the device Q_3. The diode in series with the auxiliary snubber conducts only if the voltage across the auxiliary winding $v_{aux} > V_g$, i.e.

$$v_{Q_3} > \frac{n_2}{n_{aux}} V_g + V_o.$$

By imposing that the voltage across Q_3 does not exceed the maximum voltage rating, voltage V_{clamp} is selected. Hence the design equation is derived as

$$n_{aux} \geq \frac{n_2 V_g}{V_{\text{clamp}} - V_o}. \tag{5.1}$$

A transient which causes a positive current i_{Q3} is considered in Fig. 5.2. During the off-time, Q_3 carries $i_{Q3} = (n+1)i_R - ni_\mu$. A positive i_{Q3} means $(n+1)i_R > ni_\mu$, while the on-time condition is $(n+1)i_R = ni_\mu$. Hence to move toward on-phase, a decrease of i_R and/or an increase of i_μ is required. Note that this condition is the opposite of the freewheeling-phase. When $i_{Q_3} > 0$ at turn off of Q_3, the auxiliary diode is forced into conduction and across L_μ a

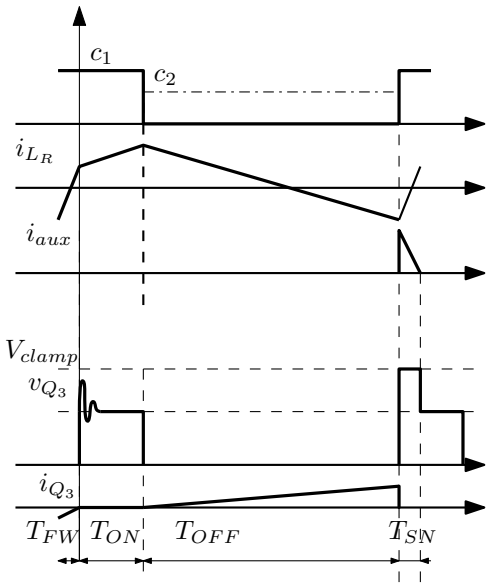


FIGURE 5.2: Transient waveforms when the auxiliary winding snubber is employed.

positive voltage

$$V_{L_\mu} = \frac{n_1}{n_{aux}} V_g > 0$$

forces the current i_μ to increase. At the same time, voltage

$$V_{L_R} = -\left(V_g \left(\frac{n_1 + n_2}{n_{aux}} - 1 \right) + V_{C_R} + V_o) \right) < 0$$

forces i_R to decrease. The auxiliary current becomes quickly zero and the auxiliary diode stops conducting entering the on-time.

5.2.2 Snubber Design Considerations

The auxiliary winding snubber can be designed to suppress transient event only, working like a clamp, or to operate also during steady-state, suppressing the steady-state ringing as well. In the first case, the auxiliary winding does not alter the efficiency of the converter. Hence a winding with a small wire section can be employed, without reducing significantly the core space intended for the two main windings. In the second case, the steady-state ringing is reduced too, leading to a lower voltage stress for Q_3, which can be as low

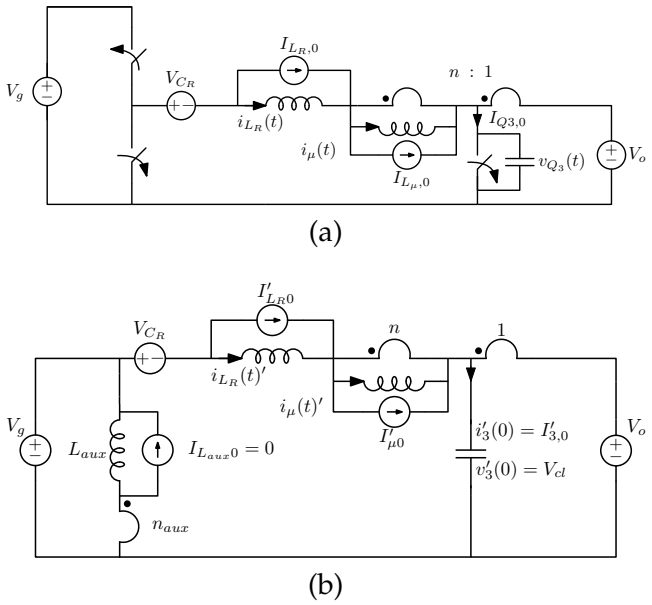


FIGURE 5.3: Equivalent circuit at the end of the freewheeling phase (a) and at the beginning of the snubber operation phase (b).

as the ideal value $V_{Q3_{on}}$. Removal of ringing causes a reduction of both *rms* current value and allows to choose lower R_{dson} devices for Q_3. An additional benefit of both solutions is that the auxiliary diode experiences a low current peak $i_{Q_3} n_2 / n_{aux}$.

Up to this point an ideal auxiliary winding has been considered. In order to predict the actual voltage stress across Q_3, also the leakage inductance of the auxiliary winding must be taken into account. In the next paragraph the time-domain analysis of a snubber designed to suppress the steady state voltage ringing is disclosed.

5.2.3 Effect of Auxiliary Parasitic Inductance

To evaluate the effect of the series parasitic inductance L_{aux} of the auxiliary winding, a snubber with V_{clamp} near to Q_3 on-voltage $V_{Q3,\text{on}}$ is designed. In steady state, the off-phase is followed by the freewheeling-phase, at the end of which the body diode stops conducting (Fig. 5.3a).

The transient starts with the first resonant phase (Fig. 5.3a), whose analytical description is given by (4.20). When the voltage voltage V_{Q3} reaches

V_{clamp}, the equivalent circuit becomes the one depicted in Fig.5.3b. At this instant, capacitor voltage and current are

$$\begin{aligned} V'_{C_{Q3},0} &= V_{\text{clamp}} \\ I'_{C_{Q3},0} &= \frac{V_{\text{clamp}}}{Z_0}\sqrt{\frac{V_{Q3,\text{on}}}{V_{\text{clamp}}} - 1}, \end{aligned}$$

while the current in the auxiliary winding parasitic inductance L_{aux} is zero. During the auxiliary diode conduction, the voltage and current across C_{Q3} are given by:

$$\begin{cases} v'_{C_{Q3}}(t) = V'_{Q3,\text{on}} + (V'_{C_{Q3},0} - V'_{Q3,\text{on}})\cos(\omega'_0) + Z'_0 I'_{C_{Q3},0}\sin(\omega'_0) \\ i'_{C_{Q3}}(t) = I'_{Q3,0}\cos(\omega'_0 t) + \frac{V'_{Q3,\text{on}} - V_{\text{clamp}}}{Z'_0}\sin(\omega' t) \end{cases} \tag{5.2}$$

where

$$\begin{aligned} V'_{Q3,\text{on}} &= \frac{\xi^2}{1+\xi^2}V_{Q3,\text{on}} + \frac{1}{1+\xi^2}V_{\text{clamp}} \\ \omega'_0 &= \omega_0 + \omega_{\text{sn}} = \omega_0\,(1 + 1/\xi) \\ Z'_0 &= \frac{1}{\omega'_0 C_{Q3}} \\ \omega_{\text{sn}} &\triangleq \frac{n_{aux}}{\sqrt{L_{aux}C_{Q3}}} \\ \xi &\triangleq \omega_0/\omega_{\text{sn}} = \sqrt{\frac{\lambda_{aux}}{\lambda}\left(\frac{(n+1)^2 + n^2\lambda}{n_{aux}^2}\right)} \end{aligned}$$

with $\lambda_{\text{aux}} = L_{\text{aux}}/L_\mu$. To quantify the effectiveness of the snubber, the maximum value of (5.2) has to be found and compared with the imposed clamp voltage V_{clamp}.

For this reason, in the following analysis V_{clamp} is normalized with respect to $V_{Q3,\text{on}}$ and $\beta = V_{\text{clamp}}/V_{Q3,\text{on}}$ and the steady state ringing is considered (i.e.

$I_{Q3,0} = 0$). The peak voltage during the second phase is

$$\hat{V}'_{Q3} = V'_{Q3,\text{on}} + \sqrt{{V'_{Q3,\text{on}}}^2 + (Z'_0 I'_{Q_3,0})^2} \tag{5.3}$$

while

$$I'_{Q_3} = \frac{V_{Q3,\text{on}}}{Z_0}\sqrt{1 - \left(\frac{V_{\text{clamp}}}{V_{Q3,\text{on}}} - 1\right)^2}. \tag{5.4}$$

Putting (5.4) in (5.3) and normalizing with respect to $V_{Q3,\text{on}}$ yields

$$\frac{\hat{V}'_{Q3}}{V_{Q3,\text{on}}} = \frac{\beta}{1+\xi^2} + \frac{\xi^2}{1+\xi^2}\left(1 + \sqrt{1 + \frac{\beta(2-\beta)}{\xi^2}}\right). \tag{5.5}$$

For two limit cases $L_{\text{aux}} \to 0$ and $L_{\text{aux}} \to \infty$, (5.5) yields

$$\lim_{\xi \to 0} \hat{V}'_{Q3} \to V_{\text{clamp}}$$

$$\lim_{\xi \to \infty} \hat{V}'_{Q3} \to 2V_{Q3,\text{on}}.$$

These two expressions respectively agree with the ideal snubber operation disclosed above, and with the snubber-less operation described in [96]. If the clamp voltage is selected next to the $V_{Q3,\text{on}}$ ($\beta \to 1$), then (5.5) becomes:

$$\frac{\hat{V}'_{Q3}}{V_{Q3,\text{on}}} = 1 + \frac{\xi}{\sqrt{1+\xi^2}} = 1 + \frac{Z_0}{Z'_0} \tag{5.6}$$

which shows that the clamp will always reduce the peak voltage, because $Z_0 < Z'_0$ even if the auxiliary winding parasitic inductance is greater than L_R. Depending on the converter design (i.e. n,λ and V_{clamp}), a suitable value for λ_{aux} can be chosen from (5.3).

Equivalent Circuits

In the previous section the dynamics of the second phase is considered with respect to the first phase. The transient can be better understood referring to

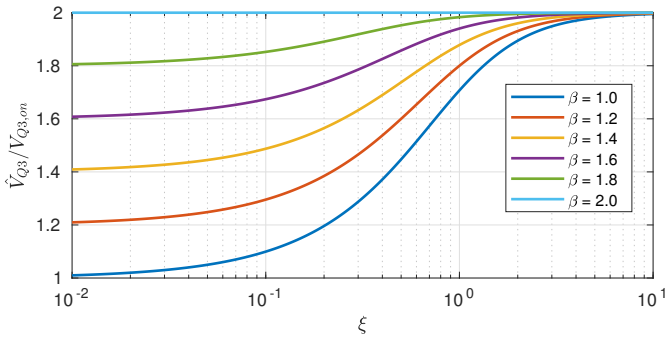


FIGURE 5.4: Q_3 voltage stress normalized with rispect to on-voltage as a function of parameter ξ.

the two equivalent circuits in Fig. 5.5. In both circuits, C_{Q3} sees an equivalent

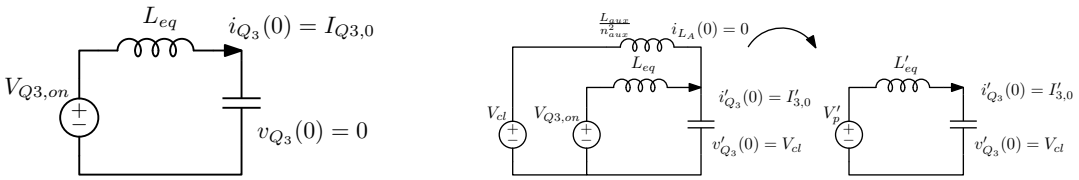


FIGURE 5.5: Equivalent circuits of the first (a) and second phase (b) of the transient.

inductance. In the first phase it is L_{eq} (4.21) and when the snubber starts conducting, an additional branch (Fig. 5.5b) appears. Applying thevenin equivalent circuit the effective inductance $L'_{\text{eq}} = L_{\text{eq}} \parallel L_{aux}/n^2$ and $V'_{Q3,\text{on}}$ can be calculated.

State Plane Analysis

Another way to look at the resonant transient is the state plane analysis. The state plane consist is a cartesian plane where C_{Q3} voltage and current are represented. Expressions (4.20) and (5.2) are normalized with respect to the normalizing voltage $V_N \triangleq V_{Q3,\text{on}}$ and normalizing current $I_N \triangleq V_{Q3,\text{on}}/Z_0$ yielding for the first phase:

$$\begin{cases} \nu_3 = 1 - \cos(\omega_0) + \jmath_{3,0} \sin(\omega_0 t) \\ \jmath_3 = \jmath_{3,0} \cos(\omega_0 t) + \sin(\omega_0 t) \end{cases} \tag{5.7}$$

where $\nu_3 \triangleq v_{Q_3}(t)/V_N$ and $\jmath_3 \triangleq i_{Q_3}(t)/I_N$. For the second phase, calling $\nu'_3 \triangleq v'_{Q_3}/V_N$, $\jmath'_3 = i'_{Q_3}/I_N$ gives:

$$\begin{cases} \nu'_3 = \nu'_{Q3,on} + (\nu_{cl} - \nu'_{Q3,on})\cos(\omega'_0 t) + \frac{\xi}{\sqrt{1+\xi^2}}\jmath'_{3,0}\sin(\omega'_0 t) \\ \jmath'_3 = -(\nu_{\rm cl} - \nu'_{Q3,on})\frac{\sqrt{1+\xi^2}}{\xi} + \jmath'_{3,0}\cos(\omega'_0 t) \end{cases} \tag{5.8}$$

where $\nu'_{Q3,on}$ and $\nu_{\rm cl}$ are the normalize quantities of $V'_{Q3,\rm on}$ and $V_{\rm clamp}$.

The phase portrait is obtained by squaring and adding the voltage and current equations. In this way the dependence from the time disappears. The phase portrait of (5.7) is

$$(\nu_3 - 1)^2 + \jmath_3^2 = 1 + \jmath_{3,0}^2 \tag{5.9}$$

and represents a circle of center $\mathcal{C} = (1\,;\,0)$ and radius $r = \sqrt{1+\jmath_{3,0}}$. Normalizing (5.8) leads to

$$(1+\xi^2)(\nu'_3 - \nu'_{Q3,on})^2 + \xi^2\jmath'_3 = \xi^2(1+\jmath_{3,0}^2) - \frac{\xi^2}{1+\xi^2}(\nu_{\rm cl}-1)^2 \tag{5.10}$$

which is the expression of an ellipse. The center of the ellipse is $\mathcal{C}' = (\nu'_{Q3,on}\,;\,0)$, while

$$\begin{aligned} a &= \frac{\xi}{\sqrt{1+\xi^2}}\sqrt{1+\jmath_{3,0}^2 - (\nu_{\rm cl}-1)^2(1-\xi^2)} \\ b &= \frac{1}{\sqrt{1+\xi^2}}\sqrt{\frac{1+\jmath_{3,0}^2}{1+\xi^2} - (\nu_{\rm cl}-1)^2} \\ e &= \frac{1}{\sqrt{1+\xi^2}} \end{aligned}$$

are respectively the major and minor axis and the eccentricity. Note that this ellipse degenerate in a circle only when $\xi \to \infty$. Without snubber the

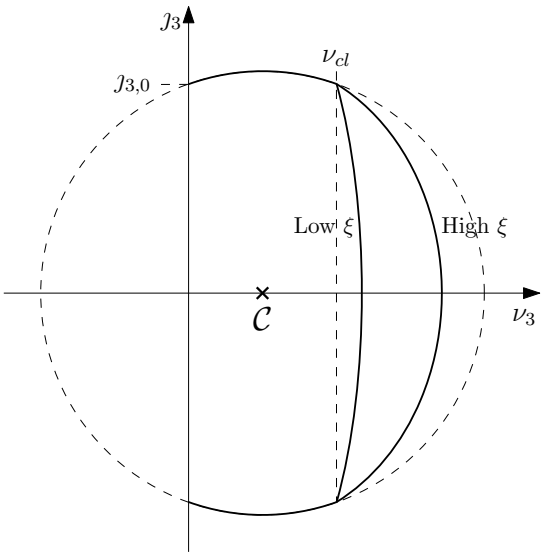


FIGURE 5.6: Phase portrait where the dashed circle represents the no-snubber transient, while the two ellipse arc refer to a low and a high value of ξ.

normalized peak voltage is given by (5.9) evaluated for $\jmath_3 = 0$

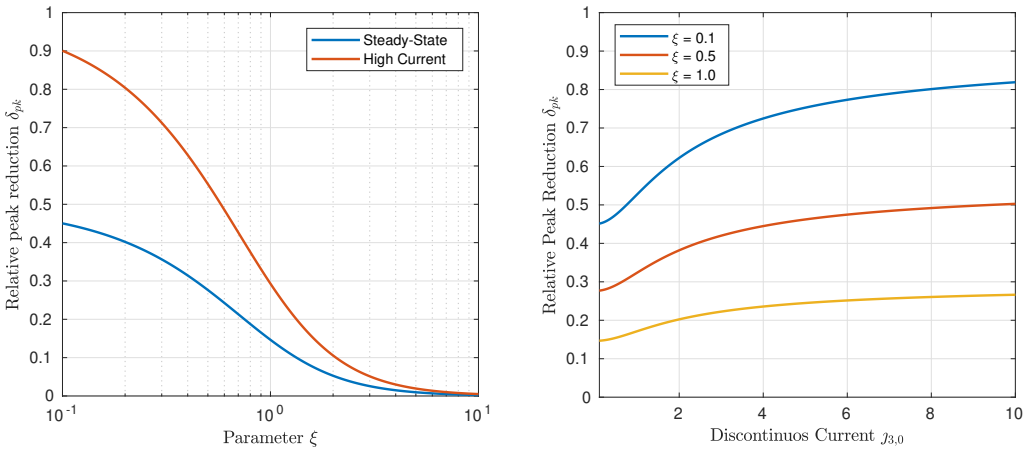
$$\hat{v}_3^{No-SN} = 1 + \sqrt{1 + \jmath_{3,0}^2}. \tag{5.11}$$

while in case of snubber employment the peak voltage is

$$\hat{v}_3^{SN} = \frac{\xi^2}{1+\xi^2} + \frac{\nu_{\rm cl}}{1+\xi^2}\sqrt{1 + \jmath_{3,0}^2 - (\nu_{\rm cl}-1)^2(1-\xi^2)}. \tag{5.12}$$

These expressions are valid for a general value of $V_{\rm cl}$. The clamp voltage must be higher than $V_{Q3,\rm on}$ because otherwise the snubber will conduct also during on-state causing increased losses. Ideally the clamp voltage should be slightly higher than $V_{Q3,\rm on}$. For this reason, it is of interest to evaluate (5.12) in the case $\nu_{\rm cl} = 1$:

$$\hat{v}_3^{SN*} = 1 + \frac{\xi}{\sqrt{1+\xi^2}}\sqrt{1 + \jmath_{3,0}^2}$$



(a) (b)

FIGURE 5.7: Relative peak reduction: steady and high current case as a function of ξ (a) and as a function of the discontinuos current $\jmath_{3,0}$ (b)

From which the relative peak reduction can be calculated:

$$\delta_{pk} \triangleq \frac{\nu_3^{\hat{No-SN}} - \nu_3^{\hat{SN}*}}{\nu_3^{\hat{SN}*}} = \left(1 - \frac{\xi}{\sqrt{1+\xi^2}}\right) \frac{\sqrt{1+\jmath_{3,0}^2}}{1+\sqrt{1+\jmath_{3,0}^2}}. \tag{5.13}$$

Two limit cases of (5.13) are of interest, i.e. the steady state case ($\jmath_{3,0} = 0$) and the high current case ($\jmath_{3,0} \gg 1$) which yield

$$\delta_{pk} = \begin{cases} \frac{1}{2}\left(1 - \frac{\xi}{\sqrt{1+\xi^2}}\right) & \text{in steady state} \\ \left(1 - \frac{\xi}{\sqrt{1+\xi^2}}\right) & \text{with high discontinuos current} \end{cases} \tag{5.14}$$

Fig. 5.7a shows (5.14). The effectiveness of the snubber quickly drops if $\xi \geq 1$, but the high current reduction is always double of the steady state ringing reduction. The advantages of the snubber become more and more relevant as the discontinuous current increases.

The proposed snubber does not require and additional core and can be freely designed to limit voltage spike, but care must be taken with its parasitics in order to keep it effective. Moreover a custom inductor three-winding coupled inductor must be wound. For these reasons, in the next section a

control based solution is proposed, which does not require additional hardware and which is suitable for an integrated solution.

5.2.4 Coupled Inductor Design

The analysis carried in the previous sections lets some design guidelines to be drawn. In order to maximize the advantages offered by the topology and the snubber effectiveness, a low leakage-inductance inductor has to be designed. The cores considered in the following are POT 7, 9, 11 and 14 [103]. In the SCTI converter the primary winding experiences a zero average current, while the secondary winding has to withstand the total output current plus a non negligible ripple. This observation suggests that the secondary winding resistance should be minimized, while the primary resistance can have a higher value. The secondary winding should have the minimum number of windings, while maintaining a good coupling with the primary. For these reasons the winding schemes in Fig. 5.8 are considered.

5.2.5 Inductor Design Optimization

In order to optimize the inductor design, a finite element analysis is performed. Because of the axial symmetry of the POT core, a simulation can be performed through [104], a free-software which solves 2D electromagnetic problems. The problem design and solution can be automated through several programming languages – Matlab® API is used in this case.

From (5.1) and selecting V_{clamp} equal to $V_{Q3_{on}} \simeq 7.3$ V, $n_{aux} \simeq 8$ is calculated. In the following an inductor with $n = N_1/N_2 = 5$ and $n_{aux} = N_{aux}/N_2$ and $L_\mu = 10$ µH is designed. POT cores with all the air gaps available in [103] are considered. Core manufacturers provide parameter A_L through which

$$N_1 = \sqrt{\frac{L_\mu}{A_L}}$$

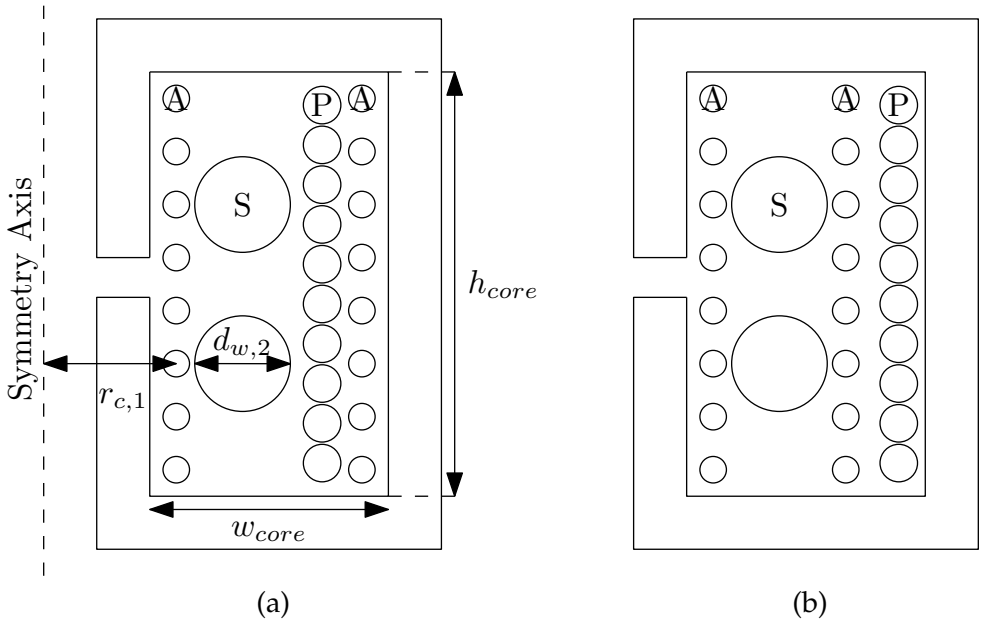


FIGURE 5.8: Two proposed winding schemes: primary (P), secondary (S) and auxiliary (A) windings are shown.

can be calculated. From this follows $N_2 = nN_1$ and $N_3 = n_{aux}N_2$. To select the diameter of the three winding wires, the *rms* currents across the three windings $I_{RMS,1}$, $I_{RMS,2}$ and $I_{RMS,3}$ are estimated through a Matlab® script and the conduction losses

$$P_{\text{cond}} = R_1 I_{RMS,1}^2 + R_2 I_{RMS,2}^2 + R_3 I_{RMS,3}^2$$

are minimized. Considering the axial symmetry, the DC resistances R_1, R_2 and R_3 can be estimated through:

$$R_w = n_w \rho_{\text{Cu}} \frac{r_{\text{c}}}{2d_w^2} \tag{5.15}$$

where r_{c} is the horizontal distance between the center of the winding and the symmetry axis, while d_w is the diameter of the winding cross-section (refer to Fig. 5.8a). The optimization problem becomes

$$\begin{aligned} \underset{d_{w,1},d_{w,2},d_{w,3}}{\arg\min} \quad & \sum_{i=1}^{3} \rho_{\mathrm{Cu}} n_i \frac{r_{\mathrm{c,i}}}{2d_{w,i}^2} I_{RMS,i}^2 = \sum_{i=1}^{3} \frac{K_i}{d_{w,i}^2} \\ \text{subject to} \quad & \sum_{i=1}^{3} d_{w,i} = k_f w_{\mathrm{core}} \end{aligned} \tag{5.16}$$

where ρ_{Cu} is the copper resistivity, w_{core} is the core width and k_f the fill-factor. The solution to (5.16) is

$$d_{w,i}^{\mathrm{opt}} = k_f w_{\mathrm{core}} \frac{\sqrt[3]{K_i}}{\sum_{j=1}^{3} \sqrt[3]{K_j}}. \tag{5.17}$$

The diameter of the windings is then selected as

$$d_{w,i} = \min(d_{w,i}^{\mathrm{opt}}, h_{\mathrm{core}}/n_i),$$

with h_{core} the height of the core window. FEMM program allows the self and mutual inductances to be evaluated. In order to obtain an equivalent 3-winding cantilever model [105] the approach outlined in [106] is followed. In this way magnetizing and leakage inductances are evaluated and $\lambda = L_R/L_\mu$ and $\lambda_{aux} = L_{aux}/L_\mu$ are calculated.

The three main quantities to be considered are $\lambda, \lambda_{\mathrm{aux}}$ and the secondary resistance R_{sec}. Primary winding parasitic resistance usually has the highest value, but the *rms* current value is reduced because of the zero average current. Auxiliary winding only carries only the ringing current and its effect on the conduction losses can be neglected. In order visualize the three parameters, a radar chart can be employed. As an example the plot of the three parameters of the POT9 core normalized to the maximum value is shown in Fig. 5.9. The legend shows the core number followed by the air gap (e.g. POT9/003 is a POT9 core with 3 mm air gap). In this plot, the core with best performance has smallest area. Fig. 5.9 reveals that the most suitable air gap for the POT9 core is 4 mm. In Fig. 5.10 the flux density of the core with smallest (POT11/003)

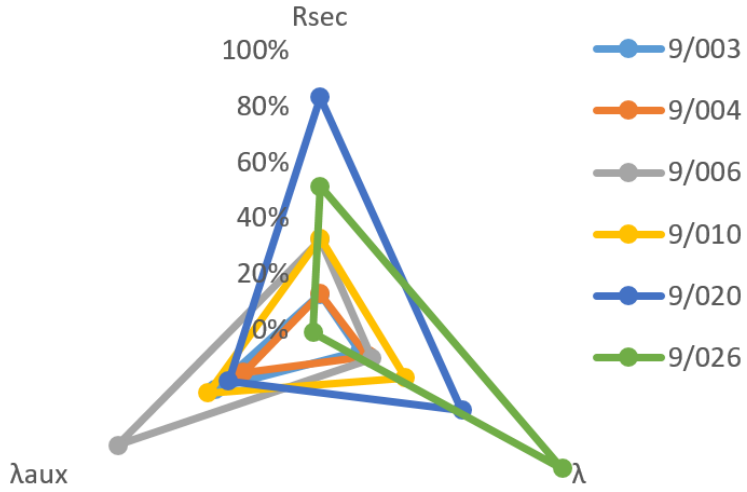
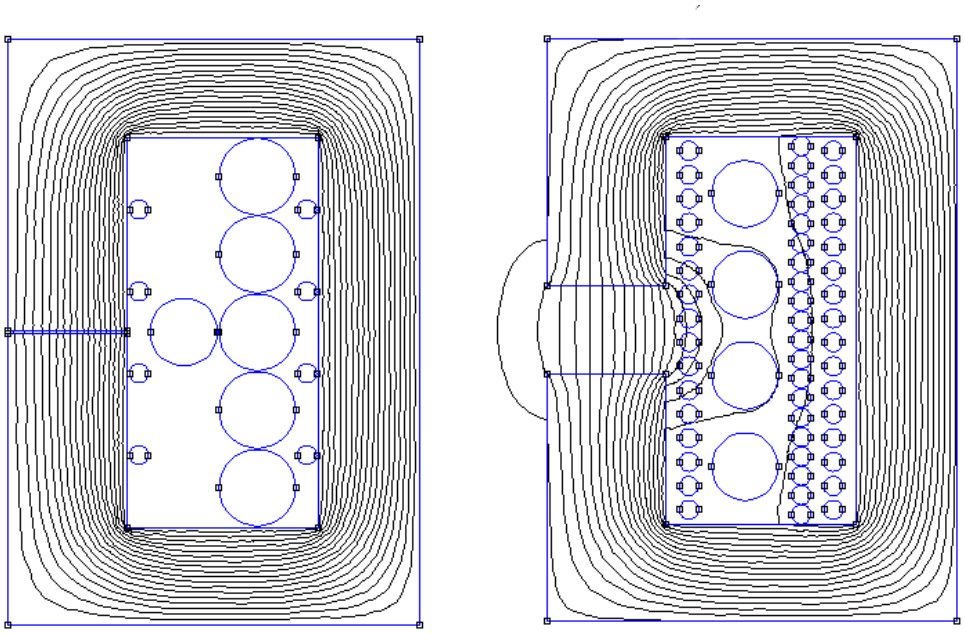


FIGURE 5.9: Radar chart of λ, λ_{aux} and R_{sec} for a POT9 core.



(a) (b)

FIGURE 5.10: Flux density plot generated by [104] for (a) 11/003 and (b) 11/100 cores.

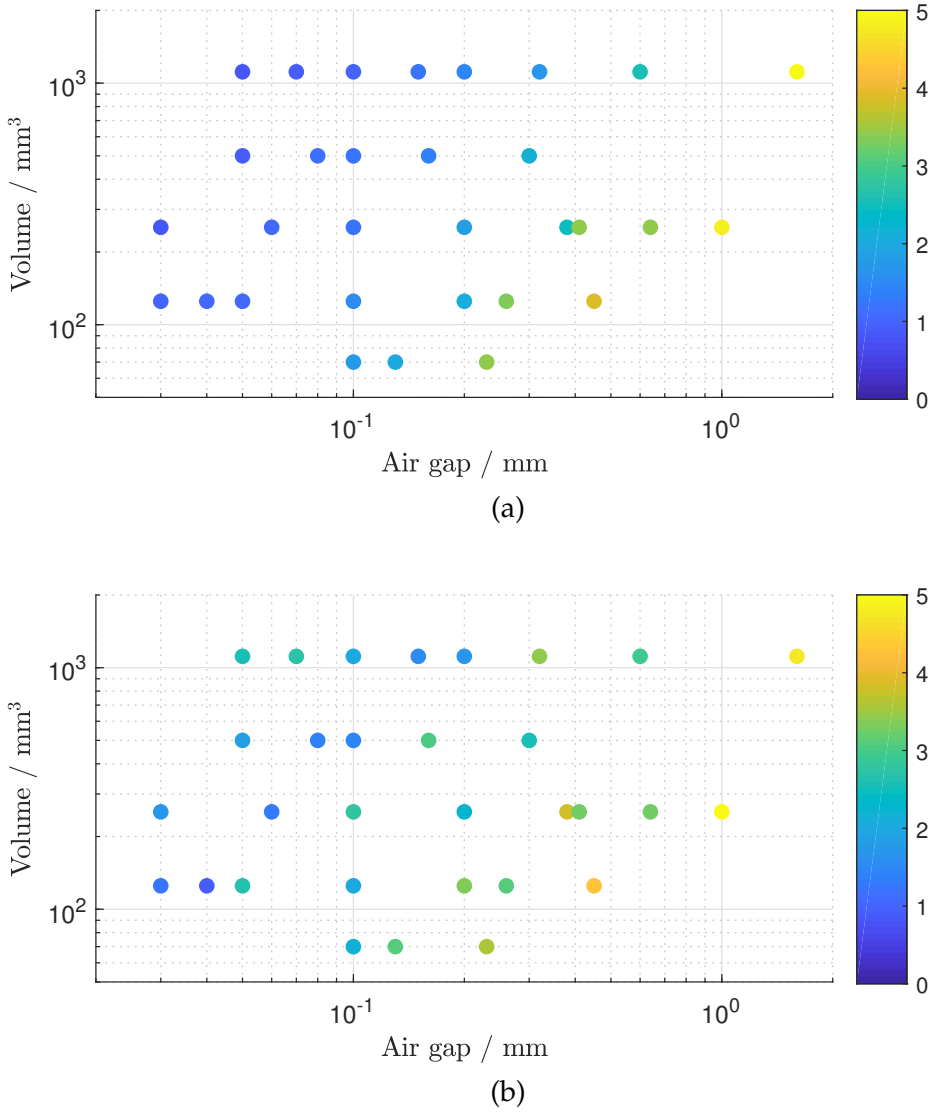


FIGURE 5.11: Parameters (a) λ, and (b) λ_{aux} as a function of both volume and air gap (first winding scheme).

and greatest (POT11/100) radar chart area are shown. Bigger air gap results in increased winding number and hence losses.

The effect of air gap and volume can be better understood from Fig. 5.11, which refers to the first winding arrangement (Fig. 5.8a). Fig. 5.11 clearly shows that and lower air gap improves the coupling. To verify which winding arrangement maximizes the proposed snubber effectiveness, the plot of (5.3) is required. A ξ value lower than one indicated an effective snubber action, hence Fig. 5.11 indicates that the second winding scheme (Fig. 5.8b) is more

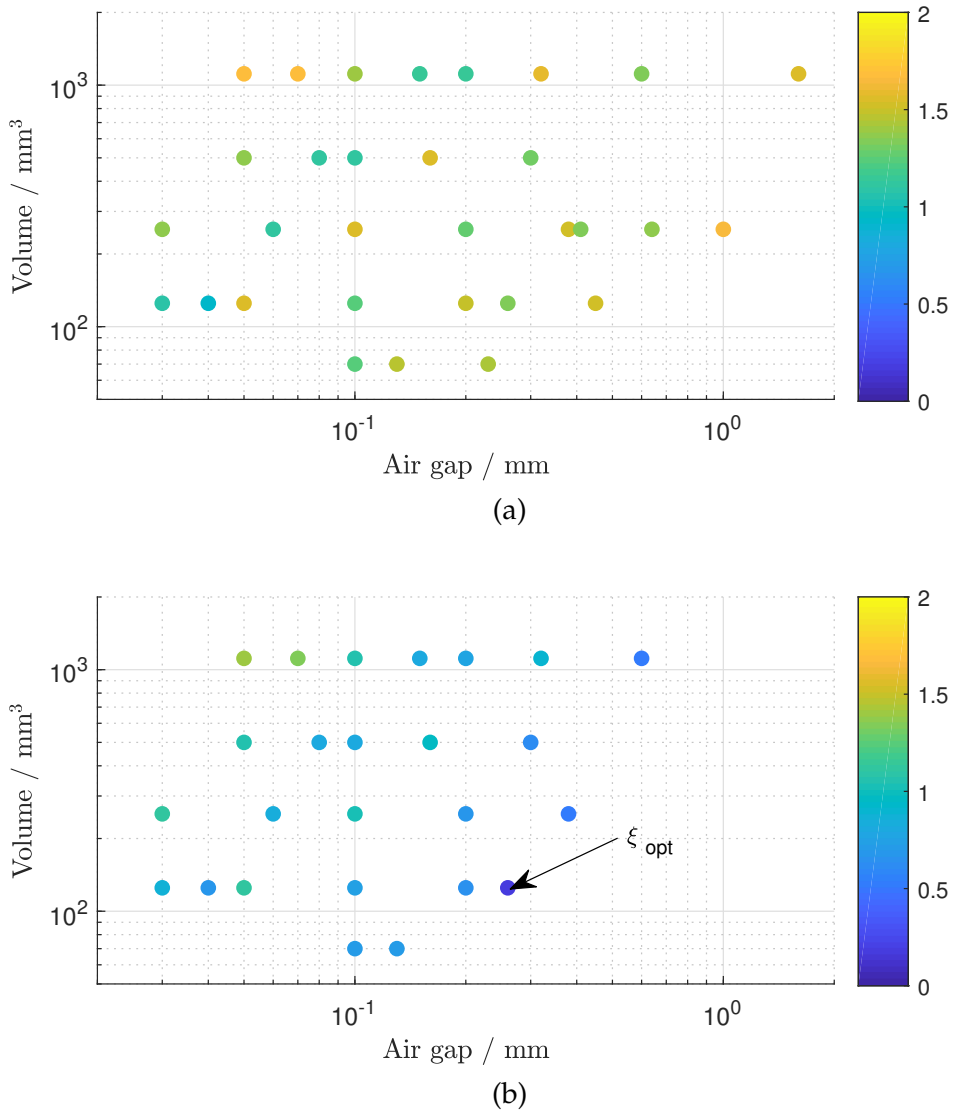


FIGURE 5.12: ξ value for the (a) first and (b) second winding scheme.

suitable.

5.2.6 Simulation Results

To test the snubber operation, a Matlab/Simulink® PLECS® closed-loop simulation of a SCTI converter with a digital PID controller is performed. A switching frequency of $f_s = 200\,\text{MHz}/1024 = 195.4\,\text{kHz}$ is selected. The inductor model comprises magnetizing inductance, leakage inductance and resistance for the three windings. Capacitor C_R is selected in order to move

TABLE 5.1: Inductor parameters used in the simulations of Fig. 5.13.

Parameter	Value
L_μ	9 µH
L_R	504 nH
L_{R2}	20 nH
R_{pri}	160 mΩ
R_{sec}	17 mΩ

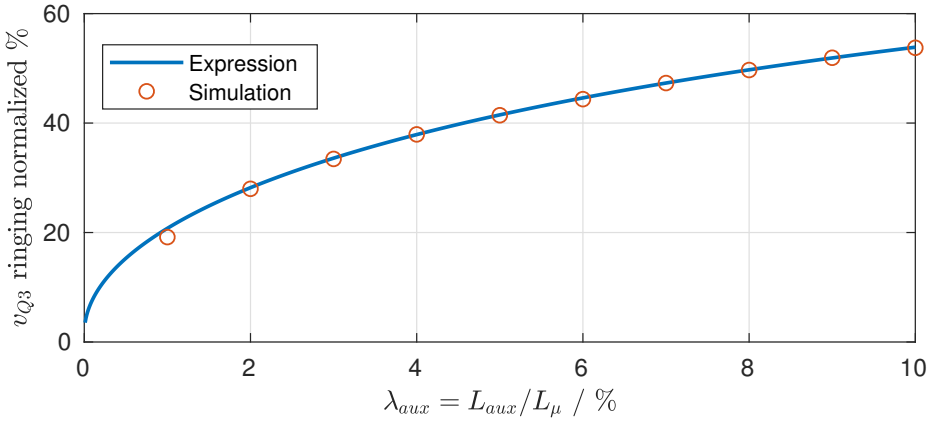


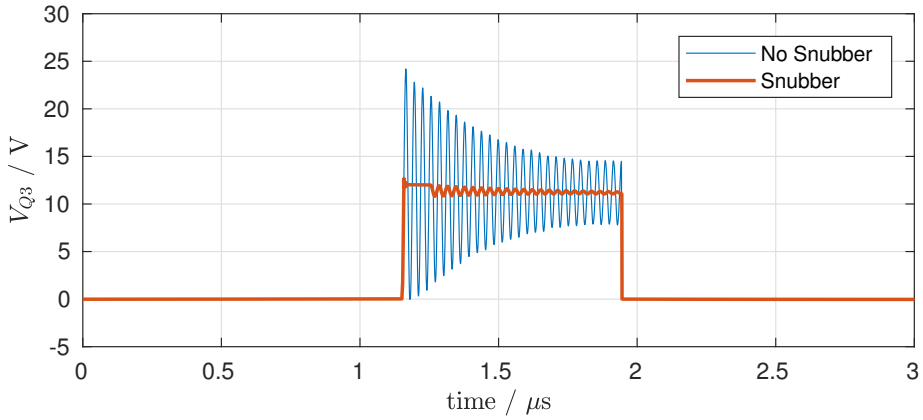
FIGURE 5.13: Peak overshoot of V_{Q3} normalized to the snubber-less peak value

its resonance with the parasitic inductance L_R lower than the switching frequency:

$$C_R \gg \frac{1}{(2\pi f_s)^2 L_R}. \tag{5.18}$$

The output capacitance C_o is designed to have a ripple less that 1.5% and the calculation of its value is based on an estimation of the secondary winding current ripple. All the MOSFETs are modeled by and on-resistance of 17 m■, while the output capacitance $C_{ds3} = 1$ nF is added to Q_3 only in order to decrease the simulation time.

To verify (5.5) a parametric simulation is performed using an inductor with parameters reported in Tab. 5.1, and for increasing values of the auxiliary winding leakage inductance. The peak of the steady state ringing is shown Fig. 5.13 along with the peak predicted by (5.5). For very large leakage inductances, the voltage stress tends to become equal to the snubber-less operation, while the case $L_{\text{aux}} = 0$ coincides with the ideal snubber operation.



(a)

FIGURE 5.14: V_{Q3} ringing with and without the proposed snubber.

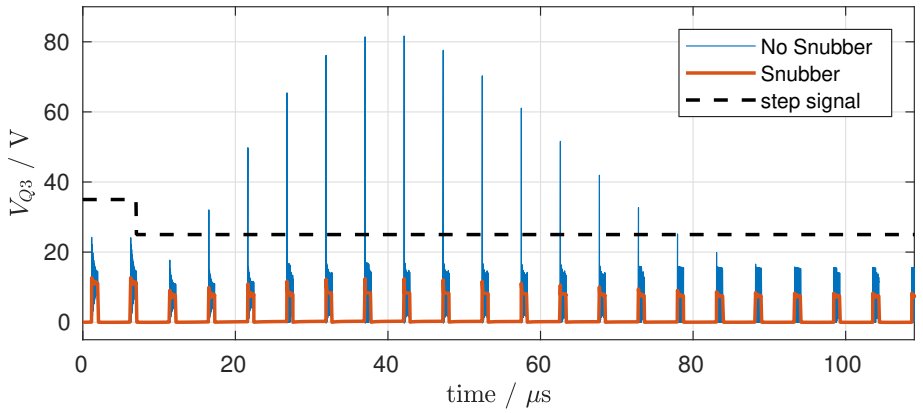


FIGURE 5.15: V_{Q3} ringing with and without the proposed snubber when a input voltage step from 72 V to 48 V is applied.

The maximum value for L_{aux} allowed can be found through Fig. 5.4.

Next two simulations with the core which has the lowest value of ξ (i.e. POT9/004, shown in Fig. 5.12 as ξ_{opt}) are performed, the first with the snubber in place, while the second with the auxiliary winding disconnected. The result is shown in Fig. 5.14a. The snubber effectively reduces the ringing.

Next, an input voltage step is simulated and V_{Q3} with and without snubber is measured and shown in Fig. 5.15 Without snubber Q_3 voltage stress reaches 80 V, while with the proposed solution V_{Q3} remains below 25 V, thus enabling the use of low-voltage rating devices (e.g. 30 V MOSFETs).

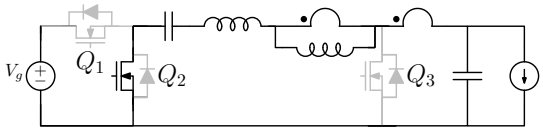


FIGURE 5.16: Intermediate topological state IDLE introduced by the approach during critical switching cycles.

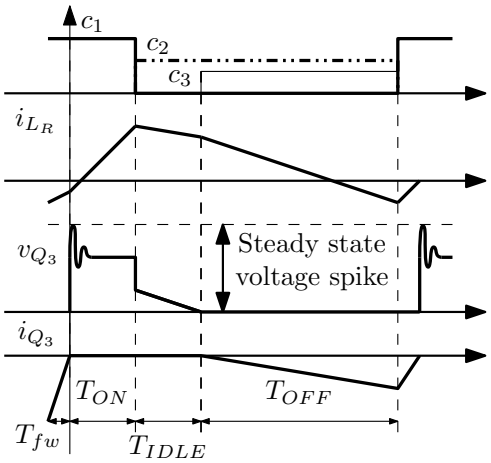


FIGURE 5.17: Operation of the proposed approach during a critical switching cycle.

5.3 Control-Based Solution

The over-voltage event discussed in section 4.5 occurs when condition (4.12) for ZVS turn-off of Q_3 is not satisfied. Therefore the condition for ZVS turn-off Q_3 is also the condition for safe turn-off of Q_3. In summary:

$$\begin{cases} \dfrac{\mathrm{d}i_{Q_3}}{\mathrm{d}t}(T_{\mathrm{ON}}) > 0 \quad \text{then } i_{Q3}(T_{\mathrm{OFF}}) > 0 \\ \dfrac{\mathrm{d}i_{Q_3}}{\mathrm{d}t}(T_{\mathrm{ON}}) < 0 \quad \text{then } i_{Q3}(T_{\mathrm{OFF}}) < 0 \end{cases} \tag{5.19}$$

This means that condition for safe switching of Q_3 can be tested *before* entering the OFF state directly from sign of $di_{Q_3}/dt|_{t=T_{ON}}$ or, equivalently by evaluating condition (4.13) at the same instant. The proposed technique introduces an additional topological state in between states ON and OFF, called IDLE and illustrated in Fig. 5.16, and which only occurs in those switching cycles that would cause the overvoltage problem. Consider Fig. 5.17: For $t = T_{ON}$, if the condition on v_{C_R} is not satisfied the proposed technique turns on Q_2 but

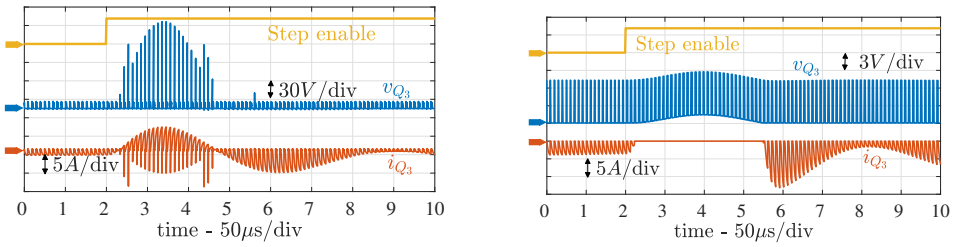


FIGURE 5.18: Simulated transient due to a 20%-to-30% duty cycle variation with conventional modulation (a) and with the proposed approach (b).

leaves Q_3 temporarily off, setting the topology in IDLE state. In this condition Q_3 and its body diode are both off and V_{Q_3} decreases. Consequently v_{C_R} increases, due to positive magnetizing current, until condition (4.13) becomes true. At this point Q_3 is turned on and the SCTI enters the OFF state. Notice that, in steady-state, the proposed approach is entirely inactive, and does not interfere with the normal converter operation. At the same time, the IDLE state can be introduced for several consecutive switching cycles during a transient, to prevent hard turn-off of Q_3.

Fig. 5.18 reports the simulation of a transient induced in the converter described by parameters of Tab. 4.1 by an abrupt duty cycle step from 20% to 30%. With conventional control technique (Fig. 5.18a), a voltage spike clearly appears across Q_3. When the proposed approach is enabled, the transient causes the proposed technique to intervene, preventing current i_{Q_3} from becoming positive and eliminating the voltage spike across Q_3.

5.3.1 Practical implementation of the Control Technique

Directly monitoring condition (4.13) would present some technical challenges, as it would involve an accurate differential sensing of v_{C_R}. Presence of high-frequency common-mode voltage at the terminals of C_R would further complicate the sensing. However, (4.13) can be equivalently expressed by the

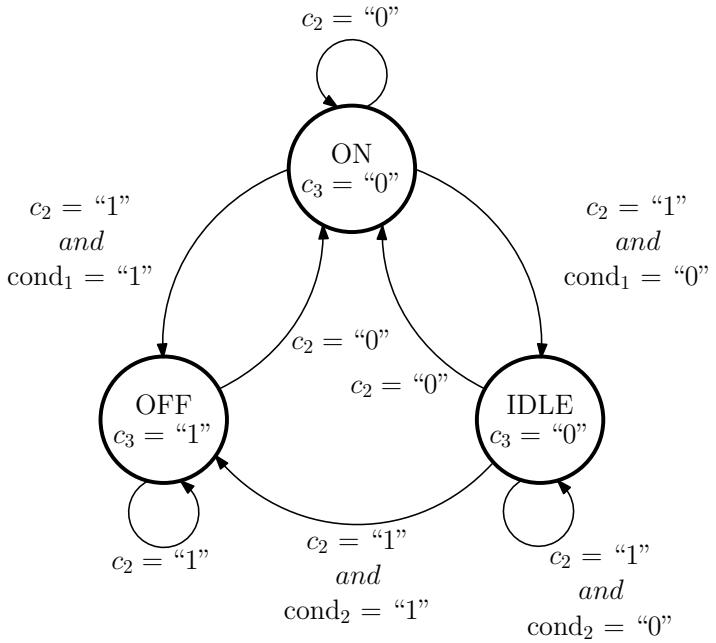


FIGURE 5.19: FSM state transition diagram of the proposed technique.

following two conditions on v_{Q_3}

$$v_{Q_3} \leq \begin{cases} kV_g & \text{during } T_{ON} \quad (\text{cond}_1) \\ 0 & \text{during } T_{IDLE} \quad (\text{cond}_2), \end{cases} \tag{5.20}$$

where

$$k \triangleq \frac{1}{n+1} \frac{1}{1+\lambda \left(\dfrac{n}{n+1} \right)^2} \left(= \frac{\mathrm{d}M_0}{\mathrm{d}d} \right) \approx \frac{1}{n+1}, \tag{5.21}$$

under the approximation (4.8). With this equivalent formulation, the system enters the IDLE state if $v_{Q_3} < kV_g$ at the end of the on-time. The IDLE state is then maintained either until $v_{Q_3} \leq 0$, or until the end of the switching period, whichever comes first. In the first case the system is brought into the OFF state, while in the second case a new switching period starts with the converter in the ON state. These steps are summarized by the FSM state transition diagram illustrated in Fig. 5.19. The possible topological sequences of the technique, according to the proposed approach, are sketched in Fig. 5.20.

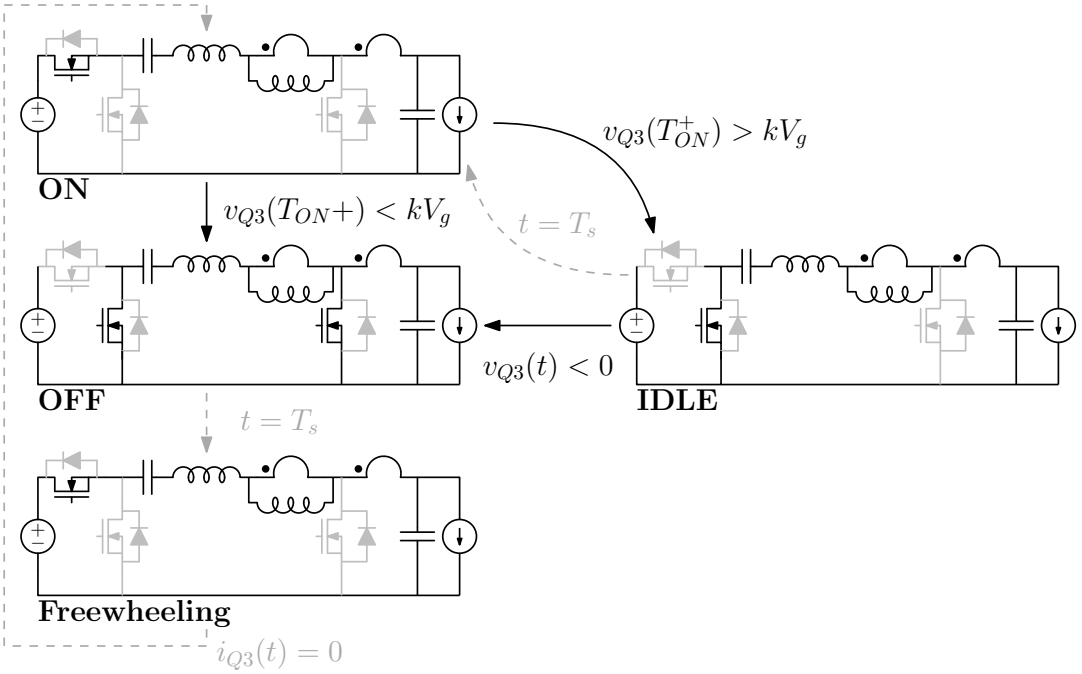


FIGURE 5.20: Simplified diagram of the technique operation during a single switching cycle, where black transitions are due to the proposed technique.

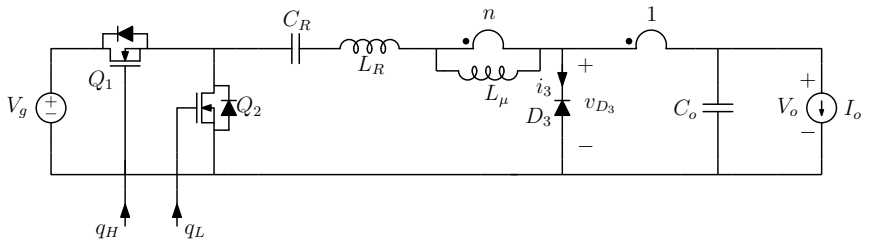


FIGURE 5.21: SCTI Converter with an ideal diode in place of Q_3.

5.3.2 Relation Between the Proposed Technique and Diode Emulation of Q_3

The over-voltage issue outlined in Section III occurs only when Q_3 is a *synchronous* rectifier, i.e. with a controlled device capable of carrying current of both signs. If a diode were employed in place of Q_3, as in Fig. 5.21, no over-voltage would result from a transient condition. The behavior of the converter operated with the proposed technique is equivalent of the operation of the converter with a near-ideal diode. First it is shown that the *steady-state* converter operation is not altered when Q_3 is replaced by an ideal diode D_3. The voltage v_{D3} is a linear combination of V_{CR}, V_o and V_g, hence it is piecewise

constant (SRA). Moreover

$$\bar{v}_{D3} = D_{\text{on}} V_{D3,ON} + D_{\text{off}} V_{D3,OFF} + D_{\text{fw}} V_{D3,FW} = V_o$$

and since $V_{D3,OFF} = V_{D3,FW} = 0$, $V_{D3,ON} = V_o / D_{\text{on}}$, where D_{on} is given in (4.9). At the beginning of T_{OFF} the voltage across D_3 undergoes a step change

$$\Delta V_{D3} = -\frac{V_g(n+1)}{n^2\lambda + (n+1)^2} = -\frac{V_o}{M}\frac{M_0}{D} \tag{5.22}$$

In order to let the diode turn on, thus entering the OFF State, it is required that $V_{D3,ON} + \Delta V_{D3} \leq 0$. Solving the inequality leads to

$$\begin{aligned} V_{D3,ON} = \frac{V_o}{D_{ON}} = \frac{V_o}{M}\left(M + \left(\frac{1}{D} - 1\right) M_0\right) &\leq -\Delta V_{D3} = \frac{V_o}{M}\frac{M_0}{D} \\ M &\leq M_0 \end{aligned} \tag{5.23}$$

where M_0 is defined in (4.6), and $M_0 \geq M$ for every $I_0 \neq 0$ has been previously proven. Hence the converter operated with ideal diode behaves like the converter operated with an ideal MOSFET.

During *transient* events, at the beginning of the OFF phase the diode may or may not immediately conduct. If it turns on, then i_3 is necessarily negative. Otherwise the diode remains in cut-off operation ($i_3 = 0$), reproducing the IDLE state of the proposed technique until i_3 becomes negative. Consequently, the same effects of the proposed technique could be achieved by sensing v_{D_3} and by turning on the switch when a negative voltage is sensed. This would result in condition 2 in (5.20).

The proposed implementation presents nonetheless a number of advantages over such simple attempt to diode emulation. First of all, in steady-state the output of the comparator which performs this operation would have to change its logical output immediately after T_{ON}. Any propagation delay would however cause the body diode of Q_3 to conduct and increase the losses.

In addition, waveform V_{Q_3} presents ringing close to the switching instants, which would pose the additional problem of avoiding commutation chattering. The proposed technique solves these issues by performing a predictive comparison *before* the switching instant, when V_{Q_3} has already settled and the delay of the comparator does not represent a critical issue.

5.3.3 Closed Loop Control

The proposed technique acts on a cycle basis and does not interfere with steady-state operation. Furthermore, transients leading to the intervention of the approach, and therefore to the introduction of the IDLE state, tend to be of large-signal nature. In other words, the *small-signal* properties of the converter are not affected by the proposed provision.

To verify its operation in closed loop, a digital controller is implemented on a commercial FPGA board. A fast ($f_c \simeq f_s/20$) digital controller is considered in order to test the proposed technique behavior for a closed loop system.

To implement the controller, an estimation of the loop gain is needed. A PLECS simulation is performed, injecting a small duty cycle perturbation at a test frequency f_{test}. Then FFT is performed on both duty cycle and output voltage and the ratio between the spectrum of these two signals at the test frequency is calculated, giving and estimation of $\hat{v}_o/\hat{d}$. The result for the frequencies of interest is shown in Fig. 5.22. In the same figure, the experimental frequency response of the converter prototype described in Section 5.3.4 is also superimposed, confirming the validity of the simulations. The experimental measurements are obtained through a schema similar to Fig. 5.23. A square wave of test frequency f_T obtained from digital counter is added the steady-state duty cycle and delivered to the output pin of the FPGA board. Then both duty cycle and output voltage are sensed through an oscilloscope and the waveforms are saved for the post-processing. A

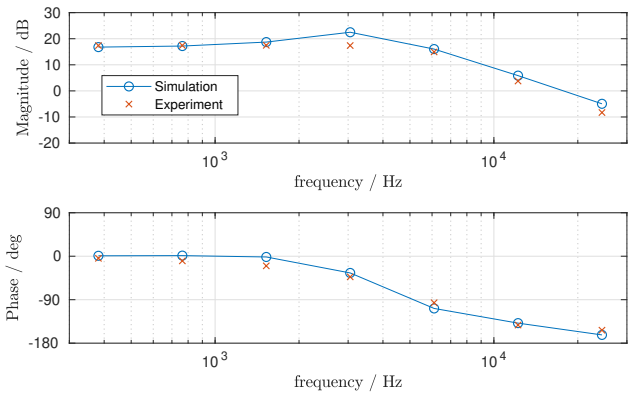


FIGURE 5.22: Experimental (blue crosses) and simulated (red circles) duty cycle-to-output voltage frequency response obtained via perturbation injection.

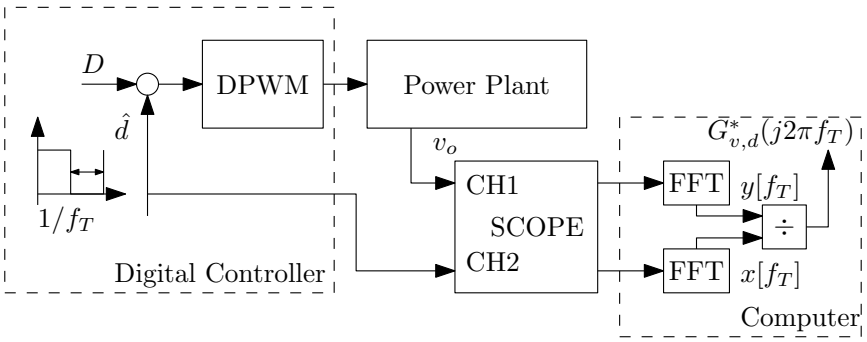
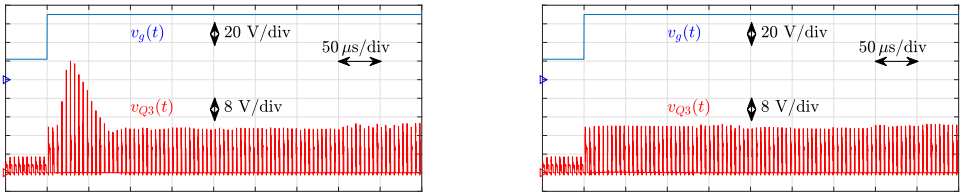


FIGURE 5.23: Experimental setup for the transfer function measurement.

MATLAB®script is used to evaluate the FFT of both signals and to extract the spectrum component at f_T. The ratio between the two spectral components gives the experimental estimated transfer ratio $G^*_{v,d}(j2\pi f_T)$.

Simulations show the presence of a resonance locate at about 3 kHz, but which depends on the value of C_R, L_R, L_μ and n. A PID controller can be employed when the crossing frequency is chosen higher than the resonance frequency. For the simulation and the experimental setup a digital PID controller is implemented in MATLAB® Simulink® with crossing frequency $f_c \simeq 10$ kHz and phase margin $m_\phi \simeq 60°$. A simulated input voltage step is shown in Fig. 5.24. With conventional control the line step causes a big voltage spike, while it does not appear with the proposed technique enabled. The FMS does not interfere with the controller operation, which performs as if the



(a) (b)

FIGURE 5.24: Closed loop converter simulation for an input voltage step from 22 V to 70 V with (a) a conventional controller and (b) with the proposed approach.

converter were synchronously operated. Note that this simulation requires the inclusion of Q_3 parasitic capacitance, which causes a loss of speed and reliability for the simulation, if the proposed technique is not implemented.

5.3.4 Experimental Results

Conditions (5.20), which implement the proposed control technique for avoiding the over-voltage issue at the drain of Q_3, are realized with two separate comparators, while the subsequent logic which processes their outputs is here implemented in the commercial FPGA board. Since V_g can be as high as 90 V in the target application, the first condition of (5.20) is scaled by an attenuation factor α,

$$\alpha v_{Q_3} \leq \alpha k V_g. \tag{5.24}$$

As for the second inequality in (5.20), for the same reasons it is also scaled by an attenuation factor β, and level-shifted by a dc term $(1-\beta)V_{bias}$ in order to allow a single-supply implementation of the technique,

$$\beta v_{Q_3} + (1-\beta)V_{bias} \leq (1-\beta)V_{bias}. \tag{5.25}$$

The implementation scheme of the two modified inequalities of system (4.12) is shown on Fig. 5.25. In the implementation, a resistance R^* is also included

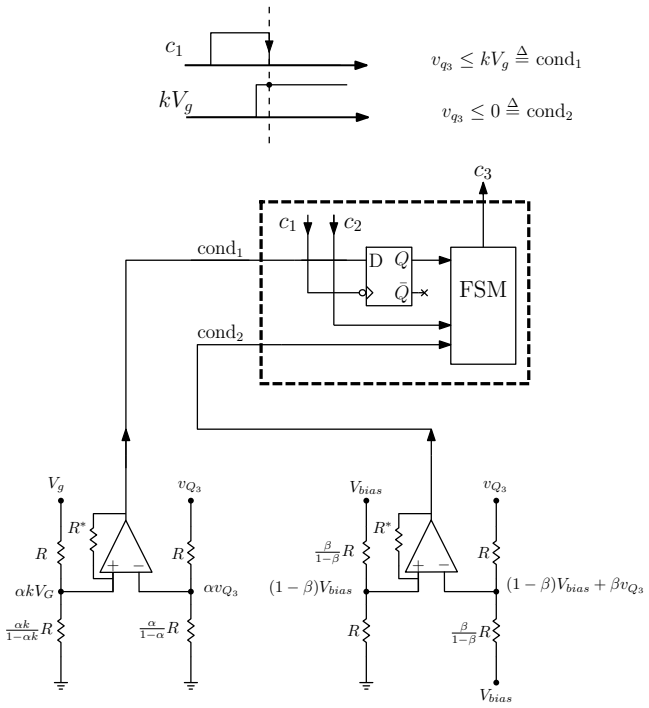
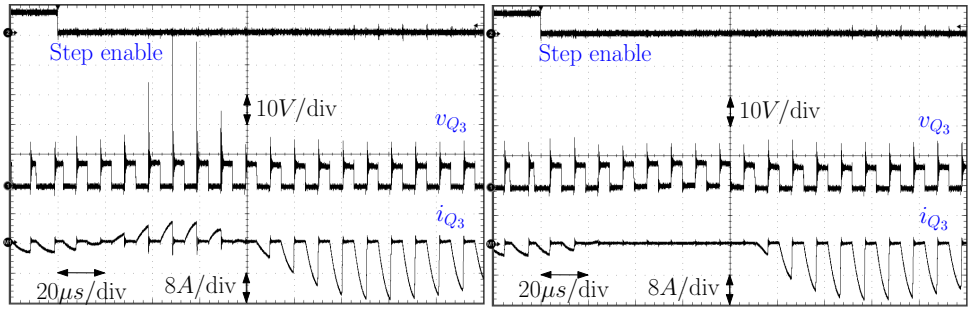


FIGURE 5.25: Implementation of the proposed control technique. The inequalities of system (5.20) are implemented with two comparators.

in positive-feedback configuration around the comparators, in order to provide a hysteresis window in the transitions and prevent chattering. Notice that, based on (5.25), only the lower threshold is of interest, hence a large hysteresis window can be employed if needed, without affect the accuracy of the approach. The proposed technique is VHDL coded in the FPGA board. The simplified code is shown in Fig. 5.25. The code consists in two parts. The first one is the sequential part which is clocked with the internal FPGA clock at 200 MHz and which updates the next state. The second is combinational and contains the logic to select the next state. In this second part, no memory digital elements are synthetized. In a first test, the proposed technique is first disabled, and a 20%-to-45% duty cycle step variation is applied to the converter in order to induce a large-signal transient severe enough to cause Q_3 to temporarily undergo hard turn-off. The transient event is reported in Fig. 5.26a, which clearly shows the large voltage spike at the drain of Q_3 when the device turns off at positive drain-to-source current. In the measurements,



(a) (b)

FIGURE 5.26: Transient due to duty cycle step variation $D = 20\%$-to-45%. Comparison between experimental waveforms with conventional control (a) with the proposed technique (b).

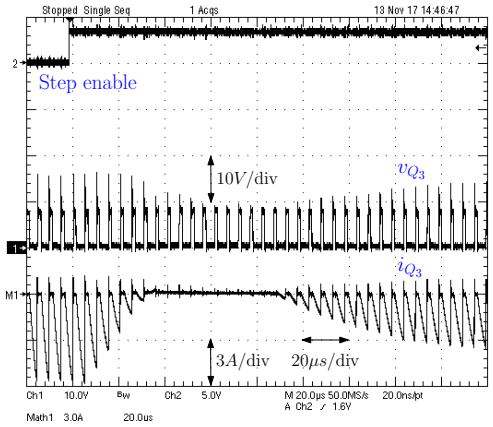
i_{Q_3} is calculated as $i_{Q_3} = i_{L_R} - i'_o$ by separately measuring i_{L_R} and i'_o with current probes.

Next, the proposed technique is enabled, and the same large-signal transient is induced in the converter. Corresponding results, illustrated in Fig. 5.26b, show how the turn-off of Q_3 at positive current is now completely prevented. As a result, no voltage spike is seen across Q_3. Furthermore, the converter falls back into normal steady-state operation after the transient.

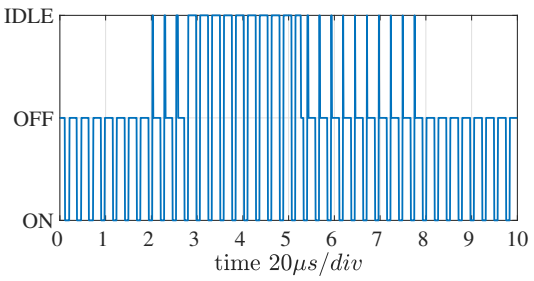
A similar transient measurement is illustrated in Fig. 5.27a, while Fig. 5.27b reports the corresponding states of the FSM, acquired from the FPGA with a digital acquisition software. Both Fig. 5.27a and 5.27b are triggered and acquired on the same transient event. The figure proves that, in steady-state before and after the transient event, the converter normally rotates between the ON and OFF states, but during the transient the FSM temporarily forces the converter to operate in the IDLE subtopology, as intended.

Closed Loop Results

The output voltage is sensed through a fully differential opamp which sets the output common mode for the 12 bit pipelined AD converter. A digital PI controller is implemented and tested with conventional control and with the proposed technique enabled.



(a)



(b)

FIGURE 5.27: Transient due to step of duty cycle $D = 20\% \rightarrow 30\%$ with the proposed approach. (a) SCTI waveforms and (b) corresponding states of the FSM.

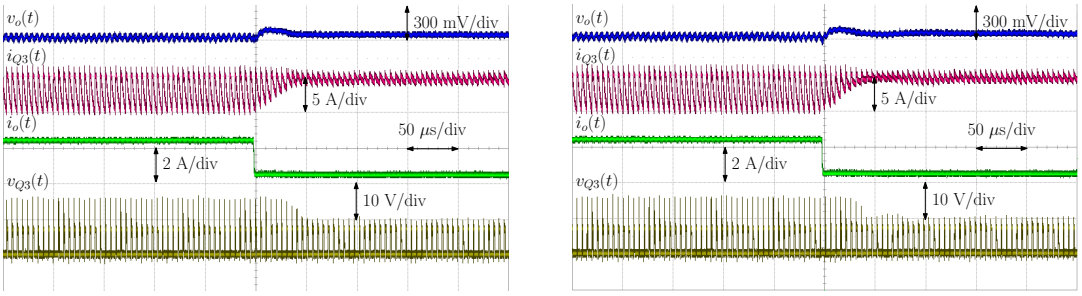


FIGURE 5.28: Load step from 2.2 A to 0.5 A with the proposed technique disabled (a) and enabled (b).

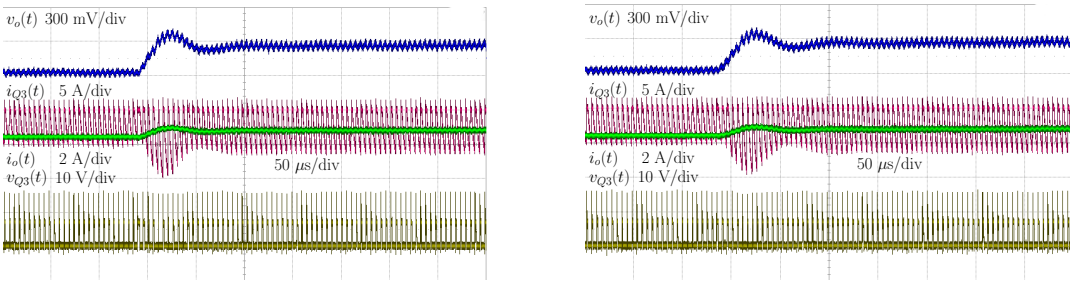


FIGURE 5.29: Reference voltage step from 1.5 V to 1.8 V with conventional control (a) and with the proposed technique enabled (b).

To verify that the FSM operation does not interfere with the control loop, first a load step is induced. The load steps from 2.2 A to 0.5 A for both disabled and enabled technique are depicted in Fig. 5.28a and Fig. 5.28b respectively. The output voltage is regulated and the FSM machine does not intervene (thus being transparent) when i_{Q3} current has negative slope during T_{OFF}.

The response of the converter to a 1.5 V to 1.8 V reference step is shown in Fig. 5.29. These experimental results show that the technique does not alter the small signal behaviour of the converter and can be included in a standard PID controlled SCTI converter, without requiring an *ad hoc* controller design.

5.4 Conclusion and Summary of Contributions

When the ZVS turn-off of Q_3 is lost, the SCTI experiences a large voltage spike, which poses a reliability issue. In this chapter two possible solutions to this problem have been devised, namely a *hardware* and a *software* solution. The first one consists of an auxiliary winding snubber, which requires only an additional power diode with reduced current rating and an auxiliary winding on the same magnetic core. The design equation for the snubber have been provided and the parasitic inductances have been taken into account. Then an optimization based on finite element simulations is proposed. This approach is verified through computer simulations. The second control-based solution does not require any additional power circuitry, but only two analog comparators and a simple finite state machine. The FSM is devised, described and both simulation and experimental results corroborate the theoretical analysis.

Chapter 6

Conclusion

This research activity has been carried out thanks to a collaboration between Power Electronics Group of the Department of Information Engineering (DEI) and Infineon Technologies S.r.l. and focused on digital control and optimization for automotive dc-dc switching converters. Part of the research activity is developed during a six months visiting period at Infineon Technologies A.G. in Munich (Germany) under the supervision of prof. Georg Pelz.

Digital control solutions were devised used to both regulate and optimize the operation of the converters. This approach is applied to three automotive scenarios:

1. Bidirectional high-power switching converter for EV or HEV powertrains
2. Low-power dc-dc converter for the standard 12 V-to-5 V application
3. High-step down 48 V-to-1.5 V bus to microcontroller power supply.

In the first two cases, a two-loop digital system is applied, i.e. the output voltage regulation loop and the optimizer loop. As for the third, a digital finite state machine is employed in order to avoid a potentially catastrophic voltage spike, which can occur if conventional modulation is adopted. The main contributions of this thesis can be summarized as follows:

- Minimum conduction losses trajectories (MCT) have been calculated for the SR-DHB converter under the fundamental harmonic approximation, which has been verified through both a multi-harmonic simulations and experimental measurements. A simplified piecewise linear trajectory based on least square error minimization is developed for the integration (ASIC) and small microcontroller. As a secondary effect, the reduction of switching losses on the proposed trajectory is studied analytically. These results are presented in a journal publication [107].

- An online efficiency optimization loop is devised for the non-resonant dual half-bridge converter in the 12 V-to-5 V application. One of the modulation quantities offered by the topology is used for the output voltage regulation, while the other two are considered as degrees of freedom, which define the optimization plane and which can be employed to improve the efficiency. The efficiency is simulated considering conduction losses and a modified version of the approach proposed in [70] for the switching losses. Several standard modulation techniques are analyzed on the optimization plane and it is shown that no one of them is optimal over the full output power range.

  To find the efficiency peak in every output power condition, a second low-speed optimization loop is devised. The input current is measured and a simplex algorithm based finite state machine acts on the two degrees of freedom in order to minimize it. This way the best efficiency point is reached in every operating condition. Experimental measurements validate the approach.

- For the high step-down 48 V-to-1.5 V the SCTI topology is considered and its voltage conversion ratio is calculated. A reliability issue related to this topology is then identified. In SCTI topology an overvoltage on the synchronous rectifier can follow several transient events, e.g. duty cycle

or input voltage steps. The cause is found to be the forced discontinuity in the MOSFET current – a linear combination of inductance currents – which induce a voltage spike limited only by the parasitic capacitance of the MOSFET Ṫhe analytical expression of the overvoltage is then calculated.

- To address the aforementioned issue, a snubber-based on an auxiliary winding is devised. The proposed snubber requires only an additional winding a power diode, whose current requirement are reduced. The effect of parasitic inductances is studied and analytical expressions are give for the design. An optimization of the three-winding coupled-inductor is proposed and performed through finite element method (FEM). The resulting optimized designed is simulated to prove the effectiveness of the approach and the results are presented on the Workshop on Control and Modeling for Power Electronics 2018 [108].

- An alternative approach based on a finite state machine is developed for the SCTI topology. It requires only two analog comparators and a three state FSM. The effectiveness of the proposed technique is verified through both simulations and experimental results, by showing a spike-inducing transient with conventional control and with the FSM enabled. A standard digital PID controller is designed as a output regulation loop and the FSM is demonstrated not to interfere with the control loop. The proposed technique intervenes during transient only, being transparent in steady state. This work has been first proposed in [96] and then expanded for a journal publication which is currently under revision.

- Tapped-inductors optimized for the SCTI topology are not commercially available. In order to employ this topology on a product, the optimization should be carried with off-the-shelf components. In conjunction with the visiting program at Infineon Technologies A.G., Cadence®

simulations driven by machine learning algorithm developed by the hosting group of prof. Pelz are run in order to find which inductor can be employed in a 48 V bus to 0.9 V microcontroller core supply application. Design guidelines for the SCTI tapped-inductor resulted from this work.

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