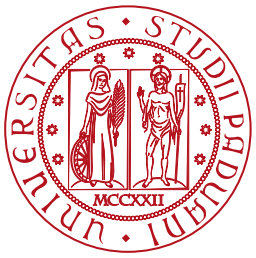

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Implementation and Modeling of Online Efficiency Optimization Techniques for High-Frequency dc-dc Converters in Automotive Applications

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Abstract

In recent years, the automotive industry has been characterized by a growth in the field of electronics. This growth concerns many aspects in the car design such as energy efficiency, safety, x-by-wire systems, connectivity and comfort. For this reason, while in the past electronic power consumption was negligible with respect to the total car energy consumption, a particular attention is paid nowadays to the efficiency of these devices. Furthermore, there is a political and social pressure to reduce CO_2 emissions that results in penalties and taxes for those companies who do not comply with the limits imposed by national and international targets. It is clear that failure to meet these standards causes a loss of competitiveness and profit. Therefore many efforts have been made during the last years by the automotive industry to find affordable solutions to improve the energy efficiency of each part of the vehicle. For small power devices such as safety systems (airbag, adaptive cruise control, collision avoidance etc...), vehicle networking, body (windows drivers, led driver etc...) the state of the art technologies belong to the class Smart Power Technology (SPT). Such class of technologies allows to include in the same chip die low voltage digital and analog devices like MOSFET and bipolar transistors (smart part) and power devices like high voltage DMOS (power part). The smart part of the technology is used by designers to implement systems like over temperature, short circuit protection and over

voltage management circuits, while the power part is used to implement the power stage. The most widespread class of power stages is so far represented by linear regulators because of their relative simplicity, low noise, small size and low cost. The major weakness, however, is their typically poor efficiency. As a consequence, although linear regulators still represent the main source of profit, the automotive silicon industry is investing more in highly efficient solutions such as switching converters. The main reasons that obstruct the diffusion of switched-mode power supplies in low power automotive applications are the additional costs and additional area consumption caused by the need to include bulky inductors.

Goal of this Ph.D. research is to explore on the fly efficiency optimization strategies, also known as online efficiency optimization techniques, in which the converter is dynamically brought to its maximum efficiency operating point regardless of the specific operating conditions. This research activity is conducted through the collaboration between Infineon Technologies Italia and the Department of Information Engineering (DEI) of the University of Padova within the framework of a contract of *Apprenticeship in Higher Education and Research*, and focuses on modeling and design of efficiency optimization techniques for high-frequency dc-dc converters in automotive applications. Part of the research activity has been developed during a six months visiting period at the *Colorado Power Electronics Center* of the University of Colorado at Boulder, under the supervision of Prof. Dragan Maksimović.

The approach followed during the research activity aims to transfer the hardware complexity from the power stage, that is typically the most expensive part, to the control stage. In this regard, the digital control appears a natural choice enabling the possibility to explore advanced control strategies and modulation schemes that exploit the degrees of freedom offered by the con-

verter for purpose of regulation and efficiency optimization. Moreover, being the compactness one of the major issues, the soft switching capability become a crucial aspect allowing to thereby increase the switching frequency without compromise the converter efficiency and to reduce the passive component size. The thesis is organized as follows. First of all, a general overview of the automotive power electronics is presented in order to clarify the motivation of this research. The first part of the thesis focuses on the steady state analysis of the Dual Half Bridge converter with particular regard to the efficiency characterization. Such topology is considered, in both its resonant and non-resonant versions, because of its degrees of freedom inherently available in the converter modulation space. Control strategy are proposed that allow to accomplish the output voltage regulation and an online efficiency optimization. In systems like the one under consideration, the controller moves the converter from one operating point to a new one every time a new event occurs (for example a load step or battery line variation). For this reason, a wide area of the control space can be potentially spanned during the normal operations, therefore an accurate dynamic analysis is mandatory to ensure the stability of the system throughout the entire control space. For this reason another important topic analyzed in this thesis is the dynamic study of digitally controlled Dual Active Bridge converters. The dynamics introduced by uniformly sampled phase shift modulators and combined phase shift and pulse width modulators is analyzed in detail and incorporated into a multi-harmonic small-signal model valid for both the resonant and non resonant dual half-bridge topologies.
All the results presented in this thesis are validated both via simulations and experiments made on discrete components prototype.

Sommario

Negli ultimi anni si è assistito ad un rapido sviluppo nell'ambito dell'elettronica di potenza applicata all'industria automobilistica. Questa evoluzione riguarda molti aspetti nella progettazione dell'automobile, ad esempio l'efficienza energetica, la sicurezza, l'introduzione di sistemi x-by-wire, connettività e confort. Per questa ragione, mentre in passato il consumo di potenza associato ai dispositivi elettronici era trascurabile rispetto al consumo totale dell'auto, oggi si presta molta attenzione all'efficienza di ciascun dispositivo. Vi sono inoltre pressioni sociali e politiche che spingono verso la riduzione delle emissioni di CO_2. Queste si traducono in sanzioni e tasse aggiuntive per le aziende inadempienti nei confronti dei limiti imposti dalle normative nazionali e internazionali, e in un conseguente danno di immagine delle stesse. È perciò chiaro che non rispettare questi standard causa una perdita di profitto e competitività. Perciò, negli ultimi anni, sono stati fatti molti investimenti finalizzati a trovare soluzioni economicamente realizzabili con lo scopo di migliorare l'efficienza energetica di ogni parte del veicolo. A questo proposito, il progetto di sistemi di alimentazione ad alta efficienza è di cruciale importanza. Per sistemi di alimentazione di dispositivi a bassa potenza quali i sistemi di sicurezza (airbag, sistemi anti-collisione etc...), connettività e illuminazione, lo stato dell'arte prevede l'utilizzo di circuiti di potenza appartenenti alla classe Smart Power Technology (SPT). Questa tecnologia permette di includere nello stesso

chip, componenti analogici, digitali e transistori di potenza. Il punto di forza più importante di questa tecnologia è la possibilità di includere nello stesso circuito integrato oltre che al convertitore, sistemi di anti-surriscaldamento, protezione da cortocircuiti e sovratensioni e implementare sistemi di gestione intelligente dell'energia. Per molto tempo, la classe di convertitori di potenza più utilizzata è rappresentata dai regolatori lineari. Le caratteristiche principali di questi convertitori sono la loro bassa complessità dell'hardware e la riduzione dei costi e dimensioni. Per contro, risultano poco efficienti dal punto di vista energetico poiché la regolazione della tensione di uscita avviene dissipando la potenza in eccesso nel convertitore stesso. Di conseguenza, benché i regolatori lineari rappresentino ancora la maggior fonte di profitto, l'industria automobilistica sta investendo in soluzioni più efficienti come ad esempio i convertitori a commutazione. Le ragioni più importanti che hanno ostacolato la diffusione di questa classe di convertitori nell'ambito dei sistemi a bassa potenza sono i costi tipicamente più elevati e l'ingombro causato dall'impiego di componenti esterni quali induttori e condensatori di filtro.
Questa attività di ricerca di dottorato si inquadra quindi nell'ambito dello sviluppo di tecniche di ottimizzazione online dell'efficienza, ossia sistemi nei quali il convertitore è mantenuto nel suo punto operativo di massima efficienza a prescindere dalle condizioni in cui esso si trova. L'attività di ricerca è svolta in cotutela con Infineon Technologies Italia Srl nell'ambito di un contratto di *Apprendistato in Alta Formazione e Ricerca* dal titolo "Studio e progetto di architetture e topologie circuitali innovative per convertitori DC/DC ad alta efficienza e ad alta frequenza di commutazione per applicazioni nel campo dell'industria automobilistica". Una parte dell'attività è stata svolta durante un periodo di studio di sei mesi presso il *Colorado Power Electronics Center* dell'Università del Colorado a Boulder, sotto la supervisione del Prof. Dragan

Maksimović.

L'approccio seguito mira a trasferire la complessità dell'hardware dal convertitore al controllo con un impatto minimo sul costo complessivo del sistema. A questo proposito, l'implementazione digitale del controllore rende possibile lo sviluppo di strategie di controllo avanzate e schemi di modulazione che sfruttano i gradi di libertà del convertitore per motivi di regolazione e ottimizzazione dell'efficienza. Un esempio è la possibilità di utilizzare tecniche soft-switching le quali consentono di aumentare notevolmente la frequenza di commutazione senza compromettere lefficienza del convertitore e, in aggiunta, di ridurre le dimensioni dei componenti passivi. In particolare la ricerca è focalizzata sullo studio dei convertitori a doppio mezzo ponte, nelle loro versioni risonante e non risonante. Questa classe di convertitori è stata scelta per la bassa complessità dell'hardware e per il numero dei gradi di libertà che possono essere utilizzati per finalità di controllo. La prima parte della tesi tratta il tema della modellizzazione di questi convertitori dal punto di vista statico con particolare attenzione agli aspetti che riguardano la caratterizzazione dell'efficienza. Sulla base dei risultati ottenuti, sono proposte delle tecniche di controllo multivariabile e ottimizzazione online dellefficienza. In sistemi di questo tipo, il convertitore si porta da un punto operativo all'altro ogni volta che si verifica un evento (ad esempio una variazione del carico o della tensione di batteria). Per questo motivo, durante il normale funzionamento, il punto operativo del convertitore può attraversare un'ampia porzione dello spazio di controllo quindi è richiesta un'accurata analisi dinamica per garantire la stabilità del sistema. Un'importante tematica affrontata in questa tesi, è lo studio dinamico dei convertitori a doppio mezzo ponte con controllo digitale multivariabile. In dettaglio, sono stati approfonditi aspetti riguardanti la modellistica della dinamica introdotta dai modulatori a sfasamento digi-

tale a campionamento uniforme e dai modulatori a sfasamento e larghezza d'impulso a campionamento uniforme. Tali modelli sono stati impiegati al fine di costruire un modello ai piccoli segnali di tipo multi-armonica per il convertitore a doppio mezzo ponte con controllo digitale multivariabile. Tutti i risultati presentati in questa tesi sono validati tramite simulazioni e misure sperimentali fatte su prototipi a componenti discreti.

Contents

Chapter 1

Introduction

Contents

1.1 Overview of power electronics for automotive applications

In recent years, the automotive industry has been characterized by a global growth in the field of electronics and analysts agree with the fact that this tendency will be maintained for several years. Such a growth is principally due to two reasons:

- Increasing cars demand, especially attributable to the BRIC nations (Brazil, Russia, India and China).
- Rapidly increasing complexity and number of applications in the auto-

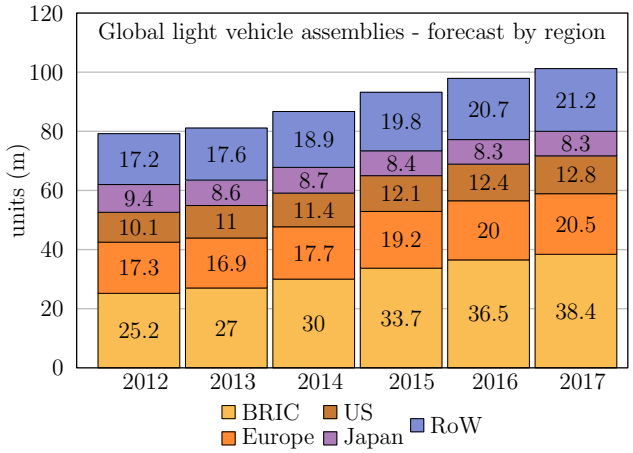
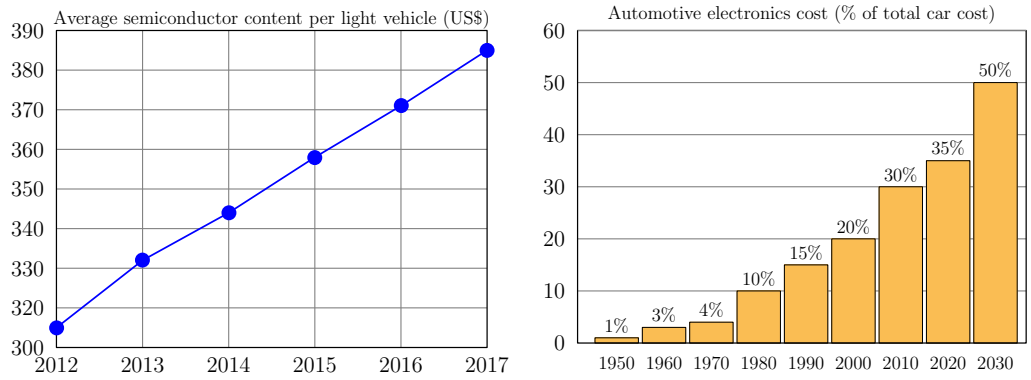


Figure 1.1: Global light vehicle assemblies - forecast by region. *Source: PwC Autofacts (Q3 2013).*

motive world.

In Fig. 1.1 the global car vehicles assemblies forecast is plotted for the period 2012-2017 and confirms a global compound annual growth of about 5%. Furthermore, the electronic content in the vehicle is thereby increasing. The silicon cost in current cars is constantly increasing (Fig. 1.2a) with a total electronic cost which is forecast to reach the 50% of the total car cost in next fifteen years (Fig. 1.2b). Safety systems, advanced driver assistance systems, efficient powertrain solutions, connectivity and comfort are all elements that contribute to sustain this trend. This tendency has both social and political nature. For instance, rating agency like the american *National Highway Traffic Safety Administration* (NHTSA) and the european *European New Car Assessment Programme* (Euro NCAP) promote the development of innovative safety systems which are nowadays based on electronic systems. Protection systems like airbag and crash avoidance systems like emergency braking systems and attention assist are becoming mandatory to obtain the maximum rate. Since statistical data confirm a correlation between these rates and car popularity, companies are investing many resources in this area.



(a) (b)

Figure 1.2: Car electronic content: (a) Average semiconductor content per vehicle, (b) Automotive electronics cost.
Source: Spotlight on Automotive PwC Semiconductor Report 2013

Another key topic driving the automotive industry is the CO_2 regulation. Oil-dependence as well as climate change is subject of discussion for governments and communities. Even though not in an uniform way, countries have defined CO_2 regulations aiming to reduce fuel consumption and emissions. In Fig. 1.3, the main mandatory CO_2 regulation for passenger car is plotted with the window time 2000-2025. Concretely, such regulations define penalties and additional taxes for those companies who not comply with the limits or incentives for the customer. As a consequence, failure to meet these standards causes a loss of competitiveness and profit. Therefore, innovative and affordable solutions in the field of energy efficiency are also required. In this direction, partial or full electrification of the vehicle aiming to replace mechanical and hydraulic components with lighter electric devices become a central point. Furthermore, all new electromechanical systems are driven by an *Electronic Control Unit* (ECU) usually implemented with a microcontroller. The number of ECUs in a car at the end of 2013 is around 70-90 for mid range cars and 100-120 for high end car. For all the reason

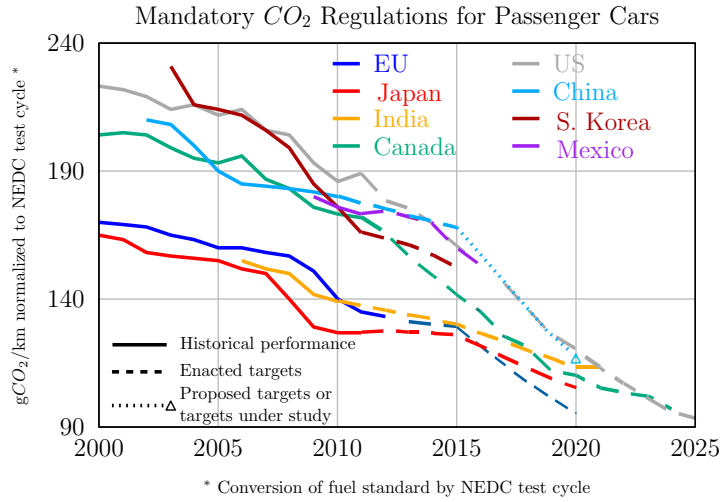


Figure 1.3: Mandatory CO_2 regulations for passenger cars.
Source: International Council on Clean Transportation (ICCT) report, February 2014

explained above, the electronic power consumption is no longer negligible and an efficient power supply is mandatory. Another important reason that makes it desirable to achieve high efficiency in automotive power supply is the harsh condition in which power converters operate, especially for *drive-by-wire* applications [1]. Since high environment temperature is the primary reason of packaging limitations, minimization of the overheating caused by power losses is an important point. DC to DC switched-mode converters play an important role in this direction and they are replacing linear voltage regulators, which have represented the most widespread technical solution so far. Linear regulators provide a stabilized, high precision output voltage with few external components in a very small footprint. However, the maximum efficiency of such converters is equal to the ratio between the output and the input voltage. In standard applications, the input voltage is around 12V and the output voltage is 5V or 3.3V. Therefore, the use of linear regulators leads to an efficiency of 41.6% or 27.5% respectively. On the contrary, an

ideal switched-mode converter achieves an efficiency of 100%. For this class of converters power losses are only caused by parasitic elements such as current paths resistance and parasitic capacitances of electronic switches. These parasitic elements only depend on the available technology.
The state of the art technology in the field of standard automotive power supply is represented by the *Smart Power Technology* (SPT). SPT allows the integration of analog, digital and power elements on one single IC with consequent advantage of higher integration and cost reduction. Using this technology, in small power applications (5-15W) the sole external components are inductors and filter capacitors.

1.2 High efficiency converters

In recent years, many efforts have been made in the field of efficiency optimization of power converters. The approaches followed by designers differ by application and power rate, but they all aim to minimize the main causes of losses in a converter. A first example of efficiency optimization relates to the choice of the best hardware components and the choice of their parameters in order to minimize the resistance of the current path and the transistor parasitic capacitances. Beyond these consideration related to the available technology, many techniques have been developed in the past to extend the operating region in which the converter is characterized by high efficiency. For instance, some techniques are based on an alternative driving strategies including on-off control, dead time optimization and gate voltage control [2,3]. When the main cause of efficiency drop are the conduction losses, a typical strategy adopted is the paralleling of switches or the adoption of a multi-phase architecture [4–6] used to uniformly distribute the current in multiple paths

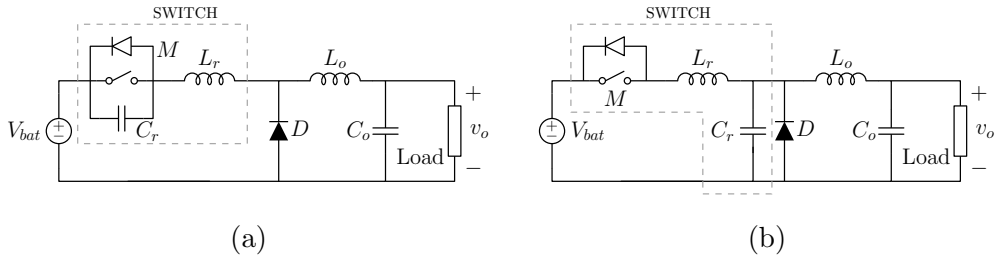


Figure 1.4: Quasi-resonant buck converter: (a) ZVS-QRC, (b) ZCS-QRC.

between the input and the output stage of a converter.

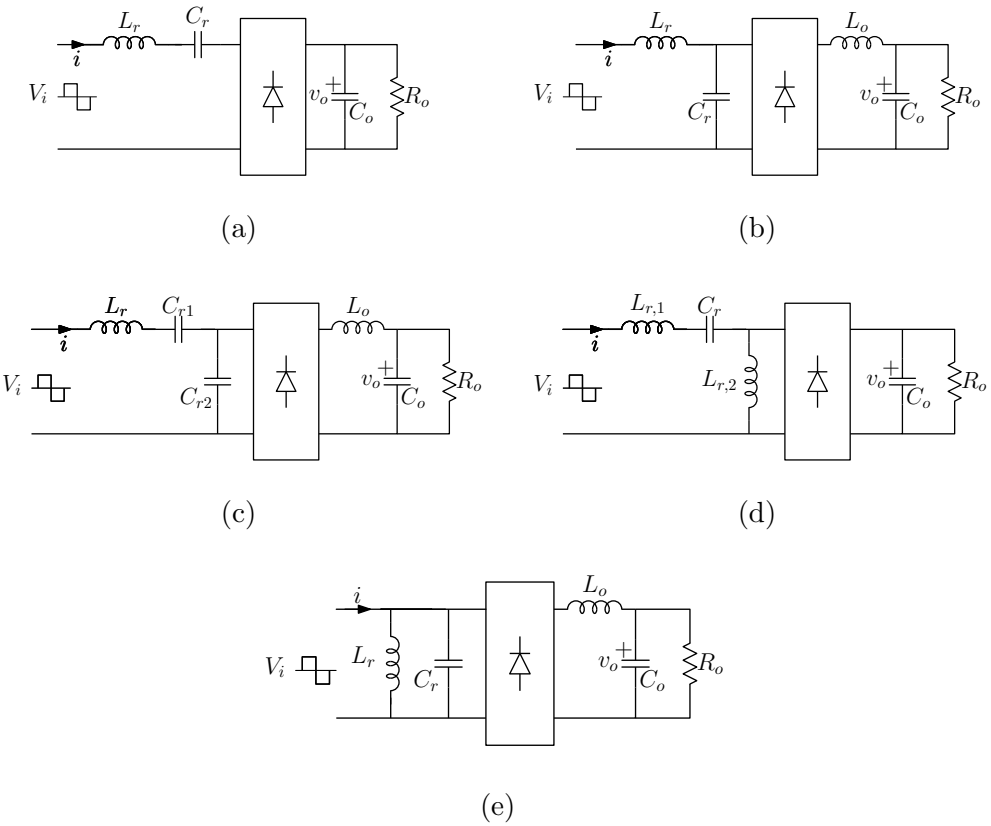


Figure 1.5: Resonant converters topologies: (a) Series resonant converter with series load, (b) series resonant converter with parallel load, (c) LCC resonant converter, (d) LLC resonant converter, (e) parallel resonant converter.

In high frequency or high voltage applications switching losses represent one major cause of efficiency drop. For such applications many researches propose alternative topologies based on Quasi-Resonant Converters (QRC) [7–12] or resonant converters [13–18]. Such converters are developed to guarantee the Zero Current Switching (ZCS) or Zero Voltage Switching (ZVS) of transistors to reduce the associated power losses. Quasi-resonant converters are based on conventional converters with additional circuitry designed to modify the switching behavior of the converter. Fig. 1.4 shows two examples of QRCs based on buck topology. In such converters, additional resonant components L_r and C_r placed to achieve soft switching are located in series or in parallel with parasitic elements so that they actively contribute to the power conversion. In these class of converters, transistors *turn-on* and *turn-off* instants are typically imposed by the values of L_r and C_r to achieve ZVS or ZCS, therefore they are usually frequency controlled with a constant on-time or off-time modulation. Output filter elements L_o and C_o are supposed to be much larger then resonant components ($L_o \gg L_r$ and $C_o \gg C_r$).

The other soft switching class of converter is the class of resonant converters. Resonant converters use the energy stored in a resonant circuit (resonant tank) to perform the power conversion. Such converters are designed to shape the tank current in order to make the switches operate in ZVS or ZCS. Some examples are shown in Fig. 1.5 where simplified schematic diagrams are sketched. Resonant converters can be classified depending on the type of resonant circuit used (series or parallel) and on the connection of the load. Hybrid examples of resonant converter are the LCC and LLC converters sketched respectively in Fig. 1.5c and Fig. 1.5d. Reference [19] illustrates a steady state analysis and design methodology of the LLC where the converter is controlled with narrow variations of switching frequency. The paper also

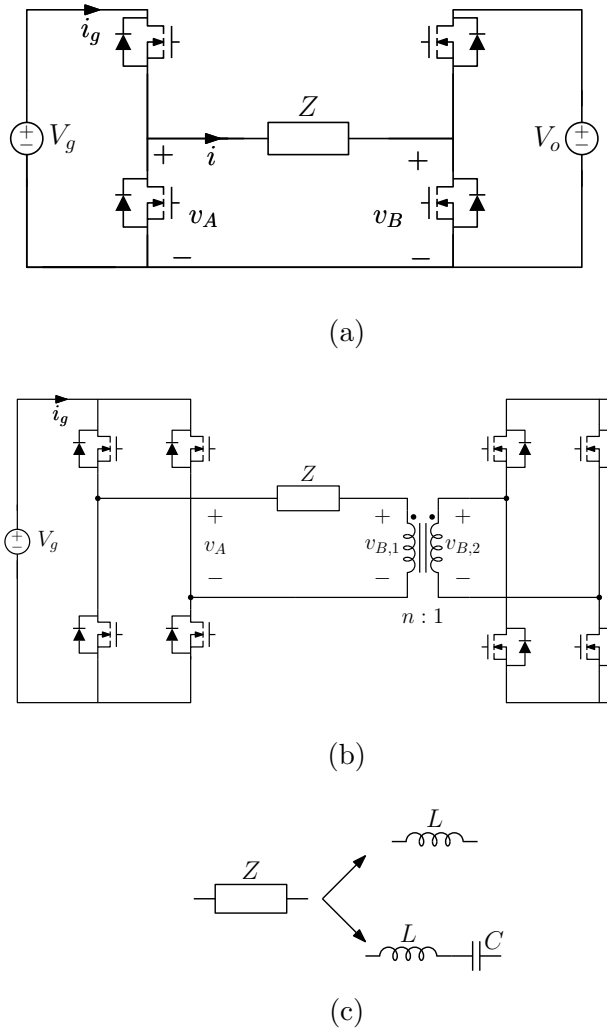


Figure 1.6: Schematic diagrams of the dual active bridge: (a) half bridge version, (b) full bridge version, (c) impedance.

shows that the zero voltage switching can be achieved over the entire operating range. Reference [20] proposes a design methodology of a LCC-based electronic ballast for fluorescent lamps.

Another approach to efficiency optimization is based on the choice of converters in which many control inputs can be used for purpose of regulation. A typical example is the class of Dual Active Bridge (DAB) converters il-

lustrated in Fig. 1.6. Many versions of the DAB converters exist and they can be categorized according to the bridge topology (half or full bridge) or according to the kind of impedance placed between the bridges which can be purely inductive or a resonant circuit. This class of converters is of particular interest in the context of online efficiency optimization due to its number of available control variables. This fact opens up the possibility to exploit the degrees of freedom not directly used for purpose of regulation to implement smart control and modulation techniques aiming to optimize the energy efficiency. Some example are multi-angle control [21, 22] and efficiency optimized modulation scheme like those described in [6, 23–27]. This approach allows to use simple power stages and transfer the hardware complexity to the control stage. Such multi-variable modulations aim to minimize the RMS current [21, 22] of the inductor current or to extend the operating range in which the converter operates in soft switching [25, 28]. This approach is supported by the evolution of the digital control which allow the implementation of advanced techniques based on multi-variable control [6, 24, 26, 28–31]. When the efficiency optimization is performed by a multi-variable control, the used strategy can be *offline* or *online*. The offline optimization requires a preliminary efficiency characterization and the calculation of optimal control trajectories typically stored in look up table [6, 22, 24]. In presence of variable conditions caused by load and battery changes or environment variations (for instance change in temperature) the best efficiency operating point can be subjected to significant variations. As a consequence, pre-calculated trajectories can only optimize the efficiency over a limited range of operating conditions. On the contrary, online efficiency optimization is based on an additional loop performing the efficiency optimization for instance through the average input current minimization.

1.3 Objective of the thesis

Goal of this dissertation is to propose and analyze online efficiency optimization solutions for switched-mode power supplies employed in automotive applications. Fig. 1.7 shows the power supply architecture considered throughout this thesis. The automotive application block represents an electric or electromechanical system, for instance an airbag system. This system is commonly driven by an Electronic Control Unit (ECU) that is typically a microcontroller supplied by a switching DC-DC converter connected to a battery.

The first part of this thesis focuses on the efficiency characterization and online efficiency optimization techniques of resonant and non-resonant dual active bridge. The approach followed in this research is based on a muli-loop system composed by a fast regulation loop and a slower efficiency optimization loop. The regulation loop senses the output voltage and performs the control by means of a digital regulator while the optimization loop performs a minimum average input current tracking. The output voltage and average input current are processed by a multivariable controller which acts on two or more control variables of the converter, which act as degrees of freedom exploited for efficiency maximization purposes. Converters considered in this work are the resonant (chapter 4) and non-resonant (chapter 5) versions of the dual half bridge converters of Fig. 1.6a. In conjunction with the visiting program at the Colorado Power Electronics Center the resonant version of the dual half bridge converter is studied in the context of a research employing non-conventional technologies based on Gallium Nitride (GaN). Since the disclosed efficiency optimization solutions involve the simultaneous modulation of a number of control variables available in the resonant and non-resonant topologies, such as the phase shift between input and output

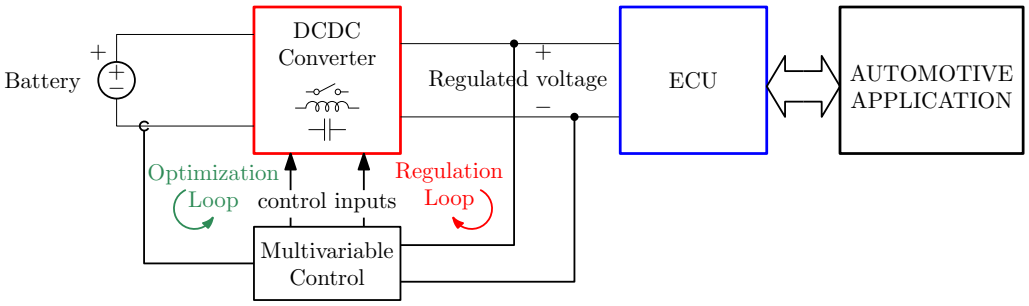


Figure 1.7: Block diagram of the online efficiency optimization scheme considered throughout the thesis.

legs and the duty cycles of the two legs, it becomes crucial to reliably model the dynamical response to the converter when subject to these types of multivariable modulations. The second part of the thesis therefore focuses on the dynamic modeling of the system of Fig. 1.7. A generalized dynamical modeling approach is developed which accounts for the effects of combined phase shift and duty cycle modulations, and which simultaneously embeds the important small-signal delay effects associated to the digital nature of the modulators involved.

Following a brief description of the chapter contents is summarized.

Chapter 2: In this chapter a preliminary review of the physical phenomena causing power losses during switches commutation is presented. Subsequently, the *soft switching* condition is defined focusing on its advantages. The conditions required to guarantee *full* soft switching are also discussed. Then, a model to estimate the power losses for the case of *partial* soft switching is proposed.

Chapter 3 In this chapter the steady state analysis of the Dual Half-Bridge Series Resonant Converters is discussed with particular focus on the efficiency behavior. Methodologies based on exact calculation of resonant tank current and voltage waveforms, fundamental harmonic approxima-

tion and multi-harmonic approach are reviewed and compared.

Chapter 4 This chapter proposes a digital online efficiency optimization technique for dc-dc Dual Half-Bridge Series Resonant Converters based on the architecture illustrated in Fig. 1.7. The proposed technique implements an advanced modulation scheme which exploits the degrees of freedom inherently available in the converter modulation space in order to simultaneously regulate the output voltage and maintain the system in its maximum efficiency point. Furthermore, the proposed multivariable control technique robustly brings the converter back to maximum efficiency even in presence of abrupt load changes.

Chapter 5 In this chapter the steady state analysis of the non-resonant version of the dc-dc Dual Active Bridge converter is presented. Each region of the control space is characterized from the efficiency standpoint. Moving from the results of this analysis, a digital online efficiency optimization technique based on the architecture illustrated in Fig. 1.7 is discussed.

Chapter 6 This chapter introduces the dynamic analysis of the control system of Fig. 1.7. A brief review of the dynamic phasor approach used to model the dynamics of AC signals is given. Finally, the state of the art regarding the dynamic modeling of uniformly sampled modulators is introduced.

Chapter 7 This chapter clarifies the modeling procedure for describing the small-signal dynamics of uniformly sampled phase shift modulators. Then, it provides an extension of traditional phasor modeling to digital phase-controlled converters, allowing to account for the additional modulator dynamics in the design of the closed-loop compensation.

Chapter 8 This chapter discusses the small-signal dynamics of combined phase shift and pulse width modulators when implemented digitally, clarifying how the dynamical contributions of PSM+PWM around the generic harmonic of the switching rate can be expressed in the framework of dynamic phasor modeling. The study extends results discussed in 7 for uniformly sampled pulse width and phase shift modulators, illustrating the effects of sampling delays on the modulator output dynamics.

Chapter 9 This chapter addresses the problem of small-signal modeling of digitally controlled dc-dc series resonant converters when controlled using a combination of phase shift and pulse width modulation. The analysis here disclosed, extends the dynamic phasor approach, employed for instance when a pure phase shift control is used, to a more general multi-harmonic model which accounts for the effects of duty cycle modulation on both the baseband components and the switching frequency components.

Chapter 10 This chapter summarizes the main contributions of this dissertation and provides some conclusive remarks.

Part I

Online Efficiency Optimization Techniques

Chapter 2

Switching losses in a half-bridge

Contents

2.1 Introduction

In this chapter the analysis of the switching losses of the half-bridge with inductive load is presented. This configuration is widely used in power electronics to design high efficiency dc-dc and ac-dc converters. The simplified schematic diagram is shown in Fig. 2.1a in which the power switches are mosfets M_1 and M_2. Such mosfets are driven in a complementary way by the driving signals $v_{g1}(t)$ and $v_{g2}(t)$ defined in Fig. 2.1b with a dead time t_{dead} to prevent short circuits between voltage V_{dd} and the ground. Switching behaviors of a power mosfet (and the associated power losses as well), depend

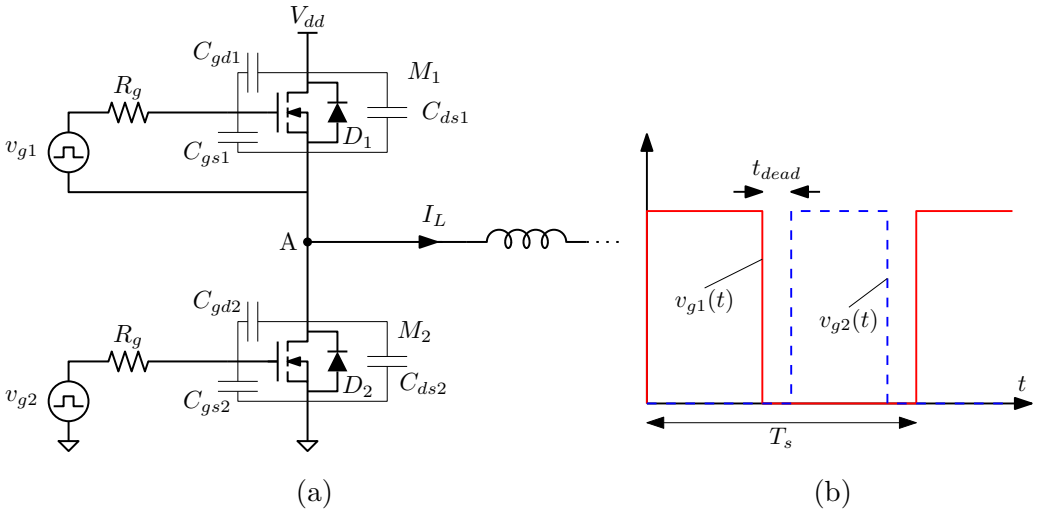


Figure 2.1: Half bridge schematic diagram (a) and driving signals $v_{g1}(t)$ and $v_{g2}(t)$ (b).

both on the topology in which the transistor is included and on the mosfet physics. The primary cause of losses during a commutation is represented by parasitic capacitances C_{gsx}, C_{gdx} and C_{dsx}. In section 2.2 the most used model to study the switching behaviors is reviewed with particular focus on power losses thematic during the *turn-on* and *turn-off*. In section 2.3 the phenomena of *soft switching* is presented highlighting the conditions which allow to reduce switching losses. In section 2.4 the case of partial ZVS in a half bridge is presented and a methodology to calculate the associated power losses is shown.

2.2 Overview of hard-switching power losses

Switching with an inductive load is very common in power electronics. Fig. 2.2a shows the traditional test circuit used to study the switching behaviors of a converter. The mosfet is represented by a *three-port* block with parasitic capacitors C_{gs}, C_{gd} and C_{ds} and a voltage-dependent current

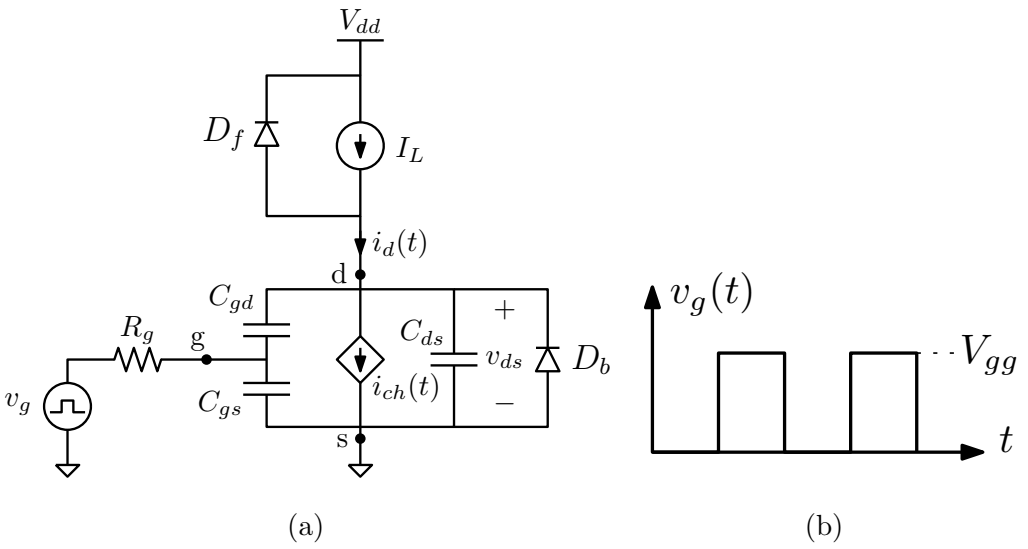
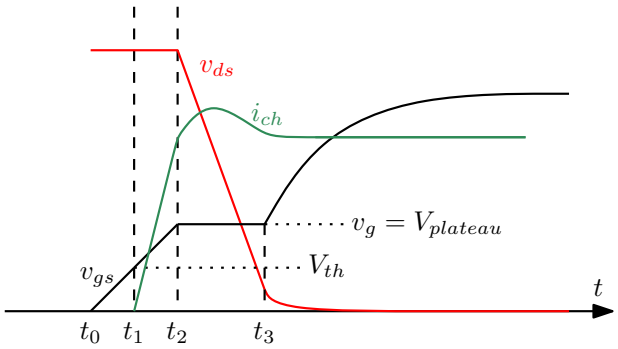


Figure 2.2: Switching circuit test with inductive load (a) and waveform $v_g(t)$ produced by the driver (b).

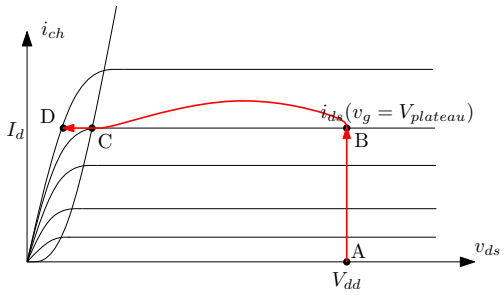
generator modeling the current flowing through the channel $i_{ch}(t)$. In this section the current flowing in the parasitic capacitors are indicated with i_{Cxy} where $x, y \in \{g, d, s\}$ and, for convention, the sign is positive when the current flows from node x to node y. For instance, current $i_{Cgd}(t)$ is the current flowing in the capacitor C_{gd} and is positive when flowing from the gate to the drain. The drain current $i_d(t)$ is equal to

$$i_d(t) = i_{ch}(t) + i_{Cds}(t) - i_{Cgd}(t). \tag{2.1}$$

If it is reasonable to assume that the current in the inductive load does not change during the *turn-on* and *turn-off* intervals, the inductor can be represented by a constant current generator I_L. Finally, the driver is represented by a pulse generator as shown in Fig. 2.2b.



(a)



(b)

Figure 2.3: Main waveforms at the turn-on (a) and the associated trajectory of the point (v_{ds}, i_{ch}) on the $v_{ds} - i_{ch}$ plane (b).

Turn-on phase

The *turn-on* phase is described in Fig. 2.3. At the beginning of the *turn-on* phase the mosfet is off, therefore the current I_L flows through the freewheeling diode D_f and the capacitor C_{ds} is charged to the voltage V_{dd} plus the diode forward voltage. When at the time t_0 the driver voltage rises from 0V to V_{gg}, the gate voltage $v_{gs}(t)$ exponentially tends to V_{gg} with time constant $R_g(C_{gs}+C_{gd})$. When $v_{gs}(t)$ reaches the mosfet threshold voltage V_{TH} (at time t_1), the current can rise according with the triode mosfet current expression. In this phase, the trajectory of the point (v_{ds}, i_{ch}) is vertical as shown in Fig. 2.3b (point A to point B). When at instant t_2, $i_{ch}(t)$ reaches the value

I_D, the freewheeling diode turns off and the voltage v_{ds} is no longer clamped to the voltage V_{dd}. As a result, the driver current discharges C_{gd} through the channel. In this phase we have the relation

$$i_{ch}(t) = I_L + i_{Cgd}(t) + |i_{Cds}(t)| > i_d(t) = I_L \tag{2.2}$$

and the trajectory is shown in Fig. 2.3b (point B to point C). In this phase the gate voltage $v_{gs}(t)$ is almost constant and the value is known as *plateau voltage* V_{plateau}. Finally, at the instant t_3, $v_{ds}(t)$ drops below $v_{gs}(t) - V_{TH}$, the mosfet enters in linear region, the gate voltage tends again exponentially to V_{gg} and the resistance of the mosfet channel gets low. In this phase the trajectory of the point (v_{ds}, i_{ch}) is the one from point C to point D in Fig. 2.3b. An approximate power losses calculation can be accomplished with the following steps:

i) Calculate the plateau voltage using the mosfet current expression in saturation mode

$$I_D = \frac{k}{2}\left(V_{plateau} - V_{th}\right)^2 \tag{2.3}$$

where k is the product of the process transconductance parameter and of the transistor width-to-length ratio.

ii) Calculate instants t_1 and t_2 through the relations

$$\begin{cases} v(t_1) = V_{th} = V_{gg}\left(1 - e^{t_1/\left(R_g\left(C_{gs}+C_{gd}\right)\right)}\right) \\ v(t_2) = V_{plateau} = V_{gg}\left(1 - e^{t_2/\left(R_g\left(C_{gs}+C_{gd}\right)\right)}\right) \end{cases}. \tag{2.4}$$

The capacitance at the gate $(C_{gs} + C_{gd})$ is typically reported in the device data-sheet and indicated with C_{iss}. By Fig. 2.3a, the current

rising time t_{ri} can be calculated as

$$t_{ri} = t_2 - t_1. \tag{2.5}$$

iii) Calculate the voltage fall time $t_{fv} = t_3 - t_2$. The time t_{fv} is the time which the constant gate current $V_{plateau}/R_g$ takes to discharge the capacitance C_{gd}

$$\frac{V_{plateau}}{R_g C_{gd}} t_{fv} = V_{dd}. \tag{2.6}$$

iv) Finally, the power losses can be calculated integrating the instantaneous power losses

$$p(t) = i_{ch}(t) v_{ds}(t) \tag{2.7}$$

during the dead time. Assuming $i_{ch}(t)$ and $v_{ds}(t)$ piecewise linear, $p(t)$ is triangular in shape and the total power loss $P_{\text{turn-on}}$ due to the mosfet *turn-on* is further simplified as

$$\begin{aligned} P_{\text{turn-on}} &= \int_{\text{turn-on}} p(t)dt \approx \\ &\approx \frac{1}{2} V_{dd} I_L (t_{ri} + t_{fv}) f_s. \end{aligned} \tag{2.8}$$

Turn-off phase

The *turn-off* phase is the inverse process of the *turn-on*. In this section the analysis is presented as done for the *turn-on* phase and some considerations are given to motivate the need to make the converter switch in ZVS at the turn-on. The *turn-off* phase is described in Fig. 2.4. At the instant t_0 of Fig. 2.4a, the current I_L flows all in the mosfet channel and the drain-source voltage is almost zero. When the gate driver voltage drops to zero, the gate-source voltage $v_{gs}(t)$ tends to zero exponentially with time constant

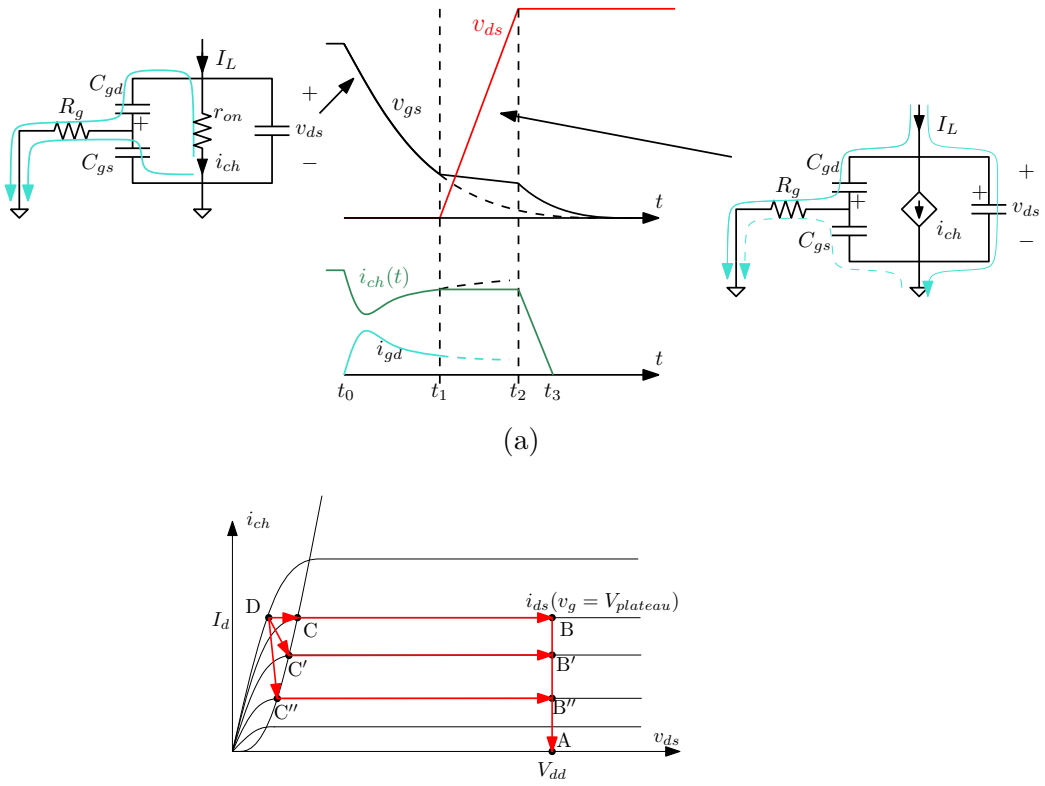


Figure 2.4: Main waveforms at the turn-off (a) and the associated trajectory of the point (v_{ds}, i_{ch}) on the $v_{ds} - i_{ch}$ plane.

$R_g(C_{gs} + C_{gd})$. In this phase, the current flowing in the channel is

$$i_{ch}(t) = I_L - |i_{gd}(t)|. \tag{2.9}$$

If $I_L \gg |i_{gd}(t)|$ then the channel current stays almost constant and the trajectory of the point (v_{ds}, i_{ch}) is the one from point D to point C of Fig. 2.4b. If $|i_{gd}(t)|$ is comparable with I_L then $i_{ch}(t)$ decreases and the trajectory of the point (v_{ds}, i_{ch}) is similar to those from D to C′ or C″ (see Fig. 2.4b). When the mosfet enters in saturation at the instant t_1, the current I_L charges capacitors C_{ds} and discharges C_{gd}. In this phase the channel current is almost

constant therefore, in analogy with the case of *turn-on* phase, the gate-source voltage presents a plateau. In this phase, the trajectory of (v_{ds}, i_{ch}) is one of those from C, C′, C″ to B, B′ or B″ as shown in Fig. 2.4b. Finally, when $v_{ds}(s)$ reaches $V_{DD} + V_{TH}$ at the instant t_2, the freewheeling diode turns on, $v_{gs}(t)$ exponentially drops to zero *opening* the mosfet channel.
Now, an important consideration can be done. The integral

$$E = \int_{turn-off} i_d(t) v_{ds}(t) dt \tag{2.10}$$

does not represent the total power losses during the turn-off phase, but is the sum of the energy dissipated by the channel and the energy stored into the parasitic capacitors. Since the $C_{ds} \gg C_{gd}$ we can assume that the energy is all stored in C_{ds}.

$$\begin{aligned} E &= \int_{turn-off} i_d(t) v_{ds}(t) dt \\ &\approx \int_{turn-off} i_{ch}(t) v_{ds}(t) dt + E_{Cds} \end{aligned} \tag{2.11}$$

where E_{Cds} is the energy stored in C_{ds}. This energy is definitively lost if the switch turns on again in hard-switching mode. On the contrary, if the successive *turn-on* is a ZVS transition, the energy can be recovered.
Moreover, if the driver discharges the gate capacitance with a high current, the trajectory of the point (v_{ds}, i_{ch}) crosses regions characterized by low instantaneous power losses. In this situation, since $i_{ch}(t)$ drops before the rising edge of v_{ds}, the transition is also called *Zero-Current Switching* (ZCS). In those situations, power losses at turn-off can be neglected.

2.3 Soft-switching

In section 2.2 the *turn-on* and *turn-off* transitions have been analyzed highlighting the main causes of losses. In both cases, the circuit of Fig. 2.2a was considered and the current I_L was assumed to be positive. If we consider the case $I_L < 0$, the above considerations are no longer valid. Let us analyze the *turn-off* and *turn-on* phases in this situation:

- In the *turn-off* case, as v_{gs} decreases and the channel becomes less and less conductive, the (negative) channel current is progressively diverted through the switch body diode D_b, which becomes forward-biased. This process is essentially lossless, and one speaks of *Zero-Current Switching* turn-off. Notice, however, that the subsequent turn-off of the body diode is usually lossy due to the associated reverse recovery transient.

- In a similar way, at the *turn-on*, the current already flows through the diode D_b so the switch can turn on with the voltage around 0V. This situation is known as *Zero-Voltage Switching* (ZVS) turn-on.

The considerations expressed above, suggest that the soft switching capability can be exploited if the device is included in a converter topology which is able to shape the current in a convenient way.

2.3.1 Soft switching in a half bridge

Consider now the circuit of Fig. 2.5. Let us define the following parameters:

- C_{oss}, defined as the small-signal capacitance measured between the drain and source terminals of the MOSFET when $v_{gs} = 0$. C_{oss} is therefore equal to the parallel combination of C_{ds} and C_{gd}. Such capacitance is typically non-linear, and its value depends on the drain to source bias

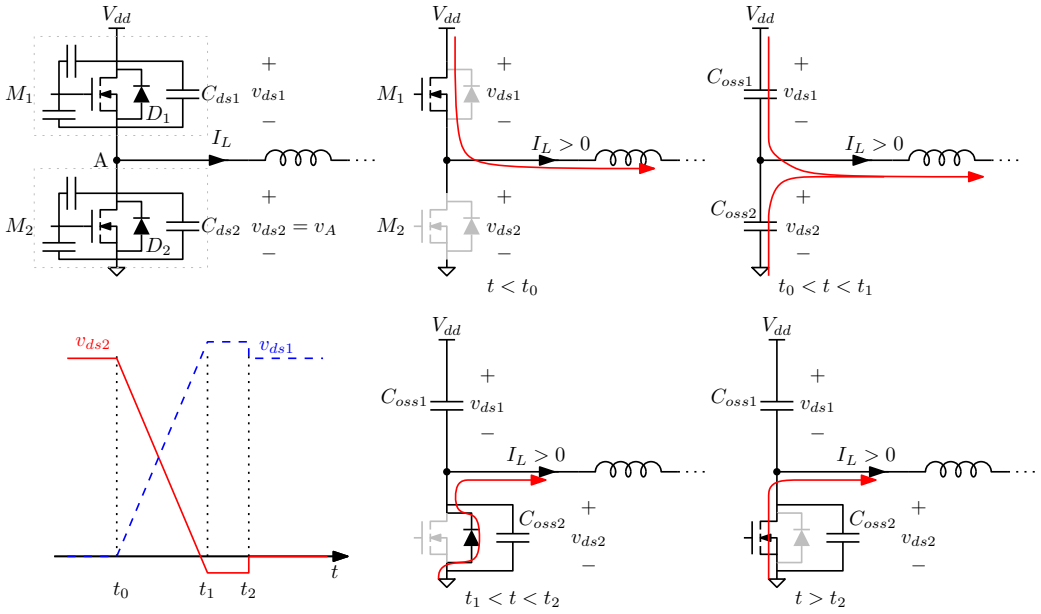


Figure 2.5: Main waveform and topologies sequence during a ZVS transition in a half bridge.

voltage. The C_{oss} *vs.* v_{ds} characteristic can be typically found in the device data-sheet.

- C_{sw}, defined as the small-signal capacitance measured at the switching node A when both mosfets composing the bridge are turned off (e.g. during the dead time).

Since the voltage v_{ds1} across C_{oss1} is

$$v_{ds1} = V_{dd} - v_{ds2}, \tag{2.12}$$

the total capacitance C_{sw} at the node A is

$$C_{sw}(v_{ds2}) = C_{oss1}(V_{dd} - v_{ds2}) + C_{oss2}(v_{ds2}). \tag{2.13}$$

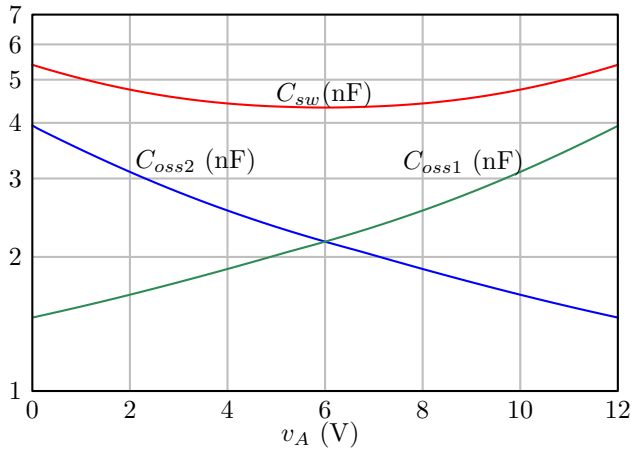


Figure 2.6: Capacitances C_{oss1}, C_{oss2} and total switching node capacitance C_{sw} as function of the switching node voltage v_A.

The plot of C_{oss1}, C_{oss1} and C_{sw} as function of the switching node voltage $v_A = v_{ds2}$ is shown in Fig. 2.6 for the mosfets Infineon OptiMOS®3 power MOSFET of the type IPD036N04L G and $V_{dd} = 12$V.

Suppose at time $t < t_0$ the current I_L is positive, the high side mosfet M_1 is on and the low side M_2 is off. At time t_0, M_1 turns off as explained in section 2.2. During the interval $t_0 < t < t_1$ the switching node capacitance formed by the parallel of C_{oss1} and C_{oss2} is charged by the inductive current I_L . In this phase, the energy stored in C_{oss1} is recovered and the capacitance C_{oss2} is charged. Once the voltage v_{ds2} gets negative, the body diode of M_2 is forward biased and turns on ($t_1 < t < t_2$). At instant t_3 the dead time ends and M_2 turns on at ZVS with low losses. This condition is here referred to as *full ZVS turn-on* and occurs if the current I_L is large enough to charge/discharge the switching node before the end of the dead time. This is an attractive feature for switched-mode converters because it allows to increase the switching frequency without efficiency penalties. To calculate the minimum current to guarantee full ZVS turn-on, consider the equation of the switching node capacitance assuming that the current I_L is constant

during the dead time

$$C_{sw}(v_A)dv_A = I_L dt \tag{2.14}$$

which can be integrated as

$$\int_0^{V_{dd}} C_{sw}(v_A)dv_A = \int_{t_0}^{t_1} I_L dt. \tag{2.15}$$

By (2.15) the minimum inductor current $I_{L,min}$ to achieve full ZVS is

$$I_{L,min} = \frac{\int_0^{V_{dd}} C_{sw}(v_A)dv_A}{t_{\text{dead}}}. \tag{2.16}$$

The time interval t_{D2} in which the body diode of M_2 remains forward biased can be calculated as

$$t_{D2} = t_{\text{dead}} - \frac{\int_0^{V_{dd}} C_{sw}(v_A)dv_A}{I_L}, \tag{2.17}$$

therefore, defined V_D the forward diode voltage, the associated power losses are

$$P_{D2} = I_L V_D t_{D2} f_s. \tag{2.18}$$

On the contrary, if I_L is negative, when M_1 turns off the current flows through the diode D_1. After the dead time, the mosfet M_2 turns on in hard switching as explained in section 2.2. Notice that in this case the energy previously stored in C_{ds2} is *not* recovered.

These considerations suggest that for the case of the half bridge, the best situation occurs when the current is positive in the mosfet which turns off. Therefore, the modulation scheme of converters employing half bridges, may be chosen is such way that the inductor current can be shaped to have the

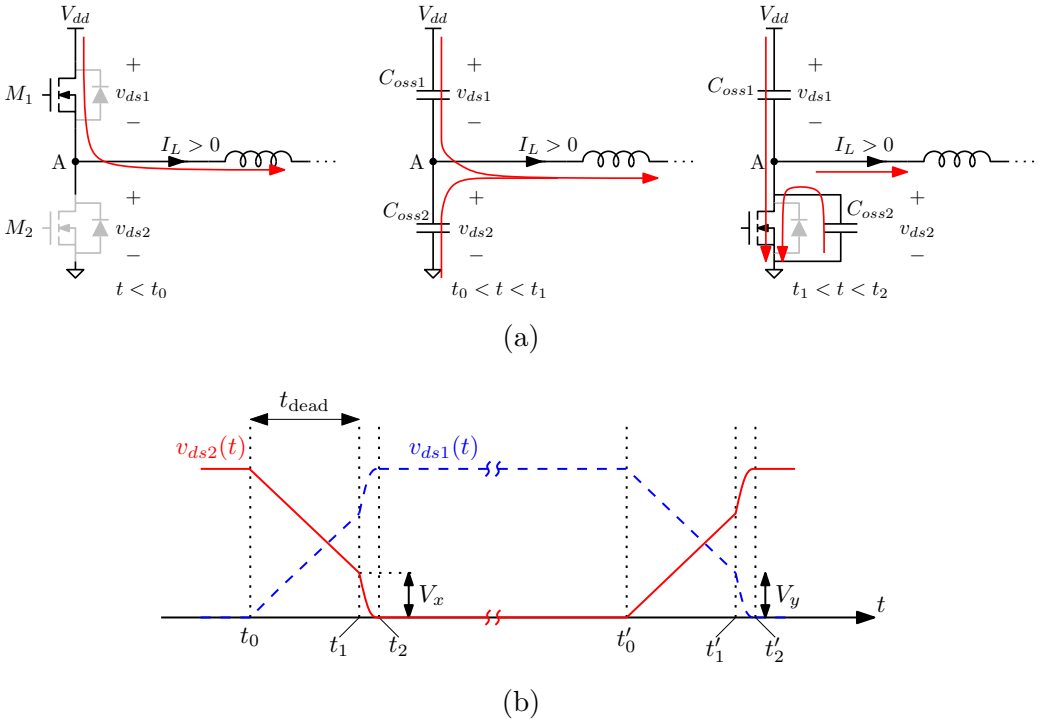


Figure 2.7: Topologies sequence (a) and main waveforms during a partial ZVS transition in a half bridge (b).

appropriate sign.

2.4 Partial soft-switching

Consider the case of the half bridge of Fig. 2.1a in which the current I_L is positive, the mosfet M_1 turns off and, after a dead time t_{dead}, M_2 turns on. This is the situation which allows to recover the energy stored in the parasitic capacitance C_{oss2}. However, if the current I_L is not large enough (i.e. condition (2.16) is not met), at the end of the dead time the capacitance C_{oss2} is not completely discharged and C_{oss1} is not completely charged to V_{dd}. The switching process is sketched in Fig. 2.7. In this case both the discharging process of C_{oss2} and the charging process of C_{oss1} are completed through

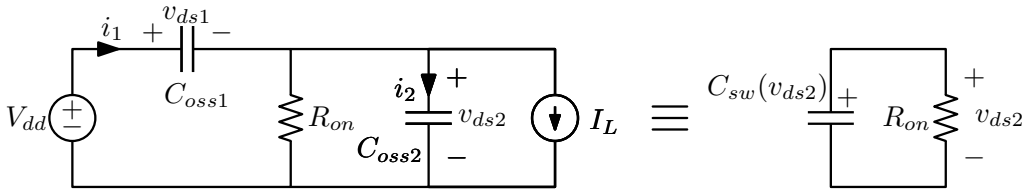


Figure 2.8: Equivalent circuit at the end of the dead time. Transistor M_1 is off and M_2 is on.

the resistive path represented by the newly formed channel of MOSFET M_2. This situation is here referred as *partial soft-switching* because only a portion of the energy stored in C_{oss2} is recovered. From Fig. 2.7, an approximate power losses calculation associated to the case of partial soft-switching can be performed in two steps,

i) Calculation of the switching node voltage $V_x = v_{ds2}(t_1)$ at the end of the dead time.

ii) Calculation of the power losses during the time interval $[t_1 \quad t_2]$ caused by the discharge of C_{oss2} and by the charge of C_{oss1} through the on-resistance of M_2.

The solution of this problem is not simple because C_{oss1} and C_{oss2} are *non-linear* and *voltage-dependent*.

As for *i*), let us calculate V_x numerically by solving the following equation

$$\int_0^{V_x} C_{sw}(v_A)dv_A = \int_0^{t_{\text{dead}}} I_L dt, \tag{2.19}$$

As for *ii*), consider the equivalent circuit of Fig. 2.8 valid during the time interval $[t_1 \quad t_2]$. At time t_2, the transient is assumed to have completed and goal of this discussion is the calculation of the power dissipated by the on-resistance R_{on} of the mosfet. The approach followed hereafter is an extension of the model disclosed in [32] where a method for modeling non-linear

capacitances based on the definition of linear equivalent capacitances is used. In such a method, the calculation is performed in the special case in which the inductor is disconnected (e.g. $I_L = 0$) and therefore the switching node is discharged from V_{dd} to 0V and vice versa. The mentioned model is here reformulated for the case of partial soft-switching, i.e. for a generic value of $v_{ds1}(t_1)$. Notice that in the case we want to model, since the mosfet resistance is small (R_{on} in Fig. 2.8), the capacitance currents $i_1(t)$ and $i_2(t)$ are much greater than I_L. In other words, we can state that the inductor current does not significantly alter the charging-discharging process so that I_L can be neglected. The quick increment of the derivative dv_{ds2}/dt in the time interval $[t_1 \quad t_2]$ with respect to the one in the interval $[t_0 \quad t_1]$ confirms the validity of our hypothesis. The foregoing considerations lead to the following expressions describing the circuit of Fig. 2.8

$$\begin{cases} \dfrac{d}{dt}v_{ds1}(t) = \dfrac{1}{C_{oss1}(V_{dd} - v_{ds2})}i_1(t) \\ \dfrac{d}{dt}v_{ds2}(t) = \dfrac{1}{C_{oss2}(v_{ds2})}i_2(t) \end{cases}. \tag{2.20}$$

Since the current flowing in the resistor R_{on} is

$$\frac{v_{ds2}(t)}{R_{on}} \approx \frac{v_{ds2}(t)}{R_{on}} + I_L = i_1(t) - i_2(t) \tag{2.21}$$

the dynamic equation describing the circuit of Fig. 2.8 is

$$\left[C_{oss1}(V_{dd} - v_{ds2}) + C_{oss2}(v_{ds2})\right] \frac{d}{dt}v_{ds2}(t) = -\frac{v_{ds2}(t)}{R_{on}} \tag{2.22}$$

that can be written in terms of the switching capacitance

$$C_{sw}(v_{ds2})\frac{d}{dt}v_{ds2}(t) = -\frac{v_{ds2}(t)}{R_{on}}. \tag{2.23}$$

Equation (2.23) shows that the circuit of Fig. 2.8 is equivalent of the circuit formed by the switching node capacitance $C_{sw}(v_{ds2})$ and the on-resistance of the mosfet as shown in Fig. 2.8. Therefore, the energy dissipated on R_{on} can be conveniently calculated using the latter equivalent circuit yielding

$$E_x = \int_0^{V_x} vC_{sw}(v)dv. \tag{2.24}$$

In a similar way, named V_y the voltage shorted at the turn-off of M_2 and turn-on of M_1 (see Fig. 2.7), the corresponding lost energy is

$$E_y = \int_{V_{dd}-V_y}^{V_{dd}} (V_{dd} - v)C_{sw}(v)dv. \tag{2.25}$$

The total power losses in the case of partial soft switching are then

$$P_{part,ZVS} = f_s(E_x + E_y). \tag{2.26}$$

When particularized to the case of $I_L = 0$, we have $V_x = V_y = V_{dd}$ and (2.26) can be expressed in terms of an equivalent capacitance C_{eq} as explained in [32],

$$P_{part,ZVS} = 2C_{eq}V_g^2 \tag{2.27}$$

where C_{eq} is the linear equivalent capacitance of the mosfet which have the same amount of stored charge at V_g as the non linear capacitance C_{oss},

$$C_{eq} = \frac{1}{V_g}\int_0^{V_g} C_{oss}(v)dv. \tag{2.28}$$

Chapter 3

Steady state analysis of the DHB-SRC

Contents

3.1 Introduction

In this chapter the steady state analysis of the Dual Half Bridge Series Resonant Converter (DHB-SRC) illustrated in Fig. 3.1a is presented. The analysis is formulated for a general combination of duty cycle/phase shift modulation

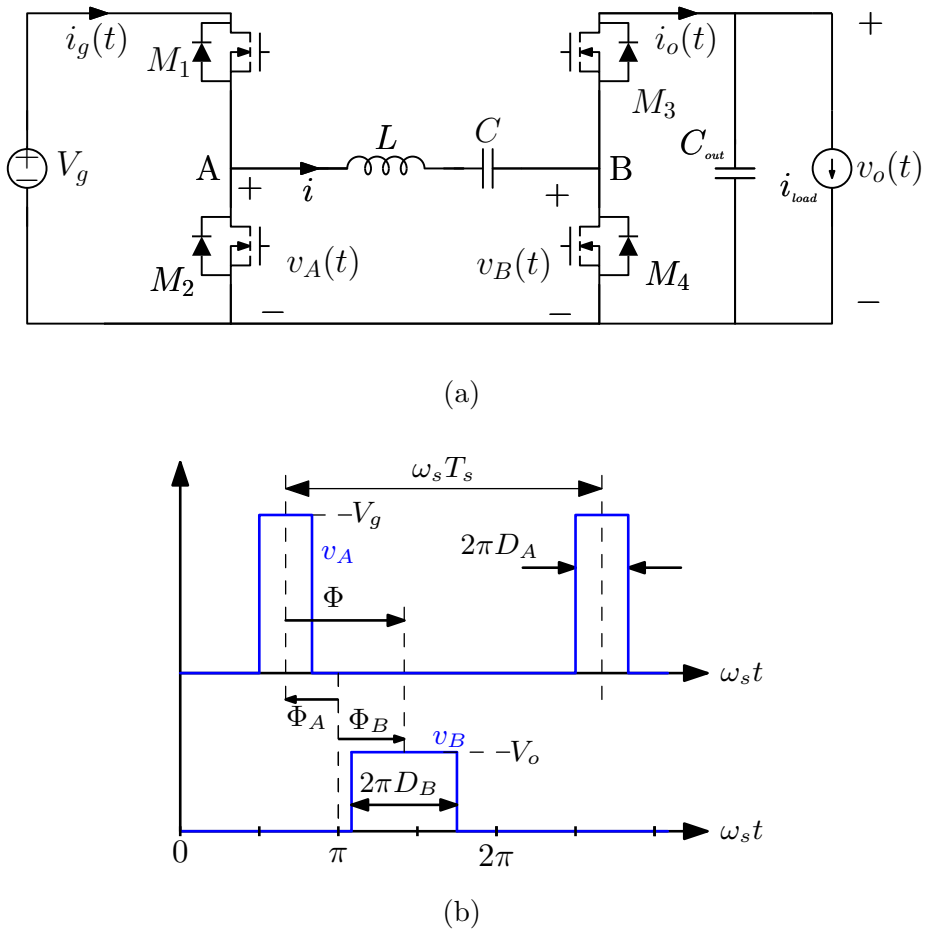


Figure 3.1: Schematic diagram of the Dual Half Bridge - Series Resonant Converter (a) and Voltage waveforms at node A and B (b).

in order to be readily applicable to the online efficiency optimization strategy discussed in the next chapter.

In Fig. 3.1a the input half bridge behaves as an inverter and produces the waveform $v_A(t)$ at the node A from the battery voltage V_g. On the other hand, the output half bridge produces the waveform $v_B(t)$ at the node B. Voltage waveforms $v_A(t)$ and $v_B(t)$ produced by each leg are illustrated in Fig. 3.1b for an arbitrary operating point. Parameters of waveforms $v_A(t)$ and $v_B(t)$, are duty cycles D_A, D_B and phase angles Φ_A, Φ_B. Notice that, with

the definition here used, phase Φ_A has the meaning of a leading angle, while Φ_B has the meaning of a phase delay. Therefore, the total phase difference Φ between $v_A(t)$ and $v_B(t)$ is

$$\Phi = \Phi_A + \Phi_B. \tag{3.1}$$

In steady state, voltages waveforms $v_A(t)$ and $v_B(t)$ are periodic with period

$$T_s = \frac{2\pi}{\omega_s} = \frac{1}{f_s} \tag{3.2}$$

where f_s is the switching frequency and ω_s is the angular switching frequency. The voltage $v_A(t) - v_B(t)$ is applied to a LC series resonant circuit producing the resonant tank current $i(t)$, which is in turn rectified by the output half bridge to produce the output current $i_o(t)$. The capacitor C_{out} is placed to filter the current $i_o(t)$. The following parameters can be defined:

- $Z_o = \sqrt{\frac{L}{C}}$ is the characteristic impedance of the resonant tank.
- $\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{LC}}$ is the resonant angular frequency.
- $r = \frac{\omega_o}{\omega_s}$ is the ratio between resonant and switching frequency.
- $M = \frac{V_o}{V_g}$ is the conversion ratio of the converter.

Among the methodologies presented in literature, the two most commonly used approaches are the one based on the analytic determination of current waveforms [33] and the one based on the fundamental harmonic approximation [15, 19, 22]. The first is based on the solution of the differential equations governing the dynamics of the resonant tank inductor current $i(t)$ and the resonant tank capacitor voltage $v_C(t)$ during each of the phases inside the

switching period. In order to obtain manageable equations, the lossless approximation is commonly employed. Therefore, this methodology is only valid if it is reasonable to assume that non-idealities do not significantly modify the converter operation.

The methodology based on the fundamental harmonic approximation consists in neglecting all the higher order harmonics and it is justified by the passband nature of the resonant tank. This way all the current and voltage waveforms are supposed to be sinusoidal and the calculation of the quantities of interest such us the power delivered to the load are straightforward. When the converter of Fig. 3.1a is driven above resonance $f_s > f_o$, because of the passband nature of the resonant tank, higher order harmonics are automatically filtered. On the contrary, if the converter is driven below frequency, the fundamental harmonic approximation is valid under the condition that the resonant frequency f_0 is placed close enough to the switching frequency. If switching frequency is much lower than the resonant one, other harmonics may be amplified by the resonant circuit and the fundamental harmonic approximation is no longer valid. In this work, the resonant converter of Fig. 3.1a is driven above resonance ($r < 1$).

This chapter is organized as follows: Section 3.2 reviews the *analytical* methodology based on the calculation of the exact current and voltage waveforms. Section 3.3, on the other hand, illustrates the analysis of the DHB-SRC is the methodology based on the fundamental harmonic approximation. In section 3.4, it is shown that the duty cycle modulation can cause a high distortion in some operating regions. The limitations of the fundamental harmonic approximation are highlighted for this case and a *multi-harmonic approach* is presented.

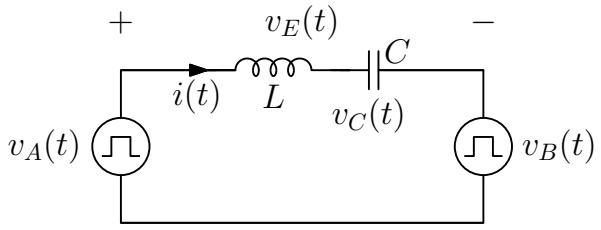


Figure 3.2: Equivalent circuit of the tank network of a series resonant converter.

3.2 Steady state analysis of the DHB-SRC based on exact waveform calculation

Consider the simplified circuit describing a resonant tank supplied by waveforms $v_A(t)$ and $v_B(t)$ sketched in Fig. 3.2. The switching period is in general divided in m *subintervals* $j = 1 \div m$, each one corresponding to a converter topological configuration. For each subinterval j, dynamic equations describing the system are:

$$\begin{cases} \dfrac{d}{dt} i^{(j)}(t) = \dfrac{1}{L}\left(v_E^{(j)}(t) - v_C^{(j)}(t)\right) \\ \dfrac{d}{dt} v_C^{(j)}(t) = \dfrac{1}{C} i^{(j)}(t) \end{cases} \tag{3.3}$$

where $v_E^{(j)}(t)$ is the voltage applied to the resonant tank and its value depends on the switches state as shown in Tab. 3.1.
Defining the base quantities

$$\begin{aligned} V_n &\triangleq V_g : \text{base voltage} \\ I_n &\triangleq \frac{V_n}{Z_0} : \text{base current} \end{aligned} \tag{3.4}$$

normalized solutions of (3.3) are:

Table 3.1: Voltage applied to the resonant tank as function of the switches configuration.

M1	M2	M3	M4	$v_E(t)$
ON	OFF	OFF	ON	V_g
ON	OFF	ON	OFF	$V_g - V_o$
OFF	ON	OFF	ON	0
OFF	ON	ON	OFF	$-V_o$

$$\begin{cases} i_n^{(j)}(\theta) = I_{n,0}^{(j)} \cos(r\theta) - \left(V_{Cn,0}^{(j)} - V_{En}^{(j)}\right) \sin(r\theta) \\ v_{Cn}^{(j)}(\theta) = \left(V_{Cn,0}^{(j)} - V_{En}^{(j)}\right) \cos(r\theta) + I_{n,0}^{(j)} \sin(r\theta) + V_{En} \end{cases} \tag{3.5}$$

where $\theta = \omega_s t$ and

- $I_{n,0}^{(j)}$ is the normalized value of the current at the beginning of the subinterval j.
- $V_{Cn,0}^{(j)}$ is the normalized value of the voltage v_C at the beginning of the subinterval j.
- $V_{En}^{(j)}$ is the normalized value of the voltage applied to the resonant tank during the interval j.

Eq. (3.5) are the representation on the normalized plane of the resonant current and resonant voltage. In [33], where a series resonant converter with an output diodes bridge is presented, the solution (3.5) is written as

$$i_n(\theta)^2 + (v_{Cn}(\theta) - V_{En})^2 = \rho^2 \tag{3.6}$$

where

$$\rho^2 = I_{n,0}^2 + (V_{Cn,0} - V_{En})^2 . \tag{3.7}$$

Expression (3.6) shows that the point $(v_{Cn}(t), i_n(t))$ describes an arc on the normalized state space centered in $c = (V_{En}, 0)$ with radius ρ. In that case the problem of the calculation of transistors turn-on and turn-off angles become a geometrical problem.

For the case of the dual active bridge converter, turn-on and turn-off instants are univocally individuated by the phase shift and duty cycles.

Values of initial conditions $V_{Cn,0}^{(j)}$ and $I_{n,0}^{(j)}$ are calculated for each phase of the switching period imposing the *continuity of waveforms* $v_c(t)$ and $i(t)$ and the output current can be calculated integrating the resonant current in the active period of transistor M_3. In the next session the problem is solved for a generic switching sequence. Notice that the switching sequence depends on the value of phase shift and duty cycles, therefore the calculation has to be performed for all possible sequences which, for the converter of Fig. 3.1a are seven. In section 3.2.1 a systematic method to find initial conditions of equation 3.5 is shown for a generic switching sequence. In section 3.2.2 the method is used for the case in which v_A and v_B are square waveforms ($D_A = D_B = 0.5$) and with positive phase shift $\varphi > 0$. Another approach which allows to calculate an approximate but more general result will be presented in section 3.3.

3.2.1 General method

The analytical determination of the current waveforms requires a systematic method for complex topologies. The outcome is the mathematical expression of phase currents as a function of phase shift, duty cycles and other design parameters of the converter. The integral of such current over those subintervals partecipating to the power transfer to the output gives the average output current.

As said above, each switching period is divided in m subintervals. Let us

indicate the duration of the j-th subinterval with δ_j, here expressed in radiants. By (3.5), the value of the state variable x ($x \in \{i_n, v_{Cn}\}$ for the DHB-SRC) *at the end* of the j-th subinterval can be written as function of the initial value $X_0^{(j)}$ and is here referred as $x_f^{(j)}$. Imposing the continuity of the state variable during the switching instants, and indicating with $\mathbf{x}_0^{(j)}$ and $\mathbf{x}_f^{(j)}$ the vectors of initial and final values of the subinterval j

$$\begin{aligned} \mathbf{x}_0^{(j)} &= \begin{bmatrix} I_{n,0}^{(j)} & V_{Cn,0}^{(j)} \end{bmatrix}^T \\ \mathbf{x}_f^{(j)} &= \begin{bmatrix} i_n^{(n)}(\delta_j) & v_{Cn}(\delta_j) \end{bmatrix}^T, \end{aligned} \tag{3.8}$$

we can write

$$\begin{aligned} \mathbf{x}_f^{(j)} &= \mathbf{M}_j \mathbf{x}_0^{(j)} + \mathbf{N}_j V_{En}^{(j)} \\ &= \mathbf{M}_j \mathbf{x}_f^{(j-1)} + \mathbf{N}_j V_{En}^{(j)}. \end{aligned} \tag{3.9}$$

Let us define the matrix

$$\mathbf{M}_{m,j} = \prod_{k=j}^{m} \mathbf{M}_k. \tag{3.10}$$

Iterating (3.9) we can obtain the expression $\mathbf{x}_f^{(m)}$ as function of the initial values $\mathbf{x}_0^{(1)}$

$$\begin{aligned} \mathbf{x}_f^{(m)} &= \mathbf{M}_{m,1} \mathbf{x}_0^{(1)} + \left(\sum_{j=1}^{m-1} \mathbf{M}_{m,j+1} \mathbf{N}_j V_{En}^{(j)} \right) + \mathbf{N}_m V_{En}^{(m)} \\ &= \mathbf{M}_{m,1} \mathbf{x}_0^{(1)} + \mathbf{F} \end{aligned}. \tag{3.11}$$

Finally, imposing the steady state condition

$$\mathbf{x}_f^{(m)} = \mathbf{M}_{m,1} \mathbf{x}_0^{(1)} + \mathbf{F} = \mathbf{x}_0^{(1)}, \tag{3.12}$$

the initial state variable vector $\mathbf{x}_0^{(1)}$ can be calculated giving

$$\mathbf{x}_0^{(1)} = (\mathbf{I} - \mathbf{M}_{m,1})^{-1} \mathbf{F}, \tag{3.13}$$

where $\mathbf{I}$ is the identity matrix.

3.2.2 Case $D_A = D_B = 0.5$

As anticipated, the analysis disclosed in section 3.2.1 may be done for all the switching sequences to give a complete result. In this section the case of square waveform ($D_A = D_B = 0.5$) is presented. As explained above, the steps to follow are the following:

i) Identification of the switching sequence.

ii) Calculation of matrices $\mathbf{M}_{m,1}$, $\mathbf{F}$ and calculation the initial conditions $\mathbf{x}_0^{(1)}$ using (3.13).

iii) Calculation of the average output power integrating the instantaneous power at port B.

As for *i*), consider the main waveforms of the converter shown in Fig. 3.3 which allows to write the table 3.2.
Following the steps described in 3.2.1 and using the parameters listed in Tab. 3.2 it is possible to write matrices $\mathbf{M}_{m,1}$, $\mathbf{F}$

$$\mathbf{M}_{m,1} = \begin{bmatrix} \cos(2\pi r) & -\sin(2\pi r) \\ \sin(2\pi r) & \cos(2\pi r) \end{bmatrix} \tag{3.14}$$

$$\mathbf{F} = \begin{bmatrix} \sin(2\pi r) - \sin(\pi r) + M\{\sin[r(\pi - \varphi)] - \sin[r(2\pi - \varphi)]\} \\ \cos(\pi r) - \cos(2\pi r) + M\{\cos[r(2\pi - \varphi)] - \cos[r(\pi - \varphi)]\} \end{bmatrix} \tag{3.15}$$

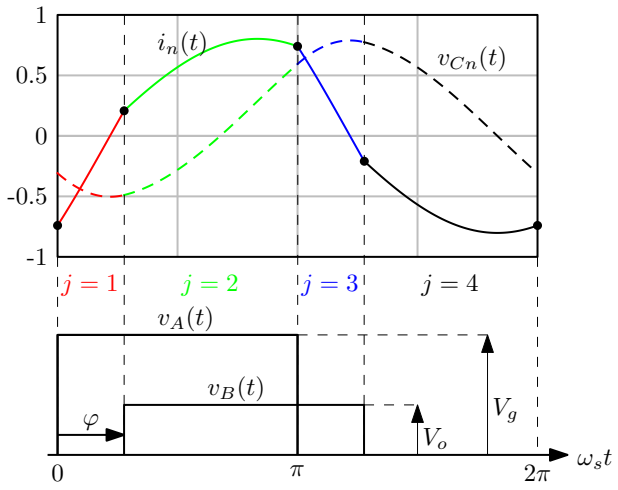


Figure 3.3: Main waveforms of the converter in steady state.

Table 3.2: Switching sequence for the case $D_A = D_B = 0.5$.

Phase	M1	M2	M3	M4	$v_E(t)$	$V_{En}^{(j)}(t)$	δ_j
$j=1$	on	off	off	on	V_g	1	φ
$j=2$	on	off	on	off	$V_g - V_o$	$1-M$	$\pi-\varphi$
$j=3$	off	on	on	off	$-V_o$	$-M$	φ
$j=4$	off	on	off	on	0	0	$\pi-\varphi$

and finally calculate the initial conditions $I_{n,0}^{(j)}$ and $V_{Cn,0}^{(j)}$

$$\begin{cases} I_{n,0}^{(j)} = \frac{1}{2}\csc(r\pi)\left[M\cos(r\varphi) - M\cos(r(\varphi-\pi)) + \cos(\pi r) - 1\right] \\ V_{Cn,0}^{(j)} = \frac{1}{2}\csc(r\pi)\left[M(\sin\left(r(\varphi-\pi)\right) - \sin(r\varphi)) + \sin(\pi r)\right] \end{cases} \tag{3.16}$$

Integrating the current expression over the subintervals in which M_3 is on ($j=2$ and $j=3$), the average output current or, equivalently, the average output power can be calculated. Defining the base power

$$P_n = \frac{V_g^2}{Z_0} \tag{3.17}$$

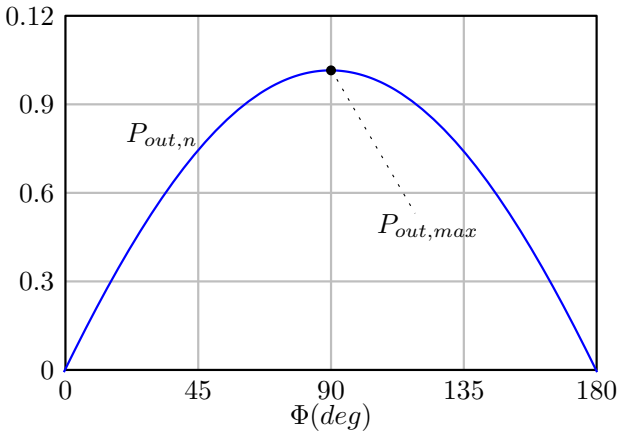


Figure 3.4: Normalized output power plotted with parameters $r = 0.67$ and $M = 5/12$.

the final expression of the normalized output power $P_{out,n}$ is the following

$$P_{out,n} = \frac{P_{out}}{P_n} = \frac{M}{2\pi r}\left(\frac{\cos\left(r\frac{\pi - 2\varphi}{2}\right)}{\cos\left(r\frac{\pi}{2}\right)} - 1\right) \tag{3.18}$$

Expression (3.18) shows that the maximum power capability occurs for

$$\varphi = \Phi_{\max} = \frac{\pi}{2}. \tag{3.19}$$

In Fig. 3.4 the expression (3.18) is plotted for the case $r = 0.67$ and $M = \frac{5}{12}$.

3.3 Analysis based on fundamental harmonic approximation

In previous sections the steady state analysis of the DHB-SRC was described based on an analytical approach. In general, the method yields a number of expressions of the output power equal to the number of possible switching

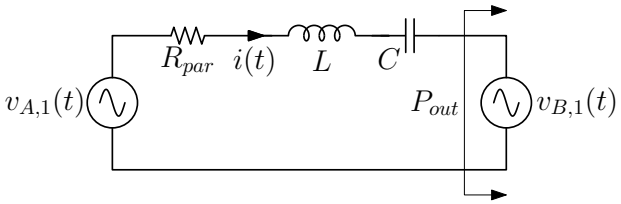


Figure 3.5: Resonant tank representation in the fundamental harmonic approximation.

patterns. In this section an approximate method based on the *Fundamental Harmonic Approximation* (FHA) is explained. The method allows to calculate a general expression of the output power that is independent of the switching sequence and is in general accurate enough for the design standpoint. Under the FHA, the resonant circuit can be drown as shown in Fig. 3.5. The parasitic resistance R_{par} embeds the resonant tank inductor and capacitor ESR (ESR_L and ESR_C) as well as of the on-resistance R_{on} of the electronic switches

$$R_{par} = ESR_L + ESR_C + 2R_{on}. \tag{3.20}$$

The quality factor Q of the resonant tank is defined as

$$Q = \frac{Z_0}{R_{par}}. \tag{3.21}$$

Sinusoidal waveforms $v_{A,1}(t)$ and $v_{B,1}(t)$ are the fundamental harmonics of $v_A(t)$ and $v_B(t)$

$$\begin{cases} v_{A,1}(t) = \dfrac{2}{\pi} V_g \sin(\pi D_A) \sin(\omega_s t + \Phi_A) \\ v_{B,1}(t) = \dfrac{2}{\pi} V_o \sin(\pi d_B) \sin(\omega_s t - \Phi_B) \end{cases} \tag{3.22}$$

and associated phasors are

$$\begin{cases} \vec{\boldsymbol{V}}_A = \dfrac{2}{\pi} V_g \sin(\pi D_A)\, e^{+j\Phi_A} \\ \vec{\boldsymbol{V}}_B = \dfrac{2}{\pi} V_o \sin(\pi d_B)\, e^{-j\Phi_B} \end{cases} . \tag{3.23}$$

In this work, the amplitude of a phasor is the amplitude of the associated fundamental harmonics. The power transferred to the load can be calculated as the active power absorbed by the generator $v_{B,1}$

$$P_{out} = \Re\left[\frac{1}{2}\vec{\boldsymbol{V}}_B \vec{\boldsymbol{I}}^*\right] \tag{3.24}$$

which leads to the expression

$$\begin{aligned} P_{out} = {} & 2QrM \sin(\pi D_B) \times \\ & \times \frac{r\cos(\Phi)\sin(\pi D_A) - rM\sin(\pi D_B) + Q\left(1-r^2\right)\sin(\pi D_A)\sin(\Phi)}{\pi^2 Z_0 \left[r^2 + Q^2\left(1-r^2\right)^2\right]} \end{aligned} \tag{3.25}$$

Expression 3.25 shows that the power transfer can be controlled by acting on the control inputs D_A, D_B and Φ which represent the degrees of freedom of this topology. This feature can be exploited to perform a multivariable control which regulates the output voltage and simultaneously uses the degrees of freedom not directly used to perform the regulation to achieve further goals like efficiency optimization, EMI reduction or dynamics improvement. This thesis focuses on online efficiency optimization and in chapter 4 the problem of the optimization for the DHB-SRC is discussed.

The maximum power capability $P_{\max} = P_{out}(\Phi_{\max}, D_{A,\max}, D_{B,\max})$ is calcu-

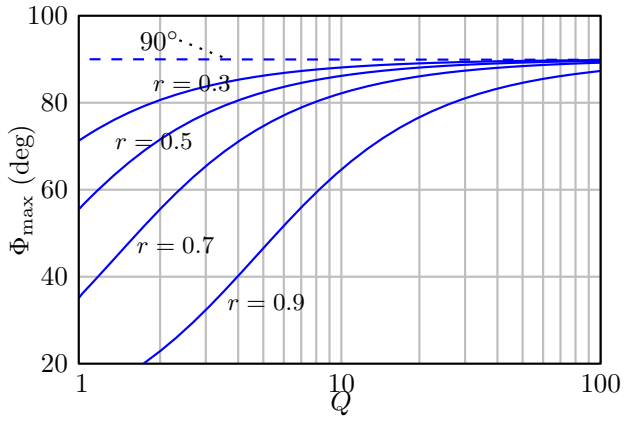


Figure 3.6: Phase shift of the maximum power point as function of Q for some values of parameter r.

lated solving the equations system

$$\begin{cases} \dfrac{\partial}{\partial \Phi} P_{out} = 0 \\ \dfrac{\partial}{\partial D_A} P_{out} = 0 \\ \dfrac{\partial}{\partial D_B} P_{out} = 0 \end{cases} \tag{3.26}$$

which yields the solution

$$\begin{cases} \Phi_{\max} = \arctan\left(Q \dfrac{1-r^2}{r^2}\right) \\ D_{A,\max} = 0.5 \\ D_{B,\max} = 0.5 \end{cases} . \tag{3.27}$$

The solution (3.27), shows that the maximum power transfer occurs for $D_A = D_B = 0.5$ while $\Phi_{\max}$ is a function of resonant tank quality factor Q and parameter r. In Fig. 3.6 the value of $\Phi_{\max}$ as function of Q for some values of r is plotted. As can be seen by the figure, $\Phi_{\max}$ tends to 90° for high values of Q (i.e. low values of R_{par}) and decreases as the dissipation effects increase.

For the simple case of *lossless tank* ($Q \to \infty$), the expression (3.25) can be simplified giving the following expression

$$\begin{aligned} P'_{out} &= \lim_{Q \to +\infty} P_{out} \\ &= \frac{2}{\pi^2} \frac{r}{1-r^2} \frac{V_g V_o}{Z_0} \sin(\pi D_A) \sin(\pi D_B) \sin(\Phi) \end{aligned} \tag{3.28}$$

As anticipated, under the FHA and in the lossless tank case, maximum power transfer in the forward direction occurs for $D_A = D_B = 0.5$ and $\Phi = 90°$. At this operating point one has

$$P'_{out,max} = \frac{2}{\pi^2} \frac{r}{1-r^2} \frac{V_g V_o}{Z_0}. \tag{3.29}$$

Expression (3.29) shows that the FHA allows to calculate simple relations which are generally sufficient to design the converter through the choice of parameters r and Z_0.
Dividing both terms of (3.28) by the output voltage V_o, the expression of the output current is obtained

$$I_{out} = \frac{2}{\pi^2} \frac{r}{1-r^2} \frac{V_g}{Z_0} \sin(\pi D_A) \sin(\pi D_B) \sin(\Phi). \tag{3.30}$$

3.4 Multi-harmonic approach

Although the FHA is typically a valid approach to develop useful relations for converter design, such relations may not be accurate enough for the analysis point of view. For instance, in some operating points the spectrum of the inductor current consists of not negligible higher order harmonics. As a consequence, the estimation of switching and conduction losses can be compromised by a not accurate calculation of parameters like current values

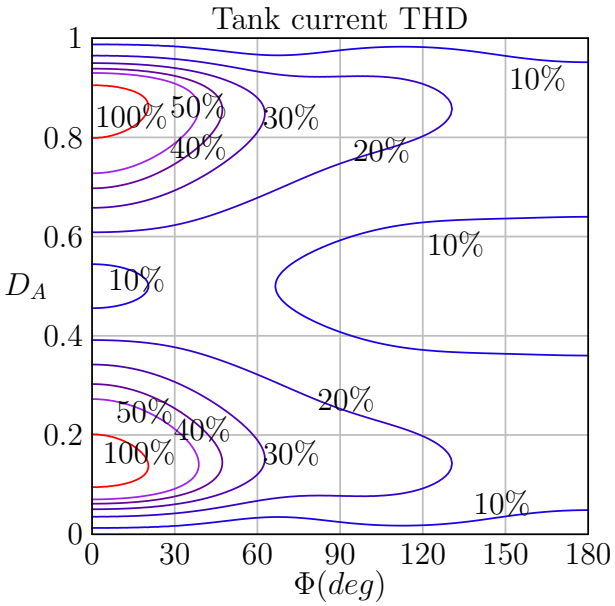


Figure 3.7: Total harmonic distortion of the resonant tank current.

at the switching instants and RMS resonant current.

In order to quantify the validity of the FHA let us define the Total Harmonic Distortion (THD) of the resonant tank current waveform

$$THD = \frac{\sqrt{I_{rms}^2 - I_{rms,1}^2}}{I_{rms,1}}, \tag{3.31}$$

where I_{rms} is the RMS value of the resonant tank current $i(t)$ while $I_{rms,1}$ is the RMS of the fundamental harmonic of $i(t)$. This parameter tends to zero when the distortion is low and grows up for highly distorted waveforms. THD of $i(t)$ is shown in Fig. 3.7 on the $D_B = 0.5$ plane and as a function of D_A and Φ, obtained with the above procedure and by evaluating P_{out} over seven harmonics. Contours of Fig. 3.7 refers to the case of conversion ratio $M = \frac{V_o}{V_g} = \frac{5}{12}$, $r = 0.67$ and resonant circuit quality factor $Q = \frac{Z_0}{R_{par}} = 10$. Notice that around the maximum power point ($D_A = 50\%$, $\Phi = \Phi_{\max}$) the

current distortion is less then 10% so the equation (3.29) can be considered accurate enough for the design. On the other hand, the presence of regions characterized by high THD motivates the use of a multi-harmonic model to analyze the steady state proprieties of the converter. The methodology used for derivation of Eq. 3.28 can be extended for the calculation of the power transferred by the generic n-th harmonic yielding

$$P_{out,n} = 2QrM \sin(n\pi D_B) \cdot \frac{nr\cos(n\Phi)\sin(n\pi D_A) - nrM\sin(n\pi D_B) + Q\left(n^2 - r^2\right)\sin(n\pi D_A)\sin(n\Phi)}{n\pi^2 Z_0\left[Q^2\left(n^2 - r^2\right)^2 + (nr)^2\right]} \tag{3.32}$$

and then the total active power transferred by the converter is evaluated by summing over the spectrum,

$$P_{out} = \sum_{n=1}^{+\infty} P_{out,n}. \tag{3.33}$$

In a similar manner, it is possible to derive analytical expressions for the tank RMS current $I_{rms,n}$ associated with the n-th harmonic, as well as the total tank RMS current. The above considerations allow to approximate the active power, the tank RMS current and the current values during the commutations arbitrarily well by taking a suitable number of terms in the summation. The total RMS current is then evaluated as

$$I_{rms}^2 \approx \sum_{n=1}^{N} I_{rms,n}^2 \tag{3.34}$$

and, being $I_{sw,x}$ the current at the switching instant t_x ($x = 1..4$) one has

$$I_{sw,x} \approx \sum_{n=1}^{N} |I_n| \cos(2\pi n f_s t_x + \arg I_n). \tag{3.35}$$

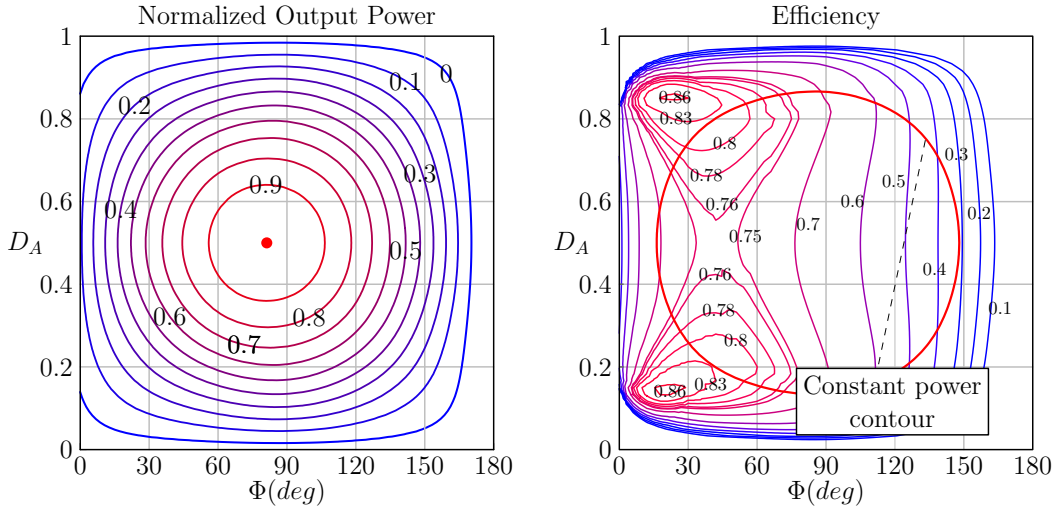


Figure 3.8: Power contours (a) and efficiency contours (b) of a DHB-SRC on the $D_B = 0.5$ plane as function of Φ and D_A.

The switching instants t_x can be directly derived by the knowledge of the operating point (Φ,D_A,D_B):

$$\begin{cases} t_1 = -\dfrac{D_A}{2}T_s \\ t_2 = \dfrac{D_A}{2}T_s \\ t_3 = -\dfrac{D_B}{2}T_s + \dfrac{\Phi}{2\pi}T_s \\ t_4 = \dfrac{D_B}{2}T_s + \dfrac{\Phi}{2\pi}T_s \end{cases} . \tag{3.36}$$

Fig. 3.8a reports the constant contours of normalized output power $P_{out}/P_{out,max}$.

For any given output power level, there are infinite steady-state points in which the system could operate. Such steady-state operating points, however, are not equivalent in terms of efficiency and, in general, a maximum efficiency point exists. As a numerical example, Fig. 3.8b reports the constant efficiency contours in the $D_B = 0.5$ plane with the same parameters of Fig. 3.8a. The

Table 3.3: Parameters of the DHB-SRC Case Study

Switching frequency f_s	200kHz
Input voltage V_g	12V
Output voltage V_o	5V
Maximum output current $I_{load,max}$	1.2A
Tank capacitance C	630nF
Tank inductance L	2.1 µH
Output capacitance C_o	110 µF
Equivalent parasitic resistance R_{par}	0.2Ω
Input current sensing resistance R_{sense}	0.2Ω

efficiency η of a switching converter can be calculated as

$$\eta = \frac{P_{out}}{P_{out} + P_{losses}} \tag{3.37}$$

where P_{losses} are the power losses of the converter calculated including conduction and switching losses of the converter with the specifications listed in Tab. 3.3 in which Infineon OptiMOS®3 power MOSFET of the type IPD036N04L G are used. As for the conduction losses, expression (3.34) is used for the RMS current calculation and seven harmonics are taken into account. For the switching losses contribution, power losses are calculated for each operating point depending on the nature of the commutation (hard-switching, full soft-switching or partial soft-switching) as explained in chapter 2. Expressions (3.35) are used to estimate the current value at the switching instants, limiting the summation to twenty harmonics. In Fig. 3.8b one constant power contour is overlapped to highlight that even though there are infinite operating points compatible with any power value, they are not all

equivalent from the efficiency point of view and therefore the control inputs Φ and D_A can be managed in order to keep the converter in its maximum efficiency point. The latter consideration is the focus of chapter 3.

Chapter 4

Online efficiency optimization technique of a DHB-SRC

Contents

4.1 Introduction

This chapter presents a method to perform an online efficiency optimization for dc-dc Dual Half-Bridge Series Resonant Converters. Section 3.3 shows that for any power level there are infinite compatible operating points that are, in general, not equivalent from the efficiency standpoint.

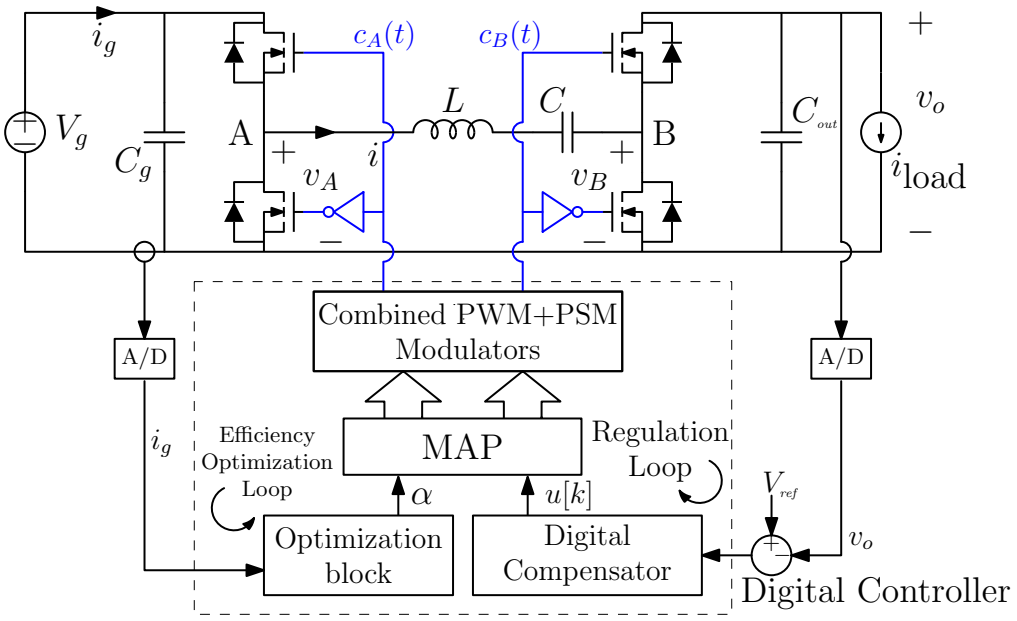


Figure 4.1: Block diagram of the proposed multivariable control.

The described technique implements an advanced modulation scheme which exploits the degrees of freedom inherently available in the converter modulation space in order to simultaneously regulate the output voltage and maintain the system in its maximum efficiency point. The proposed system is illustrated in Fig. 4.1 and includes a fast control loop regulating the output voltage, and a slower optimization loop minimizing the average input current I_g. As for the regulation loop, it relies on a standard PI compensation designed for a given bandwidth and stability margins. On the other hand, the optimization loop is implemented as a minimum current tracking minimizing the average input current I_g. The algorithm employed for minimum current tracking is by all means analogous to the well known Perturb&Observe method commonly employed for Maximum Power Point Tracking in photovoltaic systems [34, 35]. The flowchart of the algorithm is sketched in Fig. 4.2. Effectiveness of such solution is ensured by the uniqueness of the maximum efficiency point for any

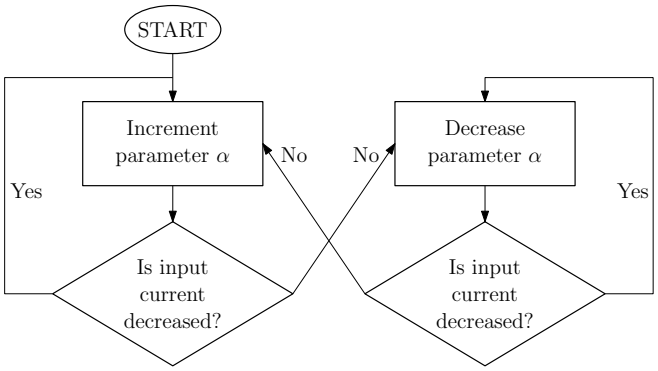


Figure 4.2: Flowchart of the Perturb&Observe algorithm for minimum input current tracking.

given output power level. From this prospect, two important considerations can be done from Fig. 3.8b

1. Controlling the converter on the plane portion $D_A < 0.5$ is equivalent to controlling it in the complementary half-plane ($D_A > 0.5$), both from the power delivering and efficiency standpoint.

2. To within such symmetry of the efficiency characteristic, the power contours presents an *unique* absolute maximum efficiency point.

In Fig. 4.1 the digital regulator produces a discrete time control signal $u[k]$ updated on a clock cycle basis at the beginning of the switching period while the optimization block produces the parameter α. Update frequency of the parameter α is lower than the switching frequency to avoid interference between regulation and optimization loop. The map block translates the pair ($u[k]$,α) into the modulating signal used to drive the converter. In this work, phase shift φ and duty cycle d_A are used to perform the multi variable control while duty cycle d_B is kept constant, therefore modulating signals are the duty cycle reference $u_{d_A}[k]$ and phase shift reference $u_{\varphi}[k]$. The control point

can then be defined as:

$$\mathcal{Q}[k] = (u_{\varphi}[k], u_{d_A}[k]) \tag{4.1}$$

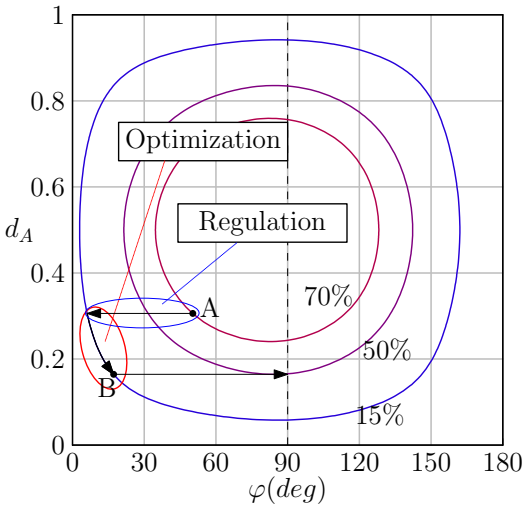
The choice of the map is the key of the method because it defines the adopted control strategy. In section 4.2, regulation issues deriving by a bad choice of the map are illustrated and a solution is then presented in section 4.3.
Fig. 3.8b shows that the plane portion $\varphi > \Phi_{\max}$ is characterized by low efficiency, therefore the converter is made work in the other half plane ($\varphi < \Phi_{\max}$). Notice that because of the power contours symmetry (Fig. 3.8a), this restriction does not limit the power range.
In the following, the modulating signal $u_{d_A}[k]$ is expressed in normalized form so it can assume values in the range $[0, 1]$ while $u_{\varphi}[k]$ is expressed in radians and can assume values in the range $[-\pi, \pi]$.

4.2 Non-interacting control

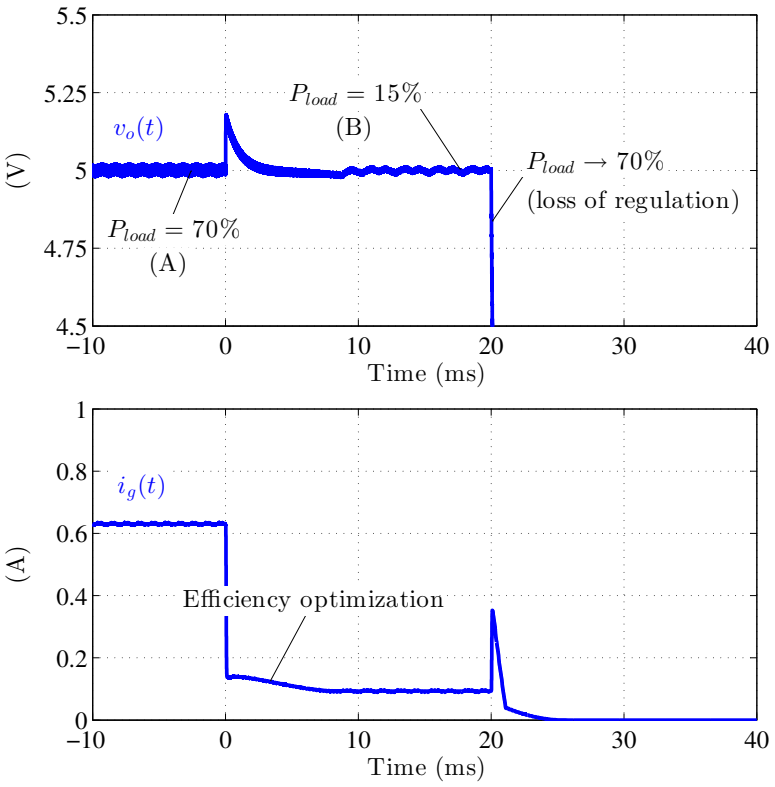
The simplest choice of the map consists in assigning signals $u[k]$ and α directly to the phase shift and duty cycle modulating signal $u_{\varphi}[k]$ and $u_{d_A}[k]$. This approach is here referred to of *Non-Interacting Control*. Following this approach the map can be:

$$\begin{cases} u_{\varphi}[k] = u[k] \\ u_{d_A}[k] = \alpha \end{cases}. \tag{4.2}$$

In this manner, with reference to Fig. 4.3a, the regulation loop acts horizontally along the (φ,d_A) plane while the slower optimization loop would act vertically. The serious drawback of this implementation is observed in the case of abrupt



(a)



(b)

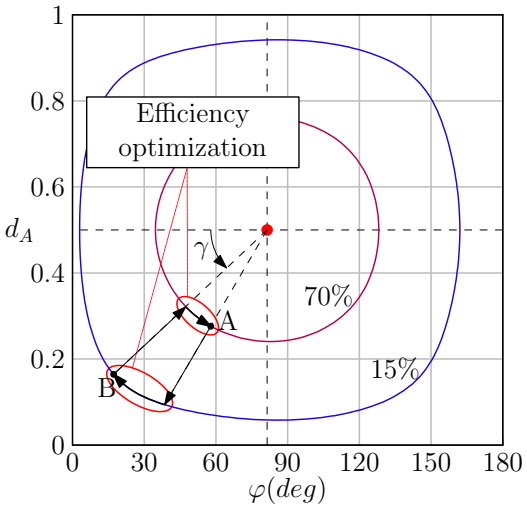
Figure 4.3: Non-Interacting control: operation across different power levels in the control plane (a) and corresponding time-domain waveforms (b).

load step bringing the converter from a low to a higher power level. As example, consider the case in which the system is forced from 70% of the maximum power, to 15% and vice versa. Starting from point A at 70% level, after the load change to level 15% it can quickly find a point on 15% constant current contour. Then, the optimization loop can find the optimal point B. However, after a load change from 70% to 15% starting from B, due to the fast regulation loop acting on φ only, the system would not immediately find a new steady state operating point corresponding to 70% load power, but would rather saturate at $\varphi = 90°$. This point corresponds to a 50% steady-state power, insufficient to meet the load demand. As a result, output voltage regulation would be temporarily or definitively lost. Fig. 4.3b shows the situation by means of a Simulink simulation. As can be seen by the figure, after the load step the output voltage drops and the system is not able to maintain the regulation.

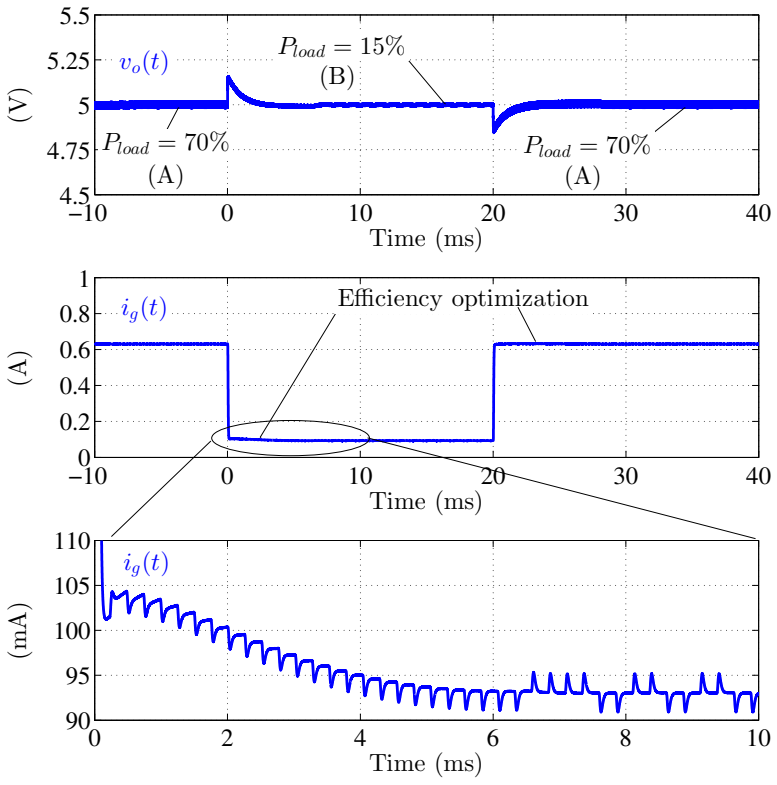
4.3 Interacting control

In order to overcome the regulation issues explained in the previous section the control strategy named *Interacting Control* is proposed. With this method, control point $\mathcal{Q}[k]$ is constrained to lie on a control line always passing through the maximum power point while the optimization loop looks for the best efficiency point by adjusting the slope of the control line. Expressing the phase shift in radians, control line equation is

$$d_A = \alpha \left(\varphi - \Phi_{\max}\right) + 0.5 \tag{4.3}$$



(a)



(b)

Figure 4.4: Interacting control: operation across different power levels in the control plane (a) and corresponding time-domain waveforms (b).

and a possible map is

$$\begin{cases} u_{\varphi}[k] = u[k] \\ u_{d_A}[k] = \alpha\left(u[k] - \Phi_{\max}\right) + 0.5 \end{cases}. \tag{4.4}$$

With this map, $u[k]$ is the phase shift modulating signal while α is the line slope.

To demonstrate the robustness of the interacting control, consider the situation which causes regulation faults when using the *Non-Interacting Control*. In this case, as can be seen by Fig. 4.4a, when the converter is brought from 15% level to 70% of the maximum power, the regulation loop immediately finds the new steady-state point regardless of the severity of the transient. The slower efficiency optimization loop would then gradually rotate the line until the best efficiency is achieved for that power level at point A. Fig. 4.4b illustrates this situation with a Simulink based simulation in which only the dissipative effects caused by the conduction losses are modeled.

Notice that the choice of this map is not unique. For instance, an alternative map that can be used to constrain the control point on the line defined in (4.3) involves the use of polar coordinates. To make the discussion consistent, let us define the normalized control point $\mathcal{Q}_n[k]$,

$$\mathcal{Q}_n[k] = (u_{\varphi,n}[k], u_{d_A,n}[k]) = \left(\frac{u_{\varphi}[k]}{\pi}, u_{d_A}[k]\right). \tag{4.5}$$

In this case a possible map is

$$\begin{cases} u_{\varphi,n}[k] = \Phi_{\max,n} - u[k]\cos\alpha \\ u_{d_A,n}[k] = 0.5 - u[k]\sin\alpha \end{cases}. \tag{4.6}$$

Using this map, $u[k]$ is the distance between the point $\mathcal{Q}_n[k]$ and the normalized maximum power point $(\Phi_{\max,n}, 0.5)$ while α coincides with the angle γ formed by line $u_{d_A} = 0.5$ and the line individuated by points $(\Phi_{\max,n}, 0.5)$ and $\mathcal{Q}_n[k]$.

However, for low power applications low complexity calculations are typically preferable to minimize the controller power consumption. For this reason, map defined by (4.4) is more suitable than the one defined by (4.6) and it will be used throughout this thesis.

4.4 Implementation

The proposed multivariable control is prototyped with parameter listed in Tab. 3.3. For faster prototyping and testing of the digital technique, the voltage regulation and the optimization algorithm are implemented on a Cyclone-II FPGA development board from Altera. Sensing and A/D path for the input current is designed for a resolution of 1 mA/LSB. As previously anticipated in chapter 3, the parasitic resistance R_{par} models MOSFETs on-resistances as well as the resonant tank equivalent resistance. As for the minimum input current tracking algorithm, it is clocked at $T_{clk} = 1$ms in order to allow the output voltage regulation loop to settle to a new steady-state point before the control line slope is further updated. For the Perturb&Observe algorithm to work properly and reach the absolute maximum efficiency point, the latter must be unique and no relative maxima should exist in the efficiency vs. duty cycle plots. Otherwise, the system could reach a suboptimal steady-state point. A preliminary experimental characterization of the converter efficiency is performed and illustrated in Fig. 4.5 for different output power levels and as a function the parameter α expressed in rad^{-1}. Correspondingly,

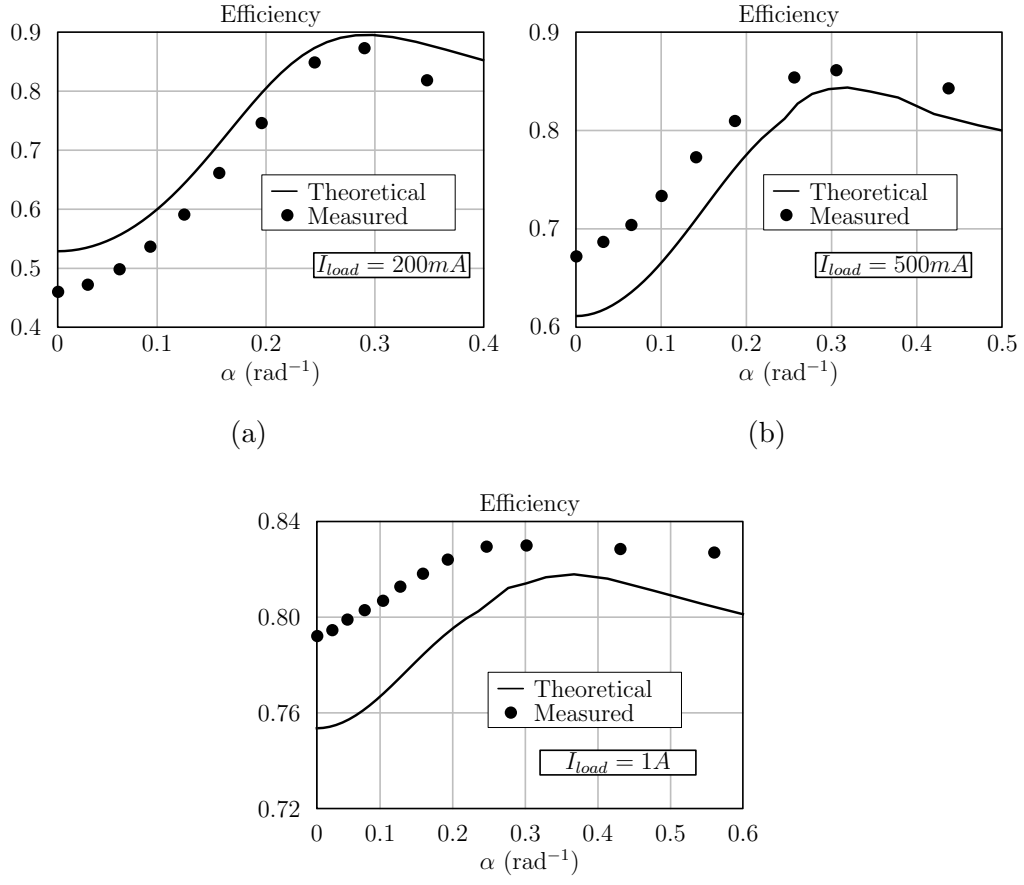


Figure 4.5: Experimental verification of the uniqueness of the efficiency maximum point.

theoretical efficiency calculated with the model derived in section 3.4 is shown. The value of R_{par} used in this work and reported in Tab 3.3 is obtained by the expression

$$R_{par} = ESR_L + 2R_{on}, \tag{4.7}$$

where ESR_L is the inductor resistance measured at the switching frequency using an impedance analyzer. The value of the mosfet on-resistance R_{on} is the one indicate in the device data sheet. Experimental results confirm the

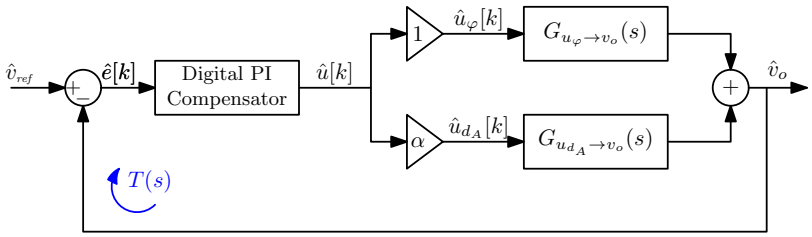


Figure 4.6: Simplified small-signal block diagram of the system.

existence of a unique maximum efficiency point for all power levels.

4.5 Regulation loop design

During a generic transient bringing the system to a new best efficiency point, a large area of the control space can be potentially spanned. For this reason, the control space needs to be analyzed in order to assess the stability of the system. As explained in section 4.3, the regulation loop moves the control vector on the straight line passing on the maximum output power point. The transfer functions of interest are those from modulating signals $u_{\varphi}[k]$ and $u_{d_A}[k]$ to the output voltage $v_o(t)$ indicated as $G_{u_{\varphi}\to v_o}(s)$ and $G_{u_{d_A}\to v_o}(s)$. The simplified block diagram describing the dynamics of the regulation loop is sketched in Fig. 4.6. The regulation loop relies on a standard PI compensation designed for a given bandwidth and stability margins. In this section it is assumed that the control to output transfer functions of the converter have been derived according to the modeling methodology discussed in chapter 9. Such a methodology permits to represent the further dynamics introduced by the sampled nature of the regulator and modulators with analog transfer functions. The PI regulator design is therefore performed considering the

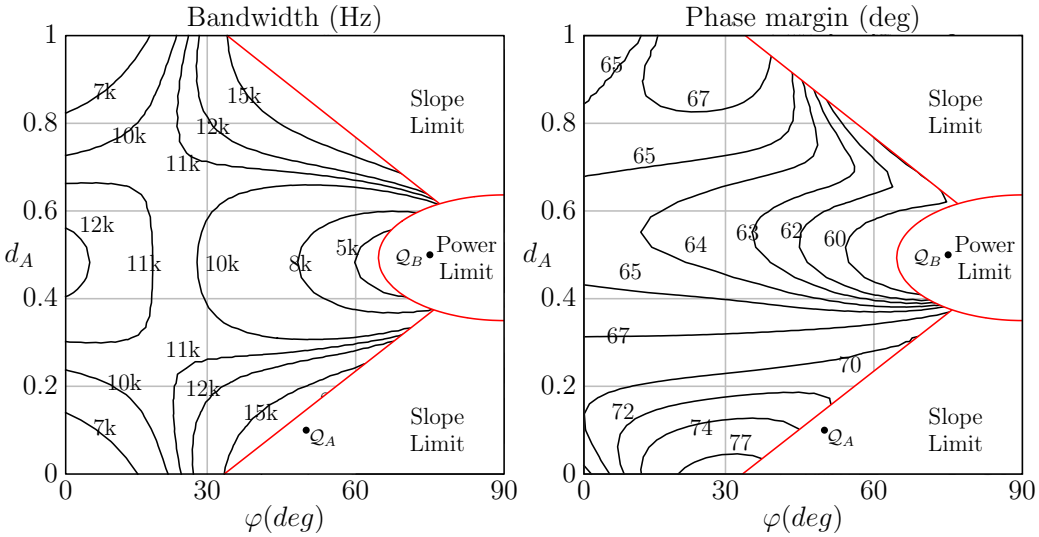


Figure 4.7: (a) Control bandwidth and (b) phase margin of the regulation loop on the control plane.

conventional analog transfer function

$$G_{PI}(s) = K_i \frac{1 + \frac{s}{\omega_z}}{s}. \tag{4.8}$$

The integral gain K_i is numerically chosen in order to obtain a bandwidth range of about [5kHz, 15kHz] over the entire control plane. The angular frequency ω_z of the PI zero is then chosen as high as possible to maximize the loop gain, with the constraint of a minimum phase margin of about 60° over the entire plane. The bandwidth and phase margin of the loop are plotted on the control plane in Fig. 4.7. As shown in this figure, some prohibited regions are defined:

1. The first prohibited region is delimited by the power limit. Fig. 4.8 plots the DC slope of the static characteristic (3.33). As can be seen by the figure, the power regulation capability of the converter in the

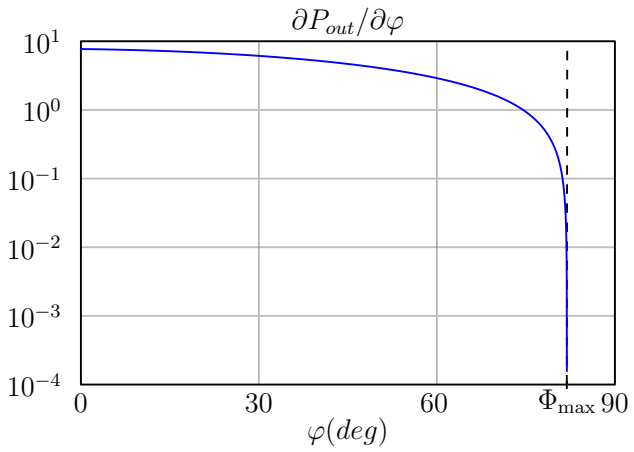


Figure 4.8: Static gain of the output power characteristic.

neighborhood of the maximum power point degrades to zero, and consequently the control loop gain reduces to zero as well. For instance, in the operating point $\mathcal{Q}_A = (\varphi = 75°, d_A = 0.5)$ the Bode plot is the one shown in Fig. 4.9a. Notice that in this case the regulation bandwidth is only 2kHz.

2. The other two prohibited regions are delimited by the slope limit of the control line. As can be seen by Fig. 4.6, if parameter α tends to infinite (e.g. the control line gets vertical), amplitude loop gain increases as well with consequent increment of the system bandwidth. This fact could bring the system to instability because of reduced phase margin or causes multiple 0dB crossings in the Bode diagram generated by high frequency resonances as shown in Fig. 4.9b. This figure shows the situation in the operating point $\mathcal{Q}_B = (\varphi = 50°, d_A = 0.1)$.

The limitation imposed by the slope limit can be acceptable if maximum efficiency points are always located into the permitted region. Even though in this case study this condition is met, such limitation can compromise the generality of the approach. A possible solution involves the use of a *dynamic*

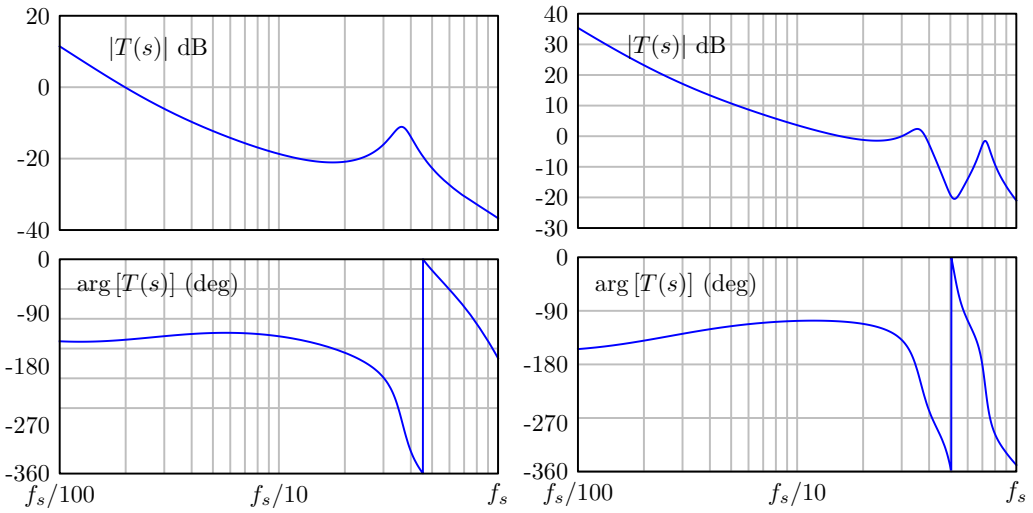


Figure 4.9: Bode diagrams of the loop gain (a) in the operating point $\mathcal{Q}_A$ and (b) in the operating point $\mathcal{Q}_B$.

map. For instance, consider the normalized control plane of Fig. 4.10. The normalization is the one described in (4.5) and here reported for clarity,

$$\begin{cases} u_{\varphi,n}[k] = \dfrac{u_{\varphi}[k]}{\pi} \\ u_{d_A,n}[k] = u_{d_A}[k] \end{cases}. \tag{4.9}$$

When the control point is above the diagonal line $u_{d_A,n} = u_{\varphi,n}$, the map

$$\begin{cases} u_{\varphi,n}[k] = u[k] \\ u_{d_A,n}[k] = \alpha\,(u[k] - 0.5) + 0.5 \end{cases}, \tag{4.10}$$

which corresponds to the map (4.4) previously defined.

On the contrary, when the control point moves below the diagonal, the used

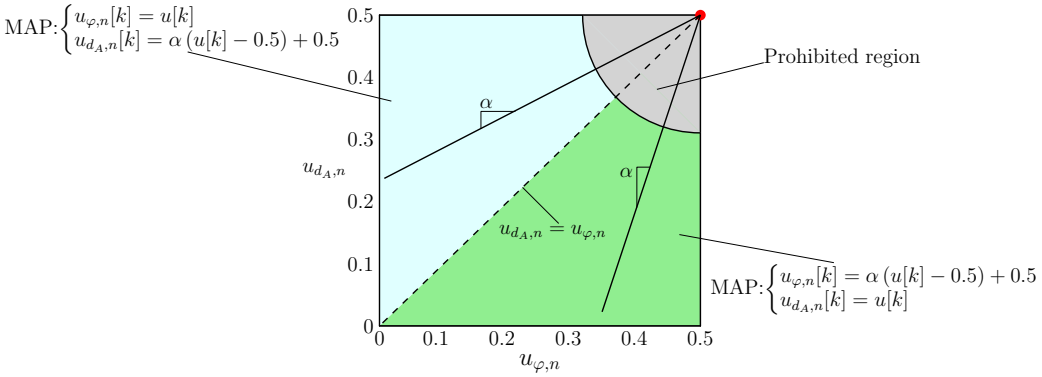


Figure 4.10: Modified map used to solve stability issues due to high values of parameter α.

map is:

$$\begin{cases} u_{\varphi[k],n} = \alpha\,(u[k] - 0.5) + 0.5 \\ u_{d_A,n}[k] = u[k] \end{cases}. \tag{4.11}$$

With this strategy, the parameter α is always upper limited

$$\alpha \in [-1, 1], \tag{4.12}$$

and the only prohibited region is the one delimited by the power limit.

Fig. 4.11 shows the obtained bandwidth and phase margin over the control plane using the control strategy just defined.

Notice that bandwidth and phase margin contours of Fig. 4.11 are continuous also along the diagonal $u_{d_A,n} = u_{\varphi,n}$. This nice characteristic is consequence of the choice of the normalization defined in (4.9).

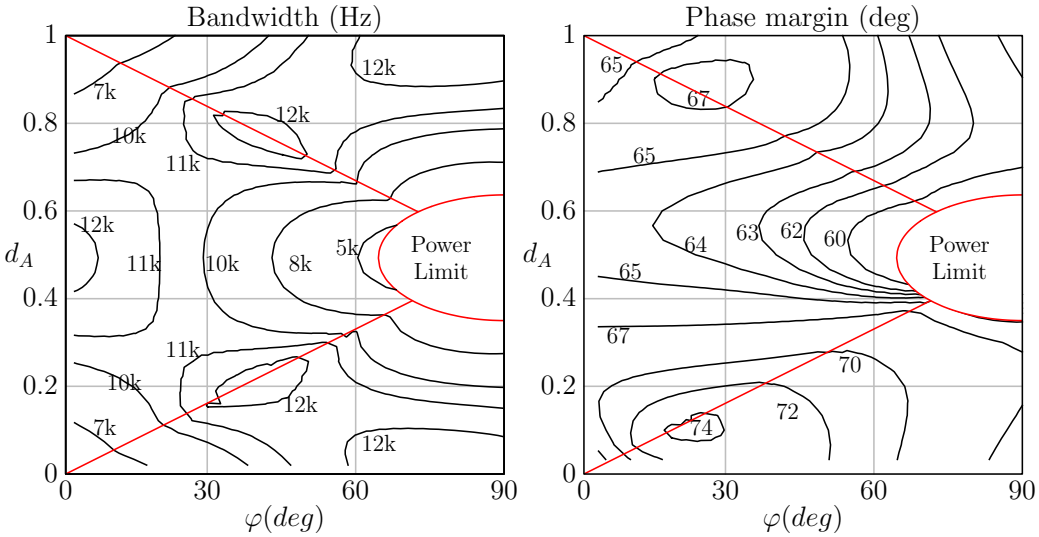


Figure 4.11: (a) Control bandwidth and (b) phase margin of the regulation loop on the control plane using the proposed dynamic map.

4.6 Experimental results

A more complete characterization of the prototype efficiency is illustrated in Fig 4.12a. Measurements, which cover the portion of the control plane in which the converter can operate, closely confirm the theoretical curves of Fig. 3.8b obtained by a Matlab Simulink based simulation where only the conduction losses are modeled. In the same figure, experimental trajectories of the control vector during the optimization process for a number of different power levels are also reported using the *Interacting control* described in the previous section. To obtain these trajectories, the optimization algorithm is initially disabled ($d_A = 0.5$), and the regulation loop enabled to keep the output voltage regulated by acting only on φ. As the optimization loop is enabled, duty-cycle d_A starts to decrease while the regulation loop keeps the control vector on the constant output power curve. Duty cycle d_A continues

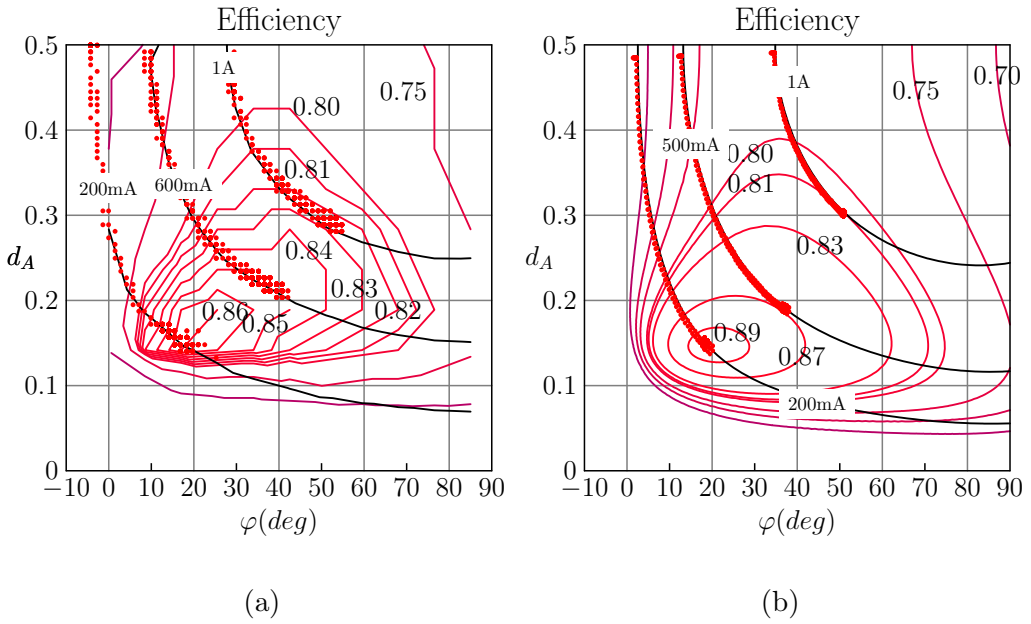
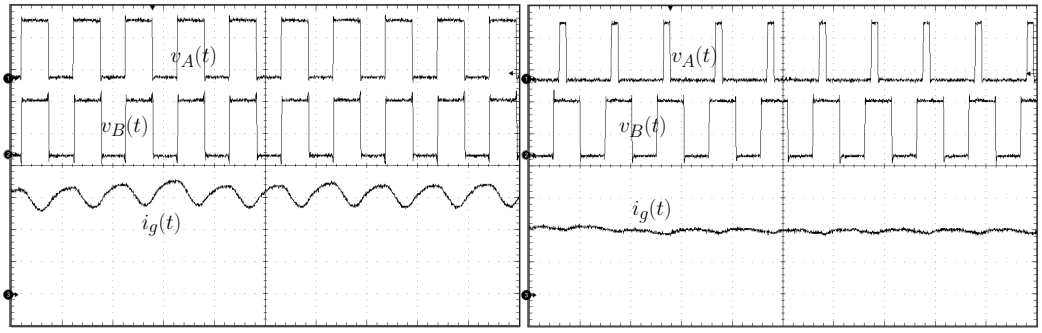


Figure 4.12: (a) Experimental and (b) theoretical efficiency contours on $\varphi - d_A$ plane along with (a) experimental and (b) simulated trajectories of the control vector during the efficiency optimization process for various power levels.

to decrease until the control point reaches the maximum efficiency point. The same test is made via Simulink simulation and results are reported in Fig. 4.12b. Oscilloscope screenshots of the control steady-state operation before and after the efficiency optimization step are respectively reported in Fig. 4.13a and Fig. 4.13b with a load current of 220mA. From the figures, it is evident the input current reduction from 180mA to 112mA.

Experimental closed-loop transient responses to a 220mA - 460mA and to a 220mA - 680mA step load are reported in Fig. 4.14 and 4.15. For each case the system was tested with the efficiency optimization loop disabled first, then enabled. Notice how the regulation dynamics is practically unaffected by the minimum input current tracking mechanism. At the same time, when the efficiency optimization loop is enabled, the input operating current is visibly

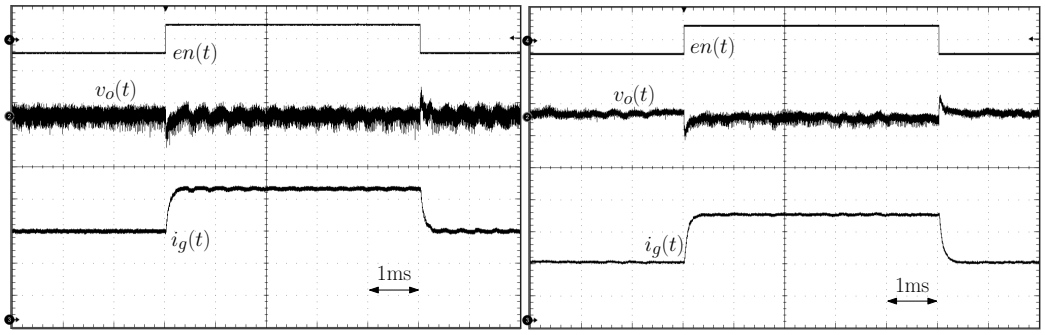


(a) (b)

Figure 4.13: Experimental steady-state operation (a) before and (b) after the efficiency optimization process. Input current i_g: 60mA/div; Switching node voltage A $v_A(t)$: 6V/div; Switching node voltage B $v_B(t)$: 3V/div; time scale: 5 µs/div.

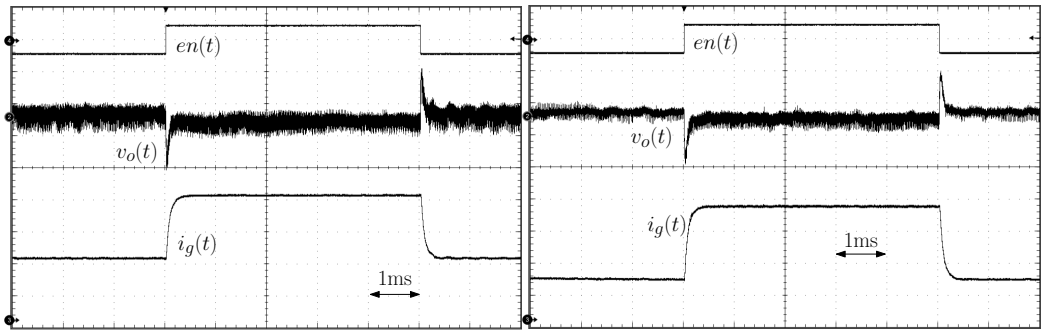
reduced.

Although the foregoing theoretical analysis has been developed neglecting switching losses, the experimental investigation discussed in this section confirms the effectiveness of the approach in achieving the maximum efficiency point. Efficiency improvement enabled by the proposed technique is reported in Fig. 4.16. Experimental prototype efficiency is reported as a function of the load current with and without the efficiency optimization loop enabled. When disabled, the efficiency optimization loop drives a constant $d_A = 0.5$. The proposed technique significantly improves the efficiency especially at low power levels and allows, in general, to operate the converter above 80% efficiency at all power levels.



(a) (b)

Figure 4.14: Experimental closed-loop response to a 220mA to 460mA step load (a) with efficiency optimization loop disabled and (b) enabled. Input current i_g: 70mA/div; output voltage v_o: 50mV/div; Load enable en: 20 V/div; time scale: 1 ms/div.



(a) (b)

Figure 4.15: Experimental closed-loop response to a 220mA to 680mA step load (a) with efficiency optimization loop disabled and (b) enabled. Input current i_g: 100mA/div; output voltage v_o: 50mV/div; Load enable en: 20 V/div; time scale: 1 ms/div.

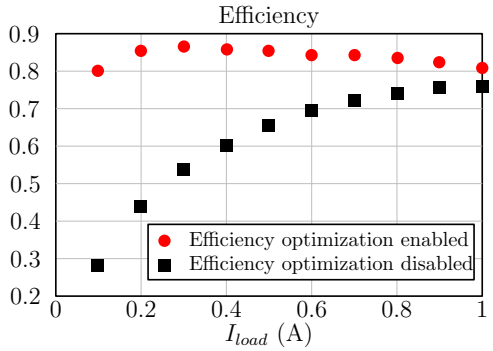


Figure 4.16: Experimental efficiency without and with the proposed efficiency optimization technique.

Table 4.1: Parameters of the 100MHz GaN based DHB-SRC Prototype

Switching frequency f_s	100 MHz
Input voltage V_g	20 V
Output voltage V_o	12.0 V
Maximum output current $I_{load,max}$	170 mA
Tank capacitance C	39 pF
Tank inductance L	82 nH
Output capacitance C_o	300 nF
Equivalent parasitic resistance R_{par}	2 Ω
Input current sensing resistance R_{sense}	1 Ω

4.7 100MHz GaN based case

In this section the case study of the dual DHB-SRC operating at up to 100 MHz switching frequency using GaN half-bridge stages with integrated gate drivers is presented. The results presented in this section are related to a six months visiting period at the *Colorado Power Electronics Center* (CoPEC).

In power electronics the GaN technology is an emerging applied science enabling high-efficiency switched-mode power conversion at very high switching frequencies, thus opening practical opportunities to reduce the size of passive components and to realize wide-bandwidth control loops. An experimental prototype is designed and developed to convert an input dc voltage of 20V to a 12V output at 100MHz switching frequency and up to 1.75W of output power. Examples of operating waveforms in the experimental 100 MHz DHB-SRC prototype are shown in Fig. 4.17, including both the inverter and the rectifier switching-node voltages, along with the inductor current $i(t)$, which

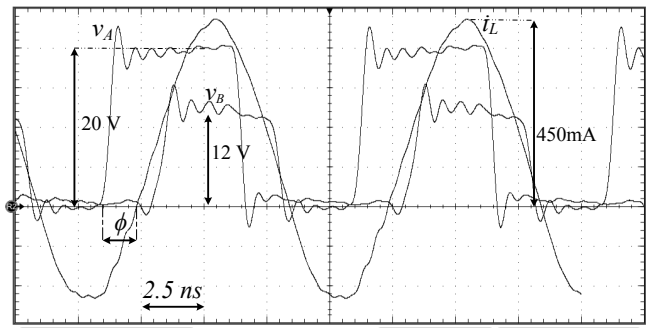
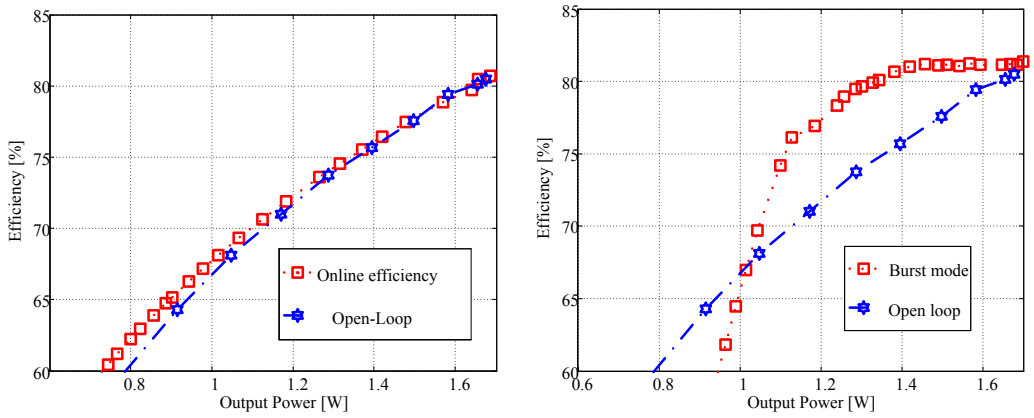


Figure 4.17: Experimental waveforms for the switching nodes and the inductor current. Switching nodes v_A, v_B: $5V$/div; Estimated tank current i_L: $95mA$/div; Time scale: $2.5ns$/div.

is obtained indirectly by shifting a signal proportional to the resonant-tank capacitor voltage measured using a differential voltage probe.

The efficiency optimization technique based on the interacting control described in section 4.3 is applied. As shown in Fig. 4.18a, in this specific case the efficiency obtained controlling the converter using the phase shift only, is very close to the optimal one. The main reason for such marginal efficiency improvement is to be traced to the relatively large on-resistance of the GaN switches – reported in Tab. 4.1 – which dominates conduction losses and strongly modifies the efficiency contours with respect to the one devised for the silicon-based DHB-SRC.

As an alternative solution studied during the visiting period at CoPEC, an on-off control also known as burst control is investigated. The burst control is an effective approach to maintain high efficiency over wide range of loads for high switching frequency converters. A conventional hysteretical voltage loop is used to turn the converter on or off. For this purpose, minimum and maximum thresholds of the output voltage are defined. Whenever the converter is on, it operates with the control values corresponding to the maximum efficiency, producing a burst that charges up the output filter capacitor. When



(a) (b)

Figure 4.18: Experimental efficiency plots comparing a) the converter with phase shift control and with the interacting control disclosed in section 4.3 b) the converter with phase shift control and burst control.

the output voltage exceeds a defined maximum threshold, all the switches are turned off. Turn-off instant is calculated in such way that in this instant the tank energy is entirely stored in the resonant capacitance. This way, the circulating current is zero during the off state. When the converter is off, the output capacitor is discharged by the load current till the output voltage reaches the lower threshold. Effectiveness of the solution is demonstrated by the efficiency plot of Fig. 4.18b.

Chapter 5

Non-resonant soft switching DAB

Contents

5.1 Introduction

In chapter 3 the steady state analysis of the DHB-SRC has been performed. The study emphasizes the presence of many degrees of freedom, which have been exploited in chapter 4 to perform an online efficiency optimization technique. As already explained, the choice of a resonant converter is motivated

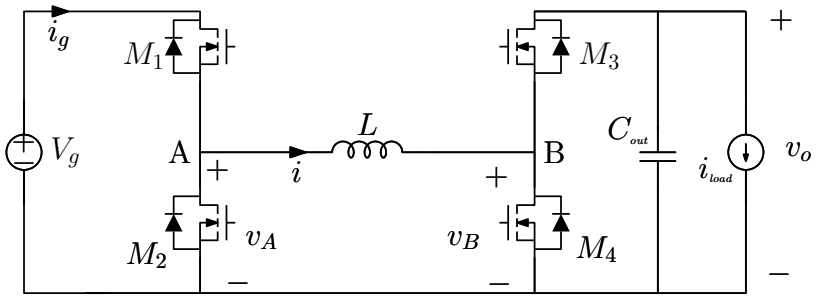


Figure 5.1: Schematic diagram of the non isolated Dual Active Bridge.

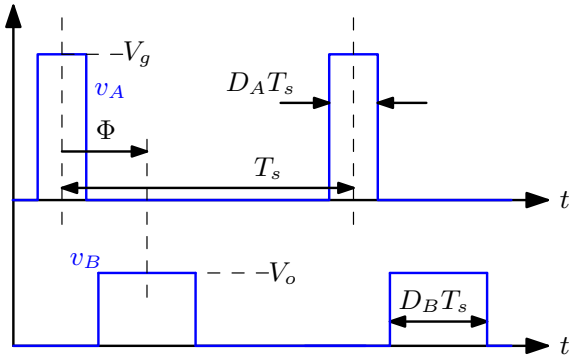


Figure 5.2: Non isolated Dual Active Bridge: voltage waveforms at nodes A and B.

by the fact that, if designed correctly, it enables the soft-switching which is a desirable feature for high frequency converters. However, the soft switching condition is not an exclusive feature of resonant converters but it can be achieved also by other topologies. For the case of the ZVS, what makes this property feasible to achieve, is the possibility to shape the inductor current in such way that, during the commutations, the current has the correct sign. Some examples of such converters are shown in [6, 21, 23, 24, 26, 28] and all belong to the class of Dual Active Bridge (DAB) converters. In this chapter the *non-isolated* half bridge version of the DAB shown in Fig. 5.1 is analyzed with particular focus on the converter efficiency. The most traditional way to control such converter is to drive the two bridges in a complementary

way (*Buck-Boost mode*) so that $D_B = 1 - D_A = D$. While minimizing the complexity of the controller, such solution creates an efficiency penalty represented by the doubled switching losses. The situation can be improved by acting on the input leg only in *Buck mode*, and on the output leg only in *Boost mode*. In this case, however, a control strategy is normally required to ease the transition between the two operating modes [36].

5.2 Steady state analysis of the DAB

Main voltages waveforms of the DAB converter of Fig. 5.1 are shown in Fig. 5.2. Assuming all the components are ideal, the conversion ratio M of the DAB can be calculated by imposing that the average voltage across the inductor is zero,

$$M = \frac{V_o}{V_g} = \frac{D_A}{D_B}. \tag{5.1}$$

Contrary to the case of the resonant converter presented in chapter 3, the DAB of Fig. 5.1 behaves as a ideal voltage generator, meaning that there is no load dependence on the output voltage expression

$$V_o = V_g \frac{D_A}{D_B}. \tag{5.2}$$

It worth to notice also that the conversion ratio M does not depend on the phase shift Φ. However, if a small inductor is chosen, the current ripple is high and so the phase shift becomes an additional degree of freedom that can be used to shape the waveform $i(t)$ for purpose of efficiency optimization. For instance, [6] proposes a modulation scheme which allows to obtain a current waveform like the one sketched in Fig. 5.3. Such technique exploits the degrees of freedom of the topology, combined with an appropriate choice of

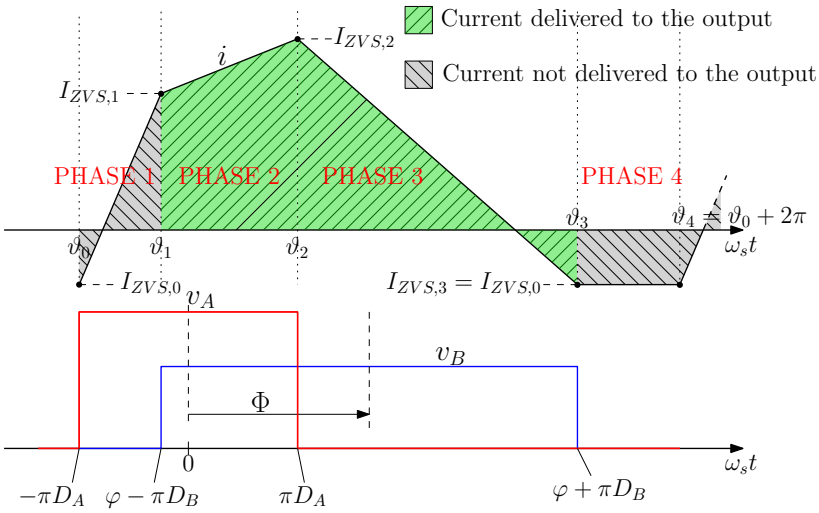


Figure 5.3: Example of modulation strategy employing the phase shift modulation to shape the inductor current [6].

the inductance, to achieve ZVS operation for a desired range of the operating conditions. Such modulation scheme requires the current to change sign during the switching period, leading to an inductance value much smaller than what normally required in more traditional designs. At the instants ϑ_0, ϑ_1, ϑ_2 and ϑ_3 the ZVS condition - complete or partial, depending on the current value - is met. Phase 4 is introduced to limit the inductor current when the power is not delivered to the load reducing the conduction losses. Observe that the ZVS condition that requires currents $I_{ZVS,i}$ to be large enough tends to simultaneously increase conduction losses. Therefore, in general a trade-off exists and can be obtained by modulating instants ϑ_1, ϑ_2 and ϑ_3, or equivalently, duty cycles D_A, D_B and phase shift Φ. The current waveform of Fig. 5.3, can be achieved with the mosfet sequence of Tab. 5.1 which is obtained under the following condition:

$$\begin{cases} -\pi D_A < \varphi - \pi D_B < \pi D_A \\ \pi D_A < \varphi + \pi D_B < 2\pi - \pi D_A \end{cases} \tag{5.3}$$

Table 5.1: Switching sequence related to the waveform of Fig. 5.3.

phase	M_1	M_2	M_3	M_4
1	on	off	off	on
2	on	off	on	off
3	off	on	on	off
4	off	on	off	on

Inequalities (5.3), individuate a region on the control space. Similarly, the control space can be divided in m regions, each one related to a different switching sequence. For instance, when the converter operates in step-down mode, the control space can be divided in five regions. Such regions are illustrated in Fig. 5.4a for the conversion ratio $M = 5/12$.
Each of these regions has different characteristics in terms of efficiency. For instance, the region (1) is the one which allow to obtain the waveform of Fig. 5.3.

5.3 Efficiency characterization

In this section the efficiency characterization of the DAB is presented. Since not all the regions composing the plane are characterized by ZVS, both conduction and switching losses are considered. For reasons of clarity let us consider the dual active bridge with parameters listed in Tab. 5.2 designed for a maximum output current of about 1.5A. As for the switches, Infineon OptiMOS®3 power MOSFET of the type IPD036N04L G are considered. Because of the frequency dependence of the inductor ESR, two values are used for the parasitic resistance. The DC parasitic resistance $R_{par,dc}$ is used to calculate the conduction losses associated with the average inductor current

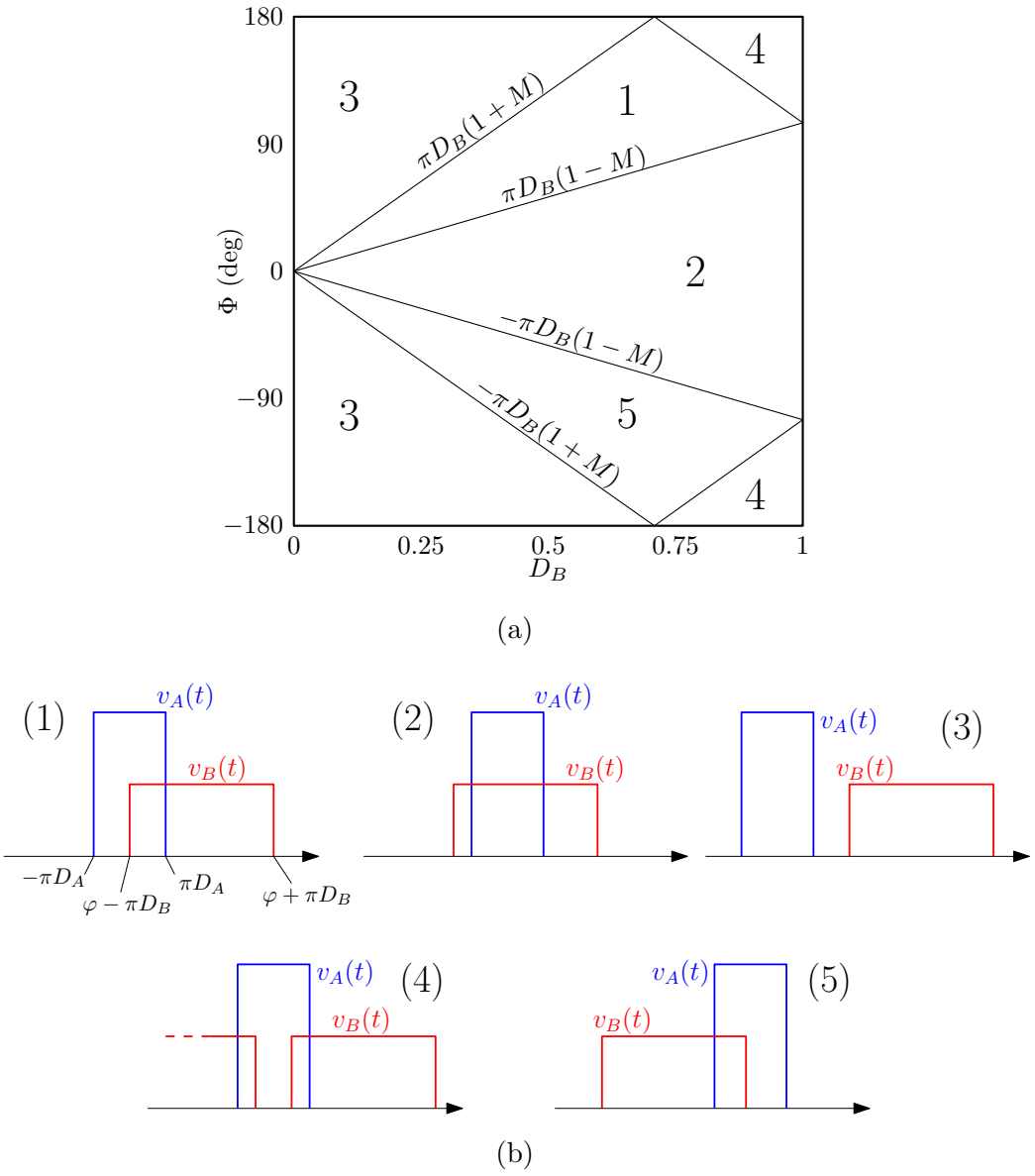


Figure 5.4: Regions of the control space (a) and associated switching node waveforms (b).

while $R_{par,ac}$ is used to calculate the conduction losses caused by the current ripple. In both cases, such parameters account for the dissipative effects of the mosfets and the inductor. In $R_{par,dc}$ the DC resistance of the inductor is included while in $R_{par,ac}$ the equivalent resistance at the switching frequency

Table 5.2: DAB specifications.

Switching frequency f_s	200 kHz
Input voltage V_g	12 V
Output voltage V_o	5 V
Inductor L	2 μHz
DC Equivalent parasitic resistance $R_{par,dc}$	6 mΩ
AC equivalent parasitic resistance $R_{par,ac}$	0.15 Ω

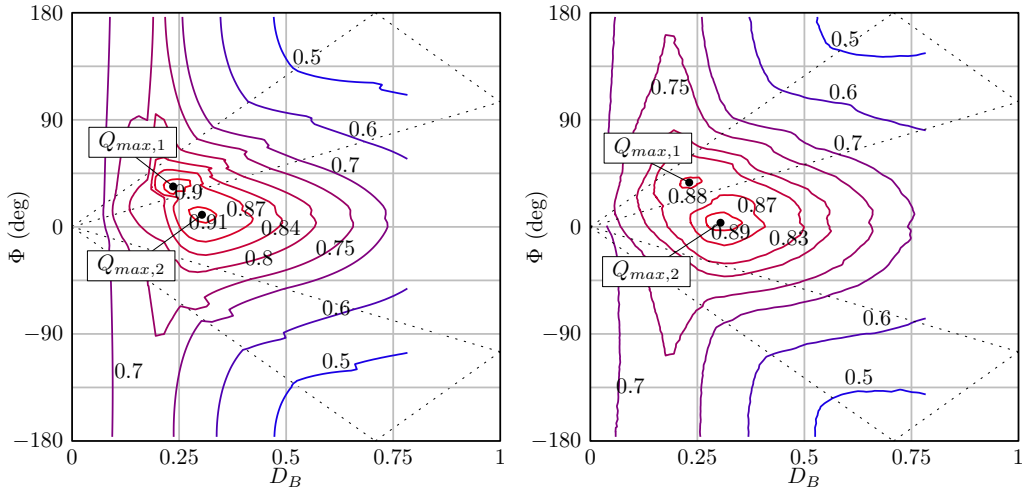
is used. If $I_{ac,RMS}$ is the RMS of the current ripple and I_{avg} is the average value of the inductor current, conduction power losses are calculated as follows

$$P_{cond} = R_{par,dc} I_{avg}^2 + R_{par,ac} I_{ac,RMS}^2. \tag{5.4}$$

For the switching losses contribution, power losses are calculated for each operating point depending on the nature of the commutation (hard-switching, full soft-switching or partial soft-switching) as explained in chapter 2.

5.3.1 Validation of the power losses model

The calculated efficiency is plotted in Fig. 5.5a on the $D_B - \Phi$ plane for the case of 200mA load. The dead time is chosen constant and equal to $t_{\text{dead}} = 100\text{ns}$. Notice that, since the output voltage is constant over the plane of Fig. 5.5a, the duty cycle D_A is a function of D_B through the relation (5.1). In order to validate the losses model the same characterization is also made via experiment on a prototype with specifications listed in Tab. 5.2. The characterization setup is composed by the power stage, a control stage and a NI LabVIEW based system. The control stage is composed by an output voltage sensing board and a FPGA board in which regulator and Combined Phase-



(a) (b)

Figure 5.5: Efficiency of the DAB converter on the control space: (a) calculated, (b) experimental.

Shift and Pulse Width Modulators (CPSPWM) are implemented. During the characterization the LABView system spans the control space imposing the operating point (Φ, D_B) and measures the converter input and output power while the control stage keeps the output voltage regulation acting on D_A. The result of the characterization is plotted in Fig. 5.5b. The good matching between Fig. 5.5a and Fig. 5.5b confirms the accuracy of the model.

As can be seen by the figure, in which the regions defined in Fig. 5.4a are highlighted, regions 1 and 2 are those characterized by high efficiency. In each of these two regions a maximum efficiency point exists ($Q_{max,1}$ and $Q_{max,1}$ in Fig. 5.5a). The region 1 is associated with the switching sequence of Tab. 5.1 and described in [6]. In region 2 the current shape is the one sketched in Fig. 5.6. Contrary to the case of the waveform of Fig. 5.3, in this case there is one hard switching commutation at the falling edge of $v_B(t)$. Based on the power losses model explained above, such hard switching commutation causes

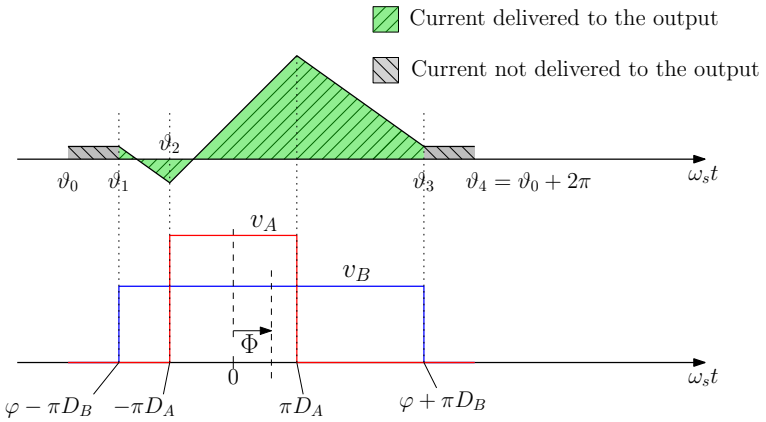


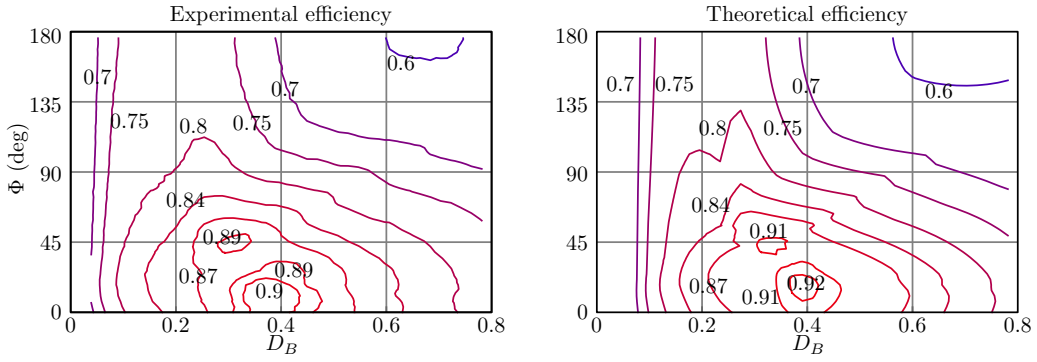
Figure 5.6: Current waveform in the region 2 of Fig. 5.4a.

a 1% efficiency penalty in the point Q_{max_2} with respect to the point Q_{max_1} but there is a gain of almost 3% of efficiency because of reduced conduction losses.

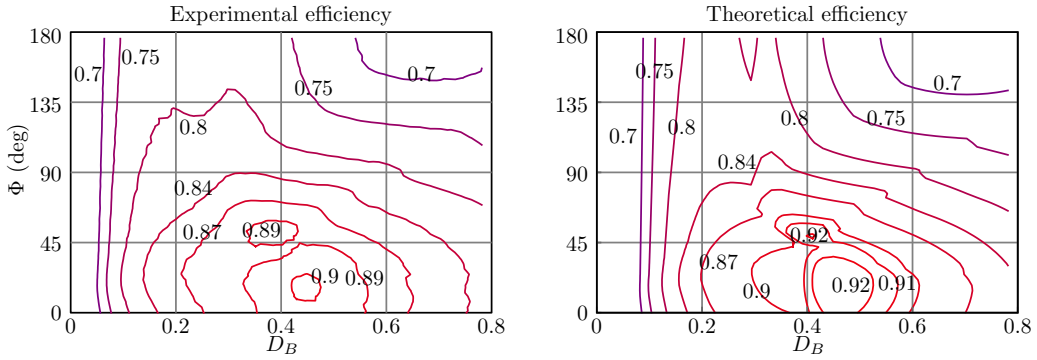
To conclude, one may argue that the total efficiency is comparable with most traditional buck-boost converters with the same power rate. It worth to notice that the value of the inductance is 2µH, which is rather small for a 200kHz converter with this power rate. As a comparison, if the converter is controlled driving the two bridges in a complementary way, to keep the current ripple around 30% of the maximum average inductor current current, an inductance value of about 40µH may be chosen, twenty times higher. In this case, a high value of the inductor is mandatory to reduce the current ripple and consequent conduction losses. Indeed, using the traditional buck-boost modulation scheme is equivalent to constrain the conditions

$$\begin{cases} D_B = 1 - D_A \\ \Phi = 180° \end{cases}. \tag{5.5}$$

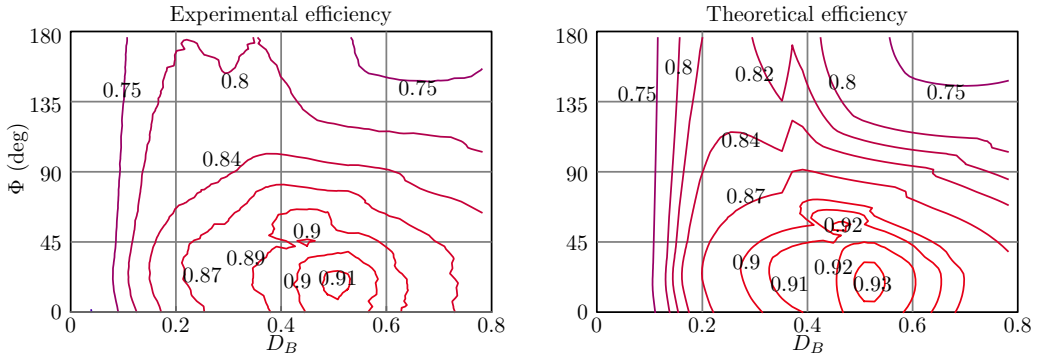
By (5.1) we have $D_B \approx 0.63$ and $D_A \approx 0.27$. For the converter with specifications listed in Tab. 5.2, in this case the efficiency is lower than 70% as can be seen in Fig. 5.5 at coordinates (Φ,D_B)=(180,0.63). In order to further validate the model the calculated and measured efficiency is plotted for several values of the load in Fig. 5.7. As can be seen by the figure, the presence of two maximum efficiency points, one in the region 1 and the other in the region 2, is confirmed for a wide range of the load.



(a)



(b)



(c)

Figure 5.7: Experimental and calculated efficiency of the DAB converter on the control space: (a) load: 400mA, (b) load: 600mA, (c) load: 800mA.

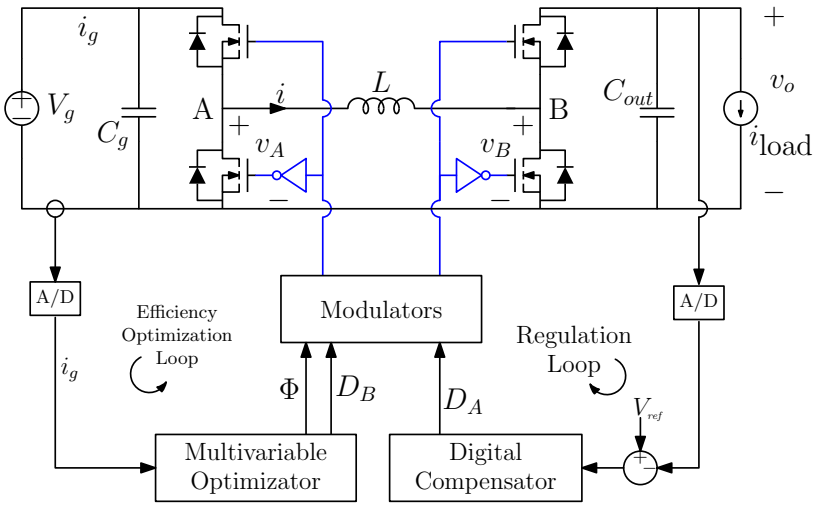


Figure 5.8: Control scheme of the DAB converter.

5.4 Online efficiency optimization

The steady state analysis of section 5.2 shows that, on first approximation, the conversion ratio M depends on D_A and D_B and is independent of the phase shift Φ. However, as seen in section 5.3, the converter efficiency is deeply affected by Φ so this degree of freedom should be used in the optimization process. Furthermore, the efficiency strongly depends on the duty cycle D_B too, therefore the DAB converter requires a multi-variable optimization. In this section an online efficiency optimization technique based on the simplex method is tested. The general control scheme is sketched in Fig. 5.8. The control system is composed by a fast regulation loop controlling the output voltage and a slower efficiency optimization loop. The regulation loop controls the output voltage v_o acting on the duty-cycle D_A. The optimization loop periodically senses the average input current and updates D_B and Φ in order to optimize the system efficiency. The efficiency optimization algorithm is based on the simplex algorithm disclosed in [37] and used in [38] to develop a two-dimensional maximum power point tracking in a photovoltaic system.

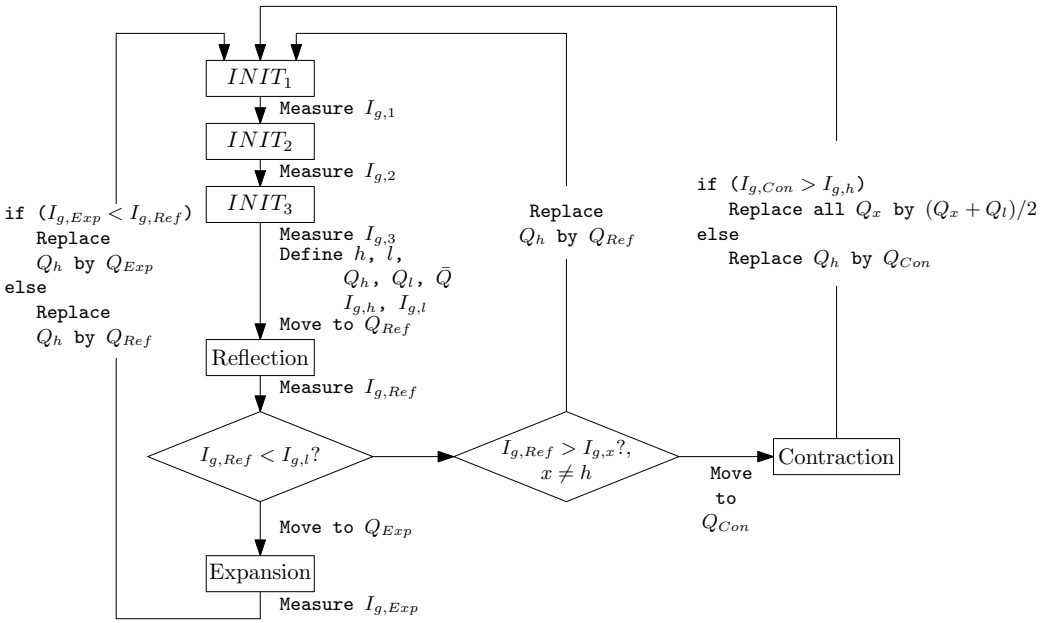


Figure 5.9: Flowchart of the optimization finite state machine.

As seen in section 5.3.1, for the converter under analysis, two maximum efficiency points exist. Even though this fact cannot guarantee the absolute maximum efficiency point is always reached, one can observe that the efficiency difference between the maximum efficiency point in region 1 of Fig. 5.4a and the one in region 2 is about 1% (see Fig. 5.5 and Fig. 5.7). For this reason, both points are accepted as result of the optimization process. In those systems in which the difference between different maximum efficiency points is relevant, the algorithm may be modified in order to constrain the converter to operate in the best efficiency region.

5.4.1 Algorithm description

The algorithm requires the definition of $n + 1$ operating points where n is the number of variables used to perform the optimization. Since the optimization space is the one defined by Φ and D_B in this case $n = 2$. The three operating

points individuate a triangle that is a *two*-dimensional simplex. The algorithm is implemented by means of a *Finite-State Machine* (FSM) with the flowchart depicted in Fig. 5.9. The FSM is clocked by a clock $clk(t)$ of period T_{FSM} which is long enough to assume that the converter is in steady state at the end of each FSM clock period. During each period (e.g. FSM state) the converter operating point (D_B,Φ) is constant. At the end of each period, before moving to a new FSM state, the average input current is sampled and associated with the operating point. Then, the FSM moves from the present state to the next state depending on the present state and the measured current. The FSM has six states, the first three $INIT_1$, $INIT_2$, $INIT_3$ are associated with the three operating points $Q_1 = (\Phi_1, D_{B1})$, $Q_2 = (\Phi_2, D_{B2})$ and $Q_3 = (\Phi_3, D_{B3})$ forming the vertexes of the initial simplex. At the end of states $INIT_x$, the associated average input current $I_{g,x}$ is memorized. At the end of state $INIT_3$ the following parameters are calculated,

h is the reference to the simplex vertex associated with the highest average input current.

l is the reference to the simplex vertex associated with the lowest average input current.

Q_h is the simplex vertex with the highest average input current.

Q_l is the simplex vertex with the highest average input current.

$I_{g,h}$ is the highest average input current.

$I_{g,l}$ is the lowest average input current.

$\bar{Q}$ is the centroid of the points Q_x with suffix $x \neq h$.

The other three states *Reflection*, *Expansion* and *Contraction* are reached after the namesake operations listed below.

Reflection this operation is executed after the state $INIT_3$ to generate the new operating point

$$Q_{Ref} = (1 + \alpha)\bar{Q} - \alpha Q_h, \tag{5.6}$$

where α is a positive constant, the *reflection coefficient*. After this operation, the FSM moves from the state $INIT_3$ to the namesake state *Reflection*. Once again, the converter stays in this state for a time T_{FSM}. At the end of this state, the average input current $I_{g,Ref}$ is sampled.
If $I_{g,Ref} \leq I_{g,l}$ the *Expansion* operation is performed and the namesake state is set as *next state*.
If $I_{g,Ref} > I_{g,l}$ and $I_{g,Ref} > I_{g,x}$ the *Contraction* operation is performed and the namesake state is set as *next state*.
Otherwise, Q_h is replaced by Q_{Ref} and the $INIT_1$ is set as *next state*.

Expansion This operation is performed at the end of the *Reflection* state if $I_{g,Ref} \leq I_{g,l}$. The operation is

$$Q_{Exp} = \gamma Q_{Ref} + (1 - \gamma)\bar{Q} \tag{5.7}$$

where $\gamma > 1$ is the *expansion constant*. Then, the FSM moves from the *Reflection* to the *Expansion* state. After a time T_{FSM}, the average input current $I_{g,Exp}$ is sampled. The *next state* is $INIT_1$. Before moving to the new state, Q_h is replaced by Q_{Exp} if $I_{g,Exp} < I_{g,Ref}$, Q_{Ref} otherwise.

Contraction This operation is performed passing from the *Reflection state*

to the *Contraction state*. The associated operating point is

$$Q_{Con} = \beta Q^* + (1 - \beta)\bar{Q} \tag{5.8}$$

where $0 < \beta < 1$ is the *contraction coefficient* and Q^* is equal to Q_h if $I_{g,h} < I_{g,Ref}$, Q_{Ref} otherwise. Once again, after a time interval T_{FSM}, the average input current $I_{g,Con}$ is sampled and the state $INIT_3$ is set as *next state*.

Before moving from the *Contraction state* to $INIT_3$ state, if $I_{g,Con} < I_{g,h}$, Q_h is replaced by Q_{Con}. Otherwise, all Q_x's are replaced by $(Q_x + Q_l)/2$.

5.4.2 Implementation and experimental validation

In order to test the algorithm explained above, a prototype of the system of Fig. 5.8 is developed. Specifications of the power stage are listed in Tab. 5.2. As for the converter switching devices, Infineon OptiMOS® 3 power MOSFET of the type IPD036N04L G is employed, having $r_{ds,on} \approx 3.6\Omega$ and rated 40 V, 90 A. For fast prototyping both regulator and optimization block have been implemented on a Cyclone-II FPGA development board. The resolution of duty cycle and phase shift command signals are about 0.4% and 1.4° respectively. For the sensing resistance used to measure the input current a value of 0.2Ω is chosen. The output voltage loop gain $T(s)$ is compensated by means of a PID regulator designed for a bandwidth $f_{bw} > 4$kHz and a

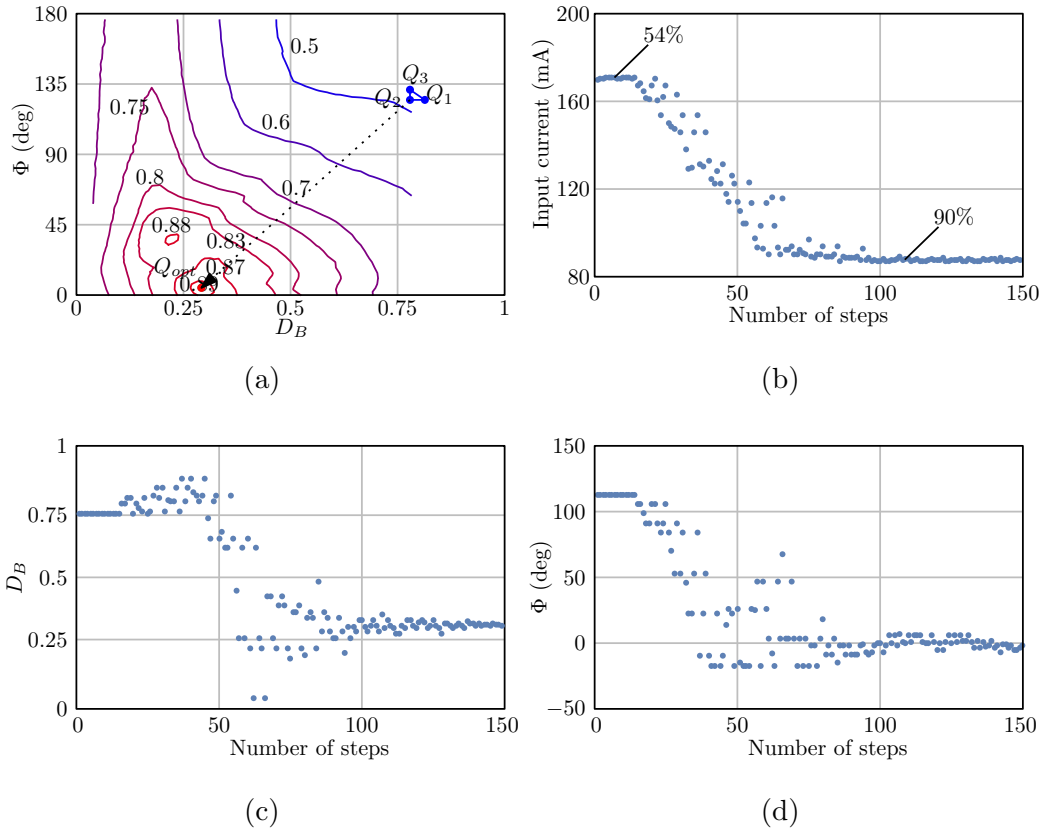


Figure 5.10: Main system signals acquired during the efficiency optimization: (a) Initial simplex and final point on the optimization space; (b) Average input current acquired by the ADC during the optimization; (c) Duty cycle D_B during the optimization; (d) Phase shift Φ during the optimization.

phase margin PM$>45°$. Parameters α, β, γ of the FSM are chosen be

$$\begin{cases} \alpha = 1 \\ \beta = 0.5 \\ \gamma = 2 \end{cases} . \tag{5.9}$$

This choice minimizes the computational complexity allowing to implement the products simply by using shift registers. In order to test the effectiveness of the approach the converter is made operate in a low efficiency point with

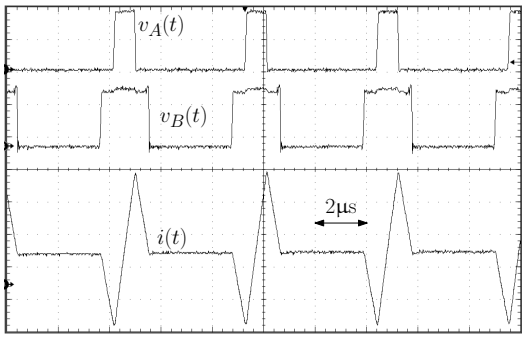


Figure 5.11: Experimental steady-state operation after the optimization. Inductor current i: 600mA/div; Switching node voltage $v_A(t)$: 6V/div; Switching node voltage $v_B(t)$: 3V/div; time scale: 2µs/div.

the optimization loop disabled. The initial simplex vertexes are

$$\begin{cases} Q_1 = (112°, 0.74) \\ Q_2 = (105°, 0.74) \\ Q_3 = (105°, 0.78) \end{cases} \tag{5.10}$$

and shown on the $D_B - \Phi$ plane in Fig. 5.10a. Once the optimization loop is enabled, Φ and D_B are updated on a FSM clock cycle basis with period T_{FSM}. The input current acquired by the ADC is plotted in Fig. 5.10b while the evolution of D_B and Φ during the optimization are plotted in Fig. 5.10c and 5.10d respectively. In this experiment, the optimization loop converges to the relative maximum point with efficiency around 90% after about 50 FSM clock cycles. Oscilloscope screenshot showing the switching node and the inductor current waveforms are shown in Fig. 5.11.

In general, since two maximum efficiency points exist for a given load value, it is not possible to guarantee the system to converge in the absolute maximum efficiency point. It may be possible only limiting the converter working in a specific region, but it requires a preliminary converter characterization. The trajectory of the simplex during the optimization depends on the initial

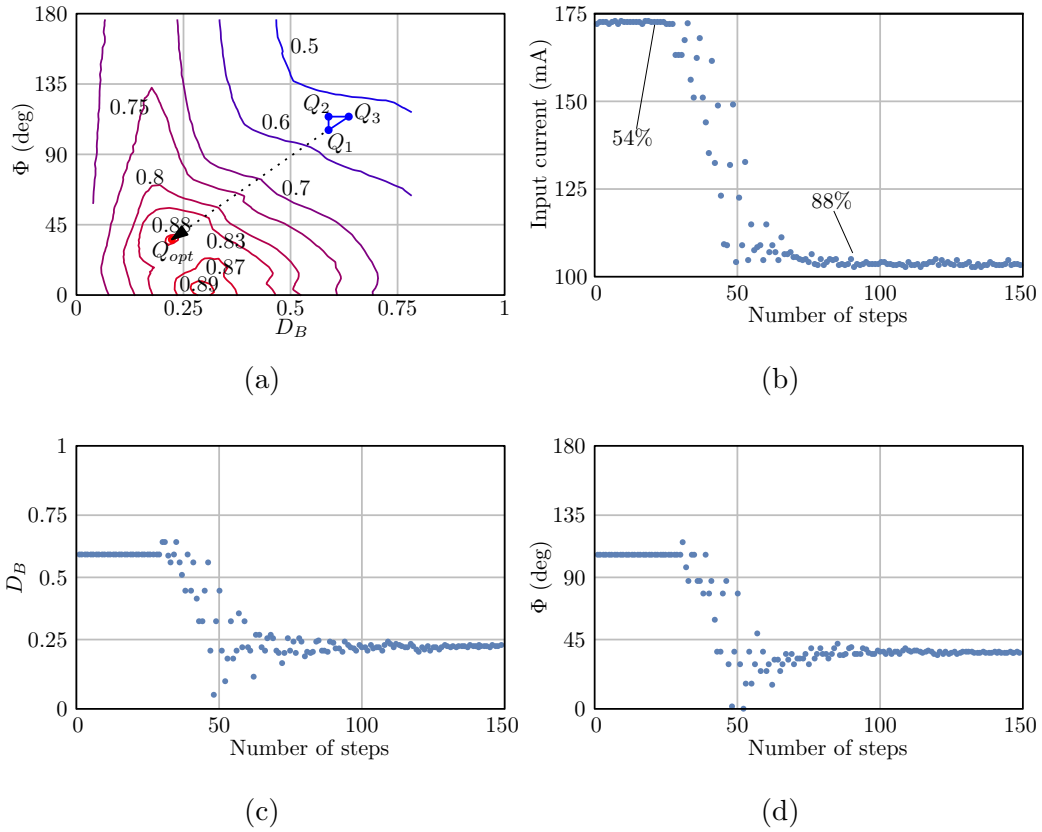


Figure 5.12: Main system signals acquired during the efficiency optimization: (a) Initial simplex and final point on the optimization space; (b) Average input current acquired by the ADC during the optimization; (c) Duty cycle D_B during the optimization; (d) Phase shift Φ during the optimization.

position. For instance consider the case in which the initial simplex vertexes are

$$\begin{cases} Q_1 = (105°, 0.58) \\ Q_2 = (105°, 0.63) \\ Q_3 = (114°, 0.63) \end{cases}. \tag{5.11}$$

As shown in Fig. 5.12, in this case the optimization loop finds the relative maximum efficiency point with efficiency of about 88%. Fig. 5.11 shows the steady-state switching node and inductor current in the optimal efficiency point.

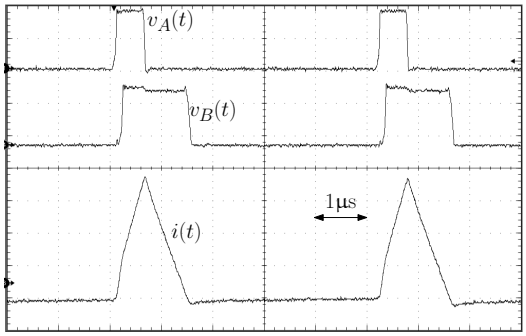


Figure 5.13: Experimental steady-state operation after the optimization. Inductor current i: 600mA/div; Switching node voltage $v_A(t)$: 6V/div; Switching node voltage $v_B(t)$: 3V/div; time scale: 1µs/div.

Part II

Dynamic Study of Digitally Controlled Dual Active Bridge Converters

Chapter 6

Introduction to the dynamic analysis of resonant converters

Contents

6.1 System under study

This section discusses the problem of the dynamic study of a dual active bridge converter when regulated by means of a digital multivariable control with the architecture described in Fig. 1.7. In such a system, the regulation loop bandwidth is designed to be much larger than the optimization loop one, so that the *interaction* between the two loops can be neglected in the

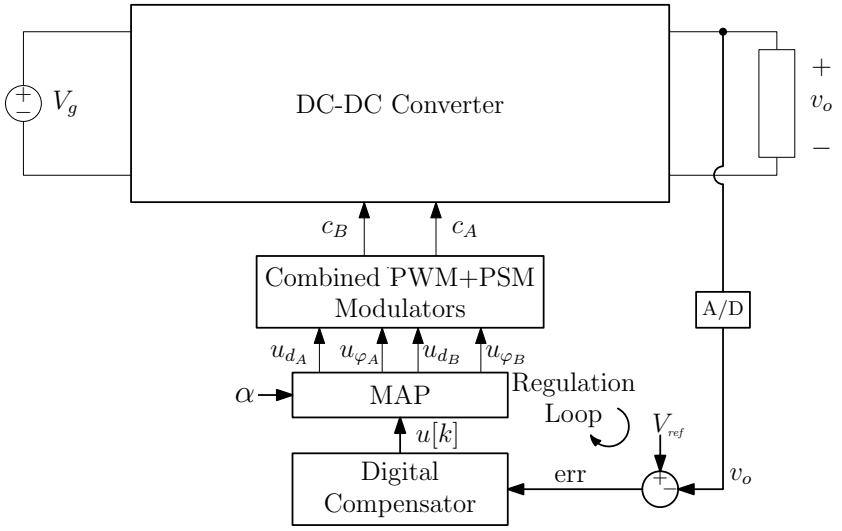


Figure 6.1: General regulation scheme.

stability analysis. Nonetheless, as the optimization process proceeds, the converter operating point slowly spans large portions of the control plane. For such reason, the assessment of the stability of the system cannot be limited to one specific condition, but a general analysis must be developed for an arbitrary operating point. The approximation therefore consists in assuming that the converter operating point changes in a *quasi-stationary* fashion during the efficiency optimization, so that it can be treated as a parameter of the dynamical analysis.

The general scheme of the system under study is exemplified in Fig. 6.1 where, according to the previous consideration, the optimization loop is removed and only the regulation loop is shown. As can be seen in the figure, the output voltage regulation is performed through a feedback control. The output voltage is acquired using an *Analog to Digital Converter* (ADC) and compared with a voltage reference V_{ref}. The voltage error is then processed by a digital regulator which returns a discrete time control signal $u[k]$ updated on a switching cycle basis. The map block translates signal $u[k]$ into the

modulating signals. Parameter α is generated by the optimization block to bring the converter in an efficient operating point and it is considered a parameter of the problem. Control inputs of the dual active bridge, whether resonant or non-resonant version, are duty cycle references u_{d_x} and phase references u_{φ_x} where $x \in \{A, B\}$. Signals u_{φ_x} and u_{d_x} are inputs of digital modulators which produce modulated signals $c_x(t)$ driving the converter. In order to asses the stability of the system one has to describe the dynamics of main blocks composing the loop that are regulator, modulators and the power stage.

The regulator is the block designed to guarantee the stability and dynamic performance of the system and it typically relies on a standard PI or PID controller. In order to perform the design of this block the small-signal analysis of all the other blocks composing the feedback system is required.

This part is organized as follows: in this chapter an overview of dynamic phasors and modeling of phase-shift controlled DHB converters is presented. Chapters 7 and 8 treat the problem of characterization of additional dynamics introduced in the regulation loop by uniformly sampled *phase shift* and *combined phase shift and pulse width* modulators. Chapter 9 addresses the problem of small-signal modeling of a DHB-SRC with a multi-variable digital control using a general multi-harmonic approach.

6.2 Review of dynamic phasor modeling

AC analysis of switching converters is well established in literature and is formulated within the framework of the so called *averaged modeling* [39,40]. The key of this theory is the averaging of the converter waveforms over a switching period to remove switching harmonics. Expressions of state variables as well

as control inputs are eventually linearized to perform the small-signal analysis. The approximations commonly involved in this theory are *small-ripple* approximation and the hypothesis of *linear-ripple* approximation of currents and voltages over the time.

The theory is extended to the case of soft-switching topologies and AC-DC converters (in which previous hypothesis are not verified) with the theory of *generalized averaging*, introduced in [41]. This theory shows how dynamic analysis of a converter can be accomplished through an appropriate averaging operation around the converter switching frequency. When generalized averaging is further specialized and only the spectral sidebands immediately close to the carrier frequency are retained, the phasor transform [42] is obtained. *Dynamic phasors* represent an extension of the fundamental approximation approach [14] to the dynamical case, and have been employed to study the small-signal behavior of electronic ballasts [43, 44] and further generalized in [45] to a dual-bridge series resonant dcdc converter subject to multi-angle modulation.

To define a dynamic phasor consider a generic amplitude and phase modulated signal

$$s(t) = a(t)\cos\left(\omega_s t - \varphi(t)\right). \tag{6.1}$$

When amplitude $a(t)$ and phase $\varphi(t)$ of $s(t)$ are constants, ($a(t) = A$ and $\varphi = \Phi$), signal $s(t)$ represents the steady state fundamental harmonic of any voltage or current waveform of the circuit. If, more generally, the instantaneous phase shift $\varphi(t)$ as well as the instantaneous amplitude $a(t)$ contain a DC term plus a small sinusoidal modulation component

$$\begin{cases} a(t) = A + \hat{a}(t) \\ \varphi(t) = \Phi + \hat{\varphi}(t) \end{cases} \tag{6.2}$$

with $|\hat{a}| \ll 1$, and $|\hat{\varphi}| \ll A$ oscillating at some angular frequency ω_m, such modulation frequency creates two sidebands in $s(t)$, located at $\omega_s \pm \omega_m$ [46]. These sidebands are the primary drivers of the converter small-signal dynamics. The concept of dynamic phasor is motivated by the need to extend the fundamental harmonic approximation into a more general narrowband approximation valid for amplitude and phase modulated signals. Within this approximation, only the components of $s(t)$ at ω_s, $\omega_s + \omega_m$ and $\omega_s - \omega_m$ are considered. According to the foregoing introduction, signal $s(t)$ can be written as

$$s(t) = \frac{1}{2}a(t)e^{j(\omega_s t - \varphi(t))} + \frac{1}{2}a(t)e^{-j(\omega_s t - \varphi(t))} \tag{6.3}$$

Modulation theory [46] shows that the assumption of small variations of $\varphi(t)$ and $a(t)$ is sufficient to realize the narrowband condition introduced above, and approximate the spectrum of $s(t)$ by three spectral lines only, one carrier frequency ω_s, plus two sidebands at $\omega_s \pm \omega_m$. Complex signal

$$\vec{\boldsymbol{s}}(t) = a(t)e^{-j\varphi(t)} \tag{6.4}$$

is defined as the *dynamic phasor* associated with the signal $s(t)$. This amounts to the following operations on the original real signal $s(t)$ (see Fig. 6.2):

i) The negative-frequency part of the signals spectrum is suppressed, and the positive-frequency portion of the spectrum is multiplied by 2. In modulation theory, the resulting complex time-domain signal $z_s(t)$ is commonly referred to as *analytic signal*. Observe that, due to the Hermitian symmetry of a real signals spectrum, suppressing the negative frequencies is a lossless operation from an information theory standpoint.

ii) Frequency origin is shifted to $\omega = \omega_s$. In the time domain, this amounts

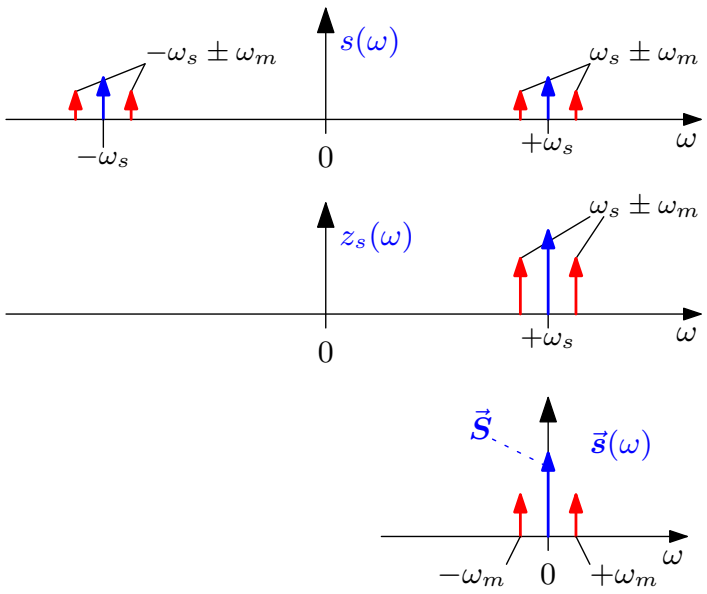


Figure 6.2: Definition of dynamic phasor: (top) spectrum of a phase-modulated signal $s(t)$, (middle) spectrum of the analytic signal $z_s(t)$ and (bottom) spectrum of the dynamic phasor $\vec{\boldsymbol{s}}(t)$.

to multiplying the analytic signal by the complex exponential carrier $\exp(j\omega_s t)$.

To go back from the dynamic phasor to the original signal, one computes

$$s(t) = \Re\left[\vec{\boldsymbol{s}}(t)e^{j\omega_s t}\right] \tag{6.5}$$

Given the small amplitude of $\hat{a}(t)$ and $\hat{\varphi}(t)$, the dynamic phasor of $s(t)$ has the following first-order approximation,

$$\begin{aligned} \vec{\boldsymbol{s}}(t) &= a(t)e^{-j\varphi(t)} \\ &\approx \vec{\boldsymbol{S}}\left(1 + \frac{1}{A}\hat{a}(t) - j\hat{\varphi}(t)\right) \end{aligned} \tag{6.6}$$

with $\vec{\boldsymbol{S}} = Ae^{-j\Phi}$ DC component of the signals dynamic phasor. In the small-signal approximation, amplitude modulation is seen as a vector component

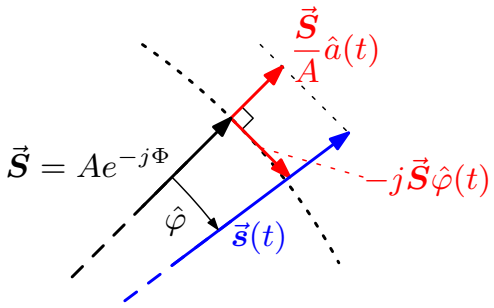


Figure 6.3: Small-signal components of a signals dynamic phasor with amplitude and phase modulation.

in phase with $\vec{S}$ and phase modulation appears as a vector component *in quadrature* with respect to $\vec{S}$. Observe that, in the above equations, $\hat{\varphi}$ represents the instantaneous small-signal phase lag of $\vec{s}(t)$ with respect to $\vec{S}$ and $\hat{a}$ represents the instantaneous small-signal amplitude variation of $\vec{S}$. A geometrical representation of such general small-signal decomposition is shown in Fig. 6.3.

6.3 Modeling of the power stage

AC voltages and currents of a resonant converter responding to frequency, duty cycle or phase control commands can be conveniently represented as dynamic phasors. It has been shown [42–45] how the phasor transformation (6.5) leads to equivalent small-signal circuits which can be used to systematically derive, either analytically or numerically, all the transfer functions of interest for controller design. Phasor equivalent circuits make use of a combination of inductances, capacitances and complex resistances in order to describe the mathematical relationships between voltage and current phasors in the

resonant tank [42]. For instance, consider the ideal inductor equation

$$v(t) = L\frac{di(t)}{dt} \tag{6.7}$$

where $v(t)$ and $i(t)$ are related to their dynamic phasor by (6.5),

$$\begin{cases} i(t) = \Re\left[\vec{\boldsymbol{i}}e^{j\omega_s t}\right] \\ v(t) = \Re[\vec{\boldsymbol{v}}e^{j\omega_s t}] \end{cases}. \tag{6.8}$$

By substitution of (6.8) in (6.7) we obtain the relation

$$L\frac{d}{dt}\Re\left[\vec{\boldsymbol{i}}(t)e^{j\omega_s t}\right] = \Re\left[\vec{\boldsymbol{v}}(t)e^{j\omega_s t}\right], \tag{6.9}$$

that can be expanded as

$$\Re\left[L\frac{d\vec{\boldsymbol{i}}(t)}{dt}e^{j\omega_s t} + j\omega_s L\vec{\boldsymbol{i}}(t)e^{j\omega_s t}\right] = \Re\left[\vec{\boldsymbol{v}}(t)e^{j\omega_s t}\right]. \tag{6.10}$$

Equation (6.10) is equivalent to

$$L\frac{d\vec{\boldsymbol{i}}(t)}{dt} + j\omega_s L\vec{\boldsymbol{i}}(t) = \vec{\boldsymbol{v}}(t). \tag{6.11}$$

To conclude, the ideal inductor equation becomes, in the phasor domain,

$$v(t) = L\frac{di(t)}{dt} \quad \overset{\textit{Phasor transform}}{\longrightarrow} \quad \vec{\boldsymbol{v}}(t) = L\frac{d\vec{\boldsymbol{i}}(t)}{dt} + j\omega_s L\vec{\boldsymbol{i}}(t), \tag{6.12}$$

which can be represented as a complex resistance $j\omega_s L$ in series with an ideal inductance L. Phasor current $\vec{\boldsymbol{i}}(t)$, flowing through such circuit element, produces voltage phasor $\vec{\boldsymbol{v}}(t)$.

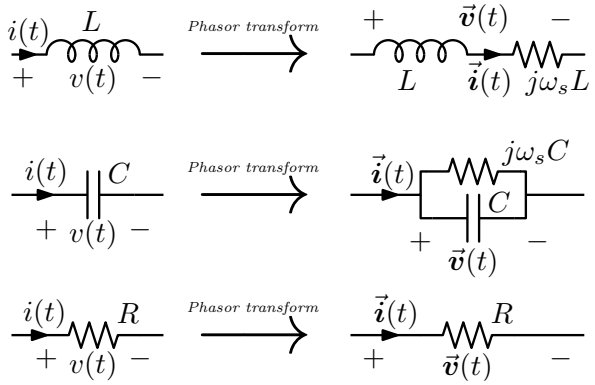


Figure 6.4: Phasor transformations of the ideal capacitor, inductor and resistor.

Similarly, for the ideal capacitor equation $i(t) = Cdv(t)/dt$ becomes,

$$i(t) = C\frac{dv(t)}{dt} \quad \overset{\text{Phasor transform}}{\longrightarrow} \quad \vec{\boldsymbol{i}}(t) = C\frac{d\vec{\boldsymbol{v}}(t)}{dt} + j\omega_s C\vec{\boldsymbol{v}}(t), \tag{6.13}$$

which can be represented as a complex resistance $j\omega_s C$ in parallel with an ideal capacitance C. On the contrary, ideal resistor equation is invariant with respect to the phasor transformation. The circuit transformation is also illustrated in Fig. 6.4.

Such representations are not only useful in dc-ac resonant inverters, where it is of interest to investigate how the tank current envelope $|\vec{\boldsymbol{i}}(t)|$ responds to the control command [43, 44], but also for dc-dc converters when the small ripple approximation is not verified.

Notice that, once the phasor transformation is performed, currents and voltages are complex functions of the time. Therefore, for each independent capacitor (inductor), two state variable are considered, one for the real part and one for the imaginary part of the associated voltage (current) dynamic phasor.

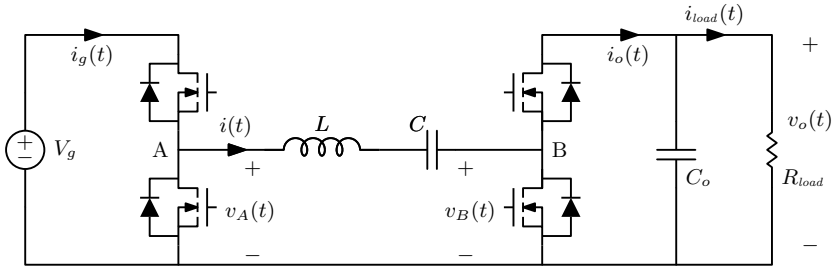


Figure 6.5: Schematic diagram of the Dual Half Bridge Converter.

6.3.1 Modeling of a phase shift controlled DHB-SRC

Let us apply the concepts illustrated above to the phase-controlled series resonant converter of Fig. 6.5. In the model, dc-side quantities averaged over the switching period T_s are indicated as $\bar{x}(t)$, whereas dynamic phasors are indicated as $\vec{\boldsymbol{x}}(t)$. In this section, waveforms $v_A(t)$ and $v_B(t)$ have constant frequency f_s and constant duty cycles $D_A = D_B = 0.5$. As for $v_g(t)$ and $v_o(t)$, as long as the *small-ripple approximation* can be invoked, we can state that they are essentially baseband signals, with negligible content at multiple of the switching frequency

$$\begin{cases} v_o(t) \approx \bar{v}_o(t) = V_o + \hat{\bar{v}}_o \\ v_g(t) \approx \bar{v}_g(t) = V_g + \hat{\bar{v}}_g \end{cases}. \tag{6.14}$$

With these assumptions, $v_A(t)$ and $v_B(t)$ are formed by baseband terms $v_A^{(0)}(t)$, $v_B^{(0)}(t)$ plus harmonics $v_A^{(l)}(t)$ and $v_B^{(l)}(t)$ oscillating at frequencies $f_l = lf_s$, $(l = 1, 3, 5..)$. Baseband terms are

$$\begin{cases} v_A^{(0)}(t) = \dfrac{\bar{v}_g(t)}{2} \\ v_B^{(0)}(t) = \dfrac{\bar{v}_o(t)}{2} \end{cases} \tag{6.15}$$

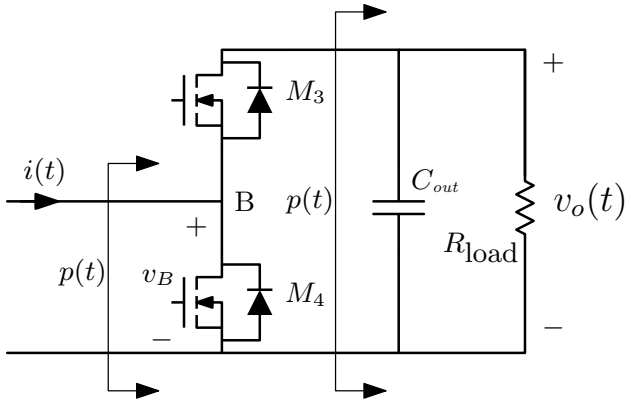


Figure 6.6: Output stage of the series resonant dc-dc converter.

while harmonic expressions are

$$\begin{cases} v_A^{(l)}(t) = \dfrac{2}{l\pi}\bar{v}_g(t)\cos\left(l\omega_s t + l\varphi_A(t)\right) \\ v_B^{(l)}(t) = \dfrac{2}{l\pi}\bar{v}_o(t)\cos\left(l\omega_s t - l\varphi_B(t)\right) \end{cases}. \tag{6.16}$$

In general, all terms (6.15) and (6.16) participate to the converter dynamics. However, the converter of Fig. 6.5 is supposed to be designed in such way that the fundamental harmonic approximation can be applied. In this case, only the dynamics associated with the fundamental harmonic ($l = 1$) and the average dynamics are considered. When the converter is perturbed with a small-signal oscillating at some frequency f_m, for each harmonic defined in (6.16), the dynamic phasor definition (6.6) can be applied,

$$\begin{cases} \vec{\boldsymbol{v}}_A(t) = \vec{\boldsymbol{V}}_A\left(1 + \dfrac{1}{V_g}\hat{\bar{v}}_g(t) + j\hat{\varphi}_A(t)\right) \\ \vec{\boldsymbol{v}}_B(t) = \vec{\boldsymbol{V}}_B\left(1 + \dfrac{1}{V_o}\hat{\bar{v}}_o(t) - j\hat{\varphi}_B(t)\right) \end{cases}. \tag{6.17}$$

As for the average output current $\bar{i}_o(t)$, the conservation of the averaged power can be used. Under the hypothesis of lossless bridges, the instantaneous power $p(t)$ at the AC-side of the leg B is equal to the instantaneous power at the

DC-side (Fig. 6.6)

$$p(t) = v_B(t)i(t) \tag{6.18}$$

that can be represented as $p(t) = \bar{p}(t) + \tilde{p}(t)$ where $\bar{p}(t)$ represents the average power and $\tilde{p}(t)$ is the fluctuating power responsible for the output ripple. Since we are interested in describing the average dynamics of the output voltage, the fluctuating term $\tilde{p}(t)$ is neglected. The average power $\bar{p}(t) = P_{DC} + \hat{\bar{p}}(t)$ is calculated as follows

$$\bar{p}(t) = \bar{v}_B(t)\bar{i}(t) + \frac{1}{2}\Re\sum_{l=1}^{\infty}\left[\vec{v}_B^{(l)}(t)\vec{i}^{(l)*}(t)\right] \tag{6.19}$$

where

$$\begin{cases} \bar{v}_B(t) = V_B + V_o\hat{d}_B(t) + D_B\hat{\bar{v}}_o(t) \\ \bar{i}(t) = \bar{I} + \hat{i}(t) \\ \vec{v}_B^{(l)}(t) = \vec{V}_B^{(l)} + \frac{\vec{V}_B^{(l)}}{B^{(l)}}\hat{a}_B^{(l)}(t) - j\vec{V}_B^{(l)}\hat{\varphi}_B^{(l)}(t) + \frac{\vec{V}_B^{(l)}}{V_o}\hat{\bar{v}}_o(t) \\ \vec{i}^{(l)}(t) = \vec{I}^{(l)} + \hat{\vec{i}}^{(l)}(t) \end{cases} . \tag{6.20}$$

In (6.19), the term $\bar{v}_B(t)\bar{i}(t)$ accounts for the power delivered by the average tank current and the average voltage of $v_B(t)$. The generic term $\frac{1}{2}\vec{v}_B^{(l)}(t)\vec{i}^{(l)*}(t)$ represents the average (baseband) component of the power associated to the l-th harmonics of $v_B(t)$ and $i(t)$. Since the fundamental harmonic approximation is applied, only the first term of the summation is considered.

To derive the output voltage dynamic equation, consider the average power $\bar{p}_{c_o}(t)$ entering in the output capacitor

$$\bar{p}_{c_o}(t) = \bar{p}(t) - \frac{\overline{v_o^2}(t)}{R_{\text{LOAD}}} \tag{6.21}$$

where $\overline{v_o^2}(t)/R_{\mathrm{LOAD}}$ is the instantaneous power delivered to the load. Under the small-ripple approximation (6.14), one has $\overline{v_o^2}(t) \approx \bar{v}_o^2(t)$. The average current $\bar{i}_{c_o}(t)$ flowing through the output capacitor is derived dividing Eq. (6.21) by $\bar{v}_o(t)$,

$$\bar{i}_{c_o}(t) = \frac{1}{\bar{v}_o(t)} \left(\bar{p}(t) - \frac{\bar{v}_o^2(t)}{R_{\mathrm{LOAD}}} \right). \tag{6.22}$$

Finally, the dynamic equation describing the dynamics of the output capacitor is

$$\frac{d}{dt}\bar{v}_o(t) = \frac{1}{C_o \bar{v}_o(t)} \left(\bar{p}(t) - \frac{\bar{v}_o^2(t)}{R_{\mathrm{LOAD}}} \right). \tag{6.23}$$

After linearization, equation (6.22) yields the averaged output current expression $\bar{i}_o(t)$

$$\bar{i}_o(t) = \frac{V_o}{R_{load}} + \frac{1}{2}\hat{\bar{i}}(t) - \Re\left[\frac{\vec{\boldsymbol{I}}^*}{2}\frac{\vec{\boldsymbol{V}}_B}{V_o}\right]\hat{\varphi}_B(t) + \Re\left[\frac{1}{2}\frac{\vec{\boldsymbol{V}}_B}{V_o}\hat{\vec{\boldsymbol{i}}}^*(t)\right], \tag{6.24}$$

where $\vec{\boldsymbol{x}}^*(t)$ denotes the complex conjugate of $\vec{\boldsymbol{x}}(t)$. Similar procedure can be followed to calculate the expression for $\bar{i}_g(t)$. The *combined linear steady state and small-signal model* of the DHB-SRC can be drawn as shown in Fig. 6.7. The equivalent circuit makes use of two *phasor transformers*, i.e. two-port network elements governed by the equations

$$\begin{cases} \vec{\boldsymbol{v}}_A(t) = \vec{\boldsymbol{n}}_A \bar{v}_g(t) \\ \bar{v}_A(t) = \bar{n}_A \bar{v}_g(t) \\ \bar{i}_g(t) = \dfrac{1}{2}\Re\left[\vec{\boldsymbol{n}}_A \vec{\boldsymbol{i}}^*(t)\right] + \bar{n}_A \bar{i}(t) \end{cases} \text{, where } \begin{cases} \vec{\boldsymbol{n}}_A \triangleq \dfrac{2}{\pi} e^{+j\Phi_A} \\ \bar{n}_A \triangleq 1/2 \end{cases}, \tag{6.25}$$

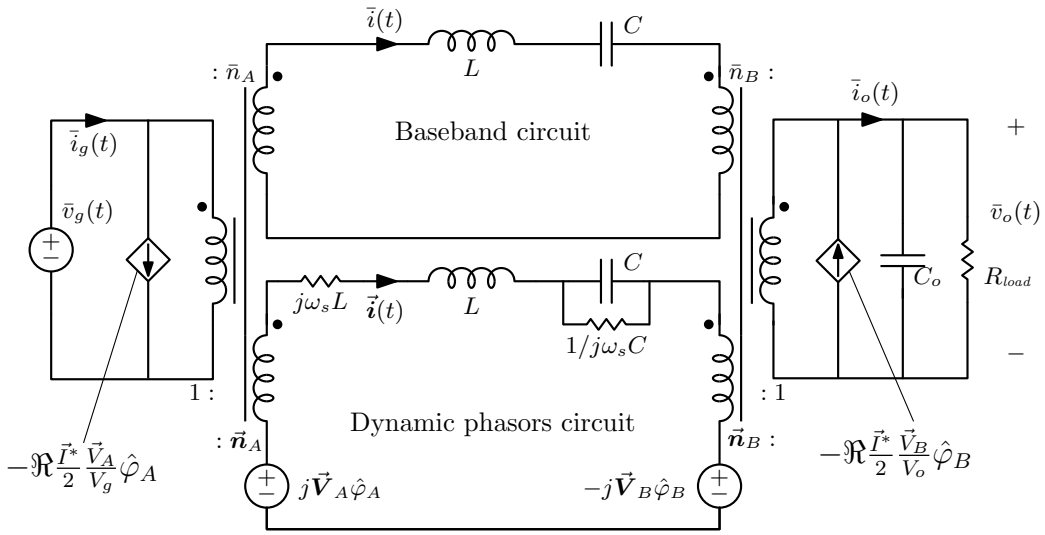


Figure 6.7: Combined linear steady state and small-signal model of the phase-controlled converter of Fig. 6.5.

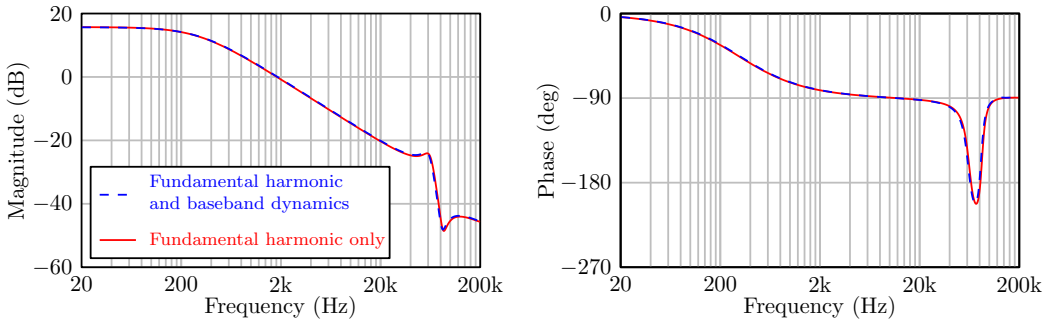
and

$$\begin{cases} \vec{\boldsymbol{v}}_B(t) = \vec{\boldsymbol{n}}_B \bar{v}_o(t) \\ \bar{v}_B(t) = \bar{n}_B \bar{v}_o(t) \\ \bar{i}_o(t) = \dfrac{1}{2}\Re\left[\vec{\boldsymbol{n}}_B \vec{\boldsymbol{i}}^*(t)\right] + \bar{n}_B \bar{i}(t) \end{cases} \text{, where } \begin{cases} \vec{\boldsymbol{n}}_B \triangleq \dfrac{2}{\pi} e^{-j\Phi_B} \\ \bar{n}_B \triangleq 1/2 \end{cases} . \tag{6.26}$$

The equations above express, to within the narrowband approximation, the conservation of the average power in the inversion/rectification operation implemented by the input and output bridges. The equivalent circuit model leads to transfer functions

$$\begin{cases} G_{v\varphi_A}(s) \triangleq \dfrac{\hat{\bar{v}}_o(s)}{\hat{\varphi}_A(s)} \\ G_{v\varphi_B}(s) \triangleq \dfrac{\hat{\bar{v}}_o(s)}{\hat{\varphi}_B(s)} \end{cases} , \tag{6.27}$$

which relates the small-signal variations of φ_A and φ_B to corresponding perturbations of $\bar{v}_o$.



(a) (b)

Figure 6.8: Bode plot of the transfer function $G_{v\varphi_B}(s)$: (a) Magnitude, (b) Phase.

Knowledge of $G_{v\varphi}(s)$ is sufficient, in analog control, to determine the small-signal dynamics of the plant and proceed with controller design. In other words, if the continuous-time phase control signal $u(t)$ produced by the analog compensator is expressed in radians, one has $\hat{\varphi}(t) = \hat{\varphi}_A(t) + \hat{\varphi}_B(t) = \hat{u}(t)$. On the other hand, additional dynamics is present in digital control loops due to the non-instantaneous relationship between the control command $\hat{u}[k]$ and $\hat{\varphi}(t)$. Characterization of such further dynamics is object chapters 7. The transfer function $G_{v\varphi_B}(s)$ obtained by the equivalent circuit of Fig. 6.7 calculated with the following parameters,

$$\begin{cases} f_s = 200\text{kHz} \\ L = 2.2\mu\text{H} \\ C = 630\text{nF} \\ C_o = 110\mu\text{F} \end{cases}, \tag{6.28}$$

are shown in the Bode diagram of Fig. 6.8 in the operating point $\Phi = 30°$. In the figure, the comparison between the model calculated with and without the average dynamics of the resonant tank is shown. It worth to notice that, for the case of pure phase shift modulation, the baseband circuit of Fig. 6.7

has a very weak influence on the converter dynamics. However, as will be shown in chapter 9, this fact is no longer valid when a duty cycle modulation is included.

6.4 Dynamic modeling of uniformly sampled modulators

The modulator is the block used to generate converter driving signals starting from duty cycle and phase shift reference signals. In an analog control, modulating signals are continuous-time signals. In this case, modulators are also called *naturally sampled* and they are known not to introduce any additional small-signal dynamics in the feedback regulation loop [47]. The reason is that, since the control command produced by the analog regulator is transmitted instantaneously to the power converter, in the small-signal domain the modulator is modeled as a simple constant gain. As shown in the first part of this thesis, digital implementation of such modulators are employed in conjunction with full-bridge or Dual Active Bridge converters control, advanced multi-variable digital controllers and online efficiency optimization algorithms. Other examples are investigated in [29, 48–51]. In such *uniformly sample modulators*, the control command is discrete in time and is produced by a digital compensator which updates its values on a clock cycle basis. Because of the sampled nature of the modulating signal, the control command no longer transmits instantaneously to the power converter. As a result, when implemented digitally, modulation introduces additional dynamics which is not accounted for by traditional models. In [47], a method is presented for AC analysis of most used PWM modulators. Named $u_d[k]$ the duty cycle modulating signal and $c(t)$ the modulated signal, [47] presents a methodology

to calculate the transfer function

$$G_{u_d \to d}(s) = \frac{\hat{d}(s)}{\hat{u}_d(s)} \tag{6.29}$$

where with the notation d the average of the signal $c(t)$ is indicated.
In the following this concept is extended for the case of Uniformly Sampled Phase Shift Modulators (USPSM) (chapter 7) and for the case of combined phase shift and pulse width modulators (chapter 8). In this case, defined the dynamic phasor

$$\vec{\boldsymbol{c}}(t) = \vec{\boldsymbol{C}} \left(1 + \frac{\hat{a}}{|\vec{\boldsymbol{C}}|} - j\hat{\varphi}(t) \right) \tag{6.30}$$

associated with the fundamental harmonic of $c(t)$, transfer functions of interest are

$$\begin{cases} G_{u_d \to a}(s) = \dfrac{\hat{a}(s)}{\hat{u}_d(s)} \\ G_{u_d \to \varphi}(s) = \dfrac{\hat{\varphi}(s)}{\hat{u}_d(s)} \\ G_{u_\varphi \to \varphi}(s) = \dfrac{\hat{\varphi}(s)}{\hat{u}_\varphi(s)} \\ G_{u_\varphi \to a}(s) = \dfrac{\hat{a}(s)}{\hat{u}_\varphi(s)} \end{cases} . \tag{6.31}$$

Transfer functions listed in (6.31) describe how instantaneous amplitude and phase of $\vec{\boldsymbol{c}}(t)$ are related to the modulating signals $u_d[k]$ and $u_\varphi[k]$.

Chapter 7

Small-signal analysis of phase shift modulators

Contents

7.1 Introduction

This chapter clarifies the modeling procedure for describing the small-signal dynamics of most used uniformly sampled phase shift modulators. The methodology follows the approach published in [47] and makes use of the

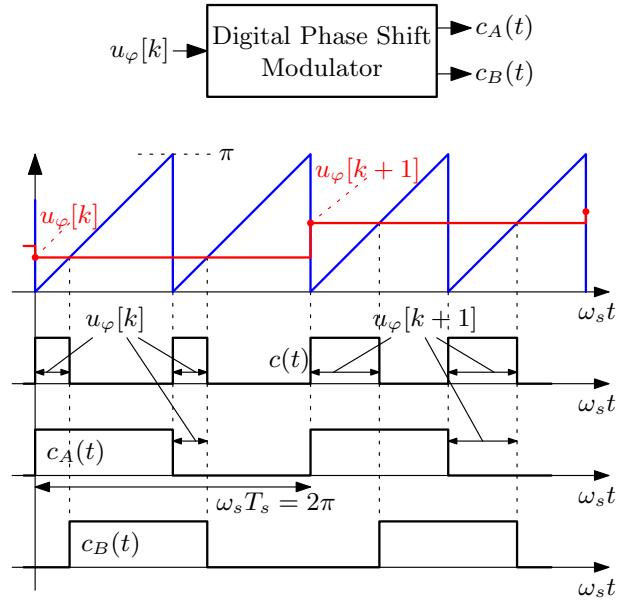


Figure 7.1: Operation of a uniformly sampled trailing edge phase shift modulator. Both $u_\varphi[k]$ and time are expressed in radians.

theory of *dynamic phasors*. The analysis here disclosed refers to the case of pure phase shift modulation in which duty cycle of modulated signals are kept constants and equal to 50% for simplicity. Results shown in this work indicates that discrete-time, or uniformly sampled, PSM introduces a transport delay of small-signal nature. Furthermore, and in close analogy with the theory of uniformly sampled pulse width modulators, such delay depends on the modulator carrier type as well as on the converter operating point.

7.2 Model derivation

In this section the derivation of transport delay of PSM modulators under study is disclosed for the case of the *trailing edge modulator*. In next sections results for *leading-edge* and *symmetrical* modulators are presented as well.

Main waveforms of the trailing edge modulator are illustrated in Fig. 7.1. Assume $u_\varphi[k]$ consists of the DC term Φ plus a sinusoidal modulation at angular frequency ω_m,

$$\begin{aligned} u_\varphi[k] &= \Phi + \hat{u}_\varphi[k] \\ &= \Phi + \hat{u}_m \sin\left(\omega_m k T_s\right). \end{aligned} \tag{7.1}$$

Following [47], it is assumed that the modulation and sampling frequencies are commensurable,

$$\frac{\omega_m}{\omega_s} = \frac{L}{N}, \quad L, N \in \mathbb{N} \tag{7.2}$$

This assumption has the sole objective of simplifying calculations by allowing the use of Fourier series rather than double integrals. The conclusions that will be drawn are not affected by such hypothesis. The modulator produces the modulated signals $c_A(t)$ and $c_B(t)$. Based on the foregoing discussions, only components of $c_A(t)$ and $c_B(t)$ at $\omega_s+\omega_m$ and $\omega_s-\omega_m$ will be considered rather than the entire signal spectra. Not to further complicate the mathematical notation, however, the same symbols c_A and c_B will be employed in the following. Signal $c_A(t)$ is simply a 50% duty cycle square-wave phase-locked to the sampling instants. Therefore, phasor $\vec{\boldsymbol{c}}_A(t)$ associated with $c_A(t)$ is constant,

$$\vec{\boldsymbol{c}}_A = \vec{\boldsymbol{C}}_A = \text{constant} \tag{7.3}$$

In the following, phase Φ_A of $\vec{\boldsymbol{C}}_A$ is taken as a reference and set to zero.

$$\Phi_A = 0 \tag{7.4}$$

This choice makes $\vec{\boldsymbol{C}}_A$ a positive real number. On the other hand, phase modulation of $c_B(t)$ forces its dynamic phasor to vary in time. To be general,

both phase and amplitude modulation of $c_B(t)$ will be hypothesized,

$$\vec{\boldsymbol{c}}_B(t) = a_B(t)e^{-j\varphi_B(t)}. \tag{7.5}$$

Observe that the steady-state value of $\vec{\boldsymbol{c}}_B(t)$ is simply

$$\vec{\boldsymbol{C}}_B = \vec{\boldsymbol{C}}_A e^{-j\Phi_B}, \tag{7.6}$$

and from (7.3) and (7.4), total phase shift $\varphi(t)$ coincides with phase angle $\varphi_B(t)$

$$\varphi(t) = \varphi_B(t). \tag{7.7}$$

Goal of the following calculation is to derive a closed-form expression for both $a_B(t)$ and $\varphi(t)$ in the small-signal limit. As already explained in chapter 6, under this hypothesis, the dynamic phasor defined in (7.5) can be expressed as follows,

$$\vec{\boldsymbol{c}}_B(t) = \vec{\boldsymbol{C}}_B \left(1 + \frac{1}{|\vec{\boldsymbol{C}}_B|}\hat{a}_B(t) - j\hat{\varphi}_B(t)\right) \tag{7.8}$$

which phasor representation is sketched in Fig. 7.2.

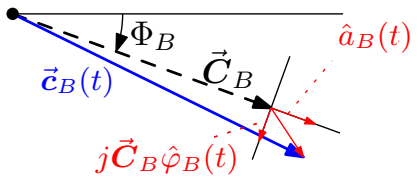


Figure 7.2: Phasor representation of the signal $c_B(t)$.

The followed methodology is by all means the same exemplified in section 6.2. Start by evaluating the spectrum of $c_B(t)$ at a generic frequency ω.

$$c_B(\omega) \triangleq \frac{1}{T_p}\int_{T_p} c_B(\tau)e^{-j\omega\tau}d\tau \tag{7.9}$$

where $T_p \triangleq NT_s = LT_m$ is the period of the perturbation. The analytic signal $z_{c_B}(\omega)$ is derived by suppressing the negative portion of the spectrum and multiplying the positive portion by two. Formally, $z_{c_B}(\omega)$ is calculated by multiplying $c_B(\omega)$ by $2u(\omega)$ where $u(\omega)$ is the *Heaveside function*,

$$z_{c_B}(\omega) \triangleq \begin{cases} 2c_B(\omega) & \omega > 0 \\ c_B(\omega) & \omega = 0 \\ 0 & \omega < 0 \end{cases} . \tag{7.10}$$

Finally, the spectrum $\vec{\boldsymbol{c}}_B(\omega)$ of the dynamic phasor $\vec{\boldsymbol{c}}_B(t)$ associated with $c_B(t)$ is obtained by evaluating (7.10) at $\omega = \omega_s \pm \omega_m$,

$$\vec{\boldsymbol{c}}_B(\omega) \triangleq \begin{cases} z_{c_B}(\omega + \omega_s) & \omega = \pm\omega_m \\ 0 & otherwise \end{cases} . \tag{7.11}$$

In turn, $\vec{\boldsymbol{c}}_B(\omega)$ can be evaluated analytically once the time-domain expression of $c_B(t)$ is given. For the trailing-edge phase shift modulator one has

$$c_B(t) = \begin{cases} 0 & k\omega_s T_s \le \omega_s t \le k\omega_s T_s + u_\varphi[k] \\ 1 & k\omega_s T_s + u_\varphi[k] \le \omega_s t \le k\omega_s T_s + u_\varphi[k] + \dfrac{\omega_s T_s}{2} \\ 0 & k\omega_s T_s + u_\varphi[k] + \dfrac{\omega_s T_s}{2} \le \omega_s t \le (k+1)\,\omega_s T_s \end{cases} , \tag{7.12}$$

where index $k = 0 \ldots N-1$ runs through all switching intervals inside the perturbation period T_p.

Evaluation of $\vec{\boldsymbol{c}}_B(\omega)$ at the two frequencies of interest $\omega = \pm\omega_m$ yields

$$\vec{\boldsymbol{c}}_B(\omega = \pm\omega_m) = \frac{2}{N\left(\omega_s \pm \omega_m\right) T_s} \quad \left(1 - e^{-j(\omega_s \pm \omega_m)\frac{T_s}{2}}\right) \sum_{k=0}^{N-1} e^{-j(\omega_s \pm \omega_m)\left(kT_s + u_\varphi[k]\frac{T_s}{2\pi}\right)}. \tag{7.13}$$

Expression (7.13) is the *exact* expression of $\vec{\boldsymbol{c}}_B(\pm\omega_m)$.
Introduce now a small-signal assumption $u[k] \ll 1$ by truncating $\vec{\boldsymbol{c}}_B(\pm\omega_m)$ to its first-order Taylor expansion on $\hat{u}_m$. Result of such approximation is

$$\vec{\boldsymbol{c}}_B(\pm\omega_m) \approx \mp 2j \frac{\hat{u}_m}{2\pi} \cos\left(\frac{\omega_m T_s}{4}\right) e^{-j(\omega_s \pm \omega_m)\frac{(\Phi + \frac{\pi}{2})}{\omega_s}}. \tag{7.14}$$

Going back to the time domain, the dc+small-signal expression of $\vec{\boldsymbol{c}}_B(t)$ is

$$\vec{\boldsymbol{c}}_B(t) = \vec{\boldsymbol{C}}_B + \vec{\boldsymbol{c}}_B(\omega_m) e^{j\omega_m t} + \vec{\boldsymbol{c}}_B(-\omega_m) e^{-j\omega_m t}, \tag{7.15}$$

which can be re-arranged as follows,

$$\vec{\boldsymbol{c}}_B(t) = \vec{\boldsymbol{C}}_B \left(1 - j\hat{u}_m \cos\left(\frac{\omega_m T_s}{4}\right) \sin\left(\omega_m \left(t - t_{PSM,TE}\right)\right)\right), \tag{7.16}$$

with

$$t_{PSM,TE} \triangleq \frac{1}{\omega_s}\left(\Phi + \frac{\pi}{2}\right). \tag{7.17}$$

Comparing (6.6) with (7.16), one concludes that

i) $\hat{a}_B(t) = 0$, i.e. no amplitude modulation is present. As shown in the next chapter this is not a general result, but is rather the consequence of the duty cycle being equal to 50%.

ii) the small-signal component of the instantaneous phase shift is

$$\hat{\varphi}(t) = \hat{u}_m \cos\left(\frac{\omega_m T_s}{4}\right) \sin\left(\omega_m \left(t - t_{PSM,TE}\right)\right). \tag{7.18}$$

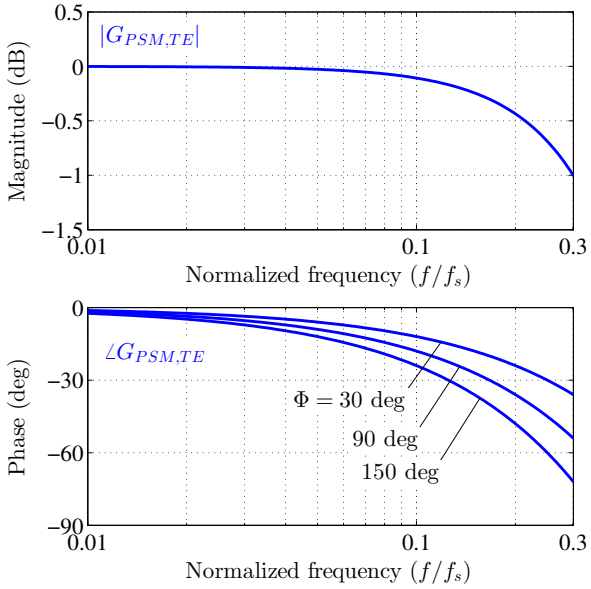


Figure 7.3: Frequency response of a uniformly sampled trailing-edge phase shift modulator.

The result (7.18) can be written in terms of small-signal frequency response (transfer function) relating $\hat{u}[k]$ to $\hat{\varphi}(t)$ obtaining the formulation introduced in (6.31)

$$G_{PSM,TE}(j\omega_m) \triangleq \frac{\hat{\varphi}(\omega_m)}{\hat{u}(\omega_m)} = \cos\left(\frac{\omega_m T_s}{4}\right) e^{-j\omega_m t_{PSM,TE}}. \tag{7.19}$$

7.3 Results discussion

Fig. 7.3 illustrates the Bode diagrams of $G_{PSM,TE}$ as a function of the normalized frequency f/f_s. As anticipated, the USPSM modulator introduces a transport delay of small-signal nature which manifests itself as a negative phase response throughout the entire frequency range. Such transport delay $t_{PSM,TE}$, expressed in (7.17), depends in general on both the switching rate and on the steady-state phase shift Φ. Notice, however, that the small-signal

phase lag introduced by $t_{PSM,TE}$ can be written in terms of the normalized frequency,

$$\angle G_{PSM,TE}(j\omega) = -\omega t_{PSM,TE} = -\frac{\omega}{\omega_s}\left(\Phi + \frac{\pi}{2}\right). \tag{7.20}$$

At $\omega/\omega_s = 1/10$, for instance, the modulator phase lag varies between 9° and 27° as the operating point Φ varies from 0 to 180°. Expression of $G_{PSM,TE}$ also indicates a magnitude attenuation effect, expressed by the $\cos(\omega_m T_s/4)$ term. As visible from Fig. 7.3, such attenuation is equal to ≈ -1 dB for $\omega/\omega_s \approx 0.3$, and therefore remains an entirely negligible effect throughout most of the frequency range. In a practical application of the foregoing model, the small-signal transport delay introduced by the phase shift modulation is the most relevant effect, and $G_{PSM,TE}$ can be approximated as

$$G_{PSM,TE}(j\omega) \approx e^{-j\omega t_{PSM,TE}}. \tag{7.21}$$

The above discussion leads to an extension of the phasor model of the control-to-output dynamics (6.27),

$$\begin{aligned} G_{vu}(s) \triangleq \frac{\hat{\tilde{v}}_o(s)}{\hat{u}(s)} &= G_{PSM}(s) G_{v\varphi}(s) \\ &\approx G_{v\varphi}(s) e^{-st_{PSM}}, \end{aligned} \tag{7.22}$$

which now includes the small-signal modulation dynamics. An additional delay term t_{cntrl} due to A/D conversion and controller computational latency can be included as well, leading to an overall loop delay $t_d \triangleq t_{cntrl} + t_{PSM}$,

$$\begin{aligned} G_{vu}(s) &\approx G_{v\varphi}(s) e^{-st_d}, \\ t_d &\triangleq t_{cntrl} + t_{PSM}. \end{aligned} \tag{7.23}$$

As a conclusive remark related to the model applicability, it is to be noted

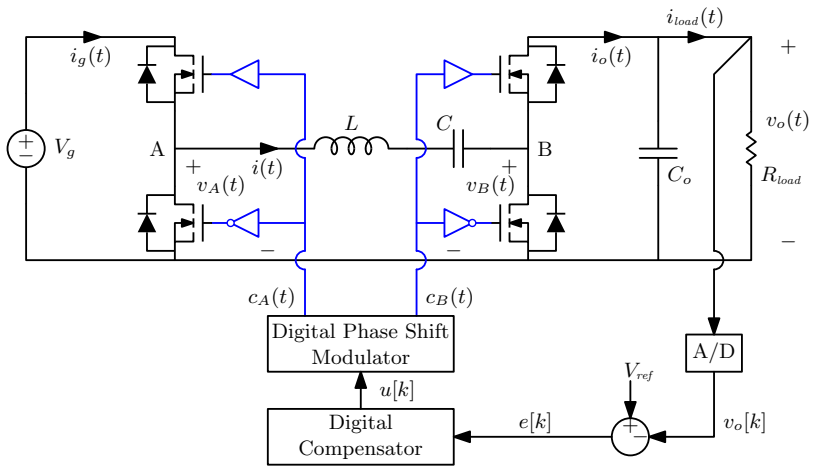


Figure 7.4: Digital phase-controlled dual half-bridge series resonant converter.

that the developed theory relies on *averaged* modeling. In fact, both dynamic phasor models and the narrowband approximation invoked to derive (7.19) only examine a limited range of the frequency axis around ω_s. Furthermore, the output dynamics of the converter is only described in the low-frequency range. Application of the averaging approach in digitally controlled converters, however, is only possible to the extent that aliasing effects induced by the sampling operation are negligible. In the scenario of Fig. 7.4, this requirement is enforced by the filter capacitor C_o, which strongly limits the switching ripple superimposed to the output voltage. Under different circumstances, however, in which sampling-induced effects may become relevant, one should resort to an exact discrete-time description of the converter dynamics [52] [53].

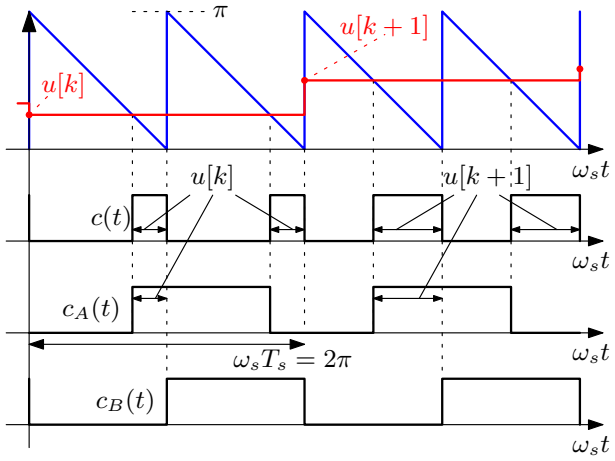


Figure 7.5: Operation of a uniformly sampled leading-edge phase shift modulator.Both $u[k]$ and time are expressed in radians.

7.4 Results for different types of phase shift modulators

Phase shift modulators are here classified according to the PWM carrier employed to generate the phase shift between $c_A(t)$ and $c_B(t)$. The trailing-edge modulator discussed above and whose operating waveforms are depicted in Fig. 7.1 generates a fixed-phase $c_A(t)$ and a phase-modulated $c_B(t)$ lagging $c_A(t)$ by a controllable amount $\varphi_B(t) = \varphi(t)$.

If the PWM carrier signal is changed to a leading-edge type, as in Fig. 7.5, the corresponding modulator will generate a fixed-phase $c_B(t)$ and a phase-modulated $c_A(t)$ *leading* $c_B(t)$ by a controllable angle $\varphi_A(t) = -\varphi(t)$.

As for the symmetrical phase shift modulator, obtained using a symmetrical (triangle-wave) PWM carrier, signals $c_A(t)$ and $c_B(t)$ are both phase-modulated symmetrically with respect to the carrier valley point, $c_A(t)$ being anticipated by $\varphi_A(t) = -\varphi(t)/2$ and $c_B(t)$ being delayed by $\varphi_B(t) = \varphi(t)/2$. Main operating waveforms are sketched in Fig. 7.6. With these generalizations, the

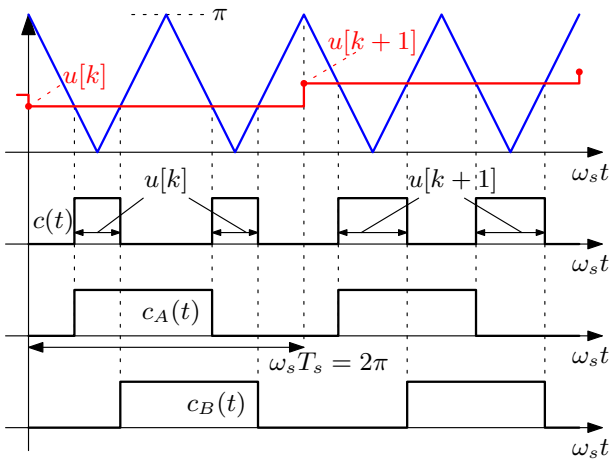


Figure 7.6: Operation of a uniformly sampled symmetrical phase shift modulator. Both $u[k]$ and time are expressed in radians.

most general form of the linear equivalent circuit model of a digital phase-controlled resonant converter becomes the one illustrated in Fig. 7.7. In such a scheme, the baseband circuit is not included because, as shown in section 6.3.1, the average dynamics does not influence the total dynamics in pure phase shift controlled DHB-SRC. Gains $(k_{\varphi_A}, k_{\varphi_B})$ are equal to $(0, 1)$, $(1, 0)$ or $(1/2, 1/2)$ for the trailing-edge, leading-edge or symmetrical modulation respectively. Complex transformers are still governed by (6.25) and (6.26), with the complex turns ratios redefined as

$$\vec{\boldsymbol{n}}_A \triangleq \frac{2}{\pi} e^{j\Phi_A}, \qquad \vec{\boldsymbol{n}}_B \triangleq \frac{2}{\pi} e^{-j\Phi_B}. \tag{7.24}$$

Uniformly sampled phase shift modulators of the leading-edge and symmetrical type can be analyzed following the same lines as done in section 7.2, leading to the following general results:

i) The frequency response of any uniformly sampled phase shift modulator

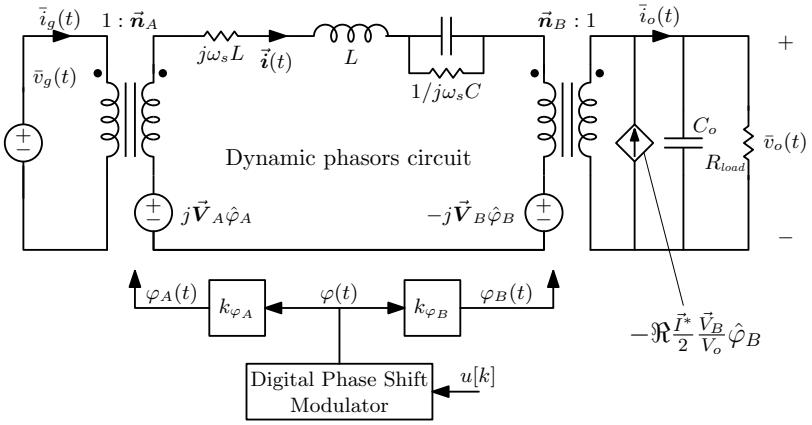


Figure 7.7: Combined linear steady state and small signal model of the phase-controlled converter of Fig. 7.4 valid for a generic phase shift modulation.

Table 7.1: Frequency responses of basic types of single-update uniformly sampled phase shift modulators

Carrier type	$\lvert G_{PSM}(\omega)\rvert$	t_{PSM}
Trailing-edge	$\cos\left(\frac{\pi}{2}\frac{\omega}{\omega_s}\right)$	$\frac{1}{\omega_s}\left(\Phi+\frac{\pi}{2}\right)$
Leading-edge	$\cos\left(\frac{\pi}{2}\frac{\omega}{\omega_s}\right)$	$\frac{1}{\omega_s}\left(\frac{3}{2}\pi-\Phi\right)$
Symmetrical	$\cos\left(\frac{\pi}{2}\frac{\omega}{\omega_s}\right)\cos\left(\frac{\Phi}{2}\frac{\omega}{\omega_s}\right)$	$\frac{\pi}{\omega_s}=\frac{T_s}{2}$

can be put in the general form

$$G_{PSM}(j\omega) = |G_{PSM}(\omega)|e^{-j\omega t_{PSM}}. \tag{7.25}$$

ii) The most relevant dynamic effect introduced by a sampled PSM is the small-signal transport delay t_{PSM} which depends, in general, on the carrier type and on the steady-state phase shift Φ.

iii) The symmetrical phase shift modulator exhibits a small-signal delay

Table 7.2: Frequency responses of basic types of double-update uniformly sampled phase shift modulators

Carrier type	$\lvert G_{PSM}(\omega)\rvert$	t_{PSM}
Trailing-edge	1	$\dfrac{\Phi}{\omega_s}$
Leading-edge	1	$\dfrac{\pi-\Phi}{\omega_s}$
Symmetrical	$\cos\left(\dfrac{\Phi}{2}\dfrac{\omega}{\omega_s}\right)$	$\dfrac{\pi}{2\omega_s}=\dfrac{T_s}{4}$

which is independent of Φ.

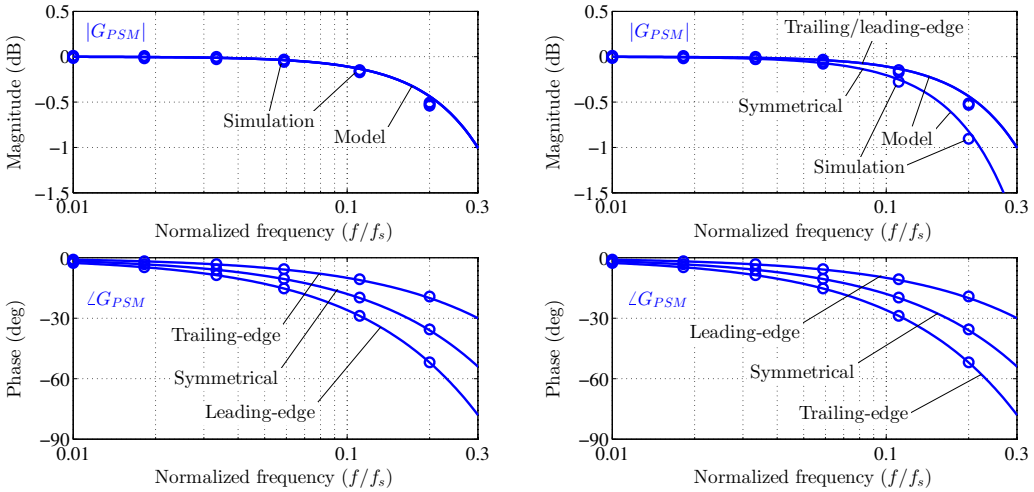
Closed-form expressions of $|G_{PSM}(\omega)|$ and t_{PSM} are reported in Tab. 7.1 for the trailing-edge, leading-edge and symmetrical modulators.

7.4.1 Double-update modulators

All modulators discussed in the previous sections process a modulating signal sampled at the switching rate f_s, and can therefore be referred to as *single-update* modulators. In resonant dc-dc converters employing a full-bridge rectifier, however, the fundamental frequency of the output voltage ripple is equal to *twice* f_s. It becomes then possible to operate both the controller and the modulator at a sampling rate equal to $2f_s$. Such *double-update* modulators can be treated using the theory developed above. Main results for the double-update trailing-edge, leading-edge and symmetrical phase shift modulators are reported in Tab. 7.2. Double-update operation has the general advantage of reducing the equivalent small-signal transport delay with respect to the single-sampled case. Furthermore, it removes the small amplitude attenuation present in single-update trailing-edge and leading-edge modulators.

7.5 Simulation Results

The theoretical framework developed in the previous sections is first validated by means of a campaign of computer simulations. The simulations are carried out by simulating the modulator as a standalone system and in open-loop. The time-domain responses of various single-update and double-update USPSMs to the modulating signal (7.1) are acquired for different ω_m's, and successively post-processed with a Discrete Fourier Transform-based analysis in order to extract the spectrum of the signal's instantaneous phase. More precisely, the mathematical post-processing follows the dynamic phasor definition outlines in section 6.2: outputs $c_A(t)$ and $c_B(t)$ of the modulator are first DFT-transformed, then their negative frequencies suppressed. Signals are then time-domain multiplied by the complex carrier $e^{-j\omega_s t}$ in order to shift their spectra. The instantaneous phase of the time-domain signals resulting from this operation is then analyzed in the frequency domain and its frequency components at $\omega = \pm\omega_m$ determined in both amplitude and phase. The dependence of such amplitude and phase on ω_m represents the frequency response under study. Fig. 7.8a illustrates the theoretical vs. simulated frequency responses for a trailing-edge, leading-edge and symmetrical phase shift modulator of the single-update type and around a steady-state operating point $\Phi = 10°$. Fig. 7.8b reports simulation results for $\Phi = 170°$, while corresponding simulation results for double-update modulators are reported in Fig. 7.9a and 7.9b. In the small-signal limit, simulations fully validate the theory and theoretical models predict the observed dependence of t_{PSM} on Φ. Comparison of Fig. 7.8a with 7.8b, and of Fig. 7.9a with 7.9b, confirms that t_{PSM} increases with Φ for a trailing-edge modulator, it decreases with Φ for a leading-edge modulator, and remains constant for a symmetrical modulator. Magnitude Bode diagrams also reveal the dependence of the attenuation



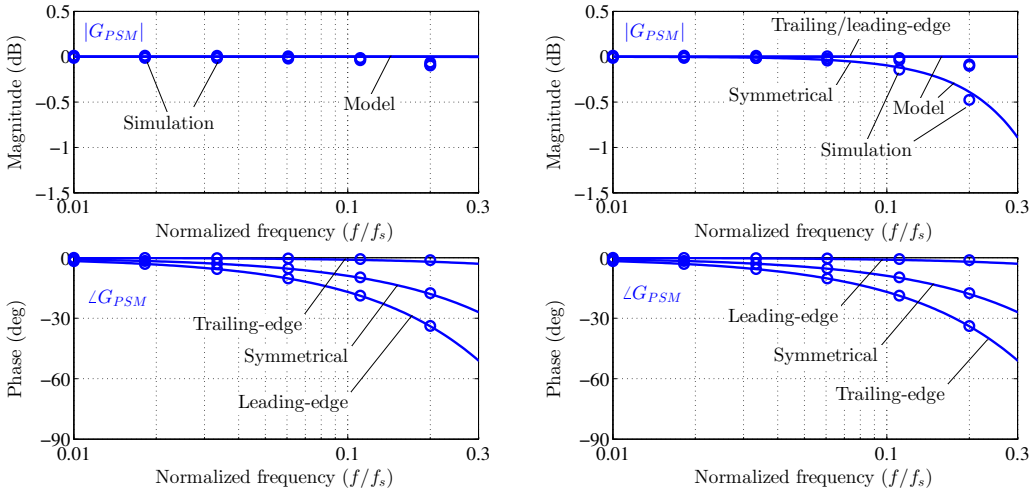
(a) (b)

Figure 7.8: Theoretical vs. simulated frequency response: trailing-edge, leading-edge and symmetrical single-update modulation with (a) $\Phi = 10°$ and (b) $\Phi = 170°$.

term on Φ for the symmetrical modulator, in agreement with the expressions reported in Tab. 7.1 and 7.2.

7.6 Experimental Results

The digital phase-controlled series resonant converter of Fig. 7.4 is prototyped for experimentally validating the foregoing models. Prototype parameters are those reported in Tab. 7.3. The prototype operates off a 12 V voltage source and produces a dc regulated output at 5 V, 1 A. The LC tank has a resonant frequency of about 132 kHz and is operated above resonance at a switching rate of 195 kHz. The inductance is realized with a Coilcraft® SMT power inductor of the DO3316P Series. As for the converter switching devices, Infineon OptiMOS®3 power MOSFET of the type IPD036N04L G is



(a) (b)

Figure 7.9: Theoretical vs. simulated frequency response: trailing-edge, leading-edge and symmetrical double-update modulation with (a) $\Phi = 10°$ and (b) $\Phi = 170°$.

Table 7.3: Case study converter parameters

Input voltage V_g	12 V
Output voltage V_o	5 V
Maximum output current I_{load}	1 A
Switching frequency f_s	195 kHz
Tank inductance L	2.3 µH
Tank capacitance C	630 nF
Equivalent tank parasitic resistance r_{par}	0.2 Ω
Output capacitance C_o	110 µF

employed, having $r_{ds,on} \approx 3.6$ mΩ and rated 40 V, 90 A. The 0.2 Ω equivalent tank parasitic resistance r_{par} accounts for the tank inductor parasitic resistance r_L and the MOSFETs $r_{ds,on}$. As for r_L, a value of 0.196 Ω is estimated by measuring the inductor resistance at 200 kHz using an impedance analyzer.

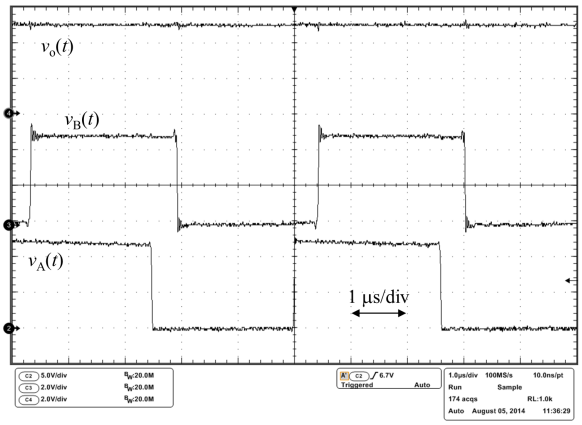


Figure 7.10: Converter steady-state operation at $V_g = 12$ V, $I_{load} = 1$ A. Output voltage $v_o(t)$: 2 V/div; $v_A(t)$: 5 V/div; $v_B(t)$: 2 V/div; time scale: 1 µs/div.

Considering that, in every instant in time, two MOSFETs are connected in series with the LC tank, r_{par} is estimated as $r_{par} = r_L + 2r_{ds,on} = 0.196\ \Omega + 2 \times 0.0036\ \Omega \approx 0.2\ \Omega$. The digital controller is VHDL-coded and implemented on a commercial FPGA development board by Altera®. The voltage loop gain $T(s)$ is compensated by means of a proportional-integral (PI) regulator designed for a crossover frequency of about 10 kHz. Experimental waveforms pertaining to the converter steady-state operation at $V_g = 12$ V, $I_{load} = 1$ A are reported in Fig. 7.10. In this operating point, $\Phi \approx 33°$. All three types of single-udpate phase shift modulation discussed above – trailing-edge, leading-edge and symmetrical – are tested. The trailing-edge and leading-edge implementations each have a hardware resolution of 8 bits, whereas the symmetrical modulator have a hardware resolution of 7 bits. In terms of the control angle φ, this amounts into a phase-shift hardware resolution of $\approx 1.4°$ and $\approx 2.8°$ respectively. In order to improve the resolution beyond such hardware limits, a 7-bit first-order Σ-Δ modulator is interposed between the digital compensator and the digital PSM [54]. With the use of the Σ-Δ block, the effective phase-shift resolution is reduced to few tens of thousandths

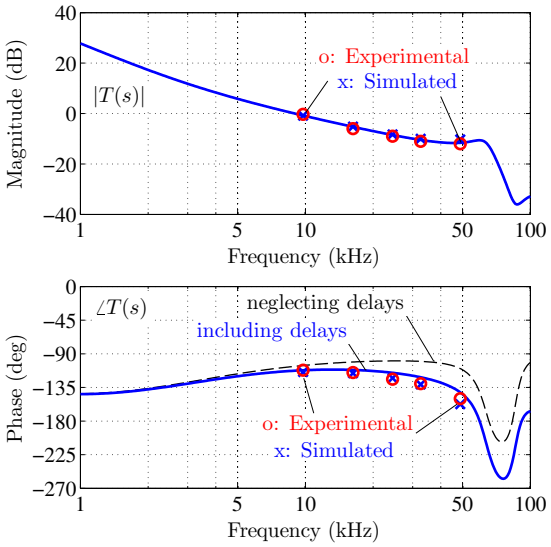


Figure 7.11: Experimental, simulated and theoretical loop gain $T(s)$ of the case study converter of Fig. 7.4; trailing-edge phase shift modulation.

of degrees. In all cases, sampling of the output voltage is executed at the beginning of the switching interval, so that $t_{cntrl} = 0$ and $t_d = t_{PSM}$. Clearly, this choice for the sampling strategy entails reserving a small initial portion of each switching cycle to A/D acquisition, control and Σ-Δ calculations. Denote with $G_c(s)$ the PI compensator transfer function,

$$G_c(s) \triangleq K_p + \frac{K_s}{s}. \tag{7.26}$$

Since $t_d = t_{PSM}$, the theoretical $T(s)$ is

$$\begin{aligned} T(s) &= G_c(s)G_{v\varphi}(s)G_{PSM}(s) \\ &\approx G_c(s)G_{v\varphi}(s)e^{-st_{PSM}}, \end{aligned} \tag{7.27}$$

where the amplitude attenuation term in $G_{PSM}(s)$ is approximated to unity in the last expression. The converter is tested at $I_{load} = 1$ A output current.

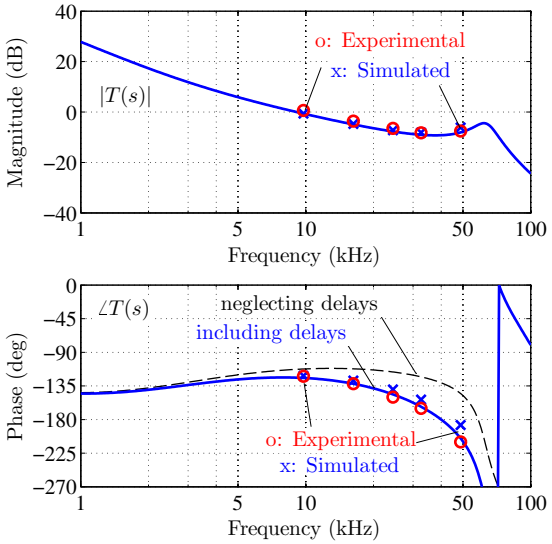


Figure 7.12: Experimental, simulated and theoretical loop gain $T(s)$ of the case study converter of Fig. 7.4; leading-edge phase shift modulation.

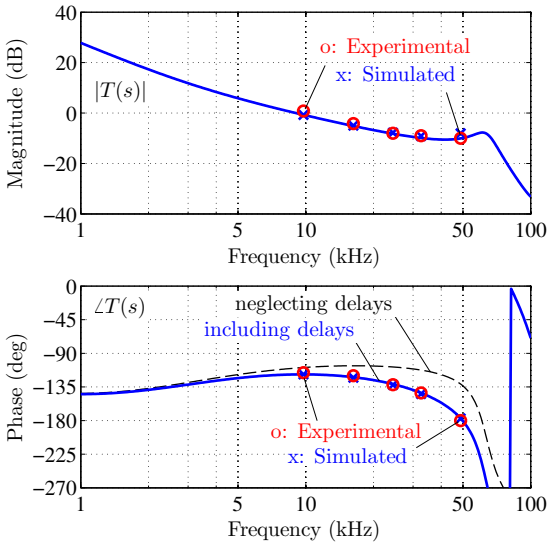


Figure 7.13: Experimental, simulated and theoretical loop gain $T(s)$ of the case study converter of Fig. 7.4; symmetrical phase shift modulation.

Since $\Phi \approx 33°$, one has

$$\begin{aligned} t_{PSM,TE} &= \frac{1}{\omega_s}\left(\Phi + \frac{\pi}{2}\right) \approx 1.76\ \mu\text{s}, \\ t_{PSM,LE} &= \frac{1}{\omega_s}\left(\frac{3}{2}\pi - \Phi\right) \approx 3.36\ \mu\text{s}, \\ t_{PSM,Sym} &= \frac{\pi}{\omega_s} = \frac{T_s}{2} \approx 2.56\ \mu\text{s}. \end{aligned} \tag{7.28}$$

for the trailing-edge, leading-edge and symmetrical modulator types respectively. Fig. 7.11, 7.12 and 7.13 report the Bode diagrams of the loop gain $T(s)$ with the three different types of phase shift modulation. The theoretical expression (7.27) is compared with both simulated and experimental points taken at different frequencies. In both experiments and simulations, the loop gain is extracted using Middlebrook's injection technique by superimposing a square-wave perturbation of small amplitude to the digital phase control command $u_\varphi[k]$ [55]. Successively, signals before and after the injection point are post-processed with a DFT-based analysis, and their spectral components at the perturbation frequency extracted in order to calculate the experimental loop gain in amplitude and phase. In the figures, the simplified loop gain without any modulation or control delay is also illustrated. The importance of such delays, and in particular of the phase shift modulator dynamics, is especially evident in the phase response. On the other hand, the extended model (7.27) based on the theory disclosed in this work correctly captures the loop dynamics over a wide range of frequencies.

Chapter 8

Small-signal analysis of combined phase shift and pulse width modulators

Contents

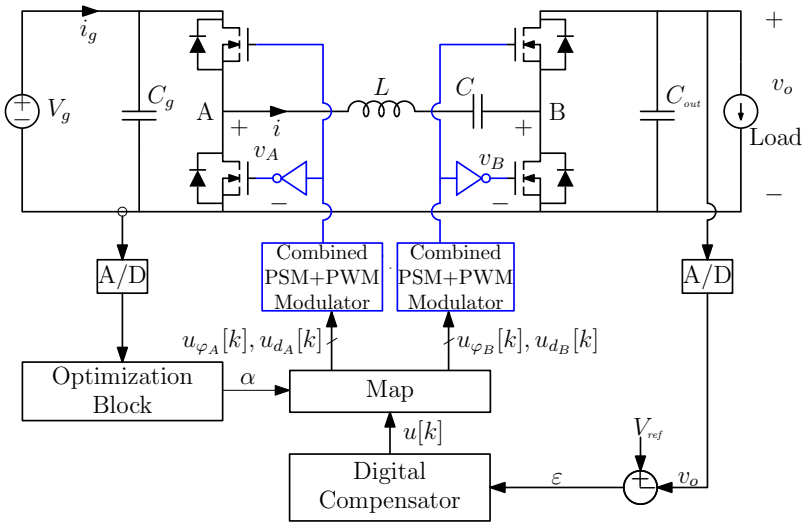


Figure 8.1: Digital dual half-bridge series resonant converter employing a combined PSM+PWM modulation.

8.1 Introduction

In chapter 7 the most commonly used phase shift modulators have been characterized from a dynamic standpoint. The AC analysis is made for *pure* phase shift modulations and results indicate, as main effect, the presence of a transport delay in close analogy with the theory of uniformly sampled pulse width modulators [55]. Such delay depends on the modulator carrier type as well as on the converter operating point. However, control techniques such as those described in chapters 4, 5 and in [6, 29, 49, 52] aim to exploit additional degrees of freedom offered by these topologies for efficiency optimization purposes. Such systems include combination of phase shift and pulse width modulation as part of a feedback loop capable of dynamically tracking the converter maximum efficiency point. Their adoption in a closed-loop system, on the other hand, is often complicated by the need to model and quantify the dynamical effects of the many degrees of freedom involved.

An example in which a combined uniformly sampled phase shift and pulse

width (PSM+PWM) modulation is employed is depicted in Fig. 8.1. The output voltage is sensed on a clock cycle basis by an ADC. The measured voltage is then compared with a reference and the error is processed by a digital compensator. The output of the regulator is then converted into a phase shift and duty cycle commands through a map. In such online efficiency optimization system, the parameters of the map is slowly tuned by an optimization block which adjusts α using a minimum input current tracking algorithm.

The analysis disclosed in this chapter is motivated by the need to understand the small-signal dynamical behavior of a power converter when subject to a generic digital PSM+PWM modulation. First objective of this chapter is then to extend the concepts already presented in chapter 7 to the case of combined uniformly sampled PSM+PWM and around a generic phase/duty cycle operating point. Furthermore, the analysis is developed for the generic harmonic of the switching frequency, therefore including the baseband dynamics as a special case. While this chapter focuses on the dynamics of the combined PSM+PWM modulator proper, the results are subsequently employed in chapter 9 to construct an extended multi-harmonic dynamic model of a digitally controlled series resonant dc-dc converter.

8.2 Combined Phase Shift and Pulse Width Uniformly Sampled Modulator

The modulation scheme treated throughout this chapter is depicted in Fig. 8.2. The inputs of the modulator are the phase reference u_φ and the duty cycle reference u_d. These discrete-time control signals are periodically updated every $T_{\text{sample}} = T_s$ seconds.

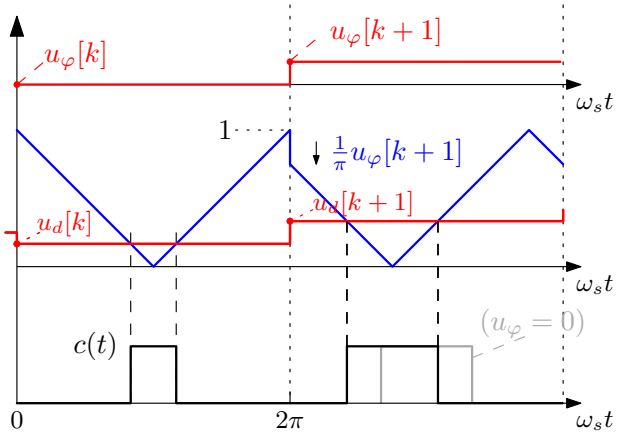


Figure 8.2: Combined PSM+PWM uniformly sampled modulation scheme.

As seen in Fig. 8.2, the modulating signal u_d produces the desired duty cycle by comparison with a symmetrical carrier. However, differently from a pure PWM modulator, the carrier initial value is reduced by a quantity proportional to the phase command u_φ. Starting from such value, the carrier bounces off the 0 and 1 boundaries before returning to the initial value after one entire switching period. This mechanism allows to generate the desired phase shift in the produced pulse. In this chapter, u_φ has the meaning of a *leading* angle, i.e. a positive value of u_φ anticipates the pulse relative to its position at $u_\varphi = 0$. The symmetrical triangular carrier is chosen to make the phase shift and the duty cycle references independent of each other in steady state: a static variation of the phase shift reference u_φ does not influence the value of the duty cycle; in a similar way, static variations of the duty cycle reference u_d do not modify the initial phase of the harmonics composing the modulated signal $c(t)$, but only their amplitude. According to Fig. 8.2, as

long as $u_d[k] < 1 - \frac{1}{\pi}u_\varphi[k]$, the modulator output signal $c(t)$ can be written as

$$c(t) = \begin{cases} 0, & kT_s < t < t_1[k] \\ 1, & t_1[k] < t < t_2[k] \\ 0, & t_2[k] < t < (k+1)T_s \end{cases} \tag{8.1}$$

where

$$\begin{cases} t_1[k] = kT_s + \frac{T_s}{2}\left(1 - \frac{u_\varphi[k]}{\pi} - u_d[k]\right) \\ t_2[k] = kT_s + \frac{T_s}{2}\left(1 - \frac{u_\varphi[k]}{\pi} + u_d[k]\right) \end{cases}. \tag{8.2}$$

In steady state, $u_d[k] = D$ and $u_\varphi[k] = \Phi$ so $c(t)$ is composed by its average value $C_0 = D$ plus harmonics

$$c(t) = \sum_{l=1}^{+\infty} c^{(l)}(t) + D, \tag{8.3}$$

with

$$c^{(l)}(t) \triangleq \frac{2}{l\pi}\sin(l\pi D)\cos[l\omega_s t - l(\pi - \Phi)]. \tag{8.4}$$

When, on the other hand, $u_d[k] > 1 - \frac{1}{\pi}u_\varphi[k]$, the output sequence is

$$c(t) = \begin{cases} 1, & kT_s < t < t_1'[k] \\ 0, & t_1'[k] < t < t_2'[k] \\ 1, & t_2'[k] < t < (k+1)T_s \end{cases}, \tag{8.5}$$

where

$$\begin{cases} t_1'(k) = kT_s + \frac{T_s}{2}\left(1 - \frac{u_\varphi[k]}{\pi} + u_d[k]\right) \\ t_2'(k) = kT_s + \frac{T_s}{2}\left(3 - \frac{u_\varphi[k]}{\pi} - u_d[k]\right) \end{cases}. \tag{8.6}$$

Since the methodology to derive the model of the modulator is the same for

both the cases, only the case defined by (8.1) and (8.2) are considered in the following. The resulting small-signal models are therefore valid in the neighborhood of any operating point (D, Φ) satisfying the constraint

$$D < 1 - \frac{\Phi}{\pi}. \tag{8.7}$$

The traditional phasor technique is normally used in the analysis of circuits and systems operating in sinusoidal steady state. By extension, periodic steady state operation of nonlinear systems can also be described by associating a phasor to each harmonic. For instance, the l-th harmonic (8.4) of the steady state PSM+PWM signal $c(t)$ can be represented by the phasor

$$\vec{C}^{(l)} = \frac{2}{l\pi} \sin(l\pi D) e^{-jl(\pi-\Phi)}, \tag{8.8}$$

which is valid when $u_d = D$ and $u_\varphi = \Phi$.

8.3 Modulator Small-Signal Analysis

The concepts of dynamic phasor described in section 6.2 can be applied harmonic by harmonic to the PSM+PWM signal $c(t)$ when modulating signals u_d and u_φ are slightly perturbed around their steady state operating points. A dynamic phasor

$$\vec{\boldsymbol{c}}^{(l)}(t) \approx \vec{C}^{(l)} \left(1 + \frac{\hat{a}^{(l)}(t)}{|\vec{C}^{(l)}|} + j\hat{\varphi}^{(l)}(t) \right) \tag{8.9}$$

can be associated to the l-th harmonic of $c(t)$. Fig. 8.3 illustrates the above decomposition for the fundamental harmonic phasor $\vec{c}^{(1)}(t)$. Goal of the following sections is to study the dynamic small-signal relationship between

$\vec{c}^{(l)}(t)$ and the modulating signals u_d and u_φ.

8.3.1 Phasor Dynamics due to Pulse Width Modulation

Consider the modulation scheme of Fig. 8.2 with a constant phase control signal $u_\varphi[k] = \Phi$, and assume that the duty cycle control signal consists of a DC term D plus a small discrete time sinusoidal perturbation with rate ω_m,

$$u_d[k] = D + \hat{u}_d \sin(\omega_m k T_s). \tag{8.10}$$

As done in section 7.2 for the case of pure phase shift modulation, it is assumed that the modulation and sampling frequencies are commensurable,

$$\frac{\omega_m}{\omega_s} = \frac{L}{N}, \quad L, N \in \mathbb{N} \tag{8.11}$$

with the sole objective of simplifying calculations by allowing the use of Fourier series rather than double integrals. The conclusions that will be drawn are not affected by such hypothesis. The goal of this section is to derive the effect generated by a perturbation of the duty cycle $\hat{u}_d$ on the amplitude and phase of the dynamic phasor $\vec{c}^{(l)}(t)$. Let us start with the evaluation of the spectrum of $c(t)$ at the frequency rate $\omega = \omega_{lq} = l\omega_s + q\omega_m$, $l, q \in \mathbb{Z}$,

$$\begin{aligned} c(\omega = \omega_{lq}) &= \frac{1}{T}\int_0^T c(\tau) e^{-j\tau\omega_{lq}} d\tau \\ &= \frac{2}{T}\frac{e^{-j\omega_{lq}\frac{T_s}{2}\left(1-\frac{\Phi}{\pi}\right)}}{\omega_{lq}} \sum_{k=0}^{N-1} e^{-j\omega_{lq}kT_s} \sin\left(\omega_{lq} u_d[k] \frac{T_s}{2}\right) \end{aligned} \tag{8.12}$$

where the time interval $[0, T]$ contains N switching periods and L modulation periods. Note that when evaluated at $\omega = l\omega_s$, equation (8.12) returns the phasors defined in (8.8). The upper side band $c^{(l)}_{\text{usb}}(\omega_m)$ and the lower side band $c^{(l)}_{\text{lsb}}(\omega_m)$ are calculated, in the limit that $\hat{u}_d$ is small, from (8.10) and (8.12) by imposing $q = +1$ and $q = -1$ respectively

$$c^{(l)}_{\text{usb}}(\omega_m) = -j \cos\left((l\omega_s + \omega_m) D \frac{T_s}{2}\right) e^{-j(l\omega_s+\omega_m)\frac{T_s}{2}\left(1-\frac{\Phi}{\pi}\right)} \hat{u}_d \tag{8.13}$$

$$c^{(l)}_{\text{lsb}}(\omega_m) = j \cos\left((l\omega_s - \omega_m) D \frac{T_s}{2}\right) e^{-j(l\omega_s-\omega_m)\frac{T_s}{2}\left(1-\frac{\Phi}{\pi}\right)} \hat{u}_d. \tag{8.14}$$

Going back to the time domain, the dynamic phasor $\vec{c}^{(l)}(t)$ can be calculated from (8.13) and (8.14)

$$\vec{c}^{(l)}(t) = \vec{C}^{(l)} + c^{(l)}_{\text{usb}}(\omega_m) e^{j\omega_m t} + c^{(l)}_{\text{lsb}}(\omega_m) e^{-j\omega_m t} \tag{8.15}$$

Notice that, when evaluated at the baseband ($l = 0$), (8.13) and (8.14) yield a couple of hermitian conjugate spectral lines, as expected. In the time domain, this corresponds to a real-valued signal. For $l \neq 0$, on the other hand, the time-domain counterpart of these two spectral lines is the complex-valued phasor $\vec{c}^{(l)}(t)$. Equation (8.15) can be easily rearranged in the form (8.9), with

$$\hat{a}^{(l)}(t) = 2 \cos(l\pi D) \cos\left(\omega_m D \frac{T_s}{2}\right) \sin\left[\omega_m (t - t_d)\right] \hat{u}_d \tag{8.16}$$

$$\hat{\varphi}^{(l)}(t) = -l\pi \sin\left(\omega_m D \frac{T_s}{2}\right) \cos\left[\omega_m (t - t_d)\right] \hat{u}_d \tag{8.17}$$

where

$$t_d = \frac{T_s}{2}\left(1 - \frac{\Phi}{\pi}\right). \tag{8.18}$$

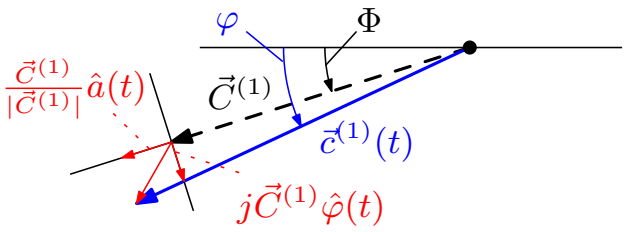


Figure 8.3: Phasor representation of an amplitude and phase perturbation of the dynamic phasor $\vec{c}^{(1)}(t)$

As expected, both amplitude and phase perturbations $\hat{a}^{(l)}(t)$ and $\hat{\varphi}^{(l)}(t)$ depend on the modulator operating point (D, Φ). Furthermore, expressions (8.16) and (8.17) show that a perturbation $\hat{u}_d$ of the duty cycle command $u_d[k]$ produce

i) an amplitude perturbation $\hat{a}^{(l)}(t)$ at the modulator output $c(t)$. Such perturbation acts with a transport delay (8.18) with respect to the sampling instant. As secondary effect, there is a small attenuation depending on the modulating frequency ω_m through the term $\cos\left(\omega_m D\frac{T_s}{2}\right)$;

ii) a "parasitic" phase perturbation $\hat{\varphi}^{(l)}(t)$ oscillating in quadrature with respect to $\hat{a}^{(l)}(t)$ and still delayed by t_d. It worth to note that

$$\lim_{\omega_m \to 0} \hat{\varphi}^{(l)}(t) = 0 \tag{8.19}$$

according to the fact that, for symmetrical carrier duty cycle modulators, a variation of the duty cycle does not affect the initial phase of harmonics of $c(t)$ *in steady state*.

8.3.2 Phasor Dynamics due to Phase Shift Modulation

To deduce the dynamics introduced by a phase shift perturbation it is possible to follow the procedure explained in section 8.3.1 for the duty cycle case.

In this case, assume a constant $u_d[k] = D$, and consider $u_\varphi[k]$ as a superposition of a dc term Φ plus a small discrete time sinusoidal perturbation with rate ω_m

$$u_\varphi[k] = \Phi + \hat{u}_\varphi \sin(\omega_m k T_s). \tag{8.20}$$

The spectrum of $c(t)$ calculated for $\omega_{lq} = l\omega_s \pm q\omega_m$ is

$$\begin{aligned} c(\omega = \omega_{lq}) &= \frac{1}{T}\int_0^T c(\tau) e^{-j\tau\omega_{lq}} d\tau \\ &= \frac{2}{T}\frac{e^{-j\omega_{lq}\frac{T_s}{2}}}{\omega_{lq}} \sin\left(\omega_{lq}\frac{D}{2}T_s\right) \sum_{k=0}^{N-1} e^{-j\omega_{lq}\left(kT_s - u_\varphi[k]\frac{T_s}{2\pi}\right)}. \end{aligned} \tag{8.21}$$

In the limit that $\hat{u}_\varphi$ is small, the upper side band $c^{(l)}_{\text{usb}}(\omega_m)$ and the lower side band $c^{(l)}_{\text{lsb}}(\omega_m)$ are

$$c^{(l)}_{\text{usb}}(\omega_m) = \frac{\hat{u}_\varphi}{2\pi} \sin\left((l\omega_s + \omega_m)\frac{D}{2}T_s\right) e^{-j(l\omega_s+\omega_m)\frac{T_s}{2}\left(1-\frac{\Phi}{\pi}\right)} \tag{8.22}$$

$$c^{(l)}_{\text{lsb}}(\omega_m) = -\frac{\hat{u}_\varphi}{2\pi} \sin\left((l\omega_s - \omega_m)\frac{D}{2}T_s\right) e^{-j(l\omega_s-\omega_m)\frac{T_s}{2}\left(1-\frac{\Phi}{\pi}\right)}. \tag{8.23}$$

Then, using (8.15), the signal composed by (8.22) and (8.23) can be brought back to the time domain. When written in the form (8.9), result is

$$\hat{\varphi}^{(l)}(t) = l\cos\left(\omega_m D\frac{T_s}{2}\right) \sin\left[\omega_m(t - t_d)\right]\hat{u}_\varphi \tag{8.24}$$

$$\hat{a}^{(l)}(t) = \frac{2}{\pi}\cos(l\pi D) \sin\left(\omega_m D\frac{T_s}{2}\right) \cos\left[\omega_m(t - t_d)\right]\hat{u}_\varphi. \tag{8.25}$$

Once again, both these terms depend on the modulator operating point (D, Φ). Similarly to the case of a duty cycle perturbation, when the phase shift modulating signal is perturbed with a small discrete time sinusoidal signal, the following terms appear in the dynamic phasor $\vec{c}^{(l)}(t)$:

i) a phase perturbation $\hat{\varphi}^{(l)}(t)$ acting with a transport delay equal to the delay (8.18) introduced by the pulse width modulation. As a secondary effect, there is a small attenuation depending on the modulating frequency ω_m through the term $\cos\left(\omega_m D\frac{T_s}{2}\right)$;

ii) a "parasitic" amplitude perturbation $\hat{a}^{(l)}(t)$ oscillating in quadrature with respect to $\hat{\varphi}^{(l)}(t)$. It worth to note that

$$\lim_{\omega_m \to 0} \hat{a}^{(l)}(t) = 0 \tag{8.26}$$

according to the fact that, a variation of the phase shift does not affect the amplitude of harmonics of $c(t)$ *in steady state*.

8.3.3 Modulator Frequency Response

Small-signal relations expressed in time domain calculated in sec 8.3.1 and 8.3.2 indicate how a discrete time sinusoidal perturbation at the input of the modulator reflect to the output. These relations can be written in a more convenient frequency-domain form. To this purpose, define

$$G^{(l)}_{u_d \to a}(s) \triangleq \frac{\hat{a}^{(l)}(s)}{\hat{u}_d(s)} \tag{8.27}$$

which relates the small-signal variations of $\hat{u}_d$ to the corresponding perturbations of $\hat{a}^{(l)}(t)$. Using the same notation we define the transfer functions $G^{(l)}_{u_d \to \varphi}(s)$, $G^{(l)}_{u_\varphi \to a}(s)$ and $G^{(l)}_{u_\varphi \to \varphi}(s)$. The frequency responses can be derived

by the time domain equations (8.16), (8.17), (8.25) and (8.24), yielding

$$\begin{cases} G^{(l)}_{u_d\to a}(j\omega) = 2\cos(l\pi D)\cos\left(\omega D\frac{T_s}{2}\right)e^{-j\omega t_d} \\ G^{(l)}_{u_d\to \varphi}(j\omega) = jl\pi\sin\left(\omega D\frac{T_s}{2}\right)e^{-j\omega t_d} \\ G^{(l)}_{u_\varphi\to \varphi}(j\omega) = l\cos\left(\omega D\frac{T_s}{2}\right)e^{-j\omega t_d} \\ G^{(l)}_{u_\varphi\to a}(j\omega) = j\frac{2}{\pi}\cos(l\pi D)\sin\left(\omega D\frac{T_s}{2}\right)e^{-j\omega t_d} \end{cases} \tag{8.28}$$

As explained above for the time domain expressions, transfer functions $G^{(l)}_{u_d\to a}(s)$ and $G^{(l)}_{u_\varphi\to\varphi}(s)$ indicate, as major effect, a common transport delay depending on the steady state value of the phase modulating signal. As secondary effect there is a small attenuation term negligible at low frequencies. Although the modulator of Fig. 8.2 is designed to make the duty cycle and the phase shift independent in steady state, in the dynamical case cross-coupling effects are produced, described by transfer functions $G^{(l)}_{u_d\to\varphi}(s)$ and $G^{(l)}_{u_\varphi\to a}(s)$. The above analysis indicates that such cross-coupling effects are of derivative nature, since both $G^{(l)}_{u_d\to\varphi}(j\omega)$ and $G^{(l)}_{u_\varphi\to a}(j\omega)$ have a low-frequency asymptotic expression of the type

$$G^{(l)}_{u_d\to\varphi}(j\omega) \overset{low\ freq}{\propto} j\omega e^{-j\omega t_d} \tag{8.29}$$

and

$$G^{(l)}_{u_\varphi\to a}(j\omega) \overset{low\ freq}{\propto} j\omega e^{-j\omega t_d}. \tag{8.30}$$

As a final remark on (8.28), these can also be employed, in the formal limit as $l \to 0$, to describe the baseband dynamics. In this limit, one can see that both $G^{(l)}_{u_d\to\varphi}(j\omega)$ and $G^{(l)}_{u_\varphi\to\varphi}(j\omega)$ vanish, as no phase dynamics is present in the baseband. As for $G^{(l)}_{u_d\to a}(j\omega)$ and $G^{(l)}_{u_\varphi\to a}(j\omega)$, their limit as $l \to 0$

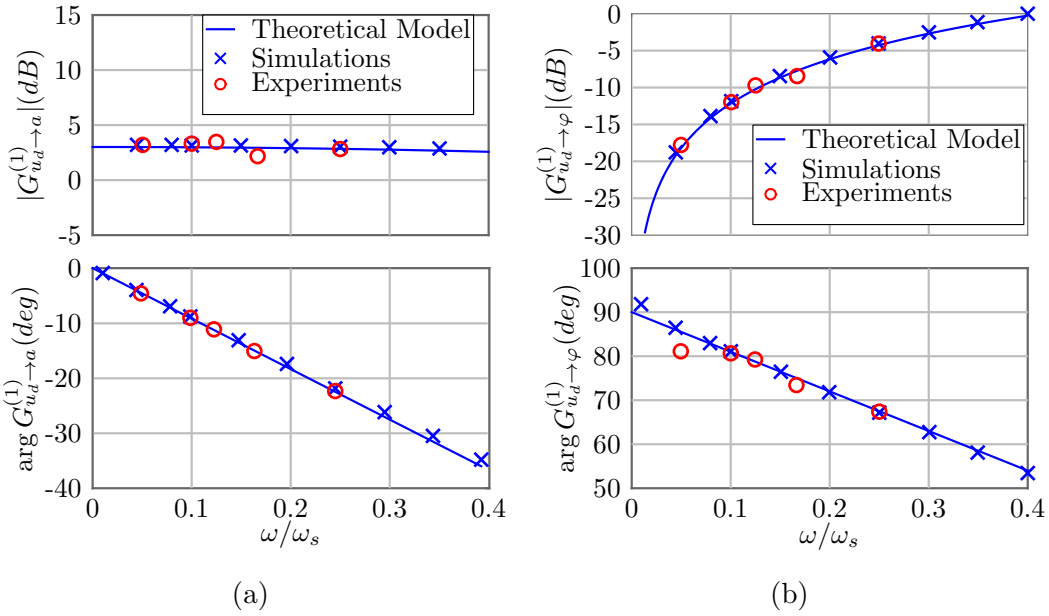


Figure 8.4: Theoretical, simulated and experimental frequency response (a) $G_{u_d\to a}$, (b) $G_{u_d\to\varphi}$ relative to the switching frequency harmonic $l = 1$. Operating point is $(D = 0.25, \Phi = 90°)$.

yields the average dynamics of $c(t)$ when subject to both duty cycle and phase modulation. Observe that a factor of 2 appears as a multiplier in both transfer functions because of the way dynamic phasors have been defined in this work.

8.4 Simulation and Experimental Results

For experimental testing, the digital modulator of Fig. 8.2 is implemented on an Altera® commercial FPGA development board. The modulator frequency is 50 kHz; its resolution is equal to 10 bits, which amounts to a phase angle resolution of 0.3° and duty cycle resolution of 0.2%.

A sinusoidal perturbation, either of the duty cycle command or of the phase command, is digitally superimposed to the modulating signal, the

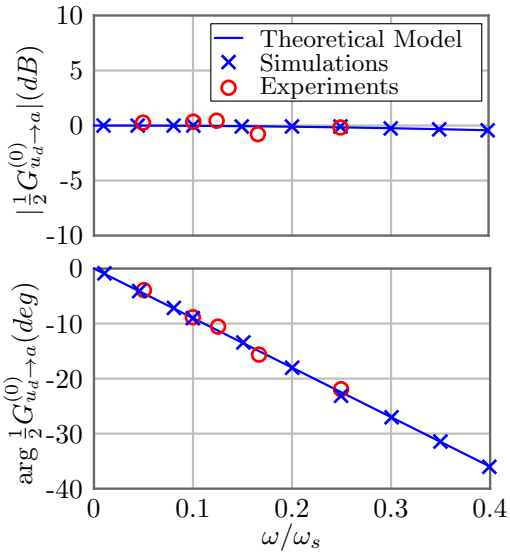


Figure 8.5: Theoretical, simulated and experimental frequency response $\frac{1}{2}G_{u_d\to a}$ relative to the baseband dynamics $l = 0$. Operating point is ($D = 0.25, \Phi = 90°$).

modulated waveform successively acquired using a high frequency oscilloscope with sampled frequency of 1 GSPS and an observation window of 5 ms. A square wave signal in phase with the perturbation is also acquired as time reference. Samples are then post-processed with a Discrete Fourier Transform-based analysis in order to extract the spectrum of the signals and analyze the relevant harmonics. This procedure is iterated for several values of the modulating perturbation frequency ω_m. Also, three harmonics were examined in the experimental testing, namely the switching harmonic $l = 1$, the baseband harmonic $l = 0$ and the second harmonic $l = 2$.

Results obtained with a duty cycle perturbation are shown in Fig. 8.4a and 8.4b relative to the fundamental harmonic $l = 1$. The experimental operating point is ($D = 0.25$, $\Phi = 90°$) and the amplitude of the duty cycle perturbation is 1%. Results for the baseband case $l = 0$ and the same operating point are shown in Fig. 8.5. Notice that since this case represents the average dynamics,

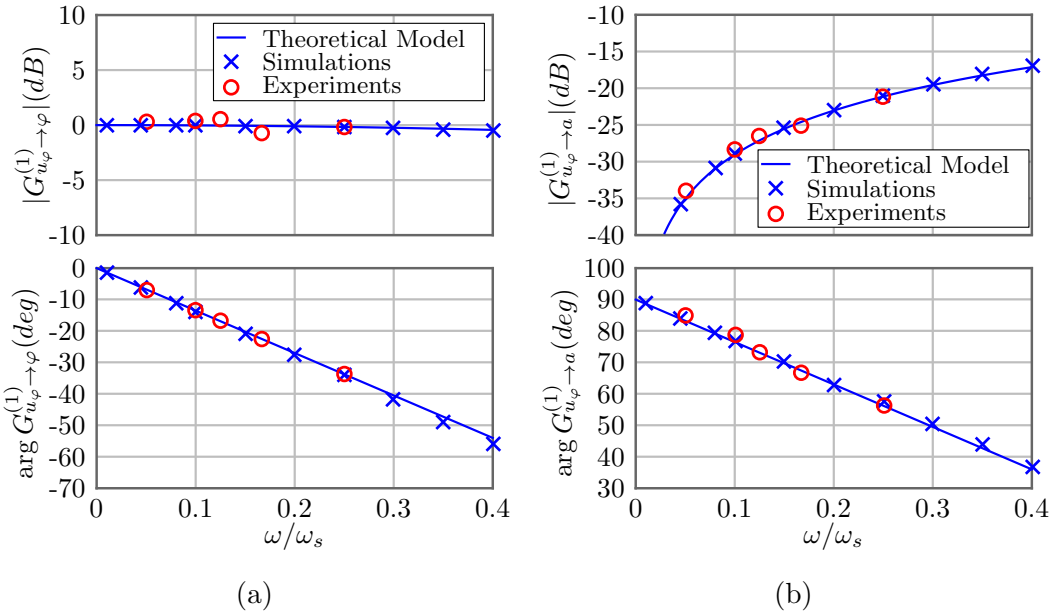


Figure 8.6: Theoretical, simulated and experimental frequency response of (a) $G_{u_\varphi\to\varphi}$, (b) $G_{u_\varphi\to a}$ relative to the switching frequency harmonic $l = 1$. Operating point is $(D = 0.25, \Phi = 45°)$.

the transfer function $G^{(0)}_{u_d\to\varphi}(j\omega)$ is equal to zero and not shown.

Results obtained with a phase shift perturbation and for $l = 1$ are shown in Fig. 8.6b and 8.6a. In this case the experimental operating point is $(D = 0.25,\ \Phi = 45°)$ and the phase angle perturbation amplitude is about 1.75°. Results for the baseband case ($l = 0$) are shown in Fig. 8.7. As for the case of the duty cycle perturbation the transfer function $G^{(0)}_{u_\varphi\to\varphi}(j\omega)$ is zero and therefore not shown. As anticipated, the modulator introduces a high-frequency cross-coupling effect in average dynamics as well.

To conclude, the case of the second harmonic $l = 2$ is shown as well and results are shown in Fig. 8.8a and 8.8b. In this operating point one has $\cos(2\pi D) = 0$, and the transfer function $G^{(2)}_{u_\varphi\to a}(j\omega)$ vanishes. Plotted markers in Fig. 8.8b only represent the measured noise.

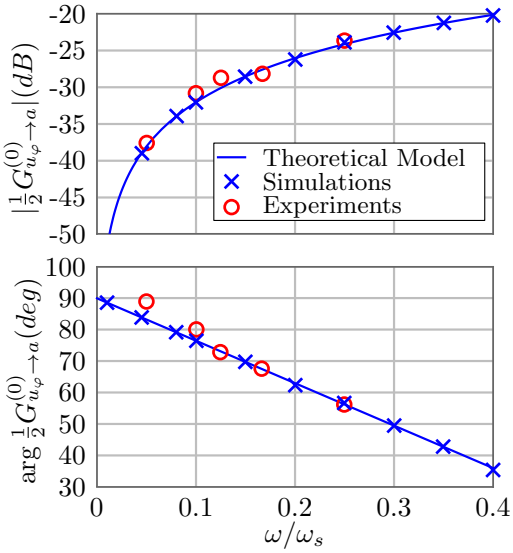
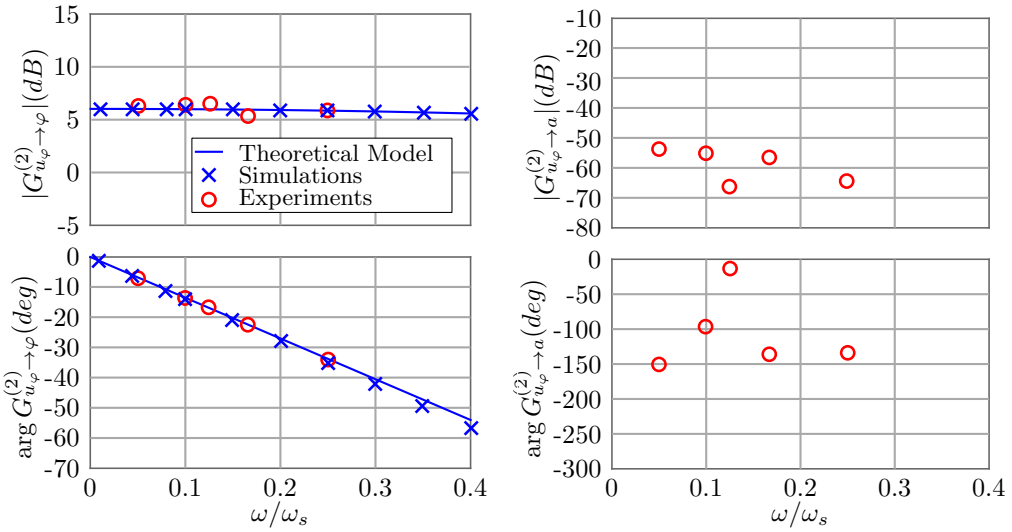


Figure 8.7: Theoretical, simulated and experimental frequency response $\frac{1}{2}G_{u_\varphi \to a}$ relative to the baseband dynamics $l = 0$. Operating point is $(D = 0.25, \Phi = 45°)$.



(a) (b)

Figure 8.8: Theoretical, simulated and experimental frequency response of (a) $G_{u_\varphi \to \varphi}$ (b) $G_{u_\varphi \to a}$ relative to the second harmonic $l = 2$. Operating point is $(D = 0.25, \Phi = 45°)$.

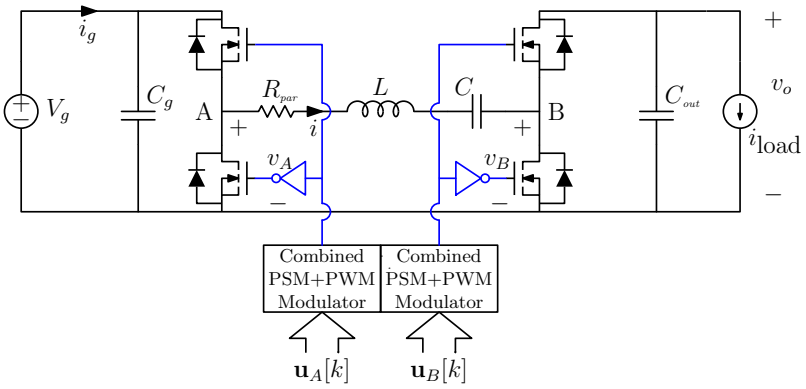
Chapter 9

Dynamic analysis of a digitally controlled DHB-SRC

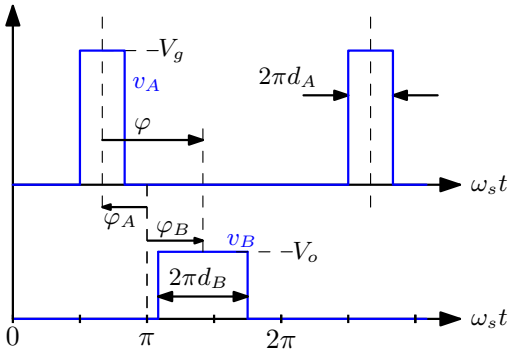
Contents

9.1 Introduction

Dual half-bridge or full-bridge dc-dc resonant converters operating at constant switching frequency are often controlled by varying the phase shift between



(a)



(b)

Figure 9.1: (a) Multi-variable controlled resonant converter with combined phase shift and pulse width uniformly sampled modulation and (b) voltage waveforms $v_A(t)$ and $v_B(t)$ in a generic operating point.

the driving signals of the input and output legs. As shown in chapter 4, such single-variable control approaches typically have the disadvantage of a degraded efficiency, especially in light load conditions. In section 6.3.1 it has been shown how the dynamics of phase-controlled converters is usually studied according to the dynamic phasor approach [41–44, 48], in which the tank response in the vicinity of the switching frequency is described in terms of voltage and current phasors.

Adoption of efficiency optimization approaches in a closed-loop feedback

system, however, poses the general problem of dynamic analysis of the power converter when two or more control variables are employed for regulation purposes. Furthermore, a correct dynamical modeling of a multi-variable-controlled converter is mandatory for the design and implementation of *online* efficiency optimization techniques as those presented in chapters 4. Moving from these considerations, this section analyzes the small-signal dynamic response of dc-dc series resonant converters when subject to a combined phase shift and pulse width modulation (PSM+PWM), i.e. when the converter legs are modulated by both adjusting their duty cycle and their mutual phase shift. Fig. 9.1a exemplifies the general scenario considered in this paper, where each leg of the converter is driven by a PSM+PWM modulator. Voltage waveforms $v_A(t)$ and $v_B(t)$ produced by each leg are illustrated in Fig. 9.1b for an arbitrary operating point. Starting from the results presented in chapter 8 on the dynamics introduced by a combined PSM+PWM uniformly sampled modulator in both the baseband region and in the vicinity of the generic switching harmonic, this chapter formulates an extended model valid for the converter system of Fig. 9.1a. The approach followed in this chapter to obtain the small-signal circuit of the DHB-SRC is similar to the one shown in section 6.3.1.

9.2 Multi-variable controller case study

Consider the block diagram of Fig. 9.1a. Each leg of the converter is driven by a PSM+PWM uniformly sampled modulator. Vectors $\mathbf{u}_x[k] = [u_{d_x}[k], u_{\varphi_x}[k]]$, where x is the generic leg ($x \in \{A, B\}$), represent the modulating signals. Elements of $\mathbf{u}_x[k]$ are the references of duty cycle and phase shift of leg A and leg B as defined in Fig. 9.1b. Note that, according to Fig. 9.1b, the phase

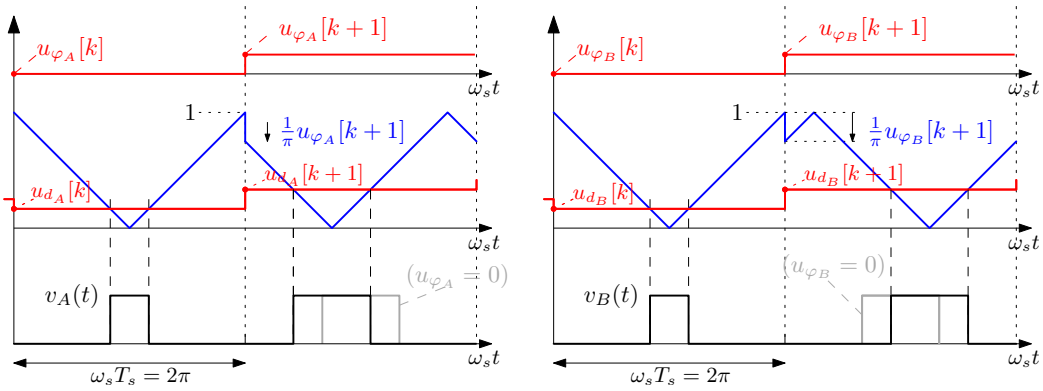


Figure 9.2: General PSM+PWM modulation scheme for the dc-dc resonant converter illustrated in Fig. 9.1a.

shift φ is defined as the phase difference between fundamental harmonics of $v_A(t)$ and $v_B(t)$. The modulation schemes for leg A and leg B are reported in Fig. 9.2 and follow the PSM+PWM approach described in chapter 8. For the modulators of Fig. 9.2, $u_{\varphi_B}[k]$ has the effect of delaying $v_B(t)$ with respect to its position for $u_{\varphi_B} = 0$, while a positive value of $u_{\varphi_A}[k]$ acts as to anticipate $v_A(t)$ with respect to its position for $u_{\varphi_A} = 0$. Vectors $\mathbf{u}_x[k]$ are updated periodically with a sampling period $T_{\text{sample}} = T_s$, where T_s is the switching period. The carrier is a symmetrical triangle wave, a choice which allows to set the duty cycle and phase shift independently of each other in steady-state condition. The modulators work as a traditional PWM modulator except for the fact that the initial value of the carrier is updated to perform the phase shift modulation. In steady state, and following the modulation schemes defined in Fig. 9.2, the l-th harmonic of $v_A(t)$ and $v_B(t)$ can be represented by the complex phasors

$$\begin{cases} \vec{V}_A^{(l)} = \dfrac{2}{l\pi} V_g \sin(l\pi D_A) e^{-jl(\pi - \Phi_A)} \\ \\ \vec{V}_B^{(l)} = \dfrac{2}{l\pi} V_o \sin(l\pi D_B) e^{-jl(\pi + \Phi_B)} \end{cases} . \tag{9.1}$$

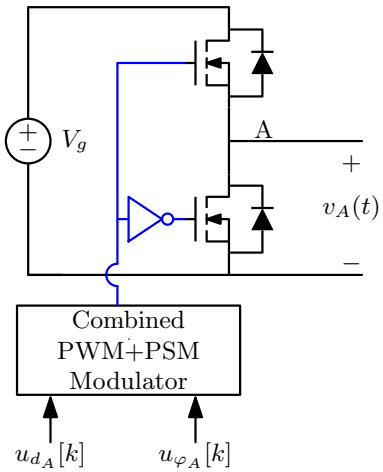


Figure 9.3: Block diagram of leg A

9.3 Multi-Harmonic Small-Signal Model

9.3.1 Modulator phasor dynamics

Consider the leg A of Fig. 9.3 driven by the uniformly sampled combined phase shift and pulse width modulator with modulation scheme of Fig. 9.2. In chapter 8 it is shown that a small discrete time sinusoidal perturbation of the duty cycle control signal

$$u_{d_A}[k] = D_A + \hat{u}_{d_A} \sin(\omega_m k T_s) \tag{9.2}$$

produces a baseband perturbation located at $\pm\omega_m$ as well as sidebands perturbation located at $l\omega_s \pm \omega_m$. Such spectrum is sketched in Fig. 9.4. Baseband perturbation can be treated using the traditional averaging small-signal modeling while the perturbation in the vicinity of multiple of switching frequency $l\omega_s$ can be embedded using the dynamic phasor modeling approach.

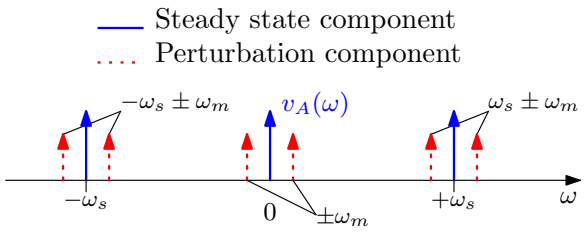


Figure 9.4: Spectrum of $v_A(t)$ in the small-signal limit.

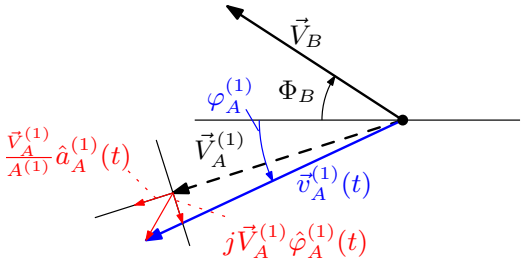


Figure 9.5: Small-signal components of dynamic phasor $\vec{v}_A^{(1)}(t)$ with amplitude and phase modulation.

The same spectrum is generated when the phase shift command is perturbed

$$u_{\varphi_A}[k] = \Phi_A + \hat{u}_{\varphi_A} \sin\left(\omega_m k T_s\right). \tag{9.3}$$

In chapter 8 it is shown that perturbations (9.2) and (9.3) individually affect both the amplitude $\hat{a}_A^{(l)}(t)$ and the phase $\hat{\varphi}_A^{(l)}(t)$ of the dynamic phasor $\vec{v}_A^{(l)}(t)$

$$\vec{v}_A^{(l)}(t) = \vec{V}_A^{(l)} + \hat{\vec{v}}_A^{(l)}(t) = \vec{V}_A^{(l)} \left(1 + \frac{\hat{a}_A^{(l)}(t)}{A^{(l)}} + j\hat{\varphi}_A^{(l)}(t)\right), \tag{9.4}$$

where $A^{(l)} = |\vec{V}_A^{(l)}|$. The vector representation is illustrated in Fig. 9.5 for the fundamental frequency $l = 1$. Frequency-domain expressions of $\hat{a}_A^{(l)}(t)$ and

$\hat{\varphi}_A^{(l)}(t)$ have been derived in closed form,

$$\begin{aligned}\hat{a}_A^{(l)}(\omega_m) = G^{(l)}_{u_{d_A}\to a}(j\omega_m)\hat{u}_{d_A} + G^{(l)}_{u_{d_A}\to\varphi}(j\omega_m)\hat{u}_{\varphi_A} = \\ \hat{u}_{d_A} 2\cos(l\pi D_A)\cos\left(\omega_m D_A\frac{T_s}{2}\right)e^{-j\omega_m t_{d,A}} + \\ j\hat{u}_{\varphi_A}\frac{2}{\pi}\cos(l\pi D_A)\sin\left(\omega_m D_A\frac{T_s}{2}\right)e^{-j\omega_m t_{d,A}}\end{aligned} \tag{9.5}$$

and

$$\begin{aligned}\hat{\varphi}_A^{(l)}(\omega_m) = G^{(l)}_{u_{\varphi_A}\to a}(j\omega_m)\hat{u}_{d_A} + G^{(l)}_{u_{\varphi_A}\to\varphi}(j\omega_m)\hat{u}_{\varphi_A} = \\ \hat{u}_{\varphi_A} l\cos\left(\omega_m D_A\frac{T_s}{2}\right)e^{-j\omega_m t_{d,A}} + \\ j\hat{u}_{d_A} l\pi\sin\left(\omega_m D_A\frac{T_s}{2}\right)e^{-j\omega_m t_{d,A}}.\end{aligned} \tag{9.6}$$

In both expressions, $t_{d,A}$ is defined as

$$t_{d,A} = \frac{T_s}{2}\left(1 - \frac{\Phi_A}{\pi}\right). \tag{9.7}$$

Equations (9.5) and (9.6) show that in analogy with the theory of uniformly sampled pulse width modulators, the sampled nature of the modulating signal introduces a small-signal transport delay $t_{d,A}$ in the transfer functions $G^{(l)}_{u_{d_A}\to a}(s)$ and $G^{(l)}_{u_{\varphi_A}\to\varphi}(s)$. Such delay depends on the steady state phase Φ_A. As a secondary effect, a small attenuation term is also seen in the magnitude response of the modulator. These results generalize dynamical effects of uniform sampling in pulse width and phase shift modulators already documented in [47].

The modulator also introduces a dynamic cross-coupling effect between phase and duty cycle commands through the transfer functions $G^{(l)}_{u_{d_A}\to\varphi}(s)$ and $G^{(l)}_{u_{\varphi_A}\to a}(s)$. Such cross-coupling effect vanishes at low frequencies. More

generally, the dynamic behavior of the cross-coupling is of derivative nature, since

$$G^{(l)}_{u_{d_A}\to\varphi}(j\omega_m) \overset{low\ freq}{\propto} j\omega_m e^{-j\omega_m t_{d,A}} \tag{9.8}$$

and

$$G^{(l)}_{u_{\varphi_A}\to a}(j\omega_m) \overset{low\ freq}{\propto} j\omega_m e^{-j\omega_m t_{d,A}}. \tag{9.9}$$

Therefore $G^{(l)}_{u_{d_A}\to a}(s)$ and $G^{(l)}_{u_{\varphi_A}\to\varphi}(s)$ represent a high-frequency effect introduced by the modulation.
Similarly, perturbation of control signals

$$u_{d_B}[k] = D_A + \hat{u}_{d_B}\sin(\omega_m k T_s) \tag{9.10}$$

and

$$u_{\varphi_B}[k] = \Phi_A + \hat{u}_{\varphi_B}\sin(\omega_m k T_s) \tag{9.11}$$

produce a perturbation of the dynamic phasor $\vec{v}^{(l)}_B(t)$

$$\vec{v}^{(l)}_B = \vec{V}^{(l)}_B + \hat{\vec{v}}^{(l)}_B = \vec{V}^{(l)}_B\left(1 + \frac{\hat{a}^{(l)}_B}{B^{(l)}} - j\hat{\varphi}^{(l)}_B\right) \tag{9.12}$$

where $B^{(l)} = |\vec{V}^{(l)}_B|$. Such perturbations in closed form are

$$\begin{aligned}\hat{a}^{(l)}_B = G^{(l)}_{u_{d_A}\to a}(j\omega_m)\hat{u}_{d_B} + G^{(l)}_{u_{d_B}\to\varphi}(j\omega_m)\hat{u}_{\varphi_B} = \\ \hat{u}_{d_B} 2\cos(l\pi D_B)\cos\left(\omega_m D_B\frac{T_s}{2}\right)e^{-j\omega_m t_{d,B}} + \\ j\hat{u}_{\varphi_B}\frac{2}{\pi}\cos(l\pi D_B)\sin\left(\omega_m D_B\frac{T_s}{2}\right)e^{-j\omega_m t_{d,B}}\end{aligned} \tag{9.13}$$

$$\begin{aligned}\hat{\varphi}_B^{(l)}(\omega_m) = G^{(l)}_{u_{\varphi_B}\to a}(j\omega_m)\hat{u}_{d_B} + G^{(l)}_{u_{\varphi_B}\to \varphi}(j\omega_m)\hat{u}_{\varphi_B} = \\ \hat{u}_{\varphi_B} l \cos\left(\omega_m D_B \frac{T_s}{2}\right) e^{-j\omega_m t_{d,B}} + \\ j\hat{u}_{d_B} l\pi \sin\left(\omega_m D_B \frac{T_s}{2}\right) e^{-j\omega_m t_{d,B}}\end{aligned} \tag{9.14}$$

with

$$t_{d,B} = \frac{T_s}{2}\left(1 + \frac{\Phi_B}{\pi}\right). \tag{9.15}$$

Equations (9.13) and (9.14) are identical to (9.5) and (9.6) except for the sign of steady state phase angle Φ_B, which in this case acts as a lagging angle rather than a leading angle.

9.3.2 Modulator baseband dynamics

The baseband dynamics induced by the modulator can be treated as a special case of phasor dynamics by studying the above results for $l = 0$. In this limit the dynamic phasors $\vec{v}_A^{(0)}(t)$ and $\vec{v}_B^{(0)}(t)$ become real-valued signals and there are no phase perturbations, i.e. $\hat{\varphi}_A^{(0)}(\omega_m) = 0$ and $\hat{\varphi}_B^{(0)}(\omega_m) = 0$. Furthermore, because of the choice adopted for defining dynamic phasors, the $l = 0$ steady-state phasor is two times the average value V_x of $v_x(t)$,

$$\begin{cases}\vec{V}_A^{(0)} = 2D_A V_g = 2V_A, \\ \vec{V}_B^{(0)} = 2D_B V_g = 2V_B.\end{cases} \tag{9.16}$$

More generally, the baseband dynamics $\bar{v}_A(t)$ and $\bar{v}_B(t)$ of the switching nodes are

$$\begin{cases}\bar{v}_A(t) = V_A + \hat{\bar{v}}_A = \frac{1}{2}\vec{v}_A^{(0)}(t) = V_A + \frac{1}{2}\hat{a}_A^{(0)}(t), \\ \bar{v}_B(t) = V_B + \hat{\bar{v}}_B = \frac{1}{2}\vec{v}_B^{(0)}(t) = V_B + \frac{1}{2}\hat{a}_B^{(0)}(t).\end{cases} \tag{9.17}$$

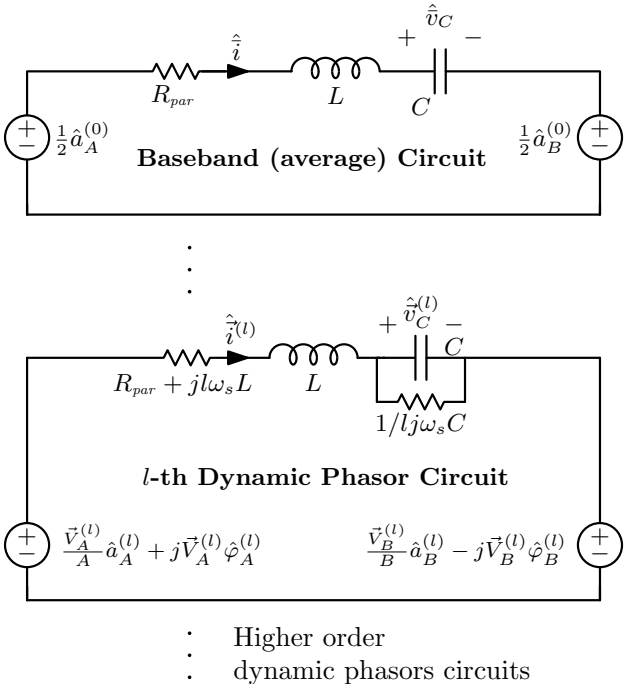


Figure 9.6: Small-signal circuit of the resonant tank.

Note that, based on (9.5) and (9.13), perturbations $\hat{u}_{\varphi_A}$ and $\hat{u}_{\varphi_B}$ of the phase shift modulating signals contribute to the baseband perturbation of $\bar{v}_A(t)$ and $\bar{v}_B(t)$.

9.3.3 Multi-Harmonic Small-Signal Model of the Tank Dynamics

The dynamic effect described by (9.5), (9.6), (9.13) and (9.14) can be included in the small-signal circuit of the resonant tank as follows:

- A small-signal phasor equivalent circuit is associated to each harmonic of the switching rate. Each of these circuits makes use of complex electrical elements as discussed in [42], describing the phasor dynamics of the resonant tank in the vicinity of the associated harmonic. The small-signal average circuit is included as well to model the baseband

dynamics.

- The switching node perturbations are included by means of independent voltage sources modeling the amplitude and phase small-signal contributions $\hat{a}_x^{(l)}(t)$ and $\hat{\varphi}_x^{(l)}(t)$ of each leg, according to (9.4) and (9.12).

The resulting circuit is depicted in Fig. 9.6. Observe that this model does not account for small-signal contributions due to perturbations of the input and output voltge. This issue is addressed in the next section.

9.3.4 Output Voltage Dynamics

In order to describe the influence of the output capacitor voltage on the system dynamics two effects have to be considered, namely *i*) the effect of a perturbation of the output voltage on the resonant current $i(t)$, and *ii*) the effect of a perturbation of the tank current and modulator inputs on the output voltage $v_o(t)$. As already shown in chapter 6.3.1, both phenomena can be accounted for in a simplified manner as long as the *small-ripple approximation* can be invoked for $v_o(t)$. Dynamically speaking, this is equivalent of stating that $v_o(t)$ is essentially a baseband signal, with negligible content at the switching frequency and its harmonics,

$$v_o(t) \approx \bar{v}_o(t) = V_o + \hat{\bar{v}}_o(t). \tag{9.18}$$

As for *i*), and as long as (9.18) is valid, the effect can be seen as a series of AM modulations of the harmonic components of $v_B(t)$, $\hat{\bar{v}}_o(t)$ being the modulating signal. More formally, the steady-state expression of $v_B(t)$ is

$$v_B(t) = D_B V_o + V_o \sum_{l=1}^{+\infty} c_B^{(l)}(t), \tag{9.19}$$

with

$$c_B^{(l)}(t) = \frac{2}{l\pi}\sin\left(l\pi D_B\right)\cos\left[l\omega_s t - l\left(\pi + \Phi_B\right)\right] \tag{9.20}$$

expression of the l-th harmonic of the modulated signal. A small-signal perturbation $\hat{\tilde{v}}_o(t)$ of the average output voltage yields, for the l-th harmonic, the contribution

$$v_B^{(l)}(t) = \left(V_o + \hat{\tilde{v}}_o(t)\right) c_B^{(l)}(t). \tag{9.21}$$

In terms of dynamic phasor, the above result can be expressed as

$$\vec{v}_B^{(l)}(t) = \vec{V}_B^{(l)} + \hat{\vec{v}}_B^{(l)}(t) = \vec{V}_B^{(l)} + \frac{\vec{V}_B^{(l)}}{V_o}\hat{\tilde{v}}_o(t). \tag{9.22}$$

The term $\hat{\vec{v}}_B^{(l)}(t)$ represents the perturbation of the dynamic phasor $\vec{v}_B^{(l)}(t)$ caused by a small-signal baseband perturbation $\hat{\tilde{v}}_o$ of the output voltage. This effect can be included into the equivalent small-signal circuit of Fig. 9.6 by means of a controlled voltage source yielding the small-signal circuit of Fig. 9.7.

As for *ii*), under the hypothesis of lossless bridges, the instantaneous power $p(t)$ at the AC-side of the leg B is equal to the instantaneous power at the DC-side (Fig. 9.8)

$$p(t) = v_B(t)i(t) \tag{9.23}$$

that can be represented as $p(t) = \bar{p}(t) + \tilde{p}(t)$ where $\bar{p}(t)$ represents the average power and $\tilde{p}(t)$ is the fluctuating power responsible for the output ripple. Since we are interested in describing the average dynamics of the output voltage, the fluctuating term $\tilde{p}(t)$ is neglected. The average power $\bar{p}(t) = P_{DC} + \hat{\bar{p}}(t)$ is calculated as follows

$$\bar{p}(t) = \bar{v}_B(t)\bar{i}(t) + \frac{1}{2}\Re\sum_{l=1}^{\infty}\left[\vec{v}_B^{(l)}(t)\vec{i}^{(l)*}(t)\right] \tag{9.24}$$

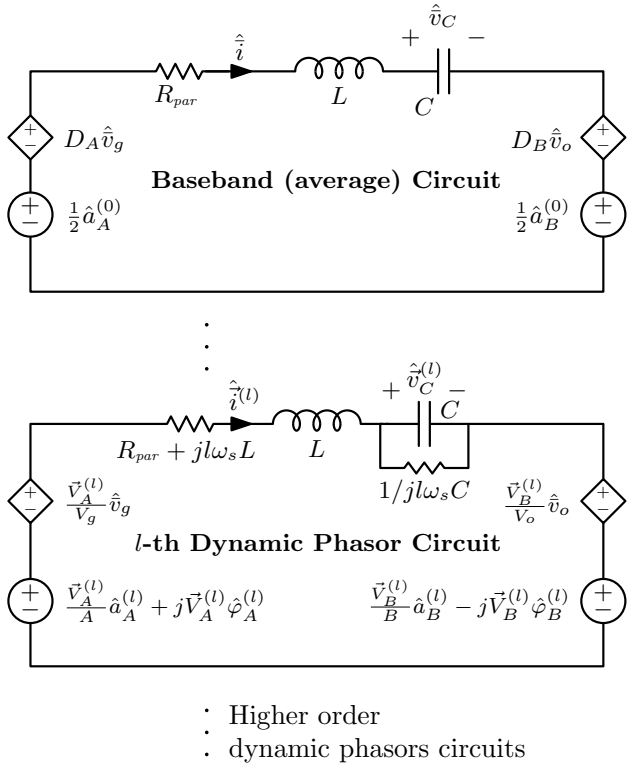


Figure 9.7: Small-signal circuit of the resonant tank including small-signal baseband contributions due to $\hat{\bar{v}}_g(t)$ and $\hat{\bar{v}}_o(t)$.

where

$$\begin{cases} \bar{v}_B(t) = V_B + V_o\hat{d}_B(t) + D_B\hat{\bar{v}}_o(t) \\ \bar{i}(t) = \bar{I} + \hat{i}(t) \\ \vec{v}_B^{(l)}(t) = \vec{V}_B^{(l)} + \frac{\vec{V}_B^{(l)}}{B^{(l)}}\hat{a}_B^{(l)}(t) - j\vec{V}_B^{(l)}\hat{\varphi}_B^{(l)}(t) + \frac{\vec{V}_B^{(l)}}{V_o}\hat{\bar{v}}_o(t) \\ \vec{i}^{(l)}(t) = \vec{I}^{(l)} + \hat{\vec{i}}^{(l)}(t) \end{cases} \tag{9.25}$$

In (9.24), the term $\bar{v}_B(t)\bar{i}(t)$ accounts for the power delivered by the average tank current and the average voltage of $v_B(t)$. The generic term $\frac{1}{2}\vec{v}_B^{(l)}(t)\vec{i}^{(l)*}(t)$ represents the average (baseband) component of the power associated to the l-th harmonics of $v_B(t)$ and $i(t)$.

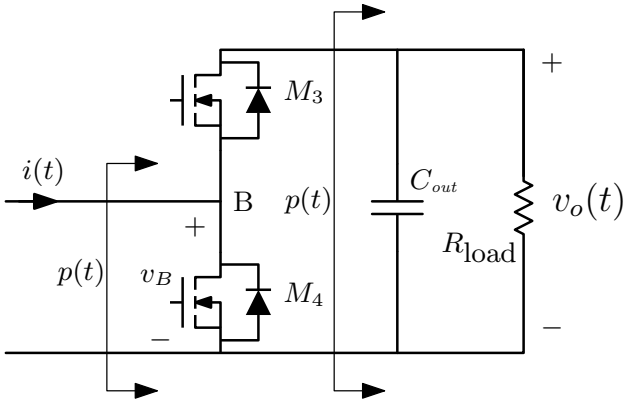


Figure 9.8: Output stage of the series resonant dc-dc converter.

To derive the output voltage dynamic equation, consider the average power $\bar{p}_{c_o}(t)$ entering in the output capacitor

$$\bar{p}_{c_o}(t) = \bar{p}(t) - \frac{\overline{v_o^2}(t)}{R_{\text{LOAD}}} \tag{9.26}$$

where $\overline{v_o^2}(t)/R_{\text{LOAD}}$ is the instantaneous power delivered to the load. Under the small-ripple approximation (9.18), one has $\overline{v_o^2}(t) \approx \bar{v}_o^2(t)$. The average current $\bar{i}_{c_o}(t)$ flowing through the output capacitor is derived dividing Eq. (9.26) by $\bar{v}_o(t)$,

$$\bar{i}_{c_o}(t) = \frac{1}{\bar{v}_o(t)} \left(\bar{p}(t) - \frac{\bar{v}_o^2(t)}{R_{\text{LOAD}}} \right). \tag{9.27}$$

Finally, the dynamic equation describing the dynamics of the output capacitor is

$$\frac{d}{dt}\bar{v}_o(t) = \frac{1}{C_o \bar{v}_o(t)} \left(\bar{p}(t) - \frac{\bar{v}_o^2(t)}{R_{\text{LOAD}}} \right). \tag{9.28}$$

After linearization, equation (9.28) yields the small-signal circuit of Fig. 9.9 that describes the dynamics of the output stage of the series resonant dc-dc converter. The small-signal circuit of the output stage is composed by a baseband average circuit including the RC load, a series of controlled current sources connected in a Norton configuration that takes account of perturbation

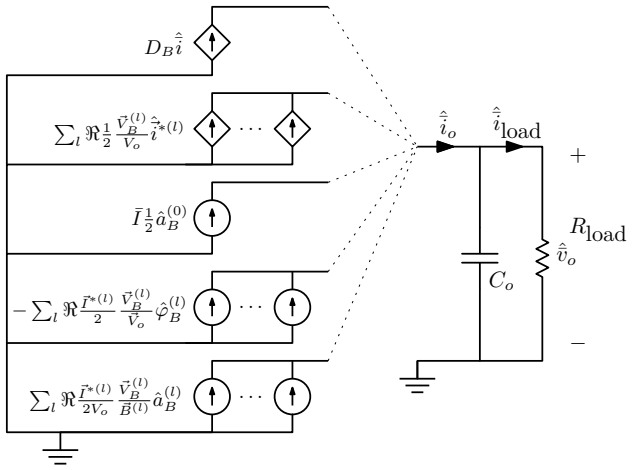


Figure 9.9: Small-signal circuit of the output stage.

in the tank current and a series of independent voltage sources that accounts for the perturbations in the driving signals. The equivalent small-signal circuit of the converter is sketched in Fig. 9.10 where only baseband and fundamental harmonic dynamics are shown explicitly. The input stage circuit is obtained in the same way of the output stage described above. The dynamics of the modulators are represented by block diagrams that feed the inputs $\hat{a}_x^{(l)}(t)$ and $\varphi_x^{(l)}(t)$ of the small-signal circuit.

9.4 Experimental Results

To validate the model the system of Fig. 9.11 has been developed. The converter used to validate the model is the one with parameters summarized in Tab. 9.1. The LC tank has a resonant frequency of about 132 kHz and is operated above resonance at a switching rate of 195 kHz. The inductance is realized with a Coilcraft SMT power inductor of the DO3316P Series. As for the converter switching devices, Infineon OptiMOS®3 power MOSFET of the type IPD036N04L G is employed, having $r_{ds,on} \approx 3.6\,\text{m}\Omega$ and rated 40 V, 90 A. As for the parasitic resistance of the inductor r_L, a value of

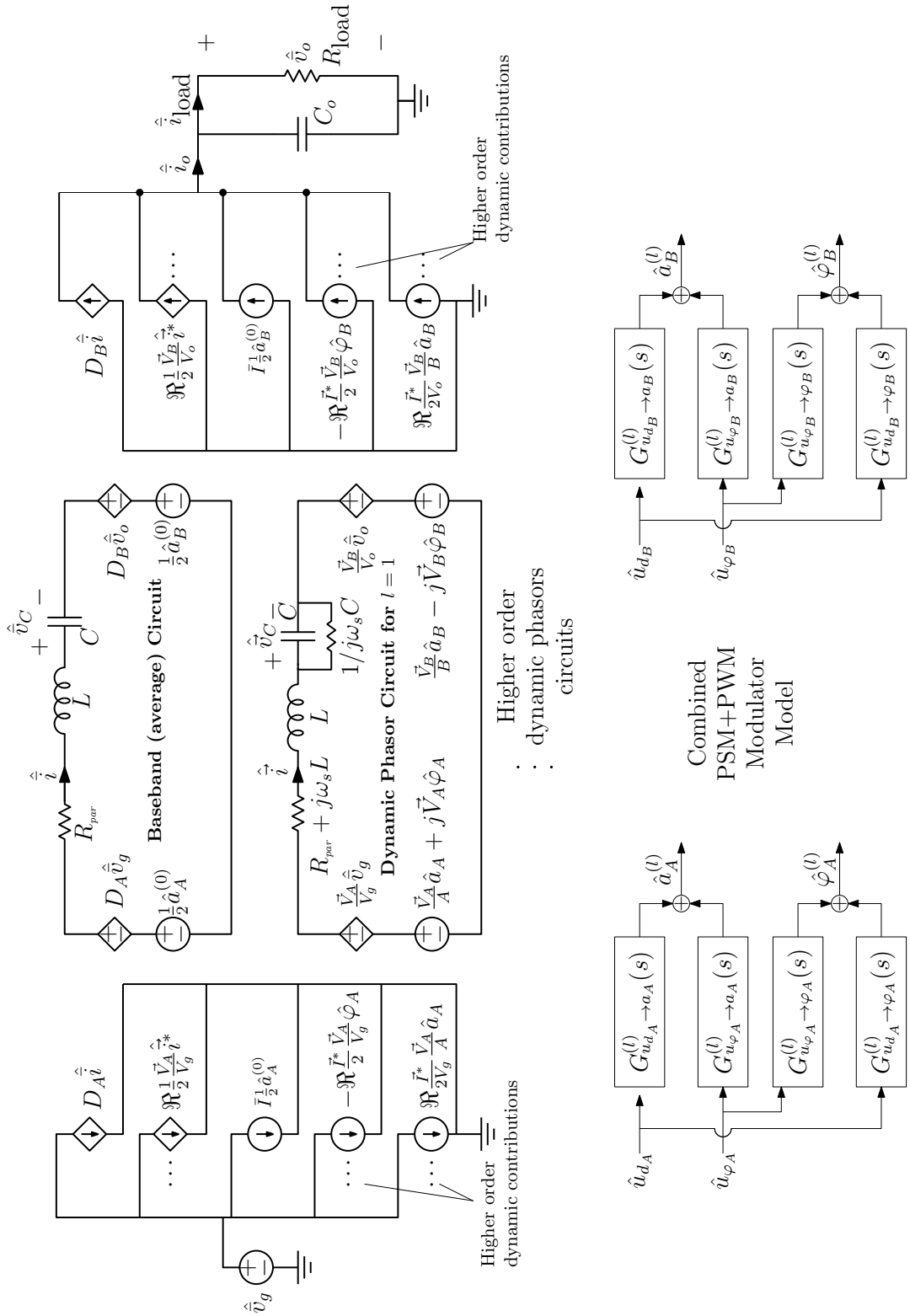


Figure 9.10: Proposed multi-harmonic small-signal circuit. Perturbations of baseband and phasor quantities are indicated with $\hat{\tilde{x}}$ and $\hat{\vec{x}}$ respectively.

Table 9.1: Parameters of the DHB-SRC Case Study

Switching frequency f_s	200 kHz
Input voltage V_g	12 V
Output voltage V_o	5 V
Maximum output current $I_{load,max}$	1.2 A
Tank capacitance C	635 nF
Tank inductance L	2.28 µH
Output capacitance C_o	110 µF
Equivalent parasitic resistance R_{par}	0.22 Ω

0.196 Ω is estimated by measuring the inductor resistance at 200 kHz using an impedance analyzer. Considering that, in every instant, two MOSFETs are connected in series with the LC tank, R_{par} is estimated as $R_{par} = r_L + 2r_{ds,on} = 0.196\ \Omega + 0.0036\ \Omega \approx 0.2\ \Omega$. The digital controller including the regulator, the map and the combined PWM+PSM modulators are VHDL-coded and implemented on a commercial FPGA development board provided by Altera. The voltage loop gain $T(s)$ is compensated by means of a proportional integral (PI) regulator designed for a crossover frequency of about 10 kHz. The two modulating signals used for regulating the output voltage are u_{d_A} and u_{φ_A}, while leg B is kept at $D_B = 0.5$, $\Phi_B = 0$. The control scheme is similar to the one presented in chapter 4 with the sole difference that both phase shift and pulse width modulations are performed on the leg A as illustrated in Fig. 9.12. The map transforming the control signal $u[k]$ into the modulating

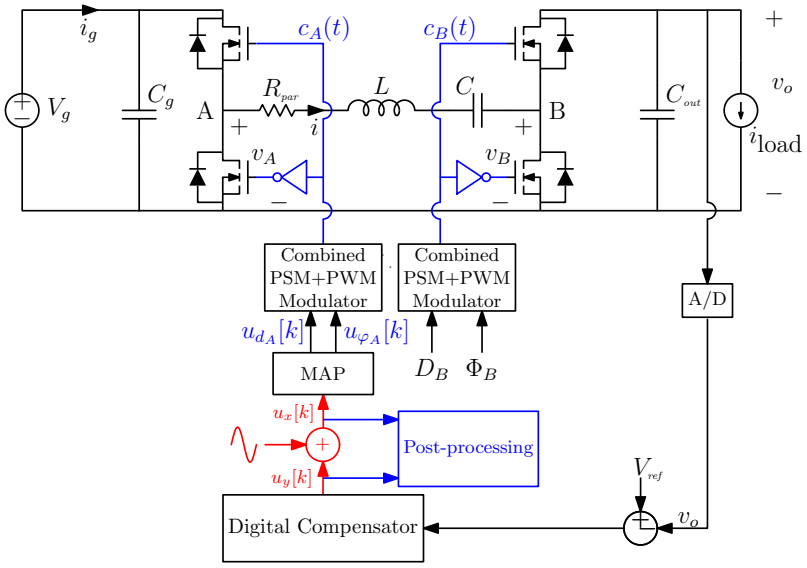


Figure 9.11: Multi-variable controlled series resonant converter considered for experimental validation, including perturbation injection for loop gain measurement.

vector (u_{d_A}, u_{φ_A}) is, therefore,

$$\begin{cases} u_{\varphi_A}[k] = u[k] \\ u_{d_A}[k] = u_{\varphi_A}[k]/\pi \end{cases} \tag{9.29}$$

with the phase signal u_{φ_A} expressed in radians.

The converter is operated at $V_g = 12\,\text{V}$, $V_o = 5\,\text{V}$, $R_{load} = 12\,\Omega$ with modulator operating point $\Phi_A = 32°$, $D_A = 0.18$. The 8 bits of the modulator allows a resolution of 1.4° for the phase shift and 0.7% for the duty cycle. In order to improve the resolution beyond such hardware limits, a 7-bit first-order $\Sigma - \Delta$ modulator is interposed between the digital compensator and the digital PSM+PWM modulator.

In both experiments and simulations, the loop gain is extracted using Middlebrooks injection technique by superimposing a square-wave perturba-

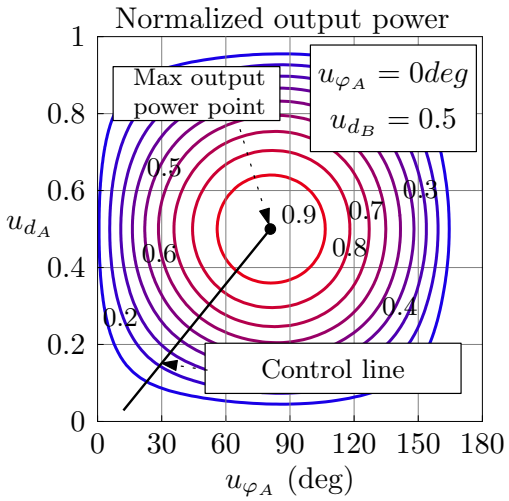


Figure 9.12: Control line and constant output power contours relative to the online efficiency optimization technique described in [56].

tion of small amplitude to the digital phase control command $u[k]$ (Fig. 9.11). Successively, signals before and after the injection point are post-processed with a DFT-based analysis, and their spectral components at the perturbation frequency extracted in order to calculate the experimental loop gain in amplitude and phase. Fig. 9.13 compares the Bode plot calculated with the proposed model, with switching level Simulink simulations and experimental results.

In order to highlight the importance of including multiple harmonics in the dynamic analysis of the converter, consider the following numerical case study. An 8 MHz implementation of the converter of Fig. 9.1a is designed to work above resonance with resonance frequency f_0 equal to 3.2 MHz. The baseband small-signal circuit introduces a resonance in the transfer function $G_{u_d \to v_o}(s)$ located at f_0; on the other hand, the dynamic phasor small-signal circuit relative to the fundamental harmonic $l = 1$ introduces resonances located at $f_s - f_0 = 4.8$ MHz and $f_s + f_0 = 11.2$ MHz. In this case the frequency resonance introduced by the average dynamics heavily modifies the

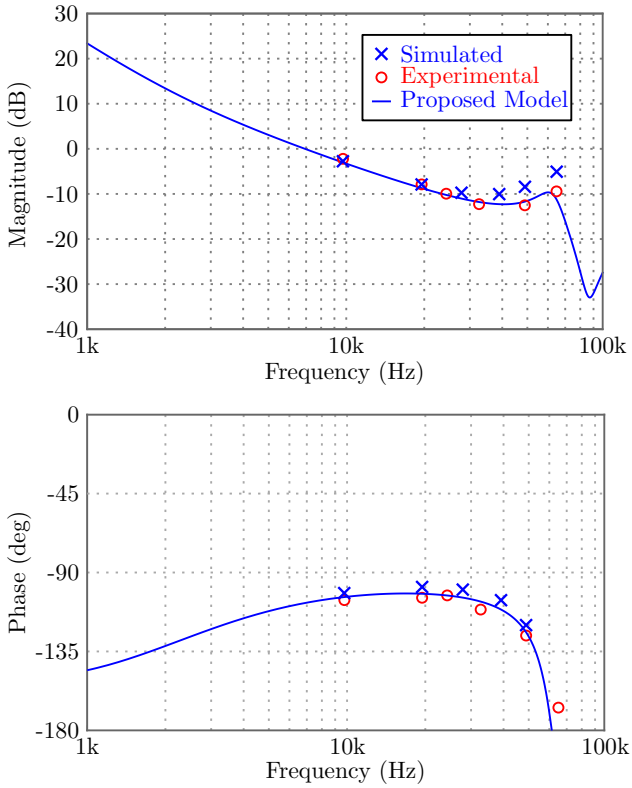


Figure 9.13: Theoretical, simulated and experimental loop gain Bode diagrams of the system of Fig. 9.11

converter frequency response and cannot be neglected for the regulator design. Fig. 9.14 shows the transfer function $G_{u\to v_o}(s)$ between the control signal $u[k]$ and the output voltage v_o using the map (9.29), comparing a single-harmonic model with a multi-harmonic model accounting for both the baseband and the switching frequency dynamics.

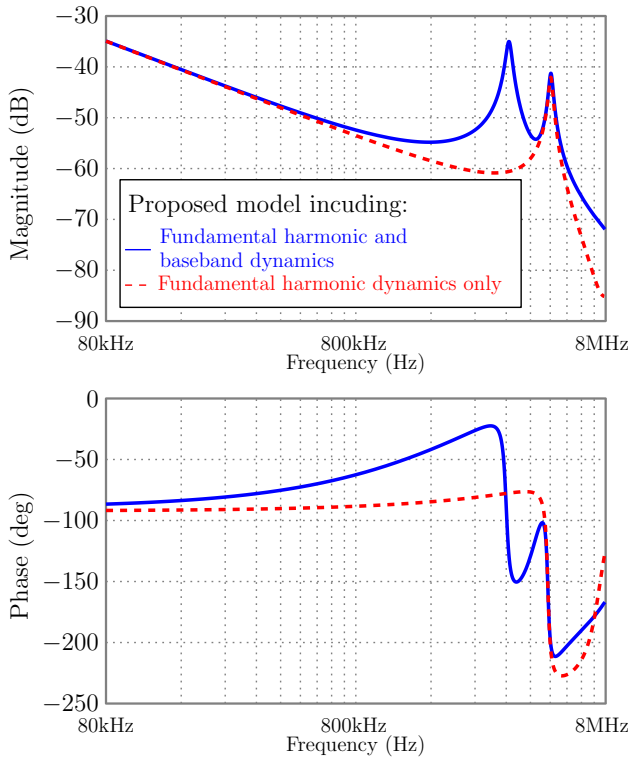


Figure 9.14: Bode diagrams of the transfer function $G_{u \to v_o}(s)$ for the $f_s = 8$ MHz converter numerical case study.

Chapter 10

Conclusions

This research activity is conducted through the collaboration between Infineon Technologies Italia and the Department of Information Engineering (DEI) of the University of Padova within the framework of a contract of *Apprenticeship in Higher Education and Research*, and focuses on modeling and design of efficiency optimization techniques for high-frequency dc-dc converters in automotive applications. Part of the research activity has been developed during a six months visiting period at the *Colorado Power Electronics Center* of the University of Colorado at Boulder, under the supervision of Prof. Dragan Maksimović.

The architecture of the system considered throughout the thesis is based on a multiple loop approach in which the regulation loop and the optimization loop simultaneously operate to guarantee a stable voltage supply to the electronic control unit and an efficient power conversion. The two topologies of dc-dc converters considered in the work are the DHB-SRC and the non resonant version of the DAB converter. Both converters are chosen because of their relative low hardware complexity and the number of degrees of freedom available for purpose of regulation and optimization.

Main contributions of the thesis are summarized as follows:

1. A multivariable control strategy combining a fast regulation loop with a slower efficiency optimization loop operating is proposed for the DHB-SRC. Power and efficiency contours of the converter are first analyzed using a multi-harmonic model for steady-state analysis, combined with an approximated model of conduction and switching losses. For the latter, the methodology originally disclosed in [32] is reformulated to include partial ZVS switching and incorporated in the calculations.
   A robust interacting control is then proposed which enables to maintain output voltage regulation and on-the-fly efficiency optimization againts abrupt changes in the load current. Convergence of the optimization method, which does not require a preliminary efficiency characterization of the power converter, is ensured by the uniqueness of the maximum efficiency point in the control plane. Experimental measures confirm the effectiveness of the proposed efficiency optimization approach. Results of the research is disclosed in [56] and a patent [57] is filed.

2. In conjunction with the visiting program at the Colorado Power Electronics Center, a 100MHz DHB-SRC is developed based on Gallium-Nitride (GaN) technology. In [58] the interacting control for online efficiency optimization already developed for the resonant converter stage is combined to a burst control.

3. The non-resonant dual active bridge is analyzed from a static point of view revealing that the choice of a small inductance in conjunction with a smart modulation scheme enables the possibility to design a high frequency and high efficiency converter. The steady-state and power losses modeling methodology already developed for estimating

conduction and switching losses in the resonant converter are adopted to the non-resonant dual active bridge case as well. The different possible switching sequences are analyzed in a systematic way revealing the best operating regions of the converter from the efficiency standpoint.

4. Moving from the results of the steady state analysis of the DAB converter a multivariable control strategy based on a multiple-loop structure is proposed in chapter 5. A technique based on the simplex algorithm is developed for the maximum efficiency operating point tracking.

The second part of the thesis focuses on the dynamic study of the regulation loop of the analyzed converters. In particular, the modeling procedure for describing the small-signal dynamics of uniformly sampled phase shift modulators and combined phase shift and pulse width modulators is clarified. The main contributions are listed below:

1. As for pure phase shift modulators, in analogy with the theory of pulse width modulators, it is found that the sampled nature of the modulating signal introduces a small-signal transport delay in the modulator frequency response. Such delay depends on the modulator operating point as well as on the type of carrier employed to generate the desired phase shift. As a secondary effect, a small attenuation term is also seen in the magnitude response of the modulator. Preliminary results are presented in [59] and extended for journal publication in [60].

2. As for the combined phase shift and pulse width modulators, the study indicates that small variations of the duty cycle and phase shift modulating signals individually induce both amplitude and phase perturbations on the dynamic phasor at the output of the modulator. Furthermore, even though the modulating scheme is chosen in order to make the duty

cycle and phase shift modulating signals independent in steady state, the study reveales a dynamical cross-coupling between the duty cycle and phase modulating signals. Results of the research are disclosed in [61].

3. These results are employed to develop a multi-harmonic small-signal circuit for a digitally controlled DHB-SRC. The obtained model includes the additional dynamics introduced by sampled nature of the modulator. Results of the research are published in [62].

All the theoretical findings are validated both via simulations and experimental tests.

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