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CICLO XXII

# ESD AND IONIZING RADIATION EFFECTS ON ULTRATHIN BODY SOI AND MULTIPLE GATE TECHNOLOGIES

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*To Stefania*

*This proceeding can be criticizable:*
*but, certainly, it leads to interesting results*

A.N. Kolmogorov

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# Abstract

This thesis addresses two main reliability challenges of advanced UltraThin Body (UTB) Silicon On Insulator (SOI) and FinFET CMOS technologies: ElectroStatic Discharge (ESD) and (space) ionizing radiations. First, both technologies have a limited available silicon volume to dissipate the ESD current. Therefore, a detailed ESD analysis on such devices is required. Secondly, these advanced technologies will be incorporated in future Commercial-Off-The-Shelf (COTS) components that may be used in space applications, which rennires the impact of ionizing radiation on such technologies.

ESD analysis has been performed on structures implemented in planar UTB SOI, SOI FinFET, and bulk FinFET technologies. Complex dependencies of the different ESD performance parameters on both device geometry and process technology are found. For UTB SOI devices, a detailed electrical investigation is carried out in order to carefully classify the observed failure mechanisms. It is found that grounded gate NMOS devices are robust enough when local clamping devices are used, and that strain improves the ESD robustness and has an impact on the device failure mechanisms. Concerning FinFET technology, non-uniform failure exists for grounded gate NMOS devices at high current levels which can be improved by increasing gate length and various ballasting techniques. On the other hand, voltage clamping capability seemed more of a concern due to the oxide breakdown voltage for long gate lengths. Narrow fin devices have improved cooling properties, especially for bulk FinFETs, but suffer from reduced area efficiency. Selective epitaxial growth, strain, and silicide blocking can improve the ESD performance of FinFET devices. From RF point of view, concerning SOI FinFET technology, the large overhead capacitance of the narrow-fin devices degrades the RF figure of merit with respect to the wide fin devices, making wide-fin devices the preferred choice. Regarding bulk FinFET technology, the landing pad of narrow-fin devices is not fully used during the current conduction; however, the full junction contributes to the parasitic capacitance. Therefore, despite the quite remarkable improvement in ESD robustness observed for narrow-fin bulk FinFET devices, narrow and wide-fin bulk FinFET diodes have similar ESD-RF performance, which is comparable to the best SOI FinFET diodes.

Heavy-ions induced microdose has been investigated on MOS in planar UTB SOI and SOI FinFET technologies. The degradation of the electrical DC parameters is found

to strongly depend on both device geometry and process technology. UTB SOI devices display the lack of early breakdown due to the very thin gate oxide, and varying impact on the long-term degradation kinetics depending on the adopted technological solutions. Concerning SOI FinFETs, the changes of the DC parameters after irradiation strongly depend on the Linear Energy Transfer (LET), incidence angle, strain, and channel type, depending on the balance between damage to the high-k (top and sidewall) gate oxide and to the buried oxide. In addition, heavy-ion strikes impact both on the degradation kinetics and on the time to breakdown under constant voltage stress. The soft rupture of the gate oxide is a considerable concern, not only for the increase in gate leakage, but also for the effects on the DC characteristics. Interface state generation in the side oxide/body interface, due to ions passing through the lateral gates, is another remarkable effect that can be observed only with these vertical devices. Heavy ions can induce permanent damage on FinFETs with large statistical spread. The distribution of the inverse of the gate leakage currents and of the threshold voltage shifts follows a Weibull distribution. Moreover, the reciprocal of the gate leakage current does not respect the Poisson area scaling. A new model for the gate leakage current is proposed, predicting a size of the heavy-ion damage of 30 nm and a higher defect generation takes place in the sidewall gate oxide.

Dose enhancement effects due to interconnects in deep-submicron CMOS have been studied. The presence of metal-1 tracks in the proximity of the device active areas significantly modifies the response to X-rays. The impact of the secondary electron emission from metal-1 layers is strongly dependent on the relative position to the transistor lateral isolation and LDD spacers.

In conclusion, ESD is not a showstopper for the introduction of UTB SOI and FinFET technologies. However, heavy-ion induced microdose is a serious concern for multiple gate technologies, while it is not a showstopper for the UTB SOI. Finally, dose enhancement in deep-submicron devices must be carefully considered when X-ray facilities are used to perform total-dose tests.

# List of Acronyms

| | |
|---|---|
| *2-D* | Two Dimensional |
| *BEOL* | Back End Of Line |
| *BJT* | Bipolar Junction Transistor |
| *BOX* | Buried Oxide |
| *CCTLP* | Capacitively Coupled Transmission Line Pulse |
| *CESL* | Contact Etch Stop Layer |
| *CDF* | Cumulative Distribution Function |
| *CDM* | Charged Device Model |
| *CHC* | Channel Hot Carrier |
| *CMOS* | Complementary Metal Oxide Semiconductor (technology) |
| *COTS* | Commercial Off The Shelf |
| *CVS* | Constant Voltage Stress |
| *DC* | Direct Current |
| *DIBL* | Drain Induced Barrier Lowering |
| *DUT* | Device Under Test |
| *EOT* | Equivalent Oxide Thickness |
| *ESD* | Electro Static Discharge |
| *ESDA* | Electro Static Discharge Association |
| *EOS* | Electrical Over Stress |
| *FDSOI* | Fully Depleted Silicon On Insulator |
| *FEOL* | Front End Of Line |
| *FinFET* | Fin Field Effect Transistor |
| *FinFLASH* | Fin Flash (memory) |
| *FOM* | Figure Of Merit |
| *FUSI* | Fully Silicided |
| *ggNMOS* | grounded-gate NMOS |
| *GOX* | Gate OXide |
| *HBM* | Human Body Model |
| *HDD* | Highly Doped Drain |
| *HMM* | Human Metal Model |
| *HV* | High Voltage |

| | |
|---|---|
| *IC* | Integrated Circuit |
| *ITRS* | International Technology Roadmap for Semiconductors |
| *JEDEC* | Joint Electron Device Engineering Council |
| *LDD* | Lightly Doped Drain |
| *LET* | Linear Energy Transfer |
| *LTRD* | Long-Term Reliability Degradation |
| *MM* | Machine Model |
| *MOSFET* | Metal Oxide Semiconductor Field Effect Transistor |
| *NBTI* | Negative Bias Temperature Instability |
| *PDF* | Probability Density Function |
| *PDSOI* | Partially Depleted Silicon On Insulator |
| *QM* | Quantum Mechanical |
| *RF* | Radio Frequency |
| *RH* | Radiation Hardened |
| *RILC* | Radiation-Induced Leakage Current |
| *RISB* | Radiation-Induced Soft Breakdown |
| *RSB* | Radiation-induced Soft Breakdown |
| *SB* | Silicide Blocking |
| *SCE* | Short Channel Effect |
| *sCESL* | strained Contact Etch Stop Layer |
| *SDF* | Spacer Defined Fins |
| *SEE* | Single Event Effect |
| *SEG* | Selective Epitaxial Growth |
| *SEGR* | Single-Event Gate Rupture |
| *SEM* | Scanning Electron Microscope |
| *SET* | Single Event Transient |
| *SEU* | Single Event Upset |
| *SICL* | Stress-Induced Soft Breakdown |
| *SJ* | Super Junction |
| *SOI* | Silicon On Insulator |
| *SONOS* | Silicon Oxide Nitride Oxide Silicon (memory) |
| *SRAM* | Static Random Access Memory |
| *SRB* | Strain Relaxed Buffer |
| *STI* | Shallow Trench Isolation |
| *SVS* | Staircase Voltage Stress |
| *SWS* | Source-to-Well Spacing |
| *TAT* | Trap Assisted Tunneling |
| *TCAD* | Technology Computer Aided Design |
| *tCESL* | tensile Contact Etch Stop Layer |
| *TDDB* | Time-Dependent Dielectric Breakdown |

| | |
|---|---|
| *TEM* | Transmission Electron Microscope |
| *TID* | Total Ionizing Dose |
| *TLP* | Transmission Line Pulse |
| *vfTLP* | very fast Transmission Line Pulse |
| *UTB* | Ultra Thin Body |
| *WKB* | Wentzel Kramer Brillouin (approximation) |

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*International journal contributions*

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*Awards*

Co-author of the Best Student Paper at the 2008 EOS/ESD Symposium:

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*Italian journal contributions*

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# Italian Summary – Riassunto in Italiano

Questa tesi si focalizza sullo studio della robustezza alla scariche elettrostatiche (*ElectroStatic Discharge* ESD) e della sensibilità a radiazioni ionizzanti delle tecnologie *UltraThin Body* (UTB) *Silicon On Insulator* (SOI) e *multi gate* FinFET, candidate a sostituire il MOSFET convenzionale bulk a partire dal nodo tecnologico dei 22 nm. Entrambe le tecnologie presentano un ridotto volume di silicio disponibile a dissipare la corrente indotta da un evento ESD. Pertanto, la robustezza ESD di tali tecnologie deve essere analizzata in dettaglio. D'altro canto, queste tecnologie, assieme a quella convenzionale bulk, potranno essere utilizzate anche per la fabbricazione di componenti *Commercial-Off-The-Shelf* (COTS) per applicazioni spaziali, che richiedono un'analisi accurata degli effetti indotti da radiazioni.

***Robustezza ESD***

L'analisi delle prestazioni ESD è stata condotta su strutture (MOSFET e diodi) implementate nelle tecnologie UTB SOI, SOI FinFET e bulk FinFET. Sono state trovate complesse dipendenze dalla geometria dei dispositivi e dal processo utilizzato.

*Robustezza ESD della tecnologia UTB SOI*

Per quanto riguarda la tecnologia UTB SOI, è stata proposto un nuovo metodo di analisi basato sulle caratteristiche elettriche DC al fine di individuare quali meccanismi di guasto si verificano (ad esempio, rottura dell'ossido di gate o filamento tra i terminali di source e drain).

Si è trovato che MOSFET di tipo N stressati in configurazione *grounded gate* (in cui l'ESD viene scaricata dal BJT parassita) mostrano una moderata robustezza a ESD (fino a 1 mA/μm) quando utilizzati come *local clamp*. Inoltre, si è dimostrato che lo strain, utilizzato per aumentare la mobilità dei portatori, aumenta la robustezza ESD e ha un impatto sui meccanismi di guasto.

*Robustezza ESD della tecnologia FinFET*

Per quanto riguarda la tecnologia FinFET, dispositivi NMOS in configurazione *grounded gate* mostrano ad alti livelli di iniezione un guasto dovuto ad una non uniforme distribuzione di corrente, che può essere migliorata aumentando la lunghezza di gate o utilizzando tecniche di *ballasting* (ad esempio, *silicide blocking*). Tuttavia, si è visto che la capacità di *voltage clamping* è fortemente limitata dalla rottura dell'ossido di gate per dispositivi con elevate lunghezze di gate.

FinFET con *fin* stretto, specialmente quelli realizzati in tecnologia bulk, mostrano una migliore dissipazione del calore sviluppato durante un evento ESD, ma allo stesso tempo, a causa dello spazio esistente tra un *fin* e l'altro, mostrano un'efficienza di layout ridotta rispetto ai dispostivi con *fin* largo.

Si è inoltre dimostrato che l'utilizzo della crescita epitassiale selettiva del silicio (*Selective Epitaxial Growth* SEG), lo strain e il *silicide blocking* possono aumentare la robustezza ESD nei dispositivi FinFET.

Da un punto di vista RF, dispositivi SOI FinFET con *fin* stretti presentano una figura di merito ESD-RF degradata rispetto ai dispositivi con *fin* largo, a causa di una grande capacità di *overhead*. Pertanto, i dispositivi con *fin* largo sono preferibili quando utilizzati come strutture di protezione a ESD per applicazioni RF. Per quanto riguarda invece la tecnologia bulk FinFET, il *landing pad* dei dispositivi con *fin* stretto è parzialmente utilizzato durante la conduzione di corrente ESD, tuttavia, la capacità di giunzione del *landing pad* contribuisce alla capacità parassita totale. Pertanto, sebbene i dispositivi con *fin* stretto mostrino una maggiore robustezza ESD intrinseca, le prestazioni ESD-RF sono simili sia per dispositivi con *fin* stretto cheper quelli con *fin* largo e sono comparabili con le migliori prestazioni ESD-RF dei SOI FinFET.

***Effetti indotti da ioni pesanti***

Gli effetti da microdose indotti da ioni pensati sono stati studiati per MOSFET realizzati nelle tecnologie UTB SOI e SOI FinFET. La degradazione delle caratteristiche elettriche DC dipende pesantemente sia dalla geometria del dispositivo che dal processo utilizzato.

*Effetti da microdose in dispositivi UTB SOI*

Sono stati osservati interessanti cambiamenti immediatamente dopo irraggiamento e durante stress elettrici in tali dispositivi utilizzanti anche tecniche strain: mancanza di rottura del'ossido di gate anticipata a causa dello spessore molto ridotto (solo 1.5 nm SiON) e dipendenza delle cinetiche di degradazione dallo strain utilizzato.

*Effetti da microdose in dispositivi SOI FinFET*

Gli effetti permanenti indotti da ioni pesanti sulle caratteristiche elettriche di SOI FinFET con ossido di gate ad alta costante dielettrica (high-k) dipendono pesantemente dagli effetti di microdose nell'ossido sepolto, dalla rottura dell'ossido di gate, e dalla generazione di stati trappola all'interfaccia ossido di gate/silicio. Contrariamente ai risultati ottenuti in esperimenti di *Single Event Gate Rupture* (SEGR) di solito eseguiti su grandi condensatori anche con ossidi high-k, dispositivi multiple gate mostrano soft breakdown e una considerevole variazione delle caratteristiche elettriche.

Ioni pesanti posso indurre difetti nei dispositivi FinFET con un ampio spread statistico. La distribuzione della variazione di tensione di soglia e dell'inverso della corrente di perdita dell'ossido di gate seguono la distribuzione di *Weibull*. Tuttavia, si è dimostrato che il reciproco della corrente di perdita non segue la cosiddetta *Poisson area scaling*. Un nuovo modello statistico è stato sviluppato, trovando che una maggiore generazione di difetti si verifica negli ossidi di gate verticali rispetto a quello orizzontale e che la traccia dello ione utile a creare difetti nell'ossido di gate è di circa 30 nm. Pertanto, un ulteriore scaling dei dispositivi multi gate può portare a drammatiche conseguenze per applicazioni spaziali poiché la traccia dello ione può risultare più grande del dispositivo stesso.

Infine, si è valutata anche l'affidabilità di tali dispositivi mediante stress di vita accelerati ad alti campi elettrici e si è trovato una riduzione del tempo al breakdown nei dispositivi irraggiati.

***Dose enhancement in MOSFET planari bulk***

Per quanto riguarda i MOSFET planari bulk si è studiato l'impatto della presenza della prima metal di interconnessione in prossimità dell'area attiva del dispositivo. Si è dimostrato che la sensibilità a raggi X dipende fortemente dalla posizione della metal di interconnessione, specialmente se fatta in rame, rispetto all'ossido di isolamento laterale (*Shallow Trench Isolation* STI) e agli *LDD spacers*.

In conclusione, la sensibilità a ESD non è un fattore di ritardo per l'introduzione nel mercato delle tecnologie UTB SOI e FinFET. Invece, per quanto riguarda la tecnologia *multi gate* FinFET, gli effetti da microdose indotti da ioni pesanti rappresentano un serio problema, mentre non lo è per la tecnologia UTB SOI. Infine, gli effetti indotti da *dose enhancement* in MOSFET convenzionali submicrometrici devono essere attentamente monitorati quando sono usate *facility* a raggi X per eseguire test di dose totale.

# Table of Contents

# Chapter 1

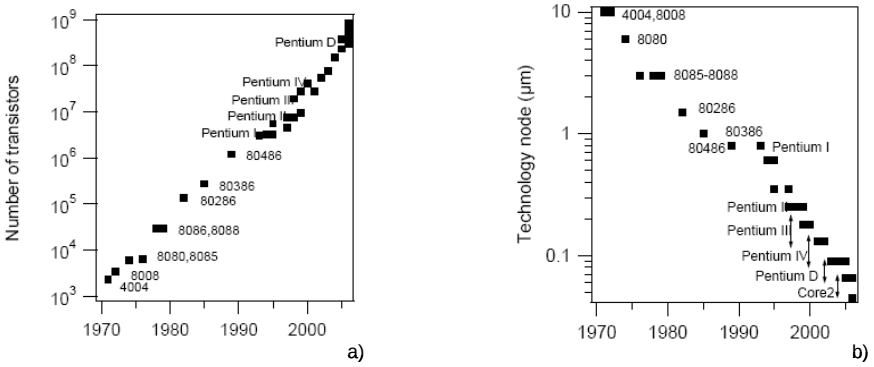
# Introduction

The reliability of the microelectronic devices and circuits is a major factor that determines both their manufacturability and application lifetime. Design for reliability should be implemented during technology, device and circuit development to avoid undesirable product development cycles and costly yield loss and field failures. The specific reliability problem studied in this PhD is caused by ElectroStatic Discharge (ESD) events and ionizing radiations.

## 1.1 CMOS Technology Scaling

The defining characteristic of the evolution in Complementary-Metal-Oxide-Semiconductor (CMOS) technology has been the continuous increase in the number of transistors on a chip at an exponential rate by reducing the size of the transistor, as given by Moore's Law [Intel_1]. This is illustrated in Figure 1.1, which charts the evolution of transistor technology at chipmaker Intel. The graph on the left shows how the number of transistors on a chip has increased from a mere 2300 in case of its first processor, the Intel4004 (released in 1971), to 800 million in case of the Core2, which was released in 2006. Likewise, the process technology has shown remarkable improvement over the years, shrinking from 10 μm feature sizes in 1971 to sub-45 nm feature sizes in 2007, a mind-boggling progress made in the span of 30 years.

CMOS technology is now entering a phase where simple shrinking is no longer sufficient to guarantee the performance gains required from each new technology generation. Alternative materials and structures are required (Figure 1.2) [Skotnicki08]. On one hand, Silicon-On-Insulator (SOI) technology is now becoming mainstream thanks to its superior control of Short-Channel Effects (SCE) and promise for scalability [Celler03]. According to the 2008 International Technology Roadmap for




a) Evolution of transistor count over time. b) Evolution of transistor feature size over time.

Figure 1.1: Graphs showing the increase in transistor count as well as the accompanying feature size reduction over time. This is a good illustration of Moore's Law and trends in scaling. Data have been used from [Intel_2], [Intel_3], and [Intel_4].

Semiconductors (ITRS) [ITRS08], multi-gate FinFET devices [Choi04] [Colinge08] and Fully Depleted (FD) SOI MOSFETs with Ultra-Thin Body (UTB) [Choi00] are the main candidates to continue with CMOS scaling below the 22 nm technological node. On the other hand, the use of high-κ dielectrics in combination with metal gates is needed to reduce the gate leakage current and to obtain correct N- and P-MOS threshold voltages without using channel doping. The implementation of a high-κ gate oxide induces mobility degradation [Gusev01], which can be compensated by the introduction of a strained silicon (Si) channel [Takagi08]. Uniaxial and/or biaxial strain in the channel through the use of stressor layers and/or substrate engineering are an example of how mobility improvement can be obtained.

## 1.2 Why Is Reliability Important?

Reliability is becoming a major bottleneck in the further downscaling of Very Large Scale Integration (VLSI) technologies [Groeseneken08_3]. On one hand, the dependability is affected by the continuous increase in electric fields and current densities, power densities and chip temperatures, number of interfaces, process complexity, and failure rate requirements. On the other hand, the speed of introduction new materials and architectures exceeds capabilities to explore reliability performance. It is therefore of primary importance to identify potential reliability issues in advanced technologies, which may be used also in space applications.

A large variety of degradation and failure mechanisms needs to be investigated, such as Hot Carrier (HC) degradation, Time-Dependent Dielectric Breakdown (TDDB),

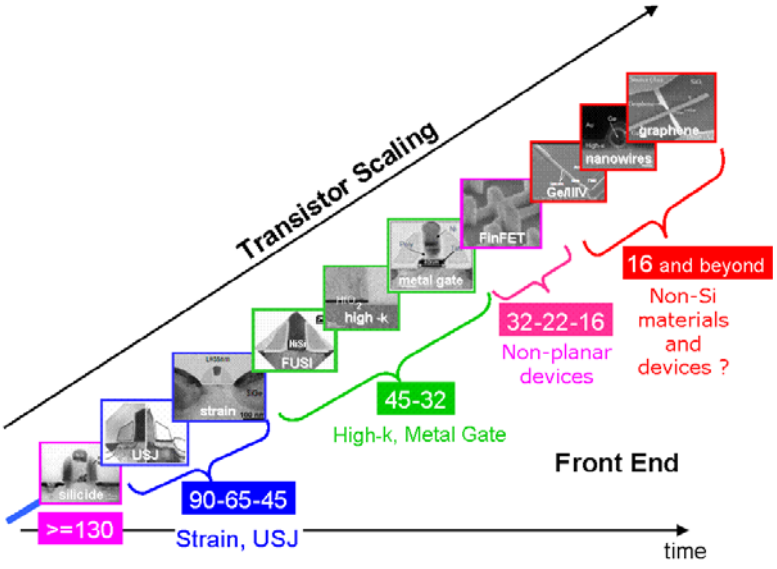
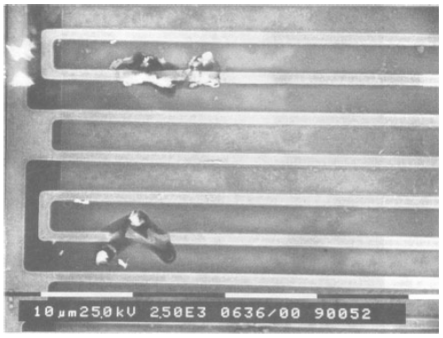


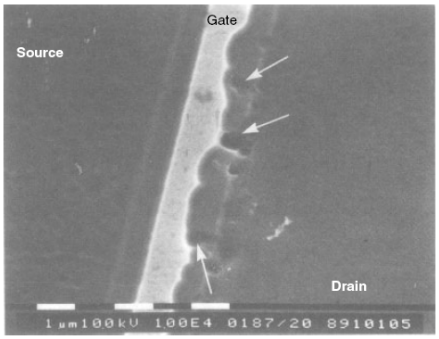

Figure 1.2: The evolution of the Si process technology after the 130 nm node [Groeseneken08_2].

Bias Temperature Instability (BTI), electromigration, stress voiding, interconnect dielectric instability and breakdown, electrostatic discharge, and ionizing radiations from space applications to sea level effects [Ohring98] [Santarini08]. Each of these reliability mechanisms has its own set of issues associated with technology scaling. This Ph.D. focuses on reliability problems associated with ionizing radiation effects and ESD events.

## 1.3 Electrostatic Discharge in Microelectronics

The phenomenon of ESD gives rise to images of lightning strikes or the sparks that leap from one's fingertips when touching a metal doorknob in dry winter. The sparks are the result of the ionization of the air gap between the charged human body and the zero-potential surface of the doorknob. Clearly a high voltage discharge takes place under these circumstances with highly visible (and sometimes tangible) effects. In the semiconductor industry, the potentially destructive nature of ESD in ICs became more apparent as semiconductor devices became smaller and more complex. The high voltages result in large electric fields and high current densities in the small devices, which can lead to breakdown of insulators and thermal damage in the ICs. The losses in the IC industry caused by ESD can be substantial if no efforts are made to understand and solve the problem. ESD causes about 37 % of IC failures [Santarini08] and represents annually a loss of billions of dollars due to repair, rework, shipping, labor and overhead costs



a)


b)

Figure 1.3: a) SEM photograph of silicon melting due to current filamentation in an nMOS output transistor and b) SEM photograph of an nMOS transistor showing gate-oxide damage [Amerasekera02].

associated with the damage, which highlights the importance of fundamental understanding of ESD aspects and design of efficient ESD protection.

ESD is the transient discharge of static charge, which can arise from human handling or contact with machines. In a typical work environment, a charge of about 0.6 µC can be induced on a body capacitance of 150 pF, leading to electrostatic potentials of 4 kV or greater. Any contact by the charged human body with a grounded object such as an IC pin can result in a discharge for about 100 ns, with peak currents in the ampere range. The energy associated with this discharge could mean failure to electronic devices and components. Typically, the damage is thermally initiated in the form of device or interconnect burnout (Figure 1.3a). The high currents could also lead to on-chip voltages that are high enough to cause oxide breakdown in thin gate MOS processes (Figure 1.3b). Many semiconductor devices can be damaged even at a few hundred volts, but the damage is too weak to be detected easily, resulting in what is known as walking wounded or latency effects. A device can be exposed to undetected ESD events, starting in the fabrication area during process and extending through the various manufacturing stages up to the system level. Thus, precautions to suppress ESD become important through all phases of an IC's life.

The introduction of each new generation of silicon technology results in new challenges in terms of ESD capability and protection circuit design. Hence, it is necessary to understand the main issues involved in ESD protection circuit design and the physical mechanisms taking place in order to ensure that the design can be scaled or transferred with minimum impact to the ESD performance.

To prevent ESD related failures, protection circuits are implemented within the IC chip (Figure 1.4). The ESD clamp is designed to protect the input gates or the output drain junctions by discharging the high ESD current. The clamp has a low resistance to $V_{SS}$ (Ground) during ESD. Good ESD protection elements should:

- clamp the ESD voltage when shunting the ESD stress current
- turn on fast

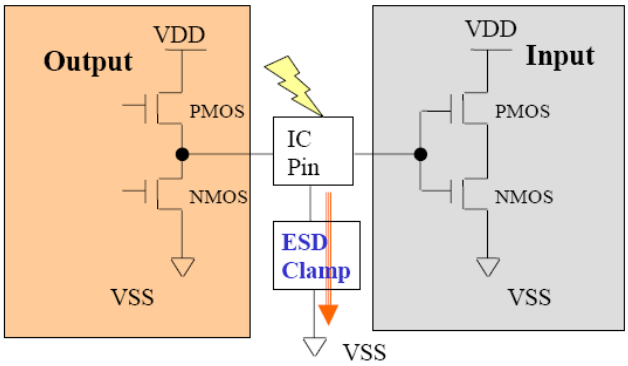



Figure 1.4: Generic on-chip ESD protection methodology.

- carry large currents
- have low on-resistance
- occupy minimum area at the bond pad
- have minimum capacitance
- introduce minimum series resistance
- be immune to process drifts
- be robust for numerous pulses
- offer protection for various ESD stress models
- not interfere with the IC's functional testing
- not cause increased $V_{CC}$ or I/O leakage
- survive the burn-in tests.

The ESD design window can be defined as the region in which the ESD protection elements need to operate, as shown in Figure 1.5. For the low voltage side, the window is limited by the normal operating regime, with which the ESD protection should not infer. For the high voltage side, the window is limited by the IC reliability, caused by the gate-oxide breakdown, turn-on parasitics, etc.

A typical snapback device IV is display in the ESD design window in Figure 1.5. In such devices, at a certain moment the device will be turn on, which allows to efficient dissipation of the ESD current. These devices turn on at their trigger point ($Vt_1$, $It_1$), which needs to be set before core damage. The holding voltage ($V_h$) denotes the minimum voltage to maintain the device action and should be at a safe level above $V_{DD}$ to avoid latch-up issues [Boselli05]. After snapback. The parasitic device dissipates the ESD current with a certain on-resistance ($R_{on}$) until its failure point ($Vt_2$, $It_2$) is reached. $It_2$ should be above the minimum required ESD current level.

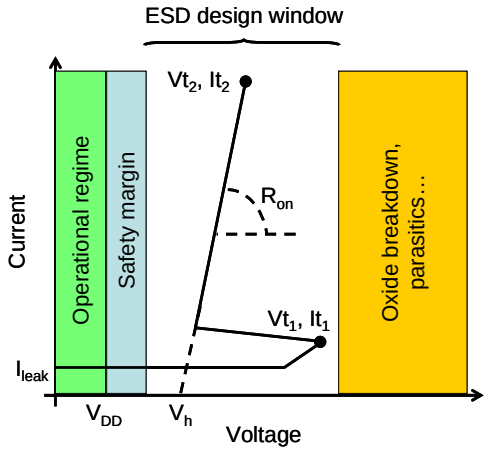



Figure 1.5: ESD design window.

## *1.3.1 ESD Challenges for Technology Scaling*

The introduction of each new generation of silicon technology can result in new challenges in terms of ESD capability and protection circuit design. The ESD performance for specific protection circuits change over time. Initially the ESD performance improves as the circuit designs mature and problems are solved or debugged. After a certain time the technology changes (i.e., LDD, silicides) cause the circuit to no longer function to its original capability, and the introduction of new protection techniques are needed to restore good ESD performance. CMOS ICs in automotive environments require very high ESD protection levels, which places an even higher demand on the design of protection circuits. The speed with which new technologies are introduced have reduced the available time for protection circuit development. In fact it is becoming more and more important to design circuits that can be transferred into the newer technologies with minimum changes. Hence, it is necessary to understand the main issues involved in ESD protection circuit design and the physical mechanisms taking place in order to ensure that the design can be scaled or transferred with minimum impact to the ESD performance.

The importance of building-in reliability demands design approaches that include ESD robustness as part of the technology roadmap. Figure 1.6 and Figure 1.7 depict how this ESD design window shrinks with every new CMOS bulk generation and how it will vanish. In Figure 1.6, the transient oxide breakdown voltage $BV_{OX}$ is compared with the scaling behavior of the corresponding grounded-gate (GG) NMOS ESD parameters ($Vt_1$ and $V_h$) as function of the oxide thickness. Clearly, the $BV_{OX}$ is decreasing faster with technology advancement than the corresponding NMOS clamping capabilities (Figure 1.6) [Mergens05]. As such, the ESD design window, delimited by the IC normal

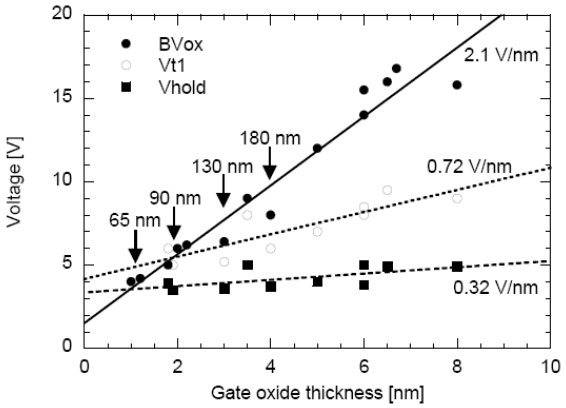



Figure 1.6: Oxide breakdown voltage ($BV_{OX}$), trigger ($Vt_1$) and holding voltage ($V_h$) of grounded-gate NMOS as a function of CMOS technology scaling [Mergens05].

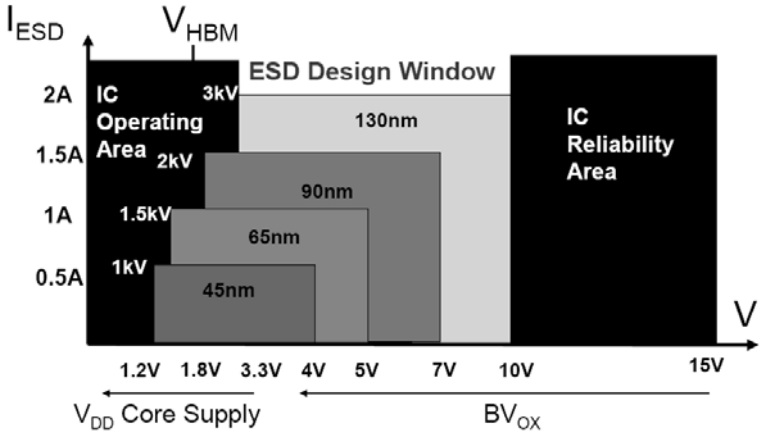



Figure 1.7: Impact of technology scaling on ESD design window [Duvvury08_1] [Duvvury08_2].

operation and IC reliability, in which the ESD device needs to operate, shrinks with each new technology generation Fig. 1.7. This means that traditional ESD protection cannot be used anymore as the sum of all voltage drops along the ESD path easily exceeds the breakdown voltage of the gate oxide of the core circuit.

The situation for the 65 nm node is even worse, as any overshoot due to slow turn-on of the ESD protection device needs to be carefully monitored, in order not to damage the core circuit. Nowadays, a lot of research is being done towards finding new ESD protection devices, optimizing trigger-speed of the ESD protection device and developing new ESD protection methodologies, such as distributed ESD protection clamps and local clamping without relying on any power clamp [Amerasekara02] To further continue CMOS scaling, more and more advanced techniques have to be introduced to cope with the challenges of nanometer-sized devices. Examples of these techniques include the introduction of high-K materials, metal gates, elevated source and drain, ultra-shallow

junctions, and strain engineering. ESD engineers have to follow this technology development very closely to detect any ESD problems early and to provide suitable solutions for them.

The ITRS forecasts the gate length of a transistor to shrink to 9 nm in 2016 [ITRS08]. Even if processing technology can provide these tiny physical dimensions, bulk CMOS will be electrically limited by short-channel effects. Out of the newly arising devices, UTB SOI and FinFET show promising performance. The roadmap suggests parallel scaling scenarios: some companies will extend planar bulk CMOS as long as possible, while others will switch to FinFET devices or to UTB SOI. While such parallel device technologies may co-exist for the years to come, it is conceivable that FinFET and planar devices may be combined together on the same chip. The life of planar CMOS would continue in the I/O / high voltage / mixed-signal area, and FinFETs would provide the high performance core devices. Possible merger scenarios could be bulk FinFETs combined with planar bulk devices, or FinFETs combined with planar UTB SOI. Regardless how the scenarios above will be implemented, major challenges for ESD development are ahead. The following options need to be explored: non-planar devices with ever smaller and 3-D devices geometries (i.e. FinFETs), new materials (high-k gate dielectrics), or strained silicon for enhanced carrier mobility, or non-silicon devices to name just a few. The ultimate MOSFET device and its susceptibility towards ESD stress is studied in the first part of the thesis.

## 1.4 Ionizing Radiation in Microelectronics

Every electronic device is subjected to radiation. Even the PC you use in your office or your house is subjected to a flux of ionizing particles that pass through its electronic components and that may cause a bit-flip or a soft error. In the last years, the radiation effects on electronic devices have become a major concern for manufacturing companies, as demonstrated by the words of Intel's senior scientist Eric Hannah [BBC08]: “What happens if a cosmic ray causes a collision inside the silicon chip, that releases lots of charged particles. All our logic is based on charge, so it gets interference. The risk from cosmic rays may not be thought of as a big problem on a single computer with a single chip, as there is the potential for error only perhaps every several years. But on a supercomputer with 10,000 chips, there was the potential for 10 or 20 faults a week. And the risk of cosmic ray interference will only increase as chips get smaller. This is because circuits will require less charge per switch to operate. Since the amount of charge from cosmic rays will remain the same, there will be a "bigger disturb". And this is potentially a problem not just for PCs and supercomputers, but anything with computer-operated parts - for example cars.” “You could be going down the autobahn at 200 miles an hour and suddenly discover your anti-lock braking system doesn't work because it had a

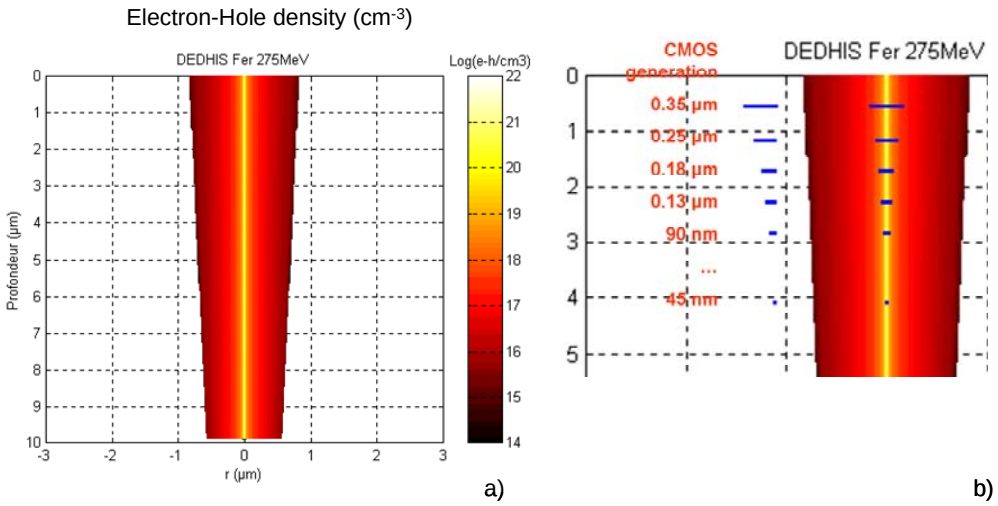



Figure 1.8: a) Simulated electron-hole density in the silicon induced by Fe ions with energy E = 275 MeV and LET = 24 MeVcm$^2$/mg [Foulliat04]. b) The simulated electron-hole density is compared with the CMOS minimum size.

cosmic ray event," Mr. Hannah said. "It's strange, but this is the reality we're moving into as we get smaller and smaller circuits."

Future small satellite systems for both Earth observation as well as deep-space exploration are greatly enabled by the technological advances in deep submicron microelectronics or even nanoelectronics technologies [Alkalai00]. Whereas these technologies advances are being fueled by the commercial (non-space) industries, more recently there has been an exciting new synergism evolving between the two otherwise disjoint markets. In other words, both the commercial and space industries are enabled by advances in low-power, highly integrated, miniaturized (low-volume), lightweight, and reliable real-time embedded systems. Recent announcements by commercial semiconductor manufactures to introduce SOI technology into their commercial product lines is driven by the need for high-performance low-power integrated devices. Moreover, SOI has been the technology of choice for many space semiconductor manufactures where radiation requirements are critical. This technology has inherent immunity to Single-Event-Effects (SEE) built into the process, which makes it very attractive to space applications [Schwank03].

## *1.4.1 Radiation Challenges for Advanced Technologies*

Over the course of the past decade, the Total Ionizing Dose (TID) radiation hardness of commercial microelectronics technologies has been evolving rapidly. For example, while only few years ago total dose failure levels of a few tens of krad($SiO_2$) were common, today's advanced digital CMOS ICs can in some cases approach failure

levels of 500 krad($SiO_2$) [Barnaby06] [Fleetwood03] [Oldham03]. However, it should be remarked that there is no guarantee of this performance. Considerable variation exists between manufactures, and since total dose hardness is maintained over that commercial manufactures monitor, there is no assurance that a given level of hardness is maintained over time. It has been shown that a considerable variability can exist within a single fabrication lot, with as much as a factor five variation in failure threshold observed within a single lot, including a factor of three variation within the same trend. As such, relying on the TID hardness of commercial ICs remains problematic [Felix06] [Hughes03] In this thesis, we will present how secondary electrons, emitted by the first metal layer, alter TID effects in MOSFETs.

Unfortunately, the situation is much different for single-event effects. SEE has recently become a substantial Achilles heel for the reliability of even earth-based advanced CMOS technologies. As the amount of charge that represents stored information has dropped lower and lower, so the sensitivity of CMOS devices to single-particle charge collection transients has increased [Dodd09].

A growing concern for energetic particle environments is microdose effects, that is, total-dose effects caused by individual energetic particles. These interesting effects sit at the intersection of traditional ionizing radiation dose effects and SEE [Dodd09]. Microdose is not really a new effect, having been known about and studied for some time. Indeed, the possibility that a single charged particle could cause total dose failure of a single transistor was postulated nearly twenty years ago by Oldham et al. [Oldham93].

A typical symptom of microdose has been the appearance of “stuck bits” with increasing particle fluence [Edmonds01]. Recently, the appearance of large increases in off-state leakage current in power MOSFETs has also been attributed to particle microdose effects [Felix07]. In the three-dimensional world of FinFETs, a heavy-ion strike at normal incidence may traverse the vertical sidewall gate oxide all along its length, possibly leading to dramatic consequences. Furthermore, the effect, that may pass unnoticed on a large structure, can become source of concern when the device size is comparable to (if not smaller than) the ion-track size (Figure 1.8), as in the case of state-of-the-art FinFETs. In the thesis, we will present an original experimental and modeling contribution illustrating how heavy ions may impact the electrical characteristics of sub 32-nm FinFETs in a permanent way.

## 1.5 Objectives of the Thesis

This thesis has three main objectives, namely to investigate the ESD robustness and microdose effects induced by heavy-ion strikes on the upcoming FinFET and UTB SOI technologies, and to analyze the dose enhancement due to interconnects.

Our first main objective is to investigate whether ESD is a potential showstopper for the introduction of FinFET and UTB FD SOI technologies. This is achieved by analyzing the ESD capability of basic ESD protection devices implemented in such technologies, such as gated diodes and MOS transistors. The 3D-nature of FinFET devices offers an increased set of geometrical parameters compared to planar transistors. Their impact on the ESD robustness needs to be evaluated and understood by means also of Technology Computer Aided Design (TACD) simulations. Further, different process and layout options are introduced to improve the overall device performance.

The second main objective is to provide an insight into the microdose effects induced by heavy-ion strikes on MOS FinFET and UTB FD SOI technologies. A fundamental understanding of the physics of the device degradation immediately after irradiation and during subsequent electrical stresses is the main part of the chapter. A statistical approach is proposed to investigate the degradation of FinFET devices.

The third main purpose is to analyze how the presence of the first metal tracks in the proximity of the device active areas may significantly modify the response to X-rays of deep-submicron planar CMOS technologies. This has been evaluated by means of TCAD simulations and transport code.

## 1.6 Outline of the Thesis

A summary of the different chapters of this thesis is provided below.

**Chapter 2: ESD Test Methods and Devices**

The fundamental protection elements and the commonly used and advanced ESD characterization and analysis techniques are summarized in this chapter.

**Chapters 3 and 4: ESD in Ultrathin-Body SOI and FinFET Devices**

In these chapters, the ESD robustness of the new emerging UTB FD SOI and FinFET technologies are evaluated. A fundamental understanding, supported by TCAD simulations, of the physics of the devices under ESD stress conditions is carried out.

**Chapter 5: Ionizing Radiation Effects**

This chapter gives an overview about the radiation environments, the importance of radiation effects for electronic devices, and about the basic mechanisms of interaction between ionizing particles and electronic devices.

**Chapters 6 and 7: Microdose Effects on FinFETs and Ultrathin-Body SOI Devices**

These chapters address to the physical understanding of microdose effects induced by heavy-ion strikes on the new emerging UTB FD SOI and FinFET technologies.

**Chapter 8: Dose Enhancement due to Interconnects in Deep-Submicron MOSFETs**

This chapter presents the first original experimental contribution illustrating how secondary electrons, emitted by the first metal layer, alter total-dose effects in devices manufactured with a 90-nm CMOS process and designed with different ad-hoc interconnect layouts.

**Chapter 9: Conclusions and Outlook**

The main results obtained from this work are summarized and a brief outlook is given towards future research.

# Chapter 2

# ESD Test Methods and Devices

Standard ESD qualification tools yield only pass-fail measurements while TLP can additionally be used for quasi-static device analysis. HBM testing with voltage and current capturing (HBM-IV) is the best ESD characterization and analysis tool to obtain both quasi-static and transient device information under realistic ESD stress conditions. The ESD protection elements commonly used are described.

## 2.1 Introduction

Devices subjected to high-current and high-voltage stress operate in very different mode under these conditions compared to the normal operating conditions. An understanding of the high-current device behavior is essential in analyzing the phenomena taking place in the IC during an ESD stress event. In the first part of this chapter the behavior of the main circuit elements used in ESD protection circuits is discussed.

Several ESD stress models exist: the Human Body Model (HBM), Machine Model (MM), and the Charged Device Model (CDM) etc. The ESD test should reproduce the different failure signatures and quantify the sensitivities attributable to the various types of ESD in an IC environment. ESD test standards specify how an IC has to be stressed in an ESD test system. They specify the discharge current waveforms for a given pre-charge voltage, acknowledging that the discharge current through the IC, generating voltage differences and heating up structures, is responsible for the majority of ESD failure mechanisms. In principle, the ESD sensitivity levels should allow a comparison with the levels of electrostatic voltage measured in a fabrication process.

In addition to the RLC-type stress methods (such as HBM, MM,CDM, etc.), square pulse methods have been used as an engineering toll (i.e., Transmission Line Pulse

(TLP)) in order to characterize and optimize ESD protection. These methods are extremely valuable for the analysis of poorly performing ESD protection in products. Square pulses can provide detailed insight into the quasi-static current versus voltage characteristics of an ESD protection element and of the elements to be protected in the ESD-relevant time and current domain. Solid-state pulse generators are used for longer pulse durations at lower amplitudes. In the second part of this chapter, all these ESD stress systems are described together with how to enhance these ESD techniques to give more information regarding transient device behavior under HBM condition.

## 2.2 ESD Test Methods

ESD events are recognized as a significant contributor of early life failures and failures throughout the operating life of semiconductors devices. Although contemporary IC designs include ESD protection circuitry, the effectiveness of this protection must be determined in a manner which will ensure its effectiveness in the "real world" if the part is to meet the reliability requirements for a given application [ESDA]. An ESD event may carry amperes of current in a short period of time, typically from hundreds of picoseconds to hundreds of nanoseconds. Needless to say such events are very harmful for sensitive electronic components and ICs.

For the purpose of reproduction under controlled conditions, the real world ESD events are classified in two main categories:

i. Component-level ESD testing, that is used to determine whether components such as ICs will be able to survive the manufacturing process in ESD-controlled areas.
ii. System-level ESD testing, which is used to see whether systems can survive ESD events occurring in the real world.

The most widely used ESD stress models for component-level ESD qualifications are:

- The Human Body Model (HBM), representing an ESD event caused by a charged human discharging the current into a grounded IC.
- The Machine Model (MM), representing a discharge coming from a charged machine into a grounded IC. This ESD model is typically used in automotive assembly lines.
- The Charged Device Model (CDM), covering the ESD discharge when a device or an IC is self-charged during the manufacturing process and comes into the contact with grounded equipment.

ESD qualification tests (HBM, MM, CDM) are Boolean, and often destructive in nature. User only gets the feedback whether or not the Device Under Test (DUT) meets the ESD qualification criterion. Therefore, these tests are usually supplemented with non-

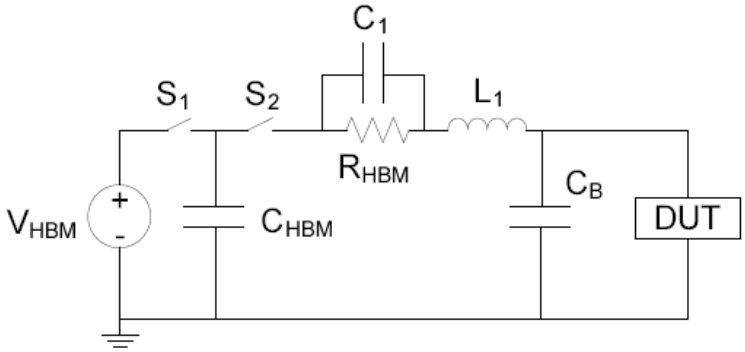



Figure 2.1: Equivalent HBM discharge schematic.

destructive tests to collect additional information for analysis and design optimization. Obviously, detailed information on the ESD behavior of protection elements and circuits are required for their optimization. For such analysis and design optimization, TLP [Maloney85] technique is employed as an alternative and/or supplement to the model based qualifications, even though miscorrelation can exist with respect to HBM test [Scholz09_1]. The TLP technique has gained popularity in the semiconductors industry in recent years due its flexibility and ease of generating pulse with different pulse widths and magnitudes. Later, specific variants of TLP, such as Very Fast TLP (VFTLP) [Gieser98] and Capacitive Coupled TLP (CCTLP) [Wolf05], have been designed specifically to investigate the device response under CMD ESD stress conditions.

The most widely used ESD stress models for system-level ESD qualification is IEC 61000-4-2, simulating the case when a person is touching a pin of a grounded electrical component using a metal tool.

This thesis focuses only on on-wafer component ESD stress without further discussing system-level ESD stress.

### *2.2.1 Human Body Model (HBM)*

It represents the discharge of a standing individual through a pointing finger, which reproduces field failures caused by human handling. It is considered as “the ESD model” because of its common presence in the daily life in a variety of situations. A simple RLC network describes the Human Body Model (Figure 2.1): the static energy is stored in the capacitor $C_{HBM}$ (100 pF) that, once the switch is open, can discharge through the body resistor $R_{HBM}$ (1.5 kΩ) in the device under test. In practice, the HBM acts like a current source with a rise-time of about 10 ns and a current peak of 1.3 A (for 2 kV pre-charge). The HBM tester can be modeled by using a 4 order lumped element model [Verhaege93].

Other parasitic elements ($C_1$ , $L_1$, and $C_B$) are added in order to account for the interaction between the discharge source and the measurement board: their proper

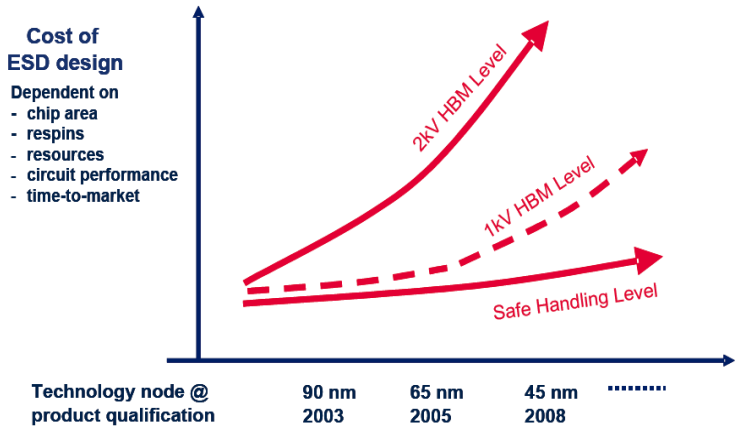



Figure 2.2: The projected cost of ESD requirements as a function of calendar year and the technology node, comparing current customer requirements versus lower recommended target and safe level requirements for handling in an ESD protected area with basic ESD control measures [Duvvury07].

evaluation is critical to assess reproducible stresses. In particular, the test board capacitance $C_B$ is crucial because its discharge occurs at every snapback point in the characteristic, therefore causing an extra stress to the device under stress.

In the semiconductor industry, $\pm$2kV HBM, is very common requirement for general-purpose ICs. However, recently the Industry Council on ESD Target Levels [IndustryCouncil07] has launched a proposal to reduce the safe level from 2 kV down to 1 kV. The reason is that no obvious correlation of Electrical Overstress (EOS) and ESD field returns to HBM levels of 500 V - 2 kV has been observed. Further, the cost for maintaining the 2 kV HBM levels increases exponentially for each new production technology node, see Figure 2.2 [Duvvury07]. This cost is determined by an increased silicon area for ESD, more silicon respins, increasing engineering resources, decreased circuit performance and larger time-to-market. When reducing the level to 1 kV HBM, the costs are reduced drastically. The Industry Council argues that nowadays basic factory control of ESD can guarantee maximum HBM levels of even lower than 500 V. Therefore, we might expect another decrease of the safe levels in the coming years. However, for some special applications, a much higher ESD protection level is required. For example certain automotive applications and smart card ICs require $\pm$15 kV HBM ESD protection.

### *2.2.2 Machine Model (MM)*

It represents the discharge of a sitting individual through a metal/low resistive tool and it reproduces field failures caused by automatic testing. Analogously to the HBM, it

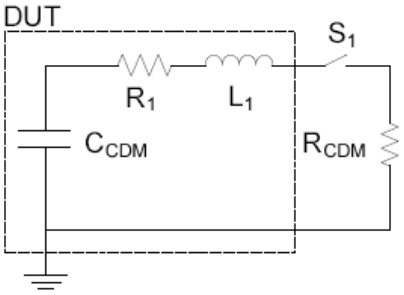



Figure 2.3: Equivalent CDM discharge schematic.

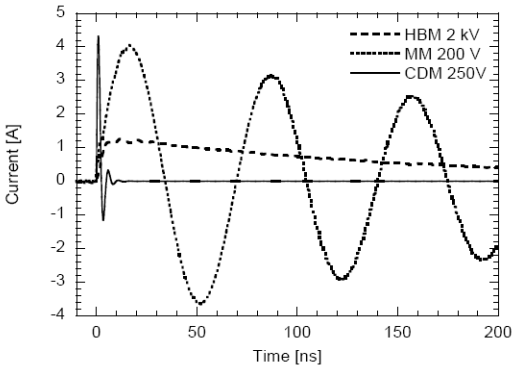



Figure 2.4: Comparison of typical HBM, MM, and CDM discharge currents.

is modeled by an RLC network but with $R_{HBM}$ = 0 Ω. It acts like a current source with a rise-time of about 10ns and a current peak of 3.5A (for 200V stress). Therefore the tester model is the same as in the case of HBM but with different values of the parasitics.

For instance, $C_1$ has now a lower influence because $R_{HBM}$ is very small (Figure 2.1). The major parasitic is the inductance $L_1$ because for its different value both the oscillations period and the current peak will significantly change. Many studies have been carried out on the correlation between HBM and MM tests: it turned out that their comparison is meaningful only if they induce similar failure. In this case, it has been experimentally verified that $V_{MM} \approx 7 \ldots 12.5 \cdot V_{HBM}$.

### *2.2.3 Charged Device Model (CDM)*

CDM represents the discharge of a charged device to ground through a single device pin: it is therefore a complete different stress compared to HBM and MM, aiming to reproduce the real ESD world during handling, working, picking and so on. Contrary to HBM and MM, which have discharges occurring between two pins, CDM is a single-pin

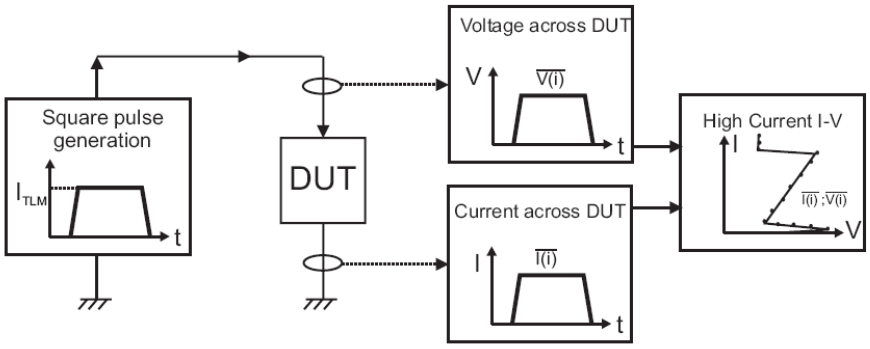



Figure 2.5: Representation of a TLP measurement.

discharge event. The rise-time is about 500 ps and the current peak can easily exceed 7-10 A.

An equivalent electrical schematic reproducing a CDM pulse is shown in Figure 2.3. Note that now the discharge capacitor $C_{CDM}$ is part of the DUT itself. $R_1$ and $L_1$ are typically 10 Ω and 10 nH, respectively. $R_{CDM}$ is the total resistance of the discharge path.

In Figure 2.4, an overlay is shown between the HBM, MM, and CDM discharge currents.

### *2.2.4 Transmission Line Pulse (TLP) System*

TLP testing is a very popular method among the ESD community to assess the robustness of an ESD protection circuits. It simply consists in a square current pulse generator in which the pulse duration and the pulse amplitude are respectively determined by the length of the 50-Ω transmission line and by the pre-charging of the line itself, respectively. With increasing the pulse amplitude and averaging the corresponding clamping voltage across a user defined window in the stable region of the pulse it is possible to deduce the high current ESD-like $I(V)$ characterization in the relevant ESD domain (Figure 2.5). This unveils the trigger ($Vt_1$) and the holding voltages ($V_h$) of the device under test. Furthermore, after each zap it is possible to fully characterize the DUT by immediately recognizing eventual degradations and therefore showing the maximum ESD stress handling capability.

Standard TLP has a typical pulse duration of 100 ns and a rise time between 2 ns and 10 ns. The 100 ns pulse duration was chosen, such that similar TLP and HBM current levels yield roughly the same energy content.

### *2.2.5 Very Fast TLP (VFTLP)*

VFTLP has pulse widths of 1-5 ns and a rise time of typically 200 ps. As such, VFTLP has similar characteristics as CDM and hence correlates better to CDM than standard TLP. However, no one-to-one correlation exists, since VFTLP is a two-pin test and CDM a single pin event. Also CDM is package dependent, whereas VFTLP is mainly used on-wafer. Still, VFTLP can be useful for transient device analysis and modeling in the CDM time-domain. A rough correlation exists between VFTLP and CDM according to [CDM08], which is about 90 V/A for small packages and 45 V/A for large packages based on the CDM peak current values.

### *2.2.6 HBM-IV*

In this section, a new ESD measurement system is developed which uses HBM pulses to obtain both quasi-static and transient device information. The benefit over TLP is that real-life ESD pulses are used instead of artificial rectangular pulses. HBM-IV is used in this thesis besides TLP to evaluate the ESD robustness of different devices.

Conventional HBM testers only yield pass-fail results. The obtained failure level shows how much ESD stress a device is able to withstand. However, no information of the device response under such ESD stress can be obtained and often miscorrelation is observed between TLP and HBM test results. By equipping the HBM test system with a voltage and current probe, the test system transforms into a research tool, rather than being limited to a product qualification tool. With such a setup, the voltage and current in time during a HBM stress are captured. For each time point of the obtained waveform data, current is plotted over voltage, thereby forming the HBM IV curve. An example is shown in Figure 2.6, where a diode is stressed with 1000 V HBM. A HBM IV curve reveals three distinct regions: the device turn-on (A), an oscillating part around the peak current (B) and a stable linear part (C) during the falling HBM current. The first two parts show the transient device behavior under ESD stress, whereas the latter represents the quasi-static device behavior. With one HBM pulse it is possible to characterize simultaneously the transient and quasi-static device behavior of a device under HBM stress conditions. In case of TLP, the measurement of an IV curve, which is built-up point by point, can take easily a couple of minutes. On contrary, a single HBM-IV pulse yields the same IV curve within less than a second, and on top yields additional transient information. Of course, some amount of step stressing is still required to determine the HBM failure level.

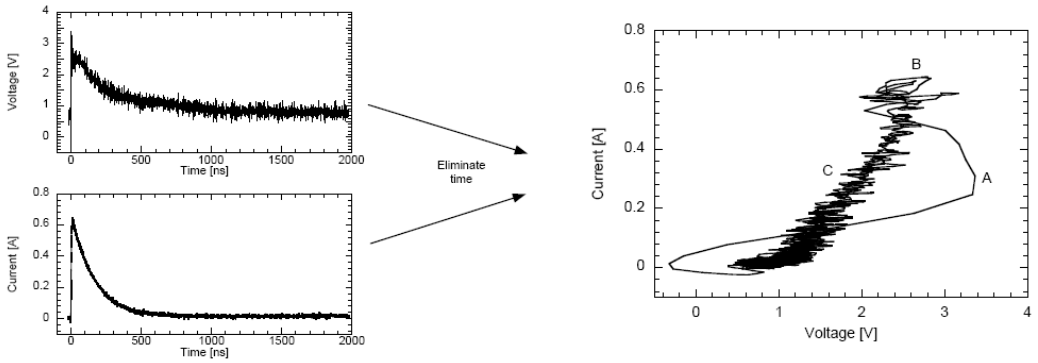



Figure 2.6: HBM IV curve obtained from a diode for a HBM pre-charge voltage of 1000 V.

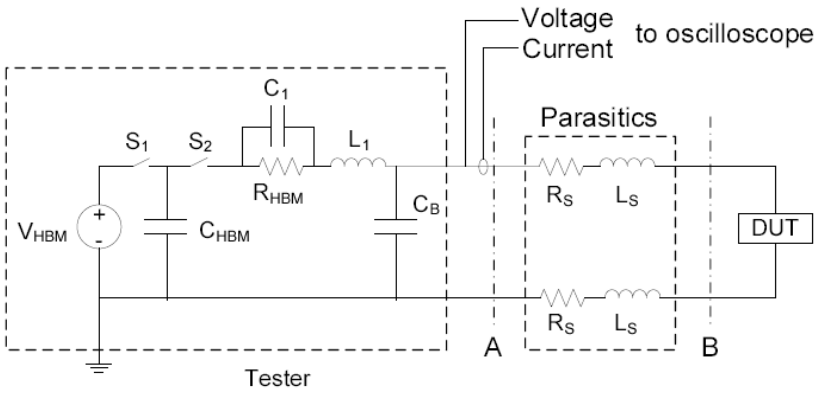



Figure 2.7: Electrical schematic of a HBM tester including the system parasitics. The dashed lines indicate the measurement planes A and B.

Each HBM voltage and current measurement is very sensitive to parasitic elements due to its fast, high-current nature. An electrical schematic showing the most important system parasitics of the HBM tester is shown in Figure 2.7. Voltage and current are measured as close as possible to the needle, measurement plane A in Figure 2.7. However, these waveforms are distorted due to the needle parasitics, $R_s$ and $L_s$ (measurement plane B in Figure 2.7). These parasitic elements cause an additional voltage drop around the current peak and the linear region of the HBM IV curve, C in Figure 2.6, which needs to be calibrated out. Also the current transformers, which are used to measure the discharge current, are usually limited in their bandwidth. Commercially available current transformers, which are suitable for on-wafer HBM measurements, have a bandwidth between 25 kHz and 2 GHz. The limitation for lower frequencies distorts the measurement of the falling part of the current waveform and needs to be corrected. Due to the limited power of the signal spectrum at high frequencies

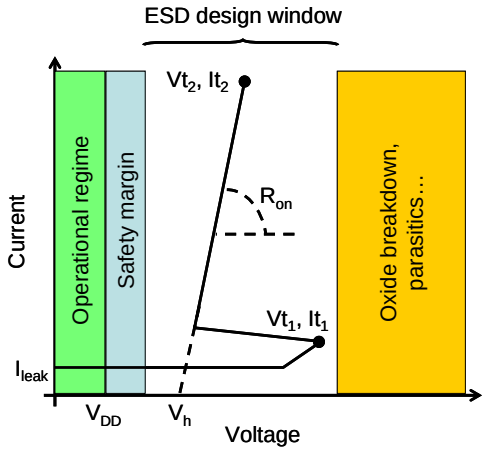



Figure 2.8: ESD design window.

of the voltage and current, additional filtering is required in the frequency domain. The full calibration method is described in detail in [Scholz07_1] [Scholz07_2] [Scholz09].

## 2.3 On-Chip Protection Against ESD: Principles and Devices

There are many possible candidates that can act as a single element protection structure, depending on the technology, the applications and the design constraints. Single protection elements submitted to an ESD event are forced to work under high injection conditions [PhDBoselli]. It is therefore important to review the relevant aspects of the main protection devices under these conditions, with particular emphasis on the principle of the "snapback conduction mode" of the nMOS transistors.

### *2.3.1 Grounded-Gate nMOS*

In CMOS technology the nMOS transistors (in grounded gate configuration ggnMOS, with all electrodes grounded with exception of the drain) are widely used as protection elements because they exploit a very appealing characteristic when subjected to an ESD event: the snapback conduction mode (Figure 2.8). This mode is characterized by low voltage and low on-resistance (2-5 Ω), which imply low power dissipation. The snapback conduction mode exploits the parasitic bipolar action intrinsic in the structure and is reached in this way: when a positive pulse (ESD) is applied to the drain junction ($n^+$/p substrate) the device is forced into a high impedance state (reverse biasing) until the breakdown voltage ($V_{BR}$) is reached (Figure 2.9).

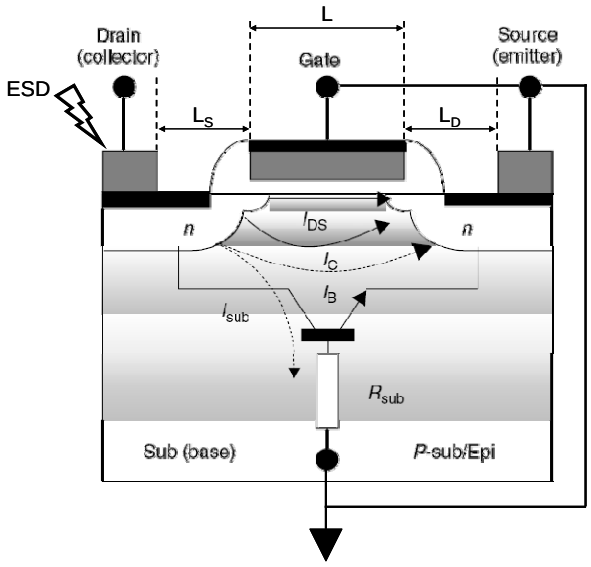



Figure 2.9: Art impression of the mechanisms turning-on the bipolar parasitic transistor in a ggnMOS.

Hole-electron pairs are generated inside the depletion region, because of the high value of the electric field, electrons are collected at the drain contact, while the holes are collected at the grounded substrate contact, increasing the local substrate potential with respect to the grounded source junction. When this local potential difference is high enough to forward bias the source-substrate junction, electrons are injected from the source (acting as the emitter of the parasitic npn) to the drain.

If this parasitic bipolar structure (Drain = Collector, Substrate = Base, and Source = Emitter) has a forward gain high enough, it can provide its own base current, keeping the structure self-biased. Once the bipolar structure turns on, the voltage can decrease from its maximum value ($Vt_1 \approx V_{BR}$) to a minimum value ($V_h$) because there is no need anymore to force the drain junction in deep breakdown to sustain the forced current. Notice that between the triggering voltage ($Vt_1$) and the holding voltage ($V_h$) there is a Negative Differential Resistivity (NDR) region that is not stable (or, in other words, it is not possible to bias the device in these points) but it simply represents the transition between two stable biasing points (high and low impedance).

Once the holding voltage is reached, the forced current is entirely sustained by the parasitic bipolar transistor (snapback conduction mode). In this region the resistivity becomes once again positive (the on-resistance, which assesses the shunting capabilities of the device) because conductivity modulation of the substrate takes place, implying that a larger substrate current is needed to keep the parasitic bipolar device on. Still, it has to be noted that not all the substrate of the bipolar structure acts as a base and, similarly, only a portion of the collector junction is forward biased. By further increasing the current, self-heating effects come into play, increasing the internal temperature.

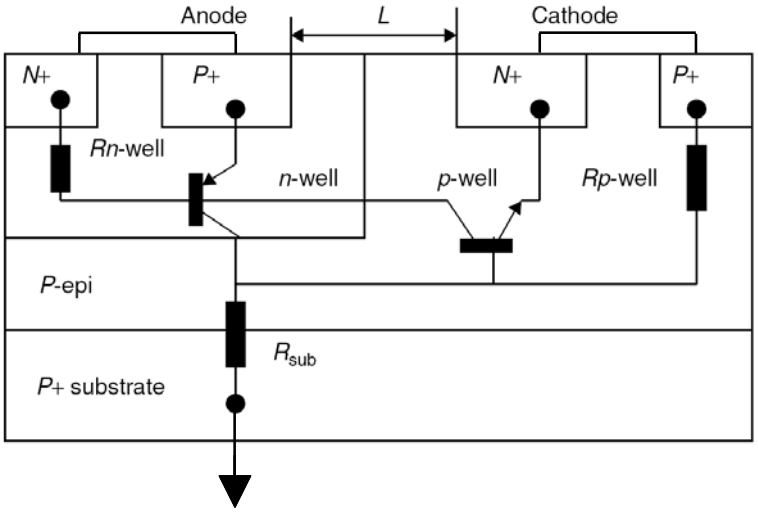



Figure 2.10: Cross-section of a SCR (pnpn structure).

When this reaches the melting point of silicon (1685 K), a change of phase might take place by leading to an irreversible change of the device characteristics. This phenomenon, causing the destruction of the device, is called "second (or thermal) breakdown" ($Vt_2$) and its relative current ($It_2$) is considered as the onset of the irreversible damage. Given its crucial importance, the ggnMOS has been object of intensive studies, in particular with respect to the impact of design parameters ($L_D$ distance, L, dynamic coupling, multi-fingers layout) and process parameters (LDD option, salicide, P-well profile) in order to maximize the performances and to generate reliable models for compact modeling simulations.

### *2.3.2 Silicon Controlled Rectifier (SCR)*

The Silicon Controlled Rectifier (SCR) consists of a pnpn structure (Figure 2.10). It can be seen as a npn and a pnp transistor configured such that the base of the pnp (n-well) is also the collector of the npn and, on the other way around, the base of the npn (p-well) is also the collector of the pnp. When used as protection device it is configured as a two terminals device: the cathode and the n-well are grounded whereas the stress is applied to the anode, which is tied to the p-well. This ensures that during normal operating conditions, latch-up will not take place. When an ESD stress is applied to the anode, the n-well/p-well junction is forced into reverse biasing until it reaches the breakdown ($Vt_1$). The generated holes are collected at the p-well contact while biasing the base of the lateral npn and, therefore, turning it on. At this point the electron current injected into the n-well will bias the base of the vertical pnp.

Therefore, there is no need anymore of the current generated by the avalanche of n-well/p-well to keep on the vertical pnp: the externally seen voltage decreases (and, hence, we have a NDR region exactly as in Figure 2.8) until a minimum is reached ($V_h$). Now the device has a $R_{on}$ in the order of 1-2 Ω, because the main voltage drop is across the region between the anode and the cathode, which is conductivity modulated. Such a low $R_{on}$ turns in an extremely low power dissipation leading to a very high ESD robustness.

Nevertheless, the triggering voltage $Vt_1$ corresponds to the breakdown of the n-well/p-well junction, depending on the n-well profile and substrate doping level. It must be lowered in order to obtain good protection: both design and process alternatives (MLSCR and LVTSCR) have been proposed to do that [Ming-Dou Ker05].

### *2.3.3 Lateral npn*

Almost all what was said about the ggnMOS applies to the lateral npn transistors ($R_{on}$ = 2-5 Ω) and the main difference between the two structures consists in the presence of a field oxide instead of the gate. This has beneficial effects in terms of gate edge problems and linear scaling with the width. The main drawback is that the base of the transistor (LOCOS) might be very long leading to a higher $Vt_1$. Lateral pnp transistors have higher on-resistance ($R_{on}$ = 30 Ω).

### *2.3.4 Diodes*

Simple diodes can be used as clamping elements during ESD events in forward biasing mode, in which they show a low on-resistance (10 Ω) and a low triggering voltage $Vt_1$ . On the other hand, in reverse biasing mode they are bad clamping elements because of their high on-resistance (100 Ω), which leads to a large power dissipation.

### *2.3.5 Protection Networks*

In few cases it is possible to guarantee the needed protection with single protection elements. More often a protection network is built up to exactly tailor to the ESD requirements in terms of triggering voltage ($Vt_1$) and holding voltage ($V_h$). The strategy to design a protection network can be quite complex. In Figure 2.11 a basic protection network is shown: two-stages are separated by an isolation resistor. The first stage (the primary element) will shunt most of the current during an ESD event and for this reason the potential candidates for this role are often the devices with the lowest on resistance (ggnMOS and SCR). Still, a protection is needed in the early phase of the ESD stress when the primary element has not been activated yet. This is the function of the second stage, normally consisting in a small ggnMOS or a diode. The resistive element, while the initial ESD stress is clamped by the secondary element (protecting the eventual gate oxide

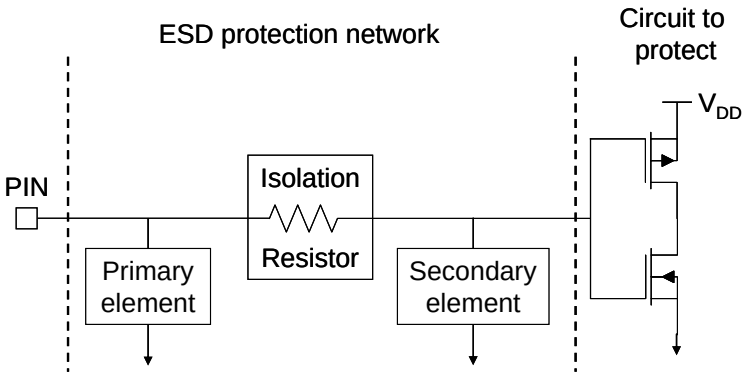



Figure 2.11: Generical two-stages protection scheme.

from breakdown), acts as a load enabling the switching-on of the primary protection element.

## 2.4 Conclusions

In this chapter, first an overview was given of the main semiconductors devices that can provide ESD protection circuit in CMOS technology. Secondly, an overview was presented of the different standard component-level ESD stress models. TLP and its variants were shown to yield additional device information besides only pass-fail results. Enhanced characterization and analysis techniques were demonstrated based on HBM. A very powerful method called HBM-IV was demonstrated, which could yield besides the exact same quasi-static device parameters as obtained from TLP also transient turn-on information, in only a fraction of the measurement time compared to TLP.

# Chapter 3

# ESD in Ultrathin Body SOI MOSFETs

The ESD sensitivity of fully depleted SOI MOSFETs with ultra-thin silicon body and ultra-thin gate oxide is studied. An original and detailed electrical analysis is carried out in order to investigate the degradation of the electrical DC parameters and classify the observed failure modes and mechanisms. The impact of device geometry and strain engineering is also analyzed.

## 3.1 Introduction

CMOS technology is now entering a phase where simple shrinking is no longer sufficient to guarantee the performance gains required from each new generation of devices. Alternative materials and structures are required. On one hand, SOI technology is now becoming mainstream thanks to its superior control of Short-Channel Effects (SCE) and promise for scalability [Celler03]. According to the 2008 ITRS [ITRS08], UTB FD SOI MOSFETs [Choi00], together with FinFET devices [Choi04], are the main candidates to continue with CMOS scaling below the 22-nm technological node. On the other hand, mobility-enhancing techniques are used to improve transistor performance. Uniaxial and/or biaxial strain in the channel through the use of stressor layers and/or substrate engineering are examples of how mobility improvements can be obtained [Takagi08].

For SOI, both the lateral (Shallow Trench Isolations, STIs) and vertical electrical isolation (buried oxide, BOX) largely prevent the heat dissipation during ESD events [Ramaswamy95] [Amerasekera02]. The shrinking of the silicon film further reduces the

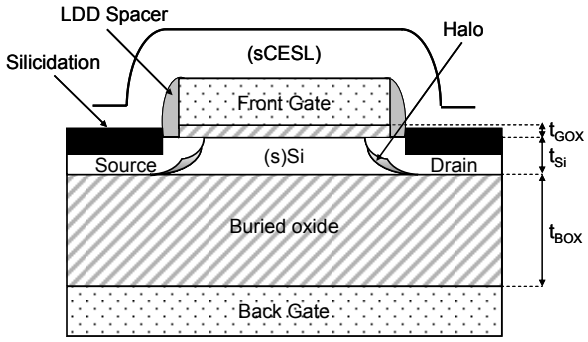



Figure 3.1: Schematic cross-section of the devices under study (not to scale).

ESD robustness [Thijs09], making the silicon-body thickness one of the main restrictions for ESD protection structures in advanced SOI CMOS ICs.

In this chapter, we will investigate the ESD sensitivity and the degradation of the electrical DC characteristics of UTB FD SOI MOSFETs with ultra-thin gate oxide, including the impact of the device geometry and to the impact of strain engineering. The focus will be on the devices that need to be protected from ESD, rather than on the protection structures themselves.

## 3.2 Experiments and Devices

N-channel FD SOI MOSFETs have been manufactured in a 65 nm IMEC CMOS process. The devices feature 1.5 nm thermal silicon oxynitride (SiON) as gate dielectric, 15 nm undoped top silicon layer ($t_{Si}$), 150 nm thick BOX, 25 nm Si source/drain (S/D) elevation prior to Highly Doped Drain (HDD) formation, and Ni silicidation. The operating voltage ($V_{DD}$) is 1 V. Devices with 0.25 µm minimal gate width ($W$) and 0.15 µm minimal gate length ($L$) were used. Polysilicon was used as gate material, inducing a negative front-gate threshold voltage ($V_{TH,FG}$) for NMOSFETs. Final devices will feature metal gates with proper workfunctions to adjust $V_{TH,FG}$. Three variants have been processed (Figure 3.1):

1) SOI: reference devices processed on SIMOX substrates;
2) strained Contact Etch Stop Layer (sCESL+SOI): obtained by depositing (in one step) an additional 100 nm tensile nitride (intrinsic stress 800 MPa) that generates additional uniaxial strain along the channel;
3) strained SOI (sSOI): fabricated using wafer bonding and a donor wafer with a Si-capped $Si_{0.8}Ge_{0.2}$ Strain Relaxed Buffer (SRB) that generates additional biaxial strain along the channel.

More technological information can be found in [Augendre05].

The devices were stressed in grounded-gate configuration by means of a solid-state pulser (TLP-like) at wafer level with square-pulse width of 100 ns and rise time of 5 ns. To measure the failure voltage ($Vt_2$) and the failure current ($It_2$), we applied a sequence of pulses to the drain terminal with increasing peak voltage (starting at $V_{DS} = 1$ V and increasing by 100 mV every step, while keeping the front-gate and source terminals grounded). After each pulse a full set of device DC characteristics was measured:

a) the front-gate current versus the front-gate voltage ($I_G$-$V_{GS}$) with $V_{DS} = V_{BS} = 0$ V;
b) the drain current versus the front-gate voltage ($I_{DS}$-$V_{GS}$), for different back-gate voltages while keeping $V_{DS} = 25$ mV;
c) the drain current versus the drain voltage ($I_{DS,front\text{-}channel}$-$V_{DS}$), for different $V_{GS}$ while keeping $V_{BS} = 0$ V;
d) the drain current versus the drain voltage ($I_{DS,back\text{-}channel}$-$V_{DS}$), for different $V_{BS}$ while keeping $V_{GS} = 0$ V; and
e) the drain leakage current ($I_{DS,leakage}$) at different drain voltages and $V_{GS} = 0$ V.

To perform both ESD stresses and four-terminals DC measurements on the Device Under Test (DUT), an RF switch was used to switch the gate terminal between the ground loop and a Source Monitor Unit (SMU) of the parameter analyzer (HP4156C). During the ESD stresses, the gate terminal was shorted to the grounded source terminal by means of a ground loop similar to the one usually used in the TLP stress systems for the source, which ensures very low impedance to the ground. To measure the device DC characteristics, the gate terminal was connected to the parameter analyzer.

More than 150 devices have been tested for this work.

## 3.3 ESD Effects on SOI MOSFETs

Destructive ESD events at the drain terminal give rise to either or both of two distinct phenomena: gate-oxide (GOX) breakdown and/or creation of an additional conductive path between source and drain, which is called “filament”. Figure 3.2 and Figure 3.3 illustrate these two phenomena through electrical failure signatures.

GOX breakdown during ESD can occur either in the central gate area (over the conducting channel), or in the overlap regions between gate and source/drain extensions (Figure 3.4). In our samples, the GOX breakdown occurs near the overlap region between the gate and drain extension. The GOX breakdown is a statistical process and is triggered when a critical density of traps is reached in the GOX [Degraeve98]. The breakdown current (at $V_{GS} = 1$ V) measured in our devices ranges from few hundreds of nA to hundreds of μA. The GOX breakdown can be of different type and magnitude. The hard breakdown shows a nearly ohmic current-voltage relation (Figure 3.2.a), while the soft

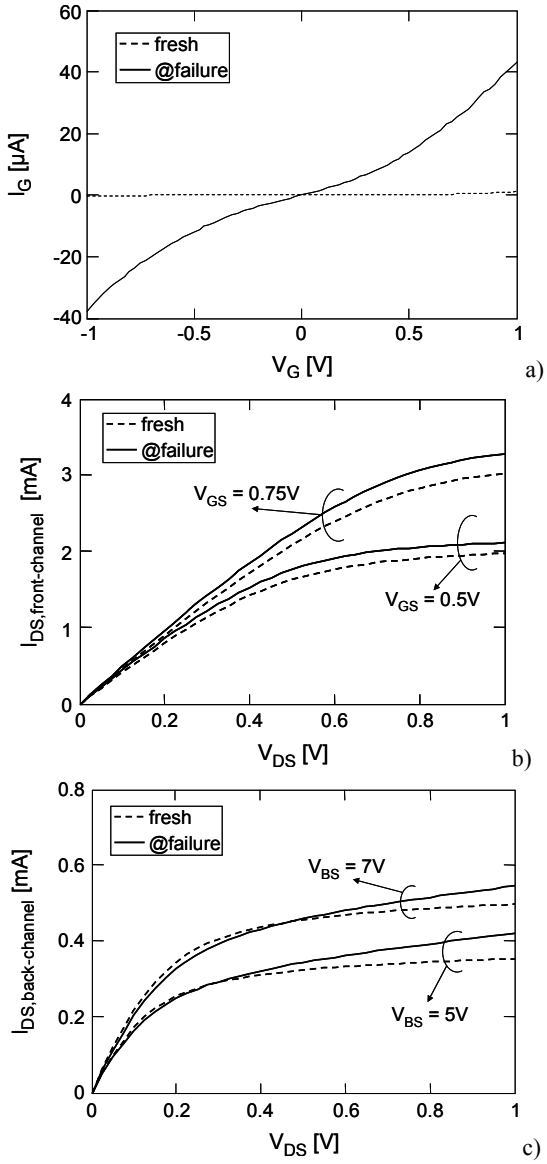



Figure 3.2: a) $I_G$-$V_G$ ($V_{DS}$ = $V_{BS}$ = 0 V), b) front- and c) back- channel $I_{DS}$-$V_{DS}$ ($V_{BS}$ = 0 V and $V_{GS}$ = 0 V, respectively) for a conventional FD SOI MOSFET ($W/L$ = 10 µm/0.25 µm). The gate oxide hard breakdown occurred, resulting in a large $I_G$ increase and $I_{DS}$ increase that depends on both $V_{GS}$ and $V_{BS}$.

breakdown displays a power-law characteristic (Figure 3.3.a). Such different behaviour is due to the different conduction mechanism for hard and soft breakdowns [Kaczer07]. This is related to the types of oxide traps, the free energy levels and the different number of traps in the percolation path, or a different location of the trap centroid between anode and cathode [Pompl01].

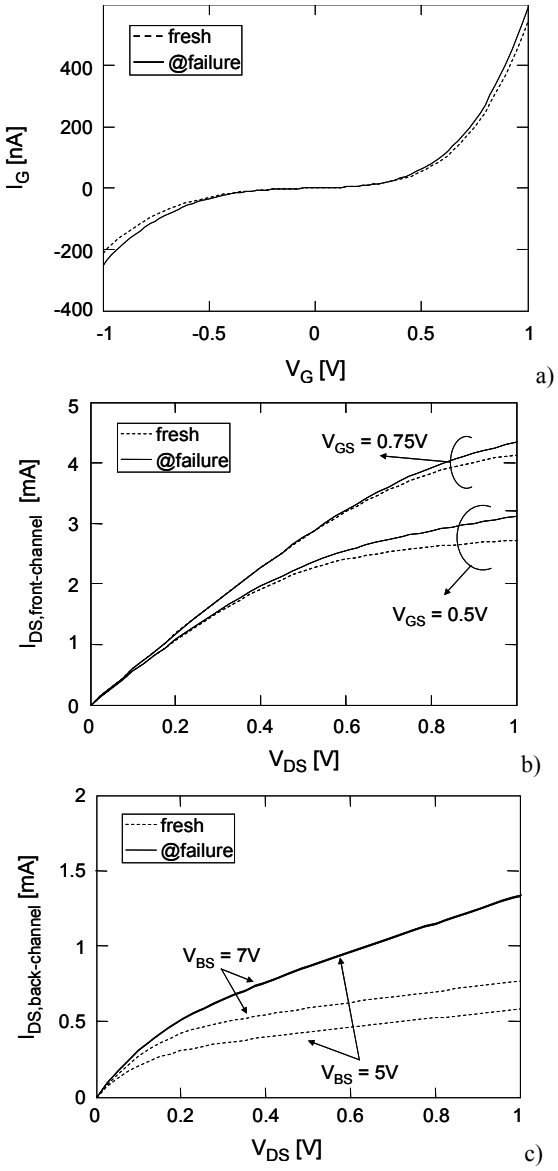



Figure 3.3: a) $I_G$-$V_G$, b) front- and c) back- channel $I_{DS}$-$V_{DS}$ (at the same bias conditions reported in Figure 3.2) for a conventional FD SOI MOSFET ($W/L$ = 10 μm/0.16 μm). Both the gate-oxide soft breakdown and filamentation near the gate oxide/silicon interface occurred, resulting in back-channel $I_{DS}$-$V_{DS}$ independence of $V_{BS}$.

Figure 3.3.b and Figure 3.3.c show the source-drain filament formation, possibly due to silicon and/or silicide being melted by Joule heating [Amerasekera02]. The measured filaments resistance ($R_{filament}$), extracted from the $I_{DS,front-channel}$-$V_{DS}$ and $I_{DS,back-channel}$-$V_{DS}$ curves, is given by:

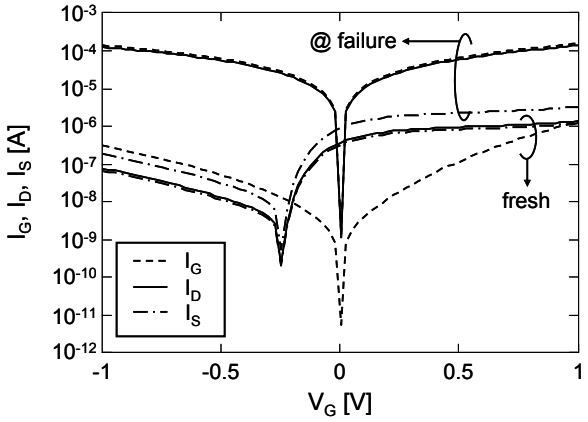



Figure 3.4: Gate, source, and drain currents versus gate voltage ($V_{DS}$ = $V_{BS}$ = 0 V) before ESD stress and after failure for a conventional FD SOI MOSFET ($W/L$ = 10 μm/0.25 μm). After failure, a significant increase in the gate and drain leakage currents (≈ 100 μA) is observed, indicating the occurrence of GOX breakdown close to the overlap region between the gate and drain extension

$$R_{filament} = \left( \left. \frac{\partial I_{DS}}{\partial V_{DS}} \right|_{V_{GS}, V_{DS}} \right)^{-1}_{@\ failure} \tag{3.1},$$

$R_{filament}$ may be as low as a few hundreds of Ohms.

The two mechanisms that can be distinguished based on the different electrical signature as a function of the applied bias are

1. the current due to GOX breakdown depends on the field across the GOX;
2. the current due to a filament between source and drain mainly depends on $V_{DS}$ and may be independent of either or both the $V_{GS}$ and $V_{BS}$. In particular, if the drain/source current is independent of both $V_{GS}$ and $V_{BS}$, the filament may be located in the whole silicon body. While, if the drain/source current is independent only of $V_{BS}$ ($V_{GS}$), the filament may be located near the GOX/silicon (silicon/BOX) interface (Figure 3.3).

A low-value resistor is used to model the filament, whereas a voltage-dependent current source is more appropriate to account for the GOX breakdown conduction. In short, ESD events can induce either GOX breakdown (Figure 3.2) or a combination of GOX breakdown and filament formation (Figure 3.3).

## 3.4 Failure Criterion

The device failure is usually taken as the amplitude of the pulse at which a large change occurs (i.e. 10x) in the leakage current of the terminal subjected to the ESD. A full set of DC measurements, after each ESD step, permits to detect also any parameter degradation before the destructive ESD event and (based on the consideration made in the paragraph 3.3) the failure mechanism. For these reasons, it is useful to know how the GOX is damaged, since Stress-Induced Leakage Current (SILC), progressive, soft, and hard GOX breakdowns can occur in ultra-thin GOX (< 2.5 nm) under ESD stresses [Salman03] [Ille06] [Ille07].

To develop a failure criterion independent from the device size, we consider the following DC parameters:

1. $I_{G,ON}$: the gate current at $V_{GS}$ = 1 V and $V_{DS} = V_{BS}$ = 0 V;
2. $I_{G,OFF}$: the gate current at $V_{GS}$ = -0.75 V and $V_{DS} = V_{BS}$ = 0 V; and
3. $I^*_{DS,OFF}$ (= $I_{DS,OFF}/L$): drain current normalized to the gate length at $V_{GS}$ = -0.75 V, $V_{DS}$ = 25 mV, and $V_{BS}$ = 0 V. $V_{GS}$ was chosen -0.75 V instead of 0 V because $V_{TH,FG}$ varies between -0.3 V and -0.2 V, depending on the device geometry and strain level. The drain current is normalized to the gate length since the filament resistance is (in first approximation) directly proportional to $L$ and does not depend on $W$.

Notice that, contrary to $I^*_{DS,OFF}$, the choice of the bias condition for $I_{G,ON}$ and $I_{G,OFF}$ is not related to the fact that the samples have $V_{TH,FG} < 0$ V, but only to monitor the gate current in the inversion ($V_{GS}$ = 1 V) and accumulation ($V_{GS}$ = -0.75 V, similar results are obtained also for $V_{GS}$ = -1 V) regions.

The information about the GOX degradation and breakdown is given by the $I_{G,ON}$ variation ($\Delta I_{G,ON}$) before and after stress. After the first ESD pulses, $\Delta I_{G,ON}$ is below 300 - 400 pA (Figure 3.5 and Figure 3.6), so the first threshold for detection of events in $\Delta I_{G,ON}$ can be set about ten times this value (3 – 4 nA). Concerning more severe GOX events, the soft breakdown experiences a $\Delta I_{G,ON}$ increase between 10 nA and 1 µA, while the hard breakdown exhibits a larger increase in $\Delta I_{G,ON}$ (> 1 µA). Furthermore, when $\Delta I_{G,ON}$ > 100 nA, there is also an increase in absolute value of the $I_{G,OFF}$ variation ($|\Delta I_{G,OFF}|$), which causes a large increase in $I^*_{DS,OFF}$ variation ($\Delta I^*_{DS,OFF}$ > 10 µA/µm) (Figure 3.5). In other words, when a hard or severe soft GOX breakdown occurs, it is detected also from $\Delta I^*_{DS,OFF}$, since a non-marginal amount of current is injected from the gate to the drain biasing negatively the gate electrode. However, some MOSFETs affected by progressive and/or non-severe soft breakdown ($\Delta I_{G,ON}$ < 100 nA) show a large increase in $\Delta I^*_{DS,OFF}$, although $\Delta I_{G,OFF}$ is not so large to induce this strong increase in $\Delta I^*_{DS,OFF}$ (Figure 3.6). This “odd” behavior is due to the filament formation between source and drain, as confirmed by the $I_{DS}$-$V_{DS}$ analyses at front- and back-channel transistors (Figure 3.3).

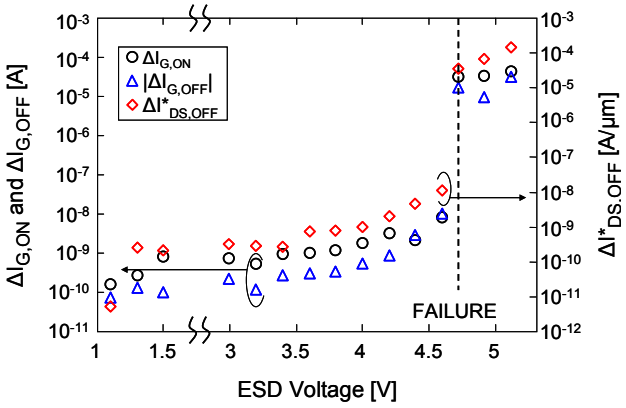



Figure 3.5: $\Delta I_{G,ON}$ ($V_{GS}$ = 1 V and $V_{DS}$ = $V_{BS}$ = 0 V), $|\Delta I_{G,OFF}|$ ($V_{GS}$ = -0.75 V and $V_{DS}$ = $V_{BS}$ = 0 V), $\Delta I^*_{DS,OFF}$ ($V_{GS}$ = -0.75 V, $V_{DS}$ = 25 mV, and $V_{BS}$ = 0 V) as a function of the measured ESD voltage for a conventional FD SOI MOSFET (W/L = 10 μm/0.25 μm). The sample experiences a progressive gate-oxide breakdown, followed by the hard rupture.

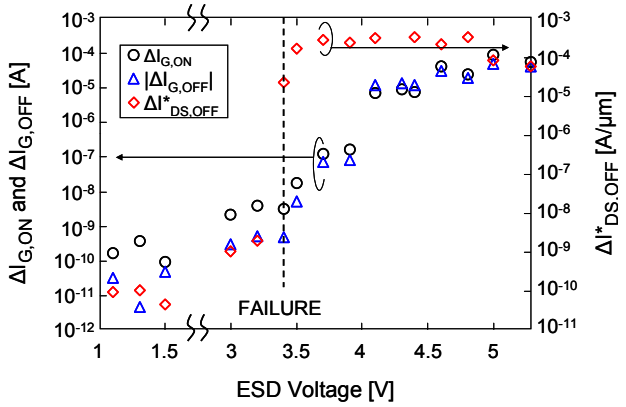



Figure 3.6: $\Delta I_{G,ON}$, $|\Delta I_{G,OFF}|$, and $\Delta I^*_{DS,OFF}$ (at the same bias conditions reported in Figure 3.5) as a function of the measured ESD voltage for a conventional FD SOI MOSFET (W/L = 10 μm/0.16 μm). The sample experiences a small increase in the gate current (indicating a soft gate-oxide breakdown) and a larger increase of $I^*_{DS,OFF}$, indicating the filament formation occurrence.

Based on these considerations, the destructive device failure was taken as the amplitude of the pulse at which either $\Delta I_{G,ON}$ > 10 nA or $\Delta I^*_{DS,OFF}$ > 10 μA/μm, whichever took place first. When the $\Delta I^*_{DS,OFF}$ condition is met, the other parameters ($\Delta I_{G,ON}$ < 1 μA and $|\Delta I_{G,OFF}|$ < 100 nA) are checked to detect a possible filament formation. Other failure criteria can be used. For instance, taking into account also any change in the $V_{TH,FG}$ shift and in the transconductance ($g_m$) drop, whichever took place first. However, such failure criterion can be too severe, especially if only a modest degradation occurs, and does not give any indication about the occurred failure mechanism.

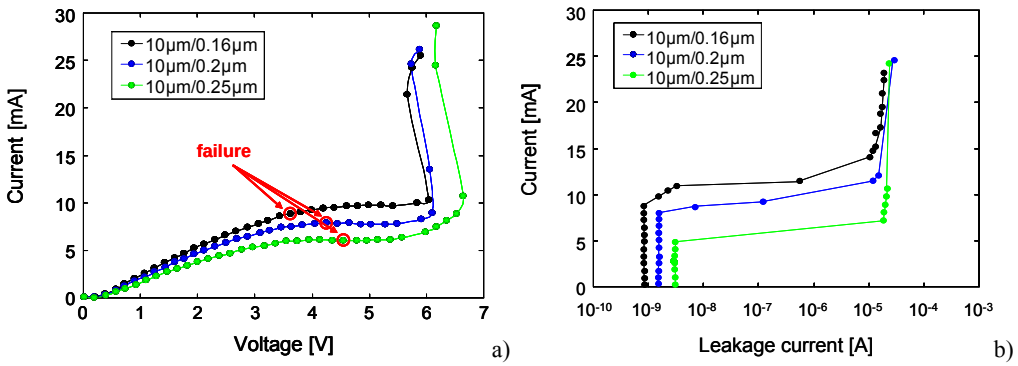



Figure 3.7: a) TLP IV curves and b) leakage current evolutions for N-channel FD SOI MOSFETs with $W/L$ = 10 µm/0.16 µm, 10 µm/0.2 µm, and 10 µm/0.25 µm, respectively. A sequence of pulses was applied to the drain terminal with increasing peak voltage, while keeping the front-gate and source terminals grounded.

## 3.5 Geometry Dependence

In this paragraph, the impact of gate length and width on the failure current and voltage of conventional SOI MOSFETs is investigated.

### *3.5.1 Gate-Length Dependence*

Figure 3.7 shows the TLP IV characteristics for SOI MOSFETs with $W$ = 10 µm and different $L$. Even though the devices are stressed in GG configuration, they start to conduct as soon as a positive voltage is applied because of $V_{TH,FG} < 0$ V. Two regions can be separated. In the first one (voltage < 2.5/3 V, depending on L), the current increases linearly with increasing voltage. In the second region (voltage > 2.5/3 V, depending on $L$), the current saturates due to velocity saturation and self-heating. Figure 3.7 also shows a qualitative scaling with $L$: $It_2$ decreases while $Vt_2$ increases with increasing $L$. However, this scaling is limited by sub-linear scaling of current with L and saturation of the current at higher voltages.

Figure 3.8 shows $It_2$ normalized to $W$ ($It_2/W$) as a function of $L$ for different strain levels, while Figure 3.9 shows $Vt_2$ as a function of $L$ for SOI MOSFETs with different W. When L is increased, $Vt_2$ increases monotonically (regardless of $W$), while $It_2/W$ decreases monotonically, regardless of the strain level.

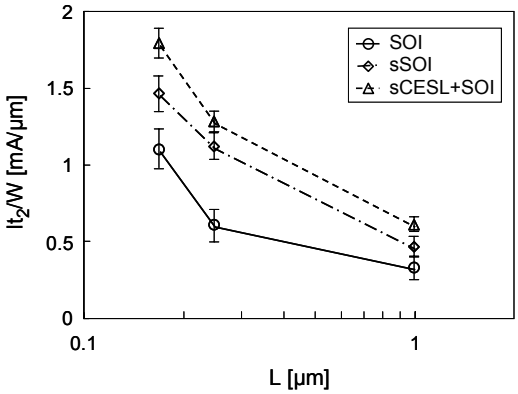



Figure 3.8: Failure current ($It_2$) normalized to the gate width ($W$) as a function of the gate length for FD SOI MOSFETs with $W$ = 10 µm stressed in GG configuration.

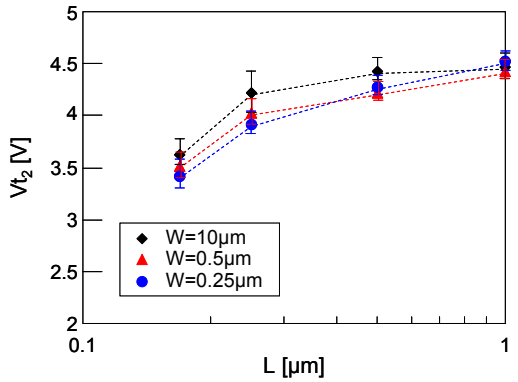



Figure 3.9: Failure voltage ($Vt_2$) as a function of the gate length ($L$) for conventional FD SOI MOSFETs with different gate widths ($W$) stressed in GG configuration.

Even though the devices are stressed in GG configuration, a MOS conduction exists on the top of the parasitic-bipolar conduction because of $V_{TH,FG} < 0$ V. This improves the current uniformity at high current levels [Amerasekera02] and the increase in L mainly induces only additional self-heating, reducing $It_2$ and increasing $Vt_2$. A secondary effect, enhanced by $V_{TH,FG} < 0$ V, is that when a large voltage is applied to the drain, while keeping the other terminals grounded, a significant amount of hot carriers flows through the channel generating hot-carrier-induced degradation. Clearly, devices with short $L$ (at constant drain bias) present larger electric field and hence are more sensitive. Furthermore, during the ESD discharge, the device region more prone to degradation is the one close to the drain, as extensively investigated in [Groeseneken01] [Aur88].

### *3.5.2 Gate-Width Dependence*

Figure 3.9 shows that $Vt_2$ decreases with decreasing $W$ for short $L$ (< 0.25 μm), while $Vt_2$ is almost independent on $W$ for long $L$ (≥ 0.25 μm), where the Channel-Hot-Carrier (CHC) effects are negligible. Such trend can be explained by means of the similarity between drain ESD events and CHC stresses, which show an enhanced degradation on narrow width [Li03]. The reason can be found in a different electric field distribution between wide and narrow devices that makes wider transistors more robust to the CHC effects.

The high-current characteristics of narrow MOSFETs can not be measured with the TLP test setup. This is because the ESD current, which is in the order of some hundred of μA's in such devices, is not high enough to be measured by a TLP system (current probe). Therefore, we can make only some conjecture about the $It_2$ dependence on W.

An improvement in $It_2$ due to the MOS conduction (induced by $V_{TH,FG} < 0$ V) on the top of the parasitic-bipolar conduction is expected for wider MOSFETs. Such amelioration is usually observed for low values of gate bias (< 1 V) [Oh02] [PhDOh], similarly to this case. Single-finger devices, as in this case, can be affected by isothermal current instability which is initiated by impact ionization under high field conditions [Vashchenko08]. Locally, a high Joule power level is generated, which results in a filament formation and finally local burnout. This means that even within a single wide finger there can exist a degree of non-uniformity. Therefore, an improvement in $It_2$ will be apparent in wide devices where the ESD current is strongly non-uniform. On the other hand, $It_2$ will be degraded with gate bias for narrow MOSFETs, where ESD current is known to conduct nearly uniformly [Oh02] [PhDOh].

## 3.6 Impact of Strain

The TLP IV curves for UTB FD SOI MOSFETs with aspect ratio $W/L$ = 10 μm/0.16 μm and different strain levels are shown in Figure 3.10. Two regions can be observed. In the first part of the stress, where the drain current increases linearly with increasing voltage, the sSOI devices exhibit the largest amount of current and the lowest on-resistance ($R_{on}$) compared to the other samples. These are because sSOI transistors have the highest mobility and lowest $V_{TH,FG}$. The lowest amount of current and largest $R_{on}$ is observed for SOI MOSFETs. This is due to the lower mobility (but the same $V_{TH,FG}$) of SOI devices with respect to sCESL+SOI ones. In the second part of the stress, (where the voltage is larger than 2.5/3 V) the current shows a different behavior depending on the strain level. For SOI MOSFETs, the current saturates with increasing voltage. On the contrary, for sSOI and sCESL+SOI devices, the current saturation does not occur and the failure happens before the turn-on of the parasitic BJT, suggested by the

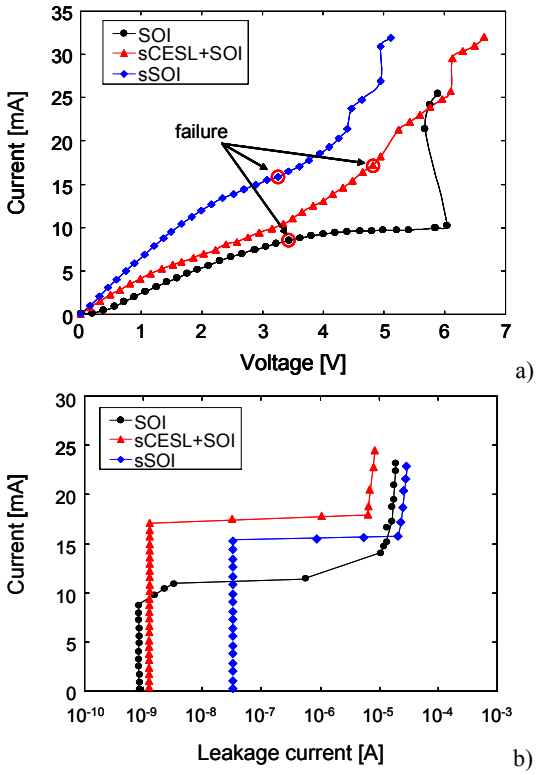



Figure 3.10: TLP IV curves and b) leakage current evolutions for N-channel FD SOI MOSFET with $W/L$ = 10 µm/0.16 µm and different strain levels. A sequence of pulses was applied to the drain terminal with increasing peak voltage, while keeping the front-gate and source terminals grounded.

increase in the slope of the IV curves. The turn-on voltage of the parasitic BJT is lower in strained devices because of a larger common-emitter current gain ($\beta$) due to a higher mobility.

$It_2/W$ as a function of $L$ for devices with different strain level is shown in Figure 3.8. An increase up to 20 % and 44 % is observed for sCESL+SOI and sSOI, respectively, with respect to SOI. Similar to SOI FinFETs (see Chapter 4), the $It_2$ improvement is larger for short L, where the effectiveness of the strain is larger. This behavior can be attributed to larger MOS current, mobility modulation (of both majority and minority carriers) and thermal conductivity modulation induced by the strain, as recently shown in [Lu09].

Table 3.I: Percentage of samples affected a) only by gate-oxide breakdown and b) by both gate-oxide breakdown and filament for different gate length ($L$), gate width ($W$), and strain level.

**a) ONLY GATE-OXIDE BREAKDOWN**

| | Device size | | | |
|---|---|---|---|---|
| | L ≤ 0.25µm | | L ≥ 0.5µm | |
| **Strain level** | W ≤ 0.25µm | W ≥ 0.5µm | W ≤ 0.25µm | W ≥ 0.5µm |
| SOI | 65 % | 68 % | 100 % | 100 % |
| sSOI | 47 % | 84 % | 100 % | 100 % |
| sCESL+SOI | 100 % | 100 % | 100 % | 100 % |

**b) GATE-OXIDE BREAKDOWN + FILAMENT**

| | Device size | | | |
|---|---|---|---|---|
| | L ≤ 0.25µm | | L ≥ 0.5µm | |
| **Strain level** | W ≤ 0.25µm | W ≥ 0.5µm | W ≤ 0.25µm | W ≥ 0.5µm |
| SOI | 35 % | 32 % | 0 % | 0 % |
| sSOI | 53 % | 16 % | 0 % | 0 % |
| sCESL+SOI | 0% | 0 % | 0 % | 0 % |

## 3.7 Failure Mechanisms

In order to carefully analyze the failure mechanisms, we have reported in Table 3.I the percentage of samples affected a) only by GOX breakdown and b) by both (progressive and/or non-severe soft) GOX breakdown and filamentation for different $L$, $W$, and strain levels.

The GOX breakdown alone (without filamentation) is the only failure mechanism for MOSFETs with long $L$, regardless of $W$ and strain level, while GOX breakdown together with filamentation can occur for short $L$. This is because the base voltage of the parasitic NPN increases with increasing $L$, leading the GOX subjected to more severe stress and lower current levels for long $L$ compared to short ones [Salman02]. In addition, for short gate lengths, where the power to failure ($P_f = Vt_2 \cdot It_2$) is 3.5x larger than for long $L$ (5 mW/µm vs. 1.3 mW/µm), filament between source and drain junctions is supposed to form more easily [Bock01], while with increasing $L$ the volume of the gate increases which improves the heat dissipation.

It is interesting to observe that the position (in the silicon body) of the filamentation depends on $W$. For wide devices, the filament is located close to the GOX/silicon interface (Figure 3.3). On the other hand, for narrow MOSFETs, the whole silicon body is affected by such failure mechanism (Figure 3.11), since the drain/source current is independent of both $V_{GS}$ and $V_{BS}$. This W dependency is due to the reduction in heat

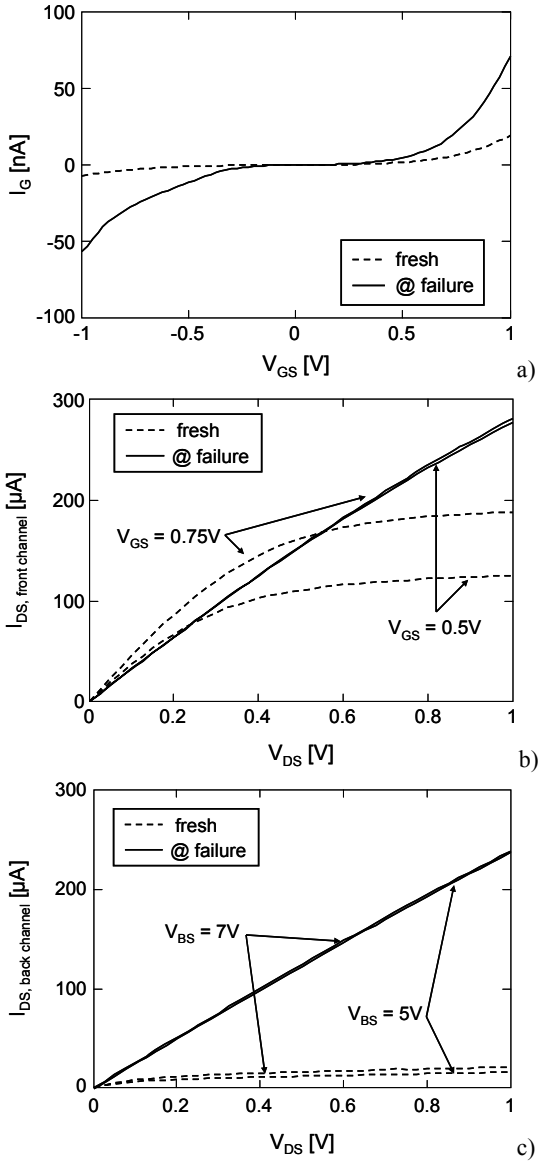



Figure 3.11: a) $I_G$-$V_G$, b) front- and c) back- channel $I_{DS}$-$V_{DS}$ (at the same bias conditions reported in Figure 3.2) for a conventional FD SOI MOSFET ($W/L$ = 0.25 µm/0.17 µm). Both the gate-oxide soft breakdown and filamentation in the whole silicon body (resulting in front- and back-channel $I_{DS}$-$V_{DS}$ independence on $V_{GS}$ and $V_{BS}$, respectively) occurred.

removal attributed to the STIs for narrow transistors [Ramaswamy95] and to a reduction of the available silicon volume ($2.55 \cdot 10^{-14}$ cm$^3$ for $W/L$ = 10 µm/0.17 µm, while only $6.38 \cdot 10^{-16}$ cm$^3$ for $W/L$ = 0.25 µm/0.17µm).

The percentage of short-channel samples affected by both GOX breakdown and filamentation depends on $W$ and strain levels. When W is decreased, the percentage of

Table 3.II: Thermal parameters of the materials used for the manufacturing of sCESL+SOI and SOI fully depleted MOSFETs.

| Material | Thermal conductivity [W/cm·K] | Specific heat capacitance [J/g·K] | Melting point [K] |
|---|---|---|---|
| Si | 1.5 | 0.7 | 1687 |
| SiN | - | - | 1023 |
| $Si_3N_4$ (like the strain layer) | 0.28 | 0.73 | 2173 |
| SiC | 1.14 | 0.75 | 3003 |
| $SiO_2$ | 0.014 | 1 | 1923 |
| low-k (silica based) | ~ same $SiO_2$ | ~ same $SiO_2$ | - |

sSOI samples affected also by filamentation increases from 16 % to 53 %. Such percentage is almost independent of *W* for SOI MOSFETs. The different trends are due to the different amount of current density ($I_{DS}/W$) flowing in the channel. For sSOI transistors, the drain current density increases up to 20 % with decreasing W (indicating that strain is more efficient for narrow devices), while it increases up to only 6 % in SOI transistors [Augendre05].

Finally, regardless of W and L, sCESL+SOI devices only present hard GOX breakdown and no filamentation (see Table 3.I). Similarly to the results found by Kubota et al. for NPN lateral BJT with field oxide [Kubota95], the failure of sCESL+SOI samples can be attributed to dislocations at the drain side, triggered by the interplay between the local thermal ESD stress and the residual mechanical stress induced by the sCESL. Moreover, the capping layer induces an additional lateral mechanical stress close to the overlap region between the gate and drain/source extension [Yamashita08]. Therefore, dislocations can induce the GOX breakdown before the source-drain filament formation. The thermal properties of the SiN stressor were found not to improve the cooling of the fins (Table 3.II), similar to SOI FinFETs (see Chapter 4). The thermal conductivity of the 100 nm SiN strain layer is about 4x lower than the one of the 50 nm SiC layer, which is used instead for the SOI devices between the active device area and the low-k layer. On the contrary, the specific heat capacitance is about the same in both cases.

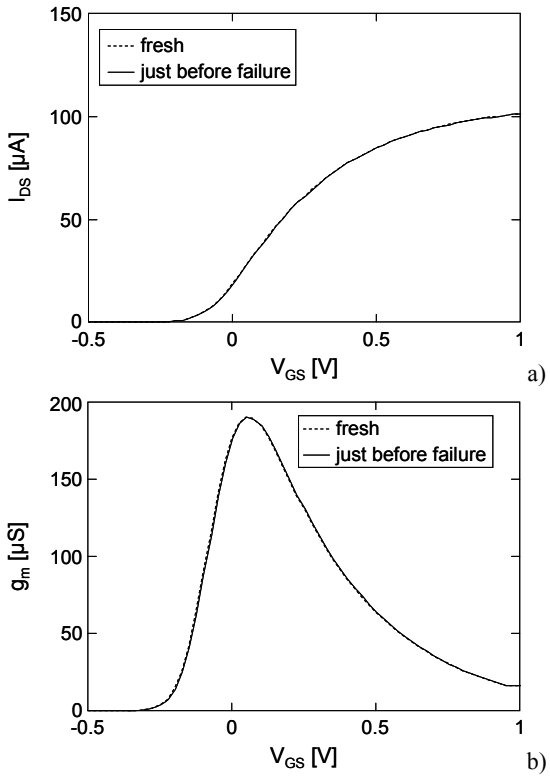



Figure 3.12: a) $I_{DS}$-$V_{GS}$ and b) $g_m$-$V_{GS}$ ($V_{DS}$ = 25 mV and $V_{BS}$ = 0 V) for a conventional FD SOI MOSFET ($W/L$ = 10 µm/0.5 µm). No degradation of the electrical DC parameters is observed at the ESD zap just before failure.

## 3.8 Degradation of the Electrical DC Parameters

We continue our analysis taking into account the degradation of the electrical DC characteristics, namely the transconductance ($g_m$) and the front-gate threshold voltage ($V_{TH,FG}$).

For $L \geq 0.5$ µm, the devices exhibit only a negligible $g_m$ drop (< 1 %) and $V_{TH,FG}$ shift (< 2 mV), regardless of W and strain level (Figure 3.12). On the contrary, for $L \leq 0.25$ µm, the devices show a modest degradation of the electrical DC parameters (Figures 3.13, 3.14, 3.16, and 3.17), depending on the strain level but not on $W$.

Figure 3.13 shows the $V_{TH,FG}$ shift and the relative gm drop as a function of the ESD voltage for a SOI MOSFET with $W/L$ = 10 µm/0.25 µm. Two phases can be distinguished. For low ESD stress levels (voltage < 3.2 V and current < 0.5 mA/µm, see Figure 3.7), a negligible degradation of $V_{TH,FG}$ and gm is observed. On the other hand, for high ESD stress levels (voltage > 3.2 V and current ≈ 0.5 mA/µm, see Figure 3.7), the

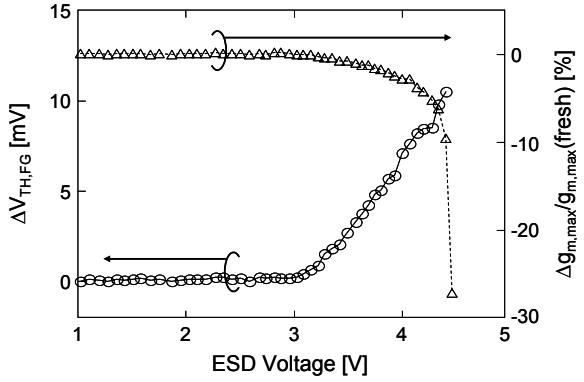



Figure 3.13: $V_{TH,FG}$ shift and relative $g_m$ drop ($V_{DS}$ = 25 mV and $V_{BS}$ = 0 V) as a function of the TLP pulse voltage for a conventional SOI MOSFET with $W/L$ = 10 µm/0.25 µm.

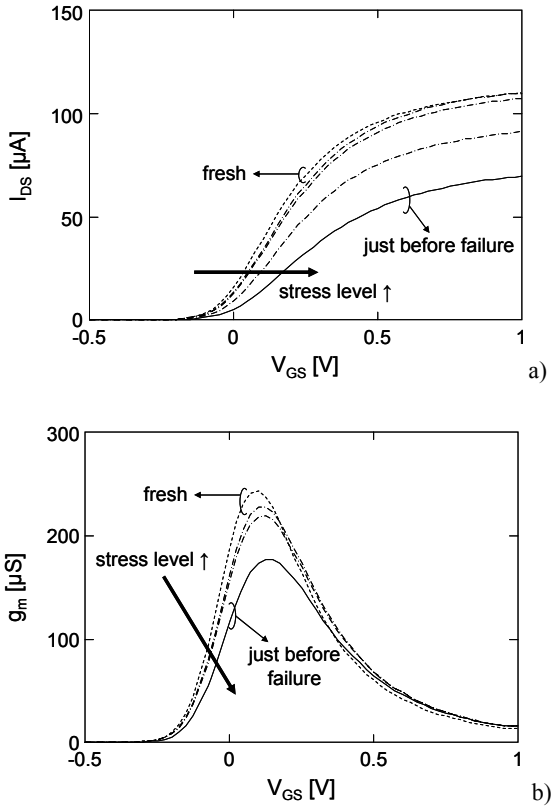



Figure 3.14: a) $I_{DS}$-$V_{GS}$ and b) $g_m$-$V_{GS}$ ($V_{DS}$ = 25 mV and $V_{BS}$ = 0 V) for a conventional SOI MOSFET ($W/L$ = 10 µm/0.25 µm). The front-gate threshold voltage increases while the transconductance decreases with increasing ESD stress level.

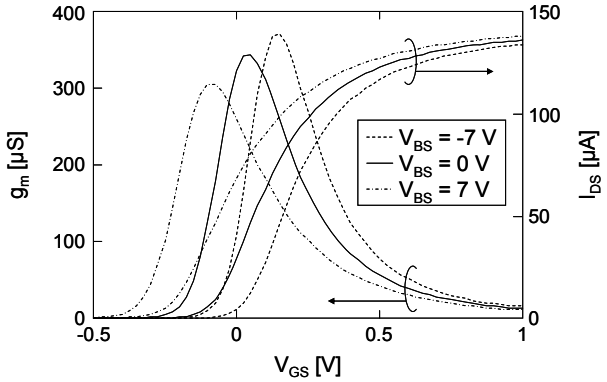



Figure 3.15*: $I_{DS}$-$V_{GS}$* and $g_m$-$V_{GS}$ ($V_{DS}$ = 25 mV and $V_{BS}$ = -7 V, 0 V, and 7 V) for a conventional FD SOI MOSFET ($W/L$ = 10 µm/0.17 µm) for different back-gate biases . Both $V_{TH,FG}$ and $g_m$ increase with increasing back-gate voltage.

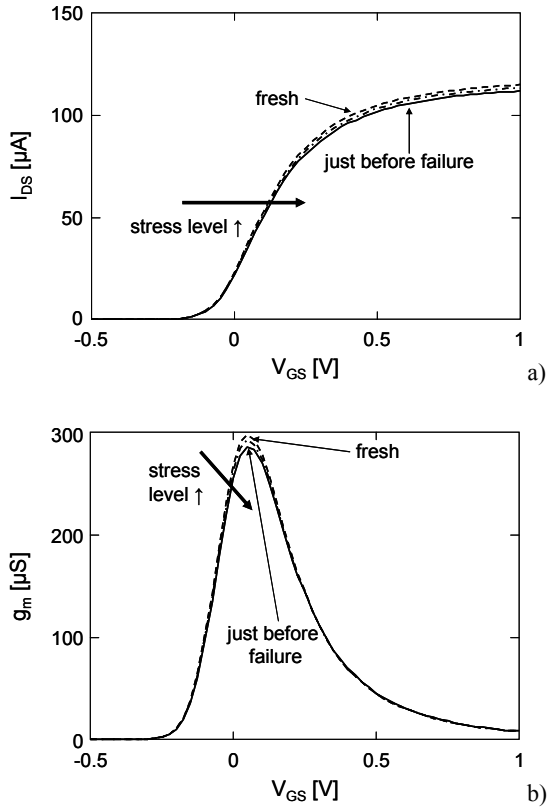



Figure 3.16: a) $I_{DS}$-$V_{GS}$ and b) $g_m$-$V_{GS}$ ($V_{DS}$ = 25 mV and $V_{BS}$ = 0 V) for a sCESL+SOI MOSFET ($W/L$ = 10 µm/0.25 µm). The front-gate threshold voltage increases while the transconductance decreases with increasing ESD stress level.

$V_{TH,FG}$ shift increases up to 12 mV while $g_m$ drops by 26 % (Figure 3.13 and Figure 3.14). Figure 3.13 also shows that the $V_{TH,FG}$ shift and the $g_m$ drop are correlated. Such

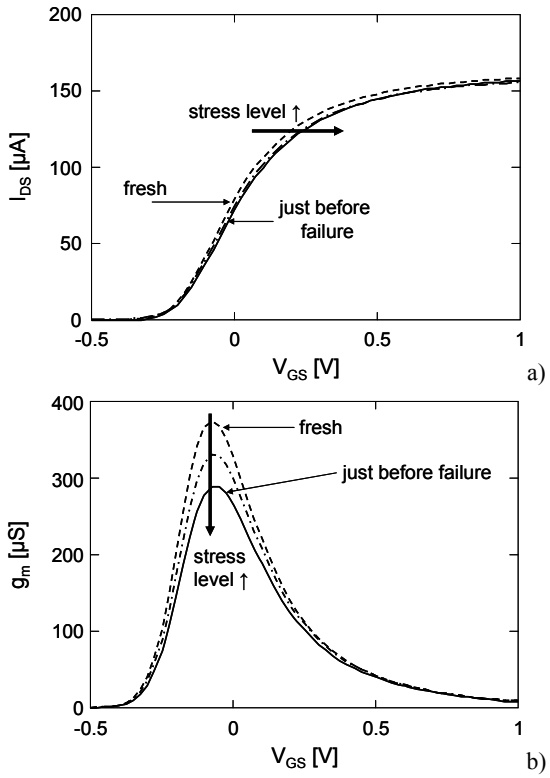



Figure 3.17: a) $I_{DS}$-$V_{GS}$ and b) $g_m$-$V_{GS}$ ($V_{DS}$ = 25 mV and $V_{BS}$ = 0 V) for a sSOI MOSFET ($W/L$ = 10 µm/0.25 µm). The front-gate threshold voltage does not significantly change while the transconductance decreases with increasing ESD stress level.

degradations cannot be attributed to charge build-up and interface states generation in the BOX because the trends cannot be emulated by biasing the back-gate at different voltages. Indeed, under such circumstance, both $V_{TH,FG}$ and gm increase with decreasing $V_{BS}$ (Figure 3.15). Therefore, the degradation of $V_{TH,FG}$ and gm is attributed to the increase in interface state density and traps in the GOX located near the overlap region between the gate and drain extension. This is because a significant amount of hot carriers flows through the channel generating hot-carrier-induced degradation.

For short-channel sCESL+SOI MOSFETs (Figure 3.16), the $V_{TH,FG}$ shifts only 4 mV and $g_m$ drops down only by 7 %. The lower degradation of sCESL+SOI samples compared to SOI ones is attributed to the better GOX quality, as shown by Time-Dependent Dielectric Breakdown measurements on the same devices [Claeys08]. As reported for bulk MOSFETs [Giusi07], in spite of the higher drain current for sCESL+SOI devices, the $I_{SUB}/I_D$ current ratio (where $I_{SUB}$ is the substrate current), which is a measure of the efficiency of the CHC generation process, is the same for the two types of devices.

For short-channel sSOI MOSFETs (Figure 3.17), $g_m$ drops down to 19 % while $V_{TH,FG}$ shifts up by 6 mV. The lower degradation of sSOI devices with respect to SOI ones is attributed to the lower $I_{SUB}/I_D$ ratio for sSOI, as reported for bulk MOSFETs [Kelly05]. Indeed, the $I_{DS}$-$V_{GS}$ and $g_m$-$V_{GS}$ characteristics confirm that the interface state generation rate is reduced in sSOI samples compared to SOI ones.

## 3.9 Conclusions

An extensive ESD characterization of UTB FD SOI MOSFETs with ultra-thin gate oxide and different strain-inducing technologies (conventional SOI, sCESL+SOI, and sSOI) has been presented. A detailed electrical investigation has been carried out in order to carefully classify the observed failure mechanisms. A new failure criterion that allows us to identify the device failure regardless of the occurred failure mechanisms (soft/hard gate-oxide breakdown and/or source-drain filamentation) has been proposed.

For long-channel MOSFETs, the failure is attributed only to the gate-oxide breakdown. In contrast, short-channel transistors can be affected by both filamentation and gate-oxide breakdown. The absence of filamentation is observed for sCESL+SOI devices, regardless of the device geometry.

Strain improves the ESD robustness up to 20 % and 44 % for sCESL+SOI and sSOI, respectively. A modest degradation of the electrical DC parameters is observed only for short gate lengths and it is larger for conventional SOI devices compared to the other types of transistors.

Final metal-gate devices may present some difference compared to the results presented in this work. For example, final MOSFETs stressed in grounded-gate configuration are expected to not have the additional MOS conduction on the top of parasitic-bipolar conduction. This can induce a different amount of failure current and degradation of the electrical DC parameters.

Our data suggest that the ESD effects on I/O MOSFETs must be constantly monitored, especially when new process modules, such as the reduction in the silicon-body thickness and the employment of channel strain techniques, are introduced into conventional CMOS technology.

Non-strained UTB FD SOI MOSFETs can achieve up to 1 mA/µm current capability (namely $It_2$), making them robust enough when local clamping devices are used. Despite our samples have negative front-gate threshold voltage, final metal-gate devices could be biased during ESD events to restore maximum $It_2$.

# Chapter 4

# ESD in FinFET Devices

Despite a small silicon volume to dissipate the heat from ESD discharges, it is demonstrated that both SOI and bulk FinFET devices can have reasonably good ESD robustness, depending strongly on layout and process parameters. A comparison between the ESD and RF-ESD performance of bulk FinFET and SOI FinFET structures is carried out.

## 4.1 Introduction

The reliability of submicrometer devices and circuits is a major issue that determines both their manufacturability and application lifetime. The design for reliability should be implemented during technology, device, and circuit development to avoid undesirable product development cycles and costly yield loss and field failures. As CMOS keeps scaling down, new technology options arise, and their ESD robustness should be preferably considered in the early technology development phase as these technology evolutions might lead to a “drastic” reduction in ESD performance.

Multi-gate devices, such as FinFETs, are one of the most promising candidates to continue with the CMOS scaling below the 22-nm node owing to their superior scalability and better gate controllability over the channel [ITRS08]. Usually, FinFET devices are fabricated on SOI substrate [Choi04]. However, SOI wafers have disadvantages with respect to self-heating, cost, defect density etc., when compared to bulk silicon substrates. It is therefore useful and cost-effective to implement FinFET technology on bulk silicon wafers. In addition, bulk silicon substrates are compatible with the existing standard planar CMOS process technologies [Okano05] [Park03].

In [Russ05] [Russ07], it was shown that early SOI FinFET structures displayed an extremely low TLP failure current $It_2$ for parasitic bipolar action. In the succeeding work

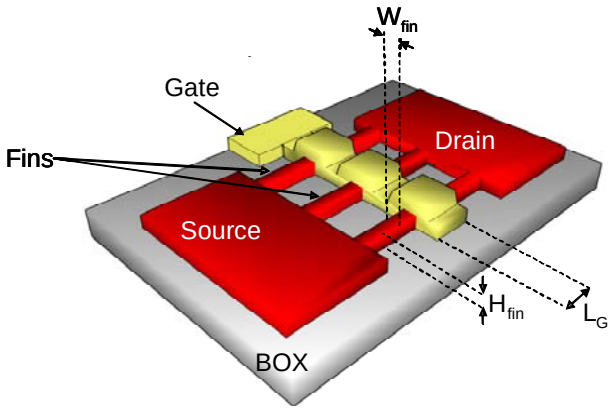



Figure 4.1: Simplified 3D layout view of a SOI FinFET device (not to scale)

[Gossner06], localized heating was demonstrated to be the cause for the high sensitivity and consequently FinFET optimization requires understanding of the thermal effects.

First, the SOI FinFET technology used in this work is described in section 4.2. After discussing the normalization methodology in section 4.3, section 4.4 describes the impact of the fin width and gate length on the ESD performance of MOS devices. Afterwards, section 4.5 discusses the impact of different process options, such as Selective Epitaxial Growth (SEG) and strain. The ESD performance of MOS and gated diodes bulk FinFETs are investigated and compared to the ones of SOI FinFETs in the sections 4.6. Finally, section 4.7 gives an insight into RF performance of FinFET gated diodes.

## 4.2 SOI FinFET Technology

State-of-the-art SOI FinFET devices developed at IMEC use a high-k gate dielectric and a metal gate. Metal gate is the preferable option over polysilicon gate since it allows obtaining correct N- and P-MOS threshold voltages $V_{TH}$ without using channel doping. The absence of channel doping also permits the drastic reduction of the dopant fluctuation effect. The devices are processed on SOI wafers with 65-nm Si film thickness on top of a 145-nm buried oxide. The Si film thickness defines the height of each fin $H_{fin}$, while its width $W_{fin}$ is defined by the active etch mask. The gate stack consists of a 100-nm polysilicon on top of a MOCVD metal gate (TiN), a 2 nm high-k HfSiON layer, and 1 nm interfacial $SiO_2$. The TiN gate has its workfunction in the middle of the bandgap such that symmetric $V_{TH}$'s for NMOS and PMOS can be achieved without any fin doping. After Ni silicidation, a tensile Contact Etch Stop Layer (tCESL) layer of 0.8 GPa is used to introduce strain for improved carrier mobility. All devices used in this paper have strain,

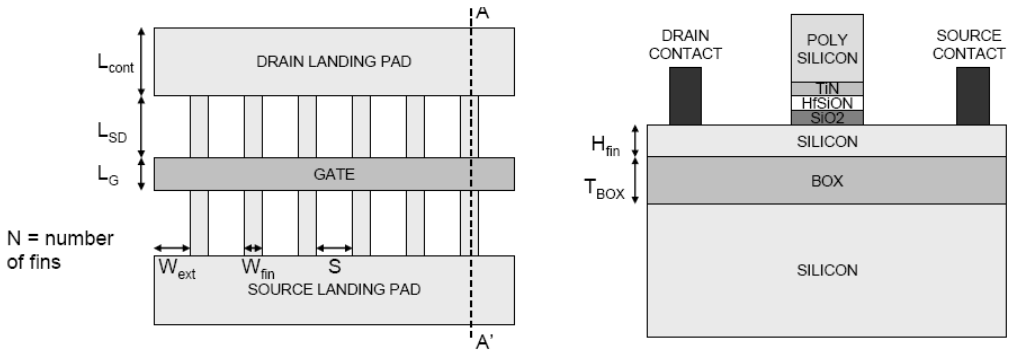



Figure 4.2: Simplified horizontal view (left) and vertical cut along cut-line A-A'(right) of a FinFET device indicating the different geometrical parameters (not to scale).

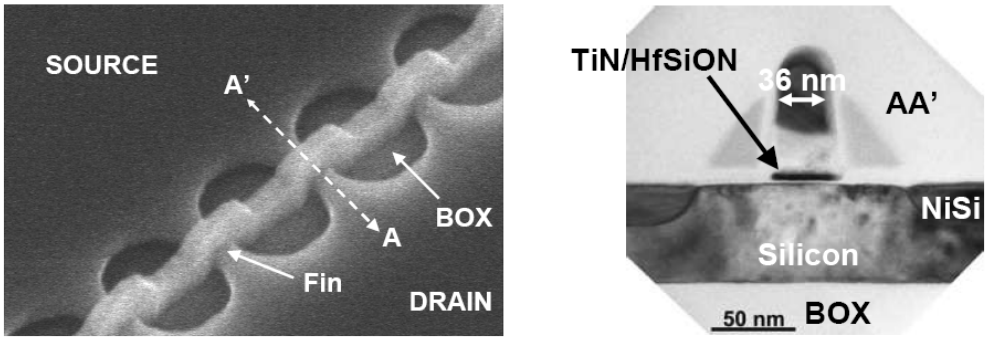



Figure 4.3: Top-down SEM (left) and cross sectional TEM image along cut-line A-A' (right) of a typical FinFET device with a thin MOCVD TiN metal gate on HfSiON dielectric.

and the impact of the absence of strain is studied in Section 4.4.2. More technological details can be found in [Collaert05_1].

FinFET devices have more geometrical dimensions than conventional planar devices. In addition to gate length $L_G$ (Figure 4.1 and Figure 4.2), we can also define fin width $W_{fin}$, fin height $H_{fin}$, distances between S/D contact area and gate ($L_S$ and $L_D$), size of the S/D contact area $L_{cont}$, spacing between two adjacent fins $S$, overlap gate on fins $W_{ext}$, and the number of fins $N$. $W_{fin}$, $W_{ext}$, $L_G$, $L_S$, $L_D$, $L_{cont}$, and $N$ can be chosen by the designer. $H_{fin}$ and $S$ are currently fixed by the process. $L_G$ is 45 nm minimal, $W_{fin}$ is 30 nm minimal, $S$ is fixed to 170 nm, $L_S$ and $L_D$ are 100 nm minimal, and $L_{cont}$ is chosen to accommodate two rows of contacts for all devices in this paper. Moreover, devices of a single "fin" of 40 µm are considered. The reader might argue the use of the word "fin" for these devices, as they are, in essence, planar SOI devices. A scanning electron microscope (SEM) image and a cross-sectional transmission electron microscope (TEM) image of the fabricated devices are shown in Figure 4.3.

## 4.3 Normalization Methodology

For interpretation of the results, different width normalizations are possible. It should always be indicated which normalization was used. First, there is normalization possible toward intrinsic silicon width $W_{intr}$

$$W_{intr} = N\, W_{fin}. \tag{4.1}$$

This normalization is preferred where current is flowing through the full cross section of the fin, e.g., as will be shown for MOS devices operating in parasitic bipolar mode. This is a measure for the intrinsic ESD performance of the device. Second, a normalization can be used to investigate the layout efficiency of the device, considering the total layout width Wlayout

$$W_{layout} = N\, W_{fin} + (N - 1)\, S \tag{4.2}$$

where $W_{layout}$ includes the overhead due to the fin-to-fin spacing $S$. The gate overlap on fins $W_{ext}$ and the size of the polycontacts are neglected. An additional layout optimization could be performed by folding the transistor and sharing different source and drain regions, reducing the overall layout area. The impact of folding on the ESD performance parameters, such as $It_2$ and $R_{on}$, is currently under investigation. This normalization is most important for an I/O layout engineer. Finally, the normalization can take into account the fact that FinFET devices exhibit a certain total channel width $W_{chan}$, defined by the top and sidewalls of the fin, per silicon footprint area. To exploit this 3-D benefit, an effective width $W_{eff}$ (3) is proposed, which corrects the intrinsic width $W_{intr}$ by the ratio of $W_{layout}$ and $W_{chan}$

$$W_{eff} = W_{intr} \frac{W_{layout}}{W_{chan}} \tag{4.3}$$

where

$$W_{chan} = N\,(W_{fin} + 2H_{fin}). \tag{4.4}$$

As such, the effective width normalization relates to intrinsic performance, the total drive current, and the layout efficiency of the device. This method is more applicable when MOS current is flowing. This is also the preferred normalization when comparing FinFET ESD performance with other technologies. Note that for wide-fin devices, all three normalizations yield almost identical results.

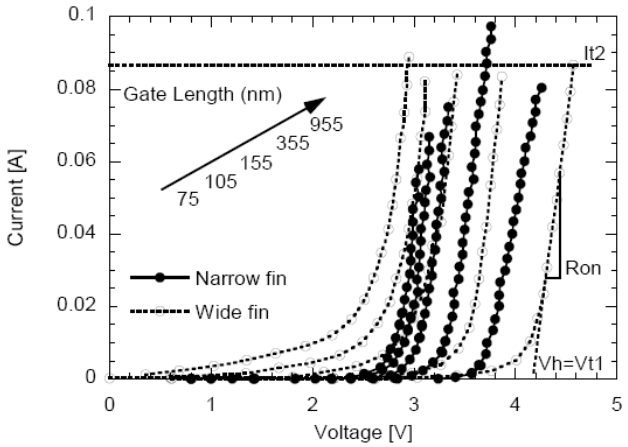



Figure 4.4: TLP-IV curves for different gate lengths of N-type FinFET in bipolar mode for both narrow (400 fins of 30 nm $W_{fin}$) and wide (single 40 µm) fin devices.

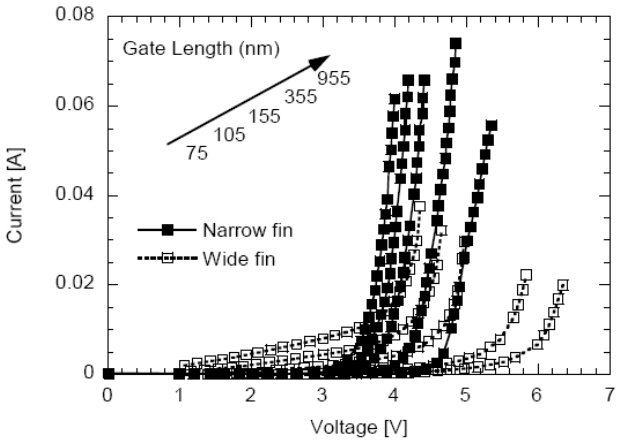



Figure 4.5: TLP-IV curves for different gate lengths of P-type FinFET in bipolar mode for both narrow (400 fins of 30 nm $W_{fin}$) and wide (single 40 µm) fin devices.

## 4.4 Impact of Layout Parameters

$W_{fin}$, $L_G$, and $N$ are the most important layout parameters which can be chosen by the ESD designer. The other layout parameters (Figure 4.2) are either fixed by the process or chosen to be minimal. The influence of $W_{fin}$ and $L_G$ on the different ESD performance parameters is investigated in this section. ESD stress is applied to the drain, while source and gate are grounded. The MOS devices are thus operated in parasitic bipolar mode, which means that each fin forms its own parasitic bipolar transistor. TLP measurements of narrow- and wide-fin NMOS and PMOS FinFET devices are shown in Figure 4.4 and

Figure 4.5, respectively, for different gate lengths. The last point indicated in each I-V curve corresponds to the maximum failure current $It_2$. After the next TLP stress level, an increase in leakage current was noticed, indicating device failure. The extraction of $It_2$, $Vt_1$, $V_h$, and $R_{on}$ is shown in Figure 4.4. The narrow-fin devices have $W_{fin}$ of 30 nm and $N$ of 400. The wide-fin devices consist of a single "fin" of 40 µm wide resembling a planar SOI device. Since the parasitic bipolars have their bases floating, no snapback is seen in the TLP I−V curves. This floating-body effect is typical for any SOI process [Amerasekera02], even though, for planar SOI, a body contact could be provided from the device side. The trigger voltage is not $BV_{CBO}$ as, e.g., for bulk technologies, but the device starts to conduct current immediately at the lower $BV_{CEO}$. This means that the trigger voltage $Vt_1$ and holding voltage $V_h$ are equal [Amerasekera02], which ensures uniform turn-on of all fingers.

Both Figure 4.4 and Figure 4.5 show that small gate lengths cannot control SCE for wide-fin devices, leading to a significant amount of current flow, even at voltages of 2 V and below. Based on Figure 4.4 and Figure 4.5, the different ESD performance parameters can be investigated.

### *4.4.1 Failure Current $It_2$*

$It_2$ as a function of $L_G$ for both NMOS and PMOS is shown in Figure 4.6 and Figure 4.7, respectively. For narrow-fin NMOS and PMOS devices, $It_2$ increases with increasing gate length and drops down again for the largest gate length. At high current levels, the current tends to localize in a few fins near the onset of failure, as described in [Gossner06]. This "nonuniform failure" is not a matter of "nonuniform turn-on" in multifinger devices. Remember that the floating base and, thus, the absence of snapback ensured all fingers to turn-on. In [Gossner06], failure analysis was used to show that fusing of single fins was the cause of failure. Increasing $L_G$ for narrow-fin devices does not only increase the silicon volume below the gate and hence its heat capacity but also it seems to have the same effect as a ballast resistance which improves the current uniformity at high current levels. This explains the increase of $It_2$ with increasing $L_G$. When further increasing $L_G$, the voltage drop also increases (increased $V_h$ and $R_{on}$, Figure 4.9 and Figure 4.10, respectively, explained further in Sections 4.3.2 and 4.3.3). As a consequence, the dissipated energy is increased, which leads to a maximum $It_2$ at medium $L_G$ (Figure 4.6 and Figure 4.7). For the shortest $L_G$, the small increase of $It_2$ is due to incorrect normalization because of a fin widening due to the Optical Proximity Correction (OPC) of the active etch mask. The shortest $L_G$ leads to shortest fin length, and thus, the fins are inevitably processed at slightly larger fin width.

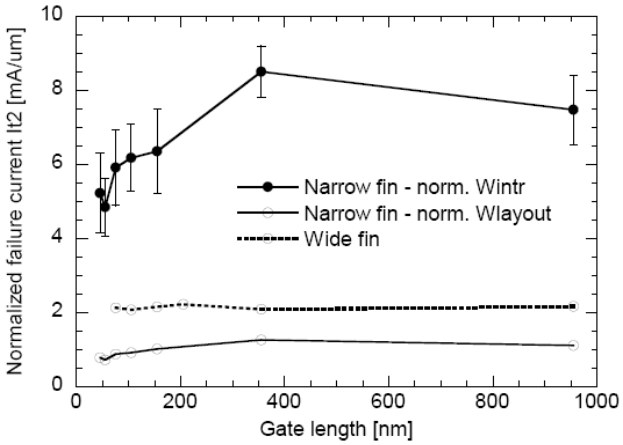



Figure 4.6: Normalized $It_2$ as a function of gate length for narrow and wide fin N-type FinFET devices in bipolar mode.

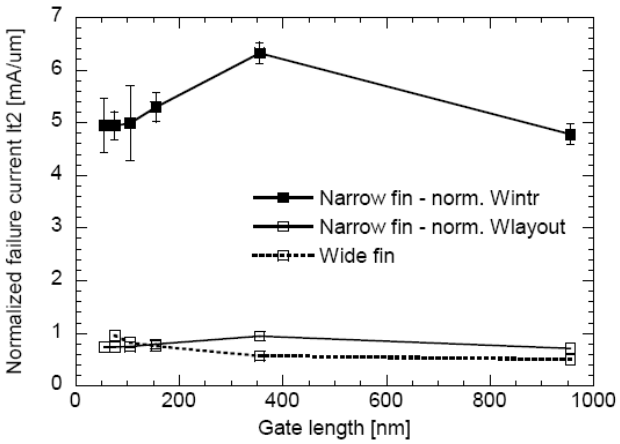



Figure 4.7: Normalized $It_2$ as a function of gate length for narrow and wide fin P-type FinFET devices in bipolar mode.

For wide-fin NMOS devices, $It_2$ is independent of $L_G$ (Figure 4.6). For a wide single fin, much less problems exist with current uniformity at high current levels, since, now, the current is located within one single wide fin and not among different narrow fins. However, it is important to notice that the failure is located at a constant current level rather than at a constant power level. This can be attributed to isothermal current instability which is initiated by impact ionization under high field conditions [Vashchenko08]. Locally, a high Joule power level is generated, which results in a filament formation and finally local burnout. This means that even within a single wide fin, there can still exist a degree of non-uniformity.

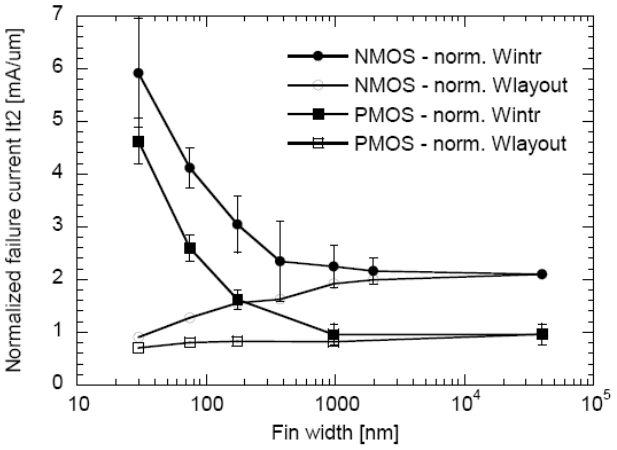



Figure 4.8 Normalized $It_2$ as a function of fin width for FinFET devices with 75 nm gate length in bipolar mode. Devices up to 175 nm fin width consist of 400 fins, up to 2 µm of 40 fins and the 40 µm wide device has only a single 'fin'.

In contrast to wide-fin NMOS devices (Figure 4.6), for PMOS devices, $It_2$ is unexpectedly decreasing with increasing $L_G$ (Figure 4.7). This can be attributed to their high holding voltage needed for bipolar action as shown in Figure 4.5 and Figure 4.9. As such, these devices are failing because of gate-oxide breakdown at the drain–gate overlap region instead of thermal failure of the fins. A possible explanation for the current localization, described in [Gossner06], could be the existence of local Schottky contacts between the S/D silicide (NiSi) and the body of the FinFETs [Hoffmann05]. Such a Schottky contact is a result of oversilicidation of the fins where the Ni silicide can overrun the lowly doped extension and grow into the channel region. The ESD robustness is very sensitive to oversilicidation. However, in a more mature technology, the problem of oversilicidation should be greatly reduced. Many arguments point to the negative impact of the oversilicidation. First, the oversilicidation is worst for narrow-fin devices [Collaert07_1]. This is in agreement with the improvement in $It_2$ with increasing gate length for these narrow-fin devices, whereas the wide-fin devices are independent of $L_G$. Second, oversilicidation is less problematic for PMOS devices as boron retards the silicidation [Collaert07] [Dixit06]. This can explain the increased $It_2$ for PMOS devices with the smallest gate length when compared to NMOS and the reduced $L_G$ dependence (Figure 4.6 and Figure 4.7). Moreover, much less statistical variation in $It_2$ was measured on PMOS than on NMOS devices. The error bars indicating the standard deviation of $It_2$ for NMOS and PMOS devices in 4.6 and Figure 4.7 for intrinsic silicon width $W_{intr}$ normalization show the increased variability for NMOS. Finally, oversilicidation is reduced by processing options like silicide blocking and Selective Epitaxial Growth

(SEG), which directly translates into an increased ESD performance as described further in Section 4.5.1.

For wide-fin NMOS devices, $It_2$ is equal to 2 mA/µm and independent of $L_G$ (Figure 6). The ESD robustness for narrow-fin NMOS devices is 0.5–1 mA/µm when normalized to layout width $W_{layout}$. However, the robustness regarding $W_{intr}$ is 5–8 mA/µm, representing an even higher intrinsic $It_2$ than the results reported for planar SOI devices [Keppens06]. This is explained by looking at the fin-width dependence of $It_2$. In Figure 4.8, the normalized $It_2$ as a function of $W_{fin}$ is shown for NMOS and PMOS devices with a gate length of 75 nm. The largest statistical variations were measured for the narrowest fins and, in general, for NMOS. This can be attributed to their higher sensitivity to oversilicidation, which has a direct negative impact on $It_2$. hen normalizing $It_2$ versus $W_{intr}$ and versus $W_{layout}$, different trends are observed. An increased intrinsic performance is measured for decreased fin width. This increase in $It_2$ can be attributed to the higher effective heat capacity of the 3-D gate, which fully surrounds the fin. Narrow fins act as "cooling fins." For wider fins, this 3-D nature of the gate disappears and the device becomes very similar to a planar device, leading to a decrease in $It_2$. The same dependence and relative difference in $It_2$ versus fin width between NMOS and PMOS are observed. However, when normalizing to $W_{layout}$, the trend becomes opposite. This is because for smaller fins, there is relatively more area overhead due to the fin-to-fin spacing, making them less area efficient. For wider fins, the difference between the two normalization techniques obviously disappears because of the reduced fin-to-fin spacing overhead. From Figure 4.8 and all subsequent figures which include fin-width dependence, it can be concluded that from a 1-µm-wide fin onward, the devices can be treated as 2-D planar SOI instead of 3-D FinFET devices.

### *4.4.2 Holding Voltage $V_h$*

The holding voltage increases with increasing gate length as expected (Figure 4.9), because $L_G$ defines the base width of the parasitic bipolar which determines the holding voltage. As such, the holding voltage can be tuned for narrow-fin devices between 2.6 and 3.6 V for NFETs and between 3.5 and 4.6 V for PFETs. The holding voltage is clearly determined as almost no statistical variation was measured. $V_h$ of the PMOS devices is higher when compared to that of NMOS due to the reduced hole versus electron mobility and the lower avalanche multiplication factor of hole current versus electron current [PhDTrémouilles]. For wide-fin devices, $V_h$ is higher than that for narrow-fin devices due to lower electric field and, hence, lower impact ionization rate. This increase is particularly pronounced for large $L_G$ and for PMOS devices.

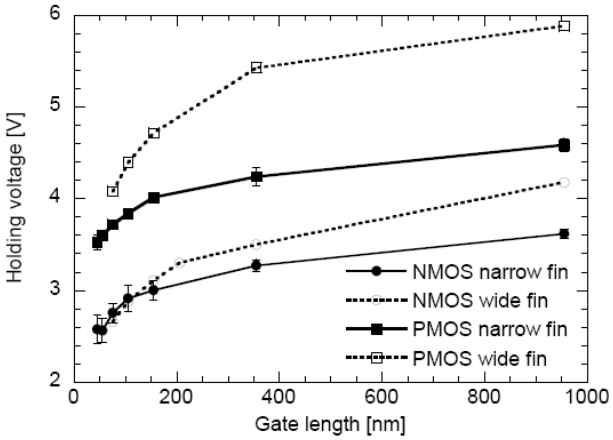



Figure 4.9: Holding voltage as a function of gate length for narrow and wide fin FinFET devices in bipolar mode.

### *4.4.3 On-Resistance Ron*

The ESD on-resistance $R_{on}$, normalized to $W_{intr}$ is shown in Figure 4.10 as a function of $L_G$. For narrow-fin NMOS devices, the on-resistance is relatively independent of $L_G$ for small gate lengths, giving a measure for the access resistance of the device, which is determined by the resistance of the source/drain landing pads, the interconnects, and amorphization of the silicon [Collaert07_1]. When further increasing $L_G$, the additional channel resistance becomes visible. Very little statistical variation was measured. Wide-fin devices exhibit the same gate length dependence but at a much higher $R_{on}$. This width dependence of $R_{on}$ is further discussed using Figure 4.10b. The resistance of the PMOS increases with increasing $L_G$ and is larger than for the NMOS, which is partly due to the lower hole mobility. In [Dixit06], the difference in silicide formation between NMOS and PMOS devices was studied. It was found that for NMOS devices, the sidewalls were completely silicided along the whole height of the S/D region, which was not the case for the PMOS, again due to the presence of boron in the S/D regions. This effect further explains the increased on-resistance for the PMOS devices. $R_{on}$ decreases with decreasing $W_{fin}$ for both NMOS and PMOS devices when normalized to $W_{intr}$, as shown in Figure 4.10b, for devices with a fixed $L_G$ of 75 nm. For narrow fins, NiSi grows from both the sidewalls and the top, so that the devices can become fully silicided, hence the lower $R_{on}$ [Hoffmann05]. The statistical variation of $R_{on}$ increases a lot when increasing the fin width. Since these devices have a gate length of 75 nm, the devices with the largest fin width lack control of SCE. Current starts to conduct already at very low voltages (Figure 4.4), which makes the extraction of the pure bipolar on-resistance very sensitive. For reference, also the normalized $R_{on}$ versus effective channel

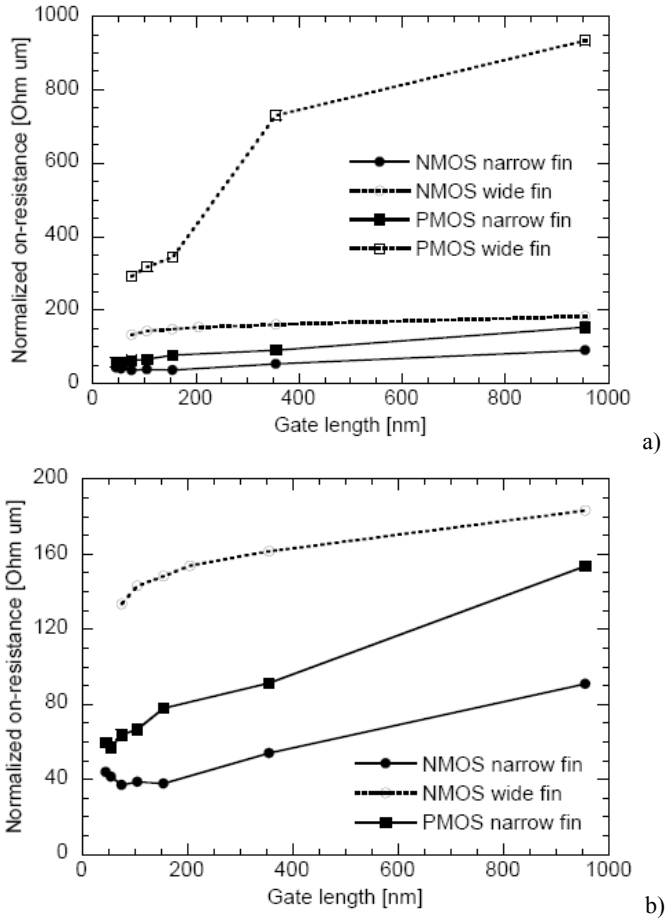



Figure 4.10: High current on-resistance normalized to intrinsic silicon width as a function of gate length for narrow and wide fin FinFET devices in bipolar mode (a) full scale, b) zoom).

width $W_{chan}$ is shown, which is more commonly used in technology-oriented papers, but less useful for ESD considerations. The gravity of the problem of series resistance in FinFET devices [Dixit05] can be clearly seen, as the resistance increases rapidly for the smallest $W_{fin}$.

## 4.5 Impact of Process Options

The FinFET technology has to cope with some challenges such as a reduced mobility, high S/D access resistance, VT variability, SCE control etc. Different process options are introduced to improve these parameters. These process options will also have

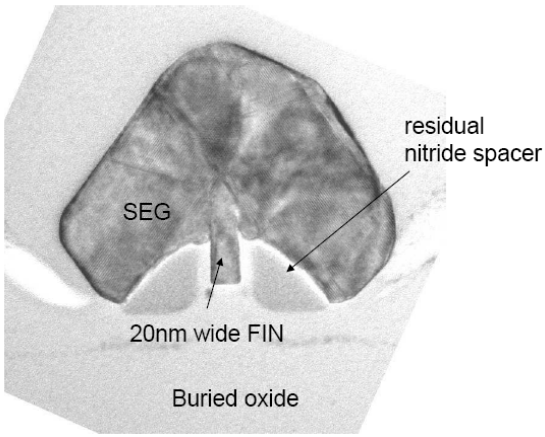



Figure 4.11: Selective Epitaxial Growth (SEG) over one fin.

an impact on the ESD robustness. Therefore, it is important to investigate their influence upfront. In this section, the impact of SEG and strain is discussed.

### *4.5.1 Selective Epitaxial Growth SEG*

For the technology nodes at and below 32 nm, fin widths smaller than 10 nm will be needed to maintain good short channel behavior [Collaert07_1]. For these narrow-fin devices, the access resistance is very high. SEG on source and drain areas is typically used to reduce the contact resistance [Kedzierski03] by almost 50% (Figure 4.11). Due to the increased silicon volume, also the problem of oversilicidation is greatly reduced, because the SEG gets silicided instead of the fin. This leads to a decrease in leakage current of four orders of magnitude [Collaert07_2].

Figure 4.12 and Figure 4.13 show the influence on narrow-fin N- and P-type FinFETs, respectively, for different $L_G$. For both NMOS and PMOS, SEG increases $It_2$ drastically and lowers $R_{on}$, while the dependence on $L_G$ remains similar. The improved robustness can be mainly attributed to the better heat removal and storage from the drain-body junction of the fin due to the larger fin dimensions in the source and drain access region. The PMOS behavior is less improved by SEG because, in general, for PMOS FinFET devices, the contact resistance is not the limiting factor but the lower carrier mobility.

Moreover, the reduction of oversilicidation is a factor which increases $It_2$ for SEG devices due to improved current uniformity. The result is lower measurement variation for SEG devices and a decrease of $V_h$ (Figure 4.12). The Schottky contact created during oversilicidation is a source for recombination of the carriers generated by impact

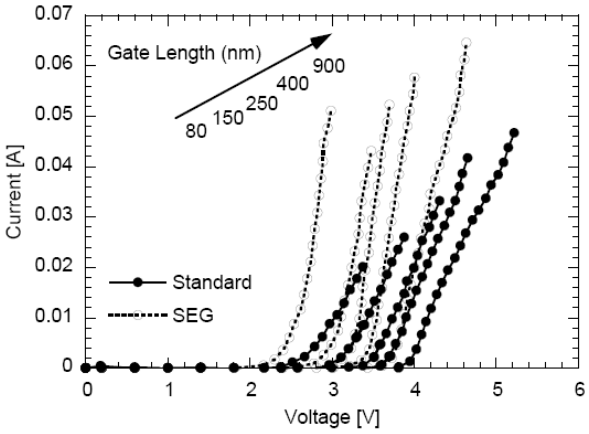



Figure 4.12: TLP-IV curves of N-type FinFET in bipolar mode as a function of gate length for wafers processed with and without SEG. The devices have a fin width of 25 nm and 225 fins in parallel.

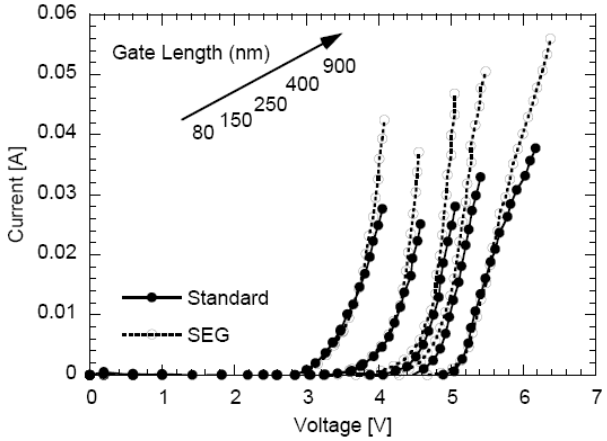



Figure 4.13: TLP-IV curves of P-type FinFET in bipolar mode as a function of gate length for wafers processed with and without SEG. The devices have a fin width of 25 nm and 225 fins in parallel.

ionization during turn-on of the parasitic bipolar, lowering its $\beta$ [Hoffmann05]. As a consequence, the required voltage to sustain bipolar operation is lower than when oversilicidation would have occurred. Since the PMOS has less problems with oversilicidation due to the presence of boron in the $P^+$ S/D regions, the decrease in $V_h$ is much less pronounced.

## *4.5.2 Strain*

Both TLP and HBM measurements are used to provide new insights into the high-current behavior of strained FinFET devices during an ESD event in section 4.4.2.1 and section 4.4.2.2 respectively. Using TLP measurements, strain is found to improve the ESD robustness up to 20 % in NMOS FinFET devices, while HBM-IV measurements

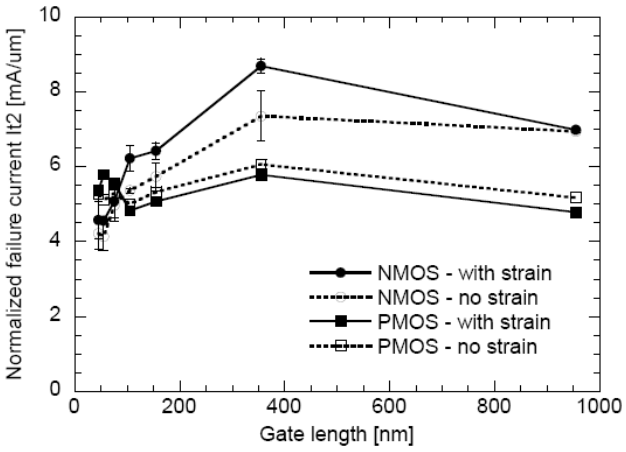



Figure 4.14: Normalized $It_2$ to intrinsic silicon width as a function of gate length for FinFET devices in bipolar mode for wafers with and without tCESL. The devices have a fin width of 30 nm and 400 fins in parallel.

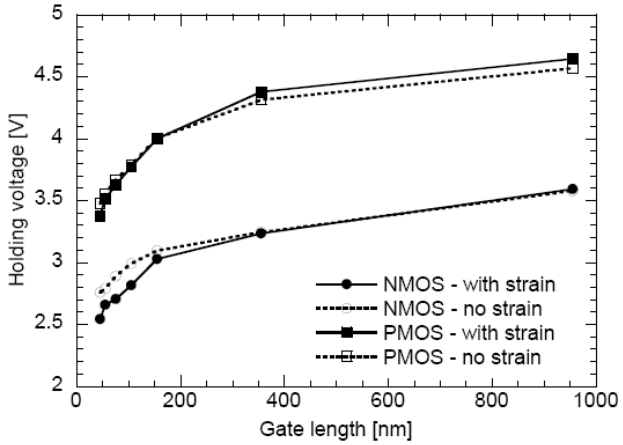



Figure 4.15: Holding voltage of FinFET in bipolar mode as a function of gate length for wafers processed with and without tCESL. The devices have a fin width of 30 nm and 400 fins in parallel.

reveal a different failure mechanism for strained versus non-strained devices for MOS devices in parasitic-bipolar mode.

### *4.5.2.1 TLP Analysis*

In narrow-fin devices, the current flows mainly in the sidewalls of the device. A change in crystal orientation degrades the electron mobility and improves the hole mobility when starting from a {100}silicon wafer with [110] current direction [Yang03], [Shin05]. In order to improve the performance, strain is introduced. For both nMOS and

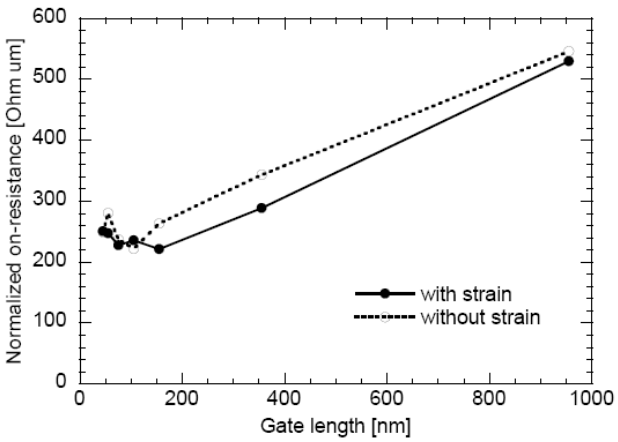



Figure 4.16: ESD on-resistance normalized to total channel width as a function of gate length for narrow N-type FinFET devices with and without tCESL in bipolar mode.

pMOS, a 100-nm tensile or compressively strained nitride layer with an intrinsic stress of 0.8 GPa was deposited [Collaert08]. An NMOS drive current improvement up to 20% was measured with tCESL. The improvement seen for pMOS due to compressive strain is lower, about 10% [Collaert08], [Shin05]. Since the PMOS improvement due to compressive strain is only moderate and almost no degradation of the PMOS due to tensile CESL is measured, a more simple process scheme with only tCESL can be used [Collaert05_2].

The intrinsic normalized $It_2$ for narrow-fin NMOS and PMOS devices with and without tCESL as a function of $L_G$ is shown in Figure 4.14. An improvement of up to 20% in $It_2$ is measured for NMOS devices with medium $L_G$. Only a slight reduction in $It_2$ is measured for PMOS. While $V_h$ is unchanged for PMOS, a decreased $V_h$ is measured for NMOS devices with the smallest $L_G$, as shown in Figure 4.15. This improvement is due to improved electron mobility and is most pronounced for small-to-medium gate lengths because they are more impacted by CESL. The explanation for the most improved $It_2$ for medium $L_G$ for NMOS devices can be found in the extraction of the ESD on-resistance $R_{on}$ normalized per $W_{chan}$ (Figure 4.16). A decrease in $R_{on}$ is measured for NMOS devices with medium $L_G$, which can be attributed to the mobility improvement due to strain. For the largest $L_G$, the impact of strain is minimal, hence no change in $R_{on}$. On the other hand, for smallest $L_G$, $R_{on}$ is dominated by the access resistance and not by the channel resistance. Note that SEG will reduce this mobility improvement, since the additional epitaxial grown silicon on the fin increases the distance of the SiN liner to the channel [Collaert05_2] and hence reduces its impact. Yet, the advantages of SEG have become very obvious.

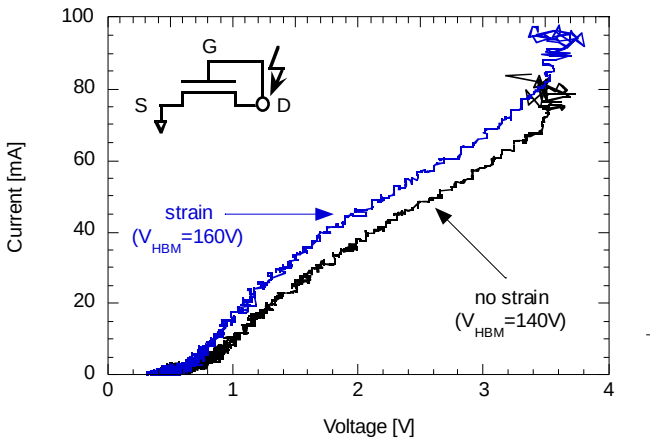



Figure 4.17: HBM-IV curves just before failure for strained and non-strained NMOS FinFETs stressed in active MOS-diode mode. The gate is tied to the drain while the source is kept grounded. The devices have a gate length of 155 nm. Strain improves the mobility and hence the MOS-drive current. Also the HBM robustness is increased.

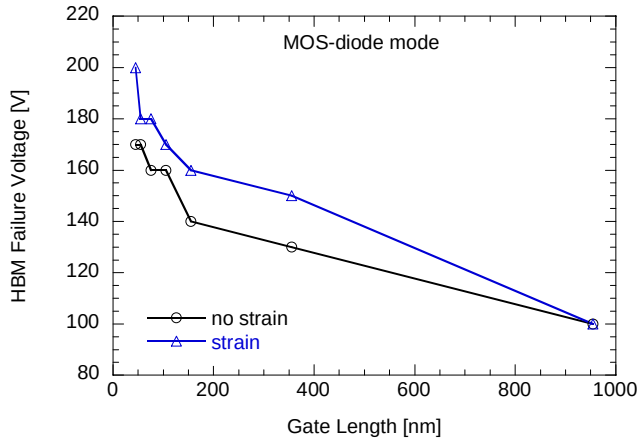



Figure 4.18: HBM-failure voltage as a function of gate length for N-type FinFETs in MOS-diode mode. Strain improves the ESD robustness up to 15 % for short and medium gate lengths.

### *4.5.2.2 HBM Transient Analysis*

HBM I-V measurements were used to investigate the impact of strain on different type of FinFET devices, namely FinFET NMOS devices in active MOS-diode mode and in parasitic-bipolar mode and gated FinFET diodes. A 10x increase in DC leakage current was considered as device failure.

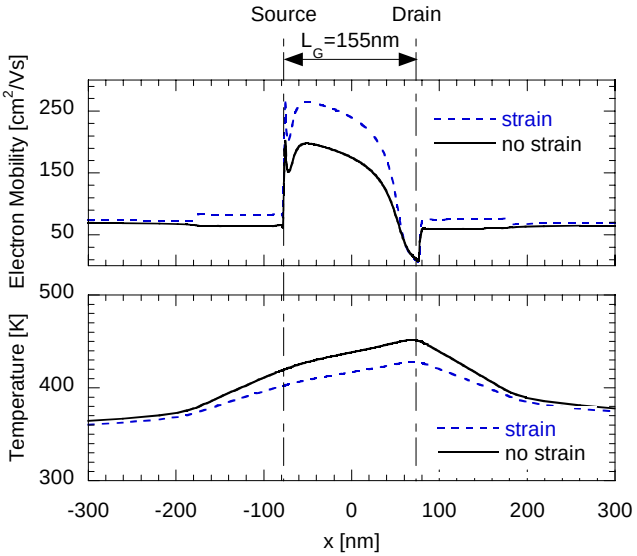



Figure 4.19: TCAD-simulated mobility and temperature profile along the fin length during a 140 V HBM pulse in MOS-diode mode. Mobility and temperature were captured during the maximum HBM current at 10 ns. Strain increases the mobility and results in a decreased temperature. The temperature profile exhibits a smooth peak, located at the drain junction.

Table 4.I: Thermal parameters of the materials used for the manufacturing of strained and non-strained FinFET devices.

| Material | Thermal conductivity [W/cm·K] | Specific heat capacitance [J/g·K] | Melting point [K] |
|---|---|---|---|
| Si | 1.5 | 0.7 | 1687 |
| SiN | - | - | 1023 |
| $Si_3N_4$ (like the strain layer) | 0.28 | 0.73 | 2173 |
| SiC | 1.14 | 0.75 | 3003 |
| SiO2 | 0.014 | 1 | 1923 |
| low-k (silica based) | ~ same $SiO_2$ | ~ same $SiO_2$ | - |

## *FinFET NMOS Devices in Active MOS-Diode Mode*

Figure 4.17 shows the HBM-IV curves, just before failure, for NMOS FinFETs with and without strain stressed in MOS-diode mode, where the ESD stress is applied to gate and drain while the source is kept grounded. The devices start to conduct current soon after reaching their threshold voltage. Strained samples exhibit a larger mobility, which is seen in increased MOS drive current. They fail at a 15 % increased HBM failure level compared to non-strained devices as seen in Figure 4.18. The ESD robustness decreases with increasing gate length (Figure 4.18), which is due to increased self-heating [Trémouilles07]. As confirmed by TCAD simulations (Figure 4.19), the increased ESD

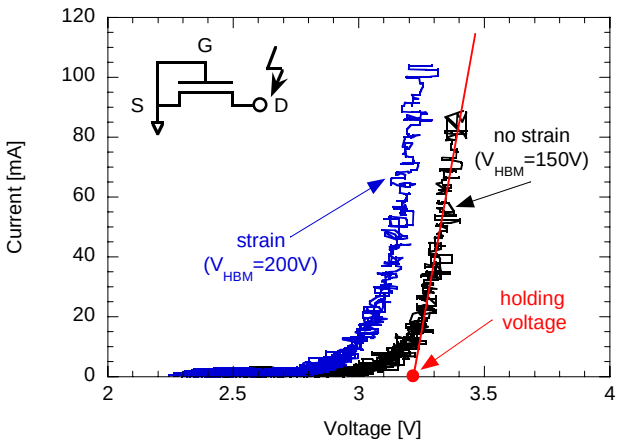



Figure 4.20: HBM-IV curves just before failure for strained and non-strained NMOS FinFETs, where the ESD current is discharged through the parasitic bipolar of the device. No snapback is seen as the parasitic bipolar has its base floating. The devices have a gate length of 155 nm.

performance for strain is due to a lower temperature in the fins owing to higher electron mobility.

On the contrary, the thermal properties of the SiN strain layer were found not to improve the cooling of the fins (Table 4.I). Indeed, the thermal conductivity of the 100-nm SiN strain layer is about four times lower than the one of the 50-nm SiC layer, which is used instead for the non-strained devices between the active device area and the low-k layer. On the contrary, the specific heat capacitance is about the same in both the cases.

## *FinFET NMOS Devices in Parasitic-Bipolar Mode*

Figure 4.20 shows the HBM-IV curves, just before failure, for NMOS FinFETs with and without strain stressed in parasitic-bipolar mode. No snapback is seen as the parasitic bipolar has its base floating enabling uniform turn-on amongst the different fins [Amerasekera02]. Strained devices exhibit a lower holding voltage because of a higher common-emitter current gain ($\beta$) of the parasitic BJT due to larger electron mobility. Moreover, strain improves the ESD robustness up to 30 % (Figure 4.21), which cannot be attributed only to lower power dissipation as for the MOS-diode mode. In [Gossner06] it was shown by failure analysis that FinFETs in bipolar mode can show non-uniformity at high current levels. This non-uniform failure is typical for ESD protection devices based on avalanche breakdown and is due to current instability at high current levels [Vashchenko08]. The different gate-length dependency in FinFET devices with strain (with a maximum sensitivity at medium $L_G$) compared to no-strain indicates a change in failure current uniformity.

Further, a different failure signature is also observed in the voltage versus time waveforms between strained and non-strained devices (Figure 4.22 and Figure 4.23).

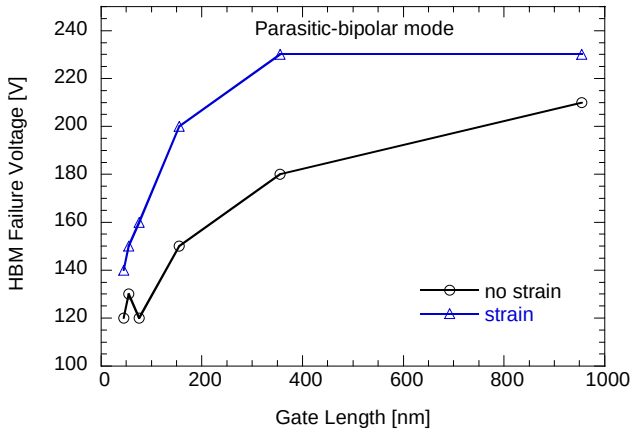



Figure 4.21: HBM-failure voltage as a function of gate length for N-type FinFETs in parasitic-bipolar mode. Strain improves the ESD robustness up to 30 % for medium gate length.

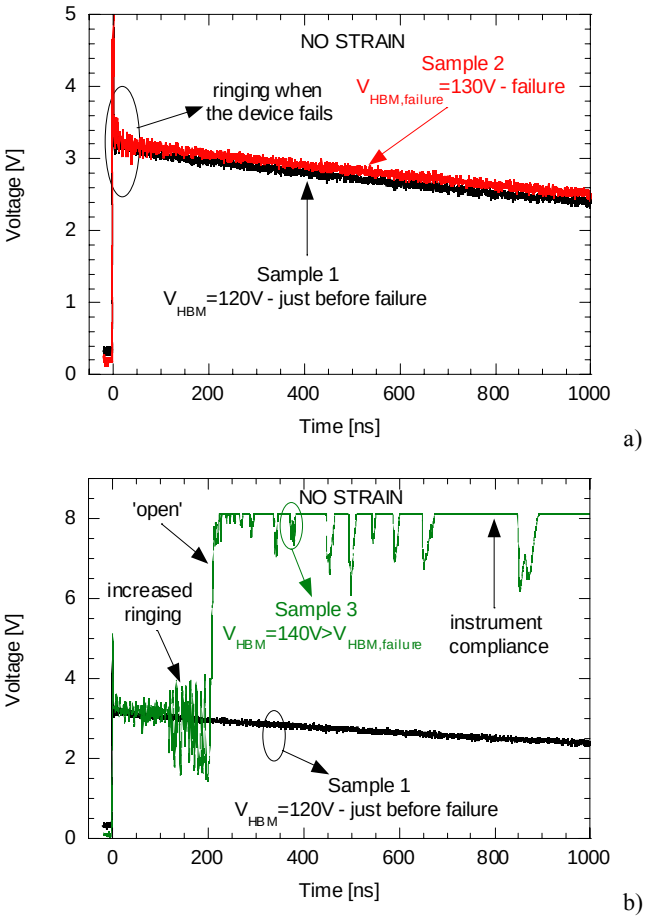



Figure 4.22: HBM-voltage waveforms for a device without strain in bipolar mode with 75 nm gate length. a) when the device fails, a small amount of ringing in the waveform is observed. b) when the stress level is increased on a fresh sample ($V_{HBM}$ = 140 V > $V_{HBM,failure}$ = 130 V), the amplitude of such ringing increases until it diverges to a high-resistive ‘open’ condition.

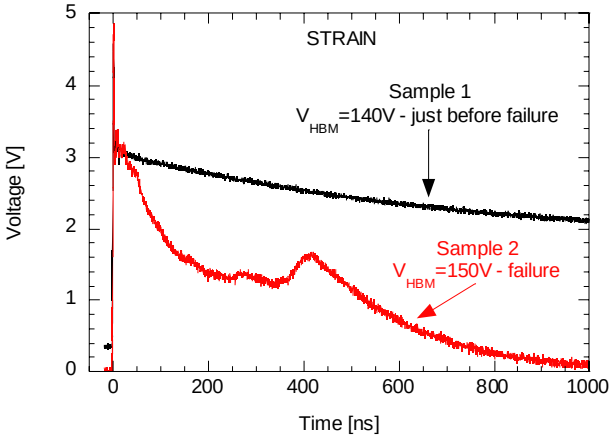



Figure 4.23: HBM-voltage waveform before and during failure of strained FinFET in bipolar mode with 75 nm gate length. When the sample fails, the voltage drops to a 'short'.

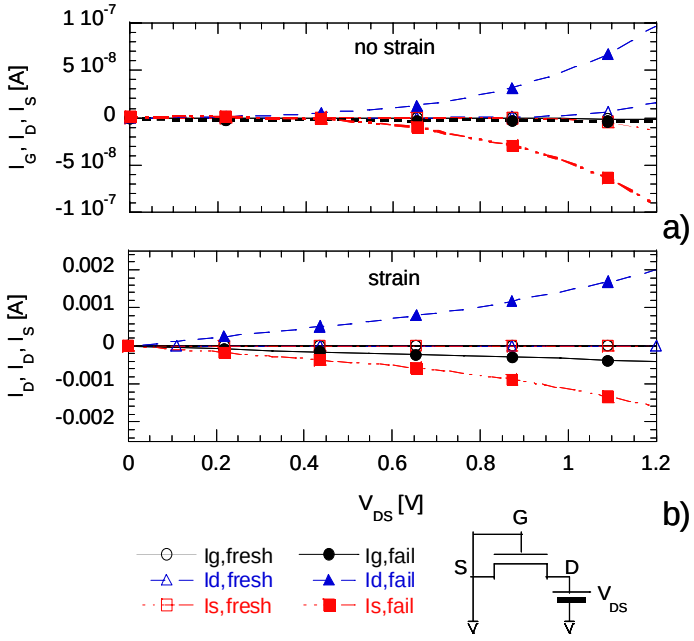



Figure 4.24: $I_{DS}$-$V_{DS}$ (at $V_{GS}$ = 0 V) curves before and after failure for FinFETs without (a) and with strain (b). In the case of no strain, the drain current after failure is in the order of hundreds of nA's, indicating filamentation between source and drain of a few fins. In the case of strain, the current flowing from source to drain shows a large increase up to several mA's, indicating the formation of filaments in almost all fins.

When a non-strained FinFET fails in bipolar mode, an unusual ringing of the HBM voltage waveform is observed at the beginning of the pulse (Figure 4.22a). This indicates a large failure non-uniformity amongst the different fins. A modest increase in DC leakage current (~100 nA), is seen (Figure 4.24a), indicating the occurrence of only a few damaged fins (i.e. filamentation between source and drain). During the next higher ESD

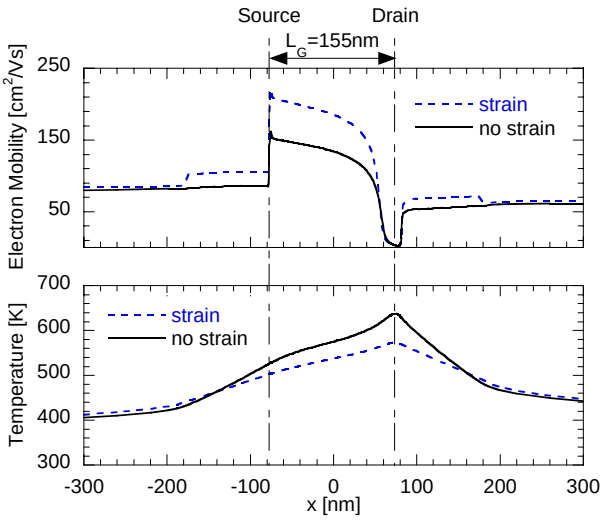



Figure 4.25: TCAD-simulated mobility and temperature profile along the fin length during a 140 V HBM pulse in bipolar mode. Mobility and temperature were captured during the maximum HBM current at 10 ns. Strain increases the mobility and results in a decreased temperature, which also is less peaked. The temperature profile is maximal at the drain where the impact ionization is highest and a sharper peak and higher temperature are seen contrary to the diode mode (Figure 4.19).

stress level, these (pre-)damaged fins need to take all the current and hence are burnt open. Consequently, a few other fins take over, until finally all fins are fused. This unstable mechanism is noticed in the voltage waveform where an increase in the amplitude of the ringing is seen, followed by transition to a high-resistive 'open' condition (Figure 4.22b). However, when a strained FinFET fails, the voltage drops down during the stress (Figure 4.23). The post-stress electrical measurements (Figure 4.24b) suggest filament between source and drain by the abrupt leakage increase (~ mA). The ringing behavior and subsequent 'open' condition are not observed anymore. This indicates a more uniform failure-current distribution for strained devices, meaning the different fins fail more simultaneously, i.e. filamentation, preventing fusing of single fins.

Moreover, the same experiments were performed for non-strained and strained FinFETs with single 'fin' devices of 40 µm (like planar SOI MOSFETs) in parasitic-bipolar mode. Such devices have much less problems with current uniformity at high current levels, since now the current is located within one single wide fin [Trémouilles07]. Strain improves the ESD robustness up to 14 %, however all devices fail to a short condition irrespective of strain. This again indicates that the ringing and 'open' are due to the non-uniform failure between separate fins in multi-fin FinFETs.

The improved failure current uniformity for multi-fin strained FinFET devices can be attributed to the lower maximum temperature observed in strained FinFETs as simulated by TCAD (Figure 4.25), which makes the devices less vulnerable to thermal

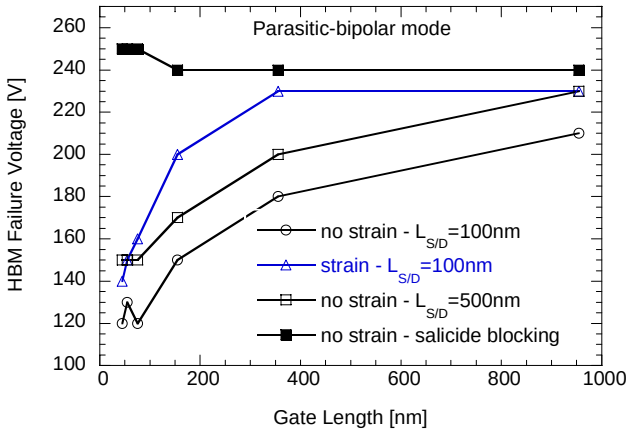



Figure 4.26: HBM-failure voltage as a function of gate length for N-type FinFETs in parasitic-bipolar mode. Silicide blocking and increase in LS/D improve the ESD robustness.

runaway. In MOS-diode mode, the ringing behavior was not observed in both no-strain and strain cases, suggesting uniform failure over the entire fin array. Moreover, similar trends and voltage failure signatures are observed for gated FinFET diodes, which were shown to fail uniformly in [Russ07].

To further substantiate the finding of failure current non-uniformity between different fins, other ESD techniques, which are well known to improve the current uniformity at high current levels [Amerasekera02], were investigated. For non-strained FinFETs, an improvement of the ESD robustness and simultaneously the lack of ringing and 'open' can be obtained by providing finger ballasting, obtained by increasing $L_{S/D}$ (= 500 nm) and/or employing silicide blocking. The latter ensures the failure current uniformity over the entire device array regardless of $L_G$ (Figure 4.26), while still some degree of non-uniformity exists in case of increased $L_{S/D}$ and in case of strain, seen by the dependence on $L_G$.

## *Gated FinFET Diodes*

Figure 4.27 shows the HBM failure level as a function of $L_G$ for strained and non-strained gated FinFET diodes, in which the ESD stress is applied to gate and anode while the cathode is kept grounded. Strain improves the HBM robustness up to 13 % and the trend is similar to the one observed for FinFETs stressed in active MOS-diode mode (Figure 4.18). Similar to the latter, the increased ESD performance for strain is due to lower power dissipation because of higher electron mobility.

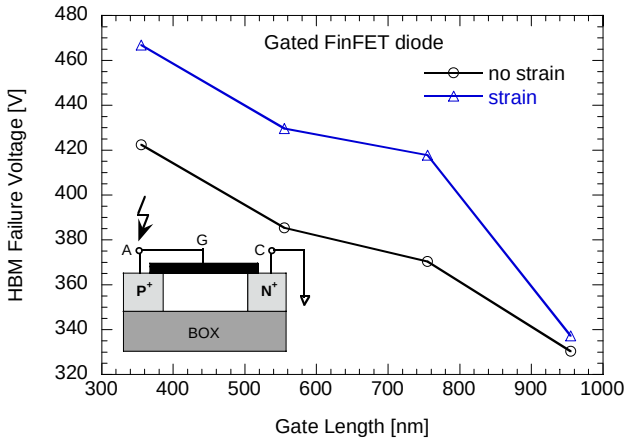



**Figure 4.27:** HBM-failure voltage as a function of gate length for gated FinFET diodes. Strain improves the ESD robustness up to 13 % for short and medium gate lengths.

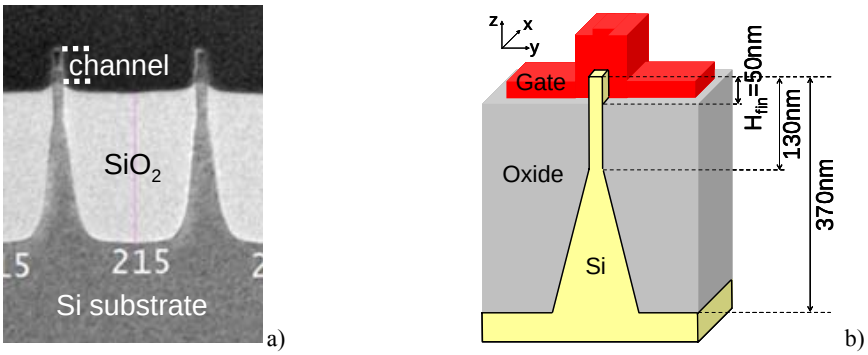



Figure 4.28: a) TEM and b) 3D schematic (not to scale) of a multi-fin bulk FinFET.

## 4.6 Bulk FinFET versus SOI FinFET

In this section, first both bulk FinFET and SOI FinFET technologies are compared. Afterwards, the ESD performance of NMOS FinFETs in parasitic bipolar mode and FinFET gated diodes of both technologies are discussed.

### *4.6.1 Technologies*

The minimal gate length is 45 nm for MOS transistors and 80 nm for gated diodes, fin width is 10 nm minimal, fin number is 400, and fin pitch is 200 nm if $W_{fin} \leq 40$ nm while fin-to-fin spacing is 300 nm otherwise. The distance between source/drain contact area and gate is fixed to 90 nm. For the reference devices, the contact area is 400 nm long and contains 2 rows of 400 contacts each one. For bulk devices also the Source-to-Well

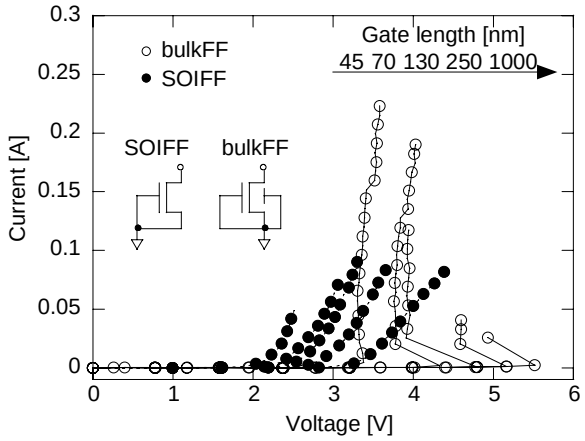



Figure 4.29: TLP I-V curves for NMOS bulk and SOI FinFETs in parasitic bipolar mode with different gate lengths. The devices have fin width of 20 nm, 180 nm fin spacing, and 400 fins in parallel.

Spacing (*SWS*) can be defined. A typical number for *SWS* was 10 μm for our test structures, even if much shorter distances can be realized.

SOI FinFETs ('SOIFF') are processed on SOI wafers with 65 nm Si film thickness ($H_{fin}$) on top of a 145 nm buried oxide (BOX). Bulk FinFETs ('bulkFF') are processed on bulk (100) wafers. For bulk FinFET structures the fin shape makes the fin-height definition difficult (Figure 4.28). However, $H_{fin}$ can be estimated as the portion of the fin wrapped around by the gate, in this case it is 50 nm.

Regardless of the substrate type, the devices feature a high-k gate dielectric (2.3 nm $HfSiO_x$ on 1 nm interfacial oxide) and a 100 nm polysilicon on top of a 5 nm TiN metal gate. In both cases, SOI or bulk substrate, the source/drain access resistance is reduced by SEG of Si on source and drain areas [Collaert08], followed by Ni and NiPt silicidation for SOIFFs and bulkFFs, respectively.

## *4.6.2 NMOS FinFET in Parasitic Bipolar Mode*

In this section, the ESD performance (failure current $It_2$, trigger voltage $Vt_1$, holding voltage $V_h$, and on-resistance $R_{on}$) of bulk NMOS FinFET devices in parasitic-bipolar mode, namely grounded-gate configuration, are investigated and compared to SOI. The devices were stressed by means of an on-wafer TLP system with pulse duration of 100 ns and rise time of 2 ns.

### *4.6.2.1 Gate Length Dependence*

Figure 4.29 shows the TLP IV curves for both NMOS bulkFFs and NMOS SOIFFs with narrow fins ($W_{fin}$ x $N$ = 20 nm x 400) and different $L_G$ stressed in parasitic bipolar

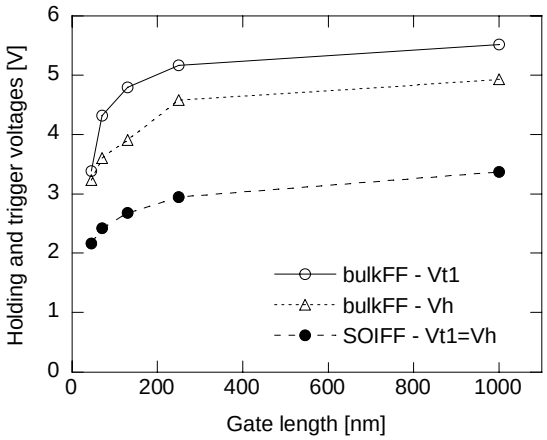



Figure 4.30: Trigger and holding voltages ($Vt_1$ and $V_h$, respectively) as a function of the gate length for NMOS bulk and SOI FinFETs in parasitic bipolar mode. The devices have fin width of 20 nm, 180 nm fin spacing, and 400 fins in parallel.

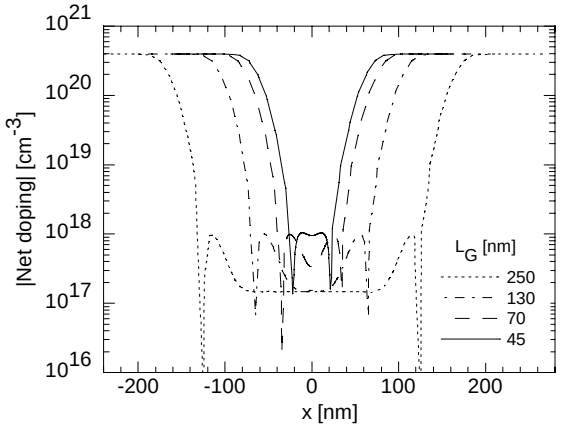



Figure 4.31: TCAD extracted net profiles (absolute value) in a cross section under the channel of a NMOS bulk FinFET. As the gate gets shorter and shorter the effective bulk doping increases because of the merging of the B halo implants. As a consequence the drain-bulk breakdown voltage is reduced.

mode, where the ESD is discharged through the parasitic bipolar (BJT). The trends observed for SOIFFs are similar to the ones already reported in [Trémouilles07]. For SOIFFs no snapback is observed as the parasitic BJT has its base floating. $Vt_1$ and $V_h$ are thus equal as the devices trigger directly at their holding voltages (Figure 4.29 and Figure 4.30) [Amerasekera02] [Yuen94]. For bulkFFs, $Vt_1$ decreases down to $V_h$ with decreasing $L_G$ (Figure 4.29 and Figure 4.30). The decrease in $Vt_1$ with decreasing $L_G$ can be due to the large amount of i) substrate current ($I_{sub}$) and/or ii) substrate resistance ($R_{sub}$), as the snapback condition is defined by [Amerasekera02] [Zhang00]:

$$R_{sub}\, I_{sub} \geq V_{BE,on}. \tag{4.5}$$

Here, $V_{BE,on}$ (≈ 0.6 V) is the base-emitter turn-on voltage. The increase in $R_{sub}$ with decreasing $L_G$ may be due to the increased spreading resistance [Zhang00]. The increase in $I_{sub}$ with decreasing $L_G$ may be due to increased junction leakage current, i.e. the reverse bias p-n junction leakage current and the junction tunnel current, at high drain voltages ($V_{DS}$). This can be attributed to an increase in the lateral electric field with decreasing $L_G$ [Vassilev06] [PhDVassilev]. Another possible reason is the increase in the doping in the bulk due to the merging of the halo implants for short $L_G$ as TCAD simulations show in Figure 4.31 and as already reported in [Boselli03]. Please remember that, contrary to bulkFFs, SOIFFs do not have halo implants. As expected, the $V_h$ increases with increasing $L_G$ for both bulkFFs and SOIFFs (Figure 4.29 and Figure 4.30), because $L_G$ defines the base width of the parasitic BJT which determines $V_h$. In addition, for a given $L_G$, $V_h$ is lower in SOIFFs due to floating base (see section 4.3.2) and a larger common-emitter current gain ($\beta$) of the parasitic BJT because of undoped channel/fin regions in SOIFFs.

Figure 4.29 also shows that the on-resistance is larger for SOIFFs than for bulk ones. This is because SOIFFs have lower junction area (= $N$ ($W_{fin}$ $H_{fin}$)), due to the lack of the bottom junction. In addition, SOI devices are more affected by self-heating because of the presence of the BOX. This allows bulkFFs to achieve much higher $It_2$.

$It_2$ and the power to failure ($P_f = Vt_2\, It_2$, where $Vt_2$ is the failure voltage) normalized per intrinsic silicon width ($W_{intr}$) as a function of the gate length for both SOIFFs and bulkFFs with narrow fins are shown in Figure 4.32 and Figure 4.33, respectively. A different $L_G$ dependency is observed comparing bulkFF and SOIFF.

For SOIFFs, $It_2$ and $P_f$ increase with increasing $L_G$, as the failure current uniformity improves with increasing $L_G$ (see section 4.3.1). For the long gate length, $It_2$ slightly drops down, as the dissipated energy is risen due to the increase in voltage drop ($V_h$). This leads to a maximum $It_2$ per intrinsic width (11.5 mA/µm) at medium $L_G$ and a maximum $P_f$ per intrinsic width (45 mW/µm) at the long $L_G$.

On the contrary, for bulkFFs, $It_2$ decreases monotonically with increasing $L_G$, leading to a maximum $It_2$ per intrinsic width (28.8 mA/µm) at the shortest $L_G$ (Figure 4.32). Also $P_f$ decreases monotonically, from 103 mW/µm to 15 mW/µm, with increasing $L_G$ (Figure 4.33). For medium and long gate lengths $It_2$ and $P_f$ are "unexpected" lower than for SOIFFs. This suggests that thermal failure is not the only failure mechanism of bulkFFs.

For $L_G \geq 250$ nm, the devices fail few ESD zaps after the triggering. Here, $V_{DS}$ is maximum (> 5 V) and higher than for short $L_G$ (Figure 4.29). All these elements suggest a gate-oxide (GOX) breakdown located near the overlap region between the gate and drain

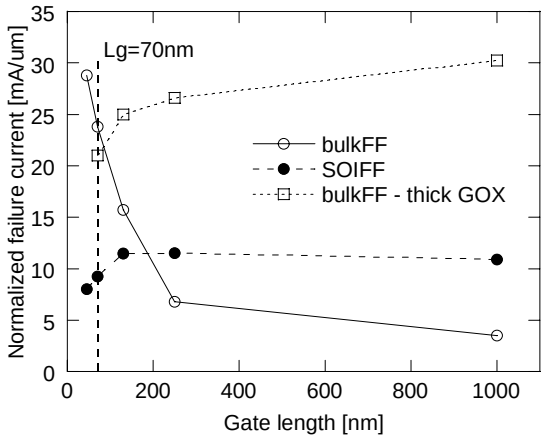



Figure 4.32: Normalized $It_2$ per intrinsic width ($W_{intr} = W_{fin}\ N$) as a function of the gate length for NMOS bulk and SOI FinFETs in parasitic bipolar mode. The devices have fin width of 20 nm, 180 nm fin spacing, and 400 fins in parallel.

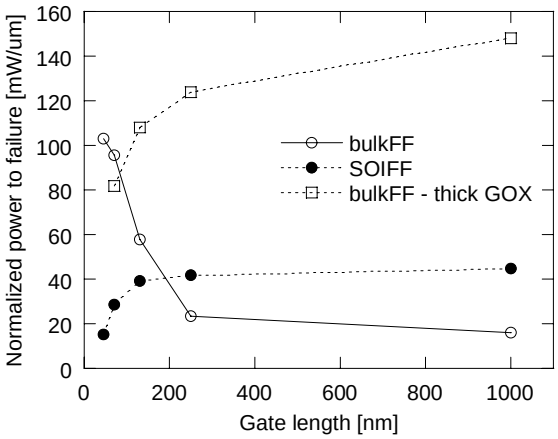



Figure 4.33: Normalized power to failure per intrinsic width ($W_{intr} = W_{fin}\ N$) as a function of the gate length for NMOS bulk and SOI FinFETs in parasitic bipolar mode. The devices have fin width of 20 nm, 180 nm fin spacing, and 400 fins in parallel.

extension due to an enhanced electric field across the GOX [Salman02]. To further substantiate this conjecture, two kinds of experiments were performed:

1) TLP measurements on bulk FinFETs with same geometry but processed with thick gate oxide (6 nm $SiO_2$).
2) Full DC measurement of the different terminal (drain, source, and gate) currents versus the gate voltage (at $V_{DS} = V_{BS} = 0$ V) on reference narrow-fin bulkFFs with different $L_G$. Such DC characteristics were measured in fresh conditions (no ESD stress was applied) and immediately after failure.

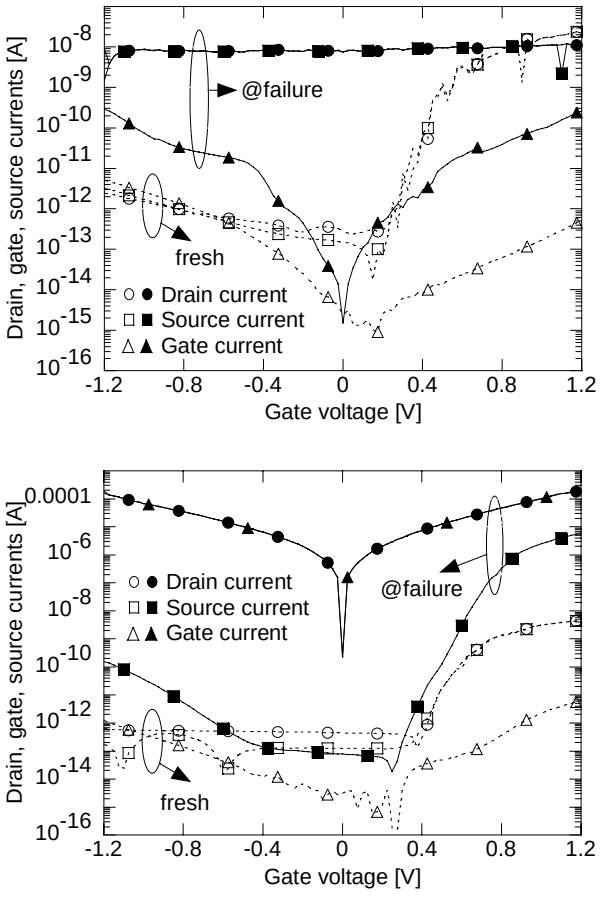



Figure 4.34: Gate, source, and drain currents versus gate voltage ($V_{DS}$ = $V_{BS}$ = 0 V) before ESD stress and after failure for bulk FinFETs with fin width of 20 nm, 180 nm fin spacing and 5 fins in parallel and a) 70 nm gate length or b) 250 nm gate length.

Concerning 1), for bulkFFs with thick GOX both $It_2$ and $P_f$ now increase with increasing $L_G$, leading a maximum $It_2$ and $P_f$ (30 mA/µm and 148 mW/µm, respectively) at the longest $L_G$ (Figure 4.32 and Figure 4.33). For such devices the failure is therefore due to thermal issues and the increased $It_2$ and $P_f$ with increasing $L_G$ is attributed to the enhanced current uniformity at high current levels and perhaps higher heat capacity, similar to SOIFFs (see section 4.3.1). For $L_G$ = 70 nm, $It_2$ is lower for bulkFFs with thick gate oxide compared to the reference bulkFFs with thin GOX (Figure 4.32). This effect can be attributed to the lack of halo implants for bulkFFs with thick GOX, as already reported in [Guo07] [Jiang96] for planar bulk MOSFETs.

Concerning DC measurements, for bulkFFs with thin GOX and short $L_G$ (i.e. 70 nm), both drain and source currents are identical and do not depend on the applied electric field across the GOX (Figure 4.34a). This suggests a possible source-drain

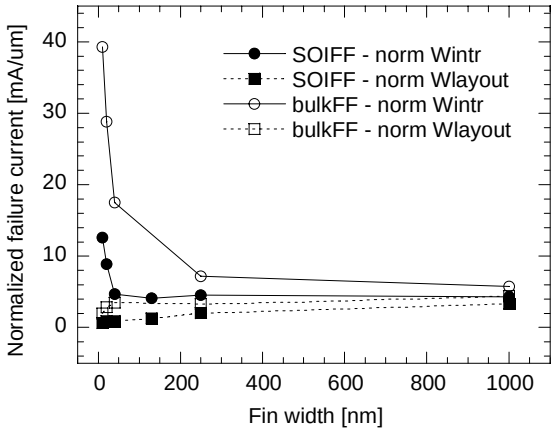



Figure 4.35: Normalized $It_2$ per intrinsic width ($W_{intr} = W_{fin}\ N$) and per layout width ($W_{layout} = W_{fin}\ N + (N\text{-}1)\ S$) as a function of the fin width for NMOS bulk and SOI FinFETs with 45 nm gate length.

filamentation (see section 3.3), probably due to melted materials first in the silicon channel and secondly through the GOX. The latter may explain the modest increase in the gate leakage current (≈ 100 pA), indicating the occurrence of GOX breakdown. On the contrary, bulkFFs with medium or long $L_G$ (i.e. 250 nm) show a significant increase in the gate and drain leakage currents (≈ 100 μA) indicating the occurrence of a hard GOX breakdown close to the overlap region between the gate and drain extension (Figure 4.34b). Notice that, for medium and long $L_G$, source and drain currents depend on the electric field across the GOX. Therefore, the source-drain filamentation has not occurred (see section 3.3).

For reference bulkFFs with $L_G \leq 130$ nm, which were shown to fail due to thermal issues (i.e. source-drain filamentation) in Figure 4.34, the improvement in $It_2$ with reducing $L_G$ may be due to a more uniform turn-on of the parasitic BJT. This can be attributed to the reduction in $Vt_1$ (down to $V_h$) with decreasing $L_G$, following the general observations for planar bulk technologies.

### *4.6.2.2 Fin Width Dependence*

Figure 4.35 shows $It_2$ normalized per intrinsic silicon width and per layout width as a function of the fin width for both SOIFFs and bulkFFs. As already reported in section 4.3.1 for SOIFFs, also bulkFFs exhibit a similar increase in intrinsic performance with decreasing $W_{fin}$ due to the higher effective heat capacity of the 3D-gate. For wider fins, this 3D-nature of the gate disappears and the device becomes very similar to a planar device, leading to a decrease in $It_2/W_{intr}$. A further reason is that the fin-to-fin spacing slightly increases, from 160 nm in the case of $W_{fin}$ = 40 nm to 190 nm for $W_{fin}$ = 10 nm. This leads to a slight decreased fin-to-fin heating, as reported for SOIFFs in [Thijs09].

When comparing the intrinsic ESD robustness of the SOI vs bulk, an improvement up to 3.2x is observed for narrow-fin bulkFFs over narrow-fin SOIFFs and minimum $L_G$. However, the respective maximum $It_2$ as a function of $L_G$ for a given $W_{fin}$ has to be compared since the two technologies exhibit a different $L_G$ dependency (Figure 4.32). Under this circumstance, an improvement up to 2.5x is still observed for narrow-fin bulkFFs over narrow-fin SOIFFs. Such amelioration is only 1.3x for wide-fin samples. The absence of BOX and the better thermal stability (100° C improvement) of the NiPt silicide (for bulkFFs) than the Ni silicide (for SOIFFs) [Lauwers04] cannot fully explain such improvement and why the factor of amelioration is larger for narrow-fin devices. This improvement can be attributed to the trapezoidal fin shape of bulkFFs (Figure 4.28), which increases the heat dissipation through the bulk silicon. For narrower fins, the percentage of the silicon-triangular area compared to the total silicon area is larger, leading to an improvement in the heat dissipation.

When normalizing to layout width however, for both bulkFFs and SOIFFs, $It_2$ decreases with decreasing $W_{fin}$ (Figure 4.35). This is because for narrower fins, there is relatively more area overhead due to the fin-to-fin spacing, making the narrow fins less area efficient than wider fins (see section 4.3.1).

## *4.6.3 FinFET Gated Diodes*

In this section, first the fin-width dependency of the ESD robustness of both SOIFF and bulkFF gated diodes is investigated. Afterwards, the impact of the number of contact rows (*ct#*) on the ESD robustness is analyzed. Finally, ESD-RF considerations are carried out, taking into account the $W_{fin}$ and *ct#*.

### *4.6.3.1 Fin Width Dependence*

The TLP IV curves for both SOIFF and bulkFF diodes with different $W_{fin}$ x $N$ are shown in Figure 4.36. It is clear that bulkFF diodes exhibit an improvement in $It_2$ (up to 9x for narrow $W_{fin}$) and $R_{on}$ compared to SOIFF samples.

Contrary to SOIFF diodes, for bulkFF devices the current can also flow below the silicon area wrapped around by the gate (= $W_{fin}$ $H_{fin}$ per each fin). This is because the junction depth ($x_j \approx 100$ nm) is larger than $H_{fin}$ and because of the presence of the bottom part of the junction, due to the lack of BOX. Therefore, to understand and compare the ESD performance of the two technologies, an effective cross section ($\sigma_{eff}$) can be defined for bulkFF diodes. We propose a definition of $\sigma_{eff}$ as follows:

$$\sigma_{eff} = H_{fin,eff} W_{fin} N, \tag{4.6}$$

where $H_{fin,eff}$ is the effective fin height given by:

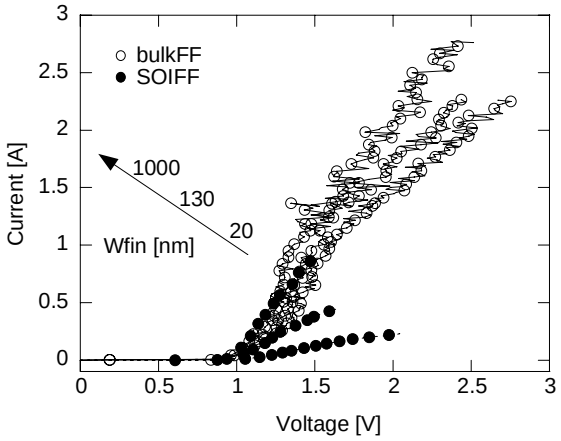



Figure 4.36: TLP IV curves for P-well bulk and SOI FinFET gated diodes with floating gate. The devices have gate length of 80 nm and different fin width x number of fins in parallel (20 nm x 400, 130 nm x 184, and 1000 nm x 64).

$$H_{fin,eff} = \begin{cases} H_{fin}^{(SOIFF)} \dfrac{It_{2,wide}^{(bulkFF)}}{It_{2,wide}^{(SOIFF)}} & for\ bulkFF \\ H_{fin}^{(SOIFF)} & for\ SOIFF \end{cases} \quad (4.7)$$

Here, $H_{fin}^{(SOIFF)}$ is the fin height of the SOIFF diodes and $It_{2,wide}^{(bulkFF)}$ and $It_{2,wide}^{(SOIFF)}$ are the failure currents of bulkFF and SOIFF diodes, respectively, with a single 'fin' of 80 µm. Such diodes are in essence planar diodes. Indeed, $It_2/W_{intr}$ = 35 mA/µm was measured for both bulkFF and conventional planar bulk diodes with the same width and gate length. To highlight and distinguish the impact on the $It_2$ of bulkFF technology from the planar bulk and SOI, $It_2$ normalized per $\sigma_{eff}$ is forced to be the same for both SOIFF and bulkFF diodes with a single 'fin' of 80 µm (Figure 4.37).

For bulkFFs the calculated $H_{fin,eff}$ is 185.4 nm. The better heat dissipation of bulk devices, due to the lack of the BOX, the different junction depth, and the "useful" bottom junction diode defined by the fins are already considered in (4.3). When decreasing Wfin, $It_2$ normalized per $\sigma_{eff}$ increases for both technologies (Figure 4.37) due to the improved cooling of the fins [Thijs08]. A further improvement (up to 3.1x) is observed for the narrow-fin bulkFF diodes compared to the SOIFF ones with the same $W_{fin}$. Such amelioration can be attributed to the following reasons (reported in order of importance):

a) The trapezoidal fin shape, which can improve the heat removal (see section III.B).
b) The additional parasitic diode, defined by the fin-to-fin spacing, at the bottom of the anode/cathode landing pad (LP).

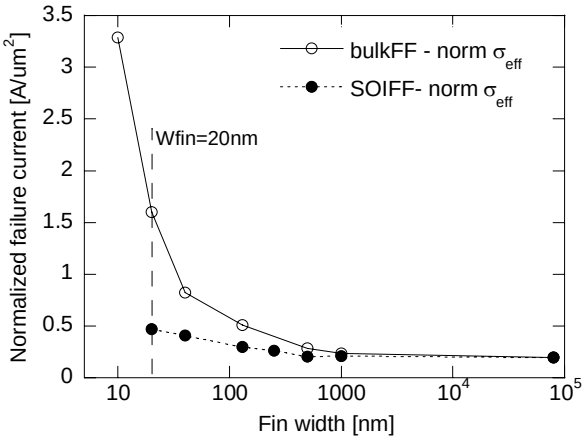



Figure 4.37: Normalized $It_2$ per effective cross-section as a function of the fin width for P-well bulk and SOI FinFET gated diodes with floating gate and gate length of 80 nm.

c) The lower channel doping in narrow fins when compared to wider fins for bulkFFs. This is because of the increased doping / side surfaces scattering of low-energy doping ions [Pelaz08]. This leads to a lower $R_{on}$ at high current levels and thus less self-heating. On the contrary, SOIFF diodes are not affected by this effect as they have undoped channel/fin regions.

### *4.6.3.2 Number of Contact Rows Dependence*

Figure 4.38 shows $It_2$ normalized per $\sigma_{eff}$ as a function of ct# for both bulkFF and SOIFF gated diodes with $L_G$ = 80 nm and $W_{fin}$ x $N$ = 20 nm x 400 or 50 µm x 1. The ESD robustness as a function of ct# depends on the fin width and on the substrate type (SOI vs. bulk).

Concerning SOIFF diodes, $It_2$ increases up to 30 % (with respect to $ct\# = 1$) with increasing $ct\#$ for wide fins, while it is much higher and constant for narrow fins. For these last, the heat is mainly removed by the lateral gates [Thijs08] and secondly by the heat spreading in the LP. These reasons and the (relative) low values of current density ($It_2/\sigma_{eff}$ = 0.5 A/µm$^2$) explain why for narrow-fin SOIFF diodes the full thermal capacity is reached using only one contact row. On the contrary, for wide-fin SOIFF devices the 3D cooling of the gate is strongly reduced since such devices are in essence planar diodes. In addition, the heat spreading along the LP width, which is equals to $W_{fin}$, is not possible because both heat and current flow uniformly in the whole LP width. For these reasons, the increase in contact holes is the only way to improve the thermal capacity.

Concerning bulkFF narrow and wide-fin diodes, $It_2$ increases with increasing $ct\#$. The largest ESD improvement (up to 76 % with respect to $ct\# = 1$) occurs for narrow-fin

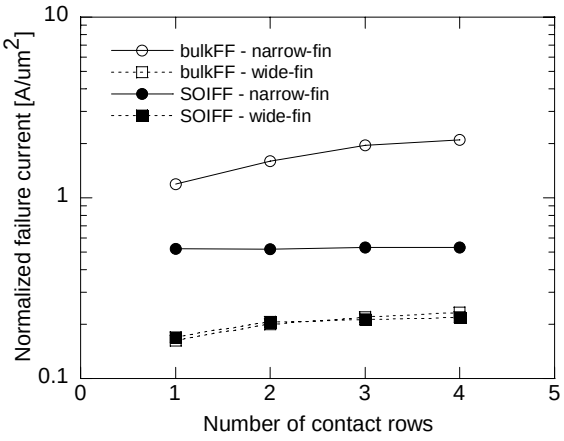



Figure 4.38: Normalized It2 per effective cross-section as a function of the number of contact rows for P-well bulk and SOI FinFET gated diodes with gate length of 80 nm. The devices have fin width of 20 nm, 180 nm fin spacing and 400 fins in parallel ('narrow-fin') or one single 'fin' 50 µm wide ('wide-fin').

bulkFF devices, while for the wide-fin ones is 42 %. For bulk devices, it is well known that an increase in ct# (and also in $L_{cont}$) induces an increase in the area of the junction diode at the bottom of the LP. This explains why wide-fin bulkFF diodes show a larger improvement (up to 12 %) with increasing ct# compared to SOIFF ones. This is difficult to see in Figure 4.38 due to the semi-logarithmic scale. For narrow-fin bulkFF diodes, contrary to SOIFF ones, due to the very high current densities ($It_2/W_{intr} \geq 1.8$ A/µm$^2$), the full thermal capacity cannot be reached using only one contact row. In this case, adding extra contact rows and adding thereby extra silicon volume and junction-diode area contribute to a larger thermal tolerance, increasing $It_2$.

## 4.7 ESD-RF Considerations

When gated diodes are used in high-speed or RF applications, also the parasitic capacitance ($C_{tot}$) is an important parameter. For these applications, the question is whether the strong intrinsic $It_2$ improvement observed for narrow-fin bulkFF diodes compared to wide-fin bulkFF and SOIFF ones (Figure 4.36) results in improved Figure-Of-Merit (FOM). The FOM to be considered is $It_2$ per capacitance [mA/fF] [Thijs08]. RF S-parameter measurements followed by de-embedding of the metal interconnects were performed on two available gated diodes in RF configuration. The gate was left floating, yielding a lower capacitance than when connected to anode or cathode. The first diode had $W_{fin}$ x $N$ = 20 nm x 400 and 80 nm $L_G$, while the second one had a single wide fin (like planar) of 80 µm width and same $L_G$ (= 80 nm).

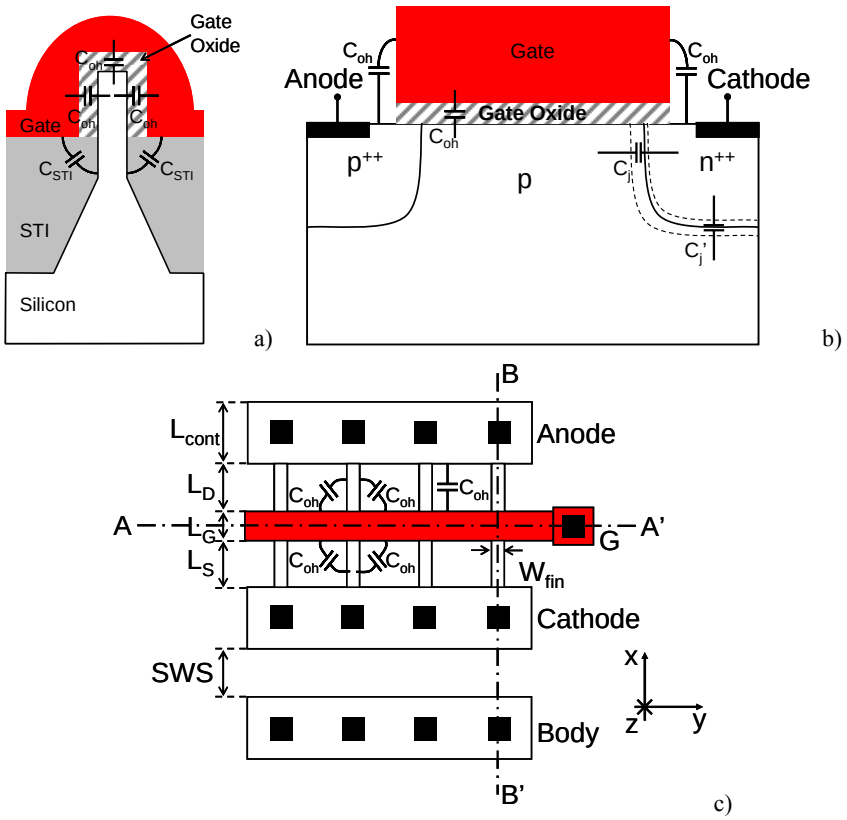



Figure 4.39: Schematic cross-section (not to scale) of a bulk FinFET diode in the a) y-z (A-A') plane, b) x-z (B-B') plane, and c) x-y plane with the corresponding parasitic capacitances.

According to [Thijs08], for SOIFF gated diodes, the measured capacitances were 20 fF and 32.5 fF, respectively, resulting in a FOM of 11.5 mA/fF for the narrow-fin diode and 33.4 mA/fF for the wide-fin one. This means that, when considering capacitance as an optimization goal, wide-fin SOIFFs have better performance. This is because narrow-fin devices are strongly affected by gate overlap and fringing capacitances [Thijs08].

For bulkFF gated diodes, the measured capacitances were 75 fF and 90 fF, respectively, resulting in a FOM of 31.6 mA/fF for the narrow-fin diode and 32.9 mA/fF for the wide-fin one. Despite the larger intrinsic $It_2$ improvement for narrow-fin bulkFF diodes, narrow and wide-fin bulkFF diodes have the similar ESD-RF performance, which is similar to the best one of SOIFF diodes.

$$C_{tot}[fF] = C_j N\left(W_{fin} x_j\right) + C_{oh} N\left(W_{fin} + 2H_{fin}\right) + \\ + C_j'\left[NW_{fin}\left(L_{cont} + L_{S/D}\right) + \left(N-1\right) SL_{cont}\right] + C_{STI}\, 2N\left(H - H_{fin}\right) \tag{4.8}$$

To understand these results for bulk FinFET diodes, formula (4.8) was derived. $C_{tot}$ is divided into four parts (Figure 4.39). The first contribution equals the junction capacitance $C_j$ from anode to cathode which is proportional to the junction cross-section ($W_{fin} \cdot x_j$). The second contribution represents the overhead capacitance $C_{oh}$ proportional to the total gate width ($W_{fin} + 2 \cdot H_{fin}$) and consists of gate overlap and outer fringing capacitance between the fins and gate [Wu07]. These two parts are also present in SOIFF structures, as already reported in [Thijs08]. BulkFF devices are also affected by other two parasitic capacitances. A third contribution is the bottom junction capacitance $C_j'$, which is proportional to the anode/cathode LP area and to $W_{fin}$. The last contribution is the Shallow Trench Isolation (STI) capacitance $C_{STI}$, which is proportional to the height of the fin isolated by the STIs. This capacitance consists of the inner fringing capacitance, which is due to the field lines originating from the lower face of the gate electrode and terminating in the lower region of the fin region [Manoj08]. The additional contribution of the parallel plate capacitance, which is due to the field lines from the lower face of the gate electrode terminating on the top bulk Si surface, is (in first approximation) negligible, similar to SOIFF devices.

Equation (4.4) consists of four unknowns, namely $C_j$, $C_{oh}$, $C_j'$, and $C_{STI}$. $C_j$ and $C_{oh}$ can be found by solving the set of equations for both narrow and wide-fin SOIFF devices, while $C_j'$ and $C_{STI}$ can be found by solving the set of equations for both narrow and wide-fin bulkFF samples. The parasitic capacitances $C_{fin}^{(SOIFF)}$ and $C_{fin}^{(bulkFF)}$ were measured for the narrow-fin ($N_{fin}$ = 400 and $W_{fin}$ = 20 nm) SOI FinFET and bulk FinFET diodes, respectively. Similarly, the parasitic capacitances $C_{pla}^{(SOIFF)}$ and $C_{pla}^{(bulkFF)}$ were measured on the single wide-fin ($N$ = 1 and $W_{fin} = W_{pla}$ = 80 µm) SOI FinFET and bulk FinFET diodes, respectively. A solution for $C_j$ and $C_{oh}$ can be analytically derived as a function of the narrow and wide-fin SOI FinFET devices and is given in (4.5) and (4.6), respectively. A solution for $C_j'$ and $C_{STI}$ can be analytically derived as a function of the narrow and wide-fin bulk FinFET devices and is given in (4.7) and (4.8), respectively.

$$C_j\left[fF/\mu m^2\right] = \frac{N_{fin}\left(W_{fin} + 2H_{fin}^{(SOIFF)}\right)\frac{C_{pla}^{(SOIFF)}}{W_{plan}} - C_{fin}^{(SOIFF)}}{N_{fin}\,2\left(H_{fin}^{(SOIFF)}\right)^2} \tag{4.9}$$

$$C_{oh}\left[fF/\mu m\right] = \frac{2H_{fin}^{(SOIFF)}C_{fin}^{(SOIFF)} - \left[N_{fin}\left(W_{fin} + 2H_{fin}^{(SOIFF)}\right)\frac{C_{pla}^{(SOIFF)}}{W_{plan}} - C_{fin}^{(SOIFF)}\right]W_{fin}}{2N_{fin}H_{fin}^{(SOIFF)}\left(W_{fin} + 2H_{fin}^{(SOIFF)}\right)} \tag{4.10}$$

$$C_j'\left[fF/\mu m^2\right]=\frac{C_{pla}^{(bulkFF)}-\left[C_j\left(W_{pla}x_j\right)+C_{oh}\left(W_{pla}+2H_{fin}^{(bulkFF)}\right)\right]}{\left(L_{cont}+L_{S/D}\right)W_{plan}} \tag{4.11}$$

$$C_{STI}\left[fF/\mu m\right]=\frac{\frac{C_{fin}^{(bulkFF)}}{N_{fin}}}{2\left(H^{(bulkFF)}-H_{fin}^{(bulkFF)}\right)}- \\ +\frac{\left\{C_j\left(W_{fin}x_j\right)+C_{oh}\left(W_{fin}+2H_{fin}^{(bulkFF)}\right)+C_j'\left[W_{fin}\left(L_{cont}+L_{S/D}\right)+\frac{N_{fin}-1}{N_{fin}}SL_{cont}\right]\right\}}{2\left(H^{(bulkFF)}-H_{fin}^{(bulkFF)}\right)} \tag{4.12}$$

Here, $H^{(bulkFF)}$ (= 370 nm) is the sum of the height of the straight fin and the height of the trapezoidal fin for a bulk FinFET devices.

For the narrow-fin bulkFF device, $C_j$ is only 1.4 %, $C_{oh}$ is 20.6 %, and $C_{STI}$ is 18.6 % of the total capacitance, while the main contribution (59.4 %) is due to $C_j'$. On the contrary, for wide-fin bulkFF samples, $C_{STI}$ is negligible (0.04 %), $C_{oh}$ is 28.8 %, and the "useful" contributions $C_j$ and $C_j'$, which participate to the ESD current flow, are 11.56 % and 59.6 %, respectively.

$It_2$ and $C_{tot}$, both normalized towards $W_{intr}$, together with the derived FOM ($It_2$ per capacitance) as a function of the fin width are shown in Figure 4.40. Symbols indicate measurement results while for intermediate fin width, the parasitic capacitance is

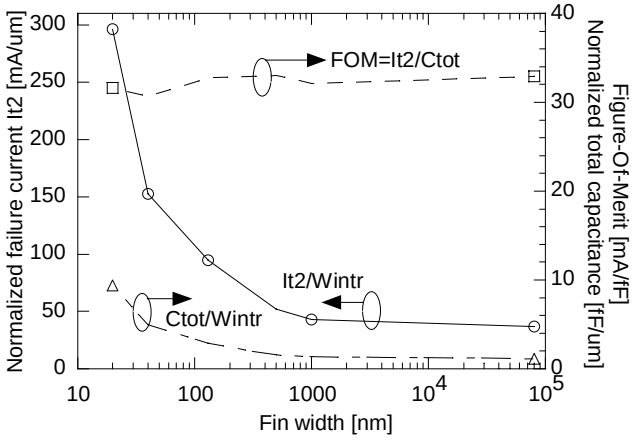



Figure 4.40: Normalized failure current $It_2$ and parasitic capacitance per intrinsic width ($W_{intr} = W_{fin}\,N$) as a function of the fin width for bulk FinFET gated diodes. The derived FOM ($It_2/C_{tot}$) does not depend on the fin width. The symbols indicate measurement data points.

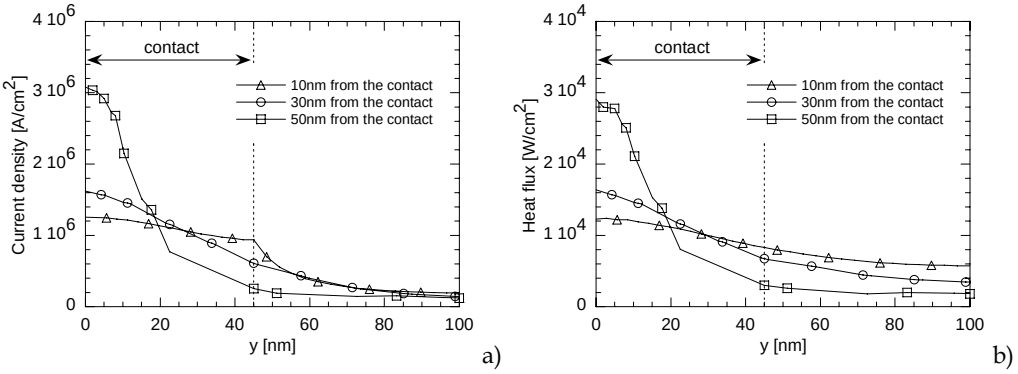



Figure 4.41: TCAD-simulated a) current density and b) heat flux distributions along the landing pad in the *y* direction of a narrow-fin bulk FinFET diode with 80 nm gate length at 0.5 A 100-ns TLP pulse. Current density and heat flux were captured at 80 ns. *y* = 0 nm corresponds to the center of the fin.

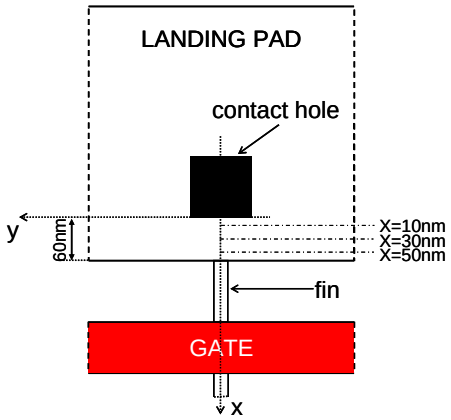



Figure 4.42: Top view of a landing pad and relative distances from the contact hole used to capture the simulated heat and current spreading in Figure 4.41.

calculated using (4.4). Even though the strong $It_2/W_{intr}$ improvement, narrow-fin bulkFF diodes do not exhibit any improvement in the ESD-RF performance with respect to wide-fin ones. This cannot be fully explained by the only large $C_{oh}$ and $C_{STI}$.

To further substantiate this conjecture, 2D TCAD simulations were performed. Figure 4.41 shows the current and heat spreading in the anode/cathode LP at different distances ($x$ = 10 nm, 30 nm, and 50 nm) from the contact (see Figure 4.42) for a narrow-fin bulkFF diode stressed with a 0.5 A TLP pulse. Close to the contact (i.e. $x$ = 10 nm) the current and heat spreading are almost uniform along the (90-nm) contact width. The heat and current flowing out of the contact width are 35.4 % and 20.3 %, respectively, of the total amount. On the contrary, when the distance from the contact is increased (i.e. $x$ = 50 nm) the current and heat densities are mainly focused in a 20 nm range, which corresponds to the fin width. This is because the heat and current flows are practically the

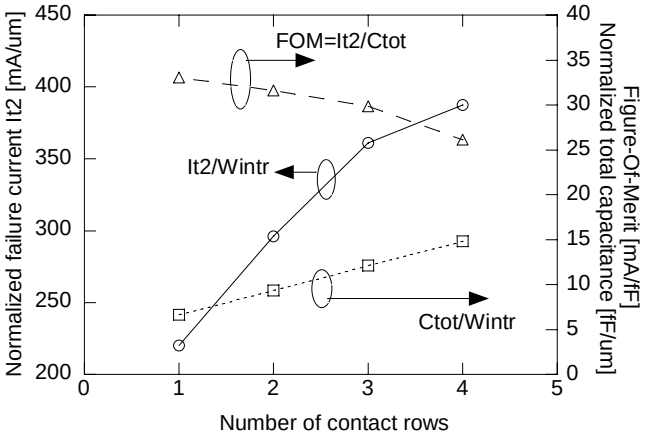



Figure 4.43: Normalized failure current $It_2$ and parasitic capacitance per intrinsic width ($W_{intr} = W_{fin}\ N$) and derived FOM ($It_2/C_{tot}$) as a function of the number of contact rows for bulk FinFET gated diodes with gate length of 80 nm, fin width of 20 nm, 180 nm fin spacing and 400 fins in parallel.

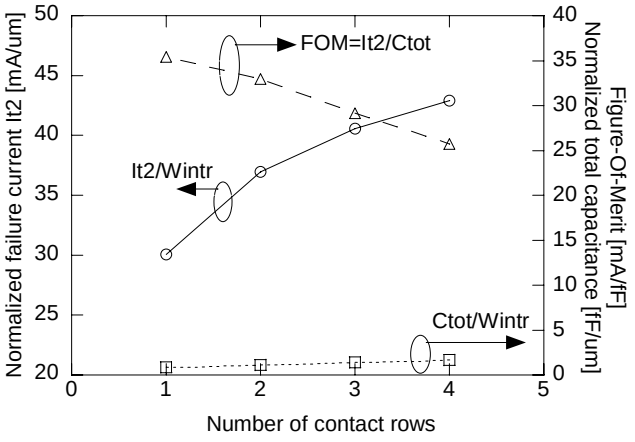



Figure 4.44: Normalized failure current $It_2$ and parasitic capacitance per intrinsic width ($W_{intr} = W_{fin}\ N$) and derived FOM ($It_2/C_{tot}$) as a function of the number of contact rows for bulk FinFET gated diodes with gate length of 80 nm and a single fin 50 μm wide.

same to the ones in the fin since the distance from the fin is only 10 nm while the distance from the contact hole is 50 nm. Therefore, for narrow-fin bulkFF diodes the landing pad is not fully used during the current conduction due to the fin-to-fin spacing; however, the full junction contributes to the parasitic capacitance. For wide-fin bulkFF diodes the bottom junction fully contributes to both current conduction and capacitance. For SOIFF diodes the LP capacitance is negligible because of the presence of BOX.

The impact of *ct#* on the FOM should be investigated since it affects both $C_j'$ and $It_2$. Since, for bulkFF gated diodes, the main contribution in total parasitic capacitance is due to the bottom junction capacitance, the question is if a reduction in $L_{cont}$ results in a

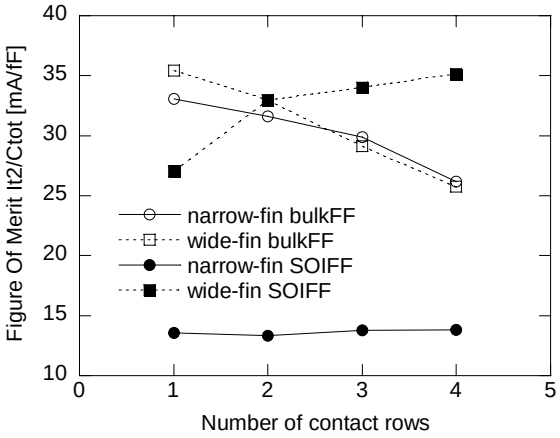



Figure 4.45: Derived FOM (It2/Ctot) as a function of the number of contact rows for bulk FinFET and SOI FinFET gated diodes with gate length of 80 nm. The devices have fin width of 20 nm, 180 nm fin spacing and 400 fins in parallel or a single 'fin' 80 μm wide.

better FOM, despite the decrease in ESD robustness (Figure 4.38). Figure 4.43 and Figure 4.44 show the measured $It_2$ and the total capacitance calculated from equation (4.4), both normalized towards $W_{intr}$, together with the derived FOM ($It_2$ per capacitance), as a function of number of contact rows for narrow and wide-fin bulkFF diodes, respectively. FOM increases with decreasing *ct#* (and decreasing $L_{cont}$), indicating that the best ESD-RF performance (33.1 mA/fF and 35.4 mA/fF for $W_{fin}$ x $N$ = 20 nm x 400 and $W_{fin}$ x $N$ = 80 μm x 1, respectively) is achieved for the short LP length, namely one contact row. When only one contact row is used an improvement in the ESD-RF performance compared to 4 contact rows up to 26 % and 38 % for narrow and wide-fin bulkFF diodes, respectively. This improvement is lower for narrow-fin devices because of a larger contribution in the total parasitic capacitance of $C_{oh}$ and $C_{STI}$ (Figure 4.45). On the other hand, for SOIFF diodes $C_{tot}$ does not depend on $L_{cont}$ because of the presence of BOX. For narrow-fin SOIFF devices FOM does not depend on *ct#*, while for the wide-fin ones it increases (up to 30 % with respect to one contact row) with increasing *ct#*. This leads to similar FOM (≈ 35.3 mA/fF) for the wide-fin SOIFF diode with 4 contact rows and the wide-fin bulkFF device with only one contact row (Figure 4.45).

## 4.8 Conclusions

This chapter provides fundamental insights into the behaviour of FinFET devices under ESD conditions for various layout and process conditions. ESD measurements showed that FinFET devices can have a reasonably good ESD robustness. The ESD performance is influenced by both inter- and intrafin current non-uniformities, which

depend heavily on the layout and process parameters. FinFET technology development is still facing a lot of process challenges which have a direct impact on the ESD performance of the devices.

A comparison between bulk FinFET and SOI FinFET structures has been carried out. For NMOS FinFETs in bipolar mode, different gate-length dependencies between the two technologies (SOI vs bulk) and an improved ESD robustness for bulk FinFET, up to 2.5x, have been observed. Bulk FinFET gated diodes have been demonstrated to have quite larger ESD robustness, up to 9x, compared to SOI FinFET diodes. The ESD-RF performance has been deeply analyzed by means of TCAD simulations and a new model for the parasitic capacitances of bulk FinFET structures has been developed, highlighting the role of device geometry and of the landing pad. For narrow-fin bulk FinFET gated diodes, the landing pad has been demonstrated to not be fully used during the current conduction; however, the full junction contributes to the parasitic capacitance of the device. Therefore, narrow and wide-fin bulk FinFET diodes have similar ESD-RF performance, comparable to the best SOI FinFET diodes.

All the results demonstrate that the possible extreme sensitivity of FinFET devices would not be a showstopper for the advanced nanotechnologies if ESD is considered during the technology development. However, even with this knowledge, the design of ESD protection for FinFET technology appears to be a challenging task for the future.

# Chapter 5

# Ionizing Radiation Effects

An overview of the radiation environments is presented; afterwards, the radiation effects on electronic devices, focusing on the single event effects and on the total-ionizing-dose effects, are reviewed.

## 5.1 Radiation Environments

Nearly every chip is hit by some sort of radiation. Not even a circuit protected by several meters of concrete can be safe, since alpha particles can originate inside the chip due to radioactive contaminants.

In the following, the most important radiation environments, such as space, the atmospheric environment, the high energy physics environment and the nuclear power plant environment, are described. The end of this paragraph is dedicated to another source of radiation: the alpha-emitter contaminants.

### *5.1.1 Space Radiation Environments*

#### *5.1.1.1 Trapped Particles*

Charged particles that come into contact with the Earth's magnetic field can become trapped in the near-Earth environment [Dodd99]. These particles include electrons, protons, and heavy ions. The trapped particle belts (Van Allen belts, Figure 5.1) consist of two regions of trapped particles: an inner and an outer belt, separated by a region of reduced particle flux (the so-called "slot" region). Although the origin of trapped particles in the near-Earth environment is not completely understood, sources include the solar wind and transient solar events, cosmic ray particles from interplanetary space, and reaction products from cosmic ray collisions with the Earth's atmosphere.

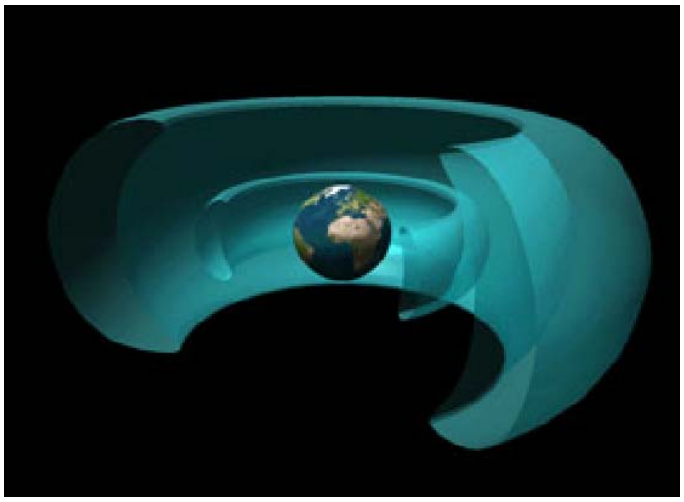


Figure 5.1: Diagram of Earth's Van Allen radiation belts [Mazur02].

### *Protons*

Regardless of origin, energetic protons do exist in the near-Earth environment and are one of the most prominent sources of damage on electronic devices. They range in energy from tens of keV to hundreds of MeV, with fluxes as high as $10^5$ protons/cm$^2$/s for protons with energy > 30 MeV [Barth97]. Protons with these energies are easily able to penetrate shielding and impinge on electronics within a spacecraft [Lum04].

Probably the most important region for protons is the South Atlantic Anomaly (SAA), a region off the east coast of South America with greatly increased proton flux at altitudes less than 1000-2000 km. The SAA exists because of the difference between the Earth's geographic spin axis and its magnetic axis, which causes a localized region of lower magnetic field off the Argentine coast [Barth97] [Dyer98]. During passes through the SAA, the flux of energetic (> 30 MeV) protons can be more than $10^4$ times as intense than at equivalent altitudes over other regions of the Earth. The SAA is illustrated in Figure 5.2, which shows flux contours for protons with energy > 30 MeV as a function of latitude and longitude at altitudes of 500 km (Figure 5.2a), 1000 km (Figure 5.2b), and 3000 km (Figure 5.2c). At low altitudes, the SAA is highly localized, and as altitude increases, the SAA becomes less distinct until at 3000 km (Figure 5.2c) the normal Van Allen belt structure re-emerges.

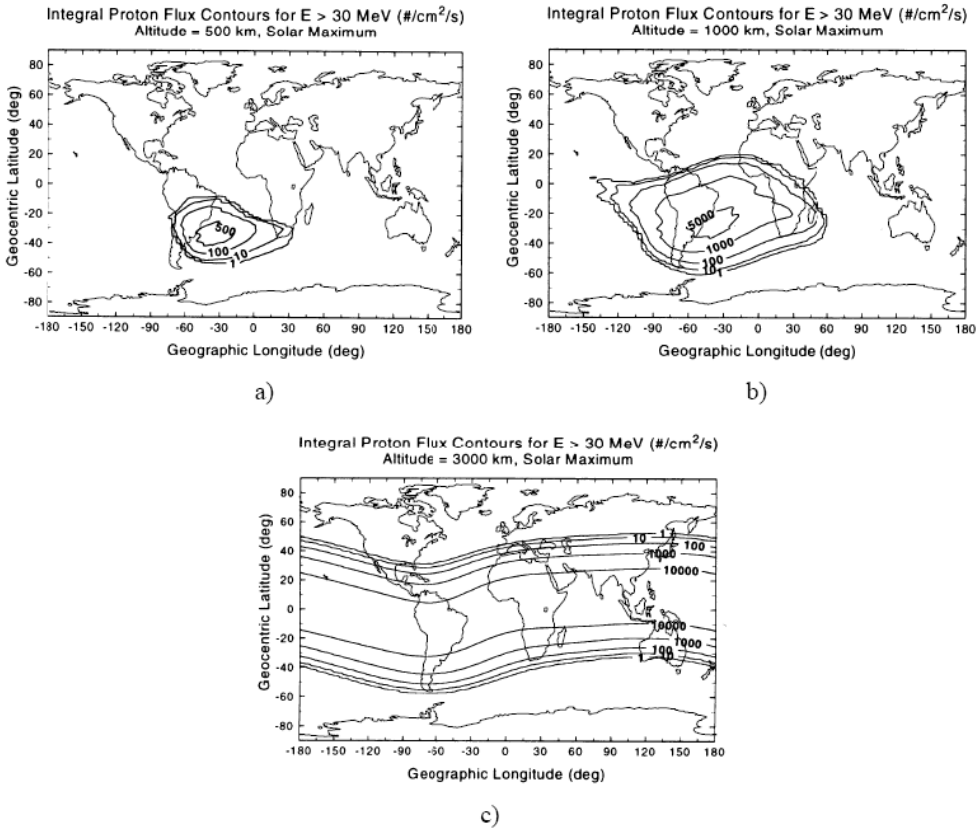



Figure 5.2: Integral proton flux contours as a function of latitude and longitude [Dodd99].

## *Heavy Ions*

The Van Allen belts are predominantly composed of trapped electrons and protons, but it is now well accepted that heavy ions are also trapped by the Earth's magnetic field [Barth03]. The origin of these particles is thought to be anomalous cosmic rays, which are neutral interstellar particles that drift into the solar system, become ionized by the solar wind and accelerated to 10's of MeV/nucleon, and are subsequently trapped by the magnetosphere [Barth97]. Several kind of heavy ions have been measured, such as He, C, N, O, and Ne. The peak in trapped heavy ion fluxes is at altitudes just above the inner proton belt. Because the trapped heavy ions have relatively low energies (10's of MeV/nucleon), these particles may not penetrate through spacecraft shielding and therefore are not expected to be a major concern for electronic devices.

### *5.1.1.2 Transient Particles*

#### *Solar Event Protons and Heavy Ions*

The activity level of the Sun is never constant, but follows a cyclical variation of active years followed by quiet years [Lum04]. The period of recent solar cycles has varied between 9 and 13 years, with an average of about 11 years. Solar cycle activity is frequently gauged by the observed number of sunspots, but many solar processes show the same variation. This includes the incidence of energetic solar events, with maximum numbers of solar flares occurring during active years. Solar events still occur during solar quiet times, but they occur less frequently. Solar events can be broadly characterized as being either gradual or impulsive [Barth97]. The gradual events produce a raised particle flux that decays slowly over several hours or even days. These events are proton-rich and can produce high-energy (> 30 MeV) proton fluences higher than $10^9$ protons/cm$^2$ accumulated over a few days. Gradual events are responsible for the majority of large proton fluence events, and occur at a frequency of about 10 per year during solar maximum conditions. Impulsive events are by definition of much shorter duration (hours at most), and are marked by increased fluences of heavy ions and low energy electrons. Impulsive events produce heavy ion fluences that can be orders of magnitude above the galactic cosmic ray background. These heavy ions have energies ranging from tens of MeV/nucleon to hundreds of GeV/nucleon, but at the upper end of this range the flux falls below the galactic cosmic ray background.

#### *Galactic Cosmic Rays*

Solar event particles are true transient particles in the sense that elevated fluxes of particles are observed only for a short time following an event. In contrast, Galactic Cosmic Rays (GCR) form a background component of radiation that shows a slow cyclical variation with solar activity [Dodd99] [Sexton92] [Barth03]. GCR are composed of very highly energetic protons and heavy ions that come from outside the solar system. These particles must fight against the solar wind to enter the solar system and are therefore at their maximum intensity at solar minimum and drop off a factor of 2 to 10 at solar maximum. The particle composition of GCR is shown in Figure 5.3. Protons comprise about 83 % of the GCR flux, He nuclei (alpha particles) account for 13 %, 3 % are electrons, and the remaining 1 % are heavier nuclei. Even though they are not very abundant, heavy ions are very important because they deposit the most energy per unit path length. Because they are so energetic (tens of MeV/nucleon to hundreds of GeV/nucleon), they do not become trapped and are not significantly attenuated by spacecraft shielding. GCR that hit the atmosphere form a cascade of secondary particles, as discussed in the next section.

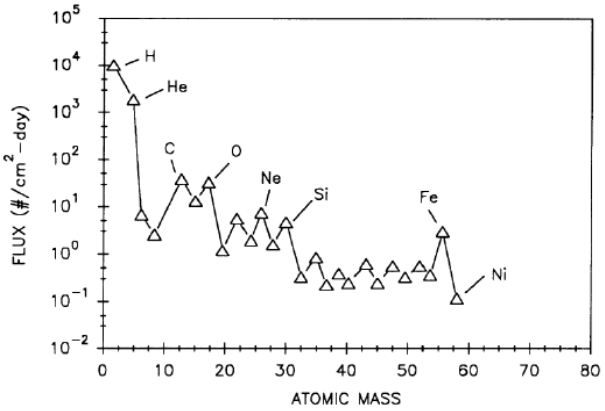



Figure 5.3: Particle composition of galactic cosmic rays [Dodd99].

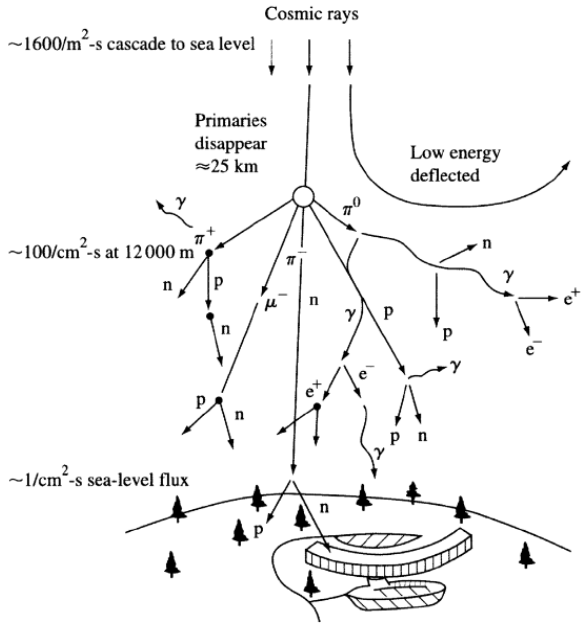



Figure 5.4: Particle shower produced by cosmic rays [Dodd99].

## *5.1.2 The Atmospheric Radiation Environment*

The atmospheric radiation environment comes about as a result of the space radiation environment impinging on Earth's atmosphere. As very highly energetic cosmic rays enter the upper atmosphere they interact with oxygen and nitrogen in the atmosphere and produce a cosmic ray shower of daughter products. The primary galactic cosmic rays are so energetic that some of the daughter products can reach all the way through the atmosphere to ground level, equivalent to passing through more than 13 feet of concrete.

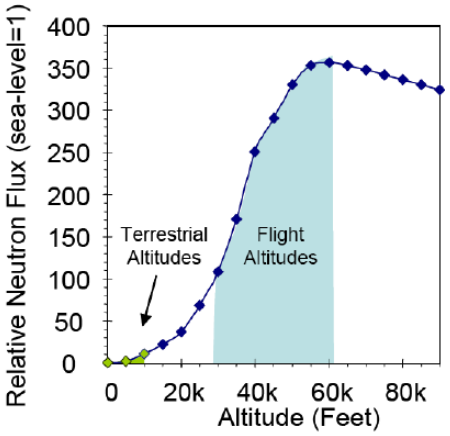



Figure 5.5: Neutron flux variation with altitude [Baumann05].

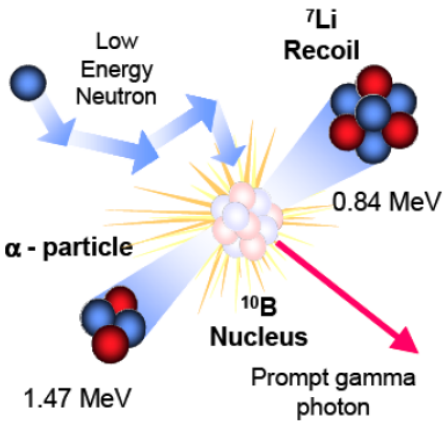



Figure 5.6: Upon capturing a neutron the B nucleus becomes unstable and breaks apart, emitting two ionizing particles: a 1.47 MeV alpha particle and a 0.84 MeV lithium recoil [Baumann05].

A diagram of a cosmic ray shower is shown in Figure 5.4 [Dodd99]. The daughter products primarily responsible for causing soft errors in high-altitude and terrestrial electronics are neutrons and protons. The fluxes of neutrons and protons have similar characteristics with respect to energy and altitude variation, with both populations extending to energies greater than 1 GeV. Both neutrons and protons show a maximum flux at an altitude of 17-18 km, with the sea-level flux being several hundred times lower than at aircraft altitudes. A plot of the altitude variation of the neutron flux is shown in Figure 5.5 [Baumann05].

The neutron flux also varies as a function of latitude: the neutron flux is highest at the poles, because the primary galactic cosmic rays can penetrate furthest into the

atmosphere there. The neutron shower from cosmic rays hits the atmosphere with a wide spectrum of energies, but they rapidly lose energy. Most atoms do not readily absorb neutrons, so the end of the cosmic shower is a flux of neutrons at their lowest energy. These are called thermal neutrons, and have about the same velocity as room-temperature atoms (~2000 m/s) [Baumann05]. The thermal neutrons survive up to several seconds since few natural atoms interact with them. Thermal neutrons are a major concern for electronic devices as they may interact with Boron that is extensively used as a p-type dopant in silicon. Boron is composed of two isotopes, $^{11}B$ (80.1 %) and $^{10}B$ (19.9 %). $^{10}B$ is unstable when exposed to neutrons and breaks into ionizing fragments shortly after absorbing a neutron as illustrated in Figure 5.6 ($^{11}B$ also reacts with neutrons; however, its reaction cross-section is nearly a million times smaller, and its reaction products, gamma rays, are much less damaging). The thermal neutron capture cross-section of 10B is extremely high in comparison to most other isotopes present in semiconductor materials - by 3 to 7 orders of magnitude [Baumann05]. Unlike most isotopes that emit gamma photons after absorbing a neutron, the $^{10}B$ nucleus breaks apart with an accompanying release of energy in the form of an excited $^{7}Li$ recoil nucleus and an alpha particle (a prompt gamma photon is also emitted from the lithium recoil soon after fission occurs). The alpha and the lithium recoil are both capable of inducing soft errors in electronic devices.

### *5.1.3 High Energy Physics and Nuclear Power Plants*

High energy physics experiments require the read-out electronics to work under extremely harsh conditions. As an example, it has been estimated that the read-out electronics used in the upgrade of the CERN Large Hadron Collider (LHC) would be subjected to Total Ionizing Dose (TID) close to hundreds of Mrad, with particle fluence up to $10^{16}$ hadrons/cm$^2$ after only 5 years of operation [Gonella07].

Nuclear power plants are another harsh environment from the standpoint of radiation.

### *5.1.4 Alpha Particles*

Radioactive contamination is not rare. Luckily, almost all of this radiation is unimportant. Still, there is one type of radioactive contamination that can produce errors in an IC, that is trace of materials that emit alpha particles (a He nucleus). For example, the first evidence of sea-level soft errors on 16 Kb DRAMs was given by May and Woods (1979). The source of the radiation was traced to alpha particle emission from contaminates in ceramic packing produced in a factory on the Green River, Colorado, which was downstream from an old uranium mine [Ziegler04].

The prime source of alpha particles is from heavy elements such as thorium or uranium, and even the smallest trace contamination of some elements can cause serious problems. The contaminants maybe present into the package or into the solder materials.

Unfortunately, these contaminants cannot be eliminated without incurring in extremely high costs.

## 5.2 Radiation Effects on IC

Depending on the radiation environment in which the chips are immersed, ionizing radiation can produce different effects. Concerning CMOS circuits, there are two broad categories of radiation effects: Single Event Effects (SEE), which are due to a single strike of a particle with high ionizing power; and Total Ionizing Dose (TID) effects, which are due to the progressive build-up of defects caused by the passage of many particles with low ionizing power, such as electrons or protons.

### *5.2.1 Single Event Effects*

#### *5.2.1.1 Basic Mechanisms of Single Event Effects*

All non-destructive single-event effects are caused by the same fundamental mechanism: collection of charge at a sensitive region of a microcircuit following the passage of an energetic particle through the device.

By definition, as ionizing radiation passes through a target material electrons and holes are released along the path of ionizing particles. There are two primary methods by which carriers are released: direct ionization by the incident particle and ionization by secondary particles created by nuclear reactions between the incident particle and the target material. Direct ionization can cause soft errors if the incident particle (such as a heavy ion) is ionizing enough to free a very high density of carriers. For lighter particles (e.g., protons), direct ionization may produce an insufficient amount of charge to cause upset directly and soft errors may instead be due to ionization produced by secondary particles.

##### *Direct Ionization*

An energetic particle passing through a semiconductor material frees charged carriers along its path as it loses energy. When all of its energy is lost, the particle comes to rest in the semiconductor, having traveled a total path length referred to as the particle's range. The terms Linear Energy Transfer (LET) or *dE/dx* is used to describe the energy loss per unit path length of a particle as it passes through a material. LET has the units of $MeV \cdot mg^{-1} \cdot cm^2$, because the energy loss per unit path length (in MeV/cm) is normalized by the density of the target material (in $mg/cm^3$). We can easily relate the LET of a particle to its charge deposition per unit path length, because for a given material it takes a certain amount of energy to release an electron-hole pair. For example,

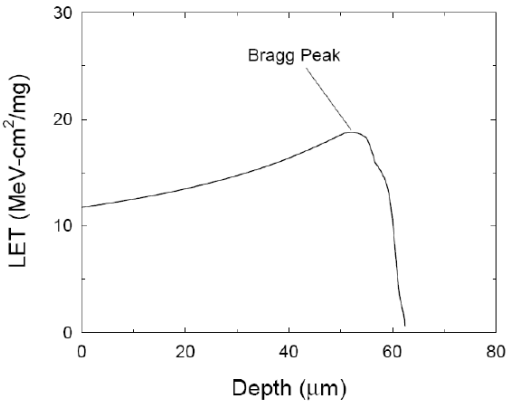



Figure 5.7: Linear energy transfer (LET) vs. depth curve for 210-MeV chlorine ions in silicon [Dod99].

in silicon one electron/hole pair is produced for every 3.6 eV of energy lost, and silicon has a density of 2328 mg/cm$^3$. Using these values it is easy to show that an LET of 97 MeV·mg$^{-1}$·cm$^2$ corresponds to a charge deposition of 1 pC/μm. A curve of particular interest for understanding the interaction of a given energetic particle with matter is the LET of the particle versus depth as it travels through the target material. Figure 5.7 shows such a curve for a 210-MeV chlorine ion traveling through silicon. This figure shows the basic characteristics of ion-induced charge deposition as a function of depth. A peak in the charge deposition occurs as the particle nears its range, and then a precipitous drop in deposition as the particle reaches its range and comes to rest. The peak in charge deposition is referred to as the Bragg peak, and in general occurs as the particle reaches an energy near 1 MeV/nucleon [Petersen97].

Whether or not the charge deposited through direct ionization is sufficient to cause an upset of course depends on the individual device and circuit that has been struck as well as the strike location and trajectory. Direct ionization is the primary charge deposition mechanism for upsets caused by heavy ions. Lighter particles such as protons do not usually produce enough charge by direct ionization to cause upsets in memory circuits, but recent research has suggested that as devices become ever more susceptible, upsets due to direct ionization by protons may occur.

### *Nuclear Reaction Effects*

As mentioned above, direct ionization by light particles usually does not produce a high enough charge density to cause upsets. Unfortunately, this does not mean that we can ignore these lighter particles. Protons and neutrons can both produce significant upset rates due to indirect mechanisms [Dodd99]. As a high-energy proton or neutron enters the semiconductor lattice it may undergo an inelastic collision with a target nucleus. This

may result in the emission of alpha (α) or gamma (γ) particles and the recoil of a daughter nucleus (e.g., Si emits α-particle and a recoiling Mg nucleus), or a spallation reaction, in which the target nucleus is broken into two fragments (e.g., Si breaks into C and O ions), each of which can recoil. Any of these reaction products can now deposit energy along their paths by direct ionization. Because these particles are much heavier than the original proton or neutron, they can deposit higher charge densities as they travel and therefore may be capable of causing a soft error. These inelastic collision products typically have fairly low energies and do not travel far from the particle impact site.

Once a nuclear reaction has occurred, the charge deposition is not greatly different in character from a directly ionizing heavy ion strike. Therefore, once deposited, it is subject to the same fields and concentration gradients and is collected in a similar manner.

### *5.2.1.2 Single Event Effects - Classification*

A particle passing through a semiconductor can give rise to several different effects,

depending on the type and bias conditions of the struck device, on the position of the ion hit and on the features of the impinging particles. The most important are [Dodd99]:

- Single Event Upset (SEU) also known as soft error, because it results in a loss of information and not in permanent damage to the affected circuit (hard error). When a particle strikes a memory cell, it may cause a flip in the stored value, what was memorized as a '0' may become a '1' and vice versa.
- Single Event Latch-up (SEL) occurs when the impinging particle activates parasitic BJT structures, causing high currents to be drawn from the power supply. A power-cycle is needed to restore proper operation, even though permanent damage may occur to the device during the high-current condition.
- Single Event Functional Interruption (SEFI) occurs when a state machine controlling a device, such as a Flash memory or an FPGA, is upset by a heavy ion, causing a stop in the device operation.
- Single Event Gate Rupture (SEGR) occurs when a particle with a high ionizing power impinges on a device biased over a critical voltage causing the rupture of the gate oxide, i.e., the formation of a conductive path which effectively shorts the anode and the cathode.

### *5.2.2 Total Ionizing Dose*

Total ionizing dose effects are related to the progressive build-up of radiation-induced trapped charge and defects inside the exposed devices, caused by low-LET particles.

For MOS device degradation, the primary concern is electron-hole pair generation in oxides. Some fraction of the electrons and holes become trapped in the oxide and they may cause the release hydrogen and induce interface traps at the $Si/SiO_2$ interface.

#### *5.2.2.1 Ionization Effects*

High-energy electrons (secondary electrons generated by photon interactions or electrons present in the environment) and protons can ionize atoms, generating electron-hole pairs [McLeanl87]. As long as the energies of the electrons and holes generated are higher than the minimum energy required to create an electron-hole pair, they can in turn generate additional electron-hole pairs. In this manner, a single, high-energy incident photon, electron, or proton can create thousands of electron-hole pairs. The minimum energy required for creating an electron-hole pair, $E_p$, in silicon, silicon/dioxide and GaAs is given in Table 5.I [Schwank02]. Also given in Table 5.I are the densities for the three materials and the initial charge pair density per rad deposited in the material, $g_0$. The latter quantity is obtained from the product of the material density and the deposited energy per rad divided by $E_p$. A rad (radiation absorbed dose) is a unit used to quantify the total absorbed ionizing dose in a material. It is a measure of the amount of energy deposited in a material and is equal to 100 ergs of energy deposited per gram of material (1 rad = 100 erg/g = $6.24 \cdot 10^{13}$ eV/g). The energy deposited in a device must be specified for the material of interest. Thus, for a MOS transistor, total dose is measured in units of rad($SiO_2$) or rad(Si).

#### *5.2.2.2 Basic Mechanisms of Total Ionizing Dose Effects*

When an MOS transistor is exposed to high-energy ionizing irradiation, electron-hole pairs are created uniformly throughout the oxide. Electron-hole pair generation in the oxide leads to almost all total dose effects. The generated carriers induce the build-up of charge, which can lead to device degradation. The mechanisms by which device degradation occurs are depicted in Figure 5.8 [Schwank02]. Figure 5.8 is a plot of an MOS band diagram for a p-substrate capacitor with a positive applied gate bias. Immediately after electron-hole pairs are created, most of the electrons will rapidly drift (within picoseconds) toward the gate and holes will drift toward the $Si/SiO_2$ interface. However, even before the electrons leave the oxide, some of the electrons will recombine with holes. The fraction of electron-hole pairs that escape recombination is called the electron-hole yield. Those holes which escape "initial" recombination will transport through the oxide toward the $Si/SiO_2$ interface by hopping through localized states in the

| Material | $E_p$ (eV) | Density ($g/cm^3$) | Pair density generated per rad, $g_0$ ($pairs/cm^3$) |
|---|---|---|---|
| GaAs | ~4.8 | 5.32 | ~7 x $10^{13}$ |
| Silicon | 3.6 | 2.328 | 4 x $10^{13}$ |
| Silicon Dioxide | 17 | 2.2 | 8.1x$10^{12}$ |

Table 5.I: Minimum energy for creating electron-hole pairs, density, and pair density generated per rad for GaAs, silicon, and silicon dioxide [Schwank02].

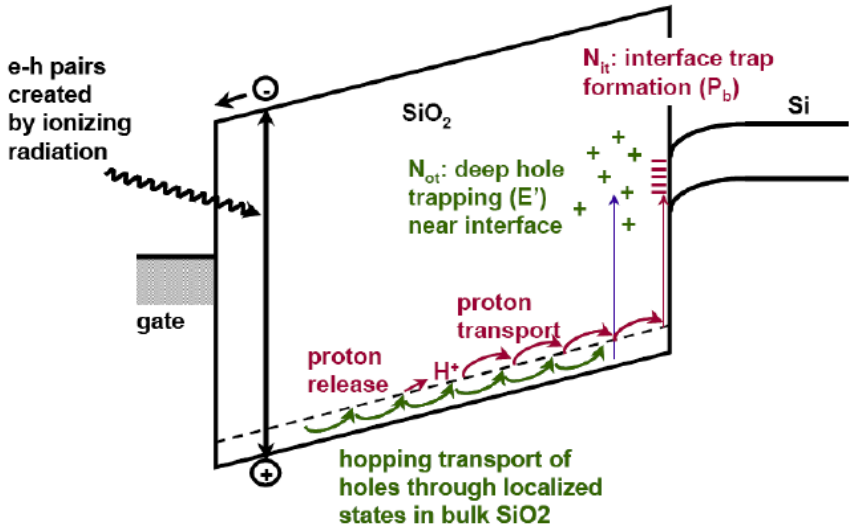



Figure 5.8: Band diagram of an MOS capacitor with a positive gate bias. Illustrated are the main processes for radiation-induced charge generation [Schwank02].

oxide. As the holes approach the interface, some fraction of the holes will be trapped, forming a positive oxide-trap charge. Hydrogen ions (protons) are likely released as holes "hop" through the oxide or as they are trapped near the $Si/SiO_2$ interface. The hydrogen ions can drift to the $Si/SiO_2$ where they may react to form interface traps. At threshold, interface traps are predominantly positively charged for p-channel transistors and negatively charged for n-channel transistors.

In addition to oxide-trapped charge and interface-trap charge buildup in gate oxides, charge buildup will also occur in other oxides including field oxides and Silicon-On-Insulator (SOI) buried oxides [Barnaby05]. The radiation-induced charge buildup in gate, field, and SOI buried oxides can cause device degradation and circuit failure. Positive charge trapping in the gate oxide can invert the channel interface causing leakage current to flow in the OFF state condition ($V_{GS}$ = 0 V). This will result in an increase in the static

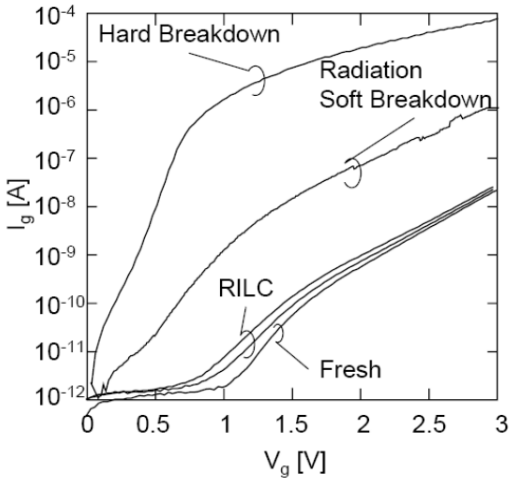



Figure 5.9: Gate Current vs. Gate Voltage ($I_g$-$V_g$) measured before and after irradiation on a 3-nm oxide. The two curves referring to RILC have been measured after irradiation with $5.8 \cdot 10^{10}$ and $1.5 \cdot 10^{11}$ Si ion/cm$^2$. The RSB has been obtained after irradiation with $10^7$ I ions/cm$^2$ [Cester01].

power supply current of an IC and may also cause IC failure. In a similar fashion, positive charge buildup in field and SOI buried oxides can cause large increases in IC static power supply leakage current (caused by parasitic leakage paths in the transistor). In fact, for advanced ICs with very thin gate oxides, radiation-induced charge buildup in field oxides and SOI buried oxides normally dominates the radiation-induced degradation of ICs. Large concentrations of interface-trap charge can decrease the mobility of carriers and increase the threshold voltage of n-channel transistors [Barnaby05]. These effects will tend to decrease the drive of transistors, degrading timing parameters of an IC.

## 5.3 Radiation Effects on Oxides

The gate oxide thinning enhances the device radiation tolerance to charge trapping problems due to TID effects. In fact, being the electron tunneling distance around 3 nm in $SiO_2$, when the oxide thickness reaches 6 nm or less the radiation induced oxide positive charge is easily recombined or neutralized by electrons tunneling from the gate and/or Si substrate. This oxide thickness was approximately reached at the CMOS technological node of 0.25 μm. Following the CMOS technological evolution the gate oxide thickness is now below 2 nm, becoming almost immune to gate oxide charge trapping problems due to the gate oxide transparency to electrons. Still, this last characteristic has become the weak point from a reliability viewpoint [Paccagnella03].

Ionizing radiation (as well as electrical stresses) can in fact produce defects acting not as trapping centers but as the agents of leakage paths across the gate oxide driving an

excess gate current. Gate leakage adversely affects the overall circuit power consumption, which has been often taken as the key parameter for reliability predictions. Figure 5.9 resumes the different leakage currents that may be measured on a thin oxide after irradiation. The characteristics of the leakage currents depend on the oxide thickness and on the ionizing particle LET.

High LET particles may cause a huge increase of the capacitor current (Hard Breakdown). This phenomenon is known as Single Event Gate Rupture (SEGR) and it has been observed on relatively thick oxides irradiated under high oxide fields with high LET particles [Fleetwood00] [Sexton98] [Titus98].

Radiation Induced Leakage Current (RILC) was reported for oxides in the range 4-10 nm [Ceschai98] [Ceschia00_1] [Larcher99]. On the contrary to SEGR, RILC is only a modest increase of the leakage current across the oxide (Figure 5.9) and may be a severe limit for non-volatile memories. When the oxide thickness is scaled well below 4 nm, as in the contemporary CMOS technologies, the leakage current due to the direct tunneling of electrons across the oxide trapezoidal barrier is very large even in unstressed devices and RILC may be negligible.

Finally, Radiation induced Soft Breakdown (RSB) has been observed in 3 and 4 nm oxides only after irradiation with high LET ions [Ceschia99_1] [Ceschia99_2] [Ceschia00_1] [Ceschia00_2], and consists in a large increase of the oxide leakage current, which is however smaller than in hard breakdown regime.

### *5.3.1 Radiation Induced Leakage Current*

The current density – oxide field characteristics ($J_g$-$E_{ox}$) of a 6-nm oxide are shown in Figure 5.10 [Ceschia99_1], before and after a high dose irradiation with 8 MeV electrons produced by a pulsed LINAC accelerator. The main effect of irradiation is represented by the increase of the low-field gate current, observed between $E_{ox}$ = 3 MV/cm and $E_{ox}$ = 6 MV/cm, due to RILC. The oxide trapped charge in the stressed capacitors is negligible, as deduced from the overlap of the high-field characteristics of irradiated and unirradiated devices, corresponding to the Fowler-Nordheim (FN) tunneling regime.

RILC is attributed to the electrons passing through the oxide by Trap Assisted Tunneling (TAT) [Ceschia98_1] [Ceschia00_2] [Larcher99]. RILC features many similarities with Stress Induced Leakage Current (SILC), the main difference being the origin of the oxide traps: the ionizing particles for RILC, the electric stress for SILC. As SILC, RILC is attributed to inelastic TAT: when bias is applied to the gate, electrons can tunnel into the oxide trap where they loose part of their energy and then they reach the anode through another tunnel process (Figure 5.11) [Ceschia98].

An analytical model of RILC has been developed for ultra-thin oxides submitted to ionizing radiation, based on the analytical solution of the Schrödinger equation for a

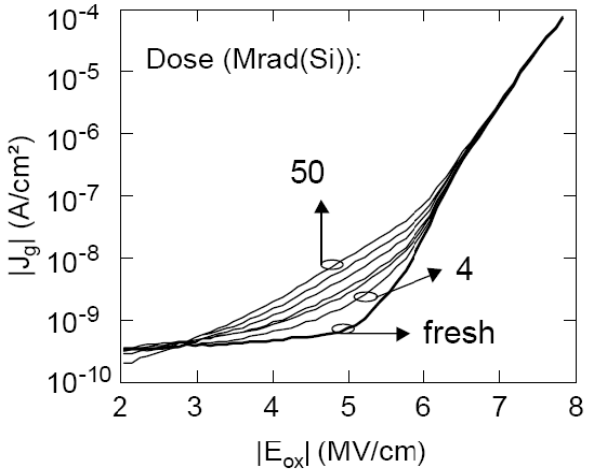



Figure 5.10: Negative $J_g$-$E_{ox}$ curves measured before (fresh) and after irradiation for various doses ranging from 4 to 50 Mrad(Si) [Ceschia99_1].

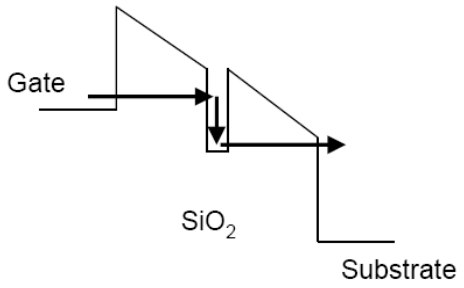



Figure 5.11: Schematic representation of inelastic TAT through a MOS capacitor.

simplified oxide band structure [Larcher99]. Here RILC occurs through a two-step process: first, an electron tunnels into the oxide defect from the cathode conduction band edge. Then, the electron tunnels out the trap after having lost approximately 1.5 eV, in agreement with previous findings for SILC. Simulation results have shown that the most effective traps promoting RILC conduction are located close to the middle of the oxide and are energetically placed 1.3 eV below the oxide conduction band.

A leakage current that may be classified as RILC has been reported also in 10 nm thick oxide after heavy ion irradiation, as illustrated in Figure 5.12 [Candelori01]. Before irradiation the FN injection is established at $|V_g| > 7$ V. After irradiation with I ions an excess leakage current appears between 5 V and 9 V, before and inside the FN regime. No current enhancement is observed after irradiation with Si ions. The excess current, measured in both negative and positive gate voltage sweeps, has been attributed to Multi-Trap Assisted Tunneling (M-TAT), as electrons should tunnel across the oxide through

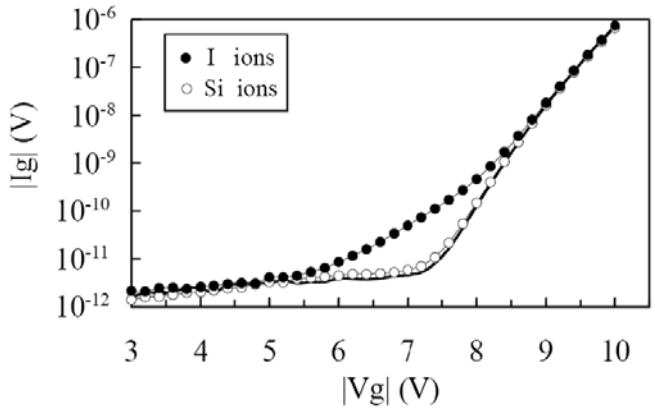



Figure 5.12: $I_g$-$V_g$ curve maeasured on a 10nm thick capacitor after 20 Mrad(Si) iodine (close circles) and silicon (open circles) irradiation. The solid line is the as-received negative $I_g$-$V_g$ curve [Candelori01].

two or more traps. While conventional RILC and SILC may be modeled by inelastic Single-Trap Assisted Tunneling (S-TAT) [Larcher99], in 10-nm oxides the tunneling probability to/from a trap 5 nm far from the interfaces is so low, that S-TAT could not support any measurable DC current. Noticeably, DC SILC has never been observed in 10-nm devices after electrical stresses [DeSalvo00] (the main component of SILC after electrical stresses for oxide thicknesses larger than 10 nm is a transient current, caused by charging/discharging of stress generated traps near the oxide interfaces [Reunnion97]). This means that a critical trap density is needed for M-TAT, which can only be produced by ions with high LET, as low LET Si ions (see Figure 5.12) are unable to produce the excess leakage. Only dense ion tracks can produce locally a high defect density, enabling M-TAT. Moreover, only high ion doses may generate M-TAT in 10-nm oxides: in fact, only for very high oxide defect densities the probability of having some traps aligned along a conductive path is high enough to produce a measurable leakage current.

### *5.3.2 Radiation Soft Breakdown*

The relative increase of the gate current due to RILC is much reduced in oxide thinner than 3-4 nm, due to the increased tunneling current even in a fresh device. A large impact on the gate current is measured instead when a Soft Breakdown (SB) event occurs [Ceschia99_1] [Ceschia99_2] [Conley01] [Massengill01] [Miranda00] [Sexton98]. RSB was detected as a sudden, large increase of the gate current, much larger than in case of RILC (see Figure 5.9), but still smaller than in case of Hard Breakdown. The electrical characteristics of RSB are similar to those ones associated to the SB produced by electrical stresses [Ceschia00_1] and can be modeled following the empirical relation proposed for electrically induced SB [Miranda99]:

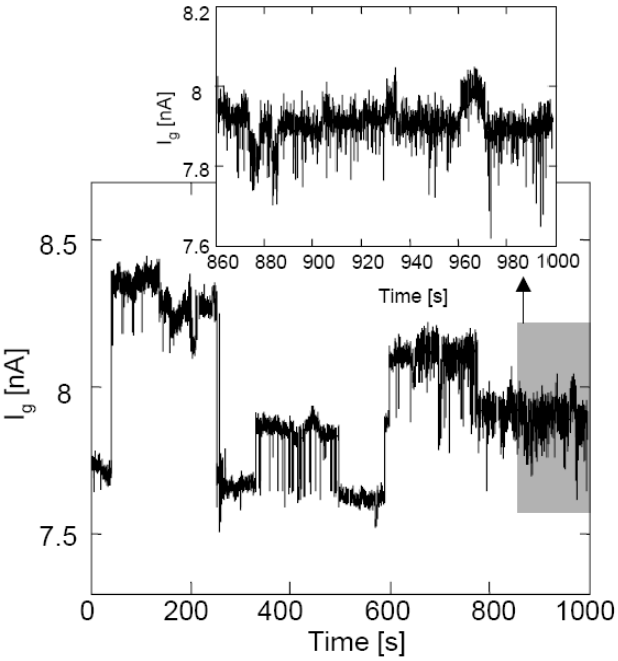



Figure 5.13: Gate current measured at $V_g$=-2.7 V as a function of measurement time in a 3-nm oxide after 7·106 I ions/cm$^2$ [Cester01].

$$I_{RSB} = a \cdot V^b \tag{5.1}$$

In contrast with RILC, which is associated to a tunneling process across a single trap, RSB conduction is activated when one or more regions with high defect density are produced in the oxide layer.

RSB is characterized by Telegraph Noise. Figure 5.13 shows the gate current measured in a 3-nm oxide after irradiation with 257 MeV I ions, at $V_g$ = -2.7 V. The RSB current approximately behaves as a multi-level Random Telegraph Noise (RTN). Such fluctuations correspond to the activation/deactivation of conductive paths (inside the radiation induced weak spots) across the oxide, occurring after irradiation [Cester01]. By focusing on a small portion of the gate current response a "small" RTN appears superimposed on the main "large" fluctuations (see inset of Figure 5.13).

## 5.4 Conclusions

In this chapter, first an overview is given of the different radiation environments, such as space, atmosphere, and high energy physics and nuclear power plants, and the

alpha-emitter contaminants. Afterwards, a review was presented of the radiation effects on electronic devices, focusing on the single-event and on the total-ionizing-dose effects, with particular attention to the radiation effects on the oxides.

# Chapter 6

# Microdose Effects on Ultrathin Body SOI MOSFETs

The short and long-term effects of heavy-ion strikes on 65 nm fully depleted SOI MOSFETs with different strain engineering solutions are studied.

## 6.1 Introduction

The thinning of the gate oxide has made CMOS increasingly robust with respect to radiation-damage. When the thickness of the gate oxide was above 10 nm, threshold voltage shift and mobility degradation due to radiation-induced charge trapping and interface state generation in the gate oxide were the biggest concerns [Oldham03]. As the oxide became thinner, this component has practically disappeared, leaving edge-related leakage current as the most prominent total-dose effect [Faccio05]. Concerning heavy ions, radiation induced leakage current and radiation soft breakdown represent the most visible manifestation of the reduction in gate oxide thickness [Scarpa97] [Ceschia98]. The sporadic collapse of the drain current in MOSFETs with either narrow or short channel has also been reported several times after irradiation with heavy ions, and may seriously challenge the reliability of advanced circuits. It has been attributed to the formation of physically damaged regions in the gate oxide close to the border regions [Cester04]. Long-term impact of irradiation has been investigated as well. Heavy-ion strikes lead to earlier breakdowns and to changes in the degradation kinetics [Cester03].

CMOS technology is now entering a phase where simple shrinking is no longer enough to grant the performance gains required from each new generation of devices. Alternative materials and structures are required. On the one hand, Silicon-On-Insulator (SOI) technology, once confined to niche applications such as rad-hard and low-power

devices, is now entering mainstream thanks to its superior control of short-channel effects and promise for scalability [Celler03]. Mobility-enhancing techniques are increasingly utilized to improve transistor performance as well [Takagi08].

These advanced solutions will be incorporated in future Commercial-Off-The-Shelf (COTS) components that may be used in space applications. It is therefore of primary importance to identify potential issues in these devices.

The total ionizing dose response of SOI technology has been thoroughly analyzed [Schwank03] [Felix04]. Radiation-induced damage to the thick buried oxide is particularly detrimental in fully depleted MOSFETs, due to the front-back channel coupling. The response of SOI devices with ultra-thin gate oxide to radiation has been analyzed using protons and electrons for the 90 nm node [Hayama04] [Simoen04] [Hayama07], and for the 65 nm fully depleted technology (also with strain-inducing techniques) [Put06]. Microdose effects due to single heavy ions strikes have been analyzed only for the 90 nm node, showing also long-term effects related to irradiation [Cester05].

This chapter illustrates how heavy ions impact conventional and strained 65 nm SOI electrical characteristics immediately after exposure, as well as affect long-term reliability. Some of the phenomena already present in previous generation SOI and bulk technologies are still observed in these devices, while others seem to have vanished. New effects peculiar to 65 nm fully depleted devices with strain-inducing engineering devices are also investigated.

## 6.2 Experimental and Devices

We studied 65-nm N-channel Fully Depleted (FD) SOI MOSFETs manufactured by IMEC [Augendre05]. These exploratory devices (Figure 6.1) feature 1.5 nm silicon oxynitride as gate dielectric, 15 nm undoped top silicon layer, 150 nm thick buried oxide (BOX), mesa isolation, and standard layout (i.e. not enclosed). The operating drain voltage ($V_{DD}$) is 1 V. Devices with channel width ($W$) 10 μm and varying channel length ($L$) were used. Polysilicon was used as gate material, causing the threshold voltage of NMOSFETs ($V_{tf}$) to be negative. Production devices will feature metal gates with proper workfunction to adjust $V_{tf}$. Three versions were processed:

1) reference SOI (SOI): reference devices processed on SIMOX substrates;
2) strained SOI (sSOI): fabricated using wafer bonding and a donor wafer with Si-capped $Si_{0.8}Ge_{0.2}$ Strain Relieved Buffer (SRB) [Taraschi];

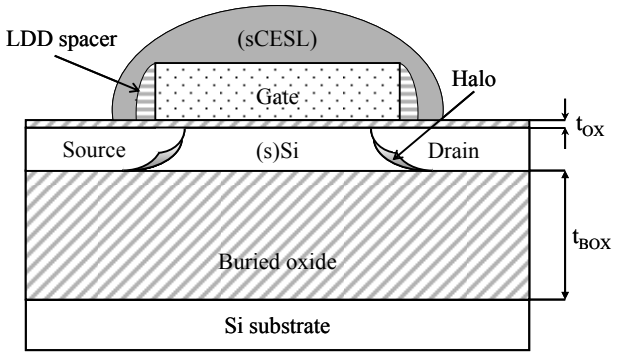



Figure 6.1: Schematic cross-section of the devices under study (not to scale).

3) strained Contact Etch Stop Layer (sCESL+SOI): obtained by depositing (in one step) an additional 100-nm tensile nitride (intrinsic stress 800 MPa) that generates additional uniaxial strain along the channel.

Before and after irradiation and during electrical stresses, on each sample we measured the gate current versus the gate voltage ($I_g$-$V_{gs}$), the drain current versus the gate voltage ($I_d$-$V_{gs}$) at different back-gate voltages, and the drain current versus the drain voltage ($I_d$-$V_{ds}$) at different gate voltages. Some samples were irradiated with 253-MeV I ions (LET = 59 MeV·cm$^2$/mg) at the SIRAD facility of the Tandem Van Der Graaf accelerator at the INFN Legnaro National Laboratories, Italy [Wyss01]. Irradiation was done at the chip level with floating device terminals. Even if this is not the worst-case condition, floating irradiations may give interesting results (for instance about switched-off devices hit by heavy ions) and do not require bonding, which may be problematic in these device due to the lack of ESD protections. Two ion fluences were used, 2.5 ions/μm$^2$ and 1 ions/μm$^2$ (called in the following high and low fluence).

To study the gate oxide time-to-breakdown (TTBD) and the MOSFET degradation kinetics, we submitted irradiated and unirradiated devices to two kinds of electrical stress:

a) Constant Voltage Stress (CVS) at $V_{gs,stress}$ = 2.75 V and $V_{ds}$ = $V_{bs}$ = 0 V on MOSFETs with $W/L$ = 10 μm/0.2 μm and $W/L$ = 10 μm/3 μm;
b) Staircase Voltage Stress (SVS) starting at $V_{gs,stress}$ = 2 V and increasing by 50 mV every 100 s until 4 V, while keeping $V_{ds}$ = $V_{bs}$ = 0 V, on MOSFETs with $W/L$ = 10 μm/10 μm.

The $V_{gs}$ voltage values for the CVS and SVS tests were selected in order to study the degradation mechanisms and the oxide breakdown in a convenient time frame. During each stress step, the gate bias was briefly lowered from the stress voltage to a monitor voltage (1 V) every 1 second, to measure the current at low electric fields, thus permitting

a finer sensitivity on the detection of breakdown events. More than 150 devices have been tested for this work.

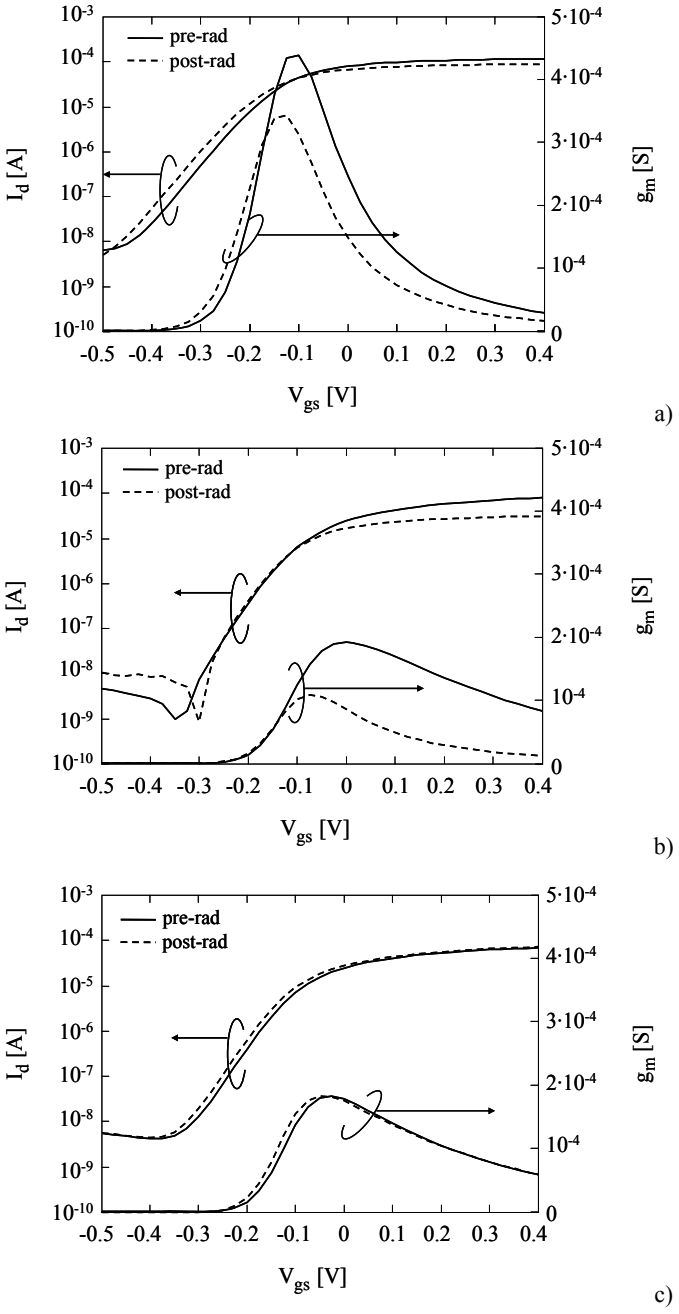



Figure 6.2*: $I_d$-$V_{gs}$* and $g_m$-$V_{gs}$ characteristics ($V_{ds}$ = 25 mV, $V_{bs}$ = 0 V) before and after heavy-ion exposure (2.5 I ions/μm$^2$) for three FD SOI transistors with sCESL: (a) *W/L* = 10 μm/0.2 μm showing both $V_{tf}$ shift and $g_m$ drop, (b) *W/L* = 10 μm/0.75 μm showing only $g_m$ drop, and (c) *W/L* = 10 μm/0.75 μm showing only $V_{tf}$ shift.

## 6.3 Effects Observed Immediately After Irradiation

Even though some of the MOSFETs showed gate oxide breakdown after exposure due to Radiation Soft Breakdown (RSB) [Ceschai00_1] [Ceschai00_2], in this chapter we will focus only on those samples in which the gate current did not significantly change. We begin our analysis with the post-radiation characteristics of the devices. Some transistor types are more affected than others depending on the channel length and on the strain-level. sCESL+SOI samples with $L < 1$ μm experience the largest degradation, while conventional SOI and sSOI devices are less impacted by the exposure. Concerning the sCESL+SOI devices, the changes in $I_{ds}$-$V_{gs}$ curves after exposure to heavy ions range from zero to more than 60 % decrease in transconductance ($g_m$) (Figure 6.2 and Figure 6.3). $V_{tf}$ may be affected as well, with a maximum shift of -20 mV (Figure 6.2 and Figure 6.3). $g_m$ drop and $V_{tf}$ shift seem to be uncorrelated, since we measured devices with both $g_m$ drop and $V_{tf}$ shift (Figure 6.2a), with only $g_m$ drop (Figure 6.2b) or only $V_{tf}$ shift (Figure 6.2c). Degradation on conventional SOI is comparatively less severe with respect to sCESL+SOI: in these devices there is no change in $V_{tf}$ and $g_m$ drop is less than 45 % after irradiation. sSOI samples are the least affected, showing no $V_{tf}$ shift and $g_m$ drops below 20 %.

The dramatic decreases in $g_m$ after heavy ion strikes (Figure 6.2 and Figure 6.3) have already been observed in bulk MOSFETs [Cester04] with short or narrow channels and also in SOI belonging to the 90 nm node, and were attributed to the formation of a physically damaged region in the gate oxide [Cester05]. A similar mechanism may explain our experimental observations: radiation-induced defects in the gate oxide and/or in the isolation oxides decrease the mobility, strongly reducing the drain current, especially in devices with $L < 1$ μm.

The small $V_{tf}$ shifts appear to be uncorrelated to the $g_m$ drops (Figure 6.3), and probably feature a different origin than the transconductance reduction. We can attribute them to positive charge trapping in the BOX, rather than to degradation of the gate oxide. Experiments with protons showed that the BOX of sCESL+SOI devices is more sensitive to total-dose effects, because of a larger presence of hydrogen [Put06]. In the same way, sCESL+SOI samples could be more sensitive to the microdose effects [Oldham93] induced by heavy-ions, and therefore feature a larger $V_{tf}$ shift, as shown in Figure 6.3. Figure 6.4 schematically depicts the involved process. Also the opposite sign of the $V_{tf}$ shift observed in the majority of the tested sCESL+SOI samples compared to the other types (Figure 6.3) shows agreement between heavy-ion and proton data [Put06].

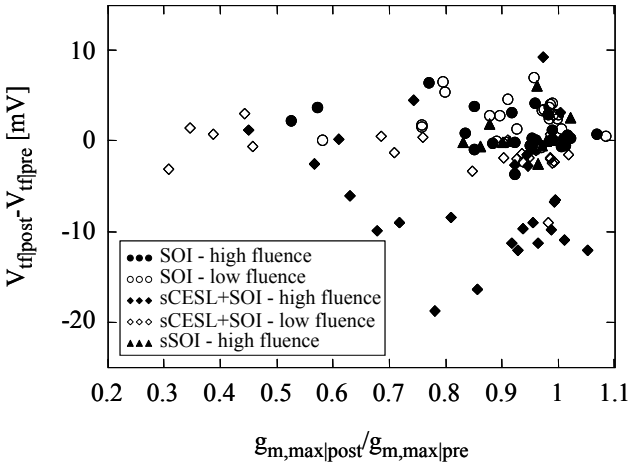



Figure 6.3: $V_{tf}$ shift as a function of $g_m$ drop after irradiation for FD SOI MOSFETs with different aspect ratio, strain-level, and irradiation fluence ($W$ = 10 µm, $g_m$ and $V_{tf}$ measured at $V_{ds}$ = 25 mV, $V_{bs}$ = 0 V).

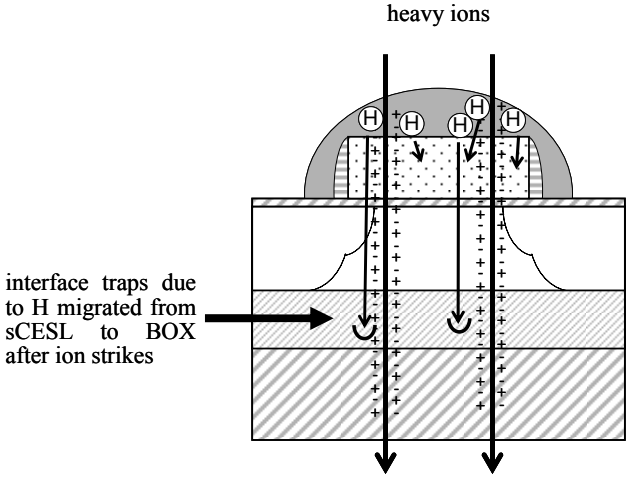



Figure 6.4: Schematic (not to scale) of enhanced hydrogen release from sCESL in FD SOI MOSFETs struck by heavy ions.

Differences between the three types of devices can be caused also by different processing: SIMOX for SOI and wafer-bonding for SOI+sCESL and sSOI, as previously reported [Schwank03]. This explains why sSOI MOSFETs are less sensitive than SOI. In SOI+sCESL the advantage granted by wafer-bonding in terms of reduced radiation sensitivity is compensated by the larger hydrogen amount, as we mentioned before.

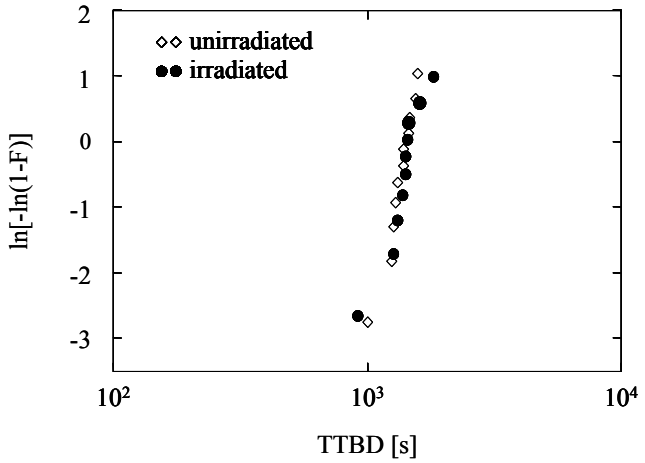



Figure 6.5: Time to breakdown for irradiated (2.5 I ions/μm$^2$) and unirradiated FD SOI MOSFETs ($W/L$ = 10 μm/10 μm) with different strain levels. The devices were stressed with a staircase voltage from 2 V to 4 V with 50-mV steps, each lasting 100 s.

## 6.4 Time to Breakdown

After irradiation, we submitted the samples with no significant $I_g$ change (max $\Delta I_g/I_{g,pre\text{-}rad} < 1$ %) and only marginal $I_d$ degradation (max $\Delta I_d/I_{d,pre\text{-}rad} < 5$ %) to electrical stresses. In particular, the time to breakdown was measured on unirradiated and irradiated devices with $W/L$ = 10 μm/10 μm struck by 250 ions on the gate area. A 20 % increase in gate current at monitor voltage was chosen as the breakdown criterion for unirradiated and irradiated devices, since they both exhibit progressive breakdown.

The results are shown in Figure 6.5: the Weibull distributions for irradiated and unirradiated samples practically overlap.

Contrary to previous experiments on devices with thicker gate oxide (both bulk [Cester03] and SOI [Cester05]), which reported a considerable TTDB reduction in devices irradiated with high-LET ions, our data indicate that no earlier breakdowns occur in these samples (Figure 6.5), even though iodine was used (LET = 59 MeV·cm$^2$/mg). The thickness of the gate oxide may play an important role. Indeed, the thinner is the oxide, the smaller the number of traps that is necessary to trigger a breakdown event [Stathis02]. So, if the irradiation creates even a handful of traps, these will show up immediately as a breakdown path in a very thin gate oxide (Figure 6.6b). On the contrary, in thicker oxides, the traps could remain "hidden" (i.e., no change at all occurs in the DC characteristics) or show small gate leakage until an electrical stress was applied (Figure 6.6a), giving rise to earlier breakdowns relative to unirradiated oxides [Cester03]. A 1.5 nm gate oxide (such as that of our devices) is so thin that it cannot hide any latent

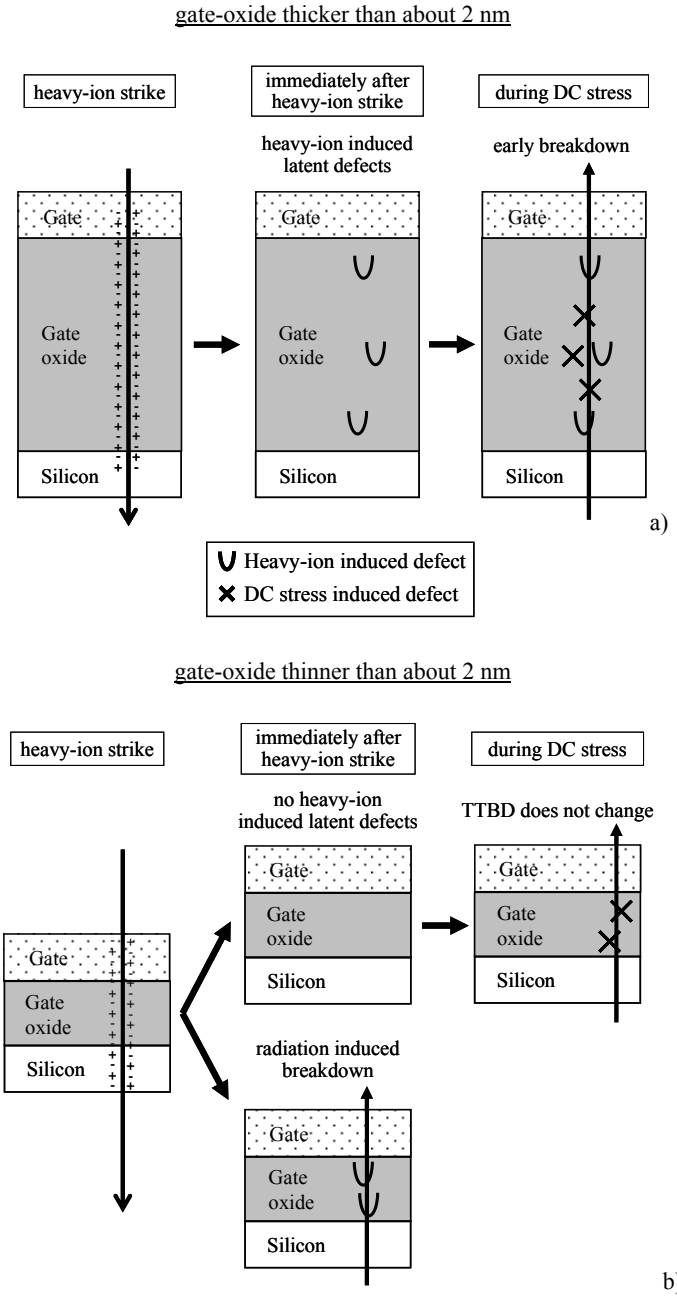



Figure 6.6: Schematic of gate oxide response to electrical stress after heavy-ion strikes: a) $t_{OX}$ > about 2 nm and b) $t_{OX}$ < about 2nm.

damage. It is very interesting to note that these transistors show progressive breakdowns [Monsieur02] as opposed to abrupt ones during electrical stresses. Progressive breakdown appears indeed in gate oxides thinner than about 2 nm.

While electrical measurements are easy to perform and give an idea about the average impact of latent damage it does not provide sufficient spatial resolution to identify its possible origin. This can be achieved by Scanning Probe techniques based on Atomic Force Microscopy (AFM) [Marinoni08] [Marinoni09] [Carvalho07]. Besides topographical information, one can also obtain electrical information, using conductive-mode AFM, directly on the ion spot [Porti05]. In this way, also the presence of ion tracks on the surface of $SiO_2$ has been investigated [Carlotti06] [Carvalho07]. In combination with HF etching, it was demonstrated that an ion track gives rise to a nanodot near the surface, below which silicon bumps at the Si-$SiO_2$ interface are found [Carlotti06]. This has been interpreted in terms of the thermal spike model for ion tracks in solid state matter. It is assumed that the local density of deposited ionization energy becomes so large that a local melting of the material occurs. This makes sense in view of the poor thermal conductivity of $SiO_2$ compared with silicon, which keeps the thermal energy confined to a narrow cylinder. Therefore, the local temperature may rise considerably above the melting temperature. In $SiO_2$, the oxygen will diffuse away, leaving behind a silicon nanodot, whenever quenching of the molten zone occurs slower than the oxygen diffusion [Carlotti06].

It can be remarked that a lower threshold oxide thickness was observed for the occurrence of the surface tracks [Carvalho07]. For thin oxides (4 and 2 nm) no such surface tracks were observed, in good agreement with the absence of accelerated wear out reported for 1.5 nm SiON, suggesting a connection between the presence of ion tracks and latent damage. This lower threshold is consistent with the thermal spike model [Carvalho07].

## 6.5 Stress-Induced Degradation in Unirradiated Devices

The degradation kinetics of these SOI devices show a complex behavior depending on the channel length and strain level, even on unirradiated devices. Figure 6.7 illustrates the evolution of $V_{tf}$ for two channel lengths (3 μm and 0.2 μm, called long and short channel in the following). Two behaviors with different degradation rates can be distinguished regardless of the transistor type and channel length: initially the $V_{tf}$ increases at about 8-9 mV/decade, afterwards at only 20 μV/decade. For a given transistor type (SOI, sSOI, sCESL+SOI) the change in the degradation rate occurs earlier (about one decade in time) for shorter channel devices. The degradation after 1 second of stress also varies considerably: short-channel devices degrade much more than corresponding long-channel ones.

The discussion begins by reviewing the degradation of unirradiated samples, and then showing the changes induced by heavy-ion strikes in the device behavior. The change in $V_{tf}$ occurring during the first phase of the CVS (Figure 6.7) can be attributed to

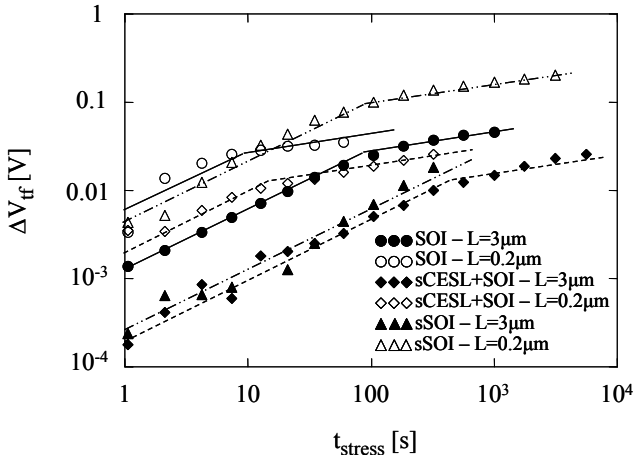



Figure 6.7: $V_{tf}$ shift as a function of stress time (constant voltage at 2.75 V) in unirradiated FD SOI MOSFETs (W/L = 10 μm/3 μm and W/L = 10 μm/0.2 μm): the degradation depends on the strain level and channel length. Typical behavior is shown for each device type.

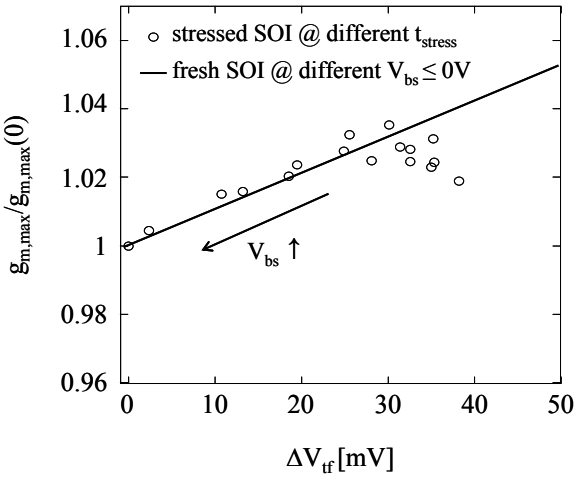



Figure 6.8: Comparison between $g_m$ variation as function of $V_{tf}$ shift at different $V_{bs} \leq 0$ V (straight line) on a fresh device and at different times during CVS at 2.75 V (circles) for the same unirradiated FD SOI MOSFETs with $W/L$ = 10 μm/0.2 μm.

negative charge build-up in the BOX (both in irradiated and unirradiated devices). It is known that applying high voltages to the front-gate oxide can result in carriers reaching the BOX and creating defects there [Zaleski95] [Ioannou05]. In fact, the modifications we observe in the subthreshold swing, $g_m$, and $V_{tf}$ in the first phase of the stresses can be reproduced by lowering $V_{bs}$ in a unirradiated, unstressed device (Figure 6.8). In other words, biasing the back gate at a given negative voltage has a similar effect on the electrical characteristics as stressing the device for a certain amount of time.

The slow-down in the $V_{tf}$ increase occurring in the second part of the stresses is accompanied by a reduction in the $g_m$, pointing to a significant accumulation of interface states in the front-gate oxide and/or in the BOX, which may reduce the channel mobility. This effect cannot be reproduced changing the bias at the back gate (Figure 6.8), suggesting it is not related to fixed charge in the BOX. It is worth remarking that not a long time elapses from the slow-down in the degradation to the breakdown of the front-gate oxide, further confirming the presence of defects also in the front-gate oxide in the last phase.

It is also interesting to note that unirradiated sCESL+SOI samples experience the smallest degradation during electrical stresses (Figure 6.7), whereas they are the most affected after irradiation (Figure 6.3). This behavior may be related to the release of H from the sCESL, which occurs after radiation, but not after electrical stress.

Short-channel devices feature a larger degradation than long-channel ones in the first seconds of stress, where BOX degradation plays the most prominent role. This behavior is possibly related to enhanced trapping/damage close to the source/drain region due for instance to process-induced damage during junction/halo implants [Ramos06] [Yasuda06] [Shickova07]

## 6.6 Stress-Induced Degradation in Irradiated Devices

Irradiation modifies this behavior, as shown in Figure 6.9 for long-channel samples struck by either 30 or 75 I ions. In the first seconds of stress (< 20-30 s, phase 'A' in Figure 6.9) no difference is noticeable between irradiated and unirradiated devices, in terms of $\Delta V_{tf,irr}(t_{stress}) - \Delta V_{tf,unirr}(t_{stress})$. Afterwards, the $\Delta V_{tf}$ in irradiated devices is larger or smaller depending on the strain-level (Phase 'B' in Figure 6.9): in SOI and sSOI, the $\Delta V_{tf}$ during CVS is decreased in heavy-ions struck devices, whereas in the sCESL+SOI the opposite behavior takes place. Finally, the difference between irradiated and unirradiated devices tends to vanish (Figure 6.9, phase 'C'). The differences affecting the $V_{tf}$ evolution are larger for the devices struck by more ions.

Short-channel devices show some differences with respect to long-channel transistors (Figure 6.10): phase 'A' is absent, $\Delta V_{tf,irr}$-$\Delta V_{tf,unirr}$ changes faster, the turnover point occurs earlier (about one-two decades earlier depending on the strain level), and the maximum $\Delta V_{tf,irr}$ - $\Delta V_{tf,unirr}$ is larger. Contrary to $V_{tf}$ (Figure 6.7), $g_m$ does not change monotonically with stress time in short-channel devices (irradiated or not), but it rather increases and then decreases with stress time. The turnover occurs at the time when the $V_{tf}$ evolution changes slope.

Figure 6.11 displays the correlation between the $g_m$ variation and the $V_{tf}$ shift during CVS for devices with $W/L$ = 10 μm/0.2 μm and featuring different strain levels and irradiated at different fluences. The $g_m$ evolution is also affected by irradiation. Heavy

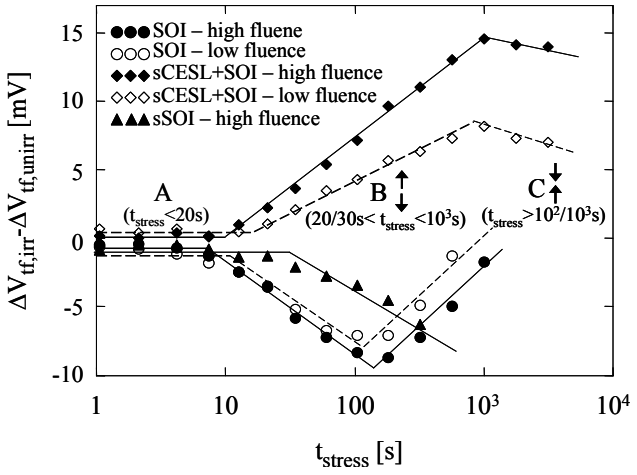



Figure 6.9: Radiation-induced alteration of the $V_{tf}$ kinetics as a function of stress time (constant voltage at 2.75 V) for irradiated FD SOI MOSFETs ($W/L$ = 10 μm/3 μm). $V_{tf}$ *vs.* $t_{stress}$ of typical irradiated devices has been subtracted from that of typical unirradiated samples.

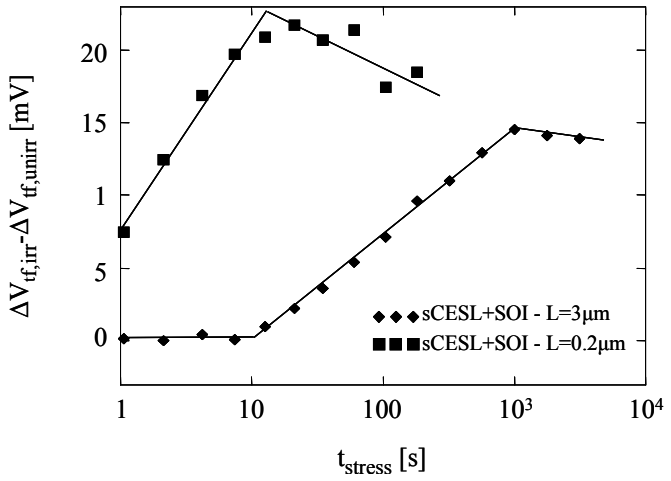



Figure 6.10: Comparison between radiation-induced alteration of $V_{tf}$ kinetics as a function of stress time for FD sCESL+SOI MOSFETs with different $L$ (3 μm and 0.2 μm). The devices were hit by 2.5 I ions/μm$^2$.

ions strikes actually improve the $g_m$ behavior during CVS both in SOI and sCESL+SOI, even though the variations are very small.

The irradiation alters the device parameter kinetics especially during the first phase of the stress, i.e., the one dominated by BOX degradation (Figure 6.9 – Figure 6.10), either modifying the charge-trapping and interface-state generation kinetics in the BOX or altering the amount of carriers which may reach the buried oxide and cause damage during electrical stress (Figure 6.12).

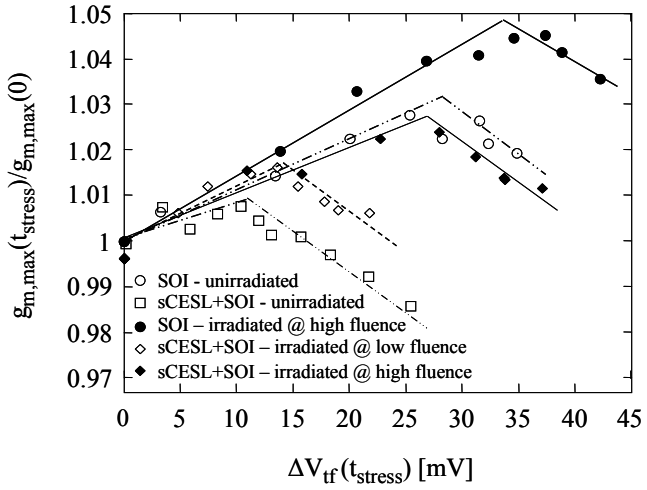



Figure 6.11: $g_m$ variation as function of $V_{tf}$ shift during constant voltage stresses at 2.75 V for irradiated (1 and 2.5 I ions/μm$^2$) and unirradiated FD SOI MOSFETs with W/L = 10 μm/0.2 μm.

The smaller increase in $V_{tf}$ in the irradiated SOI and sSOI samples as compared to the unirradiated transistors may be due to defects in the silicon body, which may act as recombination centers and prevent the carriers at the front gate from being injected in the BOX during CVS (please notice that the body is not doped). Yet, the number of defects positioned near mid-gap (E centers and/or divacancies) created by heavy-ions which may have an impact on the recombination in the silicon body is very modest. In any case, the importance of this kind of defects can be easily ascertained using X-rays instead of protons (only total dose without bulk damage).

Alternately, the same number of carriers may reach the BOX as in unirradiated oxides, but the effect can be reduced by radiation-induced changes in the BOX.

On the other hand, the larger increase in $V_{tf}$ in irradiated sCESL+SOI devices with respect to unirradiated samples during electrical stress may be ascribed to an increase in negative interface states in the BOX. This trap concentration increase may be explained by the larger presence of hydrogen in the sCESL layer [Arghavani06] [Sleeckx05]. In fact, the radiation may break or weaken the hydrogen bonds in the sCESL, releasing hydrogen into the polysilicon gate and the surrounding oxide layers. Following CVS, these hydrogen atoms may migrate through the silicon body into the BOX, creating additional interface states.

Concerning the second phase of the stress, where degradation of the gate oxide dominates the overall response, we can speculate (no experimental verification is possible since breakdown occurs first) that the gap in the degradation between irradiated and unirradiated devices tends to zero, as suggested by the rejoining curves in Figure 6.9. This would further confirm that the gate oxide is not altered by radiation, as proved by the

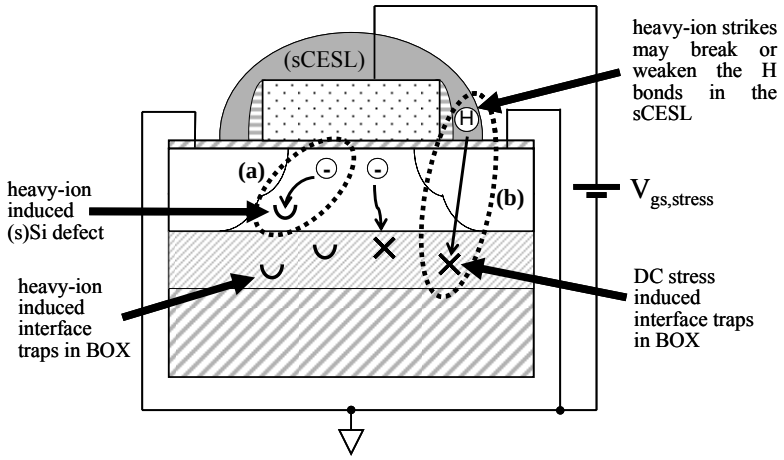



Figure 6.12: Schematic (not to scale) of proposed mechanisms which may alter the CVS response of irradiated FD SOI MOSFETs with different strain levels: (a) defects in the silicon body acting as recombination centers; (b) hydrogen in sCESL migrating through the silicon body into the BOX, creating additional interface states.

TTBD measurements shown in the previous section. In other words, when the gate oxide degradation determines the device response to electrical stress, irradiation does not alter the parameter kinetics.

We have shown that the differences between long and short channel in irradiated devices and between irradiated and unirradiated samples submitted to electrical stress are caused by the buried oxide. It is therefore expected that the radiation-induced alterations during CVS depend on the channel length, as shown in Figure 6.10. In particular the weaker areas of the BOX close to the source and drain regions may be more affected by heavy-ions, determining the larger and earlier changes in the behavior of short-channel devices.

## 6.7 Conclusions

The results of this chapter show some interesting changes in how modern devices manufactured on SOI wafers and with strain-inducing techniques respond to heavy-ion strikes (with floating device terminals) and subsequent electrical stresses: lack of early breakdown due to the very thin gate oxide, and varying impact on the long-term degradation kinetics depending on the adopted technological solutions. Even though radiation-induced changes are modest, the data suggest that permanent or semi-permanent damage from heavy-ion strikes must be constantly monitored, because of a very strong dependence on the manufacturing technology.

# Chapter 7

# Microdose Effects on FinFET Devices

Despite multigate SOI devices, such as FinFETs, have recently shown improvement in total-dose tolerance with respect to planar transistors, it is demonstrated that microdose effects are a serious concern for FinFET devices.

## 7.1 Introduction

Heavy-ion damage, including SEGR [Sexton03], RSB [Ceschia00_2], RILC [Scarpa97], microdose effects [Oldham93], and long-term reliability degradation [Choi02], may seriously limit device lifetime and reliability in space applications. The sporadic collapse of the drain current in planar MOSFETs with either narrow or short channel has also been reported several times after irradiation with heavy ions, and may challenge the reliability of advanced circuits [Cester04]. Long-term impact of irradiation has been investigated as well. Heavy-ion strikes can lead to changes in the degradation kinetics and to earlier gate-oxide breakdown [Choi02], [Cester03].

In the planar world of conventional MOSFETs, the effects of heavy-ion irradiation are usually studied at perpendicular beam incidence (or at relatively modest angles), creating defects in a (small) portion of the gate dielectrics. This is especially true using particle accelerators, where the maximum energy is reduced compared to space: grazing angle irradiation may be performed only by using very high energy ion beams available in few facilities around the world. Particles impinging at grazing angles and ion irradiation of vertical structures have been the subject of recent works [Cellere07] [Carvalho07] [Felix07], showing some surprising results. Similarly, in three-dimensional structures, as FinFET devices, the response to a heavy-ion strike may strongly depend on

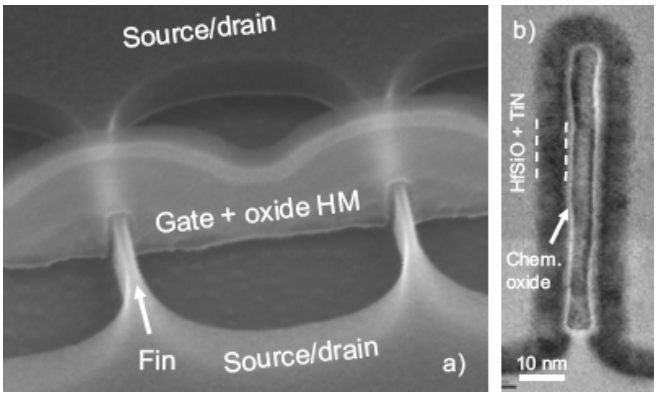



Figure 7.1: a) Top–down SEM and b) cross-sectional TEM image of a typical FinFET device with a thin MOCVD TiN metal gate on HfSiO dielectric.

the incidence angle. Furthermore, the effect, that may pass unnoticed on a large structure, can become source of concern when the device size is comparable to (if not smaller than) the ion-track size, as in the case of state-of-the-art FinFETs.

In this chapter, first the FinFET technology used in this work and the experiments are described in section 7.2. Afterwards, the short-term effects are discussed for high and very high LETs in section 7.3 and 7.4, respectively. Section 7.5 presents a new statistical approach to the modeling of the microdose induced gate-oxide degradation. In the following sections 7.6 -7.8, the angular, strain, and channel type dependence of the short-term degradation of the electrical characteristics are described. Finally, the long-term effects are discussed in section 7.9.

## 7.2 FinFET Technology and Experiments

In this section, first, the FinFET technology used for this work is described and, afterwards, the performed experiments are presented.

### *7.2.1 FinFET Technology*

We studied N- and P-channel SOI FinFETs manufactured by IMEC in a sub 32 nm CMOS process. These exploratory devices feature a high-k gate dielectric (2 nm $HfO_2$ on 1 nm interfacial $SiO_2$ = $t_{ox}$) and a metal gate (100 nm polysilicon on top of a 10 nm TiN metal). For this gate stack, the threshold voltage hysteresis is not observed in agreement with [Ribes05]. Metal gate is the preferable option over a polysilicon gate since it allows obtaining correct N- and P-MOS threshold voltages ($V_{TH}$) without using channel doping.

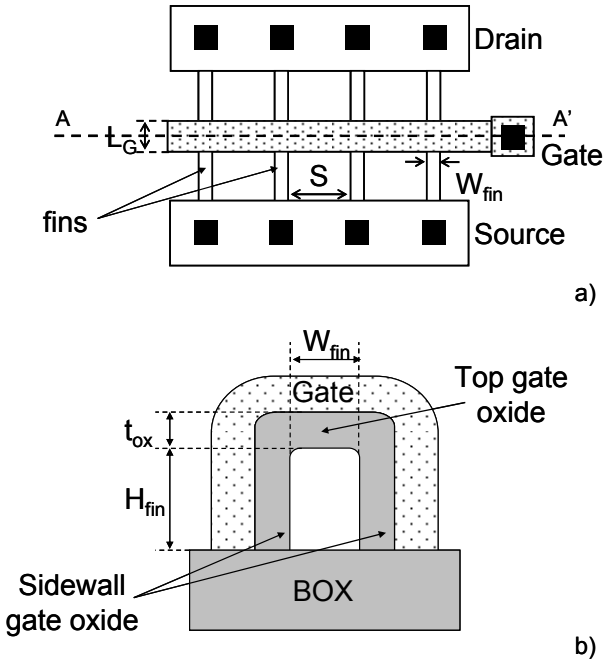



Figure 7.2: a) horizontal and b) vertical along cut-line A-A' layout view of a SOI FinFET device indicating the different geometrical parameters.

The absence of channel doping also permits the elimination of the dopant-fluctuations effects. FinFETs are more complex than conventional planar MOSFETs (Figure 7.1 and Figure 7.2). In addition to the gate length ($L_G$), we can also define the fin width ($W_{fin}$), the fin height ($H_{fin}$), the fin number ($N_{fin}$), and the fin-to-fin spacing ($S$). The measured devices have 30 nm minimal $L_G$, 18 nm minimal $W_{fin}$, and 1 ('single fin') or 30 fins in parallel ('multi fin').

Two different variants were processed:

i. non-strained FinFETs (SOI FinFETs) with 65 nm fin height ($H_{fin}$), and 145 nm Buried Oxide (BOX) thickness ($T_{BOX}$); and
ii. strained FinFETs (sSOI FinFETs) with 1.5 GPa intrinsic biaxial strain, 55 nm $H_{fin}$, and 130 nm $T_{BOX}$.

Both variants are made by wafer bonding and smart cut. Fins down to 18 nm were patterned using 193 nm optical lithography and aggressive resist and hard mask trimming. After fin patterning, the devices received a $H_2$ anneal to smoothen the sidewalls and round the corners. The devices did not receive a fin implant. After gate patterning, As/$BF_2$ extensions were implanted with a high angle and 45 nm recessed PECVD nitride spacers were formed. After the HDD implantations, a 1050° C spike anneal was given and NiSi was used as a salicide. Further details on these samples can be found in

Table 7.I: Characteristics of the heavy ions used to irradiate the FinFETs. $\theta = 0°$ corresponds to normal incidence.

| Ion | Energy [MeV] | LET [MeV·cm$^2$/mg] | Fluence [ions/cm$^2$] | Incidence angle θ [°] | # ion strikes on a single-fin FinFET with $L_G$ and $W_{fin}$ | | |
|---|---|---|---|---|---|---|---|
| | | | | | # strikes | $W_{fin}$ [nm] | $L_G$ [nm] |
| He | 4 | 0.7 | $5.1 \cdot 10^{11}$ | 0 | 3 | 18 | 30 |
| Ni | 220.7 | 28.6 | $4.12 \cdot 10^{10}$ | 0 | 1 | 18 | 135 |
| Ni | 220.7 | 28.6 | $2.06 \cdot 10^{11}$ | 0 | 1 | 18 | 30 |
| I | 247.2 | 58.8 | $1.2 \cdot 10^{11}$ | 0 | 3 | 18 | 135 |
| I | 276.9 | 60.1 | $4.12 \cdot 10^{10}$ | 0 | 1 | 18 | 135 |
| I | 276.9 | 60.1 | $7.08 \cdot 10^{9}$ | 45 | 1 | 18 | 135 |

[Collaert06]. All the devices used in this chapter are non strained unless indicated otherwise.

## *7.2.2 Experiments*

FinFETs were irradiated at different incidence angles ($\theta$) and at room temperature with heavy ions at the SIRAD facility of the Tandem Van Der Graaf accelerator at the INFN Legnaro National Laboratories, Italy [Wyss01]. Details are reported in Table 7.I. All the devices used in this chapter are irradiated at normal incidence unless indicated otherwise. Some devices were irradiated with 60-MeV protons at the Cyclone facility in Louvain-La-Neuve, Belgium, up to a fluence of $10^{12}$ p/cm$^2$, corresponding to a dose of 100 krad($SiO_2$), for comparison with the heavy-ion results. Irradiation was done at the chip level with floating device terminals. Even if this is not the worst-case condition, floating irradiations may give interesting results (for instance about switched-off devices hit by heavy ions) and do not require bonding, which is often harmful or even catastrophic in these devices, due to the lack of ESD protections [Duvvary08_3]. Reference unirradiated parts have been kept alongside the irradiated ones and exhibit repeatable characteristics. Before and after irradiation and during electrical stresses, on each sample we measured the gate current versus the gate voltage ($I_G$-$V_G$), the drain current (at $V_{DS}$ = 25 mV) versus the gate voltage ($I_{DS}$-$V_{GS}$) at different back-gate voltages ($V_{BS}$), the drain current versus the drain voltage ($I_{DS}$-$V_{DS}$) at different gate voltages, and the drain current versus the back-gate voltage ($I_{DS}$-$V_{BS}$) at $V_{GS}$ = 0 V.

To study the Time-Dependent Dielectric Breakdown (TDDB) and the degradation kinetics, we submitted irradiated and unirradiated devices to Constant Voltage Stress (CVS) at $V_{GS,stress}$ = 3 V and $V_{DS} = V_{BS}$ = 0 V on single-fin SOI FinFETs with $L_G$ = 135 nm and $W_{fin}$ = 18 nm, 108 nm, and 333 nm. The $V_{GS}$ voltage value for the CVS tests

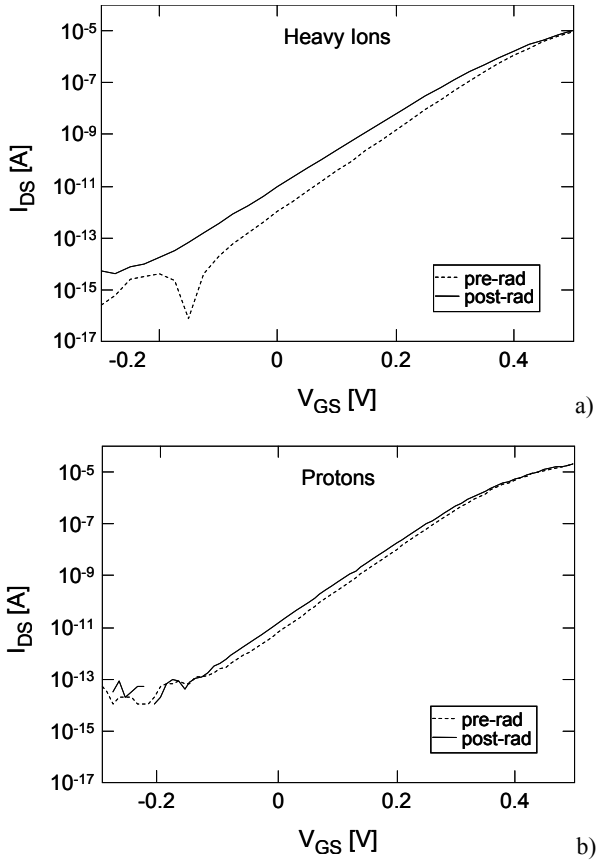



Figure 7.3: $I_{DS}$-$V_{GS}$ ($V_{DS}$ = 25 mV and $V_{BS}$ = 0 V) characteristics in semi-logarithmic scale before and after a) heavy-ion exposure ($4.12 \cdot 10^{10}$ Ni ions/cm$^2$, corresponding to one ion strike per fin) and b) protons exposure (100 krad($SiO_2$)) for two SOI FinFETs with $W_{fin}$ x $N_{fin}$ =18 nm x 30 and $L_G$ = 135 nm. The samples show a decrease in the threshold voltage.

was selected in order to study the degradation mechanisms and the oxide breakdown in a convenient time frame.

We tested more than 400 devices for this work.

## 7.3 Short-Term Effects Induced by Ions with High LET

No significant changes were observed immediately after irradiation in FinFET devices exposed to ions with low LET (0.7 MeV·cm$^2$/mg). On the contrary, for high LET (28.6 MeV·cm$^2$/mg), the post-radiation characteristics show a broad range of variations, which are investigated in this section.

We begin our analysis with the post-radiation characteristics of the devices irradiated with Ni ions in which the gate current ($I_G$) measured at $V_{GS}$ = 1.2 V did not

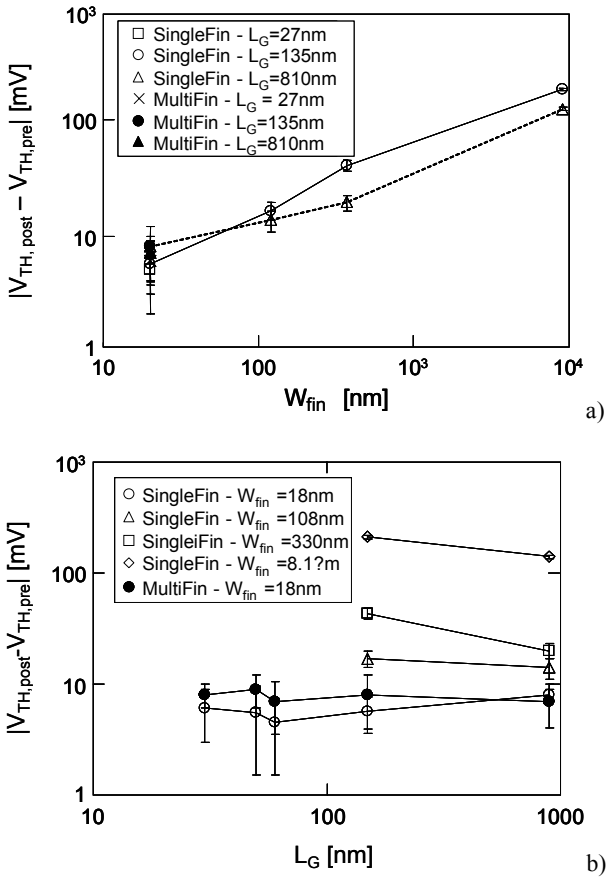



Figure 7.4: Absolute value of the average $V_{TH}$ ($V_{DS}$ = 25 mV and $V_{BS}$ = 0 V) variation as a function of a) $W_{fin}$ for different $L_G$ and b) $L_G$ for different $W_{fin}$ after heavy-ion exposure ($2.06 \cdot 10^{11}$ Ni ions/cm$^2$ for devices with $W_{fin}$ = 18 nm and 27 nm ≤ $L_G$ ≤ 54 nm and $4.12 \cdot 10^{10}$ Ni ions/cm$^2$ for transistors with $W_{fin} \geq 18$ nm and $L_G \geq 135$ nm) for SOI FinFETs. A geometry-dependent decrease in $V_{TH}$ occurs in all samples.

significatively change ($\Delta I_G$ < 100 pA). The smallest among these devices was hit by a single heavy ion. The degradation is remarkably similar to that induced by protons (Figure 7.3). From a quantitative point of view, $V_{TH}$ decreases by 14 mV and the subthreshold swing increases by 10 mV/dec in a multi-fin transistor with $W_{fin}$ = 18 nm (in the following 'narrow fin') and $L_G$ = 135 nm hit by 30 heavy ions (1 ion strike per fin), whose equivalent dose is 10.9 Mrad($SiO_2$). On the other hand, a sample with the same geometry irradiated with protons (100 krad($SiO_2$)) experiences a reduction in $V_{TH}$ of 6 mV while the subthreshold swing is unaltered.

The degradation observed in the SOI FinFETs irradiated with Ni ions is remarkably similar to that induced by protons, suggesting a microdose effect [Oldham93] [Gerardin06] in the BOX. Moreover, the electrical characteristics measured after irradiation can be emulated by positively biasing the back-gate terminal. Remarkably,

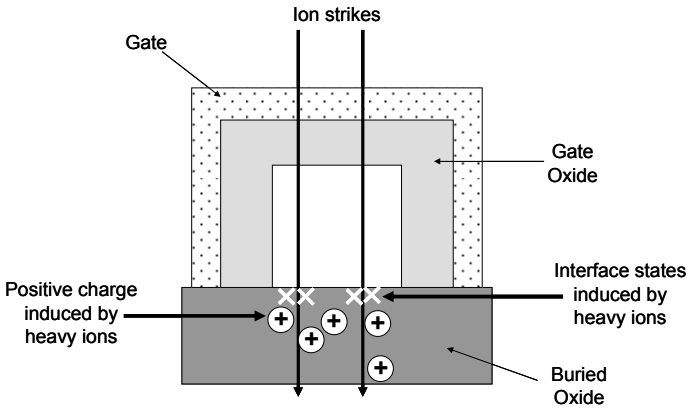



Figure 7.5: Schematic (not to scale) of interface states and positive charge in the buried oxide for SOI FinFETs struck by Ni ions.

even though the energy deposition is more localized (interface states density in the Si/BOX and/or in the Si/gate-oxide interfaces and charge trapping in the BOX are less uniform than with protons) and the charge yield much lower in the case of the heavy-ions, the effects are qualitatively comparable.

Some devices are more affected than others depending on the device geometry (Figure 7.4), however all the samples experience a decrease in $V_{TH}$ after irradiation. Concerning the dependence on the fin width, the sensitivity to heavy-ion strikes increases with increasing $W_{fin}$. In fact, in single-fin transistors $V_{TH}$ shift is some mV's for narrow fin width, while it is some tens of mV's for $W_{fin}$ = 108 nm, and increases up to some hundreds of mV for $W_{fin}$ = 8.9 µm. Multi-fin SOI FinFETs show a $V_{TH}$ shift similar to single-fin devices with the same $W_{fin}$ and $L_G$. Concerning the dependence on the gate length, both single and multi-fin narrow transistors do not show a dependence on the gate length. On the contrary, single-fin devices with $W_{fin} \geq 108$ nm exhibit an increase in $V_{TH}$ shift with decreasing gate length.

Our heavy-ion data are in agreement with total-dose results in non-planar SOI devices, which show a decrease in $V_{TH}$ due to positive charge trapping in the buried oxide (Figure 7.5), which in turn alters the potential of the front gate through capacitive coupling, and an enhancement of these effects with increasing fin width [Gaillardin06_1], [Gaillardin06_2] [Colinge06] [Wu06] [Put07]. In fact, electrostatic coupling effects in non-planar devices are strongly geometry dependent [Frei04] [Daugé04] [Ritzenthaler06]. For a transistor with $W_{fin} >> H_{fin}$, the electrostatic behavior is dominated by the front and back gates. The control of the lateral gates on the potential in the silicon body and BOX is relatively weak, similarly to a planar SOI transistor. When the fin width becomes comparable to fin height, the fringing field induced by the lateral gates penetrates in the

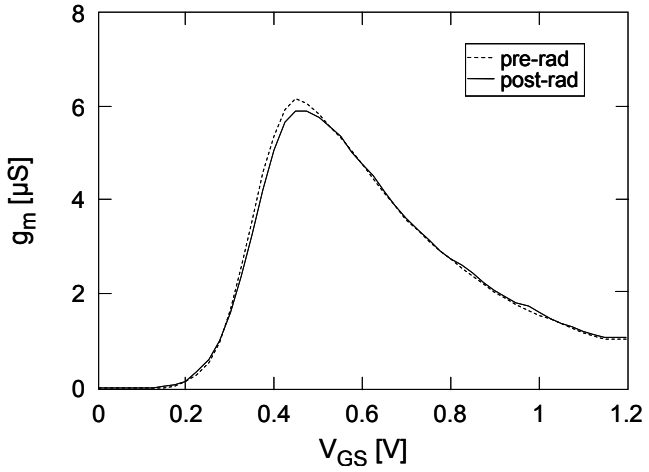



Figure 7.6: $g_m$-$V_{GS}$ ($V_{DS}$ = 25 mV and $V_{BS}$ = 0 V) characteristics before and after heavy-ion exposure ($4.12 \cdot 10^{10}$ Ni ions/cm$^2$, corresponding to one ion strike on the device) for single-fin SOI FinFET with $W_{fin}$ = 18 nm and $L_G$ = 135 nm. The transconductance decreases after irradiation.

buried oxide and at the silicon-fin/BOX interface [Frei04] [Daugé04] [Ritzenthaler06], causing the coupling between the front and back interfaces to be greatly attenuated. For this reason narrow-fin samples are less sensitive to radiation than wide-fin ($W_{fin}$ > 108 nm) devices (Figure 7.4a).

The increase in sensitivity to heavy-ion strikes with decreasing gate length observed in single-fin devices with $W_{fin} \geq$ 108 nm (Figure 7.4b) is caused by the back-channel threshold voltage roll-off. This short channel effect is more prominent because the transistors did not receive a halo-implant [Put07]. Prior to irradiation, the threshold voltage of the back channel is 7 V for samples with $L_G$ = 810 nm and only 4.5 V for the ones with $L_G$ = 135 nm. The lack of a clear dependence on the gate length observed in narrow-fin SOI FinFETs is due to the fact that the coupling between the front and back interfaces is greatly attenuated for such fin width.

The transconductance ($g_m$) after irradiation shows a small decrease up to 5 % in the case of narrow single-fin SOI FinFETs (Figure 7.6). The reduction in $g_m$ is due the increase in the interface state density, possibly located at the silicon body/BOX interface.

## 7.4 Short-Term Effects Induced by Ions with Very-High LET

An interesting difference between the DC characteristics before and after irradiation appears when the samples are hit by multiple ions (fluence = $1.2 \cdot 10^{11}$ I ions/cm$^2$) with very high LET (58.8 MeV·cm$^2$/mg). Breakdown of the gate oxide (GOX) was the most

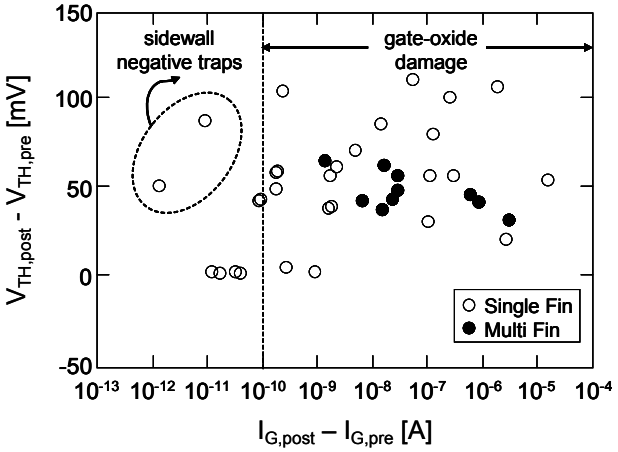



Figure 7.7: $V_{TH}$ ($V_{DS}$ = 25 mV and $V_{BS}$ = 0 V) variation as a function of $I_G$ variation ($V_{GS}$ = 1.2 V and $V_{DS}$ = $V_{BS}$ = 0 V) after heavy-ion exposure ($1.2 \cdot 10^{11}$ I ions/cm$^2$) for SOI FinFET devices with different aspect ratio. The gate-oxide breakdown and a consequent increase in $V_{TH}$ occur in most of the samples. On the contrary, some devices with $W_{fin} \leq 108$ nm experience an increase in $V_{TH}$ without corresponding increase in $I_G$.

common failure. Finally, effects which may be attributed to heavy-ions traversing the vertical gate oxide were observed in some cases at the highest tested LET.

### *7.4.1 Breakdown Effects Induced by Heavy Ions*

To investigate the radiation damage dependence on the LET, some SOI FinFETs were exposed to I ions with a fluence such that a narrow single-fin device with $L_G$ = 135 nm was hit (on average) by 3 ions. Figure 7.7 shows the $V_{TH}$ shift as a function of the maximum gate current ($I_G$) variation measured at $V_{GS}$ = 1.2 V.

Three different types of effects can be distinguished:

a) $I_G$ does not significatively change after irradiation ($\Delta I_G$ < 100 pA) and $V_{TH}$ shift is modest (some mV's) and negative;
b) $I_G$ exhibits a moderate or large increase ($\Delta I_G$ > 100 pA) and $V_{TH}$ shift is positive (as shown in Figure 7.8) and ranges between 10 mV and 100 mV;
c) $I_G$ does not significatively change but $V_{TH}$ shift is positive and larger than 50 mV.

Concerning case a), the data are in agreement with the ones observed for transistors irradiated with Ni. Microdose effects similar to those observed with Ni, are still visible in some devices hit by I ions (Figure 7.7), which feature a small negative front-gate threshold voltage shift (few mV's) and practically no change in the gate leakage current.

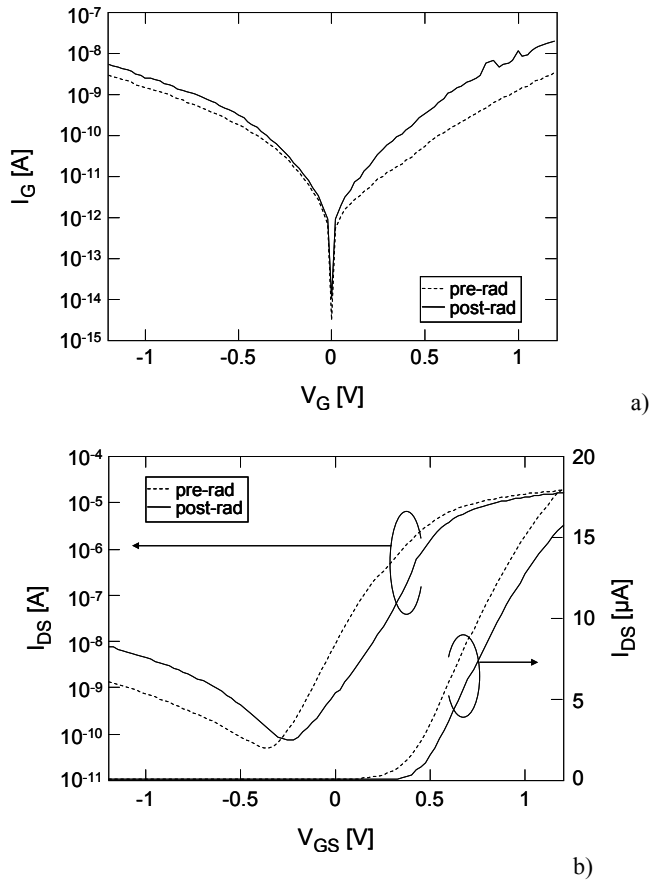



Figure 7.8: a) $I_G$-$V_{GS}$ ($V_{DS}$ = $V_{BS}$ = 0 V) and b) $I_{DS}$-$V_{DS}$ in linear and semi-logarithmic scale ($V_{DS}$ = 25 mV and $V_{BS}$ = 0 V) characteristics before and after heavy-ion exposure ($1.2 \cdot 10^{11}$ I ions/cm$^2$) for a SOI FinFET device with $W_{fin}$ x $N_{fin}$ = 330 nm x 1 and $L_G$ = 135 nm. The sample experiences a soft gate-oxide breakdown and an increase in $V_{TH}$.

Case b) is the most frequent, although the irradiation was done at the chip level with floating device terminals. More than 85 % of the irradiated samples exhibit a soft gate-oxide breakdown, regardless of the device geometry.

Gate-oxide breakdown is the most common phenomenon (Figure 7.7 and Figure 7.8). This indicates that Radiation-Induced Soft Breakdown (RSB) [Ceschia00_2], which is caused by the formation of a cluster of traps in the gate oxide (Figure 7.9), may have a non-marginal impact on the reliability of decananometer multigate devices. This is quite remarkable, given the results obtained on large capacitors during Single Event Gate Rupture (SEGR) tests [Massengill01], in which the critical breakdown voltage for gate oxide rupture was shown to be larger than the operating voltage, even for high-k dielectrics, and therefore not a serious threat for these oxide layers in harsh radiation environments. It must be remarked that a modest increase in the gate leakage current

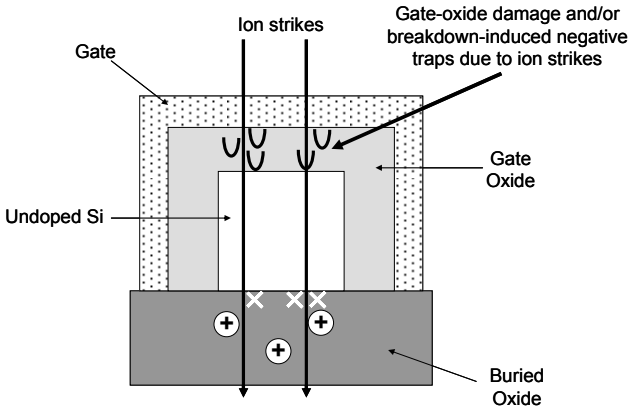



Figure 7.9: Schematic (not to scale) of gate-oxide traps, responsible of the gate-oxide breakdown, and breakdown-induced negative traps for SOI FinFETs struck by heavy ions with largest LET.

(some hundreds of pA's) may induce a non-marginal variation of the DC electrical characteristics in our small geometry devices, but would be hardly visible in a large planar MOS capacitor such as those used in [Ribes05]. Moreover, since the irradiation was done not with the worst-case bias, a more dramatic scenario can occur when a triple-gate SOI FET biased at the operating voltage ($V_{DD}$ = 1.2 V) is hit by a heavy ion with high LET, due to the larger probability of gate-oxide damage (also at lower LET), and consequent increase in the magnitude of the gate-oxide breakdown itself [Ceschia00_2].

The increase in $V_{TH}$ induced by the gate-oxide breakdown is due to the contribution of the following facts:

1) decrease in the effective gate voltage, because of the increased voltage drop in the polysilicon area, due to the breakdown gate current. However, this can account only for small $V_{TH}$ shift (some mV's);
2) reduction of carrier (electrons) density flowing in the channel, due to alteration in the channel potential caused by the breakdown path;
3) reduction of carrier density due to the coulomb effect of the charged breakdown defects [Scarpa97]. The presence of Breakdown-Induced Negative Charge (BINC) in the gate oxide after soft breakdown has been reported after electrical stresses and direct Atomic Force Microscope (AFM) measurements, that estimate a typical negative charge density of $\sim 2 \cdot 10^{12}$ e/cm$^2$ for increases in $I_G$ in the order of some hundreds of pA [Pompl99] [Porti02].

Finally, case c) displays neither the behavior associated to microdose effects in the buried oxide, nor breakdown of the gate oxide, and will be illustrated in the next section.

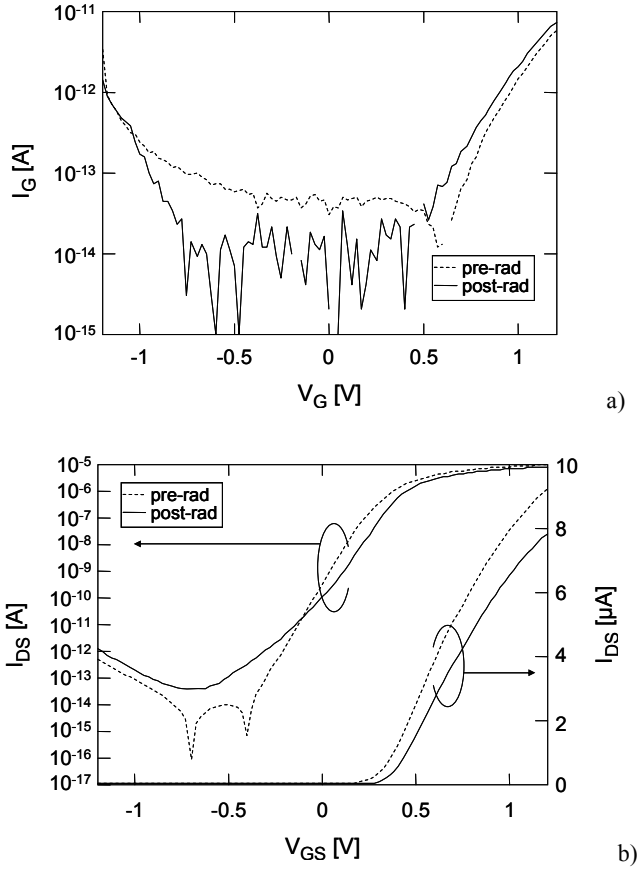



Figure 7.10: a) $I_G$-$V_{GS}$ ($V_{DS}$ = $V_{BS}$ = 0 V) and b) $I_{DS}$-$V_{DS}$ in linear and semi-logarithmic scale ($V_{DS}$ = 25 mV and $V_{BS}$ = 0 V) characteristics before and after heavy-ion exposure ($1.2 \cdot 10^{11}$ I ions/cm$^2$) for a SOI FinFET device with $W_{fin}/L_G$ = 108 nm/135 nm. The sample experiences an increase in $V_{TH}$, without showing any gate-oxide damage.

## *7.4.2 Sidewall Effects Induced by Heavy Ions*

Some SOI FinFETs with fin width $W_{fin} \leq 108$ nm do not show significant changes in $I_G$ ($\Delta I_G$ < 100 pA), while experiencing an increase in the front-gate threshold voltage (Figure 7.7 and Figure 7.10). This behavior depends on the fin width, since narrower fin devices experience a larger $V_{TH}$ shift than the ones with $W_{fin}$ = 108 nm. In addition, this phenomenon is detected only in transistors in which the fin width is smaller or comparable to the fin height. Since neither gate-oxide breakdown nor charge trapping in the buried oxide are responsible, the $V_{TH}$ increase can be the result of radiation-induced generation of interface traps in the gate oxide.

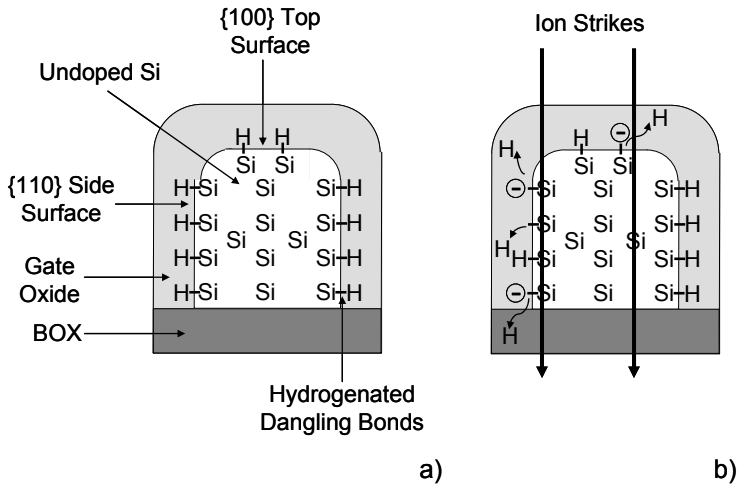



Figure 7.11: Schematic illustrations of active silicon with {100} top surface and {110} side surface: a) hydrogen passivated before irradiation and b) during heavy-ion strikes. {110} side surface has more dangling bonds than {100} top surface. Passivated dangling bonds can become electrically active defects due to an ion strike, especially if this occurs on one of the {110} side surfaces.

A very interesting observation is that multigate transistors may have different passivated interface trap density at the top and lateral gates due to different lattice orientations [Sze01]. The {110} side surfaces originally have more dangling bonds than the {100} top surface. Passivated dangling bonds can become electrically active defects due to an ion strike, especially if this occurs on one of the {110} side surfaces (Figure 7.11), resulting in a large threshold voltage shift in the side channels, as already reported for Negative Bias Temperature Instability (NBTI) stresses [Choi04] [Maeda04] [Groeseneken08_1]. This interpretation may also explains why this phenomenon is observed occasionally in our experiments: heavy ions strikes must involve the sidewall gate oxide, whose cross section for a normal impinging particle is very low (approximately the oxide thickness times the channel length), to cause significant alterations of the device characteristics. It requires a very high-LET particle as well, since it was not observed in SOI FinFETs exposed to Ni ions. This phenomenon is possibly the first evidence of radiation effects related to the verticality of the multigate transistors.

## 7.5 Statistical Modeling of the Gate-Oxide Degradation

In this section, we will discuss the experimental results obtained in multi-gate FinFETs with high-k gate oxide irradiated with heavy ions and will develop new statistical models to describe the heavy-ion induced degradation in such devices. The

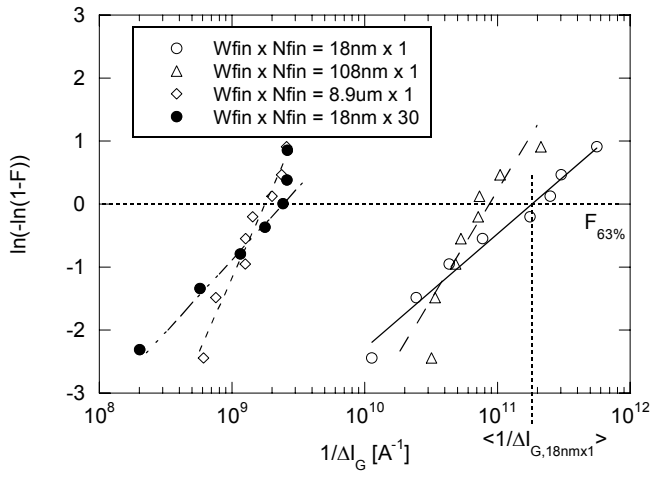



Figure 7.12: Weibull distribution of heavy-ions induced gate leakage current (at $V_{GS}$ = 1.2 V and $V_{DS} = V_{BS} = 0$ V) in NMOS FinFETs with $H_{fin}$ = 65 nm, $L_G$ = 810 nm and different $W_{fin}$ x $N_{fin}$ exposed to heavy ions ($4.12 \cdot 10^{10}$ I ions/cm$^2$ with normal incidence). The fitting lines are not from the Poisson area scaling fit.

model is based on the reliability distribution functions commonly used to estimate the Time-Dependent Dielectric Breakdown and the charge to breakdown for accelerated lifetime tests [Degraeve98] [Suñé01] [Ohring98] [Joyce89] [Cain02].

## *7.5.1 Experimental Results*

Heavy ions with very high LET can produce different permanent effects on MOSFETs in general, and FinFETs in particular, from increasing the gate leakage current ($I_G$) to changing the front- and back-gate threshold voltage (see previous section).

Interestingly enough, FinFETs irradiated at the same nominal conditions exhibit large variations in their response. Figure 7.12, for instance, shows a spread in the gate leakage current increase of almost two orders of magnitude in devices irradiated in the same conditions. Notice that the spread in gate leakage current before irradiation is less than 1 pA, which is at least an order of magnitude lower compared to the increase in gate leakage current induced by heavy-ion strikes. This increase in $I_G$ is due to the radiation induced formation of defects, which act as stepping stones for the carriers tunneling through the oxide (Trap Assisted Tunneling (TAT) [Ceschia98] [Alers98].

To better elucidate the statistical properties of the heavy-ion induced damage, Figure 7.12 shows the Weibull distribution of the cumulative probability ($F$) of the reciprocal of $I_G$ variation ($1/\Delta I_G$), measured at $V_{GS}$ = 1.2 V with the other terminals grounded for NMOS FinFETs with different $W_{fin}$ and $N_{fin}$, $H_{fin}$ = 65 nm, and $L_G$ = 810 nm irradiated at normal incidence.

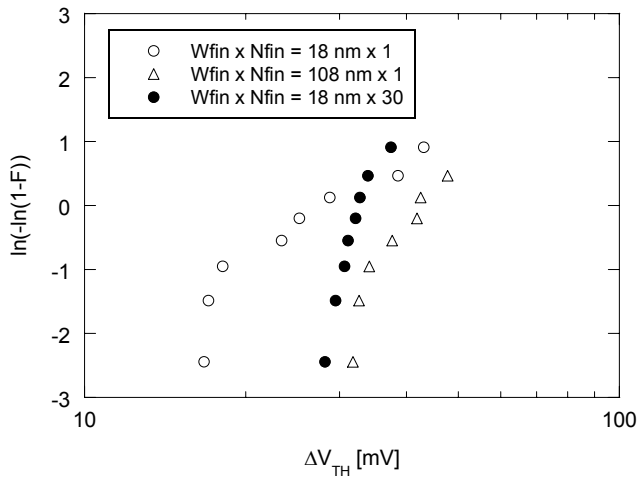



Figure 7.13: Weibull distribution of heavy-ions induced $V_{TH}$ shift ($V_{DS}$ = 25 mV and $V_{BS}$ = 0 V) in NMOS FinFETs with $H_{fin}$ = 65 nm, $L_G$ = 810 nm and different $W_{fin}$ x $N_{fin}$ exposed to heavy ions ($4.12 \cdot 10^{10}$ I ions/cm$^2$ with normal incidence). Similar results are obtained also using the LogNormal distribution.

Similarly to TDDB measurements, where the time to breakdown is inversely proportional to the critical trap density leading to the breakdown, in this circumstance $1/\Delta I_G$ was chosen as it is related to defect generation in the gate oxide induced by the radiation. For each $W_{fin}$ x $N_{fin}$, the cumulative probability follows (in first approximation) a Weibull distribution. Similar considerations can also be made for the front-gate threshold voltage ($V_{TH}$) shift (Figure 7.13). In TDDB measurements, the device area plays a fundamental role: the larger the device, the earlier the breakdown, because of the larger probability of locally reaching the defect density necessary to trigger the breakdown [Degraeve98] [Stathis99] [Stathis01]. In detail, the Poisson area scaling is valid for the average dielectric lifetime <TDDB>:

$$< TDDB(A_1) > = < TDDB(A_2) > \left( \frac{A_2}{A_1} \right)^{1/\beta} \tag{7.1}$$

where $A_1$ and $A_2$ are two different areas of the oxide films and $\beta$ is the shape parameter of the Weibull distribution. This is based on the assumption that the defect generation is uniform throughout the device area. The same thing does not happen with our radiation induced gate leakage current (see for instance Figure 7.12), where cumulative plots of devices with different areas overlap each other. A more refined analysis of the area scaling effect [Degraeve98] is shown in Figure 7.14. $1/\Delta I_G$ data from all areas are analyzed together using the Poisson area scaling for the reciprocal of the average $\Delta I_G$ ($1/<\Delta I_G>$). Similar to the Back-End Of Line (BEOL) dielectric reliability [Li05], the fit

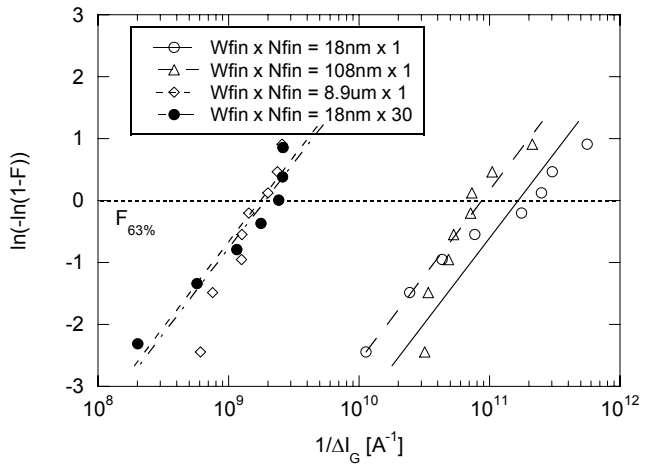



Figure 7.14: Weibull distribution of heavy-ions induced gate leakage current (at $V_{GS}$ = 1.2 V and $V_{DS} = V_{BS} = 0$ V) in NMOS FinFETs with $H_{fin}$ = 65 nm, $L_G$ = 810 nm and different $W_{fin}$ x $N_{fin}$ exposed to heavy ions ($4.12 \cdot 10^{10}$ I ions/cm$^2$ with normal incidence). The fitting lines are from the Poisson area scaling fit.

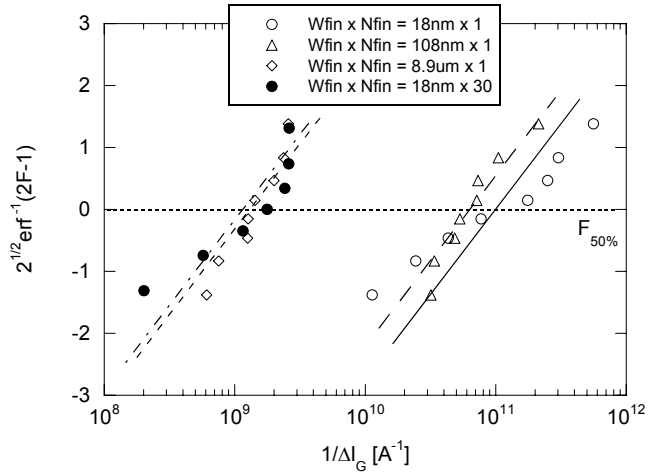



Figure 7.15: LogNormal distribution of heavy-ions induced gate leakage current (at $V_{GS}$ = 1.2 V and $V_{DS} = V_{BS} = 0$ V) in NMOS FinFETs with $H_{fin}$ = 65 nm, $L_G$ = 810 nm and different $W_{fin}$ x $N_{fin}$ exposed to heavy ions ($4.12 \cdot 10^{10}$ I ions/cm$^2$ with normal incidence). The fitting lines are from the Poisson area scaling fit.

result is not acceptable: the model given by the Poisson area scaling imposes a Weibull slope $\beta = 1$ (Figure 7.14). It is too low for $W_{fin} \geq 108$ nm and too large for $W_{fin} = 18$ nm, which demonstrates that there is some inconsistency between Poisson area scaling and our real case. On one hand, the underlying Weibull variance on the $ln(1/\Delta I_G)$ scale is at least to a large extent hidden (if not completely obliterated) by extra variance components that are LogNormally distributed and do not scale with area. On the other hand,

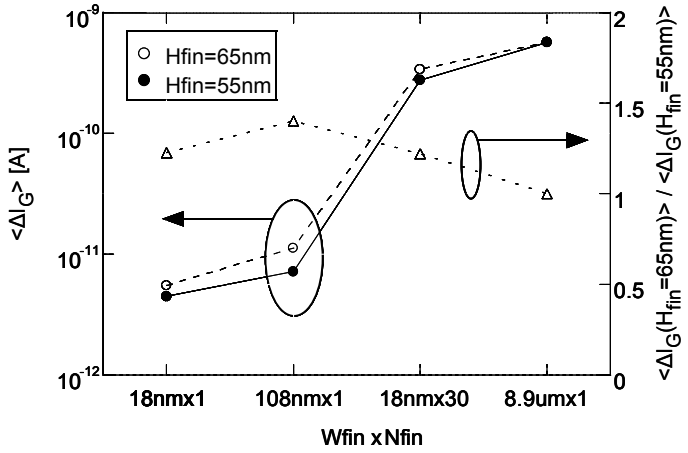



Figure 7.16: Average $\Delta I_G$ ($<\Delta I_G>$) (at $V_{GS}$ = 1.2 V and $V_{DS}$ = $V_{BS}$ = 0 V) for two different $H_{fin}$ and respective ratio as a function of $W_{fin}$ x $N_{fin}$ for NMOS SOI FinFETs with $L_G$ = 810 nm exposed to heavy ions ($4.12 \cdot 10^{10}$ I ions/cm$^2$ with normal incidence).

straightforward fits of LogNormal distributions (Figure 7.15) are also impossible, since they are fundamentally inconsistent with Poisson area scaling.

There are several possible reasons why Poisson area scaling is not respected by our radiation data:

1) At normal incidence, heavy-ion strikes in the top gate oxide travel along the oxide thickness, whereas strikes in the sidewall gate oxide travel along the gate oxide height, hence defect generation may be different in the two areas.
2) Multiple ion hits (i.e. strikes whose effects are overlapping) do not scale linearly with the area.

Concerning the first point, an ion traversing the vertical sidewall gate oxide all along its length can lead to a larger number of defect generation as compared to an ion crossing only the top gate oxide, similar to vertical power MOSFETs [Felix07]. To further highlight the role of the sidewall gate oxides on the increase in $I_G$, $<\Delta I_G>$ (Figure 7.12) for FinFETs with $H_{fin}$ = 65 nm and 55 nm were compared (Figure 7.16). For single-fin devices with $W_{fin}$ = 8.9 μm, which are in essence planar MOSFETs, $<\Delta I_G>$ is the same regardless of $H_{fin}$. On the contrary, for $W_{fin} \leq$ 108 nm FinFETs with $H_{fin}$ = 65 nm exhibit a $<\Delta I_G>$ about 1.2 – 1.3 times, almost equal to the ratio between the two fin heights, larger than the one with $H_{fin}$ = 55 nm.

Multiple ion hits were evaluated as a function of the radius of the damaged region ($r_{damage}$) in the gate oxide. Based on the model proposed by Cester et al. for nanocrystal memories [Cester07], we calculated the probability $P(h)$ that only the top gate oxide or

both top and sidewall gate oxides are hit by $h$ ($\geq 0$) ions close to the same damaged region.

We assume that:

i) The ion strikes are uniformly distributed all over the top gate oxide of the device.

ii) The top gate oxide can be divided in $N$ "cells" of area $\sigma_{top} = \pi\, r_{damage}^2$ each one.

iii) The total number of ions hitting the $N$ "cells" of top gate oxide is $M$. We assume also that each ion hits one and only one fin. This is a reasonable hypothesis as the fin-to-fin spacing is larger than 200 nm. $M$ includes only the ions that actually hit the top gate oxide, ignoring the hits occurring either between two adjacent fins or over the source/drain contacts.

iv) The ion-to-ion LET variability is negligible.

v) $r_{damage}$ is constant over the top gate oxide and along the sidewall gate oxide.

Based on such hypothesis, the probability $P_{top}$ that $h$ heavy-ion hits occurs close to the same top gate-oxide damaged area is given by the binomial distribution law:

$$P_{top}(h)=\begin{cases}\left(\frac{1}{N}\right)^{M}(N\text{-}1)^{M-h}\frac{M!}{h!(M\text{-}h)!} & if\ h\leq M\\ 0 & if\ h>M\end{cases}. \tag{7.2}$$

Of course, $P_{top}(h) = 0$ for $h > M$ because the maximum number of multiple ion hits cannot be larger than the total number of ion hits. The total number $N$ of top gate-oxide "cells" reported in (7.2) is given by:

$$N=round\left[\frac{(W_{fin}+2t_{ox})N_{fin}L_g}{\sigma_{top}}\right] \tag{7.3}$$

where the function *round*(x) rounds the element x to the nearest integer.

Since we are considering heavy-ion irradiation at normal incidence, the probability $P_{sidewall}$ that $h$ heavy-ion hits occur close to the same sidewall gate-oxide damaged area depends on $P_{top}(h)$ and is given by:

$$P_{sidewall}(h)=\begin{cases}P_{top}(h)\frac{2r_{damage}}{W_{fin}+2t_{ox}} & if\ r_{damage}<\frac{W_{fin}+2t_{ox}}{2}\\ P_{top}(h) & if\ r_{damage}\geq\frac{W_{fin}+2t_{ox}}{2}\end{cases} \tag{7.4}$$

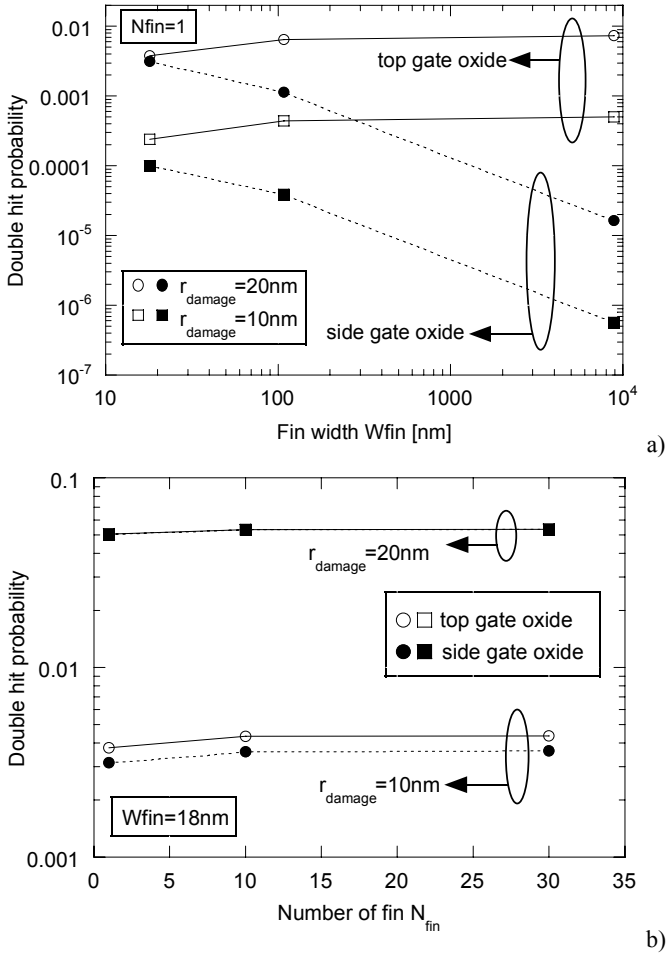



Figure 7.17: Probability that a double hit close to the same damaged region occurs on the top or along the side gate oxides of a FinFET with $L_G$ = 810 nm exposed to heavy ions ($4.12 \cdot 10^{10}$ I ions/cm$^2$ with normal incidence) as function of a) $W_{fin}$ and b) $N_{fin}$. The probabilities are calculated for two different damage radius ($r_{damage}$ = 10 nm or 20 nm).

Here, if the radius of the damaged area is equal to or larger than half of the top gate-oxide width, $P_{sidewall}$ is equal to $P_{top}$ because of (both) the sidewall gate oxides are surely struck by a heavy ion. On the contrary, $P_{sidewall}$ has to take into account the probability that an ion hits only one sidewall gate oxide ($2 \cdot r_{damage} / (W_{fin} + 2 \cdot t_{ox})$) if $r_{damage}$ is smaller than half of the top gate-oxide width.

Figure 7.17 shows the double-ion-hits probability for the top and sidewall gate oxides ($P_{top}(h = 2)$ and $P_{sidewall}(h = 2)$, respectively) as a function of $W_{fin}$ and $N_{fin}$ for two different $r_{damage}$ (10 nm and 20 nm). Obviously, the multi-hit probability is larger for the larger $r_{damage}$. When $W_{fin}$ is decreased, $P_{top}(h=2)$ slightly decreases because of an increase in $P_{top}(h \geq 3)$. On the other hand, $P_{sidewall}(h = 2)$ strongly increases with decreasing $W_{fin}$, as

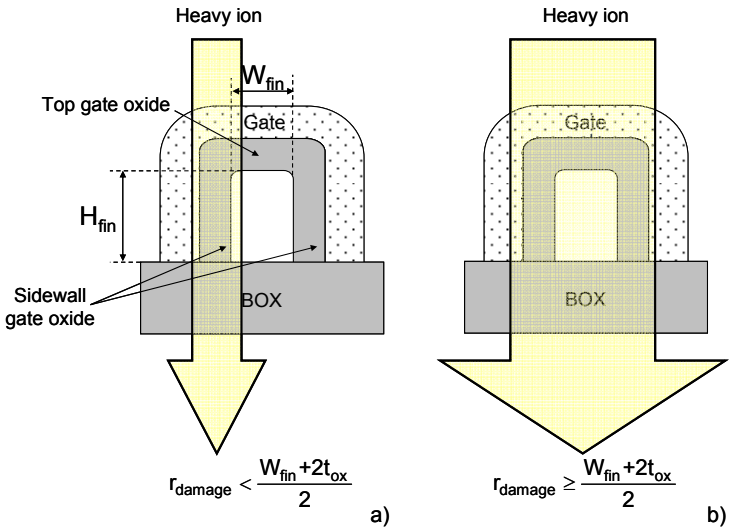



Figure 7.18: Schematic (not to scale) of gate-oxide area damaged by an heavy-ion strikes in the of a) the radius of the damaged region is smaller than the top gate-oxide width, and b) the radius of the damaged area is equal to or larger than the top gate-oxide width. In the case b), both the sidewall gate-oxide are damaged by the heavy-ion strike.

$2 \cdot t_{ox} + W_{fin}$ which defines the width of the top gate oxide, becomes comparable to $r_{damage}$. When, for narrow-fin ($W_{fin} = 18$ nm) FinFETs, $N_{fin}$ is increased, both $P_{top}(h = 2)$ and $P_{sidewall}(h = 2)$ slightly increase if $r_{damage} < (2 \cdot t_{ox} + W_{fin}) / 2$, while they are practically constant otherwise.

It should be remarked that the parameter $\beta$ of the Weibull distribution indicates how much the gate-oxide degradation depends on the position of a heavy-ion strike and on the ion-to-ion LET variability. A large $\beta$, corresponding to a large spread in $1/\Delta I_G$, indicates a strong dependence on the position of the heavy-ion strike and the LET fluctuations.

## *7.5.2 Model*

Based on the previous hypothesis and considerations, $<\Delta I_G>$ can be described by:

$$<\Delta I_G> = N \sum_{h=1}^{M} \sigma_{top} P_{top}(h) <\Delta J_{G,top}(h)> + \\ + N \sum_{h=1}^{M} \sigma_{sidewall} P_{sidewall}(h) <\Delta J_{G,sidewall}(h)> \tag{7.5}$$

where $<\Delta J_{G,top}(h)>$ and $<\Delta J_{G,sidewall}(h)>$ are the average gate current density variations induced by heavy-ion strikes close to the same damaged area of the top and sidewall gate

oxide, respectively, and $\sigma_{sidewall}$ is the cross-section of the damaged sidewall gate oxide. Notice that $\sigma_{sidewall}$ considers the possibility that an ion hits both the sidewall gate oxides if $r_{damage}$ is equal to or larger than half of the top gate-oxide width (Figure 7.18):

$$\sigma_{sidewall} = \begin{cases} 2r_{damage}H_{fin} & if\ r_{damage} < \dfrac{W_{fin}+2t_{ox}}{2} \\ 2\left(2r_{damage}H_{fin}\right) & if\ r_{damage} \geq \dfrac{W_{fin}+2t_{ox}}{2} \end{cases}. \tag{7.6}$$

Obviously, for $h > 0$, $\langle \Delta J_{G,top}(h+1) \rangle \geq \langle \Delta J_{G,top}(h) \rangle$ and $\langle \Delta J_{G,sidewall}(h+1) \rangle \geq \langle \Delta J_{G,sidewall}(h) \rangle$ since the defect generation is expected to increase with increasing number of ion hits.

The experimental $\langle \Delta I_G \rangle$ (Figure 7.12) was fitted by means of the proposed model considering single, double, and triple ion hits and different $r_{damage}$ (Figure 7.19). The best fitting is obtained for $r_{damage}$ = 15 nm. However, for $r_{damage}$ > 15 nm the probability that a quadruple ion hit occurs is not negligible (≈ 1.5 %). Therefore, $r_{damage}$ can be estimated ≥ 15 nm. For $r_{damage}$ = 15 nm $\langle \Delta J_{G,top}(h=2) \rangle \approx 200$ mA/cm$^2$ while $\langle \Delta J_{G,sidewall}(h=2) \rangle \approx 300$ mA/cm$^2$. Similar results are obtained for the other $r_{damage}$ and $h$ = 1 and 3. This indicates that the sidewall gate oxide is more prone to developing defects than the top one. On the other hand, this may also indicate that $r_{damage}$ is larger along the sidewall gate oxide, so that the current density is the same both for the top and the sidewall gate oxide.

The larger $\langle \Delta J_{G,sidewall} \rangle$ compared to $\langle \Delta J_{G,top} \rangle$ can be due to the different crystallographic orientation between top and side silicon. It should be remarked that heavy ions with very high LET can induce a large amount of interfacial state density in the sidewall gate oxide with respect to the one of the top gate oxide. Indeed, non-45° rotated multigate transistors, as our samples, have different passivated interface trap state density at the top and lateral gates due to different lattice orientations. The {110} side surfaces originally have more dangling bonds than the {100} top surface. Passivated dangling bonds can become electrically active defects due to an ion strike, especially if this occurs on one of the {110} side surfaces. Therefore, TAT can be enhanced by such defects.

Notice that $r_{damage}$ has been estimated for a very high LET and not for the worst-case bias (floating device terminals). In the case of biased irradiation (i.e. operating voltage $V_{DD}$ = 1.2 V), $r_{damage}$ may be larger (also at lower LET), leading to a more dramatic increase in $I_G$, as the charge yield and propagation effects are expected to be larger [Ceschia00_2]. On the other hand, it should be remarked that, at very high LETs, the probability of multiple hits is vanishingly small in space [Dodd99]. However, the analysis methodology presented in this work can be used also for lower LETs, whose multiple-ion-hit probability is not negligible.

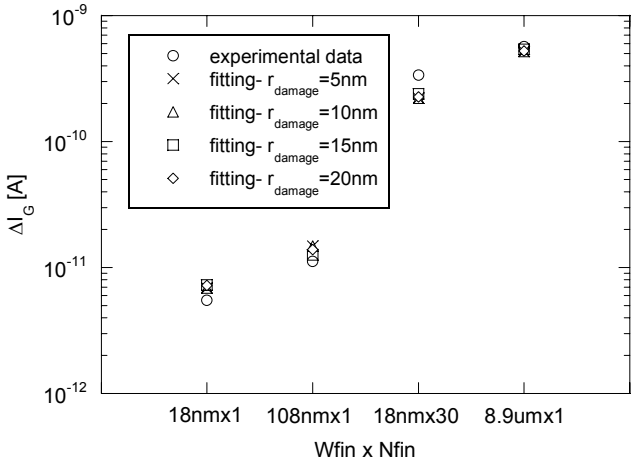



Figure 7.19: Comparison between the measured average increase in $I_G$ (at $V_{GS}$ = 1.2 V and $V_{DS} = V_{BS} = 0$ V) in NMOS FinFETs exposed to heavy-ion irradiation ($4.12 \cdot 10^{10}$ I ions/cm$^2$ with normal incidence) and the increase in $I_G$ calculated with the proposed model for four different damage radii. The considered devices have different $W_{fin}$ x $N_{fin}$, $H_{fin}$ = 65 nm, and $L_G$ = 810 nm.

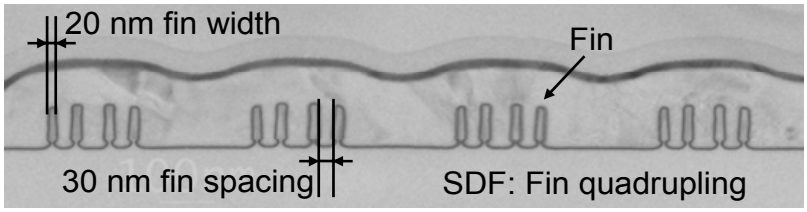



Figure 7.20: TEM image of fin quadrupling, obtained by Spacer Defined Fin methodology. The obtained fin width and fin spacing is 20 nm and 30 nm, respectively.

Further scaling down of multi-gate technology may lead to even more dramatic scenarios. For example, fin quadrupling schemes based on Spacer Defined Fins (SDF) can lead to a fin spacing as narrow as 30 nm or even less [Rooyackers06] (Figure 7.20). This means that an ion could hit two adjacent fins, broadening therefore the damaged region.

For the 22-nm technological node and beyond, the fin width is expected to reduce below 10 nm [ITRS08]. For such fin widths, the gate leakage current density is increased by quantum-mechanical effects induced by the silicon body. In detail, the total tunneling current density ($J_G$) for a planar MOSFET can be described by the model proposed by Register et al. [Register99]:

$$J_G = \sum_j \sum_i Q_{(j,i)} f_{(j,i)} T_{WKB_{(j,i)}} T_{R_{(j,i)}} \tag{7.7}$$

where $Q_{(j,i)}$ is the sub-band occupancy ($Q_{(j,i)}$-bound charge in each sub-band) of the different levels of each of the two valleys (longitudinal and transverse) ($j$ is the energy-level index and $i$ is the valleys index), $f$ is the impact frequency of the electron, $T_{WKB}(j,i)$ is the conventional Wentzel – Kramer - Brillouin (WKB) approximation for the transmission probability, and $T_R(j,i)$ is the correction factor due to reflections from the potential discontinuities. However, formula (7.7) does not take into account that an increase in fin width increases the distance between the peak of the electron concentration and the Si-$SiO_2$ interface (until $W_{fin}$ is so wide that quantum effects are not present). This results in a reduction in the tunneling current with an increase in the body thickness for double-gate devices [Chang02]. Since the WKB approximation does not consider the exact charge distribution, Mukhopadhyay et al. [Mukhopadhyay07] have introduced a $W_{fin}$ dependent semi-empirical function to account for this effect. Therefore, for a FinFET, $J_G$ is given by:

$$J_G = \left[ a_{W_{fin}} - b_{W_{fin}} ln\left( \frac{W_{fin}}{W_{fin}^{ref}} \right) \right] \left[ \sum_j \sum_i Q_{(j,i)} f_{(j,i)} T_{WKB_{(j,i)}} T_{R_{(j,i)}} \right] \tag{7.8}$$

where $a_{W_{fin}}$ and $b_{W_{fin}}$ are fitting parameters and $W_{fin}^{ref}$ is a fin width taken as reference (i.e. 5 nm). Hence, TAT through the sidewall gate oxides can be further enhanced by such quantum-mechanical effect. For our samples, which have 18 nm minimal fin width, such effect can be neglected as such increase in the sidewall gate-oxide leakage current density is lower than 5 %. However, such body-induced quantum-mechanical phenomenon has to be taken into account in the statistical analysis of heavy-ion induced degradation in further scaled down FinFETs.

Future works need to include the angular dependence, also taking into account grazing angles, LET fluctuations, and ions with a range of LETs and energies, and different $r_{damage}$, depending on the position of the ion strike (i.e., sidewall gate oxide vs. top gate oxide) and the number $h$ of multiple hits close to the same damaged region.

## 7.6 Angular Dependence

Even though some of the FinFETs showed GOX breakdown after exposure due to RSB, in this contribution we will focus only on those samples in which $I_G$ did not significatively change (< 5 %). In this section, the post-radiation characteristics of the devices hit by heavy ions with very high LET (60.1 MeV·cm$^2$/mg) are investigated.

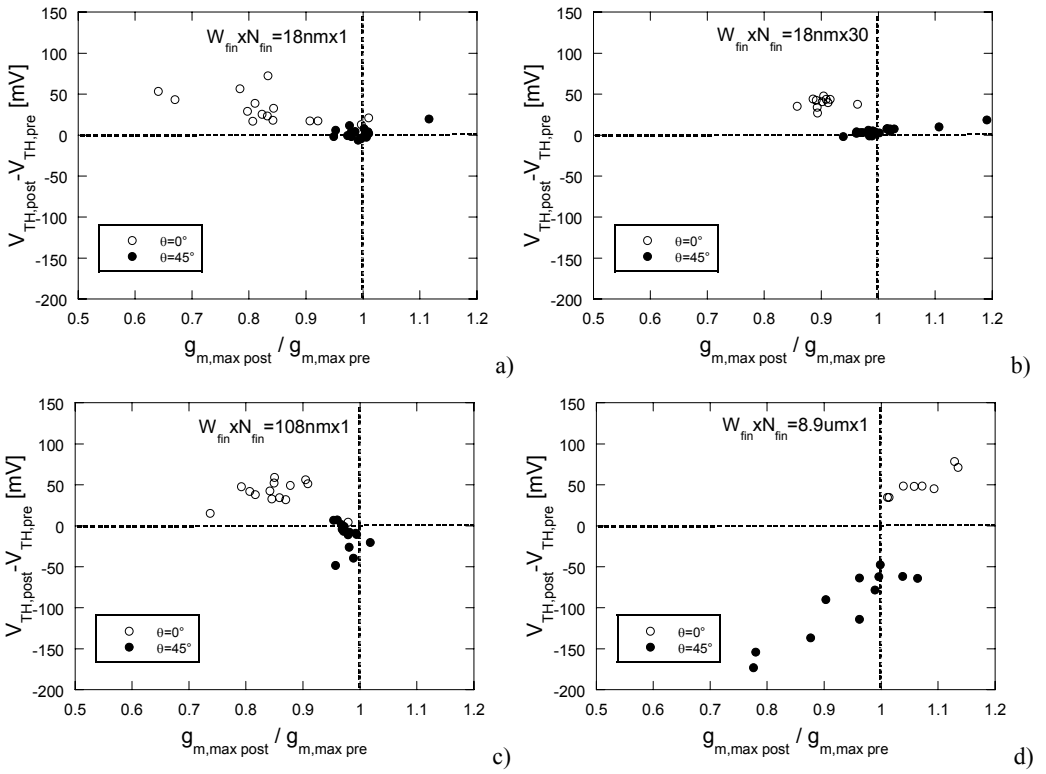



Figure 7.21: $V_{TH}$ shift as a function of $g_m$ drop after heavy-ion exposure at different incidence angles (normal incidence $4.12 \cdot 10^{10}$ I ions/cm$^2$ and 45° incidence $7.08 \cdot 10^9$ I ions/cm$^2$) for non-strained NMOS FinFETs with different $W_{fin}$ x $N_{fin}$ and $L_G$. $g_m$ and $V_{TH}$ were measured at $V_{DS}$ = 25 mV and $V_{BS}$ = 0 V.

Figure 7.21 shows the front-gate threshold voltage ($V_{TH}$) shift as a function of the peak of the transconductance ($g_m$) drop after heavy-ion exposure at $\theta$ = 0° (normal incidence) and 45° for NMOS SOI FinFETs with different $W_{fin}$ x $N_{fin}$ and $L_G$. A wide range of threshold voltage shifts, both negative and positive, and transconductance variations, both increase and decrease, is observed.

When the samples are irradiated at θ = 0°, the $V_{TH}$ shift is positive (up to 80 mV). The devices with $W_{fin} \leq$ 108 nm and long $L_G$ (= 810 nm) exhibit a larger $g_m$ drop (up to 35 %), while wide-fin ($W_{fin}$ = 8.9 µm) transistors display an improvement in gm up to 15 %. When FinFETs are irradiated at $\theta$ = 45°, the percentage of samples which show positive $V_{TH}$ shifts decreases with increasing $W_{fin}$. Indeed, 73 %, 22 %, and 0 % of the devices with $W_{fin}$ = 18 nm (narrow fin), 108 nm, and 8.9 µm, respectively, exhibit a modest increase (positive shift) in $V_{TH}$ (up to 20 mV), similar to the FinFET irradiated at $\theta$ = 0°. As a consequence, 27 %, 78 %, and 100 % of the transistors with $W_{fin}$ = 18 nm, 108 nm, and 8.9 µm, respectively, display a negative $V_{TH}$ shift. In most of the FinFETs irradiated at $\theta$ = 45°, the $g_m$ drops up to 23 %, especially for wide-fin

devices with long $L_G$. However, some sample with short $L_G$ (= 135 nm) displays a modest increase in $g_m$ (up to 10 %) regardless of $W_{fin}$.

### *7.6.1 Threshold Voltage Shift*

Shifts in $V_{TH}$ are related to microdose effects [Oldham93]. $V_{TH}$ can increase after irradiation because of negative charge trapping in the GOX, as already reported for planar bulk NMOS devices with high-k GOX [Dixit07], and/or due to an increase in the interface state density at the Si/BOX and Si/GOX interfaces. On the other hand, $V_{TH}$ can also decrease due to positive charge trapping in the BOX [Schwank03] [Paillet05]. It is the balance between these phenomena that probably gives rise to the different sign of the $V_{TH}$ shifts as a function of $\theta$. Such balance depends on the different areas of GOX vs. BOX affected by heavy-ion strikes. The amount of GOX and BOX damaged areas depend on the different regions (sidewall GOX, top GOX, or BOX) hit by the heavy ions as well as the position of the strikes, as reported in Table 7.II.

It should be remarked that multigate transistors may have a different passivated interface state density ($N_{it}$) at the top and sidewall GOX due to the different lattice orientations [Maeda04]. Therefore, heavy ions with very high LET can induce a large $N_{it}$ in the sidewall GOXs with respect to the one of the top GOX. Moreover, Monte Carlo simulations were run to look at the probability Psidewall that at least one heavy-ion strike occurs on the sidewall GOX, assuming an average size of the heavy-ion track useful to generate defects in the gate oxide of 30 nm as evaluated in (see section 7.5), and using the fluences in our experiments. For $\theta = 0°$, $P_{sidewall}$ is 100 % regardless of the device geometry; while, for $\theta = 45°$, $P_{sidewall}$ is $\approx 82$ % for short-channel FinFETs with $W_{fin} \geq 108$ nm and 100 % for the other geometries. Even though in most samples at least one sidewall GOX is affected by (at least) a heavy-ion strike, it should be remarked that, at $\theta$ = 0°, an ion strike in the sidewall GOX travels along the whole GOX height (= 68 nm). On the other hand, at θ = 45°, only a portion of the sidewall GOX is affected by the ion strike. Therefore, the number of interface states will be larger for $\theta = 0°$ with respect to $\theta = 45°$.

When FinFETs are struck by heavy ions with $\theta$ = 0° (Figure 7.21), the damaged GOX area is larger than the BOX one because at least one entire sidewall GOX is traversed by heavy ions. Thus, the radiation response of the GOX is much more important with respect to the one of the BOX, causing positive $V_{TH}$ shifts regardless of the device geometry. When the devices are struck by heavy ions with $\theta = 45°$, only a small portion of sidewall GOXs is affected by heavy-ion strikes. Therefore, the radiation response of the BOX can be, depending on the position of the strikes, less or more important than the one of the GOX, causing modest positive or negative $V_{TH}$ shifts, respectively. Moreover, the radiation response of the BOX is enhanced with increasing $W_{fin}$ (Figure 7.21). Indeed, for wide-fin SOI FinFETs, which are in essence planar SOI MOSFETs, the electrostatic

Table 7.II: Damaged regions, top GOX, sidewall GOX, and BOX damaged areas, probability, and expected $V_{TH}$ shift for SOI FinFETs with different fin widths struck by a single heavy ion with incidence angle 0° or 45°. The size of the heavy ion was considered of about 30 nm. (*) Top GOX area + sidewall GOX area = BOX area = constant. The expected $V_{TH}$ shifts are compared to the experimental $V_{TH}$ shifts.

$\theta = 0°$

| $W_{fin}$ | Damaged regions | Top GOX area [nm$^2$] | Sidewall GOX area [nm$^2$] | BOX area [nm$^2$] | Probability [%] | Expected $\Delta V_{TH}$ | Experimental $\Delta V_{TH}$ |
|---|---|---|---|---|---|---|---|
| 18 nm | 1 sidewall GOX + top GOX + BOX | 494.6 | ≤ 2040 | <494.6 | 62.5 | + | 100 % pos. $\Delta V_{TH}$ |
| | 2 sidewall GOXs + top GOX + BOX | 565.2 | 4080.0 | 565.2 | 37.5 | + | |
| 108 nm | top GOX + BOX | 706.5 | 0.0 | 706.5 | 71 | - | 100 % pos. $\Delta V_{TH}$ |
| | 1 sidewall GOX + top GOX + BOX | 706.5 | ≤ 2040 | <706.5 | 29 | + | |
| 8.9 µm | top GOX + BOX | 706.5 | 0.0 | 706.5 | 99.6 | - | 100 % pos. $\Delta V_{TH}$ |
| | 1 sidewall GOX + top GOX + BOX | 706.5 | ≤ 2040 | <706.5 | 0.4 | + | |

$\theta = 45°$

| $W_{fin}$ | Damaged regions | Top GOX area [nm$^2$] | Sidewall GOX area [nm$^2$] | BOX area [nm$^2$] | Probability [%] | Expected $\Delta V_{TH}$ | Experimental $\Delta V_{TH}$ |
|---|---|---|---|---|---|---|---|
| 18 nm | 1 sidewall GOX + BOX | 0.0 | ≤ 494.6 | <494.6 | 0.114 | - | 27 % neg. $\Delta V_{TH}$<br>73 % pos. $\Delta V_{TH}$ |
| | 2 sidewall GOXs + BOX | 0.0 | ≥ 494.6<br>≤ 1998.3 | <494.6 | 0.322 | + | |
| | 2 sidewall GOXs | 0.0 | 1998.3 | 0.0 | 0.23 | + | |
| | top GOX + 2 sidewall GOXs | < 565.2 | ≥ 999.1<br>≤ 1998.3 | 0.0 | 0.204 | + | |
| | top GOX + 1 sidewall GOX | < 565.2 | ≤ 999.1 | 0.0 | 0.13 | + | |
| 108 nm | 1 sidewall GOXs + BOX | 0.0 | ≤ 999.1 | <999.1 | 0.257 | - | 78 % neg. $\Delta V_{TH}$<br>22 % pos. $\Delta V_{TH}$ |
| | 1 sidewall GOX + top GOX + BOX | <999.1 | ≤ 999.1 | 999.1 | 0.1975 | - (*) | |
| | top GOX + BOX | 999.1 | 0.0 | 999.1 | 0.091 | - | |
| | 1 sidewall GOX + top GOX + BOX | <999.1 | ≤ 999.1 | <999.1 | 0.1975 | - | |
| | top GOX + 1 sidewall GOX | <999.1 | ≤ 999.1 | 0.0 | 0.257 | + | |
| 8.9 µm | 1 sidewall GOX + BOX | 0.0 | ≤ 999.1 | <999.1 | 0.006 | - | 100 % neg. $\Delta V_{TH}$ |
| | 1 sidewall GOX + top GOX + BOX | <999.1 | ≤ 999.1 | 999.1 | 0.005 | + (*) | |
| | top GOX + BOX | 999.1 | 0.0 | 999.1 | 0.977 | - | |
| | 1 sidewall GOX + top GOX + BOX | <999.1 | ≤ 999.1 | <999.1 | 0.005 | + | |
| | top GOX + 1 sidewall GOX | <999.1 | ≤ 999.1 | 0.0 | 0.006 | + | |

behavior is dominated by the front and back gates. The control of the lateral gates on the potential in the silicon body and BOX is relatively weak, contrary to narrow-fin devices [Frei04] [Daugé04] [Ritzenthaler06].

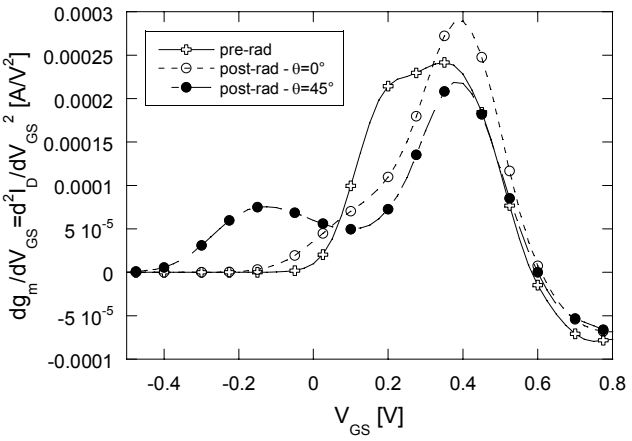



Figure 7.22: Derivative transconductance vs. gate voltage, $dg_m/dV_{GS}$, for a single-fin SOI FinFET with $W_{fin}$ = 8.9 μm and $L_G$ = 810 nm before heavy-ion exposure and after I ions irradiation at 0° and 45°. $g_m$ and $V_{TH}$ were measured at $V_{DS}$ = 25 mV and $V_{BS}$ = 0 V.

As an example of the different radiation response of GOX vs. BOX, we consider SOI FinFETs with a single wide (8.9 μm) 'fin' and long $L_G$ irradiated at $\theta$ = 0° and 45°. The different sign in $V_{TH}$ shift, positive for θ = 0° while negative for θ = 45°, can be due to the different amount of charge trapping in the GOX and BOX and interface states induced by the radiation at the Si/BOX and Si/GOX interfaces. The measurement of the subthreshold-swing variation ($\Delta S$) also indicates a larger interface-states generation for the normal incidence. Indeed, $\Delta S$ = 31 mV/dec for $\theta$ = 0° while it is only 12 mV/dec for $\theta$ = 45°. In order to further investigate the role played by the different contributions, to the $V_{TH}$ shifts, the derivative of the transconductance vs. gate voltage ($dg_m/dV_{GS}$) was plotted (Figure 7.22). Such plot reveals the formation of inversion layers at the different Si/oxide interfaces in the device [Colinge03] [Wu06]. The pre-rad curve presents a single peak, corresponding to the inversion threshold voltage at the top of the fin. When a device is irradiated at $\theta$ = 45°, positive oxide charges are created in the BOX [Schwank03], which reduces the threshold voltage of the bottom interface of the fin. As a result, an inversion layer forms at the bottom of the device before it forms at the top and two peaks, corresponding to the bottom and top inversions can be observed. When the sample is irradiated at $\theta$ = 0°, the main peak (corresponding to the top inversion) slightly shifts toward positive voltages, indicating the generation of interface states at the Si/GOX interface. The secondary peak (due to the bottom inversion) is strongly reduced if not obliterated by (probably) the creation of a large amount of interface states at the Si/BOX interface.

The reader might argue that in order to observe these effects, we need to use very high fluences and LETs, not so common in space, where, for a geosynchronous orbit, the integral flux at and above LET = 60 MeV·cm$^2$/mg, is less than 1 particle/cm$^2$ per hundred

years [Dodd99]. In the case of a single heavy-ion strike occurring for each device geometry, the $V_{TH}$ shift could result different compared to the experimental data of this work (see Table 7.II). Indeed, for $\theta$ = 0°, about 71 % and 99.6 % of the FinFETs with $W_{fin}$ = 108 nm and 8.9 µm, respectively, the $V_{TH}$ shift will be negative. The opposite sign of $\Delta V_{TH}$ (positive) will be observed otherwise. For $\theta$ = 45°, 11 %, 74 %, and 97.7 % of the samples with 18 nm, 108 nm, and 8.9 µm, respectively, will present a negative $V_{TH}$ shift; while it will be positive otherwise. Therefore, when a single heavy-ion strike occurs for all the geometries, a different complex scenario (compared to our experimental) can occur (i.e. negative $V_{TH}$ shift also for $\theta$ = 0°), depending on $W_{fin}$ and $\theta$, due to a different probability of hitting the sidewall GOXs.

### *7.6.2 Transconductance Variation*

The decrease in $g_m$ peak observed after heavy-ion strikes can be due to mobility reduction caused by the generation of interface states and to the increase in series resistance ($R_S$) (Fig. 7.23).

Dramatic changes in $g_m$ after irradiation have already been observed in planar bulk [Cester04] and SOI devices (see Chapter 6) belonging to the 65-nm node, and were attributed to the formation of a physically damaged region in the GOX.

The variation of the transconductance at higher gate voltages is related to the variation of the series resistance as well. The series resistance is extracted with the method described in [Simoen97] [Dixit05]. This method compares the total resistance ($R_{TOT}$) for a long channel ($L_{G,long}$ = 810 nm) and short channel ($L_{G,short}$ = 135 nm) device. $R_{TOT}$ is defined as:

$$R_{TOT} = \frac{V_{DS}}{I_D} = R_{CHAN} + R_S \,. \tag{7.9}$$

$R_{CHAN}$ is the intrinsic channel resistance, $V_{DS}$ = 25 mV, and $I_D$ is the drain current at $V_{GS}$ = 1.2 V, $V_{DS}$ = 25 mV, and $V_{BS}$ = 0 V. $R_S$ can be extracted with the help of the following approximation:

$$R_{CHAN,short} = \frac{L_{G,short}}{L_{G,long}} R_{CHAN,long} \,. \tag{7.10}$$

In irradiated NMOSFETs, $R_S$ increases up to 230 Ω for devices with $W_{fin} \leq$ 108 nm, while it decreases of few Ohms (less than 5 Ω) for wide-fin samples. The increase in $R_S$ can be attributed to the negative charge build-up in the nitrided LDD spacers, which wrap around the silicon fin(s) [Dixit08]. This is further substantiated by the decrease in

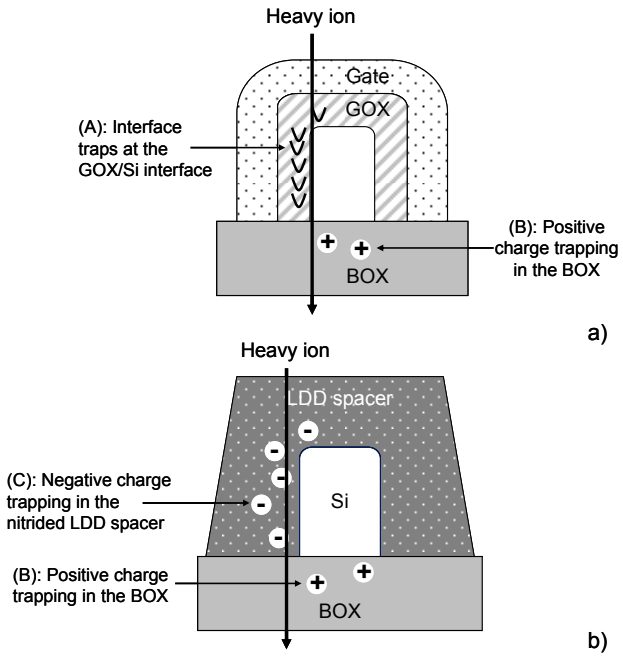



Figure 7.23. Schematic (not to scale) along cut-line A-A' of Figure.7.2 of the proposed mechanisms which may alter $g_m$ of irradiated SOI FinFETs: (A) interface states at the silicon body/gate oxide interfaces, (B) positive charge trapping the BOX, and (C) negative charge trapping in the nitrided LDD spacers.

the extracted $R_S$ for PMOS FinFET regardless of the fin width (i.e., $\Delta R_S$ = -12 Ω for $W_{fin}$ x $N_{fin}$ = 8.9 µm x 1 and -360 Ω for $W_{fin}$ x $N_{fin}$ = 18 nm x 1). However, the results obtained with this method are based on the drain current $I_D$, which depends also on the back-channel transistor. When irradiation shifts the onset of this back channel to lower gate voltages, it increases $I_D$, resulting in an apparent lower series resistance. The real variation in series resistance is masked by the onset of the back channel. This could explain the modest apparent decrease in series resistance for NMOS devices with a single wide fin.

The $g_m$ increase can be due to alterations of the parasitic back-channel transistor, induced by positive charge trapping in the BOX and back-channel threshold voltage ($V_{TH,back}$) roll-off (Fig. 7.23), emphasized by the lack of halo implants [Put07]. Notice again that for such fin width the electrostatic behavior is dominated by the front and back gates and not by the fringing field induced by the lateral gates [Frei04] [Daugé04] [Ritzenthaler06]

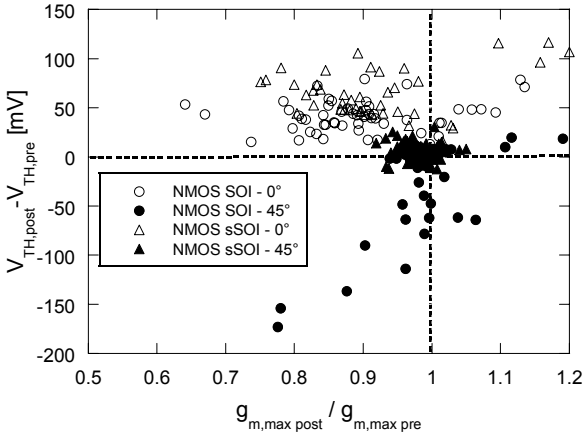



Figure 7.24: $V_{TH}$ shift as a function of $g_m$ drop after heavy-ion exposure at different incidence angles (normal incidence $4.12 \cdot 10^{10}$ I ions/cm$^2$ and 45° incidence $7.08 \cdot 10^9$ I ions/cm$^2$) for non-strained and strained NMOS FinFETs with different $W_{fin}$ x $N_{fin}$ and $L_G$. $g_m$ and $V_{TH}$ were measured at $V_{DS}$ = 25 mV and $V_{BS}$ = 0 V.

## 7.7 Strain Dependence

Even though some of the FinFETs showed gate-oxide (GOX) breakdown after exposure due to RSB, in this contribution we will focus only on those samples in which the gate current ($I_G$) did not significatively change (< 5 %). In this section, the post-radiation characteristics of the devices hit by heavy ions with very high LET (60.1 MeV·cm$^2$/mg) are investigated.

Figure 7.24 shows the $V_{TH}$ shift as a function of the $g_m$ drop after heavy-ion exposure at $\theta$ = 0° and 45° for SOI and sSOI NMOS FinFETs with different $W_{fin}$ x $N_{fin}$ and $L_G$. When the devices are irradiated at $\theta$ = 0°, sSOI FinFETs exhibit a larger positive $V_{TH}$ shift (up to 110 mV) compared to the SOI ones. On the contrary, when the devices are irradiated at $\theta$ = 45° a larger $V_{TH}$ shift is observed for SOI NMOS FinFETs.

It should be remarked that the buried interface of a tensile-stressed silicon film is under compressive stress. The oxidation of compressively stressed silicon gives rise to a higher density of dangling bond centers at the interface [Somers08]. Likewise, compressively strained Si-Si bonds are more likely to break and create new dangling bonds under irradiation conditions leading to large mobility degradation in the back channel (Figure 7.25), as observed with protons [Put07]. Indeed, such behavior was observed to depend on the back-gate voltage and can explain the larger increase in series resistance observed for strained NMOS FinFET compared to reference ones (i.e., 650 Ω vs. 230 Ω for narrow-fin samples irradiated at normal incidence). The higher generation of interface traps at the strained Si/BOX interface may be also the reason of the larger $V_{TH}$

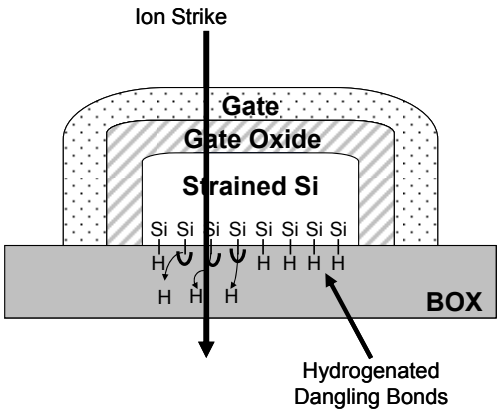



Figure 7.25: Schematic illustrations of compressive silicon / BOX interface with hydrogen passivated. The strained silicon/BOX interface has more dangling bonds than the non-strained one. Passivated dangling bonds can become electrically active defects due to an ion strike, especially if this occurs on strained FinFETs.

degradation observed for sSOI devices with respect to SOI ones, both irradiated at $\theta = 0°$. On the other hand, when the sSOI devices are irradiated at $\theta = 45°$ a balance between the large interface state density at the (strained) Si/BOX interface and the positive charge trapping in the BOX can occur, inducing a lower $V_{TH}$ degradation compared to SOI devices irradiated at the same $\theta$. Notice that the quality of the GOX is similar for both SOI and sSOI NMOS devices, as already reported for accelerated lifetime tests [Irisawa08] [Garros09].

## 7.8 Channel-Type Dependence

Figure 7.26 shows the $V_{TH}$ shift as a function of the $g_m$ drop after heavy-ion exposure at $\theta = 0°$ and 45° for SOI NMOS and PMOS FinFETs with different $W_{fin}$ x $N_{fin}$ and $L_G$. Contrary to NMOS samples, PMOS devices exhibit a negative $V_{TH}$ shift (up to -100 mV) regardless of $\theta$, while a larger $g_m$ drop (up to 30 %) is found for FinFETs irradiated at $\theta = 0°$. Radiation induced degradation of the GOX may be much smaller in P-channel than in N-channel devices, due to the opposite built-in field (please remember that the devices were unbiased during the exposure), causing the device response to be dominated by BOX degradation.

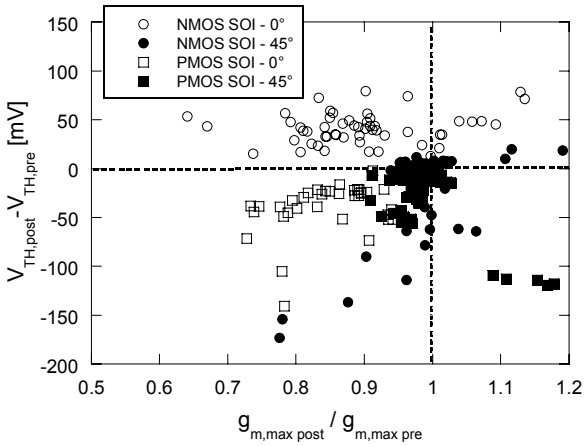



Figure 7.26: $V_{TH}$ shift as a function of $g_m$ drop after heavy-ion exposure at different incidence angles (normal incidence $4.12 \cdot 10^{10}$ I ions/cm$^2$ and 45° incidence $7.08 \cdot 10^9$ I ions/cm$^2$) for non-strained NMOS and PMOS FinFETs with different $W_{fin}$ x $N_{fin}$ and $L_G$. $g_m$ and $V_{TH}$ were measured at $|V_{DS}|$ = 25 mV and $V_{BS}$ = 0 V.

## 7.9 Long-Term Effects

In this section, the TDDB and the device parameter degradation kinetics of non-strained NMOS FinFETs hit by heavy ions with high and very high LETs are investigated.

### *7.9.1 Time-Dependent Dielectric Breakdown*

After irradiation, we submitted the samples with only marginal degradation in $I_G$ and $I_{DS}$ (less than 5%) to electrical stresses. In particular, the TDDB was measured on irradiated (at different $\theta$, LET, and fluence) and unirradiated single-fin devices with $W_{fin}$ = 18 nm and $L_G$ = 135 nm struck by 1 ion or 5 ions on the high-k GOX area. A 2x increase in $I_G$ at the monitor voltage ($V_{GS}$ = 1.2 V) was chosen as the breakdown criterion for unirradiated and irradiated devices, since they both exhibit progressive breakdown [Monsieur02] [Ribes05] (Figure 7.27). The average TDDB at $V_{GS,stress}$ = 3 V is shown in Figure 7.28. FinFETs hit by 1 Ni ion at θ = 0° have a TDDB (≈ 2400 s) similar to the one of unirradiated samples (≈ 2450 s), indicating the lack of latent GOX damage induced by the heavy-ion strike. When the fluence is increased up to 5 Ni ion strikes, the TDDB is decreased by 13 %. This can be due to latent GOX damage, possibly owing to multiple-ion hits close to the same GOX area. A stronger reduction in the FinFET lifetime is observed when 1 I ion with very high LET hits the GOX area, indicating that the TDDB

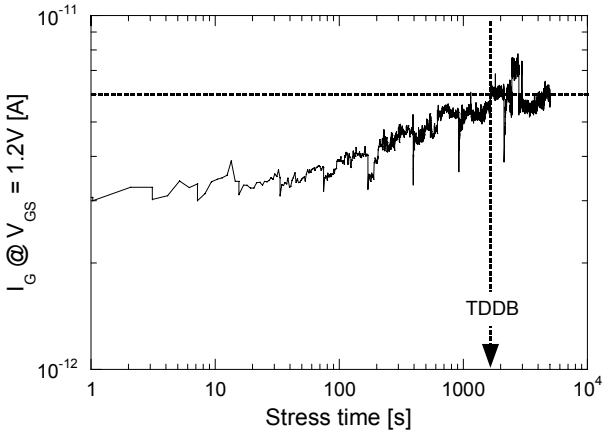



Figure 7.27: Gate current $I_G$ ($V_{GS}$ = 1.2 V and $V_{DS}$ = $V_{BS}$ = 0 V) as a function of the stress time for a non-strained NMOS FinFET with $W_{fin}$ x $N_{fin}$ = 18 nm x 1 and $L_G$ = 135 nm. The sample was submitted to Constant Voltage Stress (CVS) at $V_{GS,stress}$ = 3 V and $V_{DS}$ = $V_{BS}$.

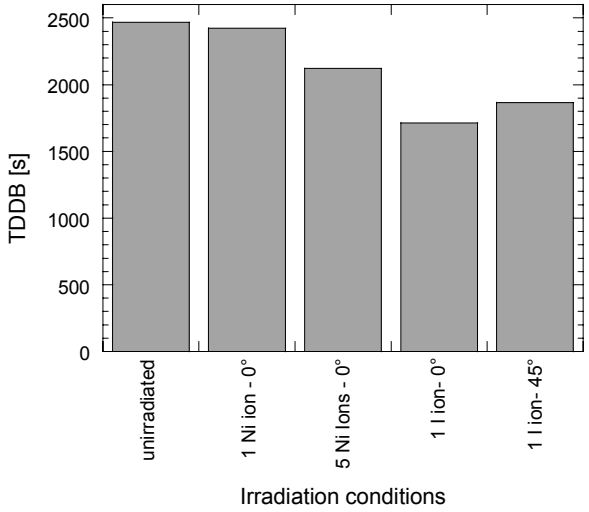



Figure 7.28: Average Time-Dependent Dielectric Breakdown (TDDB) for irradiated and unirradiated non-strained NMOS FinFETs with $W_{fin}$ x $N_{fin}$ = 18 nm x 1 and $L_G$ = 135 nm. The devices were stressed at constant voltage at $V_{GS,stress}$ = 3 V and $V_{DS}$ = $V_{BS}$ = 0 V.

decreases with increasing LET [Choi02]. Moreover, such decrease depends on $\theta$: TDDB in samples irradiated at $\theta = 45°$ is $\approx 1900$ s and $\approx 1700$ s at $\theta = 0°$. Again, this angular dependence can be explained taking into account the different GOX area affected by the heavy ion strike: $\leq 2040$ nm$^2$ for $\theta = 45°$, while $\leq 4080$ nm$^2$ for $\theta = 0°$, with the same assumptions used before. However, it should be remarked that such difference of 200 s in

TDDB is not much larger than the standard deviation of the TDDB of the samples ($\sigma_{TDDB} \approx 100$ s).

## *7.9.2 Device Parameter Degradation Kinetics*

The $V_{TH}$ degradation kinetics as a function of the injected charge ($Q_{inj}$) in the GOX during CVS for unirradiated and irradiated (at different $\theta$, LET, and fluence) single-fin NMOS SOI FinFETs with $W_{fin}$ = 18 nm and $L_G$ = 135 are shown in Figure 7.29. $V_{TH}$ shift ($\Delta V_{TH}$) increases with increasing $Q_{inj}$ following the well known power law:

$$\Delta V_{TH} = A \cdot Q_{inj}^{\,n} \tag{7.11}$$

where $A$ and $n$ are fitting parameters. The parameter $n$ is ≈ 0.25 and seems not to depend on the irradiation. On the contrary, the parameter $A$ is lower for irradiated devices with respect to unirradiated ones.

The change in $V_{TH}$ (both in irradiated and unirradiated devices) can be attributed to:

i) a significant creation of interface states either at the Si/GOX or at the Si/BOX interfaces, and
ii) negative charge build-up in the BOX.

Concerning i), a large generation in interface states can occur especially at the silicon-body/sidewall-GOX interfaces. This is because, after processing, FinFETs have a higher passivated interface trap state density at the sidewall gates compared to the top one due to different lattice orientations [Kapila07] [Groeseneken08_1]. Passivated dangling bonds can become electrically active defects due to an ion strike and during electrical stresses, especially on one of the side surfaces, resulting in a large threshold voltage shift in the side channels. This result is further substantiated by CVS on devices with different $W_{fin}$ (Figure 7.30), showing a lower increase in $V_{TH}$ shift with increasing $W_{fin}$. Concerning ii), it is well known that applying high voltages to the GOX can result in carriers reaching the BOX and creating defects there. In fact, biasing the back-gate at a given negative voltage has a similar effect on the electrical characteristics as stressing the device for a certain amount of injected charge in the GOX.

The irradiation alters this behavior, modifying the charge-trapping and interface-states generation kinetics in the BOX and in the GOX. The smaller increase in $V_{TH}$ in the irradiated samples as compared to the unirradiated devices may be due to defects (mainly vacancies, as suggested by SRIM simulations) induced by radiation in the silicon body, which may act as recombination centers and prevent the carriers at the front-gate from being injected in the BOX during CVS (please notice that the body is undoped). On the other hand, radiation can also generate defects in the GOX, inducing Trap Assisted Tunneling (TAT) and therefore paths with lower resistance through the GOX. In this manner, the electrons injected from the gate tend to tunnel mainly through such paths,

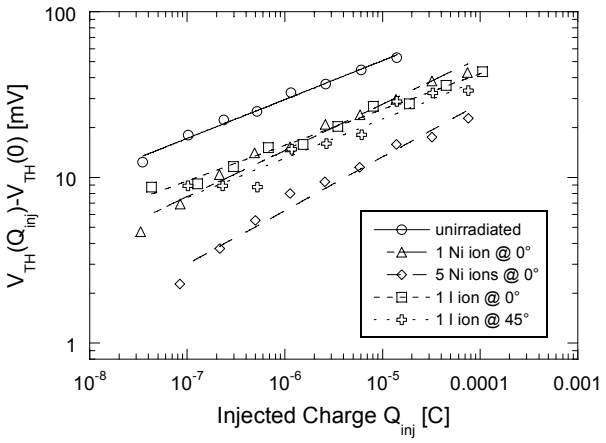



Figure 7.29: Typical $V_{TH}$ shift as a function of the injected charge during constant voltage at $V_{GS,stress}$ = 3 V in unirradiated and irradiated SOI NMOS FinFETs with $W_{fin}$ x $N_{fin}$ = 18 nm x 1 and $L_G$ = 135 nm. Immediately after irradiation FinFETs hit by 1 or 5 Ni ions at normal incidence or by 1 I ion at 45° show a modest decrease in $V_{TH}$ (≤ 3 mV), while samples hit by 1 I ion at normal incidence exhibit an increase in $V_{TH}$ of about 20 mV.

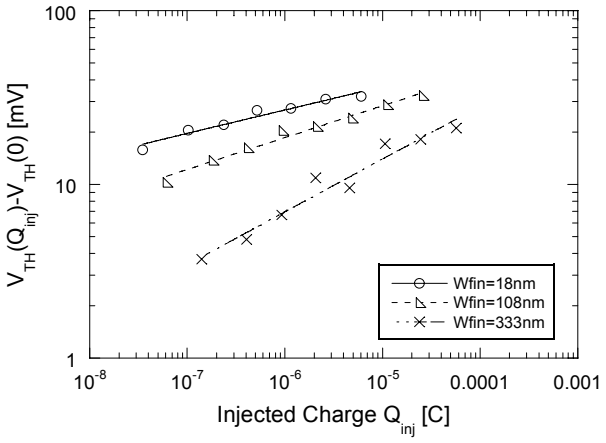



Figure 7.30: Typical $V_{TH}$ shift as a function of the injected charge during constant voltage at $V_{GS,stress}$ = 3 V in unirradiated single-fin SOI NMOS FinFETs with different $W_{fin}$ and $L_G$ = 135 nm. When the fin width is decreased, an increase in $V_{TH}$ shift is observed.

inducing a more localized damage at the BOX, which may impact less on the device characteristics than a uniform damage.

## 7.10 Conclusions

This chapter has shown that novel devices, such as FinFETs, intended to replace conventional bulk MOSFETs, feature complex geometries and innovative materials, which may deeply affect the permanent response to heavy-ion strikes. The threshold voltage shift after irradiation strongly depends on the LET, incidence angle, strain, and channel type, depending on the balance between damage to the high-k (top and sidewall) gate oxide and to the buried oxide. In addition, long term effects impacting the device wear-out have been considered. Heavy-ion strikes impact both on the degradation kinetics and on the time to breakdown under constant voltage stress.

In contrast with the reassuring data taken during SEGR experiments on large capacitors using high-k dielectrics, these multigate devices show that the soft rupture of the gate oxide may be a considerable concern, not only for the increase in gate leakage, but also for the effects on the DC characteristics. Interface state generation in the side oxide/body interface, due to ions passing through the lateral gates, is another remarkable effect that can be observed only with these vertical devices.

Heavy ions can induce permanent damage on FinFETs with large statistical spread. Nominally identical devices irradiated in the same conditions may exhibit up to two orders of magnitude of variation in the gate leakage current. The distribution of the inverse of the gate leakage currents and of the threshold voltage shifts was shown to follow a Weibull distribution. Moreover, the reciprocal of the gate leakage current was demonstrated to not respect the Poisson area scaling. A new model for the gate leakage current was proposed, which considers the contributions of both the top and the sidewall gate oxides and multiple ion hits. Our model predicts that the radius of the heavy-ion damage is about 15 nm, and a higher defect generation takes place in the sidewall gate oxide.

The data suggest that permanent or semi-permanent damage from heavy-ion strikes must be constantly monitored on FinFET devices, because of a very strong link with small geometries, especially on vertical structures.

# Chapter 8

# Dose Enhancement due to Interconnects

The presence of metal-1 tracks in the proximity of the device active areas may significantly modify the response to X-rays. The impact of the secondary electron emission from metal-1 layers is strongly dependent on the relative position to the transistor lateral isolation and LDD spacers.

## 8.1 Introduction

The radiation qualification of Commercial Off The Shelf (COTS) electronic components is an expensive and time-consuming task, made more complex by the ever-increasing process-to-process and chip-to-chip variability of modern ICs [Hughes03] [McLain07]. To measure the sensitivity to the different effects a whole set of radiation tests normally needs to be performed: total ionizing dose using an X-ray source, $Co^{60}$ γ-ray source, electron or proton beams; displacement damage using neutrons from a nuclear reactor or special neutron sources. Single event tests using high energy proton beams (60 MeV and above) and ion beams are also performed to assess the threat of single event upsets and latch-up.

Concerning total ionizing dose effects, $Co^{60}$ γ-ray sources or proton/electron beam irradiations are required to comply with the military and space standards [Fleetwood03]. On the other hand, cheaper and more accessible X-ray facilities are often used to perform total-dose tests, even though they have some shortcomings.

Secondary electrons emitted by metal layers during X-ray exposure may reach the MOSFET dielectrics, causing significant dose-enhancement effects [Schwank02] [Fleetwood85], which may be difficult to evaluate. These phenomena have been deeply

investigated for the gate electrode and oxide, which was once the major source of concern in old technologies [Scarpa97] [Ceschia98] [Ceschia00_1], but rarely considered for interconnects. The ever shrinking geometries of CMOS technology and the very high transistor density of modern ICs have caused the number and thickness of interconnect metal layers to increase from generation to generation. The presence of these layers must be carefully evaluated, especially since the switch from aluminum to copper interconnects.

Nowadays, the thinning of the gate oxide has made CMOS increasingly robust with respect to total ionizing dose, leaving edge-related issues as the most prominent effects [Oldham03] [Faccio05] [Barnaby06]. Below the 0.25 μm technology node Shallow-Trench Isolation (STI) is the only viable scheme to achieve device isolation with the required packing density and speed performance, improving also active area pitches and planarity [Peters99]. Radiation-induced charge trapping and interface state generation in the STI may turn on parasitic lateral transistors, causing increased leakage, possibly affecting the "drawn" transistor in small-width MOSFETs [Shaneyfelt98]. This makes the STI the central focus for total dose hardening [Shaneyfelt98] [Turowski04].

The presence of interconnect metal layers just a few hundreds of nanometers over the STIs and, more in general, over the MOSFET active areas, may significantly affect the outcome of irradiation performed with X rays. In this chapter, we will present the first original experimental contribution illustrating how secondary electrons, emitted by the first metal layer, alter total-dose effects in devices manufactured with a 90 nm CMOS process and designed with different ad-hoc interconnect layouts.

## 8.2 Experimental and Devices

We studied n-channel MOSFETs specifically designed and manufactured for this study by IMEC in a standard 90 nm bulk CMOS process, featuring STI and halo implants. The gate electrode was n-type polysilicon. The oxynitride (SiON) gate-oxide thickness was 1.6 nm. The back-end interconnections were manufactured with dual damascene copper in order to reduce the overall resistance, while a silica-based low-k dielectric is used as inter-layer. All the metal layers are made of copper. The maximum operating voltage ($V_{DD}$) was 1.5 V. Devices with channel width ($W$) 1 μm and 0.15 μm and channel length ($L$) 0.13 μm were used. The transistors were designed with three different metal-1 (M1) layouts (Figure 8.1 and Figure 8.2):

i. poly-M1 spacing = 1 μm (in the following '$L_{poly\text{-}M1}$ = 1 μm'): the distance between the polysilicon gate and the M1 track connected to source and drain is 1 μm;
ii. poly-M1 spacing = 1 μm + M1 plate (in the following '$L_{poly\text{-}M1}$ = 1 μm + plate'): the same layout as i. plus a floating M1 area over the gate;

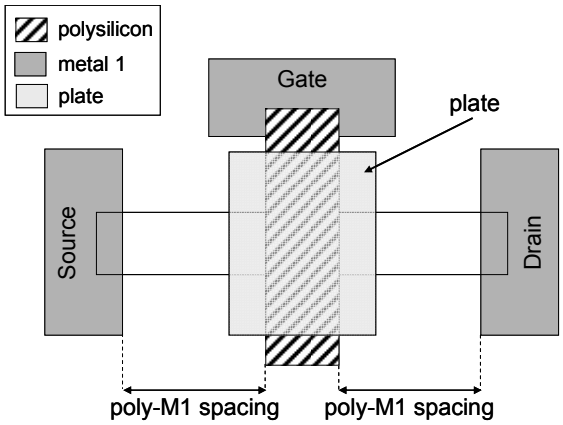



Figure 8.1: Schematic layout (not to scale) of the MOSFETs studied.

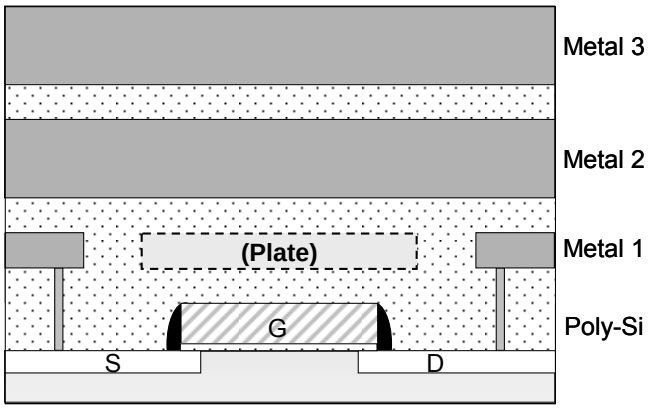



Figure 8.2: Schematic cross-section (not to scale) of a processed wafer.

iii. poly-M1 spacing = 0.1 μm (in the following '$L_{poly\text{-}M1}$ = 0.1 μm'): same as i. but the spacing between the polysilicon gate and the M1 track connected to source and drain is 0.1 μm.

Apart from the M1 layout, the transistors are perfectly identical (including source/drain vias) and located close one another in the wafer to minimize device-to-device variability.

Irradiation was performed at the SIRAD X-ray facility of the INFN Laboratori Nazionali di Legnaro, Italy. The samples were irradiated at room temperature in steps up to a total ionizing dose of 30 Mrad($SiO_2$), with the following experimental conditions: dose rate of 465 rad($SiO_2$)/s and X-ray energy of 10 keV. The irradiation was done keeping source and body terminals grounded, drain terminal at 10 mV and the gate at $V_{DD}$. The low bias at the drain ($V_{DS}$ = 10 mV) does not appreciably influence the radiation

response of the device and makes it possible to monitor the drain current during the irradiation. Before irradiation and after every irradiation step, we measured the gate current versus the gate voltage ($I_G$-$V_G$), the drain current versus the gate voltage ($I_{DS}$-$V_{GS}$) for different body voltages ($V_{BS}$ = 0 V, - 0.2 V, and -0.4 V), and the drain current versus the drain voltage ($I_{DS}$-$V_{DS}$) for different gate voltages ($V_{GS}$ = 0.9 V, 1.2 V, and 1.5 V) on each MOSFET.

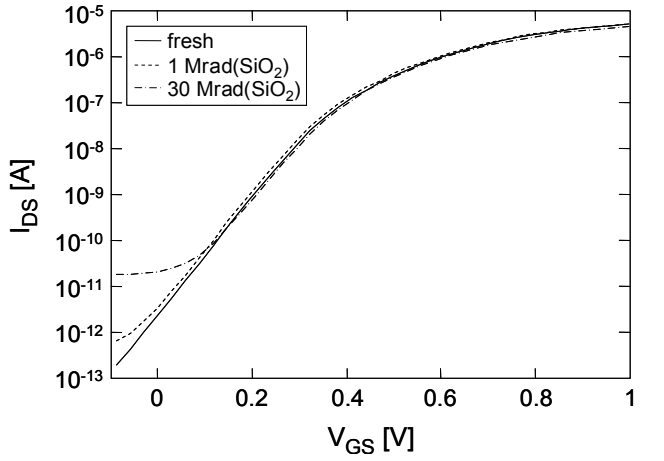
## 8.3 Results

Figure 8.3 shows the $I_{DS}$-$V_{GS}$ characteristics in semi-logarithmic (Figure 8.3a) and linear scale (Figure 8.3b) of a n-channel MOSFET with $L_{poly\text{-}M1}$ = 1 µm and $W/L$ = 0.15 µm/0.13 µm. Contrary to some results on comparable and older technologies [Oldham03] [Faccio05] [Barnaby06], these transistors exhibit only modest subthreshold humps, related to the activation of parasitic transistors at the poly/STI corners [Shaneyfelt98] [Turowski04]. This remains true also biasing the body terminal at negative voltages ($V_{BS}$ < 0 V), as shown in Figure 8.3. This is the best bias condition to better notice the influence of the parasitic MOSFET on the $I_{DS}$-$V_{GS}$ curves, because it allows us to detect charge trapped deeper in the STIs than at $V_{BS}$ = 0 V, due to the larger depletion region [Shigyo99]. Furthermore, Figure 8.3 shows that the threshold voltage ($V_{TH}$) shift is modest in such samples. In fact, $|\Delta V_{TH}|$ < 15 mV for the devices with $W$ = 0.15 µm (in the following 'narrow-channel MOSFETs'), while for the samples with $W$ = 1 µm (in the following 'wide-channel MOSFETs') the $V_{TH}$ shift is less than 5 mV up to 30 Mrad($SiO_2$).

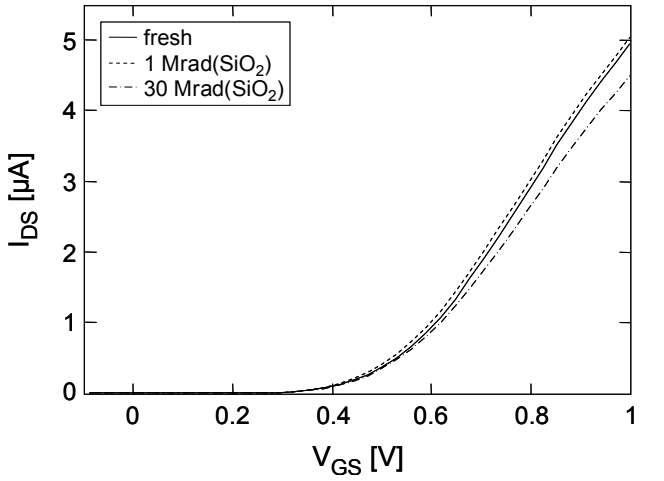
In order to analyze the dependence on the M1 layout and device geometry we will focus on $I_{DS,ON}$ (i.e. the drain current at $V_{GS}$ = 1.5 V, $V_{DS}$ = 25 mV, and $V_{BS}$ = 0 V) and $I_{DS,OFF}$ (i.e. the drain current at $V_{GS}$ = 0 V, $V_{DS}$ = 25 mV, and $V_{BS}$ = -0.4 V). These quantities are highly indicative of MOSFET degradation, and can be used to detect changes in threshold voltage, mobility, series resistance ($R_s$), and parasitic transistor leakage. We want to remark that the data reported in Figure 8.4, Figure 8.5, and presented in the following part of this section are measured on transistors belonging to the same die. Even though we found some die-to-die variability in the MOSFET parameters, the same quantitative relations between the degradation of the different layouts were observed in each tested die.

### *8.3.1 $I_{DS,ON}$ Degradation*

Figure 8.4 shows the typical relative variation of $I_{DS,ON}$ ($\Delta I_{DS,ON}(TID)/ I_{DS,ON}(fresh)$) as a function of the received dose for different layouts and channel widths. For each transistor the degradation kinetics of $I_{DS,ON}$ can be divided in two phases, based on the




a)




b)

Figure 8.3: $I_{DS}$-$V_{GS}$ characteristics ($V_{DS}$ = 25 mV and $V_{BS}$ = -0.4V) in a) semi-logarithmic and b) linear scale before irradiation, after 1 Mrad($SiO_2$), and after 30 Mrad($SiO_2$) for a nMOSFET with $L_{poly\text{-}M1}$ = 1 µm and $W/L$ = 0.15 µm/0.13 µm.

changing slope of the curves. This behavior depends on channel width: the slope change occurs at lower doses (between 1 and 1.5 Mrad($SiO_2$)) in narrow-channel MOSFETs than in wide-channel ones (between 2.3 and 3.4 Mrad($SiO_2$)). Furthermore narrow MOSFETs are more affected than wide ones. For example, at the end of the irradiation (*TID* = 30 Mrad($SiO_2$)) the drain current drop is larger than 10 % for narrow MOSFETs, while less than 6 % for wide ones.

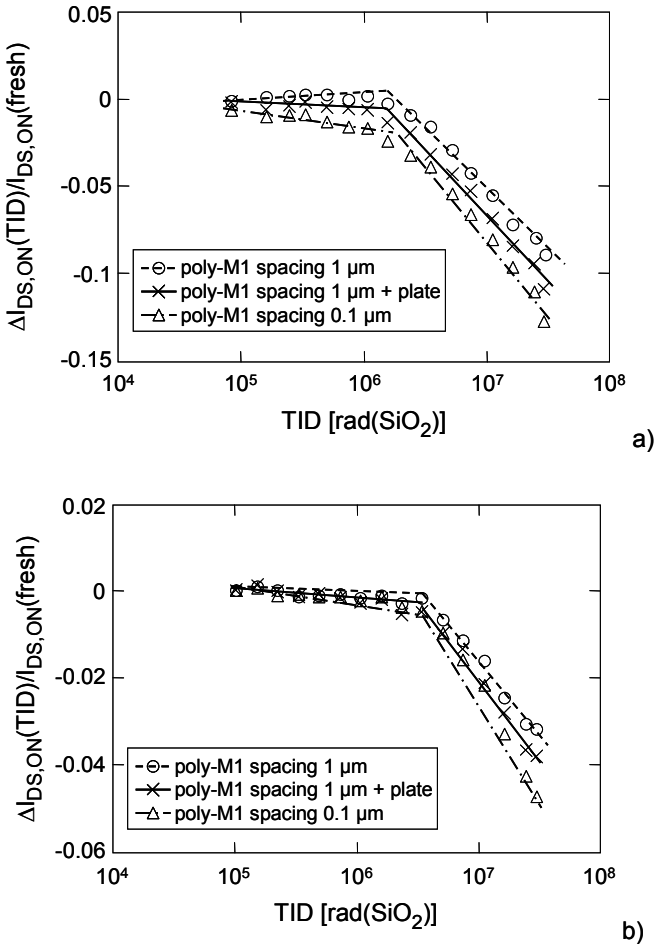



Figure 8.4: Typical relative $I_{DS,ON}$ variation ($V_{GS}$ = 1.5 V, $V_{DS}$ = 25 mV, and $V_{BS}$ = 0 V) as a function of the Total Ionizing Dose (TID) for nMOSFETs with different metal-1 layouts and with a) $W/L$ = 0.15 µm/0.13 µm and b) $W/L$ = 1 µm/0.13 µm.

Concerning the dependence on the M1 layout, the degradation of $I_{DS,ON}$ depends on the chosen layout for both channel widths. The drain current related to MOSFETs with the larger poly-M1 spacing degrades less than the other samples, independent from channel width. In other words, the slope is smaller in MOSFETs with $L_{poly\text{-}M1}$ = 1 µm than in samples with $L_{poly\text{-}M1}$ = 1 µm + plate or $L_{poly\text{-}M1}$ = 0.1 µm, indicating that the first one is less affected by radiation. Moreover, in the first irradiation phase, narrow transistors with $L_{poly\text{-}M1}$ = 1 µm experience an increase in $I_{DS,ON}$ while the wide counterparts remain unaltered. On the contrary, in the devices with other layouts the drain current degradation slope decreases monotonically. Moreover, Figure 8.4 shows that the transistors with $L_{poly\text{-}M1}$ = 0.1 µm exhibits the largest degradation regardless of the channel width. Indeed, the

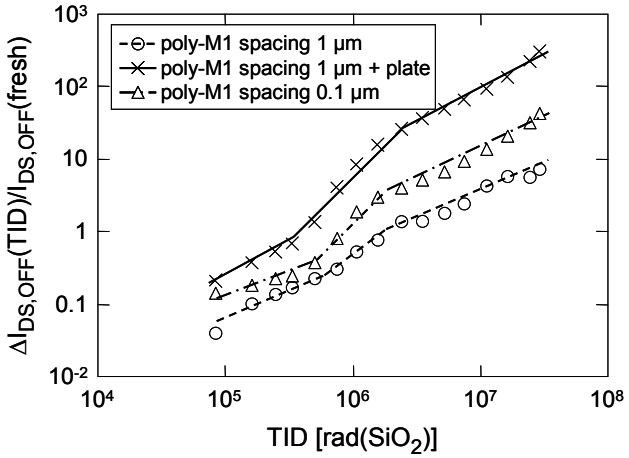



Figure 8.5: Typical relative $I_{DS,OFF}$ variation ($V_{GS}$ = 0 V, $V_{DS}$ = 25 mV, and $V_{BS}$ = -0.4 V) as a function of the Total Ionizing Dose (TID) for nMOSFETs with different metal-1 layouts and with $W/L$ = 0.15 µm/0.13 µm.

slope is larger in MOSFETs with $L_{poly\text{-}M1}$ = 0.1 µm than in the ones with $L_{poly\text{-}M1}$ = 1 µm or $L_{poly\text{-}M1}$ = 1 µm + plate.

## *8.3.2 $I_{DS,OFF}$ Degradation*

Concerning the degradation kinetics of $I_{DS,OFF}$, Figure 8.5 shows the typical relative variation of $I_{DS,OFF}$ ($\Delta I_{DS,OFF}(TID)/ I_{DS,OFF}(fresh)$) as a function of the dose for narrow-channel MOSFETs with different layouts. The same curves for wide-channel devices do not exhibit any dependence on the layout and the increase in relative $I_{DS,OFF}$ variation is less than 10 %. For each layout the kinetics can be divided in three phases; each of them follows a power law of the dose of the form:

$$\Delta I_{DS,OFF}(dose)/ I_{DS,OFF}(fresh) = A \cdot dose^{k} \qquad (8.1)$$

where $A$ and $k$ are fitting parameters. The exponent $k$ is different for each of the three mentioned phases, but (in first approximation) does not depend on the layout: $k$ is equal to ~ 0.8 – 0.9 in the first phase ($dose \leq$ 650 krad($SiO_2$)), ~ 2.5 in the second phase (650 krad($SiO_2$) < $dose$ < 2.6 Mrad($SiO_2$)), and ~ 1 the last one ($dose \geq$ 2.6 Mrad($SiO_2$)). On the other hand, the factor A depends mainly on the metal-1 layout. As reported in Figure 8.5 the $I_{DS,OFF}$ degradation is smaller in narrow devices with $L_{poly\text{-}M1}$ = 1 µm. On the contrary, narrow-channel samples with plate exhibit the largest $I_{DS,OFF}$ degradation, differently from what we observe concerning $I_{DS,ON}$ degradation.

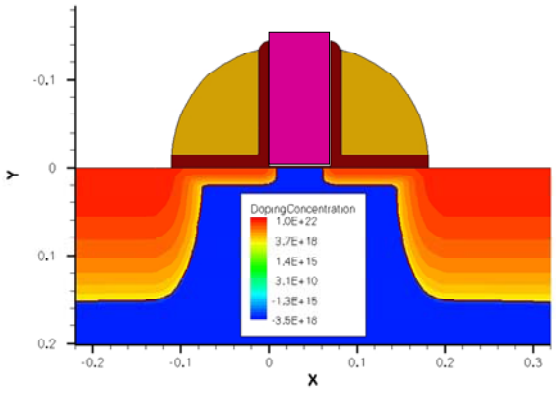



Figure 8.6: 2-D structure of the nMOSFET used in our simulations ($W/L$ = 0.15 µm/ 0.09 µm).

## 8.4 Discussion

As we have shown in the previous section, the kinetics degradation of a given parameter considered in this work is qualitatively the same, irrespective of the layout. Therefore, the first part of the discussion will be devoted to analyzing the mechanisms underlying the device response to total ionizing dose, whereas the second part will investigate the impact of the metal-1 layout on those mechanisms.

### *8.4.1 MOSFET Degradation*

The drain current decrease as a function of the received dose (Figure 8.4) may be due to different causes:

a) threshold voltage shift and mobility degradation due to charge trapping and interface state generation at the gate oxide/Si channel interface;
b) threshold voltage shift and mobility degradation due to charge trapping and interface state generation at the STI/Si channel interfaces;
c) increased series resistance due to negative charge build-up in the LDD spacers (the nitrided LDD spacers, differently from STIs, are prone to trap electrons [Wrazien03] [Gerardin06]).

Concerning mechanism a), the increase in the interface state density at the gate oxide/Si channel interface can account only for a small degradation of the drain current. Indeed, the change in the subthreshold swing is less than 2 mV/dec after 30 Mrad($SiO_2$), corresponding to an increase in the interface state density smaller than $10^{11}$ $cm^{-2}$, and the threshold voltage shift is unappreciable. This indicates that the generation of interface

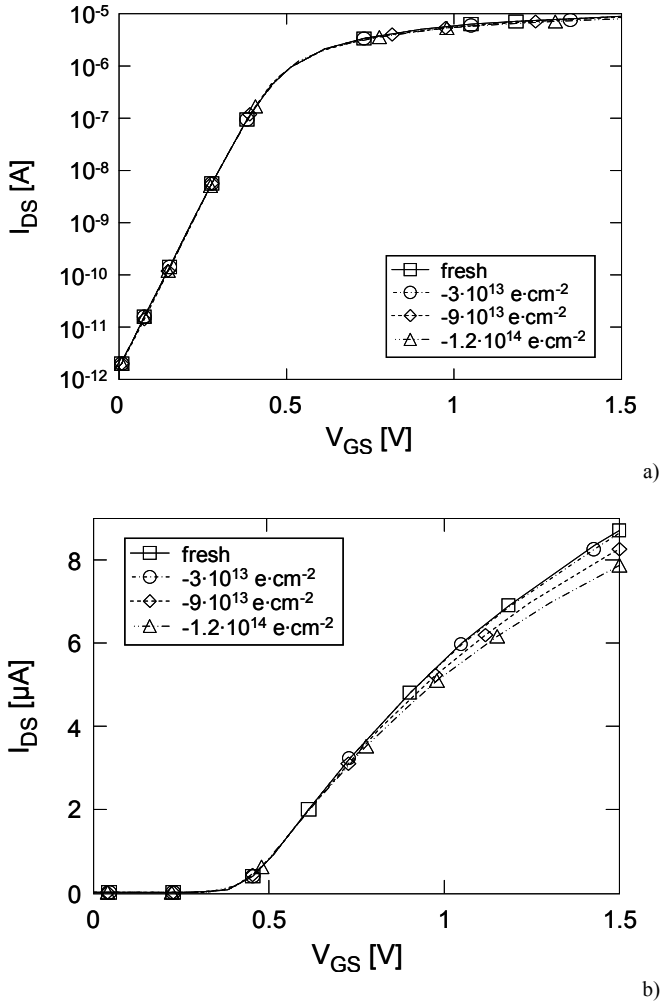



Figure 8.7: Simulated $I_{DS}$-$V_{GS}$ curves ($V_{DS}$ = 25 mV and $V_{BS}$ = 0 V) in a) semi-logarithmic and b) linear scale for different amounts of negative charge trapping in the LDD spacers for a nMOSFET ($W/L$ = 0.15 µm/ 0.13 µm).

states and charge trapping due to radiation is very limited, as expected from an ultra-thin gate oxide [Saks86].

Mechanism b) is usually invoked to explain differences in the degradation between narrow and wide channel device [Faccio05] and is known to generate a hump in the subthreshold characteristic, similar to that visible in Figure 8.3a. Indeed, $I_{DS,OFF}$ degradation (Figure 8.5) can be ascribed to a change in the threshold voltage of parasitic transistors caused by radiation-induced trapped charge in the STI [Faccio05].

But neither a) nor b) can alone explain the degradation of series resistance that seems to characterize the behavior of our transistors. To evaluate the impact of mechanism c) we performed TCAD physical device simulations with ISE TCAD DESSIS simulator. We based our simulations on standard values available for 90-nm IMEC

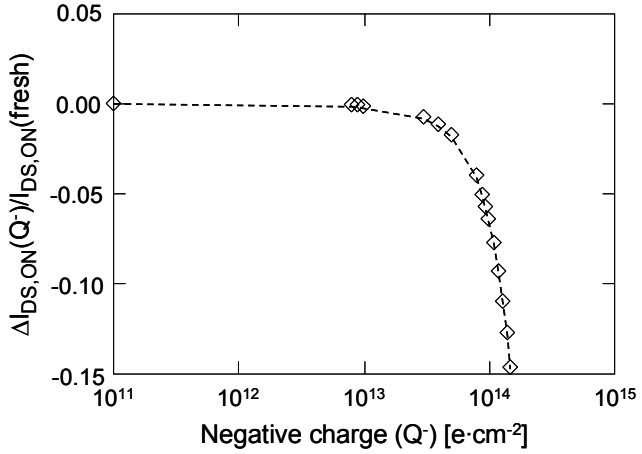



Figure 8.8: Simulated relative $I_{DS,ON}$ variation ($V_{GS}$ = 1.5 V, $V_{DS}$ = 25 mV, and $V_{BS}$ = 0 V) as a function of the negative charge trapping density in LDD spacers ($Q^-$) for a nMOSFET with $W/L$ = 0.15 µm/0.13.

technologies (Figure 8.6), using the hydrodynamic model with high-field saturation and mobility degradation models including doping-dependence and carrier-carrier scattering.

Figure 8.7 shows the simulated $I_{DS}$-$V_{GS}$ curves in linear and semi-logarithmic scale for different amounts of negative trapped charge in the LDD spacers that measure 90 nm and 120 nm in length and height, respectively (see Figure 8.6) Radiation-induced charge trapping was simulated using an equivalent negative sheet of charge inserted at the spacer/silicon interface ranging from $1 \cdot 10^{11}$ to $1.5 \cdot 10^{14}$ [cm$^{-2}$]. In agreement with the experimental results reported in Figure 8.3, a negligible increase in subthreshold swing and a modest increase in $V_{TH}$ (up to ~ 10 mV) are observed in the simulated electrical DC characteristics. At the same time the simulations reproduce very well the behavior at high gate voltage. Obviously, the simulated characteristics do not show any increase in $I_{DS,OFF}$, as no positive trapped charge has been introduced in the STIs.

Figure 8.8 shows the simulated relative $I_{DS,ON}$ degradation as a function of the amount of negative trapped charge in the LDD spacers. Based on the changing slope of the curve, the simulated degradation kinetics of $I_{DS,ON}$ can be divided in two phases: in the first one ($Q^- < 3 \cdot 10^{13}$ e·cm$^{-2}$) $I_{DS,ON}$ slowly decreases, whereas in the second phase ($Q^- > 3 \cdot 10^{13}$ e·cm$^{-2}$) the change is much more pronounced. This trend is qualitatively in good agreement with the experimental results shown in Figure 8.4 (of course a correlation between trapped charge and dose would be required for a full assessment).

What our 2-D simulations cannot explain is the different amount of degradation between wide and narrow devices (see again Figure 8.4). This fact can be justified assuming that the increase in series resistance is enhanced in narrow devices due to further negatively charged interface states that may be present on the STI sides (along the device length). Latent pre-existing defects, which may lead to defects after X-ray

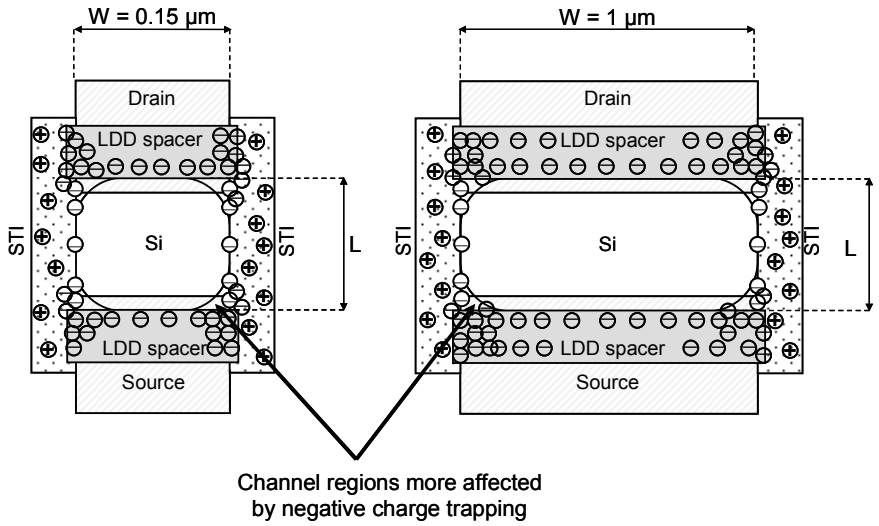



Figure 8.9: Schematic top view (not to scale) for a narrow (on the left) and wide (on the right) channel MOSFETs. For narrow devices the series resistance is further increased by negatively charged interface states in the STIs close to the drain/source junction.

exposure, generated from mechanical stress to the atomic structure cannot be excluded. This phenomenon is certainly emphasized at the LDD-STI corners as shown in Figure 8.9, affecting the series resistance especially in narrow devices ($W$ = 0.15 µm) and to a lesser extent in wide ones ($W$ = 1 µm).

## *8.4.2 Layout Dependence of Degradation*

Before going on with the discussion, we want to further remark that the different types of transistors we tested are identical but for the M1 layout, as described in the experimental and devices section. The higher degradation of $\Delta I_{DS,ON}(TID)/I_{DS,ON}(fresh)$ in MOSFETs with $L_{poly\text{-}M1}$ = 0.1 µm as compared to the ones with $L_{poly\text{-}M1}$ = 1 µm can be explained by dose enhancement effects due to the copper metal 1 layer. In fact, secondary electrons generated in the overlap area between metal 1 and the source/ drain junctions may cause enhanced charge trapping and interface state generation in the regions directly above the source and drain junctions. A smaller $L_{poly\text{-}M1}$ means that the metal track is closer to the LDD spacers, whose degradation, as we have suggested in the previous section, could be the main cause of the increase in series resistance, that leads to the reduction of $I_{DS,ON}$ with dose in these devices.

Transport code [Casino] was run to look at the range of 10-keV secondary electrons with initial momentum normal to the layers in low-k dielectrics for a typical 90-nm CMOS process. Here, the isolation between two consecutive metal layers is ~ 200 nm, the polysilicon is ~ 150 nm, metal 1 is ~ 150 nm, and metals 2 and 3 are ~ 250 nm

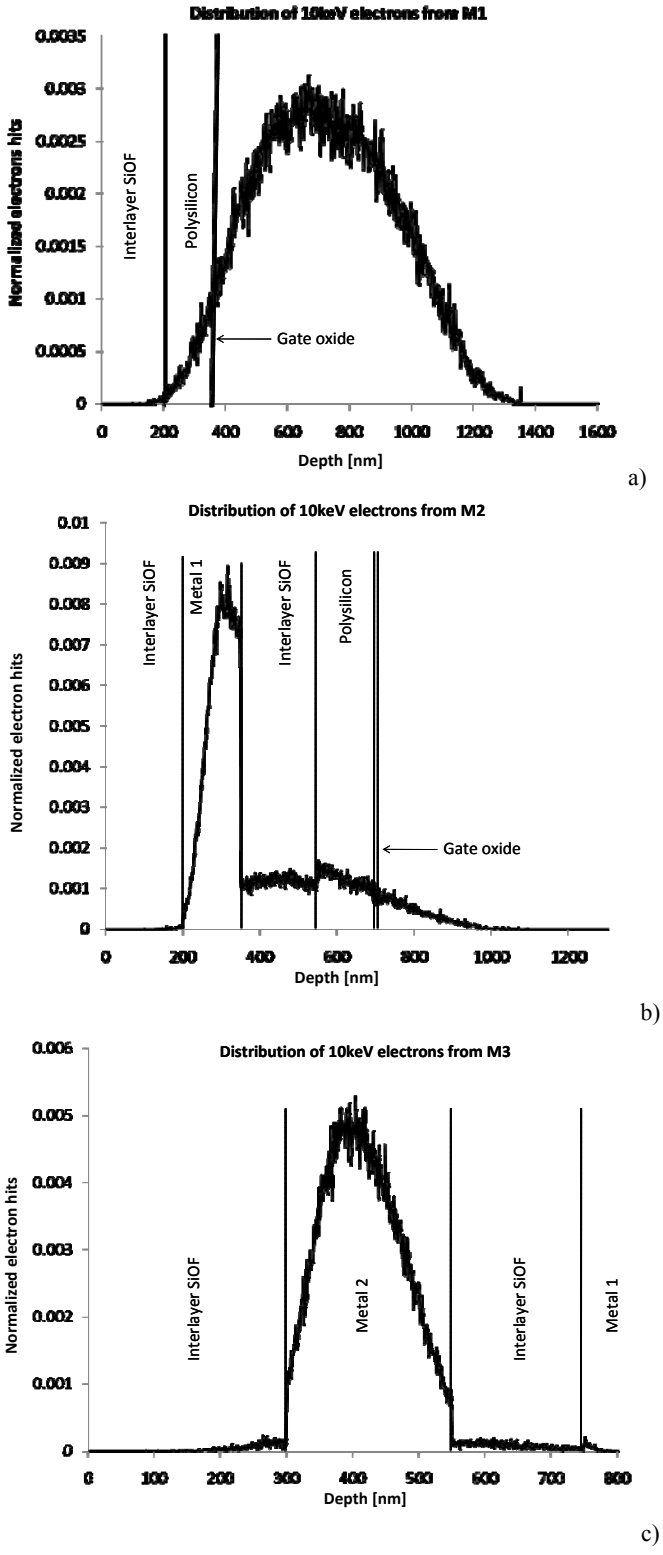



Figure 8.10: Normalized distribution of 10-keV electron hits emitted by a) Cu metal 1, b) Cu metal 2, and c) Cu metal 3 in a typical 90-nm CMOS process. Notice that the initial momentum of the electrons is normal to the layers.

[Thompson02]. The electron distributions (Figure 8.10) show that the secondary electrons emitted by metal 1 of copper can be deposited in the active device area. On the contrary, only a negligible amount of secondary electrons emitted by metal 2 (in these simulations the electrons do not have isotropic initial momentum) and 3 of copper can get to such area. For this reason, a contribution in dose enhancement effects should be expected by only metal 1, the more because metal layers are made of copper [Solin00]. On the contrary, metals 2 and 3 should not influence appreciably the response of the MOSFET under X-ray exposure, since they are too far from the sensitive regions.

In a similar way, the secondary electrons emitted by the M1-plate increase total-ionizing-dose effects in the LDD spacers, and STI. As a result, $I_{DS,ON}$ degradation is larger with the M1 plate, for a given M1-poly spacing.

Concerning the drain-source leakage current, as we mentioned, $I_{DS,OFF}$ degradation is related to the shift in threshold voltage of the parasitic lateral transistors due to radiation-induced trapped charge in the STI [Faccio05]. Reducing $L_{poly\text{-}M1}$ has a detrimental effect on $I_{DS,OFF}$, since it increases dose enhancement in the lateral isolation. The presence of the metal-1 plate is even more harmful for $I_{DS,OFF}$, because the overlap area with the STI is larger in this case.

To summarize, the dose to failure of $I_{DS,ON}$ and $I_{DS,OFF}$ as a function of layout is presented in Figure 8.11 for narrow-channel transistors. The dose to failure for each layout is calculated as the dose at which $I_{DS,ON}$ decreases by 10 % in Figure 8.11.a, and $I_{DS,OFF}$ doubles in Figure 8.11.b. All values are normalized to the corresponding dose value of the reference device with $L_{poly\text{-}M1}$ = 1 μm and no plate. Concerning $I_{DS,ON}$, the presence of M1 plate reduces the dose at which the device goes out of specification (with respect to the reference sample) by 37 %. A similar result is obtained reducing $L_{poly\text{-}M1}$ from 1 μm to 0.1 μm (48 % of the corresponding dose for a reference sample). Concerning drain-source leakage current, the presence of the M1-plate drastically reduces the dose at which $I_{DS,OFF}$ doubles (by 80%). Reducing $L_{poly\text{-}M1}$ has also a very strong impact on $I_{DS,OFF}$, causing a 63% decrease in the dose to failure.

These results are quite remarkable compared to the ones in the literature [Hughes03] [McLain07] [Fleetwood03], but we have to remark that the metal layers of our process are made of copper instead of aluminum, which is usually employed, especially as metal 1.

Dose enhancement with gamma-rays due to metal layers is expected to be much smaller than with x-rays for two reasons. Photons produced by X-rays (~ 10 keV) interact with matter primarily via the photoelectric effect, which scales with $Z^4$. On the other hand, higher-energy photons generated by $Co^{60}$ (~ 1 MeV) interact with matter primarily via the Compton effect, which is largely independent of Z. As a consequence secondary electron generation changes considerably from material to material in the first case, and much less in the second [Fleetwood85]. Furthermore, because of the very different range of the secondary electrons generated by X- and γ-rays, only regions close to the area of

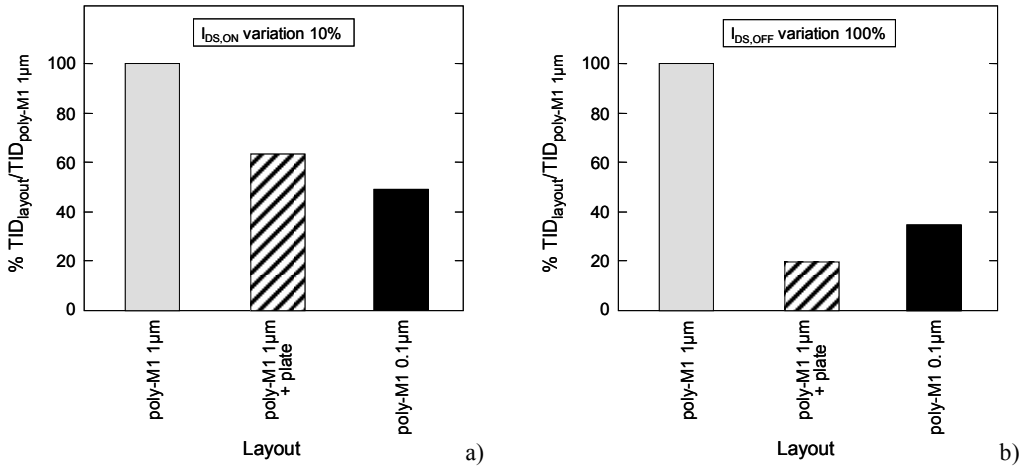



Figure 8.11: Normalized TID enhancement in a) $I_{DS,ON}$ and b) $I_{DS,OFF}$ as a function of the device layout for transistors with $W/L$ = 0.15 µm/0.13 µm. The normalized TID for each layout is calculated as the TID at which $I_{DS,ON}$ decreases of 10 % or $I_{DS,OFF}$ increases of 100 % normalized to the corresponding TID for a nMOSFET with $L_{poly\text{-}M1}$ = 1 µm and $W/L$ = 0.15 µm/0.13 µm.

interest may enhance the dose in the first case. For gamma rays instead, also regions further away can contribute, thus making the overall contribution of metal 1 less important.

## 8.5 Conclusions

The presence of metal-1 tracks in the proximity of the device active areas may significantly modify the response to X-rays of deep-submicron CMOS technologies. The impact of the secondary electron emission from metal-1 layers is strongly dependent on the relative position to the transistor lateral isolation, LDD spacers, and gate oxide. In particular, secondary electrons generated over source/drain junctions cause significant dose-enhancement effects in the LDD spacers, which are the main responsible of series resistance degradation in these devices.

Dose enhancement in deep-submicron devices must be carefully considered when X-ray facilities are used to perform total-dose tests, due to the strong impact that metal-1 interconnects, especially when made of copper, can have on the final results.

# Chapter 9

# Conclusions and Outlook

ESD is not a showstopper for the introduction of Ultrathin Body SOI and FinFET technologies, which ESD robustness strongly depends on layout and process parameters. Further, microdose effects induced by heavy ions are a serious concern for the introduction of FinFET technology in future COTS components for space applications.

## 9.1 Conclusions

In this thesis, three major challenges for novel devices, such as Ultrathin Body SOI and FinFET devices, have been addressed. First, the basic ESD performance of common protection devices implemented in UTB SOI, SOI FinFET, and bulk FinFET technologies has been analyzed. Secondly, the heavy-ion induced microdose effects on UTB SOI and SOI FinFET technologies have been investigated. Large dependencies on device layout parameters and process options have been found regarding both ESD and microdose effects. Thirdly, it has been shown that the total-dose hardness of commercial ICs remains problematic since a considerable variability can exist within a single fabrication lot.

*ESD robustness of Ultrathin Body SOI*

Non-strained UTB SOI MOSFETs can achieve up to 1 mA/μm current capability, making them robust enough when local clamping devices are used. Indeed, such value of normalized $It_2$ is comparable to the ones obtained for partially depleted SOI with larger silicon thickness, whose $It_2$ per transistor width ranges between 3.5 mA/μm and 1.1 mA/μm [Russ08]. Despite our samples have negative front-gate threshold voltage, final metal-gate devices could be biased during ESD events to restore maximum $It_2$. Uniaxial and biaxial strain improve the ESD robustness up to 20 % and 44 %, respectively. Moreover, for devices with uniaxial strain the failure can be attributed to

dislocations at the drain side, triggered by the interplay between the local thermal ESD stress and the residual mechanical stress induced by the SiN capping layer.

*ESD robustness of FinFET*

The ESD performance of grounded-gate MOS devices and gated diodes, implemented in both SOI and bulk FinFET technologies has been studied. Compared to planar bulk technologies, a layout width efficiency of 37 % and 11 % for NMOS bulk FinFET and SOI bulk FinFET, respectively, was measured. The influence of various geometrical parameters on the ESD robustness has been studied. For grounded-gate NMOS, different gate-length dependencies between the two technologies (SOI vs. bulk) and strongly improved ESD robustness, up to 2.5x, were observed. Bulk FinFET gated diodes have been demonstrated to have quite larger ESD robustness, up to 9x, compared to SOI FinFET diodes. Despite the quite remarkable improvement in ESD robustness observed for narrow-fin bulk FinFET diodes, narrow and wide-fin bulk FinFET diodes have similar ESD-RF performance, which are comparable to the best SOI FinFET diodes. The ESD performance was found also to strongly depend on the different process options. The use of strained SiN layers is found to improve the ESD robustness of gated SOI FinFET diodes and SOI FinFETs in MOS-diode mode up to 15 % by reducing the power dissipation. For SOI FinFETs in bipolar mode, an improvement up to 30 % was measured and attributed to reduced power dissipation and improved failure uniformity.

*Microdose effects on Ultrathin Body SOI*

Some interesting changes were observed in how modern devices manufactured on SOI wafers and with strain-inducing techniques respond to heavy-ion strikes and subsequent electrical stresses: lack of early breakdown due to the very thin gate oxide (1.5 nm), and varying impact on the long-term degradation kinetics depending on the adopted technological solutions. Even though radiation-induced changes are modest, the permanent or semi-permanent damage from heavy-ion strikes must be constantly monitored, because of a very strong dependence on the manufacturing technology.

*Microdose effects on FinFET*

Heavy-ion strikes in state-of-the-art SOI FinFETs featuring high-k gate oxide may have measurable permanent effects, due to microdose in the buried oxide, breakdown of the gate oxide, or interface state generation in the top oxide/body and side oxide/body interfaces. In contrast with the reassuring data taken during SEGR experiments on large capacitors using high-k dielectrics, these multigate devices show that the soft rupture of the gate oxide may be a considerable concern, not only for the increase in gate leakage, but also for the effects on the DC characteristics. Heavy ions can induce permanent damage on FinFETs with large statistical spread. The distribution of the inverse of the gate leakage currents and of the threshold voltage shifts was shown to follow a Weibull

distribution. Moreover, the reciprocal of the gate leakage current was demonstrated to not respect the Poisson area scaling. A new model for the gate leakage current has been proposed. The size of the heavy-ion damage has been estimated of about 30 nm and a higher defect generation takes place in the sidewall gate oxide. Further scaling down of multi-gate technology may lead to even more dramatic scenarios. Long term effects impacting the device wear-out have been considered. Heavy-ion strikes impact both on the degradation kinetics and on the time to breakdown under constant voltage stress.

*Dose Enhancement due to Interconnects*

The presence of metal-1 tracks in the proximity of the device active areas may significantly modify the response to X-rays of deep-submicron CMOS technologies. Dose enhancement in deep-submicron devices must be carefully considered when X-ray facilities are used to perform total-dose tests, due to the strong impact that metal 1 interconnects, especially when made of copper, can have on the final results.

## 9.2 Recommendations for Future Research

At the end of this Ph.D., I would like to make some recommendations for future research in this field.

1. The ESD performance evaluation performed in this thesis on Ultrathin Body and FinFET devices needs to be further expanded. Some items are still open regarding the impact on area efficiency by folding of the multi-finger transistors, the transient behavior, the different failure mechanisms. For the latter, failure analysis should provide clear answers. Future work to study the turn-on and failure of UTB SOI and FinFET devices is planned using Scanning Electron Microscope (SEM) and Transient Interferometric Mapping (TIM). Such analysis techniques will be also used to investigate the failure mechanism occurring in such devices during CDM stress. In such time domain mechanical stress can be triggered by thee interplay between the ESD stress and the residual mechanical stress induced by the process (e.g. strain or source/drain vias and metal layers).
2. In this thesis, FinFET devices are fabricated with landing pad. However, the landing pad has been demonstrated to not be fully used during the current conduction. Future work to investigate the ESD robustness and the ESD-RF performance of FinFETs with different layout of the landing pad (i.e. no landing pad) is planned.
3. Throughout this thesis, a deeper insight into the microdose effects on ultrathin body SOI and SOI FinFET has been presented. However, a lot of research can be done in this field to study the synergy between microdose

and electrical stresses (such as ESD, BTI, and hot carriers) and to include into the new statistical model the angular dependence, also taking into account grazing angles, LET fluctuations, and ions with a range of LETs and energies, and different size of the ion track, depending on the position of the ion strike (i.e., sidewall gate oxide vs. top gate oxide) and the number of multiple hits close to the same damaged region.

## 9.3 Outlook

To conclude this thesis, a brief outlook for future ESD and radiation research is given. Due to an explosively growing number of technology options, tremendous challenges are posed to the ESD protection and radiation communities.

Besides novel device architectures such as 3D-FinFET devices, also new materials may be used to continue down Moore's road. New high mobility channels such as germanium and III-V compounds may be needed for future device generations.

In general, ESD protection and ionizing radiation effects for/on high-voltage and analog technologies still holds a lot of challenges.

Further, the study of the reliability and failure mechanisms of Micro Electro-Mechanical System (MEMS) actuators under ESD stress and ionizing radiation has received increasing attention in recent times. RF-MEMS ohmic and capacitive switches have also been shown to have serious reliability problems both under DC and ESD stress [Tazzoli07] and total dose radiation [Tazzoli09].

Carbon Nano Tubes (CNT) and graphene nanoribbons are currently being researched since they have many properties, from their unique dimensions (a diameter close to 1 nm, while their length can be up to 1000 times longer) to an unusual current conduction mechanism, that make them ideal components for electrical circuits. Few ESD and radiation results have been published so far [Chen09] [Allada].

3D integration seems promising for system integration with applications ranging from electronics for consumer, automotive, and medical applications. During the stacking process, CDM-like discharge events could occur from die to die and therefore adequate ESD protection would be required. Due to increased interconnect resistances across the different dies, novel ESD protection strategies might be required. Regarding ionizing radiations, long-term and transient effects could strongly depend on the transport of the incident radiation through any materials or structures that surround the sensitive circuitry and on the energy deposition in the electronic materials by the impinging radiation.

Other exciting new technology developments include biosensors, neurons-on-chip, plastic and organic electronics, etc. Little or nothing is known how these technologies behave under ESD stress conditions [Jeon02] and ionizing radiations. Therefore, there are many unexplored ESD and radiation problems which are waiting for new solutions.

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