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Analysis on boundary conditions of soft switching for DC electric spring with parallel topology

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Abstract

The concept of DC electric spring (DCES) has been introduced some years ago to solve the voltage stabilisation issue caused by the high penetration of intermittent renewable energy sources (RESs) into DC power systems. Recently, a featured DCES topology has been proposed, comprising an isolated three-port DC/DC converter and an embedded energy storage system. The three ports are connected to a DC power system at the supply side, the critical load (CL) and the non-critical load (NCL) at the user side, whilst the energy storage system is paralleled at the CL port. To improve the performance of the topology, this paper investigates the chance of making soft the switching of the DCES converters. After the DCES operation is analysed, equations describing the currents transients during switching have been worked out, from which the boundary conditions for zero-voltage switching (ZVS) to occur are formulated and the resultant ZVS zone is illustrated with the help of visual graphs. The boundary conditions are examined to evaluate how the circuit parameters influence the extension of the ZVS zone. The examination shows that a suitable selection of the parameters widens the ZVS zone notably; its optimal extension is then found for a case study. The effectiveness of the ZVS findings for the featured DCES topology is validated by both simulation and experiment results.

1 | INTRODUCTION

Electric spring (ES) is a user-level technique proposed in [1] to match the power demand with the power generation in distribution networks with high penetration of intermittent renewable energy sources (RESs). The technique was initially applied to the AC power systems and, at a later time, to the DC ones. To distinguish between the two applications, ESs are designated with alternating current electric springs (ACESs) and DCESs, respectively [1, 2]. Hereafter, DCESs are considered.

Based on the ES concept, the user loads of a DC power system are sorted into two groups termed critical load (CL) and non-critical load (NCL), according to the variations of the supply voltage that they tolerate without their service being deteriorated; in particular, the requirements for the supply voltage range of CLs are much tighter than for NCLs. To stabilise the CL voltage in presence of fluctuations of the DC power system, the DCESs transfer a portion of them to NCL while the remaining portion is borne by a battery. Notice that resorting to a battery, even if for a partial transfer of the power fluctuations, enables the setup of an energy storage system at the user level [3].

To avoid the series connection of NCL and ES [3–5], a featured DCES topology has been proposed in a recent paper [6]. The topology, which comprises an isolated DC/DC three-port converter (TPC) [7] and an energy storage system, has one port connected to a DC power system with RESs and the other two ports connected to NCL and CL, separately. The energy storage system, in turn, is built up around a bi-directional buck-boost converter (BBC) [8] and a battery bank and is connected in parallel to the CL port. It is designed to stabilise the CL supply voltage while allowing the state-of-charge of the battery to vary within settled limits.

Compared to the DCES of series-type in [3], the one in [6] utilises pure DC/DC converters, thus eliminating the need of using bulky filters. Compared to DCESs based on three DC/DC converters [4], it utilises fewer power converters, which simplifies the control system. Furthermore, it keeps CL and

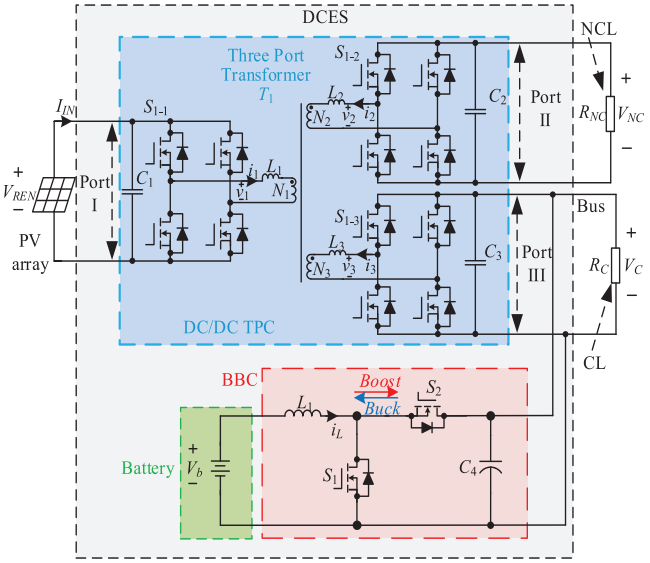


FIGURE 1 DC electric spring (DCES) topology in [6]

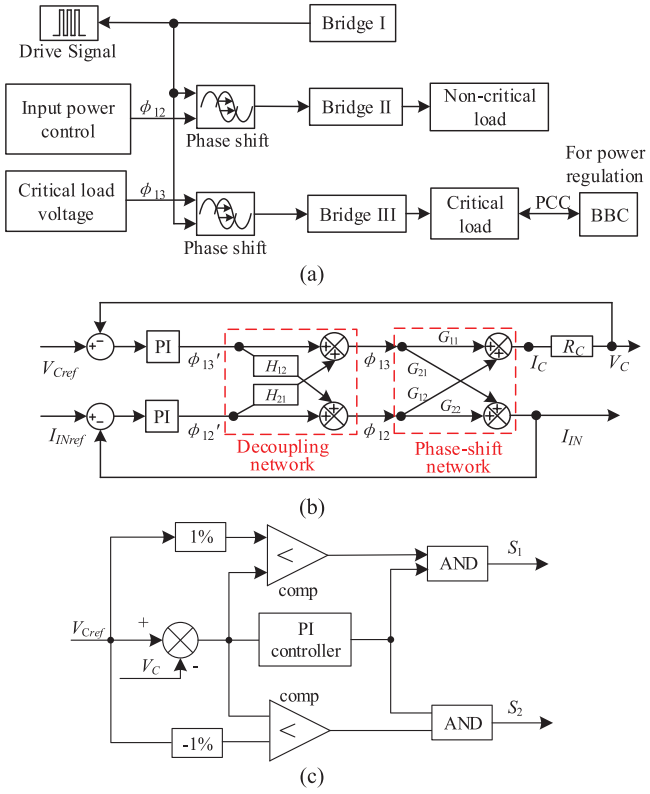


FIGURE 2 DCES control system diagram: (a) DCES control diagram, (b) three-port DC/DC converter (TPC) control diagram, (c) buck-boost converter (BBC) control diagram

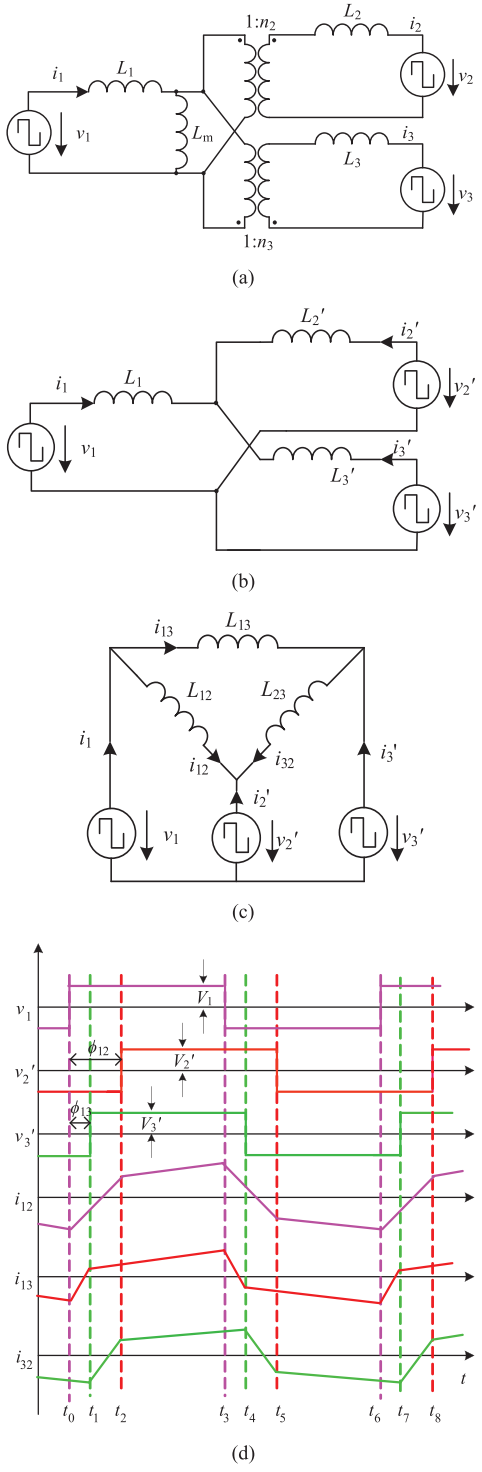


FIGURE 3 Equivalent circuit of the three-port converter: (a) Equivalent circuit of DC/DC TPC, (b) equivalent circuit at primary side, (c) Δ-type equivalent circuit at primary side, (d) ideal voltage and current waveforms of the Δ-type equivalent circuit

NCL isolated from each other but both paralleled to a DC bus, which is consistent with the type of connection traditionally used in DC power systems.

Operation and soft switching of the converters embedded in a DCES are extensively discussed in the literature [9–16]. Regarding the operation, reference [9] reports on the voltage-current waveforms and the control of the dual active bridges (DABs) in an exhaustive way.

Regarding zero-voltage switching (ZVS), reference [10] is concerned with the modulation strategies and soft-switching techniques for DABs. Thanks to the use of the single-active-

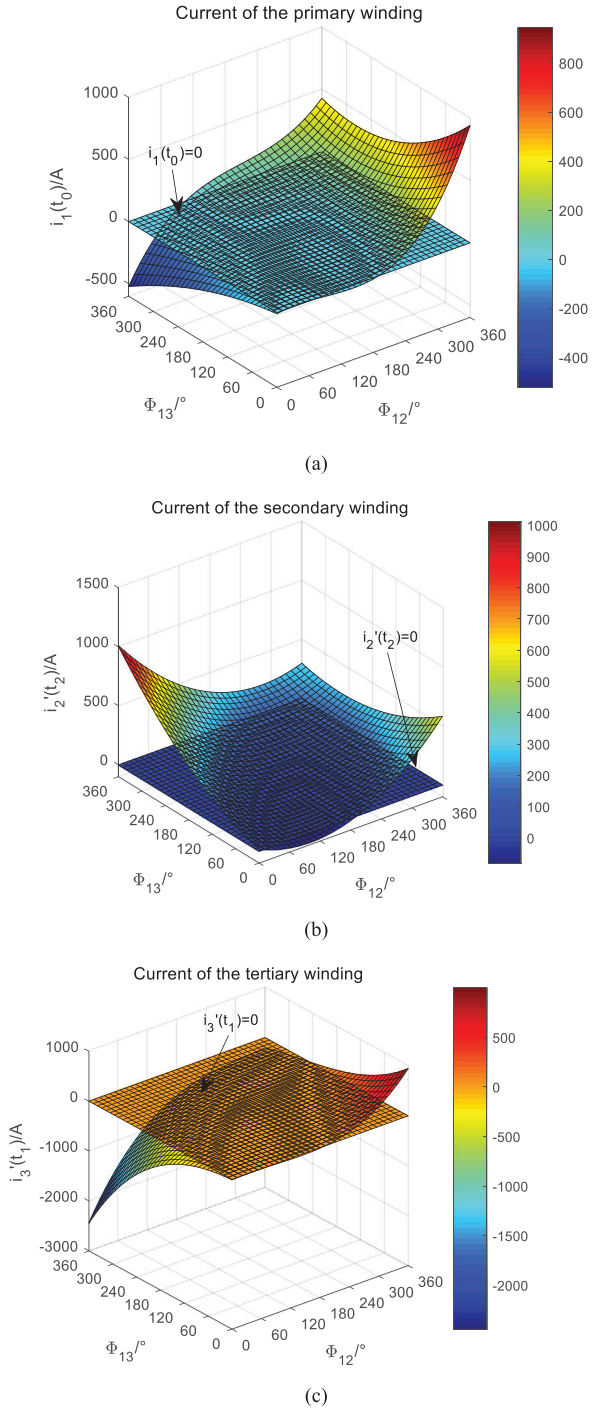


FIGURE 4 Surface of winding currents at turn on of switches $S_{1\text{-}1}$, $S_{1\text{-}2}$, $S_{1\text{-}3}$ versus phase-shift angles: (a) Surface of primary current, (b) surface of secondary current, (c) surface of tertiary current

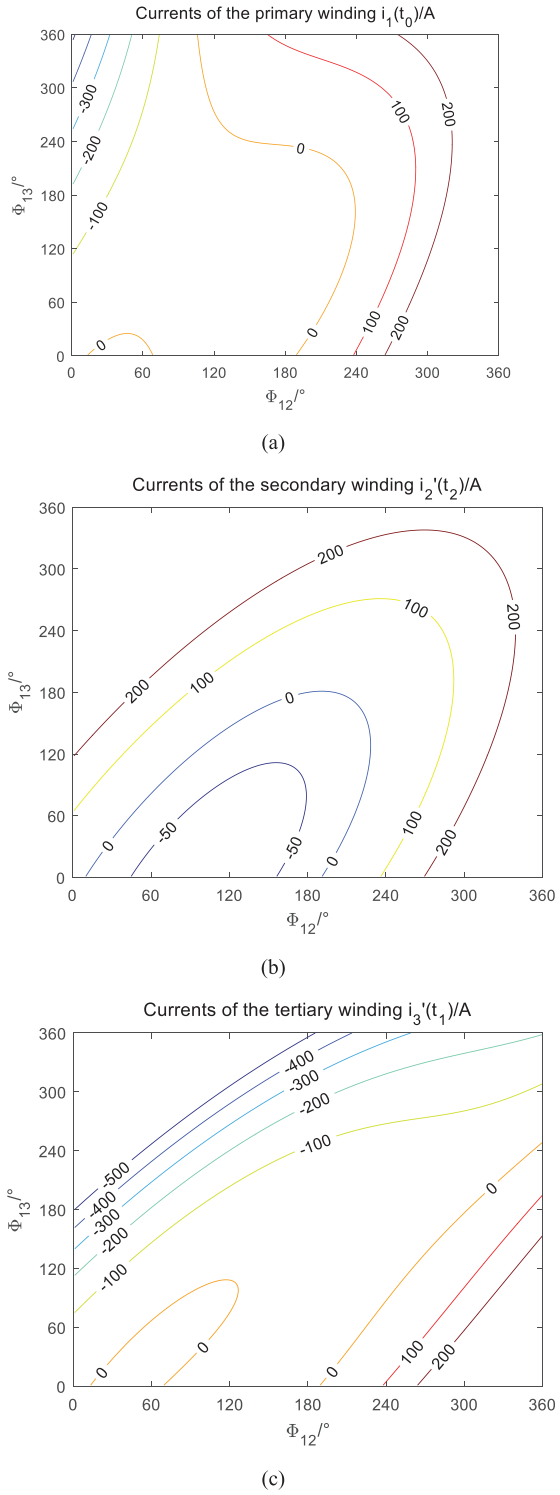


FIGURE 5 Contour line of winding currents at turn on of switches $S_{1\text{-}1}$, $S_{1\text{-}2}$, $S_{1\text{-}3}$ versus phase-shift angles: (a) Contour line of primary current, (b) contour line of secondary current, (c) contour line of tertiary current

bridge modulation, the ZVS region of the DAB topology is extended over a wide input/output voltage range.

Reference [11] presents a detailed analysis of the ZVS operation of three-level DABs controlled with the phase-shift strategy under different voltage conversion ratios. Reference [12] introduces a ZVS technique for full-bridge DC-DC converters controlled with PWM, whereas ZVS operation is met for different input and output conditions. However, both papers do not discuss how the DCES operation modes and circuit parameters impact the achievement of the ZVS operation.

Reference [13] proposes a ZVS half-bridge bi-directional three-port converter. Besides, the soft switching is implemented by the snubber capacitor and transformer leakage inductance. However, the ZVS zone is not discussed when the port voltage

TABLE 1 Parameters of DC electric spring

Parameter	Values
Input voltage (V_1)	48 V
Nominal value of non-critical load (NCL) voltage (V_2)	120 V
Reference value of critical load (CL) voltage (V_{3ref})	120 V
Turns ratio of T_1	2:5:5
Leakage inductance	$L_1 = 45\ \mu$H
	$L_2 = 280\ \mu$H
	$L_3 = 280\ \mu$H
Switching frequency	$f_s = 20$ kHz
Resistance of the CL (R_C)	150 Ω
Resistance of the NCL (R_{NC})	150 Ω

varies within a wide range. In reference [14], an isolated TPC is projected, its phase-shift control and duty-cycle control are discussed, and the dynamic analysis of the converter and the associated control are developed. However, the soft switching of the three-port converter is not analysed in this paper. In reference [15], a duty-ratio control method has been proposed for the DAB and TPC converters when the input voltage varies over a wide range. By adjusting the duty ratio of the voltage, ZVS conditions are achieved over the full operating range. However, no boundary condition or equation of the ZVS is given for the guidance of duty-ratio adjustment of TPC.

The ZVS capabilities of TPCs without auxiliary circuits are studied in [16] over a broad operating situations. The ZVS conditions are expressed in terms of power flow but no search is carried out on the extension of the ZVS zone and its possible enlargement.

This paper performs a thorough analysis of the soft-switching capabilities of the featured DCES topology. In detail, it inspects the occurrence of the ZVS operation and sets the boundary conditions for ZVS to occur and formulates the extension of the ZVS zone in terms of circuit parameters. As a final task, it optimises the ZVS zone extension by an appropriate selection of the circuit parameters for a case study. The organisation of the paper is as follows. Section 2 reviews the structure and operation of the featured DCES topology. Section 3 analyses the ZVS operation of the DCES converters and evaluates the influence of the circuit parameters on the ZVS zone extension. Sections 4 and 5 validate the results of the analysis by simulation and experimentation, respectively. Section 6 concludes the paper.

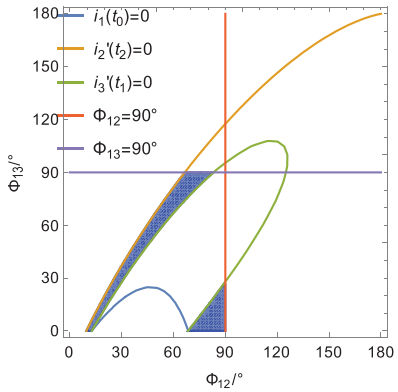


FIGURE 6 Zero-voltage switching (ZVS) zone versus phase-shift angles

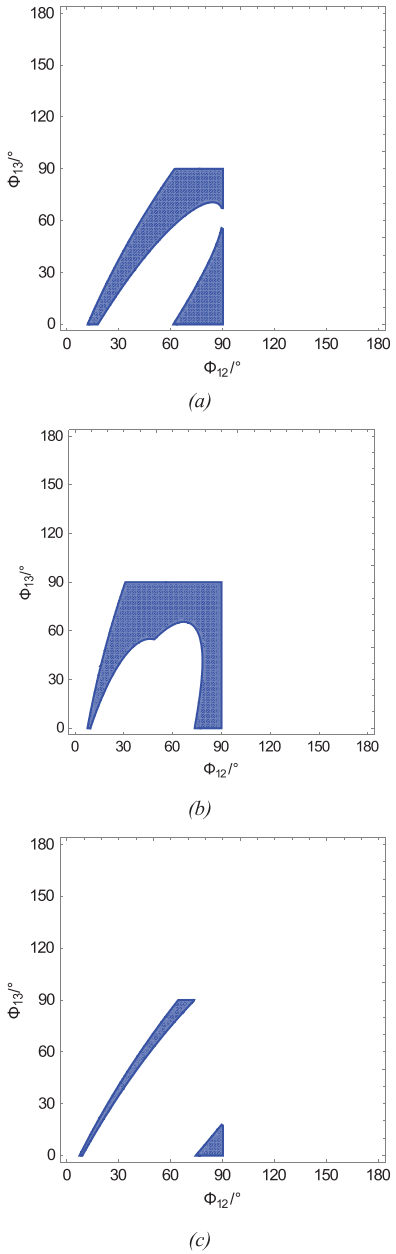
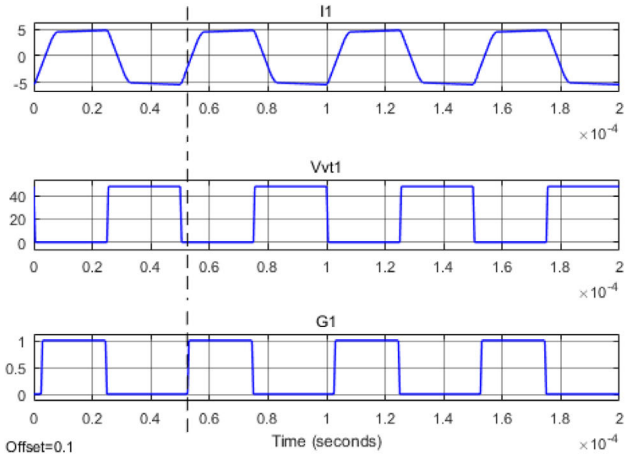


FIGURE 7 ZVS zone with different circuit parameters: (a) ZVS zone for $L_1 = 45\ \mu$H, $L_2 = L_3 = 375\ \mu$H, $R_2 = R_3 = 150\ \Omega$, (b) ZVS zone for $L_1 = 10\ \mu$H, $L_2 = L_3 = 280\ \mu$H, $R_2 = R_3 = 150\ \Omega$, (c) ZVS zone for $L_1 = 45\ \mu$H, $L_2 = L_3 = 280\ \mu$H, $R_2 = R_3 = 200\ \Omega$

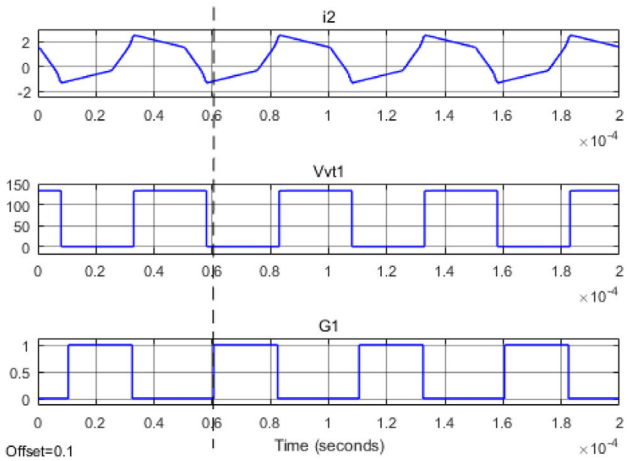
2 | FEATURED DCES TOPOLOGY

2.1 | DCES structure

The structure of the featured DCES topology is shown within the outer dashed line of Figure 1 [7]. Its main sections are the



(a)



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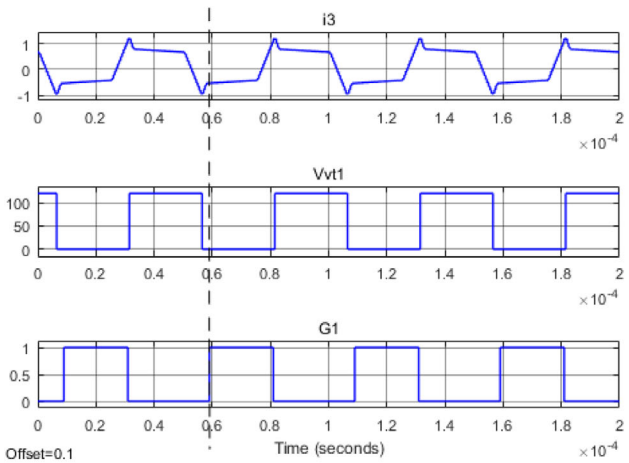
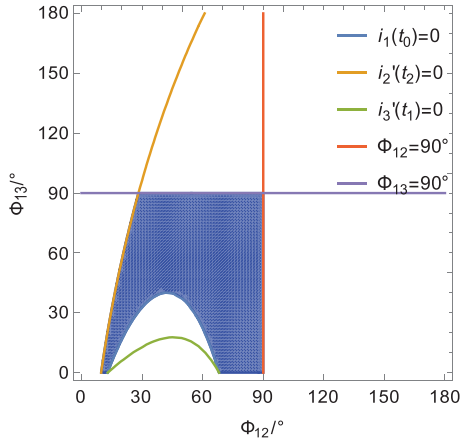


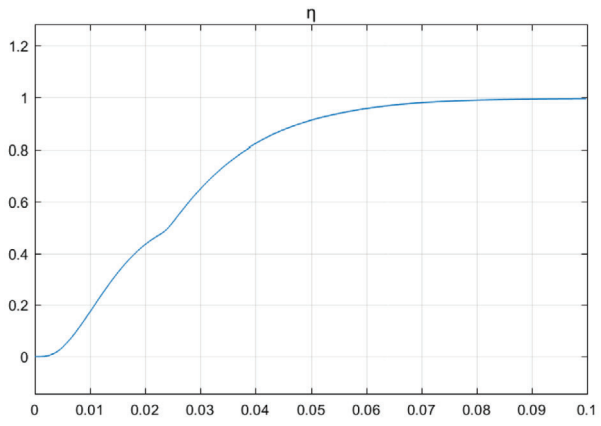
(c)

FIGURE 8 Winding current, voltage and gate signal of switches $S_{1\text{-}1}$, $S_{1\text{-}2}$, $S_{1\text{-}3}$ of the three H-bridges for: (a) Port I, (b) port II, (c) port III

isolated DC/DC TPC and the energy storage system and are shown within the dashed upper and lower lines, respectively. The isolated DC/DC TPC uses full H-bridges at each port, whereas input port I is fed by a DC power system with intermittent RESs, whilst output port II supplies NCL and output port III supplies CL. The ports are linked together by help of a high-



(a)



(b)

FIGURE 9 ZVS operation is realised with circuit parameters: $L_1 = 10$ μH, $L_2 = L_3 = 375$ μH, $R_2 = R_3 = 150$ Ω: (a) ZVS zone, (b) efficiency curve

frequency three-winding transformer. The difference between a conventional isolated TPC-based DCES and that of Figure 1 lies in the insertion of the energy storage system in parallel to CL at port III. Such a system is interfaced to the battery with a boost DC/DC converter, modified to support the bi-directional power flow. In Figure 1, the DC power system is represented by a photovoltaic (PV) array, and this arrangement is utilised as case of study in the paper.

2.2 | DCES operation

According to the working state of the battery, DCES operates according to three operating modes: Battery-balancing, battery-discharging and battery-charging modes.

In battery-balanced mode (mode #1), RES generates enough power to keep the CL voltage regulated at the settled value, and the RES power fluctuations are forced to flow into NCL. In operating mode #1, the battery does not exchange any power and the power generated from RES is drawn by CL, which is supplied at nominal voltage, and NCL.

In battery-discharging mode (mode #2), RES does not generate enough power to supply CL at nominal voltage, even if the

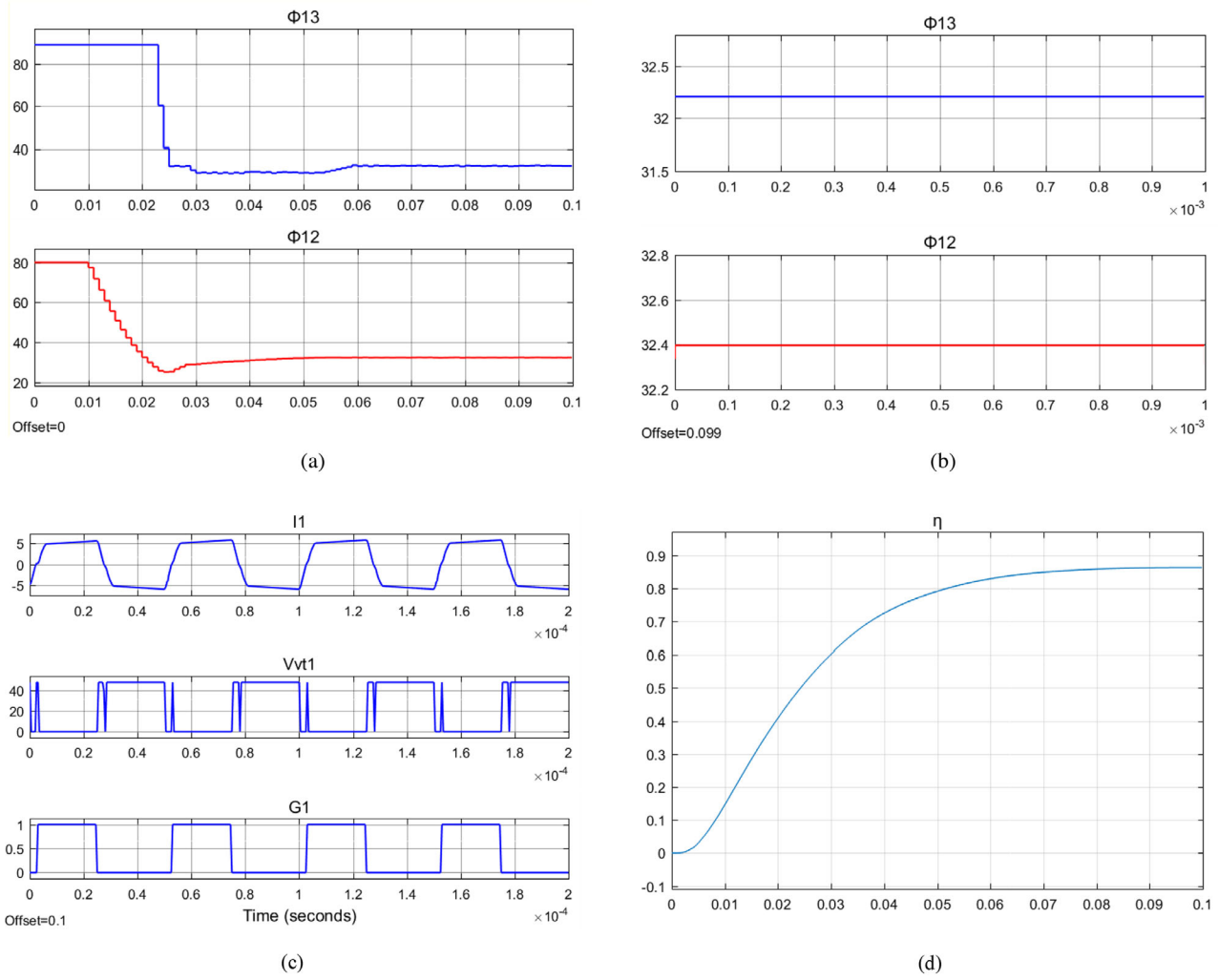


FIGURE 10 ZVS operation is lost for circuit parameters: $L_1 = 10\,\mu$H, $L_2 = L_3 = 375\,\mu$H, $R_2 = R_3 = 150\,\Omega$: (a) Phase-shift angle change, (b) phase-shift angle at steady state, (c) port I waveforms of winding current, and voltage and gate signal of switch $S_{1\text{-}1}$, (d) efficiency curve

NCL voltage is reduced to draw less power than the appointed one. In operating mode #2, the battery is discharged and delivers the deficit of power to CL so as to maintain it supplied at nominal voltage.

In battery-charging mode (mode #3), the power generated by RES exceeds both CL and NCL consumptions despite NCL drawing more power than the appointed one. In operating mode #3, the battery is charged and the storage of the in-excess energy in the battery helps to maintain the CL voltage at nominal value.

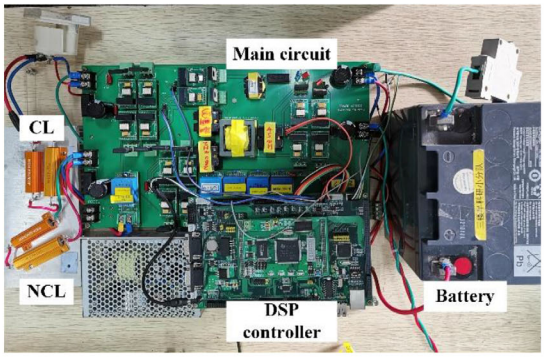
3 | SOFT-SWITCHING ANALYSIS

3.1 | DCES control

The diagram of the DCES control system is shown in Figure 2(a); it exerts two control actions, one on TPC and the other one on BBC [7]. The TPC control, in turn, incorporates two networks: Decoupling network and phase-shift network that are instrumental in the accurate and coordinate operation of DCES. The diagram of the TPC control is illustrated in Figure 2(b), where H_{12} and H_{21} are the elements of decoupling matrix **H**, G_{11}, G_{12}, G_{21}, and G_{22} are the elements of relationship matrix **G** between current and phase angles. Matrix **H** and **G** are explicated in [7].

The conventional phase-shift technique is adopted for the TPC control and is aimed at properly adjusting the power flow from RES to both CL and NCL. The signals driving the H-bridges have phase-shift angles ϕ_{12} and ϕ_{13} between ports I and II and between ports I and III, respectively. They are obtained by manipulating the outputs ϕ_{12}' and ϕ_{13}' of the loop proportional integral (PI) regulators through the decoupling network. The adjustment of the power flows enables the regulation of the CL voltage at the settled value.

To avoid that the BBC switches S_1 and S_2 is turned on at the same time, and an intermediate idle state is introduced when BBC is requested to change from buck to boost mode and vice versa. This is attained by imposing a threshold of 1% of V_{Cref} for the change of mode to take place. Therefore, the BBC operates in buck mode when V_C goes beyond V_{Cref} of the threshold, operates in boost mode when the V_C goes below V_{Cref} of the



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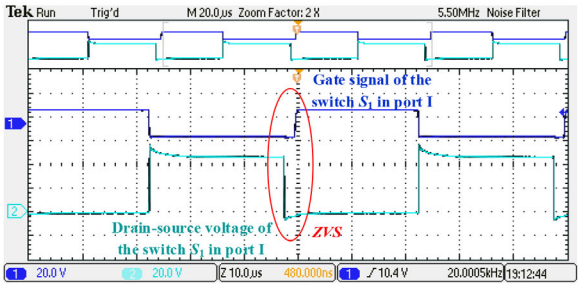

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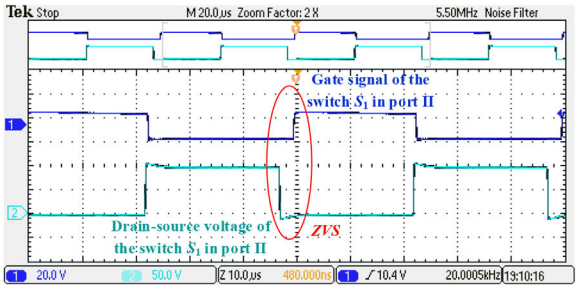

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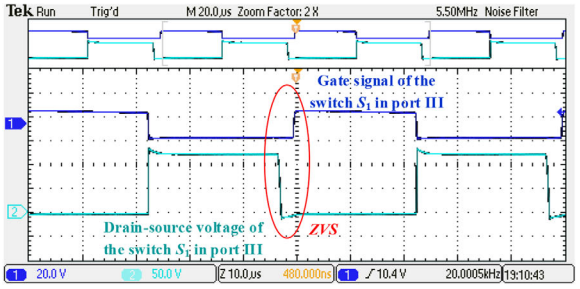
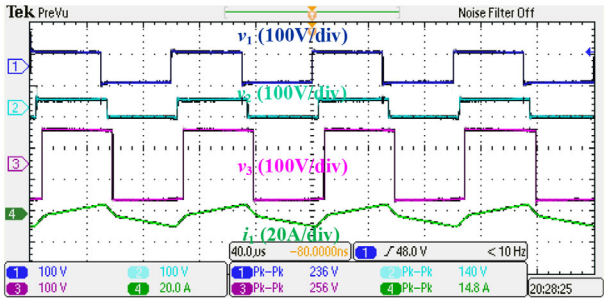


d

FIGURE 11 Experimental setup and waveforms of the DCES: (a) Experimental setup of the DCES, (b) waveforms of voltage and gate signal of switch $S_{1\text{-}1}$ for port I, (c) waveforms of voltage and gate signal of switch $S_{1\text{-}2}$ for port I, (d) waveforms of voltage and gate signal of switch $S_{1\text{-}3}$ for port III

threshold, and stays in the idle state when V_C differs from V_{Cref} less than the threshold. The resulting BBC control diagram is illustrated in Figure 2(c). As the diagram underlines, the signals driving the BBC switches, also denoted with S_1 and S_2, are synthesised by digital calculation using logic ports 'AND' and a PI controller.

Circuital modelling of an isolated DC/DC TPC with DABs yields the well-known equivalent circuit of Figure 3(a) [16, 17]. In the circuit, inductance L_m is the magnetising inductance of the primary winding, inductances L_1, L_2 and L_3 are, respectively, the leakage inductances of the primary, secondary and tertiary windings, and voltages v_1, v_2, and v_3 are the midpoint voltages of three H-bridges. The equivalent circuit with secondary and tertiary windings referred to the primary and with the *Y*-Δ transformation are drawn in Figures 3(b) and (c), where the magnetising inductance is neglected because of the much bigger than the downstream impedances. The expressions of the referred-to-primary leakage inductances and voltages are given in Equation (1) [6] and those of the leakage inductances for the Δ-type circuit in Equation (2):



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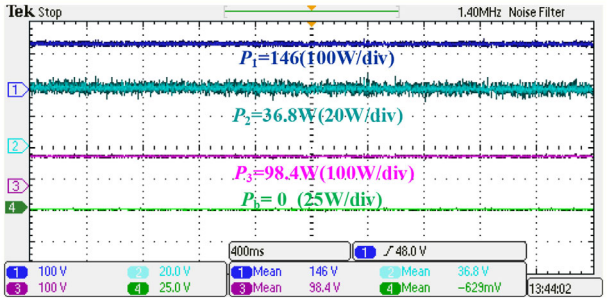

b

FIGURE 12 Experiment results: (a) midpoint voltage and primary side current of the transformer, (b) power flow

$$\begin{cases} L_2' = \dfrac{L_2 N_1^2}{N_2^2} == \dfrac{L_2}{n_2^2} \\ L_3' = \dfrac{L_3 N_1^2}{N_3^2} = \dfrac{L_3}{n_3^2} \\ v_2' = \dfrac{v_2 N_1}{N_2} = \dfrac{v_2}{n_2} \\ v_3' = \dfrac{v_3 N_1}{N_3} = \dfrac{v_3}{n_3} \end{cases} \tag{1}$$

$$\begin{cases} L_{12} = L_1 + L_2' + L_1 L_2' / L_3' \\ L_{23} = L_2' + L_3' + L_2' L_3' / L_1 \\ L_{13} = L_1 + L_3' + L_1 L_3' / L_2' \end{cases} \tag{2}$$

Waveforms of voltages and current in the Δ-type circuit are illustrated in Figure 3(d), where V_1 denotes the DC voltage of port I, and V_2' and V_3' denote the DC voltages of ports II and III referred to the primary [19].

Each of the port pairs of the isolated DC/DC TPC can be regarded as a DAB [10, 18]. Therefore, the equations of the

power flows can be obtained by applying the superposition principle, leading to [20, 21]

$$\begin{cases} P_{12} = \dfrac{V_1 V_2'}{2\pi f_s L_{12}} \varphi_{12} \left(1 - \dfrac{\varphi_{12}}{\pi}\right) \\ P_{13} = \dfrac{V_1 V_3'}{2\pi f_s L_{13}} \varphi_{13} \left(1 - \dfrac{\varphi_{13}}{\pi}\right) \\ P_{32} = \dfrac{V_2' V_3'}{2\pi f_s L_{23}} \varphi_{32} \left(1 - \dfrac{\varphi_{32}}{\pi}\right) \\ = \dfrac{V_2' V_3'}{2\pi f_s L_{23}} (\varphi_{12} - \varphi_{13}) \left(1 - \dfrac{\varphi_{12} - \varphi_{13}}{\pi}\right) \end{cases} \tag{3}$$

where P_{12}, P_{13} and P_{32} designate the power flows from ports I to II, from ports I to III and from ports III to II, respectively, and f_s is the switching frequency. It is worth to notice that the power flows are determined by the phase-shift angle between the related two ports.

By Equation (3), the power flows P_1, P_2 and P_3 at the ports of the circuit in Figure 3(a) can be written as

$$\begin{cases} P_1 = P_{12} + P_{13} \\ \quad = \dfrac{V_1 V_2'}{2\pi f_s L_{12}} \varphi_{12} \left(1 - \dfrac{\varphi_{12}}{\pi}\right) + \dfrac{V_1 V_3'}{2\pi f_s L_{13}} \varphi_{13} \left(1 - \dfrac{\varphi_{13}}{\pi}\right) \\ P_2 = P_{12} + P_{32} \\ \quad = \dfrac{V_1 V_2'}{2\pi f_s L_{12}} \varphi_{12} \left(1 - \dfrac{\varphi_{12}}{\pi}\right) + \dfrac{V_2' V_3'}{2\pi f_s L_{23}} (\varphi_{12} - \varphi_{13}) \\ \left(1 - \dfrac{\varphi_{12} - \varphi_{13}}{\pi}\right) \\ P_3 = P_{13} - P_{32} \\ \quad = \dfrac{V_1 V_3'}{2\pi f_s L_{13}} \varphi_{13} \left(1 - \dfrac{\varphi_{13}}{\pi}\right) - \dfrac{V_2' V_3'}{2\pi f_s L_{23}} \\ (\varphi_{12} - \varphi_{13}) \left(1 - \dfrac{\varphi_{12} - \varphi_{13}}{\pi}\right) \end{cases} \tag{4}$$

3.2 | ZVS analysis

Since the battery-balanced mode is the main operation mode of DCES, the ZVS analysis focuses on the switching of TPC. If the current in a leg flows through the anti-paralleled body diode of the switch, the latter can turn on at zero voltage since the conduction of the diode clamps the voltage across the switch to zero. Therefore, the ZVS of the switches depends on whether the leg current flows through the anti-paralleled body diode at or just before the switching instants.

According to Figures 3(a) and (d), the currents in the three windings of TPC are given by

$$\begin{cases} i_1(t) = i_{12}(t) + i_{13}(t) \\ i_2'(t) = -i_{12}(t) - i_{32}(t) \\ i_3'(t) = -i_{13}(t) + i_{32}(t) \end{cases} \tag{5}$$

Being the current of four switches that are symmetrical and having the four switches in the three H-bridges with a similar behaviour at turn-on, switches $S_{1\text{-}1}$, $S_{1\text{-}2}$, $S_{1\text{-}3}$ of the three H-bridges are taken as an example. At the turn on of switches $S_{1\text{-}1}$, $S_{1\text{-}2}$, or $S_{1\text{-}3}$, the currents are negative before the switch is turned on if they flow into the anti-paralleled body diodes of the switches [22]. Therefore, ZVS is imposed in all switches of the H-bridges if all winding currents at the midpoint of the voltage rising edge, denoted with $i_1(t_0)$, $i_2'(t_2)$ and $i_3'(t_1)$, are negative [16], that is, it must be

$$\begin{cases} i_1(t_0) = i_{12}(t_0) + i_{13}(t_0) < 0 \\ i_2'(t_2) = -i_{12}(t_2) - i_{32}(t_2) < 0 \\ i_3'(t_1) = -i_{13}(t_1) + i_{32}(t_1) < 0 \end{cases} \tag{6}$$

Using Figures 3(c) and (d), currents i_{12}, i_{13} and i_{32} in Equation (6) are expressed as follows:

$$\begin{cases} i_{12}(t) = \begin{cases} i_{12}(t_0) + \dfrac{V_1 + V_2'}{L_{12}} (t - t_0) & t_0 \le t < t_2 \\ i_{12}(t_2) + \dfrac{V_1 - V_2'}{L_{12}} (t - t_2) & t_2 \le t < t_3 \end{cases} \\ i_{13}(t) = \begin{cases} i_{13}(t_0) + \dfrac{V_1 + V_3'}{L_{13}} (t - t_0) & t_0 \le t < t_1 \\ i_{13}(t_1) + \dfrac{V_1 - V_3'}{L_{13}} (t - t_1) & t_1 \le t < t_3 \end{cases} \\ i_{32}(t) = \begin{cases} i_{32}(t_1) + \dfrac{V_3' + V_2'}{L_{23}} (t - t_1) & t_1 \le t < t_2 \\ i_{32}(t_2) + \dfrac{V_3' - V_2'}{L_{23}} (t - t_2) & t_2 \le t < t_4 \end{cases} \end{cases} \tag{7}$$

At steady state, the average value of the winding currents in a switching cycle is zero and their waveform is symmetric, then it is

$$\begin{cases} i_{12}(t_0) = -i_{12}(t_3) \\ i_{13}(t_0) = -i_{13}(t_3) \\ i_{32}(t_0) = -i_{32}(t_3) \end{cases} \tag{8}$$

By combining Equations (7) and (8), the winding currents at t_0, t_1 and t_2 are calculated in

$$\begin{cases} i_{12}(t_0) = \dfrac{\pi V_2' - \pi V_1 - 2V_2' \varphi_{12}}{4\pi L_{12} f_s} \\ i_{12}(t_2) = \dfrac{\pi V_2' - \pi V_1 + 2V_1 \varphi_{12}}{4\pi L_{12} f_s} \\ i_{13}(t_0) = \dfrac{\pi V_3' - \pi V_1 - 2V_3' \varphi_{13}}{4\pi L_{13} f_s} \\ i_{13}(t_1) = \dfrac{\pi V_3' - \pi V_1 + 2V_1 \varphi_{13}}{4\pi L_{13} f_s} \\ i_{32}(t_1) = \dfrac{\pi V_2' - \pi V_3' + 2V_2' \varphi_{13} - 2V_2' \varphi_{12}}{4\pi L_{32} f_s} \\ i_{32}(t_2) = \dfrac{\pi V_2' - \pi V_3' + 2V_3' \varphi_{12} - 2V_3' \varphi_{13}}{4\pi L_{32} f_s} \end{cases} \tag{9}$$

Substitution of Equations (9) into (6) yields [23]

$$\begin{cases} i_1(t_0) = i_{12}(t_0) + i_{13}(t_0) \\ \quad = \dfrac{\pi V_2' - \pi V_1 - 2V_2'\varphi_{12}}{4\pi L_{12} f_s} + \dfrac{\pi V_3' - \pi V_1 - 2V_3'\varphi_{13}}{4\pi L_{13} f_s} < 0 \\ i_2'(t_2) = -i_{12}(t_2) - i_{32}(t_2) \\ \quad = \dfrac{\pi V_1 - \pi V_2' - 2V_1\varphi_{12}}{4\pi L_{12} f_s} \\ \qquad - \dfrac{\pi V_2' - \pi V_3' + 2V_3'\varphi_{12} - 2V_3'\varphi_{13}}{4\pi L_{23} f_s} < 0 \\ i_3'(t_1) = -i_{13}(t_1) + i_{32}(t_1) \\ \quad = \dfrac{\pi V_1 - \pi V_3' - 2V_1\varphi_{13}}{4\pi L_{13} f_s} \\ \qquad + \dfrac{\pi V_2' - \pi V_3' + 2V_2'\varphi_{13} - 2V_2'\varphi_{12}}{4\pi L_{23} f_s} < 0 \end{cases} \tag{10}$$

Under DCES voltage stabilising action, CL voltage V_C is kept constant whilst V_{NC} is subjected to variations. By accounting that $V_C = V_3$ and $V_{NC} = V_2$, and by equating the power flow at port II to NCL consumption, we have

$$\begin{aligned} \frac{V_2^2}{R_2} = P_2 = \frac{V_1 V_2}{2\pi f_s L_{12} n_2}\varphi_{12}\left(1 - \frac{\varphi_{12}}{\pi}\right) \\ + \frac{V_2 V_3}{2\pi f_s L_{23} n_2 n_3}(\varphi_{12} - \varphi_{13})\left(1 - \frac{\varphi_{12} - \varphi_{13}}{\pi}\right) \end{aligned} \tag{11}$$

Finally, by Equation (11), voltage V'_2 at port II referred to the primary is formulated as

$$\begin{aligned} V_2' = \frac{V_2}{n_2} = \frac{V_1 R_2}{2\pi f_s L_{12} n_2^2}\varphi_{12}\left(1 - \frac{\varphi_{12}}{\pi}\right) \\ + \frac{V_3 R_2}{2\pi f_s L_{23} n_2^2 n_3}(\varphi_{12} - \varphi_{13})\left(1 - \frac{\varphi_{12} - \varphi_{13}}{\pi}\right) \end{aligned} \tag{12}$$

Substitution of Equations (12) into (10) gives the expressions of the winding currents at the switching instants t_0, t_2 and t_1 as a function of the phase-shift angles $\boldsymbol{\phi}_{12}$ and $\boldsymbol{\phi}_{13}$ and the circuit data. Figures 4(a)–(c) show the surfaces described by $i_1(t_0)$, $i_2'(t_2)$ and $i_3'(t_1)$ along the two axes $\boldsymbol{\phi}_{12}$ and $\boldsymbol{\phi}_{13}$, which point out that only a portion of the surfaces takes negative values, producing ZVS of the respective H-bridge. The ranges of $\boldsymbol{\phi}_{12}$ and $\boldsymbol{\phi}_{13}$ in correspondence of such a portion enable ZVS of that H-bridge. The boundary conditions for ZVS reported in the Appendix are visually represented by the graphs of Figures 5(a)–(c) based on the DCES data listed in Table 1.

ZVS operation of TPC is reached under the concurrent occurrence of ZVS for all TPC H-bridges. To find out this condition, they come useful to trace the contours of $i_1(t_0)$, $i_2'(t_2)$ and $i_3'(t_1)$ as shown in Figures 5(a)–(c). The contours are constituted by the intersection of the surfaces in Figures 4(a)–(c) with planes set at different values of the currents. The contours show that for each winding current, there is an area of the plane $\boldsymbol{\phi}_{12}$–$\boldsymbol{\phi}_{13}$, circumscribed by the curve of zero current, where the current at the switching instant is negative.

The outcomes in Figures 5(a)–(c) are put together in Figure 6 to identify the pairs $\boldsymbol{\phi}_{12}$, $\boldsymbol{\phi}_{13}$ assuring ZVS operation of TPC. As per Figure 6, the pairs must fall within the two shaded areas, here defined as the ZVS zone of TPC. The zone has been limited by the upper value of $\pi/2$ for the phase-shift angles since higher values lead to unduly high peaks of the currents.

The ZVS zone in Figure 6 could be somewhat narrow to maintain ZVS under large variations of the operating conditions of DCES. It is therefore of interest to evaluate the chance of widening the ZVS zone by a proper selection of the DCES data. According to the expressions in the Appendix, the extension of the ZVS zone depends on circuit parameters, switching frequency and turn ratios. Being the latter ones usually fixed by DCES specifications, the evaluation is restricted to the circuit parameters.

3.3 | Circuit parameters against ZVS zone

The influence of the circuit parameters, specifically leakage inductances L_1, L_2 and L_3 and load resistances R_C and R_{NC}, on the ZVS zone is assessed here through the redetermination of its extension by changing one at a time the pair L_2, L_3 then L_1, and finally the pair R_C, R_{NC} with respect to the values used in Figure 6. The results are traced in Figures 7(a)–(c).

In Figure 7(a), both L_2 and L_3 have increased by about 30% and, compared to Figure 6, the extension of the resulting ZVS zone has widened notably. In Figure 7(b), L_1 has decreased by about 75% and the extension of the resulting ZVS zone has widened even further. Last, in Figure 7(c), both R_C and R_{NC} have increased by about 30% and the extension of the resulting ZVS zone has narrowed slightly. Incidentally, it has been verified that if the circuit parameters change in the direction contrary to the ones stated above, the ZVS zone will also change to the opposite direction. It can therefore be concluded that the ZVS zone is greatly influenced by the leakage inductances of the circuit, whereby it is enlarged by an increase of the secondary and tertiary inductances and a decrease of the primary one. Load resistances instead do not influence much the ZVS zone.

4 | SIMULATION RESULTS

The behaviour of a DCES with the topology of Figure 1 has been simulated, using the parameters in Table 1, to check the findings of the ZVS analysis. The steady-state waveforms of the key quantities of the circuit are plotted in Figures 8(a)–(c), which refer respectively to ports I, II, and III. Moreover, each figure has three channels that plot, respectively, the winding current, and the voltage and gate signal of the upper left switch in the three H-bridges.

The waveforms of Figure 8(a) underline that at the turn on of switch $S_{1\text{-}1}$ that happens when its gate signal changes from 0 to 1, the winding current of port I is negative and the voltage across switch $S_{1\text{-}1}$ is zero, confirming that its switching is soft. It can be readily inferred that the same happens for the other three switches of port I. Similarly, Figures 8(b) and (c) confirm the

ZVS of the switches of ports II and III. It can be then asserted that ZVS operation is obtained for the DCES.

Afterwards, a simulation of the DCES behaviour has been run by assigning the following values to the circuit parameters: $L_1 = 10\ \mu$H, $L_2 = L_3 = 375\ \mu$H and $R_2 = R_3 = 150\ \Omega$. The new values produce the ZVS zone of Figure 9(a). The efficiency curve, traced as a function of time, is shown in Figure 9(b) with the circuit parameters when the ZVS operation is realised. The curve points out that the efficiency can reach 99.45% in simulation.

The steady-state waveforms of the key quantities of port I are plotted in Figure 10(b) under the pair ϕ_{12}, ϕ_{13} illustrated in Figure 10(a). The plots show that ZVS operation is lost for the pair ($\phi_{12} = 32.4°$, $\phi_{13} = 32.2°$) at the steady state. The phase-shift angles are regulated automatically with the circuit parameter until the system reaches the steady state. This result matches with Figure 9(a) as the angle values of the pair at the steady state are out of the ZVS zone. The efficiency curve at steady state is traced in Figure 10(d) when ZVS operation is lost and shows that the efficiency is 88%.

5 | EXPERIMENTAL RESULTS

A DCES setup with the topology of Figure 1 and the circuit parameters in Table 1 has been arranged in a laboratory to further validate the ZVS analysis by experiments. An overall picture of the setup is shown in Figure 11(a). The type of MOSFET is RU1Z200Q, whose drain-source on-state resistance is 5.5 mΩ.

The hardware of the DC/DC TPC and BBC is located on a board and includes the isolation-type voltage and current sensors. The input to port I is an adjustable voltage source emulating a PV array whilst standard resistors are connected to the NCL and CL DC buses of port II and III of the DCES, respectively. The control system of the DCES is implemented in a digital signal processor (DSP) controller based on the TM320F28335.

The results of the experimental tests are reported in Figures 11(b)–(d). Each figure refers to one of the three H-bridges and contains two channels: The upper channel plots the gate signal of the upper left switch, whilst the lower channel plots the voltage across it. The experimental waveforms in Figure 12 indicate that the voltage across the switches is zero when they are turned on by the change of the gate signals from 0 to 1, thus proving the achievement of ZVS operation for TPC also by experiments.

In Figure 12(a), the first three channels record the voltages v_1, v_2, v_3 on the primary, secondary and tertiary sides of the transformer, respectively. The fourth channel records the current i_1 on the primary side of the transformer. From the records, it turns out that the phase-shift angles ϕ_{12} and ϕ_{13} are equal to 20 and 42°, which means that they are within the ZVS zone according to Figure 9(a).

Figure 12(b) gives the records of the output power of the four DCES ports, namely, input power, CL power, NCL power, and power generated by DCES, which are designated as P_1, P_2, P_3 and P_b, respectively. It can be seen that the CL power is kept at about 98 W, which is its rated value. Owing to the fact that ϕ_{12} is much smaller than ϕ_{13}, the NCL works out of its rated state and draws a power of 36.8 W.

6 | CONCLUSION

The paper has investigated the soft switching of a featured topology of DCES, built up around an isolated DC/DC TPC and a bi-directional energy storage. Based on the topology and the control strategy of the DCES, theoretical formulas have been deduced for the ZVS conditions of TPC, the detailed derivation process of which can be seen in the Appendix. The ZVS zone has been found as a function of the phase-shift angles of the H-bridges. Afterwards, the influence of the leakage inductances of the windings and the CL and NCL resistances on the ZVS zone has been evaluated, aimed at a convenient selection of them to widen the ZVS zone. The main outcomes of this evaluation can be summarised as follows: The ZVS zone is notably widened (i) by increasing the leakage inductances of the secondary and tertiary windings, and (ii) by decreasing the leakage inductance of the primary winding; it is also widened but to a lesser extent by increasing the load resistances. Simulation and experimental results have been provided to corroborate the theoretical findings.

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APPENDIX A

$$
\begin{aligned}
i_1(t_0) &= i_{12}(t_0) + i_{13}(t_0) \\
&= \left[-\pi V_1 (L_{12} + L_{13}) + V_2' L_{13} (\pi - 2\Phi_{12}) \right. \\
&\quad \left. + V_3' (\pi - 2\Phi_{13}) L_{12} \right] / 4\pi L_{12} L_{13} f_s \\
&= \left\{ \begin{array}{l} -2\pi^2 f_s L_{12} L_{23} (L_{12} + L_{13}) {n_2}^2 n_3 V_1 \\ \quad + L_{13} \left[V_1 R_2 L_{23} n_3 \Phi_{12} \left(1 - \dfrac{\Phi_{12}}{\pi} \right) \right. \\ \quad \left. + V_3 R_2 L_{12} (\Phi_{12} - \Phi_{13}) \left(1 - \dfrac{\Phi_{12} - \Phi_{13}}{\pi} \right) \right] \\ (\pi - 2\Phi_{12}) \\ \quad + 2\pi f_s {L_{12}}^2 L_{23} {n_2}^2 n_3 V_3' (\pi - 2\Phi_{13}) \end{array} \right\} / \\
&\quad 8\pi^2 {L_{12}}^2 L_{13} L_{23} f_s^2 {n_2}^2 n_3 < 0
\end{aligned} \tag{13}
$$

$$
\begin{aligned}
i_2'(t_2) &= -i_{12}(t_2) - i_{32}(t_2) \\
&= \left[V_1 L_{23} (\pi - 2\Phi_{12}) - \pi V_2' (L_{12} + L_{23}) \right. \\
&\quad \left. - V_3' L_{12} (2\Phi_{12} - 2\Phi_{13} - \pi) \right] / 4\pi L_{12} L_{23} f_s \\
&= \left\{ \begin{array}{l} 2\pi f_s L_{12} {L_{23}}^2 n_2^2 n_3 V_1 (\pi - 2\Phi_{12}) \\ -\pi (L_{12} + L_{23}) \left[V_1 R_2 L_{23} n_3 \Phi_{12} \left(1 - \dfrac{\Phi_{12}}{\pi} \right) \right. \\ \quad \left. + V_3 R_2 L_{12} (\Phi_{12} - \Phi_{13}) \left(1 - \dfrac{\Phi_{12} - \Phi_{13}}{\pi} \right) \right] \\ -2\pi f_s {L_{12}}^2 L_{23} n_2^2 n_3 V_3' (2\Phi_{12} - 2\Phi_{13} - \pi) \end{array} \right\} / \\
&\quad 8\pi^2 {L_{12}}^2 {L_{23}}^2 f_s^2 n_2^2 n_3 < 0
\end{aligned} \tag{14}
$$

$$
\begin{aligned}
i_3'(t_1) &= -i_{13}(t_1) + i_{32}(t_1) \\
&= \left[V_1 L_{23} (\pi - 2\Phi_{13}) + V_2' L_{13} (\pi + 2\Phi_{13} - 2\Phi_{12}) \right. \\
&\quad \left. - \pi V_3' (L_{13} + L_{23}) \right] / 4\pi L_{13} L_{23} f_s \\
&= \left\{ \begin{array}{l} 2\pi f_s L_{12} {L_{23}}^2 n_2^2 n_3 V_1 (\pi - 2\Phi_{13}) \\ \quad + L_{13} \left[V_1 R_2 L_{23} n_3 \varphi_{12} \left(1 - \dfrac{\Phi_{12}}{\pi} \right) \right. \\ \quad \left. + V_3 R_2 L_{12} (\Phi_{12} - \Phi_{13}) \left(1 - \dfrac{\Phi_{12} - \Phi_{13}}{\pi} \right) \right] \\ (\pi + 2\Phi_{13} - 2\Phi_{12}) \\ -2\pi^2 f_s L_{12} L_{23} (L_{13} + L_{23}) n_2^2 n_3 V_3' \end{array} \right\} / \\
&\quad 8\pi^2 L_{12} L_{13} {L_{23}}^2 f_s^2 n_2^2 n_3 < 0
\end{aligned} \tag{15}
$$