Applied Physics Letters

RESEARCH ARTICLE | SEPTEMBER 07 2023

Gate leakage modeling in lateral β-Ga_2O_3 MOSFETs with Al_2O_3 gate dielectric

Manuel Fregolent ; Enrico Brusaterra ; Carlo De Santi ; Kornelius Tetzner ; Joachim Würfl ; Gaudenzio Meneghesso ; Enrico Zanoni ; Matteo Meneghini

Appl. Phys. Lett. 123, 103504 (2023)
https://doi.org/10.1063/5.0154878

Applied Physics Letters ARTICLE pubs.aip.org/aip/apl

Gate leakage modeling in lateral β-Ga_2O_3 MOSFETs with Al_2O_3 gate dielectric

Cite as: Appl. Phys. Lett. **123**, 103504 (2023); doi: 10.1063/5.0154878
Submitted: 16 April 2023 · Accepted: 10 August 2023 ·
Published Online: 7 September 2023

Manuel Fregolent,[1,a)] Enrico Brusaterra,[1,2] Carlo De Santi,[1] Kornelius Tetzner,[2] Joachim Würfl,[2] Gaudenzio Meneghesso,[1,3] Enrico Zanoni,[1] and Matteo Meneghini[1,4]

AFFILIATIONS

[1]Department of Information Engineering, University of Padova, Padova, Italy
[2]Ferdinand-Braun-Institut (FBH), Leibniz-Institut für Höchstfrequenztechnik, Gustav-Kirchhoff-Straße 4, 12489 Berlin, Germany
[3]IUNET - National Interuniversity Consortium for Nanoelectronics, Italy
[4]Department of Physics and Astronomy, University of Padova, Padova, Italy

[a)]Author to whom correspondence should be addressed: manuel.fregolent@dei.unipd.it

ABSTRACT

We present a detailed model of the static and dynamic gate leakage current in lateral β-Ga_2O_3 MOSFETs with an Al_2O_3 gate insulator, covering a wide temperature range. We demonstrate that (i) in the DC regime, current originates from Poole–Frenkel conduction (PFC) in forward bias at high-temperature, while (ii) at low temperature the conduction is dominated by Fowler–Nordheim tunneling. Furthermore, (iii) we modeled the gate current transient during a constant gate stress as effect of electron trapping in deep levels located in the oxide that inhibits the PF conduction mechanism. This hypothesis was supported by a TCAD model that accurately reproduces the experimental results.

Monoclinic gallium oxide (β-Ga_2O_3) transistors and rectifiers are promising devices with perspective application in high-power, high frequency,[1,2] and high efficiency conversion of energy.[3,4] β-Ga_2O_3 transistors are mostly based on lateral or vertical MOS structures,[3,5,6] in which the gate insulator usually consists of aluminum oxide (Al_2O_3).[7–10] Currently, the development of gallium oxide technology is mainly driven to the optimization of the breakdown voltage and ON-resistance of the devices, to fully exploit the theoretical limitation given by the high Baliga Figure of Merit.[11] A full understanding of the gate leakage in Al_2O_3/β-Ga_2O_3 transistors is still missing in the literature; this is of paramount importance because it can be related to many macroscopic effects, such as excess of power consumption, limitation in the gate swing,[12] an increase in the high-frequency noise in RF transistors.[13–17] Moreover, gate leakage was demonstrated to play a fundamental role for the gate reliability in other wide bandgap transistors, such as GaN MOS/MOSFETs,[16,17] GaN HEMTs with p-GaN or MIS gate,[18–20] and SiC MOSFETs.[21]

The goal of this study is to model the static and dynamic behavior of the gate leakage current in β-Ga_2O_3 MOSFETs with Al_2O_3 dielectric. The results indicate that (i) the gate leakage is dominated by Poole–Frenkel (PF) conduction in forward bias at room temperatures and higher, whereas (ii) at cryogenic temperatures in forward bias the dominant process is Fowler–Nordheim (FN) tunneling. In addition, the gate current shows a decrease with thermally activated time constants, associated with the trapping of electrons that inhibit the FN conduction process. Gate leakage dynamic model is also supported by TCAD simulations capable of reproducing the experimental data.

Devices under test consist of β-Ga_2O_3 MOSFETs, processed on homoepitaxial Mg-doped (100) β-Ga_2O_3 wafers. After the epitaxial growth of a 200 nm thin Si-doped β-Ga_2O_3 channel ($n = 2.3 \times 10^{17}$ cm^{-3}) using metal-organic chemical vapor deposition (MOCVD), a 100 nm-gate recess was formed by etching the semiconductor material with BCl_3 reactive ion etching. Then, a 25 nm thick Al_2O_3 dielectric was deposited by thermal atomic layer deposition (ALD) at a temperature of 300 °C using a SENTECH system SI PEALD. A saturation dose of trimethylaluminium and water vapor with a total of 268 cycles were predetermined using a constant N_2-flow as carrier and purge gas to achieve the dielectric properties. Al_2O_3 gate dielectric was preferred with respect to SiO_2 or others because it is currently the most common choice for β-Ga_2O_3 power devices, because of the high dielectric constant[3] and good interface quality.[22,23] Both Ohmic and gate contact consist of a Ti/Au metal stack. Detailed information on the hepitaxial growth, processing, and electrical characteristics can be found in the works of Tetzner *et al.*[7,24] that reports on the same devices considered in this study.

To evaluate the physical processes responsible for conduction, we carried out temperature-dependent characterization between 120 and 350 K. Figure 1(b) reports the I_G–V_G curves collected in this temperature range, whereas Fig. 1(c) shows the extracted I_G–T characteristic for some relevant voltage levels. The measurements were performed with an Agilent 4155C semiconductor parameter analyzer, by first sweeping the devices in negative bias (from 0 to −20 V) and then in positive bias (from 0 to 5 V). The samples were enclosed in a cryogenic probe station that provides temperature control and excellent shielding from electrical noise. The negative bias sweep was proven to not introduce any trapping effect that can impact the forward characteristics.

To avoid possible effect of the electron trapping discussed in Ref. 25, before every measurement the devices were exposed to 15 min of UV illumination, which was proven to completely restore the prior trapping state. A demonstration of the effectiveness of the UV-assisted detrapping is reported in Fig. SM1 in the supplementary material.

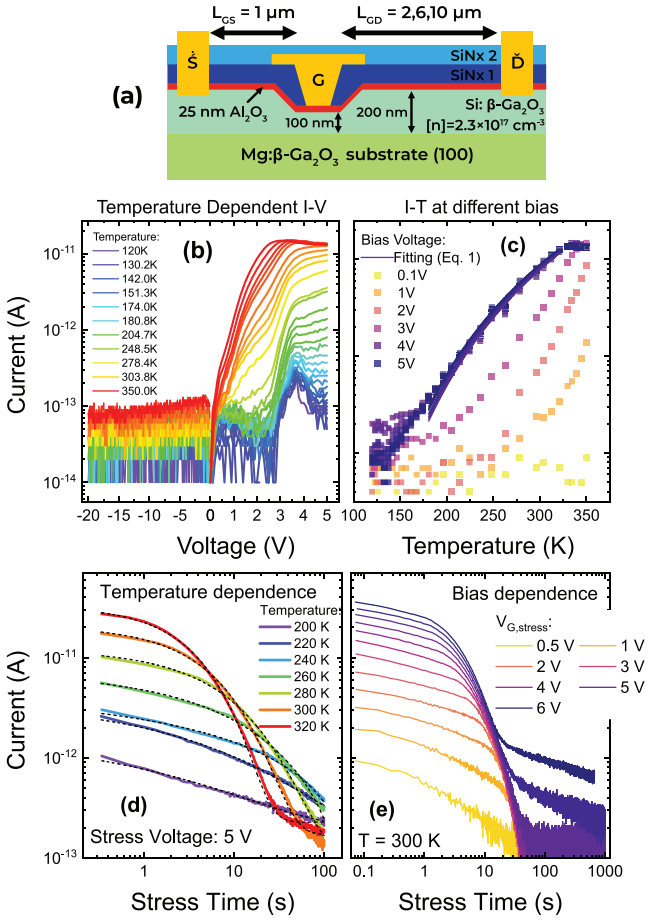

FIG. 1. (a) Schematic cross section of the devices. (b) I_G–V_G characteristics of the devices under test detected from 120 to 350 K show a strong dependence on temperature. (c) Gate current–temperature characteristics extrapolated from (b). Solid lines are fitting of the experimental data according to the adopted models [Eq. (1)]. (d) Gate current transients recorded during a constant voltage experiment at different temperatures and (e) at different bias levels. The current transient is composed of a stretched exponential as presented in Eq. (3).

Figure 1(b) shows that for high voltages (>3 V) at high temperatures (>350 K), the I_G–V_G becomes flat and slightly decreases during the measurements. By performing the same measurement with different sweep rates (not shown here), we noticed a correlation with the duration of the measurements, so it is possibly related to a dynamic decrease in the gate current. To investigate the process, we analyzed the gate leakage current transient during a constant voltage experiment, at different temperatures and constant $V_G = 5$ V [Fig. 1(d)], and constant temperature ($T = 300$ K) and different voltages [Fig. 1(e)]. The gate current shows a significant decrease over time, with a strongly temperature-enhanced time constant at high temperature compatible with the duration of the I_G–V_G measurements (∼100 s).

As an initial step, we analyzed the DC I_G–V_G characteristics to understand the static conduction model, which may provide information on the physical properties of the dielectric layer.[26]

Given the insufficient accuracy of the experimental setup at the lowest current range, the reverse leakage current was analyzed qualitatively. To improve the signal to noise ratio, we considered the average of the reverse leakage current reported in Fig. 1(b) for each temperature and then extracted a tentative activation energy from the Arrhenius Plot in Fig. 2(a) of 24 meV, by fitting the reasonable experimental data.

In strong forward bias regime ($V_G > 4$ V) at high temperatures (>200 K), results indicate that the current is compatible with a Poole–Frenkel conduction mechanism (PFC), in which the electrons are transported by a series of capture-emission process from shallow deep levels[26,27] [see Figs. 4(a) and 4(b)]:

$$I = q\,\mu\,N_c\,F\,e^{-q\frac{\left(E_{A,0}-\beta\sqrt{F}\right)}{kT}}, \tag{1}$$

where q is the electron charge, μ is the electron mobility in the oxide, N_c is the effective density of states of the conduction band, F is the electric field, $E_{A,0}$ is the ideal activation energy of the defect that assists conduction (in the absence of electric field), k is the Boltzmann's constant, and T is the absolute temperature.

The term $E_{A,0} - \beta\sqrt{F} \triangleq E_A^*$ describes activation energy reduction induced by the electric field by the Poole–Frenkel mechanism (PFM), where $\beta = \sqrt{\frac{q}{\pi\varepsilon_0\varepsilon_r}} = 2.51 \times 10^{-4}\ \text{eV}\,(\text{V}\times\text{cm})^{-\frac{1}{2}}$ for aluminum oxide [see Fig. 2(d) for a schematic view of the P–F model and the notation].

By fitting the I_G–T data in Fig. 1(c), we extracted the activation energies that are reported in a Poole–Frenkel plot in Fig. 2(b). Electric field values used in the calculations were extracted from a TCAD simulation of the structure. Effective activation energy E_A^* extracted from the fit was found to decrease with increasing electric field, as expected from the PF model, and the extracted value for β (i.e., the slope of the Poole–Frenkel plot) is in good agreement with the theoretical value reported above, thus confirming the validity of the model.[28]

At low temperature, most of the thermal processes are suppressed and the conduction can be associated with tunneling processes. In positive bias condition, the bands of the oxide form a triangular potential barrier, and so the current can be modeled by the Fowler–Nordheim tunneling [Fig. 4(a)], in which

$$J = \frac{q^3F^2}{8\pi h\Phi_B}\exp\left(\frac{-8\pi\sqrt{2qm_T^*}}{3hF}\Phi_{B,FN}^{3/2}\right), \tag{2}$$

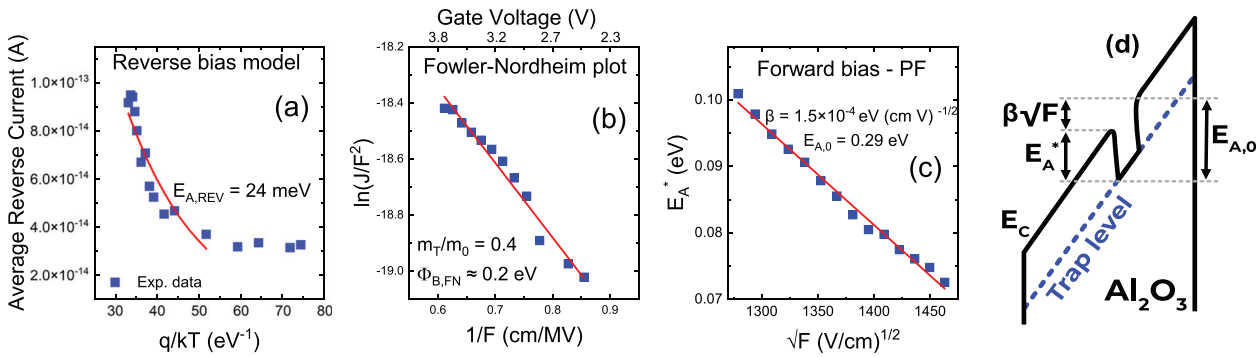

FIG. 2. Fitting of the data in Fig. 1 with the proposed conduction models. (a) Average reverse current exponentially depends on temperature with activation energy of 24 meV; (b) low-temperature low-forward bias is dominated by Fowler–Nordheim tunneling. (c) Activation energy in high-temperature forward bias is strongly dependent on the electric field, compatible with P–F effect. (d) Notation of activation energies according to the discussed model.

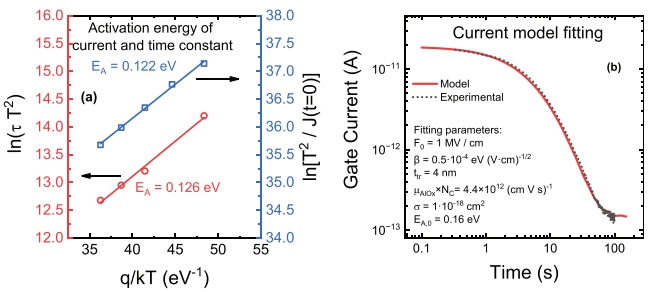

FIG. 3. Temperature dependence of the time constants of the gate current collapse and of the current at $t = 0$ extracted from Fig. 1(c).

where h is Plank's constant, $\Phi_{B,FN}$ is the barrier height, and m_T^* is the effective tunneling mass. The F–N conduction model was verified by considering the linearity of the F–N plot [Fig. 2(c)][26] for positive gate voltage and low temperature range (120 K–150 K) defined as

$$\ln\left(J/F^2\right) = \ln\left(\frac{q^2}{8\pi h\Phi_{B,FN}}\right) + \frac{1}{F}\left(\frac{-8\pi\sqrt{2qm_T^*}}{3h}\Phi_{B,FN}^{3/2}\right). \quad (3)$$

The fitting parameters reported in Fig. 2(b) identify a low barrier for tunneling, thus suggesting that the electrons do not tunnel to the conduction band edge, but are more likely to be injected in deep levels band in the oxide.

Then, we consider the time dependance of the gate current. First, from the results in Fig. 1(d), we experimentally verified that the transient is fitted by the sum of a stretched exponential and a constant term:

$$I(t) = I_0 \times e^{-\left(\frac{t}{\tau}\right)^{\alpha}} + I_{TE}, \quad (4)$$

where I_0 represents the DC, τ is the time constant of the exponential decay, and α is the stretching factor. The activation energy, obtained by the fitted value of the time constants, is reported in Fig. 3(a). The physical origin of this behavior is different from that reported for the threshold voltage in recent reports,[25] and its origin will be discussed in the following.

It is worth noting that the activation energy of the trapping process is similar to the activation energy extracted for the Poole–Frenkel conduction [see Fig. 3(a)]. In our model, we consider that the current decrease is the results of a trapping mechanisms taking place at the oxide, in which the trapping rate is proportional to the current flowing through the oxide $J(t)$:[29,30]

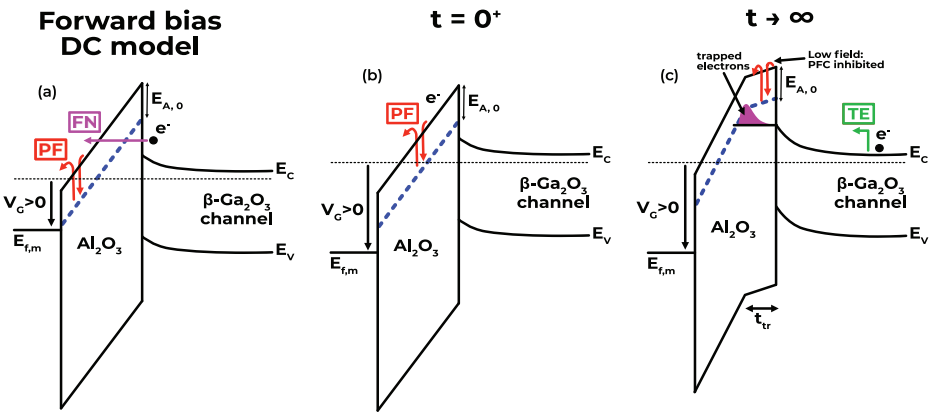

FIG. 4. Schematized conduction model. Poole–Frenkel mechanism dominates in (a) forward bias at high temperatures. (b) For $t = 0$, conduction is in line with the static process. (c) During the transient, electrons are trapped in the insulator layer, thus modifying the bending of the band diagram.

$$\frac{dn_T}{dt} = \frac{J(t)\sigma}{q}(N_T - n_T), \tag{5}$$

where σ is the capture cross section of the defect and N_T is the defect concentration. As a first order approximation, we can assume that the electrons are trapped in a centroid at position t_{tr} [Fig. 4(c)], as already proposed in the case of inhibition of TAT conduction by Oh and Yeow in Ref. 31. This induces a reduction of the ideal electric field F_0 proportional to the number of trapped electrons:

$$F(n_T) = F_0 - \frac{qt_{tr}}{\varepsilon_{ox}} n_T, \tag{6}$$

where n_T represents the volumetric trapped charge concentrated at the centroid. As discussed in Eq. (1), P–F current is proportional to the electric field. If we consider that the current is limited by the region with the lowest electric field (i.e., the region subject to electron trapping), we obtain

$$J(t) = q\,\mu N_C\, e^{-\frac{qE_A^*}{kT}}\left(F_0 - \frac{qt_{tr}}{\varepsilon_{ox}} n_T\right). \tag{7}$$

By inserting Eq. (7) in Eq. (5), we obtain a rate equation in which the trapping rate is function of the trapped charge itself,

$$\frac{dn_T}{dt} = \frac{\sigma}{q}(N_T - n_T)\, q\,\mu N_C\, e^{-\frac{qE_A^*}{kT}}\left(F_0 - \frac{qt_{tr}}{\varepsilon_{ox}} n_T\right), \tag{8}$$

with the boundary condition $n_T(0) = 1 \times 10^{19}\ \mathrm{cm}^{-3}$, which represents an estimation of the electrons already trapped in the oxide.[25] We proceeded then through numerical integration of Eqs. (7) and (8); the fitting parameters (μ, E_A, σ) were obtained through a minimization algorithm.

The results in Fig. 3(b) indicate that the equations well reproduce the experimental data, with reasonable fitting parameters. The one that deviates most from the ideal value is the PF coefficient β that results ~1/3 of the value obtained in the DC characterization section. However, the absolute value of the parameter is still reasonable, and the difference can be associated with other effects not considered by the simple model described above.

With respect to the constant component of the current I_{TE} in Eq. (4) (i.e., the residual current after the transient), we found that it is thermally enhanced and can be attributed to a thermionic emission term, due to the potential barrier associated with the depletion region at the β-Ga_2O_3/Al_2O_3 interface. In the case of strong positive bias [Fig. 1(e)], the logarithmic trapping discussed in Ref. 25 induces a small decrease for longer times of the I_{TE} component that cannot be considered constant anymore.

The proposed gate leakage model was then validated by means of TCAD simulations based on the Synopsys Sentaurus framework. The device structure was first implemented following the cross section reported in Fig. 1(a). Doping of the n-type channel was implemented by introducing a shallow donor trap with concentration of $n = 2.3 \times 10^{17}\ \mathrm{cm}^{-3}$, to guarantee a realistic device physics. Drain and source contacts were implemented as Ohmic, and the gate as Schottky with work function $\chi_{Ti} = 4.33$ eV, to match the one of titanium.[32] The simulation was then tuned in terms of fixed oxide charge, contact resistances, and interface states to match the I_D–V_G characteristics of the physical devices in terms of threshold voltage, subthreshold slope,

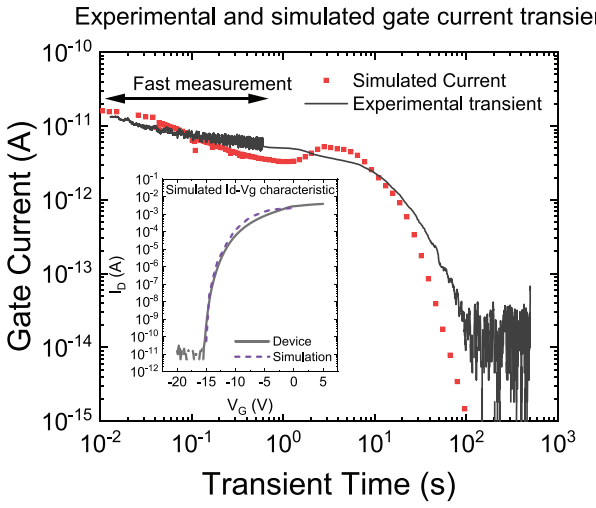

FIG. 5. TCAD simulation of the gate current drop and comparison with the measured behavior. (inset) Matching between simulated and real I_D–V_{GS} (prior to stress).

saturation current to guarantee the same electrostatic behavior (Fig. 5, inset). To simulate the gate leakage current, we included in the oxide layer a deep level with activation energy of 0.12 eV coupled by tunneling to the channel to simulate the Poole–Frenkel conduction model. The activation energy was chosen as fitting parameter. Finally, trapping in the oxide was induced by adding a high concentration ($1 \times 10^{18}\ \mathrm{cm}^{-3}$) ideally empty deep level distribution along the oxide region (the activation energy does not influence trapping). Gate current was then simulated in transient mode. To match the time constants of the current transients, we adjusted the cross section and the constant emission rate of the deep levels (that models self-detrapping of electrons from the level by tunneling). The results of the simulations were compared with the experimental gate current transients in Fig. 5. The current transient from 10 ms to 1 s was obtained by exploiting the fast current measurement of the Agilent 4155 that allows sampling times below 1 ms. This mode cannot be used to sample the full transient because of the lower current sensibility and limited memory buffer of the instrument. Simulations are in line with the experimental data, especially in terms of the trapping time constant and value of the initial gate current.

In conclusion, we discussed the gate leakage current model in the static and the dynamic regime of β-Ga_2O_3 lateral MOSFETs. We demonstrated that the gate leakage is dominated by a Poole–Frenkel conduction mechanism at high-temperature/high-bias, whereas at low temperatures and forward bias the gate leakage current can be ascribed to Fowler–Nordheim tunneling. In addition, we modeled the time-dependent drop of the gate leakage transient by considering the trapping of electrons within the gate dielectric. A model based on rate equations was proposed, whose effectiveness has been validated by means of TCAD simulations, that showed excellent agreement with the experimental results.

See the supplementary material for the details of the demonstration of the light-induced detrapping process in the β-Ga_2O_3 transistors under test.

The authors thank Z. Galazka from Leibniz-Institut für Kristallzüchtung for providing the β-Ga_2O_3 bulk crystal as well as A. Popp and S. Bin Anooz for the MOCVD layer deposition of n-type β-Ga_2O_3.

This study was carried out within the MOST—Sustainable Mobility Center and received funding from the European Union Next-GenerationEU [PIANO NAZIONALE DI RIPRESA E RESILIENZA (PNRR)—MISSIONE 4 COMPONENTE 2, INVESTIMENTO 1.4 – D.D. 1033 17/06/2022, CN00000023]. This manuscript reflects only the authors' views and opinions, neither the European Union nor the European Commission can be considered responsible for them.

This work was funded by the Federal Ministry of Education and Research in Germany within the Research Project GoNext, Funding No. 16ES1084K.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Manuel Fregolent: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Software (equal); Validation (equal); Visualization (equal); Writing – original draft (equal). **Enrico Brusaterra:** Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – review & editing (equal). **Carlo De Santi:** Formal analysis (equal); Methodology (equal); Supervision (equal); Validation (equal); Writing – review & editing (equal). **Kornelius Tetzner:** Funding acquisition (equal); Resources (equal); Validation (equal); Writing – review & editing (equal). **Joachim Hans Würfl:** Funding acquisition (equal); Resources (equal); Validation (equal); Writing – review & editing (equal). **Gaudenzio Meneghesso:** Funding acquisition (equal); Resources (equal); Supervision (equal). **Enrico Zanoni:** Funding acquisition (equal); Resources (equal); Supervision (equal). **Matteo Meneghini:** Funding acquisition (equal); Methodology (equal); Resources (equal); Supervision (equal); Validation (equal); Writing – original draft (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]C. Wang, J. Zhang, S. Xu, C. Zhang, Q. Feng, Y. Zhang, J. Ning, S. Zhao, H. Zhou, and Y. Hao, "Progress in state-of-the-art technologies of Ga_2O_3 devices," J. Phys. D **54**(24), 243001 (2021).

[2]N. Yadava and R. K. Chauhan, "Review—Recent advances in designing gallium oxide MOSFET for RF application," ECS J. Solid State Sci. Technol. **9**(6), 065010 (2020).

[3]A. J. Green, J. Speck, G. Xing, P. Moens, F. Allerstam, K. Gumaelius, T. Neyer, A. Arias-Purdue, V. Mehrotra, A. Kuramata, K. Sasaki, S. Watanabe, K. Koshi, J. Blevins, O. Bierwagen, S. Krishnamoorthy, K. Leedy, A. R. Arehart, A. T. Neal, S. Mou, S. A. Ringel, A. Kumar, A. Sharma, K. Ghosh, U. Singisetti, W. Li, K. Chabak, K. Liddy, A. Islam, S. Rajan, S. Graham, S. Choi, Z. Cheng, and M. Higashiwaki, "β-Gallium oxide power electronics," APL Mater. **10**(2), 029201 (2022).

[4]M. Higashiwaki, "β-gallium oxide devices: Progress and outlook," Phys. Status Solidi RRL **15**(11), 2100357 (2021).

[5]X. Chen, F. Li, and H. L. Hess, "Trench gate β-Ga_2O_3 MOSFETs: A review," Eng. Res. Express **5**(1), 012004 (2023).

[6]C. Gupta and S. S. Pasayat, "Vertical GaN and vertical Ga_2O_3 power transistors: Status and challenges," Phys. Status Solidi A **219**(7), 2100659 (2022).

[7]K. Tetzner, E. Bahat Treidel, O. Hilt, A. Popp, S. Bin Anooz, G. Wagner, A. Thies, K. Ickert, H. Gargouri, and J. Wurfl, "Lateral 1.8 kV β-Ga_2O_3 MOSFET with 155 MW/cm^2 power figure of merit," IEEE Electron Device Lett. **40**(9), 1503–1506 (2019).

[8]Z. Hu, K. Nomoto, W. Li, R. Jinno, T. Nakamura, D. Jena, and H. Xing, in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)* (IEEE, 2019), pp. 483–486.

[9]M. H. Wong, K. Goto, H. Murakami, Y. Kumagai, and M. Higashiwaki, "Current aperture vertical β-Ga_2O_3 MOSFETs fabricated by N- and Si-ion implantation doping," IEEE Electron Device Lett. **40**(3), 431–434 (2019).

[10]A. J. Green, K. D. Chabak, M. Baldini, N. Moser, R. Gilbert, R. C. Fitch, G. Wagner, Z. Galazka, J. McCandless, A. Crespo, K. Leedy, and G. H. Jessen, "β-Ga_2O_3 MOSFETs for radio frequency operation," IEEE Electron Device Lett. **38**(6), 790–793 (2017).

[11]A. C. Liu, C. H. Hsieh, C. Langpoklakpam, K. J. Singh, W. C. Lee, Y. K. Hsiao, R. H. Horng, H. C. Kuo, and C. C. Tu, "State-of-the-art β-Ga_2O_3 field-effect transistors for power electronics," ACS Omega **7**(41), 36070–36091 (2022).

[12]T. Kamimura, Y. Nakata, M. H. Wong, and M. Higashiwaki, "Normally-off Ga_2O_3 MOSFETs with unintentionally nitrogen-doped channel layer grown by plasma-assisted molecular beam epitaxy," IEEE Electron Device Lett. **40**(7), 1064–1067 (2019).

[13]F. Danneville, G. Dambrine, H. Happy, P. Tadyszak, and A. Cappy, "Influence of the gate leakage current on the noise performance of MESFETs and MODFETs," Solid State Electron. **38**(5), 1081–1087 (1995).

[14]S. L. Rumyantsev, N. Pala, M. S. Shur, R. Gaska, M. E. Levinshtein, M. A. Khan, G. Simin, X. Hu, and J. Yang, "Effect of gate leakage current on noise properties of AlGaN/GaN field effect transistors," J. Appl. Phys. **88**(11), 6726–6730 (2000).

[15]C. Sanabria, A. Chakraborty, H. Xu, M. J. Rodwell, U. K. Mishra, and R. A. York, "The effect of gate leakage on the noise figure of AlGaN/GaN HEMTs," IEEE Electron Device Lett. **27**(1), 19–21 (2006).

[16]D. Bisi, S. H. Chan, X. Liu, R. Yeluri, S. Keller, M. Meneghini, G. Meneghesso, E. Zanoni, and U. K. Mishra, "On trapping mechanisms at oxide-traps in Al_2O_3/GaN metal-oxide-semiconductor capacitors," Appl. Phys. Lett. **108**(11), 112104 (2016).

[17]M. Ruzzarin, M. Meneghini, D. Bisi, M. Sun, T. Palacios, G. Meneghesso, and E. Zanoni, "Instability of dynamic-RON and threshold voltage in GaN-on-GaN vertical field-effect transistors," IEEE Trans. Electron Devices **64**(8), 3126–3131 (2017).

[18]Y. Qi, Y. Zhu, J. Zhang, X. Lin, K. Cheng, L. Jiang, and H. Yu, "Evaluation of LPCVD SiN_x gate dielectric reliability by TDDB measurement in Si-substrate-based AlGaN/GaN MIS-HEMT," IEEE Trans. Electron Devices **65**(5), 1759–1764 (2018).

[19]J. He, J. Wei, S. Yang, M. Hua, K. Zhong, and K. J. Chen, "Temperature-dependent gate degradation of p-GaN gate HEMTs under static and dynamic positive gate stress," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs 2019-May* (IEEE, 2019), pp. 295–298.

[20]A. Stockman, F. Masin, M. Meneghini, E. Zanoni, G. Meneghesso, B. Bakeroot, and P. Moens, "Gate conduction mechanisms and lifetime modeling of p-gate AlGaN/GaN high-electron-mobility transistors," IEEE Trans. Electron Devices **65**(12), 5365–5372 (2018).

[21]J. Wang and X. Jiang, "Review and analysis of SiC MOSFETs' ruggedness and reliability," IET Power Electron. **13**(3), 445–455 (2020).

[22]A. Jayawardena, R. P. Ramamurthy, A. C. Ahyi, D. Morisette, and S. Dhar, "Interface trapping in ($\bar{2}$01) β-Ga_2O_3 MOS capacitors with deposited dielectrics," Appl. Phys. Lett. **112**(19), 192108 (2018).

[23]H. Zhou, S. Alghamdi, M. Si, G. Qiu, and P. D. Ye, "Al_2O_3/β-Ga_2O_3(-201) interface improvement through piranha pretreatment and postdeposition annealing," IEEE Electron Device Lett. **37**(11), 1411–1414 (2016).

[24]K. Tetzner, O. Hilt, A. Popp, S. Bin Anooz, and J. Würfl, "Challenges to overcome breakdown limitations in lateral β-Ga_2O_3 MOSFET devices," Microelectron. Rel. **114**, 113951 (2020).

[25]M. Fregolent, E. Brusaterra, C. De Santi, K. Tetzner, J. Würfl, G. Meneghesso, E. Zanoni, and M. Meneghini, "Logarithmic trapping and detrapping in β-Ga_2O_3 MOSFETs: Experimental analysis and modeling," Appl. Phys. Lett. **120**(16), 163502 (2022).
[26]F. C. Chiu, "A review on conduction mechanisms in dielectric films," Adv. Mater. Sci. Eng. **2014**, 578168.
[27]F. C. Chiu, C. Y. Lee, and T. M. Pan, "Current conduction mechanisms in Pr_2O_3/oxynitride laminated gate dielectrics," J. Appl. Phys. **105**(7), 74103 (2009).
[28]H. Schroeder, "Poole-Frenkel-effect as dominating current mechanism in thin oxide films—An illusion?!," J. Appl. Phys. **117**(21), 215103 (2015).
[29]C. De Santi, M. Fregolent, M. Buffolo, M. H. Wong, M. Higashiwaki, G. Meneghesso, E. Zanoni, and M. Meneghini, "Carrier capture kinetics, deep levels, and isolation properties of β-Ga_2O_3 Schottky-barrier diodes damaged by nitrogen implantation," Appl. Phys. Lett. **117**(26), 262108 (2020).
[30]D. R. Wolters and J. J. van der Schoot, "Kinetics of charge trapping in dielectrics," J. Appl. Phys. **58**(2), 831–837 (1985).
[31]S. J. Oh and Y. T. Yeow, "Voltage shifts of Fowler-Nordheim tunneling J-V plots in thin gate oxide MOS structures due to trapped charges," Solid State Electron. **32**(6), 507–511 (1989).
[32]B. Ofuonye, J. Lee, M. Yan, C. Sun, J. M. Zuo, and I. Adesida, "Electrical and microstructural properties of thermally annealed Ni/Au and Ni/Pt/Au Schottky contacts on AlGaN/GaN heterostructures," Semicond. Sci. Technol. **29**(9), 095005 (2014).