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Full Length Article

Measurements of radiation effects in an antifuse FPGA

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ABSTRACT

This paper presents the irradiation and the measurement analysis for a commercial antifuse Field Programmable Gate Array (FPGA) from Microsemi's Axcelerator family, part number AX250. Following proton and X-ray beam irradiation, at very high dose rate above 1krad/s, the total ionizing dose (TID) first effects were visible around 260 krad (SiO_2), and this threshold value increases at lower radiation dose rates. We expect for most space and accelerator applications that this value will be at least several Mrads, or even that the FPGA might never reach this threshold. At very high radiation dose rates, TID-induced leakage currents were observed in the device. FPGA data were recorded continuously for more than 100 h after each irradiation with a fully operating FPGA. Quantitatively, the room-temperature annealing of the radiation-induced defects leads to a fast decrease of the device leakage current by a factor of 7 in the first 100 h after irradiation. The last measurements done after three months place the currents to within 30% to 70 % relative to the before-irradiation values in case of two tested FPGA. Several firmware configurations were used to test different logic resources and to measure single event upsets (SEUs). An upper limit of SEU logic cross-section was found to be $(2.56 \pm 0.51) \cdot 10^{-13}$ cm^2/FPGA for dose rates around 1krad/s. SEU cross-section values for RAM blocks have on average a value of $(3.72 \pm 0.8) \cdot 10^{-14}$ cm^2/bit. The complete list of results is given and the effects are extrapolated to a high-energy physics experiment environment — LHCb RICH at CERN.

1. Introduction

Reconfigurable devices are in high demand in safety–critical systems. Such systems, like those in high energy physics experiments at the Large Hadron Collider [1], operate in harsh environments associated with multiple sources and types of radiation. Careful design considerations are imposed to increase the reliability of the entire system against radiation-induced failures. In many cases, the Field Programmable Gate Array (FPGA) is a common solution to use in such environments as a replacement for Application Specific Integrated Circuits (ASICs). In the readout systems, the advantage of choosing FPGAs over ASICs allows the experiment to benefit from: design flexibility, in-flight full reconfiguration, lower price, high logic density, low non-recurring engineering costs (NRE), partial reconfiguration, and dynamic self-correcting mechanisms. Usually, the commercial-grade FPGAs are known to be sensitive to ionizing and non-ionizing radiation, yet these are preferred over radiation hard by design FPGA due to costs considerations. For example, the cumulative effects in commercial CMOS FPGAs are linked to the usage of the Shallow Trench Isolation (STI) or local oxidation of silicon (LOCOS) features [2] in the fabrication process. The single event effects (SEEs) in FPGAs are due to the sudden, large, and localized charge production induced by slow ions – these ions are close to Bragg peak – in active layers of the device. This could lead to changes in logic, latch bit flips or produce transient changes. Radiation hard FPGAs cannot be used in all applications operating in radiation environments due to their limited resources or because they are much more expensive, especially when used in large readout systems with thousands of FPGAs. Hence, there is a strong interest in testing and qualifying commercial-grade FPGAs, which would allow these to be used in radiation environments. The FPGAs are provided with various error mitigation solutions on both logic and hardware level [3,4].

This paper introduces measurements done to test the reliability of an antifuse FPGA from the Axcelerator family of Microchip (former Actel and Microsemi) [5] in a radiation environment. For this FPGA, our main objectives are: to understand and map the radiation effects dependence on both total ionizing dose (TID) and on dose rates, and to measure the SEE rate for this incident proton energy, which generates ion production through collisions. The scope is to qualify the FPGA for a large range of space and accelerator applications or experiment. The antifuse FPGAs were developed at the end of 90s [6] and implement

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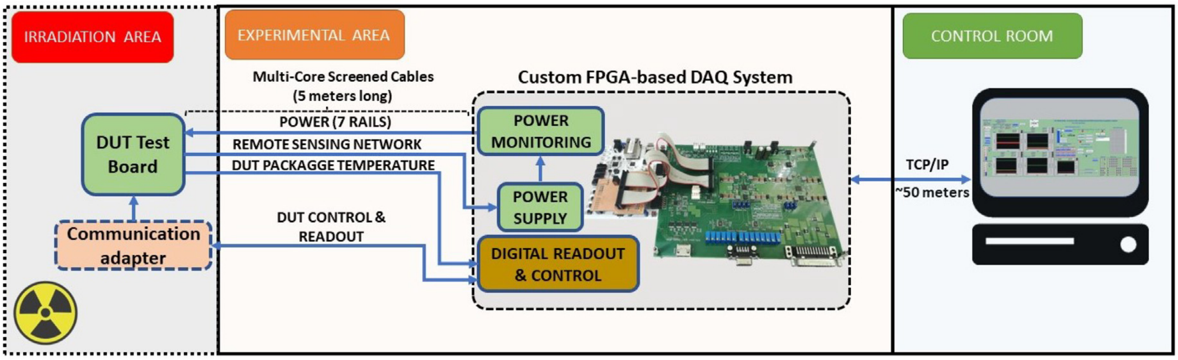


Fig. 1. The experimental setup and its layout placement that was used for testing the DUT with ionizing radiation.

the antifuse feature in the context of FPGAs. The antifuse technologies use a high-resistive dielectric, and by applying a suitable programming voltage or light, it leads to the creation of a permanent low-resistive conductive path through the dielectric — e.g., dielectric antifuses with very thin oxide between two conductors could get a conductive link after a high amplitude pulse breakdowns the dielectric in a limited region of the layer. These links are permanent, and the FPGAs are one-time programmable except for some volatile resources like SRAM, which are used in tandem with the antifuse technology in the FPGA. The antifuse technology is by nature more robust in radiation as the relatively large charge deposits which lead to single event effects, do not change these permanent conduction paths. Hence reconfiguration of user logic is less likely in this one-time programmable FPGA, and there are ways to prevent single event latch-ups (SELs) and single event dielectric rupture [7]. In this type of FPGA, the possible concerns are the TID and SEEs in user logic resources. By having this non-volatile feature, the state of the configuration memory is retained even after power cycling.

The radiation testing was done within the framework of the upgrade program of the Ring Imaging Cherenkov (RICH) sub-detectors from the Large Hadron Collider beauty (LHCb) experiment, and in preparation for the LHC third RUN (RUN3) [8,9]. The LHCb-RICH digital readout is done by SRAM-based FPGAs [10], and the antifuse FPGA was considered a backup solution. The requirements on the proposed FPGA were dictated by price, number of I/O pins, power requirements, capability for fast communication and compatibility with front-end electronics of LHCb-RICH and central LHCb DAQ units. The radiation tolerance, effective error mitigation, and programming constraints should also be added to the selection criteria. In LHCb, the FPGAs must operate with very low error rates during its entire operation period. To operate successfully for the entire time span corresponding to an integrated luminosity of 50 fb^{-1}, the FPGAs must withstand radiation levels with: a TID of 200 krad, and a flux of $1.2 \cdot 10^{12}$ high energy hadrons (HEH)/cm^2. The 1 MeV neutron equivalent (n_{eq}) fluence is expected to be $3 \cdot 10^{12}$ $n_{\mathrm{eq}}/\mathrm{cm}^2$ over 7000 h of effective LHC operation [9]. For future upgrades of the LHCb – towards the fifth LHC (RUN5) – the radiation levels are expected to be much higher: TID of 1 Mrad, and fluence of $1.5 \cdot 10^{13}$ $n_{\mathrm{eq}}/\mathrm{cm}^2$. The total expected integrated luminosity is larger than 250 fb^{-1} [11]. For a possible use of this antifuse FPGA in applications with environment like the LHCb-RICH radiation environment before and beyond RUN5, we have provided extrapolations which are given at the end of this paper.

Measuring and determining the FPGA resilience to a given radiation environment was done by exposing the device under test (DUT) to a well-defined charged particle beam or to X-ray. The DUT behavior is described by measuring its operational parameters like its power consumption, as these could change during exposure. Based on the time dependent measurements carried out before, during and after irradiation, the results are extrapolated to specific radiation environments.

2. Device under test and experimental setup

2.1. Device under test

The FPGA chosen for this irradiation campaign was an Axcelerator antifuse FPGA, part number AX250-FG484 — from now on referred to as the DUT in this paper. Its manufacturing technology is based on the 0.15 μm CMOS antifuse process (see datasheet [5]), which ensures a high device security due to the configuration memory nonvolatility. The main features of the DUT – as extracted from the datasheet – are: 350 MHz system performance, 500 MHz internal performance, 1408 register cells (R-cells), 2816 combinational cells (C-cells), up to 2816 Flip-Flops (FFs), 8 hardwired and routed clocking sources (4 of each type), up to 248 user I/O, and 55.296 kb of embedded RAM organized in 12 blocks. Due to the lack of information regarding its package composition, an X-ray imaging and a spectroscopic analysis was made to determine the X-ray attenuation during tests and proton-LET corrections. To estimate the Linear Energy Transfer (LET) of the charged particles in the die layers, a cut in the transverse section of an unused DUT was done to measure an upper-layer thickness at 0.5 mm, and the die position within the package.

The DUT, which was tested in this paper, is part of the commercial-grade antifuse FPGA portfolio of the Microchip company, and it is not declared as a radiation-hard or a radiation-tolerant FPGA. However, the company has manufactured the radiation-tolerant (RHAX250-S) and radiation-hardened (RTAX250-S) versions, with both being derivatives from the AX250. The main difference between them is the radiation hardness, as these modified versions may have added features intended to enhance the radiation resilience [12–14]. However, the radiation testing in this paper is related only to the commercial-grade version of AX250.

2.2. Experimental setup

A dedicated and versatile experimental setup was designed to measure and evaluate the DUT reliability when it is being subjected to ionizing radiation [15]. We monitor and control the DUT before, during and after the irradiation tests. The setup architecture is presented in Fig. 1, and it was designed in such a way that only the DUT is exposed to radiation. It is also flexible and can be made compatible with the facility and to respect the radiation safety constraints. It has four main components: the custom DUT test board, a communication adapter board, a custom FPGA-based data acquisition (DAQ) system and a computer.

The custom FPGA-based DAQ system represents one of the main components of the experimental setup, as it is responsible: for the remote powering of the DUT, for controlling its state and settings, and for monitoring its logic. Up to 7 individual power rails are used to power the DUT over 5 m of multi-core screened cables. All the power supply channels have remote differential feedback which measures the

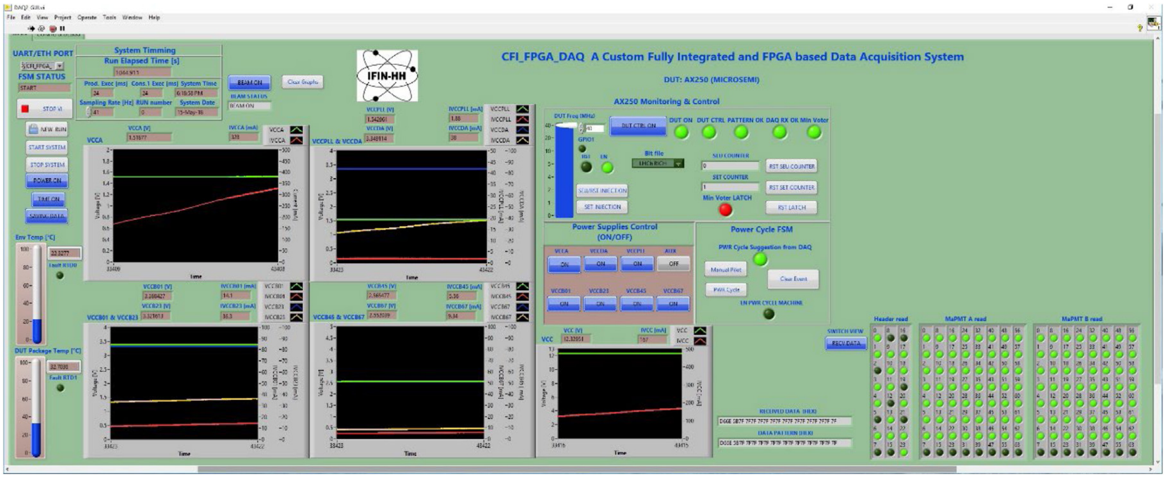


Fig. 2. LabVIEW™-based GUI designed to control, monitor, and read out the DUT, the 5 displays show key current and voltage parameter evolution during irradiation. Visible are also various switches for device control, power switch, check lights, clock frequency, etc.

voltage very close to the DUT. This ensures a very stable output voltage, and it compensates the voltage drops over the long cables. Each power rail is used to power the following DUT resources: internal core and PLL blocks with 1.5 V, JTAG interface block with 3.3 V, and 8 I/O banks with 2.5 V and 3.3 V. The power consumption on all 7 rails is monitored with a resolution of 62.5 μV for voltages and 62.5 μA for currents.

To add more information to the measurements, two resistance-to-temperature detectors (RTDs) – PT1000 platinum sensors – were used to monitor the temperature on DUT package surface and in the experimental area. Platinum RTD sensors are known to be resilient to radiation, as they are commonly used in applications operating in radiation environments [8]. This temperature monitoring is important because there is a temperature dependence in the DUT power consumption and the currents on the DUT tend to rise with the external temperature. This dependence on the environmental temperature needs to be subtracted in the annealing measurements.

The DUT test board was designed to be as simple as possible, while ensuring full functionality with minimum components on the board. About 60% of the I/O pins were routed out from the FPGA package to be used either for control or for testing. There are no other active components within a 15 cm radius with respect to the DUT center. This was designed to protect from radiation the other integrated circuits, which are used in communication with the DUT. A carefully designed layout was implemented which allows to operate the DUT continuously in radiation even for large TID-induced effects and allows precise measurements of these TID effects.

The communication between the DUT test board and the DAQ system is done with a custom communication adapter. This was designed to buffer and convert various single-ended and differential signals which are needed to implement a 1 MHz communication protocol and various control and flag signals. These signals are required by the DUT firmware to enable synchronization with the DAQ system.

A LabVIEW ™-based GUI was designed to control the operation of the DUT experimental setup through a TCP/IP intranet connection. The GUI, that is shown in Fig. 2, allows the user to control the power supply channels, to configure and read out the DUT from a safe distance. These operations are done in real time. All the recorded data concerning the DUT operational parameters which were taken before, during, and after irradiation, are being saved in ASCII files for offline analysis. The acquisition sampling rate is user configurable and can be set up to 1 KHz.

2.3. DUT firmware

Implementing the FPGA firmware dedicated to radiation testing is a key step. It is important to have a realistic logic which is as close as possible to the one proposed for the target application, i.e., the desired accelerator or space experiment. In parallel, simpler firmware versions are used to test individual hardware resources. For this DUT, several firmware versions were implemented to test specific resources: user FFs, the embedded RAM blocks, and the I/O blocks. The FF testing was done by implementing three identical branches of FFs in which a 160-bit pattern generated from the DAQ system is shifted through each branch at a 40 MHz rate.[1] The outputs of the branches are connected to the inputs of a triple modular redundancy (TMR) voter. The TMR logic can mask a SEU in one FF branch by using a voting scheme in which at least two inputs out of three need to be SEU-free to have the output data accepted by the voter. Then the output containing the 160-bit pattern from the TMR logic is shifted back to the DAQ system for comparison. The pattern is compared with the generated pattern inside the DAQ and if different the SEU counter is incremented. To test the RAM blocks, about 66% of DUT RAM resources were instantiated and hardcoded with a specific bit pattern. The RAM contents were read out at a 1 MHz rate by the DAQ and saved to disk for offline error counting. In addition, a more complex and realistic firmware was implemented to emulate a detector readout as in the case of LHCb-RICH. For this, 128 DUT input pins were used to sample a predefined external hit pattern emulating signals from a sensor array. The pattern was static and it was implemented by setting the states of the input pins either logic '0' or '1' with resistors. The inputs were sampled at a rate of 40 MHz inside the DUT logic and sent to the DAQ at a 1 MHz rate. The DAQ compares the patterns and counts the SEU. For each firmware, the FPGA is controlled and read out by the DAQ system over 5 m long screened cables. One of these cables is connected to the communication adapter attached to the DUT test board. The DUT firmware versions share the same control signals. The DAQ system provides: a 40 MHz clock to run the DUT logic, software reset, and it shares various flow control signals with the DUT. Each firmware architecture uses different types and various amounts of DUT logic resources, as can be seen in Table 1.

[1] The LHC accelerator collides bunches of particles at an interval of 25 ns, hence the electronics needs to cope with sensor signals over hundreds of thousands of channels arriving periodically at rate of 40 MHz.

Table 1
Logic resources usage within the DUT for all firmware versions.

Firmware type	Register cells (R-cells)	Combinational cells (C-Cells)	RAM blocks	I/O pins
FFs with TMR	846 (60%)	2 (0.07%)	0	5 (2%)
RAM block readout	418 (30%)	846 (30%)	8 (66%)	7 (3%)
I/O readout	326 (23%)	124 (4%)	0	135 (54%)

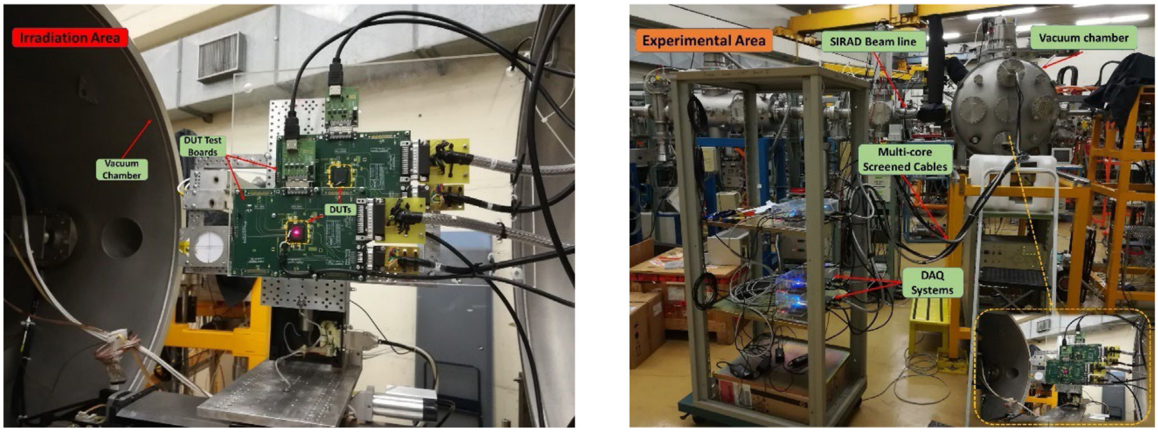


Fig. 3. The DUT test boards installed in the SIRAD vacuum chamber – irradiation area – (left side) and a view of the experimental setup installed in the vicinity of the vacuum chamber – experimental area – (right side).

3. Proton irradiation measurements

The proton irradiation was done at the SIRAD facility [16] located within Legnaro National Laboratories in Italy. The facility provided 24 MeV proton beams extracted in a vacuum chamber and with particle flux values between 10^8 and 10^9 protons/cm^2/s. Knowing the thickness of the DUT ceramic package of about 0.5 mm, the energy loss was estimated to be of about $(3.7^{+0.3}_{-0.7})$ MeV with confidence level (CL) close to 95%. This error also takes into account: beam fluctuations, beam angle, vacuum window, and package composition. The proton energies of 20 MeV or lower are highly unlikely within the FPGA active layers. Multiple samples were tested, and the TID effects and SEEs were measured. The total average fluence delivered per DUT was of from about 10^{13} to $(2.5 \pm 0.5) \cdot 10^{13}$ protons/cm^2, with an estimated 20% fluence error. All the TID values given in this paper are stated for Silicon Dioxide (SiO_2). A pause of several days was scheduled between each irradiation day, to allow time for the deactivation and for room-temperature annealing measurements. The DUT test boards were installed inside the vacuum chamber on a sample holder as it can be seen on the left side of Fig. 3. The X-Y coordinates to establish the position of the DUTs with respect to the beam exit window were determined with laser alignment. The right side of Fig. 3 shows the experimental area in the vicinity of the vacuum chamber with the rack containing the DAQ systems and the connection cables. From this area, a ~50 m ethernet cable connects to the control room to a PC for monitoring and control.

In general, the most visible TID effects are seen in leakage current increase in certain resources of FPGA or in the entire device. This assumes the drop in voltage is avoided by compensating with a fast automatic adjustment at the source. Though we have not seen in our measurements, irreversible changes or even damages could also be induced by the cumulative charge deposits, i.e. TID.

No visible TID-dependent radiation effects were observed when the DUT test board was irradiated at a relatively lower dose rate of (145 ± 29) rad/s and with TID values up to a (300 ± 60) krad dose. TID-induced effects became visible when the same DUT test board was irradiated in another run with a higher dose rate of (363 ± 72) rad/s and a TID of (3.2 ± 0.64) Mrad. An increase in the power consumption of the DUT in all its power rails was recorded — it was most visible in its core resources. The power increase is due to the accumulation of localized charges into the DUT oxide layers or at the Si–SiO_2 interface leading to a radiation-induced leakage current buildup measured after (400 ± 80) krad. This value is the cumulated TID over both runs for the same FPGA, and the time between runs was short of up to a few minutes. Fig. 4 shows the evolution of DUT core current as a function of time (left side) and of total TID (right side). Data were being recorded during a run with (3.2 ± 0.64) Mrad. The TID is directly proportional to time as the particle flux was stable on average for a given beam run. As expected, the increase in power consumption led to an increase in the power dissipation causing the DUT package temperature to reach up to 38 °C. The temperature in the experimental area remained at 23 °C.

After the beam was stopped, a strong room-temperature annealing was observed in the DUT core current (and in other resources), as these currents start to decrease in amplitude immediately after the irradiation ends. This state is due to rapid relaxation of the hole traps located near the Si–SiO_2 interface, which led to a current drop by a factor of 2 within the first 5 h. The annealing curve depicted in Fig. 5 shows the presence of other populations of hole traps localized at a distance which is farther from the Si–SiO_2 interface. These are present in the oxide and have much higher relaxation times. The DUT was left to anneal at room temperature and measurements were taken for about 135 h at an average environmental temperature of close to (23 ± 1) °C (to account for day/night measurements). During this time the core current decreased from ~400 mA to ~50 mA.

Similar annealing rates of the core current were observed when another DUT test board was irradiated with a lower dose rate (than the previous test board) of (123 ± 24) rad/s and up (3.2 ± 0.64) Mrad dose. This means that the current increase is strongly dependent on the dose rate, and at lower dose rate the second board core current – shown in Fig. 6 – increases slower before the beam stops. The annealing curve shown after the beam was stopped is almost similar to the one measured for the previous DUT board. The TID threshold from which the core current starts to increase has been found to be around (380 ± 76) krad, being close to the one measured for the previous board. Please keep in mind that this TID threshold is strongly dependent on the dose rate, and at low dose rates of at least few orders of magnitude smaller, the threshold shifts to values at least above few Mrads [17].

A third DUT test board was irradiated at higher dose rate of (1248 ± 250) rad/s, and the final delivered dose per DUT was (8 ± 2)

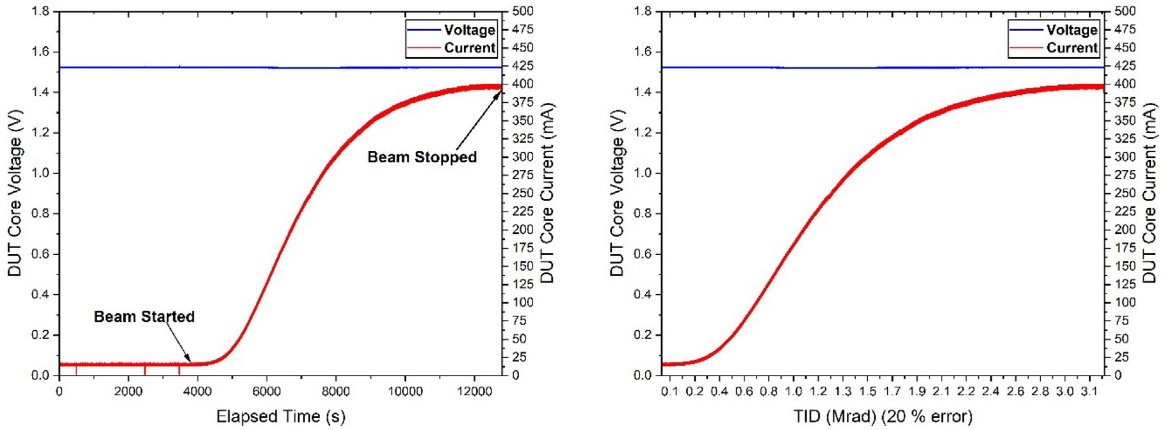


Fig. 4. The DUT core current evolution as a function of time (left side) and of TID (right side) when irradiated at a dose rate of (363 ± 73) rad/s, and with up (3.2 ± 0.72) Mrad of TID delivered. The TID threshold, from which the core current starts to visibly increase, was determined to be the sum of the TID delivered during the first run (∼300 krad) and the TID value extracted from the right-side plot just before the current starts to increase (∼100 krad), thus the TID threshold is around (400 ± 80) krad. [DUT Board no. 1].

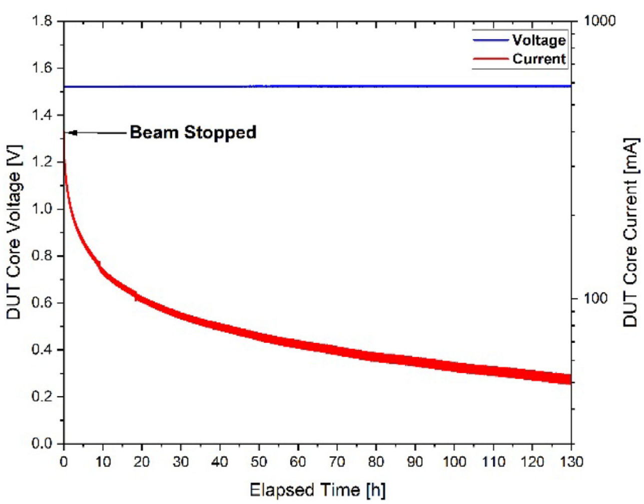


Fig. 5. The room-temperature annealing curve of the DUT core current after a cumulated TID dose of (3.5 ± 0.7) Mrad [DUT Board no. 1].

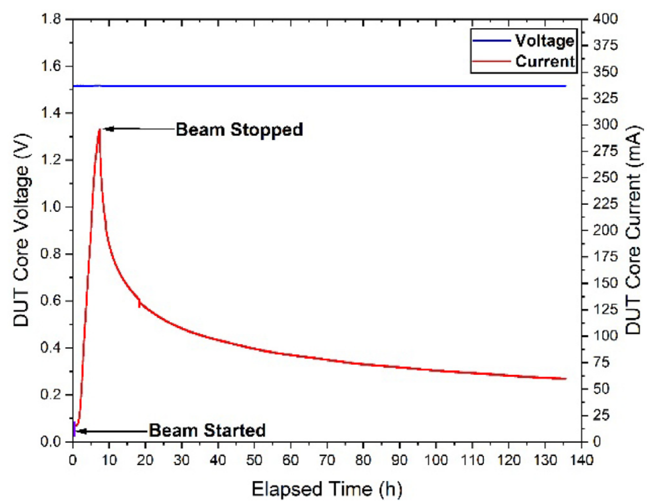


Fig. 6. The DUT core current evolution as a function of time when irradiated (123 ± 24) rad/s and up (3.2 ± 0.64) Mrad of TID delivered. The annealing curve is almost identical to the one obtained in Fig. 5. The small dip seen in the annealing curve is due to the opening of the vacuum chamber [DUT Board no. 2].

Mrad dose. Due to this high dose rate, the core current increase started to be visible at about (257 ± 51) krad, and was followed by a saturation and even a slight decrease at around (8 ± 2) Mrad. After the beam was stopped, the annealing process proceeded in the same manner as the other 2 DUT test boards. After about 38 h at room-temperature and in the same operating conditions, the DUT core current is restored from ∼470 mA to ∼60 mA. The baseline value before irradiation was of ∼10 mA. The reference value was lower on this DUT test board due to running on different firmware than the previous 2 DUT test boards. This DUT board had the "I/O readout" firmware while the previous two were running with "FFs with TMR" firmware, both firmware versions are described in Section 2.3 and Table 1.

The annealing curve path takes place in a similar manner for all three DUT test boards discussed before and is similar to what we have measured for two other test boards. One board had the same firmware as the first and second test boards from Table 2, and the other will be discussed further in the text when we discuss the SEU cross-section in RAM blocks irradiated at the same facility. Due to particular beam conditions, and, in one case, due difference in firmware, we cannot compare quantitatively the annealing and the TID effects for these two boards with the first three boards. Measurements results for all five boards are qualitatively similar, and the small observed quantitative differences could be explained by beam conditions, difference

Table 2
Summary of TID testing for 3 DUT test boards irradiated with protons.

DUT test board	Total dose [Mrad]	Dose rate [rad/s]	TID threshold [krad]
DUT Board no. 1	(3.5 ± 0.7)	1st run (145 ± 29) 2nd run (363 ± 73)	(400 ± 80) krad
DUT Board no. 2	(3.2 ± 0.64)	(123 ± 24)	(380 ± 76) krad
DUT Board no. 3	(8 ± 2)	(1248 ± 250)	(257 ± 51) krad

in firmware, and possible fabrication dispersion — the latter would explain small differences in the annealing rates. In Table 2 it can be seen a summary of TID testing for the first three DUT boards that were discussed.

No SEUs were recorded in the DUT test boards (no.1 and no.2) while irradiated with protons and different dose rate values. However, on the third board and at very high dose rates, of (1248 ± 250) rad/s, 3 SEUs were recorded while running the "I/O readout" firmware. Two SEUs were found in the data frame coming from the DUT and one SEU was seen with DUT operation failure. The latter completely froze the DUT logic, and the FPGA did not respond to any software reset. The DUT was only recovered by a full hardware reset, by means of a power cycle. Assuming a Poisson distribution, we get a value of $3^{+3.4}_{-1.4}$ for a

Table 3
Multiple measurements of SEUs cross-section values in volatile RAM blocks, the errors on the fluence are 100% correlated between measurements.

Number of SEUs recorded	Fluence [particles/cm^2]	Cross-section [cm^2/bit]
2692	$(2.1 \pm 0.4) \cdot 10^{12}$	$(3.5 \pm 0.7) \cdot 10^{-14}$
366	$(2.8 \pm 0.6) \cdot 10^{11}$	$(3.5 \pm 0.7) \cdot 10^{-14}$
1341	$(1 \pm 0.2) \cdot 10^{12}$	$(3.6 \pm 0.7) \cdot 10^{-14}$
1413	$(1 \pm 0.2) \cdot 10^{12}$	$(3.8 \pm 0.8) \cdot 10^{-14}$
1571	$(1 \pm 0.2) \cdot 10^{12}$	$(4.2 \pm 0.8) \cdot 10^{-14}$

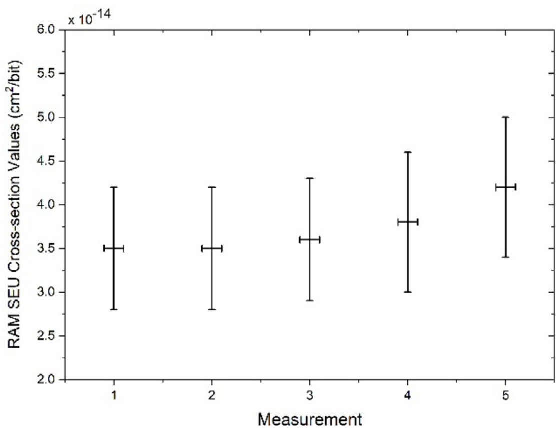


Fig. 7. Plot of measurements of SEU cross-section values within the RAM block resources, the rise tendency is given by an increase in the beam flux which was not quantified but is taken into account within the final fluence error.

95% CL. Therefore, for a total fluence of $(2.5 \pm 0.5) \cdot 10^{13}$ protons/cm^2 an upper value of $(2.56 \pm 0.51) \cdot 10^{-13}$ cm^2/DUT was obtained. The SEU cross-section for CL of 95% is defined by the limits: $(1.2^{+1.36}_{-0.54}) \cdot 10^{-13}$ cm^2/DUT, where we neglected in the first approximation the 20% error on the fluence. However, this value is valid only in extreme circumstances of operating the DUT in radiation environments with very high dose rates (1 krad/s), and it should only be considered as an upper limit, rather than an actual value of the SEU cross-section.

Dedicated tests were carried out to measure the SEU rates within the DUT RAM blocks at different fluence values — 66% out of 55 kbit RAM memory were tested by using a dedicated firmware, the "RAM block readout" from Table 1. The detailed measurement results are given in Table 3 and the average value of SEU cross-section was found to be $(3.72 \pm 0.8) \cdot 10^{-14}$ cm ^{2}/bit for protons with energy close to and higher than 20 MeV. This value is similar to other measurements published by other groups, $4.9 \cdot 10^{-14}$ cm^2/bit for 70 MeV protons [18], which likewise to us no Single event Latch-Up (SEL) was measured. The bibliographic value probably has similar error, though the latter is not given, but can be inferred to be at least larger than 2% at statistical level. A plot of the SEU cross-section measurements is given in Fig. 7.

4. X-ray irradiation results

The X-ray facility from University of Padova [19], provided 7–50 keV X-ray beams to irradiate 2 previously unused DUT test boards. It confirmed the results obtained when we measured TID effects with protons beam. The DUTs were exposed up to (2.3 ± 0.46) Mrad per DUT in several irradiation steps and with an average dose rate of (100 ± 20) rad/s. As expected, no logic errors were recorded. Similar increase of the radiation-induced leakage currents was observed in the DUT power consumption. Fig. 8 shows on the left side how the DUT core current increased as more radiation was delivered. The small current decrease between irradiation steps is due to the fast room-temperature annealing effect. The TID threshold was found to be at around (350 ± 70) krad. The average environmental temperature during the radiation tests was about 26 °C, while the DUT package temperature increased till 34.5 °C. In the right side of Fig. 8 are displayed the core current and voltage measurements as a function of an annealing time, when data were recorded over a period of about 14 h after the irradiation. The value of the core current decreased from ~274 mA to ~100 mA through room-temperature annealing.

After the irradiation, the DUT test boards were stored in safe place with a constant environment temperature of around 24 °C. Several measurements were carried out after 4 months of annealing for both DUT boards. The results showed the current dropped to within a value between 34% and 70% when compared with the reference values measured before irradiation. This difference in these two residual effects could be due to differences in the DUT boards, as different firmware versions were running on these two boards which combines with other factors like: dose rate variation, factory dispersions, etc. These low residual currents means that this DUT may recover completely from such radiation induced effects given a certain time, of several months in our case. We measured a very fast room-temperature annealing effect in the DUT, and we estimate that at low dose rates, much less than 1 rad/s, the cumulative radiation effect will be in the worst case visible only after irradiation with a TID of several Mrads.

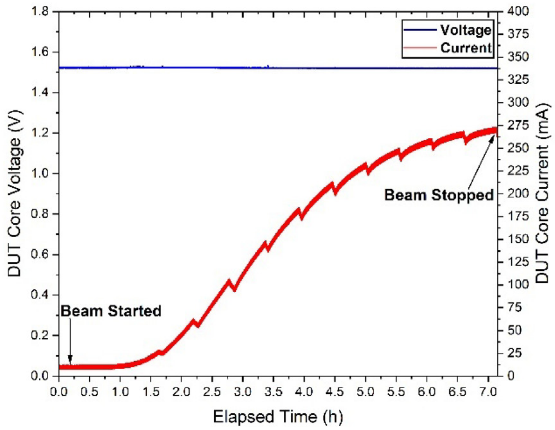
5. Conclusions

The AX250 commercial antifuse FPGA from the Microchip Axcelerator family, was proven to be very resilient to radiation effects. The DUT was tested with protons beam and at high fluence values of $(2.5 \pm 0.5) \cdot 10^{13}$ protons/cm^2. The upper limit of logic SEU cross-section was measured to be of $(2.56 \pm 0.51) \cdot 10^{-13}$ cm^2/DUT, for $3^{+3.4}_{-1.4}$ (95% CL) SEUs detected. These errors are highly unlikely to appear in a realistic application as they were seen at extreme dose rates of 1 krad/s and for extreme current values. However, all SEUs were recovered successfully with a simple power cycling. The Single Event Transients (SETs) were found to be improbable, and except for the case when the FPGA is used to configure continuously some external device, they should not affect the efficiency of the system. The RAM blocks were observed to be prone to proton-induced SEUs (actually the protons collide with nuclei and generate slow ions), and the value of SEU cross-section was determined to be $(3.72 \pm 0.8) \cdot 10^{-14}$ cm^2/bit.

The DUT survived with no permanent failure to a very high radiation flux and fluence — the largest values in the tests were a dose rate of (1248 ± 250) rad/s and a maximum deposited dose of (8 ± 2) Mrad. A high increase of the TID-induced leakage current was observed above a varying TID threshold value, especially in the DUT core resources. The rise in current was determined to be strongly correlated with the beam flux and dose rate due to the fact that the room-temperature annealing process is very strong. Overall, the DUT current values seem to be restored in a matter of a few months. For most applications in high energy physics experiments or in space industry, these radiation-induced cumulative effects in DUT are negligible, due to the much lower dose rates associated with these experimental environments. The exception seems to be a very long-lived component in the radiation induced defects which might lead to non-negligible leakage currents above a limit of several Mrads per device.

Considering the DUT behavior described in this paper, it is a good candidate to be used in the readout systems which operate in radiation environments. A few drawbacks have to be taken into account when choosing this DUT: one-time programmable, higher power consumption, low logic density when compared with the newer FPGA technologies, and its I/O voltage levels of 1.5 V might pose interfacing issues with the low-voltage peripherals as additional circuitry may be required.

Assuming the LHCb-RICH radiation environment during RUN 3 or RUN 4, the maximum TID value was estimated to be 200 krads. With an average effective operation time of about 7000 h per LHC run, the average dose rate is expected to be 0.008 rad/s. Given this very



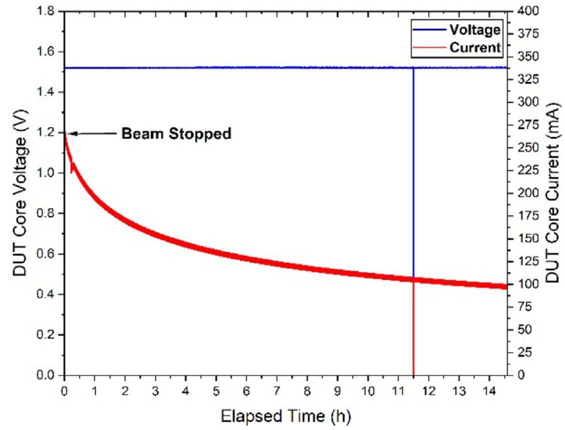


Fig. 8. The DUT core current evolution for one DUT board as a function of time (left side) when irradiated at a flux of (100 ± 20) rad/s and with TID of (2.3 ± 0.46) Mrad. The X-rays beam was delivered in smal runs. The small current drops between runs are due to the fast annealing which takes place continuously. In the right side it can be seen that the core current was more than halved during ∼14 h of room-temperature annealing.

low dose rate relative to the values used in our tests, the TID effects will not be visible as the room-temperature annealing phenomena are very strong and anneal the radiation induced defects faster than they are created. Even if we consider the next upgrade LHCb phase during RUN5, where the expected radiation levels in RICH are higher, at 1 Mrad TID with an expected dose rate of about 0.04 rad/s, we should still not see any TID-induced leakage current. The probability of SEE in the FPGA configuration is expected to be negligible for the LHCb lifetime: SET effects are expected to be benign in this application, and the SEU or SEL events in the FPGA configuration are improbable. Also, we made the assumption that we do not use the RAM blocks resources from the FPGA.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

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References

[1] L. Evans, et al., LHC machine, J. Instrum. 3 (2008) http://dx.doi.org/10.1088/1748-0221/3/08/S08001.

[2] T.R. Oldham, et al., Total ionizing dose effects in MOS oxides and devices, IEEE Trans. Nucl. Sci. 50 (3) (2003) http://dx.doi.org/10.1109/TNS.2003.812927.

[3] M. Wirthlin, FPGAs operating in a radiation environment: lessons learned from FPGAs in space, J. Instrum. 8 (2013) http://dx.doi.org/10.1088/1748-0221/8/02/S02020.

[4] M. Wirthlin, High-reliability FPGA-based systems: Space, high-energy physics, and beyond, in: Proc. of the IEEE, Vol. 103, 2015, p. 3, http://dx.doi.org/10.1109/JPROC.2015.2404212.

[5] The Axcelerator Family of Antifuse FPGAs, Microchip Technology Inc, 2023, available at https://www.microchip.com/en-us/products/fpgas-and-plds/antifuse-fpgas/axcelerator (accessed on June 28th, 2023).

[6] K.A. El-Ayat, et al., A CMOS electrically configurable gate array, IEEE J. Solid-State Circuits 24 (3) (1989) http://dx.doi.org/10.1109/4.32037.

[7] J.J. Wang, et al., Total dose and SEE of metal-to-metal antifuse FPGA, 2023, available at https://www.microsemi.com/document-portal/doc_view/131394-totaldoseantifuse (accessed on June 28th, 2023).

[8] The LHCb Collaboration, The LHCb detector at the LHC, J. Instrum. 3 (2008) http://dx.doi.org/10.1088/1748-0221/3/08/S08005.

[9] M. Fiorini, The upgrade of the LHCb RICH detectors, Nucl. Instrum. Methods Phys. Res. A 952 (2020) http://dx.doi.org/10.1016/j.nima.2018.12.003.

[10] A. Papanestis, F. Keizer, S.A. Wotton, The upgrade of the LHCb RICH system for the LHC RUN 3, J. Instrum. 15 (2020) http://dx.doi.org/10.1088/1748-0221/15/09/C09022.

[11] LHCb Collaboration, Framework TDR for the LHCb Upgrade II - Opportunities in Flavour Physics, and beyond, in the HL-LHC Era, CERN-LHCC-2021-012, 2021, available at https://cds.cern.ch/record/2776420 (accessed on June 28th, 2023).

[12] O. Melnikova, Overview of the prototyping technologies for actel®RTAX-S FPGAs, in: 2011 9th East-West Design & Test Symposium (EWDTS), Sevastopol, Ukraine, 2011, p. 3, http://dx.doi.org/10.1109/EWDTS.2011.6116422.

[13] L. Rockett, et al., Radiation hardened FPGA technology for space applications, in: 2007 IEEE Aerospace Conference, Big Sky, MT, USA, 2007, p. 3, http://dx.doi.org/10.1109/AERO.2007.353098.

[14] Microchip, Differences between RTAX-s/SL, RTAX-DSP, and axcelerator, 2023, available at https://ww1.microchip.com/downloads/aemdocuments/documents/fpga/ApplicationNotes/ApplicationNotes/rtaxs_ax_features_an.pdf (accessed on June 28th, 2023).

[15] V.M. Placinta, L.N. Cojocariu, F. Maciuc, A dedicated and versatile system for testing the radiation hardness of various integrated circuits, J. Instrum. 18 (2023) C01053, http://dx.doi.org/10.1088/1748-0221/18/01/C01053.

[16] J. Wyss, D. Bisello, D. Pantano, SIRAD: an irradiation facility at the LNL Tandem accelerator for radiation damage studies on semiconductor detectors and electronic devices and systems, Nucl. Instrum. Methods Phys. Res. A 462 (2001) http://dx.doi.org/10.1016/S0168-9002(01)00193-0.

[17] V.M. Placinta, Complex Integrated Circuits in the Radiation Environment At the LHCb High Energy Physics Experiment and Extrapolation To the Case of Space-Based Experiments, Vol. 103 (Ph.D. thesis), 2021, available at http://cds.cern.ch/record/2748584.

[18] R. Ichimiya, et al., Irradiation tests of ROHM 0.35um ASIC and actel anti-fuse FPGA for the ATLAS muon endcap level-1 trigger system, in: Proc. of the 10th Workshop on Electronics for LHC and Future Experiments, 2004, pp. 117–221, http://dx.doi.org/10.5170/CERN-2004-010.117.

[19] D. Bisello, A. Candelori, A. Kaminski, A. Litovchenko, E. Noah, L. Stefanutti, X-ray radiation source for total dose radiation studies, Radiat. Phys. Chem. 71 (2004) http://dx.doi.org/10.1016/j.radphyschem.2004.04.071.