

Threshold voltage instability in SiO₂-gate semi-vertical GaN trench MOSFETs grown on silicon substrate

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ABSTRACT

We analyze the threshold voltage stability under positive gate stress in semi-vertical GaN trench MOSFETs with silicon oxide gate insulator. The experimental results, obtained by a fast setup capable of recording the threshold voltage transient with stress time as low as 10 μ s, indicate that positive gate voltage induces a trapping of electrons in oxide border traps. In addition, experimental data obtained at different temperature and recovery bias conditions suggest that trapping proceeds through tunneling, from the inversion channel in the p-GaN layer to the traps. Finally, we developed a mathematical framework to model such tunneling process that conceptually explains the origin of the strongly stretched trapping transients and the results were compared with some relevant references on positive bias temperature instability in Si and GaN based devices.

1. Introduction

Since the first development of silicon and silicon carbide (SiC) solid-state devices for power electronics, vertical MOS configuration played a fundamental role because of the better properties in terms of breakdown voltage, ON-resistance, area consumption [1]. In the last few years, the outstanding properties of gallium nitride (GaN) in high electron mobility transistors (HEMTs) on silicon substrate demonstrated to be compatible with mass production and started to gain market share in the low (50 V \div 200 V) and medium-voltage (650 V) range [2].

Following the development of other material systems, vertical GaN technology for the high voltage range (≥ 1200 V) is under development. Regardless the demonstration of interesting properties such as avalanche capabilities [3,4], they are far to be optimized and still present strong stability and reliability issues [5,6].

In this work, we present a detailed investigation of the threshold voltage stability of vertical GaN trench MOSFETs with silicon oxide gate dielectric and polysilicon gate. The experimental results, obtained with a fast threshold voltage experimental setup, indicate the critical role of the gate insulation in the stability of the devices and indicate a possible way for the optimization of the technology. Finally, a mathematical

model that describes trapping towards tunneling was developed.

2. Devices under test and DC characterization

In this study we consider semi-vertical GaN trench MOSFETs (T-MOS) grown on a silicon substrate with polysilicon gate metal, developed with a CMOS-compatible process, whose structure is schematically reported Fig. 1.

The epitaxy consists of a strain-relief buffer layer, a n⁺ drain layer followed by a n⁻/p/n⁺ stack.

The nominal magnesium concentration in the p-GaN layer is $N_A = 1 \times 10^{19} \text{ cm}^{-3}$.

The silicon oxide (SiO₂) single-layer gate dielectric was deposited by low-pressure chemical vapor deposition at 785 °C.

The stability of the gate module was first characterized in DC regime, by performing a series of repeated I_D-V_G sweeps with increasing maximum voltage (Fig. 2a). Between each sweep, we exposed the devices to 365 nm (3.4 eV) UV illumination for few minutes, to prevent cumulative charge storage. The UV-assisted restore of the trapping state can be appreciated in Fig. 2a, where all the “go” I_D-V_G are superimposed, with a negligible contribution to the total V_{TH} shift.

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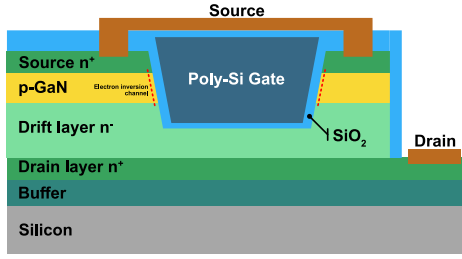


Fig. 1. Schematic structure of the vertical GaN T-MOS under test.

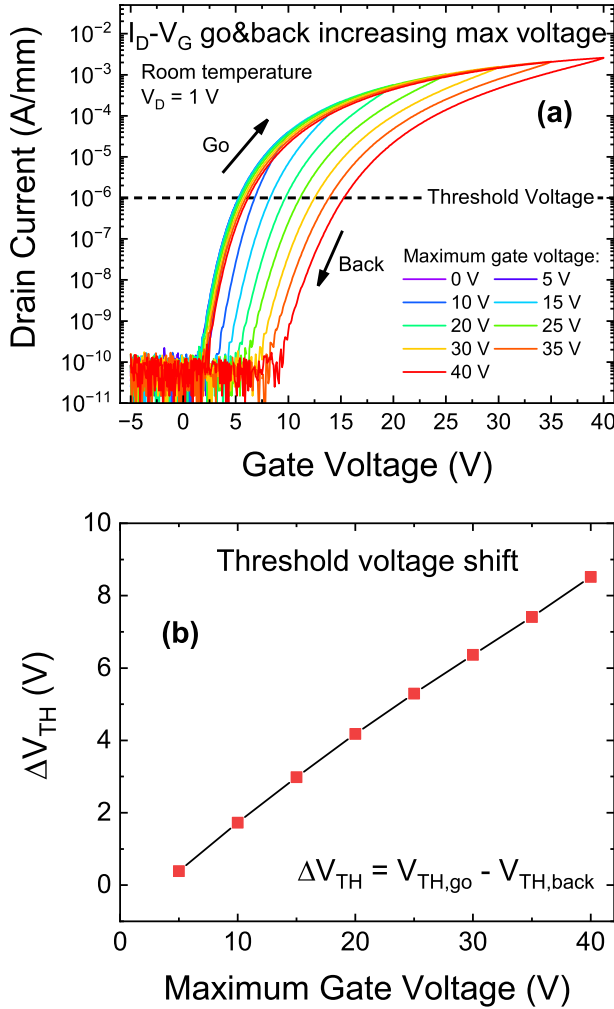


Fig. 2. (a) repeated I_D - V_G characteristics up to increasing maximum voltage shows a large hysteresis for large stress. (b) Threshold voltage shift linearly depends on the maximum gate voltage.

The threshold voltage shift, defined as the difference of V_{TH} between the go and back sweep at a drain current of $1 \mu\text{A/mm}$, is subject to a linear increase with maximum gate voltage, as presented in Fig. 2b.

3. Analysis of trapping mechanisms with threshold voltage transients

To investigate the trapping process, we relied on fast threshold voltage transient experiments, in which the device is stressed at a constant quiescent bias ($V_{G,QB}$; $V_{D,QB}$), periodically interrupted to sample the threshold voltage with a fast $10 \mu\text{s}$ gate voltage ramp. The recovery

bias is applied immediately after the stress, and the V_{TH} measurement follows the same procedure. Additional information on this setup and the typical waveforms are reported in [7,8]. During the threshold voltage measurement, the drain was biased at $V_D = 1 \text{ V}$ and the threshold voltage was extracted at a drain current of $I_D = 0.5 \text{ mA/mm}$, higher than before because of the lower resolution of fast measurements. As before, UV light was applied between each measurement to restore the original trapping state.

In the first place, we investigated the dependence of the trapping process on stress bias, by performing a series of gate stress from 0 V to 40 V , followed by a $V_G = 0 \text{ V}$ recovery, and monitored the V_{TH} with a gate sweep from 0 V to 40 V (Fig. 3). The non-monotonic threshold voltage instability detected especially for the low voltage stresses ($0 \text{ V} - 10 \text{ V}$), is the result of the trapping induced by the gate ramps, that becomes negligible for high stress times.

For high stress bias ($> 20 \text{ V}$), the threshold voltage has a monotonic increase, with a very stretched and non-exponential time dependence, which is usually a result of a process that involves trapping in the oxide layer.

This process involves border traps (levels found $1-2 \text{ nm}$ from the channel/oxide interface) easily reached by the electrons by tunneling. In addition, the trapping kinetic in those levels may be slowed by the Coulombic inhibition effects [7,9,10].

To investigate whether the recovery bias influences the detrapping process, we repeated the same experiment with a constant gate stress of 30 V and different recovery bias from 0 V to -20 V . From now on, to limit the impact of the I_D - V_G measurement the maximum voltage of the ramp was reduced to 30 V . The transients in Fig. 4.b indicate a strong effect of the negative recovery bias in the detrapping process; in contrast

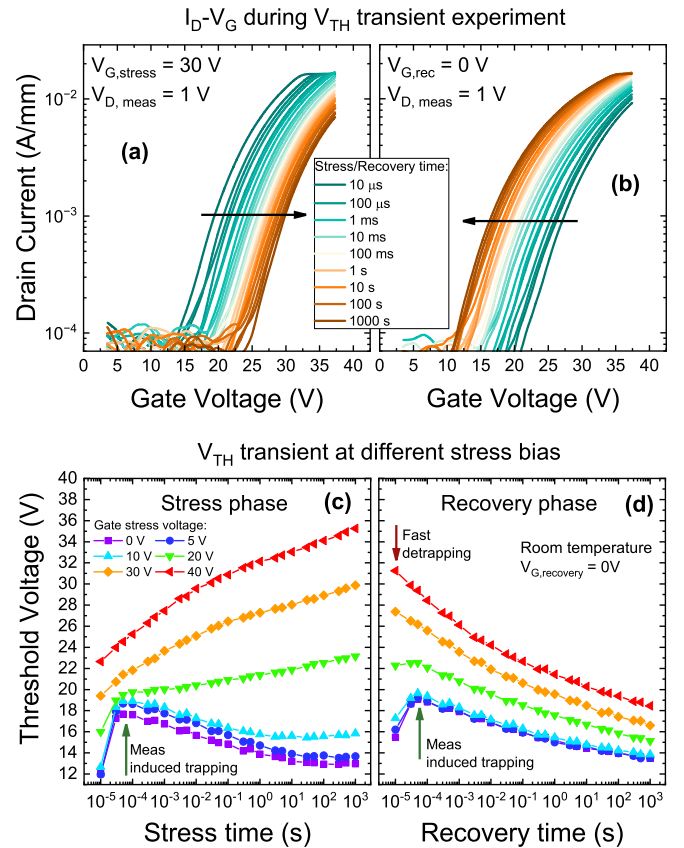


Fig. 3. I_D - V_G s during (a) stress and (b) recovery V_{TH} transient experiments; extraction of V_{TH} during (c) stress and (d) recovery at different different stress bias. The non-monotonic V_{TH} recorded for low stress voltages is the result of the trapping induced by the $10 \mu\text{s}$ ramps.

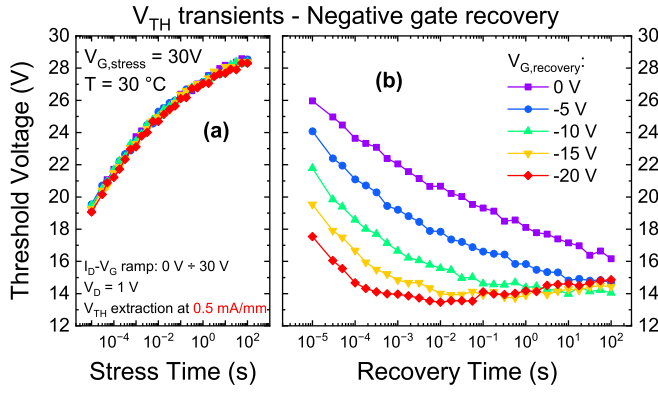


Fig. 4. (a) V_{TH} transient with a constant stress of 30 V and (b) recovery at different negative voltages. After 0.1 s of recovery time we notice the onset of a negative bias trapping mechanism.

with other records of pure inhibition-limited trapping [9].

Looking at the recovery transient induced by the -20 V bias, we noticed the establishment of a slightly positive V_{TH} shift after 0.1 s, that can be ascribed to trapping due to reverse gate leakage (i.e. electrons injected from the gate metal to deeper oxide states).

The broad trapping kinetic and the strong dependance on recovery bias suggest that trapping (and detrapping) may be promoted by injection (and emission) via tunneling of electrons from (and to) the semiconductor channel.

4. Temperature analysis

The temperature dependence of the trapping process was investigated by a constant stress $V_{G, stress} = 30$ V, followed by recovery at different voltages and temperatures. In Fig. 5 are reported the experimental results for $V_{G, rec} = 0$ V; -10 V. During stress (Fig. 5a, c) we

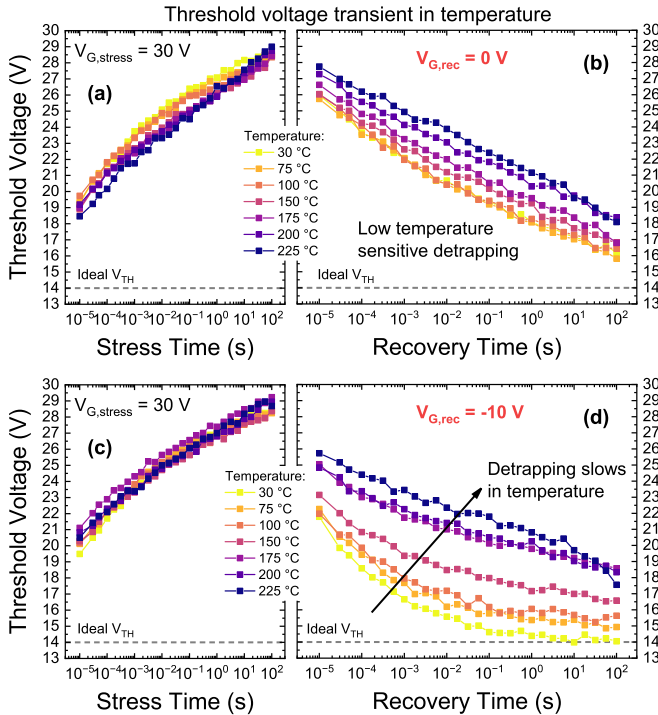


Fig. 5. Threshold voltage transients under (a, c) $V_{G, stress} = 30$ V stress and (b) $V_{G, rec} = 0$ V and (d) $V_{G, rec} = -10$ V detected at different temperatures between 30 °C to 225 °C.

noticed no temperature dependence since the trapping curves are almost superimposed one to each other.

During the recovery phase, the temperature dependence of the process at low gate voltage is negligible, while at high negative voltage and temperatures becomes slower, as a possible effect of the interplay with the positive threshold voltage increase previously identified; however, since this process is not critical for the overall stability of the devices, its detailed analysis is out of the scope of this paper. The latter results can be explained by considering a trapping process promoted by tunneling. In general, elastic tunneling does not present strong dependence on temperature, because the thermal energy of the carriers is negligible with respect to the tunneling barrier, which in turn is negligibly temperature dependent.

5. Discussion of the tunneling trapping model

In general, for MOS-like devices, trapping in the oxide layer can be the effect of trapping in interface states, border traps, and bulk states. Even if the physical microstructure of the latter two is similar, trapping in border traps is strongly enhanced because of the shorter tunneling distance from the semiconductor channel [11–13].

In GaN trench MOSFETs with p-GaN channel layer, the electron channel is formed when the p-type material reaches inversion condition. Once the electrons populate the channel, they are pushed by the electric field towards the interface and can easily reach a defect through tunneling. Since the tunneling process is elastic, electrons do not gain and lose energy during the transition.

Consequently, to reach a defect with distance x_T from the interface, an electron must overcome a trapezoidal potential barrier (Fig. 6) and the transmission coefficient is given by the solution of the Wentzel-Kramer-Brillouin approximation of the stationary Schrodinger equation, following the approach originally proposed by Oh and Yeow [14,15]:

$$T(x_T) = \exp \left\{ -\frac{4(2m^*)^{1/2}}{3qhF} \left[\overline{\Delta E_C}^{3/2} - (\Delta E_C - qFx_T)^{3/2} \right] \right\} \quad (1)$$

where F is the electric field, m^* is the effective tunneling mass and the other constant have the usual meaning. To model the contribution of the inhibition effect we considered that the trapped electrons induce an increase of the barrier proportional to the number of trapped electrons:

$$\overline{\Delta E_C}(t) = \Delta E_C + \delta E_C = \Delta E_C + \alpha \cdot n_T(t) \quad (2)$$

As one may expect, the tunneling probability increases with the electric field, and reaches its maximum for defects at the interface; furthermore Eq. (1) is independent on temperature. Since the defects are spatially distributed, each distance x_T will introduce an exponential contribution, with time constant $\tau_{x_T} = \frac{B}{T(x_T)}$, where B is a proportionality constant that ideally represents the minimum trapping time. Now, given the distribution of defects $N_T(x_T)$ [cm^{-3}], the total amount of trapped electrons per unit area can be then calculated by integrating all the

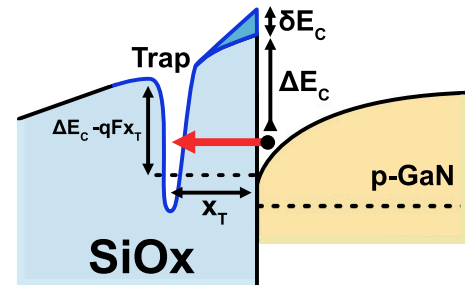


Fig. 6. Band diagram of the p-GaN/oxide with a description of the tunneling-base trapping mechanism.

exponential contributions:

$$n_T(t) = \int_0^{\infty} \left(1 - \exp \left\{ -\frac{T(x_T)}{B} t \right\} \right) N_T(x_T) dx_T \quad (3)$$

The integration of different exponential contribution gives a broad trapping transient modeled by a stretched exponential [16].

The equation developed in this section was then implemented in a numeric solver in which we simulated the effect of a constant distribution of traps. The normalized results are reported together with the fitting parameter in Fig. 7.

In case of detrapping (Fig. 8b), when the gate is biased at negative voltage, the electric field changes direction and the electrons are detrapped to the channel following a similar mathematical description of the latter case.

6. Literature review

In this section, we provide a short literature review of positive bias threshold instability (PBTI) in Si and GaN-based devices. The first works on Silicon MOSFETs, identified as root cause of the V_{TH} instability interface and bulk deep levels caused by the non-optimized oxide deposition. Quasi-logarithmic trapping transients were reported for standard SiO_2 [17], or high-K gate insulators [18,19] and were generally attributed to trapping in border traps filled by tunneling processes or repulsive trapping [10]. As discussed in this work, novel GaN technologies are still prone to charge trapping processes. In the case of GaN MIS HEMTs, given the complex structure, the V_{TH} instability can be associated to trapping (and detrapping) in interface states at the AlGaN/GaN or insulator/GaN heterointerface, or bulk insulator deep levels [20,21]. The investigation of the physical origin of the traps is not straightforward, because trapping can be the result of the interplay of different transport and tunneling processes, that are difficult to isolate and characterized separately [22,23]. For what concerns vertical GaN devices, most of the literature reports attribute again the trapping to oxide border traps, in good agreement with the results obtained for other material systems, regardless the device topology (trench MOS, finFET) [24,25], and the oxide type [26].

7. Conclusions

In conclusion, we provided a detailed investigation of threshold voltage instability in vertical GaN trench MOSFETs. We showed by

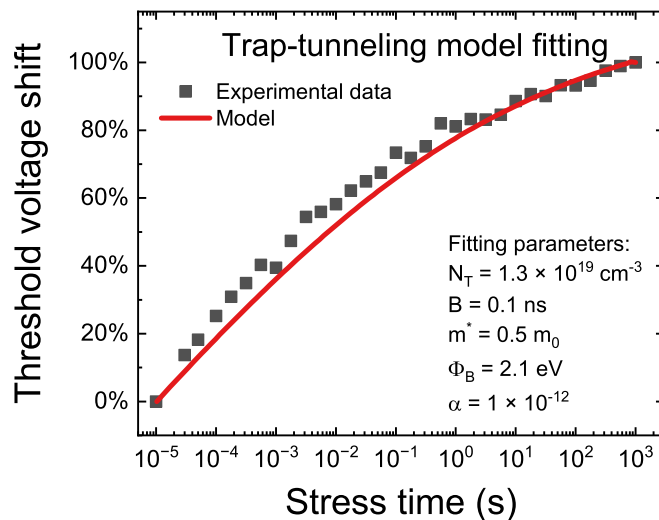
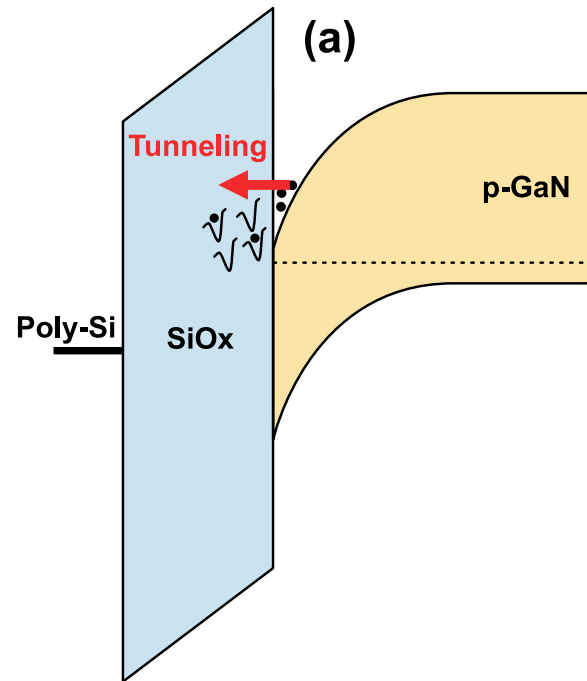


Fig. 7. Fitting of experimental data from Fig. 1 with the tunneling model developed. To get rid of additional fitting parameters, data and model was normalized between maximum to minimum.

Positive bias (stress)



Zero/negative bias (recovery)

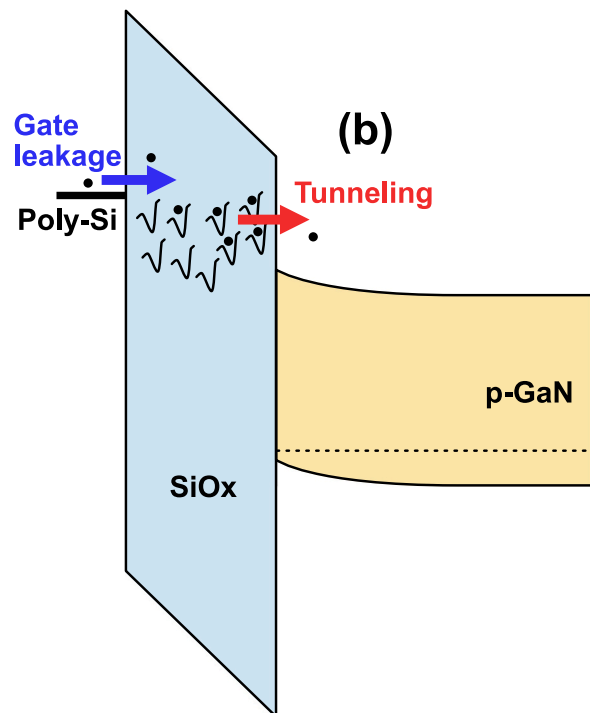


Fig. 8. schematic model of the direct tunneling model responsible of the trapping mechanism. (a) In stress condition electrons are injected to the oxide border traps, while (b) in recovery condition the electric field induces the detrapping to the channel.

analyzing the threshold voltage transient experiments in different conditions of stress and recovery bias and temperature that the trapping is due to the tunneling injection of electrons to oxide border traps. The model was then verified by developing a mathematical framework that describes the tunneling process. Since the approach proposed here does not provide a full understanding of energy level of the traps involved in trapping, additional information could be obtained by optical-assisted measurements [27] that enable to explore trapping states in wide energy range.

CRedit authorship contribution statement

All authors have contributed equally.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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