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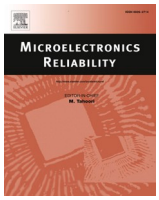

Scaling of E-mode power GaN-HEMTs for low voltage/low R_{on} applications: Implications on robustness

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ABSTRACT

We analyze the impact of scaling on the off-state, three-terminal, lateral breakdown of 100 V E-mode p-GaN/AlGaN/GaN HEMTs for low-voltage/low on-resistance applications. To this aim, we compared device structures with different SiO_2 dielectric thickness below the field plate, and varying gate-to-drain spacing and field-plate dimensions. The results indicate that: a) the breakdown voltage depends on the geometry and on the thickness of the dielectric under the field plate (t_{SiO_2}); b) scaling the dielectric thickness increases the sensitivity of breakdown voltage to the gate-drain distance, while preserving device robustness (breakdown voltages above 150 V for a 100 V technology); c) for the devices with thinner dielectric, breakdown voltage scales linearly with gate drain distance, and with field plate length. A further analysis of the data reveals that the critical parameter in terms of reliability is the distance between the field-plate edge and the drain contact; d) scaling of the dielectric thickness does not enhance charge trapping phenomena. In summary, the results provide guidelines for scaling GaN HEMT device dimensions, while preserving reliability and immunity to charge trapping phenomena.

1. Introduction

Thanks to the high breakdown voltage, large two-dimensional electron gas densities, and high electron saturation velocity, gallium nitride (GaN) high-electron-mobility transistors (HEMTs) are ideal devices for high-frequency and high-power applications, such as radars, electronic countermeasures, 5G applications, small base stations, new communication microsatellites, power transmission and automotive electronics [1–5]. Recently, the interest in GaN transistors for power applications has significantly increased.

Breakdown represents a relevant aspect for high power/high voltage HEMTs [6]: over the past years several groups have investigated the physical origin of breakdown [7–14], with the aim of developing models to explain this phenomenon, and of suggesting technological improvements to increase the robustness of the devices.

The breakdown voltage V_{BR} is typically found to scale nearly linearly with L_{GD} with a $\Delta V_{BR}/\Delta L_{GD}$ slope that is smaller than the critical field for avalanche (E_{crit} = 3.3 MV/cm [2]). Field-plates (FP) are typically added to mitigate the peak value of an electric field along the channel [10] and to suppress current collapse. [11]

One of the most relevant perspectives for GaN devices is their application in GaN-based integrated circuits, which allow the fabrication of ultra-compact switching-mode power converters [15]. To this aim, device scaling is becoming increasingly important [16–18], and this has an impact on reliability.

The purpose of this work is to provide an extensive analysis of the impact of device geometry and dielectric structure on the performance and reliability of scaled HEMTs for low-voltage/low on-resistance application, that may be adopted also in GaN integrated circuits. The results presented generate a relevant understanding on the limits of the current technologies, and on the perspectives of scaling, in terms of both performance and reliability.

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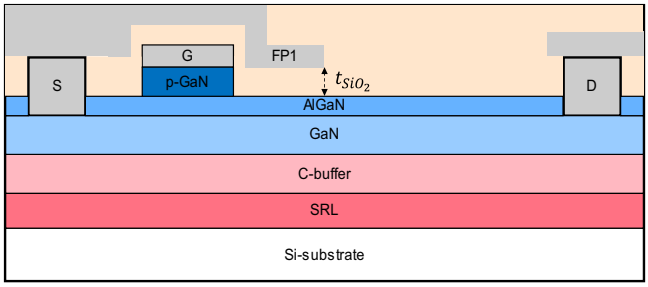

Fig. 1. Schematic structure of the pGaN/AlGaN/GaN HEMT under analysis.

2. Experimental methods

The original results described within this paper were obtained on p-GaN/AlGaN/GaN HEMTs, grown on silicon substrate by metal–organic chemical vapor deposition (MOCVD) [6]. The device processing starts with the simultaneous p-GaN gate and gate metal patterning, followed by the deposition of a thin surface passivation dielectric. On top of the passivation, a SiO_2 layer with different thicknesses t_{SiO_2} (A and B, where B is 50 % thicker than A, see Fig. 1) is deposited on different wafers with the same epitaxial stack.

The SiO_2 dielectric is opened at the location of the source and drain ohmic contacts, and an Al-based metal is deposited and patterned forming the ohmic fingers and a source-connected field plate.

The device is then finished with a CMP (chemical mechanical polishing) planarized backend and two metal layers for interconnection.

A schematic structure can be seen in Fig. 1.

A split experiment was carried out, to identify:

- The impact of gate-length
- The impact of gate-drain length
- The impact of source field plate length

on the robustness of the devices. All parameters were varied with respect to the reference devices, as specified in the figures.

The breakdown limits were characterized by means of drain current

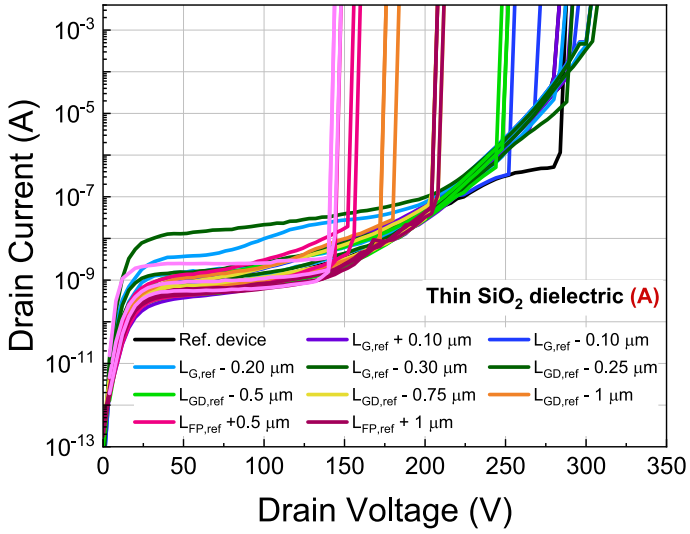

Fig. 2. Breakdown measurements carried out on devices with different thin dielectric layer. Devices with different gate-to-drain length and field plate length are plotted together (we indicate the variations, in µm, compared to the reference device).

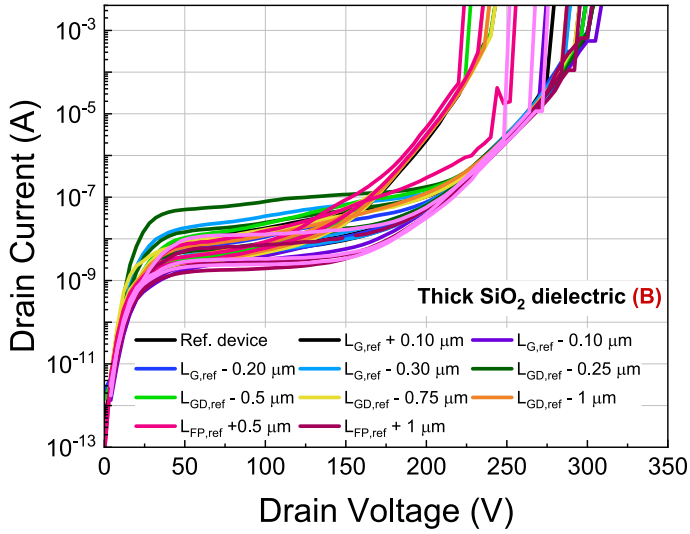

Fig. 3. Breakdown measurements carried out on devices with different thicker dielectric layer. Devices with different gate-to-drain length and field plate length are plotted together (we indicate the variations, in µm, compared to the reference device).

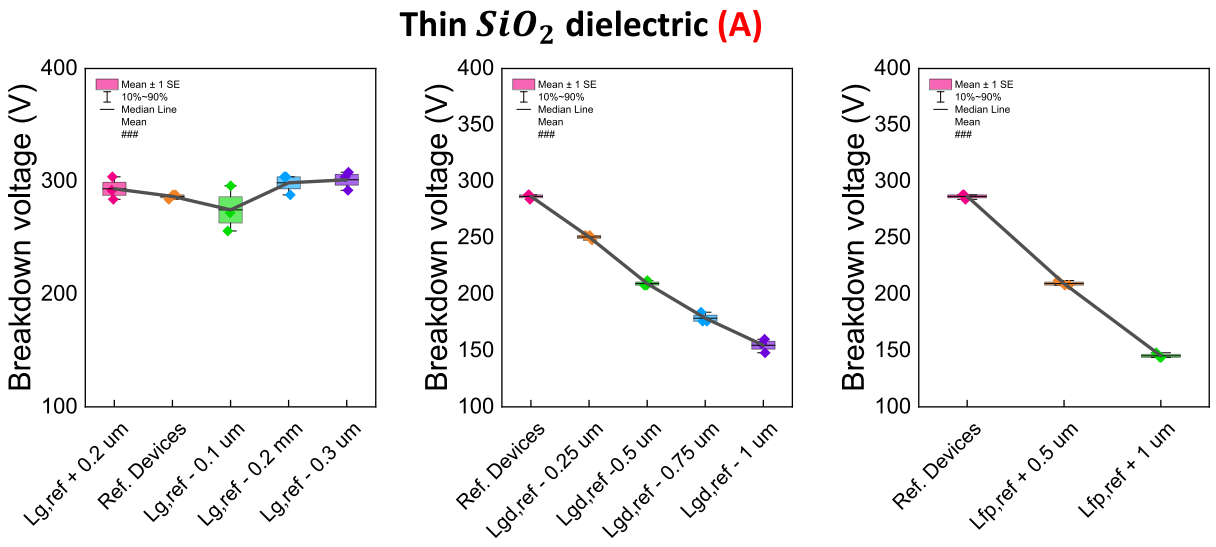

Fig. 4. Quantitative comparison of breakdown voltage for devices with a thin dielectric as a function of geometry.

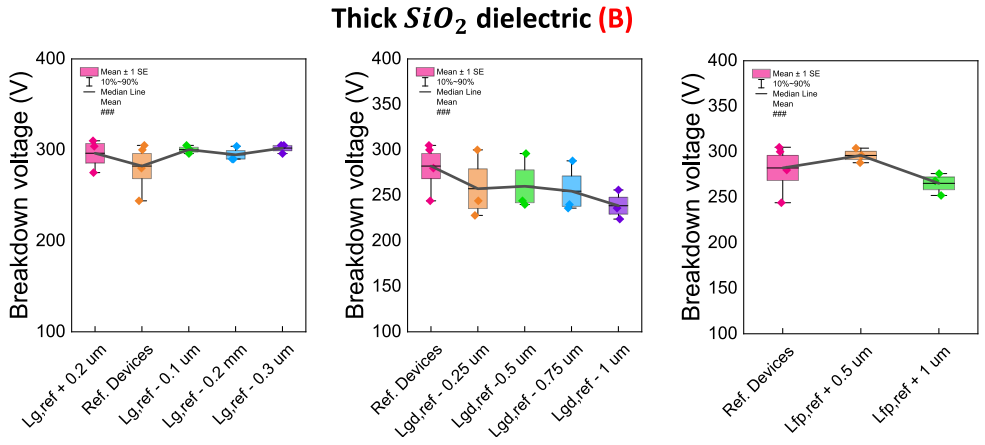

Fig. 5. Quantitative comparison of breakdown voltage for devices with a thick dielectric as a function of geometry.

vs drain voltage measurements, which were carried out in the off-state ($V_G = V_S = V_B = 0$ V), with a compliance on the current level, to avoid the catastrophic failure of the devices induced by the measurements.

3. Results and discussion

Figs. 2 and 3 report the results of breakdown measurements carried out in devices with different geometry and dielectric thickness.

The devices with thin SiO_2 dielectric (A) show breakdown voltages higher than 140 V for every geometry considered, and a breakdown voltage in excess of 250 V for the reference geometry. For this set of devices, a change in the geometry (i.e. a variation in gate-drain spacing or of field plate length) has a significant impact on breakdown voltage.

On the other hand, the devices with a thicker SiO_2 dielectric (B) show a much higher breakdown voltage (close to 250 V for most geometries), and a very limited dependence of robustness on the geometry.

A clear comparison is given by Figs. 4 and 5, which report the breakdown voltage for the two wafers with thin and thick dielectric, as a function of device geometry. As can be noticed:

- **Gate length** does not impact on off-state breakdown voltage, for both wafers. This is consistent with the hypothesis that breakdown occurs at the drain-edge of the gate [19]

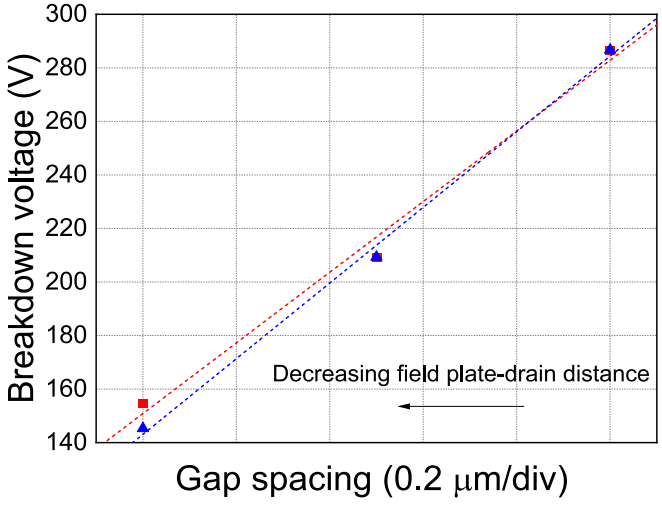

Fig. 6. Breakdown voltage of devices on the wafer with thin dielectric (A), plotted as a function of gap spacing. Gap spacing is defined as the distance between the field plate head and the drain contact. Red squares (the field plate length is constant, and the gate-drain spacing is varied); blue triangles (the gate-drain spacing is constant, and the field plate length is varied). The horizontal scale is removed for confidentiality reasons.

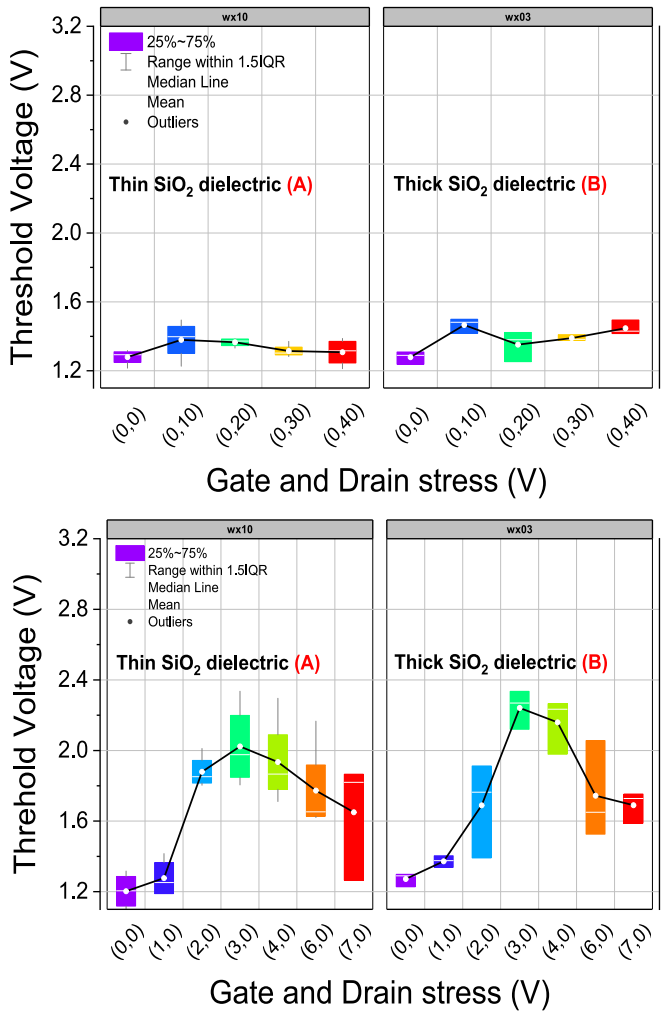

Fig. 7. Impact of charge trapping induced by off-state stress (top) and by a positive gate bias (bottom) on the threshold voltage, for the wafers with different dielectric thickness.

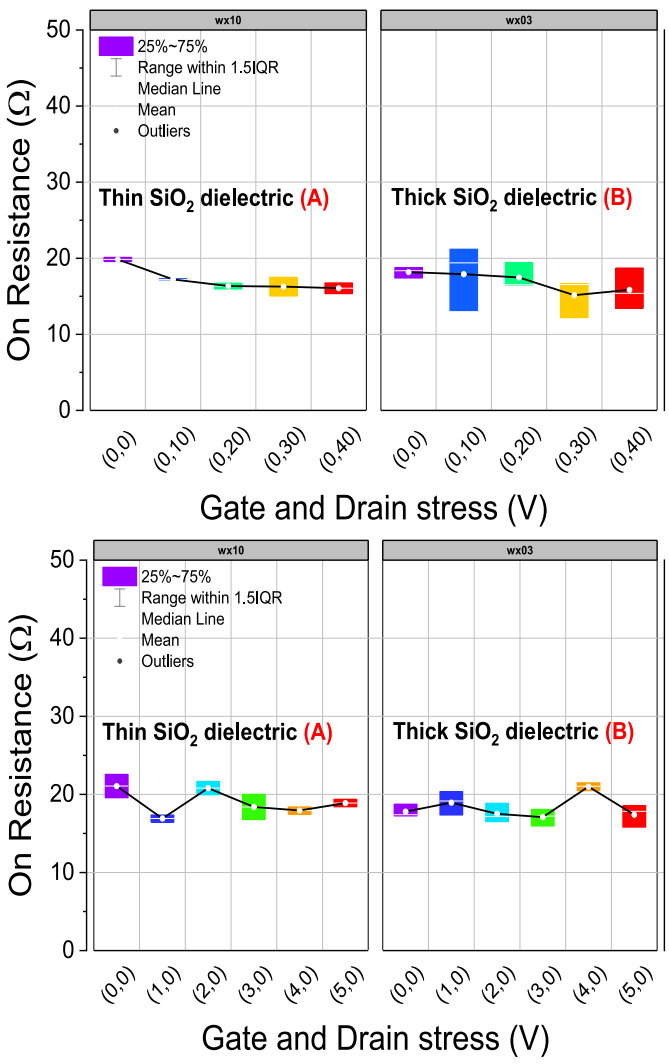

Fig. 8. Impact of charge trapping induced by off-state stress (top) and by a positive gate bias (bottom)on the on-resistance, for the wafers with different dielectric thickness.

- **For the wafer with thin dielectric (A)**, a significant reduction in breakdown voltage is observed when the gate-drain spacing is shortened, or when the field plate length is increased beyond the reference value
- **The wafer with thick dielectric (B)** does not show a reduction in breakdown voltage even for the most scaled dimensions. Failures are thus ascribed to the breakdown of the vertical stack.

The plots in Fig. 4 indicate that the wafer with thinner dielectric is sensitive to either a reduction in gate-drain spacing, or to an increase in field plate length. A more detailed analysis was carried out on this wafer. Specifically, we plotted the breakdown voltage as a function of the distance between the field plate head and the drain contact (defined as gap-spacing in the following), as shown in Fig. 6. As can be noticed, a) the real dependence is between the breakdown voltage and the gap spacing; b) this dependence holds both when the field plate length is constant, and the gate-drain spacing is varied (red squares), and when the gate-drain spacing is constant, and the field plate length is varied (blue triangles).

The key results reported above indicate that:

- a thinning of the SiO_2 dielectric can keep breakdown voltage in excess of 250 V for the reference geometry, while making the breakdown voltage more sensitive to geometry;
- the breakdown voltage depends on a trade-off between device scaling and field plate dimensions.

To evaluate the impact of SiO_2 dielectric thickness scaling on charge trapping, a detailed analysis based on pulsed measurements was carried out. Both forward gate stress and off-state stress were investigated. The results are reported in Fig. 7 (for the impact on threshold voltage) and Fig. 8 (for the impact on on-resistance).

In the figures, each point is referring to the average of three samples; measurements are taken after inducing trapping with different quiescent bias points (OFF-state pulse width = 100 μs, ON-state measuring pulse = 1 μs). Off-state stress is obtained with (V_{GS},V_{DS}) = (0 V, 0 V), (0 V, 10 V), …, i.e. with pinched-off channel and positive drain bias; gate stress is induced with (V_{GS},V_{DS}) = (0 V, 0 V), (1 V, 0 V), …, i.e. with a positive gate bias, and grounded drain. As can be noticed, a scaling of the dielectric thickness did not result in a worsening of the charge-trapping behavior. Under off-state bias, the devices did not show a significant variation in on-resistance and threshold voltage.

Some charge-trapping phenomena were observed under positive gate stress (see the threshold voltage charts on the bottom of Fig. 7); such processes are related to the trapping of electrons in the AlGaN barrier [20], and of holes at the p-GaN/AlGaN interface [21], and – being semiconductor-related – are independent of the dielectric

thickness. The results in Figs. 6 and 7 confirm that a scaling of dielectric is viable, and does not induce a worsening in the trapping properties of the devices.

4. Conclusions

In summary, we presented a detailed analysis of the impact of scaling on the robustness and charge trapping of GaN HEMTs for low-voltage applications, targeting the 100 V range. The results indicated that: a) a scaling of the SiO_2 dielectric thickness under the field plate is viable, and keeps the breakdown voltage at 250 V for the reference geometry; b) the breakdown voltage of devices with scaled dielectric shows a stronger sensitivity to the scaling of gate-drain spacing and field-plate length; c) the parameter that ultimately limits the breakdown voltage is the spacing between the field plate head and the drain contact. A trade-off for scaling can then be identified. d) Pulsed measurements revealed that scaling of the dielectric thickness does not result in additional charge trapping phenomena. In conclusion, the results of this paper provide relevant information for the scaling of GaN HEMTs for future applications in GaN-based ICs.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

All data shared in the paper has no precise indication on the gate length, gate-to-drain length and field plate. Data are confidential, but the analysis is performed in such a way to cover it.

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