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AC Grid–DC Microgrid Coupling with High-Performance Three-Phase Single-Stage Bidirectional Converters †

Ahmed Y. Farag [1], Tarek Younis [2], Davide Biadene [1] and Paolo Mattavelli [1,*]

[1] Department of Management and Engineering (DTG), University of Padova, 36100 Vicenza, Italy; ahmedyahiafarag.abdelfattah@phd.unipd.it (A.Y.F.); davide.biadene@unipd.it (D.B.)
[2] Department of Electrical Engineering, Aswan University, Aswan 81528, Egypt; tsayed@aswu.edu.eg
* Correspondence: paolo.mattavelli@unipd.it
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Abstract: This paper discusses bidirectional step-down topologies that enable the interface of the 400 V unipolar DC microgrid with the European low-voltage three-phase AC grid. The study compares three single-stage non-isolated topologies, namely, the seven-switch buck converter, Swiss converter, and Y-converter, based on semiconductor stresses and losses, magnetic component sizes and losses, and heat sink sizes. The analysis is conducted for a 10 kW converter designed for small commercial or residential use. The results indicate that the Y-converter has superior overall performance compared to the other topologies, making it a potentially better candidate for this application. A 10 kW prototype of the Y-converter is constructed. It is demonstrated to have a peak efficiency of 99.26% and an efficiency of 97.47% at the rated output power.

Keywords: DC microgrid; three-phase PFC rectifiers; seven-switch rectifier; Swiss rectifier; Y-converter

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1. Introduction

The rapid increase in the demand for electric energy, particularly in the electric vehicle market, poses significant challenges. Meeting this growing demand requires a corresponding expansion in electric energy generation, which can lead to environmental issues if traditional energy sources are relied upon. Hence, renewable energy sources present an ideal solution for addressing the surging demand while generating zero-carbon emissions. Furthermore, recent advancements in control approaches for renewable energy sources, particularly solar and wind sources, have facilitated the seamless integration of these renewable sources into the preexisting power networks [1–4].

One of the most promising solutions is the utilization of microgrids. Microgrids offer a means to meet local energy demands by connecting distributed power sources to distribution networks, eliminating the need for extensive expansion of costly centralized utility grids. Consequently, DC microgrid technology has emerged as an attractive solution for modern electrical grid systems due to its inherent compatibility with renewable energy sources, electric loads, and energy storage systems [5,6]. Typically, DC microgrids are interconnected with low- or medium-voltage utility grids, as displayed in Figure 1, to serve as a backup in situations where the load demand exceeds the generated power within the microgrid or to feed surplus-generated power from the microgrid back to the utility grid [7–9].

Several studies discussed the selection of the DC microgrid optimum voltage level [7,9–11]. The findings of these studies have demonstrated that the 400 V DC system yields superior outcomes in terms of system efficiency and necessitates fewer power conversions for connecting multiple energy sources and loads. This voltage level is particularly advantageous

for applications such as electric vehicle charging and distribution in residential or commercial buildings. When interconnecting a 400 V DC microgrid with the European low-voltage grid, which operates at a 400 V line-to-line voltage, the use of buck-type bidirectional power factor correction (PFC) converters is necessary [12].

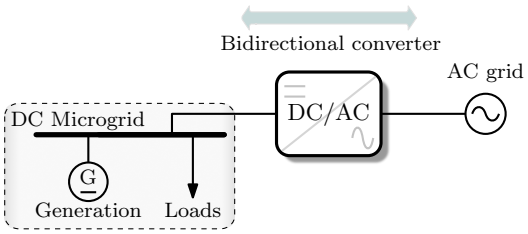

Figure 1. A bidirectional DC/AC converter connecting a DC microgrid to an AC grid.

Numerous topologies utilizing optimized modulation techniques have been proposed in the literature to attain an ultra-efficient power conversion in buck-type topologies. The first set of topologies is based on the conventional six-switch buck converter. In an effort to attain 99% efficiency, a design procedure for optimizing the six-switch buck converter is presented in [13]. Different optimized modulation techniques for this topology were explored in [14] to minimize switching losses and input capacitor voltage distortions. A further improvement to the six-switch buck converter is presented in [15,16], which is called the seven-switch buck converter. In the seven-switch converter, an additional freewheeling switch is employed to reduce conduction losses during the freewheeling mode. Bidirectional power capability for the above-mentioned topologies can be obtained using the anti-parallel configuration or using an inverting link [17,18]. A delta-type input current source converter with bidirectional capability is proposed in [19] to reduce the conduction losses of the six-switch converter.

The second set of topologies is based on employing an active third-harmonic current injection circuit such as the Swiss converter. The Swiss converter was presented in [20] and it demonstrated significant potential for achieving improved performance compared to the conventional six-switch converter. An ultra-high efficiency-interleaved Swiss converter with Silicon Carbide (SiC) devices is demonstrated in [21]. Modified modulation techniques for the Swiss converter are presented in [22,23] to improve grid current distortions. Moreover, an isolated Swiss converter is reported in [24], which employs full-bridge topology to the Swiss rectifier to attain both the soft switching and the high-frequency galvanic isolation. In addition to the Swiss converter, the hybrid active third-harmonic current injection converter was proposed and compared to the Swiss rectifier in [25], where the Swiss rectifier showed an overall better performance.

In addition to the conventional buck-type converters, the Y-converter, originally introduced in [26] for motor-drive applications, can be utilized to connect the AC grid with the DC microgrid. The Y-converter offers a bidirectional buck–boost capability and enables single-stage power conversion with a reduced number of semiconductor devices compared to traditional buck-type topologies. Consequently, the Y-converter emerges as a compelling choice for interfacing the AC grid with the DC microgrid.

In this paper, building upon [27], a comparative evaluation of bidirectional single-stage non-isolated buck-type topologies is conducted. The evaluated converters include the Y-converter, the seven-switch converter, and the Swiss converter. The operational principles of these topologies are discussed, followed by their evaluations based on various criteria: the number of semiconductors, semiconductor stresses and losses, magnetic element sizes and losses, and the size of the heat sink. This evaluation is carried out using an analytical power loss model and simulations. In comparison to [27], the magnetic element design and losses, along with the reverse recovery losses of the SiC MOSFETs, are included as part of the evaluation criteria. Additionally, a 10 kW prototype of the Y-converter is implemented to demonstrate its operation and high efficiency. The rest of this paper is structured as follows: The topology overview is discussed in Section 2. Analytical power loss models are

presented in Section 3. A comparative evaluation of the topologies is presented in Section 4. The experimental results are presented in Section 5. Finally, a conclusion is provided in Section 6.

2. Topology Overview

In this section, a brief discussion is provided on the three topologies, along with an explanation of their operational principles and the driving pulse schemes employed by each converter.

2.1. Y-Converter

Figure 2a illustrates the Y-converter topology. In the standard representation, the Y-converter can be viewed as a conventional three-phase boost voltage source converter with an additional pre-stage to incorporate the buck feature. In the modular representation, the Y-converter is constructed by connecting three four-switch buck–boost DC-DC converters in a star configuration, all connected to a common point (m). For the sake of simplicity, the analysis in this paper will utilize the modular representation.

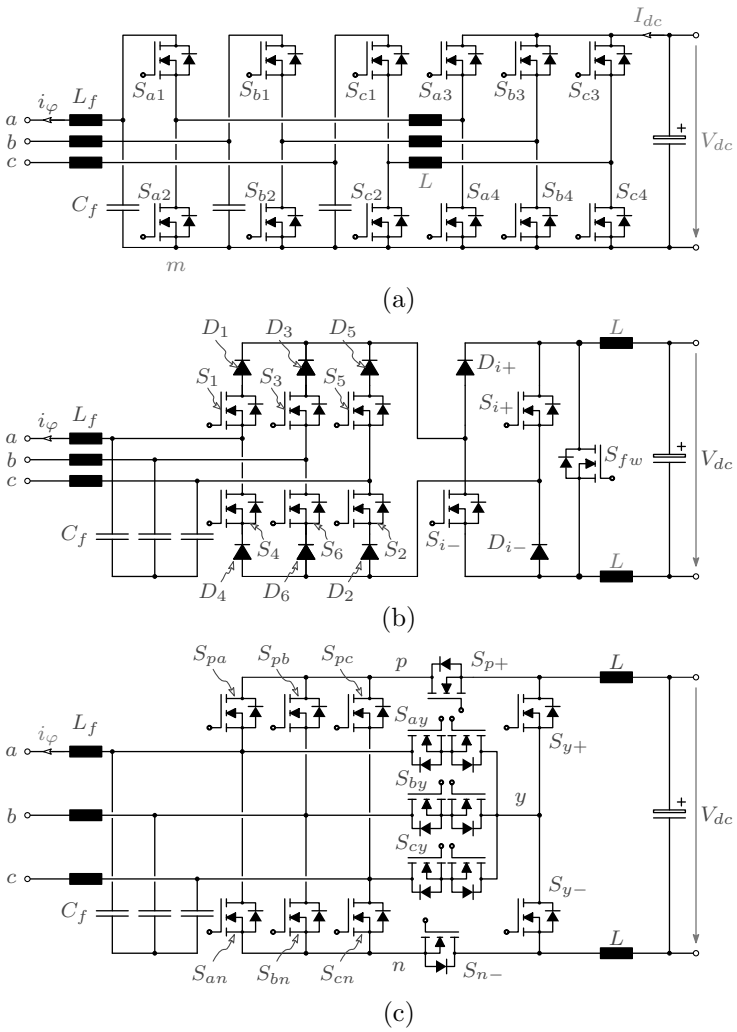

Figure 2. The three buck-type converters. (**a**) Y-converter; (**b**) seven-switch converter; and (**c**) Swiss converter.

Since each module functions as a DC-DC converter, it is essential to ensure a positive input voltage at the AC input of the modules ($V_{\{a,b,c\}m}$ must be kept ≥ 0 V). To achieve this, a suitable offset voltage must be established between the grid neutrals (n) and (m). Different pulse-width modulation (PWM) techniques can be employed based on the selected offset

voltage [26,28]. The PWM technique considered in this paper is the discontinuous PWM (DPWM), which provides a time-varying offset voltage represented by:

$$v_{off}(t) = -\min(v_a(t), v_b(t), v_c(t)) \tag{1}$$

where v_a, v_b, and v_c are the AC grid phase voltages.

The AC-side voltages (v_{am}, v_{bm}, and v_{cm}) of the three modules can be expressed as

$$\begin{aligned} v_{am} &= \hat{V}_m cos(\omega t) + v_{off} \\ v_{bm} &= \hat{V}_m cos\left(\omega t - \frac{2\pi}{3}\right) + v_{off} \\ v_{cm} &= \hat{V}_m cos\left(\omega t + \frac{2\pi}{3}\right) + v_{off} \end{aligned} \tag{2}$$

where $\hat{V}_m$ is the peak value of the phase voltages.

In DPWM, the module with the most-negative grid voltage is clamped to point m. This clamping mode has the advantage of eliminating both semiconductor switching losses and inductor core losses for the clamped module, resulting in a significant reduction in overall losses. During the remaining part of the fundamental cycle, one half-bridge (either the buck or boost) is subjected to pulse width modulation, while the other half-bridge is clamped. The choice of modulation depends on whether the AC-side module voltage is higher or lower than the DC-side voltage. The Y-converter modulation and the duty cycles of the switches are depicted in Figure 3a.

2.2. Seven-Switch Buck Converter

The seven-switch buck converter comprises three main parts: a three-phase bridge, a freewheeling switch, and an inverting link. In this paper, the three-phase bridge is created using a series combination of SiC MOSFETs and SiC diodes that enable current flow in one direction and voltage blocking in both directions.

The converter operation is analyzed using space vector PWM (SVPWM) [16] and involves six active space vectors and a zero (null) space vector. The zero-space vector is achieved by activating only the freewheeling switch, whereas in the traditional six-switch topology, the entire leg is turned on. During the freewheeling state, the seven-switch converter has the advantage of the DC link current flowing through a single semiconductor device S_{fw}, resulting in significantly reduced conduction losses compared to the four devices in the six-switch converter.

To enable bidirectional power capability, the inverting link is utilized to reverse the polarity of the DC-side voltage. In the rectification mode, the inverting link switches, such as S_{i+} and S_{i-}, are turned off, allowing power transfer from the AC side to the DC side through D_{i+} and D_{i-}. In the inversion mode, both S_{i+} and S_{i-} are turned on, creating a negative DC link that facilitates power transfer from the DC side to the AC side. The seven-switch buck converter modulation and the duty cycles of the switches are presented in Figure 3b.

2.3. Swiss Converter

The Swiss converter is composed of three primary stages: an active three-phase bridge, a third harmonic injection network, and two buck DC-DC converters. The three-phase bridge functions as an uncontrolled rectifier bridge, driven to operate in a typical manner.

The third harmonic injection network includes three four-quadrant switches and is controlled to actively inject current solely into the phase with the lowest instantaneous voltage. Switching losses in both the active bridge and the injection network are neglected since they operate at the grid frequency and twice the grid frequency, respectively. When combined, the active bridge and the injection network form a three-phase unfolder. This

three-phase AC unfolder converts the three-phase voltages into two DC voltages, namely v_{py} and v_{yn}, which are utilized by the two buck DC-DC converters. This configuration enables the control of grid currents and the DC-side voltage by solely manipulating the duty cycle of the buck converters.

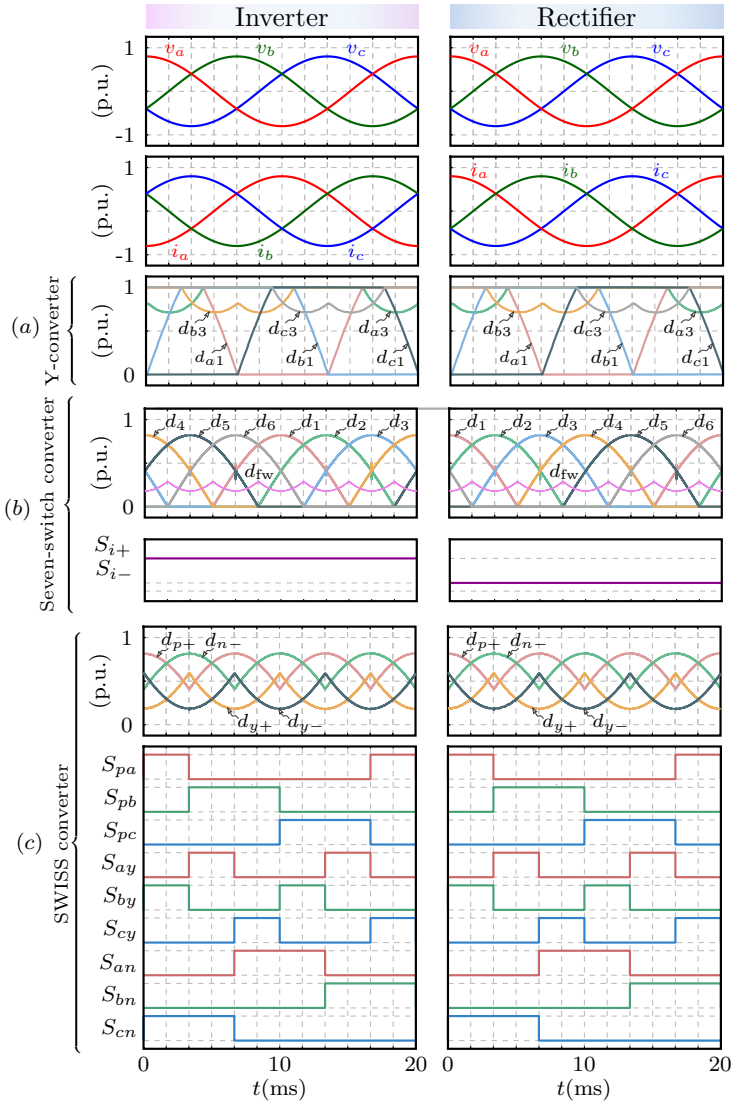

Figure 3. Modulation techniques for the three topologies. (**a**) Y-converter; (**b**) seven-switch converter; and (**c**) Swiss converter.

The duty cycles d_{p+} of switch S_{p+} and d_{n-} of switch S_{n-} are controlled in both the inverter and rectifier modes so that the AC-side current becomes sinusoidal. d_{p+} and d_{n-} can be calculated as follows:

$$\begin{aligned} d_{p+} &= \frac{2}{3}\frac{V_{dc}}{\hat{V}_m^2}\max(v_a, v_b, v_c) \\ d_{n-} &= \frac{2}{3}\frac{V_{dc}}{\hat{V}_m^2}\left|\min(v_a, v_b, v_c)\right| \end{aligned} \tag{3}$$

where V_{dc} is the DC link voltage. The Swiss converter modulation and the duty cycles of the switches are presented in Figure 3c.

3. Analytical Power Loss Model

To assess and compare the three topologies, an analytical model is developed to calculate power losses. The model takes into account various types of power losses, including conduction losses in semiconductors, switching losses in semiconductors, copper losses, and core losses in inductors. Table 1 summarizes the converter parameters and the specific semiconductors used. The model is based on the following assumptions:

1. The inductances in all converters are assumed to be constant for the whole operating power range;
2. The comparison is held at a fixed junction temperature for all devices (T_j = 25 °C);
3. The reverse recovery losses of the SiC Schottky diode are neglected as a zero-reverse recovery current diode is utilized;
4. The input filter (L_f, C_f) is fixed for all topologies; the EMI filter is not considered.

Table 1. Three-phase PFC rectifier parameters.

	Parameter	Symbol	Value	
Converter parameters [1]	Nominal power	P	10	kW
	AC line voltage	V_{ac}	400	V
	Line frequency	f	50	Hz
	Switching frequency	f_{sw}	62.5	kHz
	Output voltage	V_{dc}	400	V
SiC MOSFET	Part number		IMZ120R030M1H	
	Voltage	V_{DS}	1200	V
	Current	I_D	56	A
SiC Diode	Part number		C4D20120D	
	Voltage	V_{RRM}	1200	V
	Current	I_F	66	A
Input Filter	Inductor	L_f	50	μH
	Capacitor	C_f	11.3	μF

[1] The converter parameters are utilized in both the evaluation of the converters and the experimental prototype.

3.1. Semiconductor Conduction Losses

The conduction losses of power MOSFETs are calculated as follows:

$$P_{cond,sw} = I_{DS,RMS}^2 R_{DS,on} \tag{4}$$

where $I_{DS,RMS}$ is the RMS value of the MOSFET current, and these RMS values for the three topologies are summarized in Figure 4. $R_{DS,on}$ is the on-state resistance of the power MOSFET and it is assumed to vary with the junction temperature T_j according to the following equation:

$$R_{DS,on}(m\Omega) = a_0 + a_1 T_j + a_2 T_j^2 \tag{5}$$

The used fitting parameters for IMZ120R030M1H are:

$$a_0 = 29.78\ \text{m}\Omega, \quad a_1 = -0.01556\ \text{m}\Omega/^\circ\text{C}, \quad a_2 = 0.0009778 \times 10^{-4}\ \text{m}\Omega/^\circ\text{C}^2 \tag{6}$$

For the SiC diodes in the seven-switch converter, the conduction losses are calculated as follows:

$$P_{cond,D} = I_{D,rms}^2 R_{D,on} + I_{D,av} V_{D,on} \tag{7}$$

where $I_{D,rms}$ and $I_{D,av}$ are the RMS and the average values of the diode current, respectively. These values are summarized in Figure 4. $R_{D,on}$ and $V_{D,on}$ are the on-state resistance and

the on-state voltage of the power diode and they are assumed to vary with the junction temperature T_j, according to the following equations:

$$\begin{aligned} R_{D\,\text{on}}\,(m\Omega) &= b_0 + b_1 T_j \\ V_{D\,\text{on}}\,(\text{V}) &= c_0 + c_1 T_j \end{aligned} \tag{8}$$

The used fitting parameters for C4D20120D are:

$$b_0 = 20\ \text{m}\Omega,\ b_1 = 0.266\ \text{m}\Omega/C,\ c_0 = 0.98\ \text{V},\ c_1 = -1.71 \times 10^{-3}\ \text{V}/C \tag{9}$$

			Y-Converter		Seven-switch Converter			Swiss Converter		
Inductor	RMS		$I_{L,\text{RMS}} = \frac{I_{dc}}{4\sqrt{2}}\sqrt{12M^2 - \frac{16}{\sqrt{3}}M + 16}$		RMS	$I_{L,\text{RMS}} = \sqrt{I_{dc}^2 + \frac{\Delta I_l^2}{18}}$		RMS	$I_{L,\text{RMS}} = \sqrt{I_{dc}^2 + \frac{\Delta I_l^2}{18}}$	
Semiconductors current	$S_{\{a,b,c\}1}$	RMS	$\frac{I_{L,\text{RMS}}}{M}\sqrt{-\frac{M^2}{6} + \frac{20}{21}M - \frac{4\sqrt{3}}{9\pi}}$		$S_{1:6}$	RMS	$I_{dc}\sqrt{\frac{M}{\pi}}$	$S_{p\{a,b,c\}}$	RMS	$I_{dc}\sqrt{\frac{\sqrt{3}M}{2\pi}}$
	$S_{\{a,b,c\}2}$		$\frac{I_{L,\text{RMS}}}{M}\sqrt{\frac{7M^2}{6} - \frac{20}{21}M + \frac{4\sqrt{3}}{9\pi}}$		S_{fw}		$I_{dc}\sqrt{1 - \frac{3M}{\pi}}$	$S_{\{a,b,c\}n}$		$I_{dc}\sqrt{\frac{3\sqrt{3}M}{2\pi}}$
	$S_{\{a,b,c\}3}$		$\frac{I_{L,\text{RMS}}}{M}\sqrt{\left(1 + \frac{2}{\pi}\right)M^2 - \sqrt{\frac{2}{3}}M + \frac{4}{9\pi}}$		$S_{i+,i-}$		$\sqrt{3}I_{dc}\sqrt{\frac{M}{\pi}}$	$S_{y+,y-}$		$I_{dc}\sqrt{1 - \frac{3\sqrt{3}M}{2\pi}}$
	$S_{\{a,b,c\}4}$		$\frac{I_{L,\text{RMS}}}{M}\sqrt{-\frac{2}{\pi}M^2 + \sqrt{\frac{2}{3}}M - \frac{4}{9\pi}}$		$D_{1:6}$	Average	$I_{dc}M/\pi$	$S_{\{a,b,c\}y}$		$I_{dc}\sqrt{(2-\sqrt{3})M}$
					$D_{i+,i-}$		$3I_{dc}M/\pi$			

Figure 4. The current stresses of the different semiconductor devices in the three topologies.

3.2. Semiconductors Switching Losses

The calculation of switching losses relies on the utilization of switching energy loss E_{sw} versus drain-source current I_{DS} curves of the SiC MOSFETs. These curves can be obtained from the manufacturer's datasheet or through the implementation of a calorimetric switching loss measurement setup, as suggested in [29]. In this paper, two distinct polynomial fittings are employed to determine the turn-on energy loss $E_{sw,on}$ and the turn-off energy loss $E_{sw,off}$ individually. This separation allows for easy integration of soft switching into the power loss model whenever it occurs. The polynomial fitting equations for $E_{sw,on}$ and $E_{sw,off}$ are chosen to be fourth-order polynomials in order to minimize the root mean square error between the actual data and the fitted polynomials. The polynomial fitting equations can be expressed as:

$$E_{sw,\,\text{on}}\,(\text{mJ}) = V_{DS}\,(P_{1\,\text{on}}\,I_{DS\,\text{on}}^4 + P_{2\,\text{on}}\,I_{DS\,\text{on}}^3 + P_{3\,\text{on}}\,I_{DS\,\text{on}}^2 + P_{4\,\text{on}}\,I_{DS\,\text{on}}) \tag{10}$$

$$E_{sw,\,\text{off}}\,(\text{mJ}) = V_{DS}\,(P_{1\,\text{off}}\,I_{DS\,\text{off}}^4 + P_{2\,\text{off}}\,I_{DS\,\text{off}}^3 + P_{3\,\text{off}}\,I_{DS\,\text{off}}^2 + P_{4\,\text{off}}\,I_{DS\,\text{off}}) \tag{11}$$

where $I_{DS,on}$ and $I_{DS,off}$ represent the instantaneous values of the MOSFET turn-on and turn-off currents, respectively, and V_{DS} represents the instantaneous value of the MOSFET voltage. It is assumed that V_{DS} remains constant during the turn-on and turn-off at every instant. The fitting parameters for IMZ120R030M1H are as follows:

$$\begin{aligned} P_{1\,\text{on}} &= -7.2730 \times 10^{-10}\ \text{A}^{-3}.\text{ms}; & P_{1\,\text{off}} &= -5.4688 \times 10^{-10}\ \text{A}^{-3}.\text{ms} \\ P_{2\,\text{on}} &= +7.0371 \times 10^{-8}\ \text{A}^{-2}.\text{ms}; & P_{2\,\text{off}} &= +5.2350 \times 10^{-8}\ \text{A}^{-2}.\text{ms} \\ P_{3\,\text{on}} &= -2.1250 \times 10^{-6}\ \text{A}^{-1}.\text{ms}; & P_{3\,\text{off}} &= -1.4412 \times 10^{-6}\ \text{A}^{-1}.\text{ms} \\ P_{4\,\text{on}} &= +3.6750 \times 10^{-5}\ \text{ms}; & P_{4\,\text{off}} &= +1.5450 \times 10^{-5}\ \text{ms} \end{aligned} \tag{12}$$

Given the switch voltage and current at the turn-on and turn-off instances, the switching energy is calculated using (10) and (11), then the switching losses are calculated.

In addition to the switching losses during the first quadrant operation of SiC MOSFETs, the power loss model includes switching losses during the third quadrant operation, i.e., the synchronous rectification mode. We assume that the turn-on switching losses in the synchronous rectifier mode are negligible, while at turn-off, power loss occurs due to the reverse recovery of the integral body diode. The switching energy losses due to reverse recovery ($E_{sw_{rr}}$) can be represented as functions of I_{ds} and V_{sw} [30] based on the following polynomial fitting:

The fitting parameters for IMZ120R030M1H are as follows:

$$E_{sw_{rr}}(\text{mJ}) = V_{DS}\left(P_{1_{rr}} I_{sw_{off}}^2 + P_{2_{rr}} I_{sw_{off}} + P_{3_{rr}}\right) \tag{13}$$

$$\begin{aligned} P_{1_{rr}} &= +1.4037 \times 10^{-8}\ \text{A}^{-1}.\text{ms} \\ P_{2_{rr}} &= +1.1225 \times 10^{-5}\ \text{ms} \\ P_{3_{rr}} &= +2.8075 \times 10^{-6}\ \text{A.ms} \end{aligned} \tag{14}$$

3.3. Inductor Losses

The power inductor L is designed to provide the same inductor current ripple percentage at the rated power for all topologies ($\Delta I_{Lp} = 20\%$). It can be calculated for the Y-converter as follows [28]:

$$L = \frac{V_{dc}}{8\sqrt{2}\Delta I_{Lp} I_{\varphi} f_{sw}} \tag{15}$$

For the Swiss and seven-switch converters [13,20]:

$$L = \frac{V_{dc}}{2\Delta I_{Lp} I_{dc} f_{sw}}\left(1 - \frac{\sqrt{3}}{2M}\right) \tag{16}$$

where M is the modulation index and can be expressed as follows:

$$M = \sqrt{2}\,\frac{\hat{I_{\varphi}}}{I_{dc}} = \frac{2\,V_{dc}}{3\,V_m} \tag{17}$$

where I_{dc} is the DC-side current and $\hat{I_{\varphi}}$ is the RMS value of the AC-side phase current.

At the given M ($\approx$0.8165), previous equations result in almost the same value of L ($\approx$190 μH) for the investigated topologies.

The power loss of L is divided into copper losses and core losses. For the copper losses, due to employing Litz wires to implement the inductor, skin effects and high-frequency losses can be neglected. Therefore, the copper losses are limited to the DC copper losses, which can be calculated as follows:

$$P_{cu} = I_{Lrms}^2 R_{LDC} \tag{18}$$

where R_{LDC} is the DC resistance of L.

The core loss is calculated based on the curve-fitting equations provided by the manufacturer [31]. The provided fitting equations represent experimentally measured magnetic property curves using closed-form equations. These equations facilitate the seamless integration of these magnetic properties into the power loss model. Starting from the maximum and minimum currents of the inductor at different instances, $I_{Lmax,i}$, $I_{Lmin,i}$, the corresponding values of magnetic flux intensity (H) and magnetic flux density (B) can be calculated as follows:

$$H = \frac{0.4\pi N I_L}{100\ \text{MPL}} \tag{19}$$

$$B = \left[\frac{a + bH + cH^2}{1 + dH + eH^2}\right]^x \tag{20}$$

where N is the number of turns, MPL is the magnetic path length in meters (m), H is in Oersted (Oe), and B is in Tesla (T). a, b, c, d, e, and x are the fitting parameters of the B-H curves provided by the manufacturer. The values of these fitting parameters are summarized in Table 2.

The core losses at a specific instant can be given by:

$$P_{core} = V_c \times a_{Loss} \times (B_{max} - B_{min})^{b_{Loss}} \left(\frac{f_{sw}}{1000}\right)^{c_{Loss}} \tag{21}$$

where V_c is the magnetic core volume in m^3. a_{Loss}, b_{Loss}, and c_{Loss} are the fitting parameters for the core loss curves provided by the manufacturer. The inductor parameters along with the core loss fitting parameters are summarized in Table 2.

Table 2. Inductor parameters.

	Parameter	Symbol	Value
Inductor Parameters	Part number		KoolMu 0079908A7
	Magnetic path length	MPL	19.6 cm
	Core volume	V_c	43.4 cm^3
	Number of turns	N	80 Turns
	Inductor DC resistance	R_{LDC}	20.3 mΩ
Fitting Parameters	**Flux density B Equation (20)**	a	3.763×10^{-2} T
		b	1.712×10^{-2} T/Oe
		c	5.155×10^{-4} T/Oe^2
		d	9.190×10^{-2} Oe^{-1}
		e	4.909×10^{-4} Oe^{-2}
		x	1.812
	Core losses P_{core} Equation (21)	a_{Loss}	52.36J/($T.m^3$)
		b_{Loss}	1.988
		c_{Loss}	1.541

4. Comparative Analysis

4.1. Semiconductors Stresses

4.1.1. Voltage Stresses

In the three topologies, the maximum voltage stress on semiconductor devices is represented by three distinct values: the peak line-to-line grid voltage (566 V), the DC microgrid voltage (400 V), and the voltage at the natural commutation points of the line-to-line grid voltage (537 V). The 537 V peak voltage applies to the AC-side SiC MOSFETs ($S_{\{a,b,c\}1}$ and $S_{\{a,b,c\}2}$) in the Y-converter, the three-phase bridge devices ($S_{1:6}$ and $D_{1:6}$) in the seven-switch converter, and the three-phase bridge devices ($S_{1:6}$) in the Swiss converter. The 400 V peak voltage is applicable to the remaining devices in the Y-converter and the seven-switch converter, while the 537 V peak voltage applies to the remaining devices in the Swiss converter. The voltage stresses of the three topologies are summarized in Figure 5.

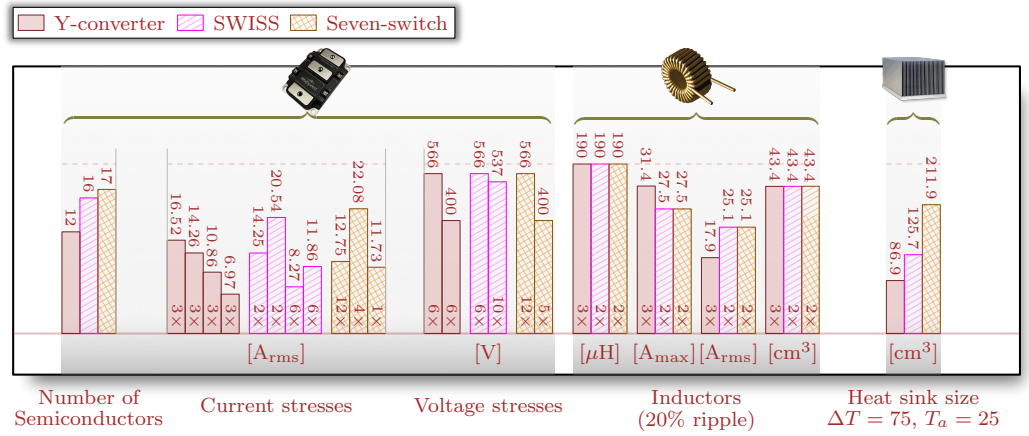

Figure 5. Comparison between the three topologies in terms of the number of semiconductors, semiconductor stresses and losses, the size of the heat sink, and the magnetic element sizes.

4.1.2. Current Stresses

The formulas for the current stresses of the semiconductor devices in the three topologies are summarized in Figure 4. Additionally, The current stresses at 10 kW are summarized in Figure 5.

In order to provide deeper insight into the current stresses of the investigated topologies, the summation of the squared RMS currents of semiconductor devices in the investigated topologies are depicted in Figure 6. According to the obtained outcomes, the Y-converter exhibits the lowest summation across the entire power range. This implies that the Y-converter necessitates semiconductor devices with a lower current rating in comparison to the seven-switch and Swiss converters. Furthermore, if the same SiC devices are employed for all three topologies, the Y-converter will incur the least conduction losses at any given power level.

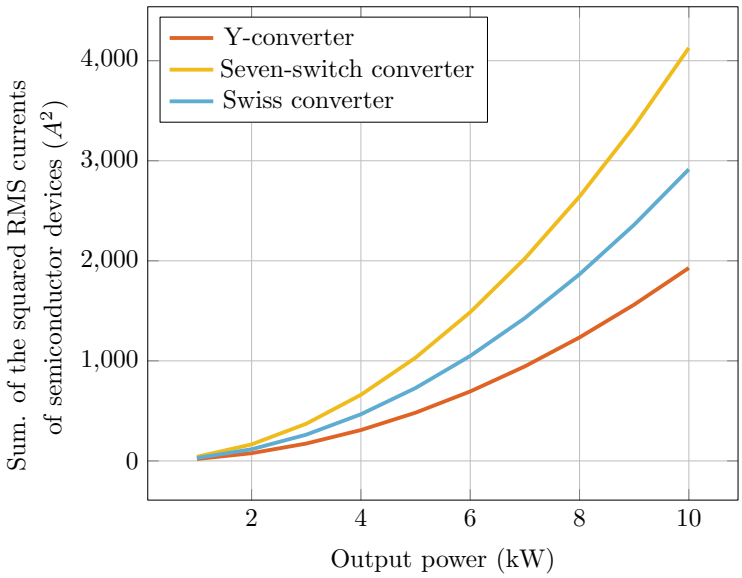

Figure 6. Summation of the squared RMS currents of semiconductor devices of the studied topologies.

4.2. Semiconductors Losses

4.2.1. Conduction Losses

The conduction losses of the topologies are illustrated in Figure 7a. The Y-converter exhibits the lowest conduction losses throughout the entire operating range. This is primarily due to its minimal number of series switches in the current path for rectification and inversion. On the other hand, the seven-switch converter experiences the highest

conduction losses. This can be attributed to the presence of SiC diodes and the excessive current stresses on the inverting link devices.

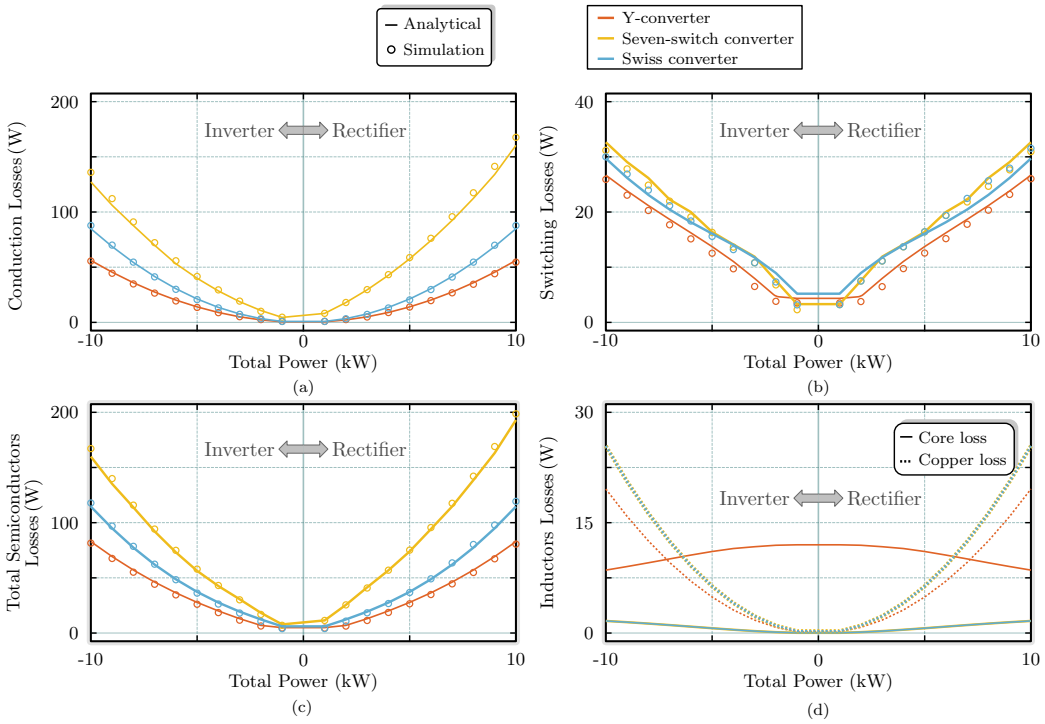

Figure 7. Comparison between the three topologies in terms of the semiconductor losses and inductor losses across the entire power operation range. Subfigures (**a**–**d**) depict different loss components: conduction losses, switching losses, semiconductor losses, and inductor losses, respectively.

4.2.2. Switching Losses

The switching losses of the topologies are depicted in Figure 7b. In the Y-converter, the use of DPWM leads to a significant reduction in switching losses. Additionally, only a single leg in each module undergoes commutation at any given time, further contributing to lower losses. In the Swiss converter, although the switching losses are confined to the fast switches (S_{p+} and S_{n-} in the rectification mode and S_{y+} and S_{y-} in the inversion mode), they are considerably high due to their operation under high currents. Given the semiconductor conduction and switching losses of the studied topologies, the total semiconductor losses are plotted in Figure 7c.

4.3. Inductor Losses

The inductor losses of the topologies are plotted in Figure 7d. Although the core losses in the Y-converter are reduced by employing DPWM, the Y-converter demonstrates the highest core losses among the studied topologies. The inductors in the Swiss converter and the seven-switch converters yield the same losses and sizes. The copper losses in the Y-converter are reduced as the total current is shared between the three phases, unlike the other topologies, where the total output current flows through the inductors.

5. Experimental Results

To demonstrate the operation and high efficiency of the Y-converter, a 10 kW prototype of the Y-converter was implemented. The experimental setup is displayed in Figure 8. The experimental results are categorized as follows: key waveforms of the Y-converter, along with the measured THD of the AC side currents, and the measured efficiency of the converter, with its corresponding calculated power loss breakdown.

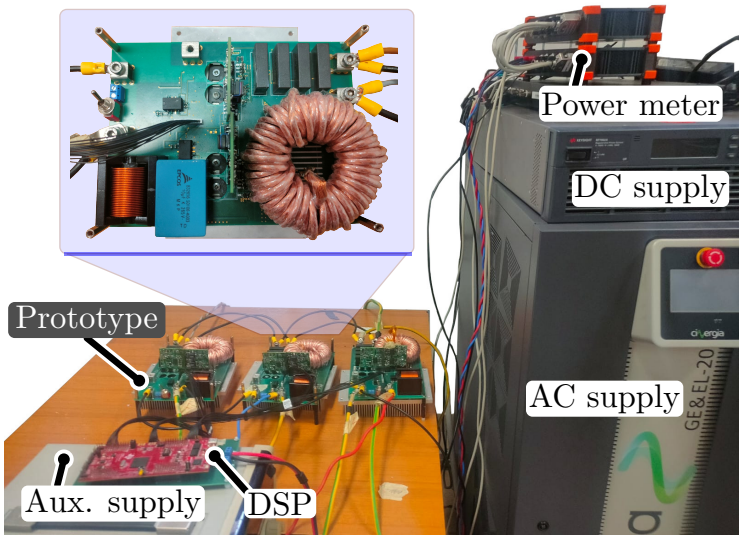

Figure 8. Picture of the Y-converter prototype.

5.1. Key Waveforms and AC Current THDs

The selected key waveforms of the Y-converter are the AC-side voltage V_{am}, the grid voltage V_{an}, the inductor current I_{La}, and the grid current I_a. Experimental results under full loads for both rectification and inversion modes are displayed in Figures 9 and 10, respectively. The results show that the clamping mode is verified where $V_{am} = 0$ V, and I_{La} is shown to be ripple-free during clamping while preserving the sinusoidal shapes of both I_{La} and I_a. The THDs of I_a at different output power levels are presented in Figure 11 with 3.8% at the converter's rated output power.

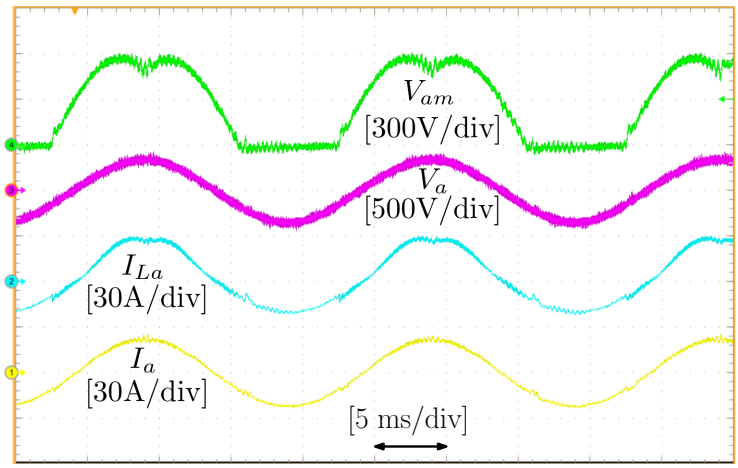

Figure 9. Key waveforms of the rectification mode at rated power.

5.2. Measured Efficiency and Power Loss Breakdown

The efficiency of the prototype is measured using the Dewesoft SIRIUS XHS high-speed data acquisition (DAQ) system. The efficiency curve is plotted in Figure 11, which shows that the converter has a peak efficiency of 99.26% at nearly 40% of the rated power and 97.49% efficiency at the rated power.

Based on the previously discussed power loss model and the measured temperatures of the semiconductor devices during experimental tests, the calculated power loss breakdown for a half load and full load are displayed in Figure 12. At a half load, the semiconductor losses represent almost 60% of the total losses with a roughly equalized distribution between conduction losses and switching losses. At a full load, the conduction loss contribution to the total losses is estimated to be 51%, which explicitly means that using another SiC

device with a lower $R_{DS,on}$ can lead to better efficiency at a full load. The "other losses", represented in the loss breakdown figure, is a generic term that represents the losses that are not included in the calculations, such as PCB losses, capacitor losses, etc., along with the mismatch between the calculated losses and the actual losses.

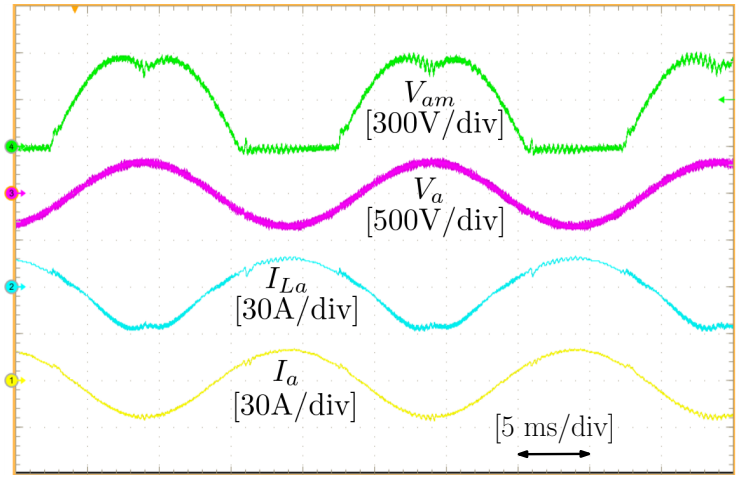

Figure 10. Key waveforms of the inversion mode at rated power.

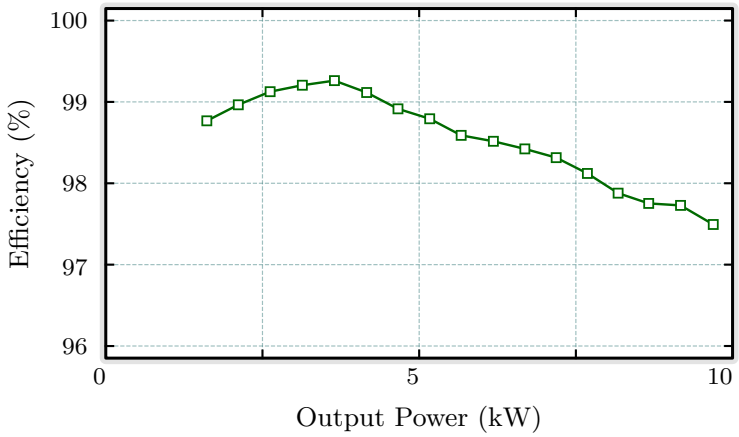

Figure 11. Measured efficiency of the prototype.

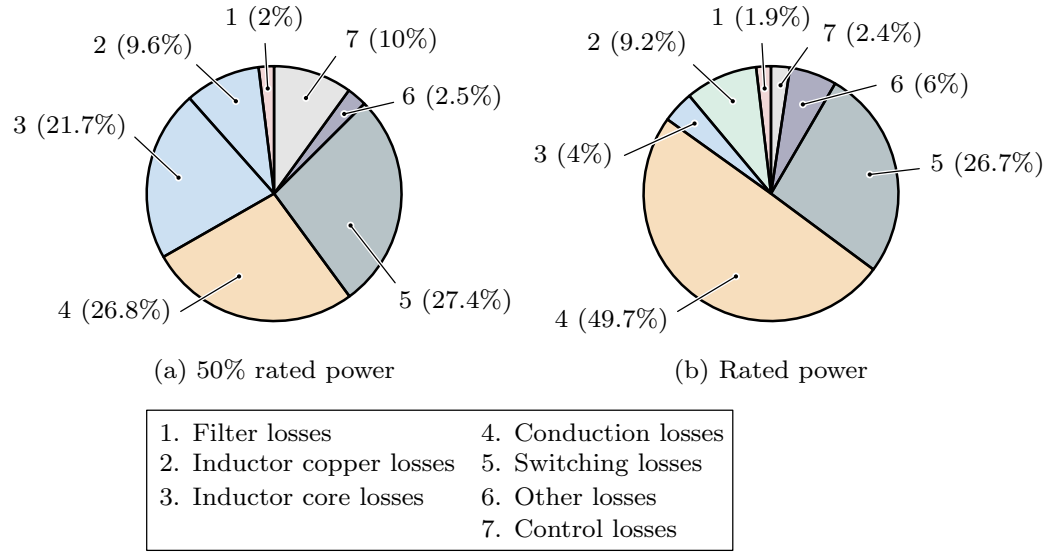

Figure 12. Loss Breakdown.

6. Discussion and Conclusions

This paper evaluates bidirectional step-down converters that enable the connection between the 400 V unipolar DC microgrid and the European low-voltage three-phase AC grid. The study compares three single-stage non-isolated topologies—the seven-switch buck converter, Swiss converter, and Y-converter—based on various factors, such as semiconductor stresses and losses, magnetic component sizes and losses, and heat sink sizes. The analysis is centered on a 10 kW converter that is suitable for residential or commercial use. The results indicate that the Y-converter has the lowest number of semiconductor devices, semiconductor device stresses, total losses, and heat sink sizes. The only drawback is that the total inductor size in the Y-converter is larger than those of the other studied topologies. Based on the findings, the Y-converter performs better overall than the other topologies, making it a potentially more suitable option for this application. A 10 kW Y-converter prototype is implemented and shown to have a peak efficiency of 99.26% and an efficiency of 97.47% at the rated output power. For future research, multi-objective optimization could be adopted for designing passive elements and selecting semiconductor devices. Subsequently, the topologies could be evaluated accordingly. This approach would offer a more comprehensive perspective on comparisons across various converter parameters, such as switching frequencies, inductor current ripples, and semiconductor device ratings. Additionally, investigating control strategies for each topology and evaluating their impacts on performances, losses, and efficiency could provide insight into the influence of these strategies on the converter's behavior. This analysis would help identify opportunities for optimization.

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Data Availability Statement: The most important data are included in the figures and tables, and the method is described so that no additional data are available.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

PFC	power factor correction
SiC	silicon carbide
PWM	pulse width modulation
DPWM	discontinuous pulse width modulation
SVPWM	space vector pulse width modulation

References

1. Kulasekaran, P.S.; Dasarathan, S. Design and Analysis of Interleaved High-Gain Bi-Directional DC-DC Converter for Microgrid Application Integrated with Photovoltaic Systems. *Energies* **2023**, *16*, 5135. [CrossRef]
2. Murshed, M.; Chamana, M.; Schmitt, K.E.K.; Bhatta, R.; Adeyanju, O.; Bayne, S. Design and Performance Analysis of a Grid-Connected Distributed Wind Turbine. *Energies* **2023**, *16*, 5778. [CrossRef]
3. Yan, S.; Gu, Z.; Park, J.H.; Xie, X. Adaptive Memory-Event-Triggered Static Output Control of T–S Fuzzy Wind Turbine Systems. *IEEE Trans. Fuzzy Syst.* **2022**, *30*, 3894–3904. [CrossRef]
4. Yan, S.; Gu, Z.; Park, J.H.; Xie, X. Sampled Memory-Event-Triggered Fuzzy Load Frequency Control for Wind Power Systems Subject to Outliers and Transmission Delays. *IEEE Trans. Cybern.* **2023**, *53*, 4043–4053. [CrossRef] [PubMed]
5. Pires, V.F.; Pires, A.; Cordeiro, A. DC Microgrids: Benefits, Architectures, Perspectives and Challenges. *Energies* **2023**, *16*, 1217. [CrossRef]

6. Ali, S.; Zheng, Z.; Aillerie, M.; Sawicki, J.P.; Péra, M.C.; Hissel, D. A Review of DC Microgrid Energy Management Systems Dedicated to Residential Applications. *Energies* **2021**, *14*, 4308. [CrossRef]
7. Kumar, D.; Zare, F.; Ghosh, A. DC Microgrid Technology: System Architectures, AC Grid Interfaces, Grounding Schemes, Power Quality, Communication Networks, Applications, and Standardizations Aspects. *IEEE Access* **2017**, *5*, 12230–12256. [CrossRef]
8. Prabhala, V.A.; Baddipadiga, B.P.; Fajri, P.; Ferdowsi, M. An Overview of Direct Current Distribution System Architectures and Benefits. *Energies* **2018**, *11*, 2463. [CrossRef]
9. Dragičević, T.; Lu, X.; Vasquez, J.C.; Guerrero, J.M. DC Microgrids—Part II: A Review of Power Architectures, Applications, and Standardization Issues. *IEEE Trans. Power Electron.* **2016**, *31*, 3528–3549. [CrossRef]
10. Elsayed, A.T.; Mohamed, A.A.; Mohammed, O.A. DC microgrids and distribution systems: An overview. *Electr. Power Syst. Res.* **2015**, *119*, 407–417. [CrossRef]
11. Justo, J.J.; Mwasilu, F.; Lee, J.; Jung, J.W. AC-microgrids versus DC-microgrids with distributed energy resources: A review. *Renew. Sustain. Energy Rev.* **2013**, *24*, 387–405. [CrossRef]
12. Kolar, J.W.; Friedli, T. The Essence of Three-Phase PFC Rectifier Systems—Part I. *IEEE Trans. Power Electron.* **2013**, *28*, 176–198. [CrossRef]
13. Stupar, A.; Friedli, T.; Minibock, J.; Kolar, J.W. Towards a 99% Efficient Three-Phase Buck-Type PFC Rectifier for 400-V DC Distribution Systems. *IEEE Trans. Power Electron.* **2012**, *27*, 1732–1744. [CrossRef]
14. Baumann, M.; Kolar, J. Comparative evaluation of modulation methods for a three-phase/switch buck power factor corrector concerning the input capacitor voltage ripple. In Proceedings of the 2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230), Vancouver, BC, Canada, 17–21 June 2001; Volume 3, pp. 1327–1332. [CrossRef]
15. Lorenzani, E.; Immovilli, F.; Migliazza, G.; Frigieri, M.; Bianchini, C.; Davoli, M. CSI7: A Modified Three-Phase Current-Source Inverter for Modular Photovoltaic Applications. *IEEE Trans. Ind. Electron.* **2017**, *64*, 5449–5459. [CrossRef]
16. Wang, W.; Gao, F.; Yang, Y.; Blaabjerg, F. Operation and Modulation of H7 Current-Source Inverter with Hybrid SiC and Si Semiconductor Switches. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *6*, 387–399. [CrossRef]
17. Vancu, M.F.; Soeiro, T.; Mühlethaler, J.; Kolar, J.W.; Aggeler, D. Comparative evaluation of bidirectional buck-type PFC converter systems for interfacing residential DC distribution systems to the smart grid. In Proceedings of the IECON 2012—38th Annual Conference on IEEE Industrial Electronics Society, Montreal, QC, Canada, 25–28 October 2012; pp. 5153–5160. [CrossRef]
18. Soeiro, T.B.; Heldwein, M.L. Bidirectional three-phase PFC concept based on an integrated inverting-link current source converter. In Proceedings of the 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, USA, 15–19 September 2013; pp. 5137–5144. [CrossRef]
19. Guo, B.; Wang, F.; Aeloiza, E. A novel three-phase current source rectifier with delta-type input connection to reduce the device conduction loss. *IEEE Trans. Power Electron.* **2016**, *31*, 1074–1084. [CrossRef]
20. Soeiro, T.B.; Friedli, T.; Kolar, J.W. Design and Implementation of a Three-Phase Buck-Type Third Harmonic Current Injection PFC Rectifier SR. *IEEE Trans. Power Electron.* **2013**, *28*, 1608–1621. [CrossRef]
21. Schrittwieser, L.; Leibl, M.; Haider, M.; Thöny, F.; Kolar, J.W.; Soeiro, T.B. 99.3% Efficient Three-Phase Buck-Type All-SiC SWISS Rectifier for DC Distribution Systems. *IEEE Trans. Power Electron.* **2019**, *34*, 126–140. [CrossRef]
22. Schrittwieser, L.; Kolar, J.W.; Soeiro, T.B. Novel SWISS Rectifier Modulation Scheme Preventing Input Current Distortions at Sector Boundaries. *IEEE Trans. Power Electron.* **2017**, *32*, 5771–5785. [CrossRef]
23. Chen, R.; Yao, Y.; Zhao, L.; Xu, M. Inhibiting mains current distortion for SWISS Rectifier—A three-phase buck-type harmonic current injection PFC converter. In Proceedings of the 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 15–19 March 2015; pp. 1850–1854. [CrossRef]
24. Zhang, B.; Xie, S.; Li, Z.; Zhao, P.; Xu, J. An Optimized Single-Stage Isolated Swiss-Type AC/DC Converter Based on Single Full-Bridge with Midpoint-Clamper. *IEEE Trans. Power Electron.* **2021**, *36*, 11288–11297. [CrossRef]
25. Soeiro, T.B.; Vancu, F.; Kolar, J.W. Hybrid Active Third-Harmonic Current Injection Mains Interface Concept for DC Distribution Systems. *IEEE Trans. Power Electron.* **2013**, *28*, 7–13. [CrossRef]
26. Antivachis, M.; Bortis, D.; Schrittwieser, L.; Kolar, J.W. Three-phase buck-boost Y-inverter with wide DC input voltage range. In Proceedings of the 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 4–8 March 2018; pp. 1492–1499. [CrossRef]
27. Farag, A.Y.; Younis, T.; Mattavelli, P.; Biadene, D. AC Grid-interface Bidirectional Buck-Type Converters for DC microgrids: A Comparative Study. In Proceedings of the IECON 2022—48th Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium, 17–20 October 2022; pp. 1–6. [CrossRef]
28. Antivachis, M.; Kleynhans, N.; Kolar, J.W. Three-Phase Sinusoidal Output Buck-Boost GaN Y-Inverter for Advanced Variable Speed AC Drives. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *10*, 3459–3476. [CrossRef]
29. Rothmund, D.; Bortis, D.; Kolar, J.W. Accurate Transient Calorimetric Measurement of Soft-Switching Losses of 10-kV SiC mosfets and Diodes. *IEEE Trans. Power Electron.* **2018**, *33*, 5240–5250. [CrossRef]

30. Sochor, P.; Huerner, A.; Hell, M.; Elpelt, R. Understanding the Turn-off Behavior of SiC MOSFET Body Diodes in Fast Switching Applications. In *PCIM Europe Digital Days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*; Mesago Messe Frankfurt GmbH: Stuttgart, Germany, 2021; pp. 1–8.
31. Magnetics Inc. Magnetics Powder Cores Catalog. 2020. Available online: https://www.mag-inc.com/Media/Magnetics/File-Library/Product%20Literature/Powder%20Core%20Literature/Magnetics-Powder-Core-Catalog-2020.pdf?ext=.pdf (accessed on 12 August 2023).