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Development of High-Performance Converters for Emerging Automotive Power Distribution Architectures

Tesi redatta con il contributo finanziario di Infineon Technologies Italia S.r.l.

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Abstract

Due to concerns about energy security and global warming, all major vehicle markets in the world have adopted efficiency or CO₂ requirements. Manufacturers that continue to focus on internal combustion engines must adopt much more extensive technology solutions to satisfy the more stringent 2025 and 2030 targets. The mild-hybrid technology offers the potential to reduce fuel consumption and CO₂ emissions more cost-effectively while saving weight and package space. However, a mild-hybrid electric vehicle (MHEV) – with its two electric networks consisting of the high voltage 48 V hybrid system and the low voltage 12 V circuit – has only recently gained a considerable market share. This is partially due to the large variety of possible mild-hybrid system architectures, each with different costs and benefits. Since both the 48 V and 12 V batteries and their buses coexist in battery-connected architectures and they interact to provide power supply to a variety of electronic loads, the development of a methodology to systematically evaluate all their possible configurations in terms of efficiency, total volume, and the cost is required. Such crucial task is further complicated by the difficulty to compare different architectural solutions, as this entails the capability to systematically enumerate the possible configurations, and to set up a methodology for their comparative evaluation.

The first part of this dissertation focuses on a specific case study treated numerically concerning the 48 V/12 V low-power battery-connected automotive scenarios where the purpose is to provide power supply to a variety of low-power electronic loads, *such as* sensors, microcontrollers, and communication transceivers (CAN). A novel architecture enumeration methodology – called constrained bucking trees (CBT) – is first proposed, assuming the presence of a single battery (*e.g.* 48 V) to sustain the whole system and modeling the latter following a tree-like approach. All the valid configurations for the considered

battery-connected architecture are then ranked in terms of efficiency, total footprint area and cost highlighting the best solution for the considered case study. Next, architectural solutions based on the use of buck converters only are compared with variants employing dedicated topologies for high step-down (HSD) conversion (*e.g.* 48 V-1 V), as well as fixed conversion ratio stages based on switched-capacitor (SC) converters. It is proved that the use of efficient HSD and SC stages leads to more efficient architectures, although in general still not cost-competitive with traditional ones due to the absence of highly integrated commercial solutions.

This first part prepares the ground to focus on specific blocks involved in the battery-connected architecture. The central part of the work focuses on the analysis, design and implementation of the isolated dc-dc converter connected under the 12 V battery and used to provide galvanic isolation between the two voltage domains. Presently adopted solutions at the industry level are based on the flyback topology with Silicon devices, a poorly efficient solution mostly justified by its low component count and reduced footprint. For this reason, a 2 MHz, 12 V, 600 mA, GaN-based active-clamped isolated SEPIC converter (ACISC) supporting full zero-voltage switching (ZVS) throughout the 9 V-18 V automotive range, is here considered a viable substitute for the battery-connected application. Designed for resonant discontinuous conduction mode (DCM) operation – which represents the novelty of this work – and leveraging the high switching frequency enabled by Gallium Nitride (GaN) devices, the selected topology leads to a reduction in total magnetic size and footprint, while maintaining a high efficiency profile as required by the automotive market. Both the theoretical model specifically developed for full ZVS resonant DCM operation, as well as the design and implementation of the transformer, are discussed. In addition, the advantages coming from the selected operating mode are highlighted and compared with the other possible ones while proving better performances once the designed 2 MHz ACISC is compared with a commercial flyback converter intended for the same application. The goal of the work presented herein is also to identify the main loss sources involved in the designed GaN-based ACISC, showing that the largest loss contribution is associated with the transformer, and in particular with primary winding losses to be attributed to skin and proximity effects in the MHz range. This result leads to the next part of this study, where

the magnetics involved in the converter – realized as a planar structure for lower profiles than conventional wire-wound components – are improved via a step-by-step optimization technique showing better results in terms of efficiency profile and in-circuit noise.

The purpose of the last activity is to compare the designed ACISC with a similar GaN-based topology, *such as* the active-clamped isolated flyback converter (ACIFC), since a more truthful comparison to the considered commercial flyback converter is now made between topologies running in the MHz range, hosting the same devices, and operating with the same resonant DCM operation. This study, which aims at showing the advantages and disadvantages of the two topologies, reveals significant better performances for the ACISC due to lower voltage stress across the switches and lower conduction and transformer winding losses.

To conclude, the three investigated topologies – ACISC, ACIFC, and flyback – are compared in terms of temperature and electromagnetic interference (EMI) noise by considering the limits set by the automotive standard CISPR25. Focusing on the EMI results obtained for the two active-clamped topologies, the ACISC still provides better performances than ACIFC due to the presence of the input inductor which acts as a filter. All developed results regarding the three isolated dc-dc converters are validated in simulation and experimentally on custom prototypes.

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Chapter 1

Introduction

Nowadays, fossil fuels are the best on-board energy sources in vehicles in terms of energy density and refueling time [1]. However, the high increase of global temperature in recent years due to climate change has forced regulatory authorities around the world to establish strict regulations on the CO₂ emissions [2]. As reported in [3], energy-related and industrial process CO₂ emissions rebounded by 1.9 gigatonnes (Gts) in 2021 – the largest ever annual rise in emissions – with global CO₂ emissions in 2021 totalling 36.6 Gt. In the stated policies scenario (STEPS), which shows the trajectory implied by today’s policy settings, CO₂ emissions reach a plateau in the mid-2020s at 37 Gt and thereafter fall slowly to 32 Gt by 2050, as shown in Fig. 1-1. This decline represents a break in the close historical relationship between growth in gross domestic product and growth in emissions, and it highlights the progress made since the Paris Agreement¹ in 2015. Prior to that, as reported in Fig. 1-1, the trajectory based on current policies was for CO₂ emissions to rise to more than 50 Gt by 2050, leading to a median global average surface temperature rise of around 3.5 °C by year 2100. The STEPS indicates a trajectory that would lead to a 2.5 °C temperature rise in 2100 due to changes in policies and technologies made since 2015 which have already reduced the projected long-term temperature rise by around 1 °C by 2100. However, the STEPS trajectory is not an adequate answer to the challenge of climate change because it would

¹The Paris Agreement is a legally binding international treaty on climate change. It was adopted by 196 Parties at the United Nations Climate Change Conference (COP21) in Paris, France, on 12 December 2015. Its overarching goal is to hold “the increase in the global average temperature to well below 2 °C above pre-industrial levels” and pursue efforts “to limit the temperature increase to 1.5 °C above pre-industrial levels”.

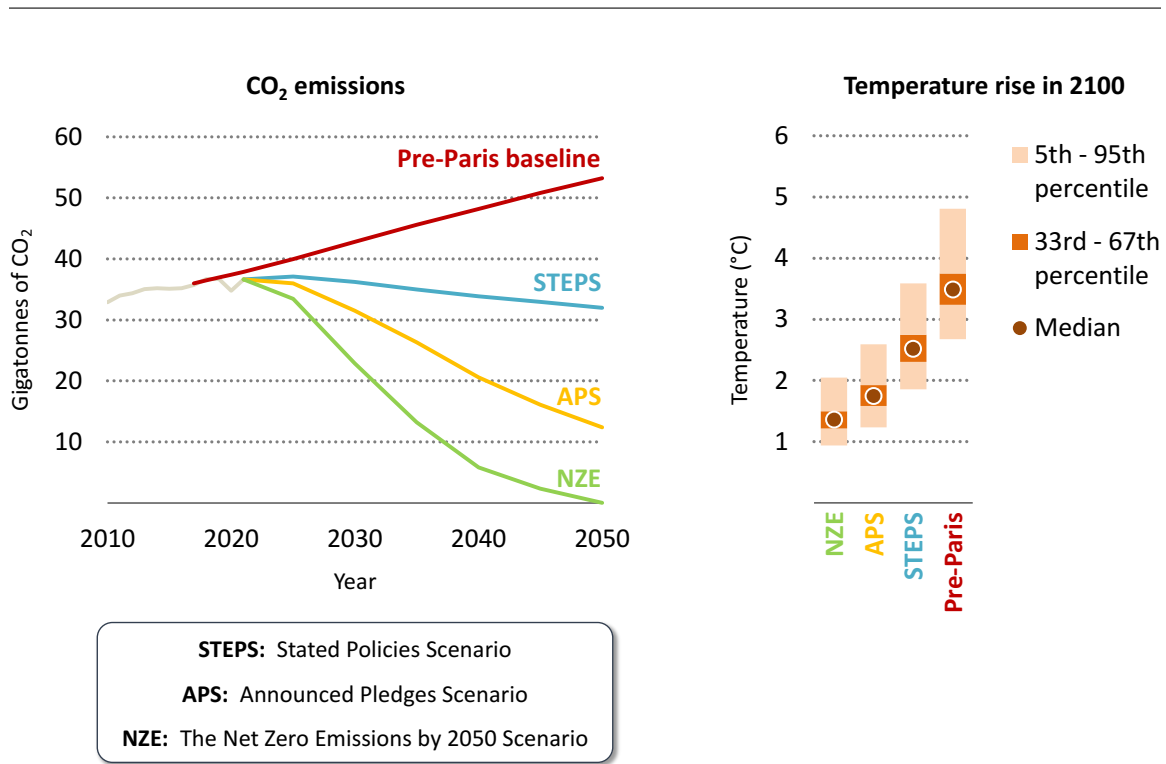


Figure 1-1: CO₂ emissions by 2050 and temperature rise in 2100 by different scenarios [3].

not be enough to avoid severe impacts from a warming planet. As reported in [4], higher temperatures caused by climate crisis can lead to increased mortality, reduced productivity and damage to infrastructure. Higher temperatures are also expected to cause a shift in the geographical distribution of climate zones while altering the distribution and abundance of many plant and animal species. Meanwhile, the yields and viability of agriculture and livestock, or the capacity of ecosystems to provide important services and goods (such as the supply of clean water or cool and clean air) could be diminished. Higher temperatures can also increase the evaporation of water, which – together with the lack of precipitation – increases the risks of severe droughts. A detailed list of climate change’s main consequences is reported in [4] while the main benefits coming from the reduction of CO₂ emissions are summarized in Fig. 1-2. As shown in Fig. 1-1, in the announced pledges scenario (APS), CO₂ emissions peak in the mid-2020s and fall to around 12 Gt in 2050. This is a bigger emissions reduction, reflecting the new or updated nationally determined contributions and announced net zero emissions pledges. The projected global median temperature rise in 2100 is about 1.7 °C. This result gets close to achieving the goal of the Paris Agreement to limit the temperature rise to “well below 2 °C”, and it marks the first time that collective

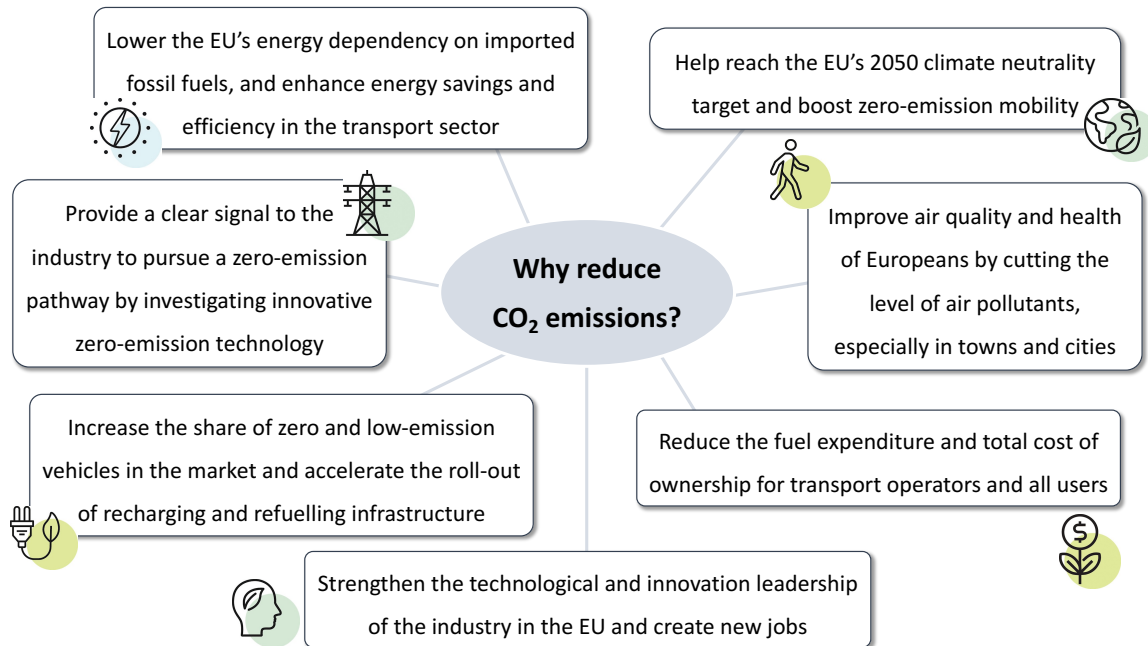


Figure 1-2: Main benefits coming from the reduction of CO₂ emissions [5].

government targets and pledges have been sufficient, if delivered in full and on time, to hold global warming to below 2 °C. However, as the Intergovernmental Panel on Climate Change (IPCC) has underlined, warming of close to 2 °C would still entail strong negative impacts for societies around the world. As shown in Fig. 1-1, the net zero emissions by 2050 (NZE) scenario allows to achieve zero CO₂ emissions in 2050 and a 1.5 °C stabilisation in the rise in global average temperatures, alongside universal access to modern energy by 2030. As a result, the NZE scenario falls within the group of scenarios categorised by the IPCC as a “no or low overshoot” scenario, and aligns with the goal of pursuing efforts to limit the temperature increase to 1.5 °C [3], as agreed in Glasgow at COP26² in 2021. These scenarios, especially the NZE one, are challenging for the vehicle manufacturers but create an ideal space for the development of new technologies and concepts. As reported in [5], heavy-duty road transportation (lorries, buses and coaches) is responsible for about 25 % of the CO₂ emissions from road transport in the European Union (EU), and for over 6 % of total EU greenhouse gas emissions. Despite the improvements achieved in fuel consumption during the recent years, the global CO₂ emissions are still rising, mainly due to

²The 2021 United Nations Climate Change conference, more commonly referred to as COP26, was the 26th United Nations Climate Change conference, held in Glasgow, Scotland, United Kingdom, from 31 October to 13 November 2021.

an increase in the road freight traffic. Therefore, to fight the climate crisis, the reduction of the local and global emissions of this type of vehicles – along with those driven daily by citizens – is crucial to bring down CO₂.

1.1 A First Step Toward Zero Pollution Objectives: the Mild-Hybrid Electric Vehicles

In order to reduce the fleet average to the mandated carbon target value, many vehicle manufacturers are expanding their product ranges to include models such as *hybrid vehicles* or pure *electric vehicles*. In fact, one option to reduce the local and global CO₂ emissions produced by vehicles is the use of pure electric powertrains³. However, the large-scale application faces the barriers of the high cost of electrical energy storage in batteries and range limitations. For these reasons, one possibility to reduce the aforementioned barriers is the use of hybrid powertrains [1]. Hybrid electric vehicles (HEVs) can operate more efficiently than the internal combustion engine (ICE) set points, and options as downsized or component simplification while fulfilling the same maximum power requirements are possible. Other benefits of the HEVs come from the energy recuperation during braking by means of an electric machine as well as the possibility to optimize the energy management between several power sources. Lastly, the introduction of high energy storage sources as the Li-ion batteries allows the development of new technologies as electrified components. With increasingly strict emission regulations, growing power load requirements of advanced automotive electronics and the conversion from mechanical components to electronic functions, the traditional 12 V lead-acid automotive battery has reached its current-carrying capacity. In response, the automotive industry has decided to develop and use 48 V as the other higher voltage [6]. The latter – which delivers more power at lower currents than a traditional 12 V lead-acid battery can produce alone – is lithium-based (Li-ion) for higher energy density by weight and volume, as shown in Tab. 1.1.

³A powertrain is a system inside a vehicle, boat or another type of machinery. The system is designed to propel the vehicle forward. In a car, a powertrain consists of the engine or motor and its internal components, such as the energy storage system, transmission and driveshaft.

Table 1.1: Typical characteristics of current Li-ion batteries for mild hybrid electric vehicles (MHEV) applications [7]

Battery type	Li-ion
Nominal voltage	48 V
Dimensions (L × W × H)	300 × 180 × 90 mm
Number of cells	up to 20
Power capability	up to 25 kW
Cooling	Natural or forced air cooling

Of interest in this dissertation is the 48 V technology, which is used in addition to the 12 V onboard network. The vehicles that use this technology are known as mild hybrid electric vehicles (MHEVs). On the one hand, this technology means that the vehicles can recover a certain amount of braking energy. On the other hand, as shown in Tab. 1.2, CO₂ can be reduced by up to 15 % (depending on the measurement guideline and driving style).

1.1.1 How Mild-Hybrid Electric Vehicles Work

All MHEVs feature a higher voltage battery in addition to the conventional 12 V battery, typically 48 V, although 24 V and 36 V systems have also been used. As shown in Fig. 1-3, the 48 V mild-hybrid system comprises of a 48 V lithium-ion storage battery, a 12 V battery, a DC/DC converter providing power from the hybrid generator via the 48 V battery while keeping the 12 V battery charged, an AC/DC converter used to change AC generator current to DC battery current, controllers for the battery, hybrid powertrain, and an electrically driven turbocharger. The result is a mild hybrid powertrain that works in parallel with the combustion engine. In mild hybrid architectures, the choice of adopting a 48 V battery leads to increase power capability by 4×, which can be used for heavier loads, such as

Table 1.2: Characteristics of hybrid electric vehicles [7]

Type	Battery type	High-volt. battery (V)	Electrical power (kW)	CO ₂ reduction* (%)
Micro hybrid	Lead-acid	12	< 5	-3
Mild hybrid	Li-ion	24-48	5-20	up to 15
Full hybrid	Li-ion	200-400	20-80	15-30

* The CO₂ reduction potential refers to chassis dynamometer type-approval tests, not real-world driving.

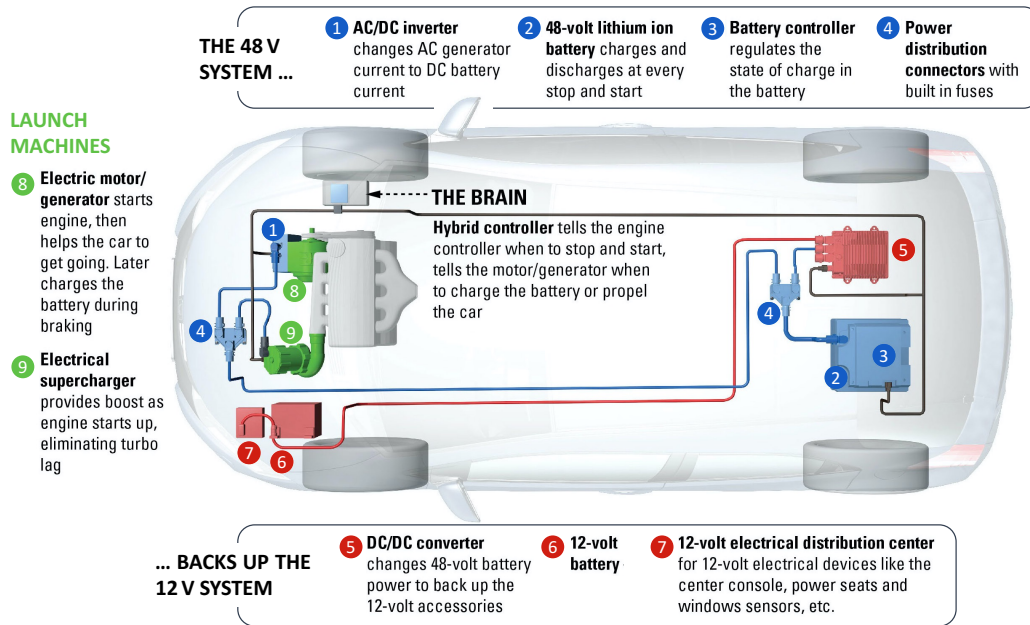


Figure 1-3: 48 V/12 V dual-battery mild hybrid system. *Source:* Delphi Technologies

the air conditioner and catalytic converter at start up [8]. To increase vehicle performance, the 48 V system powers a hybrid motor that is used for faster, smoother acceleration while saving on fuel. As shown in Fig. 1-3, in the 48 V/12 V dual-battery mild hybrid system the 48 V battery serves as a supplement (and combines) with the 12 V battery. Both the 12 V battery and the 48 V battery are used along with their distribution cables, and each battery provides power supply to the electronic loads when that particular battery is the most appropriate fit for the need. For example, the 12 V provides power to the ignition, lighting, and infotainment while the 48 V bus is responsible for the chassis-control systems, air conditioning, active/adjustable suspension, storing regenerative-braking energy, and driving electric superchargers and turbos. As shown in Tab. 1.2 and Fig. 1-4, the main differences between mild and full hybrid electric vehicles (FHEVs) are the system voltage and electrical power. While FHEVs have the ability for extended electric driving, MHEVs are usually limited to short distances of electric propulsion. A FHEV is equipped with a strong electric motor alongside a petrol or diesel internal combustion engine, that delivers additional energy as needed. The petrol or diesel engine in a MHEV does most of the work and the electric motor is there to assist. Unlike a plug-in hybrid, a mild hybrid does not require a cable to be recharged, but uses regenerative braking while driving instead.

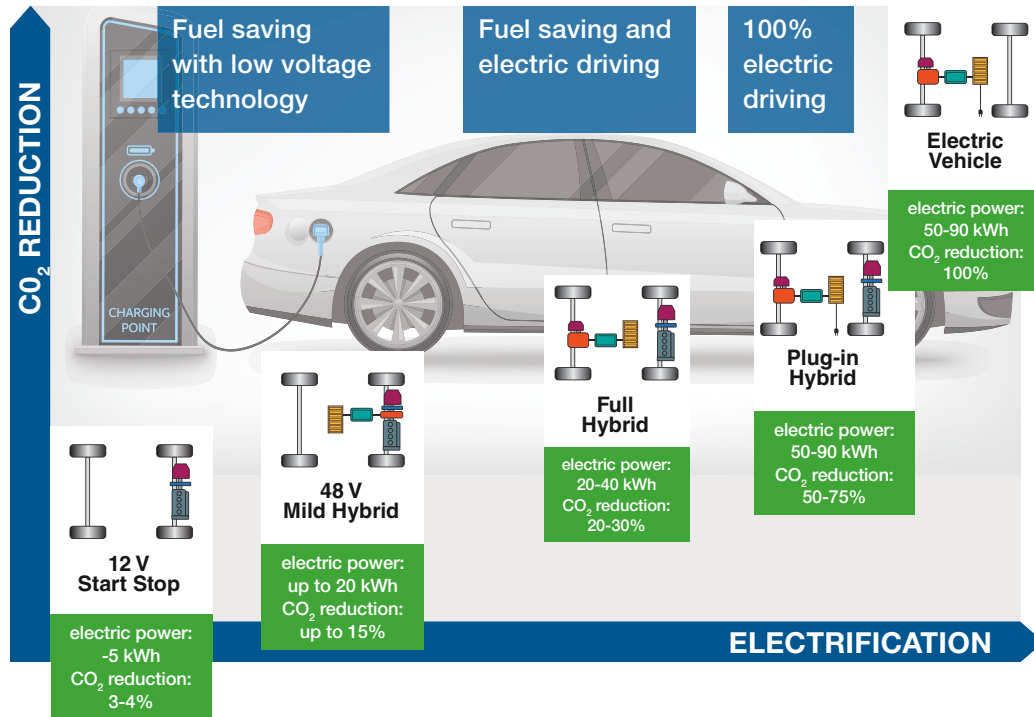


Figure 1-4: Main differences in terms of electric power and CO₂ reduction between 48 V mild hybrid, full hybrid, plug-in hybrid, and electric vehicles. *Source:* CLEPA – European Association of Automotive Suppliers

1.1.2 Mild-Hybrid Electric Vehicle Market Trends in the EU

The fast-growing adoption of electrified vehicles (EVs) and increasingly rapid build-out of the enabling charging infrastructure present their own logistical challenges. Fig. 1-5 compares the number (million units) of MHEVs with that of plug-in hybrid electric vehicles (PHEV), full hybrid electric vehicles (FHEV), and battery electric vehicles (BEV), from the year 2018 to 2023 [9]. Such a figure shows how xEV volumes will rise significantly by 2023, with MHEVs having the most significant growth.

As reported in [7] and considering the analysis made by Dataforce⁴, the market uptake of MHEVs for the period 2016 to 2021 is now considered and analyzed. Although Mercedes and Honda offered a limited number of models with mild-hybrid technology prior to 2016, manufacturers in general focused on diesel technology for the European market instead of hybrids to reach their earlier CO₂ targets. As shown in Fig. 1-6, Audi started selling significant numbers of MHEVs in 2017, reaching a sales volume of over 50,000 ve-

⁴More information available at <https://www.dataforce.de/en/>

1.1. A First Step Toward Zero Pollution Objectives: the Mild-Hybrid Electric Vehicles

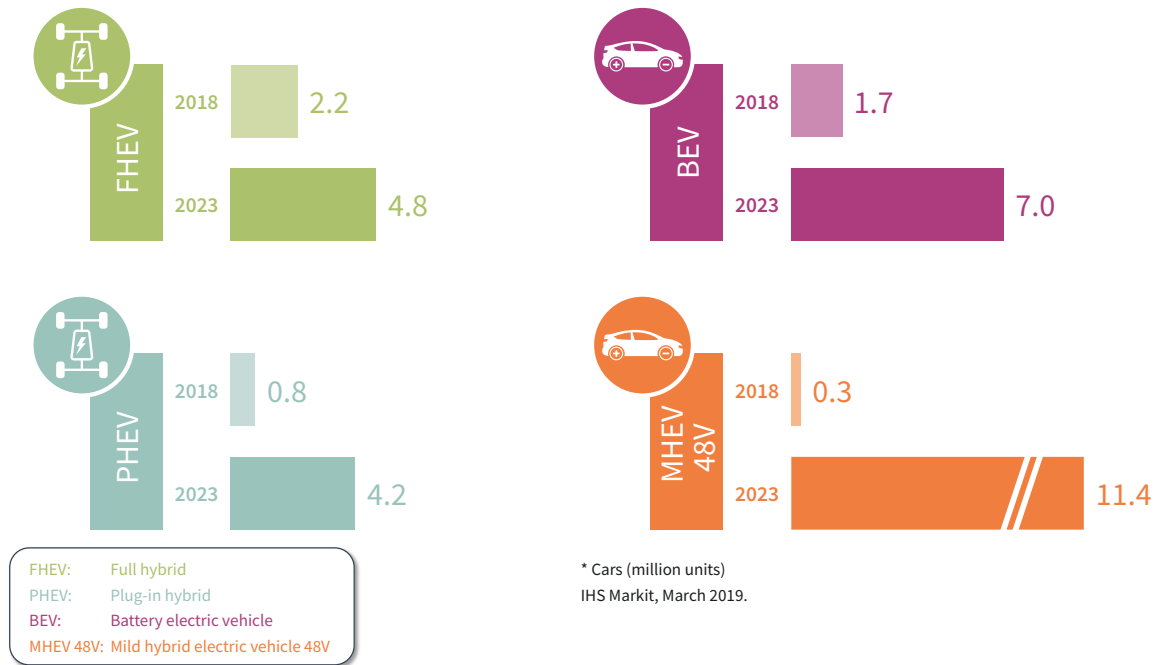


Figure 1-5: Number of xEV (million units) considering years 2018 and 2023 [9].

hicles in 2018 while becoming the leader until 2020. Although Audi sold 173,000 MHEVs in 2021, Fiat exceeded these numbers with almost 202,000 units sold. Fiat's rapid rise is remarkable considering that they sold almost no MHEVs until 2019, similar to BMW and Ford. With the exception of Mercedes, MHEV sales numbers for the ten largest manufacturers are increasing quickly since they first introduced MHEVs to the market. This rapid

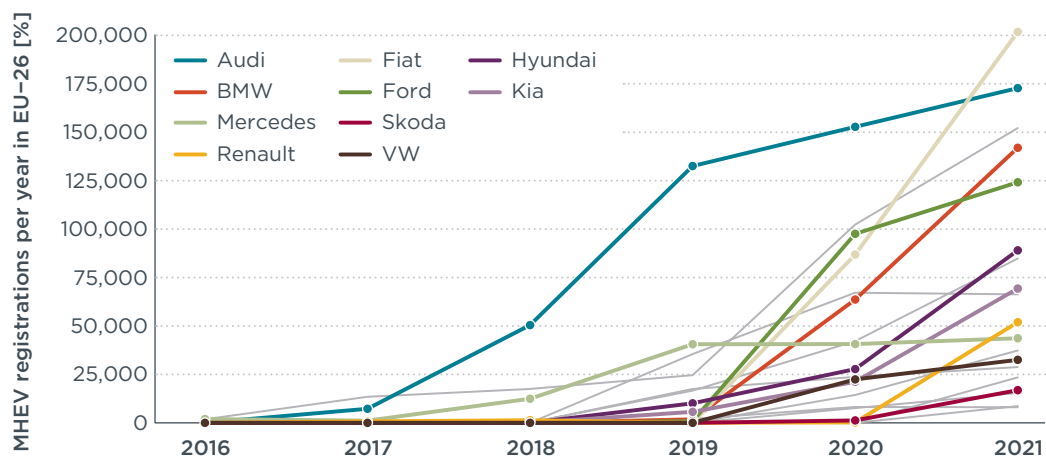


Figure 1-6: Number of registered mild-hybrid vehicles per manufacturer and year of registration. Colored curves present the 10 largest manufacturers in terms of total vehicle registrations in 26 EU countries between 2016 and 2021. The data includes EU-27 countries except Romania. *Source:* Dataforce.

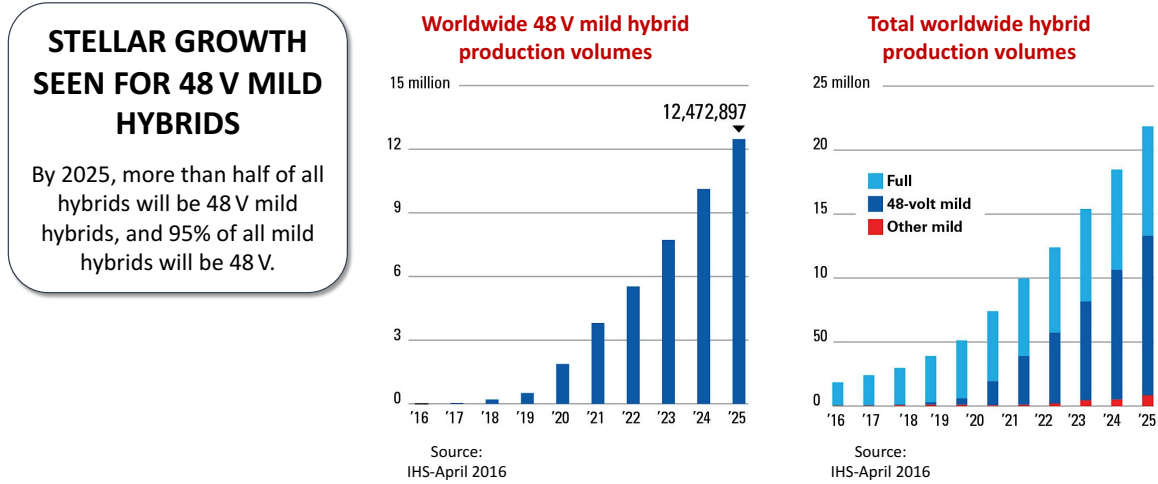


Figure 1-7: Growth for 48 V mild hybrid vehicles for the period 2016 to 2025. *Source:* Delphi

increase coincides for most brands with the new CO₂ fleet limits, which entered into force in 2020. As can be seen in Fig. 1-7, 48 V hybrids are expected to make up more than 95 % of the world’s mild hybrid market and about half of all hybrid vehicles by the end of 2025 (according to Global Insight IHS).

1.2 Scope and Outline of the Thesis

Since both the 48 V and 12 V batteries involved in MHEVs coexist in the system architectures and interact to provide power supply to a variety of electronic loads, the development of a methodology to systematically evaluate all their possible configurations in terms of efficiency, total footprint area, and cost represents an interesting challenge. Such crucial task is further complicated by the difficulty to compare different architectural solutions, as this entails the capability to systematically enumerate the possible configurations, and to set up a methodology for their comparative evaluation. This challenge leads to the realization of Chapter 2 of this dissertation, which represents the first contribution of the Ph.D. project and assumes that only the 48 V battery is currently sustaining the dual-battery architecture under investigation. The remaining chapters focus on a critical and sometimes overlooked component in these combined 12 V and 48 V systems: the isolated dc-dc converter called to provide galvanic isolation between the two voltage domains, as shown in Fig. 1-8. Such a figure, from top to bottom, shows

1. a general dual-battery 48 V/12 V system involved in 48 V MHEVs, where the block providing “galvanic isolation” is highlighted in red [10].
2. a block diagram showing the basic layout of the semiconductors used to control a belt-driven integrated starter generator (BiSG) with exciter winding (separate excitation of the synchronous machine). Such a system solution, offered by Infineon Technologies, shows a real application for 48 V mild-hybrid electrical systems and proves the need of using an isolated dc-dc converter (*e.g.* flyback converter) to separate the two voltage domains [11].
3. the block diagram of a simplified dual-battery 48 V/12 V automotive architecture where different low-power electronic loads are supplied. Such a figure shows both the case study investigated throughout this thesis and the isolated dc-dc converter on which chapters 3-7 will focus on [12–16].

Galvanic isolation shown in Fig. 1-8 is crucial for immunity against ground noise and to protect 12 V systems in case of ground lifts or fault conditions in the 48 V systems to which they connect. A conventional 12 V lead-acid battery still powers control electronics and lower-power devices even in vehicles using the 48 V battery. Systems running on these two supplies need to communicate with one another (*e.g.* a 48 V starter generator is controlled by the engine controller operating off the 12 V battery). While theoretically, the two systems can directly connect, is almost always necessary to have galvanic isolation – as shown in Fig. 1-8 – because of the following reasons [10]:

- *Transient ground potential differences.* The grounds of 12 V systems connect directly to the car chassis using bolts and the grounds of 48 V modules connect to the car chassis using cables that can be a few feet long. The high amount of switching currents present in 48 V systems – such as the starter generator or AC compressor – combined with the inductive nature of the ground cable, can result in transient ground noise that can corrupt low-voltage (3.3 V or 5 V) communication signals. For this reason, an isolated dc-dc converter providing galvanic isolation is necessary to ensure reliable data transfer.

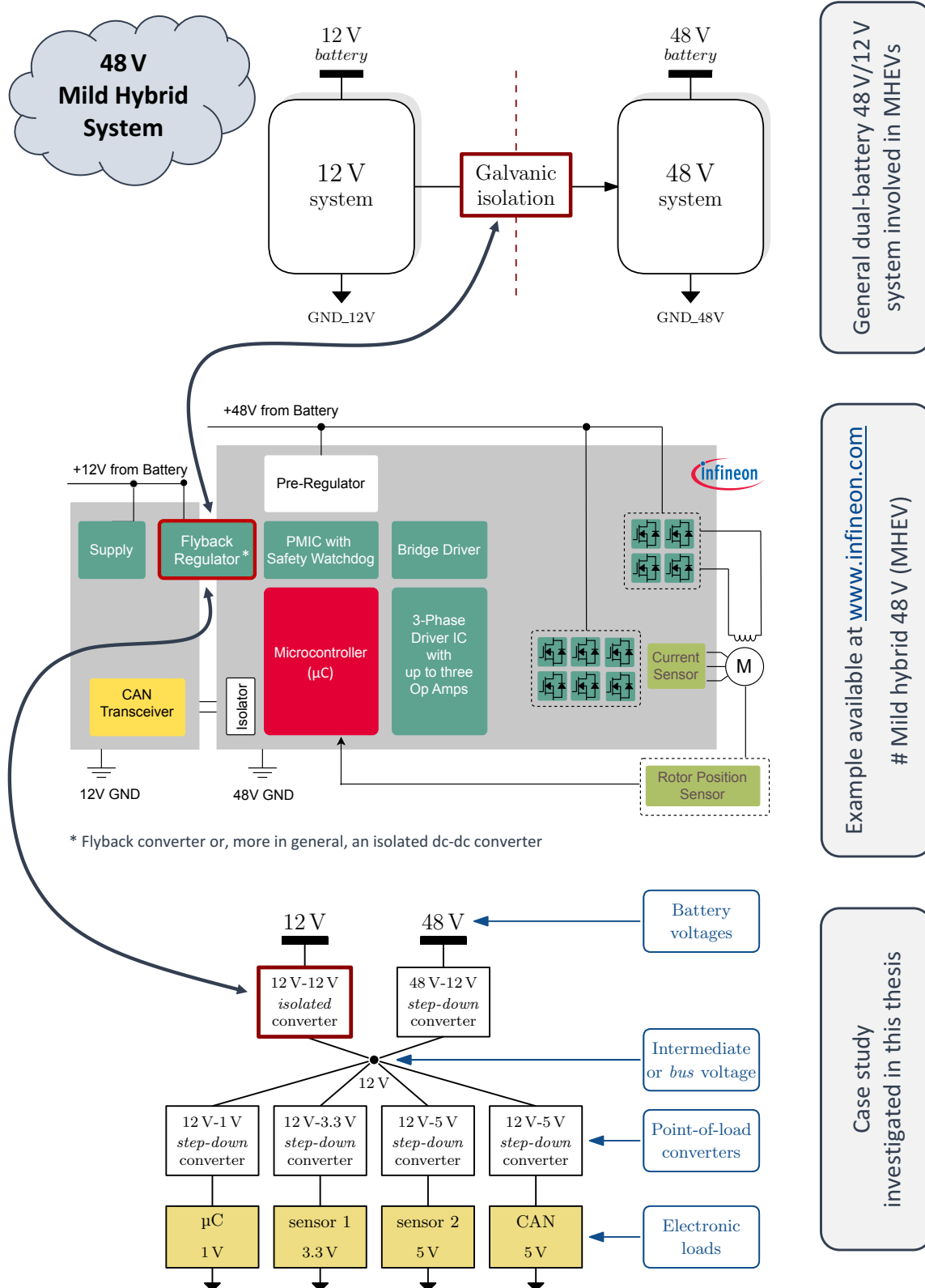


Figure 1-8: Examples of architectures that require the presence of an isolated dc-dc converter to separate the two voltage domains.

- *Ground lift on the 48 V side.* Sometimes the GND_48V shown in Fig. 1-8 could disconnect from the chassis under fault conditions or during maintenance. In this situation, all internal nodes of the 48 V system (including the interface to the 12 V system) can float up to 48 V. This poses a danger to 12 V systems, since its input/output ports may not be designed to handle 48 V. In Fig. 1-8, this fault condition does not stress the 12 V system since the 48 V appears across a galvanic isolation barrier.
- *Short-circuit conditions.* In Fig. 1-8, any short circuit inside the 48 V system can result in the 48 V appearing at the interface to the 12 V system. This potential hazard can compromise many circuits operating on the 12 V supply, including those critical to the safe operation of the MHEVs. The presence of an isolated dc-dc converter can help to ensure that any short circuits on the 48 V system do not propagate to the 12 V side of the vehicle.

The second and last contribution of the Ph.D. project faces the serious challenge of investigating and designing several isolated dc-dc topologies for the dual-battery 48 V/12 V automotive scenario shown in Fig. 1-8. The performances of such topologies are then compared in terms of efficiency, electromagnetic interference (EMI) noise, temperature, and stress across the devices to find the most suitable one for the considered application. For this work, it is assumed that the 48 V battery fails and the overall architecture under investigation is sustained by the 12 V battery.

1.2.1 Dissertation Outline

The dissertation consists of eight chapters. The current chapter, Ch. 1, introduces the considered research topic, highlighting the main aspects on which the research activity reported herein is focused.

In detail, the rest of the dissertation is organized according to the following outcome.

- **Chapter 2 “Comparative Study of 48 V-based Low-Power Automotive Architectures”.** This chapter represents the basis on which the central part of the dissertation develops. The whole study – which focuses on low-power 48 V/12 V battery-connected architectures for emerging automotive scenarios – aims at developing a

methodology to systematically enumerate all the possible configurations that a given architecture can have by modeling the latter as a mathematical tree. Such enumeration, done via analytical expressions and proved through the Matlab script reported in App. B, aims at comparing the valid configurations in terms of efficiency, cost, and size for trade-off analysis. This chapter concludes the first part of the thesis.

- **Chapter 3 “Active-Clamped Isolated SEPIC Converter in the MHz Range”.**

This chapter opens the second part of the thesis, in which the fundamental results of the Ph.D. project are presented and discussed. The 48 V/12 V battery-connected architecture is still considered and the focus is now on the converter intended to provide isolation and power interface between the 12 V battery and the low-power subnet while assuming that the overall system is sustained by the 12 V battery. Although presently adopted solutions at the industry level are based on the flyback topology, a design methodology is here proposed for a viable substitute named active-clamped isolated SEPIC converter (ACISC). The latter makes use of Gallium Nitride (GaN) technology and operates in the MHz range to reduce total magnetic size while avoiding disturbance in the typical AM band. The main contribution of this chapter is the proposal of a theoretical model specifically developed for full zero-voltage switching (ZVS) resonant discontinuous conduction mode (DCM) operation, along with the design and implementation of planar magnetics. The chapter – which compares the aforementioned operating mode with the other possible ones and highlights its main benefits – is closed with an efficiency comparison between the designed ACISC and a commercial flyback converter intended for the same application, and having the same input/output voltage and rated current specifications.

- **Chapter 4 “Power Loss Breakdown Analysis”.** This chapter, which is closely related to the previous one, aims at identifying the main loss sources involved in the designed ACISC while estimating their relative contributions. A power loss breakdown is proposed here together with the derived analytical expressions. The final section closes the chapter by summarizing some considerations to further improve the proposed power loss estimation.

- **Chapter 5 “Magnetics Analysis and Optimization Techniques”**. The results obtained in Ch. 4 lead to the realization of this new chapter in which the high-frequency planar magnetics are investigated and improved via a step-by-step optimization technique. The most relevant aspects of such magnetics are considered with the aim of improving the efficiency profile of the ACISC and reducing the in-circuit noise.
- **Chapter 6 “Active-Clamped Isolated Flyback Converter in the MHz Range”**. In this chapter, a detailed comparison between the designed ACISC and a similar topology named active-clamped isolated flyback converter (ACIFC) is given. Unlike the efficiency comparison made in Ch. 3 with a commercial flyback converter, here a more fair comparison is done between two topologies running in the MHz range, hosting the same GaN devices, and operating with the same operation mode. A table is then used to summarize all the analytical current/voltage expressions derived for the two topologies. The chapter is closed by reporting the main advantages and disadvantages of the two topologies and their efficiency profile.
- **Chapter 7 “EMI Analysis and Temperature Considerations”**. In this chapter, an overview of conducted electromagnetic interference (EMI) specifications for power converters is given, while focusing on the automotive standard CISPR25 which details EMI limits to any electric/electrical component intended for use in vehicles. The experimental setup for the EMI measurements is disclosed and the three investigated topologies (ACISC, ACIFC, and commercial flyback) are compared in terms of conducted emission and temperature in the main components.
- **Chapter 8 “Conclusions”**. A summary of the most significant results and some comments close this thesis.

Index Terms—ac winding resistance, automotive power distribution, CO₂ emissions, constrained bucking trees (CBTs), electromagnetic interference (EMI) noise, GaN devices, high-frequency operation, inter-winding capacitance, isolated dc-dc converters, mild hy-

brid electric vehicles (MHEVs), planar magnetics, power loss estimation, resonant dc-dc converters, zero-voltage switching (ZVS).

Chapter 2

Comparative Study of 48 V-based Low-Power Automotive Architectures

Selection of a dc power distribution architecture is a multi-faceted task in which system-level *efficiency*, *cost*, *size* and other metrics must be assessed in the framework of a trade-off analysis. Examples include low-power distribution architectures for emerging automotive scenarios, dc power distribution systems for telecom, mobile, aerospace and data centers, and dc micro- or nano-grids interfacing multiple sources and loads via dc-dc conversion stages [17–20]. Such crucial task is further complicated by the difficulty to compare different architectural solutions, as this entails the capability to systematically enumerate the valid architectures [17, 18], and to set up a methodology for their comparative evaluation. A block diagram of a general dc distribution architecture is shown in Fig. 2-1a, where m regulated Point-Of-Load (POL) dc voltages are obtained from a dual dc input source. Such architecture is typically realized connecting one of the batteries to the electronic loads through multiple Single-Input Single-Output (SISO) dc-dc converter modules. Fig. 2-1b shows the specific case study investigated in this work – which focuses on a dual-battery 48 V/12 V low-power automotive scenario – where the 12 V backup battery is not connected to the system since the 48 V main battery is providing power supply to a variety of low-power electronic loads such as sensors, micro-controllers (μC) and communication transceivers (CAN). Fig. 2-2 shows a possible configuration for the 48 V/12 V low-power automotive scenario depicted in Fig. 2-1b, where $m = 4$ electronic loads are supplied

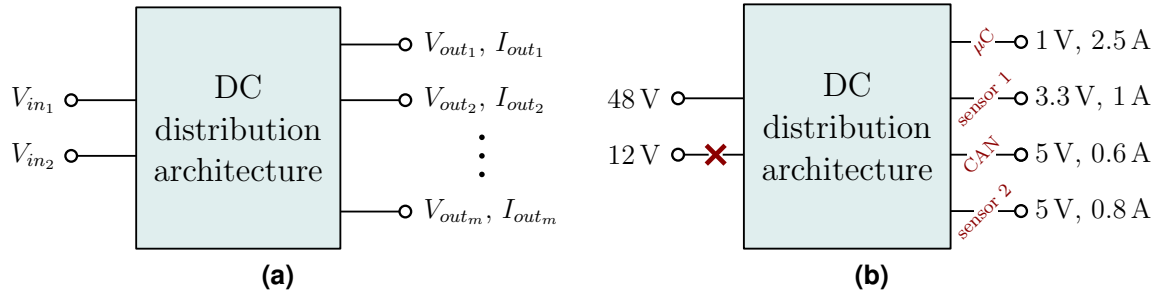


Figure 2-1: DC automotive distribution architecture where m regulated point-of-load (POL) dc voltages are obtained from a dual-battery input source: (a) general case, and (b) case study investigated in this work in which the 12 V backup battery is not connected to the system since the latter is sustained by the 48 V main battery.

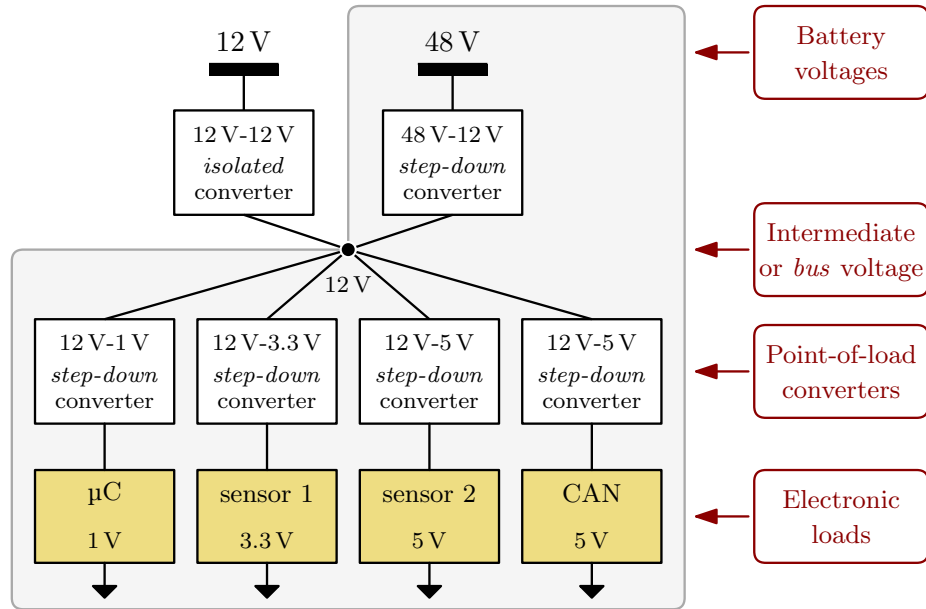


Figure 2-2: Example of a dual-battery 48 V/12 V automotive scenario referred to Fig. 2-1b, where the 48 V main battery supplies the entire system and the 12 V backup battery is disconnected. POL are highlighted in yellow.

by the 48 V main battery through step-down converters and a unique *bus* voltage equal to 12 V. Objective of this study is to explore a framework for a systematic trade-off assessment of tree-like architectural solutions. The integral part of the proposed study concerns the inclusion, in the network, of dedicated dc-dc units for High Step-Down (HSD) voltage conversion (*e.g.* 48 V-1 V), as well as fixed voltage conversion ratio stages such as Switched-Capacitor (SC) converters. The study will confirm that such dedicated solutions for dc-dc conversion can be conveniently incorporated in the candidate architectures

to improve the system-level efficiency. At the same time, the general lack of commercial products providing optimized and highly integrated implementations for these converters makes them still poorly competitive against traditional designs.

To explore the space of candidate architectures, this work builds on the *Permutation-Graph* (PG) methodology introduced in [21, 22], in which architecture enumeration is tied to that of specific permutations of the assigned dc voltage domains. By further constraining the search to *Bucking Trees* only, *i.e.* by excluding the presence of dc-dc step-up converters in the architecture, [21, 22] strongly reduce the number of candidate solutions and, therefore, the size of the system-level optimization space. In this work, the PG enumeration idea is adapted into a *Constrained Bucking Trees* (CBT) approach, in which the number of valid configurations for a given battery-connected architecture is further reduced by the constraint to have n intermediate or *bus* voltages, and a predefined set of m POL (output) voltages. The rationale behind such constraint is that, as in the automotive scenario at hand, the number and the value of the POL voltages are often dictated by the application.

This chapter is organized as follows. Section 2.1 introduces several representation and enumeration methodologies focusing on the proposed CBT method, while section 2.2 discloses the definitions adopted in this study to assess efficiency, footprint area and cost of candidate architectures. Section 2.3 addresses the core topic of this study by investigating how the system-level architectural choice changes when dedicated HSD topologies and fixed conversion ratio stages are included in the analysis. To conclude, section 2.4 shows the generalization of the CBT method, providing the analytical expression and the algorithm to enumerate the valid CBT permutations when more than one *bus* voltage is involved in the architecture.

2.1 Representation and Enumeration of Single Input Multiple Output (SIMO) Automotive Architectures

A system graph representation is adopted and used hereafter to model and enumerate all the possible configurations of a given Single Input Multiple Output (SIMO) architecture.

As reported above, the considered case study focuses on a low-power architecture supplied by one battery only, called here V_{in} , which makes use of several SISO dc-dc converters to supply a pre-determined set of m POL voltages through n bus voltages. This subsection shows four methodologies which can be used to enumerate the possible configurations, through graphical representations and analytical expressions, until the adopted one for this work is described and shown. The methodologies are listed below:

- Total Number of Possible Trees (TNPT)
- Spanning Trees (ST)
- Bucking Trees (BT)
- Constrained Bucking Trees (CBT) $\mapsto$ adopted in this work

Note that, moving from TNPT to CBT, the number N of possible configurations for a given architecture is significantly reduced since more accurate expressions and more reasonable constraints are used to enumerate physically realizable arrangements of the architecture.

2.1.1 Total Number of Possible Trees (TNPT)

In this enumeration methodology, the nodes used to represent the battery V_{in} , the m POL voltages, and n bus voltages, are generic nodes that can be interconnected between each other in any way (without constraints). The list of total possible trees can be obtained by creating a complete graph of the voltages involved in the system and finding all sub-graphs of the complete graph which contain m edges, where m is the number of low-power POL voltages supplied by the architecture. For example, the complete graph of an architecture which sustains $m = 6$ electric loads is shown in Fig. 2-3a, and the relationship between them and the battery voltage V_{in} is given below

$$0 < V_1 < V_2 < V_3 < \mathbf{V_{in}} < V_4 < V_5 < V_6 \quad (2.1)$$

In the provided example, the total number of possible trees N_{TNPT} is given by a combination of $m = 6$ gold edges. This number can be found as the number of combinations of m edges

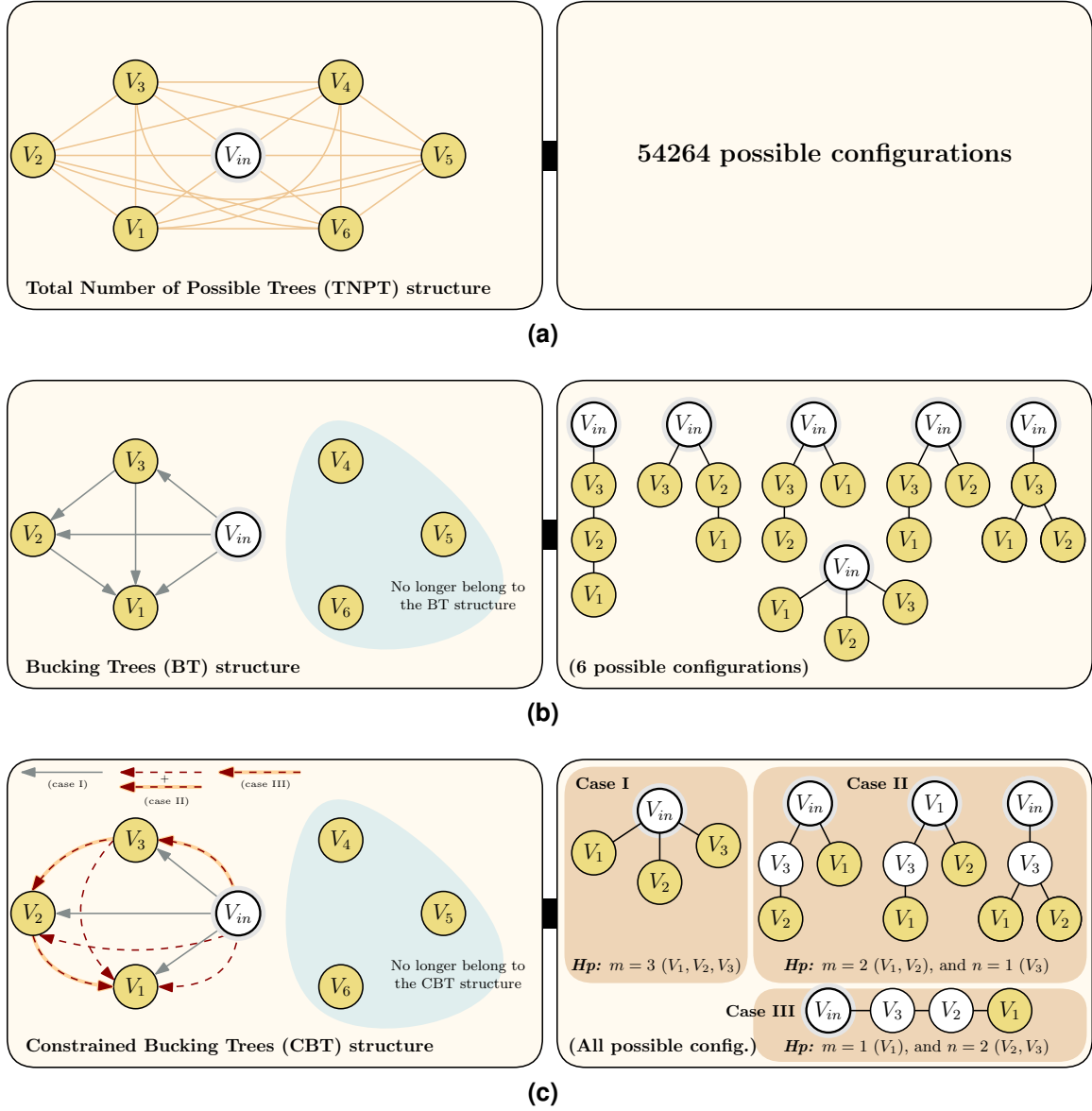


Figure 2-3: Configurations for a battery-connected architecture which supplies $m = 6$ POL voltages, when it is modeled following the (a) TNPT approach, (b) BT approach, and (c) CBT approach.

chosen from the m_e edges of the complete graph. The expression is given below

$$N_{TNBT} = \binom{m_e}{m} = \frac{m_e!}{m!(m_e - m)!}, \quad (2.2)$$

where m_e can be found using the following expression

$$m_e = \frac{m(m+1)}{2} \quad (2.3)$$

and remembering that $m + 1$ is the total number of nodes in the complete graph shown in Fig. 2-3a. The list of possible trees given by N_{TNPT} contains all possible arrangements of the m output voltages and, for the case study shown in Fig. 2-3a, it is equal to 54264. However, the majority of these arrangements are not desirable or physically realizable. As shown in [21, 22], to reduce the computational effort it is possible to build a subset of the list of all possible trees, which leads to the concept of “Spanning Trees”.

2.1.2 Spanning Trees (ST)

The spanning trees are a subset of full list of possible graphs N_{TNPT} which are taken from the complete graph of the input and outputs shown in Fig. 2-3a. A spanning tree contains all the $1 + m$ voltages, each with a path to the input battery V_{in} , and does not contain any loops. The number N_{ST} of spanning trees can be found using Cayley’s formula

$$N_{ST} = (1 + m)^{m-1}. \quad (2.4)$$

Fig. 2-4 shows the significant reduction in terms of configurations to be checked when the ST approach is adopted instead of the TNPT approach.

2.1.3 Bucking Trees (BT)

In most cases of interest, the required m POL voltages are always lower or higher than the battery voltage V_{in} . For example, if the voltages involved in the architecture are lower than the input voltage, only step-down converters should be employed since it would be inefficient to cascade step-up and step-down converter stages. This leads to the concept of “Bucking Trees” which are ST that contain only monotonic cascaded converter stages, *i.e.* no stages that boost up after bucking down. Fig. 2-3b shows the six possible configurations for the case study reported above and, as can be noted, output voltages V_4, V_5, V_6 no longer belong to the BT structure since their value is higher than V_{in} . The number N_{BT} of bucking trees can be found simply as the number of permutations of the m POL voltages

$$N_{BT} = m!. \quad (2.5)$$

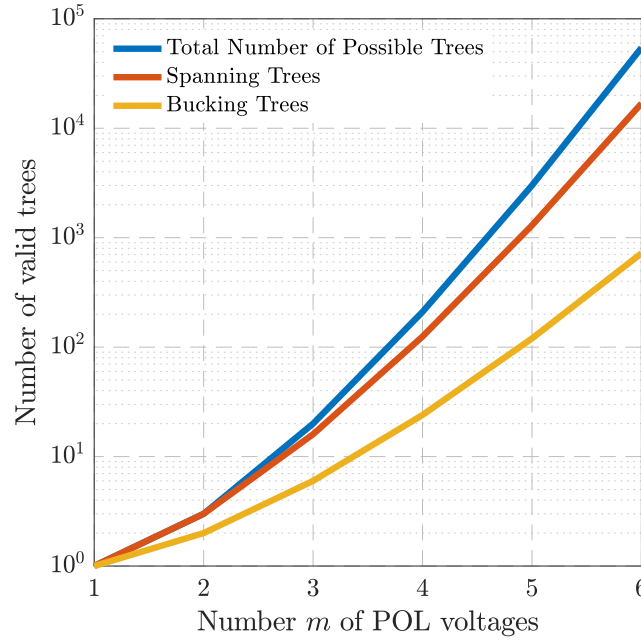


Figure 2-4: Number of possible configurations obtained for a single battery-connected architecture (having m POL voltages) when different enumeration approaches are adopted (e.g. TNPT, ST, and BT).

which yields a substantial reduction in the number of possible configurations, as illustrated in Fig. 2-4.

2.1.4 Proposed Constrained Bucking Trees (CBT) Approach

In [21, 22] each BT-based architecture is modeled as a mathematical tree, in which *i*) the input voltage and all the voltages involved in the architecture are represented by nodes, and *ii*) the edge between a parent node and a child node always represents a SISO dc-dc step-down converter. As shown in Fig. 2-4, by constraining the search to such BT only, the number of valid solutions is strongly limited compared to TNPT and ST approaches.

In the *Constrained Bucking Trees* (CBT) approach proposed and adopted in this work, the number of valid trees is further reduced by constraining all architectures to have a pre-determined set of $m \geq 1$ *point-of-load* (POL) voltages (modeled by leaf nodes) as well as a pre-determined set of $n \geq 1$ intermediate or *bus* voltages (modeled by internal nodes). Converters producing the POL voltages can either operate off the bus voltage, or can be directly connected to the battery voltage (root of the tree). The total number of voltages

in the architecture is, including the root and the bus nodes, $1 + n + m$, while the number of dc-dc converters is $n + m$. Additional assumptions in the proposed CBT approach are reported below:

1. The input voltage is greater than all the other voltages.
2. The largest POL voltage is strictly smaller than the smallest bus voltage.
3. All bus voltages are different from each other.
4. POL voltages are distinguishable, *i.e.* they associate with physically distinct loads.

Note that some of the POL voltages may share the same value.

Below the CBT simplest case is considered and analyzed, *i.e.* an architecture having $n = 1$ bus voltage. The generalization of this study is reported at the end of this chapter, showing the procedure to find the expression to analytically calculate the valid configurations when $n \geq 1$.

Permutation-Graph Construction of Bucking and Constrained Bucking Trees

Following [21, 22], BT are here associated with specific permutations of the assigned voltages. Such association between trees and permutations is crucial for the mathematical enumeration derived for the CBT approach.

To briefly review how a BT can be generated from a permutation, consider the tree shown in Fig. 2-5a. This architecture is created from the permutation $\{48 \ 12 \ 1 \ 3.3 \ 5_1 \ 5_2\}$ via the following construction rule. The first (leftmost) element, 48 V, is the input voltage of the architecture and it is the root of the tree. The second element, 12 V, is strictly smaller than 48 V so it is attached to the 48 V node. The third element, 1 V, is strictly smaller than 12 V, so it is attached to the 12 V node. The fourth element, 3.3 V, is larger than 1 V but strictly smaller than 12 V, so it is attached to 12 V. The next element, 5 V (identified with the label 5_1), is larger than 3.3 V but strictly smaller than 12 V, so it is attached to the 12 V node as well. Finally, the last element, 5 V (identified with the label 5_2), is strictly smaller than the bus voltage, so it is attached to the 12 V node. As another example, the tree shown in Fig. 2-5b is generated from the permutation $\{48 \ 1 \ 12 \ 3.3 \ 5_1 \ 5_2\}$. More generally, working

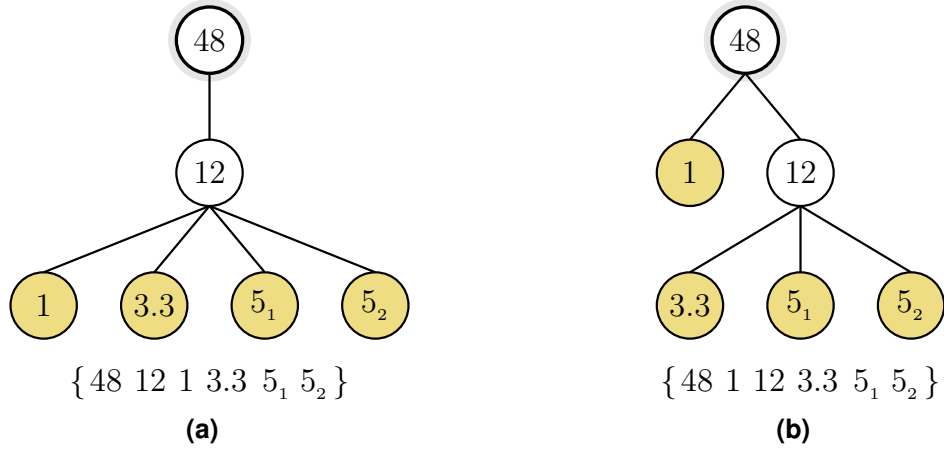


Figure 2-5: Two 48 V-based architectures having a single 12 V bus and $m = 4$ point-of-load voltages (highlighted in yellow). Corresponding permutations are reported below each tree.

Table 2.1: POL voltages and rated currents of the considered case study

Physical Load	Node label	V_o (V)	POL Rated I_o (A)	POL Rated P_o (W)
μC	1	1	2.5	2.5
sensor 1	3.3	3.3	1	3.3
sensor 2	5_1	5	0.8	4
CAN	5_2	5	0.6	3

through the permutation systematically from left to right, each new voltage is connected to the closest preceding voltage having a strictly larger value. This way the connections (edges) between two nodes always represent step-down conversions.

Enumeration of the Constrained Bucking Trees

The enumeration formula for the valid CBT is now disclosed, taking the following 48 V-based network scenario as a practical case study (the same as the one depicted in Fig. 2-1b):

- Input voltage V_{in} : 48 V
- $n = 1$ bus voltage: 12 V
- $m = 4$ point-of-load voltages, as detailed in Tab. 2.1.

In this scenario, the number N_{BT} of *Bucking Trees* is, following [21,22], $N_{BT} = (1+m)!$. On

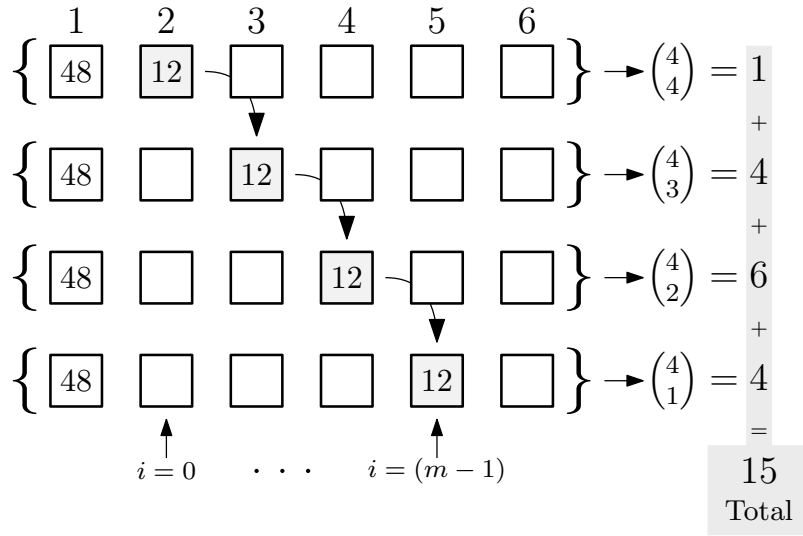


Figure 2-6: Structures of the 15 valid permutations corresponding to one 48 V input voltage, one 12 V bus voltage and $m = 4$ point-of-load voltages (blank cells).

the other hand, the number N_{CBT} of *Constrained Bucking Trees* according to the proposed approach reduces to

$$N_{CBT} = 2^m - 1. \quad (2.6)$$

To see this, consider Fig. 2-6, which exemplifies the case study under consideration. Having established that the input voltage always occupies the first (leftmost) position in the permutation (since it is greater than all the other voltages and represents the root of the tree), the *bus* voltage can only be placed between the second and the penultimate cell: according to the construction rule set out above, if a *bus* voltage was placed in the last cell, it would become a leaf node attached to the input voltage. To find the number N_{CBT} of permutations associated with valid trees, one has to enumerate all possible ways the m output voltages can be placed in the remaining (empty) positions, with the constraint that *adjacent output voltages must appear in ascending order*, otherwise some of them would become bus voltages. In Fig. 2-6, if i denotes the position of the *bus* voltage in the permutation as shown, one has $\binom{m}{m-i} = \binom{4}{4-i}$ ways to allocate the POL voltages in the empty cells for each possible choice of i . In the example of Fig. 2-6 corresponding to the selected case study this yields a total of $2^4 - 1 = 15$ valid trees, where two of which were previously exemplified in Fig. 2-5.

More generally, since i ranges from 0 to $m - 1$, an architecture having $n = 1$ bus

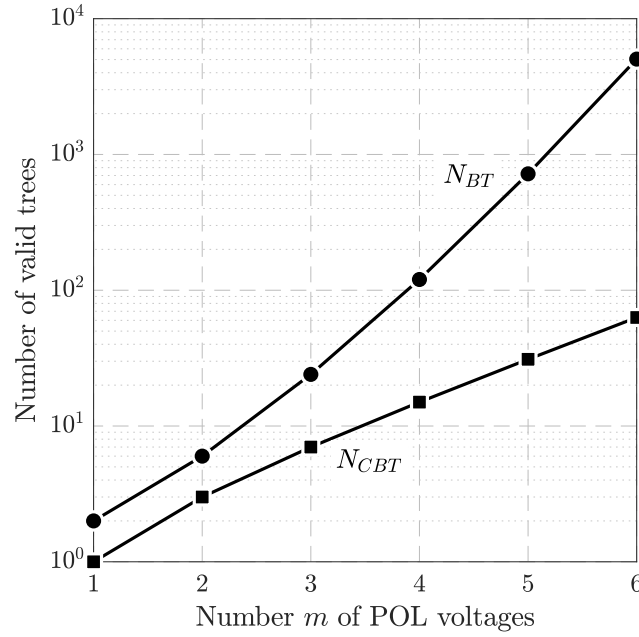


Figure 2-7: Comparison between the number N_{BT} of *Bucking Trees* (circles) and the number N_{CBT} of *Constrained Bucking Trees* (squares) as a function of the number m of POL voltages.

voltage and m electronic loads, which is modeled with the CBT method, can have

$$N_{CBT} = \sum_{i=0}^{m-1} \binom{m}{m-i} = \sum_{i=0}^m \binom{m}{m-i} - 1 = 2^m - 1,$$

different configurations, where the last equality follows from the binomial theorem [23]. App. A proves that this result can also be obtained by making use of the Tartaglia-Pascal’s triangle. Fig. 2-7 compares N_{CBT} with the number $N_{BT} = (1 + m)!$ of (unconstrained) Bucking Trees, as a function of the number m of POL voltages and assuming a single bus voltage ($n = 1$). As expected, N_{CBT} is always much smaller than N_{BT} (this can also be noted in the previous example shown in Fig. 2-3c).

Finally, Fig. 2-8 shows the $N_{CBT} = 15$ possible configurations (represented as trees and called “arch”) for the considered case study (POL voltages and rated currents were previously shown in Tab. 2.1). Trees called “arch #1” and “arch #4”, which were previously shown in Fig. 2-5, are highlighted in blue.

2.1. Representation and Enumeration of Single Input Multiple Output (SIMO) Automotive Architectures

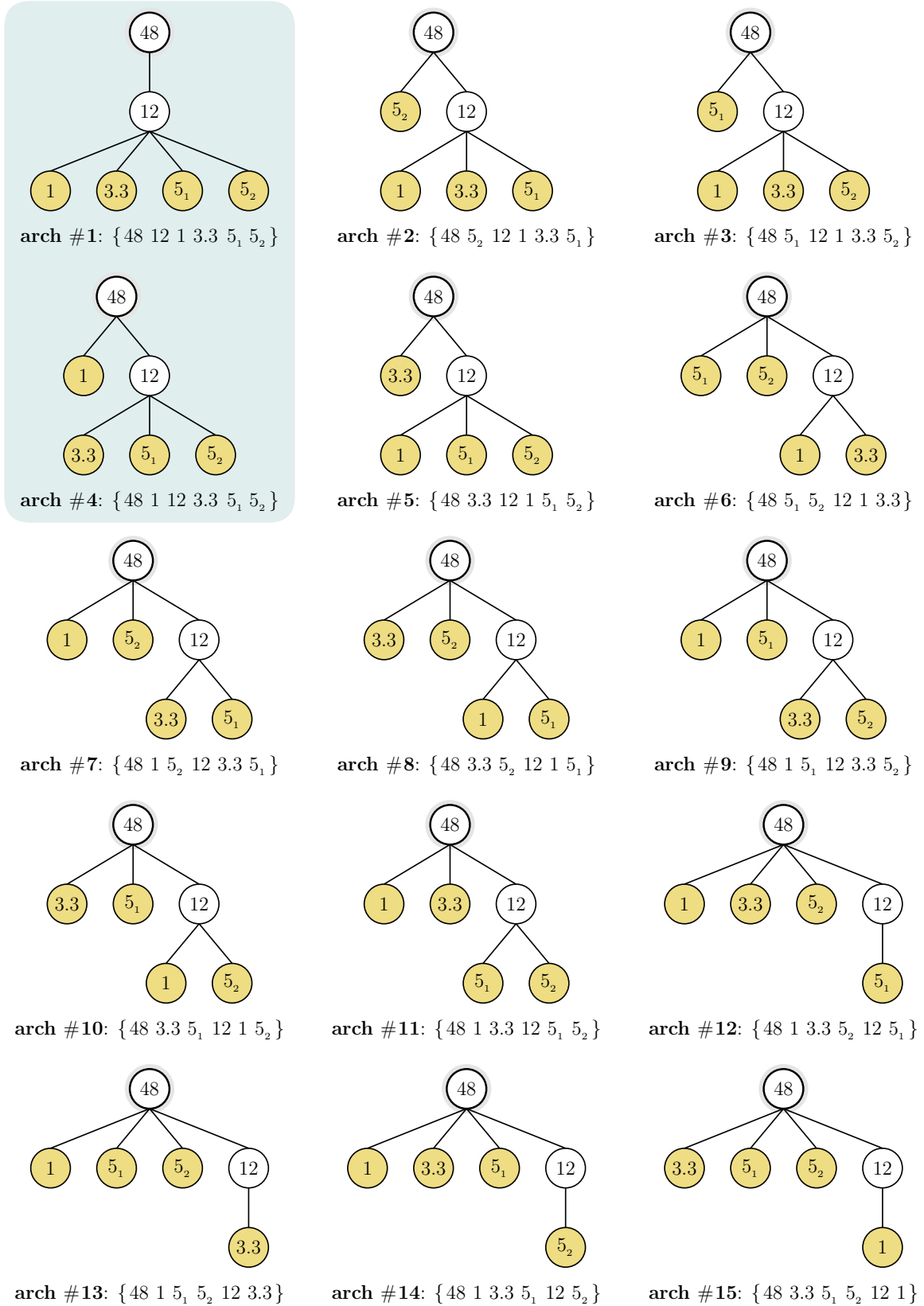


Figure 2-8: Structures of the 15 valid configurations corresponding to the considered case study: a battery-connected architecture having one 48 V input voltage, one 12 V bus voltage and $m = 4$ point-of-load voltages (Tab. 2.1). Corresponding permutations are reported below each tree.

2.2 Efficiency, Footprint and Cost Evaluation of Candidate Architectures

Once the available candidate architectures/configurations are enumerated, methods can be introduced to define and estimate system-level parameters *such as* efficiency, footprint area and cost of a given architecture.

The efficiency of each individual architecture is here evaluated following these four steps:

1. assign an efficiency profile $\eta_k(I_o)$, $k = 1 \dots m + 1$ to each SISO dc-dc step-down converter (edge) involved in the architecture;
2. select the load currents of the m POL converters; in this work, these currents are set to their rated values reported in Tab. 2.1;
3. starting from the POL converters and proceeding towards the root, calculate the input current $I_{in,k}$ of the k -th converter as

$$I_{in,k} = \frac{1}{\eta_k(I_{o,k})} \frac{V_{o,k} \cdot I_{o,k}}{V_{in,k}}, \quad (2.7)$$

where $V_{in,k}$ and $V_{o,k}$ represent the k -th converter's input and output voltages, and $I_{o,k}$ its total output current. Whenever the k -th converter is feeding multiple converters, $I_{o,k}$ is simply the summation of their previously calculated input currents.

4. calculate the efficiency of the architecture as

$$\eta_{tree} \triangleq \frac{P_o}{P_{in}}, \quad (2.8)$$

where the numerator represents the total output power of the m POL converters, while the denominator represents the total power absorbed from the battery. According to the POL voltages and rated currents reported in Tab. 2.1, the total output power P_o for the considered case study is equal to 12.8 W.

The total footprint F_{tree} and cost C_{tree} of a given architecture can be estimated, in an approximate fashion, as the summation of the contributions F_k and C_k of the individual converters involved in the architecture [18,21,22],

$$F_{tree} \triangleq \sum_{k=1}^{m+1} F_k, \quad C_{tree} \triangleq \sum_{k=1}^{m+1} C_k. \quad (2.9)$$

Note that it would be impractical trying to calculate a more accurate value for F_{tree} and C_{tree} because it is required to know the final distribution of the components in the electronic device. For this reason, the proposed approach is considered a very fast and accurate enough calculation.

2.2.1 Database Construction

Preliminary to the numerical estimation of efficiency, footprint and cost of the candidate architectures according to (2.8) and (2.9) is the construction of a *database* of plausible efficiency profiles, area and cost data for each SISO dc-dc conversion step that may appear in a battery-connected architecture. For step-down units implemented around conventional synchronous Buck topologies, data can be conveniently extracted using results from WEBENCH[®] Power Designer tool by Texas Instruments [24]. For other types of conversion units, which will be considered later in the context of a comparative evaluation between ‘Buck-only’ architectures and hybrid ones, corresponding database entries will be populated based on existing commercial products whenever these are available.

Fig. 2-9a and Fig. 2-9b report the efficiency profiles *vs.* the output current I_o provided by WEBENCH[®] and used to model the efficiency of the SISO dc-dc units whenever these are realized as Buck topologies. These profiles are provided by the tool once input voltage range, current rating and switching rate of the dc-dc unit are specified as inputs. For 48 V-input converters, the input voltage range was specified as 25 V-55 V. Although several profiles for different values of the switching rate f_{sw} could, in general, be stored in the database to generalize the analysis, a fixed value $f_{sw} = 500$ kHz is assumed in this study for all Buck converters in the considered architectures.

Footprint and cost estimates for Buck-based topologies obtained from WEBENCH[®]-

proposed designs are summarized in Tab. 2.2 and 2.3. As specified in the tool documentation, the converter footprint area is calculated as the total components footprint plus 1 mm per side, while the converter total cost is calculated as the total bill of material cost.

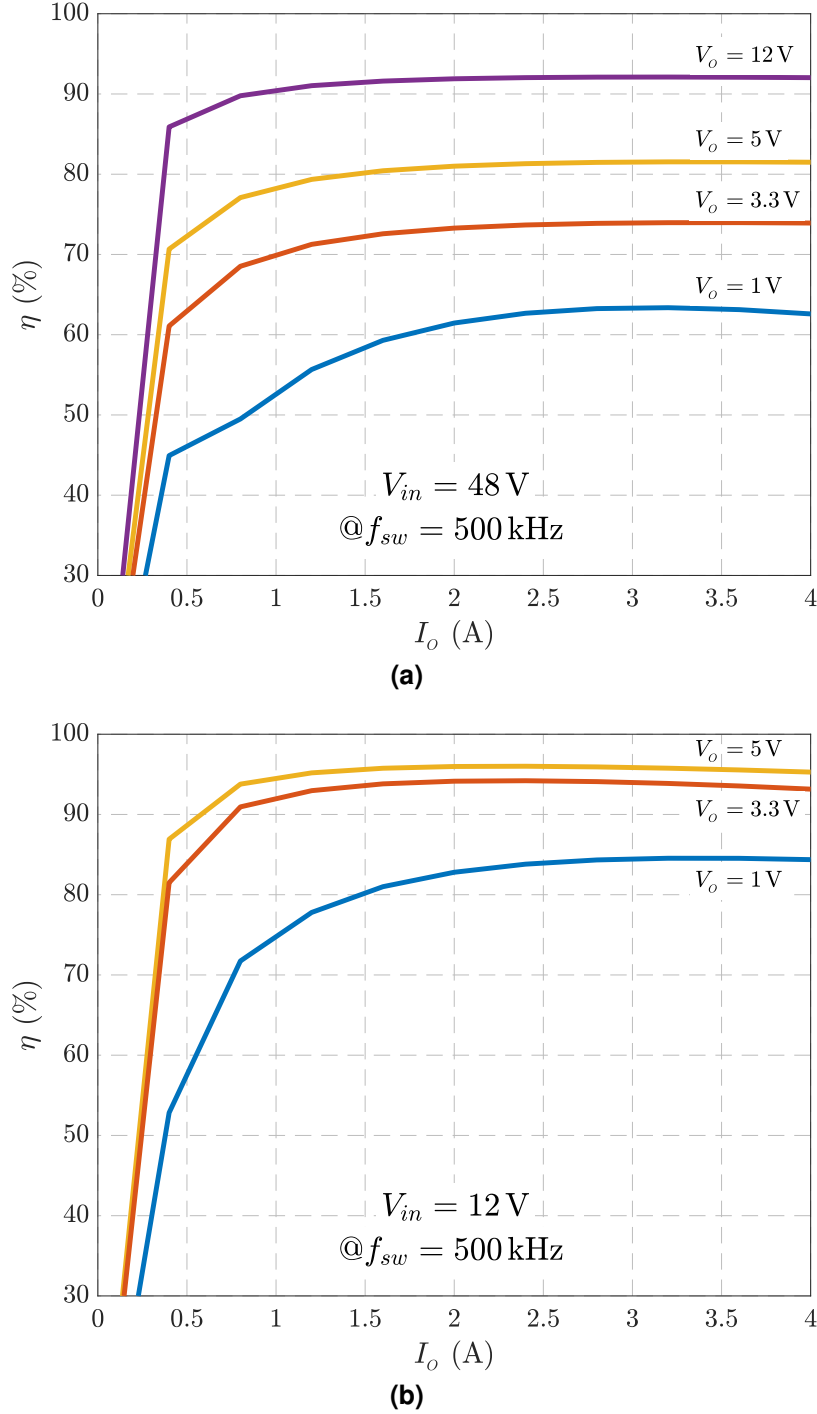


Figure 2-9: Database efficiency profiles of Buck converters running at $f_{sw} = 500 \text{ kHz}$, with an input voltage equal to (a) 48 V and (b) 12 V. Additional information is provided in Tab. 2.2 and 2.3.

Table 2.2: Database of Buck converters having $f_{sw} = 500$ kHz and input voltage equal to 48 V

Buck converter [Part Number]	V_o (V)	footprint (mm ²)	cost (USD)	$\eta(I_o)$ (%)
LM5088MH-1	12	609	4.92	Fig. 2-9a
LM5088MH-1	5	615	4.86	Fig. 2-9a
LM5088MH-1	3.3	593	4.62	Fig. 2-9a
LM5117PMHX	1	689	5.51	Fig. 2-9a

Table 2.3: Database of Buck converters having $f_{sw} = 500$ kHz and input voltage equal to 12 V

Buck converter [Part Number]	V_o (V)	footprint (mm ²)	cost (USD)	$\eta(I_o)$ (%)
LM25145RGYR	5	330	3.09	Fig. 2-9b
LM25145RGYR	3.3	330	3.21	Fig. 2-9b
LM25145RGYR	1	179	3.41	Fig. 2-9b

2.3 Comparative Study of 48 V Architectures

To develop a comparative analysis and rank the possible architectures, different scenarios will be considered. In the most conventional one, addressed in section 2.3.1, all dc-dc units in the architecture are created around synchronous Buck converter topologies. Sections 2.3.2 and 2.3.3, on the other hand, investigate the possibility of including ‘non-Buck’ stages such as dedicated High Step-Down (HSD) topologies or fixed conversion ratio Switched-Capacitor (SC) converters, in order to assess the impact of these choices and related trade-offs on a system-level scale.

2.3.1 Buck-only Architectural Solutions

Tab. 2.4 reports the efficiency ranking of the 15 valid architectures/configurations for the considered case study. Efficiency, footprint area and cost are estimated according the definitions and data disclosed in section 2.2. The most efficient architecture, which also has the lowest area and total cost, possesses all the POL voltages connected to the 12 V bus voltage and is precisely the one illustrated in Fig. 2-5a. Notice that the difference in efficiency between the best and worst architectures is almost 17%, proving the importance of considering (and enumerating) all the possible configurations for a given battery-connected

Table 2.4: Efficiency ranking of the 15 Buck-only architectures. Architectures possessing a 48 V-1 V stage are denoted with an asterisk.

ID	Architecture permutation	efficiency (%) ↓	footprint area (mm ²)	cost (USD)
1	{48 12 1 3.3 5 ₁ 5 ₂ }	82.28	1778	17.72
2	{48 5 ₂ 12 1 3.3 5 ₁ }	79.59	2063	19.49
3	{48 5 ₁ 12 1 3.3 5 ₂ }	79.05	2063	19.49
4*	{48 1 12 3.3 5 ₁ 5 ₂ }	78.19	2288	19.82
5	{48 3.3 12 1 5 ₁ 5 ₂ }	77.79	2041	19.13
6	{48 5 ₁ 5 ₂ 12 1 3.3}	76.33	2348	21.26
7*	{48 1 5 ₂ 12 3.3 5 ₁ }	75.61	2573	21.59
8	{48 3.3 5 ₂ 12 1 5 ₁ }	75.18	2326	20.90
9*	{48 1 5 ₁ 12 3.3 5 ₂ }	75.05	2573	21.59
10	{48 3.3 5 ₁ 12 1 5 ₂ }	74.67	2326	20.90
11*	{48 1 3.3 12 5 ₁ 5 ₂ }	73.96	2551	21.23
12*	{48 1 3.3 5 ₂ 12 5 ₁ }	69.75	2836	23.00
13*	{48 1 5 ₁ 5 ₂ 12 3.3}	68.02	2858	23.36
14*	{48 1 3.3 5 ₁ 12 5 ₂ }	65.71	2836	23.00
15	{48 3.3 5 ₁ 5 ₂ 12 1}	65.44	2611	22.67

architecture. The well-known reason why having an intermediate 12 V conversion step results in a higher efficiency architecture is that its presence forces the Buck converters to operate in a more efficient condition: as confirmed by the efficiency profiles of Fig. 2-9a and Fig. 2-9b, Buck converters operating at high step-down ratios become very inefficient. In a 48 V-based battery system such as the case study under consideration, where the load voltages range from 1 V to 5 V (as shown in Tab. 2.1), presence of an intermediate 12 V bus significantly improves the system efficiency.

As noted, the efficiency-optimal arch #1 also exhibits the least footprint area and cost. This is due to all the POL converters in arch #1 (Fig. 2-5a) being connected to the regulated 12 V bus rather than the 48 V battery voltage, with corresponding less stringent voltage rating requirements on the input capacitors. Fig. 2-10 shows the results generated for arch #4 once the Matlab program is compiled: on the left the structure of the Matlab tree is shown, while on the right it is reported the screenshot of the information printed in the Command Window. This window – which helps to understand the plot shown on the left providing the voltage value of the nodes and the efficiency of the dc-dc converters – also

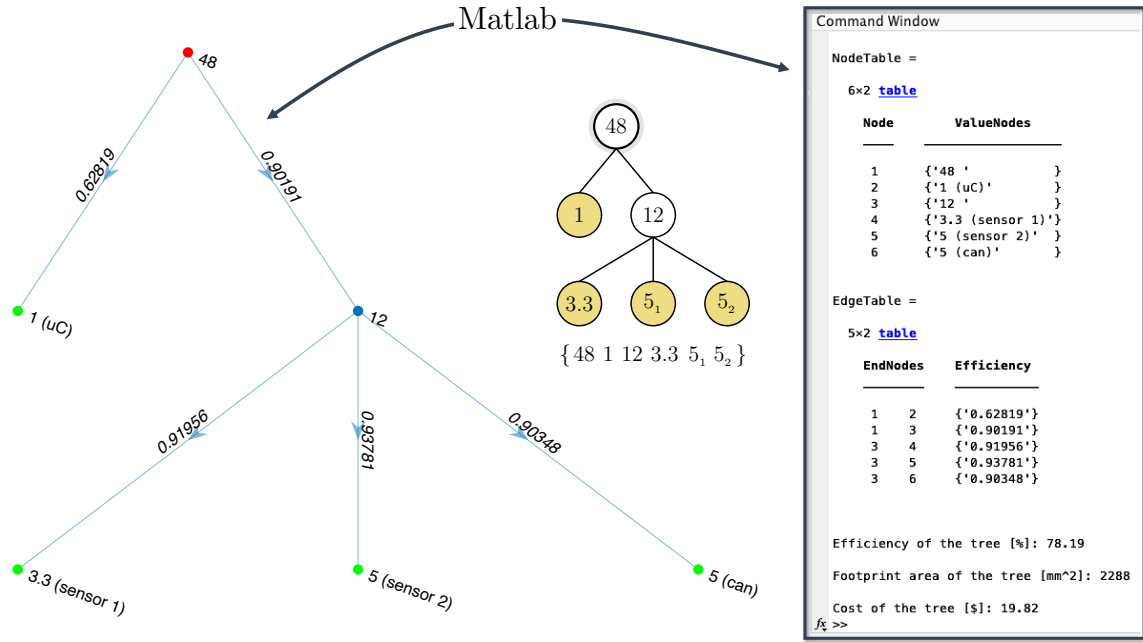


Figure 2-10: Results obtained for architecture #4 when the Matlab code reported in appendix B is compiled.

gives the results for the entire system in terms of efficiency, footprint area and cost (as can be seen, these results are the same as those reported in the fourth row of Tab. 2.4).

2.3.2 Use of Dedicated Topologies for High Step-Down (HSD) Conversion

In the ranking of Tab. 2.4, architectures possessing a 48 V-1 V stage are denoted with an asterisk. Among these, the most efficient is architecture #4, which is illustrated in Fig. 2-5b (and also in Fig. 2-10). In this architecture the 48 V-1 V stage has a very poor efficiency whenever it is made with a Buck converter – slightly above 60 % according to Fig. 2-10. It is interesting therefore to ask whether the use of *dedicated*, ‘non-Buck’ topologies for efficient HSD conversion (*e.g.* such as [25]) would lead to a different architecture ranking. To this purpose, the efficiency $\eta_{(48\text{ V}-1\text{ V})}$ of the 48 V-1 V conversion step is parameterized, and the architecture ranking is regenerated. Fig. 2-11 compares the efficiency of the best Buck-only architecture (#1 in Tab. 2.4, Fig. 2-5a) and efficiencies of all the architectures possessing a 48 V-1 V stage, when the latter is realized with an efficiency equal to

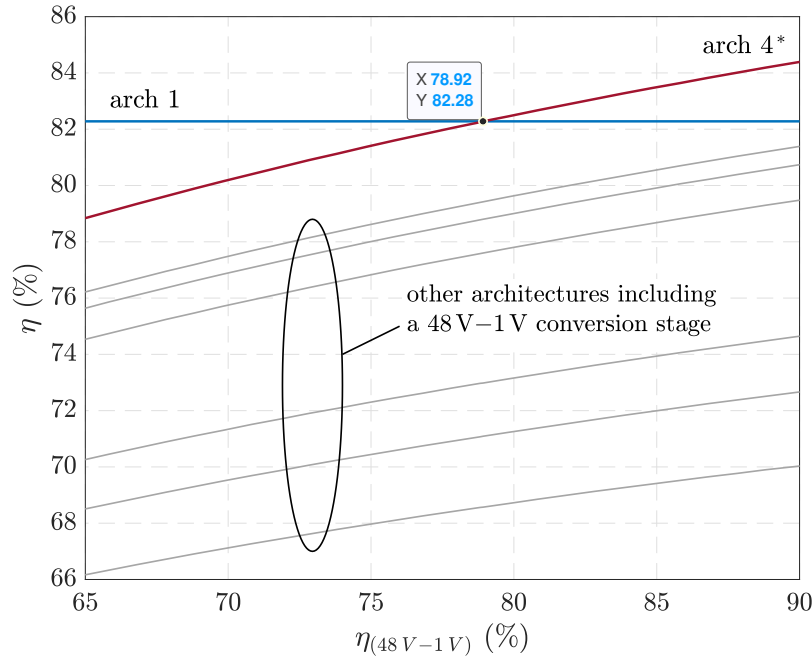


Figure 2-11: Efficiency comparison between architecture #1 in Tab. 2.4 and all the architectures possessing a 48 V-1 V stage, as a function of the efficiency $\eta_{(48\text{ V}-1\text{ V})}$ of the latter.

$\eta_{(48\text{ V}-1\text{ V})}$. Results indicate that architecture #4 (Fig. 2-5b, Fig. 2-10) becomes the most efficient architecture as long as $\eta_{(48\text{ V}-1\text{ V})}$ is larger than about 79%. This conclusion confirms that the architectural choice for best efficiency changes whenever dedicated HSD stages can be included in the system, and indicates that these converters become advantageous even when having moderate efficiencies, the reason being that they are used to *replace* less efficient solutions. Moreover, this result confirms the importance of being able to enumerate and consider all possible configurations of a given battery-connected architecture. As can be seen, the configuration that at first seems to be the most obvious one (arch #1) is no longer the most efficient one.

In the literature, a number of efficient *single-stage* high step-down converters have been reported for POL regulation off a 12 V as well as a 48 V bus [25, 26]. Commercially available 48 V solutions are presently limited, however, to very high-power POL converters intended for data-center applications [27]. Within the range of output currents targeted by this study (a few amps) the offer is much more limited: while products exist which perform voltage conversions down to 12 V-1.8 V with a peak efficiency exceeding 90 % [28],

direct 48 V-1 V conversion is most often accomplished via isolated converters in which the transformer provides most of the step-down action. In absence of commercial product references, cost and footprint area for these approaches are difficult to estimate. In general, however, these implementations invariably introduce penalties due to their additional components (*e.g.* magnetics) and consequently modest level of integration.

2.3.3 Inclusion of Fixed Conversion Ratio Stages

The general fact that adding intermediate voltage levels can result in a better system-level efficiency is here further explored. Attractive candidates, in this regard, are *switched-capacitor* (SC) conversion stages, which operate well with *fixed* voltage conversion ratios while maintaining a good power density and reduced footprint impact due to their inductor-less nature [29]. In this section, the possibility to insert an intermediate 2 : 1 unregulated SC conversion stage is investigated for the considered case study. Specifically, two distinct scenarios for the insertion of the SC stage are considered:

- **Scenario 1:** SC stage connected to the battery voltage in order to perform an unregulated 48 V-to-24 V conversion;
- **Scenario 2:** SC stage connected to the 12 V bus voltage in order to perform an unregulated 12 V-to-6 V conversion.

An example to Scenario 1 and Scenario 2 adapted to the considered case study is shown in Fig. 2-12. *Notice* that a direct 48 V-12 V conversion made with a SC stage is explicitly excluded, as this would transform the 12 V bus into an unregulated one, a scenario not examined in this work.

According to the case study examined in this work, the output current rating of the additional SC converter should be larger than about 0.5 A for Scenario 1, or about 2 A for Scenario 2. The two SC stages will be assumed to have an efficiency $\eta_{sc} = 98\%$, a figure consistent with state of the art commercial SC solutions for the above current ratings [29]. To assess the impact of the SC insertion over the Buck-only case, all other converters in the architecture will be assumed to be Buck topologies. Efficiency profiles for

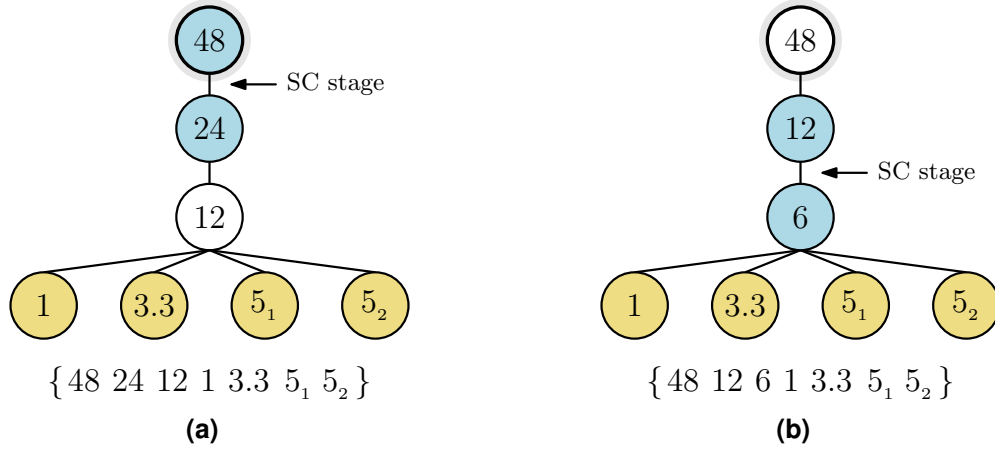


Figure 2-12: Tree structures of (a) architecture #1' for Scenario 1, and (b) architecture #1'' for Scenario 2, employing a 2 : 1 SC conversion stage. Corresponding permutations are reported below each tree.

the 24 V-input and 6 V-input Buck converters are extracted from WEBENCH[®] reference designs. Furthermore, the operation of Buck converters directly off the 48 V battery voltage is forbidden in light of the previous discussion on the inherently poor efficiency of these configurations.

The general CBT construction rule set out in section 2.1.4 can be easily reused to enumerate the architectures in the two cases. Permutations obtained for Scenario 1 can be found by following the construction rule shown in Fig. 2-6, adapted to $3 + m = 7$ total voltages. The first and second cells in Fig. 2-6 are, respectively, always occupied by 48 V and 24 V, while the position of the 12 V bus voltage is varied. Similarly, for Scenario 2 one has $3 + m = 7$ total voltages. The first and second cells in Fig. 2-6 are, respectively, always occupied by 48 V and 12 V, while the position of the 6 V output voltage of the SC stage is varied. Both scenarios give rise to 15 new architectures/configurations, which are ranked by efficiency in Tab. 2.5 and 2.6 respectively. To generate the ranking, area/cost estimates of the SC converters were adapted from the typical application example reported in [29] and following definitions (2.9). The resulting database entries for the SC stages were $F_{sc} = 280 \text{ mm}^2$, $C_{sc} = 9 \text{ USD}$ for Scenario 1, and $F_{sc} = 302 \text{ mm}^2$, $C_{sc} = 9.70 \text{ USD}$ for Scenario 2. Best architectures #1' and #1'' for Scenario 1 and Scenario 2, respectively, are shown in Fig. 2-12. To evaluate the impact of the SC stage efficiency on the

2.3. Comparative Study of 48 V Architectures

Table 2.5: Efficiency ranking of the 15 architectures employing a 48 V-24 V SC conversion stage (Scenario 1), assuming $\eta_{sc} = 98\%$.

ID	Architecture permutation	efficiency (%) ↓	area (mm ²)	cost (USD)
1'	{48 24 12 1 3.3 5 ₁ 5 ₂ }	83.94	2003	26.11
2'	{48 24 1 12 3.3 5 ₁ 5 ₂ }	83.07	2289	26.53
3'	{48 24 5 ₂ 12 1 3.3 5 ₁ }	82.88	2326	26.64
4'	{48 24 5 ₁ 12 1 3.3 5 ₂ }	82.10	2326	26.64
5'	{48 24 1 5 ₂ 12 3.3 5 ₁ }	81.94	2612	27.06
6'	{48 24 1 5 ₁ 12 3.3 5 ₂ }	81.13	2612	27.06
7'	{48 24 5 ₁ 5 ₂ 12 1 3.3}	80.95	2649	27.17
8'	{48 24 3.3 12 1 5 ₁ 5 ₂ }	80.84	2207	26.55
9'	{48 24 1 3.3 12 5 ₁ 5 ₂ }	79.93	2493	26.97
10'	{48 24 3.3 5 ₂ 12 1 5 ₁ }	79.74	2530	27.08
11'	{48 24 3.3 5 ₁ 12 1 5 ₂ }	79.00	2530	27.08
12'	{48 24 1 3.3 5 ₂ 12 5 ₁ }	76.36	2816	27.50
13'	{48 24 1 5 ₁ 5 ₂ 12 3.3}	74.23	2935	27.59
14'	{48 24 1 3.3 5 ₁ 12 5 ₂ }	71.43	2816	27.50
15'	{48 24 3.3 5 ₁ 5 ₂ 12 1}	69.87	2853	27.61

Table 2.6: Efficiency ranking of the 15 architectures employing a 12 V-6 V SC conversion stage (Scenario 2), assuming $\eta_{sc} = 98\%$.

ID	Architecture permutation	efficiency (%) ↓	area (mm ²)	cost (USD)
1''	{48 12 6 1 3.3 5 ₁ 5 ₂ }	84.30	2021	23.36
2''	{48 12 5 ₁ 6 1 3.3 5 ₂ }	84.07	2074	24.27
3''	{48 12 3.3 6 1 5 ₁ 5 ₂ }	83.94	2071	24.39
4''	{48 12 3.3 5 ₁ 6 1 5 ₂ }	83.71	2124	25.30
5''	{48 12 5 ₂ 6 1 3.3 5 ₁ }	83.64	2074	24.27
6''	{48 12 1 6 3.3 5 ₁ 5 ₂ }	83.50	1924	24.57
7''	{48 12 5 ₁ 5 ₂ 6 1 3.3}	83.41	2127	25.18
8''	{48 12 3.3 5 ₂ 6 1 5 ₁ }	83.29	2124	25.30
9''	{48 12 1 5 ₁ 6 3.3 5 ₂ }	83.27	1977	25.48
10''	{48 12 1 3.3 6 5 ₁ 5 ₂ }	83.15	1974	25.60
11''	{48 12 3.3 5 ₁ 5 ₂ 6 1}	83.06	2177	26.21
12''	{48 12 1 3.3 5 ₁ 6 5 ₂ }	82.92	2027	26.51
13''	{48 12 1 5 ₂ 6 3.3 5 ₁ }	82.85	1977	25.48
14''	{48 12 1 5 ₁ 5 ₂ 6 3.3}	82.62	2030	26.39
15''	{48 12 1 3.3 5 ₂ 6 5 ₁ }	82.50	2027	26.51

overall system-level performance, and similarly to what has been done in section 2.3.2, the efficiency of the SC stage is parameterized, and the general efficiency ranking of the various architectures is recalculated. For Scenario 1, Fig. 2-13 compares the total efficiency of Buck-only architecture #1 (Fig. 2-5a) and the efficiency of SC-based architecture #1' (Fig. 2-12a), plotted as a function of the efficiency η_{sc} of the 48 V-to-24 V SC stage. The SC-based solution becomes the most efficient architecture as long as the SC stage has a conversion efficiency larger than about 96%. For Scenario 2, Fig. 2-14 compares the efficiency of Buck-only architecture #1 with that of architectures #1'', #2'', #4'' and #11'' (Tab. 2.6). In this case the SC-based approach becomes advantageous over the Buck-only one as long as the SC stage has an efficiency larger than about 93.5%. In particular, architecture #1'' (Fig. 2-12b) settles as the most efficient one as long as the 12 V-to-6 V SC stage has a conversion efficiency larger than about 97%, and as advantageous over the Buck-only architecture for $\eta_{sc} > 95.6\%$.

Notice that, since these SC solutions introduce one *additional* conversion stage rather than replace one, efficiency requirements are more stringent than those found for HSD-based architectures. For the same reason, SC-based architectures exhibit a penalty in footprint area with compared to Buck-only ones, although not as large as if the additional stage was made with a Buck converter. On the other hand, as evident from Tab. 2.5 and 2.6, the still poorly competitive cost of commercial switched-capacitor solutions for 48 V applications represents the major limitation preventing their widespread adoption. This is mostly due to the absence of *fully integrated* SC solutions compatible with the current rating of interest. For example, the reference design adopted to generate Tab. 2.5 and 2.6 is based on a general-purpose SC product which does not integrate the semiconductor switches [29].

2.3. Comparative Study of 48 V Architectures

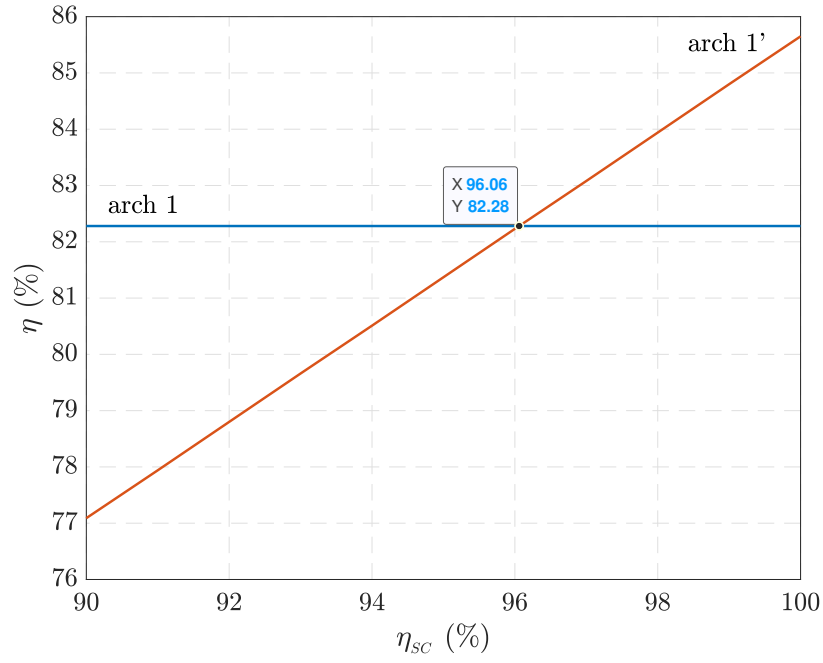


Figure 2-13: Efficiency comparison between Buck-only architecture #1 and architecture #1' possessing a 48 V-24 V SC conversion stage, as a function of the efficiency η_{sc} of the latter.

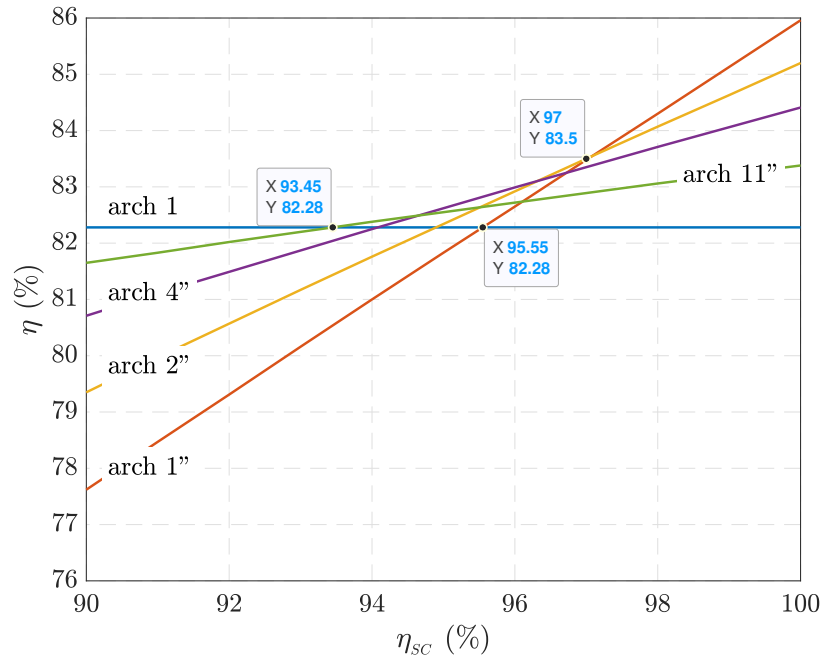


Figure 2-14: Efficiency comparison between Buck-only architecture #1 and architectures #1'', #2'', #4'' and #11'' possessing a 12 V-6 V SC conversion stage, as a function of the efficiency η_{sc} of the latter.

2.3.4 Effects of Battery Voltage Variations

To investigate how the wide battery voltage variations dictated by typical automotive specifications affect the different scenarios examined so far, the efficiency analysis of the various architectural solutions is parameterized in terms of V_{batt} . Fig. 2-15 reports the efficiency comparison between the Buck-only architecture #1 (Tab. 2.4) and architecture #4 (Tab. 2.4) when the latter employs a 90 %-efficient dedicated High Step-Down (HSD) stage for the 48 V-1 V conversion. The comparison confirms the advantages of the latter solution over the entire examined battery variation range.

Fig. 2-16 and Fig. 2-17 report an efficiency comparison between the Buck-only architecture #1 (Tab. 2.4) and the SC-based solutions examined in Scenarios 1 (architecture #1') and Scenario 2 (architecture #1''). In each figure, two assumptions for the efficiency of the SC stage are exemplified, namely $\eta_{sc} = 95\%$ and $\eta_{sc} = 98\%$. Within the test case considered in this study, the inclusion of an intermediate voltage produced by a 98 %-efficient SC converter leads to architectural solutions consistently better than the Buck-only one even in presence of large battery voltage variations.

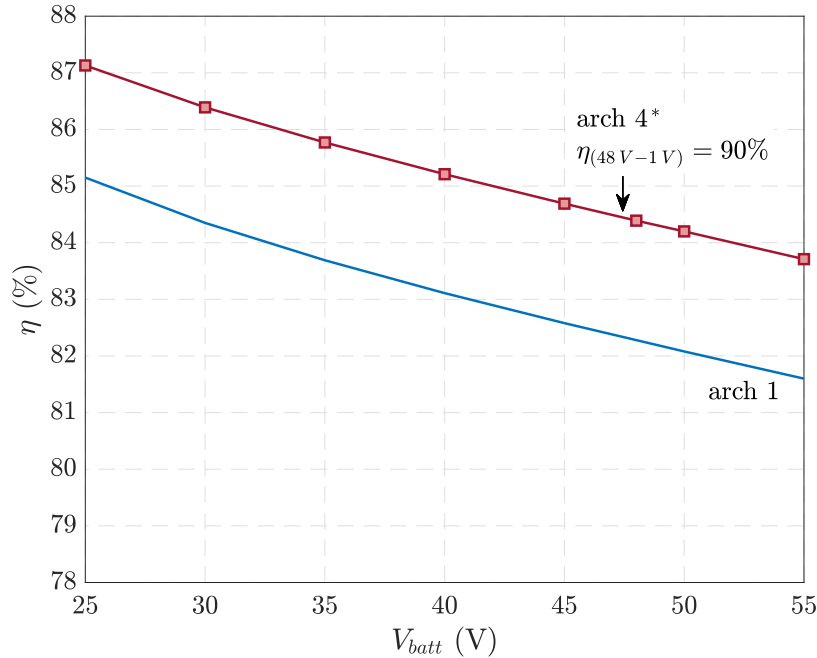


Figure 2-15: Efficiency comparison between Buck-only architecture #1 (Tab. 2.4) and architecture #4 when realized with a 90 %-efficient dedicated 48 V-1 V HSD conversion stage, as a function of the battery voltage.

2.3. Comparative Study of 48 V Architectures

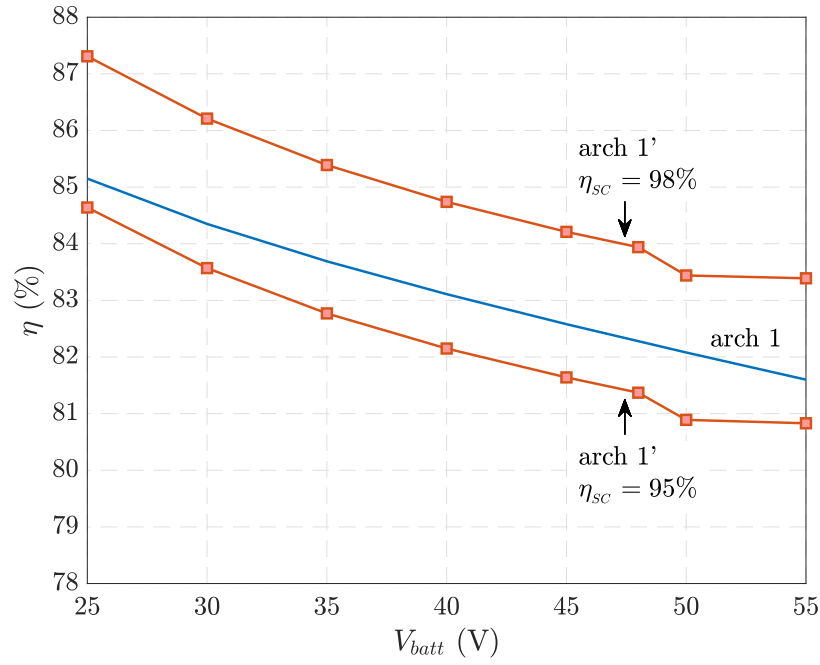


Figure 2-16: Efficiency comparison between Buck-only architecture #1 (Tab. 2.4) and the best architecture #1' possessing a 48 V-24 V SC conversion stage (Tab. 2.5), as a function of the battery voltage.

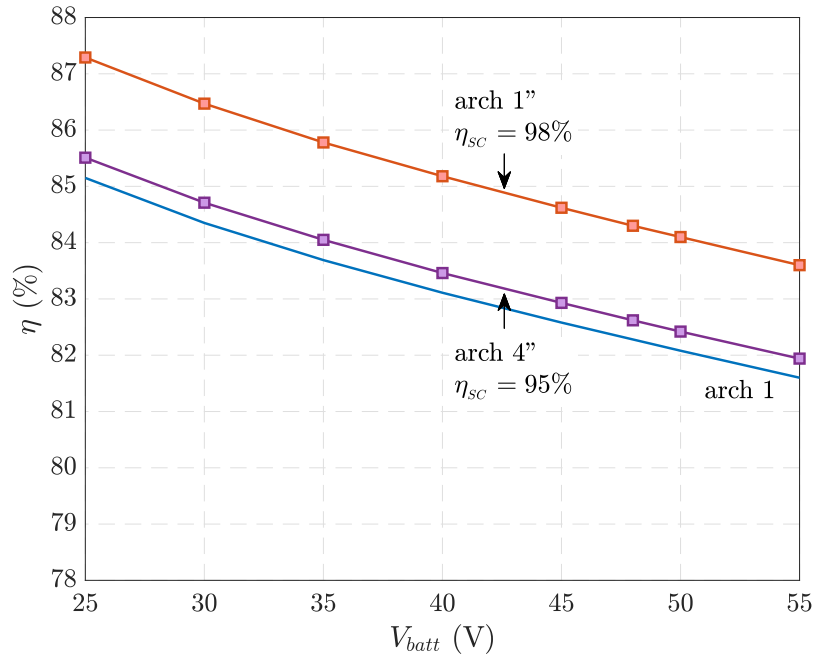


Figure 2-17: Efficiency comparison between Buck-only architecture #1 (Tab. 2.4) and the best architecture #1'' possessing a 12 V-6 V SC conversion stage (Tab. 2.6), as a function of the battery voltage.

Efficiency-wise, the two scenarios yield comparable results. It should be noted, however, that the unregulated 24 V SC output in Scenario 1 would decrease to 12.5 V when $V_{batt} = 25$ V, which could pose challenges for the regulation of the 12 V bus. In this sense, Scenario 2 is to be preferred.

2.3.5 Sensitivity Analysis

In the system-level analysis of a given candidate architecture, it is of interest to quantitatively assess which of its SISO dc-dc stages are the most critical in limiting the overall efficiency.

To this end, define the *efficiency sensitivity* $S_\eta(k)$ of a given architecture with respect to the efficiency η_k of its k -th converter as

$$S_\eta(k) \triangleq \frac{\frac{\partial \eta_{tree}}{\partial \eta_k}}{\frac{\eta_{tree}}{\eta_k}} = \frac{\partial \eta_{tree}}{\partial \eta_k} \cdot \frac{\eta_k}{\eta_{tree}} \quad (2.10)$$

where

- $\partial \eta_k$ accounts for the infinitesimal ϵ variation associated with the efficiency η_k of the k -th converter. In this case, $\partial \eta_k = 0.2\%$ since ϵ is assumed to be equal to 0.1%
- $\partial \eta_{tree}$ is equal to the overall efficiency of the tree when ϵ is added to the efficiency $\partial \eta_k$ of a given edge minus the overall efficiency of the tree when ϵ is subtracted to the efficiency $\partial \eta_k$ of the same edge

To exemplify the use of the above notion, Tab. 2.7 reports all the dc-dc converters involved in architecture #4 (Fig. 2-5b) along with the efficiency sensitivity values, assuming the 48 V-1 V stage is realized by a 90 % efficient dedicated HSD topology. Similarly, Tab. 2.8 and 2.9 report all the dc-dc converters involved in the two SC-based architectures #1' and #1'' (Fig. 2-12a and 2-12b), assuming a 98 % efficiency for the SC converters. In all cases, the most efficiency-sensitive edge is the one carrying the largest amount of power, *i.e.* the 48 V-12 V Buck converter in the first case, the SC converter in the second case, and the 48 V-12 V Buck converter in the last one.

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Table 2.7: Sensitivity results for architecture #4 employing a 48 V-1 V high step-down converter in place of a Buck converter (highest sensitivity edge highlighted in blue)

Edge # k	V_{in} (V)	V_{out} (V)	I_{out} (A)	η_k (%)	$S_\eta(k)$
1	48	1	2.50	90.00	0.21
2	48	12	1.93	91.84	0.87
3	12	3.3	1.00	91.96	0.22
4	12	5 ₁	0.80	93.78	0.33
5	12	5 ₂	0.60	90.35	0.21

Table 2.8: Sensitivity results for architecture #1' employing a 48 V-24 V SC conversion stage (highest sensitivity edge highlighted in blue)

Edge # k	V_{in} (V)	V_{out} (V)	I_{out} (A)	η_k (%)	$S_\eta(k)$
1	48	24	0.62	98.00	1.05
2	24	12	1.18	94.71	1.02
3	12	1	2.50	83.94	0.20
4	12	3.3	1.00	91.96	0.22
5	12	5 ₁	0.80	93.78	0.34
6	12	5 ₂	0.60	90.35	0.22

Table 2.9: Sensitivity results for architecture #1'' employing a 12 V-6 V SC conversion stage (highest sensitivity edge highlighted in blue)

Edge # k	V_{in} (V)	V_{out} (V)	I_{out} (A)	η_k (%)	$S_\eta(k)$
1	48	12	1.15	90.88	1.02
2	12	6	2.25	98.00	0.99
3	6	1	2.50	89.83	0.21
4	6	3.3	1.00	95.47	0.28
5	6	5 ₁	0.80	96.61	0.29
6	6	5 ₂	0.60	95.47	0.23

2.4 Generalization of the CBT Method

To treat a more realistic case focusing on architectures having more than one intermediate or *bus* voltages (and not just one as assumed for the considered case study), notice that each valid CBT architecture/configuration has always the following property:

- k out of n bus voltages have at least one POL voltage among their children;
- $n - k$ out of n bus voltages have no POL voltages among their children, *i.e.* they only feed other bus voltages.

Below are summarized the assumptions made for the CBT methodology:

1. The input voltage is greater than all the other voltages.
2. The largest POL voltage is strictly smaller than the smallest bus voltage.
3. All bus voltages are different from each other.
4. POL voltages are distinguishable, *i.e.* they associate with physically distinct loads.

Note that some of the POL voltages may share the same value.

The objective of this section is to derive an analytical expression to enumerate the valid configurations when the battery-connected architecture has $n \geq 1$ intermediate voltages.

Fig. 2-18 exemplifies two different trees having $n = 3$ bus voltages and $m = 4$ POL voltages. The tree in Fig. 2-18a has $k = 2$ bus voltages (namely 24 V and 12 V) possessing at least one POL voltage as a child node. In Fig. 2-18b, on the other hand, one has $k = 3$ as all bus voltages have a POL voltage among their children. Notice that both trees have the *same* set of voltages, but their structure is different because they originate from different permutations. In general, k can assume values ranging from 1 to $\min(n, m)$.

For a given k , a CBT valid permutation necessarily has the structure illustrated in Fig. 2-19a:

- the leftmost voltage in the permutation is the input voltage of the architecture;
- attached directly to the input voltage is a subset P_0 consisting of zero or more POL voltages, representing POL converters directly connected to the input voltage;

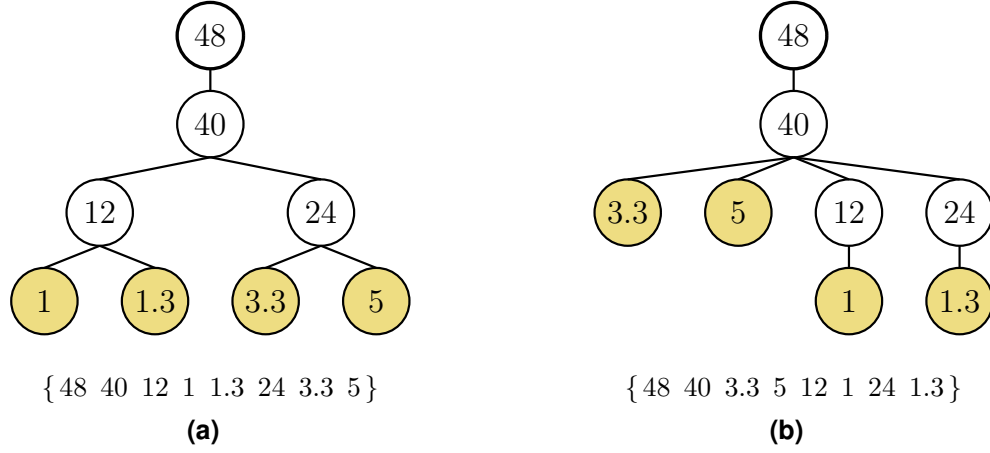


Figure 2-18: Two trees having $n = 3$ bus voltages and $m = 4$ point-of-load voltages, but with (a) $k = 2$, and (b) $k = 3$.

- next, as illustrated in Fig. 2-19a and Fig. 2-19b, there are k non-empty subsets $S_1 \dots S_k$, each composed by one or more bus voltages followed by one or more POL voltages.

It is essential to specify that, as illustrated in Fig. 2-19, bus voltages contained in each S_i must appear in *descending* order (otherwise some of them would become POL voltages), while POL voltages in P_0 and in the S_i 's must appear in *ascending* order (otherwise some of them would become bus voltages). The structure in Fig. 2-19 must be seen as a generalization to the case $n \geq 1$ of the single-bus scenario depicted in Fig. 2-6. The reader can verify that a permutation not compliant with the structure of Fig. 2-19 would not yield a

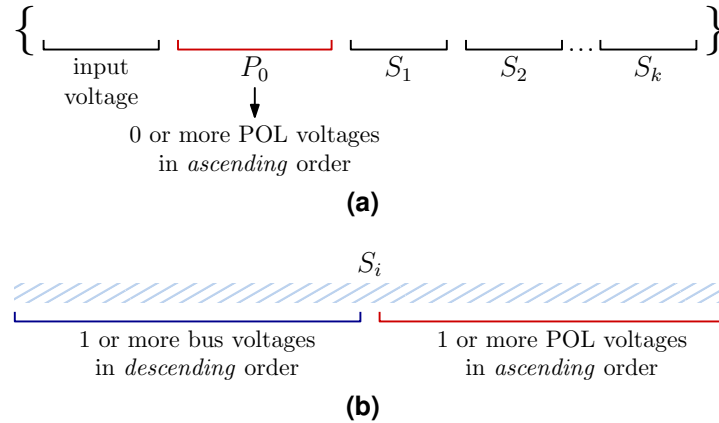


Figure 2-19: (a) General structure of a valid CBT permutation, and (b) composition of generic subset S_i in a valid CBT permutation.

valid CBT.

To exemplify the above idea, consider the permutation and the tree already reported in Fig. 2-18a, for which $k = 2$. The permutation contains subsets $P_0 = \emptyset$, $S_1 = \{40 \ 12 \ 1 \ 1.3\}$ and $S_2 = \{24 \ 3.3 \ 5\}$. Similarly, the permutation of the tree of Fig. 2-18b, for which $k = 3$, consists of subsets $P_0 = \emptyset$, $S_1 = \{40 \ 3.3 \ 5\}$, $S_2 = \{12 \ 1\}$, $S_3 = \{24 \ 1.3\}$.

The above insights on the structure of valid CBT permutations allow to derive general enumeration formulae. In fact, for a *given* k , the number a_k of possible allocations of the n bus voltages in k subsets $S_1 \dots S_k$, *with the constraint that none of the subsets is left empty*, is expressed by the recursive relationship

$$a_k = k^n - \sum_{j=1}^{k-1} a_j \binom{k}{j}, \quad (2.11)$$

with $a_1 = 1$. In the above equation, k^n represents all possible ways to allocate n distinguishable objects (the bus voltages) in k distinguishable boxes (the S_i 's). The summation term, on the other hand, subtracts all the combinations in which at least one of the S_i 's is empty.

By the same token, the number of possible allocations of the m POL voltages in k subsets $S_1 \dots S_k$ *with the constraint that none of the subsets is left empty*, is

$$b_k = k^m - \sum_{j=1}^{k-1} b_j \binom{k}{j}, \quad (2.12)$$

with $b_1 = 1$. Product $a_k b_k$ represents, for a given k , the number of valid trees in which special subset P_0 is *empty*, therefore excluding all architectures having one or more POL converters directly operating off the input voltage. The number of valid trees in which both the S_i 's *and* special subset P_0 are non-empty is, on the other hand, $a_k b_{k+1}$. In summary, the total number of valid architectures/configurations for a *given* k is $a_k (b_k + b_{k+1})$, and the total number N_{CBT} of valid CBT architectures is therefore

$$N_{CBT} = \sum_{k=1}^{\min(n,m)} a_k (b_k + b_{k+1}). \quad (2.13)$$

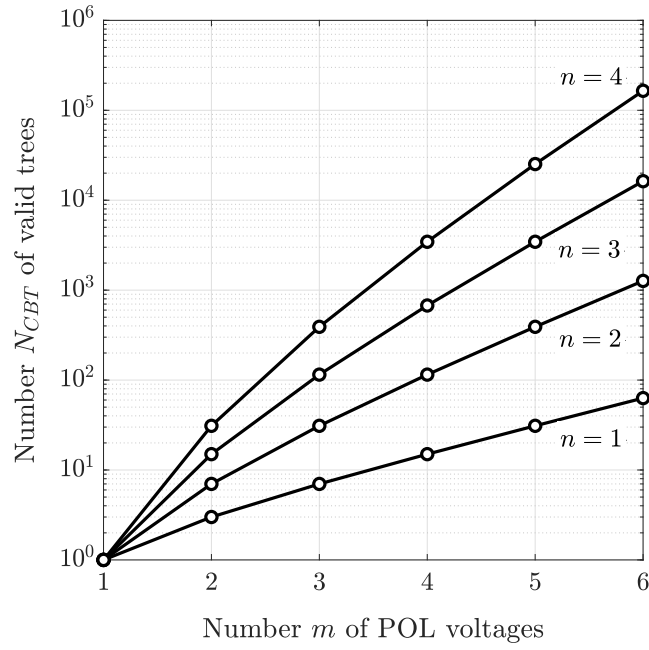


Figure 2-20: Number N_{CBT} of valid architectures as a function of the number m of POL voltages and for different values of n , according to the proposed *Constrained Bucking Trees* approach.

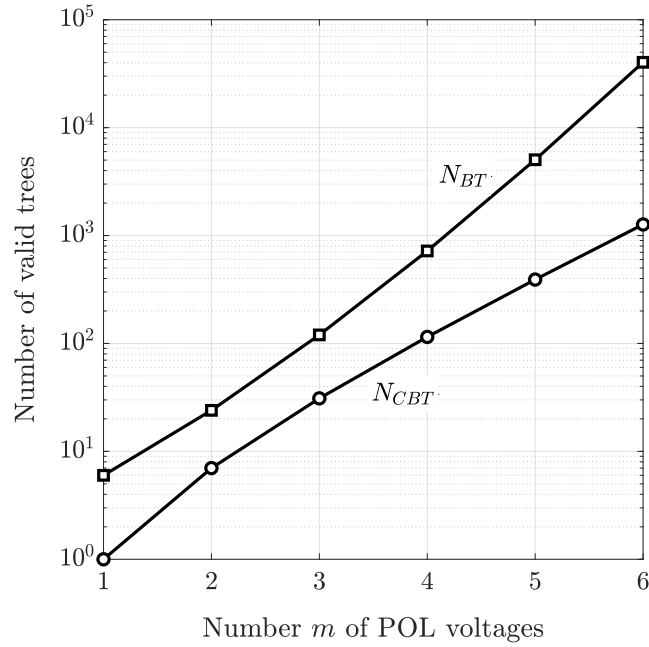


Figure 2-21: Comparison between the number N_{BT} of *Bucking Trees* (squares) and the number N_{CBT} of *Constrained Bucking Trees* (circles) as a function of the number m of POL voltages, for $n = 2$ bus voltages.

It can be verified that the above result reduces to eq. (2.6), *i.e.* $N_{CBT} = 2^m - 1$, when $n = 1$.

Fig. 2-20 illustrates the number N_{CBT} of *Constrained Bucking Trees* as a function of m and for different values of n . Fig. 2-21 compares N_{CBT} with the number $N_{BT} = (n + m)!$ of valid *Bucking Trees* [21, 22], as a function of m and for $n = 2$ bus voltages. As expected, N_{CBT} is always much smaller than N_{BT} .

2.4.1 Generation of the Constrained Bucking Trees

The N_{CBT} valid trees given by (2.13) originate from specific permutations of the $1 + n + m$ assigned voltages, *i.e.* those having the structure shown in Fig. 2-19. Examination of such internal structure not only enables the derivation of enumeration formulae – as done in section 2.1.4 – but provides insight on how to actually *generate* the set of valid solutions, which is of crucial importance in any realistic design / optimization scenario.

Systematic generation of valid CBT permutations can be achieved, for instance, by following the pseudo-code listed in Algorithm 1 (the complete Matlab code is reported in App. B). The code makes use of two recursive functions:

- PLACEBUSVOLTAGES recursively allocates the n bus voltages in various positions within the permutation;
- PLACEPOLVOLTAGES recursively allocates the m POL voltages in various positions within the permutation which are not already occupied by bus voltages.

Once the architecture voltages are specified through variable “inputVoltage” and input arrays “busVoltages” and “polVoltages” (of length n and m respectively), all valid permutations are printed by invoking the function PLACEBUSVOLTAGES(1, permutation), where the array “permutation” is initialized as having the first element occupied by the input voltage, and all the other elements set to zero. As for arrays “busVoltages” and “polVoltages”, their elements must be initialized in descending order and ascending order respectively.

It is worth noticing that the recursion depth of the proposed algorithm implementation only goes as $\Theta(n + m)$, *i.e.* it is linear with the total number of voltages in the architecture.

Algorithm 1 Generation of the valid CBT permutations

Input: inputVoltage, busVoltages, polVoltages, n , m

Output: Printout of all valid permutations

```

1: function PLACEBUSVOLTAGES( $j$ , permutation)
2:   if  $j > n$  then
3:     PLACEPOLVOLTAGES(1, permutation)
4:   else
5:     for  $i \leftarrow 2$  to  $(1 + n + m) - 1$  do
6:       if (permutation[ $i$ ] = 0 and
7:         permutation[ $i + 1$ ] = 0) then
8:         perm_new  $\leftarrow$  permutation
9:         perm_new[ $i$ ]  $\leftarrow$  busVoltages[ $j$ ]
10:        PLACEBUSVOLTAGES( $j + 1$ , perm_new)
11:       end if
12:     end for
13:   end if
14: end function
15:
16: function PLACEPOLVOLTAGES( $j$ , permutation)
17:   if  $j > m$  then
18:     print(permutation)
19:   else
20:     for  $i \leftarrow 2$  to  $(1 + n + m)$  do
21:       if (permutation[ $i$ ] = 0 and
22:         permutation[ $i - 1$ ]  $\neq$  0) then
23:         perm_new  $\leftarrow$  permutation
24:         perm_new[ $i$ ]  $\leftarrow$  polVoltages[ $j$ ]
25:         PLACEPOLVOLTAGES( $j + 1$ , perm_new)
26:       end if
27:     end for
28:   end if
29: end function

```

Chapter 3

Active-Clamped Isolated SEPIC Converter in the MHz Range

3.1 Introduction

In the automotive architecture shown in Fig. 2-2, a variety of low-power electronic loads – *such as* sensors, micro-controllers, and communication transceivers – are supplied by the 48 V main battery through an intermediate 12 V bus [30]. In case of failure of the latter, the system is sustained by a 12 V backup battery as shown in Fig. 3-1. The isolated dc-dc converter interfacing the backup battery with the low-power 12 V intermediate bus must operate efficiently over the wide 9 V-18 V automotive input voltage range, while keeping magnetic size and overall footprint at a minimum. Presently adopted solutions at the industry level are based on the flyback topology with Silicon devices, a poorly efficient solution mostly justified by its low component count and reduced footprint.

In this study, a 2 MHz GaN-based active-clamped isolated SEPIC converter (ACISC) [13,14] is considered a viable substitute for the battery-connected application. In particular, the ACISC is here operated in resonant discontinuous conduction mode (DCM) operation to achieve soft rectifier diode turn OFF, *i.e.* with low di/dt , while ensuring full zero-voltage switching (ZVS) of the switches throughout the operating range. While the ACISC topology has been the subject of several studies [31–38], along with similar topologies such as the active-clamped isolated flyback converter (ACIFC) [39–42], and the asymmetrical

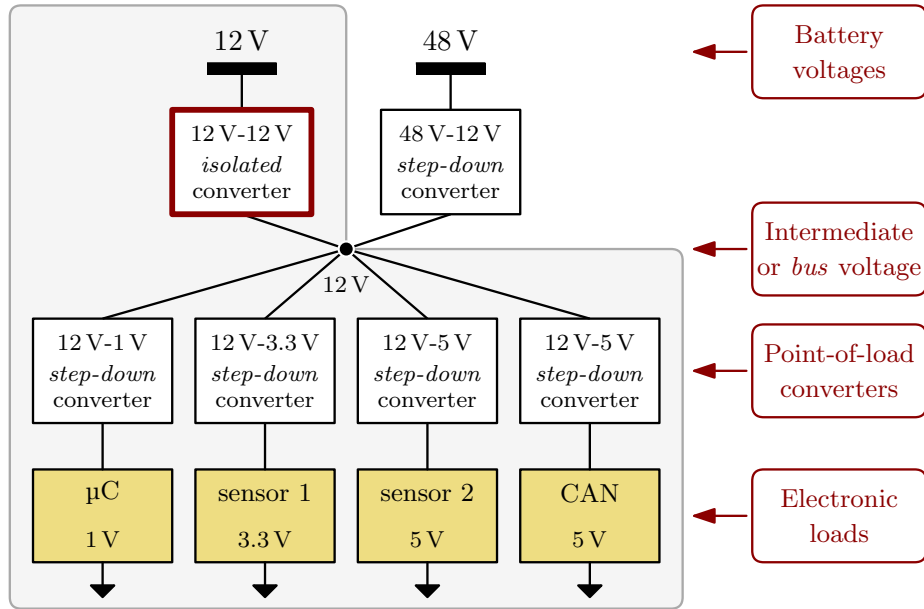


Figure 3-1: Example of a dual-battery 48 V/12 V automotive scenario referred to Fig. 2-1b, where the 12 V backup battery supplies the entire system and the 48 V main battery is disconnected. POL are highlighted in yellow.

half-bridge flyback converter (AHBFC) [43–46], its design and operation in resonant DCM are still unexplored. For this reason, the contribution of this chapter is to provide a design methodology to operate the ACISC in resonant DCM while focusing on high-frequency low-power automotive applications.¹ This chapter is organized as follows. Section 3.2 introduces the topology and its operation in continuous conduction mode (CCM) while explaining the differences with other isolated topologies. Section 3.3 explains the converter’s operation in resonant DCM while highlighting the advantages of this operating mode (section 3.3.1). In section 3.3.2 the analytical expression of M , necessary to develop the theoretical model of the converter, is derived. Section 3.3.3 addresses the design methodology for the ACISC in order to guarantee full ZVS for both switches over the entire input voltage variation, along with the design and implementation of the planar transformer. To conclude, section 3.4 reports the experimental measurements taken on a 12 V, 600 mA GaN-based prototype running at 2 MHz. In this section, the efficiency profile of the ACISC is compared with that of a 400 kHz commercial flyback operating in CCM intended for the same application, and having the same input/output voltage and rated current specifications.

¹Although here it is considered a battery-connected scenario, the ACISC (*e.g.*, operating in resonant DCM) can also be used to generate the isolated gate driver power supply for MOSFETs ($V_{out} \sim 15$ V).

3.2 Theoretical Study of the Converter in CCM

As mentioned in the introduction, presently adopted solutions at the industry level are based on the flyback topology with Silicon devices. The schematic of the flyback converter, along with the adopted model for its transformer, is shown in Fig. 3-2.

In this thesis, a given $n : 1$ transformer with $n \triangleq n_1/n_2^2$, is modeled by an equivalent primary-side leakage inductance L_{pe} , an equivalent primary-side magnetizing inductance L_{me} , and an equivalent turns ratio n_e . Although a flyback converter is an excellent topology with benefits such as low cost, low component count and reduced footprint, it has several drawbacks. The field-effect transistor (FET) and rectifier ringing associated with flyback transformer leakage inductance creates electromagnetic interference (EMI), raises component stresses and lowers the efficiency profile. In addition, the flyback converter needs a voltage clamping circuit since, at the turn-OFF of the switch, the stored energy in the transformer leakage inductance causes dangerous voltage spikes and ringing across the switch. For this reason, an isolated single-ended primary-inductor converter (SEPIC) can provide an alternative approach and alleviate some of these issues. Although the SEPIC is a non-isolated topology, one can easily add additional transformer windings to create isolated outputs as with a flyback converter. The schematic of the isolated SEPIC is shown in Fig. 3-2. An isolated SEPIC is currently used in switching mode power supplies because of its advantages such as simplicity, high power density, wide input range, and higher immunity to leakage inductance associated ringing than a flyback converter (which can improve output voltage regulation). This may eliminate the need for additional post-regulation, resulting in cost savings. However, as reported in [47], the conventional isolated SEPIC suffers from the disadvantage of

- low efficiency
- diode reverse recovery
- transformer proximity losses
- losses due to energy stored in the transformer's leakage inductance

²parameters n_1 and n_2 are the primary and secondary turns, respectively.

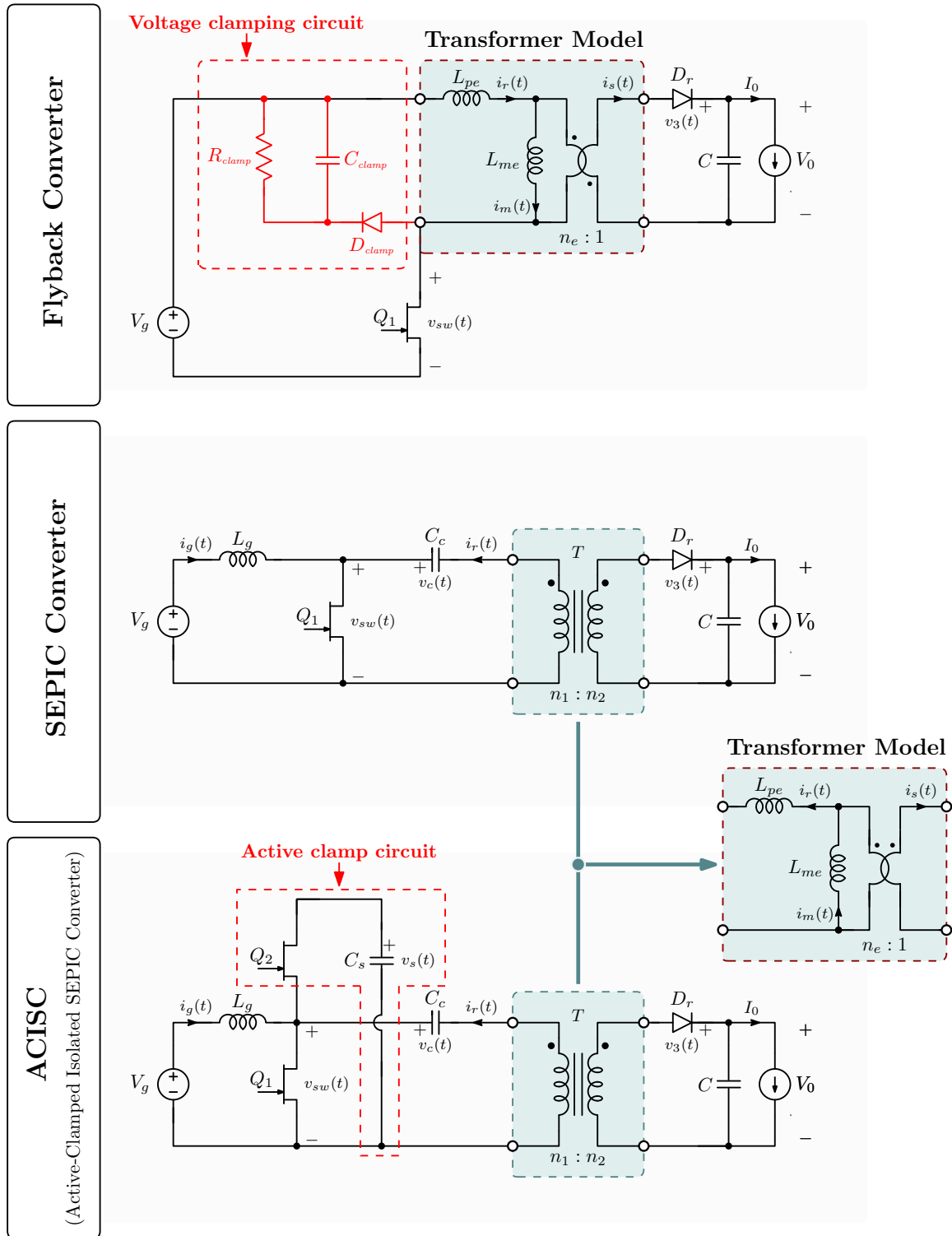


Figure 3-2: Schematics of the flyback converter, isolated SEPIC converter, and active-clamped isolated SEPIC converter (ACISC), highlighting the adopted model for the high-frequency transformer. The voltage clamping circuit for the flyback and active clamp circuit for ACISC are also highlighted.

For this reason, an active clamp circuit for the isolated SEPIC converter is proposed in this thesis – giving rise to the active-clamped isolated SEPIC converter (ACISC) shown in Fig. 3-2 – to further improve the efficiency of the converter and clamp the turn-OFF voltage spike on its transistor thanks to the presence of the clamp capacitor C_s . As can be seen in Fig. 3-2, the active clamp circuit consists of a secondary switch Q_2 and a clamp capacitor C_s . The specific ACISC topology is chosen for the considered battery-connected application shown in Fig. 3-1 since it is capable of improving the converter's efficiency by using the transformer leakage inductance L_{pe} to achieve zero-voltage switching (ZVS) of the transistors Q_1 and Q_2 . If the ACISC is designed with a negligible voltage ripple across capacitor C_c , thus having $v_c(t) \approx V_c = V_g$, piece-wise linear current/voltage waveforms are obtained, and the converter is likely to operate in continuous conduction mode (CCM), as shown in Fig. 3-3. Such a figure illustrates both the trend and the slopes of the following waveforms: input current $i_g(t)$, resonant current $i_r(t)$, magnetizing current $i_m(t)$, output diode current $i_s(t)$, together with the voltage stresses across both the switches and the output diode. Applying the *volt-second* balance on L_g it is possible to derive the average value of the voltage across the clamp capacitor: $V_s = V_g/(1 - D)$, where D is the duty cycle of the low-side switch Q_1 . As can be noted in Fig. 3-3 and looking at Tab. 3.1, in CCM operation a switching period T_s consists of three subintervals:

$$T_s = \underbrace{D_f T_s + (DT_s - D_f T_s)}_{Q_1 \text{ is ON}} + \underbrace{(1 - D)T_s}_{Q_2 \text{ is ON}} \quad (3.1)$$

where diode D_r is OFF only in the second subinterval, which is the reason why the two currents $i_m(t)$ and $i_r(t)$ coincide. In section 3.2.1 the two analytical expressions of the voltage gain M , necessary to develop the theoretical model of the converter in CCM, are derived and then compared together with simulated data points.

Table 3.1: Subintervals shown in Fig. 3-3 over a switching period T_s

	Subinterval	Q_1	Q_2	D_r	resonance ?
1	$D_f T_s$	ON	OFF	ON	X
2	$DT_s - D_f T_s$	ON	OFF	OFF	X
3	$(1 - D)T_s$	OFF	ON	ON	X

3.2. Theoretical Study of the Converter in CCM

Active-Clamped Isolated SEPIC Converter (ACISC)

CCM operation

- The following curves and slopes are derived assuming: $v_c(t) \approx V_c = V_g$
- Definition of some key parameters: $\lambda = L_{pe}/L_{me}$, $V_s = V_g/(1-D)$
- D is the duty cycle of the low-side switch Q_1

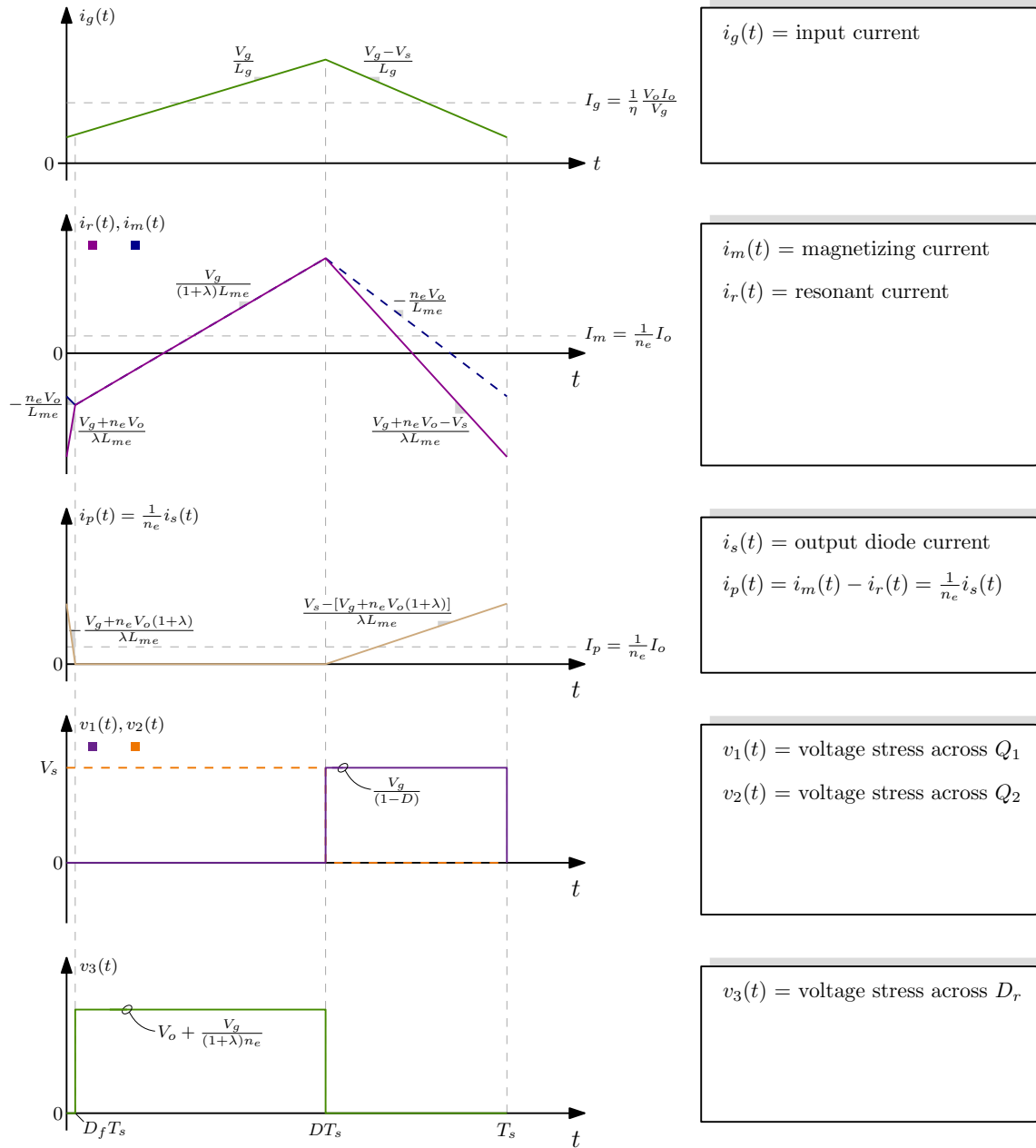


Figure 3-3: Converter waveforms in CCM operation over a switching period.

3.2.1 Voltage Gain Analysis

First expression: how to derive M_1^{CCM}

With piecewise linear current waveforms, as shown in Fig. 3-3, an approximated voltage gain expression M_1^{CCM} can be easily derived once the following assumptions are made:

- capacitor C_c has a negligible voltage ripple: $v_c(t) \approx V_c = V_g$
- the small subinterval $D_f T_s$ is neglected: $D_f T_s = 0$

In this situation, the *volt-second* balance on the magnetizing inductance L_{me} gives the following equation

$$\begin{aligned} V_{L_{me}} &= \frac{1}{T_s} \int_0^{T_s} v_{L_{me}}(t) dt = \frac{1}{T_s} \left[\int_0^{DT_s} \left(\frac{V_g}{L_{me} + L_{pe}} \right) \cdot L_{me} dt + \int_{DT_s}^{T_s} \left(-\frac{n_e V_o}{L_{me}} \right) \cdot L_{me} dt \right] = \\ &= \frac{1}{T_s} \left[\frac{V_g}{1 + \lambda} DT_s - n_e V_o (1 - D) T_s \right] \stackrel{ss}{=} 0 \end{aligned} \quad (3.2)$$

where it is possible to derive either the voltage gain expression as a function of the duty cycle D

$$M_1^{CCM} \triangleq \frac{V_o}{V_g} = \frac{D}{1 - D} \frac{1}{n_e(1 + \lambda)} \quad (3.3)$$

and the expression of D as a function of the voltage conversion ratio $M = M_1^{CCM}$

$$D = \frac{n_e(1 + \lambda)M}{1 + n_e(1 + \lambda)M}. \quad (3.4)$$

Such voltage gain expression is load (I_o) and frequency (f_s) independent, and the majority of the papers dealing with this topology adopt this approximation. However, since it does not consider the presence of the time interval $D_f T_s$, the above relation does not correctly predict the converter behaviour, as it is going to be demonstrated hereafter.

Second expression: how to derive M_2^{CCM}

In order to obtain a more precise equation for the steady-state dc-dc conversion ratio M , the presence of the small subinterval $D_f T_s$ is here considered even if the voltage ripple across

3.2. Theoretical Study of the Converter in CCM

C_c is still neglected ($v_c(t) \approx V_c = V_g$). The volt-second balance on L_g and L_{me} gives the following two equations

$$V_s = \frac{V_g}{1-D} \quad (3.5)$$

$$M_2^{CCM} \triangleq \frac{V_o}{V_g} = \frac{D-D_f}{1-D+D_f} \cdot \frac{1}{n_e(1+\lambda)} \quad (3.6)$$

where (3.6) can be rewritten to find the expression of D_f as a function of the voltage gain

$$M = M_2^{CCM}$$

$$D_f = \frac{D - n_e(1-D)(1+\lambda)M}{1 + n_e(1+\lambda)M} \quad (3.7)$$

Looking at the slopes shown in Fig. 3-3 for the current waveform $i_p(t) = i_s(t)/n_e$, charge balance on the output capacitor C provides the following relation

$$\frac{I_s}{n_e} = \frac{1}{T_s} \left[\int_0^{D_f T_s} \left| -\frac{V_g + n_e V_o(1+\lambda)}{\lambda L_{me}} \right| \cdot t \, dt + \int_{D_f T_s}^{T_s} \frac{V_s - V_g - n_e V_o(1+\lambda)}{\lambda L_{me}} \cdot t \, dt \right] \stackrel{ss}{=} \frac{I_o}{n_e} \quad (3.8)$$

which brings to

$$M_2^{CCM} \triangleq \frac{V_o}{V_g} = \frac{n_e V_o T_s}{2 I_o \lambda L_{me}} \left\{ [D(1-D) + D_f^2] [1 + n_e(1+\lambda)M] - n_e(1-D)(1+\lambda)M \right\} \quad (3.9)$$

Inserting (3.7) into (3.9) – with the aim of eliminating the dependence on D_f – brings to the final expression of the voltage gain

$$M_2^{CCM} \triangleq \frac{V_o}{V_g} = \underbrace{\frac{D}{1-D} \frac{1}{n_e(1+\lambda)}}_{M_1^{CCM}} \cdot \underbrace{2 \left(1 + \frac{\xi}{1-D} + \sqrt{\left(1 + \frac{\xi}{1-D} \right)^2 + \frac{4\xi D}{(1-D)^2}} \right)^{-1}}_{\text{corrective factor}} \quad (3.10)$$

where

$$\xi = \underbrace{2 \frac{(L_{me} \parallel L_{pe}) I_o}{n_e^2 V_o}}_{\text{active load } (I_o)} f_s = \underbrace{2 \frac{(L_{me} \parallel L_{pe})}{n_e^2 R_o}}_{\text{resistive load } (R_o)} f_s \quad (3.11)$$

is now load (I_o) and frequency (f_s) dependent. Such expression – which assumes there is an active load (I_o) connected to the converter – can be rewritten considering a resistive load (R_o), i.e. substituting I_o/V_o with R_o^{-1} . Further manipulating (3.10), it is possible to derive

the expression of duty cycle D as a function of the voltage conversion ratio $M = M_2^{CCM}$

$$D = \frac{n_e(1 + \lambda)M}{1 + n_e(1 + \lambda)M} \left[1 + \xi [1 + n_e(1 + \lambda)M] \right] \quad (3.12)$$

The above results, (3.3) and (3.10), are used in Fig. 3-4 to plot M_1^{CCM} and M_2^{CCM} as a function of D . The figure, which also reports simulated data points, refers to a converter design in CCM not disclosed in this thesis. As expected, the accuracy of M_2^{CCM} allows it to perfectly fit simulated data points due to the fact that subinterval $D_f T_s$ is now taken into account.

Parameter	Symbol	Value	Unit
Output voltage	V_o	12	V
Output resistance	R_o	20	Ω
Equivalent magnetizing inductance	L_{me}	160	μH
Equivalent turns ratio	n_e	1	
Inductance ratio	λ	2	%
Switching frequency	f_s	500	kHz

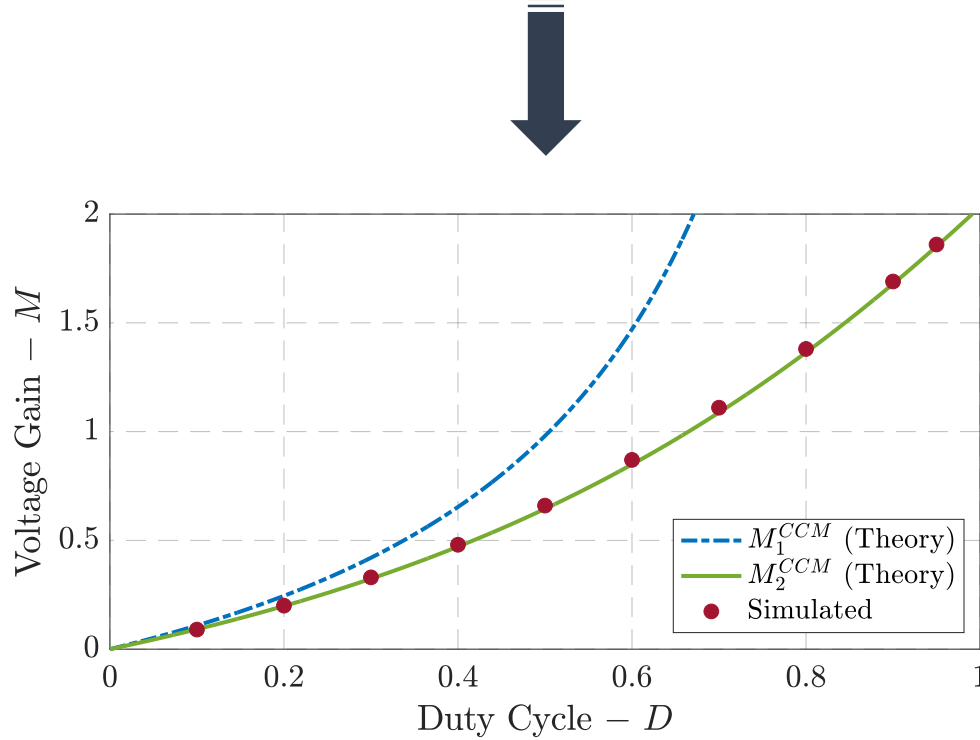


Figure 3-4: Voltage gain comparison between theoretical models and simulated data points for a 500 kHz ACISC operating in CCM. Values of the parameters involved in the two analytical expressions are listed in the table reported above.

3.3 Theoretical Study of the Converter in Resonant DCM

The ACISC topology originates from the integration of a boost *stage* with an asymmetrical half-bridge flyback converter (AHBFC) [43–46], sharing the same switches. Fig. 3-5 reports the schematic diagram of the ACISC employing two enhancement-mode GaN devices. Converter magnetics consist of input inductor L_g and a high-frequency transformer T . In the following, the latter will be modeled by an equivalent primary-side leakage inductance L_{pe} , an equivalent primary-side magnetizing inductance L_{me} , and an equivalent turns ratio n_e . Elements C_s , C_c and C are the clamping capacitor, the resonant capacitor, and the output filter capacitor, respectively.

In the following, small-ripple approximation is assumed for both the clamp and output capacitor, but not for the resonant one.

The selected ACISC topology features:

- galvanic isolation,
- low input current ripple,
- reduced voltage stresses,
- full zero-voltage switching (ZVS) operation for both switches.

Combined with the use of GaN technology, the above features make the ACISC an attractive topology for significantly increasing both the efficiency *and* the switching rate. In

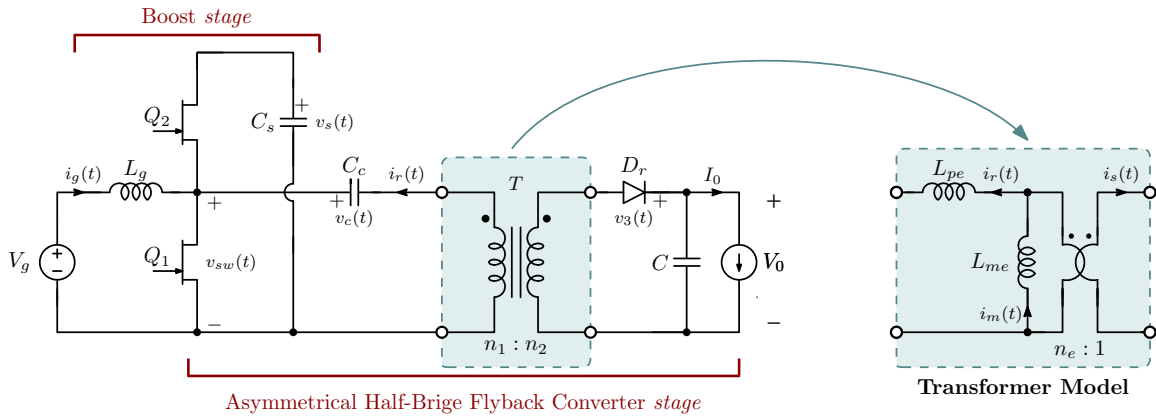


Figure 3-5: Schematic of the GaN-based active-clamped isolated SEPIC converter (ACISC), highlighting the adopted model for the high-frequency transformer.

addition, galvanic isolation is necessary to separate the two voltage domains (12 V, 48 V), as shown in Fig. 1-8.

Assuming steady-state operation and indicating average quantities with uppercase symbols, the inductors' flux balance and the capacitors' charge balance principles yield

$$\begin{cases} V_c = V_g \\ V_s = V_g/(1 - D) \\ I_r = 0 \\ I_m = I_o/n_e \end{cases}, \quad (3.13)$$

where D is the duty cycle of the low-side switch Q_1 . Fig. 3-6 shows the main converter waveforms in one of the possible resonant DCM operations. Such a figure shows the resonant voltage waveform $v_c(t)$, the input current $i_g(t)$, the resonant current $i_r(t)$ and the

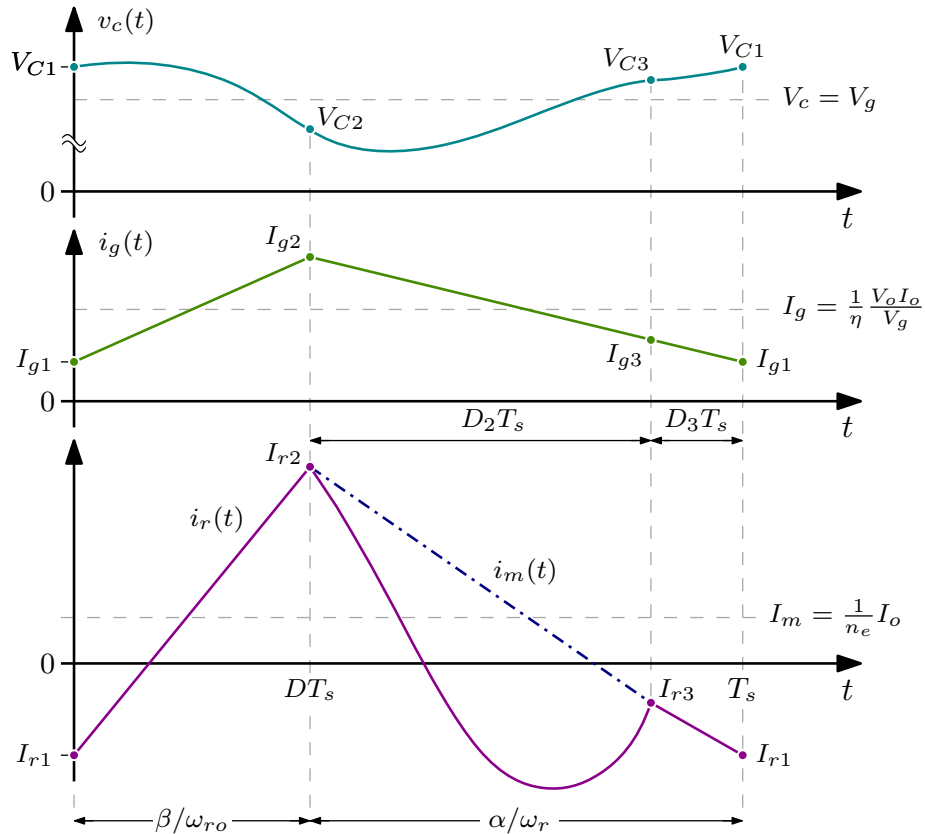


Figure 3-6: Example of converter waveforms in resonant DCM operation over a switching period.

magnetizing current $i_m(t)$, together with their average value. Here, DCM is defined by the output diode D_r being OFF during a fraction of subinterval $(1-D)T_s$ (see subinterval D_3T_s in Fig. 3-6). The ACISC subtopologies which appear during the three different subintervals (DT_s , D_2T_s and D_3T_s) are shown in Fig. 3-7.

Define first λ as the inductance ratio between the equivalent leakage inductance L_{pe} and magnetizing inductance L_{me} ,

$$\lambda \triangleq \frac{L_{pe}}{L_{me}}. \quad (3.14)$$

Furthermore, define the characteristic impedance and natural resonant frequency of the active resonant network when D_r is ON,

$$Z_r \triangleq \sqrt{\frac{L_{pe}}{C_c}}, \quad \omega_r \triangleq \frac{1}{\sqrt{L_{pe}C_c}}, \quad (3.15)$$

and when D_r is OFF,

$$Z_{ro} \triangleq \sqrt{\frac{L_{pe} + L_{me}}{C_c}}, \quad \omega_{ro} \triangleq \frac{1}{\sqrt{(L_{pe} + L_{me})C_c}}. \quad (3.16)$$

With these preliminary definitions, operation of the converter in the various subintervals can be summarized as follows:

- Interval $0 \leq t \leq DT_s$ (Fig. 3-7a)

At $t = 0$, the main switch Q_1 is turned ON, while diode D_r is already OFF. Thus, the two currents $i_r(t)$ and $i_m(t)$ increase, in a resonant manner, under the effect of the total voltage $v_c(t)$ applied to them. As can be seen in Fig. 3-6, the currents increase almost linearly since the condition $\omega_{ro}T_s \ll 2\pi$ is verified. At the same time, the input current $i_g(t)$ linearly increases with a slope equal to V_g/L_g .

- Interval $DT_s \leq t \leq (D + D_2)T_s$ (Fig. 3-7b)

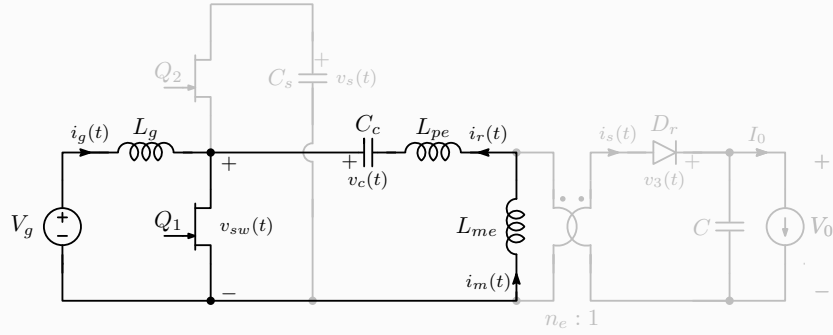
After the commutation of the two switches (turn-OFF of Q_1 followed by the turn-ON of Q_2), if the condition

$$\frac{V_s - v_c(DT_s)}{1 + \lambda} > n_e V_o \quad (3.17)$$

is verified, the output diode D_r is immediately turned ON, starting the energy transfer

Subtopology 1

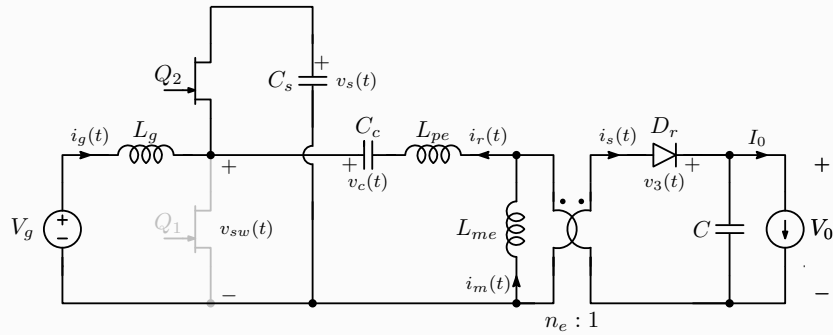
Subinterval: $0 \leq t \leq DT_s$



(a)

Subtopology 2

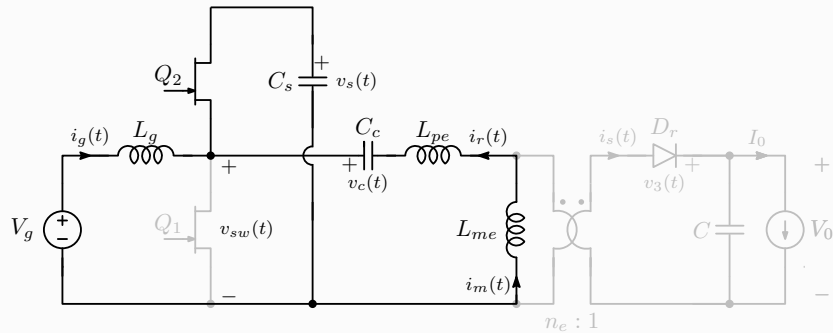
Subinterval: $DT_s \leq t \leq (D + D_2)T_s$



(b)

Subtopology 3

Subinterval: $(D + D_2)T_s \leq t \leq T_s$



(c)

Figure 3-7: Subtopologies in a switching period when the converter is operating in resonant DCM operation as depicted in Fig. 3-6. (a) During subinterval DT_s , (b) during subinterval D_2T_s , and (c) during subinterval D_3T_s .

phase toward the output. The magnetizing current $i_m(t)$ decreases linearly, since the voltage across L_{me} is equal to $-n_e V_o$, while C_c and L_{pe} continue to resonate. In this subinterval, where Q_2 is conducting, the input current decreases linearly with a slope equal to $(V_g - V_s)/L_g$.

In case (3.17) is *not* verified, a small subinterval appears, following time instant $t = DT_s$ (refer to Fig. 3-7c), in which voltage $v_c(t)$ would continue to decrease until the turn-ON of the rectifier diode D_r . This situation represents another example of a resonant DCM operation, which is likely to occur at light load.

- Interval $(D + D_2)T_s \leq t \leq T_s$ (Fig. 3-7c)

At $t = (D + D_2)T_s$ the rectifier diode D_r turns-OFF, because the resonant current $i_r(t)$ becomes equal to the magnetizing current $i_m(t)$. This event initiates the last subinterval D_3T_s , during which both currents coincide, and continue to decrease in a resonant manner.

Under the already mentioned small-ripple approximation for the clamp and output capacitors, expressions of the resonant capacitor voltage $v_c(t)$ and of the resonant current $i_r(t)$ are

$$\begin{cases} v_c(t) = -Z_o I_{ri} \sin[\omega_o(t - t_i)] + (V_{Ci} - V_x) \cos[\omega_o(t - t_i)] + V_x \\ i_r(t) = \frac{1}{Z_o} (V_{Ci} - V_x) \sin[\omega_o(t - t_i)] + I_{ri} \cos[\omega_o(t - t_i)] \end{cases}, \quad (3.18)$$

with t_i ($i = 1, 2, 3$) representing the beginning of each subinterval ($t_1 = 0$). Expressions of V_x , Z_o and ω_o , which depend on the considered subinterval, are reported in Tab. 3.2.

Table 3.2: Coefficients used in (3.18) for voltage and current equations in resonant DCM operation

Interval	V_x	Z_o	ω_o	subtopology	Q_1	Q_2	D_r	resonance ?
DT_s	0	Z_{ro}	ω_{ro}	Fig. 3-7a	ON	OFF	OFF	✓
D_2T_s	$V_s - n_e V_o$	Z_r	ω_r	Fig. 3-7b	OFF	ON	ON	✓
D_3T_s	V_s	Z_{ro}	ω_{ro}	Fig. 3-7c	OFF	ON	OFF	✓

3.3.1 Reasons Why ACISC is Operated in Resonant DCM

Fig. 3-8 shows the trend of the input current $i_g(t)$, resonant current $i_r(t)$ and magnetizing current $i_m(t)$ when the ACISC is operated under three operating modes:

1. Continuous Conduction Mode (CCM)
2. Resonant CCM
3. Resonant DCM

Looking at the first two operating modes, CCM and resonant CCM, output diode D_r is ON either when Q_2 is ON (after $t = DT_s$) and until $i_r(t)$ equals $i_m(t)$ at $t = D_f T_s$. The main reasons why the ACISC is here operated in resonant DCM rather than CCM or resonant CCM operation are mentioned as follows.

- ✓ As shown in Fig. 3-8, when the ACISC is operated in CCM and resonant CCM operations, D_r is turned-OFF with high di/dt . On the other hand, when the converter is operating in resonant DCM the output diode D_r is turned-OFF with low di/dt , avoiding steep turn-OFF fronts and, more importantly, additional resonances. The last aspect is crucial in this work because, as it will be proved later, the resonant current waveform $i_r(t)$ is already affected by resonances generated by the use of interleaved planar magnetics in the MHz range. For this reason, reducing additional resonances allows to improve both the converter's behavior and electromagnetic interference (EMI) noise aspects.
- ✓ No need for a precise transformer leakage inductance value L_{pe} , since the resonant operation can always be ensured by adjusting the value of the resonant capacitor C_c . In other words, for a given value of L_{pe} it is always possible to operate the converter in resonant DCM by changing the value of C_c giving rise to subinterval $D_3 T_s$. This represents a big advantage because, in the realization of planar transformers, it is difficult to have a strong control over L_{pe} as it happens with L_{me} .
- ✓ Considering the currents available at the switching node at the switching instant and looking at the ACISC resonant DCM waveforms shown in Fig. 3-8, the ZVS transi-

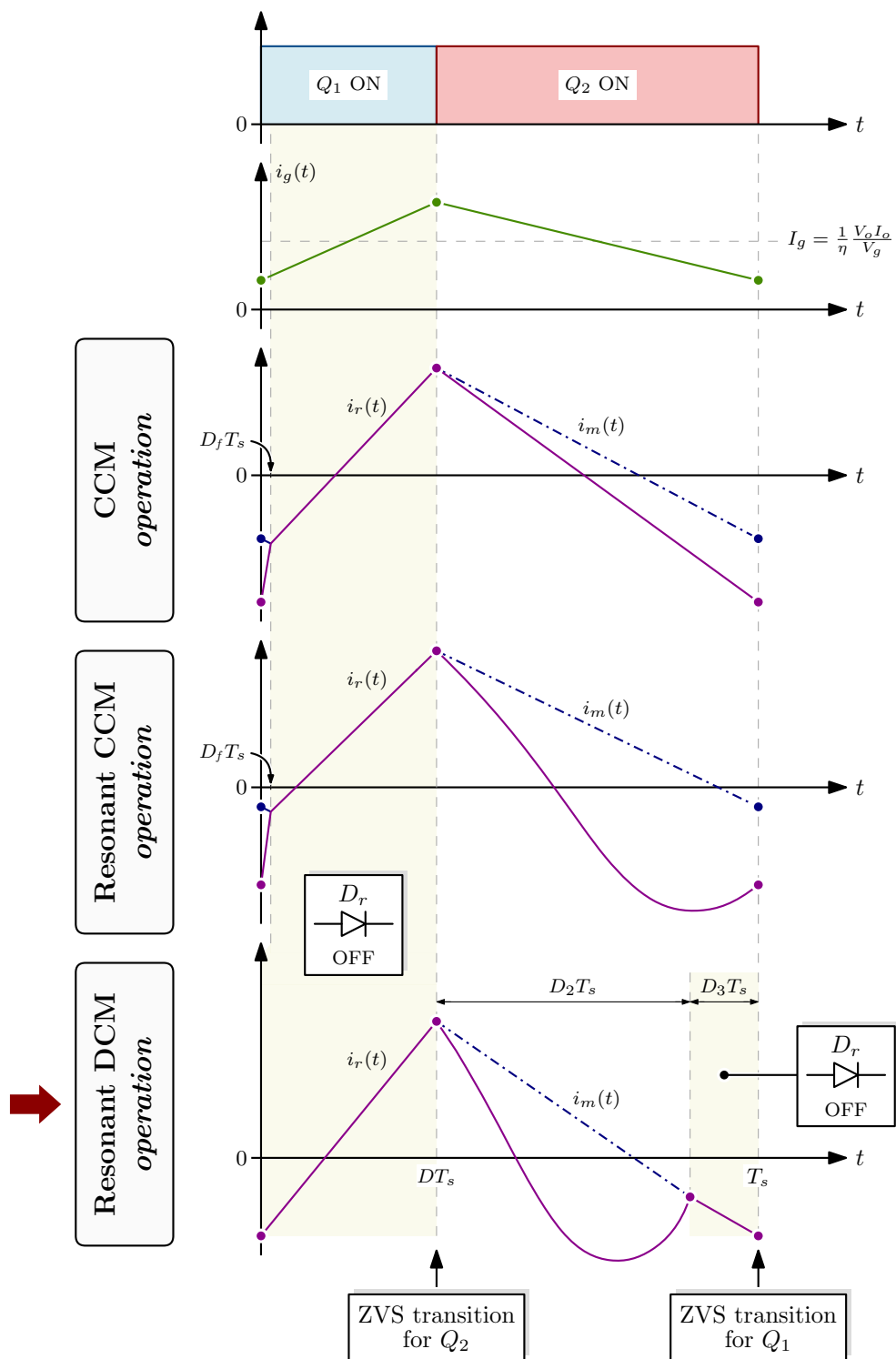


Figure 3-8: Converter waveforms over a switching period when the ACISC is operated in CCM, resonant CCM, and resonant DCM operation (highlighted areas mean that the output diode D_r is OFF).

tion for Q_1 and Q_2 depends on both the input current $i_g(t)$ and the resonant current $i_r(t)$. The latter, which is equal to $i_m(t)$ during both transitions, can be easily estimated analytically at $t = DT_s$ and $t = T_s$ since an approximated triangular waveform can be assumed for $i_m(t)$. On the other hand, CCM and resonant CCM operations call for a precise estimation of L_{pe} to correctly estimate $i_r(T_s)$ since $i_r(T_s) \neq i_m(T_s)$. In addition, the estimation of $i_r(T_s)$ in resonant CCM is further complicated by its non-linear behaviour.

To achieve the aforementioned benefits given by the DCM operation, the ACISC topology must be operated in resonant mode. In fact, non-resonant operation forces the converter to always operate in CCM, even for very low output current values [31].

3.3.2 Voltage Gain Analysis

An approximate analysis is presented in this section to relate the voltage gain $M \triangleq V_o/V_g$ and the duty cycle D of Q_1 in resonant DCM operation. When the value of the resonant capacitor C_c is reduced to allow resonant operation, its voltage ripple is significant, and cannot be neglected for a correct analytical study of the converter. An approximated closed loop solution can be found for the particular operating point corresponding at the boundary between resonant CCM and DCM operation, *i.e.*, assuming subinterval $D_3T_s = 0$ in Fig. 3-6 (a similar approach was used in [46] for the AHBFC topology). The derived voltage gain formula yields values close to the simulated ones even when the converter enters DCM. The reason for such result will be explained in the following. Thus, considering the boundary CCM/DCM operating point, the flux balance on L_{me} yields

$$V_{L_{me}} = \frac{1}{T_s} \int_0^{DT_s} \frac{v_c(t)}{1 + \lambda} dt - n_e V_o (1 - D) \stackrel{ss}{=} 0. \quad (3.19)$$

By defining

$$V_y \triangleq \frac{1}{T_s} \int_0^{DT_s} v_c(t) dt, \quad (3.20)$$

(3.19) can be re-written as

$$V_o = \frac{1}{n_e(1 + \lambda)} \frac{V_y}{1 - D}. \quad (3.21)$$

The expression of V_y , from the first equation in (3.18), is given by

$$V_y = \frac{f_s}{\omega_{ro}} [V_{C1} \sin \beta - Z_{ro} I_{r1} (1 - \cos \beta)], \quad (3.22)$$

with $\beta \triangleq \omega_{ro} D T_s$, as can be seen in Fig. 3-6. In order to evaluate V_y , suitable expressions for the initial conditions V_{C1} , V_{C2} , I_{r1} , I_{r2} (shown in Fig. 3-6) must be found. To this purpose, by exploiting the continuity property of the resonant voltage $v_c(t)$, it is possible to find the required expressions

$$\begin{cases} V_{C1} = \sin \alpha [V_{C2} \cot \alpha - Z_r I_{r2} + (V_s - n_e V_o) \tan \frac{\alpha}{2}] \\ V_{C2} = \sin \beta [V_{C1} \cot \beta - Z_{ro} I_{r1}] \end{cases}, \quad (3.23)$$

with $\alpha \triangleq \omega_r (1 - D) T_s$, as shown in Fig. 3-6. Then, by assuming an approximated triangular waveform for the magnetizing current $i_m(t)$, it is possible to express I_{r1} and I_{r2} as

$$I_{r2,1} \approx I_m \pm \frac{\Delta i_m}{2} = \frac{I_o}{n_e} \pm \frac{n_e V_o}{2 f_s L_{me}} (1 - D). \quad (3.24)$$

Substituting (3.24) and (3.23) into (3.22) yields

$$V_y = k_1 \left(\frac{V_g}{1 - D} - n_e k_2 V_o + k_3 \right), \quad (3.25)$$

where coefficients k_1 , k_2 and k_3 are

$$k_1 \triangleq \frac{f_s}{\omega_{ro}} \frac{\sin \alpha \sin \beta}{1 - \cos \alpha \cos \beta} \tan \frac{\alpha}{2}, \quad (3.26)$$

$$k_2 \triangleq 1 + Z_r \frac{1 - D}{2 f_s L_{me}} (1 - \gamma) \cot \frac{\alpha}{2}, \quad (3.27)$$

$$k_3 \triangleq Z_r \frac{I_o}{n_e} (1 + \gamma) \cot \frac{\alpha}{2}, \quad (3.28)$$

and

$$\gamma \triangleq \sqrt{\frac{1 + \lambda}{\lambda}} \cdot \cot \frac{\alpha}{2} \tan \frac{\beta}{2}. \quad (3.29)$$

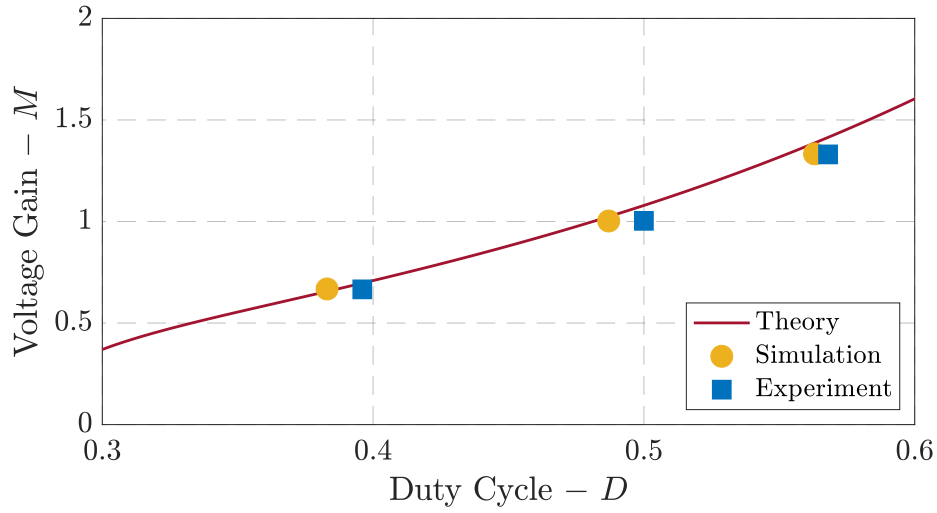


Figure 3-9: Voltage gain comparison between theoretical model, simulation, and experimental measurements when $V_o = 12$ V, $I_o = 600$ mA, and $f_s = 2$ MHz. Measured and simulated data points are taken for V_g equal to 9 V, 12 V, and 18 V.

Combining (3.25) with (3.21) yields the final expression of the voltage gain

$$M \triangleq \frac{V_o}{V_g} = \frac{k_1/[n_e(1-D)]}{(1-D)(1+\lambda) + k_1[k_2 + k_3/(n_e V_o)]}. \quad (3.30)$$

The above expression, which is the main result of this section, is extensively used in the design procedure described in section 3.3.3. The plot of M as a function of D predicted by (3.30) is shown in Fig. 3-9, together with simulated and measured data points, that correspond to the design later disclosed in this thesis. As can be seen, (3.30) fits reasonably well the resonant DCM behaviour of the converter across the 9 V-18 V input voltage range of interest because the voltage across the magnetizing inductance L_{me} , during subinterval $D_3 T_s$, is not much lower than the value $n_e V_o$ corresponding to the time interval in which output diode D_r is conducting.

3.3.3 Design Methodology for ZVS Resonant DCM Operation

The main specifications dictated by the considered application are reported in Tab. 3.3. The specified switching frequency, equal to 2 MHz, was selected to avoid disturbance in the AM band (540 kHz – 1.6 MHz) – since the low EMI noise is a critical requirement for automotive power supplies – and to reduce the size and cost of the converter’s passive

Table 3.3: Converter specifications

Parameter	Symbol	Value
Input voltage	V_g	9 V – 18 V
Nominal output voltage	V_o	12 V
Nominal output current	I_o	600 mA
Nominal output power	P_o	7.2 W
Switching frequency	f_s	2 MHz

components. The 100 V, 1.7 A EPC2106 eGaN[®] FET pair [48] hosted by the EPC9055 development board [49] is selected to implement Q_1 and Q_2 . Fig. 3-10 shows the top view of the development board, together with the two instruments used to drive the GaN switches:

1. a gate drive supply (12 V)
2. a waveform generator used to provide a 0-5 V square waveform with $f_s = 2$ MHz

This work requires to turn Q_1 and Q_2 ON with ZVS at $t = T_s$ and $t = DT_s$, respectively, to keep the switching losses under an acceptable level since the selected switching frequency is very high.

To guarantee ZVS, the net current

$$i_L(t) \triangleq i_g(t) + i_r(t) \quad (3.31)$$

injected into the switching node must have the correct polarity *and* value at each switching transition. As can be seen from Fig. 3-8, the ZVS turn-ON of Q_2 (at $t = DT_s$) is always guaranteed due to the highest positive value obtained either by $i_g(t)$ and $i_r(t)$, which brings the switching node voltage $v_{sw}(t)$ to the high-level in a few nanoseconds. On the other hand, the critical ZVS transition is the turn-ON of the low-side switch Q_1 at the end of the period ($t = T_s$), for which $i_L(t)$ must be sufficiently *negative*.

The proposed design procedure is the following. First, determine the amount of current required for the critical ZVS transition. A simple approach is to impose a design constraint on $i_L(t)$ – assumed constant and equal to $i_L(T_s)$ during the dead-time – in order to guarantee enough negative current for the complete ZVS transition of the switching node during the

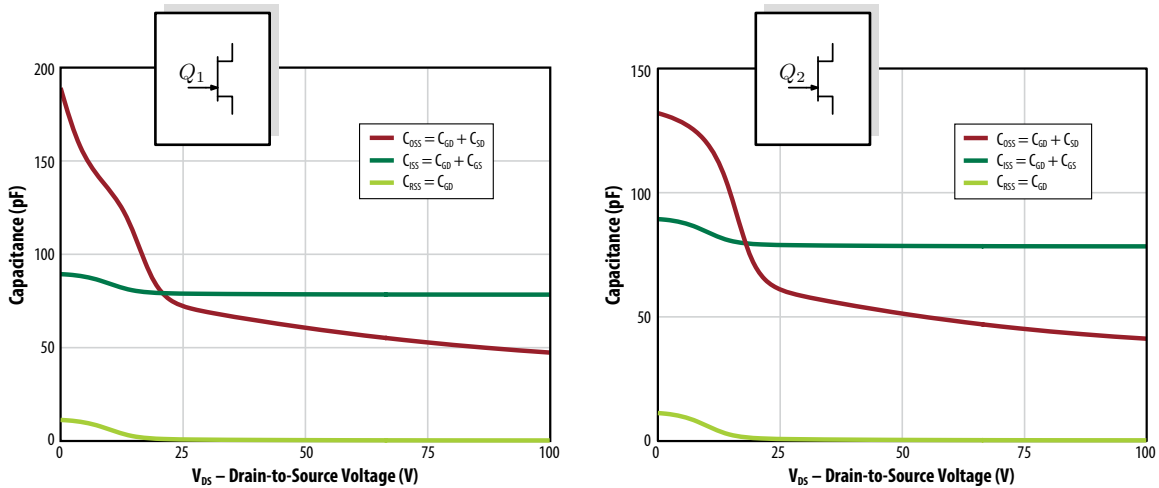
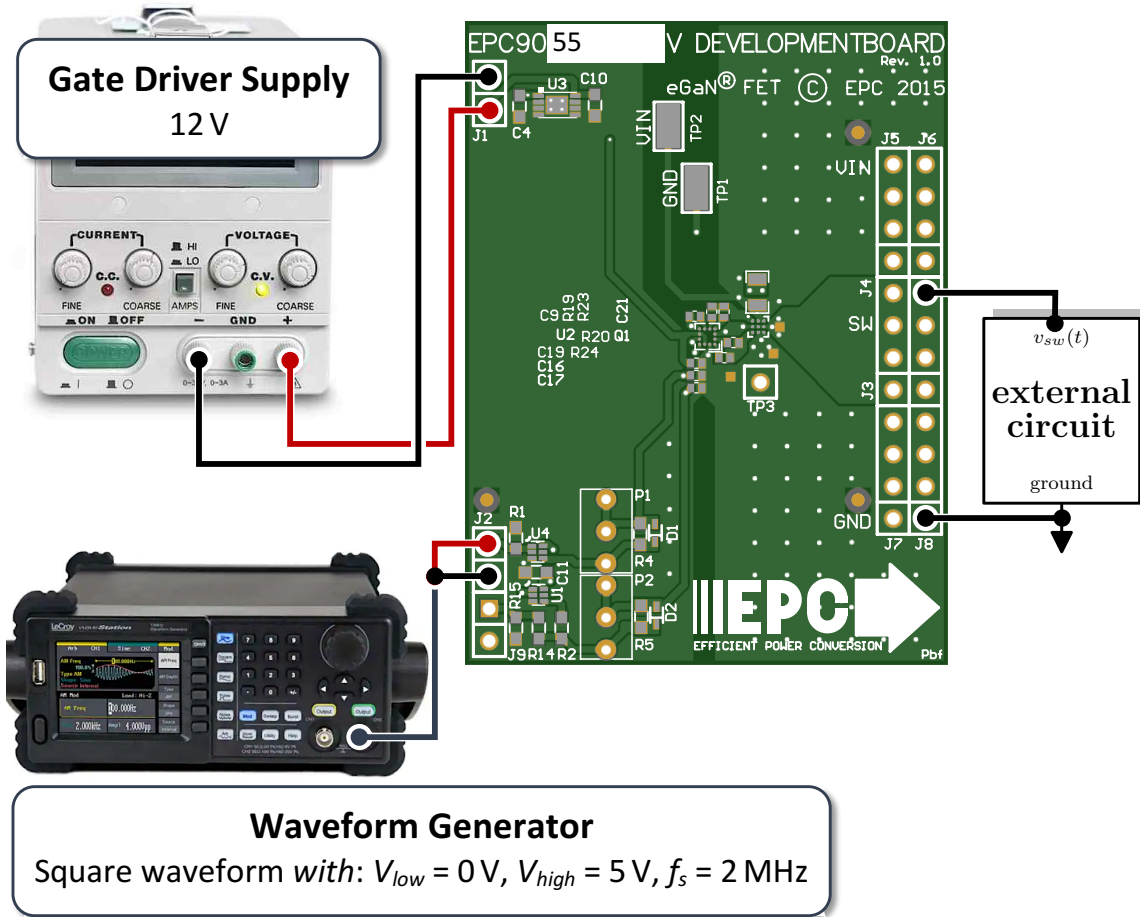


Figure 3-10: Setup used to drive the EPC2106 eGaN® FET pair hosted by the EPC9055 development board, and output capacitance C_{oss} (highlighted in red) vs. drain-to-source voltage V_{ds} for primary switch Q_1 and secondary switch Q_2 .

dead-time itself, *i.e.*,

$$i_L(T_s) < -\frac{1}{t_D} C_{eq,Q} V_s, \quad (3.32)$$

where $C_{eq,Q}$ is the charge-equivalent capacitance at the switching node [50], V_s the switching node voltage value at the switching instant, and t_D the dead-time. Assuming $t_D \approx 15$ ns, such current can be estimated from the total output capacitance profile $C_{oss}(v_{ds})$ of the two switches [48] reported in Fig. 3-10. Next, considering $\lambda = 6\%$ as a reasonable starting value for the transformer leakage-to-magnetizing inductance ratio of a high-frequency interleaved planar transformer, the possible design pairs (L_g, L_{me}) compatible with the ZVS constraint are considered, and reported in Fig. 3-11. In the plot, which assumes an initial choice $C_c = 48$ nF for the resonant capacitor and refers to the nominal operating point $V_g = V_o = 12$ V, $I_o = 0.6$ A, the ZVS and the hard-switching regions are illustrated. Furthermore, the overlaid contour lines represent the estimated *rms* value $I_{L_{rms}}$ of $i_L(t)$, a quantity directly related to the total conduction losses of the eGaN[®] pair. Such estimation involves the approximation of $i_r(t)$ with $i_m(t)$, with the consequent almost triangular wave shapes, yielding

$$I_{L_{rms}} \approx (I_g + I_m) \sqrt{1 + \frac{1}{12} \left(\frac{\Delta i_L}{I_g + I_m} \right)^2}, \quad (3.33)$$

where $\Delta i_L = \Delta i_g + \Delta i_m$. The peak-to-peak current ripple Δi_m and the average value of $i_m(t)$ are calculated using (3.24), while I_g and Δi_g are obtained as

$$I_g = \frac{1}{\eta} \frac{V_o I_o}{V_g}, \quad \Delta i_g = \frac{V_g D}{L_g} T_s. \quad (3.34)$$

To calculate the average value of the input current an efficiency $\eta = 87\%$ is assumed for the considered operating point.

The foregoing equations clearly require the duty cycle value D to be recalculated for each design pair (L_g, L_{me}) , in order to maintain $V_o = 12$ V throughout the design space. This is accomplished by using the voltage gain model (3.30) developed in section 3.3.2.

Fig. 3-11 serves as a design tool to explore the trade-off in the selection of L_g and L_{me} . On one hand, the design point (L_g, L_{me}) should be selected in proximity of the ZVS/Hard switching boundary in order to limit the value of $I_{L_{rms}}$. Within this basic constraint, the

Parameter	Symbol	Value
Input voltage	V_g	12 V
Output voltage	V_o	12 V
Output current	I_o	600 mA
Switching frequency	f_s	2 MHz
Efficiency profile	η	87 %
Inductance ratio	λ	6 %
Resonant capacitor	C_c	48 nF

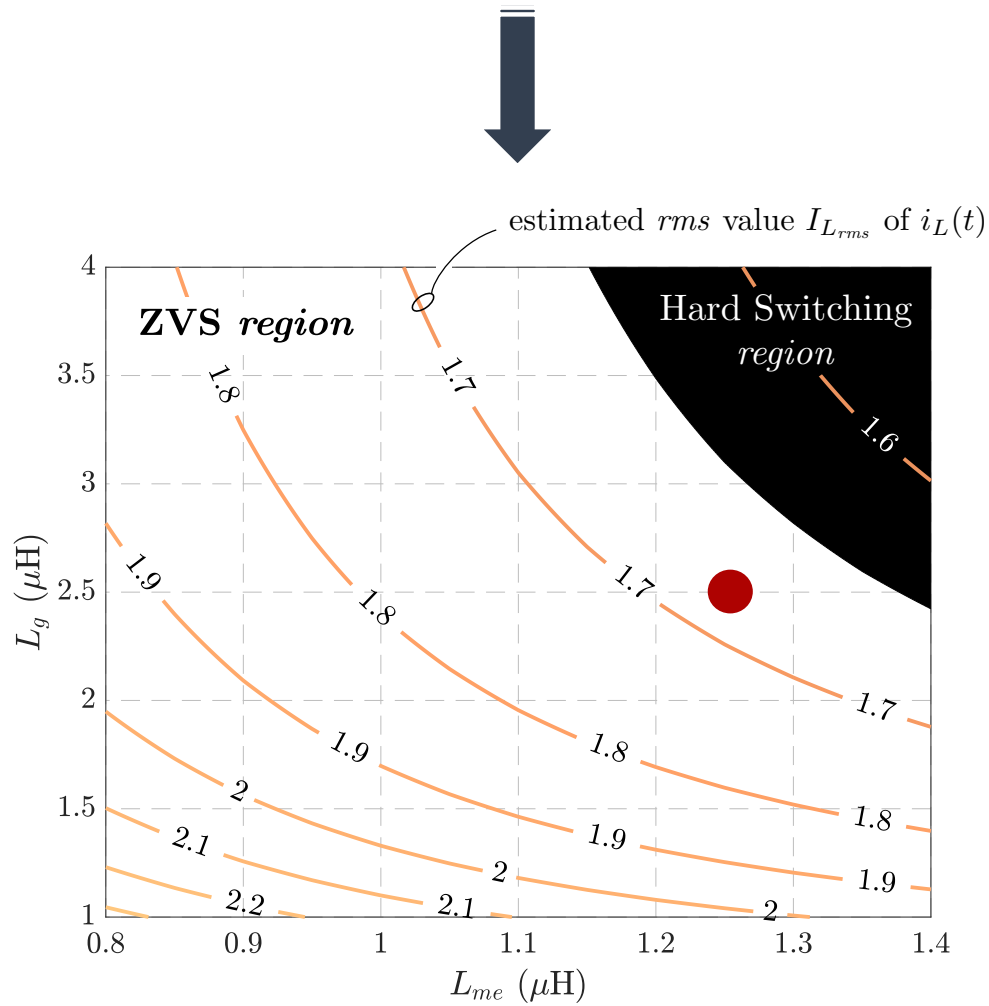


Figure 3-11: (L_g, L_{me}) design space relative to the nominal operating point, reporting the ZVS and hard-switching regions, as well as the contour plots of $I_{L_{rms}}$. The assumptions followed to plot the graph are reported in the table and the final design choice adopted in this work is highlighted with a red disk.

ACISC topology offers a degree of freedom in the relative choice of L_g and L_{me} , which translates into different amount of peak-to-peak current ripple on $i_g(t)$ and on $i_m(t)$. The specific design choice here adopted, $L_g \approx 2.5 \mu\text{H}$ and $L_{me} \approx 1.25 \mu\text{H}$, is highlighted in the plot with a red disk.

Note that choosing a small value for λ – where the latter is a variable in which only L_{me} is controlled by the designer – comes from the initial target of realizing a transformer with a reduced leakage inductance value (interleaving the turns of the windings) to get a higher value for C_c while keeping the ZVS resonant DCM operation in nominal conditions. Increasing the value of the resonant capacitor leads to reducing both its voltage ripple (which is significant in the considered operation mode) and the voltage stress across the output diode D_r . However, this choice does not represent the unique design methodology for such an application. For example, the designer can be interested in minimizing the transformer's inter-winding capacitance C_w – which is a critical parasitic capacitance of the converter in the common mode (CM) noise perspective – leading to a higher value of L_{pe} (and, consequently, of λ) since the interleaving between windings no longer represents the correct solution [51, 52]. In any case, one of the main advantages of the resonant operation is to add an additional degree of freedom, since the considered operating mode can always be ensured by adjusting the value of the resonant capacitor C_c .

Magnetics design

To obtain the required magnetizing inductance and to reduce the overall footprint, a planar transformer based on two ER9.5 half-cores (material 3F4) is built, with a suitable air gap between the central legs in order to obtain the desired magnetizing inductance value. Effective core parameters are reported in Tab. 3.4. As a first attempt, the selected number of

Table 3.4: Effective core parameters for planar ER9.5 series

Parameter	Symbol	Value	Unit
Effective volume	V_e	120	mm^3
Effective length	l_e	14.2	mm
Effective area	A_e	8.47	mm^2
Mass of core half	m	0.35	g

turns is determined starting from an analytical estimate of the core losses P_{core} . Once the peak flux density value $\hat{B}$ is estimated using the following expression

$$\hat{B} = \frac{1}{n_1} \frac{n_e V_o}{2 f_s A_e} (1 - D), \quad (3.35)$$

it is possible to calculate P_{core} at a given V_g by consulting the P_v vs. $\hat{B}$ plot reported in the 3F4's datasheet. The first choice of $n_1 = n_2 = 6$ turns with 380 μm central air gap is determined as an adequate compromise between core and winding losses, the latter being estimated based on the calculated DC windings resistance.

Fig. 3-13 illustrates the planar transformer structure. Each 6-turn winding consists of three series-connected layers of two turns each. Each two-turn layer is hosted on a 440 μm -thick PCB module, with one turn on the top and the other turn on the bottom. Primary and secondary layers are interleaved in order to minimize the leakage inductance, and separated by 60 μm -thick insulator sheets. The footprint area of the resulting structure is approximately 245 mm^2 . As anticipated, in this study the traditional 4-parameters transformer model, accounting for primary-side and secondary-side leakage inductances L_p and L_s , primary-side magnetizing inductance L_m and turns ratio n , is simplified into the *reduced transformer model* as shown in Fig. 3-12 (Step III). Extraction of reduced-model parameters L_{me} , L_{pe} , and n_e is accomplished by first experimentally characterizing the planar transformer by measuring the following three inductances

- L_{11}^{SO} : Open-circuit primary-side inductance
- L_{22}^{PO} : Open-circuit secondary-side inductance
- L_{11}^{SS} : Short-circuit primary-side inductance

The Agilent 4294A Precision Impedance Analyzer is used to measure the above inductances at $f_s = 2$ MHz. The reduced-order parameters are then simply calculated as

$$L_{pe} = L_{11}^{SS}, \quad L_{me} = L_{11}^{SO} - L_{11}^{SS}, \quad n_e = \sqrt{\frac{L_{11}^{SO} - L_{11}^{SS}}{L_{22}^{PO}}}. \quad (3.36)$$

The obtained values are reported in Tab. 3.5, from which $\lambda \approx 6.3\%$ is obtained, in good agreement with the design assumption made to obtain the plot shown in Fig. 3-11. As far

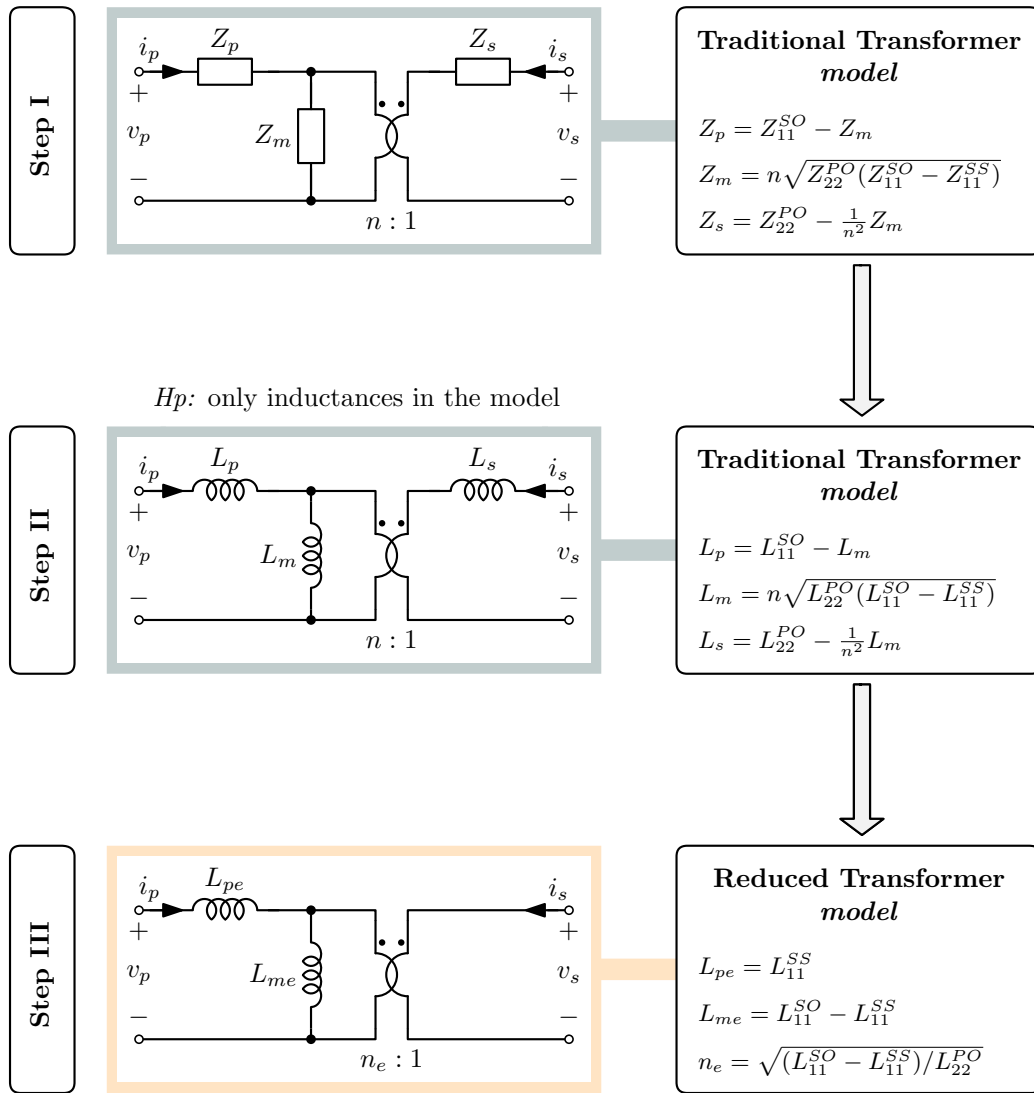


Figure 3-12: Traditional and reduced transformer model. “Step I” shows the traditional 4-parameters transformer model; “Step II” shows the same model accounting for inductances only; “Step III” reveals the reduced 3-parameters transformer model used throughout this thesis.

Table 3.5: Converter parameters characterized at $f_s = 2$ MHz

Parameter	Symbol	Value
Input inductance	L_g	2.2 μ H
Equivalent primary leakage inductance	L_{pe}	75.2 nH
Equivalent magnetizing inductance	L_{me}	1.2 μ H
Equivalent transformer turns ratio	n_e	0.97
Resonant capacitor	C_c	47.8 nF
Clamp capacitor	C_s	1 μ F
Output capacitor	C_o	10 μ F

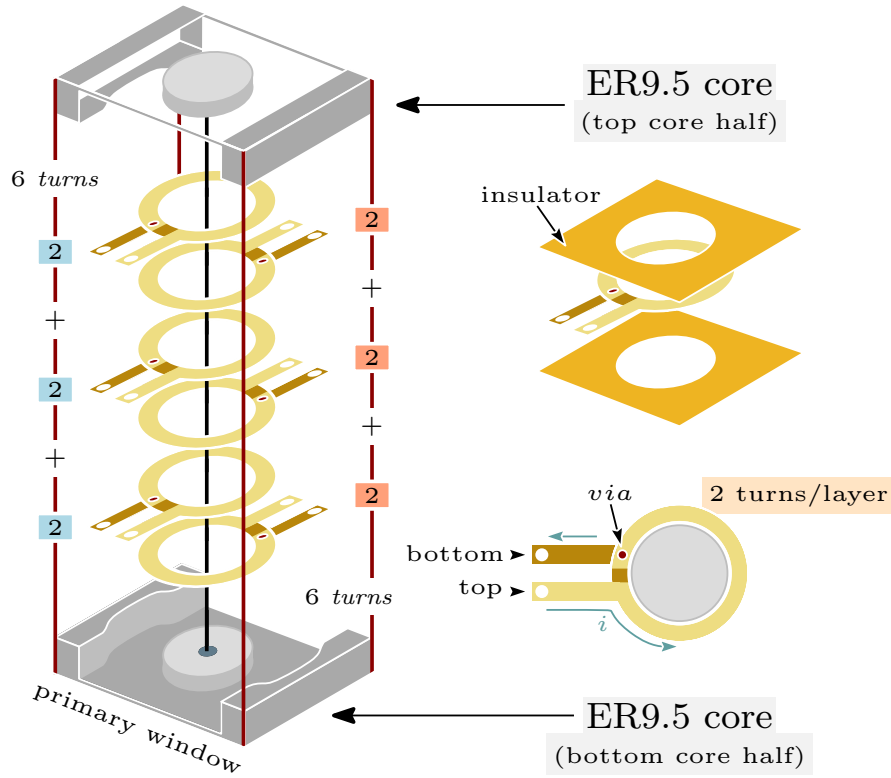


Figure 3-13: Exploded view of the planar transformer based on two ER9.5 half-cores and three two-turns layers per winding ($n_1 = n_2 = 6$).

as the required $2.5 \mu\text{H}$ input inductance is concerned, a 6-turn planar inductor employing ER9.5 cores (same 3F4 material) is realized, measuring the value, at $f_s = 2 \text{ MHz}$, reported in Tab. 3.5. The ac winding resistance value $R_{w,ac}$ of L_g is equal to $283 \text{ m}\Omega$.

3.4 Experimental Results

To validate the proposed design methodology, a 2 MHz 12 V, 600 mA GaN-based converter is created. Fig. 3-14 shows the picture of the experimental prototype with a detail of the 6 : 6 ER9.5 planar transformer. The prototype is built around the EPC9055 development board, which features the selected 100 V, 1.7 A EPC2106 half-bridge pair. Fig. 3-10 shows how the development board is supplied and driven. The latter, which already hosts a $1 \mu\text{F}$ clamp capacitor C_s , is connected at the switching node with a custom-designed PCB, where the input inductor, resonant capacitor, planar transformer, and output rectifier stage are

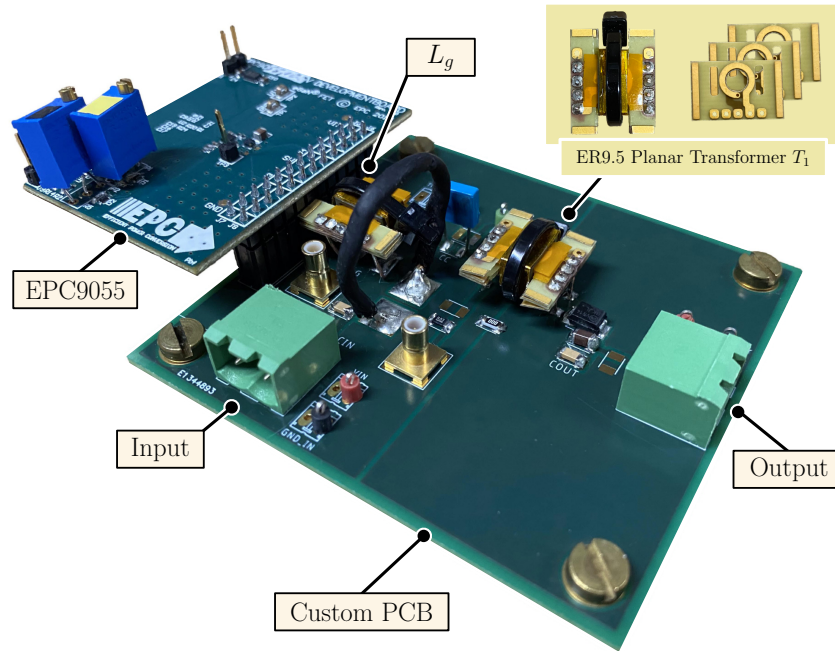
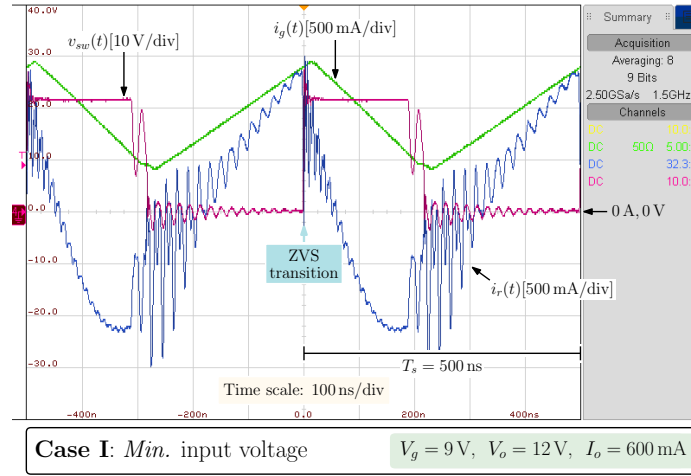


Figure 3-14: Picture of the experimental prototype.

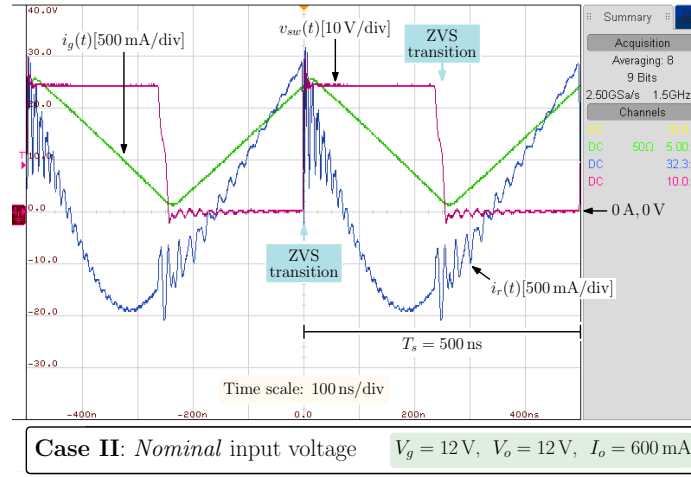
located. The experimentally characterized values of the passive components are reported in Tab. 3.5. In addition, the details of the planar transformer are reported in Tab. 3.6. A 40 V, 2 A Schottky rectifier is selected for D_r . Because of the large forward voltage drop of the body diode in GaN devices, both driving dead times for the eGaN[®] pair have been adjusted to reduce the body diode conduction time as much as possible throughout the entire input voltage operating range. Such operation was performed manually, once and for all, in nominal condition by adjusting two on-board trimmers (blue boxes in Fig. 3-14). Fig. 3-15 reports the converter experimental waveforms for $V_o = 12$ V and $I_o = 600$ mA, when the input voltage V_g assumes the minimum, nominal and maximum values. Despite the high frequency noise, the resonant current $i_r(t)$ exhibits the behaviour already shown in Fig. 3-6, especially for input voltages greater than 9 V where the converter starts operating in DCM. Fig. 3-15 shows that the critical ZVS condition – corresponding to the falling

Table 3.6: Planar transformer parameters characterized at $f_s = 2$ MHz

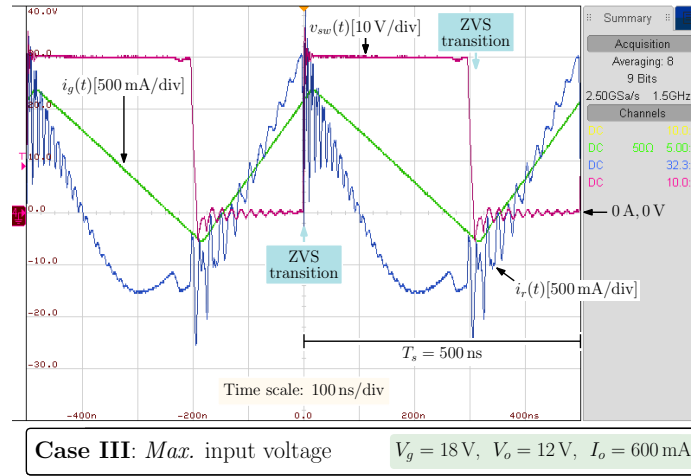
	Turns	Core material	Gap (μm)	L_{me} (μH)	L_{pe} (nH)	$R_{w1,ac}$ (m Ω)	$R_{w2,ac}$ (m Ω)
ER 9.5 Planar Transformer	6 : 6	3F4	380	1.22	75.2	248	235



(a)



(b)



(c)

Figure 3-15: Experimental screenshot of the input current $i_g(t)$ (500 mA/div), the resonant current $i_r(t)$ (500 mA/div), and the switching node voltage $v_{sw}(t)$ (10 V/div) at $V_o = 12\text{ V}$ and $I_o = 600\text{ mA}$, when the input voltage V_g is equal to (a) 9 V, (b) 12 V, and (c) 18 V. Time scale: 100 ns/div.

3.4. Experimental Results

edge of $v_{sw}(t)$ – is always satisfied, except for the minimum input voltage, for which the current $i_L(T_s)$ is not sufficiently *negative* to allow $v_{sw}(t)$ to complete the entire transition before the end of the dead-time. The fixed dead-time for the falling edge of $v_{sw}(t)$ is almost equal to 15 ns and is close to the value chosen to plot Fig. 3-11.

Finally, as it will be explained in the next sections, it is necessary to find the value of the ac winding resistances ($R_{w1,ac}$ and $R_{w2,ac}$ in Tab. 3.6) to estimate the winding losses of the planar transformer. To do so, the latter is characterized following the procedure reported below (also shown in Fig. 3-16):

- **Measure #1:** $R_{w1,ac} = \text{Re}\{Z_{11}^{SO}\}\big|_{f=2\text{ MHz}} = 248\text{ m}\Omega$, with Z_{11}^{SO} = inductance seen at the transformer's primary window by keeping the secondary open (SO),
- **Measure #2:** $R_{w2,ac} = \text{Re}\{Z_{22}^{PO}\}\big|_{f=2\text{ MHz}} = 235\text{ m}\Omega$, with Z_{22}^{PO} = inductance seen at the transformer's secondary window by keeping the primary open (PO).

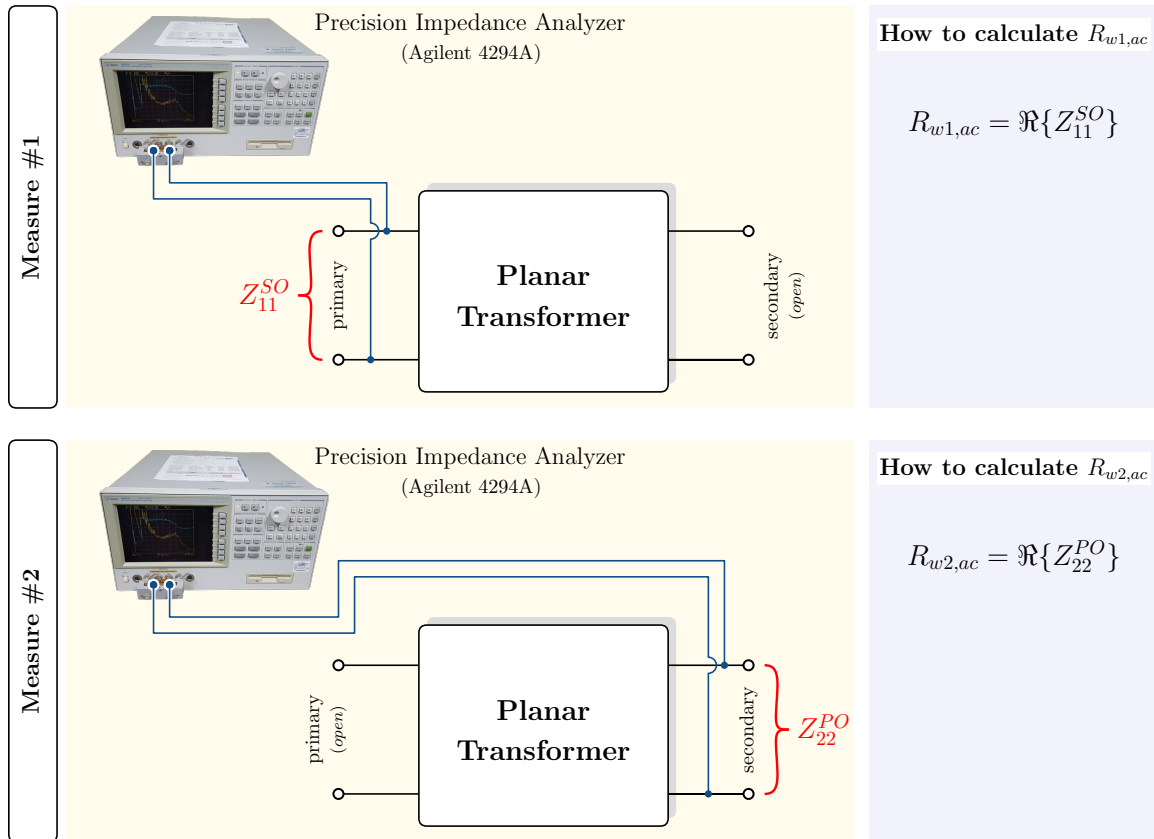
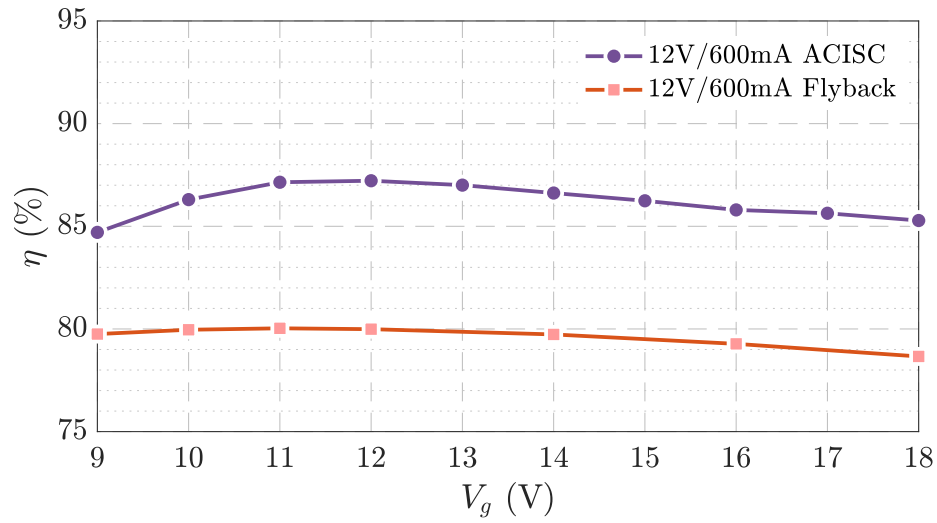


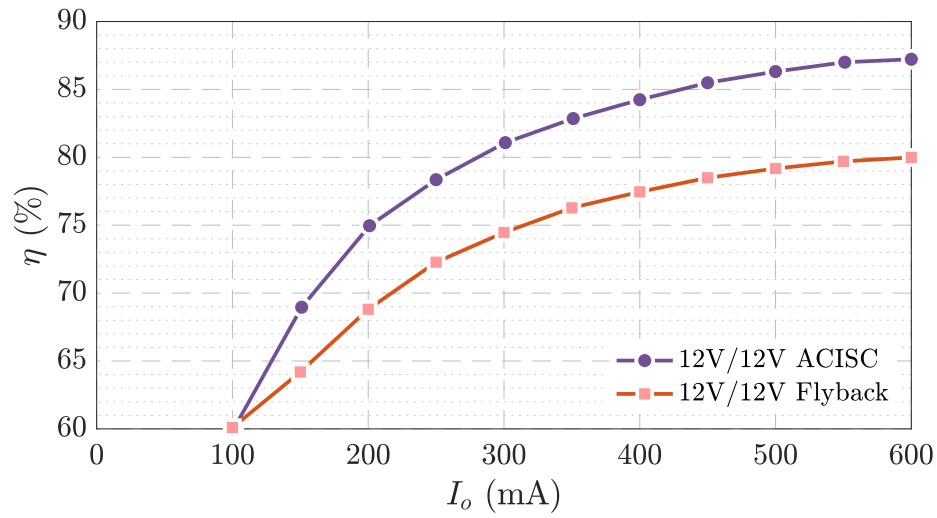
Figure 3-16: How to find the ac winding resistance values, $R_{w1,ac}$ and $R_{w2,ac}$, by characterizing the planar transformer with the Precision Impedance Analyzer.

3.4.1 Efficiency Profile

Fig. 3-17 compares the efficiency of the designed 2 MHz active-clamped isolated SEPIC converter (ACISC) with that of a 400 kHz commercial flyback converter operating in continuous conduction mode (CCM) intended for the same application, and having the same input/output voltage and rated current specifications. The efficiency profile refers to the power stage only and does not include gate driver losses. The comparison, carried out as a function of both input voltage V_g and output current I_o , reveals a peak efficiency of the



(a)



(b)

Figure 3-17: Efficiency comparison between the designed 2 MHz ACISC converter and a 400 kHz commercial flyback converter having the same input/output voltage and current rating specifications, as a function of (a) the input voltage V_g and (b) the output current I_o .

designed 2 MHz ACISC of 87.22% at $V_o = 12\text{ V}$ and $I_o = 600\text{ mA}$, approximately 7.2% better than the commercial flyback converter despite the fivefold increase in the switching frequency.

↔ The goal of the next two chapters will be to first identify what are the main loss sources of the ACISC and estimate their relative contributions with Ch. 4, and then, with Ch. 5, reducing the largest loss contribution to significantly increase the efficiency profile shown in Fig. 3-17 while minimizing the in-circuit noise.

Chapter 4

Power Loss Breakdown Analysis

4.1 Identification of the Main Loss Sources and Estimation of their Relative Contributions

As can be seen in Fig. 3-17, at the nominal operating point ($V_g = V_o = 12\text{ V}$, $I_o = 600\text{ mA}$) $\eta = 87.22\%$ and the total measured power losses are

$$P_{loss} = V_o I_o \left(\frac{1}{\eta} - 1 \right) \approx 1055\text{ mW}.$$

A power loss breakdown analysis is described *here*, for nominal conditions, with the purpose of identifying the main loss sources and estimate their relative contributions. All the analytical estimates are carried out considering a temperature equal to 100°C , except for the GaN's conduction losses where their real temperature is derived using a Laserliner ThermoCamera (thermal measurement will be discussed later in Ch. 7). The main power losses are estimated using (3.30) to determine the right value of duty cycle D to set $V_o = 12\text{ V}$ as required by the considered automotive architecture. The six main loss sources are listed below and then investigated individually:

1. Transformer Losses: Core and Winding Losses
2. Conduction Losses of the Switches

3. Capacitor's Losses
4. Input inductor Losses
5. Output Diode Losses
6. Body Diode Condition Losses of the Switches

1. Transformer Losses: Core and Winding Losses

This category, also refers to inductors and mutual inductors, namely each component that includes a magnetic core. The transformer losses can be divided in *i*) core losses and *ii*) winding losses, depending on where they take place. A description of the origin of these losses together with their different modelling is discussed hereafter.

i) Transformer Core Losses

The cores used to build transformers and inductors are usually made of soft magnetic materials. The core loss of these components is crucial for the converter's efficiency and power density [53–55]. When there is an alternating external field, the magnetic domain¹ wall moves and consumes energy, which gives rise to the core loss.

Different degrees of accuracy can be achieved in the core loss estimation depending on the available information and the desired computation effort. Basically, the core losses P_{core} are given by the sum of two sources of losses – eddy current loss and hysteresis loss – and can be split in three main terms:

$$P_{core} = P_{cl} + P_{ex} + P_{hyst}. \quad (4.1)$$

The eddy current loss is traditionally divided into two parts: one is called classic eddy current loss P_{cl} and the other one is called excess loss P_{ex} . The classical losses P_{cl} describe the loss calculated from the solution of the Maxwell's equation in a homogeneous material without any domain structure, then geometrically defined. Excess loss P_{ex} accounts for the difference between the measured loss and the sum of calculated P_{hyst} and P_{cl} . This

¹A magnetic domain is a region which has uniform magnetization.

loss is explained as eddy current loss due to localized magnetization. Because the material is composed of domains that are heterogeneous, the magnetization happens only near the domain walls when the external field changes. This means that the actual eddy current loss is higher than the calculated eddy current assumed under uniform magnetization. Finally, the last loss contribution, P_{hyst} , is associated to Barkhausen jumps. As can be observed in Fig. 4-1, the magnetic flux density B is not a single-value function of the external applied magnetic field H as consequence of a *phase lag* between the two variables. This phenomenon is called hysteresis and it is indicative of out-of-equilibrium process where an irreversible energy transformation takes place. In magnetic materials, the losses are derived by local rearrangement of the magnetic domains presented in the core. Applying an external field, the minimum energy domain configuration is destroyed and the domains move toward a new stable configuration. This jump between two consecutive stable configurations are the so-called “Barkhausen jumps”. The local flux changes around the Barkhausen jumps and generates eddy currents in the closer volume, causing the core losses. When the frequency increases, the area enclosed by the static hysteresis loop shown in Fig. 4-1 becomes bigger due to the eddy current loss. From the point of view of modelling the core

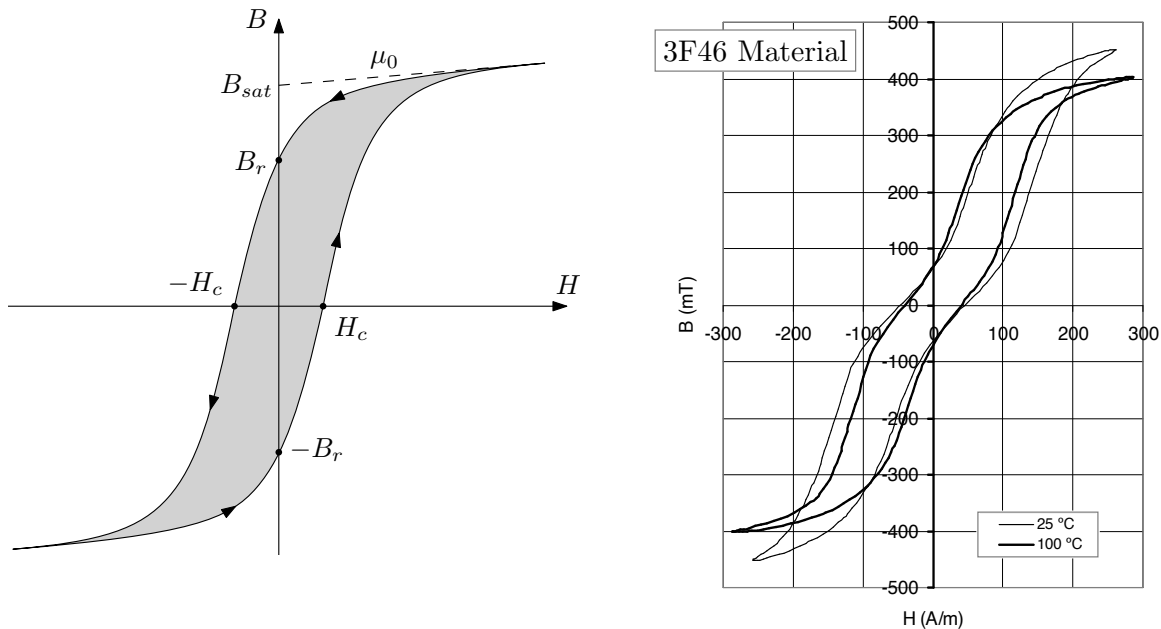


Figure 4-1: Hysteresis in magnetic components: hysteresis loop in the (H, B) -plane referred to a general case (on the left), and to the 3F46 power material measured at 10 kHz (on the right).

losses, the most reasonable and useful model is provided by the Steinmetz equation (and its further improvements). It is characterized by a few material parameters, *i.e.* k , α and β , that can be extracted by the core material datasheet. The outcome of this equation is a power loss density P_v (*e.g.*, expressed in kW/m³), thus $P_{core} = P_v V_e$, where V_e is the volume of the selected core.

The Steinmetz equation is valid only for sinusoidal flux density, and the power loss density P_v is given by

$$P_v = k f^\alpha \hat{B}^\beta \quad (4.2)$$

where f is the excitation frequency, $\hat{B}$ is the peak magnetic flux density (amplitude of the sinusoidal flux density [56]), and k , α , and β , are the Steinmetz coefficients.

Note that, in typical magnetic materials, the Steinmetz coefficients are valid for a limited range of frequencies and flux densities, and they all vary with temperature and type of selected material.

In this work, the core loss value P_{core} is estimated following these six steps:

1. Consider the magnetizing current waveform $i_m(t)$ when the ACISC is operated in resonant DCM operation, as reported in Fig. 4-2.
2. Derive its average value I_m and its peak-to-peak current value Δi_m , as done in (3.24):
 $I_m = I_o/n_e$, and $\Delta i_m = n_e V_o(1 - D)/(f_s L_{me})$. Looking at Fig. 4-2, $I_{pk} = I_m + \Delta i_m/2$.
3. Re-write the expression of the magnetizing current $i_m(t)$ considering the *Faraday's* law. The latter states that the flux $\Phi(t)$ inside the core of a given transformer induces a voltage $v_{turn}(t)$ in each turn of the winding, given by $v_{turn}(t) = d\Phi/dt$. Since the same flux $\Phi(t)$ passes through each turn of the winding, the total winding voltage is $v(t) = n_1 v_{turn}(t) = n_1 d\Phi/dt = n_1 A_e dB/dt$ (where n_1 is the number of turns at the primary window, and A_e is the area of the selected core). The expression of the magnetizing current can be rewritten in this way:

$$i_m(t) = \frac{1}{L_{me}} \cdot \int v(t) dt = \frac{1}{L_{me}} \cdot n_1 A_e B \quad (4.3)$$

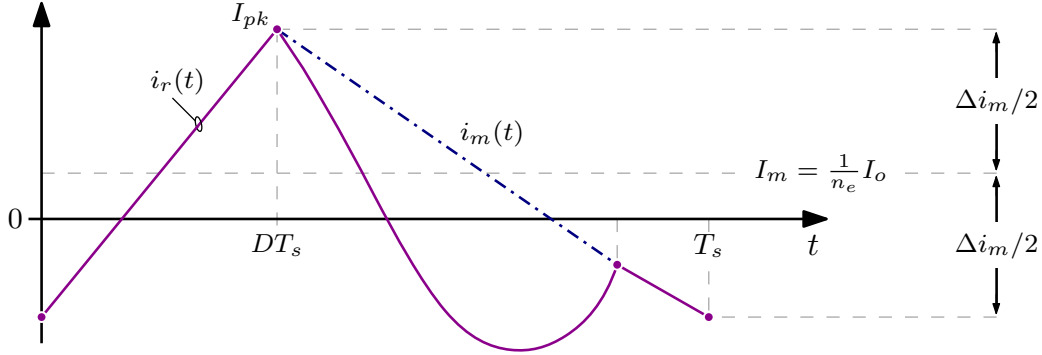


Figure 4-2: Resonant current $i_r(t)$ and magnetizing current $i_m(t)$ when the converter is operated in resonant DCM operation.

4. Find the expression of $\hat{B}$. To get $\hat{B}$, substitute $i_m(t)$ with $\Delta i_m/2$ since the P_v vs. $\hat{B}$ plot in the power material's datasheet is provided under sinusoidal excitation without dc bias

$$\frac{\Delta i_m}{2} = \frac{n_e V_o}{2 f_s L_{me}} (1 - D) = \frac{1}{L_{me}} n_1 A_e \hat{B} \mapsto \boxed{\hat{B} = \frac{1}{n_1} \frac{n_e V_o}{2 f_s A_e} (1 - D)}. \quad (4.4)$$

5. Use the P_v vs. $\hat{B}$ plot taken from the power material's datasheet considering the curve referred to the desired switching frequency. Fig. 4-3 shows the extracted curves for several high frequency power materials at $f_s = 2$ MHz and $T = 100^\circ\text{C}$.
6. Estimate the transformer core losses P_{core} . Once the core is selected, calculate $\hat{B}$ using (4.4). Changing the input voltage V_g from 9 V up to 18 V, the duty-cycle D varies according to (3.30), as reported in Fig. 3-9. Once the value of $\hat{B}$ is known, P_{core} is found multiplying the value obtained for P_v by the volume V_e of the selected core (e.g., ER9.5 planar cores have an effective volume $V_e = 120 \text{ mm}^3$).

ii) Transformer Winding Losses

The losses that occur in the winding of a magnetic core device derive from the current density distribution inside the conductor [57, 58]. At high frequency, the current density in a conductor becomes larger near the surface and decreases towards the centre, namely *skin* effect. Furthermore, when currents are flowing through more close conductors, the

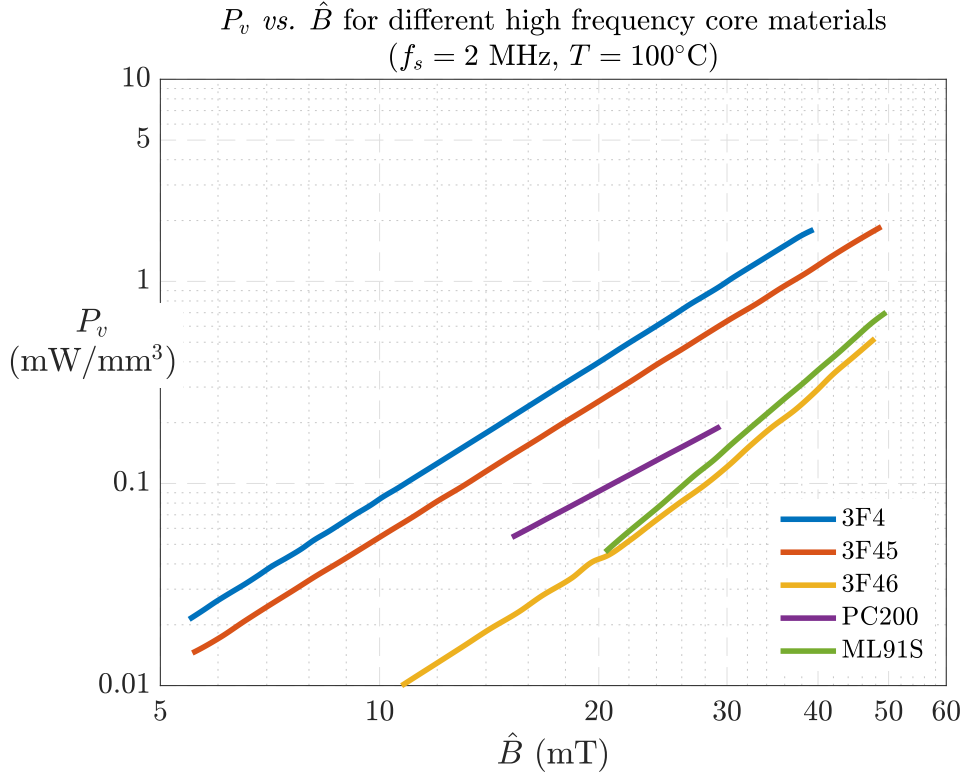


Figure 4-3: Power loss density P_v as a function of the peak flux density $\hat{B}$ for different high frequency power materials, when $f_s = 2$ MHz and $T = 100^\circ\text{C}$.

magnetic field produced by each one affected the others. The resulting current distribution is crowded around the maximum magnetic field region, namely *proximity* effect. Winding losses P_{wind} in the transformer windings are calculated after characterizing the transformer to find the primary and secondary ac winding resistances, $R_{w1,ac}$ and $R_{w2,ac}$, at $f_s = 2$ MHz. Notice that, given the high switching frequency and the relatively small output current I_o , the dc resistance contribution to the power losses of the secondary winding has been neglected. The root mean square value (*rms*) of the current flowing through the two windings (I_{rms} and I_{3rms}) is derived from simulation. The analytical expressions used to estimate the winding losses are reported below

$$P_{wind_1} = R_{w1,ac} I_{rms}^2, \quad \text{and} \quad P_{wind_2} = R_{w2,ac} (I_{3rms}^2 - I_o^2). \quad (4.5)$$

The value of the ac winding resistances are shown in Tab. 3.6. *Note* that the dc resistance contribution to the power losses of the primary winding is not considered since $I_r = 0$.

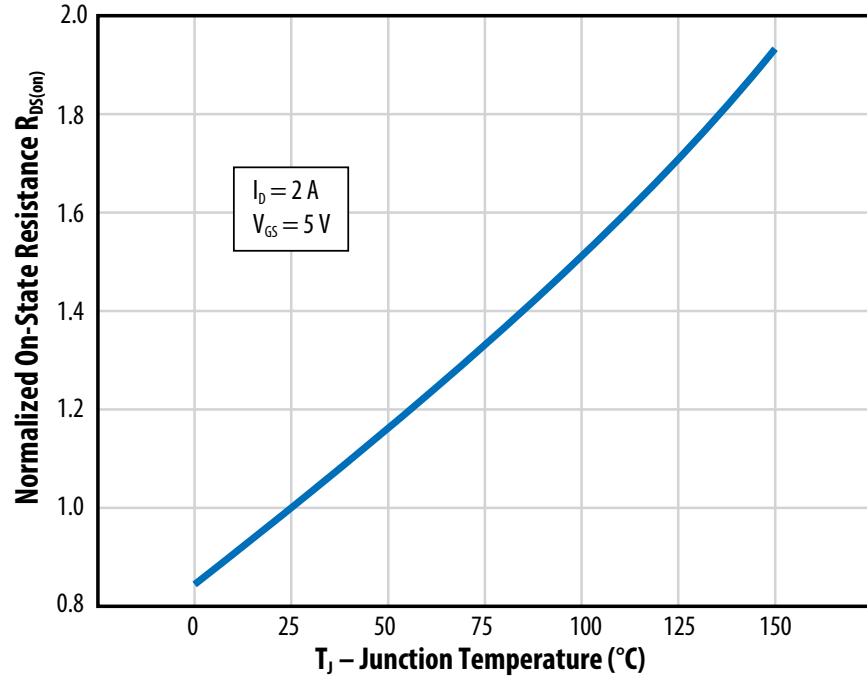


Figure 4-4: EPC2106 normalized ON-state resistance vs. junction temperature, when the drain current $I_D = 2$ A and the gate-source voltage $V_{GS} = 5$ V.

2. Conduction Losses of the Switches

Conduction losses P_{cond} of the switches are determined from the simulated switch currents and from datasheet parameters, such as the ON-state resistance $R_{ds(on)}$ of Q_1 and Q_2 . As shown in Fig. 4-4, which reports the EPC2106 normalized ON-state resistance vs. junction temperature plot, $R_{ds(on)}(50^\circ\text{C}) \approx 1.18 \cdot R_{ds(on)}(25^\circ\text{C}) = 65 \text{ m}\Omega$. As will be shown later, the temperature T_j of the EPC2106 eGaN case is approximately equal to 50°C under nominal conditions. The analytical expressions used to estimate the switch conduction losses are reported below

$$P_{cond}^{Q_1} = R_{ds(on)} I_{Q1rms}^2, \quad \text{and} \quad P_{cond}^{Q_2} = R_{ds(on)} I_{Q2rms}^2. \quad (4.6)$$

3. Capacitors' Losses

Losses associated with the resonant capacitor C_c and clamp capacitor C_s are determined both from the simulated currents flowing through them and their equivalent series resistance value R_{series} at 2 MHz. The analytical expressions used to estimate the capacitors' losses are

reported below

$$P_{C_c} = R_{series}^{C_c} I_{rms}^2, \quad \text{and} \quad P_{C_s} = R_{series}^{C_s} I_{Q2rms}^2. \quad (4.7)$$

where $R_{series}^{C_c} \sim 40 \text{ m}\Omega$ and $R_{series}^{C_s} \sim \text{a few m}\Omega$ for the selected capacitors. The $1 \mu\text{F}$ 100 V clamp capacitor C_s is already hosted by the EPC9055 development board (TDK, CGA4J3X7S2A105K125AE).

Note that P_{C_s} is negligible due to its very small series resistance value at high frequency.

4. Input Inductor Losses

The calculation of the input inductor losses P_{L_g} simply follows what has been said for the transformer ($P_{L_g} = \text{core losses} + \text{winding losses}$). Once the peak flux density value $\hat{B}$ is estimated through the following expression

$$\hat{B} = \frac{1}{n_1} \frac{DV_g}{2f_s A_e}, \quad (4.8)$$

it is possible to calculate the core losses of L_g at a given V_g by consulting the P_v vs. $\hat{B}$ plot reported in the power material's datasheet. Again, it is possible to estimate the inductor winding losses after characterizing the latter to find the ac winding resistance $R_{w,ac}$ at 2 MHz . The photo of the 6-turn planar inductor employing ER9.5 cores is shown in Fig. 3-14, and its inductance value at 2 MHz is reported in Tab. 3.5 ($R_{w,ac} = 283 \text{ m}\Omega$). The analytical expression used to estimate the winding losses is reported below

$$P_{wind} = R_{w,ac} (I_{grms}^2 - I_g^2) \quad (4.9)$$

where $I_{grms} = I_g \sqrt{1 + \Delta i_g^2 / (12 I_g^2)}$, while (3.34) is used to calculate the value of I_g and Δi_g (assuming $\eta = 1$).

5. Output Diode Losses

A 40 V , 2 A schottky power rectifier (MBRS2040LT3G) is selected for D_r since it is ideally suited for low voltage high switching power supplies. The output diode conduction losses P_{diode} can be estimated once the forward characteristics (I_F and V_F) are modeled. Fig. 4-5

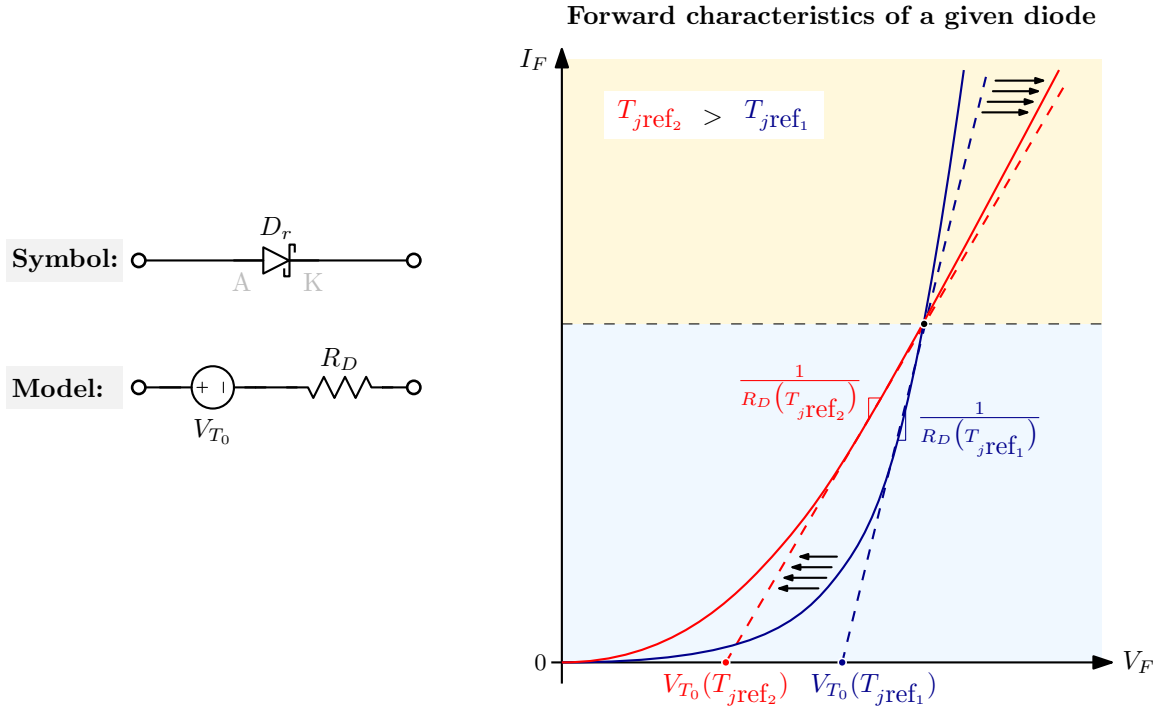


Figure 4-5: Symbol, model and forward characteristics of the chosen schottky rectifier diode.

shows symbol, model, and forward characteristics (at two different temperatures) of the chosen schottky rectifier diode, highlighting its main parameters. As can be seen from the plot, the relation between instantaneous forward current I_F and forward voltage V_F can be modeled by a straight line defined by a threshold voltage V_{T_0} and a dynamic resistance R_D . As depicted in Fig. 4-5, the two parameters V_{T_0} and R_D are calculated for two forward current levels (I_{F_1} , I_{F_2}) for a given junction temperature T_j .

Thus, it is possible to write

$$V_F(I_{F_1}, T_j) = V_{T_0}(T_j) + R_D(T_j) \cdot I_{F_1}, \quad (4.10)$$

$$V_F(I_{F_2}, T_j) = V_{T_0}(T_j) + R_D(T_j) \cdot I_{F_2}. \quad (4.11)$$

Using (4.10) and (4.11) it is possible to obtain the expression of $V_{T_0}(T_j)$ and $R_D(T_j)$

$$V_{T_0}(T_j) = \frac{V_F(I_{F_1}, T_j) \cdot I_{F_2} - V_F(I_{F_2}, T_j) \cdot I_{F_1}}{I_{F_2} - I_{F_1}}, \quad (4.12)$$

$$R_D(T_j) = \frac{V_F(I_{F2}, T_j) - V_F(I_{F1}, T_j)}{I_{F2} - I_{F1}}. \quad (4.13)$$

The output diode conduction losses P_{diode} represent the average dissipated power in the diode during the forward conduction phase,

$$P_{diode}(T_j) = \frac{1}{T_s} \int_0^{T_s} V_F(I_F, T_j) \cdot I_F(t) dt, \quad (4.14)$$

which can also be written as follows

$$P_{diode}(T_j) = \underbrace{V_{T_0}(T_j)}_{-q/m} I_F^{avg} + \underbrace{R_D(T_j)}_{m^{-1}} I_F^{rms2}, \quad (4.15)$$

where $I_F^{avg} = I_o$ is the forward average current and $I_F^{rms} = I_{3rms}$ is the forward root mean square value of the current flowing through the output diode D_r . As shown in Fig. 4-5, threshold voltage $V_{T_0}(T_j)$ and dynamic resistance $R_D(T_j)$ are extrapolated from the fitting

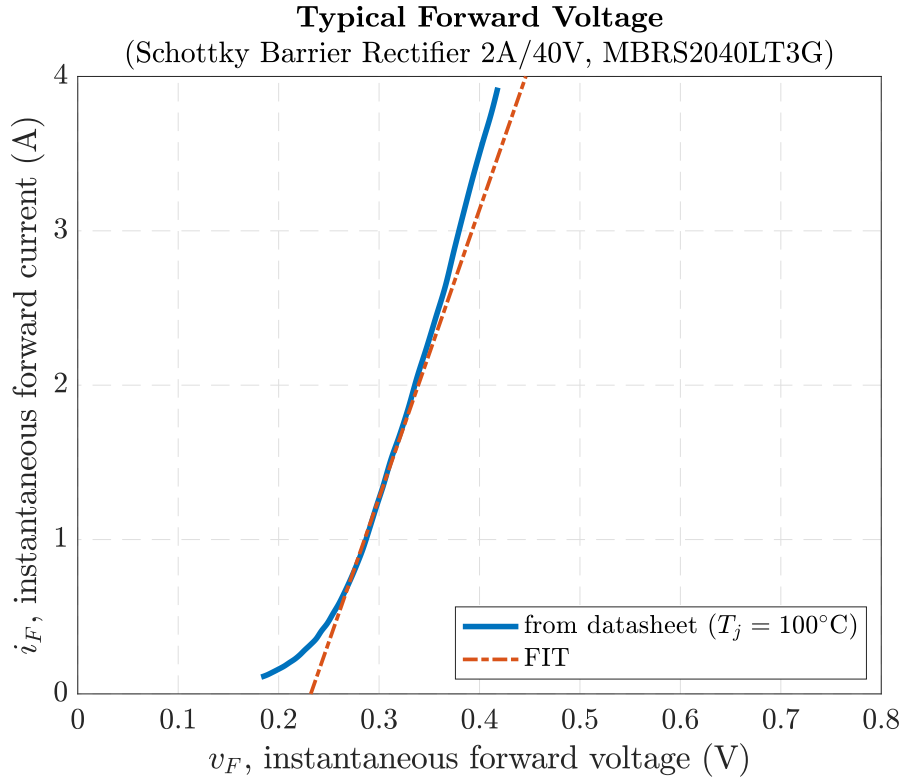


Figure 4-6: Experimental I_F - V_F characteristics of the chosen schottky rectifier diode together with its fitting curve, considering a junction temperature $T_j = 100^\circ\text{C}$.

curve $I_F = mV_F + q$ of the I_F - V_F forward characteristics of the chosen schottky rectifier. In Fig. 4-6 the procedure described above is applied to the selected 40 V, 2 A schottky power rectifier diode, obtaining the following results

$$V_{T_0}(T_j) = -\frac{q}{m} = 232 \text{ mV}, \quad \text{and} \quad R_D(T_j) = m^{-1} = 53.5 \text{ m}\Omega \quad (4.16)$$

6. Body Diode Conduction Losses of the Switches

As for the body diode conduction losses of the switches, these are *here* neglected in nominal conditions in light of the preliminary dead-time optimization described above. In general, an approximate expression to estimate such losses is reported below

$$P_{body} = |I_{L_{pk}}| \cdot V_{sd} \cdot \frac{t_{dead-time}}{T_s} \quad (4.17)$$

where $I_{L_{pk}} = I_{g_{pk}} + I_{r_{pk}}$ is the upper or lower peak value of the current ($i_g(t) + i_r(t)$) injected into the switching node, during $t_{dead-time}$, to turn Q_2 and Q_1 ON, respectively. V_{sd} is the typical source-drain forward voltage value reported on the datasheet of the selected switches (*e.g.*, $V_{sd} = 2.1 \text{ V}$ for the EPC2106). Finally, T_s is the switching period.

Note that, using (4.17), body diode losses are overestimated since the peak value of the two currents is considered constant during the entire duration of the dead-time period $t_{dead-time}$. The first dead-time, where Q_2 is turned-ON, is the most important one since the two currents are achieving the highest positive peak value, and $|I_{L_{pk}}|$ shows the maximum value. For this reason, although both dead-times are optimized in nominal conditions, optimizing the first dead-time results in significantly higher efficiency than optimizing the other one.

Total Converter's Losses

The analytical expressions used to estimate the aforementioned sources of losses are summarized in Tab. 4.1, while the power loss breakdown in nominal conditions is shown in Fig. 4-7. The largest loss contribution is associated with the transformer, and in particular with primary winding losses to be attributed to *skin* and *proximity* effects in the MHz range. At the same time, notice that the power loss breakdown illustrated in Fig. 4-7 points to an

4.1. Identification of the Main Loss Sources and Estimation of their Relative Contributions

Table 4.1: Expressions used to estimate the main power losses of the ACISC

Main Power losses	analytical expression used	from datasheet	from simulation	from theory	from PIA*
P_{L_g}	$R_{w,ac}(I_{grms}^2 - I_g^2) + P_v V_e$	P_v, V_e	—	$\hat{B}, I_g, I_{grms}$	$R_{w,ac}$
P_{C_c}	$R_{series} I_{rms}^2$	—	I_{rms}	—	R_{series}
P_{cond,Q_1}	$R_{ds(on)} I_{Q1rms}^2$	$R_{ds(on)}$	I_{Q1rms}	—	—
P_{cond,Q_2}	$R_{ds(on)} I_{Q2rms}^2$	$R_{ds(on)}$	I_{Q2rms}	—	—
P_{core}	$P_v V_e$	P_v, V_e	—	$\hat{B}$	—
P_{wind_1}	$R_{w1,ac}(I_{rms}^2 - I_r^2)$	—	I_{rms}	—	$R_{w1,ac}$
P_{wind_2}	$R_{w2,ac}(I_{3rms}^2 - I_o^2)$	—	I_{3rms}	—	$R_{w2,ac}$
P_{diode}	$V_{T0} I_o + R_D I_{3rms}^2$	V_{T0}, R_D	I_{3rms}	—	—

* PIA is the Agilent 4294A Precision Impedance Analyzer used to measure the reported parameters at $f_s = 2$ MHz. Note that P_{core} , P_{wind_1} , and P_{wind_2} are the three transformer loss contributions.

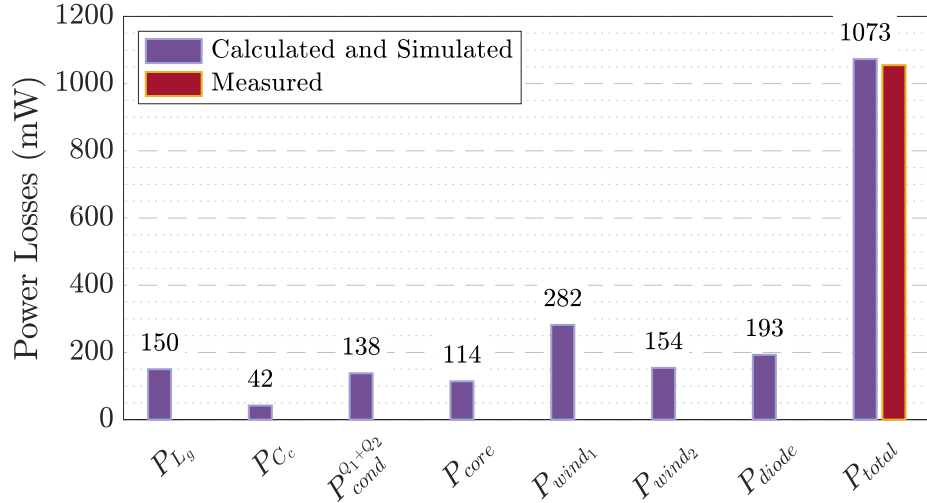


Figure 4-7: Power loss breakdown of the designed 2 MHz ACISC converter for $V_g = V_o = 12$ V and $I_o = 600$ mA (nominal conditions).

overall balanced design with the various loss contributions exhibiting comparable orders of magnitude.

As it will be shown in the next chapter, to increase the efficiency profile of the converter it is necessary to focus on reducing the winding losses of the planar transformer and, in particular, to minimize their ac winding resistance values.

4.2 Some Considerations to Improve the Proposed Power Losses Estimation

Although Sec. 4.1 provides a rigorous procedure to estimate the main converter's power losses and Fig. 4-7 shows a good agreement between the total calculated losses and experimental data, the analytical estimation of the losses can be further improved considering the following aspects:

Consideration 1: Most of the magnetic material's datasheets provide the P_v vs. $\hat{B}$ plot such that the losses are measured under sinusoidal excitation without dc bias at a given temperature. Obviously, this information is of limited help in power electronics applications because it gives a roughly and inaccurate estimate of core losses P_{core} . For this reason, a more precise methodology should be considered which accounts for all the aspects reported below:

- AC excitation frequency and amplitude . As demonstrated in the P_v vs. $\hat{B}$ plots shown in Fig. 4-8 (two high frequency power materials are considered), the ac excitation frequency and amplitude directly affect the core loss density P_v . To consider these two aspects, the designer can make use of the plots shown in Fig. 4-8 (if the

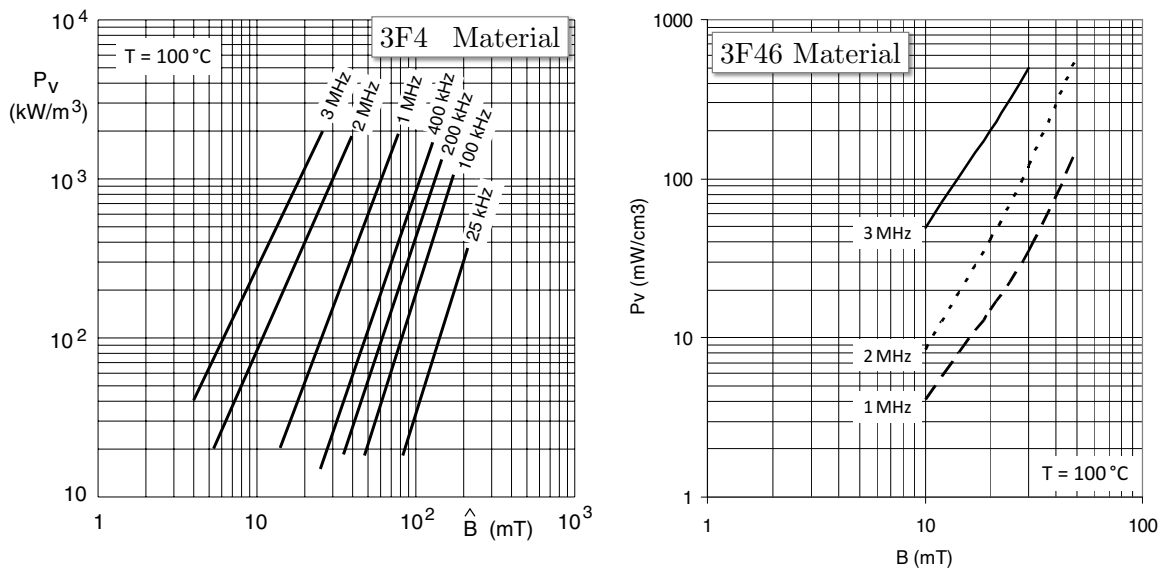


Figure 4-8: Power loss density P_v as a function of the peak flux density $\hat{B}$ for different high frequency power materials: 3F4 on the left and 3F46 on the right (from Ferroxcube).

desired frequency is considered). On the other hand, even if the estimation process of P_{core} is extremely fast once f_s and $\hat{B}$ are known, the drawback is that an inaccurate estimation of the losses is usually made following this method. This is because pre-determined constrains are assumed to plot such curves: sinusoidal excitation without dc bias at $T = 100^\circ\text{C}$. However, in the planar transformer hosted by the ACISC topology, the magnetizing current $i_m(t)$ can be approximated as a triangular waveform with dc bias ($I_m = I_o/n_e$) while the temperature of the core is significantly lower than 100°C .

- b. **Type of considered waveform** . Instead of the sinusoidal waveform considered in Fig. 4-8, rectangular voltages are the waveforms that are the most commonly seen in power electronics applications. For example, [59, 60] have reported that the core losses under rectangular or square excitation are different from the sinusoidal one, and the value of the duty cycle plays an important role in the losses.
- c. **Presence or absence of dc bias** . The dc bias affects the loss even if the dc flux does not produce loss directly [61–65]. Core losses P_{core} increase with the increasing bias, because more energy is required by further magnetizing the dipoles under the pre-magnetization condition. On the other hand, the impact of the dc bias changes by selecting different core materials: core losses under certain bias can be lower than non-biased core losses. The physics behind the impact of dc bias to core losses should be investigated in detail in order to account for it in a precise analytical estimation of P_{core} .
- d. **Temperature** . Even if this is not a general rule, ferrites usually display lowest losses between 60°C to 100°C (a parabola is often used to model the temperature dependence of core losses [66]). However, the temperature dependence of a given power material changes with the excitation level. Fig. 4-9 shows the measured power loss density P_v as a function of the temperature T , for 3F4 and 3F46 high frequency power materials. As can be observed, the minimum loss value takes place at different temperatures considering different AC flux excursions and frequencies. In addition, the shape of the parabola can be different when the test frequency is changed.

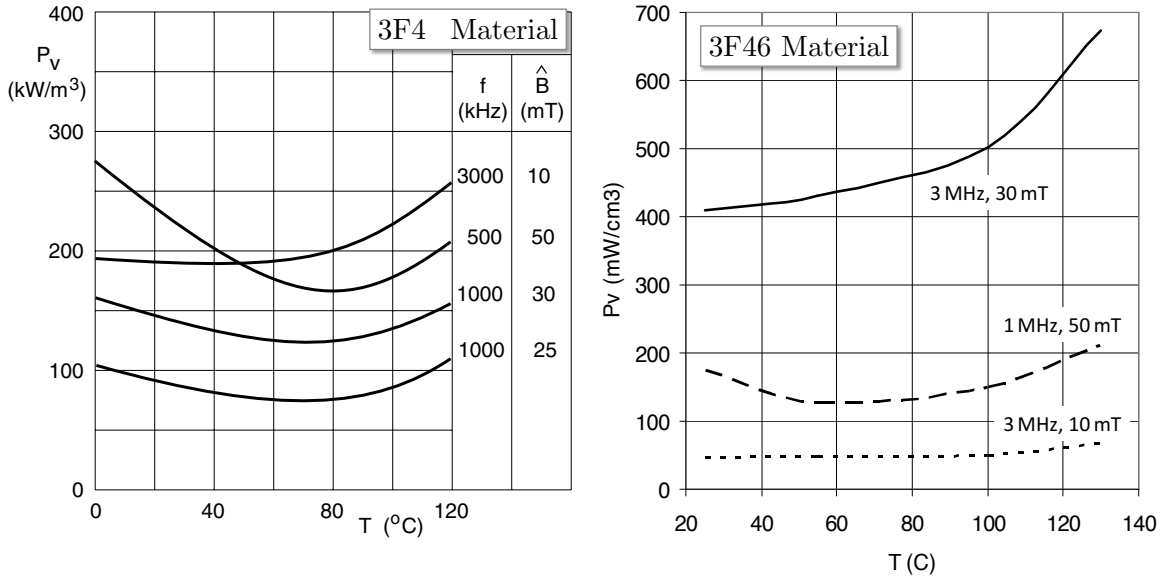


Figure 4-9: Power loss density P_v as a function of the temperature T for different high frequency power materials: 3F4 on the left and 3F46 on the right (from Ferroxcube).

In conclusion, due to the non-linearity of core losses P_{core} and their dependence on so many factors, it is very complicated to analytically estimate their contribution precisely. For this reason, the best approach to finding P_{core} under various waveforms and dc bias values is to test it, as shown in detail in [67]. However, sometimes it is not practical due to limited time and capability, thus core loss model is a way to give engineers a quick estimation. Such kinds of models usually only need limited extra measurement effort other than the datasheet, so they are preferred by engineers. These models are listed below in order of accuracy:

- Steinmetz Equation (SE) $\mapsto$ (4.2)
- Modified Steinmetz Equation (MSE)
- General Steinmetz Equation (GSE) [56]
- improved General Steinmetz Equation (iGSE) [68]
- improved² General Steinmetz Equation (i²GSE) [69, 70]

Consideration 2: Even if the dc resistance of the transformer's secondary winding $R_{w2,dc}$ is low ($\sim$ tens of $\text{m}\Omega$), the secondary winding losses $P_{wind,2}$ are greater than the ones

reported in Fig. 4-7. For this reason, a more precise expression which accounts for the dc winding resistance could be used: $P_{wind_2} = R_{w2,ac}(I_{3_{rms}}^2 - I_o^2) + R_{w2,dc}I_o^2$.

Consideration 3: As done for the GaN switches (where a ThermoCamera was used), knowing the exact core temperature of the magnetics, along with that of the output diode D_r , would allow the designer to estimate their power losses more accurately since their temperature is lower than 100 °C (as it will be proved in Sec. 7 by showing the images of thermal measurements).

Consideration 4: There are methods, not discussed in this thesis, which allow the designer to accurately estimate the ac winding resistance $R_{w,ac}$ and dc winding resistance $R_{w,dc}$ of the magnetics – *e.g.*, through 3-D Finite Element Analysis (FEA) tools – without characterizing the inductor or the transformer with the impedance analyzer. Doing so would make it possible to propose a completely theoretical estimate of converter power losses without needing to test any components. In addition, these tools allow the designer to find the best configuration for the magnetic component to optimize the desired parameters without testing several prototypes.

Consideration 5: Gate driver losses P_{gate} are not considered in the power losses estimation described above. This is because the EPC9055 development board uses a dedicated power supply for gate drivers which is different from the converter's input voltage V_g . Despite this, P_{gate} is very low since GaN devices are used instead of Si components (which have a very high total gate charge Q_g). Using the EPC2106 GaN devices, $Q_g = 700$ pC (typical value), thus $P_{gate} \simeq 2Q_g V_{gs} f_s = 14.6$ mW (with $V_{gs} = 5$ V, and $f_s = 2$ MHz).

Chapter 5

Magnetics Analysis and Optimization Techniques

5.1 Introduction

In the 48 V/12 V battery-connected architecture investigated in Ch. 2, a variety of low-power electronic loads – *e.g.*, sensors, micro-controllers, and communication transceivers – are supplied by the 48 V main battery through an intermediate 12 V bus. In case of failure of the latter, the system is sustained by a 12 V backup battery as shown in Fig. 3-1. As reported in Ch. 3, the isolated dc-dc converter interfacing the backup battery with the low-power 12 V intermediate bus must operate efficiently over the wide 9 V-18 V automotive input voltage range while keeping magnetic size and overall footprint at a minimum, as required by the automotive market. An active-clamped isolated SEPIC converter (ACISC) [31, 32, 34, 38] is considered in Ch. 3 as a strong candidate for the battery-connected application and planar magnetics are used to either operate at high frequencies and achieve lower profiles than conventional wire-wound components, aiding the miniaturization of the converter. In this chapter, an improved version of the 2 MHz GaN-based ACISC shown in Ch. 3 is provided, focusing on a step-by-step planar magnetics optimization – in terms of ac winding resistance and inter-winding capacitance – to improve the converter’s efficiency profile and reduce the in-circuit noise since the latter can lead to instability problems [51, 71–76].

This chapter is organized as follows. Sec. 5.2 shows the influence of the ac and dc winding resistance in high-frequency planar magnetics based on the characterization of several ER planar inductors. The study is carried out considering a different number of turns, air gap values, thickness/width of planar turns, and changing the position of the windings within the two half-cores. Sec. 5.3 focuses on the design and implementation of different planar transformers and inductors, illustrating a step-by-step optimization procedure for the magnetics hosted by the designed 2 MHz ACISC shown in Ch. 3. Finally, the last section reports the experimental measurements taken on the 12 V, 600 mA GaN-based prototype proposed in Ch. 3 where three different designs are investigated. In this section, both the new efficiency profiles of the converter and an analytical estimate of the main power losses are provided, along with the estimation and minimization of the planar transformer inter-winding capacitance.

5.2 Influence of the AC and DC Winding Resistance in High-Frequency Planar Magnetics

Since the ACISC prototype is running at $f_s = 2$ MHz and hosts planar magnetics, it is crucial to understand the effects which give rise to its power losses in order to minimize them. As reported in [51], eddy current effects – including *skin* and *proximity* effects – dramatically increase winding losses when planar magnetics are operated in the MHz range since they cause the current density to be non-uniform in the cross-section of the conductor leading to high winding resistance at high switching frequencies. Moreover, once a planar magnetic is designed with a certain air gap value, as done in Ch. 3, an excessive power loss caused by the *fringing* field must be considered together with *skin* and *proximity* effect losses. This section aims at showing how the ac and dc winding resistance of ER planar inductors are affected by the number of turns, the air gap, the thickness/width of the turns, and the position of the windings within the two half-cores. To investigate these aspects, six planar PCBs – which will be inserted within ER9.5 and ER14.5 planar cores – are designed and used. Tab. 5.1 lists the specifications of the samples and Fig. 5-1 shows their

Table 5.1: Specifications of the six planar PCB samples

Sample ID	#1	#2	#3	#4	#5	#6
PCB <i>series</i>	ER9.5	ER9.5	ER9.5	ER9.5	ER9.5	ER14.5
No. of total turns	1	2	3	4	4	4
No. of turns/layer	1	1	1	1	2	2
Turns width (mm)	1.25	1.25	1.25	1.25	0.30	1.00
PCB thickness (μm)	640	640	640	640	430	430
Layer thickness (μm)	70	70	70	70	115	115
Insulator thickness (μm)	100	100	100	100	200	200
Turns configuration *	1 // 1 // 1 // 1	1 // 1 + 1 // 1	1 + 1 // 1 + 1	1 + 1 + 1 + 1	2 + 2	2 + 2
PCB used in Fig. 5-4 for:	$n_1 = 5$	$n_1 = 2, 6$	$n_1 = 3$	$n_1 = 4, 5, 6$	X	X

* Turns configuration is referred to a given sample structure from the top layer to the bottom one. Symbol “+” means that a *series* connection between two layers is given. On the other hand, “//” provides a *parallel* connection. Note that “//” takes precedence over “+”.

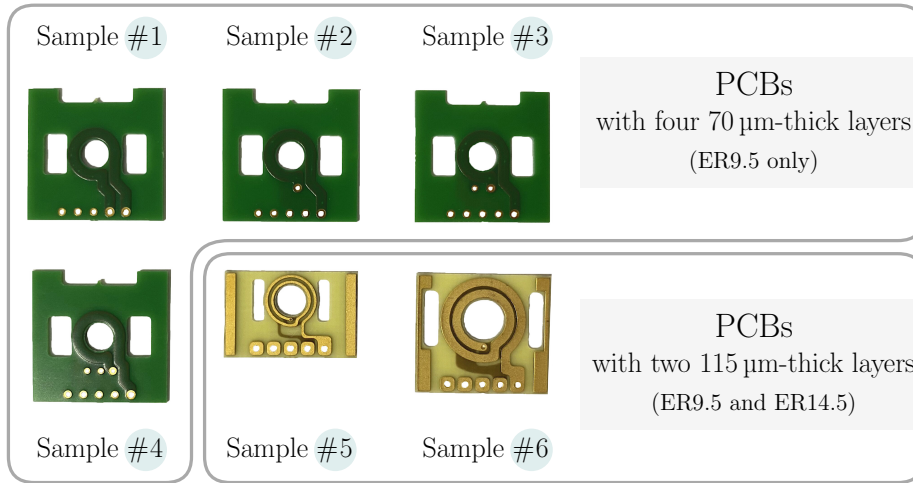

Figure 5-1: Photo of the planar PCB samples reported in Tab. 5.1.

photo. As reported in the table, the ER9.5 640 μm -thick samples #1, #2, #3, and #4 host four 70 μm -thick layers with one turn each. As shown in the penultimate row of Tab. 5.1, depending on the turns configuration the aforementioned samples provide 1, 2, 3, or 4 total turns (see the third row of Tab. 5.1). On the other hand, samples #5 and #6 – which consist of a 2-layer PCB with a total thickness of 430 μm – provide 4 total turns (half of them on top connected in series with the other ones on the bottom) with a higher layer thickness (115 μm) and different turns width depending on the considered PCB series (0.30 mm for ER9.5 and 1 mm for ER14.5). The ER planar inductors, realized with the samples reported in Tab. 5.1, make use of the 3F46 high-frequency power material [77]. The latter – which

can be used for planar magnetics running at 1-3 MHz, is one of the most efficient power materials currently available on the market. This result is proved in Ch. 4 with Fig. 4-3, where the 3F46 material is compared (at 2 MHz and 100 °C) with several high-frequency power materials, *i.e.* 3F4, 3F45, ML91S, and PC200. Fig. 5-2 shows how the value of both dc and ac winding resistance – the latter characterized at 2 MHz – changes by selecting different central air gap values (88 μm and 176 μm) and considering 4-turn ER9.5 planar inductors which make use of either sample #4 or #5 (the two samples are placed close to the top half-core separated by a 50 μm -thick insulator sheet). As expected, the value of the inductance is increased by decreasing the air gap and the dc resistance is not affected by this change since the number of turns doesn't change. On the other hand, the dc resistance doubles for sample #5 as the width of the 4 turns is drastically reduced compared to sample #4 where just one turn (taking all the available space) is hosted by each layer. Regarding the ac winding resistance, sample #4 is slightly closer to the central air gap (due to a greater PCB thickness) and, as it will be highlighted later, the closer the PCB sample gets to the

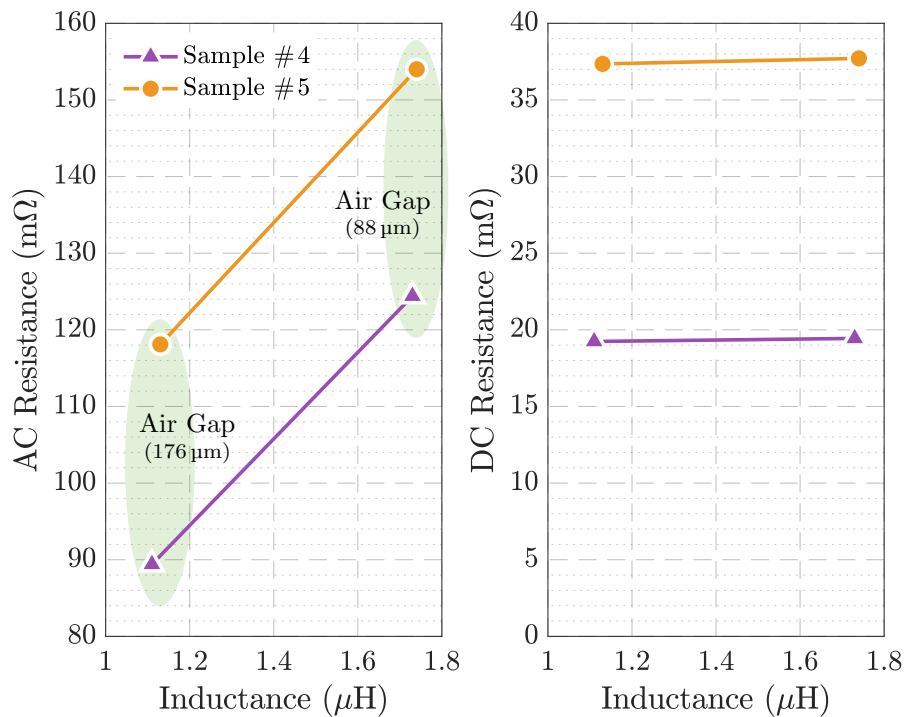


Figure 5-2: AC and DC winding resistance vs. inductance for two ER9.5 planar inductors having different air gap values between central legs, and $n_1 = 4$ turns. Specifications of samples #4 and #5 are reported in Tab. 5.1.

air gap, the more ac winding resistance increases. Nevertheless, its ac resistance value $R_{w,ac}$ is lower than sample #5 mainly due to a reduced turn thickness. Fig. 5-2 also shows that, for both samples, the ac winding resistance increases as the air gap value decreases since the flux inside the magnetic material is getting higher. The use of 2-D or 3-D Finite Element Analysis (FEA) tools can help the designer to find the best trade-off between layer thickness, turns width, ac and dc winding resistance for the considered application. Fig. 5-3 – which makes use of sample #6 within two ER14.5 planar cores having a total central air gap value equal to $310\ \mu\text{m}$ – shows how the ac resistance value is affected by the different positions of the sample within the two half-cores (0 mm on the x-axis means that the top view of sample #6 is attached to the top half-core). The ac resistance value referred to each disk is taken at 2 MHz by moving the top view of sample #6 away from the top half-core by multiple values of 0.2 mm (using, in the end, twelve total 0.2 mm-thick plastic films). As reported in [71] and demonstrated here in Fig. 5-3, bringing the PCB sample closer to the central air gap causes the ac winding resistance to significantly increase, from $120\ \text{m}\Omega$ to $190\ \text{m}\Omega$, until the PCB is again moved away from the air gap approaching the bottom half-core. The highlighted area – which lies around the peak of the ac resistance – occurs when at least part of sample #6 is within the $310\ \mu\text{m}$ air gap.

Note that the results shown in Fig. 5-3 are affected by a small error due to the difficulty

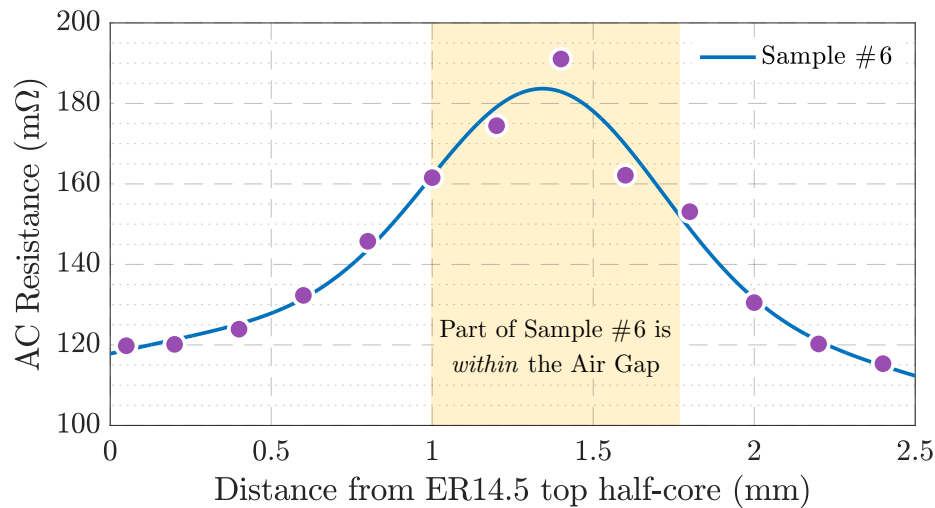


Figure 5-3: AC winding resistance at 2 MHz of a 4-turn ER14.5 gapped planar inductor vs. the distance between the top view of sample #6 and the top core half (the central air gap is equal to $310\ \mu\text{m}$).

of the measurement made with very small cores and insulator sheets. Indeed, the top half-core provides a smaller air gap ($110\text{ }\mu\text{m}$) than the bottom one and, despite this, the ac resistance at $x = 0\text{ mm}$ is slightly higher than the one at $x = 2.5\text{ mm}$ (the opposite is the case since the PCB is located further away from the air gap in the first case). Finally, Fig. 5-4 shows the ac and dc resistance trend, together with the inductance value, of several ER9.5 planar inductors having a different number of turns n_1 (2, 3, 4, 5, and 6) and air gap values ($88\text{ }\mu\text{m}$, $176\text{ }\mu\text{m}$). The information regarding the PCBs used to make n_1 is provided in Tab. 5.1 (last row) and, as mentioned before, all the samples are attached to the top

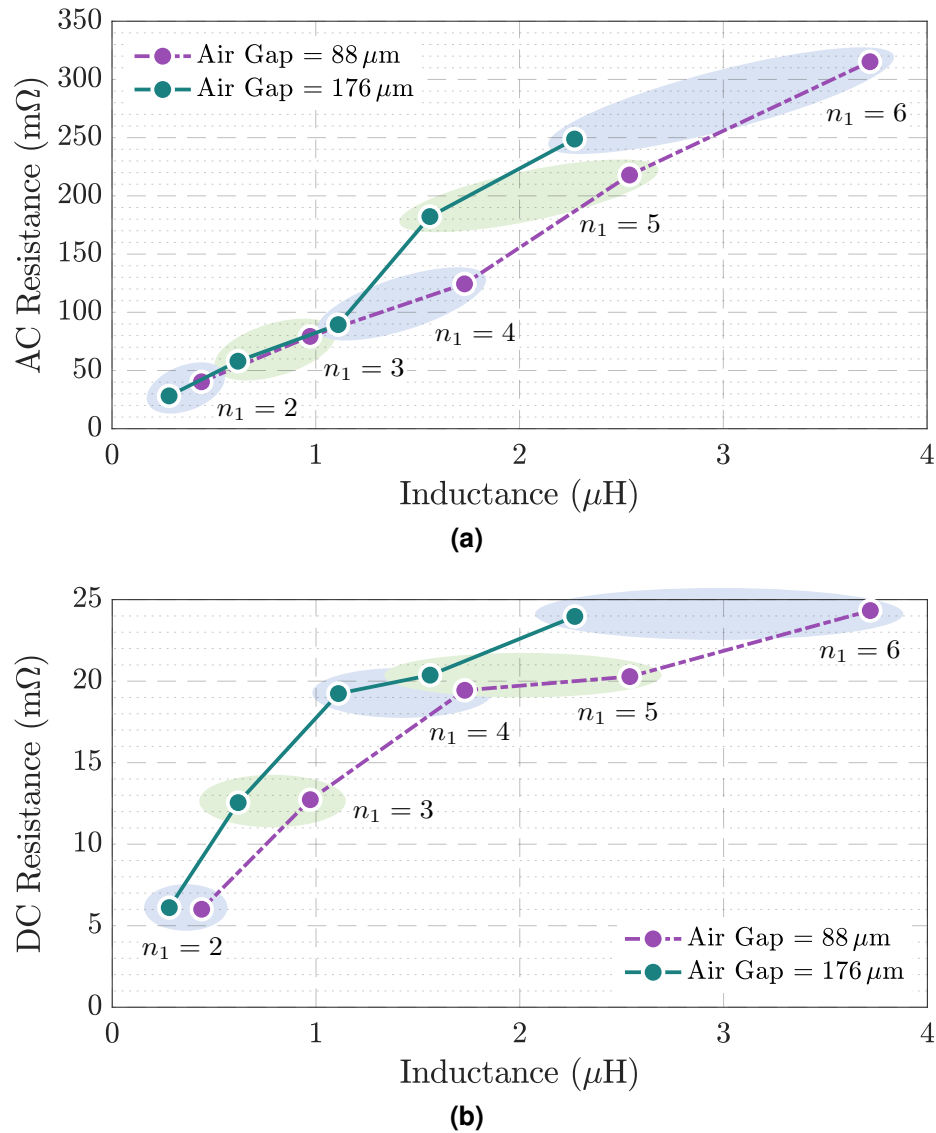


Figure 5-4: Value of (a) AC resistance, and (b) DC resistance vs. the inductance of a given ER9.5 planar inductor having different central air gap values and number of turns n_1 .

half-core separated by a 50 μm -thick insulator sheet. As expected, both the ac resistance (at 2 MHz) and dc resistance increase by increasing n_1 since the total path of the turns increases. As pointed out before, for a given number of turns the dc resistance doesn't change by increasing the central air gap value. On the other hand, for a given value of n_1 , the ac resistance tends to increase less when the air gap moves from 88 μm to 176 μm . For example, considering $n_1 \leq 4$, the resistance ratio R_{ac}/R_{dc} is almost equal to 6.5 and 4.6 when the air gap is equal to 88 μm and 176 μm , respectively. For $n_1 > 4$, the ratio between R_{ac} and R_{dc} worsens drastically still showing a better result for the larger air gap value.

5.3 Magnetics Design and Optimization Techniques for the Designed 2 MHz ACISC

The main specifications dictated by the considered application are reported in Ch. 3 and also here in Tab. 5.2. In addition, Tab. 5.3 lists the value of the components (at 2 MHz) – called here design #1 – proposed in Ch. 3 to operate the ACISC in ZVS resonant DCM operation. As demonstrated in Ch. 4 through a power loss breakdown, the largest loss contribution is associated with the transformer, and in particular with primary winding losses to be attributed to *skin* and *proximity* effects in the MHz range. Magnetics consisted of a 6 : 6 ER9.5 planar transformer – called here T_1 and reported in Tab. 5.4 with its specifications – and a 6-turn ER9.5 planar inductor called L_1 in Tab. 5.5. Considering the high ac winding resistance $R_{w,ac}$ obtained with T_1 ($\sim 250 \text{ m}\Omega @ 2 \text{ MHz}$), a new interleaved planar transformer T_2 with a fewer number of turns is now proposed to reduce winding losses. The specifications of T_2 – which has 4 turns on both sides and uses the same 430 μm -thick PCBs of T_1 – are reported in Tab. 5.4. The new 3F46 high-frequency power material is selected to limit the core losses despite the reduction of turns, whose power loss density at 2 MHz and $\hat{B} = 40 \text{ mT}$ is about 85% less than the 3F4 material used for T_1 . As can be seen in Tab. 5.4, T_2 provides an ac winding resistance reduction by almost 100 $\text{m}\Omega$ compared to T_1 .

Note that, to have a fair comparison with T_1 , the new planar transformer is supposed

Table 5.2: Converter specifications

Parameter	Symbol	Value
Nominal input voltage	V_g	12 V
Input voltage range	—	9 V – 18 V
Nominal output voltage	V_o	12 V
Nominal output current	I_o	600 mA
Nominal output power	P_o	7.2 W
Switching frequency	f_s	2 MHz

Table 5.3: ACISC parameters proposed in Ch. 3

Parameter	Symbol	Value
Equivalent primary leakage inductance	L_{pe}	75.2 nH
Equivalent magnetizing inductance	L_{me}	1.2 μ H
Equivalent transformer turns ratio	n_e	0.97
Input inductance	L_g	2.2 μ H
Clamp capacitor	C_s	1 μ F
Output capacitor	C_o	10 μ F
Design #1		

to have a similar magnetizing inductance value L_{me} and an air gap between central legs. Since this chapter aims at improving the magnetics, another important aspect to consider is the parasitic capacitance C_{tot} of the transformer. Looking at Tab. 5.4, C_{tot} is very high either for T_1 and T_2 (due to their interleaved structure) and, for this reason, can lead to EMI problems. For that purpose, planar transformer T_3 (reported in Tab. 5.4) is built around the same specifications as T_2 with the only difference that now two fully spaced sample #4 PCBs are used instead of interleaving multiple series-connected PCBs as done for the other prototypes. Fig. 5-5 shows the PCBs used for T_1 (and T_2) which host two turns each, one on top and the other one on the bottom, with the same insulator/layer thickness specifications as sample #5 (see Tab. 5.1). As it will be proved later in Sec. 5.4.2, the structure of T_3 allows to significantly reduce C_{tot} – which is less than 2 pF and almost 15 times smaller than the value obtained with T_2 – and also provides a slight improvement in terms of ac resistance for the reasons listed in Sec. 5.2. Finally, T_4 is built with 3 turns only (on both sides) to further improve the ac winding resistance value obtained with T_2 and T_3 . As can be noted, even if $R_{w1,ac}$ and $R_{w2,ac}$ are slightly decreased, no significant improvement is

Table 5.4: Planar transformer parameters characterized at $f_s = 2$ MHz

Transformer <i>turns</i>	Core Material	Air Gap (μm)	L_{me} (μH)	L_{pe} (nH)	n_e	$R_{w1,ac}$ ($\text{m}\Omega$)	$R_{w2,ac}$ ($\text{m}\Omega$)	C_{tot}^* (pF)
T_1 6 : 6	3F4	380	1.22	75.2	0.97	248	235	17.55
T_2 4 : 4	3F46	88	1.38	43.7	0.99	158	136	26.90
T_3 4 : 4	3F46	88	1.38	306.5	0.91	137	127	1.86
T_4 3 : 3	3F46	40	1.23	186.1	0.93	115	112	2.78

* C_{tot} is the total parasitic capacitance of the considered planar transformer. The obtained value accounts for both the inter-winding capacitance C_w and the parasitic capacitance between a given winding and the closest ER9.5 half-core.

Table 5.5: Input inductor parameters characterized at $f_s = 2$ MHz

Input Inductor <i>turns</i>	Core Material	Air Gap (μm)	L (μH)	$R_{w,ac}$ ($\text{m}\Omega$)
L_1 6	3F4	190	2.21	283
L_2 6	3F46	176	2.29	252

provided despite the reduction in the number of turns. For T_4 two ungapped cores are used with the central leg of one of them that has been manually reduced by almost $40 \mu\text{m}$ to meet the desired inductance value. Although $R_{w1,ac}$ is now equal to $115 \text{ m}\Omega$ (which is less than half of the value obtained with T_1), core losses become the largest loss contribution and the converter's efficiency drastically drops. For this reason, in the considered application an optimized 4 : 4 planar transformer provides the best trade-off between core and winding losses while keeping the temperature of the core under an acceptable level ($\sim 50^\circ\text{C}$ in nominal conditions).

The following section reports the experimental results obtained for three different designs. Design #1 is the same as shown in Ch. 3 (and summarized here in Tab. 5.3), where the specifications of T_1 and L_1 are reported in Tab. 5.4 and Tab. 5.5, respectively. Design #2 makes use of T_2 and L_1 , while Design #3 provides the best efficiency profile by considering an improved 6-turn input inductor L_2 and planar transformer T_2 . Note that using T_2 and not T_3 in design #3 allows having a higher value for C_c – since L_{pe} is significantly reduced (due to an interleaved structure) – which leads to reduced voltage stresses across C_c and D_r while providing almost the same value for the ac winding resistances.

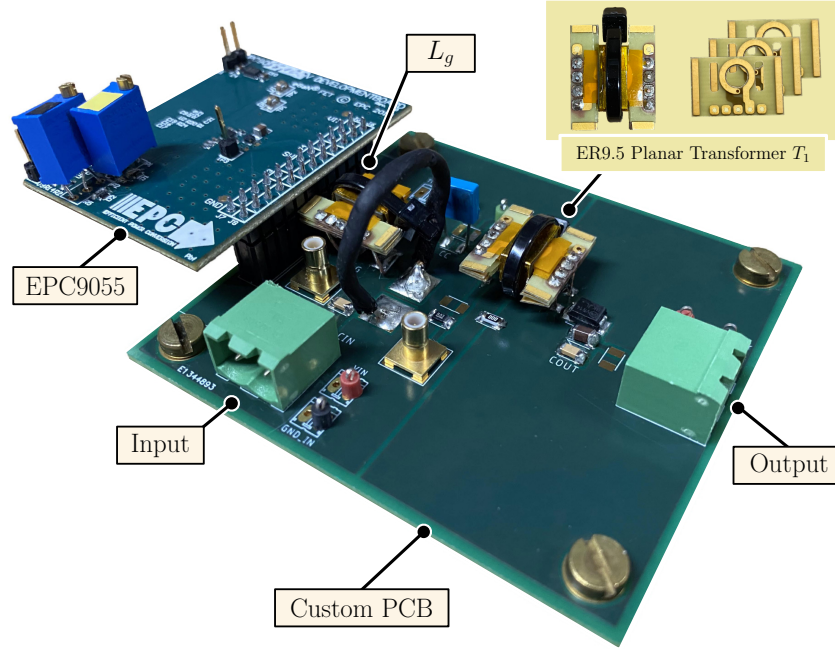


Figure 5-5: Picture of the experimental prototype.

5.4 Experimental Results

To prove the ZVS resonant DCM operation of the ACISC with new designs, the same 2 MHz 12 V, 600 mA GaN-based prototype shown in Ch. 3 and reported here in Fig. 5-5 (with a detail of T_1 and L_1) is used. Fig. 5-6 reports the converter experimental waveforms in nominal conditions ($V_g = V_o = 12$ V, $I_o = 600$ mA) when the ACISC makes use of design #2 (T_1 is replaced by T_2). Despite the high-frequency noise, which is mainly due to the high C_{tot} of T_2 , the resonant current $i_r(t)$ exhibits the behavior already shown in Ch. 3 (Fig. 3-6). Fig. 5-6 proves that the ZVS conditions are guaranteed either for Q_2 (at $t \sim 0$ ns) and Q_1 (at $t \sim 250$ ns) since the switching-node voltage $v_{sw}(t)$ is capable of completing the entire transition before the end of the two dead-times, resulting in ZVS turn-ON of both devices.

Note that, as reported in Ch. 3, the ZVS turn-ON of Q_2 (at $t = DT_s$) is always guaranteed due to the highest positive value obtained either by $i_g(t)$ and $i_r(t)$, which brings $v_{sw}(t)$ to the high level in a few nanoseconds. Fig. 5-6 also shows the experimental results obtained by using planar transformer T_3 to prove the importance of minimizing the parasitic capacitance C_{tot} of the transformer to significantly reduce the resonant current noise and,

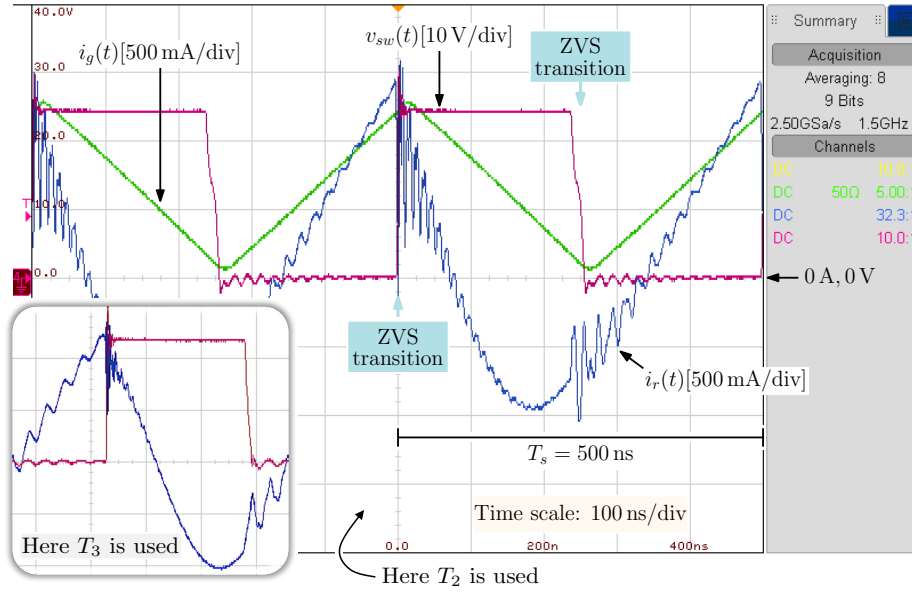


Figure 5-6: Experimental screenshot of the input current $i_g(t)$ (500 mA/div), the resonant current $i_r(t)$ (500 mA/div), and the switching node voltage $v_{sw}(t)$ (10 V/div) at $V_g = V_o = 12$ V and $I_o = 600$ mA. Time scale: 100 ns/div.

more in general, the in-circuit noise.

5.4.1 Efficiency Profile and Power Loss Breakdown Analysis

Fig. 5-7 compares the efficiency profiles of the designed 2 MHz ACISC when the latter is operated in resonant DCM operation with the three aforementioned designs. The comparison, carried out as a function of both input voltage V_g and output current I_o , reveals a peak efficiency with design #3 of 89.2% at $V_g = V_o = 12$ V and $I_o = 600$ mA, approximately 2% better than design #1 already shown in Ch. 3. In addition, the converter's efficiency at low input voltages is significantly improved since the ZVS condition for Q_1 is now fully satisfied.

At the nominal operating point, the ACISC exhibits a total power loss $P_{loss} = V_o I_o (1/\eta - 1)$ equal to 1055 mW and 872 mW for designs #1 and #3, respectively. Following the procedure shown in Ch. 4, the result of the power loss breakdown analysis for the ACISC operated with the two designs in nominal conditions is shown in Fig. 5-8. The analytical expressions used to estimate each power loss contribution are detailed in Ch. 4. *Note* that the body diode conduction losses of the switches are here neglected, as explained in

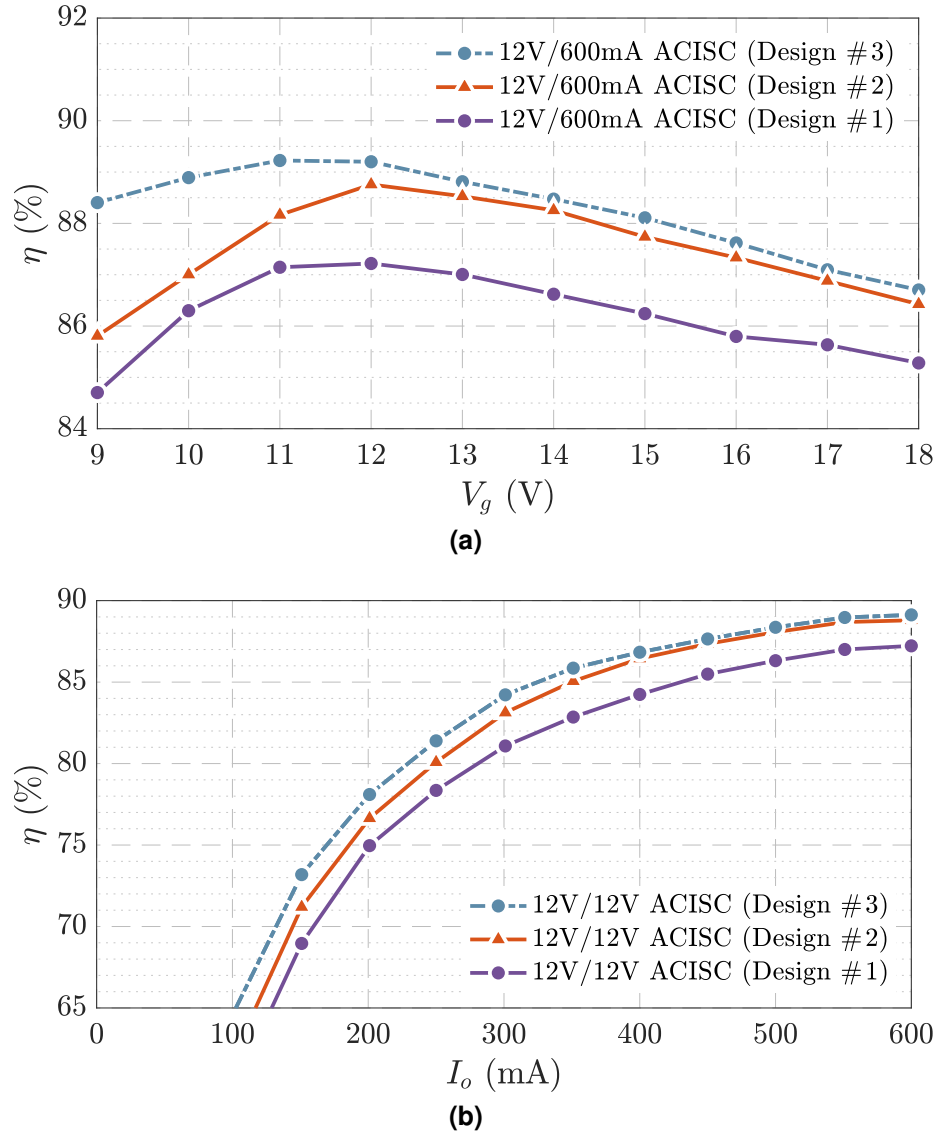


Figure 5-7: Efficiency profile of the designed 2 MHz ACISC considering designs #1, #2, and #3, as a function of (a) the input voltage V_g and (b) the output current I_o .

Ch. 4, in light of the preliminary dead-time optimization. As it can be seen in Fig. 5-8, the largest loss contribution associated with the primary transformer winding is now significantly reduced thanks to the use of T_2 which successfully reduces the ac winding resistance value by almost 100 m Ω . In addition, total input inductor loss P_{L_g} is minimized by using L_2 (which has much lower core losses than L_1) and P_{C_c} is now negligible since multiple parallel-connected SMD capacitors with less than 10 m Ω series-resistance are now used (instead of the previous through-hole capacitor, as shown in Fig. 5-5, having a 45 m Ω series-resistance).

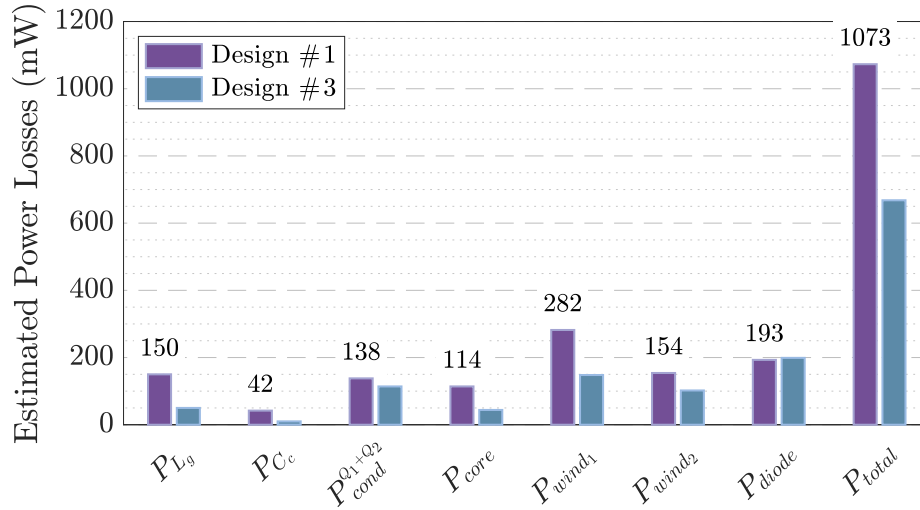


Figure 5-8: Power loss breakdown of the 2 MHz ACISC operated in nominal conditions ($V_g = V_o = 12$ V, $I_o = 600$ mA), considering designs #1 and #3.

5.4.2 Estimation and Minimization of the Inter-Winding Capacitance

To build a converter with optimized magnetics, the designer not only needs to find a way to reduce the ac winding resistances but also the inter-winding capacitance C_w between primary and secondary cannot be ignored, especially for planar transformers. Since a lower C_w is achieved at the expense of a higher leakage inductance L_{pe} [51], the designer is called to find the best trade-off for the considered application. As mentioned in Ch. 3, the resonant DCM operation is not affected by the variation of L_{pe} since the designer just needs to adjust the value of C_c to still guarantee the considered operating mode. For this reason, it is crucial to focus on minimizing C_w since the latter, subject to high-voltage stresses, causes leakage currents and consequently contributes to EMI problems due to an undesired low impedance path for common mode (CM) noise [72–74]. A comprehensive study of planar transformer parasitic elements is presented in [76], while a full procedure showing how to get the equivalent circuit using numerical methods is proposed to design low-parasitic planar transformers to address regulation problems in *LLC* converters.

This section – which aims at showing how to reduce and estimate the parasitic capacitance of the magnetics – focuses *only* on the inter-winding capacitance C_w which is generated between primary and secondary windings of a given planar transformer. As can be seen in Tab. 5.4, the 4 : 4 planar transformer T_3 represents the best solution in terms

5.4. Experimental Results

of total parasitic capacitance ($C_{tot} < 2 \text{ pF} @ 2 \text{ MHz}$) since the latter hosts two 4-turn PCBs (sample #4, Tab. 5.1) which are completely separated from each other. As it will be proved shortly, the more the distance between PCBs increases or the less the PCBs are interleaved, the more C_w decreases. Fig. 5-9 shows some photos, from different perspectives, of the planar transformer T_3 . In addition, such a figure shows the exploded view of the transformer highlighting the presence of C_w between the two samples and also the parasitic capacitance C_p between a given winding and the closest ER9.5 half-core. In a first approximation, C_{tot} can be derived as follows

$$C_{tot} \approx C_w + 2C_p. \quad (5.1)$$

To find the exact value of C_w , the planar transformer can be characterized with the precision

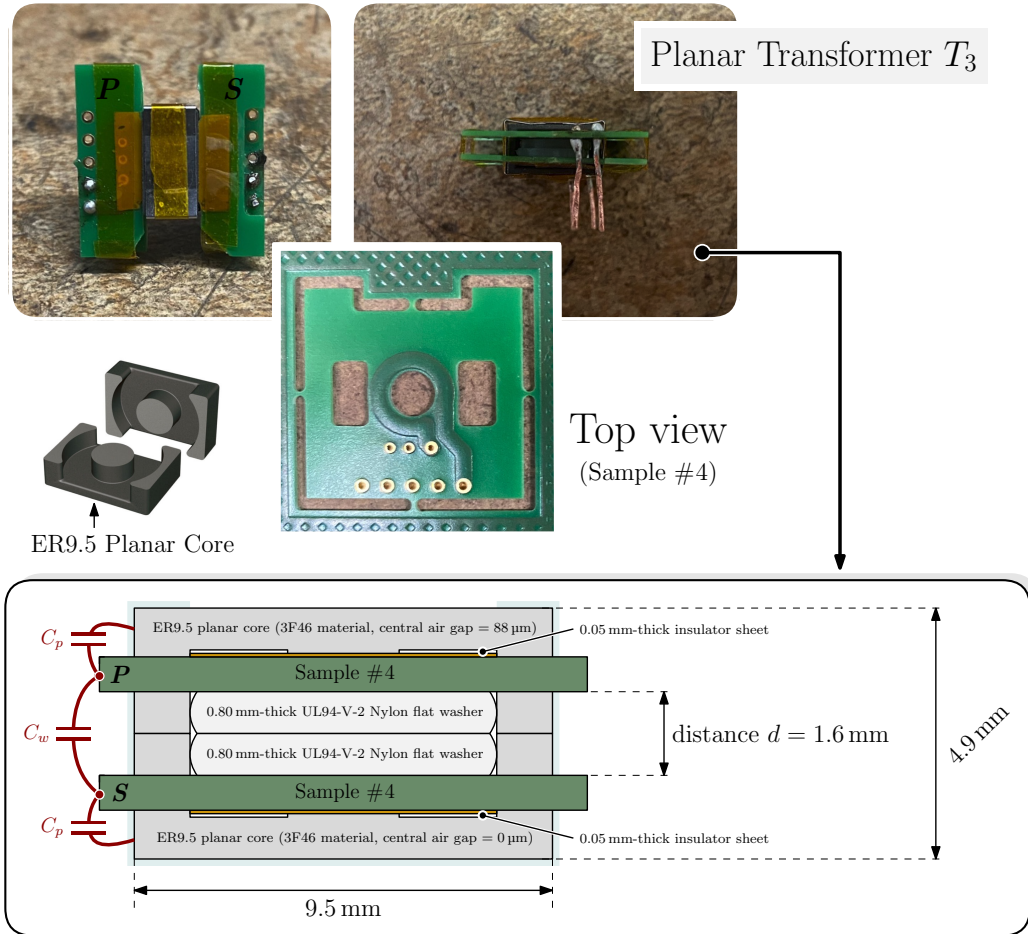


Figure 5-9: Photos and exploded view of the planar transformer T_3 , with an enlargement of the 4-turn PCB used for the windings (sample #4).

impedance analyzer without the two half-cores. On the other hand, such a value can be estimated considering T_3 a parallel plate capacitor having two conductive plates (PCBs) with an overlapping area of A_o separated by a distance equal to d , as reported in Fig. 5-10.

The expression is given below

$$C_w = \epsilon_0 \epsilon_r \frac{A_o}{d}, \quad (5.2)$$

where ϵ_0 and ϵ_r are the permittivity of free space ($8.85 \cdot 10^{-12} \text{F/m}$) and the relative permittivity of the material between layers, respectively. In this case, as can be seen in Fig. 5-9, $\epsilon_r = 3.4$ (@1 MHz) and $d = 1.60 \text{ mm}$ since two 0.80 mm-thick UL94-V-2 Nylon flat washers are used to separate the two PCBs hosted by T_3 . On the other hand, as can be noted by looking at Fig. 5-10,

$$A_o \approx \pi(R^2 - r^2) \quad (5.3)$$

because it represents the overlapped area of the turns ($R = 3.30 \text{ mm}$ and $r = 2.05 \text{ mm}$ are

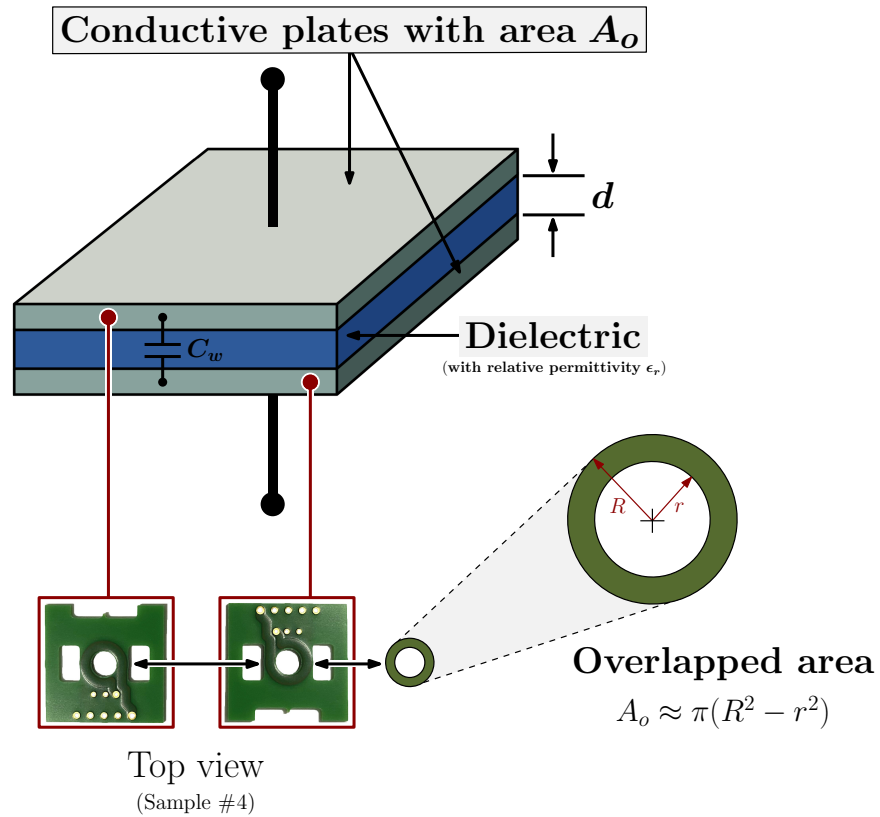


Figure 5-10: Planar transformer T_3 seen as a parallel plate capacitor having two conductive plates (PCBs), with an overlapping area of A_o separated by a distance equal to d .

the sample #4 outer and inner circumference radius, respectively). Under the aforementioned conditions, the estimated inter-winding capacitance is $C_w^{estimated} \simeq 0.40$ pF.

As it can be seen in Tab. 5.4, the estimated value is quite far from C_{tot} since the total parasitic capacitance accounts also for the capacitance C_p between a given winding PCB and the closest half-core. For this reason, to find the experimental value of C_w , planar transformer T_3 is further characterized without the two half-cores giving rise to a value close to the estimated one: $C_w = 0.69$ pF @ 2 MHz.

To summarize, looking at (5.2), inter-winding capacitance C_w can be reduced by

- increasing the distance d between PCBs
- reducing the overlapped area A_o
- reducing the number of intersections between PCBs
- using insulator materials to separate the PCBs with low relative permittivity ϵ_r

Note that both T_1 and T_2 show a high value for C_{tot} (17.55 pF and 26.90 pF, respectively) due to their interleaved structures (the distance d between PCBs is minimized). For these two planar transformers, which have n intersections between primary and secondary, their inter-winding capacitance value can be estimated with the following expression

$$C_w = n \cdot \epsilon_0 \epsilon_r \frac{A_o}{d}, \quad (5.4)$$

As a conclusion of this study, the inter-winding capacitance C_w of T_3 can be further reduced by leaving air ($\epsilon_r \approx 1$) between the two 640 μ m-thick PCBs to minimize its value. Following this approach, a value close to 0.35 pF is obtained.

Chapter 6

Active-Clamped Isolated Flyback Converter in the MHz Range

6.1 Theoretical Study of the Converter in Resonant DCM

An isolated alternative topology to the standard flyback converter and its viable substitute shown throughout this thesis is the so-called active-clamped isolated flyback converter (ACIFC) [39–42]. Fig. 6-1 reports the schematic diagram of the topology – which employs here two enhancement-mode GaN devices – and highlights the adopted model for the high-frequency transformer. Unlike the ACISC topology, this converter exhibits only a high-frequency transformer as magnetics (no input inductor L_g). Elements C_s and C are the clamping capacitor (in this case it also represents the resonant capacitor) and the output filter capacitor, respectively. Although this topology is capable of achieving ZVS for both switches, it does not employ the input inductor L_g which results in a higher differential mode (DM) conducted noise compared to the ACISC. Another drawback is the higher voltage stress across the switches due to a small value of C_s selected to guarantee a resonant DCM operation. However, one advantage of this topology is the lower voltage stress across the output diode D_r since there is no dependence on the significant voltage ripple across the resonant capacitor. Tab. 6.1 shows the expressions of the voltages and currents involved either in the two active-clamped topologies (ACISC and ACIFC) operating in resonant DCM and the standard flyback converter operating in continuous conduction

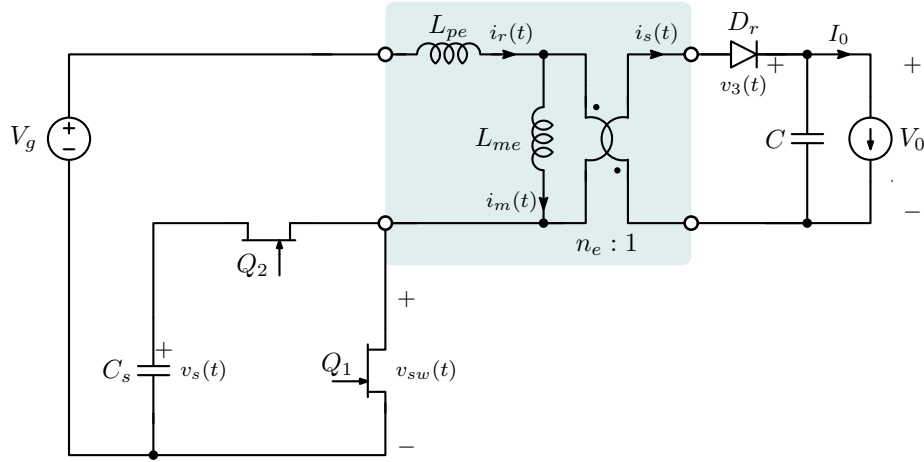


Figure 6-1: Schematic of the GaN-based active-clamped isolated flyback converter (ACIFC), highlighting the adopted model for the high-frequency transformer.

Table 6.1: Components' voltage/current stress for the three investigated topologies

<i>parameter*</i>		ACISC	ACIFC	Flyback
Input current	I_g Δi_g	$V_o I_o / (\eta V_g)$ $D V_g / (f_s L_g)$	// X	// X
Magnetizing current	I_m Δi_m	I_o / n_e $n_e V_o (1 - D) / (f_s L_{me})$	$I_g + I_o / n_e$ $D V_g / [f_s L_{me} (1 + \lambda)]$	// $n_e V_o (1 - D) / (f_s L_{me})$
Resonant current	I_r Δi_r	0 Δi_m	I_g //	// $I_m + \Delta i_m / 2$
Voltage stress	V_{Q1}, V_{Q2} V_{D_r}	$V_g / (1 - D)$ $V_o + v_c(t) / [n_e (1 + \lambda)]$	$v_s(t)$ $V_o + V_g / [n_e (1 + \lambda)]$	$V_g + n_e V_o$ //
Gain	M	eq. (3.30)	eq. (6.1)	eq. (6.1)
Missing parts		–	no L_g and C_c	no L_g, C_c, C_s , and Q_2

* I_x and Δi_x , referred to $x(t)$, stand for average current value and peak-to-peak current value, respectively. V_Q and V_{D_r} are the voltage stress across the switch and the output diode, respectively, while M is the converter's voltage gain. The last row, called "Missing parts", refers to the missing components by taking into account those in the ACISC topology. Finally, // means that the expression is equal to the one shown immediately on the left, and **X** means that there is no expression for the considered parameter.

mode (CCM) operation.

Note that the schematic of the flyback converter is the same as that shown in Fig. 6-1 replacing the active clamp (Q_2 and C_s) with a passive one. When the ACIFC is operated in resonant DCM, magnetizing and resonant currents $i_m(t)$ and $i_r(t)$ – which are reported in Fig. 6-2 – have a similar trend to that shown in Fig. 3-6: when the primary switch Q_1 is ON ($0 \leq t \leq DT_s$) there is no resonance now and the currents increase linearly. Expressions of resonant capacitor voltage $v_s(t)$ and of resonant current $i_r(t)$ are similar to the ones shown

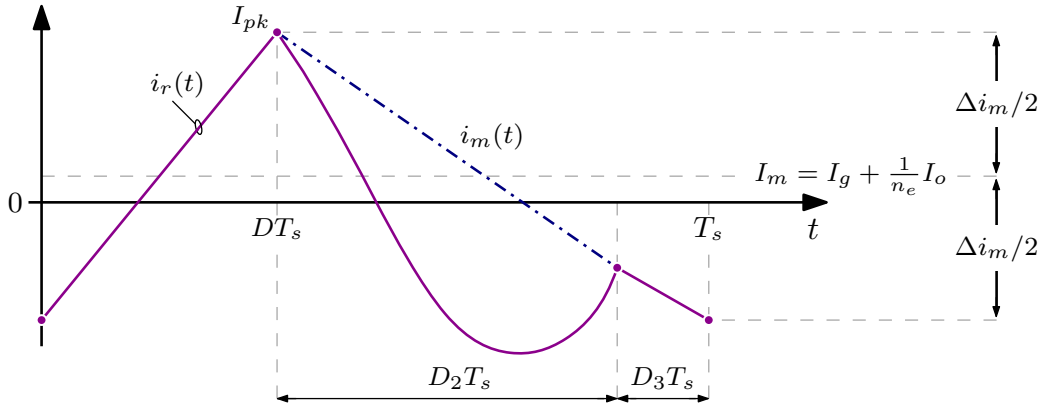


Figure 6-2: Resonant current $i_r(t)$ and magnetizing current $i_m(t)$ when the ACIFC is operated in resonant DCM operation.

Table 6.2: Coefficients used for the resonant voltage and current equations in the active-clamped isolated flyback converter (ACIFC)

Interval*	V_x	Z_o	ω_o	Q_1	Q_2	D_r	Resonance?	Note
DT_s	—	—	—	ON	OFF	OFF	no	shown in Fig. 6-2
D_2T_s	$V_g + n_e V_o$	Z_r	ω_r	OFF	ON	ON	✓	shown in Fig. 6-2
D_3T_s	V_g	Z_{ro}	ω_{ro}	OFF	ON	OFF	✓	shown in Fig. 6-2
$v_s(t) = Z_o I_{ri} \sin[\omega_o(t - t_i)] + (V_{Ci} - V_x) \cos[\omega_o(t - t_i)] + V_x$ $i_r(t) = \frac{1}{Z_o} (V_x - V_{Ci}) \sin[\omega_o(t - t_i)] + I_{ri} \cos[\omega_o(t - t_i)]$								

* Time instant t_i ($i = 1, 2, 3$) represents the beginning of each subinterval ($t_1 = 0$).

in (3.18) (now the coefficients multiplying the sine have opposite sign). Tab. 6.2 reports the new expressions of V_x , which depend on the topology and the considered subinterval, together with the resonant voltage and current equations. Following the procedure shown in section 3.3.2, even for the ACIFC is possible to find an analytical expression of the voltage gain M when the boundary CCM/DCM operating point is considered. The *volt-second* balance of the magnetizing inductance L_{me} yields

$$M \triangleq \frac{V_o}{V_g} = \frac{D}{1 - D} \frac{1}{n_e(1 + \lambda)}, \quad (6.1)$$

where D is the duty cycle of the low-side switch Q_1 , n_e is the equivalent transformer turns ratio, and $\lambda \triangleq L_{pe}/L_{me}$ is the inductance ratio.

Note that (6.1) is equal to (3.30) once the voltage ripple across the ACISC's resonant capacitor C_c is neglected ($v_c(t) \approx V_c = V_g$).

Table 6.3: ACIFC specifications

Parameter	Symbol	Value
Input voltage	V_g	9 V – 18 V
Nominal output voltage	V_o	12 V
Nominal output current	I_o	600 mA
Nominal output power	P_o	7.2 W
Switching frequency	f_s	2 MHz

6.2 Experimental Results

The main specifications dictated by the considered application are reported in Tab. 6.3. The 100 V, 1.7 A EPC2106 eGaN[®] FET pair [48] is still selected to implement Q_1 and Q_2 . As already mentioned in section 3.3.3, the turn-ON of the low-side switch Q_1 represents the critical ZVS transition for which $i_L(T_s)$ must be sufficiently *negative*. Using (3.32) – where V_s is the value of $v_{sw}(t)$ at the end of the period – it is possible to estimate the amount of current required for the critical ZVS transition assuming to have the same dead-time set for the ACISC ($t_d \approx 15$ ns). As can be seen in Fig. 6-3 – which shows the experimental

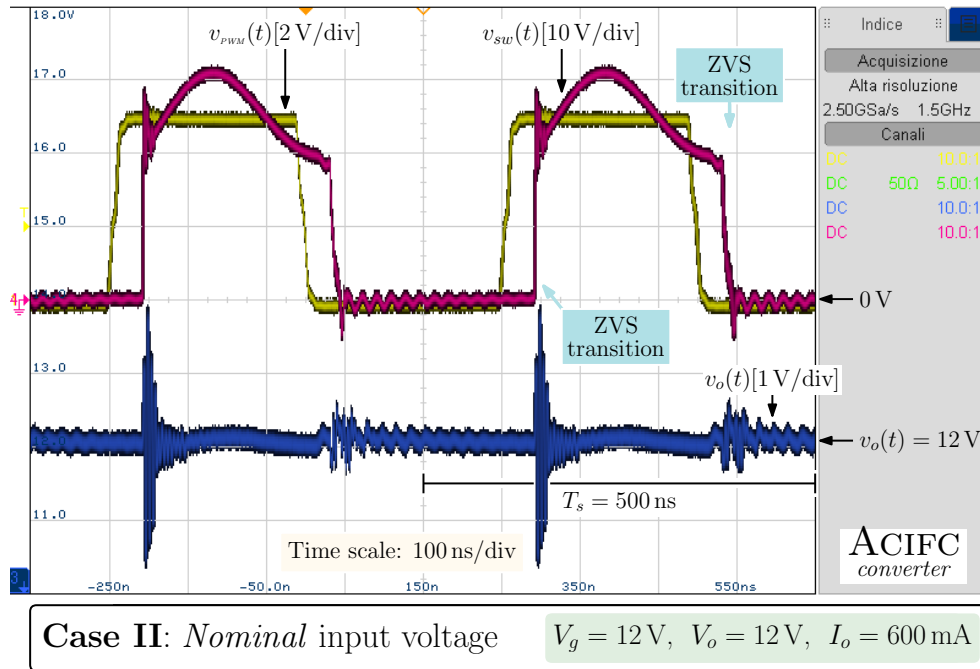


Figure 6-3: Experimental screenshot of the output voltage $v_o(t)$ (1 V/div, $v_{offset} = 14$ V), the input PWM $v_{PWM}(t)$ (2 V/div) used to drive the switches, and the switching node voltage $v_{sw}(t)$ (10 V/div) at $V_o = 12$ V and $I_o = 600$ mA, when $V_g = 12$ V. Time scale: 100 ns/div.

screenshot of $v_{sw}(t)$ in nominal condition – the value of the latter at $t = T_s$ is almost 6 V lower than the one obtained for the ACISC topology (see Fig. 3-15b). This result – which is confirmed by simulation results shown in Fig. 6-4 – represents an advantage for the ACIFC topology since a lower current $|i_L(T_s)|$ is sufficient to turn Q_1 ON with zero-voltage. On the other hand, as shown in Tab. 6.1, a big disadvantage of this topology is the higher average magnetizing current value I_m , which calls for a high peak-to-peak magnetizing current ripple value Δi_m (*i.e.* a reduced L_{me} value) to provide a sufficiently *negative* value to $i_L(T_s)$. This leads to higher conduction losses P_{cond} of the eGaN[®] pair and, more importantly, higher transformer primary winding losses P_{wind_1} . As can be seen

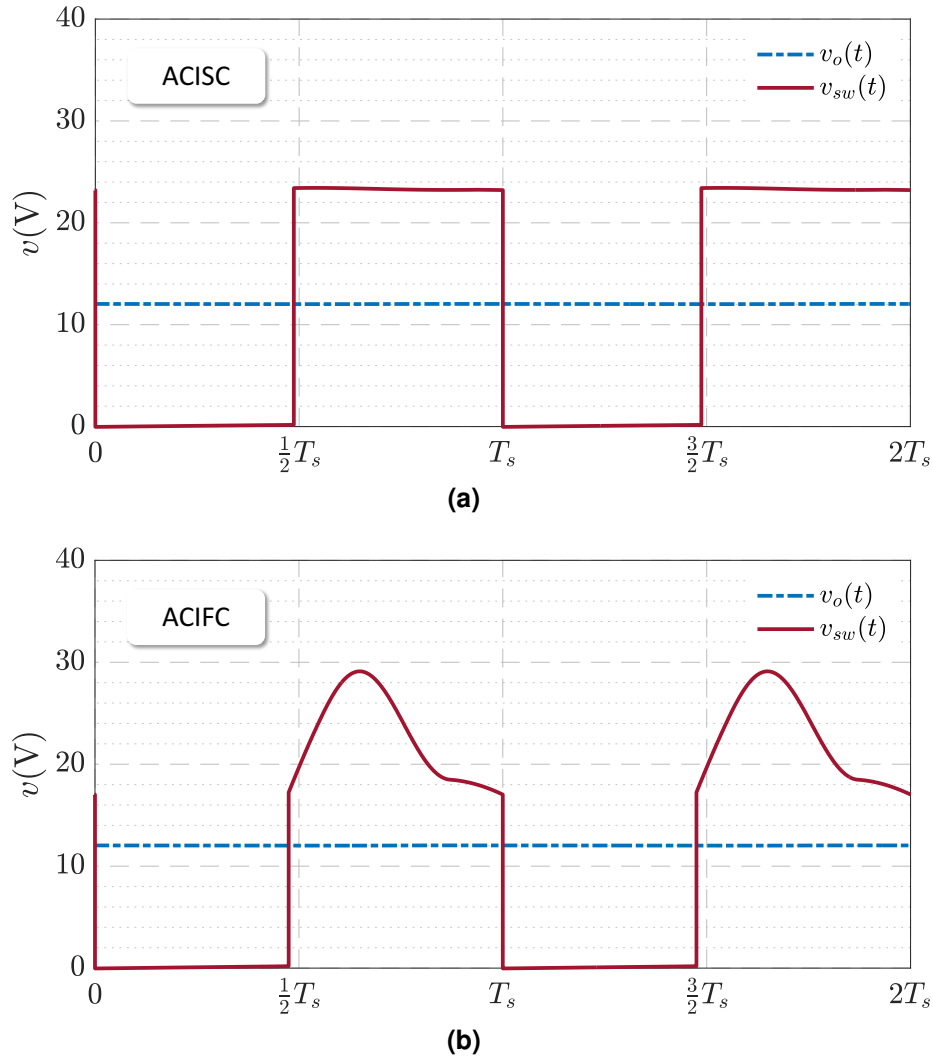


Figure 6-4: Simulation results of the output voltage $v_o(t)$ and the switching node voltage $v_{sw}(t)$ in nominal conditions ($V_o = V_g = 12$ V, $I_o = 600$ mA), for the (a) ACISC and (b) ACIFC.

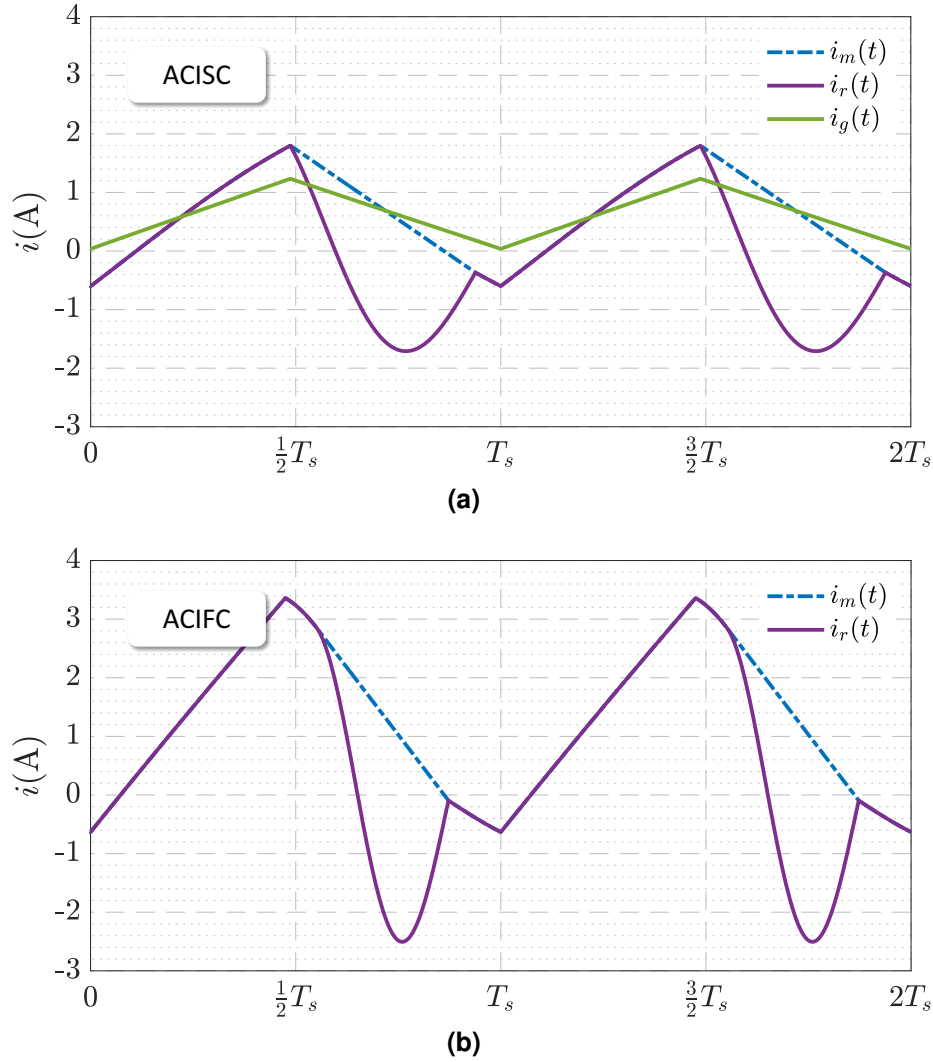


Figure 6-5: Simulation results of the magnetizing current $i_m(t)$ and the resonant current $i_r(t)$ in nominal conditions ($V_o = V_g = 12$ V, $I_o = 600$ mA), for the (a) ACISC and (b) ACIFC.

in Fig. 6-5 – which shows the simulation results for the main currents involved in the two topologies – the ACIFC presents higher currents which translate into higher switches conduction losses and transformer winding losses. A resonant capacitor $C_s = 20$ nF is used as a replacement of the one hosted by the EPC9055 development board to still have the resonant DCM operation.

Fig. 6-6 compares the efficiency of the designed 2 MHz ACISC topology with that of the 2 MHz ACIFC. The measured parameters of the 6 : 6 non-optimized interleaved planar transformers used to obtain such results are reported in Tab. 6.4. For this first comparison between the two topologies, ACISC follows the so-called design #1 and the values of its

components are reported in Tab. 3.5. The goal of this comparison is to use the same transformer for both topologies (its photo is shown in Fig. 3-14) with different central air gap values to obtain the desired magnetizing inductance value L_{me} according to the investigated

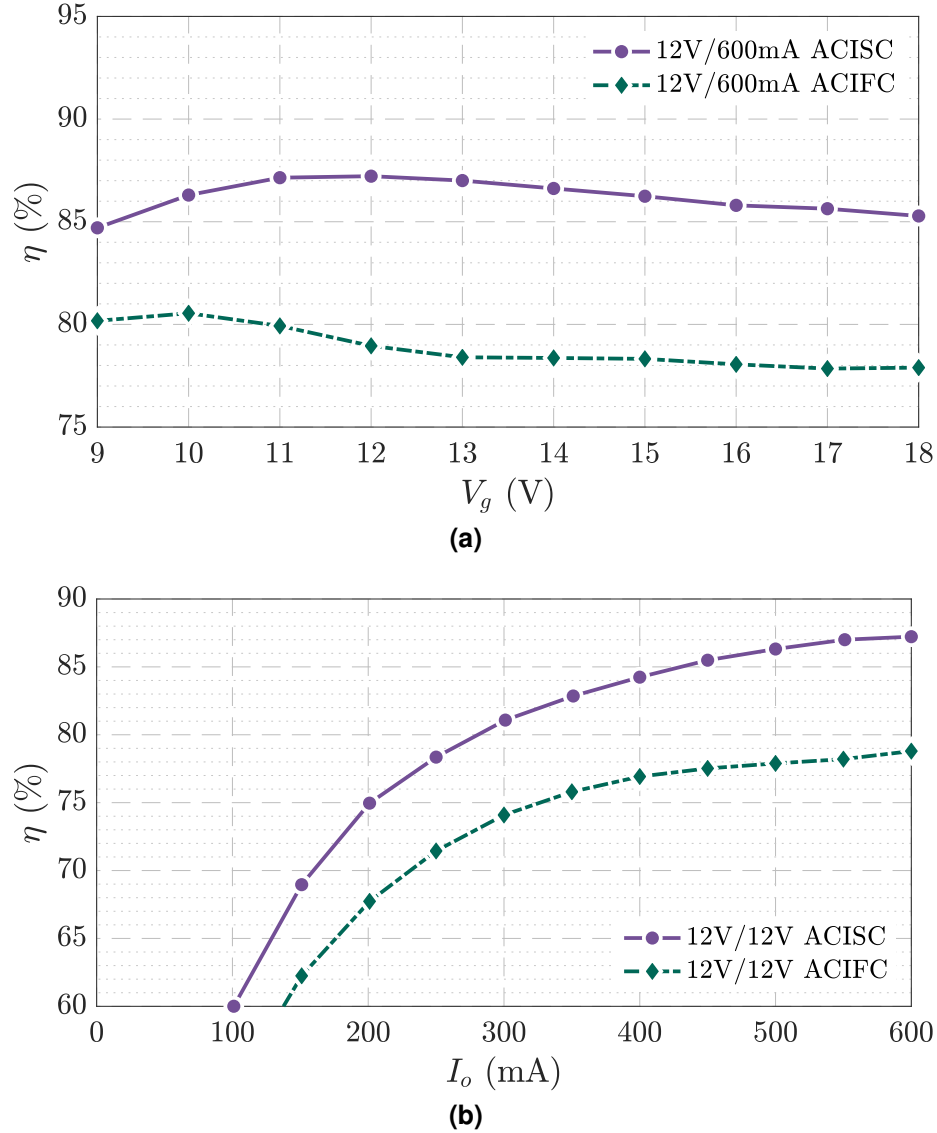


Figure 6-6: Efficiency comparison between the designed 2 MHz ACISC and the designed 2 MHz ACIFC, as a function of (a) the input voltage V_g and (b) the output current I_o .

Table 6.4: Planar transformer parameters characterized at $f_s = 2$ MHz

	Turns	Core material	Air Gap (μm)	L_{me} (μH)	L_{pe} (nH)	$R_{w1,ac}$ (m Ω)	$R_{w2,ac}$ (m Ω)
ACISC $\hookrightarrow$ transformer	6 : 6	3F4	380	1.22	75.2	248	235
ACIFC $\hookrightarrow$ transformer	6 : 6	3F4	680	0.62	75.7	197	192

topology. This way, the internal structure of the interleaved 6 : 6 planar transformer doesn't change (same PCBs, same connections and distances between them, same L_{pe} due to an interleaved structure and comparable ac winding resistance values $R_{w,ac}$). The comparison, carried out as a function of both input voltage V_g and output current I_o , reveals a peak efficiency of the designed ACISC of 87.22 % at $V_o = 12$ V and $I_o = 600$ mA, approximately 8 % better than the ACIFC topology.

Note that the efficiency profile of the ACIFC is far from the ACISC one mainly due to the low value of L_{me} required for the ZVS operation which results in a significant increase in primary transformer winding losses. Although the ac winding resistances of the ACIFC (~ 200 m Ω) are lower than those of ACISC (~ 250 m Ω), its transformer winding losses are significantly higher due to a much higher rms value of the current flowing through the windings (see Fig. 6-5). As shown for the ACISC, the transformer used for the ACIFC can be further improved by decreasing the number of turns while using the new 3F46 high-frequency power material to significantly decrease both the winding and core losses.

6.3 Advantages and Disadvantages of the Topology

The main advantages/disadvantages of the active-clamped isolated flyback converter (ACIFC) operated in resonant DCM are listed below, focusing on the comparison between the latter and the topology investigated throughout this thesis (ACISC):

Main advantages:

- reduced converter's footprint area due to the absence of the input inductor L_g and capacitor C_c
- lower voltage stress across the output diode D_r ; there is dependence on V_g and not on the significant voltage across the resonant capacitor $\hookrightarrow v_c(t) = V_g + v_{ripple}(t)$
- lower current required to turn the switches ON with zero-voltage

Main disadvantages:

- higher differential mode (DM) conducted noise mainly due to the absence of L_g

- higher voltage stress across the switches due to a significant reduction of the resonant capacitor value C_s to guarantee the resonant DCM operation
- higher switches conduction losses and transformer winding losses due to a higher average magnetizing current value I_m which calls for a high peak-to-peak magnetizing current ripple Δi_m to satisfy ZVS conditions

Adding up the advantages and disadvantages listed above, it was proved that the flyback converter with active clamp (ACIFC) has a significantly lower efficiency profile than the ACISC once they host the same planar transformer structure, the same EPC9055 development board, and run at $f_s = 2$ MHz.

In addition, as it will be proved in the next section, the ACIFC topology does not represent the best solution (compared to the ACISC) also in terms of electromagnetic interference (EMI) noise *and* temperature in the main components.

Chapter 7

EMI Analysis and Temperature Considerations

7.1 An Overview of Conducted EMI Specifications for Power Converters

Nowadays, power converters play an important role in electrical and electronic systems. Because of the switching action, all switch-mode power converters produce electrical noise, whereas the latter is also known as electromagnetic interference (EMI). The reason why it is called “interference” is because the electrical noise can either interfere with the operation of the device itself, or it can interfere with other systems in close to the noise producing culprit. Several governing bodies regulate the permissible levels/limits of conducted and radiated emissions generated by a final product (*e.g.* a commercially available power converter) in order to maintain electromagnetic compatibility (EMC).

This first section focuses on EMI standards for conducted emissions, particularly those relevant to automotive applications. In recent years, power converters embedded within products for the automotive market are increasingly demanding high switching frequencies, advances in circuit topologies, and high-speed switching power devices. The production of EMI is mainly due to the use of switching components (*e.g.* MOSFETs) by the power converters to convert voltages and power levels. These converters host either transformers

and/or capacitors, as well as inductors to *i)* boost, *ii)* reduce or *iii)* isolate electric power at the desired switching frequency. For all these reasons, an understanding of the EMI standards related to the considered low-power battery-connected application is essential.

7.1.1 EMI Standards for Automotive: CISPR 25

From a perspective of an automotive electronic product designer, the essential conducted emissions tests are those specified by the standard called “CISPR 25”. This international standard applies to automotive components and modules, with measurements performed using one or two $5\text{ }\mu\text{H}/50\text{ }\Omega$ Artificial Networks (ANs) depending on the grounding configuration. In addition, this standard details limits and procedures for the measurement of on-board radio disturbances in the range of 150 kHz to 108 MHz (in specific frequency bands) and applies to any electronic/electrical component intended for use in vehicles (*such as* the ACISC, ACIFC, and flyback converters). The conducted emission limits for Peak (PK), Quasipeak (QP), and Average (AVG) signal detectors – which are reported in Tab 7.1 for each frequency band (considering Class 5) – are intended to protect for receivers installed in a vehicle from disturbances produced by components/modules in the same vehicle.

Note that, for an acceptable radio reception in a vehicle, it is recommended that the conducted noise should not exceed the values shown in Tab 7.1. Multiple limit levels are defined since the mounting location, vehicle body construction and harness design can affect the coupling of radio disturbances to the on-board radio.

Table 7.1: CISPR 25 Class 5 conducted emission limits – voltage method

Service / Band *	frequency (MHz)	Peak (dB μ V)	Quasipeak (dB μ V)	Average (dB μ V)
LW	0.15 – 0.30	70	57	50
MW	0.53 – 1.80	54	41	34
SW	5.90 – 6.20	53	40	33
FM	76 – 108	38	25	18
TV Band I	41 – 88	34	–	24
CB	26 – 28	44	31	24
VHF	30 – 54	44	31	24
VHF	68 – 87	38	25	18

7.2 Comparison Between ACISC, ACIFC and a Commercial Flyback Converter

This section aims at comparing the designed 2 MHz ACISC topology with the 2 MHz ACIFC and the 400 kHz commercial flyback converter shown throughout this thesis, both in terms of electromagnetic interference noise *and* temperature in the main components.

7.2.1 EMI Analysis

In addition to the CISPR 25 EMI requirements, automotive power supplies should avoid some frequency bands due to their high sensitivity. One of them is the AM band (540 kHz – 1.6 MHz) because of the radio system hosted by the vehicle. Since the low-frequency AM band is the switching power supply's main working frequency band, the actual frequency band remaining for the switching power supply is limited. In the past, most dc-dc power converters that are running off the automotive battery were switching below 500 kHz and lots of filtering was needed and synchronization was used as well to avoid the tuned frequency of the AM radio.

In recent years, one of the trends in the automotive market is moving to 2 MHz power conversion to improve such aspects. The reason behind this choice is that there are no more harmonics in the AM band and the input filters are significantly smaller. Another benefit is that inductors, capacitors, and transformers are smaller as well. Therefore, to avoid *i)* the AM frequency band (540 kHz – 1.6 MHz), *ii)* the CISPR 25 limits set for the MW frequency band (530 kHz – 1.8 MHz) while *iii)* reducing the size and cost of the converter's passive components, the two GaN-based ACISC and ACIFC topologies switch at $f_s = 2$ MHz. Following this choice, the amplitude of the first converter's spectral line – which is the highest one – does not represent a problem since the standard CISPR 25 does not set constraints for such a frequency. On the other hand, as it will be shown later, a high converter's switching frequency will result in increased conducted and radiated emissions for frequencies greater than 30 MHz. In this study, the experimental setup for the EMI measurements of the three investigated topologies (ACISC, ACIFC, and a commercial

7.2. Comparison Between ACISC, ACIFC and a Commercial Flyback Converter

flyback) is shown in Fig. 7-1, and consists of

- a device under test (DUT)
- the equipment necessary to supply the converter (power supply V_g , waveform generator to drive the EPC2106 eGaN[®] FET pair, and the power supply for gate drivers)
- a line impedance stabilization network (LISN) placed between the power supply V_g and the DUT
- an electromagnetic compatibility (EMC) analyzer to measure the noise level

Although it is not an official EMI setup that literally follows the standard CISPR 25, such an EMI setup has been adopted for all three investigated topologies using the same cables

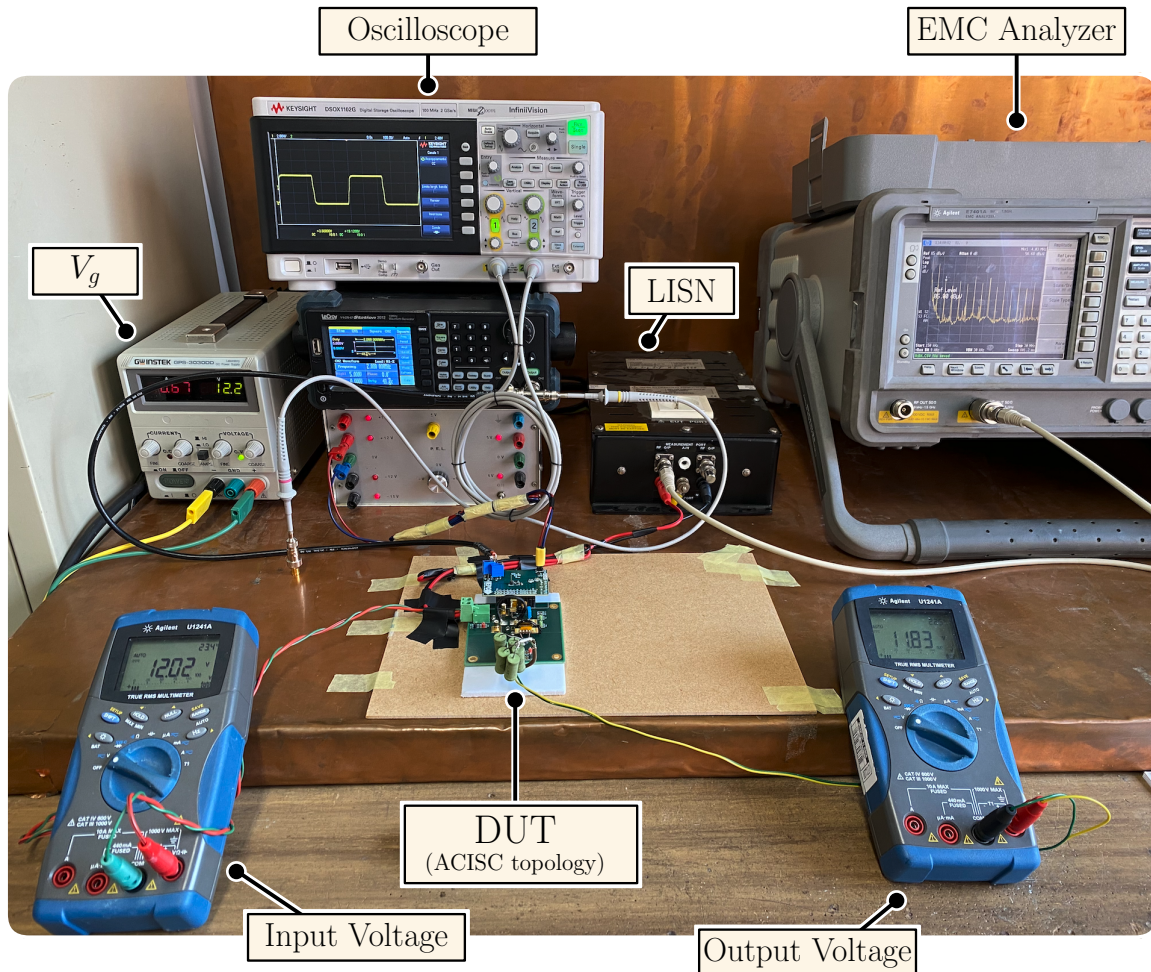


Figure 7-1: Experimental setup for the EMI measurements.

and maintaining the same distances. As mentioned above, the standard CISPR 25 – which defines measurement setups and EMI limits of conducted emissions for automotive devices with low-voltage (LV) sources or loads – is adopted, while Class 5 (*Peak* detector) is considered for the conducted disturbances' limits. Fig. 7-2 shows the photo of *i*) the LeCroy WaveStation 2012 waveform generator (WG) used to drive the EPC2106 eGaN[®] FET pair, *ii*) the ACISC employed as DUT, and *iii*) two coaxial cables – called “Cable 1” and “Cable 2” – used to drive the GaN switches through channel 2 (CH2) of the WG.

Fig. 7-3 shows the first EMI results seen at the EMC analyzer, which are obtained considering three different cases where the power supply V_g is not yet turned-ON:

- **Case 1:** WG not connected to DUT
- **Case 2:** WG connected to DUT through CH2, where the latter is OFF
- **Case 3:** WG connected to DUT through CH2, where the latter is ON

As can be seen in Fig. 7-3, once the WG is connected to the DUT through one of the two coaxial cables and CH2 is still OFF (Case 2), the noise level in the low-frequency range

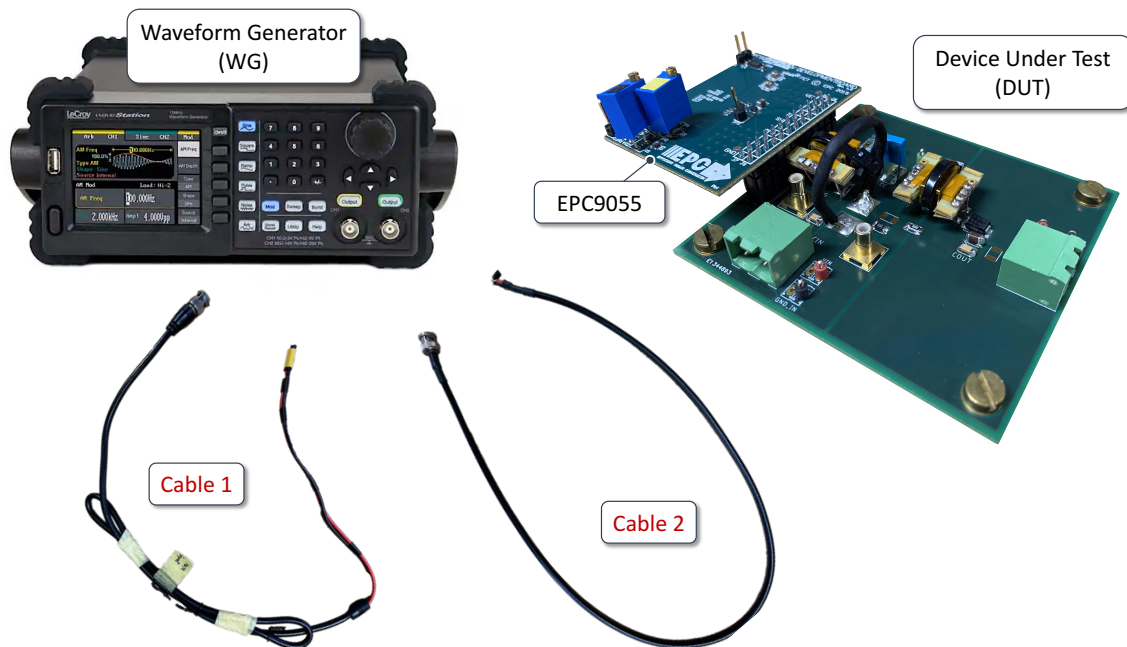


Figure 7-2: Photo of the waveform generator (WG) and coaxial cables used to drive the EPC2106 eGaN[®] FET pair hosted by the EPC9055 development board.

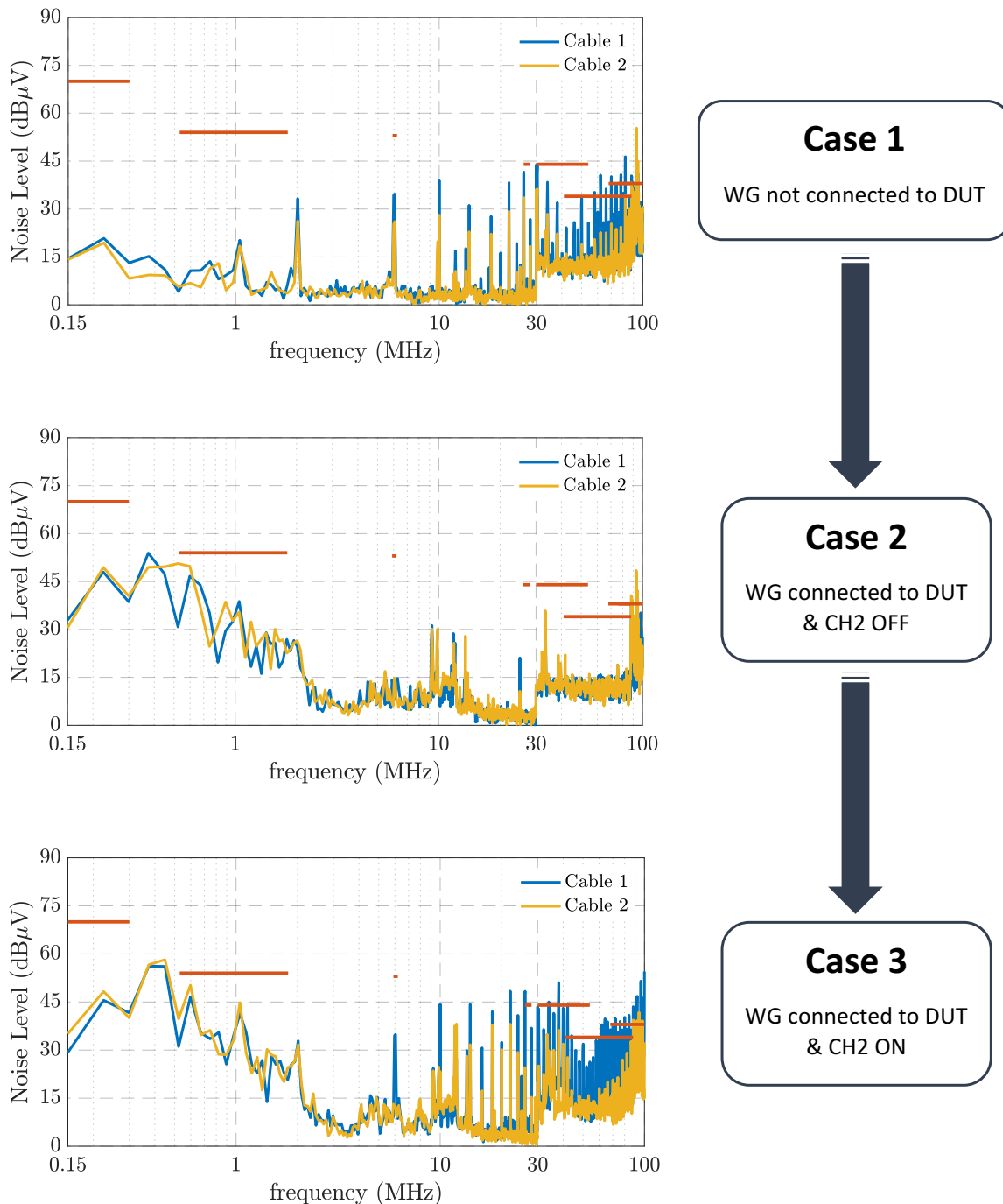


Figure 7-3: EMI results obtained in three different cases using the two coaxial cables shown in Fig. 7-2. EMI limits (CISPR 25, Class 5, *Peak* detector), highlighted in red, are reported in Tab 7.1.

($< \sim 2$ MHz) increases significantly. This is because an external waveform generator is used to drive the switches, causing additional noise, instead of having an integrated low-noise PWM (as it happens, for example, with the 400 kHz commercial flyback converter). Once CH2 is turned-ON, as it happens in Case 3 (shown in Fig. 7-3), a heavy increase in terms of noise is observed in the high-frequency range ($> \sim 10$ MHz) in addition to what has already been observed in Case 2 due to the EPC2106 eGaN[®] FET pair that is now switching at $f_s = 2$ MHz. The result coming from Case 3 represents what will be considered as *ground noise level* since all the instruments are now turned-ON, together with the switches that are now running at the desired switching frequency, while the power supply V_g is not yet turned-ON. As can be seen from Fig. 7-3, Cable 2 is better than Cable 1 in terms of noise since the latter, as shown in Fig. 7-2, is longer than Cable 2 and the two positive/negative terminals used to provide the PWM signal to the EPC9055 development board are significantly longer than those used in Cable 2, thus contributing to injecting more noise into the dc-dc power converter. For this reason, Cable 2 is used for the EMI tests and Fig. 7-4 shows both the ground noise level which will be considered for the ACISC, and the connections of the cables between the instruments and the EPC9055 development board. Since Fig. 7-3 showed that an external WG introduces additional noise at low frequencies, a resistive load is used instead of connecting an active load with the aim of not injecting additional noise into the circuit.

The EMI results obtained for the three investigated topologies once the power supply V_g is turned-ON are now presented. Fig. 7-5a, Fig. 7-6a, and Fig. 7-7a provide the conducted emission at the input V_g for ACISC, ACIFC, and the 400 kHz commercial flyback, respectively (both the standard noise level and the CISPR 25 limits are shown). Test results are obtained when the three converters are operated in nominal conditions ($V_g = V_o = 12$ V, $I_o = 600$ mA) without EMI filters and with roughly the same total input capacitance (as shown in Fig. 7-1, a resistive load of $20\ \Omega$ is used and obtained by the parallel of multiple resistances). On the other hand, Fig. 7-5b, Fig. 7-6b, and Fig. 7-7b show the same results as the previous figures with the aim of highlighting the input common mode (CM) and differential mode (DM) conducted noise.

As can be seen, ACISC is better than the ACIFC topology in terms of conducted emis-

7.2. Comparison Between ACISC, ACIFC and a Commercial Flyback Converter

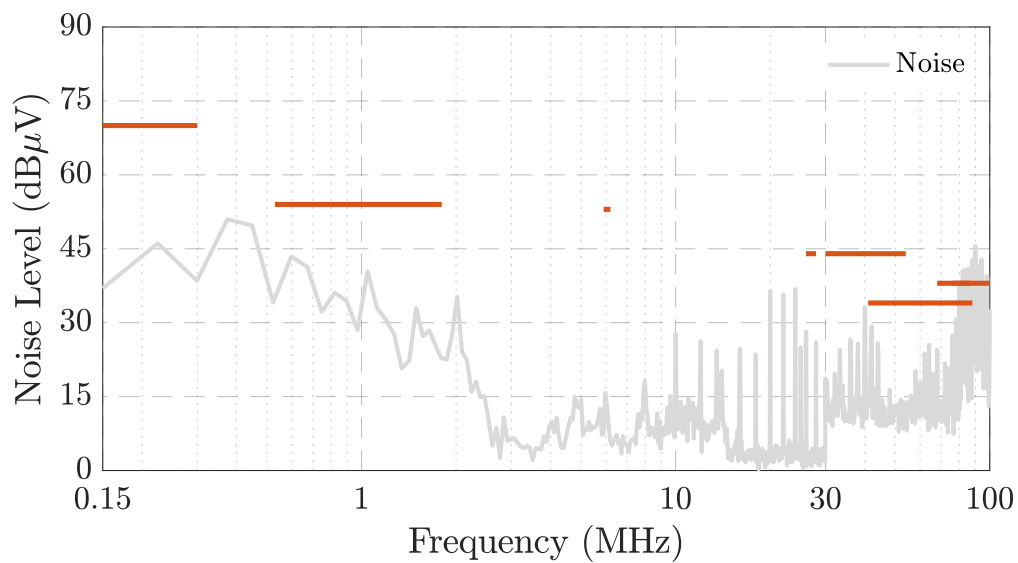
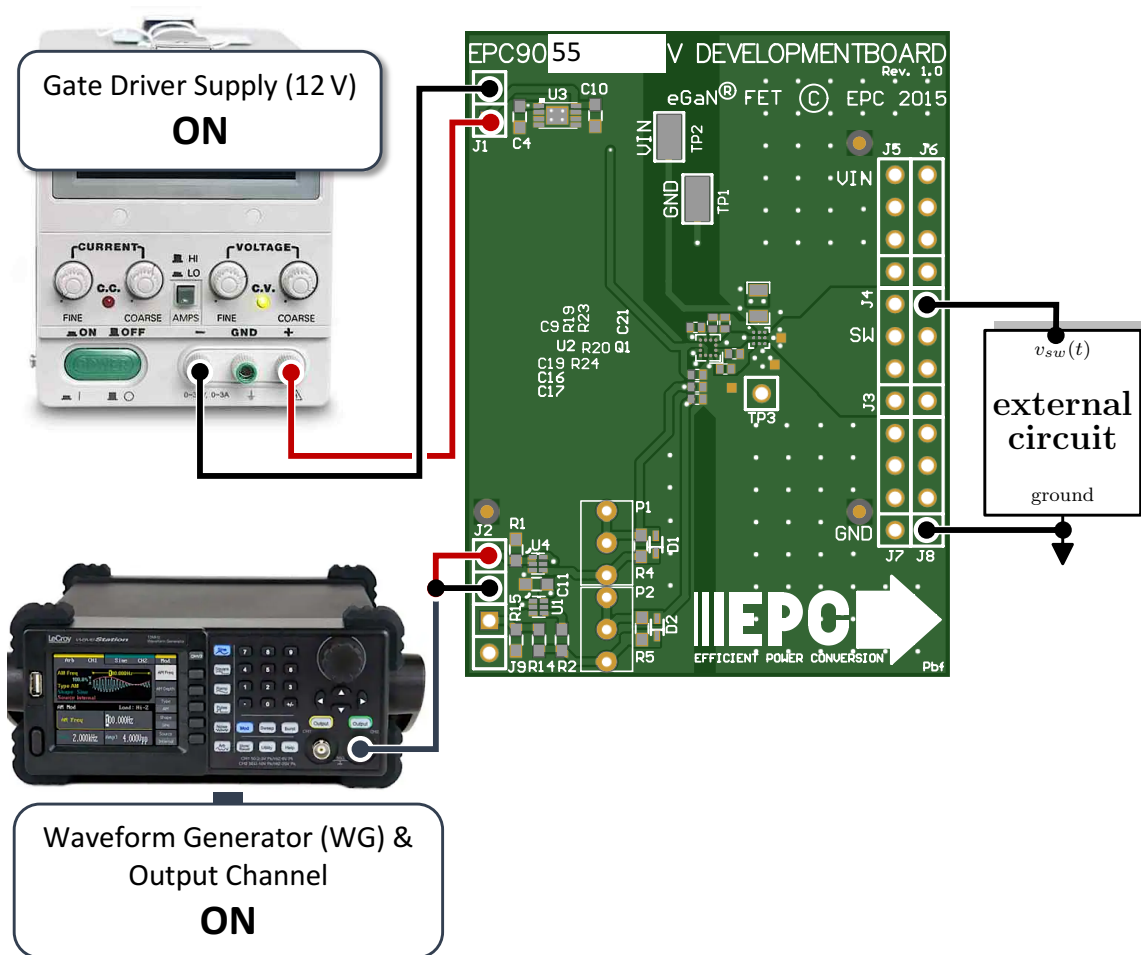


Figure 7-4: Ground noise level vs. frequency for the ACISC topology, together with the connections of the cables between the instruments and the EPC9055 development board.

sion mainly due to the presence of the input inductor L_g which acts as a filter. Comparing Fig. 7-5a with Fig. 7-6a, a reduction of almost 10 dB μ V can be observed in the ACISC topology by looking at the first spectral line (at $f_s = 2$ MHz). The much higher dv/dt of GaN devices, compared with their Si counterparts, increases conducted - and most likely radiated - emissions, especially in terms of CM noise. Indeed, Fig. 7-5b and Fig. 7-6b reveal such dominance of the CM noise in the whole considered frequency range. As expected, test results show that the frequency spectrum of the two GaN-based prototypes exceeds the CISPR 25 limits in the high-frequency range: the use of EMI filters, a better layout, and the optimization of the magnetics in terms of parasitics minimization (as shown in Ch. 5) can help the designer to keep the high-frequency spectral lines under the required limits. In general, the investigated 400 kHz commercial flyback converter provides better EMI results than the two GaN-based topologies since it has a better layout and hosts low dv/dt devices which allow to reduce conducted and radiated emissions. On the other hand, since its frequency is five times lower than the designed ACISC and ACIFC, its frequency spectrum is significantly denser.

Note that, as mentioned above, the increased ground noise level in the low-frequency range observed in Fig. 7-5a and Fig. 7-6a, compared with Fig. 7-7a, is caused by the external waveform generator used to drive the EPC2106 eGaN[®] FET pair [48] hosted by the EPC9055 development board. Finally, the reason why the bottom part of Fig. 7-6a and Fig. 7-6b (ACIFC results) seems to be cut is due to a selected attenuation value in the EMC analyzer different from 0 dB.

Tab 7.2 provides the amplitude value (in dB μ V) of the first three spectral lines comparing the results obtained for the three investigated topologies operated in nominal conditions.

Table 7.2: Summary of EMI results obtained for the three topologies

Conducted Emission on V_g *	ACISC	ACIFC	Flyback	
Amplitude of the 1 st spectral line	76.9	85.6	65.8	dB μ V
Amplitude of the 2 nd spectral line	56.6	69.2	37.7	dB μ V
Amplitude of the 3 rd spectral line	52.8	61.5	37.2	dB μ V
Reference figure	Fig. 7-5a	Fig. 7-6a	Fig. 7-7a	
Type of switches	GaN	GaN	Si	
Operating mode	(RESONANT DCM)		(CCM)	
Switching frequency f_s	2	2	0.4	MHz

* The results are obtained in nominal conditions ($V_g = V_o = 12$ V, $I_o = 600$ mA), and “Conducted Emission on V_g ” is referred to the peak value of a given spectral line.

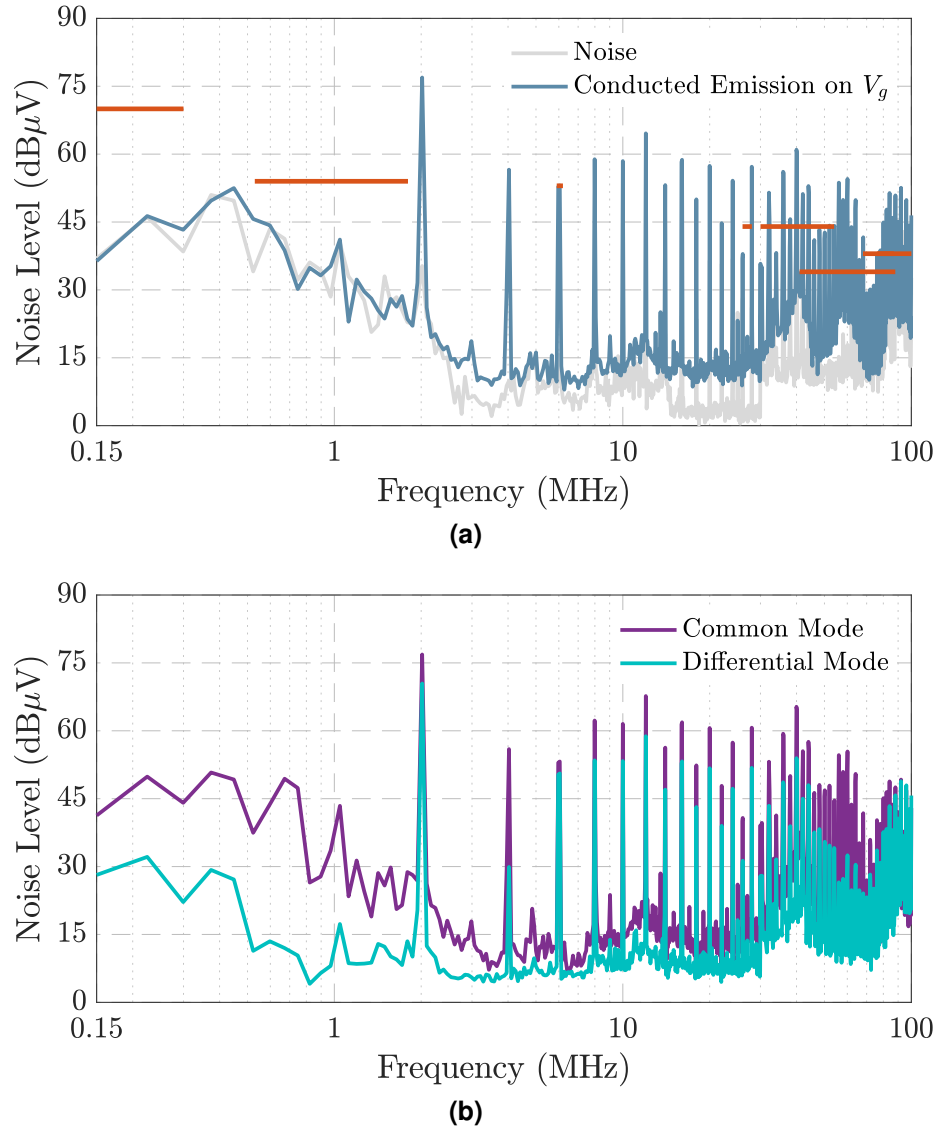


Figure 7-5: EMI results obtained for the 2 MHz ACISC operated in nominal conditions *with* a resonant DCM operation: (a) conducted emission, and (b) input CM and DM conducted noise measured at the input (power supply V_g) using a noise separator and a LISN. EMI limits (CISPR 25, Class 5, *Peak* detector), highlighted here in red, are reported in Tab 7.1.

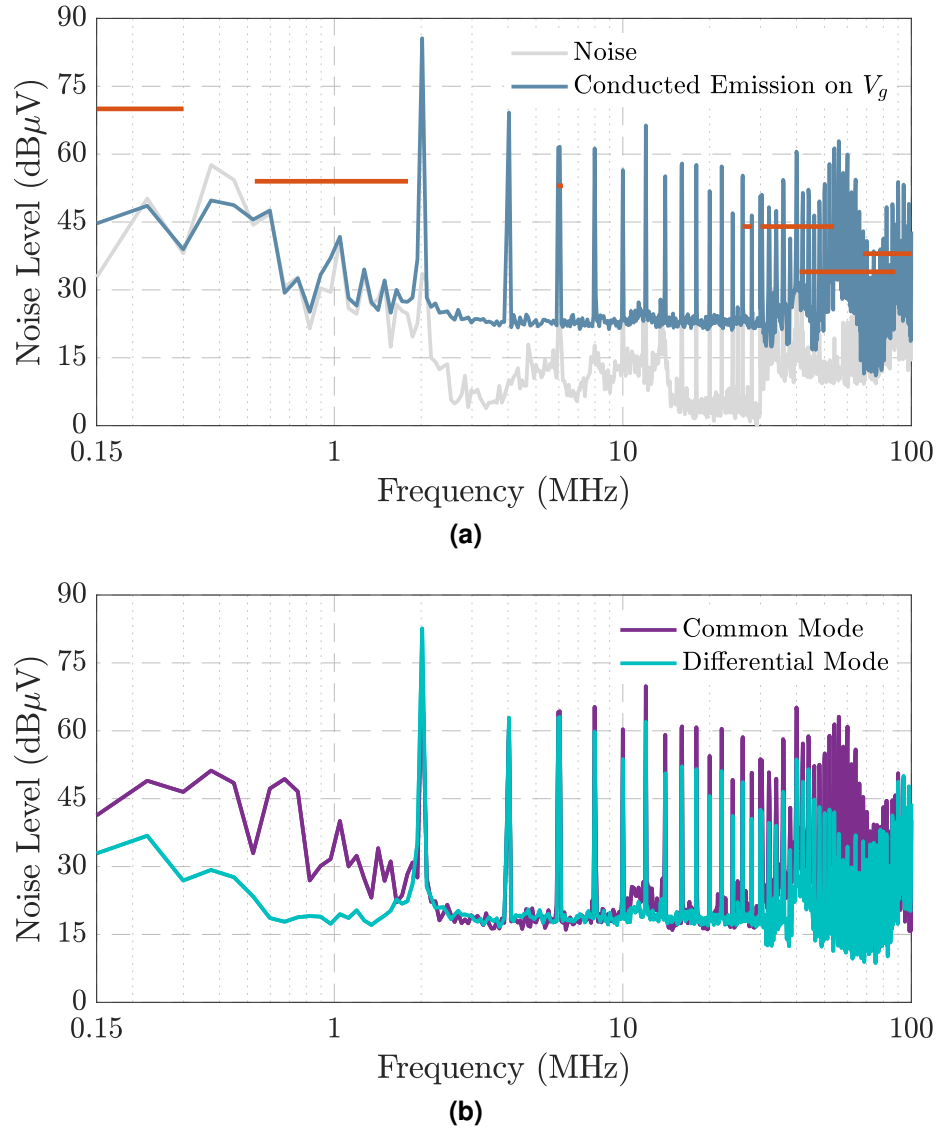


Figure 7-6: EMI results obtained for the 2 MHz ACIFC operated in nominal conditions *with* a resonant DCM operation: (a) conducted emission, and (b) input CM and DM conducted noise measured at the input (power supply V_g) using a noise separator and a LISN. EMI limits (CISPR 25, Class 5, *Peak* detector), highlighted here in red, are reported in Tab 7.1.

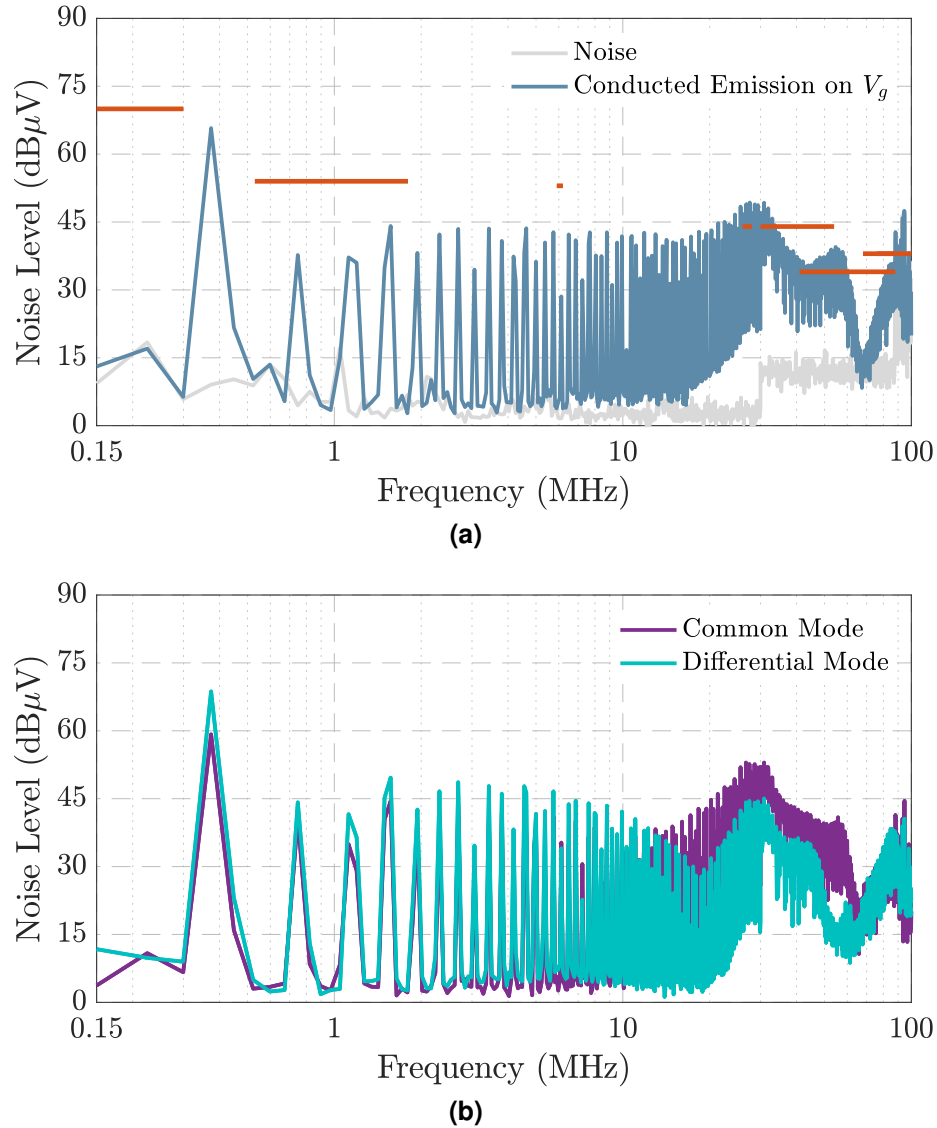


Figure 7-7: EMI results obtained for the 400 kHz commercial flyback converter operated in nominal conditions *with* a CCM operation: (a) conducted emission, and (b) input CM and DM conducted noise measured at the input (power supply V_g) using a noise separator and a LISN. EMI limits (CISPR 25, Class 5, *Peak* detector), highlighted here in red, are reported in Tab 7.1.

7.2.2 Temperature Analysis

Fig. 7-8 shows the thermal images comparison between the 2 MHz GaN-based SEPIC converter with active clamp (ACISC) and the 400 kHz Si-based commercial flyback converter. Such images, taken in nominal conditions ($V_g = V_o = 12\text{ V}$, $I_o = 600\text{ mA}$) approximately 20 minutes after the converters are turned-ON, reveal almost 27°C less in the eGaN[®] switches and 8°C less in the transformer, compared with the corresponding components in the commercial flyback converter.

Tab 7.3 summarizes the temperature results obtained for the three topologies in nominal operating conditions. Once the 2 MHz GaN-based topologies are operated in ZVS resonant DCM operation, the results prove that the ACISC is better than the ACIFC topology in

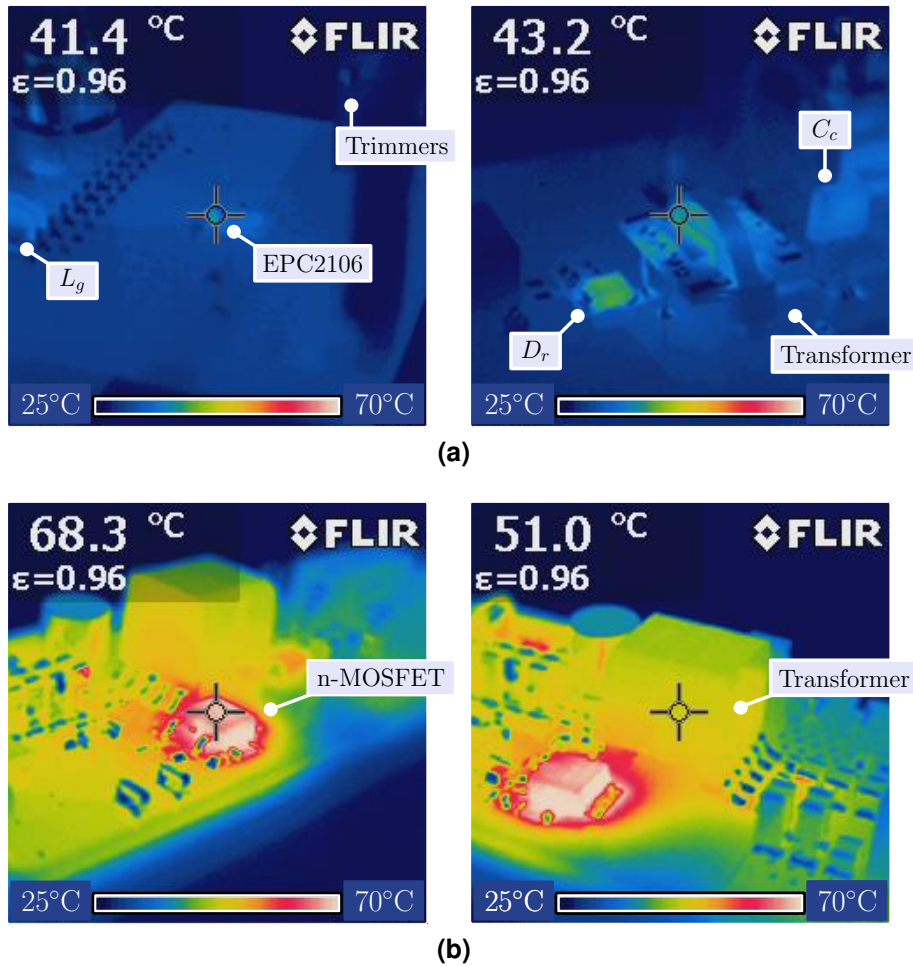


Figure 7-8: Measured temperature of transformer and switches, in nominal conditions, of: (a) the designed 2 MHz ACISC (with transformer T_1); (b) the 400 kHz commercial flyback converter.

Table 7.3: Summary of temperature results obtained for the three topologies

Temperature*	ACISC	ACIFC	Flyback	
Switches	41.4	57.5	68.3	°C
Transformer	43.2	56.0	51.0	°C
Type of switches	GaN	GaN	Si	
Operating mode	(RESONANT DCM)		(CCM)	
Switching frequency f_s	2	2	0.4	MHz

* Temperature results are obtained in nominal conditions ($V_g = V_o = 12\text{ V}$, $I_o = 600\text{ mA}$).

terms of overall temperature in the main components ($\sim -15^\circ\text{C}$). As specified in the disadvantages of the ACIFC (section 6.3), this big difference is due to a higher current flowing in the transformer primary winding and switches.

Chapter 8

Conclusions

A complete and exhaustive comparative analysis of 48 V-based low-power architectures for automotive applications is made while a system-level efficiency, cost, and size are assessed in the framework of a trade-off analysis. A novel architecture enumeration methodology – called constrained bucking trees (CBT) – is first proposed which follows a tree-like approach and yields a substantial reduction in the number of possible configurations. Next, candidate solutions are ranked in terms of efficiency, total footprint area and cost showing which is the best solution for the considered metrics. The possibility of including highly efficient dedicated dc-dc units for high step-down (HSD) conversion as well as switched-capacitor (SC) stages providing a fixed conversion ratio is explored. Adoption of such dedicated solutions leads to overall system-level efficiency improvement justifying the proposed study. The use of HSD converters, which act as substitutes for the less efficient Buck topology, entails a more relaxed efficiency requirement than for SC solutions, which introduce one additional conversion stage in the architecture. On the other hand, currently limited commercial availability of optimized and highly integrated solutions for HSD or SC conversion within the application power range makes the above solutions still poorly competitive against traditional designs.

Next, the analysis, design and experimental verification of a 2 MHz, 12 V, 600 mA GaN-based active-clamped isolated SEPIC converter (ACISC) operating in resonant discontinuous conduction mode (DCM) and intended for low-power automotive applications is addressed. The chosen converter operating mode, coupled with the proposed design

methodology and high switching rate, guarantees zero-voltage switching (ZVS) throughout the intended operating range and leads to reduced magnetic size and overall footprint. A design procedure for the converter is first proposed which enables the designer to trade-off the input inductance L_g and the magnetizing inductance L_{me} while minimizing the total switch conduction losses. The design details for the high-frequency transformer, realized here as a planar structure, and input inductor, are then outlined.

A complete power loss breakdown analysis is reported for the ACISC with the purpose of identifying the main loss sources and estimating their relative contributions. The study reveals that the largest contribution is associated with the transformer, and in particular with primary winding losses to be attributed to *skin* and *proximity* effects in the MHz range. This aspect leads to the next step of the study, in which the magnetics involved in the converter are improved via a step-by-step optimization technique showing a significant improvement in terms of efficiency profile and in-circuit noise for the designed ACISC.

Performance comparison in terms of efficiency, temperature in the main components, electromagnetic interference (EMI) noise, and devices' stresses is carried out between the designed 2 MHz GaN-based ACISC, a 2 MHz GaN-based topology named active-clamped isolated flyback converter (ACIFC), and a 400 kHz commercial flyback. Experimental results confirm full ZVS operation in nominal conditions of the GaN-based topologies operated in resonant DCM and a better performance from the ACISC topology.

The peak efficiency of the optimized ACISC operating in nominal condition at full load is 89.2 %, approximately 9 % higher than the efficiency of a commercial 400 kHz flyback converter designed for the same input/output voltages and output current rating.

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Appendix A

Correlation Between the Number of CBT and the Tartaglia-Pascal's Triangle

Considering a low-power battery-connected architecture having

- 1 input voltage
- n intermediate or *bus* voltages
- m POL voltages

the number of voltages involved in the architecture is:

$$1 + n + m.$$

Plain application of the bucking trees (BT) method to the $n + m$ voltages would yield $N_{BT} = (m + n)!$ possible configurations (trees) for the considered architecture [21,22]. The proposed CBT method reduces the number of available candidates to just $2^m - 1$, when $n = 1$. This is because, starting from the N_{BT} possible trees, one should only consider those configurations in which the desired output voltages appear as leaf nodes (POL voltages) and not as intermediate bus voltages. By associating a given voltage value with one of the $1 + n + m$ cells of a permutation, the input voltage will always be placed in the first cell. Fig. A-1 shows an example of a single-battery architecture having $V_{in} = 48\text{ V}$, a

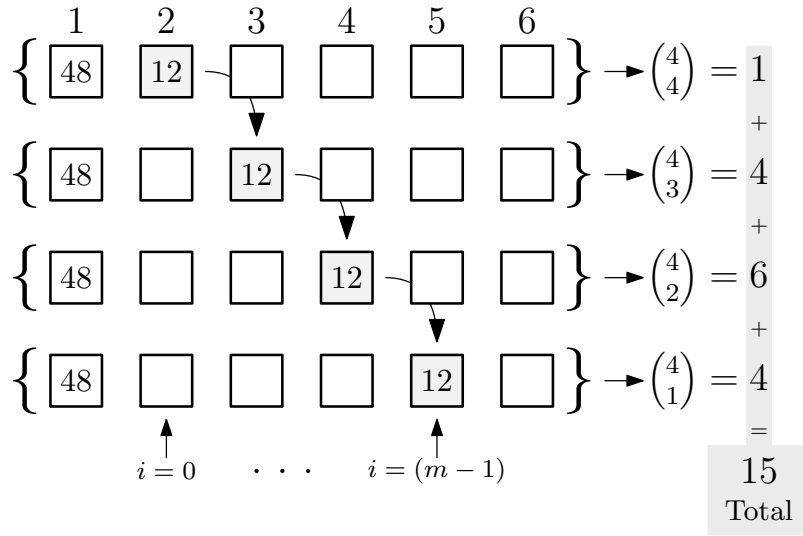


Figure A-1: Structure of the 15 valid permutations corresponding to one input voltage (48 V), one bus voltage (12 V), and $m = 4$ point-of-load voltages (blank cells).

single bus voltage equal to 12 V, and $m = 4$ POL voltages. As it can be seen from the figure, the intermediate voltage can be placed between the second cell and the penultimate cell. The latter can never be placed in the last cell because, in that case, it would become an output voltage and this is not allowed in the CBT method. By associating the index $i = 0$ to the first cell in which the intermediate voltage can be placed (second cell) and the index $i = m - 1$ to the last possible one (penultimate cell), the formula used to calculate the number of available candidates in the CBT method can be demonstrated as follow. According to the binomial formula

$$\sum_{i=0}^m \binom{m}{i} = (1 + 1)^m = 2^m \quad (\text{A.1})$$

and considering that

$$\binom{m}{i} = \frac{m!}{i!(m-i)!} = \frac{m!}{(m-i)![m-(m-i)]!} = \binom{m}{m-i} \quad (\text{A.2})$$

the number N_{CBT} of possible configurations for a given architecture having $n = 1$ intermediate voltage is

$$N_{CBT} = \sum_{i=0}^m \binom{m}{m-i} - 1 = \sum_{i=0}^m \binom{m}{i} - 1 = 2^m - 1 \quad (\text{A.3})$$

For example, when $n = 1$ and $m = 4$ there are 15 possible configurations for the architecture under investigation, as shown in Fig. A-1.

This result can be obtained by applying the formula or, in a much simpler way, by observing the fourth row of the Tartaglia-Pascal's triangle shown in Fig. A-2 ($m = 4$). The elements shown in the rows of the Tartaglia-Pascal's triangle represent the number of valid configurations for a given architecture by moving the single intermediate voltage value from the first available cell (second cell) to the last possible one (penultimate cell). Fig. A-1 is referred to the fourth row of the Tartaglia-Pascal's triangle shown in Fig. A-2. The demonstration shown in this appendix is based on the fact that each element reported in the m -th row of the Tartaglia-Pascal's triangle can be obtained using the formula of the binomial coefficient.

The sum of the elements shown in the m -th row of the Tartaglia-Pascal's triangle (excluding the rightmost one) provides the total number N_{CBT} of valid configurations for a single-battery architecture having m POL voltages and $n = 1$ intermediate voltage.

POL voltages									N_{CBT}
$m = 1$	1 st row	1	1						1
$m = 2$		1	2	1					3
$m = 3$		1	3	3	1				7
$m = 4$		1	4	6	4	1			15
$m = 5$		1	5	10	10	5	1		31
$m = 6$		1	6	15	20	15	6	1	63
$m = 7$	7 th row	1	7	21	35	35	21	7	127
$\vdots$		$i = 0$					$i = (m - 1)$		$\vdots$

Figure A-2: Tartaglia-Pascal's triangle used to find the total number N_{CBT} of possible configurations for a given single-battery architecture having $n = 1$ bus voltage

Appendix B

CBT Method: Generation and Enumeration of the Trees

B.1 Matlab Code

```
1 % *****
2 % Matlab script used to generate and enumerate all valid permutations
3 % Reference: 'Generalization of the CBT Method' (Section 2.4, Ch. 2)
4 % *****
5
6 % Run the Matlab code and open myTextFile.txt to see the results
7
8 clear all;
9 clc;
10
11 % Enter the input voltage of the battery-connected architecture
12 inputVoltage = 48;
13
14 % Enter the n intermediate voltages (in descending order)
15 intermediateVoltages = [24 12];
```

```
16 % Enter the m output voltages (in ascending order)
17 outputVoltages = [1 1.3 3.3 5];
18
19 n = length(intermediateVoltages);
20 m = length(outputVoltages);
21
22 % Inizialization of key variables used in the script
23 permutation = zeros(1, n+m+1);
24 counter = 0;
25 a = [];
26 b = [];
27 c = [];
28 var1 = 0;
29 var2 = 0;
30 N_valid_trees = 0;
31
32 % Text file is here opened
33 TextFile = fopen('myTextFile.txt','w');
34 N_CBT = ValidTrees(n, m, N_valid_trees, var1, var2);
35
36 fprintf(TextFile, '***** \n');
37 fprintf(TextFile, 'Constrained Bucking Trees (CBT) Method \n');
38 fprintf(TextFile, '***** \n\n');
39 fprintf(TextFile, 'The architecture has: \n');
40 fprintf(TextFile, '\b\b 1 input voltage \n');
41 fprintf(TextFile, '\b\b %d intermediate voltages \n', n);
42 fprintf(TextFile, '\b\b %d point-of-load voltages \n\n', m);
43 fprintf(TextFile, 'The number of valid trees is: %d\n', N_CBT);
44 fprintf(TextFile, '***** \n\n');
45
```

```

46 %% MAIN
47 % *****
48 % Print the total number of valid trees (Ncbt) in myTextFile.txt, and
49 % provide the structure of permutations which give rise to each tree.
50 % *****
51
52 permutation(1) = inputVoltage;
53
54 if n ~= 0 || m ~= 0
55     PlaceIntermediateVoltages(1, permutation, intermediateVoltages,
56         outputVoltages, counter, n, m, TextFile);
57
58 % Text file is here closed
59 fclose(TextFile);
60
61 %% RECURSIVE FUNCTIONS CALLED IN 'MAIN'
62
63 % — FUNCTION 1 —
64 % *****
65 % This function is used to insert the n intermediate voltages within
66 % the permutations in all possible modes which are considered valid.
67 % *****
68
69 function counter = PlaceIntermediateVoltages(j, permutation,
70     intermediateVoltages, outputVoltages, counter, n, m, TextFile)
71     % once all the n intermediate voltages are inserted within a given
72     % permutation (if j>n), the PlaceOutputVoltages() function is
73     % called to fill the permutation with the output voltages in all
74     % the ways which are considered valid

```

```
74     if j > n
75         counter = PlaceOutputVoltages(1, permutation, outputVoltages,
            counter, n, m, TextFile);
76     else
77         for i = 2 : 1 : (1+n+m)-1 % permutation_length-1
78             if permutation(i) == 0 && permutation(i+1) == 0
79                 permutation_new = permutation;
80                 permutation_new(i) = intermediateVoltages(j);
81                 counter = PlaceIntermediateVoltages(j+1,
            permutation_new, intermediateVoltages,
            outputVoltages, counter, n, m, TextFile);
82             end
83         end
84     end
85 end
86
87 % — FUNCTION 2 —
88 % *****
89 % This function is used to insert the m ouput voltages within the
90 % permutation in all possible modes which are considered valid.
91 % *****
92
93 function counter = PlaceOutputVoltages(j, permutation, outputVoltages,
    counter, n, m, TextFile)
94     if j > m
95         % here the permutation is printed in in myTextFile.txt
96         counter = counter + 1;
97         fprintf(TextFile, '{ \b \b');
98         for i = 1 : 1 : length(permutation)
99             fprintf(TextFile, '%g \b \b', permutation(i));
```

```

100         end
101         fprintf(TextFile,'} \b \b %d \n', counter);
102     else
103         for i = 2 : 1 : (1+n+m) % permutation_length
104             if permutation(i) == 0 && permutation(i-1) ~= 0
105                 permutation_new = permutation;
106                 permutation_new(i) = outputVoltages(j);
107                 counter = PlaceOutputVoltages(j+1, permutation_new,
108                     outputVoltages, counter, n, m, TextFile);
109             end
110         end
111     end
112
113 % — FUNCTION 3 —
114 % *****
115 % This function is used to calculate the number of N_CBT valid trees
116 % to prove the correctness of Eq.(2.13) given in Chapter 2.
117 % *****
118
119 function formula = ValidTrees(n, m, N_valid_trees, var1, var2)
120
121 if n>=0 && m>=0
122     if n == 0 && m >= 1
123         N_valid_trees = 1;
124     else
125         for k = 1 : 1 : min(n,m)
126             for j = 1 : 1 : k-1
127                 var1 = var1 + a(j)*nchoosek(k,j);
128                 var2 = var2 + b(j)*nchoosek(k+1,j+1);

```

```
129         end
130         var2 = var2 + 1*nchoosek(k+1,1); % b0=1
131         a(k) = k^n - var1;
132         b(k) = (k+1)^m - var2;
133         if k-1 == 0
134             N_valid_trees = N_valid_trees + a(k)*(b(k)+1); % b0=1
135         else
136             N_valid_trees = N_valid_trees + a(k)*(b(k)+b(k-1));
137         end
138         var1 = 0;
139         var2 = 0;
140     end
141 end
142 end
143
144 formula = N_valid_trees;
145
146 end
```

B.2 Example of a Result Obtained From the Matlab Code

Fig. B-1 shows an example of the output coming from the Matlab code reported in Sec. B.1. In this case, a single-battery architecture having

- one input voltage $\hookrightarrow$ inputVoltage = 48
- two intermediate voltages $\hookrightarrow$ intermediateVoltages = [24 12]
- four POL voltages $\hookrightarrow$ outputVoltages = [1 1.3 3.3 5]

is considered. As reported in Fig. B-1, the architecture under investigation has 115 possible configurations – which are listed here as permutations – once the CBT method is applied.

APPENDIX B. CBT METHOD: GENERATION AND ENUMERATION OF THE TREES

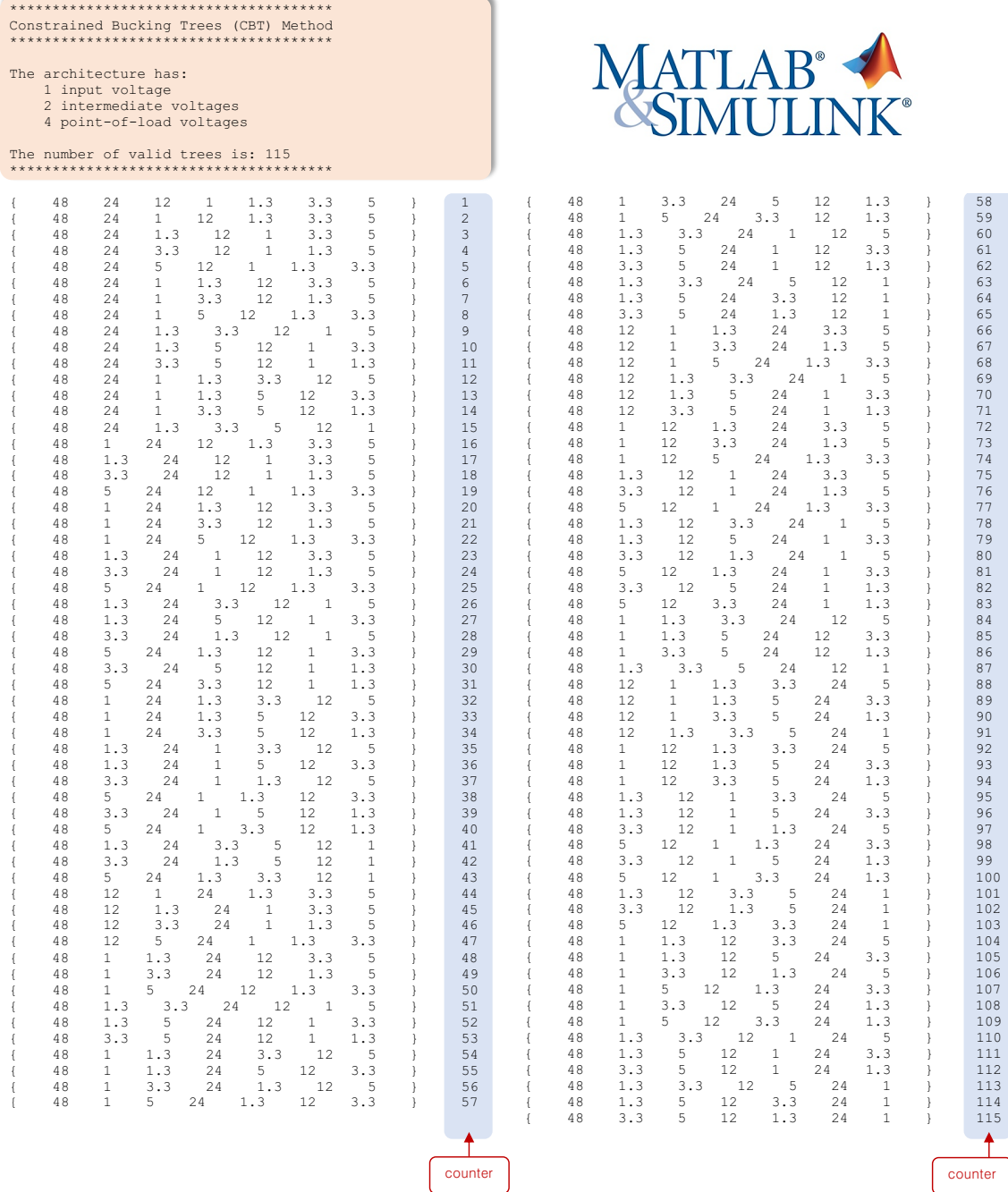


Figure B-1: Output of the Matlab code reported in section B.1 when inputVoltage = 48, intermediateVoltages = [24 12], and outputVoltages = [1 1.3 3.3 5]

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