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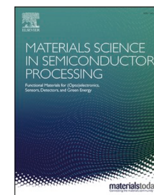

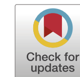

Origin and Recovery of Negative V_{TH} Shift on 4H–SiC MOS Capacitors: An Analysis Based on Inverse Laplace Transform and Temperature-Dependent Measurements

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A B S T R A C T

SiC power MOSFETs are reported to suffer from both positive and negative threshold voltage shifts. Positive shift is well understood in the literature and attributed to electron trapping in near interface oxide traps (NIOTs). Negative shift is explained by hole generation and trapping in the oxide via impact ionization favored by the strong oxide field. However, studies on negative shift are still ongoing, and the origin and nature of the process are not fully understood. This study advances the comprehension of negative threshold voltage shift by investigating MOS capacitors subject to positive bias stress.

We demonstrate that: a) a significant negative threshold shift is observed when the electric field is greater than 7.5 MV/cm; b) the detected shift is not recoverable at zero bias. Recovery can be obtained only by applying a positive gate voltage indicating a field-driven detrapping process. c) Trap-state mapping measurements were carried out to extract the activation energy of the detrapping processes, and a weak thermal activation was observed.

Results collected within this paper indicate that holes are trapped at deep centers, and thermal detrapping is not possible. Hole release is only possible when a high field is applied to the insulator, possibly due to the recombination between leaking electrons and trapped holes.

1. Introduction

Silicon carbide (SiC) power MOSFETs are considered a promising alternative to silicon-based IGBTs for high power applications. SiC is a wide bandgap material (3.26 eV) with very good physical properties for power devices. Its high thermal conductivity enables high temperature operation and allows for more efficient cooling. High bulk mobility reduces on-resistance of devices, thus decreasing conduction losses in SiC-based power converters. Finally, the high critical electric field enables the creation of small devices that can withstand very high voltages, further reducing the on-state resistance [1–4].

To unleash the full potential of such devices, their reliability needs to be improved: a relevant research challenge is the minimization of charge trapping in the oxide or at the semiconductor-oxide interface, under a gate bias stress. Different contributions analyze oxide and interface related traps, including the effects of different nitridation techniques [5–7].

An important consequence of such trapping is a threshold voltage (V_{TH}) shift, specifically under positive gate bias, where an nMOS device is turned on. Several reports [8–10] show a little positive shift under positive bias, modeled with electron trapping in oxide border traps [11]. Some results [12,13], however, also show the presence of a negative shift. At high stress fields, holes may be generated via impact ionization in the oxide, and be subsequently trapped in the oxide, yielding to a negative V_{TH} shift. This shift is particularly detrimental, because it can make it impossible to turn off a device when lowering the gate bias.

In spite of its importance, this phenomenon is still subject of intense research, and its nature has not yet been fully understood. Literature reports of negative V_{TH} shift phenomena exist, but they are mostly related to a negative bias stress [14,15]. This paper substantially advances the comprehension of such negative V_{TH} shift by studying the detrapping processes responsible for hole release after stress tests carried out at high gate bias.

The study was performed on planar 4H–SiC MOS capacitors to obtain a uniform electric field distribution, but the results are meant to show insights on MOSFETs reliability-limiting mechanisms. MOS capacitors are used as test structure to simplify the analysis, and the modeling, thanks to the more uniform electric field compared to MOSFET

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structures. The collected results demonstrate that hole trapping leads to a significant threshold voltage shift that can be recovered only under positive gate bias. On the other hand, the hole release process is weakly thermally activated. The results are interpreted by considering that holes are trapped at deep states; detrapping occurs via a trap-to-trap leakage and is favored at positive gate voltages.

2. Devices and Measurement Techniques

This study focuses on 4H–SiC n-epi vertical MOS capacitors (MOS Caps). Due to their simpler structure with respect to MOSFETs, they show a more uniform electric field across the oxide and are therefore easier to study. Since the ultimate focus of this study is the investigation of trapping phenomena related to electron injection from the channel to the oxide, the use of n-epi MOS capacitors is justified.

The analyzed devices are vertical and have a 40 nm thick SiO_2 thermally grown gate oxide with NO post-oxidation anneal. Gate is n-type poly-Si.

To characterize the V_{TH} shift induced by stress, a measurement-stress-measurement (MSM) scheme is applied, consisting of a constant gate voltage stress and a subsequent recovery phase under different bias conditions. Recovery is started right after the stress, with instrument-limited delay of a few nanoseconds.

A difference between this work and the studies of V_{TH} shift from the literature, described in the introduction, is the monitoring technique applied during stress and recovery. Conventionally, in fact, MOSFETs are used, thus V_{TH} can be measured from I_DV_G curves, by using a setup for BTI testing. For studying MOS capacitors, we defined a setup for fast (ms range) capacitance-voltage measurements [16,17]. The analysis the CV curves of MOS capacitors has the advantage of providing both a direct estimate of the trapped charge (from the integral of the CV hysteresis) and a quick evaluation of the flatband voltage (V_{FB}) shift that is related to V_{TH} according to Eq. (1) [18].

$$V_{TH} = V_{FB} + V_C + 2|\Phi_p| + \frac{1}{C_{OX}}\sqrt{2\varepsilon_s q N_A (2|\Phi_p| + V_C - V_B)} \qquad \text{Eq. 1}$$

A schematic drawing of the waveforms used for measuring the fast CV curves is reported in Fig. 1c. To ensure a very fast measurement, a single voltage waveform for stress and measurement sweep is generated and provided to a precise capacitance meter. Its analog readout is fed into an oscilloscope, triggered by the measurement voltage sweep. Data are extracted and a LOcally WEighted Scatterplot Smoothing (LOWESS) algorithm is used to filter out measurement noise.

The charge trapped and detrapped between two measurement points is determined by integrating the difference between the corresponding CV curves, while the flatband voltage V_{FB} is estimated by considering the voltage at which the measured capacitance is equal to 80% of the oxide capacitance.

3. Stress - Negative V_{TH} Shift

The first step of this analysis evaluates the flatband voltage V_{FB} variation under a constant gate voltage stress. V_{FB} is then estimated from CV curves measured with the fast approach.

Results of stress tests carried out at different voltages indicated that a negative threshold voltage shift is visible only when the stress field is greater than 8.75 MV/cm, corresponding to a voltage of 35 V (Fig. 2). Such field is needed in order to initiate impact ionization in the oxide with consequent hole generation.

For the subsequent stress and recovery tests, a stress gate voltage of 35 V has been chosen (corresponding to a field of 8.75 MV/cm). The choice of stress voltage was supported by several measurements performed at different gate voltages (not shown) and by the results visible in Ref. [19]. For simplicity, oxide field has been calculated (in a first order approximation) as $E_{OX} = V_G/_{t_{OX}}$ [19].

In the V_{FB} transient curves visible in Fig. 3 for different samples, two regimes can be observed: a first slight increase with time and a strong decrease taking place after 0.1–1 s of stress. This behavior is consistent with what observed in MOSFETs in recent studies [19], and confirms the equivalent behavior of MOS Caps and MOSFETs under the same stress conditions.

The slight positive shift is ascribed to electron trapping at oxide border traps or near-interface oxide traps (NIOTs) [8–10]. This is supported by the rate equation models described in Ref. [19], where the

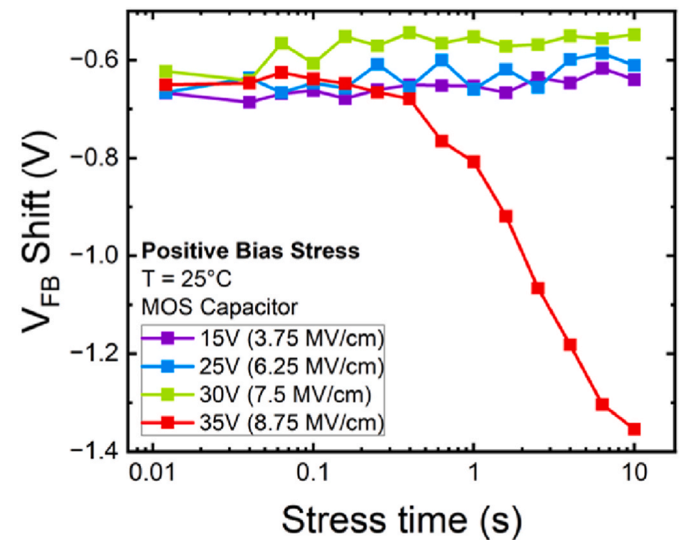

Fig. 2. V_{FB} shift curves during a 10 s positive bias stress at different bias voltages performed on different samples.

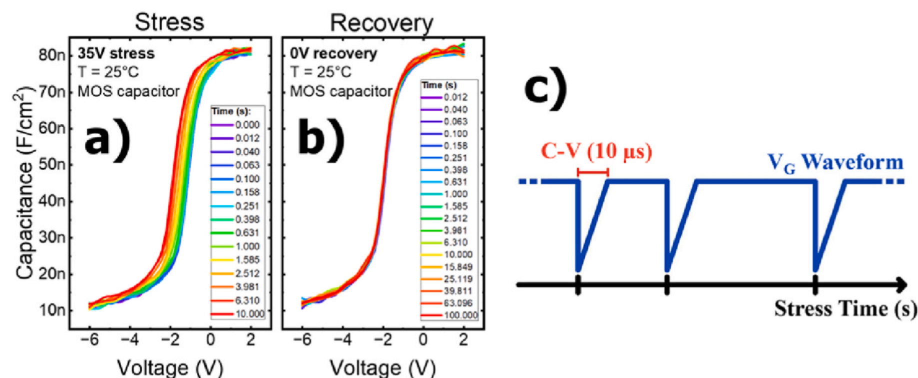

Fig. 1. Measured C–V curves during a) stress and b) recovery. Fast C–V gate voltage waveform is shown in c).

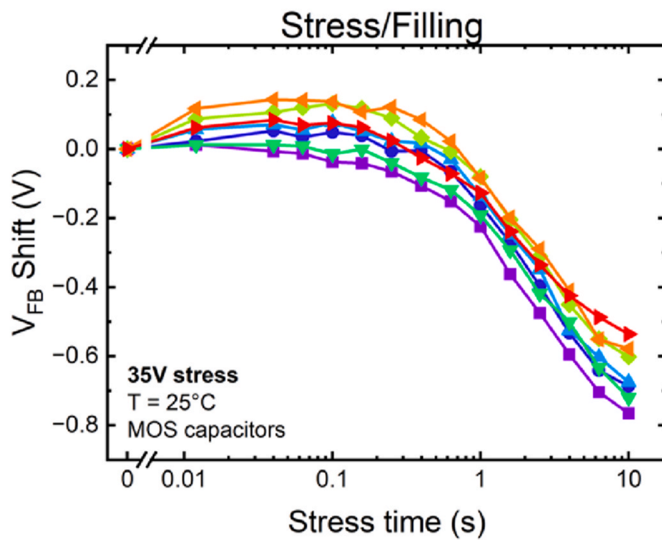

Fig. 3. V_{FB} shift curves for different samples during a 10 s positive bias stress at 35 V. Difference between curves attributed to differences among different samples. Initial V_{FB} increase is very little and sometimes masked by the subsequent negative shift.

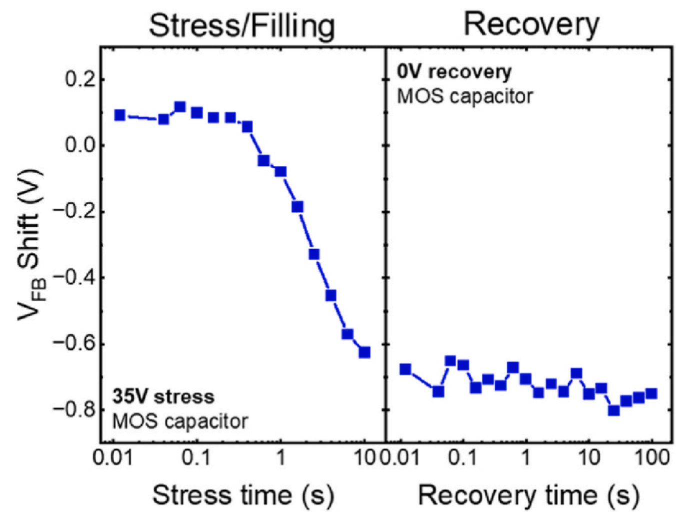

Fig. 4. V_{FB} transient for a stress and recovery experiment. Recovery was performed at 0 V and no device recovery is observed.

logarithmic positive V_{TH} shift is modeled with the inhibition model.

The observed negative shift follows a single exponential trend and is ascribed to hole trapping in the gate oxide [13,20]. Such holes are considered to be generated within the gate oxide as a consequence of the stress bias: electrons injected from the semiconductor side are accelerated and undergo impact ionization in the gate oxide generating holes [21]. Holes are therefore generated within the oxide itself, so hole trapping takes place even in presence of a n-type epi.

The field across the oxide in the chosen stress condition, is equal to 8.75 MV/cm, comparable to threshold fields found in literature for hole generation in SiO_2, like in Masin et al. [19] (8 MV/cm), T. Liu et al. [22] (8.5 MV/cm), Y. Zheng et al. [23] and Di Maria et al. [21] (7 MV/cm) [24–26].

In the analyses shown before, holes were assumed to be trapped in the oxide, and not at the interface. Interface trapping can be excluded by observing the CV curves during stress (Fig. 1a). Only a rigid shift is observed, that clearly relates to oxide trapping. No change in the slope of the curves is visible: thus, interface trapping can be excluded, and holes are trapped in the oxide layer.

4. Recovery

In prior literature reports [14,27], recovery was investigated after low positive bias stress, so in absence of substantial hole trapping. In Ref. [14], recovery after negative V_{TH} shift is shown, however such shift was induced by a negative bias stress. To investigate the action of a positive bias stress with hole generation and trapping, a matrix of experiments has been defined, involving different biases and temperatures. As a preliminary test, stressed samples have been left for some time at a 0 V gate bias to observe if any detrapping occurs naturally at room temperature. As can be seen in Fig. 4, no recovery occurs with just zero bias. This result provides also information on the recoverability of trapping phenomena. Since the trapped charge is not spontaneously detrapped, we can assume the charge trapping process as non-reversible.

Another test considered the application of different negative voltages to the oxide. This would aid a detrapping of holes towards the gate via trap-assisted tunnelling or along the valence band, without promoting further electron trapping. However, as visible in Fig. 5, no recovery occurs. V_{FB} shifts increases towards the negative voltage side, probably indicating a detrapping of the electrons previously trapped at oxide border traps.

To induce recovery, another strategy is to shine light on the samples. Photons are in fact able to transfer energy to the trapped carriers and favor their detrapping. As reported in Fig. 6, no recovery is shown. Light used in this study ranges from 500 nm (2.48 eV) to 280 nm (4.43 eV), so from the visible range to UV-C high energy light. Driving current for the LEDs used is adjusted so that each LED emits the same photon flux. Again, a further negative shift appears, probably related to light-induced detrapping of electrons from border traps (note that light may be partially shaded by the thick metal contacts on the top of the devices).

The only strategy found to induce recovery is to apply a positive bias to the oxide, lower than the threshold for impact ionization and hole generation. Several positive biases have been tested, and a partial recovery of the negative shift is observed even at the lowest biases (field-driven detrapping, see Fig. 8), as in Fig. 7 (5.6 MV/cm).

In the following experiments, the chosen recovery voltage is 30 V, corresponding to 7.5 MV/cm. Such voltage, which is below the threshold for impact ionization, is able to bring the devices to a complete recovery of negative V_{FB} shift in 1000 s.

After identifying stress and recovery voltages able to cause a negative shift during stress (35 V) and fully recover it afterwards (30 V), the stress-recovery experiment was repeated at different temperatures, with the aim of observing how the V_{FB} shift trend under stress and how the recovery trend change with different temperatures. The results are shown in Fig. 9 and two considerations can be made: during stress, the negative shift magnitude decreases with increasing temperature, while maintaining the same trend shape. This is compatible with hole generation and trapping via impact ionization, because at higher temperatures the mean free path is shorter and the probability of impact ionization is lower.

At the same time, the recovery transients show that recovery is possible and complete at every temperature. Moreover, it should be noted that the trapping time constants around 1 s visible in the stress transients (Fig. 9a), and the detrapping time constants (around 100 s (Fig. 9b) are temperature-independent.

A recovery process, such as the one studied here, is made by the superimposition of different single exponential transients, each one corresponding to the detrapping of a single trap level. The first option to properly fit such transients is to use a sum of exponentials. However, since the detrapping involves a distribution of levels, this solution only yields approximate results. To solve this problem, we fitted the transients via a stretched exponential function. Such function is equivalent to an infinite sum of single exponential transients (Eq. (2)), with a distribution of time constants [28].

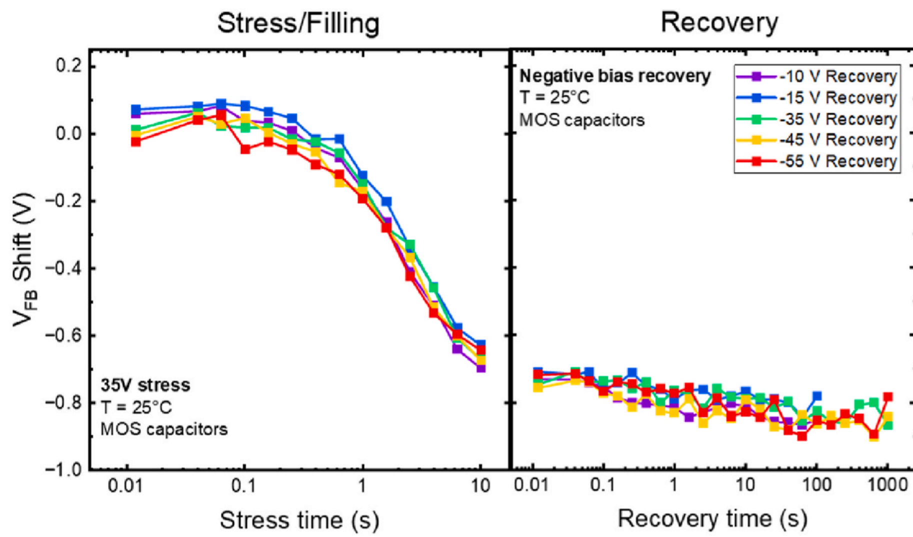

Fig. 5. V_{FB} transient for a stress and recovery experiment. Recovery was performed at different negative gate voltages and no device recovery is observed.

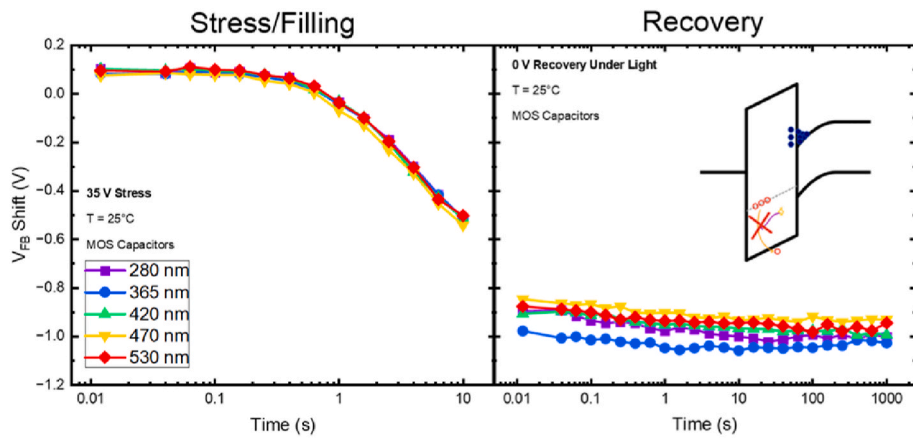

Fig. 6. V_{FB} transient for a stress and recovery experiment. Recovery was performed at 0 V under light at different wavelengths, and no device recovery was observed. Inset represents band diagram for hole release under light.

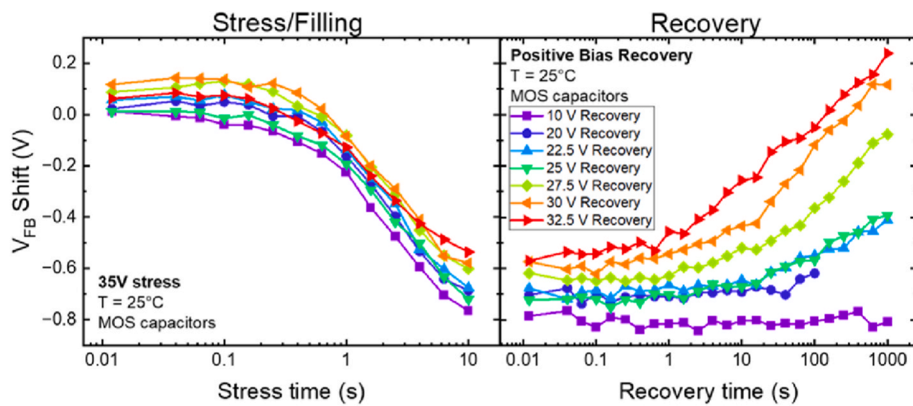

Fig. 7. V_{FB} transient for a stress and recovery experiment. Recovery was performed at different positive gate biases. Device recovery is observed even with a low bias.

$$\sum_{i=1}^{\infty} A_i e^{-\frac{t}{\tau_i}} \approx \int_0^{\infty} f(\tau) exp\left(-\frac{t}{\tau}\right) d\tau \approx A\ exp\left(-\left(\frac{t}{\tau_0}\right)^{\beta}\right) \quad \text{Eq. 2}$$

A set of parameters, namely A, β and τ_0 was extracted for each temperature, and they were used as inputs for the Trap State Mapping algorithm [29], as described in detail in the Appendix to obtain in the end the activation energy distribution of the detrapping time constants.

As a last consideration, to analyze the contribution of holes exclusively, we need to subtract the electron trapping component occurring during recovery and due to the high gate bias (30 V) needed for hole detrapping. To do this, along with the stress and recovery measurements, some identical samples were stressed at 30 V for 1000 s, at each

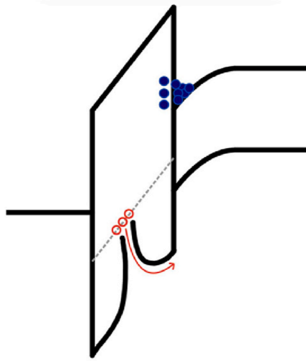

Fig. 8. Band diagram for the hole release process under a strong positive gate bias.

of the stress temperatures, thus applying the same procedure used as recovery. The obtained V_{FB} shift was subtracted from the V_{FB} shift measured during recovery on stressed samples and the resulting transients are visible in Fig. 9, and take into account exclusively the contribution of trapped holes.

5. Discussion

The distribution of activation energies of the hole detrapping process obtained by trap state mapping [29] is shown in Fig. 10. A narrow peak centered at 0.02 eV was extracted. This demonstrates that the detrapping process is weakly thermally activated. The extracted activation energies do not indicate that holes are trapped at shallow traps: in fact, detrapping does not occur at room temperature, suggesting the involvement of deep traps.

One explanation that is able to conciliate the measurement results with the estimated spectrum is to consider that holes are trapped at deep defects, and cannot be removed thermally. Detrapping is only possible at high positive bias through a trap-assisted leakage process (see Fig. 11), like the one described in Ref. [30]. Such a process cannot be considered as a pure emission one, so the activation energy determined experimentally is non-physical. It can be interpreted as the trap-to-trap energy difference of the trap-assisted process responsible for the hole release.

This interpretation is consistent with holes trapped deep in energy and explains why a) the process is weakly thermally activated, and b) only a strong field is able to detrap the holes.

A possible issue with this explanation is related to the absence of detrapping under strong negative bias (see Fig. 5). The trap-assisted hole leakage process should in fact have a symmetrical behavior with respect to the field, at least to some extent, which is not observed.

To explain this absence of symmetry, the following aspects should be considered: a) trap-assisted processes depend on the local trap concentration, which may be larger towards the interface; b) when a negative voltage is applied to the gate, the semiconductor is partly depleted, and the electric field may be lower than in forward bias. However, as visible in Fig. 5, the trend during recovery does not depend on the applied voltage, even if high voltages (up to −55 V) are used.

Another possible explanation that is also compatible with the absence of symmetry is that detrapping under positive gate bias is induced by the recombination of electrons (injected by Fowler-Nordheim tunneling from the semiconductor to the oxide) with the holes trapped in the stress phase, as in Fig. 12.

This process would only take place under positive gate bias, thus being compatible with the observations, and is almost temperature-independent. Fowler-Nordheim tunneling in fact depends mostly on the width of the tunneling barrier, which in turn depends on the field applied to the gate. This in conclusion explains the crucial role of a strong positive field.

6. Conclusions

In this work, we presented the first detailed analysis of hole

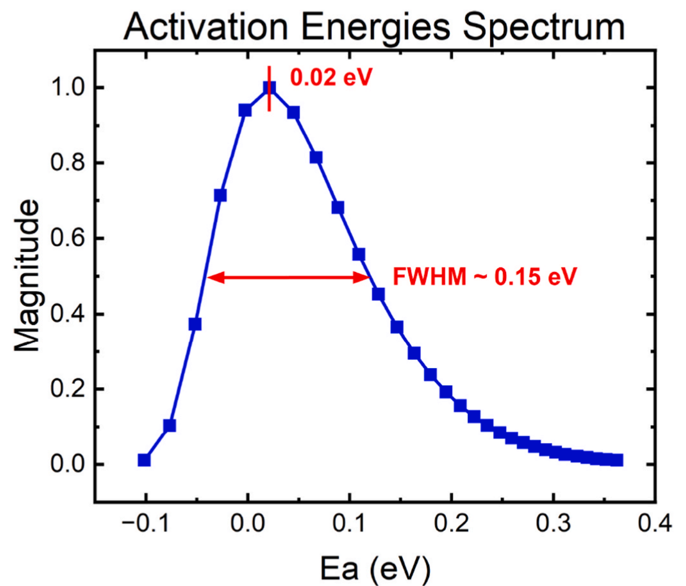

Fig. 10. Activation energies spectrum (or energy distribution) of the trapped holes, as extracted from the Trap State Mapping algorithm.

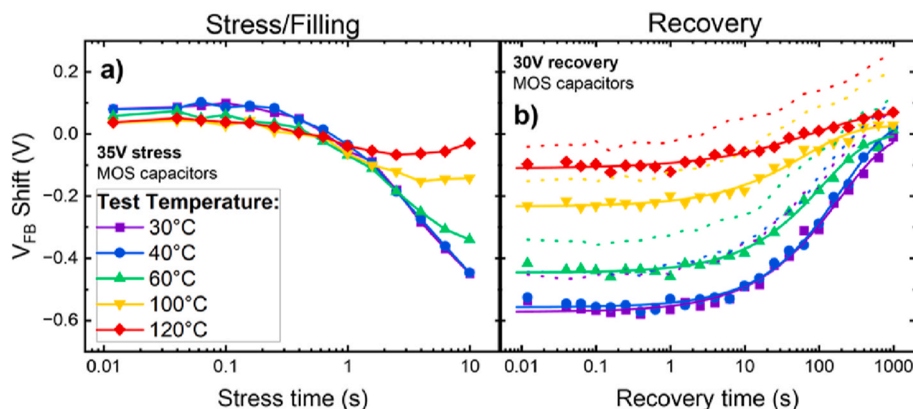

Fig. 9. V_{FB} transient for a stress and recovery experiment. Stress (a) and recovery (b) were performed at different temperatures. In (b), small dots are transients as measured, big dots are transient without electron trapping contribution. Solid lines are the model fit of Eq. (2).

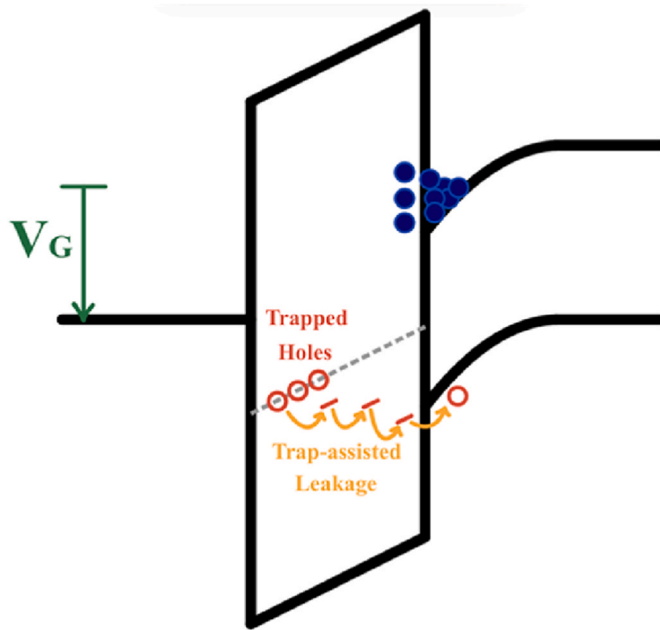

Fig. 11. Band diagram for trap-assisted hole release process, under a strong positive gate bias.

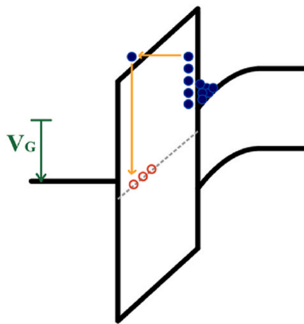

Fig. 12. Band diagram of the recombination between Fowler-Nordheim injected electrons and trapped holes.

detrapping after positive gate stress of 4H–SiC vertical MOS capacitors.

With a strong positive stress bias, V_{FB} trend exhibits a) a slight positive shift attributed to electrons trapping in border traps or NIOTs and b) a strong negative shift explained by hole trapping in the oxide. Holes are believed to be generated within the oxide via impact ionization, under a strong field in the oxide.

To better understand the physics of hole trapping and release, the recovery process was analyzed as a function of bias, light and temperature. The process proved to be almost temperature-independent and no recovery was observed at room temperature with 0 V, negative or low positive bias. High energy light, up to 280 nm UV-C light has been used to induce the recovery of trapped holes, but without any effect. The only recovery strategy that proved to work has been the application of a strong positive bias, just below the threshold for impact ionization.

The results are interpreted by considering that holes are trapped at deep defect levels. Thermal detrapping is not possible, and only field or recombination with electrons can promote the release of holes, which is weakly thermally activated.

Author statement

I declare that every named author of this original research paper on the Origin and Recovery of Negative V_{TH} Shift on 4H–SiC MOS Capacitors: an Analysis Based on Inverse Laplace Transform and Temperature-Dependent Measurements has contributed equally to the submitted work.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

Appendix. Trap State Mapping Technique

Trap State Mapping is a technique, proposed by Modolo et al. [29], to estimate the energy distribution of traps starting from measured V_{TH}/V_{FB} transient curves where such levels are detrapped. These transients need to be measured at different temperatures because the temperature dependence of the process is fundamental to obtain the final activation energies spectrum.

This technique was tested on GaN devices in the past and is reportedly able to estimate a trap density that, if used in a TCAD simulation, yields to the reproduction, in an independent way, of the measured transients used to estimate the trap density in the first place. The technique is described in detail in Ref. [29] and is briefly outlined in the following.

The equivalence between a stretched exponential function and an infinite sum of single exponentials has been described in Eq. (2). This last expression can also be considered in its integral form, where the amplitudes of the individual exponentials are expressed as a function of their time constants with the function $f(\tau)$. This expression also corresponds to the Laplace Transform of the function $f(\tau)$, allowing the extraction of $f(\tau)$ by calculating an Inverse Laplace Transform.

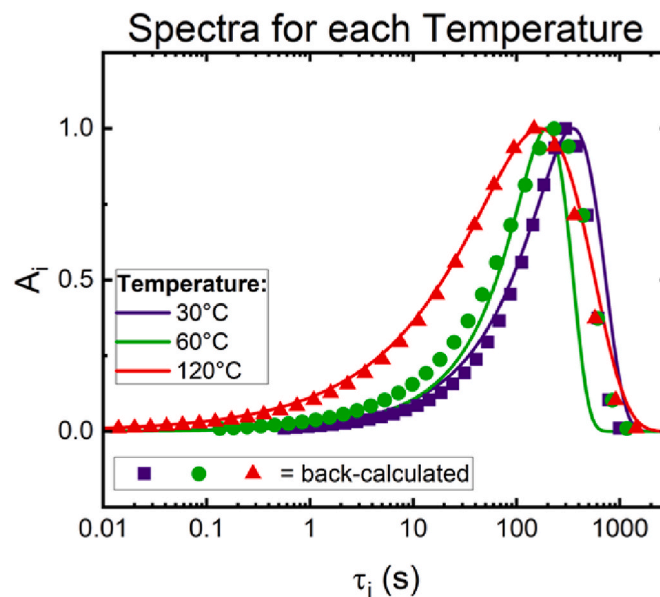

Fig. 13. Exponential amplitude distributions at different test temperatures, calculated applying the Inverse Laplace Transform to fitted transients.

By repeating this process at each test temperature, the curves in Fig. 13 can be obtained. They represent, for each temperature, the time constant spectra of the individual exponential components that, summed, yield the measured stretched exponential transient. From Fig. 13, we can see how the time constants spectrum changes with temperature. By assuming the amplitude contribution of a single trap level is the same at every temperature (or that the influence of temperature on a single exponential transient is only on the time constant and not on the amplitude), the algorithm proceeds in discretizing the amplitude axis. At each amplitude discretization level, a single trap level is associated, and an Arrhenius plot is built using the different time constants extracted at the different temperatures for that single trap level. The procedure is applied with a fine discretization of the amplitude axis, achievable via software automation; activation energy E_C and cross-section σ_e are evaluated for each trap level. This allows to create a link between the amplitude of a single exponential transient and the activation energy associated with the corresponding trap level, thus enabling the possibility of generating an activation energy spectrum and therefore to obtain the energy distribution of the trapped charge (that is being detrapped during recovery), as visible in Fig. 10. Every dot in the figure represents a discretization point in the amplitude spectrum.

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