Enhancing DC Microgrids Integration with Three-Phase AC Grids Using Multiport Converters

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Abstract

DC Microgrids offer a zero-carbon emission solution to meet the escalating demand for electric energy by facilitating the integration of renewable energy sources, energy storage, and loads. To enhance the stability and sustainability of DC microgrids, a bidirectional power interface with the utility grid is adopted. This paper proposes a non-isolated multiport converter that interfaces three-phase AC grids with multiple microgrids, allowing for minimizing the overall size and cost compared to the multi-converter approach, and providing additional flexibility and resilience to the system. The main objective of the study is to validate the superior performance of the proposed converter compared to the conventional approach of interconnecting DC-DC and AC-DC converters in a cascaded connection. The study comprehensively evaluates semiconductor device stresses, losses, total chip area, and magnetic element size for both approaches. Finally, experimental results of the proposed converter are presented.

1 Introduction

The surging demand for electric energy presents challenges that require a proportional increase in energy generation. Relying on traditional sources can lead to environmental issues, making renewable energy sources an ideal, zero-carbon emission solution. DC Microgrids (DC MGs) emerge as a promising solution, connecting distributed power sources to distribution networks and avoiding the need for extensive centralized utility grid expansion. Additionally, they gain prominence in modern electrical grid systems due to their natural compatibility with renewable sources, electric loads, and energy storage. The DC MGs are commonly linked with low- or medium-voltage utility grids to enhance stability and sustainability.

Towards selecting the optimum voltage level for low-voltage (LV) DC MGs, various studies have assessed a range of DC levels, spanning from 12 V to 1500 V. Notably, the 400 V DC system has emerged as the preferred choice for residential and commercial DC microgrids due to its superior overall system efficiency and the need for fewer power conversions when connecting multiple energy sources and loads. To establish a highly efficient power interface between the three-phase AC grid and the 400 V DC MG, optimized single-stage converters, such as the current source converter, the swiss converter, and the Y-converter have been evaluated. Among these converters, the Y-converter demonstrated superior overall performance in terms of efficiency and power density. Additionally, two-stage converters formed by a cascaded connection of the voltage source converter (VSC) and an additional step-down stage are addressed in the literature [1].

With the increasing adoption of DC MGs for residential and commercial applications, the conventional practice of providing a dedicated converter for each MG to interface with the utility grid can lead to a significant increase in system size and cost. An alternative and more efficient solution is the use of MPCs, which consolidate multiple energy ports into a single hub. Fig. 1 illustrates the concept of interfacing the utility grid with multiple DC MGs using a single MPC.

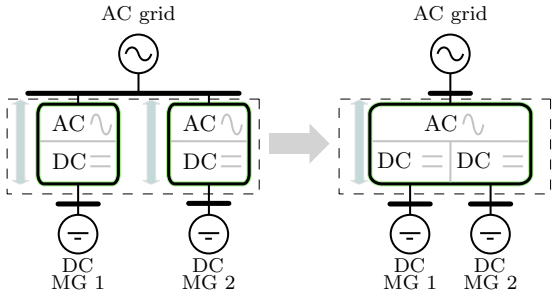


Fig. 1: Multiport converter linking DC microgrids with the AC grid instead of coventional two-port converters.

MPCs not only offer the opportunity to minimize overall size and cost compared to the multi-converter approach but also provide flexibility and resilience to both the DC MGs and the utility grid. When MPCs are utilized, DC MGs can directly exchange power through the MPC, reducing dependence on the utility grid. This approach opens up opportunities for optimizing power flow among different energy ports, enhancing the overall efficiency and reliability of the system.

A significant obstacle in the widespread adoption of MPCs for power applications lies in the challenge of validating their superior performance compared to the conventional approach of interconnecting DC-DC and AC-DC converters in a cascaded connection. While various AC-DC MPCs have been proposed to interface single-phase and three-phase AC grids with DC systems, a detailed performance evaluation of the MPC approach versus the cascaded-converter approach is currently lacking [2].

Typically, evaluations focus on the number of semiconductor devices and passive elements in both approaches. However, these numbers alone can be misleading without addressing their corresponding stresses, losses, total chip area for semiconductor devices, and the total losses and size of passive elements. A comprehensive performance evaluation, considering these factors, is crucial for making informed decisions regarding the suitability of MPCs in practical power applications.

In this paper, a non-isolated MPC is proposed, named as multiport Y-converter (Y-MPC), to interface the three-phase AC grid with 400 V DC MGs. The primary objective of this study is to conduct a comprehensive evaluation of the proposed converter in comparison to the conventional cascaded connection approach. For this specific application, the conventional topology involves the cascaded connection of VSC and DC-DC interleaved bucks (IBs) and it will be named herein as VSC+IBs. The paper provides a detailed comparison addressing stresses, losses, total chip area of semiconductor devices for both topologies, and estimates the total size of magnetic elements to meet the CISPR 11 Class B EMI standard. The remainder of the paper is structured as follows: Sec. 2 provides a comprehensive overview of both approaches, Sec. 3 presents the evaluation of semiconductor devices' stresses, losses, total chip area, and magnetic element size. Experimental results are presented in Sec. 4, and finally, Sec. 5 provides the conclusion.

2 Topology Overview

In this section, a concise overview is provided on the two topologies, accompanied by an explanation of their operational principles and their key waveforms.

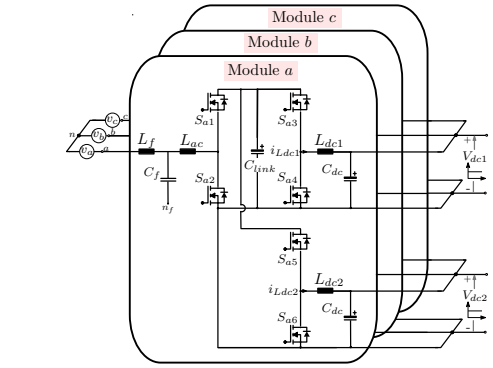
2.1 VSC+IBs

VSC is typically chosen as the interface converter between the three-phase AC grid and the DC systems due to its simple structure, control, and high power density. However, when interfacing the 400 V DC MGs with the European LV AC grid (operating with a line-to-line voltage of 400 V_{RMS}), an additional step-down stage is required. This step-down stage is implemented using three-phase IBs to minimize current stresses on the semiconductor devices and reduce the size of the buck stage inductor.

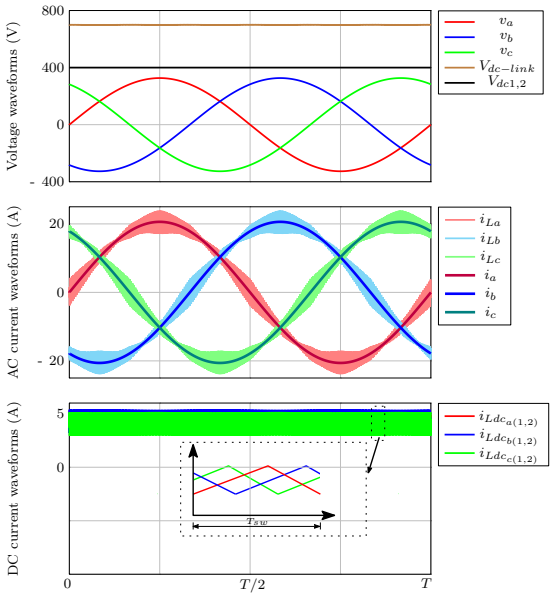
Fig. 2a illustrates, in a modular representation, the cascaded connection between the VSC and the three-phase IBs to form a MPC. The VSC and IBs are connected to the same DC-link, which is controlled at a fixed voltage of 700 V, given that the VSC operates with sinusoidal pulse width modulation. Key waveforms are depicted in Fig. 2b, including voltage, AC grid current, and inductor current waveforms.

2.2 Y-MPC

Fig. 3a illustrates the proposed Y-MPC in a modular representation. The structure is based on the Y-converter introduced in [3], transforming it from a two-port converter to function as a multi-port converter capable of linking multiple DC ports



(a) Schematic of the VSC+IBs



(b) Key waveforms of the

Fig. 2: Schematic and key waveforms of the VSC+IBs.

to a three-phase AC grid. The original two-port Y-converter consisted of three four-switch buck-boost modules while the proposed converter transforms each module into a six-switch DC-DC converter. In the context of a three-port converter, the upgraded design features a common buck half-bridge and two boost half-bridges, establishing connections to the DC ports. To facilitate the incorporation of additional DC ports, the configuration can be easily expanded by integrating one boost converter into each module for every extra DC port.

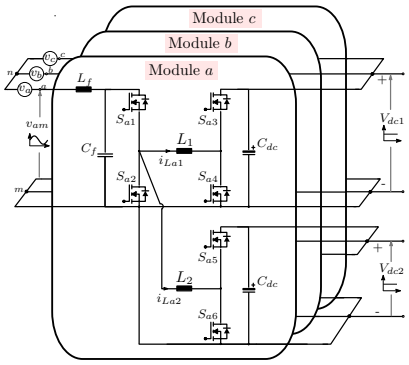
Similar to the two-port Y-converter, the three modified modules are interconnected at a central point denoted as m, which functions as the neutral point for the Y-connection of the modules. As each module serves as a DC-DC converter, it is crucial to maintain a non-negative voltage on the AC side of the module ($v_{\{a,b,c\}m} \geq 0$ V). To achieve this, an offset voltage is necessary between grid neutral point n and m. A constant offset voltage (V_{off}) is then applied, which should be higher than the peak value of the AC grid phase voltage ($\hat{V}_m$). The AC-side voltages v_{am}, v_{bm}, and v_{cm} can be mathematically expressed

as:

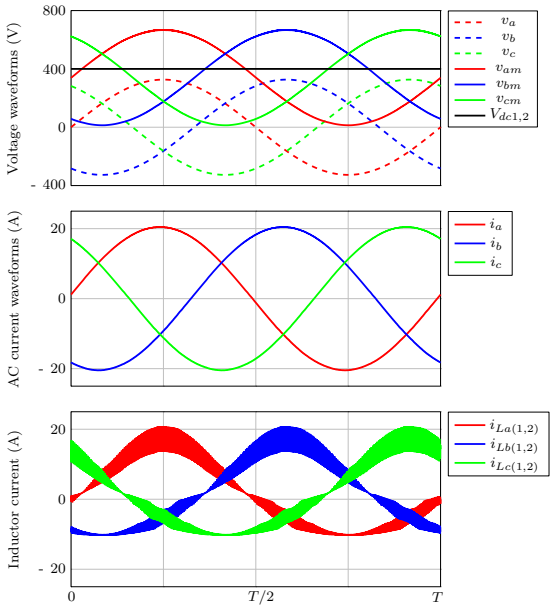
$$\begin{aligned} v_{am} &= \hat{V}_m \sin(\omega t) + V_{off} \\ v_{bm} &= \hat{V}_m \sin(\omega t - 2\pi/3) + V_{off} \\ v_{cm} &= \hat{V}_m \sin(\omega t + 2\pi/3) + V_{off} \end{aligned} \tag{1}$$

where ω is the AC grid frequency in rad/s.

Considering module a and assuming V_{dc1} equals V_{dc2}, the module operates in two modes. The first mode is considered a buck mode when v_{am} is greater than $V_{dc1,2}$. In this mode, only the buck half-bridge is modulated, while the boost half-bridges are clamped with S_{a3}, S_{a5} on and S_{a4}, S_{a6} off. Conversely, when v_{am} is lower than $V_{dc1,2}$, the boost mode is in operation. In this mode, only the boost half-bridges are modulated, while the buck half-bridge is clamped with S_{a1} on and S_{a2} off. The key waveforms of the proposed converter are plotted in Fig. 3b, including the voltage, AC grid current, and inductor current waveforms.



(a) Schematic of the Y-MPC



(b) Key waveforms of the Y-MPC

Fig. 3: Schematic and key waveforms of the Y-MPC.

3 Topology Comparison and Evaluation

In this section, the power converters are evaluated in terms of stresses, losses, the total chip area of semiconductor devices, and the total size of magnetic elements. For semiconductor devices, the selection criteria are discussed along with the estimation of the corresponding total chip area. The semiconductor is also evaluated using PLECS simulation for the entire power range.

For magnetic elements, a simplified analytical method is presented for magnetic element design and volume estimation to meet the CISPR 11 Class B EMI standard for the AC grid. The specifications and ratings utilized in the evaluation are summarized in Table 1. The AC and DC power ratings are selected for residential and commercial applications and are chosen to be $\pm 10\,\mathrm{kW}$ and $\pm 5\,\mathrm{kW}$, respectively.

Table 1 Specifications utilized in converters evaluation

Parameter	Symbol	Value
Rated AC power	$P_{ac,r}$	$\pm 10\,\mathrm{kW}$
Rated DC power	$P_{dc1,r}$, $P_{dc2,r}$	$\pm 5\,\mathrm{kW}$
AC line voltage, frequency	V_{ll}, f_o	$400\,\mathrm{V}$, $50\,\mathrm{Hz}$
DC voltage	V_{dc1}, V_{dc2}	$400\,\mathrm{V}$
Switching frequency	f_{sw}	$62.5\,\mathrm{kHz}$

3.1 Semiconductor Devices

The initial step in device selection involves determining their voltage ratings based on the specific stresses encountered in the converter configurations. For the VSC+IBs, where all devices experience a voltage stress equal to the DC-link voltage V_{link} ($700\,\mathrm{V}$), $1200\,\mathrm{V}$ SiC devices are chosen. In the case of the Y-MPC, the AC-side buck half-bridges handle voltages with a peak value of $\hat{V}_m + V_{off}$ ($655\,\mathrm{V}$ at V_{off} equals $340\,\mathrm{V}$), justifying the use of $1200\,\mathrm{V}$ SiC devices. Meanwhile, the DC-side boost half-bridges are subjected to the respective DC port voltage ($400\,\mathrm{V}$), allowing the adoption of $650\,\mathrm{V}$ SiC devices.

The CoolSiC discrete MOSFETs from Infineon with TO247-4 package are chosen for the evaluation. This SiC family includes devices with the desired voltage ratings of $1200\,\mathrm{V}$ (IMZ120, IMZA120) and $650\,\mathrm{V}$ (IMZ65). To assess the chip area of the devices, it is assumed that the specific on-resistance $R_{ds,sp}$ remains constant for all devices with the same voltage rating. Specifically, it is set at $200\,\mathrm{m\Omega \cdot mm^2}$ and $350\,\mathrm{m\Omega \cdot mm^2}$ for the $650\,\mathrm{V}$ and $1200\,\mathrm{V}$ devices, respectively [4, 5].

The selection criterion for the SiC devices is to achieve the lowest overall semiconductor chip area for the converter. Starting from the devices with the highest R_{ds}, the junction temperature of each device is calculated using PLECS thermal modeling. The device is selected if its junction temperature is below $125\,^\circ\mathrm{C}$; otherwise, the device with a lower R_{ds} is chosen until the temperature criterion is met. In addition to the PLECS Foster model for the thermal chain between the device chip and case, a thermal resistance is added to the model to

represent the case to heat sink resistance and it is assumed to be equal for all devices given their TO247-4 package and it is equal to $0.3\,\mathrm{K\,W^{-1}}$. Accordingly, The selected devices for each converter are presented in Table 2.

Table 2 Selected SiC devices for converters evaluation

Device symbol	VSC+IBs	Y-MPC
$S_{(a,b,c)1}$	IMZA120R040M1H	IMZ120R030M1H
$S_{(a,b,c)2}$	IMZA120R040M1H	IMZ120R060M1H
$S_{(a,b,c)3,5}$	IMZ120R140M1H	IMZA65R057M1H
$S_{(a,b,c)4,6}$	IMZ120R140M1H	IMZA65R107M1H

Fig. 4 summarizes the evaluation of semiconductor devices for the two converters. It presents the voltage and current stresses, along with the total chip area for each converter. The Y-MPC exhibits a slightly higher total chip area than the VSC+IBs, with only a 2.8% increment. Considering that the theoretical limit for $R_{ds,sp}$ of 1200 V SiC devices is four times the limit for $R_{ds,sp}$ of 650 V SiC devices, advancements in SiC devices manufacturing towards the nearly ideal theoretical limits could potentially alter the evaluation results in favor of the Y-MPC.

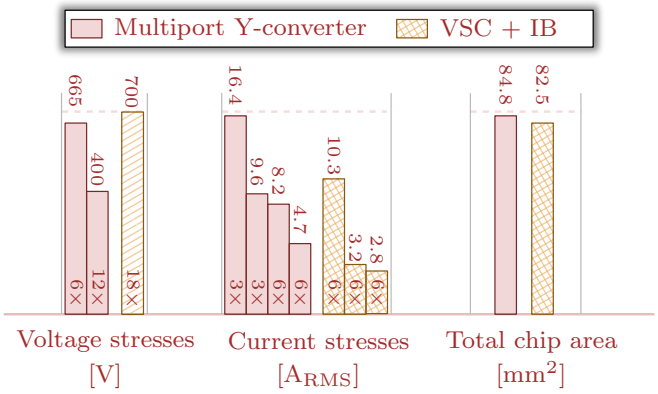


Fig. 4: Evaluation of both converters in terms of semiconductor stresses and chip area.

The semiconductor losses of the converters across the entire power range are illustrated in Fig. 5. The Y-MPC exhibits higher conduction losses due to relatively higher current stresses compared to VSC+IBs. However, the Y-MPC achieves significantly lower switching losses since not all devices are continuously commutating. This is in contrast to VSC+IBs, where all devices continuously commutate, subjecting them to the V_{link} voltage stress. Overall, semiconductor losses demonstrate that the Y-MPC outperforms VSC+IBs across the entire power range. At rated power in rectification mode, semiconductor losses for Y-MPC and VSC+IBs are 149 W and 172 W, respectively. For rated power in inversion mode, the losses are 164 W for Y-MPC and 173 W for VSC+IBs.

3.2 Magnetic Elements

The VSC+IBs configuration includes three distinct magnetic elements: the VSC inductance L_{ac}, the IBs inductors $L_{dc(1,2)}$, and the EMI filter inductor L_f. The selection of L_{ac} directly influences the total harmonic distortion (THD) and the resultant high-frequency noise generated by its switching ripple current. Studies recommend allowing for a maximum peak-to-peak ripple current $\Delta I_{Lac,pkpk}$ ranging from 20% to 40% of the peak grid current to limit the peak switching current and high-frequency losses [6]. In this evaluation, $\Delta I_{Lac,pkpk}$ is set to be 40%, aiming to reduce the inductor's volume. Similarly, for $L_{dc(1,2)}$, the peak-to-peak ripple current $\Delta I_{Ldc,pkpk}$ is set to be 60% for each inductor. The design equations for L_{ac} and $L_{dc(1,2)}$ are as follows:

$$L_{ac} = \frac{1}{\Delta I_{Lac,pkpk}\ f_{sw}} \cdot \frac{\sqrt{2}\ V_{ll}\ \cos\left(\frac{\pi}{6}\right)}{\left(\frac{2}{3}\ V_{link} - \sqrt{\frac{2}{3}}\ V_{ll}\right)\ V_{link}} \tag{2}$$

$$L_{dc(1,2)} = \frac{1}{\Delta I_{Ldc(1,2),\text{pk-pk}}\ f_{\text{sw}}} \cdot \frac{V_{dc(1,2)}(V_{\text{link}} - V_{dc(1,2)})}{V_{\text{link}}} \tag{3}$$

In the Y-MPC, the generated high-frequency noise is dependent on the operating mode. In buck mode, the converter exhibits a switched high-frequency current, while in boost mode, it exhibits a triangular high-frequency current. The peak RMS value of the high-frequency ripple current in both modes can be calculated as follows [7]:

$$I_{hf_{\text{RMS}}} = \begin{cases} \hat{I}_m \sqrt{\frac{\hat{V}_m + V_{off}}{V_{dc(1,2)}} - 1} & \text{Buck mode} \\ \frac{V_{dc(1,2)}}{8\sqrt{3}\ L_{1,2}\ f_{sw}} & \text{Boost mode} \end{cases} \tag{4}$$

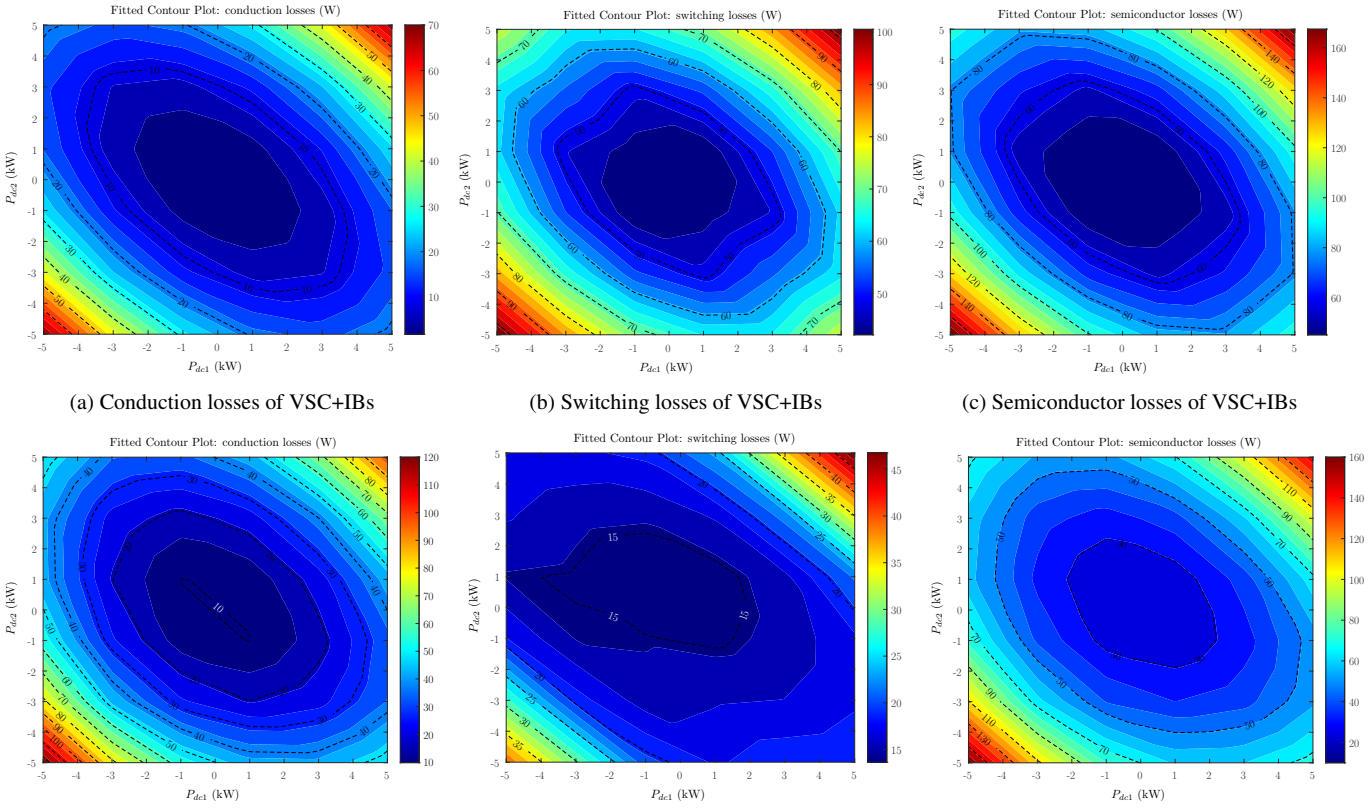
where $\hat{I}_m$ is the peak grid current.

A minimum limit for L_1 and L_2 can be defined to restrict $I_{hf_{\text{RMS}}}$ in both buck and boost modes to the same value. For the presented case study, the minimum limit for L_1 and L_2 is set at 50 µH. To limit the peak switching current and core losses, L_1 and L_2 are chosen to be 150 µH.

For the EMI filter design, high-frequency emissions are calculated, and accordingly, the required attenuation to meet CISPR 11 Class B is defined, and the passive components are designed. The $I_{hf_{\text{RMS}}}$ at the first switching harmonic that falls into the EMI standard limit (above 150 kHz), denoted as $I_{hf-h_{\text{RMS}}}$, can be calculated as follows:

$$I_{hf-h_{\text{RMS}}} = \begin{cases} \frac{V_{link}}{8\sqrt{3}\ L_{ac}\ f_{sw}\ n_h^2} & \text{VSC+IBs} \\ \frac{\hat{I}_m}{n_h} \sqrt{\frac{\hat{V}_m + V_{off}}{V_{dc(1,2)}} - 1} & \text{Y-MPC} \end{cases} \tag{5}$$

where n_h is the switching harmonic order (equals to 3 at the selected f_{sw}).



(a) Conduction losses of VSC+IBs (b) Switching losses of VSC+IBs (c) Semiconductor losses of VSC+IBs

(d) Conduction losses of Y-MPC (e) Switching losses of Y-MPC (f) Semiconductor losses of Y-MPC

Fig. 5: Fitted contour plots illustrating the power losses of the semiconductor devices in the proposed converter at rated power.

The required attenuation by the EMI filter in $\mathrm{dB\,\mu V}$, denoted as ATT, can be determined for both converters as follows:

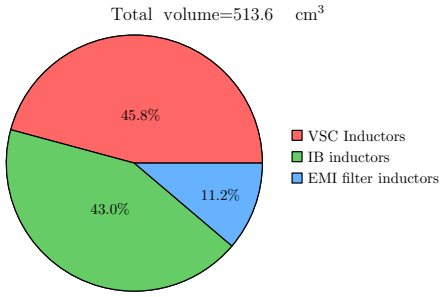
$$ATT = V_{hf-h_{\mathrm{RMS}}} - V_{CISPR} + 10 \tag{6}$$

where $V_{hf-h_{\mathrm{RMS}}}$ is the noise in $\mathrm{dB\,\mu V}$ generated from $I_{hf-h_{\mathrm{RMS}}}$ considering a $50\,\Omega$ LISN, and V_{CISPR} is the specified noise limit at the switching harmonic in $\mathrm{dB\,\mu V}$ with an additional margin of $10\,\mathrm{dB\,\mu V}$. For a multi-stage LC filter with n_f input filter stages equal to 3, the product of filter inductance L_f and capacitance C_f is calculated as:

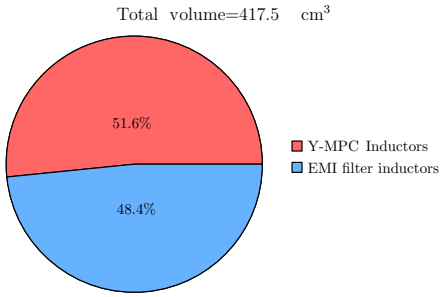
$$L_f\, C_f = \frac{10^{ATT/(20n_f)}}{(2\pi n_h f_{sw})^2} \tag{7}$$

Finally, L_f can be calculated by selecting the total filter capacitance to limit its reactive power to 5% of $P_{ac,r}$ and then using (7) to calculate L_f.

A simple approach to estimate the inductor volume is presented in [8]. The estimated total inductors volume of both converters is illustrated in Fig. 6 where the Y-MPC yields a total inductors volume equal to 81% of the VSC+IBs inductors volume.



(a) VSC+IBs inductors volume



(b) Y-MPC inductors volume

Fig. 6: Evaluation of converters in terms of inductors volume.

4 Experimental Results

Fig. 7 illustrates the experimental prototype of the Y-MPC. The prototype is constructed by combining six Imperix SIC power modules (PEB8024 with C2M0080120D SiC MOSFET) for the boost half-bridges and three half-bridges with UF4SC120023K4S SiC MOSFETS. Control is achieved using

two B-box controllers in a master-slave configuration. Bidirectional AC and DC power supplies are employed to emulate the AC grid and DC microgrids. The single-stage input filter is utilized with $L_f = 1.2\,\text{mH}$ and $C_f = 10\,\mu\text{F}$, while L_1 and L_2 are implemented using $350\,\mu\text{H}$ inductors.

Experimental waveforms are displayed in Fig. 8, where the converter operates with V_{dc1} and V_{dc2} set to $360\,\text{V}$ and $400\,\text{V}$, respectively, and P_{dc1} and P_{dc2} equal to $3\,\text{kW}$.

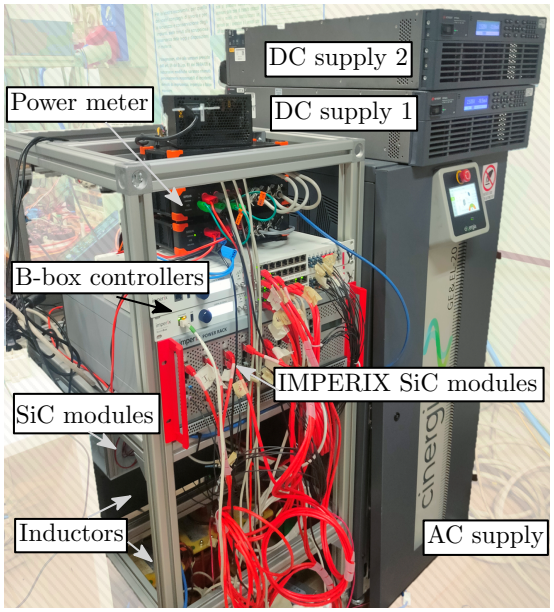


Fig. 7: Experimental prototype of the Y-MPC

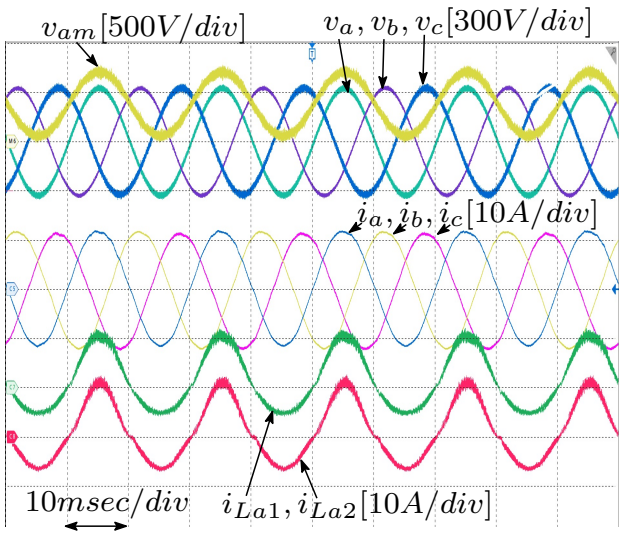


Fig. 8: Experimental waveforms in rectification mode.

5 Conclusion

This paper introduces a non-isolated multiport converter designed for interfacing three-phase AC grids with $400\,\text{V}$ DC microgrids. A comprehensive evaluation compares this converter to the conventional cascaded connection approach involving AC-DC and DC-DC converters. The assessment covers semiconductor device stresses, losses, total chip area, and magnetic element size. The study confirms the superior performance of the proposed converter, particularly in semiconductor losses and total inductor volume, compared to the conventional cascaded connection approach. Experimental results are also presented to demonstrate the validity of the proposed converter.

6 Acknowledgements

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