# Switching Noise Propagation and Suppression in Multi-sampled Power Electronics Control Systems

Ruzica Cvetanovic, *Student Member, IEEE*, Ivan Z. Petric, *Member, IEEE*, Paolo Mattavelli, *Fellow, IEEE*, Simone Buso, *Member, IEEE* 

Abstract—This article addresses switching noise propagation and its suppression in multi-sampled pulse-width modulated (MS-PWM) current-controlled systems. MS-PWM enables very high control bandwidths by reducing digital delays. However, when the sampling instants occur near the commutation ones, system performance is prone to being impaired by switching noise. It is analyzed how using the typically considered moving average filters (MAFs) in feedback may have an adverse effect, especially when the number of the noise-corrupted samples is high compared to the number of averaged samples. It is also shown that, without any filters, MS-PWM on its own may mask the negative impact of noise, due to modulator-related non-linear effects. However, these non-linearities can lead to an undesirable response to transients and output waveform distortion. Hence, this article proposes MS-PWM with medianbased feedback filtering. To avoid ranking within median filter (MED) being affected by the switching ripple, repetitive ripple removal (RRR) is added before MED. The effectiveness of the proposed strategy in suppressing the switching noise is verified in simulations and experiments, during dc and ac operation. RRR + MED successfully suppresses noise-sensitive operating point regions that appear with MAF. Finally, it is shown that, even with added RRR + MED, MS-PWM still retains dynamic improvements over the standard DS-PWM without any filters, offering better reference tracking and disturbance rejection.

*Index Terms*—Current-control, median filter (MED), moving average filter (MAF), multi-sampled pulse-width modulation (MS-PWM), multi-rate systems, switching noise.

## I. INTRODUCTION

**C**ONTROL of most medium to high power contemporary power electronics systems (PESs) is realized in digital platforms [1]. The converter switching states are usually determined using pulse-width modulation (PWM) [1]. Typically, feedback sampling and control execution are performed once or twice per modulation period, yielding single-sampled PWM (SS-PWM) or double-sampled PWM (DS-PWM) [1].

Manuscript received April 28, 2023; revised August 1, 2023; accepted September 18, 2023. The research has been funded by the project "Network 4 Energy Sustainable Transition – NEST" under the National Recovery and Resilience Plan (NRRP), Mission 4 Component 2 Investment 1.3 - Call for tender N. 341 del 15.03.2022 of Ministero dell'Università e della Ricerca (MUR), funded by the European Union – NextGenerationEU. The NEST project code is PE0000021, Concession Decree No. 1561 of 11.10.2022 by MUR, CUP C93C22005230007.

R. Cvetanovic, and S. Buso are with the Department of Information Engineering, University of Padova, 35131 Padova, Italy (e-mail: ruzica.cvetanovic@phd.unipd.it; simone.buso@dei.unipd.it).

I. Z. Petric is with Hanwha Q CELLS America Inc., Santa Clara, California, USA (e-mail: ivan.petric@phd.unipd.it).

P. Mattavelli is with the Department of Management and Engineering, University of Padova, 36100 Vicenza, Italy (e-mail: paolo.mattavelli@unipd.it).

To ensure that, in the absence of any non-idealities, the average value of the feedback signal is acquired, sampling instants in current-controlled systems are often chosen to coincide with peaks and/or valleys of the triangular PWM carrier [1]. However, various phenomena, such as dead-times, antialiasing filters and noise, cause feedback acquisition errors, which impair system performance [2], [3]. Another shortcoming of (S/D)S-PWM is a high modulation delay, which limits the achievable bandwidths and deteriorates the robustness of PESs [1]. To handle these issues, multi-sampled (oversampled) control is becoming prevalent in high-performance PESs [2]–[9].

1

Two different types of multi-sampled control strategies can be distinguished. The first one [2]-[4], termed multi-rate single/double-sampled PWM (MR-(S/D)S-PWM), is aimed solely at suppressing the feedback acquisition errors. It includes oversampling the feedback signal, applying digital filtering, and decimating the control execution to (S/D)S-PWM. Nevertheless, feedback filters introduce additional phase lag, which further limits the achievable bandwidths of MR-(S/D)S-PWM. A significant improvement can be obtained using advanced modulation methods, such as multi-sampled PWM (MS-PWM) [5]-[9]. In MS-PWM, which is the second considered type of multi-sampled control strategy, feedback sampling and control execution are performed more than twice per modulation period. By reducing the modulation delay, MS-PWM can break the bandwidth limitations exhibited by SS-PWM, DS-PWM and MR-(S/D)S-PWM [1], [5]-[11], while also ensuring high noise immunity [6], [7].

Since in both MR-(S/D)S-PWM and MS-PWM the feedback is, by definition, oversampled, when the sampling instants occur near the commutation ones, system performance is prone to being affected by switching noise [4], [12]. Switching noise, whose propagation and suppression is the primary focus of this article, originates from high-frequency oscillations caused by fast commutations and parasitic LC elements [2], [13]–[20]. Contrary to white noise, whose propagation was addressed in [6], [7], switching noise exhibits non-stationary nature [21], [22]. In the PESs tested in [6], [7] white noise was the dominant source of noise. Thus, the developed models for noise propagation, which assumed noise to be stationary and uncorrelated with the feedback, were applicable. However, there are PESs where the switching noise is dominant and thus, these models can not be applied on their own.

To the best of the authors' knowledge, only a few references addressed the impact of switching noise in multi-sampled PESs. In [4] enhanced feedback averaging is proposed for multi-rate control systems, where the samples acquired closely after the gate turn-on and -off commands are replaced by the previously acquired ones. However, this approach does not take into account whether or not the replaced samples are in fact corrupted. Moreover, it does not consider the impact of the delays in the propagation path of the switching signal, which shift the real switching instants with respect to the commanded ones. A similar switching noise-suppression approach is proposed in [12], for MS-PWM control without any feedback filters. There, in addition to the previously mentioned shortcomings, the proposed approach introduces some dc tracking error. Switching noise propagation and mitigation in current controlled MR-(S/D)S-PWM systems was addressed in [23], for dc operation. It is shown that, the typically considered moving average filters (MAFs) may bring a detrimental impact, especially when the number of corrupted samples is high with respect to the number of samples used for filtering. As an alternative, [23] proposes the use of a modified median filter (MED) [20], [24], [25]. To decouple the ranking within MED from the switching ripple, [23] adds a repetitive ripple removal (RRR) [9] beforehand. It is shown in [23] that MR-DS-PWM with RRR + MED eliminates noise-sensitive operating point regions that appear with MAF. Moreover, with such a configuration, the well-known switching noise sensitivity of typically used DS-PWM for small and large duty cycles is eliminated as well. Still, switching noise propagation and suppression during ac operation was not addressed in [23]. Furthermore, as shown in this article, the control strategy proposed in [23], featuring MR-DS-PWM with RRR + MED, significantly impairs dynamic performance compared to typically used DS-PWM without any filters, due to the delay introduced by the filtering scheme.

With a goal of developing a robust control strategy that ensures high noise immunity for dc and ac operation without impairing dynamic performance, this article addresses switching noise propagation and suppression in MS-PWM systems. It is shown how MS-PWM without feedback filters does not necessarily exhibit high switching noise sensitivity, as the corrupted samples can be masked by the PWM decimation effect and vertical intersections between the modulating signal and the carrier. As in the case of MR-(S/D)S-PWM, the use of MAF in MS-PWM fails to effectively suppress the switching noise, while RRR + MED successfully suppresses it for dc and ac operation. The dynamic performance of different strategies is analyzed, where benefits of using MS-PWM with respect to MR-DS-PWM and DS-PWM are explained. As verified in simulations and experiments, the proposed control strategy featuring MS-PWM with RRR + MED not only ensures high noise immunity, but also offers better dynamic performance than the control strategy proposed in [23] as well as typically used DS-PWM without any filters. Design guidelines for determining the key parameter values of the proposed control strategy are also provided.

The rest of the article is organized as follows. In Section II, the basic principles of switching noise propagation in the considered multi-sampled systems are outlined. Switching noise suppression using median-based feedback filtering is explained in Section III, along with an overview of its impact



Fig. 1: Block diagram of the considered multi-sampled current-controlled digital pulse-width modulated power electronics system.



Fig. 2: Synchronization between PWM carrier, feedback sampling instants and modulating signal sampling (update) instants for the system from Fig. 1, given for: (a) MR-DS-PWM and (b) MS-PWM control, both with N = 8.

on the dynamic performance. Simulation and experimental results, obtained using a laboratory prototype of a currentcontrolled voltage-source converter, are presented in Section IV and V. Section VI concludes the article. Extension of the presented methodology to multi-level and interleaved PESs is discussed in the Appendix.

# II. SENSITIVITY OF DIGITAL CONTROL SYSTEMS TO SWITCHING NOISE

## A. Considered Multi-sampled Systems

In this article, digitally controlled pulse-width modulated (PWM) converters are considered, which feature single PWM carrier and two commutations per modulation period. Extension to multi-level and interleaved converters is addressed in the Appendix. The analyzed converters operate using a single-stage control loop, where the inductor current  $i_L$  is directly controlled. Nevertheless, the analysis can be extended to single-stage output voltage control and multi-stage control loop configurations. A block diagram of the considered system is shown in Fig. 1. An analog-to-digital converter (ADC) performs the transition from the continuous to the digital domain, with sampling frequency  $f_s = N f_{pwm}$ , where N is the multi-sampling (oversampling) factor and  $f_{pwm}$  is the frequency of the triangular PWM carrier  $w^1$ . The sampled inductor current  $i_s$  is processed by a feedback filtering block,

<sup>1</sup>Constant  $f_{pwm}$  is assumed in this article. Extension of the presented methodology to the PESs with variable  $f_{pwm}$  is a topic of future research.

whose specific structures are addressed in Section III. After feedback filtering, a rate change from  $f_s$  to  $f_c = N_c f_{pwm}$  may be imposed, where  $N_c$  and  $f_c$  are the control update factor and frequency, respectively.

When  $N_c = N$  the entire digital domain is executed at the single-rate  $f_s = f_c$ . Typically, N is set to 1 or 2, yielding single- (SS-PWM) or double-sampled PWM (DS-PWM). For  $N_c = N > 2$ , multi-sampled PWM (MS-PWM) is obtained. When  $N_c < N$  the digital domain features two execution rates. For  $N_c = 1$  and  $N_c = 2$  multi-rate single- and double-sampled PWM (MR-(S/D)S-PWM) is obtained. In all of the considered control systems, both feedback and modulating signal sampling instants are assumed to be synchronized with w so that, within each carrier (modulation) period  $T_{pwm} = \frac{1}{f_{pwm}}$ , one of the sampling instants coincide with w = 0, while the others are equidistantly spaced across  $T_{pwm}$ , as illustrated in Fig. 2, for MR-DS-PWM and MS-PWM.

The filtered feedback signal  $i_f$  is subtracted from the reference set-point  $i_r$ . The resulting error signal e is forwarded to the current controller  $G_c$ , whose output is delayed by one control update period  $T_c = \frac{1}{f_c}$ , due to finite execution time. The voltage reference generated by the current controller is scaled to the range [0,1] and the resulting digital modulating signal  $m_s$  is used by PWM to perform the transition from digital to continuous domain. The signal  $m_s$  is held constant over one  $T_c$ , to obtain the modulating signal m. Intersections<sup>2</sup> between m and w define the switching signal x, which is the square waveform whose steady-state duty cycle D determines the operating point of the converter.

#### B. Conditions for Sampling the Switching Noise

Very steep edges of PWM voltage waveforms during commutations of the converter (high dv/dt), together with various parasitic LC elements (due to e.g., power switches nonidealities, long cables in industrial drives, etc), give rise to high frequency oscillations in the output waveforms, which is known as switching noise [2], [13]-[20]. This type of noise is strongly dependent on the hardware design and PCB layout, and might exhibit a wide range of spectral content and amplitude [19], of which waveforms in Fig. 3 are just some examples. In addition, sensing circuits may significantly impact the shape of the switching noise oscillations [17]. Being correlated with the feedback signal and non-stationary, [6], [7], the switching noise is very difficult to handle analytically. Following the methodology from [23], some basic principles about its propagation in multi-sampled systems are outlined in this article. As a starting point, systems where the switching noise oscillations decay within one sampling period are considered, so that maximum one sample per commutation can be corrupted (as in Fig. 3). Systems where this does not hold (due to e.g., less noise damping, higher switching and sampling frequencies, etc) bring additional complexity and will be the subject of future studies.

When the sampling instants occur during a time span where the above mentioned oscillations are present, switching noise



Fig. 3: Impact of switching noise on feedback acquisition. Sensed and sampled inductor current (normalized to peak-peak switching ripple component  $\Delta I_{PP}$ ) during open-loop operation of the system from Fig. 1 with N = 8 around:  $D = 0.75 = D_s$  for the switching noise with magnitudes (a) lower and (b) higher than  $\frac{\Delta I_{PP}}{2}$ ; and around (c)  $D = 0.625 \neq D_s$  for the switching noise with magnitude higher than  $\frac{\Delta I_{PP}}{2}$ .

may be introduced in the feedback. The operating points around which this happens are determined by N, the synchronization between the carrier w and the sampling instants, and the delays in the propagation path of the switching signal. For the considered synchronization between w and the sampling instants, these operating points, critical for switching noise sensitivity, are given by

$$D_s = mod\left(\frac{2h}{N} \pm 2\tau_{dr}, 1\right) \tag{1}$$

where  $h \in \mathbb{N}_0$ ,  $h \leq \frac{N}{2}$ ,  $\tau_{dr} = \frac{\tau_d}{T_{pum}}$ , and  $\tau_d$  is the total propagation delay of the switching signal, for example caused by dead-time<sup>3</sup> and driver circuits. Eq. (1) is derived by determining the operating points at which the switching instants coincide with the sampling instants. Note that each of the two signs  $(\pm)$  in (1) corresponds to one of the switching instants (turn-on or turn-off). Thus, if the switching noise oscillations are present only for one of the commutations<sup>4</sup>, depending on whether these are the turn-on or turn-off ones, instead of  $\pm$ , either + or - should be used in (1). The range of operating points around  $D_s$ , at which the switching noise is sampled, is determined by the duration (damping) of the switching noise oscillations. As an example, the switching noise sampling around  $D = D_s$  is illustrated in Fig. 3 (a) and (b), for two different switching noise magnitudes. On the contrary, as illustrated in Fig. 3 (c), when  $D \neq D_s$ , switching noise is not sampled. It is interesting to note that for (S/D)S-PWM, (1) predicts the well-known switching noise sensitivity for small and/or large duty cycles.

<sup>&</sup>lt;sup>2</sup>For MS-PWM, a proper logic is implemented to prevent multipleswitching and pulse-skipping [5].

<sup>&</sup>lt;sup>3</sup>In closed loop operation dead-time delays the switching instants for a value equal to half of the imposed dead-time value.

<sup>&</sup>lt;sup>4</sup>This might happen e.g., when one of the commutations is soft.

## C. Specific Properties of MS-PWM

Whether or not the sampled switching noise will affect system performance depends on the adopted feedback filtering and control strategy. As shown in [23], unless properly filtered, samples corrupted by the switching noise may significantly degrade performance of (S/D)S-PWM and MR-(S/D)S-PWM. On the other hand, this is not necessarily the case for MS-PWM. Namely, as in MS-PWM both the feedback and the modulating signal are oversampled, a few specific switching noise propagation properties may arise.

Since in a digital system the switching noise can be considered as an impulse<sup>5</sup>, some insight about its propagation from feedback to the modulator input can be obtained by analyzing the impulse response of the digital part. However, its propagation through the entire control loop cannot be analyzed this simply, due to the non-linearity of MS-PWM. For example, if the impulse response of the controller and the feedback filter decay by the instant at which the modulating waveform intersects with the carrier, switching noise may be completely blanked by the system itself. For a purely proportional control, this means that if the switching noise is sampled at an instant other than the one directly preceding the intersection<sup>6</sup>, it will not have any impact on the response. A similar effect, illustrated in Fig. 4 (a), can be observed in systems with high-frequency proportional dominant controllers, such as proportional-integral (PI) and proportionalresonant (PR), where the integral (resonant) action is limited well-below the cross-over frequency of the control loop. There, the propagation of switching noise, which is a highfrequency disturbance for the system, is mostly determined by the proportional gain of the controller. As a consequence, and due to the modulator decimation effect, the switching noise sensitivity of MS-PWM control without feedback filters may significantly vary, depending on which sample within the carrier period is corrupted.

Next, it may happen that the impact of noise is masked by the vertical intersections between the modulating signal and the carrier, as illustrated in Fig. 4 (b) and explained below. Due to the imposed synchronization between the carrier and the sampling instants, vertical intersections may occur only around certain operating points, critical for modulator linearity

$$D_c = \frac{2p}{N} \tag{2}$$

where  $p \in \mathbb{N}$ ,  $p < \frac{N}{2}$  [5]. It is interesting to note that for  $\tau_D = 0$ ,  $D_c$  coincides with  $D_s$  (see (1)), i.e., the operating points critical for switching noise sensitivity are at the same time critical for modulator linearity. Depending on the total delay in the propagation path of feedback and switching signals, switching ripple component of the modulating signal may periodically trigger vertical intersections around  $D_c$ , resulting in a set of modulator related non-linear effects [5], [8], [11]. For example, counter-phase vertical intersections



Fig. 4: Modulating signal and carrier waveforms around  $D = D_c = D_s$  for MS-PWM with N = 8 and high-frequency dominant controller, illustrating phenomena that cause specific switching noise propagation properties of MS-PWM without filters: (a) the corrupted sample (shown in red color) is not the one directly preceding the switching instant; (b) counter-phase vertical intersections exist between m and w; (c) vertical intersections are turned into horizontal ones by high noise magnitude.

prevent modulation of one or both edges of the switching signal, resulting in reduced or zero modulator gain [5], [8]. Nevertheless, this non-linearity may have a positive effect on the noise propagation. Namely, counter-phase vertical intersections can also prevent the noise corrupted samples to have an impact on the system performance (see Fig. 4 (b)), provided that the noise magnitude is small enough. On the contrary, high-enough switching noise magnitude is sufficient to turn vertical into horizontal intersections, as illustrated in Fig. 4 (c), which increases the sensitivity of MS-PWM to switching noise.

The impact of the above explained phenomena is illustrated in subsequent sections, using simulations and experiments. Nonetheless, general statements about switching noise sensitivity of MS-PWM without specific feedback filters, are difficult to make, due to a set of non-linear effects related to modulator, switching noise and their interaction. Thus, to enhance the modulator linearity and ensure switching noise immunity, this article proposes the use of MS-PWM in combination with advanced feedback filtering strategies, as explained in the following section.

#### **III. SWITCHING NOISE SUPPRESSION**

In order to enhance system's noise suppression capabilities, different approaches have been investigated. One of those is placing a moving average filter (MAF) in the loop, which simply uses N latest samples to obtain the averaged value of the feedback signal over one  $T_{pwm}$ . Its z-domain transfer function is

$$G_{MAF}(z) = \frac{1}{N} \sum_{q=0}^{N-1} z^{-q}.$$
(3)

Even though MAF is often reported in the literature as an effective noise-suppression solution [2], it is shown in [23]

<sup>&</sup>lt;sup>5</sup>This is valid in systems where the switching noise oscillations decay within one  $T_s$ , such as those from Fig. 3, that are considered in this article.

<sup>&</sup>lt;sup>6</sup>In systems with one-step computational delay, the sample of the modulating signal that is affected by the switching noise is delayed by  $T_c$  with respect to the switching noise affected sample of the feedback signal.



Fig. 5: Working principle of (a) MED and (b) ripple removal (RR) + MED and their capability to suppress the switching noise with magnitude higher than half of the peak-peak switching ripple component. MED fails to suppress the switching noise, while RR + MED successfully suppresses it. The dashed boxes highlight the samples that participate in the filtering at the time instant for which the illustration is given.

that, when a greater portion of the samples being averaged is corrupted, it may fail to suppress the switching noise and even bring in additional sensitivity for MR-(S/D)S-PWM control, which is not present for (S/D)S-PWM. For systems where no more than one sample per commutation is switching noise corrupted, noise suppressing capabilities of MR-(S/D)S-PWM with MAF are determined by the switching noise magnitude and N. Thus, even for higher N (such as N = 32), MR-(S/D)S-PWM with MAF may exhibit worse performance than typically used (S/D)S-PWM, if the switching noise magnitude is high enough.

Recognizing the impulsive character of the switching noise, to overcome this limitation of MAF, a median-based feedback filtering, whose basic principles are outlined below, is proposed in [23] as an effective way to suppress switching noise in MR-(S/D)S-PWM systems. Analysis of its implementation within MS-PWM systems is the focus of this article.

#### A. Median-based Feedback Filtering

The median filter (MED) is a non-linear rank filter that relies on sorting N latest samples to obtain the median over one  $T_{pwm}$  [20], [24], [25]. Thus, at time instant  $k_sT_s$ , for a given input signal  $i_s$ , the output of MED,  $i_f$ , is calculated as

$$i_f[k_s] = MED(i_s[k_s], ..., i_s[k_s - (N-1)]).$$
 (4)

When the multi-sampling factor is even, two middle samples are averaged to obtain the median. Provided that the magnitudes of the switching noise oscillations are lower than half of the peak-peak current ripple, the switching noise can be successfully suppressed using MED, as explained in [23]. Otherwise, even with MED, the switching noise may be introduced in feedback, which is illustrated in Fig. 5 (a).

To solve this, [23] proposed adding a ripple removal filter before MED. In this way, it is ensured that the switching ripple does not affect ranking within MED and thus, that the switching noise is successfully suppressed even if its magnitude is larger than half of the peak-peak current ripple, as illustrated in Fig. 5 (b).



Fig. 6: Simulated phase frequency response measurements of MAF, MED and RRR + MED. In the frequency range of interest, all of the considered feedback filters are well approximated by the delay  $\tau_{fbd} = \frac{T_{pwm}}{T_{pd}}$ .

Regarding ripple removal filter, a possible option is a predictive one, which is based on sample-by-sample ripple reconstruction algorithm [10]. Although it may offer very fast response, the precise knowledge of the converter parameters is necessary for its implementation. As an alternative, in this article, the repetitive ripple removal (RRR) from [9] is used

$$G_{RRR}(z) = \frac{(1+R)\left(1 - \left(z^{-N} - \frac{1}{N}\sum_{q=1}^{N}z^{-q}\right)\right)}{1 - \left(z^{-N} - \frac{1}{N}\sum_{q=1}^{N}z^{-q}\right) + R}$$
(5)

where gain R defines the settling time of the RRR [9].

The effectiveness of the proposed feedback filtering strategy, RRR + MED, in suppressing the switching noise in MR-(S/D)S-PWM and MS-PWM systems is verified in simulations and experiments in Section IV and V. Other feedback filtering strategies, MAF and MED, as well as control strategies without any feedback filters are also considered for comparison. The dynamic performance of the different strategies is briefly addressed below, where the benefits of using MS-PWM with respect to MR-DS-PWM and DS-PWM are explained. This is further experimentally examined in Section V.

#### B. Dynamic Performance of Different Strategies

The delay present in the control loop,  $\tau_{cld}$ , is a limiting factor for achieving robust high bandwidth control [1]. For the same control loop cross-over frequency, lower values of  $\tau_{cld}$ increase the phase margin, which results in better transient performance in terms of reference tracking and disturbance rejection. Thus, small-signal dynamic performance of different strategies can be compared by comparing  $\tau_{cld}$ , which is addressed in this subsection. Given the control system from Fig. 1, main contributors to  $\tau_{cld}$  are the digital PWM, feedback filters and finite control algorithm computation time.

From the small-signal point of view, PWM can be approximated as [1], [8]

$$G_{pwm}(s) \approx e^{-s\frac{T_c}{2}} \tag{6}$$

where s is the complex variable of the Laplace transform. For the purpose of investigating their impact on phase margin, all of the considered feedback configurations can be approximately represented as

$$G_{fb}(s) \approx e^{-s\tau_{fbd}},$$
 (7)

where  $\tau_{fbd} = 0$  in case no feedback filters are used, and  $\tau_{fbd} = \frac{T_{pwm}}{2}$  in case of MAF, MED, and RRR<sup>7</sup> + MED [2], [20], [25]. Since MED is a non-linear filter, its frequency response is strictly not defined and cannot be given analytically. However, for assessing its impact on control loop's small-signal dynamics, MED can be represented as the delay equal to  $\frac{N}{2}T_s = \frac{T_{pwm}}{2}$  [20], [25]. Validity of such a representation in the frequency range below the switching frequency was verified using simulated frequency response measurements<sup>8</sup> in MATLAB Simulink. The results are shown in Fig. 6, where in addition to MED, simulated phase frequency response measurements of MAF and RRR + MED are also included. As can be seen, in terms of phase and in the frequency range of interest, all of the considered feedback filtering strategies are well approximated by (7).

Considering one step computational delay [1], in addition to delays from modulation and filtering, the total control loop delay  $\tau_{cld}$  can be calculated as

$$\tau_{cld} = \frac{3T_c}{2} + \tau_{fbd}.$$
(8)

Since in MS-PWM control  $T_c = T_s < \frac{T_{pwm}}{2}$ ,  $\tau_{cld}$  is lower than in MR-(S/D)S-PWM control with the same feedback configuration. In addition, since in MS-PWM with either MAF, MED or RRR + MED,  $\tau_{cld}^{MS-PWM} = \frac{(3+N)}{2N}T_{pwm}$ , for  $N \ge 6$ , the total control loop delay is lower than in DS-PWM control without any filters, where  $\tau_{cld}^{DS-PWM} = \frac{3}{2}T_{pwm}$ . Thus, MS-PWM with either MAF, MED or RRR + MED, outperforms not only MR-(S/D)S-PWM with the same feedback filtering strategy, but also, for  $N \ge 6$ , DS-PWM without any filters. This is an important remark which shows that in addition to high-noise immunity offered by the proposed feedback filtering strategy, high control loop bandwidth and high phase margin can also be ensured by using MS-PWM. This is verified experimentally in Section V.

#### C. Design Guidelines

This subsection aims to briefly discuss design consideration steps to determine key parameter values, N and R, of the proposed control strategy. Regarding the value of N, the switching noise suppression capabilities of RRR + MED are not expected to be impacted by it. This is because the proposed feedback filtering strategy is designed to cancel out disturbance of impulsive nature. Nevertheless, to more effectively suppress white noise and aliasing, it is of interest to choose higher N [2], [6], [7]. Moreover, from the dynamic performance point-of-view, though the delay introduced by RRR + MED does not depend on N (see (7)) [20], [25], it is of interest to choose higher N to reduce the modulation delay (see (6)) [8]–[10]. Thereby, hardware capabilities of the adopted control platform, in terms of its computational power and the speed of the ADC, typically define an upper limit for the value of N. This of course means that, for PESs with high  $f_{pwm}$ , high values of N may be difficult to achieve.

TABLE I: Hardware and Control Parameters of the Tested Converter

Parameter	label	value	unit
Input dc voltage	E	120	V
Filter inductance	L	1.5	mH
Switching frequency	$f_{pwm}$	10	kHz
Fundamental frequency	$f_1$	50	Hz
Sampling frequency	$f_s$	80	kHz
Control update frequency	$f_c$	$\{20, 80\}$	kHz
Crossover frequency	$f_{cr}$	1	kHz
Proportional gain	$k_p$	9.2	Ω
Integral / resonant gain	$k_i$	5.6	$k\Omega/s$

Regarding the value of R, to achieve a lower settling time of the RRR, it is of interest to choose higher R [9]. However, to ensure a negligible phase lag of the RRR below  $f_{pwm}$ , which is favorable from the small-signal dynamics point-of-view, Rmust be set relatively low, as explained in [9]. There, it is recommended to choose R in the range 0.125-0.25, resulting in RRR's settling time in the range  $(10 - 20) T_{pwm}$ . In this article, R = 0.125 is used.

#### **IV. SIMULATION RESULTS**

#### A. Simulink Implementation

To evaluate and compare switching noise suppression capabilities of different feedback filtering and control strategies, the system from Fig. 1 is implemented in MATLAB Simulink environment, using Simscape Electrical Specialized Power Systems Library. A buck converter and a full-bridge inverter with the hardware and control loop parameters from Table I are used as examples<sup>9</sup> for validations during dc and sinusoidal ac operation, respectively. A constant voltage load is used at the output in both regimes. MR-DS-PWM and MS-PWM control are implemented with N = 8 and the feedback configurations from Section III are considered. As a standard example, PI current controller is used [1] for validations during dc operation

$$G_c(z) = k_p + k_i T_c \frac{z}{z-1} \tag{9}$$

where proportional gain  $k_p$  is chosen to achieve the desired crossover frequency  $f_{cr} = 0.1 f_{pwm}$  and integral gain  $k_i = 2\pi f_{cr} 0.1 k_p$  is chosen so that its impact is limited to low frequencies only. This sets a constant crossover frequency, while, depending on the feedback configuration and control strategy, the phase margin is changed due to digital delays and feedback filters. For validations during the sinusoidal ac operation, PR current controller is used

$$G_c(z) = k_p + k_i T_c \frac{1 - \cos\left(2\pi f_1 T_c\right) z^{-1}}{1 - 2\cos\left(2\pi f_1 T_c\right) z^{-1} + z^{-2}}$$
(10)

where  $f_1$  is the fundamental frequency to be tracked, and  $k_p$ ,  $k_i$  are the same as before.

Switching noise is emulated by including parasitic capacitances and inductances of the power switches in the simulation model. More details about obtaining switching noise

<sup>&</sup>lt;sup>7</sup>As shown in [9], RRR brings a negligible phase lag below the switching frequency and thus has hardly any impact on small-signal dynamics of interest.

<sup>&</sup>lt;sup>8</sup>Describing function modelling approach can be used for further validations, which is left for future work.

<sup>&</sup>lt;sup>9</sup>Simulations were performed also for other parameters, such as higher  $f_{pwm}$ , and the conclusions remained the same.



Fig. 7: Variance of the duty cycle for MR-DS-PWM control with N = 8 obtained using Simulink model of the buck converter with parameters from Table I in four different scenarios: (a) only white noise is present and  $\tau_{dr} = 0$ ; (b) white + switching noise from Fig. 3 (a) is present and  $\tau_{dr} = 0$ ; (c) white + switching noise from Fig. 3 (b) and (c) is present and  $\tau_{dr} = 0$ ; (d) white + switching noise from Fig. 3 (b) and (c) is present and  $\tau_{dr} = 0.015$ .

in simulations are found in [23]. Simulations were run for different values of the parasitic elements, such that different damping and magnitude of the switching noise oscillations are obtained. In this section, due to space limitations, the results are presented only for the switching noise obtained with the same settings as those used to obtain waveforms in Fig. 3.

White noise, with a comparably small power, obtained from a band-limited white noise generator, is also added in the simulation. The noise variance is set to  $1.4 \cdot 10^{-3}$  A<sup>2</sup>. In addition, PWM and ADC quantization is included, with the quantization levels<sup>10</sup> equal to those of the prototype from Section V.

## B. Duty Cycle Variance for DC Operation

Switching noise sensitivity and suppression capabilities during dc operation are evaluated as follows. For each considered case, the current reference is set to 4 A and the sweep of the output voltage is performed, such that the operating point changes from D = 0.01 to D = 0.99. For each operating point, the applied duty cycle is detected over 50 ms of the steady state operation, after which its variance is calculated. In this way, the duty cycle variance as a function of the operating point is obtained, and used as an indicator of noise sensitivity.

In Fig. 7 and Fig. 8 the results for MR-DS-PWM and MS-PWM control are shown, where different colors denote different feedback configurations: without any filters (blue),



Fig. 8: Variance of the duty cycle for MS-PWM control with N = 8 obtained using Simulink model of the buck converter with parameters from Table I in four different scenarios: (a) only white noise is present and  $\tau_{dr} = 0$ ; (b) white + switching noise from Fig. 3 (a) is present and  $\tau_{dr} = 0$ ; (c) white + switching noise from Fig. 3 (b) and (c) is present and  $\tau_{dr} = 0$ ; (d) white + switching noise from Fig. 3 (b) and (c) is present and  $\tau_{dr} = 0.015$ .

MAF (red), MED (yellow), RRR + MED (green). The results are given for four different scenarios, in terms of type of noise and delay present in the propagation path of the switching signal:

- Scenario A: only white noise is present and  $\tau_{dr} = 0$ ;
- Scenario B: the white noise and the switching noise corresponding to Fig. 3 (a) are present and  $\tau_{dr} = 0$ ;
- Scenario C: the white noise and the switching noise corresponding to Fig. 3 (b) and (c) are present and τ<sub>dr</sub> = 0;
- Scenario D: the white noise and the switching noise corresponding to Fig. 3 (b) and (c) are present and  $\tau_{dr} = 0.015$ .

Scenario A, for which the results are shown in Fig. 7 (a) and Fig. 8 (a), illustrates white noise propagation properties and is intended as a baseline. Nevertheless, it also reveals an interesting property of MS-PWM without any filters. Namely, very high noise attenuation is observed around  $D = D_c$ , due to vertical intersections between m and w, which cause the modulator to exhibit reduced- and zero-gain [5], [8]. Other than this, white noise attenuation for all considered strategies can be analyzed using methods derived in [6], [7].

In the other scenarios, for which the results are shown in Fig. 7 (b)-(d) and Fig. 8 (b)-(d), in addition to white noise, switching noise is present as well. Still, around the operating points that are away from  $D_s$ , white noise is dominant in the feedback signal, and thus the resulting noise attenuation levels are practically the same as in Fig. 7 (a) and Fig. 8 (a). Around  $D_s$  however, switching noise is dominant in the feedback signal and thus the reasoning presented in previous

<sup>&</sup>lt;sup>10</sup>The quantization levels are such that the quantization induced limitcycling is negligible [26]. This allows the analysis of the switching noise to be decoupled from the quantization noise.

sections has to be applied in order to describe noise sensitivity and suppression capabilities of the considered systems, as addressed below.

Let us firstly explain the results in scenarios B and C, where  $\tau_{dr} = 0$ . For DS-PWM without any filters (blue results in Fig. 7 (b) and (c)), duty cycle variance increases as *D* approaches 0 and 1. This well-known sensitivity region of DS-PWM is in agreement with (1). For MR-DS-PWM and MS-PWM the number of the switching noise sensitive operating points increases with respect to DS-PWM. For N = 8, according to (1),  $D_s \in \{0, 0.25, 0.5, 0.75, 1\}$ .

For MS-PWM without any filters, (blue results in Fig. 8 (b) and (c)), due to modulator non-linearity, specific switching noise propagation properties arise, as explained in Section II.C. Namely, in both scenario B and C, around  $D_s = 0.5$ , due to the corrupted sample not being the one that directly precedes the switching instant (see Fig. 4 (a)), the system is not sensitive to switching noise. Around  $D_s = 0.25$  and  $D_s = 0.75$ , on the other hand, very low duty cycle variance in scenario B is a consequence of vertical intersections between m and w, which mask the impact of switching noise (see Fig. 3 (b)). However, around the same operating points switching noise sensitivity is high in scenario C, because the switching noise magnitude in that case is sufficient to turn vertical into horizontal intersections (see Fig. 3 (c)).

Regarding the switching noise suppression capabilities of MAF, MED and RRR + MED, from the presented results it can be observed that for each of the filtering strategies, they remain the same regardless of whether MR-DS-PWM or MS-PWM control strategy is used. With MAF, the duty cycle variance exhibits very high peaks around  $D_s$  in both scenarios B and C, due to the averaging within MAF being affected by the switching noise-corrupted samples. This illustrates the ineffectiveness of MAF in suppressing switching noise, as it does not feature a mechanism for discarding the noise-corrupted samples.

When MED without ripple removal is used, the switching noise is successfully suppressed in scenario B, since the magnitude of the switching noise oscillations is lower than half of the peak-peak current ripple. However, in scenario C, the switching noise suppression is very poor around  $D_s \in \{0.25, 0.5, 0.75\}$ , due to the fact that the magnitude of the switching noise oscillations is greater than half of the peak-peak current ripple, and the samples corrupted by the switching noise affect the median.

When RRR + MED is used, the peaks of the duty cycle variance that are observed around  $D_s$  in both scenarios B and C are significantly lower compared to cases when either MAF or MED without ripple removal are used in feedback. The small residual peaks are assumed to be the consequence of the RRR, which does not ideally eliminate the switching ripple. Higher performance ripple removal techniques will be addressed in future work.

The results for scenario D, where  $\tau_{dr} = 0.015$ , are shown in Fig. 7 (d) and Fig. 8 (d), for MR-DS-PWM and MS-PWM control. For each considered feedback filtering strategy, the number of the switching noise sensitivity peaks is doubled with respect to the results obtained with  $\tau_{dr} = 0$ . Moreover,



Fig. 9: Variance of the duty cycle during sinusoidal ac operation for (a) MR-DS-PWM and (b) MS-PWM control with N = 8 obtained using Simulink model of the current-controlled voltage-loaded full-bridge inverter with parameters from Table I. White + switching noise from Fig. 3 (b) and (c) is present and  $\tau_{dr} = 0$ . Variance is calculated after removing fundamental frequency component multiples from the spectrum of the detected duty cycle.

the peaks of the switching noise sensitivity are observed at the operating points that are shifted by  $\pm 2\tau_{dr}$  with respect to those observed with  $\tau_{dr} = 0$ . Both phenomena are predicted by (1) and are due to the fact that the non-zero delay in the propagation path of the switching signal shifts the switching instants, i.e., instants at which the switching noise is generated, with respect to the sampling instants. Other than this, the switching noise suppression capabilities of the considered systems are qualitatively the same as those with  $\tau_{dr} = 0$ , shown in Fig. 7 (c) and Fig. 8 (c) and discussed above.

According to the presented results, the proposed feedback filtering strategy comprising RRR + MED successfully suppresses the switching noise in all considered scenarios and also offers good white noise attenuation properties, outperforming thereby the conventionally used MAF. In addition, its effectiveness remains the same regardless of whether MR-DS-PWM or MS-PWM control strategy is adopted. However, as explained in Section III.B and verified experimentally in Section V.B, for the same control loop bandwidth, MS-PWM offers higher phase margin, which is why MS-PWM with RRR + MED is preferable to MR-DS-PWM with RRR + MED, but also to DS-PWM without any filters.

## C. Duty Cycle Variance for AC Operation

Switching noise sensitivity and suppression capabilities during sinusoidal ac operation are evaluated as follows. For each considered case, the current reference magnitude is set to 6 A and the sweep of the output voltage magnitude is performed, such that the modulation index M changes from M = 0.6 to M = 0.9. Dead-time is set to zero, to exclude it as a source of distortion and focus on the distortion due to the switching noise. The switching noise from Fig. 3 (b) and (c) is present and  $\tau_{dr} = 0$ . For each modulation index, the applied duty cycle is detected over 160 ms of the sinusoidal ac operation with  $f_1 = 50$  Hz. After removing the components that are multiples of the fundamental frequency from the spectrum of the detected duty cycle, its variance is calculated. In this way, the duty cycle variance as a function of the modulation index is obtained, and used as an indicator of noise sensitivity.

The results are shown in Fig. 9 (a) and (b) for MR-DS-PWM and MS-PWM control, where different colors denote different feedback configurations, same as before. For DS-PWM without filters, no distortion is observed, since the modulation index is such that operation around very high and very low operating points, where the switching noise is sampled for DS-PWM (see (1)), is not present. MS-PWM without filters features increased variance around M = 0.75, due to combined effect of switching noise and modulator related non-linearities [5], as discussed in Section II.C. With MAF in either MR-DS-PWM or MS-PWM, high variance is observed when M is close to 0.75, since then the peaks of the modulating signal fundamental component coincide with the operating points where the switching noise is sampled. This makes the impact of switching noise pronounced, due to the modulating signal's slope around the critical operating points being low. Poor switching noise suppression around M = 0.75is also observed when MED without ripple removal is used, since in the tested scenario, the magnitude of the switching noise oscillations is greater than half of the peak-peak current ripple, and the samples corrupted by the switching noise affect the median. With RRR + MED, no switching noise sensitivity peaks around M = 0.75 are observed neither for MR-DS-PWM nor for MS-PWM. A slight increase in the variance that is observed with an increase of M is due to the sideband components in the switching ripple waveform being higher, and thus the RRR being less effective in removing them [9]. Nevertheless, with RRR + MED, the switching noise is successfully suppressed for all considered modulation indices, both for MR-DS-PWM and MS-PWM, validating thereby the effectiveness of the proposed feedback filtering strategy during ac operation. Benefits of MS-PWM with RRR + MED compared to MR-DS-PWM with RRR + MED, in terms of superior dynamic performance, are verified experimentally in Section V in the manuscript.

#### V. EXPERIMENTAL RESULTS

## A. Test Setup

For the experimental validation, a laboratory prototype of a current-controlled voltage-source converter is realized with the hardware and control parameters from Table I. The picture and block diagram of the setup are shown in Figs. 10-11.

The setup consists of three main parts, denoted by three different colors in Fig. 11. Red part represents the tested converter, which can be configured as half- or full-bridge, and is realized using the SiC modules from Imperix [27]. An inductive filter is used and, depending on the position of selector  $s_1$ , either a constant voltage load or a resistive load connected in parallel with the output capacitor is used. Inductor current is sensed using a LEM based current transducer.

The control system, denoted by blue color in Fig. 11, is implemented on Imperix B-Box Embedded Control Module, using both the DSP and FPGA that are available on the board. The 16 bit ADC, the digital feedback filters and the current controller are implemented on the DSP. Due to the algorithm computation time, the modulating signal update is delayed by one control period,  $T_c$ . The digital modulating



Fig. 10: Test-setup used for experimental validation: 1) input dc power supply TDK/Lambda GEN300-17; 2) SiC modules from Imperix; 3) Boom Box controller; 4) laptop; 5) resistive load; 6) inductor and sensing circuits; 7) electronic load EA-EL 9750-120 B used as a constant voltage load; 8) Tektronix MS056 oscilloscope.



Fig. 11: Block diagram of the test-setup used for experimental validation.

signal,  $m_s$ , is forwarded to the FPGA via Imperix sandbox, which serves as an interface between DSP and FPGA, and ensures a proper synchronization. The PWM is coded in VHDL and implemented on the FPGA, with the PWM clock that runs at  $f_{clk} = 125$  MHz. The switching signal, x, is sent back to DSP where dead-time equal to 0.8 us is realized. For evaluating noise sensitivity, duty cycle, d, is detected on the FPGA, forwarded to DSP and exported using Imperix Cockpit. Post-processing, denoted by yellow color in Fig. 11, is performed in MATLAB. For examining transient response and waveform distortion, inductor current is acquired with 125 MS/s rate, using Tektronix TCP202 current probe and MS056 oscilloscope.

#### B. DC Operation

To evaluate the performance of the previously discussed control strategies during dc operation, the prototype from Fig. 11 is configured as a constant voltage-loaded buck converter. A PI current controller is used, designed as per Section IV.A.

The working principle of the proposed feedback filtering strategy is illustrated in Fig. 12 (a) and (b) for MR-DS-PWM and MS-PWM control. The sampled feedback signal,  $i_s$ , the output of the RRR,  $i_{rr}$ , and the filtered signal after RRR + MED (that is decimated for MR-DS-PWM),  $i_f$ , are acquired during the steady-state closed-loop operation around



Fig. 12: Experimental verification of the working principle of RRR + MED during closed-loop steady-state dc operation of the current-controlled voltage-loaded buck converter around one of the operating points where the switching noise is sampled,  $D \approx 0.3$ , for (a) MR-DS-PWM and (b) MS-PWM. Sampled inductor current,  $i_s$ , the output of the RRR,  $i_{rr}$  and the filtered signal after RRR and MED,  $i_f$ , are exported from DSP.



Fig. 13: Experimentally obtained duty cycle variance for (a) MR-DS-PWM and (b) MS-PWM control with N = 8, obtained using the current-controlled voltage-loaded buck converter with parameters from Table I. Different colors denote different feedback configurations.

one of the operating points where the switching noise is sampled,  $D \approx 0.3$ , and exported from the DSP. As seen, the RRR successfully removes the switching ripple from the sampled feedback signal, leaving only impulses generated by the switching noise. These are then successfully removed by the MED.

In order to obtain duty cycle variance as a function of the operating point, a procedure similar to the one described in Section IV is used. The electronic load is programmed to perform the sweep of the output voltage values, such that the operating point changes from D = 0.01 to D = 0.99. For each operating point, the variance of the duty cycle detected during 50 ms of the steady-state operation is calculated.

The experimentally measured duty cycle variances for MR-DS-PWM and MS-PWM control with the feedback filtering strategies from Section III are shown in Fig. 13. The results for DS-PWM and MS-PWM control without any filters are also included. As seen, DS-PWM exhibits very high switching noise sensitivity for small *D*, whereas it is only slightly sensitive for large *D*. This is due to the shape of the switching noise oscillations coming out of the sensing circuit, which are such that the ones corresponding to turn-off commutations hardly exists whereas the turn-on ones are very poorly damped.



Fig. 14: Dynamic performance comparison of the current-controlled voltageloaded buck converter with different control strategies and feedback configurations. Experimentally measured inductor current in response to (a) the step change of the current reference (b) the sudden change of the load voltage. The switching ripple is filtered out for a better visualisation. Residual oscillations at approximately 7 kHz that are visible in the waveforms in (b) are due to the dynamics of the electronic load EA-EL 9750-120 B that was used for triggering the load transient. (c) Loop gain obtained analytically and using simulated frequency response measurements. Due to reduced digital delays, the proposed control strategy with MS-PWM, RRR, and MED, outperforms not only MR-DS-PWM, but also DS-PWM without any filters.

For MS-PWM without any filters, high noise attenuation around  $D_c$  is observed, due to vertical intersections between m and w, as explained in Section II.C and IV.B. Moreover, negligible switching noise sensitivity is exhibited in the tested scenario. This is an interesting result which illustrates that, contrary to what is commonly assumed, MS-PWM without feedback filters does not necessarily exhibit high switching noise sensitivity. Nevertheless, as explained in Section II.C, switching noise sensitivity of MS-PWM without feedback filters is difficult to characterize in a general case, due to a set of non-linear effects related to modulator, switching noise and their interaction.

MAF in either MR-DS-PWM or MS-PWM control fails to suppress the switching noise and strongly deteriorates performance with respect to DS-PWM and MS-PWM without any filters. For MR-DS-PWM and MS-PWM control with MED only, the presence of the switching noise sensitivity peak is clearly visible for low values of D. This illustrates how MED without ripple removal may be ineffective in mitigating the switching noise, due to the ranking being affected by the switching ripple. With RRR + MED the switching noise is successfully suppressed for the whole range of operating points. Moreover, white noise suppression capabilities approach those obtained with MAF. As seen, the effectiveness of the proposed feedback filtering strategy in suppressing the switching and white noise is the same for MR-DS-PWM an MS-PWM control strategy. Therefore, from the noise suppression point of view, MR-DS-PWM and MS-PWM control with RRR + MED both outperform conventionally used DS-PWM without any filters, MR-DS-PWM with MAF, as well as MS-PWM with MAF. However, an important benefit of MS-PWM with RRR + MED with respect to MR-DS-PWM with RRR + MED is considerably better dynamic performance, featured by high control loop bandwidth and high phase margin, as explained in Section III.B and further examined below.

To evaluate the dynamic performance, a step change of the current reference from 2 A to 8 A is imposed, and the inductor current is measured using the oscilloscope. The results are shown for DS-PWM without filters, MR-DS-PWM and MS-PWM with MAF and RRR + MED. Constant voltage load is set to achieve operation around D = 0.45, where the switching noise is not sampled (see Fig. 13), so as to observe the step response without any jittering. For a better visualization, the switching ripple is removed from the data acquired by the oscilloscope and the results are plotted in Fig. 14 (a). From the presented results it can be observed that the step responses obtained with MAF and RRR + MED coincide, both for MR-DS-PWM and MS-PWM. This is in accordance with the reasoning from Section III.B, where the considered feedback filtering strategies are approximated as the same delay  $(\tau_{fbd} = \frac{T_{pwm}}{2})$ . Due to this delay, dynamic performance of MR-DS-PWM significantly deteriorates with respect to DS-PWM, which results in step responses with high overshoot. On the contrary, despite the delay introduced by the feedback filtering, the step responses for MS-PWM exhibit no overshoot, owing to the reduced computation and modulation delay achieved by MS-PWM, as explained in Section II.C.

As an additional verification of the dynamic performance benefits that the proposed control strategy offers, inductor current in response to the sudden change of the load voltage from 80 V to 40 V is experimentally measured using oscilloscope. The current reference is set to 3 A. The results are shown in Fig. 14 (b), for the same strategies and parameter settings as for the results in Fig. 14 (a). For a better visualization, the switching ripple is removed from the data acquired by the oscilloscope. Residual oscillations at approximately 7 kHz that are visible in the waveforms in Fig. 14 (b) are due to the dynamics of the electronic load EA-EL 9750-120 B that was used for triggering the load transient. The results in Fig. 14 (b) clearly show that MS-PWM with RRR + MED features higher load disturbance rejection capabilities than MR-DS-PWM with the same feedback filtering strategy. obtained analytically and using simulated frequency response measurements is shown in Fig. 14 (c), for the same strategies and parameter settings as for the results in Fig. 14 (a) and (b). As seen, significant improvement of the phase margin (PM) is obtained for MS-PWM (PM=  $64^{\circ}$ ), compared to both MR-DS-PWM (PM=  $57^{\circ}$ ) and DS-PWM (PM=  $43^{\circ}$ ). The results in Fig. 14 clearly illustrate dynamic performance benefits of the proposed strategy, featuring MS-PWM with RRR + MED, which outperforms not only MR-DS-PWM, but also conventionally used DS-PWM without filters.

According to all of the above presented, a great consistency between experimental and simulation results is observed, which further illustrates validity of the performed analyses and proposed methodology, described in Section II and III. The presented validations for dc operation demonstrate that MS-PWM with RRR + MED is a robust control strategy that ensures high noise immunity and high dynamic performance. Its effectiveness in ac operation is demonstrated next.

#### C. AC Operation

For validations during sinusoidal ac operation, the prototype from Fig. 11 is configured as a full-bridge voltage-source converter with an inductive output filter and a resistive load connected in parallel with the output capacitor<sup>11</sup>. PR current controller is used, designed as per Section IV.A. For the subsequent validations, the inductor current reference is set to  $i_r = 7.5$  A, so that the peaks of the modulating signal fundamental component coincide with the operating points where the switching noise is sampled. In this way, the slope of the inductor current around the operating points critical for switching noise easier to visualize. Experimental measurements are performed for MR-DS-PWM and MS-PWM control and the conclusions remained the same. Due to space limitations, the results are presented only for MS-PWM.

The working principle of RRR + MED during sinusoidal ac operation is illustrated in Fig. 15, where the sampled feedback signal,  $i_s$ , the output of the RRR,  $i_{rr}$ , and the filtered signal after RRR and MED,  $i_f$ , are shown. The data is directly exported from the DSP. According to the presented results, as in case of dc operation, the RRR successfully removes the switching ripple from the sampled feedback signal, leaving only impulses generated by the switching noise. These are then successfully removed by the MED.

To illustrate the benefits of using RRR + MED with respect to MAF, the inductor current is acquired by the oscilloscope for both feedback filtering strategies and compared in Fig. 16. For a better visualization, the switching ripple is removed from the plotted data. As seen, a considerable distortion around the current's fundamental cycle minimum and maximum is observed with MAF. This distortion is not present with RRR + MED. Since, as previously explained and illustrated in Fig. 15, in the tested regime the operating points where the switching noise is sampled coincide with the peaks of the current's

To further elaborate on dynamic performance, the loop gain

<sup>&</sup>lt;sup>11</sup>Sinusoidal ac operation with different types of load, such as constant voltage load, was tested in simulations, and the conclusions remained the same as those presented in this section.



Fig. 15: Experimental verification of the working principle of RRR + MED during closed-loop sinusoidal ac operation with M = 0.75 for MS-PWM control. Sampled inductor current,  $i_s$ , the output of the RRR,  $i_{rr}$  and the filtered signal after RRR + MED,  $i_f$ , are exported from DSP.

fundamental component, it is clear that the distortion is due to ineffectiveness of MAF in suppressing the switching noise. This demonstrates that, especially for lower N and higher switching noise magnitudes, MAF may bring a detrimental impact not only during dc, but also during ac operation. On the other hand, RRR + MED is validated to successfully suppress the switching noise.

#### VI. CONCLUSIONS

This article has addressed the switching noise propagation and suppression in multi-sampled pulse-width modulated current-controlled systems. For the operating points where the sampling instants occur near the commutation ones, the switching noise is introduced in feedback. It is shown how MS-PWM without feedback filters does not necessarily feature high switching noise sensitivity, due to modulator non-linearity. For lower multi-sampling factors and/or higher switching noise magnitudes, MAF fails to suppress the switching noise, whereas RRR + MED successfully suppresses it during dc and ac operation. The proposed control strategy, MS-PWM with RRR + MED, not only ensures high noise immunity and enhances modulator linearity, but also breaks the bandwidth limitations encountered with MR-DS-PWM with either MAF or RRR + MED, outperforming thereby typically used DS-PWM.

#### APPENDIX

To evaluate the performance of the proposed feedback filtering strategy in PESs with multiple commutations per modulation period, multi-level voltage source converters consisting of



Fig. 16: Experimentally measured inductor current for MS-PWM illustrating superiority of RRR + MED over MAF during sinusoidal ac operation with M = 0.75. The current is plotted after removing the switching ripple from the data acquired by the oscilloscope.

cascaded half- or full-bridge cells with inductive output filter are considered. Nevertheless, the presented methodology is easily applicable to other multi-level and interleaved converters as well. Control system similar to the one in Fig. 1 is assumed, with the only difference being the modulator. For multilevel and interleaved converters, symmetric<sup>12</sup> phase-shifted PWM (PS-PWM), consisting of  $N_w$  phase-shifted triangular carriers, is assumed [28]. There, an often implemented control strategy is multi-sampled PS-PWM (MS-PS-PWM), in which  $N = N_c = 2N_w$ . Due to frequency multiplication of PS-PWM, MS-PS-PWM is often considered as equivalent to DS-PWM in two-level converters, and used in this article as a benchmark [28]. Similar to MR-DS-PWM control aimed at enhancing noise suppression for two-level converters, multirate multi-sampled PS-PWM control (MR-MS-PS-PWM) is considered. There the feedback is further oversampled at  $f_s >$  $2N_w f_{pwm}$ , filtered and then decimated to  $f_c = 2N_w f_{pwm}$ , i.e.,  $N_c = 2N_w$  and  $N > 2N_w$ . To further improve dynamic performance, decimation to  $f_c = 2N_w f_{pwm}$  could be omitted resulting in the control strategy for multi-level converters with  $f_s = f_c > N_w f_{pwm}$ , which is equivalent to MS-PWM for two-level converters. Discussion about properties of such a control strategy is left for future work.

To compare the switching noise sensitivity of MR-MS-PS-PWM with different feedback filters, variance of each carrier's duty cycle is obtained from simulations, organized in a similar way as described in Section IV.A. As an example, three-level converter consisting of two cascaded half-bridge cells  $(N_w = 2)$  is implemented, with the dc voltage of each cell being 120V, L = 1.5 mH and  $f_{pwm} = 10$  kHz. PI controller is configured to achieve cross-over frequency of  $f_{cr} = 0.1 N_w f_{pwm}$ , MR-MS-PS-PWM is implemented with N = 16 and  $\tau_{dr} = 0$ . The same feedback filtering strategies are considered as previously for two-level converters: MAF, MED and RRR + MED. The results for dc operation are shown in Fig. 17. Firstly, it is seen that for each carrier, the results are practically the same. This is due to symmetric PS-PWM. Compared to DS-PWM for two-level converters, which is sensitive to switching noise only around D = 0 and D = 1, an

<sup>12</sup>In symmetric PS-PWM, the same modulating signal is used for all carriers.

12



Fig. 17: Variance of the duty cycle for MR-MS-PS-PWM control with N = 16 and  $N_w = 2$  obtained using Simulink model of the cascaded half-bridge converter with inductive output filter and constant voltage load: (a) carrier 1; (b) carrier 2.

additional switching noise sensitive operating point is observed for MS-PS-PWM. This is in accordance with (1), which for  $N = 2N_w = 4$  and  $\tau_{dr} = 0$  predicts  $D_s \in \{0, 0.5, 1\}$ . For higher number of phase-shifted carriers, the number of switching noise sensitive operating points further increases. This is an important remark pointing out to the fact that MS-PS-PWM is not, as often claimed to be, a natural linear extension of DS-PWM. According to (1), for MR-MS-PS-PWM, additional switching noise sensitive operating points appear, due to the feedback signal being further oversampled. Around these operating points, as seen from Fig. 17, neither MAF not MED without RRR are able to suppress the switching noise, resulting in very high variance. Still, compared to MAF, significantly lower switching noise sensitivity peaks appear with MED. For MR-MS-PS-PWM with RRR + MED, switching noise is successfully suppressed for all operating points. This illustrates effectiveness of the proposed feedback filtering strategy even in PESs with multiple commutations per modulation period.

#### REFERENCES

- S. Buso and P. Mattavelli, *Digital Control in Power Electronics*, ser. Synthesis Lectures on Power Electronics. Cham: Springer International Publishing, 2015.
- [2] S. N. Vukosavić, L. S. Perić, and E. Levi, "AC Current Controller with Error-Free Feedback Acquisition System," *IEEE Transactions on Energy Conversion*, vol. 31, no. 1, pp. 381–391, Mar. 2016.
- [3] J. Yang, J. Liu, J. Zhang, N. Zhao, Y. Wang, and T. Q. Zheng, "Multirate Digital Signal Processing and Noise Suppression for Dual Active Bridge DC–DC Converters in a Power Electronic Traction Transformer," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10885–10902, Dec. 2018.
- [4] B. Weber, K. Wiedmann, and A. Mertens, "Increased signal-to-noise ratio of sensorless control using current oversampling," in 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Jun. 2015, pp. 1129–1134.
- [5] I. Z. Petric, P. Mattavelli, and S. Buso, "Investigation of Nonlinearities Introduced by Multi-sampled Pulsewidth Modulators," *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 2538–2550, Mar. 2022.
- [6] I. Z. Petric, P. Mattavelli, and S. Buso, "Feedback Noise Propagation in Multisampled DC–DC Power Electronic Converters," *IEEE Transactions* on Power Electronics, vol. 37, no. 1, pp. 150–161, Jan. 2022.

- [7] I. Z. Petric, R. Cvetanovic, P. Mattavelli, and S. Buso, "Models for Stationary Noise Propagation in Multi-Sampled PWM Power Electronic Control Systems with Decimation," *IEEE Transactions on Power Electronics*, pp. 1–16, 2023.
- [8] L. Corradini and P. Mattavelli, "Modeling of Multisampled Pulse Width Modulators for Digitally Controlled DC–DC Converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1839–1847, Jul. 2008.
- [9] L. Corradini, P. Mattavelli, E. Tedeschi, and D. Trevisan, "High-Bandwidth Multisampled Digitally Controlled DC–DC Converters Using Ripple Compensation," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 4, pp. 1501–1508, Apr. 2008.
- [10] L. Corradini and P. Mattavelli, "Analysis of multiple sampling technique for digitally controlled dc-dc converters," in 2006 37th IEEE Power Electronics Specialists Conference, Jun. 2006, pp. 1–6.
- [11] I. Z. Petric, P. Mattavelli, and S. Buso, "A Jitter Amplification Phenomenon in Multisampled Digital Control of Power Converters," *IEEE Transactions on Power Electronics*, vol. 36, no. 8, pp. 8685–8695, Aug. 2021.
- [12] S. Takeuchi and K. Wada, "Experimental verification of noiseless sampling for buck chopper circuit with current control," in 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), May 2014, pp. 3646–3651.
- [13] L. Saunders, G. Skibinski, S. Evon, and D. Kempkes, "Riding the reflected wave-IGBT drive technology demands new motor and cable considerations," in *Proceedings of 1996 IAS Petroleum and Chemical Industry Technical Conference*, Sep. 1996, pp. 75–84.
- [14] S. Amarir and K. Al-Haddad, "A Modeling Technique to Analyze the Impact of Inverter Supply Voltage and Cable Length on Industrial Motor-Drives," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 753–762, Mar. 2008.
- [15] Z.-n. Ariga and K. Wada, "Analysis and evaluation of near field noise voltage on power electronics circuits," in 2009 International Conference on Power Electronics and Drive Systems (PEDS), Nov. 2009, pp. 1014– 1019.
- [16] H. Song, I. Cvetkovic, R. Zhang, C. DiMarino, and D. Boroyevich, "Gate Driver Switching Noise Propagation Study for Medium Voltage SiC-based Power Electronics Building Blocks," in 2022 IEEE Energy Conversion Congress and Exposition (ECCE), Oct. 2022, pp. 1–8.
- [17] M. R. Nielsen, M. Kirkeby, H. Zhao, D. N. Dalal, M. Møller Bech, and S. Munk-Nielsen, "Noise Analysis of Current Sensor for Medium Voltage Power Converter Enabled by Silicon-Carbide MOSFETs," in 2022 IEEE 9th Workshop on Wide Bandgap Power Devices & Applications (WiPDA), Nov. 2022, pp. 180–185.
- [18] S.-S. Min and R.-Y. Kim, "Improved Gate-Voltage-Driven Desaturation Short-Circuit Protection Circuit with Robust Switching Noise Immunity for WBG Power Semiconductors," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2022.
- [19] B. Zhang and S. Wang, "A Survey of EMI Research in Power Electronics Systems With Wide-Bandgap Semiconductor Devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 626–643, Mar. 2020.
- [20] L. Wang, Y. Shi, and H. Li, "Anti-EMI Noise Digital Filter Design for a 60-kW Five-Level SiC Inverter Without Fiber Isolation," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 13–17, Jan. 2018.
- [21] W. Gardner, Introduction to Random Processes: With Applications to Signals and Systems. Macmillan Publishing Company, 1986.
- [22] P. Midya and P. Krein, "Noise properties of pulse-width modulated power converters: Open-loop effects," *IEEE Transactions on Power Electronics*, vol. 15, no. 6, pp. 1134–1143, Nov. 2000.
- [23] R. Cvetanovic, I. Z. Petric, P. Mattavelli, and S. Buso, "Median Filters for Switching Noise Mitigation in Oversampled Power Electronics Control Systems," accepted for IEEE Energy Conversion Conference and Expo (ECCE) 2023; available on: https://www.techrxiv.org/.
- [24] W. Karl, S. Leeb, L. Jones, J. Kirtley, and G. Verghese, "Applications of rank-based median filters in power electronics," *IEEE Transactions* on *Power Electronics*, vol. 7, no. 3, pp. 437–443, Jul. 1992.
- [25] O. Vainio and S. Ovaska, "Multistage adaptive filters for in-phase processing of line-frequency signals," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 2, pp. 258–264, Apr. 1997.
- [26] H. Peng, A. Prodic, E. Alarcon, and D. Maksimovic, "Modeling of Quantization Effects in Digitally Controlled DC–DC Converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 208–215, 2007.
- [27] PEB8024 Half-bridge SiC power module, Imperix, Mar. 2021, rev. C.
- [28] R. Cvetanovic, I. Z. Petric, P. Mattavelli, and S. Buso, "Small-Signal Modeling of Phase-Shifted Digital PWM in Interleaved and Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 38, no. 3, pp. 3057–3068, 2023.



**Ruzica Cvetanovic** (Student Member, IEEE) was born in Belgrade, Serbia, in 1996. She received the B.S. and M.S. degrees in electrical engineering from the University of Belgrade, Belgrade, in 2019 and 2020, respectively. Since 2022, she has been working toward the Ph.D. degree with the Power Electronics Group, Department of Information Engineering, University of Padova, Padova, Italy.

From 2020 to 2021, she worked with the Power Converters and Systems Group, School of Electrical Engineering, University of Belgrade. In 2021, she

joined the Power Electronics Group, Department of Information Engineering, University of Padova, as a Visiting Researcher. Her research interests include modeling and digital control of grid-tied power electronics converters.



**Paolo Mattavelli** (Fellow, IEEE) received the MS degree (with honors) and the Ph. D. degree in electrical engineering from the University of Padova (Italy) in 1992 and in 1995, respectively. From 1995 to 2001, he was a researcher at the University of Padova. From 2001 to 2005 he was an associate professor at the University of Udine, where he led the Power Electronics Laboratory. In 2005 he joined the University of Padova in Vicenza with the same duties. From 2010 to 2012 he was with the Center for Power Electronics Systems (CPES) at Virginia

Tech. He is currently a professor at the University of Padova. His major field of interest includes analysis, modeling and analog and digital control of power converters, grid-connected converters for renewable energy systems and micro-grids, high-temperature and high-power density power electronics. In these research fields, he has been leading several industrial and government projects. His current google scholar h-index is 81. From 2003 to 2012 he served as an Associate Editor for IEEE Transactions on Power Electronics. From 2005 to 2010 he was the IPCC (Industrial Power Converter Committee) Technical Review Chair for the IEEE Transactions on Industry Applications. For terms 2003-2006, 2006-2009 and 2013-2015 he has been a member-at-large of the IEEE Power Electronics Society's Administrative Committee. He also received in 2005, 2006, 2011 and 2012 the Prize Paper Award in the IEEE Transactions on Power Electronics and in 2007, the 2nd Prize Paper Award at the IEEE Industry Application Annual Meeting. He is an IEEE Fellow and Co-Editor in Chief for the IEEE Transactions on Power Electronics.



**Ivan Z. Petric** (Member, IEEE) was born in Belgrade, Serbia, in 1994. He received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Belgrade, Serbia, in 2017 and 2018, respectively, and the Ph.D. degree in electrical engineering from the University of Padova, Italy, in 2023.

From 2018 to 2019, he was a Researcher with the Power Electronics, Machines and Control Group, The University of Nottingham, U.K. In 2022, he was a Visiting Researcher with the Electrical Engineering

and Computer Sciences Department, University of California, Berkeley, CA, USA. His research interests include modeling and control of power converters, advanced modulation strategies, and grid-connected converters for renewable energy sources and smart microgrids.



Simone Buso (Member, IEEE) received the M.Sc. degree in electronic engineering and the Ph.D. degree in industrial electronics from the University of Padova, Italy, in 1992 and 1997, respectively. He is currently an Associate Professor of electronics with the Department of Information Engineering (DEI) at the University of Padova. His main research interests are in the industrial and power electronics fields and are related specifically to switching converters, renewable energy sources and smart micro-grids.