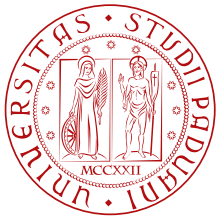

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Analysis of multi-sampled pulsewidth modulation and its application in grid-tied converters

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Abstract

Power electronic systems are essential parts of most modern technologies that depend on converting electrical energy from one form to another. One of such applications is the electric power grid, where more and more grid-tied converters are present, bringing a true paradigm shift in the generation, transmission, distribution, and consumption of electricity.

To enable their highly-sophisticated usage as energy-processors, power electronic converters are actively controlled. For a set hardware design, it is the task of the control system to enable highest dynamic performance, which determines the overall system capabilities. The actuation of any power electronic converter is determined by the modulation strategy, which dynamically adjusts its switching states in order to achieve the desired system behavior. Nowadays, power electronic control systems are typically implemented within digital control platforms, as they offer much higher levels of flexibility and unmatched regulation capacities with respect to analog control systems. However, significant demerits of digital control are the associated delays, which are not present when using analog controllers.

The focus of this dissertation is the multi-sampled pulsewidth modulation (MS-PWM), which relies on executing the control action more than twice per modulation period with a target of achieving analog-like dynamic performance while retaining all the benefits of the digital control systems. This dissertation brings the analysis of some fundamental aspects of this modulation strategy, as well as an investigation of its applicability in grid-tied power electronic converters.

Besides the positive impact of MS-PWM on reducing the control delays, it is known that several nonlinearities arise due to the switching ripple being introduced in the control system. This has resulted in most reported MS-PWM applications to rely on ripple-removal filters, which have a strong negative impact on the dynamic performance. In this dissertation, particular attention is placed on analyzing the MS-PWM nonlinearities caused by jump discontinuities of the modulating waveform. Besides the two known types, another one is discovered and shown to bring a mechanism for limit cycle oscillations. The resulting effects are analyzed, statistically modelled, and a solution for their cancellation is proposed. By examining the impact of the control system on the discontinuities, it is shown how it affects which nonlinearity is introduced and to what extent. This part of the dissertation is focused on providing a methodology for the control system design that minimizes the impact of the MS-PWM nonlinearities, without having to completely remove the switching ripple. It is concluded that the appropriate filtering is crucial for the performance of MS-PWM with lower multisampling factors while, for high-enough number

of samples, the effects caused by the discontinuities are strongly reduced. The analysis is verified in simulations and experimentally.

The dissertation continues by exploring noise propagation in digitally-controlled PWM-based power electronic systems. Motivated by the fact that, in MS-PWM, the feedback signal is by definition over-sampled, focus is placed on investigating whether the noise impact can be strongly suppressed, while retaining the high dynamic performance. First, it is shown that the MS-PWM systems feature an inherent decimation mechanism, which limits the noise attenuation capabilities. Accordingly, new models for noise propagation in systems with decimation are derived and digital anti-aliasing filters are proposed to reduce the related aliasing. Extensive experimental measurements validate the derived models and show that, with the appropriate digital filters, MS-PWM can bring strong noise suppression without heavily impacting the system dynamics.

Finally, this dissertation examines the potential of MS-PWM to achieve robust stability of grid-tied converters. Namely, due to control delays, power converters introduce negative damping at high-frequencies, which may result in harmonic instability, therefore compromising the system operation. To address this, many control strategies have been proposed to introduce active damping (AD) to the system, however, their effectiveness is compromised at very high frequencies. In this dissertation, it is explored how MS-PWM inherently brings the required damping, in an extended frequency range, without introducing additional complexity to the control system. Experimental impedance measurements and tested grid-connected scenarios validate that MS-PWM provides robust stability, outperforming the typically-used AD methods. Additionally, noise sensitivity is analyzed and the derived models show that MS-PWM outperforms AD in this respect as well. These findings are supported by experimental measurements and simulations.

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Chapter 1

Introduction

1.1 Motivation and objectives

The rise of civilization has been strongly linked with our capabilities of harnessing energy from the surroundings and converting it into a suitable form. From the earliest applications of burning biomass for the purposes of heating and cooking, via creating machinery that helped us surpass our physical limitations, to the highly-sophisticated era of digital information processing, modern society owes its current state to the technological developments related to energy. Starting from the 20th century, participation of electricity in the energy transfer and final consumption has significantly increased and, with the increasing relevance of sustainability, this trend is only expected to continue [1].

The fundamental infrastructure for a widespread use of the electrical energy is the electric power grid, which consists of systems for generation, transmission, and distribution. The electric power grid is experiencing one of the greatest revolutions of the 21st century. Large, centralized, power plants based on fossil fuels are being replaced by distributed generation using renewable energy sources. These sources are by their nature intermittent, hence, storage of the electrical energy is gaining almost the same importance as its generation. Transmission and distribution networks are partly changing from ac grids to dc grids and are becoming significantly more complex in order to accommodate some novel, challenging, services such as, for example, the electric vehicle fast charging stations. Even the end-consumption is changing from dominantly passive to almost entirely electronically controlled loads. Traditional, centralized, systems are expected to be gradually replaced by many smaller, quasi-independent, "smart-grid" blocks that would incorporate localized generation, storage, and consumption.

The enabling technology and the driving force of this change is power electronics. Whether to interface a wind-turbine to the grid, store energy using batteries or hydrogen, replace large capacitor banks for reactive power compensation, or to provide many other functions, the use of grid-connected electronic power converters is unavoidable.

To enable the required flexibility in energy processing, grid-tied converters are actively controlled, with the control systems being divided in several hierarchical levels [2]. Higher levels that, amongst all,

determine the needed power flows, adaptation to particular operating conditions, and reactive power and harmonic compensation, are in the end all serviced by the foundation layer, i.e. the "zero-level" control. This control layer is in charge of regulating the currents or voltages of individual converters, using appropriate feedback or feedforward systems. Dynamic performance of these control loops has a determining impact on the overall system performance, particularly regarding stability, resonance damping, and power quality[1].

For a hardware-defined power converter's switching frequency, limited mainly by the losses and the electromagnetic interference (EMI), it is the task of the zero-level control to achieve as high dynamic performance as possible, while maintaining stability, required output waveform quality, and a satisfactory robustness against uncertainties. The zero-level control is intimately related to the power electronic hardware stage and, in parallel with designing the appropriate controller structure, the most important step is determining the suitable modulation (switching) strategy. This dissertation is indeed focused on analyzing a specific modulation strategy, rather than on a particular controller structure design.

In most power electronic systems, digital control is nowadays a standard solution as it offers a much higher flexibility compared to analog control circuits. This is especially important for applications that require sophisticated control laws, controller auto-tuning, communications, various monitoring tasks, additional protection levels, and similar [3].

It is known that the highest dynamic performance is obtained using nonlinear techniques that instantaneously impact the switching state of the converter [4]. Amongst these, the most widely implemented one is the hysteresis controller. Despite its superior dynamic capabilities, a demerit of the hysteresis-based control is the variable switching frequency, which is often unacceptable, due to problems with filtering and excitation of resonances. To solve this issue, the hysteresis control with frequency stabilization algorithms is the topic of extensive research [3]. While commonly implemented using analog circuits, the fully-digital hysteresis control is starting to gain a significant interest, however, it is still not a standardized solution [3]. Another widely-investigated nonlinear control strategy is the model predictive control (MPC) [5]. MPC determines the switching state of the converter as a result of minimizing a certain cost function over a finite prediction horizon, using constrained optimization methods. While offering a relatively simply-posed multi-objective control, several aspects limit its use in power electronics. These include a non-standardized choice of cost functions, incompatibility with tools developed for linear control theory, and a high computational burden in conjunction with a high sampling rate requirement in order to achieve an output waveform quality comparable to other control strategies. Moreover, MPC is highly sensitive to parameter and model uncertainties.

Undoubtedly, most power electronic control systems rely on the pulsewidth modulation (PWM) technique to determine the switching state of the converter [3]. PWM fixes the modulation period, while the state durations are determined by the controller output, i.e. the modulating waveform. A fixed

[1]Not to limit the application space to grid-tied converters only, dynamic capabilities of the inner current or voltage control loops have a determining influence on the performance of all power electronic systems, from switched-mode power supplies for CPUs to traction inverters in electric drives.

switching frequency and a well-known output harmonic content allow PWM-based systems to have simple filtering schemes, as well as to avoid the risk of triggering system resonances. This modulation scheme allows the effective use of both linear and nonlinear control structures, derived using frequency-domain or time-domain methods. PWM is also used together with predictive, e.g. dead-beat, controllers [6]. Moreover, PWM behaves closely to a linear wideband amplifier, which effectively enables analyses using the standard control theory.

Traditionally, in digital PWM applications, the feedback is sampled and the controller output is updated once or twice per switching period, which introduces a significant modulation delay [3]. This delay, together with times needed for analog-to-digital conversion and algorithm execution, strongly deteriorates dynamic performance of the digital PWM. However, with the advancement of the technology related to microcontrollers, digital signal processors (DSPs), and field-programmable gate arrays (FPGAs), increasingly more information can be processed within a certain time interval, using standard control platforms. In regard to processing power, novel wide bandgap devices, based on Silicon Carbide (SiC) or Gallium Nitride (GaN), enable very high switching frequencies [7]. However, in many higher power or voltage applications, the switching frequencies are expected to remain quite low compared to information processing capabilities. Hence, to fully exploit the emerging capacities of digital control platforms, one of the possible directions is going towards analog-like controllers in digital systems [3].

This dissertation follows the trend of investigating smart digital control solutions, by focusing on the *multi-sampled pulsewidth modulation* (MS-PWM). A step towards overcoming the bandwidth limitations of digital control loops is made by adopting the MS-PWM control, in which the feedback is sampled and the control action is executed with a rate higher than double the switching frequency. This reduces the modulation delays and enables analog-like dynamic performance [3].

MS-PWM control was explored in the past and it was shown that it offers improvement of both small-signal and large-signal dynamic capabilities. Besides custom hardware control platforms, its implementation was successfully demonstrated in commercially available DSPs. However, MS-PWM is still a "young" technique with many aspects that require further analysis before it can be widely implemented on an industrial level.

For example, with MS-PWM the switching ripple is unavoidably introduced in the feedback signal. Properties of MS-PWM operated converters, without entirely filtering out the switching ripple, are still not completely clarified. It is known that the sampled switching ripple may cause vertical crossings between the modulating waveform and the PWM carrier, which brings some nonlinearities to the system. However, a clear procedure for determining which nonlinearity will be present and to what extent, depending on the control system and hardware parameters, was not present in the literature. This has brought a motivation to dedicate a part of this research to the analysis of the related MS-PWM nonlinearities. Besides the already-reported types, another nonlinear effect is identified, explained, and statistically modeled in this thesis. Classification of all MS-PWM nonlinearities is given, their impact on a converter's operation is analyzed, and a methodology is provided for their minimization via the

appropriate control system design.

Another relevant question is the noise sensitivity of MS-PWM control systems. In return for enabling high dynamic capabilities, most related control strategies bring a significant sensitivity to the measurement noise, which correspondingly limits their practical applicability. However, the fact that MS-PWM is based on oversampling the feedback and that its delay reduction does not come from a derivative action has brought an inspiration to examine whether MS-PWM may jointly offer strong noise suppression and high dynamic performance. In this thesis, it is shown that MS-PWM control systems feature an inherent decimation effect caused by the PWM carrier, which limits the noise suppression. To address this, an analytical model is derived for noise propagation in multi-sampled digital control systems. It is shown analytically and verified experimentally that, with the proposed anti-aliasing digital filter design, MS-PWM may indeed offer both strong noise suppression and fast dynamics.

The final motivation behind this dissertation was to further investigate the applicability of MS-PWM in grid-connected converters, relying on the fundamental properties analyzed beforehand. Namely, the increasing presence of grid-connected converters gives rise to stability issues of power grids. Due to dynamic interactions between controlled converters and passive filters, resonance destabilization may occur. One of the problems, related to high-frequency harmonic instability, comes from the negative damping introduced due to the control delays. This has attracted a significant attention and has driven research in the field of passivity-based control, which focuses on adding damping to the system. However, the developed damping strategies bring certain negative aspects, like ineffectiveness at very high frequencies. In this thesis, it is shown that MS-PWM outperforms these strategies and uniquely offers robust high-frequency stability by inherently reducing the control delays.

1.2 Review of previous research

The idea behind this review is to bring an insight into the development of the multi-sampled pulsewidth modulation, both from the chronological perspective, as well as by grouping together the related, distinct, research paths. Results achieved by other authors that are published in parallel with the writing of this thesis are placed in this section as well. The original contributions of this thesis, and related publications, are highlighted in the following section.

Digital control in power electronics has gained interest starting from the late 1960s [8]. The considered applications mostly involved medium- and high-power inverters in variable speed drives and uninterruptible ac power supplies, i.e. power converters with switching frequencies limited to a few tens of kHz. A comprehensive review of these early works is available in [9]. Regarding digital control in high switching frequency converters, e.g. in voltage regulator modules (VRMs), extensive research has started in the late 1990s and the early 2000s [10–14]. Moreover, at this time, a great research effort was placed on investigating the fundamental principles and specific properties of digital control in power electronics, rather than just its application.

Regarding the pulsewidth modulation, first, analog, solutions were based on the “naturally sampled”

PWM (NS-PWM). In his fundamental work [15], *Bowes* has introduced the "regularly sampled", or "uniformly sampled", PWM (US-PWM) to power electronics, by first processing the analog modulating waveform with the zero-order-hold (ZOH) circuit. In [15], the sample-and-hold action was performed once per switching period, which was termed the "symmetric" modulation. This strategy has brought a linear relationship between the sampled modulating waveform and the switching pulse duration. US-PWM with two samples per switching period was termed the "asymmetric" modulation. The discrete-time sample-and-hold nature of US-PWM lent itself suitable for digital control techniques, particularly in the early years, when the processing capabilities were severely limited [9]. However, it was shown that the introduced ZOH action brings a delay, which is not present in the case of NS-PWM [16,17]. Therefore, for applications that required a very high dynamic performance, analog control with NS-PWM was for long time the only viable strategy.

The background of MS-PWM in power electronics is seemingly perplexed and, when put in perspective, the idea behind it is as old as digital control itself. For instance, the implementation of the digital NS-PWM approximation was reported in [9], although, quite clearly ahead of feasibility for its widespread use. With the advancement of digital control platforms, the idea to reduce the delay associated with the ZOH, by mimicking the NS-PWM, has started to develop more firmly. In [18], *Walker* was the first one to specifically discuss the implementation and some important properties of the digital approximation of NS-PWM. In that paper, the modulation was termed the "re-sampled uniform" PWM and some important practical remarks were reported for the first time. These included handling the, later termed, *counter-phase* and *in-phase vertical crossings*, caused by the discontinuous nature of the modulating signal, in order to prevent the *pulse-skipping* and the *multiple-switching* phenomena. It was shown that the re-sampled US-PWM reduces the modulation delay. Furthermore, it was pointed out that this modulation strategy is highly suitable for multilevel converters with multiple phase-shifted carriers.

A significant expansion of knowledge on MS-PWM was brought by a series of publications from *Corradini et al.* [19–27]. There, the modulation was first termed the multi-sampled PWM, which is used in this thesis as well. The analysis was narrowed down to the two-level modulation and, for the first time, some unique MS-PWM properties that do not have their counterparts in NS-PWM were analyzed. The associated publications have brought the small-signal model of MS-PWM, based on the describing function (DF) approach. This has proven that MS-PWM reduces the modulation delay and, for high multisampling factors, approaches NS-PWM. Besides the dynamic modeling, a great effort was dedicated to analyzing the impact of the sampled switching ripple, which was shown to cause the vertical crossings even in steady-state conditions. It was revealed that the vertical crossings introduce a nonlinear behavior, which impairs the converter's transient response capabilities by reducing the modulation gain or even bringing uncontrollable operating points, termed the dead-bands[2]. These nonlinearities were analyzed through the modulator's static transcharacteristic, whose calculation is presented in [24]. The related publications have also analyzed different carrier waveforms and have demonstrated that the triangular

[2]It should be elucidated that the dead-bands are not the same as the pulse-skipping and cannot be avoided by a simple logic in the controller. This is often misconstrued in the literature, even in recent publications [28, 29].

carrier modulation is superior for MS-PWM, due to its higher linearity. For suppressing the impact of the modulating waveform discontinuities, in these publications, the groundwork was placed for either completely filtering out the switching ripple [25,26] or dynamically re-adjusting the modulating waveform update instants [23]. In [25] it was shown that MS-PWM has a great potential for grid-tied applications as well.

In [24], it was clearly presented that the MS-PWM nonlinearites are reduced as the multisampling factor is increased. Moreover, in this thesis it will be shown that higher multisampling factors also bring other positive aspects. Therefore, concluding that benefits obtained by increasing the sampling frequency quickly saturate [30] is not generally valid.

Besides the vertical crossings, presence of the switching ripple in the modulating waveform brings other nonlinear effects, which are more evident for high multisampling factors and are practically shared with NS-PWM [31, 32]. For example, in [33], the analysis was provided for determining the maximal bandwidth that retains the smooth modulation in case of highly-oversampled systems. From the early research stages, it was recognized that certain feedback filtering is necessary for the robust implementation of MS-PWM. Starting from the work in [19], it was clear that a compromise must be made between reducing the switching ripple content and keeping a high dynamic performance. In the above-listed publications by *Corradini et al.*, impacts of the moving average filter (MAF), the repetitive filter (RF), and the ripple predictor were analyzed. The application of these filters, and their combinations with phase-leading elements, was revisited in a recent work [34]. A short overview of the relevant ripple filtering strategies is placed in Chapter 2 of this thesis.

In a highly-oversampled class-D audio amplifier application, analyzed in [35], it was shown that, for sawtooth carriers, the ripple impact may be compensated by summing the carrier with the PWM output. This was proven to be equivalent to pre-distorting the carrier based on the output filter. However, this strategy has not found a vast application space and it does not cover the triangular carrier modulation.

An interesting possibility for counteracting the modulating waveform discontinuities and, hence, linearizing the MS-PWM operation, is to replace the ZOH with the first-order-hold (FOH) [36, 37]. In theory, this positively impacts the shape of the modulating waveform, bringing the operation closer to NS-PWM. However, this has not yet been widely investigated and some clear demerits are the necessity for a custom hardware control platform as well as an increased high-frequency gain, which amplifies the feedback noise.

In [38, 39], multi-rate system analyses were provided and it was shown that MS-PWM may offer an improved output harmonic content, particularly in applications with very low switching frequencies. Note, however, that it was shown in [34] that MS-PWM may actually increase the output distortion. In this thesis, it is verified that the output waveform quality is indeed deteriorated for low multisampling factors, without ripple filtering, due to the emphasized nonlinear effects related to the vertical crossings. These findings are supported by a recent publication [40], where resonant filters are added to the controller to compensate the impact of the counter-phase vertical crossings on the output waveform distortion.

MS-PWM has recently gained more interest for grid-tied converter applications, where the system stability may become compromised due to the interactions between various power electronic systems. One of the first studies on the positive impact of MS-PWM on damping the LCL filter resonance is reported in [41]. In this thesis, research effort was dedicated to investigating the impedance properties of grid-connected converters with MS-PWM control systems. Corresponding findings are supported by later publications that deal with the positive impact of MS-PWM in circulating current control loops of parallel inverters [42] and the impedance properties of systems that employ both MS-PWM and active damping techniques [43].

Regarding direct comparison with other high-performance digital control strategies, in [44], it was shown that a linear single-loop MS-PWM current controller outperforms an oversampled fixed switching frequency finite-control-set model predictive controller (FCS-MPC). It was shown that, compared to MS-PWM, even the improved oversampled MPC implementation suffers worse output waveform quality, higher computational complexity, and higher sensitivity to model uncertainties.

In [3,45], for a voltage source inverter (VSI) current control application, a linear single-loop MS-PWM controller was outperformed by a double-sampled dead-beat controller and a fully-digital implementation of the nonlinear hysteresis controller. However, this does not invalidate the MS-PWM itself, due to some specific limitations of the other two strategies. Namely, the implemented dead-beat, although belonging to the group of predictive controllers, is in fact a proportional controller with a feedforward action based on the output voltage, realized using the double-sampled PWM. Due to its model-based design, the response is significantly deteriorated with the presence of parameter mismatch or unmodeled dynamics. Another down side of the dead-beat control is that, in its basic implementation, it requires an additional measurement, which complicates the required hardware and increases the noise sensitivity. If the output voltage is estimated, sensitivity to model and parameter uncertainties is further increased and the dynamic response is slightly deteriorated. Moreover, the dead-beat control is particularly sensitive to the dead time and requires its compensation. Extremely fast dynamic response of the dead-beat control is aided by the feedforward action, which can be applied to the MS-PWM systems as well. Indeed, in [46–49], it was shown that the MS-PWM dead-beat implementation results in improved disturbance rejection, reduced sensitivity to parameter mismatch and unmodeled dynamics, and an improved large-signal response. Regarding the hysteresis control, this type of bang-bang nonlinear strategy guarantees the fastest possible current response [3]. However, its fully-digital implementation requires very high multisampling factors, high bandwidth sensing, external analog current reference generation, an additional frequency stabilization algorithm, compensation of the dead time and sampling delays, and more [50]. Therefore, although providing an unmatched dynamic response, its implementation requires specific control hardware and a highly optimized design.

In multilevel and interleaved power converter applications, harmonic cancellation may be achieved when using multiple properly phase-shifted carriers [51]. In balanced conditions, the phase-shifted PWM (PS-PWM) results in the multiplication of the switching ripple frequency, which allows for MS-PWM

implementation without introducing ripple to the feedback. For such cases, most of the specific MS-PWM nonlinearities are avoided and the modulation properties are quite similar to the single- or double-sampled PWM. An early application of MS-PWM in a three-level converter, with 4 sampling instants that coincide with the average current value, is reported in [52]. Other applications with the phase-shifted MS-PWM and the multisampling factor determined by the increased ripple frequency can be found amongst [28, 53–57]. It should be mentioned that, in response to transients, even in perfectly balanced conditions, the vertical crossings may appear. Moreover, for unbalanced operation with the phase-shifted MS-PWM, which is often met in, for example, flying capacitor multilevel (FCML) converters [58], the ideal frequency multiplication is not achieved and the switching ripple is sampled. MS-PWM properties in related conditions are not yet widely investigated in the literature.

Some other publications that are closely related to MS-PWM and the topics covered in this thesis are reported here. In [59], the multi-sampled space vector modulation (MS-SVM) was introduced and shown to be able to suppress the low-order harmonics in low-switching frequency current source converters. The positive impact of MS-SVM on the output waveform quality was also reported in [60]. In [61], the generation of limit cycle oscillations (LCOs) was analyzed for the MS-PWM control of a buck converter. A recent work on predicting the counter-phase vertical crossings in MS-PWM systems was published in [62]. In [63, 64], it was analyzed how the oversampled filtering, with the decimation to the double-sampled PWM, can be used to strongly suppress the aliasing and the feedback noise. The oversampling also offers a great advantage in parameter estimation and condition monitoring. These topics are out-of-scope of this thesis and some related applications can be found in [29].

1.3 Dissertation outline and summary of main contributions

Besides the introduction, this dissertation consists of the following parts.

Chapter 2: Control system architecture. This chapter is practically an extension of the introduction. First, the structure of the digital control system is explained and relevant blocks and signals, used throughout the thesis, are defined. Then, the chapter continues with the important aspects, properties, and definitions related to the pulsewidth modulation. A brief overview of the existing knowledge on MS-PWM, which this thesis builds upon, is presented.

Chapter 3: Experimental set-ups. This chapter describes the hardware set-ups and the control platforms that are used for all experimental verifications in the thesis.

Chapter 4: Nonlinearities caused by the switching ripple. This is the first chapter that features original contributions of this thesis. Based on the previous work, it is known that the switching ripple introduces several nonlinearities to MS-PWM control systems. Consequently, most MS-PWM implementations rely on completely removing the switching ripple using digital filters. However, these filters have a strong impact on the overall performance; hence, there is a motivation to further analyze the MS-PWM operation with a non-negligible switching ripple being present in the feedback. The chapter begins by briefly revisiting the nonlinear phenomena that are present in, but are not uniquely

related to, MS-PWM. This includes the aliasing, which may appear in all digital control systems, and the ripple modulation, which may appear in NS-PWM and MS-PWM. Then, this chapter explores the nonlinearities caused by the jump discontinuities in the modulating waveform, which are only present in MS-PWM. Besides the known effects caused by the counter-phase vertical crossings, another nonlinear mechanism is discovered and analyzed. Its highly-detrimental impact, manifested by duty cycle jittering, is explained and statistically modelled. Then, the focus of the chapter is placed on investigating the connection between control systems settings and the exhibited MS-PWM nonlinearities. The main original contributions found in this chapter are:

- Discovery and analysis of the MS-PWM infinite-gain zones, which bring a limit cycle oscillation mechanism.
- Analytical and numerical methods for determining which discontinuity-related MS-PWM nonlinearity is present and to what extent, depending on the control system parameters.
- Framework for control system design focused on suppressing the impact of MS-PWM nonlinearities, without needing to completely remove the switching ripple.

The material from this chapter is published in two journal manuscripts [65, 66].

Chapter 5: Analysis of noise propagation in multi-sampled control systems. This chapter investigates noise sensitivity of multi-sampled PWM-based power electronic systems. The main motivation is to analyze whether MS-PWM can jointly enable a strong noise suppression and a high dynamic performance. The chapter begins by briefly explaining the main sources of noise that are present in power electronic control systems. Then, a known linear analytical model for white noise propagation is presented and shown to be valid only for single-sampled and double-sampled PWM. For MS-PWM, it is explained that the modulator down-samples the digital modulating signal, which causes aliasing and limits the achievable noise suppression. Correspondingly, design of anti-aliasing digital filters is proposed to reduce the impact of the modulator-related decimation. The chapter continues with the derivation of noise propagation models that include decimation in both open-loop and closed-loop system configurations. The derived models are experimentally verified and the proposed anti-aliasing digital filters are shown to enable strong white noise suppression, without significantly impacting the dynamic performance. This chapter also features a comparison of noise attenuation capabilities of MS-PWM and a commonly implemented technique for oversampled filtering. The main original contributions found in this chapter are:

- Validation that, in terms of noise propagation, the multi-sampled digital pulsewidth modulator introduces decimation.
- Derivation of white noise propagation models that take into account decimation in open-loop and closed-loop systems.

- Proposed design of anti-aliasing filters that enable MS-PWM systems to strongly suppress the feedback noise, with a low impact on the dynamic performance.

The material from this chapter is published in one conference [67] and one journal manuscript [68]. Another journal manuscript [69] is submitted at the time of writing.

Chapter 6: Impedance shaping for robust stability of grid-connected VSCs. This chapter analyzes the effectiveness of MS-PWM in preventing the high-frequency harmonic instability of grid-tied voltage source converters (VSCs), caused by delays of the current control system. The investigation is based on the admittance (impedance)-based stability approach; more specifically, on the passivity analysis. The chapter begins by analyzing the impact of the control system on the VSC admittance properties. Correspondingly, the chapter proceeds with a direct comparison between MS-PWM and typically-used active damping (AD) strategies in effectiveness of passivizing the VSC admittance. The admittance measurement set-up, designed to enable high-precision measurements in a wide frequency range, is explained and it is shown that MS-PWM inherently achieves passivity in a very wide frequency range, while the remaining non-passive zones are by all means negligible. Based on conclusions from Chapter 4, the impact of the MS-PWM nonlinearities is examined and it is shown that the resulting effects are not detrimental for the passivity properties. Moreover, it is verified that the digital filter design from Chapter 4 can be used to linearize the VSC behavior. As for the AD strategies, the admittance measurements verify that their effectiveness is limited to medium frequencies, while being detrimental at very high frequencies. The implications of the admittance properties are verified by testing the stability of specific grid-connected scenarios. As predicted by the analysis, only MS-PWM retains stability for all tested cases, while AD strategies cause instability. The final part of this chapter examines noise sensitivity of the tested passivizing control strategies. Models, derived based on the analysis from Chapter 5, are supported by experimental measurements. It is shown that AD strategies are not highly sensitive, however, MS-PWM brings a superior performance. Based on the design procedure from Chapter 5, the anti-aliasing digital filters are tested for MS-PWM and it is demonstrated that they enable strong noise suppression, while having a negligible impact on the admittance properties. The main original contributions found in this chapter are:

- Investigation of the impact of MS-PWM on passivizing the VSC admittance, also considering the MS-PWM nonlinearities.
- Comparison in passivizing effectiveness of MS-PWM and AD control strategies.
- Analysis and modeling of noise sensitivity of AD control strategies.

The material from this chapter is published in two journal manuscripts [70, 71].

Besides the papers listed above, additional publications on topics closely related to this thesis include a conference [72] and two journal [73, 74] manuscripts.

Chapter 2

Control system architecture

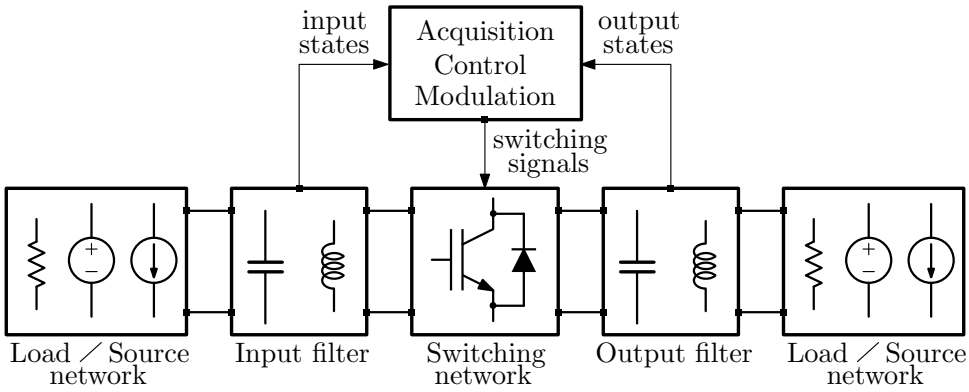


Figure 2.1: Illustration of a digitally controlled power electronic system.

A power electronic system (PES) is illustrated in Fig. 2.1. It comprises the switching network, based on the power semiconductor devices (switches), which interfaces different electrical systems via passive filters. In the given illustration, two electrical systems are present; however, a PES can interface an arbitrary number of systems, which is typically referred to as multi-port conversion. Depending on the switching network topology and the switch technology, PESs can enable energy flow in an arbitrary direction. The energy flow depends on the state of the switching network, which can be manipulated by using controllable power devices (e.g. transistors) [75].

A fundamental step in designing the power electronic control system is the choice of the actuation strategy. Namely, based on the required energy flow, the state of the switching network must be dynamically adjusted. This requires an appropriate transformation from the controller outputs to the switching signals that determine the switching network state. This is typically referred to as the modulation strategy of PESs. As noted in the introduction, there are several ways to control the switching network state. The one analyzed in this thesis is the pulsewidth modulation (PWM).

PESs are most-often controlled in closed-loop configurations, in order to compensate disturbances and nonlinearities, and to improve the dynamic performance [75]. Nowadays, high-performance control

systems for power electronic converters are mostly realized within digital control platforms. This is due to the simplicity, flexibility, reproducibility, and adaptability of digital controllers, as well as due to many added functionalities that are unavailable when using analog systems [3,4]. The digital closed-loop control is what enables the use of PESs as true energy-processors, creating an unbreakable link between the power electronics and most of the existing and emerging technologies [1].

This chapter begins by introducing the structure of the digital PWM-based control system, which will be used throughout this thesis, with only minor variations in each chapter. Then, the pulsewidth modulation is explained in more detail and is classified based on different possible implementations. Some of the important PWM properties are briefly summarized by recalling the pioneering work and the main motivation for the multi-sampled PWM is elaborated accordingly.

This thesis is focused on analyzing fundamental properties of MS-PWM. As the main accent is placed on the modulation itself, it was found suitable to analyze it within systems with relatively simple structures, where the resulting effects are easily observed. The aspired outcome is to motivate the implementation of MS-PWM in arbitrary power electronic control systems, with much higher levels of complexity, while being fully aware of its potentialities and limitations.

As an example, a natural extension of this research is the analysis of joined properties of multiple phase-shifted multi-sampled pulsewidth modulators that may be employed in series or parallel stacked converters [51, 55, 76–78]. Related research is being conducted at the time of writing [74], while this thesis focuses on applications that require a single modulator.

2.1 Elements of digital PWM-based control systems

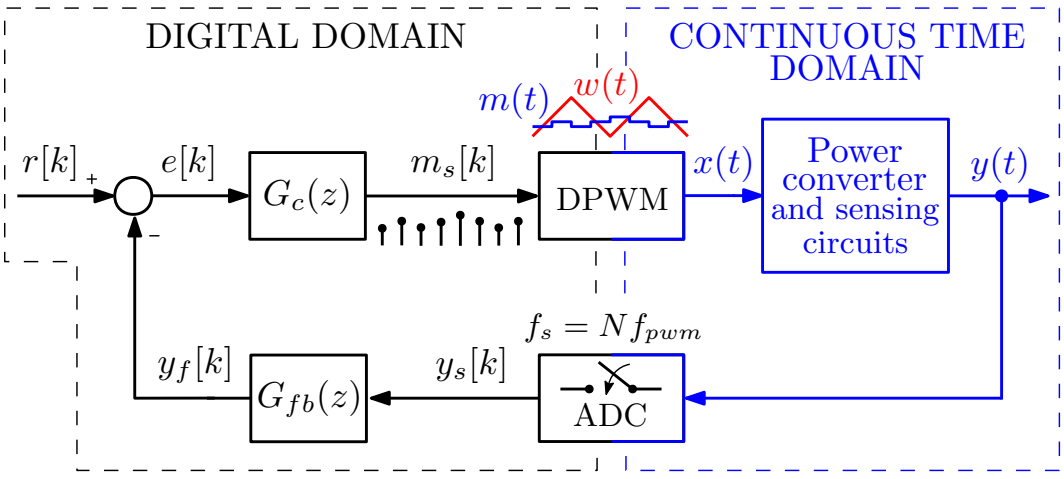


Figure 2.2: Block diagram of a single-stage closed-loop digital control system.

A digital, single-stage, PWM-based, closed-loop control system is shown in Fig. 2.2. The switching state of the converter is determined by the logic switching signal $x(t)$. It is assumed that x is a square waveform with a fixed period, referred to as the switching (modulation) period T_{pwm}. The switching

frequency is labeled as $f_{pwm} = \frac{1}{T_{pwm}}$. Choice of the switching frequency depends on the hardware design, and is limited by the power semiconductor technology, thermal constraints due to switching losses, electromagnetic interference (EMI), and more [75].

The regulated output $y(t)$ is fed-back to the control system. Its transition from the continuous time domain to the digital domain is performed by an analog-to-digital converter (ADC), with the sampling frequency $f_s = Nf_{pwm}$, where N is the multisampling (oversampling[1]) factor. The illustrated digital domain comprises a feedback filter $G_{fb}(z)$, a reference set-point $r[k]$, and a controller $G_c(z)$, which processes the error signal $e[k]$. The operating frequency of the digital part is determined by the sampling frequency. The controller's output $m_s[k]$, in the form of an impulse train, is used as the input of the digital pulsewidth modulator (DPWM). The update period of m_s, $T_s = \frac{1}{f_s}$ is interchangeably referred to as the sampling and the control period[2]. The DPWM block serves as an interface between the digital and the continuous time domains. Its inherent zero-order hold action transforms $m_s[k]$ into the piecewise constant modulating waveform $m(t)$, which is compared with the DPWM's carrier $w(t)$, resulting in the switching signal $x(t)$.

2.2 Pulsewidth modulation

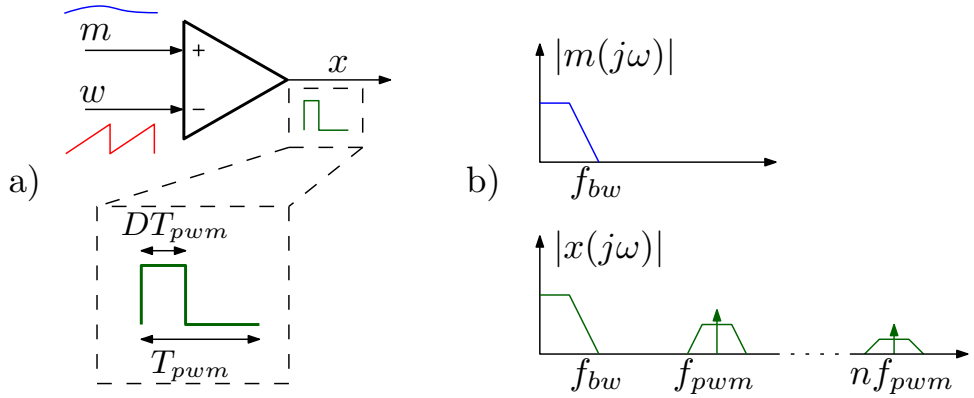


Figure 2.3: Illustration of the PWM process: (a) Comparison between the modulating waveform m and the carrier w, which results in the switching signal x; (b) Spectra of the modulating waveform and the switching signal. The bandwidth of interest for replication is labeled with f_{bw}.

Let us here recall some basic operating principles of pulsewidth modulators.

The goal of PWM is to re-create the low-frequency content of its input reference (modulating) waveform m, using the high-frequency switching square-waveform x. The period of x, T_{pwm}, is determined by the carrier w. The shape of w can be arbitrary and the most-widely used ones are analyzed in Section 2.2.3.

[1] Oversampling is the traditional term, used in digital signal processing applications. The term multisampling is more specific to the analyzed pulsewidth modulation in power electronic applications.

[2] Throughout this thesis, most of the analyzed digital control systems are single-rate, meaning that all digital blocks operate with the rate determined by the sampling frequency. However, in a general case, the digital system can have an arbitrary number of operating frequencies. Multi-rate digital systems will be analyzed in a smaller extent, as a benchmark or in cases where they bring unique properties.

The high state (on state) of x is obtained when $m > w$, while $m < w$ results in its low state (off state)[3]. The switching waveform x exhibits a variable pulsewidth (on state duration), depending on the difference between m and w. Within one switching period, the pulsewidth of x relative to T_{pwm} is referred to as its duty cycle D. The pulsewidth of x determines its low-frequency spectrum, such that it corresponds to the one of the modulating waveform.

Besides recreating the low-frequency spectrum of m, the PWM generates harmonic components around the multiples of f_{pwm}, which are referred to as the switching harmonics and their sidebands. Note that x is not necessarily periodic, depending on the ratio between the carrier and the modulating signal frequencies [15]. This fact is not crucial for the analysis found in this thesis; hence, for simplicity it is always assumed that the PWM process is periodic. Generation of the PWM output spectrum, for a fixed frequency f_{pwm}, is analyzed using the double Fourier series expansion and can be read in [15, 79–81]. An illustration of the PWM process described above is shown in Fig. 2.3.

Providing a fixed switching frequency is one of the main advantages of PWM in power electronic applications, as it results in a deterministic harmonic content localized around multiples of f_{pwm}, which simplifies the hardware design process with respect to both thermal considerations and passive filtering. Additionally, PWM allows the effective use of linear controllers, which leads to a relatively simple control system design.

2.2.1 Digital PWM resolution

When implemented digitally, the carrier waveform is generated using an integer counter with a clock rate $f_{clk} = \frac{1}{T_{clk}}$. The total number of clock counts sets the switching period as $T_{pwm} = N_{clk}T_{clk}$. The time resolution of a DPWM, $\Delta t_{min} = T_{clk}$, is defined as the smallest feasible variation of the pulsewidth of x [4]. The duty cycle resolution is defined as $\Delta D_{min} = \frac{\Delta t_{min}}{T_{pwm}} = \frac{1}{N_{clk}}$. In case N_{clk} is a power of two, the DPWM resolution can be expressed by an equivalent number of bits as $n_{bit} = log_2(N_{clk})$. The DPWM resolution determines how coarse of an actuator the converter is, as it translates to the smallest possible variation of the converter's output voltage. For a small-enough ΔD_{min}, the DPWM quantizer behaves like a linear block [82].

In closed-loop systems, if the DPWM resolution is not high enough with respect to the ADC resolution, limit-cycle oscillations (LCOs) are bound to appear [4, 82–84]. In modern digital control platforms, f_{clk} is typically in the order of 100 MHz, which, to put in a perspective, results in a DPWM resolution of over 10 bits for applications with $f_{pwm} < 100$ kHz. For extremely high switching frequencies, which are not the focus of this thesis, increasing the clock rate to a sufficiently high value would significantly increase the power consumption of the control platform. Therefore, the high clock rate counters are often replaced by tapped delay-lines or some hybrid combination of both [14, 82, 85, 86].

[3]It is assumed that, during one switching period, an appropriate logic is implemented to allow only one transition (switching action) from the high to the low state (turn off) and from the low to the high state (turn on).

2.2.2 Classification based on modulating waveform properties

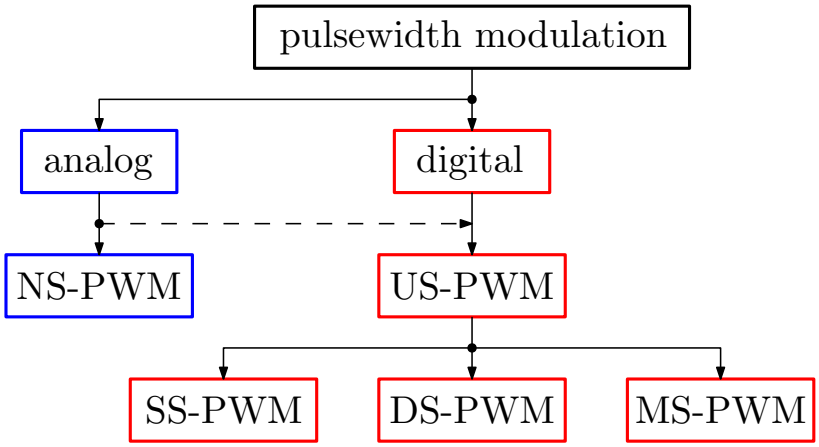


Figure 2.4: Classification of the pulsewidth modulation based on the modulating waveform properties. The used acronyms are: naturally-sampled (NS), uniformly-sampled (US), single-sampled (SS), double-sampled (DS), multi-sampled (MS).

The pulsewidth modulators can be separated in two main groups based on the properties of the modulating waveform [27]. The PWM classification, used in this thesis, is illustrated in Fig. 2.4.

The first group, known as the naturally-sampled PWM (NS-PWM), relies on using the analog modulating waveform m, without any additional processing [15]. Its name comes from the fact that m is being sampled by the comparator itself, at the instants when it becomes equal to w. NS-PWM can only be realized within analog control systems. A significant merit of NS-PWM is that it, in a small-signal sense, it behaves as a pure gain, without introducing any delays [17]. In this thesis, the terms analog modulation and NS-PWM will be used interchangeably.

The second group is known as the uniformly-sampled PWM (US-PWM). In US-PWM, the modulating waveform m is obtained by processing the controller's output m_s with a zero-order hold (ZOH). US-PWM can be realized within analog control systems; however, it is inherent to digital system where the ZOH is part of the DPWM. An important difference with respect to NS-PWM is that, in US-PWM, there is always a certain amount of delay between the instant at which m_s is updated and the instant at which its held version m intersects with w. This introduces delay (both small-signal and large-signal), which is analyzed in Section 2.2.4. US-PWM can be divided in 3 distinct types, depending on the ratio between the ZOH sampling frequency and the switching frequency[4].

The single-sampled PWM (SS-PWM) is obtained if the sampling frequency is equal to the switching frequency, i.e. $f_s = f_{pwm}$ and $N = 1$. The double-sampled PWM (DS-PWM) is obtained for $f_s = 2f_{pwm}$, i.e. $N = 2$. An illustration of a control system with SS-PWM and DS-PWM is shown in Fig. 2.5. The figure also illustrates sampling of the output y, which is assumed to have a triangular shape. SS-PWM and DS-PWM are singled-out, for an intuitive reason. Namely, within one switching period, the switching

[4]It is important to note that the term "sampled" refers to the modulating waveform; hence, in digital systems, the ZOH sampling rate is equal to the controller update rate, which is the same as f_s for single-rate systems such as the one in Fig. 2.2.

signal x can be affected by changing its rising and falling edges. SS-PWM can only modulate the two edges together, while DS-PWM can impact both of them independently. As it will be shown in the following section, whether one or two edges of x can be modulated depends also on the type of carrier used. For many effects analyzed in this thesis, conclusions do not qualitatively differ for SS-PWM and DS-PWM. In such cases, they will be jointly referred to as the (S/D)S-PWM. When needed to avoid confusion between the sampling of the modulating waveform and the sampling of the feedback signal, SS-PWM and DS-PWM will also be referred to as the single-update and double-update PWM [3].

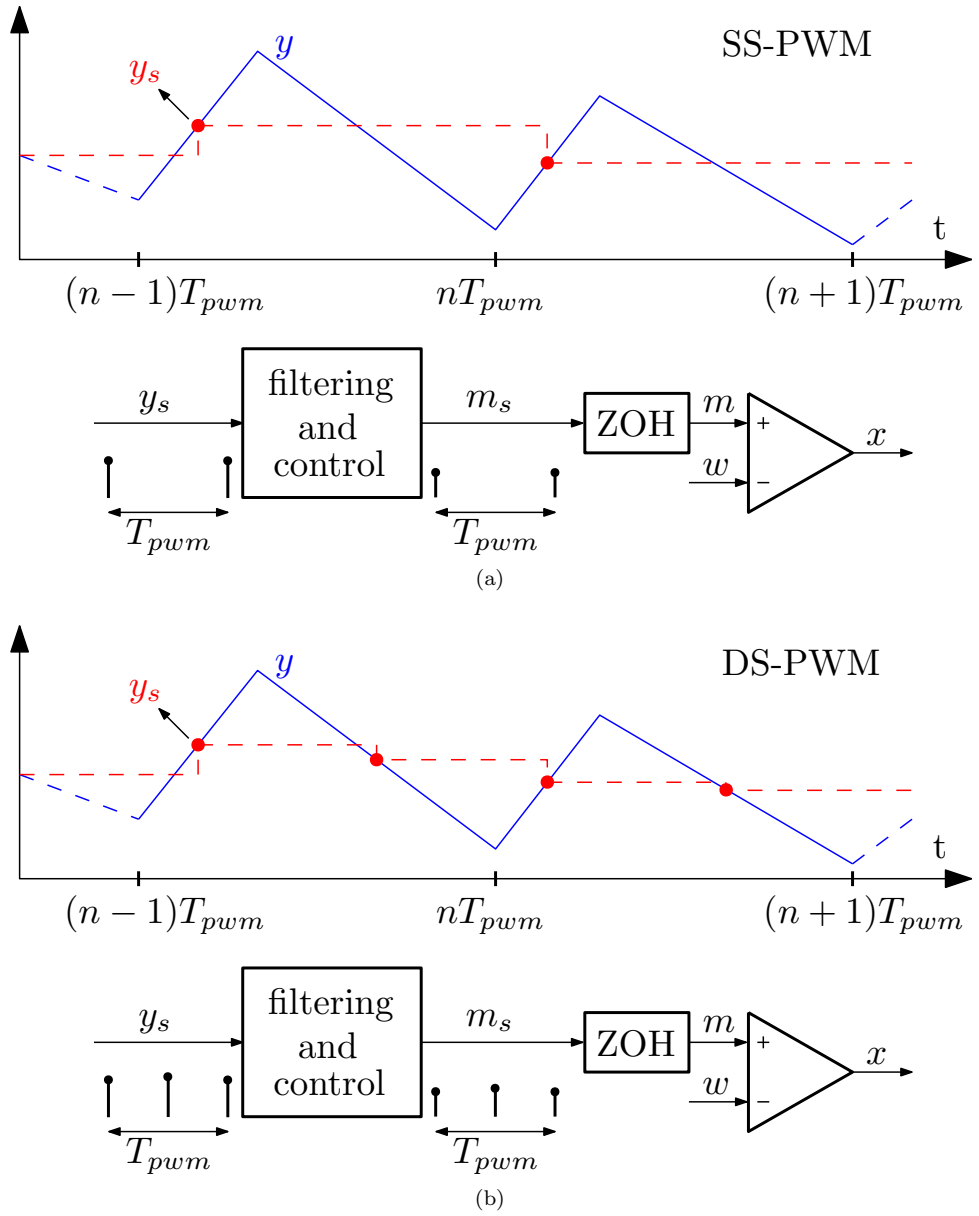


Figure 2.5: Illustration of a digital control system operating with: (a) SS-PWM and (b) DS-PWM. The feedback signal y is assumed to feature a triangular ripple shape.

The multi-sampled PWM (MS-PWM) is obtained when the sampling frequency is higher than twice the switching frequency, i.e. $f_s = Nf_{pwm}$, where $N > 2$ [18]. An illustration of a control system with

MS-PWM is shown in Fig. 2.6. Updating the controller's output more than 2 times in a modulation period means that not every sample of m_s determines an edge of x; however, as shown in Section 2.2.4, increase of N reduces the modulation delay.

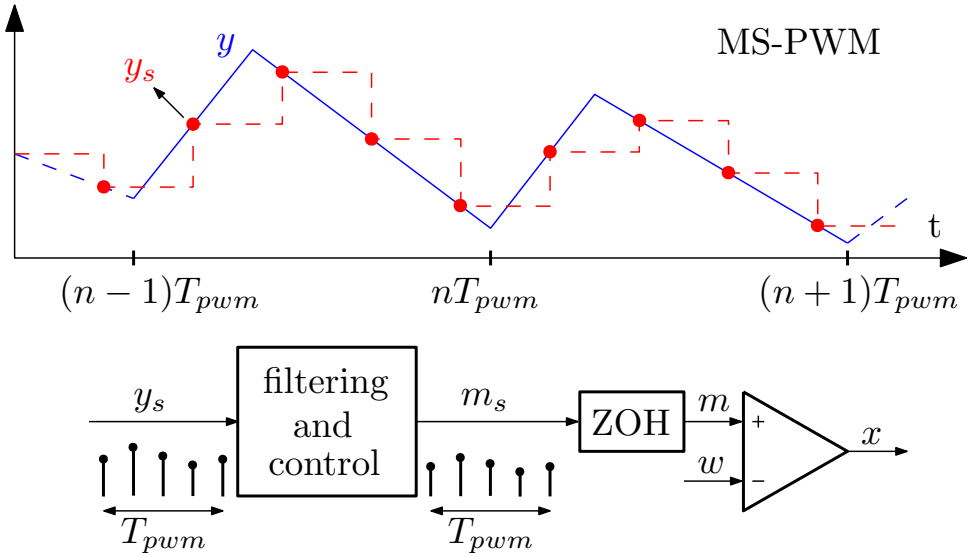


Figure 2.6: Illustration of a digital control system operating with MS-PWM. The feedback signal y is assumed to feature a triangular ripple shape.

Finally, let us mention the case of multi-rate digital control systems. A typical related scenario would be to implement filtering and control at different rates, by either adding an interpolator or a decimator after G_{fb} in Fig. 2.2. One example is the implementation of the oversampled filtering followed by the control action that is performed at a decreased rate. Note again that the control rate determines the type of US-PWM, i.e. SS-PWM, DS-PWM, or MS-PWM[5]. To differentiate these multi-rate (MR) cases from the single-rate ones, they will be labeled as MR-SS-PWM, MR-DS-PWM, and MR-MS-PWM. An example of MR-DS-PWM with a decimation between the filter and the controller is illustrated in Fig. 2.7.

There are two fundamental differences between the above-mentioned PWM types. First, a difference between NS-PWM and US-PWM is in their dynamic response capabilities. NS-PWM offers a faster large-signal response without introducing any small-signal delay [17]. This is the exact motivation for the implementation of MS-PWM. The second difference puts together SS-PWM and DS-PWM. Namely, given that y is periodic with T_{pwm}, up to two samples per period can be aligned with its average value, resulting in the cancellation of high-frequency harmonic content in y_s and, consequently, also m. Contrarily, for NS-PWM and MS-PWM, the switching harmonics are unavoidably introduced in the closed-loop system. This results in specific nonlinearities, some of which are discussed in Section 2.3.2 and some that are the focus of Chapter 4.

[5]Motivation for downsampling the filtered feedback can vary, e.g. to still use the standard SS-PWM or DS-PWM [63], or simply due to the fact that the control execution time limits the update rate. Oversampled filtering followed by a decimation to a lower-rate MS-PWM is analyzed in [72].

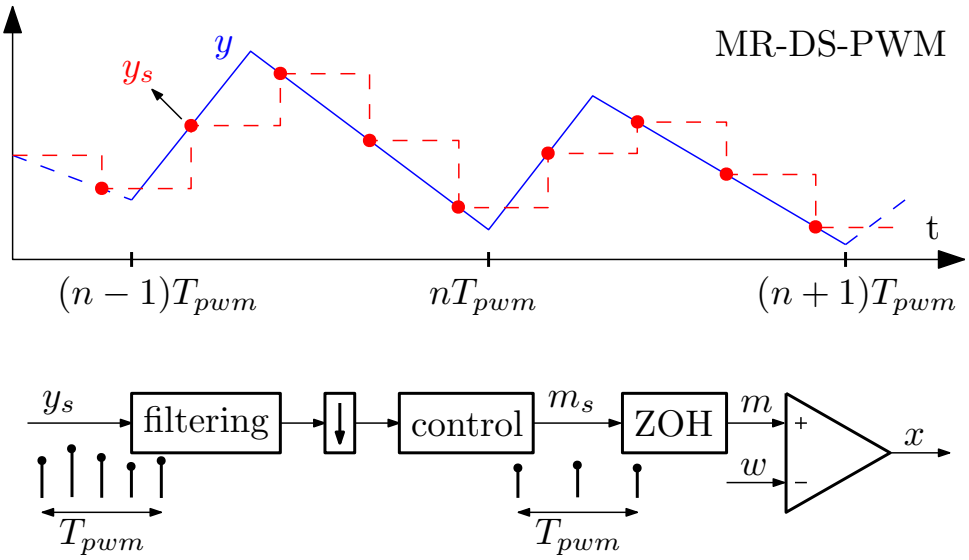


Figure 2.7: Illustration of a digital control system operating with MR-DS-PWM. The feedback signal y is assumed to feature a triangular ripple shape.

2.2.3 Classification based on carrier's waveform

Different shapes of w result in specific modulation schemes; the three typically used types are the trailing-edge, leading-edge, and symmetric dual-edge (triangular) modulators. These are illustrated in Fig. 2.8.

Let us start by introducing a convention that will be used throughout this thesis. The time axis is normalized by T_{pwm} so that all modulation properties are examined within the range $\frac{t}{T_{pwm}} \in [0,1)$. Also, the carriers are normalized and limited to $w \in [0,1]$. This results in the modulating waveform m being unitless and also bounded to range $m \in [0,1]$. The carrier parametrization that will be used throughout this thesis is:

$$w(t,\zeta) = \begin{cases} 1 - \frac{1}{\zeta}\frac{t}{T_{pwm}}, & \text{if } 0 < \frac{t}{T_{pwm}} < \zeta \\ \frac{1}{1-\zeta}\left(\frac{t}{T_{pwm}} - \zeta\right), & \text{if } \zeta < \frac{t}{T_{pwm}} < 1 \end{cases}, \tag{2.1}$$

where the trailing-edge, leading-edge, and triangular modulators are obtained for ζ equal to 0, 1, and 0.5, respectively.

The trailing-edge modulation, shown in Fig. 2.8a, uses a positive-slope sawtooth carrier. It relies on fixing the rising edge of x while the falling edge is modulated by m. The leading-edge modulation, shown in Fig. 2.8b, uses a negative-slope sawtooth carrier. It modulates the rising edge of x while the falling edge is fixed. The trailing- and leading-edge modulators can be grouped together as the single-edge ones, as they only modulate one edge of x while the other one is fixed by the corresponding infinite slope of w. For the single-edge modulators, the switching signal x is always aligned with either the beginning or the end of the modulation period. The symmetric dual-edge modulation, shown in Fig. 2.8c, uses the triangular carrier with equal rise and fall times, allowing both edges of x to be modulated.

Let us here point to a connection between the carrier type and the sampling rate of US-PWM. Namely, for a single-edge modulator, only one value of m is needed to fully determine its output x. For

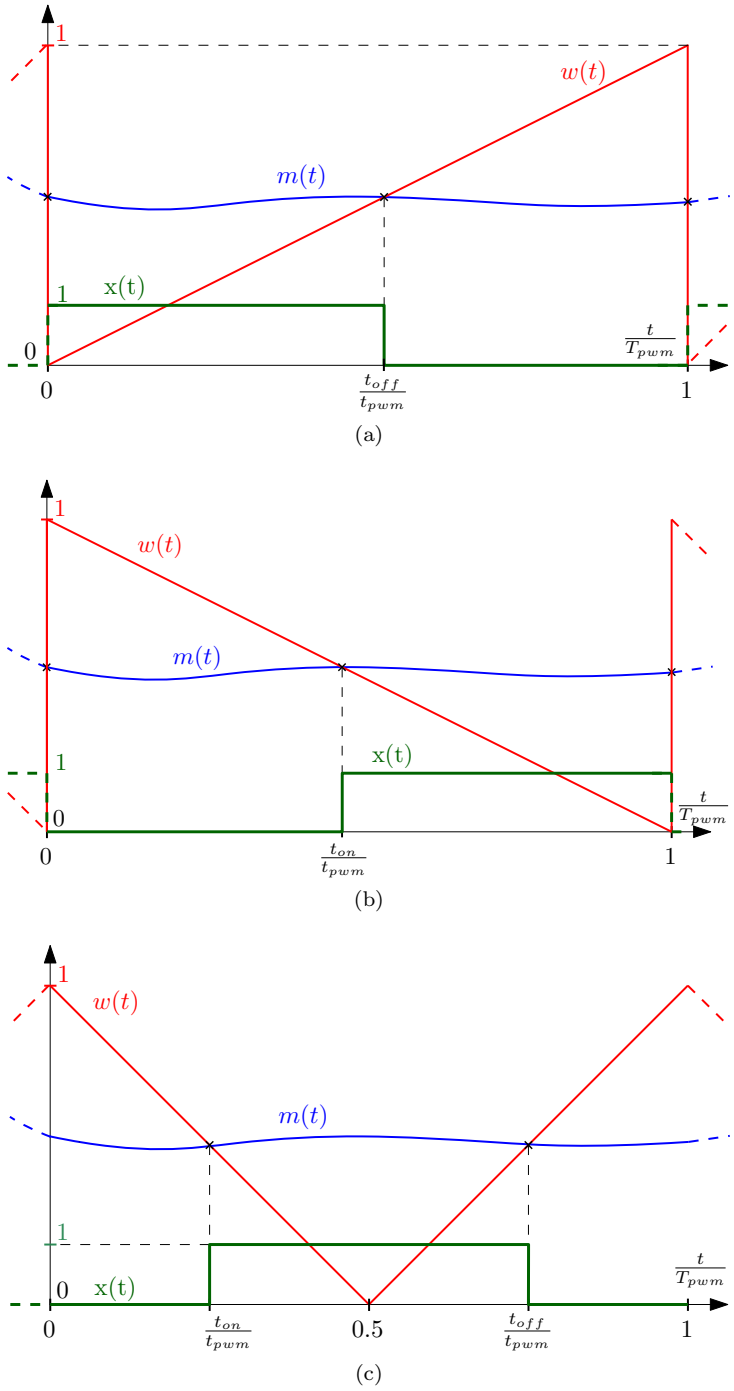


Figure 2.8: Typically used PWM carriers: (a) trailing-edge, (b) leading-edge, and (c) symmetric dual-edge (triangular). Illustrations are given for analog m, corresponding to NS-PWM.

the triangular modulator, two, possibly different, values of m are used. Therefore, a naturally-imposed choice is to use SS-PWM for the single-edge modulators and DS-PWM for the dual-edge ones. It will be shown in Chapter 5 that modulators indeed do exhibit a nonlinear re-sampling behavior, with a rate that depends on the number of modulated edges of x.

2.2.4 Small-signal US-PWM modeling

2.2.4.1 Sampling instants

Let us start by defining the sampling instants of m_s. With respect to the carrier parametrization in (2.1), the array of N normalized sampling instants within one switching period is chosen as:

$$t^l_{sample} = T_{pwm}\,(l-1)\,\frac{1}{N} \qquad , \qquad l \in [1, N]. \tag{2.2}$$

The reason behind this choice is evident for SS-PWM and DS-PWM. Namely, for the single-edge carriers with $N = 1$ and the triangular carriers with $N = 2$, the sampling instants in (2.2) correspond to the peaks or valleys of w. These values of w are suitable for the update of m_s as they do not introduce any limitation on the applicable value of D. Moreover, these instants guarantee that the modulated edge of x is determined by a horizontal crossing between m and w [27], which prevents nonlinearities that are discused in Chapter 4. For MS-PWM, additional sampling instants are uniformly distributed across T_{pwm}. This choice is arbitrary, motivated by the pioneering work in [24].

Note that, due to delays of the digital control systems, there is always a time shift between the instant at which the feedback is sampled and the instant at which the controller's output is updated. These delays arise due to the ADC acquisition time and the execution time of the digital blocks in Fig. 2.2. Hence, to allow the precise update instants in (2.2), m_s is often updated one T_s after the feedback is sampled [3]. This will be referred to as the one step computation delay. Alternatively, feedback sampling is sometimes re-scheduled in advance to the instants in (2.2) [87]. Moreover, even without the delays, sampling the feedback at instants in (2.2) is not always the optimal choice, which is briefly discussed in Section 4.3.

2.2.4.2 Modulation delay

As mentioned in Section 2.2.2, in US-PWM, the modulation delay is present due to a time difference between the instants at which m_s is sampled and the ones at which the switching actions occur. An illustration of this time difference is shown in Fig. 2.9, for the triangular carrier and two values of N. The modulation delay impacts the large-signal [47] and the small-signal [17] response.

Consider a small perturbation being applied to m_s, such that $m_s = M_s + \hat{m}_s$. Small-signal modulator modeling relies on determining the resulting response of the duty cycle, i.e. $d = D + \hat{d}$ [4]. As explained in [4], the duty cycle D is inherently a discrete-time variable, even for analog PWM; however, its continuous-time representation $d(t)$ is often used as a control input in the averaged modeling[6] [88]. Hence, the modulator modeling corresponds to finding an expression between the discrete-time $m_s[k]$ and the continuous-time $d(t)$ [27]. Small-signal modeling of SS-PWM and DS-PWM can be read in [17, 89, 90]. A generalization that covers MS-PWM is derived in [24].

The s-domain pulse-to-continuous transfer function $G_{dpwm}(s) = \frac{\hat{d}(s)}{\hat{m}_s(s)}$ is derived by finding the delays

[6] Regardless of the modeling strategy, the modulation delay is present and impacts the converter operation [4].

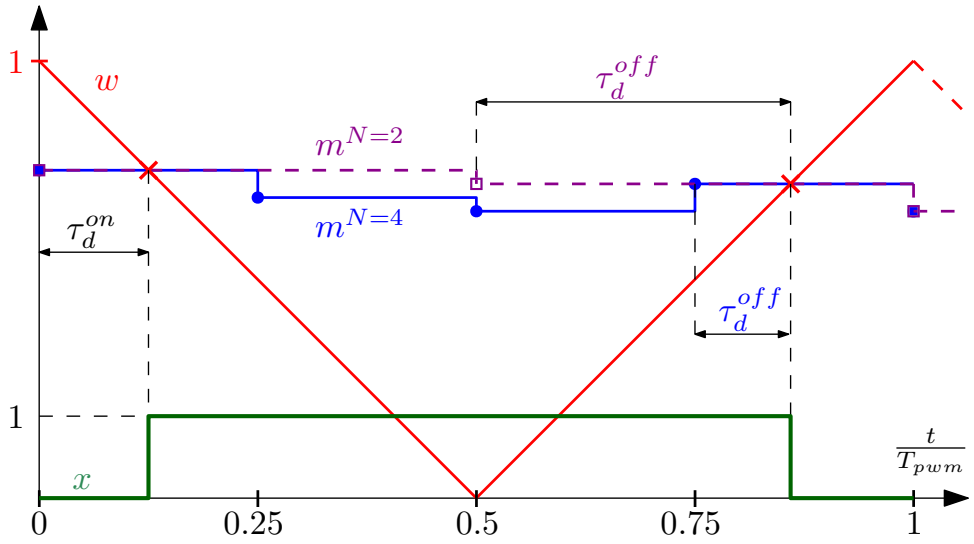


Figure 2.9: Illustration of the time difference between the sampling of m_s and the corresponding switching action, for DS-PWM ($N = 2$) and MS-PWM ($N = 4$).

between the sampling of m_s and the rising (τ_D^{on}) and falling edges (τ_D^{off}) of x [89]. These delays depend on the operating point and the oversampling factor [27]. An illustration of the US-PWM small-signal block diagram is shown in Fig. 2.10, and the corresponding modulator's transfer function is:

$$G_{dpwm}(s) = \frac{\hat{d}(s)}{\hat{m}_s(s)} = \zeta e^{-s\tau_D^{on}(D,N)} + (1-\zeta)e^{-s\tau_D^{off}(D,N)}, \tag{2.3}$$

where ζ is the parameter from (2.1) that determines the carrier type, $s = \sigma + j\omega$ is the complex variable of the Laplace transform, j is the imaginary unit, and ω is the angular frequency.

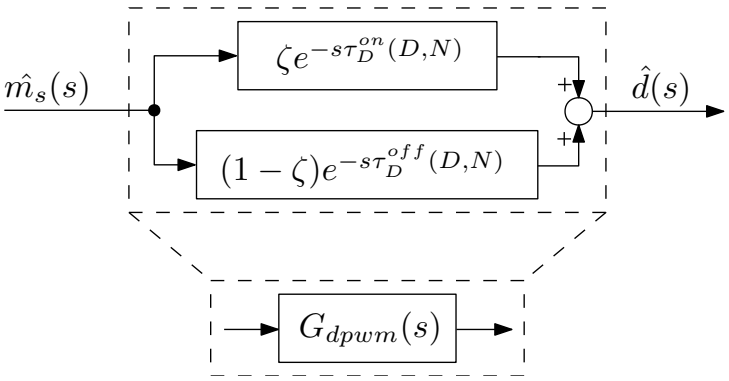


Figure 2.10: Small-signal block diagram of US-PWM modulators.

In [24], it has been shown that for the trailing-edge, leading-edge, and triangular carriers, the frequency response of $G_{dpwm}(s)$ can always be represented in the following form:

$$G_{dpwm}(j\omega) = \frac{\hat{d}(j\omega)}{\hat{m}_s(j\omega)} = A(j\omega, D, N) \cdot e^{-j\omega\Delta t_{dpwm}(D,N)}, \tag{2.4}$$

where A is a real function and Δt_{dpwm} represents the small-signal modulation delay. The gain A and

the delay Δt_{dpwm} are expressed in Table 2.1, for all analyzed carriers.

Table 2.1: Small-signal gain and delay of US-PWM modulators.

Carrier type	$A(j\omega, D, N)$	$\Delta t_{dpwm}(D, N)$
Trailing-edge	1	$(D - q_N[D])\, T_{pwm}$
Leading-edge	1	$(1 - D - q_N[1-D])\, T_{pwm}$
Triangular (N even)	$\cos\left(\omega T_{pwm}\left(\frac{D}{2} - q_N[\frac{D}{2}] - \frac{1}{2N}\right)\right)$	$\frac{T_{pwm}}{2N}$
Triangular (N odd)	$\cos\left(\omega T_{pwm}\left(\frac{D}{2} - q_N[\frac{D}{2} + \frac{1}{2N}]\right)\right)$	$\frac{T_{pwm}}{2N}$

The time-quantization parameter $q_n[\frac{t}{T_{pwm}}] = \frac{floor\left(N\frac{t}{T_{pwm}}\right)}{N}$ is defined as in [27] and corresponds to allocating the nearest preceding sampling instant.

First, it should be noted that, for all carriers, the gain A is either identically equal to, or very close to 1. Additionally, regardless of the carrier type, the introduced phase lag is decreased with the increase of N, which is expected due to the delay reduction between the sampling of m_s and the resulting switching actions. Clearly, for high values of N, MS-PWM approaches the NS-PWM and the introduced phase lag becomes negligible. The maximal achievable N depends on the available processing power relative to the switching frequency. Some application scenarios are more likely to allow high values of N (e.g. high power converters) than others (e.g. high switching frequency converters). Another important fact is that, for the trailing-edge and the leading-edge modulators, the time delay is a discontinuous function of the steady state duty cycle D. For the triangular modulators, the time delay is equal to $\frac{T_s}{2}$, which points to one of its advantages in terms of a superior linearity in MS-PWM applications [27]. Another advantage of the triangular modulator, as analyzed in [27], is the drastically lower nonlinearity induced by the switching ripple in m; the relevant effects are analyzed in Chapter 4.

Relying on the conclusions from [27], due to its superiority in MS-PWM applications, the triangular modulator is used throughout this thesis. Given that A is very close to unity, the triangular US-PWM modulator is often modelled as a transport delay in the Laplace s-domain:

$$G_{dpwm}(s) = \frac{\hat{d}(s)}{\hat{m}_s(s)} \approx e^{-s\frac{T_{pwm}}{2N}} = e^{-s\frac{T_s}{2}}. \tag{2.5}$$

The delay model from (2.5) does not capture the operating point dependency from (2.3). However, it brings a good prediction in a wide frequency range, making it suitable for most applications. A significant mismatch arises at frequencies close to the Nyquist frequency (NF) [73], which is relevant for the applications analyzed in Chapter 6.

Let us here state two important facts. First off, even though the US-PWM incorporates a ZOH, its small-signal model *does not* correspond to the one of the ZOH, which is often misinterpreted in the literature. Secondly, an important assumption used to derive the MS-PWM modulator's small signal model is that the ripple in m is small [24]. Analysis of MS-PWM operation with a non-negligible switching ripple in m is analyzed in Chapter 4.

Finally, let us mention another promising PWM carrier, which is not analyzed in this thesis. This is the asymmetric dual-edge carrier, which may bring a faster large-signal response as well as a phase-leading small-signal behavior. Its NS-PWM implementation is first analyzed in [91], while its fully-digital US-PWM implementation is recently published in [92]. The digital implementation is still limited to custom hardware, e.g. Field-Programmable Gate Array (FPGA).

2.3 Bandwidth limitations of PWM-based control systems

Bandwidth capabilities of power electronic systems are increased with higher switching frequencies. This is due to faster reaction times as well as smaller required passive filters at the output. However, the switching frequency is constrained by hardware specifications and is not a control design parameter.

Therefore, it is often a control task to achieve the maximal bandwidth for a given switching frequency. This brings many benefits such as a faster torque response and operating speed of electric drives [93,94], harmonic distortion compensation in grid-tied converters, uninterruptible power supplies (UPS), and active filters [3,25,95,96], as well as minimization of passive filters [97,98] that leads to cost reduction and higher power densities. In this section, the main bandwidth limitations in pulsewidth modulated power electronic systems are explained.

2.3.1 Small-signal limitations

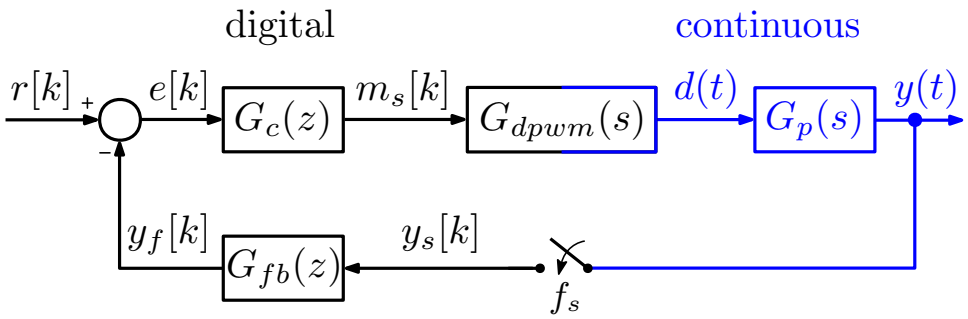


Figure 2.11: Small-signal block diagram of the system from Fig. 2.2.

Let us start by analyzing the small-signal representation of the closed-loop control system from Fig. 2.2. The corresponding block-diagram is shown in Fig. 2.11, where all signals represent the small-signal perturbations while the symbol " ˆ " is omitted. The DPWM interfaces the digital domain with the analog domain, and its small-signal transfer function is shown in the previous section. As an example, let us assume that the plant G_p is obtained using the state-space averaging technique [99]; hence, it relates the applied continuous-time duty cycle d with the converter's fed-back output y (e.g., a current through some inductor or a voltage across some capacitor). Its order depends on the output filter of the converter.

Using the standard tools of the linear control theory, the closed-loop system from Fig. 2.11 can be

analyzed in terms of its reference tracking performance, disturbance rejection, and stability margins. An important thing to notice is that the analyzed system features both the continuous and the discrete time domain. Depending on the required analysis, the transformation can be performed either from the continuous to the discrete time domain ($\mathcal{Z}\left\{\mathcal{L}^{-1}\left\{G_{dpwm}(s)G_p(s)\right\}\right\}$)[7], or from the discrete to the continuous time domain ($\mathcal{L}\left\{\mathcal{Z}^{-1}\left\{G_{fb}(z)G_c(z)\right\}\right\}$). Symbols $\mathcal{L}$ and $\mathcal{Z}$ label the Laplace and the Z transforms, respectively.

For simplicity, let us here neglect the sampler and assume that the frequency response of all individual blocks in Fig. 2.11 is known. The stability margins can be assessed using the open-loop transfer function $W_{ol}(j\omega)$:

$$W_{ol}(j\omega) = G_{fb}(j\omega)G_c(j\omega)G_{dpwm}(j\omega)G_p(j\omega). \tag{2.6}$$

Assuming a fixed crossover frequency ω_c and using $G_{dpwm}(j\omega)$ from (2.4), the phase margin can be found from (2.6) as:

$$PM = \pi + arg\{W_{ol}\left(j\omega_c\right)\} = \pi + arg\{G_p\left(j\omega_c\right)G_{fb}\left(j\omega_c\right)G_c\left(j\omega_c\right)\} - \omega_c\Delta t_{dpwm}. \tag{2.7}$$

From (2.7), it is clear that the small-signal stability is impacted by the modulation delay. Moreover, in practice, additional delays are always present due to a limited bandwidth of the sensing circuitry and the times related to the ADC acquisition, signal propagation, and the control execution. In general, for control systems with (S/D)S-PWM, the introduced small-signal phase lag is the limiting factor and the achievable bandwidths are often determined by the modulation delay [3]. Note that the phase lag can be partially compensated by adding phase-leading actions to the controller [3, 100], however, with a limited impact at high frequencies and at the expense of an increased noise sensitivity.

2.3.2 Large-signal limitations

For NS-PWM and MS-PWM with high enough N, the modulation delay is negligible. However, even without any other phase-lagging blocks in Fig. 2.11, the bandwidth cannot be set to an arbitrarily high value. Namely, all PWM-based systems feature large-signal limitations that arise for two reasons [33, 101–106]. The first one is the overlap between the bandwidth of the modulating signal m and the switching harmonic sidebands generated by the PWM [104, 105]. The second one is related to maintaining the modulation smooth by limiting the slew rate of m [33, 101–103, 106].

For the first type of large-signal limitations, let us consider the following application scenario, which may appear in both NS-PWM and US-PWM systems. The case of interest is when the modulating signal m is multi-tone, i.e. it contains a dominant fundamental-frequency (or dc) component as well

[7] As shown in [4], the impulse-invariant discretization of the averaged continuous-time dynamics is equivalent to using the direct discrete-time modeling for time-invariant topologies (e.g. buck converters).

as other harmonics. These harmonics are introduced in m either by the tracking reference or a feedback/feedforward reaction to a disturbance. A typical example may be found in an active filtering application [95]. The desired PWM behavior is that of a linear wideband amplifier, i.e. such that the bandwidth of m is faithfully replicated in its output. As noted previously, and illustrated in Fig. 2.3, by comparing m with w, PWM generates its output with the spectrum that contains components at frequencies of m, w, as well as their linear combinations (with integer coefficients). It is clear that, for m with components at high-enough frequencies, the PWM sidebands may cause an overlap. This creates an interference that resembles aliasing; hence, a criterion similar to the sampling theorem can be used to limit the bandwidth of m such that an acceptable amount of error is introduced by the modulation process.

Finding the exact bandwidth limitation requires computing the output spectrum of the switching signal x, using Bessel's functions for a given multi-tone m, and setting a limit to the introduced "aliasing" error [105]. The resulting expressions are very complex; however, a simple rule-of-thumb limitation can be found, in a manner similar to the Carson's rule [107] used in the telecommunication theory. Based on the analysis from [104], it can be shown that, for m that contains a dominant component at frequency f_1 and series of harmonics with the maximal frequency f_m^{max} and relatively small magnitudes, the lowest-frequency sideband harmonic with a non-negligible magnitude appears at the frequency $f_x^{min} = f_{pwm} - f_1 - f_m^{max}$. The bandwidth limitation is obtained by setting $f_x^{min} > f_m^{max}$, which leads to $2f_m^{max} + f_1 < f_{pwm}$. This guarantees some gap is placed between the bandwidth of m and the strong switching harmonic sidebands. A more conservative but memorable condition is obtained when f_m^{max} is set equal to f_1:

$$f_m^{max} < \frac{1}{3} f_{pwm}. \tag{2.8}$$

This limitation is often met in high-power applications, where the switching frequencies are very low. There, the carrier-based PWM is often replaced by pre-calculated switching patterns [108].

The second large-signal limitation, relevant for NS-PWM and MS-PWM, is related to maintaining the modulation smooth in the presence of switching harmonics in the modulating waveform [33,101,102,106]. To avoid considering the impact of the sampler, let us refer to the NS-PWM, while the same conclusions are brought for MS-PWM with high values of N [33]. Consider the block diagram from Fig. 2.2, where the control system is realized in the analog domain ($f_s \to \infty$). The switching harmonics, that appear due to PWM, propagate to the converter's output, after being filtered by the plant. These harmonics are then fed-back, processed by the controller and, finally, they appear in the modulating waveform m. As noted in [33,101,102,106], a condition for the smooth modulation is satisfied if the slope of m never exceeds the slope of w at their intersections. Otherwise, the modulator exhibits a chaotic, unstable operation. The magnitude of the switching ripple in m and, consequently, its slope, depend on the filtering characteristic of the entire closed-loop system and are amplified with higher controller gains. Therefore, the maximally-allowed slew rate of m limits the controller and, consequently, the achievable

bandwidth. It is important to note that the slope of m also depends on the operating point. The procedure for calculating the maximal controller gain is reported in [33].

To conclude, the bandwidth of PWM-based control systems depends on the small-signal and the large-signal effects. Which one of them will be dominant and cause a limitation depends on the sampling strategy and the physical parameters of the converter. For (S/D)S-PWM, the bandwidth is mainly limited by small-signal stability margins, which are often compromised by delays. Additionally, the bandwidth of m is limited by the allowed interference with the switching sidebands. For NS-PWM and MS-PWM, the bandwidth is generally limited by the large-signal effects, either the interference of m with the switching sidebands, or due to the slope of m with respect to w. For MS-PWM, additional nonlinearities arise due to the switching ripple in m [24, 66]; these are the main focus of the analysis in Chapter 4.

2.3.3 Filtering the switching ripple in MS-PWM

Based on the analysis from the previous section, it is clear that the presence of the switching ripple in the modulating waveform is detrimental for the operation. The switching ripple that appears in the converter's output is determined by the topology, the switching frequency, and the passive filters, which are all related to the hardware design process. Within the control domain, the switching ripple can be suppressed using appropriate filters, e.g. $G_{fb}(z)$ in Fig. 2.2.

Ripple filtering directly impacts the slope of m, which has a positive effect on enabling a smooth modulation. Moreover, in the case of MS-PWM, as discussed in Chapter 4, the switching ripple in m brings another set of nonlinearities [24, 66]. For this reason, in many MS-PWM applications, the switching ripple is completely filtered out [19, 25, 26, 34, 109]. The design goal is to remove the ripple content from m, while imposing as low as possible impact on the dynamic response. While an arbitrary filter may be used, let us here point to some structures whose application is reported in the literature.

First, let us start with the finite impulse response (FIR) moving average filter (MAF). It relies on using the N latest feedback samples to obtain the averaged output over one T_{pwm}:

$$G_{MAF}(z) = \frac{1}{N} \sum_{n=0}^{N-1} z^{-n}. \tag{2.9}$$

The MAF is widely used due to its simplicity, capability to effectively remove the switching ripple, as well as to provide a strong noise attenuation [63, 68], which is analyzed in Chapter 5. However, its big demerit is the significant added phase lag, which compromises the small-signal stability. Namely, the phase response of the MAF is close to a transport delay equal to one half of the averaging period, i.e. $e^{-s\frac{T_{pwm}}{2}}$. This value is equal to the modulation delay for SS-PWM; hence, using the MAF completely cancels the dynamic improvements obtained with MS-PWM. It should be noted that MR-SS-PWM and MR-DS-PWM are often implemented with the oversampled MAF [63, 100, 110, 111]. This is done to suppress the feedback acquisition errors, caused by an imperfect sampling synchronization, parasitic

oscillations, and various sources of noise [63]. It is clear that the difference between the average of N samples and the actual dc component of the output variable depends on the value of N.

To reduce its impact on the dynamic response, the MAF can be simply modified by using less samples for averaging. In [25], the following filter, based on two samples, is used:

$$G_{MAF,r}(z) = \frac{1}{2}\left(1 + z^{-\frac{N}{2}}\right). \tag{2.10}$$

The filter in (2.10) introduces a smaller phase lag, however, the ripple is not completely removed (the even switching harmonics remain) and the strong capability for noise suppression is lost.

Additionally, the averaging delay can be partially compensated by adding a phase-leading structure in cascade with the filter, which is analyzed in [34, 63, 100, 109]. This involves either directly applying a derivative action [63, 109] or a linear predictor [34, 100]. Both methods are structurally similar and bring an increased noise sensitivity.

A repetitive filter for ripple removal is proposed in [26]:

$$G_{RF}(z) = \frac{(1+R)\left(1 - \left(z^{-N} - \frac{1}{N}\sum_{n=1}^{N} z^{-n}\right)\right)}{1 - \left(z^{-N} - \frac{1}{N}\sum_{n=1}^{N} z^{-n}\right) + R}, \tag{2.11}$$

where the gain R determines the settling time. This structure brings a negligible phase lag below the switching frequency, which is favorable regarding the small-signal dynamics. However, as for the most repetitive filters, its settling time is relatively long. In [26], it is explained that the gain R must be set relatively low, i.e. the ripple reconstruction must be slow so that the filter would not compromise stability. There, the settling time is set to $(10 - 20)$ switching periods. Therefore, the repetitive filter is only suitable when the steady-state is kept for a long time. If it is frequently perturbed, the effectiveness of the filter is strongly limited. Moreover, it does not bring any low-pass filtering action; hence, it does not suppress the feedback noise.

Let us also mention a technique that removes the switching ripple based on prediction [19]. It relies on reconstructing the ripple component and subtracting it from the feedback. In this way, a very simple ripple removal is obtained, with practically zero delay; however, there is a high sensitivity to parameter mismatch.

In case the described filters are not suitable, a simple infinite impulse response (IIR) low-pass filter may be used to smooth the ripple in m with a low impact on the dynamic response. However, care must be taken not to trigger some of the MS-PWM specific nonlinearities, analyzed in Chapter 4.

In conclusion, there is a trade-off between suppressing the large-signal effects, by filtering the switching ripple, and maintaining the small-signal dynamic improvements obtained with MS-PWM. Therefore, there is a large degree of flexibility and space for optimization in an MS-PWM control system design.

Chapter 3

Experimental set-ups

This thesis is focused on analyzing some general properties of the multi-sampled pulsewidth modulation, regardless of the specific converter topology. For this reason, it was found that the two-level buck-type converters are suitable for an in-depth analysis of the multi-sampled modulation, without introducing an extra layer of complexity related to the topology itself.

3.1 Power converters

For all results in this thesis, two hardware systems were used, both configured as two-level buck-type converters.

The first one, referred to as the set-up A, was used in the early research stage, for part of results presented in Chapter 4, which are published in [65]. It was formed using one leg of a three-phase inverter, connected to LC output filter and resistive load. The schematic of the set-up A corresponds to Fig. 3.1a and the hardware parameters are shown in Table 3.1.

Table 3.1: Hardware parameters of the set-up A.

Description	label	value	unit
Nominal input voltage	V_{in}	200	V
Switching frequency	f_{pwm}	20	kHz
Filter inductance	L	0.6	mH
Output capacitance	C	30	μF
Output load resistance	R	30	Ω

The set-up B consists of a full-bridge buck converter, compatible with applications as a bidirectional dc-dc or ac-dc converter. The used transistor devices are FGA60N65SMD IGBTs. The input voltage supply was formed using the regenerative power system Keysight RP7962A. The switching frequency was chosen based on the used IGBTs and the inductor cores and set to 20 kHz.

For dc-dc tests in Chapters 4 and 5, the set-up B was configured as a half-bridge buck converter with LC output filter and resistive load, shown in Fig. 3.1a. This is referred to as the set-up B.1. For ac-dc

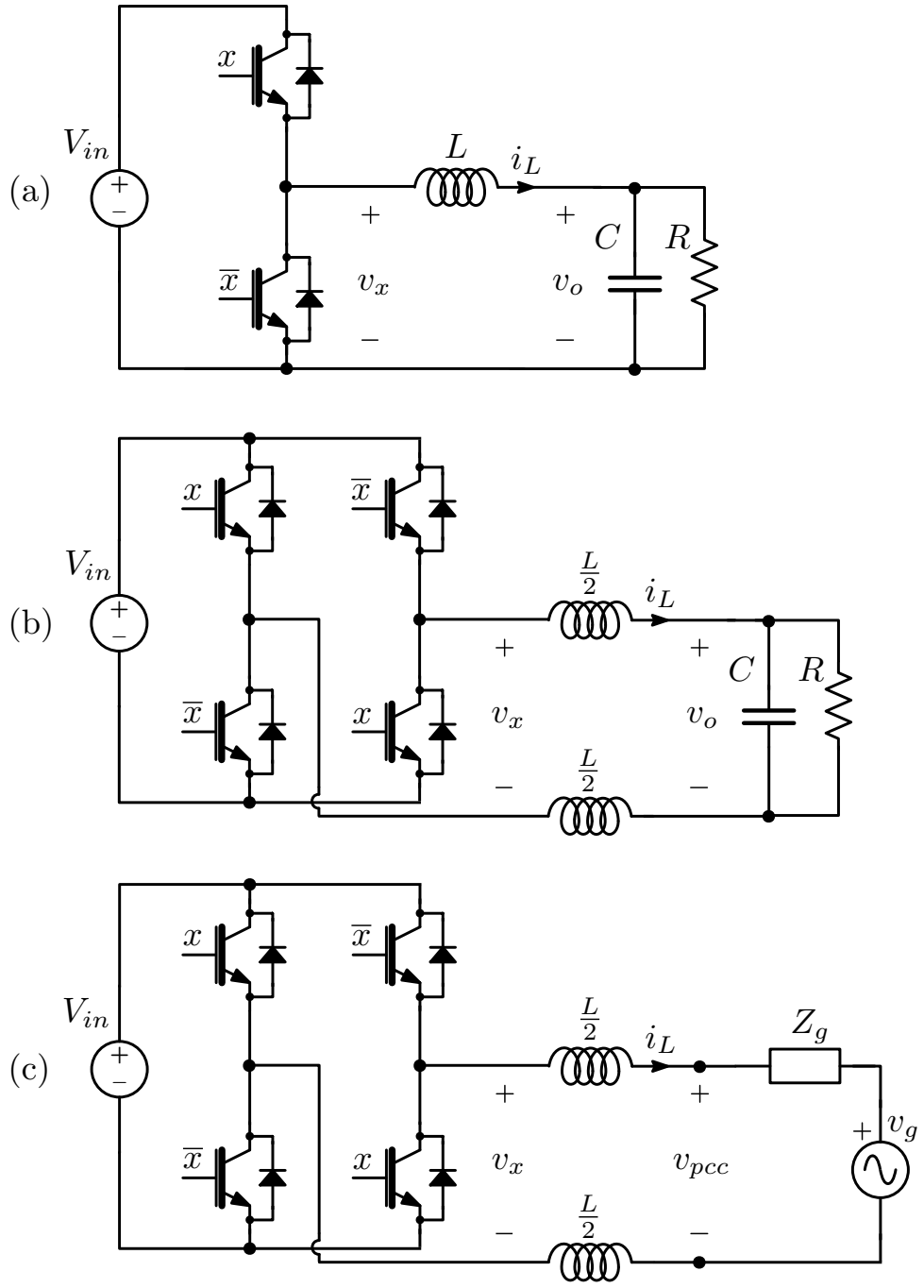


Figure 3.1: Converter topologies used in this thesis: (a) half-bridge buck converter with an *RLC* load, used in the set-ups A and B.1; (b) full-bridge buck converter with an *RLC* load, used in the set-up B.2; (c) full-bridge buck converter connected to an ac source, used in the set-up B.3.

tests in Chapter 4, the set-up B was configured as a full-bridge inverter/rectifier operating with bipolar modulation. The used coupled inductor was split between the two legs of the converter. The full-bridge configuration is again used with *LC* filter and resistive load, as shown in Fig. 3.1b. This is referred to as the set-up B.2. The parameters of the set-ups B.1 and B.2 are shown in Table 3.2.

For the grid-connected application in Chapter 6, the full-bridge configuration was connected via an

Table 3.2: Hardware parameters of the set-ups B.1 and B.2.

Description	label	value	unit
Nominal power	S_n	3	kVA
Nominal input voltage	V_{in}	400	V
Switching frequency	f_{pwm}	20	kHz
Filter inductance	L	$\{1.2, 1.5\}$	mH
Output capacitance	C	20	μF
Output load resistance	R	47	Ω
Dead time	t_{dt}	500	ns

inductive filter to a sinusoidal voltage source, formed using the Chroma 6460 programmable ac supply. This is referred to as the set-up B.3, which is illustrated in Fig. 3.1c and whose parameters are shown in Table 3.3.

Table 3.3: Hardware parameters of the set-up B.3

Description	label	value	unit
Nominal power	S_n	3	kVA
Nominal input voltage	V_{in}	400	V
Nominal PCC voltage	$v_{pcc,RMS}$	230	V
Nominal admittance	Y_n	56.7	mS
Fundamental frequency	f_1	50	Hz
Switching frequency	f_{pwm}	20	kHz
Filter inductance	L	$\{1.5, 2.5\}$	mH
Dead time	t_{dt}	500	ns

A photo of the experimental set-up B, configured for the grid-connected application (set-up B.3) is shown in Fig. 3.2.

3.2 Control platforms

For control system implementation, two digital platforms were used.

In the set-up A, the converter was controlled using a digital signal processor (DSP) from Texas Instruments C2000 series, TMS320F28379D. This will be referred to as the DSP control platform.

For all configurations of the set-up B, the control system was implemented on an NI sbRIO-9606, which is based on a Xilinix Zynq 7020 all programmable system on chip (AP-SoC). This system will be referred to as the FPGA control platform. Controlled variables are sensed using a custom interfacing board, which is re-configurable to enable current measurements (based on a shunt-resistor) and voltage measurements (based on a voltage divider). The interfacing board is built based on the original design from [112]. The board uses conditioning circuits with a high common mode rejection capability, 12 bit

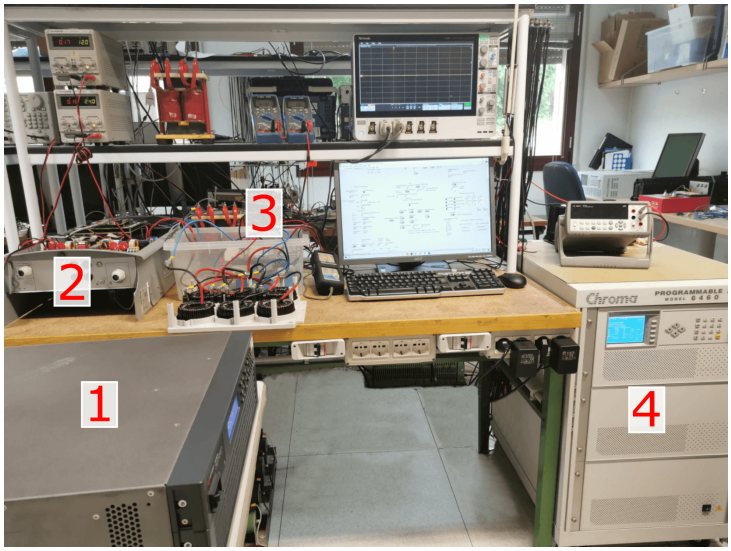


Figure 3.2: The experimental set-up B configured for the grid-connected application: (1) Keysight RP7962A, used as the input power supply; (2) converter and the control board; (3) point of common coupling with the inductor and additional filters used to form various grid impedances; (4) Chroma 6460, used as the programmable ac supply.

ADC module AD9226 by Analog Devices, and digital isolators that enable the FPGA platform to read the digital signal values at very high rates. The maximally achieved sampling rate is 40 MHz. The FPGA is programmed in LabVIEW and features a DPWM with the counter clock rate equal to 160 MHz, communication and protection systems, synchronization and control loops.

Chapter 4

Nonlinearities caused by the switching ripple

4.1 Introduction

The positive impact of multi-sampled PWM on the dynamic performance is evident from the small-signal model in (2.5). However, the underlying modeling approach from [24] relies on the assumption that the switching ripple in m is small enough. For MS-PWM, in general, this cannot be ensured without specific ripple removal filters, some of which are described in Section 2.3.3. Due to the several mentioned drawbacks of these filters, there is a motivation to further analyze the MS-PWM operation with a non-negligible switching ripple content in m.

The focus of this chapter is the analysis of the modulator nonlinearities that are caused by the switching ripple. Three sets of analyzed nonlinearities are those due to *aliasing*, *ripple modulation*, and *modulating waveform discontinuities*. The aliasing problems are present only in digital control systems. The effects caused by the ripple modulation [31–33, 88, 113, 114] are found in both NS-PWM and MS-PWM. The modulating waveform discontinuities are uniquely related to MS-PWM; moreover, it will be shown that their impact is emphasized for lower oversampling factors. The first two types of nonlinearities are only briefly discussed here, being covered by the previously published work. The third one is analyzed in detail, and the corresponding results are one of the main contributions of this thesis.

Regarding the effects caused by the modulating waveform discontinuities, the focus of this chapter is first placed on explaining each specific nonlinearity that may arise. Their impact is manifested through the reduced-gain [24], zero-gain [24], and infinite-gain [65] zones of the modulator. The discovery and analysis of the infinite-gain zones is one of the original contributions of this thesis. It is shown that the infinite-gain zones may result in limit cycle oscillations, bringing a highly detrimental impact on a converter's operation. This effect is statistically modelled and an algorithm is proposed to cancel out the induced oscillations. Additionally, this chapter brings a generalized methodology suitable to predict

which nonlinearity will appear, depending on the control system parameters. The corresponding findings are published in [65, 66]. The main results of this chapter can be summarized as:

- Analysis and classification of the MS-PWM nonlinearities caused by the modulating waveform discontinuities. Specifically, the infinite-gain zones are introduced for the first time.
- A methodology for predicting the appearance of MS-PWM nonlinearites and quantifying the resulting effects.
- A framework for designing the control system so as to suppress or even completely cancel the discontinuity-related MS-PWM nonlinearities, without needing to remove the switching ripple.

4.2 Converters under test

The phenomena described in this chapter are directly related to the shape of the switching ripple in the modulating waveform, which depends on the converter topology and the control system structure. In this chapter, the experimental results are given for two-level current-controlled buck-type converters. Specifically, the hardware set-ups A, B.1, and B.2, described in Section 3.1, are used. The corresponding schematics are shown in Fig. 3.1.

Numerical results reported in this chapter correspond to these systems; however, the presented methodology can be extended to other topologies and controller structures, operating with multi-sampled pulsewidth modulation, without any particular challenges.

4.2.1 Controller design

For the analysis in this chapter, single-stage current control systems are considered. Current control was found suitable to address the modulator's properties in the presence of strong switching harmonics. The cut-off frequency of the output LC filter is chosen to be sufficiently low, such that the output voltage dynamics are negligible. An illustration of the implemented digital control system is shown in Fig. 4.1, assuming the half-bridge buck configuration.

Let us start the analysis in s-domain, which is often a viable approach for the controller design [3]. A simplified s-domain representation of the system from Fig. 4.1, where the feedback filter and the modulation delay are neglected, is shown in Fig. 4.2. As the buck-type converters are large-scale linear, in all expressions the small-signal label " ˆ " will be omitted.

For the analyzed two-level converters, there is only one active switching signal x. The switched node voltage of the converter v_x is determined by the switching signal and the input voltage, i.e. for the half-bridge configuration it is equal to $v_x(t) = x(t)V_{in}$, while for the full-bridge with bipolar modulation it is equal to $v_x(t) = (2x(t) - 1)V_{in}$. It is assumed that the input voltage dynamics are negligible. Using the averaged modeling, the one-cycle average of v_x is related to the input voltage using the continuous duty cycle $d(t)$ as the control variable [75, 99]. Therefore, neglecting the modulation block, the controller can

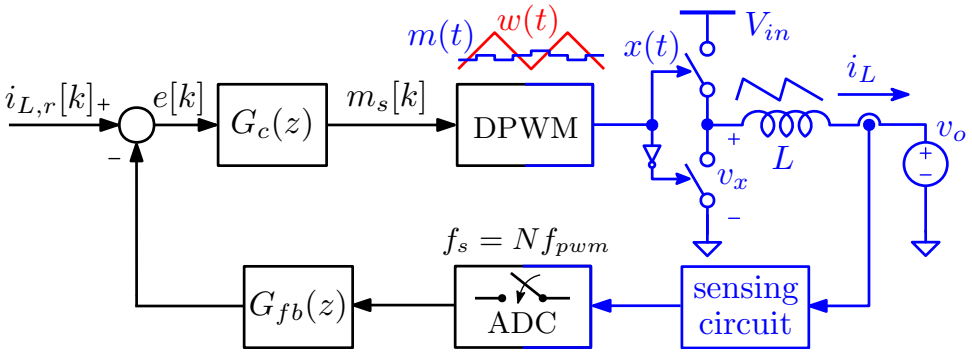


Figure 4.1: A digital current control system of a two-level half-bridge buck converter. The inductor current i_L is sampled by the ADC, processed by a digital filter G_{fb}, and subtracted from the reference $i_{L,r}$. The resulting error signal e is processed by the controller G_c to obtain m_s. The modulating waveform m is obtained after the ZOH processing of m_s within the DPWM.

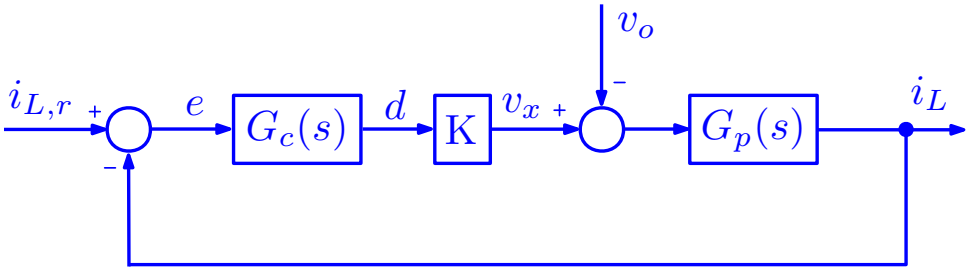


Figure 4.2: S-domain small-signal block diagram of current-controlled buck-type converters, without including the feedback filter and the modulation delay.

be seen to output the required duty cycle of x, which determines the applied switched node voltage as $v_x = d \cdot K + V_x^0$, where K is the gain and V_x^0 is the dc offset[1]. For the half-bridge configurations, $K = V_{in}$ and $V_x^0 = 0$. For the full-bridge configurations with bipolar modulation, $K = 2V_{in}$ and $V_x^0 = -V_{in}$. The switched node voltage, together with the disturbance v_o, determines the inductor current response as:

$$G_p(s) = \frac{i_L(s)}{v_x(s) - v_o(s)} = \frac{1}{sL}. \tag{4.1}$$

Let us now present the typically used controller structures, for the inner current control loops, corresponding to Fig. 4.2. Given that the analyzed plant model in (4.1) is an integrator, a zero steady-state error can be achieved using just proportional control, i.e.:

$$G_c^P = k_p, \tag{4.2}$$

where k_p is the proportional gain. For the set crossover frequency f_c, the proportional gain is calculated as $k_p = 2\pi f_c \frac{L}{K}$. As explained in Section 2.3, the maximal crossover frequency is limited by the control delays (which are left out of the small-signal block diagram in Fig. 4.2) and the switching frequency [3, 33].

[1]The offset does not impact the small-signal analysis, which is why it is left out of the block diagram.

For dc-dc converters, to improve robustness against the model uncertainties and other disturbances, an integrator is often added to form the proportional-integral (PI) controller [3]:

$$G_c^{PI} = k_p + k_i \frac{1}{s} = \frac{k_p s + k_i}{s} = k_p \frac{s + \omega_i}{s}, \tag{4.3}$$

where k_i is the integral gain and $\omega_i = \frac{k_i}{k_p}$ is the angular frequency of the zero added by the integral action. An often used PI controller design strategy is to calculate k_p like for the P controller, while the zero of the integral gain is placed such that its impact at the crossover frequency is negligible [3], e.g. $\omega_i = \frac{k_i}{k_p} < 0.1 \cdot 2\pi f_c$.

In case of converters with a sinusoidal ac operating point, the integrator can be replaced with a resonator [115, 116]:

$$G_c^{PR} = k_p + k_r \frac{s}{s^2 + \omega_1^2}, \tag{4.4}$$

where k_r is the resonant gain and ω_1 is the angular frequency of the sinusoidal reference. As the resonant action corresponds to the integral action observed in a rotating reference frame [3], the same design approach as for k_i of the PI controller is often used, i.e. $\frac{k_r}{k_p} < 0.1 \cdot 2\pi f_c$.

The analysis found in this chapter can be directly extended to any linear controller; however, these structures (P, PI, PR) and their combinations are most often used for single-stage current-controlled converters. An important property of these controllers is that, at high frequencies ($\omega \to \infty$), their frequency response converges to the one determined by the proportional gain. For this reason, they will be referred to as the *high-frequency proportional-dominant* controllers.

4.2.2 Impact of the control system on the modulating waveform shape

From Fig. 4.1, it can be seen that the current ripple propagates to m_s after being processed by the sensing circuits, the ADC, the feedback filter, and the controller. It is clear that all of these blocks, together with the ZOH of the DPWM, have an impact on the shape of ripple in the modulating waveform.

Let us start by analyzing the impact of the controller itself, using the standard structures introduced in the previous section. Other blocks, such as the feedback filter, will be used to modify the shape of m throughout this chapter. Additionally, the impact of the controller will be first examined assuming an analog control system, shown in Fig. 4.3, such that the continuous-time m is observed. The sampled-and-held version of m, present in MS-PWM, is related to this continuous-time waveform [24], making it useful for bringing some general conclusions before going into the sampled nature of the system.

Let us separate the inductor current as $i_L(t) =< i_L > + i_L^{ac}(t)$, where $< i_L >$ is its average value over one T_{pwm} and i_L^{ac} is its ripple component.

In order to provide results that have a general value, the following reasoning is made. For the analyzed two-level buck converters with constant output voltage, the inductor current ripple is triangular, with slopes that depend on V_{in}, L, f_{pwm}, and the steady-state duty cycle D [75]. Its peak-to-peak value Δi_L^{p-p} can be found as:

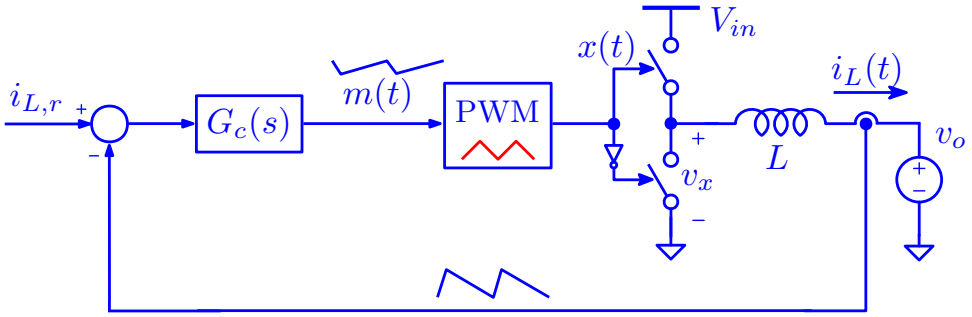


Figure 4.3: Block diagram of the analog current control system used to examine the impact of the controller on the modulating waveform ripple.

$$\Delta i_L^{p-p} = f(D)\frac{V_{in}}{Lf_{pwm}}, \tag{4.5}$$

where $f(D)$ is determined by the topology configuration. For the half-bridge buck-type converters $f(D) = D(1-D)$, while for the full-bridge buck-type converters with bipolar modulation $f(D) = 2D(1-D)$ [75].

In the same way, the modulating waveform is separated in two parts as $m(t) =< m > +m^{ac}(t)$. Since the switching frequency is always above the feasible control bandwidths, the ripple component i_L^{ac} propagates to the modulating waveform as if the system is in the open-loop configuration. Starting with the proportional controller in (4.2), it is clear that:

$$m^{ac}(t) = -k_p i_L^{ac}(t). \tag{4.6}$$

For P controllers, m^{ac} completely retains the shape of i_L^{ac}. In case of PI or PR controllers with gains designed as in the previous section, the impact of the integral or the resonant action is bandlimited well-below the crossover frequency; hence, also below the switching frequency. Consequently, for these high-frequency proportional-dominant controllers, the modulating waveform ripple is well approximated by (4.6). Using (4.5) and the relation between the proportional gain and the crossover frequency of the system shown in Fig. 4.2, it is possible to correlate the steady-state peak-to-peak magnitude of the modulating waveform Δm_{p-p} with the designed relative crossover frequency $f_{c,r} = \frac{f_c}{f_{pwm}}$:

$$\Delta m_{p-p} = k_p \Delta i_L^{p-p} = 2\pi f_c \frac{L}{K}\Delta i_L^{p-p} = 2\pi f_c \frac{L}{K} f(D)\frac{V_{in}}{Lf_{pwm}} = 2\pi f_{c,r} D(1-D). \tag{4.7}$$

From (4.7) it is clear that the modulating waveform ripple is simply proportional to the designed value of $f_{c,r}$, independently from the specific values of V_{in} and L. Moreover, it is equal for the half-bridge and the full-bridge buck converters. The expression (4.7) is a very close approximation for all mentioned high-frequency proportional-dominant controllers; hence, it can be concluded that these controller structures will bring very similar properties related to nonlinearities caused by the modulating waveform ripple. For other linear controllers, such as those involving a derivative action, the modulating waveform ripple is strongly affected by the controller; hence, their analysis must be conducted independently.

Based on the considerations above, it is concluded that the investigation of the ripple-induced nonlinearities can be performed in a scalable way, by varying only the relative crossover frequency of control loops with the high-frequency proportional-dominant controllers. This is found useful for bringing generalized conclusions, regardless of the exact values of f_{pwm}, V_{in}, L, k_r, and k_i. Note that, for LC output filters where the resonant frequency is near the crossover frequency, the plant cannot be modeled as a simple integrator from (4.1). Hence, the actual crossover frequency differs from $\frac{k_p K}{2\pi L}$. In those cases, the subsequent analysis is dependent on the designed value of k_p and not the obtained value of f_c.

4.3 Aliasing in digitally controlled power converters

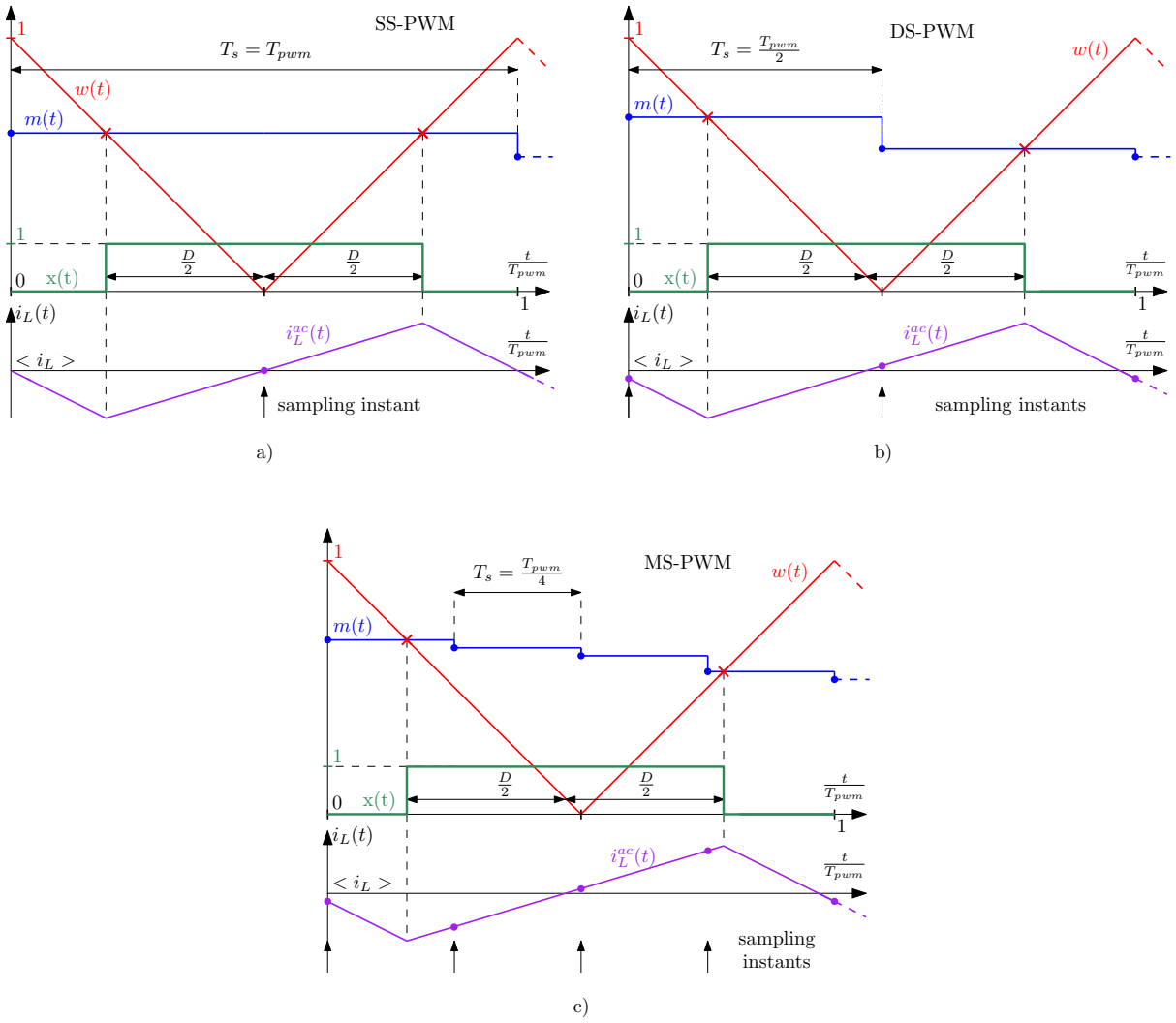


Figure 4.4: Illustration of the sampling instants from (2.2), for the inductor current control loop with negligible output voltage dynamics for: (a) single-sampled (SS-PWM), (b) double-sampled (DS-PWM), and (c) multi-sampled (MS-PWM) with $N = 4$.

In digitally controlled power converters, aliasing-related issues may arise as the switching ripple is sampled [26, 34]. The switching harmonics cannot be fully removed using analog anti-aliasing filters,

unless completely deteriorating the closed-loop dynamics. Therefore, without high oversampling, the bandwidth of the feedback signal is always above the Nyquist frequency and the aliasing is bound to occur. This is particularly evident in the inner inductor current control loops, which experience the strongest switching harmonic content [3].

For SS-PWM and DS-PWM, the feedback sampling instants can be chosen to align with the one-cycle average of i_L, which results in the direct removal of the switching ripple component [3]. For the analyzed two-level inductor current control loops, neglecting any parisitic resistances and the output voltage dynamics, these instants coincide with the mid-points of the switching signal $x(t)$. This kind of sampling synchronization is referred to as the *center-pulse sampling*.

For SS-PWM and the triangular carrier, neglecting the presence of any delays, the mid-points of x coincide with the peaks or valleys of the carrier, depending on when the modulating waveform is updated. An example is shown in Fig. 4.4a, where the modulating waveform is updated once per T_{pwm} at each peak of $w(t)$, with the corresponding center-pulse instant being found at the valley of $w(t)$. However, the presence of dead times and actuation delays always causes x to be, at least slightly, shifted. Moreover, with the parasitic resistances and a non-constant output voltage, the average value of i_L no longer coincides with the mid-points of x. In practice, for SS-PWM, these effects result in a low-frequency acquisition error that can be suppressed by re-scheduling the sampling instants accordingly [117].

For DS-PWM and the triangular carrier, it is often assumed that synchronizing the sampling instants with the peaks and valleys of the carrier results in the center-pulse sampling. However, even without any dead times or delays, the switching signal may be asymmetric with respect to the carrier, resulting in the switching ripple being sampled. This is illustrated in Fig. 4.4b. Therefore, for DS-PWM, besides the low-frequency aliasing, the switching harmonics may also be introduced in the feedback signal unless the sampling instants are dynamically adjusted. This effect brings one of the motivations for highly oversampling the feedback and then averaging it over one switching period, i.e. MR-DS-PWM [63].

For MS-PWM, $N > 2$ samples are taken within a switching period; hence, the ripple is unavoidably sampled. In case the average of N consecutive samples differs from $< i_L >$, a low-frequency aliasing error is introduced. An example of MS-PWM with $N = 4$ and the sampling instants from (2.2) is shown in Fig. 4.4c. Intuitively, the low-frequency aliasing is less emphasized for higher oversampling factors, as the average value of the sampled feedback comes closer to the one-cycle average value $< i_L >$.

In case the digital control system features outer loops that generate a dc current reference, the aliasing issues may be less critical as the resulting dc offset would be compensated by the outer controller. In case the current reference is an ac signal, the aliasing may cause a distortion [34,66]. A detailed analysis of the aliasing-related problems is out-of-scope of this thesis; however, it is an important and under-investigated topic related to MS-PWM.

4.4 Ripple modulation

In this section, the ripple modulation effect is explained by first introducing the concept of the modulator's gain. The ripple modulation is well-documented for NS-PWM and, as it will be shown later on in this chapter, its impact remains practically unchanged for MS-PWM with high values of N. The following analysis assumes the implementation of NS-PWM, to simply introduce general notions that are later extended to the analysis of the MS-PWM nonlinearities.

4.4.1 Gain of the pulsewidth modulator

A way to describe the pulsewidth modulator as an actuator is through its static transcharacteristic [24]. This function relates the steady-state value of the PWM output duty cycle D with the average value of the modulating waveform over one switching period, $< m >$. The slope of the transcharacteristic, labeled as $k_{mod} = \frac{\mathrm{dD}}{\mathrm{d<m>}}$, will be referred to as the modulator's gain. It is important not to misconstrue this static gain with the one from the small-signal model, which does not take ripple into account.

It is well known that the gain of NS-PWM depends on the switching ripple in $m(t)$; this effect is termed the *ripple modulation* [31–33, 88, 113, 114]. A detailed analysis and derivations for the gain of single edge modulators in the presence of the switching ripple can be read in [32, 113, 114].

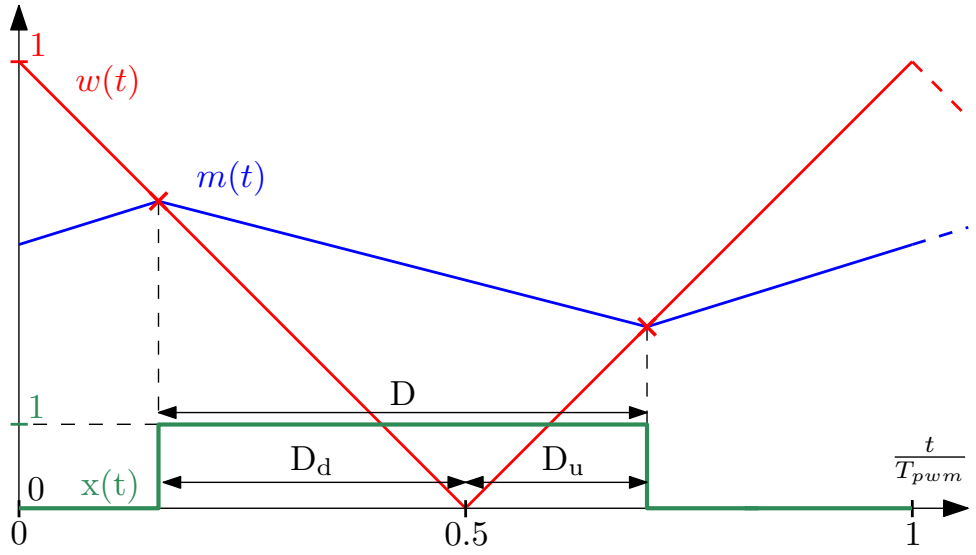


Figure 4.5: Illustration of NS-PWM for a modulating waveform with the triangular ripple.

In this thesis, detailed derivations are omitted and only a simple illustration of the effect is presented. An example of NS-PWM operation with triangular ripple in m is shown in Fig. 4.5. The duty cycle D of the converter is represented using the sum of the up-count (positive slope of w) duty cycle D_u and the down-count (negative slope of w) duty cycle D_d:

$$D = D_u + D_d = \frac{\Delta t_{on,u}}{T_{pwm}} + \frac{\Delta t_{on,d}}{T_{pwm}}, \tag{4.8}$$

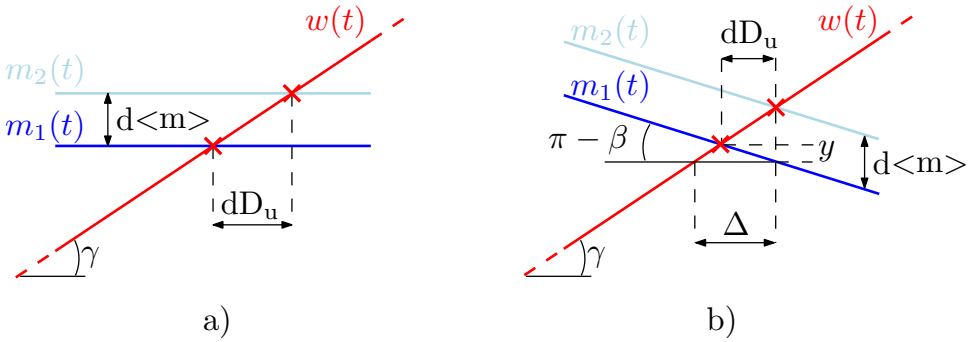


Figure 4.6: Illustrations for calculating the modulator's gain in case of m with: (a) no ripple, (b) triangular ripple with slope β.

where $\Delta t_{on,u}$ is the on-time of the switching signal $x(t)$ during the positive slope of w and $\Delta t_{on,d}$ is the on-time during the negative slope of w. The introduced quantities, D_u and D_d, are referred to as the *partial duty cycles*. To illustrate the impact of the switching ripple, two distinct cases are shown in Fig. 4.6, where the modulating waveform is slightly perturbed such that $< \mathrm{m}_2 > = < \mathrm{m}_1 > + \mathrm{d} < \mathrm{m} >$. Focusing on the positive slope of w, the result of applying the perturbation $\mathrm{d} < \mathrm{m} >$ is a change of the corresponding partial duty cycle $\mathrm{dD_u}$.

First, let us observe the case without the switching ripple in m, seen in Fig. 4.6a. It is straightforward to conclude that:

$$\frac{\mathrm{dD_u}}{\mathrm{d} < \mathrm{m} >} = \frac{1}{tg(\gamma)}, \tag{4.9}$$

where γ defines the slope of w. In this case, the perturbation $\mathrm{d} < \mathrm{m} >$ yields an equal response for both slopes of the triangular carrier, i.e. $\mathrm{dD_u} = \mathrm{dD_d}$. Therefore, it can be concluded that the resulting modulator's gain is equal to $k_{mod} = \frac{2}{|tg(\gamma)|}$. For the normalized triangular carrier, the counter slope is equal to $tg(\gamma) = 2$, which results in $k_{mod} = 1$. For the trailing-edge and leading-edge carriers, the slope of w is decreased to $|tg(\gamma)| = 1$ and only one edge of x is being modulated; hence, again $k_{mod} = 1$. It is clear that the unity gain will be present also for US-PWM, if the switching ripple is not sampled or is completely removed by filtering.

Now, let us observe the case where m contains the triangular switching ripple, as seen in Fig. 4.6b. Again focusing on the positive slope of w, a few geometrical identities allow us to find the response to the perturbation $\mathrm{d} < \mathrm{m} >$. The slope of m, just before its intersection with w, is defined by the *tangent* of the angle β. The set of equations necessary to find the modulator's gain is:

$$\begin{aligned} \Delta &= \frac{\mathrm{d} < \mathrm{m} >}{tg(\gamma)} \\ \frac{\Delta - \mathrm{dD_u}}{y} &= \frac{\Delta}{\mathrm{d} < \mathrm{m} >} \\ \frac{y}{\mathrm{dD_u}} &= tg(\pi - \beta) = -tg(\beta). \end{aligned} \tag{4.10}$$

From (4.10), it is straightforward to find the resulting response of D_u:

$$\frac{\mathrm{dD_u}}{\mathrm{d} < \mathrm{m} >} = \frac{1}{tg(\gamma) - tg(\beta)} = \frac{1}{tg(\gamma)} \frac{1}{1 - \frac{tg(\beta)}{tg(\gamma)}}, \tag{4.11}$$

which reduces to (4.9) for the slope $tg(\beta)$ equal to zero, i.e. for m without the switching ripple. For the triangular carrier and m that contains switching ripple, correlating (4.11) with k_{mod} is not trivial as $\mathrm{dD_u}$ and $\mathrm{dD_d}$ may differ, even in their signs. This fact is mentioned to result in a time variant modulator's gain for the triangular carriers [32]. However, the principles regarding the gain dependency on the slope of m at the intersection with w remain similar.

Let us introduce here, for the first time, the terms *in-phase* and *counter-phase* operation. The modulator operation is referred to as the *in-phase* if the derivative of $m(t)$, just before its intersection with $w(t)$, has the same sign as the derivative of $w(t)$, i.e. $tg(\gamma) \cdot tg(\beta) > 0$. The modulator operation is referred to as the *counter-phase* if the derivative of $m(t)$, just before its intersection with $w(t)$, has the opposite sign to the derivative of $w(t)$, i.e. $tg(\gamma) \cdot tg(\beta) < 0$. From (4.11), it is clear that, with respect to the partial duty cycle D_u, the *counter-phase* operation decreases the gain, while the *in-phase* operation increases it. As explained in Section 4.2.2, for the high-frequency proportional-dominant controllers, the modulating waveform ripple is just an inverted and scaled version of the feedback variable's ripple. For buck converters with a constant output voltage, the switching ripple in i_L is determined by the integral of the switching signal x; hence, without any filters or delays, m and w are always in the *counter-phase* relation (as seen in Fig. 4.5). However, with the introduction of delays or high-frequency filtering, the relation between m and w can change to the *in-phase* one. Similar conclusions are brought in [113].

As the switching ripple shape and, hence, the slope $tg(\beta)$, depend on the duty cycle, it is clear that the *ripple modulation* causes the modulator's gain to be operating point dependent. In [31] it is reported that this effect can be partially compensated for the single-edge modulators, by pre-distorting the carrier.

4.4.2 Calculating the modulator transcharacteristic for NS-PWM

In this section, the procedure for calculating the modulator transcharacteristic is presented for NS-PWM. The extension to MS-PWM is given in Section 4.5.4.1.

To calculate the modulator's static transcharacteristic, it is necessary to find the steady-state waveform $m(t)$ with respect to $w(t)$ inside one switching period of the converter.

For this, it is first necessary to find the ripple component m^{ac}. This waveform can be calculated analytically by solving a set of differential equations that describe the closed-loop control system. For the supposed steady-state duty cycle D, the converter's circuit is solved for all topological states and the ripple in the output waveform is found. If the control loop features any feedback filtering, the corresponding set of differential equations is used to find the filtered ripple component. The filtered output ripple is then used to solve the set of controller-related equations taking into account the negative feedback sign, which results in m_1^{ac}. Finally, an arbitrary amount of time delay $t_d = \tau_D T_{pwm}$ is added

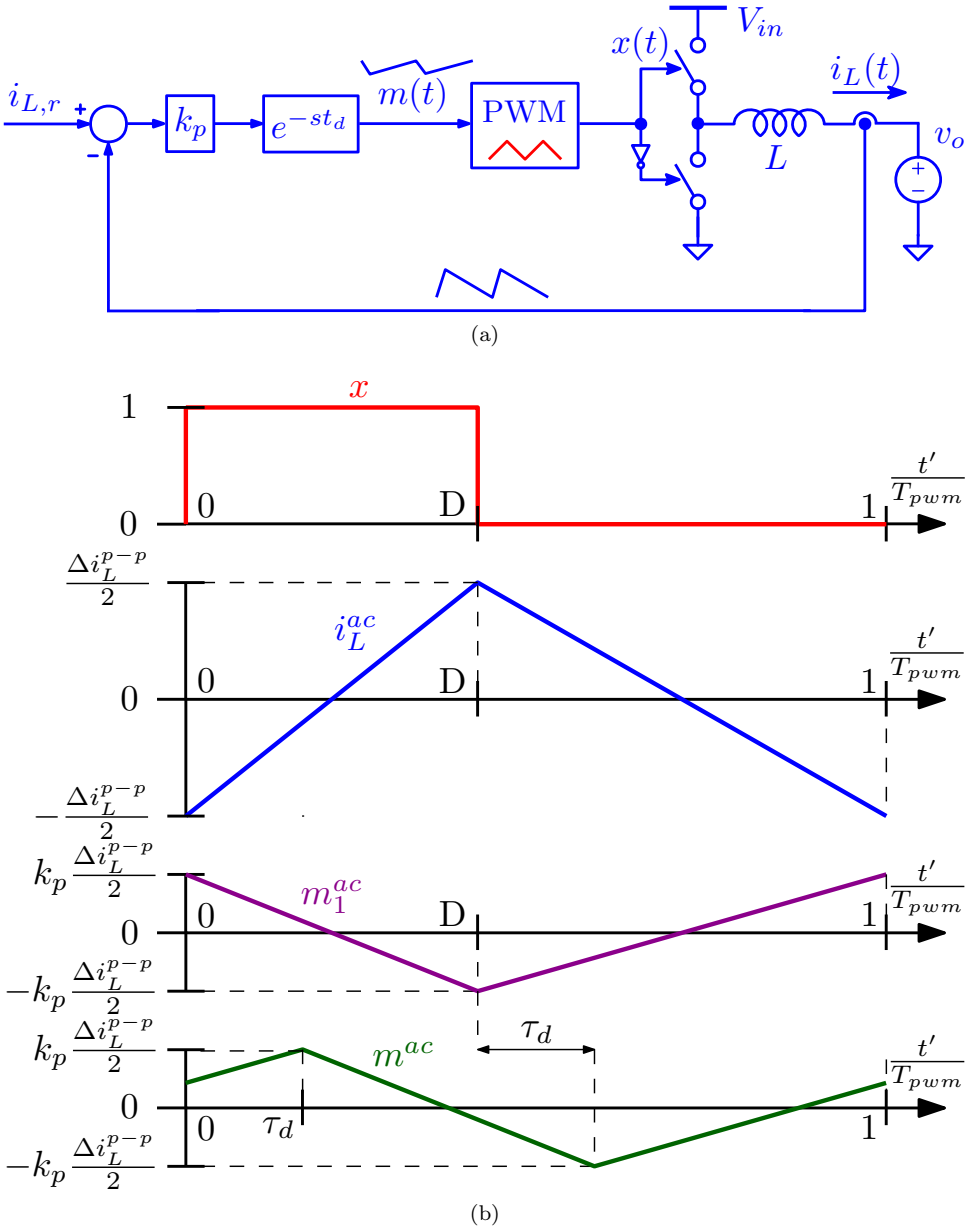


Figure 4.7: (a) Illustration of a current control loop, for a buck converter with a constant output voltage. The control system features a proportional gain and a delay t_d. (b) The corresponding switching ripple components.

to obtain m^{ac}. As mentioned in the previous section, the time delay can impact the slope of m at the intersection with w and, hence, also the modulator's gain. It will be shown in the following sections that the time delay also plays a crucial role in determining the types of nonlinearities that arise with MS-PWM.

The procedure described above is illustrated in Fig. 4.7 for the proportional current control, without feedback filters. It is assumed that the output voltage is constant and that the converter operates in steady-state. It is important to notice that the resulting ripple component m^{ac} is found relative to the applied switching signal x and its shape does not depend on the position of the actual switching instants,

determined by the intersections of m and w. For this reason, the time is labeled as t' in Fig. 4.7b, to emphasize that it is not synchronized with the carrier but with the turn-on instant t_{on} of x. As an illustration corresponding to Fig. 4.7 with $\tau_d = 0$, Fig. 4.8 is given. It is clear that $t' = t - t_{on}$.

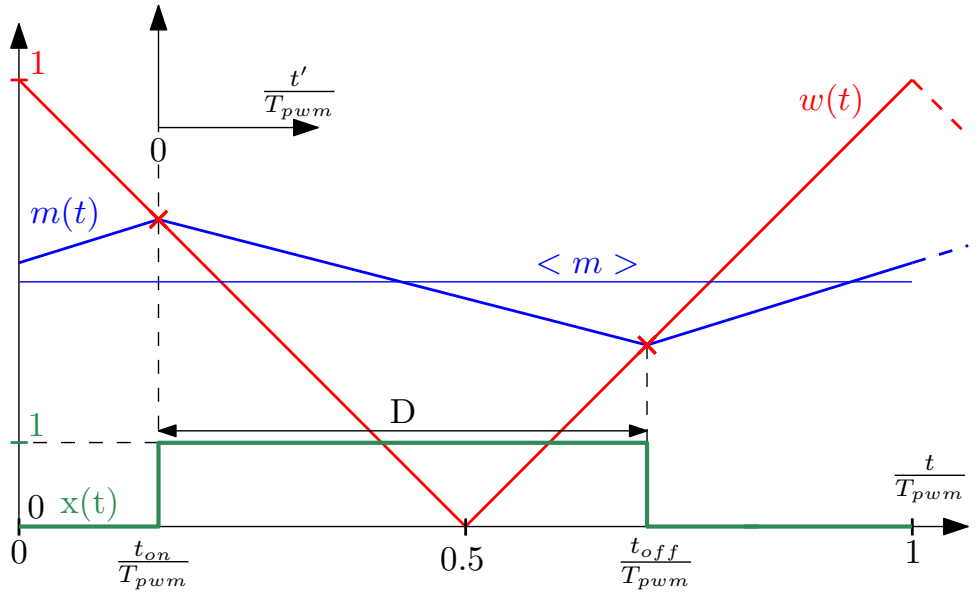


Figure 4.8: Illustration of NS-PWM waveforms, corresponding to Fig. 4.7 for $t_d = 0$.

The next step is to determine the average value of m and its position with respect to w. The triangular carrier waveform is obtained by substituting $\zeta = 0.5$ in (2.1):

$$w(t) = \begin{cases} 1 - 2\frac{t}{T_{pwm}}, & \text{if } 0 \le t \le \frac{T_{pwm}}{2} \\ 2\frac{t}{T_{pwm}} - 1, & \text{if } \frac{T_{pwm}}{2} < t < 1 \end{cases}. \tag{4.12}$$

Let us define the slope of the modulating waveform as $s_m(t) = \frac{\mathrm{d}m(t)}{\mathrm{dt}} = \frac{\mathrm{d}m^{ac}(t)}{\mathrm{dt}}$. As the switching instants are determined by the intersections between two continuous functions, m and w, the following identities hold:

$$\begin{aligned} &m(t_{on}) = w(t_{on}) \\ &m(t_{on} + DT_{pwm}) = w(t_{on} + DT_{pwm}) \\ &m(t_{on} + DT_{pwm}) = m(t_{on}) + I \\ &I = \int_{t_{on}}^{t_{on}+DT_{pwm}} s_m(t)\,dt = \int_{0}^{DT_{pwm}} s_m(t')\,dt'. \end{aligned} \tag{4.13}$$

It is important to note that the integral I is completely determined without knowing the value of t_{on}. Actually, being an integral of the slope, this value is determined by $I = m^{ac}(t' = DT_{pwm}) - m^{ac}(t' = 0)$. Using (4.12) and (4.13), the turn on instant can be found as:

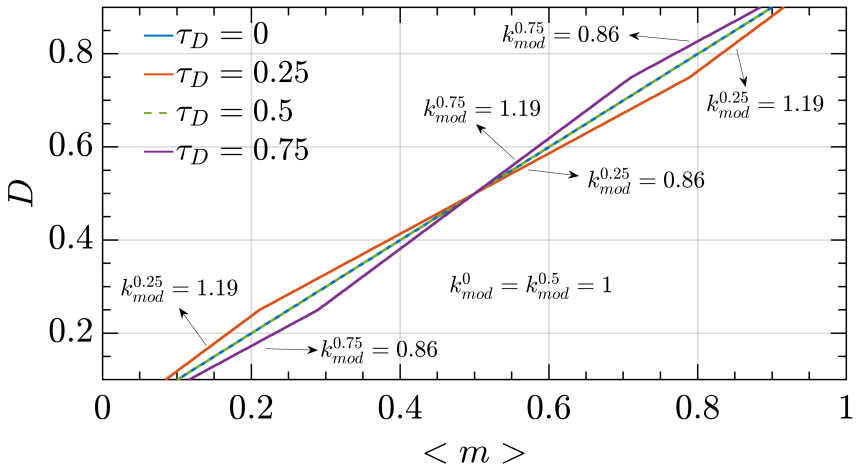
$$t_{on} = \frac{T_{pwm}}{2}\left((1 - D) + \frac{1}{2}I\right). \tag{4.14}$$

Once the value of t_{on} is calculated, the modulating waveform $m(t)$ is found as:

$$m(t) = m(t_{on}) + \int_{t_{on}}^{t_{on}+t} s_m(t)\,dt = w(t_{on}) + \int_{t_{on}}^{t_{on}+t} s_m(t)\,dt = 1 - 2\frac{t_{on}}{T_{pwm}} + \int_{t_{on}}^{t_{on}+t} s_m(t)\,dt. \quad (4.15)$$

From (4.15), the average value $< m >$, for the initially set value of D, may be found. This pair determines one point of the modulator transcharacteristic. The complete transcharacteristic is obtained by repeating the procedure above for all $D \in [0, 1]$. For the leading- and trailing-edge carriers, the only change that needs to be made is to replace the carrier parameter ζ in (2.1).

As an illustration of the *ripple modulation* in NS-PWM, Fig. 4.9 shows the transcharacteristics obtained using the procedure above, for several values of τ_D. The calculations were performed for the current controlled buck converter, as in Fig. 4.7a, with the proportional gain determined as $k_p = 2\pi f_c \frac{L}{V_{in}}$ to set the crossover frequency to $f_c = 0.1 f_{pwm}$. As explained in Section 4.2.2, for the proportional current control, the exact hardware parameters do not change the modulating waveform properties as long as the analysis is performed with respect to the relative crossover frequency. An interesting thing to note in Fig. 4.9 is that, for the analyzed modulation with the triangular carrier and the triangular switching ripple, for both $\tau_D = 0$ and $\tau_D = 0.5$, the modulator's gain is constant and equal to 1, like for the case of m without ripple.



The analysis and illustrations in this section were given for NS-PWM. For MS-PWM with high values of N, the sampled feedback becomes very close to the analog waveform. Hence, similar effects of the *ripple modulation* are expected [31, 32], which is validated in Section 4.5.4.1.

Note also that the above-described procedure for calculating m allows to determine the maximal bandwidth that satisfies the condition for smooth modulation, described in Section 2.3.2.

4.5 MS-PWM nonlinearities caused by modulating waveform discontinuities

This section discusses the modulator nonlinearities specific to MS-PWM control. Depending on the types of intersections between the modulating waveform and the carrier, the nonlinearities are manifested as reduced-gain, zero-gain, and infinite-gain zones in the static modulator transcharacteristic. The nonlinear behavior is caused by the modulating waveform jump discontinuities, whose pattern depends on the switching ripple, the controller gains, the multisampling factor, and the high-frequency response of the control system. Provisions for minimizing these nonlinearities are presented and a few application examples of converters operating in each of the nonlinear zones are given. For converters with a dc operating point, the nonlinearities can lead to an undesirable response to transients and to an increased jitter of the duty cycle. For converters with an ac operating point, the nonlinearities can also lead to the output waveform distortion.

This section begins by classifying the types on intersections between m and w and explaining their general impact on a converter's operation. This part is completely independent of the converter's topology or the control system's architecture. Subsequently, the quantitative analysis is performed for two-level, current-controlled, half-bridge and full-bridge buck converters. As mentioned at the beginning of this chapter, the same methodology can be applied to other converter topologies or feedback variables.

4.5.1 Multi-sampled control loop settings

The control system that will be referred to in this section corresponds to the one of Fig. 4.1. The triangular carrier is used and the modulating waveform update instants are equal to those in (2.2).

In general, with multiple update instants throughout the switching period, more than 2 intersections between m and w may occur. To prevent an increased number of transistor commutations, the switching action is determined based on the first intersection between m and w, for each slope of the carrier. This is equivalent to allowing the turn on only during the negative slope of the carrier, and the turn off only during the positive one. Multiple intersections can be caused by a transient or, in the steady-state, by the switching ripple, as is explained in the following sections. It should be mentioned that, for large-signal disturbances, it may be favorable to allow multiple switching actions, which would result in a faster nonlinear response and a variable switching frequency during transients [91, 118, 119].

Operation of the MS-PWM modulator for $N = 4$, with the chosen update instants and the logic that prevents multiple switching actions is illustrated in Fig. 4.10.

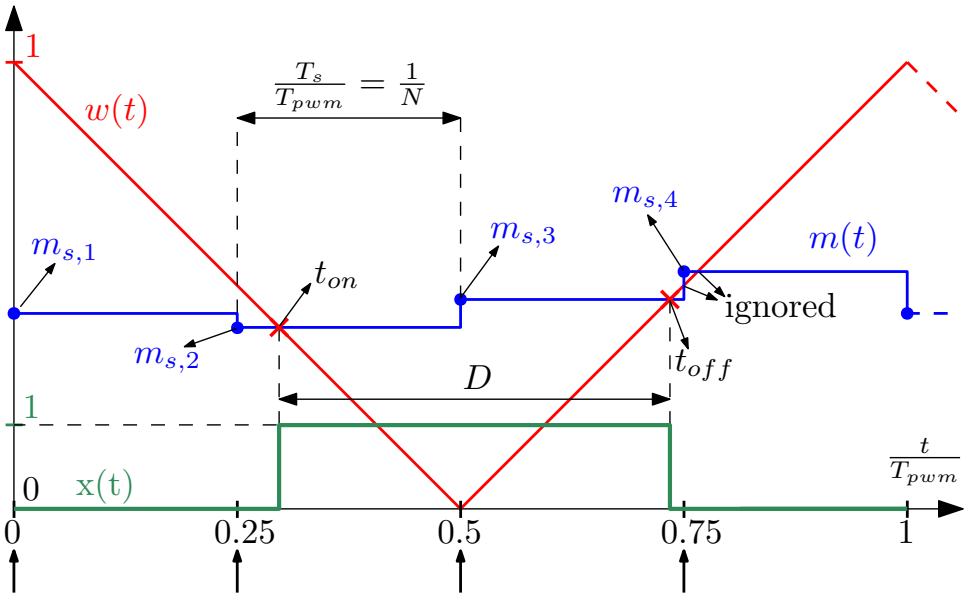


Figure 4.10: Illustration of the modulating waveform $m(t)$, the carrier $w(t)$, and the switching signal $x(t)$ for one switching period of MS-PWM with $N = 4$. The chosen update instants are illustrated as arrows. The illustration also shows that multiple switching is avoided by allowing only the turn-off to occur during the positive slope of the carrier.

4.5.2 Types of intersections between the modulating waveform and the carrier

An important difference between MS-PWM, NS-PWM, and (S/D)S-PWM[2] is that, for MS-PWM, an update of m can cause a vertical crossing with w, i.e. a switching action may occur when $m \neq w$. For NS-PWM, even if m is not constant over T_{pwm}, it is a continuous function; hence, it is always true that $m = w$ at a given switching instant. For MS-PWM, the discontinuous nature of m gives rise to various types of intersections with w, each of which brings a unique impact on the modulator transcharacteristic and, hence, k_{mod} [27, 66]. The modulator transcharacteristic can be defined in the same way as for NS-PWM. The average value of the modulating waveform over one switching period, $< \mathrm{m} >$, is found as the average of N controller outputs m_s starting from when $w = 1$, i.e. in the range $\frac{t}{T_{pwm}} \in [0, 1)$. In Fig. 4.10, this corresponds to $< \mathrm{m} > = \frac{m_{s,1}+m_{s,2}+m_{s,3}+m_{s,4}}{4}$. It will be shown that an MS-PWM transcharacteristic generally features distinct zones with specific gains, which are referred to as the nonlinearity zones. All types of intersections between m and w are shown in Fig. 4.11 and the corresponding nonlinearity zones are illustrated in Fig. 4.12.

For (S/D)S-PWM, the update of m occurs when w is equal to 0 or 1. This always yields horizontal crossings between m and w and, as explained in Section 4.4.1, results in the unity modulator's gain $k_{mod} = 1$.

For MS-PWM, an intersection between m and w can be either horizontal or vertical. In Fig. 4.11a, horizontal crossings are shown. For cases when horizontal crossings occur for both slopes of w, the

[2] With update instants that coincide with peaks and valleys of the carrier.

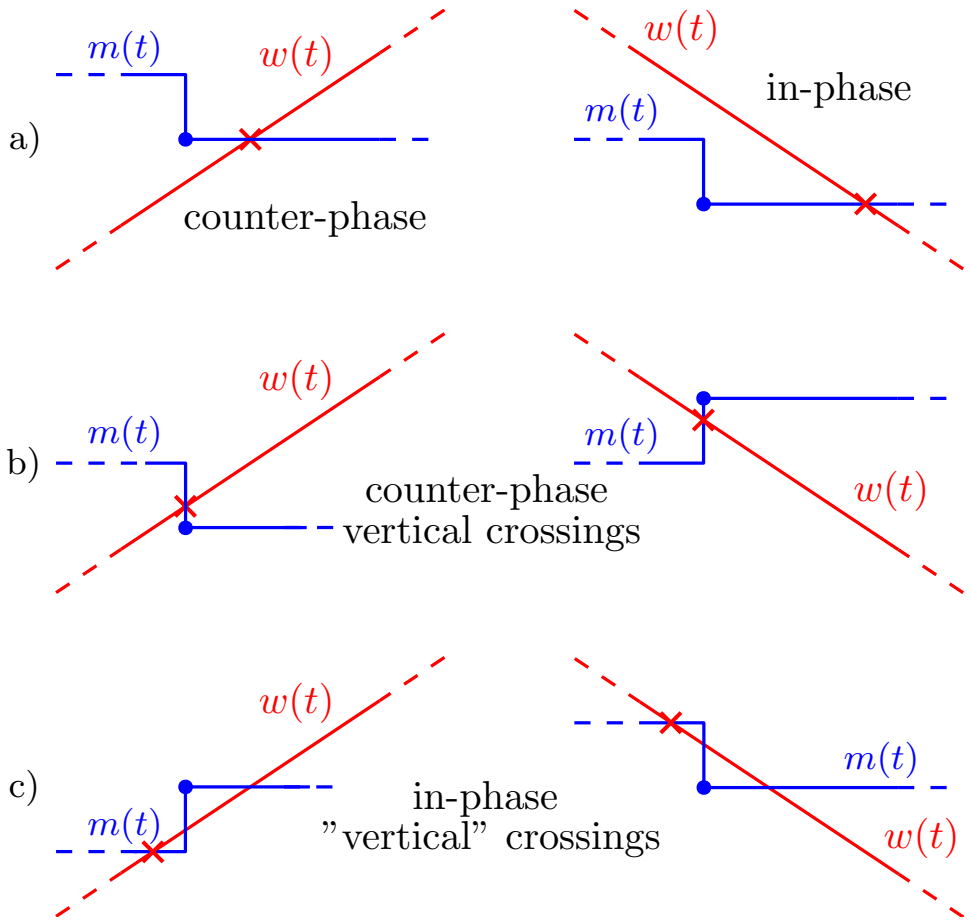


Figure 4.11: Types of intersections between the modulating waveform m and the carrier w: (a) horizontal crossings; (b) counter-phase vertical crossings; (c) in-phase "vertical" crossings. The closest update of m to the intersection with w is labeled with a blue dot. The intersection that defines the switching signal x is labeled with a red cross.

modulator's gain is $k_{mod} \approx 1$. As for the NS-PWM modulators, the gain is not exactly equal to 1, due to the ripple modulation[3] described in Section 4.4. The operation with double horizontal crossings will be referred to as the linear operation of the modulator, as the duty cycle is determined by a unique modulating waveform and both edges of x are equally modulated by applying a small perturbation d < m >. In Figs. 4.11b and 4.11c, vertical intersections are shown. It is clear from Fig. 4.10 that vertical intersections between m and w may only occur at instants when the modulating waveform is updated and the carrier is not equal to 0 or 1.

4.5.2.1 Critical duty cycles and critical modulating segments

For the triangular carrier parametrized in (4.12) and the sampling instants chosen as in (2.2), the vertical intersections may occur only when the normalized value of w is equal to $\frac{2i}{N}$, where $1 \leq i < \frac{N}{2}$ and i is an integer. Assuming that both switching instants occur for a similar value of w, the duty cycle in the

[3] In Section 4.5.4.1, it will be shown that for high values of N, the impact of the ripple modulation on k_{mod} is practically the same as for NS-PWM. For low values of N, the ripple modulation is not easily distinguished from the discontinuity-related effects, described in this section, which also impact the modulator's gain.

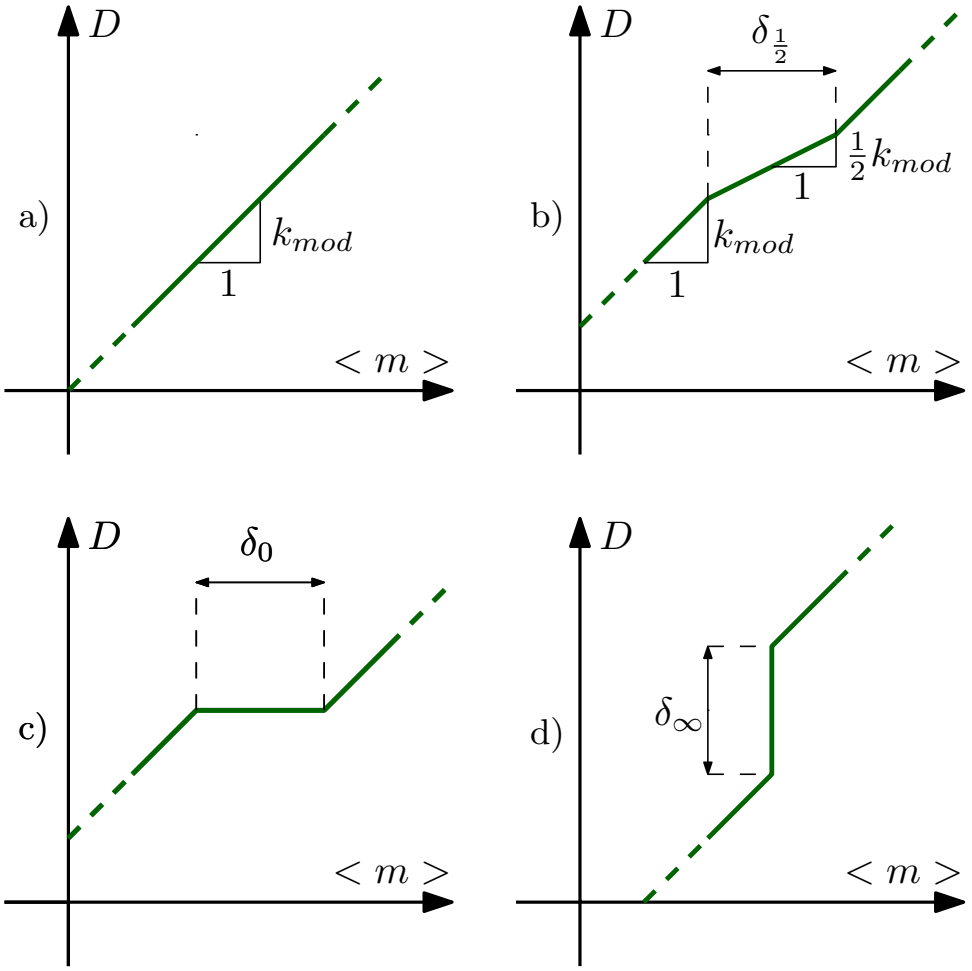


Figure 4.12: Types of zones that may appear in MS-PWM transcharacteristics: (a) linear zone corresponding to double horizontal crossings; (b) reduced-gain zone corresponding to a single counter-phase vertical crossing; (c) zero-gain (dead-band) zone corresponding to double counter-phase vertical crossings; (d) infinite-gain (jitter) zone corresponding to the in-phase "vertical" crossings. Extensions of the nonlinearity zones are labeled with δ.

presence of vertical crossings is close to the value of $\frac{2i}{N}$. This precise operating point, labeled as D_c, is defined as the *critical duty cycle*. It will be shown that the nonlinearity zones in the transcharacteristics are located around these values of D. For a given N, the *critical duty cycles* are found as:

$$D_c = \frac{2i}{N} \quad , \quad 1 \leq i < \frac{N}{2}, \tag{4.16}$$

Note that the exact operating points, for which the vertical intersections may occur, span a certain range around D_c.

The *critical modulating segments* are the two adjacent segments of m before and after the update instant closest to the intersection between w and m, i.e. those shown in Fig. 4.11. For each operating point, there are two pairs of critical modulating segments, one for the positive and one for the negative slope of the carrier.

Finally, let us define the *discontinuities* of the critical modulating segments for both positive ($\Delta m_{c,u}$)

and negative ($\Delta m_{c,d}$) slopes of w as:

$$\begin{aligned}\Delta m_{c,u} &= m(T_{c,u}+\epsilon) - m(T_{c,u}-\epsilon)\\ \Delta m_{c,d} &= m(T_{c,d}-\epsilon) - m(T_{c,d}+\epsilon)\end{aligned} \tag{4.17}$$

where ϵ is an infinitely small positive number and $T_{c,u}$ and $T_{c,d}$ are the modulating waveform update instants closest to the intersection with the carrier.

For further classification, let us again recall the *in-phase* and *counter-phase* operating regimes. The in-phase operating regimes occur when the difference between values of the *critical modulating segments* has the same sign as the slope of w. The counter-phase operating regimes occur when the difference between values of the *critical modulating segments* has the opposite sign compared to the slope of w. It will be shown that, regarding vertical crossings, different behavior is obtained for the counter-phase and the in-phase regimes. Note that, the signs in (4.17) are chosen so that a positive value of $\Delta m_{c,u,d}$ always corresponds to the in-phase condition.

An illustration of the critical modulating segments and their discontinuities is shown in Fig. 4.13.

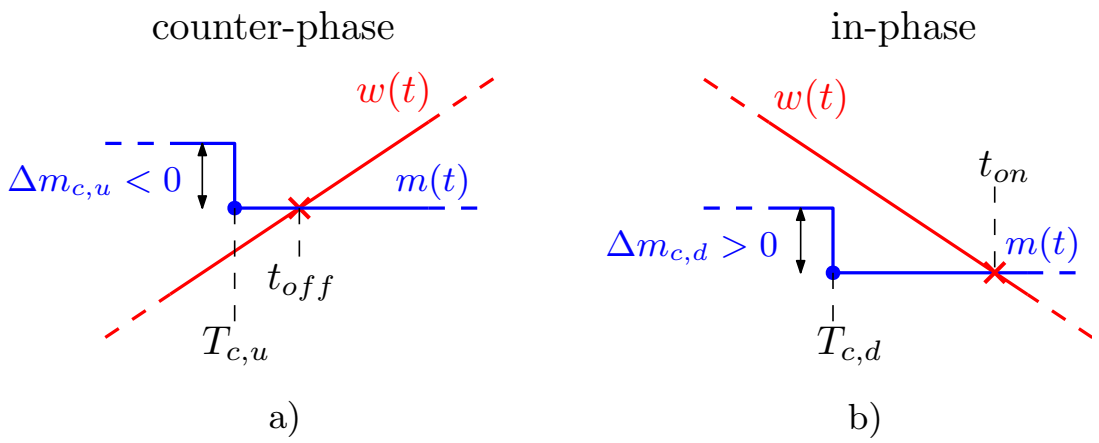


Figure 4.13: Illustration of the critical modulating segments and their discontinuities for (a) counter-phase and (b) in-phase operation. The modulating waveform update instants closest to the intersection with the carrier are labeled as $T_{c,u}$ for the positive slope of w and $T_{c,d}$ for the negative slope of w. The turn-on and turn-off instants are labeled with t_{on} and t_{off}, respectively.

4.5.2.2 Counter-phase vertical crossings

In Fig. 4.14, the counter-phase vertical crossings are shown. A counter-phase vertical crossing prevents the modulation of the corresponding edge of $x(t)$, which reduces the modulator's gain [27].

The operation with a single counter-phase vertical crossing is shown in Fig. 4.14a. Let us assume that the steady-state operation is determined by $m(t)$ drawn using the dark blue color. By applying a perturbation d < m >, the modulator's gain determines the response $\mathrm{dD} = \mathrm{dD_u} + \mathrm{dD_d}$. For the analyzed case, the rising edge of x is not modulated at all ($\mathrm{dD_d} = 0$). Hence, neglecting the ripple modulation, the modulator's gain is effectively halved, i.e. $k_{mod} \approx \frac{1}{2}$. The corresponding nonlinearity zone in the modulator transcharacteristic, referred to as the reduced-gain zone, is illustrated in Fig. 4.12b.

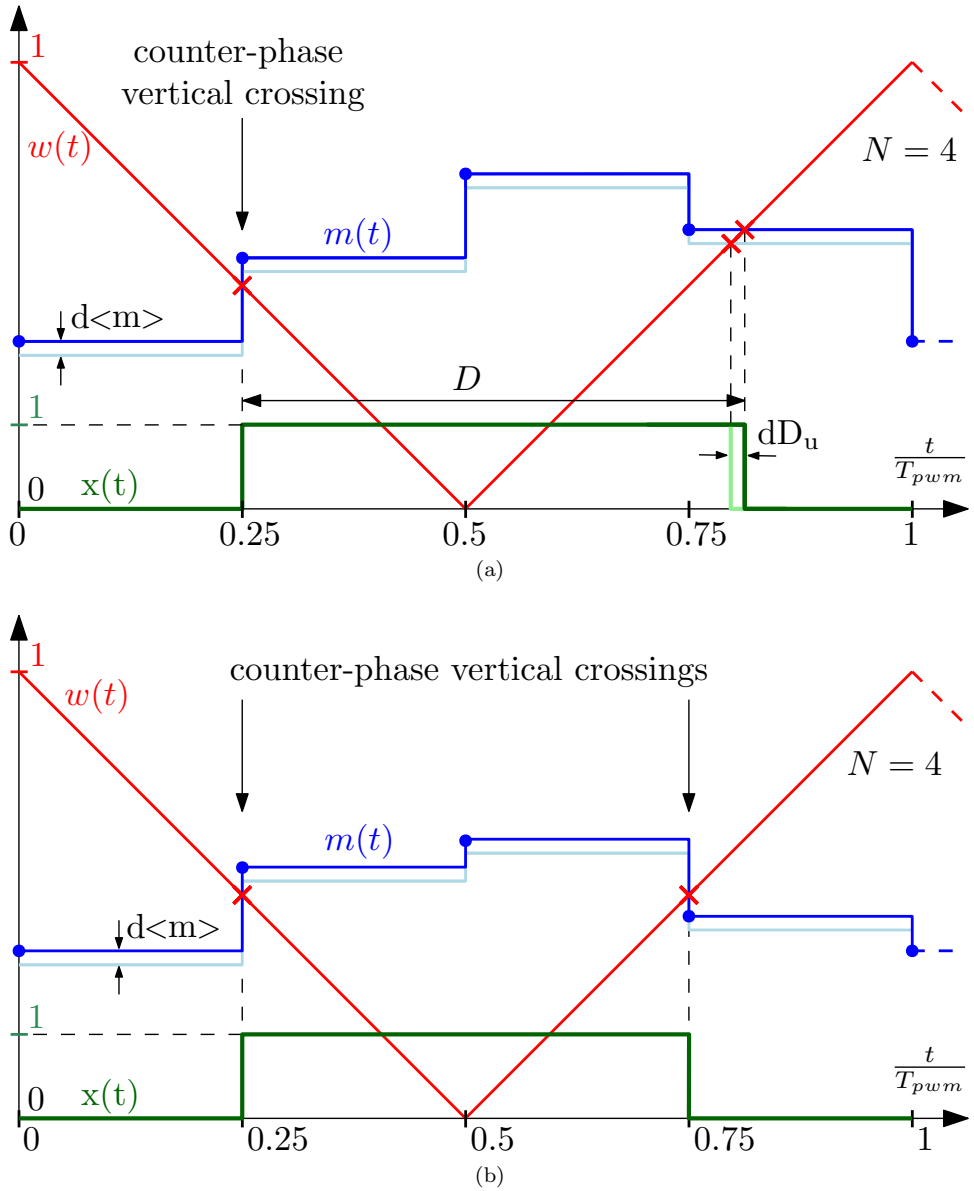


Figure 4.14: Illustration of MS-PWM operation with $N = 4$ and (a) single and (b) double counter phase vertical crossing. For a small change d < m >, the edge of x determined by a vertical crossing is not being modulated.

Now let us consider the case shown in Fig. 4.14b. There, both edges of x are locked due to double vertical crossings and the perturbation of m does not at all affect the applied D. In this case, the converter practically works in open-loop conditions, with $D = D_c$, and the control system is ineffective, i.e. $k_{mod} = 0$. The corresponding nonlinearity zone in the modulator transcharacteristic, referred to as the dead-band or the zero-gain zone, is illustrated in Fig. 4.12c.

The impact of the reduced- and, especially, the zero-gain zones on a response to small- or large-signal disturbances is very difficult to analyze in a general form and a case-by-case study is needed. For dc-dc converters, several examples of deteriorated transient responses are given in [24, 27]. In Section 4.5.6.2, it will be shown that, for converters with an ac operating point, these nonlinearity zones result in the

output distortion.

It should be noted that, for the MS-PWM implementation in certain DSP platforms, an additional logic must be implemented to prevent the *pulse-skipping* phenomenon [18, 72]. Namely, if the PWM output is toggled only when $m = w$, it is necessary to predict a vertical crossing and force the switching action to occur. In case FPGAs are used, the *pulse-skipping* is easily prevented by using the logic comparison $m \geq w$.

4.5.2.3 In-phase "vertical" crossings

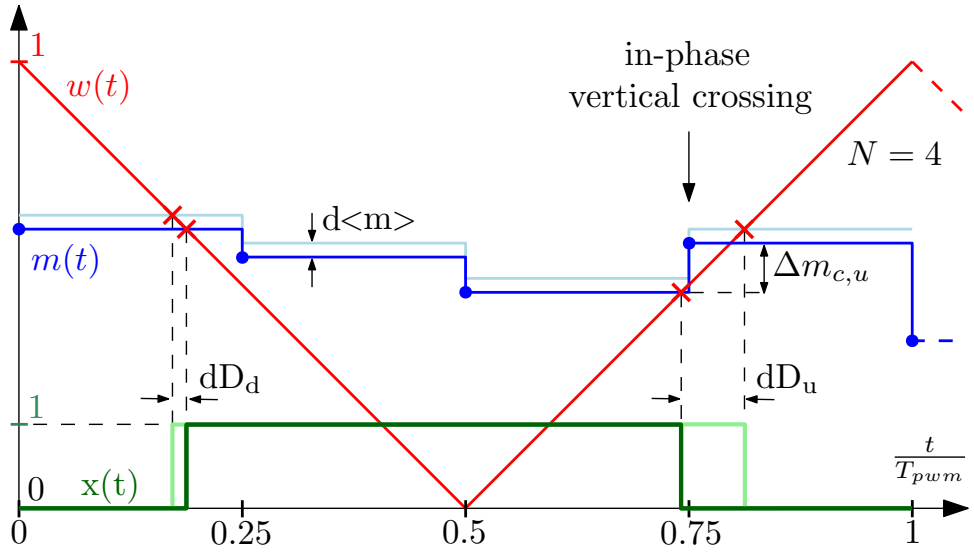


Figure 4.15: Illustration of MS-PWM operation with $N = 4$ and a single in-phase "vertical" crossing. For a small change d < m >, the response of the falling edge of x is determined by the corresponding critical modulating segment discontinuity $\Delta m_{c,u}$.

Consider the case shown in Fig. 4.15, where the in-phase "vertical" crossing occurs just after the falling edge of x. With the logic that prevents multiple commutations, the in-phase "vertical" crossings are actually turned into horizontal crossings; however, this operation brings another nonlinear phenomenon. Namely, for the illustrated case, by applying a small positive perturbation d < m >, the falling edge of x is no longer triggered by the same modulating segment, but by the following one. Hence, the resulting response $\mathrm{dD_u}$ is not dominantly affected by the value of d < m > but by the critical modulating segment discontinuity $\Delta m_{c,u}$, which can result in a large gain of the modulator. The in-phase "vertical" crossings can appear for both slopes of w, or in combination with a horizontal or a counter-phase vertical crossing.

In the following section it will be shown that, due to the discontinuity of the modulating waveform, the in-phase operation yields a whole range of duty cycles for which a steady-state operation cannot be found. For those duty cycles, the transcharacteristic cannot be defined; however, to indicate its impact, the corresponding nonlinearity zone will be represented by a vertical line, i.e. $k_{mod} \to \infty$, as illustrated in Fig. 4.12d. These nonlinearity zones will be referred to as the infinite-gain or jitter zones, because

they result in LCOs.

4.5.3 Duty cycle jittering caused by the in-phase "vertical" crossings

Discovery and analysis of the effects caused by the in-phase "vertical" crossings are amongst the original contributions of this thesis. Therefore, this entire section is devoted to the analysis of this specific discontinuity-related nonlinearity.

4.5.3.1 Explanation of the jittering mechanism

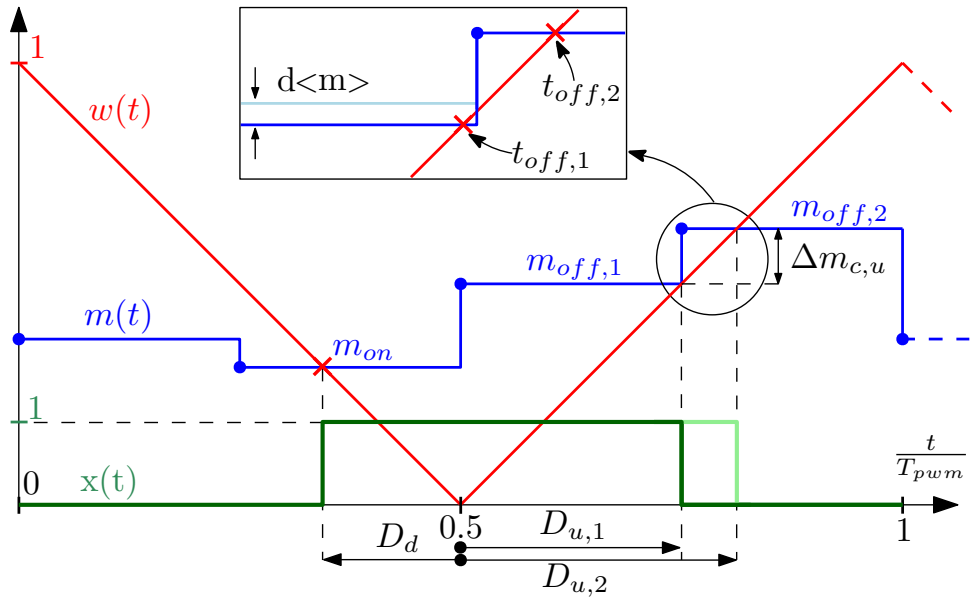


Figure 4.16: Example of an operating condition that may result in the jitter amplification, for MS-PWM with $N = 4$.

The jitter amplification phenomenon, described in this section, is a result of the in-phase discontinuity of m. The mechanism behind it is illustrated in Fig. 4.16, for $N = 4$.

Consider an initial operating point, shown in Fig. 4.16, where the falling edge of x is triggered by the intersection between w and the modulating segment $m_{off,1}$. This determines the duty cycle $D_1 = D_d + D_{u,1}$. In case the closed-loop control results in a small change of the controller's output, such that a higher duty cycle is required (a value between $D_d + D_{u,1}$ and $D_d + D_{u,2}$), the modulating waveform is incremented by a certain amount d < m >. As illustrated in Fig. 4.16, a very small positive change of the segment $m_{off,1}$ causes the intersection between m and w to be determined by the following segment $m_{off,2}$, which changes the up-count partial duty cycle from $D_{u,1}$ to $D_{u,2}$. Since the applied duty cycle is higher than the required one, the controller will react by decreasing the value of m, which may cause the segment $m_{off,1}$ again to intersect with w in the following switching period. This causes limit cycling (duty cycle jittering) by an extent that is determined by the discontinuity of these critical modulating segments: $x = f(\Delta m_{c,u}, t)$. As it will be shown in the following sections, the critical modulating segments can exhibit a large discontinuity, resulting in a very high modulator's gain under this condition.

Let us here assert that, around each D_c, the in-phase discontinuity of the critical modulating segments determines the height of the jitter zone δ_∞ in an MS-PWM transcharacteristic (see Fig. 4.12d.). Without a formal proof, this relation comes from that fact that, for a fixed switching ripple, this discontinuity defines a range of duty cycles that cannot be achieved in steady-state. Referring to Fig. 4.16, this range is equal to $D_{u,2} - D_{u,1} = \frac{\Delta m_{c,u}}{2}$. In an MS-PWM transcharacteristic, this corresponds to the respective jitter zone height being equal to $\delta_\infty = \frac{\Delta m_{c,u}}{2}$. For the case when the in-phase regime is present for both slopes of the carrier, the accumulated height[4] of the jitter zones, around the observed D_c, can be estimated as:

$$\Delta D_\infty = \delta_{\infty,u} + \delta_{\infty,d} = \frac{\Delta m_{c,u}^{in-p}}{2} + \frac{\Delta m_{c,d}^{in-p}}{2}, \tag{4.18}$$

where Δm_c^{in-p} labels the in-phase discontinuity. As noted before, the in-phase operation does not always occur simultaneously for both slopes of w, in which case only one Δm_c^{in-p} in (4.18) is present.

4.5.3.2 Statistical approach for the jitter modeling

To gain a quantitative insight into the effects that jittering imposes on a converter's output, a simple statistical approach is proposed. The principle behind the described effect is that a small change of the modulating segment can lead to a large change of the switching pulse width. In Fig. 4.16, the mechanism is shown for the jittering of the falling edge of the switching impulse, but it can equally appear for the rising edge or for both the edges.

Consider again the operating condition shown in Fig. 4.16. Assuming that the rising edge of the switching impulse is fixed (the corresponding value of the modulating segment is equal to m_{on}), the applied duty cycle depends on the value of the critical modulating segment that first intersects with the carrier during the positive slope of w. The relevant critical modulating segments are $m_{off,1}$ and $m_{off,2}$, which correspond to the duty cycles equal to $D_1 = D_d + D_{u,1}$ and $D_2 = D_d + D_{u,2}$, respectively. Assuming that the controller tries to impose a duty cycle value exactly in between D_1 and D_2, it can be supposed that there is an equal probability that the switching will occur at $t_{off,1}$, resulting in D_1, or at $t_{off,2}$, resulting in D_2. In other words, dithering will occur between the boundary values D_1 and D_2. Hence, the expected value [120] of the applied duty cycle μ_D is equal to:

$$\mu_D = \frac{1}{2}(D_1 + D_2) = \frac{1}{2}\left(m_{on} + \frac{m_{off,1} + m_{off,2}}{2}\right) \tag{4.19}$$

The variance [120] of the applied duty cycle σ_D^2 is calculated as:

$$\sigma_D^2 = \frac{1}{2}\left((D_1 - \mu_D)^2 + (D_2 - \mu_D)^2\right) = \frac{\Delta m_{c,u}^2}{16} = \frac{\delta_{\infty,u}^2}{4} \tag{4.20}$$

where $\Delta m_{c,u} = m_{off,2} - m_{off,1}$. In case the jittering occurs simultaneously for both slopes of w, the

[4] As it will be shown, if the in-phase operation is present for both slopes of w, the resulting transcharacteristic will feature two jitter zones around the corresponding D_c that are either separated or merged together, depending on the size of the discontinuity of m.

value of δ_∞ should be replaced by ΔD_∞ from (4.18). Equation (4.20) shows that the variance of the duty cycle changes as a quadratic function of the discontinuity of the critical modulating segments. Therefore, any reduction of this discontinuity is expected to strongly reduce the negative effects on a converter's output. Note that the actual expected value μ_D in (4.20) depends on the duty cycle imposed by the controller, which can be anywhere between the boundary values D_1 and D_2. A merit of this simplified variance expression is that it provides an intuitive quantification of the jittering impact based only on Δm_c, and not on the exact operating point.

4.5.3.3 Algorithm for jittering prevention

This section proposes an algorithm that can be used for cancelling the duty cycle jittering. The algorithm is intended for use under dc or slowly-varying operating points; however it is designed such as not to impair a response to large-signal transients. The flowchart of the algorithm is shown in Fig. 4.17.

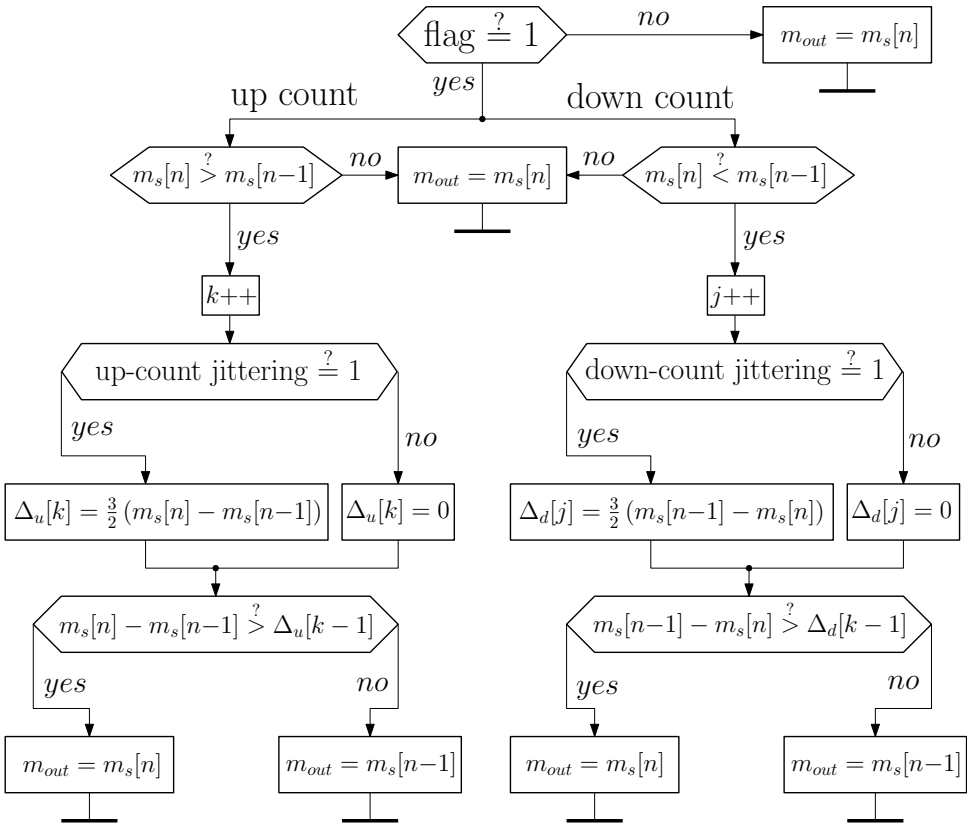


Figure 4.17: Flowchart of the algorithm proposed for cancelling the duty cycle jittering. At the sampling instant $[n]$, in case the jittering is detected and a large-signal transient is not present, the controller's output $m_s[n]$ is discarded and the previous value is used instead.

The idea behind the proposed method is to block the update of the second segment in a pair of critical modulating segments, in case the jittering is detected. The algorithm first detects whether the switching action is occurring near the modulating waveform update, by comparing the value of the modulating segment with the value of the carrier at the following update instant. If the absolute value of the time

difference between the switching action and the modulating waveform update is below a chosen value Δt^{flag}, referred to as the *flag* zone time-span, the *flag* is raised. If the absolute value is above Δt^{flag}, the *flag* is cleared and the modulating waveform update is always allowed. When the *flag* is raised, if the detected operation is counter-phase, the modulating waveform update is always allowed. If the in-phase operation is detected, in order to start blocking the update, additional indicators are used. In Fig. 4.17, they are labelled as *up-count jittering* and *down-count jittering*, for both slopes of the carrier. These indicators prevent blocking the modulating waveform update in case the *flag* is raised, but the jittering has not yet occurred. These indicators are set when, for the first time since the *flag* is raised, for the respective carrier slope, the switching action moves from one critical modulating segment to the other.

By preventing the modulating waveform update the discontinuity effect is cancelled, however, care must be taken regarding large-signal disturbances. Namely, regardless of the position relative to the carrier, the modulating waveform should always be updated if a large disturbance is detected. This prevents delays when reacting to faults or reference changes. For this reason, adaptive limits for critical modulating segment differences are used to decide whether to update or not. In Fig. 4.17, the limit is labelled as Δ_u for the up-count and Δ_d for the down-count jittering. There are two distinct limits, as the jittering can occur for both slopes of the carrier, independently. These limits are adapted using the previous value of Δm_c, which the algorithm tracks, imposing a 50% higher margin, heuristically. This margin should be sized to ensure that the control system is robust to noise present in the experimental set-up. On the other hand, over-sizing the margin deteriorates the capability of the algorithm to respond to large-signal disturbances. Each time the counter-phase operation is detected, or the *flag* is cleared, the adaptive limits are reset to 0. This allows the first in-phase change of the critical modulating segment pair to be always updated, which is required to set the limit based on the current operating point. After the limit is set, if a large-signal disturbance occurs, for which the difference between the critical segments is higher than the set limit, the modulating waveform update is allowed. Cases when the adaptive limit is set by the large-signal disturbance do not cause problems for the algorithm, as the operating point significantly changes, which causes the *flag* to be cleared and the limit to be reset to 0. Note that the magnitude of a large-signal disturbance that clears the *flag* is correlated to the choice of the *flag* zone time-span Δt^{flag}, which is why that value should also be sized carefully.

An initial guess for Δt^{flag}, below which the *flag* is raised, can be made using the modulating waveform discontinuities[5]. Consider again the operating point shown in Fig. 4.16; the *flag* zone time-span can be chosen as $\Delta t^{flag} = t_{off,2} - t_{off,1}$. This results in $\Delta t^{flag} \approx \frac{1}{2}\Delta m_{c,u} T_{pwm}$, considering that $t_{off,1}$ is close to the relevant update instant. Such design choice is made for the subsequent results in this thesis.

To summarize, in order for the algorithm to start preventing the update, at least 3 switching periods with the *flag* raised are needed. The first one is needed to set the *flag* if the switching action is occurring near the modulating waveform update. The second period is required for the jittering to occur for the first time. During the second period, the adaptive limit is calculated. It becomes active in the next,

[5]The discontinuities can be calculated off-line based on the control system parameters. The procedure for their calculation is analyzed in Section 4.5.4.

third, period when the jittering prevention starts.

4.5.3.4 Approximate in-phase conditions for current control loops with one step delay and low-pass feedback filters

For reasons described in Section 4.4.1, for inner current control loops the counter-phase operation is enabled by default. Consider again the system shown in Fig 4.1 (as noted in Section 4.2.2, the same analysis is valid for the full-bridge configuration). Blocks that may impact the shape of m, and hence also its intersection with w, are the feedback filters and the controller. This section offers a simplified analysis of how this cascade may change the operation from the counter-phase to the in-phase.

It is mentioned in Section 4.4.1 that, for current control with NS-PWM, the time delay may change the operation from the counter-phase to the in-phase. For this reason, it is expected that a similar impact on m may be brought by low-pass filters, due to the introduced phase lag at high frequencies. Therefore, the analysis is performed for the control system with a first-order low-pass filter in the feedback. The discretization is, arbitrarily, performed using the bilinear transform:

$$G_{fb}(z) = \frac{a_f}{a_f+2}\frac{z+1}{z+\frac{a_f-2}{a_f+2}} \quad , \quad a_f = \omega_{c,f}T_s, \tag{4.21}$$

where $\omega_{c,f}$ is the filter's angular cut-off frequency. Regarding the controller, the analysis is performed for the discretized version of the PI structure from (4.3), with the added one step computation delay:

$$G_c(z) = \left(k_p + k_i T_s \frac{1}{1-z^{-1}}\right) z^{-1}. \tag{4.22}$$

The in-phase conditions are derived for $N = \{4, 6, 8\}$, by calculating the discontinuity of the critical modulating segments. Consider the illustration shown in Fig. 4.18. For $N = 4$, there is only one critical segment pair per slope of w, i.e. $\Delta m_{c,u}^{1,2} = m_{4,2} - m_{4,1}$, where 4 indexes the oversampling factor. This critical segment pair may cause vertical crossings for operating points near $D_c = \frac{1}{2}$. For $N = 6$, it is of interest to observe $\Delta m_{c,u}^{1,2} = m_{6,2} - m_{6,1}$ for operating points near $D_c = \frac{1}{3}$ and $\Delta m_{c,u}^{2,3} = m_{6,3} - m_{6,2}$ for operating points near $D_c = \frac{2}{3}$. For $N = 8$, it is of interest to observe $\Delta m_{c,u}^{1,2} = m_{8,2} - m_{8,1}$ for operating points near $D_c = \frac{1}{4}$, $\Delta m_{c,u}^{2,3} = m_{8,3} - m_{8,2}$ for operating points near $D_c = \frac{1}{2}$, and $\Delta m_{c,u}^{3,4} = m_{8,4} - m_{8,3}$ for operating points near $D_c = \frac{3}{4}$.

As seen from (4.7), for buck-type converters the switching ripple is anti-symmetric around $D = 0.5$. For this reason, the properties derived for the positive slope of the triangular carrier w, for a certain value of D, are the same as those for the negative slope of w, for $1 - D$. Hence, all derivations are given only for the positive slope of w. An illustration of this anti-symmetry is shown in Fig. 4.19 for simulated modulating waveforms of the current-controlled system from Fig. 4.1, obtained for $D = 0.67$ and $D = 0.33$. It is clear that the discontinuities of $m^{0.33}$ and $m^{0.67}$, calculated using the sign convention from (4.17), are the same for opposite slopes of w, i.e. $m_{6,4}^{0.67} - m_{6,5}^{0.67} = m_{6,2}^{0.33} - m_{6,1}^{0.33}$ and $m_{6,5}^{0.33} - m_{6,6}^{0.33} = m_{6,3}^{0.67} - m_{6,2}^{0.67}$.

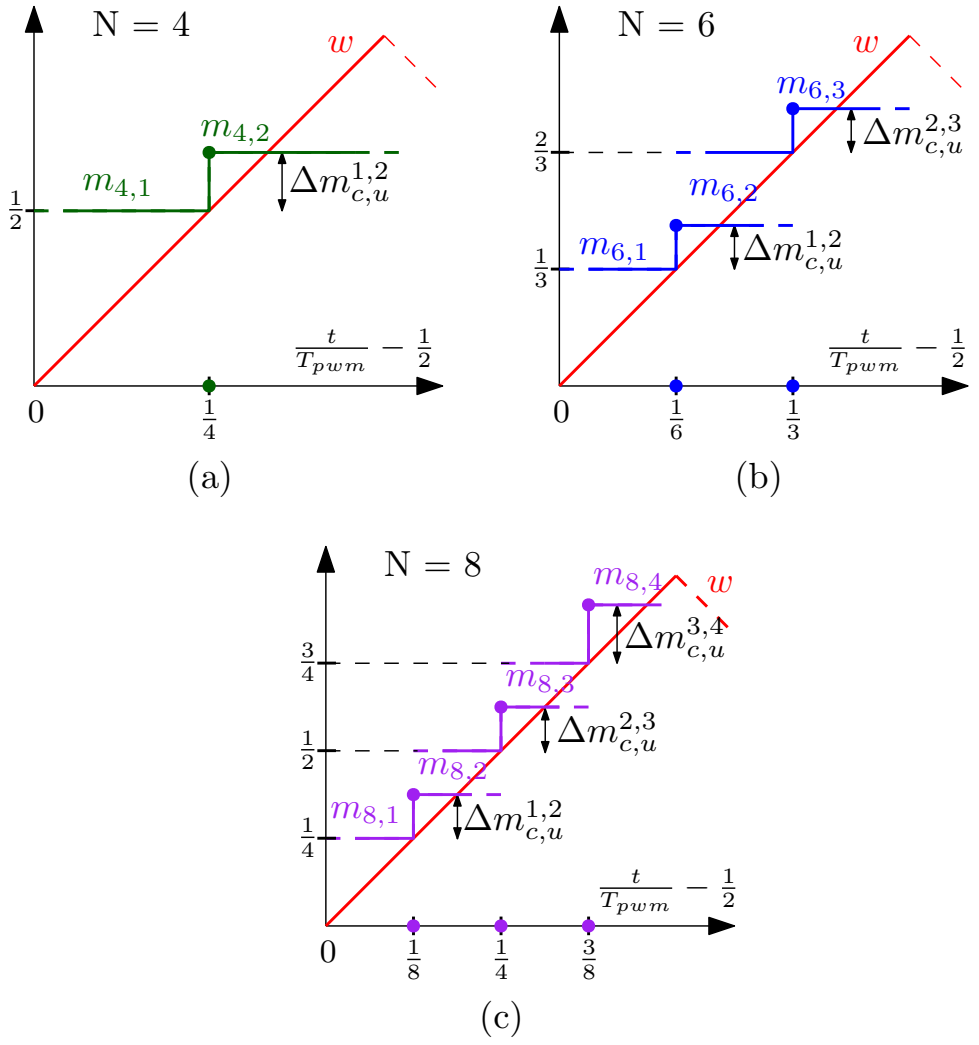


Figure 4.18: Illustration of the critical modulating segments for the positive slope of w and: (a) $N = 4$ around $D_c = \frac{1}{2}$, (b) $N = 6$ around $D_c = \frac{1}{3}$ and $D_c = \frac{2}{3}$, (c) $N = 8$ around $D_c = \frac{1}{4}$, $D_c = \frac{1}{2}$, and $D_c = \frac{3}{4}$.

For the simplified analysis in this section, the following assumptions and approximations are made. First, as before, it is assumed that the output voltage dynamics are slow, i.e. v_o in Fig. 4.1 is constant. Secondly, the converter is assumed to work with the zero reference tracking error, at the operating point equal to the analyzed critical duty cycle, i.e. $D = D_c$. Additionally, it is assumed that inside one T_{pwm}, both intersections between m and w occur exactly for $w = D_c$, i.e. $D_u = D_d = \frac{D_c}{2}$. This fixes the switching signal x to be centred around $w = 0$, which removes the necessity to re-iterate the calculation of the switching ripple component, once the actual intersections between sampled m and w are found. Referring to Fig. 4.4c and the sampling instants from (2.2), this approximation means that, at the peaks/valleys of w the average current is sampled (the controller error is 0), while for the other sampling instants the current error is equal to a fraction of the switching ripple.

With these assumptions, for the current ripple with its peak-to-peak value $\Delta i_L^{p-p} = 2\Delta I$, it is possible to directly compute the modulating waveform discontinuities, using the difference equations corresponding to G_c and G_{fb}. The resulting expressions for Δm_c are given in (4.23) - (4.27), where

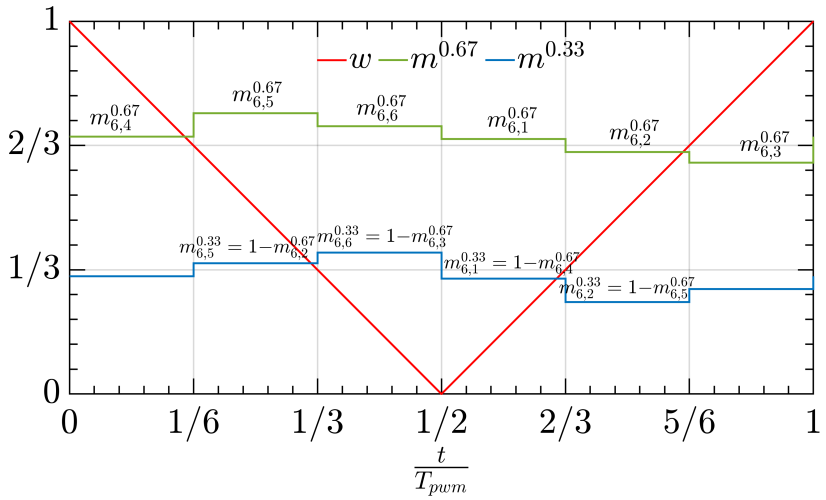


Figure 4.19: Illustration of the anti-symmetry between modulating waveforms for $D = 0.67$ and $D = 0.33$, for the proportional current control system with $N = 6$. The modulating waveforms are obtained from simulations, using the proportional controller with $k_p = 2\pi f_c \frac{L}{V_{in}}$, for $f_c = 0.1 f_{pwm}$.

$\omega_{i,rel} = \frac{\omega_i}{2\pi f_s} = \frac{\omega_i}{2\pi N f_{pwm}} = \frac{T_s}{2\pi}\frac{k_i}{k_p}$ is the relative angular frequency of the zero related to the integral action. By comparing the calculated discontinuities with zero, it is possible to find the value of the filter's cut-off frequency, for which the operation turns from the counter-phase to the in-phase. The equation is not shown for $N = 8$ and $D_c = \frac{3}{4}$, because already for $N = 8$ and $D_c = \frac{1}{2}$, the operation is always counter-phase (the first-order low-pass filter cannot provide enough phase lag to enable the in-phase operation, at least for realistic values of $\omega_{i,rel}$). The same is valid for the case of $N = 6$ and $D_c = \frac{2}{3}$ in (4.25). This indicates that, for the current control loops, the in-phase operation may occur only for the first pair of the critical modulating segments of the respective slope of w. For the positive slope of w this corresponds to the lowest value of D_c while for the negative slope it corresponds to the highest value of D_c. Note again that these expressions are given for the controller that features one step computation delay, which on its own has an impact on bringing the operation closer to the in-phase condition.

$$\Delta m_{c,u}^{1,2}\big|_{N=4,D_c=\frac{1}{2}} = \frac{k_p a_f \Delta I}{a_f^2 + 4}\left[4\pi\omega_{i,rel} - a_f + 2\right] \tag{4.23}$$

$$\Delta m_{c,u}^{1,2}\big|_{N=6,D_c=\frac{1}{3}} = \frac{k_p a_f \Delta I}{({a_f}^2 + 12)\,(3{a_f}^2 + 4)}\left[-3a_f^3 + 6a_f^2\,(2\pi\omega_{i,rel} + 1) - 28a_f + 80\pi\omega_{i,rel} + 24\right] \tag{4.24}$$

$$\Delta m_{c,u}^{2,3}\big|_{N=6,D_c=\frac{2}{3}} = \frac{k_p a_f \Delta I}{2\,({a_f}^2 + 12)\,(3{a_f}^2 + 4)}\left[-3{a_f}^3\,(2\pi\omega_{i,rel} + 1) + 6{a_f}^2\,(2\pi\omega_{i,rel} + 1)\right.$$
$$\left. - 52a_f\,(2\pi\omega_{i,rel} + 1) + 8\,(10\pi\omega_{i,rel} - 3)\right] \tag{4.25}$$

$$\Delta m_{c,u}^{1,2}\big|_{N=8,D_c=\frac{1}{4}} = \frac{k_p a_f \Delta I}{3\left({a_f}^2+4\right)\left({a_f}^4+24{a_f}^2+16\right)} \cdot \Big[-3a_f^5 + 6a_f^4\left(2\pi\omega_{i,rel}+1\right) - 72a_f^3 + 16a_f^2\left(14\pi\omega_{i,rel}+5\right) - 176a_f + 32\left(14\pi\omega_{i,rel}+3\right)\Big] \tag{4.26}$$

$$\Delta m_{c,u}^{2,3}\big|_{N=8,D_c=\frac{1}{2}} = \frac{k_p a_f \Delta I}{2\left({a_f}^4+24{a_f}^2+16\right)}\Big[-{a_f}^3\left(2\pi\omega_{i,rel}+1\right) + 2{a_f}^2\left(2\pi\omega_{i,rel}+1\right) - 28a_f\left(2\pi\omega_{i,rel}+1\right) + 8\left(6\pi\omega_{i,rel}-1\right)\Big] \tag{4.27}$$

For the illustration of the filter's impact, a case of $N = 4$ and $D_c = \frac{1}{2}$ is analyzed in more detail. The in-phase condition is satisfied if (4.23) is greater than zero, which yields the following inequality:

$$a_f < 2\left(1+2\pi\omega_{i,rel}\right) \tag{4.28}$$

For the high-frequency proportional-dominant PI controllers, the zero related to the integral action is always significantly below the switching frequency, which allows the simplification of the condition above to:

$$a_f < 2 \implies \omega_{c,f} < \frac{4}{\pi}\omega_{pwm} \tag{4.29}$$

Therefore, this approximated analysis tells that, for the analyzed four-time-sampled current control loop, if the angular cut-off frequency of the first-order feedback filter is placed below (4.29), the modulating waveform will be in-phase with the carrier and the jitter amplification may occur. From (4.28) it is evident that the increase of the integral gain results in a higher boundary value of $\omega_{c,f}$ that enables the in-phase regime. This further points to a correlation between the in-phase operation of the current control loops and the phase lag introduced from sampled i_L to m. For the other values of the multisampling factor, the derived expressions are not so simple; however, the trends related to the impact of the filter and the integral action remain the same[6].

In this section, the expressions for Δm are derived only for the single first-order digital low-pass filter $G_{fb}(z)$ in (4.21). However, based on the noticed correlation between the introduced phase lag and the in-phase condition, it is of interest to see whether these simple expressions can be also used to predict the in-phase operation for some other filters, e.g. for analog low-pass filters. For this reason, the in-phase conditions are transformed to show the dependence on the phase lag at the switching frequency, introduced by the feedback filter.

The boundary lines ($\Delta m = 0$), for the lowest values of D_c and the positive slope of w, are shown

[6]In [65], the analysis is performed for the same current control system, with a PID controller. There, it is shown that practically for any non-zero derivative gains, the in-phase operation is prevented. Again, this is consistent with the reasoning that, in current control systems, the phase lag tends to change the operation from the counter-phase to the in-phase. The PID structure is not often used for current controllers; hence, for consistency with the structures used throughout this chapter, the related expressions are not shown.

in Fig. 4.20. The calculations are performed for values of ω_i from 0 ($k_i = 0$) to 0.15 ω_{pwm}. The proportional gain is calculated as $k_p = 2\pi f_c \frac{L}{V_{in}}$, for $f_c = 0.093 f_{pwm}$. Due to the approximations used in the modulating waveform calculations, it was of interest to verify these results. Therefore, simulations were implemented in MATLAB/Simulink, for the buck converter corresponding to the set-up A, described in Table 3.1. Values of m, for different filter's cut-off frequencies, were obtained while the converter was working with a fixed reference corresponding to the duty cycle $D = D_c$. The first set of verifications was performed by implementing $G_{fb}(z)$ as in (4.21); the corresponding results are shown in Fig. 4.20 using circular markers. The second set of verifications, with the results plotted using diamond markers, was performed using an analog low-pass filter:

$$G_{fb}(s) = \frac{\omega_{c,f}}{s + \omega_{c,f}} \tag{4.30}$$

From Fig. 4.20, it can be seen that the results for analog and digital filter implementations match well with the analytical traces and are very close to each other. These results confirm that the presented simplified expressions are well-suited to predict the in-phase operation independently of the specific converter parameters or filter configurations.

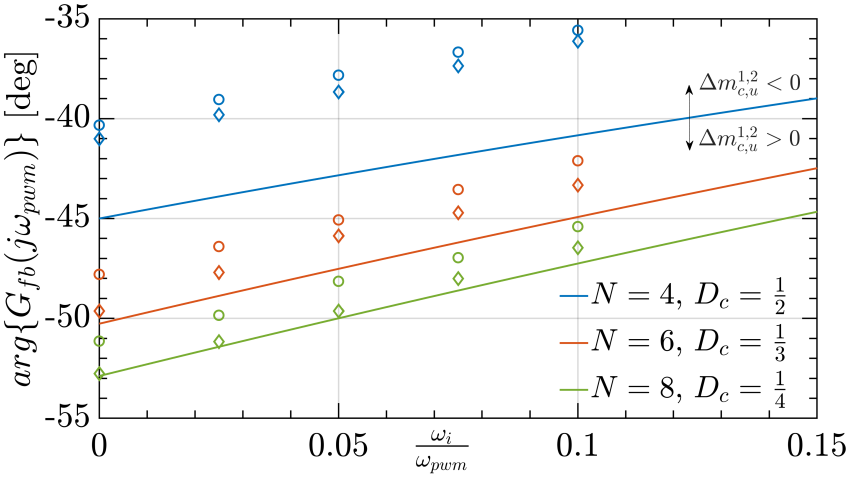


Figure 4.20: The in-phase condition boundary lines for the PI current control loops with $f_c = 0.093 f_{pwm}$. The results are shown for $N = 4$ and $D_c = \frac{1}{2}$, $N = 6$ and $D_c = \frac{1}{3}$, and $N = 8$ and $D_c = \frac{1}{4}$. The in-phase condition is satisfied below the boundary lines. The circular markers show simulated results with the digital low-pass filter $G_{fb}(z)$ in (4.21). The diamond markers show simulated results with the analog low-pass filter $G_{fb}(s)$ in (4.30).

To illustrate the impact of the feedback filter from (4.21) on m, the simulated modulating waveforms are shown in Fig. 4.21, for the same set-up as for Fig. 4.20, with $N = 4$ and $\omega_i = 0.03 \cdot \omega_{pwm}$. From Fig. 4.21, it is clear that without any filters, the operation is counter-phase for both slopes of w. Adding the digital low-pass filter from (4.21), with $\omega_{c,f} = 1.5 \cdot \omega_{pwm}$, almost completely flattens out both critical modulating segment pairs, by bringing the system to the border between the counter-phase and the in-phase operation. It is interesting to notice that for $N = 4$, due to the anti-symmetry of the triangular

switching ripple, the critical modulating segments for both slopes of w are affected in the same way. Moreover, for $N = 4$, only one critical duty cycle is present. Therefore, this specific filter setting is very attractive, as it prevents any vertical crossings from occurring. This fact will be exploited later on in the thesis. For the case of $\omega_{c,f} = \omega_{pwm}$, the operation is in-phase for both slopes of w.

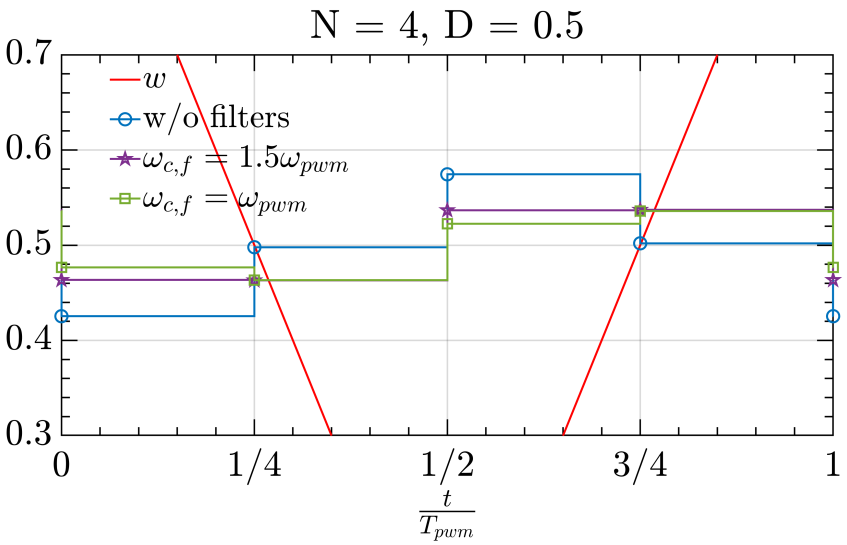


Figure 4.21: Illustration of the impact of $G_{fb}(z)$ from (4.21) on the intersections between m and w.

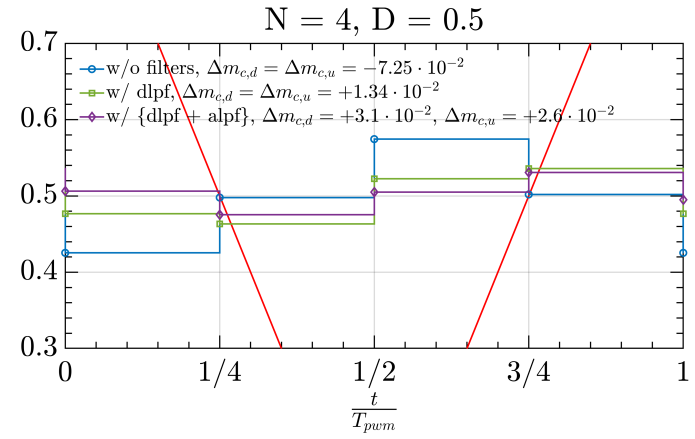
4.5.3.5 Examples of operation with duty cycle jittering

This section shows simulation and experimental results for operating regimes that feature the jitter amplification. The results are given for the current control loop of the dc-dc buck converter, corresponding to the set-up A described in Table 3.1. The DSP control platform, described in Section 3.2, is used for the experimental results. The PI controller from (4.22) is used, with $k_p = 0.035$ and $\omega_i = 0.03 \cdot \omega_{pwm}$.

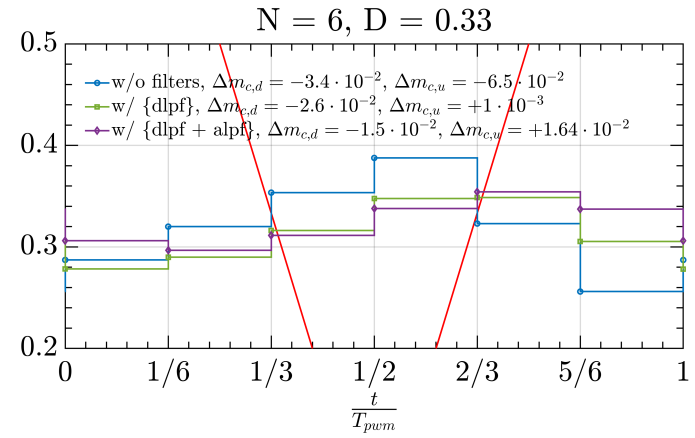
Tests are organized in the following way. For the oversampling factors $N \in \{4, 6, 8\}$, the operation is tested for three feedback configurations. First, as a benchmark, the operation is tested without any feedback filters, which results in the counter-phase operation. Then, the digital low-pass filter (dlpf) from (4.21) is introduced, with the cut-off frequency equal to $\omega_{c,f} = \omega_{pwm}$. The dlpf introduces 52° phase lag at the switching frequency, which, based on Fig. 4.20, enables the in-phase operation for $N = 4$ and is close to the borderline for $N = 6$ and $N = 8$. Finally, the analog low-pass filter (alpf) from (4.30), with the cut-off frequency equal to $\omega_{c,f} = 1.5\omega_{pwm}$ is added in a cascade with the dlpf. The alpf introduces 34° phase lag at the switching frequency. Based on Fig. 4.20, this filter cascade enables the in-phase regime for all tested values of the multisampling factor.

As a first validation, the simulated modulating waveforms corresponding to the tested regimes are plotted in Fig. 4.22, with their discontinuities reported in the legend. The modulating waveforms are obtained for the operation with a fixed reference, corresponding to the lowest critical duty cycle. For the case of $N = 4$ with both alpf and dlpf, the jittering occurs for $D = D_c = 0.5$; hence, the corresponding

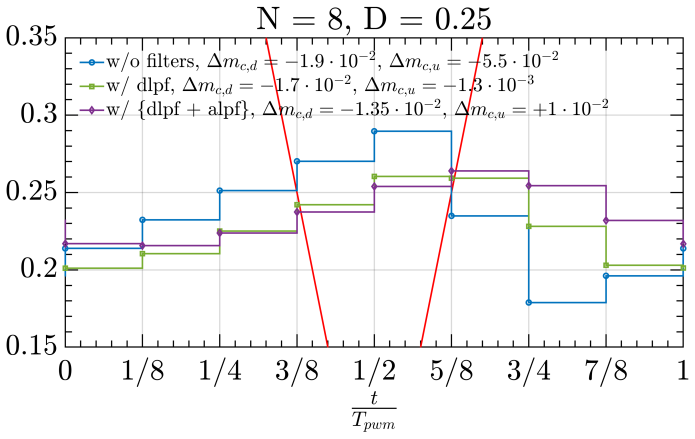
modulating waveform is not in steady-state. For other cases with the in-phase operation, the jittering occurs around, but not exactly for $D = D_c$.



(a)



(b)



(c)

Figure 4.22: Simulation results of modulating waveforms for different tested filter configurations: (a) $N = 4$, $D = D_c = \frac{1}{2}$; (b) $N = 6$, $D = D_c = \frac{1}{3}$; (c) $N = 8$, $D = D_c = \frac{1}{4}$.

The following results show three operating conditions, for each tested multisampling factor. Current references are chosen to result in a duty cycle that causes the jitter amplification when the filters are

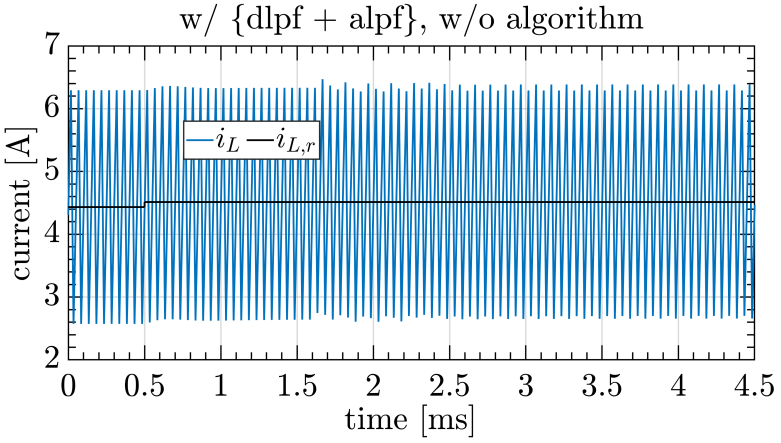
activated. Then, for the same regimes, the results are shown when the anti-jittering algorithm from Section 4.5.3.3 is activated. Finally, when the filters are bypassed, the operating mode is counter-phase, which is used as a benchmark case without the jittering.

Simulations results in Fig. 4.23 are given to examine the time-domain effects of the jittering and the dynamic performance of the anti-jittering algorithm. Responses are tested for $N = 6$ and a step reference change from $i_{L,r1} = 4.43$ A ($D = 0.665$) to $i_{L,r1} = 4.51$ A ($D = 0.677$). The results are given for the cascade of dlpf and alpf, without (Fig. 4.23a) and with (Fig. 4.23b) the proposed anti-jittering algorithm. From Fig. 4.23, it can be seen that the operating point enters the jitter zone at approximately $t = 1.6$ ms. A short transient is noticed when the anti-jittering algorithm is used, as the blocking of the modulating waveform update begins only after the first jitter is detected. In Fig. 4.23c, the reference tracking errors are plotted in order to observe the algorithm's impact on the transient response. The error traces are plotted relative to the current reference and, for a better visualization, the switching ripple is removed using a moving average filter. It can be seen that the algorithm does not significantly impact the step response, and the error caused by blocking the modulating waveform is quickly compensated by the controller.

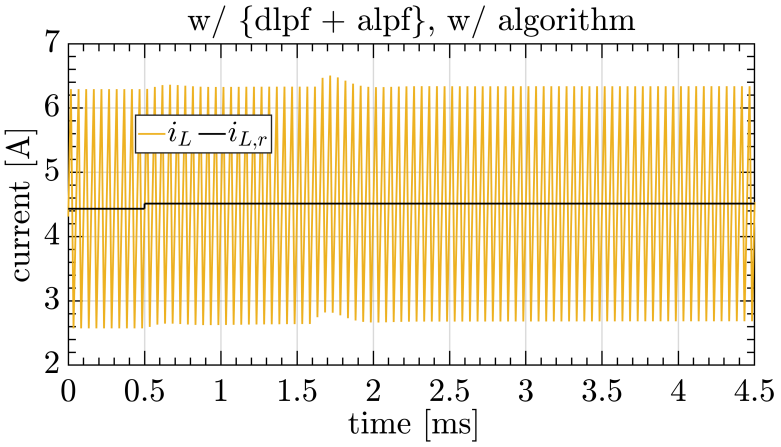
In Fig. 4.24, the experimental results of the inductor current spectra are shown, for $N = 4$ and $N = 8$, both with the cascade of alpf and dlpf. The inductor current data is obtained using a current probe with 300 kHz bandwidth and the oscilloscope RIGOL MS05104. The data is acquired with a rate of 500 MS/s, and the window length is equal to 50 ms. For $N = 4$, the current reference is set to 3.25 A and the corresponding results are shown in Fig. 4.24a. When both filters are activated, the jittering is present simultaneously for positive and negative slopes of the carrier. From the presented results, it is clear that the jittering causes a very high detrimental impact on the inductor current, which is successfully cancelled using the proposed algorithm. Similar conclusions are found for $N = 8$ in Fig. 4.24b, however, with a lower impact of jittering, which is expected as the discontinuities are decreased with the increase of N.

An important feature of the anti-jittering algorithm is to detect large-signal disturbances and prevent the blocking of the modulating waveform update. Fig. 4.25 is given to demonstrate that the algorithm allows detection of large-signal disturbances and offers an unimpaired response to a reference step change. The experimental verification is performed for the case of $N = 4$ with the cascade of dlpf and alpf, corresponding to results in Fig. 4.24a. The values of m are exported from the DSP memory. This example demonstrates the effectiveness of the proposed adaptive limits, described in Section 4.5.3.3, which are used to determine whether the modulating waveform update should be allowed or not.

Finally, the duty cycle variances, for all tested regimes, are calculated and compared with the analytical values from (4.20). For calculations, the differences between critical modulating segments are found for $D = D_c$, as shown in Fig. 4.22. For $N = 4$ with the dlpf, for $D = 0.48$, the calculated and the measured duty cycle variances are equal to $1.12 \cdot 10^{-5}$ and $1.38 \cdot 10^{-5}$, respectively. Without the jittering, the measured duty cycle variance is 10 times lower. For $N = 4$ with the cascade of dlpf and alpf, for



(a)



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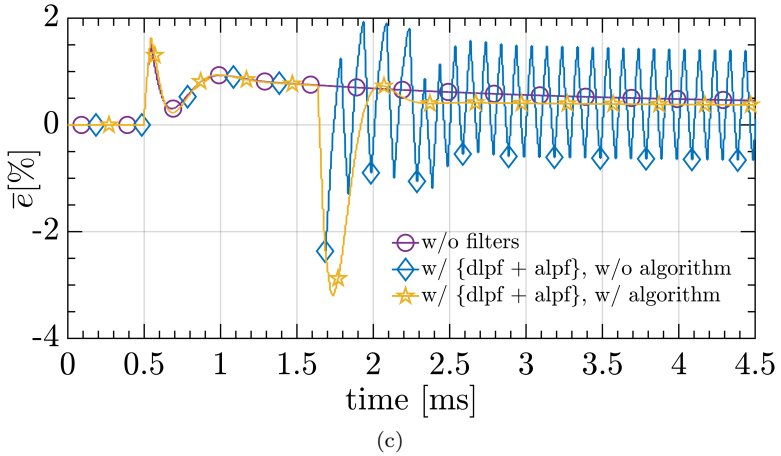
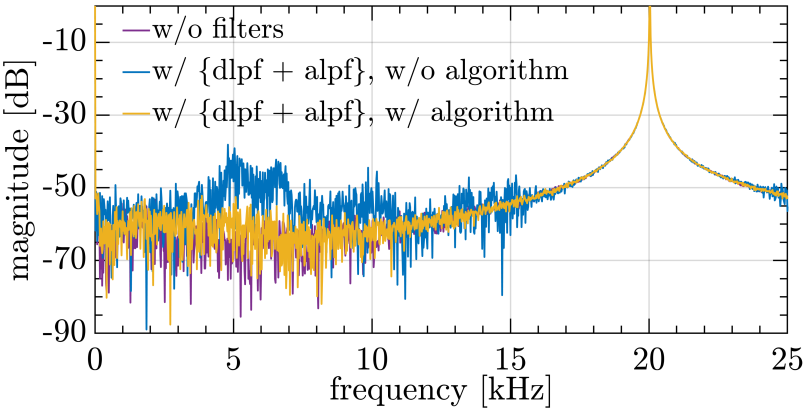


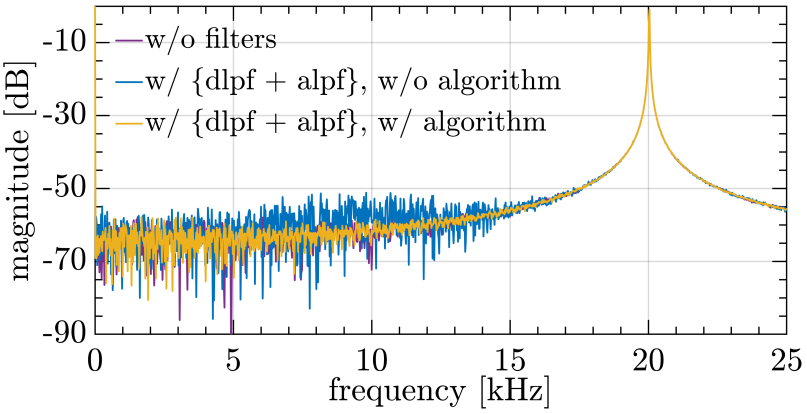
(c)

Figure 4.23: Simulation results of the reference current step responses for $N = 6$: (a) without the proposed anti-jittering algorithm; (b) with the proposed anti-jittering algorithm; (c) relative reference tracking errors.

$D = 0.5$, the calculated and the measured duty cycle variances are equal to $2 \cdot 10^{-4}$ and $2.78 \cdot 10^{-4}$, respectively. It should be noted that for this case, the jittering occurs simultaneously for both slopes of w; hence the statistical prediction is obtained using both $\Delta m_{c,d}$ and $\Delta m_{c,u}$. Without the jittering,



(a)



(b)

Figure 4.24: Experimental results of the inductor current spectra for: (a) $N = 4$ and $D \approx 0.5$; (b) $N = 8$ and $D \approx 0.25$.

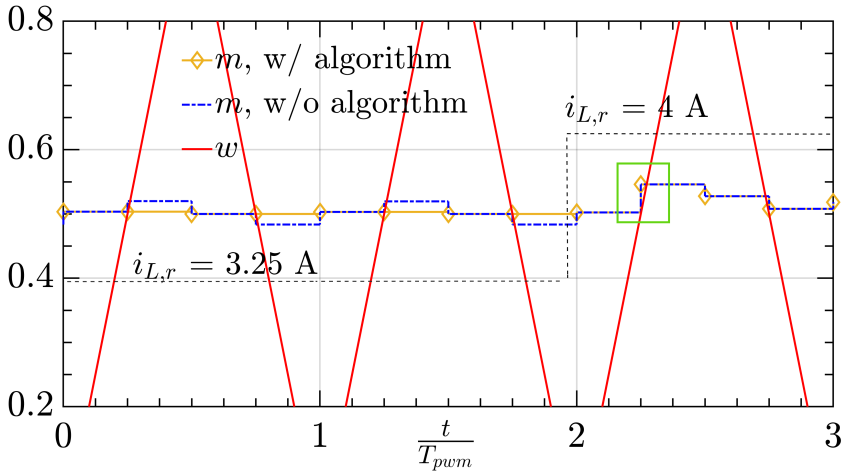


Figure 4.25: Experimental demonstration of the anti-jittering algorithm operation for the reference current step change from 3.25 A to 4 A, for the case of $N = 4$ with alpf and dlpf. Blocking of the modulating waveform update is prevented after a large disturbance is detected.

the measured duty cycle variance is decreased more than 100 times. For $N = 6$ with the cascade of dlpf and alpf, for $D = 0.325$, the calculated and the measured duty cycle variances are equal to $1.68 \cdot 10^{-5}$ and $2.8 \cdot 10^{-5}$, respectively. Without the jittering, the measured variance is reduced approximately 17 times. For $N = 8$ with the cascade of dlpf and alpf, for $D = 0.246$, the calculated and the measured duty cycle variances are equal to $6.25 \cdot 10^{-6}$ and $1.06 \cdot 10^{-5}$, respectively. Without the jittering, the measured variance is reduced approximately 20 times. From these results, it is clear that the statistical model from (4.20) offers a decent prediction of the intensity of duty cycle jittering. A certain amount of mismatch is expected, as the resulting LCOs are a stochastic phenomenon with a pattern that is not completely predictable.

From the presented results, it is clear that the jittering may result in a very high impact on the converter's output. The results also clearly demonstrate that the proposed anti-jittering algorithm is capable of canceling the jittering phenomenon.

4.5.4 MS-PWM modulating waveform and its discontinuities

Let us now continue with the analysis of all discontinuity-related nonlinearities. In this section, the procedure for calculating m in MS-PWM control systems is explained. Additionally, the impact of N, the control loop bandwidth, and the time delay on the modulating waveform discontinuities is analyzed.

4.5.4.1 Calculating the modulator transcharacteristic for MS-PWM

As explained in Section 4.4.2, the calculation of the modulator transcharacteristic corresponds to finding the steady-state waveform $m(t)$ that results in a specific value of D. For the case of NS-PWM, this procedure is relatively simple due to the fact that, for a given converter topology, the shape of the modulating waveform ripple $m^{ac}(t)$ is completely defined by the value of D. For a fixed value of D, any variation of the turn-on instant is equivalent to a time translation of $m^{ac}(t)$ [27].

On the contrary, for MS-PWM, the modulating waveform ripple cannot be specified within a time translation. For a specific value of D, in case the turn-on instant is changed, the output waveform ripple is simply translated, however, its sampled version features a shape change. Of course, this directly impacts the shape of $m(t)$ as well. Therefore, to obtain the MS-PWM transcharacteristic, an iterative numeric solver is needed, with the necessary steps reported in [27].

The analysis is simplified for control systems with a proportional controller and without digital feedback filters. For those, the sampler can be moved after the controller without impacting the shape of m [27]. This allows us to find the "analog equivalent" of the modulating waveform ripple, labeled m_{NS}^{ac}, based only on the value of D, just like for NS-PWM. Based on m_{NS}^{ac} and D, the entire "equivalent analog" modulating waveform m_{NS} can be found just like in Section 4.4.2. Then, an iterative procedure from [27] is used to determine the turn on instant that corresponds to the chosen sampling instants and the value of D, resulting in the complete sampled-and-held waveform m.

For the following results, the modulating waveforms and their discontinuties are calculated assuming

the proportional controller (without the one step computation delay) and without the feedback filters, i.e. as in Fig. 4.7a, only for the digital control. This configuration is chosen in order to show results of a general value, that are scalable with the relative crossover frequency $f_{c,r}$. The following methodology can, however, be extended to an arbitrary linear control system. Moreover, the calculations are performed for the set-up B.1, described in Table 3.2; however, as explained in Section 4.2.2, the results do not change for different converter parameters as long as the system with a proportional controller is analyzed with respect to the relative crossover frequency $f_{c,r}$. As noted before, the modulating waveform analysis for a proportional controller is expected to bring good results also for other high-frequency proportional-dominant controller structures, which is verified in the following sections.

In this chapter, it was mentioned several times that, for MS-PWM with very high oversampling factors, the operation resembles the analog NS-PWM. To corroborate this claim, MS-PWM transcharacteristics are calculated for the proportional control system with $N = 64$, $f_{c,r} = 0.1$, and 4 values of the time delay. Results are shown in Fig. 4.26 along with the ones obtained for NS-PWM (also shown in Fig. 4.9). The transcharacteristics overlap almost perfectly, which confirms the assumed behavior of highly oversampled MS-PWM systems. Note that, for the case of MS-PWM with $N = 64$, there are many critical operating points where the vertical crossings may occur (see (4.16)); however, their impact is not highly evident in the transcharacteristics, as the discontinuities of m are greatly reduced for high values of N. For this reason, it is clear that the analysis of the effects caused by the discontinuities can be limited to low values of N.

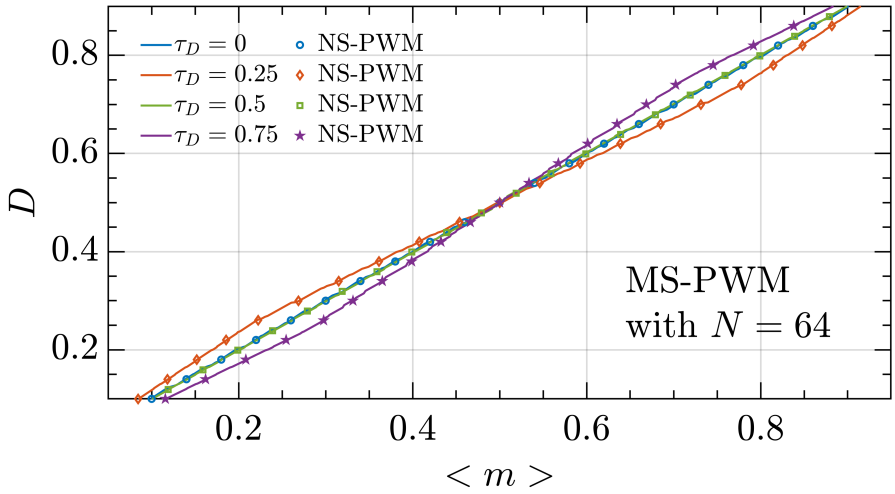


Figure 4.26: Calculated MS-PWM transcharacteristics for $N = 64$ and 4 values of the time delay τ_D. Results are compared to those obtained for the analog NS-PWM, which are plotted sparsely using only markers for a better visualization.

4.5.4.2 Discontinuity graphs

As noted in Section 4.5.3.1, around each D_c, the in-phase discontinuity of the critical modulating segments determines the height of the jitter zone in an MS-PWM transcharacteristic. Also for the counter-phase vertical crossings, it is clear that the discontinuities are correlated with the extension of the reduced- and the zero-gain zones. Therefore, it is of interest to find a way to easily determine whether the control system design enables the in-phase or the counter-phase operation, and to predict the size of the critical modulating segments' discontinuties.

Let us here propose an approximated procedure for calculating m in case of the proportional-dominant controllers, which does not require any iteration. This procedure relies on the approximation that m is obtained by simply sampling the "equivalent analog" m_{NS} at the chosen instants, e.g. those in (2.2). An illustration of the resulting waveforms is shown in Fig. 4.27. It is clear that, after m_{NS} is sampled in this way, the actual switching instants are slightly shifted, which translates the initially assumed m_{NS} as well; hence, an error is introduced. It is obvious that this error is increased for a higher switching ripple and lower values of N. Nevertheless, in this section it will be shown that this approximated method provides a good prediction of the critical modulating segments' discontinuties.

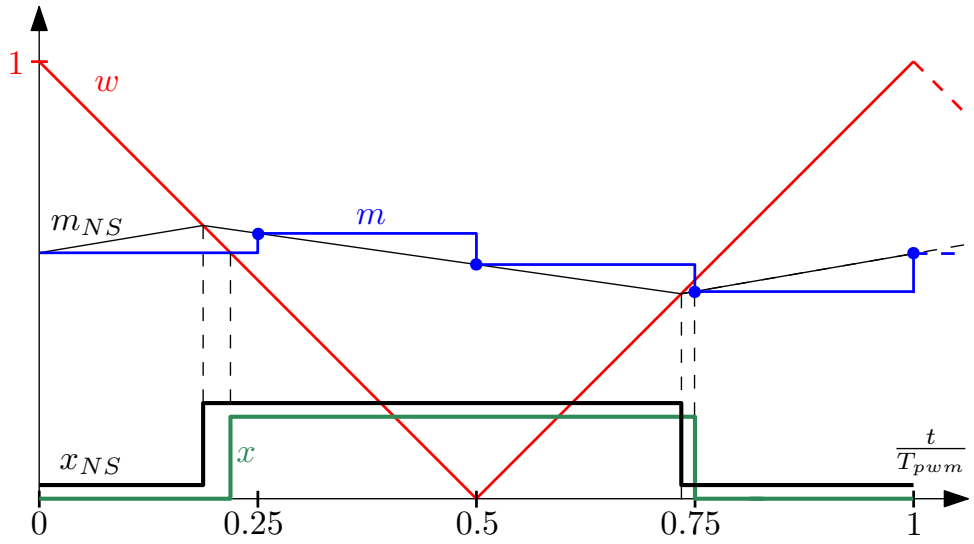


Figure 4.27: Illustration of the approximated procedure for calculating m, based on NS-PWM.

In this section, the discontinuity graphs are provided to illustrate the change of $\Delta m_{c,u,d}$, for various control loop bandwidths, as a function of the time delay. Dependency on the time delay comes from the fact that the types of intersections between m and w are determined by the shape of the m, which changes as the switching ripple component is shifted with respect to the carrier[7].

As an illustration of the time delay dependency, Fig. 4.28 shows how shifting the "equivalent analog" modulating waveform affects the discontinuity of the sampled-and-held m (using the approximation from

[7]Changing the time delay is not the only way to impact the intersections between the modulating waveform and the carrier. This can be also achieved by using filters with high-frequency properties suitable to re-shape the waveform m with respect to w, as shown in Section 4.5.3.4. However, the time delay was found to be a useful parameter to examine the discontinuities, without needing to resort to a specific filter design.

Fig. 4.27). It can be seen that the discontinuity for the positive slope of w is completely removed for $\tau_{D,2}$. As explained above, this sampling approximation does not completely match the system's behavior; however, it is clear that time-shifting the ripple component with respect to w will impact the shape of m.

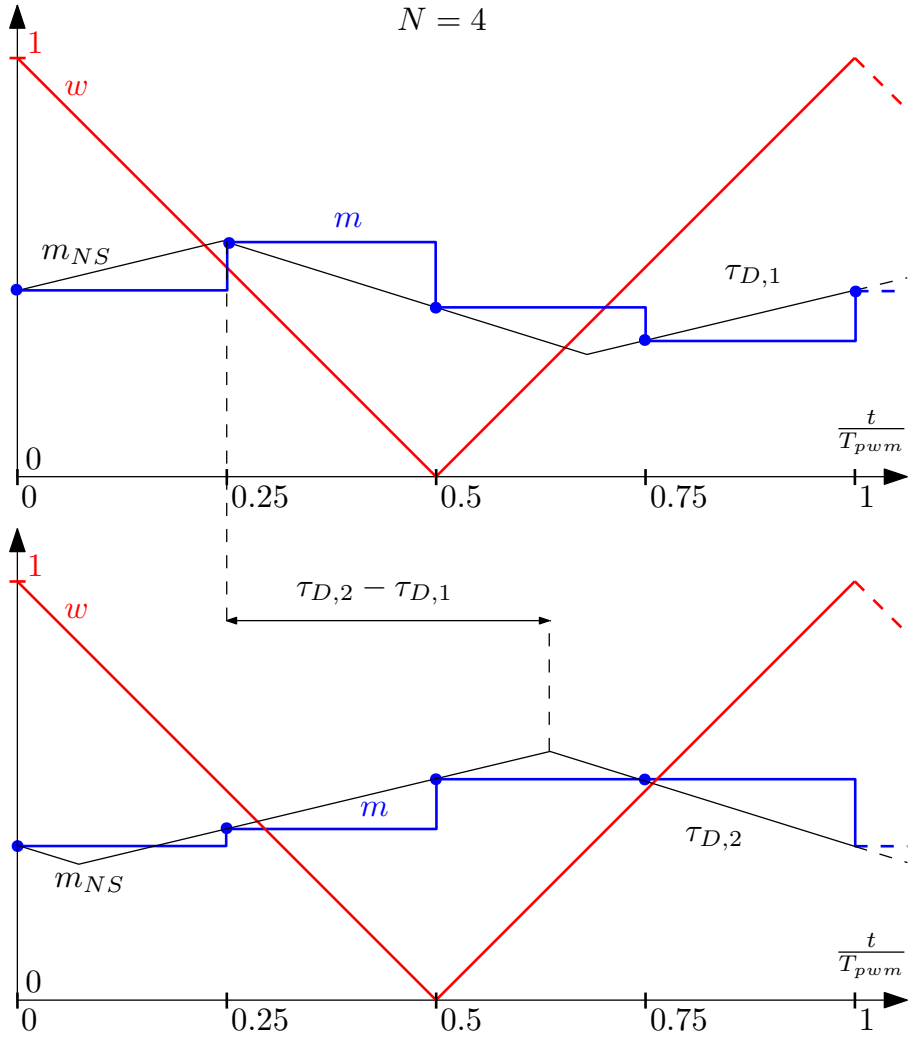


Figure 4.28: Illustration of the time delay impact on the sampled modulating waveform.

Due to the periodicity of the switching ripple, the analysis is limited to the range $\tau_D \in [0, 1)$. Results are given for $N \in \{4, 6, 8\}$ as the discontinuity-related effects are suppressed with the increase of the oversampling factor.

The following discontinuity graphs show $\Delta m_{c,u,d}$ for each examined pair of (N, D_c). The critical modulating segments' discontinuties are calculated as in (4.17), by finding the waveform m for $D = D_c$. As previously noted, the vertical crossings appear also in the vicinity of these duty cycles, however, it is of interest to see how this simple procedure based on a single operating point can be used to predict the properties of MS-PWM transcharacteristics. As stated in Section 4.5.4.1, for the exact calculation of m, an iterative procedure is needed. In this section m is also found using the proposed approximated

procedure, corresponding to Fig. 4.27. The approximated procedure is interesting as it reveals the discontinuities by simply solving a set of equations, i.e. without any iteration.

Note again that, due to the anti-symmetry of the current ripple in buck converters, the discontinuity graphs for $D = D_c$ for the positive slope of w are the same as the discontinuity graphs for $D = 1 - D_c$ for the negative slope of w. That is why, for $D_c = \frac{1}{2}$, the discontinuity graphs for the positive and negative slopes are always equal.

The results for $N = 4$ and $D_c = \frac{1}{2}$ are shown in Fig. 4.29. In this figure, a comparison is given for different values of $f_{c,r}$. It can be seen that the values of $\Delta m_{c,u,d}$ are indeed proportional to the relative crossover frequency. The graphs show a range of time delays for which the size of the discontinuities varies linearly, and a range for which it is constant. For the case of $f_{c,r} = \frac{1}{6}$, a comparison is made with the exact iterative calculation of m. The resulting values in the flat region are perfectly matched, while a small mismatch is seen elsewhere. For the figure clarity, other discontinuity graphs do not feature a comparison with the exact procedure; however, it is verified that the mismatch remains practically of the same entity. An important thing to note is the existence of two values of τ_D, almost independent on the relative crossover frequency, for which the operation turns from the counter-phase to the in-phase. For $N = 4$ and $D_c = \frac{1}{2}$, these values of τ_D are unique for both slopes of w, which is important as it indicates that the existence of such τ_D flattens out both pairs of the critical modulating segments, thus preventing any vertical crossings from occurring. This value of τ_D is tightly correlated with the low-pass filter design that brings the operation to a border between the in-phase and the counter-phase, seen in Fig. 4.21 in Section 4.5.3.4.

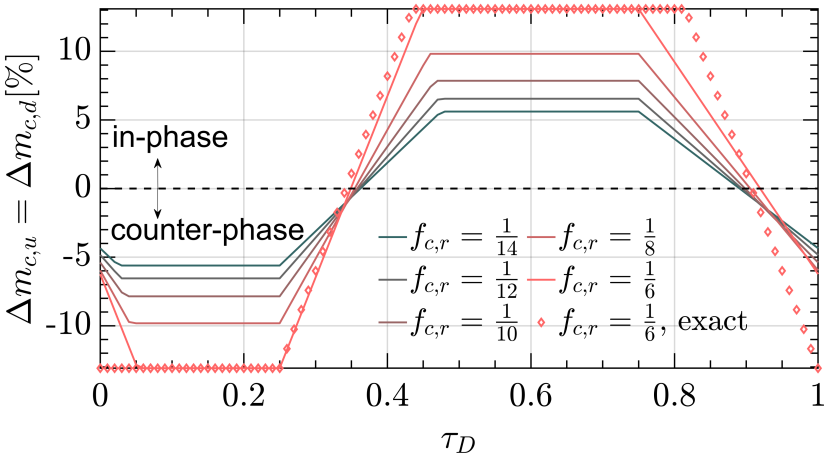


Figure 4.29: Discontinuity graphs for $N = 4$ and $D_c = 0.5$. Modulating waveforms are calculated using the approximated procedure for several values of $f_{c,r}$. For $f_{c,r} = \frac{1}{6}$, the result is compared with the one obtained using the exact procedure for the calculation of m.

For the figure clarity, results for other values of (N, D_c) are given only for $f_{c,r} = \frac{1}{10}$. It is verified that with the change of $f_{c,r}$, conclusions remain the same as for $N = 4$; the values of discontinuities are scaled, while the borders between the in-phase and the counter-phase operation remain located at nearly

constant values of τ_D.

In Fig. 4.30, discontinuity graphs are given for $N = 6$, $D_c = \frac{1}{3}$. The results are not shown for $N = 6$, $D_c = \frac{2}{3}$ as the two discontinuity graphs are anti-symmetric (what is $\Delta m_{c,u}$ for one would be $\Delta m_{c,d}$ for the other, and vice-versa). It can be seen that the sum of the maximum discontinuities for the positive and negative slopes of w is scaled by a factor $\frac{4}{6}$ compared to $N = 4$, which supports the fact that the increase of N suppresses the discontinuities.

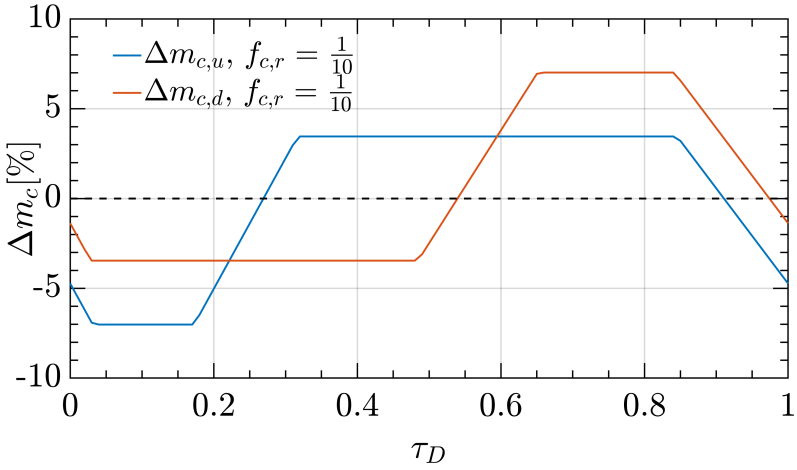


Figure 4.30: Discontinuity graphs for $N = 6$ and $D_c = 0.33$. The graphs are obtained using the approximated procedure for $f_{c,r} = \frac{1}{10}$.

In Fig. 4.31, the discontinuity graphs are given for $N = 8$, $D_c = \frac{1}{4}$, yielding similar conclusions as for $N = 6$, $D_c = \frac{1}{3}$. In Fig. 4.32, the discontinuity graph, valid for both slopes of the carrier, is given for $N = 8$, $D_c = \frac{1}{2}$. As for $N = 4$, $D_c = \frac{1}{2}$, there are two values of the time delay τ_D that result in a borderline operation for both slopes of w.

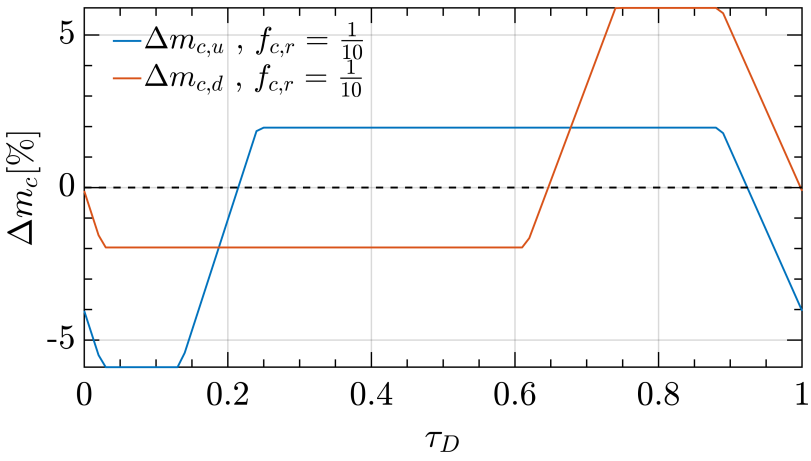


Figure 4.31: Discontinuity graphs for $N = 8$ and $D_c = 0.25$. The graphs are obtained using the approximated procedure for $f_{c,r} = \frac{1}{10}$.

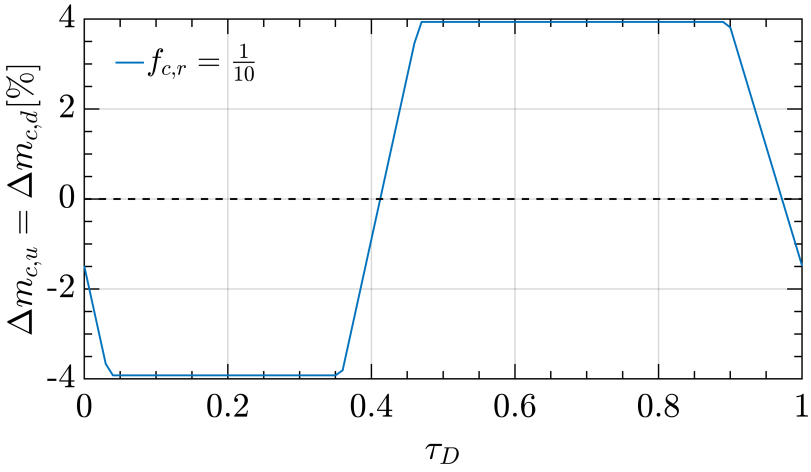


Figure 4.32: Discontinuity graphs for $N = 8$ and $D_c = 0.5$. The graphs are obtained using the approximated procedure for $f_{c,r} = \frac{1}{10}$.

An important thing to notice is that for critical duty cycles other than $D_c = \frac{1}{2}$, there is no unique time delay that results in the borderline operation between the in-phase and the counter-phase for both slopes of w. This means that, unlike for $D_c = \frac{1}{2}$, there is no time delay that can flatten out both pairs of the critical modulating segments.

To verify the applicability of the discontinuity graphs, which are calculated only for $D = D_c$, on predicting the MS-PWM operation around the analyzed operating point, three examples of modulator transcharacteristics are given in Fig. 4.33, for the case of $N = 4$, $D_c = \frac{1}{2}$, and $f_{c,r} = \frac{1}{10}$. The transcharacteristics are calculated using the exact procedure described in Section 4.5.4.1. The time delays are chosen to emphasize the counter-phase regime ($\tau_D = 0.1$), the in-phase regime ($\tau_D = 0.5$), as well as the borderline between the two ($\tau_D = 0.347$).

As predicted by the discontinuity graph in Fig. 4.29, the MS-PWM transcharacteristic for $N = 4$ can be completely linearized by imposing an appropriate time delay. Let us here make a connection between this result and the one from Section 4.5.3.4. Namely, by subtracting the one step computation delay that is assumed in Section 4.5.3.4, the borderline for $N = 4$ is here obtained for $\tau_D = 0.347 - \frac{1}{N} = 0.097$. The phase lag of the remaining transport delay, at the switching frequency, is approximately equal to $-35°$, which is close to the simulated borderline in Fig. 4.20. This hints that the analysis based on the time delay may also be used to directly predict the impact of feedback low-pass filters, which adds to the generality of the presented results.

Regarding the in-phase regime, seen in Fig. 4.33 for $\tau_d = 0.5$, the vertical part of the transcharacteristic matches with the value obtained using (4.18) and the discontinuity graph shown in Fig. 4.29. For the case shown, the two jitter zones corresponding to the positive and negative slopes of w are merged together. Note that the match between the jitter zone heights and the values predicted by the discontinuity graphs is confirmed for other values of (N, D_c) as well.

To conclude, the discontinuity graphs represent valuable means of predicting the MS-PWM behavior

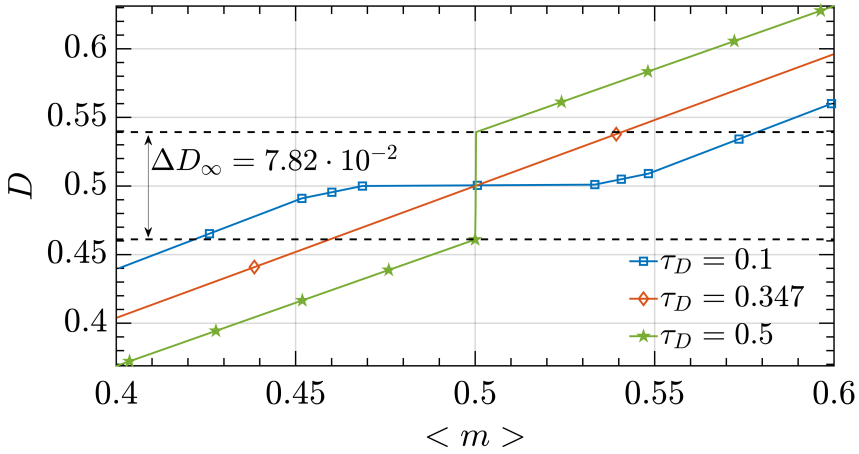


Figure 4.33: Demonstration of the impact of τ_D on the MS-PWM nonlinearities around $D_c = \frac{1}{2}$ for $N = 4$ and $f_{c,r} = \frac{1}{10}$. The transcharacteristics are given for the counter-phase operation (squares), which features the reduced- and zero-gain zones, the in-phase operation (stars), which features the jitter zone, and the borderline case (diamonds), which results in the linear transcharacteristic.

due to the following facts:

- they are easily calculated by solving a set of equations, without any iteration, for a single operating point;
- they can be used to find a borderline between the counter-phase and the in-phase operation, which remains nearly constant with the change of the relative crossover frequency $f_{c,r}$;
- they can be used to quantify the height of the jitter zone in case of the in-phase operation.

4.5.5 Analysis of MS-PWM transcharacteristics

This section analyzes the appearance and quantifies the extensions of the nonlinear zones in MS-PWM transcharacteristics. All transcharacteristics are obtained using the exact procedure described in Section 4.5.4.1. As for the discontinuity graphs, the following results are given as functions of the time delay.

4.5.5.1 Measures of MS-PWM nonlinearity

Let the MS-PWM transcharacteristic be labeled as $G = D(< \mathrm{m} >)$. The nonlinearity measures of G used in this section are:

- Root mean square (RMS) measure calculated as $\mathrm{RMS}(G - L(G))$, where $L(G)$ represents the linear regression of G, obtained using the least-square error criterion. This standard measure of nonlinearity is valuable as it tells us how close is G to its nearest possible straight line. However, it does not discriminate the different types of nonlinearities, which is important due to their unique impacts on a converter's output.

- Modified differential nonlinearity (M-DNL) measure. This measure discriminates the different nonlinearity zones in an MS-PWM transcharacteristic, and shows their relative extensions. The standard differential nonlinearity measure, i.e. $DNL = max\{|\frac{dD}{d<\mathrm{m}>} - 1|\}$, is not useful as the crucial information on the relative extension of each zone is not provided. As explained before, and seen in Fig. 4.12, there are only 3 possible types of nonlinearity zones. M-DNL shows which one is present and to what extent. For the analyzed transcharacteristic G, different zones are detected, and their total relative extensions are plotted: $\Delta< \mathrm{m} >_{\frac{1}{2}}$ is the total span of $< \mathrm{m} >$ for which G features a slope close to $\frac{1}{2}$ (the reduced-gain zone); $\Delta< \mathrm{m} >_0$ is the total span of $< \mathrm{m} >$ for which G features a slope equal to 0 (the zero-gain zone); $\Delta\mathrm{D}_\infty$ is the total span of D for which G is vertical (the infinite-gain zone).

In order to separately analyze each critical duty cycle D_c, the RMS and M-DNL measures are calculated for a certain ΔD around each D_c, where ΔD is chosen such that the related nonlinearity zones are fully covered.

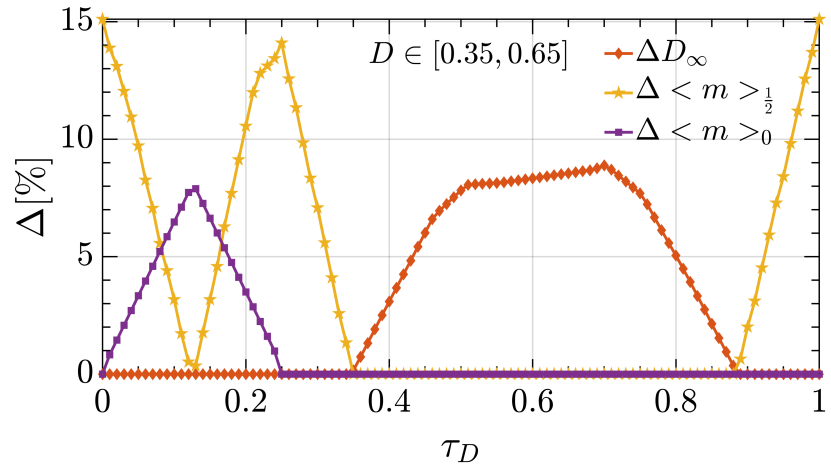
4.5.5.2 Nonlinearity graphs

For each analyzed N, the transcharacteristics are calculated for $\tau_D \in [0, 1]$ with 1% resolution and the duty cycle resolution of 0.1%. The results are given for the proportional controller and $f_{c,r} = \frac{1}{10}$.

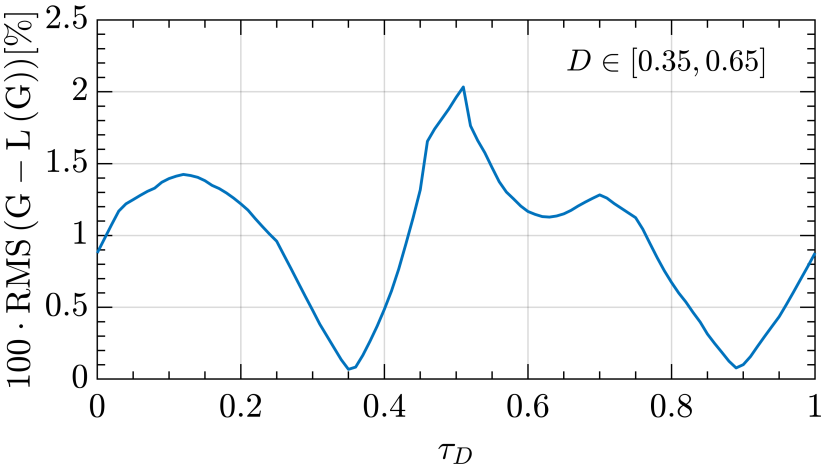
In Fig. 4.34, M-DNL and RMS measures are given for $N = 4$ around $D_c = \frac{1}{2}$. From Fig. 4.34a, it can be seen that the infinite-gain zones occur for approximately $\tau_D \in (0.35, 0.89)$. There, the values of ΔD_∞ are in excellent match with the values obtained using (4.18) and the discontinuity graph seen in Fig. 4.29. Note that M-DNL does not discriminate whether the jitter zones for the positive and negative slopes of w are merged into a single jitter zone, but only shows their joined height. It is also visible that the zero-gain zone has the highest extent for $\tau_D \approx 0.13$. There are regions around $\tau_D = 0.3$ and $\tau_D = 0.95$ where the reduced-gain (corresponding to a single counter-phase vertical crossing) is the only nonlinearity. For dc-dc converters, these regions are favorable as there are no uncontrollable operating points caused by the zero-gain zones and no LCOs caused by the infinite-gain zones. From Fig. 4.34b, it is clear that the border between the counter-phase and the in-phase operation ($\tau_D \approx 0.35$ and $\tau_D \approx 0.89$) results in the lowest RMS measure. Due to the finite resolution of τ_D, the plot only gets to show RMS values close, but not exactly equal to 0.

In Fig. 4.35, M-DNL and RMS measures are given for $N = 6$ around $D_c = \frac{1}{3}$. Note that, due to the anti-symmetry of the triangular switching ripple, these results are also valid around $D_c = \frac{2}{3}$. From Fig. 4.35b, it can be seen that the local minima are found near the values of τ_D where, for one slope of the carrier, there is a transition between the counter-phase and in-phase regimes. The minimization of the modulator nonlinearity near these borderlines is intuitive, as it corresponds to the flattening of one critical modulating segment pair. These borderline values of τ_D can be also read from the discontinuity graph in Fig. 4.30.

In Fig. 4.36, M-DNL and RMS measures are given for $N = 8$ around $D_c = \frac{1}{4}$ that are, thanks to the



(a)



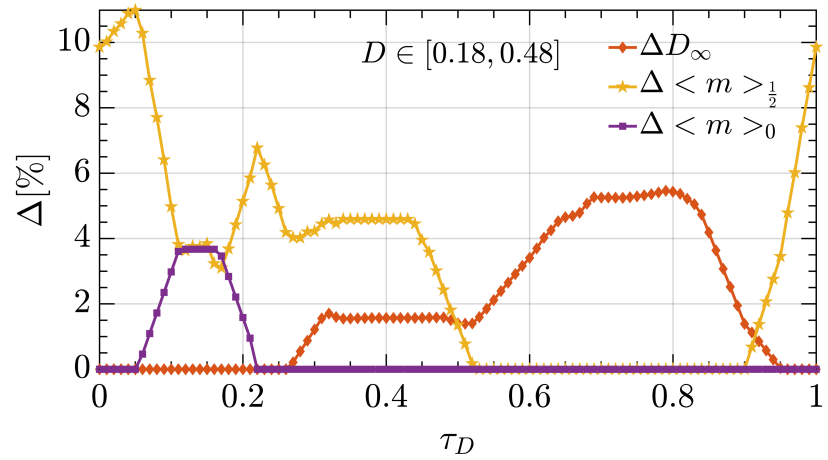
(b)

Figure 4.34: Nonlinearity measures for $N = 4$, $D \in [0.35, 0.65]$, and $f_{c,r} = \frac{1}{10}$: (a) M-DNL, (b) RMS measure.

anti-symmetry, also valid for $D_c = \frac{3}{4}$. The conclusions are the same as for $N = 6$, $D_c = \frac{1}{3}$.
In Fig. 4.37, M-DNL and RMS measures are given for $N = 8$ around $D_c = \frac{1}{2}$. The conclusions are the same as for $N = 4$, $D_c = \frac{1}{2}$. There are two values of the time delay, $\tau_D \approx 0.39$ and $\tau_D \approx 0.95$, for which the transcharacteristic can be completely linearized around that value of D_c. Again, these are not precisely obtained here due to the resolution of τ_D used for calculations.

From the presented results, it is clear that the increase of N results in lower nonlinearity measures. It should be noted that the nonlinearity measures are also calculated for several other values of $f_{c,r}$, and the results follow the same trends as those reported above. The reduced-gain, zero-gain, and infinite-gain zones are present in nearly the same range of τ_D, while their extensions are scaled proportionally to $f_{c,r}$.

The dependency of the nonlinearity measures on the time delay allows for an easy prediction of the MS-PWM behavior for existing delays in the system, e.g. for a verification if the dead-bands or the jitter-zones will appear. Furthermore, the results can be used to minimize the nonlinearities by imposing



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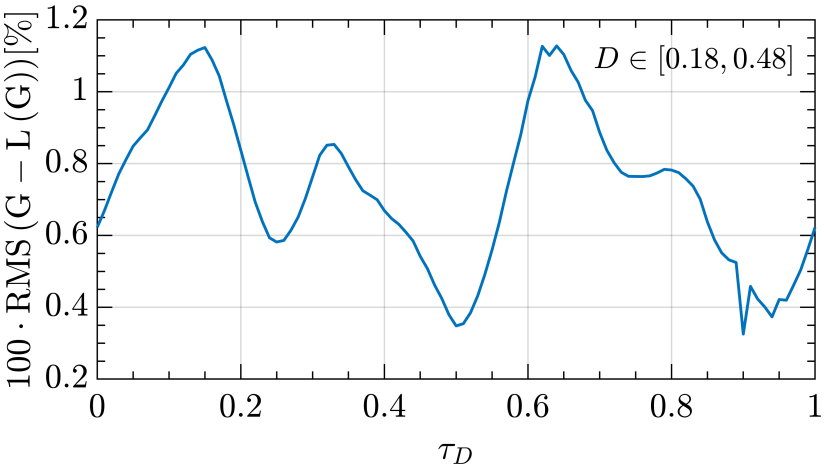


(b)

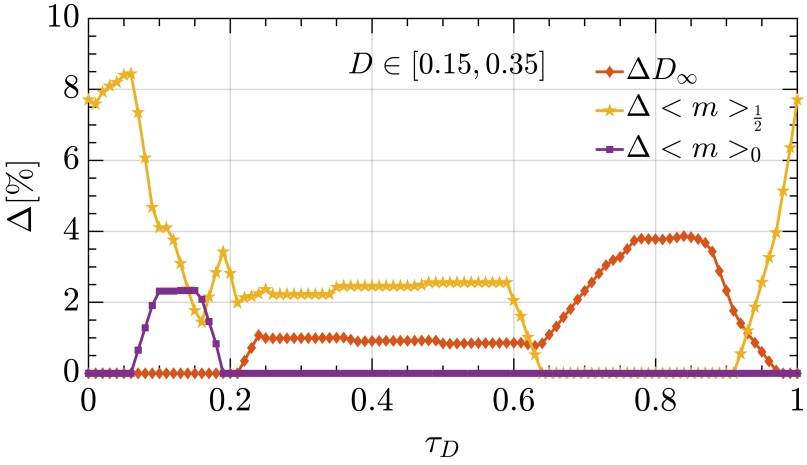
Figure 4.35: Nonlinearity measures for $N = 6$, $D \in [0.18, 0.48]$, and $f_{c,r} = \frac{1}{10}$: (a) M-DNL, (b) RMS measure.

an additional time delay. This is legitimate if structural delays of the system are below the desired value, also considering the resulting impact on the dynamic response. Note that it may not be optimal to add the time delay as a compensation measure. Instead, digital filters may be used, such that the desired effect on the shape of m is achieved, but with a more favorable impact on the dynamic performance. One example of such design is the borderline digital low-pass filter from Section 4.5.3.4.

To illustrate each of the distinct regions seen in the M-DNL graph in Fig. 4.35a, transcharacteristics corresponding to specific values of τ_D are plotted in Fig. 4.38.

4.5.6 Experimental verifications

The impact of the MS-PWM nonlinearities on a power converter's operation depends on the entire closed-loop control system design. As noted in Section 4.5.5, higher controller gains result in higher



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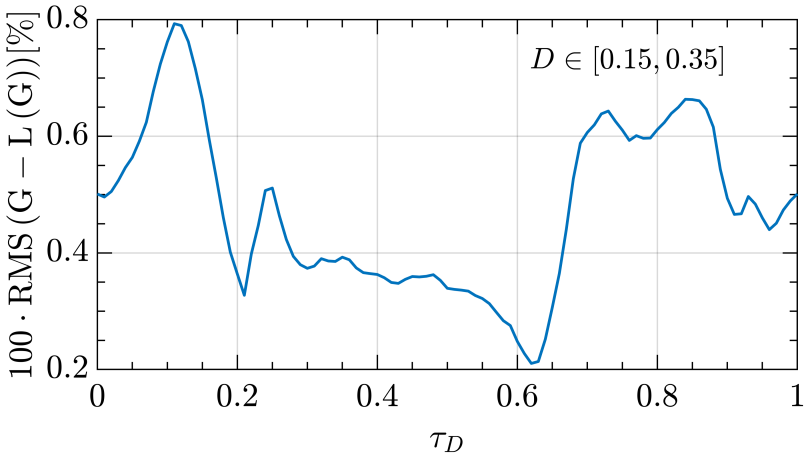


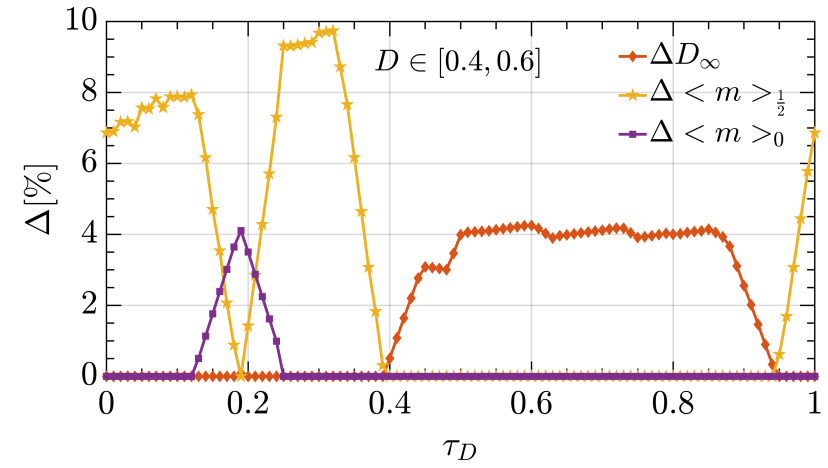
(b)

Figure 4.36: Nonlinearity measures for $N = 8$, $D \in [0.15, 0.35]$, and $f_{c,r} = \frac{1}{10}$: (a) M-DNL, (b) RMS measure.

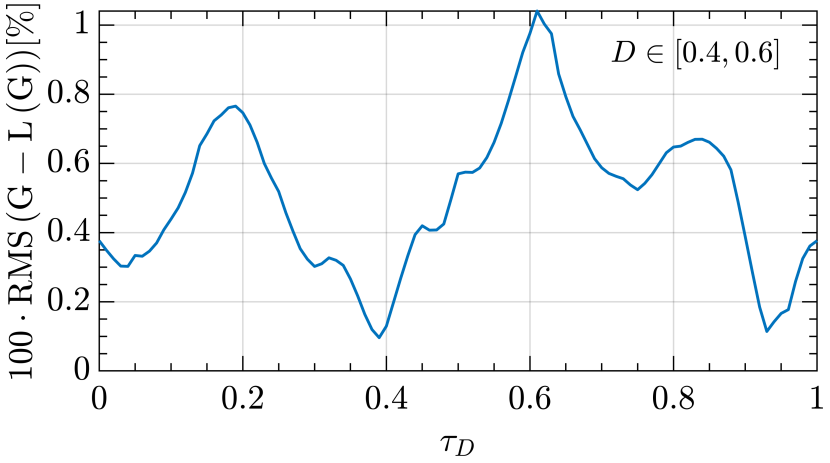
nonlinearity measures, however, also in a stronger disturbance rejection, which may mitigate the final impact on the converter's output. Therefore, this section offers an experimental examination of the MS-PWM nonlinearities in typical application scenarios. For dc-dc converters, the impacts on the transient response and the occurence of LCOs are investigated. For ac-type converters, it is examined how the MS-PWM nonlinearities impact the output waveform distortion.

For the following experimental tests, the used hardware set-ups are B.1 and B.2, described in Table 3.2, with the inductance value $L = 1.5$ mH. The FPGA control platform is described in Section 3.2. For postprocessing, data are acquired with 25 MS/s rate, using the Tektronix MS056 oscilloscope. The inductor current is sensed using the Tektronix TCP202 current probe. For the total harmonic distortion (THD) calculations, 100 ms of data are acquired.

The FPGA platform reads the ADC output with a rate of 40 MHz. This allows to set a value of τ_D with a resolution of 0.05%, using a delay line. Structural delays in the set-up include 700 ns due to the



(a)



(b)

Figure 4.37: Nonlinearity measures for $N = 8$, $D \in [0.4, 0.6]$, and $f_{c,r} = \frac{1}{10}$: (a) M-DNL, (b) RMS measure.

algorithm computation and 1.5 μs due to hardware delays from the current sensing to the transistor gate voltage. The modulating waveform is updated as soon as the control action is calculated, i.e. without the one step computation delay. The current sampling instants are re-scheduled to compensate the control execution time. In this way, the modulating waveform update instants correspond to those in (2.2). The transcharacteristics are experimentally measured by sweeping the current reference while storing the values of m and the detected D inside the control platform. For visualization, the experimentally obtained transcharacteristics are filtered by averaging results from 10 consecutive switching periods.

4.5.6.1 Impact of MS-PWM nonlinearities in dc-dc converters

To verify the impact of the MS-PWM nonlinearities on a dc-dc power converter's operation, the half-bridge set-up B.1, shown in Fig. 3.1a is used. The implemented controller is a PI from (4.3), discretized using the backward Euler method, and the crossover frequency is chosen as $f_c = \frac{1}{10} f_{pwm}$. The propor-

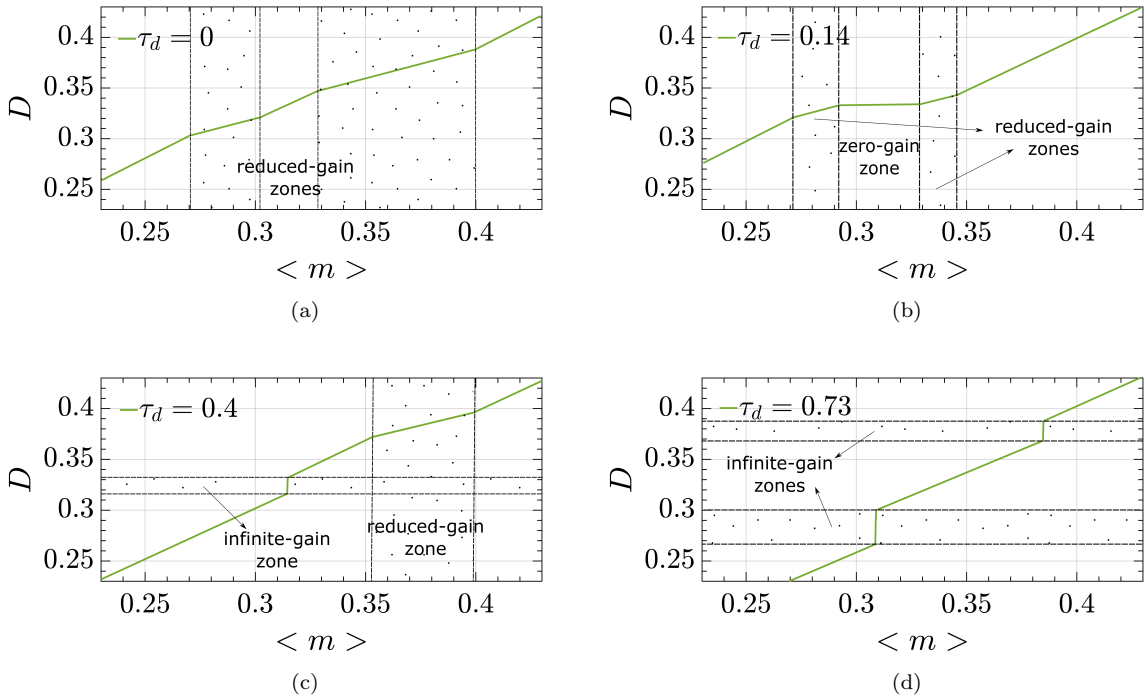


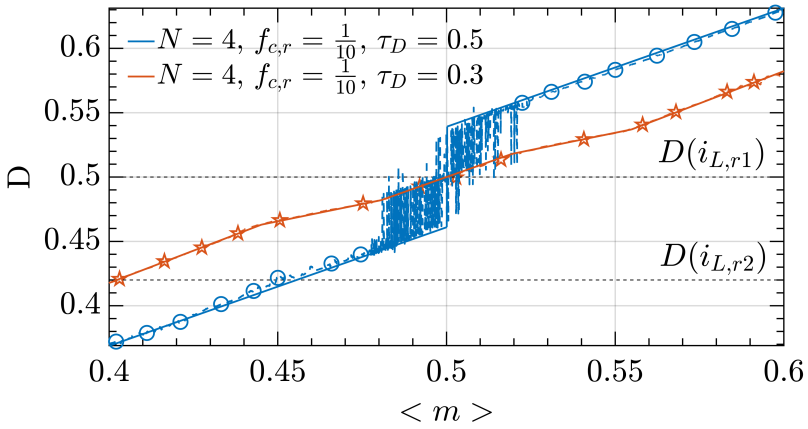
Figure 4.38: Examples of transcharacteristics around $D = 0.33$, for $N = 6$ and 4 values of τ_D. Each sub-figure corresponds to a different combination of the nonlinearity zones, as seen in Fig. 4.35a.

tional gain is calculated as $k_p = 2\pi f_c \frac{L}{V_{in}} = 0.048\ \frac{1}{\mathrm{A}}$. The integral gain is set to $k_i = 151\ \frac{1}{\mathrm{As}}$, to avoid an additional crossover before the LC resonance. Note again that the resulting MS-PWM control system is directly analyzed with respect to the previously shown nonlinearity graphs, which are calculated for the purely proportional controller. The impact of the added integral action at the frequencies of the switching harmonics is low; hence, a good match is expected.

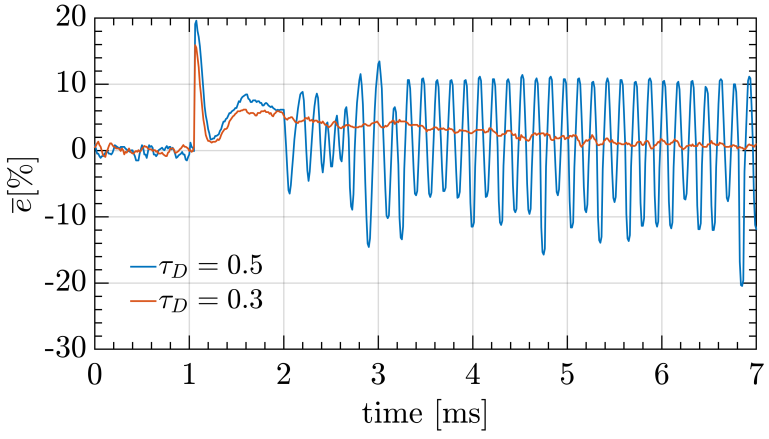
For dc-dc converters, it is instructive to verify the jittering operation, which appears when the operating point enters the infinite-gain zone of the MS-PWM trancharacteristics. This operation is problematic because it results in LCOs, which cannot be suppressed by the feedback. The difference compared to the results shown in Section 4.5.3.5 is that, here, the time delay is used instead of the low-pass filters. The control loop configuration with $N = 4$ and $\tau_D = 0.5$ is chosen. From Fig. 4.34a, it can be seen that this time delay results in $\Delta D_\infty = 7.82\%$. As a benchmark, the operation is also tested for $\tau_D = 0.3$, which brings the presence of the reduced-gain zones only. The experimental verification of the transcharacteristics belonging to these settings are shown in Fig. 4.39a. It can be seen that an almost perfect match is obtained, which confirms the validity of using the P-controller analysis for the PI-based control loops. The experimentally obtained points of the infinite-gain zone are plotted without averaging. Note again that in this zone the converter does not operate in steady-state; hence, the transcharacteristic is not well defined. The jittering operation is tested by imposing a step reference change, such that the duty cycle moves from the linear part, $D(i_{L,r1}) = 0.42$, to the infinite-gain part, $D(i_{L,r2}) = 0.5$. The tracking errors, relative to the dc value of the current, are shown in Fig. 4.39b. For visualization, the switching

ripple is removed using a MAF over the switching period. Starting from $t = 2$ ms, the LCOs are evident for the case of $\tau_D = 0.5$.

It is of interest to see whether the discontinuity and nonlinearity graphs can be used to predict the impact of LCOs. Given that both jitter zones in Fig. 4.39a are merged together, the variance is calculated based on (4.20) as $\sigma_D^2 = \frac{\Delta D_\infty^2}{4}$. For the corresponding jitter zone height, the predicted value of the duty cycle variance is $1.53 \cdot 10^{-3}$. The experimentally obtained variance is equal to $1.7 \cdot 10^{-3}$, which is in a good match with the prediction. This value can also be estimated from the discontinuity graph in Fig. 4.29.



(a)



(b)

Figure 4.39: Operation of the tested converter for $N = 4$ and two values of τ_D: (a) experimental verification (dashed line with markers) of the calculated transcharacteristics corresponding to $\tau_D = 0.5$ (circles) and to $\tau_D = 0.3$ (stars); (b) corresponding relative current errors for step responses from $D(i_{L,r1}) = 0.42$ to $D(i_{L,r2}) = 0.5$. The switching ripple is filtered out for a better visualization.

As mentioned in Section 4.5.2.2, impacts of the reduced- and zero-gain zones are difficult to analyze in general terms. The behavior of the converter depends on the size of the disturbance, the controller gains, the parameters of the converter, etc. Qualitatively, as long as the operation is locked in a reduced-gain

zone, the loop dynamics are halved. The zero-gain zone impact is particularly difficult to predict. For a large enough disturbance, a zero-gain zone may not have any impact at all, as the operating point may simply jump over it. If the modulating waveform is being perturbed across a dead-band, the converter practically exhibits an open-loop behavior, which may result in a significantly impaired response, far from the small-signal prediction. Nevertheless, the nonlinearity graphs can be used to find a suitable value of the time delay that minimizes the extension of the reduced- and zero-gain zones, which would consequently result in a smaller impact on the converter's operation.

4.5.6.2 Impact of MS-PWM nonlinearities in ac-type converters

For the verification of the nonlinearities' impact on ac-type power converters, the full-bridge set-up B.2, shown in Fig. 3.1b, is used. The operating parameters are summarized in Table 4.1. For the ac-dc tests, the PR controller from (4.4) is discretized using the impulse-invariant method [121]:

$$G_c(z) = k_p + k_r T_s \frac{1 - \cos(\omega_1 T_s) z^{-1}}{1 - 2\cos(\omega_1 T_s) z^{-1} + z^{-2}}. \tag{4.31}$$

The proportional gain is calculated based on the desired crossover frequency as $k_p = 2\pi f_c \frac{L}{2V_{in}}$, while the resonant gain k_r is calculated as $\frac{k_r}{k_p} = \frac{1}{10} 2\pi f_c$.

For ac-type converters, it is of interest to investigate the nonlinearities' impact on the output waveform distortion. As noted in Sections 4.5.4.2 and 4.5.5.2, the extension of the nonlinearity zones is proportional to the crossover frequency; however, the disturbance rejection also depends on it. Therefore, it is not possible to directly conclude that the increase of the nonlinearity measures, by increasing the bandwidth, would result in a worse quality of the output waveform.

The first set of results is obtained for $N = 4$. As the dead time itself is a significant source of distortion in ac-type converters [3], the impact of the MS-PWM nonlinearities cannot be observed on its own, except in simulations with the dead time set to zero. Therefore, DS-PWM ($N = 2$) is used as a benchmark. The designed control loops for $N = 2$ and $N = 4$ feature similar disturbance rejection properties; hence, the differences between these two values of N can be ascribed to the sources of distortion specific to MS-PWM.

The first goal of this section is to show that the analyzed nonlinearities are the dominant sources of distortion in MS-PWM controlled converters. This is tested by measuring the current THD for $f_{c,r} \in \{\frac{1}{14}, \frac{1}{10}, \frac{1}{6}\}$ and two sets of transcharacteristics related to $N = 4$. The first set is obtained by imposing a time delay $\tau_D = 0.1$, which results in the presence of the reduced- and zero-gain zones. The experimental verification of the corresponding transcharacteristics is shown in Fig. 4.40. Again, note that an almost perfect match is obtained between the experiments with the PR controller and the computations for the purely proportional one.

The second set is obtained by adding time delays $\tau_D = \{0.354, 0.347, 0.332\}$, respectively to the above listed values of $f_{c,r}$. These delays result in linear transcharacteristics, such as the one in Fig. 4.33. The inductor currents and their spectra are plotted in Fig. 4.41, for $f_{c,r} = \frac{1}{10}$. For time-domain

Table 4.1: Summary of the dc-ac converter results

Description	label	value	unit
Output frequency	f_1	50	Hz
Output voltage - RMS	v_c^{RMS}	230	V
Output current - RMS	i_L^{RMS}	4.9	A
Dead time	/	500	ns
Proportional gains	k_p	$\{0.017, 0.024, 0.04\}$	$\frac{1}{A}$
Resonant gains	k_r	$\{15.4, 30.2, 83.9\}$	$\frac{1}{As}$
Relative crossover frequencies	$f_{c,r}$	$\{\frac{1}{14}, \frac{1}{10}, \frac{1}{6}\}$	/
$N = 2$ - benchmark case	label	value	unit
Added delays	τ_D	0	/
Total harmonic distortion	THD	$-\{38.1, 39.8, 42.6\}$	dB
$N = 4$ - nonlinear transch.	label	value	unit
Added delays	τ_D	$\{0.1, 0.1, 0.1\}$	/
Total harmonic distortion	THD	$-\{24.9, 24, 24.1\}$	dB
$N = 4$ - linearized transch.	label	value	unit
Added delays	τ_D	$\{0.354, 0.347, 0.332\}$	/
Total harmonic distortion	THD	$-\{38.5, 39.5, 41.2\}$	dB

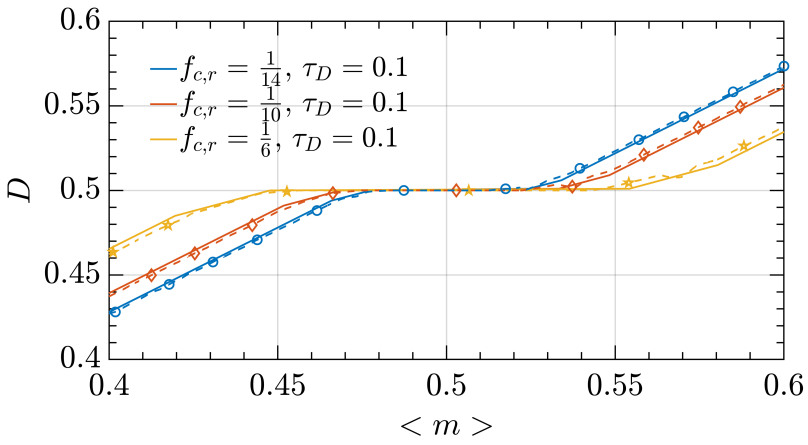
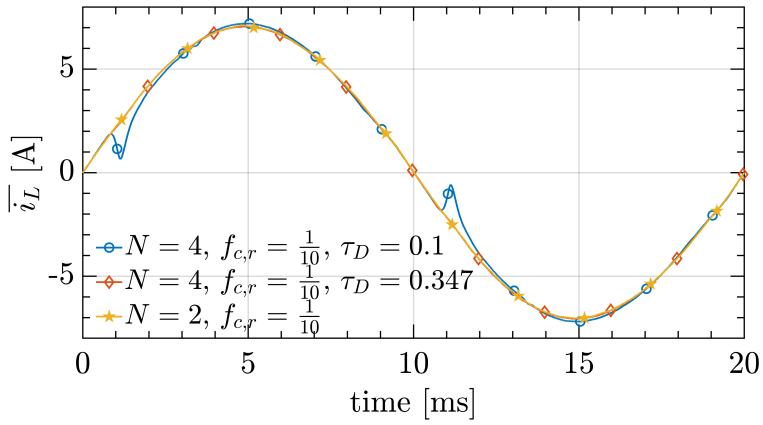


Figure 4.40: Experimental verification (dashed line with markers) of calculated transcharacteristics for $\tau_D = 0.1$ and $f_{c,r} = \{\frac{1}{14}, \frac{1}{10}, \frac{1}{6}\}$. The increase of the relative crossover frequency increases the extension of the nonlinearity zones.

visualization, the inductor current is averaged over T_{pwm} using a MAF. These results are compared to the benchmark case of the DS-PWM control, which does not feature any of the MS-PWM nonlinearities. It can be seen that for $N = 4$ and $\tau_D = 0.1$, the current is strongly distorted around the zero-crossings and the presence of strong odd harmonics is seen in the spectrum. When the time delay $\tau_D = 0.347$ is applied, the current distortion is significantly improved and the difference compared to the DS-PWM is

practically not visible. Also for other values of $f_{c,r}$, this trend is confirmed by the THD measurements, performed up to the 40^{th} harmonic, which are shown in Table 4.1. The THDs are reduced by 15 dB by adding the appropriate time delays.

The fact that these values are very close to those for $N = 2$ confirms that the remaining distortion is caused by the dead time. Differently from what was concluded in [34], the presented analysis and experiments suggest that the aliasing effect is not originating the measured distortion. Quite on the contrary, this appears to be a second order effect, negligible in size with respect to effects of the dead time and the nonlinear transcharacteristic. The aliasing-based distortion was noticed only in simulations with the linearized transcharacteristic and without any dead time. An important difference between the distortion caused by the aliasing and the modulator nonlinearities is that the aliasing-based distortion cannot be suppressed by the feedback; hence, it may be critical in some applications.



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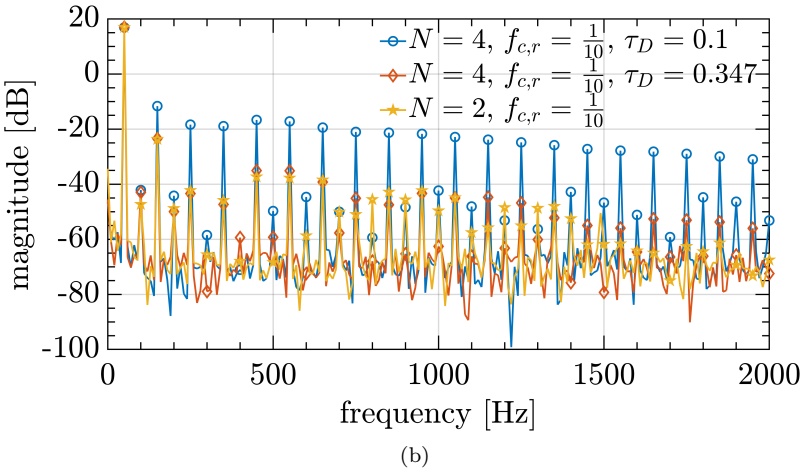


(b)

Figure 4.41: Example of the inductor current distortion for the tested full-bridge inverter. The comparison is made for $f_{c,r} = \frac{1}{10}$ between DS-PWM and MS-PWM with $N = 4$ for $\tau_D = 0.1$ and $\tau_D = 0.347$: (a) time-domain inductor current waveforms with the switching ripple removed for visualization; (b) spectral content in the frequency window used for THD calculations.

The second goal of this section is to show that higher nonlinearity measures do not necessarily result

in a higher distortion, if the control bandwidth is increased as well. This is tested by comparing the THD results for $N = 4$, $\tau_D = 0.1$, and $f_{c,r} \in \{\frac{1}{14}, \frac{1}{10}, \frac{1}{6}\}$, which corresponds to transcharacteristics in Fig. 4.40. The relative extensions of the reduced- and the zero-gain zones can be read from the nonlinearity graphs. For all values of $f_{c,r}$, the relative extensions are calculated and their values are $\Delta< \mathrm{m} >_{\frac{1}{2}} \in \{2.13, 3.18, 5.42\}\%$ and $\Delta< \mathrm{m} >_0 \in \{4.68, 6.47, 10.66\}\%$, respectively to the tested $f_{c,r}$. It can be seen that the extensions are proportionally scaled with $f_{c,r}$. The measured THD values are equal to $\{-24.9, -24, -24.1\}$ dB, respectively to the tested $f_{c,r}$. Although the extensions of the nonlinearity zones differ significantly, the resulting values of THD are similar, which confirms that the feedback is capable of suppressing the related distortion.

For values of N other than 4, the transcharacteristic cannot be completely linearized by flattening out the critical modulating segments; however, the resulting distortion can be minimized. As the nonlinearity graphs are given locally, around each D_c, they do not provide means for a global optimization, i.e. if the operating point moves across all values of D_c. In case the full-range optimization is required, the nonlinearity measures can be calculated for $D \in [0, 1]$. Another option is to use the presented nonlinearity graphs to find a value of the time delay that avoids a specific nonlinearity, e.g. the dead-band or the jitter-zone, in the entire operating range. Regarding the jitter zones, they were found to be highly unsuitable for ac-type converters as well because they introduce additional high-frequency distortion due to LCOs being manifested.

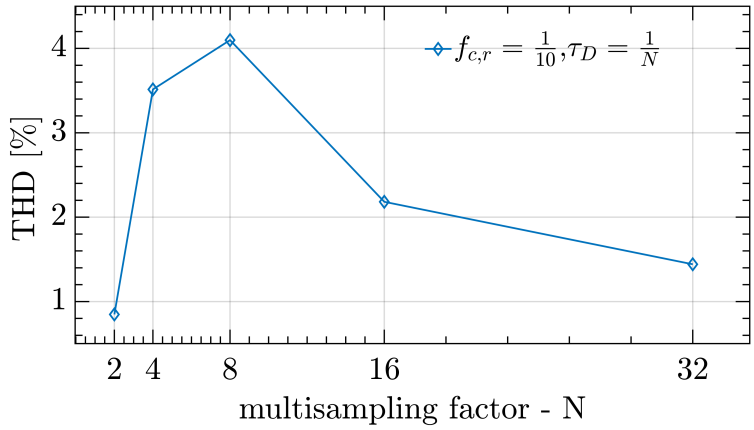


Figure 4.42: Inductor current THD for $f_{c,r} = \frac{1}{10}$ and control systems that feature the one step computation delay. The RMS value of the inductor current is equal to 4.9 A and the RMS value of the output voltage is equal to 230 V. The fundamental frequency is equal to 50 Hz.

As a final illustration, the impact of increasing the oversampling factor on the THD is shown in Fig. 4.42. The ac-dc operation perturbs the duty cycle in the range from 0.1 to 0.9. The results are shown for control systems with the one step computation delay, i.e. $\tau_D = \frac{1}{N}$. The crossover frequency is set to $f_{c,r} = \frac{1}{10}$ and no other actions for reducing the nonlinearities were taken. The double-update control clearly results in a lowest output distortion, setting the benchmark for MS-PWM to target. It can be seen that the distortion level is high for $N = 4$ and $N = 8$. The THD can be effectively reduced using

the methods proposed in this chapter and, at least for $N = 4$, even brought down to practically the same level as for $N = 2$. Without taking any actions, an effective suppression of the distortion caused by the MS-PWM nonlinearities starts to appear at $N > 8$, owing to the reduction of the discontinuities.

4.6 Summary

This chapter has analyzed the nonlinear MS-PWM properties that arise when m contains a significant switching ripple content. The main focus was placed on the set of nonlinearities caused by the jump discontinuities of m, which are specific to MS-PWM. First, the discontinuity-related nonlinearities are classified and the operating conditions that lead to them are explained in a general way. Besides the reduced- and zero-gain zones, which are already analyzed in [27], one of the original aspects of this thesis is the discovery of the third type of nonlinearities, the infinite-gain zones. These nonlinearities, which are shown to result in LCOs, are qualitatively explained, their impact on the duty cycle variance is statistically modelled, and an algorithm is proposed to cancel them out. The second part of this chapter brings the methodology for determining which nonlinearity will be manifested and to what extent, depending on the control system parameters. Moreover, provisions for minimizing their impacts are proposed and validated on the experimental prototypes.

Finally, let us note that the digital control systems that rely on multiple feedback samples per switching period are considered natural for series or parallel stacked multi-level or interleaved converters with phase-shifted PWM [55]. This is because, in balanced conditions, due to the increase of the ripple frequency, more than two instants per switching cycle appear where sampling the feedback signal yields its average value [51]. This means that the multi-sampled control can be implemented, ideally, without any ripple in m. However, in unbalanced conditions or during transients, the discontinuity-related nonlinearities may appear, a problem which is being investigated at the time of writing.

Chapter 5

Analysis of noise propagation in multi-sampled control systems

5.1 Introduction

An often mentioned advantage of adopting the single- or double-sampled PWM approach is that the sampling itself acts as a finite impulse response (FIR) filter, yielding the average feedback value. However, it is often hard to achieve a perfect synchronization, which is seen to introduce severe errors for certain operating modes [3, 63]. For example, this can cause aliasing, which is mentioned in Section 4.3. Furthermore, relying on only one or two samples per switching period can bring significant noise sensitivity [64].

To reduce the impact of acquisition errors, many applications rely on oversampling the feedback and then filtering it in the digital domain, e.g. using a moving average filter over one switching period [63, 64, 110, 111, 122, 123]. The filtered signal is then decimated to the control update rate, which is typically chosen as single- or double-update. These multi-rate strategies are introduced in Section 2.2.2 and labeled as MR-(S/D)S-PWM. For high oversampling factors, MR-(S/D)S-PWM methods approach the error-free acquisition (in terms of the actual average value) and may offer strong noise attenuation [63, 64]. These strategies can also be relatively easily implemented in commercially available DSPs, by exploiting the direct memory access (DMA) module [63]. However, strong filtering followed by the decimation to (S/D)S-PWM greatly deteriorates the dynamic capabilities of the system. These methods rely on oversampling purely for filtering purposes, with a strong penalty on the dynamic performance.

In MS-PWM control systems, the feedback is by definition oversampled, although to the purpose of improving the dynamic response. Correspondingly, the question arises of whether these systems also bring an inherent noise suppression. The motivation behind this chapter is to investigate mechanisms of noise propagation in power converters, with a specific focus on multi-sampled systems. Attention is dedicated to analyzing whether MS-PWM can reduce the impact of feedback noise, while maintaining

the dynamic benefits.

This chapter starts by recalling a standard model for noise propagation, valid for linear systems, in order to examine its validity in digitally-controlled power converters. It is shows that this simple model predicts well the system behaviour only in the case of (S/D)S-PWM. For MS-PWM, it is demonstrated how the DPWM introduces a nonlinear effect, by re-sampling the modulating waveform. This results in decimation, which causes aliasing and represents the main limiting factor for white noise attenuation in multi-sampled pulsewidth modulated power converters. The decimation effect is qualitatively explained and a design procedure is proposed for digital filters used to suppress the aliasing with as little impact on the dynamic performance. With the appropriate filter design, the decimation effects are reduced and noise propagation properties approach those of linear systems.

Additionally, in this chapter, analytical models are derived for noise propagation in power electronic control systems that feature decimation. A particularly challenging case covered is the one where the decimation occurs inside a closed-loop system. The resulting model is applicable for both MS-PWM (inherent decimation due to DPWM) and MR-(S/D)S-PWM (intentionally added decimation after over-sampled feedback filtering). Therefore, the results of this chapter can be used to estimate the noise sensitivity or to design filters to achieve a satisfactory performance in terms of the output noise content, for both MS-PWM and MR-(S/D)S-PWM.

Analytical derivations are followed by extensive experimental verifications that affirm the assumed noise signal properties in the experimental set-up, validate the derived noise propagation models, and confirm that, in terms of noise propagation, DPWM behavior closely resembles a re-sampler. Experimental results are given for a buck-type converter's single-stage current loop with a PI controller and a single-stage voltage loop with a PID controller. It is shown that, for PI controllers, strong noise suppression can be achieved by including digital filters that introduce a small impact on the dynamic performance. On the other hand, controllers with a derivative action bring a more emphasized impact of DPWM decimation; hence, stronger anti-aliasing filtering is needed for high noise attenuation.

In the end, this chapter features a comparison in terms of noise propagation and dynamic properties between MS-PWM with the proposed anti-aliasing digital filters and more commonly adopted strategies for oversampled filtering, i.e. MR-(S/D)S-PWM. It is shown that, for the same oversampling factor, noise suppression capabilities are practically the same (slightly better for MS-PWM), while MS-PWM results in drastically better dynamic capabilities.

It is important to note that this chapter mainly investigates and models the propagation of the uncorrelated, white noise, which is why the feedback signal should not be dominantly affected by, for example, the transistor switching noise. Most results found in this chapter are published in [67, 68].

5.2 Analyzed multi-sampled control system

An example of a dc-dc power converter, with MS-PWM control stage, is shown in Fig. 5.1. Results in this chapter are given for converters with dc operating points; however, it will be shown in Chapter 6

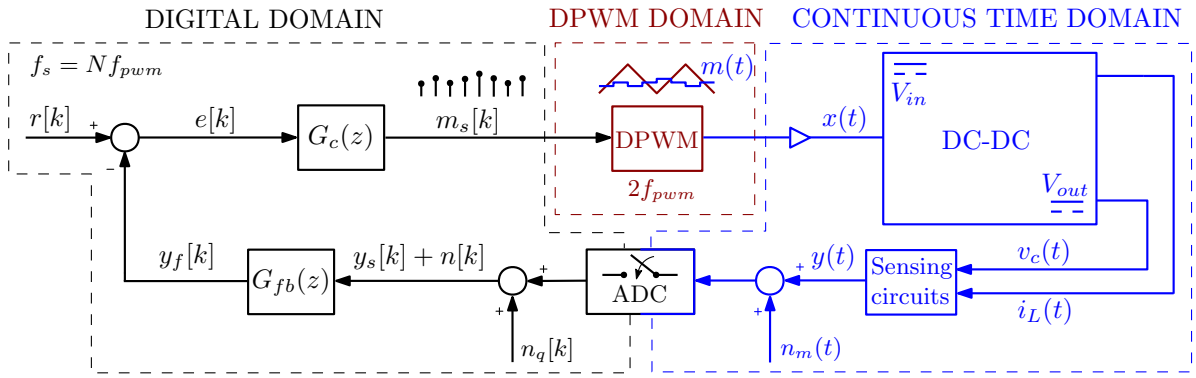


Figure 5.1: Multi-sampled control system of a dc-dc power converter with emphasis on its multi-rate structure. It is assumed that the converter features an output LC filter. The signals v_c and i_L correspond to the output capacitor voltage and the inductor current, respectively.

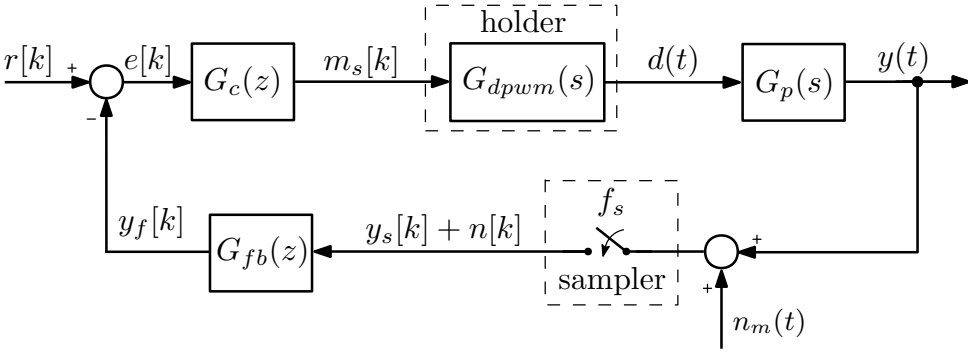


Figure 5.2: Simplified block diagram of the control system from Fig. 5.1.

that the presented analysis is directly applicable to ac-type converters as well. The analyzed converter operates using single-stage control loop configurations, where the output $y(t)$ (e.g. the inductor current $i_L(t)$ or the output capacitor voltage $v_c(t)$, in case of an LC output filter) is directly controlled by modifying the duty cycle. Single-stage loops are used in order to examine different properties of noise propagation related to the specific controller design.

The presented control system is of a multi-rate nature and can be separated in 3 sections, based on their operating frequency. As explained in Section 2.1, the ADC is used to sample the continuous time output variable, transforming it into the digital domain. After the sampling process, the ADC output is summed with $n_q(k)$, which models the quantization noise due to finite ADC resolution [3]. Note again that the control and sampling frequencies are not necessarily the same, e.g. in case of MR-(S/D)S-PWM where the decimation is imposed after the applied filtering. The DPWM block transforms its digital input m_s into the analog output x. As discussed in Section 2.1, the modulating impulse train $m_s[k]$ is held constant over one sampling period, which results in the modulating waveform $m(t)$. The triangular DPWM adjusts its output based on two values of $m(t)$ per modulation period, which is why the DPWM domain is labeled with $2f_{pwm}$. The re-sampling nature of DPWM is hinted in Section 2.2.3 and is the focal point of this chapter. The power stage and sensing circuits belong to the continuous time domain.

The converter's output $y(t)$ is summed with the measurement noise $n_m(t)$ resulting from sensing circuits.

A simplified block-diagram of the multi-sampled dc-dc converter, with only one noise signal $n_m(t)$, is shown in Fig. 5.2. It is assumed that gains of the sensing circuits are compensated within the controller and that their filtering action is negligible in the frequency range of interest; hence, they are replaced with unity gains. As explained in Section 2.2.2, the function of the holder is inherent to the DPWM, because that is the block where the conversion from the digital to analog domain takes place [3]. The small-signal DPWM model is given in (2.3).

5.2.1 Converter under test

For the experimental results shown in this chapter, the half-bridge hardware set-up B.1, with parameters from Table 3.2, is used. The inductance value is $L = 1.2$ mH. Without loss of generality, the same topology is used for the following analysis. The illustration of the half-bridge buck converter, with voltage and current measurements is shown in Fig. 5.3.

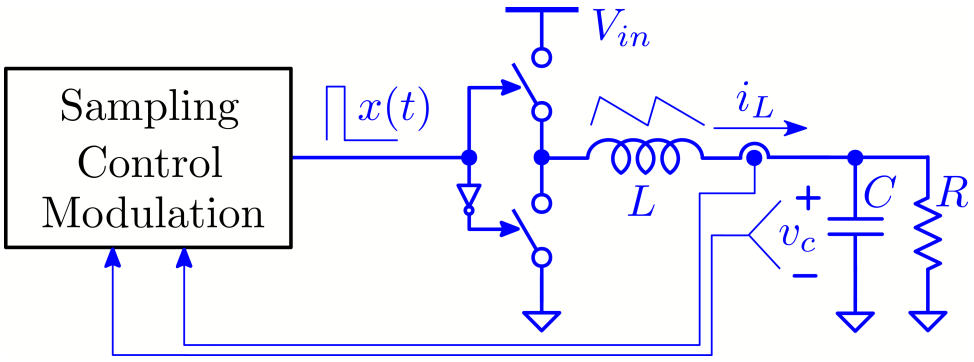


Figure 5.3: Schematic of the buck converter with the direct current or voltage control, used in this chapter.

Referring to Fig. 5.2, the plant transfer function from d to y, G_p, is obtained using the averaging technique [99]. For the current loop, it is equal to:

$$G_{p,i}(s) = \frac{i_L(s)}{d(s)} = \frac{V_{in}}{R} \frac{sRC + 1}{s^2 LC + s\frac{L}{R} + 1}. \tag{5.1}$$

For the voltage loop, it is equal to:

$$G_{p,v}(s) = \frac{v_c(s)}{d(s)} = V_{in} \frac{1}{s^2 LC + s\frac{L}{R} + 1}. \tag{5.2}$$

5.2.2 Controller design

For most results in this chapter, the control systems feature one step computation delay. The crossover frequency f_c of the control loops is chosen to be near $0.1 f_{pwm}$.

For the single-stage current loop, the zero in the plant transfer function (5.1) allows the crossover frequency to be set above the LC resonance using the PI controller structure [3]. The current controller

is labeled $G_{c,i}$:

$$G_{c,i}(z) = \left(k_{p,i} + k_{i,i}T_s\frac{1}{1-z^{-1}}\right)z^{-1}. \tag{5.3}$$

For the single-stage voltage loop, above the LC resonance the plant transfer function (5.2) exhibits a $-180°$ phase response. Therefore, in order to set such high crossover frequencies, a derivative action must be added to the controller; hence, the PID structure is chosen. Typically, to reduce its impact on noise, this kind of controller also features a low-pass filter in cascade with the derivative gain, which results in:

$$G_{c,v}(z) = \left(k_{p,v} + k_{i,v}T_s\frac{1}{1-z^{-1}} + \frac{k_d}{T_s}(1-z^{-1})G_{df}(z)\right)z^{-1}. \tag{5.4}$$

The derivative gain filter should provide attenuation at high frequencies, while not significantly reducing the phase margin. As an example, $G_{df}(z)$ is designed as a first order low-pass filter with a cut-off frequency equal to $\frac{f_{pwm}}{2}$, and is discretized using the bilinear transform. For simplicity, the entire structure $G_{c,v}$ will be referred to as the PID voltage controller. For a satisfactory phase margin near $0.1f_{pwm}$, the voltage loop is analysed only for $N \geq 2$.

The parameters of the controllers used in this chapter are summarized in Table 5.1.

Table 5.1: Controller parameters

Current loop	label	value	unit
Controller configuration	$G_{c,i}$	PI	/
Relative proportional gain	$\frac{V_{in}}{R}k_{p,i}$	0.2344	/
Relative integral gain	$\frac{V_{in}}{R}k_{i,i}$	585	$\frac{1}{\text{s}}$
Crossover frequency	$f_{c,i}$	2000	Hz
Tested oversampling factors	N	$[1, 2, 4, 8, 16, 32]$	/
Voltage loop	**label**	**value**	**unit**
Controller configuration	$G_{c,v}$	PID	/
Relative proportional gain	$V_{in}k_{p,v}$	1.3294	/
Relative Integral gain	$V_{in}k_{i,v}$	709	$\frac{1}{\text{s}}$
Relative Derivative gain	$V_{in}k_{d,v}$	$1.4 \cdot 10^{-4}$	s
Cut-off frequency of $G_{df}(z)$	$f_{c,d}$	10	kHz
Crossover frequency	$f_{c,v}$	1850	Hz
Tested oversampling factors	N	$[2, 4, 8, 16, 32]$	/

5.3 Noise properties and linear propagation modeling

5.3.1 Sources of noise and feedback acquisition errors

Some of the most relevant sources of noise and feedback acquisition errors, present in digitally controlled power converter systems, can be classified as:

- *Synchronous sampling errors.* As explained in Section 4.3, for the inductor current control with a nearly-constant output voltage and assuming no parasitic resistances, the average current value is sampled at the mid-points of the applied switched node voltage pulse (i.e. the center-pulse sampling). Often, designers rely on synchronizing the sampling instants with the peaks and valleys of the triangular carrier to obtain the average current value. However, due to many factors, such as the asymmetry of x with respect to w, parasitic resistances, actuation delays, dead-times, limited sensor bandwidths, and analog filters, the sampled value may significantly differ from the average current [3, 124]. Moreover, for voltage control loops, the average output voltage position within a switching period is not fixed for all operating points [117]. This type of an acquisition error can cause a significant impact on the system and is, therefore, one of the motivations for oversampling the feedback signal and averaging it over the switching period [63]. It should be mentioned that, at least for the current control, these errors are often reduced simply by delaying the sampling instants with respect to the ones in (2.2).

- *Switching noise*, resulting from high dv/dt and di/dt during commutations of the converter. Very steep edges of PWM voltage waveforms, together with the presence of various parasitic LC elements (due to winding parasitic capacitances, long cables in industrial drives, etc.), give rise to poorly damped oscillations in the output waveforms [63, 125, 126]. These effects again motivate the use of the oversampled averaging, for reducing the switching noise impact [63]. In multi-sampled PWM control, for certain operating points, sampling the switching noise cannot be avoided. This can cause an undesired response of the controller to noise corrupted samples of the feedback signal. The switching noise is strongly dependent on the hardware design and PCB layout, and the undesired effects depend also on the oversampling factor, the duty cycle, as well as the filter and controller design. Moreover, this type of noise is strongly correlated with the feedback signal, making it hard to treat analytically. The conclusions drawn in this chapter are valid for hardware systems that do not feature excessive propagation of switching noise.

- *Quantization noise*, which results from a finite resolution of ADC and DPWM modules [82–84]. As discussed in Section 2.2.1, in modern control platforms, the DPWM clock rates are in the order of hundreds of MHz and the effects of DPWM quantization have a small impact on the system if the switching frequencies are not extremely high. The ADC quantization noise depends on the full-scale feedback signal range and the number of ADC bits. In closed-loop systems, considering the quantization noise to be uncorrelated with the feedback is a strong assumption

[3,84], which prevents a simple analysis. For the following derivations, it is assumed that the ADC resolution is high enough such that the quantization noise is not dominant in the analyzed power converter system. This assumption often holds [64] and is validated in subsequent experimental measurements, using a 12-bit ADC.

- *Measurement noise* $n_m(t)$, which is caused by sensing and conditioning electronic circuits, as well as other sources of the electromagnetic interference (EMI) present at the converter's location [127, 128]. For the analytical considerations presented in this chapter, measurement noise is assumed to be a wide-sense stationary (WSS) Gaussian white noise [127], additive to the feedback signal. An example of noise with similar properties is the random thermal noise [127].

In closed-loop systems, such as the one in Fig. 5.1, measurement errors propagate to the output by feedback, negatively impacting the converter's operation. This motivates the analysis of noise propagation, in order to predict its overall impact on the output and, accordingly, design filters to suppress it below an acceptable level. In the subsequent analysis, it is assumed that the dominant source of noise is the *measurement noise*. This allows the use of relatively simple signal processing techniques due to its additive characteristics, being uncorrelated to the feedback signal. Extensive experimental validations support the assumed noise properties for the tested prototype.

5.3.2 Analysis of white noise propagation

For its simple and intuitive use in power electronic systems, the analysis in this chapter is performed in the frequency domain, avoiding as much as possible the strict use of the probability theory. For simplicity of the presentation, the frequency domain signals and transfer functions will be followed by parenthesis (ω), regardless of whether they belong to discrete or continuous time domains.

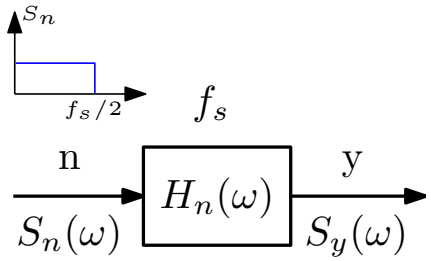


Figure 5.4: Illustration of linear processing of a discrete-time stochastic signal n. In the specific example, it is assumed that n is a white noise signal with a flat PSD S_n.

Let us start the analysis by studying the effect of processing a random discrete-time signal n by a linear time-invariant (LTI) discrete-time system with a transfer function $H_n(z)$, where z is the complex variable of the Z transform corresponding to the sampling frequency f_s. The LTI system of interest is shown in Fig. 5.4 and its output is labeled as y. The signal n is assumed to be a band-limited, WSS, and Gaussian white noise [127]. It will be pointed out throughout this chapter where and why this assumption is strictly necessary. Magnitudes of frequency components of a stochastic signal n can be

estimated from its power spectral density (PSD) $S_n(\omega)$, which is assumed to be stationary. However, information on its phase is not available; hence, it cannot be completely represented in the frequency domain. For this reason, its propagation through an LTI system cannot be analyzed directly, but only using its PSD. Let us start by finding the PSD of y, $S_y(\omega)$. Its well-known relation with $S_n(\omega)$ can be found by multiplying $y(\omega)$ with its complex conjugate[1] [127]:

$$S_y(\omega) = \frac{1}{f_s} y(\omega) y^*(\omega) = \frac{1}{f_s} \left(n(\omega) H_n(\omega)\right) \left(n(\omega) H_n(\omega)\right)^* = \frac{1}{f_s} n(\omega) n^*(\omega) |H_n(\omega)|^2 = S_n(\omega) |H_n(\omega)|^2. \tag{5.5}$$

With the information on the output PSD, the following formula can be used to calculate the in-band noise power (variance) of the output variable y, σ_y^2 [127]:

$$\sigma_y^2 = \int_0^{2\pi f_x} S_n(\omega) |H_n(\omega)|^2 d\omega, \tag{5.6}$$

where f_x defines the band of interest. Let us define the input noise power as $\sigma_n^2 = \int_0^{2\pi \frac{f_s}{2}} S_n(\omega) d\omega$. In case the input noise is white, S_n is constant (its PSD is flat across the Nyquist frequency range and $\sigma_n^2 = \frac{f_s}{2} S_n$); hence, it can be factored before the integral in (5.6). This can be used to define the Noise Attenuation Coefficient (NAC) for the white noise input as:

$$\text{NAC} = \frac{\sigma_y^2}{\sigma_n^2} = \frac{2}{f_s} \int_0^{2\pi f_x} |H_n(\omega)|^2 d\omega. \tag{5.7}$$

Going back to the analyzed power converter system in Fig. 5.2, as n_m is uncorrelated to the feedback, the sampler f_s can be applied to it independently, resulting in a discrete-time signal n entering the closed-loop system. In order to find the magnitude response $|H_n(\omega)|$, the system from Fig. 5.2 is transformed into the frequency domain:

$$H_n(\omega) = \frac{y(\omega)}{n(\omega)} = -\frac{W_{ol}(\omega)}{1 + W_{ol}(\omega)} = -\frac{G_{fb}(\omega) G_c(\omega) G_{dpwm}(\omega) G_p(\omega)}{1 + G_{fb}(\omega) G_c(\omega) G_{dpwm}(\omega) G_p(\omega)}, \tag{5.8}$$

where $W_{ol}(\omega)$ is the open-loop transfer function of the system shown in Fig. 5.2. The discrete-time blocks are transformed to the frequency domain using $z = e^{j\omega T_s}$. To consider the impact of the sampler in Fig. 5.2, the frequency response of the cascade of G_p and G_{dpwm} is obtained by first transforming it to the Z-domain, using the impulse-invariant discretization with frequency f_s [4].

PSD of the sampled, band-limited, white noise signal is spread across the Nyquist frequency window; hence, it is reduced as the sampling frequency is increased. This spreading is determined by the factor $\frac{2}{f_s}$ in (5.7). The integrand in (5.7) determines the filtering impact of the system, depending on its magnitude

[1] Strictly speaking, multiplication of a frequency domain signal with its complex conjugate results in its squared frequency components' magnitudes, which are related to the energy spectral density (ESD) [127]. However, this relaxed and somewhat mathematically inaccurate definition will be used here to avoid adding complexity by introducing limit values and expectation operators. Additionally, the factor $\frac{1}{2}$ is needed to obtain squared RMS values from squared magnitudes. The considered PSD is, therefore, found by dividing the squared RMS values of frequency components by the total one-sided frequency range of interest $\frac{f_s}{2}$. In case of discrete-time measurements with a finite number of samples, PSD is obtained by dividing with spectral resolution instead.

response in the frequency range of interest. An intuitive way of decreasing the noise power, even without oversampling, is to design control loops with lower bandwidths, providing a higher filtering action by $|H_n(\omega)|$. These two mechanisms jointly impact the white noise propagation in linear multi-sampled systems.

The Nyquist frequency of the multi-sampled systems surpasses the switching frequency of the converter. As the small-signal plant model $G_p(s)$ is obtained using the averaging technique [99], it is only valid up to a fraction of the switching frequency. Additionally, at higher frequencies, the switching ripple is dominant in the output spectrum, which is why it is hard to experimentally measure the noise floor without incorporating its impact. Hence, in order to correctly estimate the output variance, the frequency window in (5.7) must be limited below f_{pwm}.

It is important to notice that the analysis based on (5.7) is strictly valid for linear systems only, which is not the case for switched power converters. However, it is of interest to examine how well, and under what conditions, can (5.7) be used to predict noise propagation in power electronic converters. In Section 5.5 the analysis is extended to cover the main nonlinearity, later to be shown as caused by the carrier in MS-PWM.

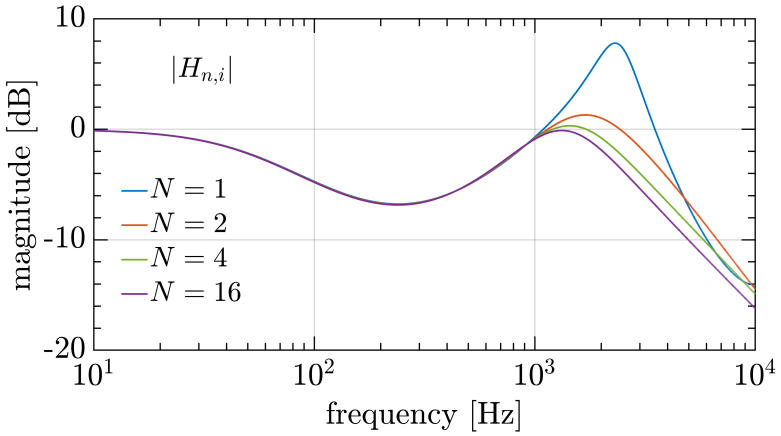
For subsequent verifications, the controller parameters in Table 5.1 are chosen according to the lowest tested N, after which they are kept constant. In this way, the crossover frequency remains the same, while the phase margin is increased for higher oversampling factors. This allows the examination of noise propagation for different multisampling factors in relative terms, without significantly altering the MS-PWM nonlinearities, which are analyzed in Chapter 4. Furthermore, by having significant differences in the phase margins for lower values of N, the results are expected to emphasize the impact of filtering brought by the closed-loop system $|H_n(\omega)|$. For higher values of N, phase margin differences are very small; hence, the only expected impact on noise propagation is, instead, the white noise spreading across the Nyquist frequency window.

Magnitude responses of the closed-loop transfer functions from the feedback noise to the output, $|H_n(\omega)|$, for the analyzed current and voltage control loops, are shown in Fig. 5.5.

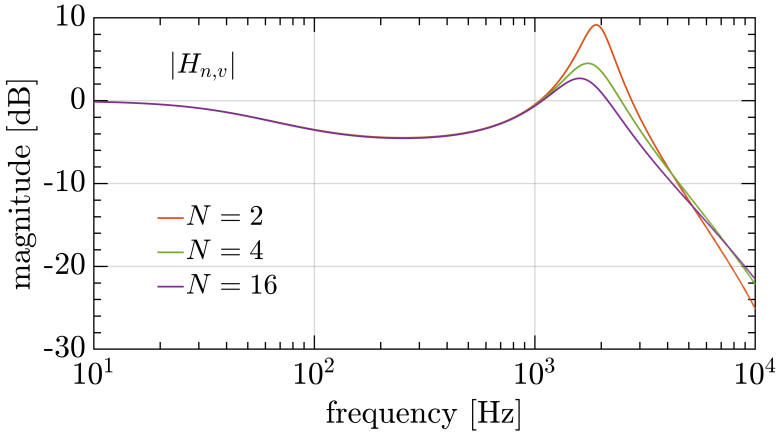
5.3.3 Noise measurement organization

The organization of the system used for noise propagation measurements is illustrated in Fig. 5.6. The converter is run in closed-loop configuration, with an imposed constant reference value. After the steady state is reached, the output is measured and its PSD, determined by the feedback noise propagation, is estimated.

In simulations, the noise signal is sampled independently from the feedback to be able to directly find the frequency response from n to y. For white noise, this corresponds to obtaining the frequency response $H_n(\omega)$. In this case, both n and y are acquired for postprocessing with $f_{acq} = f_s$. For later-shown experimental tests, this approach is not feasible, as the input noise cannot be sampled independently from the feedback. Therefore, only the output y is acquired using an oscilloscope. The output is probed



(a)



(b)

Figure 5.5: Magnitude responses of the closed-loop transfer functions for: (a) direct current control $H_{n,i}$ and (b) direct voltage control $H_{n,v}$. Hardware and control parameters are shown in Table 3.2 and Table 5.1.

before being conditioned for sampling, in order to observe the impact of the feedback noise on the physical output itself, i.e. i_L or v_c. Since only the output is measured, the analytical procedure can be used to predict its variance based on knowing the input noise power or, more simply, by finding the output noise power relative to one of the measured cases. Both approaches are used in this thesis. The oscilloscope acquisition rate f_{acq} is set significantly higher than the probe bandwidth, to prevent aliasing, and the window length T_{data} is determined to obtain a satisfactory frequency resolution (equal to $\frac{1}{T_{data}}$), such that spectral leakage from dominant switching harmonics is not high. Specific oscilloscope settings are explained in Section 5.6. The resulting output noise power is calculated from the acquired signals, in the frequency domain, by summing the squared RMS component values in the frequency region of interest.

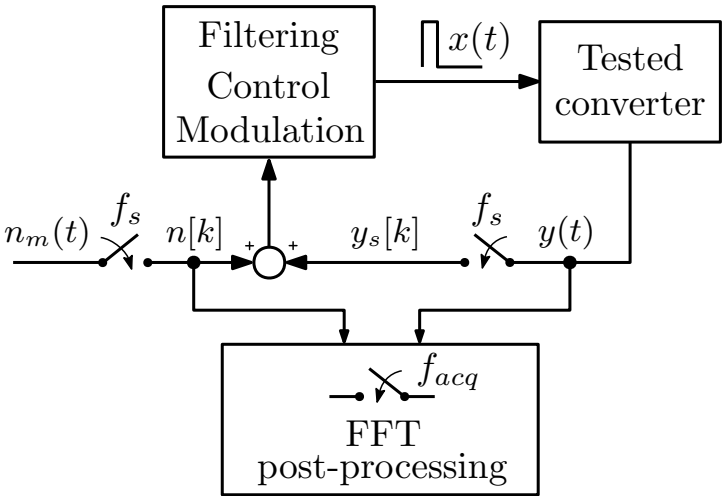


Figure 5.6: Block diagram of the noise measurement set-up. For simulations, the noise signal n_m is injected using a random number generator. It is sampled independently of (but synchronously with) the feedback, to be able to also observe the discrete signal n. For experiments, there is a unique sampler after the summing block and only the output signal y is acquired via an oscilloscope.

5.4 Impact of DPWM decimation

5.4.1 Aliasing caused by DPWM decimation

The analytical model in (5.7) is strictly valid only for LTI systems. Power converters, although being nonlinear due to their switched nature, are well-modelled below $0.5f_{pwm}$, using small-signal averaging techniques [3, 99]. Therefore, it is expected that (5.7) can offer a good prediction when the bandwidth of interest is limited below $0.5f_{pwm}$, where the modulation process is practically linear [3].

However, let us observe the case of a control system with MS-PWM, where an interesting phenomenon takes place. Consider the system shown in Fig. 5.2, where both the controller and the feedback filter are replaced by purely proportional actions. If the feedback signal, which is summed with the band-limited white noise, is oversampled ($N > 2$), the noise floor is pushed down compared to DS-PWM and the PSD of the digital signal m_s is reduced. Nevertheless, the output of the triangular modulator is still determined by only two intersections between m and w. Hence, just two samples of m_s are chosen, i.e re-sampled, by the modulator in order to produce its output x. As the considered control system is purely proportional, this corresponds to using exactly two feedback samples. *Therefore, resulting noise propagation cannot differ from the case of a system that would sample the feedback only twice per switching period.* An illustration of this mechanism is shown in Fig. 5.7. It is clear that, in order to ensure that x is determined based on multiple feedback samples taken inside one modulation period, some filtering action needs to be included in G_{fb} or G_c, making each individual value of m_s dependent on previous feedback samples as well. As it will be shown, this comes down to providing an anti-aliasing function using digital filters, before re-sampling occurs from f_s to $2f_{pwm}$.

The mechanism discussed above points out that the impact of the triangular DPWM on noise propagation may be estimated by modeling it as a decimator of m_s with the decimation factor $M = \frac{f_s}{2f_{pwm}}$.

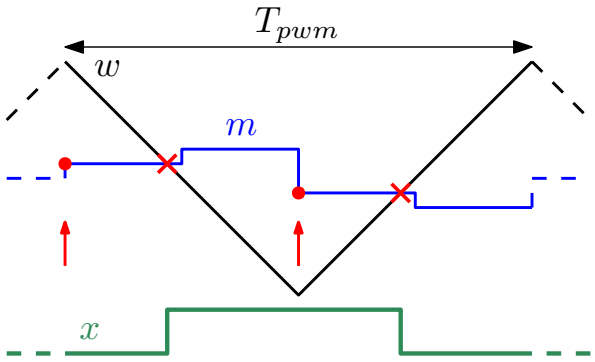


Figure 5.7: Illustration of the triangular DPWM re-sampling its input signal twice per switching period.

The assumed nonlinear impact of the DPWM is examined in simulations, for the current-controlled configuration of the converter shown in Fig. 5.3. Noise propagation is tested for SS-PWM, DS-PWM, and MS-PWM with $N = 4$. As noted in Section 5.3.3, calculating the ratio of frequency components' magnitudes of i_L and n corresponds to finding $|H_n(\omega)|$, assuming a linear system behavior. The expected magnitude responses correspond to $|H_{n,i}(\omega)|$ shown in Fig. 5.5a. Note again that this kind of test cannot be performed experimentally, as noise cannot be sampled independently of the feedback.

The results of these simulations are shown in Fig. 5.8. As can be seen, for $N = 1$ and $N = 2$, the simulated magnitude response is in perfect match with the small-signal prediction. This confirms that the linear analysis in (5.7) is well-suited for predicting noise propagation in systems with (S/D)S-PWM. However, for $N = 4$, when the sampled feedback contains noise components at $f > f_{pwm}$, the simulated magnitude response shows a significant mismatch from the small-signal model. This indicates that converters with MS-PWM exhibit a highly-nonlinear behavior in terms of noise propagation. At this point, based on the mechanisms described above, it is presumed that the reason behind this is that the aliasing of noise spectral components at $f > f_{pwm}$ occurs due to the decimation process introduced by the triangular DPWM. The assumed decimation behavior is supported by experimental tests in Section 5.6, where an excellent match is obtained with the extended analysis from Section 5.5.

The frequency zones of interest are summarized in Fig. 5.9, by comparing a double-sampled system with an N-sampled system. It is assumed that the control system is purely proportional and the impact of the feedback is neglected for the illustration. By oversampling the feedback, white noise spectral power is spread up to $\frac{1}{2}Nf_{pwm}$. This results in the reduction of the PSD compared to the double-sampled case, $s_N = \frac{2}{N}s_2$. The frequency range, in which noise propagation is analyzed, $f < f_x$, is marked as A. The zone B marks the region in which the spectral components are folded back due to the DPWM decimation. Without any digital filtering, aliasing due to the DPWM decimation limits the achievable PSD to the value determined by the double-sampled case. Regarding noise propagation, this can be considered equivalent to the implementation of MR-DS-PWM with the controller output being decimated to $N = 2$, without any prior filtering. In order to achieve the PSD equal to $\frac{s}{N}$ in zone A, spectral components in zone B must be completely filtered-out in the digital domain, prior to entering the DPWM. Hence, calculations using (5.7) are expected to provide valid predictions of noise propagation

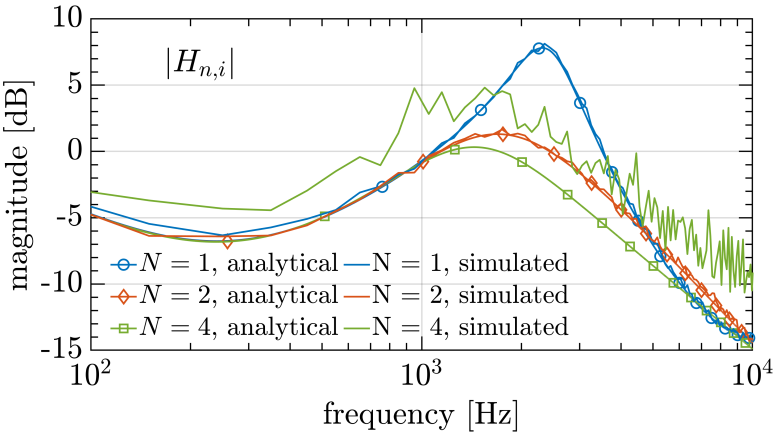


Figure 5.8: Comparison between the simulated magnitude response from n to i_L and $|H_{n,i}|$, for the converter described in Table 3.2 and the PI controller described in Table 5.1. The converter runs at the operating point $D = 0.4$. The acquired data length is equal to 200 ms and the spectrum is averaged over 100 Hz for better visualization. The exact simulation settings are described in Section 5.6.1.

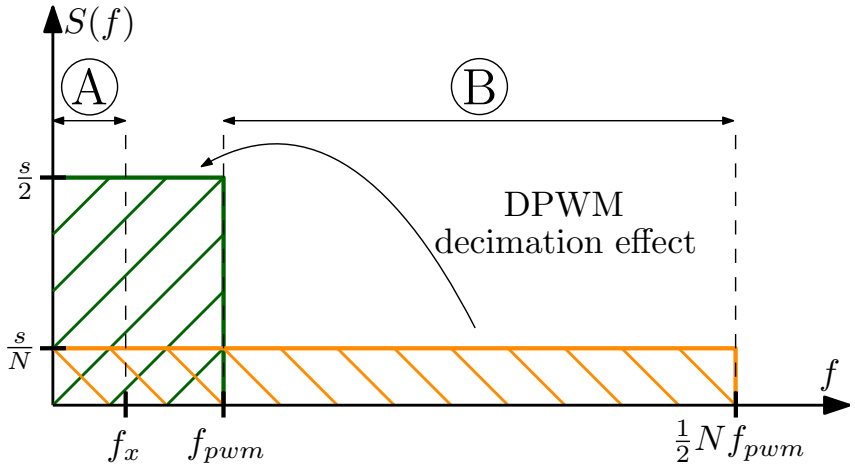


Figure 5.9: Illustration of the oversampling impact on the white noise PSD for the triangular PWM carrier and a purely proportional control system, neglecting the impact of the feedback. Zone A represents the frequency window of interest for noise measurements. Zone B represents the frequency window that must be filtered in digital domain to suppress the DPWM decimation effect.

for MS-PWM only if the entire spectral content in zone B is removed.

In order to reduce the spectral fold-back and make noise propagation properties closer to the ones of (S/D)S-PWM, some digital filtering is required. It is of interest to design these filters such that their impact is low in the control bandwidth, in order to retain a good dynamic performance. Filtering should ideally be limited only to $f > f_{pwm}$. In this way, the spectral aliasing would be reduced and the noise suppressed at frequencies well-below f_{pwm}, where the filter does not have a direct impact. The triangular carrier is already proven to be the most suitable for MS-PWM, with respect to reducing the impact of the discontinuity-related nonlinearities and bringing a constant modulation delay [27]. This section points to another possible advantage. Namely, in case of single-edge modulators, only one sample of m_s per modulation period is used to determine the switching signal; hence, even for $N = 2$ the decimation

occurs. Therefore, anti-aliasing digital filtering should be performed in the region $f > \frac{f_{pwm}}{2}$, which would imply a significant deterioration of the system dynamics.

5.4.2 Qualitative approach to anti-aliasing digital filter design

In this section, digital feedback filters are designed so as to suppress the DPWM decimation effect. The design goal is to provide attenuation of m_s at $f > f_{pwm}$ (zone B in Fig. 5.9), with the least impact on degrading the dynamic performance.

Let us start by analyzing the response from the sampled noise n to the DPWM's input signal m_s, for the system in Fig. 5.2. The corresponding transfer function is:

$$H_{nm}(\omega) = \frac{m_s(\omega)}{n(\omega)} = -\frac{G_{fb}(\omega)G_c(\omega)}{1 + W_{ol}(\omega)}. \tag{5.9}$$

Consider the frequency window in which the DPWM-related aliasing takes place ($f > f_{pwm}$). It is clear that, at such high frequencies, the closed-loop is ineffective, i.e. $|W_{ol}(\omega)| \ll 1$. This allows to simplify the analysis by considering the open-loop structure:

$$H_{nm}(\omega) \approx -G_{fb}(\omega)G_c(\omega). \tag{5.10}$$

From (5.10), it is clear that $G_{fb}(\omega)$ or $G_c(\omega)$ should be designed to attenuate components at $f > f_{pwm}$.

For the current loop with the PI controller, without a feedback filter, the high-frequency gain of $H_{nm_i}(\omega)$ is practically determined by the proportional action. Therefore, a similar decimation impact is expected as that illustrated in Fig. 5.9, i.e. the PSD remaining constant with the increase of N above 2.

For the voltage loop with the PID controller, without a feedback filter, the impact of the decimation is more severe. Due to the derivative action, the gain of $H_{nm_v}(\omega)$ increases with the frequency, with the maximum value being determined by the Nyquist frequency. For this reason, higher values of N increase the total noise power above f_{pwm} and, consequently, also the in-band PSD after the aliasing takes place. For this reason, it is expected that a higher attenuation at $f > f_{pwm}$ is required for control loops that employ the PID, with respect to those with the high-frequency proportional-dominant controllers, e.g. P, PI, or PR.

Considerations above are summarized in Fig. 5.10, by showing results of approximated calculations for the total noise power that gets folded back due to the aliasing. Values are given for the current and voltage controllers from (5.3) and (5.4), without feedback filters. The same assumption as in (5.10) is made, i.e. that $|H_{nm}(\omega)| \approx |G_c(\omega)|$ at $f > f_{pwm}$. The traces in Fig. 5.10 show the numerically integrated squared magnitude responses of H_{nm} in the range $[f_{pwm}, \frac{f_s}{2}]$, normalized by the same frequency range as well as by the results for $N = 4$. This practically corresponds to calculating (5.7) except that the frequency range up to f_{pwm} is neglected so that $|H_{nm}(\omega)| \approx |G_c(\omega)|$ remains valid. From the presented results, it is clear that, for the PI controller, the total noise power that participates in the aliasing practically does not change as the sampling frequency is increased. This result comes from the nearly-

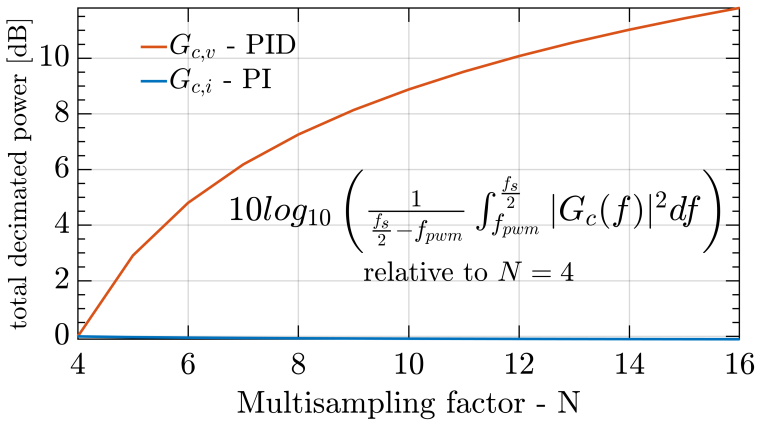


Figure 5.10: Impact of the designed current PI and voltage PID (with the filtered derivative) controllers on the total noise power above f_{pwm}, which participates in the aliasing caused by the DPWM decimation. Controller parameters are equal to those in Table 5.1. The results are given relative to $N = 4$.

.

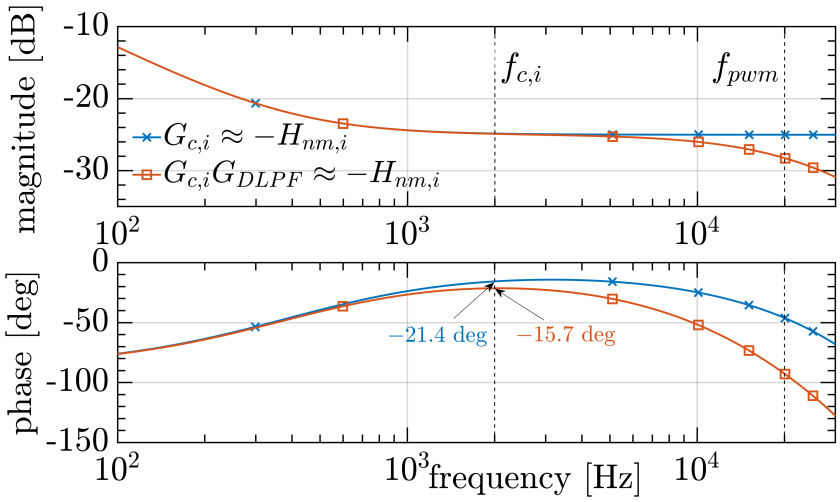
constant high-frequency gain of $G_{c,i}$. On the other hand, for the PID controller, the noise power that gets folded back is strongly amplified as N is increased. It should be again noted that the voltage controller from (5.4) contains also a low-pass filter for the derivative action. Without including such filter, the noise power amplification is significantly higher.

In the following sections, based on the conclusions above, for the PI current controller the suppression of the DPWM decimation effect is tested by introducing a single first-order digital low-pass filter (DLPF) with the cut-off frequency equal to the switching frequency. This filter, labeled as $G_{DLPF}(z)$, is implemented as:

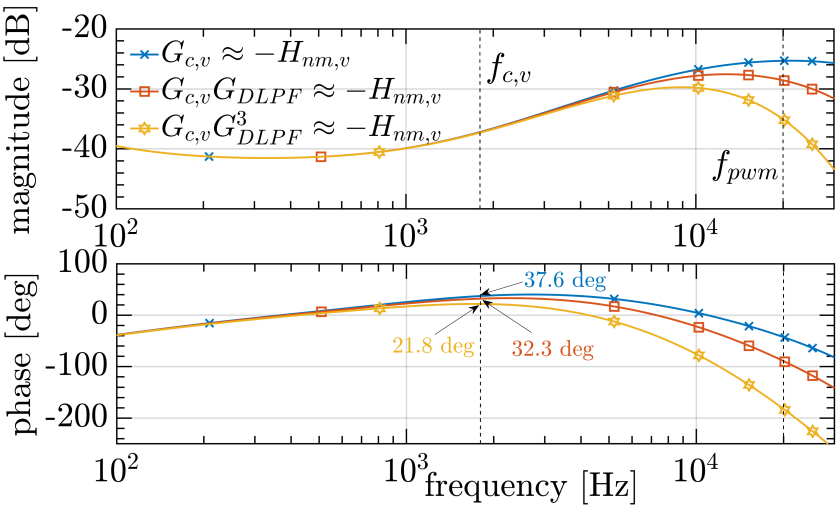
$$G_{DLPF}(z) = a\frac{z+1}{z+b}, \tag{5.11}$$

where $a = \frac{\pi}{\pi+N}$ and $b = \frac{\pi-N}{\pi+N}$. DLPF from (5.11) results in a small impact on the system dynamics as it introduces approximately 6° phase lag at the set crossover frequency $f_{c,i} = 0.1f_{pwm}$. The frequency responses of $H_{nm,i}$, with and without the DLPF, are shown in Fig. 5.11a, given for $N = 8$. For the voltage loop with the PID controller, noise propagation is examined by including the $G_{DLPF}(z)$ from (5.11), and also a third-order filter, equivalent to the cascade of three $G_{DLPF}(z)$, labeled $G^3_{DLPF}(z)$. The filter $G^3_{DLPF}(z)$ introduces approximately 16° phase lag at the crossover frequency of the voltage loop, which results in a non-negligible impact on the dynamic response. The corresponding frequency responses of $H_{nm,v}(\omega)$ are shown in Fig. 5.11b, given for $N = 8$. In the following sections, the aliasing suppression capability of the MAF from (2.9) is tested as well.

Note that, for all following results, digital feedback filters are only used for oversampling factors $N > 2$ as their sole purpose is the suppression of the aliasing effect due to the DPWM decimation, and not the direct attenuation of the spectral content up to f_x.



(a)



(b)

Figure 5.11: Frequency responses of cascades of the controller $G_c(z)$ and the feedback filter $G_{fb}(z)$ for (a) the current loop with the PI controller and (b) the voltage loop with the PID controller. The controller parameters are shown in Table 5.1 and the plots are given for $N = 8$.

5.5 Extended models that include decimation effects

The goal of this section is to derive a better-suited model of noise propagation for systems that feature decimation. The motivating example is the DPWM decimation, which occurs inside the MS-PWM closed-loop system. Another strategy that is covered by this analysis is the case of oversampled filtering followed by the decimation to SS-PWM or DS-PWM (MR-(S/D)S-PWM) [63]. The section starts with the analysis of open-loop systems, which is a simpler case and is used as a building block for the closed-loop analysis. A relevant open-loop scenario is found in an application discussed in Chapter 6.

For all calculations, the noise signal is assumed to be a WSS and Gaussian process. For the final equivalent models, it is also assumed to be band-limited white noise.

5.5.1 Open-loop systems

5.5.1.1 Model derivation

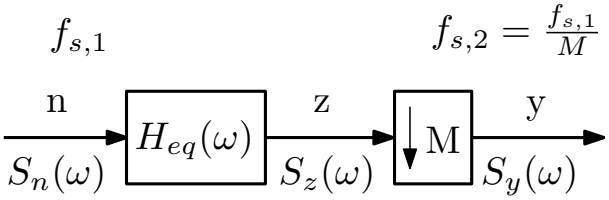


Figure 5.12: Open-loop oversampled filtering, followed by an M-time down-sampler.

Consider an open loop system shown in Fig. 5.12. The input noise signal n, sampled with frequency $f_{s,1}$, is processed by H_{eq}, after which it is decimated to $f_{s,2} = \frac{f_{s,1}}{M}$. In order to quantify noise propagation, it is of interest to find the relation between the PSD of n, $S_n(\omega)$, and the PSD of y, $S_y(\omega)$. Then, the output noise variance, in the frequency range of interest, can be easily calculated by integrating $S_y(\omega)$. Relation between S_z and S_n is found as in (5.5):

$$S_z(\omega) = S_n(\omega)|H_{eq}(\omega)|^2. \tag{5.12}$$

Let us now consider the impact of the decimator, which down-samples the signal z M times to obtain the signal y. From signal processing theory, it is known that the impact of an integer-rate down-sampler on its input signal can be calculated as[2]:

$$y(\omega) = \sum_{k=0}^{M-1} z(\omega - k2\pi f_{s,2}). \tag{5.13}$$

The expression (5.13) represents the spectral folding of the signal $z(\omega)$ and can be used to find the impact of aliasing if $z(\omega)$ contains components above the baseband of the decimator, i.e. $\frac{f_{s,2}}{2}$. However, it cannot be applied directly as complete information on the magnitude and the phase of a stochastic signal $n(\omega)$, and therefore $z(\omega)$ as well, is not available. Let us, for this reason, find the expression[3] for

[2]Note that, when considering the Discrete Fourier Transform (DFT), an additional scaling factor $\frac{1}{M}$ is needed to address the reduced number of samples at the output. However, for all computations shown in this chapter, the scaling is incorporated in the DFT algorithm; hence, it is left out of the following expressions.

[3]What may confuse is that, in (5.14), the first factor should be determined by the sampling frequency of the domain where the signal y is, i.e. $\frac{1}{f_{s,2}}$. However, since the fold-backs of z and z^* both bring a factor of $\frac{1}{M}$, what is left is $\frac{1}{f_{s,2}}\frac{1}{M^2}$. Then, the expression can be manipulated to obtain $\frac{1}{f_{s,1}}\frac{f_{s,1}}{f_{s,2}}\frac{1}{M^2} = \frac{1}{f_{s,1}}M\frac{1}{M^2} = \frac{1}{f_{s,1}}\frac{1}{M}$. The remaining scaling factor $\frac{1}{M}$ is again incorporated in the DFT calculation and is, hence, left out.

the PSD of y:

$$
\begin{aligned}
S_y(\omega) &= \frac{1}{f_{s,1}} y(\omega) y^*(\omega) = \frac{1}{f_{s,1}} \left(\sum_{k=0}^{M-1} z(\omega - k2\pi f_{s,2}) \right) \left(\sum_{l=0}^{M-1} z(\omega - l2\pi f_{s,2}) \right)^* = \\
&= \frac{1}{f_{s,1}} \sum_{\{k,l\}=0}^{M-1} z(\omega - k2\pi f_{s,2}) z^*(\omega - l2\pi f_{s,2}) = \\
&= \frac{1}{f_{s,1}} \sum_{k=0}^{M-1} z(\omega - k2\pi f_{s,2}) z^*(\omega - k2\pi f_{s,2}) + \frac{1}{f_{s,1}} \sum_{\{k,l\}=0, k\neq l}^{M-1} z(\omega - k2\pi f_{s,2}) z^*(\omega - l2\pi f_{s,2}) = \\
&= \sum_{k=0}^{M-1} S_z(\omega - k2\pi f_{s,2}) + \frac{1}{f_{s,1}} \underbrace{\sum_{\{k,l\}=0, k\neq l}^{M-1} z(\omega - k2\pi f_{s,2}) z^*(\omega - l2\pi f_{s,2})}_{=0, \text{ if z is a stationary stochastic signal.}} .
\end{aligned}
\tag{5.14}
$$

It can be seen that the PSD of y can be found using the sum of two contributions. The first one represents the same spectral fold-back as in (5.13) applied directly to the PSD of z, while the second one represents a sum of products between different frequency bands of z. As noted above, it is assumed that n is a sampled WSS and Gaussian process, which also makes it strictly stationary [127]. Linear processing of WSS and Gaussian signals retains these properties, hence, signal z is also strictly stationary [127]. As shown in [129, 130], stationary stochastic signals exhibit no spectral correlation, hence, the second contribution in (5.14) is identically equal to 0, and the PSD of y can be found as:

$$
S_y(\omega) = \sum_{k=0}^{M-1} S_z(\omega - k2\pi f_{s,2}) = \sum_{k=0}^{M-1} S_n(\omega - k2\pi f_{s,2}) |H_{eq}(\omega - k2\pi f_{s,2})|^2. \tag{5.15}
$$

This result is very important, and not trivial, as it allows the fold-back expression to be applied to the *squared magnitudes* of stationary signal's frequency components, in the same way as it would be applied to the signal itself. In this way, only the information on magnitudes (or the PSD) of n is necessary to find the PSD of the down-sampler's output. Additionally, it should be noted that the decimated signal y remains stationary [131]. Finally, as the input signal n is assumed to be band-limited white noise, i.e. its one-sided power spectrum is constant across the bandwidth and equal to $S_n(\omega) = S_n = \frac{2}{f_{s,1}} \sigma_n^2$ [127], the PSD of n can be factored outside of the sum in (5.15), which yields the following expression:

$$
S_y(\omega) = S_n \sum_{k=0}^{M-1} |H_{eq}(\omega - k2\pi f_{s,2})|^2 = \frac{2}{f_{s,1}} \sigma_n^2 |H_{eq}^{M:1}(\omega)|^2. \tag{5.16}
$$

The steps above allow us to analyze noise propagation in the system shown in Fig. 5.12 using its equivalent representation in Fig. 5.13. It is important to note that this equivalent squared magnitude response $|H_{eq}^{M:1}(\omega)|^2$ is only valid for the analysis of the WSS Gaussian white noise and should not be misunderstood as being applicable to any input signal. For a stationary input noise with the frequency-dependent PSD, (5.15) must be used instead. Finally, if the noise is not stationary, both terms from the last row of (5.14) must be used.

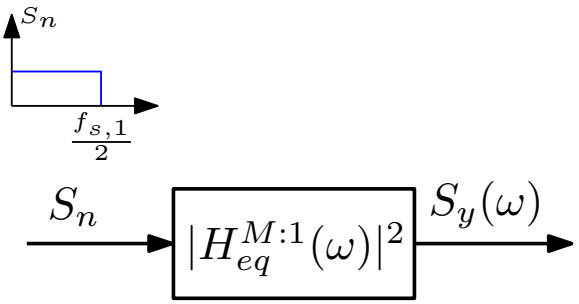


Figure 5.13: Equivalent system to the one in Fig. 5.12, valid for noise propagation analysis in case of a WSS Gaussian white noise input.

5.5.1.2 Validation in simulations

To verify the derived model, a few examples of estimating S_y are given, for several different filters H_{eq} discretized with $T_{s,1} = \frac{1}{f_{s,1}} = \frac{1}{Mf_{s,2}}$. The decimation is performed with frequency $f_{s,2} = 2f_{pwm} = 40$ kHz, to correspond to the hardware set-up used in this chapter. The tested filters are:

- Derivative filter, $H_{eq,1}(z) = \frac{k_{ad}}{T_{s,1}}\left(1 - z^{-1}\right)$, with the gain $k_{ad} = 1.52 \cdot 10^{-5}$. The exact derivative gain is not important, however, in Section 6.6 this specific value is used in an active damping control scheme, for which the noise sensitivity is examined.
- Proportional gain with $k_{p,i}$ from Table 5.1, $H_{eq,2}(z) = k_{p,i}$.
- Cascade of the same proportional gain as above and the DLPF from (5.11), $H_{eq,3}(z) = k_{p,i}G_{DLPF}(z)$.
- PID structure used as the voltage controller in (5.4) with the parameters from Table 5.1, $H_{eq,4}(z) = G_{c,v}(z)$.
- Cascade of the same PID structure as above and 3 DLPFs from (5.11), $H_{eq,5}(z) = G_{c,v}(z)G_{DLPF}^3(z)$.

The simulation model, corresponding to Fig. 5.12, is implemented in MATLAB/Simulink, where n is obtained from a band-limited white noise generator. The noise variance is arbitrarily chosen as $\sigma_n^2 = 150 \cdot 10^{-3}$. The output signal y is acquired with $T_{s,2} = \frac{1}{f_{s,2}}$ with data length of 200 ms, which yielded a 5 Hz spectral resolution. Results are given for $M \in \{1, 2, 4, 8, 16\}$. Note that, the filters $G_{DLPF}(z)$ and $G_{DLPF}^3(z)$ are left out for $M = 1$ as it was only of interest to test their impact on the aliasing, which occurs for $M > 1$. MATLAB is used for postprocessing of simulation results, by calculating the output PSD and the total output noise power. For a better visualization, the PSD is filtered using a MAF with 100 Hz window and is plotted with a thinner line compared to analytical results. For comparison with the analytical predictions, the PSD is scaled with the input variance σ_n^2 such that the relative output noise power corresponds to the area below the given traces. The analytical traces are, correspondingly, calculated as $\frac{S_y(\omega)}{\sigma_n^2} = \frac{2}{f_{s,1}}|H_{eq}^{M:1}(\omega)|^2$ (see (5.16)). The relative output noise power is calculated as the integral of the scaled PSD from 200 Hz to $f_x = 10$ kHz. Lower frequencies are not considered due to the finite spectral resolution of the simulated PSD. Results of the output noise power are shown scaled with the result for $M = 1$, i.e. the case without the decimation occurring.

First, in Fig. 5.14, the results are shown for the case of the derivative filter $H_{eq,1}(z) = \frac{k_{ad}}{T_{s,1}}\left(1 - z^{-1}\right)$. It can be seen that, as M is increased, the PSD flattens out and increases as well, which results in the output noise power amplification. The second result, for the purely proportional gain $H_{eq,2}(z) = k_{p,i}$, is shown in Fig. 5.15. The PSDs perfectly overlap for all values of M, meaning that there is no impact of increasing $f_{s,1}$ above $f_{s,2}$, which is consistent with the illustration from Fig. 5.9. The third result, shown in Fig. 5.16, shows the impact of introducing the DLPF from (5.11) in the cascade with the same proportional gain from above, in order to suppress the aliasing effect, $H_{eq,3}(z) = k_{p,i}G_{DLPF}(z)$. It can be seen that the output noise power is now strongly reduced by increasing the value of M. This result provides additional motivation for introducing the DLPF in the subsequent experimental tests; however, this model does not consider the impact of the closed-loop, which is addressed in the following section. The fourth result, shown in Fig. 5.17, shows the propagation for the PID structure (with the filtered derivative action) from (5.4), $H_{eq,4}(z) = G_{c,v}(z)$. It can be seen that, except for $M = 2$, the output noise power is amplified. Finally, for the same PID structure, results in Fig. 5.18 show that the output noise power is strongly suppressed by introducing a cascade of 3 DLPFs from (5.11), $H_{eq,5}(z) = G_{c,v}(z)G^3_{DLPF}(z)$. For all cases shown, the match between the simulations and the analytical results is practically perfect, which validates the derived model for open-loop systems.

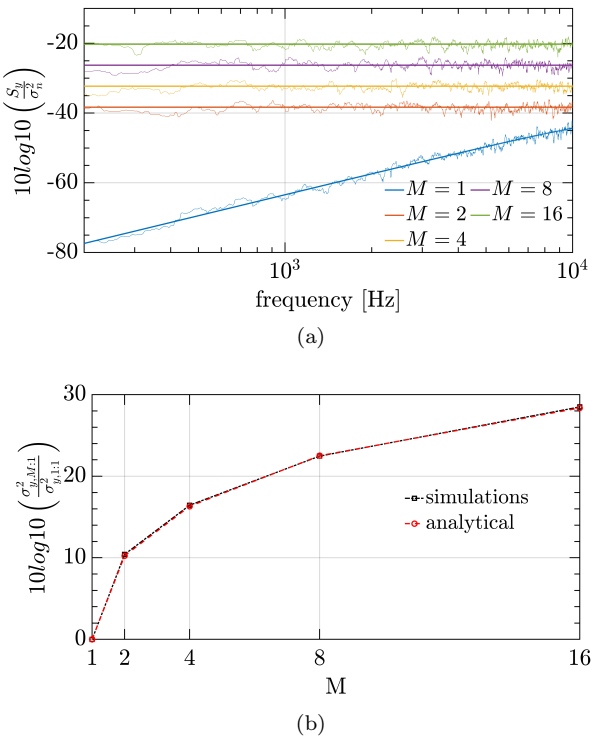


Figure 5.14: Impact of the open-loop decimation for the derivative filter, $H_{eq,1}(z) = \frac{k_{ad}}{T_{s,1}}\left(1 - z^{-1}\right)$: (a) the PSD relative to the input noise variance; (b) the output variance up to $\frac{f_{pwm}}{2} = 10$ kHz, relative to the result for $M = 1$.

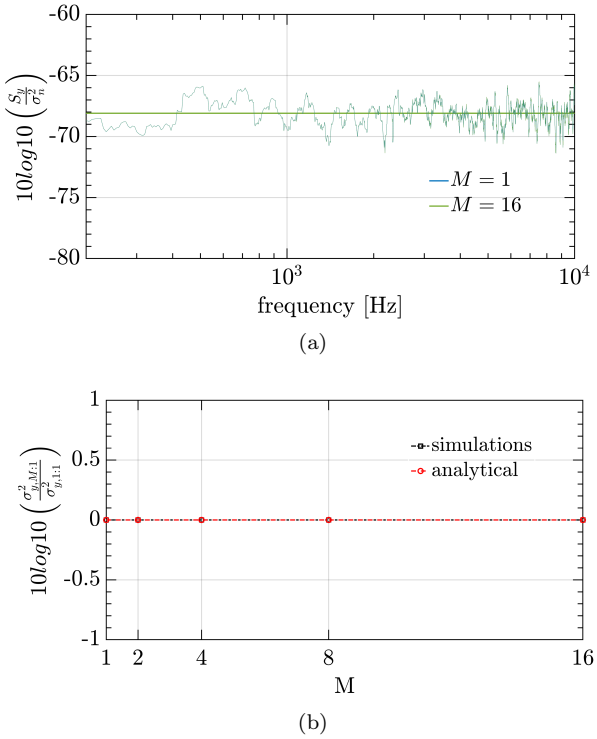


Figure 5.15: Impact of the open-loop decimation for the proportional gain, $H_{eq,2}(z) = k_{p,i}$: (a) the PSD relative to the input noise variance; (b) the output variance up to $\frac{f_{pwm}}{2} = 10$ kHz, relative to the result for $M = 1$.

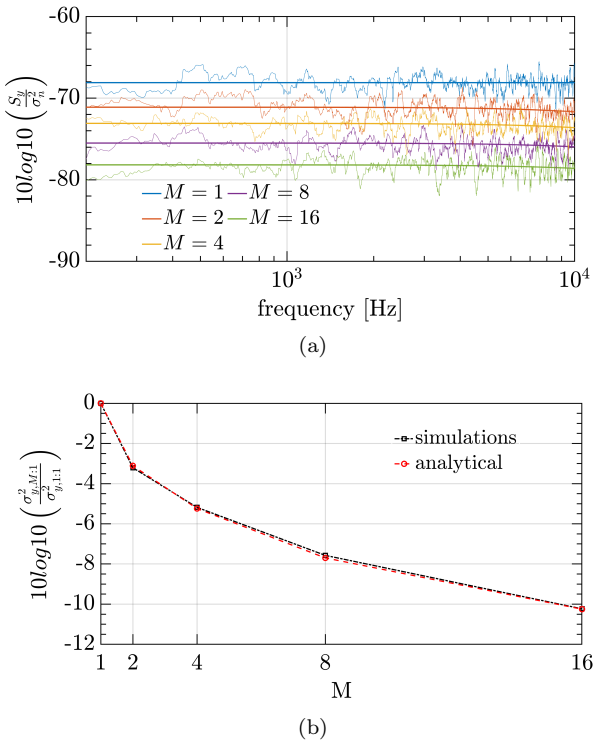


Figure 5.16: Impact of the open-loop decimation for the proportional gain and the DLPF from (5.11), $H_{eq,3} = k_{p,i}G_{DLPF}(z)$: (a) the PSD relative to the input noise variance; (b) the output variance up to $\frac{f_{pwm}}{2} = 10$ kHz, relative to the result for $M = 1$.

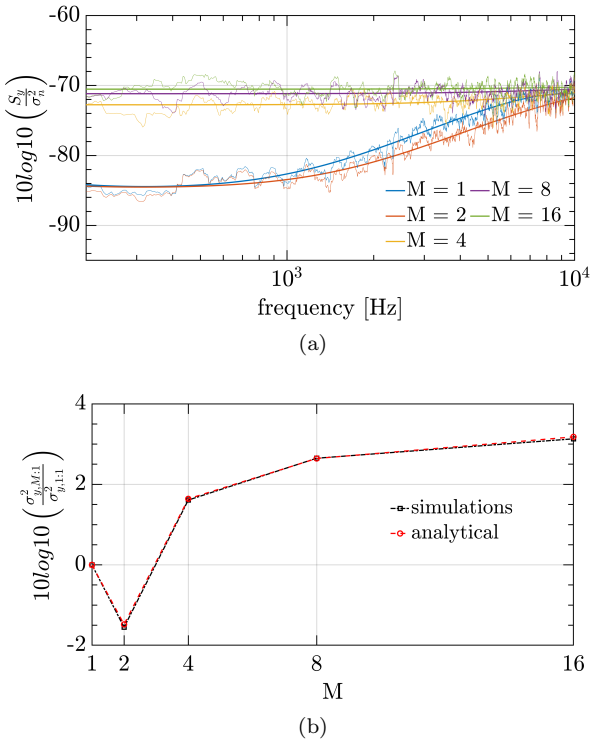


Figure 5.17: Impact of the open-loop decimation for the PID structure from (5.4), $H_{eq,4}(z) = G_{c,v}(z)$: (a) the PSD relative to the input noise variance; (b) the output variance up to $\frac{f_{pwm}}{2} = 10$ kHz, relative to the result for $M = 1$.

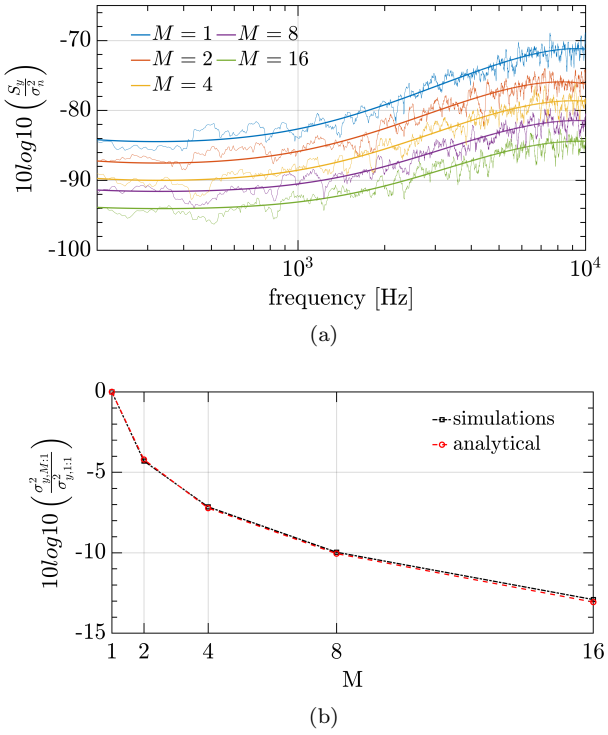


Figure 5.18: Impact of the open-loop decimation for the PID structure from (5.4) and the cascade of 3 DLPFs from (5.11), $H_{eq,5}(z) = G_{c,v}(z)G_{DLPF}^3(z)$: (a) the PSD relative to the input noise variance; (b) the output variance up to $\frac{f_{pwm}}{2} = 10$ kHz, relative to the result for $M = 1$.

5.5.2 Closed-loop systems

In this section, the case of decimation occurring inside a closed-loop system is analyzed. This case is of interest for modeling the DPWM decimation effects explained in Section 5.4. Additionally, it is directly applicable to the widely used control strategy in power electronics, where the feedback is oversampled, filtered, and then decimated to a lower control update rate, i.e. the MR-(S/D)S-PWM control [63, 110, 111]. Although being a very common choice in industrial applications, no simple and effective analysis is present in the literature to model the impact of such system on noise propagation.

5.5.2.1 Model derivation

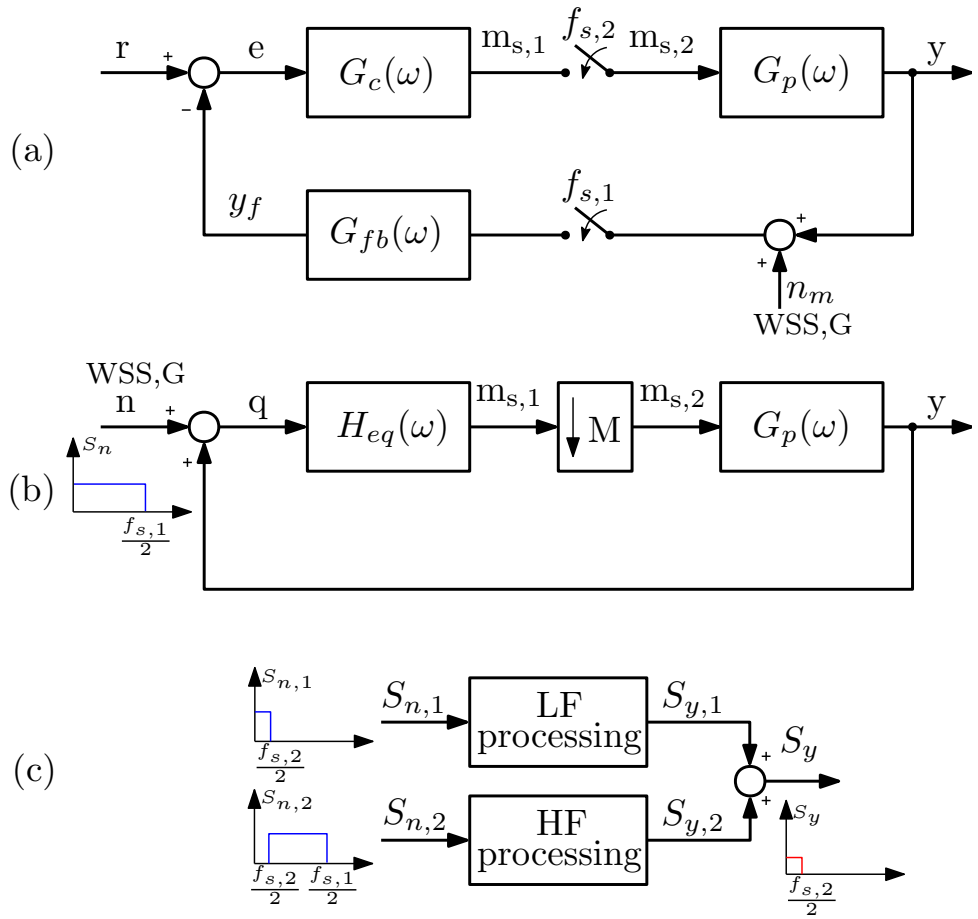


Figure 5.19: Closed-loop system with a multi-rate structure: (a) reference tracking system of interest; (b) simplified system focused on noise propagation; (c) equivalent system used for calculating the output PSD, where the input noise is represented as a sum of two uncorrelated WSS and Gaussian processes.

Let us consider a closed-loop reference tracking system with a band-limited white measurement noise n_m being added to the feedback, as shown in Fig. 5.19a. The feedback is oversampled with frequency $f_{s,1} = Mf_{s,2}$ and processed by a filter $G_{fb}(z)$. In case of MR-DS-PWM, the decimation to the control rate $f_{s,2}$ occurs after $G_{fb}(z)$. In case of MS-PWM, which is illustrated in Fig. 5.19a, the filtered feedback is subtracted from the reference r and processed by the controller $G_c(z)$, all with frequency $f_{s,1}$. Then,

the DPWM itself down-samples its input with frequency $f_{s,2} = 2f_{pwm}$. The DPWM output is processed by the plant filter G_p. Note again that the DPWM has an intrinsic ZOH action, meaning that its output is not actually in the discrete time domain with frequency $f_{s,2}$, but rather in the continuous time domain. It is assumed that the frequency response of G_p correctly incorporates the modulation effects, as described before. Therefore, the analyzed system features 3 domains: the oversampled domain with $f_{s,1}$, the downsampled DPWM domain with $f_{s,2}$, and the continuous time domain[4]. As explained before, the bandwidth of interest for noise propagation analysis is set below f_{pwm}, to be applicable for converter models obtained using the state-space averaging and also to avoid problems related to PSD measurements at frequencies where the switching ripple dominates the spectra.

To simplify the analyzed system, the following steps are taken. First of all, considering that n_m is uncorrelated to the feedback y, the sampler $f_{s,1}$ can be applied independently to y and n_m, resulting in the sampled WSS Gaussian process n being the same as analyzed for the open-loop case. Next, it is assumed that the closed-loop system has a low-pass nature, owing to the filtering characteristic of G_p, which is determined by the output filter of the converter. Low-pass filtering nature of G_p is the main simplifying assumption, as it implies that the impact of noise on the output signal y is band-limited well-below $f_{pwm} = \frac{f_{s,2}}{2}$. Hence, the Nyquist frequency of the sampler $f_{s,1}$ is always above the bandwidth of the signal y and, therefore, the spectrum of its sampled output is equal to the one of y in the frequency range of interest. This allows for the simplification of the system, such that the sampler $f_{s,1}$ is completely neglected and the only considered rate change is the decimation between the controller and the plant. Fig. 5.19b shows the simplified system, considering only noise propagation ($r = 0$) and merging together the filter and the controller, such that $H_{eq}(\omega) = -G_{fb}(\omega)G_c(\omega)$.

As the discrete input noise signal is band-limited up to $\frac{f_{s,1}}{2}$, its propagation cannot be analyzed directly, without incorporating effects of the down-sampler M. Let us again use the important fact that the noise is assumed to be a stationary signal, hence it exhibits no spectral correlation. This allows us to partially process n across its bandwidth. For this purpose, n is represented as a sum of two signals, n_1 and n_2, with the following PSDs:

$$
\begin{aligned}
S_{n,1} &= \begin{cases} S_n = \frac{2}{f_{s,1}}\sigma_n^2, & \text{if } f < \frac{f_{s,2}}{2} \\ 0, & \text{if } \frac{f_{s,2}}{2} < f < \frac{f_{s,1}}{2} \end{cases} \\
S_{n,2} &= \begin{cases} 0, & \text{if } f < \frac{f_{s,2}}{2} \\ S_n = \frac{2}{f_{s,1}}\sigma_n^2, & \text{if } \frac{f_{s,2}}{2} < f < \frac{f_{s,1}}{2} \end{cases}
\end{aligned}
\tag{5.17}
$$

Given that n_1 and n_2 exhibit no cross-correlation, after being processed by the closed-loop system, the resulting output signals y_1 and y_2 remain uncorrelated. Hence, the total output PSD can be found as an algebraic sum of the two PSDs, $S_{y,1}$ and $S_{y,2}$, corresponding to y_1 and y_2, respectively. This is illustrated in Fig. 5.19c. As noted above, for all PSD calculations, the spectral region of interest[5] is

[4] This is also illustrated in Fig. 5.1, where $f_{s,1} = f_s$ and $f_{s,2} = 2f_{pwm}$.

[5] All subsequently derived PSD expressions are valid only in the range $f \in \left(0, \frac{f_{s,2}}{2}\right)$, which, for clarity, is left out of the expressions.

below $\frac{f_{s,2}}{2}$.

Let us first consider the case of n_1. This signal is purposely chosen to be limited exactly by the Nyquist frequency of the down-sampler M, $\frac{f_{s,2}}{2}$, meaning that it does not cause any spectral fold-back. Let us define the open-loop transfer function, neglecting the decimator, as:

$$W_{ol,n}(\omega) = H_{eq}(\omega)G_p(\omega). \tag{5.18}$$

The propagation of n_1 is trivial to analyze as it corresponds to the linear processing by a single-rate closed-loop system with the open-loop transfer function from (5.18):

$$S_{y,1}(\omega) = S_{n,1}(\omega)\frac{|W_{ol,n}(\omega)|^2}{|1 - W_{ol,n}(\omega)|^2} = S_n\frac{|W_{ol,n}(\omega)|^2}{|1 - W_{ol,n}(\omega)|^2}. \tag{5.19}$$

Note that the negative sign is incorporated in H_{eq} to correspond to the system shown in Fig. 5.19a.

The high-frequency part is more challenging for the analysis. Let us consider the same closed-loop system from Fig. 5.19b, where the signal indices will be labeled with 2, to indicate that the analysis refers to the high-frequency noise signal n_2. It can be seen that the signal q_2 is equal to $q_2 = n_2 + y_2$. Although n_2 is found in the frequency range $\left(\frac{f_{s,2}}{2}, \frac{f_{s,1}}{2}\right)$, after being processed by H_{eq} and down-sampled M times, the PSD of the digital signal $m_{s,2,2}$ is folded back below $\frac{f_{s,2}}{2}$. Based on the above-mentioned low-pass assumption of G_p, it is concluded that the signal y_2 remains band-limited below $\frac{f_{s,2}}{2}$ even after the inherent holder action performs the conversion to the continuous time domain. This crucial assumption allows us to claim that the signal q_2 is completely determined by n_2 above $\frac{f_{s,2}}{2}$ and by y_2 below $\frac{f_{s,2}}{2}$. To propagate the signal q_2 to the output y_2, spectral fold-back needs to be applied only to the part above $\frac{f_{s,2}}{2}$, which results in:

$$\begin{aligned} y_2(\omega) &= G_p(\omega)\sum_{k=0}^{M-1} n_2(\omega - k2\pi f_{s,2})H_{eq}(\omega - k2\pi f_{s,2}) + W_{ol,n}(\omega)y_2(\omega) = \\ &= \frac{G_p(\omega)}{1 - W_{ol,n}(\omega)}\sum_{k=0}^{M-1} n_2(\omega - k2\pi f_{s,2})H_{eq}(\omega - k2\pi f_{s,2}). \end{aligned} \tag{5.20}$$

Let us now find the PSD of y_2 in the same way as for the open-loop system in (5.14), again using the fact that stationary signals exhibit no spectral correlation:

$$\begin{aligned} &S_{y,2}(\omega) = \frac{1}{f_{s,1}}y_2(\omega)y_2^*(\omega) = \\ &= \frac{1}{f_{s,1}}\frac{|G_p(\omega)|^2}{|1 - W_{ol,n}(\omega)|^2}\left(\sum_{k=0}^{M-1} n_2(\omega - k2\pi f_{s,2})H_{eq}(\omega - k2\pi f_{s,2})\right)\left(\sum_{l=0}^{M-1} n_2^*(\omega - l2\pi f_{s,2})H_{eq}^*(\omega - l2\pi f_{s,2})\right) = \\ &= \frac{|G_p(\omega)|^2}{|1 - W_{ol,n}(\omega)|^2}\sum_{k=0}^{M-1} S_{n,2}(\omega - k2\pi f_{s,2})|H_{eq}(\omega - k2\pi f_{s,2})|^2 = \\ &= S_n\frac{|G_p(\omega)|^2}{|1 - W_{ol,n}(\omega)|^2}\sum_{k=1}^{M-1} |H_{eq}(\omega - k2\pi f_{s,2})|^2. \end{aligned} \tag{5.21}$$

Note that in the last row of (5.21) the baseband is missing as $S_{n,2} = 0$ for $k = 0$ (see (5.17)). Nevertheless, the expression (5.21) is exactly valid in the range $f \in \left(0, \frac{f_{s,2}}{2}\right)$, due to the spectral fold-back.

Summing $S_{y,1}$ and $S_{y,2}$, the total output PSD is found as:

$$\begin{aligned}
&S_y(\omega) = S_{y,1}(\omega) + S_{y,2}(\omega) = \\
&= S_n \frac{|W_{ol,n}(\omega)|^2}{|1 - W_{ol,n}(\omega)|^2} + S_n \frac{|G_p(\omega)|^2}{|1 - W_{ol,n}(\omega)|^2} \sum_{k=1}^{M-1} |H_{eq}(\omega - k2\pi f_{s,2})|^2 = \\
&= S_n \frac{1}{|1 - W_{ol,n}(\omega)|^2} \left(|H_{eq}(\omega)|^2 |G_p(\omega)|^2 + |G_p(\omega)|^2 \sum_{k=1}^{M-1} |H_{eq}(\omega - k2\pi f_{s,2})|^2 \right) = \\
&= S_n \frac{|G_p(\omega)|^2}{|1 - W_{ol,n}(\omega)|^2} \sum_{k=0}^{M-1} |H_{eq}(\omega - k2\pi f_{s,2})|^2 = \\
&= \frac{2}{f_{s,1}} \sigma_n^2 \frac{|G_p(\omega)|^2}{|1 - W_{ol,n}(\omega)|^2} |H_{eq}^{M:1}(\omega)|^2.
\end{aligned} \tag{5.22}$$

Note that this corresponds to using the same equivalent magnitude response (applied to transfer functions between the sampled noise and the decimator) as derived for the open-loop system, only in the forward path, while the feedback impact is determined by the loop without the rate change. This result is important as it allows to use just the magnitude response for the spectral fold-back, while the feedback still incorporates the phase response of the system, which impacts the filtering performance of the closed-loop structure.

A block diagram corresponding to (5.22) is shown in Fig. 5.20. The block $|\mathrm{CL}(\omega)|^2$ represents the squared magnitude response of a loop that comprises the single-rate open-loop transfer function $W_{ol,n}$ from (5.18) in its feedback. In case of MS-PWM, H_{eq} includes the filter and the controller, while in the case of MR-(S/D)S-PWM it includes only the filter (the controller would be placed in the cascade with G_p). Another difference between MS-PWM and MR-(S/D)S-PWM is in the frequency response of G_p, which needs to include the appropriate DPWM small-signal model from (2.3). In general terms, H_{eq} consists of all oversampled blocks, i.e. those found between the samplers $f_{s,1}$ and $f_{s,2}$ in Fig. 5.19a. The system in Fig. 5.20 is only valid for a low-pass plant and a WSS Gaussian white noise input. For other input noise properties, the analysis cannot be simplified to this form.

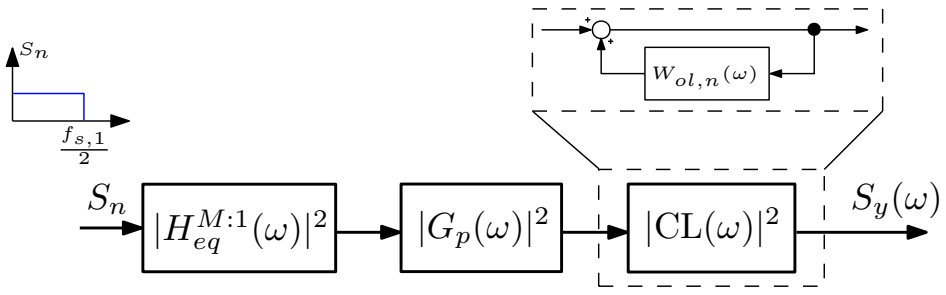


Figure 5.20: Equivalent system to the one in Fig. 5.19a, valid for noise propagation analysis in case of a low-pass G_p and a WSS Gaussian white noise input.

5.5.2.2 Validation in simulations

Same as for the open-loop case, simulations are used to verify the derived noise propagation model. The simulated model is implemented to completely correspond to Fig. 5.19a, with the reference being set to 0. The oversampled period is set as $T_{s,1} = \frac{1}{f_{s,1}} = \frac{1}{Mf_{s,2}}$, while the decimation rate is set as $f_{s,2} = 2f_{pwm} = 40$ kHz, to correspond to the set-up used in this chapter. Relative output noise power is again found in the range from 200 Hz to $\frac{f_{pwm}}{2} = 10$ kHz. The plant transfer function is simulated in the continuous time domain, while the ZOH is included after the re-sampler $f_{s,2}$. Therefore, the simulated system features 3 domains, just like discussed before.

The tested controllers, filters, and plant transfer functions, with the parameters from Tables 3.2 and 5.1 are:

- Current loop with $G_{p,i}$ from (5.1), PI controller from (5.3), without any feedback filter.
- Current loop with $G_{p,i}$ from (5.1), PI controller from (5.3), with the DLPF from (5.11).
- Voltage loop with $G_{p,v}$ from (5.2), PID controller from (5.4), without any feedback filter.
- Voltage loop with $G_{p,v}$ from (5.2), PID controller from (5.4), with the DLPF from (5.11).
- Voltage loop with $G_{p,v}$ from (5.2), PID controller from (5.4), with 3 DLPFs from (5.11).
- Voltage loop with $G_{p,v}$ from (5.2), PID controller from (5.4), with MAF from (2.9).

The controllers are implemented without one step computation delay. As before, G_{fb} is only used for $M > 1$, to verify its impact on suppressing the aliasing.

The results are shown in Figs. 5.21 - 5.26. Again, the simulations show an excellent match with the analytical results, which validates the derived model. Trends related to the impact of adding the feedback filters are similar to those for the before-tested open-loop systems.

To conclude, the expression (5.22), derived in this section, can be used to replace the qualitative approach from Section 5.4.2 in designing the anti-aliasing digital low-pass filters needed to suppress the impact of the decimation on noise propagation.

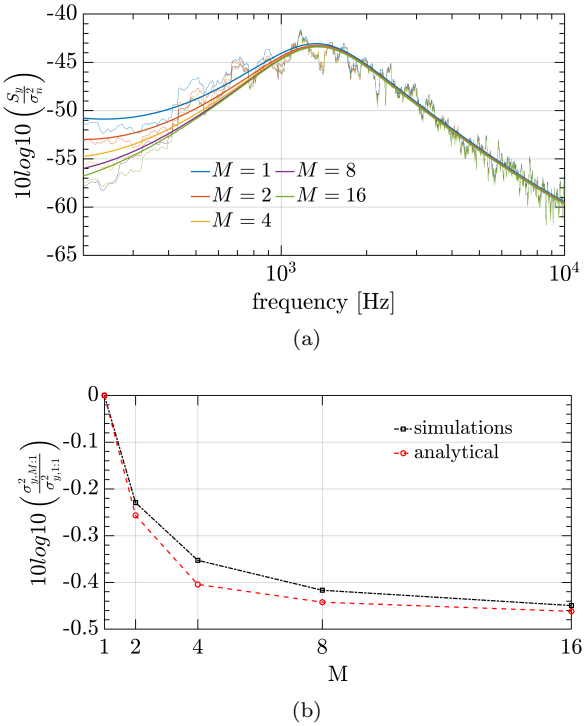


Figure 5.21: Impact of the closed-loop decimation for $G_c = k_{p,i} + k_{i,i}T_s\frac{1}{1-z^{-1}}$, $G_{fb} = 1$, G_p from (5.1), with parameters from Tables 3.2 and 5.1: (a) the PSD relative to the input noise variance; (b) the output variance up to $\frac{f_{pwm}}{2} = 10$ kHz, relative to the result for $M = 1$.

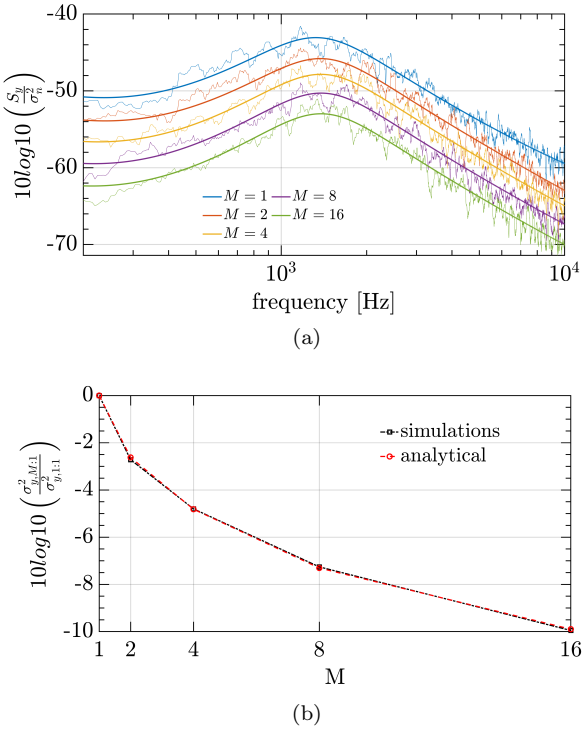


Figure 5.22: Impact of the closed-loop decimation for $G_c = k_{p,i} + k_{i,i}T_s\frac{1}{1-z^{-1}}$, G_{fb} is the DLPF from (5.11), G_p from (5.1): (a) the PSD relative to the input noise variance; (b) the output variance up to $\frac{f_{pwm}}{2} = 10$ kHz, relative to the result for $M = 1$.

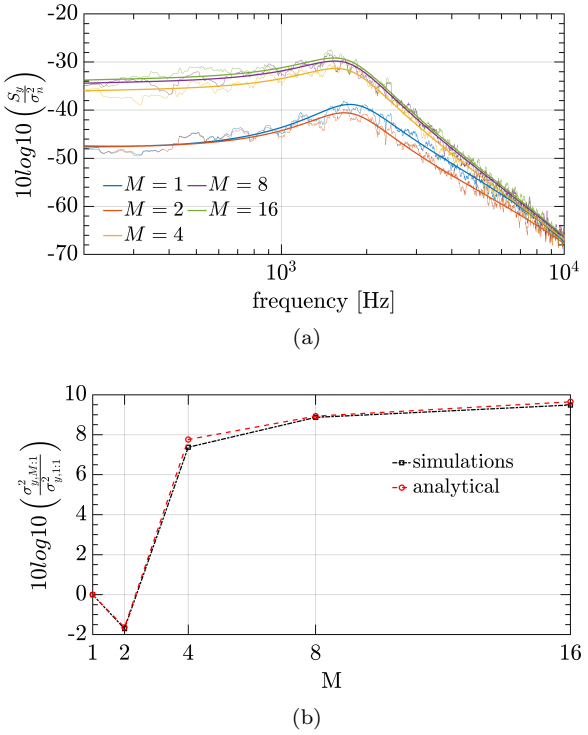


Figure 5.23: Impact of the closed-loop decimation for $G_c = k_{p,v} + k_{i,v}T_s\frac{1}{1-z^{-1}} + \frac{k_d}{T_s}(1-z^{-1})G_{df}(z)$, $G_{fb} = 1$, G_p from (5.2): (a) the PSD relative to the input noise variance; (b) the output variance up to $\frac{f_{pwm}}{2} = 10$ kHz, relative to the result for $M = 1$.

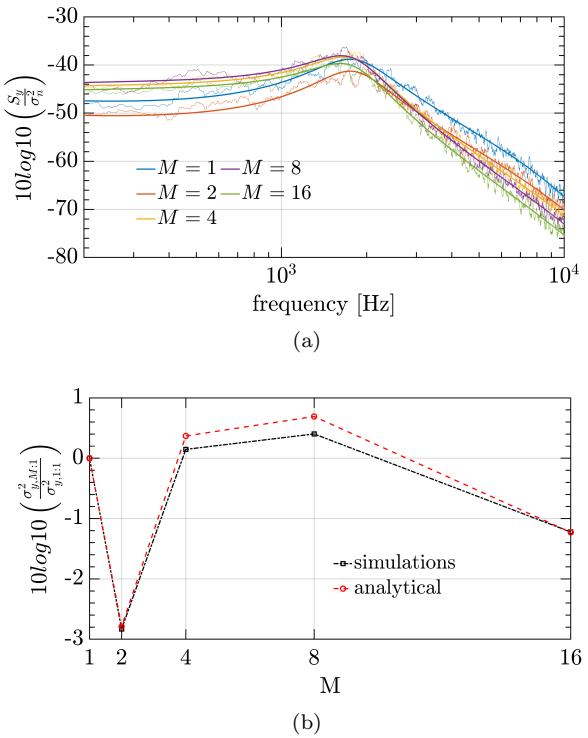
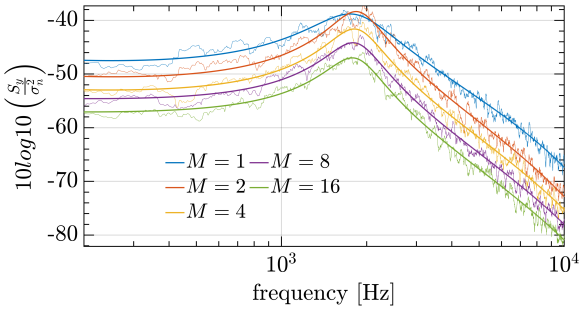
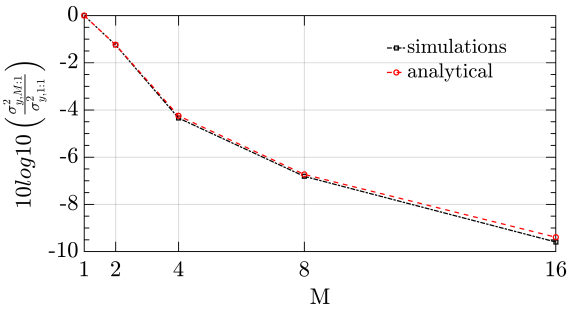


Figure 5.24: Impact of the closed-loop decimation for $G_c = k_{p,v} + k_{i,v}T_s\frac{1}{1-z^{-1}} + \frac{k_d}{T_s}(1-z^{-1})G_{df}(z)$, G_{fb} is the DLPF from (5.11), G_p from (5.2): (a) the PSD relative to the input noise variance; (b) the output variance up to $\frac{f_{pwm}}{2} = 10$ kHz, relative to the result for $M = 1$.

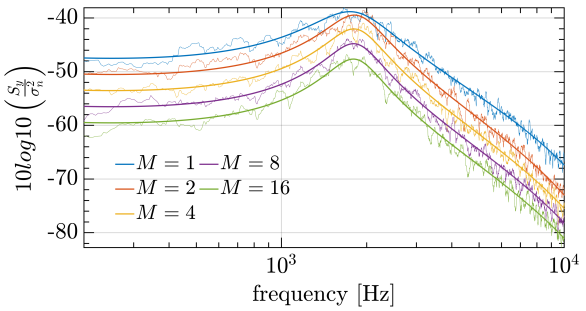


(a)

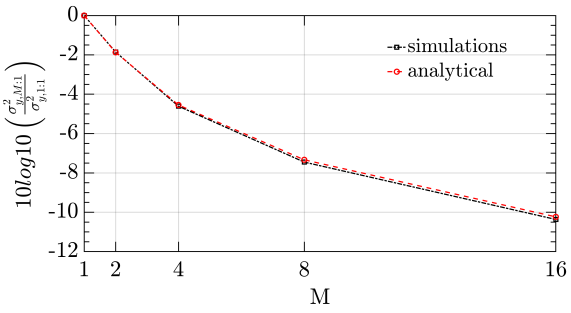


(b)

Figure 5.25: Impact of the closed-loop decimation for $G_c = k_{p,v} + k_{i,v}T_s\frac{1}{1-z^{-1}} + \frac{k_d}{T_s}(1-z^{-1})G_{df}(z)$, G_{fb} is a cascade of 3 DLPFs from (5.11), G_p from (5.2): (a) the PSD relative to the input noise variance; (b) the output variance up to $\frac{f_{pwm}}{2} = 10$ kHz, relative to the result for $M = 1$.



(a)



(b)

Figure 5.26: Impact of the closed-loop decimation for $G_c = k_{p,v} + k_{i,v}T_s\frac{1}{1-z^{-1}} + \frac{k_d}{T_s}(1-z^{-1})G_{df}(z)$, G_{fb} is the MAF from (2.9), G_p from (5.2): (a) the PSD relative to the input noise variance; (b) the output variance up to $\frac{f_{pwm}}{2} = 10$ kHz, relative to the result for $M = 1$.

5.6 Experimental verification of noise propagation

Noise propagation properties are verified experimentally on the buck-type converter, described in Section 5.2.1. Hardware parameters are equal to those in Table 3.2 and the controller parameters are equal to those in Table 5.1.

The control system is implemented on the FPGA platform, described in Section 3.2. The 12-bit ADC quantization in the experimental set-up corresponds to $LSB_i = 17$ mA for the current loop, and $LSB_v = 75$ mV for the voltage loop.

For postprocessing, 50 ms of data is acquired with a 250 MS/s rate, using the high-resolution mode (15 bits) of Tektronix MS056 oscilloscope with channel bandwidths set to 20 MHz. The inductor current is sensed using Tektronix TCP202 current probe, and the capacitor voltage is sensed using ROHDE & SCHWARZ RT-ZD01 differential voltage probe, with the attenuation set to 100. Signal offsets and scales that result in the maximal resolution are set on the oscilloscope.

Measurements are conducted for steady-state duty cycles equal to $D = [0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8]$. To avoid overcrowding the figures, for all tested operating points, the analytical results use the DPWM model from (2.3) with only $D = 0.5$, as its operating point dependency was verified to have a small impact in the frequency range of interest. By covering a wide range of operating points, the sensitivity of noise propagation properties can be examined. This is important as in experimental prototypes certain amount of switching noise is always present. All presented measurements were repeated multiple times, in order to verify that they do not significantly vary from one measurement to another. The input voltage for the voltage loop tests is set to $V_{in} = 160$ V, so that the voltage probe attenuation would not have to be changed to 1000, which would increase the noise resulting from the oscilloscope itself. For the current loop tests, the input voltage is set to $V_{in} = 200$ V. The upper frequency limit for the variance calculation is arbitrarily chosen as $f_x = 0.4 f_{pwm} = 8$ kHz.

The input noise powers, corresponding to i_L and v_c measurements, are estimated in the following way. The converter is set to run in an open-loop condition and the feedback is sampled once per switching period, for the total length of 50 ms. In this way, both impacts of the closed-loop and the switching harmonics are removed and the input noise power is estimated from the spectral content of the sampled signal. These measurements were repeated and averaged across the tested operating points. The resulting values of the input noise powers are $\sigma^2_{n,i} = 1.7 \cdot 10^{-3}$ A^2 and $\sigma^2_{n,v} = 154 \cdot 10^{-3}$ V^2. These values are significantly higher than the quantization noise powers, determined by $\frac{\mathrm{LSB}^2_{\mathrm{i,v}}}{12}$ [3]. For all tests in this section, the results are given relative to the lowest tested value of N; hence, the information on the input noise power is not used. However, it is used in Section 6.6, where absolute values of the output noise power are given.

Two switching periods of i_L and v_c are shown in Fig. 5.27, for the highest possible sampling rate of the oscilloscope, without bandwidth limitations on the input channels. The presence of the switching noise is clearly seen, and its magnitude compared to the switching ripple component is much higher in the capacitor voltage than in the inductor current. In order to verify that the spikes are an actual

differential voltage across the capacitor terminals, both leads of the probe were connected to the negative capacitor terminal. This ground voltage measurement is also shown in Fig. 5.27 as v_g and it can be seen that its value is negligible.

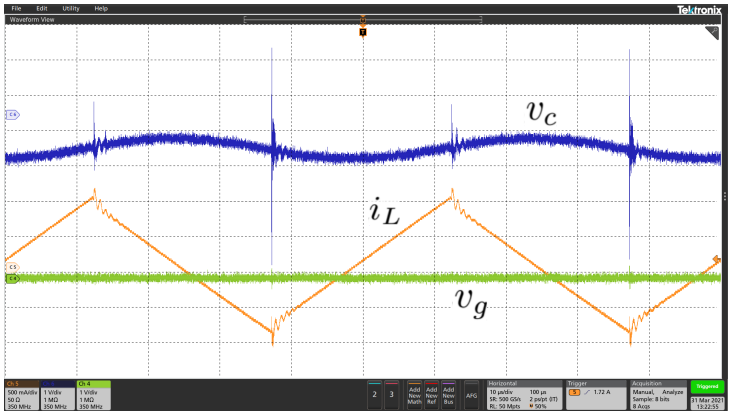


Figure 5.27: Oscilloscope screen capture showing switching components over 2 switching periods. The blue trace features 1 V/div scale and corresponds to $v_c(t)$. The orange trace features 500 mA/div scale and corresponds to $i_L(t)$. The green trace features 1 V/div scale and corresponds to the voltage measured by connecting both probe leads to the capacitor ground connection, $v_g(t)$.

Cascade of the feedback filter and the controller is labeled as $H_{eq} = -G_c G_{fb}$, for consistency with Section 5.5. For all following results, two traces are plotted for the analytical predictions based on (5.7). The first one corresponds to not including the decimation impact, i.e. $H_n(\omega)$ is determined as in (5.8). The second one corresponds to the extended model from (5.22); referring to (5.7), $|H_n(\omega)|^2$ is replaced by:

$$|H_n(\omega)|^2 = \frac{|G_{dpwm}(\omega)G_p(\omega)|^2}{|1 - H_{eq}(\omega)G_{dpwm}(\omega)G_p(\omega)|^2}|H_{eq}^{M:1}(\omega)|^2. \tag{5.23}$$

The decimation frequency is equal to $2f_{pwm}$. Note again that the frequency response of the cascade $G_{dpwm}G_p$ is obtained by first transforming it to the Z-domain, using the impulse-invariant discretization with frequency $f_s = Nf_{pwm}$. Both analytical models are used in order to show that introducing the appropriate filtering brings the MS-PWM noise propagation properties close to the ones of linear systems.

The controller/filter cascades validated in Section 5.5.2.2 correspond to those that are introduced in Section 5.4.2 based on the qualitative analysis, and that are experimentally tested here. Note, however, that there are differences between the model simulated in Section 5.5.2.2 and the experimental set-up, so the results are not expected to be equivalent. First of all, in MS-PWM, the DPWM is *assumed* to re-sample the modulating waveform twice per switching period. However, it is not exactly an ideal, theoretical, decimator so it is of interest to see how the derived theory directly applies to that case. Secondly, in the simulations from Section 5.5.2.2, the plant model (in the continuous time domain) follows a re-sampler and a ZOH with $T_{s,2}$, which does not match the small-signal response of the multi-sampled modulator.

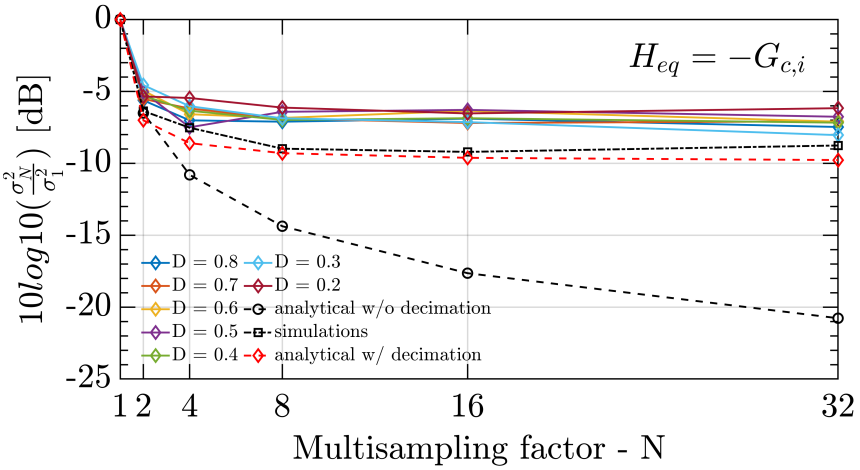
5.6.1 Benchmark simulation settings

Simulations are performed in MATLAB/Simulink (using PLECS Blockset) by adding a random signal to the feedback, as for the validations in Section 5.5. The injected signal features high enough bandwidth, so that it can be considered as white noise for all examined sampling frequencies. In simulations, data acquisition, ADC and DPWM quantization effects match those in the experimentally tested prototype. One of the motivations for providing the simulation results here is to compare noise propagation between the simulations that feature practically ideal white noise injection and the experiments with realistic noise coming from the set-up. The switching noise is not simulated, as it is strongly dependent on hardware realisation; hence, the results would lack generality in conclusions. The simulations were performed for many operating points and different values of input noise powers. The relative noise attenuation results did not change; hence, the experimental results are here compared with the simulations for an arbitrarily chosen $D = 0.4$ and the input noise powers corresponding to the ones that are estimated from the experimental set-up.

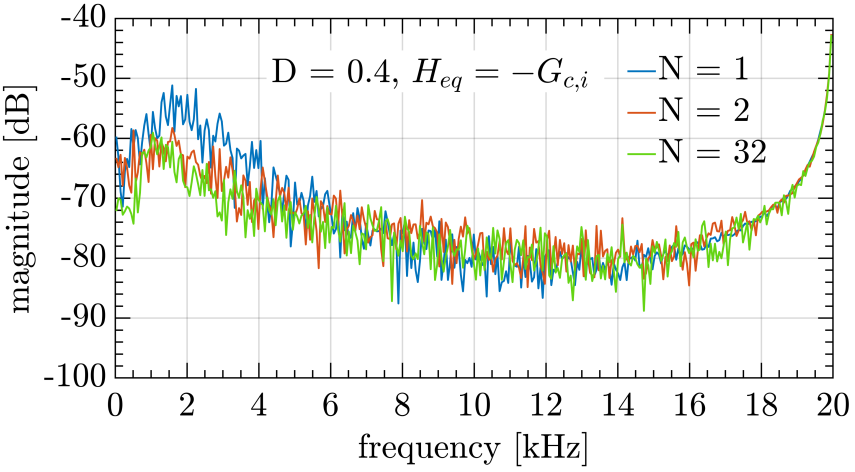
5.6.2 Results for the PI current loop

Variances of i_L corresponding to the measured, simulated, and analytical results are shown in Figs. 5.28a and 5.29a. The results are given relative to the lowest tested oversampling factor ($N = 1$ for the current loop).

In Fig. 5.28a, the results are given for the control loop without any digital feedback filters, where $H_{eq}(z) = -G_{c,i}(z)$. It can be seen that the linear analysis using (5.8) shows a good match for (S/D)S-PWM. For $N > 2$, a great mismatch from the analytical values using (5.8) is obtained both in the simulations and the experimental measurements. Including the extended model from (5.23) brings a very good prediction of the MS-PWM behavior. This is the first confirmation that DPWM's behavior truly resembles a re-sampler. As observed, for $N > 2$, the noise power remains nearly constant, with small variations caused by the impact of the phase margin on filtering performance. Note that this result is completely coherent with the previous reasoning regarding the impact of aliasing for the high-frequency proportional-dominant controllers. Namely, if no digital filtering is used to attenuate components in zone B in Fig. 5.9, the DPWM decimation action causes aliasing and no benefit in terms of noise attenuation is obtained compared to DS-PWM. The spectral plots in Fig. 5.28b show negligible difference in the noise floor between the cases with $N = 2$ and $N = 32$. All spectral results are averaged over 60 Hz window for clarity and the dc component is removed. For this control loop realization, the phase margins are equal to $\{25.75°, 53.3°, 66.98°, 73.77°, 77.15°, 78.84°\}$ for $N = \{1, 2, 4, 8, 16, 32\}$ respectively. The experimentally obtained variances, relative to $N = 1$ and averaged over the tested values of D, are equal to $\{-5.2, -6.45, -6.75, -6.76, -7.12\}$ dB, for N starting from 2. It can be seen that a strong noise attenuation is obtained when increasing N from 1 to 2, both due to doubling of the sampling frequency and a significant increase of the phase margin that results in a higher filtering action by the closed-loop system.



(a)

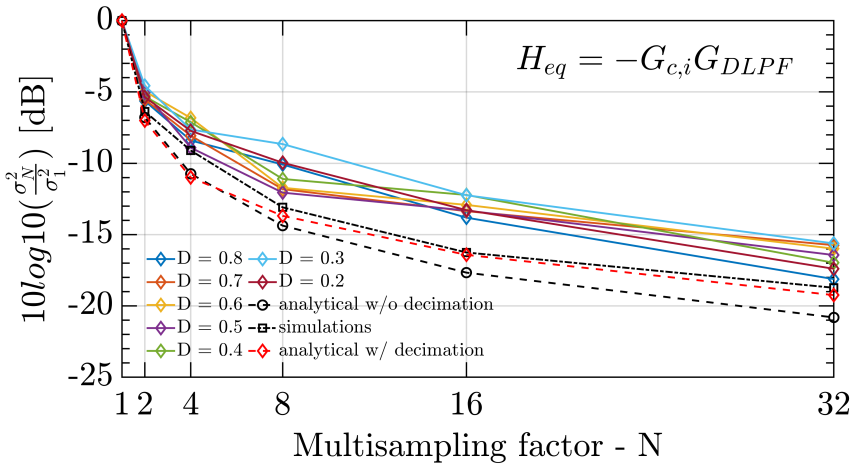


(b)

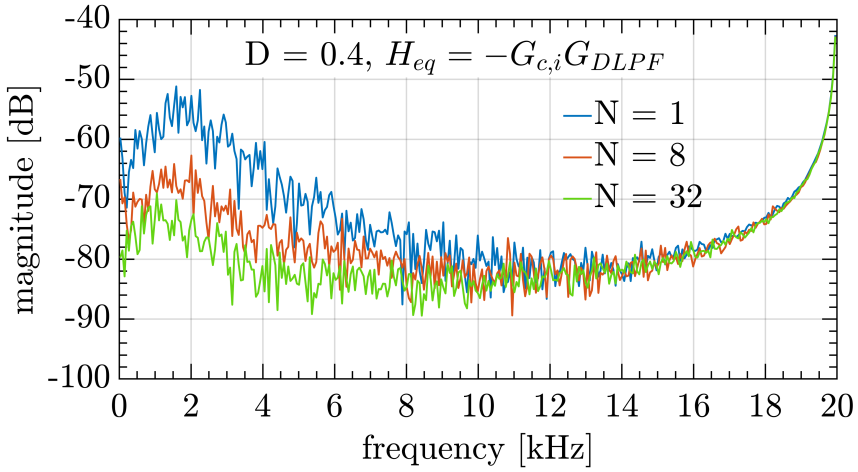
Figure 5.28: Comparison between the experiments, simulations, and analytical models for the current loop without a feedback filter: (a) variance results (b) spectral results (experimental).

In Fig. 5.29a, the variance results are shown for the case when the DLPF is introduced in the feedback, i.e. $H_{eq}(z) = -G_{c,i}(z)G_{DLPF}(z)$. It can be seen that the addition of $G_{DLPF}(z)$ brings a good match between the simulations, experiments, and both analytical models (with and without including the decimation). This confirms that appropriate high-frequency filtering brings the MS-PWM noise propagation properties close to the ones of linear systems. The trends are consistent for all operating points. For this control loop realization, the phase margins are equal to $\{25.75°, 53.3°, 61.2°, 68°, 71.38°, 73.1°\}$ for $N = \{1, 2, 4, 8, 16, 32\}$ respectively. The experimentally obtained variances, relative to $N = 1$ and averaged over the tested values of D, are equal to $\{-5.2, -7.81, -10.77, -13.3, -16.6\}$ dB, for N starting from 2. It can be seen that, for higher values of N where the phase margins are very similar, the noise power is attenuated by approximately -3 dB for each doubling of N. These results confirm that the multi-sampled control loop with the $G_{DLPF}(z)$ significantly suppresses the feedback noise, without strongly affecting the dynamic performance. In Fig. 5.29b, the spectral results show a significant dif-

ference in the noise floor when the multisampling factor is increased. It should be noted again that the results for $N = 1$ and $N = 2$ are obtained without $G_{DLPF}(z)$ as the DPWM decimation does not occur for those cases.



(a)



(b)

Figure 5.29: Comparison between the experiments, simulations, and analytical models for the current loop with $G_{DLPF}(z)$ from (5.11): (a) variance results (b) spectral results (experimental).

For a time domain illustration, the peaks of i_L are detected and plotted in Fig. 5.30 for $N = 1$ and $N = 32$ with the DLPF, being the extreme cases. The plot features relative values, obtained by subtracting the mean value of the current peaks and dividing by the dc value of i_L, for $D = 0.4$.

From these results, it is concluded that MS-PWM control loops with the PI controllers can offer high noise attenuation, without a significant impact on the dynamic response.

5.6.3 Results for the PID voltage loop

In Fig. 5.31, variance results are shown for the voltage loop, without and with $G_{DLPF}(z)$ added in the feedback. The noise power is shown relative to $N = 2$. It is interesting to note that here, unlike

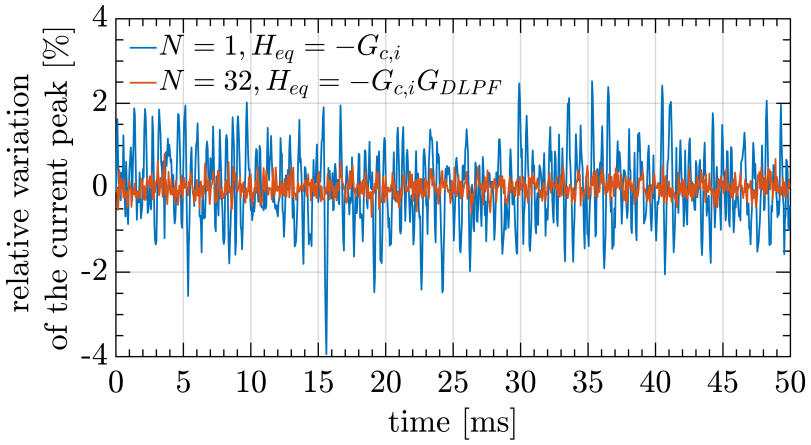
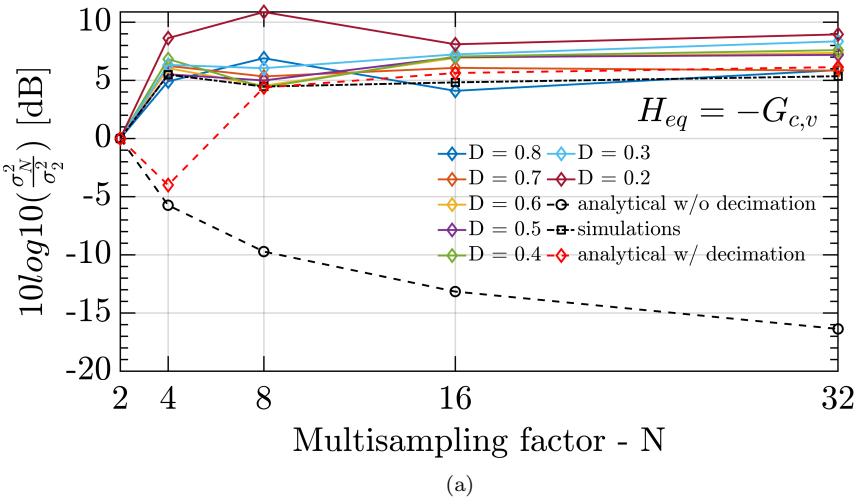


Figure 5.30: Experimental results showing a time-domain impact of noise for the tested current loops. The case with $N = 1$ without a feedback filter is compared to the case with $N = 32$ and $G_{DLPF}(z)$ from (5.11). The results show the relative variation of the detected current peak values.

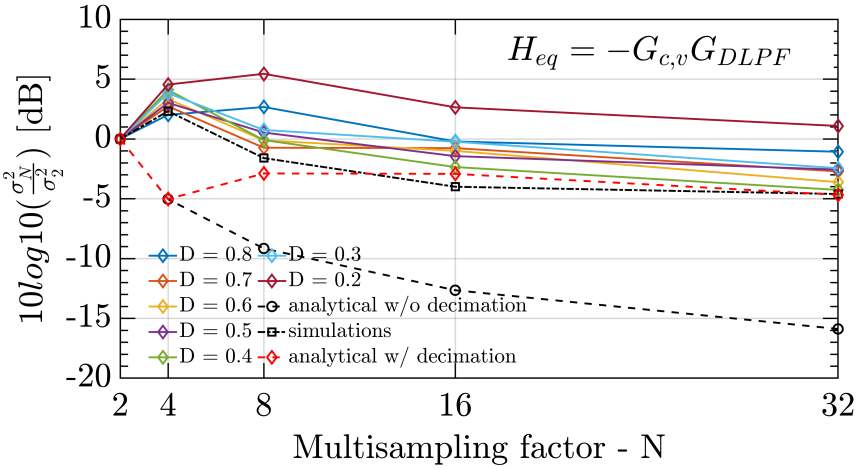
for the current loop, using MS-PWM control without any digital filters (Fig. 5.31a) results in noise amplification rather than attenuation, which is compliant with the conclusions made in Sections 5.4 and 5.5. For this control loop realization, the phase margins are equal to $\{20.1°, 35.5°, 43.1°, 46.8°, 48.7°\}$ for $N = \{2, 4, 8, 16, 32\}$ respectively. The experimentally obtained variances, relative to $N = 2$ and averaged over the tested values of D, are equal to $\{6.36, 6.16, 6.64, 7.3\}$ dB, for N starting from 4. With the increase of N, even though the phase margin is increased, the noise power is amplified due to the high-frequency behavior of the derivative action. Again, the extended analytical results that include the decimation impact show an excellent match with the simulations and experiments, except for $N = 4$. At this point, it is assumed that the mismatch for $N = 4$ may come from some nonlinear phenomenon that is not modeled.

When the $G_{DLPF}(z)$ is introduced (Fig. 5.31b), the aliasing is suppressed; however, the noise power is still not significantly reduced compared to DS-PWM ($N = 2$). The phase margins are equal to $\{20.1°, 30.2°, 37.8°, 41.6°, 43.4°\}$ for $N = \{2, 4, 8, 16, 32\}$ respectively. The experimentally obtained variances, relative to $N = 2$ and averaged over the tested values of D, are equal to $\{3.37, 1.21, -0.482, -2.23\}$ dB, for N starting from 4. The same conclusions are brought regarding the match with the analytical models.

The experimental results show consistent trends with the change of the operating point. A higher mismatch in Fig. 5.31a can be seen for $D = 0.2$ and $N = 8$, and in Fig. 5.31b for $D = 0.2$ and $N > 4$, and $D = 0.8$ and $N = 8$. It is assumed that this is caused by sampling the switching noise or by the discontinuity-related nonlinearities, which both may appear around those values of D and N [24]. The sensitivity to switching noise propagation depends on the values of N and D, and the impulse response of $H_{eq}(z)$. The switching noise differs greatly from white noise; hence, it is not covered by the models derived in this chapter. However, it should be noted that the voltage loop shows a higher sensitivity to switching noise than the current loop. This sensitivity certainly rises due to the derivative action in the



(a)



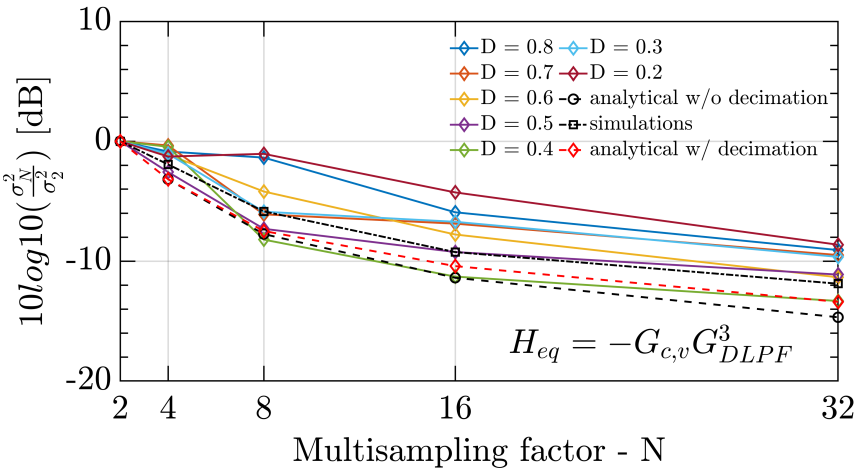
(b)

Figure 5.31: Comparison between the variances obtained from the experiments, simulations, and analytical models for the voltage loop (a) without a feedback filter and (b) with $G_{DLPF}(z)$ from (5.11).

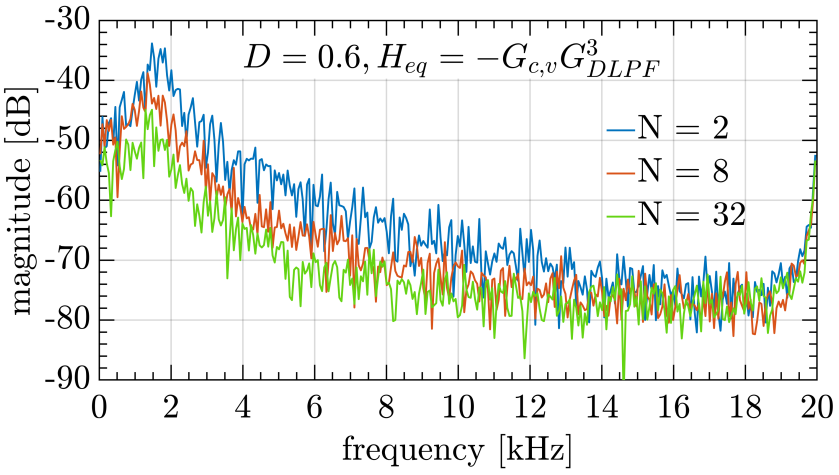
controller, as well as the higher relative magnitude of the switching noise, seen in Fig. 5.27.

In order to further test the suppression of the aliasing effect, the third-order $G^3_{DLPF}(z)$ is added to the feedback. These results are shown in Fig. 5.32. The variance results in Fig. 5.32a show that the DPWM decimation is indeed suppressed by using filters with a higher attenuation at $f > f_{pwm}$, and the noise power keeps decreasing with the increase of N. The simulated and experimental results show a good match with the analytical predictions, both with and without including the decimation effects. For this control loop realization, the phase margins are equal to $\{20.1°, 19.7°, 27.3°, 31.1°, 33°\}$ for $N = \{2, 4, 8, 16, 32\}$ respectively. The experimentally obtained variances, relative to $N = 2$ and averaged over the tested values of D, are equal to $\{-0.97, -4.87, -7.44, -10.38\}$ dB, for N starting from 4. Again, for higher values of N, the noise power is reduced by approximately -3 dB for each doubling of N. A similar operating point dependency is seen as the one for the cases without the filter and with the $G_{DLPF}(z)$. In Fig. 5.32b, the spectral plots are given to show the impact of MS-PWM control on

lowering the noise floor.



(a)



(b)

Figure 5.32: Comparison between the experiments, simulations, and analytical models for the voltage loop with a cascade of 3 DLPFs from (5.11), $G_{DLPF}^3(z)$: (a) variance results; (b) spectral results (experimental).

The filter $G_{DLPF}^3(z)$ introduces nearly 16° phase lag at $f_{c,v}$, which is close to using a MAF, where N latest feedback samples are averaged, i.e. $G_{MAF}(z)$ from (2.9). Hence, the feedback configuration with $G_{MAF}(z)$ is tested as well, and the variance results are shown in Fig. 5.33. These experimental results show an excellent match with the simulations and analytical predictions, while being very consistent for all operating points. For this scenario, the phase margins are equal to $\{20.1°, 23.1°, 28.6°, 31.4°, 32.7°\}$ for $N = \{2, 4, 8, 16, 32\}$ respectively. The experimentally obtained variances, relative to $N = 2$ and averaged over the tested values of D, are equal to $\{-3.9, -7.4, -10.5, -13.5\}$ dB, for N starting from 4. Figure 5.34 is given for a comparison of the voltage spectra for all tested feedback configurations.

For a time-domain illustration, the peaks of v_c are detected and plotted in Fig. 5.35 for $N = 2$ and $N = 32$ with the MAF, being the extreme cases. The plot features relative values, obtained by

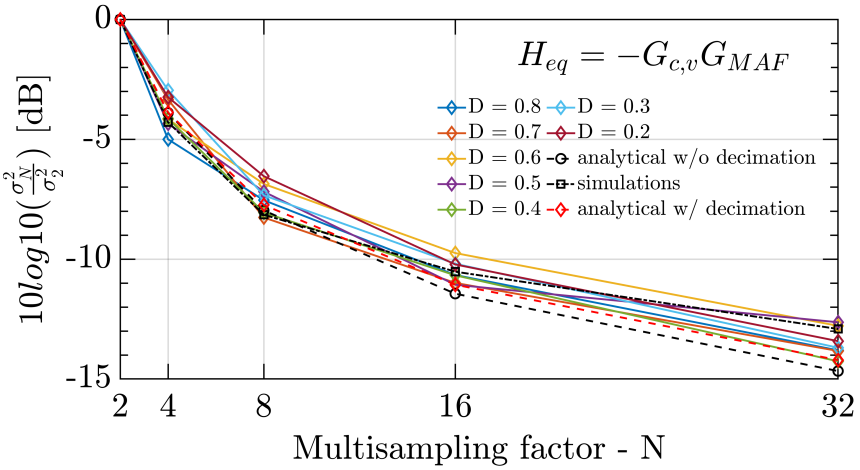


Figure 5.33: Comparison between the variances obtained from the experiments, simulations, and analytical models for the voltage loop with $G_{MAF}(z)$ from (2.9).

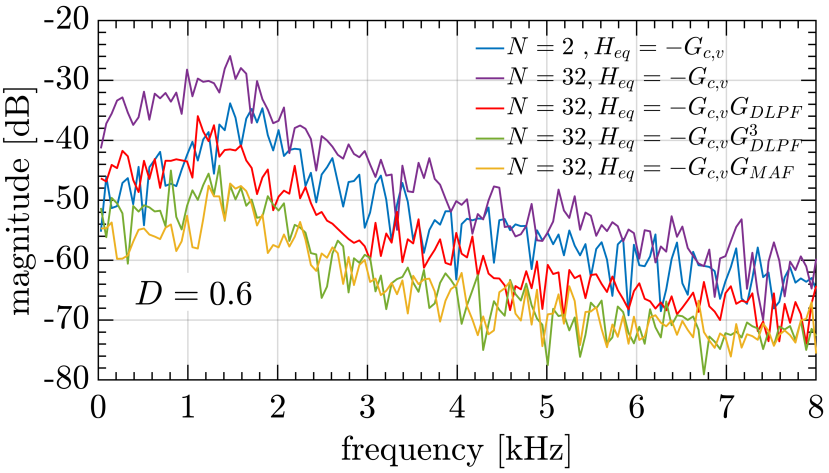


Figure 5.34: Spectral results (experimental) in the frequency window used for the variance calculations for all tested feedback configurations of the voltage loop.

subtracting the mean value of the voltage peaks, and dividing by the dc value of v_c, for $D = 0.6$.

It is concluded that, for MS-PWM control loops with the PID controllers, high noise attenuation can only be achieved with a significant impact on the system dynamics (Fig. 5.32 and Fig. 5.33). It is recommended to use $G_{MAF}(z)$ instead of $G_{DLPF}^3(z)$ due to the higher noise suppression, better consistency across operating points, and a similar impact on the dynamic response. Furthermore, the MAF removes the switching ripple, which suppresses the problems caused by the MS-PWM nonlinearities discussed in Chapter 4. Even if strong noise attenuation is not required, it is still recommended to use anti-aliasing digital low-pass filters in the PID-based MS-PWM loops, e.g. $G_{DLPF}(z)$, as the dynamic response is not notably deteriorated and the output noise power is significantly reduced.

It should be noted that, as N is increased, even with the use of filters with a high attenuation (such as MAFs), the dynamic properties are improved compared to the DS-PWM without any filtering. A

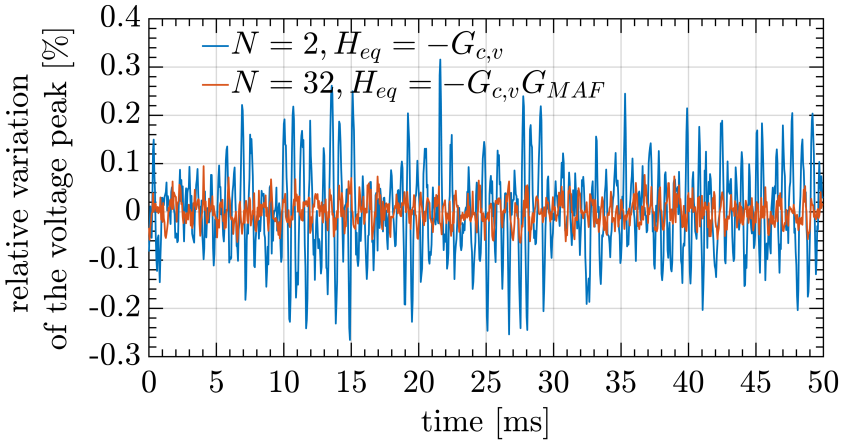


Figure 5.35: Experimental results showing time-domain impact of noise for the tested voltage loops. The case with $N = 2$ without a feedback filter is compared to the case with $N = 32$ and $G_{MAF}(z)$ from (2.9). The results show the relative variation of the detected voltage peak values.

comparison in terms of the noise suppression and dynamic performance between DS-PWM, MS-PWM, and MR-DS-PWM methods is provided in the following section.

5.6.4 Comparison between MS-PWM and MR-DS-PWM methods

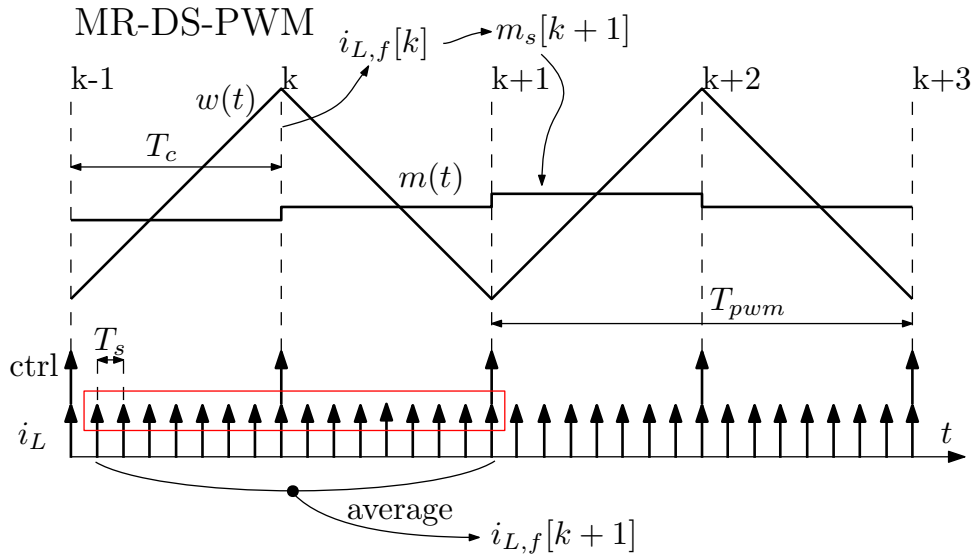


Figure 5.36: Timing illustration for MR-DS-PWM with the MAF and one step computation delay. The control period is labeled with T_c and is, for the case shown, 8 times greater than the sampling period T_s.

In this section, noise propagation is examined for the multi-rate strategies that use oversampling only for filtering purposes. These methods, readily implementable in commercially available DSPs, belong to the MR-(S/D)S-PWM group, for which the feedback is acquired with a high sampling rate, filtered, and then decimated to the single- or double-update rate [63, 110]. An example of a timing diagram for MR-DS-PWM with the MAF is given in Fig. 5.36. The analysis is performed for the current control loops.

Again, the results are compared with both analytical models, with and without including the decimation impact. It is interesting to note that practically the same extended model is used for MS-PWM and MR-DS-PWM, as both cases feature the decimation inside the closed-loop system. A small, but important, difference for MR-DS-PWM is that the equivalent fold-back transfer function H_{eq} in (5.23) includes only G_{fb}, while the controller is placed in the cascade with G_p. Another difference is found in the frequency response of G_{dpwm} and one step computation delay (if added), which are determined by Nf_{pwm} for MS-PWM and $2f_{pwm}$ for MR-DS-PWM.

In this section, five cases of different control strategies are compared in terms of dynamics and noise attenuation. For all oversampled strategies, $N = 16$ is chosen. Case A represents the standard DS-PWM control, which is used as a benchmark. The equivalent time delay, introduced by the modulation and one step computation delay, is approximately $\tau_{d,A} = \frac{3}{2}T_{s,A} = \frac{3}{4}T_{pwm}$. Case B represents MR-DS-PWM control with $G_{MAF}(z)$ from (2.9). When implemented in DSPs, this strategy relies on a DMA module to buffer the highly-oversampled feedback signal, which is then averaged over the switching period at the double-update rate [63]. Given that the phase response of the MAF over T_{pwm} is very close to a delay of $\frac{1}{2}T_{pwm}$, the total time delay of case B is $\tau_{d,B} \approx \frac{3}{2}T_{s,B} + \frac{1}{2}T_{pwm} = \frac{5}{4}T_{pwm}$. Case B is expected to provide strong noise attenuation at the expense of a significantly reduced phase margin. Case C is the same as case B, only without the one step computation delay. An almost instantaneous control execution is possible using custom hardware platforms, e.g. FPGAs [3]. When using DSPs, this delay reduction can be achieved by re-scheduling the control interrupts just before the instants when the DPWM carrier is equal to its peak or valley (assuming a short enough computation time) [87, 110]. The equivalent time delay of case C is $\tau_{d,C} \approx \frac{1}{2}T_{s,C} + \frac{1}{2}T_{pwm} = \frac{3}{4}T_{pwm}$. Case C is expected to provide strong noise attenuation while retaining similar dynamics to case A. Case D is MS-PWM control with $G_{MAF}(z)$ from (2.9). The equivalent time delay of case D is $\tau_{d,D} \approx \frac{3}{2}T_{s,D} + \frac{1}{2}T_{pwm} = \frac{\frac{3}{N}+1}{2}T_{pwm}$. As noted, all results are given for $N = 16$; however, it is interesting to point out that, starting from $N = 6$, the MS-PWM control with the MAF brings less delay than DS-PWM without any filters. Case D is expected to provide strong noise attenuation with better dynamics compared to the cases above. Finally, case E represents the MS-PWM control with $G_{DLPF}(z)$ from (5.11). This case is expected to provide strong noise attenuation with the best dynamic performance.

For all strategies, the PI current controller is used, with slightly higher gains compared to Section 5.6.2. All other parameters of the experimental set-up are the same as for the previously shown results. The summary of compared strategies and their parameters is shown in Table 5.2.

Noise power attenuation, relative to case A, is shown in Fig. 5.37. As consistency of the results for different operating points is demonstrated in Section 5.6.2, the output noise power is shown just for one duty cycle, $D = 0.45$.

From Fig. 5.37 it can be seen that, compared to DS-PWM, all examined strategies that use oversampling and digital filtering result in strong noise attenuation. The difference between cases B and C is due to a higher phase margin in case C, which brings a higher filtering by the closed-loop system. As

Table 5.2: Control strategies tested in this section

Description	label	value	unit
Controller configuration	$G_{c,i}$	PI	/
Relative proportional gain	$\frac{V_{in}}{R}k_{p,i}$	0.3064	/
Relative integral gain	$\frac{V_{in}}{R}k_{i,i}$	366	$\frac{1}{\text{s}}$
Crossover frequency	$f_{c,i}$	≈ 2400	Hz
DS-PWM group			
case A	label	value	unit
Filter configuration	/	/	/
One step computation delay	z^{-1}	yes	/
Phase margin	PM	54.2	°
MR-DS-PWM group - $N = 16$			
case B	label	value	unit
Filter configuration	$G_{MAF}(z)$	/	/
One step computation delay	z^{-1}	yes	/
Phase margin	PM	33.9	°
case C	label	value	unit
Filter configuration	$G_{MAF}(z)$	/	/
One step computation delay	z^{-1}	no	/
Phase margin	PM	54.9	°
MS-PWM group - $N = 16$			
case D	label	value	unit
Filter configuration	$G_{MAF}(z)$	/	/
One step computation delay	z^{-1}	yes	/
Phase margin	PM	62.8	°
case E	label	value	unit
Filter configuration	$G_{DLPF}(z)$	/	/
One step computation delay	z^{-1}	yes	/
Phase margin	PM	75.7	°

expected, the results for cases C and D are very close as the same digital MAF is used and the phase margins are similar. Note that the phase margin for case D is affected by the one step computation delay, which is not present only for case C. Finally, case E provides nearly the same noise attenuation as cases C and D, while the dynamic properties are significantly improved. This is a confirmation that, in order to achieve high noise attenuation in current control loops, the MS-PWM control with the anti-aliasing $G_{DLPF}(z)$ is a good choice. It can be seen that both analytical models, with and without including the decimation, provide an excellent prediction of the output noise power. This is due to the fact that all tested cases feature digital filtering[6] at $f > f_{pwm}$ that suppresses aliasing and brings noise propagation properties close to the ones of linear systems. These results further affirm that the extended model that

[6]Except the DS-PWM, which does not feature decimation in any case.

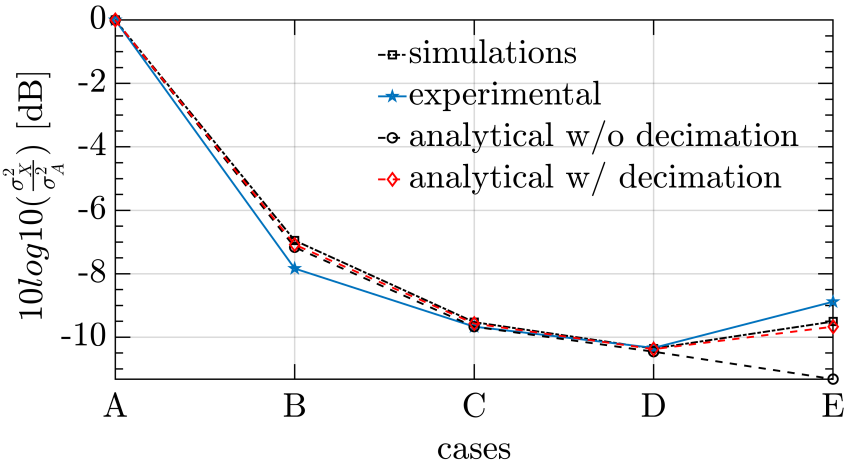


Figure 5.37: Comparison of noise attenuation for the tested strategies. A: DS-PWM; B: MR-DS-PWM with $G_{MAF}(z)$ and one step computation delay; C: MR-DS-PWM with $G_{MAF}(z)$, without one step computation delay; D: MS-PWM with $G_{MAF}(z)$; E: MS-PWM with $G_{DLPF}(z)$.

includes the decimation is well suited for both MS-PWM and MR-DS-PWM.

5.7 Summary

This chapter has provided the analysis of noise propagation in digitally controlled multi-sampled power converters. First, it is concluded that the analytical model for LTI systems is able to predict-well noise propagation in case of (S/D)S-PWM. A limiting aspect for the case of MS-PWM is the nonlinear property of the DPWM, which closely resembles a decimator. Hence, for strong noise attenuation, anti-aliasing digital filters are required to suppress the decimation effect caused by the DPWM. Design of such filters is proposed, first using a qualitative approach, and it is shown that the single-stage loops with the high-frequency proportional-dominant controllers (P, PI, PR) can strongly suppress noise with a small impact on the dynamic response. Without any filters, these controllers result in a nearly constant output noise power, as N is increased above 2. Contrarily, when controllers include a derivative action, the oversampling on its own brings noise amplification. In such cases, for strong noise suppression, the required anti-aliasing digital filters introduce a higher impact on the system dynamics.

Additionally, this chapter brings an analogy, in terms of noise propagation, between MS-PWM and MR-(S/D)S-PWM, which both include decimation inside the closed-loop system. Models for noise propagation analysis in systems that feature decimation are derived and verified in simulations and experimentally. The proposed models can be used for the quantitative anti-aliasing digital filter design, for both cases of MS-PWM and MR-(S/D)S-PWM.

A very good match between the proposed models and the experimental measurements validates that, in terms of noise propagation, DPWM does introduce the decimation action. This brings an interesting conclusion that, in case of the oversampled US-PWM control systems, decimation cannot be avoided.

Either it will be performed intentionally (MR-(S/D)S-PWM), or inherently (by the DPWM in case of MS-PWM). Hence, for noise suppression, suitable anti-aliasing filtering is always needed. In general, noise attenuation capabilities of these two control strategies are practically the same. An important difference is that, in case of MS-PWM, for similar filtering, significantly better dynamics can be achieved owing to the modulation delay reduction.

Chapter 6

Impedance shaping for robust stability of grid-connected VSCs

6.1 Introduction

Existing power systems are experiencing a great change due to the increasing presence of grid-tied power electronic converters. These devices are more and more necessary to fully exploit renewable energy resources, enable electrification of transportation, and the storage of electrical energy, among other functions [1, 132]. Heavy presence of actively controlled voltage-source converters (VSCs), connected to ac distribution networks, rises some concern, as it is known that, due to the interaction between various grid-connected converters, harmonic instability may arise and compromise the system operation [133]. This may occur, for example, when control systems of grid-tied VSCs introduce negative damping at frequencies of poorly damped grid resonances. In the low frequency range, negative damping is introduced by the Phase-Locked Loop (PLL) of inverters and the constant power control of rectifiers [133,134]. In the high frequency range, negative damping is caused by the time delay and current control loop dynamics (in case of grid-following converters) [133, 135]. This chapter focuses on the investigation of harmonic instability at high frequencies, caused by delays of the current control system [135].

For stability analysis of systems with interconnected power converters, the impedance based approach is found to be very effective [135–147]. It consists of representing each converter with its Norton or Thevenin equivalent circuit and assessing the system stability properties by analyzing the resulting admittance network. A sufficient, but not necessary, condition for the system stability is obtained if each admittance is passive, i.e. its real part is non-negative at the frequencies of interest [134, 135, 148–150]. For this reason, to prevent the harmonic instability, passivity-based control (PBC) has been more and more often considered [134, 135, 141, 148–164]. This concept has proved to be powerful for the analysis and the improvement of the stability of a system that consists of many interconnected power converters [133, 153, 165–167]. Initially, focus was placed on passivizing the admittance up to the Nyquist frequency

(NF). However, more recently, it has been pointed out that passivity should be investigated also above the NF, where the coupling between sidebands, generated by sampling and modulation, introduces a destabilizing mechanism [141,143,144,168]. Based on these considerations, in some countries, the heavy impact of grid-tied VSCs on the traction system stability has resulted in the requirement to comply with input admittance passivity standards [152].

For US-PWM with one step computation delay, the VSC admittance exhibits a negative conductance above, approximately, one sixth of the sampling frequency f_s [135]. For enhancing passivity of VSCs operating with (S/D)S-PWM, many different strategies of active damping (AD) have been developed. Some improvement is obtained by adding damping filters to the current controller [153, 169–171], however, most methods employ additional feedforward[1] or feedback actions [135,143,148–150,154–164,172]. While certain multi-loop methods are developed specifically for VSCs with LCL filters [157,159,161,163, 164, 172, 173], this chapter compares and refers to the most generally applicable ones, that are relevant also for VSCs with L filters[2] [135, 143, 148, 149]. These methods rely on derivative-based feedforward of the voltage at the point of common coupling (PCC). In terms of effectiveness, for full passivity up to the NF, analog or oversampled derivative action must be applied. This kind of AD, first analyzed in [135] and generalized in [149], will be referred to as the Derivative Active Damping (D-AD). The passive region can also be extended without the analog or oversampled implementation of the derivative action, which is referred to as Discretized Derivative Active Damping (DD-AD) [143, 148]. DD-AD effectively increases the passive region up to approximately $\frac{f_s}{3}$.

Given that high-frequency passivity issues arise due to digital delays, the investigation of MS-PWM performance in this application was found to be a natural choice. This has motivated the comparison between AD and MS-PWM in terms of passivizing the VSC admittance in the high-frequency range. The results found in this chapter are published in papers [70, 71, 73]. The conclusions of this research are reinforced, based on a later, independent source [43].

First contribution presented in this chapter deals with investigating the capability of MS-PWM control to render the admittance passive by inherently reducing, instead of compensating, digital delays and, in this way, approaching the NS-PWM. It is shown that the increase of the oversampling factor improves passivity, by boosting the admittance phase even above the switching frequency. In this way, passivity is achieved almost effortlessly and the design of the current control loop can be performed solely based on the required closed-loop tracking performance. Extensive experimental verification is provided to validate the small-signal analysis and to examine the impact of the MS-PWM nonlinearities investigated in Chapter 4. It is found that the impact of the MS-PWM nonlinearities on admittance passivity is not detrimental; just some mismatch from analytical modeling is seen, mainly for lower values

[1] Note that the subsequently introduced active damping action based on the output voltage can only be considered as a feedforward in case the VSC is connected via an L filter to an ideal grid with zero impedance. Otherwise, the AD action should strictly be classified as a feedback. Given that analyzing interconnection stability only makes sense in case of a non-ideal grid, the feedforward active damping is an incorrect term, although widely spread in the literature. However, to avoid misinterpretation, the term feedforward will be used in this chapter.

[2] Regarding passivation effectiveness, conclusions do not differ between the two groups. Notable difference is the fact that in case of LCL filters, the capacitor current feedback can replace the output voltage derivative.

of oversampling factors. Importantly, it is found that operation in reduced-gain or zero-gain zones always brings the admittance closer to being fully passive, which is in agreement with the reasoning that for those nonlinearities, the modulator is "less active".

Second contribution is a direct comparison in effectiveness of D-AD, DD-AD, and MS-PWM in passivizing the admittance in the high-frequency range. Even though in [141] it is shown that this frequency range is important for stability, there is a lack of detailed investigation of corresponding AD effectiveness, which is addressed in this chapter. Admittance properties are analytically investigated and experimentally validated up to twice the switching frequency of the tested VSC. Results show that AD *does not* provide robust stability of grid-tied VSCs for harmonic resonances around and above the NF. This property is predictable by a linear single-frequency model of the VSC admittance. Experimental results are given to show destabilization of grid anti-resonances found slightly below the NF for DD-AD and above NF for D-AD. MS-PWM enables stable operation for all tested cases by passivizing the VSC in a wider frequency range.

Third contribution is the analytical modeling, experimental measurements, and comparison of noise sensitivity of D-AD, DD-AD, and MS-PWM. A potential practical challenge with D-AD and DD-AD concerns noise sensitivity due to implementation of the derivative feedforward action. Accordingly, this chapter provides investigation of noise propagation, which has not been analyzed in the literature yet. The proposed analytical models predict well the experimental measurements in case of both single-loop (MS-PWM) and double-loop (AD) control systems. Another step forward is taken by modeling the noise propagation for the case of oversampled (or analog) derivative being followed by a re-sampler, i.e. the case of D-AD. This analysis takes into account the impact of decimation on noise propagation, using models derived in Chapter 5. An important conclusion is that D-AD and DD-AD strategies *are not* highly sensitive to measurement noise, thanks to a relatively low required value of the derivative gain. For DD-AD, it is shown that, for all practical purposes, noise sensitivity is the same as without AD. Following the anti-aliasing digital filter design guideline from Chapter 5, MS-PWM is shown to be able to offer strong additional noise attenuation. It is verified that corresponding digital filters do not pose a significant impact on admittance properties in the frequency range of interest.

6.2 Control of grid-following VSCs

Grid-following VSCs are employed in power systems as current-controlled converters. As the most general case, this chapter considers a single-phase VSC with an inductive output filter, as shown in Fig. 6.1a. However, the analysis is easily extendible to three-phase VSCs in stationary coordinates as well as to any output filter structure. The current reference $i_{L,r}$ is provided by outer loops that control the required power flow by changing the reference current magnitude $|i_{L,r}|$ and phase angle Φ, with respect to the voltage at PCC, v_{pcc}. A PLL is used to track the fundamental component of v_{pcc}.

The closed-loop block diagram of the current control system is shown in Fig. 6.1b, where v_{pcc} is shown as a disturbance. The current controller (CC) $G_c(z)$ processes the error between $i_{L,r}$ and the

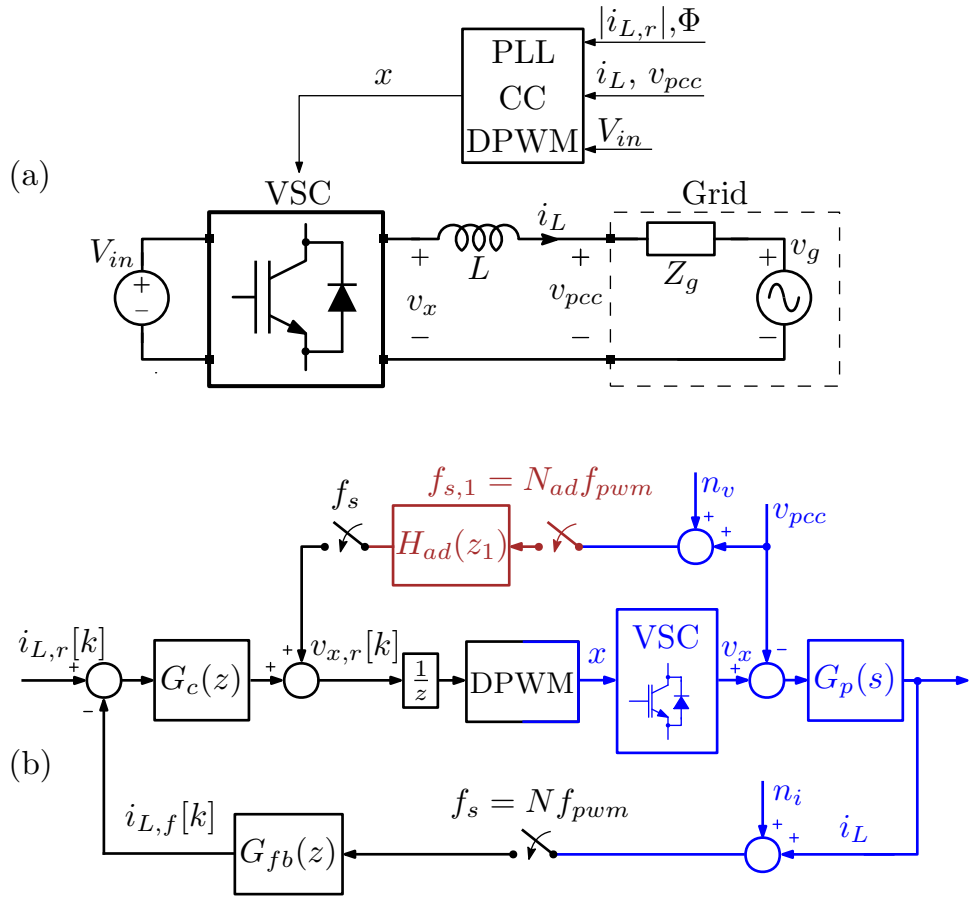


Figure 6.1: Illustration of a grid-following VSC: (a) schematic representing connection to a grid; (b) multi-rate current control system with a feedforward action. Black color depicts blocks executed at the current sampling rate. Red color depicts the feedforward execution rate. Continuous-time domain is shown in blue. Signals n_i and n_v represent measurement noise for current and voltage sensing, respectively.

filtered inductor current feedback $i_{L,f}$. In this chapter, the control execution and the feedback sampling are always performed with the same frequency, f_s. The complete control signal, i.e. the reference average switched node voltage $v_{x,r}$, may also include an action based on v_{pcc}, which will be referred to as AD, $H_{ad}(z_1)$. The execution rate of the AD block is independently chosen as $f_{s,1} = N_{ad} f_{pwm}$, where N_{ad} will be referred to as the AD oversampling factor. The Z-domain variable z_1 corresponds to $T_{s,1} = \frac{1}{f_{s,1}}$. In case $f_{s,1} \neq f_s$, a rate conversion needs to be included after H_{ad}. The reference voltage signal $v_{x,r}$ is scaled with V_{in} to obtain the digital modulating signal m_s, which is not illustrated in Fig. 6.1. It is assumed that, due to finite algorithm computation time, the controller output is delayed by one control period. The switching signal x, together with V_{in}, determines the VSC output switched node voltage v_x, as explained in Section 4.2.1. The difference between the VSC switched node voltage v_x and v_{pcc} is applied to the output inductive filter, which determines the plant transfer function as:

$$G_p(s) = \frac{i_L(s)}{v_x(s) - v_{pcc}(s)} = \frac{1}{sL}. \tag{6.1}$$

The analyzed system is modeled without any resistances, which represents the worst case regarding

stability, as any resistance positively impacts the system resonance damping [150].

6.2.1 Equivalent time delay and controller design

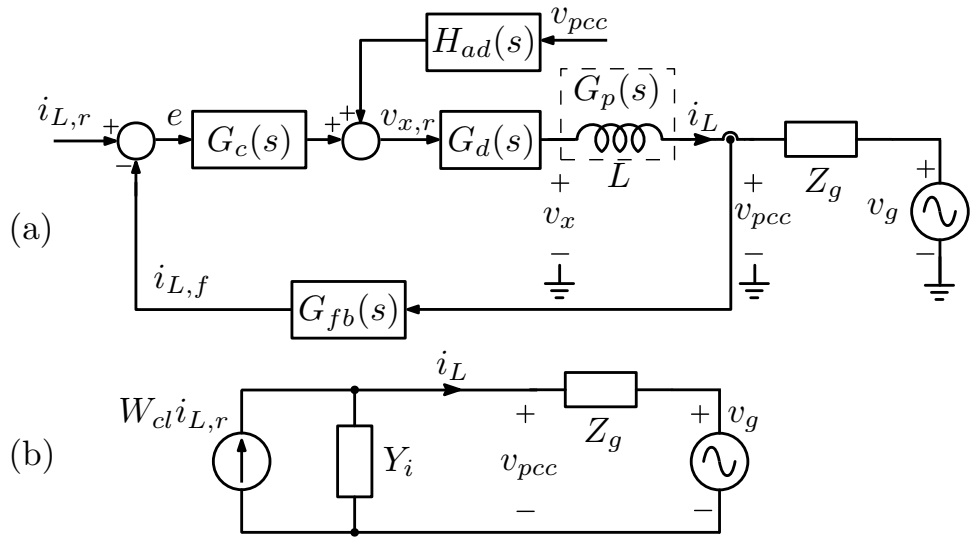


Figure 6.2: S-domain representation of a grid-following VSC: (a) current control system and grid connection; (b) Norton equivalent circuit used for impedance-based stability assessment.

In this chapter, modeling is performed in the s-domain to allow investigation of the VSC admittance properties, which determine the continuous-time physical response of the converter, even above the NF [141]. Impact of the sampling and modulation sidebands [73,141,143,144,167,168] is not considered, as it introduces additional complexity, without being crucial for the conclusions drawn in this chapter. The s-domain representation of the system is shown in Fig 6.2a. All modeled time delays are represented by a unique block $G_d(s)$.

As mentioned before, and seen from (2.3), digitally-controlled VSCs exhibit operating point dependency, which is often overlooked when using delay or ZOH models for the DPWM, due to a limited impact at low and medium frequencies [73]. In [73], it is shown that this operating point dependency may have a significant impact in the high frequency range. However, for the purpose of bringing some general conclusions based on simple and intuitive expressions, for most parts of this chapter, the simplified delay model from (2.5) is considered[3]. It will be pointed out when the delay model brings a significant mismatch from the actual VSC behavior and some considerations regarding the impact of the operating point dependency on admittance properties are placed in Section 6.4. Together with the added one step computation delay, the total time delay in the digital current control system is found as:

$$G_d(s) = \frac{v_x(s)}{v_{x,r}(s)} \approx e^{-s\tau_D} = e^{-s\frac{3}{2}T_s} = e^{-s\frac{3}{2}\frac{T_{pwm}}{N}} \tag{6.2}$$

As a standard approach for sinusoidal reference tracking [3], the proportional-resonant (PR) current

[3]For the tested buck-type VSC, scaling used to transform $v_{x,r}$ to m_s is inversely applied to obtain v_x from d (the continuous time duty cycle of x); hence, it can be omitted from the small-signal analysis, using the plant described in (6.1).

controller structure from (4.4) is chosen. As a design example used here, the proportional gain is chosen as $k_p = \omega_c L$, where $\omega_c = 2\pi f_c$ is the sought angular crossover frequency of the current loop. The resonant gain is chosen as $k_r = \frac{1}{10}\omega_c k_p$, which limits its impact to lower frequencies. In this chapter, the relative crossover frequency (bandwidth) is labeled $\alpha = f_{c,r} = \frac{\omega_c}{\omega_{pwm}}$. As discussed in Section 2.3, the value of α is limited by the small-signal stability margins and the PWM carrier frequency.

6.3 Impedance-based stability analysis of grid-tied VSCs

6.3.1 Norton equivalent circuit

The impedance-based stability assessment requires representing the VSC with its Norton equivalent circuit, as in Fig 6.2b. The Norton current source determines the short circuit current of the VSC, i.e. the value of i_L when $v_{pcc} = 0$. It is defined by the inner closed-loop transfer function, W_{cl}, of the system shown in Fig 6.2a:

$$W_{cl}(s) = \frac{i_L(s)}{i_{L,r}(s)}\bigg|_{v_{pcc}=0} = \frac{W_{ol}(s)}{1 + W_{ol}(s)}, \tag{6.3}$$

where $W_{ol}(s) = G_c(s)G_d(s)G_p(s)G_{fb}(s)$ is the open-loop gain of the corresponding system. The input admittance Y_i is found as the inductor current response to the voltage v_{pcc}, when the current reference is set to 0:

$$Y_i(s) = -\frac{i_L(s)}{v_{pcc}(s)}\bigg|_{i_{L,r}=0} = \frac{G_p(s)\left(1 - H_{ad}(s)G_d(s)\right)}{1 + W_{ol}(s)}. \tag{6.4}$$

From (6.4), it can be seen that the VSC input admittance is shaped by the output filter and the current control system, which includes digital delays and, if implemented, AD. Without the AD filter, at frequencies above the control bandwidth, where $|W_{ol}(s)| \approx 0$, Y_i converges to the physical filter admittance. The impact of outer loops on the admittance is not modeled, as this chapter focuses on properties at frequencies significantly above their bandwidth [134].

Considering the VSC connection to a non-ideal grid, i.e. such that $Z_g \neq 0$, the inductor current can be calculated using the equivalent circuit parameters as:

$$i_L(s) = \frac{W_{cl}(s)}{1 + Y_i(s)Z_g(s)} i_{L,r}(s) - \frac{Y_i(s)}{1 + Y_i(s)Z_g(s)} v_g(s). \tag{6.5}$$

Assuming that W_{cl} is stable, stability of the grid-connected VSC depends on the product $Y_i(s)Z_g(s)$, which is referred to as the minor-loop gain [137]. Stability analysis can be performed by applying the Nyquist stability criterion to the minor-loop gain[4].

[4]The admittance Y_i in (6.4) is the so-called single-frequency model [73, 141, 143]. Impact of sampling and modulation sideband components can be taken into account using multi-frequency modeling [73, 141, 143]. It is important to note that the multi-frequency model is by itself non-linear; hence, using control tools derived for linear systems, such as the Nyquist stability criterion, is not strictly accurate. It will be shown that single-frequency Y_i models well the VSC behaviour in the frequency range of interest. Consequently, linear analysis will be used to predict stability of the grid-connected operation.

6.3.2 Passivity criterion

A linear single-input single-output (SISO) system, such as $Y_i(s)$, is said to be passive if the real part of its frequency response is non-negative for all frequencies [149]. In other words, $Y_i(s)$ is passive if its phase response is limited to the range $[-\frac{\pi}{2}, \frac{\pi}{2}]$. A stronger condition of "strict" passivity is obtained by limiting the phase to the open interval $(-\frac{\pi}{2}, \frac{\pi}{2})$. In case both $Y_i(s)$ and $Z_g(s)$ are passive, the minor-loop gain always satisfies the Nyquist stability criterion as its phase is limited to the range $[-\pi, \pi]$. Imposing the requirement[5] for passive behavior of $Y_i(s)$, as in [152], comes from the fact that a sufficient condition for the VSC stability is satisfied if $Y_i(s)$ is passive and the VSC is connected to another passive network.

In this chapter, the input feedforward passivity (IFP) index is used as a measure of the VSC passivity [149, 150]. It is defined as the minimum value of the real part of the input admittance, i.e. the minimum value of the input conductance:

$$\mathrm{IFP(Y_i)} = min_{\omega \in \mathbb{R}} Re\{Y_i(j\omega)\}. \tag{6.6}$$

The IFP is useful to quantify the impact a VSC may have on the grid stability, as it points to the minimal damping introduced by it. The IFP is negative in case of a non-passive input admittance.

Considering a system without the AD and the feedback filters, for a purely proportional current controller, the real part of $Y_i(j\omega)$ is calculated using (6.4):

$$Re\{Y_i(j\omega)\}|_{H_{ad}=0, G_{fb}=1, k_r=0} = \frac{\omega_c}{L} \frac{\cos(\omega\tau_D)}{(\omega_c - \omega\sin(\omega\tau_D))^2 + (\omega\cos(\omega\tau_D))^2}. \tag{6.7}$$

The expression is not given for the case of a PR controller, as it is more complicated and, hence, lacks a clear qualitative insight. Nonetheless, the resonant gain is designed such that its impact at high frequencies is very small, meaning that the IFP for a PR controller will be very similar to the one obtained with the proportional gain only [149]. It can be seen from (6.7) that, for the proportional controller, the sign of the conductance depends only on the cosine term, while its magnitude depends also on the bandwidth and is inversely proportional to the value of the inductance. The conductance first becomes negative when the argument of the cosine term goes over $\frac{\pi}{2}$. Considering the total time delay in (6.2), this occurs at the frequency $\frac{Nf_{pwm}}{6}$, which is often referred to as the critical frequency [149]. For the case of SS-PWM, the non-passive region is found above $\frac{f_{pwm}}{6}$, for DS-PWM above $\frac{f_{pwm}}{3}$, and so on. It can be concluded that, for the case of NS-PWM, without any other control delays, the admittance is inherently passive at high frequencies.

To illustrate the impact of system parameters on passivity, the IFP is found for the conductance from (6.7) and the results are shown in Fig. 6.3. The values are given for different multisampling factors and three values of α, corresponding to $\frac{\omega_c}{\omega_{pwm}} = \{5, 10, 20\}\%$. For $N = 1$, results are not shown for $\alpha = 0.2$ as

[5] In [152] the passivity requirement is set above 5^{th} harmonic of the fundamental. Low frequency passivity issues, e.g. caused by dynamics of the PLL, are not investigated in this chapter. Since the PLL bandwidth is always set considerably lower than the one of the current loop, its impact on Y_i in medium- and high-frequency range is negligible [134]; hence it is not included in the admittance model.

such gain results in the instability of $W_{cl}(s)$ in (6.3). For better generality, the values on the left axis show the IFP relative to the VSC filter susceptance at the angular frequency ω_m, for which the IFP is found. In this way, the results become independent on the specific value of L. On the right axis, the values of ω_m are shown. Firstly, it can be seen that control loops with high bandwidths bring a significantly stronger negative damping, while the frequency at which the IFP is found remains practically constant. This yields the conclusion that, for a constant delay, the passivity issues are more likely to be found in high bandwidth systems. Secondly, as the value of N is increased, the relative IFP rapidly converges towards 0. Additionally, ω_m moves to higher frequencies meaning that the absolute IFP, i.e. negative conductance, reduces even more. Finally, it can be concluded that lower values of L result in a stronger negative damping. As mentioned, repeating the analysis for realistic values of k_r practically does not change the results shown in Fig. 6.3.

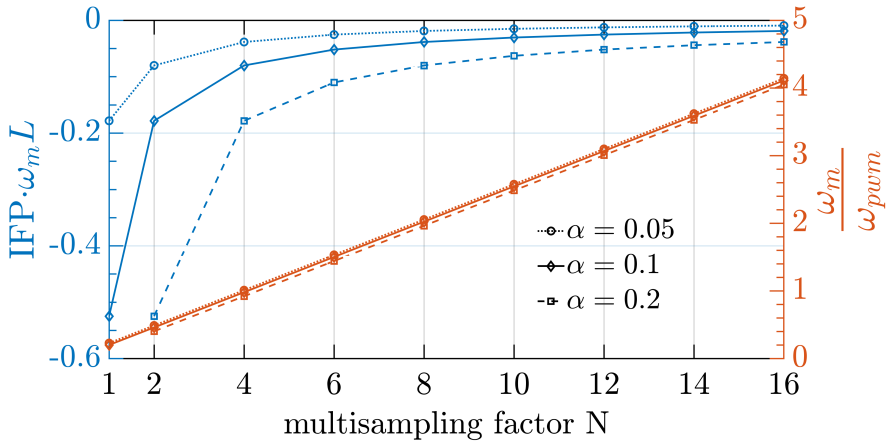


Figure 6.3: Left axis shows the relative passivity index of the VSC input admittance for a proportional controller and three different values of the relative crossover frequency α. Right axis shows frequency for which the IFP is found, relative to the switching frequency.

There is some ambiguity regarding the interpretation of standards like [152] to determine the upper frequency limit for passivity measurements. Several publications have shown that, for single- and double-update PWM, investigation is necessary also above the Nyquist frequency due to the sampling and modulation sideband components [141, 143]. In [148], authors conclude that if an LCL filter is used, even in the case the inner current loop is non-passive, high-frequency components on the grid side flow mainly through the capacitor; hence the non-passive high-frequency region of the inner current loop gets compensated and passivity should only be addressed around the bandwidth. However, it should be noted that the existence of an LCL filter can only reduce, and not completely remove, the non-passive behavior. This is due to the fact that a parallel connection of a non-passive element and a reactive element remains non-passive [149]. A generalized conclusion is hard to be brought, as it depends on the control bandwidth, passive component sizing, and losses in the circuit.

As for the MS-PWM, the results shown in Fig. 6.3 predict the existence of very small negative conductances at frequencies significantly above the switching frequency. However, this comes from the

small-signal modeling that does not take into account the PWM large-signal behavior. Namely, a two-level converter still physically reacts to disturbances only twice per switching period, by modifying rising and falling edges of $x(t)$. This brings doubts that a VSC can be active at, for instance, $f = 4f_{pwm}$. Additionally, for high values of N, the small-signal analysis predicts the existence of negative conductances with values very close to 0; hence, even very small resistances would be enough to compensate and make the experimental measurements of non-passive zones impossible. In the end, given that, at frequencies significantly above the bandwidth, the admittance magnitude is determined by the physical VSC output filter, its low-pass nature would require extremely high values of perturbation voltages to cause the resulting current to even be detectable by the ADC. Therefore, the subsequent admittance measurements are performed up to $2f_{pwm}$, which corresponds to the sampling frequency for DS-PWM.

6.4 Analysis and experimental verification of admittance properties

In this section, the VSC admittance is measured for all compared control strategies. First, the admittance measurements are given for the case of DS-PWM without AD, to serve as a benchmark. Then, it is shown that MS-PWM is capable of rendering the admittance passive in a wide frequency range, without any active damping. The results are given for values of $N \in \{4, 8, 16, 32\}$. Finally, the impact of AD on admittance properties is examined, and a comparison between all tested strategies is presented.

For the experimental verification, the set-up B.3 is used. It is illustrated in Fig. 3.1c and its parameters are shown in Table 3.3. Two inductive filters with different values of L are used to demonstrate the impact of the inductance on the IFP, as seen in Fig. 6.3. The control system is implemented on the FPGA platform described in Section 3.2. For all tested cases, the control system features one step computation delay. The feedback filter G_{fb} is not used, except for two tests where this is clearly indicated. For the digital implementation of the PR controller, the impulse-invariant structure from (4.31) is used.

6.4.1 Measurement set-up

Direct admittance measurements of current-controlled converters are typically performed by setting the current reference to 0, which disconnects the Norton current source shown in Fig. 6.2b [143, 148]. The perturbation voltage is applied to the converter's output filter and the measured current determines the admittance response at the same frequency. As mentioned in Section 6.3.1, even if a PLL is used during the admittance measurements, its bandwidth must be set well-below the current loop bandwidth [139]; hence, its impact can always be considered negligible for the examined high-frequency passivity properties [134].

The circuit used for the admittance measurements, shown in Fig 6.4, consists of the tested VSC with its inductive output filter, the perturbation branch, and the bias branch. For the first set of results, the perturbation source v_p was formed using the power operational amplifier PA107DP, from APEX.

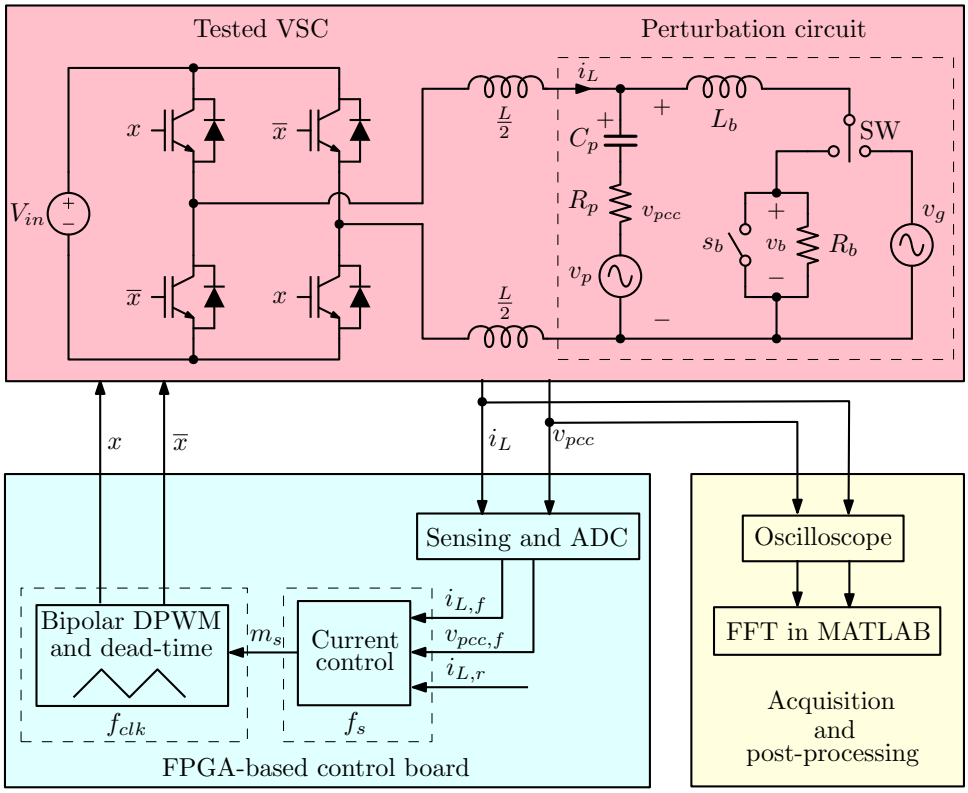


Figure 6.4: Illustration of the set-up for admittance measurements.

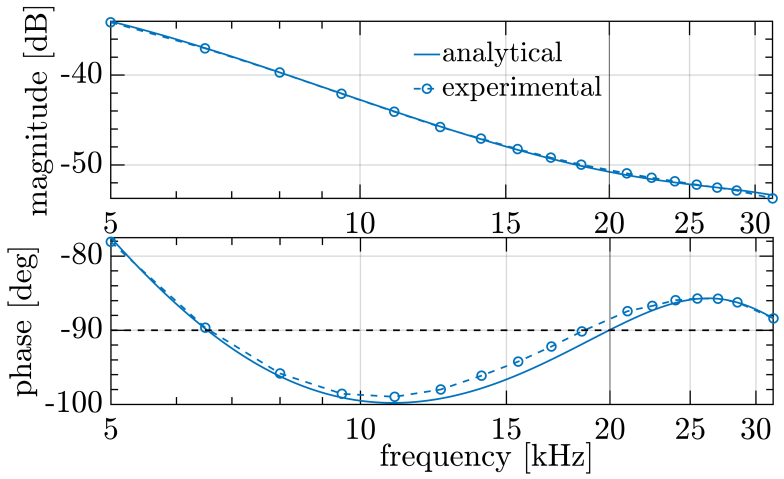
Due to the current limit of PA107DP, the corresponding admittance measurements were conducted for a reduced value of $V_{in} = 250$ V and for the higher-value inductance $L = 2.5$ mH, so that the switching ripple in i_L is decreased. The value of V_{in} does not impact the small-signal admittance, as seen from (6.4). Subsequently, PA107DP was replaced by MP118, also from APEX, which allowed measurements with $L = 1.5$ mH as well. The perturbation source is connected in series with a capacitor $C_p = 10$ μF and a resistor $R_p = 1$ Ω that is used to smooth any transients. The capacitor is used to block dc currents as well as to decouple the bias branch from the VSC, so that the switching ripple harmonics of i_L would remain practically the same as if the VSC was connected to an ideal grid. In this way, the ripple-induced MS-PWM nonlinearites, analyzed in Chapter 4, are not altered by the measurement set-up. The bias branch features an inductance $L_b = 2.4$ mH, which attenuates the perturbation components so that the perturbation source is not heavily loaded, and a resistor R_b that can be bypassed with a switch s_b. The bias branch has two functions. First of all, it allows the circulation of any dc current. All admittance measurements are performed for an imposed dc current reference, such that no current crossover occurs. This scenario is more critical for passivity as it is reported that dead-times may provide a certain damping when the current crosses 0 [174]. Note that a dc component of i_L does not impact the admittance measurements in the high frequency range. Secondly, if the switch SW is in its left position, when the switch s_b is opened, a dc component of i_L provides a voltage drop across R_b. This creates a dc component of v_{pcc}, referred to as the bias voltage v_b, without needing to use an additional dc power supply. By imposing an adequate bias voltage, the admittance can be measured around specific operating

points. Alternatively, in case the switch SW is in its right position, the admittance measurements can be obtained while the VSC is directly connected to an ac power supply, e.g. the power grid. As the DPWM exhibits several nonlinearities and, as seen from (2.3), operating point dependency, investigation of small-signal properties of the system makes sense to be performed only around stable and constant operating points. When the converter operates connected to an ac grid, its operating point moves in a certain range and the measured admittance is expected to be some sort of an average of the results obtained for steady operating points in the same range. Detailed investigation and modeling of the impact of the DPWM's operating point dependency on the admittance measurements can be read in [73]. Measurements around specific, critical, operating points also allow investigation of the impact of the discontinuity-related MS-PWM nonlinearities on admittance properties. The admittances are measured both without and for three positive values of the voltage bias. For the bias values of 65 V and 75 V, the resistance is set to $R_b = 24\ \Omega$. For a 150 V bias, the resistance is set to $R_b = 48\ \Omega$. These bias values determine the steady-state operating point as $D = 0.5(\frac{v_b}{V_{in}} + 1)$, if series voltage drops are neglected.

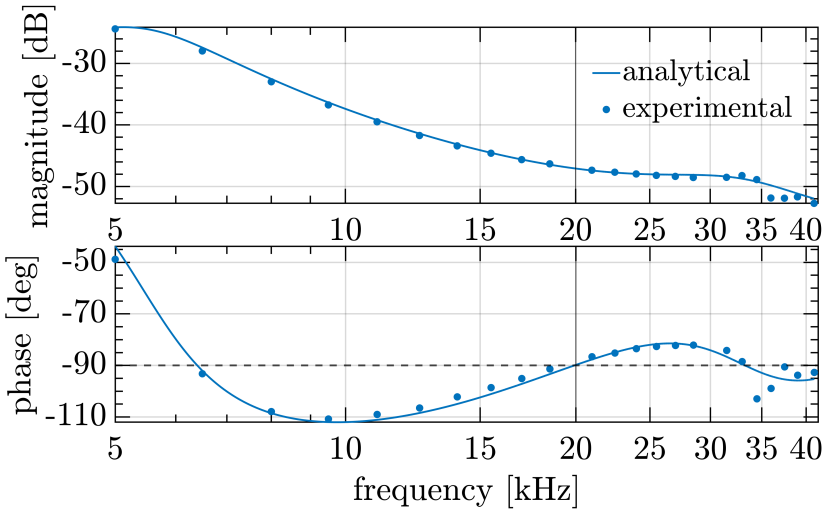
The first set of measurements, using PA107DP and for $L = 2.5$ mH, was conducted for 17 frequencies, one at the time, in the range from 5 kHz to 31.5 kHz ($0.25f_{pwm}$ to $1.575f_{pwm}$), avoiding the switching frequency. When PA107DP was replaced with MP118, the corresponding measurements for $L = 1.5$ mH were conducted in an extended frequency range from 5 kHz to 41 kHz, which is just above f_s for $N = 2$. Qualitatively, the results did not change, however, to discriminate between these two sets of measurements, data points obtained using PA107DP are plotted using dashed line with markers, while the ones obtained using MP118 are plotted using only circular markers. For each point, a sinusoidal v_p, with the perturbation frequency f_p, is imposed. Its magnitude is calculated to obtain at least 100 mA magnitude of the perturbation current component flowing through the VSC. This allowed precise measurements using the oscilloscope, in the presence of the switching ripple and noise. The inductor current i_L and the PCC voltage v_{pcc} are acquired using the Tektronix 5 series oscilloscope with the data length equal to 40 ms and the acquisition rate equal to 250 MS/s. This yields a spectral resolution, relative to the perturbation frequency, of 0.5 % for $f_p = 5$ kHz, which further improves as f_p is increased. The data is postprocessed in MATLAB, by calculating the FFT of $-i_L$ and v_{pcc}. Based on the magnitude ratio and the phase difference of the perturbation components, the admittance at f_p is calculated. The measurements are performed for the relative crossover frequency $\alpha = 0.1$ and $\alpha = 0.2$. The results are compared with the frequency response of the analytical model from (6.4). For MS-PWM, in the frequency range of interest, it was verified that the analytical model of Y_i does not vary significantly in case the complete DPWM model from (2.3) is included; hence, the delay model from (2.5) is used for the analytical traces. Note that, for DS-PWM and $D = 0.5$, the DPWM model is exactly equal to the delay from (2.5).

6.4.2 Benchmark results for DS-PWM without AD

Let us begin by showing the impact of delays on admittance properties in case no passivizing strategy is used, i.e. for DS-PWM without AD. The results obtained without applying the output bias voltage ($D = 0.5$) are shown in Fig. 6.5, for different values of α and L, to emphasize their impact. First of all, it can be seen that a very good match with the analytical prediction is obtained, even above the NF. Approximately at frequencies $f > 1.5 f_{pwm}$, the single-frequency model (6.4) starts to show a more significant mismatch, which is addressed in [73]. Note the existence of two non-passive zones, where the phase drops below $-90°$. The first one starts at approximately 6.5 kHz, which is consistent with the often mentioned critical frequency $\frac{f_s}{6}$ [135]. Another non-passive zone appears above the NF. The goal of the passivity-based design, which is analyzed in the following sections, is to suppress these non-passive zones.



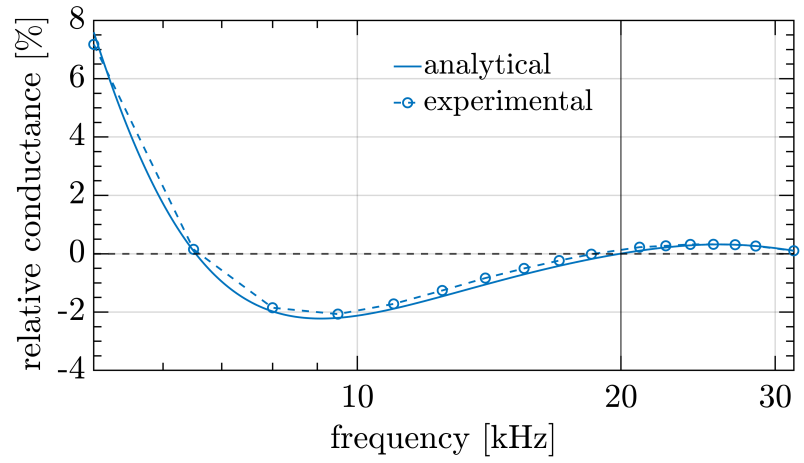
(a)



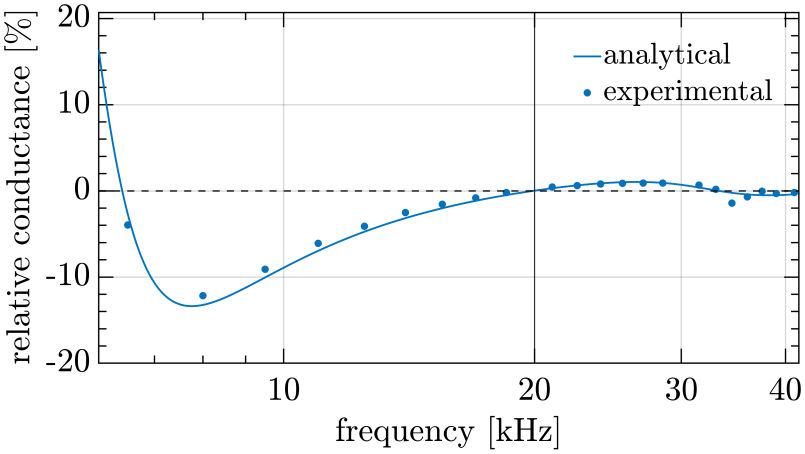
(b)

Figure 6.5: Admittance measurements for DS-PWM without AD: $N = 2$, $H_{ad} = 0$, and: (a) $L = 2.5$ mH and $\alpha = 0.1$; (b) $L = 1.5$ mH and $\alpha = 0.2$. The vertical line marks the switching (and the Nyquist) frequency. The results are measured without the output bias voltage.

An alternative representation, useful for bringing conclusions regarding passivity, is to show only the real part of Y_i, i.e. its conductance. For admittances in Fig. 6.5, conductances are shown in Fig. 6.6, with values being scaled by the nominal VSC admittance $Y_n = \frac{S_n}{v_{pcc,RMS}^2} = 56.7$ mS.



(a)



(b)

Figure 6.6: Relative conductance for DS-PWM without AD: $N = 2$, $H_{ad} = 0$, and: (a) $L = 2.5$ mH and $\alpha = 0.1$; (b)$L = 1.5$ mH and $\alpha = 0.2$. The vertical line marks the switching (and the Nyquist) frequency. The results are measured without the output bias voltage.

6.4.3 Results for MS-PWM without AD

In this section, the impact of MS-PWM on admittance properties is investigated. Specifically, attention is dedicated to examine the impact of the MS-PWM nonlinearities on the passivation effectiveness. All results are given for $L = 2.5$ mH and $\alpha = 0.1$ as, at the time of these measurements, only PA107DP was available. The results were later repeated for the other values of L and α and the conclusions did not qualitatively change.

The results for $N = 4$ are given in Fig. 6.7, without the voltage bias and for the bias levels of 75 V

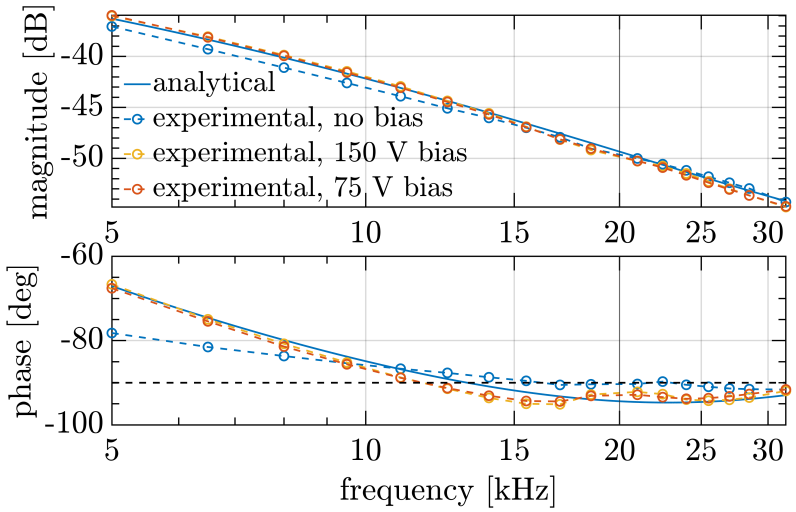


Figure 6.7: Admittance measurements for MS-PWM without AD: $N = 4$, $H_{ad} = 0$, $L = 2.5$ mH, $\alpha = 0.1$, and 3 dc values of the output bias voltage. Without the dc bias, vertical crossings between m and w occur. The vertical line marks the switching frequency.

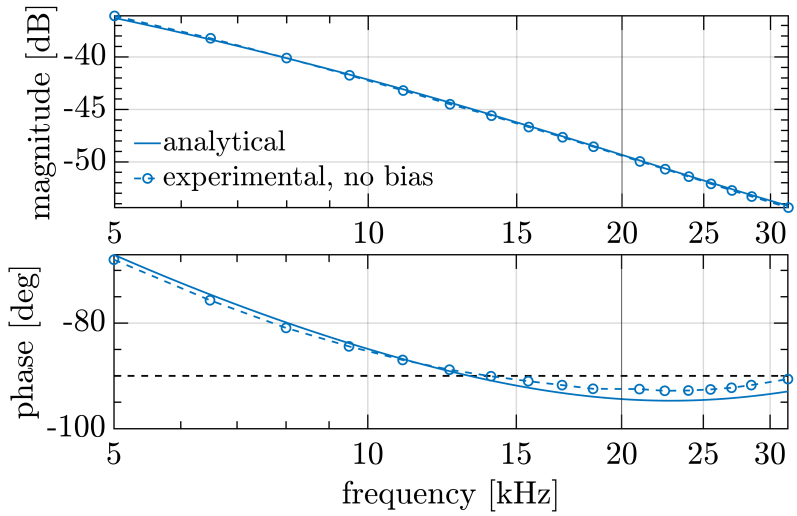


Figure 6.8: Admittance measurements for MS-PWM without AD: $N = 4$, $H_{ad} = 0$, $L = 2.5$ mH, $\alpha = 0.1$, without the output bias voltage. MS-PWM is linearized such that no vertical crossings between m and w occur. The vertical line marks the switching frequency.

and 150 V. Without the bias voltage, duty cycle is perturbed around a steady-state value of $D = 0.5$. It can be seen that, for that case, the measurements show a slight mismatch from the analytical results, particularly in the range below 10 kHz. It is verified that, for this operating point, one edge of x is determined by a vertical crossing between m and w, which results in the reduced-gain operation, as discussed in Chapter 4. It is interesting to note that, at higher frequencies, this nonlinearity does not cause the admittance to go deeper in the non-passive zone; on the contrary, it seems that this operation adds some damping to the system. The same effect is noticed for other values of N under reduced-gain operation. Moreover, for operation inside the dead-bands (double vertical crossings, see Chapter 4), it is verified that the VSC is completely passive as its admittance phase is locked at $-90°$. In Fig. 6.7, when

a dc bias is added, the operating point is such that no vertical crossings occur, and a good match with the analytical results is seen. Around 12 kHz, the admittance enters the non-passive zone, however, this zone is much less emphasized compared to $N = 2$.

It is of interest to verify whether the mismatch for $N = 4$ without the bias results from the discontinuity-related MS-PWM nonlinearity. For this, the MS-PWM behavior is linearized, based on the approach from Chapter 4. As shown in Section 4.5.3.4, for $N = 4$, the vertical crossings caused by the modulating waveform discontinuities can be completely prevented by adding a feedback low-pass filter with the suitable cut-off frequency. For the specific case, G_{fb} from (4.21) is used, with the cut-off frequency $\omega_{c,f} = 39$ kHz. The role of G_{fb} is solely on shifting the switching ripple component of m with respect to the carrier, in order to disable vertical crossings, and its impact on dynamics is negligible. The corresponding results are shown in Fig. 6.8, and it can be seen that a good match with the analytical predictions is once again obtained. This confirms that the effect observed in Fig. 6.7 is due to the MS-PWM nonlinearities and not the small-signal modeling errors.

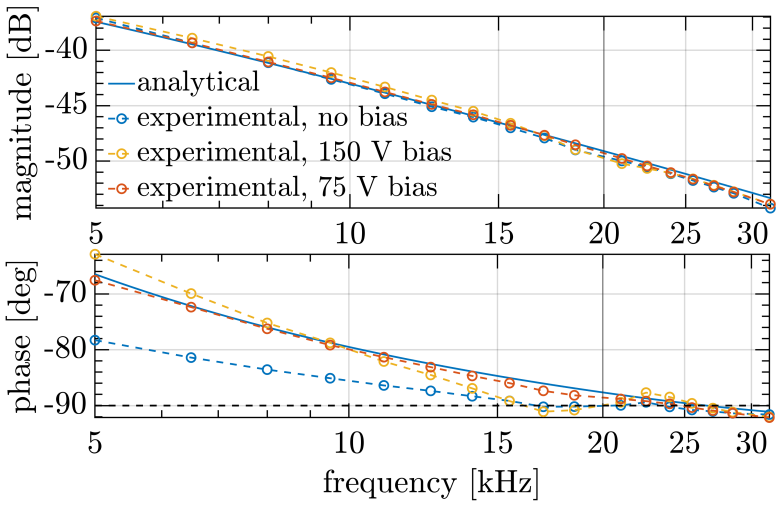


Figure 6.9: Admittance measurements for MS-PWM without AD: $N = 8$, $H_{ad} = 0$, $L = 2.5$ mH, $\alpha = 0.1$, and 3 dc values of the output bias voltage. Without dc bias, vertical crossings between m and w occur. The vertical line marks the switching frequency.

The results for $N = 8$ are given in Fig. 6.9 and similar conclusions as for $N = 4$ are brought. Analysis predicts that the non-passive zone occurs around 26 kHz, with the phase of Y_i being just slightly under $-\frac{\pi}{2}$. As for $N = 4$, without the output bias, the reduced-gain operation is present and a mismatch from the analytical predictions is seen. Again, this mismatch is more evident at lower frequencies, and no detrimental impact on passivity occurs. Note that some drop in the phase is seen with 150 V bias at frequencies very close to the switching frequency. This effect is also measured for other oversampling factors, as well as for DS-PWM, and is most-likely caused by some other nonlinearity in the system (e.g. related to the sampling and modulation sidebands).

The results for $N = 16$ are given in Fig. 6.10. For the 75 V bias, the reduced-gain operation is present. The results are also shown for the 65 V bias, which slightly moves the operating point, enough

to prevent the vertical crossings between m and w, yielding again a very good match with the analytical results. The measurements show that, for all tested operating points, the admittance does not enter the non-passive zone. Moreover, the admittance is strictly passive, which indicates additional robustness.

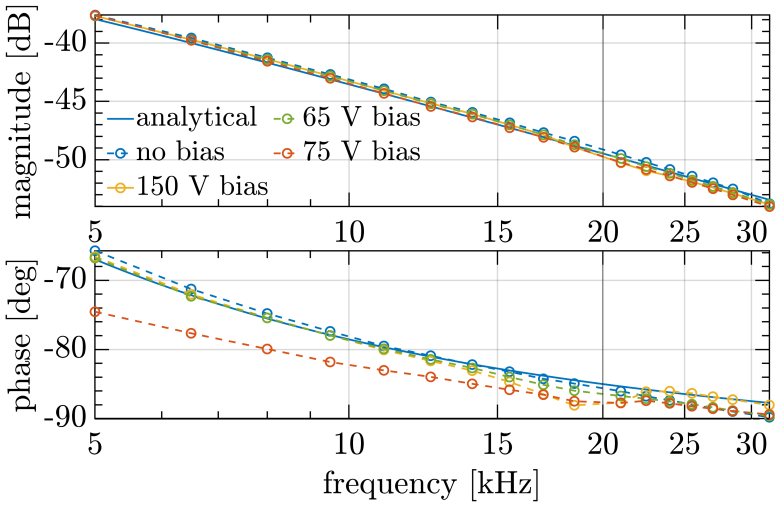


Figure 6.10: Admittance measurements for MS-PWM without AD: $N = 16$, $H_{ad} = 0$, $L = 2.5$ mH, $\alpha = 0.1$, and 4 dc values of the output bias voltage. For 75 V bias, vertical crossings between m and w occur. Word "experimental" is omitted from the legend to fit the figure. The vertical line marks the switching frequency.

The results for $N = 32$ are given in Fig. 6.11. For all operating points, the match with the analytical results is excellent and the admittance is strictly passive.

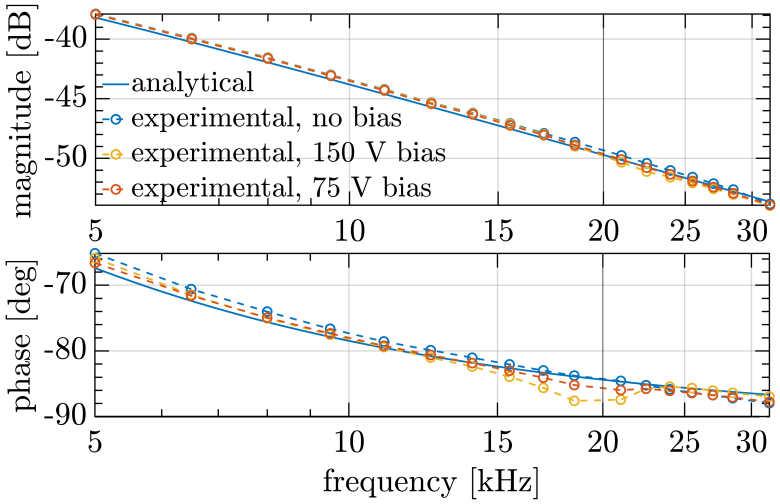


Figure 6.11: Admittance measurements for MS-PWM without AD: $N = 32$, $H_{ad} = 0$, $L = 2.5$ mH, $\alpha = 0.1$, and 3 dc values of the output bias voltage. The vertical line marks the switching frequency.

For a comparison, Fig. 6.12 shows real parts of the measured admittances for all tested values of N. A clear improvement of passivity is obtained as N is increased. The results are given for the operating points that do not feature vertical crossings between m and w.

The results of admittance measurements, performed while the VSC was connected to a sinusoidal

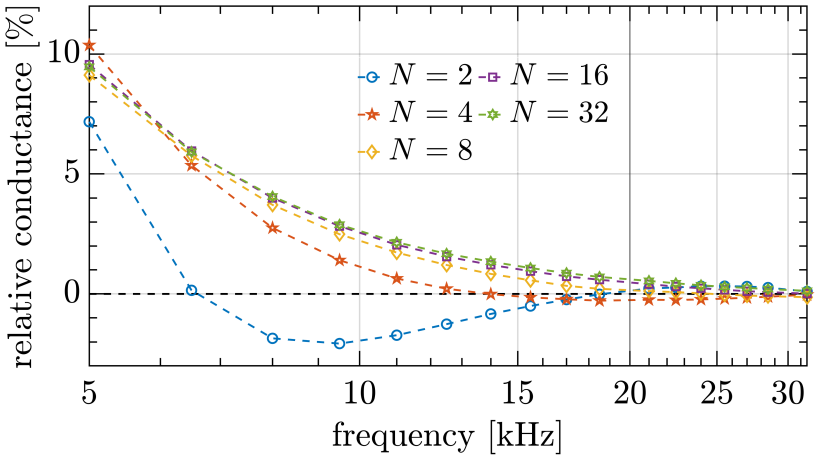


Figure 6.12: Comparison of experimentally measured conductances for all tested values of N, $L = 2.5$ mH, and $\alpha = 0.1$. The results are given for operating points that do not feature vertical crossings between m and w. The vertical line marks the switching frequency.

ac source with the frequency f_1, are not shown. This kind of set-up perturbs the operating point with the frequency f_1, which is not consistent with the small-signal analysis of an inherently nonlinear system. However, it should be noted that both simulations and measurements were performed for such case, as required by the standard [152], and the impact of the MS-PWM nonlinearities was not seen; the measurements still matched well with the analytical modeling and all passivity-related conclusions remained valid. The results were somewhere in between the results for the tested dc operating points that did not feature vertical crossings between m and w. This leads to a conclusion that, regarding passivity, effects of the MS-PWM nonlinearities, which arise at specific operating points, may be masked by the ac operation. However, a general conclusion for any fundamental frequency and perturbation magnitude cannot be brought. Detailed investigation of impact of such measurement scenario is analyzed in [73], but is not further discussed in this thesis.

It should be stated that the experimental results show a very good match with the analytical ones, with errors in the range of a few degrees. This affirms the validity of the used single-frequency modeling. In [143], where a more complex multi-frequency modeling procedure is presented, some mismatch is present both in phase and magnitude. Experimental measurements in [143] are performed up to the switching frequency, for the case of SS-PWM. In [148], measurements are performed up to slightly above the Nyquist frequency, for SS-PWM, and a higher mismatch from the analytical modeling is seen compared to the results presented above. This can be partly due to the use of Z-domain modeling in [148], which fails around the Nyquist frequency.

To conclude, the results of this section have shown that MS-PWM is capable of rendering the admittance strictly passive in a wide frequency range, which, incidentally, provides compliance with the standard [152] without any active damping. Some impact of the MS-PWM nonlinearities is present; however, its nature is not found to be detrimental for passivity properties.

6.4.4 Results for DS-PWM with AD

In this section, active damping strategies are introduced, and the corresponding conductance measurements are given for $L = 1.5$ mH and $\alpha = 0.2$.

The first method considered for comparison is D-AD [135], which extends passivity up to the NF by adding a derivative feedforward of v_{pcc} to the controller output:

$$H_{ad}(s) = sk_{ad}. \tag{6.8}$$

The AD gain design is based on the procedure from [135]. Calculating the real part of (6.4) with H_{ad} from (6.8), for a proportional controller and without the feedback filter, yields the same expression as (6.7) multiplied by $\left(1 - k_{ad}\frac{\omega^2}{\omega_c}\right)$. The active damping gain k_{ad} is chosen such that this added term changes its sign at the same frequency as the cosine term in (6.7), i.e.:

$$k_{ad} = \frac{4\tau_D^2}{\pi^2}\omega_c. \tag{6.9}$$

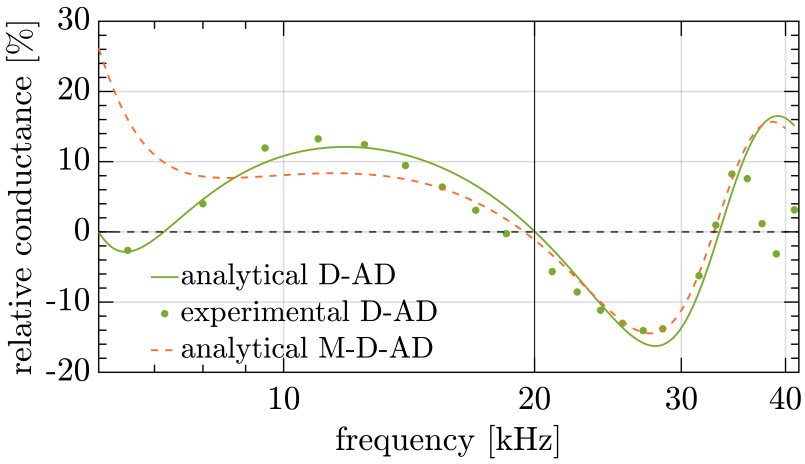


Figure 6.13: Relative conductance for DS-PWM with D-AD: $N = 2$, $N_{ad} = 16$, $H_{ad} = \frac{k_{ad}}{T_{s,1}}(1 - z_1^{-1})$, $L = 1.5$ mH, and $\alpha = 0.2$. Orange dashed line shows the impact of including the additional filter H_{bq} from (6.10) in cascade with the derivative gain [135]. The vertical line marks the switching (and the Nyquist) frequency. The results are measured without the output bias voltage.

For all subsequent experimental tests employing AD, the gain k_{ad} is calculated using (6.9). In [135], it is shown that, for passivity up to the NF, the derivative action must be implemented in the analog domain, or using oversampling. The latter approach is chosen here, in order to keep the implementation fully digital. Backward-Euler discretization is chosen, as advised in [135]. Referring to Fig. 6.1b, D-AD is implemented with $N = 2$, $N_{ad} = 16$, $H_{ad}(z_1) = k_{ad}f_{s,1}(1 - z_1^{-1})$. The AD oversampling factor was chosen to be as high as allowed by the control platform.

The relative value of the measured conductance for D-AD is shown in Fig. 6.13. A very good match with the s-domain analytical results is obtained, apart for frequencies very close to f_s. It is supposed

that this mismatch comes from not including the modulation and sampling sideband effects [73]. The results in Fig. 6.13 confirm that D-AD is capable of improving passivity up to the NF[6]. It can be seen that, above the NF, a non-passive zone is introduced with a peak of negative conductance being slightly higher than for the case of DS-PWM without AD (see Fig. 6.6b). In [155], this effect is mentioned, however it is not thoroughly investigated in the literature, even if, from [141], it is clear that admittance properties above the NF need to be examined.

D-AD (as well as M-D-AD) was also tested for other values of the derivative gain (by multiplying k_{ad} from (6.9) with a factor K) and the corresponding analytical results are shown in Fig. 6.14. For reference, the M-D-AD filter H_{bq} is designed in s-domain based on the approach from [135]:

$$H_{ad}^{\mathrm{M-D-AD}}(s) = sKk_{ad} \cdot H_{bq}(s) = sKk_{ad} \cdot \frac{s^2 + 2\xi_z\omega_z s + \omega_z^2}{s^2 + 2\xi_p\omega_p s + \omega_p^2}, \tag{6.10}$$

where $\omega_p = 0.1 \cdot 2\pi f_s$, $\omega_z = 0.2 \cdot 2\pi f_s$, $\xi_p = 2$, $\xi_z = \frac{\omega_p\left((2\pi f_s)^2 - 4\omega_z^2\right)}{\omega_z\left((2\pi f_s)^2 - 4\omega_p^2\right)}$. For both D-AD and M-D-AD, the trend is that higher values of k_{ad} add more positive damping in the frequency region from $\frac{f_s}{6}$ to the NF and more negative damping in the region above the NF, where the peak negative conductance is found. Lower values of k_{ad} decrease the peak negative conductance above the NF; however, passivity is not achieved around $\frac{f_s}{6}$. From the presented results, it can be concluded that for some applications it may be favorable to choose a lower value of k_{ad}, in order to suppress the emphasized negative peak above the NF, which, in the following section, will be shown to bring stability issues. Additional considerations regarding AD design are out-of-scope of this thesis and are left for future research.

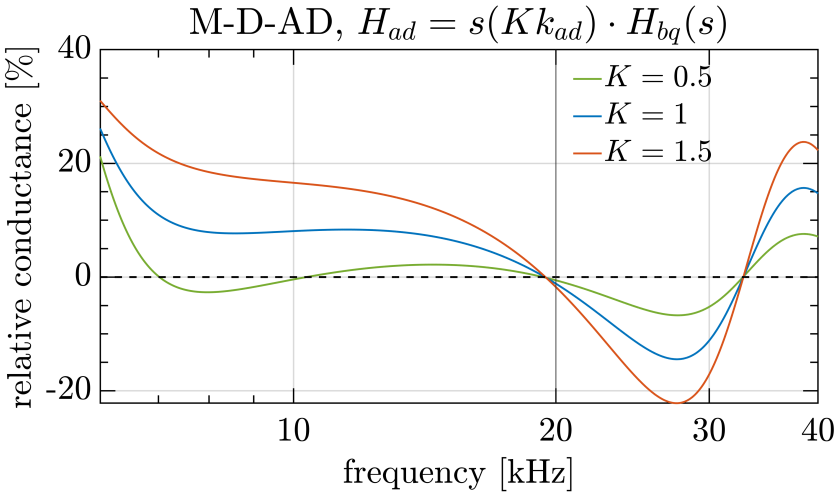


Figure 6.14: Impact of the AD derivative gain on the conductance for DS-PWM with M-D-AD, for $L = 1.5$ mH and $\alpha = 0.2$. The vertical line marks the switching (and the Nyquist) frequency.

[6]In [135], an additional biquad filter H_{bq} is added in cascade with the derivative action, which is referred to as the modified active damping (M-D-AD). This filter adds damping to the narrow non-passive zone around $\frac{f_s}{6}$ that remains when a purely derivative H_{ad} is used. It is not included for the experimental comparison in this chapter as it lacks a standardized design procedure [149] and its impact above the NF, where robustness of D-AD is tested, is negligible. However, it is important to note that M-D-AD can fully passivize the admittance below the NF. The analytical trace corresponding to M-D-AD is shown in Fig. 6.13 using the orange dashed line.

Second AD method compared, DD-AD, uses the same derivative action as D-AD, however, without the oversampling: $N = 2$, $N_{ad} = 2$, $H_{ad}(z) = k_{ad} f_s (1 - z^{-1})$. DD-AD is analyzed in [148], with a specific parameter design procedure. However, it was verified that implementing the derivative gain as (6.9) brings practically the same results, without needing to use one fixed value of bandwidth as in [148]. In [148], Z-domain modeling was used to predict the impact of DD-AD on the admittance, which yielded a significant mismatch as frequencies approached the NF. Hence, here, H_{ad} is directly transformed to s-domain, using $z = e^{sT_s}$. The results are reported in Fig. 6.15. It can be seen that a good match between the experiments and the analytical results is obtained, in the same frequency range as in Fig. 6.6 and Fig. 6.13. From Fig. 6.15, it can be seen that DD-AD improves passivity at medium frequencies; however, above approximately $\frac{f_s}{3}$, the passivity is lost. The same frequency limit is reported in papers that use single-loop AD, by adding a derivative gain to the controller structure [153]. Note that the negative conductance peak for DD-AD is slightly reduced compared to the case of DS-PWM without AD.

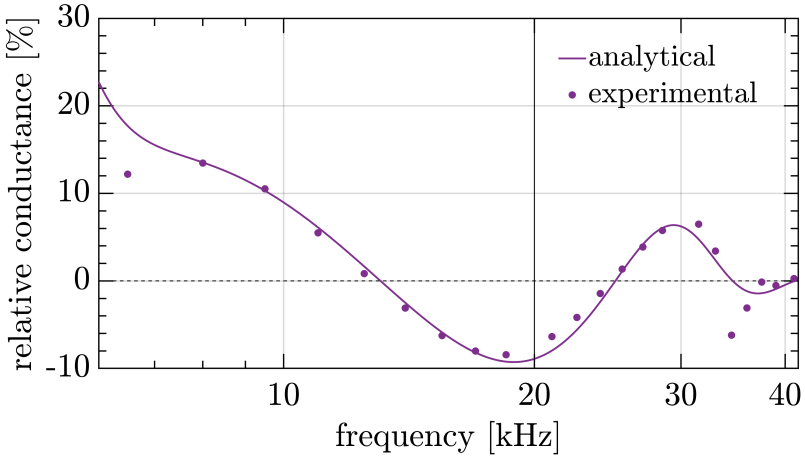


Figure 6.15: Relative conductance for DS-PWM with DD-AD: $N = 2$, $N_{ad} = 2$, $H_{ad} = \frac{k_{ad}}{T_{s,1}}(1 - z_1^{-1})$, $L = 1.5$ mH, and $\alpha = 0.2$. The vertical line marks the switching (and the Nyquist) frequency. The results are measured without the output bias voltage.

In [73], admittance properties for DS-PWM without AD are examined for many steady-state values of D. It is found that, as D approaches extreme values, the negative conductance peaks become less emphasized, which can be predicted by including the full DPWM model from (2.3). To illustrate this, Fig. 6.16 is given to show the impact of D for DS-PWM with and without AD. It can be seen that the negative conductance peaks are highest for $D = 0.5$. The duty cycle dependence is most evident for the case of D-AD. Based on these results it can be concluded that, for the sinusoidal ac operation, the highest introduced negative damping is expected around the zero crossings of v_g, where $D = 0.5$. This is validated in time-domain experimental tests shown in Section 6.5.2.2 (see Fig. 6.30i).

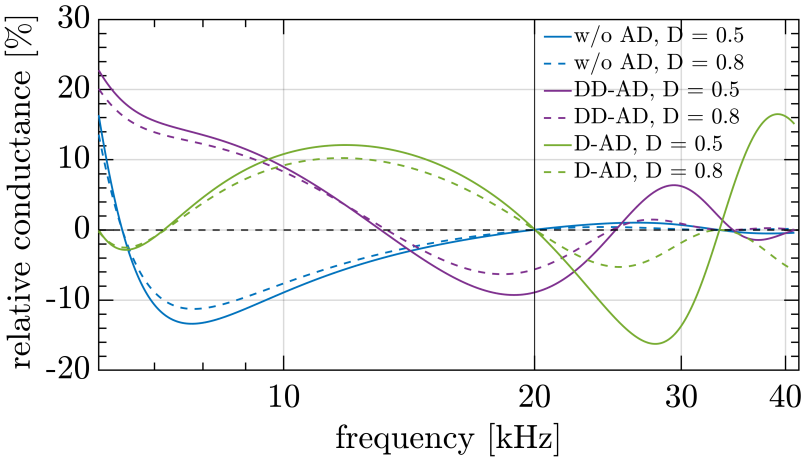


Figure 6.16: Comparison of the operating point impact on the conductance for DS-PWM with and without AD, for $L = 1.5$ mH and $\alpha = 0.2$. The vertical line marks the switching (and the Nyquist) frequency.

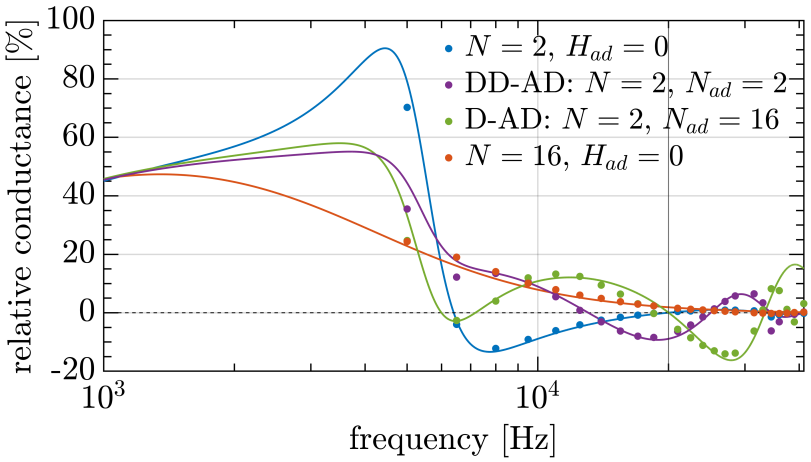


Figure 6.17: Comparison of conductances for all tested control strategies: $L = 1.5$ mH, $\alpha = 0.2$. The vertical line marks the switching frequency. The results are measured without the output bias voltage.

6.4.5 Comparison of effectiveness

In Fig. 6.17, conductances for all tested cases are shown in a wider frequency range. It can be seen that both D-AD and DD-AD are able to extend the passive zone; however, for both methods, another emphasized non-passive zone is introduced. This points to the fact that the addition of AD only shifts the non-passive zone to higher frequencies and can, therefore, compromise stability, instead of guaranteeing it. It is important to note that these non-passive zones are found in the frequency range where the single-frequency admittance models predict well the experimentally-measured VSC responses. This is important as it can be assumed that assessing stability using the Nyquist criterion most-likely yields correct conclusions, which is validated in the following section. MS-PWM shows a natural drop towards zero conductance, where Y_i starts to behave as an inductor. A summary of the measured conductances

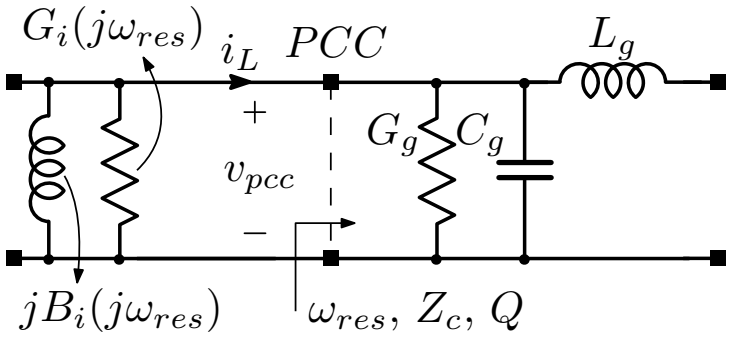


Figure 6.18: Impedance network at the frequency of the grid anti-resonance. The VSC admittance is represented as $Y_i(j\omega_{res}) = G_i(j\omega_{res}) + jB_i(j\omega_{res})$. Grid impedance features passive damping, represented by G_g.

is shown in Table 6.1, by providing peaks of negative values and frequencies for which they are found. The results are given for $\alpha = 0.2$ and both tested inductances. For MS-PWM and $N = 16$, the analytical model predicts the non-passive zone to fall outside of the measurement range.

Table 6.1: Comparison of conductance minimums and frequencies for which they are found: $min\{\mathrm{R_e}\{\mathrm{Y_i}\}\}$ [%] @ f_{min} [kHz]. The results are given for the relative bandwidth $\alpha = 0.2$.

PWM	DS-PWM			MS-PWM
AD	w/o AD	D-AD	DD-AD	w/o AD
$L = 1.5$ mH				
measured	-12.2 @ 8	-14.1 @ 27	-8.4 @ 18.5	-0.2 @ 36
analytical	-13.4 @ 7.8	-16.2 @ 27.9	-9.3 @ 18.9	-0.1 @ 81
$L = 2.5$ mH				
measured	-8.2 @ 8	-7.9 @ 27	-5 @ 18.5	-0.1 @ 36
analytical	-8 @ 7.8	-9.7 @ 27.9	-5.6 @ 18.9	-0.05 @ 81

6.5 Passivity implications in grid-connected scenarios

Impedance-based analysis from Section 6.3 predicts that a VSC can be destabilized if connected to a grid with a certain Z_g. For grid-following VSCs with inductive filters, a parallel anti-resonance that coincides with the non-passive zone of Y_i can cause instability [135]. In this section, operation stability is tested for all strategies compared in Section 6.4, by connecting the same VSC to a grid with a specific Z_g. Results presented in this section hold, in relative terms, also for VSC designs with different switching frequencies. Therefore, irrespective of the specific design parameters, reliable conclusions can be drawn on the robustness ensured by each controller organization.

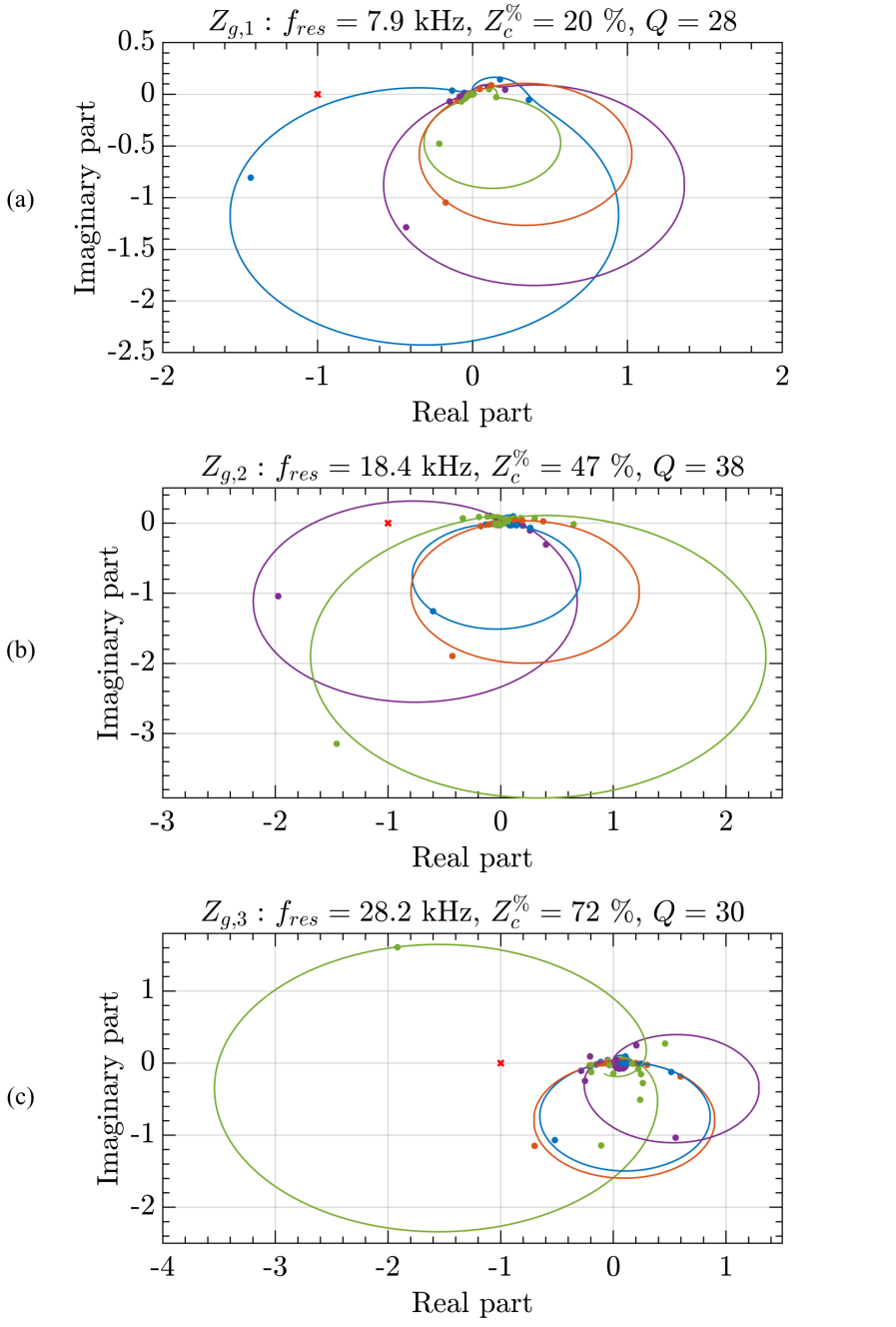


Figure 6.19: Nyquist plots of the minor-loop gain $Y_i(j\omega)Z_g(j\omega)$ for three different grid anti-resonant networks and all compared control strategies. All results are given for $L = 1.5$ mH and $\alpha = 0.2$. The parameters of Z_g correspond to the ones experimentally tested.

6.5.1 Analysis of the equivalent impedance network

Let us suppose that the analyzed VSC is connected to a grid with an anti-resonance formed by L_g and C_g[7]. Grid passive damping can be modeled as a parallel conductance G_g. Such grid impedance can, therefore, be described using its anti-resonant frequency $f_{res} = \frac{\omega_{res}}{2\pi} = \frac{1}{2\pi\sqrt{L_g C_g}}$, characteristic impedance $Z_c = \sqrt{\frac{L_g}{C_g}}$, and quality factor $Q = \frac{1}{Z_c G_g}$. Considering passive damping is important, as a non-passive Y_i does not necessarily destabilize a grid anti-resonance with a realistic value of Q [70].

In this section, VSC connection to three different grid anti-resonant networks is tested. The anti-resonances that coincide with the non-passive admittance zones are formed using an inductor $L_g = 72$ μH and different parallel capacitors C_g. Passive damping is estimated using the procedure described in the following section. The first anti-resonance, corresponding to $Z_{g,1}$, is obtained with $C_g = 5.6$ μF. It is very close to the negative conductance peak for $N = 2$ without AD and its parameters are $f_{res} = 7.9$ kHz, $Q = 28$, $Z_c = 3.6$ Ω, and $G_g^{\%} = 17.6$ %. The second anti-resonance, corresponding to $Z_{g,2}$, is obtained with $C_g = 1$ μF. It is very close to the negative conductance peak for DD-AD and its parameters are $f_{res} = 18.4$ kHz, $Q = 38$, $Z_c = 8.3$ Ω, and $G_g^{\%} = 5.6$ %. The third anti-resonance, corresponding to $Z_{g,3}$, is obtained with $C_g = 440$ nF. It is very close to the negative conductance peak for D-AD and its parameters are $f_{res} = 28.2$ kHz, $Q = 30$, $Z_c = 12.7$ Ω, $G_g^{\%} = 4.6$ %.

The equivalent impedance network at the frequency of the grid anti-resonance is illustrated in Fig. 6.18. At ω_{res}, the VSC input admittance is represented by its conductance $G_i(j\omega_{res})$ and susceptance $B_i(j\omega_{res})$. Intuitively, from Fig. 6.18, it can be concluded that the overall system damping at ω_{res} is impacted by the parallel connection of $G_i(j\omega_{res})$ and G_g. Hence, the value of $G_i(j\omega_{res}) + G_g$ indicates the damping of the anti-resonant network. This intuitive approach is valuable as it allows to predict the stability properties based solely on the admittance measurements, without knowing the analytical expression for Y_i. The formal approach, in case Y_i is analytically known, is to analyze stability using the Nyquist plots of the minor-loop gain. Examples of Nyquist plots, with the analytical and measured data points, are shown in Fig. 6.19, for all tested control strategies and grid impedances, for $L = 1.5$ mH and $\alpha = 0.2$. From Fig. 6.19a, it is clear that, although the anti-resonance $Z_{g,1}$ coincides with the non-passive zone of Y_i for DS-PWM without AD, passive damping of $Z_{g,1}$ is high enough to prevent instability. This can be also concluded from the fact that, for that case, $G_i(j\omega_{res}) + G_g > 0$. The Nyquist plots in Figs. 6.19b and 6.19c predict instability for DD-AD and D-AD, respectively.

6.5.1.1 Experimental measurement of anti-resonant circuit parameters

The grid voltage is formed using Chroma 6460 programmable ac source. Due to the unknown high-frequency damping properties of the ac source, it was of interest to decouple it from the anti-resonant circuit. This was achieved by connecting Chroma via an LC filter with the inductance $L_{ch} = 324$ μH and the capacitance $C_{ch} = 150$ μF. In this way, an almost ideal ac source, at the frequencies of interest,

[7]Note that the specific values of L_g and C_g should not be understood as parts of a properly designed LCL filter, but as anti-resonance forming components that may be found due to, for example, the presence of grid-forming VSCs [162].

was formed. With such a configuration of the reactive elements, two anti-resonant frequencies appear in the circuit. The first one, due to decoupling of the ac source, is found close to 650 Hz and it has no direct implications on the subsequent stability tests.

Passive damping of each of the three tested anti-resonant networks was measured in two ways. First, an impedance analyzer was used to directly measure the network parameters, without connecting the VSC and the ac voltage source. For the anti-resonant networks $Z_{g,1}$, $Z_{g,2}$, and $Z_{g,3}$, the measured values of Q were found equal to $\{44, 60, 72\}$, respectively. The resulting values of Q factors seemed unrealistically high, and their implementation in the simulation model did not bring a good match with the subsequently shown experimental results. It is assumed that this was due to the low magnitude of the imposed perturbation, which was not able to stimulate certain loss mechanisms in the circuit.

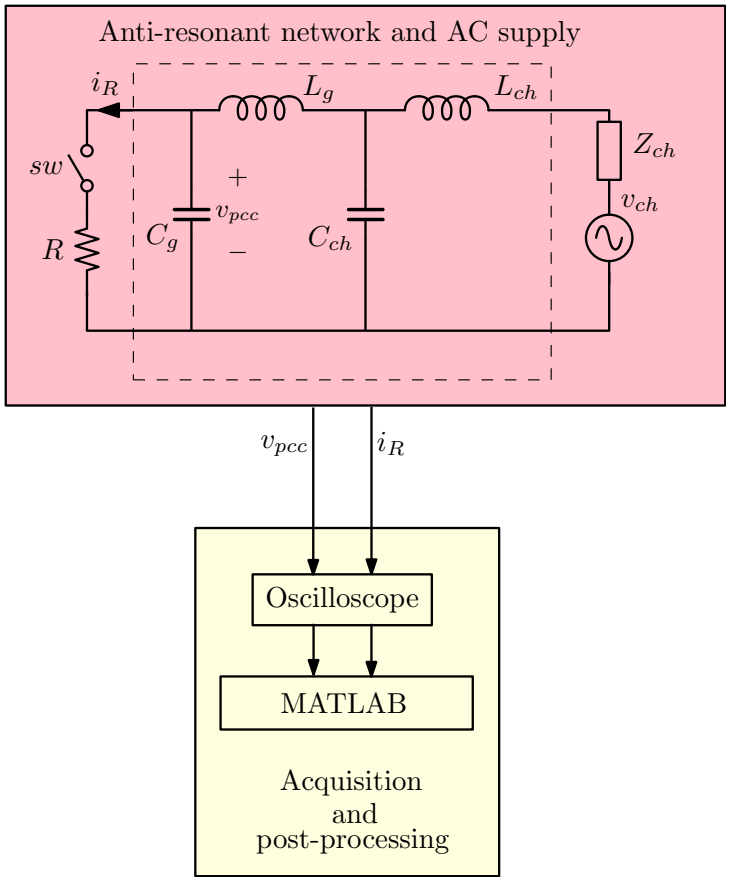
For this reason, Q factors were estimated by triggering an open-loop transient, while the VSC was disconnected. This kind of approach was taken in order to consider also the impact of the ac voltage power supply, due to its unknown damping properties (i.e. its internal impedance Z_{ch}). The schematic of the relevant set-up is shown in Fig. 6.20a. The Chroma voltage source was set to output a sinusoidal voltage with 20 V magnitude and 50 Hz. The resistor $R = 20\ \Omega$ was placed in series with the switch sw. Near the peak of the voltage v_{pcc}, the switch was turned off, which resulted in a transient due to the current i_R becoming equal to 0. Correspondingly, v_{pcc} was acquired using the oscilloscope and plotted in MATLAB, in order to estimate damping of the triggered oscillations. Passive damping, i.e. the Q factor, of the anti-resonant networks was calculated based on the measured time constant of the exponential decay as:

$$Q = \frac{\pi f_{res} \tau}{2}, \tag{6.11}$$

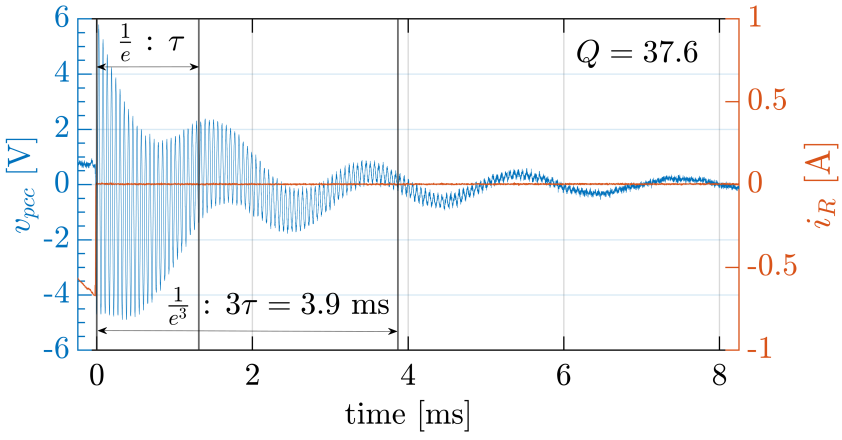
where τ is the time needed for the oscillation magnitude to decay by the factor of e. An example of the measurement procedure for $Z_{g,2}$ is shown in Fig. 6.20b. In Fig. 6.20b, a lower-frequency oscillation is visible, which appears to be due to the above-mentioned Chroma decoupling LC filter. The 50 Hz component is removed from the voltage waveform, for a better visualization of the decayed oscillatory response. For the tested anti-resonant networks $Z_{g,1}$, $Z_{g,2}$, and $Z_{g,3}$, the estimated values of Q are equal to $\{28, 38, 30\}$, respectively. These values were verified in simulations, which closely matched the subsequently shown experimental responses.

6.5.2 Tests for various grid anti-resonances

The objective of this section is to verify the implications of connecting a VSC with a non-passive input admittance to a grid with an anti-resonance that coincides with the non-passive region. The VSC works as a rectifier with a unity power factor, as the used Chroma power supply does not support regenerative operation. The output frequency is $f_1 = 50$ Hz, and the PLL is implemented with 5 Hz bandwidth. The schematic of the grid-connected scenario is shown in Fig. 6.21.



(a)



(b)

Figure 6.20: (a) Circuit used for measuring passive damping of the tested anti-resonant networks. (b) Measured response for $Z_{g,2}$; the fundamental component of v_{pcc} is filtered out for a better visualization.

6.5.2.1 Comparison between MS-PWM and DS-PWM without AD

In this section, the operation is tested for $N = \{2, 4, 32\}$, two values of the relative crossover frequency $\alpha = 0.1$ and $\alpha = 0.2$, and two values of the filter inductance, $L = 1.5$ mH and $L = 2.5$ mH. The two inductors feature the same core properties and similar winding resistances, yielding comparable losses.

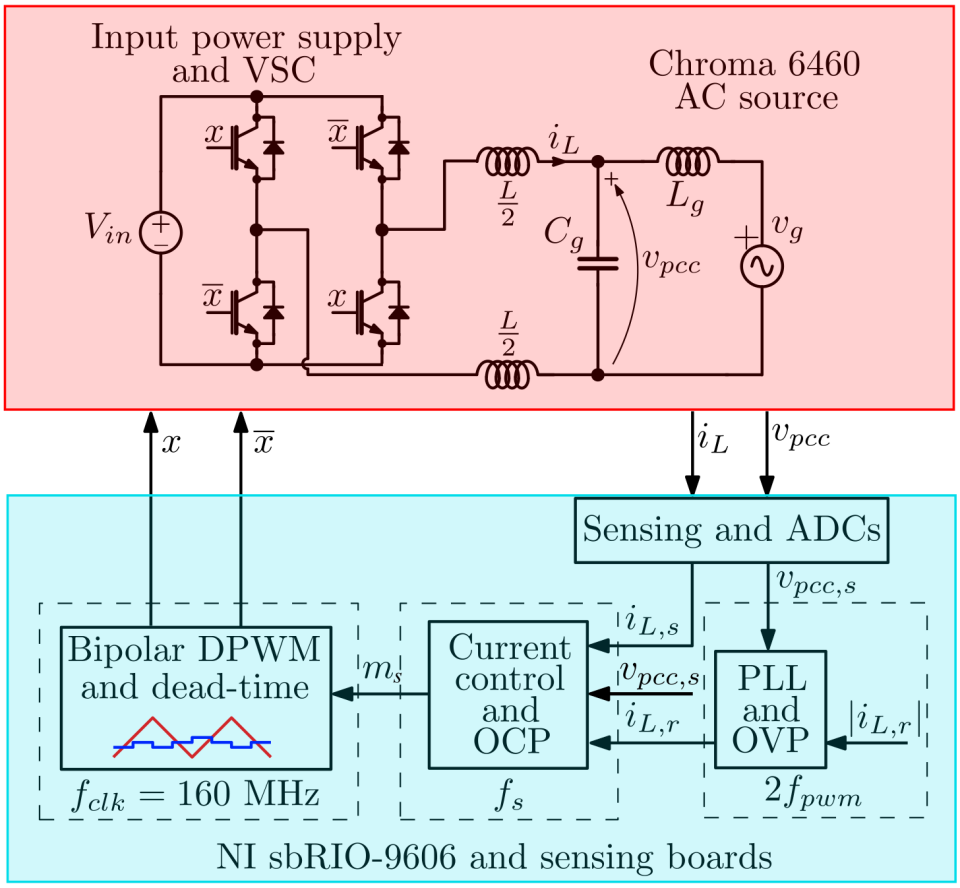


Figure 6.21: Illustration of the grid-connected set-up. The grid anti-resonance appears due to the presence of C_g and L_g. In blue part, OCP and OVP stand for over-current and over-voltage protection, respectively.

Tests in this section are performed for the grid impedance $Z_{g,1}$. The corresponding anti-resonance appears at $f_{res} = 7.9$ kHz, which is very close to the frequency where the IFP is found for $N = 2$. For the other tested values of N, MS-PWM renders the admittance passive around f_{res}. To illustrate the impact of the tested values of L and α on the negative damping introduced by the VSC, for DS-PWM without AD, Fig. 6.22 shows the real part of Y_i. The small-signal modeling predicts that the configuration with the higher bandwidth and the lower inductance will have the worst impact on stability. Based on Fig. 6.19a, even for the case with the highest negative damping ($L = 1.5$ mH and $\alpha = 0.2$), instability is not expected.

The experimental results show oscilloscope measurements of one fundamental period of i_L (blue trace) and v_{pcc} (red trace). A transient is triggered by imposing the step change of the current magnitude reference from 4 A to 12 A. The reference step is synchronized with the instant where the current is at its peak value. To test the impact of various system parameters on damping, results are also given for two settings of the input/output voltages: $V_{in} = 400$ V and $v_{pcc,RMS} = 230$ V, and $V_{in} = 250$ V and $v_{pcc,RMS} = 110$ V.

In Fig. 6.23, results are shown for the case of $N = 2$, $\alpha = 0.2$, $L = 1.5$ mH, $V_{in} = 400$ V, and

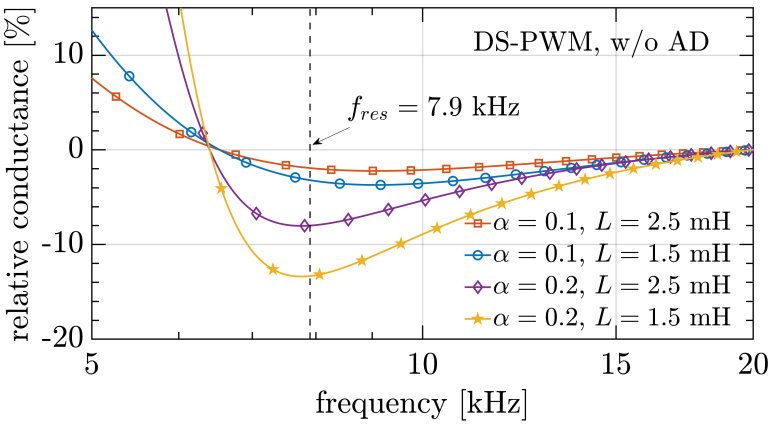


Figure 6.22: Real part of the VSC input admittance Y_i for DS-PWM, the two tested inductances L, and the two tested relative bandwidths α.

$v_{pcc,rms} = 230$ V. For all tested cases with $N = 2$ and $\alpha = 0.2$, the phase margin is around 30°, which results in a step response overshoot. This bandwidth setting, corresponding to 10 % of the sampling frequency, is used for experimental results in [135] and a slightly higher one is used in [148]. When the reference step change is imposed, the oscillations at the anti-resonant frequency are evident, especially in the v_{pcc} trace. After nearly half of the fundamental period, the oscillations are fully damped due to the non-negligible passive damping of the grid anti-resonant circuit. Note also the additional presence of a lower frequency oscillation in v_{pcc}, corresponding to the before-mentioned ac source decoupling.

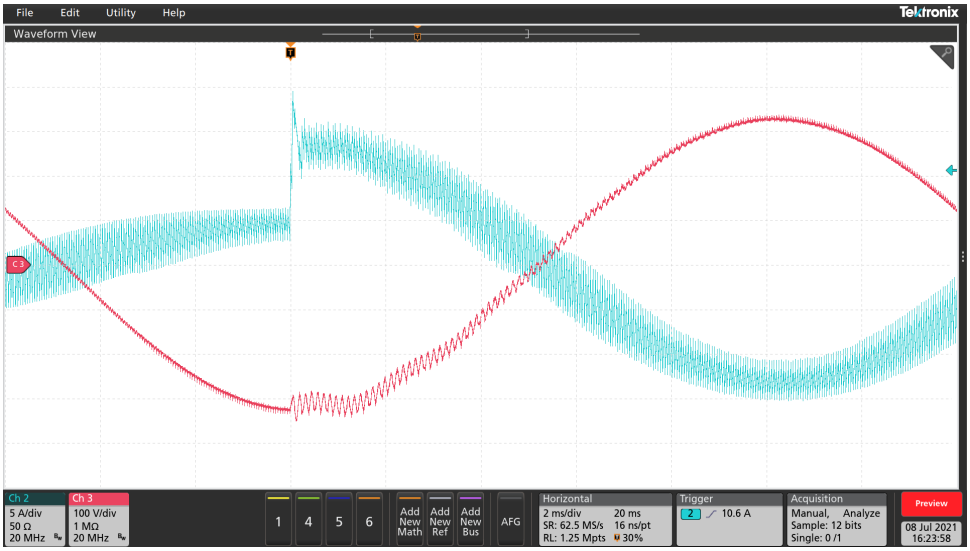


Figure 6.23: Experimental tests of the grid-connected scenario. Reference current magnitude is changed from 4 A to 12 A. System parameters are: $N = 2$, $\alpha = 0.2$, $L = 1.5$ mH, $V_{in} = 400$ V, and $v_{pcc,rms} = 230$ V.

For the subsequent test, shown in Fig. 6.24, DS-PWM is again used with $\alpha = 0.2$ and $L = 1.5$ mH. However, the voltages are changed to $V_{in} = 250$ V, and $v_{pcc,rms} = 110$ V. It can be seen that much stronger oscillations are triggered, but again, parasitic resistances of the experimental anti-resonant

impedance $Z_{g,1}$ prevent the full system instability to occur. The reason for stronger oscillations is consistent with the previously mentioned impact of D on admittance properties. Namely, for the configuration with $V_{in} = 400$ V, and $v_{pcc,rms} = 230$ V, the maximal value of D is equal to approximately 0.91, while for $V_{in} = 250$ V, and $v_{pcc,rms} = 110$ V, it is equal to 0.81. Given that the first negative conductance peak is decreased as values of D approach extreme values (see Fig. 6.16 and [73]), the oscillations are more damped. For all subsequent tests, the configuration with $V_{in} = 250$ V and $v_{pcc,rms} = 110$ V is chosen to enable a more critical scenario regarding stability.

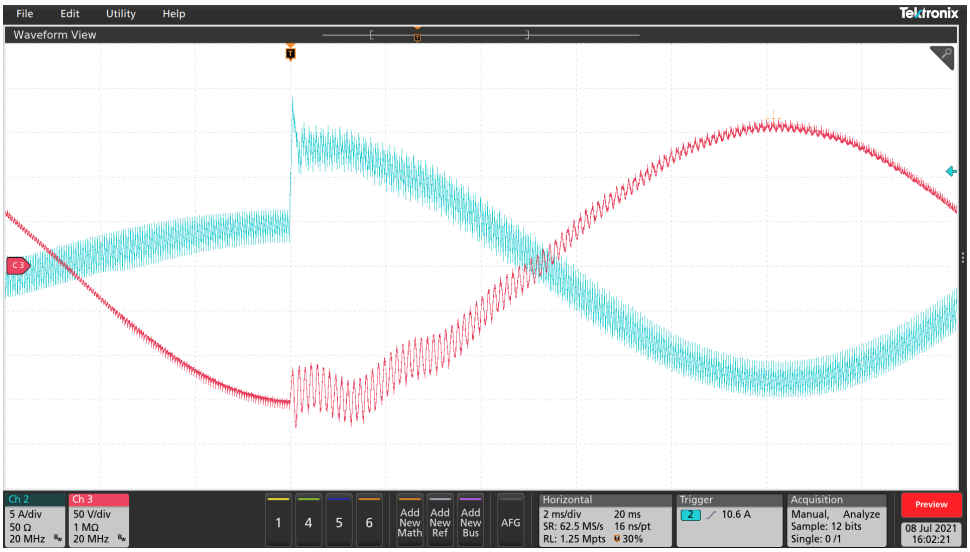


Figure 6.24: Experimental tests of the grid-connected scenario. Reference current magnitude is changed from 4 A to 12 A. System parameters are: $N = 2$, $\alpha = 0.2$, $L = 1.5$ mH, $V_{in} = 250$ V, and $v_{pcc,rms} = 110$ V.

In Fig. 6.25, results are shown for the case of the higher inductance: $N = 2$, $\alpha = 0.2$, $L = 2.5$ mH, $V_{in} = 250$ V and $v_{pcc,rms} = 110$ V. It can be seen that much stronger resonance damping is present than in Fig. 6.24. Since the two cases feature the same crossover frequency and phase margin, the only difference in damping comes from the more favourable passivity measures of VSCs with higher values of L, as predicted by Fig. 6.22.

To show the impact of reducing the bandwidth, the results in Fig. 6.26 are shown for the case of $N = 2$, $\alpha = 0.1$, $L = 1.5$ mH, $V_{in} = 250$ V and $v_{pcc,rms} = 110$ V. It can be seen that oscillations are strongly damped compared to the case with the same parameters except for a higher α, seen in Fig. 6.24.

To verify the positive impact of MS-PWM, the control systems with $N = 4$ and $N = 32$ were tested for the most critical system configuration: $\alpha = 0.2$, $L = 1.5$ mH, $V_{in} = 250$ V, and $v_{pcc,rms} = 110$ V. The results are directly comparable to the one seen in Fig. 6.24. For $N = 4$, the results are shown in Fig. 6.27. It can be seen that, compared to the double-update case, the triggered oscillations are fully damped in a significantly shorter time. For $N = 32$, the results are shown in Fig. 6.28 and it is clear that the damping is even higher.

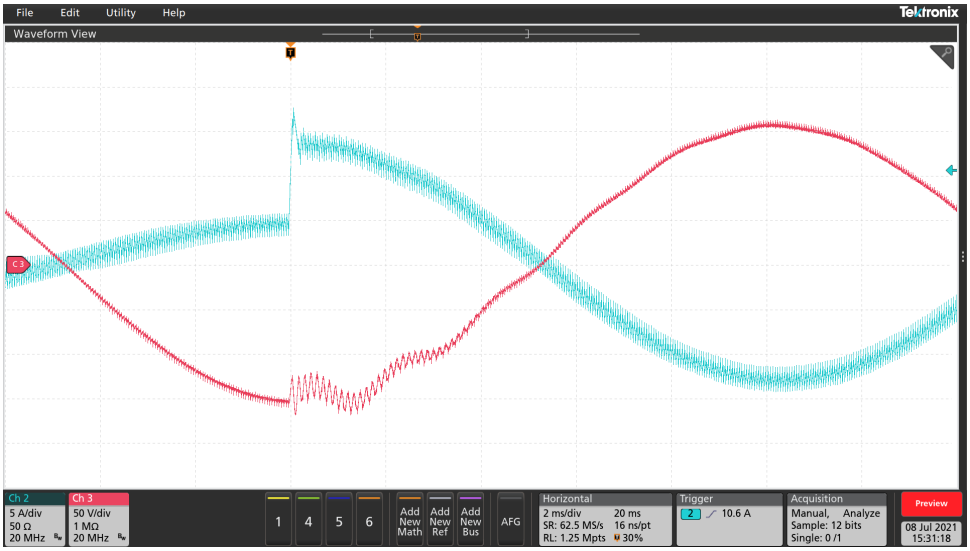


Figure 6.25: Experimental tests of the grid-connected scenario. Reference current magnitude is changed from 4 A to 12 A. The control system parameters are: $N = 2$, $\alpha = 0.2$, $L = 2.5$ mH, $V_{in} = 250$ V, and $v_{pcc,rms} = 110$ V.

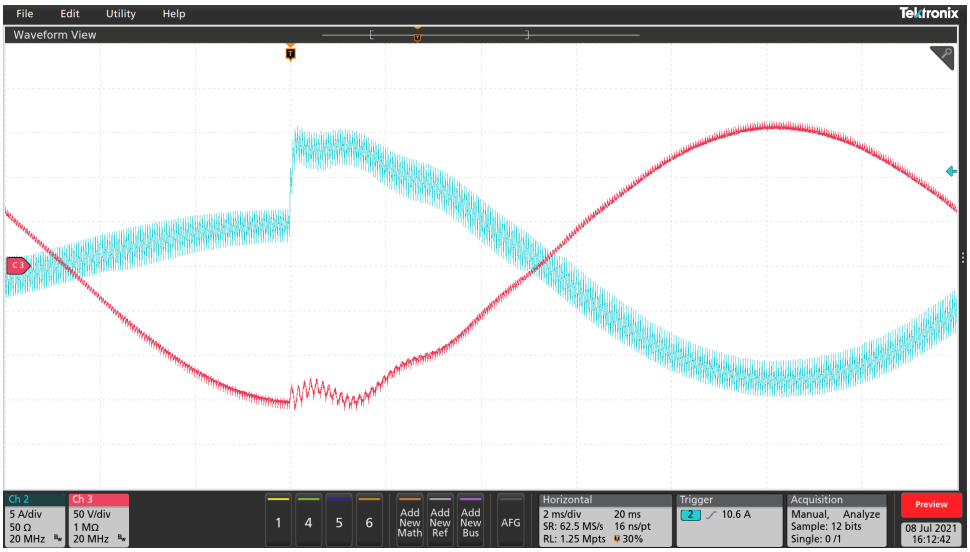


Figure 6.26: Experimental tests of the grid-connected scenario. Reference current magnitude is changed from 4 A to 12 A. System parameters are: $N = 2$, $\alpha = 0.1$, $L = 1.5$ mH, $V_{in} = 250$ V, and $v_{pcc,rms} = 110$ V.

The experimental results are consistent with the analytical prediction of the impact of N, L, and α on the introduced negative damping. For the tested impedance $Z_{g,1}$, transients trigger oscillations at the anti-resonant frequency; however, the system instability does not occur. This confirms that passivity is not a necessary condition for the system stability, as damped grid resonances can compensate the non-passive input admittance of the VSC.

Two positive aspects of MS-PWM are seen from the presented results. Firstly, due to delay reduction, for the same crossover frequency, the phase margin is improved compared to $N = 2$, which can be seen from the step response. Secondly, MS-PWM renders the admittance passive, which adds a high damping

to oscillations at the anti-resonant frequency. Therefore, MS-PWM offers the capability of implementing very high bandwidth loops, while the passivity extension is inherently provided, without any additional active damping strategy.

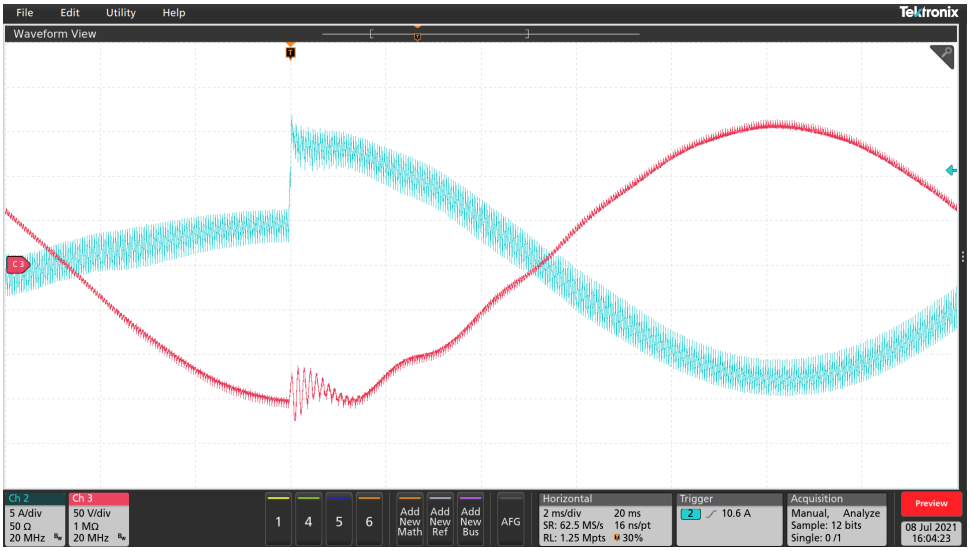


Figure 6.27: Experimental tests of the grid-connected scenario. Reference current magnitude is changed from 4 A to 12 A. System parameters are: $N = 4$, $\alpha = 0.2$, $L = 1.5$ mH, $V_{in} = 250$ V, and $v_{pcc,rms} = 110$ V.

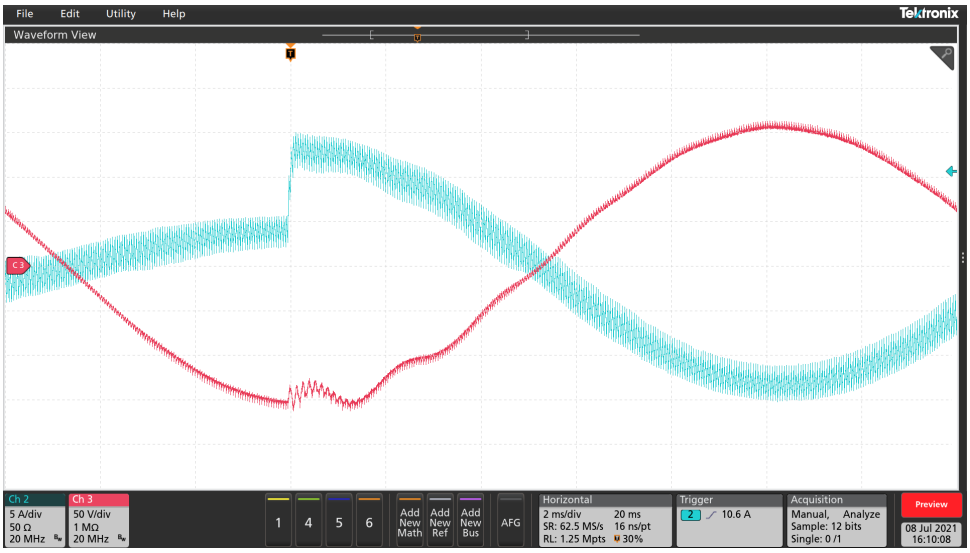


Figure 6.28: Experimental tests of the grid-connected scenario. Reference current magnitude is changed from 4 A to 12 A. System parameters are: $N = 32$, $\alpha = 0.2$, $L = 1.5$ mH, $V_{in} = 250$ V, and $v_{pcc,rms} = 110$ V.

As a final verification, hardware-in-the-loop (HIL) results are given to demonstrate the instability condition in case the VSC is connected to a grid with a high quality factor. These results were not obtainable in the experimental set-up; however, in a general case, the grid resonance can feature very low passive damping. The simulations were organized using the Typhoon HIL 402 HIL platform to

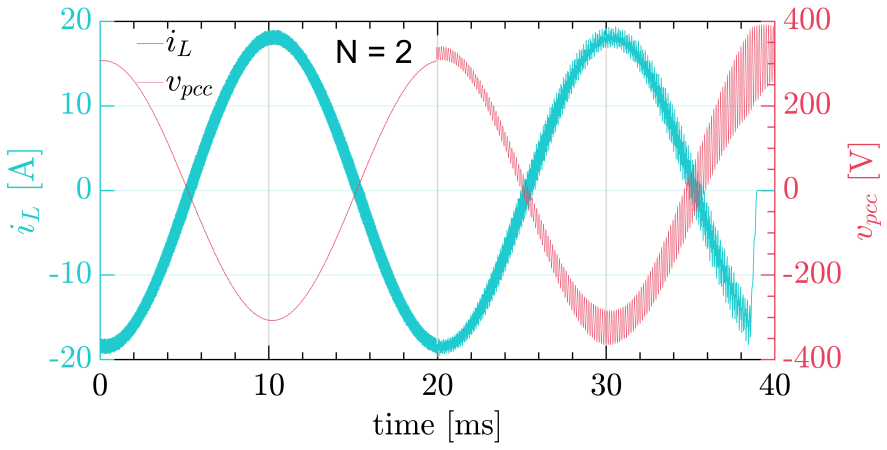
emulate the VSC and the grid, i.e. red part in Fig. 6.21. The inductor current and the PCC voltage are obtained via HIL analog outputs. Sensing, ADC, PLL, current control, and PWM were implemented in the same control platform that was used for the experimental tests, i.e. the blue part in Fig. 6.21 remains unchanged, except for the input signal scaling. Resulting transistor switching signals are connected to HIL digital inputs. In order to verify the consistency of the simulation, all admittance measurements were repeated and results matched those obtained experimentally; hence, admittance properties remain unchanged. For the instability test, the operation is compared between $N = 2$ and $N = 16$ and the chosen system parameters are: $\alpha = 0.2$, $L = 2.5$ mH, $V_{in} = 400$ V, $v_{pcc,rms} = 230$ V, $P = P_n = 3$ kW. The values of L_g and C_g correspond to $Z_{g,1}$. An 1 Ω resistor is placed in series with the grid inductance L_g. At $t = 20$ ms, the resistor is paralleled with another 50 mΩ resistor, in order to reduce the passive damping and observe the resulting transient. The voltage protection is set to turn off the VSC when $|v_{pcc}|$ exceeds 380 V or $|i_L|$ exceeds 25 A. The results are shown in Fig. 6.29. It can be seen that, for $N = 2$, a stable operation cannot be maintained as the grid anti-resonance, which falls into the non-passive admittance region, is no longer damped by the 1 Ω resistor. The protection is triggered at approximately $t = 39$ ms and the VSC is turned off. On the other hand, for $N = 16$ and the same exact test, the operation remains stable and the anti-resonant oscillations are quickly damped.

6.5.2.2 Impact of AD strategies and comparison of effectiveness with MS-PWM

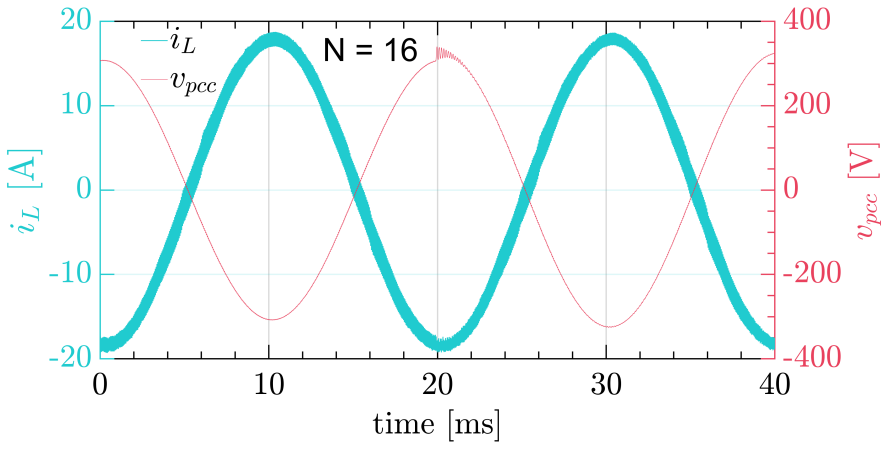
Let us now compare the effectiveness of DS-PWM with the previously analyzed AD strategies and MS-PWM. The operation is tested for $L = 1.5$ mH and $\alpha = 0.2$, and the three anti-resonant networks described in Section 6.5.1. The tested scenarios correspond to the predictions by the Nyquist plots in Fig. 6.19. Voltage levels are set to $V_{in} = 250$ V and $v_{pcc,RMS} = 110$ V.

Results of grid-connected tests are shown in Fig. 6.30. The oscilloscope screen shows i_L (orange) and v_{pcc} (red). Each column in Fig. 6.30 shows results for one of the tested grid anti-resonant networks. Note that the switching ripple in v_{pcc} changes for different Z_g configurations. In the first two rows, the results are shown for the case of MS-PWM with $N = 4$ and $N = 16$, which enable a stable operation for all the tested anti-resonances. A transient is imposed by stepping the current reference from 4 A to 15 A, at the peak of the fundamental component. The results for $N = 4$ are given to show that it is not always necessary to raise N to very high values. Note that, based on the measurements from Section 6.4.3, MS-PWM with $N = 4$ results in a small non-passive zone around f_{pwm}, which coincides with the anti-resonance $Z_{g,2}$. However, the negative conductance is very small and the passive grid damping is enough to compensate it.

In the third row of Fig. 6.30, results are shown for DS-PWM strategies that feature non-passive zones, which coincide with the correspondingly tested anti-resonances. In Fig. 6.30g, strong anti-resonant oscillations are triggered; however, as predicted by Fig. 6.19a, due to a sufficiently high passive damping of $Z_{g,1}$, instability is prevented. In Figs. 6.30h and 6.30i, instability occurs for AD strategies, as predicted by Figs. 6.19b and 6.19c. For these anti-resonances, DS-PWM without AD is stable, which



(a)



(b)

Figure 6.29: HIL tests of the grid-connected scenario. The 1 Ω resistance, placed in series with L_g, is paralleled with a 50 mΩ resistor at $t = 20$ ms. System parameters are: $\alpha = 0.2$, $L = 2.5$ mH, $V_{in} = 400$ V, $v_{pcc,rms} = 230$ V, and: (a) $N = 2$, (b) $N = 16$.

is used to impose transients by activating the respective AD strategy. In Fig. 6.30h, the overvoltage protection is triggered when DD-AD is activated, and the VSC is turned off. In Fig. 6.30i, when D-AD is activated, the protection is not triggered; however, instability clearly occurs and the controller output bounces from positive to negative saturation limits. From Fig. 6.30i, it is clear that oscillations are much more emphasized around the zero crossings of v_{pcc}, where $D = 0.5$. This is in agreement with the comments made in Section 6.4.4 regarding the impact of the operating point on the negative conductance peak. Note that this case corresponds to instability caused by an anti-resonance above the NF. Its enabling mechanism is the coupling between the sampling and modulation sidebands, which allows the controller to react to a disturbance even above the NF [141]. In the fourth row of Fig. 6.30, zoomed-in waveforms corresponding to the third row are given to show that the oscillations are triggered at the anti-resonant frequency.

It is concluded that the implementation of DS-PWM with AD may destabilize the operation for

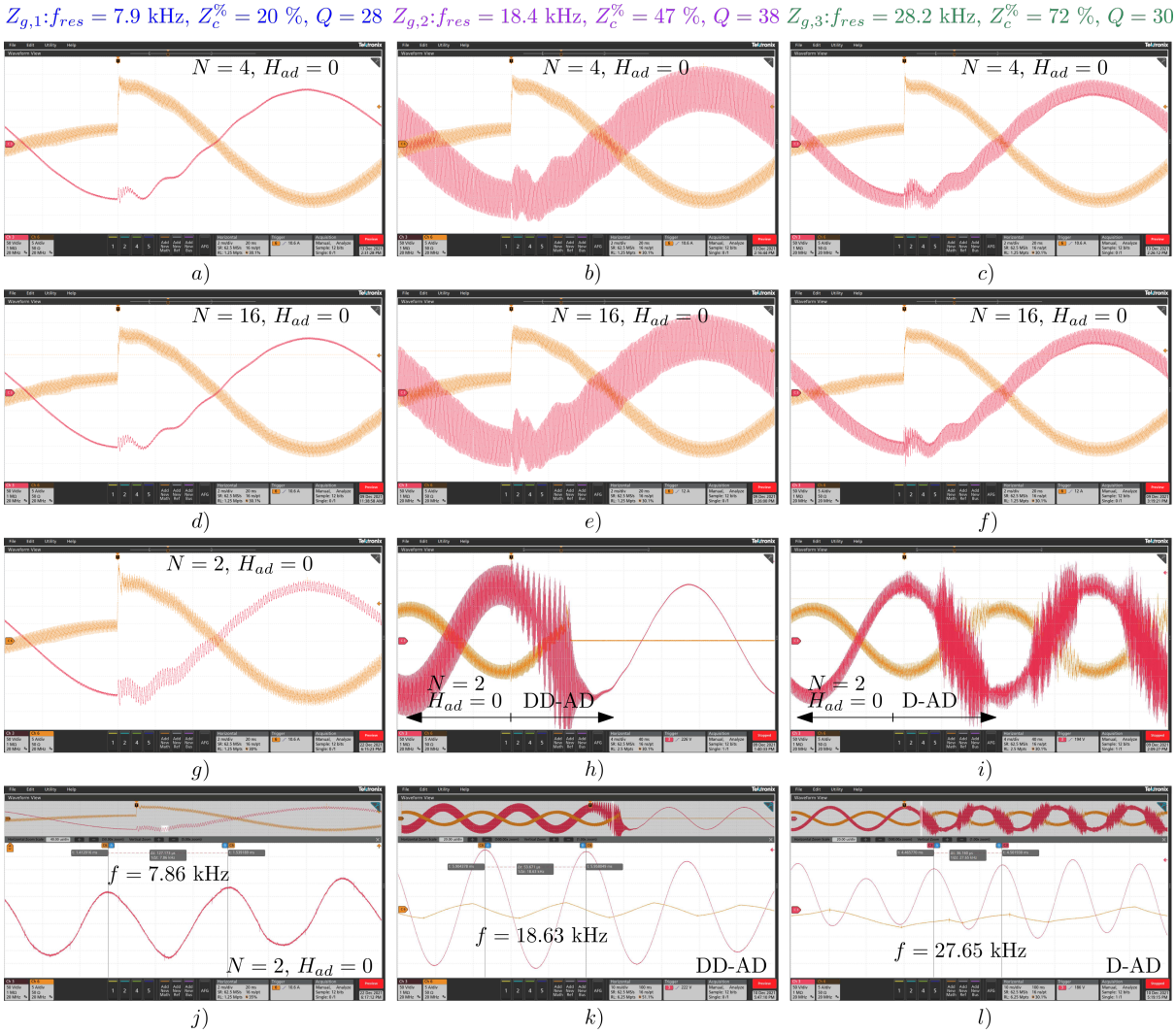


Figure 6.30: Experimental demonstration of passivity implications in grid-connected scenarios. Orange line shows i_L and red line shows v_{pcc} that has a variable ripple depending on C_g. Each column features results for one of the tested grid anti-resonant networks, described in Section 6.5.1. The results are shown as transient responses to: (a), (b), (c) the step current reference change for MS-PWM with N = 4; (d), (e), (f) MS-PWM with $N = 16$; (g) DS-PWM without AD with non-passive zone of Y_i coinciding with $Z_{g,1}$ anti-resonance; the transient causes strong oscillations at f_{res} but the passive grid damping prevents instability; (h) the operation change from DS-PWM without AD to DD-AD; due to a weakly-damped $Z_{g,2}$ anti-resonance, coinciding with the non-passive zone of Y_i, instability occurs and the protection is triggered; (i) the operation change from DS-PWM without AD to D-AD; due to a weakly-damped $Z_{g,3}$ anti-resonance, coinciding with the non-passive zone of Y_i, instability occurs; (j), (k), (l) zoomed-in waveforms from the row above, showing the oscillation frequencies.

certain grid anti-resonances. Hence, AD *does not guarantee stability* of a grid-connected VSC for any passive grid impedance. On the other hand, MS-PWM retains stability for all tested cases.

6.5.2.3 Some considerations on validity of single-frequency models

As previously mentioned, the modeling approach used in this chapter does not include the impact of the sidebands generated by the sampling and the modulation. Some of the reasoning behind this is given

below.

First of all, the single-frequency model offers a good prediction of VSC behavior in the frequency range of interest (up to at least 1.5 f_{pwm}). This is validated based on the match with the admittance measurements as well as the grid-connected stability tests. Secondly, multi-frequency models are successfully derived only for single-loop controllers without AD. Their extension to derivative-based AD is not straightforward as two signals of different harmonic properties are sampled, at possibly different rates, and the application of superposition is questionable due to the nonlinear nature of the multi-frequency system. In [18], the modeling approach offers inclusion of the AD, however, the resulting MIMO model is quite complex and its implementation has resulted in a significant mismatch with the behavior of the analyzed system (whether in simulations or experiments). There is definitely a motivation for deriving a multi-frequency model for the case of AD and correlating it with the grid-connected stability; however, this is out-of-scope of the conducted research on MS-PWM and is, hence, left for future work.

Here, it is investigated how the Nyquist plots change for different models, for DS-PWM without AD. Besides the single-frequency model from (6.4) and the multi-frequency model from [73], it was of interest to see how credible it is to make conclusions regarding stability based only on the equivalent network parameters at the anti-resonant frequency, as in Fig. 6.18. Namely, by considering the VSC admittance only at the anti-resonant frequency, the values of the equivalent resistor and the inductor (if inductive) can be calculated and used to extrapolate Y_i for other frequencies as well. This approach may be of interest as it is based only on one measurement point. In Fig. 6.31, the Nyquist plots are shown for the case of DS-PWM without AD, $L = 1.5$ mH, $\alpha = 0.2$, the first tested grid impedance $Z_{g,1}$, and:

- Experimentally measured points of Y_i, corresponding to Fig. 6.5b.
- Extrapolated trace considering Y_i to be a parallel connection of the equivalent resistor and inductor, obtained at the anti-resonant frequency.
- Multi-frequency model of Y_i from [73].
- Single-frequency model of Y_i, used in the previous sections.

As it can be seen from the Fig. 6.31, all 4 modeling approaches yield very similar Nyquist contours. Although one might argue that the single-frequency model is not mathematically accurate, it is linear and sufficient to give a good insight on a connection stability. Since the focus of this chapter is not on the modeling itself, it was concluded that the fact that all outcomes of the grid-connected tests are predictable by the linear single-frequency models is good enough for the purpose of comparison.

6.6 Noise sensitivity of passivizing current control strategies

A question that arises for AD strategies is their noise sensitivity [159], as the derivative action is applied to v_{pcc}. The goal of this section is to quantify the noise propagation from sensing to the output current i_L, for passivizing control strategies tested beforehand. As seen in Fig 6.1b, noise due to the current

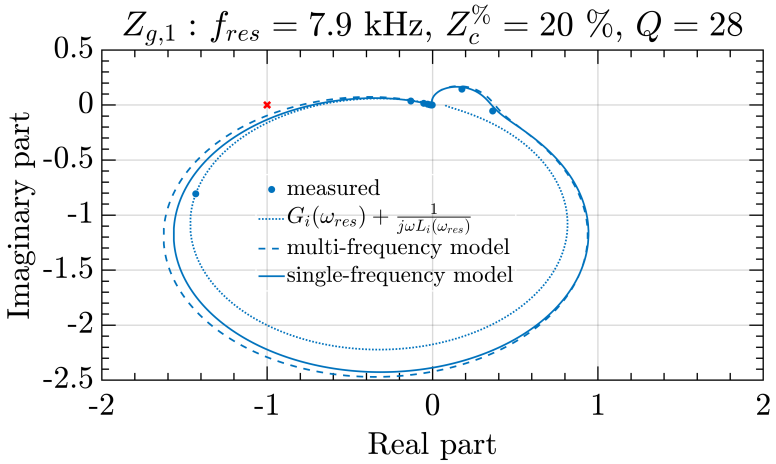


Figure 6.31: Comparison of Nyquist plots for DS-PWM without AD, obtained with various modeling strategies. The results are given for $Z_{g,1}$, $L = 1.5$ mH, and $\alpha = 0.2$.

measurement, n_i, is present for all strategies, while AD brings an additional noise path to the system, from n_v to i_L. Results of this section are based on the analysis from Chapter 5. Again, it is assumed that n_i and n_v are uncorrelated WSS Gaussian white noise signals [127], with corresponding variances labeled as σ_i^2 and σ_v^2.

For all compared strategies, noise propagation due to n_i is determined by:

$$\sigma_{i_L}^2\big|_{n_v=0} = \int_0^{f_x} \sigma_i^2 \frac{2}{f_s} |H_{ni}(f)|^2 df = \int_0^{f_x} S_{ni}(f) df, \tag{6.12}$$

where f_x is the band of interest, $|H_{ni}(f)|^2 = \frac{|W_{ol}(f)|^2}{|1+W_{ol}(f)|^2}$ is the squared magnitude response from n_i to i_L in Fig. 6.1b, and $S_{ni}(f)$ is the PSD of the inductor current, caused by n_i. The PSD is decreased by oversampling the feedback, as determined by f_s. As shown in Section 5.6, the analytical prediction using (6.12) provides good results for SS-PWM and DS-PWM single-loop controllers. For the case of MS-PWM, it is shown that the limiting aspect is the fact that the triangular DPWM behaves as a decimator with frequency $2f_{pwm}$, thus causing aliasing of noise components above f_{pwm}. For this reason, digital anti-aliasing filters are needed to suppress the resulting noise floor below the level determined by DS-PWM.

For AD, noise propagation due to n_v is determined by:

$$\sigma_{i_L}^2\big|_{n_i=0} = \int_0^{f_x} \sigma_v^2 \frac{2}{f_{s,1}} |H_{nv}(f)|^2 df = \int_0^{f_x} S_{nv}(f) df, \tag{6.13}$$

where $|H_{nv}(f)|^2$ is the squared magnitude response from n_v to i_L and $S_{nv}(f)$ is the PSD of the inductor current, caused by n_v. Assuming that the two noise signals are uncorrelated, the total in-band variance of i_L is obtained as an algebraic sum of (6.12) and (6.13) [127].

An interesting fact is that, for the case of D-AD, the white noise n_v is shaped by the active damping filter before being sampled with f_s. In case of the oversampled digital implementation, this corresponds

to the decimation from $f_{s,1}$ to f_s. Let us, for this reason, define $|H_{nv}(f)|^2$ as a product of squared magnitude responses from n_v to the decimator output and from the decimator output to i_L:

$$|H_{nv}(f)|^2 = |H_{ad}^{M:1}(f)|^2 \frac{|G_d(f)G_p(f)|^2}{|1+W_{ol}(f)|^2}, \tag{6.14}$$

where $M = \frac{f_{s,1}}{f_s}$ is the decimation factor and $|H_{ad}^{M:1}(f)|^2$ is the modified squared magnitude response of the AD filter that includes the decimation impact. Given that n_v is a stationary white stochastic signal, it exhibits no spectral correlation and its PSD is constant [130, 175]. As explained in Section 5.5, assuming integer values of M, this allows us to form the equivalent model for the PSD analysis, as in (5.16):

$$|H_{ad}^{M:1}(f)|^2 = \sum_{k=0}^{M-1} |H_{ad}(f - kf_s)|^2. \tag{6.15}$$

For the case of DD-AD, where $M = 1$, $|H_{ad}^{M:1}(f)|^2 = |H_{ad}(f)|^2$. The equivalent squared magnitude response from (6.15) is verified in simulations in Section 5.5.1.2 (see Fig. 5.14).

Individual impacts of (6.12) and (6.13) on the total variance of i_L, for DS-PWM, are illustrated in Fig. 6.32 by showing S_{ni} and S_{nv}, calculated for the input noise powers found in the experimental set-up (see Section 5.6). It can be seen that, for DD-AD, the PSD due to the voltage noise sensing is well below the one due to the current noise sensing; hence, the voltage noise propagation is completely masked and $\sigma_{i_L}^2$ is expected to be the same as for DS-PWM without AD. This outcome is the result of a relatively low required derivative gain k_{ad} in (6.9). For D-AD, however, the derivative in H_{ad} first causes the amplification of the high-frequency noise content, which then gets decimated and folded back to frequencies below the NF. This causes the in-band noise power to significantly increase. From Fig. 6.32 it can be seen that for $N_{ad} = 16$, which is used in this section, the PSDs due to n_i and n_v almost overlap. For $N_{ad} = 32$, n_v has a higher impact than n_i. Note that, for the analog implementation of D-AD, $M \to \infty$ and the impact of n_v is even higher, with the exact amount being dependent on the actual bandwidth of the input noise signal. These conclusions come from the fact that for D-AD, H_{ad} needed to render Y_i fully passive up to the NF, does not include an anti-aliasing filter [135]. In cases where the full passivity up to the NF is not crucial, an anti-aliasing filter can be placed between H_{ad} and the decimator, which would result in a strong noise suppression compared to DD-AD, while offering a similar passivizing effectiveness. This requires additional investigation and is a potential topic of future research. It should be noted that results in Fig. 6.32 are directly proportional to given σ_i^2 and σ_v^2. Hence, for a higher ratio $\frac{\sigma_v^2}{\sigma_i^2}$, D-AD can show an increased sensitivity even for lower values of N_{ad}. However, regarding DD-AD, the PSD line for n_v stays more than 20 dB $\frac{\mathrm{A}^2}{\mathrm{Hz}}$ below the one for n_i, meaning that σ_v^2 should increase more than 100 times to result in a comparable impact, which is not a realistic case. Hence, it can be concluded that DD-AD is not likely to be prone to noise sensitivity.

For the experimental verification, the reference current is set to 5 A RMS and $L = 2.5$ mH is used in order to capture the current signal using the oscilloscope with 2 A/div scale. Larger scale was resulting in the noise floor of the oscilloscope compromising i_L noise measurements. The output variance, up to

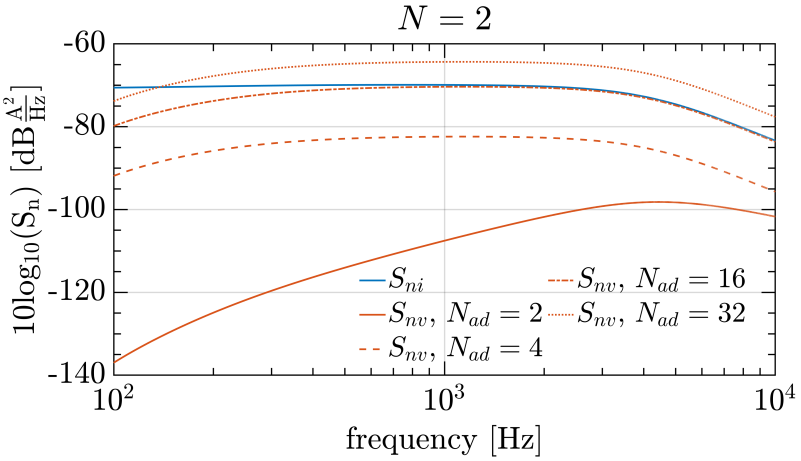
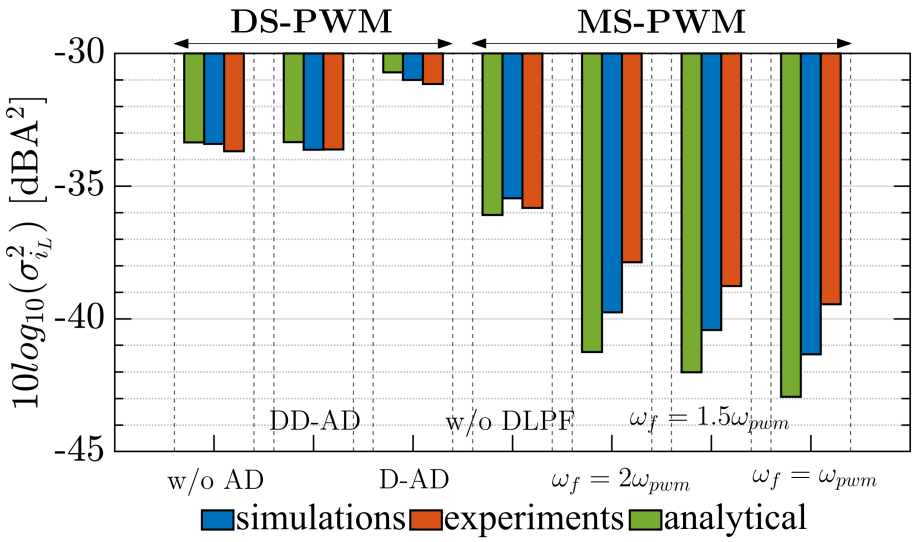


Figure 6.32: Output power spectral densities ($S_n \in \{S_{ni}, S_{nv}\}$) of i_L for DS-PWM due to current noise sensing (blue trace) and voltage noise sensing (red traces). Presented results are calculated for $L = 2.5$ mH, $\alpha = 0.1$, $\sigma_i^2 = 1.7 \cdot 10^{-3}$ A^2, and $\sigma_v^2 = 154 \cdot 10^{-3}$ V^2.

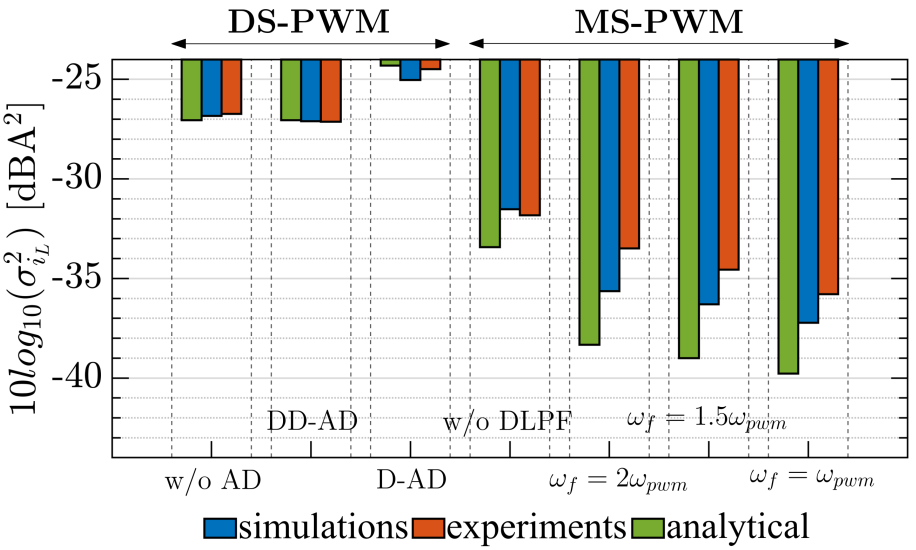
$\frac{f_{pwm}}{2}$, is calculated in MATLAB using 200 ms of the oscilloscope data, sampled with 250 MS/s. For post-processing, the fundamental component of i_L and its harmonics are removed from the spectra, so that distortion does not impact the variance calculations. As a benchmark, simulations are implemented in Simulink using PLECS Blockset, as in Chapter 5. White noise signals are injected, with variances corresponding to the measured σ_i^2 and σ_v^2.

Results that show the output variance $\sigma_{i_L}^2$, for all tested strategies, are presented in Fig. 6.33. The experimental measurements are compared with the simulations and the analytical results. Results in Fig. 6.33a are given for the relative bandwidth $\alpha = 0.1$. First, it can be seen that an excellent analytical prediction is obtained for DS-PWM without AD and with DD-AD. The results show almost the same output noise power for these two strategies. As both cases feature the same magnitude response $|H_{ni}|$, it is concluded that the voltage noise propagation for DD-AD is completely masked by the stronger current noise propagation, which is consistent with Fig. 6.32. For D-AD, the analytical model predicts 2.6 dBA^2 noise power increase, while the simulations and experiments show approximately 2.4 dBA^2 and 2.5 dBA^2 increase, respectively, which supports the validity of the model (6.15). As discussed above, for set-ups that feature a higher ratio $\frac{\sigma_v^2}{\sigma_i^2}$, higher noise sensitivity of D-AD is expected.

Equation (6.12) predicts that, compared to DS-PWM, implementing MS-PWM with $N = 16$ would decrease the output noise power by, at least, a factor 8. The exact amount depends on the impact of delay reduction on $|H_{ni}|$. However, as analyzed in Chapter 5, for $N > 2$ and the high-frequency proportional-dominant controllers, the PSD remains almost unaffected due to the aliasing caused by the DPWM decimation; hence, additional high-frequency digital filtering is needed to enable a strong in-band noise suppression. Here, three DLPFs $G_{fb}(z)$ are tested to observe their impact on noise attenuation. The filter structure corresponds to the one in (4.21), and the tested cut-off frequencies are $\omega_{c,f} = \{2, 1.5, 1\} \cdot \omega_{pwm}$. It is important to notice that these DLPFs do not directly attenuate noise power in the observed frequency window. The design goal is to suppress the noise power above f_{pwm} with as little impact on the dynamic



(a)



(b)

Figure 6.33: Variance of i_L up to $\frac{f_{pwm}}{2}$ for $L = 2.5$ mH and: (a) $\alpha = 0.1$; (b) $\alpha = 0.2$.

performance[8]. DLPFs with lower cut-off frequencies bring more filtering at $f > f_{pwm}$; hence, the aliasing is additionally suppressed and the in-band noise power is expected to further decrease. The analytical prediction for MS-PWM is obtained using the equivalent transfer function as in (5.23). Note that, even without the DLPFs, the output noise power is reduced compared to DS-PWM without AD by 2.2 dBA^2, due to a higher phase margin, which brings additional filtering by the closed-loop system.

Same conclusions are brought based on results shown in Fig. 6.33b, given for $\alpha = 0.2$, except that all variances are increased due to the higher bandwidth setting. It can be also seen that a higher noise suppression of MS-PWM without DLPF relative to DS-PWM without AD is obtained, equal to

[8]In order to verify that the implemented DLPFs do not strongly deteriorate passivity properties, the admittances are measured for the tested DLPFs and only a small impact is seen. Negative conductance peaks, measured for $\alpha = 0.2$ for compatibility with results in Table 6.1, are $\{-0.25, -0.17\}$ % for $L = \{1.5, 2.5\}$ mH at 28 kHz.

approximately 5 dBA^2, due to a higher phase margin difference between the two. Compared to $\alpha = 0.1$, a slightly higher error between the analytical data and measurements is obtained for MS-PWM. Some mismatch is assumed to come from the ac operation tested in this chapter. Still, the trend is well-predicted and the error is not much higher than in Chapter 5.

The main conclusion of this section is that implementing AD does not necessarily result in excessive noise sensitivity. Still, MS-PWM is able to offer additional noise suppression without compromising the passivation effectiveness.

6.7 Summary

Firstly, this chapter has shown that MS-PWM is capable of rendering the VSC admittance passive in a wide frequency range. This is achieved without any passive or active damping technique, which significantly reduces the system complexity and cost. Some impact of the MS-PWM nonlinearities is present; however, it is not found to be detrimental for passivity properties. Even for lower values of N, where the measured admittance still features a small non-passive zone, the resulting negative damping is strongly reduced compared to double-update.

Secondly, this chapter has provided a comparison in terms of the effectiveness and noise sensitivity of different control strategies used to render the admittance of grid-connected VSCs passive. MS-PWM is compared against typically used derivative-based AD methods. It is shown that MS-PWM outperforms AD in the passivizing effectiveness, as AD brings a negative impact around and above the Nyquist frequency. Grid-connected operation is tested for different anti-resonant networks and the results demonstrate that only MS-PWM enables robust stability. Analytical modeling of noise propagation is proposed and verified, revealing that AD strategies are not highly sensitive. Still, MS-PWM outperforms AD in this respect as well.

MS-PWM is shown to be a promising candidate for grid-connected VSCs as it enables very high bandwidths, while inherently suppressing the non-passive input admittance behavior, therefore guaranteeing robustness to high-frequency harmonic instability of current-controlled grid-connected VSCs. To enable highest damping and lowest impact of the MS-PWM nonlinearities, it is advisable to choose as high an oversampling factor as allowed by the control platform.

Chapter 7

Conclusions

This thesis analyzes the multi-sampled pulsewidth modulation and focuses on its fundamental properties, important implementation aspects, and applicability for solving a practical problem found in grid-tied converters. The dissertation structure is organized such that it first brings the analysis of negative aspects of MS-PWM and provides a methodology for their suppression. Then, it investigates a way to emphasize inherently positive aspects of MS-PWM. Finally, it builds upon these findings to examine the potential of MS-PWM in solving a practical problem, while having a full awareness of its capacities and limitations.

The first three chapters serve as an introduction and a review of the existing knowledge.

Chapter 4 analyzes the MS-PWM nonlinearities caused by the switching ripple, particularly those related to the jump discontinuities of the modulating waveform. The discontinuity-related nonlinearities are classified, relations between the modulating waveform and the carrier that enable them are explained, and the resulting impacts on the converter's operation are described. Then, the chapter focuses on the MS-PWM nonlinearity that is discovered during this work. It is demonstrated how this nonlinearity, which is manifested as the infinite-gain zone of the modulator, brings a mechanism for limit-cycle oscillations. The consequential jittering of the duty cycle is statistically modelled and it is shown to be directly dependent on the size of the critical modulating waveform discontinuities. An algorithm is proposed to remove the jittering in steady-state conditions. Then, the chapter continues with exploring how different control system settings, feedback filters, and controller structures, impact the sign and size of the critical discontinuities, in this way determining which nonlinearity will arise and to what extent. The end result is a framework for the system design that minimizes the impact of the MS-PWM nonlinearities, without having to completely filter out the switching ripple. The main conclusions of this chapter are:

- Sign of the critical modulating waveform discontinuities determines which type of nonlinearity will be brought to the system. The negative sign, i.e. the counter-phase operation, brings the reduced-gain and the zero-gain zones. The positive sign, i.e. the in-phase operation, brings the infinite-gain zones that are, in general, highly unfavourable.

- Size of the discontinuities determines the nonlinearities' extension and, hence, the overall impact on the converter. The discontinuities can be reduced by an appropriate filtering or simply by increasing the oversampling factor. This brings a motivation for choosing as high an oversampling factor as possible.

Chapter 5 analyzes the noise propagation in MS-PWM systems. First, it is shown that the DPWM down-samples the modulating waveform, which causes aliasing and limits the noise suppression when the oversampling factor is increased above 2. Correspondingly, design of the anti-aliasing digital filter is proposed, with a goal to reduce the decimation impact while not strongly affecting the dynamic performance. Then, new analytical models are derived for noise propagation in open-loop and closed-loop systems that feature decimation. Extensive experimental measurements validate the derived models and show that the MS-PWM control systems with the high-frequency proportional-dominant controllers (P, PI, PR) and the proposed anti-aliasing filters can strongly suppress noise with a small impact on the dynamic response. Without any filters, increase of the oversampling factor above 2 practically does not have any impact on the output noise power. Contrarily, for MS-PWM systems with derivative-based controllers, increase of the oversampling factor on its own brings noise amplification. In such cases, for strong noise suppression, the required anti-aliasing digital filters introduce a higher impact on the system dynamics. This chapter is concluded by comparing the noise suppression capacities of MS-PWM and a more common MR-DS-PWM strategy, which applies the oversampled filtering and subsequently decimates the control rate to double-update. The newly derived models for noise propagation are shown to be valid also for MR-DS-PWM. It is revealed that the noise attenuation capabilities of these two strategies are practically the same. However, unlike MS-PWM, MR-DS-PWM strongly penalizes the dynamic performance. The main conclusions of this chapter are:

- In terms of noise propagation, digital pulsewidth modulators introduce a re-sampling action with the rate determined by the number of modulated edges of the switching signal. Correspondingly, for MS-PWM with the triangular carrier, the decimation occurs when the oversampling factor is increased above 2.

- To enable strong noise suppression with MS-PWM, some anti-aliasing digital filtering is needed. These filters can be designed so as to impose a small impact on the dynamic performance.

- For strong noise suppression and a high dynamic performance, choosing as high an oversampling factor as possible is advised. However, care should be taken if derivative-based controllers are used. For those, without including the anti-aliasing digital filters, the increase of the oversampling factor amplifies noise rather than suppressing it.

Chapter 6 analyzes the effectiveness of MS-PWM in providing robust stability of grid-tied VSCs. The chapter begins by analyzing the impact of the control system delays on introducing negative damping in the high-frequency range. It is explained how the system stability can be analyzed using the VSC admittance and how a sufficient condition for stability can be achieved by rendering the admittance

passive. The chapter continues with the experimental admittance measurements and comparison between the control system with MS-PWM and the ones with DS-PWM and typically-used active damping methods, based on the derivative feedforward actions. It is demonstrated that MS-PWM is capable of rendering the admittance passive in a wide frequency range, without having to use any additional active damping technique. Furthermore, impact of the MS-PWM nonlinearities is examined and it is shown not to be detrimental for the passivity properties. Suppression of the nonlinearities using a digital filter designed in Chapter 4 is successfully tested as well. As for the AD strategies, it is shown that their effectiveness is limited to the medium frequency range, while bringing a detrimental impact at very high frequencies. The implications of the examined admittance properties on stability is experimentally tested by connecting the VSC to a grid with specific impedances. It is verified that MS-PWM enables robust stability, while AD strategies cause instability for some of the tested scenarios. In the end, the chapter examines the noise sensitivity of the analyzed passivizing control strategies by deriving the corresponding noise propagation models and comparing them with the experimental measurements. It is shown that the derivative-based AD strategies are not highly sensitive; however, MS-PWM again offers a superior performance. For MS-PWM, anti-aliasing filters designed based on the procedure from Chapter 5 are tested and it is demonstrated that a strong noise suppression is possible, with a negligible impact on the admittance properties. In summary, it is verified that MS-PWM is a very suitable high-performance control strategy for grid-tied VSCs. Together with enabling a high dynamic performance, it inherently suppresses the non-passive admittance behavior and therefore offers a robustness to high-frequency harmonic stability problems found in grid-following VSCs. The main conclusions of this chapter are:

- MS-PWM is suitable for the high-frequency passivity-oriented control design. It inherently extends the passive zone by reducing, instead of compensating, control delays.
- For highest damping and lowest impact of MS-PWM nonlinearities, it is advisable to choose as high an oversampling factor as allowed by the control platform.

Some practical remarks on MS-PWM, based on the research conducted in this thesis, are listed here.

- The oversampling factor should always be chosen as high as allowed by the control platform. Besides the positive impact on delay reduction and noise suppression, higher oversampling factors significantly reduce the impact of the MS-PWM nonlinearities caused by the modulating waveform discontinuities, which are the main limitation of this modulation strategy.
- With MS-PWM, applying some low-pass filtering to the feedback signal is generally advisable. First, a suitable anti-aliasing filter design can enable a strong noise suppression. Second, particularly for lower oversampling factors, the discontinuity-related nonlinearities can be effectively mitigated with an appropriate design. In this case, care must be taken because low-pass filters do not always bring a positive impact, as they may cause the in-phase operation and, consequently, introduce limit-cycle oscillations. Third, for high oversampling factors, although the discontinuities

have a low impact, low-pass filtering reduces the switching ripple magnitude, which suppresses the effects of ripple modulation. The simplest solution that removes practically all of the nonlinearities is the moving average filter, however, its impact on the dynamic performance is very high.

To conclude, there are several interesting topics for further research:

- Analysis of sensitivity to the switching noise caused by high dv/dt and di/dt during commutations of the converter. In principle, sampling of the switching noise is not only present in MS-PWM and its suppression is a topic of high importance in many applications. As noted in Chapter 5, this type of noise is correlated to the feedback signal and is strongly dependent on the hardware design; hence, it is hard to treat analytically. With a proper hardware and sensing circuit design, switching noise is not highly manifested and MS-PWM can be fully exploited in relevant industrial applications. On the other hand, in systems where the feedback signal is strongly corrupted by the switching noise, having a very high bandwidth control is a hardly attainable goal. However, with many samples per switching period, it may be possible to implement some smart filtering strategy. For example, ripple predictors may be used to replace a noise-corrupted sample by tracking its difference from the estimated value. Another possibility is the use of non-linear rank filters to discard the corrupted sample with a low impact on the dynamic response. Finally, it should be mentioned that using moving average filters may help reduce the switching noise impact if the number of samples if sufficiently high. For example, if one out of 32 samples contains the switching noise, the averaging will strongly reduce its impact. However, for a lower number of samples, the averaging may have a detrimental impact on the system performance. For example, if 4 samples are averaged, out of which 1 is corrupted by the switching noise, its impact is not highly suppressed. Moreover, the averaging action maintains the information on the corrupted sample throughout the averaging period. On the other hand, without any filters, if the switching noise is acquired several sampling periods before the switching action occurs, it may not have any impact at all on the modulating segment that intersects with the carrier. In general, for MS-PWM, it is not clear whether simple low-pass filtering reduces or amplifies problems related to the switching noise. It is, however, evident that, once again, related effects are reduced for higher oversampling factors.

- Further optimization in designing the feedback filters. Supposing that the switching noise is not highly manifested, the objective is to effectively suppress the MS-PWM nonlinearities caused by the switching ripple and, if needed, to provide an anti-aliasing function for a strong white noise suppression. The design should be such that it brings as low impact on the dynamic performance as possible.

- Investigation of MS-PWM properties in multi-level and interleaved converters with PS-PWM. In most reported applications, to avoid sampling the switching ripple, the oversampling factor is determined by the number of phase-shifted carriers, i.e. by the ripple frequency multiplication. However, in unbalanced conditions, the ripple is unavoidably sampled and, therefore, the MS-

PWM nonlinearites are expected to arise. Moreover, with a powerful-enough control platform, nothing prevents an additional increase of the oversampling factor. It is expected that this would further push the dynamic capabilities, even though at the expense of the switching ripple being introduced in the feedback.

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