Design and Implementation of a Two-Stage Resonant Converter for Wide Output Range Operation

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***Abstract*—This paper proposes and analyzes a two-stage isolated dc-dc converter for electric vehicle charging applications, where high efficiency over a wide range of battery voltages is required. It employs a first pre-regulation stage and a second half-bridge LLC stage, integrated with the first. The second stage is always operated at resonance, ensuring high efficiency. The first pre-regulation stage is responsible for the desired input-to-output voltage conversion ratio and the zero-voltage switching operation of all the switches. This allows low conversion losses even with voltages that may vary over a wide range. The paper presents the conversion structure, the converter analysis, the design of the magnetic elements, and demonstrates the converter operation considering an experimental prototype interfacing a 750 V dc-link with an output bus with nominal voltage range 250 V-500 V. The implemented module is rated 5 kW and achieves a peak efficiency of 98.0% at 3 kW output power.**

***Index Terms*—battery charger, buck-boost, dc-dc converter, DCX, fast-charging, resonant LLC, pre-regulation, soft-switching.**

I. Introduction

THE ELECTRIC transportation paradigm is gaining ground in many countries. DC-DC converters with galvanic isolation are the beating heart of an effective electric-vehicle (EV) battery charging systems [1]–[4]. This application field calls for novel conversion solutions with extraordinary features in terms of size, efficiency, and cost [5].

Many topologies are described in the literature differing in terms of zero-voltage switching (ZVS) capabilities, efficiency, power density, cost, and complexity. Among these, the dual-active-bridge (DAB) and the resonant LLC converter are often considered for their several merits [2], [6]. The DAB converter offers straight-forward voltage regulation and its voltage step-up/down capability is convenient in many applications, such as for the connection of renewable sources to dc distribution busses operating at different voltage levels in stationary microgrids [7] as well as for battery chargers

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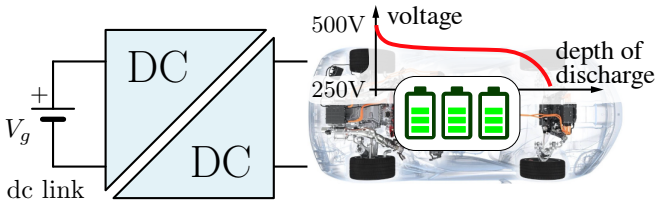


Fig. 1. EV-charging application.

[2]. However, if operated with input/output voltage ratios far from the transformer turns ratio or at light-load, the DAB converter reactive power can increase dramatically and lose ZVS conditions, which severely degrades the efficiency of conversion, especially at high switching frequencies [2], [8]. This condition on the voltage ratio is often encountered in the considered application, represented in Fig. 1, where battery state of charge variations due to typical mission profiles may bring to wide ranges of operating voltages [2], [5], [9]–[11]. Recently, even if different techniques were proposed to overcome these limitations, like, for example, [8], [12], [13], resonant topologies proved to be the most suitable choice when aiming at high power density, full ZVS, and low cost [2], [6].

The resonant LLC converter is renown for its simple structure and efficient power conversion [6], [10], [14]. LLC resonant converters can achieve ZVS operation for the primary-side switches and zero-current switching (ZCS) operation for secondary-side switches, but performance significantly degrades at input or output voltages that do not allow near-resonance operation [2], [14]. The literature reports different approaches to overcome the limitations of frequency-modulated LLC converters [2], [10], [15], [16]. In the following, in order to provide a representative overview of the different approaches and the several contributions available in the literature, these are classified based on whether the approaches focus on:

1) primary-side [15], [17]–[19] or secondary-side structures [11], [20]–[22];
2) resonant tank [23];
3) conversion structure considering partial-power conversion [3], [24], [25], and
4) number of stages [10], [26]–[31].

Table I summarizes the main features and limitations related to

TABLE I
OVERVIEW OF REPRESENTATIVE APPROACHES FOR HIGH-EFFICIENCY DC-DC CONVERTER STRUCTURES

Class	Reference	Features	Limitations
1	[11]	• Wide output voltage range, • ZVS of primary switches independent from load conditions,	• Two additional switches at low-voltage side, • parallel-connected LLC converters can suffer from unbalanced power sharing due to asymmetries in the two resonant tanks, • high component count.
1	[20]	• Very wide output voltage range, • passive rectification with no additional active switches.	• Efficiency decreases rapidly far from nominal conditions, • reconfigurable structure requiring phase-shift control to mitigate current and voltage stresses on the components, • parallel-connected LLC converters can suffer from unbalanced power sharing due to asymmetries in the two resonant tanks: control provisions needed.
1	[17]	• Very wide output voltage range, • passive rectification with no additional active switches, • ZVS of primary switches independent from load conditions.	• Efficiency decreases rapidly far from nominal conditions.
1	[22]	• Very wide range of output voltages.	• Frequency modulation and PWM modulation of auxiliary switches, • additional switches with dedicated modulation capable of smooth transitions between the different configurations.
1	[21]	• Wide output voltage range.	• Hybrid modulation required to ensure a wide output voltage range, • limited efficiency improvements due to high output-stage conduction loss.
2	[23]	• Wide range of output voltages, • smooth transitions between the configurations.	• Additional LCL-T resonant tank, • careful design of the additional resonant tank required to limit related losses.
3	[24]	• Low switching losses on output switches.	• Narrow range of operating voltages, • active rectification with very low conduction losses but relatively high number of switches (8 for active rectification, plus 8 for output voltage modulation), • use of two transformers.
3	[25]	• High efficiency.	• Additional complexity in the structure, DCX stages design, and modulation, • increased component count.
3	[32]	• Wide input voltage range.	• Complex modulations, • high component count, • no galvanic isolation.
4	[30]	• Wide input voltage range, • high efficiency.	• High component count.
4	[28]	• Good efficiency over a wide range of input and output voltages.	• No galvanic isolation, • poor efficiency at light-load.
4	herein	• Wide output voltage range, • low component count, • galvanic isolation, • passive rectification with no additional active switches.	• Poor efficiency at light-load, which requires adequate modulation.

the relevant approaches defined above and discussed in more details next.

1) Approaches considering the primary or secondary side structures: An LLC structure reconfigurable for half-bridge or full-bridge operation combined with auxiliary switches at secondary side is proposed in [22]. Such a solution is able to cover a very wide range of output voltages, but additional switches and dedicated modulation capable of smoothly transit between the configurations are required. Similarly, [21] proposes a full-bridge LLC working at resonance frequency with a voltage quadrupler and an auxiliary switch at the output. Such a converter shows limited efficiency improvements, due to the high conduction loss of the output stage. In [17], an interleaved LLC is proposed with series-connected secondary sides and shared rectifier. Such a solution adopts phase-shift modulation between the two parallel LLC working at resonance frequency. It shows good performance at close-to-zero phase-shift but the efficiency decreases rapidly when far from the nominal conditions. Similarly, [20] describes an interleaved LLC with reconfigurable voltage multiplying rectifier that changes configuration from voltage doubler to voltage quadrupler. Such an approach adopts passive rectification and does not require additional MOSFETs, unlike conventional approaches as [11], [22]. Smooth transitions between the two configurations are achieved, however a phase-shift control must be introduced in order to mitigate current and voltage stresses on the components. Additionally the two parallel-connected LLC converters

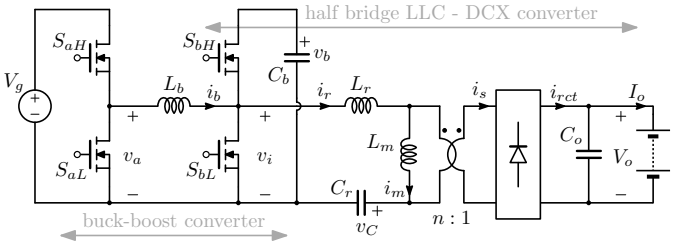


Fig. 2. Two-stage converter with pre-regulation & LLC stage.

can suffer from unbalanced power sharing due to asymmetries in the two resonant tanks, implying the adoption of additional tricks in the control strategy of the converter. An interleaved LLC is proposed in [11], achieving voltage regulation in a wide range similar to the one considered in Fig. 1. The converter can achieve ZVS for the primary switches regardless of the operating condition, however the component count is doubled and the efficiency drops when operating far from nominal condition.

2) Approaches considering the resonant tank: A reconfigurable topology employing an additional LCL-T resonant tank and with smooth transitions between the configurations is proposed in [23]. With this solution, a careful design of the additional resonant tank is required to limit the related losses and preserve overall efficiency.

3) Approaches exploiting partial power processing: A solution using input-parallel and output-series partial power processing (PPP) and resonant CLLC-type DCXs is proposed in [24], considering a narrower range of operating voltages with respect to the one considered herein. The topology is characterized by low switching losses on the output switches, but it requires an active rectification with very low conduction losses and a relatively high number of devices. The conventional LLC-type DCX design has been widely investigated in the literature [24], [28], [30], [33]. Partial power conversion solutions show potential advantages to accommodate wide operating voltage ranges for applications like in Fig. 1, at the cost of high components number, complex design of DCXs stages, and complex modulations [24], [25], [32].

4) Approaches considering additional conversion stages: Input voltage regulation is a practical solution in case wide input and output voltage regulation is needed, featuring simplicity, low component count, and adaptation to resonant or quasi-resonant stages with optimal efficiency and switching frequency [10], [26], [27], [30]. In [30], a two-stage structure for an input-series output-parallel modular power supply is proposed. With an input voltage $\leq 1\,\mathrm{kV}$ for each module, a solution with a buck pre-regulator and an LLC converter operated as dc-transformer is adopted. [28] proposes an interleaved CLLC with buck-boost pre-regulation. The converter shows good efficiency over a wide range of input and output voltages, with the disadvantage of no galvanic isolation and poor efficiency at light-load.

Based on the brief literature overview reported above, to improve the performance of the LLC resonant dc-dc converter in a wide output-voltage range, in this paper a two-stage conversion structure is considered, analyzed, and experimentally evaluated. The structure is shown in Fig. 2, where the two stages appear highlighted [29], [34]. They are constituted of a pre-regulation stage and a DCX-LLC, employing the LLC converter at its maximum efficiency condition and avoiding the efficiency degradation due to the classical frequency modulation. The topology was studied in [29] considering telecom applications with input voltage range $250\,\mathrm{V}$-$420\,\mathrm{V}$, output voltage $24\,\mathrm{V}$ and power ratings $750\,\mathrm{W}$. In [34], the potentiality of adopting a phase-shift modulation is not considered to improve the ZVS performances of the topology and the pre-regulator is operated in hard switching at lower switching frequency. Moreover a bulkier capacitor is needed to stabilize the intermediate bus voltage. In this paper, the topology is studied and demonstrated considering a battery changing application with nominal input voltage $750\,\mathrm{V}$, output voltage $250\,\mathrm{V}$-$500\,\mathrm{V}$, implementing a prototype module rated $5\,\mathrm{kW}$. Based on the analysis, a modulation scheme is also derived to operate the converter at high efficiency.

The principle of the considered conversion structure is to operate the second stage at conditions that ensure maximum efficiency, namely, at resonance, and exploit the pre-regulation stage to impose such an optimal operating condition for the second, LLC stage. The pre-regulation stage can also help in achieving zero-voltage turn-on of the switches that drive the second stage over a wide range of output voltages [2], [10]. Of course, the exploitation of latest wide-bandgap power semiconductors allows to further reduce semiconductor loss [35]. In spite of the presence of an additional stage, some valuable characteristics are highlighted and shown in terms of overall conversion efficiency. In particular, light-load low-voltage operation is possible with limited efficiency degradation, which is instead difficult to achieve with the LLC topology.

This paper extends the results preliminary presented in [36], [37], reporting additional analyses, discussion, and experimental results. In the following, the topology is introduced in Sect. II. Its main loss contributions are analyzed in Sect. III and experimentally evaluated in Sect. V. Conclusions are reported in Sect. VI.

II. Converter Structure and Operation

A. Converter Description and Operation

The two-stage topology is displayed in Fig. 2. Its peculiarity is the integration of the two power switches S_{bH} and S_{bL} of the buck-boost stage as primary switches of the half-bridge LLC [29], [34]. Thanks to such a peculiarity, the inductor current i_b and the resonant current i_r in Fig. 2 may jointly contribute in reducing the conduction loss of S_{bH} and S_{bL} and, notably, achieve ZVS. In this way, ZVS can be achieved even with lower values of magnetizing current, which also helps in reducing overall losses.

In order to exploit the high performance of the LLC stage working as dc-transformer (DCX) [25], the right-leg (i.e.,

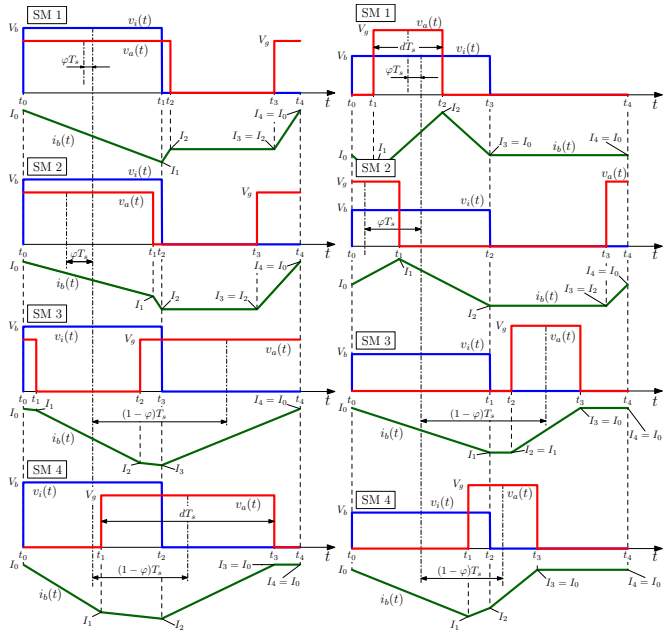


Fig. 3. Main converter waveforms for different phase-shift values considering (a) boost case and (b) buck case. Switching events are marked at time instants t_k ($k = 0, \dots, 4$), with $t_0 = 0$ and $t_4 = T_s$. The corresponding switching modes are defined analytically in Table II.

S_{bH} and S_{bL}) duty-cycle is fixed at 50%. Whereas, the two remaining degrees of freedom, that is, the duty-cycle d of the left-leg referred to the upper switch S_{aH} and the phase-shift φ between the driving signals of the two legs, can be used to adjust *i*) the inductor current at switching instants, which is important for ZVS constraints, and *ii*) the output voltage, which is important to allow operation at resonance of the LLC stage. Therefore, the total voltage gain of the structure can be computed as the product of the voltage gain of the pre-regulation buck-boost and the half-bridge LLC working as DCX:

$$M = \frac{V_o}{V_g} = M^{\mathrm{BB}} \cdot M^{\mathrm{LLC}} = \frac{V_b}{V_g} \cdot \frac{V_o}{V_b} = 2d \cdot \frac{1}{2n} = \frac{d}{n} \quad (1)$$

Remarkably, the voltage gain is a function of the duty-cycle d of the left-leg only. Whereas, the phase-shift φ represents a degree of freedom that can be used to shape the piece-wise linear current i_b to ensure ZVS of the four switches. The phase-shift φ is herein defined as the time distance between the centers of the positive pulses of v_a and v_i, normalized by T_s, as shown in Fig. 3.

Two main operation modes may be distinguished, namely, boost mode, when $d > 0.5$, and buck mode, when $d < 0.5$. For each operation mode, phase-shift variations give rise to four different shapes of the inductor current i_b, herein refereed to as switching modes (SM). The total eight SMs, depending on the values of d and φ, are displayed in Fig. 3a and Fig. 3b. Table IIIa and Table IIIb report an analytical description of the SMs, which is useful for the analysis of the converter operation. Remarkably, Fig. 3 and Table II mark the switching events at the time instants t_0, t_1, t_2, and t_3; this nomenclature

TABLE II
SWITCHING MODES (SM) BASED ON FIG. 3 & ASSOCIATED SWITCHING INSTANTS

SM	φ values	switching instants $4 \cdot t_1/T_s$	$4 \cdot t_2/T_s$	$4 \cdot t_3/T_s$
1	$\frac{1-2d}{4} \le \varphi < \frac{2d-1}{4}$	2	$1 - 4\varphi + 2d$	$5 - 4\varphi - 2d$
2	$\frac{2d-1}{4} \le \varphi < \frac{3-2d}{4}$	$1 - 4\varphi + 2d$	2	$5 - 4\varphi - 2d$
3	$\frac{3-2d}{4} \le \varphi < \frac{1+2d}{4}$	$1 - 4\varphi + 2d$	$5 - 4\varphi - 2d$	2
4	$\frac{1+2d}{4} \le \varphi < \frac{5-2d}{4}$	$5 - 4\varphi - 2d$	2	$5 - 4\varphi + 2d$

(a) Boost operation mode (i.e., $d \ge 0.5$)

SM	φ values	switching instants $4 \cdot t_1/T_s$	$4 \cdot t_2/T_s$	$4 \cdot t_3/T_s$
1	$\frac{2d-1}{4} \le \varphi < \frac{1-2d}{4}$	$1 - 4\varphi - 2d$	$1 - 4\varphi + 2d$	2
2	$\frac{1-2d}{4} \le \varphi < \frac{1+2d}{4}$	$1 - 4\varphi + 2d$	2	$5 - 4\varphi - 2d$
3	$\frac{1+2d}{4} \le \varphi < \frac{3-2d}{4}$	2	$5 - 4\varphi - 2d$	$5 - 4\varphi + 2d$
4	$\frac{3-2d}{4} \le \varphi < \frac{3+2d}{4}$	$5 - 4\varphi - 2d$	2	$5 - 4\varphi + 2d$

(b) Buck operation mode (i.e., $d < 0.5$)

is used in the following to compute the corresponding values of inductor current i_b at those mentioned instants, that is, I_0, I_1, I_2, and I_3, respectively.

B. Inductor Current Derivation

The equivalent circuit in Fig. 4 can be referred to for the derivation of the current i_b through the inductor L_b. Source voltages v_i and v_a model the voltages imposed by the half-bridges in Fig. 2, according to Table II.

The instantaneous inductor current i_b in the time domain can be computed as:

$$i_b(t) = I_0 + \frac{1}{L_b} \int_{t_0}^{t} (v_a(\tau) - v_i(\tau))\, \mathrm{d}\tau \quad (2)$$

where $I_0 = i_b(t_0)$, $t_0 < t$, is the initial value of the inductor current. Being the inductor current waveform piecewise linear, (2) can be computed as:

$$i_{b_k}(t) = i_b(t_{k-1}) + \frac{v_{L_b}(t)}{L_b} \cdot (t - t_{k-1}) \ , \quad t \in [t_{k-1},\, t_k) \quad (3)$$

for $k = 1, 2, 3, 4$. Let us call I_k the inductor current values $i_b(t_k)$ and V_{L_k} the voltage across the inductor during $[t_{k-1},\, t_k)$. The initial value $I_0 = i_b(t_0)$ is calculated imposing the capacitor charge balance during the conduction phase of S_{bH}, between $t = 0$ and $t = T_s/2$, thus:

$$I_0 = \frac{2n}{T_s} \int_0^{T_s/2} i_b(t)\, \mathrm{d}t = \frac{n}{2T_s} \sum_{k=1}^{N} \Delta t_k (I_{k-1} + I_k) \quad (4)$$

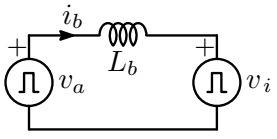


Fig. 4. Equivalent circuit for inductor current analysis.

where $\Delta t_k = t_k - t_{k-1}$ and $N = 1, 2$, or 3 is the number of piecewise representations in the considered half-period, depending on the SM. Observing that $I_k = I_{k-1} + V_{L_k}\Delta t_k / L_b$ and $\sum_{k=1}^{N} \Delta t_k = T_s/2$, (4) yields:

$$I_0 = n\frac{I_0}{2} + \frac{n}{2L_bT_s}\sum_{k=1}^{N} V_{L_k}\Delta t_k(\Delta t_k + 2\Delta t_{k+1} + 2\Delta t_{k+2}) \quad (5)$$

with $\Delta t_k = 0$ for $k > N$. Equation (5) allows to determine the initial value I_0, once the output current is known.

An additional parameter worth computing is the inductor rms current:

$$i_b^{\text{rms}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_b^2(t)\,\mathrm{d}t} = \sqrt{\frac{1}{T_s}\sum_{k=1}^{4}\int_{t_{k-1}}^{t_k} i_{b_k}^2(t)\,\mathrm{d}t} \quad (6)$$

where $i_{b_k}(t) = I_{k-1} + \dfrac{V_{L_k}}{L_b}t$, $t \in [t_{k-1},\, t_k)$, it yields:

$$i_b^{\text{rms}} = \sqrt{\frac{1}{T_s}\sum_{k=1}^{4}\left[I_{k-1}^2\Delta t_k + \frac{I_{k-1}V_{L_k}}{L_b}\Delta t_k^2 + \left(\frac{V_{L_k}}{L_b}\right)^2\frac{\Delta t_k^3}{3}\right]} \quad (7)$$

The equations reported above can help to properly define the modulation parameter φ, as shown in the following sections.

III. Main Loss Contributions

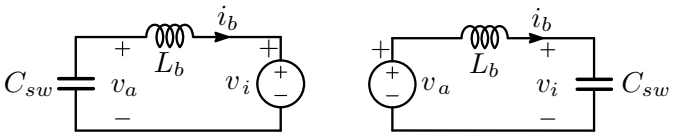
Since all the diodes of the DCX-LLC can achieve ZCS turn-off and, with a proper modulation of the phase-shift φ, ZVS turn-on can be achieved for all the active switches, the main loss components include conduction losses of MOSFETs and diodes, magnetic components losses, and MOSFETs turn-off losses. Phase-shift modulation has a significant impact on both MOSFETs switching and conduction losses and inductor losses. The ac resistance and the ferrite losses of the inductor should be accurately took into account in the design of the component to allow a convenient exploitation of the phase-shift modulation. Instead, the transformer losses of the LLC are not affected by φ variations. Besides, optimal design for maximum efficiency of the LLC transformer is facilitated by the fixed operation at nominal conditions allowed by the pre-regulation stage.

The following paragraphs discuss the ZVS conditions for switching losses minimization, the conduction losses evaluation of the inductor and the transformer, and the design procedure of the magnetic components.

A. Conditions for Zero-Voltage Switching Operation

Switching losses mainly depend on the switches output capacitance C_{oss}, the inductor current at switching instants t_k, which are marked as I_k in Fig. 3, and the chosen dead-times. To minimize such a loss contribution, ZVS at turn-on is necessary [38]. This poses minimum switched current constraints for ZVS, which can be determined as discussed in [38]–[40].

Fig. 5 shows a couple of equivalent circuits helping in the analysis of the SMs in Fig. 3. Generators v_i, in Fig. 5a, and v_a, in Fig. 5b, are set as per the considered SM, resulting in different minimum current conditions, function of the input and output voltages. By the methods in [39], [40], the minimum current condition for the ZVS of the left-leg (refer to Fig. 5a) can be calculated by solving iteratively the following expression for $t_{\text{ZVS}} \le t_{\text{dead}}$:



(a) Turn-on S_{aH} and S_{aL} (b) Turn-on S_{bH} and S_{bL}

Fig. 5. Equivalent circuits during ZVS transients.

$$t_{\text{ZVS}} = \int_0^{V_g} \frac{C_{sw}(v_a)}{\sqrt{i_{\text{ZVS}}^2 + \dfrac{2}{L_b}\displaystyle\int_0^{v_a} C_{sw}(v)(v_i - v)\,\mathrm{d}v}}\,\mathrm{d}v_a \quad (8)$$

where t_{ZVS} is the duration of the transition with an initial inductor current i_{ZVS}, and C_{sw} is the equivalent charge capacitance at the switching node [39]. Equation (8) can be adapted to the equivalent circuit in Fig. 5b by substituting V_g with V_b and v_i with v_a, respectively.

By this approach, ZVS regions for all the switches in the output-current, output-voltage (i.e., duty-cycle d), and phase-shift space can be computed, as displayed in Fig. 6. Fig. 7a and Fig. 7c show the ZVS region at minimum and nominal output voltage respectively. Notably, ZVS is achieved over the whole range of transferred power and output voltages. In Fig. 6, and then in Fig. 7a and Fig. 7c, red lines highlight those points where ZVS is achieved for all the switches with minimum inductor rms current, which relates to the minimum phase-shift values to achieve ZVS. Such an inductor current computed as in (7) is shown in Fig. 7b and Fig. 7d for minimum and nominal output voltages, respectively. Fig. 8 shows the switches rms currents at $V_o = 400\,\text{V}$ and $I_o = 12.5\,\text{A}$. For low phase-shifts, where ZVS is achieved for all the switches with minimum inductor rms current, the effect of the current compensation of the right-leg switches is appreciable, which is one of the peculiarities of the analyzed topology in Fig. 2.

It is worth remarking that absence of ZVS turn-on makes switching losses become a predominant portion of the total

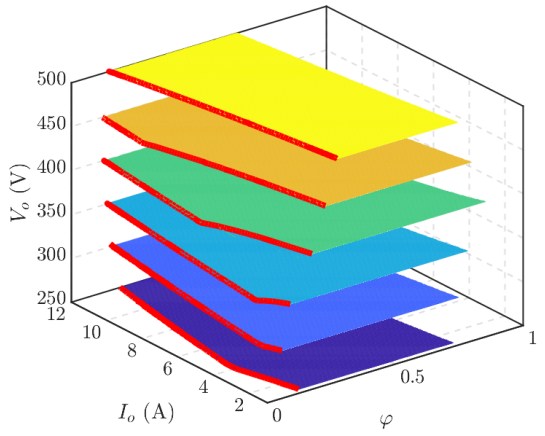


Fig. 6. ZVS regions for the whole output voltage range. Converter parameters are reported in Table III.

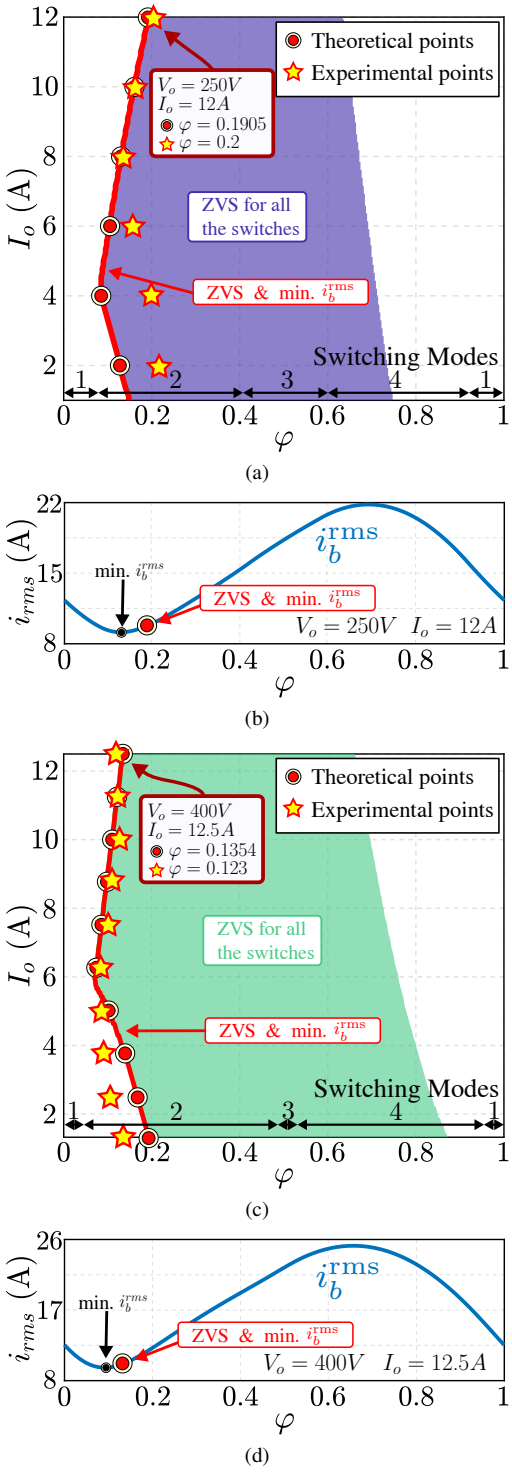


Fig. 7. Results obtained by exploiting the phase-shift φ to achieve ZVS. At $V_o = 250\,\mathrm{V}$, $I_o = 12\,\mathrm{A}$: (a) ZVS region, (b) inductor rms current. At $V_o = 400\,\mathrm{V}$ and $I_o = 12.5\,\mathrm{A}$: (c) ZVS region; (d) inductor rms current. Optimal values of phase-shift φ are those lying along the line labeled as "*ZVS* & min. $i_b^{\rm rms}$", for which ZVS is achieved with minimum circulating rms currents. Switching modes as defined in Fig. 3 are also reported on the bottom of (a) and (c).

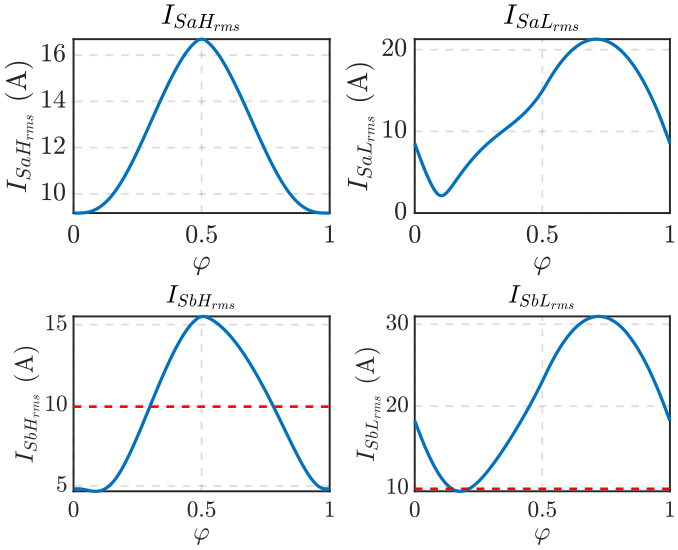


Fig. 8. Switches rms currents at $V_o = 400\,\mathrm{V}$, $I_o = 12.5\,\mathrm{A}$. The red-dashed line shows the resonant current component i_r on the right-leg MOSFETs.

converter loss, especially in high-voltage applications [41]. For this reason ZVS turn-on is aimed herein, especially at low output voltages, where state-of-the-art LLC topologies present significant efficiency degradations due the lost of ZVS [2].

B. Conduction Losses Estimation

Generally, the conduction losses of a magnetic element can be modeled by summing dc losses, related to the windings dc resistance $R^{\rm dc}$ and the dc value of the current $i^{\rm dc}$, and ac losses, which can be estimated by considering the rms of the first M ac frequency components $i^{\rm ac_m}$ and the related ac winding resistances. Therefore, the conduction losses related to the inductor L_b can be modeled as:

$$P_{L_b}^{\rm cond} = R_b^{\rm dc} \cdot i_b^{\rm dc\,2} + \sum_{m=1}^{M} R_b^{\rm ac_m} \cdot i_b^{\rm ac_m\,2} \tag{9}$$

Equation (9) is adopted for the estimation of the winding losses of the inductor in Sect. V. In the considered case, the number of harmonics for an acceptable estimate is set $M = 3$. Instead, the conduction losses of the transformer of the LLC stage are not affected by any modulations. The LLC behaves as a DCX and the winding losses of the transformer can be simplified as:

$$P_{\rm Tr}^{\rm cond} \simeq R_{\rm Tr}^{\rm ac_1} \cdot i_r^{\rm rms\,2} \tag{10}$$

where $R_{\rm Tr}^{\rm ac_1}$ is the ac resistance of the windings referred to the primary side at fundamental frequency and $i_r^{\rm rms}$ is the rms value of the resonant current. In this approximation, the magnetizing current effect on the conduction losses is overestimated, which is acceptable when such a current is relatively small, as in the considered DCX-LLC structure.

C. Optimal Switching Mode (SM) Selection

In Sect. II-A, eight SMs are identified depending on the phase-shift φ and the duty-cycle d, as defined in Fig. 3 and Table II. Each SM is characterized by a unique switching

sequence, which gives rise to eight different shapes of the inductor current i_b. A proper SM must be selected in order to obtain a shape for the current i_b that is suitable to ensure ZVS for all the switches. This can be performed by verifying condition (8) for each of the converter switches. Moreover, if multiple SMs appear suitable for the aimed ZVS conditions, the SM ensuring minimum circulating currents should be selected. To better explain the procedure, the modulation planes for a couple of representative operating points are reported in Fig. 7. It is possible to notice that there is a wide range of phase-shifts, covering multiple SMs, that allow to satisfy ZVS conditions. Notably, the SM that encloses all the operation points while in ZVS with minimum inductor rms currents (i.e., all the operating points highlighted with the red lines in Fig. 7a and Fig. 7c) is SM 2. This is verified for buck and boost operation modes and for the whole output power range.

IV. Design Considerations

A design procedure of the converter in Fig. 2 is shown in the following based on the analyses presented in Sect. II.

A. Transformer Design: Preliminary Considerations

From (1), the transformer turns ratio n is set to 1 to make the LLC converter operate at the resonant frequency f_s at the output nominal voltage V_o equal to 400 V and the intermediate-bus voltage V_b equal to 800 V.

The value of the magnetizing inductance L_m is typically chosen to ensure a sufficiently high magnetizing current to allow ZVS and a desired voltage gain [20]. Lower L_m values give lower voltage gains and ease ZVS, but it also implies higher transformer losses. Differently, with the aimed DCX operation of the LLC stage in Fig. 2, ZVS can be achieved regardless of the contribution by the magnetizing current. This is illustrated in Fig. 9 considering the operating point $V_o = 250\,\text{V}$, $I_o = 10\,\text{A}$. The red dashed-line at the boundary represents the minimum absolute switched current to achieve ZVS, estimated via (8). The red dotted-line shows the additional contribution by the magnetizing current at the switching instants. Notably, ZVS conditions can be satisfied by a proper modulation of the phase-shift φ, then, even large magnetization inductances can be selected. For example, a transformer with $L_m = 180\,\mu\text{H}$ was designed and adopted in the prototype shown herein, while a classical design for a DCX-LLC would require a magnetizing inductance not higher than:

$$\frac{V_b}{4 f_s i_{\text{ZVS}}} \tag{11}$$

where i_{ZVS} is the constant current needed for zero-voltage transition at the bus voltage V_b, and f_s is the switching frequency. In the considered prototype, the classical design procedure would result in $L_m \leq 90\,\mu\text{H}$ in order to fulfill ZVS constraints of the LLC leg, with consequently higher rms currents.

For what concerns the design of the resonant $L_r C_r$ tank, the transformer leakage inductance can be exploited for the implementation of the inductive part. Given the DCX-LLC operation mode, low values of L_m can be used, which is beneficial in terms of transformer design, losses, and resonant capacitor voltage stress. Interleaving is also possible for the primary and secondary-side windings to limit the leakage inductance. The capacitive part can be selected on the basis of the desired resonant frequency (i.e., converter switching frequency given the DCX-LLC operation).

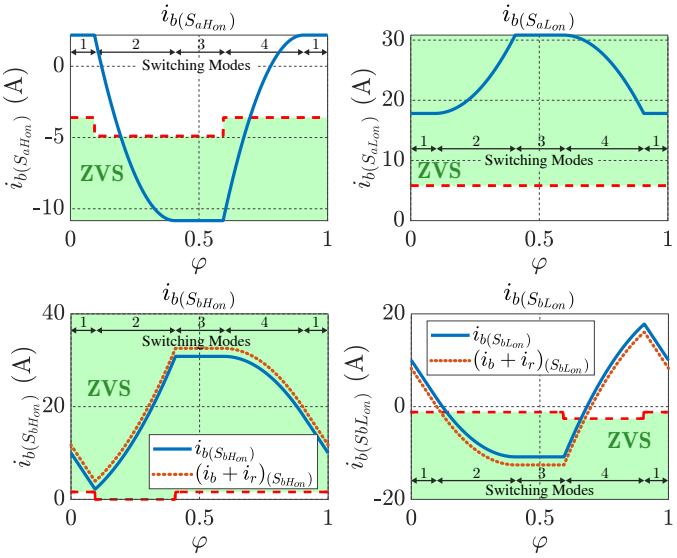


Fig. 9. Inductor current at switching instants *versus* φ; $V_o = 250\,\text{V}$, $I_o = 10\,\text{A}$. The term $i_b + i_r$ shows the additional contribution by the magnetizing current.

B. Transformer Losses Minimization

Magnetic losses include winding loss and core loss, both of which should be carefully estimated for overall minimum losses. The transformer design procedure adopted herein is based on [42]. Once the magnetic core is selected, with given magnetic volume V_c, window winding area W_a, core cross-sectional area A_c, Steinmetz parameters K_c, α, and β, and maximum window filling factor k_u of the transformer (typ., assume $k_u \leq 40\%$), it is possible to calculate the winding losses as:

$$\begin{cases} P^{\text{cond}} = RF(f_s)\rho_w V_w k_u J_0^2 \\ J_0 = \dfrac{\sum VA}{K_v f_s k_f B_{max} k_u A_p} \end{cases} \tag{12}$$

where ρ_w is the copper resistivity, V_w is the total windings volume, $RF(f_s) = R^{\text{ac}}/R^{\text{dc}}$ is the resistivity factor for the selected litz wire at fundamental frequency [42], J_0 is the current density, $\sum VA$ is the power rating of the transformer, K_v is the waveform factor, f_s is the fundamental frequency, B_{max} is the peak flux density, k_f is core stacking factor, and $A_p = A_c W_a$ is the area product of the core. While, core losses are given by Steinmetz equation:

$$P^{\text{core}} = V_c K_c f_s^{\alpha} B_{max}^{\beta} \tag{13}$$

where K_c, α and β and the Steinmetz parameters for the considered material.

The total loss of the transformer is finally computed as:

$$P^{\text{cond}} + P^{\text{core}} . \tag{14}$$

Such a total loss must be lower than the thermal dissipation capability of the component, which can be estimated during the design phase.

Fig. 10 reports the results using (14), showing a total loss of 17 W at nominal conditions, namely, $V_o = 400\,\text{V}$ and $P_o = 5\,\text{kW}$. At the point of minimum total loss, $B_{max}^{\text{opt}} = 89\,\text{mT}$ and the total loss is equally shared among winding and total losses. A prototype of the transformer was implemented using a core PQ50/50 N87 and two parallel litz wires $500 \times 71\,\mu\text{m}$, resulting in a measured total power loss of 21 W at the same nominal conditions.

Fig. 11 depicts the winding layout of the designed transformer. The transformer has an unitary turns ratio n, current density of $J_0 = 4.3\,\text{A/mm}^2$, and number of windings per turn of $N_p = N_s = 17$ given by:

$$N_p = N_s = \frac{V_o}{K_v f_s B_{max}^{\text{opt}} A_c} \tag{15}$$

where B_{max}^{opt} is the selected peak flux density. Remarkably, a corresponding transformer design for a full-bridge LLC with the same B_{max} and current density J_0 would lead to a required area-product A_p higher by 10% than the obtained design, that is, to higher wire resistance and core loss.

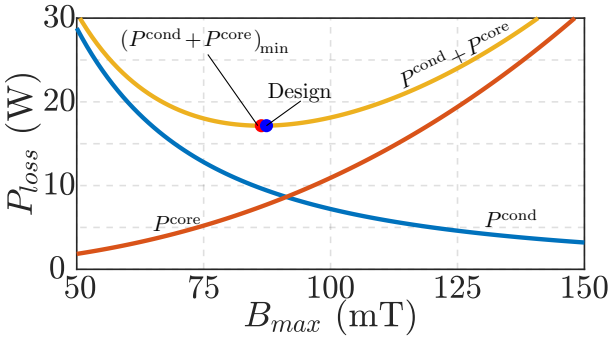


Fig. 10. P-B plot for transformer design at $V_o^{\text{nom}} = 400\,\text{V}$ and $P_o^{\text{nom}} = 5\,\text{kW}$. The design point is obtained with two parallel litz wires $500 \times 71\,\mu\text{m}$ each and number of turns $N_p = N_s = 17$.

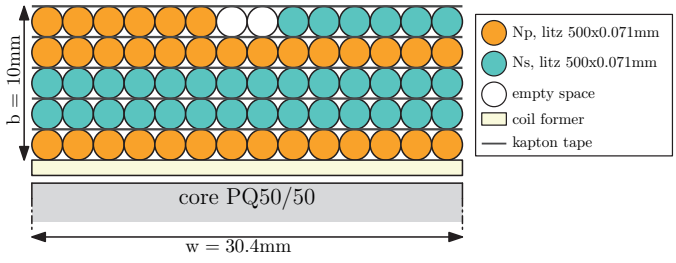


Fig. 11. Winding layout of the designed transformer. Number of turns $N_p = N_s = 17$. Each turn is composed of two parallel litz wires $500 \times 71\,\mu\text{m}$ each.

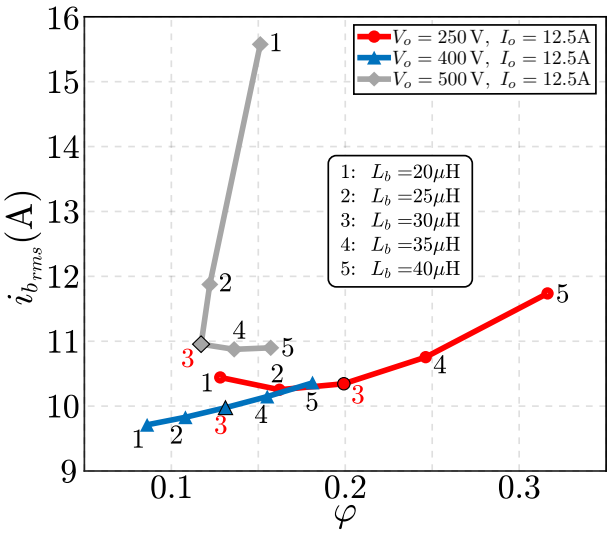


Fig. 12. Selection of the optimal inductance value, at maximum output current $I_o = 12.5\,\text{A}$. ZVS is always achieved for each point.

C. Inductor Design Considerations

In order to minimize conduction losses, the inductor value is selected to minimize the rms value of the current i_b, that is, i_b^{rms}, over the entire voltage conversion range. Specifically, the inductance value was selected aiming at ZVS with minimum circulating current. Fig. 12 reports the required minimum phase-shift and resulting inductor rms current considering different inductor values, while always ensuring ZVS. Data are reported for different output voltage values and nominal output current. In this comparison, $L_b = 30\,\mu\text{H}$ emerges as the best overall choice in terms of rms current for the output voltage range in the considered application, and shown in Table III. This value was selected for the implementation of an inductor L_b, by a procedure similar to the one used for the transformer design in Sect. IV-B. It is worth reporting that, a wider output voltage range would require an inductor with larger core and wire sections in order to satisfy thermal constraints.

V. Experimental Results

The experimental prototype displayed in Fig. 13 of a 5-kW module with parameters in Table III has been implemented to validate the reported analysis, modulation, and design choices.

TABLE III
PROTOTYPE PARAMETERS.

Parameter	Symbol	Value	
Input voltage	V_g	750	V
Output voltage	V_o	250-500	V
Nominal power	P_o^{nom}	5	kW
Switching frequency	f_s	200	kHz
Leakage inductance	L_r	1.8	µH
Magnetizing inductance	L_m	180	µH
Inductance	L_b	30	µH
Turns ratio	n	1	-
Resonant capacitance	C_r	290	nF
S_{aH}, S_{aL}	SCT3040KR, SiC MOSFETs		
S_{bH}, S_{bL}	G3R30MT12K, SiC MOSFETs		
Output Rectifier	SK20KDD12SCp, SiC diodes		

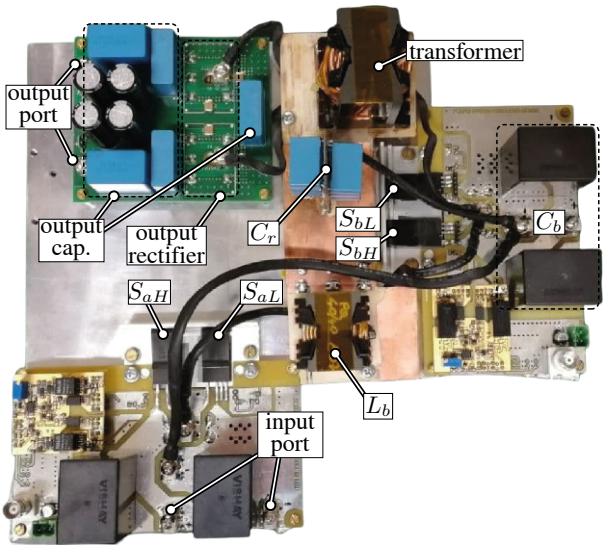


Fig. 13. Photo of the implemented experimental prototype.

A. Switches Zero-Voltage Turn-on

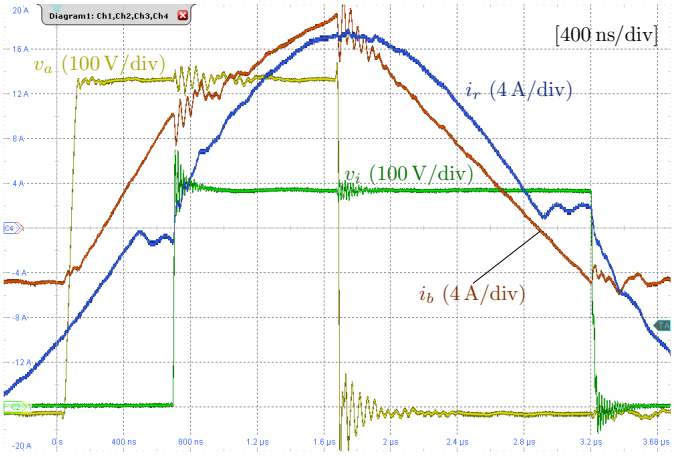
Operation at $\varphi = 0.25$, output voltage of 250 V, and output current of 10 A has been evaluated experimentally and shown in Fig. 14. At this operating point, ZVS is verified for all the switches. Notably, according to Fig. 7, ZVS can be achieved with phase-shift values between $\varphi = 0.16$ and $\varphi = 0.65$. At the boundary condition for ZVS of $\varphi = 0.16$ the inductor conduction losses are 35% lower than the losses at the operating point in Fig. 14, with $\varphi = 0.25$.

With $\varphi = 0$, non-ZVS transitions for S_{bL} occur at low power levels, as expected based on simulation models. This precludes operation at output powers higher than 1.1 kW, due to excessive switching loss in S_{bL}. Converter operation at such an operating point is displayed in Fig. 14a (i.e., $\varphi = 0$, $V_o = 250$ V, $I_o = 4.4$ A). At this point, S_{bL} experiences non-ZVS transitions, while ZVS is achieved for all the other switches. An increase of delivered output power with $\varphi = 0$ leads to higher switching and conduction loss and to non-ZVS transitions for switch S_{aH} too.

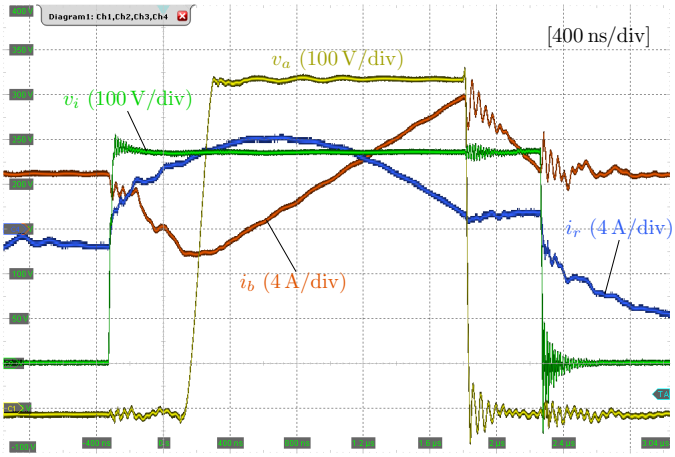
The thermometric images in Fig. 15 show significant differences in case temperature of S_{bL} while at the two operating points considered above. In spite of the lower transferred power, operation with $\varphi = 0$ gives temperatures of about 70°C, indicating significantly high losses on the transistor. Such a dissipation is not observed after properly adjusting φ, which is the degree of freedom available for modulation. By exploiting φ, ZVS for all the switches is achieved, allowing higher output power with overall lower losses, as shown by comparing Fig. 15a and Fig. 15b.

B. Power Losses Measurement

Fig. 16 shows the thermal figure of the transformer at the nominal design conditions in Fig. 10. The estimated power loss of the prototype is about 21 W. Fig. 16 also reports core and windings temperatures, showing a uniform temperature profile for the component.

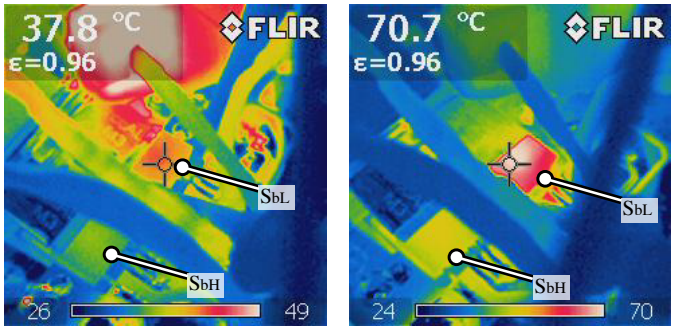


(a) ZVS for all switches at $\varphi = 0.25$ (SM 2), $V_o = 250$ V, $P_o = 2.5$ kW



(b) Non-ZVS for S_{bL} at $\varphi = 0$ (SM 1), $V_o = 250$ V, $P_o = 1.1$ kW

Fig. 14. Experimental waveforms at $V_o = 250$ V during (a) ZVS operation at $\varphi = 0.25$, $P_o = 2.5$ kW, (b) non-ZVS operation at S_{bL}, $\varphi = 0$, $P_o = 1.1$ kW.



(a) (b)

Fig. 15. Thermography of S_{bH}-S_{bL} at $V_o = 250$ V during (a) ZVS operation at $\varphi = 0.25$, $P_o = 2.5$ kW, (b) non-ZVS operation at S_{bL}, $\varphi = 0$, $P_o = 1.1$ kW.

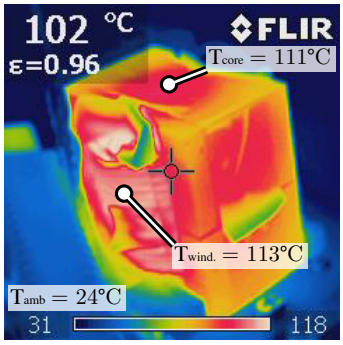


Fig. 16. Thermography of the transformer at $V_o = 400\,\mathrm{V}$, $P_o = 5\,\mathrm{kW}$.

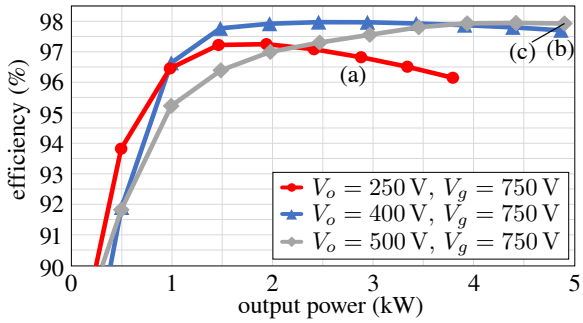


Fig. 17. Measured efficiency at minimum, nominal, and maximum output voltage.

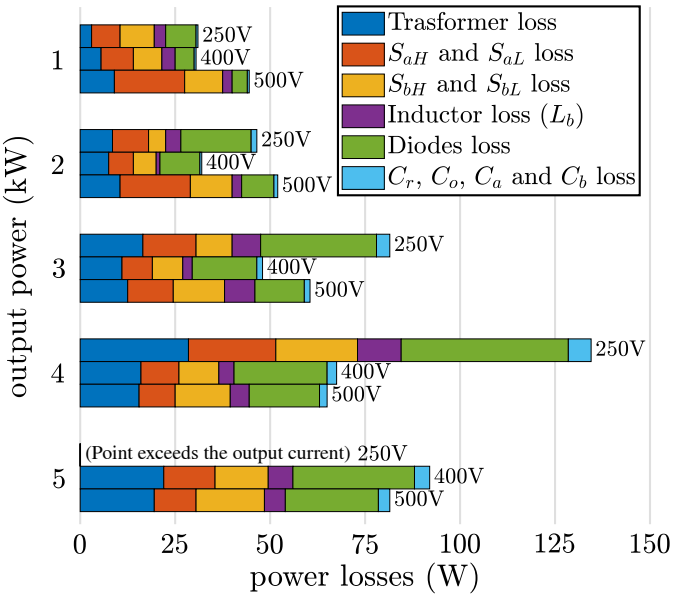


Fig. 18. Loss breakdown at different output power and minimum, nominal, and maximum output voltages.

Power dissipation was measured based on thermal measurements of the magnetic component at thermal steady-state. Approaches based on similar principles and applications can be found adopted, for example, in [43]. For the results presented herein, in particular, the thermal resistance of the component was evaluated first, by means of a test consisting in the measurement of the average temperature of the component at thermal steady-state while stimulated by a constant dc current. Temperature measurements were performed through thermal couples positioned at four different points on the component surface, two on the windings and two on the core. A thermal resistance of about $4\,\mathrm{W/°C}$ was estimated as the average of different tests at different dc currents. Then, once the component-to-ambient thermal resistance R_θ is estimated, power dissipation could be computed. Other, more advanced, thermometric approaches are possible and described in the literature, like, for example, [44]. Similar considerations can be done for the inductor losses measurement.

A similar approach was applied to estimate the power dissipation of the switches. Switches temperatures were taken considering the spot at higher temperature on the case of the devices (see, e.g., Fig. 15). Thermal resistances of $1.6\,\mathrm{W/°C}$ and $1.8\,\mathrm{W/°C}$ were estimated for the left-leg and the right-leg MOSFETs, respectively. Then, referring to Fig. 15, it is possible to estimate losses of the devices: temperatures in Fig. 15a of S_{bL} correspond to about $9\,\mathrm{W}$, temperatures in Fig. 15b of S_{bL} correspond to about $26\,\mathrm{W}$.

C. Efficiency and Loss Breakdown

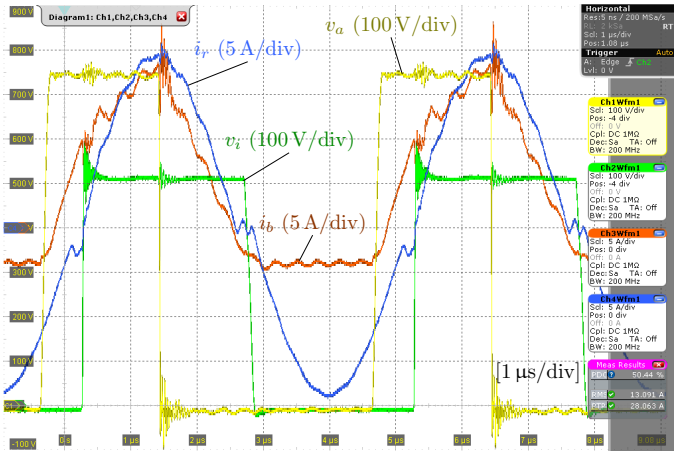
Fig. 17 shows the converter efficiency measured at the minimum, nominal, and maximum output voltage, that is, $250\,\mathrm{V}$, $400\,\mathrm{V}$, and $500\,\mathrm{V}$, respectively. Efficiency measurements were performed by means of a Keysight PA2203A power analyzer. The measured peak efficiency at minimum output voltage is 97.25%, while at maximum output voltage is 97.9%, which are both very close to the absolute maximum efficiency of 98.0% measured in nominal conditions.

A loss breakdown over the considered wide output voltage range of operation is reported in Fig. 18. The loss breakdown was performed based on the models presented in the previous sections, which have been validated experimentally by means of the thermal measurements discussed in Sect. V-B. The total discrepancy among estimations based on the described models and the collected measurements resulted lower than about 10% of the measured total power loss.

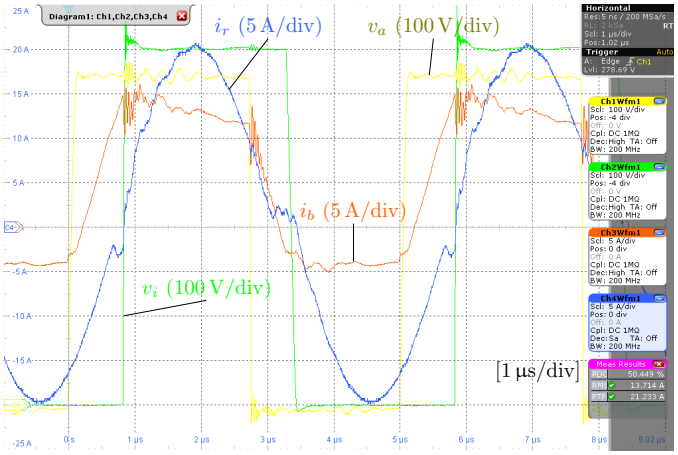
Finally, to prove ZVS operation achieved by exploiting the derived phase-shifts φ based on the analyses and considerations in Sect. III, Fig. 19 shows the converter waveforms at other relevant points of operation. Remarkably, ZVS for all the switches is achieved with minimum phase-shift of 0.2 for $V_o = 250\,\mathrm{V}$ and $P_o = 3\,\mathrm{kW}$, of 0.12 for $V_o = 400\,\mathrm{V}$ and $P_o = 5\,\mathrm{kW}$, and of 0.24 for $V_o = 500\,\mathrm{V}$ and $P_o = 5\,\mathrm{kW}$, as expected based on the discussion in Sect. III-C. The complete set of minimum phase-shifts for ZVS is reported in Fig. 7a at minimum output voltage, in Fig. 7c at nominal output voltage.

VI. Conclusion

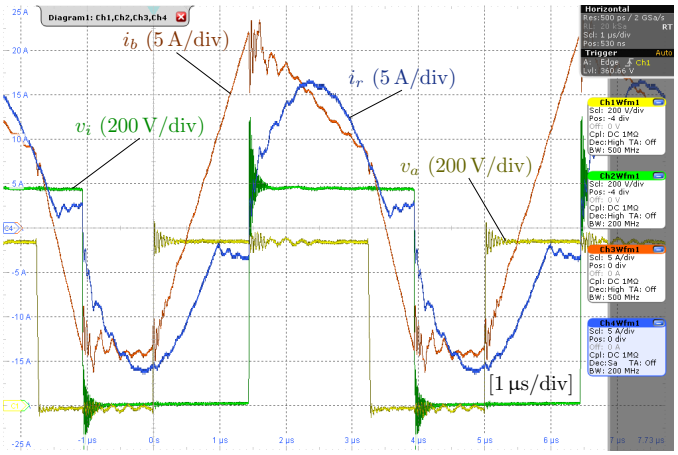
A two-stage topology is proposed in this paper for increasing the efficiency of the LLC converter, targeting battery charging applications with a wide range of operating voltages. The two stages share part of the switching components, then a coordinated operation of the stages to achieve low loss operation has been researched. The topology has been analyzed, highlighting the available parameters for modulation



(a) Converter waveforms at $V_o = 250\,\mathrm{V}$, $P_o = 3\,\mathrm{kW}$. Soft-switching transitions, $\varphi = 0.2$.



(b) Converter waveforms at $V_o = 400\,\mathrm{V}$, $P_o = 5\,\mathrm{kW}$. Soft-switching transitions, $\varphi = 0.12$.



(c) Converter waveforms at $V_o = 500\,\mathrm{V}$, $P_o = 5\,\mathrm{kW}$. Soft-switching transitions, $\varphi = 0.24$.

Fig. 19. Converter waveforms for (a) $V_o = 250\,\mathrm{V}$, $P_o = 3\,\mathrm{kW}$; (b) $V_o = 400\,\mathrm{V}$, $P_o = 5\,\mathrm{kW}$; and (c) $V_o = 500\,\mathrm{V}$, $P_o = 5\,\mathrm{kW}$. Such points refer to those ones labeled in Fig. 17. ZVS is achieved at minimum phase-shift and, then, at minimum rms currents.

and demonstrating how to exploit these parameters in order to achieve ZVS for the active switches and minimum rms current circulation. As a result, a modulation scheme has been derived for high-efficiency operation, aiming at ZVS with minimum rms currents. The design of the main components has been outlined considering the targeted application, also reporting loss evaluations experimentally validated. The reported analysis and the experimental characterizations and tests were performed on a 5- kW prototype module based on silicon-carbide (SiC) devices. The results confirmed that ZVS is crucial in order to achieve minimum total loss, which can be obtained by the derived modulation scheme. Conversion performances covering the whole power and voltage ranges have been reported experimentally, showing high efficiency over a wide range of operating conditions, recording a peak efficiency of 98.0% at 3 kW transferred power. The considered output voltage range is 250-500 V, which may be easily extended ≥ 1 kV by the series connection of more modules.

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