UNIVERSITÀ
DEGLI STUDI
DI PADOVA

Head Office: Università degli Studi di Padova

Department of Information Engineering

Ph.D. COURSE IN: Information Engineering
(IF ANY) CURRICULUM:
SERIES: XXXIV cycle

EFFICIENT SOFT ERROR TOLERANT FLIP-FLOP CIRCUITS AND DESIGN METHODOLOGY FOR CMOS DIGITAL SYSTEMS

Thesis written with the financial contribution of STMicroelectronics Pvt. Ltd.

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DEDICATION

To my father

(Late) Shri. Praveen Kumar Jain

ACKNOLEDGEMENTS

I would like to express my gratitude to many people who have played an integral role in helping me during this endeavor over all these years.

I dedicate my sincere thanks:

- To my Parents Shri. Praveen and Smt. Sharda for giving me life and take care of me.
- To my lovely wife Dr. Sonal for helping me in everything.
- To my supervisors at STMicroelectronics Mr. Andrea Mario Veggetti, Mr. Pankaj Rohilla and Mr. Pier Luigi Rolandi for allowing me to enroll in this program and for supporting me throughout this work.
- To my advisor Prof. Simone Gerardin for giving me chance to research at University of Padova and for his guidance.
- To my colleagues at STMicroelectronics Dennis Crippa, Antonio Benfante, Himanshu Choudhary, Himanshu Mittal and Marica Casargi for their invaluable contributions, discussions, and support to all our projects.
- To Dr. Marta Begatin for her guidance and support in radiation tests.
- Finally, to the Almighty, for his grace and blessings without which none of this would have been possible.

Terminology

ASIC	Application Specific Integrated Circuit
BCD	Bipolar CMOS DMOS
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CTS	Clock Tree Synthesis
DPC	Dual Phase Clocked
DPCR	Dual Phase Clocked Robust
DUT	Device Under Test
DTI	Deep Trench Isolation
DFF	D Flip-flop
FF	Flip-flop
FIT	Failure in Time
IC	Integrated Circuit
LET	Linear Energy Transfer
LVS	Layout vs. Schematic
MBU	Multi-Bit Upset
MCU	Multi Cell Upset
MOS	Metal Oxide Semiconductor
OOP	Optimal Operating Point
PIPB	Propagation Induced Pulse Broadening
PVT	Process Voltage Temperature
PLL	Phase Locked Loop
RHBD	Radiation Hardening By Design
RHBP	Radiation Hardening By Process
SEE	Single Event Effects
SEB	Single Event Burnout
SER	Soft Error Rate
SEGR	Single Event Gate Rupture
SET	Single Event Transient
SEU	Single Event Upset
SPICE	Simulation Program with Integrated Circuits Emphasis

SRAM	Static Random Access Memory
SPC	Single Phase Clocked
TID	Total Ionizing Dose
TMR	Triple Modular Redundancy
TCAD	Technology Computer-Aided Design
VLSI	Very Large Scale Integration
µC	Microcontroller

Abstract

Radiation-induced soft errors is a well-known problem in electronic designs. It happens due to ionizing radiation interaction with the semiconductor material resulting into temporary change of state. The change of state could be due to radiation particle directly affecting the storage element known as single event upset (SEU) or a single event transient (SET) in any combinational element getting latched by storage element. With shrinking feature size and increase in packing density of CMOS transistors used in electronics systems, probability of occurrence of soft errors has gone up. Specific radiation hardening design and methodologies are required to make the electronic system tolerant to radiation-induced faults. In this thesis work, radiation induced effects on CMOS circuits and various methods used to assess and mitigate them is studied. Various soft error tolerant flip-flop and latch circuits which are the most basic sequential elements used in every electronic digital system, are investigated. Each of these circuits have their own merits and demerits. These hardening techniques normally improve the radiation tolerance but degrades other parameters like area, power dissipation and speed of the circuit. Depending on the target application and radiation environment, particular hardened circuits and methods are used to meet the acceptable failure rate with least possible penalty. Moreover, design and implementation cost is another factor which is considered. A new low power robust flip-flop circuit is discussed in detail, targeted for low to medium radiation tolerance applications which promises to improve power dissipation penalty. An additional novel flip-flop circuit and design methodology targeted for high radiation environment applications is also discussed which employs spatial and temporal redundancy to overcome both SEU and SET faults and has embedded timing pre-error detection capability. This timing error sensing capability can be used at system level in many ways to make a system more efficient and adaptable to changing operating environment and long-term device degradations. Both designs were implemented and validated in ST 90nm BCD technology process using CMOS devices using two test-chips. Complete design, implementation, simulation and test details are presented in this work. Comparative analysis is done with respect to standard D flip-flop circuit and other popular hardening strictures such as dual interlocked cell (DICE) based flip-flop, and triple modular redundancy (TMR) flip-flop. Proposed design appears to provide an efficient alternative to soft error tolerant designs.

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Chapter 1. Introduction

Electronics circuits and systems are now part of almost all the applications involving computing, sensors, artificial intelligence, driving, industrial, medical etc. They have penetrated deeply into human life and become critical part of it. Key enablers for this to happen are the innovations in semiconductor integrated circuits manufacturing which has enabled technology scaling to nanometer dimensions leading to high packing density or in other words more functionality in smaller chip area, reduced power consumption with voltage scaling and higher performances. With decreasing feature sizes and reduced supply voltages, digital circuits are more vulnerable to radiation effects. Single event effects (SEEs) are particular constituent of radiation induced effects which could affect deep sub-micron devises adversely, making them to deviate from the expected behavior. SEEs are caused when radiation particles such as protons, neutrons, alpha particles, or heavy ions strike sensitive diffusion regions in VLSI designs. Historically, SEEs were troublesome for military and space applications but in recent technologies they are a threat to many terrestrial applications as well.

The study and analysis of radiation effects on circuits has been a major area of research and a lot of work has been done to devise solutions to solve this problem. The technique of designing and fabricating electronic systems to withstand radiation is called radiation hardening. Radiation hardening by design (RHBD) is one approach which has become a necessary practice while designing circuits, to mitigate SEEs. Flip-flops being key building blocks of digital circuits must be hardened to achieve required tolerance against SEEs. While employing RHBD techniques has tradeoffs between occupied silicon area, speed and power consumption, novel designs help to minimize these penalties.

This work is focused on understanding the basic mechanism of SEEs, its effect on digital circuits, and devising efficient solutions to overcome erroneous conditions arise due to it. The radiation effects are studied on flip-flops and memories designed on ST 90nm BCD technology CMOS devices through dedicated test structures, simulations, and radiation tests. Two novel flip-flop structures are designed, implemented and validated on silicon. With the help of experimental results, a comparative analysis has been performed with state-of-the-art solutions.

The thesis is organized as follows :-

Chapter 2 provides an overview of the radiation environment, radiation effects on devices and circuits, techniques to achieve radiation hardness and radiation assessment at CAD level.

In Chapter 3, various state of the art solutions for soft error mitigation are presented. These structures are categorized according to the target radiation tolerance level and their merits and demerits are discussed. Hardening techniques for memory circuits are briefly discussed. In-situ delay monitor circuits which enables efficient and reliable system design are also discussed in this chapter.

Chapter 4 presents the design, implementation, and CAD analysis details for proposed solutions. Two structures are discussed here. One low power radiation hardened flip-flop circuit offering medium radiation tolerance and another efficient multi-bit flip-flop system with embedded pre-error detection capability. The complete design methodology adopted for later solution is presented. The flip-flops are also compared with state-of-the-art solutions here.

In Chapter 5, the details of two test-chips implemented ion ST 90nm BCD technology is discussed. The test-chips are used to study radiation effects on ST's standard library offer and to validate the proposed solutions. The test setup, flow and measurements details are provided. Then, electrical and radiation test results obtained from multiple test samples are discussed and analyzed. Radiation test are conducted with Alpha, neutron and heavy ion particles.

Finally, Chapter 6 concludes the work.

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Chapter 2. Single Event Effects on CMOS circuits

Radiation is defined as “the process in which energy is emitted as particles or waves.” [1]. Radiation can cause degradation, malfunction, loss of function or even permanent damage in electronic circuits and devices [2]. The way radiation interacts with solid material depends on various factors and it could cause different problems in different materials and devices depending on these factors. These factors are type, kinetic energy, mass, and charge state of the incoming particle and the mass, atomic number and density of the target material. When a radiation particle travels through a material, it loses its kinetic energy predominantly through Columbic interactions with the electrons of that material and thus leaves a trail of ionization in its wake as shown in Figure 2-1 (ions can also interact directly with material nuclei but this reaction probability is usually significantly lower than the electronic interaction) [3]. The higher the energy of the ion, the farther it travels before being "stopped" by the material. The distance required to stop an ion (its range) is both a function of its energy and the properties of the material (primarily the material’s density) in which it is traveling. The stopping power or linear energy transfer (LET) is a function of the material through which a charged particle is traveling and refers to the energy loss of the particle per unit length in the material.

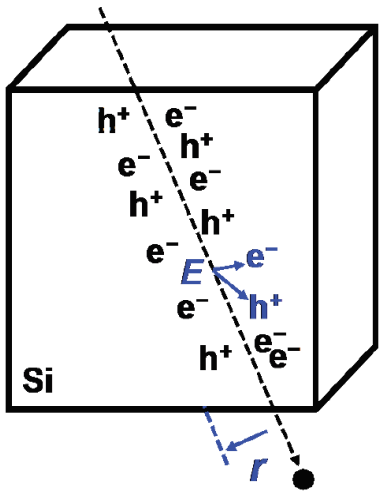


Figure 2-1 Energy Deposition of an energetic ion and resultant creation of electron hole pair, After [3]

The LET (MeV-cm2/mg) is a function of both the ion's mass and energy and density of the target material.

$$LET = \frac{1}{\rho}\frac{dE}{dx} \quad (\mathrm{MeV-cm2/mg}) \tag{2.1}$$

where dE/dx is the energy loss per unit length and ρ is the material density in mg/cm3. The maximum LET value near the end of the particle's range is called the Bragg peak [4]. Radiation particles interact with material, depositing charge by two major mechanisms: direct ionization and indirect ionization. In direct ionization, a high energy charged particle interacts directly with the electrons in the target material, breaking them free from their bound states, creating a dense track of free charge. During indirect ionization, the high energy particle collides with a nucleus in the target material, freeing that nucleus from its bound location, generating secondary particles as result of this nuclear reaction. These secondary particles then create the dense track of free charge. Depending on where the particle itself and the generated particles end up in silicon, they cause different effects in devices as shown in Figure 2-2.

The two major radiation effects on CMOS circuits and devices are

- Single Event Effects (SEEs):- Which occurs due to one-time particle strike resulting in charge generation in the sensitive volume. SEE are discussed in detail in this chapter.
- Cumulative Effects:- Damage due to radiation gets accumulated over longer duration due to permanent damages to dielectric oxide, isolation regions, lattice disruptions. Total Ionizing Dose (TID) effects [5] are one of such type of effects which affects all device types affecting their threshold voltage. TID effects are briefly discussed in this chapter later. Another type of cumulative effect known as Displacement Damage is limited to Bipolar Technologies and Optical devices which is beyond the scope this work.

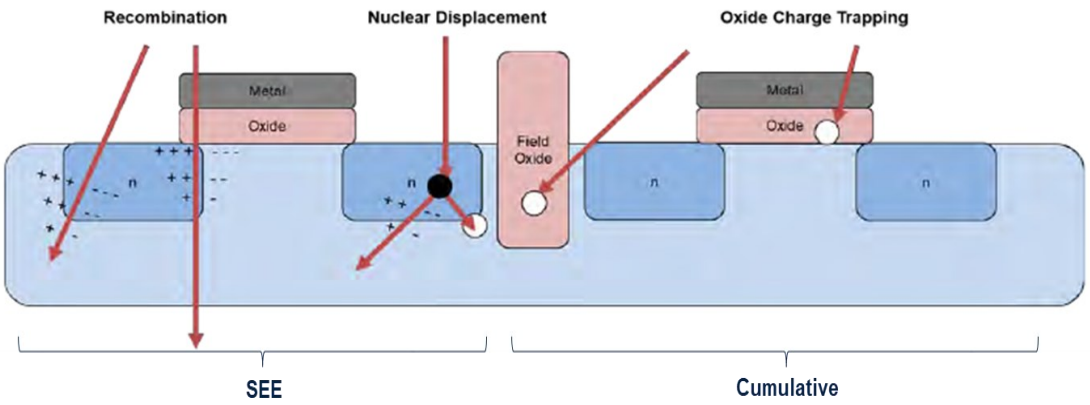


Figure 2-2 Particle Strike in Silicon showing different effects, After [6]

SEE on CMOS circuits is well studied now and failures have been reported starting from early 1970s (Figure 2-3). In this chapter, radiation environment and fundamental aspects of SEE caused by ionizing radiation is discussed.

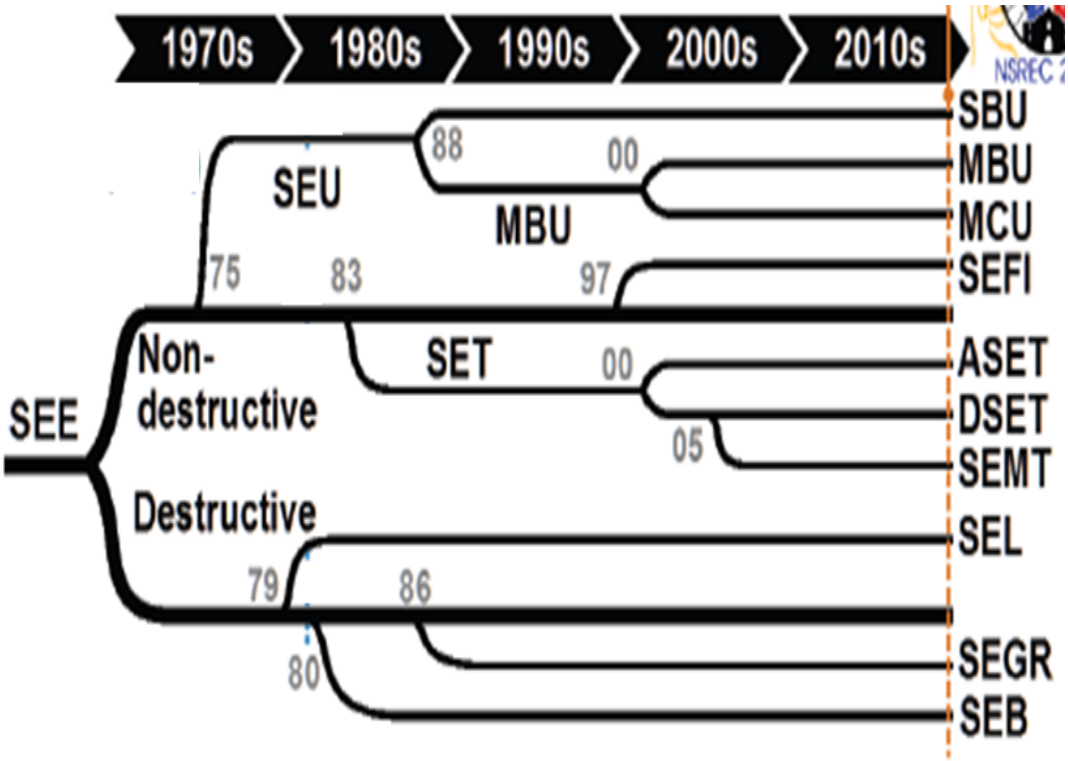


Figure 2-3 Evolution of radiation induced single event effects (SEE) in electronic devices. (Small font indicates typical year reported in literature), After [6]

2.1 Radiation Environment and Sources

Radiation is prevalent everywhere. Ionizing radiation is present on the Earth's surface as well as in space. It can interact with semiconductor devices and cause faults. The main contributors for radiation in the semiconductor devices are as follows:

1) Radioactive elements present in the packaging material

   There are radioactive impurities like Uranium and Thorium, present in the packaging materials of the semiconductor devices which tend to decay to a lower energy state [6] emitting secondary particles comprising of isotopes and alpha particles. A kinetic energy between the range 4 to 9 MeV is generated by these isotopes. The alpha particles which are emitted from these sources are one of the major sources of SEE.

2) High energy cos=mic ray particles

   Cosmic rays come from the outer space due to various solar interactions, and it reaches the Earth's atmosphere [7]. The spectrum of radiation environments typically consists of various particles such as

   - Protons and other heavy nuclei associated with solar events
   - Trapped radiation (by the Earth's Van Allen belts)
   - Galactic Cosmic Rays (GCR) that consist of interplanetary protons, electrons and ionized heavy nuclei
   - Neutrons (primarily cosmic ray albedo-neutrons or CRAN particles)
   - Photons (ϒ-rays, X-rays, UV/EUV, optical, infra-red and radio waves)

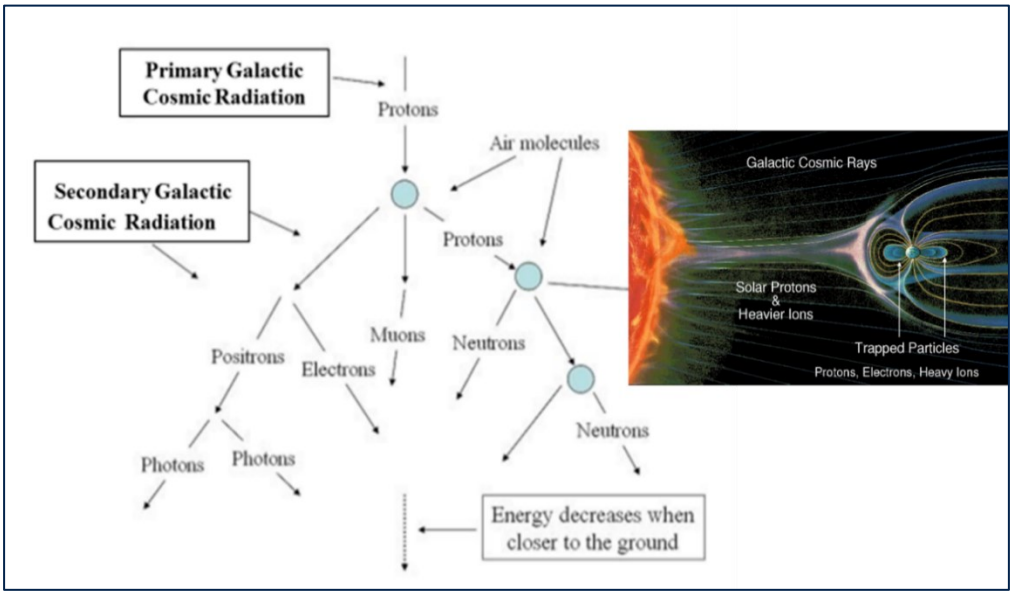


Figure 2-4 View of Cosmic Rays Causing Cascade of Particles, After [7]

Trapped particles, which are 93% protons, 6% alpha particles, and about 1% heavy nuclei, contribute the most to radiation effects in low and medium Earth orbits that pass through the Van Allen belts [8]. CRAN particles are primarily secondary cosmic ray neutrons produced by the interaction of GCR with the earth's atmosphere at about 55km above the earth surface. Secondary neutrons are the most important contributor to single event effects at altitudes below 60,000 feet. Neutron of the cosmic radiation which is having an energy greater than 1MeV can generate secondary ions when it reacts with Si nuclei, this results in Soft Errors in Semiconductor devices at terrestrial level.

3) Low energy neutrons

   Interaction between low energy Neutrons (< 1MeV) with isotope Boron-10, releases Lithium nucleus of energy 0.84MeV, gamma rays with energy of around 400KeV energy and an alpha particle of energy 1.4MeV. This one is the common source of SEE especially in circuits having BPSG (Boro-phospho-silicate glass) which is commonly used in semiconductor device fabrication for intermetal layers isolation. The BPSG includes additives of both boron and phosphorus [9].

A summary of the radiation environment at different elevation level is given in Table 2-1.

Table 2-1 Radiation Environment at different Levels, After [7]

ENVIRONMENT (ELEVATION LEVEL)	PARTICLES / RAYS AFFECTING / SOURCE OF SE	LET / E_T	FLUX	MAIN CONSTITUENTS	COMMENTS / ORIGIN
Space (Outer space)	Cosmic ray particles	up to 10^{19} eV		92% protons 6% alphas 1% heavy nuclei	Due to Supernova explosions, Pulsars, & galactic explosions
Terrestrial environment (<60,000ft)(Sea level / ground level)	Cosmic particles	10^{11} eV		96% neutrons <1% primary particles (~0% solar cosmic)	
	Alpha particles	4 – 9 MeV			Due to packaging material consisting of thorium and uranium
		5.3 MeV		Polonium (alpha emitter)	Naturally occurring radioactive lead 210 decays into Bismuth (210) and then Polonium (210).
	Neutrons	< 1MeV (~25meV)	56.5cm^{-2} s^{-1}		interacts with Boron (10) -> B10 makes up about 20% of B11 used as a p- type dopant -> alpha(1.47 MeV) and Li particles (0.84MeV)formed
		> 1MeV (100MeV to > 10GeV)	10 / cm^2/hr		Causes inelastic energy transfer to Si.
	High power sources in proximity			Power cables and supplies; Power distribution units; Universal power supplies; Lighting systems; Power generators	SEUs can occur if power distribution units, power generators, or lighting systems are too close to the chassis or if multiple power cables are on or beside the chassis
Terrestrial environment (12000m)	Secondary cosmic particles		100 / cm^2	proton, neutrons, pions, muons, electrons, and photons	Due to Interaction of cosmic rays with atmospheric particles

2.2 SEE Basic Mechanism

When radiation particles such as protons, neutrons, alpha particles, or heavy ions strike sensitive diffusion regions in VLSI designs, SEEs are caused leading to potential system failures. All single-event effects are caused by the same fundamental mechanism: collection of charge at a sensitive region of a microcircuit following the passage of an energetic particle through the device as shown in Figure 2-5. Radiation effects from heavy ions are most often due to direct ionization while the vast majority of SEEs from protons are due to indirect ionization through collisions with heavier nuclei except for low energy protons which cause upsets from direct ionization. SEEs from neutrons, are entirely due to indirect ionization, as they do not cause direct ionization owing to their neutral charge.

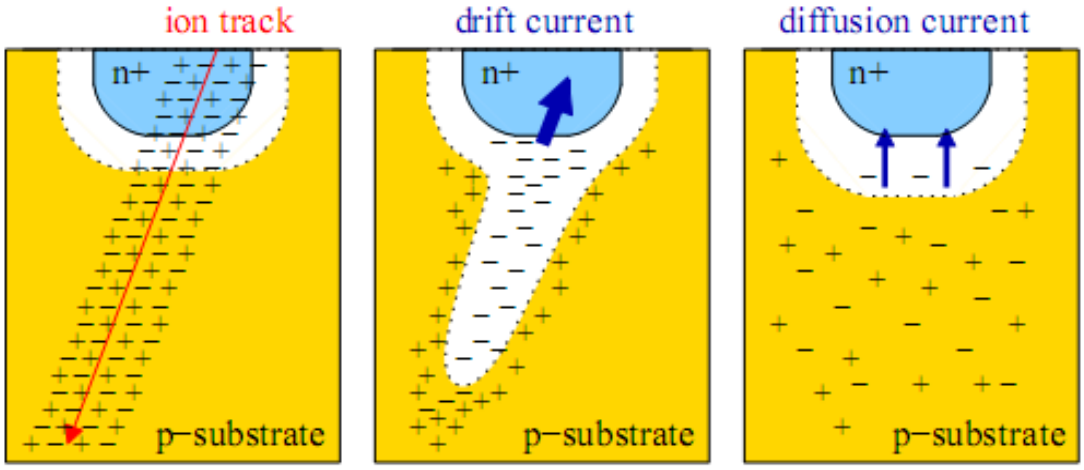


Figure 2-5 Particle Strike in semiconductor Device – Charge Generation and Collection, After [3]

There are three stages involved in the formation of a SEE – charge generation, charge collection and circuit response. Charge generation is decided by the particle's mass and energy and the properties of the materials it passes through. Charge is generated from a single event phenomenon generally within a few microns of the location of the incident ion. In silicon, one electron-hole pair is produced for every 3.6 eV of energy lost by the impinging radiation. As silicon has a density of 2328 mg/cm3, it is easy to calculate from equation (2.1) that an LET of 97 MeV-cm2/mg corresponds to a charge deposition of 1 pC/μm. Hence, the amount of collected charge in silicon can be given by the formula

Q=0.01036.LET pC /μm (2.2)

Thus, the collected charge (Q_c) for these events is from 1-100 fC depending on the type of ion, its trajectory, and its energy over the path through or near the junction. There are basically three mechanisms that act on the charge deposited by an energetic particle strike: 1) carriers can move by drift in response to applied or built-in electrical field in the device, 2) carriers can move by diffusion under the influence of carrier concentration gradients within the device, or 3) carriers can be annihilated by recombination through direct or indirect processes. The process of drift is followed by the process of Diffusion. Diffusion, it is a slow process and thus takes more time as compared to the drift process.

The steps of drift, diffusion and recombination causes generation of the transient pulse of current at a terminal of the device. There is a short-lived initial spike observed in the current pulse. The transient in the rising time is caused due to the Drift. The shape that current pulse attain can be written mathematically in the form of double exponential current pulse :-

$$Ip = Io(\, e^{-t/Tf} - \, e^{-t/Tr}) \qquad (2.3)$$

Where, Ip = transient current pulse, Io = peak current, Tr = rise time for the current pulse, Tf = fall time for current pulse. The graph of the current is represented in the Figure-1.3. This double exponential current pulse has a rise-time in range of tens of pico-seconds(ps) and a fall time of around 200 ps to 300 ps.,

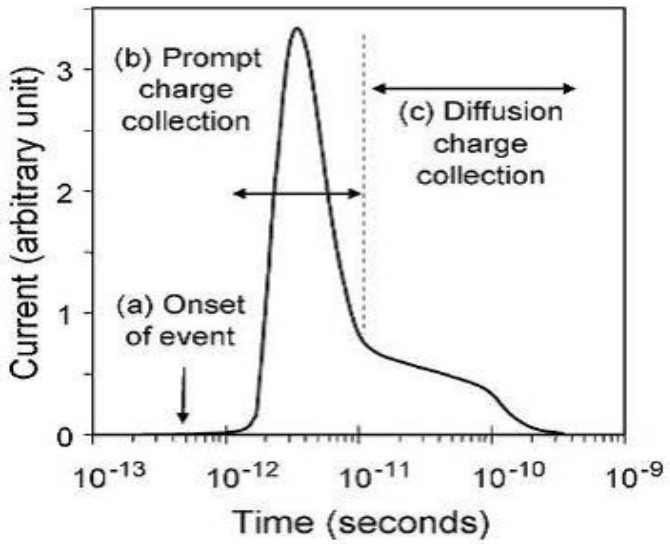


Figure 2-6 Radiation Strike induced current pulse waveform, After [3]

2.3 Types of SEE

Single-event effects may be broadly characterized as either non-destructive (causing a soft error) or destructive SEE (resulting in a hard error). The error is “soft” because the circuit/device itself is not permanently damaged by radiation – if new data is written to the bit, the device will store it correctly – in contrast, a “hard” error is manifested when the device is physically damaged such that improper operation occurs, data is lost, and the damaged state is permanent. Different types of soft and hard errors are shown in Figure 2-7.

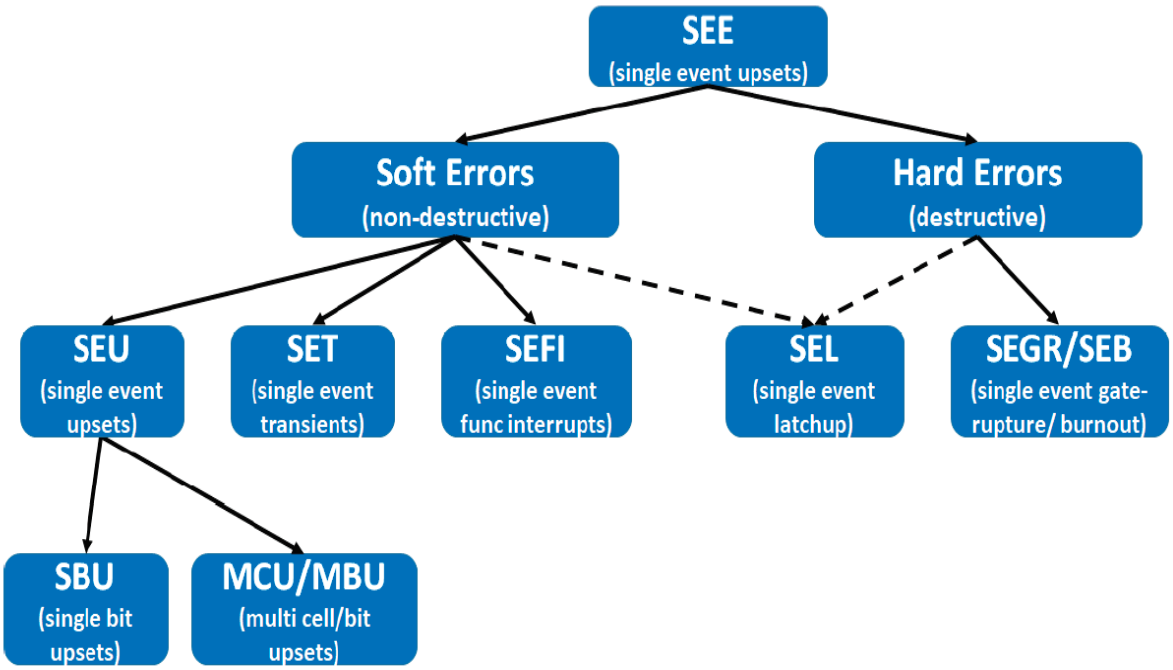


Figure 2-7 Types of SEE, After [10]

2.3.1 Single Event Upset (SEU)

An SEU is a static upset in storage cells such as Static Random Access Memory (SRAM) cells, latches and flip-flops. The upset rate due to such an event is largely independent of the clock frequency [11]. This can be better understood by Figure 2-8 where a conceptual depiction of the behavior of a simple two-inverter-based latch after a radiation strike is shown. The output voltage of the struck inverter (V_A) drops abruptly because of the collected charge Q_c. This drop (the first edge in the bottom signal chart) is then transferred to the second inverter output (V_B) but with a certain propagation delay of t_{pd}. During t_{pd}, the pull-up pMOS transistor of the first inverter can provide a current to recharge the node. If this recharging process is faster than t_{pd}, V_A can return

to the original level (no SEU) else it will result in a change of V_B and new a value is stored in the latch.

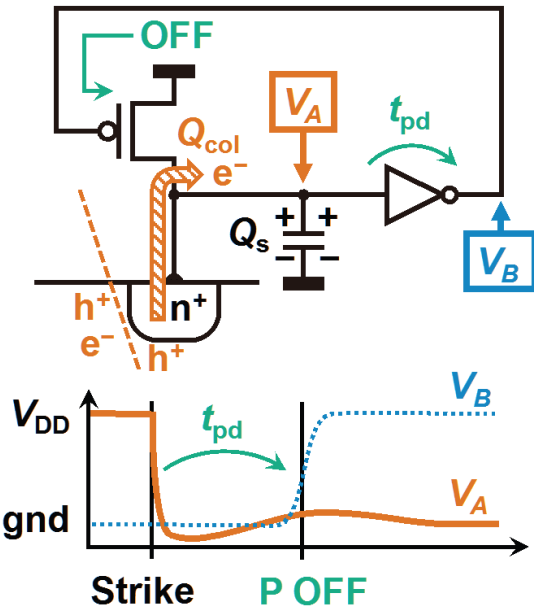


Figure 2-8 Conceptual Depiction of Particle strike on latch element, After [6]

Depending on the number of bits flipped due to a single particle strike event, SEUs can further be classified as Single-Bit Upsets (SBU) and Multi-Cell or Multi-Bit Upsets (MCU/MBU). MCUs typically refer to upsets along both bit-line and word-line directions in a memory array, while MBUs are used to refer to upsets strictly along the word-line direction (i.e. within the same word). While MCU/MBU are usually a small fraction of the overall SEUs, they may render error correction schemes less effective without appropriate memory interleaving to tackle such events. A pictorial representation of a memory array with different bit interleaving configuration is shown in Figure 2-9 (interleaving distance 8) and Figure 2-10 (interleaving distance 4). The red spot highlights the affected cells due to a radiation strike. In case of higher interleaving distance (Figure 2-9) only a single bit of a word is affected despite of the fact that there are MCUs in array whereas for lower interleaving distance (Figure 2-10), two bits of the same word gets affected due to a radiation strike resulting in MBU. Single-Event Functional Interrupts (SEFI) are SEUs that happen in a critical register such as those found in field programmable gate arrays (FPGAs) or DRAM control circuitry, so that the error causes the product to malfunction. Digital functions most likely to cause SEFIs are clock and control trees, phase locked loops, counters,

address registers and poorly regulated power networks. Such events typically require a reset or power cycling.

Databit 0								Databit 1								Databit 2							
56	57	58	59	60	61	62	63	56	57	58	59	60	61	62	63	56	57	58	59	60	61	62	63
48	49	50	51	52	53	54	55	48	49	50	51	52	53	54	55	48	49	50	51	52	53	54	55
40	41	42	43	44	45	46	47	40	41	42	43	44	45	46	47	40	41	42	43	44	45	46	47
32	33	34	35	36	37	38	39	32	33	34	35	36	37	38	39	32	33	34	35	36	37	38	39
24	25	26	27	28	29	30	31	24	25	26	27	28	29	30	31	24	25	26	27	28	29	30	31
16	17	18	19	20	21	22	23	16	17	18	19	20	21	22	23	16	17	18	19	20	21	22	23
8	9	10	11	12	13	14	15	8	9	10	11	12	13	14	15	8	9	10	11	12	13	14	15
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7

Figure 2-9 Memory Array Matrix with bit interleaving distance 8

Databit 0				Databit 1				Databit 2				Databit 3				Databit 4				Databit 5			
28	29	30	31	28	29	30	31	28	29	30	31	28	29	30	31	28	29	30	31	28	29	30	31
24	25	26	27	24	25	26	27	24	25	26	27	24	25	26	27	24	25	26	27	24	25	26	27
20	21	22	23	20	21	22	23	20	21	22	23	20	21	22	23	20	21	22	23	20	21	22	23
16	17	18	19	16	17	18	19	16	17	18	19	16	17	18	19	16	17	18	19	16	17	18	19
12	13	14	15	12	13	14	15	12	13	14	15	12	13	14	15	12	13	14	15	12	13	14	15
8	9	10	11	8	9	10	11	8	9	10	11	8	9	10	11	8	9	10	11	8	9	10	11
4	5	6	7	4	5	6	7	4	5	6	7	4	5	6	7	4	5	6	7	4	5	6	7
0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3

Figure 2-10 Memory Array Matrix with bit interleaving distance 4

2.3.2 Single Event Transients (SET)

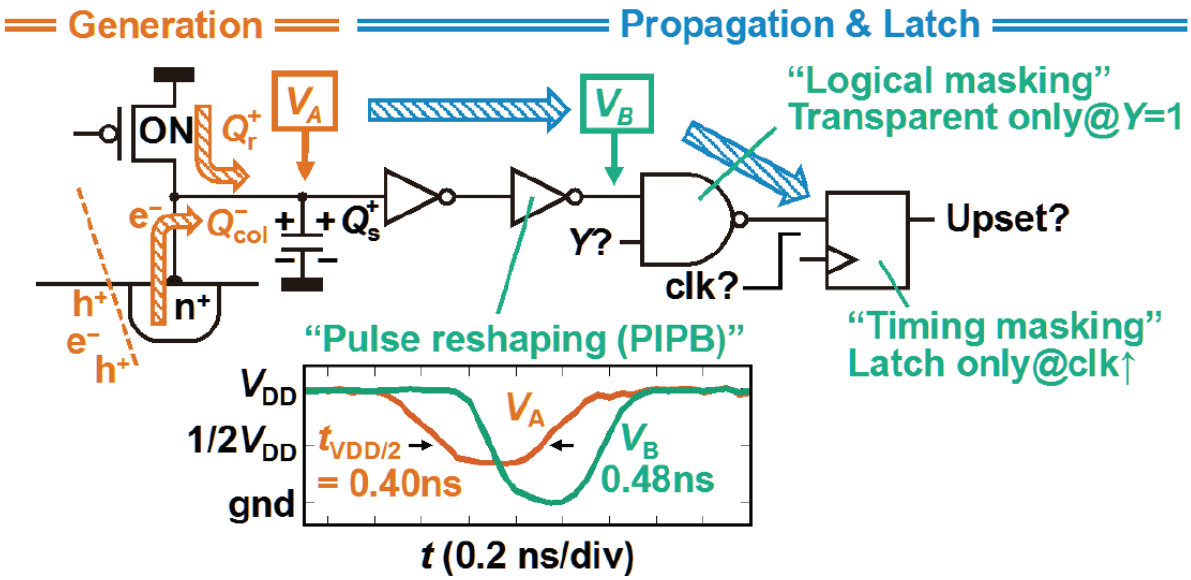


Figure 2-11 Basic Mechanism of SET. The bottom waveforms were SET pulses measured at different locations on an inverter chain, After [6]

For sequential CMOS ICs, an energetic particle strike may cause a transient voltage perturbation, called an SET, which propagates through the circuit and may become stored as incorrect data, causing disruption of the circuit operation. An SET

will result in an error if the SET pulse arrives at a storage node so as to get latched. A conceptual depiction is shown in Figure 2-11. An SET event travelling through a combinational path is shown. On radiation strike V_A abruptly drops due to Q_c and a transient pulse is created. This pulse propagates through the combinational path to V_B and pulse shape gets altered. This pulse can be logically masked if Y = 0 else it will reach to input of the storage cell. If this SET pulse arrives during the set-up-and-hold time of the primary latch, it will be latched and result in an error. Thus, upset rates due to SETs depend on the pulse width of the SET and the clock frequency [12] [13]. With increasing clock frequency, there are more latching clock edges to capture an SET. SETs in analog electronics are referred to as ASET while those in digital combinatorial logic are referred to as DSET. SEE can cause multiple transients as well through the same mechanism as MCUs. These are called single-event multiple transients (SEMTs). The probability of SEMTs is increasing with device scaling but the probability of SEMTs being captured by storage is pretty low [13].

2.3.3 Single Event Latchup (SEL)

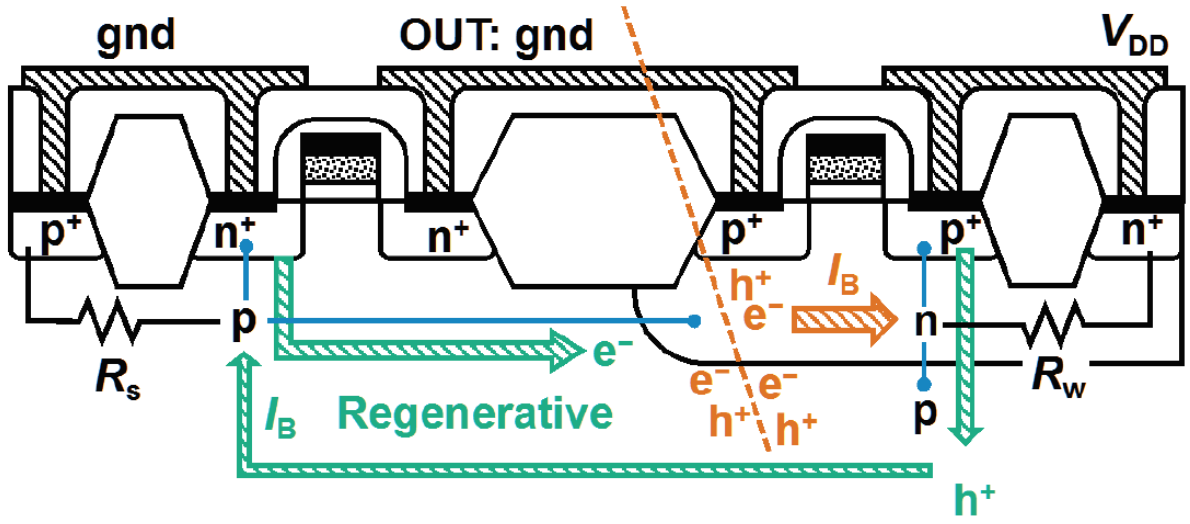


Figure 2-12 Basic Mechanism of SEL, After [6]

SEL may or may not be destructive. Due to the proximity of semiconductor regions in CMOS transistors, they contain parasitic bipolar structures as shown in Figure 2-12. An SEL happens when an ion strike triggers the parasitic PNPN structure present in CMOS devices creating a low resistance path between the power and ground. A full chip power cycle is typically needed to recover from SEL. SEL is generally non-destructive with external resistances to limit the current. However, if enough current is drawn it can result in catastrophic damage to metallization and junctions leading to a hard error.

2.3.4 Other Destructive Effects

Single-Event Burnout (SEB), and Single-Event Gate Rupture (SEGR) are other destructive SEEs which permanently damages the device. SEB typically occurs in power devices where an ion strike could lead to destructive burnout due to high current conditions caused by junction breakdown and thermal runaway [14]. SEGR results in rupture of the gate dielectric due to the high electric field created by an ion strike [14]. SEGR impacts power MOSFETs and non-volatile structures. Both SEB and SEGR are destructive events that lead to hard fails. These effects are beyond the scope of this work.

2.4 SEE Prediction

With increasing penetration of electronic devices in various applications and increasing chip density in these electronic systems, the probability of failure due to SEEs has gone high. System designers must perform failure rate assessment of their designs for the target application as per the radiation environment and product lifetime. First of all, basic measurement terms used for SEE prediction are defined followed by methods for SEE prediction using dedicated radiation tests and by computed aided design (CAD) simulations.

2.4.1 Basic measurement terms used to quantify SEE

Critical Charge :- Minimum charge required to be deposited on the node in order to cause a flip in the state of that node. The critical charge at the node which is under the observation can be calculated by doing the integration of the minimum current pulse required to cause the flip (Equ. 2.3) under the time period of the pulse. This can be shown in the equation 2.4.

$$Qcritical = \int_0^t Imin(t)dt \qquad (2.4)$$

Cross-section :- The concept of a cross section is used to express the sensitive area of a circuit which can interact with particle to cause an adverse impact on circuit functionality. The bit cross section indicates the sensitivity of a bit to a certain particle. It is defined in equation 2.5.

$$\sigma = \frac{number\ of\ errors}{fluence \cdot number\ of\ bits} \qquad (2.5)$$

It is measured in cm^2. The calculated values are usually plotted and fitted as continuous wave using Weibull distribution function [5] given by equation 2.6.

$$XS = XS_{sat}\{1 - \exp\left(-\left(\frac{LET - LET_{th}}{W}\right)^{S}\right)\} \qquad (2.6)$$

Where XS_{sat} is the cross-section at saturation (high LET), LET_{th} is the threshold LET to observe the event, S and W are shape and width fitting parameters respectively. An example of a cross-section curve fitted with Weibull Distribution function is shown in Figure 2-13.

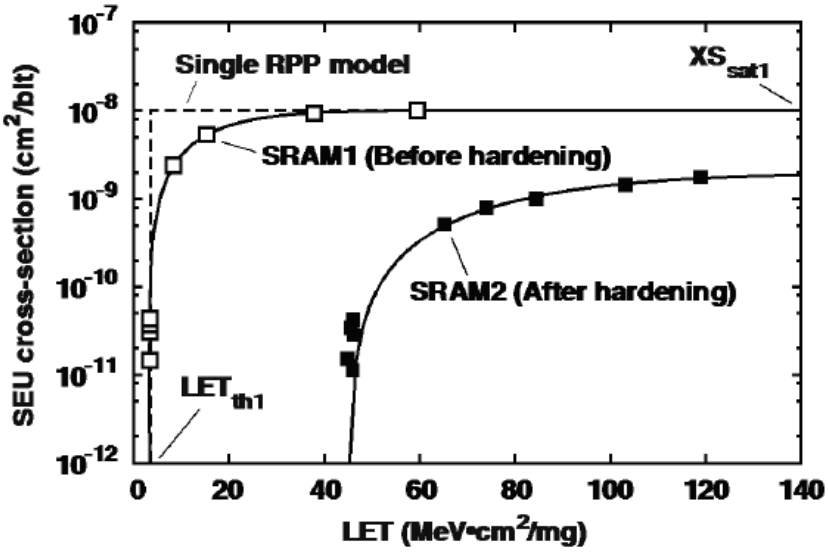


Figure 2-13 Cross-section representation example curve, After [6]

Soft Error Rate (SER) :- The rate at which soft errors occur is called soft error rate (SER). The unit of measure commonly used with SER and other hard reliability mechanisms is failure in time (FIT). One FIT is equivalent to one failure in billion hours of device operation. For one mega bit cells FIT_Mb [#err/(Mb*Gh)] is defined by equation 2.7.

$$FIT\_Mb = Natural_{RadFlux} \times \frac{\#errors \times (10^6 \times 10^9)}{Test_{RadFlux} \times TestTime \times \#cells} \qquad (2.7)$$

Natural Radiation Flux is the flux present in nature related to the specified particle [#particle/(cm^2*h)]

- Neutron: it is considered the Flux at New York latitude and see level altitude that is 13 Neutrons /(cm^2*h)
- Alpha: it basically depends on impurities in silicon and package; different Alpha emissions categories are defined:
    - Standard: 10 – 0,01
    - Low Emission (LE): ≤ $1*10^{-2}$
    - Ultra Low Emission (ULE): ≤ $1*10^{-3}$
    - Hyper Low Emission (HLE): ≤ $5*10^{-4}$

2.4.2 SEE prediction through radiation test

SEE testing is required to determine the presence and characteristics of single event induced faults on target device and technology. Through dedicated radiation tests only sensitivity of process and design can be estimated accurately. It can help in identifying vulnerable areas of the circuit where appropriate mitigation technique can be deployed to overcome it. Tests can be performed in real time in a radiation environment or accelerated tests can be performed in radiation test facilities. Real time tests are obsolete now, as it is impractical to wait for a radiation event to occur on chip in its normal environment. With the advent of particle accelerators and controlled radiation sources the tests are carried out in accelerated manner at specific test facilities. Normally, broad beam based tests are conducted with Alpha, neutron and Heavy Ion particles which covers largely the entire radiation spectrum where the device would operate. The basic principle of SEE test is that a device is exposed to a known fluence of certain particle beams, during or after which the errors are observed. The radiation response depends on various factors such as the operating condition of device (bias, frequency and temperature), type of radiation (energy, LET etc.) and angular positioning. Hence, comprehensive testing varying various factors is needed to completely understand and quantify the effects [15]. In this dissertation, broad beam tests based on alpha, neutron and heavy ions are conducted to study the SEE on ST 90nm process and to validate the effectiveness of proposed radiation solutions. Other test methods include focused beam tests such as pulsed laser test which are used to identify sensitive areas of a circuit and vulnerability to SEL. It is not discussed in this work.

While radiation tests provide an accurate estimate of radiation sensitivity of the target device or circuit, it is a very costly test procedure and moreover it's more costly to do re-spin to fix faults. Also, radiation test facilities are very limited in number and there is a long queue to get the product tested. Considering these factors CAD assessment of SEE is very important and cost saving.

2.4.3 CAD assessment of SER

SER Analysis is complex at CAD level due to vast degree of possibilities of particle interaction with devices, and due to randomness of event in time and space etc. With help of advanced CAD simulation tools, modelling, and datasheets, assessment of SER effects has become partially feasible. CAD assessment can be done at different levels

Transistor Level : With the help of advanced CAD tools which perform device level simulations emulating accurately the interaction of different radiation particles with material like Technology Computer Aided Design (TCAD) from SYNOPSYS. Particles with different energy, size and incident angles can be simulated. But this tool cannot be used at circuit level.

Circuit Level:- Spice simulations using charge injection models can be used to perform radiation effect simulation on circuits like flip-flops or memory cells or latches or combinatorial cells. Many models are presented in literature to accurately depict the SEE. With the help of Layout definition coupled with Monte Carlo simulation runs for process variations, an accurate SEE analysis can be performed. One such system is shown in Figure 2-14.

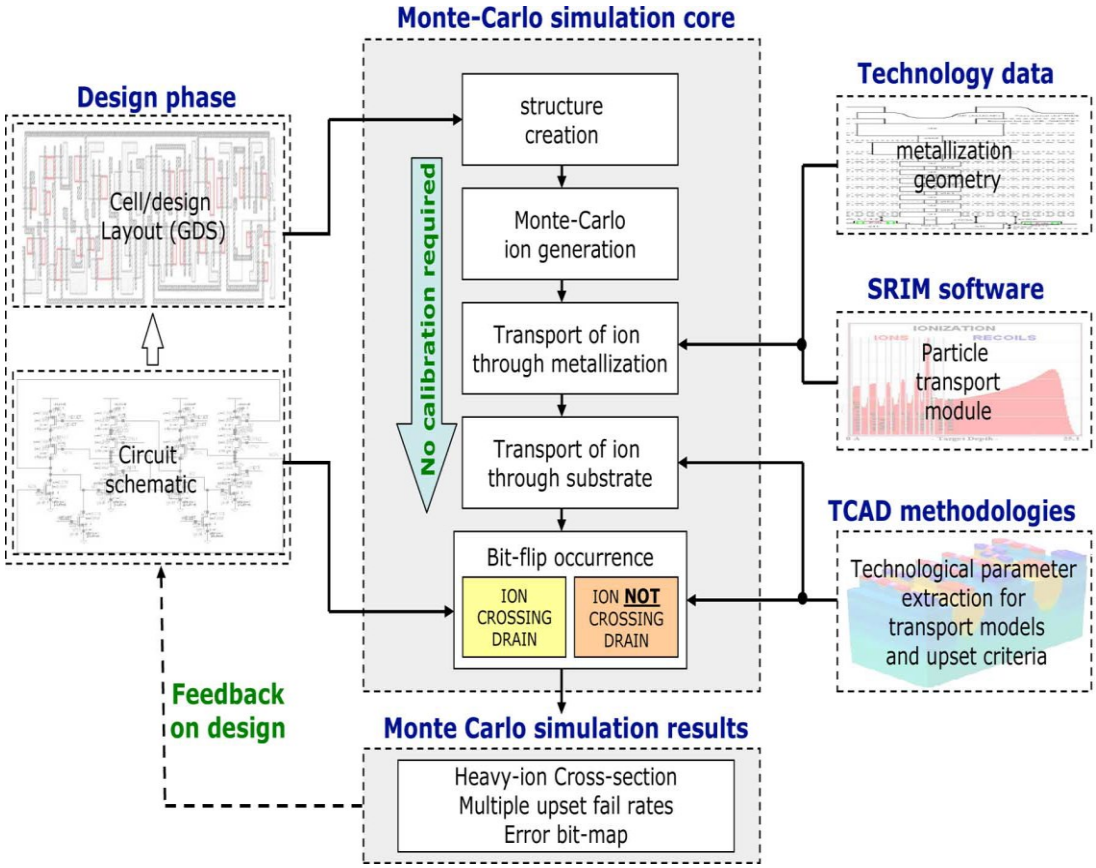


Figure 2-14 A typical Circuit level flow for SER assessment at CAD level, After [16]

System Level:- At this level mostly functional simulations can be performed based on high level digital simulation tools and verification environment. Fault injections in verification environment can be done in a random manner on circuit nodes to find the sensitive ones which can directly impact the functionality of system. Further the system can be mapped on FPGA or other prototype boards where fault injection can be done accelerating the FIT estimation task. Another way is to do bottom-up SER estimation based on components used in SoC and their radiation tolerance data.

In this work, a bias dependent current pulse model defined in [17] is used for circuit level SEE simulations. For digital systems, random fault injection in digital verification environment based on CADENCE tools is used to validate the effectiveness of proposed solutions.

2.5 SEE Mitigation

There are several methods for mitigating the effects of radiation. Radiation effects can be mitigated by using specific fabrication process, package type or through design [18]. Radiation effects can be mitigated by using design techniques at all levels of the system. From the basic structure level to the circuit level to the system level, there are methods that can be implemented to mitigate all types of radiation effects [19] [10].

2.5.1 Radiation Hardening By Process (RHBP)

Radiation Hardening by Process (RHBP) is done by carefully selecting the starting material or by modifying the process and/or the design of device primitives used to create a semiconductor device [18]. Modification is typically done by adding or changing a process step without impacting the performance or normal operating characteristics of the device. Most of the commercial foundries have now started to deploy robust process steps and materials to mitigate SEEs but these come at extra cost as modifying fabrication processes is expensive and may only be feasible for specific applications. This method of hardening is not considered for discussion in this work.

2.5.2 Radiation Hardening By Design (RHBD)

Radiation Hardened by Design (RHBD) uses design techniques implemented in a standard commercial foundry to make a non-hardened process hard to a certain degree or it can also be implemented in a dedicated hardened process to further enhance the radiation tolerance. The work carried out in this dissertation and presented in this report is based on RHBD principles only. Some of the basic concepts used for RHBD are described here.

2.5.2.1 Layout Level Hardening Techniques

A robust layout design is a must for overall design hardening against radiation. A weak chip layout would result into higher SER and could also lead to SEL in the chip. For SEL mitigation substrate contacts can be placed closer to reduce the substrate resistance to avoid SEL. The impact of substrate placement distance on SER was presented in [20]. Using well isolation like deep trench isolation also reduces the probability of SEL [21] [19] [10]. For SER mitigation most important thing to implement during layout implementation is Critical node separation in layout [22] [23].

2.5.2.2 Increasing the Q_{crit} of nodes

The very basic design technique to mitigate SEEs is to increase the overall critical charge (Q_{crit}) of the critical nodes, so that it becomes more difficult for an SET/SEU to

occur. The Critical Charge for any circuit node would be directly proportional to the node capacitance and power supply. Therefore, this can be achieved by increasing the device sizes (W and L), increasing the MOS junction capacitance by making bigger diffusion area, increasing fanout and increasing the operating supply voltage.

2.5.2.3 Hardware (Spatial) Redundancy

This involves adding redundant circuit elements in design to store the information at multiple places. The output is based on voting mechanism or some other advanced method. A popular methodology known as triple modular redundancy [24] is shown in Figure 2-15. Here triplication of storage elements is done, and the flip-flops are placed spatially apart, and the outcome is decided based on the voting mechanism. This is the most effective method for SEUs as the probability of the same particle affecting two storing elements placed at safe distance apart is very low. However, data corruption can still occur if all redundant elements capture wrong data from common input affected by SET in the combinational path or the voter logic of previous stage flip-flop.

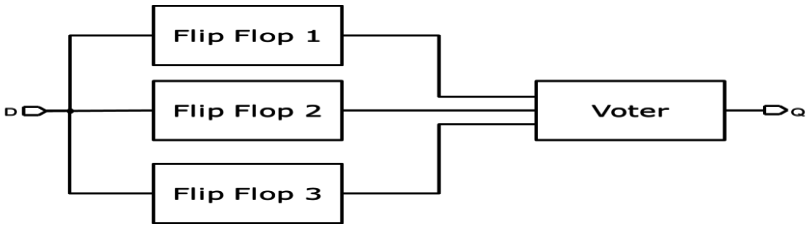


Figure 2-15 Triple Modular Redundancy Flip-Flop, After [24]

2.5.2.4 Temporal Redundancy

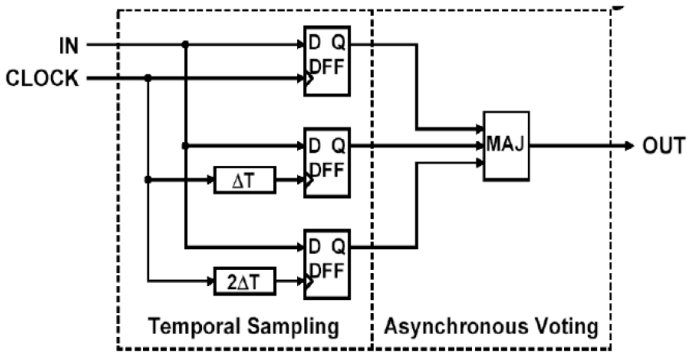


Figure 2-16 Temporal Redundancy – Data is sampled multiple times ∆T time apart, After [24]

The Temporal redundancy concept involves adding the redundancy in time domain. This is mainly employed against SETs in which the same device or data path is

sampled 3 times and the results stored and voted as shown in Fig 1.7. One of the side effects of using this technique is that it limits the maximum speed at which the circuit can operate. If the delay is long enough it will filter out the signal [24].

2.5.2.5 Logical Correction

This involves using error correction and detection algorithms (EDAC) like Hamming Codes, Reed-Solomon codes etc. During write operation, parity bits are computed based on the EDAC algorithm used and stored in the memory in extra memory bits alongside original data. During read operation, stored data along with parity bits are read and decoded, and error free data is passed to the output [10].

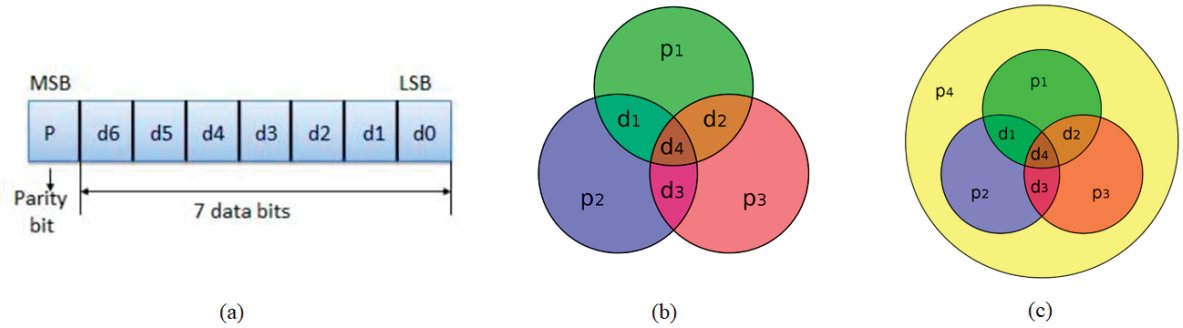


Figure 2-17 (a) Illustration of parity bit used for error detection and (b) a (7,4) Hamming code used for error correction, and (c) (8,4) extended Hamming code (SEC-DED) , After [10]

2.5.2.6 System level

Through architectural changes in processor [25] [26] or through software SEE fault can be mitigated, Processors can have error detection and recovery modules in place at various stages so that errors which occur can be detected and then the processor can enter in recovery phase. Alternatively, through efficient software involving multiple checkpoints and storing critical information at multiple places the SEE errors can be avoided or recovered.

Based on the methods discussed above, there are many designs reported in literature. While it is not possible to discuss all the published techniques, the most common techniques which are found to be relevant to this work, are discussed in 0.

2.6 Summary

In this chapter, an overview of SEE has been discussed. The basic mechanism of SEE shows how radiation interacts with silicon. The various sources of radiation in space as well as terrestrial level indicates radiation is present everywhere and even terrestrial applications can have significant failures. A study on different types of SEE reveals that SEUs and SETs are the main constituents of soft errors. With technology shrinking multiple node charge sharing leads to single event multiple upsets and single event multiple transients. The basic concepts used for radiation hardening are discussed and the importance of RHBD is understood. Through application of redundancy in circuits and increasing Q_{crit} of sensitive nodes hardening of circuits can be done. SEE prediction is very important while designing radhard systems and it can be done through radiation tests and at CAD level as well. The measurement terms like Q_{crit}, FIT rate, and cross-section are presented which are used in this work.

Chapter 3. RHBD Sequential Elements and In-Situ Timing Monitors

RHBD is a cost-effective solution for SEE mitigation to achieve required robustness levels as per the target application and environment. A lot of work has been done in the domain of robust circuit designs for different application types. There are various spatial, temporal and layout level methods of hardening that can be deployed to harden the latch, flip-flop and memory circuit against SEE. These hardening methods impose penalty in terms of power, performance, area and overall development cost. Therefore, appropriate mitigation methods should be used depending on the target application and radiation environment. In this chapter various hardening techniques reported in literature are discussed along with their pros and cons. These techniques are classified in terms of their suitability to tolerance requirement. Then, radiation hardening methods used for memory circuits is also discussed. Further, work done to enable the digital system to adapt to slow device degradations and to changing operating environment is discussed. These are based on in-situ timing monitors. They improve overall reliability and efficiency of the digital system.

3.1 RHBD Flip-flops and Latches

A latch or flip-flop is basic storage element in sequential circuits. Latches and flip-flops have two stable states and can be used to store state information. A latch is level triggered circuit which captures data during either the clock-high or clock-low state, while a flip-flop is clock edge triggered, which is designed using two latches. The design of a standard D-flip-flop circuit formed using two latches is shown in Figure 3-1 wherein an illustration of an SEU in the second latch is also demonstrated. As can be observed, each latch is designed using basic back-to-back connected inverters, wherein the feedback loop is controlled by the state of the clock. A latch is said to be in the hold state when the loop is closed. In the hold state, a latch can be upset by a radiation event at one of the off-state devices in the latch. As described in section 2.3.1, an SEU in a latch occurs when the voltage transient created by the radiation strike is longer than the feedback loop delay of the latch.

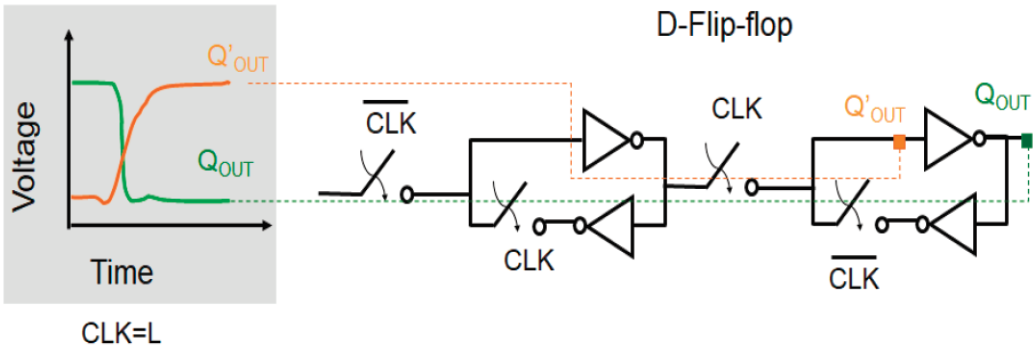


Figure 3-1 Design of a standard D-flip-flop formed using two latches and illustration of SEU in the secondary latch, After [10].

Latches and flip-flops are prone to both SETs and SEUs. Many circuits based on the RHBD concepts mentioned in section 2.5.2 are reported in literature. The main parameters for evaluating such circuits are tolerance level achieved against SEUs and SETs, impact of hardening on area, power and timing, and design cost involved. The circuits are characterized depending on the radiation tolerance they can achieve. This is for using appropriate circuit in the application depending on its target failure rate.

3.1.1 Low Radiation Tolerance

The circuits belonging to this category provide partial immunity to SEU to improve the FIT rate of the system with lower penalties. They are suitable for soft radiative environments. These circuits require cell re-design as standard library cells cannot be used as is. The very basic concept of hardening used here is increasing the Q_{crit} of storage nodes. As discussed, earlier Q_{crit} of a node can be done by simply increasing the device size but it may not be always effective as with increasing sizes the sensitive volume also increases [27]. There are some innovative structures reported which increase the Q_{crit} without impacting sensitive volume much. One such method is hysteresis based latch hardening reported in [28] [29]. In Figure 3-2 a robust Schmitt trigger latch is shown which is based on a Schmitt trigger inverter. This configuration delays the impact of a radiation strike to reach the complimentary node due to which the node hit by radiation gets enough time to go back to the original state. The main disadvantage with this circuit is that the hysteresis works in both the hold state and write state of the latch degrading the overall performance of the latch. The area, delay and power penalty reported in 65nm are 18%, 96% and 68% respectively, and an improvement of 3X in simulated neutron SER rate with respect to reference DFF. Another improved circuit shown in Figure 3-3 where the storage nodes of the standard latch are each connected to a secondary cross-coupled inverter pair (or 'hysteresis' inverters) with a weaker drive. Here, the hysteresis inverters are gated by the clock and they are active on during the hold mode of the latch. This helps improve the speed and power performance. The average increase in critical charge reported in this structure is around 3X with respect to standard flip-flop and area, power and delay penalty in 28nm node is reported to be 50%, 30% and 70% compared to standard flip-flop. Another circuit (shown in Figure 3-4(a)) called charge steering latch [30] improves the SEU tolerance by providing an alternate low impedance path for excess carriers generated during an ionizing particle strike. Charge steering is achieved using guard transistors. The combined effect of the Q_{coll} decrease at the sensitive node (due to excess carriers being steered away from it) along with the Q_{crit} increase that comes from the additional parasitic capacitances, results in a significant improvement in the SEU performance. The SEU improvement achieved with this circuit is shown in Figure 3-4(b) which shows significant improvement compared to standard DFF and hysteresis based DFF.

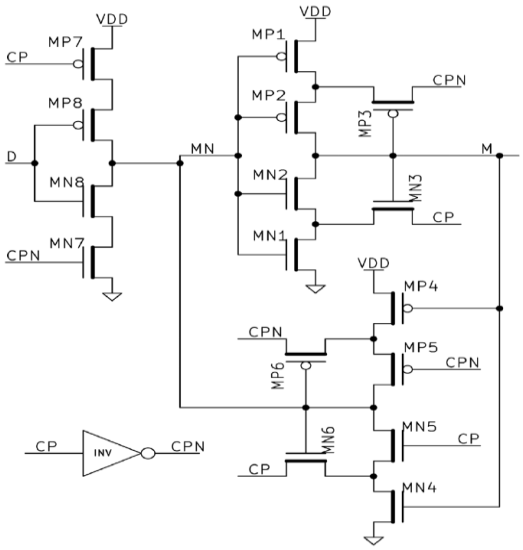


Figure 3-2 Robust Schmitt Trigger Latch Schematic, After [29]

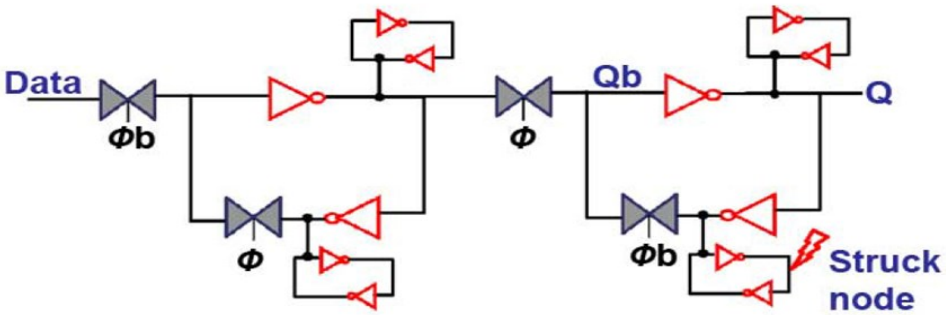


Figure 3-3 Hysteresis Based Flip-flop Circuit, After [28]

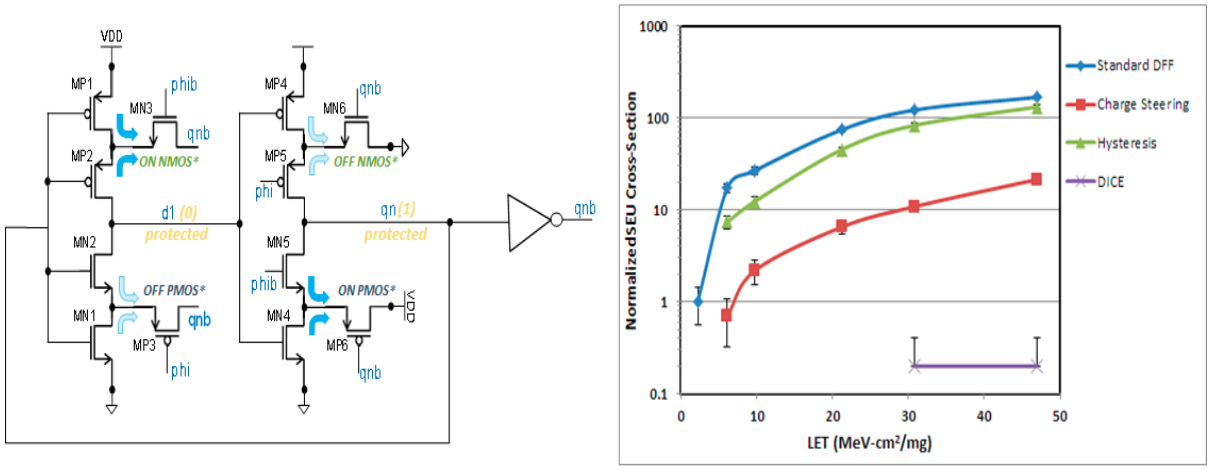


Figure 3-4 (a) Schematic of the charge-steering D-latch, and (b) Normalized heavy-ion SEU cross-section as a function of the LET of the ion for standard DFF, hysteresis DFF, charge-steering and DICE designs for 16-nm FinFET technology, After [30]

3.1.2 Medium Radiation Tolerance

The circuits in this category employ the spatial hardening and temporal hardening concept along with increasing Q_{crit} to achieve radiation hardening. They provide good tolerance against SEUs which leads to a significant drop in FIT rate, but, for higher LET particles which can affect multiple nodes of the circuit, they fail to correct error. Therefore, at lower technology nodes, partial immunity is achieved against high energy particles. Again, the circuits reported require a re-design of cells like circuits reported in earlier section and there is significant impact on area, power and performance as well. In all reported structure minimum 2X area and power impact is reported. Most popular and extensively used structure belonging this category is the dual interlocked storage cell (DICE) [31] shown in Figure 3-5. Interleaving provides dual node feedback to each storage node, meaning that the logic state of each of the four nodes of the cell is controlled by two adjacent nodes that do not directly depend on one another. At least two storage nodes in the latch must be driven by inputs in order for the latch to write properly. A radiation strike causing upset on a single node is largely filtered by such structure.

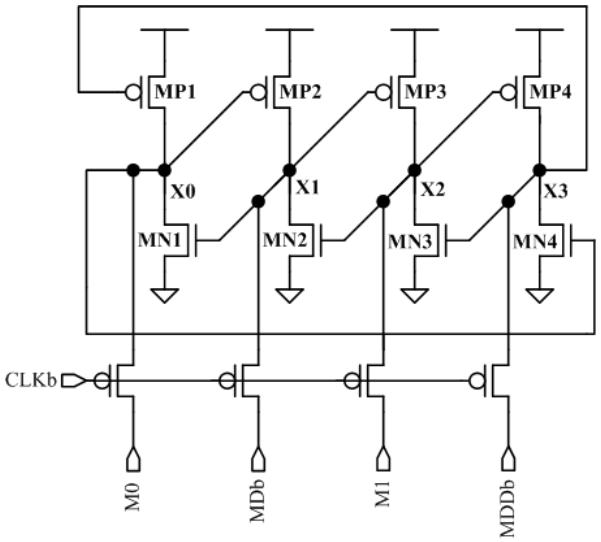


Figure 3-5 DICE latch schematic view, After [31]

Another latch circuit based on spatial redundancy known as QUATRO latch (Figure 3-6) is reported in [32]. It employes Cascode Voltage Switch Logic (CVSL) which can provide better performance than DICE at high LET values. It contains four storage nodes (A, B, C, and D) similar to a DICE latch. The latch is constructed by utilizing two pairs of conventional cross-coupled devices each having its own load. The cross-coupled NMOS transistors have PMOS transistor loads and cross-coupled

PMOS transistors have NMOS transistor loads. Again here two nodes must be written simultaneously to change the state of the latch. A modified quatro cell (Figure 3-6) [33] deploys guard gates on outer transistors which further enhances the robustness of the latch against radiation strike. These circuits are reported to give better tolerance than dice with lesser speed penalty and more area and power penalty.

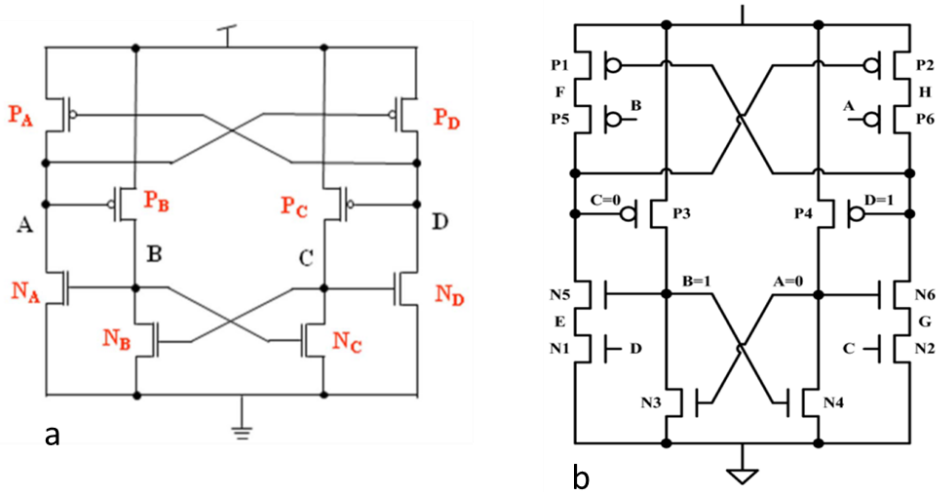


Figure 3-6 (a) QUATRO Latch circuit [32] (b) Modified QUATRO Latch Circuit, After [33]

Another redundancy based hardening technique known as BISER (built-in soft error resilience) [34] involves storing the data simultaneously in two laches as shown in Figure 3-7. The data stored in the two latches is compared using a C-element. In case of a fault in one of the latches the C-element output remains unresolved but week keeper on output node helps in giving the correct value at output. It is reported that the BISER technique helps to achieve more than an order of magnitude improvement in the SER with minimal area impact (since the redundant latch is a scan-reuse latch), and less than 10% power and performance impact.

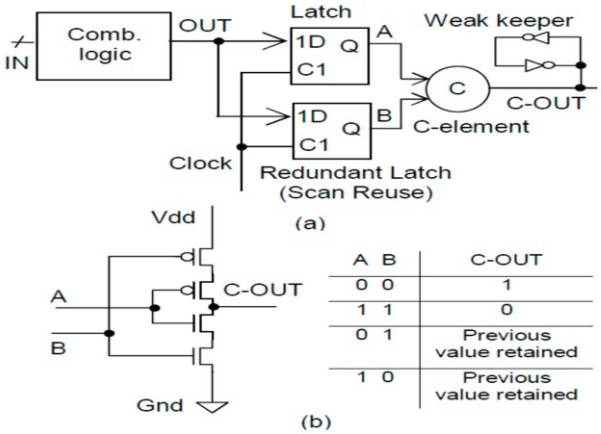


Figure 3-7 (a) BISER based latch hardening design and (b) design of C-element, After [34]

A temporal hardening based latch is shown in Figure 3-8. The temporal latch employs triply redundant feedback nodes that are separated in time (temporally separated) by intentionally differing delays. The temporal redundancy makes a temporal latch tolerant to both SET and SEU effects [24]. The triply redundant feedback paths meet at a single majority gate, so the ultimate value in the latch storage feedback path is determined by a vote of the delayed versions of the stored node. In the event of a strike on the storage node, the charge is removed from the upset node until two of the feedback paths agree. Consequently, the circuit is hard to an SET duration up to the length of one of the delay elements. The same analysis applies to the other nodes in the feedback path, i.e., at the delay chain outputs, as well as for SEU. The key drawbacks in using temporal latches in an RHBD design are their size and the relatively long setup time, which for fully hardened operation is greater than two delays.

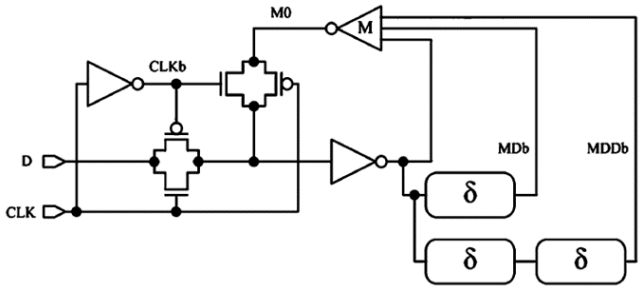


Figure 3-8 Temporal Latch Circuit, After [24]

Such redundancy based techniques are generally not sensitive to single node charge collection and require charge collection at two different off-state nodes to flip the cell. With decreasing feature size and increased packing density leading to increased multi-node charge collection, such redundancy based latch designs are susceptible to an upset. A variant of the DICE latch called LEAP-DICE was shown to help mitigate impact of multimode charge collection in the DICE design [23] [27]. LEAP stands for Layout Design through Error-Aware Transistor Positioning and is a layout principle for soft error resilience of digital circuits. LEAP looks at the circuit response to single event charge collection at each individual node, then places the transistors in such a way that during a particle strike, multiple diffusion nodes can act together to fully or partially cancel the overall effect of the single event on the circuit. This concept can be applied in all circuits discussed above to improve the tolerance towards multiple node upsets. Based on the above principle, the LEAP-DICE (shown in Figure 3-9(a))

design was developed and implemented in a 180 nm CMOS process [23] [27]. Figure 3-9(b) showing cross-section of different structures shows that the LET upset threshold for LEAP-DICE is shown to be about an order of magnitude larger than the lowest LET upset threshold for DICE. In addition, the LEAP-DICE flip-flop has ~5X lower SEU rate on average, compared to the reference DICE flip-flop. LEAP methodology significantly improves the robustness but area penalty is more, and design cost and complexity is huge. Another variant of DICE working on true single phase clock is presented in [35]. The circuit improves the power dissipation due to the usage of single phase clock maintaining the same level of robustness.

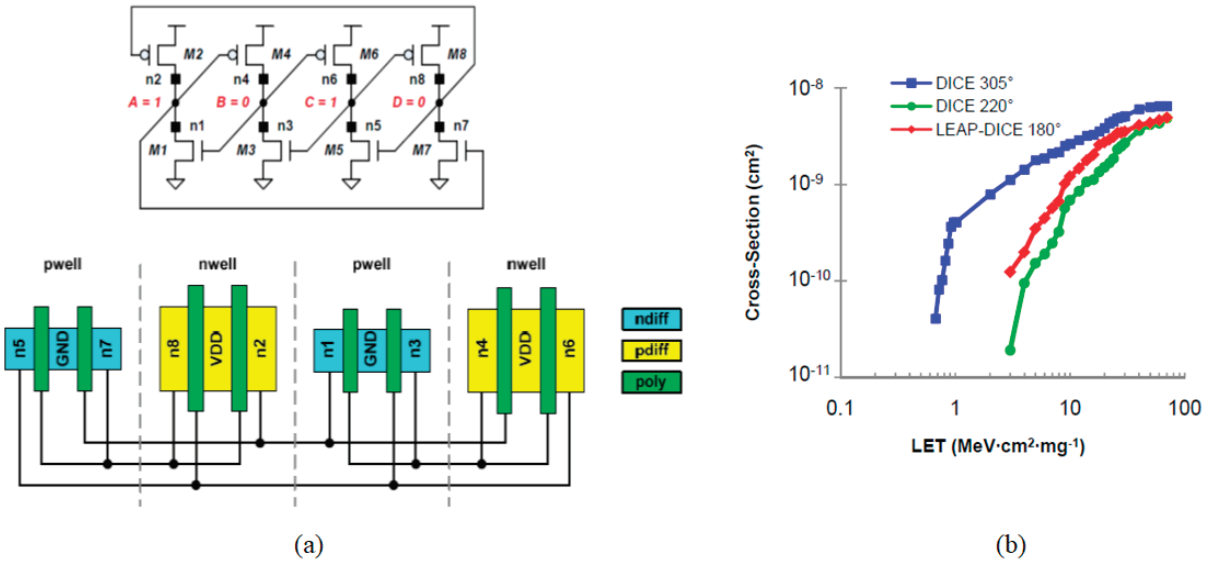


Figure 3-9 (a) DICE latch schematic and the LEAP principle based layout positioning of the transistors, and (b) SEU cross-section of standard DICE and the LEAP-DICE designs as a function of LET for select sensitive directions, After [23]

3.1.3 High Radiation Tolerance

Circuits providing complete immunity to SEU are put in this category. Such circuits are based on Modular redundancy approach along with majority voting. A typical example of Triple module redundancy (TMR) based is shown in Figure 3-10 With enough separation between redundant flip-flops, if one of the flip-flop states gets altered by a radiation strike, the other two vote out the erroneous data, giving a correct value at the output. Such circuits are suitable for harsh radiation conditions or for critical applications requiring extremely low FIT rates. The penalty in area, power and performance is huge with this type of hardening mechanism. Depending on the majority voter design, these designs may or may not require a re-design of the cells. Majority voter designs shown in Figure 3-11 are studied in [36]. The one based on

NAND logical scheme Figure 3-11(a) and mux based scheme Figure 3-11(b) can be implemented with standard logic gated not requiring cell re-designing.

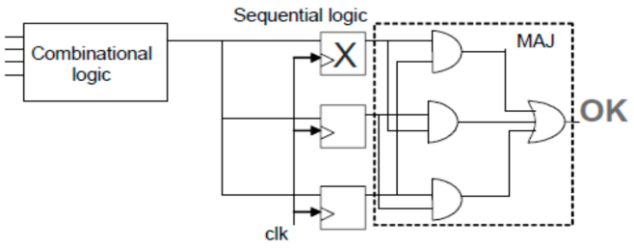


Figure 3-10 Triple modular redundancy (TMR) in the sequential logic (flip-flops) along with a majority voter, After [10]

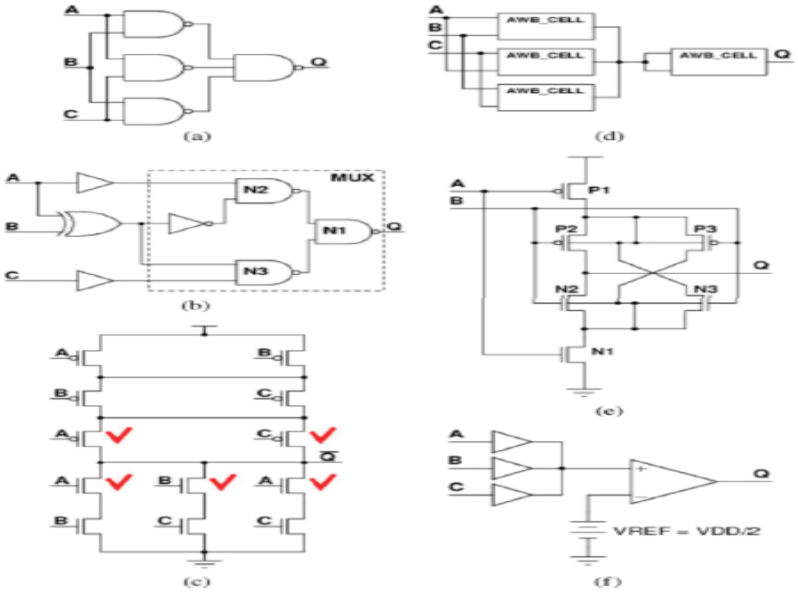


Figure 3-11Majority voter designs investigated in [36]. (a) "NAND" logical scheme; (b) "MUX" logical scheme; (c) "12TI" transistor-level implementation; (d) "AWB" logical scheme; (e) AWB_CELL transistor-level implementation; (f) "ACOMP" logical scheme, After [10]

The TMR flip-flop design is prone to SET faults. Any SET on input combinational logic can be stored in all three redundant flip-flops leading to an erroneous output. Also, an SET on the voter logic of TMR can propagate to the next stage flip-flop. To overcome this, one of the solutions is Full TMR design wherein input combinational logic and voter circuitry is also triplicated along with flip-flops (Figure 3-12). The penalty in all aspects is huge but this methodology gives best SER immunity.

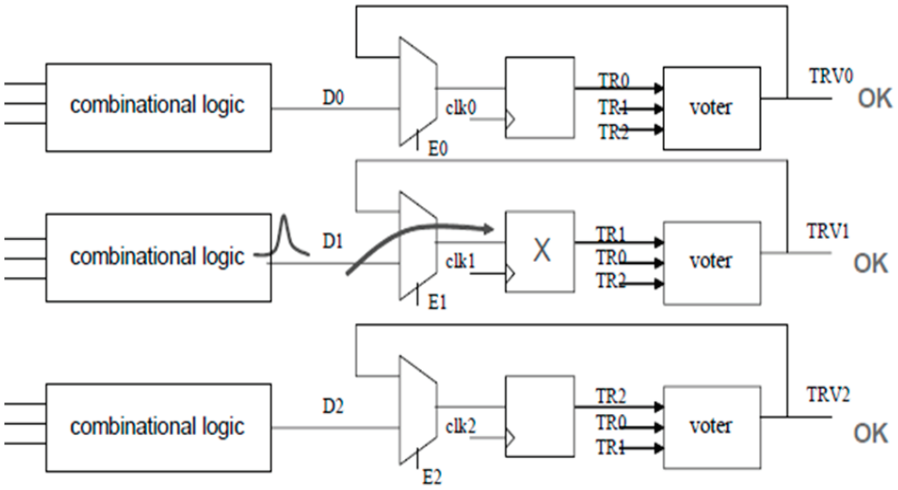


Figure 3-12 Full TMR based design, After [10]

Another methodology based on the combination of temporal hardening and modular redundancy can overcome both SEU and SET faults. A scheme shown in Figure 3-13 shows sampling of the input data coming from combinational logic at three different intervals with skewed clocks. If delay between two clocks is more than the width of the SET pulse, SET pulse could get stored in only one of the three flip-flops. The circuit is called ΔTMR design.

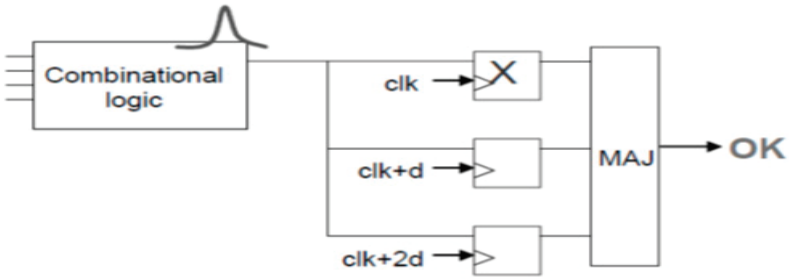


Figure 3-13 Temporal redundancy based combinational logic SET hardening using three copies of latch circuit with delayed clock signals, After [10]

Another scheme showing SET filtering on D inputs of a TMR flip-flop is shown in Figure 3-14(a). The D-SET filter scheme is shown in Figure 3-14(b) which is based on standard delay elements. Here data is delayed and the clock going to the three copies of flip-flops is the same. Again, three different sampling times and majority voting filters out the SET event.

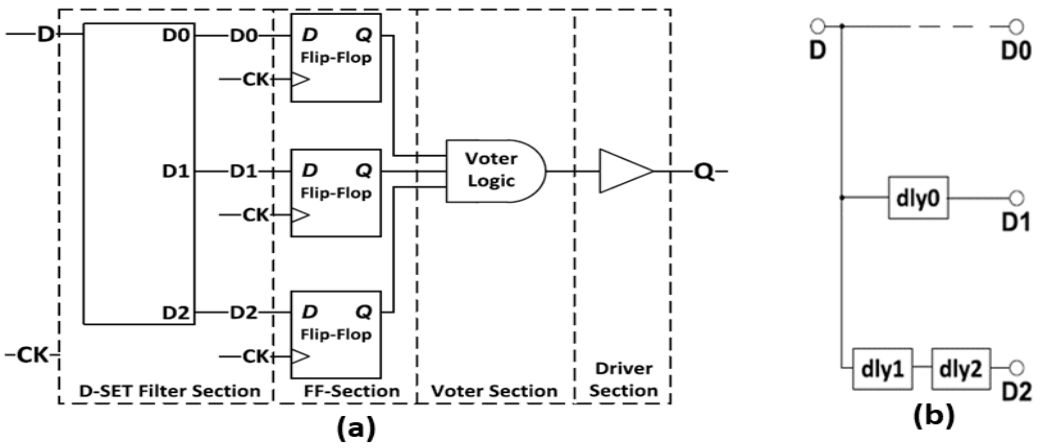


Figure 3-14 (a) ΔTMR flip-flop logic diagram (b) Baseline SET filer Architecture (D1D2), After [37]

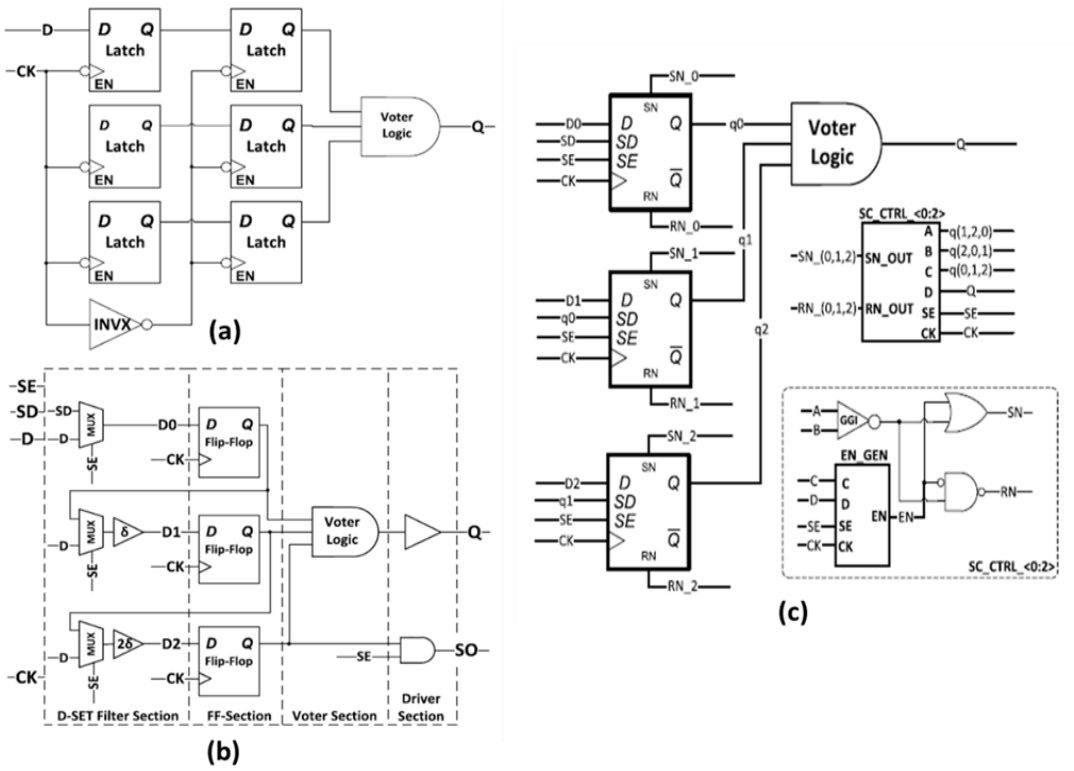


Figure 3-15 (a) Latch Based ΔTMR (L-ΔTMR) without D-SET filter (b) Scannable ΔTMR flip-flop (S-ΔTMR-II) (c) Self-Correcting ΔTMR, After [37]

Different variants of ΔTMR flip-flops are studied in [37]. In Figure 3-15(a), a latch based ΔTMR is shown where no D-SET filter is used, and the delay is managed at the implementation side. A scannable version of ΔTMR is shown in Figure 3-15(b). A self-correcting ΔTMR design is shown in Figure 3-15(c). In low power digital systems clock gating is used extensively to minimize the dynamic power of the system. This low-power feature has a dangerous side effect, if clock-gating is applied to a system

configuration which is exposed to radiation. The induced SEUs would accumulate over time and might lead to a fault in the complete TMR flip-flop, bringing the system to a deadlock in the worst case. Consequently, the use of activated self-correcting registers while the clock is gated is one option to address this issue. Or specific refresh cycle correcting the data of the flip-flop can also be provided in the system on detection of a radiation event. In the circuit shown asynchronous set and reset signals are used to correct the data. Another scheme for self-correcting TMR based on C-element is presented in [38]. Different implementation configuration of abovementioned circuits studied in [37] are shown in Table 3-1. The configurations are based on delay used for SET filtering, physical spacing between different gates of flip-flop and architecture of flip-flop. Comparing with standard flip-flop, huge area impact of 6X-10X is reported along with high power dissipation penalties ranging 4X to 15X and ~2X timing impact. The irradiation results shown in Figure 3-16 show that the modular robust solution provide a high order of magnitude decrease in sensitivity with respect to the reference standard flip-flop. ΔTMR with large spacing and large delta delay (DTMRR05) had no fails even for higher LETs. The standard TMR without SET protection i.e. no D-SET filtering had higher failure rate with increasing LET. With larger spacing and D-SET filter delay complete immunity can be achieved but this comes with a high cost in area, power and timing.

Table 3-1 Design Configurations of different ΔTMR flip-flops studied in, After [37]

Campaign No.	CUT	δ-size [ns]	Min t_{setup} overhead	Min Δ_{seq} [µm]	Min Δ_{sec} [µm]	Norm. A	Norm. t_{pg}	Norm. E	Description
1	DFF_STD	n/a	n/a	n/a	n/a	1.0	1.0	1.0	Standard D-flip-flop
1	DTMR_01	0.18	2δ	15	0.5	11.9	1.7	14.4	ΔTMR with δ, small spacing
2	DTMRR00	–	–	10	10	6.7	1.9	4.6	ΔTMR w/o δ, larger spacing
2	DTMRR05	0.5	2δ	14	10	8.1	1.9	7.4	ΔTMR, larger δ, spacing
2	LDTMRR00	–	–	5	n/a	7.9	1.8	5.5	L-ΔTMR w/o δ
2	LDTMRR05	0.5	2δ	5	n/a	7.9	1.8	8.4	L-ΔTMR with δ
3	DTMRR05N	0.5	2δ	14	10	8.1	1.9	7.4	DTMRR05 + deep N-well
3	SDTMRB05	0.5	2δ	19	9	10.8	2.1	7.9	S-ΔTMR-I with δ, spacing
3	SDTMRN05	0.5	2δ	19	9	10.8	2.0	7.8	SDTMRB05 w/o async. re-/set

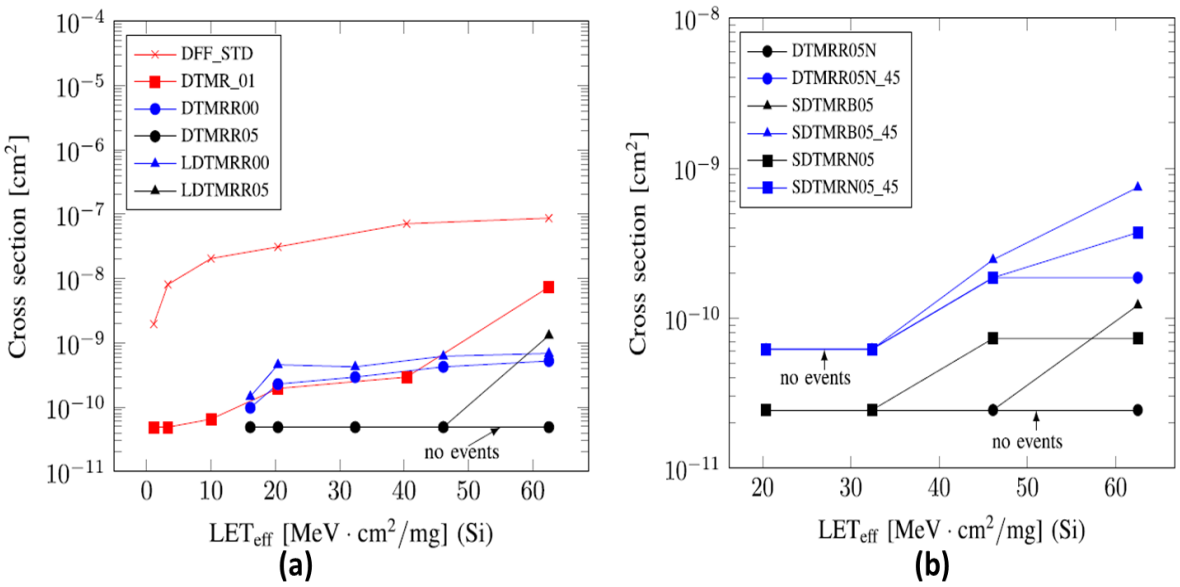


Figure 3-16 Cross-section as a function of effective LET (LET_{eff}) for all irradiated shift registers (a) Experimental results for campaign 1 and 2 (b) Experimental results for campaign 3, untilted and 45degree angled, , After [37]

3.2 Radiation Hardening in memory

A typical memory cell in 6T transistor topology is based on a back-to-back inverter latch with access transistors to read and write the memory cell as shown in Figure 3-17(a). The way an upset occurs is similar to the back-to-back connected inverter latch as explained earlier in section 2.3.1 and scheme of events is also shown in Figure 3-17(b). At bit cell level, similar hardening techniques like increasing the critical charge and spatial redundancy, discussed in earlier section can be applied here to mitigate the errors. The key drawback is that the memory performance degrades significantly, and area penalty is also very high which is not acceptable for memory designs where millions of cells are used for storage purpose. Therefore, for memory circuits a logical error correction technique is used for error detection and correction which has lesser impact on performance, area and power dissipation compared to bit-cell hardening based methods.

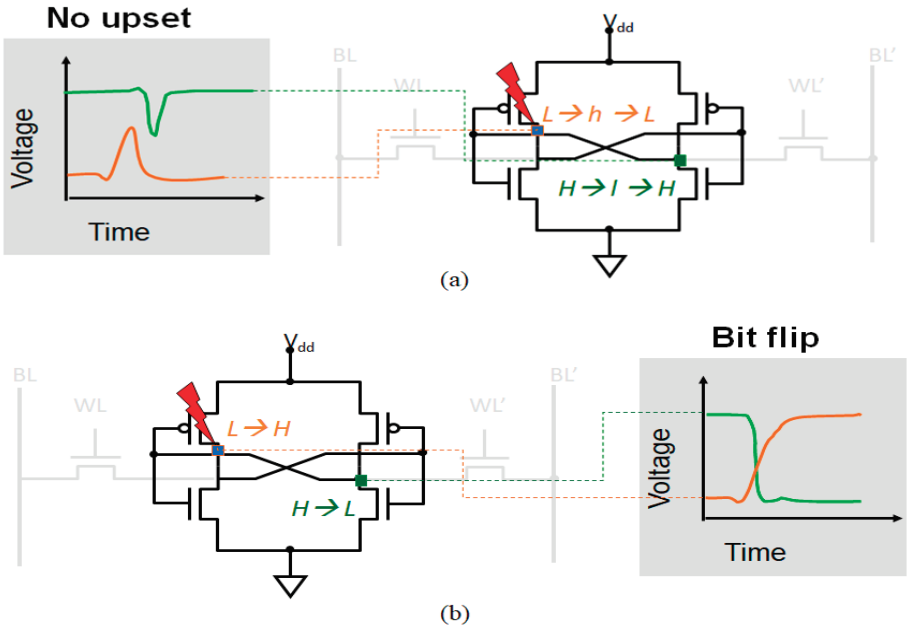


Figure 3-17 Illustration of single-event strike in an SRAM bit-cell. In (a), the transient voltage pulse-width is shorter than the delay between the two inverters in the SRAM cell and hence the bit does not flip. In (b), the transient pulse-width is longer than the loop delay and hence results in the bit being flipped, After [10]

Various logical error detection and corrections (EDAC) [39] schemes are shown in Figure 3-18. The very basic parity bit concept is an error detection mechanism only. The hamming and extended hamming codes can correct up to one error and detect two errors. This is called the single error correction and double error detection (SECDED) scheme. The size of the memory must increase in order to store the

additional parity bits required per memory word. Typically for a 32-bit word size, 7 parity bits are needed for SECDED. The functionality of a memory read and write protected using SECDED is as follows. During write phase, the encoder structure calculates the parity bits and stores it in the memory along with the data, while during read, data and parity bits are read simultaneously, decoder decodes parity bits and data bits. It can correct read data, in case of single bit error, but in case of two bit errors, it flags it as uncorrectable data. The memory array which consists of many bit cells is prone to multiple cell upsets. An appropriate interleaving coupled with SECDED can give good error protection as presented in [40] and also proven in our trials on 90nm (explained later in section 5.6). However, at very low technology nodes, multiple bit upsets can still occur or there could be other reliability issues leading to multiple bit fails. For that multiple bit error correction algorithms like read-solomon codes (Figure 3-18) should be deployed. There are some other error correction algorithms which can detect and correct multi-bit adjacent errors [41]. These are derived from hamming codes only. They will require additional parity bits.

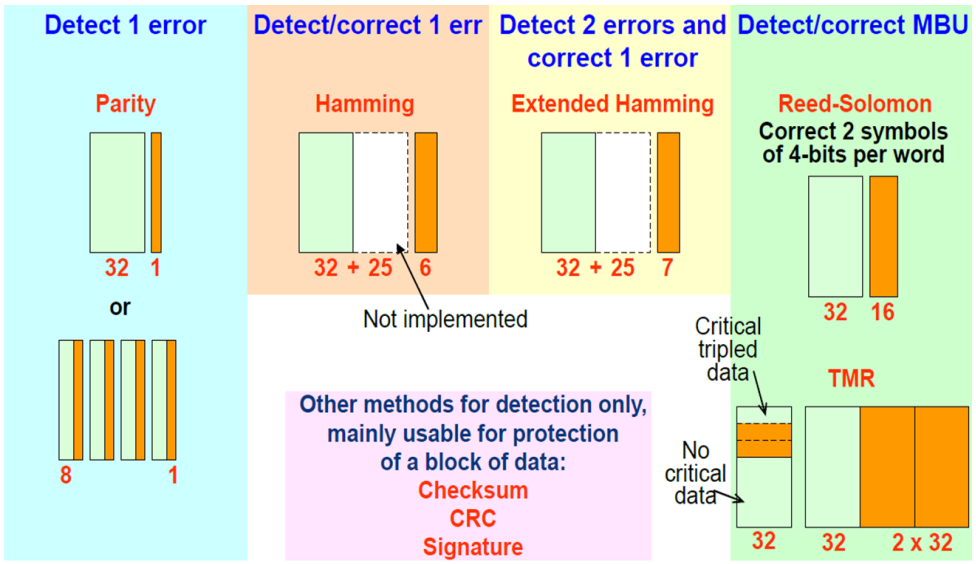


Figure 3-18 EDAC techniques

Another important SEE problem associated with memory cicuits is error accumulation. As the SECDED scheme is able to provide correct output data but it doesn't correct the memory content by writing corrected data back to the memory. Therefore, errors could accumulate in the memory array over time, in case of another strike, multiple bit upsets can occur, which would be uncorrectable. Therefore, it's important to write corrected data back into the memory either at the same time or through a dedicated self-refresh mechanism [10].

3.3 In-situ Timing Monitors

Digital systems are designed with sufficient margins to account for the rising variations at advance process nodes and aging degradation over time. These systems are usually designed for error free operation at desired operating frequency considering the worst manufacturing process scenario, worst operating scenario and device degradation over product lifetime. However, it is very rare that such scenarios would occur during the product lifetime. Therefore, it is very important to understand the environment wherein the product is working, so that the system's operating point can be dynamically adjusted and optimized, to achieve error free operation either at lowest power consumption for a particular speed, or higher performance can be achieved without boosting power supply. This is achieved with the use of embedded timing sensors. This illustration is depicted in [42]. Figure 3-19 shows the margin taken during implementation phase and application of in-situ delay monitors to bring the system to work at optimal operating point (OOP) using voltage regulation.

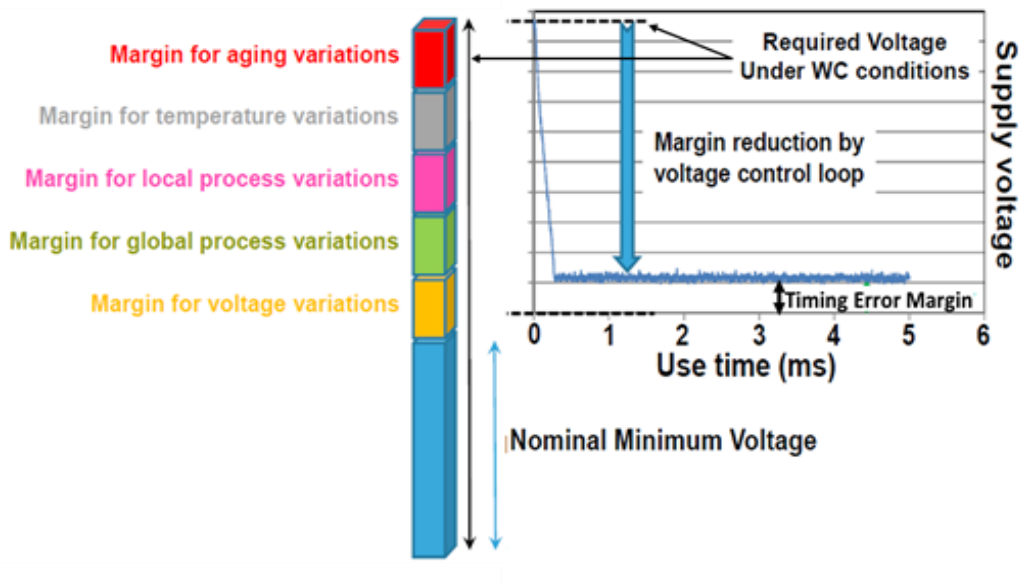


Figure 3-19 Margins for semi-custom designs account for various variations and applications of in-situ delay monitors, After [42]

In-situ delay monitors which can detect timing pre-error condition or post-error conditions are very effective embedded timing sensing solutions over global process, voltage and temperature monitoring solutions. As they are embedded within the digital system close to the actual path and have similar local variations. They provide maximum efficiency gain and better reliability as well [42]. The ones based on timing pre-error detection are called canary structures, a typical example is shown in Figure

3-20, and the one based on timing post-error detection are called razor flip-flops as shown in Figure 3-21. The basic principle is that the incoming data is stored in a main flip-flop and a shadow latch or flip-flop. For canary structures, the shadow flip-flop has more setup time compared to the main flip-flop, so in case of data transitions closer to the clock edge the shadow or canary flip-flop would store an incorrect value. For razor structures, the shadow element is made to have relaxed timing constraint such that in case of failure in the main flip-flop, the shadow element still holds the correct value. Comparing the output of the main flip-flop and the shadow element error condition is detection. In case of no error both should have the same data value stored.

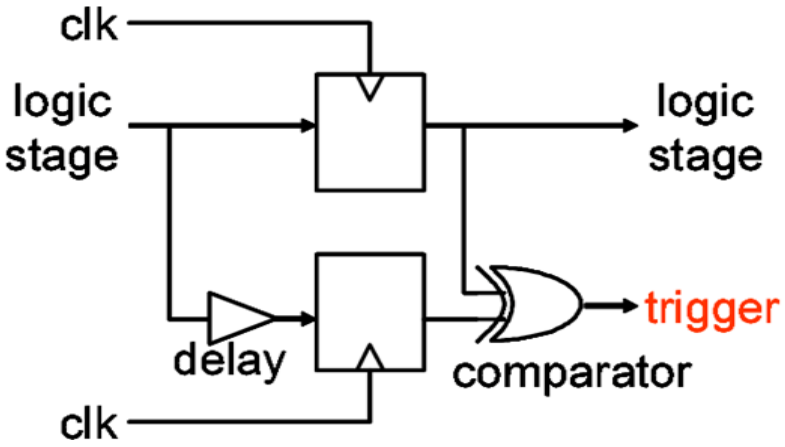


Figure 3-20 Canary Flip-flop Scheme

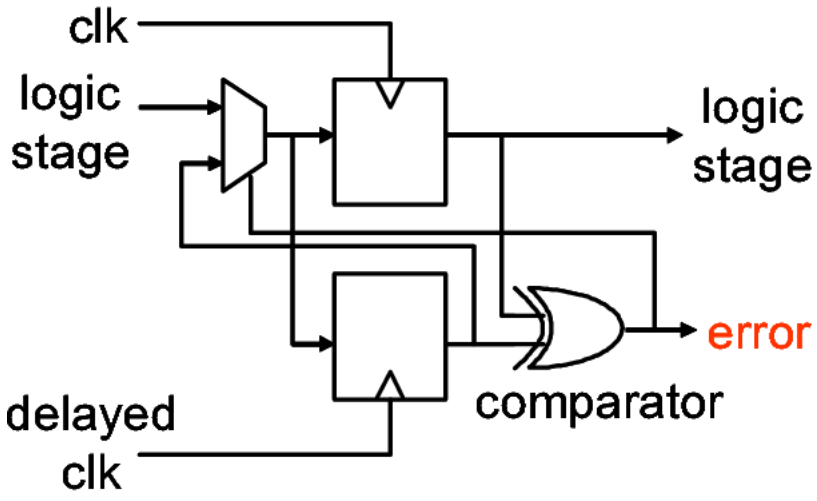


Figure 3-21 Razor Flip-flop Scheme

Razor circuit was first introduced with Razor-1 in [43], an improved version Razor-II was reported in [44], and a low-cost iRazor solution was reported in [45]. Here, the timing fault is allowed to occur in the main flip-flop; after that, advanced error correction and recovery mechanisms such as global clock gating, micro rollbacks,

pipeline flushing, architectural replays, etc., are deployed to restore the system to a normal state. These mechanisms can be very costly, design specific, and do not guarantee complete error recovery in all scenarios, such as higher error rates. All these structures reported implementation of microprocessor based systems using razor flip-flop and they claim to provide minimum 30% power savings with respect to standard flip-flop based implementation. Also, in case performance boost is required instead of energy saving, they reported to give a minimum 30% performance boost. Due to inherent error detection capability, some of such designs also offer detection of soft errors. In razor-II, the SEU effectiveness of the razor-II flip-flop is presented. The errors detected by Razor-II flip-flops are recovered through an architectural replay mechanism that is very specific to microprocessors. It can be suitable for lower robustness applications as it offers no protection against SETs and multi-bit errors. This methodology requires complex error recovery mechanisms such as local micro rollbacks, pipeline flushing, etc., which may or may not recover errors leading to system reset. Moreover, not all types of digital systems can be designed using this methodology as error recovery might not be possible in other digital system.

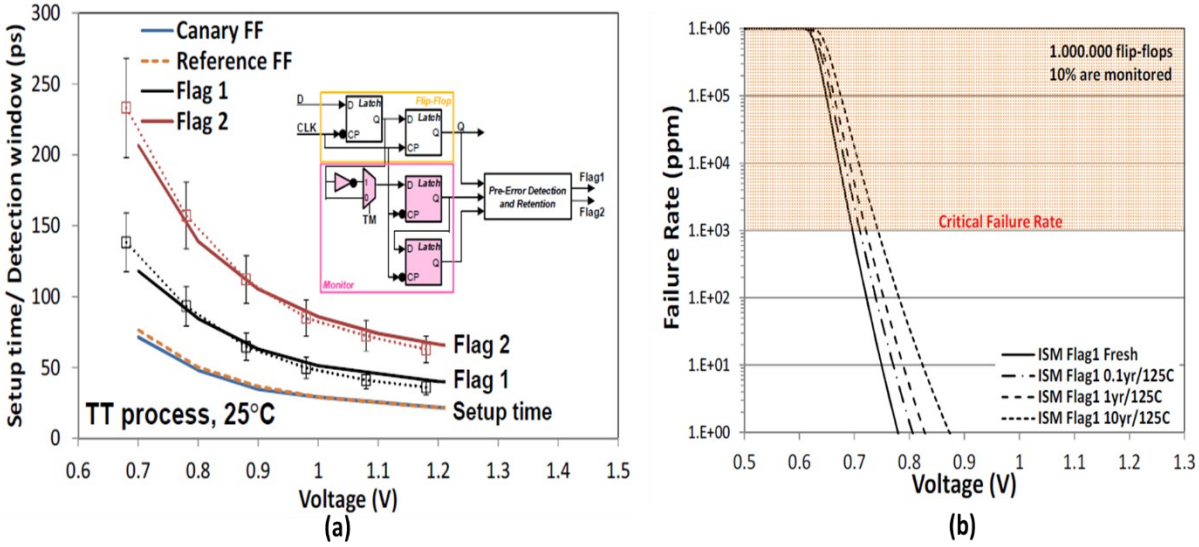


Figure 3-22 (a) In-situ Monitor timing pre-error detection window widoe and setup time of reference flip-flop model vs hardware correlation (b) Failure rate with in-situ monitors, After, [42]

Canary flip-flops based systems always operate at safe distance to actual failing point (Figure 3-22(a)). This results in lesser efficiency with respect to razor but reliability of the system is better. In [42] digital system implementation based on canary flip-flop and experimental results are discussed. They have demonstrated the

effectiveness of the canary structure in enabling digital systems to adapt to optimal operating point at time 0 and with aging (Figure 3-22(b)). The data presented demonstrates a minimum of 20% of power savings. In [46] [47] robustness factor and implementation strategy are discussed. As a summary from [42] [46] [47] [48] [49] it is evident that the canary-based in-situ monitors can be effectively and reliably used to provide prior setup violations, enabling automatic voltage frequency regulation to overcome cost impact, enhance performance, and adapt to device wear-outs.

3.4 Summary

Different RHBD structures have been studied. A summary of the study is reported in Table 3-2. It is evident that with increasing requirement of tolerance there are higher penalties in area, power and speed. The need for efficient tolerant structures is never ending and, in this work, novel solutions have been proposed to address these issues which are explained later in next sections.

Table 3-2 Summary of RHBD flip-flops

Radiation Tolerance	**Type of Circuit**	**Implementation Cost**	**Area, Power and Speed Impact**	**Type of SEE mitigated**
Low	Schimitt inverter based latch, Hysteresis flip-flop, Charge Steering flip-flop	High (New Cell Design)	Low	Mainly SEU
Medium	DICE, QUATRO, BISER, LEAP-DICE, Temporal flip-flop	High (New Cell Design)	Medium	Mainly SEU (SET partially only few circuits reported)
High	Modular flip-flop TMR, ΔTMR, L-ΔTMR, S-ΔTMR, Self-Correcting ΔTMR	Low (Implemented with Standard Library cells)	High	TMR – SEU Rest - SEU and SET both

For Memory circuits SECDED correction coupled higher bit interleaving is found to be suitable for fault tolerance. This is used as is in this work.

Review of in-situ delay monitors provides an opportunity to reduce the penalties due to redundant structures. This is exploited in this work to overcome power and performance impact without any increase in area penalty for high radiation tolerance circuits.

Chapter 4. Proposed Design Solutions

From the previous discussion it is evident that there is a continuous need of decreasing the cost factor in terms of silicon area, power dissipation, timing penalty and development cost along with increase in overall design robustness. There is always a scope of more innovation this area. In the proposed solutions, power efficiency, adaptability and overall robustness has been targeted primarily. One of the solutions is targeted for medium radiation tolerance based and another for high radiation tolerance with embedded timing pre-error detection capability for adaptability. While former would require dedicated cell design the later can be used to make any digital design hardened using standard library cells. The later also addresses the overall design robustness from other prevalent degradation issues like device aging, TID etc. In this chapter detailed design, functionality, working and CAD simulation data is discussed.

4.1 Single Phase Clocked C-Element Flip-flop (SPCRC2-DFF)

This design is targeted for medium radiation tolerance similar to the DICE latch, and QUATTRO latch as explained earlier in 3.1.2. The proposed circuit is based on single phase clocking which helps in improving the tolerance to a radiation strike and reducing the power consumption by the flip-flop. A standard dual phase and single-phase clocked latch is shown in Figure 4-1. The dual phase clocked latch has internal pair of inverters within the latch circuit generating two phases of the clock whereas single phase clocked latch does not need such inverters and it can be directly fed with the clock from the clock tree network. With no inverters present within the latch circuit the single-phase latch has less toggling power compared to the dual phase clocked latch for medium to low data switching rate. For very high data switching (~50% of clock rate) power consumption of the two are comparable [50] [51].

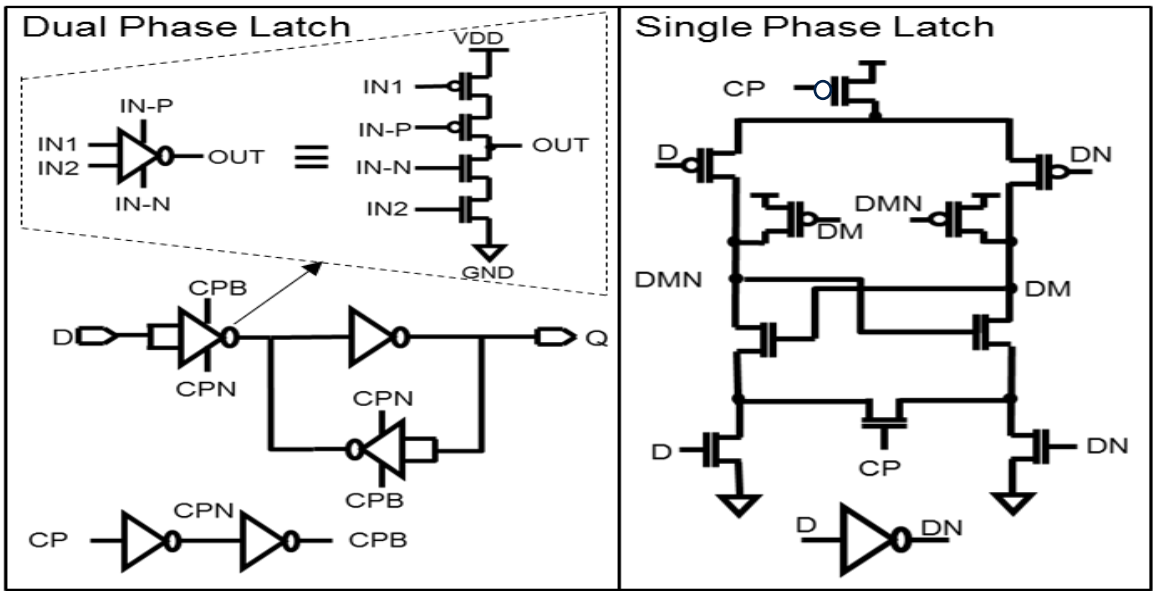


Figure 4-1 Dual Phase Clocked Latch and Single-Phase Clocked Latch, After [50]

In Figure 4-2 sensitive clock nodes with respect to two flip-flop types is shown. In case of dual phase clock flip-flop sensitive nodes 2 and 3 are the internal clock nodes of the flip-flop which are low capacitance nodes and have lower critical charge. The master -clock node 1 is driving many flip-flops and has high critical charge. In case of a single-phase clocked system the sensitive node 4, 5 and 6 all are same as there is no internal inverter or buffer. The critical charge is higher in this case. Therefore, dual phase systems show less tolerance to a radiation strike compared to single phase clocked systems. This is also illustrated in [52] wherein single-phase clock DICE latch

is presented and in [51] where a single-phase robust flip-flop is presented. The radiation results presented showed improved tolerance for single phase clocked flip-flop. A summary of the comparison between the two class of latches is shown in Table 4-1.

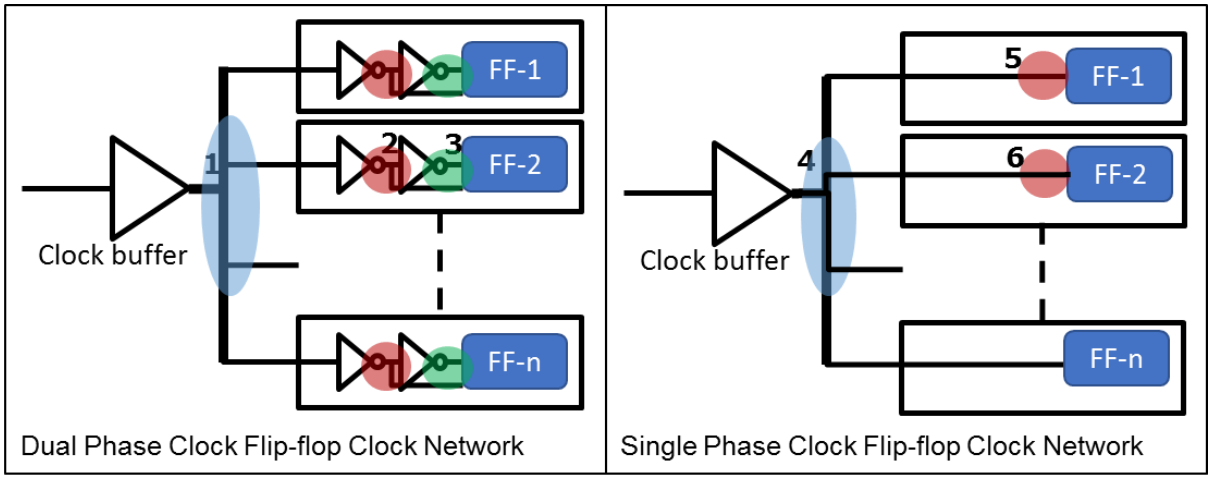


Figure 4-2 Sensitive Clock Nodes from Clock Tree to flip-flop

Table 4-1Dual Phase Latch v/s Single Phase Latch

Parameter	Dual Phase Latch	Single Phase Latch
Functionality	Inverted and buffered both clocks are used for sampling input data	Only one clock phase is used for sampling input Data
Power	Continuous power dissipation on clock inverters due to clock toggling irrespective of data switching activity	Dynamic power dissipation occurs on data change. With clock toggling, power dissipation is less.
Impact on Clock tree	Input clock capacitance is low, therefore less cells are used for clock balancing	Input clock capacitance is high. More cells are needed for clock balancing.
Radiation Robustness	Internal clock nets being low on capacitance are sensitive to radiation strike induced state change.	Clock net capacitance is high, therefore more immune to radiation strike.

Clock Slope Sensitivity	The latch is immune to clock tree network rise and fall transition time.	The latch is sensitive to clock signal transition time.

The advantages of single-phase clocked latch over dual phase clocked latch provided enough motivation to proceed with the design of a robust flip-flop circuit working on single phase clock only. The details on the proposed flip-flop circuit are mentioned below.

4.1.1 SPCRC2-DFF Design and Functionality

The proposed flip-flop circuit is based on differential latches which operate on true single-phase clock. The circuit provides tolerance to both SET and SEU. It comprises of an input stage, master latch, slave latch and output stage as shown in Figure 4-3.

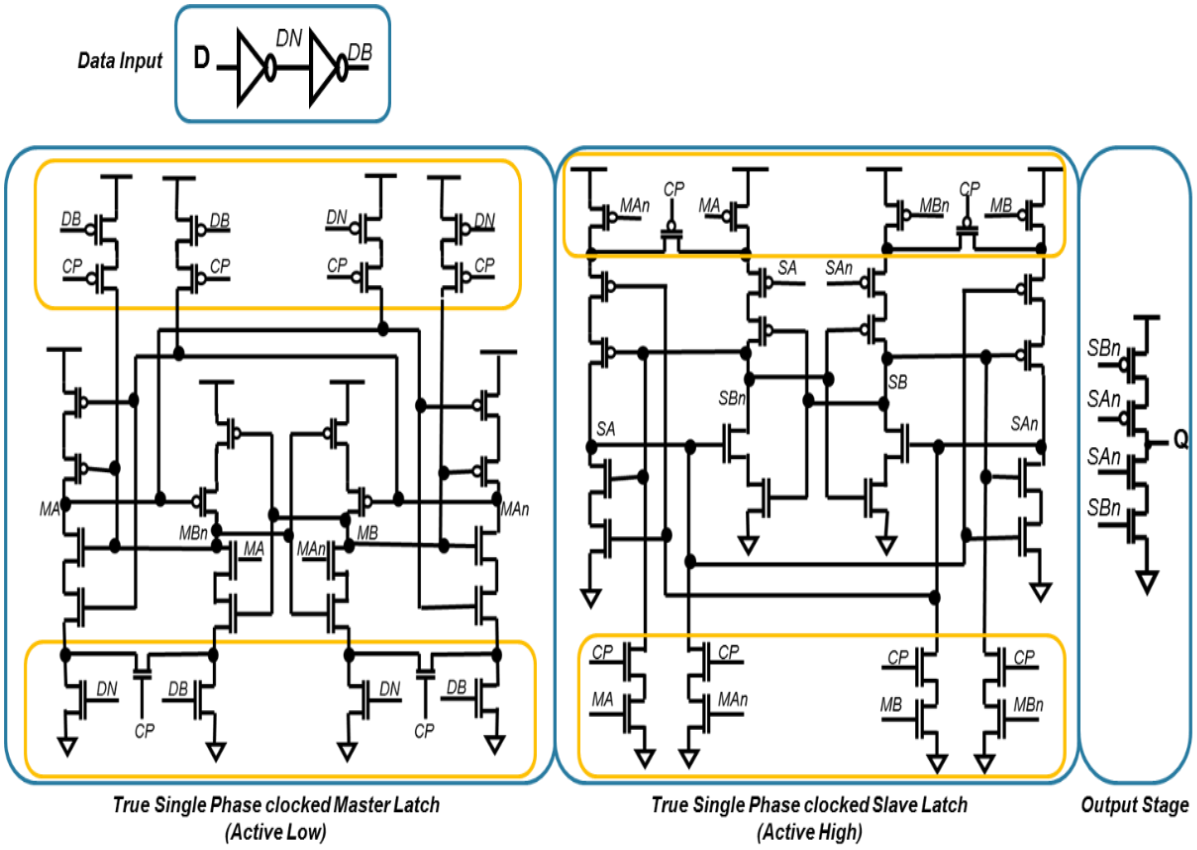


Figure 4-3 . Single Phase Clocked C-Element Based D Flip-flop (SPCRC2-DFF) Circuit Schematic

Input Stage: The input stage comprises of inverter stages generating differential inputs for master latch. The delay of the inverter stages should be chosen based on the glitch width required to be filtered arising from an SET fault.

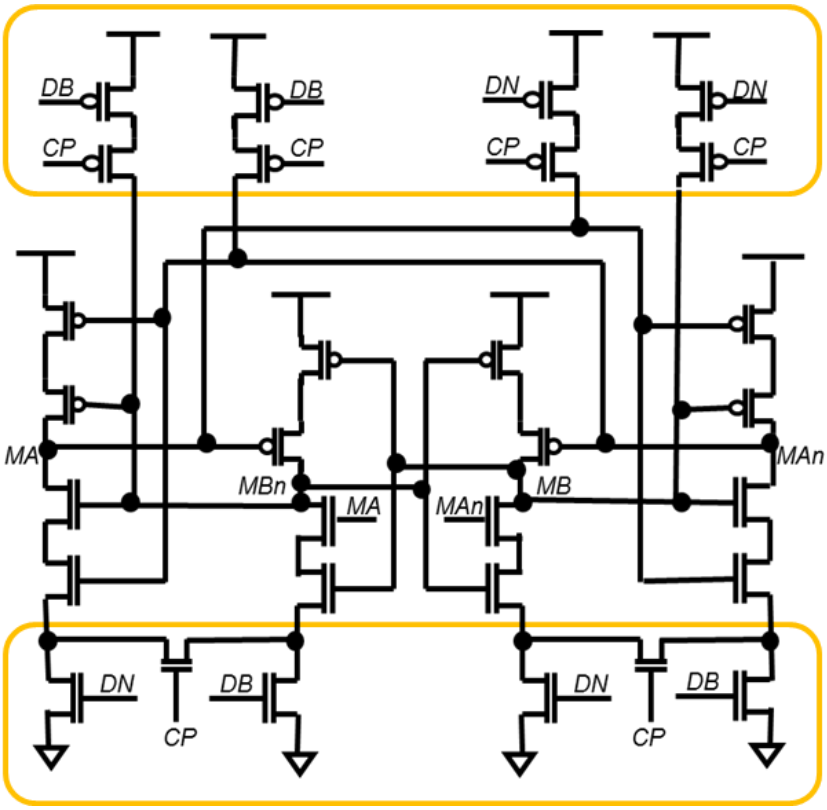


Figure 4-4 Single Phase Clocked Master Latch (Active Low)

Master Latch: The master latch (shown in Figure 4-4) takes the input differential data and passes it to internal storage nodes MA, MB, MAn and MBn when clock CP is low. In this case, the PMOS connected to CP turns ON enabling paths to internal storage nodes MA, MB, MAn, MBn and the clocked equalization NMOS turns off so that only one path to ground is active. For D=DB=1, DN=0, from the supply side, PMOS connected to DN turns on, charging nodes MA and MB. At the same time NMOS connected to D and DB turns on providing a path to GND for nodes MAn, MBn to discharge. And eventually MA=MB=1, MAn=MBn=0. Similarly, for D=DB=0. DN=1, MAn and MBn charges to 1, MA and MB discharges to 0. When Clock CP is high, the PMOS connected to CP turns off blocking any impact of data signals on internal storage nodes and the clocked equalization NMOS turns on to provide a path to ground to all nodes irrespective of data input signals. The internal storing nodes M* resolve to a stable value only when data on all D* are stable. In case of glitch due to an SET on any of these input nodes, the storing nodes do not resolve to stable value and once the event is passed the states gets resolved. When clock is high, i.e. the latch mode, each storing node data is dependent on two states of other nodes. In case

of a radiation event on any one of the nodes, the latch state doesn't change and eventually gets resolved to its previous value when the event has passed.

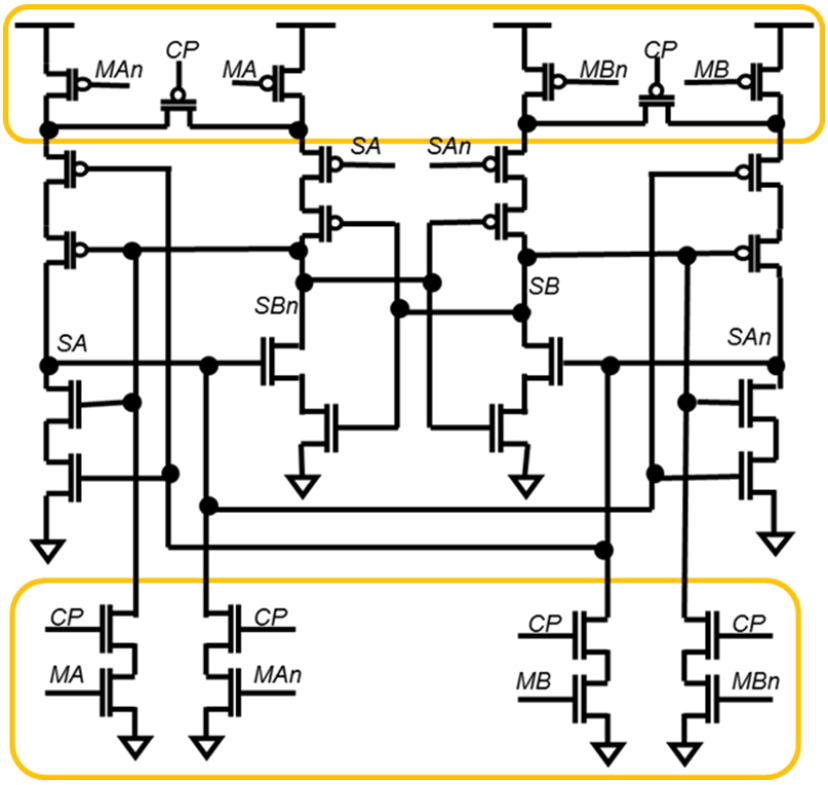


Figure 4-5 Single Phase Clocked Slave Latch (Active High)

Slave Latch: Differential data from the master latch is passed to the slave latch (shown in Figure 4-5) through NMOS gates controlled with clock CP and differential inputs MA, MB, MAn and MBn. The data is stored in internal nodes SA, SB, SAn and SBn. The slave latch operates in a similar manner as the master latch except that it becomes transparent when clock is high and latches the data when the clock is low. In transparent mode, any glitch on MA, MB, MAn and MBn doesn't get passed to the output as the internal nodes SA, SB, SAn and SBn do not resolve to a stable value; in latch mode, any radiation strike on one of the storing nodes doesn't alter the stored data due to dual dependency on two different nodes.

Output Stage: The final output stage is based on C-element wherein the final output of the flip-flop is dependent on two internal slave nodes. Any event on one of the nodes doesn't affect the output.

Functional Waveforms of the flip-flop circuit are shown in Figure 4-6 which could help to understand the abovementioned functionality in a better way.

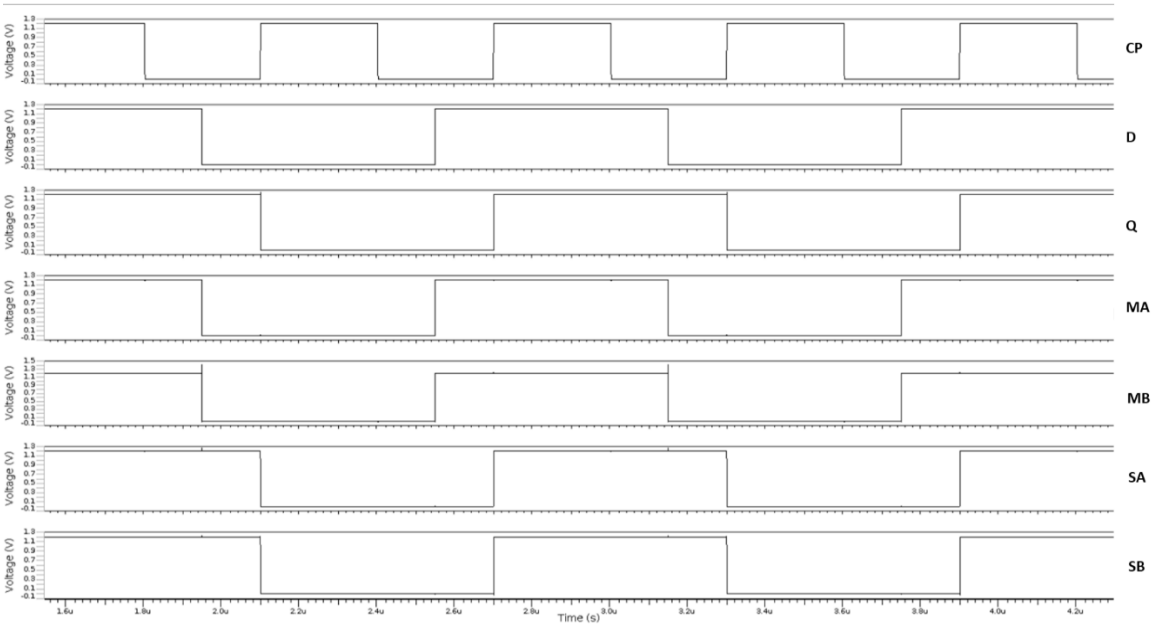


Figure 4-6 Waveforms Showing Normal Functionality of SPCRC2-DFF

4.1.2 SPCRC2-DFF Physical Implementation

The flip-flop is implemented in 90nm ST BCD technology with CMOS HVT devices. The layout is implemented in traditional style with 2.5um separation between the critical node pairs (MA, MB), (MAn, MBn), (SA, SB) and (SAn, SBn) in order to avoid multiple bit upset scenario. Still, the circuit is not completely immune to charge sharing and multi-node upsets, and in order to achieve better immunity advance layout methods like LEAP [23] [53] deploying multi-bit flip-flop layout as single cell and interleaving the critical nodes across different bits should be used. In this work the layout used is traditional one as shown in Figure 4-7 due to complexity of LEAP layout implementation and limited layout resources.

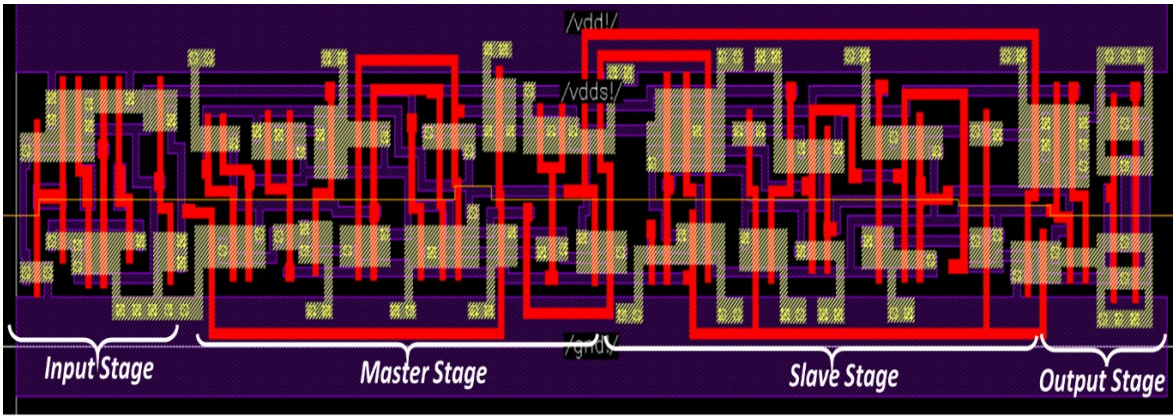


Figure 4-7 SPCRC2-DFF Layout View

4.1.3 Radiation Tolerance with SPCRC2-DFF

The flip-flop is designed to have interdependeny of sensitive nodes on one another. When the latch is in non-transparent mode i.e. storing the data value, each sensitive node value is dependent on two other nodes. In Figure 4-8 MA, MB, MAn and MBn are shown to be the sensitive nodes for the Master latch. Similarly SA, SB, SAn and SBn are the sensitive nodes for the Slave latch. Table 4-2 shows the interdependency of the sensitive nodes.

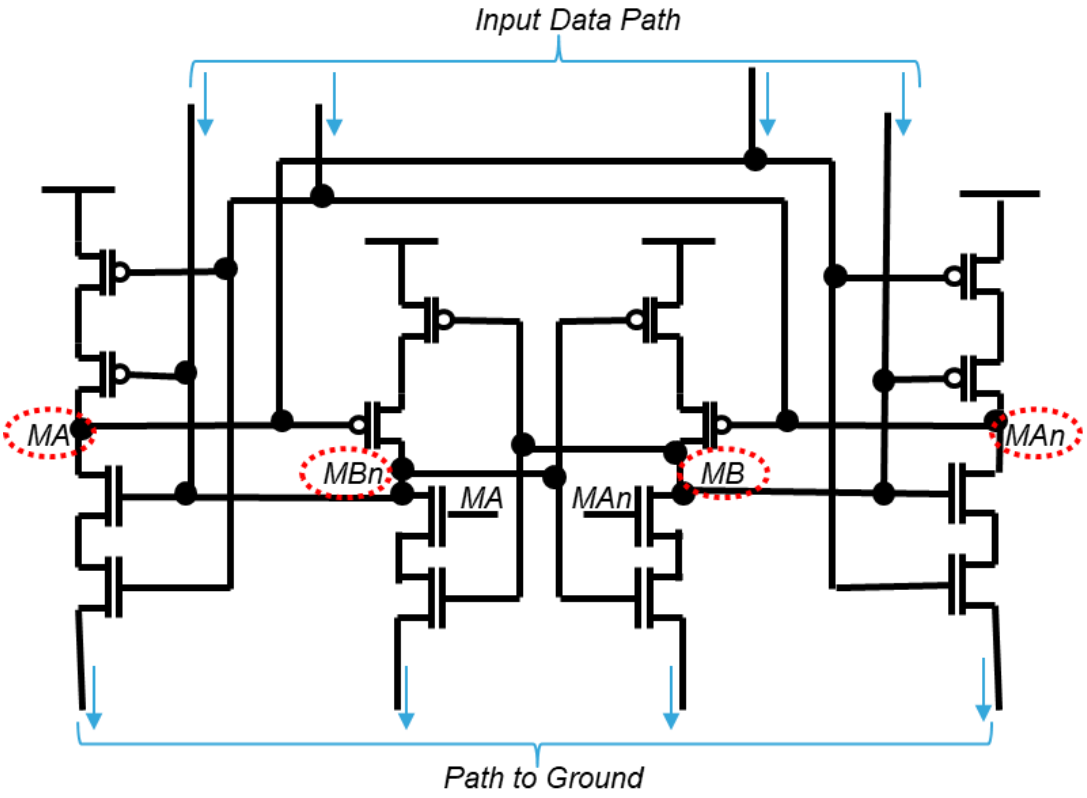


Figure 4-8 Master Latch Sensitive Nodes

Table 4-2 Showing dependency of sensitive nodes for Master and Slave Latch in non-transparent mode

Master Latch		Slave Latch	
Nodes	**Dependency**	**Nodes**	**Dependency**
MA	MAn, MBn	SA	SAn, SBn
MB	MAn, MBn	SB	SAn, SBn
MAn	MA, MB	SAn	SA, SB
MBn	MA, MB	SBn	SA, SB

In case of an SEU when a particle strike one of the sensitive nodes, this interdependency on two nodes prevents change of the stored value and the latch soon recovers to the good value. An SEU event on the master node MA is shown in Figure 4-9 and on the Slave latch node SA in Figure 4-10. The C-element output driver prevents any transition on the primary output of the flip-flop due to an upset on the internal nodes of the slave latch. It is to be noted that the sensitive node on which the particle has hit, changes its value momentarily till the strike effect ends and later on it recovers back to the old value due to its dependency on other two nodes. Similar behaviour is observed for all sensitive nodes. Hence, the immune response against SEU is very good. However, in case of charge sharing and upset of multiple nodes the circuit could get corrupted with the wrong value. Such cases can be avoided using improved layout methodology like LEAP as explained in 4.1.2. The circuit also offers partial protection against SET on the D input of the flip-flop as the master latch samples the differential input data. Increasing the delay between the differential inputs would prevent higher SET pulse to be filtered but this would degrade the setup time of the flip-flop.

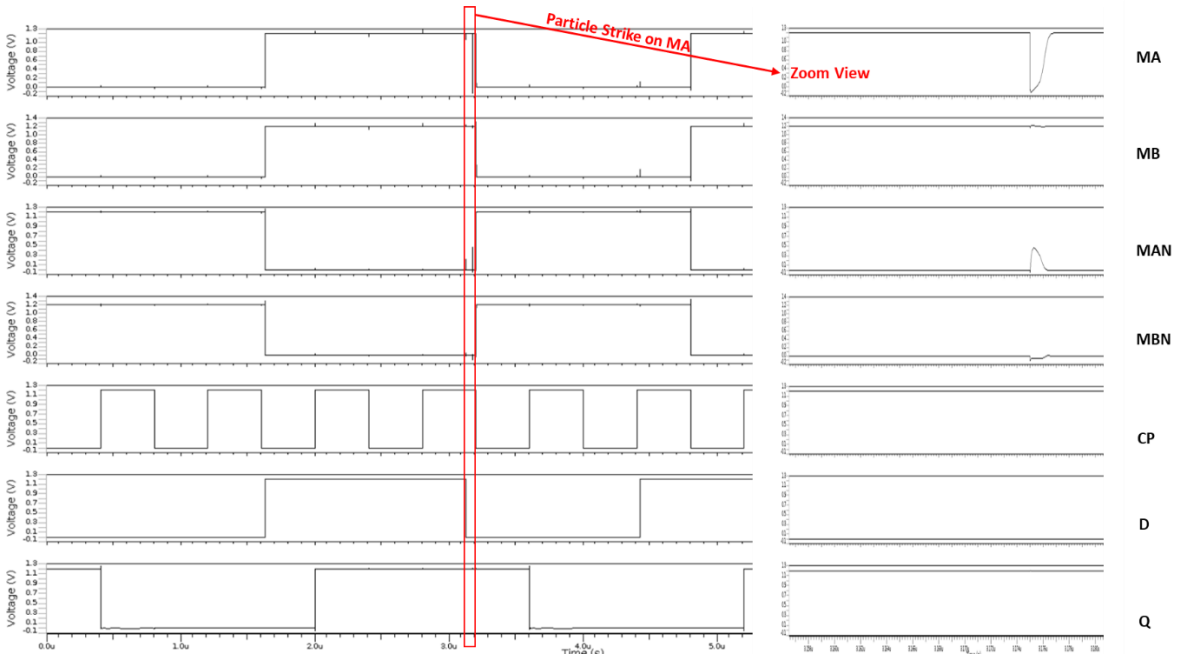


Figure 4-9 Waveforms showing Particle Strike on Master Latch Node MA and its impact on other nodes.

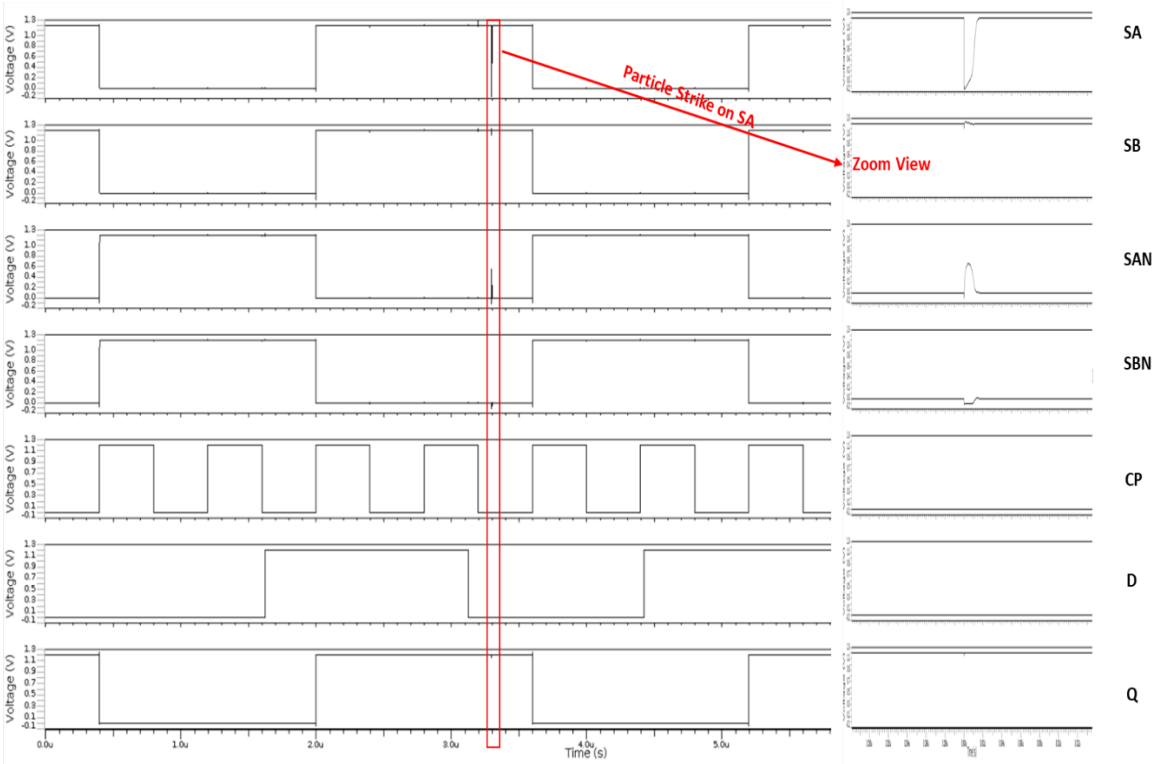


Figure 4-10 Waveforms showing Particle Strike on Slave Latch Node SA and its impact on other nodes.

4.1.4 SPCRC2-DFF Comparative Analysis based on Simulations

The circuit is implemented in 90nm ST BCD technology and comparative analysis is performed with standard flip-flop solutions used at ST i.e. standard flip-flop DPC-DFF (Figure 4-11), DICE based flip-flop DPCR-DFF (Figure 4-12) and TMR solution (Figure 2-15). The TMR-FF is implemented with standard library cells wherein standard DPC-DFF is triplicated, and voter circuits is implemented using AND-OR gates. The spice simulations were carried out using the Eldo tool from Siemens on the post layout parasitic extracted netlist of standalone flip-flops. The simulations are carried out to extract various parameters of the flip-flop on standalone basis. The flip-flop inputs are fed through ideal sources and a nominal cap load is connected to output. The simulations are done at typical process, 1.2V, and 25°C, and results are normalized to reference flip-flop DPC-DFF. The results are shown in Table 4-3 and Table 4-4.

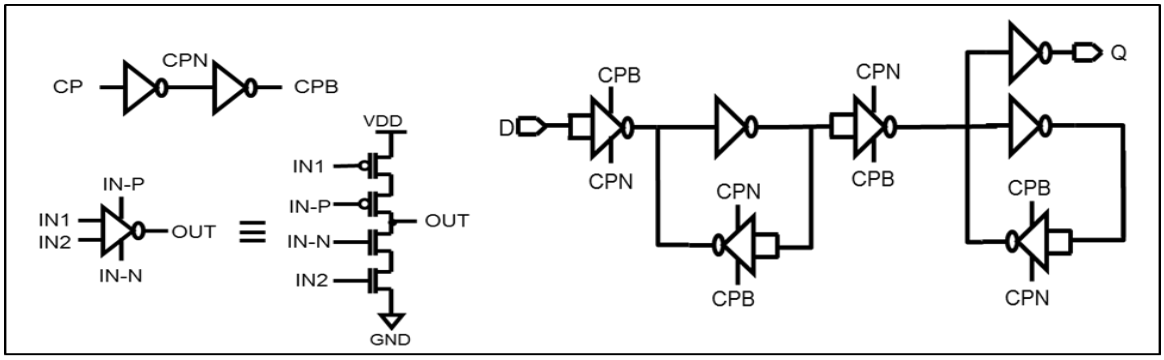


Figure 4-11Dual Phase Clocked D Flip-Flop (DPC-DFF) Schematic View

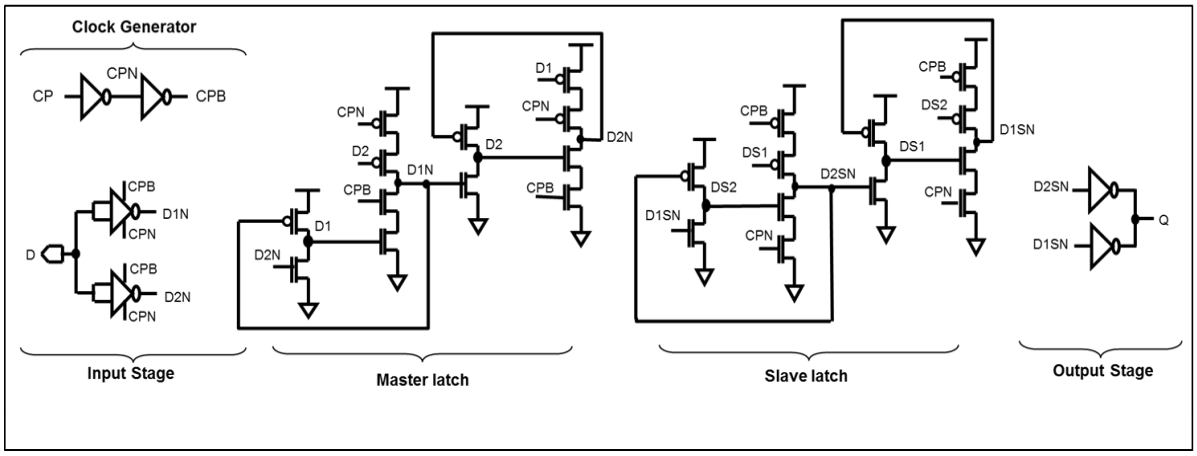


Figure 4-12 Dual Phase Clocked RadHard D Flip-Flop (DPCR-DFF) Schematic View

Table 4-3 Comparative Analysis of Different flip-flops for Performance Parameters

DFF ->	DPC	DPCR	SPCRC2	TMR
CLK CAP	1	5.56	5.76	3.01
CP-Q Rise Delay	1	1.10	1.38	1.82
CP-Q Fall Delay	1	1.98	0.80	1.93
Setup Time Rise	1	1.92	4.54	1
Setup Time Fall	1	1.48	3.87	1
Area	1	2.6	3.3	3.9

Table 4-4 Power Consumption of different flip-flops

Dynamic Power	Only Clock Toggling	12.5% Data Switching	25% Data Switching	50% Data Switching
DPCR-DF	2.12	2.38	2.50	2.64
SPCRC2-DFF	0.17	1.30	1.96	2.71
TMR DFF	3.1	4.23	5.04	5.79
DPC-DFF	1	1	1	1

It is observed that robust solutions have a significant impact on area, power and performance with respect to standard DPC-DFF and this is on the expected lines. The proposed SPCRC2-DFF is 3.3X in area compared to DPC-DFF. It has ~15% impact on average delay (average of rise and fall delay), and ~4X impact on the setup time compared to DPC-DFF. The impact in delay is due to the differential input based design wherein more time is required for the data to be stable before the clock edge. On these parameters the DICE solution DPCD-DFF is better compared to SPCRC2-DFF as the penalty in performance and area is lesser. In terms of power dissipation, power dissipation of different flip-flops for different data toggling rate is shown in Table 4-4. Up to 25% switching rate which is the typical maximum data switching rate of flip-flop used in digital design, the SPCRC2-DFF has much lower power consumption than DPCR-DFF and TMR-DFF. This is mainly due to single phase clocking. Overall, the proposed circuit lags in performance with increase in setup time requirement but gains in power consumption. These standalone flip-flop simulation results don't include the impact on clock tree as the input clock capacitance of flip-flops would directly govern number of clock tree cells required and switching power. Therefore, comparison at system level is also needed for complete analysis, which is shown later in Chapter 5.

Radiation effect on flip-flops is estimated through SPICE simulations using the bias dependent current pulse model given in [17]. The off devices are recognized under different input configurations of CP, D and Q and nodes connected to them are identified. Afterward, a current pulse is applied on these nodes imitating the radiation strike. Using this methodology, the critical charge of various nodes in flip-flops with a strike affecting a single node is measured. The results are shown in Figure 4-13. The TMR flip-flop was excluded from the study due to inherent robustness of the architecture. The DPC-DFF showed maximum failures and lower critical charge values. The master and slave nodes storing charge were found to be sensitive along with the clock nets. However, in robust flip-flops no failures were found with a single strike on data storing nodes. In the DPCR-DFF some failures were observed due to a strike at the clock nodes with higher critical charge whereas in SPCRC2-DFF no failures were observed. Further analysis has been performed with specific Monte-Carlo based current injection simulation environment. Here, the strike at multiple nodes is simulated to study the impact of radiation particles having higher LET which can affect a larger area. For the simulations, the rise time was fixed at 10ps and the peak current and fall time are varied within a range of 2mA to 5mA and 100ps to 1ns

respectively through Monte-Carlo runs. The pulse is introduced on a single node or multiple nodes in the simulation either as a source or a sink depending on the logic state of the node. 1000 Monte-Carlo iterations were performed for each structure for all combinations of CP, D and Q, and flip-flop output was observed for failures. The nodes were selected in the similar manner as explained above considering the off devices in each input configuration. Simulations are performed with following scenarios

(1) single node being affected in first run,

(2) multiple active regions falling within 0.5um of radius,

(3) within 1um radius

(4) within 2um radius.

Beyond 2um, many nodes of the circuit were failing. The results are compiled in Table 4-5. The results are highly dependent on how the layout is done and how critical nodes are placed within the layout as illustrated in [23] [53]. As a rule of thumb, a 2.5um distance between all critical storage nodes is kept during layout implementation of robust flip-flops. The DPC-DFF shows a maximum number of failures and TMR-DFF has no failure due to inherent architecture (flip-flops are placed at least 5um apart [54] [55]). The SPCRC2-DFF shows good immunity till 2um whereas DPCR-DFF lags due to clock inverters and DICE latch failing after a certain distance. The TMR-FF didn’t show any fails at the final output due to voting mechanism. The voter circuit is however prone to SET and did show glitches at output which could be latched by subsequent flip-flop stages in digital system but on standalone simulations it showed no impact.

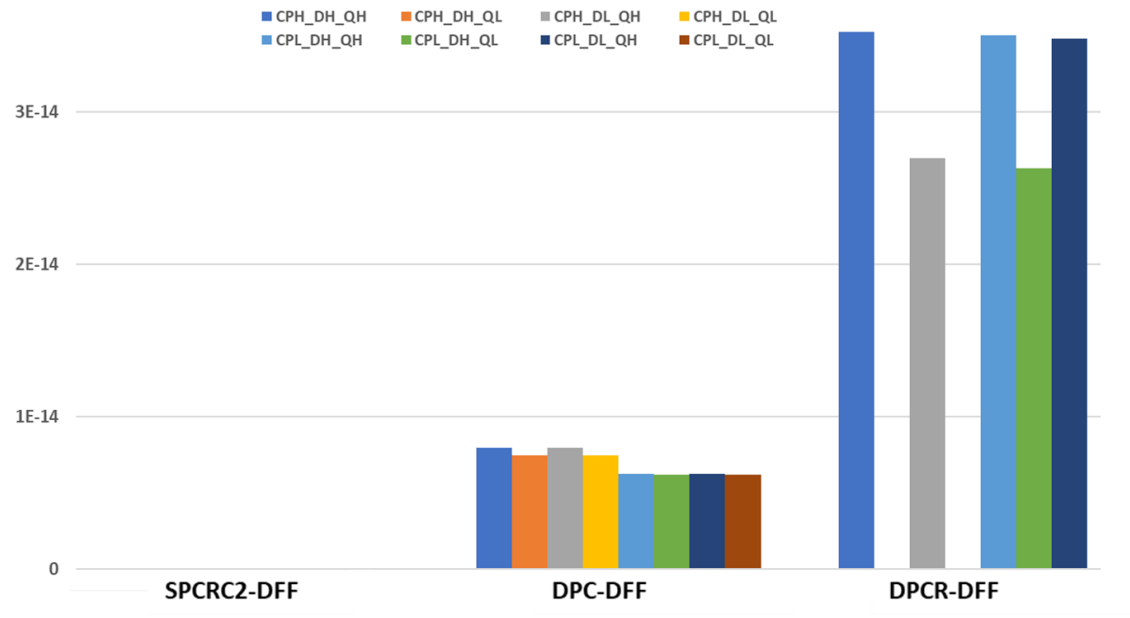


Figure 4-13 Minimum Critical Charge in Coulombs for different DFF

Table 4-5 Monte Carlo Simulation Results showing radiation sensitivity

	DPC_DFF	SPCRC2_DFF	DPCR_DFF	TMR_DFF
Monte Carlo Pass1 Single Node Upset	**81%**	**No Fail**	**5%**	**No Fail**
Monte Carlo Pass2 Multiple Node Upset 0.5um	**81.5%**	**No Fail**	**5.4%**	**No Fail**
Monte Carlo Pass3 Multiple Node Upset 1um	**84%**	**0.1%**	**6.2%**	**No Fail**
Monte Carlo Pass4 Multiple Node Upset 2um	**86%**	**0.3%**	**14%**	**No Fail**
Monte Carlo Pass4 Multiple Node Upset 3um	**90%**	**40%**	**48%**	**No Fail**

4.1.5 Summary

The proposed SPCRC2-DFF which is based on a single-phase clocked latch, differential input stage and C-element latch design is found to be robust and less power consuming with respect to other structures. The single-phase clocking does offer benefits both in power reduction and improving radiation robustness. In this section, basic design, functionality and standalone comparison based on CAD simulation is

given. In Chapter 5 silicon implementation results along with radiation test results are provided.

The proposed flip-flop is suitable for medium to low radiation robustness applications. It requires specific designing of the flip-flop and cannot be implemented with any standard cell library like TMR. Therefore, cost of development could be high like any other radhard flip-flop solution requiring complete designing of flip-flops. Further, it is not suitable for high radiation tolerance applications and relies on standard margining methods to account for device reliability issues over time. Therefore, a new system was developed to address all such issues which is explained in section 4.2.

4.2 Multi-Bit Flip-flop System with Embedded Timing Sensing

The need to have a cost-effective adaptable solution suitable for high radiation tolerance and high reliable applications lead to the design of the proposed multi-bit flip-flop system. It is based on spatial as well as temporal redundancy to overcome all types of radiation related faults. It can also act like an in-situ timing sensor which can detect run time timing violations facilitating DVFS to gain power and performance or adapting according to operating environment. It can be designed with standard library cells thereby reducing the initial cost factor for having a radhard design. The proposed system based on n-bit is shown in Figure 4-14.

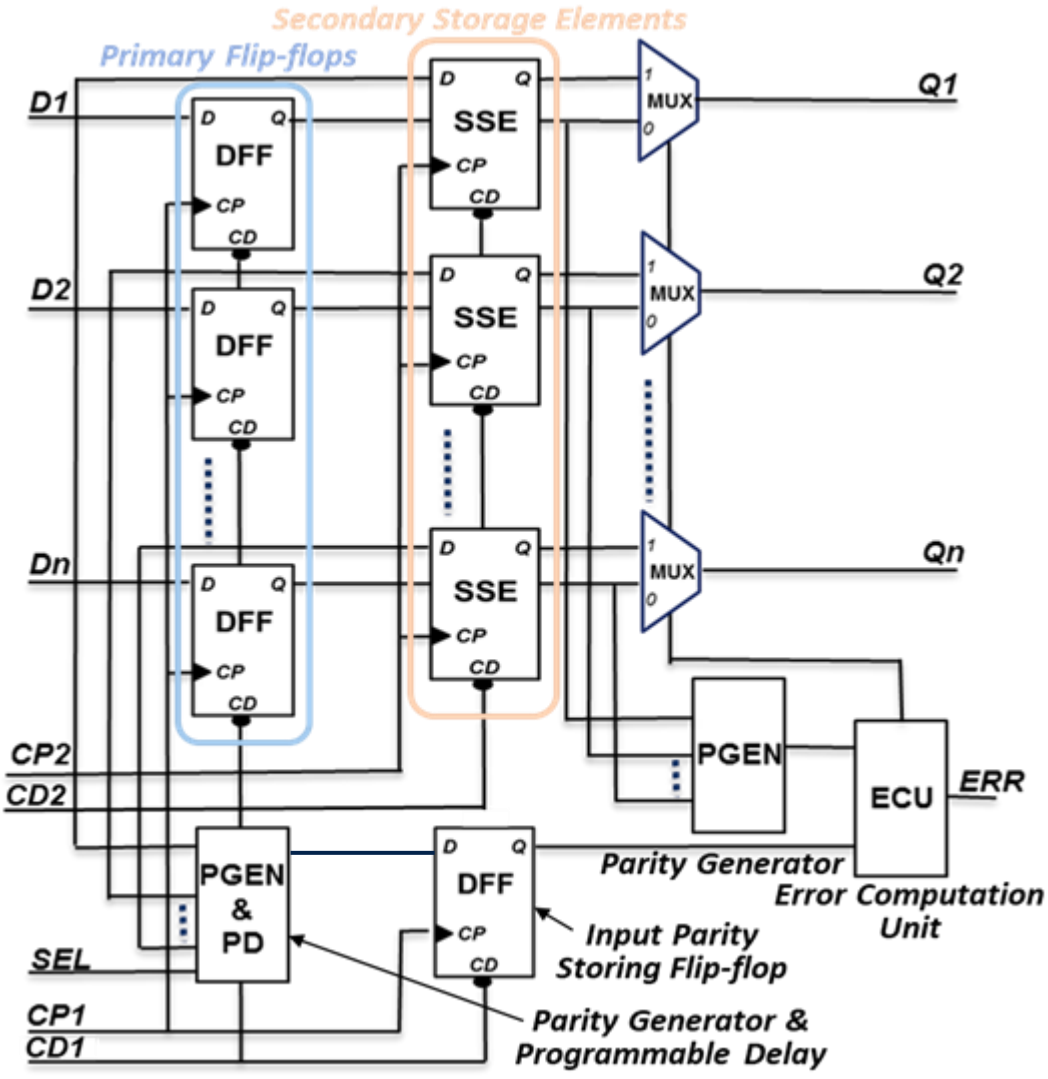


Figure 4-14 Proposed Multi-Bit Flip-flop System Block Diagram

It comprises of

- Primary FFs: any standard D FF can be used.
- Replica Secondary Storage Element (SSE) for each Primary FF in original

system. Here, SSE can be D FF or a simple latch as well. However, latch-based designs would require large hold margins. In the present scope of paper, we concentrate only on FF based SSE.

- PGEN: n-bit Parity Generator. It can be an even or an odd parity generator.
- PD: Programmable Delay with select lines to fix the timing margin.
- Error Computation Unit (ECU) based on basic XOR gates. Its purpose is to compare the input parity stored in FF with the parity computed from the data stored in the primary FFs.
- Output selection unit (MUX or similar logic): depending upon error condition it selects whether data stored in the primary FF should pass through (ERR=0) or from SSE (ERR=1).
- The clock CP2 is skewed with respect to CP1 to provide multiple sampling times for the D inputs so that any transient event due to radiation on the D inputs can be filtered.
- Separate reset lines CD1 and CD2 for primary FFs and SSE respectively enable the circuit to avoid SET-induced faults on reset tree.

To explain the system's working under various scenarios, an example of a 2-bit flip-flop system as a reference is used. Two implementations based on even and odd parity are shown in Figure 4-15 and Figure 4-16, respectively. The parity generators used are XOR (for the first implementation) and XNOR (for the second implementation) gates. The clock going to secondary FFs is skewed with respect to the primary clock. The window of timing error detection is based on XOR and XNOR gate delay, respectively; no additional delay has been added. To understand the system's working, different scenarios that could arise during the FF operation are illustrated in detail below.

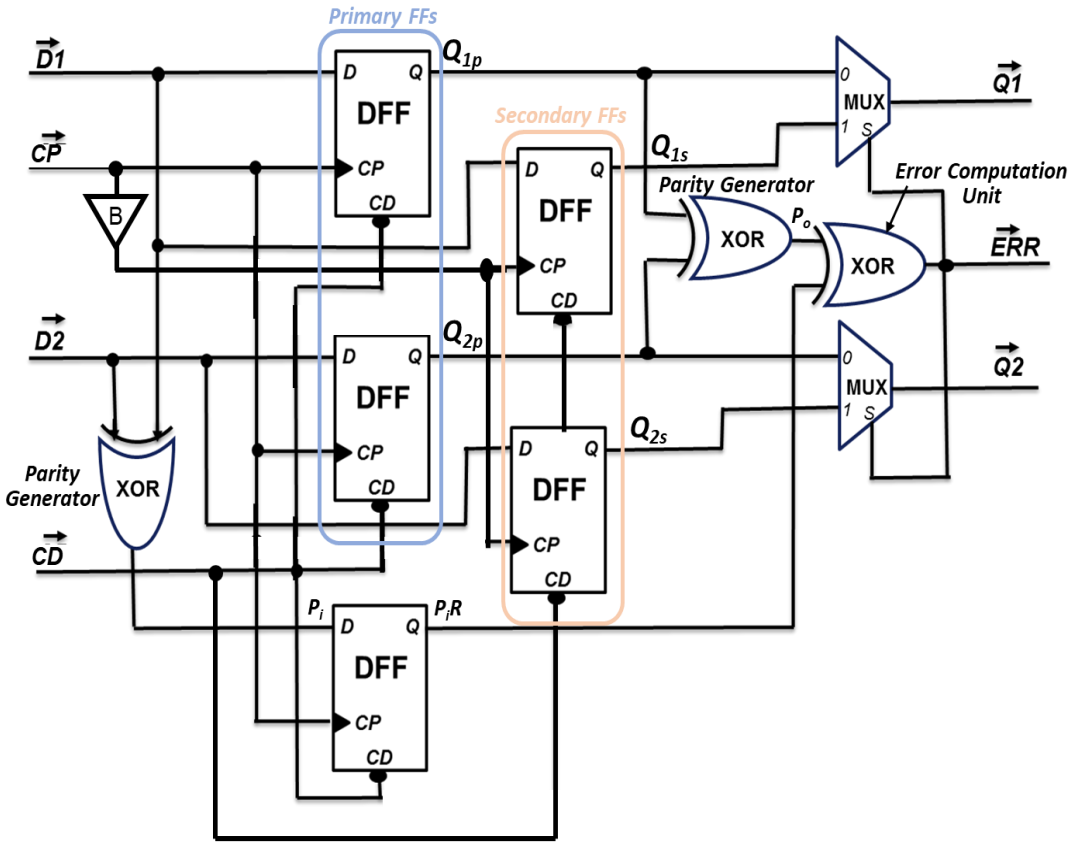


Figure 4-15 2-Bit Even Parity Proposed FF System Circuit Diagram with common reset and skewed clock

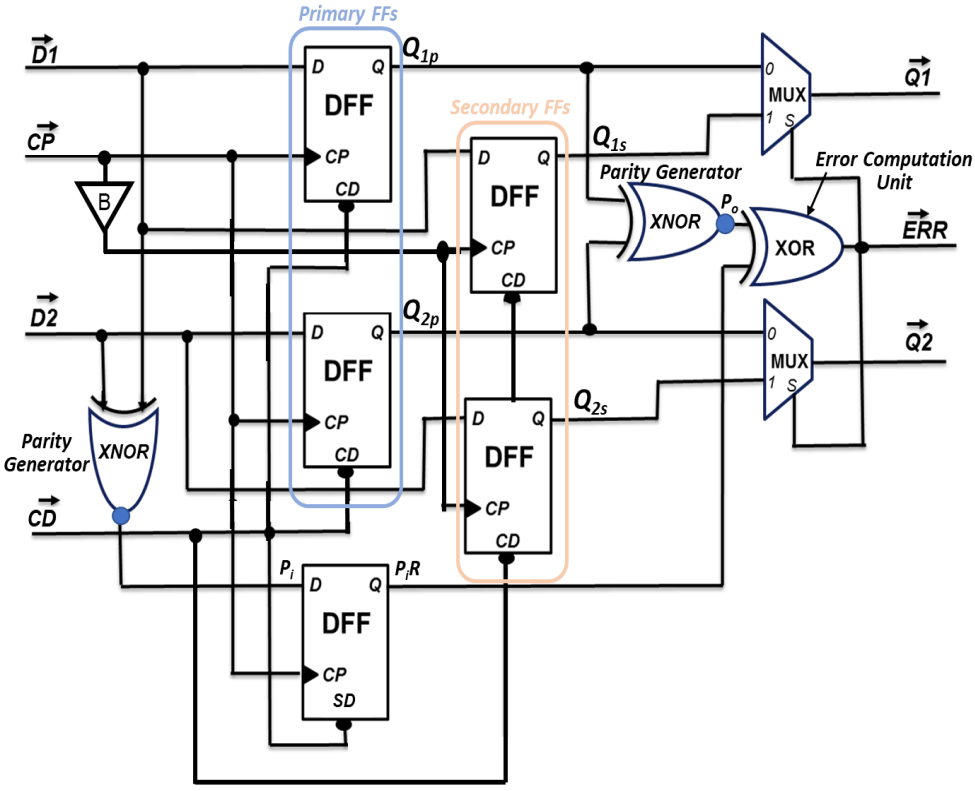


Figure 4-16 2-Bit Odd Parity Proposed FF System Circuit Diagram with common reset and skewed clock

4.2.1 Functionality in Normal Mode

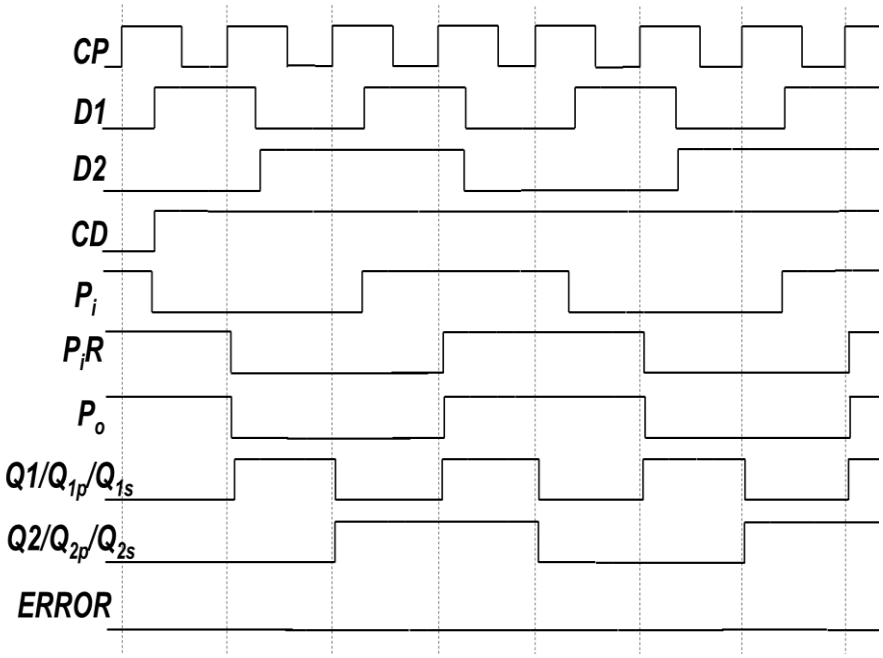


Figure 4-17 2-Bit Even Parity Flip-Flop System Signal Waveforms in normal operation mode

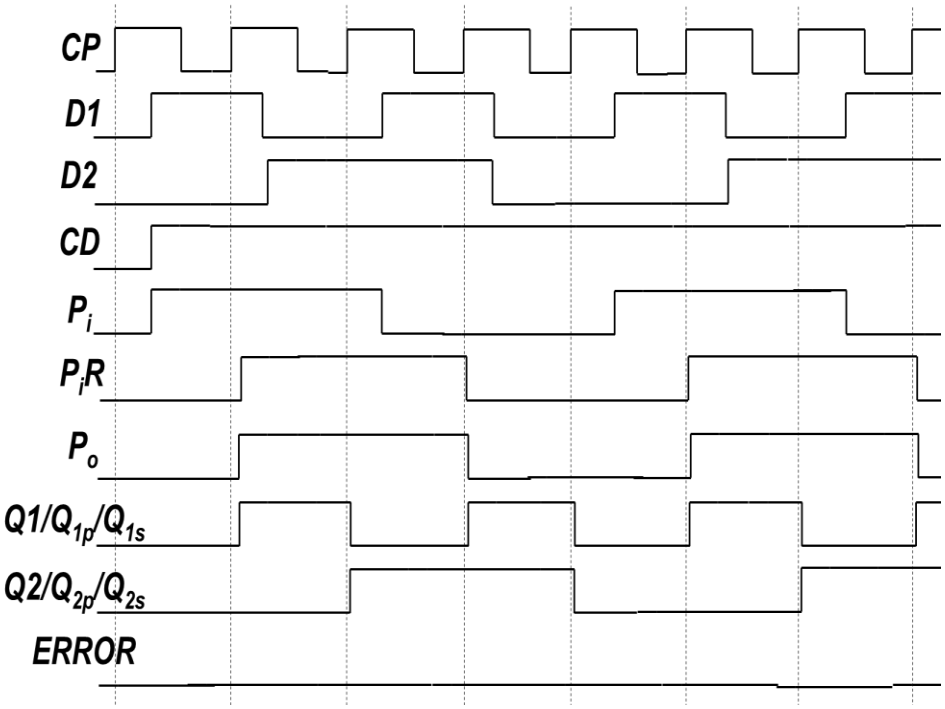


Figure 4-18 2-Bit Odd Parity Proposed FF System Circuit Diagram with common reset and skewed clock

Functionality in normal mode for even party DFF and odd Parity DFF is shown in Figure 4-17 and Figure 4-18 respectively. The primary and secondary FFs samples D1 and D2 at clock edge and Parity (Pi) generated based on D1 and D2 gets stored in parity DFF (PiR). The same is computed based on the output of primary FFs (Po) and is compared with the stored parity bit (PiR). Under normal operation, they are the

same, and the error signal is low. With the error signal low, the output of the primary FFs is passed to Q1 and Q2 outputs. This is the normal working model assuming no-fault condition arises.

4.2.2 Radiation Strike Causing SEU

In case of a radiation event, the data stored on one of the FFs could get disturbed. Here, only a single bit upset is considered, as, during physical implementation, it is ensured that all the FFs belonging to one group are placed at a safe distance from one another so that multi-bit upset (MBU) conditions can be avoided as demonstrated in [54]. More details on placement constraints are given in section Chapter 1. The SEU event on different FFs present in the same group of flip-flops is considered below.

4.2.2.1 Radiation Strike upsets one of the primary FFs

On the upset in one of the primary DFFs, their output changes, resulting in a change of the output parity signal P_o and the input parity bit P_{iR} stored in register remains unchanged. Thereby resulting in the assertion of the error signal. With error signal high, the secondary FF output that holds the correct data are passed to Q1 and Q2 through MUX. Thus, the SEU fault gets filtered out and final outputs Q1 and Q2 remain correct even if the output of one of the primary DFFs is altered. An example of such a scenario is shown in Figure 4-19 in error conditions 1 and 2.

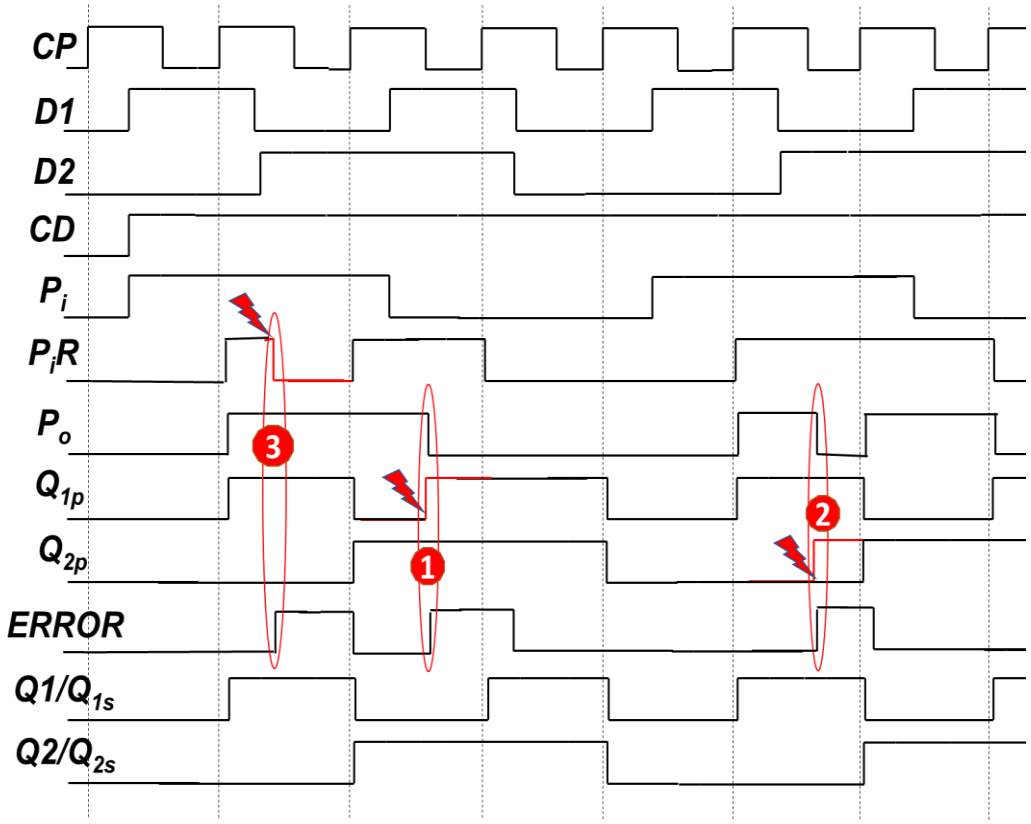


Figure 4-19 2-Bit Even Parity FF System Signal Waveforms showing radiation strike events resulting in SEU faults in different FFs. Condition 1 illustrates the SEU in primary DFF Q1p, condition 2 shows SEU in primary DFF Q2p and condition 3 shows SEU on parity storing DFF

4.2.2.2 Radiation Strike upsets one of the secondary FFs (i.e., SSE)

On the upset in one of the secondary FFs there is no impact on parity generation and comparison logic as shown in Figure 4-20. Hence, no error signal is generated, and the primary FF output continues to pass through MUX to Q1 and Q2.

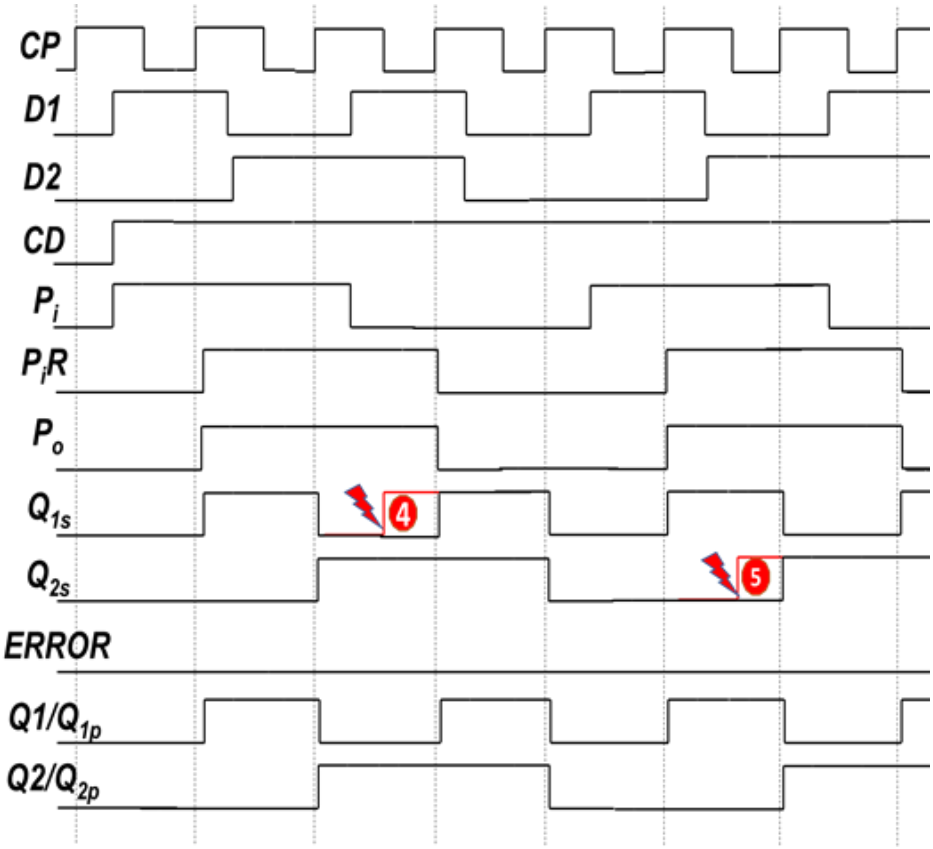


Figure 4-20. 2-Bit Even Parity FF System Signal Waveforms showing radiation strike events resulting in SEU faults in Secondary FFs. Condition 4 illustrates the SEU in secondary DFF Q1s and condition 5 shows SEU in secondary DFF Q2s

4.2.2.3 Radiation Strike upsets the parity storing FF

As shown in Figure 4-19 (error condition 3) an upset in parity storing DFF results in change of PiR, and Po retains its previous value. This will result in the error signal assertion, but both primary FF and SSE have corrected data stored in them, so Q1 and Q2 do not change.

4.2.3 Radiation Strike Causing SET

A transient pulse SET could occur on any combinational path if radiation strikes on combinational logic cells. This may or may not result in change of state of FF. However, since the probability is not zero, as illustrated in [6], the system must take care of SET events as well. Different paths are considered below where an SET can occur and how the impact can be mitigated.

4.2.3.1 SET event on Data Inputs

One of the paths, D1 or D2, could get a glitch arising due to radiation strike close to the rising edge of FF, resulting in incorrect data being latched. Multiple sampling points in the proposed circuit effectively detect the error introduced due to

SET. Different scenarios showing SET on the D1 path captured by different FFs are shown in Fig. 9. The same is true for D2 input as well. In cases when SET is not captured in FFs, there will be no impact on the system. In error condition 6, when parity FF gets corrupted due to a glitch, the error signal goes high, but there is no impact on final outputs Q1 and Q2. In case of error condition 7, when primary FF gets corrupted and Q1p changes its state resulting in a change of Po and subsequently assertion of the error signal, the outputs Q1 and Q2 comes through Q1s and Q2s, which store good values because they are sampling data on skewed clock CP_{Skew}. If SSE (Q1s) gets corrupted (error condition 8), there is no effect on the rest of the circuit, and the output holds a good value. The clock skew should be greater than SET pulse width for the above scenario to hold true.

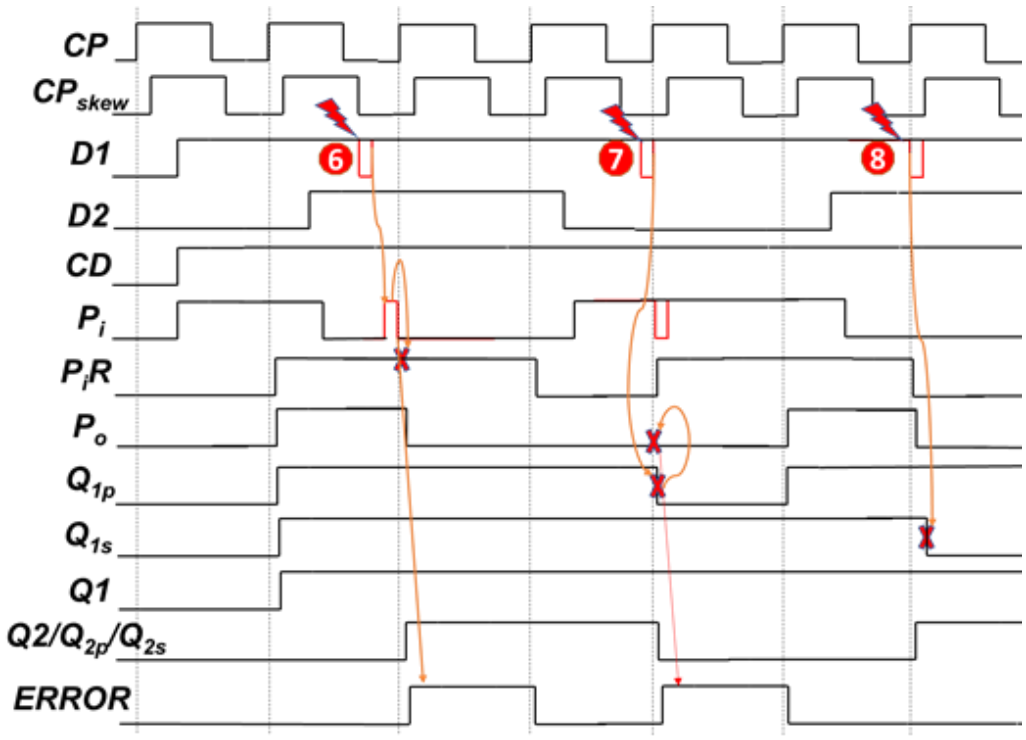


Figure 4-21 2-Bit Even Parity FF System Signal Waveforms showing radiation strike event resulting in SET faults in Data Path D1 at various time intervals. Condition 6 illustrates the SET captured by parity storing DFF, condition 7 illustrates SET captured by Primary DFF Q1p and condition 8 shows SET event captured by secondary DFF Q1s.

4.2.3.2 SET event on Clock paths

Clock paths are susceptible to SET as the data paths. However, due to the construction of balanced tree networks to minimize skew, the capacitance on the nodes is relatively higher, which requires higher energy particles to cause a

meaningful transient on the clock path resulting in failures. Experimental results reported in [56] and [57] on 28nm and 90nm technology nodes respectively show that burst errors due to an SET in the clock tree start to occur for particles with LET > 10 MeVmg-1cm2. The SET on the clock path could result in either clock jitter or radiation induced clock race. The probability of radiation-induced clock jitter resulting in setup violation in flip-flop, is very low, and the same can be detected and corrected with the timing pre-error detection mechanism of the proposed solution. On the other hand, radiation-induced clock race could cause an error in the given system. Robust clock tree solution such as mesh type [56], hardened clock spine [58], etc., can be adopted to mitigate these types of errors. These methods are proven to be effective for higher LETs (> 10 MeVmg-1cm2). In order to make the system more robust specially for low capacitance clock nodes, it is best to deploy SET mitigation at leaf cell level i.e., the clock input of FF. In the proposed system, the clock inputs to primary FFs can be connected to the clock network through delay filters based on guard gates [59] (Figure 4-22). These can filter out unwanted transient pulses on clock lines. The SSE does not require such filters.

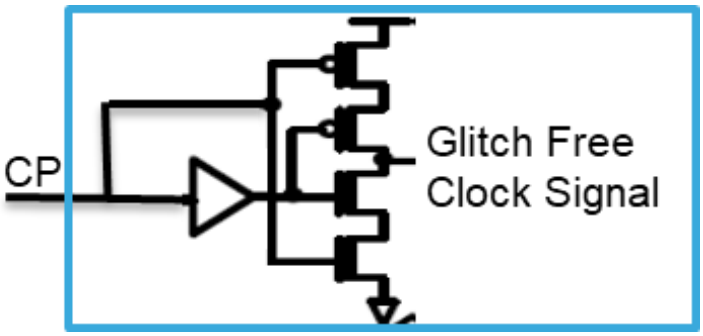


Figure 4-22 Glitch Filter based on Guard Gate [59]

4.2.3.3 SET event on RESET path

An SET on the Reset path could result in localized resetting of flip-flops as the reset buffer tree could have low capacitance points having less critical charge. To avoid this, separate reset paths can be used inside multi-bit system, as shown in Figure 4-23. In the case of even parity, the DFF storing parity should give “1” on reset (i.e., of SET type) and in the case of odd parity it should give “0”. This is required to generate the error condition, when an SET event occurs on CD1 (as shown in Figure 4-24), which eventually makes Q1-Q2 controlled by SSE. This requirement of specific polarity on reset also results in false error signal assertion in the actual reset condition. Normally,

this false error assertion is automatically ignored by the system as the whole digital system will be under reset, but for some specific cases, the system designer needs to take care of this. In the case of an event on CD2, there is no impact as Q1 and Q2 are driven by primary FFs, which are unaffected. CD1 and CD2 are controlled with the same reset signal at the top but the buffer tree is different. Another way of managing this is to place glitch filtering at the input of each flip-flop reset but the penalty of that could be huge in terms of area and power.

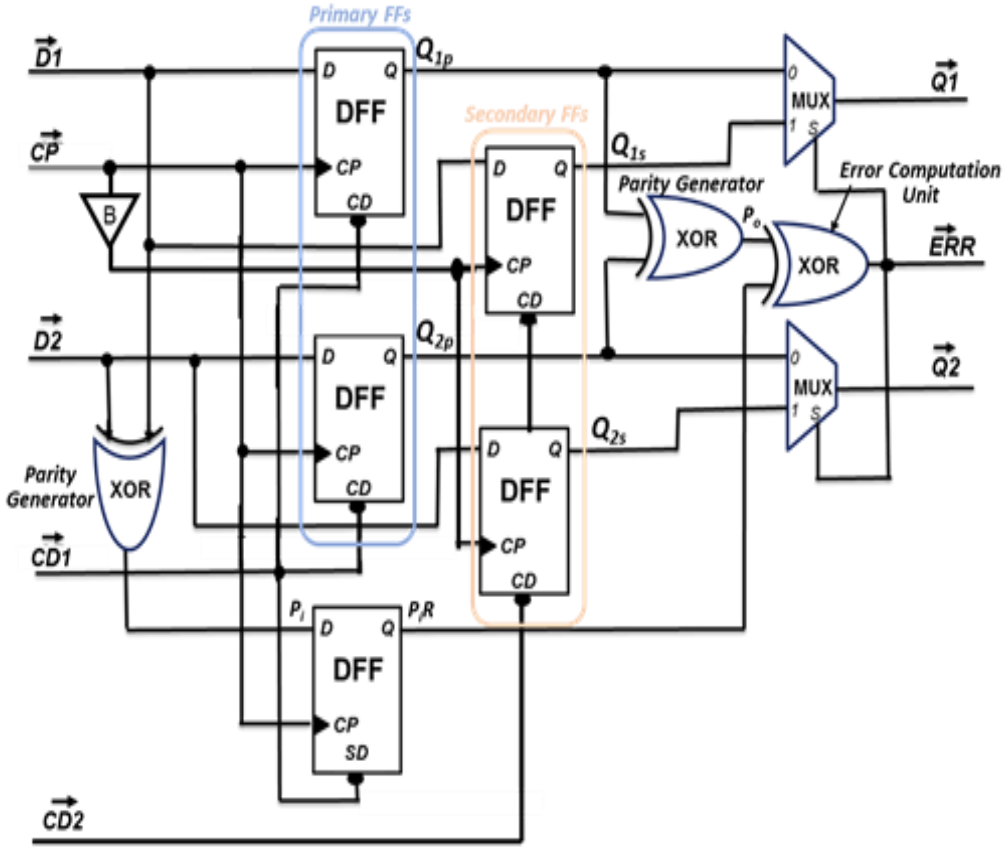


Figure 4-23 2-Bit Even Parity Proposed FF System Circuit Diagram with sperate reset and skewed clock.

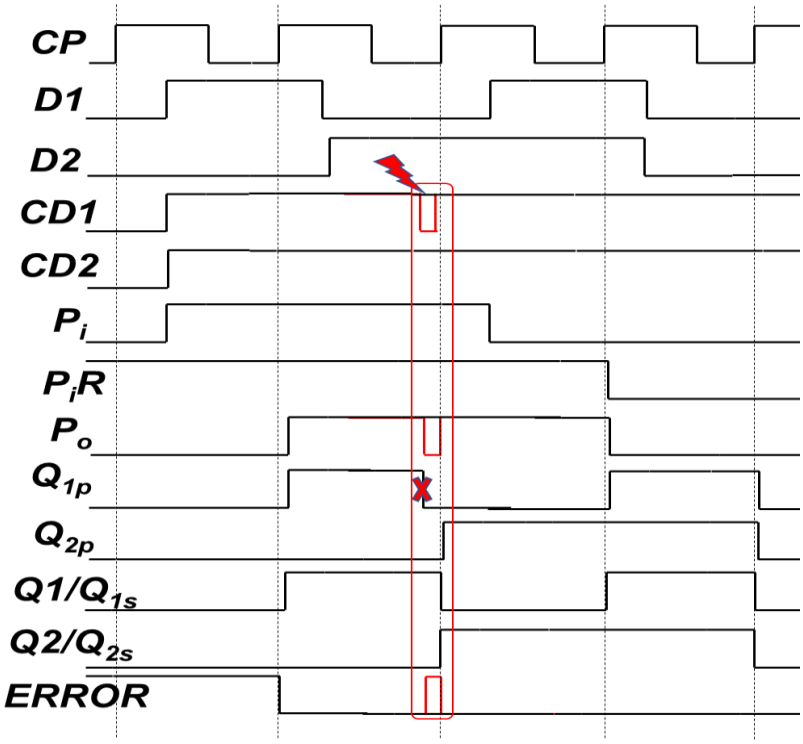


Figure 4-24 2-Bit Even Parity FF System Signal Waveforms showing radiation strike events resulting in SET on reset path CD1

4.2.3.4 SET event on added circuitry

The added logic of parity computation, error detection, and correction is also prone to SET faults. Any SET event in the input party generation circuit would result in a glitch on Pi input which can be latched and result in corruption of PiR. However, this will be masked as explained in 4.2.2.3, and will not affect the final output. SET on output parity computation and the error generation circuit would result in a glitch on the ERROR signal which again will not affect the final outputs and can be registered as error event by the system. Any SET event on output mux driving the final output would result in a glitch on outputs which could eventually propagate to data inputs of subsequent stage FFs. They are treated like SET on data inputs for subsequent stage flip-flops and will be filtered by the mechanism already explained in 4.2.3.1.

4.2.4 Timing Pre-error Sensing Mode

The parity generation and comparison logic also enable the timing pre-error sensing capability. The transitions on data inputs occurring very close to the clock edge can be detected. This concept is very well illustrated in [42]. The input parity bit computed from D1 and D2 gets delayed by the XOR gate intrinsic delay and stored in parity FF, whereas the parity bit calculated from the outputs of the primary FF will be

based upon the data sampled in primary FFs without any delay on the same clock edge. When D1 or D2 changes very close to the clock rising edge, the two parity bits will be different, resulting in the assertion of the ERROR signal, as shown in Figure 4-25. The ERROR signal arising due to timing is different in terms of periodicity with respect to error from radiation events. It is more systematic i.e.; it will be asserted more frequently. The digital system can work in a closed loop based on this feedback from the FFs as demonstrated in [47]. It can take corrective actions like scaling supply voltage, reducing clock frequency, etc., to reach the OOP. Here, the primary outputs Q1 and Q2 are not affected and store correct value, therefore no impact on system functionality. One limitation of this logic is that in a particular case, wherein D1 and D2 both change simultaneously, resulting in same parity computation, the timing sensing won't be able to detect the data alteration. Nevertheless, as timing faults are systematic faults, the error could get captured in subsequent clock cycles when parity change occurs. In order to tune the window of timing error detection, the delay on the input parity generation path can further be tuned by including a programmable delay in the path or a fixed delay in the path as per system and process requirements.

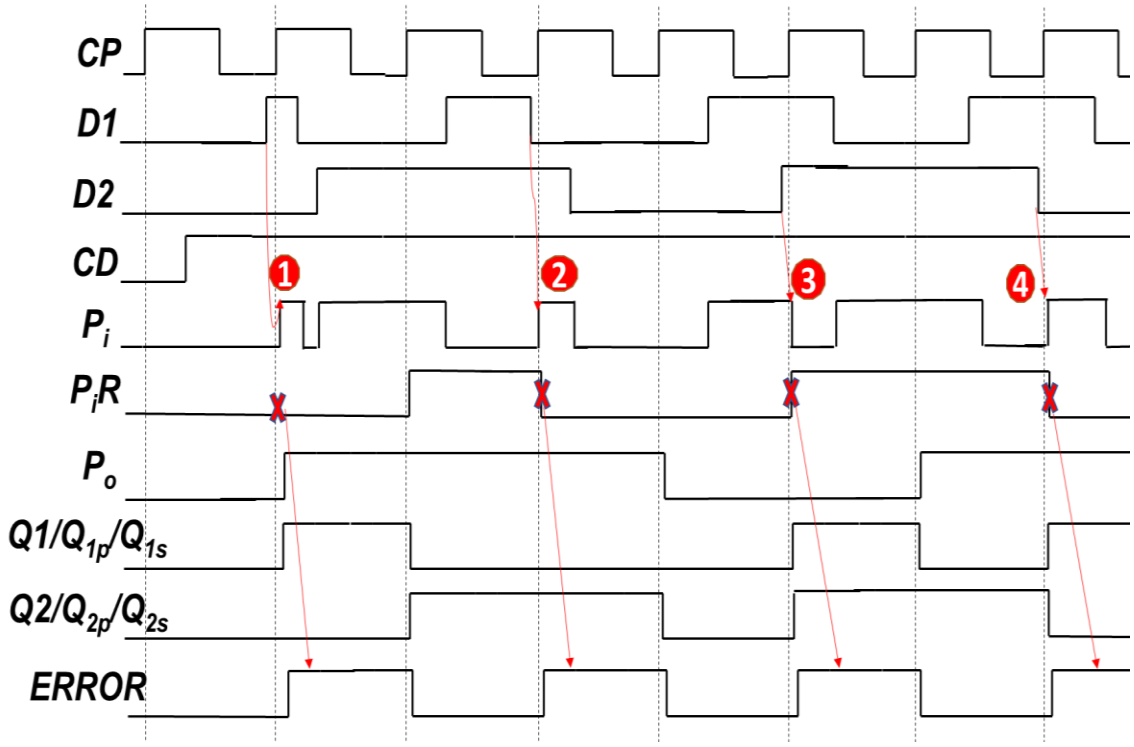


Figure 4-25 2-Bit Even Parity FF System Signal Waveforms showing timing pre-error sensing capability. Condition 1 and 2 illustrate the transitions on D1 input close to clock edge. Condition 3 and 4 illustrate the transition on D2 input close to clock edge.

4.2.5 Multiple Event Upsets

Apart from various scenarios discussed above, there is one particular scenario of multiple events wherein multiple strikes could result in the accumulation of bitflips in flip-flops. This condition would arise if the digital system is in power saving mode by applying clock gating, and no refresh cycle is provided to correct the data stored in primary and secondary FFs. The proposed system does not automatically correct the data stored in FFs. It only detects and masks the bit upsets introduced due to radiation event. Typically, such bit upsets are automatically corrected through subsequent clock pulses or dedicated refresh cycles, or dedicated self-correcting designs are needed, like self-correcting ΔTMR [37]. The detection capability of the proposed system allows the system designer to use the ERROR signal to detect a radiation strike event and provide refresh cycles to the system so that accumulation of errors can be avoided, and good functionality of the system can be maintained. However, an actual error condition might still happen if the ERROR signal is not asserted on the first radiation strike and the subsequent strike happens on the same flip-flop group, but the probability of such occurrence is very low.

4.2.6 Digital System Design based on Proposed Flip-flop

As mentioned earlier, the proposed circuit can be designed with standard library cells. It does not require the designing of specific rad-hard cells. With certain design constraints, any digital system can be implemented with standard semi-custom design flow using the proposed flip-flop. In a generic digital design, the sequential elements can be replaced with proposed DFF with grouping of DFFs belonging to similar power and clock domains. An example of a typical digital system path with the proposed 2-bit DFF implementation is shown in Fig. 14. The ERROR signals coming from different groups are combined with OR logic, then passed to a sample and count circuit to generate the error signal. For timing error, count should be more than two in reasonable time window, whereas for other cases where the count is less than two, they can be treated as radiation error.

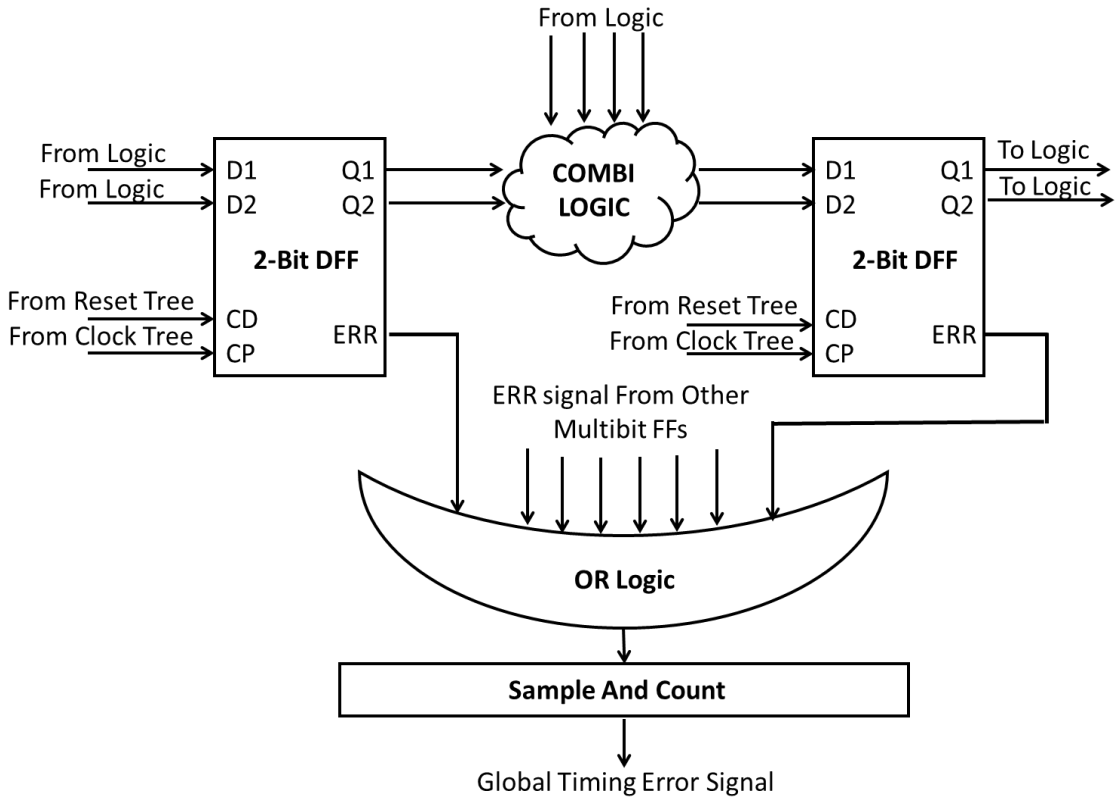


Figure 4-26 Digital System based on the Proposed 2-bit DFF.

4.2.6.1 Timing Constraints with Proposed Design

Additional logic required for the proposed circuit does impose a timing penalty on the digital system along with particular constraints for the proper functioning of the system. The overall impact on performance and timing constraints required for the proposed methodology can be well understood by the below equations. For a standard digital system design, basic timing constraints are given by: -

$$T_{CKPeriod} > T_{pdFF} + T_{comb} + T_{setupFF} + T_{margin} - T_{skew} \quad (4.1)$$

$$T_{comb} + T_{skew} > T_{holdFF} \quad (4.2)$$

Where $T_{CKPeriod}$ is the Clock Period, T_{pdFF} is the CP-Q delay of STD launch FF, $T_{setupFF}$ is the setup time of STD capture FF, T_{comb} is the combinational delay between launch and capture FF, T_{skew} is the clock skew between launch and capture FF clock, T_{holdFF} is the hold time of STD FF and T_{margin} is the extra time margin taken to account for PVT variations, voltage drops, jitter, aging etc. as shown in Figure 3-19. Maximum frequency of digital design is limited by equation 4.1 where T_{margin} has a significant

weight. In the proposed multibit system, timing margin can be squeezed with the help of timing pre-error detection. The timing constraint equation for maximum frequency is given by equation 4.3 and for hold time equation 4.4.

$$T_{CKPeriod} > T_{pdFF} + T_{comb} + T_{setupFF} + T_{mux} + T_{PGdelay} + T_{error} - T_{skew} \quad (4.3)$$

$$T_{comb} + T_{skew} + T_{cpskew} > T_{holdFF} \quad (4.4)$$

$$T_{margin} > T_{mux} + T_{PGdelay} + T_{error} \quad (4.5)$$

$$T_{cpskew} < T_{pdFF} + T_{error} \quad (4.6)$$

Here, T_{cpskew} is the introduced clock skew between primary and secondary FFs, Tmux is the delay of output mux of launch FF, $T_{PGdelay}$ is the delay of input parity generator of capture FF, Terror is the propagation delay of ERROR signal from output of primary launch FFs. For the system to be effective and efficient with no impact on the target frequency of the original design, time margins taken during implementation should compensate for the increase in delay components as shown in equation 4.5. Usually, margins taken for the desired operating point are sufficient to offer optimization, even after compensating the additional delays [25] [45] [44] [42] [47] [46]. This has also been demonstrated in the subsequent sections with experimental data. The input and output parity generator delay becomes the timing margin window for detecting timing pre-errors and limiting factor to the number of bits that can be grouped. As for higher bit groups, the parity generator delay would be more.

As explained in 4.2.3, the width of SET that can be filtered on the D inputs of FF is driven by clock skew introduced between primary and secondary FF. To filter wider pulses, more clock skew needs to be introduced. An increase in clock skew, firstly, impacts the hold timing constraints as per relation given in equation 4.4; secondly, it is also limited by internal cell delays as equation 4.6. Using this relation and knowing the desired pulse widths to be filtered, appropriate skew values can be introduced.

4.2.6.2 Digital Design Flow with Proposed Design:

A standard digital implementation flow diagram is shown in Figure 4-27, along with additional steps required to insert multi-bit FFs. The grouping of FFs is done after compiled netlist is available during synthesis flow. The grouping is done for FFs with common clock and power domain and at the same hierarchy level. After grouping, FFs

are replaced with equivalent multi-bit FFs. Thereafter, a new netlist is generated along with additional timing constraints, without any change in cell list and placement constraints. The generated netlist is verified with respect to the original netlist with a formal equivalence checking tool by setting appropriate black-box definitions and constraints on added logic. After checks with this new netlist and constraints, DFT insertion continues, and synthesis is completed. The gate-level netlist and constraints are passed to the backend implementation tool for the next steps.

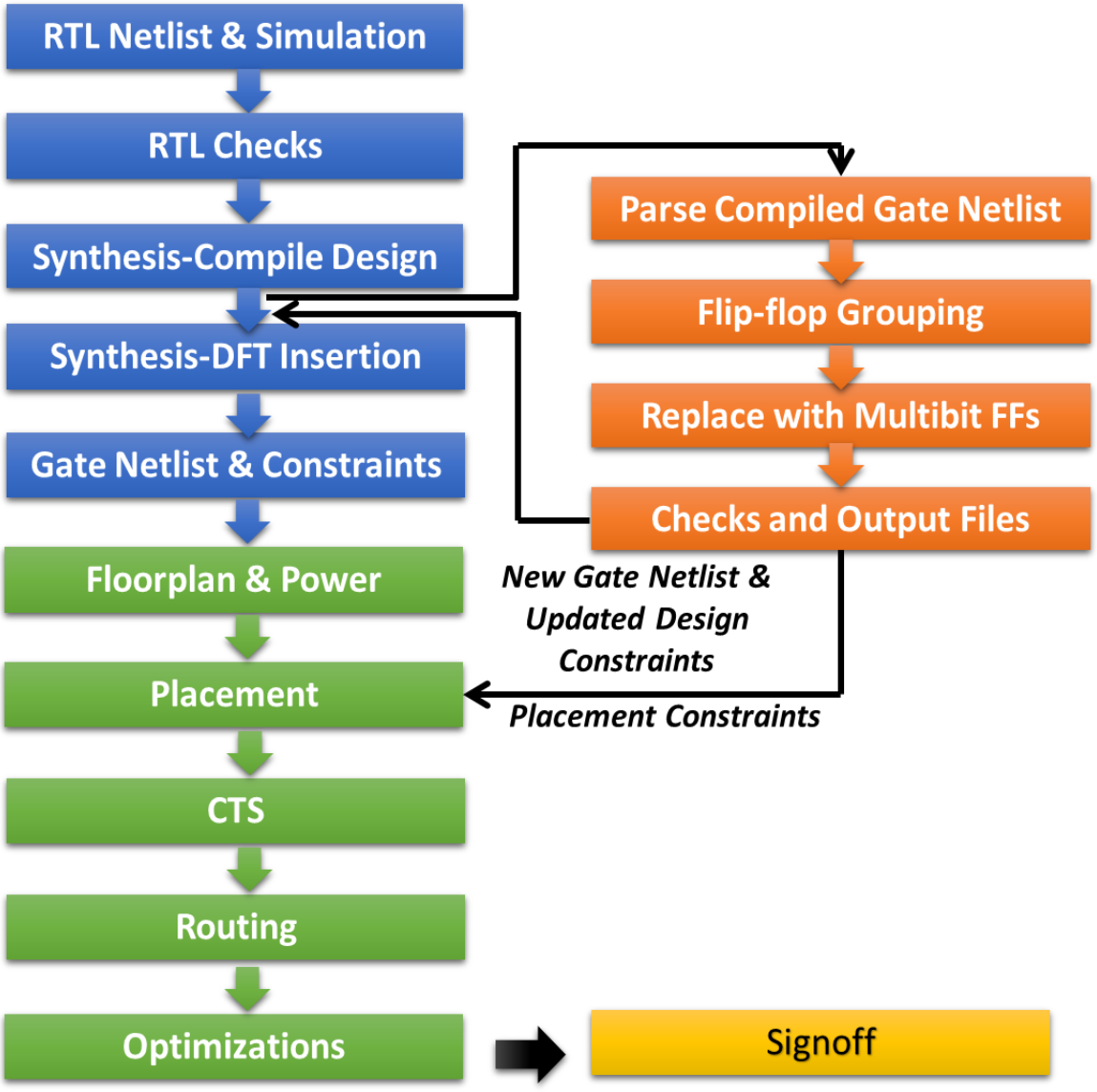


Figure 4-27 Digital Implementation flow diagram for Proposed DFF

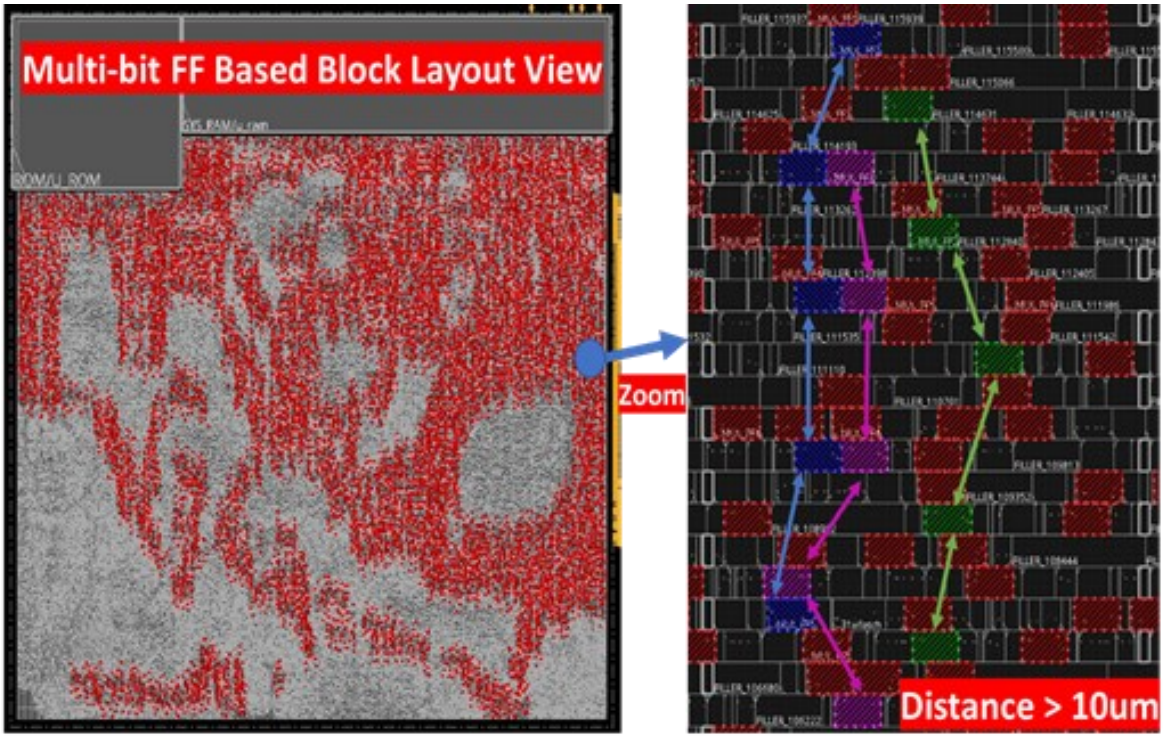


Figure 4-28 Multi-bit FF based ARM blocks layout view showing placed cells. Instances in red colour are showing 2-bit grouped flip-flops. In the zoomed view, instances of three different 2-bit groups are shown as example in blue, magenta and green colour. With the help of placement constraint, a minimum distance of 10um is maintained within the cells belonging to same group.

The following backend implementation flow in green in Figure 4-27 is a standard one with just one additional placement constraint during the placement step wherein spacing between cells belonging to one FF group is forced during the cell placement step to avoid multi-bit/multi-node upsets on cells of same group. This is shown in Figure 4-28 where cells of the same group are placed at least 10um apart from each other, avoiding MBU within the same group. This approach is presented in [54] [55] wherein a design flow for TMR flip-flop is presented and impact of spacing between flip-flops is presented. The space between flip-flops of the same group can be filled with other design cells, not causing any area penalty. However, for higher bit groupings (> 8bits), the congestion issues do appear due to complex interleaved routing spread over bigger area. Finally, signoff checks are performed on design after clock tree build-up, routing, and timing optimizations.

The complete flow is automated using TCL scripts for synthesis, place and route and formal verification. The scripts are not shared due to confidentiality.

4.2.7 Multi-bit Flip-flop CAD Assessment

The proposed system is implemented in 90 nm ST BCD technology based on a High Vt standard cell library. No special radiation hardened cells were developed for implementation of proposed design. The design and implementation was purely done using standard library cells, standard static memory and standard design flow. The proposed design is validated on standalone basis using SPICE simulations and through digital system implementation based on proposed design. For digital implementation functional simulations and formal verification has been performed and physical implementation number were extracted to study the impact on area, timing and power.

4.2.7.1 Standalone Flip-flop implementation and comparison:

The proposed design is implemented in multiple bit configurations based on standard library cells in order to validate the functionality of the flip-flop system and to extract various parameters of flip-flop. The design is based on standard dual clock phase master-slave D FF (STD FF) shown in Figure 4-1 and the same has been used as reference for comparative analysis and data normalization. For the proposed design 2-bit, 4-bit, and 8-bit even parity versions are implemented. Standard TMR (Figure 2-15) and ∆TMR (Figure 2-16) are also implemented to compare the proposed design effectiveness with respect to prevalent designs used in industry. Simulations were caried out on all FFs to characterize various parameters of FFs under default working mode with no error condition. Table 4-6 summarizes the main characteristics of the architectures mentioned above. Effective per bit data of proposed FF on standalone basis shows 2x impact on CP-Q delay, ~3.5x increase in area, ~5x on switching power, and ~1.5x impact on setup time with respect to STD FF. These results are in line with other standard robust solutions TMR and ∆TMR. In ∆TMR FF, where temporal hardening is used by adding clock skew, the impact on timing is very high as it requires at least two flip-flops sampled data to be resolved so that the majority voter could converge to the valid output. In the proposed system, the setup time and propagation delay are independent of the delay in input parity logic and clock skew, as in default case of no error condition, the final outputs are governed by primary FFs passing through the output mux. It is also observed that with higher bit groupings in the proposed methodology, the area and power show improvement and performance remain the same. Only ∆TMR and the proposed design are tolerant to

both SEU and SET. The SET pulse width which can be filtered by different flip-flops is also computed by giving varied pulse width glitches on the D input of the flip-flop close to the clock edge. It is observed that the TMR and STD DFF can capture data with pulse widths more than 87 ps at typical corner. This comes as inherent property of the flip-flop. Any glitch less than this value is likely to be filtered by the flip-flop. But in a radiation environment the glitch width can go above 100ps where these flip-flop circuits would tend to get affected by SET. In case of ΔTMR, a SET pulse up to 285 ps can be filtered, and in the proposed flip-flop design with single buffer clock skew, SET pulse up to 142 ps, 150 ps, and 165 ps for 2-, 4- and 8-bit implementation respectively can be filtered. The same can be enhanced by increasing the clock skew respecting the timing constraints given in equations 4.4 and 4.6. A variation of minimum SET pulse width filtered with respect to clock skew between primary and secondary flip-flop is shown in Figure 4-29. Introducing increased clock skew would increase the SET filtering capability but at the same time it adversely impacts the timing performance of the circuit. The optimal value should be chosen depending on the design requirement and radiation environment.

Table 4-6 Standalone Simulation results for different FF variants at typical process, 1.0 V and 25°C. Data is normalized to STD FF data.

	STD FF	**TMR FF**	**ΔTMR FF**	**2-Bit FF***	**4-Bit FF***	**8-Bit FF***
CLK Cap	1	3.01	3.03	1.97	1.63	1.48
CP-Q Delay	1	1.86	1.88	2.04	2.02	2.03
Setup	1	1	7.05	1.46	1.46	1.46
Area	1	3.9	4.5	3.85	3.51	3.18
Switching Power 25% Data Activity	1	4.23	5.52	4.99	5.02	3.74
Min Captured Pulse Width on D inp (ps)	87.5	87.5	285.5	142.5	150	165.5
SET Tolerance	No	No	Yes	Yes	Yes	Yes
SEU Tolerance	No	Yes	Yes	Yes	Yes	Yes
Timing Pre-error Detection	No	No	No	Yes	Yes	Yes

* Data reported is scaled to single bit for one-to-one comparison with other Flip-Flops

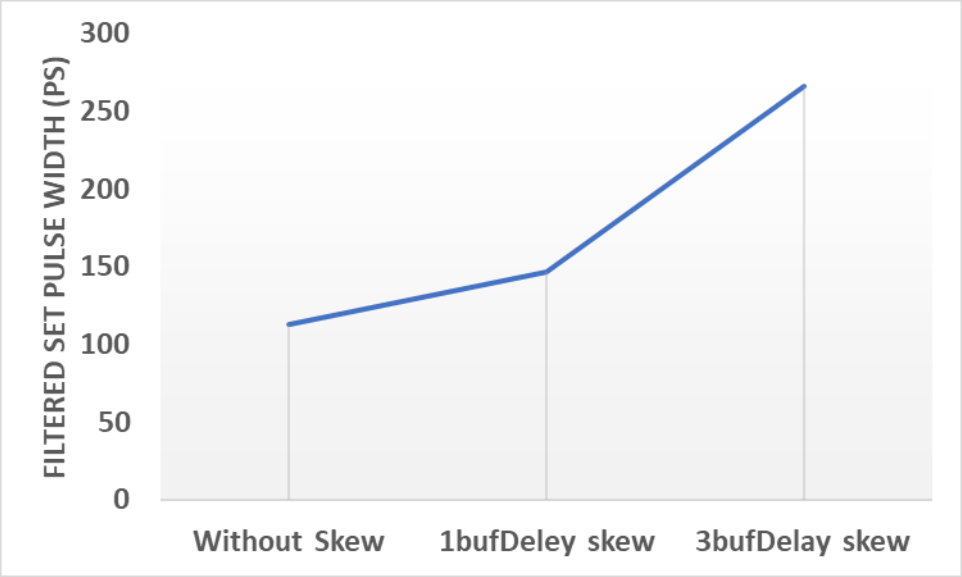


Figure 4-29 Graph Showing minimum SET pulse width that can be filtered by 2-Bit even parity implementation with different clock skew

To validate the timing sensing capability of the proposed design an exhaustive monte-carlo simulation run was performed. The time difference between data and clock going into the flip-flop were varied and for each time instance 10000 monte-carlo runs performed to extract the operational failures in flip-flop and timing error signal generation from the flip-flop. The timing window for pre-error detection is shown in Figure 4-30 for different implementation configurations. The 8-bit FF has the largest window size as input parity logic has more delay with respect to 4-bit and 2-bit configurations. The data path delay introduced in parity storing flip-flop with respect to the primary flip-flops directly governs the timing pre-error detection window size, and it can be enhanced by adding additional delay in the path. A higher window size improves the efficacy of pre-error detection as with higher window size the probability of missing a timing error would be low as demonstrated in [42]. On the other hand, a higher window size would translate into more margins for design that can adversely impact the optimization efficiency of the system. There is a trade-off between efficacy of error detection with respect to optimization efficiency. Typically, the circuit can be tuned to have window size sufficient to cover minimum resolution of clock source used or minimum step size of voltage regulator controlling the supply of the digital system. This is to ensure that during the frequency and voltage regulation the minimum step increase or decrease should not lead to huge variation in path delays.

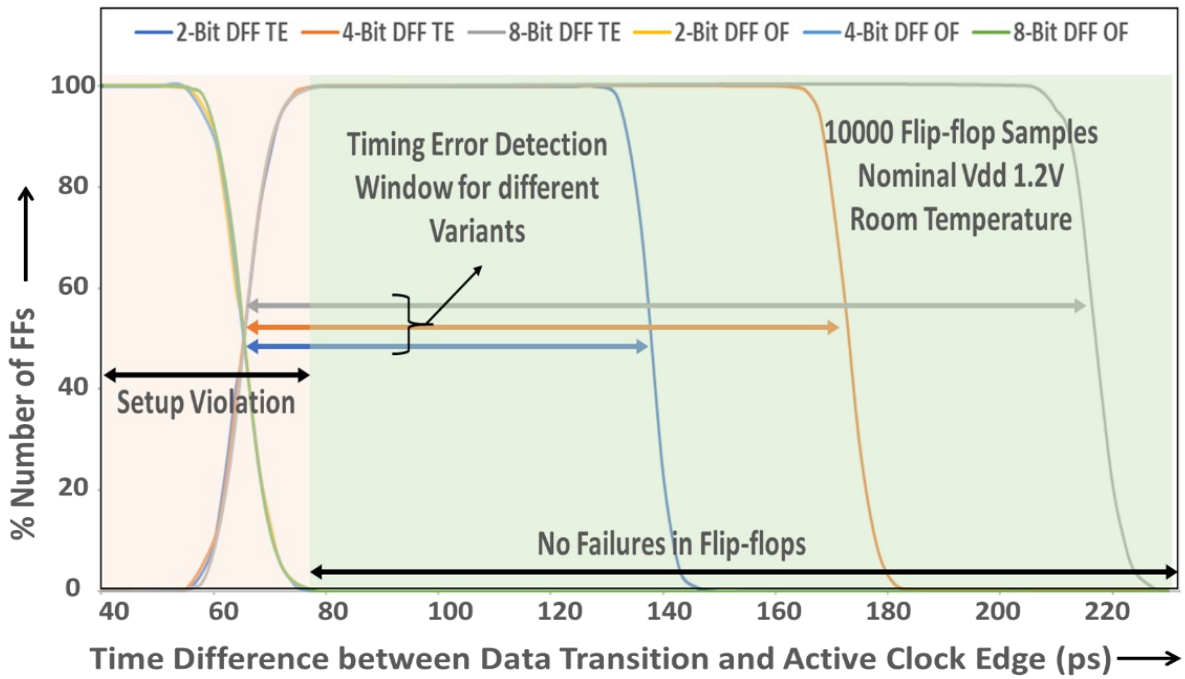


Figure 4-30 Graph showing Number of flip-flops Failing with change in time difference between data and clock. Data obtained from Monte Carlo simulations at nominal operating conditions. TE suffix denotes number of Flip-flops showing timing pre-error and OF denotes actual operation failures in flip-flops

4.2.7.2 Digital system implementation and comparison

A Digital Microcontroller (µC) (shown in Figure 4-31) based on ARM cortex M4, memory, and basic peripherals like GPIO, registers bank, counter, etc., was implemented to study the implications of the proposed design in a digital application. The design has approximately 200K gates and 4.82k standard DFFs. 32Kbyte standard ROM is used for code memory and 32Kbyte Standard RAM is used for system memory. SRAM circuit has dedicated SECDED EDAC mechanism with auto correction. One instance was implemented with reference DFF. For the proposed design, all the DFFs in the design were replaced with the proposed robust DFF system as per the design flow mentioned in section 4.2.6.2. Only 2-, 4-, and 8-bit configuration were implemented completely as for higher configurations the trade-offs were very poor due to increase in routing congestion and high timing penalty. Another instance was implemented with TMR DFF based µC to benchmark against a standard radiation hardening methodology. Both TMR and the proposed design based µCs followed the same placement constraints of introducing spacing between DFF of the same group.

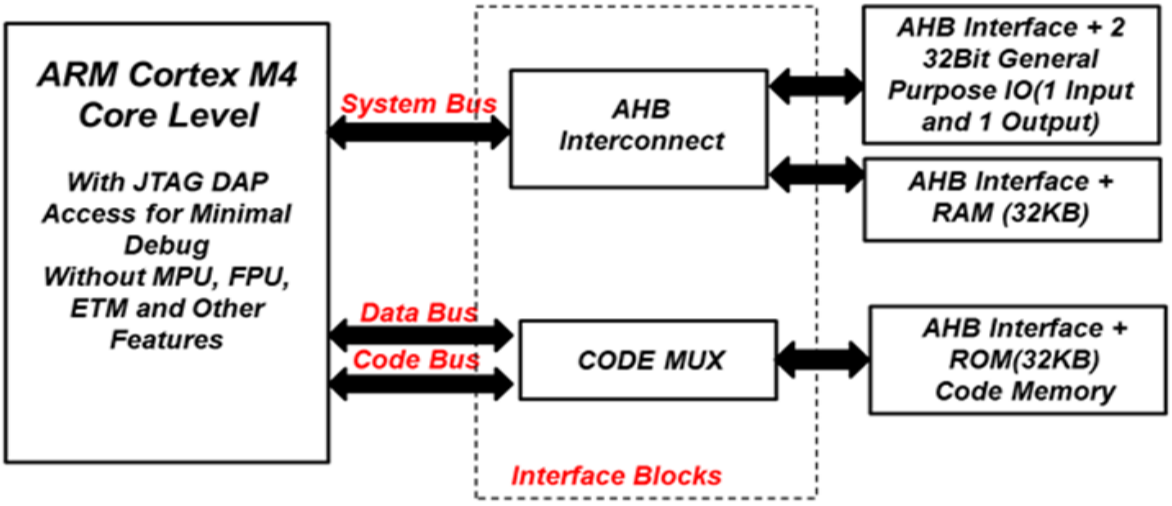


Figure 4-31 Microcontroller (µC) architecture implemented

For the proposed design, the number of standard DFFs which can be grouped to be replaced with proposed DFF was extracted from implementation data. Figure 4-32 shows the percentage share of different bit groupings formed in different implementations of the proposed multi-bit system. It shows that in the given µC design more than 95% of the flip-flops can be grouped in either 2-, 4- or 8-bit groups. This could be different for other designs but in the current design replacement percentage was quite high. With higher bit groupings more area savings is achieved.

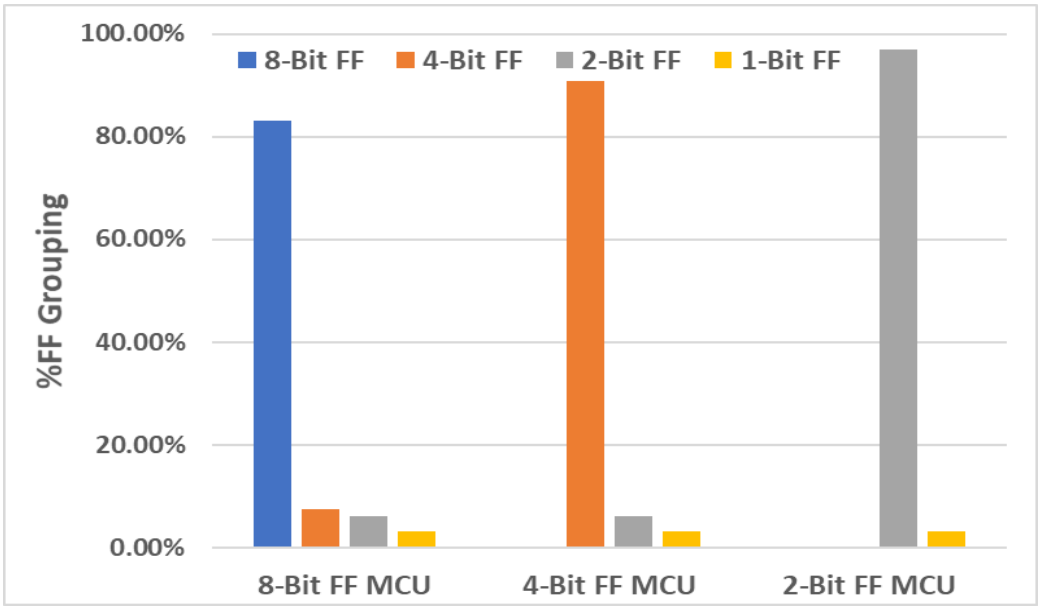


Figure 4-32 Percentage Number of different FF groupings in different µC implementation

The implementation trials were done using the Cadence Innovus tool at 18 ns clock period and signoff corner wc_1.00V_125°C. The timing margin for robust µCs is reduced by 300ps for implementation trials, to account for additional logic delay. The

core area of the design was reduced in multiple implementation trials for different DFF variants for the given target frequency till no timing and design rule checks (DRC) violations were observed. The results shown in Table 4-7 are in line with the hardening benchmark TMR DFF. With higher bit groupings of 8-bit area and leakage power are better than for the TMR solution. Also, with the higher grouping of DFFs, the area, leakage power, and number of DFFs added reduces, whereas vector less dynamic power reported by the tool increases due to more switching in redundant logic. To study the timing impact, the timing histogram for different implementation was extracted from the innovus tool. Figure 4-33 shows the number of paths and timing slack for different implementations. It shows that at worst corner wc_1.00V_125°C, approximately 15% of the paths have slack < 500ps, and the rest have more than 500ps margin. Also, the worst critical path delay scenario may or may not occur during the device lifetime. Therefore, there is a sufficient margin for the typical operating range, which can be optimized with the help of timing pre-error detection, and optimal operating point can be found.

Table 4-7 Place & Route data from µC implementation done with different FF variants. Data is normalized to STD. FF data.

Flip-flop Variant used	STD FF	TMR FF	2-Bit FF	4-Bit FF	8-Bit FF
Core Area (with Macros)	1	1.39	1.36	1.33	1.31
Core Area (without Macros)	1	1.78	1.71	1.64	1.60
Num. of FF	1	3.00	2.51	2.29	2.19
Leakage Power	1	1.43	1.49	1.43	1.37
Vector less Dynamic Power	1	1.84	1.91	2.11	2.16

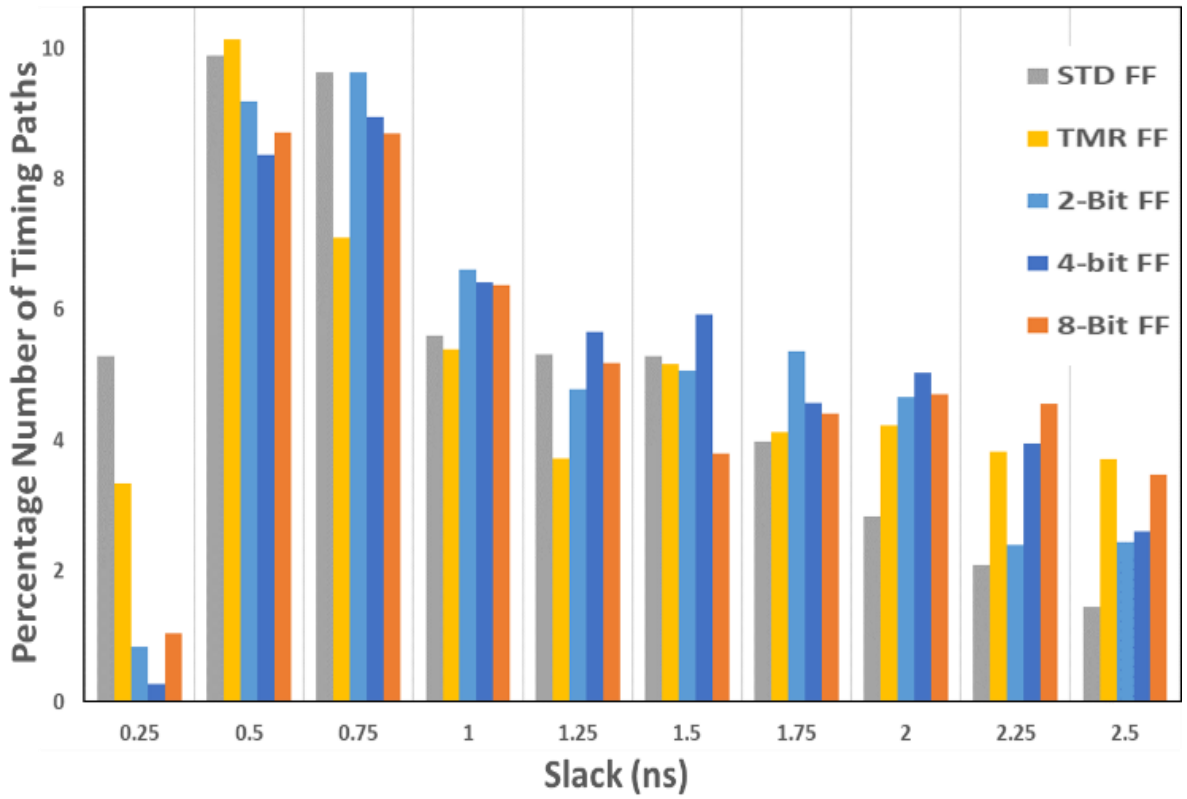


Figure 4-33 Timing Graph showing timing slack vs number of paths at worst corner for different FF implementations.

Functional verification was performed with delay back annotated gate level Verilog simulations. All systems were found to be functioning correctly with more than 99% toggle coverage from the testbench. For SEU fault tolerance random fault injection method is used to inject faults in the DFF at random time intervals. With 10000 faults introduced, approximately 15% of actual failures were observed in case of reference DFF based implementation where no hardening was done. Whereas in case of robust solutions no fails were observed. Meaningful SET fault tolerance characterization was found to be difficult to perform due to infinite possible scenarios, hardware limitations and huge simulation effort. For this analysis, the standalone study presented earlier in this section is found to be most relevant.

4.2.8 Summary

A multi-bit DFF system based on spatial and temporal redundancy having embedded timing pre-error detection capability has been presented. The proposed solution is low cost as it does not require any special designing of radiation hardened library cell. The functionality and implementation of the proposed solution was

discussed in detail explaining the tolerance against SEU and SET under various scenarios along with timing pre-error detection. Then the experimental data has been presented based on standalone simulations on flip-flop and through digital circuit implementation in ST 90nm technology. With the help from experimental data, it is demonstrated that the proposed solution has similar penalty in terms of area, power and performance when compared to other high radiation tolerant flip-flops. Also, the tolerance against radiation is in line with existing robust solutions with added advantage of embedded timing pre-error detection which can provide adaptability to digital system to further improve design robustness against other prevalent degradation effects and to improve performance or reduce power consumption. In Chapter 5 silicon implementation results along with radiation test results are provided.

Chapter 5. Silicon Implementation and Test Results

Dedicated test-chips were implemented to study the impact of radiation on silicon and to study the effectiveness of the robust solutions. The test-chips were mainly implemented on ST BCD 90nm technology with CMOS HVT devices. The technology is 5 Metal layer process with junction isolation and deep trench isolation. The electrical tests were performed at the ST lab in Agrate, Italy and radiation tests were carried out at three main locations – 1) Alpha Tests – University of Padova, Italy, 2) Heavy Ion Tests – Legnaro Heavy Ion Accelerator, Italy and 3) Neutron test facility at Didcot, UK. Two test-chips were implemented, one is targeted for studying radiation effects on standard library cells and memory circuits, and the other is targeted for studying radiation effects on digital system. In this chapter design and implementation details, test setup and flow, results and analysis is discussed.

5.1 SERVAL Test-chip Design

The main purpose of this test-chip is to provide first SER radiation immunity assessment for 90nm ST BCD CMOS technology related to Flip-Flops of standard cell libraries and SRAM memory bit cell and to validate the effectiveness of radiation hardening methods. These structures are optimized for low power applications and implemented using high Vt transistors with nominal operating voltage 1.2V. A 8.8umX6.9um silicon area has been dedicated for this purpose.

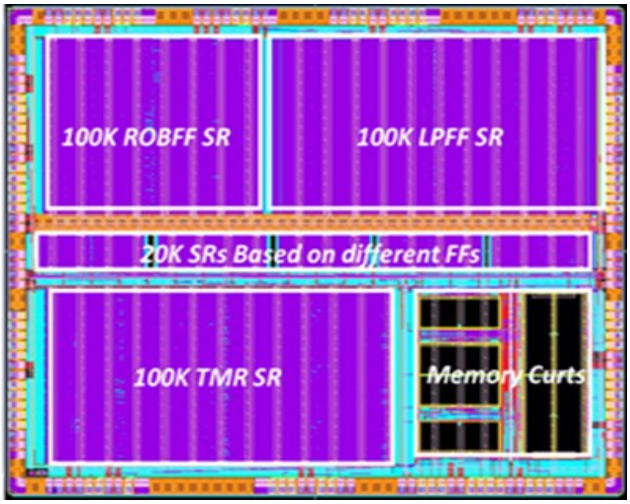


Figure 5-1 SERVAL Test-chip Layout View

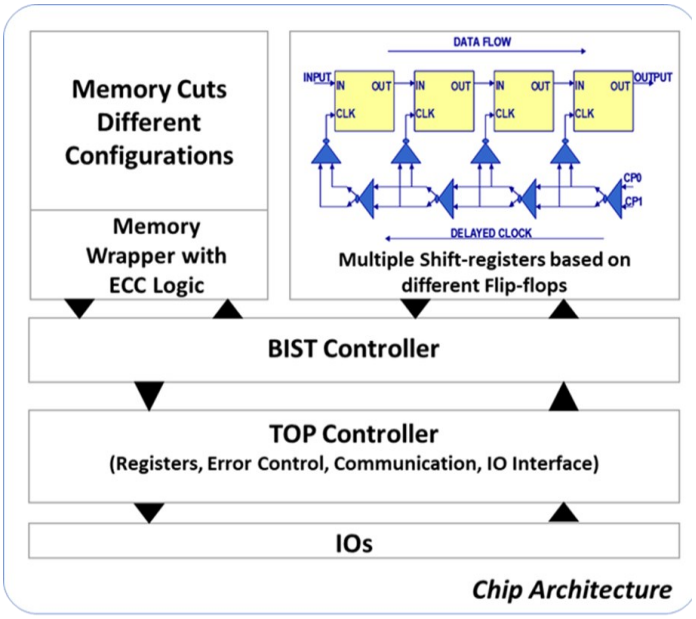


Figure 5-2 SERVAL Test-chip Architecture

The test-chip consists of multiple blocks of shift-registers (SR) based on different flip-flops, multiple SRAM memory instances along with wrapper logic, controllers and glue logic as shown in Figure 5-2. The test-chip controller and glue-

logic are triplicated in TMR configuration to make them immune to radiation strike and this logic can be bypassed as well in order to have direct access to all devices under test (DUTs). Different DUTs selected for SER characterization are given in Table 5-1. The SRAM cut is based on single port 6T SRAM cell, 312Kb in size and eight instances of this cut are placed in different orientations in the test-chip. The MUX configuration is 16 which should avoid multiple bit upset (MBU) in a single word. The memory wrapper consists of single error correction double error detection (SECDED) logic which can be bypassed. 5 different DFF types from standard library offer based on dual phase clocked (Figure 4-11) latches have been used for the SR implementation along with 3 robust DFFs based on the most popular hardening methods DICE (Figure 4-12), TMR (Figure 2-15) and the proposed SPCRC2-DFF (Figure 4-3). These standard flip-flops are the most used flip-flop types in commercial chips and are best suited for analysis. For standard flip-flops, a 20k instance SR and for robust flip-flops, a 100k SR has been implemented in order to speed up test time especially for robust flip-flop tests under neutron beam. The SR has been designed to be able to see the SEU failure sensitivity of flip-flops. To enable this, they are implemented with robust clock, all un-used inputs like reset, scan-enable and scan input tied to inactive state and direct path from output of DFF to D input of DFF with no combinational cell in between. To avoid hold violation clock path is skewed in reverse direction of data flow as shown in Figure 5-2. The test-chip has Built in self-test (BIST) capabilities for both SRAM and SRs. All the test blocks are implemented with deep n-well (DNW) DTI isolation to avoid any single event latch-up (SEL). The design is implemented using standard design flow methods and tools. The test-chip is packaged with CPGA144 with no covering on top to avoid any effect of package material during radiation tests. Another version SERVAL test-chip (SERVAL ver. 2) was implemented with a bug fix on SPCRC2-DFF based SR, rest all structures remain same.

Table 5-1 Memory cut and Flip-flop Description (SERVAL Test-chip)

Index	**Mem cut Name**	**Cut Size**	**# Instances**	**Memory Configuration**
1	Memcut	312Kb	8	Mux 16 Configuration with cuts places in different orientation
index	**FF Type**	**#DFFs (r by c)**	**#DFFs (total)**	**FF Type**
2	RQ	126X160	20160	Reset DFF
3	RQT (DPC-DFF)	126X160	20160	Scan Reset DFF
4	RQ20	126X160	20160	Reset DFF 4x Output Drive
5	RQNT	126X160	20160	Scan Reset DFF with inverted output
6	SQT	126X160	20160	Scan Set DFF
7	ROB (DPCR-DFF)	626x160	100160	Dual clocked DICE based DFF

8	TMR DFF	626X160	100160	TMR based Scan reset DFF
9	LPFF (SPCRC2-DFF)	626X160	100160	Single Phase clocked robust DFF

5.2 LPTCHIP Test-Chip Design

The main objectives of this test-chip are :-

- Radiation impact Analysis on Digital Systems and Evaluation of effectiveness of different radhard structures and methodologies.
- ECC effectiveness on RAM against radiation.
- Aging degradation study on digital system with embedded timing sensors.

Based on different DFFs multiple µCs have been implemented. In these implementations a standard clock tree has been used and storage elements have been changed for different µC blocks. The µC architecture. shown in Figure 4-31 comprises of ARM cortex M4 with some features disabled, RAM, ROM, interface blocks and General Purpose Input Outputs (GPIOs). The code memory ROM stores the software code. There are two GPIO ports one acting as input and another as output, and 32 Kbyte system ram is with smart ECC based on SECDED hamming codes which automatically writes the corrected data back to RAM in case of error event. There is toggle bit corresponding to each ARM implementation, which goes to primary output of the chip. This bit tells the external tester that the ARM is alive and running.

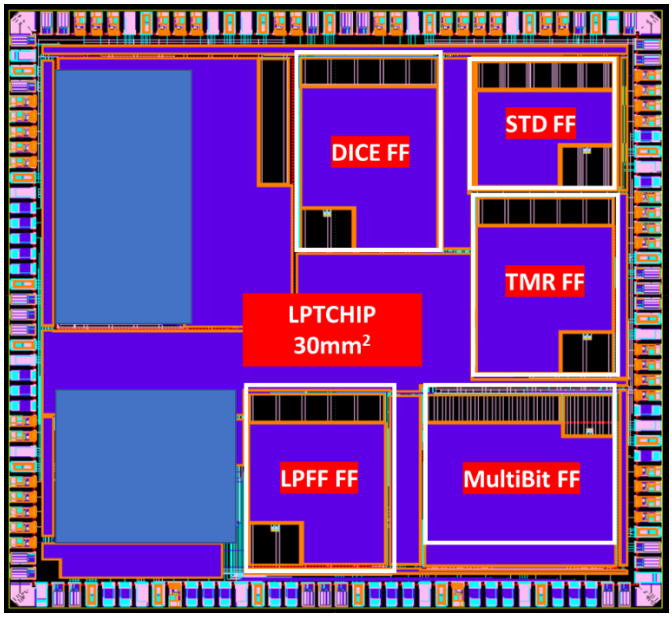


Figure 5-3 LPTCHIP Layout View

The Test-chip consists of Multiple µC variants implemented with different flip-flop types as shown in Table 5-2. In variants with robust DFF all the standard flip-flops

were replaced with hardened flip-flop. In case of multi-bit implementation, the error signal coming from multiple groups of flip-flops is ORed and registered. It comes out of the chip as primary output.

Table 5-2 µC Variants in LPTCHIP

	Variants	Description	Gate Count	Core Area (mm^2)	#DFFs
1	STD-FF Based	Based on DPC-DFF	200k	1.4	4.85k
2	DICE-FF Based	Based on DPCR-DFF	229k	1.78	4.85k
3	TMR-FF Based	Based on TMR DFF	295k	2.01	14.5k
4	LPFF Based (p)	Based on SPCRC2 DFF	234k	1.84	4.85k
5	Multi-Bit FF Based (P)	2-Bit Implementation with single buffer skew and common reset	293k	2.01	12.1k

These implementations are loaded with multiple sets of soft code exciting different paths of the µC. There is possibility to select one of the algorithms only or to run all sequentially. This is done to see the impact of algorithms on radiation tests as different paths are excited. These algorithms are:-

- Matrix Multiplication -> Large Matrix Multiplication Program Memory Intensive
- Bubble Sort -> Sorting algorithm
- Bit count -> Number of Bits Counting
- FIR -> DSP algorithm
- FPU Check -> Floating point arithmetic (CPU intensive)
- QS CHECK -> Sorting algorithm

5.3 Test Setup and Flow

The test-chips are targeted for functional tests, electrical characterization and radiation tests with alpha particles, neutrons and heavy ions. A specific test board was implemented to meet the testing requirement for different radiation sources [60]. For example, in order to fit inside the vacuum chamber for Heavy Ions testing or the isolation chamber for alpha testing, the testing board must be compact and the number of external instruments and cables must be minimized. On the other side for Neutron facilities, only the DUT must be inside the beam, while the rest of testing equipment must be as far as possible from the beam. The testing board as shown in Figure 5-4 is composed of an ST Nucleo Board with STM32 ARM microcontroller [61] that acts as digital tester; Power Down and Power Up sequences are managed directly on board with relays; current consumptions are measured with instrumentation amplifiers on-board in order to avoid external amperemeters. This allows to have no external instruments (apart from the power supplier) and to have just the USB communication with the PC. The Board is divided in two parts as shown in Figure 5-4, the mother board with all the testing capabilities and the daughter board with DUT socket only. Normally the two parts are directly attached through a connector, but in case of neutron testing, the two parts can be detached, and a long cable can be inserted between the connectors. The whole testing algorithm is executed by the STM32 microcontroller, including current consumption acquisitions and power up/down cycles. Test board can be controlled with remote PC during radiation tests.

Figure 5-4 Test Board Image

For LPTCHIP a closed loop test setup was prepared for electrical characterization mainly to demonstrate the automatic voltage and frequency

regulation based on the timing pre-error detection signal coming from the proposed multi-bit DFFs. The closed loop system shown in Figure 5-5 comprises of LPTCHIP on daughter board controlled by ST Nucleo based mother board and a voltage regulator controlling the power supply to the LPTCHIP. The voltage regulator provides precise voltage steps of 1 mV to the LPTCHIP. This enables the automatic voltage regulation scheme based on a timing error signal coming from the chip.

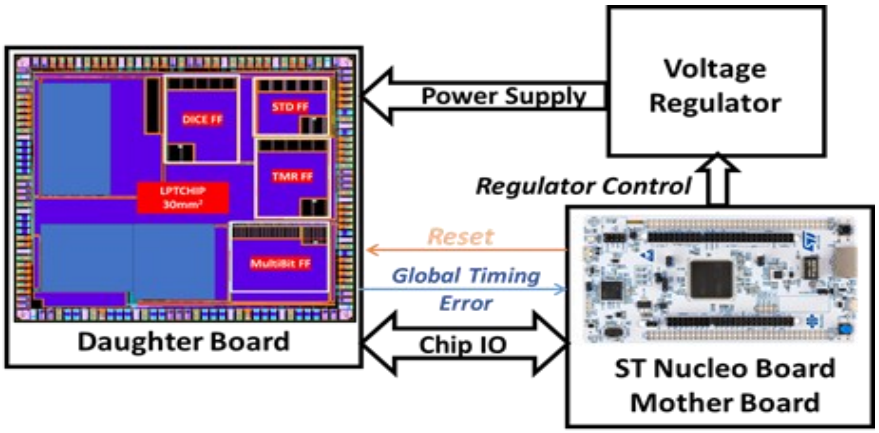


Figure 5-5 LPTCHIP Close loop test setup

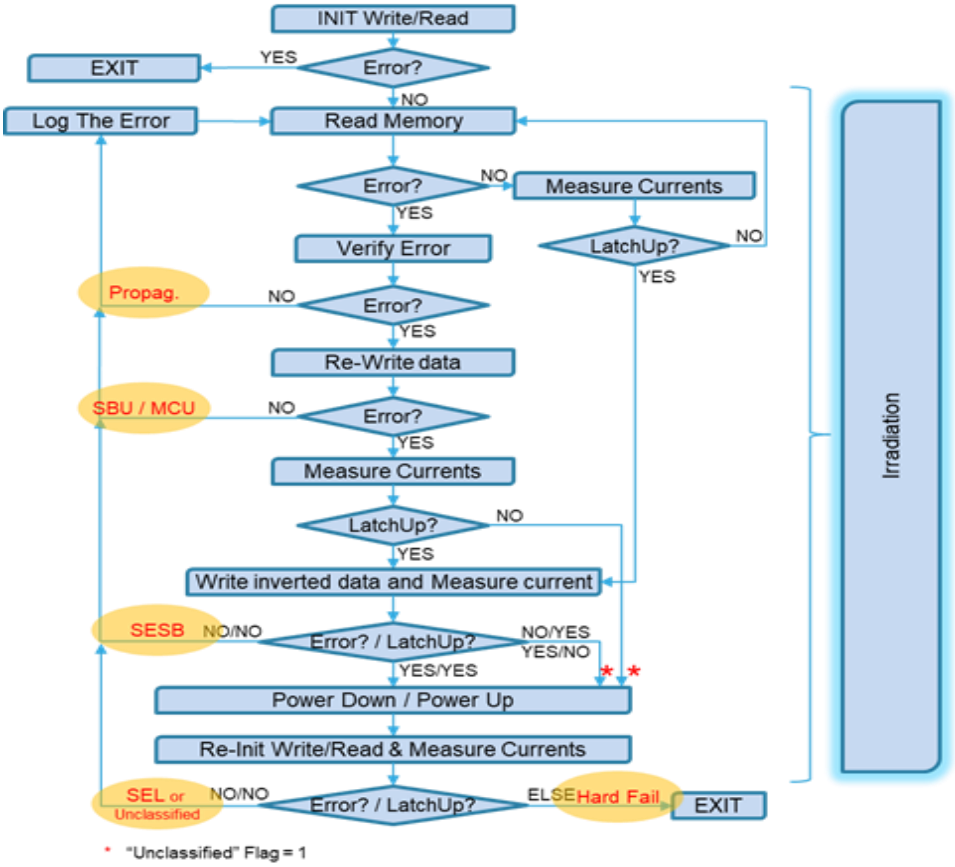


Figure 5-6 Memory Radiation Test Flow

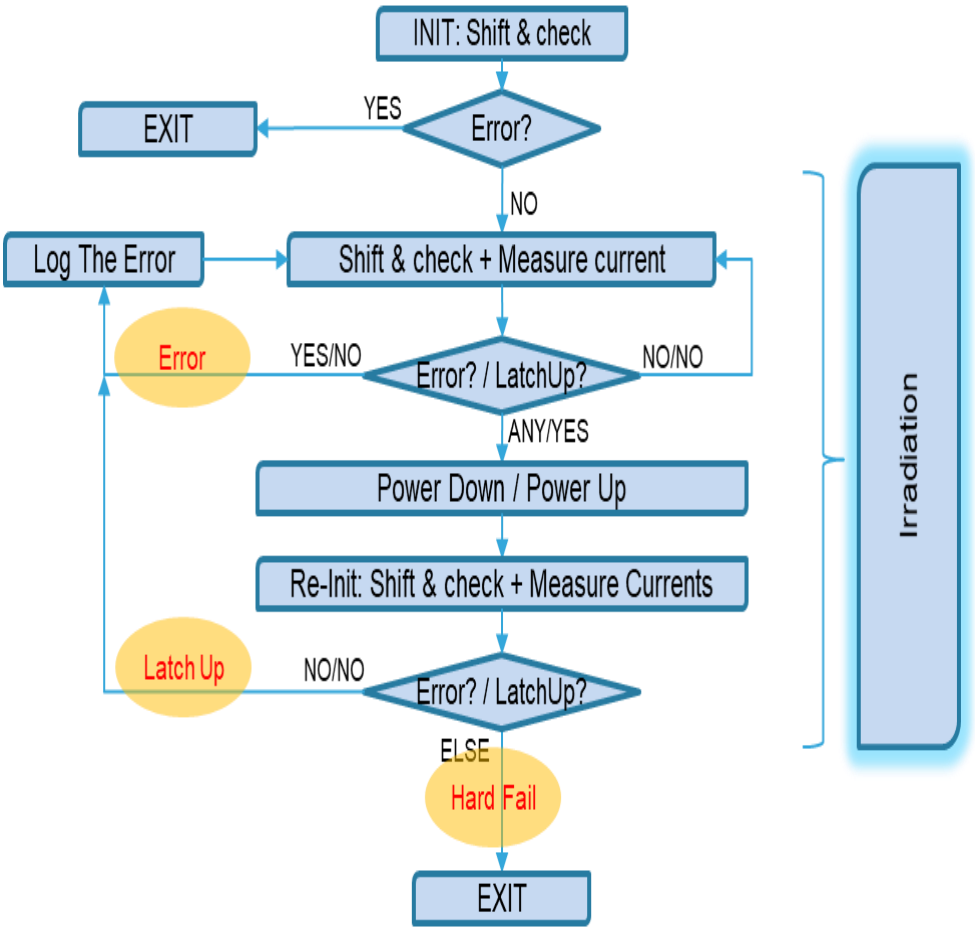


Figure 5-7 DFF Shift Register Test flow

The Test Flow is composed by 2 main actions; first action is purely digital: access to RAM or flipflop writing and reading the data for checking data integrity; second action is purely analog: measure current consumption to monitor Latch Up. The test flow for memory and flip-flop shift-register is shown in Figure 5-6 and Figure 5-7 respectively. The data logs obtained from these procedures are later analyzed to filter irrelevant events such as latch up or burst errors in some cases. For the SERVAL test-chip the BIST circuit loads different patterns into the shift registers and checks the expected outcome with the chip under the beam. The Nucleo based mother board continuously monitors the error signal reported with BIST and downloads the data stream in case an error is reported. For LPTCHIP test-chip similar test-flow is adopted.

5.4 Radiation Tests and Measurements

The test-chips are irradiated with alpha, heavy ions and neutron particles based on standard specification defined in [60] [62]. For Alpha particle tests, a radioactive Americium-241 (^{241}Am) source was used at Dept. of Information Engineering, Padova, Italy. This source can generate alpha particles with energies 5.486 MeV for 85% of the time, 5.443 MeV for 13% of the time, and 5.388 MeV for the remaining 2% as per the alpha decay it undergoes [63]. The test flux is in the range of approximately 17800 - 18200 particles·cm^{-2}·s^{-1}. An arrangement of alpha source with DUT flipped is shown in Figure 5-8. The alpha particles land on test-chip directly at various angles. For FIT rate calculation the ultra low emission flux i.e. 1*10^{-3} particles·cm^{-2}·s^{-1} is used.

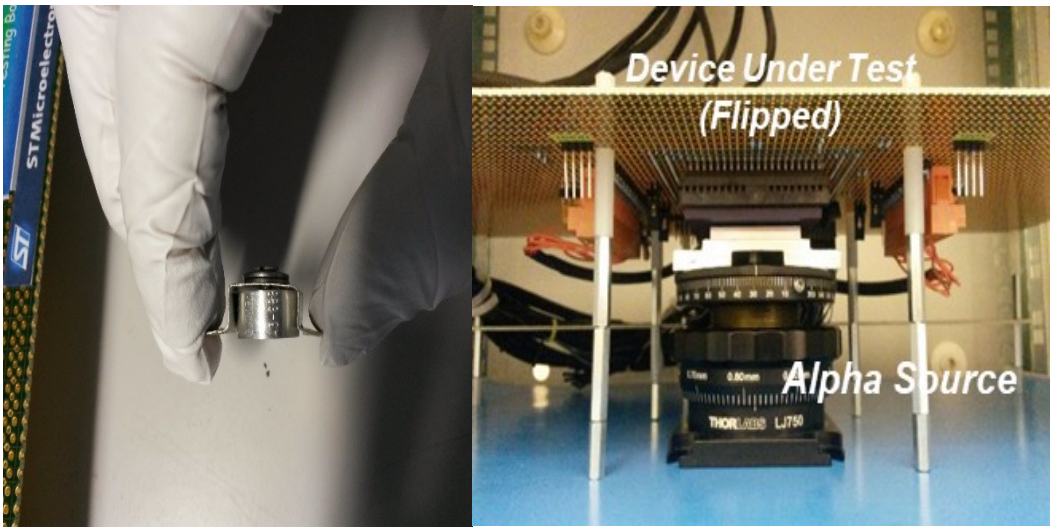


Figure 5-8 Alpha Source and DUT arrangement

Heavy ions tests were carried out at the SIRAD line of the TANDEM accelerator at the Laboratori Nazionali di Legnaro, Padova, Italy using particles (Si, Ni and Ag) with LET ranging from about 3 to 60 MeV·cm^2/mg in order to characterize the threshold LET and the saturation cross section for upsets. The test board placement in the test facility is shown in Figure 5-9. The heavy ions travel through the accelerator and hits the silicon placed in the test board. As explained earlier only the daughter board goes inside the chamber whereas the mother board is placed outside the chamber. Heavy ion cocktail details are given in Table 5-3. The various particles have different flux and the range of flux calculated is given in the table. The same has been used to calculate the cross-section for a particular particle.

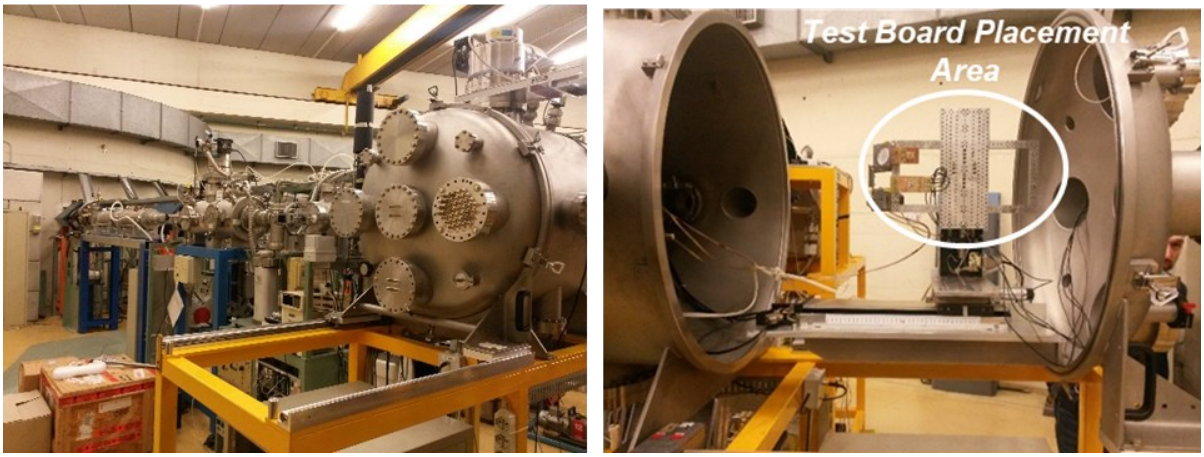


Figure 5-9 Heavy Ion Accelerator Lab and test board placement

Table 5-3 Heavy Ion Particles Details

Particle	LET ($MeVmg^{-1}cm^2$)	Flux Low Range ($particles \cdot cm^{-2} \cdot s^{-1}$)	Flux High Range ($particles \cdot cm^{-2} \cdot s^{-1}$)
Ag	58	3300	3600
Ni	28.4	9500	12500
Si	8	40000	100000

The final Neutrons irradiation were conducted at the ChipIr beam line at the ISIS accelerator of the Rutherford Appleton Laboratories, Didcot, UK. The ChipIr facility features a wide energy neutron spectrum which is very similar to the atmospheric one. The test flux is in the range of approximately $4.5*10^6 – 4.75*10^6$ $particles \cdot cm^{-2} \cdot s^{-1}$. For FIT rate calculation, the natural flux at sea level altitude i.e., 13 $particles \cdot cm^{-2} \cdot s^{-1}$ is used.

There were many issues with availability of labs and the irradiation program due to which all chips could not be tested with all the particles discussed above. A summary of various irradiation campaigns done on different chips is given below in

Table 5-4 Radiation Test Summary of different chips

Test Chip Name	Radiation Test Conducted	Test Specs
SERVAL ver1	Alpha, Heavy Ion and Neutron	Room Temperature, Multiple Bias, 0-10 MHz Clock, Multiple Patterns checker board, All 0, All 1.
SERVAL ver2 (Fix on SPCRC2-DFF SR)	Alpha Only	Room Temperature, Multiple Bias, 0-10 MHz Clock, Multiple Patterns checker board, All 0, All 1.
LPTCHIP	Alpha and Heavy Ion (Ni)	Room Temperature, Multiple Bias, 0-10 MHz Clock, Functional Checks of μC

As discussed in section 2.4.1 the radiation results can be expressed as FIT rate or cross-section area. The heavy ions test results are measured using cross-section which indicates the sensitivity of a bit to a particular particle. The bit cross section [6] is defined as:

$$\sigma = \frac{number\ of\ errors}{fluence\ \cdot number\ of\ bits} \qquad (5.1)$$

and measured in cm^2. The calculated values are plotted as continuous wave using Weibull distribution function [5].

$$\mathrm{XS} = \mathrm{XS_{sat}}\{1 - \exp\left(-\left(\frac{\mathrm{LET}-\mathrm{LET_{th}}}{\mathrm{W}}\right)^{\mathrm{S}}\right)\} \qquad (5.2)$$

Where XS_{sat} is the cross-section at saturation (high LET), LET_{th} is the threshold LET to observe the event, S and W are shape and width fitting parameters respectively.

Further for alpha particle and neutron particle actual FIT rate per mega-bit of cells can be calculated using the natural flux data for these particles. The expression for FIT rate per million cells is given by

$$FIT\_Mb = Natural_{RadFlux} \times \frac{\#errors \times (10^6 \times 10^9)}{Test_{RadFlux} \times TestTime \times \#cells} \qquad (5.3)$$

The Failure in Time (FIT) rate is the number of errors expected in 1Giga hours of device operation. As described above in this section the natural flux for alpha particle is taken as 10^{-3} particles·cm^{-2}·s^{-1} and for neutron it is taken as 13 particles·cm^{-2}·s^{-1}.

5.5 Radiation Test Results on 90nm Standard Library Cells

The shift registers implemented in the SERVAL test-chip (summarized in Table 5-1), were tested according to the flow mentioned in section 5.3 at 10MHz clock frequency. The checkerboard pattern was loaded and unloaded through shifter chain and failures were observed. The burst errors due to clock tree failures are filtered which was only observed with high energy heavy ions. (The abbreviations used in figures are mentioned in Table 5-1). The heavy ion and neutron particle data for SPCRC2-DFF could not be extracted due to unavailability of test facility for SERVAL ver. 2 tests.

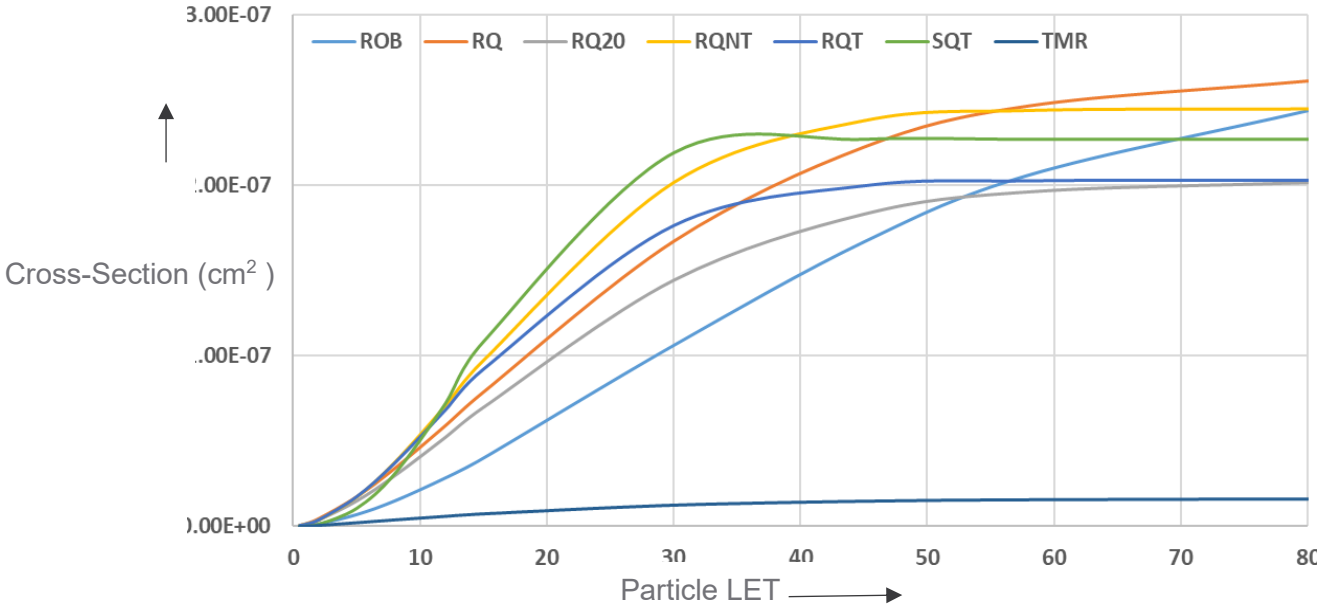


Figure 5-10 Heavy Ions flip-flop cross-section vs particle LET

Figure 5-11 Alphas and Neutron Particle radiation results showing FIT rate at different bias voltage for different flip-flops

The cross-section results computed using equation 5.1 with different heavy ions and fitted as per Weibull distribution curve equation 5.2 is shown in Figure 5-10. The FIT rate data for alpha and neutron particles computed using equation 5.3 is shown in Figure 5-11 for different bias voltage. It was observed that standard flip-flops are sensitive to all particles alpha, neutron and heavy ions. Medium radiation tolerance structure i.e. DICE DFF is found to be resilient against alpha particle and lower LET heavy ion but for neutron and high energy ions it showed high failure rate. The high tolerance structure TMR DFF is found to be resilient across all particle types.

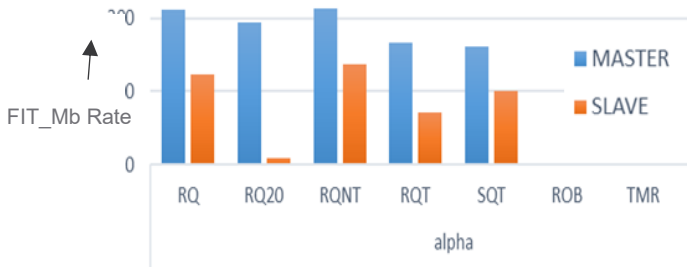


Figure 5-12 Alpha Particle radiation results showing FIT rate for master and slave latch separately

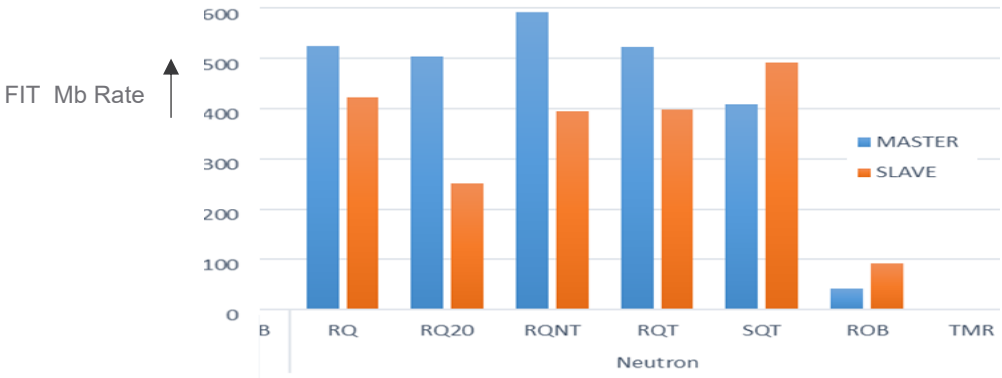


Figure 5-13 Neutron Particle radiation results showing FIT rate for master and slave latch separately

On further analysis among different variants of standard DFF some observations were made. The RQ20 with higher output drive strength was observed to be more robust amongst standard flip-flops and RQNT most sensitive due to a greater number of devices and layout configuration. Figure 5-12 and Figure 5-13 shows the radiation sensitivity for master and slave latch separately for alpha and neutron particles respectively. It was observed that the slave latch is more robust than the master latch because of the presence of the output buffer that increase the capacitance inside the latch. The DFF with bigger output buffer RQ20 shows a much higher robustness The sensitivity gap between master and slave with Neutrons is less than with alpha

because of higher energy of the neutron's induced particles. Figure 5-14 shows the sensitivity with respect to stored value. It was observed that more upsets occur in "0->1" upsets (up-flips) with respect to "1->0" upsets (down-flips). This result is consistent among all shift registers chains for alpha particles except for RQNT flip-flop wherein the output is negated and for neutron particles the sensitivity gap reduces due to the emergence of secondary particles. In SQT higher sensitivity was observed towards storing 0 which is linked with an additional set path present in circuit.

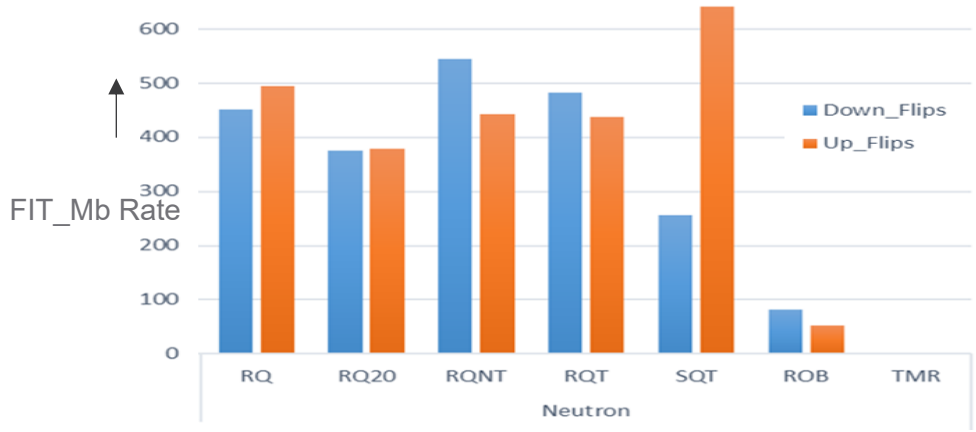


Figure 5-14 Neutron Particle radiation results showing FIT rate for data stored in flip-flop

5.6 Radiation Test Results on 90nm SRAM

SRAM radiation tests are carried out as per the flow mentioned in section 5.3. With ECC protection on no failures have been observed therefore all tests are carried out bypassing the ECC logic. The cross section was calculated using equation 5.1 with heavy ion irradiation with particle characteristics mentioned in section 5.4. The data obtained is being fit and extrapolated according to the Weibull distribution equation 5.2. The results are shown in Figure 5-15. The results are in line with experimental data available in literature.

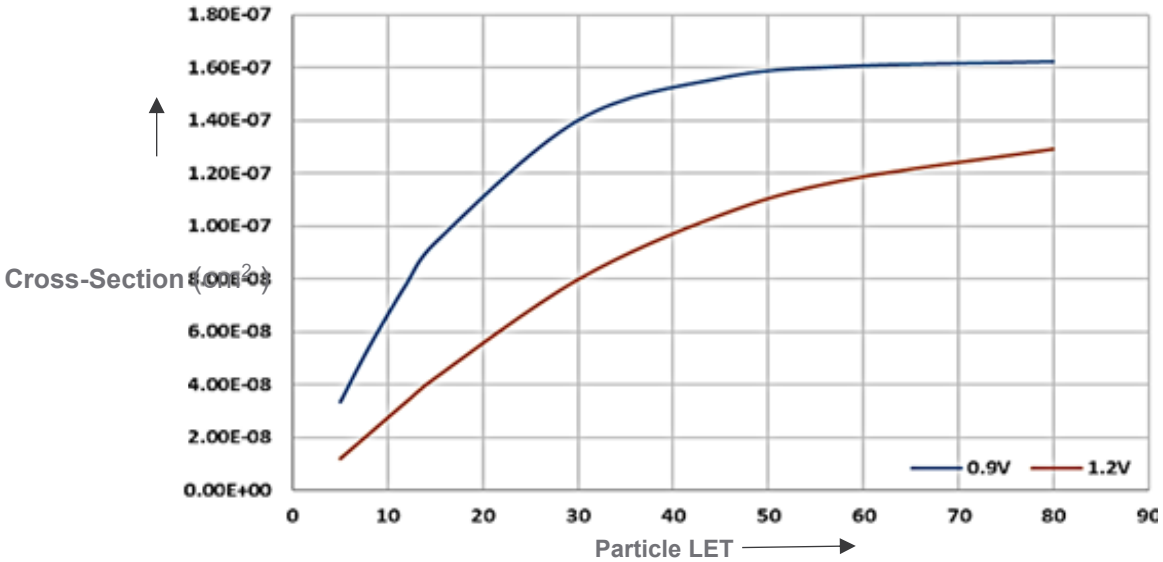


Figure 5-15 Heavy Ion Cross Section vs LET of SRAM at different bias voltage

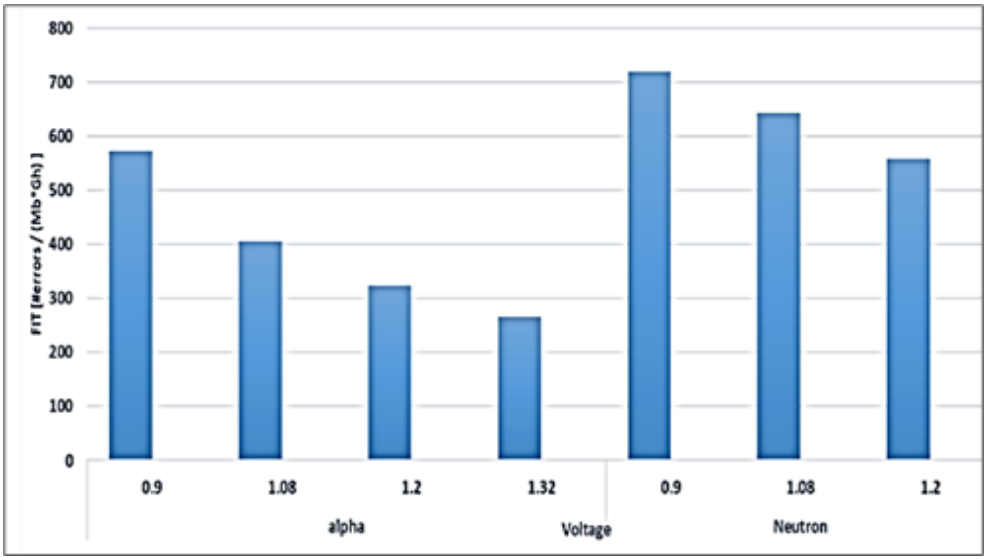


Figure 5-16 Alpha and Neutron FIT rate SRAM at different bias voltage

The FIT rate with alpha and neutron particles calculated using equation 5.3 at different bias voltages is shown in Figure 5-16. Significant drop in failures were observed with increasing bias voltage.

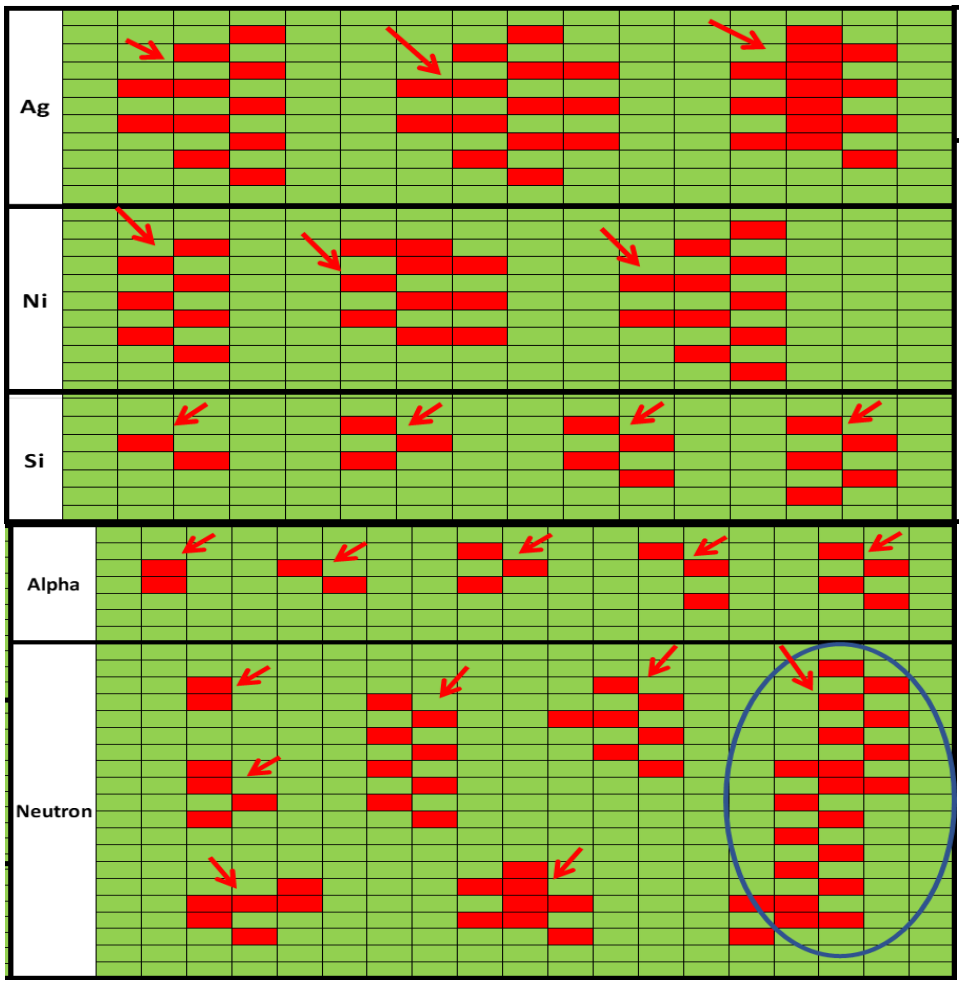


Figure 5-17 Radiation strike bit map on memory array (in red color affected cells)

The bit map image for memory cuts showing location of faults has been made to understand the multiple cell upsets. The bitmap showing the failing cells in red is shown in Figure 5-17. For alpha radiation, 2-4 multiple cell upsets (MCU) are observed whereas for neutron and heavy ions 2 to 21 bit fails were observed. Similarly with heavy ions more MCUs were observed with high energy particles. However, no MBUs were observed with any of the particles. This is mainly due to memory bit interleaving and mux configuration. It was observed that the maximum adjacent bit fails in a single row was less than 4 bits. Therefore, it was concluded that MUX4 configuration coupled with SECDEC ECC protection can protect the memory against soft errors in this technology node.

5.7 SPCRC2-DFF Silicon Results and Analysis

Electrical and radiation tests were carried out on SPCRC2-DFF based SR and µC present on the SERVAL and LPTCHIP respectively. There was a bug identified in the clock tree structure used for SPCRC2-DFF based SR, due to which it cannot be tested successfully in SERVAL version 1. Later version 2 was planned for the same chip wherein alpha radiation test were conducted on the SR. The electrical characterization was performed on both SERVAL ver. 2 and the LPTCHIP in ST lab. Both chips were found to give functionally correct output. Both test-chips were functioning correctly down to 0.9V. Each µC implemented on the LPTCHIP has dedicated power supply on-chip so independent power measurements were possible with the test-chip. Power numbers were extracted from electrical characterization of different µCs at 75MHz clock frequency for different bias voltages. The results are shown in Figure 5-18. The data obtained is normalized with respect to reference DPC-DFF and the mean value of multiple samples is plotted here. The results clearly demonstrate that the SPCRC2-DFF has lesser power dissipation with respect to DPCR-DFF and TMR-DFF based µC. It is 10% higher with respect to standard DFF and 10% lower with respect to DICE based DPCR-DFF. This is mainly attributed to the use of single-phase clocking inside the proposed design.

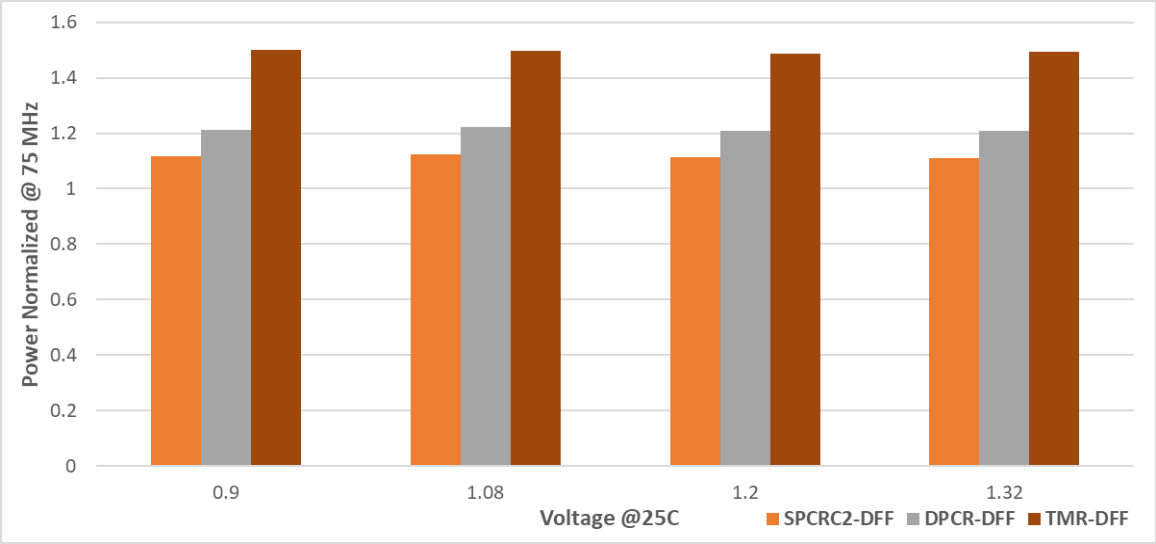


Figure 5-18 Power Consumption of µCs @ 75MHz at room temperature

Radiation test characterization on SERVAL ver. 2 was performed in a similar way as for other SR described in section 5.5. However, only alpha particle irradiation can be performed in this chip due to unavailability of the test facility for Heavy ions and

neutrons particles. The results for alpha particles are shown in Figure 5-19. The proposed SPCRC2-DFF showed good resilience with respect to alpha particles which is inline with the expected behavior from hardened structures.

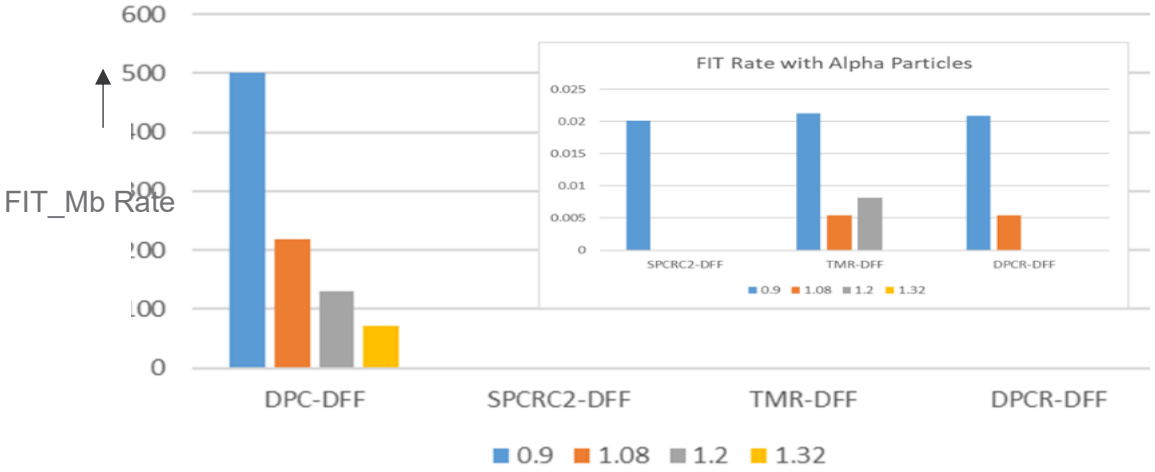
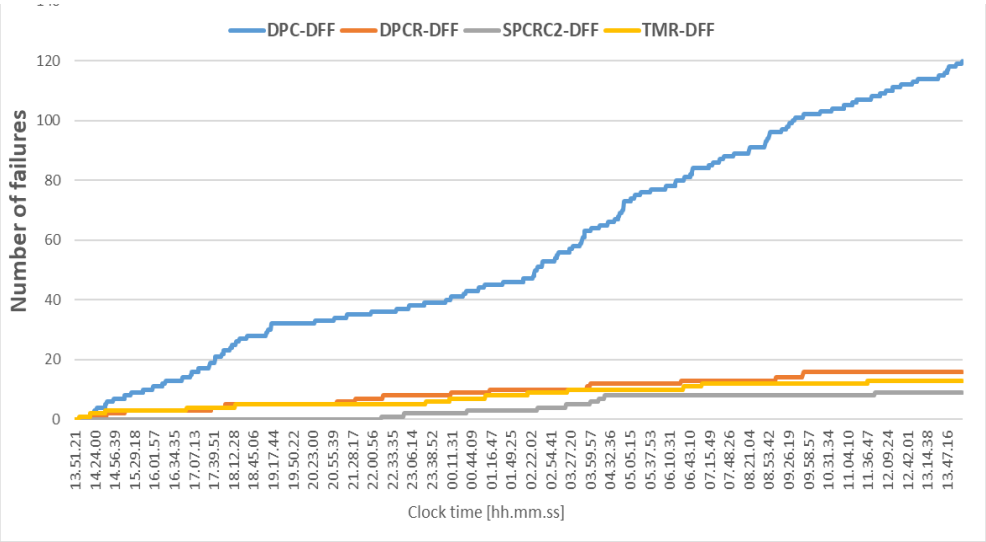


Figure 5-19 SPCRC2-DFF FIT rate comparison on Alpha-particle strike at different bias voltages

The radiation tests are again carried out on the LPTCHIP with the alpha source with the same setup used for the SERVAL test-chip earlier. The µCs are made to operate in parallel at room temperature and output signals are observed through the nucleo board. In case of data error or nonresponsive µC, error count is incremented and µCs are reset and started again. The operation is carried out at lower voltage (0.9V) to get maximum faults and at two different clock frequencies (1MHz and 54MHz). The FIT rate calculated is tabulated in Table 5-5. It is observed that at lower frequency, faults are less with respect to higher frequency. This signifies that SET faults are non-dominant in µC at lower frequency. On comparing the data with the SR data obtained it is clearly visible that most of the SEUs arising in µCs are masked by the logic and software. This is also illustrated in [32] wherein alpha particle results on digital circuits at different clock frequency is presented. At higher frequency (54MHz), detailed failure analysis with time was performed. The results are shown in \Figure 5-20. At higher frequency rate the increase in faults is arising due to SET faults being captured by the flip-flops and accumulation of errors in flip-flops.

Table 5-5 FIT_Mb rate on Alpha Particle irradiation on different DFF based µC showing SPCRC2-DFF comparative analysis

	DPC-DFF	**DPCR FF**	**TMR FF**	**SPCRC2-DFF**
1MHz	28.3	0.9	0.6	0.6
54MHz	31.6	6	4.9	6



\Figure 5-20 Number of faults due to alpha radiation in µC with time @ 54MHz for SPCRC2-DFF Comparative Analysis

Further, irradiation tests carried out with Ni heavy ion on multiple µC structures. The tests were performed at 0.9V room temperature only at 54MHz. The tests could be conducted only for a short duration due to the unavailability of the accelerator. But the results (\Figure 5-20) extracted clearly demonstrates the improved tolerance with SPCRC2-DFF. The cross-section calculated is tabulated in Table 5-6. Comparing the heavy ion cross-section number obtained from SR with cross-section number obtained on µC, the effect of logical and software masking of errors is evident.

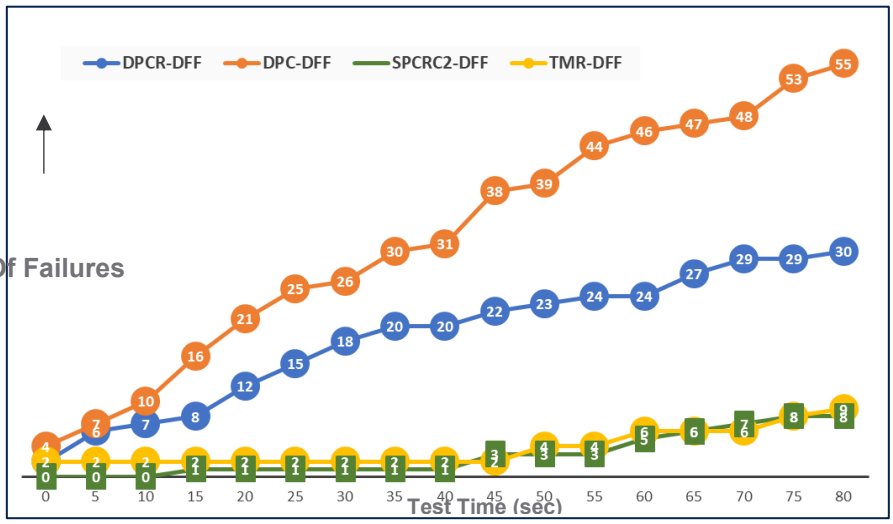


Figure 5-21 Nickel Ion radiation results showing number of fails reported with test time at 0.9 V and room temperature for SPCRC2-DFF Comparative Analysis

Table 5-6 Cross-section value for different µCs for Ni Ion. SPCRC2-DFF comparative Study

DPC-DFF	DPCR-DFF	SPCRC2-DFF	TMR-DFF
1.146E-08	6.25E-09	1.67E-09	1.87E-09

5.8 Multi-Bit DFF Silicon Results and Analysis

As described above, multiple packaged samples of the LPTCHIP test-chip have been characterized electrically and under radiation. CPGA144 package with no covering on top is used to avoid any effect of package material during radiation tests. The electrical characterization was performed in the ST lab in Agrate, Italy. The maximum frequency of multi-bit µC operation at various voltages and temperature points was measured based on actual hard faults where the device gives incorrect responses and based on global timing error signal. The data is plotted for multiple samples and shown in Figure 5-22. It is observed that the error signal coming from the timing sensor always flags error before actual failures in design. The timing error margin window at the system level can also be computed with the help of the graph. In a typical corner (1.2 V and 25°C), it comes out to be around 350 ps.

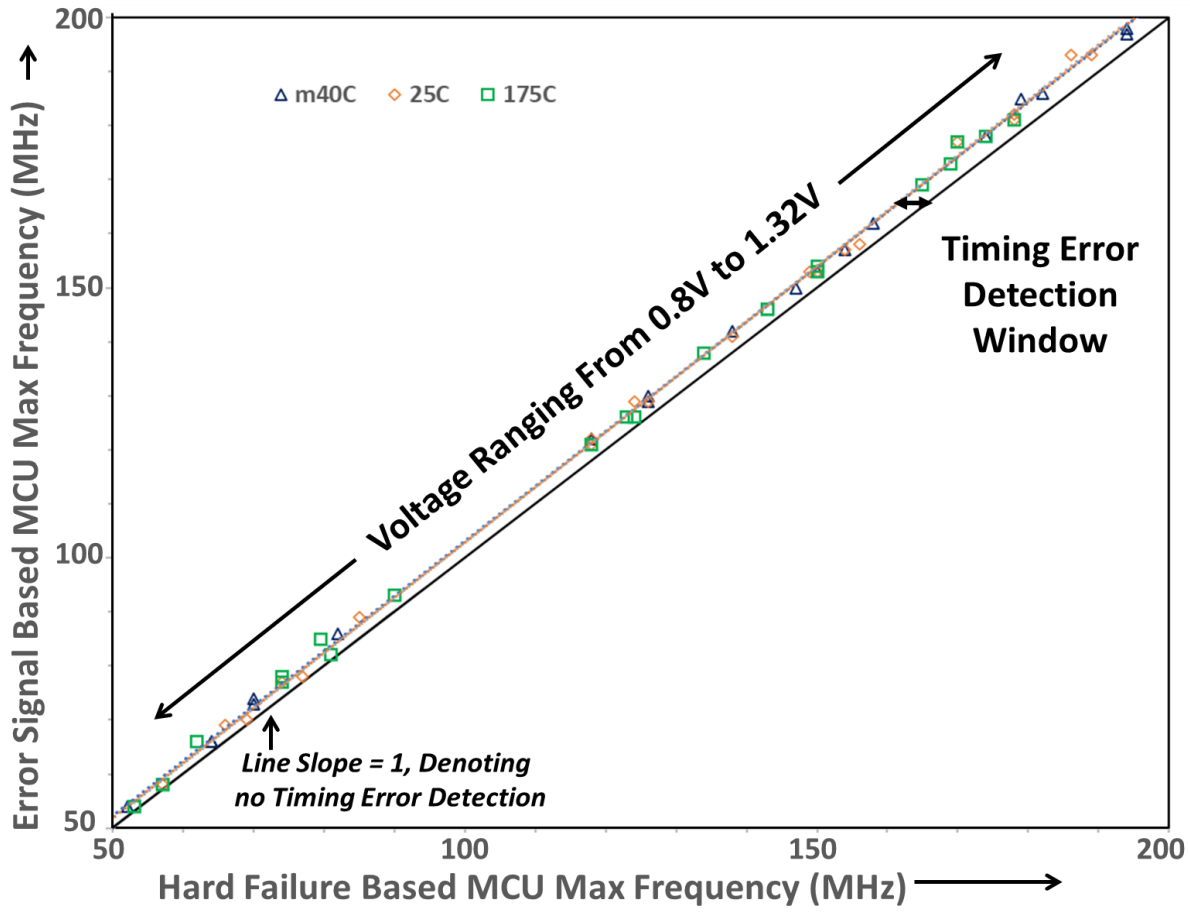


Figure 5-22 Max Frequency Data of Multi-bit DFF based µC across multiple bias voltage and temperature.

In Figure 5-23 percentage differences of dynamic power with respect to reference DPC-DFF are plotted at room temperature and 1.2 V operating voltage for various frequencies. It is noted that the usage of hardened DFF increases the consumption by 13% for SPCRC2-DFF, 22% for dice based DPCR-DFF and by 50% for both TMR and the proposed multibit FF. With automatic voltage regulation application in multi-bit µC, power consumption can be brought down to 12% gain with respect to DPC-DFF µC. The multi-bit µC can operate at 0.91 V for a frequency target of 75 MHz as we move at higher performance operating points, the gain in power reduction reduces. We reach the limit of lowering supply voltage at 0.8 V wherein memory minimum operating supply voltage is hit, and supply voltage cannot be scaled down further. Therefore, power gain becomes constant at lower operating frequencies. Similar regulation cycle can be performed with frequency as well. Wherein for a target voltage the clock frequency can be scaled up or down depending on the feedback. The step size of regulation for both supply voltage and clock frequency should be set at the minimum value possible.

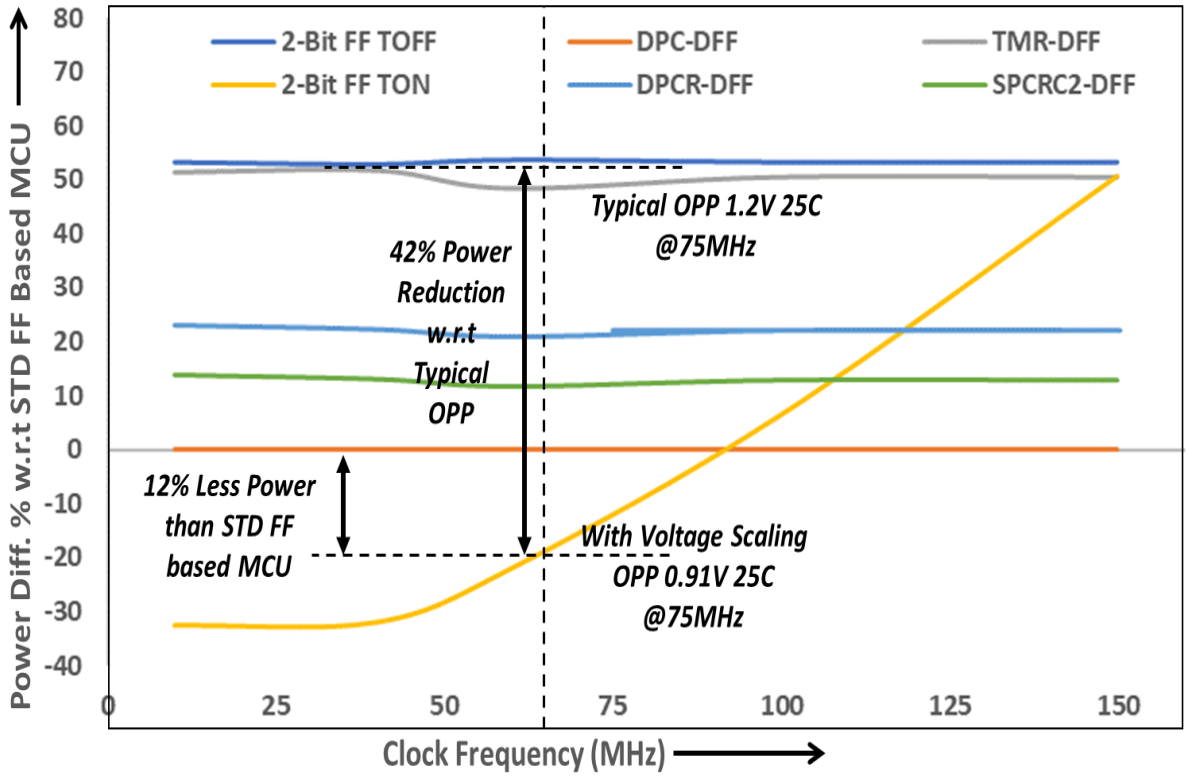


Figure 5-23 Power Consumption at 1.2V room temperature for different µCs at different clock frequencies.

Thermal stress tests were also performed on the multi-bit µC. With timing pre-error detection, the multi-bit flip-flop should flag an error before actual fail. The thermal stress was applied in 2 cycles. In cycle 1, the device was made to operate at a supply of 1.32V and temperature of 150°C for 10Hours. In cycle 2, the same device was operated at 1.45V and 175°C for 10Hours. After each cycle, the maximum operating frequency of clock is characterized for the multi-bit based µC. The results shown in Figure 5-24 wherein maximum operating frequency at which actual fails occur and at which timing error is asserted is plotted after each thermal cycle with respect to original maximum frequency of the design. The data shows 2-3% degradation on the first thermal stress cycle and 5-7% degradation on the second. It is observed that the timing pre-error signal always gets asserted before actual fail in design. Even with varied device degradations going into various paths of the design, the embedded timing sensing capability managed work effectively and warn the system about possible failures.

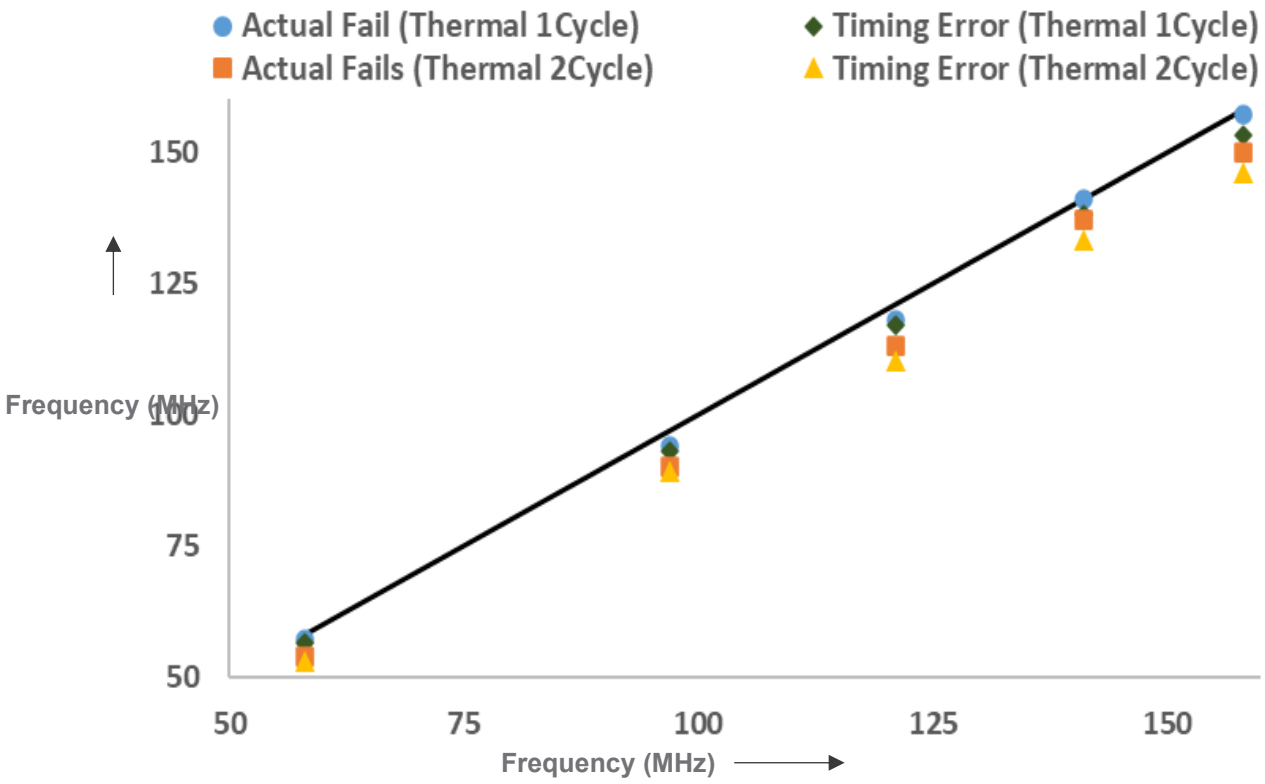


Figure 5-24 Thermal Stress Max Frequency Data of Multi-bit DFF based µC across multiple bias voltage and temperature

Radiation tests setup and flow used on the LPTCHIP is already described in section 5.7. The FIT rate data and number of fails with time against alpha particles are

shown in Table 5-7 and Figure 5-25 respectively. The data is in line with robust solutions and the proposed multibit showed good resilience with respect to alpha particles. However, few faults arising due to SET events and error accumulation are also present in the proposed Multibit solution as the version on silicon was based on 2-Bit even parity scheme with 1 buffer clock skew and common reset. By clock skew tuning and using SET filtering techniques on clock and reset paths as mentioned in section 4.2.3, SET can be avoided. Error accumulation due to multiple event upsets can be avoided by modified software which provides refresh cycles to the system on assertion of error as illustrated in section 4.2.5. This is not possible with other robust solutions based on voting mechanism because they can do error correction only and not error detection.

Table 5-7 FIT_Mb rate on Alpha Particle irradiation on different DFF based µC showing proposed MultiBit-DFF comparative analysis

	DPC-DFF	DPCR-DFF	SPCRC2-DFF	TMR DFF	Multibit DFF
1MHz	28.3	0.9	0.6	0.6	1
54MHz	31.6	6	6	4.9	5.3

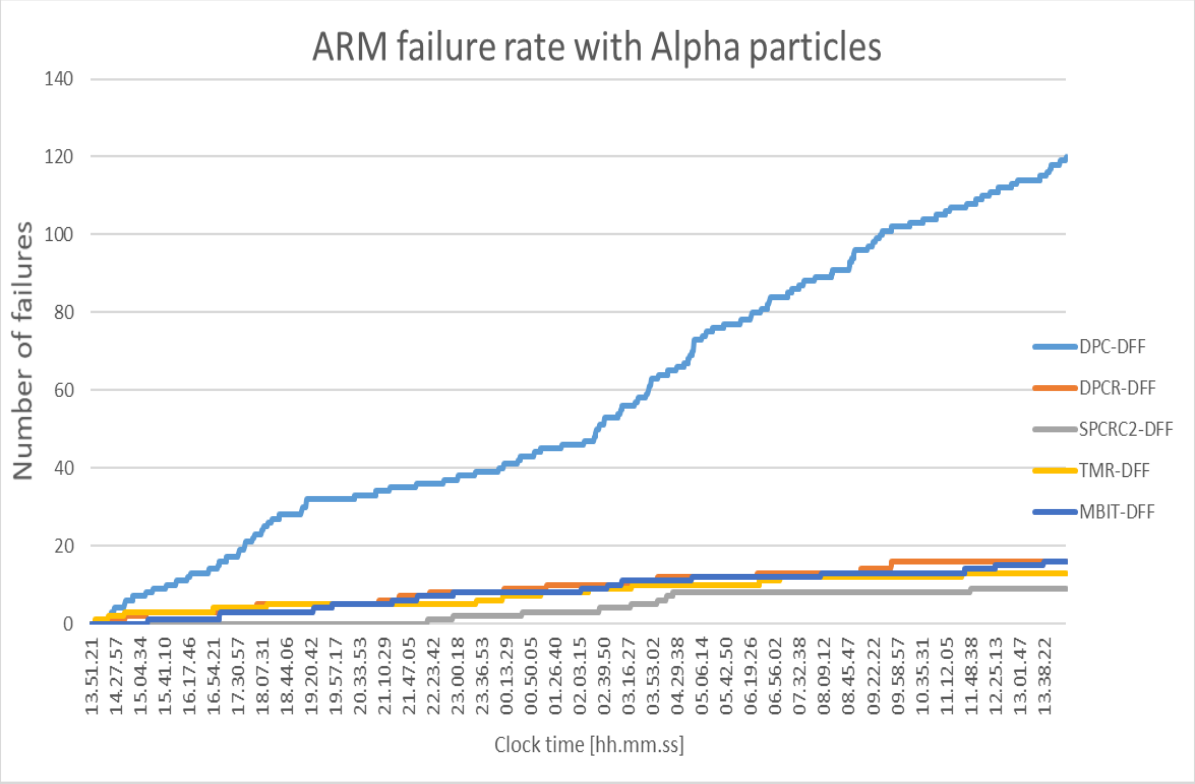


Figure 5-25 Number of faults due to alpha radiation in µC with time @ 54MHz for MultiBit-DFF Comparative Analysis

Further, for Ni Ions (having 28.4 LET as shown in Table 5-3) radiation test results are shown in Table 5-8 and Figure 5-26. This heavy ion test shows the effectiveness of multi-bit system at higher LET. Very few fails were observed during the test which are attributed to SET faults and multiple event upsets.

Table 5-8 Cross-section value for different µCs for Ni Ion. MultiBit-DFF comparative Study

DPC-DFF	DPCR-DFF	SPCRC2-DFF	TMR-DFF	MBIT FF
1.14566E-08	6.25E-09	1.67E-09	1.87E-09	8.33E-10

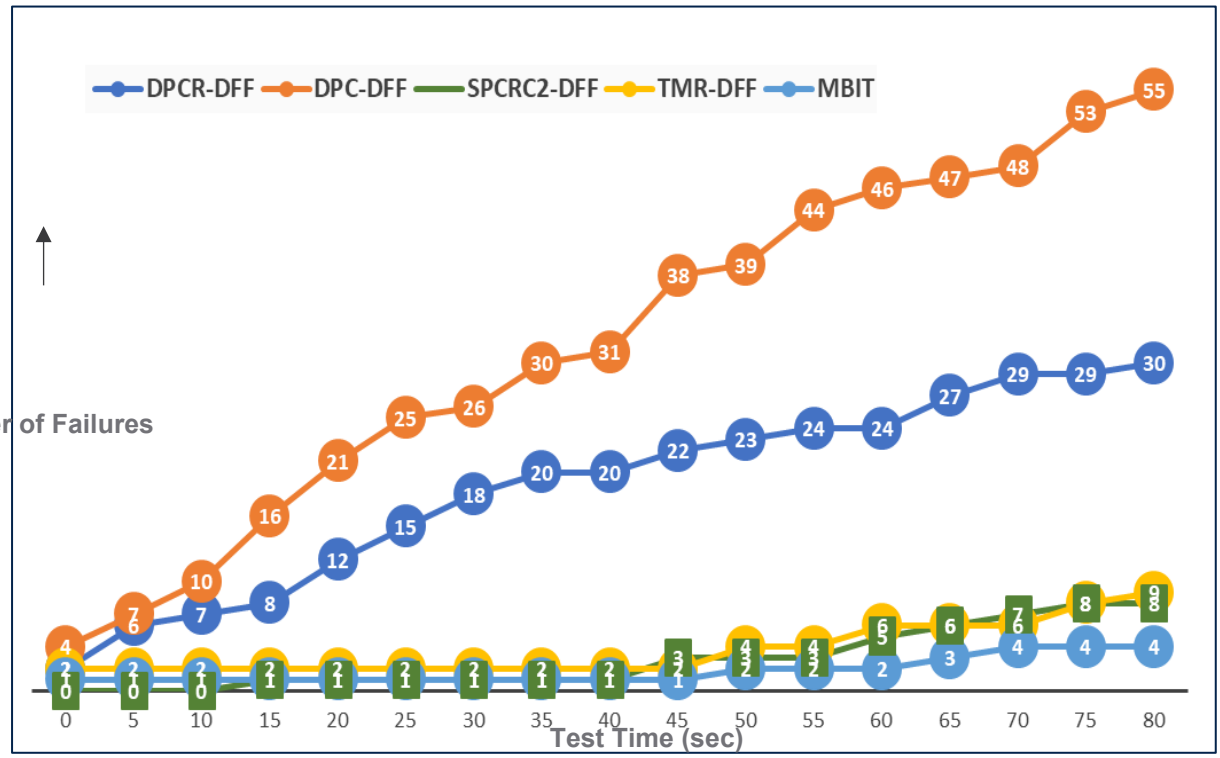


Figure 5-26 Nickel Ion radiation results showing number of fails reported with test time at 0.9 V and room temperature for SPCRC2-DFF Comparative Analysis

5.9 Summary

Two test-chips were implemented to study the impact of radiation on the ST 90nm library flip-flops and SRAM cut. One of the chips is based on shift registers implemented with thousands of flip-flops and memory cuts, the other one is based on digital microcontroller implementations with different flip-flop variants. The test-chips were implemented with state-of-the-art solutions DICE and TMR along with proposed solutions. These were tested, first electrically in the ST lab and radiation tests were carried out at different facilities. The SERVAL chip was irradiated with alpha, neutron and heavy ions whereas the LPTCHIP was irradiated with alpha particles and Ni Heavy Ion only. The electrical characterization and radiation qualification results were extracted from the test-chips through a dedicated test setup. The radiation test results show good alignment with measurement data present in literature for standard library cells and memory cuts. The microcontrollers were tested at different clock frequency and at higher frequency, they show a greater number of fails due to SET dominance which is also on the expected lines. Also, logical error masking is evident from the microcontroller results as the number of fails reported with microcontrollers are much lower with respect to the fails observed in the shift-registers. Both the proposed solutions were found to be working correctly on silicon and results obtained are very well aligned with what was expected from simulations results. The proposed SPCRC2-DFF is found to have improved tolerance (~4X with Ni Heavy Ion) and lesser power dissipation (~12% in Microcontroller) compared to the DICE cell based DPCR-DFF. Also, it is proven on silicon, the proposed multi-bit DFF solution and methodology is tolerant to radiation even for higher LETs and the embedded timing sensing capability which comes for free in terms of area is able to detect timing pre-errors in the system across different PVT corners and on thermal stress as well. With application of voltage regulation on the microcontroller implemented with the multi-bit solution, the power dissipation is reduced by ~40% with respect to TMR and multi-bit flop-flop typical operating point and 12% lower with respect to standard flip-flop. Both the proposed solutions showed good efficiency enhancement and radiation tolerance compared to existing solutions.

Chapter 6. Conclusions

This thesis work explores the radiation induced single event effects on digital circuits and various hardening methods used for making digital circuits tolerant to radiation. Following conclusions can be drawn based on this work.

Radiation induced single event effects are prominent in electronics systems even at terrestrial level not limited to space. Radiation induced SETs and SEUs are the main constituents of soft errors which can occur at any time during the device lifecycle, making the system deviate from the expected behavior or even fail. However, certain failure rates could be tolerated by some applications, but they could be catastrophic for critical applications like medical, automotive, aviation etc. There is a need to assess radiation effects on technology and to have radiation tolerant designs.

Various RHBD methods were explored for flip-flop circuits. There is a definite trade-off between level of radiation tolerance achieved and size, power and speed of the circuit. The higher level of tolerance incurs more penalties. Moreover, at lower feature sizes multiple node charge sharing mechanism makes some of the hardening techniques ineffective. The need for efficient radiation hardened circuits is strongly present. Two new solutions were presented in this work.

The radiation effects assessment on flip-flops and SRAM implemented with ST 90nm BCD technology low power CMOS devices was performed through dedicated test structures and radiation tests. The test results were in line with measurement data reported in literature on similar technology feature size. The trends in failure rate with voltage and frequency are also in line with failure rate decreasing with increasing supply voltages and failure rate increasing with clock frequency due to SET dominance. Radiation hardened flip-flop circuits were found to provide good tolerance against low energy alpha particles with negligible fails. However, significant fails were observed with neutron particles and high energy Heavy Ions in medium tolerant design DICE cell-based flip-flops which showed the effect of multiple node upsets. To avoid multiple node upsets, LEAP methodology can be adopted while layout implementation of such circuits but that results in heavy area penalties. At higher energy, the TMR flip-flop with physical spacing between flip-flops showed good resilience. For SRAM, SECDED was found to work effectively and cross-section without error correction is aligned to reported data.

A novel radiation hardened circuit based on single phase clocked latch and spatial redundancy (SPCRC2-DFF) is presented. CAD results showed that the proposed circuit has improved tolerance and lesser power dissipation with respect to conventional robust structures. This has been proven with silicon results as well. The proposed solution was tested in dedicated shift-register configuration as well as on a practical digital system. In microcontroller implementation, the power consumption is ~10% lower with respect DPCR-DFF and radiation tests with Ni heavy ion shows 4X lower sensitive cross-section. This is largely due to single phase clock operation, differential data input scheme and c-element based latch structure. However, there is a penalty in terms of silicon area and timing performance. Also, it is prone to multiple node upsets which is very prominent at lower technology nodes. Therefore, it is not a scalable solution for lower technology nodes. It could be targeted for specific applications requiring medium range tolerance and better power efficiency.

A Multi-bit FF system has been presented, which can be adopted in any digital system with standard library cells and standard digital design flow. The functionality and design constraints required for the proposed system have been explained in detail. Through architectural explanations and experimental data, it has been shown that the proposed flip-flop has high tolerance against both SEU and SET. Further, the effectiveness of timing pre-error sensing has been demonstrated, which helps in efficient voltage and frequency regulation. Area overhead due to redundant logic is lower with respect to standard robust solution TMR, delta-TMR, etc. Overall, the proposed system offers both radiation robustness and adaptability, a combination of which is missing in conventional robust architectures. Application developers can exploit this peculiarity to make resilient and efficient digital systems. The microcontroller implementation showed ~40% reduction in power dissipation with voltage regulation done based on timing pre-error detection. It is ~10% lower with respect to standard flip-flop.

References

[1] ""“Radiation,” Def. 1a. Webster’s Encyclopedic Unabridged Dictionary of the English Language," 1995.

[2] S. Kerns, B. Shafer, L. Rockett, J. Pridmore, D. Berndt, N. v. Vonno and F. Barber, "The design of radiation-hardened ICs for space: a compendium of approaches," *Proceedings of the IEEE,* vol. 76, no. 11, 1988.

[3] M. Bagatin and S. Gerardin, Ionizing Radiation Effects in Electronics, CRC Press, 2015.

[4] C. M. Hsieh, P. C. Murley and R. R. O'Brien, "Dynamics of Charge Collection from Alpha-Particle Tracks in Integrated Circuits," in *19th International Reliability Physics Symposium*, 1981.

[5] P. Paillet, "Overview of the main concepts of radiation effects and their evolution over the 30 years of RADECS conferences," Short Course at RADECS 2019.

[6] D. Kobayashi, "Basics of SEE Mechanisms and Predictions," IEEE NSREC Short Course Notebook, 2019.

[7] J. Barth, C. Dyer and E. Stassinopoulos, "Space, atmospheric, and terrestrial radiation environments," *IEEE Transactions on Nuclear Science,* vol. 50, no. 3, 2003.

[8] E. Stassinopoulos and J. Raymond, "The space radiation environment for electronics," *Proceedings of the IEEE,* vol. 76, no. 11, 1988.

[9] "Borophosphosilicate glass," Wikipedia, [Online]. Available: https://en.wikipedia.org/wiki/Borophosphosilicate_glass. [Accessed October 2021].

[10] B. Narsimham, "Hardening Techniques for Digital Circuits," in *IEEE NSREC short course Notebook*, 2021.

[11] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Transactions on Device and Materials Reliability,* vol. 5, pp. 305-316, 2005.

[12] S. Buchner and M. Baze, "Single-event transients in fast electronic circuits," in *Proc. IEEE Nuclear and Space Radiation Effects Conf. Short Course Text*, IEEE, 2001.

[13] S. Jagannathan, T. D. Loveless, B. L. Bhuva, N. J. Gaspard, N. Mahatme, T. Assis, S.-J. Wen, R. Wong and L. W. Massengill, "Frequency Dependence of Alpha-Particle Induced Soft Error Rates of Flip-Flops in 40-nm CMOS Technology," *IEEE Transactions on Nuclear Science,* vol. 59, pp. 2796-2802, 2012.

[14] F. Sexton, "Destructive single-event effects in semiconductor devices and ICs," *IEEE Transactions on Nuclear Science,* vol. 50, no. 3, 2003.

[15] A. Javanainen, "SEE TESTING WITH BROAD AND FOCUSED PARTICLE BEAMS," in *IEEE NSREC Short Course Notebook*, 2019.

[16] P. Roche, G. Gasiot, J. L. Autran, D. Munteanu, R. A. Reed and R. A. Weller, "Application of the TIARA Radiation Transport Tool to Single Event Effects Simulation," *IEEE Transactions on Nuclear Science,* vol. 61, no. 3, 2014.

[17] J. S. Kauppila, A. L. Sternberg, M. L. Alles, A. M. Francis, J. Holmes, O. A. Amusan and L. W. Massengill, "A bias-dependent single-event compact model implemented into BSIM4 and a 90 nm CMOS process design kit," *IEEE Transactions on nuclear Science,* vol. 56, p. 3152–3157, 2009.

[18] K. M. Chavali, "Mitigation of Soft Error Rate using Design, Process and Material Improvements," in *2019 IEEE International Integrated Reliability Workshop (IIRW)*, 2019.

[19] M. Nicolaidis, "Design for soft error mitigation," *IEEE Transactions on Device and Materials Reliability,* vol. 5, pp. 405-418, 2005.

[20] I. Chatterjee, S. Jagannathan, D. Loveless, B. L. Bhuva, S.-J. Wen, R. Wong and M. Sachdev, "Impact of well contacts on the single event response of radiation-hardened 40-nm flip-flops," in *2012 IEEE International Reliability Physics Symposium (IRPS)*, 2012.

[21] M. Nicolaidis, "A low-cost single-event latchup mitigation scheme," in *12th IEEE International On-Line Testing Symposium (IOLTS'06)*, 2006, p. 5.

[22] J. Chen, S. Chen, Y. He, J. Qin, B. Liang, B. Liu and P. Huang, "Novel Layout Technique for Single-Event Transient Mitigation Using Dummy Transistor," *IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY,* vol. 13, no. 1, pp. 177-182, MARCH 2013.

[23] H.-H. K. Lee, L. Klas, B. Mounaim, R. Prasanthi, I. R. Linscott, U. S. Inan and M. Subhasish, "LEAP: Layout Design through Error-Aware Transistor Positioning for soft-error resilient sequential cell design," in *2010 IEEE International Reliability Physics Symposium*, 2010.

[24] D. G. Mavis and P. H. Eaton, "Soft error rate mitigation techniques for modern microcircuits," in *2002 IEEE International Reliability Physics Symposium. Proceedings. 40th Annual (Cat. No.02CH37320)*, 2002.

[25] D. Bull, S. Das, K. Shivashankar, G. S. Dasika, K. Flautner and D. Blaauw, "A Power-Efficient 32 bit ARM Processor Using Timing-Error Detection and Correction for Transient-Error Tolerance and Adaptation to PVT Variation," *IEEE Journal of Solid-State Circuits,* vol. 46, pp. 18-31, 2011.

[26] D. Bull, S. Das, K. Shivashankar, G. S. Dasika, K. Flautner and D. Blaauw, "Correction to “A Power-Efficient 32 bit ARM Processor Using Timing-Error Detection and Correction for Transient-Error Tolerance and Adaptation to PVT Variation”," *IEEE Journal of Solid-State Circuits,* vol. 46, pp. 705-705, 2011.

[27] H.-H. K. Lee, K. Lilja, M. Bounasser, I. Linscott and U. Inan, "Design Framework for Soft-Error-Resilient Sequential Cells," *IEEE Transactions on Nuclear Science,* vol. 58, no. 6, 2011.

[28] B. Narasimham, K. Chandrasekharan, Z. Liu, J. K. Wang, G. Djaja, N. J. Gaspard, J. S. Kauppila and B. L. Bhuva, "A Hysteresis-Based D-Flip-Flop Design in 28 nm CMOS for Improved SER Hardness at Low Performance Overhead," *IEEE Transactions on Nuclear Science,* vol. 59, pp. 2847-2851, 2012.

[29] M. Glorieux, S. Clerc, G. Gasiot, J.-L. Autran and P. Roche, "New D-Flip-Flop Design in 65 nm CMOS for Improved SEU and Low Power Overhead at System Level," *IEEE Transactions on Nuclear Science,* vol. 60, no. 6, 2013.

[30] B. Narasimham, K. Chandrasekharan, J. K. Wang, K. Ni, B. L. Bhuva and R. D. Schrimpf, "Charge-Steering Latch Design in 16 nm FinFET Technology for Improved Soft Error Hardness," *IEEE Transactions on Nuclear Science,* vol. 64, pp. 353-358, 2017.

[31] T. Calin, M. Nicolaidis and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Transactions on Nuclear Science,* vol. 43, pp. 2874-2878, 1996.

[32] S. Jagannathan, T. D. Loveless, B. L. Bhuva, S.-J. Wen, R. Wong, M. Sachdev, D. Rennie and L. W. Massengill, "Single-Event Tolerant Flip-Flop Design in 40-nm Bulk CMOS Technology," *IEEE Transactions on Nuclear Science,* vol. 58, pp. 3033-3037, 2011.

[33] Y.-Q. Li, H.-B. Wang, R. Liu, L. Chen, I. Nofal, S.-T. Shi, A.-L. He, G. Guo, S. H. Baeg, S.-J. Wen, R. Wong, M. Chen and Q. Wu, "A Quatro-Based 65-nm Flip-Flop Circuit for Soft-Error Resilience," *IEEE Transactions on Nuclear Science,* vol. 64, pp. 1554-1561, 2017.

[34] S. Mitra, M. Zhang, N. Seifert, T. Mak and K. S. Kim, "Soft Error Resilient System Design through Error Correction," in *2006 IFIP International Conference on Very Large Scale Integration*, 2006, pp. 332-337.

[35] S. Gupta and J. Mekie, "Soft Error Resilient and Energy Efficient Dual Modular TSPC Flip-Flop," *2019 32nd International Conference on VLSI Design and 2019 18th International Conference on Embedded Systems (VLSID),* 2019.

[36] I. A. Danilov, M. S. Gorbunov and A. A. Antonov, "SET Tolerance of 65 nm CMOS Majority Voters: A Comparative Study," *IEEE Transactions on Nuclear Science,* vol. 61, no. 4, 2014.

[37] O. Schrape, M. Andjelković, A. Breitenreiter, S. Zeidler, A. Balashov and M. Krstić, "Design and Evaluation of Radiation-Hardened Standard Cell Flip-Flops," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 68, pp. 4796-4809, 2021.

[38] C. Ramamurthy, A. Gujja, V. Vashishtha, S. Chellappa and L. T. Clark, "Muller C-element Self-corrected Triple Modular Redundant Logic with Multithreading

and Low Power Modes," *2017 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS),* 2017.

[39] C.-L. Chen and M. Hsiao, "Error-correcting codes for semiconductor memory applications: A state-of-the-art review," *IBM Journal of Research and development,* vol. 28, no. 2, pp. 124-134, 1984.

[40] Y. Cui and X. Zhang, "Research and implemention of interleaving grouping Hamming code algorithm," *2013 IEEE International Conference on Signal Processing, Communication and Computing (ICSPCC 2013),* 2013.

[41] J. Li, P. Reviriego, L. Xiao, C. Argyrides and J. Li, "Extending 3-bit burst error-correction codes with quadruple adjacent error correction," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 26, no. 2, pp. 221-229, 2017.

[42] V. Huard, F. Cacho, F. Giner, M. Saliva, A. Benhassain, D. Patel, N. Torres, S. Naudet, A. Jain and C. Parthasarathy, "Adaptive wearout management with in-situ aging monitors," in *2014 IEEE International Reliability Physics Symposium*, 2014.

[43] S. Das, D. Roberts, S. Lee, S. Pant, D. Blaauw, T. Austin, K. Flautner and T. Mudge, "A self-tuning DVS processor using delay-error detection and correction," *IEEE Journal of Solid-State Circuits}, title={A self-tuning DVS processor using delay-error detection and correction,* vol. 41, no. 4, pp. 792-804, 2006.

[44] S. Das, C. Tokunaga, S. Pant, W.-H. Ma, S. Kalaiselvan, K. Lai, D. M. Bull and D. T. Blaauw, "RazorII: In Situ Error Detection and Correction for PVT and SER Tolerance," *IEEE Journal of Solid-State Circuits,* vol. 44, pp. 32-48, 2009.

[45] Y. Zhang, M. Khayatzadeh, K. Yang, M. Saligane, N. Pinckney, M. Alioto, D. Blaauw and D. Sylvester, "iRazor: Current-Based Error Detection and Correction Scheme for PVT Variation in 40-nm ARM Cortex-R4 Processor," *IEEE Journal of Solid-State Circuits,* vol. 53, pp. 619-631, 2018.

[46] A. Benhassain, F. Cacho, V. Huard, S. Mhira, L. Anghel, C. Parthasarathy, A. Jain and A. Sivadasan, "Robustness of timing in-situ monitors for AVS management," in *2016 IEEE International Reliability Physics Symposium (IRPS)*, 2016.

[47] A. Benhassain, F. Cacho, V. Huard, M. Saliva, L. Anghel, C. Parthasarathy, A. Jain and F. Giner, "Timing in-situ monitors: Implementation strategy and applications results," in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, 2015.

[48] T. Sato and Y. Kunitake, "A Simple Flip-Flop Circuit for Typical-Case Designs for DFM," in *8th International Symposium on Quality Electronic Design (ISQED'07)*, 2007.

[49] M. Saliva, F. Cacho, V. Huard, X. Federspiel, D. Angot, A. Benhassain, A. Bravaix and L. Anghel, "Digital circuits reliability with in-situ monitors in 28nm fully depleted SOI," in *2015 Design, Automation Test in Europe Conference Exhibition (DATE)*, 2015.

[50] J. Yuan and C. Svensson, "New single-clock CMOS latches and flipflops with improved speed and power savings," *IEEE Journal of Solid-State Circuits,* vol. 32, p. 62–69, 1997.

[51] A. Jain, A. Gupta, S. Garg, A. Veggetti, A. Castelnovo, D. Crippa, S. Gerardin, M. Bagatin and C. Cazzaniga, "A low cost robust radiation hardened flip-flop circuit," in *TENCON 2017-2017 IEEE Region 10 Conference*, 2017.

[52] S. M. Jahinuzzaman and R. Islam, "TSPC-DICE: A single phase clock high performance SEU hardened flip-flop," in *2010 53rd IEEE International Midwest Symposium on Circuits and Systems*, 2010.

[53] K. Lilja, M. Bounasser, S.-J. Wen, R. Wong, J. Holst, N. Gaspard, S. Jagannathan, D. Loveless and B. Bhuva, "Single-Event Performance and Layout Optimization of Flip-Flops in a 28-nm Bulk Technology," *IEEE Transactions on Nuclear Science,* vol. 60, pp. 2782-2788, 2013.

[54] V. Petrovic and M. Krstic, "Design flow for radhard TMR Flip-Flops," in *2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems*, 2015.

[55] C. Ramamurthy, S. Chellappa and L. T. Clark, "Physical Design Methodologies for Soft Error Mitigation Using Redundancy," in *2015 15th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, 2015.

[56] H.-B. Wang, N. Mahatme, L. Chen, M. Newton, Y.-Q. Li, R. Liu, M. Chen, B. L. Bhuva, K. Lilja, S.-J. Wen, R. Wong, R. Fung and S. Baeg, "Single-Event Transient Sensitivity Evaluation of Clock Networks at 28-nm CMOS Technology," *IEEE Transactions on Nuclear Science,* vol. 63, pp. 385-391, 2016.

[57] D. L. Hansen, E. J. Miller, A. Kleinosowski, K. Kohnen, A. Le, D. Wong, K. Amador, M. Baze, D. DeSalvo, M. Dooley, K. Gerst, B. Hughlock, B. Jeppson, R. D. Jobe, D. Nardi, I. Ojalvo, B. Rasmussen, D. Sunderland, J. Truong, M. Yoo and E. Zayas, "Clock, Flip-Flop, and Combinatorial Logic Contributions to the SEU Cross Section in 90 nm ASIC Technology," *IEEE Transactions on Nuclear Science,* vol. 56, pp. 3542-3550, 2009.

[58] S. Chellappa, L. T. Clark and K. E. Holbert, "A 90-nm Radiation Hardened Clock Spine," *IEEE Transactions on Nuclear Science,* vol. 59, pp. 1020-1026, 2012.

[59] A. Balasubramanian, B. L. Bhuva, J. D. Black and L. W. Massengill, "RHBD techniques for mitigating effects of single-event hits using guard-gates," *IEEE Transactions on Nuclear Science,* vol. 52, pp. 2531-2535, 2005.

[60] "Single Event Effects Test Method and Guidelines," in *European Space Agency, ESA/SCC Basic Specification No.22900*, 1995.

[61] "STM32 Nucleo board 144 product documentation," [Online]. Available: https://www.st.com/resource/en/user_manual/dm00368330-stm32-nucleo144-boards-mb1312-stmicroelectronics.pdf. [Accessed January 2020].

[62] "ESCC Basic Specification 25100," [Online]. Available: https://escies.org/download/webDocumentFile?id=62690. [Accessed January 2020].

[63] "Americium-241," [Online]. Available: https://en.wikipedia.org/wiki/Americium-241. [Accessed December 2021].

[64] A. Sivadasan, R. J. Shah, V. Huard, F. Cacho and L. Anghel, "NBTI aged cell rejuvenation with back biasing and resulting critical path reordering for digital circuits in 28nm FDSOI," in *2018 Design, Automation Test in Europe Conference Exhibition (DATE)*, 2018.

[65] O. Schrape, A. Breitenreiter, C. Schulze, S. Zeidler and M. Krstić, "Radiation-Hardness-by-Design Latch-based Triple Modular Redundancy Flip-Flops," in *2021 IEEE 12th Latin America Symposium on Circuits and System (LASCAS)*, 2021.

[66] O. Schrape, A. Breitenreiter, S. Zeidler and M. Krstic, "Aspects on Timing Modeling of Radiation-Hardness by Design Standard Cell-Based △TMR Flip-Flops," in *2019 22nd Euromicro Conference on Digital System Design (DSD)*, 2019.

[67] R. Reis, C. Meinhardt, A. L. Zimpeck, L. H. Brendler and L. Moraes, "Circuit Level Design Methods to Mitigate Soft Errors," in *2020 IEEE Latin-American Test Symposium (LATS)*, 2020.

[68] L. W. Massengill, B. L. Bhuva, W. T. Holman, M. L. Alles and T. D. Loveless, "Technology scaling and soft error reliability," in *2012 IEEE International Reliability Physics Symposium (IRPS)*, 2012.

[69] N. N. Mahatme, N. J. Gaspard, T. Assis, S. Jagannathan, I. Chatterjee, T. D. Loveless, B. L. Bhuva, L. W. Massengill, S. J. Wen and R. Wong, "Impact of technology scaling on the combinational logic soft error rate," in *2014 IEEE International Reliability Physics Symposium*, 2014.

[70] Y. Lin, M. Zwolinski and B. Halak, "A low-cost radiation hardened flip-flop," in *2014 Design, Automation Test in Europe Conference Exhibition (DATE)*, 2014.

[71] M. Li, B. Cao, F. Lai and N. Zhang, "Design and Verification of Radiation Hardened Scanning D Flip-Flop," in *2020 IEEE 3rd International Conference on Electronics Technology (ICET)*, 2020.

[72] J. Li and J. Draper, "Joint Soft-Error-Rate (SER) Estimation for Combinational Logic and Sequential Elements," in *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2016.

[73] S. Kumar, S. Chellappa and L. T. Clark, "Temporal pulse-clocked multi-bit flip-flop mitigating SET and SEU," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015.

[74] A. Jain, A. M. Veggetti, D. Crippa, A. Benfante, S. Gerardin and M. Bagatin, "Radiation Tolerant Multi-Bit Flip-Flop System With Embedded Timing Pre-Error Sensing," *IEEE Journal of Solid-State Circuits,* pp. 1-13, 2022.

[75] A. Jain, A. Veggetti, D. Crippa, A. Benfante, S. Gerardin and M. Bagatin, "Single Phase Clock Based Radiation Tolerant D Flip-flop Circuit," in *2020 IEEE 26th International Symposium on On-Line Testing and Robust System Design (IOLTS)*, 2020.

[76] T. Heijmen, "Soft error rates in deep-submicron CMOS technologies," in *12th IEEE International On-Line Testing Symposium (IOLTS'06)*, 2006.

[77] A. Hasanbegović and S. Aunet, "Heavy Ion Characterization of Temporal-, Dual- and Triple Redundant Flip-Flops Across a Wide Supply Voltage Range in a 65 nm Bulk CMOS Process," *IEEE Transactions on Nuclear Science,* vol. 63, pp. 2962-2970, 2016.

[78] A. Hasanbegovic and S. Aunet, "Supply Voltage Dependency on the Single Event Upset Susceptibility of Temporal Dual-Feedback Flip-Flops in a 90 nm Bulk CMOS Process," *IEEE Transactions on Nuclear Science,* vol. 62, pp. 1888-1897, 2015.

[79] R. Dash, R. Garg, S. P. Khatri and G. Choi, "SEU hardened clock regeneration circuits," in *2009 10th International Symposium on Quality Electronic Design*, 2009.

[80] H.-M. Chou, M.-Y. Hsiao, Y.-C. Chen, K.-H. Yang, J. Tsao, C.-L. Lung, S.-C. Chang, W.-B. Jone and T.-F. Chen, "Soft-Error-Tolerant Design Methodology for Balancing Performance, Power, and Reliability," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 23, pp. 1628-1639, 2015.

[81] A. Chavan, E. MacDonald, J. Neff and E. Bozeman, "Radiation hardened Flip-Flop design for super and sub threshold voltage operation," in *2011 Aerospace Conference*, 2011.

[82] D. R. Blum and J. G. Delgado-Frias, "Delay and Energy Analysis of SEU and SET-Tolerant Pipeline Latches and Flip-Flops," *IEEE Transactions on Nuclear Science,* vol. 56, pp. 1618-1628, 2009.

[83] F. S. Alghareb, M. Lin and R. F. DeMara, "Soft Error Effect Tolerant Temporal Self-Voting Checkers: Energy vs. Resilience Tradeoffs," in *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2016.

[84] J. D. Black, P. E. Dodd and K. M. Warren, "Physics of Multiple-Node Charge Collection and Impacts on Single-Event Characterization and Soft Error Rate Prediction," *IEEE Transactions on Nuclear Science,* vol. 60, no. 3, 2013.

[85] P. Paillet, "Overview of the main concepts of radiation effects and their evolution over the 30 years of RADECS conferences," in *Short Course Notes RADECS*, 2019.

[86] J. Black, A. Sternberg, M. Alles, A. Witulski, B. Bhuva, L. Massengill, J. Benedetto, M. Baze, J. Wert and M. Hubert, "HBD layout isolation techniques for multiple node charge collection," *IEEE Transactions on Nuclear Science,* vol. 52, no. 6, 2005.

[87] J. Maiz, S. Hareland, K. Zhang and P. Armstrong, "Characterization of multi-bit soft error events in advanced SRAMs," *IEEE International Electron Devices Meeting 2003,* pp. 21-25, 2003.