UNIVERSITY OF PADOVA

DOCTORAL THESIS

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# Analysis and Design of High-Performance Low-Power IoT Transmitters, and Ultra-Low-Noise Millimetre-Wave Oscillators in CMOS Technology

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During these three years I have had the opportunity to work with many excellent people who have supported and helped me on this journey of personal and technical growth. With their help I realised that a good engineer is much more than a good technician.

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# *Abstract*

Integrated electronics are the backbone of the technological progress we enjoy every day. Without chips, there would be no modern telecommunications or computing, no internet, computers, smartphones, AI and so on. The whole world is more dependent than ever on the successful development of newer, faster and more efficient electronic circuits, especially in the radio frequency (RF) segment. The focus of this work is twofold: on the one hand, the exponential increase in the number of connected devices is driving the development of increasingly complex, efficient and cheap low-power front-ends; on the other hand, the introduction of faster communication protocols, such as 6G, the rise of automotive RADARs, calls for the development of high-performance, low-noise integrated oscillators.

After a brief introduction, the first part of the thesis focuses on the design of a low power, efficient 2.4 GHz Cartesian transmitter for Internet-of-Things (IoT) applications. Firstly, a thorough analysis of the passive resistive mixer is carried out, showing how its operation leads to inefficient transmitters. A passive reactive mixer is proposed as a solution to the shortcomings of the common passive resistive mixer. The proposed mixer is analysed and a set of useful design equations is obtained. The prototypes of the IoT Cartesian transmitter are realised in a 22 nm FD-SOI process and show an efficiency of 22% for a 16-QAM 2.4 Mbaud signal with an average output power of 2.7 dBm.

The second part of the thesis focuses on the design of low phase noise oscillators. Achieving ultra-low phase noise in ultra-scaled CMOS technologies is no easy task due to low supply voltages and low quality of the passive devices. Three different topologies are designs are proposed as an alternative solution. First, a reconfigurable octacore DCO exploits the synchronisation of the oscillators to improve the phase noise by 9 dB; the reconfigurable network allows to dynamically trade phase noise with power consumption. The impact of the switches on the phase noise and coupling bandwidth is evaluated using a rigorous time-variant analysis. The prototypes are realised in a 28 nm CMOS process, and show a phase noise of -126 dBc/Hz at 1 MHz offset at 10.7 GHz. Secondly, a series CMOS VCO with a transformer based feedback network is presented: series VCO are able to achieve much better phase noise by a factor of $20\log Q$ where Q is the quality factor of the tank. Finally, a 5 GHz VCO with a stacked differential-pair is presented. The stacking of the active devices allow the VCO to operate from a 1.6 V supply without reliability concerns. The prototypes, realised in a 22 nm FD-SOI CMOS technology and achieve a phase noise of -126 dBc/Hz at 1 MHz offset at 5.2 GHz and a tuning range of 16.6%.

# Introduction

Our modern world relies on fast communications and smart devices that simplify our daily lives in ways that would have been impossible just a few decades ago. Lightning-fast 5G mobile internet enables seamless video calls, media sharing, unlimited access to any resource available on the web, and many other things we now take for granted. Ultra-low power wireless devices are at the heart of the growing Internet of Things (IoT) market, which is set to revolutionise every aspect of our lives. Given its inherent ubiquity, any device must be cheap and require little maintenance to operate: just think of applications such as health and medical, wearables, distributed sensors, smart mesh networks, smart appliances and so on [1–3]. The transport of goods and people is becoming safer and more reliable thanks to increasingly advanced sensors and systems. The automotive sector in particular is undergoing the most dramatic change in decades: the electrification of the car. Hundreds of sensors and kilometres of wiring power the modern car, and this is just the beginning: the move to electric cars will only increase the need for advanced electronics. One of the most fascinating examples of RF development is automotive radar, which has gone from a niche, very expensive option to almost every new car, making roads safer. In addition, modern cars are seeing the rise of vehicle-to-vehicle communication as a means to improve traffic flow, increase passenger comfort and safety, and receive a constant stream of information about its surroundings, enabling novel self-driving features [4]. These and many other sensors work together to enable what is perhaps the holy grail of the automotive market: the self-driving car; a dream that seems closer than ever, with extraordinary results such as Bertha (Fig. 1) [5]. While safety and efficiency are top priorities, customers also expect high standards of comfort and connectivity: advanced infotainment, in-car WiFi and Bluetooth, GPS, remote monitoring, etc. The car of the future is *connected*, with the number of electronic chips and devices increasing exponentially. In other words, the car of the future is less about mechanical parts and more about chips and software [4, 6].

The main driver behind the widespread adoption of advanced RF electronic systems is the relentless effort of thousands of engineers to integrate increasingly complex systems into low-cost, monolithic CMOS chips capable of delivering high-performance solutions to (almost) every market. In fact, year after year, the humble

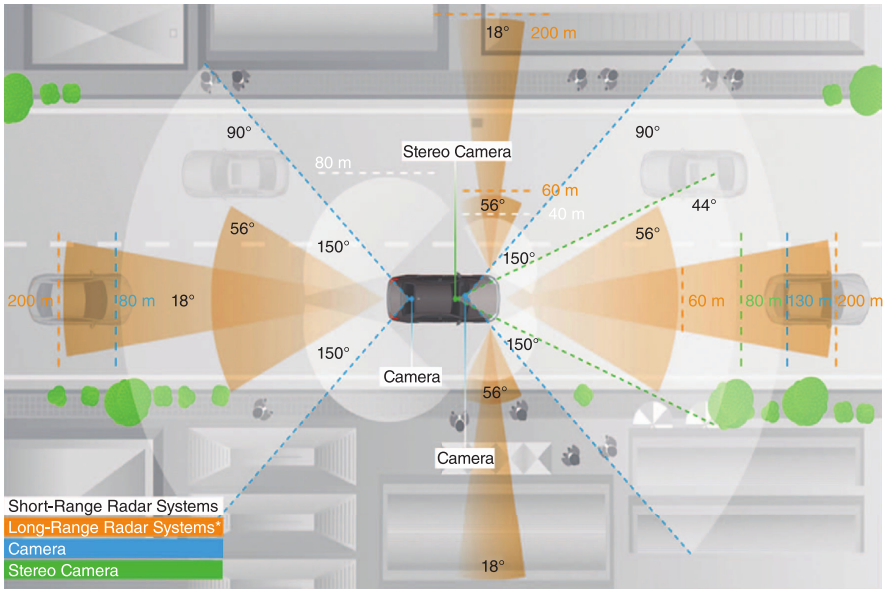


FIGURE 1: A picture depicting some of the sensors enabling the self-driving car Bertha [5]. Many are powered by mm-wave circuits.

silicon MOS transistor is creeping into parts of the RF spectrum that were once the domain of more expensive, exotic materials. By switching to a CMOS process, designers can integrate the entire RF front-end, baseband circuitry and digital logic in the same die, saving costs and reducing PCB complexity. In addition, at mm-wave frequencies, due to the small wavelength of the carrier signal, it is possible to integrate the antenna array directly on the chip itself, reducing losses. Automotive radar is a good example of the power of CMOS integration: operating in the millimetre-wave range and requiring relatively high power bursts, it was once implemented using expensive materials such as GaAs and discrete components. In the 2010s, SiGe became competitive and the first monolithic radar transceivers appeared, opening the gates to mass adoption, but with limited integration capabilities. For this reason, CMOS is likely to enter the market soon, as the feasibility of a CMOS radar at 77 GHz has already been demonstrated in various works [7, 8]. The introduction of a fully integrated CMOS radar would be a massive breakthrough, allowing the RF front-end to be integrated with the baseband and digital sections, reducing costs and increasing performance [9]. Another example of modern CMOS competitiveness is the 5G mm-wave front-ends for mobile phones. Once again, a market once dominated by GaAs [10] and SiGe is now slowly being penetrated by bulk or SOI CMOS solutions [11]. Although still in its infancy, modern research is demonstrating the feasibility of CMOS for sub-THz designs [12–15], that will soon be required for 6G applications (Fig. 2).

While CMOS has had to compete with more powerful but expensive exotic materials in high performance mm-wave applications, one area where it has always

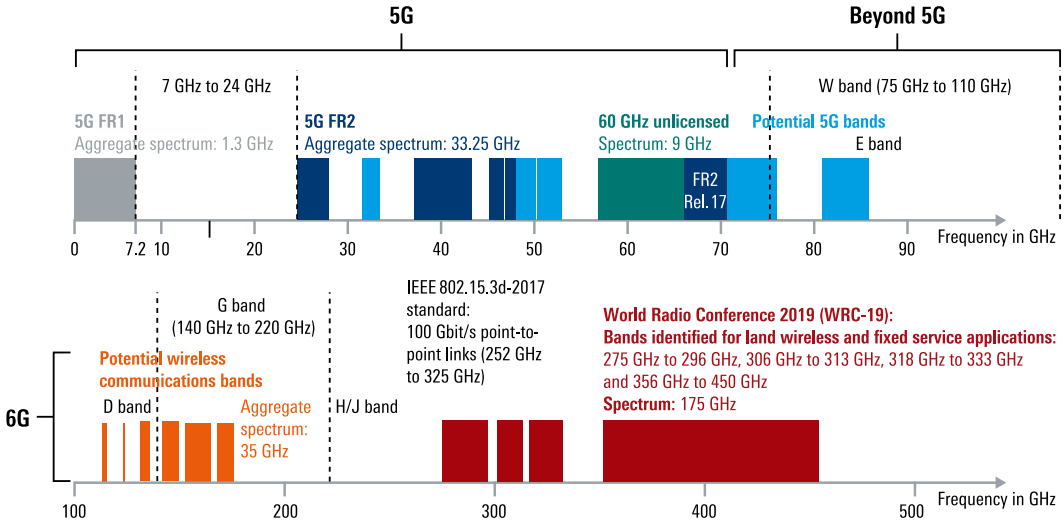


FIGURE 2: The spectrum of 5G and 6G communication protocols. The 6G protocol poses a challenge to CMOS RF technologies with its sub-THz capabilities [16].

dominated is in low power, low cost devices such as IoT devices. In this market, CMOS has always been the obvious choice for mass-producing the tiny, low-cost chips that required to connect millions, if not billions, of devices to the internet.

In general, the reduction of the minimum gate length improves the digital performance of the switch by reducing the MOSFETs channel resistance and parasitics, increasing the speed and lowering the power consumptions of digital circuits. On the other hand, scaling beyond 100 nm has had little benefit in analog applications: short channel effects and other non-idealities limit the improvements in the MOS transconductance ($g_m$); nanoscale lithographic and crystal imperfections more heavily affect smaller devices, impairing the matching [17]. For RF applications, the speed and bandwidth of the transistors are being limited by wiring parasitics and quantum effects, effectively neutralising the scaling advantages [17]. Moreover, the lower supply voltages imposed by scaled CMOS technologies harms noise and linearity performance of analog circuits [18].

Silicon-on-insulator CMOS technologies have shown promising results for RF and mm-wave applications, mitigating some of the issues introduced by nanoscale processes. SOI is a planar CMOS technology where a buried oxide layer (BOX) is embedded under in the substrate, effectively insulating the channels from the bulk and improving the transistor characteristics. An improvement of the SOI technology is the fully-depleted SOI (FD-SOI), where the transistor channel is built on top of a thin BOX layer, effectively insulating it from the rest of the devices, as shown in Fig. 3(b). The ultra-thin channel is left intrinsic, improving the carrier mobility

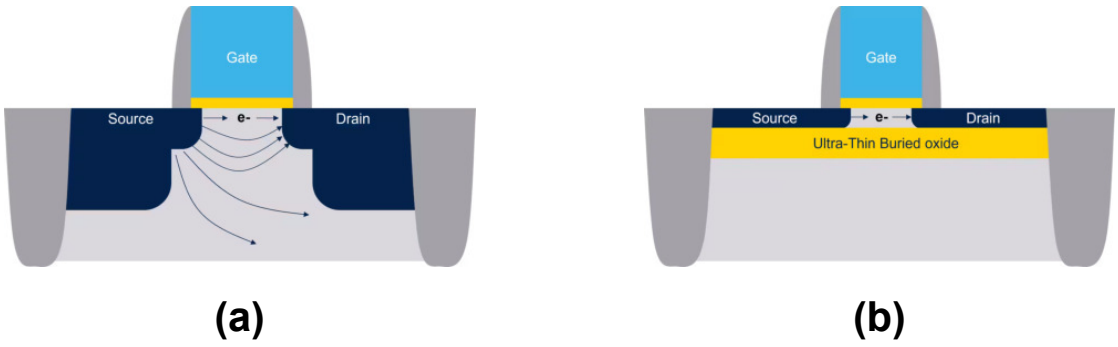


FIGURE 3: Cross section of a (a) bulk MOSFET (b) fully-depleted (FD) SOI MOSFET. Courtesy of *ST-Microelectronics*.

and avoiding issues due to the doping process. FD-SOI transistors reduced parasitic capacitances, lower leakage currents, lower noise and so on enable high performance RFICs [19]. The presence of the BOX layer in FD-SOI technologies allows the designer to alter the substrate polarisation and dynamically change some of the transistor properties such as the threshold voltage. This technique, called body-biasing, allows the designer to dynamically trade transistor speed for sub-threshold current leakage. However, SOI processes adoption has been slowed by their relative cost and poor thermal dissipation due to the buried oxide layer [20–22] posing a challenge for the thermal management of large systems such as phase shifter arrays [23].

Another casualty of scaling are the passives: the lower levels of the metal stack are extremely close to the substrate, increasing parasitic capacitance, and are very thin, being optimised for density. These two factors combine to degrade the performance of metal-oxide-metal (MOM) capacitors and inductors, fundamental building blocks of RF and mm-wave design. Again, the buried oxide layer in SOI mitigates this problem, but at the cost of a more expensive process compared to bulk CMOS.

In this thesis are reported the results achieved during the three years of Ph.D. that focused on two main aspects: the design of low-power and high-efficiency IoT transmitters; and the design of high-performance low-noise harmonic oscillators. The thesis reflects the dual focus of the Ph.D. by being divided into two main areas of interest: Chapters 1, 2, and 3 explore the analysis of mixers and design of an IoT transmitter; Chapters 4, 5, 6, and 7 explore three different oscillator topologies to improve the phase noise performance of integrated harmonic oscillators.

In Chapter 1 introduces the world of IoT and its role in shaping the low-power transceiver design. It introduces the topic of RF transmitters and their role in the quest for efficient IoT devices. Moreover, the chapter presents the challenges imposed by the adoption of higher data rate protocols to accommodate newer IoT

applications on current low-power transmitter topologies (e.g., the polar TX). The chapter with an overview on the role of the modulator in the efficiency of the transmitter.

Chapter 2 presents a time-variant analysis of the I/Q passive resistive mixer. First the quadrature passive resistive mixer is presented alongside its non-idealities that limit its performances. The obtained model is then applied to the 50 and 25% LO duty-cycle cases, resulting in a LTI Thevenin equivalent source. The Chapter ends with a discussion on the obtained results.

Chapter 3 explores the advantages of the passive reactive mixer for low-power Cartesian modulators. A thorough analysis of the capacitive passive mixer is carried out, revealing its filter-before-upconversion behaviour allows for simpler, less power hungry baseband interfaces. The analysis also results in useful design equations that are leveraged to optimise the TX efficiency. The Chapter reports the design of a 2.4 GHz Cartesian TX for IoT employing the proposed passive capacitive mixer. The prototypes are fully characterised, showing a state-of-the-art system efficiency of 22% when transmitting a 16-QAM signal at 2.4 Mbaud at an average output power of 2.7 dBm.

In Chapter 4 is introduced the role and importance of the harmonic oscillator in the modern radiofrequency integrated circuit (RFIC) design: from communications to RADAR applications, the local oscillator is the most critical component. The most used oscillator topology, the class-B cross-couple differential-pair oscillator, is discussed, highlighting its limits. The Chapter discusses the role of current trends of CMOS scaling in limiting the phase noise performance of the class-B oscillator, showing that newer solutions are needed to reach ever lower phase noise.

In Chapter 5 is reported the analysis, design an measurement of a 12 GHz reconfigurable octacore digitally controlled oscillator (DCO) capable of trading phase noise for power consumption, dynamically changing the number of active cores. The time-variant analysis studies the impact on phase noise of the presence of MOS switches in the coupling network. The prototypes, realised in a 28 nm process, reach a phase noise of -126 dBc/Hz at 1 MHz offset at 10.7 GHz when all eight cores are operating; as expected, the phase noise increases when the number of active cores is decreased. The design and implementation was carried out during the Master's thesis at Infineon Villach; the measurement and analysis were carried out during the Ph.D.

In Chapter 6 series oscillators are presented showing how they can potentially achieve more than 20 dB of phase noise improvement over their parallel counterpart. A 10 GHz transformer-based series VCO is proposed and analysed. The Chapter also includes its design and prototype characterisation.

The last proposed low-noise oscillator is presented in Chapter 7. The proposed VCO exploits CMOS stacking to safely increase the oscillation swing and decrease the phase noise beyond what normally possible in ultra-scaled CMOS technologies. The prototypes are designed and realised in a 22 nm FD-SOI CMOS technology, and reach a phase noise of -126 dBc/Hz at 1 MHz offset at 5.2 GHz, with a supply voltage of 1.6 V, double the maximum limit imposed by the technology.

Finally the conclusions and closing words are reached in Chapter 7.2.

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# Chapter 1

# Low Power Transmitters for the Next Generation of IoT

## 1.1 Internet of Things

More of a paradigm than a well defined technology, the Internet of Things (IoT) has evolved over the years to become a massive reality in our lives. In an IoT world every device will be able to collect, elaborate, and send data over the internet to enhance its functionality or to enable new ones altogether. Put plainly, IoT is a system of interrelated computing devices, mechanical and digital machines, objects, animals or people that are provided with the ability to transfer data over a network without requiring human-to-human or human-to-computer interaction [3]. The first example of an IoT device was a modified Coke machine at Carnegie Mellon University becoming the first network-connected appliance. Nowadays, IoT devices can be as simple as a remotely-operated light bulb, up to extremely complex and sophisticated city-wide networks of sensors monitoring the air quality, weather, traffic [25,26], or entire facilities operated by thousands of smart sensors and robots, all interconnected through the internet. The success of IoT is measured by the billions of internet-enabled that are already operating, with a projected doubling of active devices before the year 2030 [24].

Given its inherent flexibility the concept of IoT can be, and is, applied to hundreds, if not thousands, of different fields, such as:

- multimedia
- edge computing
- health
- wearables
- home automation (domotics)

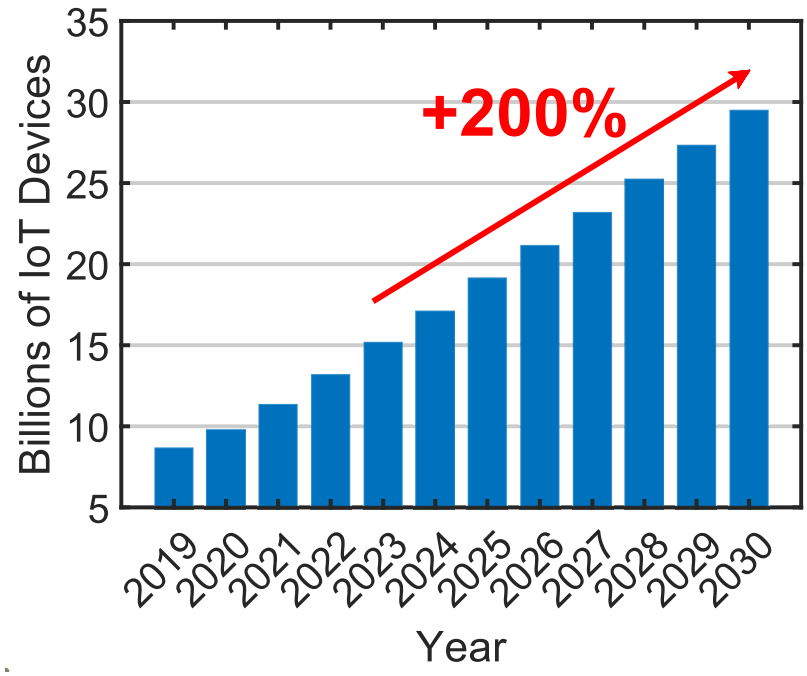


FIGURE 1.1: Projected growth of the connected IoT devices [24].

- agriculture
- energy (smart grid)
- manufacturing
- logistics
- urban monitoring (smart cities)
- safety and surveillance

The list is endless and it keeps growing [1–3, 25]. IoT devices have a vast impact on our life, but they also pose some challenges. IoT devices generate a large amount of data that needs to be stored, processed, but, most importantly, continuously transmitted to the internet. Any IoT device needs a way to communicate to the external world.

Power consumption of an IoT device is a crucial factor that affects its performance, battery life, and environmental impact. IoT devices often use wireless communication technologies that consume different amounts of power depending on the network conditions, data rate, and power saving features. For example, WiFi is a common wireless protocol for IoT devices, but it has high power consumption and requires AC-powered devices. On the other hand, low-power wide-area networks


FIGURE 1.2: Wearable tech is one of the most promising IoT applications, with millions of devices already shipped.

(LPWAN) such as LTE-M or NB-IoT offer lower power consumption and longer battery life for IoT devices that operate in remote or hard-to-reach locations. However, these technologies also have trade-offs in terms of bandwidth, latency, and coverage [1–3].

Power consumption optimization is not only important for improving the performance and reliability of IoT devices, but also for reducing their environmental impact. IoT devices are expected to reach billions of units in the near future [27], which means they will consume a significant amount of energy and generate a lot of electronic waste. By designing IoT devices that consume less power and last longer, developers can contribute to a more sustainable and greener IoT ecosystem.

The impact of the RF front-end in IoT devices is significant, as it determines the performance, power consumption, and efficiency of the device [28]. The RF front-end refers to the components that are responsible for receiving and transmitting RF signals, such as filters, amplifiers, switches, and antennas. While the digital circuitry takes advantage of CMOS scaling, the power consumption of the analog circuitry is largely determined by design specifications. There are two main ways to reduce the power consumption of a radio. One is to implement clever communication protocols that, for example, reduce the amount of time the radio is on by transmitting short bursts of data and then switching off completely, or by using wake-up receivers that go into a super-low power state while waiting for an external transmission. The other is to act at the transistor level and increase the efficiency

TABLE 1.1: Comparison of requirements of different IoT classes.

| Required parameter | Standard IoT | Multimedia IoT | Automotive IoT |
|---|---|---|---|
| Average data size | Kilobytes | Megabytes to Gigabytes | Megabytes |
| Bandwidth | Kb/s | Mb/s | Mb/s |
| Latency | High | Medium/Low | Low |
| Power consumption | Low | High | Medium/High |
| Possible protocol(s) | BLE, ZigBee, LoRa | Bluetooth, WiFi, 5G | 5G |

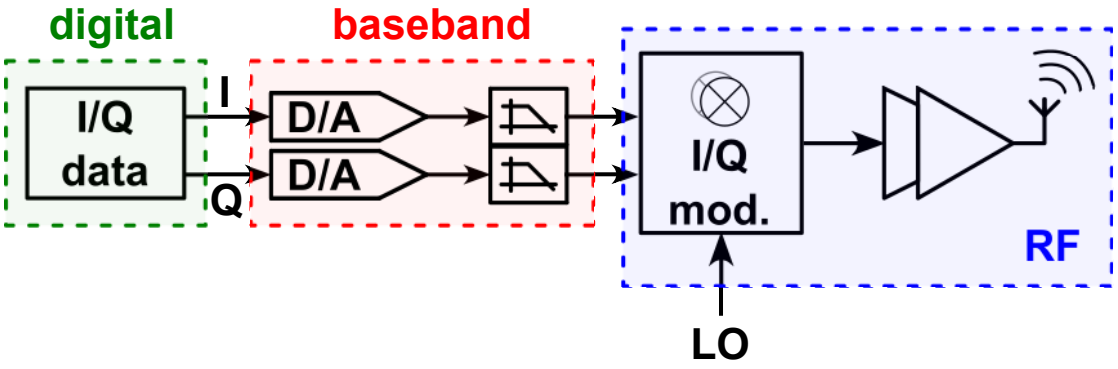


FIGURE 1.3: Block diagram of a generic TX.

of the system. The latter is what the RF designer has most control over, as it requires the development of clever topologies and strategies to overcome the inherent limitations of CMOS technology. So, how do we improve the efficiency of an IoT transmitter (TX)? Before answering this question, we first have to understand what a TX is.

## 1.2 What is a transmitter?

In RF electronics, the TX is a system of blocks responsible for transmitting data. Modern transmitters are digital, which means that the data being transmitted comes from a digital signal, but the circuitry and the signal itself are still analog. An example of a modern digital transmitter is shown in Fig. 1.3 and consists of four main blocks: the digital circuitry that prepares the data, the baseband circuitry that performs the D/A conversion of the data, a modulator that shifts the baseband data signal to a higher frequency, and a power amplifier (PA) that drives the antenna.

In its essence, wireless data transmission is composed by two elements: a carrier signal and a modulating signal containing the information (Fig. 1.4). The carrier is usually a sinusoidal tone at a fixed frequency $f_0$ (in reality it can be changed to transmit in different channels). The modulating signal is a much more complex waveform that carries the data, it is generated by the D/A converters driven by the

digital circuitry and filtered to remove any spurious or unwanted content. Usually, the spectrum of the modulating signal is located at baseband (i.e., it extends from 0 up to $B/2$ Hz (Fig. 1.4) which would impossible to transmit unless first translated to a higher frequency, in a process called modulation. In practice, this is achieved by altering the physical properties of the carrier signal (amplitude, frequency, phase etc.), effectively encoding the data within the carrier itself. The effect of the modulation can be better appreciated in the frequency domain: in Fig. 1.4 the baseband modulating signal (in blue) is shifted from DC to $f_0$ after the modulation, making it much easier to transmit. The circuit block that implements the modulation is called modulator. The most basic modulator can be realised by multiplying the carrier signal by the baseband signal (Fig. 1.5(a)). In the frequency domain, the time multiplication becomes a convolution, thus realising the desired frequency translation.

An immediate improvement over the simple modulator is the I/Q modulator obtained by adding a branch with an LO in quadrature, as in Fig. 1.5(b). In this way it is possible to encode two signals with the same bandwidth. This can be thought as encoding the real $a(t)$ and imaginary $b(t)$ part of modulated signal. The I/Q modulator is at the heart of digital radios, where the data is encoded in in-phase and quadrature amplitude components that identify different points in the complex numbers plane; by assigning a unique value to each point we can build a constellation of symbols (Fig. 1.6). This modulations scheme is called M-QAM where M is the number of symbols in the constellation. The higher the M, the more bits per symbol, the higher the spectral efficiency of the modulation.

The circuit block that implements the time-domain multiplication is called mixer; there are many mixer topologies, but they can be broadly divided into active and passive mixers. Roughly speaking, if the transistors are used as transconductors, then the mixer is active (a famous example is the Gilbert cell). If the transistors are used as switches, then it's passive. Passive mixers show better linearity and lower power consumption (the mixer itself is passive but dynamic power is dissipated by the LO drivers), but they are lossy. Usually, passive mixers are preferred over active ones for low power applications such as IoT.

Since passive mixers are inherently lossy, a PA is required to amplify the signal before it is fed to the antenna. The PA is a critical block, as it must amplify the signal without distortion, while wasting as little power as possible. In most RF applications, the power consumption of the PA is so much higher than the rest of the system that the overall efficiency of the transmitter is largely determined by the efficiency of the PA. Conversely, in applications where the output signal power is low (e.g., IoT), the power consumption of the baseband circuitry and mixer has a much greater impact on the system efficiency. For this reason, increasing the efficiency in

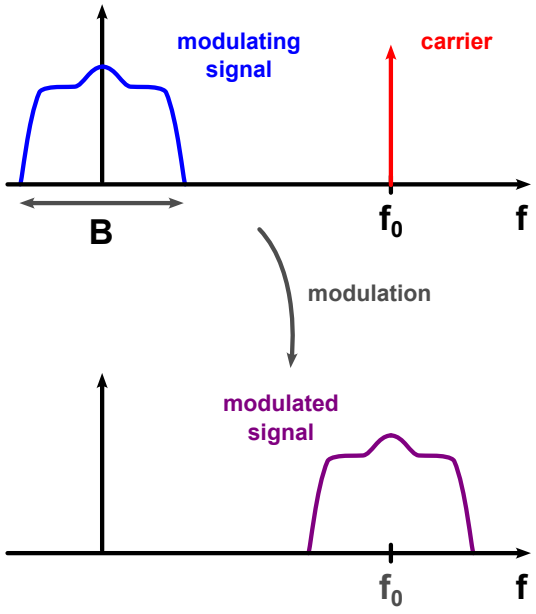


FIGURE 1.4: The baseband modulating signal is upconverted to the carrier frequency by the modulation of the carrier.

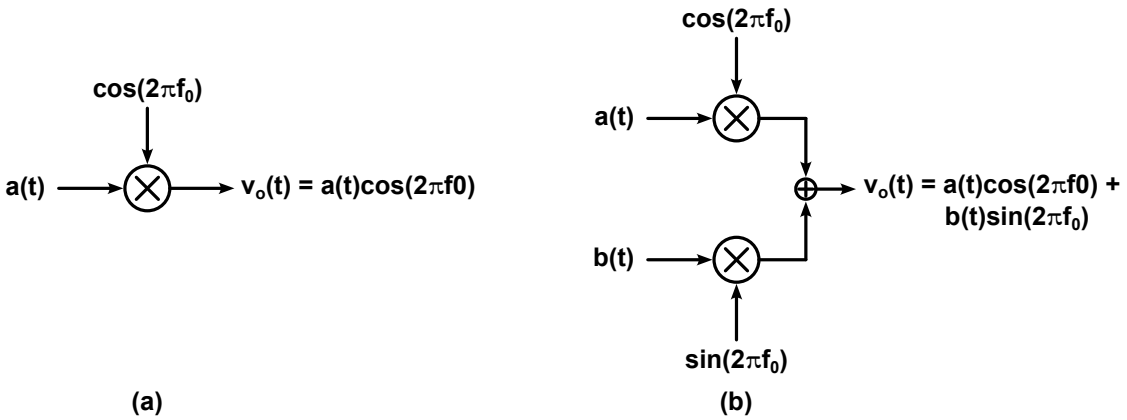


FIGURE 1.5: Basic modulators: (a) simple modulator; (b) I/Q modulator.

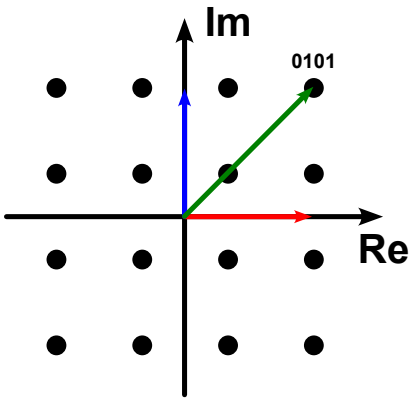


FIGURE 1.6: Example of a 16-QAM constellation: the real (red) and imaginary (blue) vectors identify a point in the complex numbers plane.

low power RF front-ends is more about working on the entire system, and less about optimising the PA efficiency.

The following two Chapters focus on the study of two different classes of passive mixers, with the aim of designing an efficient IoT Cartesian modulator: in Chapter 2 a time-variant analysis of the passive resistive mixer is performed, deriving a powerful yet simple model of the mixer operation; in Chapter 3 a prototype of a Cartesian TX for IoT based on a passive reactive mixer is presented and analysed, demonstrating how the use of a passive reactive mixer can simplify the baseband circuitry, increase the overall TX efficiency while retaining the ability to modulate QAM signals.

# Chapter 2

# A Time-Variant Analysis of Passive Resistive Mixers Using Thevenin Theorem

Passive resistive mixers have gained popularity in radio frequency (RF) and millimetre wave (mm-wave) applications over their active counterparts due to their high linearity and simplicity. Passive mixers are often implemented using CMOS transistors driven by a strong local oscillator (LO) signal, effectively acting as ideal switches or, more realistically, variable resistors (hence the name of passive *resistive* mixers). The former interpretation forms the backbone of the classical mixer theory and provides a simplified model for explaining their basic behaviour, but it fails to capture the effects of the MOS switch resistance on the conversion gain. This is especially noticeable in high frequency applications, where, in order to limit the parasitics, the gate area of the CMOS switches must be minimised, leading to a degradation in their on- *and* off-resistance. Taking into account the switch resistance leads to a more challenging analysis, which is the subject of several papers [29–32]. However, these works either ignore the switch off-resistance and source resistance, or assume non-overlapping LO quadrature signals with a 25% duty cycle [31].

This Chapter presents a more general analysis that takes into account the finite on- and off-resistance of the switches, the source resistance, the presence of a load impedance and a quadrature (I-Q) architecture.

## 2.1 Analysis of the Passive Resistive Mixer

We will analyze the double-balanced quadrature (I-Q) passive resistive mixer, whose schematic is shown in Fig. 2.1. It is composed by one in-phase and one quadrature cell connected in parallel, loaded by capacitor $C_L$. A single cell of the mixer is itself comprised of a voltage source, $v_{m,I(Q)}(t)$, along with the source resistance $R_s$, and

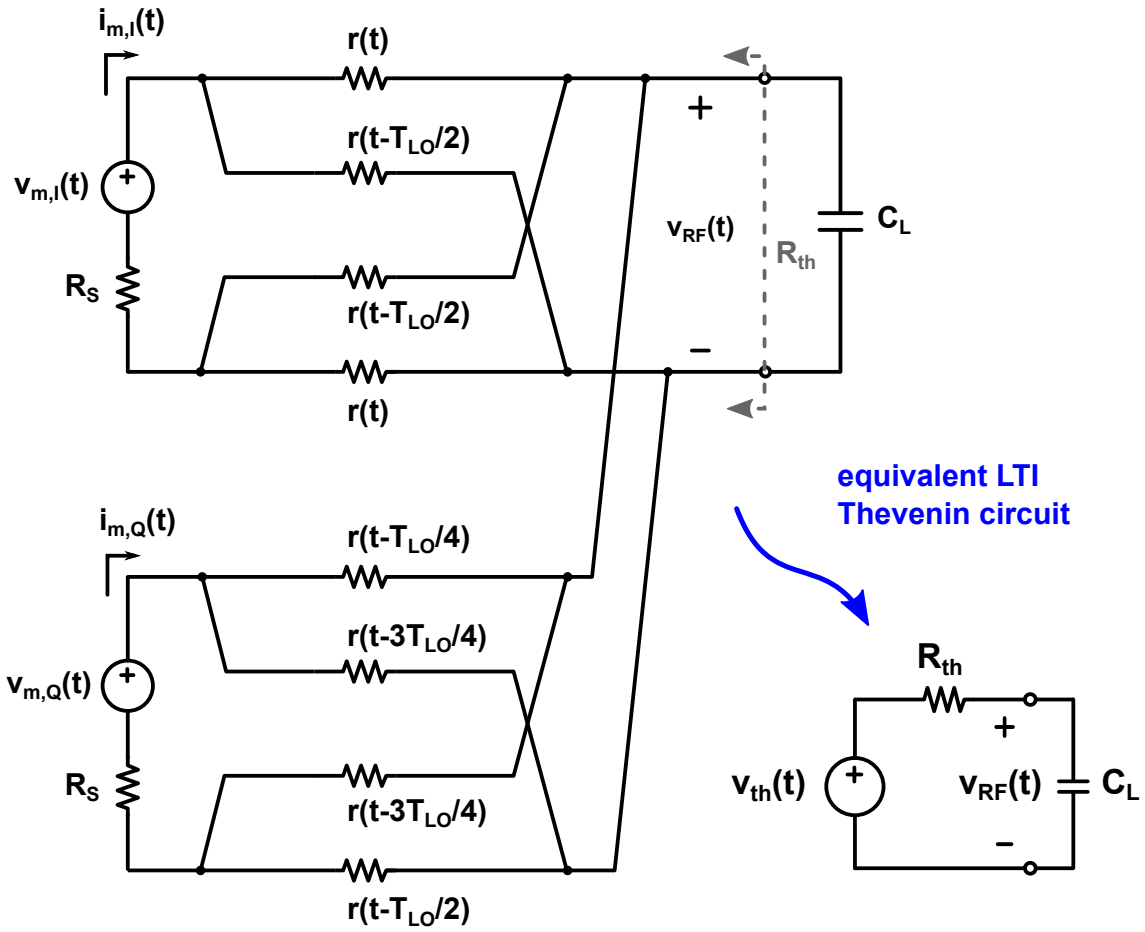


FIGURE 2.1: Schematic of the passive resistive quadrature mixer, and its Thevenin equivalent.

the mixer switches, here represented by time varying resistors $r(t)$. The latter are all identical but for a time shift representing the different LO phases.

The arrangement in Fig. 2.1 is typically used as an upconversion mixer, and, in the following, we will refer to this scenario. However, it should be noticed that the presented results can be rather promptly extented to the downconversion case leveraging interreciprocity, and, in particular, the frequency reversal theorem [33].

Since the the passive reactive mixer is a linear, although time-variant, circuit, it can be represented by a Thevenin equivalent circuit as seen by the load $C_L$ (Fig. 2.1). This equivalent network is made of the voltage generator $v_{th}(t)$, and the Thevenin resistance $r_{th}(t)$.

To derive the Thevenin equivalent, we will first focus on the in-phase cell alone, computing its Thevenin equivalent circuit. Next, the procedure will be repeated on the quadrature cell. Finally, the overall equivalent circuit of the I-Q mixer will be obtained.

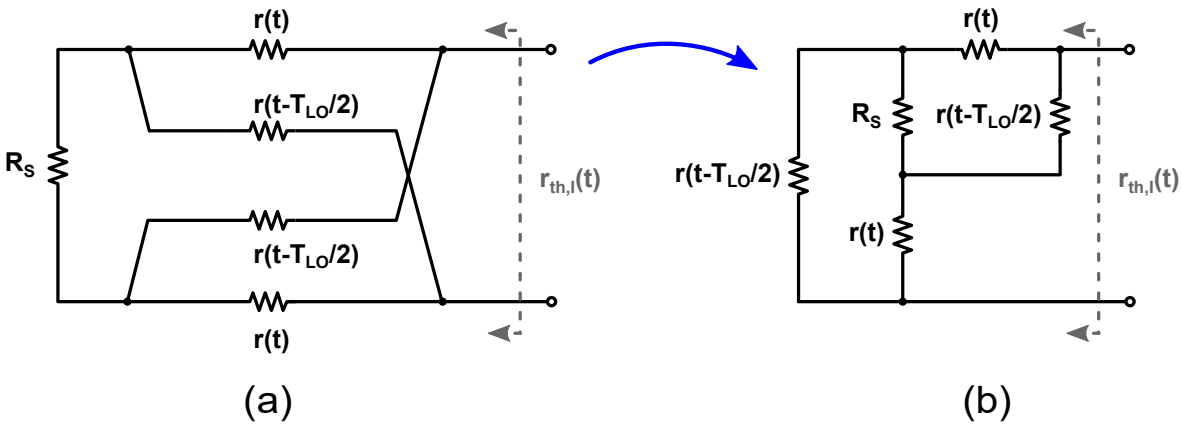


FIGURE 2.2: Circuit used for the evaluation of the Thevenin resistance of the in-phase cell: (a) original circuit; (b) rearranged circuit.

### 2.1.1 Thevenin Resistance of the In-phase Cell

To compute the Thevenin resistance of the in-phase cell, $r_{th,I}$, we use the schematic in Fig. 2.2(a). The network can be rearranged as in Fig. 2.2(b). After a delta-star transformation, the Thevenin resistance is easily found as:

$$r_{th,I}(t) = \frac{2r(t)r(t - T_{LO}/2) + r(t)R_s + r(t - T_{LO}/2)R_s}{r(t) + r(t - T_{LO}/2) + 2R_s} \tag{2.1}$$

This result may seem unremarkable: $r_{th,I}(t)$ is time-varying and gives little insight into the operation of the mixer. However, as it will be shown in Section 2.2, under some assumptions that are readily met in practice, $r_{th,I}$ is actually constant in time.

### 2.1.2 Thevenin Voltage Source of the In-phase Cell

The derivation of the Thevenin voltage source of the in-phase cell requires a slightly more involved approach.

The circuit can be rearranged as shown in Fig. 2.3, from which follows

$$v_{m,I}(t) = \frac{i_{m,I}(t)}{2}\left[2R_s + r(t) + r(t - T_{LO}/2)\right] \tag{2.2}$$

and

$$v_{th,I}(t) = \frac{i_{m,I}(t)}{2}\left[r(t - T_{LO}/2) - r(t)\right] \tag{2.3}$$

Combining (2.2) and (2.3) we get

$$v_{th,I}(t) = \frac{r(t - T_{LO}/2) - r(t)}{2R_s + r(t) + r(t - T_{LO}/2)} v_{m,I}(t) = m_I(t)v_{m,I}(t) \tag{2.4}$$

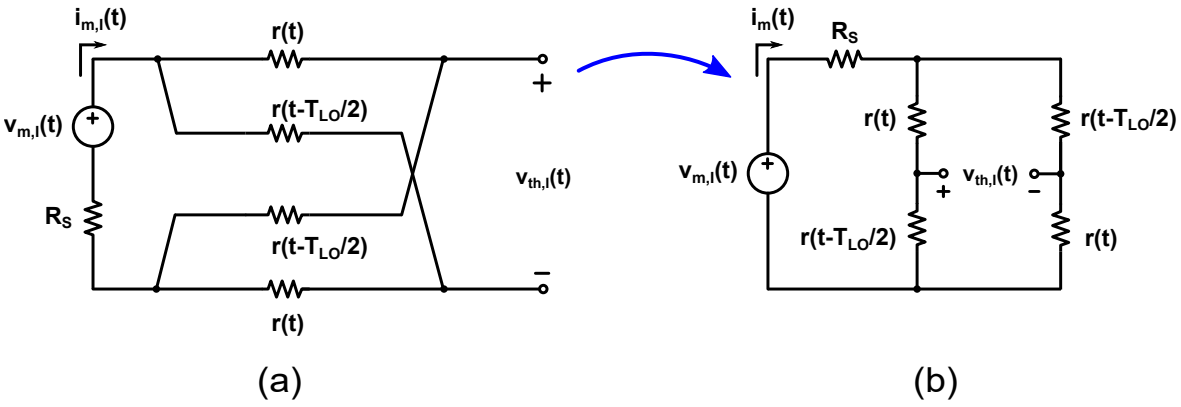


FIGURE 2.3: Circuit used for the evaluation of the Thevenin voltage of the in-phase cell.

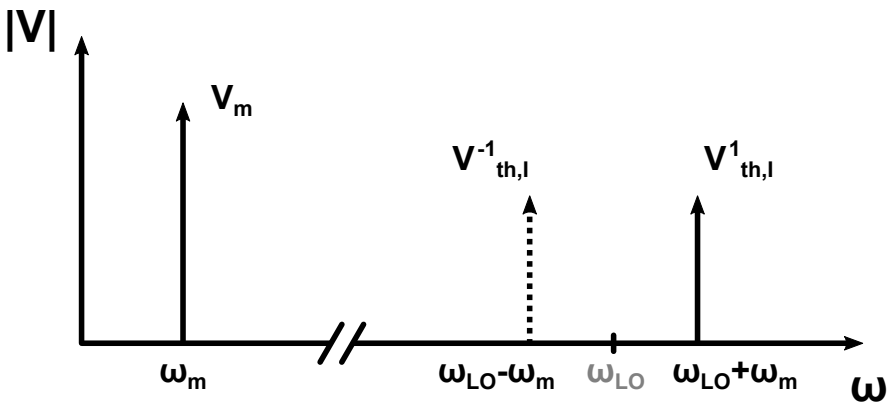


FIGURE 2.4: Sketch of the frequency components taken into account in the analysis of the in-phase cell. The lower-sideband, $V_{th,I}^{-1}$, vanishes due to the operation of the complete quadrature (I-Q) mixer.

where $m_I(t)$ is the modulating function of the in-phase cell. Since the mixer operation is periodic with period $T_{LO} = 2\pi/\omega_{LO}$, $m_I(t)$ can be expanded in bilateral Fourier series:

$$m_I(t) = \sum_{k=-\infty}^{\infty} m_{I,k} e^{jk\omega_{LO}t} \tag{2.5}$$

Assuming the circuit is excited by an exponential tone with amplitude $V_{m,I}$ and frequency $\omega_m$, the upper-sideband, $V_{th,I}^{1}$, that is, the frequency component of $v_{th,I}(t)$ at frequency $\omega_{LO} + \omega_m$, is

$$V_{th,I}^{1} = m_{I,1} V_{m,I} \tag{2.6}$$

A sketch of the frequency components taken into account in the calculation is shown in Fig. 2.4. Note that the lower-sideband (at frequency $\omega_{LO} - \omega_m$) will vanish due to the operation of the complete quadrature (I-Q) mixer.

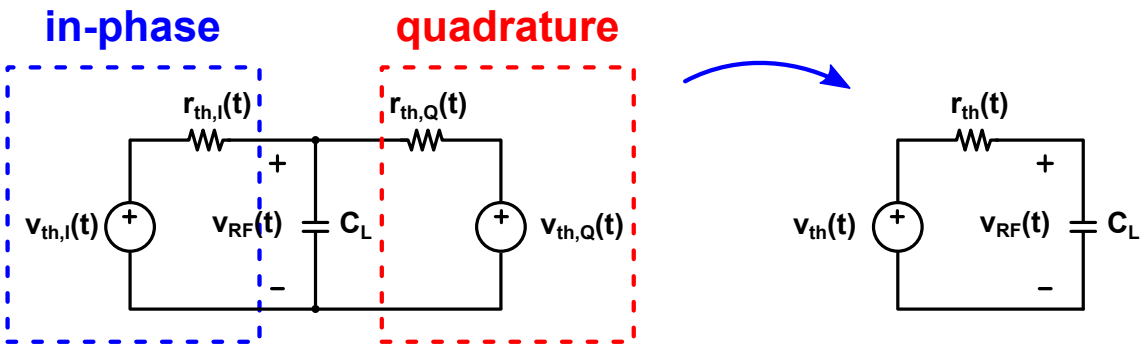


FIGURE 2.5: Equivalent Thevenin circuit for the overall I-Q mixer. The in-phase and quadrature cell are replaced by their equivalent Thevenin circuits.

### 2.1.3 Equivalent Thevenin Circuit of the Quadrature Cell

The foregoing analysis can be applied to the quadrature cell as well. Taking into account the time shift due to the quadrature phase of the LO we get

$$r_{th,Q}(t) = r_{th,I}(t - T_{LO}/4) \tag{2.7}$$

$$m_Q(t) = m_I(t - T_{LO}/4) \tag{2.8}$$

and

$$V^1_{th,Q} = m_{Q,1} V_{m,Q} \tag{2.9}$$

where $m_{Q,1} = -jm_{I,1}$ and $V_{m,Q} = jV_{m,I}$.

### 2.1.4 Equivalent Thevenin Circuit for the Overall I-Q Mixer

Given the linearity of the system, the Thevenin equivalent circuits of the in-phase and quadrature cells can be further combined into a single equivalent Thevenin circuit for the overall I-Q mixer, as sketched in Fig. 2.5. We have:

$$r_{th}(t) = \left( \frac{1}{r_{th,I}(t)} + \frac{1}{r_{th,Q}(t)} \right)^{-1} \tag{2.10}$$

and

$$v_{th}(t) = \left( \frac{v_{th,I}(t)}{r_{th,I}(t)} + \frac{v_{th,Q}(t)}{r_{th,Q}(t)} \right) r_{th}(t) \tag{2.11}$$

Using (2.1), (2.4), (2.7), and (2.8), (2.11) can be recast as

$$v_{th}(t) = \left[ m(t) v_{m,I}(t) + m(t - T_{LO}/4) v_{m,Q}(t) \right] r_{th}(t) \tag{2.12}$$

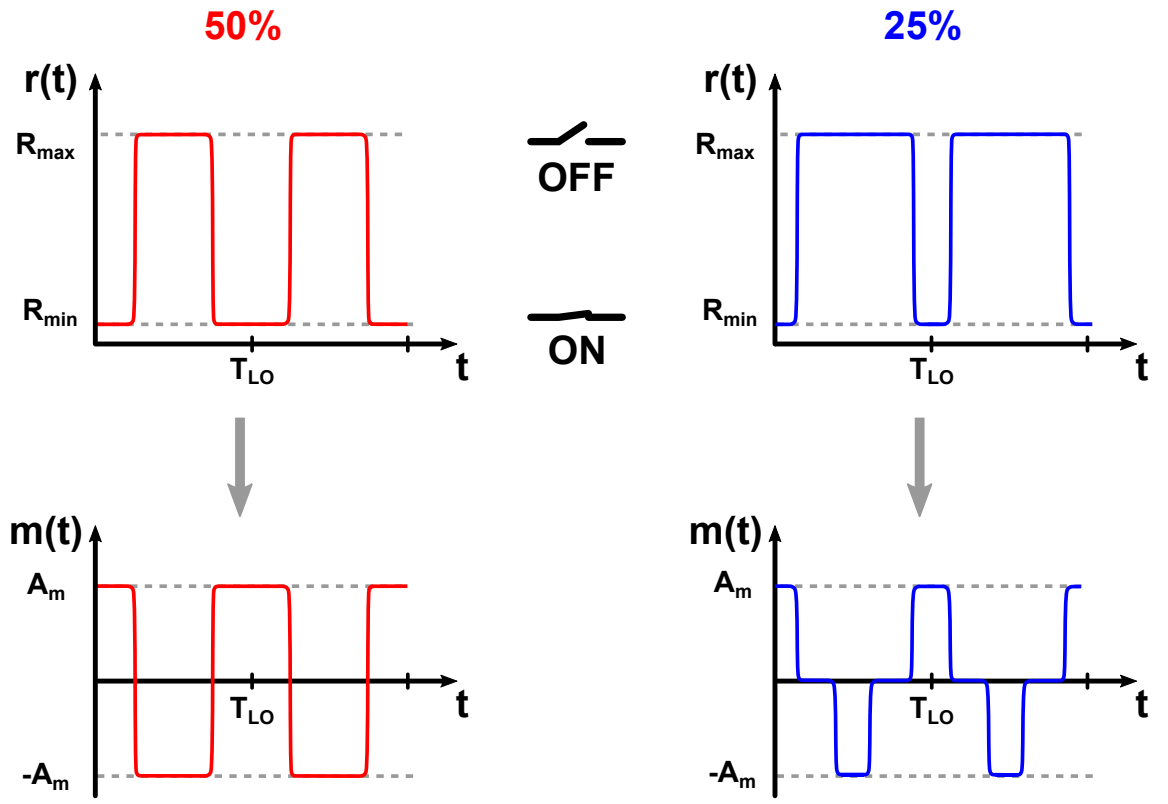


FIGURE 2.6: Sketch of the $r(t)$ and $m(t)$ waveforms for the I-Q mixer with 50% (left) and 25% (right) duty-cycle LO.

where

$$m(t) = \frac{r(t - T_{LO}/2) - r(t)}{2r(t)r(t - T_{LO}/2) + R_s\left[r(t) + r(t - T_{LO}/2)\right]} \tag{2.13}$$

This result may look cumbersome and of hardly any use given its time-variant nature. However, as soon as a resistance waveform $r(t)$ of practical interest is considered, (2.10) and (2.12) strongly simplify, as we are about to see.

## 2.2 Practical Applications

### 2.2.1 I-Q Mixer with 50% Duty-Cycle LO

If the mixer is driven by a (quadrature) LO with 50% duty-cycle, the switches spend an equal time on and off. The resulting $r(t)$ is a square wave with period $1/T_{LO}$ with maximum value $R_{max}$ (switch off-resistance) and minimum value $R_{min}$ (switch on-resistance), as sketched in Fig. 2.6 on the left.

Remarkably, with this particular $r(t)$, the Thevenin resistance of both the in-phase and quadrature cells [see (2.1) and (2.7)] is constant:

$$r_{th,I}(t) = r_{th,Q}(t) = \frac{2R_{max}R_{min} + R_{max}R_s + R_{min}R_s}{R_{max} + R_{min} + 2R_s} \tag{2.14}$$

Hence, from (2.10), we get

$$R_{th} = r_{th}(t) = \frac{1}{2}\frac{2R_{min} + R_s\left(1 + \frac{R_{min}}{R_{max}}\right)}{1 + \frac{R_{min}}{R_{max}} + \frac{2R_s}{R_{max}}} \tag{2.15}$$

This result shows that the equivalent Thevenin circuit of the I-Q mixer with 50% duty-cycle LO is actually a time-invariant circuit, which greatly simplifies the analysis of the interaction of the mixer with the load.

With the given $r(t)$, the resulting $m(t)$ waveform (Fig. 2.6 on the left) is a zero-mean square wave with peak value

$$A_m = \frac{R_{max} - R_{min}}{2R_{max}R_{min} + R_s(R_{max} + R_{min})} \tag{2.16}$$

Since $R_{th}$ is constant in time and $m(t)$ is periodic, from (2.12) we get that the upper-sideband of $v_{th}(t)$, $V_{th}^1$, at frequency $\omega_{LO} + \omega_m$ is

$$V_{th}^1 = 2m_1 R_{th} V_m = A_{v0} V_m \tag{2.17}$$

where

$$m_1 = \frac{2}{\pi}\frac{R_{max} - R_{min}}{2R_{max}R_{min} + R_s(R_{max} + R_{min})} \tag{2.18}$$

is the first coefficient of the bilateral Fourier series expansion of $m(t)$, $V_m = |V_{m,I}| = |V_{m,Q}|$, and we assume, without loss of generality, that $V_{m,I}$ is a real number. Using (2.15) and (2.18) the open-circuit conversion gain of the I-Q mixer, $A_{v0}$, is

$$A_{v0} = \frac{2}{\pi} \cdot \frac{1 - \frac{R_{min}}{R_{max}}}{1 + \frac{R_{min}}{R_{max}} + \frac{2R_s}{R_{max}}} \tag{2.19}$$

It can be noticed that whenever the ratio $R_{max}/R_{min}$ is not very large, $A_{v0}$ decreases with respect to the ideal $2/\pi$ level. Likewise, if the source resistance $R_s$ is large, compararable with the off-resistance of the switches, a decrease in $A_{v0}$ is observed. Such decreases are due to the loading effect of the switches resistances on the signal source. Interestingly, (2.19) shows that the source resistance $R_s$ has an impact on the conversion gain of the mixer, even without the presence of any explicit load impedance, due to the loading effect of the time-variant resistive network.

Now we consider the impact of the load impedance. Since the equivalent Thevenin circuit in Fig. 2.5 is time-invariant, taking into account the load impedance is easy. We analyze in detail the case the load impedance is a capacitor $C_L$ (Fig. 2.1). The

(loaded) mixer conversion gain is immediately found as

$$A_v(j(\omega_{LO}+\omega_m)) = \frac{A_{v0}}{1+j(\omega_{LO}+\omega_m)R_{th}C_L} \tag{2.20}$$

It may be noticed that the mixer input signal is first frequency converted and then filtered, a result already observed in [29], here derived in a more general framework, i.e., a I-Q mixer, $R_s \neq 0$ and $R_{max} < \infty$.

### 2.2.2 I-Q Mixer with 25% Duty-Cycle LO

Another case of practical interest is a I-Q mixer driven by an LO signal with a 25% duty-cycle. It provides a larger conversion gain compared to the I-Q mixer with an LO signal with 50% duty-cycle; for this reason it is widely used. The $r(t)$ waveform for the I-Q mixer with a 25% duty-cycle LO is sketched in Fig. 2.6 on the right.

Unlike the case of the mixer with 50% duty-cycle LO, in the mixer with 25% duty-cycle LO, the Thevenin resistances of the in-phase and quadrature cells, given by (2.1) and (2.7), are not time-invariant. However, the Thevenin resistance of the overall I-Q mixer, given by (2.10), is still constant:

$$R_{th} = r_{th}(t) = \frac{2R_{min} + R_s(1+\frac{R_{min}}{R_{max}})}{1+\frac{3R_{min}}{R_{max}}+\frac{R_s}{R_{max}}\left(3+\frac{R_{min}}{R_{max}}\right)} \tag{2.21}$$

Therefore, (2.17) and (2.20) still hold—with (2.21) in place of (2.15), of course.

The waveform of $m(t)$ for the I-Q mixer with a 25% duty-cycle LO is sketched in Fig. 2.6 on the right, from which we get:

$$m_1 = \frac{\sqrt{2}}{\pi}\frac{R_{max}-R_{min}}{2R_{max}R_{min}+R_s(R_{max}+R_{min})} \tag{2.22}$$

and

$$A_{v0} = \frac{2\sqrt{2}}{\pi}\cdot\frac{1-\frac{R_{min}}{R_{max}}}{1+3\frac{R_{min}}{R_{max}}+\frac{R_s}{R_{max}}\left(3+\frac{R_{min}}{R_{max}}\right)} \tag{2.23}$$

## 2.3 Simulation Results

Simulations are carried out to validate the presented analysis for both the I-Q mixer with 50% duty-cycle LO and for the I-Q mixer with 25% duty-cycle LO. A first set of simulations aims to verify the open-circuit gain: no load is applied to the I-Q mixer RF port. In Fig. 2.7(a), the gain is reported for various $R_{max}/R_{min}$ ratios, while $R_s = 0$. In Fig. 2.7(b) instead, $R_s$ is swept while keeping $R_{min} = 100\,\Omega$ and

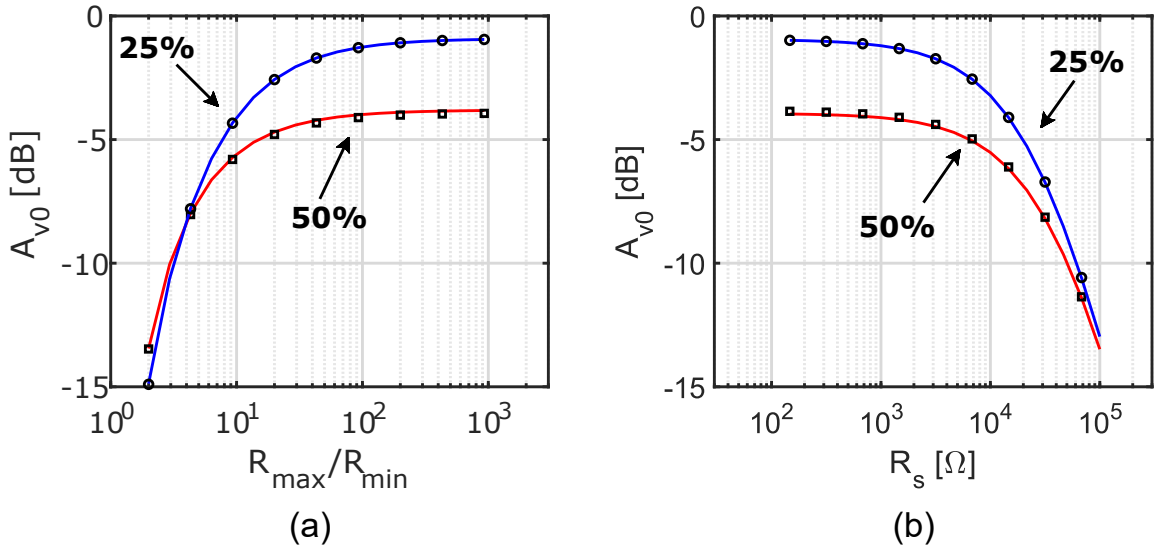


FIGURE 2.7: Open-circuit mixer gain $A_{v0}$: (a) gain vs. $R_{max}/R_{min}$; (b) gain vs. $R_s$. Simulations (markers) are compared with estimates from (2.19) and (2.23).

$R_{max}/R_{min} = 1000$. The simulated values (square markers for the 50% duty-cycle LO and circle markers for the 25% duty-cycle LO) are compared against the estimates coming from (2.19) (solid red line) and (2.23) (solid blue line), showing very good agreement. The impact of $R_s$ on the gain is negligible until $R_s$ reaches values comparable with the switch off-resistance.

Next, the focus is shifted on the bandwidth of the mixer, $BW = 1/(2\pi R_{th} C_L)$. The plots in Fig. 2.8 show the decrease in bandwidth with increasing $R_{min}$ (Fig. 2.8(a), with $R_{max}/R_{min} = 1000$, $C_L = 100\,fF$, and nil $R_s$), and increasing $C_L$ (Fig. 2.8(b), with $R_{min} = 100\,\Omega$, $R_{max}/R_{min} = 1000$, and nil $R_s$). Again, there is very good agreement between simulations (markers) and calculations (solid lines).

The impact of $R_s$ on the mixer bandwidth is assessed in Fig. 2.9 (a), where the bandwidth is plotted vs. $R_s$ with $R_{min} = 100\,\Omega$, $R_{max}/R_{min} = 1000$, and $C_L = 100\,fF$. Simulations (squares) agree very well with calculations (solid line). Notice that the bandwidth severely decreases, even for relatively small values of $R_s$. On the contrary, the switch on/off-resistance ratio has little effect on the bandwidth itself, as shown in Fig. 2.9 (b), for $C_L = 100\,fF$, and nil $R_s$. Even in this case the good agreement between calculations (solid lines) and simulations (markers) supports the accuracy of the presented analysis.

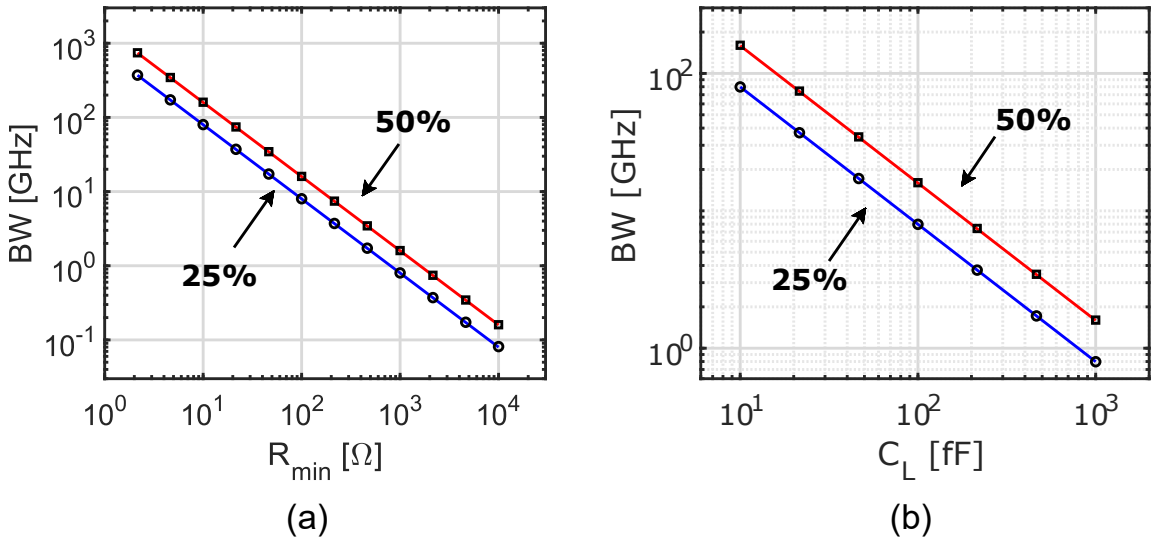


FIGURE 2.8: Mixer bandwidth $BW$: (a) bandwidth vs. $R_{min}$; (b) bandwidth vs. $C_L$. Simulations (markers) are compared with estimates from (2.20).

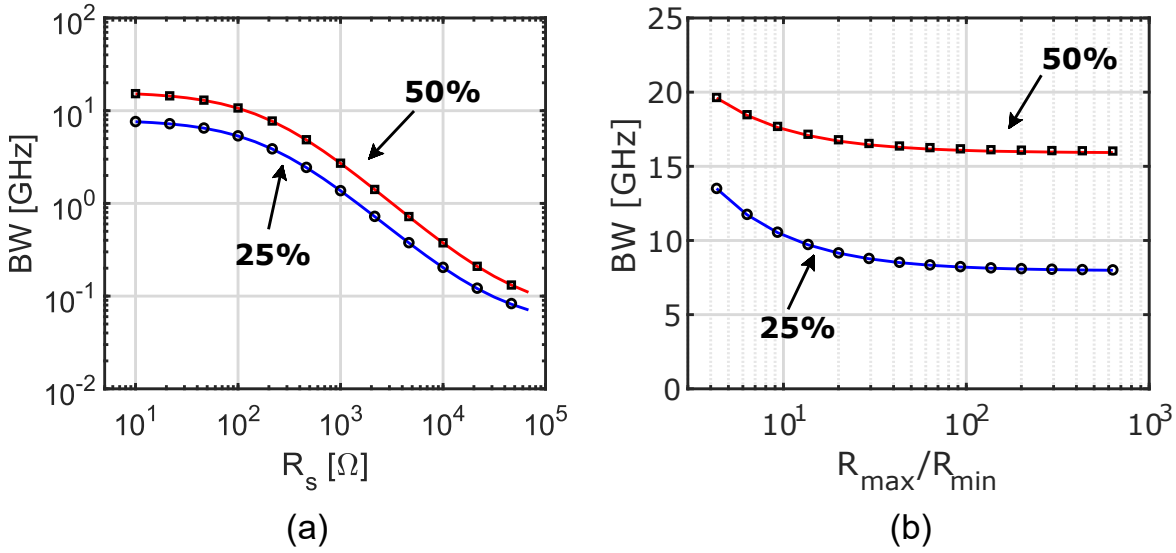


FIGURE 2.9: Mixer bandwidth $BW$: (a) bandwidth vs. $R_s$; (b) bandwidth vs. $R_{max}/R_{min}$. Simulations (markers) are compared with estimates from (2.20).

## 2.4 Remarks on the Time Variant Analysis of the Passive Resistive Mixer

The Thevenin theorem is leveraged in this Chapter to analyse the behavior of an upconversion quadrature passive resistive mixer under more general conditions than previously reported in the literature. The presented analysis takes into account the resistance of the sources driving the mixer, and the finite off-resistance of the switches. The result is that, in practical use cases, an equivalent time invariant circuit can be derived for the open-circuit mixer, that greatly simplifies the analysis of the interaction of the mixer with the load impedance. Simulations confirm the proposed analysis.

# Chapter 3

# Analysis and Design of Reactive Passive Mixers for High-Order Modulation IoT Cartesian Transmitters

The number of Internet-of-Things (IoT) devices is projected to grow relentlessly, fuelled by an increasingly diversified market: multimedia devices, smart sensors, life and health devices, and wearable electronics are only a small set of the possible applications [1–3]. The energy consumption of a IoT device must be kept as low as possible, while its efficiency is to be maximized. Moreover, a IoT device must be able to transmit an ever growing amount of data at data rates that are also increasing [1]. The majority of IoT devices exchange data using narrowband wireless protocols (e.g., ZigBee [34, 35], Bluetooth Low Energy (BLE) [36–39], etc.) and operate in the 2.4 GHz ISM band [3], which effectively limits the symbol rate to a few Mbaud. The low-power constraint favours the adoption of simple modulation schemes (e.g., GFSK, QPSK, 8-DQPSK [40]) that have limited spectral efficiency, whereas high-order QAM modulations are relegated to higher power applications (e.g., WiFi [41], LTE, 5G). However, upcoming IoT applications for multimedia, augmented reality, video streaming, disaster monitoring, etc., require higher data rates and lower latencies [1]. In practice, such a goal can be achieved by increasing the channel bandwidth (i.e., the symbol rate), or by increasing the modulation spectral efficiency using higher-order modulations. The already crowded ISM spectrum makes the former approach inconvenient, leaving the latter as the only viable choice for high data rate applications.

Unlike phase-only modulations such as GFSK or QPSK, high-order QAM modulations encode information in both the phase and the amplitude of the carrier, thus needing a more complex transmitter. There are essentially two possible architectures for a transmitter (TX) supporting QAM modulations: the polar transmitter and the

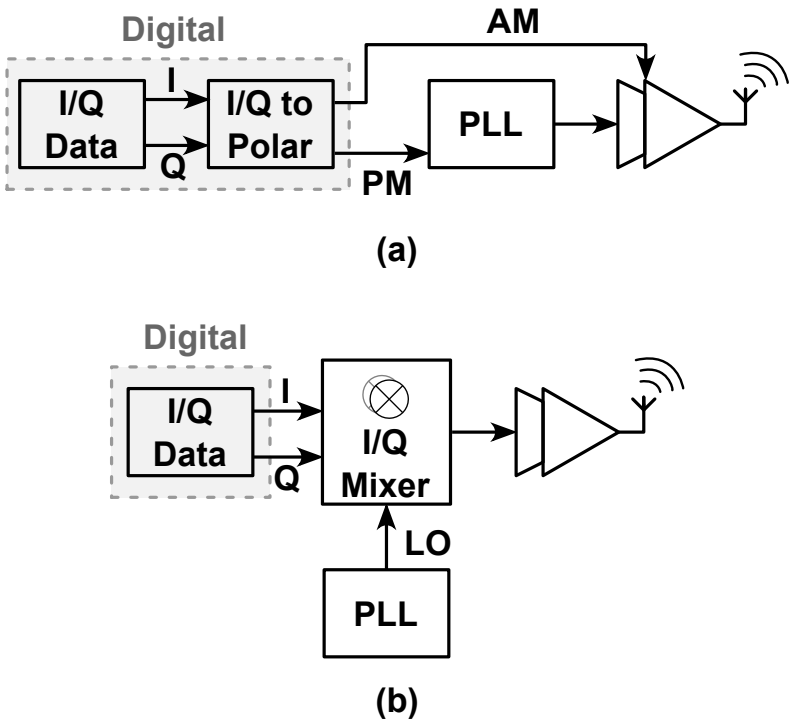


FIGURE 3.1: Transmitter block diagram: (a) polar architecture; (b) Cartesian architecture.

Cartesian transmitter. A block diagram of each architecture is sketched in Fig. 3.1.

The polar architecture, shown in Fig. 3.1(a), is often chosen for low-energy applications [42–46], as it requires a more compact circuitry, and can employ a saturated power amplifier. Both these features lead to a high overall system efficiency. In a polar transmitter, the phase modulation (PM) is realised by modulating the phase-locked loop (PLL) that generates the carrier, while the amplitude modulation (AM) is obtained by modulating the envelope of the signal acting directly on the power amplifier (PA), for example, by modulating the PA supply voltage. The main drawback of the polar architecture stems from the necessity to convert the baseband modulating data from the native in-phase (I) and quadrature (Q) format into a AM/PM (polar) format. The I/Q to AM/PM conversion is a non-linear operation. The result is that the AM and PM modulating signals have a larger bandwidth with respect to the bandwidth of the original I/Q signals, i.e., the symbol rate. This makes the design of the PA and PLL more challenging, and may also lead to unwanted spectral emissions [47, 48]. Moreover, the AM and PM signal paths are quite different, leading to possible synchronisation issues between the two components, and, consequently, to spectral regrowth [49]. Therefore, for high data rate IoT applications, where amplitude and phase modulations are employed to increase the channel capacity, the polar transmitter becomes a less obvious choice.

The other possible transmitter architecture, shown in Fig. 3.1(b), is the Cartesian

transmitter. In this case, the PLL is not modulated, which simplifies its design and implementation. The PA, on the other hand, has to be (highly) linear, a requirement that goes along with reduced efficiency with respect to a saturated PA. The core of the Cartesian transmitter is the I/Q modulator, typically implemented by means of a quadrature (I/Q) mixer. The main drawbacks of the Cartesian architecture are the need of two identical baseband signal paths (namely, the in-phase and quadrature paths), and the presence of an additional block in the chain: the I/Q mixer. As a consequence, for low power applications such as IoT devices, the efficiency of the Cartesian transmitter is ultimately limited by the power consumption of the additional baseband circuitry and the I/Q modulator needed for its operation.

The aim of this work is to present an unconventional I/Q modulator implementation that allows to simplify the baseband circuitry of a IoT Cartesian TX, and the baseband interface to the I/Q modulator, thus drastically limiting the power consumption of these building blocks. As a consequence, the power consumption and the system efficiency of the TX are only limited by the performance of the PA, as it should be in any well designed transmitter. In Section 3.1, an in-depth analysis of the proposed I/Q modulator based on a reactive passive mixer, along with a comparison with a more conventional modulator implementation. In Section 3.2, the design of a proof-of-concept Cartesian transmitter for IoT devices employing the proposed reactive I/Q modulator is presented. The TX operates in the 2.4 GHz ISM band and, thanks to the proposed modulator, is capable of achieving a 22% system efficiency while producing a 9.6 Mb/s 16-QAM modulated signal with a 2.7 dBm average output power. Experimental results on TX prototypes implemented in a 22 nm FD-SOI CMOS technology are presented in Section 3.3, while Section 3.4 concludes the Chapter.

## 3.1 An Efficient I/Q Modulator for IoT Devices

Conventionally, I/Q modulators for Cartesian transmitters are implemented leveraging resistive passive mixers. This is typically the choice for CMOS implementations [34, 35, 50–53]. Conceptual schematics of resistive passive mixers are shown in Fig. 3.2, where the commutating transistors are driven by the local oscillator (LO). Depending on the source/load impedance levels, the resistive passive mixers operate in two regimes: current mode (Fig. 3.2(a)), or voltage mode (Fig. 3.2(b)). In current mode, the mixer is driven by a high impedance source and needs to be loaded by a low impedance load, such as a transimpedance amplifier (TIA). When the mixer is used for upconversion, the TIA operates at high frequency (RF), which implies a

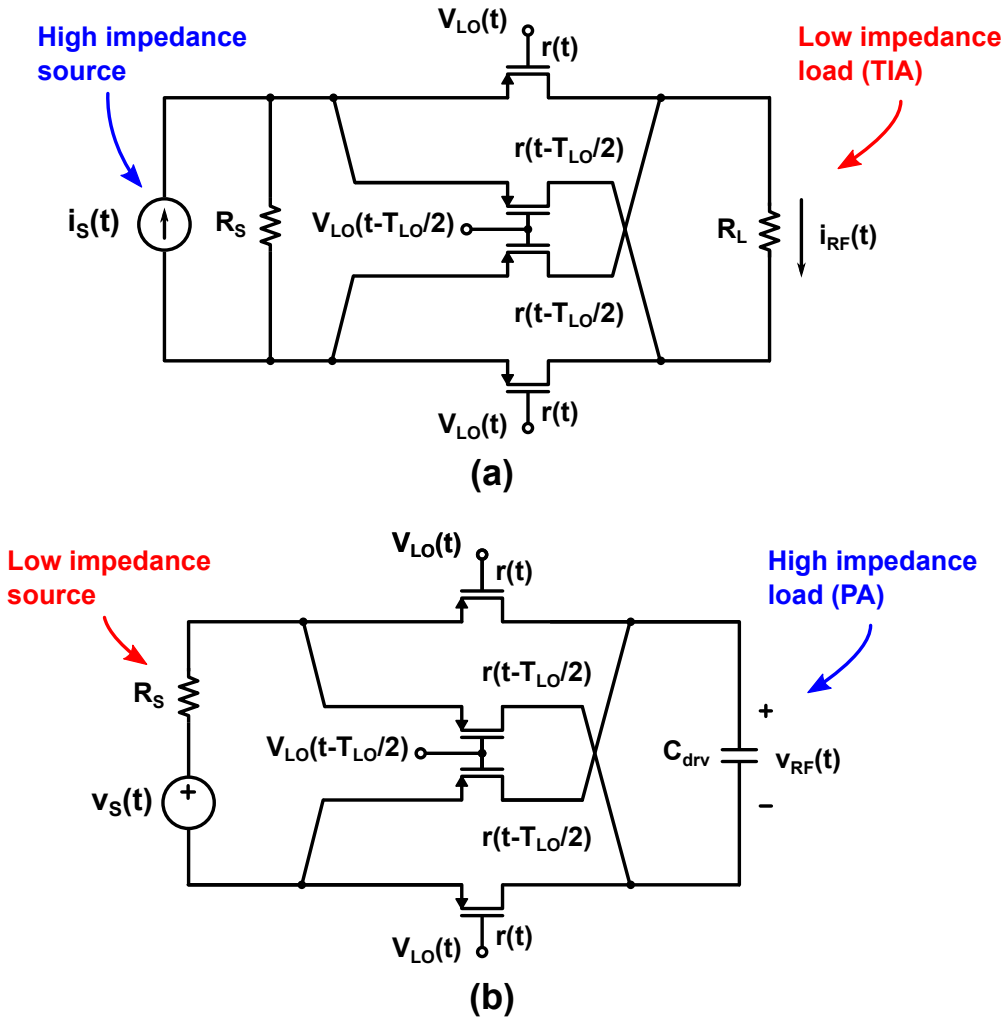


FIGURE 3.2: Simplified schematics of a passive resistive mixer used in: (a) current mode; (b) voltage mode.

relatively large power consumption [34, 50, 53]. Consequently, we disregard this mode of operation for the implementation of a TX for IoT.

In voltage mode, the load impedance of the resistive passive mixer can be high, e.g., it can be the input capacitance of a PA driver amplifier. The source resistance, however, has to be low for the mixer to operate properly in upconversion. As explained in Section 3.1.1, the resistive passive mixer is equivalent to the cascade of a multiplier and a filter, such that the baseband signal is first upconverted, and then filtered. A high source resistance combined with a capacitive load impedance would result in a strong attenuation of the upconverted signal, as shown by the simulation results reported in Section 3.1.3. To drive the mixer with a low source resistance, a buffer stage is usually employed, which complicates the baseband interface and increases the power consumption of the system.

Striving to improve on the system efficiency of a Cartesian transmitter, we resort to reactive passive mixers (Fig. 3.3). Reactive passive mixers based on varactors are

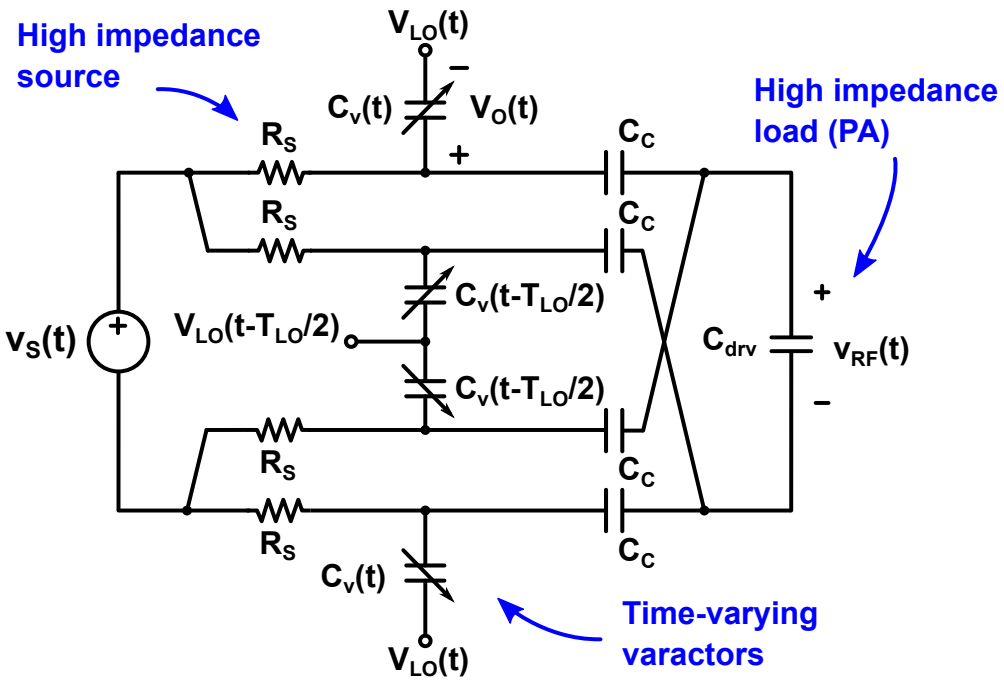


FIGURE 3.3: Simplified schematic of a reactive passive mixer based on varactors.

often used in sub-THz applications [54], where they are able to provide large upconversion gains. However, in the context of low power applications, the key advantage they feature is that they can be loaded by a capacitive impedance, and yet be driven by a high impedance source without incurring in any conversion gain penalty. The reason for this is that, as shown in Section 3.1.2, they are equivalent to the cascade of a filter and a multiplier, such that the baseband signal is first filtered, and then upconverted. The bandwidth of this equivalent filter has to be comparable to the symbol rate; it does not need to be larger than the carrier frequency. Therefore, the filtering action does not impair the upconversion gain. On the contrary, the interface between the I/Q modulator and preceding digital-to-analog converters (DACs) is strongly simplified: no buffer is needed, while the equivalent baseband filter of the reactive passive mixer can be actually used as a reconstruction filter, avoiding the need of an explicit circuit. Overall, by removing the need for additional building blocks, using reactive passive mixers yields both power and area savings with respect to the conventional implementation of a I/Q modulator based on resistive passive mixers.

### 3.1.1 Analysis of the Resistive Passive Mixer

The analysis of the resistive passive mixer is the subject of several works in the literature [29–32] and is also discussed in depth in Chapter 2. In particular, in [29] and

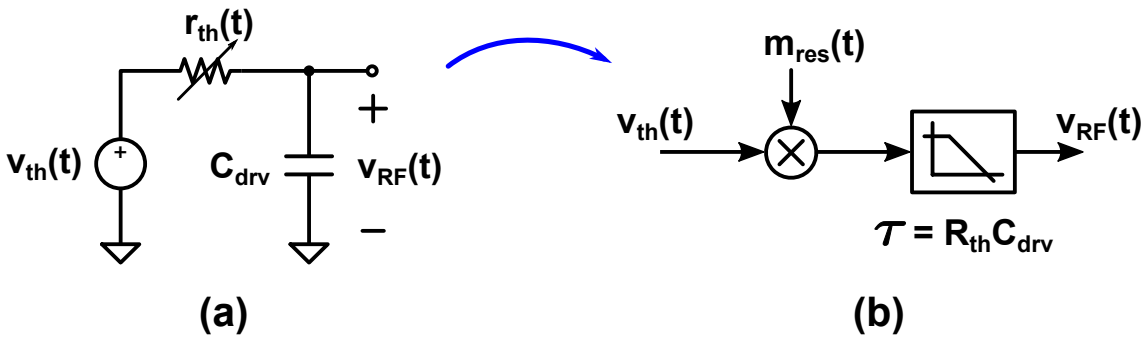


FIGURE 3.4: Analysis of the resistive passive mixer: (a) Thevenin equivalent circuit; (b) block diagram of the signal flow: the baseband signal is first upconverted, then filtered.

as discussed in Chapter 2, the circuit in Fig. 3.2 is analysed by deriving a Thevenin equivalent circuit for the combination of the source and the commutating transistors. For an easier comparison with the reactive passive mixer, here are reported the main results.

The transistors are modelled as time-varying resistances, $r(t)$, that alternate between a maximum value $R_{max}$ (switch off-resistance) and a minimum value $R_{min}$ (switch on-resistance) at the LO frequency.

As discussed in Chapter 2, the Thevenin equivalent resistance $r_{th}(t)$ is time-varying, as illustrated in Fig. 3.4(a):

$$r_{th}(t) = \frac{2r(t)r(t - T_{LO}/2) + r(t)R_s + r(t - T_{LO}/2)R_s}{r(t) + r(t - T_{LO}/2) + 2R_s} \tag{3.1}$$

$T_{LO}$ being the LO period. However, for resistance waveforms $r(t)$ of practical interest, $r_{th}(t)$ becomes a constant. This is, for example, the case when the mixer is driven by a LO with a 50% duty-cycle, and the transistors (i.e., the switches) spend equal time on and off. In this case, (3.1) simplifies to

$$R_{th} = \frac{2R_{max}R_{min} + R_{max}R_s + R_{min}R_s}{R_{max} + R_{min} + 2R_s} \tag{3.2}$$

Hence, the Thevenin equivalent of the resistive passive mixer becomes a time-invariant circuit, which greatly simplifies the analysis of the interaction of the mixer with the load impedance.

The equivalent Thevenin voltage source is

$$v_{th}(t) = \frac{r(t - T_{LO}/2) - r(t)}{2R_s + r(t) + r(t - T_{LO}/2)} v_s(t) = m_{\text{res}}(t)v_s(t) \tag{3.3}$$

where $m_{\text{res}}(t)$ is the modulating function for the resistive mixer. The baseband input

signal, $v_s(t)$, is upconverted by $m_{\text{res}}(t)$ into the sidebands of $v_{th}(t)$. Then, $v_{th}(t)$ is filtered by the network made by $R_{th}$ and the load impedance to produce the output signal $v_{\text{RF}}(t)$. In Fig. 3.4, the case of a capacitive load, i.e., the circuit in Fig. 3.2(b), is illustrated. The bottom line is that, in the resistive passive mixer, the baseband signal is first upconverted, and then filtered, as shown by the block diagram in Fig. 3.4(b).

The foregoing analysis can be expanded to the case two resistive passive mixers are combined in a I/Q modulator. The I/Q modulator conversion gain found in Chapter 2 is:

$$A_{v,\text{res}}(j(\omega_{LO}+\omega_s)) = \frac{A_{v0,\text{res}}}{1+j(\omega_{LO}+\omega_s)R_{th}^{I/Q}C_{drv}} \tag{3.4}$$

where $\omega_{LO}$ and $\omega_s$ are the frequencies of the LO and $v_s(t)$ (assumed to be a test tone), respectively,

$$A_{v0,\text{res}} = \frac{2}{\pi}\cdot\frac{1-\frac{R_{min}}{R_{max}}}{1+\frac{R_{min}}{R_{max}}+\frac{2R_s}{R_{max}}} \tag{3.5}$$

and

$$R_{th}^{I/Q} = \frac{1}{2}\frac{2R_{min}+R_s\left(1+\frac{R_{min}}{R_{max}}\right)}{1+\frac{R_{min}}{R_{max}}+\frac{2R_s}{R_{max}}} \tag{3.6}$$

Equation (3.4) remarks that, if the resistive passive mixer is capacitively loaded and driven by a high impedance source (i.e., $R_{th}^{I/Q}$ is large), the equivalent first-order R-C filter might impair the mixer gain, heavily attenuating the upconverted signal.

### 3.1.2 Analysis of the Reactive Passive Mixer

The analysis of the reactive passive mixer starts from the schematic in Fig. 3.3. The varactors are the time-variant elements that operate the upconversion. In Fig. 3.3, one should notice that both terminals of $C_{drv}$ are virtual grounds for the LO signal, $V_{LO}(t)$. Consequently, there is no LO feedthrough to the output signal, $v_{RF}(t)$. The voltage across the varactor, $V_O(t)$ in Fig. 3.3, is made of a large-signal component, namely the LO signal attenuated by the non-linear capacitive divider made of the varactor capacitance and $C_C$, and a small perturbation, $v_O(t)$, which is due to the upconversion of the baseband input signal, $v_s(t)$. The differential circuit in Fig. 3.3 can be analyzed using its equivalent half-circuit, shown in Fig. 3.5(a). The upconverted output signal, $v_{RF}(t)$, is related to the small-signal $v_O(t)$ as

$$v_{RF}(t) = \frac{C_C}{2C_C+2C_{drv}}\left[v_O(t)-v_O(t-T_{LO}/2)\right] \tag{3.7}$$

To obtain the relationship between $v_s(t)$ and $v_O(t)$, we proceed as in [55]. We

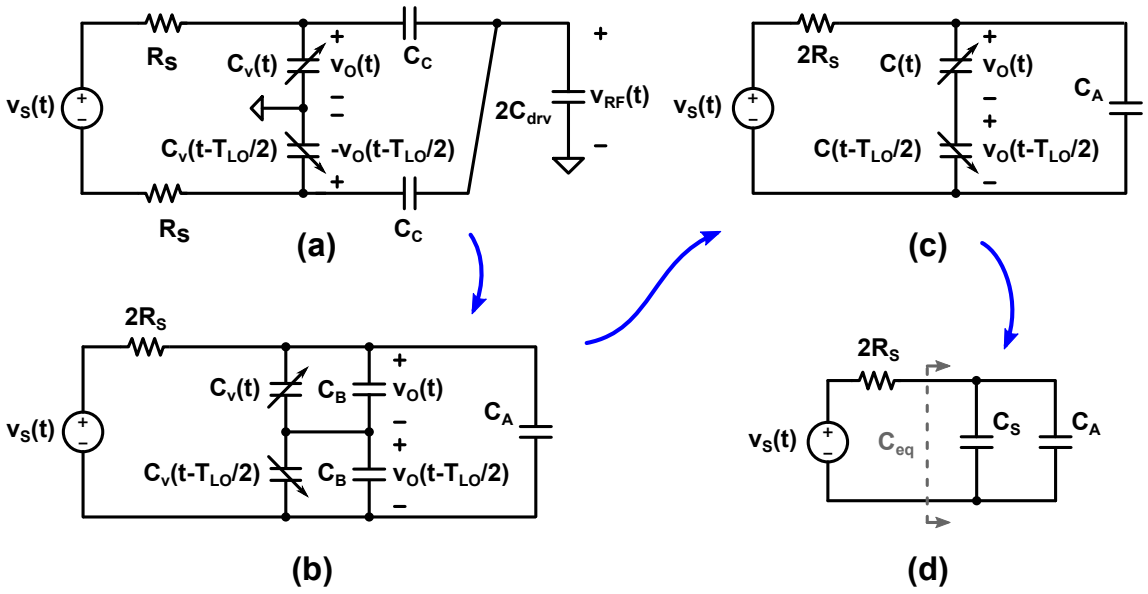


FIGURE 3.5: Analysis of the reactive passive mixer: (a) equivalent half-circuit of the mixer in Fig. 3.3; (b) star-delta transformation of $C_C$ and $C_{drv}$ network; (c) further simplification of the network; (d) equivalent linear time-invariant circuit.

compute the incremental charge, $q_v(t)$, stored in the varactor, and due to the small-signal $v_O(t)$, as

$$q_v(t) = C_v(t) \cdot v_O(t) \tag{3.8}$$

where $C_v(t)$ is the incremental varactor capacitance computed around the time-varying operating point set by the LO signal. The network in Fig. 3.5(a) is then rearranged as in Fig. 3.5(b) by transforming the star network made of capacitors $C_C$ and $2C_{drv}$ in its equivalent delta network:

$$C_A = \frac{C_C^2}{(2C_C + 2C_{drv})} \tag{3.9}$$

$$C_B = \frac{C_C C_{drv}}{(C_C + C_{drv})} \tag{3.10}$$

We take into account the parallel combination of $C_B$ and $C_v(t)$ in Fig. 3.5(b) by computing the total incremental charge stored by the two capacitors, $q(t)$, as:

$$q(t) = [C_v(t) + C_B] \cdot v_O(t) = C(t) \cdot v_O(t) \tag{3.11}$$

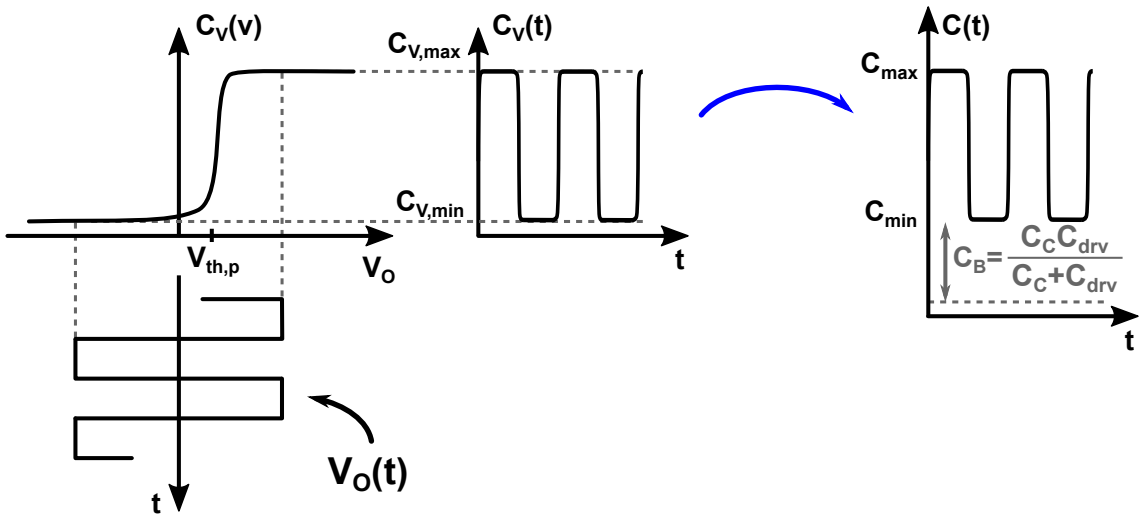


FIGURE 3.6: Waveform of the varactor capacitance, $C_v(t)$, and waveform of the overall time-varying capacitance of the reactive passive mixer, $C(t)$.

The parallel combination of $C_B$ and $C_v(t - T_{LO}/2)$ in Fig. 3.5(b) is in series with $C(t)$. Thus, it stores the same incremental charge, $q(t)$. Consequently:

$$\begin{aligned} q(t) &= [C_v(t - T_{LO}/2) + C_B] \cdot v_O(t - T_{LO}/2) \\ &= C(t - T_{LO}/2) \cdot v_O(t - T_{LO}/2) \end{aligned} \tag{3.12}$$

The result of the foregoing manipulations is the equivalent linear time-variant network in Fig. 3.5(c).

Now we assume that the C-V characteristic of the varactor is monotonic, with a sharp transition between the maximum ($C_{v,max}$) and minimum ($C_{v,min}$) value of capacitance. If the LO signal is a square wave with a 50% duty-cycle, then $C_v(t)$ will be likewise. Moreover, $C(t)$ in (3.11) will also feature the same waveform, alternating between $C_{max} = C_{v,max} + C_c C_{drv}/(C_c + C_{drv})$ and $C_{min} = C_{v,min} + C_c C_{drv}/(C_c + C_{drv})$, as shown in Fig. 3.6. Notice that $C(t - T_{LO}/2)$ in (3.12) will be equal to $C_{max}$ when $C(t)$ is equal to $C_{min}$, and viceversa. As a consequence, the series combination, $C_S$, of $C(t)$ and $C(t - T_{LO}/2)$ in Fig. 3.5(c) is time invariant

$$C_S = \frac{C_{max} C_{min}}{C_{max} + C_{min}} \tag{3.13}$$

as sketched in Fig. 3.5(d).

The linear time-invariant equivalent circuit in Fig. 3.5(d) makes it easy to relate the incremental charge stored in the time-varying capacitors $q(t)$ to the baseband

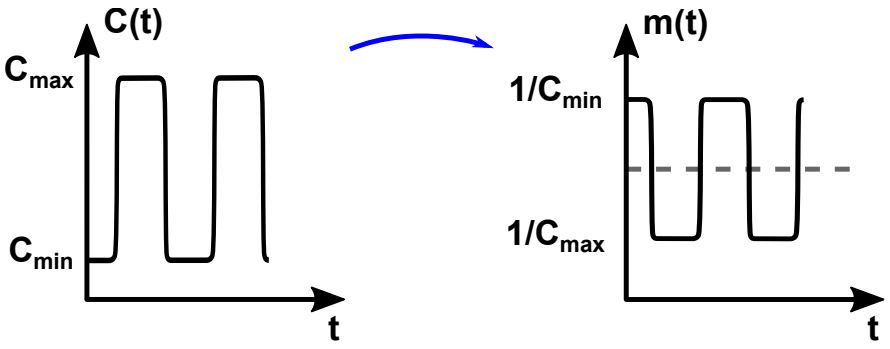


FIGURE 3.7: Sketch of the $C(t)$ waveform, and corresponding waveform of the modulating function, $m_I(t)$.

voltage $v_s(t)$ by means of a filter with frequency response

$$H_q(j\omega_s) = \frac{C_S}{1 + j\omega_s 2R_s C_{\text{eq}}} \tag{3.14}$$

where

$$C_{\text{eq}} = C_S + C_A = \frac{C_{max}C_{min}}{C_{max} + C_{min}} + \frac{C_C^2}{2C_C + 2C_{drv}} \tag{3.15}$$

Having obtained the charge stored in the time-varying capacitors, we now compute $v_O(t)$ and $v_O(t - T_{LO}/2)$ using (3.11) and (3.12), which can be conveniently recast as

$$v_O(t) = \frac{q(t)}{C(t)} \tag{3.16}$$

$$v_O(t - T_{LO}/2) = \frac{q(t)}{C(t - T_{LO}/2)} \tag{3.17}$$

We define the modulating function $m(t)$ and we expand it in Fourier series as

$$m(t) = \frac{1}{C(t)} = \sum_{k=-\infty}^{\infty} M_k e^{jk\omega_{LO}t} \tag{3.18}$$

Since the waveform of $C(t)$ is a square wave with 50% duty-cycle, so it is $m(t)$ in (3.18), with minimum value $1/C_{max}$ and maximum value $1/C_{min}$, as sketched in Fig. 3.7. Consequently,

$$M_1 = \frac{2}{\pi}\frac{C_{max} - C_{min}}{C_{max}C_{min}} \tag{3.19}$$

Using (3.14), (3.16)-(3.19), the fact that

$$m(t - T_{LO}/2) = \frac{1}{C(t - T_{LO}/2)} = \sum_{k=-\infty}^{\infty} (-1)^k M_k e^{jk\omega_{LO}t} \tag{3.20}$$

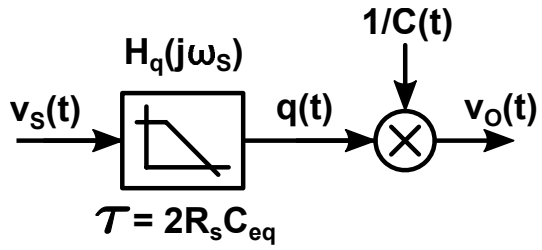


FIGURE 3.8: Signal flow block diagram of the reactive passive mixer: the baseband signal is first filtered, then upconverted.

and (3.7), the conversion gain of the reactive passive mixer is computed as

$$A^m_{v,\text{var}}(j(\omega_{\text{LO}}+\omega_s)) = \frac{A^m_{v0,\text{var}}}{1+j\omega_s 2R_sC_{\text{eq}}} \tag{3.21}$$

where

$$A^m_{v0,\text{var}} = \frac{2}{\pi}\frac{\frac{C_{v,max}}{C_{v,min}}-1}{\left(\frac{C_{v,max}}{C_{v,min}}+1\right)\left(\frac{C_{drv}}{C_c}+1\right)+\frac{2C_{drv}}{C_{v,min}}} \tag{3.22}$$

The foregoing analysis shows that, in the reactive passive mixer, the input baseband signal, $v_s(t)$, is first filtered, and then upconverted into $v_O(t)$, as illustrated in Fig. 3.8. The upconverted output signal, $v_{RF}(t)$, is then simply proportional to $v_O(t)$, as shown by (3.7). This behavior is in sharp contrast with the behavior of the resistive passive mixer discussed in Section 3.1.1. The reactive passive mixer can be driven by a high impedance source and can be loaded by a capacitive impedance because the fltering action (with bandwidth $1/(2R_sC_{\text{eq}})$) takes place at baseband, not impairing the upconversion gain. The conversion gain increases as the ratio between the maximum ($C_{v,max}$) and minimum ($C_{v,min}$) capacitance of the varactor increases, until reaching the upper bound for $A^m_{v,\text{var}}$, that is, $2/\pi$. The modulator load capacitance, $C_{drv}$, decreases $A^m_{v,\text{var}}$ as it loads the varactor, effectively reducing the capacitance variation.

The analysis is now readily extended to an I/Q modulator made of two reactive passive mixers driven by quadrature LO signals. The equivalent half-circuit of the the I/Q modulator is shown in Fig. 3.9(a). The main difference with the analysis of the circuit in Fig. 3.3 is the loading effect of one reactive passive mixer on the other. The latter can be evaluated with the help of Fig. 3.9(b), where

$$C_Q = \frac{C_{v,min}C_C}{C_{v,min}+C_C}+\frac{C_{v,max}C_C}{C_{v,max}+C_C} \tag{3.23}$$

Therefore, (3.7) and (3.15) can be rather promptly adapted by replacing the term $2C_{drv}$ with $2C_{drv}+C_Q$. Moreover, given the symmetry of the circuit, $C_I = C_Q$. Using

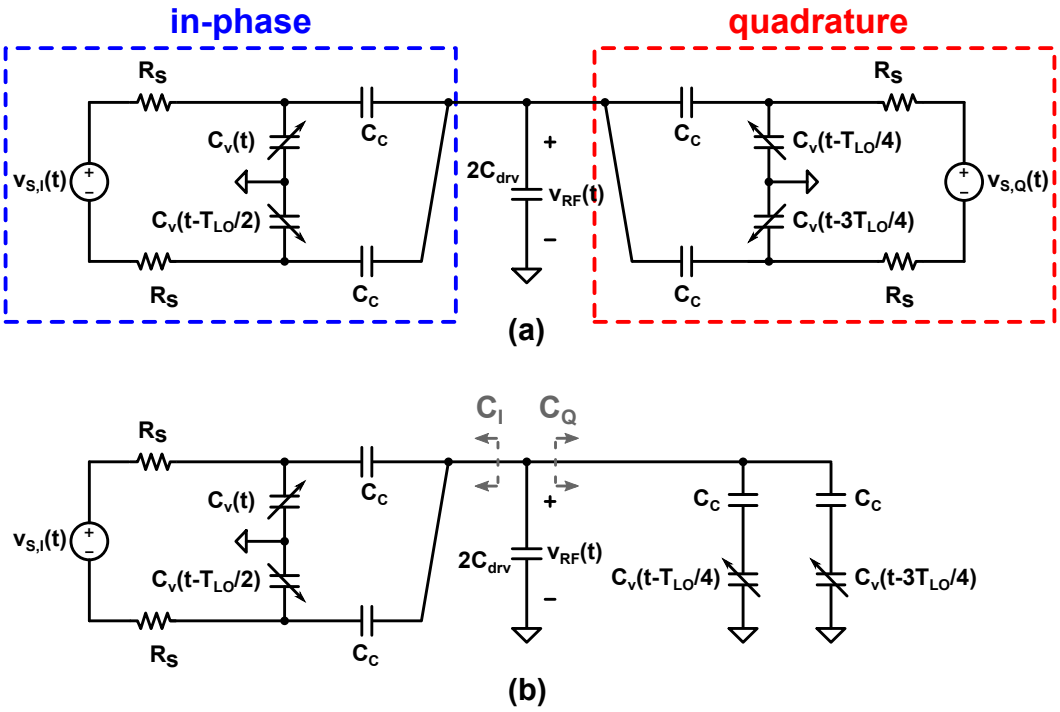


FIGURE 3.9: Analysis of the reactive I/Q modulator: (a) equivalent half-circuit; (b) schematic for the evaluation of $C_{Q(I)}$.

this, and leveraging linear superposition, the conversion gain of the I/Q modulator based on the reactive passive mixers is obtained as

$$A_{v,\text{var}}(j(\omega_{\text{LO}}+\omega_s)) = \frac{A_{v0,\text{var}}}{1+j\omega_s 2R_s C_{\text{eq}}^{I/Q}} \tag{3.24}$$

where

$$A_{v0,\text{var}} = \frac{4}{\pi}\frac{\frac{C_{v,max}}{C_{v,min}}-1}{\left(\frac{C_{v,max}}{C_{v,min}}+1\right)\left(\frac{2C_{drv}+C_Q}{2C_c}+1\right)+\frac{2C_{drv}+C_Q}{C_{v,min}}} \tag{3.25}$$

and $C_{eq}^{I/Q}$ is given by (3.15), adjusted for the additional load $C_{Q(I)}$.

At first glance, (3.25) might deceive into thinking that the maximum conversion gain of the reactive I/Q modulator is $4/\pi$, but this is not the case. Assuming negligible $C_{drv}$, and very large $C_C$, $2C_{drv}+C_{Q(I)} \approx C_{v,max}+C_{v,min}$, and, consequently, $A_{v0,\text{var}} \approx 2/\pi \cdot (C_{v,max}-C_{v,min})/(C_{v,max}+C_{v,min})$, that is, the same result as given by (3.22) for nil $C_{drv}$. In other words, the loading effect of one reactive passive mixer on the other is to halve the conversion gain; such a gain loss is however compensated by the superposition of the upconverted in-phase and quadrature baseband signals.

### 3.1.3 Resistive vs. Reactive Passive Mixer

To put the analysis presented in Sections 3.1.1 and 3.1.2 in perspective, some simulations results, based on the design reported in Section 3.2, are anticipated. A comparison between a I/Q modulator based on conventional resistive passive mixers, and the proposed I/Q modulator based on reactive passive mixers is carried out. The same circuit, whose parameters are discussed in Section 3.2, is used for both modulators: the only difference is that the transistors that are used as switches in the resistive passive mixer are turned into varactors by connecting together the source and drain terminals in the reactive passive mixer (see Fig. 3.14). Both modulators are driven by the same high impedance source, which is a combination of the output impedance of the baseband DACs and explicit resistors, and are loaded by the same capacitive load, namely the input capacitance of the PA driver, $C_{drv}$. The comparison aims at emphasizing the impact of the different filtering action in the I/Q modulator signal flow: after upconversion in the resistive passive mixer; before upconversion in the reactive passive mixer.

Using the circuit parameters reported in Section 3.2, the cutoff frequencies of $A_{v,\text{res}}$ and $A_{v,\text{var}}$ are evaluated using (3.4) and (3.24), respectively, to be around 10 MHz for the resistive mixer, and around 4 MHz for the reactive mixer. In the Cartesian TX presented in Section 3.2, the symbol rate is up to 2.4 Mbaud and the carrier frequency is 2.4 GHz. Hence, while the baseband signal is within the passband of the reactive mixer, it is completely out-of-band for the resistive mixer, since, in the latter, the filtering action takes place after upconversion. As the in-band gain is comparable for the two modulators, that is, $A_{v0,\text{res}} \approx A_{v0,\text{var}}$, from (3.4) we expect the conversion gain of the resistive mixer to be some $20\log_{10}(2.4 \cdot 10^9/10 \cdot 10^6) = 47$ dB lower than that of the reactive mixer.

Figure 3.10 shows the simulated output power of the Cartesian TX presented in Section 3.2 vs. the input code of the baseband DACs for both the TX with the reactive mixer (blue curve) and the one with the conventional resistive mixer (red curve). It is clear that a conventional resistive mixer is not compatible with a high impedance signal source, and that the analytical estimate of the loss in conversion gain we carried out is quite close to the simulation result.

### 3.1.4 Linearity of the Reactive Passive Mixer

A very efficient modulator is of little use if it has a very small linear dynamic range. The analysis reported in Section 3.1.2 shows that the upconversion gain of the reactive passive mixer depends on the varactor capacitance waveform $C_v(t)$. The latter,

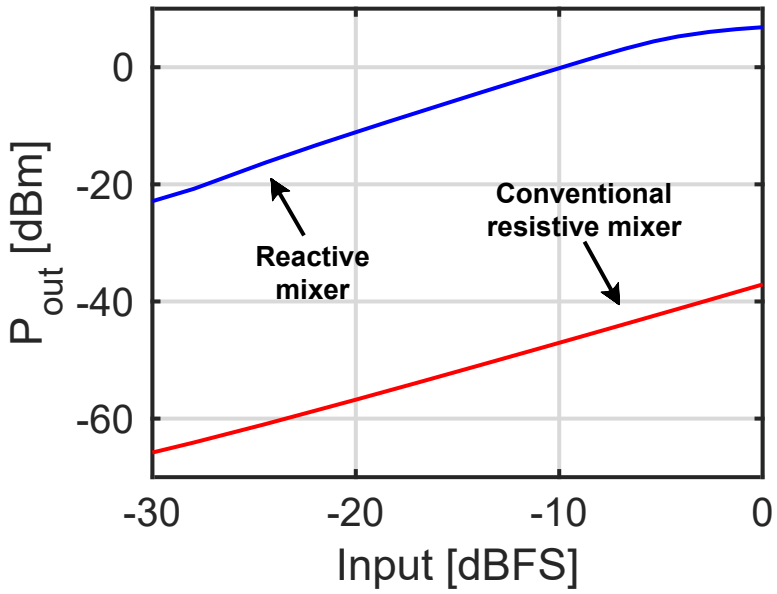


FIGURE 3.10: Simulated output power of the Cartesian TX discussed in Section 3.2 with the proposed reactive mixer (blue curve) and a conventional passive resistive mixer (red line).

in general, depends on the varactor C-V characteristic, the LO signal, and the baseband signal. The sharper the transition between $C_{v,min}$ and $C_{v,max}$ in the C-V characteristic of the varactor, the better the linearity of the mixer. This can be intuitively appreciated with the help of the sketch in Fig. 3.11. With a sharp C-V curve, the varactor capacitance waveform, $C_v(t)$, is less sensitive on the baseband signal, allowing for a higher dynamic range. Basically, the conversion gain is unchanged until the amplitude of the baseband signal becomes comparable to the amplitude of the LO signal, thus affecting $C_v(t)$. In Fig. 3.12 the simulated upconverted output voltage of the reactive mixer is reported versus the DAC input code: the 1 dB compression point is only reached for a full-scale I and Q signal.

## 3.2 Design of a IoT Cartesian Transmitter Based on a Reactive I/Q Modulator

To verify the effectiveness of the reactive I/Q modulator proposed in Section 3.1, a Cartesian transmitter is designed in a 22 nm FD-SOI CMOS technology for operation in the 2.4 GHz ISM band. The target peak output power is about 8 dBm. The TX should support high-order modulations, such as 16-QAM.

The block diagram of the proposed Cartesian TX is shown in Fig. 3.13. The reactive I/Q modulator is directly fed by a pair of 8-bit pseudo-differential R-2R DACs without any other active stage in-between. A unit resistance R of 10 kΩ is chosen to

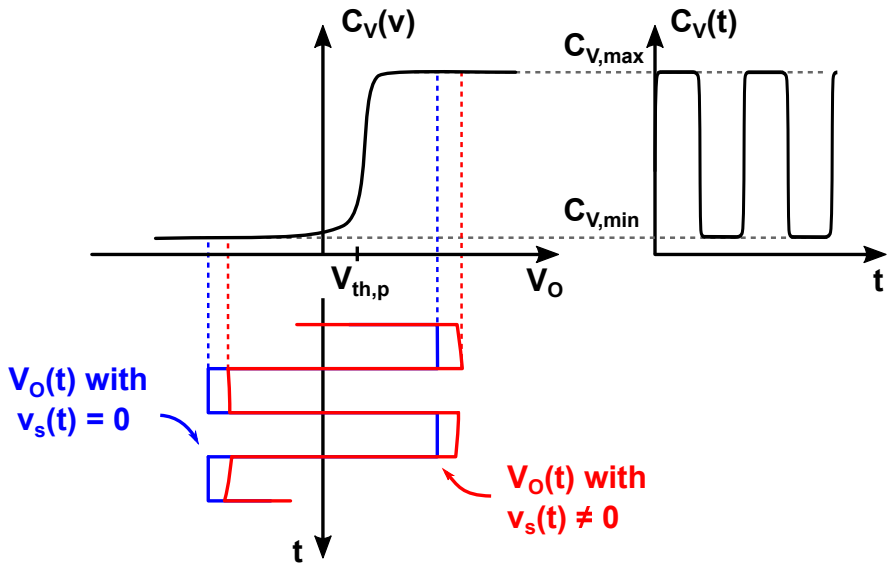


FIGURE 3.11: Sketch of the voltage across the mixer varactors and varactor capacitance waveform.

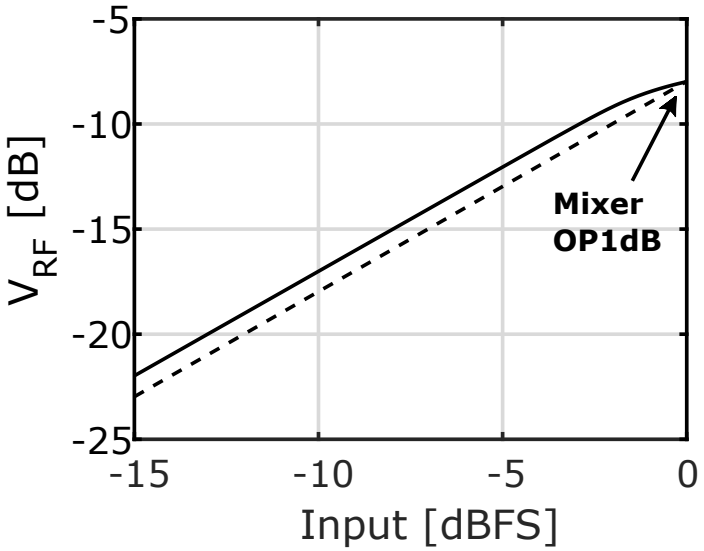


FIGURE 3.12: Simulated mixer output voltage vs. input DAC word.

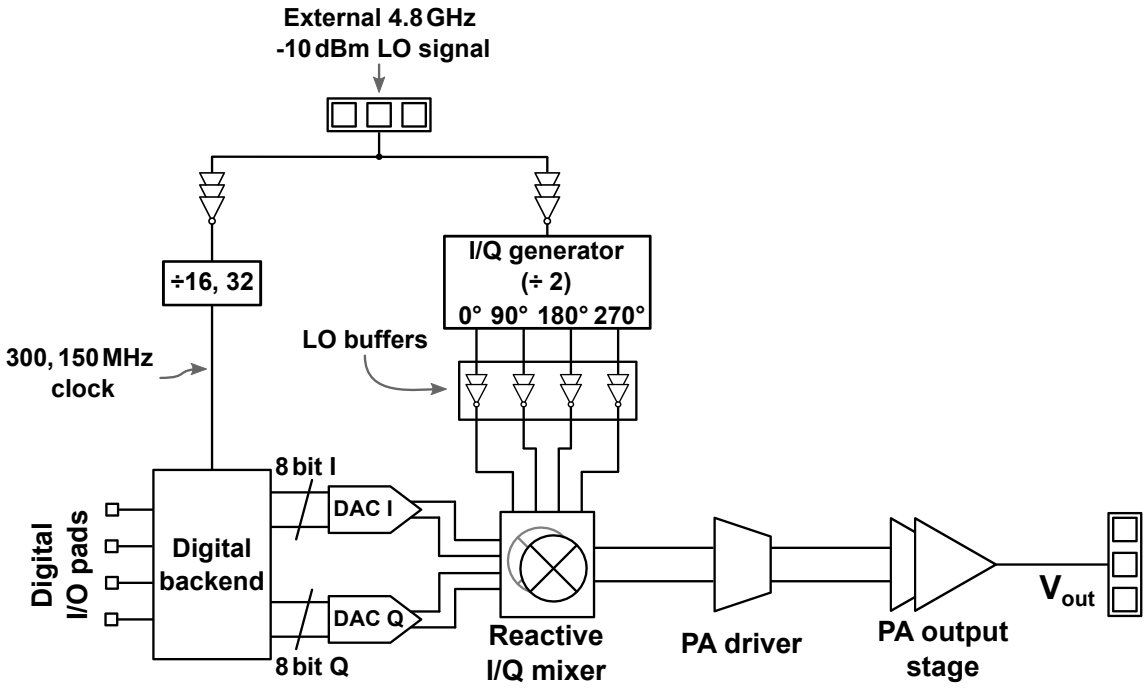


FIGURE 3.13: Block diagram of the proposed 2.4 GHz Cartesian transmitter based on reactive passive mixers.

limit the power consumption of each DAC to about 100 $\mu$W. An external LO signal is fed to the system at twice the carrier frequency (4.8 GHz). An integrated clock divider by two generates the quadrature sequence (i.e, a 4-phase LO signal) necessary to drive the reactive I/Q modulator. The external LO signal also drives a programmable divider that clocks both the digital backed and the DACs at 150 or 300 MHz (Fig. 3.13). The included simple digital backend contains a 8-bit rolling register capable of storing 1k-symbols. The data is loaded offline and then looped, giving the flexibility to test various modulation formats. The symbol rate can be set to 1.2 or 2.4 Mbaud by changing the division ratio of the programmable divider. Two integrated digital pulse-shaping interpolation filters (interpolation ratio equal to 128) process the symbols and drive the in-phase and quadrature DACs.

The reactive passive mixers used in the proposed I/Q modulator (Fig. 3.14) are based on inversion-mode pMOS varactors for sharper transition between $C_{v,min}$ and $C_{v,max}$. Due to the use of a FD-SOI technology in this design, the accumulation region is avoided in the used varactor (the bulk is isolated), and the C-V characteristic is monotonic. The implemented mixer is double-balanced: $V_{RF,p}$ and $V_{RF,n}$ in Fig. 3.14, are ac-grounds for the odd harmonics of the local oscillator (LO), while the 2$^{nd}$ harmonics of the in-phase and quadrature LO signals cancel each other at nodes $V_{RF,p}$ and $V_{RF,n}$. The filter-before-upconversion feature of the reactive passive mixer discussed in Section 3.1.2 is exploited as a reconstruction filter for the DAC signal. Additional resistors $R_A = 90\,k\Omega$ set the bandwidth of the mixer equivalent

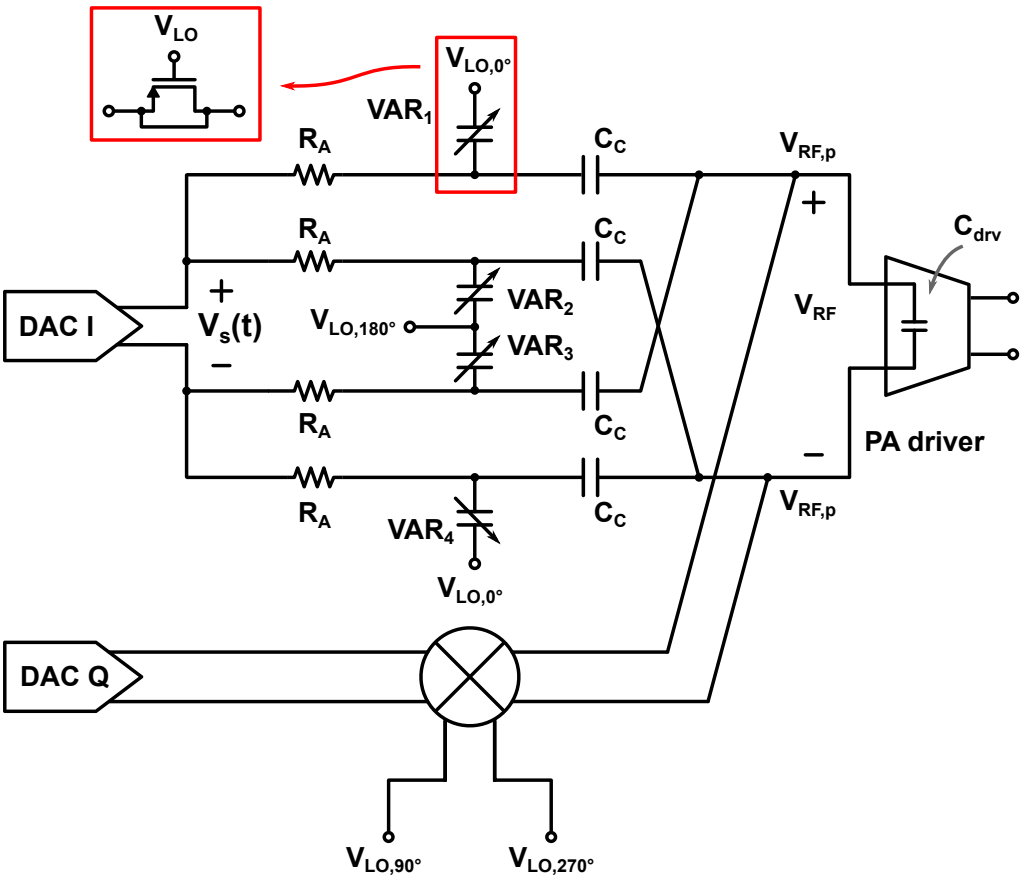


FIGURE 3.14: Proposed reactive mixer schematic.

R-C filter to 4 MHz (Fig. 3.14).

The modulated signal is amplified by a two-stage PA, whose output feeds the antenna port (Fig. 3.13). The schematic of the PA driver stage is shown in Fig. 3.15. The PA driver is a class-A fully differential amplifier with a tuned load. The inductance in the load resonator is made of two 3 nH coils ($L_1$ in Fig. 3.15). The quality factor of the load resonator is about 10. The input common mode voltage of the PA driver, $V_{\text{bias,drv}}$, is generated by a simple bias circuit, as shown in Fig. 3.15.

The PA output stage is a class-AB pseudo-differential design. Its simplified schematic is depicted in Fig. 3.16. A complementary topology is used to fully exploit the reduced supply of ultra-scaled CMOS technologies (0.8 V in this design) without incurring in any reliability issue related to the voltage stress of the transistors. The output stage makes use of neutralization capacitors ($C_7$–$C_{10}$ in Fig. 3.16) for improved stability against load and PVT variation. The PA output stage is loaded by a doubly-tuned transformer matching network, that also implements differential-to-single-ended conversion. The inductance of the primary and secondary windings are 1.15 nH. The transformer is implemented with the thickest traces available in the metal stack. A stacked layout is used to maximize the magnetic coupling factor

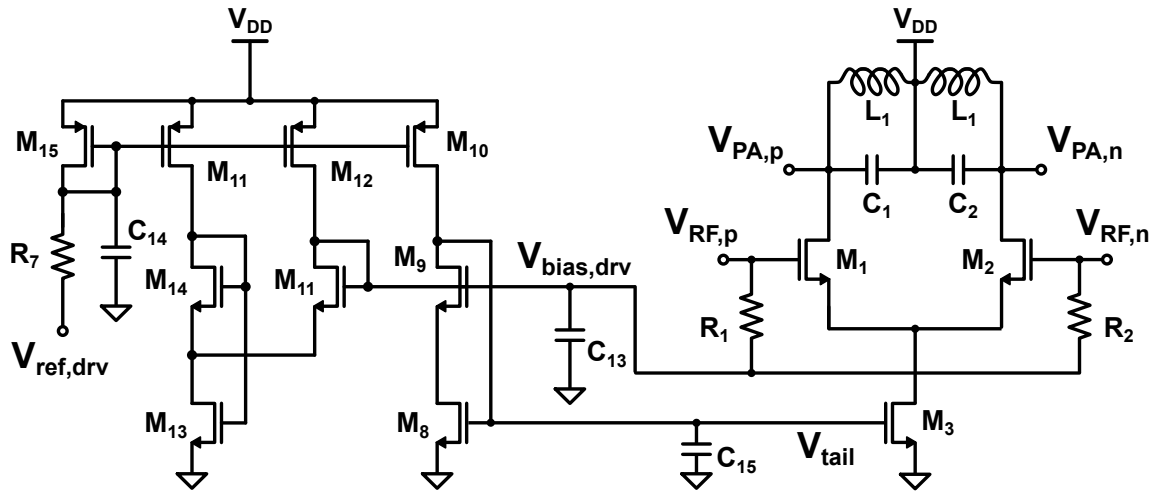


FIGURE 3.15: Transistor level schematic of the PA driver stage.

($k = 0.89$) and, consequently, minimize the losses in the PA output network, as discussed in [56,57]. Two capacitors shunt the primary and secondary coils and set the resonance of the network to $f_{LO} = 2.4\,\text{GHz}$.

### 3.2.1 Optimization of the Reactive I/Q Modulator-PA Driver Cascade

For a given peak output power, the PA output stage is designed for maximum efficiency. The PA output stage needs a sufficiently large input signal to be able to deliver the peak power to the output port. This sets a requirement on the overall gain of the cascade of the reactive I/Q modulator and the PA driver. It is not straighforward to single out the optimal gain partition between the I/Q modulator and PA driver. The PA driver and the reactive passive mixer are sized with the goal of minimizing the power consumption of the cascade, while ensuring that a signal large enough is provided to the PA output stage. Moreover, these blocks must be designed such that the linearity of the overall TX chain is limited by the PA output stage.

To find the optimal sizing of the I/Q modulator and PA driver cascade, we start by observing that both the gain and the power consumption of the PA driver are approximately proportional to its input capacitance, $C_{drv}$. The reactive mixer is passive. However, dynamic power is dissipated at the LO port by the inverters that drive the varactor gates. The amount of dynamic power dissipated by the 8 LO drivers is

$$P_{d,LO} = 8V_{DD}^2 C_{in,LO} f_{LO} \tag{3.26}$$

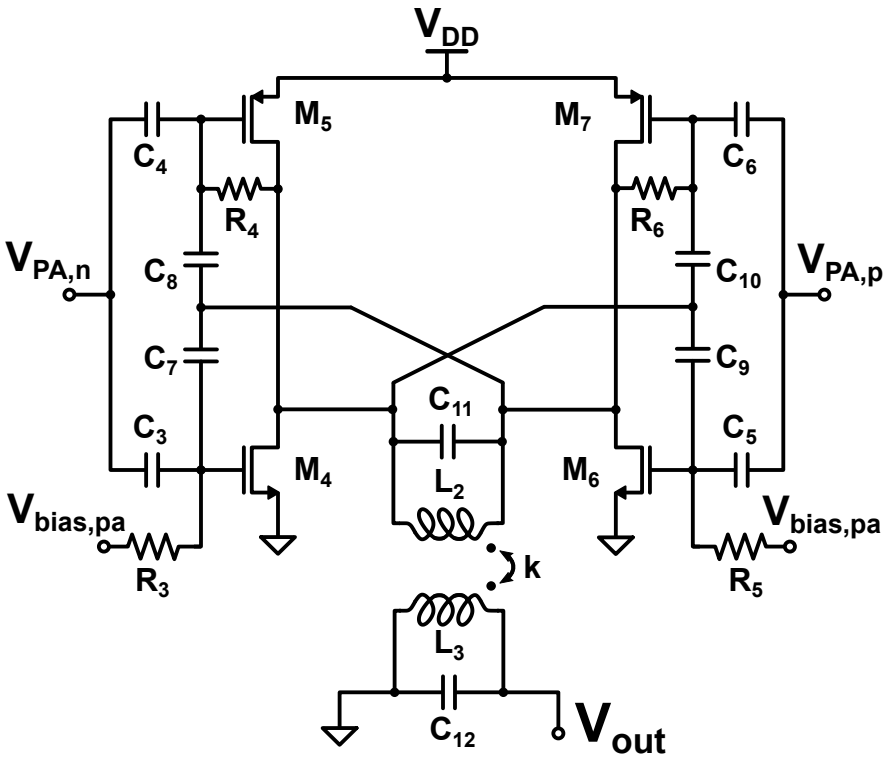


FIGURE 3.16: Transistor level schematic of the class AB differential PA output stage.

where $V_{DD}$ is the supply voltage, and $C_{in,LO}$ is the equivalent capacitance driven by each inverter. $C_{in,LO}$ is made of the series combination of the non-linear varactor capacitance and $C_C$ (recall that $C_{drv}$ is at virtual ground for the LO), making it dependent of the varactor sizing. A worst-case approximation of $C_{in,LO}$ is $C_{in,LO} = C_{v,max}C_C/(C_{v,max} + C_C)$. Such an approximation tends to overstimate $C_{in,LO}$; this is anyway acceptable to derive a guideline for the mixer sizing.

For a given mixer upconversion gain, and a given capacitance ratio $C_{v,max}/C_{v,min}$, (3.25) shows that if $C_{drv}$ is increased, then both the varactor capacitance and $C_C$ have to increase as well. Therefore, $C_{in,LO}$ increases alongside $C_{drv}$, which results in an increase of $P_{d,LO}$. In other words, a larger $C_{drv}$, which means a higher gain and power consumption for the PA driver stage, also means a higher power consumption for the circuits driving the LO ports of the reactive I/Q modulator. The power consumption of the PA driver-reactive mixer cascade is consequently related to $C_{drv}$.

Decreasing $C_{drv}$ results in a lower power consumption for the cascade, but also a lower gain for the PA driver. For a target overall gain of the I/Q modulator and PA driver cascade, the gain of the mixer must be consequently increased. This means, as just discussed, increasing $C_v$ and $C_C$, and, in turn, $C_{in,LO}$ and so $P_{d,LO}$. Hence, for a given gain of the cascade, there is an optimal $C_{drv}$ that minimizes the overall power consumption.

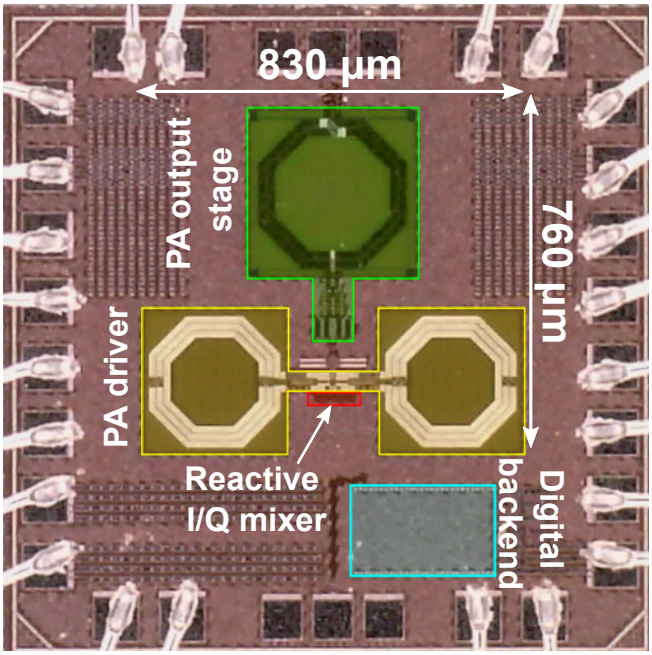


FIGURE 3.17: Microphotograph of the prototype realised in a 22 nm FD-SOI CMOS process. The active area is $830\times760\,\mu\text{m}^2$. The highlighted areas represent the main blocks of the TX.

In the presented design, the minimum power consumption of the I/Q modulator and PA driver cascade is achieved by setting the mixer in-band gain, $A_{v0,\text{var}}$, approximately 1 dB lower than its maximum possible value, which, as shown by (3.25), is the one for nil $C_{drv}$. If the mixer gain is increased beyond this optimal value, the increase in $P_{d,LO}$ will quickly exceed any reduction in the power dissipated by the PA driver. The optimal gain partition in this design is achieved by setting the varactor capacitance to $C_{v,max} = 100\,\text{fF}$ with a ratio of $C_{v,max}/C_{v,min} = 5.8$, while $C_c = 280\,\text{fF}$ and $C_{drv} = 13\,\text{fF}$.

## 3.3 Measurement Results

Prototypes of the proposed Cartesian TX for IoT applications, featuring the discussed reactive I/Q modulator, are implemented in a 22 nm FD-SOI CMOS technology. A microphotograph of the chip is shown in Fig. 3.17, where the main functional blocks of the system are highlighted. The active area is $830\times760\,\mu\text{m}^2$.

The experimental data is acquired using the test setup shown in Fig. 3.18. A signal generator provides the external 4.8 GHz LO signal. This signal is at twice the desired carrier frequency, as discussed in Section 3.2. For spectrum and power measurements, the TX output is connected to a spectrum analyzer. A digital 8 GHz 20 GS/s oscilloscope is used instead for the acquisition of time-domain waveforms

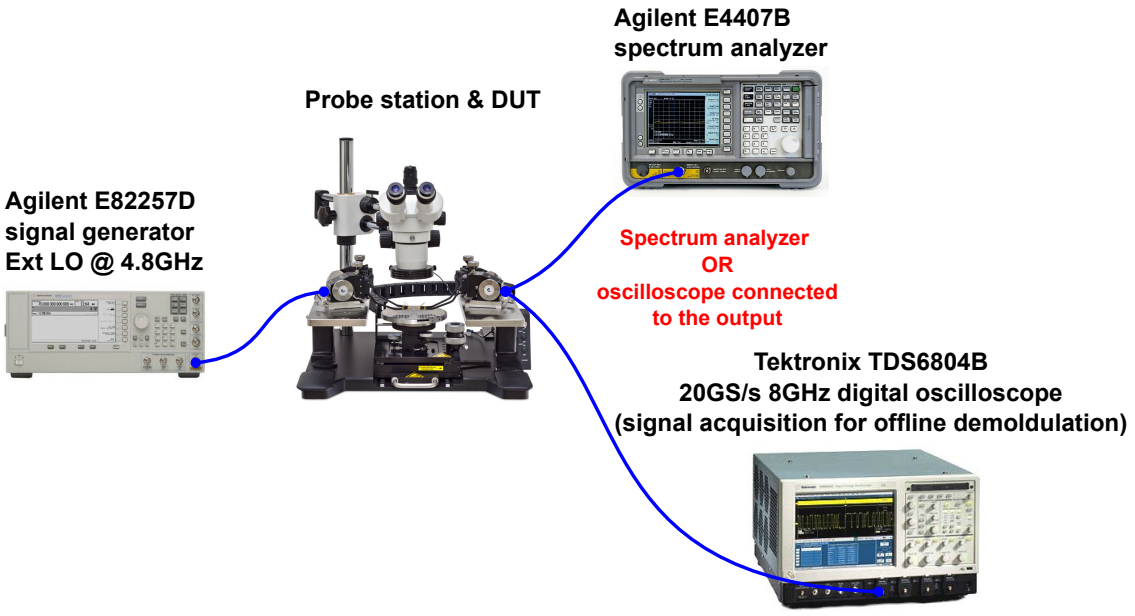


FIGURE 3.18: Schematic representation of the measurement test setup.

of the modulated RF signals. The obtained waveform samples are saved, and then demodulated and analyzed offline with the help of MATLAB.

The TX prototypes are first characterised in continuous wave (CW) operation. Figure 3.19 reports the measured and simulated output power and system efficiency. The prototypes show a saturated output power of $P_{sat} = 6.6$ dBm, and an output-referred 1 dB compression point $OP1dB = 5.5$ dBm. The measured CW system efficiency at the $OP1dB$ is 34.1%. There is an excellent agreement between the measured and simulated results.

The measured and simulated frequency response of the Cartesian TX is reported in Fig. 3.20. The output power is set to the $OP1dB$. The measured 3 dB bandwidth of the TX spans from 2.27 to 2.55 GHz, i.e., it is 280 MHz wide. Again, there is a very good agreement between the experimental results and the circuit simulations.

After the characterisation in CW operation, the TX performance with modulated signals is evaluated. The average output power and system efficiency are reported in Fig. 3.21 for both QPSK and 16-QAM modulated signals. The saturated output power for both modulation schemes is about 6.2 dBm, and, correspondingly, the peak system efficiency is about 35%.

A wideband spectrum measurement is reported in Fig. 3.22. The TX signal is 16-QAM-modulated at 2.4 Mbaud symbol rate with a 2.7 dBm average output power. All spurious spectral content is below -55 dBc. The most relevant suprious content is probably due to the limited attenuation of the digital interpolation filter, or to FM radio interference with the measurement setup. The effectiveness of the baseband filtering, intrinsically embedded in the operation of the proposed reactive passive

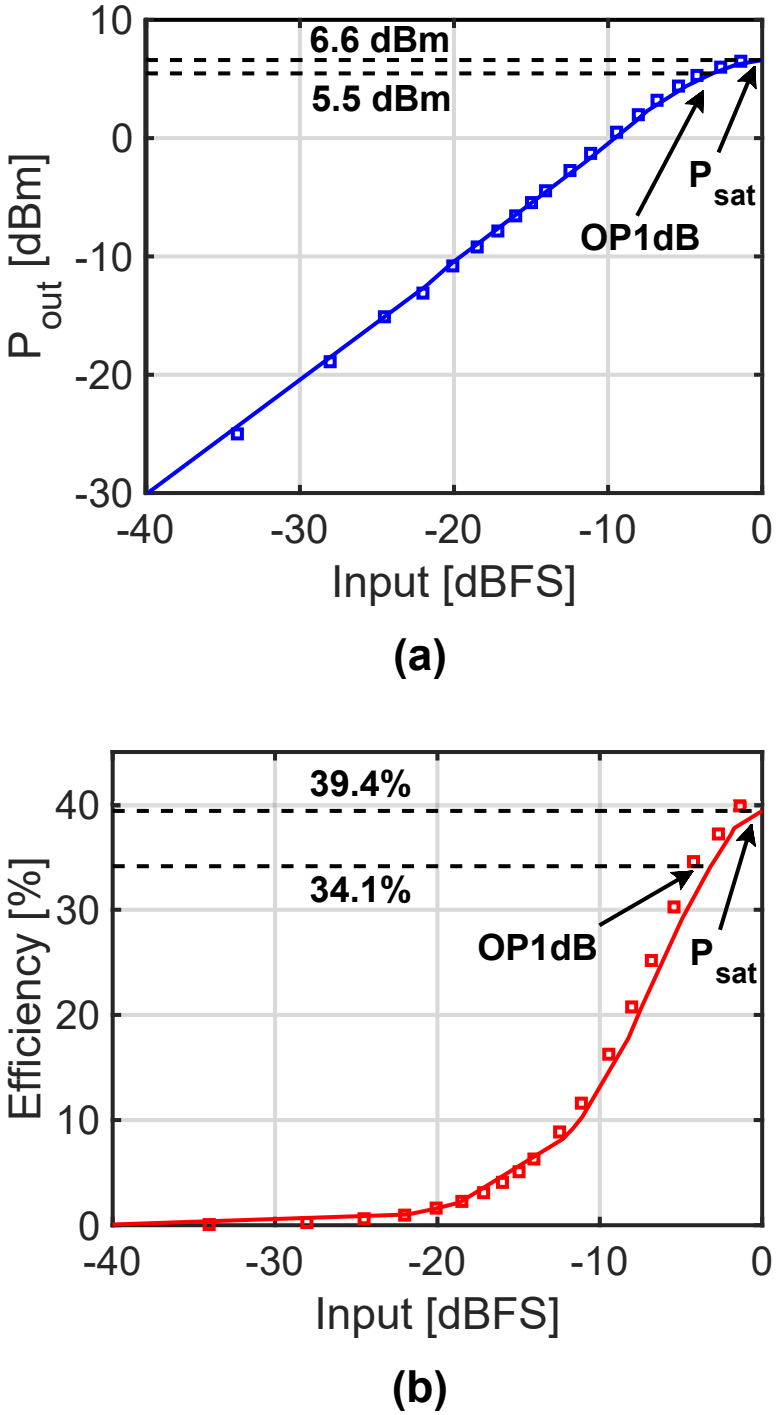


FIGURE 3.19: Measured (solid line) and simulated (square markers) TX performance in CW operation at 2.4 GHz: (a) output power; (b) system efficiency.

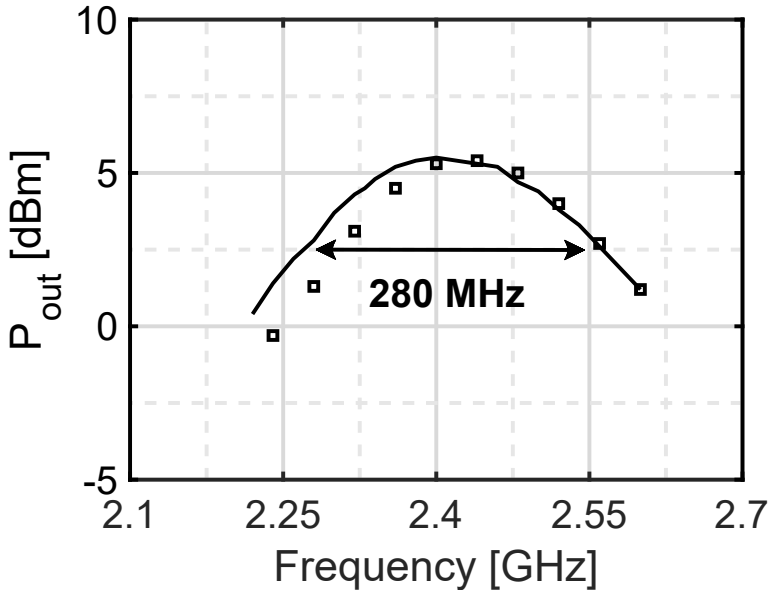


FIGURE 3.20: Measured (solid line) and simulated (square markers) frequency response of the TX. The output power is set to the $OP1dB$.

I/Q modulator, is underlined by the lack of strong TX replicas at $\pm 300$ MHz offsets.

To gauge the linearity of the proposed Cartesian TX, figures of merit borrowed from the Bluetooth 5.1 standard [40] are used in addition to EVM, namely, the adjacent channel leakage ratio (ACLR) and the alternate channel power ($P_{alt}$). Tests with QPSK and 16-QAM modulated signals are carried out both for 2.4 Mbaud and 1.2 Mbaud symbol rates. No predistortion is applied. The normalized constellation diagram and output spectrum of a QPSK-modulated signal at 2.4 Mbaud symbol rate with 5.1 dBm average output power are reported in Fig. 3.23. The measurement shows: EVM $= -27.9$ dB, ACLR $= -29$ dBc, and $P_{alt} = -35$ dBm. The corresponding system efficiency is 31.6% (Fig. 3.21). Changing the modulation format to 16-QAM, to increase the data rate to 9.6 Mb/s, yields: EVM $= -24.5$ dB, ACLR $= -32$ dBc, and $P_{alt} = -36$ dBm at 2.7 dBm average output power (Fig. 3.24), with 22% system efficiency (Fig. 3.21).

Similar results are obtained when the symbol rate is reduced to 1.2 Mbaud, as reported in Fig. 3.25, for a QPSK-modulated signal, and in Fig. 3.26, for a 16-QAM-modulated signal. In particular, the QPSK signal tests show EVM $= -28$ dB with ACLR $= -26$ dBc, and $P_{alt} = -34$ dBm at 5.1 dBm output power with corresponding 31.6% system efficiency. The 16-QAM tests report instead EVM $= -24.7$ dB with ACLR $= -31$ dBc, and $P_{alt} = -35$ dBm at a 2.7 dBm average output power and 22% system efficiency.

The TX power consumption while transmitting a 16-QAM 2.4 Mbaud signal at 2.7 dBm average ouput power is 8.5 mW. The corresponding breakdown of the power

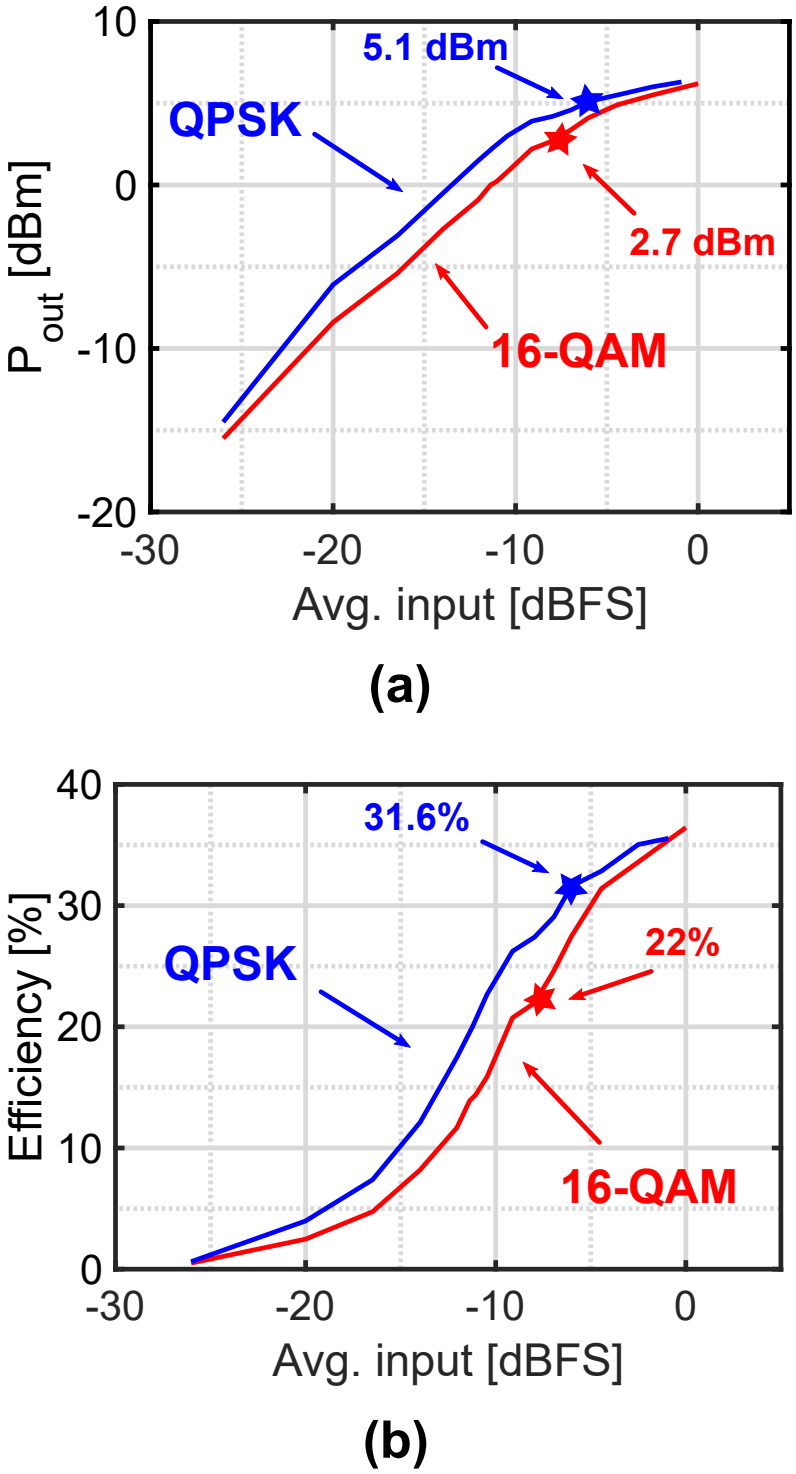


FIGURE 3.21: Measured TX performance at 2.4 Mbaud symbol rate: (a) average output power; (b) system efficiency.

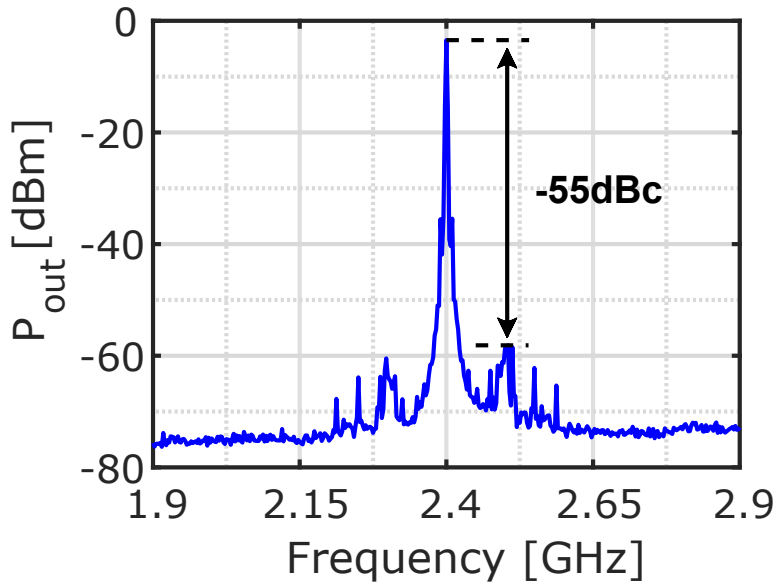


FIGURE 3.22: Wideband TX output spectrum with 16-QAM, 2.4 Mbaud modulation at 2.7 dBm average output power. Spurious signals at 87 to 106 MHz offsets are likely due to FM radio interference with the measurement setup.

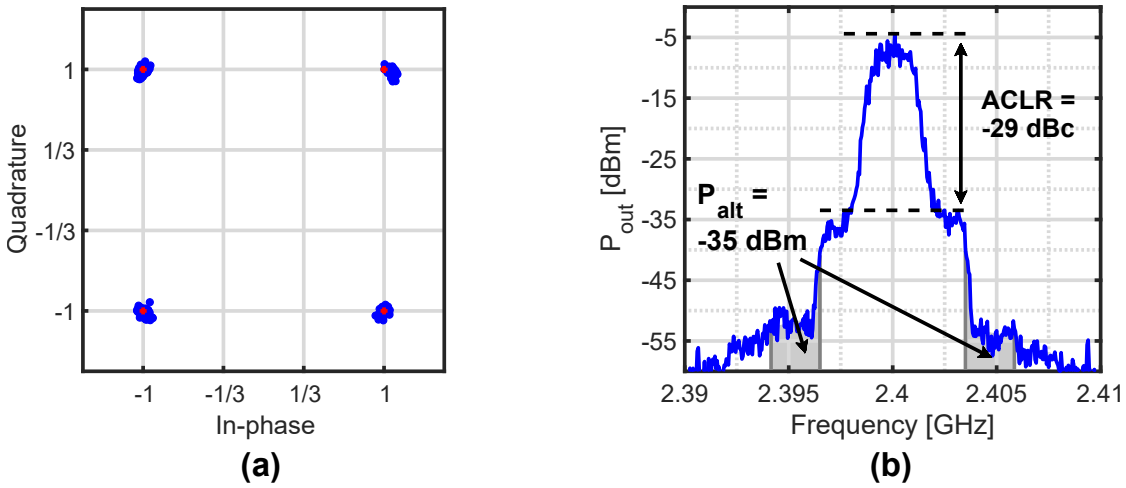


FIGURE 3.23: Measured QPSK modulated signal at 2.4 Mbaud symbol rate and 5.1 dBm output power: (a) normalized constellation diagram; (b) output spectrum.

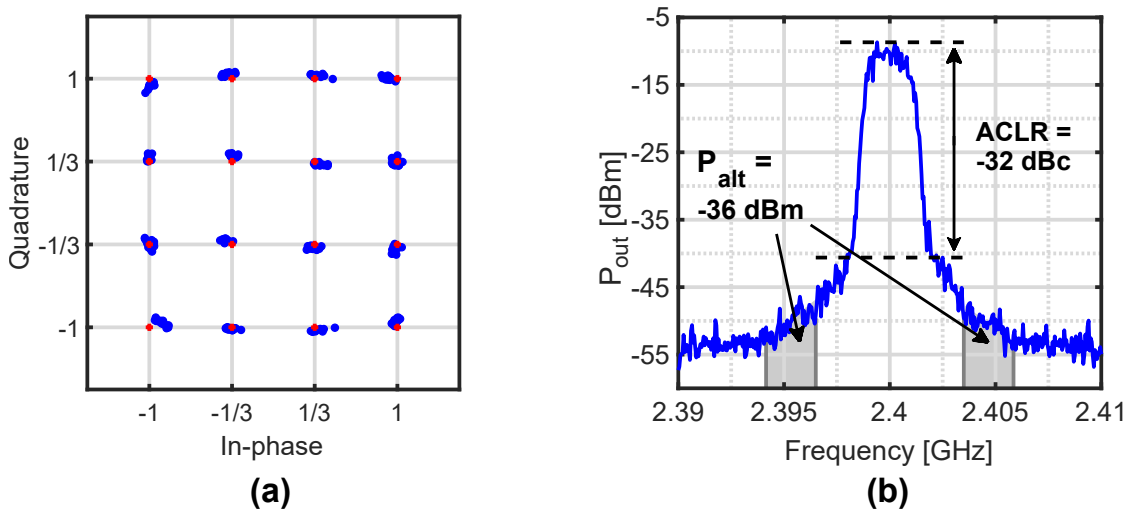


FIGURE 3.24: Measured 16-QAM modulated signal at 2.4 Mbaud symbol rate and 2.7 dBm output power: (a) normalized constellation diagram; (b) output spectrum.

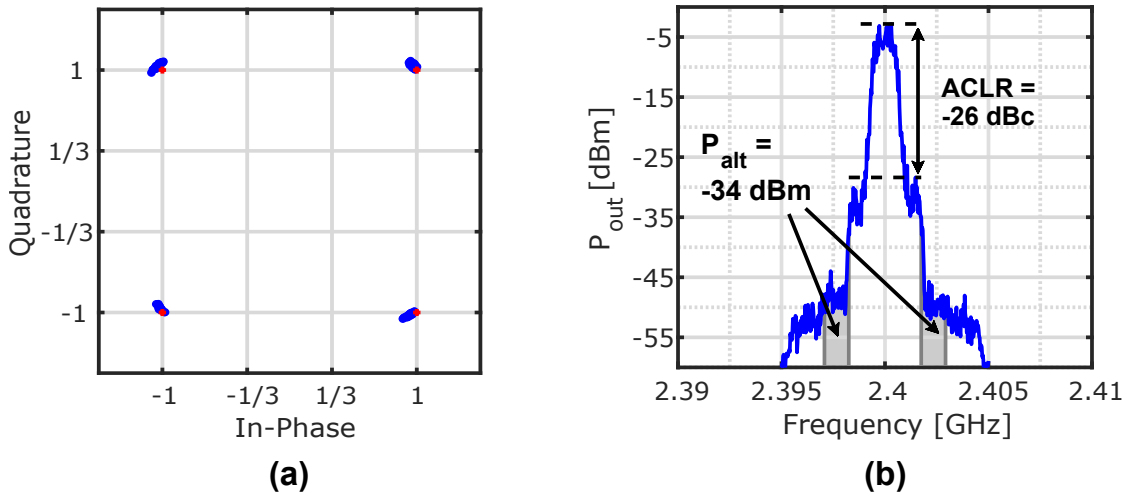


FIGURE 3.25: Measured QPSK modulated signal at 1.2 Mbaud symbol rate and 5.1 dBm output power: (a) normalized constellation diagrams; (b) output spectrum.

TABLE 3.1: Performance summary and comparison with the state-of-the-art.

| | **This work** | [58] | [51] | [52] | [42] | [43] | [44] | [36] | [37] | [41] |
|---|---|---|---|---|---|---|---|---|---|---|
| Technology | **22 nm FD-SOI** | 65 nm | 40 nm | 65 nm | 28 nm | 130 nm | 28 nm | 65 nm | 40 nm | 28 nm |
| Active area [$mm^2$] | **0.63** | 0.49 | 0.95* | 0.5 | 0.65 | 3* | 1.9* | 0.5** | 1.3* | 0.65 |
| Supply voltage [V] | **0.8** | 1.2/1.8 | 1.2 | 1.2 | 0.5/1 | 1.2/3.3 | 0.5/1 | 1/1.5 | 1 | 0.9 |
| Carrier frequency [GHz] | **2.4** | 2.4 | 2.4 | 1 | 2.4 | 2.4 | 2.5 | 2.4 | 2.4 | 2.4 |
| Symbol rate [Mbaud] | **2.4** | 1 | 1 | 16 | 1 | 1 | 1 | 1 | 1 | 1/20 |
| Modulation | **QPSK/ 16-QAM** | GFSK/ 8-DQPSK | GFSK/ 8-DQPSK | 16-QAM | GFSK | GFSK/ 8-DQPSK | GFSK | GFSK | GFSK | FSK/ 16-QAM |
| Architecture | **Cartesian** | Cartesian | Polar/ Cartesian | Cartesian | Polar | Polar | Polar | Polar | Polar | Polar |
| Data rate [Mb/s] | **4.8/9.6** | 1/3 | 1/3 | 64 | 1 | 1/3 | 1 | 1 | 1 | 1/43.3 |
| Average $P_{out}$ [dBm] | **5.1/2.7** | 6.4/4 | 0/0 | 2.5 | 0/3 | 2 | 0 | 2.7 | -2 | 0/0 |
| EVM [dB] | **-27.9/-24.5** | NA/-21.9 | NA/-25.2 | -31 | NA | NA/-24.4 | NA | NA | NA | -35.9/-22.4 |
| ACLR [dBc] | **-28/-32** | -29.3/-30.3 | NA# | -41 | NA# | NA# | NA# | NA# | NA# | NA# |
| $P_{alt}$ [dBm] | **-37/-36** | -34/-33 | NA# | NA | NA# | NA# | NA# | NA# | NA# | NA# |
| DC power [mW] | **10.2/8.5** | 77.2/64.6 | 10**/15** | 45 | 4.4**/6.3** | 89.2**/99.3** | 3.7** | 5.2** | 4.4** | 15.3/27.3** |
| System efficiency [%] | **31.6/22** | 5.7/3.9 | 10**/6.7** | 4 | 23**/32** | 1.8**/1.6** | 27** | 34.7** | 14** | 6.5/3.7** |

* includes both TX and RX ** includes LO generation # ACLR and $P_{alt}$ not reported but TX compliant with Bluetooth spectral mask

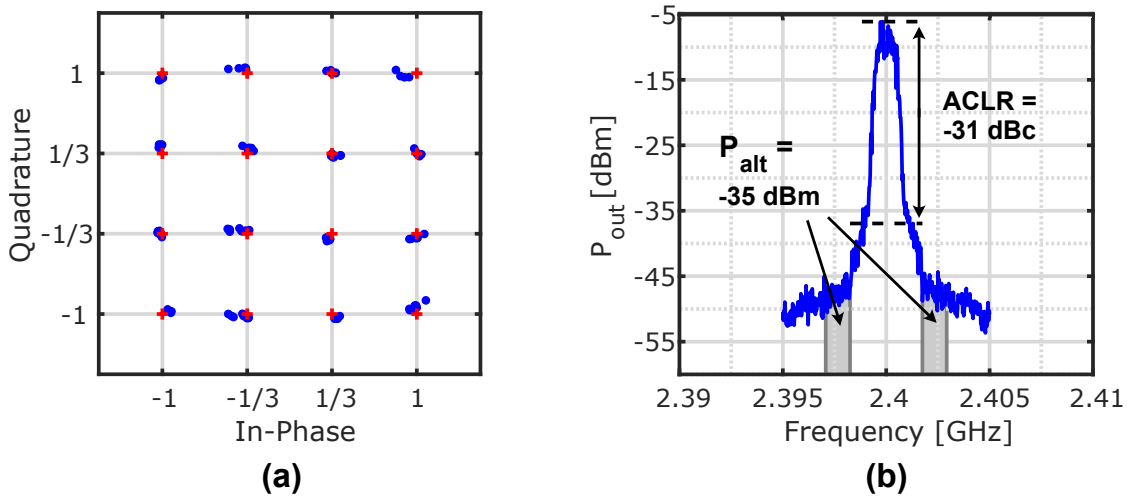


FIGURE 3.26: Measured 16-QAM modulated signal at 1.2 Mbaud symbol rate and 2.7 dBm output power: (a) normalized constellation diagrams; (b) output spectrum.

dissipation is depicted in Fig. 3.27. The vast majority of the power (>90%) is dissipated by the PA, as it should be in an efficient transmitter.

The performance of the measured prototypes is summarized and compared to the state-of-the-art in Table 3.1. A comparison between the proposed Cartesian TX and the state-of-the-art is also graphically carried out in Fig. 3.28, where various low-power transmitters are categorised in terms of achieved data rates and system efficiencies. Compared to the state-of-the-art, the system efficiency of the proposed TX, based on an unconventional reactive I/Q modulator, is superior to other Cartesian modulators, and almost in line with polar transmitters.

## 3.4 Final Remarks on the Reactive Passive Mixer

A reactive I/Q modulator is proposed to simplify the circuitry of a Cartesian TX. The reactive I/Q modulator can be driven by high impedance source and can be loaded by a capacitive impedance, which simplifies the interface with the baseband DACs and RF amplifier, hence increasing the system efficiency. The reported rigorous analysis of the proposed reactive I/Q modulator results in useful design equations that are exploited to optimize the TX design. A system with high linearity, able to transmit signals with high-order modulations, emerges. Achieving high system efficiency is intrinsically difficult in a low power, high data rate system because of the relatively low power delivered to the antenna: the use of the reactive I/Q modulator helps solving this issue.

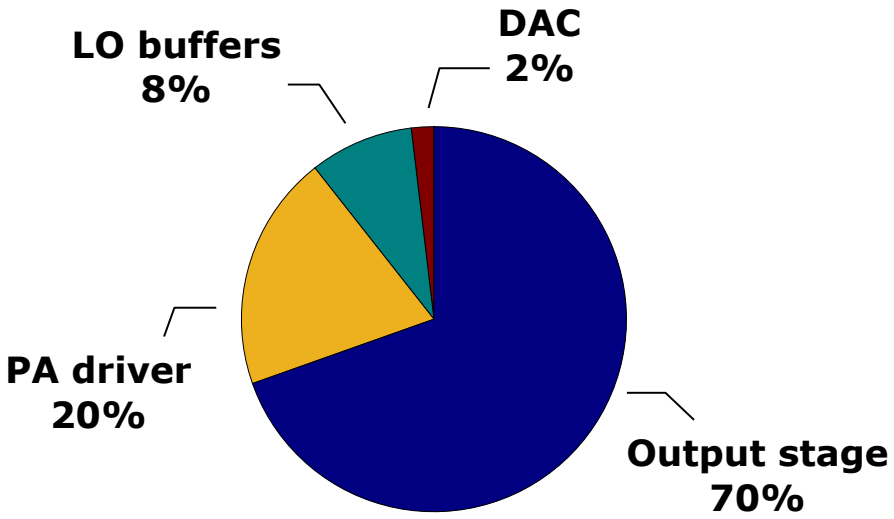


FIGURE 3.27: Breakdown of the system power consumption while transmitting a 16-QAM-modulated 2.4 Mbaud signal with 2.7 dBm average output power.

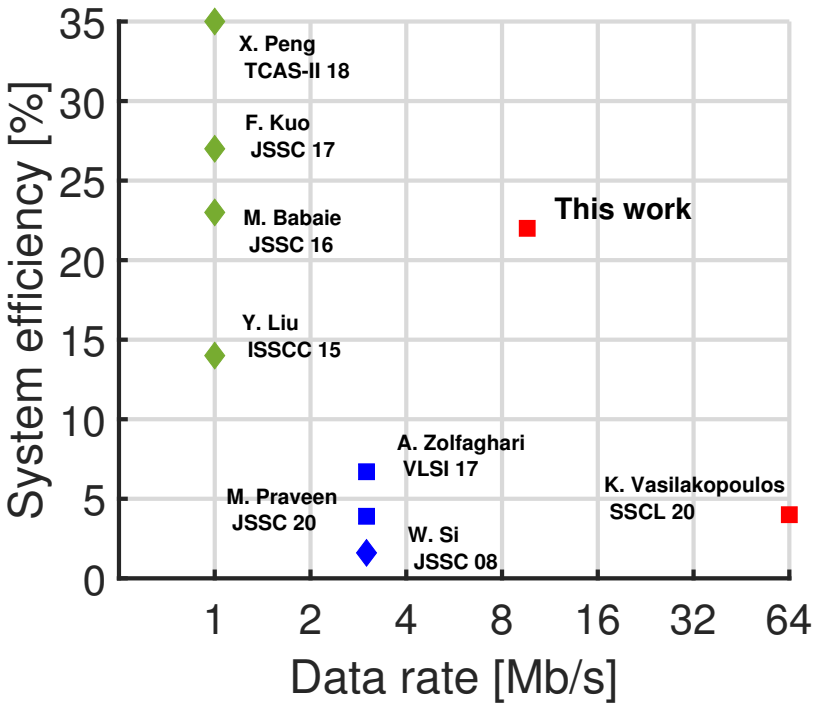


FIGURE 3.28: Comparison with the state-of-the-art. Modulation scheme: 16-QAM (red), GFSK (green), 8-DPSK (blue). Architecture: polar (◇), Cartesian (□).

Prototypes of a proof-of-concept Cartesian TX show 22% average system efficiency while transmitting 16-QAM-modulated signals at a 9.6 Mb/s data rate with an average output power of 2.7 dBm and an EVM of -24.5 dB.

# Chapter 4

# Integrated mm-wave Harmonic Oscillators

## 4.1 What Is an Oscillator?

An oscillator is one of the fundamental building block of many RF circuits; its job is to convert the constant supply voltage in a stable, periodic signal at a determined frequency. Since it generates its own output, it falls in the category of so called "autonomous circuit", circuits that do not require any time-varying input to produce a time-varying output. It finds ample use in both communication and RADAR applications. One may think that creating an oscillator is quite easy (how many times a block that is supposed to *amplify* ends up *oscillating* instead!), but the implementation is far from trivial and full of pitfalls; the ideally perfectly stable tone is, in reality, marred by instabilities such as frequency drift and phase noise. While the former is solved by using a phase-locked-loop (PLL) and a sufficiently stable reference (e.g. low-frequency quartz oscillators), the latter only comes down to the quality of the oscillator design. Additionally, the inherent time-variant operation of the oscillator also complicates the formal analysis of its behaviour, requiring a deep understanding of the underlying mechanisms if the designer wants to achieve the maximum performance possible. Moreover, the (im)purity of the produced signal is often the bottleneck in modern communication systems, as the phase noise is directly transferred to the modulated data (Fig. 4.1), deteriorating its signal-to-noise ratio (SNR) and widening the output spectrum [59]. In digital circuits, a stable clock signal is of fundamental importance to the correct operation of the logic blocks. A measure of the clock stability is the *jitter*, measured in units of time. The phase noise of the oscillator generating the clock has a direct impact on its jitter and, thus, the operation of the digital circuitry. All of these factors contribute to make the oscillator one of the most studied analog RF blocks, still attracting a lot of attention from the analog designer community.

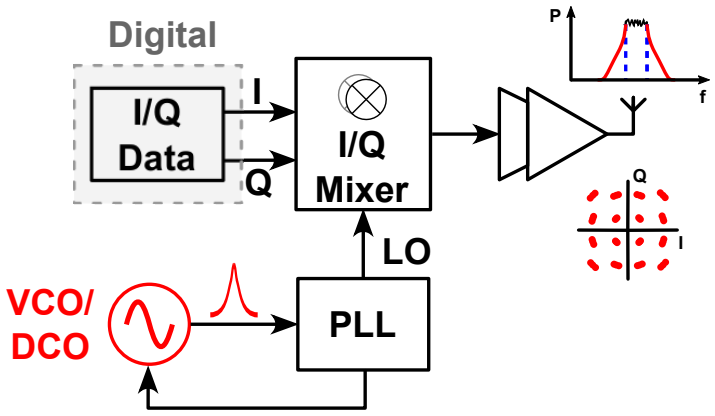


FIGURE 4.1: Example of a transmitter chain with a noisy oscillator. The output signal spectrum is larger than expected and invades nearby channels. The encoded I/Q signal has a lower SNR.

During these years, three different RF oscillators were designed, each one of them employing a different topology to break free from the limitations of modern CMOS ultra-scaled technologies.

## 4.2 Basics of CMOS Harmonic Oscillators

The most common CMOS oscillator topology is the parallel oscillator. It is composed by a parallel LC network (also called *tank*) and a negative admittance, needed to compensate the losses of the real tank. The LC tank is driven by a current source. The negative admittance can be realised with the help of active devices and a feedback network. The most used topology for CMOS implementations is the cross-coupled differential-pair class-B oscillator [59], shown in Fig. 4.2. The tank is composed by the inductance $L_p$ and capacitance $C_p$; at its resonant frequency is $\omega_0 = 1/\sqrt{L_p C_p}$ the real tank losses can be represented by the equivalent resistor $R_p$. It is important to note that this element is parasitic, i.e., that it stems from the losses of the real reactive elements ($L_p$ and $C_p$). As the tank quality factor $Q_p$ increases, $R_p$ increases as well. The MOSFETs $M_1$ and $M_2$ realise the cross-coupled differential-pair. This configuration shows a negative differential admittance of $-g_m/2$, where $g_m$ is the transconductance of a single MOS. If $R_p < 2/g_m$ (the losses are compensated by the active devices) then the system is unstable: the thermal noise naturally present in the circuit is enough to kick-start the oscillation. In an ideal system, the oscillation amplitude would grow indefinitely, however, in reality, higher order mechanisms limit the amplitude (distortion, limited supply etc.). In this case, the oscillators operates in class-B: each transistor spends half of the time injecting current into the tank. If the oscillation signal is large, the transistors operate in hard switching and

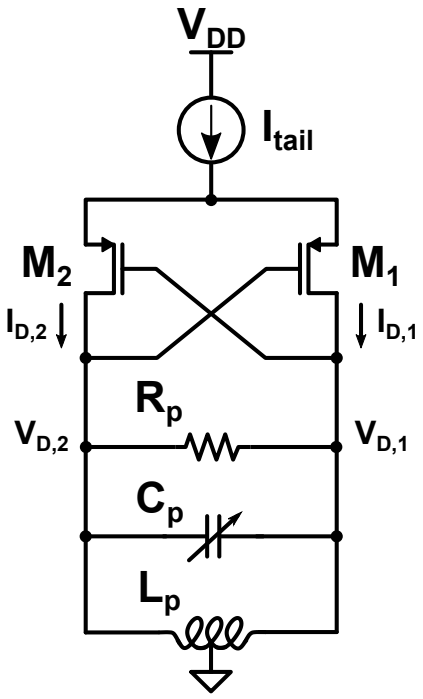


FIGURE 4.2: Simplified schematic of a class-B CMOS parallel oscillator. $R_p$ is the equivalent parallel resistance of the tank at the resonance.

the drain current of each MOSFET is a square wave with frequency $\omega_0$ and swing $0 - I_{tail}$ (Fig. 4.3). While the current is rich in harmonic content, the voltage across the tank is (almost) sinusoidal, as the parallel $LC$ circuit show a high resistance only around the resonant frequency $\omega_0$, thus converting into voltage only the first current harmonic. For a pMOS oscillator as the one in Fig. 4.2, the inductor center tap is placed at 0 so the single ended voltage swing has 0 mean and can move between $\pm V_{DD}$. The differential oscillation amplitude across the tank is given by

$$V_0 = 2I_{D,1}^0 \frac{R_p}{2} = \frac{2}{\pi} I_{tail} R_p < 2V_{DD} \tag{4.1}$$

where $I_{D,1}^0$ is the amplitude of the first harmonic of the drain current. The same results applies for a nMOS pair, except that that now the oscillation swings around $V_{DD}$. In reality, due to the presence of the tail generator, the maximum voltage swing is reduced.

While the class-B is the most popular, the cross-coupled differential-differential pair oscillator can also operate in class-C [60], class-D [61] and class-F [62] to reduce the phase noise. For example, in the class-C oscillator, the MOS transistors inject current into the tank in short, high pulses, resulting in a higher first voltage/current harmonic with the same current consumption.

However, all of the previous topologies employ a parallel LC tank as resonator. An emerging class of harmonic oscillators is the series resonance LC oscillator. For

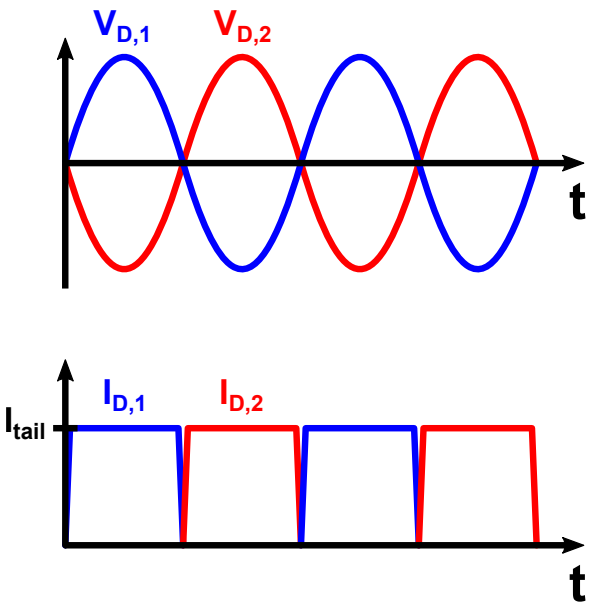


FIGURE 4.3: Voltage and current at the cross-couple drains in steady state (hard-switching).

reasons that will be explored in Chapter 6, it is able to achieve much better phase noise performance than its LC parallel counterparts [63]. The implementation of an integrated series VCO has proved challenging, but some prototypes show promising results [64, 65].

## 4.3 Phase Noise

If we look closely at the output spectrum of a real oscillator, we would see something like Fig. 4.4: the ideal single tone is replaced by a signal with left and right sidebands, an effect due to the perturbation of the ideal tone by the noise of the system. Signals in an electronic circuit can be perturbed by noise sources in both amplitude and phase. In an oscillator, however, phase noise is dominant. In fact, the mechanisms that limit the amplitude of the oscillation also greatly reduce the effect of any amplitude perturbation. In addition, these same mechanisms tend to restore the amplitude of the signal after a perturbation. Instead, there is no such recovery or mitigation effect for the phase perturbation: the (small) phase errors accumulate over time. For this reason, phase noise dominates (at least near the carrier). More precisely, the output signal of a real oscillator is

$$v_o(t) = A_0 cos\left[2\pi f_0 t + \phi_n(t)\right] \tag{4.2}$$

where $A_0$ is the amplitude, $f_0$ the frequency, and $\phi_n(t)$ is the phase perturbation or phase noise.

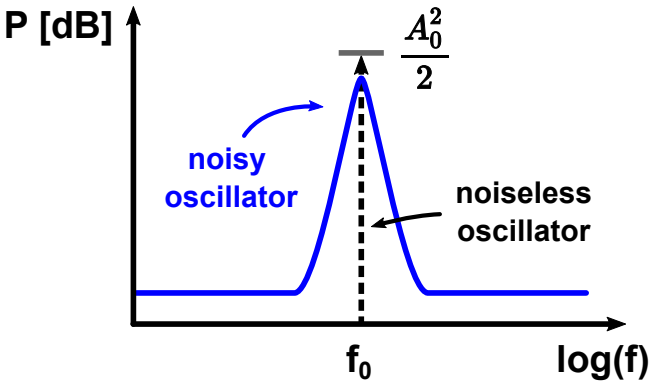


FIGURE 4.4: The output spectrum of a real oscillator (blue) and its ideal counterpart (black).

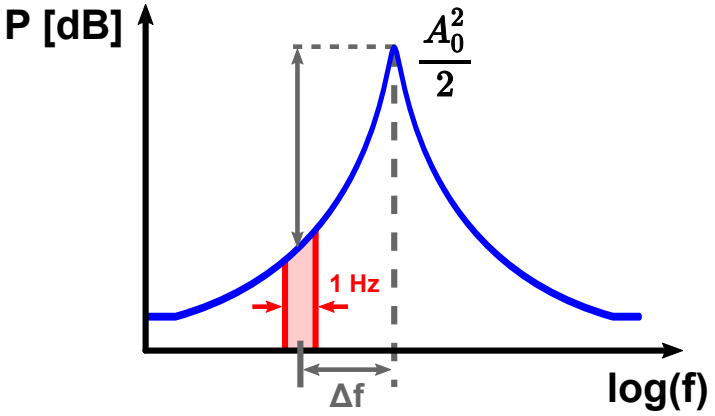


FIGURE 4.5: The phase noise is defined as the ratio of the integrated noise power and the carrier power.

The phase noise itself is measured as a ratio of the noise power integrated in 1 Hz intervals at a frequency offset from the carrier $\Delta f$, and the carrier amplitude $A_0^2/2$ (Fig. 4.5). It is measured in dBc/Hz.

A typical sideband is sketched in Fig. 4.6, where it is possible to discern three separate segments. Since the phase errors accumulate over time, the conversion from injected amplitude noise to phase noise can be thought as an "integrator". In this way the phase noise arising from upconverted white noise has a slope proportional to $1/f^2$. The region closest to the carrier is often dominated by flicker noise or $1/f$ noise from the active devices, which becomes the segment with slope $1/f^3$ in Fig. 4.6.

The first attempt at quantifying the phase noise of a given oscillator were based on a linear time-invariant (LTI) model of the oscillator. This approach gave birth to the famous Leeson equation

$$\mathcal{L}(\Delta f) = 10\log\left[\frac{kTF}{A_0^2}\frac{R_P}{Q_P^2}\left(\frac{f_0}{\Delta f}\right)^2\right] \tag{4.3}$$

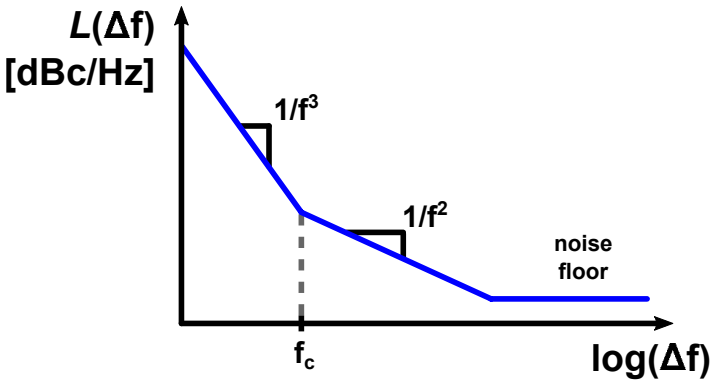


FIGURE 4.6: Phase noise sideband of a real oscillator.

where $Q_P$ is the tank quality factor, and $F$ is the excess noise factor to empirically include the noise introduced by the actives. As simple as it is, the LTI approach (and consequently the Leeson equation) is not able to explain the $1/f^3$ region and cannot be easily generalised to the treatment of active devices with strongly time-dependent operation.

A new, more accurate model for phase noise has been proposed in [66]. Consider the simplest LC oscillator in Fig. 4.7: the effect of a current pulse on the large signal depends on the time of injection $\tau$. If the pulse is injected at the peak of $v_o(t)$, the amplitude is affected but not the phase (Fig. 4.8(a)). On the other hand, if the injection occurs during the zero crossing, the phase of the oscillation is disturbed (Fig. 4.8(b)). This simple and intuitive example shows that the operation of even the simplest oscillator we can think of cannot be described by an LTI model. The transfer function that relates the phase noise to the noise injected into the LC tank is time-variant in nature and is often referred to as the Impulse Sensitivity Function (ISF). The ISF is periodic with the same frequency as of the oscillator carrier and can be thought of as a description of how sensitive the oscillator is to a disturbance at any given time. The ISF can be determined analytically only for the simplest oscillators, in most cases simulation is the only feasible option [66]. The time variant nature also easily explains how the low frequency flicker noise is upconverted and integrated to become phase noise. In the frequency domain, the ISF components convolve with the noise sidebands of the current injected into the tank, translating them in frequency and around the carrier.

The time-variant approach allows us to analytically determine the noise contribution of the cross-couple differential-pair in a class-B oscillator that results to be $1+\gamma$, where $\gamma$ is the channel noise factor of the MOS transistors realising the differential pair [59].

Among the other things, the LTV model can predict the upconversion of $1/f$ noise into phase noise, but the analysis can be extremely complicated. In fact, if

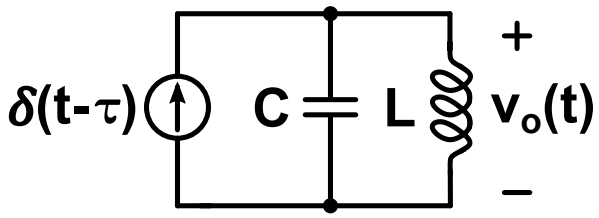


FIGURE 4.7: Simple LC oscillator excited by a current pulse.

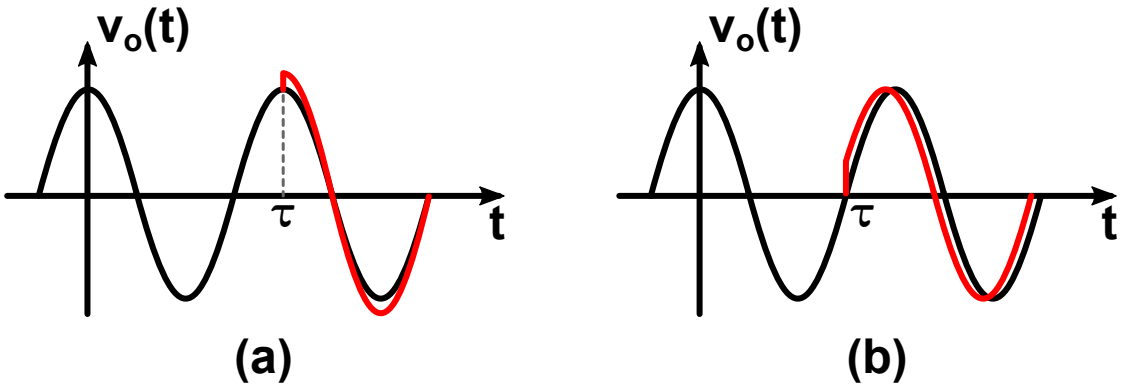


FIGURE 4.8: Impulse response of the simple LC oscillator for two injection times: (a) at the peak the phase is unchanged; (b) at the crossing the phase is affected.

we assume only first-order effects, the upconversion vanishes and there is no $1/f^3$ region. A full analysis would require considering higher-order effects such as short-channel effects, parastic capacitances and so on, making it infeasible. Some empirical solutions have been found: in class-B oscillators, for example, it has been shown that having a common mode resonance at $2f_0$ mitigates the effects of $1/f$ upconversion. This (relatively) simple solution is quite sensitive to PVT variations [59]. Class-C oscillators, in theory, offer another option to reduce the $1/f$ noise upconversion [67, 68].

The bias circuitry itself is one of the main contributors of phase noise, both directly (by injecting noise) and indirectly (by introducing parasitics and altering the waveforms of the circuit). Using a current mirror is a popular solution as it offers a high output resistance. The drawback is the added $1/f$ noise coming from the mirror itself and the reference branch, the latter even amplified by the mirror ratio. Designing longer (and wider) MOSFETs for the mirror lowers the injected $1/f$ noise but introduces a large amount of parasitic capacitance $C_{tail}$ that deteriorates the phase noise if the differential-pair transistors are allowed to enter the linear region. A solution is to place a shunt inductance $L_{tail}$ as seen in Fig. 4.9, that resonates with $C_{tail}$ at $2f_0$ and increases the common mode impedance. Another option is to add small degeneration resistances to the sources of the mirror MOSFETs, thus boosting the current mirror output impedance.

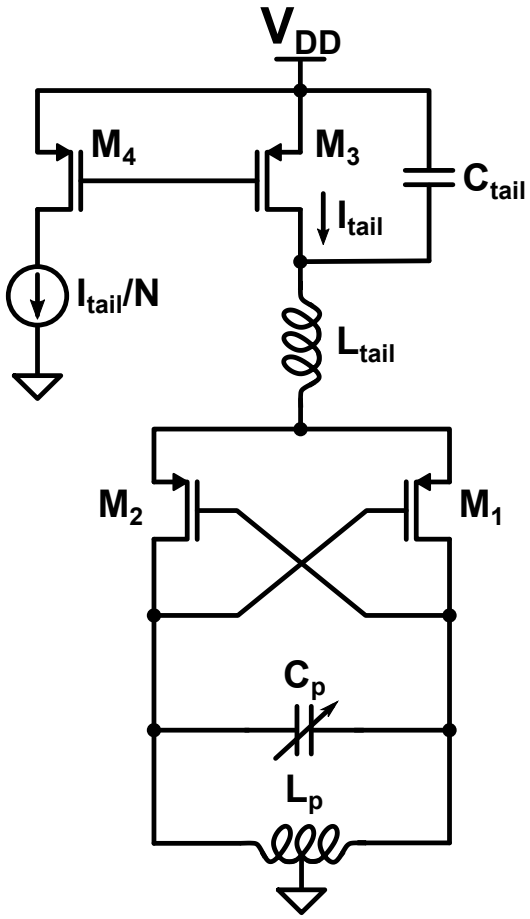


FIGURE 4.9: Class-B oscillator with resonant tail filter.

## 4.4 Limitations of the class-B Oscillator

The ubiquitous class-B oscillator may be the workhorse of many RF designs, but the designer trying to achieve very low phase noise will soon discover its fundamental limitations. Leeson's equation (4.3) contains many terms, but most are correlated and cannot be changed in without affecting others. In essence, to reduce phase noise, the designer must maximise the output swing ($A_0$), maximise the passive quality factor ($Q_P$) and reduce the tank impedance $\sqrt{L_P/C_P}$. The swing cannot grow indefinitely as it is limited by the reliability rules of ultra-scaled technologies; $Q_P$ is also given by the technology itself and rarely exceeds 10 or 20. So in the end, lower phase noise means designing an oscillator with a lower tank inductance. This can be done up to a point, after which the parasitic inductance of the interconnects would become dominant and quickly degrade the quality factor of $L_P$.

If even lower phase noise is required, then the single core class-B oscillator may not be sufficient and other solutions should be explored. Three different approaches are presented in the following Chapters: Chapter 5 presents a multi-core oscillator where the synchronisation of N cores reduces the phase noise by a factor of N; Chapter 6 presents a series resonant LC VCO; finally, Chapter 7 demonstrates the use of a stacked stage to increase the supply, without sacrificing reliability.

# Chapter 5

# A Reconfigurable 12 GHz Multi-Core DCO

## 5.1 Multi-Core Harmonic Oscillators

Usually, the local oscillator (LO) is designed to meet the most stringent phase noise requirement set by the communication standard. The 5G protocol, however, is not just about high data rates: its wide range of applications means that the highest modulation order is not always needed, including the ability to fall back to simpler modulation schemes with less stringent phase noise demands. Therefore, it makes sense to conceive an oscillator capable of dynamically scaling phase noise, trading performance for power consumption.

To achieve low phase noise levels, a large amplitude of oscillation and a small tank equivalent resistance at resonance ($R_T$) are required, while a high quality factor (Q) of the resonating $LC$ tank is needed to keep the power consumption at bay [69]. Ultra-scaled CMOS technologies are no friends to low phase noise, as they feature limited supply voltages and reduced voltage ratings. Moreover, there is a practical limit to the minimum tank inductance, and hence $R_T$, that can be realized without dramatically impairing the resonator Q [70].

To further improve phase noise, though, $N$ identical oscillators can be coupled and operated in a synchronous fashion [36, 70–78], which reduces the phase noise by a factor $N$. With this approach, a higher power consumption is traded for a lower phase noise, ideally keeping a constant figure-of-merit (FoM). Clearly, implementing an oscillator array comes with the drawback of a larger silicon area.

The implementation of large arrays of coupled oscillators and the achievement of the related phase noise benefit is not trivial. Ideally, the operation of the coupled oscillator array should not be affected by the coupling network, nor the latter should introduce any phase noise impairment. However, if the oscillator coupling impedance is high, the desired phase noise improvement may be experienced only at small frequency offsets from the carrier [71]; additionally, mismatches between

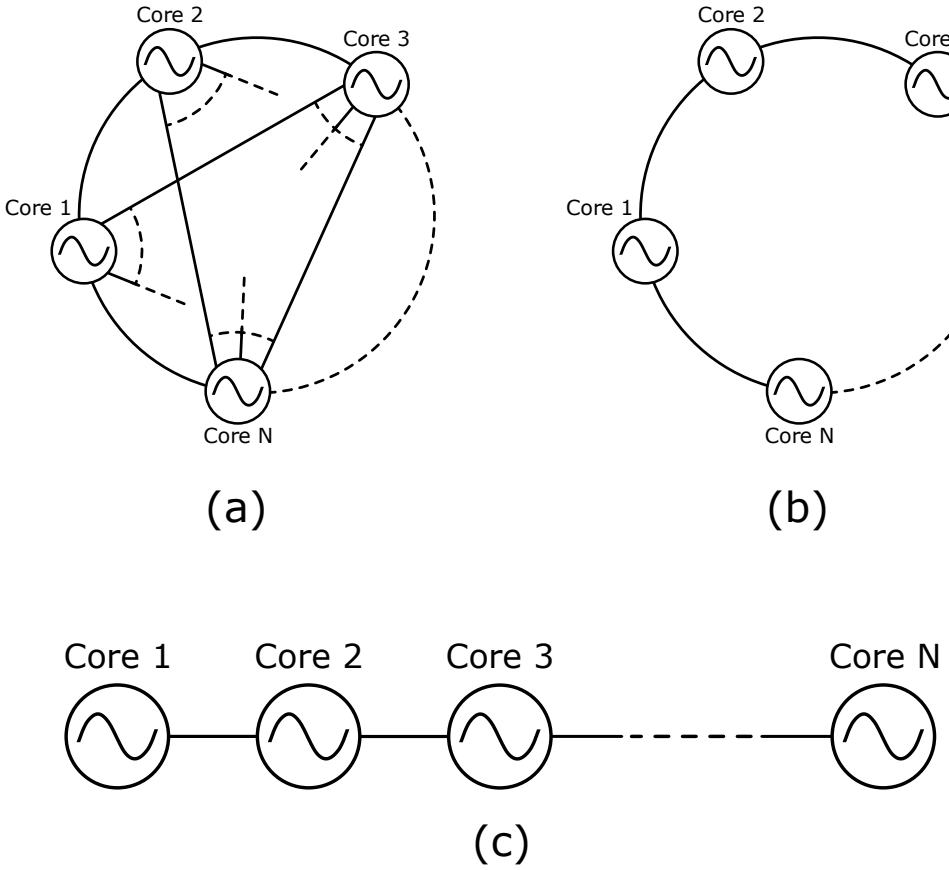


FIGURE 5.1: Architectures for $N$ coupled oscillators: (a) star connection; (b) ring connection; (c) nearest-neighbor bilateral coupling.

the resonance frequencies of the individual oscillators in the array may induce a phase noise degradation that increases with the impedance of the coupling network [73,79]. Thus, as $N$ increases, the coupling network becomes correspondingly more difficult to design, as the star connection of Fig. 5.1(a) [72], where each oscillator is globally coupled to all the others, becomes impractical. A simplification of the star topology is the ring of Fig. 5.1(b) [73]; even in this case, though, closing the ring may be cumbersome, if a large number of oscillators is involved. Moreover, the layout of the ring may be complicated by the requirement of aligning all transistors in the same direction, which is common in advanced CMOS technologies. Eventually, one may have to resort to the nearest-neighbor bilateral coupling of Fig. 5.1(c). The latter sets some challenges, as it is more susceptible to mismatch-induced phase noise degradation [73, 79, 80]. Moreover, the coupling network of a large array of oscillators tends to introduce more parasitics due to its larger footprint, potentially creating unwanted systematic mismatches between the oscillators and shifts in the oscillation frequency.

As previously discussed, the lowest achievable phase noise may not always be needed. Hence, a reconfigurable coupled oscillator array can be devised [73]. The

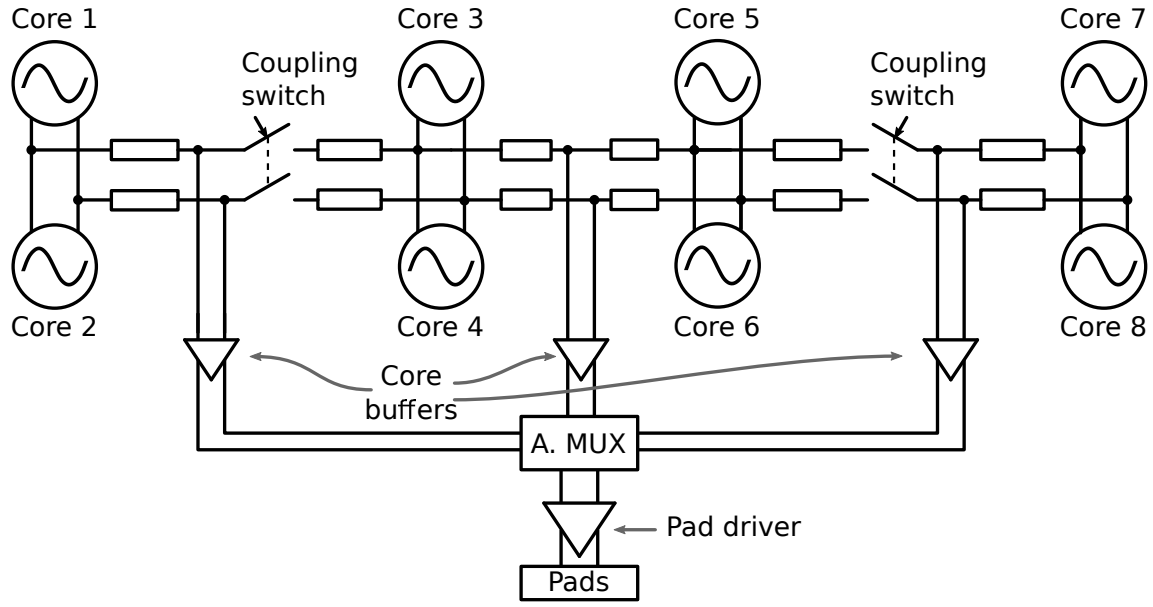


FIGURE 5.2: Block diagram of the proposed octacore DCO.

goal is to be able to switch off some oscillators to save power when the resulting phase noise deterioration is acceptable. Such reconfigurability requires the possibility to individually turn on/off and disconnect the oscillators from the array (Fig. 5.2); the latter operation is non-trivial, as it requires additional switches in the coupling networks, which may increase the coupling impedance and consequently deteriorate phase noise.

This Chapter discusses an octacore oscillator array in which the number of active oscillators can be changed in a scalable fashion to trade higher phase noise for lower power consumption. The design is implemented in a 28 nm CMOS technology and is based on 8 digitally-controlled oscillator (DCO) cores. A block diagram of the circuit is sketched in Fig. 5.2: the 8 oscillator cores are arranged in 4 pairs of tightly coupled oscillators, which are further interconnected in a nearest-neighbor bilateral coupling scheme. While this circuit was first introduced in [81], we present here an in-depth discussion, with particular care to the design and implementation of the coupling arrangement.

The architecture chosen for the coupling network is illustrated in Section 5.2. In Section 5.3, a time variant analysis of the switches required to reconfigure the circuit is presented, obtaining useful guidelines for the switch design and, hence, for the minimization the phase noise penalty due to the reconfigurable coupling network. The design of the oscillator core is presented in Section 5.4, while the experimental characterization of the circuit prototypes is reported in Section 5.5. Measurements show a DCO that is capable of reaching an outstandingly low phase noise of -126 dBc/Hz at 1 MHz offset from the 10.7 GHz carrier. Conclusions are

drawn in Section 5.6.

## 5.2 Reconfigurable Coupling Network

One of the main targets of the presented design is to implement scalability in the multicore topology, i.e., to be able to reduce power consumption whenever the lowest possible phase noise is not required [73]. Ideally, this would mean to be able to turn on any number of oscillator cores and operate them synchronously; hence, the coupling network should provide a relatively low-impedance connection between the cores that are on while avoiding any loading on the active oscillators by the cores that are off. In practice, this is difficult to guarantee, and a compromise between reconfigurability and performance has to be found.

It is known [73,79,80] that, in the presence of a mismatch $\Delta f_0$ between the individual oscillation frequencies of two standalone oscillators, the phase noise performance of the two oscillators coupled together deteriorates as the impedance of the coupling network $R_C$ increases. The phase noise penalty $\Delta\mathcal{L}$ in a dualcore oscillator system is captured by [73,79]

$$\Delta\mathcal{L} \approx 30\log_{10}\left[1+\frac{R_C}{R_T}Q^2\left(\frac{\Delta f_0}{f_0}\right)^2\right] \tag{5.1}$$

where $Q$ is assumed identical in both standalone oscillators, and $f_0$ is the nominal oscillation frequency. This is a particular problem in nearest-neighbor coupling because of the intrinsic asymmetry of the network, as illustrated in Fig. 5.3, where the parasitics introduced by the coupling network are depicted as lumped elements $C_P$ and $R_C$. The oscillators at the edge of the array are connected to a single neighbor, while the other oscillators are connected to two neighbors. Ideally, if the oscillators are strongly coupled, and thus synchronized, they all operate in phase, such that the current through the coupling impedance $R_C$ is nil [71,80]. It is however clear from Fig. 5.3 that the edge oscillators are only loaded by half of the parasitic capacitance than the other cores, introducing a systematic frequency mismatch. Reconfigurability exacerbates this issue, as the switches implementing it contribute significant resistive and capacitive parasitics, increasing $R_C$ and $C_P$ (and $\Delta f_0$ in (5.1)), potentially leading to severe phase noise degradation.

Another impairment due to non-negligible coupling impedance is that the phase noise improvement due to synchronization is only enjoyed at frequency offsets from the carrier lower than [71]

$$\Delta f_c = \frac{R_T f_0}{2R_C Q} \tag{5.2}$$

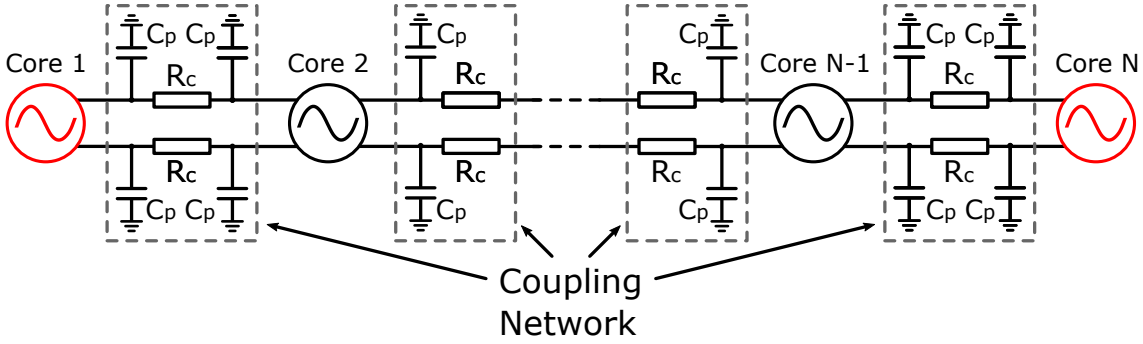


FIGURE 5.3: Parasitics introduced by the coupling network in a nearest-neighbor bilateral coupling architecture.

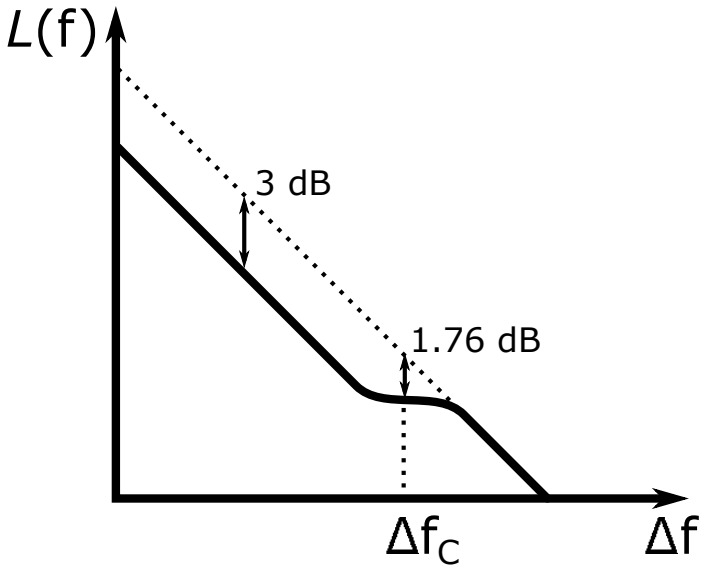


FIGURE 5.4: Impact of the coupling impedance $R_C$ on the phase noise sideband of a dualcore system.

As sketched in Fig. 5.4 for a dualcore system, at small offsets the phase noise improves by 3 dB with respect to the phase noise of the stand-alone oscillator, while at offsets larger than $\Delta f_c$ such an improvement vanishes, each oscillator effectively working as a standalone oscillator at such offsets. It is therefore of paramount importance to keep $R_C$ as small as possible.

To minimize the phase noise penalty by keeping $R_C$ and $C_P$ small while allowing system scalability, the reconfigurable octacore oscillator is organized as follows: the oscillators are grouped into tightly coupled pairs, connected by relatively short (compared to the oscillation wavelength) low-ohmic transmission lines, and all pairs are arranged in the array shown in Fig. 5.2. Short transmission lines and switches connect the pairs at the edges of the array to the ones at the center, while the two pairs in the center are connected to each other by short transmission lines with no switches. In this way, each oscillator pair is equally loaded by one set of switches,

which greatly reduces the systematic frequency mismatches, as the switches are the main contributors to $C_P$. At the same time, we can operate the array in 2-core, 4-core, 6-core, and 8-core configurations without any appreciable loss of flexibility.

Since $C_P$ is largely determined by the switches (which, as we will discuss later, must have a very high aspect ratio), the proposed arrangement results in a highly symmetrical array, each oscillator core being loaded by a single $C_P$. Furthermore, it minimizes the overall number of switches and the associated coupling resistances with it, with benefits in terms of possible degradation of the phase noise performance. This is especially true as the switch at the center of the array has been removed, since the latter makes the circuit particularly sensitive to random mismatches, as discussed in [73].

The two edge core pairs and the center core quad are buffered individually, as shown in Fig. 5.2. An analog multiplexer selects among the buffer outputs and feeds a pad driver for measurement purposes. Hence, with reference to Fig. 5.2, cores 1 and 2 are used in the 2-core configuration, cores 3–6 in the 4-core configuration, and cores 1–6 in the 6-core configuration. Obviously, all cores are used in the 8-core configuration.

## 5.3 Analysis and Implementation of the Coupling Switch

As discussed in Section 5.2, the introduction of switches in the coupling network should lead to the minimum possible increase of network parasitics. The details of the implementation of the coupling switches are shown in Fig. 5.5. The switches are realized with pMOS devices in series with the differential transmission lines interconnecting the tanks of adjacent oscillator pairs, as mentioned. The use of pMOS devices is required because it would not be possible to turn off nMOS switches, for the following reason: since the inductor of the LC tank has its center tap connected to ground (Fig. 5.5), it is clear that drain/source of the MOS switch are biased to 0 V, too, while experiencing the full ac swing of the (single-ended) oscillation, whose peak amplitude is much larger than the threshold voltage of the nMOS device. This means that an nMOS switch would be forced to turn on when the negative half-wave of the oscillation exceeds the value of the threshold voltage, even if its gate voltage was set to 0 V. Switched-off cores would then significantly load the active cores, leading to a severe degradation of the phase noise performance.

Using pMOS switches solves the issue, where low-threshold-voltage devices are employed to maximize the on-conductance. When the gate voltage of the pMOS switch is set to 0 V and the switch is nominally on, the device is dynamically turned on during the positive half-wave of the (single-ended) oscillation, as illustrated in

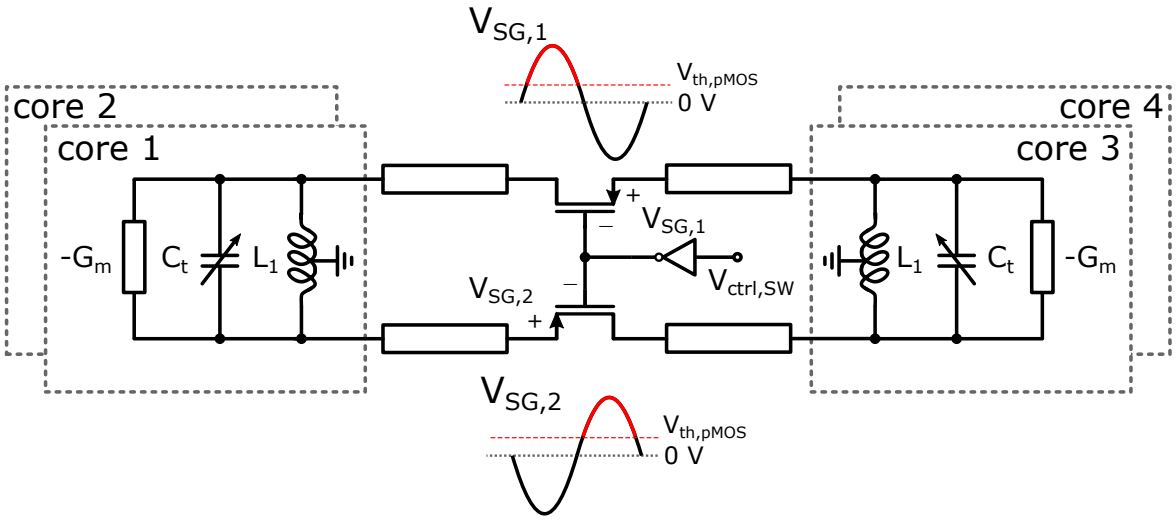


FIGURE 5.5: Simplified schematic of the switches in the reconfigurable coupling network, limited to the coupling between two core pairs. The switches are on during the red portion of the waveforms.

Fig. 5.5. This resembles the behavior of the active transistor in a class-C amplifier or oscillator. As it will be clear momentarily, a lower-than-expected switch conductance is the result of this class-C behavior. More importantly, though, a pMOS switch guarantees that the respective oscillator core is effectively isolated from the rest of the array when the switch is turned off, i.e., when its gate voltage is set to a sufficiently high dc voltage. Another reason to favor pMOS over nMOS switches is that the source/drain diodes of an nMOS device would partially turn on during the negative half-wave of the oscillation. Again, this problem disappears using pMOS devices.

Finally, it is clear that pMOS and nMOS devices swap roles in the above analysis if the center tap of the tank inductor is connected to the power supply rather than ground.

### 5.3.1 Time-Variant Analysis of the Coupling Switch

Since the coupling switch is on only over a relatively small fraction of the oscillation period, as illustrated in Fig. 5.5, a conventional small-signal analysis to estimate the coupling resistance $R_C$ would not produce a correct result. As a matter of fact, assuming $R_C$ is the reciprocal of the small-signal channel conductance of the switch leads to large errors, as we will see presently, which calls for the adoption of a time-variant analysis. More specifically, this effect is not solely related to a lower average switch conductance (the obvious consequence of the switch being on less than 100% of the time), and is not captured by a standard time-invariant analysis. Fortunately,

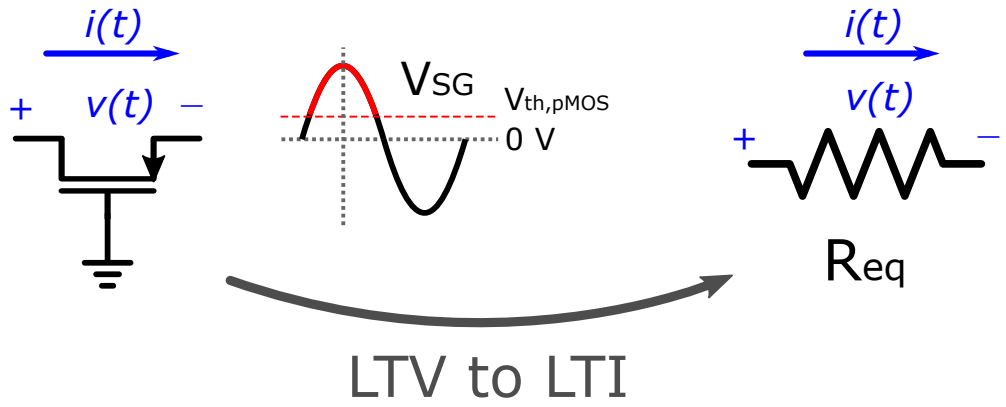


FIGURE 5.6: Time-invariant model of the coupling switch.

it is still possible to derive a time-invariant equivalent resistance $R_{eq}$ to model the coupling switch in the on-state, as sketched in Fig. 5.6.

Our time-variant analysis starts with the observation that the gate of the pMOS switch is grounded when the switch is on, while the large-signal oscillations at drain and source are identical, as the oscillators in the coupled array are all working in phase. If the tank Q is at least moderately high, the single-ended oscillations at the tank outputs are sinusoidal; hence, without further loss of generality, we can write the switch source-to-gate voltage as

$$V_{SG}(t) = V_{pk}\cos(\omega_0 t) \tag{5.3}$$

where $V_{pk}$ is the single-ended oscillation amplitude, and $\omega_0 = 2\pi f_0$.

To assess the impact of the switch on phase noise, we assume that the oscillation at the drain is affected by phase noise while the oscillation at the source is not, and derive the expression of the current induced across the switch by the phase noise itself (the procedure can be seen as the extension of Thevenin's theorem beyond the case of a linear time-invariant circuit).

Accordingly, the voltage $v(t)$ between drain and source in Fig. 5.6 is

$$v(t) = V_{pk}\cos(\omega_0 t + \phi(t)) - V_{pk}\cos(\omega_0 t) \approx -\phi(t)V_{pk}\sin(\omega_0 t) \tag{5.4}$$

where $\phi(t)$ is the (very small) phase disturbance. We assume next that $\phi(t)$ is a single complex tone at frequency $\Delta\omega \ll \omega_0$, i.e.,

$$\phi(t) = A_\phi e^{j\Delta\omega t} \tag{5.5}$$

From (5.4) and (5.5) we obtain

$$v(t) = V_{USB}e^{j(\omega_0+\Delta\omega)t} + V_{LSB}e^{j(-\omega_0+\Delta\omega)t} \tag{5.6}$$

where the complex amplitude of the upper and lower sidebands of the voltage across the switch, $V_{USB}$ and $V_{LSB}$, are given by

$$V_{USB} = -\frac{A_\phi V_{pk}}{2j} \tag{5.7}$$

and

$$V_{LSB} = \frac{A_\phi V_{pk}}{2j} \tag{5.8}$$

Obviously,

$$V_{USB} = -V_{LSB} \tag{5.9}$$

From (5.6), it is now immediate to obtain the spectrum of $v(t)$, illustrated in Fig. 5.7.

The current $i(t)$ flowing through the switch is linked to $v(t)$ by the transistor time-varying channel conductance $g(t)$, as

$$i(t) = g(t) \cdot v(t) \tag{5.10}$$

Since the operation of the transistor is periodic, the time-varying switch conductance can be expressed with its bilateral Fourier series with coefficients $g_k$, i.e.,

$$g(t) = \sum_{k=-\infty}^{\infty} g_k e^{jk\omega_0 t} \tag{5.11}$$

Because of (5.6), (5.10) and (5.11), $i(t)$ is made of tones at frequencies $k\omega_0 + \Delta\omega$, $k$ being an integer number:

$$i(t) = I_{USB} e^{j(\omega_0+\Delta\omega)t} + I_{LSB} e^{j(-\omega_0+\Delta\omega)t} + \tilde{i}(t) \tag{5.12}$$

where $\tilde{i}(t)$ contains the components of $i(t)$ around harmonics other than the fundamental. Using (5.6)–(5.12), and with the aid of Fig. 5.7, we obtain

$$I_{USB} = g_0 V_{USB} + g_2 V_{LSB} \tag{5.13}$$

and

$$I_{LSB} = g_0 V_{LSB} + g_{-2} V_{USB} \tag{5.14}$$

We now observe that, since $V_{SG}(t)$ in (5.3) is an even function, so is $g(t)$, which means that the its Fourier components are all real-valued, yielding $g_{-2} = g_{2*} = g_2$. Finally, from (5.13), (5.14) and (5.9) we obtain

$$\frac{V_{USB}}{I_{USB}} = \frac{V_{LSB}}{I_{LSB}} = \frac{1}{g_0 - g_2} \equiv R_{\text{eq}} \tag{5.15}$$

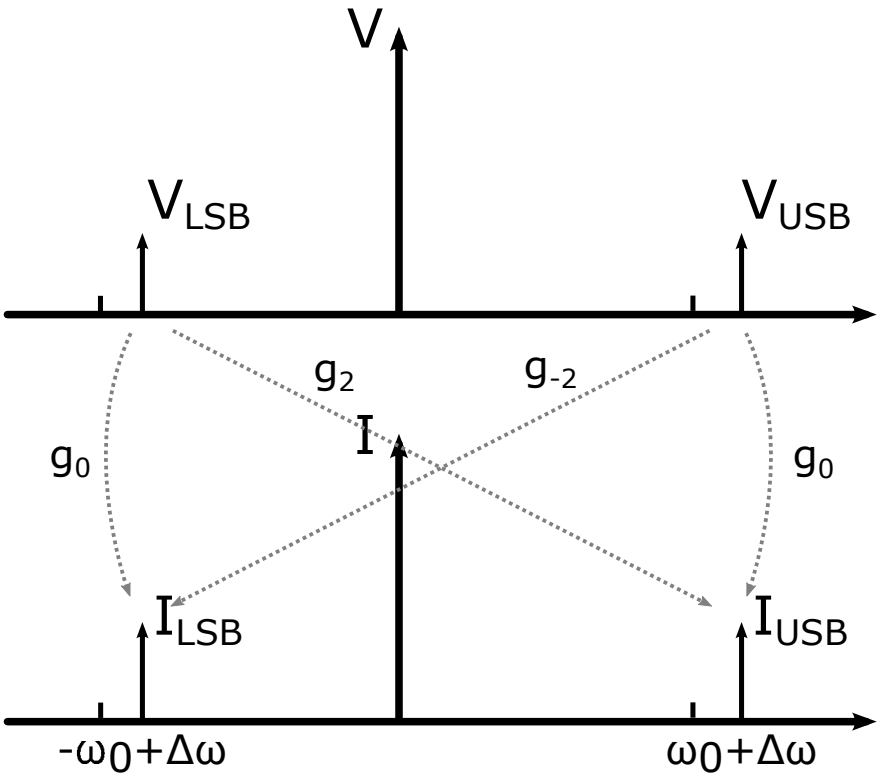


FIGURE 5.7: Spectra of $v(t)$ and $i(t)$ close to $\omega_0$.

Equation (5.15) shows that the upper (lower) sideband of the voltage across the switch can be related to the upper (lower) sideband of the current through the switch by a time-invariant equivalent resistance $R_{\text{eq}}$, which captures the time-variant nature of the switch operation in a simple and elegant manner. Since the switch operates in a rather deep class-C regime, $g_2$ is positive and not much smaller than $g_0$, which means that $R_{\text{eq}}$ is significantly higher than $1/g_0$.

As anticipated at the beginning of this Section, this result makes it clear that using the small-signal channel conductance or the average channel conductance instead of $R_{\text{eq}}$ is bound to lead to a substantial underestimation of the coupling resistance.

### 5.3.2 Simulation Results

Several transistor-level simulations have been carried out to verify the theoretical predictions of Section 5.3.1. In order to estimate the relevant Fourier coefficients of the time-varying conductance of the pMOS switch channel − namely, $g_0$ and $g_2$ − we make use of the simulation test bench of Fig. 5.8. Compared to the circuit of Fig. 5.5, we changed the reference node for simplicity, driving the gate terminal of the switch with the waveform $-V_{SG}(t)$, and biasing source and drain to ground. To avoid any undesired interaction with the parasitic capacitances of the switch, an

$LC$ resonator is connected between source and drain and tuned to the same angular oscillation frequency $\omega_0$ of the coupled oscillator. The precise values of $L$ and $C$ are not particularly important, as long as the resonance frequency, which includes the effect of all parasitic MOS capacitances, is $\omega_0$ (in principle, we could operate the test bench at $\omega_1 \neq \omega_0$, as long as $L$ and $C$ resonate at $\omega_1$; in practice, though, it is more convenient to choose $\omega_1 = \omega_0$, as the real waveform of $V_{SG}(t)$ is then generated directly by the oscillator [not shown in Fig. 5.8]).

We proceed by connecting a small-signal current source between source and drain, with unit amplitude and frequency equal to $\omega_0 + \Delta\omega$. If $L$ and $C$ are lossless, their parallel impedance at $\omega_0 + \Delta\omega$ has an absolute value of approximately $1/(2\Delta\omega C)$, and if this is much larger than the time-variant resistance of the switch channel, the voltage sidebands created by the current source at $\omega_0 + \Delta\omega$ ($V_{USB}$) and at $-\omega_0 + \Delta\omega$ ($V_{LSB}$) are functions solely of such a resistance and will therefore be constant with a varying $\Delta\omega$, until $\Delta\omega$ is so large that $1/(2\Delta\omega C)$ starts dominating. The qualitative plot of $V_{USB}$ and $V_{LSB}$ is shown in Fig. 5.9, and is straightforwardly obtained by running a periodic state-state (PSS) analysis followed by a periodic ac analysis with e.g. the *spectre* simulator.

Assuming, without loss of generality, a positive value of $\Delta\omega$, the small-signal current source at $\omega_0 + \Delta\omega$ is described with $I_{USB} = 1$ in (5.13) and $I_{LSB} = 0$ in (5.14), immediately obtaining the desired valued of $g_0$ and $g_2$ as

$$g_0 = \frac{1}{V_{USB}\left(1 - \left|\frac{V_{LSB}}{V_{USB}}\right|^2\right)} \tag{5.16}$$

and

$$g_2 = -g_0\left(\frac{V_{LSB}}{V_{USB}}\right)^* \tag{5.17}$$

where $V_{USB}$ and $V_{LSB}$ are from the flat portions of the sidebands.

It is worth remarking that the PSS waveform of $V_{SG}(t)$ will have a non-zero initial phase $\psi$ in general, that is,

$$V_{SG}(t) = V_{pk}\cos(\omega_0 t + \psi) \tag{5.18}$$

such that $g_2 = |g_2|e^{j2\psi}$. Thus, only the absolute magnitude of $g_2$ estimated with (5.17) should be used in (5.15) to compute $R_{\text{eq}}$.

Finally, since we have forced $I_{USB} = 1$ and $I_{LSB} = 0$, we point out that (5.7)–(5.9) do not apply in this context.

Once obtained the Fourier coefficients, the equivalent resistance $R_{\text{eq}}$ was then computed with (5.15).

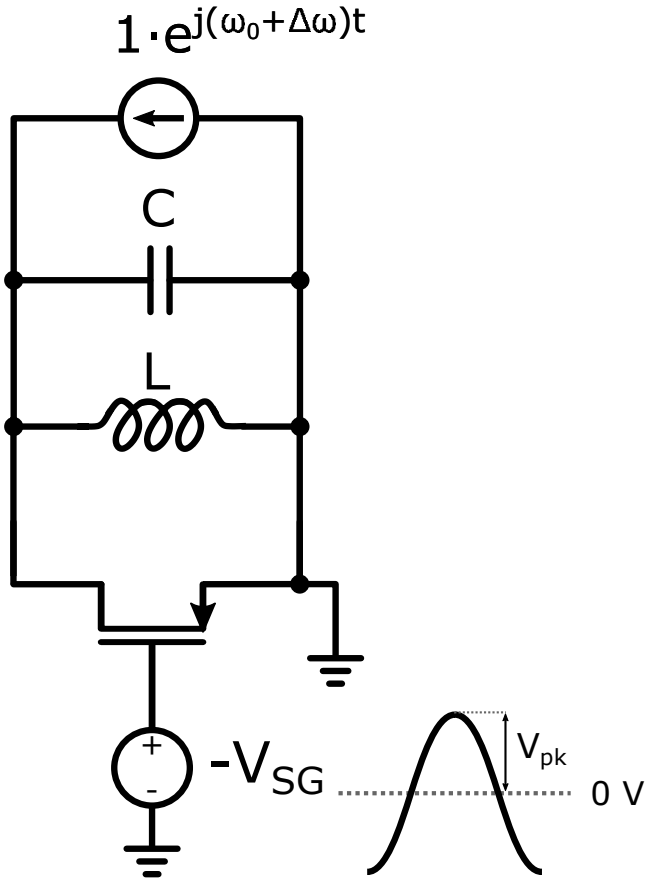


FIGURE 5.8: Test bench for the estimation of the Fourier coefficients of the time-varying switch conductance.

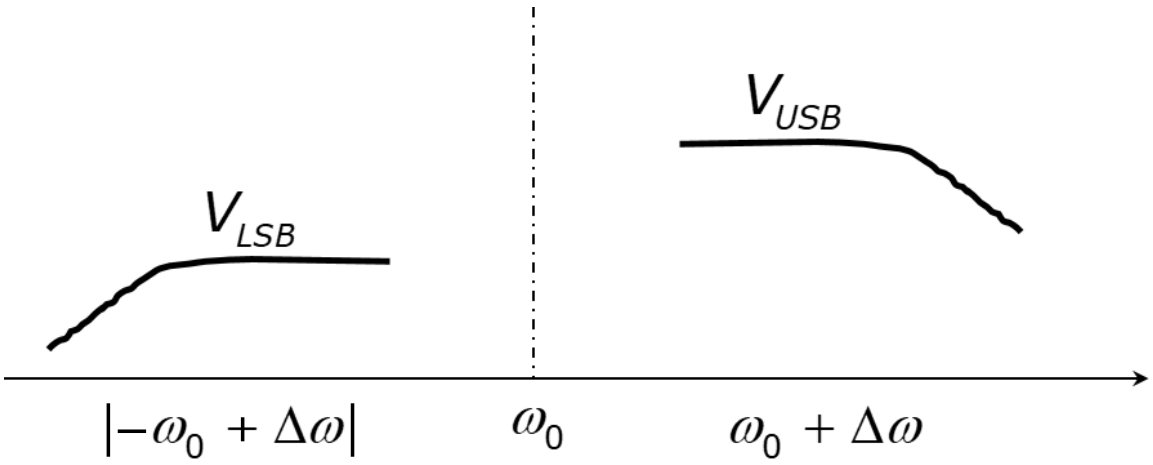


FIGURE 5.9: Lower and upper voltage sidebands obtained from the simulation in Fig. 5.8.

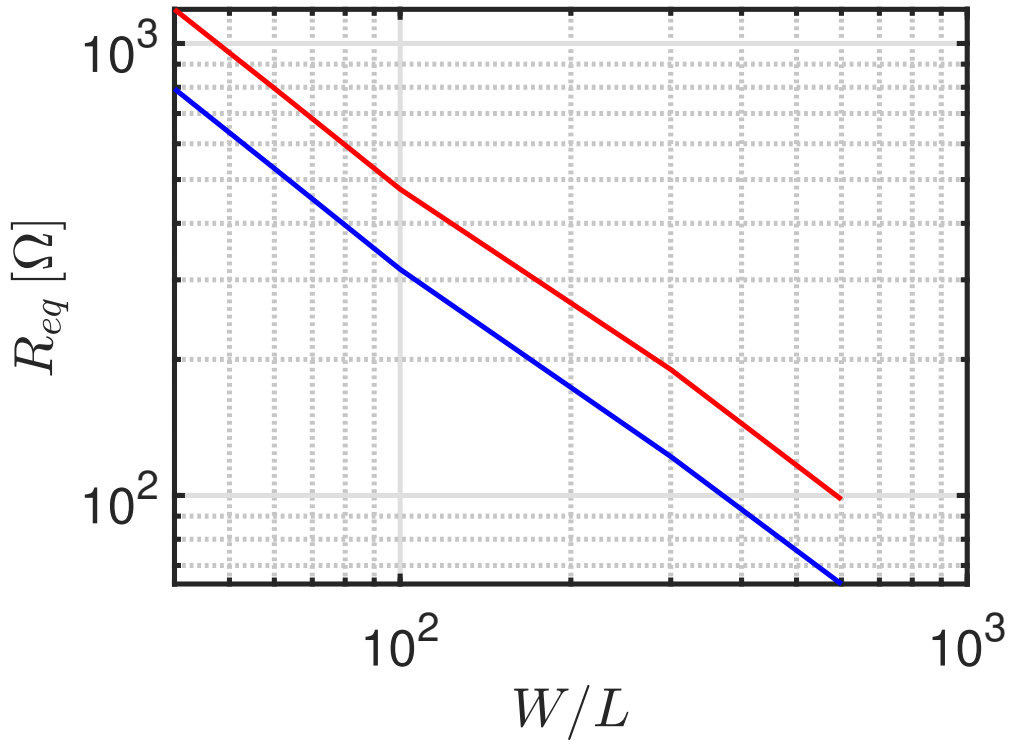


FIGURE 5.10: Equivalent switch resistance $R_{\text{eq}}$ vs switch aspect ratio (red curve). $R_{\text{eq}}$ is estimated at $V_{pk} = 1.1$ V using (5.15). The blue curve shows $1/g_0$ for comparison.

Figure 5.10 shows $R_{\text{eq}}$ vs switch aspect ratio for $V_{pk} = 1.1$ V and compares it to the case when the switch resistance is assumed to coincide with the inverse of the average channel conductance $g_0$. Fig. 5.10 shows that the difference between the two is indeed remarkable.

Since both $g_0$ and $g_2$ are highly sensitive to the amplitude of the signal driving the switch, simulations were performed for several values of $V_{pk}$, with $W/L$ fixed to 800. The results are shown in Fig. 5.11: $R_{\text{eq}}$ increases significantly as $V_{pk}$ decreases, as a consequence of the smaller amount of time the switch is turned on. Again, it is clear that using the average channel conductance to assess the equivalent switch resistance leads to a significant underestimation of $R_{\text{eq}}$.

Next, two coupled oscillators are considered (the oscillator core is described in detail in Section 5.4), with the single-ended amplitude of oscillation set to 1.1 V. The offset frequency at which the phase noise improvement afforded by oscillator coupling vanishes is estimated with (5.2) and $R_C = R_{\text{eq}}$, and compared to simulation results. As shown in Fig. 5.12, there is a very good agreement between theory and simulations. In Fig. 5.12, simulations are also compared to the predictions given by (5.2) if the impact of the switch is assumed to be described by the average channel conductance, i.e., with $R_C = 1/g_0$. In this case, there is a clear mismatch between simulations and calculations: for a target value of $\Delta f_c$, the switch has to be almost

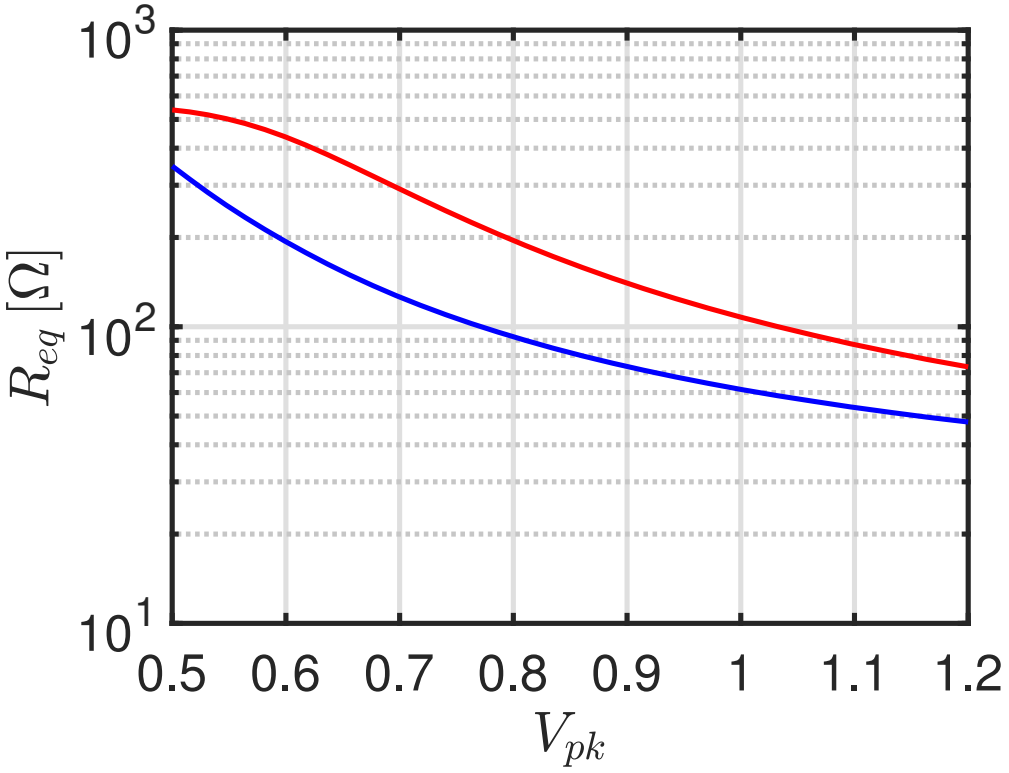


FIGURE 5.11: Equivalent switch resistance $R_{\text{eq}}$ vs oscillation amplitude (red curve). $R_{\text{eq}}$ is estimated for a switch with $W/L = 800$ using (5.15). The blue curve shows $1/g_0$ for comparison.

twice as large, compared to the outcome of a time-invariant analysis.

Finally, the phase noise penalty induced by $\Delta f_0$ is simulated at 1 MHz frequency offset for two coupled oscillators and compared to estimates obtained with (5.1) for a few values of the switch aspect ratio (as shown in [73], the effect of $\Delta f_0$ and $R_C$ together is to lower the oscillation amplitude, raising phase noise). The phase noise penalty estimates obtained setting $R_C = R_{\text{eq}}$ in (5.1) are compared to simulations with $\Delta f_0/f_0 = 1\%$ and $\Delta f_0/f_0 = 2\%$ in Fig. 5.13: the agreement is very good. Simulations are also compared to estimates obtained with $R_C = 1/g_0$, in which case we observe a substantial discrepancy.

The above several results emphasize the importance of the time-variant analysis of Section 5.3.1 to correctly assess the impact of the pMOS switch on the noise performance of the synchronized oscillator system. Based on phase noise simulations, the aspect ratio $W/L$ of the switch has been set to 800 (with, of course, minimum channel length) in order to keep the coupling resistance low and avoid phase noise degradation. Such a large figure may seem an overkill, but is in fact justified by the theoretical results just discussed.

Moreover, the data in Figs. 5.12-5.13 lead us to conclude that $R_{\text{eq}}$ impacts phase noise mainly through the indirect path via $\Delta f_0$ (qualitatively, the dualcore oscillator

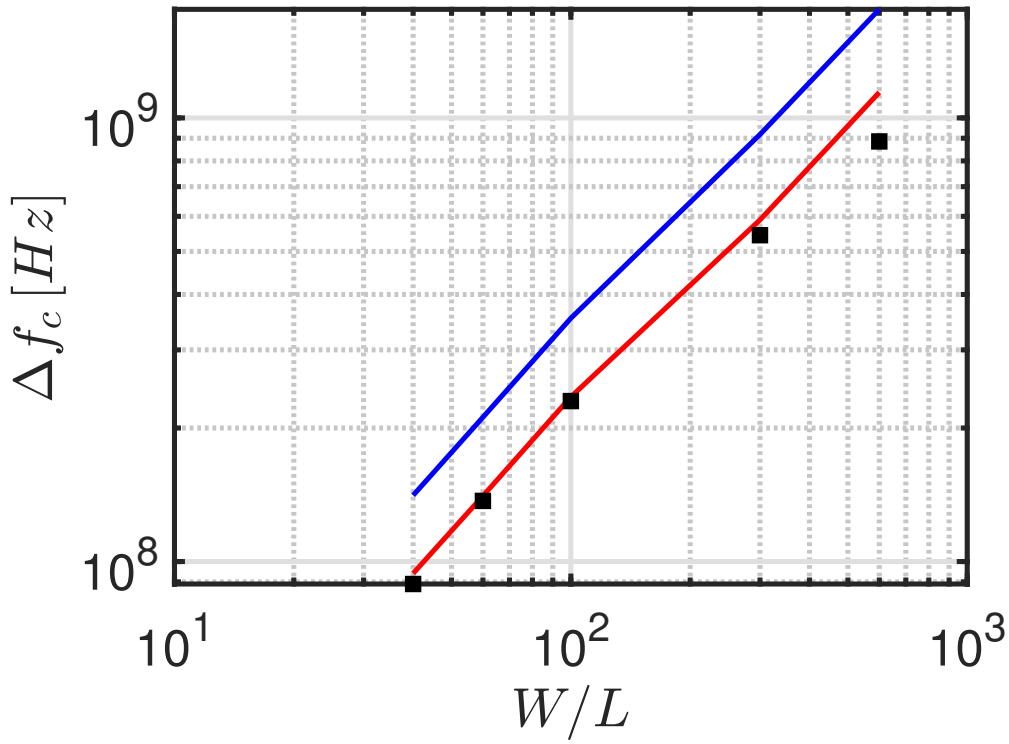


FIGURE 5.12: $\Delta f_c$ (defined in Fig. 5.4) vs switch aspect ratio. Simulations (black squares) are compared with estimates from (5.2) with $R_C = R_{\text{eq}}$ (red line) and $R_C = 1/g_0$ (blue line).

data of Fig. 5.13 applies to an octacore oscillator as well) rather than determining directly a low $\Delta f_c$, at least for reasonable values of component mismatch and offset frequencies. This conclusion justifies the great effort spent in ensuring the highest possible symmetry in the octacore oscillator array described in Section 5.2.

## 5.4 Design of the DCO core

The simplified schematic of the class-B oscillator core is shown in Fig. 5.14; pMOS devices are preferred to nMOS because of the lower amount of 1/f noise they produce, and are used both in the cross-coupled differential pair that sustains the oscillation, and in the biasing circuitry. The single-ended amplitude of oscillation is kept below 1.1 V to avoid any reliability concerns. The tail current source uses thick-oxide devices with a long channel to further reduce the 1/f noise current, whose power spectral density is approximately inversely proportional to channel length. In order to contain frequency pushing from the power supply, the tail current source is implemented as a high-swing cascode current mirror. RC filters with large time constants ($RC > 300\,\mu$s) block the noise from the reference branch of the tail current source, as shown in Fig. 5.14.

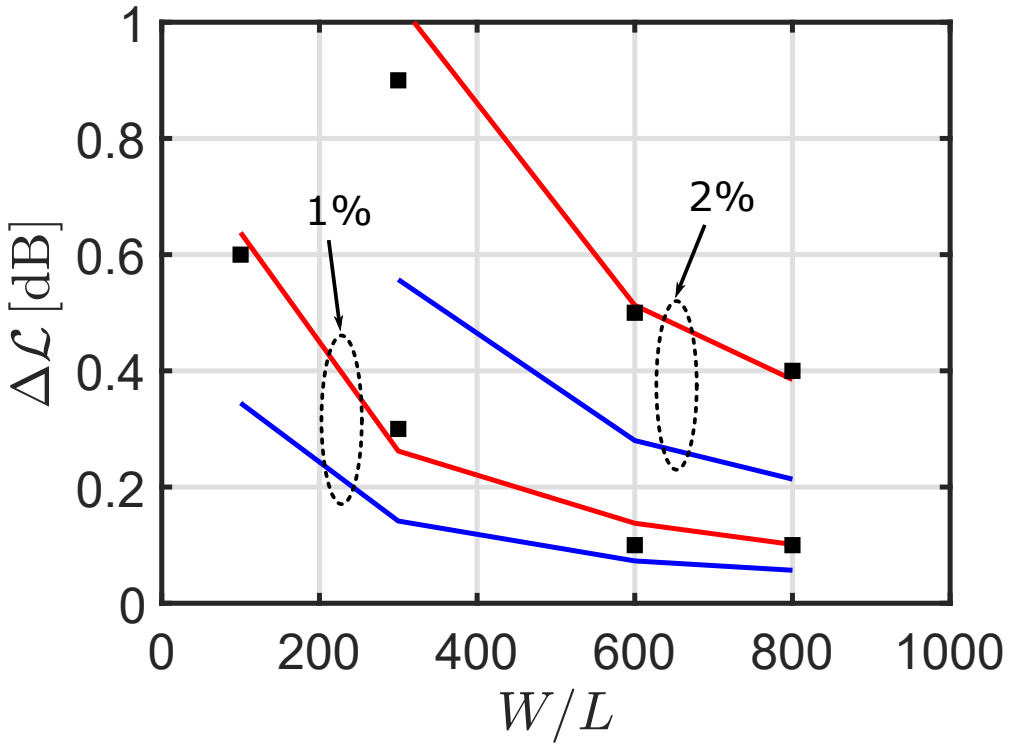


FIGURE 5.13: Phase noise penalty $\Delta\mathcal{L}$ at 1 MHz offset vs switch aspect ratio for $\Delta f_0/f_0 = 1\%$ and $\Delta f_0/f_0 = 2\%$. Simulations (black squares) are compared with estimates from (5.1) with $R_C = R_{\text{eq}}$ (red line) and $R_C = 1/g_0$ (blue line).

The LC resonator features a single-turn differential inductor $L_1$ of approximately 180 pH. Frequency tuning is achieved by means of a digitally-controlled bank of switched capacitors, segmented into three sub-banks: a 2-bit coarse bank, a 3-bit intermediate bank, and a 4-bit fine bank, a frequency resolution of 6 MHz.

The unit capacitor cell was sized taking into account opposing constraints: the width of switch $M_3$ (see Fig. 5.14) is selected based on the trade-off between the Q of the unit cell and the on/off capacitance ratio, while the large bias resistors $R > 10\,\text{k}\Omega$ avoid degrading the Q of the capacitor bank; their value, however, is limited by the need of keeping the switching time of the bank within the requirements set by the use of the DCO in a digital PLL.

Particular attention is devoted to the return path of the common-mode tank current, and a dedicated interconnection is provided to this aim. Its parasitic inductance, $L_{\text{tail}} \approx 160\,\text{pH}$ in Fig. 5.14, is carefully modeled by means of electromagnetic simulations and taken into account when tuning the tank common-mode resonance to the second harmonic, which reduces 1/f noise upconversion into phase noise [82, 83].

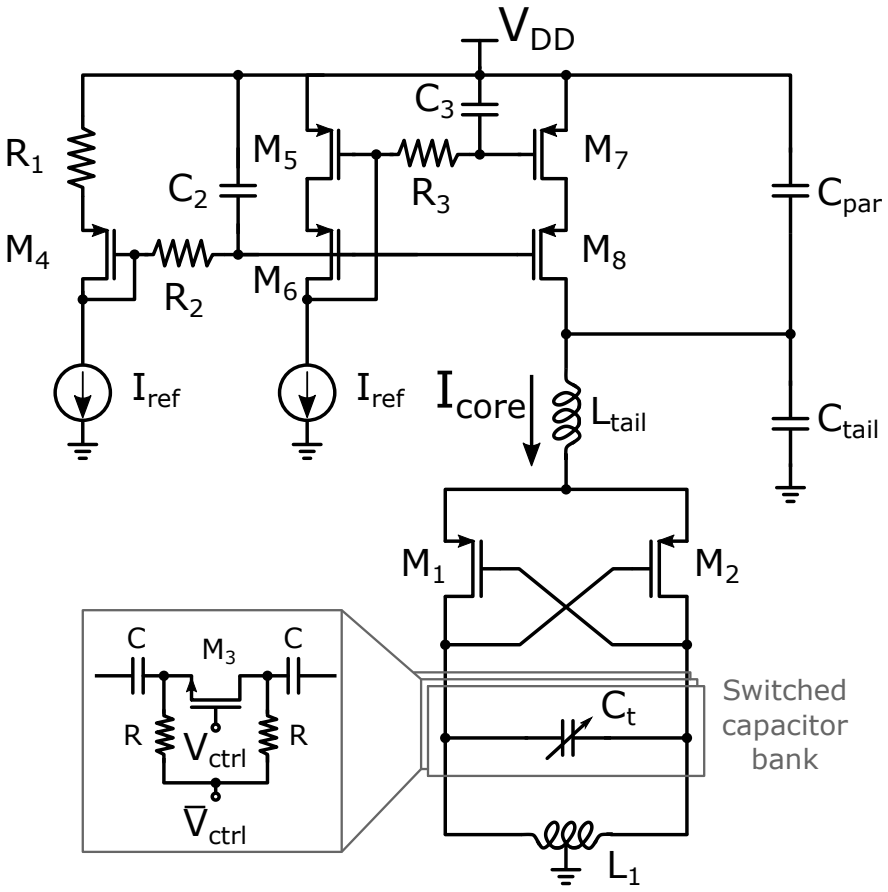


FIGURE 5.14: Simplified schematic of the DCO core.

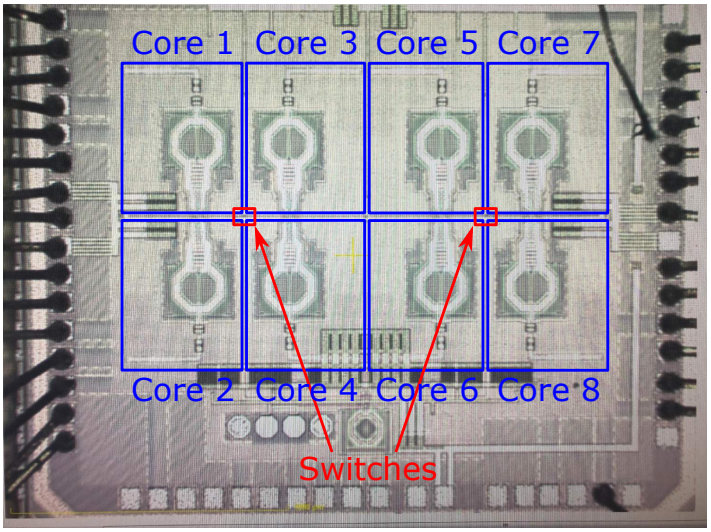


FIGURE 5.15: Chip microphotograph.

## 5.5 Measurement Results of the Octacore DCO

The octacore DCO has been fabricated in a 28 nm CMOS technology. A microphotograph of the die is shown in Fig. 5.15, where the overall area is about 3.1 $mm^2$ (this value was reported incorrectly in [81], as the layout shrinking factor had not been taken into account). The oscillator is powered by a 1.1 V supply.

The tuning range of the octacore DCO is as wide as 27%, spanning from 10.7 to 14.1 GHz, with a frequency resolution of 6 MHz. The measured phase noise is shown in Fig. 5.16 for an oscillation frequency of 10.7 GHz. Both the 8-core, 4-core and 2-core configurations are assessed. The phase noise at 1 MHz offset is as low as -126 dBc/Hz in the 8-core configuration, while the $1/f^3$ corner frequency is approximately 500 kHz. Phase noise increases by 3 dB in the 4-core configuration, and by 6 dB in the 2-core configuration, as expected. Phase noise has also been measured in the 6-core configuration, not shown in Fig. 5.16 for clarity: it is 1.2 dB higher than in the 8-core configuration, again as expected.

Figure 5.17 shows phase noise as a function of the bias current $I_{core}$ in each oscillator core for a few values of the frequency offset when the oscillator is operated in 8-core configuration at 10.7 GHz. The minimum phase noise level is achieved with $I_{core} = 19.6$ mA. The optimal value of $I_{core}$ decreases at higher frequencies, as a consequence of the increasing tank equivalent resistance at resonance.

The phase noise performance of the octacore DCO across the tuning range is reported in Fig. 5.18. We notice that there is a slight phase noise increase at 10 MHz offset as the oscillation frequency increases: this is in line with the expected phase noise dependence on the oscillation frequency. At lower offsets, however, we observe a larger increase of the $1/f^3$ sideband with the oscillation frequency than was

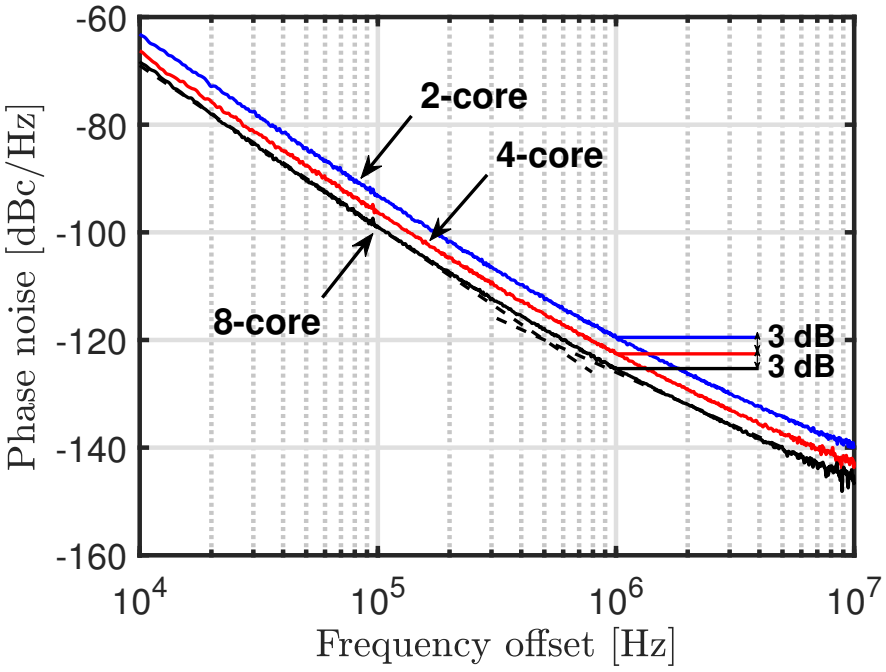


FIGURE 5.16: Measured phase noise for 8-core, 4-core, and 2-core oscillator configuration operating at 10.7 GHz.

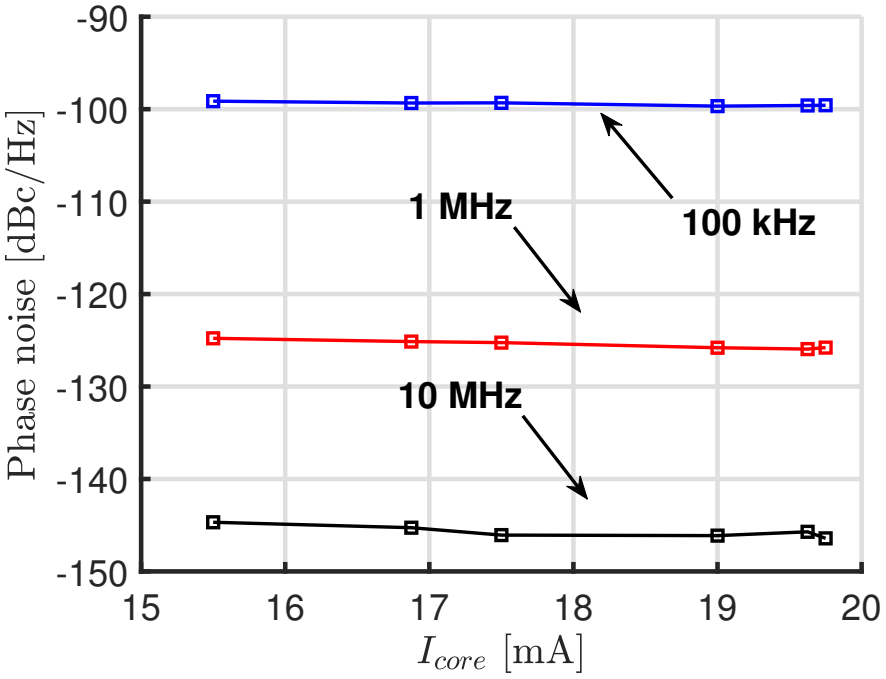


FIGURE 5.17: Phase noise of the octacore DCO at 10.7 GHz and three frequency offsets vs bias current in each oscillator core.

TABLE 5.1: Performance summary and comparison with the state-of-the-art.

| | **This work** | [72] | [73] | [74] | [70] | [36] | [75] | [76] | [77] | [71] | [83] | [68] | [84] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Technology | **28 nm CMOS** | 130 nm BiCMOS | 55 nm BiCMOS | 65 nm CMOS | 40 nm CMOS | 65 nm CMOS | 40 nm CMOS | 65 nm CMOS | 40 nm CMOS | 65 nm CMOS | 28 nm CMOS | 28 nm CMOS | 65 nm CMOS |
| Number of cores | **8** | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 2 | 1 | 1 | 1 |
| Center frequency [GHz] | **12.4** | 15 | 20 | 54 | 27 | 47 | 29.4 | 56.4 | 3.6 | 4.5 | 27 | 19.5 | 5.7 |
| Tuning range [%] | **27** | 16 | 15 | 9 | 26 | 17 | 73 | 14 | 27 | 19 | 14 | 12 | 24 |
| Phase noise at 1 MHz [dBc/Hz] | **-126** | -124 | -118.5 | -111 | -110 | -106 | -108.5 | -105 | -139 | -137 | -106 | -112 | -128 |
| Eq. phase noise referred to 10.7 GHz at 1 MHz [dBc/Hz] | **-126** | -127 | -124 | -125 | -117 | -119 | -113 | -120 | -128 | -129 | -114 | -117 | -122 |
| $V_{dd}$ [V] | **1.1** | 3 | 1.2 | 1.2 | 0.95 | 0.9 | 1.1 | 0.55 | 1.1 | 2.15 | 1 | 0.9 | 0.4 |
| $P_{DC}$ [mW] | **173** | 72 | 50 | 146 | 16 | 21.5 | 9 | 24 | 23 | 127 | 12 | 21 | 6 |
| FoM [dBc/Hz] | **-184** | -189 | -187.5 | -184 | -187 | -186.5 | -181 | -186.5 | -195 | -189 | -184 | -185 | -195 |
| Area [$mm^2$] | **3.1** | 1 | 0.6 | 1.7 | 0.1 | 0.04 | 0.08 | 0.032 | 0.36 | 0.37 | 0.15 | 0.07 | 0.24 |

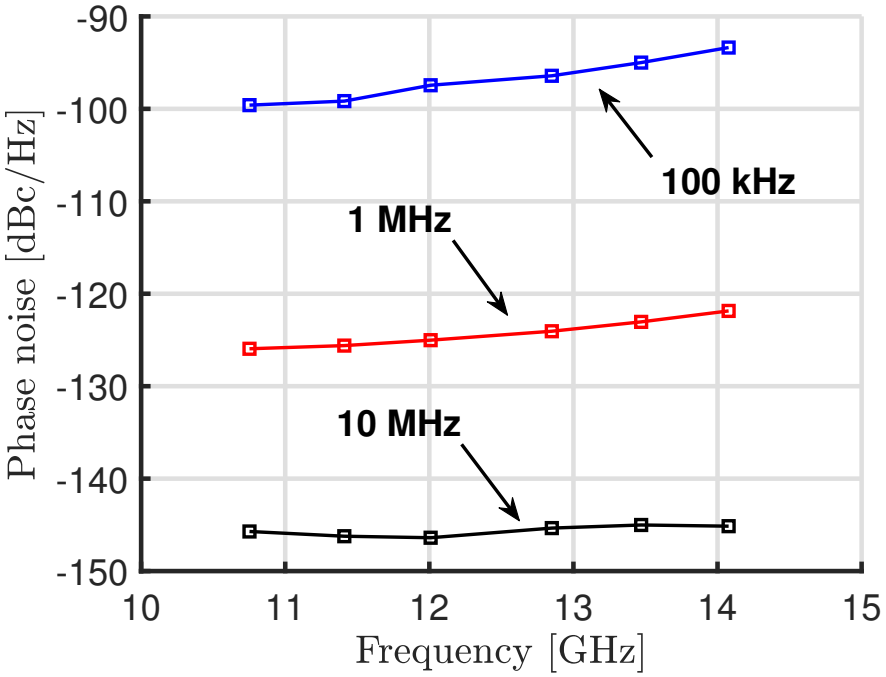


FIGURE 5.18: Phase noise of the octacore DCO across tuning range.

expected from simulations. This is also captured by the results in Fig. 5.19, where the DCO $1/f^3$ corner frequency is reported across the tuning range. The increase of the $1/f$ noise upconversion may be due to a mistuning of the common-mode resonance of the tank caused by unaccounted parasitics, despite the efforts made in the design phase.

The measured phase-noise figure-of-merit (FoM) varies between -185 and -184 dBc/Hz across the tuning range, as illustrated in Fig. 5.20.

The measured supply frequency pushing is reported in Fig. 5.21. As a consequence of the use of a cascode tail current source in the DCO cores, an excellent frequency pushing lower than 12 MHz/V across the tuning range was measured.

The octacore DCO performance is summarized in Table 5.1 and compared to state-of-the-art multicore oscillators as well as to high-performance single-core oscillators. The comparison is also illustrated in Fig. 5.22, where the oscillator performance is reported in a concise form as a phase noise (normalized to a common carrier frequency) versus FoM scatter plot (better performance towards bottom-left corner).

When compared to multicore oscillators operating beyond 10 GHz, the octacore DCO achieves the best phase noise among CMOS implementations [36, 70, 73, 74, 76], almost reaching the performance of bipolar circuits, which can leverage higher supply voltages [72]. Notably, the octacore DCO is the only multicore oscillator in Table 5.1 and Fig. 5.22 implemented in a 28 nm CMOS technology. A comparison with high-performance single-core implementations in 28 nm CMOS [68, 83] shows

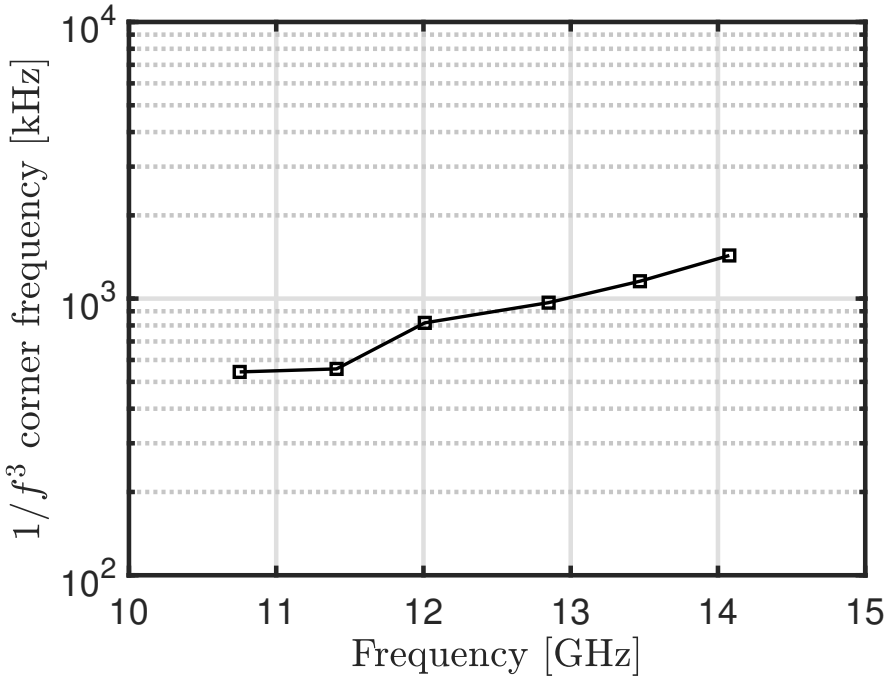


FIGURE 5.19: $1/f^3$ corner frequency of the octacore DCO across tuning range.

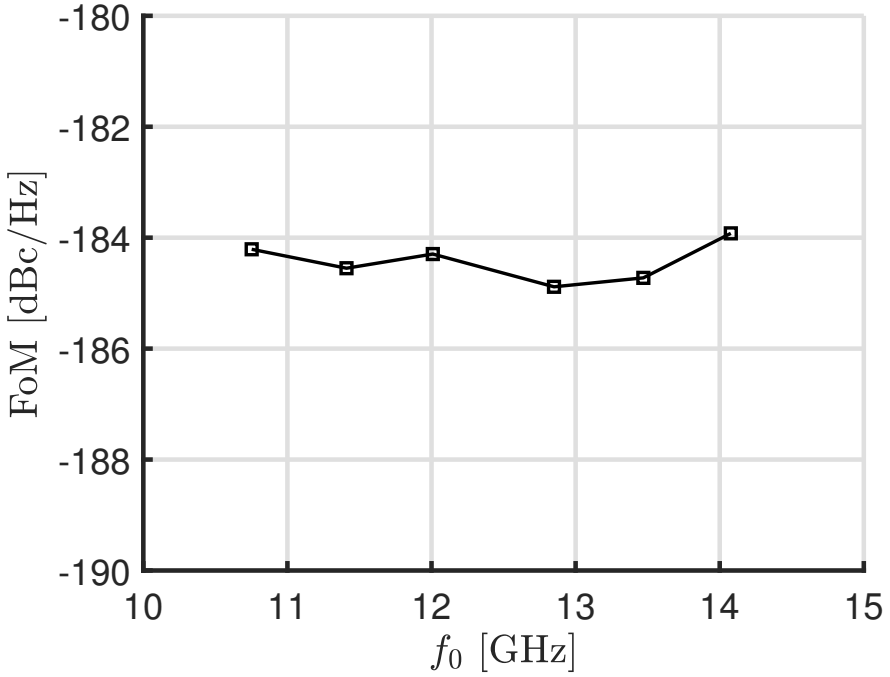


FIGURE 5.20: FoM across tuning range.

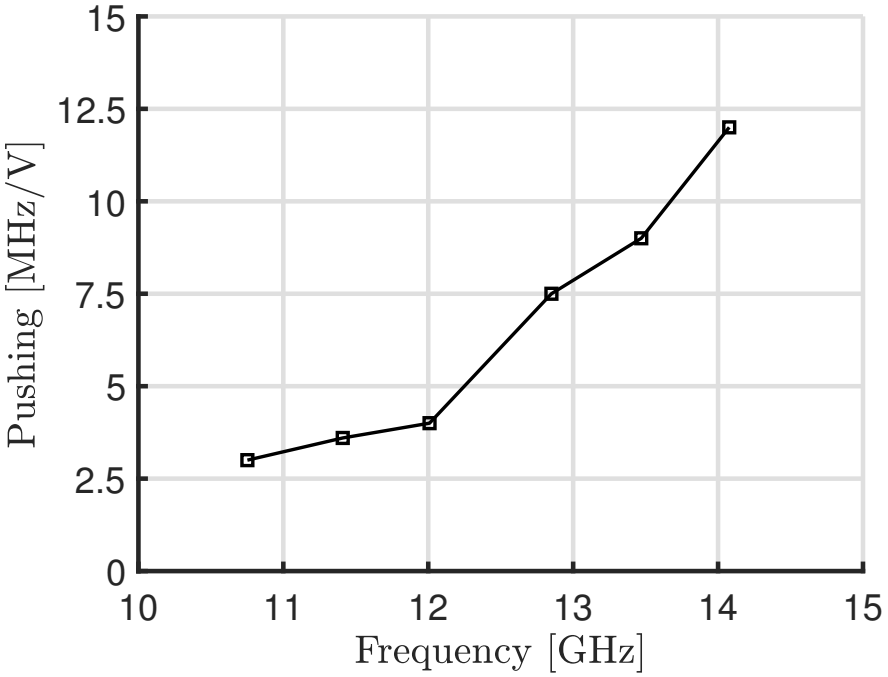


FIGURE 5.21: Frequency pushing from power supply.

similar FoMs on the one hand, and, on the other hand, that the excellent phase noise performance of the octacore DCO is both due to the multicore topology, and to the intrinsic good performance of its class-B cores. It is also interesting to notice that the designs operating below 10 GHz [71,77,84] leverage the higher tank Q achievable in the sub-10 GHz range [69] to deliver a higher performance, both in terms of phase noise and FoM.

## 5.6 A summary of the octa-core DCO performance

Achieving a very low phase noise and being able to do so in a scalable fashion over a wide range of power consumption levels, trading a lower phase noise for a higher power consumption with no excess noise penalty, is not an easy feat to accomplish. This Chapter presented an octacore design where power consumption and phase noise can be scaled over 4 different core configurations (2-core, 4-core, 6-core, and 8-core) without any appreciable drawbacks. This was attained both by optimizing the circuit architecture, strategically placing a limited number of switches in the coupling network without sacrificing flexibility, and by carefully designing the coupling network itself.

A thorough time-variant analysis of the equivalent resistance of the coupling switch was carried out, emphasizing the trade-off between switch size and overall performance of the coupled oscillator array. The 28 nm CMOS prototype shows

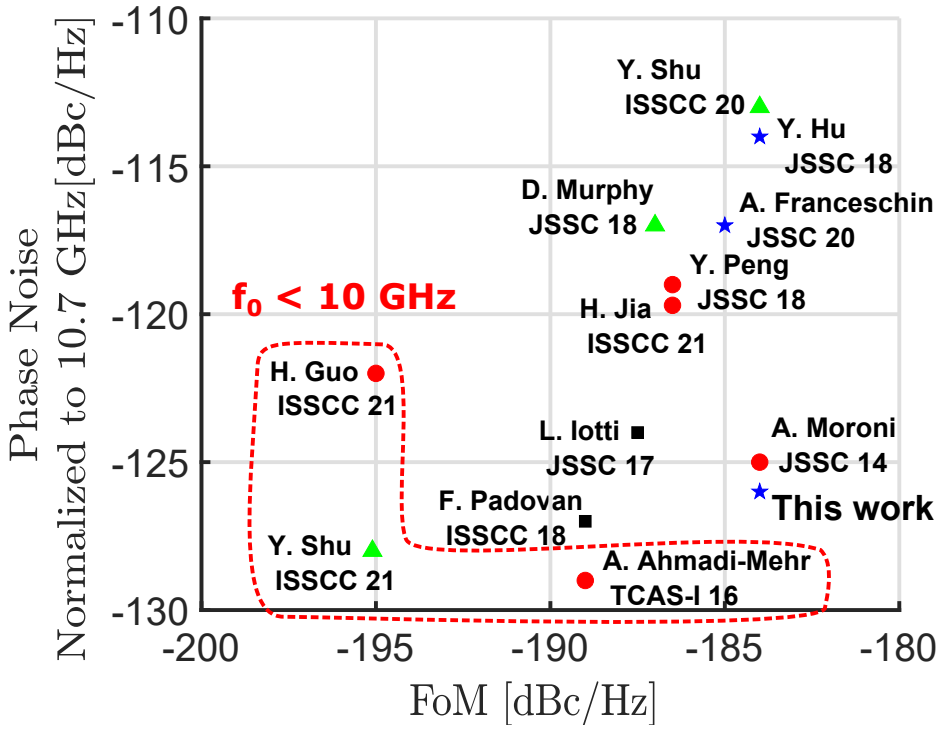


FIGURE 5.22: Comparison with state-of-the-art oscillators. Designs in: ⋆ 28 nm CMOS; □ BiCMOS; ○ 65 nm CMOS; △ 40 nm CMOS.

a 27% tuning range and a phase noise of −126 dBc/Hz at 1 MHz offset from the 10.7 GHz carrier, with a FoM of −184 dBc/Hz and an excellent pushing performance of less than 12 MHz/V.

# Chapter 6

# A 10 GHz Transformer-Feedback Based Series VCO in 22 nm FD-SOI

Most integrated harmonic oscillators are implemented with a parallel LC resonant tank [68, 71, 73, 85] that filters the current coming from the active devices. The LC tank operates in its parallel resonance, where it shows a large equivalent parallel resistance $R_P$ at the frequency $\omega_0 = 1/\sqrt{LC}$. While widely adopted, this topology faces insurmountable challenges when an extremely low phase noise is needed. In particular the oscillation frequency is limited by the supply, technological scaling and reliability concerns. The only other feasible way to reduce the phase noise is to reduce the value of tank inductance L, but this is only possible up to a certain point without seriously degrading its quality factor Q, and before the explicit inductance becomes comparable to the parasitic one introduced by the interconnections.

These limitations are intrinsic to the parallel topology, so a shift to a new topology is needed: the series LC resonant oscillator. As the name suggests, it exploits the LC series resonance to filter the voltage waveform coming from the active devices. In this case the active core acts as a voltage source (small output impedance) rather than a current source. In this case the current is sinusoidal while the voltage applied to the tank, $V_T$, can be a harmonic-rich signal. The higher the Q of the resonator, the lower the equivalent resistance $R_S$ at the resonance, the higher the current across the tank. If the LC tank is driven by a square wave voltage with swing 0-$V_{DD}$ and fundamental frequency $\omega_0$, the first harmonic current flowing through the tank is

$$I_0 = \frac{2}{\pi}\frac{V_{DD}}{R_S} \tag{6.1}$$

The oscillation voltage amplitude of the first harmonic across the L or C is given by

$$A_0 = I_0\omega_0 L = \frac{2}{\pi}V_{DD}Q \tag{6.2}$$

At mm-wave, the tank Q can be higher than 10 and the oscillation amplitude is

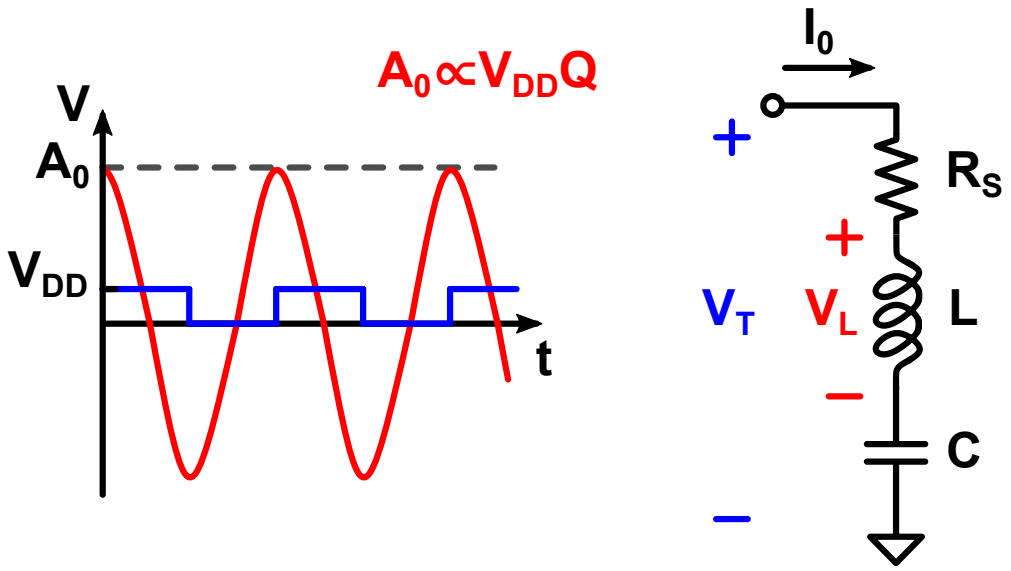


FIGURE 6.1: Sketch of the voltage waveforms in a RLC series resonator at $\omega_0$: in blue the voltage across the tank $V_T$; in red the voltage across the inductor $V_L$.

much bigger than $V_{DD}$, allowing for very low phase noise. Additionally, the high amplitude oscillation is found across the reactive elements of the tank, which can tolerate such high voltages – even in ultra-scaled technologies – while the active devices are only subject to the much smaller 0-$V_{DD}$ excursion.

Another advantage of series-resonance VCOs concerns the conversion of MOS noise into phase noise. In fact, it can be demonstrated that, unlike in the parallel oscillator where the actives noise contribution is proportional $\gamma$ (the MOS channel noise factor), in the series oscillator this contribution can be made negligibly small. If the MOS devices are operating as switches (deep triode when switched on) their noise contribution only comes from the channel resistance $R_{DS,on}$, which degrades the tank Q factor. However, if large enough devices are employed, this degradation can be avoided. In reality, given the finite rise and fall-times of the signals at the gate and drains, the active devices spend a (small) portion of time in saturation, where the white noise contribution increases and some flicker noise is also injected and upconverted into phase noise [63].

The phase noise advantage of the series oscillator can be better appreciated by comparing it to the parallel case. Let us consider the two oscillators in Fig. 6.2. For a fair comparison the two oscillator have identical operating frequency $\omega_0 = 1/\sqrt{LC}$, first harmonic amplitude $V_T$ and quality factor $Q$. The phase noise equation for the series oscillator with noiseless actives (Fig. 6.2(b)) is [63]

$$\mathcal{L}_{series}(\Delta\omega) = 10\log\left[\frac{k_B T}{V_T^2}\frac{R_S}{Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \tag{6.3}$$

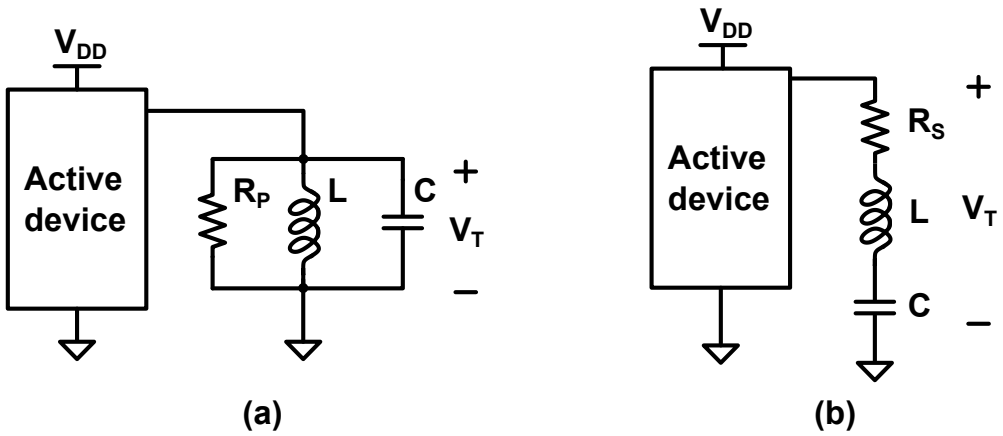


FIGURE 6.2: Schematic of a parallel (a) and series oscillator (b).

where $k$ is the Boltzmann constant, $T$ the temperature in Kelvin, and $R_S$ is the tank equivalent series resistance at the resonance. Recalling that the parallel oscillator (Fig. 6.2(a)) phase noise is given by

$$\mathcal{L}_{parallel}(\Delta\omega) = 10\log\left[\frac{k_B T}{V_T^2}\frac{R_P}{Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \tag{6.4}$$

where $R_P$ is the equivalent parallel resistance at the resonance. Recalling that at $\omega_0$ $R_S/R_P = 1/Q^2$, the phase noise improvement can be defined as

$$\Delta\mathcal{L}(\Delta\omega) = \mathcal{L}_{series}(\Delta\omega) - \mathcal{L}_{parallel}(\Delta\omega) = 10\log\left[\frac{R_S}{R_P}\right] = -10\log Q^2 \tag{6.5}$$

The series oscillator can achieve a better phase noise than the parallel oscillator of a factor of $1/Q^2$. At mm-wave, where the quality factor of the tank often exceeds 10, this can lead to a theoretical lowering of 20 dB of phase noise. In practice the phase noise improvement may be limited by other considerations such as the noise from the active devices or possible degradation of the tank $Q$ due to the need to use passives able to withstand higher voltages.

The concept of a series oscillator is not new as it was explored in [63] but without a prototype example, then in [64] a BiCMOS implementation of a series oscillator shows a -138 dBc/Hz phase noise at 10 GHz at 1 MHz offset but its topology cannot be easily adapted to a CMOS process. The first CMOS working prototype of a series quadrature oscillator is found in [65] but the need for four different LC tanks implies a large area consumption.

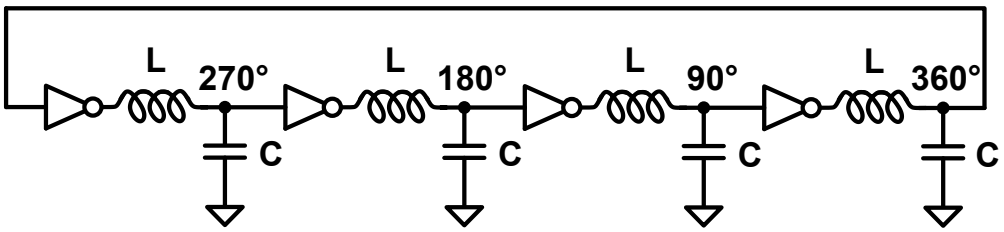


FIGURE 6.3: Schematic of a four-stage series oscillator.

## 6.1 Analysis of the Feedback Network

To implement a series oscillator we need an active device capable of starting and maintaining the oscillation, a tank and a feedback network. In parallel oscillator the active device acts as a negative admittance at the equilibrium (small-signals) and as a current generator in steady state. For the series oscillator we need a negative resistance at the equilibrium to start the oscillation and a device that acts as a voltage generator at steady-state. The cross-couple differential-pair satisfies the equilibrium condition but not the steady-state behaviour, we have to look elsewhere for a solution. CMOS transistors in ultra-scaled technologies are very good switches as their performance benefits from technological scaling (low on resistance, smaller parasitics) and the output resistance of a CMOS inverter can be made very small, provided that large enough transistors are used, so small that its large signal operation could be approximated to a voltage-controlled voltage-source (VCVS). On the other hand, if the inverter gates are biased at the logic threshold, both the pMOS and the nMOS are in saturation and act as trasconductors. The CMOS inverter is then a candidate to implement the actives for the series oscillator.

In the cross-couple differential-pair, the feedback network is built by simply connecting the gate to the drain of the other transistor. For the series oscillator there is no immediate solution. One way, proposed in [63] and demonstrated in practice in [65] exploits the $\pm 90^\circ$ phase shift of the voltage depending if the signal is taken across the inductor or capacitor. The Barkhausen criterion requires a $\pm 360^\circ$ total phase shift, easily obtained by cascading four stages as shown in 6.3. The main drawback of this topology is determined by the presence of four separate inductors that demand a large of area. Moreover, the input capacitance of the inverters is connected in parallel to the tank capacitance, reducing the tuning range.

Since the CMOS inverter already introduces a phase shift of $180^\circ$, to satisfy the Barkhausen criterion we need a feedback network that adds the remaining $180^\circ$ of phase shift. As we have seen, the tank itself can only provide $90^\circ$ and an additional network is required to reach $180^\circ$. The proposed series VCO is shown in Fig. 6.4:

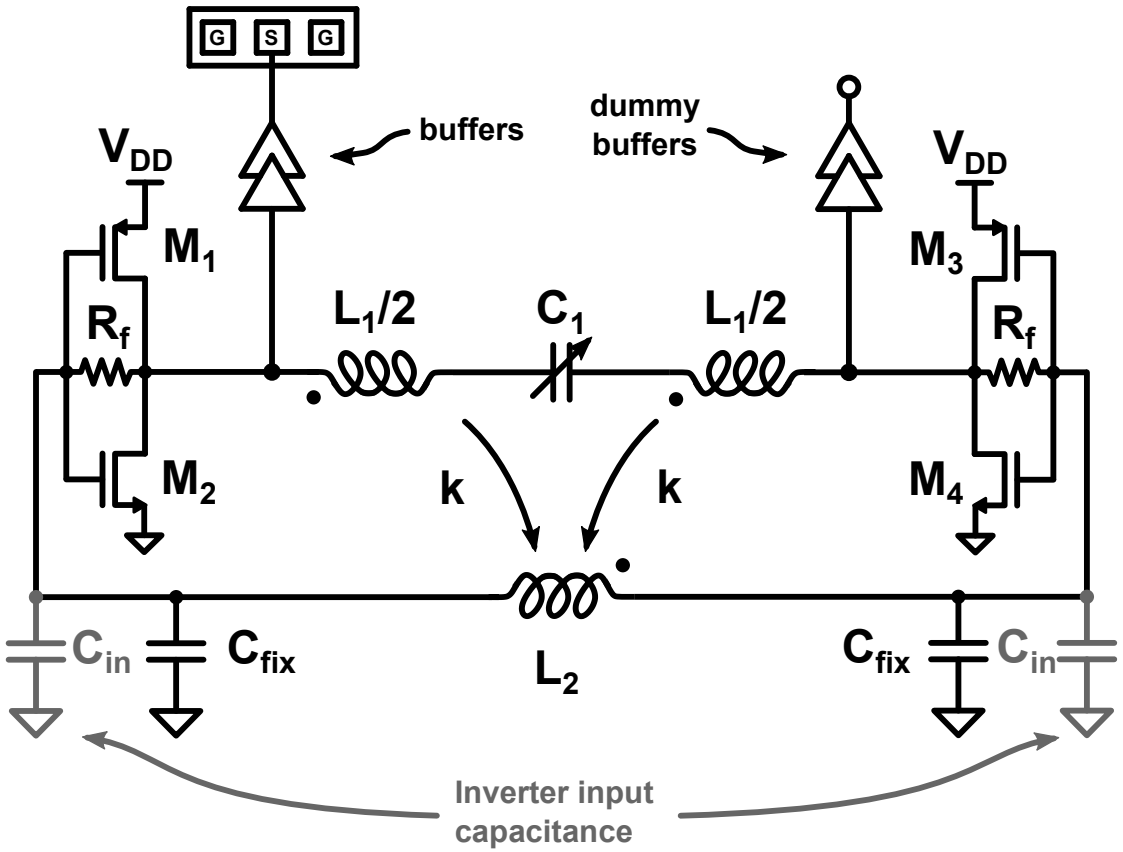


FIGURE 6.4: Schematic of the proposed series VCO.

$M_{1\text{-}4}$ form the CMOS inverters and the resistors $R_f$ are needed to self-bias the inverters to their logic threshold at equilibrium for the startup of the oscillator. The tank is composed by a doubly-tuned transformer network that introduces the 180° phase shift and provides passive voltage gain to maintain the oscillation. The input capacitance of the inverters $C_{in}$ is resonated with $L_2$.

The study of the passive network starts by considering the equivalent single-ended schematic of the VCO in Fig. 6.5, where $C_2 = (C_{in} + C_{fix})/2$. For now, $M_1$ and $M_2$ are considered ideal, with nil input capacitance and nil output resistance. At startup the self-biased inverter operates as a trasconductor, injecting current into the feedback network which is then converted into voltage by the transimpedance of the network and fed back to the inverters. The oscillation grows in amplitude until the swing at the inverter output is limited by the voltage supply, at this point $M_1$ and $M_2$ operate as switches in deep triode and the inverter becomes a VCVS, applying a voltage to the feedback network that is amplified and fed back. Therefore, the network has to operate as a transimpedance at startup and as a voltage amplification at large signal. The active devices are disconnected and the passive feedback network can be rearranged in a two port configuration as shown in Fig. 6.6.

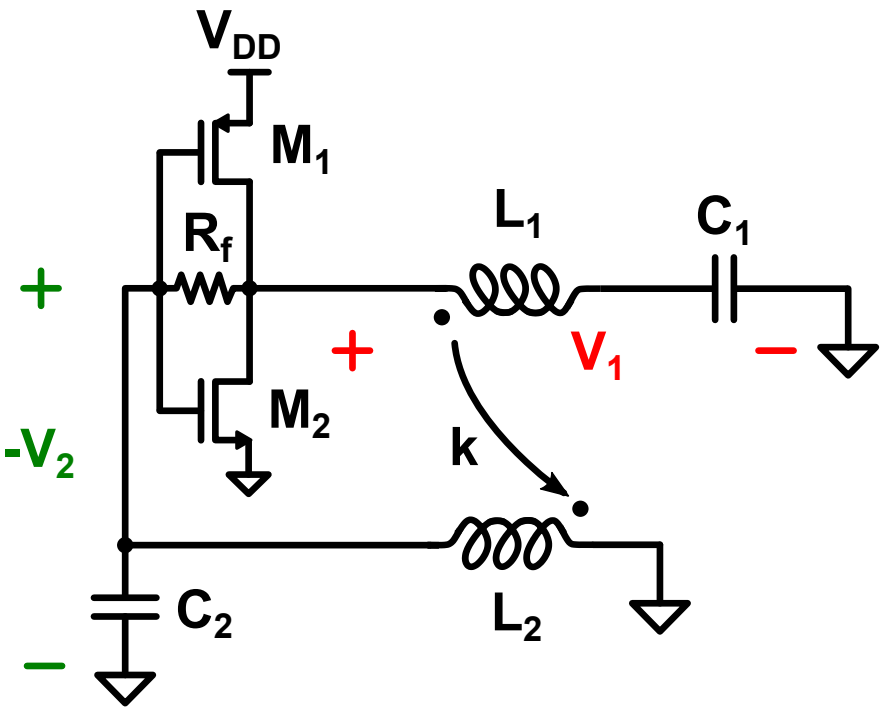


FIGURE 6.5: Equivalent single-ended schematic of the VCO.

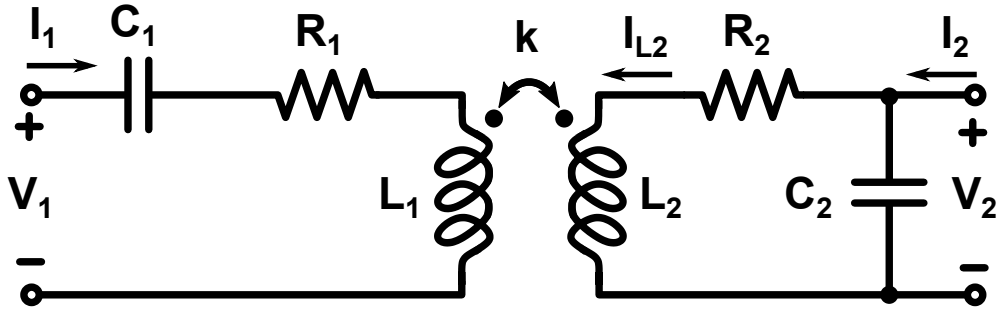


FIGURE 6.6: Equivalent schematic of the doubly-tuned transformer based feedback network.

For the purpose of this analysis we are interested in computing the the equivalent impedance seen from the actives at the resonance $Z_{11}(j\omega_0)$, the transimpedance $Z_{21}(j\omega_0)$ necessary to calculate the loop gain at startup, and the voltage gain $A_v(j\omega) = V_2/V_1 = Z_{12}/Z_{11}$ of the network for large signal operation. After some algebra, we obtain

$$Z_{11}(j\omega) = \left.\frac{V_1}{I_1}\right|_{I_2=0} = Z_1\left(1 + \frac{\omega^2 k^2 L_1 L_2}{Z_1 Z_2}\right) \tag{6.6}$$

$$Z_{21}(j\omega) = Z_{12}(j\omega) = \left.\frac{V_2}{I_1}\right|_{I_2=0} = \frac{\omega^2 k^2 L_1 L_2}{C_2 Z_2} \tag{6.7}$$

where

$$Z_1(j\omega) = \frac{1}{j\omega C_1} + j\omega L_1 + R_1 \tag{6.8}$$

$$Z_2(j\omega) = \frac{1}{j\omega C_2} + j\omega L_2 + R_2 \tag{6.9}$$

By setting $L_1C_1 = L_2C_2 = 1/\omega_0^2$, at the resonance $Z_1(j\omega_0) = R_1$ and $Z_2(j\omega_0) = R_2$ and (6.6), (6.7) become

$$R_{11} = Z_{11}(j\omega_0) = R_1\left(1 + k^2 Q_1 Q_2\right) = R_1(1+\varepsilon) \tag{6.10}$$

$$R_{21} = Z_{21}(j\omega_0) = \frac{\omega_0^2 k^2 L_1 L_2}{C_2 R_2} = R_1 \varepsilon \frac{n}{k} \tag{6.11}$$

from which immediately follows

$$A_v(j\omega_0) = \frac{R_{21}}{R_{11}} = \frac{\varepsilon}{1+\varepsilon}\frac{n}{k} \tag{6.12}$$

where $Q_1$ and $Q_2$ are respectively the primary and secondary resonator quality factor and $n = \sqrt{L_2/L_1}$ is the turn ratio of the mutual inductor. At equilibrium, the loop gain of the oscillator is given by

$$T = -2g_m R_{21} = -2g_m R_1 \varepsilon \frac{n}{k} \tag{6.13}$$

where $g_m$ is the transconductance of $M_1$ and $M_2$. The effect of $R_f$ can be safely ignored if its value is sufficiently high. Equation (6.10) shows that the equivalent series resistance of the tank at the resonance is increased by a factor of $1+\varepsilon$ due to the loading effect of the secondary resonator. Since $\varepsilon \propto Q_2$, the tank degradation can be mitigated by decreasing the secondary resonator quality factor. One might be misled into thinking that the degradation can be made virtually negligible by arbitrarily decreasing $\varepsilon$, however the startup condition $|T| > 1$ and (6.13) immediately set a minimum $\varepsilon$ required.

To study the phase noise of the proposed topology, it is useful to rewrite (6.3) as

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{k_B T R_{n,eq}}{(I_1 \Delta\omega L_1)^2}\right] \tag{6.14}$$

where $I_1$ is the first harmonic current through the tank and $R_{n,eq}$ is the equivalent noise resistance of the tank. The presence of the secondary resonator impacts the phase noise through two different mechanisms: 1) increasing the electrical series resistance of the tank $R_{11}$ thus decreasing of the equivalent tank quality factor $Q_{eq} = Q_1/(1+\varepsilon)$; 2) $R_2$ injects noise into the tank increasing the equivalent input referred noise of the network $v_{n,eq}$. This effect can be modelled by an equivalent noise resistance $R_{n,eq}$ so that

$$\frac{\overline{v_{n,eq}}^2}{\Delta\omega} = 4k_B T R_{n,eq} \tag{6.15}$$

note that for this particular circuit $R_{eq,n} \neq R_{11}$. In light of the foregoing considerations, (6.14) becomes

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{k_B T R_n R_{11}^2}{(V_1 \Delta\omega L_1)^2}\right] = 10\log\left[\frac{k_B T}{V_1^2}\frac{R_{n,eq}}{Q_1^2}(1+\varepsilon)^2\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \tag{6.16}$$

To determine $R_{n,eq}$, we first compute the output noise and then refer it to the input (Fig. 6.7). After some algebra, it is possible to express the input referred noise only as a function of $R_1$ and $\varepsilon$

$$\frac{\overline{v_{n,eq}}^2}{\Delta\omega} = 4k_B T R_1\left(1+\frac{1}{\varepsilon}\right) \tag{6.17}$$

hence

$$R_{n,eq} = R_1\left(1+\frac{1}{\varepsilon}\right) \tag{6.18}$$

By plugging (6.18) into (6.16) we arrive at the final expression of the phase noise of the proposed series VCO

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{k_B T}{V_1^2}\frac{R_1(1+\varepsilon)^2\left(1+\frac{1}{\varepsilon}\right)}{Q_1^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \tag{6.19}$$

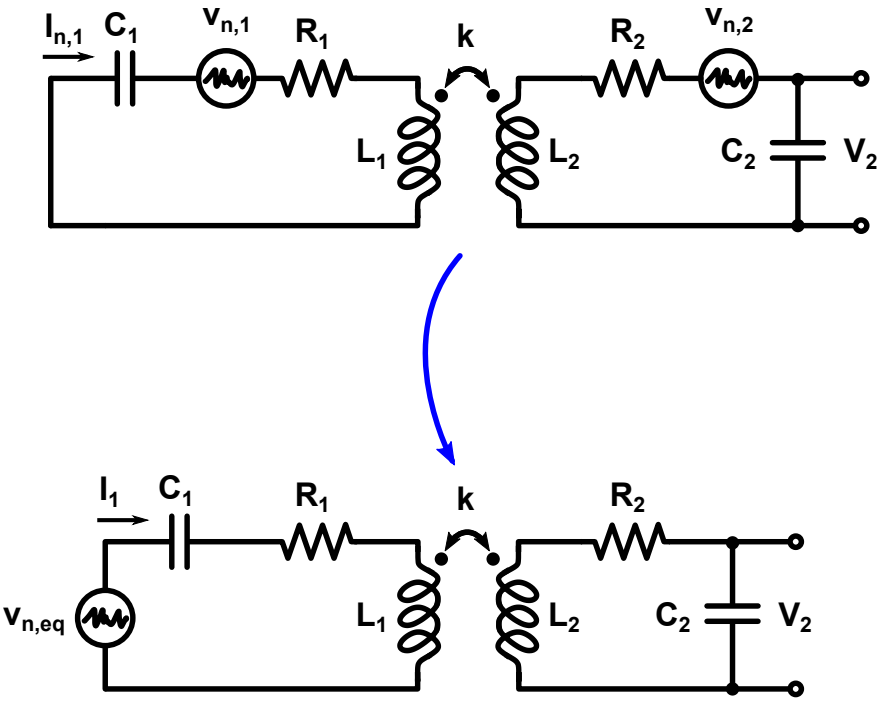


FIGURE 6.7: Input referred noise of the passive feedback network.

The presence of the secondary resonator introduces a phase noise penalty over an ideal oscillator with a $L_1C_1$ resonator with a quality factor $Q_1$ of

$$\Delta\mathcal{L}(\varepsilon) = 10\log\left[(1+\varepsilon)^2\left(1+\frac{1}{\varepsilon}\right)\right] \tag{6.20}$$

Interestingly, (6.20) shows that the phase noise penalty cannot be nil as it has a minimum value of 8.3 dB for $\varepsilon = 0.5$, regardless of the specific network values. In other words, the presence of the secondary resonator required to complete the feedback network, decreases the series oscillator phase noise advantage to $20\log Q_1 - 8.3\,dB$. This is not a deal breaker as the quality factor of the tank can easily reach values above 10 at mm-wave, thus leaving more than 12 dB of theoretical improvement over the parallel topology.

## 6.2 Impact of the Inverters on Phase Noise

The presence of active devices introduces white and flicker noise in the oscillator. This section will focus on the injection of white noise by the CMOS transistors at large signal regime; the flicker noise contribution is naturally limited by the large dimensions of the active devices required for the operation of the series oscillator.

In steady-state, the oscillation amplitude at the gate of the inverters is supposed to be large enough to push the transistors in deep-triode region. If the pMOS and

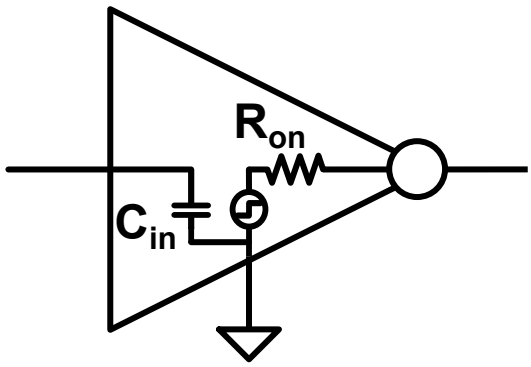


FIGURE 6.8: The inverter can be seen as an equivalent Thevenin VCVS with output impedance $R_{on}$ and input capacitance $C_{in}$.

nMOS are sized with identical on resistance $R_{on}$, the inverter behaves like an equivalent Thevenin VCVS with an output resistance of $R_{on}$ and input capacitance $C_{in}$. The output resistance is placed in series with the tank and can be incorporated in the tank series resistance so that $R_1' = R_1 + R_{on}$, and the transistors have nil on resistance (Fig. 6.9). In this way (6.16) can be easily adapted to take into account the added resistance from the inverters: by replacing $R_1$ with $R_1'$ we have that

$$R_{11} = R_1 \left(1 + \varepsilon + \frac{R_{on}}{R_1}\right) \tag{6.21}$$

and

$$R_{n,eq} = R_1 \left(1 + \frac{R_{on}}{R_1}\right) \left(1 + \frac{1 + \frac{R_{on}}{R_1}}{\varepsilon}\right) \tag{6.22}$$

which lead us to the new phase noise expression

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{k_B T}{V_1^2}\frac{R_1}{Q_1^2}\left(1 + \varepsilon + \frac{R_{on}}{R_1}\right)^2 \left(1 + \frac{R_{on}}{R_1}\right) \left(1 + \frac{1 + \frac{R_{on}}{R_1}}{\varepsilon}\right) \left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \tag{6.23}$$

While the $R_{on}$ decreases when increasing the MOS form factor $W/L$, the input capacitance of the inverter $C_{in}$ increase with along the gate area $WL$. In the proposed topology, $C_{in}$ loads the second port of the feedback network so, to maintain the same natural frequency $\omega_0$, once $L_2$ is fixed, a maximum $C_{in}$ is also fixed and, in turn, a maximum gate area $WL$. Since the minimum length of the devices $L_{min}$ is technology dependent, the gate area constraint immediately sets the minimum inverter output resistance achievable for any given $L_2$. Moreover, from (6.12), $A_v(j\omega_0) \propto n = \sqrt{L_2/L_1}$ meaning that, in order to maintain the oscillation, there's a minimum value of $L_2$ and, thus, minimum $R_{on}$. Interestingly, this topology benefits from the scaling of the channel length, as it tends to reduce the MOSFET capacitances as well as the channel resistance. In any case, this constraint can be used to

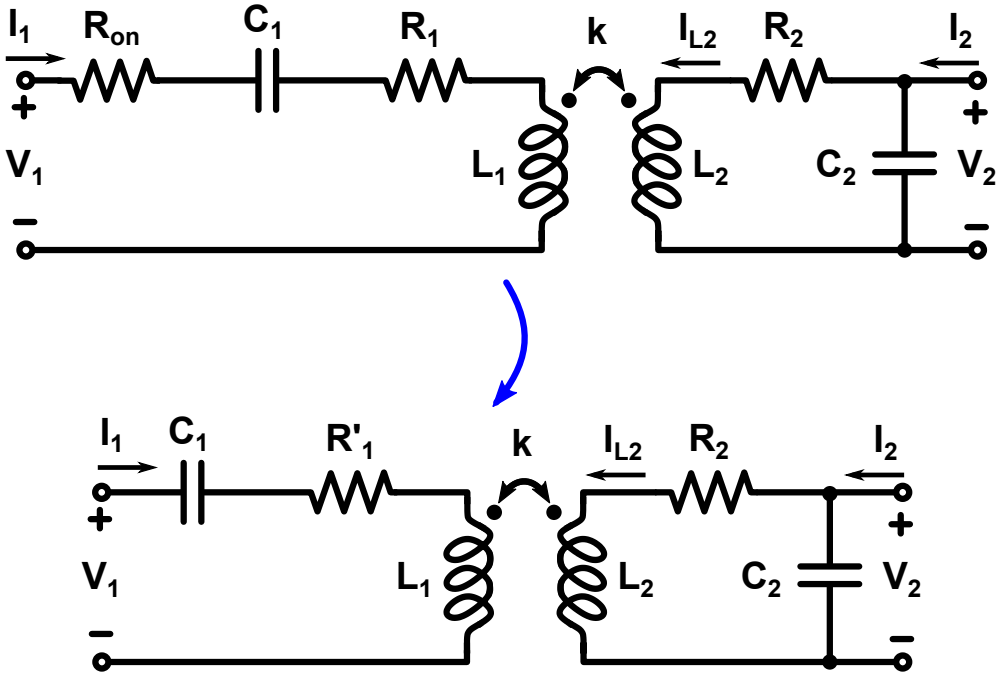


FIGURE 6.9: The inverter can be seen as an equivalent Thevenin voltage source with output impedance $R_{on}$, with an input capacitance $C_{in}$.

find a minimum $R_{on}$ achievable; by expressing $C_2$ as

$$C_2 = C_{in,MAX} = \frac{1}{(\omega_0 A_v k)^2 L_1} \left(\frac{1+\varepsilon}{\varepsilon}\right)^2 \tag{6.24}$$

it is possible to find the minimum $R_{on}$ when $C_{in} = C_{in,MAX}$

$$R_{on,min} = \tau L_1 \omega_0^2 A_v^2 k^2 \left(\frac{1+\varepsilon}{\varepsilon}\right)^2 \tag{6.25}$$

where $\tau = C_{in} R_{on}$ is a technological figure of merit that relates the input capacitance to the output resistance of the inverter. More scaled technologies tend to have lower $\tau$. We can now plug (6.25) into (6.23) thus removing the dependence from $R_{on}$. At this point, once $\omega_0$, $A_v$, $Q_1$, $k$, and a target phase noise $\mathcal{L}(\Delta\omega)$ are set, (6.25) together with (6.23) immediately returns an optimum $\varepsilon$ which, in turn, determines a minimum phase noise degradation. To fix the ideas, for an oscillator at 10 GHz with $Q_1 = 16$, $k = 0.2$ and $A_v = 1.2$ we have a minimum degradation of 11.6 dB, 3 dB higher than in the case without the inverter parasitics. Ideally, to limit the degradation, the designer should select the lowest feasible coupling factor and voltage gain required to maintain the oscillation.

The foregoing analysis can be easily extended to the schematic in Fig. 6.4. Since

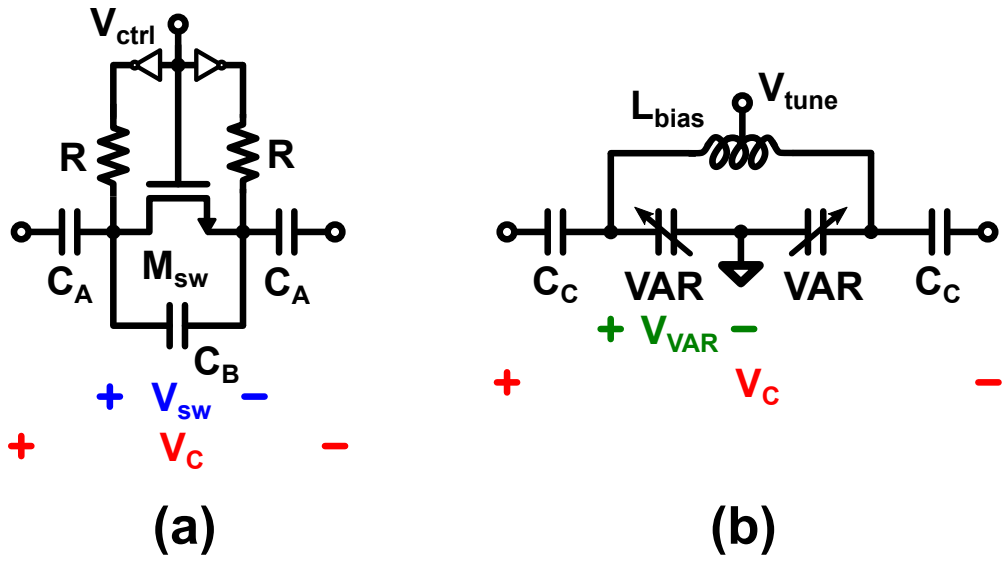


FIGURE 6.10: Transistor level schematic of the (a) switched capacitors; (b) varactor.

there are now two switches in series at any given moment, the resulting $R_{on}$ is doubled. At the same time, the actives can be twice as wide, as the differential capacitance seen by $L_2$ is $C_{in}/2$, thus compensating for the doubling of $R_{on}$.

## 6.3 Design of the Transformer-Based Series VCO

The design flow starts from selecting a target phase noise, for this project $\Delta\mathcal{L}(2\pi \cdot 1\,MHz) = -133\,\text{dBc/Hz}$ is selected. The target coupling factor is set at $k = 0.1$, together with a target $Q_1 = 14$. The voltage gain of the feedback network is set to $A_v = 2$. For an operating frequency of $\omega_0 = 2\pi \cdot 10\,\text{GHz}$ and a supply of $V_{DD} = 0.8\,\text{V}$, the resulting feedback network parameters are $L_1 = 210\,\text{pH}$, $L_2 = 120\,\text{pH}$, $C_1 = 1.2\,\text{pF}$, $C_2 = 2.1\,\text{pF}$ with a $Q_2 = 5.6$. The actives dimensions are limited by $C_{in} \leq 2C_2$, leaving us with a pMOS $(W/L)$ of $(2.23\,mm/18\,nm)$ and an nMOS dimension of $(1.8\,mm/18\,nm)$. An additional $C_{fix} = 180\,\text{fF}$ is added to the inverter inputs to tune the resonant network at exactly 10 GHz. The bias resistors $R_f$ are set to $1\,\text{k}\Omega$.

The continuous tuning between 9.5 to 10.5 GHz is achieved by subdividing the tank into seven identical switched capacitor cells (Fig. 6.10(a)), and a single varactor cell(Fig. 6.10(b)). The capacitive cells are designed to withstand a differential voltage swing $V_C \approx 8\,\text{V}$. The most critical components are the MOS switch $\text{M}_{\text{sw}}$ and the varactors VAR, as they are rated for just 1.8 V. When the switch is open, it behaves like a capacitance $C_B$ in series to the explicit capacitances $C_A$; the voltage across $\text{M}_{\text{sw}}$ is then given by the capacitive divider $C_A - C_B$. The higher is $V_C$, the bigger

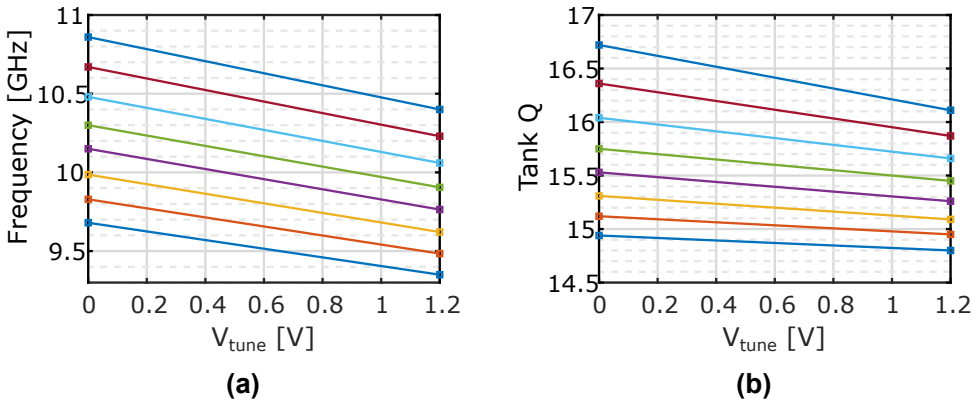


FIGURE 6.11: Simulated tank resonant frequency (a) and quality factor $Q_1$ (b).

$C_B$ must be to avoid damage to the switch. On the one hand, increasing $C_B$ reduces the cell on-off capacitance ratio, which negatively impacts the tuning range; on the other hand, the switches can be made quite large so that $C_B$ is completely absorbed by their parasitic capacitance, thus improving the quality factor of the cells. Two inverters connected with large resistances $R$ to the floating source and drain of $M_{sw}$ provide the DC bias to keep the switch on/off. The signal $V_{ctrl}$ switches the cell off or on by changing between 0 and 1.2 V.

In the case of the varactor cell, the addition of the capacitive divider also require the introduction of $L_{bias}$ to set a DC value to the otherwise floating node between the varactor and $C_C$, as sketched in Fig. 6.10(b). The varactors are realised with thick oxide n-type accumulation varactors. The control voltage $V_{tune}$ can vary between 0 and 1.2 V.

Since $Q_2$ is relatively low and the target tuning rage is small ($\approx$ 10%), no tuning of the secondary capacitance is required.

Lastly, a cascade of inverters implement the output buffer that feeds the signal to the GSG pads for the prototypes characterisation.

## 6.4 Simulation Results

Here are reported the post-layout simulated performance of the VCO. The resonant frequency and quality factor of the primary resonator are reported in Fig. 6.11. The secondary inductor is left open.

Next, the operating frequency of the oscillator is reported in Fig. 6.12 against the varactor tuning voltage $V_{tune}$. The VCO is to continuously cover the 9.67-10.63 GHz range, for a tuning range of 9.5%.

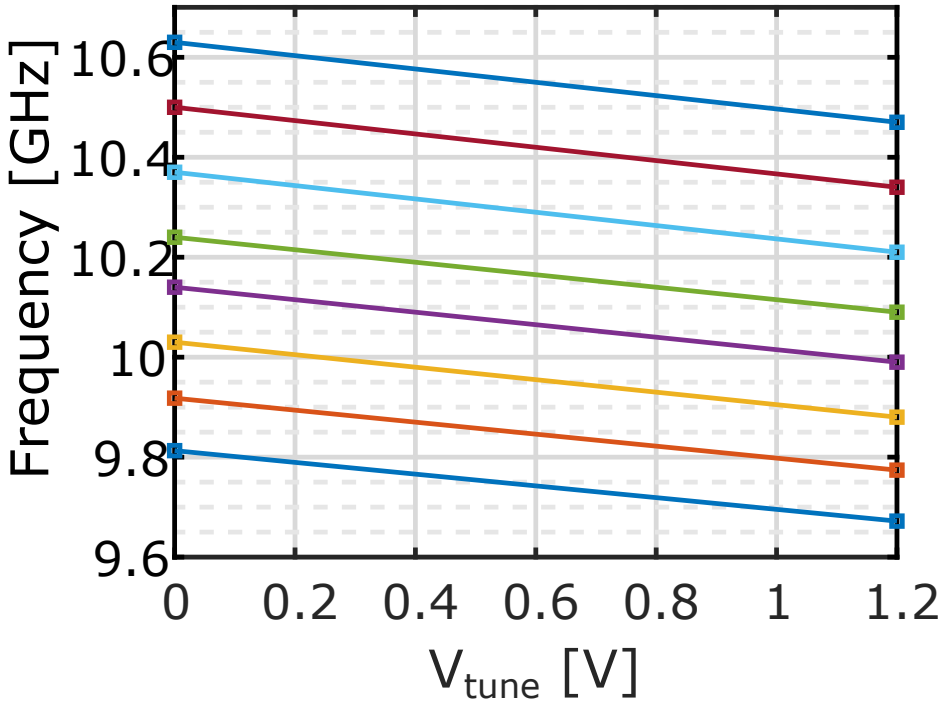


FIGURE 6.12: Simulated VCO tuning range.

The phase noise performance for three different offsets is plotted against the operating frequency in Fig. 6.13. The lowest phase noise of -136 dBc/Hz at 1 MHz offset is simulated at 10 GHz. The phase noise at lower offsets sees an increase of flicker noise injection above 10 GHz. The VCO draws 0.33 W from a 0.8 V supply.

The figure-of-merit of the series VCO calculated at 1 MHz offset is reported next, in Fig. 6.14, varying between -189 and -191 dBc/Hz.

## 6.5 Measurement Result and Discussion

The prototypes are realised in a 22 nm FD-SOI CMOS process; the nominal supply voltage is 0.8 V. The digital control bits operating the switched capacitor banks operate at 1.6 V. The active area is 300 $\mu m \times 100\,\mu m$.

During the characterisation phase, it became evident that the VCO was not operating as expected. The DC power draw is much higher than anticipated (around 0.5 W) and the VCO fails to operate for the upper portion of the tuning range. The phase nose measured is also much higher than expected. After some debugging, it was determined that the oscillation amplitude at the inverter output is about 20 times lower than what expected, around 40 mV.

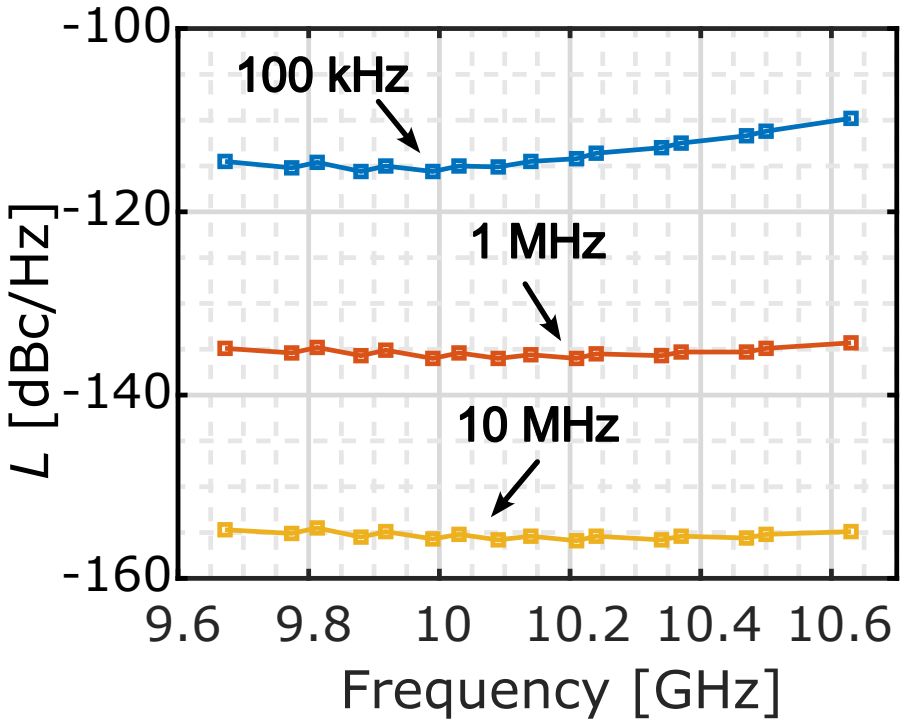


FIGURE 6.13: Simulated VCO phase noise performance vs. frequency, at three different offsets.

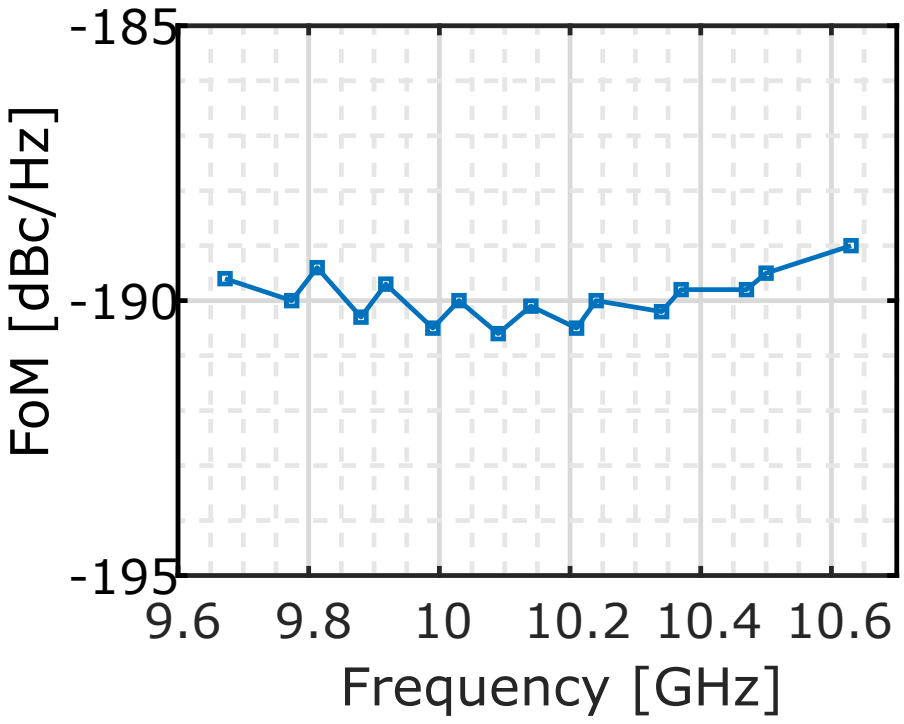


FIGURE 6.14: Simulated VCO FoM vs. frequency.

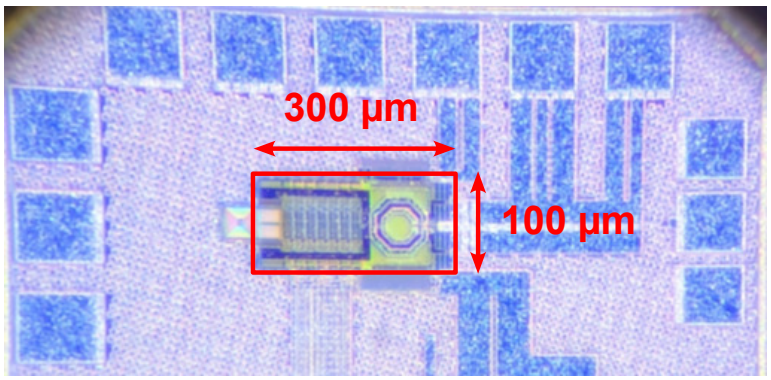


FIGURE 6.15: Chip microphotograph.

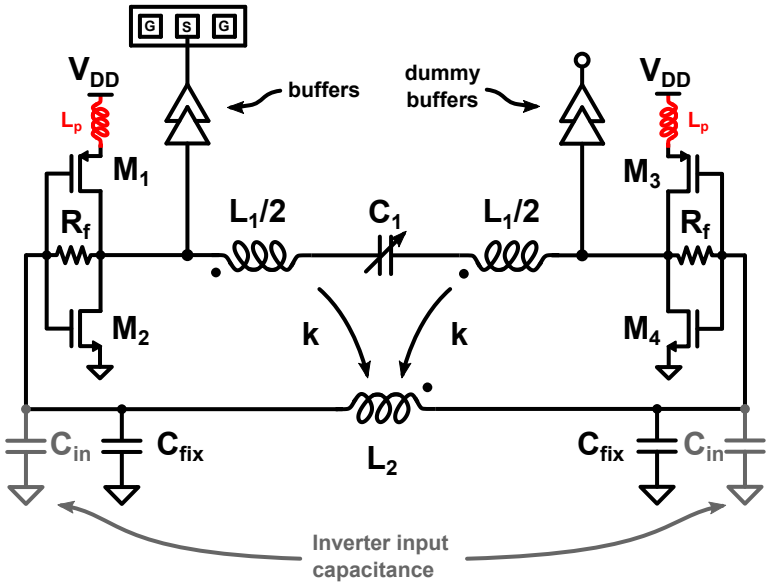


FIGURE 6.16: Presence of a higher-than-expected parasitic inductance on the supply path in the real oscillator.

The most probable cause, even if the layout was thoroughly characterised with the help EM simulations, is the presence of a higher-than-expected parasitic inductance on the supply path, denoted as $L_p$ in Fig. 6.16. The pseudo-differential nature of the structure makes it more sensitive to any supply non-idealities.

A novel transformer-based series VCO was presented. The proposed feedback network saves valuable silicon area when compared to multi-core implementations or series ring oscillators, without compromising the benefits of the series VCO. A thorough analysis of the impact of the feedback network on the phase noise is carried out, finding an simple and elegant optimisation strategy. Even without a working prototype, we remain confident that this topology is worth pursuing in an effort to break free from the phase noise limitations imposed by ultra-scaled technologies.

# Chapter 7

# Stacked VCO

In this Chapter, transistor stacking is introduced in the design of a class-C VCO to enable the use of a supply voltage which is twice the nominal one, while still using thin-oxide core devices. Doubling the supply voltage doubles the maximum attainable amplitude of oscillation, hence reducing the phase noise. The supply voltage limitation could be circumvented by using thick oxide MOSFETs in the cross-coupled differential pair, but this would lead to larger parasitics, resulting in a reduced tuning range, and lower maximum operating frequency [86]. Prototypes implemented in a 22 nm FD-SOI CMOS technology achieve a phase noise of -126 dBc/Hz at 1 MHz offset from the 5.2 GHz carrier, while featuring a 16.6% tuning range.

## 7.1 Analysis and Design of the Stacked Class-C VCO

The schematic of the proposed stacked class-C is show in Fig. 7.1. The differential negative-resistance cell is implemented by closing the positive feedback loop around a stacked transconductor, made of the combination of a common-source stage ($M_1 - M_2$) and a common-gate stage with series-shunt feedback ($M_3 - M_4$), rather than a conventional differential pair. This allows to partition the voltage swing across the tank among the common-source transistors ($M_1 - M_2$) and the common-gate transistors ($M_3 - M_4$), which, ultimately, allows for a doubled amplitude of oscillation without exceeding the voltage ratings of the devices.

### 7.1.1 Analysis of the Stacked VCO

In order to equally partition the single-ended tank voltage ($V_{D,3}$ in Fig. 7.1) between $M_1$ and $M_3$, and obtain $V_{DS,1} = V_{DS,3}$, the voltage gain of the common-gate stage with series-shunt feedback is to be set to

$$A_v(j\omega_0) = \frac{V_{D,3}}{V_{S,3}} = 2 \tag{7.1}$$

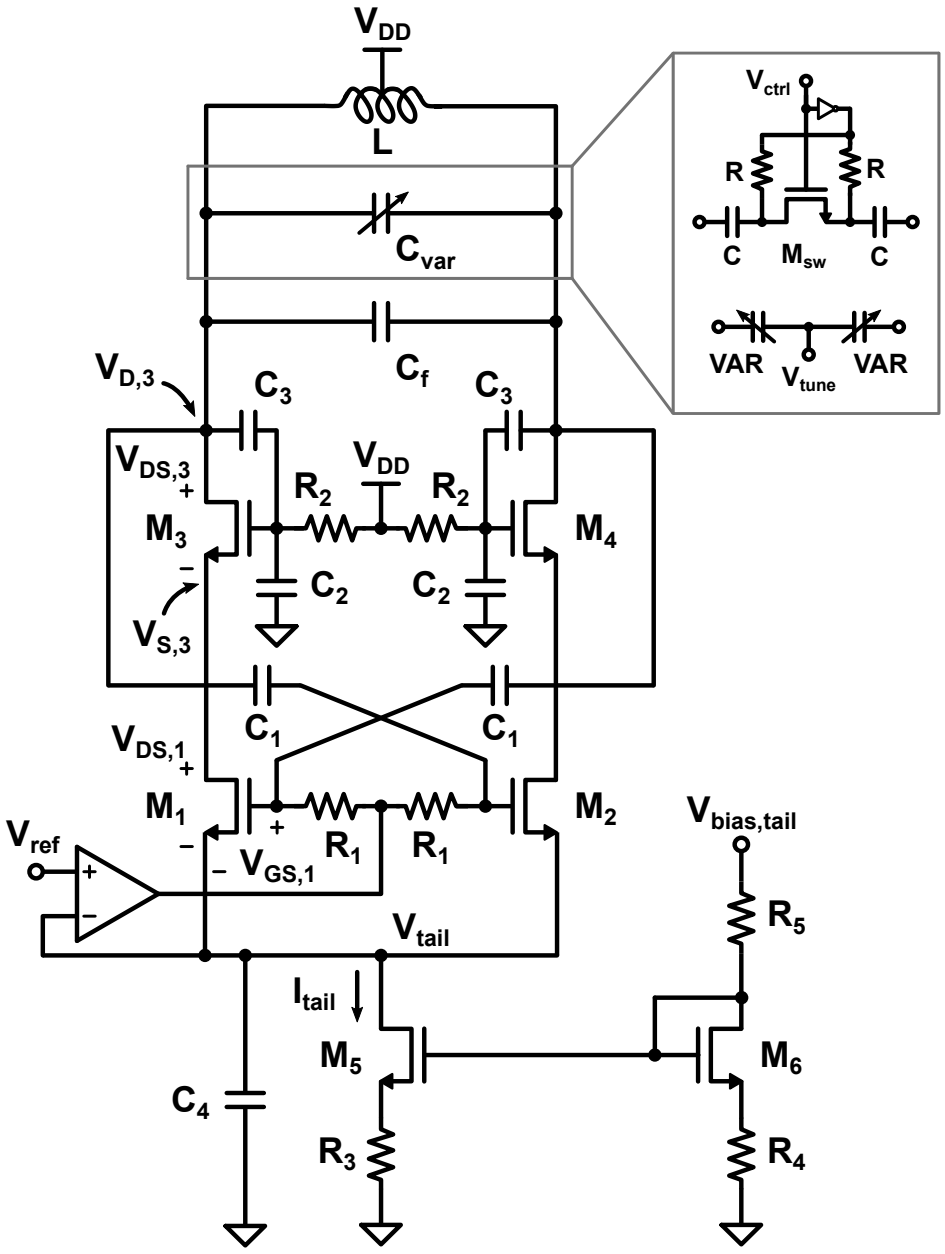


FIGURE 7.1: Transistor level schematic of the proposed class-C stacked VCO.

Moreover, the impedance looking into the source terminal of $M_3$ must be set to

$$Z_{in}(j\omega_0) = \frac{R_T}{4} \tag{7.2}$$

$R_T$ being the equivalent tank resistance at resonance. The small-signal analysis presented in [87] shows that:

$$A_v(j\omega_0) = \frac{g_{m3(4)} R_T/2}{1 + \beta\chi + \beta g_{m3(4)} R_T/2}. \tag{7.3}$$

and

$$Z_{in}(j\omega_0) = \frac{1}{g_{m3(4)}} \left(1 + \beta\chi + \beta g_{m3(4)} \frac{R_T}{2}\right) \tag{7.4}$$

where $\chi = C_{GS3(4)}/C_3$, $\beta = C_3/(C_3 + C_2)$ is the feedback factor of the series-shunt feedback around the common-gate stage, $C_{GS3(4)}$ is the gate-source capacitance of $M_{3(4)}$, and $g_{m3(4)}$ is the transconductance of $M_{3(4)}$. The capacitance $C_3$ is the parallel combination of an explicit capacitance and the gate-drain capacitance of $M_{3(4)}$. The design constraints (7.1) and (7.2), applied to (7.3) and (7.4), result in constraints on the feedback factor $\beta$ and the parameter $\chi$, from which the sizing of $C_2$-$C_3$ follows. While (7.1)-(7.4) are derived using a small-signal analysis, the oscillator actually operates at large-signal, such that the design needs to be refined based on circuit simulations. In this design, the capacitors values are eventually set as $C_2 = 1\,\text{pF}$ and $C_3 = 130\,\text{fF}$.

The simulated drain-source voltages of the common-source stage and common-gate stage ($V_{DS,1}$ and $V_{DS,3}$, respectively) are shown in Fig. 7.2 on the left. The amplitudes of the two drain-source voltages are almost equal, as required by the design.

In Fig. 7.2, the single-ended tank voltage, $V_{D,3}$, is also reported on the right. Its peak-to-peak amplitude is larger than 2 V. If we directly fed back this signal to the gate of $M_{1(2)}$, we would exceed the voltage ratings of the devices. Consequently, $C_1$ in Fig. 7.1 is sized to be roughly equal to the gate-source capacitance of $M_{1(2)}$, $C_1 = 240\,\text{fF}$, such that an attenuation by a factor 2 is introduced due to the capacitive voltage divider. Such an attenuation has a negative impact on the phase noise performance, since it increases the noise contribution of $M_{1(2)}$, as we will see promptly.

Ideally, doubling the voltage supply and, therefore, the oscillation amplitude, would improve the phase noise of the stacked class-C oscillator by 6 dB compared to a conventional implementation. This is highlighted by Leeson's equation

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left[\frac{k_B T F R_T}{n^2 V^2}\left(\frac{\omega_0}{Q\Delta\omega}\right)^2\right] \tag{7.5}$$

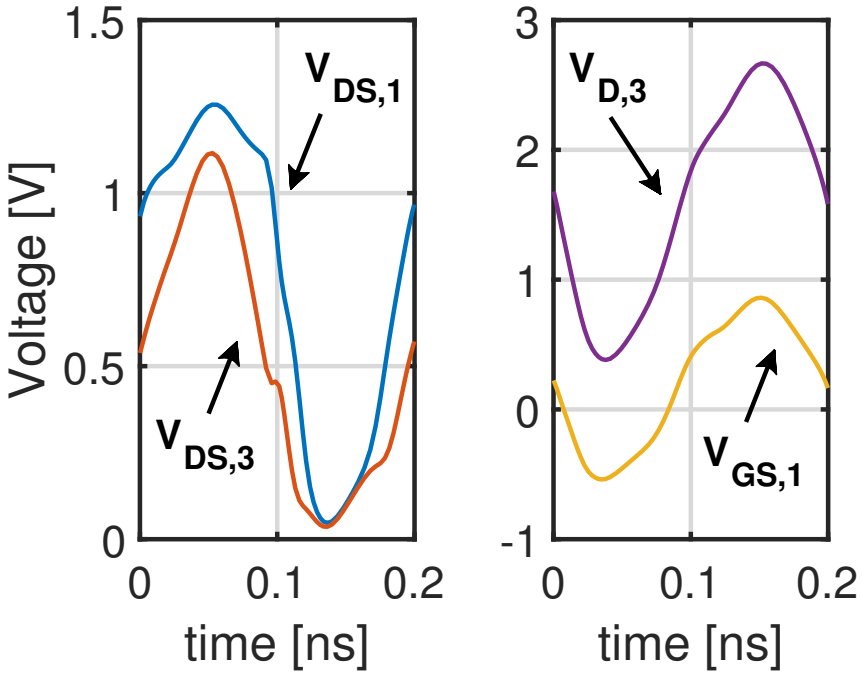


FIGURE 7.2: Simulated voltage waveforms. $V_{DS,1}$ (blue curve) is the drain-source voltage of $M_1$, $V_{DS,3}$ (orange curve) is the drain-source voltage of $M_3$, $V_{GS,1}$ (yellow curve) is the gate-source voltage of $M_1$,

where $V$ is the oscillation amplitude of the conventional oscillator, $n = 2$ is the increase of the oscillation amplitude in the stacked oscillator, $Q$ is the tank quality factor, and $F$ is the excess noise factor. Neglecting the contribution of the tail current source, the excess noise factor of a conventional class-C (or, to that regard, a class-B) oscillator is [60, 88]

$$F_c = 1 + \gamma \tag{7.6}$$

where $\gamma$ is the transistor's excess noise factor. The attenuation between the tank voltage and the gate voltage of $M_{1(2)}$ by a factor $n$, needed in the stacked oscillator, increases $F$, as discussed in [60, 88] to

$$F_{st} = 1 + n\gamma \tag{7.7}$$

Notice that in (7.7) the noise contribution of $M_3$-$M_4$ is neglected, as it is heavily attenuated by the degeneration introduced by $M_1$-$M_2$. From (7.5)-(7.7) the phase noise improvement in the stacked oscillator with respect to a conventional implementation is

$$\Delta\mathcal{L} \leq 10\log_{10}\left(n^2\frac{1+\gamma}{1+n\gamma}\right) \tag{7.8}$$

The increase in the amplitude of oscillation is partially compensated by an increase in the relative noise contribution of the pair $M_1$-$M_2$ with respect to the tank losses.

For $n = 2$ and $\gamma = 1$, (7.8) evaluates to $\Delta\mathcal{L} = 4.3\,\text{dB}$, which is, nevertheless, a significant improvement with respect to a conventional oscillator.

### 7.1.2 Design of the Stacked VCO

The stacked class-C oscillator is realized with a $L = 475\,\text{pH}$ tank inductor, implemented as a double-turn coil by exploiting both the thickest metal layer of the metal stack and the top aluminium layer in parallel. EM simulations show an inductor quality factor $Q = 14$ at 5 GHz.

The capacitive part of the tank is split in three parts: a 3-bit capacitive bank, that provides coarse tuning, a varactor, responsible for the fine tuning, and a fixed capacitance $C_f = 330\,\text{fF}$ (Fig. 7.1). The coarse tuning is made of a 3-bit binary-weighted capacitive bank, realized with 7 identical capacitive unit-cells. Each unit cell introduces a capacitance variation of 100 fF. To ensure reliable operation of the switches of the capacitor bank, thick-oxide devices with 100 nm channel length are used. This results in larger capacitive parasitics and a small decrease of the tuning range of the oscillator. An accumulation-mode varactor provides a 150 fF capacitance variation, allowing for continuos frequency tuning. The varactor's capacitance variation is larger than the one introduced by the unit-cell of the coarse tuning capacitor bank to ensure overlap between adjacent frequency sub-bands.

The tail capacitance $C_4 = 3.4\,\text{pF}$ (Fig. 7.1) ensures class-C operation [60]. Small degeneration resistances $R_3$-$R_4$ are introduced in the tail current source to reduce the the flicker noise contribution of $M_5$-$M_6$. Transistors $M_5$-$M_6$ are biased with a small overdrive voltage ($V_{\text{ov},5(6)} \approx 110\,\text{mV}$) to maximize the oscillation amplitude while keeping $M_5$-$M_6$ in the saturation region.

### 7.1.3 Design of the Dynamic Bias Loop

The proposed stacked class-C oscillator is biased by a feedback loop [68, 89], based on a operational transconductance amplifier (OTA), as shown in Fig. 7.1. The schematic of the OTA is shown in Fig. 7.3. The OTA is realised with core MOSFETs and uses cascode transistors to be able to operate under the same supply voltage as the oscillator. The OTA is made of a cascade of a common-drain stage ($M_{13}$-$M_{14}$), that acts as a level shifter, followed by a conventional single-stage OTA loaded by a cascode current mirror. The tail generator is also a cascode current mirror. All MOSFETs are thin-oxide devices.

In class-C oscillators, the noise of the OTA in the dynamic bias loop can become a dominant contributor to the oscillator phase noise at lower frequency offsets, if not treated properly [68]. To avoid such a scenario, in this design the bandwidth of

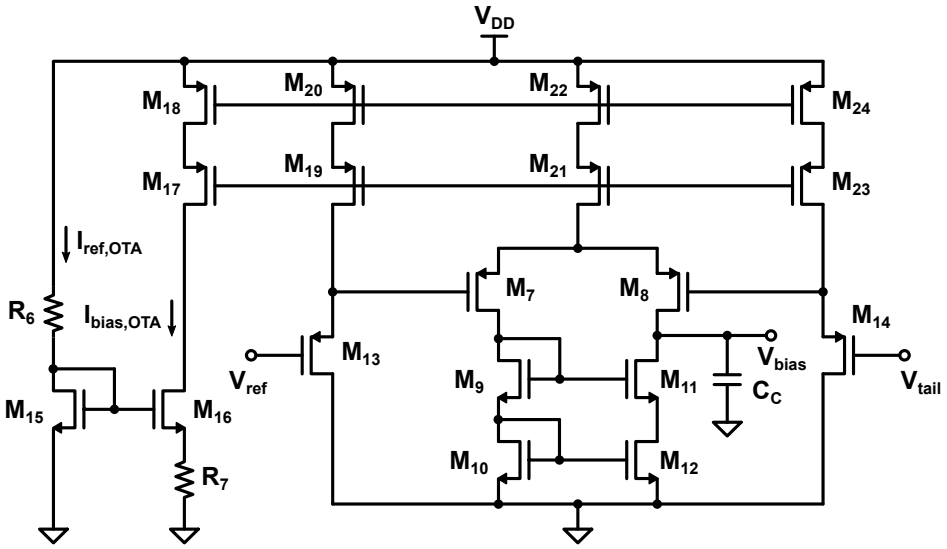


FIGURE 7.3: Transistor level schematic of bias OTA.

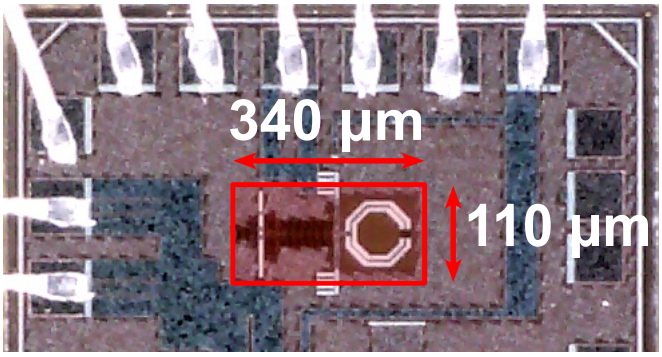


FIGURE 7.4: Chip microphotograph.

the OTA is limited to be at around 1.8 kHz by using an ultra-low biasing current of $I_{bias,OTA} = 18\,\text{nA}$ (which sets all OTA transistors in the sub-threshold region) and a $C_C = 13\,\text{pF}$ load capacitance. Additionally, all OTA transistors have a $L = 400\,\text{nm}$ channel length to further reduce their flicker noise contribution. The generation of $I_{bias,OTA}$ is accomplished using a Widlar current reference ($M_{15}$-$M_{16}$ and $R_6$-$R_7$ in Fig. 7.3).

## 7.2 Measurement Results and Final Remarks

Proof-of-concept prototypes of the proposed class-C stacked VCO are realized in a 22 nm FD-SOI CMOS technology. The chip microphotograph is shown in Fig. 7.4. The core area is $340\,\mu m \times 110\,\mu m$. The supply voltage is set 1.6 V, twice as large as the nominal 0.8 V supply voltage of the thin-oxide core devices of the used technology.

The phase noise of the VCO was measured using the delay line method described in [90], by setting up an ad hoc measurement bench. The VCO signal and

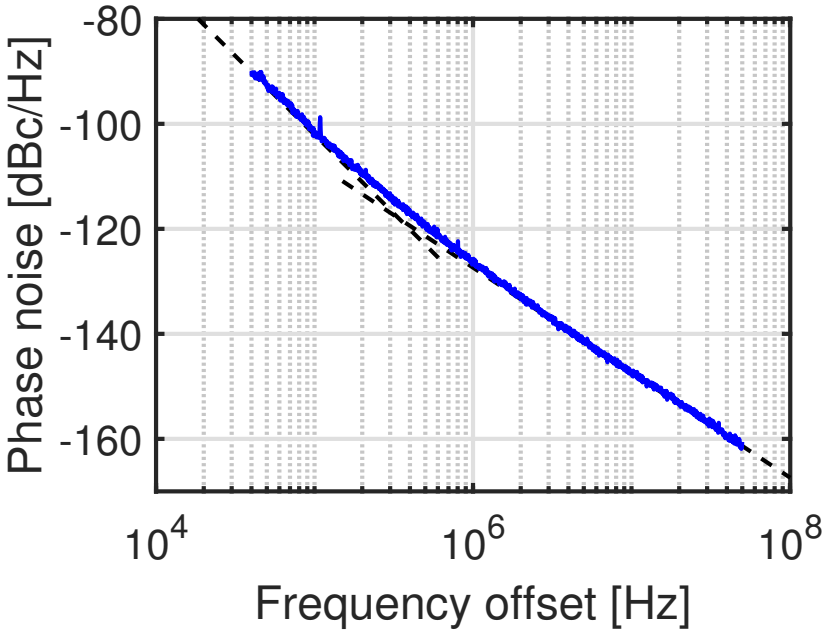


FIGURE 7.5: Measured phase noise for $I_{tail} = 21\,mA$ with the VCO operating at 5.2 GHz. The dashed lines represent the -30 and -20 dB/dec asymptotes.

its delayed version are fed to a mixer which acts as a phase/frequency detector. The demodulated signal at the mixer output is measured by means of a spectrum analyzer. The phase noise is then obtained processing the measured signal as described in [90].

The measured phase noise at 1 MHz offset from the 5.2 GHz carrier is -126 dBc/Hz. The oscillator bias current is set to $I_{tail} = 21$ mA; the OTA reference voltage $V_{ref}$ (Fig. 7.1) is set to $V_{ref} = 0.25$ V. The measured phase noise sideband reported in Fig. 7.5 clearly shows the flicker and white noise regions. The measured $1/f^3$ phase noise corner frequency is just over 300 kHz.

The phase noise performance of the VCO as a function of the bias current is shown in Fig. 7.6 for three different frequency offsets. The operating frequency is 5.2 GHz. The phase noise decreases with increasing bias current, reaching the lowest value for $I_{tail} = 21$ mA.

The measured phase noise across the tuning range is reported in Fig. 7.7 showing little variation across the frequency operating range of the proposed oscillator.

Figure 7.8 reports the measured oscillation frequency as a function of the continuous tuning control voltage $V_{\text{tune}}$ for all the 8 sub-bands of the switched-capacitor coarse tuning. The measured oscillation frequency spans from 4.39 GHz to 5.2 GHz with a considerable overlap between adjacent bands. The resulting tuning range is 16.6%.

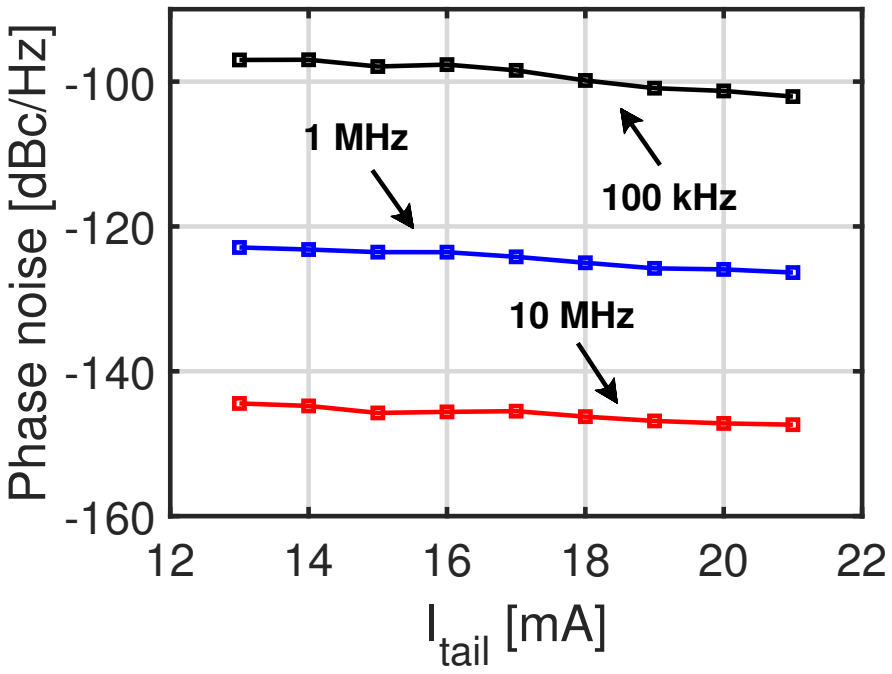


FIGURE 7.6: Phase noise of the class-C VCO at three frequency offsets operating at 5.2 GHz for different values of $I_{tail}$.

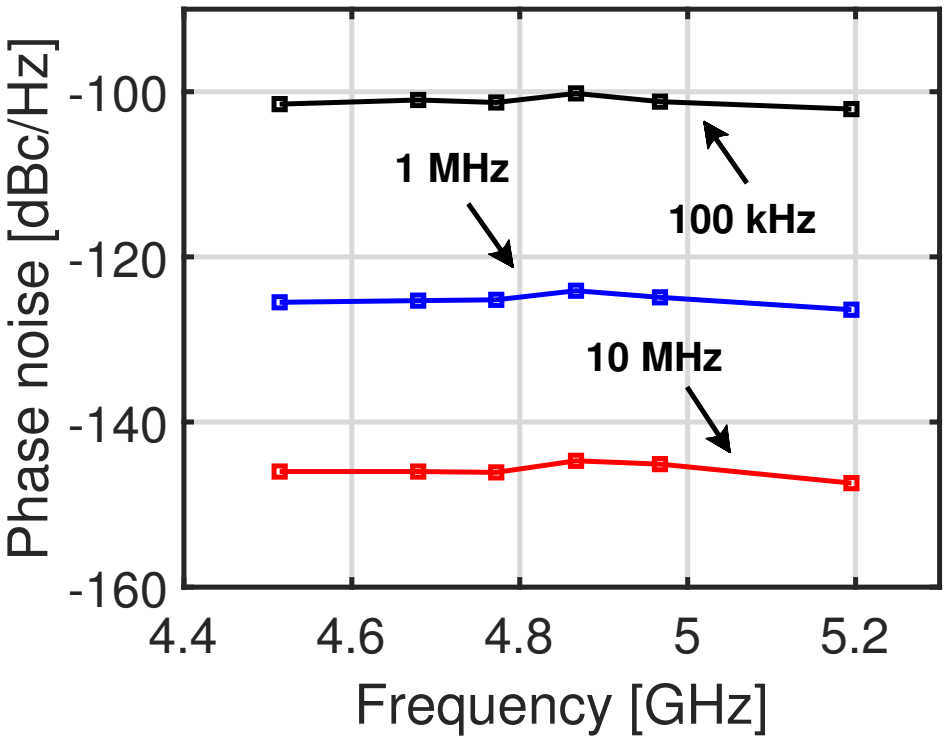


FIGURE 7.7: Phase noise of the class-C VCO at three frequency offsets across the tuning range.

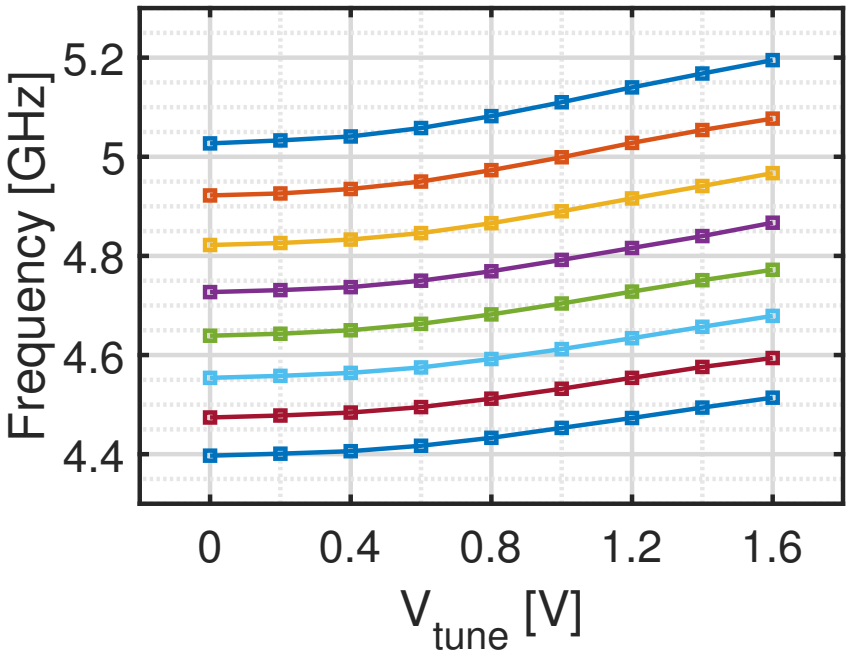


FIGURE 7.8: Measured tuning range of the VCO. The operating frequency spans from 4.39 GHz to 5.2 GHz.

The measured figure-of-merit (FoM) is -185.4 dBc/Hz, a value that is probably due to a suboptimal layout of the circuit, rather than to inherent limitations of the stacked topology.

The VCO performance is compared with the state-of-the-art in Tab. 7.1. The proposed stacked class-C oscillator shows a very good phase noise performance thanks to the higher supply voltage allowed by the employed stacked circuit topology.

The use of a stacked transconductor in the negative-resistance cell of a class-C oscillator is proposed as a means to increase the amplitude of oscillation, and consequently decrease the phase noise, without compromising the reliability of the circuit.

Prototypes of the proposed VCO, realised in a 22 nm FD-SOI technology, operate under a 1.6 V supply voltage (twice as large as the nominal one) showing a measured phase noise of -126 dB at 1 MHz offset from the 5.2 GHz carrier, while consuming 33.8 mW.

TABLE 7.1: Performance summary and comparison with the state-of-the-art.

| | **This work** | [91] | [92] | [93] | [94] | [86] |
|---|---|---|---|---|---|---|
| CMOS technology [nm] | **22 FD-SOI** | 65 | 65 | 40 | 22 FD-SOI | 65 |
| $V_{DD}$ [V] | **1.6** | 1 | 1.2 | 1 | 0.9 | 1 |
| Power [mW] | **33.8** | 5 | 0.72 | 16 | 5.98 | 5.3 |
| Frequency [GHz] | **5.2** | 8 | 3.6 | 3.37 | 9 | 7.92 |
| Tuning range [%] | **16.6** | 32.9 | 18.2 | 55.5 | 39 | 22.9 |
| PN @100kHz [dBc/Hz] | **-102** | -98.2 | -94[a] | -103 | -89 | -88 |
| PN @1MHz [dBc/Hz] | **-126.4** | -121.7 | -114 | -127 | -110 | -115 |
| Eq. PN @100kHz ref. to 5.2 GHz [dBc/Hz] | **-102** | -102 | -90 | -98 | -93.3 | -91 |
| Eq. PN @1MHz ref. to 5.2 GHz [dBc/Hz] | **-126.4** | -125.4 | -110 | -123 | -114.3 | -118 |
| FoM [dBc/Hz] | **-185.4** | -192 | -186 | -188 | -181 | -186 |
| Core area [$mm^2$] | **0.037** | 0.126 | 0.08 | 0.12 | 0.01 | 0.116 |

[a] Graphically estimated

# Conclusions

This thesis covers the two main topics explored during the Ph.D.: the design of low-power IoT transmitters and the design of low noise integrated oscillators. The octacore DCO was done in collaboration with Infineon Villach; the rest of the work was done at the ICARUS research Group in the University of Padova.

During the design of the low-power IoT radio, the analysis of the passive resistive mixer results in a simple LTI model capable of accurately predicting its gain and bandwidth while taking into account the baseband source output resistance, the switch on/off resistances and the load impedance. The analysis also shows that the passive resistive mixer acts as a upconverter first, followed by a first order RC filter, whose bandwidth depends on the baseband source resistance and load impedance, requiring a more complex and power hungry baseband circuitry that would impair the efficiency of a low-power transmitter. The passive reactive mixer is introduced as an alternative to the common resistive mixer: the rigorous analysis demonstrates that it acts as a filter first followed by an upconverter. The passive reactive mixer is leveraged to simplify the baseband circuitry, thus cutting its power consumption and increasing the TX efficiency. Its feasibility is tested by designing a testbench IoT radio operating in the 2.4 GHz range with a reactive mixer based Cartesian modulator. The prototypes are realised in a 22 nm FD-SOI CMOS technology and show a 22% system efficiency when transmitting a 16-QAM signal at 2.4 Mbaud at 2.7 dBm.

The research carried out on low phase noise oscillator led to the realisation of three different proof-of-concept oscillators. In the multi-core design, a lot of effort was devoted to designing a robust reconfigurable coupling for an array of eight oscillators. The addition of switches allows the coupling network to operate the array in 2,4,6, and 8-core configuration, trading phase noise for power consumption. The addition of switches in the coupling network introduces a strongly time-varying impedance: the analysis resulted in a simple LTI model of the switch, demonstrating how its equivalent resistance can impact the phase noise of the array. The prototypes show a phase noise of -126 dBc/Hz at 1 MHz offset at 10.7 GHz, with a FoM of -184 dBc/Hz and a tuning range of 27%. While unsuccessful, the design of the series VCO resulted in a thorough analysis of the proposed feedback network, along with useful design considerations for future iterations. The series VCO promises much lower phase noise than the parallel counterpart, but it also comes with its own set of

challenges. Nonetheless, this project was a great learning experience in the design of a high performance oscillator. The last work, done in collaboration with Andrea Gobbo and Agata Iesurum at the ICARUS Group, presents a 5 GHz stacked VCO capable of operating from a 1.6 V supply, double of technological maximum limit. The stacked topology equally splits the oscillation amplitude between the MOSFETs, thus avoiding any reliability concerns. As a result of the increased oscillation amplitude, the phase noise is improved. The prototypes are realised in a 22 nm FD-SOI process and achieve a phase noise of -126 dBc/Hz at 1 MHz offset from the 5.2 GHz carrier, with a FoM of -185 dBc/Hz, and a tuning range of 16.6%.

The presented work led to the publication of three conference articles [81, 95, 96], and one journal [97]. Additionally, a letter [98] and a journal [99] have been submitted, and are currently under review.

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