IEEE Open Journal of
Power Electronics

Received 31 July 2024; revised 3 September 2024; accepted 13 September 2024. Date of publication 16 September 2024; date of current version 26 September 2024. The review of this article was arranged by Associate Editor Yam Siwakoti.

Digital Object Identifier 10.1109/OJPEL.2024.3462773

Single-Stage Non-Isolated Multiport Y-Converter for Interlinking 400 V DC Microgrids With the Three-Phase AC Grid

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This work was supported by European Union's Horizon Europe Research and Innovation Programme through Project "iPLUG" under Grant 101069770.

ABSTRACT The integration of dc microgrids (MGs) into distribution networks offers a promising solution to address the growing demand for electric energy by facilitating the incorporation of renewable energy sources and energy storage systems. To ensure sustained and reliable operation, dc MGs are commonly linked to utility grids through interlinking converters. However, with the increasing adoption of small-scale dc MGs for residential and commercial applications, the traditional approach of using a dedicated converter for each MG can significantly increase system size and cost. This paper proposes a single-stage non-isolated multiport converter (MPC) to interface the three-phase ac grid with 400 V dc MGs. The MPC enables direct power sharing between dc MGs, minimizes the dependence on the ac grid, and enhances the efficiency and power density of the power electronic interface compared to using multiple two-port converters. The motivations for the proposed converter include its single-stage power conversion among different ports, potentially leading to enhanced efficiency and power density. Furthermore, the absence of bulky intermediate dc-link capacitors and transformers in the proposed topology contributes to improved power density and reduced costs. Although designed for 400 V dc MGs in this study, the proposed MPC boasts buck-boost capability and bidirectional power flow at all ports, independent of the dc ports' voltage, providing the flexibility to directly interface with a wide range of dc systems. The performance of the converter is assessed through experimental tests under various operating conditions.

INDEX TERMS AC-DC power conversion, Multiport converters, Single-stage converters, Three-phase modular converters, Three-phase bidirectional rectifiers.

I. INTRODUCTION

The increasing adoption of renewable energy sources (RESs), energy storage systems (ESSs), and electric vehicle charging stations necessitates traditional power systems to accommodate larger capacities and loads. In response, dc microgrids (MGs) are emerging as a viable solution for effectively integrating distributed energy sources and storage systems into existing power systems while meeting local demand [1], [2]. Several studies have investigated the optimal voltage level selection for low-voltage dc MGs [3], [4], [5]. The findings of these studies have identified 400 V dc voltage level as the preferred choice for residential and commercial applications, attributed to its superior overall system efficiency and the need for fewer power conversion stages when connecting multiple energy sources and loads. To ensure sustained and reliable operation, dc MGs are often interconnected with utility grids through a bidirectional power converter called interlinking converter (ILC). This converter enables the power exchange between the dc MGs and the utility grid, helping maintain the power balance within the dc MGs.

Both isolated and non-isolated converters have been explored in the literature for interfacing the ac grid with the dc MG [6], [7]. To enhance the efficiency and power density of the power electronic interface, non-isolated converters are preferred [8], particularly since galvanic isolation is not mandatory according to relevant standards [9], [10].

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A. TWO-PORT INTERLINKING CONVERTERS

When integrating 400 V dc MG with the European low-voltage (LV) three-phase ac grid, which operates at a line-to-line voltage of 400 V_{rms}, buck-type three-phase converters are commonly employed to establish a single-stage power interface [11]. Several optimized buck-type converters have been proposed in the literature to serve as ILCs, including current source converters (CSCs) in both six-switch and seven-switch configurations [12], [13]. The bidirectional power flow capability for the CSCs can be attained through an inverting link [14]. Additionally, other notable options include the Swiss converter [15], the integrated active filter converter [16], and the Y-converter [17], [18]. Previous studies demonstrated that the Y-converter potentially achieves superior overall performance among buck-type converters [19], [20], [21].

Besides the single-stage buck-type converter, two-stage converters can offer an alternative for interfacing 400 V dc MGs with the LV ac grid [22]. In these two-stage converters, a cascaded connection of either two-level or three-level voltage source converters (VSCs) and a dc-dc step-down converter is employed. While VSCs are renowned for their simple structure, control, and high power density, the two-stage solution is less favorable, as the inclusion of an extra power conversion stage and the necessity for intermediate dc-link capacitors result in a degradation of the overall efficiency and power density of the ILC [20], [23].

B. MULTIPORT INERLINKING CONVERTERS: MOTIVATIONS AND STRUCTURES

The rising popularity of dc MGs in residential and commercial settings, as discussed in [24], has prompted a reassessment of conventional approaches to grid interfacing. Traditionally, each MG would utilize a dedicated converter for connection to the grid [6], a practice that often leads to larger system sizes and higher costs. In response to these challenges, multiport converters (MPCs) have emerged as promising and efficient solutions [25], [26]. MPCs offer an effective approach by integrating multiple energy ports into a single hub, thereby providing a more streamlined and potentially cost-effective solution. Fig. 1 depicts the proposed concept of using a single MPC to interface the utility grid with multiple dc MGs.

MPCs offer a multifaceted solution beyond mere cost and size reduction compared to the conventional multi-converter approach. They introduce enhanced flexibility and resilience by enabling direct power exchange between various ports. When utilized to link dc MGs with the ac grid, MPCs empower dc MGs to exchange power directly through the converter, reducing dependence on the utility grid. This strategic integration opens avenues for optimizing power flow among different energy ports and maximizing the utilization and sharing of RESs and ESSs within the dc MGs, thereby improving the overall performance of the system.

In the literature, various MPCs have been proposed to establish a direct interface between three-phase ac grids and dc systems. These MPCs can be categorized into three groups

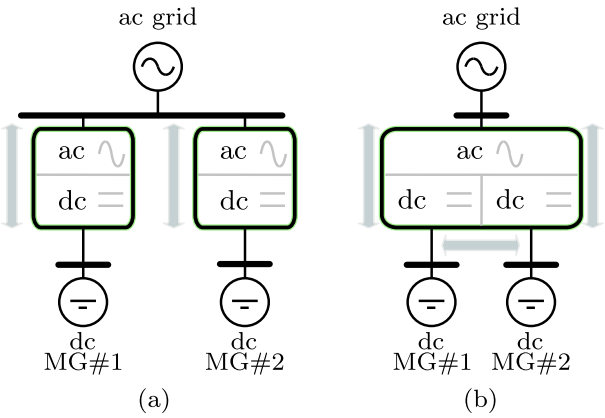

FIGURE 1. Integration of two dc MGs with the ac grid: (a) Utilizing two-port converters; (b) Utilizing a Multiport converter.

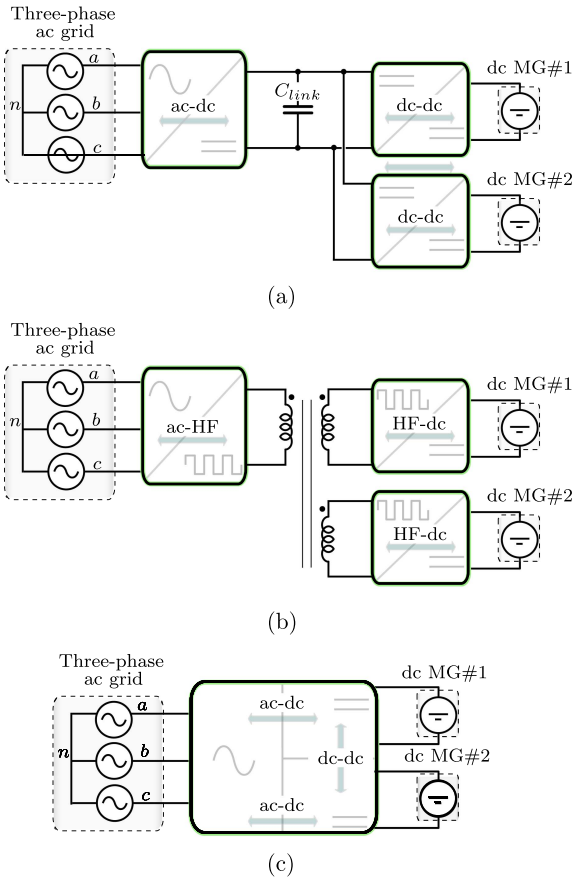

FIGURE 2. Different MPC structures for interfacing dc systems with the ac grid: (a) dc-coupled MPCs; (b) Magnetically-coupled MPCs; (c) Modified MPC structures.

based on the structure of the converter topology, as illustrated in Fig. 2: dc-link coupled MPCs, magnetically coupled MPCs, and modified MPC structures. DC-link coupled MPCs, depicted in Fig. 2(a), are formed by interconnecting conventional two-port ac-dc and dc-dc converters to a common intermediate dc-link capacitor. This approach has been widely

studied in various applications. For instance, in the field of PV generation, dc-link coupled MPCs have been explored to form a modular PV generation system based on a dc bus architecture [27]. Additionally, they have been investigated for the implementation of soft open points (SOPs) in distribution networks, where they enhance flexibility and increase the hosting capacity by integrating RESs and ESSs in multiterminal SOPs [28], [29], [30]. Furthermore, dc-link coupled MPCs have been utilized for integrating RESs and ESSs into the ac grid [31].

While dc-link coupled MPCs are utilized in various applications, they suffer from significant drawbacks. As the power flow among the ports undergoes a two-stage power conversion, the efficiency of the MPC is potentially degraded. Additionally, the reliance on a common bulky intermediate dc-link capacitor [32], as depicted in Fig. 2(a), increases the size of the MPC and may introduce reliability concerns [33]. Any failure or degradation of the capacitor can disrupt the operation of the entire converter. Moreover, dc-link voltage regulation may be critical, especially when power fluctuations occur at one of the ports, making prompt and robust control of the dc-link voltage crucial [28], [34].

Magnetically coupled MPCs, illustrated in Fig. 2(b), incorporate magnetic coupling elements such as high-frequency (HF) transformers and coupled inductors in the converter topology for the power transfer between the ports. In [35], [36], [37], partially isolated MPCs based on dual three-phase active bridges are introduced in three-port and four-port configurations. Another approach is demonstrated in [38], [39], where an MPC combines a VSC with three-phase or single-phase converters through three HF transformers. A three-phase center-tapped HF transformer is proposed in [40] to connect two VSCs. Coupled inductors are adopted in [41] to develop a three-port inverter, while in [42], a multi-winding HF transformer is utilized to couple ac and dc ports.

The incorporation of HF transformers and coupled inductors adds to the overall complexity of the converter topology, necessitating customized and optimized designs [43]. Additionally, the presence of these magnetic components increases the volume of the MPC and introduces additional power losses, leading to reduced overall efficiency and power density of the MPC.

To address the limitations of both the dc-link coupled and magnetically coupled MPCs, modified MPC structures, displayed in Fig. 2(c), have been developed. These modifications involve transforming two-port converters into MPCs without relying on dc-link capacitors or magnetic coupling. In [44], multilevel inverters are employed as multisource inverters, adopting classic multilevel inverter structures. However, these MPCs were originally proposed for multisource inverters, and therefore, bidirectional power flow control at all ports is not fully explored, with only limited operating modes considered [45]. Moreover, the power delivered to each port depends on the voltage ratio of the dc ports, limiting their applicability as multiport interlinking converters, especially for interfacing directly with 400 V dc systems [46]. Another MPC converter, based on the two-level VSC, is presented in [47], where each leg is simultaneously used as a buck-boost converter. However, this converter also presents constraints in the power flow and the output voltage operating range, preventing direct connection to 400 V dc systems.

C. PROPOSED CONVERTER

This paper introduces a single-stage non-isolated MPC, named the multiport Y-converter (Y-MPC), designed to link the three-phase ac grid with 400 V dc MGs. Building upon the Y-converter, renowned for its superior performance as a buck-type ILC [21], the proposed Y-MPC extends its capabilities into a multiport ILC, facilitating direct power exchange between dc MGs. In applications, this enhancement aims to bolster flexibility and resilience, reduce reliance on the ac grid, and optimize the utilization and sharing of RESs and ESSs within the dc MGs. The proposed converter offers several advantages, including single-stage power conversion among different ports, potentially leading to enhanced efficiency and power density. Furthermore, the absence of bulky intermediate dc-link capacitors and HF transformers in the proposed topology favors power density and reduces costs. While designed for 400 V dc MGs in this study, the proposed MPC presents buck-boost capability and bidirectional power flow at all ports, independent of the dc ports' voltage. This feature provides the flexibility to directly interface with a wide range of dc systems.

The rest of the paper is structured as follows: Section II offers a comprehensive discussion on the converter's operation, Section III includes an evaluation of the proposed converter compared to using two Y-converters to interface the MGs in terms of semiconductor losses. Section IV presents the converter's control structure and modulation techniques, and Section V showcases the experimental results at various operating conditions. Finally, Section VI reports the conclusion.

II. PROPOSED MULTIPORT Y-CONVERTER

A. DERIVATION AND OPERATION PRINCIPLE

The proposed multiport converter topology is derived from the Y-converter, as depicted in Fig. 3(a), transforming it from a two-port configuration into a multi-port structure capable of connecting multiple dc ports to a three-phase ac grid, as illustrated in Fig. 3(b). Initially, the two-port Y-converter comprised three four-switch buck-boost modules [17], [48]. Alternatively, in the proposed converter, each module is expanded into a six-switch dc-dc converter. Considering the structure of a three-port converter, the upgraded design includes a shared buck half-bridge and two boost half-bridges, establishing connections to the dc ports. Notably, the configuration is potentially adaptable to additional dc ports by incorporating one boost converter into each module for every extra dc port, thus maintaining scalability.

Similar to the two-port Y-converter, the three modified modules are interconnected at a central point denoted as m,

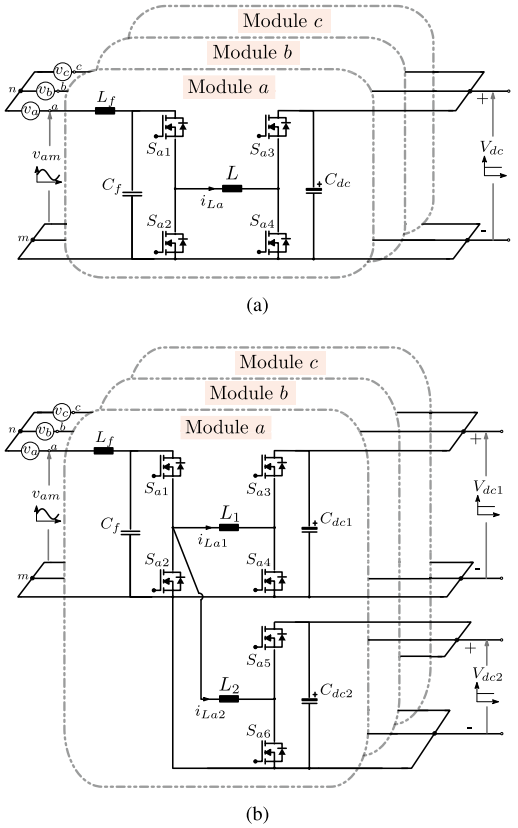

FIGURE 3. A schematic of two-port and multiport Y-converters in a modular form: (a) Two-port Y-converter; (b) The proposed Multiport Y-converter.

serving as the neutral point for the Y-connection of the modules. Since each module functions as a dc-dc converter, maintaining a non-negative voltage on the ac side of the module ($v_{\{a,b,c\}m} \geq 0$ V) is crucial. To achieve this, an offset voltage is required between the grid's neutral point n and m. A constant offset voltage (V_{off}) is then applied, which must exceed the peak value of the ac grid phase voltage ($\hat{V}_m$). The ac-side voltages v_{am}, v_{bm}, and v_{cm} can be expressed as follows:

$$v_{xm}(t) = v_x(t) + V_{off} = \hat{V}_m \sin(\omega t + \theta_x) + V_{off} \quad (1)$$

where v_x, with $x = (a, b, c)$, represents the ac grid phase voltages, ω denotes the ac grid frequency in rad/s, and θ_x signifies the respective phase angles of v_x.

Since V_{off} also represents the common-mode voltage (CMV) of the converter, the fixed CMV is an additional advantage of the proposed topology. While CMV can pose a threat to overall system performance by inducing leakage current through parasitic capacitances to ground and causing electromagnetic interference (EMI) in the high-frequency range [49], the fixed CMV in the proposed topology minimizes these issues as the leakage current flowing through parasitic capacitances is significantly reduced.

The analysis of the converter is presented by considering a single module (module a), as depicted in Fig. 4, and it similarly applies to the other modules as well. This module

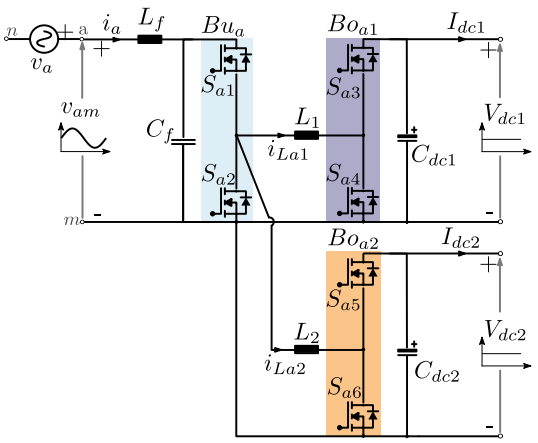

FIGURE 4. Module *a* of the proposed converter.

consists of the two inductors L_1 and L_2 along with three half-bridges: one on the ac side, labeled as Bu_a, and the others on the dc sides, labeled as Bo_{a1} and Bo_{a2}. Although this article mainly focuses on interfacing 400 V dc systems, the subsequent analysis is generalized for arbitrary values of V_{dc1} and V_{dc2}. Additionally, it is assumed that at least one of the dc ports' voltage is lower than the peak of the ac side voltage ($\hat{V}_m + V_{off}$), and V_{dc1} is lower than V_{dc2}. Based on these assumptions, the Bu_a and Bo_{a1} half-bridges are under control, ensuring that only one of them is modulated at any given moment, while the other remains clamped based on the values of v_{am} and V_{dc1}, whereas Bo_{a2} will be modulated continuously.

B. ANALYSIS AND FUNDAMENTAL RELATIONS

1) BUCK MODE

When v_{am} exceeds V_{dc1}, module a operates in buck mode. In this mode, the Bu_a half-bridge switches, while the Bo_{a1} half-bridge is clamped with S_{a3} on and S_{a4} off, as illustrated in Fig. 5(a). Simultaneously, the Bo_{a2} half-bridge operates with a fixed duty cycle, depending on the ratio between V_{dc1} and V_{dc2}. The duty cycles of S_{a1} and S_{a5}, denoted as d_{Bu_a} and $d_{Bo_{a2}}$, respectively, can be calculated using the following equations:

$$d_{Bu_a}(t) = \frac{V_{dc1}}{v_{am}(t)} = \frac{V_{dc1}}{\hat{V}_m \sin(\omega t) + V_{off}} \quad (2)$$

$$d_{Bo_{a2}} = \frac{V_{dc1}}{V_{dc2}} \quad (3)$$

The ac grid current of phase a, denoted as i_a, is assumed to be pure sinusoidal and in phase with its corresponding phase voltage v_a and then can be calculated as follows:

$$i_a(t) = \hat{I}_m \sin(\omega t) = (\hat{I}_{m1} + \hat{I}_{m2}) \sin(\omega t)$$
$$= \left(\frac{2P_{dc1}}{3\hat{V}_m} + \frac{2P_{dc2}}{3\hat{V}_m} \right) \sin(\omega t) \quad (4)$$

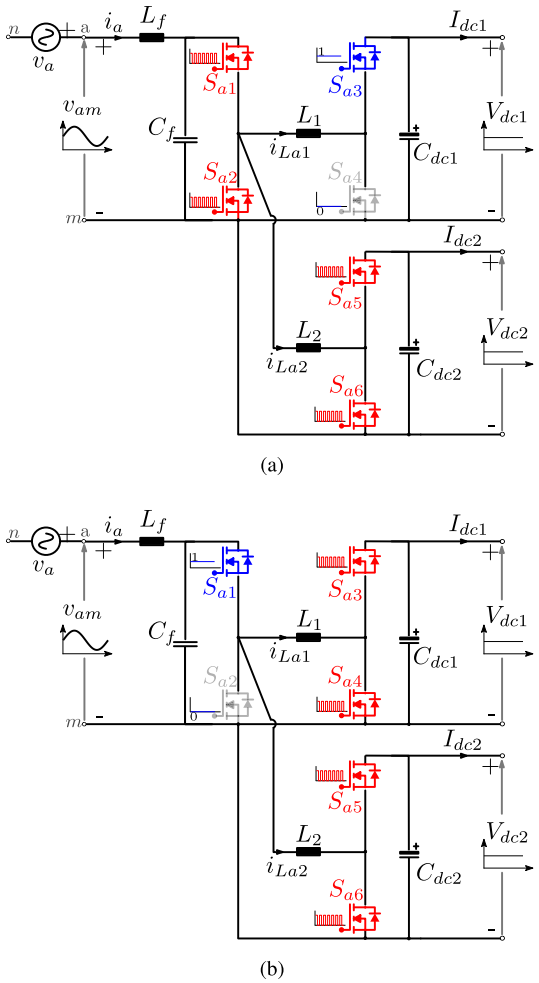

FIGURE 5. Operation modes of one module of the proposed converter: (a) Buck mode when $v_{am} > V_{dc1}$; (b) Boost mode when $v_{am} < V_{dc1}$.

where P_{dc1} and P_{dc2} represent the power delivered to dc ports 1 and 2, respectively, while $\hat{I}_m$ denotes the peak phase current. Additionally, $\hat{I}_{m1}$ and $\hat{I}_{m2}$ signify the equivalent reference peak phase current solely due to the power of dc MG#1 and #2, respectively.

The summation of average inductor currents (i.e., $i_{La1,av} + i_{La2,av}$), denoted as $i_{La,av}$, can be derived by applying Kirchhoff's current law (KCL) at the ac input of the module, as follows:

$$i_{La,av}(t) = i_{La1,av}(t) + i_{La2,av}(t) = \frac{i_a(t) - i_{Cf,a}(t)}{d_{Bu_a}(t)} \tag{5}$$

where $i_{Cf,a}$ represents the current through the input capacitor C_f. By neglecting $i_{Cf,a}$, the equation can be simplified as follows:

$$i_{La,av}(t) = \frac{i_a(t)}{d_{Bu_a}(t)} = \frac{\hat{I}_m \sin(\omega t)}{d_{Bu_a}(t)} \tag{6}$$

TABLE 1. Summary of the Basic Equations of the Proposed Converter

Parameter	Equation	Parameter	Equation
v_x	$\hat{V}_m \sin(\omega t + \theta_x)$	v_{xm}	$v_x + V_{off}$
d_{Bu_x}	$\frac{\min(v_{xm}, V_{dc1}, V_{dc2})}{v_{xm}}$	$d_{Bo_{x1}}$	$\frac{\min(v_{xm}, V_{dc1}, V_{dc2})}{V_{dc1}}$
$d_{Bo_{x2}}$	$\frac{\min(v_{xm}, V_{dc1}, V_{dc2})}{V_{dc2}}$	$i_{Lx,av}$	$\frac{\hat{I}_m \sin(\omega t + \theta_x)}{d_{Bu_x}}$
$i_{Lx1,av}$	$\frac{2P_{dc1} \sin(\omega t + \theta_x)}{3\hat{V}_m d_{Bu_x}}$	$i_{Lx2,av}$	$\frac{2P_{dc2} \sin(\omega t + \theta_x)}{3\hat{V}_m d_{Bu_x}}$

Using (4) and (6), $i_{la1,av}$ and $i_{la2,av}$ can be determined as follows:

$$i_{La1,av}(t) = \frac{\hat{I}_{m1} \sin(\omega t)}{d_{Bu_a}}$$
$$i_{La2,av}(t) = \frac{\hat{I}_{m2} \sin(\omega t)}{d_{Bu_a}} \tag{7}$$

2) BOOST MODE

The second mode of operation occurs when v_{am} falls below V_{dc1}. In this mode, module a operates in boost mode. In this mode, the Bo_{a1} half-bridge switches, while the Bu_a half-bridge is clamped with S_{a1} on and S_{a2} off, as depicted in Fig. 5(b). Simultaneously, the Bo_{a2} half-bridge operates with a time-varying duty cycle. The duty cycles of S_{a3}, denoted as $d_{Bo_{a1}}$, and $d_{Bo_{a2}}$ can be calculated using the following equations:

$$d_{Bo_{a1}}(t) = \frac{v_{am}(t)}{V_{dc1}} \tag{8}$$

$$d_{Bo_{a2}}(t) = \frac{v_{am}(t)}{V_{dc2}} \tag{9}$$

Using (7) and given that $d_{Bu_a} = 1$ in this mode, $i_{La1,av}$ and $i_{La2,av}$ can be determined as:

$$i_{La1,av}(t) = \hat{I}_{m1} \sin(\omega t)$$
$$i_{La2,av}(t) = \hat{I}_{m2} \sin(\omega t) \tag{10}$$

The key waveforms for module a of the proposed converter are plotted in Fig. 6. Additionally, the basic characteristic equations of the proposed converter are summarized in Table 1. These equations are applicable to any values of V_{dc1} and V_{dc2}, including the scenario presented in the analysis (where V_{dc1} is lower than V_{dc2}) and also when V_{dc1} is higher than V_{dc2}. The Appendix section presents formulas for calculating the rms current stresses of the Y-MPC inductors and semiconductor devices.

III. TOPOLOGY EVALUATION

This section presents a comprehensive evaluation of semiconductor losses of the proposed converter compared to the use of two separate Y-converters for integrating the two dc MGs with the ac grid. The objective of this evaluation is to demonstrate the advantages of adopting the proposed Y-MPC in enhancing

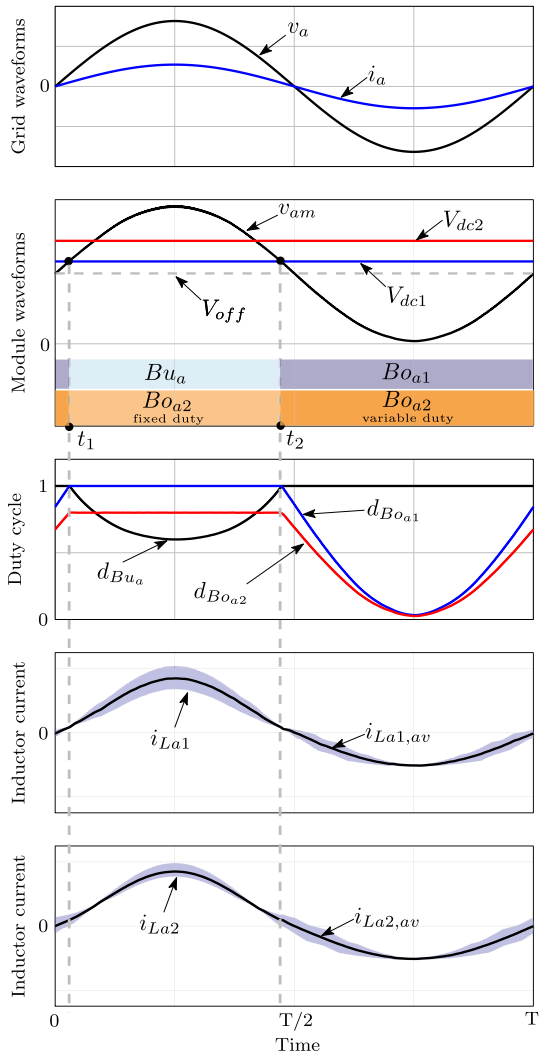

FIGURE 6. Key waveforms of module *a* of the proposed converter.

TABLE 2. Parameters of the Proposed Converter

Parameter	Symbol	Value
Rated ac power	$P_{ac,r}$	10 kW
Rated dc power	$P_{dc1,r}$, $P_{dc2,r}$	5 kW
ac line voltage, frequency	V_{ll}, f_o	400 V, 50 Hz
dc MG voltage	V_{dc1}, V_{dc2}	400 V ($\pm$10%)
Switching frequency	f_{sw}	62.5 kHz
Inductance	L_1, L_2	330 µH

the efficiency of the power electronic interface between the ac grid and the dc MGs. The specifications and ratings guiding the evaluation are summarized in Table 2. The chosen power level for the power exchange of each MG is 5 kw, which is selected for small-scale residential and commercial MGs. Therefore, two Y-converters rated at 5 kw each are adopted, while the Y-MPC is rated at 10 kw. The losses of the inductors L_1 and L_2 are not included in the comparison as both solutions exhibit the same inductor current waveforms, and the same values of inductors are adopted in both solutions.

For both the proposed converter and Y-converter, the ac-side half-bridges commutate at v_{xm}, which reaches a peak value of $\hat{V}_m + V_{off}$. Since V_{off} must surpass $\hat{V}_m$, the peak value is 665 V when V_{off} equals 340 V. Consequently, 1200 V SiC MOSFETs are chosen for the ac-side half-bridges in both converters. On the other hand, the dc-side half-bridges operate at the dc MG voltage (400 V), allowing the use of 650 V SiC MOSFETs for the dc-side devices in both converters.

In this assessment, SiC MOSFETs from Infineon are utilized. For the dc-side half-bridges, 650 V SiC MOSFETs with a nominal on-state resistance R_{ds} of $57m\omega$ (IMZA65R057M1H) are selected for both converters. For the ac-side half-bridges, 1200 V SiC MOSFETs with R_{ds} of 40 mΩ and 20 mΩ (IMZA120R040M1H, IMZA120R020M1H) are chosen for the Y-converter and the Y-MPC respectively. This selection is based on the higher current stresses endured by the ac-side half-bridges in the Y-MPC, which handle double the rated power and double the rated current compared to those in the Y-converter. Additionally, the junction temperature T_j of each device is calculated using PLECS thermal modeling simulations to ensure that the T_j of every device remains below 120 °C for all possible operating conditions.

The semiconductor losses of both converters are evaluated using PLECS while P_{dc1} and P_{dc2} are swept from -5 kW to 5 kW, covering all possible operating conditions for the proposed case study. The calculated semiconductor losses of both converters are reported in Fig. 7. At the rated power in rectification mode (i.e., when P_{dc1} and P_{dc2} equal to 5 kW), the Y-MPC exhibits semiconductor losses equal to 113.9 W, while the two Y-converters exhibit total semiconductor losses equal to 110.5 W. At the rated power in inversion mode (i.e., when P_{dc1} and P_{dc2} equal to -5 kW), the Y-MPC exhibits semiconductor losses equal to 119.7 W, while the two Y-converters exhibit total semiconductor losses equal to 117.2 W. Accordingly, both solutions attain almost the same semiconductor losses at rated power in both rectification and inversion modes, with slightly higher losses for the Y-MPC, mainly driven by the increased current stress on the ac-side half-bridges.

Although both converters exhibit similar semiconductor losses at rated power in both rectification and inversion modes, the proposed Y-MPC features significantly reduced losses for most of the operating range, especially at light-load and when the two dc MGs are directly transferring power between themselves. When a dc MG needs to absorb active power while the other MG presents surplus generation, the Y-MPC enables direct power sharing between the dc MGs, with the ac grid involved just to compensate for remaining power needs or unbalances.

For instance, when P_{dc1} and P_{dc2} equal 5 kW and -5 kW respectively, the Y-MPC allows for direct power transfer from dc MG#1 to dc MG#2 through the dc-side half-bridges, while

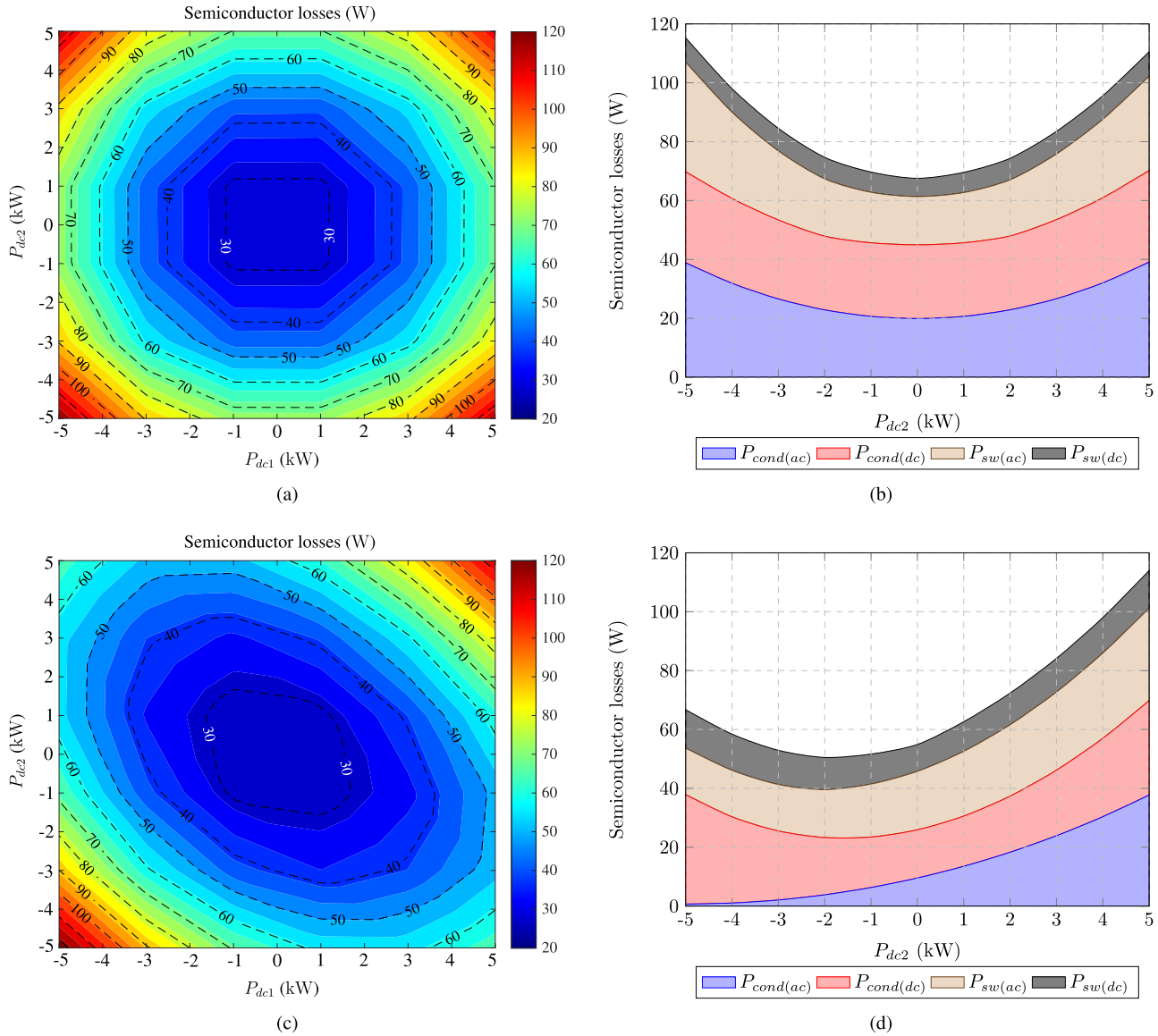

FIGURE 7. Evaluation of the semiconductor losses using PLECS: (a) For two Y-converters at different values of P_{dc1} and P_{dc2}; (b) Semiconductor losses breakdown of two Y-converters at P_{dc1} equal to 5 kW and different values of P_{dc2}; (c) For the proposed converter at different values of P_{dc1} and P_{dc2}; (d) Semiconductor losses breakdown of the proposed converter at P_{dc1} equal to 5 kW and different values of P_{dc2}.

the ac-side half-bridges do not exchange the power with the ac grid. On the other hand, in the two Y-converters, both ac-side and dc-side half-bridges handle the power, resulting in increased semiconductor losses compared to the Y-MPC. At P_{dc1} and P_{dc2} equal to 5 kW and −5 kW, the Y-MPC exhibits semiconductor losses equal to 66.5 W, while the two Y-converters exhibit total semiconductor losses equal to 115.3 W, showcasing the significant reduction in semiconductor losses gained by the proposed Y-MPC.

The semiconductor losses breakdown for the two Y-converters and the Y-MPC is displayed in Fig. 7(a) and 7(b), respectively, with P_{dc1} set to 5 kW and P_{dc2} swept from −5 kW to 5 kW. The losses are categorized into conduction losses of ac-side devices $P_{cond(ac)}$, conduction losses of dc-side devices $P_{cond(dc)}$, switching losses of ac-side devices $P_{sw(ac)}$, and switching losses of dc-side devices $P_{sw(dc)}$. The breakdown highlights that the reduction in losses is attributed to the decrease in conduction and switching losses of the ac-side devices, achieved by enabling direct power sharing between dc MG#1 and dc MG#2 through the proposed Y-MPC (i.e., P_{dc1} and P_{dc2} have opposite signs).

The presented evaluations show that the proposed Y-MPC offers superior performance compared to the two Y-converters. This enhanced performance includes a reduction in semiconductor device count from 24 to 18 devices, along with their corresponding driving circuitry. Additionally, it facilitates direct power sharing between the dc MGs, which is beneficial for minimizing dependence on the ac grid and improving the utilization of energy sources and storage in the dc MGs. Furthermore, this direct power-sharing contributes to

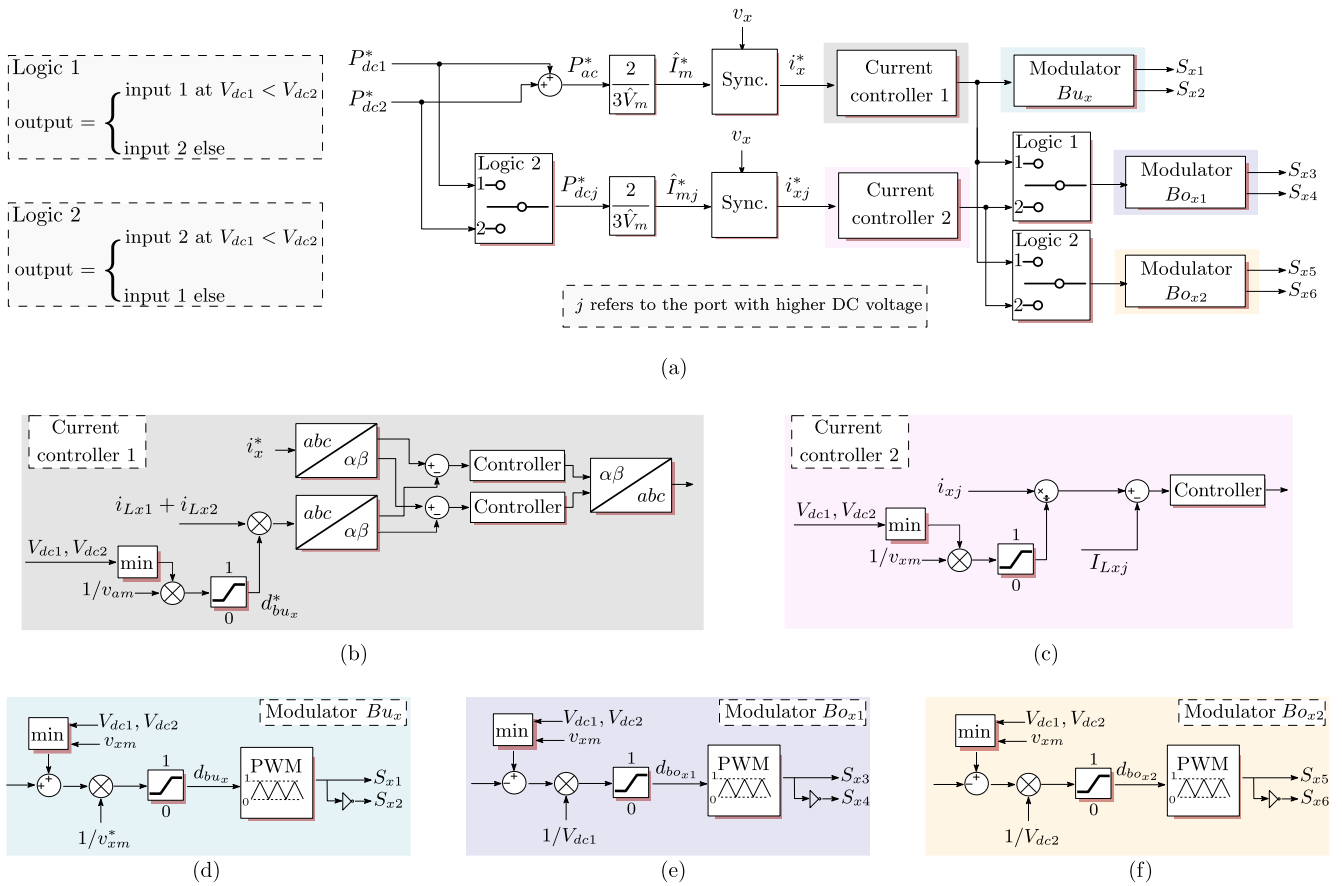

FIGURE 8. A detailed block diagram illustrating the control structure of the proposed converter: (a) The overall block diagram of the proposed control structure; (b) A detailed description of current controller 1 block; (c) A detailed description of current controller 2 block; (d) A detailed description of Bu_x modulators; (e) A detailed description of Bo_{x1} modulators; and (f) A detailed description of Bo_{x2} modulators.

the improved efficiency of the power electronic interface, as demonstrated in Fig. 7(a) and 7(c), where the larger blue area in the Y-MPC semiconductor losses plot indicates reduced losses compared to the two Y-converters across most of the operating range.

Finally, it is worth reporting that, in addition to the presented comparison between the Y-MPC and the two Y-converters, a detailed evaluation was conducted in [50] between the Y-MPC and the dc-link coupled MPC represented in Fig. 2(a). This latter non-isolated solution was implemented using a VSC as ac-dc converter and multiple buck converters as dc-dc converters. The outcome of the comparison shows that the Y-MPC outperforms the dc-link coupled MPC in terms of semiconductor losses and size of the magnetic elements, in addition to not requiring bulky intermediate dc-link capacitors.

IV. CONTROL AND MODULATION

This section describes the control and modulation schemes devised for the proposed converter. Such schemes were employed in the implemented experimental prototype to collect the results reported in the next Section V.

The operation of the converter is determined based on two power references P^*_{dc1} and P^*_{dc2} assumed to be assigned to the dc ports. In practical applications, such power references may be adjusted by a dc microgrid controller to achieve desired power balances among the ports, or they may vary based on the measured voltage level at the dc ports in a droop-like control fashion.

Fig. 8(a) displays the overall control organization. The implementation of the several control sub-blocks is provided and discussed in the following by referring to Fig. 8(b)–8(f). Considering Fig. 8(a), the two power references P^*_{dc1} and P^*_{dc2} are first translated into a power reference P^*_{ac} for the ac port of the converter, which is actually controlled as a current source to ensure a regulated power transfer with desired power factor at the ac port and the exchange of pure sinusoidal currents with the grid-connected at the port. A second current controller is employed to regulate the current exchanged at the dc port with the highest dc voltage.

By utilizing (4), P^*_{ac} is translated into the reference peak phase current, denoted as $\hat{I}^*_m$, which is subsequently input to the synchronization stage. The synchronization stage is responsible for generating sinusoidal grid current references, denoted as i^*_x, for the grid current control loop, displayed

TABLE 3. Parameters of the PI Controllers Adopted in the Current Control Loops as a Function of the Cross-Over Frequency f_c

Parameter	Symbol	Equation
Proportional gain	K_p	$2\pi f_c L$
Integral gain	K_i	$K_p f_c$

in Fig. 8(b). The ac grid currents are estimated based on measurements of the inductors' currents: by utilizing (6), i_x can be calculated by multiplying $i_{Lx,av}$ by d_{bu_x}. This approach allows the regulation of both the grid and the inductor currents without the need for additional cascaded loops. Subsequently, the reference and feedback currents in the *abc* frame are controlled by linear regulators in the $\alpha\beta$ frame. The output of the ac grid current controller is directed to the Bu_x modulator and the Bo_{x1} or the Bo_{x1} modulators based on the state of Logic 1 and Logic 2, as indicated in Fig. 8(a). The logic allows the connection of the ac current controller output to the modulator of the dc port with the lowest voltage. For Logic 1, its input 1 is selected when V_{dc1} is lower than V_{dc2}, input 2 is selected otherwise. Logic 2 operates complementarily, connecting input 2 to its output when V_{dc1} is lower than V_{dc2} or input 1 otherwise.

The second current controller in Fig. 8(a) is employed to regulate the power of the dc port with higher voltage. The reference of this controller is determined based on the power reference provided by Logic 2 (i.e., P^*_{dc2} when V_{dc1} is lower than V_{dc2}, P^*_{dc1} otherwise). Subsequently, the power reference is translated into the equivalent reference peak phase current attributable to the port with higher voltage (i.e., $\hat{I}^*_{m2}$ when V_{dc1} is lower than V_{dc2}, it is $\hat{I}^*_{m1}$ otherwise). The reference peak current is fed into the synchronization stage to generate the sinusoidal current references for the current controller. The controller, detailed in Fig. 8(c), employs the reference inductors currents of the dc port with higher voltage, defined using (7) and regulates the inductors currents in the *abc* frame, to prevent circulating currents in the converter. Similar to the ac grid current controllers, the output of the controllers is directed to either Bo_{x1} or Bo_{x2} modulators based on Logic 1 and Logic 2.

In the experimental verification, proportional-integrative (PI) controllers were used for implementing the current control loops in Fig. 8(b) and 8(c); controller design was based on the modeling reported in [51]. The crossover frequency f_c was set to $f_{sw}/15$. The specifications of the PI controllers are detailed in Table 3, with the assumption that $L_1 = L_2 = L$.

Finally, Fig. 8(d), 8(e), and 8(f) display the modulators for Bu_x, Bo_{x1}, and Bo_{x2}, respectively. These modulators are based on the equations for Bu_x, Bo_{x1}, and Bo_{x1} summarized in Table 1. For all modulators, the instantaneous minimum value of v_{am}, V_{dc1}, and V_{dc2} is defined. After adding the controllers' action, this value is divided by the corresponding dc-link voltage of the modulator's half-bridges to determine the duty cycle.

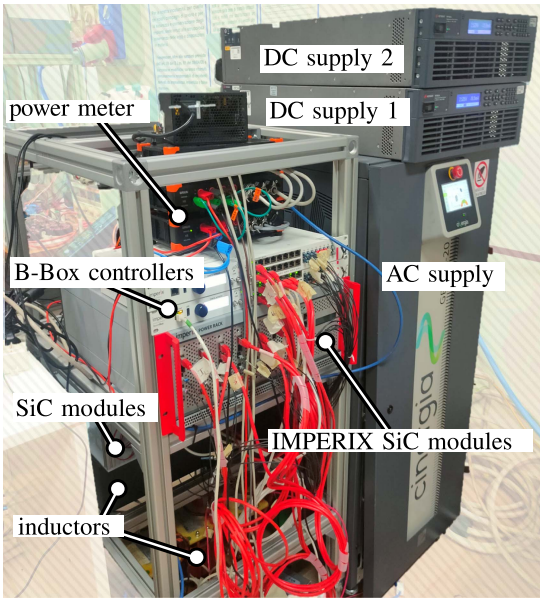

FIGURE 9. Picture of the experimental prototype of the proposed converter.

TABLE 4. SiC Devices and Passive Components Utilized in the Experimental Prototype

	Parameter	Symbol	Value
ac-side SiC MOSFET	Part number		UF4SC120023K4S
	Voltage	V_{DS}	1200 V
	On-state resistance	R_{DS}	23 mΩ
dc-side SiC MOSFET	Part number		C2M0080120D
	Voltage	V_{DS}	1200 V
	On-state resistance	R_{DS}	80 mΩ
Inductor parameters	Inductor	L_1, L_2	330 μH
	Core part number		Fluxsan FS-301026-2
	Inductor dc resistance	R_{Ldc}	21 mΩ
Input filter	Inductor	L_f	1.2 mH
	Capacitor	C_f	10 μF

V. EXPERIMENTAL RESULTS

Fig. 9 illustrates the experimental prototype of the Y-MPC, serving to validate the converter's operation and confirm the correctness of the presented waveforms. The Y-MPC prototype is constructed by combining six Imperix half-bridge power modules PEB8024 with C2M0080120D SiC MOSFETs for the dc-side half-bridges, while the ac-side half-bridges are implemented with UF4SC120023K4S SiC MOSFETs featuring lower R_{ds} compared to the dc-side devices due to higher current stresses. Control of the prototype is achieved using two synchronized B-box controllers in an input/output extension mode. Bidirectional ac and dc power supplies are employed to emulate the ac grid and dc MGs. L_1 and L_2 are implemented using 330 μH inductors, and a single-stage input filter is utilized with $L_f = 1.2$mH and $C_f = 10\,\mu$F. The specifications of the SiC devices and passive components utilized are summarized in Table 4.

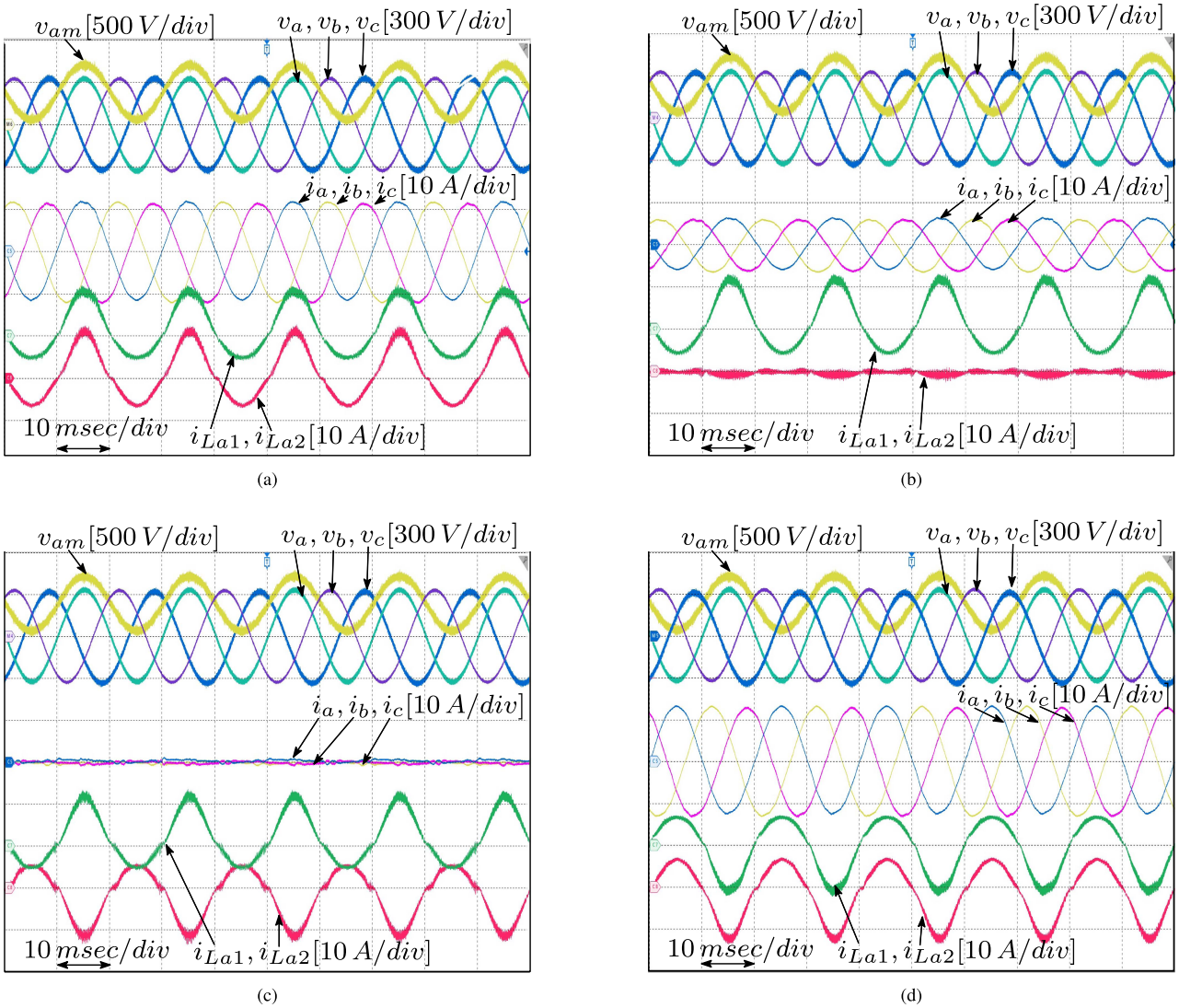

FIGURE 10. Experimental waveforms of the proposed converter with V_{dc1} and V_{dc2} are set to 360V and 400V under different values of P_{dc1} and P_{dc2}: (a) P_{dc1} and P_{dc2} both equal to 3 kW; (b) P_{dc1} and P_{dc2} equal to 3 kW and 0 kW, respectively; (c) P_{dc1} and P_{dc2} equal to 3 kW and -3 kW, respectively; and (d) P_{dc1} and P_{dc2} equal to -3 kW and -3 kW, respectively.

To capture the experimental waveforms, an 8-channel oscilloscope is employed to directly measure and display the quantities: v_a, v_b, v_{am}, i_a, i_b, i_c, i_{La1}, and i_{La2}. The voltage v_c is also displayed and calculated mathematically using the oscilloscope's internal math functions, as the imposed ac voltages are balanced (i.e., $v_c = -v_a - v_b$). Additionally, the Dewesoft SIRIUS XHS high-speed data acquisition system is employed to accurately measure the prototype's efficiency.

Experimental waveforms of the Y-MPC prototype are presented in Fig. 10 to showcase its performance under different operating conditions. For the presented operating points, V_{dc1} and V_{dc2} are set to 360 V and 400 V, respectively, with the ac grid voltage set to its rated value. Additionally, P_{dc1} is fixed at 3 kW. The first operating point is displayed in Fig. 10(a), where P_{dc2} equals 3 kW so both MGs are absorbing power from the ac grid. As evident from the waveforms, the ac currents are sinusoidal and well-synchronized with the ac voltages, resulting in a measured power factor equal to 0.99. The measured efficiency of the prototype at this operating point equals 94.75%.

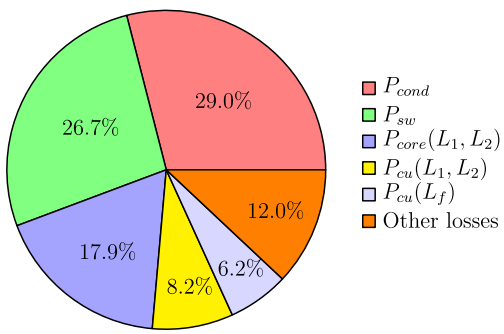

FIGURE 11. Calculated losses breakdown of the experimental prototype at P_{dc1} and P_{dc2} both equal to 3 kW.

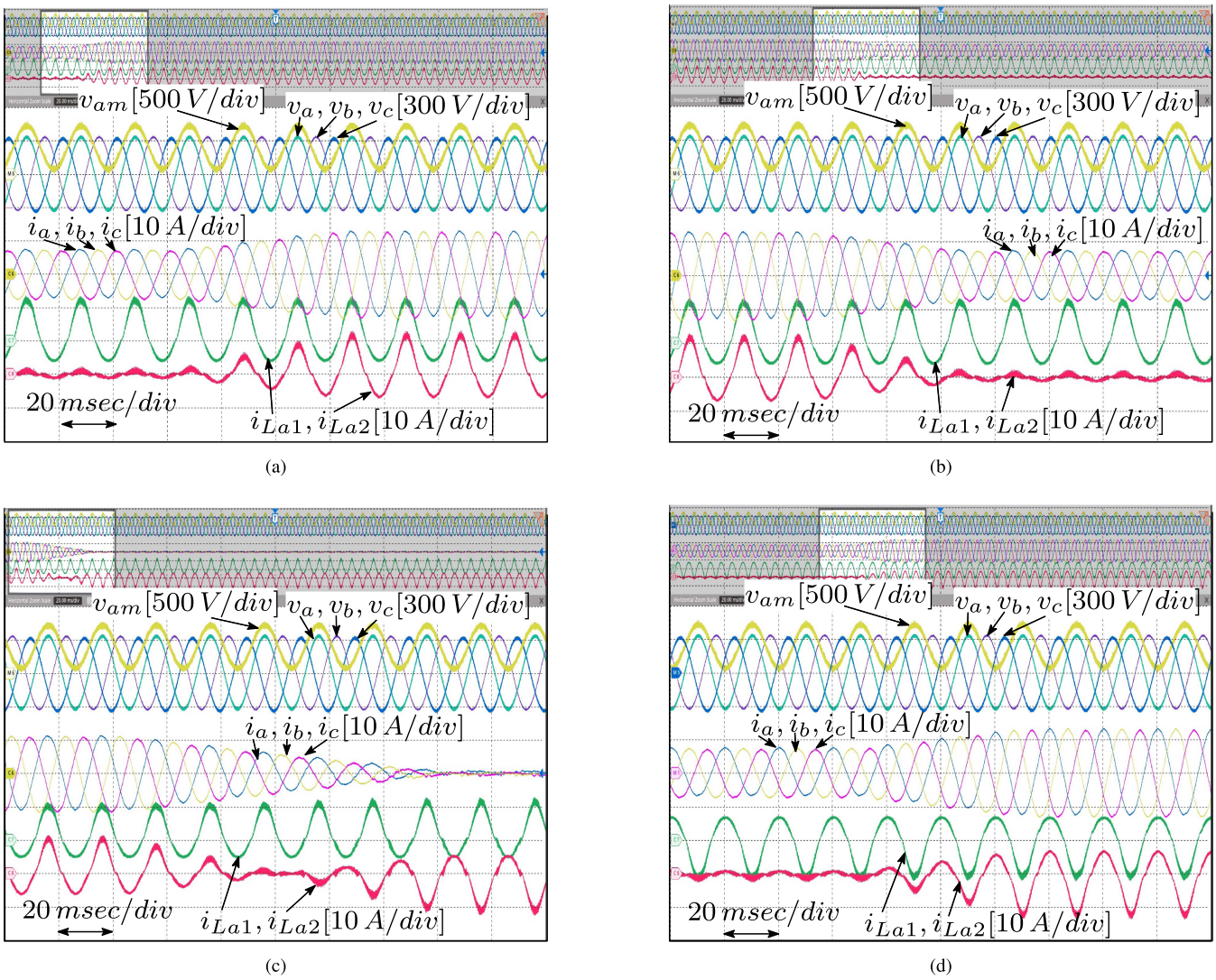

FIGURE 12. Experimental waveforms illustrating the transient behavior of the experimental prototype: (a) P_{dc1} equal to 3 kW and P_{dc2} increased from 0.3 kW to 3 kW; (b) P_{dc1} equal to 3 kW and P_{dc2} decreased from 3 kW to 0.3 kW; (c) P_{dc1} equal to 3 kW and P_{dc2} changed from 3 kW to −3 kW; (d) P_{dc1} equal to −3 kW and P_{dc2} changed from −0.3 kW to −3 kW.

The second operating point is presented in Fig. 10(b), where P_{dc2} is controlled to zero, representing the case when the power balance in dc MG#2 is attained only by its RESs, ESSs, and loads. In this case, only MG#1 absorbs power from the ac grid. To ensure zero power delivered to dc MG#2, i_{Lx2} is controlled to have an average low-frequency component set to zero. Therefore, in the presented waveforms, i_{La2} has only the high-frequency ripple component, resulting in no power for dc MG#2. The waveform i_{La1} remains the same as in the first operating point due to the fixed value of P_{dc1}. The measured efficiency of the prototype at this operating point equals 94.63%.

In the third operating point, depicted in Fig. 10(c), P_{dc2} is controlled to equal −3 kW. This case represents when dc MG#2 has an excess of power generation, allowing it to meet the power demand of dc MG#1 directly through the Y-MPC, and hence no active power is drawn from the ac grid. In the presented waveforms, i_{La2} is inverted with respect to i_{La1} due to the different direction of power flow of the dc MGs. Additionally, as there is no active power drawn from the ac grid, the ac grid currents are minimized, and only the current due to the reactive power drawn by C_f flows. The measured efficiency of the prototype at this operating point equals 95.71%.

In the last operating point, shown in Fig. 10(d), both P_{dc1} and P_{dc2} are set to −3 kW. This case represents when both dc MGs have a surplus power generation that is fed to the ac grid. In the presented waveforms, the ac grid currents are inverted with respect to their corresponding ac voltages, indicating the power flow direction to the ac grid. The measured efficiency of the prototype at this operating point equals 94.73%.

The calculated power loss breakdown for the experimental prototype, with both P_{dc1} and P_{dc2} set to 3 kW, is presented in Fig. 11. The losses are grouped as *i*) conduction and switching losses of semiconductor devices denoted as P_{cond} and P_{sw},

ii) core and copper losses of the main inductors denoted as $P_{core}(L_1, L_2)$ and $P_{cu}(L_1, L_2)$, and *iii*) copper losses of the input filter denoted as $P_{cu}(L_f)$. The calculated losses indicate that total semiconductor losses represent 55.7% of the total losses, while the losses in the main inductors account for 26.1% of the total losses. The term "other losses" includes losses not specifically calculated, such as those in the connections between modules, PCB losses, capacitor losses, etc., as well as the mismatch between the calculated and actual losses.

The transient behavior of the Y-MPC prototype is examined under various conditions. In Fig. 12(a), the converter initially operates with P_{dc1} and P_{dc2} equal to 3 kW and 0.3 kW, respectively. P_{dc2} is then increased from 0.3 kW to 3 kW while keeping P_{dc1} constant. In Fig. 12(b), P_{dc2} is decreased from 3 kW to 0.3 kW with P_{dc1} kept constant at 3 kW. In Fig. 12(c), P_{dc2} is changed from 3 kW to −3 kW with P_{dc1} kept constant at 3 kW, causing P_{ac} to drop from 6 kW to 0 kW. In Fig. 12(d), P_{dc2} is changed from −0.3 kW to −3 kW with P_{dc1} kept constant at −3 kW. The experimental results illustrate the change in i_{La2} to deliver the required P_{dc2}, while i_{La1} remains unaffected by the change in P_{dc2}, validating the power decoupling feature of the proposed converter and its ability to regulate the power flow to the dc MG#2 without causing a disturbance to the power flow of dc MG#1.

VI. CONCLUSION

This paper proposes a single-stage non-isolated MPC for interlinking the three-phase ac grid with 400 V dc MGs. Adopting an MPC for interlinking the dc MGs with the ac grid facilitates direct power sharing between the dc MGs, minimizing dependence on the ac grid, and improving the utilization of RESs and ESSs in the dc MGs compared to the conventional method of employing dedicated converters for each MG. The key motivations for the proposed converter include its ability to achieve single-stage power conversion among various ports, potentially leading to improved efficiency and power density. Moreover, the absence of bulky intermediate dc-link capacitors and HF transformers in the proposed topology contributes to enhanced power density and cost reduction. Additionally, although this study focuses on 400 V dc MGs, the proposed MPC offers buck-boost capability and bidirectional power flow across all ports, regardless of the dc ports' voltage, enabling direct interfacing with a broad spectrum of dc systems. The analysis and performance of the converter are thoroughly evaluated through experimental tests conducted under diverse operating conditions.

APPENDIX
CURRENT STRESS FORMULAS FOR INDUCTORS AND SEMICONDUCTOR DEVICES

This appendix summarizes formulas for calculating the rms current stresses of the Y-MPC inductors and semiconductor devices. These formulas can aid in properly sizing and selecting different components, calculating power losses, and deriving information useful for further comparisons with other topologies. The following equations are valid for any values of V_{dc1} and V_{dc2}, as long as at least one of them is lower than 650 V.

Three different modulation indexes are defined in order to calculate the component stresses. The first one, denoted as M_i, is utilized for calculating the stresses of the ac-side semiconductor devices as well as the inductors stresses. The other modulation indexes, denoted as M_{i1} and M_{i2}, are utilized for calculating the stresses of the dc-side semiconductor devices of dc port#1 and dc port#2, respectively. The three modulation indexes are calculated as follows:

$$M_i = \frac{2\ \min\left(V_{dc1}, V_{dc2}\right)}{3\hat{V}_m} \tag{A1}$$

$$M_{i1} = \frac{2V_{dc1}}{3\hat{V}_m} \tag{A2}$$

$$M_{i2} = \frac{2V_{dc2}}{3\hat{V}_m} \tag{A3}$$

Using (4) and (A1), the current stresses of L_1 and L_2 are calculated as follows:

$$I_{Lx1,\mathrm{rms}} = \hat{I}_{m1} \cdot \frac{\sqrt{3M_i^2 - \frac{8}{3}M_i + \frac{16}{3}}}{2\sqrt{2}M_i} \tag{A4}$$

$$I_{Lx2,\mathrm{rms}} = \hat{I}_{m2} \cdot \frac{\sqrt{3M_i^2 - \frac{8}{3}M_i + \frac{16}{3}}}{2\sqrt{2}M_i} \tag{A5}$$

To calculate the current stresses of the ac-side devices, the rms value of the summation of L_1 and L_2 currents, denoted as $I_{Lx,\mathrm{rms}}$, is determined. Then, the stresses of the ac-side devices are calculated as follows:

$$I_{Lx,\mathrm{rms}} = \hat{I}_m \cdot \frac{\sqrt{3M_i^2 - \frac{8}{3}M_i + \frac{16}{3}}}{2\sqrt{2}M_i} \tag{A6}$$

$$I_{Sx1,\mathrm{rms}} = I_{Lx,\mathrm{rms}} \cdot \frac{\sqrt{1.5M_i^2 - \frac{32M_i}{45} + \frac{4}{45}}}{M_i} \tag{A7}$$

$$I_{Sx2,\mathrm{rms}} = I_{Lx,\mathrm{rms}} \cdot \frac{\sqrt{-0.5M_i^2 + \frac{32M_i}{45} - \frac{4}{45}}}{M_i} \tag{A8}$$

Using (A2) and (A4), the current stresses of the dc-side semiconductor devices of dc port#1 are calculated as follows:

$$I_{Sx3,\mathrm{rms}} = I_{Lx1,\mathrm{rms}} \cdot \frac{\sqrt{-\frac{2}{13}M_{i1}^2 + 1.1M_{i1} - \frac{4}{13}}}{M_{i1}} \tag{A9}$$

$$I_{Sx4,\mathrm{rms}} = I_{Lx1,\mathrm{rms}} \cdot \frac{\sqrt{\frac{15}{13}M_{i1}^2 - 1.1M_{i1} + \frac{4}{13}}}{M_{i1}} \tag{A10}$$

Similarily, using (A3) and (A5), the current stresses of the dc-side semiconductor devices of dc port#2 are calculated as follows:

$$I_{Sx5,\mathrm{rms}} = I_{Lx2,\mathrm{rms}} \cdot \frac{\sqrt{-\frac{2}{13}M_{i2}^2 + 1.1M_{i2} - \frac{4}{13}}}{M_{i2}} \tag{A11}$$

$$I_{Sx6,\mathrm{rms}} = I_{Lx2,\mathrm{rms}} \cdot \frac{\sqrt{\frac{15}{13}M_{i2}^2 - 1.1M_{i2} + \frac{4}{13}}}{M_{i2}} \tag{A12}$$

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Open Access funding provided by 'Università degli Studi di Padova' within the CRUI CARE Agreement