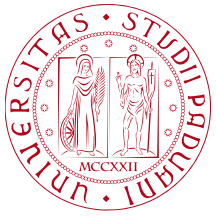

UNIVERSITÀ
DEGLI STUDI
DI PADOVA

Head Office: Università degli Studi di Padova

Department of Management and Engineering

PH.D. COURSE IN MECHATRONICS AND PRODUCT INNOVATION ENGINEERING

CURRICULUM: MECHATRONICS

CYCLE: XXXVI

High-Efficiency Electronic Power Converters for Extreme Fast Charging (XFC) Stations

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List of Acronyms

ac alternate-current

ac-dc ac-to-dc

ac-FE ac front-end

BB-LLC buck-boost LLC

BEV battery electric vehicle

BPF band-pass filter

CC constant-current

CCM continuous conduction mode

CO_2 carbon dioxide

CV constant-voltage

DAB dual active bridge

dc direct-current

dc-dc dc-to-dc

DCX dc-transformer

DPT double-pulse tester

EMI electromagnetic interference

ESC extremum seeking control

ESR equivalent series resistance

EV electric vehicle

FB-LLC full-bridge LLC

FET field-effect transistor

FFT fast Fourier transform

FHA first harmonic approximation

FPGA field programmable gate array

GaN Gallium Nitride

HB-LLC half-bridge LLC

HEMT high electron mobility transistor

HF high-frequency

ICEV internal combustion engine vehicle

IPOS input-parallel output-series

LPF low-pass filter

LV low-voltage

MOSFET metal-oxide-semiconductor field-effect transistor

MPPT maximum power point tracking

MV medium-voltage

PCB printed circuit board

PFC power factor correction

PHEV plug-in hybrid electric vehicle

PID proportional-integral-derivative

PPP partial-power processing

PSFB phase-shift full-bridge

RES renewable energy sources

rms root-mean-square

RT real-time

Si Silicon

SiC Silicon Carbide

SM switching mode

SoC state of charge

SST solid-state transformer

TBB twin-bus buck

WBG wide-bandgap

XFC extreme fast charger

ZCS zero-current switching

ZVS zero-voltage switching

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Abstract

The transportation sector significantly contributes to global greenhouse gas emissions, accounting for approximately 23% of worldwide carbon dioxide (CO_2) emissions. In response to environmental concerns and the need to contrast climate change, governments are supporting the phase-out of internal combustion engine vehicles (ICEVs) no longer meeting the stringent emission standards and, at the same time, promoting the adoption of electric vehicles (EVs). This transition is supported by several advantages, including absence of local pollution, reduced maintenance costs, lower overall ownership expenses, charging using locally available renewable energy, and limited acoustic emissions. Nonetheless, several challenges hinder the widespread adoption of EVs. Potential EV buyers are often deterred by the higher initial purchase price than equivalent ICEVs, limited driving range (typically 250 to $500\,\mathrm{km}$), longer charging times, often exceeding 30 minutes for a full charge, and the lack of charging infrastructure. Expanding the charging infrastructure and enhancing the related technologies is crucial for a broader adoption of EVs. Notably, battery chargers of extraordinary performance are required to meet expectations and allow reduced charging times. EV extreme fast chargers (XFCs) are being developed, featuring charging powers of $350\,\mathrm{kW}$ or more. At the core of such systems, advanced high-power dc-dc converters–having efficiency, flexible interconnection, and safety as key design features–perform the involved power processing.

This dissertation focuses on the development of a dc-dc converter module for EV XFC systems facing the challenge of obtaining galvanic isolation and high conversion efficiency over the wide range of operating conditions occurring in battery charging. The dissertation's key contributions are divided into several parts. Initially, it provides an overview of existing dc-dc converter topologies suitable for EV XFC systems, exploring multi-stage

configurations to enhance efficiency beyond the limitations of resonant converters. Differently, multi-stage topologies can accommodate wider operating voltage ranges with very high efficiencies. Novel multi-stage topologies are introduced and then compared. The dissertation also presents loss models for these converters, enabling comprehensive simulations to estimate losses and pinpoint areas for improvement. A simulation-based comparison of multi-stage dc-dc converter topologies is performed to identify optimal topologies for efficient EV charging, which are then investigated experimentally. The central part of the work presents the analysis and experimental results of the proposed buck-boost LLC (BB-LLC) and twin-bus buck (TBB) converters, contributing to the development of efficient two-stage EV charging solutions. It covers modeling, design considerations, and modulation techniques. The dissertation's final section introduces an extremum seeking control (ESC) technique to determine optimal operating points for the TBB converter. This technique offers a model-free on-line optimization method that is robust against parameter uncertainties and changes in operating point. Overall, it is shown that the solution features high conversion efficiency over a wide range of output voltages.

In conclusion, the research efforts described in this dissertation yielded several contributions, particularly in the domains of converter analysis and modeling, converter design and prototyping, and converter on-line optimization. Experimental results are reported considering a converter module prototype rated $10\,\mathrm{kW}$, input voltage $800\,\mathrm{V}$, and output range $250\,\mathrm{V}$ to $500\,\mathrm{V}$, employing Silicon Carbide (SiC) and Gallium Nitride (GaN) semiconductors. These contributions are instrumental in advancing the state-of-the-art in high-power dc-dc converters for EV charging applications, contributing to a more sustainable and environmentally friendly transportation landscape.

Acknowledgments

I wish to thank, first and foremost, my supervisors Prof. Tommaso Caldognetto and Prof. Paolo Mattavelli for their invaluable support during my Ph.D. studies. They have wisely and carefully guided me in my research activities, always ready to provide the finest help and advice when needed. All the positive scientific results I achieved during these years are owed to them. In particular, I extend a special thanks to Tommaso Caldognetto, who has been a constant and pleasant presence during my Ph.D. His guidance and infinite patience have been crucial for my activities and my professional growth.

With them, I would like to thank all the people of the Power Electronics Group at the University of Padova: Prof. Giorgio Spiazzi, Prof. Simone Buso, Prof. Paolo Magnone, Dr. Davide Biadene, Dr. Giovanni Bonanno, Dr. Marco Stellini, and Dr. Andrea Petucco, for their contributions and helpful suggestions.

I would also like to express my gratitude to my Ph.D. colleagues Alessandro Vaccaro, Ezio Gallo, Stefano Cabizza, and Ružica Cvetanović, who have been pleasant company to talk with and share points of view during our coffee breaks.

Special thanks go to my parents, sister, and brother, as well as my friends, who have always supported me.

Lastly, the deepest thanks go to the person I love, Isabella, for her love and infinite patience during my period of study. She has always supported me morally and emotionally in times of need, and it is to her that I dedicate this significant achievement.

Chapter 1

Introduction

Growing concerns about climate change are driving the developments towards decarbonization and clean technology. The escalating apprehension regarding the long-term environmental repercussions of carbon dioxide (CO_2) emissions from fossil fuel combustion has prompted a worldwide transition towards renewable energy generation and extensive electrification across domestic and industrial sectors. This transformative shift is motivated by the urgent imperative to contrast climate change and cut greenhouse gas emissions [1–4].

In 2022, global energy-related CO_2 emissions increased by 0.9%, equivalent to 321 million tonnes, reaching a new record of over 36.8 billion tonnes [1]. This rise in emissions was notably slower than the global economic growth rate, which stood at 3.2%. This trend signifies a return to the decade-long pattern that was briefly altered in 2021 due to the swift and emissions-intensive economic recovery from the Covid-19 pandemic, as can be noted form Fig. 1.1a. Several factors contributed to the increase in emissions, including extreme weather events, as well as a higher number of nuclear power plants being offline. However, there was a notable reduction of 550 million tonnes in emissions due to the expanded deployment of clean energy technologies [1].

The transportation sector plays a pivotal role in this transition, contributing approximately to 23% of global CO_2 emissions, as depicted in Fig. 1.1b [1, 4]. Consequently, it has become a focal point of political attention and regulatory action. Governments worldwide are enacting stringent emissions standards and regulations to mitigate pollution and address the climate change [2, 6]. As a result, there is a gradual phasing out of internal

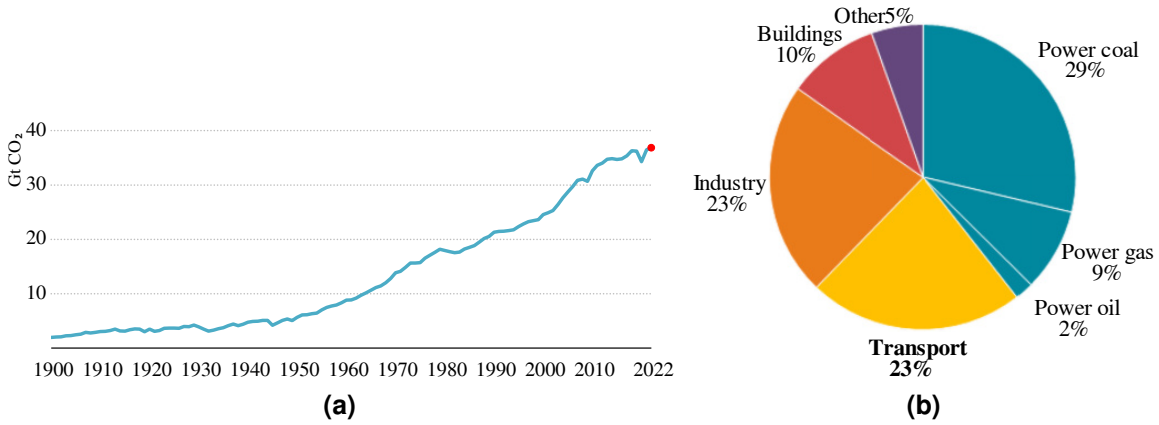


Figure 1.1: Global CO_2 emissions. (a) 1900-2022 [1]; and (b) emissions by sector [5].

combustion engine vehicles (ICEVs) due to their inability to meet these stringent emission requirements. The electric vehicles (EVs), powered by renewable electricity, are emerging as a promising alternative to traditional ICEVs. They offer the potential to significantly reduce petroleum consumption and greenhouse gas emissions [1–4, 6], exploiting alternative energy resources. Simultaneously, there has been a remarkable surge in the adoption of EVs [6]. This shift is supported by several compelling advantages, such as: absence of local pollution, reduced maintenance costs, lower overall ownership expenses, charging using locally available renewable energy, and limited noise emissions [2, 4, 6, 7].

In 2022, despite global challenges like supply chain disruptions and economic uncertainties, electric car sales, including both battery electric vehicles (BEVs) and plug-in hybrid electric vehicles (PHEVs), exceeded 10 million units, marking a 55% increase from the previous year. Impressively, the electric vehicle market has shown exponential growth, with sales increasing from 1 million to over 10 million in just five years. Furthermore, electric cars' share of the total car market grew from 9% in 2021 to 14% in 2022, reflecting substantial market penetration. Despite this progress, several challenges must still be addressed to further accelerate the adoption of EVs. Potential EV buyers are often deterred by the higher upfront costs compared to their internal combustion engine counterparts [8]. Concerns about "range anxiety" persist due to the typical limited range of EVs, usually falling in the range of 250 to 500 kilometers [9]. Additionally, the extended charging times, often exceeding 30 minutes for a full charge, and the insufficient availability of charging

Figure 1.2: Fast-charging station. Source: [14].

infrastructure are significant barriers to widespread EV adoption [2, 3, 8, 10–12].

Overcoming these challenges necessitates improvements in current battery technology, including cost reduction, enhanced energy density, faster charging rates, and longer operational lifespans. Important is the substantial scaling up of charging infrastructure to meet the growing demand for faster and more readily accessible charging stations [2,3,6,11,13]. Within this context, this dissertation focuses on addressing the technical challenges associated with the development of dc extreme fast chargers (XFCs). These chargers play a pivotal role in alleviating one of the major hurdles to widespread EV adoption, i.e., long charging times.

1.1 Electric Vehicle Extreme Fast Charging

The adoption of EVs faces significant challenges, primarily related to charging time and driving range. This growing demand and the need to cover extensive journeys on a single charge has led to many modern EVs providing driving ranges exceeding 350 kilometers. This enhanced range has, in turn, prompted the need for XFCs infrastructure, characterized by an output voltage range of 500 - $1000\,\mathrm{V}$ with charging powers of $350\,\mathrm{kW}$ or more [3,9]. Distinguishing the XFCs from conventional dc fast-chargers in Fig. 1.2 typically rated at 50 - $150\,\mathrm{kW}$, this new generation of chargers has gained significant attention. The primary objective of XFCs is to recharge an EV's battery from 10% to 80% in a time comparable to

refueling ICEVs, a feature especially beneficial for long-distance travel and public transportation [3, 13]. This addresses the issue of range anxiety and allows for the development of smaller, more affordable EVs, expanding their market reach.

To put this into perspective, let's consider an EV with a battery capacity of $60\,\mathrm{kWh}$ and an energy consumption of $15\,\mathrm{kWh}$ per 100 kilometers [11]. A typical on-board charger rated at $11\,\mathrm{kW}$ would need over 4 hours to add 300 kilometers of range to an EV. Even a $50\,\mathrm{kW}$ dc fast-charger would require about an hour for the same task, while a $135\,\mathrm{kW}$ Tesla supercharger could achieve it in 20 minutes. The emergence of $350\,\mathrm{kW}$ dc XFCs now offers the potential to add 300 kilometers of range in 10 minutes, getting closer to the refueling experience of gasoline vehicles [9, 11]. The emergence of these XFCs present numerous technical challenges in charger design and operation. This section outlines the key requirements, discusses the challenges, and provides an overview of the current state-of-the-art in extreme fast charging technology.

1.1.1 Challenges

From a technical standpoint, the development of extreme fast battery chargers comes with a set of critical requirements. Firstly, these chargers should deliver high conversion efficiency to effectively transfer energy to the EV while minimizing heat generation. Additionally, high power density is essential to reduce the overall size and footprint of the charging system. Safety is a paramount concern, requiring galvanic isolation between the main grid and the EV's battery [3, 15, 16]. This ensures that the charging process is safe and complies with established safety standards. Moreover, these chargers should support a wide output voltage range to accommodate a broad range of commercially available EVs. However, achieving high efficiency, power density, galvanic isolation, and wide output voltage range in a single system poses significant technical challenges, requiring sophisticated design and control strategies [11]. Furthermore, maintaining grid stability and quality is crucial. Therefore, XFCs need to generate clean grid-side currents with low distortion and harmonics [11]. These charging stations introduce high-power loads that can overload transformers, increase power losses, and decrease overall power quality. Notably, to address these

Table 1.1: Specifications of currently available dc-fast and XFCs.

Charger	Power	Input voltage	Output voltage	Weight
EVTEC espresso&charge	150 kW	400 Vac ±10%	170 - 940 V	500 kg
Siemens VersiCharge Ultra	175 kW	480 Vac ±10%	200 - 920 V	1265 kg
Blink RT 175-S	175 kW	480 Vac ±10%	200 - 920 V	1248 kg
Delta UFC 200	200 kW	400 Vac ±10%	200 - 920 V	550 kg
Tesla Supercharger V3	250 kW	430 Vac ±10%	50 - 410 V	NA*
Beny BADC262-D	262 kW	380 Vac ±15%	150 - 1000 V	500 kg
ABB Terra 360	350 kW	400 Vac ±10%	200 - 920 V	720 kg
Tritium Veefil PK350	350 kW	480 Vac ±10%	150 - 920 V	913 kg
Enel JuicePump	350 kW	480 Vac ±10%	50 - 950 V	2000 kg
Enercon e-charger 600	350 kW	400 Vac ±10%	200 - 920 V	3800 kg
PHIHONG DO 360	360 kW	480 Vac ±10%	150 - 950 V	1000 kg
INGEREV RAPID ST400	400 kW	400 Vac ±10%	50 - 1000 V	2090 kg
EnerCharge EC500	480 kW	400 Vac ±10%	50 - 1000 V	900 kg

* NA: not available.

challenges, integrating multiple renewable resources, energy storage systems, and providing ancillary services to the grid becomes essential, both fo the power distribution system and XFC stations [3, 9, 11].

In conclusion, while the need for rapid charging infrastructure for EVs is evident, its deployment comes with technical, economic, and grid management challenges. These challenges are being addressed through innovations in station design, integration of renewable resources, and smart charging management, all aimed at making EV charging efficient, accessible, and sustainable [3, 11].

1.1.2 State-of-the-Art and Standards

DC fast-chargers are critical components of the EV charging infrastructure. They provide a direct flow of dc current directly to the vehicle's battery pack while maintaining galvanic isolation from the mains and other vehicles [11,12,16–18]. Currently, several commercially available dc fast chargers have power ratings ranging from 50 kW to 150 kW. To meet the 10-minute charging time limit that is considered acceptable by most drivers during travel, an increasing number of 350 kW charging stations are gaining popularity [3, 6, 9, 11]. Table 1.1 summarizes some dc fast-chargers and relevant currently available XFCs. As can

be observed, there is a shift towards higher-voltage battery systems, which can provide numerous benefits, including reduced cable size and weight, as well as lower converter and motor currents, resulting in improved overall efficiency [3, 13]. Several EV manufacturers have embraced this trend in their flagship electric vehicles, allowing for remarkably fast recharging. Table 1.2 reports EVs models by some representative manufacturers. Automakers, including Hyundai, Porsche, Kia, Lotus, Audi, Lucid Motors, XPENG, and BYD, have adopted $800\,\mathrm{V}$ battery systems to reduce weight and charging times [2, 3, 11, 18].

All available XFCs support one or more of the existing dc fast-charging standards, presented in Table 1.3. Fast-charging standards include CCS (EU-defined), CHAdeMO (Japan-defined), and GB/T (China-defined), each with varying maximum charging power capacities. Fast-charging standards for dc chargers have evolved to accommodate XFCs. For instance, CHAdeMO and CCS standards have introduced new voltage and power classes, with CHAdeMO defining $1\,\mathrm{kV}$, $400\,\mathrm{kW}$ charging levels and CCS having a maximum of $920\,\mathrm{V}$ and $350\,\mathrm{kW}$ [3, 13]. These standards are widely compatible due to their alignment with international standards for both ac and dc charging modes. Tesla adopts its own fast-charging standard for EVs. Efforts have also made to prepare for future increases in maximum charging power demands, with the development of a $900\,\mathrm{kW}$ standard, ChaoJi, which significantly increases maximum dc voltage and output current to $1500\,\mathrm{V}$ and $600\,\mathrm{A}$, respectively. Efforts are currently underway to develop a new megawatt charging standard, the Ultra-ChaoJi [20]. This development extends beyond passenger EVs, looking at electrified transportation such as buses, trucks, and aircraft [3, 6, 13]. The adoption of XFCs and advancements in battery technology and cooling systems represents crucial steps toward achieving parity in recharging/refueling times between EVs and ICEVs [13].

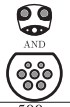
1.1.3 Architectures

XFCs are commonly located along highways to cater to long-distance travels. Typically, a standard XFC station incorporates several XFCs, resulting in a total power capacity in the megawatt range [3, 11]. To prevent overloading the electricity grid, a direct connection

Table 1.2: Specifications of representative commercial EV models [19].

EV model	Year	Battery capacity	Battery voltage	Distance range	Max charging power (time)
Citroen e-C4	2023	54 kWh	400 V	320 km	101 kW(29m)
Jeep Avenger Electric	2023	54 kWh	400 V	300 km	100 kW(26m)
Lexus RZ 450e	2023	71 kWh	400 V	320 km	147 kW(28m)
Subaru Solterra AWD	2022	71 kWh	400 V	320 km	147 kW(28m)
Fiat 600e	2023	54 kWh	400 V	305 km	100 kW(26m)
Opel Astra Electric	2023	54 kWh	400 V	310 km	100 kW(26m)
Toyota bZ4X FWD	2022	71 kWh	400 V	340 km	147 kW(28m)
Renault Megane E-Tech EV60	2022	95 kWh	400 V	380 km	129 kW(30m)
Nissan Ariya 87kWh	2022	91 kWh	400 V	385 km	130 kW(35m)
NIO ET7 75 kWh	2022	75 kWh	400 V	400 km	140 kW(31m)
Zeekr X Long Range RWD	2023	69 kWh	400 V	360 km	150 kW(28m)
BYD SEAL RWD Design	2023	84 kWh	800 V	500 km	150 kW(38m)
Smart #3	2023	66 kWh	400 V	355 km	150 kW(27m)
Mini Countryman E	2023	67 kWh	400 V	380 km	130 kW(29m)
MG MG4 Electric	2022	64 kWh	400 V	360 km	140 kW(27m)
Volvo C40	2022	82 kWh	400 V	420 km	205 kW(28m)
Peugeot e-3008 LR	2024	103 kWh	400 V	520 km	160 kW(32m)
Skoda Enyaq Coupe iV 80	2022	82 kWh	400 V	475 km	143 kW(27m)
BMW i4 eDrive40	2021	84 kWh	400 V	515 km	207 kW(27m)
Tesla Model S Dual Motor	2023	100 kWh	400 V	575 km	250 kW(30m)
Volkswagen ID.7 Pro S	2023	91 kWh	400 V	520 km	200 kW(27m)
Mercedes EQS 450+	2021	120 kWh	400 V	432 km	207 kW(28m)
XPENG G9 RWD LR	2023	98 kWh	800 V	470 km	300 kW(20m)
Lucid Air Pure AWD	2023	94 kWh	800 V	590 km	200 kW(25m)
Audi e-tron GT quattro	2021	93 kWh	800 V	420 km	268 kW(17m)
Lotus Eletre	2023	112 kWh	800 V	495 km	350 kW(20m)
Kia EV6 LR 2WD	2021	77 kWh	800 V	410 km	233 kW(16m)
Porsche Taycan Plus	2023	93 kWh	800 V	485 km	268 kW(17m)
Hyundai IONIQ 6 LR 2WD	2022	77 kWh	800 V	495 km	233 kW(16m)

Table 1.3: Overview of fast-charging standards. Adapted from [3].

Standard	CHAdeMO	GB/T	CCS Type 1	CCS Type 2	Tesla	ChaoJi
Compliant Standards	IEEE 2030.1.1 IEC 62916-3	IEC 62916-3	SAE J1772 IEC 62916-3	IEC 62916-3	No related items	CHAdeMO and GB/T (IEC and CCS not yet but is ongoing)
Connector Inlet						
Maximum Voltage (V)	1000	750	600	900	500	1500
Maximum Current (A)	400	250	400	400	631	600
Maximum Power (kW)	400	185	200	350	250	900
Maximum Market Power (kW)	150	125	150	350	250	N.A.
Communication Protocol	CAN		PLC		CAN	CAN
V2X Function	Yes	No			No	Yes
Start year	2009	2013	2014	2013	2012	2020

to the medium-voltage (MV) distribution grid is typically adopted in the XFCs reported in Table 1.1 [3, 9, 11, 15, 17]. However, a challenge arises when multiple EVs are charging simultaneously, leading to a highly variable power demand. By strategically scheduling the charging of multiple vehicles and taking advantage of the diversity in EV battery capacities and charge acceptance based on state of charge (SoC), it's possible to substantially reduce the actual power demand from the grid compared to the rated value [11]. Additionally, if an energy storage system is available at the station, it can further decrease peak power demand, contributing to a more efficient and stable charging process [3, 11, 18].

In charging stations, each charging port typically requires isolation from the grid and other charging ports for safety requirements and to facilitate energy transfer [17]. Safety standards establish that these charging stations must ensure galvanic isolation, including isolation monitoring, between the distribution grid and the EV's battery [16]. The vehicle chassis is connected to the ground through the charging cable, ensuring that the driver can safely touch the vehicle even in the presence of an isolation fault.

Inside the XFC station, the low-voltage (LV) distribution network can be either ac or dc, as shown in Fig. 1.3 [3, 11, 15, 17]. For ac-connected systems in Fig. 1.3b, a step-down transformer interfaces the MV grid with a three-phase LV ac sub-grid. Each charger has a separate ac-dc stage. This approach involves more conversion stages, increasing complexity and cost while reducing efficiency. Advantages include the maturity of rectifier technology, established standards, and well-developed practices for ac power distribution. Most state-of-the-art XFC stations in Table 1.1 follow this approach. DC-connected systems in Fig. 1.3a use a central front-end ac-dc converter to create a dc bus, offering a more energy-efficient way to interface with energy storage and renewable energy sources (RES). This central front-end typically comprises a MV-LV grid transformer followed by rectifier stage. Alternatively, a solid-state transformer (SST) can be used, which combines the functions of rectification, voltage step-down, and isolation into a single unit, offering advantages in terms of energy conversion efficiency, installation cost reduction, and compact size [9, 17]. Each charger connects to the dc bus through an isolated dc-dc converter, eliminating individual ac-dc converters. This results in improved system efficiency compared to ac-connected systems. The dc rectified voltage, for both ac and dc-connected stations,

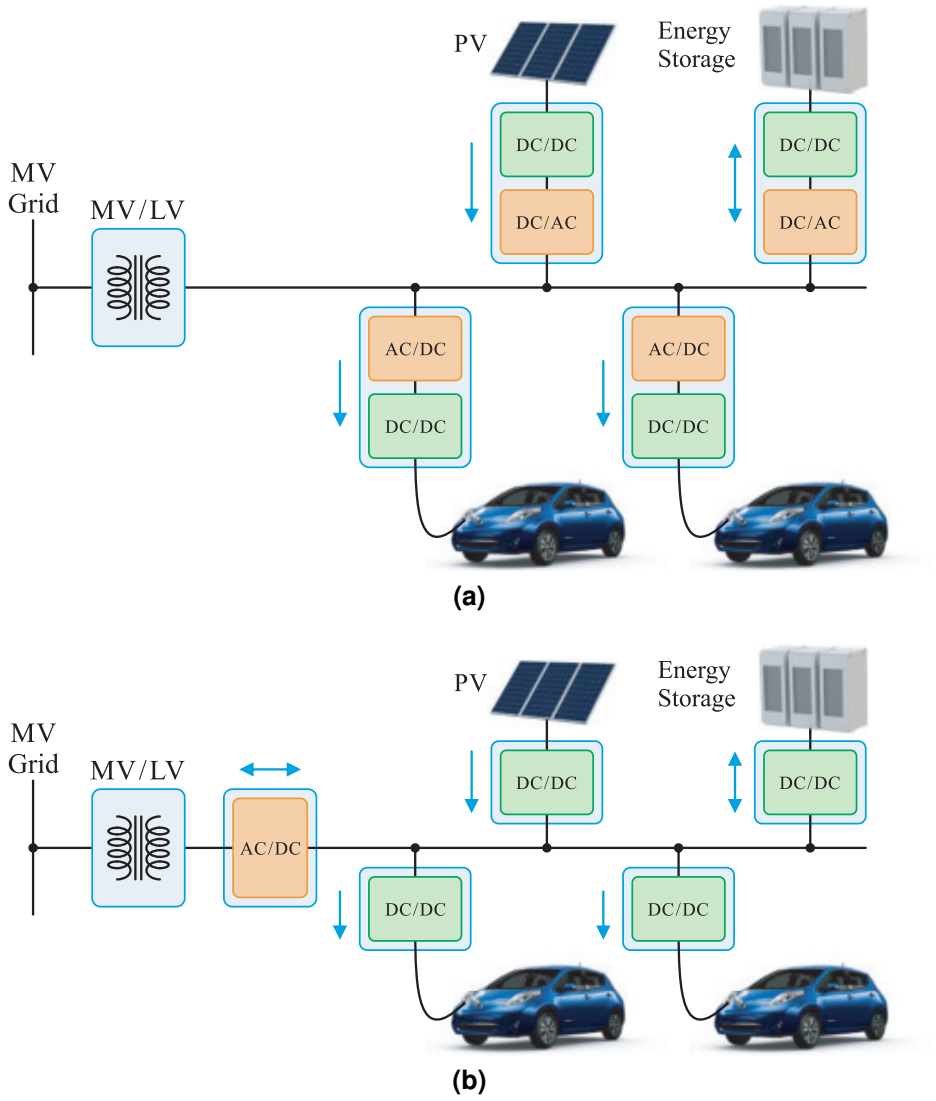


Figure 1.3: Configurations for XFC stations: (a) ac-connected; and (b) dc-connected. Source: [3].

is typically lower than 1000 V, in compliance with standards [11, 16, 17]. However, the dc-connected stations faces challenges related to dc protection and metering, as there are no established standards for protection coordination and certified dc metering [3, 11, 17]. For these reasons and for the existing industrial power electronics knowledge and resources, ac-connected XFC stations remains the mainstream solution for now and the near future.

Considering the ac-connected XFC in Fig. 1.3b, it consists of two conversion stages. The first stage involves ac-dc rectification with a power factor correction (PFC), ensuring high power factor. Here, three-phase input ac voltage, usually up to 480 V, is transformed into an intermediate dc voltage of approximately 800 V [3,15]. Common topologies for this

stage include the three-phase Vienna rectifier, the three-phase neutral point clamped (NPC) rectifier, the three-phase buck, and the three-phase flying capacitor rectifier [3, 11, 15]. The second stage, the dc-dc converter, converts the intermediate dc voltage into a regulated dc voltage suitable for EV charging. Common topologies for this stage include LLC, dual active bridge (DAB), resonant DAB, phase-shift full-bridge (PSFB) converter, and interleaved buck [3,11,15]. The galvanic isolation of the single EV charger is typically achieved within the dc-dc converter stage by employing a high-frequency transformer. These transformers operate at a higher frequency, approximately 50 - $300\,\mathrm{kHz}$, compared to the line frequency, significantly reducing the overall system volume, and are the more commonly adopted solution in practice [15].

In the design of XFCs, modular configurations are commonly employed, in the ac-dc stage and, especially, in the dc-dc isolated conversion stage. Modularity is adopted due to several advantages, including scalability, upgradability, reduced component voltage and current stresses, compatibility with a wide range of EV voltage levels, high efficiency over a broad operation range, simplified cooling, the ability to reconfigure unit connections to achieve a broader output voltage/load range and the ability to fully utilize charging power capacity for multiple EVs with proper control [3, 11]. Modular designs accommodate the varying voltage levels of different EV models, such as those listed in Table 1.2, which may have $400\,\mathrm{V}$ or $800\,\mathrm{V}$ systems, allowing the XFC to provide output voltages ranging from $200\,\mathrm{V}$ to $1000\,\mathrm{V}$ through proper control strategies [3]. These strategies typically consist in the series or parallel connection of several modules, depending on the battery voltage system and required charging power. Fig. 1.4 shows an example of XFC with specifications in Table 1.1 and made of twelve dc-dc modules. It can supply up to four charging point with an overall maximum power of $600\,\mathrm{kW}$. It employs reconfiguration switching matrices after the dc-dc stage to allocate power to specific charging units, enabling simultaneous charging of multiple EVs, also with different battery voltage system.

Remarkably, the dc-dc converter accomplishes the task of constant-current (CC) and constant-voltage (CV) charging of the battery. Key characteristics of the dc-dc converter include high efficiency, high-frequency operation, high power density, low output voltage ripple, soft switching capabilities, stable voltage regulation, and a wide range of output

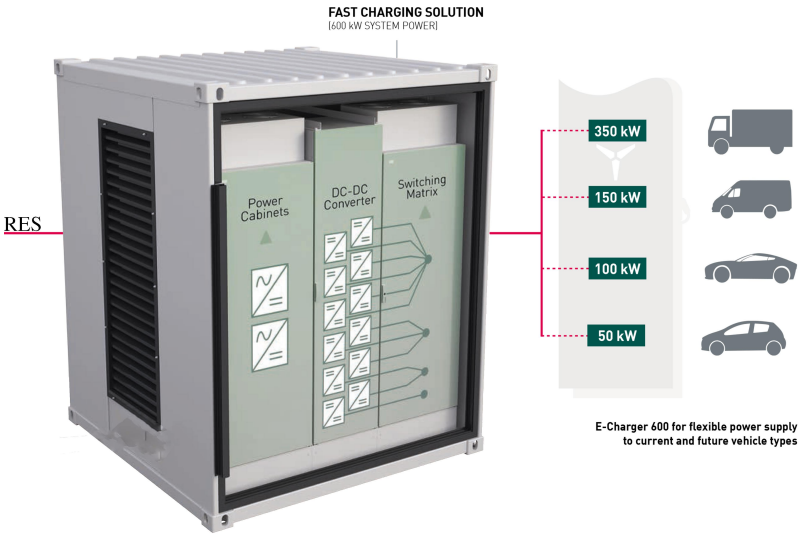


Figure 1.4: Example of XFC. Modular structure can accommodate varying voltage levels of different EV models and several charging points. Source: [21].

voltage [15]. *It is worth noting that this dissertation only focuses on the converter-level challenges, in particular on the efficiency performances of the dc-dc power stage.* The ac-dc converter architectures and the integration of fast-charging stations into the grid are not discussed herein.

1.2 Investigated Aspects and Contributions

The main objective of this dissertation is to compare, analyze, design, and experimentally evaluate dc-dc converter topologies suitable for XFC in EV applications. The dc-dc converter module should feature several pivotal attributes, including superior efficiency performances for a wide output voltage range compatible with EVs battery systems, high-frequency operation, remarkable power density, minimal output voltage fluctuations, soft-switching operation, and the possibility to adapt the output range to both $400\,\mathrm{V}$ and $800\,\mathrm{V}$ battery systems. In particular, this research takes into account the demanding criteria for achieving high efficiency. To address this, cutting-edge wide-bandgap (WBG) semiconductor devices, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), are incorporated into the investigations within the dissertation.

The research contributions of this dissertation can be categorized in the following points:

- **Converter modeling and analysis.** State-of-the-art dc-dc converter suitable for EV charging applications are discussed and investigated. The literature predominantly features the adoption of resonant LLC-like converters, despite their significant efficiency drawbacks. To address this issue, a closer examination is conducted regarding the efficacy of multi-stage LLC-based dc-dc converter topologies. Comprehensive models for the constituent components of these converters, encompassing semiconductors, capacitors, inductors, and transformers, are provided. These models facilitate in-depth simulations to assess the performance of various topologies. The study includes a detailed comparative analysis, focusing on efficiency performance and a breakdown of losses, thereby comparing the selected two-stage topologies with the LLC converter. The aim of this analysis is to highlight both the advantages and limitations of these topological solutions.

- **Converter design and prototyping.** A comprehensive design procedure is outlined for two promising topologies, specifically emphasizing the transformer design process, for their experimental validation. Additionally, practical design aspects of experimental dc-dc converter modules are detailed. A calorimetric method is proposed to evaluate efficiency performance and loss distribution. This method provides a means of assessing the converter's efficiency and identifying the breakdown of losses. The two promising topologies, between those considered, are subjected to experimental investigations and a promising solution is identified.

- **Converter on-line optimization.** A model-free on-line search method, free from complex modeling requirements, is introduced in this study. This approach is then employed to explore and maximize the efficiency performances of the most promising dc-dc converter solution between the considered topologies, and suitable for EV charging applications.

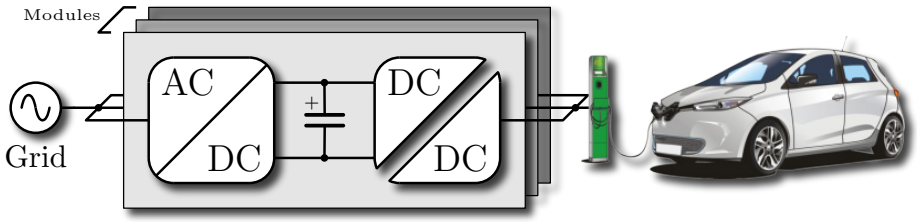


Figure 1.5: Typical EV XFC architecture, consisting of several converter modules in parallel.

1.3 Specifications and Considered Architecture

The considered XFC architecture consists of two converter stages, as shown in Fig. 1.5. *It's important to note that this dissertation primarily focuses on evaluating the efficiency of the isolated dc-dc power stage.* The discussion here does not encompass the ac-dc converter architectures or the integration of fast-charging stations into the grid. The isolated dc-dc converter provides the galvanic isolation from the main distribution grid and regulates the charging process by controlling the output voltage and current.

Given the power requirements of XFC, introduced in Sect. 1.1, many manufacturers, as listed in Table 1.1, have embraced *modular designs*. These involve parallel configurations of multiple converter units, each rated at a fraction of the total power. These modules typically range from 10 to $75\,\mathrm{kW}$ [17]. This modular approach offers several advantages, including simplified design of magnetic components, the use of discrete semiconductor devices without the need for paralleling, and the ability to deactivate one or more modules during light load operation. These factors collectively contribute to higher efficiency across the entire charging range.

Additionally, the *XFC must support a broad output voltage range*, typically spanning from 250 to $1000\,\mathrm{V}$, to accommodate both $400\,\mathrm{V}$ and $800\,\mathrm{V}$ battery systems. This voltage range translates into 250 - $500\,\mathrm{V}$ and 500 - $1000\,\mathrm{V}$, respectively [11, 18]. Leveraging the modularity of the isolated dc-dc stage, reconfigurable series/parallel modules with output voltages within the range of 250 - $500\,\mathrm{V}$ can effectively serve both $400\,\mathrm{V}$ and $800\,\mathrm{V}$ battery systems. This architecture, as introduced in Sect. 1.1.3, is already adopted in the industry and substantially narrows the charger's required output voltage range. Consequently, it significantly enhances the achievable converter performance.

Table 1.4: Isolated dc-dc converter module specifications.

Parameter	Symbol	Value	
Input voltage	V_g	800	V
Output voltage	V_o	250 - 500	V
Nominal output voltage	V_o^{nom}	400	V
Maximum output current	I_o^{max}	25	A
Nominal power	P_o^{nom}	10	kW
Targeted efficiency	η	> 98.5	%

The research efforts detailed in this dissertation, as introduced in Sect. 1.2, have been substantiated through the investigation of a demonstrative dc-dc conversion module. This module is designed with a power rating of $10\,\mathrm{kW}$, featuring a nominal input voltage of $800\,\mathrm{V}$, and an adjustable output voltage from $250\,\mathrm{V}$ to $500\,\mathrm{V}$. These parameters are outlined in Table 1.4. The input voltage is assumed provided by a front-end three-phase power-factor-correction stage.

Remarkably, *the primary objective is to attain an efficiency exceeding* 98.5% *across a wide range of output voltages.* This target aims to compete with or even surpass the efficiency performances of commercially available EV XFC systems listed in Table 1.1.

1.4 Dissertation Outline

The dissertation consists of seven chapters, followed by a concluding chapter, which are summarized as follows:

- **Chapter 2** provides an overview of dc-dc converter topologies suitable for EV fast charging systems. Resonant converters, like the LLC and CLLC, are discussed, highlighting their efficiency limitations outside the resonant operation. To address this issue, the chapter explores multi-stage configurations that include resonant converters to improve efficiency. It also introduces new multi-stage topologies designed for EV applications, setting the stage for a detailed comparison in Ch. 4 to identify the optimal dc-dc converter topology for efficient EV fast charging systems.

- **Chapter 3** introduces essential loss models that will be implemented in the PLECS®

circuital simulation environment. These models are crucial for estimating losses in various converter topologies, particularly the multi-stage configurations discussed in Ch. 2. Implementing these loss models enables the selection of the most suitable topology among those introduced. Additionally, these models allow for a detailed analysis of loss distribution within each topology, helping identify bottlenecks. This information can guide targeted modifications to enhance overall efficiency.

- **Chapter 4** conducts a simulation-based comparison of multi-stage dc-dc converter topologies introduced in Ch. 2, tailored for EV fast charging systems. Simulation models from Ch. 3, implemented using PLECS®+ Simulink® and MATLAB®, are utilized. Design parameters target an EV battery pack with voltage and power requirements as introduced in Sect. 1.3. The goal is to comprehensively assess efficiency and identify the optimal converter topology for EV charging. Promising solutions are further investigated experimentally in Ch. 5 and Ch. 6.

- **Chapter 5** presents a detailed analysis and experimental validation of the proposed buck-boost LLC (BB-LLC) converter, introduced in Ch. 2 and evaluated through simulations in Ch. 4. The BB-LLC is a two-stage isolated dc-dc converter featuring a first pre-regulation stage and a second LLC stage, integrated with the first. The chapter explores the converter's structure, the operational characteristics and experimental results on a $5\text{-}\,\mathrm{kW}$ module prototype. By combining theoretical analysis with practical validation, this chapter aims to provide a comprehensive understanding of the BB-LLC converter's performance, highlighting also the main drawbacks in light-load conditions and maximum voltage region.

- **Chapter 6** presents the analysis and experimental validation of the proposed CLLC + twin-bus buck (TBB), introduced in Ch. 2 and previously evaluated through simulations in Ch. 4. The proposed structure is a two-stage isolated dc-dc converter featuring a first CLLC stage and a second buck post-regulation stage. The chapter covers the solution in detail, including modeling, analyses, design considerations for key circuit components, and modulation techniques. Experimental results are presented based on a converter module prototype rated at $10\,\mathrm{kW}$, with input and output voltages

aligned with the specifications introduced in Sect. 1.3 for the considered application. The proposed solution shows superior efficiency performances, contributing to the development of efficient two-stage EV charging solutions.

- **Chapter 7** introduces an extremum seeking control (ESC) technique to determine the optimal operating points of the TBB converter discussed in Ch. 6. Traditional off-line optimization techniques face limitations due to challenges in precisely modeling converter behavior and their dependence on specific operating points. To overcome these limitations, this chapter explores a model-free on-line search method based on the ESC technique. This method is applied to find the optimal switching frequency of the TBB converter stage. The chapter concludes by verifying the effectiveness of this search technique applied to the TBB prototype presented in Ch. 6.

- **Chapter 8** provides a comprehensive summary of the findings and contributions presented throughout the dissertation. At the end, the dissertation's conclusions emphasize the importance of high efficiency dc-dc converter topologies to meet the growing demand for fast and efficient EV charging, contributing to a more sustainable and environmentally friendly transportation system.

1.5 List of Publications

The publications developed during my Ph.D. have been the result of several projects and activities. In the following, the publications are reported in chronological order.

Related to the dissertation core topic:

- **N. Zanatta**, T. Caldognetto, G. Spiazzi, and P. Mattavelli, "A two-stage isolated resonant DC-DC converter for wide voltage range operation," in *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*. Kiel, Germany: IEEE, Sep. 2021, pp. 1–6.

- **N. Zanatta**, T. Caldognetto, G. Spiazzi, and P. Mattavelli, "Analysis and performance evaluation of a two-stage resonant converter for wide voltage range operation," in

2022 IEEE Applied Power Electronics Conference and Exposition (APEC). IEEE, mar 2022.

- **N. Zanatta**, T. Caldognetto, D. Biadene, G. Spiazzi, and P. Mattavelli, "Analysis and design of a partial-power post-regulator based DC/DC converter for automotive applications," in *2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*. IEEE, jun 2022.

- **N. Zanatta**, T. Caldognetto, D. Biadene, G. Spiazzi, and P. Mattavelli, "Design and implementation of a two-stage resonant converter for wide output range operation," *IEEE Transactions on Industry Applications*, vol. 58, no. 6, pp. 7457–7468, nov 2022.

- **N. Zanatta**, T. Caldognetto, D. Biadene, G. Spiazzi, and P. Mattavelli, "A two-stage twin-bus buck converter for battery charging applications," in *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, mar 2023.

- **N. Zanatta**, T. Caldognetto, D. Biadene, G. Spiazzi, and P. Mattavelli, "A two-stage DC-DC isolated converter for battery-charging applications," *IEEE Open Journal of Power Electronics*, vol. 4, pp. 343–356, apr 2023.

- **N. Zanatta**, T. Caldognetto, D. Biadene, and P. Mattavelli, "Extremum seeking control for the efficiency optimization of a multi-stage converter," in *Proceedings of SIE 2023*. Springer Nature Switzerland, 2023.

Other publications:

- S. Pistollato, **N. Zanatta**, T. Caldognetto, and P. Mattavelli, "A low complexity algorithm for efficiency optimization of dual active bridge converters," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 18–32, 2021.

Chapter 2

DC-DC Converter Topologies for DC Fast-Charging

Chapter in Brief

The chapter gives an overview of the most renown dc-dc converter topologies suitable for EV fast charging systems. Resonant converter topologies are the most widely used. While efficient within their resonant operation, they experience efficiency drops in other operating points still relevant for battery voltage regulation over a wide range. To address this limitation, a strategy involving resonant topologies, such as the LLC or CLLC, operating at peak efficiency using a multi-stage configuration is explored. Multi-stage structures, including a resonant converter as one of the stages, show promising efficiency improvements. The chapter introduces new multi-stage topologies for EV applications. These topologies are extensively compared in the forthcoming Ch. 4, aiming to identify the optimal dc-dc converter topology for efficient and high- performance EV fast charging system.

2.1 Introduction

The demand for EVs has witnessed exponential growth in recent years [6, 12]. This high demand, coupled with the strive for longer ranges and reduced charging time, has propelled the development of next-generation EVs featuring higher battery capacities and charging rates. Consequently, there is an urgent need for advanced EV charging infrastructure capable of delivering higher power outputs at faster rates [15, 22, 23].

Furthermore, new wide-bandgap (WBG) semiconductors has brought about a revolu-

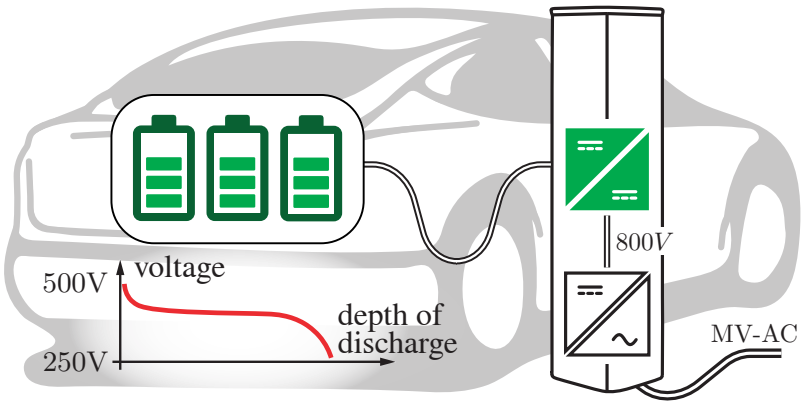
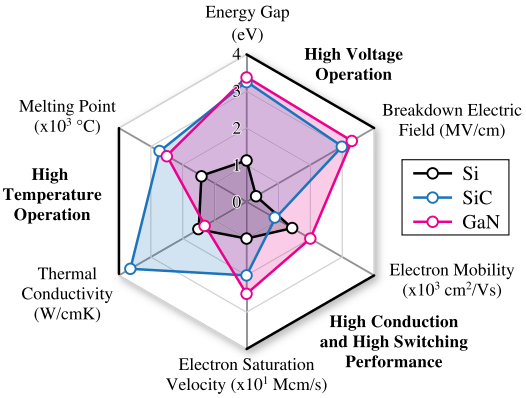


Figure 2.1: EV-charging application.

Parameter	Symbol	Si	SiC	GaN
Band gap	E_g (eV)	1.12	3.26	3.39
Electron mobility	μ_n (cm^2/Vs)	1430	900	2000
Electron saturation vel.	v_n (Mcm/s)	10	20	25
Breakdown el. field	E_b (MV/cm)	0.3	3.0	3.3
Thermal conductivity	λ_{th} (W/cmK)	1.5	3.7	1.3
Melting point	T_m (°C)	1414	2730	2500

(a)



(b)

Figure 2.2: Key material properties of Si, SiC and GaN semiconductors. Source: [24].

tion in power electronics. Silicon Carbide (SiC) and Gallium Nitride (GaN) WBG power switches show unprecedented performance levels, allowing enhanced power density and efficiency. Compared to traditional Silicon (Si)-based counterparts, WBG devices offer advantages such as higher voltage breakdown thresholds, faster switching speeds, and lower on-resistance [24]. This is also visible in Fig. 2.2 where the properties of WBG materials highlight their superior performances. The design of dc-dc power electronics converters for applications of Fig. 2.1 exploits the capabilities offered by these modern semiconductor technologies [23].

As the demand for efficient EV charging solutions grows, the selection of an appropriate converter topology becomes a critical consideration. Different dc-dc converter topologies have been explored to fulfill the requirements of EV fast charging systems. This

chapter delves into an extensive literature review of converter topologies adopted for EV fast-chargers, leading to *the identification of resonant converter topologies as commonly adopted solutions in this domain.* While resonant converter topologies offer compelling advantages, they show a *decrease in efficiency when operating outside the resonant mode.* This condition is necessary to regulate the output voltage across the full battery voltage range, as introduced in Sect. 1.3. To address this limitation, various methods have been proposed, as discussed herein.

Notably, the use of a resonant topology like the LLC or the CLLC operating at peak efficiency condition combined with other conversion stages in a multi-stage configuration, has shown considerable efficiency gains. These advantages are discussed herein.

In addition, *this chapter introduces a new multi-stage dc-dc topology solutions suitable for EV applications* in Fig. 2.1. In Ch. 4 these topologies are compared in detail using the loss models detailed in Ch. 3. The aim is to ascertain the optimal converter topology to meet the demands of efficient and high-performance EV fast charging systems.

Part of the content of this chapter has been published in [25, 26].

2.2 State-of-The-Art Topologies for DC Fast-Charging

DC-DC converters with galvanic isolation are fundamental components of efficient EV battery charging systems in the application in Fig. 1.3. This section provides a comprehensive overview of the state-of-the-art converter topologies employed for EV fast-charging. The selection of an appropriate converter topology is a critical aspect of efficient and reliable EV charging system.

2.2.1 Challenges

DC-DC converters are the essential components of an effective EV battery charging system [9, 18, 27]. Positioned after the ac-dc front-end, these converters serve as a crucial interface to the EV battery. Given that an EV's battery must remain electrically isolated from the ground for safety reasons, as introduced in Sect. 1.1.3, galvanic isolation becomes essential.

Achieving this requirement in a limited space is made possible through the utilization of an isolated dc-dc converter [11].

Several topologies are highlighted in the literature for their merits in terms of efficiency and power density, including the PSFB and the resonant LLC converter for unidirectional power flow, and the DAB and the resonant CLLC converter for bidirectional power flow [11, 15, 28–32].

The PSFB converter provides zero-voltage switching (ZVS) turn-on capability for enhanced efficiency. Nonetheless, it suffers from challenges such as high turn-off losses in active switches, elevated diode losses, and the potential for significant ringing due to resonances involving the transformer leakage inductance and parasitic capacitances [11]. A current-fed variant mitigates overshoots but introduces load-dependent ZVS. Auxiliary circuits, as in [33], have been suggested to sustain ZVS across varying loads. However, achieving ZVS under light-load conditions remains difficult, and overall efficiency may be constrained during wide output voltage variations.

The DAB converter offers advantages such as high power density, efficiency, and buck-boost capabilities. It controls the power flow through the transformer leakage inductance using the phase-shift control. Various modulation schemes have been explored in the literature, including the triple-phase-shift (TPS) aimed at handling wider voltage and power ranges [31]. However, these strategies come with trade-offs and added complexity. The DAB converter inherently generates high reactive currents to achieve ZVS conditions, particularly in scenarios involving wide output voltage ranges and in light-load conditions, leading to increased losses.

The resonant LLC converter, depicted in Fig. 2.3, is a widely used topology for various applications due to its simple structure and efficient power conversion. This converter offers the advantage of inherent ZVS and zero-current switching (ZCS) operations for the primary-side and secondary-side switches, respectively [30, 34, 35]. In this topology, output voltage regulation is commonly obtained through frequency modulation that modifies the resonant tank's impedance ratio. The LLC converter exploits transformer magnetizing current for ZVS turn-on, resulting in very low turn-on, turn-off and transformer losses [11]. However, performance significantly degrades when input or output voltages deviate from

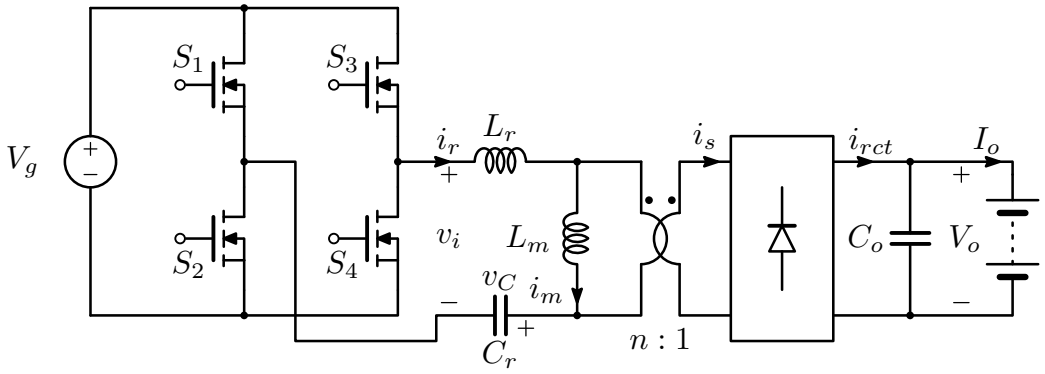


Figure 2.3: LLC resonant converter.

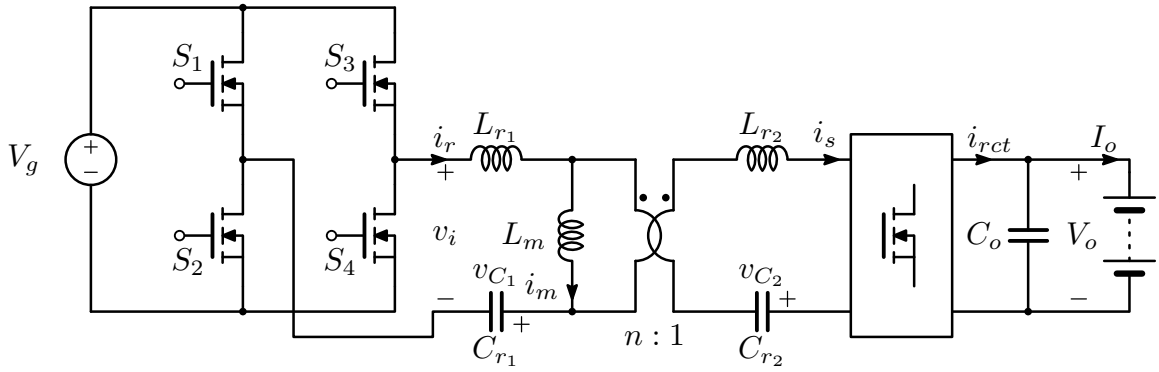


Figure 2.4: CLLC resonant converter.

the near-resonance operation [11, 30, 36, 37]. While achieving high efficiency with a fixed input-to-output voltage ratio, it encounters challenges related to voltage regulation at light loads and in maintaining ZVS over a wide output range, impacting efficiency [11]. Conditions that impede near-resonance operation for classical LLC converters are often found in the considered application in Fig. 2.1, where battery state of charge variations due to typical mission profiles may bring to wide ranges of operating voltages [11, 12, 15, 38, 39].

A bidirectional variant of the LLC converter is the CLLC converter, as illustrated in Fig. 2.4. It offers symmetric voltage gain characteristics in both power flow directions, which reduces control complexity as compared to the DAB converter [31]. Additionally, its resonant capacitors distributed on both sides of the transformer alleviate voltage as stress compared to the LLC converter, and, due to its smaller leakage inductance requirement, it exhibits reduced reactive power circulation [11]. Although it shares similarities with the LLC converter, the CLLC converter faces similar design trade-offs concerning ZVS

conditions and efficiency degradation within a wide range of voltage and power levels.

Compared to PSFB and DAB converters, these resonant topologies offer distinct advantages, yet some disadvantages persist. They exhibit inherent ZVS conditions over a wide range, low reactive currents, and minimal magnetic losses. However, their controllability can be limited within a broad output range, and efficiency drops away from resonance. On the other hand, PSFB and DAB converters feature simpler control and wide operational range, yet they entail inherent reactive currents, especially pronounced in light-load conditions to achieve ZVS, as well as high turn-off and diode losses. Despite these challenges, resonant LLC and CLLC converters remain compelling options due to their inherent strengths. For these reasons, *this dissertation focuses on these resonant topologies and methods for enhancing their efficiency.* Their potential to enhance efficiency in XFC applications serves as the motivation for a thorough exploration of efficiency improvement strategies.

2.2.2 Literature Overview

This section provides a review of the main dc-dc converter topologies suitable for EV fast charging applications, with a particular focus on addressing the challenges related to the aforementioned resonant converter topologies.

Solutions to Overcome Limitations of Frequency-Modulated Resonant Converters. Numerous approaches and methods to overcome the limitations of frequency-modulated resonant converters are reported in the literature [26, 30, 37]. The most relevant methods are summarized in the following.

Solutions include variants in the conversion circuits related to the primary-side [40–42] or the secondary-side [43–47], the resonant tank [48, 48–50], the application of strategies like the partial-power processing (PPP) [9, 30, 51–59], and the design of structures using multiple stages of conversion [26, 60–62].

Table 2.1 summarizes some relevant converter structures for EV fast-charging applications. For each approach, the table includes the core topology and the related class (Cl.): Cl. 0 represents classic topologies (i.e., without topological variants); Cl. 1 represents

Cl.	**Ref.**	**Topol.**	**ac-FE**	V_{in}	V_{out}	P_{rated}	$\eta_{\max}$	**S/D/T/I***	**Peculiarities**
0	[28]	HB-CLLC	no	500 V	200 - 420 V	1 kW	96.5% (0.6 kW, 300 V-out)	4/0/1/2	Bidirectional operation, limited controllability under wide V_{out}.
0	[36]	LLC	no	380 - 420 V	400 V	6.6 kW	98% (3 kW, 390 V-in)	4/4/1/0	High η, wide variation of f_s, narrow V_{in}, fixed V_{out}, η drops far from resonance.
1	[44]	FB/HB-LLC + VD	no	400 V	100 - 400 V	2 kW	96.36% (0.5 kW, 200 V-out)	6/4/1/0	Wide controllable V_{out}, high η over a wide load range.
3	[63]	sw. tank	no	200 - 400 V	1200 V	4 kW	97.71% (4 kW, 350 V-in)	22/0/0/6	Low volume, no galvanic isolation.
0	[64]	PSFB	no	700 - 800 V	350 - 700 V	20 kW	98.9% (13 kW, 700 V-in, 686 V-out)	4/4/1/1	High η, hard switching operated, high magnetics volumes, low sw. frequency.
0	[10]	LLC	yes	7 kV	400 V	350 kW	98.6% (350 kW, 400 V-out)	6/0/1/1	10 kV SiC devices, 4.16 kV ac grid input, limited controllability under wide V_{out}.

3	[56]	CLLC + buck	no	750 V	314 - 450 V	18 kW	98.8% (18 kW, 375 V-out)	20/0/2/3	High η, power density and component count.
1	[39]	interl. LLC	no	390 V	230 - 440 V	1.3 kW	97.31% (1.3 kW, 440 V-out)	6/6/2/0	Limited V_{out} range.
4	[60]	ISOP boost + LLC	no	$1-2$ kV	700 V	12 kW	93.7% (12 kW, 1.2 kV-in)	5/5/1/1	Modularity, high pre-regulator losses.
1	[42]	LLC	no	160 - 320 V	400 V	1 kW	95.2% (1 kW, 160 V-in)	4/4/2/1	Wide V_{in}, simple control, fixed V_{out}.
0	[65]	CLLC	no	400 V	250 - 450 V	1 kW	97.9% (1 kW, 325 V-out)	4/0/1/2	Wide V_{out}, low η far from resonance.
1	[41]	interl. LLC	no	390 V	10 - 420 V	1 kW	98.1% (0.82 kW, 420 V-out)	4/4/2/0	Very wide V_{out}, limited η far from nominal conditions.
1	[45]	LLC + VQ	no	390 V	250 - 420 V	1.3 kW	93.94% (0.95 kW, 420 V-out)	5/6/1/1	Wide V_{out}, limited η.

0	[66]	LLC	yes	380 - 660 V	200 - 500 V	6.6 kW	98% (6.6 kW, 440 V-out)	8/0/1/1	Bidirectional, low voltage-gain of the dc-dc stage, 220 V ac input.
2	[48]	LLC with adj. transf.	no	390 V	126 - 420 V	1 kW	97.18% (0.7 kW, 420 V-out)	8/6/1/1	Wide V_{out}, smooth transitions without transients.
0	[23]	CLLLC	yes	650 - 900 V	214 - 413 V	11 kW	98.75% (11 kW, 792 V-in, 330 V-out)	8/0/2/2	Bidir., 380 V input PFC for voltage regulation, low η at light-load.
1	[67]	active NPC DAB	no	10 kV	700 V	30 kW	99.1% (10 kW, 700 V-out)	10/0/1/1	High η and power density, fixed conversion ratio, careful layout and integrated modules required.
4	[62]	3-ph. CLLC + buck	no	850 V	200 - 800 V	12.5 kW	97.72% (12.5 kW, 800 V-out)	20/0/3/4	Ultra wide V_{out} for 400 and 800 V battery systems, low η over the wide range, high component count.
0	[22]	interl. buck	yes	900 V	200 - 650 V	22 kW	99.51% (22 kW, 200 V-out)	6/0/0/6	Very high η, no galvanic isolation, 480 V ac input, low power density.

3	[30]	3-port CLLC + PPP	no	388 - 412 V	250 - 450 V	2.3 kW	98% (2.3 kW, 450 V-out)	8/0/1/1	PPP, with low-voltage devices, and limited overall conduction losses, high component count and complexity.
3	[58]	2-level + PPP	no	1500 V	630 - 900 V	50 kW	NA**	14/8/2/4	Modularity, utilization of low voltage semiconductors.
0	[68]	buck-boost	yes	150 V	48 - 450 V	1.5 kW	95.6% (1.5 kW, 110 V-in ac, 250 V-out)	6/0/0/2	Bidir., non-isolated, limited η, 85-265 V ac input.
0	[69]	PSFB	yes	400 V	330 V	3.3 kW	97.2% (3.3 kW, 330 V-out)	4/4/1/1	On-board charger, 230 V ac input, fixed V_{out}.
1	[47]	res. LCL-T	no	800 V	150 - 500 V, 500 - 950 V	6.6 kW	98.2% (6.6 kW, 580 V-out)	8/0/1/2	Wide V_{out}, reconfig. rect., phase-shift modulation, res. network for η optimization during CC charging phase.

* S/D/T/I: number of active switches, diodes, transformers, and inductors, respectively.

** NA: not available.

Table 2.1: Relevant converter structures for EV-charging applications.

topologies with modifications in the primary or secondary-side structures; Cl. 2 represents modifications in the resonant tank; Cl. 3 represents topologies that adopt additional PPP stages; and Cl. 4 represents multi-stage topologies. The table also reports, for each topology: the presence of an ac front-end (ac-FE) stage, the input voltage of the dc stage V_{in} and its output voltage V_{out}, the rated power P_{rated}, the peak efficiency $\eta_{\max}$, and the number of active switches, diodes, transformers, and inductors used in the dc-dc stage, indicated by the symbols S, D, T, and I, respectively.

Approaches Considering Modifications in the Primary or Secondary-Side Structures. An LLC structure reconfigurable for half-bridge or full-bridge operation combined with auxiliary switches at secondary side is proposed in [44]. Such a solution is able to cover a very wide range of output voltages, but additional switches and dedicated modulation capable of smoothly transit between the configurations are required. Similarly, [45] proposes a full-bridge LLC working at resonance frequency with a voltage quadrupler and an auxiliary switch at the output. Such a converter shows limited efficiency improvements, due to the high conduction loss of the output stage. In [41], an interleaved LLC is proposed with series-connected secondary sides and shared rectifier. Such a solution adopts phase-shift modulation between the two parallel LLC working at resonance frequency. It shows good performance at close-to-zero phase-shift but the efficiency decreases rapidly when far from the nominal conditions. Similarly, [70] describes an interleaved LLC with reconfigurable voltage multiplying rectifier that changes configuration from voltage doubler to voltage quadrupler. Such an approach adopts passive rectification and does not require additional metal-oxide-semiconductor field-effect transistors (MOSFETs), unlike conventional approaches as [39, 44]. Smooth transitions between the two configurations are achieved, however a phase-shift control must be introduced in order to mitigate current and voltage stresses on the components. Additionally the two parallel-connected LLC converters can suffer from unbalanced power sharing due to asymmetries in the two resonant tanks, implying the adoption of additional tricks in the control strategy of the converter. An interleaved LLC is proposed in [39], achieving voltage regulation in a wide range similar. The converter can achieve ZVS for the primary switches regardless of the operating condi-

tion, however the component count is doubled and the efficiency drops when operating far from nominal condition.

Approaches Considering Modifications in the Resonant Tank Structure. Converters that adopt reconfigurable structures as described, for example, in [39,40,44,46,49], can obtain wide voltage gain, but achieving smooth transitions between the different configurations may be difficult to cope with. A careful design of the additional resonant tank is required to limit the related losses and preserve overall efficiency.

Approaches Considering Partial-Power Processing Additional Stages. Solutions implementing PPP strategies show potential advantages to accommodate wide operating voltage ranges and high efficiency, at the cost of a high components number and complex design and modulation [51, 55, 58].

For example, a solution using input-parallel output-series (IPOS) PPP and resonant CLLC-type dc-transformer (DCX) is proposed in [56], considering a narrow range of operating voltages. The topology is characterized by low switching losses on the output switches, but it requires an active rectification with very low conduction losses and a relatively high number of devices.

Approaches Implementing Multiple Stages. An effective method to overcome the limitations of the frequency-modulated LLC converter is to keep working the LLC stage at its optimal operating point (i.e., DCX operation) [34, 35] and employ an additional conversion stage to regulate the output voltage, which results in multi-stage structures [60–62, 71, 72]. In these structures, the isolated DCX-LLC resonant converter, widely used in applications including power supply, energy storage, data centers, and solid-state transformers, is often employed because it can interface with galvanic isolation two dc buses involving very limited power losses [34, 35]. These multi-stage topologies are favorable to accommodate wide operating voltage ranges with very high efficiencies; however, more components are required, which might reduce the overall power density.

The integration of power switches in multi-stage structures are studied in several paper to address these disadvantages [26, 73–75]. The half-bridge LLC converter could be inte-

grated with a boost structure by sharing the switches and regulating the voltage via the duty cycle. Compared with two-stage topologies, these can reduce the number of switching devices. Input voltage regulation is a practical solution in case wide input and output voltage regulation is needed, featuring simplicity, low component count, and adaptation to resonant or quasi-resonant stages with optimal efficiency and switching frequency [38, 60, 71, 72]. In [60], a two-stage structure for an input-series output-parallel modular power supply is proposed. With an input voltage $\leq 1\,\mathrm{kV}$ for each module, a solution with a buck pre-regulator and an LLC converter operated as DCX is adopted. [76] proposes an interleaved CLLC with buck-boost pre-regulation. The converter shows good efficiency over a wide range of input and output voltages, with the disadvantage of no galvanic isolation and poor efficiency at light-load.

In addition, several configurations of two-stage dc-dc converters exploiting a voltage post-regulator are described in the literature [57, 77, 78]. This approach inherits all the advantages of the multi-stage approach with pre-regulation and, additionally, it has demonstrated reduced voltage or current stresses in the post-regulator, ensuring the DCX stage operates at its peak efficiency.

Building upon the aforementioned review of relevant literature, it becomes evident that *multi-stage configurations based on resonant converters emerges as a promising solution for investigation.* The aim of this dissertation is to enhance the performance of the LLC resonant dc-dc converter in a wide output-voltage range. To achieve this goal, with the hints taken from the literature, a thorough exploration, analysis, and experimental evaluation of two-stage LLC-based conversion structures is undertaken. Topological solutions are proposed in the subsequent Sect. 2.3, followed by a comprehensive analysis and comparison in Ch. 4. The two most promising solutions are experimentally evaluated in Ch. 5 and Ch. 6.

2.3 Investigated Multi-Stage DC-DC Converter Topologies

Considering the literature overview in the previous Sect. 2.2 provided above, the enhancement of the LLC performance across a wide output-voltage range for EV charging applications is pursued through the exploration of two-stage conversion structures in this

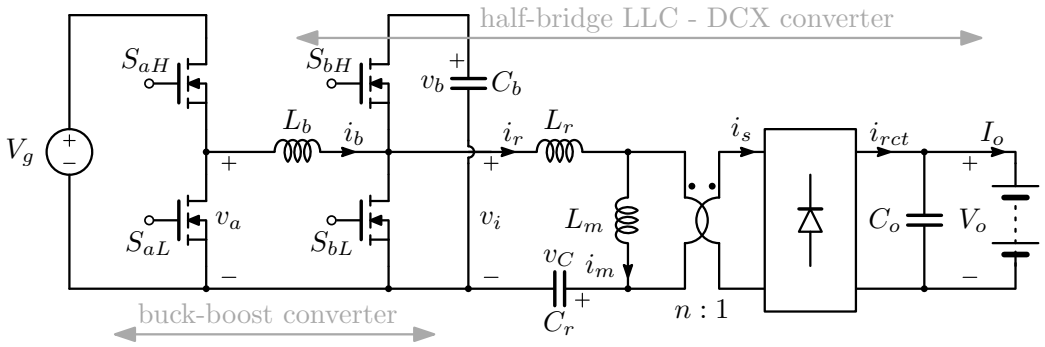


Figure 2.5: Two-stage converter with pre-regulation & DCX-LLC stage.

section. Specifically, three distinct two-stage configurations, two of them with characteristics of PPP architectures, are introduced herein and are considered for investigation in Ch. 4. These topologies are selected for their potential to address the efficiency challenges discussed in Sect. 2.2.2. Furthermore, it is noteworthy to mention that variations and modifications aimed at further refining efficiency enhancements are thoroughly explored in the upcoming comparative Ch. 4. An high overall conversion efficiency over the wide range of operating voltages of application of Fig. 2.1 can be achieved at the cost of a higher number of components. The primary objective is to identify the most promising candidates for achieving optimal performance in the context of multi-stage LLC-based conversion structures for EV charging applications.

2.3.1 Buck-Boost LLC

Input voltage regulation in a two-stage dc-dc structure proves to be a practical solution when wide input and output voltage regulation is necessary. This approach is simple and it offers a reduced component count, and the ability to adapt to resonant stages with optimal efficiency [38, 60, 71, 72]. The proposed structure is shown in Fig. 2.5, where the two stages are highlighted [74, 75]. They are constituted of a pre-regulation stage and a DCX-LLC, employing the LLC converter at its maximum efficiency condition and avoiding the efficiency degradation due to the classical frequency modulation. The topology was studied in [74] considering telecom applications with input voltage range $250\,\mathrm{V}$ - $420\,\mathrm{V}$, output voltage $24\,\mathrm{V}$ and power ratings $750\,\mathrm{W}$. In [75], the potentiality of adopting a phase-shift modulation is not considered to improve the ZVS performances of the topology and the pre-

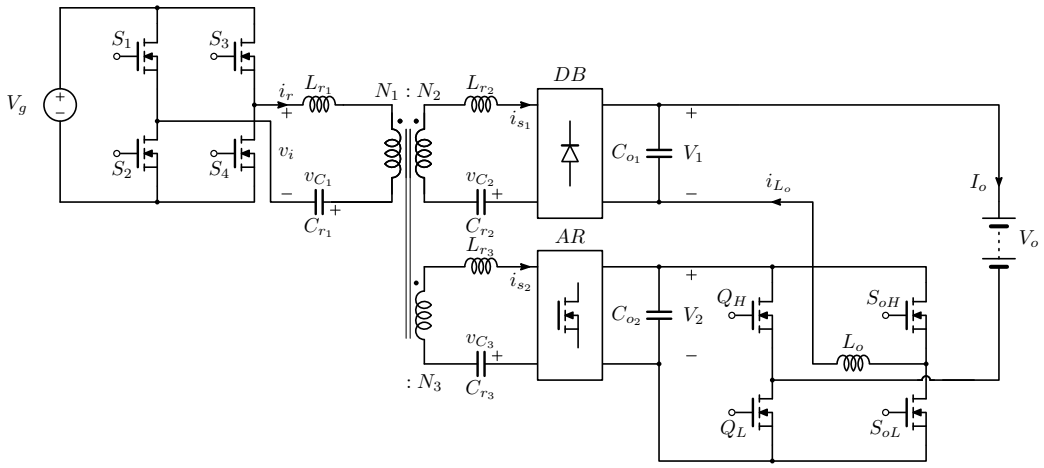


Figure 2.6: Two-stage converter with two-output DCX & PPP post-regulator.

regulator is operated in hard switching at lower switching frequency. Moreover a bulkier capacitor is needed to stabilize the intermediate bus voltage.

The principle of the considered conversion structure in Fig. 2.5 is to operate the second resonant stage at conditions that ensure maximum efficiency, namely, at resonance, and exploit the pre-regulation stage to impose such an optimal operating condition for the second, DCX-LLC stage. The pre-regulation stage can also help in achieving zero-voltage turn-on of the switches that drive the second stage over a wide range of output voltages [11, 38]. Notably, the exploitation of latest wide-bandgap power semiconductors allows to further reduce semiconductor loss [79].

In conclusion, the investigated multi-stage dc-dc converter topology, as presented in Fig. 2.5, demonstrates a promising approach for efficiency improvements in EV charging applications. Analysis of the proposed structure and performance evaluation are explored in Ch. 4, shedding light on its potential benefits as multi-stage dc-dc converter.

2.3.2 CLLC & Partial-Power Post-Regulator

Output voltage regulation within a two-stage dc-dc structure emerges as a compelling solution for EV applications. This approach enables seamless adaptation from the DCX resonant stage, optimized for efficiency, to a subsequent post-regulation stage with reduced voltage or current stresses, a concept well-supported by prior research [38, 56, 60, 71, 72]. Notably, the topology described herein closely aligns with this principle.

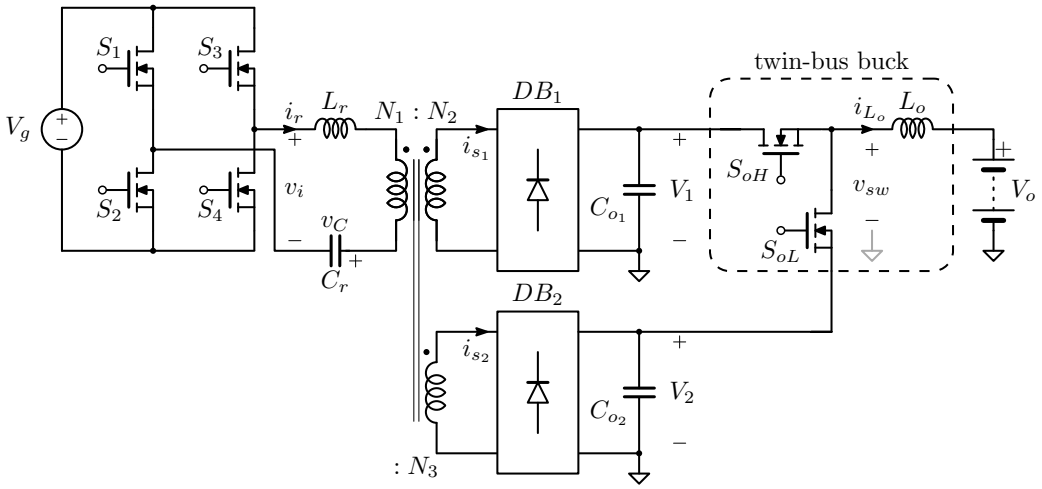


Figure 2.7: Two-stage converter with two-output DCX-LLC & TBB post-regulator.

The proposed structure is shown in Fig. 2.6, where the output of a post-regulator is connected in series with the output of the main resonant converter and the load [56]. It comprises a DCX-CLLC stage and a buck post-regulation stage, employing the CLLC converter at its maximum efficiency condition and avoiding the efficiency degradation due to the classical frequency modulation. A more complex bidirectional and interleaved version of the topology was explored in [56] considering EV applications.

This two-stage structure depicted in Fig. 2.6 also exhibits characteristics akin to IPOS-PPP, where only a fraction of the rated power is processed by the buck post-regulator, thus enhancing overall efficiency. Despite the very low voltage stress in the post-regulator, all the converter output current flows through the series of rectification stages, which may impact the efficiency. This topology's analysis and performance evaluation are presented in the forthcoming Ch. 4, aiming to identify its viability and potential benefits for multi-stage dc-dc converters in EV charging systems.

2.3.3 LLC & Twin-Bus Buck Post-Regulator

To enhance the performance of the LLC resonant dc-dc converter across a wide output-voltage range, a two-stage conversion structure in which the second stage performs the post-regulation of the output voltage represent a promising solution.

The proposed structure is depicted in Fig. 2.7. The post-regulation stage is directly con-

nected to intermediate dc-links (i.e., V_1 and V_2), supplied by an isolation stage based on a resonant LLC-like structure with dual outputs. The underlying principle of this solution is to operate the input isolation stage at peak efficiency and employ the post-regulation stage to perform output voltage regulation with minimal voltage stresses. Operating the second stage with constrained voltage stresses holds the potential for achieving low conversion losses across the extensive range of output voltages relevant to EV battery charging. Remarkably, this converter structure also exhibits characteristics similar to those of PPP solutions, where only a portion of the rated power undergoes processing by the buck post-regulator, thereby augmenting overall efficiency.

With its features, this topology is a promising candidate for addressing the efficiency challenges associated with the dc-dc conversion structures for EV charging applications.

2.4 Summary

In this chapter, an overview of prominent dc-dc converter topologies suitable for EV fast charging systems is presented. Resonant converter topologies are identified as notable candidates due to their inherent advantages, including high efficiency during resonant operation. However, the need for voltage regulation across wide battery voltage ranges poses relevant challenges to avoid undesired efficiency drops outside the resonant operation. To address this limitation, a strategy involving multi-stage configurations, where resonant topologies like the LLC or CLLC operate at their peak efficiency within a two-stage structure, is explored. *The resulting multi-stage configurations demonstrates potential for significant efficiency improvements and power delivery for EV charging applications. Novel multi-stage dc-dc converter topologies for EV applications are introduced.* These topologies are investigated in details in Ch. 4, utilizing loss models described in Ch. 3, to identify the most suitable converter topology for efficient and high-performance EV fast charging systems.

The next Ch. 3 delves into a comprehensive analysis of loss models, which is crucial for accurately evaluating the performance of the introduced converter topologies in terms of efficiency and power loss. The subsequent Ch. 4 provides an in-depth comparative analysis of the various converter topologies, leading to valuable insights into their strengths

and weaknesses for EV fast charging applications. This systematic investigation lays the foundation for the subsequent experimental validation in Ch. 5 and in Ch. 6.

Chapter 3

Loss and Simulation Models

Chapter in Brief

This chapter discusses the key loss models implemented in simulation for the selection of the most suitable multi-stage topology among those introduced in Ch. 2. These loss models allows the estimation of the converters losses, facilitating a detailed breakdown of the losses associated with the components of the various topologies. By analyzing the loss breakdown, it becomes possible to identify components with higher losses and make targeted modifications to the topology, thereby improving overall efficiency.

3.1 Introduction

This chapter provides an overview of the theoretical background of main component modeling, employed to design and estimate the losses of the converter components. The components of a power converter include MOSFETs, diodes, magnetic elements, and capacitors. A proper modelization of these components ensures their optimal selection, avoiding both oversizing and undersizing, and achieving a balanced distribution of losses among all of them. Moreover, the models enable accurate sizing of the volume required for each component, and then for the entire converter. Therefore, loss models play a fundamental role in converter design. Furthermore, the implementation of component models in a simulation environment allows for the estimation of converter component losses, thereby enabling the evaluation of converter efficiency. This approach also facilitates further improvements in the design of individual components and even topological modifications to enhance the

overall converter topology.

The primary objective of this chapter is to identify component models that aid the selection of prominent topology solution and in optimizing the design of the converter elements for the considered application of dc fast-chargers for EV applications. It is important to note that while this chapter focuses on developing component models for design purposes, a comprehensive analysis and modelization focused on component optimization, including efficiency and occupied volume, has not been addressed in this dissertation. Finally, this chapter presents the loss measurement techniques applied for the estimation of the single components losses in the experimental prototypes. These losses measurements enable the estimation of system losses and serve as a means to validate the adopted models during the design phase.

Part of the content of this chapter has been published in [25, 26, 80, 81].

3.2 Main Loss Sources

To introduce the main components contributing to losses in a dc-dc converter for EV battery charging applications, the resonant LLC converter discussed in Ch. 2 is considered next. The following list outlines the primary sources of losses:

- MOSFET losses, encompassing conduction and switching losses;
- Diode losses;
- Inductor losses, encompassing winding and core losses;
- Transformer losses, encompassing winding and core losses;
- Capacitor losses.

It is worth noting that additional loss terms may be considered, such as ac losses in printed circuit board (PCB) traces, which are typically of lower relevance. In the following section, the major loss elements listed above are analyzed.

3.3 Loss Models

The advancement of power electronics is closely linked to the development of power semiconductor devices. These devices have improved over time, offering higher current/voltage ratings and reduced conduction and switching losses, thereby enabling higher switching frequencies. This progress in power semiconductors contributes to achieving higher system efficiencies and lower system volumes, leading to overall higher power densities. Higher switching frequencies offer the advantage of reducing the size of passive components, such as magnetic elements. Magnetic components, like inductors and transformers, currently occupy a significant amount of space in power electronic systems and contribute to substantial losses. The rising switching frequencies of today's systems are leading to the emergence of high-frequency losses that involve all the components of the converter and are difficult to be accurately quantified [82]. Several publications have focused on modeling magnetic components losses [82–92], switches losses [93–97], or capacitor losses [98], recognizing the significance of understanding and accurately characterizing their losses behavior.

Herein, the major loss elements mentioned in the previous Sect. 3.2 are analyzed in detail. *These loss models, specifically designed for implementation in a PLECS®/Simulink® simulation environment, are adopted and utilized in the subsequent chapters for the topology comparisons and components design.*

3.3.1 MOSFETs

Modern GaN and SiC power semiconductors emerges as key enablers for advancements in power electronics, offering improved performance compared to traditional Si semiconductors. The superior switching characteristics of these WBG devices allow for higher operating frequencies and downsizing of passive components in power converters. However, at high frequencies, switching losses become a limiting factor, even for such WBG semiconductors. The accurate determination of switching losses is crucial for optimizing modern power converters, as they typically dominate the loss breakdown in compact converter designs [95, 99].

Conduction Losses

WBG semiconductors offer significantly lower on-resistances, as shown in Fig. 2.2, which allows higher voltage and power levels in power converter designs. To calculate the conduction losses of the switching devices, a simple expression incorporating the on-resistance, $R_{ds(\mathrm{on})}$ and the rms current flowing through the device, $I_{S_1}^{\mathrm{rms}}$, is employed. The expression results as follows:

$$P_{\mathrm{cond}}^{S_1} = R_{ds(\mathrm{on})} I_{S_1}^{\mathrm{rms}2} \tag{3.1}$$

This expression quantifies the dissipated power due to the voltage drop across the device during conduction. The accurate selection of the MOSFET with lowest conduction losses aids in the optimization of power converter designs ensuring efficient operation at higher voltages and power levels. However, it is important to note that simply choosing a device with the lowest on-resistance does not guarantee the lowest overall losses. In fact, devices with lower on-resistances often exhibit higher switching losses [24]. This trade-off is particularly relevant in the context of the increasing trend in switching frequencies: the higher the switching frequency, the greater the switching losses in the devices. Therefore, the optimal choice of a MOSFET device involves carefully estimating both conduction and switching losses to achieve the best trade-off for the considered topologies introduced in Ch. 2. By accurately evaluating and minimizing both types of losses, power converter designs can achieve optimal performance and efficiency.

Switching Losses

Switching losses are a critical issue in power electronic converters, and in general, WBG semiconductors offer lower switching losses compared to traditional silicon devices [24]. The improved figure-of-merit of WBG semiconductors allows higher switching frequencies which allows to reduce the volume of passive components for maximal power density [95, 99]. However, as switching frequency increase the use of modulations capable of minimizing switching losses is of paramount importance. Anyway, it is crucial to identify the conditions under which soft switching can be achieved [95]. By accurately optimizing such a switching conditions, power converter designs can achieve higher efficiency and

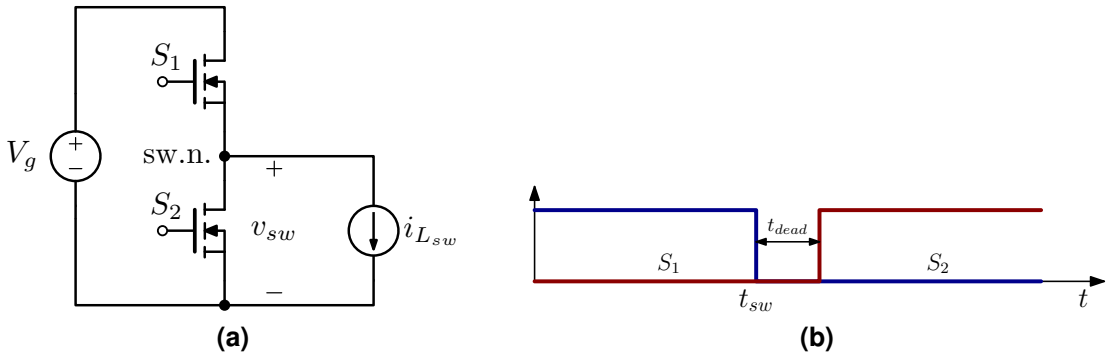


Figure 3.1: (a) Simplified circuit of the switching leg simulated in LTspice® environment; and (b) Gate commands during the commutation.

improved performances. Despite operating under ZVS conditions, WBG devices may still experience losses associated with the energy stored in the drain-source output capacitance (C_{oss}) of the devices. These losses become particularly significant at higher frequencies and voltages, which are common operating conditions for these devices [94, 99]. The causes of these losses have been attributed to various factors, including leakage current through the substrate, trapping in the buffer region stack, and resistive power dissipation in the termination region [94]. Additionally, the estimation of switching losses involves considerations beyond the chosen WBG device and its output capacitance. Surrounding parasitic inductances, such as drain, source, and PCB parasitics, significantly influence the switching losses [99]. The used dead-time, if not modulated, can affect the losses as the conduction angle of the WBG device body diode changes. For a certain operating point, if the dead-time is not sufficient for achieving ZVS, the switching losses increase. On the other hand, if the dead-time is too long, the losses increase due to the body diode losses. Additionally, selecting high gate resistances to limit overshoots can prolong the rise and fall times of the switching device, bringing increased switching losses [99].

For the purposes of this chapter, which focuses on the selection of a suitable simulation model for the evaluation of the converter losses, SPICE models were utilized for the evaluation of the switching losses. Although SPICE models typically rely on small-signal C_{oss} data and may not accurately represent the large-signal behavior and losses, they provide valuable insights into the switching performance of devices and allow the comparison among different devices.

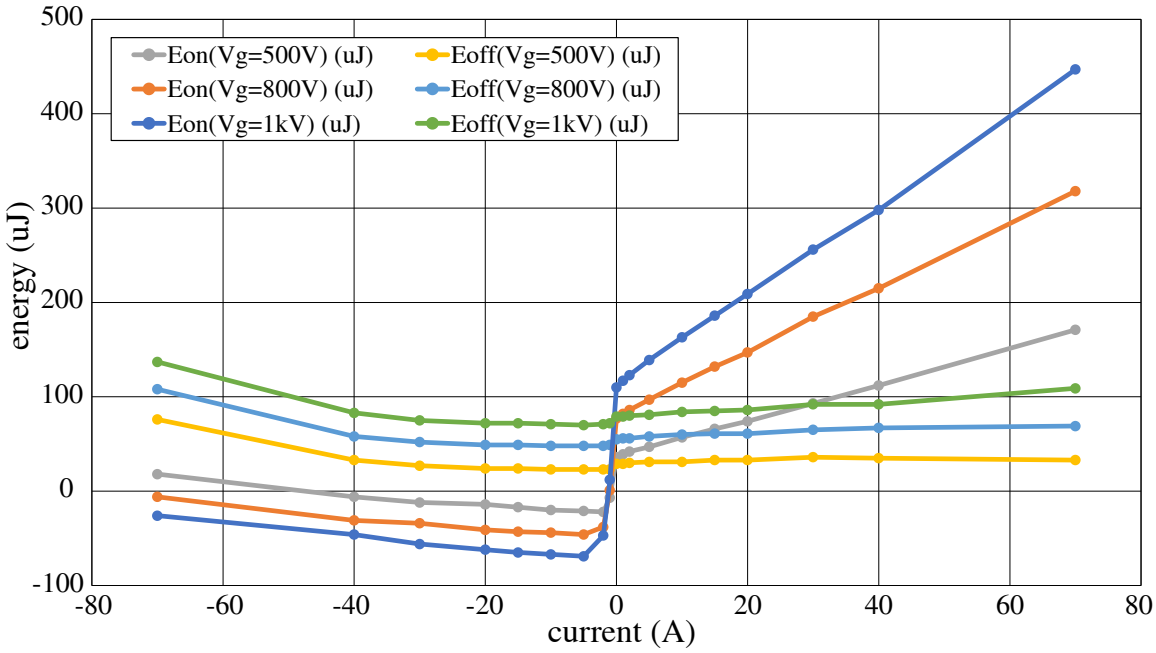


Figure 3.2: Example of turn-on and turn-off energy losses at different dc voltages V_g and different switched currents $i_{L_{sw}}$. Wolfspeed 1.2 kV SiC MOSFET C3M0032120K.

To model the switching losses for evaluating the efficiency of the topologies in Ch. 2, a LTspice® simulation is implemented. A single switching action of a switching leg, as shown in Fig. 3.1, facilitated the assessment of switching losses across the entire range of possible current values. During the switching transition, the equivalent inductance seen from the switching node, sw.n., is treated as a constant current generator with a value equal to the switched current. Gate commands are illustrated in Fig. 3.1b, while the dead-time t_{dead} is kept constant. Gate resistances and parasitic inductances were included in the simulation model to obtain accurate results. Additional details are included in App. A.

In Fig. 3.2, the switching energy losses for the turn-on $E_{on}(V_g)$ and the turn-off $E_{off}(V_g)$ transients are depicted at different switched current values $i_{L_{sw}}$ and dc voltages V_g. These simulation results were obtained using LTspice®, implementing SPICE manufacturer's models of the Wolfspeed SiC MOSFET C3M0032120K, chosen as an example. In the literature, good match between SPICE simulated losses and experimental double-pulse tester (DPT) measures is reported [100, 101].

These results are exploited for evaluating the switching loss in the loss-breakdown comparison of the selected topologies in Ch. 2. To this end, the obtained LTspice® results are

compiled into a lookup table enabling an estimation and analysis of switching losses within the PLECS® simulation environment. The subsequent section shows how these results were implemented in PLECS®/Simulink® environment.

3.3.2 Diodes

Similarly to the MOSFET devices, the high voltage WBG diodes offer promising characteristics, such as lower conduction losses, faster switching speeds, and higher efficiency as compared to traditional Si-based diodes. As a result, they become a key enabler for achieving higher switching frequencies and power densities in modern power converters.

SiC Schottky diodes are chosen due to their fast switching capability, zero reverse recovery current, and minimal reverse recovery charge [102]. Due to the specific characteristics of the power converter topologies analyzed in Ch. 2, which are resonant topologies characterized by ZCS in the rectifying diodes, the diode losses are predominantly associated with conduction losses [39]. This remark is especially important when the topologies operate at resonance, as for the topologies proposed in Ch. 2 (except for the LLC converter, which is frequency-modulated).

The conduction losses of a rectification diode, denoted as P_d, can be estimated by linearizing its forward characteristic. Fig. 3.3c shows an example of forward characteristic of the Wolfspeed SiC Schottky diode C5D50065D [102]. The relation between instantaneous forward current I_F and forward voltage V_F can be represented by a linear model defined by a threshold voltage V_{T_j} and a resistance R_{T_j}. The linearization of such a characteristic yields a temperature-dependent linear model, as shown in Fig. 3.3b, described by the following equation:

$$V_F = V_{T_{25}} + \alpha_V T_j + I_F(R_{T_{25}} + \alpha_R T_j) \tag{3.2}$$

where $V_{T_{25}}$ and $R_{T_{25}}$ are the threshold voltage and resistance at 25°C. T_j represents the device junction temperature and α_V and α_R are parameters provided by the manufacturer [102].

This linear model allows for the estimation of conduction losses in the diode as a function of the forward current and the junction temperature. By incorporating these losses

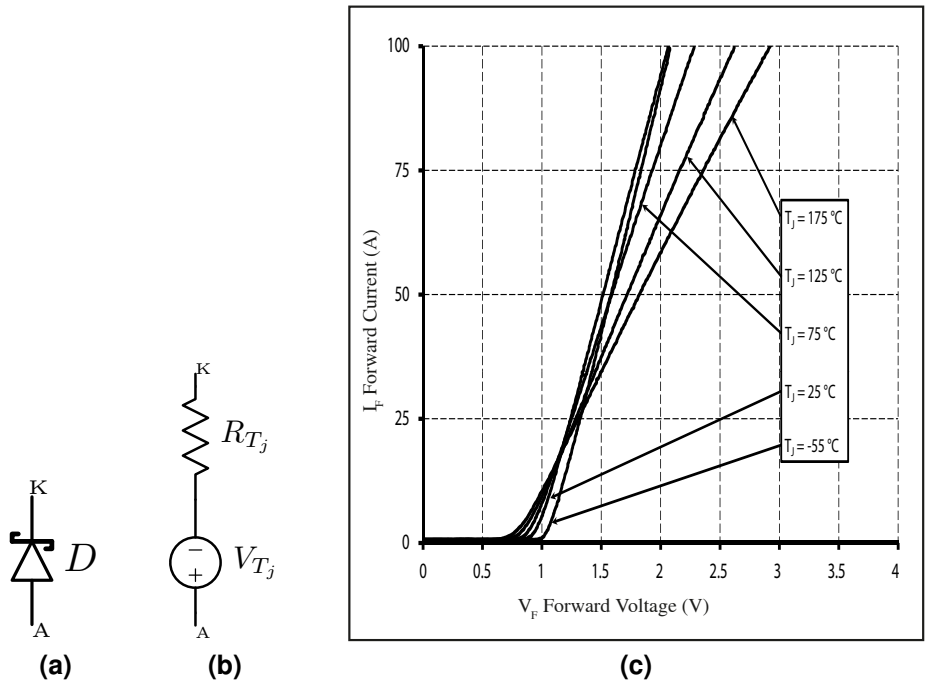


Figure 3.3: (a) Schottky diode symbol; (b) Simplified circuit for the conduction losses estimation; (c) Forward characteristic of the Wolfspeed SiC Schottky diode C5D50065D [102] at different junction temperatures.

into the PLECS® simulation environment, it is possible to obtain valuable insights into the impact of diode behavior on the system's performance.

The DCX operation of the compared topologies in Ch. 2 results in negligible switching losses for the diodes [39]. Therefore, by employing this simplified model, it is possible to estimate the diode losses accurately in the resonant operation of the selected power converter topologies. However, it is essential to note that in the full-bridge LLC (FB-LLC) topology, under operating conditions below resonance, there may be additional contributions from switching losses, which are not considered in the simplified model. Therefore, when analyzing the LLC topology, the obtained estimation of losses may potentially provide an underestimation of the diode losses and an overestimation of the overall efficiency. However, despite this simplification, the focus on conduction losses remains appropriate for the majority of the analyzed operating conditions and considers topologies in Ch. 2. The subsequent section presents how the diode losses are calculated in PLECS® simulation environment, and Ch. 4 provides a comprehensive evaluation of their influence on the

overall efficiency on the selected topologies.

3.3.3 Magnetic Elements

The losses in magnetic elements, such as transformers and inductors, play a significant role in the overall efficiency and power density of power electronic systems. Understanding and accurately characterizing these losses are crucial for developing effective loss models and thermal management strategies. This is especially crucial in the context of the growing trend of increasing switching frequencies, where core losses and winding losses become more pronounced.

The losses in transformers and inductors can be divided into two main categories: core losses and winding losses. The cores used to manufacture high-frequency transformers and inductors are usually made of soft-magnetic materials. Core losses occur within the magnetic core of these components and are mainly attributed to two sources: hysteresis loss and eddy current loss [92]. Hysteresis loss occurs when the magnetic domains within the core material undergo cyclic magnetization and demagnetization, resulting in energy dissipation. On the other hand, eddy current loss are due to the formation of circulating currents within the core material in response to the alternating magnetic field, leading to further energy losses [84, 92, 103]. Winding losses, also referred as copper losses, occur in the windings of the transformer or inductor. These losses are primarily due to the ohmic dc and ac resistances of the windings, resulting in heat generation during the current flow.

Accurate estimation of core losses and winding losses in magnetic elements is paramount for optimizing the design of these components, leading to improved efficiency and thermal behavior in power converter topologies. Different approaches for modeling these losses can be employed, depending on the available information, desired computational effort, or desired degree of accuracy. Efforts to improve the accuracy of these loss models have led to various techniques in the literature, enabling better design and optimization of power electronic systems. Relevant examples can be found in [83, 88, 92, 104].

Herein, core losses and winding losses in magnetic elements are investigated. In particular, some methods in the literature used for their modeling and estimation are discussed,

and a suitable approach for magnetic elements design is proposed. Such an approach allows an efficient design and implementation of transformers and inductors for power converters for fast-charging applications.

Core Loss

The classic and widely used model for core losses estimation is the renown Steinmetz equation, which describes the total core loss under sinusoidal excitation [105]:

$$P^{\text{core}} = K_c f_s^{\alpha} B_{\text{max}}^{\beta} \tag{3.3}$$

where P^{core} is the time-average core loss per unit volume, B_{max} is the peak value of the flux density with sinusoidal excitation at frequency f_s, and K_c, α, and β are constants that can be found from manufacturers' data [92, 103].

However, in power electronics applications, non-sinusoidal excitation under dc bias commonly occurs, making the application of the classic Steinmetz equation limited [88, 92, 103, 103, 104]. To address this drawback and accurately estimate losses for a wider variety of waveforms, different approaches have been developed [84]. These methods for core losses estimation can involve the decomposition of the total loss into several other components (e.g., hysteresis, eddy current and residual losses). But the models of such a components are based on parameters that are not always available and often difficult to extract [103]. Another approach to overcome the limitation of the Steinmetz equation is the improved Generalized Steinmetz Equation (iGSE) [103, 106]. The iGSE is capable of accurately calculating losses of any flux waveform using the Steinmetz parameters, however it neglects the fact that Steinmetz parameters change under changing dc bias condition [103, 104]. Other approaches are based on the calculation of the losses with a loss map based on measurements; but various operating points for different flux densities, frequency, temperature and dc bias must be tested [84]. A further approach in [103] shows the dependency of the Steinmetz parameters on dc pre-magnetization of the soft-magnetic core. It allows to calculate the core losses under dc bias conditions (i.e., typical condition in inductors). In [84] a model that considers relaxation processes when calculating core losses

is proposed. This phenomena is supposed to occur during the short period after switching with winding voltage imposed to zero [84].

The above mentioned approaches are the most accurate core loss models in the literature [88], reported in order of accuracy, but with the drawback of increasing complexity. Despite the limitations of some of these models, they provide valuable insights and enable the design and optimization of magnetic elements for the considered topologies in Ch. 2. For the purpose of designing high-frequency (HF) transformers and inductors the Steinmetz equation (3.3) is a satisfactory trade-off between simplicity and accuracy and is therefore used in this dissertation for the estimation of the core losses. Referring to (3.3), the material parameters K_c, α, β are referred to as the Steinmetz parameters. They are valid for a limited frequency and flux density range [103] and can be found from manufacturers' datasheets. App. B, additional details regarding the extraction of the Steinmetz parameters are provided, reporting as an example the N97 core material [107]. The obtained parameters are: $K_c = 1.18$, $\alpha = 1.96$, and $\beta = 2.346$. Notably, even though this approach is of limited accuracy, its application is instrumental for the design of transformers and inductors for the topology selection presented in Ch. 4.

Winding Loss

Operating magnetic elements at high frequencies can lead to a significant reduction in their physical size, making them more compact and suitable for various applications. Beyond core losses, this reduction in size comes with the introduction of an additional loss mechanism, the winding losses, which impact the overall performance of the magnetic device. These losses contribute to increase the temperature of the magnetic device, which can affect the device's efficiency and reliability.

Winding losses, also referred to as copper losses, at high frequencies, are exacerbated by the phenomenon known as the *skin depth* effect. At high-frequency, the current tends to bunch towards the surface of the conductor due to the ac magnetic field created by the conductor current. This results in an increase in effective resistance, known as R_{ac}, as the net area available for current flow is reduced. Additionally, at high frequencies, the magnetic fields of adjacent conductors can interfere with each other, causing further

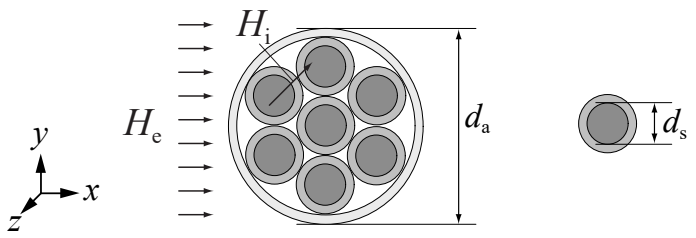


Figure 3.4: Cross-section of a round litz wire winding. Source: [82].

increases in resistance, a phenomenon referred to as the *proximity effect* [87,89,90,92,104]. Both the skin depth and proximity effects contribute to increased losses in conductors and are directly related to Faraday's law, where eddy currents are induced to oppose the flux created in the windings by the ac currents [92].

To mitigate the limitations posed by skin depth and proximity effects, *litz wires*, as displayed in Fig. 3.4, are often used. Litz wires are composed of multiple individually insulated strands, twisted together to form a bundle. Each strand equally occupies each position in the bundle, ensuring in average equal exposure to the external magnetic field [82, 92]. The accurate modeling of these high-frequency effects is crucial for ensuring an optimal trade-off between reduced size and losses in magnetic elements design.

In the following, some details and equations for winding losses calculation in litz wires are provided. The insights gained from this analysis enable the optimization of the design for the implementation of inductors and transformers, ensuring the efficient utilization of magnetic elements and enhanced performances in the considered application for EVs.

Winding Losses in Litz Wires. The study of winding losses in litz wires had notable contributions from researchers such as Dowell [90] and Ferreira [87, 89]. Dowell's equations [90] provide a one-dimensional solution for the ac resistance of transformer windings. Dowell recognized that the leakage flux lines run parallel to the surface of foil windings, and his work laid the groundwork for understanding the effects of eddy currents in winding conductors. Ferreira, on the other hand, offered a more rigorous solution for determining the ac resistance of round wires [87, 89]. In their work, Ferreira extended the one-dimensional analysis based on Dowell's equations and demonstrated the orthogonality between the skin effect and the proximity effect for the one-dimensional Cartesian solu-

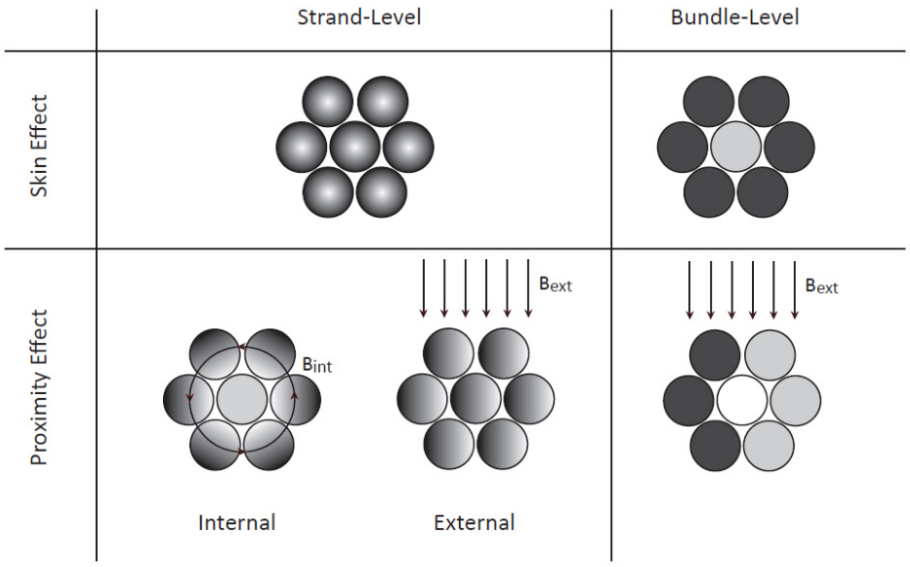


Figure 3.5: Types of eddy current effects in round litz wires. Source: [108].

tion. The orthogonality allows to calculate the losses separately, enabling more accurate predictions of winding losses in litz wires [89]. The skin effect and the proximity effect, as studied by Ferreira, have different underlying causes. The skin depth, a physical material constant, is not dependent on the geometry of the conductor. In contrast, the proximity effect is caused by eddy currents induced by an externally applied magnetic field. These effects are important considerations in understanding the losses in litz wire windings and have guided the development of accurate and practical winding loss models based on Dowell's equations and Ferreira's findings [86, 89, 92, 104, 108].

The skin effect and proximity effect in litz wire windings can be separated into two levels: strand-level and bundle-level effects. The strand-level effect occurs within individual strands, while the bundle-level effect is related to eddy currents circulating in paths involving multiple strands [89], as illustrated in Figure 3.5. The bundle-level proximity loss can be mitigated by simple twisting of the litz wire, reducing the bundle-level effects significantly [86, 109]. Therefore, for the following formulas, the bundle-level effects are generally neglected [82], and the focus is on the strand-level effects. The effective resistance of

the litz wire can be expressed as:

$$R_{\mathrm{ac}} = R_{\mathrm{dc}} \cdot (RF_{se} + RF_{ip} + RF_{ep}) \tag{3.4}$$

where R_{dc} is the dc resistance of the windings and RF are the resistance factors for the skin effect, RF_{se}, the internal proximity effect, RF_{ip}, and the external proximity effect, RF_{ep}. The proximity effects are caused by eddy currents induced by the sum of the external magnetic field H_e and the internal magnetic field H_i. In particular, in the internal proximity effect, eddy currents originate from the neighboring strands, and in the external proximity effect, eddy currents originates from the neighboring conductors [86,92,108,109], as shown in Fig. 3.5.

DC Resistance of Litz Wires. The dc resistance of a litz wire winding in (3.4) R_{dc}, made of n_s strands, each with diameter d_s, can be calculated as:

$$R_{\mathrm{dc}} = n_s \rho \frac{4}{\pi d_s^2} l \tag{3.5}$$

where ρ is the copper resistivity and l is the length of the conductor.

Skin Effect Losses of Litz Wires. The skin effect resistance factor RF_{se} for a litz wire as in Fig. 3.4 is given by [82, 86, 109]:

$$RF_{se}(f) = \frac{\zeta(f)}{2\sqrt{2}} \psi_1(\zeta) \tag{3.6}$$

where:

- ζ is the penetration ratio, defined as:

$$\zeta(f) = \frac{d_s}{\delta\sqrt{2}} \tag{3.7}$$

where δ is the skin depth, given by:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}} \tag{3.8}$$

- $\psi_{1(\zeta)}$ is the skin effect losses function for round litz wires, defined as [82,86,89,109]:

$$\psi_1(\zeta) = \frac{ber_0(\zeta)\, bei_1(\zeta) - ber_0(\zeta)\, ber_1(\zeta) - bei_0(\zeta)\, ber_1(\zeta) - bei_0(\zeta)\, bei_1(\zeta)}{ber_1^2(\zeta) + bei_1^2(\zeta)} \tag{3.9}$$

  where $ber_n(x)$ and $bei_n(x)$ are Kelvin functions, that are the real and imaginary parts of $J_n\left(xe^{\frac{3\pi i}{4}}\right)$ respectively, where x is real and $J_n(z)$ is the n^{th} order Bessel function of the first kind [82, 86, 109].

Proximity Effect Losses of Litz Wires. The magnetic field that leads to proximity effect losses is the sum of the external magnetic field H_e and the internal magnetic field H_i. For the calculation of the internal magnetic field, it is assumed that the current is equally distributed over the litz wire cross-sectional area. Consequently, each strand is assumed to be penetrated by the average internal magnetic field [82].

The resistance factor equation for the internal proximity effect losses, RF_{ip}, is given by [82, 86, 109]:

$$RF_{ip}(f) = \frac{\zeta(f) p_f n_s}{2\sqrt{2}} \psi_2(\zeta) \tag{3.10}$$

where:

- p_f is the packing factor of the bundle, defined as:

$$p_f = n_s \left(\frac{d_s}{d_a}\right)^2 \tag{3.11}$$

  where d_a is the diameter of the bundle, that could be estimated as [110]:

$$d_a = 135 \cdot 10^{-6} \left(\frac{n_s}{3}\right)^{0.45} \left(\frac{d_s}{40 \cdot 10^{-6}}\right)^{0.85} \tag{3.12}$$

- $\psi_{2(\zeta)}$ is the internal proximity effect losses function defined as [82, 86, 109]:

$$\psi_2(\zeta) = \frac{bei_2(\zeta)\, ber_1(\zeta) - ber_2(\zeta)\, ber_1(\zeta) - ber_2(\zeta)\, bei_1(\zeta) - bei_2(\zeta)\, bei_1(\zeta)}{ber_0^2(\zeta) + bei_0^2(\zeta)} \tag{3.13}$$

The resistance factor equation for the external proximity effect losses, RF_{ep}, is given by [82, 86, 109]:

$$RF_{ep}(f) = \frac{\zeta(f)\pi^2 d_s^2 n_s^2}{2\sqrt{2}} \left(\frac{\hat{H}_e}{\hat{I}}\right)^2 \tag{3.14}$$

where $\hat{I}$ is the magnitude of the current flowing through the windings.

One approach to mitigate the proximity effect loss is to interleave the windings, that is, involves alternating the primary and secondary layers. By doing so, the external proximity effect RF_{ep} can be strongly reduced, and the ac resistance of the winding can be improved. Additionally, interleaving the windings reduces the leakage inductances [92].

Winding losses can be therefore derived from (3.4) as follows:

$$P^{\text{cond}} = R_{\text{dc}} I_{\text{dc}}^2 + \sum_{i=1}^{M} R_{\text{ac}}(f_i) I_{i,\text{rms}}^2 \tag{3.15}$$

where $I_{i,\text{rms}}$ is the rms current at the frequency component f_i flowing in the windings.

It is essential to note that the discussed equations provide an idealized estimation of winding losses, not considering fringing effects or magnetic energy stored in the windings themselves. In practice, more accurate estimates can be obtained by employing finite element analysis, which accounts for various complexities and non-idealities [92]. However, such an approach goes beyond the scope and objectives of this dissertation. Therefore, for the purpose of this study, simplified analytical models and formulae are utilized to estimate winding losses in magnetic elements for the aim of compare the topologies proposed in Ch. 2.

Design Procedure of the Magnetic Elements

The design of inductors and transformers is a crucial step in the development of an high efficiency electronic power converter. A well-balanced design results in a trade-off between core losses and winding losses [92]. Especially in the context of high-frequency operation, where the physical size of these magnetic components can be significantly reduced, understanding the impact of various loss mechanisms becomes paramount.

At high frequencies, core losses and winding losses become more pronounced due to the rapid changes in the magnetic flux $B_{\max}$ and the alternating currents flowing through the windings. To achieve an efficient design, the magnetic element must be optimized to strike a balance between core losses and copper losses. If a core fully filled with copper is desired, the value of $B_{\max}$ can be adjusted by changing the number of windings. Increasing the number of windings reduces $B_{\max}$, thereby decreasing the core losses while increasing the copper losses. On the other hand, reducing the number of windings increases $B_{\max}$, leading to higher core losses but lower copper losses. The objective is to find an optimal configuration that minimizes the total power losses while meeting the required performance specifications. This involves careful consideration of various design parameters, such as the core material, winding wire, number of turns, and operating frequency. On this basis, the following procedure outlines the key steps involved in the design process:

1. Select the operating frequency, f_s, and appropriate litz wires to mitigate skin and proximity effects in the windings.

2. Select a magnetic core and core material. The cores have specific characteristics: a magnetic volume V_c, a core cross-sectional area A_c, a window winding area W_a, a total windings volume V_w, and the Steinmetz parameters K_c, α and β. Geometric dimensions are shown in Fig. 3.6.

3. Choose litz wire section and number of turns that fully filled the core.

4. Calculate winding losses as in (3.15), considering the resistance of the wire, skin effect, and proximity effect.

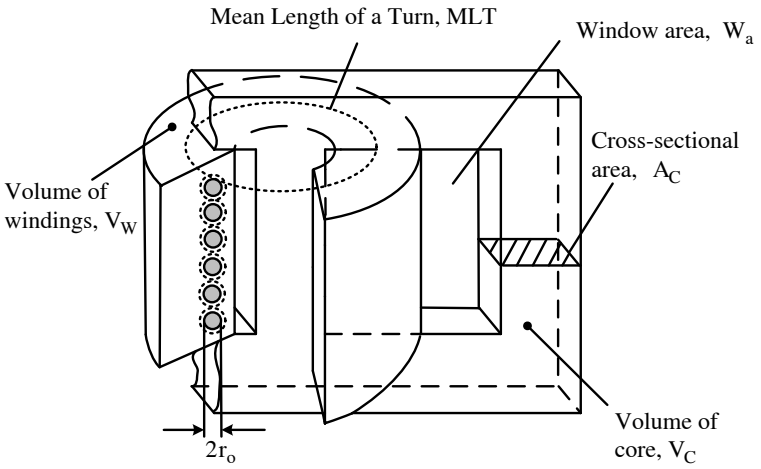


Figure 3.6: Example of layout of a magnetic element. Source: [92].

5. Estimate core losses with the Steinmetz equation in (3.3) based on core material properties and operating conditions.

6. Calculate total losses $P^{\text{loss}}(B_{\max}) = P^{\text{core}} + P^{\text{cond}}$, where $B_{\max}$ is the peak value of the flux density.

7. Repeat from step 2 the procedure until $P_{\text{tot}}(B_{\max})$ is minimized.

8. Ensure that the design can handle the generated heat without compromising performance.

The procedure outlined above is described in further detail in the following for both transformers and inductors. These formulas provide a systematic approach to estimate core losses, winding losses, and minimize their combined effect.

Transformer Design Procedure. The rms value of the impressed voltage on a winding V_{rms} can be derived form Faraday's law as [92]:

$$V^{\text{rms}} = K_v f_s N B_{\max} k_f A_c \tag{3.16}$$

where K_v is the waveform factor, $K_v = 4$ for square-wave excitation, and k_f is the core stacking factor, $k_f = 1$ for ferrite cores [92].

The power rating of the transformer, $\sum VA$, is given by taking the sum of the $V_i^{\mathrm{rms}}\, I_i^{\mathrm{rms}}$ products in an n winding transformer:

$$\sum VA = \sum_{i=1}^{n} V_i^{\mathrm{rms}} I_i^{\mathrm{rms}} = \sum_{i=1}^{n} K_v f_s N_i B_{\max} k_f A_c\, I_i^{\mathrm{rms}} = K_v f_s B_{\max} k_f A_c \sum_{i=1}^{n} N_i I_i^{\mathrm{rms}} \tag{3.17}$$

where N_i is the number of windings in the i-th winding that carriers the current I_i^{rms}. A core window filling factor k_u can be defined as [92]:

$$k_u = \frac{W_c}{W_a} = \frac{\sum_{i=1}^{n} N_i A_{w_i}}{W_a} = \frac{\sum_{i=1}^{n} N_i I_i^{\mathrm{rms}}}{W_a J_0} \tag{3.18}$$

where W_c is the total effective conducting area, $A_{w_i} = I_i^{\mathrm{rms}}/J_i$ is the conducting area of the i-th winding and J_0 is the current density equal for each i-th winding. Therefore, by substituting (3.18) in (3.17), it yields:

$$\sum VA = K_v f_s B_{\max} k_f J_0 k_u A_p \tag{3.19}$$

where $A_p = A_c W_a$ is the area product of the core.

The dc resistance of the windings can be defined as [92]:

$$R_{\mathrm{dc}} = \rho_w \sum_{i=1}^{n} \frac{N_i l_i W_a}{A_{w_i} W_a} \tag{3.20}$$

where ρ_w is the copper resistivity and $l_i = V_{w_i}/W_a$ is the mean length of a turn. Winding losses can be therefore calculated from (3.15), (3.18) and (3.20) as:

$$P^{\mathrm{cond}} = RF(f_s) R_{\mathrm{dc}} (A_{w_i} J_0)^2 = RF(f_s) \rho_w V_w k_u J_0^2 \tag{3.21}$$

where $RF(f_s)$ is given in (3.4), the window filling factor with litz wires is about $k_u \leq 0.4$ and J_0 is given by (3.19). This results in the expression for the estimation of the winding losses, which is a function of $B_{\max}$:

$$P^{\mathrm{cond}}(B_{\max}) = RF(f_s) \rho_w V_w k_u \left(\frac{\sum VA}{K_v f_s k_f B_{\max} k_u A_p} \right)^2 \tag{3.22}$$

where P^{cond} represents the winding losses, $RF(f_s)$ is a factor accounting for the skin and proximity effects in (3.4), ρ_w is the resistivity of the winding material, V_w is the winding volume, $k_u \simeq 0.4$ is the filling factor, $\sum VA$ is the sum of the $V_i^{\text{rms}} I_i^{\text{rms}}$ products in an n-winding transformer, $K_v = 4$ is the waveform factor for square-wave excitation, f_s is the switching frequency, $k_f = 1$ is the stacking factor for ferrites, $B_{\max}$ is the peak value of the magnetic flux density, and A_p is the area product of the selected core.

From (3.3) and (3.22), the minimum total losses of the transformer, $P^{\text{cond}}(B_{\max}) + P^{\text{core}}(B_{\max})$, can be computed by solving the following equation for $B_{\max}$:

$$\begin{cases} P^{\text{cond}}(B_{\max}) = RF(f_s)\rho_w V_w k_u \left(\dfrac{\sum VA}{K_v f_s k_f B_{\max} k_u A_p} \right)^2 \\ P^{\text{core}}(B_{\max}) = V_c K_c f_s^{\alpha} B_{\max}^{\beta} \end{cases} \tag{3.23}$$

The found minimum of losses must be lower than the maximum thermal dissipation capability of the selected core, that can be determined as:

$$P^{\text{diss core}} = h_c k_a A_p^{1/2} \Delta T \tag{3.24}$$

where h_c is the heat transfer coefficient (typical values in the range 10 to $30\,\text{W/°C}\,\text{m}^2$ [92], $28\,\text{W/°C}\,\text{m}^2$ found experimentally for core PQ65/60), k_a is the surface area coefficient of the would transformer (typically, $k_a = 40$ [92]), A_p is the area product and ΔT is the desired maximum temperature increment. Once $B_{\max}$ that minimizes the contribution $P^{\text{cond}}(B_{\max}) + P^{\text{core}}(B_{\max})$ is found, denoted as B_{opt}, the number of turns of the i-th winding can be determined from Faraday's law as:

$$N_i = \frac{V_{\text{rms},i}}{K_v f_s B_{\text{opt}} k_f A_c} \tag{3.25}$$

Fig. 3.7 is an example of transformer losses minimization derived from (3.23). The selected core is the PQ65/60, core material N87 with Steinmetz parameters $K_c = 3.76$, $\alpha = 1.86$ and $\beta = 2.57$. Selected litz wire $2\times(825 \times 50\,\mu\text{m})$, and number of turns $N_1 = 24$ and $N_2 = 12$.

Finally, a useful expression for estimating the total equivalent leakage inductance L_{lk}

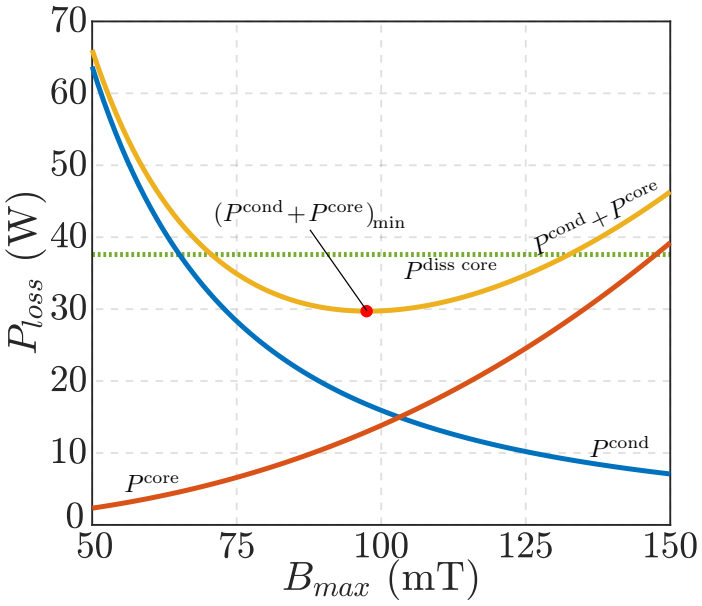


Figure 3.7: Example of transformer design. Core: PQ65/60, core material N87 with Steinmetz parameters $K_c = 3.76$, $\alpha = 1.86$, and $\beta = 2.57$. Litz wire: $2\times(825 \times 50\,\mu\text{m})$. Number of turns $N_1 = 24$ and $N_2 = 12$.

of the transformer windings is given by:

$$L_{lk} = \frac{\mu_0 N_i^2 l_{mlt} b}{3w} \tag{3.26}$$

where l_{mlt} represents the mean length of a turn, b is the thickness occupied by the windings, and w is the width occupied by the windings in the core. This expression is derived in [92] and is applicable specifically in the case of transformers with interleaved windings.

Inductor Design Procedure. The peak value of the current in the inductor $\hat{I}$ can be derived as follows [92]:

$$\hat{I} = \frac{B_{\text{max}} l_c}{\mu_{eff} \mu_0 N} \tag{3.27}$$

where l_c is the effective length of the magnetic path, μ_{eff} is the relative permeability accounting for the gap and N is the number of turns.

The maximum energy stored in an inductor can be expressed as [92]:

$$\frac{1}{2} L \hat{I}^2 = \frac{1}{2} B_{\text{max}} A_c N \hat{I} \tag{3.28}$$

where L is the inductor value.

Considering that the total conduction area is $W_c = NA_w = k_u W_a$ and $J_0 = I_{\mathrm{rms}}/A_w = K_i \hat{I}/A_w$ with K_i denoting the current waveform factor, the current density J_0 can be expressed as a function of $B_{\max}$ as follows:

$$J_0 = \frac{LI_{\mathrm{rms}}^2}{K_i B_{\max} k_u A_p} \tag{3.29}$$

This leads to the expression for estimating the winding losses, which is a function of $B_{\max}$:

$$P^{\mathrm{cond}}(B_{\max}) = RF(f_s)\rho_w V_w k_u \left(\frac{LI_{\mathrm{rms}}^2}{K_i B_{\max} k_u A_p} \right)^2 \tag{3.30}$$

Similarly to (3.3), core losses of the inductor can be calculated using the following equation:

$$P^{\mathrm{core}}(\Delta B) = V_c K_c f_s^{\alpha} \left(\frac{\Delta B}{2} \right)^{\beta} \tag{3.31}$$

The number of turns N of the inductor is given by:

$$N = \sqrt{\frac{Ll_c}{\mu_0 \mu_{eff} A_c}} \tag{3.32}$$

where the relative permeability can be determined as:

$$\mu_{eff} = \frac{B_{\max}^2 V_c K_i^2}{\mu_0 LI_{\mathrm{rms}}^2} \tag{3.33}$$

From (3.30) and (3.31), the minimum total losses of the inductor can be computed as done for the transformer core in (3.23). In this case too, total losses must be lower than the maximum thermal dissipation capability of the inductor, as in (3.24).

Fig. 3.8 shows an example of inductor losses minimization derived with (3.30) and (3.31). Selected core is the PQ40/40, core material N97 with Steinmetz parameters $K_c = 1.18$, $\alpha = 1.96$ and $\beta = 2.35$. Selected litz wire $3\times(825 \times 50\,\mu\mathrm{m})$, and number of turns $N = 15$.

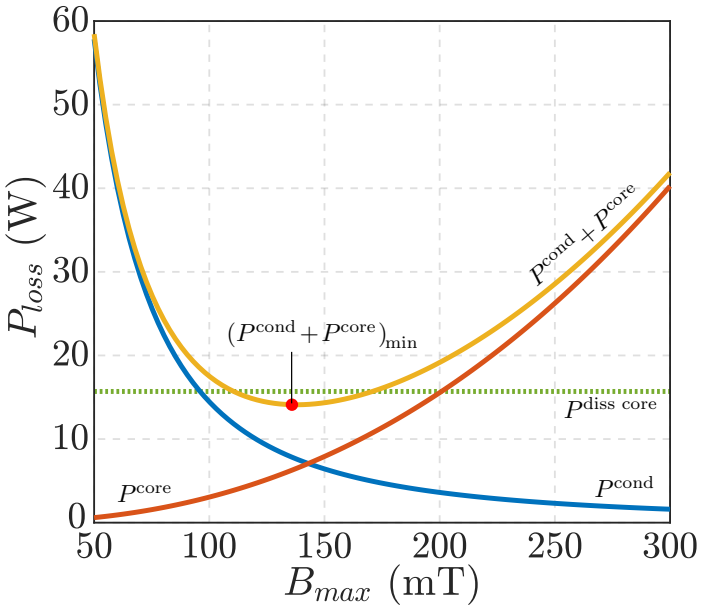


Figure 3.8: Example of inductor design. Core: PQ40/40, core material N97 with Steinmetz parameters $K_c = 1.18$, $\alpha = 1.96$, and $\beta = 2.35$. Litz wire: $3\times(825 \times 50\,\mu\text{m})$. Number of turns $N = 15$.

By following this design procedure and considering the interplay between core and winding losses, it is possible to achieve an efficient magnetic design for the considered high-frequency power electronics application. These simplified models shown to offer a good compromise between accuracy and computational efficiency, making them suitable for the comparison of the topologies in Ch. 2.

3.3.4 Capacitors

Capacitor losses are associated with resonant capacitors, such as C_r, and dc bus capacitors, like C_g and C_o in the LLC schematic in Fig. 2.3. By carefully selecting and parallelizing capacitors in the dc bus capacitor bank and resonant capacitors, the overall equivalent series resistance (ESR) can be effectively reduced. This reduction directly contributes to diminishing losses associated with capacitor heating and energy dissipation. Parallelization not only aids in minimizing losses but also ensures efficient distribution of the load, leading to improved power sharing among capacitors. Efficient estimation of these losses is crucial for accurate converter design and optimization.

For resonant capacitors and dc link capacitors, their losses can be determined through

various methods. Simulated currents $I_{C_i,\mathrm{rms}}$ flowing through these capacitors provide insights into their losses, coupled with the consideration of their equivalent series resistance value at a specified frequency, $ESR(f)$, often at the frequency of the ripple current. The estimation of capacitor losses can be expressed using analytical expressions, as detailed below:

$$P_{C_i}^{\mathrm{loss}} = ESR_{C_i}(f_{\mathrm{ripple}})I_{C_i,\mathrm{rms}}^2 \tag{3.34}$$

The ESR typically ranges from few $\mathrm{m}\Omega$ to tens of $\mathrm{m}\Omega$, under the specified operating conditions. The meticulous design and parallel connection of the dc bus capacitor bank and resonant capacitors contribute in achieving optimal converter performance and minimizing losses.

3.4 Loss Extrapolation from Simulations

This section presents the implementation of the theoretical description of the models presented in Sect. 3.3 within the PLECS® Blockset package implemented in Simulink® environment, and subsequent calculation in MATLAB®.

Specifically, the PLECS® simulation environment is employed to simulate the circuit behavior and extract currents and voltage waveforms during steady-state operation. The extracted quantities of interest allows for subsequent power loss calculations. The power losses are subsequently computed using MATLAB®, where the quantities of interest are combined with the established loss models as described in Sect. 3.3. Notably, PLECS® simulation environment provides a comprehensive platform for directly extract the losses associated with MOSFETs and diodes. This is facilitated by utilizing energy loss maps integrated into the PLECS® domain, enabling direct estimation of MOSFETs and diodes losses. In the following the process of calculating the losses within the simulation environment is outlined.

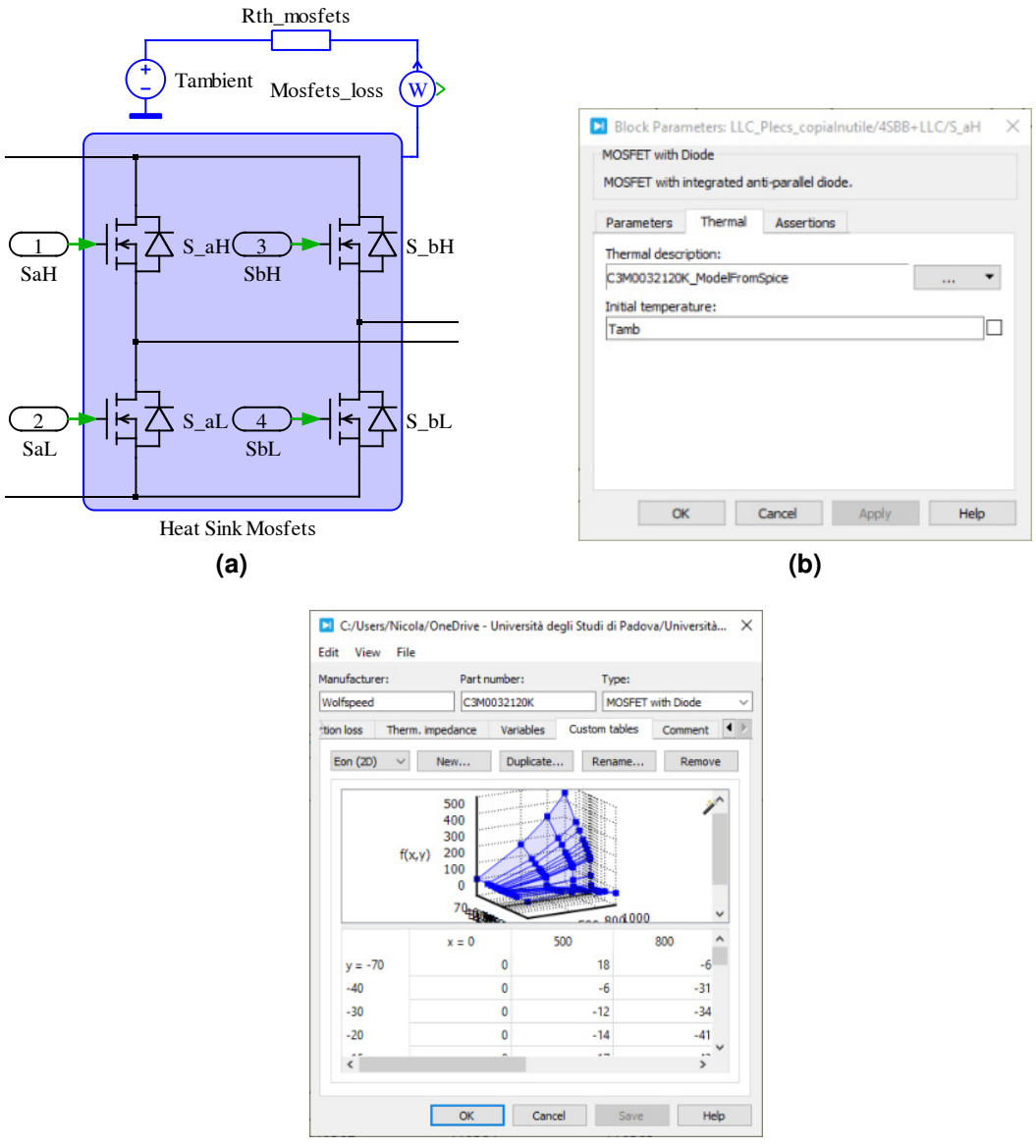


Figure 3.9: MOSFETs loss estimation in PLECS® simulation environment. Considered device: Wolfspeed C3M0032120K 1.2 kV SiC MOSFET. (a) PLECS® schematic; (b) thermal model; and (c) lookup table for switching loss calculation.

3.4.1 MOSFETs

Switch losses are directly obtained from PLECS® simulations by utilizing energy loss maps integrated into the switch models for switching losses. The relation (3.1) is employed to determine conduction losses. Conduction losses were evaluated assuming a device temperature of 50°C. Notably, these energy loss maps were obtained using LTspice®, implementing the manufacturer's SPICE models of the switching device.

The switch model implementing the total switches loss calculation and the lookup table for switching loss calculation, are illustrated in Figs. 3.9b and 3.9c, respectively. The switching energy loss lookup tables for turn-on $E_{on}(V_g)$ and turn-off $E_{off}(V_g)$ transients at various switched current values can resemble those depicted in the example presented in Fig. 3.2. App. A reports additional details.

As depicted in Fig. 3.9a, within the PLECS® simulation environment, the total device losses can be extracted following a steady-state simulation that incorporates the *heatsink* behavioral block. This simulation block enables a direct extraction of the total losses for the devices implementing thermal description models, such as MOSFETs and diodes.

3.4.2 Diodes

Similarly for the MOSFETs losses, diode losses are computed within the PLECS® environment using lookup tables data integrated into the diode's thermal model. As noted in Sect. 3.3.2, only conduction losses are taken into account for diodes, as switching losses in resonant topologies operated as dc-transformers are considered negligible [39]. Consequently, the lookup tables exclusively contain data related to conduction losses. An illustrative model example is presented in Fig. 3.10. Conduction losses were evaluated assuming a device temperature of 50°C.

By utilizing the *heatsink* behavioral block, the losses can be directly extracted, enabling the estimation of the total loss.

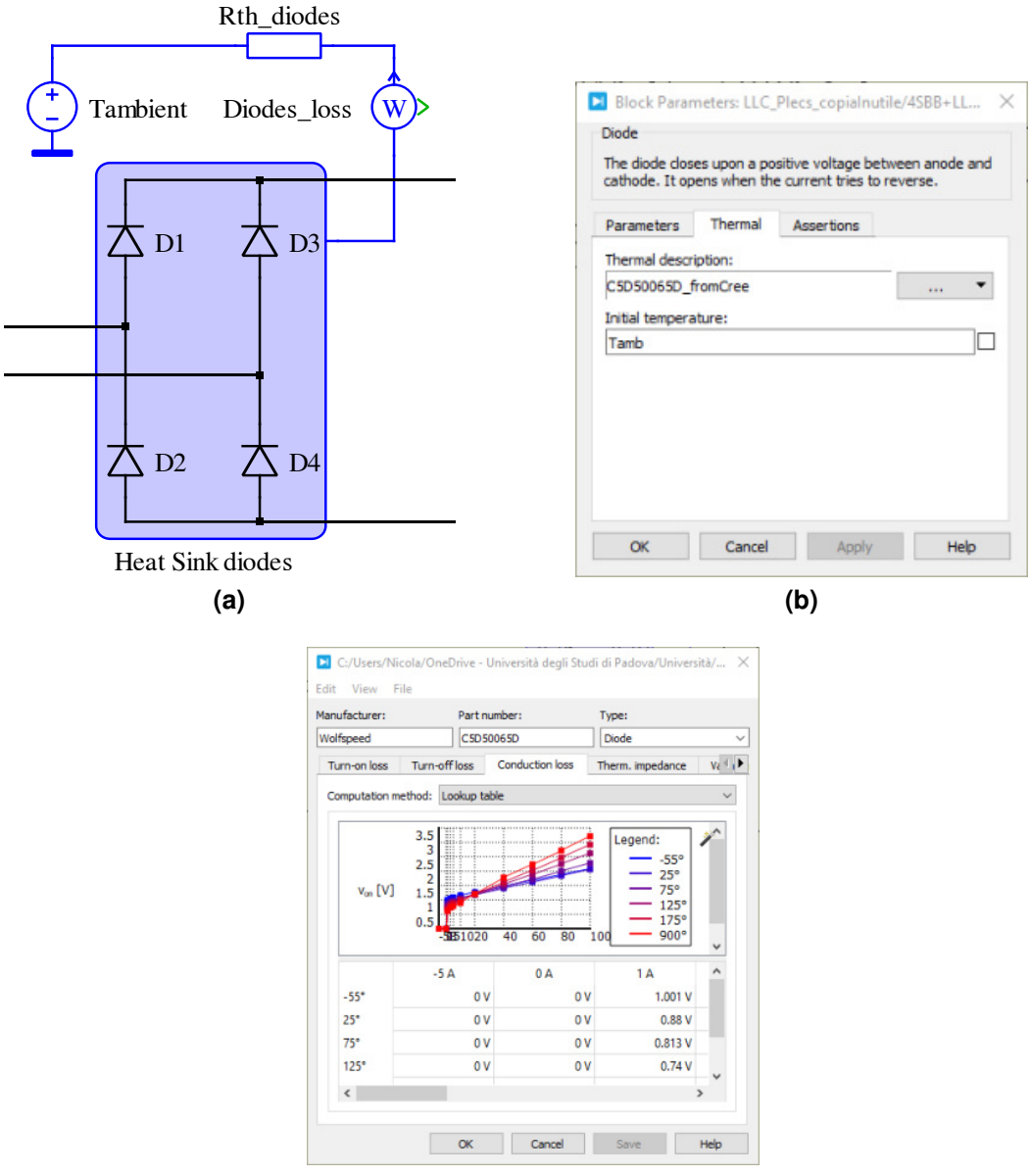


Figure 3.10: Diodes loss estimation in PLECS® simulation environment. Considered device: Wolfspeed C5D50065D 650 V SiC Schottky diode. (a) PLECS® schematic; (b) thermal model; and (c) lookup table for conduction loss calculation.

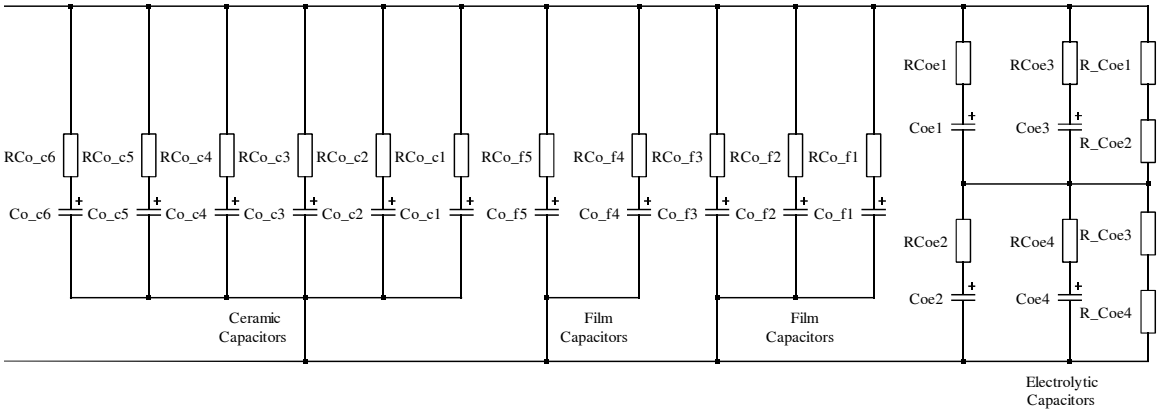


Figure 3.11: DC link capacitors loss estimation in PLECS® simulation environment.

3.4.3 Transformer and Inductor

Within the PLECS® simulation, voltage and current entities of interest are obtained. These quantities are collected after reaching the steady-state convergence, and then elaborated in MATLAB® environment for loss estimation. Conduction losses are calculated by analyzing current harmonics up to the fourth order using the fast Fourier transform (FFT) MATLAB® algorithm. Remarkably, the loss expressions used for the calculations are (3.3) for the core losses and (3.15) for the conduction losses. The obtained results provide insights into the total losses due to the transformers and the inductors under given operating conditions.

3.4.4 Capacitors

In the PLECS® simulation environment, the capacitor bank, such as the one shown in Fig. 3.11 for a dc link, is simulated. Each individual capacitor is modeled with its ESR. Within the PLECS® simulation, the currents flowing through each capacitor are exported, once steady-state convergence is achieved. In the MATLAB® environment, the capacitor losses are calculated using the obtained current profiles and by determining its rms value through (3.34).

This allows the determination of the total losses incurred by the capacitors in the converter. Furthermore, it provides a detailed breakdown of the loss contributions from the individual capacitors, contributing to a comprehensive understanding of the converter's loss behavior.

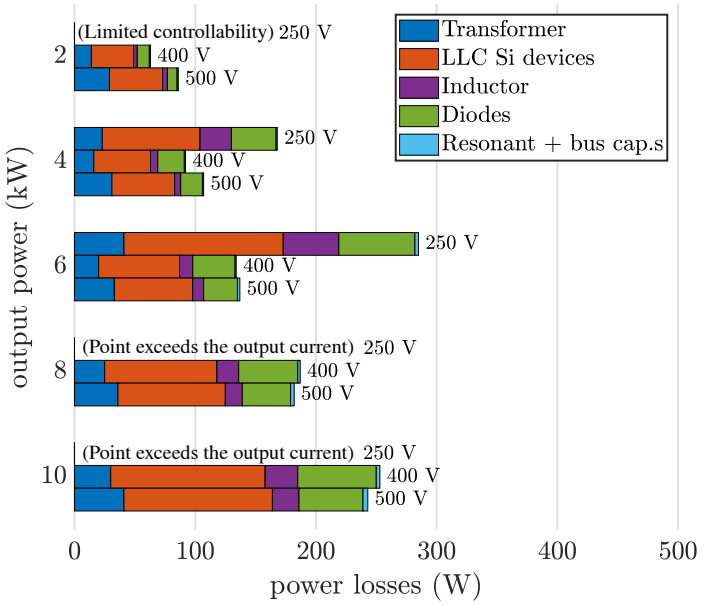


Figure 3.12: Example of loss breakdown of the Si-based LLC at different output power and output voltages.

3.4.5 Example of Loss Breakdown

This subsection presents an example of loss breakdown analysis obtained using the proposed approaches. This example serves as a preliminary insight into the subsequent loss breakdown comparisons in Ch. 4.

Fig. 3.12 showcases a loss breakdown analysis conducted on a Si-based LLC converter with topology as in Fig. 2.3. The depicted loss breakdown demonstrates the distribution of losses among the different components of the converter: MOSFETs, diodes, inductors, transformer and capacitors. The approach utilized to derive these loss contributions involves a combination of simulation in PLECS® and subsequent calculations in MATLAB®, as described above in this Sect. 3.4. The resulting loss breakdown provides valuable insights into the relative contributions of each component to the overall losses of the converter. Such detailed information is crucial for design optimization and performance evaluation.

3.5 Loss Measurement Approach

This section presents the loss measurement techniques to estimate the losses of the components in the experimental prototypes. These losses measurements enable a precise evaluation of system losses and validate an tune the adopted loss models in Sect. 3.3. Accurate measurement of losses in switching devices and magnetic elements is essential for optimizing the performance of power converters, as these components contribute significantly to overall losses, as illustrated in the loss breakdown example of Fig. 3.12.

Various methods have been proposed in the literature to measure these losses, each with its advantages and limitations. For example, DPT is a commonly used method for measuring switching losses in switching devices. This method relies on electric measurements to calculate the energy dissipated during a switching transition. However, the measurement accuracy of electric methods is affected by the performance of the measurement setup [99]. An alternative approach is offered by calorimetric measurement, which exploits thermal quantities (e.g., temperature or heat flux) to measure the component losses independently of their electrical characteristics. These methods can be categorized into steady-state and transient techniques. Transient methods analyze the thermal dynamics of the system, reducing the measurement times compared to the steady-state ones. Examples of this approach can be found in [99, 103, 111, 112]. However, they often require an external heat chamber for performing measurements at timed intervals. In contrast, steady-state methods operate until a thermal equilibrium is reached, allowing the estimation from observed temperature values. This method may require several hours to achieve thermal equilibrium, particularly for components such as transformers.

In this dissertation, a simplified and less precise version of the steady-state thermometric method is employed. This method does not adopt external heat chambers and involves a thermal camera or thermocouples next to converter components to monitor the temperature. The adopted method involves injecting a dc current into the device under test and measuring the well-known dc losses. After reaching the thermal steady-state, the losses can be extracted during converter operation by mapping the component temperature at different currents. Fig. 3.13b illustrates the power loss map of the switching devices in Fig. 3.13a,

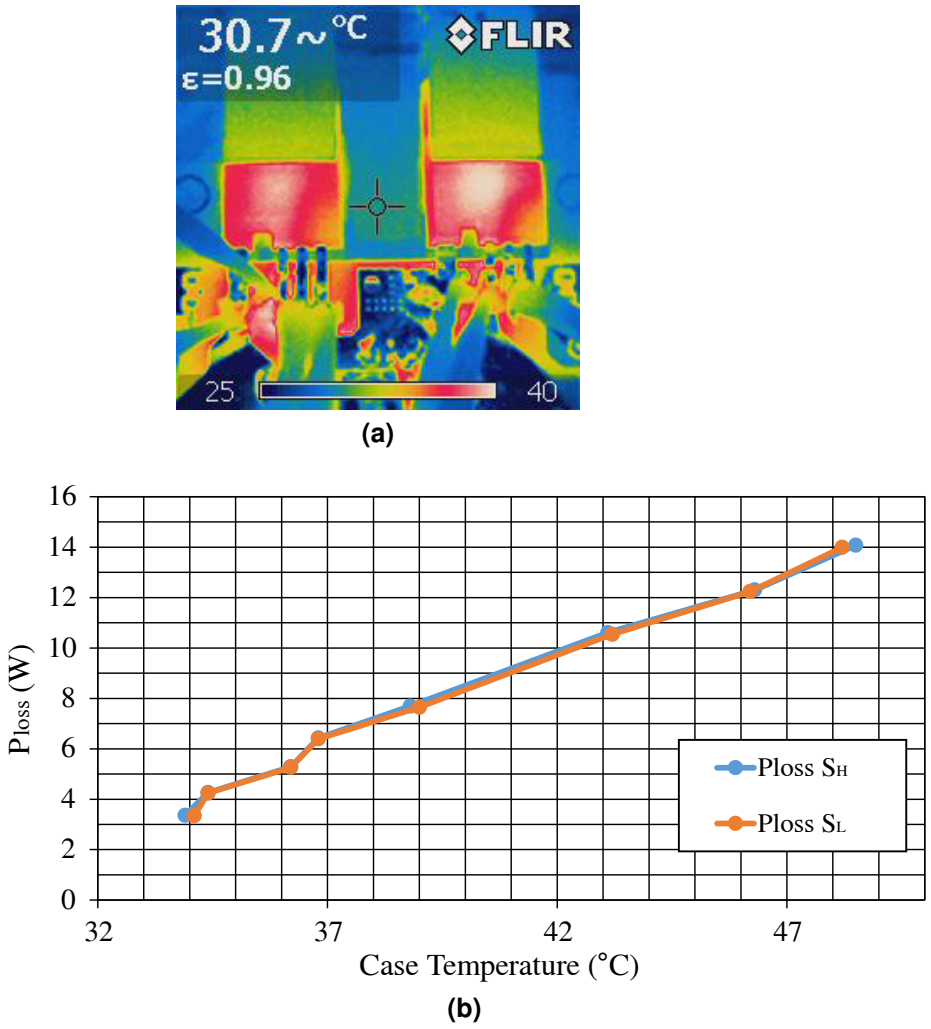


Figure 3.13: MOSFETs loss measurement under dc current excitation. (a) MOSFETs under test; and (b) measured losses at corresponding case temperature.

mounted on the converter prototype, under dc current flowing through both the devices.

While this approach simplifies the measurement process and may introduce some lack of accuracy in the loss estimations, it provides valuable insights into the component's thermal behavior and loss characteristics. This enables a loss estimation for power converter discrete components, including diodes, MOSFETs, inductors, and transformers.

In the upcoming chapters, the predicted losses using the models presented in Sect. 3.3 are experimentally validated using the described thermometric method. This validation provides a comprehensive analysis of the loss breakdown in various power semiconductor devices and magnetic elements, enhancing the understanding of losses and their implications in power converter design and performance.

3.6 Summary

This chapter introduced loss models integrated into the PLECS®/Simulink® simulation environment used to estimate the converter losses of the multi-stage converter topologies introduced in Ch. 2. *The implementation of these loss models in the simulation environment serves multiple purposes, including the selection of the optimal multi-stage topology, the loss breakdown analysis, and the optimization of the converter design.* The theoretical foundation of component modeling is outlined, emphasizing its significance in the design of power converter components. These components encompass MOSFETs, diodes, magnetic elements, and capacitors. The modeling ensures proper component selection, accurate volume sizing, and overall converter efficiency improvement. By implementing component models in simulation environments, converter component losses can be estimated, facilitating efficiency evaluation and guiding design enhancements. The presented loss measurement technique provides valuable insights into the losses of individual components in experimental prototypes, validating the models during the design phase.

Chapter 4

Topology Comparison

Chapter in Brief

The chapter conducts a simulation-based comparison of the multi-stage dc-dc converter topologies introduced in Ch. 2 and tailored for EV XFC systems. Resonant converters offer efficiency benefits limited to operating frequency near their resonant frequency. LLC-based two-stage converters emerged as promising solutions to address the limits of frequency modulated single-stage resonant converters. Three two-stage topologies are introduced in Ch. 2, forming the basis of the investigation herein. Circuital modifications and WBG semiconductor implementation are explored. Simulation models from Ch. 3 are employed using PLECS® Blockset in Simulink® and MATLAB®. Design parameters derive from the procedures introduced in Ch. 3, considering a $400\,\mathrm{V}$ EV battery pack with $800\,\mathrm{V}$ input, 250 - $500\,\mathrm{V}$ output, and 10- kW power. These scaled prototypes represent a practical parallel module operation. The goal is a comprehensive assessment of efficiency and identification of the optimal converter topology for EV charging, among the proposal in Ch. 2. Promising solutions are further explored experimentally in Ch. 5 and Ch. 6.

4.1 Introduction

DC-DC converters in EV charging application play a pivotal role in the battery voltage regulation. As introduced in Ch. 2, LLC-based multi-stage converter configurations have emerged as promising solutions to address the efficiency limitations of single-stage resonant converters. In this chapter, a simulation-based comparative analysis of the multi-stage dc-dc converter topologies introduced in Sect. 2.3 is performed to identify the most suitable architecture for an efficient EV extreme-fast charging systems. Sect. 2.3 proposes relevant

two-stage converter topologies, including the buck-boost LLC in Sect. 2.3.1 and a DCX-CLLC post-regulated partial-power processing (PPP) topology configuration in Sect. 2.3.2, as well as the DCX-LLC TBB post-regulated topology in Sect. 2.3.3. Additionally topological variants with small circuital modifications (e.g., interleaved stages, active rectification) and/or technology (e.g., utilization of WBG semiconductors) are investigated, being implemented based on performance outcomes. The simulation models developed in Sect. 3.3 are employed to rigorously analyze the efficiency of these multi-stage converter topologies. For simulation purposes, the PLECS® Blockset in Simulink® platform integrated with MATLAB® is employed as described in Sect. 3.4. Design parameters for each analyzed topology are outlined, following the design procedures introduced in Ch. 3. Furthermore, it is important to note that the selected converter topologies are designed for a $400\,\mathrm{V}$ EV battery pack, as mentioned in Sect. 1.3. Specifically, the nominal input voltage provided by the PFC is set at $800\,\mathrm{V}$, with an output voltage range of 250 - $500\,\mathrm{V}$ and a power rating of $10\,\mathrm{kW}$. In actual applications, multiple power modules, typically rated near to $50\,\mathrm{kW}$, are connected in parallel to form the required power rating of the XFC station.

In summary, *this chapter aims to evaluate and compare the efficiency performance of multi-stage converter topologies of Ch. 2.* The analyses through models in Ch. 3 provide valuable insights into most suitable architectures for EV charging applications. The most attractive solutions are explored experimentally in Ch. 5 and Ch. 6.

Part of the content of this chapter has been published in [25, 26].

4.2 Evaluated Topologies

Two-stage dc-dc converter configurations, as introduced in Ch. 2, shows promising attributes for addressing the efficiency limitations associated with single-stage resonant converters. As introduced in Ch. 2, by employing a pre-regulation or a post-regulation stage, these topologies allow the resonant converter to operate in DCX conditions, mitigating efficiency degradation typically encountered in wide load and voltage range scenarios.

The following multi-stage dc-dc converter topologies are compared in this chapter:

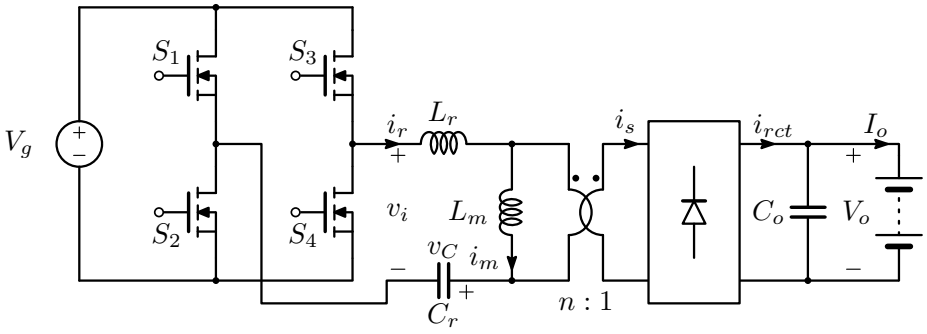


Figure 4.1: Full-bridge LLC converter topology with passive rectification.

1. Benchmark: single-stage LLC (reference point for comparison);
2. Buck-boost LLC (Sect. 2.3.1);
3. DCX-CLLC & PPP (Sect. 2.3.2);
4. DCX-LLC & TBB (Sect. 2.3.3).

These topologies are also evaluated by implementing circuit variations (such as interleaved stages, and active rectification), as well as different combinations of WBG semiconductor technologies. Specifically, the considered voltage ratings for SiC MOSFETs and SiC Schottky diodes are $650\,\mathrm{V}$ or $1200\,\mathrm{V}$. For GaN high electron mobility transistors (HEMTs), the considered voltage ratings are $400\,\mathrm{V}$ or $650\,\mathrm{V}$, which are typical voltage ratings available in the market. The $1200\,\mathrm{V}$ GaN technology is still in its early stages of development, and its incorporation is restricted to the SiC MOSFETs.

Different topology variants, including both circuit variations and implementation of WBG technology are analyzed herein. For these circuits a short description of the operating principles is given, they are therefore designed in Sect. 4.3 and compared in Sect. 4.4, shedding light on their performance characteristics and potential advantages.

4.2.1 Full-Bridge LLC

The FB-LLC is simulated in three different variants:

- $1200\,\mathrm{V}$ Si-based MOSFETs and $650\,\mathrm{V}$ SiC-based diodes;
- $1200\,\mathrm{V}$ SiC-based MOSFETs and $650\,\mathrm{V}$ SiC-based diodes;

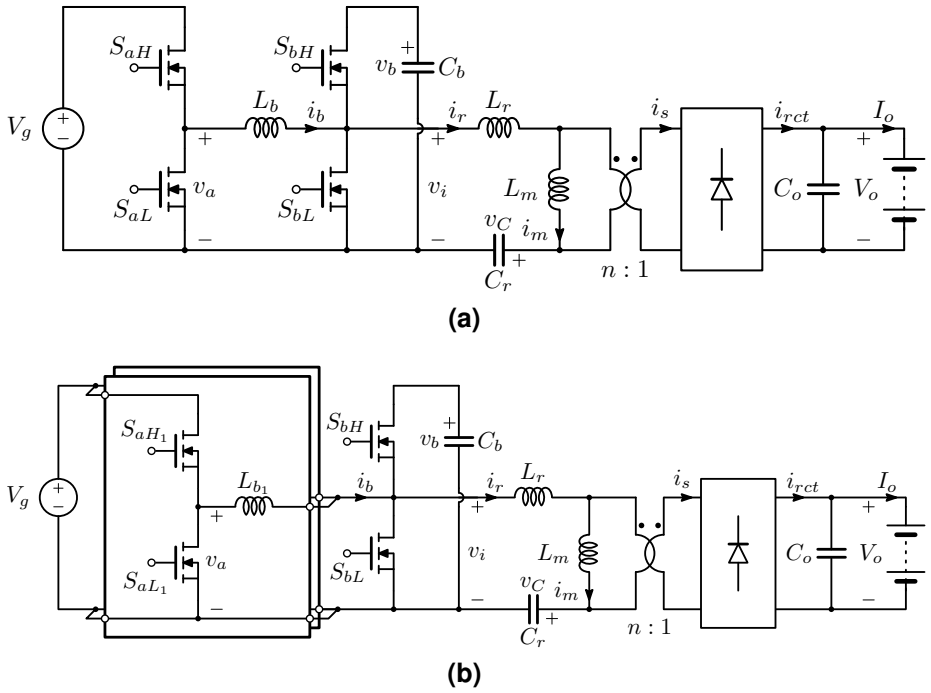


Figure 4.2: (a) Buck-boost LLC; (b) Buck-boost LLC with interleaved buck-boost pre-regulation stage.

- 1200 V SiC-based MOSFETs and 650 V GaN-based active rectification.

The schematic of the FB-LLC with passive rectification is provided in Fig. 4.1 for reference. The implementation of GaN active rectification involves substituting the passive rectifier bridge with an active H-bridge composed of GaN devices, equipped with appropriate driving circuits.

In the following Sect. 4.3.1 and Sect. 4.4.1, the design and efficiency analysis of each of these variations of the LLC converter are presented. Moreover, the LLC employing entirely SiC switching devices is used as a benchmark for comparison with all the other aforementioned topologies at the beginning in Sect. 4.2.

4.2.2 Buck-Boost LLC

The BB-LLC is simulated in two different variants:

- 1200 V SiC-based MOSFETs;

- 1200 V SiC-based MOSFETs with interleaved buck-boost stage.

The schematic of the BB-LLC topology is provided in Fig. 4.2a for reference. A topology variation with an interleaved buck-boost stage is proposed in Fig. 4.2b in order to reduce the circulating currents in the input inductor. Active rectification is not considered for this topology. In the forthcoming Sect. 4.3.2 and Sect. 4.4.2, the design and efficiency analysis of each of these BB-LLC variations are presented.

4.2.3 CLLC & Partial-Power Post-Regulator

The DCX-CLLC & PPP is simulated in two different variants:

- $400\,\mathrm{V}$ GaN-based PPP stage;
- $400\,\mathrm{V}$ GaN-based and interleaved buck PPP stage.

The schematic of the DCX-CLLC & PPP topology is provided in Fig. 4.3a for reference. A topology variation with interleaved buck stage is proposed in Fig. 4.3b. Active rectification is required for the rectifier preceding the PPP stage, owing to reverse power flow in the low output voltage region, consequently a CLLC resonant converter configuration is necessary. Active rectification is not considered for the main converter rectifier. In Sect. 4.3.3 and Sect. 4.4.3, the design and efficiency analysis of each of these DCX-CLLC & PPP variations are presented.

4.2.4 LLC & Twin-Bus Buck Post-Regulator

The DCX-LLC & TBB is simulated in three different variants:

- $650\,\mathrm{V}$ SiC-based TBB stage;
- $650\,\mathrm{V}$ SiC-based interleaved TBB stage;
- $650\,\mathrm{V}$ GaN-based interleaved TBB stage.

The schematic of the DCX-LLC & TBB topology is provided in Fig. 4.4a for reference and documentation convenience. A topology variant with interleaved TBB stage is proposed in Fig. 4.4b to reduce the circulating currents in the output inductor. This latter

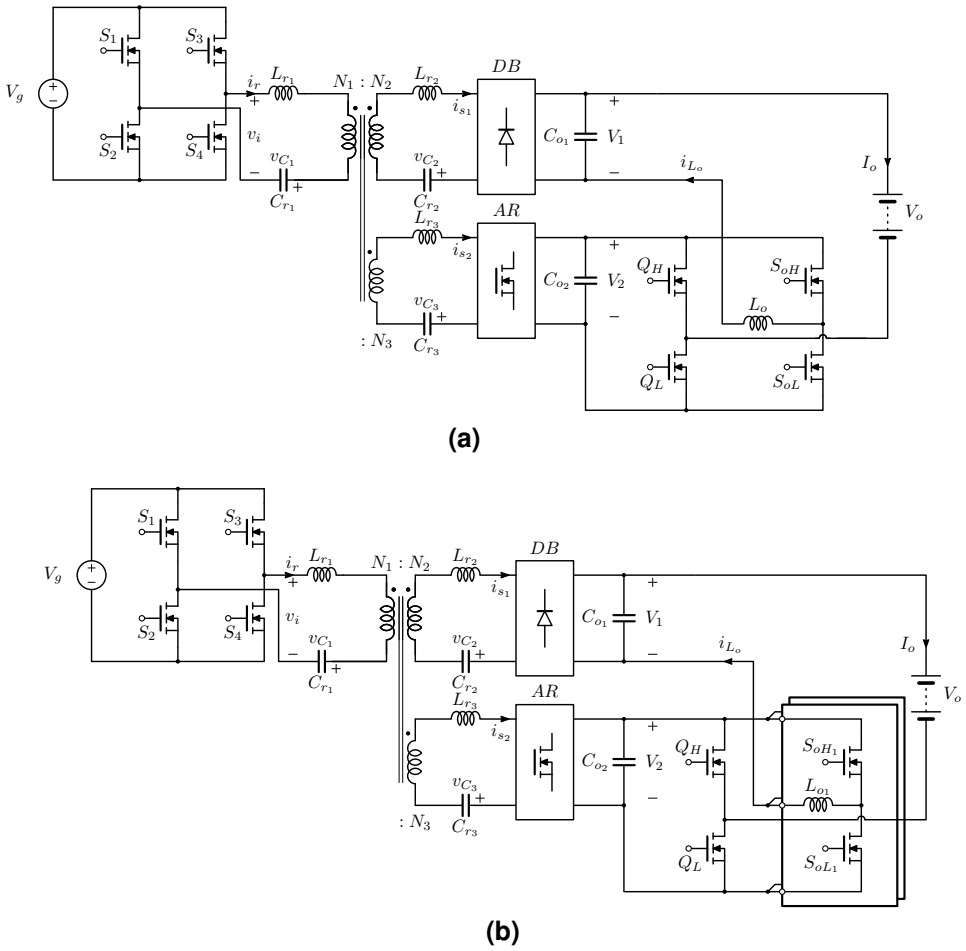


Figure 4.3: (a) DCX-CLLC & input-parallel output-series (IPOS) PPP converter; (b) DCX-CLLC & interleaved IPOS PPP converter.

variant is simulated using both $650\,\mathrm{V}$ SiC and GaN switching devices. Active rectification is not considered for this topology. In the subsequent Sect. 4.3.4 and Sect. 4.4.4, the design and efficiency analysis of each of these DCX-LLC & TBB variants are presented.

4.3 Design of the Considered Topologies

In this section, the design of the four dc-dc converter topologies in Sect. 4.2 is detailed. The design parameters are set in accordance with the specifications outlined in Table 4.1 and the requirements for EV applications specified in Sect. 1.3. The input voltage to the dc-dc converter is assumed supplied by a PFC stage at $800\,\mathrm{V}$. The battery voltage operates in the range of 250 - $500\,\mathrm{V}$, which is also the output voltage of the converter. The power ratings

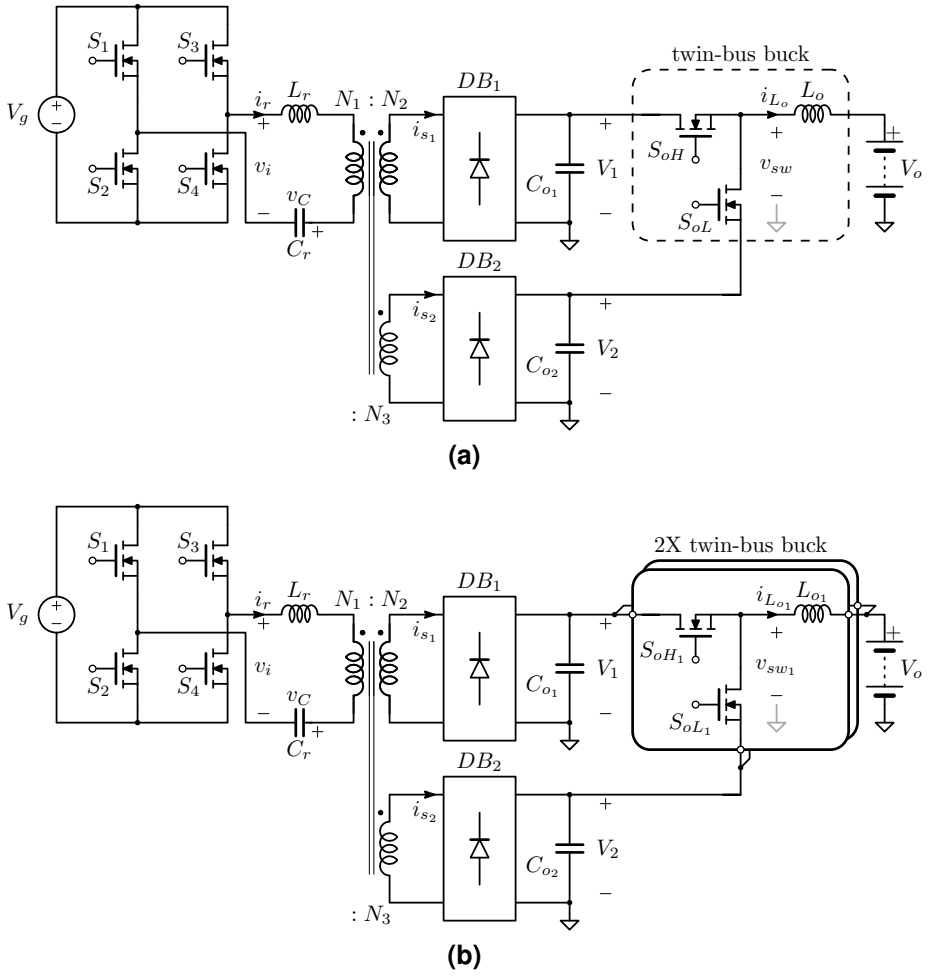


Figure 4.4: (a) DCX-LLC & TBB converter; and (b) DCX-LLC & interleaved TBB converter.

Table 4.1: Converters design parameters.

Parameter	**Symbol**	**Value**	
Input voltage	V_g	800	V
Output voltage	V_o	250 - 500	V
Nominal output voltage	V_o^{nom}	400	V
Maximum output current	$I_o^{\max}$	25	A
Nominal power	P_o^{nom}	10	kW
Switching frequency	f_s	200	kHz

Table 4.2: Full-bridge LLC converter parameters.

Parameter	Symbol	Value	
Resonance frequency	f_r	200	kHz
Switching frequency range	$f_s^{\min}$, $f_s^{\max}$	130 - 400	kHz
Turns ratio N_p/N_s	n	2	-
Number of windings pri.	N_p	24	-
Number of windings sec.	N_s	12	-
Magnetizing inductance	L_m	150	µH
Transformer	Core: PQ65/60, material: N87 [113]		
Litz wire	Pri: $2\times(825 \times 50\mu\text{m})$, sec: $4\times(825 \times 50\mu\text{m})$		
Windings ac resistance (pri.)	$R_{ac}(f_r)$	29	mΩ
Resonant inductor	L_r	2×16	µH
Number of windings	N	15	-
Inductor	$2\times$ Core: PQ40/40, material: N97 [107]		
Litz wire	$3\times(825 \times 50\mu\text{m})$		
Windings ac resistance	$R_{ac}(f_r)$	27.9	mΩ
Resonant capacitance	C_r	19.8	nF
S_1, S_2, S_3, S_4	IXFB40N110Q3, 1.1 kV, 260 mΩ Si MOSFETs [114]		
	G3R30MT12K, 1.2 kV, 30 mΩ SiC MOSFETs [115]		
Diode rectifier	C5D50065D, 650 V SiC diodes [102]		
Active rectifier	GPI65060DFN, 650 V, 25 mΩ GaN HEMTs [116]		

of the converter modules are chosen 10 kW to ease the realization of the demonstration prototype. Notably, in practical applications, multiple modules rated 10 - 75 kW are often connected in parallel to achieve required power ratings [17]. The switching frequency has been set to the nominal value of 200 kHz. Additionally, the output current limit for the converter, selected at the nominal power and voltage is set to 25 A.

In the following subsections, design the details for each of the four topologies, including the FB-LLC, BB-LLC, DCX-CLLC & PPP, and DCX-LLC & TBB are presented. The parameters summarized in Table 4.1 are considered.

4.3.1 Full-Bridge LLC

The input and output voltage levels, as detailed in Table 4.1, guide the design choices of the FB-LLC converter. Ensuring resonance frequency equal to the switching frequency

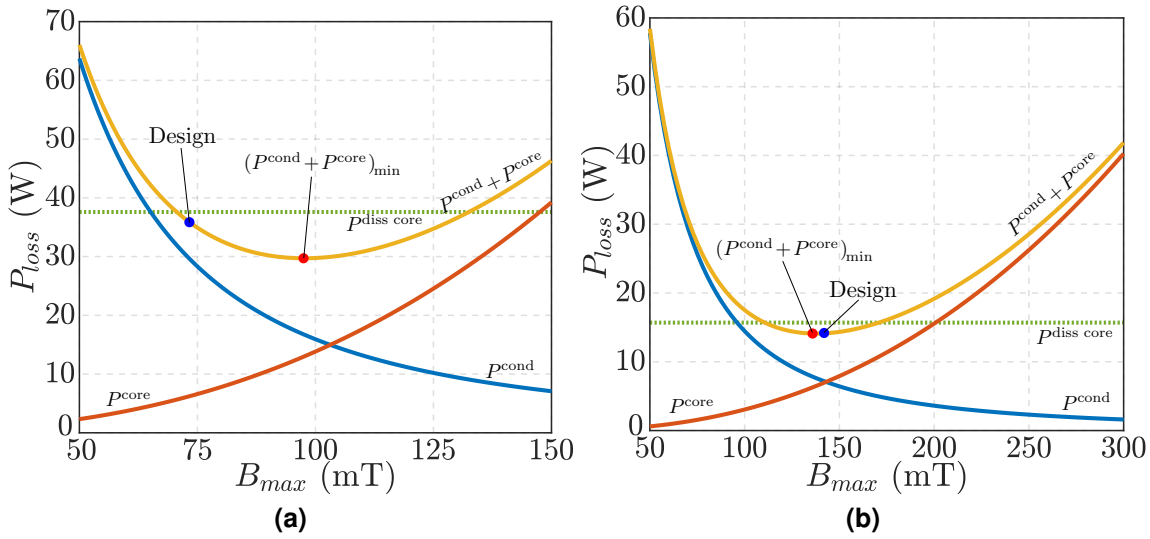


Figure 4.5: (a) Transformer design; and (b) inductor design of the LLC with parameters in Table 4.2.

(i.e., $f_r = f_s$), the transformer turns ratio is set to $n = N_p/N_s = 2$. Following the transformer design procedure outlined in Sect. 3.3.3, a total losses diagram is constructed as displayed in Fig. 4.5a. Under nominal conditions (i.e., $V_o = 400\,\text{V}$ and $P_o = 10\,\text{kW}$), total losses of 30 W are indicated, with $B_{\text{opt}} = 89\,\text{mT}$ at the minimum loss point, according with Fig. 4.5a. At this point, losses are evenly distributed between windings and core. It's notable that the chosen design point, as shown in Fig. 4.5a, is more conservative in terms of core losses due to a trade-off between available space and discrete conductor sections. Then, the designed transformer presents $N_p = 24$ primary windings and $N_s = 12$ secondary windings, with current density $J_0 = 4.3\text{A}/\,\text{mm}^2$. Litz wire specifications are chosen as 2 parallel litz wires $825 \times 50\,\mu\text{m}$ for the primary and 4 in parallel for the secondary side. The chosen core, satisfying maximum thermal dissipation requirements as in (3.24), is the PQ65/60 with material N87 [113]. The calculated ac resistance with (3.4) referred to the primary side is reported in Table 4.2, together with the summary of the FB-LLC transformer specifications.

To achieve comprehensive output voltage regulation across varying load conditions, the resonant inductor is set to $L_r = 32\,\mu\text{H}$. This selection ensures the converter to regulate the maximum output voltage $V_o = 500\,\text{V}$ while providing extensive regulation coverage at minimum output voltage. The maximum switching frequency, limiting the gain at mini-

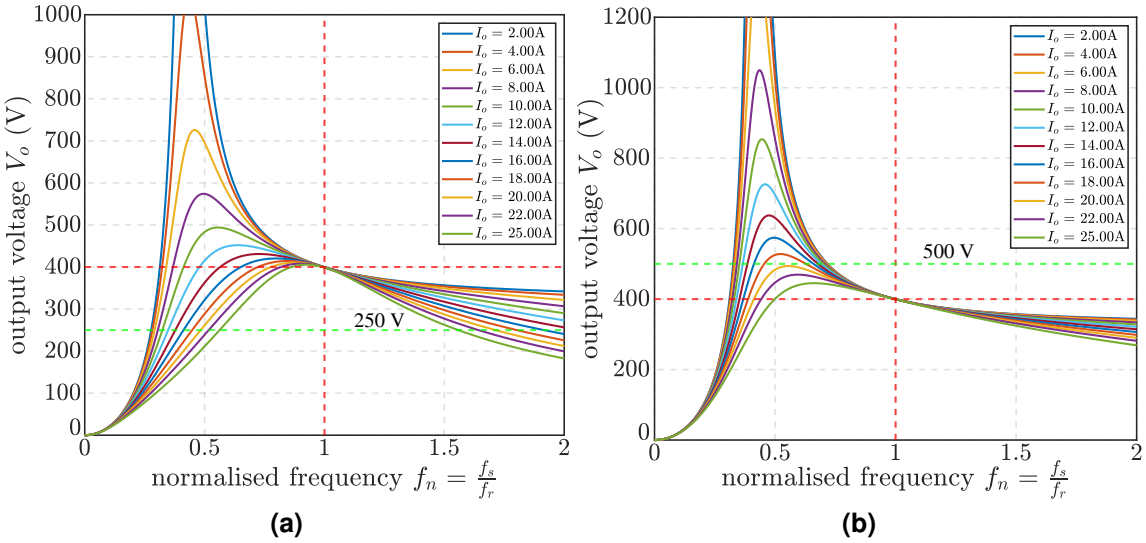


Figure 4.6: Intrinsic voltage gain of the LLC converter with parameters in Table 4.2 determined with first harmonic approximation (FHA). (a) $V_o = 250\,\mathrm{V}$; and (b) $V_o = 500\,\mathrm{V}$. Being $f_s < 400\,\mathrm{kHz}$, V_o can be regulated at 250 V only if $I_o > 14\,\mathrm{A}$.

mum output voltage, is fixed at $400\,\mathrm{kHz}$. This can be observed in Fig. 4.6, illustrating the LLC intrinsic voltage gain variations at minimum and maximum output voltage with varying load current for the chosen inductance. The resonant capacitor value is deduced from the chosen inductance and established resonance frequency, as listed in Table 4.2.

The LLC resonant inductor is designed as a series combination of two inductors, each with a value of $L_{r_1} = L_{r_2} = 16\,\mu\mathrm{H}$, following the design methodology detailed in Sect. 3.3.3. The resulting design, shown in Fig. 4.5b, employs $N = 15$ windings for each inductor, PQ40/40 cores made of material N97 [107], and a configuration of 3 litz wires $825 \times 50\,\mu\mathrm{m}$ in parallel. The ac resistance of the inductor determined by (3.4) is reported in Table 4.2, with the summary of inductors parameters.

The devices implemented in the three technology variants introduced in Sect. 4.2.1 are described herein. For the input stage of the LLC, $1200\,\mathrm{V}$ Si (first variant) or $1200\,\mathrm{V}$ SiC-based MOSFETs (second variant) are chosen, providing a proper margin on the input voltage. The passive rectifier diodes are $650\,\mathrm{V}$ SiC-based devices, considering the maximum output voltage of $500\,\mathrm{V}$. In the third topology variant, the active rectifier bridge implements $650\,\mathrm{V}$ GaN devices. Further details can be found in Table 4.2.

The FB-LLC converter, designed with the summarized parameters in Table 4.2, is sim-

Table 4.3: BB-LLC converter parameters.

Parameter	Symbol	Value	
Resonance & sw. frequencies	f_r, f_s	200	kHz
Intermediate bus voltage	V_b	500 - 1000	V
Turns ratio N_p/N_s	n	1	-
Number of windings pri.	N_p	13	-
Number of windings sec.	N_s	13	-
Magnetizing inductance	L_m	150	µH
Transformer	Core: PQ65/60, material: N87 [113]		
Litz wire	$4\times(825 \times 50\mu\text{m})$ for both pri. and sec.		
Windings ac resistance (pri.)	$R_{ac}(f_r)$	37.5	mΩ
Buck-boost inductor	L_b	2×8	µH
Number of windings	N	12	-
Inductor	$2\times$ Core: PQ40/40, material: N97 [107]		
Litz wire	$4\times(825 \times 50\mu\text{m})$		
Windings ac resistance	$R_{ac}(f_r)$	13.7	mΩ
Leakage inductance	L_r	2.4	µH
Resonant capacitance	C_r	264	nF
S_{aH}, S_{aL}, S_{bH}, S_{bL}	G3R30MT12K, 1.2 kV, 30 mΩ SiC MOSFETs [115]		
Diode rectifier	C5D50065D, 650 V SiC diodes [102]		

ulated with the results reported in Sect. 4.4.1.

4.3.2 Buck-Boost LLC

Converter Operation. The BB-LLC converter topology illustrated in Fig. 4.2a comprises a primary four-switch buck-boost stage followed by a secondary half-bridge LLC (HB-LLC) stage. This latter stage, operating at resonance (i.e., $f_s = f_r$), behaves as a DCX. Notably, this DCX stage shares two switches with the pre-regulation stage, enabling a reduction in rms current through these switches. Consequently, the duty-cycle of this shared leg (i.e., leg b in Fig. 4.2a) is fixed at 50%. By applying the volt-second balance principle to L_b, the voltage gain of the pre-regulation stage can be expressed as:

$$M_{BB} = \frac{V_b}{V_g} = 2d \tag{4.1}$$

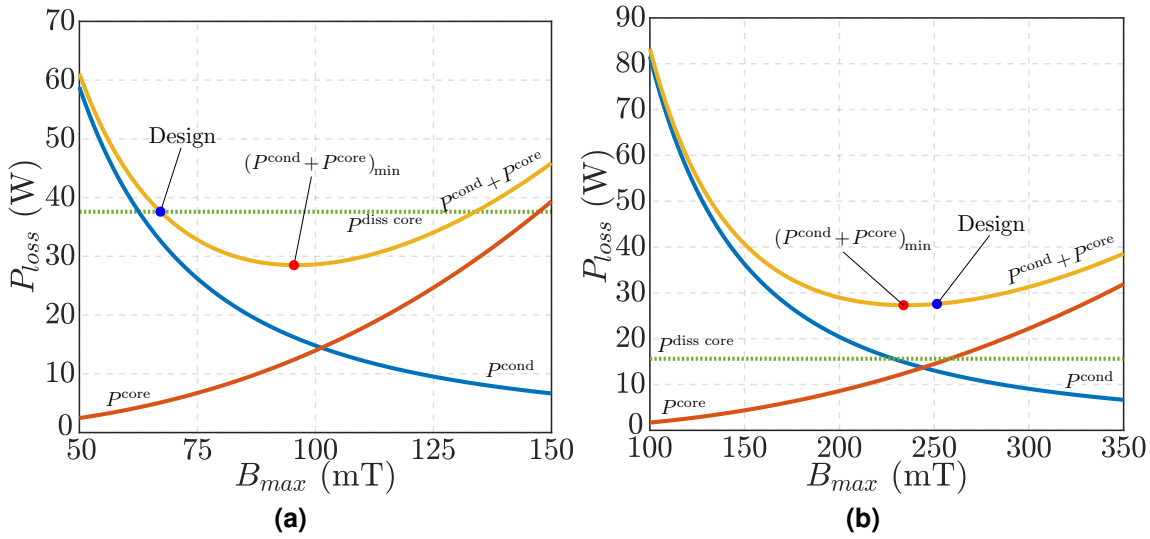


Figure 4.7: (a) Transformer design; and (b) inductor design of the BB-LLC with parameters in Table 4.3. Forced air flow to increase thermal dissipation capability of the inductors is needed.

where d is the duty-cycle of the input leg a, used to regulate the intermediate leg voltage V_b. The voltage gain of an HB-LLC in DCX operation is:

$$M_{HB-LLC_{DCX}} = \frac{V_o}{V_b} = \frac{1}{2n} \tag{4.2}$$

where n is the transformer turns ratio. The overall voltage gain of the BB-LLC can be determined as:

$$M_{BB-LLC} = \frac{V_o}{V_g} = \frac{d}{n} \tag{4.3}$$

Considering the requirements in Table 4.1, the transformer turns ratio should be set as $n = N_p/N_s = 1$.

Converter Design. Following the transformer design procedure detailed in Sect. 3.3.3, a total losses diagram is constructed and shown in Fig. 4.7a. This P-B plot reveals a total loss of 28 W under nominal conditions ($V_o = 400\,\text{V}$ and $P_o = 10\,\text{kW}$), with the minimum loss point at $B_{\text{opt}} = 95\,\text{mT}$, where losses are evenly distributed between windings and the core. The resulting designed transformer comprises $N_p = 13$ primary windings and $N_s = 13$ secondary windings, with a current density of $J_0 = 4.3\,\text{A}/\,\text{mm}^2$. Litz wire specifications include 4 parallel litz wires of $825 \times 50\,\mu\text{m}$ for both primary and secondary

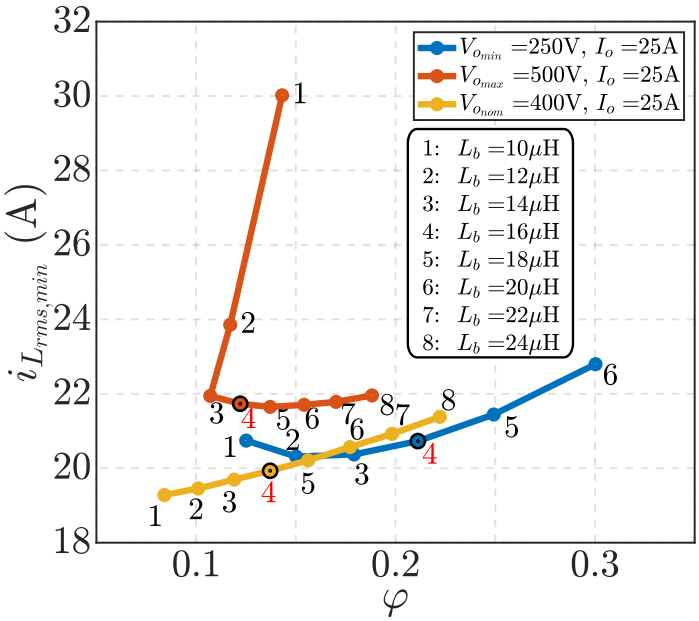


Figure 4.8: Selection of the optimal inductance value L_b at maximum output current. $L_b = 16\,\mu\text{H}$ is a trade-off for the minimization of the rms current in the whole range. ZVS is always achieved for each point.

side. The chosen core, meeting the maximum thermal dissipation requirements as defined in (3.24), is the PQ65/60 with N87 material [113]. The calculated ac resistance referred to the primary side, using (3.4), is reported in Table 4.3 as part of the BB-LLC transformer specifications.

The leakage inductance of the transformer, which serves as the resonant inductance of the LLC stage L_r can be determined from (3.26). The resonant capacitor value is derived from the transformer leakage inductance and established resonance frequency, as listed in Table 4.3.

To achieve a proper magnitude of the switched current for satisfying ZVS conditions throughout the output voltage range, the inductor value of the buck-boost stage should be appropriately set. For wide output voltage range ZVS and minimal rms circulating currents, the resonant inductor is set to $L_r = 16\,\mu\text{H}$. In Fig. 4.8, the rms current of different inductor values L_b at boundary conditions for ZVS (i.e., at the minimum phase-shift φ between the two legs that minimizes the rms current for a given inductance) is depicted. The BB-LLC inductor L_b is designed as a series combination of two inductors, each with a value of $L_{r_1} = L_{r_2} = 8\,\mu\text{H}$, following the design methodology detailed in Sect. 3.3.3.

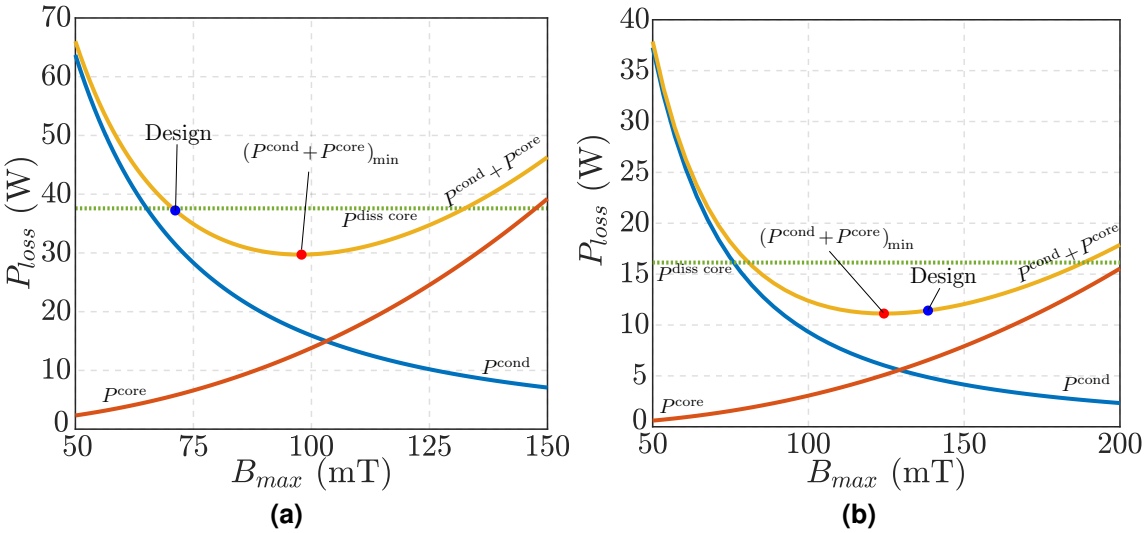


Figure 4.9: (a) Transformer design; and (b) inductor design of the CLLC & IPOS PPP with parameters in Table 4.4.

The resulting design, shown in Fig. 4.7b, employs $N = 12$ windings for each inductor, PQ40/40 cores made of material N97 [107], and a configuration of 4 litz wires of $825 \times 50\,\mu\text{m}$ in parallel. Notably, the designed inductor requires forced airflow to enhance the component's thermal dissipation. This emerges from Fig. 4.7b, showing that the power dissipation capacity in stationary conditions, as in (3.24), needs to be increased. The ac resistance of the inductor determined using (3.4) is reported in Table 4.3, along with a summary of inductor parameters.

The devices implemented in the two topology variants introduced in Sect. 4.2.2 are described herein. For both the topology variants, interleaved buck-boost or not, $1200\,\text{V}$ SiC MOSFETs are used, providing a margin on the bus voltages V_g and V_b. The passive rectifier diodes are $650\,\text{V}$ SiC-based devices, considering the maximum output voltage of $500\,\text{V}$. Further details can be found in Table 4.3.

In conclusion, the BB-LLC converter, designed with the summarized parameters in Table 4.3, has been subjected to simulation, and the results are presented in Sect. 4.4.2.

Table 4.4: DCX-CLLC & IPOS PPP converter parameters.

Parameter	**Symbol**	**Value**	
CLLC resonance & sw. freq.	f_r, f_s	200	kHz
PPP sw. frequency range	f_{s_o}	50 - 400	kHz
Intermediate bus voltage	V_1	375	V
Intermediate bus voltage	V_2	125	V
Turns ratio N_2/N_1	n_1	0.458	-
Turns ratio N_3/N_1	n_2	0.167	-
Number of windings pri.	N_1	24	-
Number of windings sec.1	N_2	11	-
Number of windings sec.2	N_3	4	-
Magnetizing inductance	L_m	200	µH
Transformer	Core: PQ65/60, material: N87 [113]		
Litz wire	Pri: $2\times(825 \times 50\mu\text{m})$, Sec.s: $4\times(825 \times 50\mu\text{m})$		
Windings ac resistance (pri.)	$R_{ac}(f_r)$	72.5	mΩ
Buck inductor	L_o	30	µH
Number of windings	N	20	-
Inductor	Core: PQ40/40, material: N97 [107]		
Litz wire	$3\times(825 \times 50\mu\text{m})$		
Windings ac resistance	$R_{ac}(f_r)$	31.6	mΩ
Leakage inductance	L_r	8	µH
Resonant capacitance	C_r	78	nF
S_1, S_2, S_3, S_4	G3R30MT12K, 1.2 kV, 30 mΩ SiC MOSFETs [115]		
Diode rectifier DB	C5D50065D, 650 V SiC diodes [102]		
S_{oH}, S_{oL}; Q_H, Q_L; AR act. rect.	EPC2215, 200 V, 8 mΩ GaN FETs [117]		

4.3.3 CLLC & Partial-Power Post-Regulator

Converter Operation. The CLLC & IPOS PPP converter topology, as shown in Fig. 4.3a, comprises a primary isolation stage based on an CLLC resonant converter and a secondary PPP stage based on a buck converter. The CLLC stage behaves as a high-efficiency two-output DCX (i.e., $f_s = f_r$), generating secondary voltages V_1 and V_2. The PPP stage is responsible for regulating the output voltage. It is connected in series with the secondary V_1 of the DCX-CLLC and is supplied by the secondary V_2. The two additional switches, Q_H and Q_L, enable the use of low voltage devices in the PPP stage. Specifically, when $V_o > V_1$, Q_L is turned on and the voltage stress on such devices is $V_o^{\max} - V_1$. When $V_o < V_1$, Q_H is turned on and the voltage stress becomes $V_1 - V_o^{\min}$. In this scenario, reverse power flow occurs in the DB_2 rectifier, necessitating active rectification in this specific rectifier. The voltage stress is minimized when:

$$V_1 = \frac{V_o^{\max} - V_o^{\min}}{2} \tag{4.4}$$

As a result, V_1 represents the mean output voltage range, allowing the PPP stage to operate with reduced voltage stress. To meet the specifications outlined in Table 4.1, the transformer turns ratio can be set as follows:

$$\begin{aligned} n_1 &= \frac{N_2}{N_1} = \frac{V_1}{V_g} = \frac{V_o^{\max} + V_o^{\min}}{2} \\ n_2 &= \frac{N_3}{N_1} = \frac{V_2}{V_g} = V_o^{\max} - V_1 = V_1 - V_o^{\min} \end{aligned} \tag{4.5}$$

Converter Design. Following the transformer design procedure explained in Sect. 3.3.3, a total losses diagram is formulated and depicted in Fig. 4.9a. This P-B plot indicates total losses of $30\,\mathrm{W}$ under nominal conditions (i.e., $V_o = 400\,\mathrm{V}$ and $P_o = 10\,\mathrm{kW}$), with the minimum loss point at $B_{\mathrm{opt}} = 97\,\mathrm{mT}$, resulting in a balanced distribution of losses between the windings and the core. The resulting transformer design encompasses $N_1 = 24$ primary windings and $N_2 = 11$ and $N_3 = 4$ secondary windings, with a current density of $J_0 = 4.4\,\mathrm{A/mm^2}$. Litz wire specifications include 2 parallel litz wires of $825 \times 50\,\mu\mathrm{m}$ for primary and 4 parallel same litz wires for secondaries. The selected core, which meets

the maximum thermal dissipation requirements as outlined in (3.24), is the PQ65/60 with material N87 [113]. The calculated ac resistance referred to the primary side, using (3.4), is presented in Table 4.4 as part of the CLLC & PPP transformer specifications.

The leakage inductance of the transformer, which serves as the resonant inductance of the CLLC stage, L_r, can be determined using (3.26). The resonant capacitor value is derived from the transformer's leakage inductance and the established resonance frequency, as listed in Table 4.4.

To achieve the proper magnitude of the switched current and ensure ZVS conditions throughout the output voltage range, the inductor value for the buck PPP stage must be determined. The switching frequency of the buck f_{s_o} is modulated and used to help in achieving ZVS. To cover a wide output voltage range with ZVS and minimal rms circulating currents, the output inductor is set to $L_o = 30\,\mu\mathrm{H}$. The design of inductor L_o follows the methodology detailed in Sect. 3.3.3. The resulting design, illustrated in Fig. 4.9b, employs $N = 20$ windings, PQ40/40 core made of material N97 [107], and a configuration of 3 litz wires of $825 \times 50\,\mu\mathrm{m}$ in parallel. The ac resistance of the inductor determined using (3.4) is reported in Table 4.4, along with a summary of inductor parameters.

The devices implemented in the two topology variants introduced in Sect. 4.2.3 are described herein. $1200\,\mathrm{V}$ SiC MOSFETs are chosen for the input CLLC. The main passive rectifier diodes are $650\,\mathrm{V}$ SiC-based devices, considering the intermediate voltage V_1. For both topology variants, interleaved PPP stage or not, and for the active rectifier DB_2, $200\,\mathrm{V}$ GaN field-effect transistor (FET) are chosen. Further details can be found in Table 4.4.

In conclusion, the CLLC & IPOS PPP converter, designed with the summarized parameters in Table 4.4, has been subjected to simulation, and the results are presented in Sect. 4.4.3.

4.3.4 LLC & Twin-Bus Buck Post-Regulator

Converter Operation. The DCX-LLC & TBB converter topology, depicted in Fig. 4.4a, comprises a primary isolation stage based on an LLC resonant converter and a secondary post-regulation stage based on a buck converter. The LLC stage functions as a high-

Table 4.5: DCX-LLC & TBB converter parameters.

Parameter	**Symbol**	**Value**	
LLC resonance & sw. freq.	f_r, f_s	200	kHz
TBB sw. frequency range	f_{s_o}	50 - 400	kHz
Intermediate bus voltage	V_1	500	V
Intermediate bus voltage	V_2	250	V
Turns ratio N_2/N_1	n_1	0.625	-
Turns ratio N_3/N_1	n_2	0.292	-
Number of windings pri.	N_1	24	-
Number of windings sec.1	N_2	15	-
Number of windings sec.2	N_3	7	-
Magnetizing inductance	L_m	200	µH
Transformer	Core: PQ65/60, material: N87 [113]		
Litz wire	Pri: $2\times(825 \times 50\mu m)$, Sec.s: $3\times(825 \times 50\mu m)$		
Windings ac resistance (pri.)	$R_{ac}(f_r)$	82.8	mΩ
Buck inductor	L_o	30	µH
Number of windings	N	20	-
Inductor	Core: PQ40/40, material: N97 [107]		
Litz wire	$3\times(825 \times 50\mu m)$		
Windings ac resistance	$R_{ac}(f_r)$	31.6	mΩ
Leakage inductance	L_r	8	µH
Resonant capacitance	C_r	78	nF
S_1, S_2, S_3, S_4	G3R30MT12K, 1.2 kV, 30 mΩ SiC MOSFETs [115]		
Diode rectifiers	C5D50065D, 650 V SiC diodes [102]		
S_{oH}, S_{oL}	C3M0025065K, 650 V, 25 mΩ SiC MOSFETs [118]		
	GPI65060DFN, 650 V, 25 mΩ GaN HEMTs [116]		

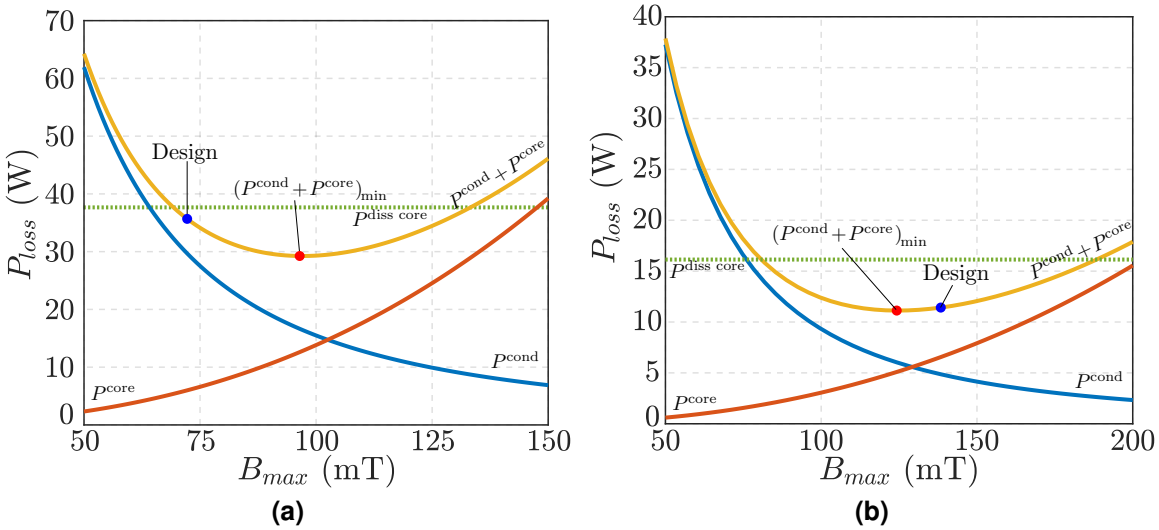


Figure 4.10: (a) Transformer design; and (b) inductor design of the LLC & TBB with parameters in Table 4.5.

efficiency two-output DCX ($f_s = f_r$), generating secondary voltages V_1 and V_2. The TBB post-regulation stage is responsible for output voltage regulation, with its voltage stress, i.e., $V_1 - V_2$, being lower than the output voltage V_o. The output voltage V_o is a function of the TBB input voltages V_1 and V_2, and the duty-cycle d of the upper switch S_{oH}:

$$V_o = dV_1 + (1-d)V_2 \tag{4.6}$$

Minimizing the voltage stress on the TBB switching devices is achieved by maximizing the duty-cycle excursion. To satisfy the specifications listed in Table 4.1, the transformer turns ratio can only be set as follows:

$$\begin{aligned} n_1 &= \frac{N_2}{N_1} = \frac{V_1}{V_g} = \frac{V_o^{\max}}{V_g} \\ n_2 &= \frac{N_3}{N_1} = \frac{V_2}{V_g} = \frac{V_o^{\min}}{V_g} \end{aligned} \tag{4.7}$$

Converter Design. Following the transformer design procedure explained in Sect. 3.3.3, a total losses diagram is formulated and depicted in Fig. 4.10a. This P-B plot indicates total losses of 29 W under nominal conditions ($V_o = 400\,\text{V}$ and $P_o = 10\,\text{kW}$), with the minimum loss point at $B_{\text{opt}} = 96\,\text{mT}$, resulting in an even distribution of losses between windings

and the core. The resulting transformer design encompasses $N_1 = 24$ primary windings and $N_2 = 15$ and $N_3 = 7$ secondary windings, with a current density of $J_0 = 4.2\mathrm{A}/\,\mathrm{mm}^2$. Litz wire specifications include 2 parallel litz wires of $825 \times 50\,\mu\mathrm{m}$ for primary and 3 parallel same litz wires for secondaries. The selected core, which meets the maximum thermal dissipation requirements as outlined in (3.24), is the PQ65/60 with N87 material [113]. The calculated ac resistance referred to the primary side, using (3.4), is presented in Table 4.5 as part of the DCX-LLC & TBB transformer specifications.

The leakage inductance of the transformer, which serves as the resonant inductance of the LLC stage, L_r, can be determined using (3.26). The resonant capacitor value is derived from the transformer's leakage inductance and the established resonance frequency, as listed in Table 4.5.

To achieve the proper magnitude of the switched current and ensure ZVS conditions throughout the output voltage range, the inductor value of the TBB stage must be determined. The switching frequency of the buck, f_{s_o}, is modulated within the specified range to assist in achieving ZVS. To cover a wide output voltage range while maintaining ZVS and minimal rms circulating currents, the output inductor is set to $L_o = 30\,\mu\mathrm{H}$. The inductor L_o is designed following the design methodology detailed in Sect. 3.3.3. The resulting design, illustrated in Fig. 4.10b, employs $N = 20$ windings, PQ40/40 core made of N97 material [107], and a configuration of 3 litz wires of $825 \times 50\,\mu\mathrm{m}$ in parallel. The ac resistance of the inductor determined using (3.4) is reported in Table 4.5, along with a summary of inductor parameters.

The devices implemented in the three topology variants introduced in Sect. 4.2.4 are described herein. $1200\,\mathrm{V}$ SiC MOSFETs are chosen for the input LLC. The passive rectifier diodes are $650\,\mathrm{V}$ SiC-based devices. In the first two variants $650\,\mathrm{V}$ SiC MOSFETs are used in the buck post-regulation stage. Notably, the maximum voltage stress on the devices is about $250\,\mathrm{V}$, and the chosen devices have the closest voltage rating. The third, interleaved, variant implements $650\,\mathrm{V}$ GaN FETs. Further details can be found in Table 4.4.

In conclusion, the LLC & TBB converter, designed with the summarized parameters in Table 4.5, has been subjected to simulation, and the results are presented in Sect. 4.4.4.

Table 4.6: Component count of evaluated LLC topologies.

Topology variant	Quantity			
	Switch	Diode	Transf.	Induct.
Si-based LLC	4	4	1	2
SiC-based LLC	4	4	1	2
SiC-based LLC with GaN-based active rect.	8	0	1	2

4.4 Comparative Analysis

In this section, the simulation results obtained by implementing the converter topologies described in Sect. 4.2 using the design parameters outlined in Sect. 4.3 are presented. The simulations are conducted using a PLECS®/Simulink® + MATLAB® environment. The circuit configurations for the different topology variants and WBG technology are built in PLECS®, and the simulations are performed to assess their performance and efficiency.

To evaluate the efficiency and loss distribution of each converter topology, the breakdown of the losses is determined accordingly to Sect. 3.4. This allowed to identify the contributions of different components to the overall losses and optimize the design accordingly. As an example, the implementation of the LLC simulation setup in the PLECS®/Simulink®+ MATLAB® environment is provided in App. C. This example demonstrates how the circuit models, including the proposed topology variants and associated components, are built and how the simulations are executed.

In the following, the simulation results are presented for each converter topology and a comparative analysis is performed to evaluate their performance an component count.

4.4.1 Full-Bridge LLC

Efficiency performance results of the Si-based, SiC-based, and SiC-based FB-LLC with active rectification are presented in Fig. 4.11. The breakdown of the losses is illustrated in Fig. 4.12. The schematics of the topologies are introduced in Sect. 4.2.1, along with the design parameters discussed in Sect. 4.3.1. The component count for all three implemented topologies is provided in Table 4.6, indicating the number of diodes, MOSFETs, transformers, and inductors utilized in each variant. Notably, the implementation of the WBG

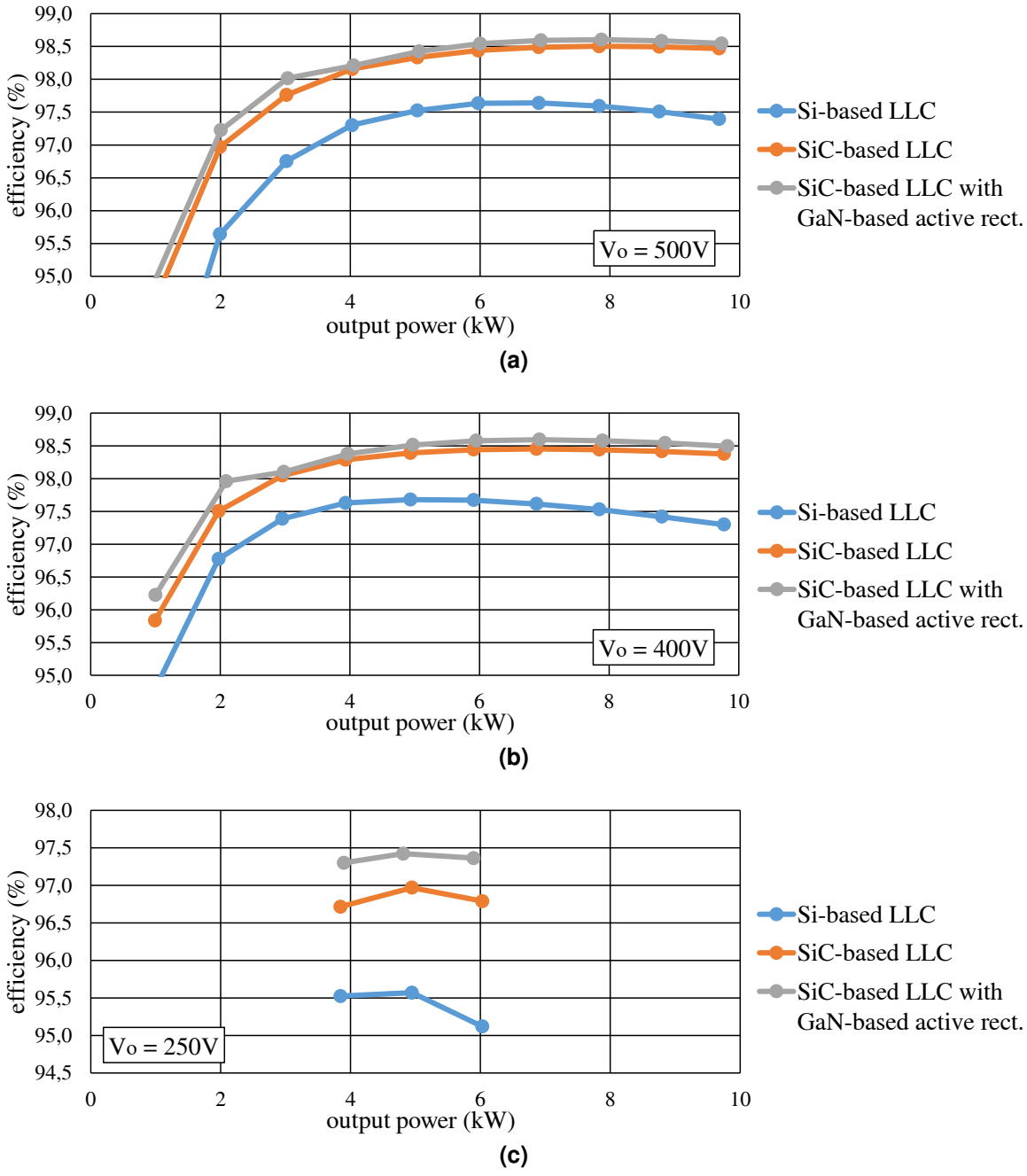


Figure 4.11: Efficiency comparison between Si-based LLC, SiC-based LLC and SiC-based LLC with GaN active rectifier. (a) $V_o = 500\,\mathrm{V}$; (b) $V_o = 400\,\mathrm{V}$; and (c) $V_o = 250\,\mathrm{V}$. Topologies in Sect. 4.2.1 and design specifications in Table 4.2.

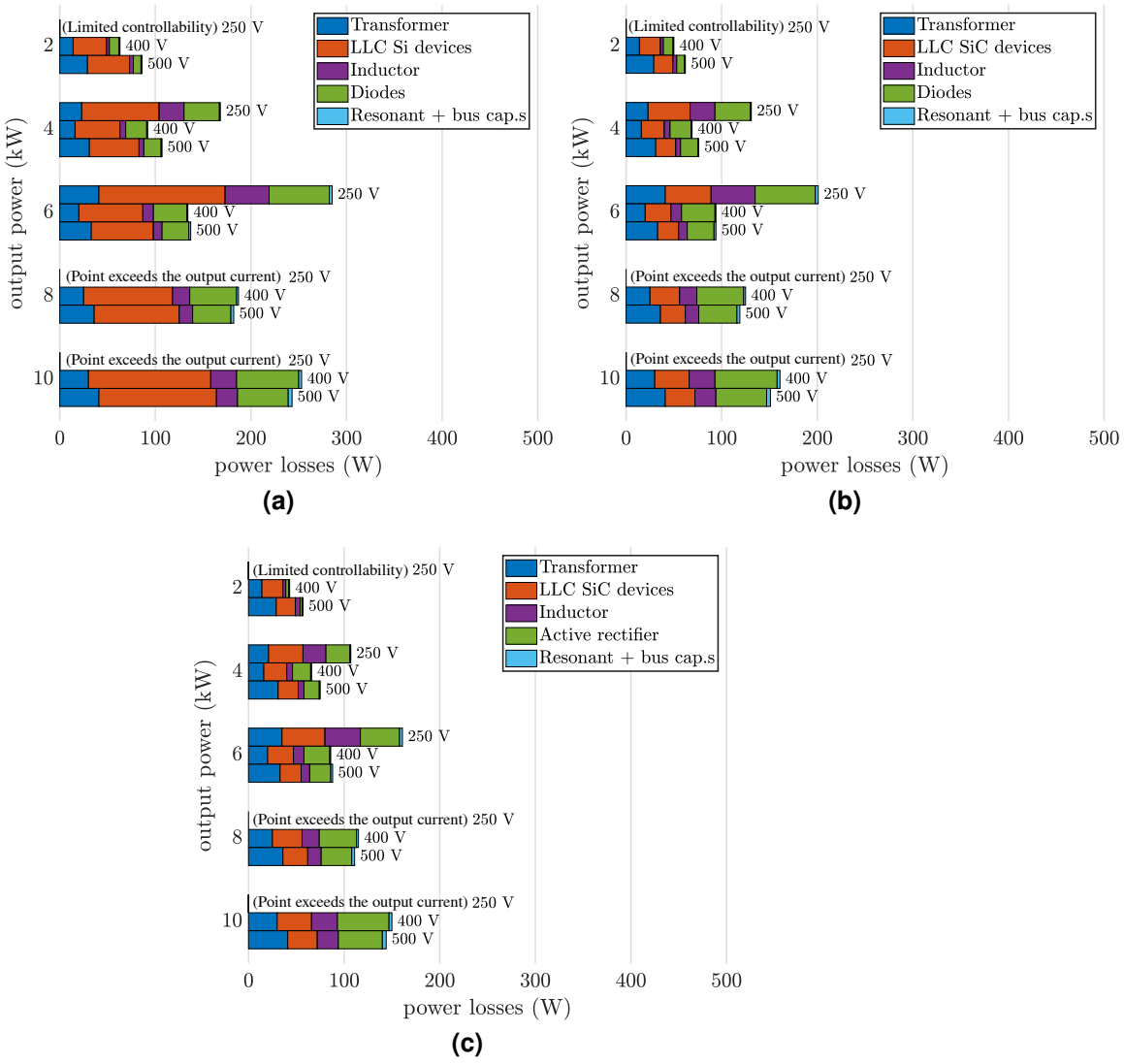


Figure 4.12: Loss breakdown at different output power and minimum, nominal, and maximum output voltages. FB-LLC topologies with efficiency profiles in Fig. 4.11. (a) Si-based LLC, (b) SiC-based LLC, (c) SiC-based LLC with GaN-based active rectification. Topologies in Sect. 4.2.1 and design specifications in Table 4.2.

Table 4.7: Component count of evaluated BB-LLC topologies.

Topology variant	Quantity			
	Switch	Diode	Transf.	Induct.
SiC-based BB-LLC	4	4	1	2
Interleaved SiC-based BB-LLC	6	4	1	2

materials demonstrates significantly improved performance compared to Silicon. This is evident in the loss breakdown depicted in Fig. 4.12.

In general, frequency-modulated FB-LLC converter has low-efficiency performances in the minimum output voltage range (refer to Fig. 4.11c) due to the limited voltage gain and the higher switching frequencies. Furthermore, the low Q-factor in the light-load region and minimum output voltage pose a lower limit in the transferred power due to the upper limit in the switching frequency.

While the SiC-based LLC with active rectification showcases the highest performance, its advantages over the passive rectification-based topology are not significantly pronounced. The latter represents a balanced trade-off between efficiency and implementation cost (component count). Furthermore, the passive rectification-based design serve as a benchmark for comparison with other multi-stage topologies in the subsequent subsections.

4.4.2 Buck-Boost LLC

Efficiency performance results of the SiC-based LLC, and SiC-based and interleaved SiC-based BB-LLC are presented in Fig. 4.13. The breakdown of the losses is illustrated in Fig. 4.14. The schematics of the topologies are introduced in Sect. 4.2.2, along with the design parameters discussed in Sect. 4.3.2. The component count for all three implemented topologies is provided in Table 4.7, indicating the number of diodes, MOSFETs, transformers, and inductors utilized in each variant.

The BB-LLC, compared with the traditional LLC, demonstrates favorable performance overall. At nominal voltage level, efficiencies are nearly overlapping. However, at maximum output voltage, the efficiency decreases due to losses in the pre-regulation stage. This is also visible in Fig. 4.14. On the other hand, at minimum output voltage, the BB-LLC ex-

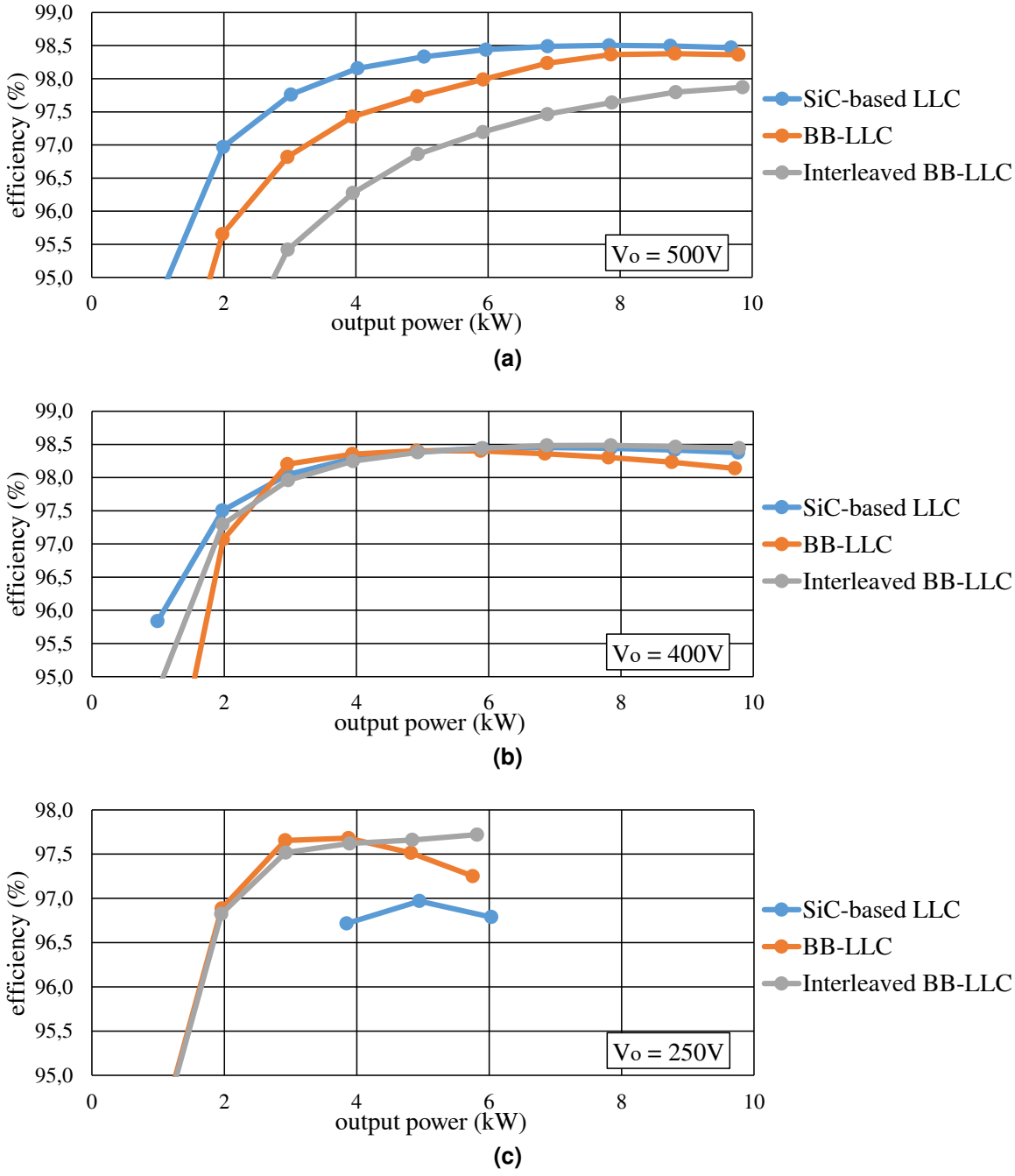


Figure 4.13: Efficiency comparison between SiC-based LLC, SiC-based BB-LLC and interleaved SiC-based BB-LLC. (a) $V_o = 500\,\mathrm{V}$; (b) $V_o = 400\,\mathrm{V}$; and (c) $V_o = 250\,\mathrm{V}$. Topologies in Sect. 4.2.2 and design specifications in Table 4.3.

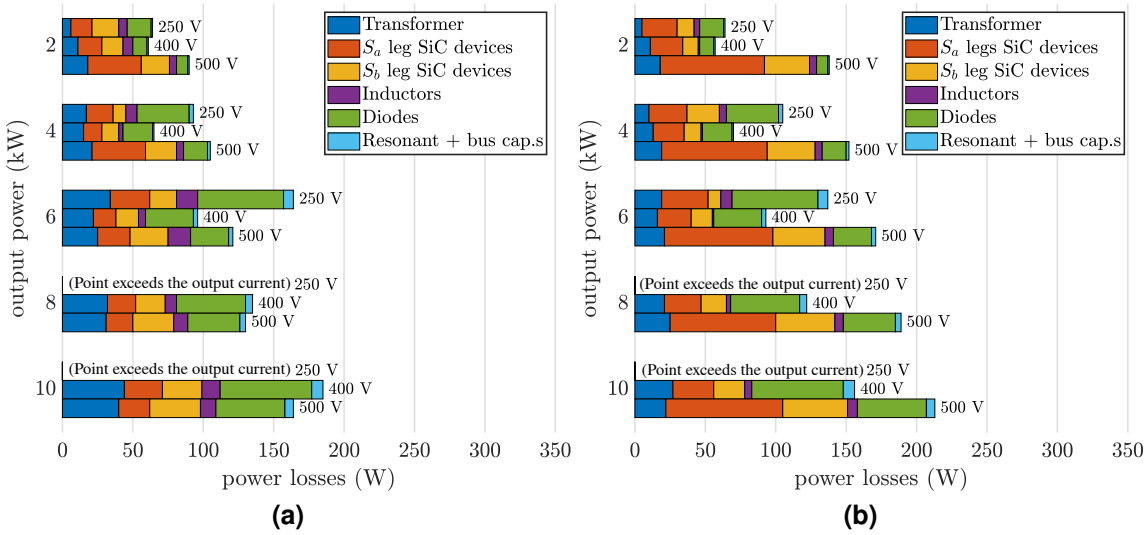


Figure 4.14: Loss breakdown at different output power and minimum, nominal, and maximum output voltages. BB-LLC topologies with efficiency profiles in Fig. 4.13. (a) SiC-based BB-LLC, (b) interleaved SiC-based BB-LLC. Topologies in Sect. 4.2.2 and design specifications in Table 4.3.

Table 4.8: Component count of evaluated PPP topologies.

Topology variant	Quantity			
	Switch	Diode	Transf.	Induct.
SiC-based CLLC + PPP	12	4	1	1
SiC-based CLLC + interleaved PPP	14	4	1	2

hibits significantly improved efficiencies compared to the LLC and voltage controllability in the whole range. Conversely, the second topology variant, i.e., the interleaved BB-LLC, exhibits improved performance at nominal and minimum voltage compared to the standard BB-LLC. However, it suffers from high additional switching losses in the pre-regulation stage at maximum output voltage, leading to a drastic reduction in efficiency. In conclusion, the simple BB-LLC is selected for comparison with the other topologies in Sect. 4.5.

4.4.3 CLLC & Partial-Power Post-Regulator

Efficiency performance results of the SiC-based CLLC and, SiC-based CLLC + PPP and interleaved PPP are presented in Fig. 4.15. The breakdown of the losses is illustrated in Fig. 4.16. The schematics of the topologies are introduced in Sect. 4.2.3, along with the design parameters discussed in Sect. 4.3.3. The component count for all three implemented

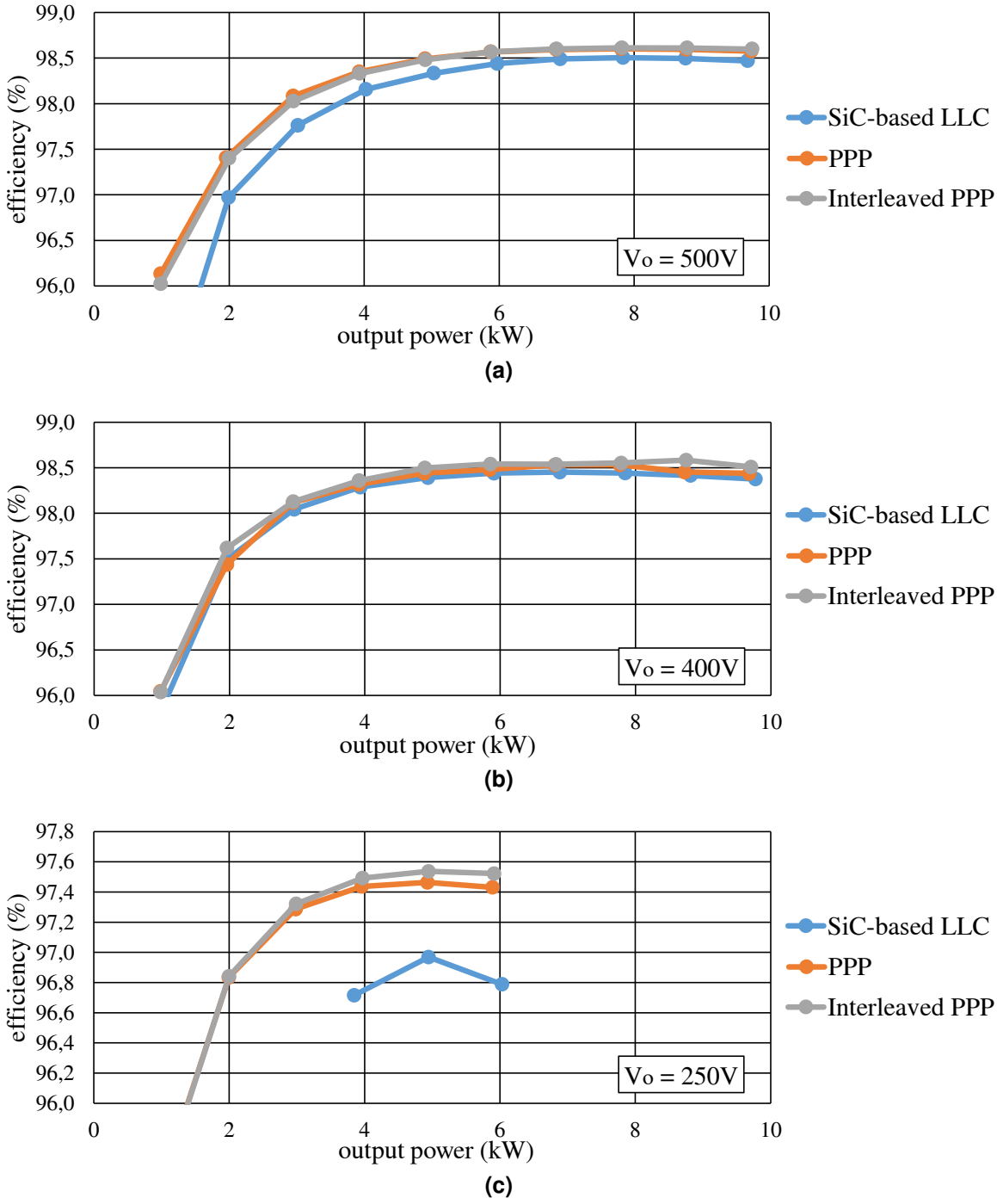


Figure 4.15: Efficiency comparison between SiC-based CLLC and, GaN-based and interleaved GaN-based PPP. (a) $V_o = 500\,\mathrm{V}$; (b) $V_o = 400\,\mathrm{V}$; and (c) $V_o = 250\,\mathrm{V}$. Topologies in Sect. 4.2.3 and design specifications in Table 4.4.

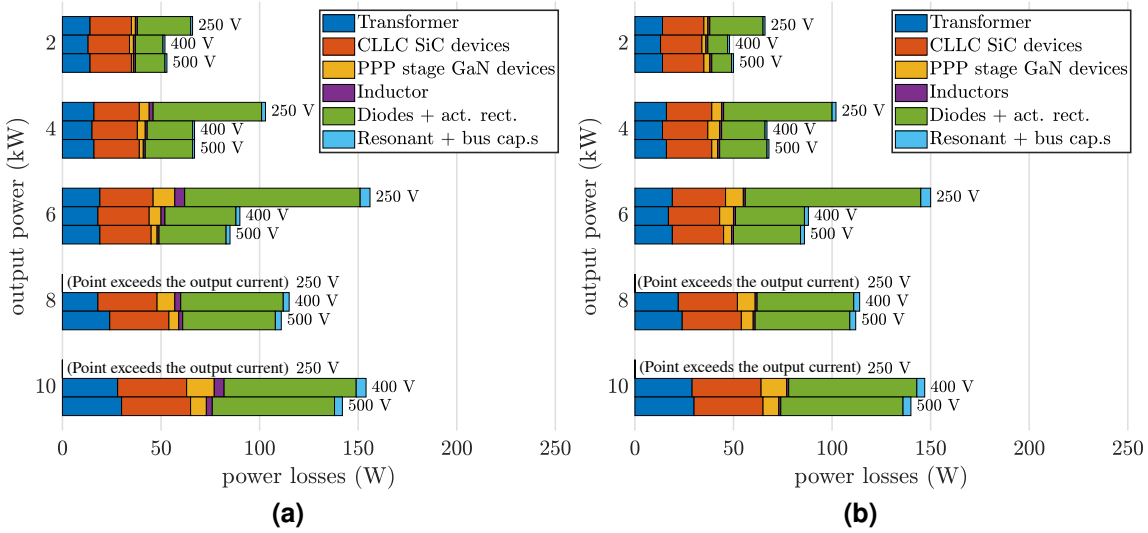


Figure 4.16: Loss breakdown at different output power and minimum, nominal, and maximum output voltages. PPP topologies with efficiency profiles in Fig. 4.15. SiC-based CLLC + (a) GaN-based PPP; and (b) interleaved GaN-based PPP. Topologies in Sect. 4.2.3 and design specifications in Table 4.4.

topologies is provided in Table 4.8, indicating the number of diodes, MOSFETs, transformers, and inductors utilized in each variant.

Notably, the implementation of the PPP stage combined with WBG materials demonstrates significantly improved performance compared to SiC-based LLC. This is evident from the efficiency profiles in Fig. 4.15. Specifically, the interleaved variant of the buck PPP topology demonstrates superior performance, exhibiting notable advantages across a wide output voltage range when compared to the LLC. However, it's important to note that this enhanced performance comes at the cost of a significantly higher number of components, as reported in Table 4.8. In conclusion, this latest variant of PPP is selected for comparison with the other topologies in Sect. 4.5.

4.4.4 LLC & Twin-Bus Buck Post-Regulator

Efficiency performance results of the SiC-based LLC and, SiC-based LLC + TBB, SiC-based interleaved TBB and GaN-based interleaved TBB are presented in Fig. 4.17. The breakdown of the losses is illustrated in Fig. 4.18. The schematics of the topologies are introduced in Sect. 4.2.4, along with the design parameters discussed in Sect. 4.3.4. The

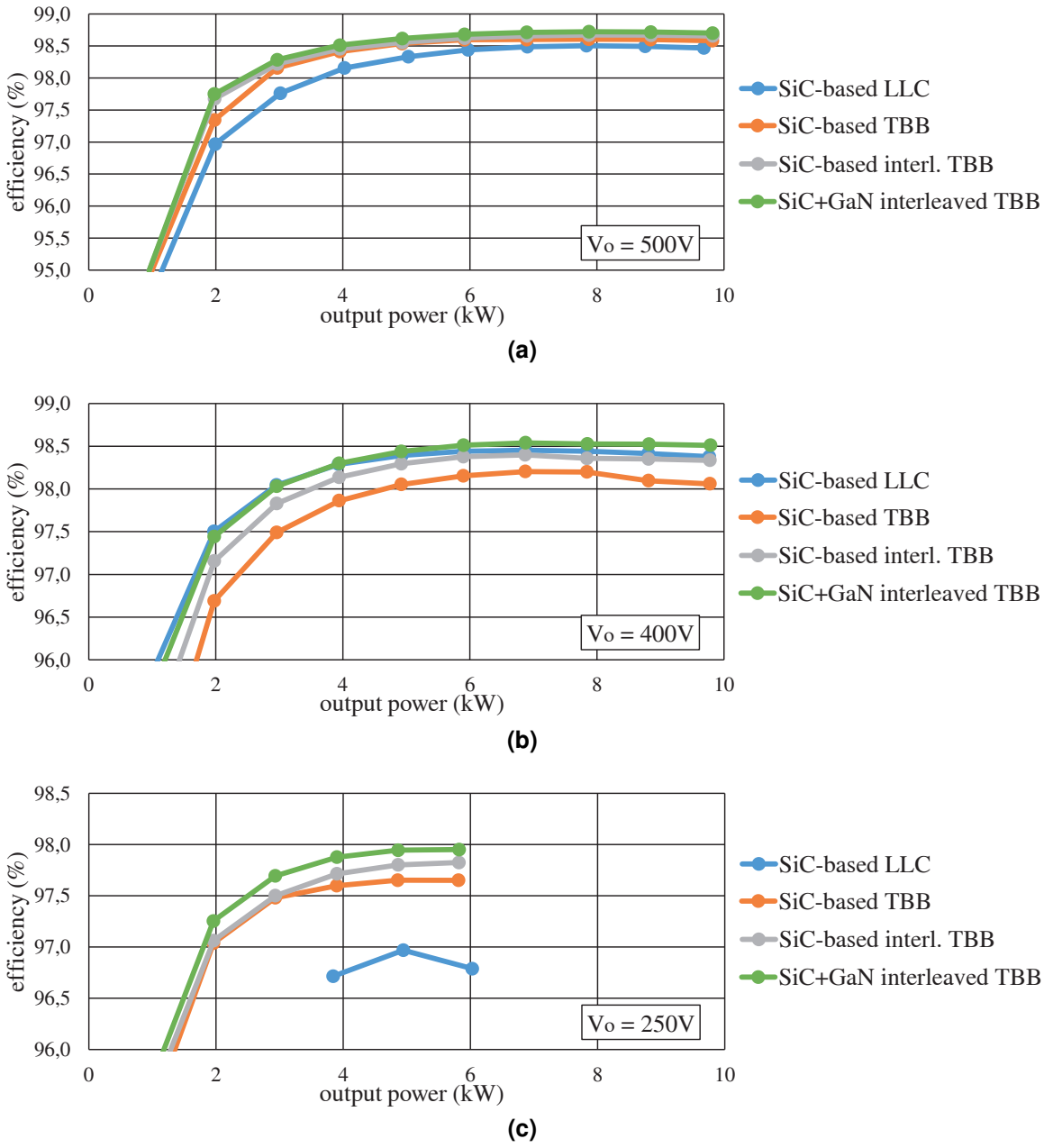


Figure 4.17: Efficiency comparison between SiC-based LLC, SiC-based TBB and GaN-based interleaved TBB. (a) $V_o = 500\,\text{V}$; (b) $V_o = 400\,\text{V}$; and (c) $V_o = 250\,\text{V}$. Topologies in Sect. 4.2.4 and design specifications in Table 4.5.

Table 4.9: Component count of evaluated TBB topologies.

Topology variant	**Quantity**			
	Switch	Diode	Transf.	Induct.
SiC-based LLC + TBB	6	8	1	1
SiC-based LLC + interleaved TBB	8	8	1	2
SiC-based LLC + GaN-based interl. TBB	8	8	1	2

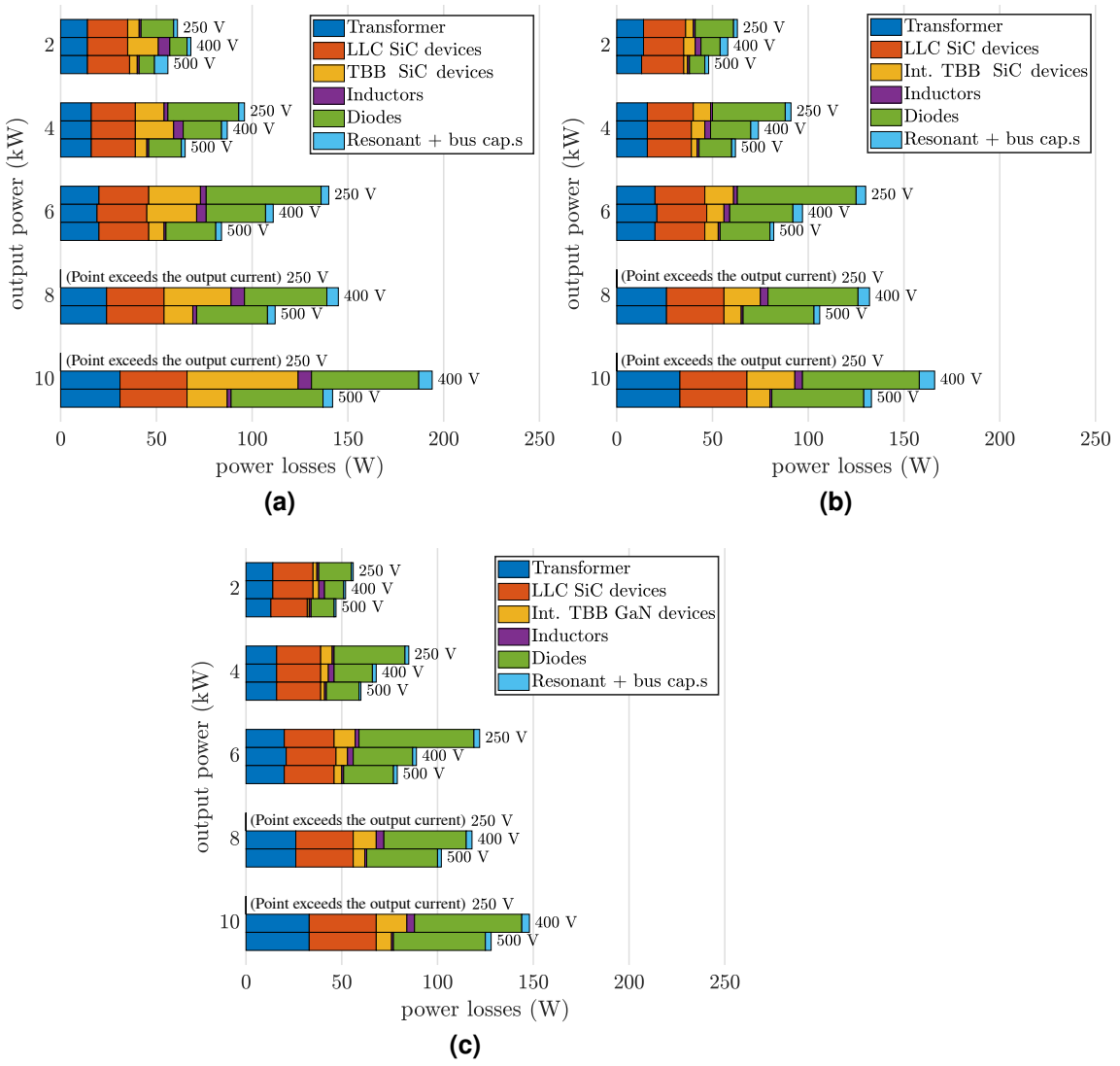


Figure 4.18: Loss breakdown at different output power and minimum, nominal, and maximum output voltages. TBB topologies with efficiency profiles in Fig. 4.17. SiC-based LLC + (a) TBB; (b) interleaved TBB; and (c) GaN-based interleaved TBB. Topologies in Sect. 4.2.4 and design specifications in Table 4.5.

Table 4.10: Component count of the selected topologies for the evaluation.

Topology variant	Quantity			
	Switch	Diode	Transf.	Induct.
SiC-based LLC	4	4	1	2
SiC-based LLC with GaN-based active rect.	8	0	1	2
SiC-based BB-LLC	4	4	1	2
SiC-based CLLC + GaN-based interl. PPP	14	4	1	2
SiC-based LLC + GaN-based interl. TBB	8	8	1	2

component count for all three implemented topologies is provided in Table 4.9, indicating the number of diodes, MOSFETs, transformers, and inductors utilized in each variant.

Notably, the implementation of interleaved TBB stage combined with WBG materials demonstrates significantly improved performance compared to SiC-based LLC. This is evident from Fig. 4.17. In particular, the variant with interleaved GaN-based TBB showcases the highest performance, with pronounced advantages in the wide output voltage range compared to the LLC. Importantly, the elevated diode losses depicted in Fig. 4.18 can be significantly diminished by incorporating active rectification. However, it should be noted that this approach would substantially increase the component count. In conclusion, this latest variant of TBB is selected for comparison with the other topologies in Sect. 4.5.

It is worth noting that a variant of the proposed topology, where the two outputs of the DCX-LLC are connected in series, was also explored. However, the analysis revealed both advantages and disadvantages. While there appeared to be potential benefits in terms of transformer design, this solution is outweighed by the drawback of additional losses incurred due to the output current flowing through both diode rectifier bridges.

4.5 Topology Performance Comparison and Final Considerations

Finally, Fig. 4.19 provides a comprehensive comparison of the efficiencies exhibited by the top-performing topologies that are extensively examined in the preceding sections. When compared to the LLC and its active rectification variant, all the reported topologies gen-

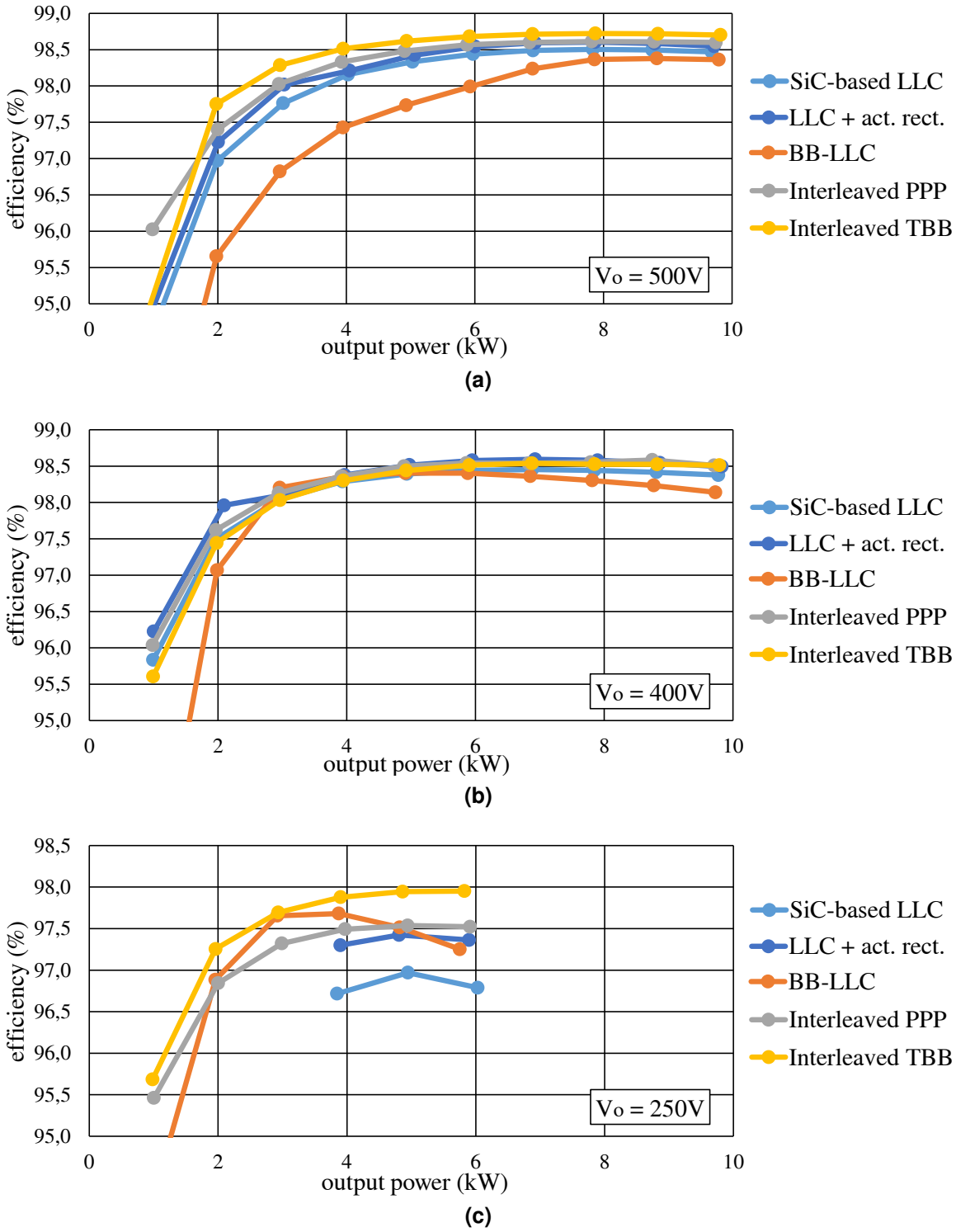


Figure 4.19: Efficiency comparison between SiC-based LLC, SiC-based BB-LLC, SiC-based CLLC + interleaved PPP and SiC-based LLC + GaN-based interleaved TBB. (a) $V_o = 500\,\mathrm{V}$; (b) $V_o = 400\,\mathrm{V}$; and (c) $V_o = 250\,\mathrm{V}$. The interleaved TBB showed the highest performances overall, but at the cost of a higher number of components.

erally exhibit superior efficiency performance. However, this improvement comes at the cost of increased component count, as detailed in Table 4.10. In general, the major loss contribution comes from the rectification stages; if active rectification is implemented, the performances of all the considered topologies will improve consequently, at the cost of higher circuit complexity. Notable efficiency enhancements are observed in the interleaved TBB topology, warranting further investigations in Ch. 6 and Ch. 7. The PPP topology showcases excellent efficiency performance, akin to the TBB, but employs a substantial number of switching devices, over three times the count of those used in the LLC. Consequently, it has not been subjected to experimental investigation. The BB-LLC demonstrates commendable efficiency performance, employing the same number of components as the LLC (refer to Table 4.10). As a result, it is examined in Ch. 5.

In conclusion, the comprehensive simulation-based comparison of various multi-stage converter topologies for EV fast charging systems provides valuable insights into their efficiency and performance trade-offs. While the investigated topologies exhibit improved efficiency over the traditional LLC, considerations such as component count and practical implementation challenges play a crucial role in determining the optimal choice.

4.6 Summary

This chapter presents a simulation-based comparison of the two-stage dc-dc converter topologies introduced in Ch. 2. Three two-stage topologies are introduced in Ch. 2 as the focal points of this investigation. Modifications to circuit designs and the utilization of WBG semiconductors are explored to enhance performance. Simulation models developed in Ch. 3 are employed in PLECS®/Simulink® and MATLAB® environment. Design parameters are obtained by the guidelines established in Ch. 3, targeting a $400\,\mathrm{V}$ EV battery pack with a 800-V input, output voltage ranging from $250\,\mathrm{V}$ to $500\,\mathrm{V}$, and power rating of $10\,\mathrm{kW}$. These scaled prototypes can be used for actual parallel module operation, aiming for a comprehensive efficiency assessment and the identification of the optimal converter topology for EV charging applications. Promising solutions, particularly the BB-LLC and the TBB converter, exhibit favorable efficiency performance and a reasonable component

count. These solutions are further investigated through experimental validation in Ch. 5 and Ch. 6.

Chapter 5

Buck-Boost LLC

Chapter in Brief

In this chapter, a detailed analysis and experimental validation of the proposed buck-boost LLC, introduced in Sect. 2.3.1 and evaluated through simulations in Sect. 4.4.2, is presented. The buck-boost LLC (BB-LLC) is a two-stage isolated dc-dc converter that employs a first pre-regulation stage and a second half-bridge LLC stage, integrated with the first. The second stage is always operated at resonance, ensuring high efficiency. The first pre-regulation stage is responsible for the desired input-to-output voltage conversion ratio and the ZVS operation of all the switches. This allows low conversion losses even with voltages that may vary over a wide range. This chapter provides an in-depth exploration of the converter's structural aspects, followed by a comprehensive analysis of its operational characteristics. The design considerations for the magnetic components are discussed, and the converter's performance is demonstrated through experimental validation. Input and output voltages are compliant with those introduced in Sect. 1.3 for EV applications. The experimental prototype interfaces a $750\,\mathrm{V}$ dc-link with an output bus with nominal voltage range $250\,\mathrm{V}$ - $500\,\mathrm{V}$. The implemented module, rated at $5\,\mathrm{kW}$, achieves a peak efficiency of 98.0% at an output power of $3\,\mathrm{kW}$. By combining theoretical analysis with practical validation, this chapter aims to offer a comprehensive understanding of the BB-LLC converter's performance and potential benefits, contributing to the advancement of efficient and reliable EV charging solutions.

5.1 Introduction

Input voltage regulation proves to be a practical solution when wide input and output voltage regulation is necessary. This approach offers simplicity, a reduced component count, and the ability to adapt to resonant stages with optimal efficiency [38, 60, 71, 72]. This is

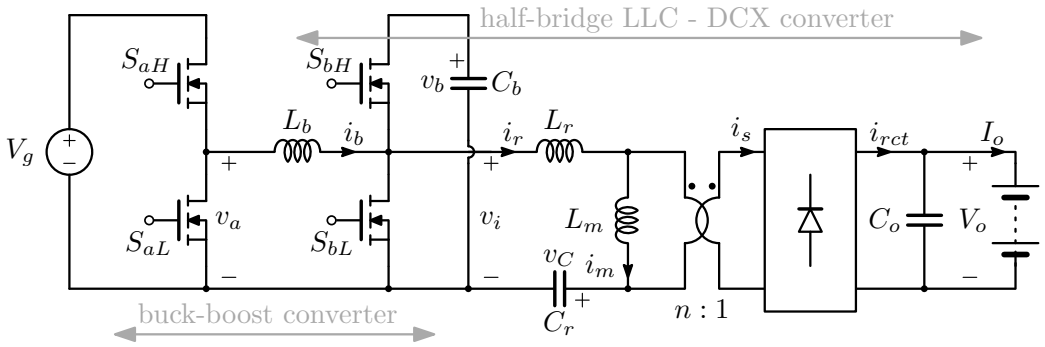


Figure 5.1: Two-stage converter with buck-boost pre-regulation & DCX-LLC stage.

precisely the case with the topology described in this chapter.

The structure is re-proposed in Fig. 5.1 for ease of documentation. It is constituted of a pre-regulation stage and a half-bridge DCX-LLC, employing the LLC converter at its maximum efficiency condition and avoiding the efficiency degradation due to the classical frequency modulation. The topology was studied in [74] considering telecom applications with input voltage range $250\,\mathrm{V}$ - $420\,\mathrm{V}$, output voltage $24\,\mathrm{V}$ and power ratings $750\,\mathrm{W}$. In [75], the potentiality of adopting a phase-shift modulation is not considered to improve the ZVS performances of the topology and the pre-regulator is operated in hard switching at lower switching frequency. Moreover a bulkier capacitor is needed to stabilize the intermediate bus voltage. Accordingly to the application specifications in Sect. 1.3, herein the topology is studied and demonstrated considering a nominal input voltage of $750\,\mathrm{V}$, output voltage $250\,\mathrm{V}$ - $500\,\mathrm{V}$, implementing a prototype module rated $5\,\mathrm{kW}$. Based on the analysis, a modulation scheme is also derived to operate the converter at high efficiency.

The principle of the considered conversion structure is to operate the second stage at conditions that ensure maximum efficiency, namely, at resonance, and exploit the pre-regulation stage to impose such an optimal operating condition for the second, LLC stage. The pre-regulation stage can also help in achieving zero-voltage turn-on of the switches that drive the second stage over a wide range of output voltages [11,38]. The exploitation of latest WBG power semiconductors allows to further reduce semiconductor loss [79]. In spite of the presence of an additional stage, some valuable characteristics are highlighted and shown in terms of overall conversion efficiency. In particular, light-load low-voltage operation is possible with limited efficiency degradation, which is instead difficult to achieve

with the LLC topology.

Part of the content of this chapter has been published in [26, 73, 81].

5.2 Operating Principle

The two-stage topology is displayed in Fig. 5.1. Its peculiarity is the integration of the two power switches S_{bH} and S_{bL} of the buck-boost stage as primary switches of the half-bridge LLC [74, 75]. Thanks to such a peculiarity, the inductor current i_b and the resonant current i_r in Fig. 5.1 may jointly contribute in reducing the conduction loss of S_{bH} and S_{bL} and, notably, achieve ZVS. In this way, ZVS can be achieved even with lower values of magnetizing current, which also helps in reducing overall losses.

In order to exploit the high performance of the LLC stage working as dc-transformer [55], the right-leg (i.e., S_{bH} and S_{bL}) duty-cycle is fixed at 50%. Whereas, the two remaining degrees of freedom, that is, the duty-cycle d of the left-leg referred to the upper switch S_{aH} and the phase-shift φ between the driving signals of the two legs, can be used to adjust *i*) the inductor current at switching instants, which is important for ZVS constraints, and *ii*) the output voltage, which is important to allow operation at resonance of the LLC stage.

5.2.1 Operation

First, the total voltage gain of the structure can be computed as the product of the voltage gain M_{BB} of the pre-regulation buck-boost and the half-bridge LLC working as DCX. From the volt-second balance on L_b, it yields:

$$d \cdot V_g - \frac{V_b}{2} = 0 \quad \Rightarrow \quad M_{\mathrm{BB}} = \frac{V_b}{V_g} = 2d \tag{5.1}$$

Considering the half-bridge LLC working as DCX:

$$M_{\mathrm{LLC}} = \frac{V_o}{V_b} = \frac{1}{2n} \tag{5.2}$$

Combining (5.1) and (5.2), the whole converter voltage gain is:

$$M = \frac{V_o}{V_g} = M_{\mathrm{BB}} \cdot M_{\mathrm{LLC}} = \frac{d}{n} \tag{5.3}$$

Remarkably, the voltage gain is a function of the duty-cycle d of the left-leg only. Whereas, the phase-shift φ represents a degree of freedom that can be used to shape the piece-wise linear current i_b to ensure ZVS of the four switches. The phase-shift φ is herein defined as the time distance between the centers of the positive pulses of v_a and v_i, normalized by T_s, as shown in Fig. 5.2.

Two main operation modes may be distinguished, namely, boost mode, when $d > 0.5$, and buck mode, when $d < 0.5$. For each operation mode, phase-shift variations give rise to four different shapes of the inductor current i_b, herein refereed to as switching modes (switching mode (SM)). The total eight SMs, depending on the values of d and φ, are displayed in Fig. 5.2a and Fig. 5.2b. Table 5.1a and Table 5.1b report an analytical description of the SMs, which is useful for the analysis of the converter operation. Remarkably, Fig. 5.2 and Table 5.1 mark the switching events at the time instants t_0, t_1, t_2, and t_3; this nomenclature is used in the following to compute the corresponding values of inductor current i_b at those mentioned instants, that is, I_0, I_1, I_2, and I_3, respectively.

5.2.2 Inductor Current Derivation

The equivalent circuit in Fig. 5.3 can be referred to for the derivation of the current i_b through the inductor L_b. Source voltages v_i and v_a model the voltages imposed by the half-bridges in Fig. 5.1, according to Table 5.1.

The instantaneous inductor current i_b in the time domain can be computed as:

$$i_b(t) = I_0 + \frac{1}{L_b} \int_{t_0}^{t} \left(v_a(\tau) - v_i(\tau)\right) \, \mathrm{d}\tau \tag{5.4}$$

where $I_0 = i_b(t_0)$, $t_0 < t$, is the initial value of the inductor current. Being the inductor

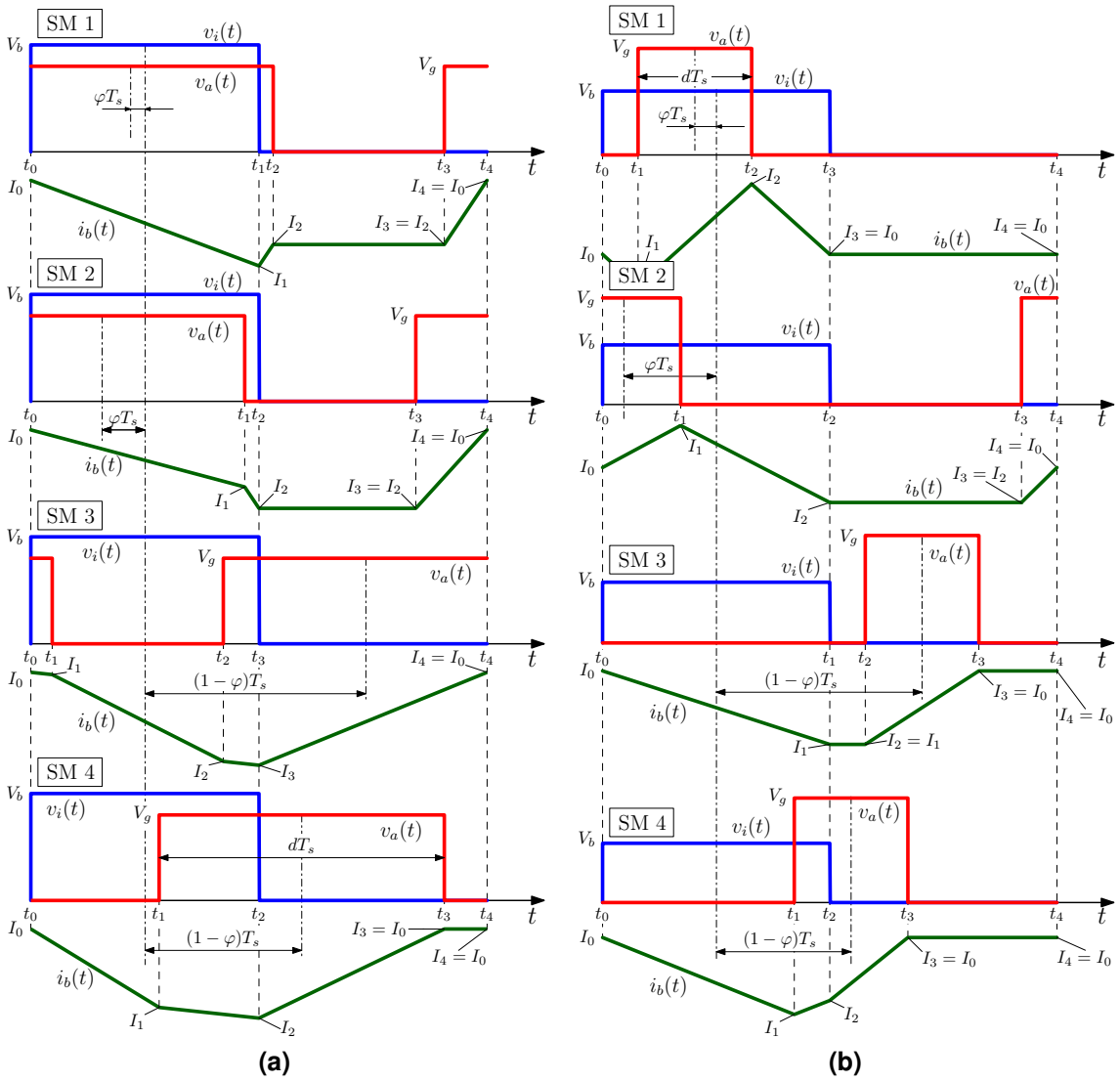


Figure 5.2: Main waveforms of BB-LLC for different phase-shift values considering (a) boost case and (b) buck case. Switching events are marked at time instants t_k ($k = 0, \ldots, 4$), with $t_0 = 0$ and $t_4 = T_s$. The corresponding switching modes are defined analytically in Table 5.1.

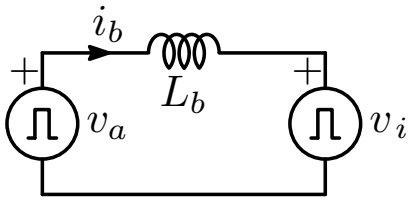


Figure 5.3: Equivalent circuit for inductor current analysis.

Table 5.1: Switching modes based on Fig. 5.2 & associated switching instants.

(a) Boost operation mode (i.e., $d \geq 0.5$)

SM	φ **values**	**switching instants**		
		$\boldsymbol{4 \cdot t_1/T_s}$	$\boldsymbol{4 \cdot t_2/T_s}$	$\boldsymbol{4 \cdot t_3/T_s}$
1	$\frac{1-2d}{4} \leq \varphi < \frac{2d-1}{4}$	2	$1-4\varphi+2d$	$5-4\varphi-2d$
2	$\frac{2d-1}{4} \leq \varphi < \frac{3-2d}{4}$	$1-4\varphi+2d$	2	$5-4\varphi-2d$
3	$\frac{3-2d}{4} \leq \varphi < \frac{1+2d}{4}$	$1-4\varphi+2d$	$5-4\varphi-2d$	2
4	$\frac{1+2d}{4} \leq \varphi < \frac{5-2d}{4}$	$5-4\varphi-2d$	2	$5-4\varphi+2d$

(b) Buck operation mode (i.e., $d < 0.5$)

SM	φ **values**	**switching instants**		
		$\boldsymbol{4 \cdot t_1/T_s}$	$\boldsymbol{4 \cdot t_2/T_s}$	$\boldsymbol{4 \cdot t_3/T_s}$
1	$\frac{2d-1}{4} \leq \varphi < \frac{1-2d}{4}$	$1-4\varphi-2d$	$1-4\varphi+2d$	2
2	$\frac{1-2d}{4} \leq \varphi < \frac{1+2d}{4}$	$1-4\varphi+2d$	2	$5-4\varphi-2d$
3	$\frac{1+2d}{4} \leq \varphi < \frac{3-2d}{4}$	2	$5-4\varphi-2d$	$5-4\varphi+2d$
4	$\frac{3-2d}{4} \leq \varphi < \frac{3+2d}{4}$	$5-4\varphi-2d$	2	$5-4\varphi+2d$

current waveform piecewise linear, (5.4) can be computed as:

$$i_{b_k}(t) = i_b(t_{k-1}) + \frac{v_{L_b}(t)}{L_b} \cdot (t - t_{k-1}) \ , \quad t \in [t_{k-1},\, t_k) \tag{5.5}$$

for $k = 1, 2, 3, 4$. It is called I_k the inductor current values $i_b(t_k)$ and V_{L_k} the voltage across the inductor during $[t_{k-1},\, t_k)$. The initial value $I_0 = i_b(t_0)$ is calculated imposing the capacitor charge balance during the conduction phase of S_{bH}, between $t = 0$ and $t = T_s/2$, thus:

$$I_0 = \frac{2n}{T_s} \int_0^{T_s/2} i_b(t)\, \mathrm{d}t = \frac{n}{2T_s} \sum_{k=1}^{N} \Delta t_k (I_{k-1} + I_k) \tag{5.6}$$

where $\Delta t_k = t_k - t_{k-1}$ and $N = 1, 2$, or 3 is the number of piecewise representations in the considered half-period, depending on the SM. Observing that $I_k = I_{k-1} + V_{L_k} \Delta t_k / L_b$ and $\sum_{k=1}^{N} \Delta t_k = T_s/2$, (5.6) yields:

$$I_0 = n\frac{I_0}{2} + \frac{n}{2L_b T_s} \sum_{k=1}^{N} V_{L_k} \Delta t_k (\Delta t_k + 2\Delta t_{k+1} + 2\Delta t_{k+2}) \tag{5.7}$$

with $\Delta t_k = 0$ for $k > N$. Equation (5.7) allows to determine the initial value I_0, once the output current is known.

An additional parameter worth computing is the inductor rms current:

$$i_b^{\mathrm{rms}} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_b^2(t)\, \mathrm{d}t} = \sqrt{\frac{1}{T_s} \sum_{k=1}^{4} \int_{t_{k-1}}^{t_k} i_{b_k}^2(t)\, \mathrm{d}t} \tag{5.8}$$

where $i_{b_k}(t) = I_{k-1} + \dfrac{V_{L_k}}{L_b} t$, $t \in [t_{k-1},\, t_k)$, it yields:

$$i_b^{\mathrm{rms}} = \sqrt{\frac{1}{T_s} \sum_{k=1}^{4} \left[I_{k-1}^2 \Delta t_k + \frac{I_{k-1} V_{L_k}}{L_b} \Delta t_k^2 + \left(\frac{V_{L_k}}{L_b} \right)^2 \frac{\Delta t_k^3}{3} \right]} \tag{5.9}$$

The equations reported above can help to properly define the modulation parameter φ, as shown in the following sections.

5.3 Main Loss Contribution

Since all the diodes of the DCX-LLC can achieve ZCS turn-off and, with a proper modulation of the phase-shift φ, ZVS turn-on can be achieved for all the active switches, the main loss components include conduction losses of MOSFETs and diodes, magnetic components losses, and MOSFETs turn-off losses. Phase-shift modulation has a significant impact on both MOSFETs switching and conduction losses and inductor losses. The ac resistance and the core losses of the inductor should be accurately took into account in the design of the component to allow a convenient exploitation of the phase-shift modulation. Instead, the transformer losses of the LLC are not affected by φ variations. Besides, optimal design for maximum efficiency of the LLC transformer is facilitated by the fixed operation at nominal conditions allowed by the pre-regulation stage.

The following paragraphs discuss the ZVS conditions for switching losses minimization, the conduction losses evaluation of the inductor and the transformer, and the design procedure of the magnetic components.

5.3.1 Conditions for Zero-Voltage Switching Operation

Switching losses mainly depend on the switches output capacitance C_{oss}, the inductor current at switching instants t_k, which are marked as I_k in Fig. 5.2, and the chosen dead-times. To minimize such a loss contribution, ZVS at turn-on is necessary [95]. This poses minimum switched current constraints for ZVS, which can be determined as discussed in [95–97].

Fig. 5.4 shows a couple of equivalent circuits helping in the analysis of the SMs in Fig. 5.2. Generators v_i, in Fig. 5.4a, and v_a, in Fig. 5.4b, are set as per the considered SM, resulting in different minimum current conditions, function of the input and output voltages. By the methods in [96, 97], the minimum current condition for the ZVS of the left-leg (refer to Fig. 5.4a) can be calculated by solving iteratively the following expression for $t_{\mathrm{ZVS}} \leq t_{\mathrm{dead}}$:

$$t_{\mathrm{ZVS}} = \int_0^{V_g} \frac{C_{sw}(v_a)}{\sqrt{i_{\mathrm{ZVS}}^2 + \dfrac{2}{L_b}\displaystyle\int_0^{v_a} C_{sw}(v)(v_i - v)\,\mathrm{d}v}}\,\mathrm{d}v_a \tag{5.10}$$

(a) Turn-on S_{aH} and S_{aL} **(b)** Turn-on S_{bH} and S_{bL}

Figure 5.4: Equivalent circuits during ZVS transients.

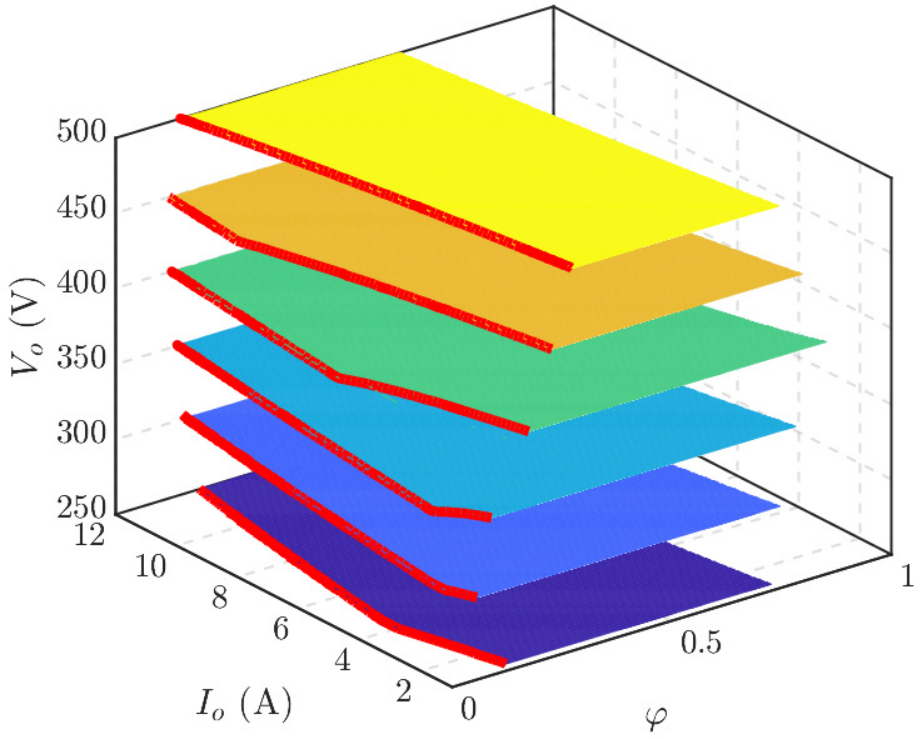


Figure 5.5: ZVS regions for the whole output voltage range. Converter parameters are reported in Table 5.2.

where t_{ZVS} is the duration of the transition with an initial inductor current i_{ZVS}, and C_{sw} is the equivalent charge capacitance at the switching node [97]. Equation (5.10) can be adapted to the equivalent circuit in Fig. 5.4b by substituting V_g with V_b and v_i with v_a, respectively.

By this approach, ZVS regions for all the switches in the output-current, output-voltage (i.e., duty-cycle d), and phase-shift space can be computed, as displayed in Fig. 5.5. Fig. 5.6a and Fig. 5.6c show the ZVS region at minimum and nominal output voltage respectively. Notably, ZVS is achieved over the whole range of transferred power and output voltages. In Fig. 5.5, and then in Fig. 5.6a and Fig. 5.6c, red lines highlight those points where ZVS

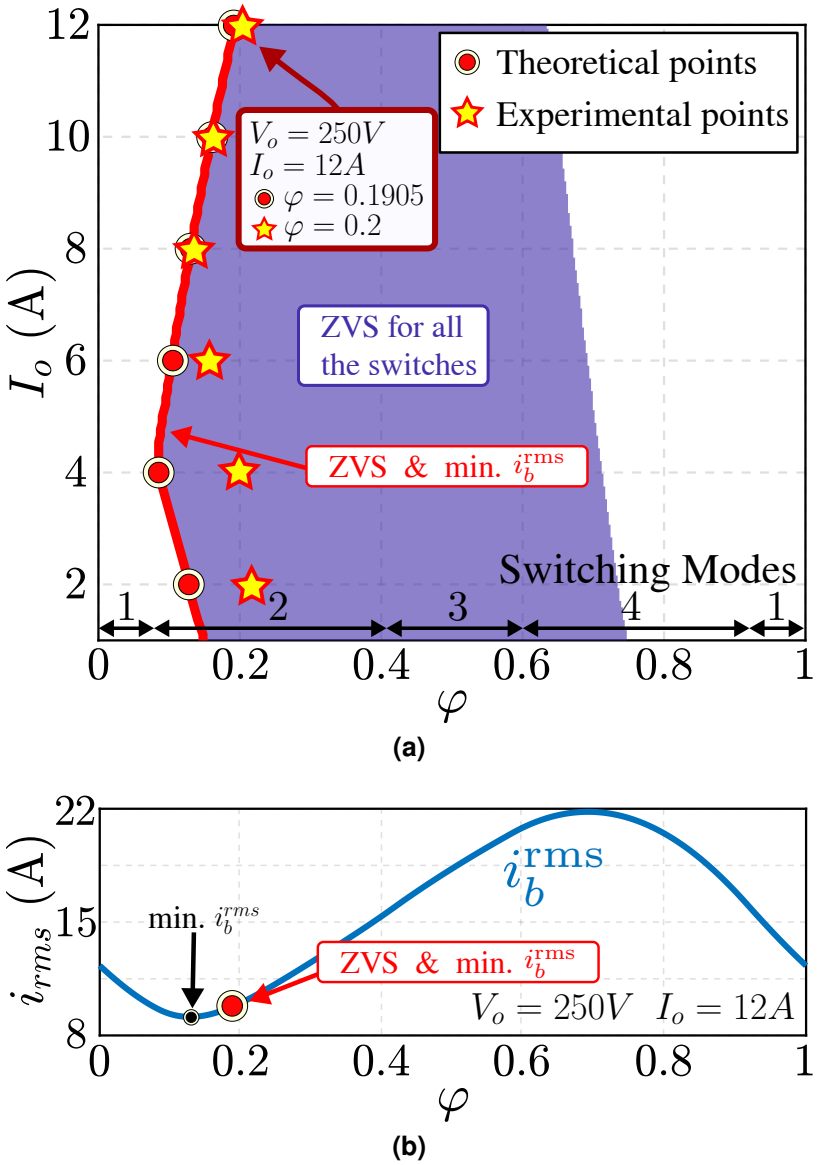
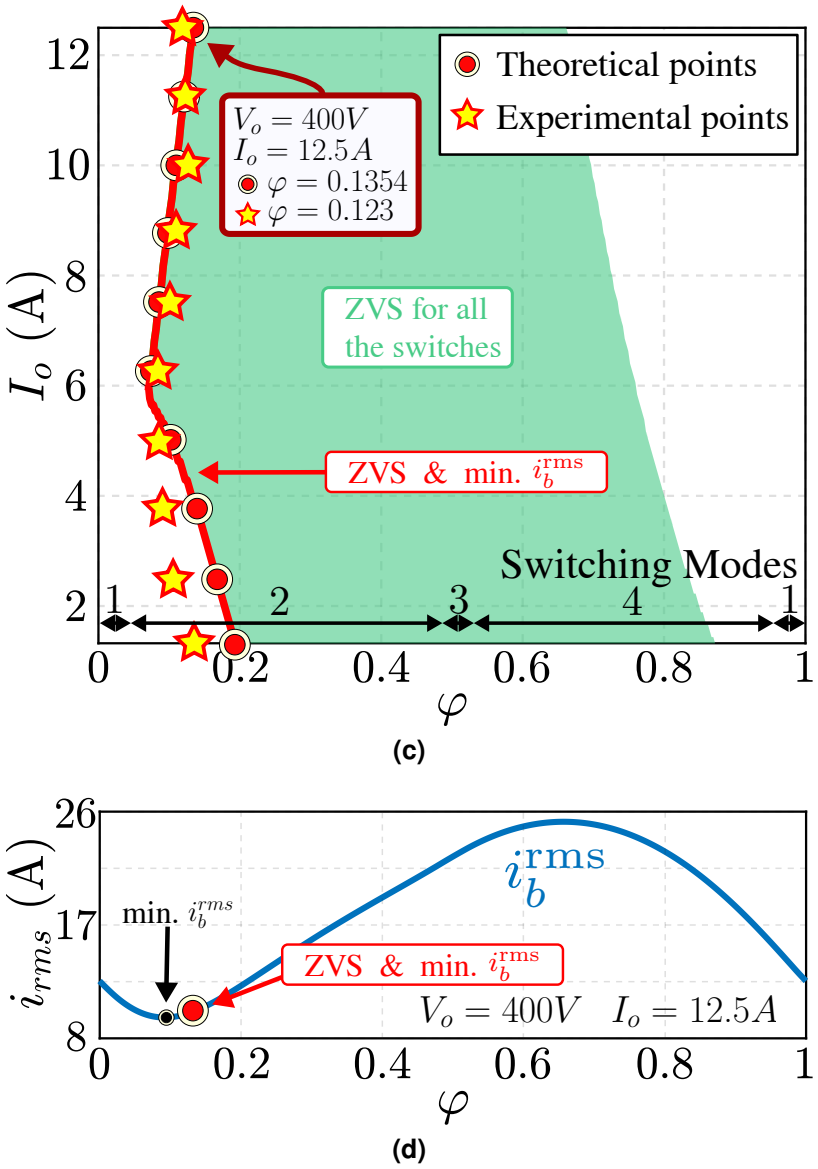


Figure 5.6: Results obtained by exploiting the phase-shift φ to achieve ZVS. At $V_o = 250\,\text{V}$, $I_o = 12\,\text{A}$: (a) ZVS region; and (b) inductor rms current. At $V_o = 400\,\text{V}$ and $I_o = 12.5\,\text{A}$: (c) ZVS region; and (d) inductor rms current. Optimal values of phase-shift φ are those lying along the line labeled as "*ZVS* & min. $i_b^{\rm rms}$", for which ZVS is achieved with minimum circulating rms currents. Switching modes as defined in Fig. 5.2 are also reported on the bottom of (a) and (c).



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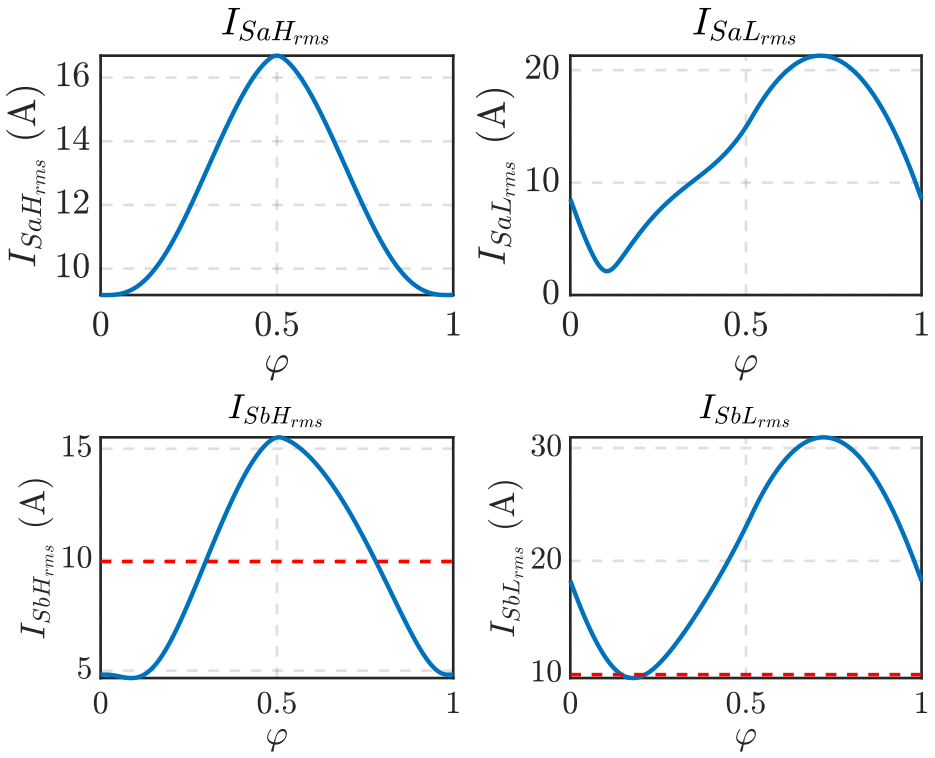


Figure 5.7: Switches rms currents at $V_o = 400\,\mathrm{V}$, $I_o = 12.5\,\mathrm{A}$. The red-dashed line shows the resonant current component i_r on the right-leg MOSFETs.

is achieved for all the switches with minimum inductor rms current, which relates to the minimum phase-shift values to achieve ZVS. Such an inductor current computed as in (5.9) is shown in Fig. 5.6b and Fig. 5.6d for minimum and nominal output voltages, respectively. Fig. 5.7 shows the switches rms currents at $V_o = 400\,\mathrm{V}$ and $I_o = 12.5\,\mathrm{A}$. For low phase-shifts, where ZVS is achieved for all the switches with minimum inductor rms current, the effect of the current compensation of the right-leg switches is appreciable, which is one of the peculiarities of the analyzed topology in Fig. 5.1.

It is worth remarking that absence of ZVS turn-on makes switching losses become a predominant portion of the total converter loss, especially in high-voltage applications [33]. For this reason ZVS turn-on is aimed herein, especially at low output voltages, where state-of-the-art LLC topologies present significant efficiency degradations due the lost of ZVS [11].

5.3.2 Conduction Losses Calculation

Equation 3.15 allows to model the conduction losses of a magnetic element by summing both dc losses, which are associated with the winding's dc resistance (R^{dc}) and the dc value of the current (i^{dc}), and ac losses. The ac losses can be estimated by considering the rms of the first M ac frequency components ($i^{\mathrm{ac_m}}$) and the corresponding ac winding resistances. The ac winding resistances can be calculated using 3.4. Therefore, the conduction losses related to the inductor L_b can be modeled as:

$$P_{L_b}^{\mathrm{cond}} = R_b^{\mathrm{dc}} \cdot i_b^{\mathrm{dc}\,2} + \sum_{m=1}^{M} R_b^{\mathrm{ac_m}} \cdot i_b^{\mathrm{ac_m}\,2} \tag{5.11}$$

Equation (5.11) is adopted for the estimation of the winding losses of the inductor in Sect. 5.5.2. In the considered case, the number of harmonics for an acceptable estimate is set $M = 3$. Instead, the conduction losses of the transformer of the LLC stage are not affected by any modulations. The LLC behaves as a DCX and the winding losses of the transformer can be simplified as:

$$P_{\mathrm{Tr}}^{\mathrm{cond}} \simeq R_{\mathrm{Tr}}^{\mathrm{ac_1}} \cdot i_r^{\mathrm{rms}\,2} \tag{5.12}$$

where $R_{\mathrm{Tr}}^{\mathrm{ac_1}}$ is the ac resistance of the windings referred to the primary side at fundamental frequency and i_r^{rms} is the rms value of the resonant current. In this approximation, the magnetizing current effect on the conduction losses is overestimated, which is acceptable when such a current is relatively small, as in the considered DCX-LLC structure.

5.3.3 Optimal Switching Mode Selection

In Sect. 5.2.1, eight SMs are identified depending on the phase-shift φ and the duty-cycle d, as defined in Fig. 5.2 and Table 5.1. Each SM is characterized by a unique switching sequence, which gives rise to eight different shapes of the inductor current i_b. A proper SM must be selected in order to obtain a shape for the current i_b that is suitable to ensure ZVS for all the switches. This can be performed by verifying condition (5.10) for each of the converter switches. Moreover, if multiple SMs appear suitable for the aimed ZVS

conditions, the SM ensuring minimum circulating currents should be selected. To better explain the procedure, the modulation planes for a couple of representative operating points are reported in Fig. 5.6. It is possible to notice that there is a wide range of phase-shifts, covering multiple SMs, that allow to satisfy ZVS conditions. Notably, the SM that encloses all the operation points while in ZVS with minimum inductor rms currents (i.e., all the operating points highlighted with the red lines in Fig. 5.6a and Fig. 5.6c) is SM 2. This is verified for buck and boost operation modes and for the whole output power range.

5.4 Converter Design Considerations

Some adopted design considerations of the converter in Fig. 5.1 are reported in the following based on the analyses presented in Sect. 5.2. Transformer and inductor design procedures adhere to the guidelines outlined in Sect. 3.3.3.

5.4.1 Transformer Design

From (5.3), the transformer turns ratio n is set to 1 to make the LLC converter operate at the resonant frequency f_s at the output nominal voltage V_o equal to $400\,\mathrm{V}$ and the intermediate-bus voltage V_b equal to $800\,\mathrm{V}$.

The value of the magnetizing inductance L_m is typically chosen to ensure a sufficiently high magnetizing current to allow ZVS and a desired voltage gain [70]. Lower L_m values give lower voltage gains and ease ZVS, but it also implies higher transformer losses. Differently, with the aimed DCX operation of the LLC stage in Fig. 5.1, ZVS can be achieved regardless of the contribution by the magnetizing current. This is illustrated in Fig. 5.8 considering the operating point $V_o = 250\,\mathrm{V}$, $I_o = 10\,\mathrm{A}$. The red dashed-line at the boundary represents the minimum absolute switched current to achieve ZVS, estimated via (5.10). The red dotted-line shows the additional contribution by the magnetizing current at the switching instants. Notably, ZVS conditions can be satisfied by a proper modulation of the phase-shift φ, then, even large magnetization inductances can be selected. For example, a transformer with $L_m = 180\,\mu\mathrm{H}$ is designed and adopted in the prototype shown herein, while a classical design for a DCX-LLC would require a magnetizing inductance not higher

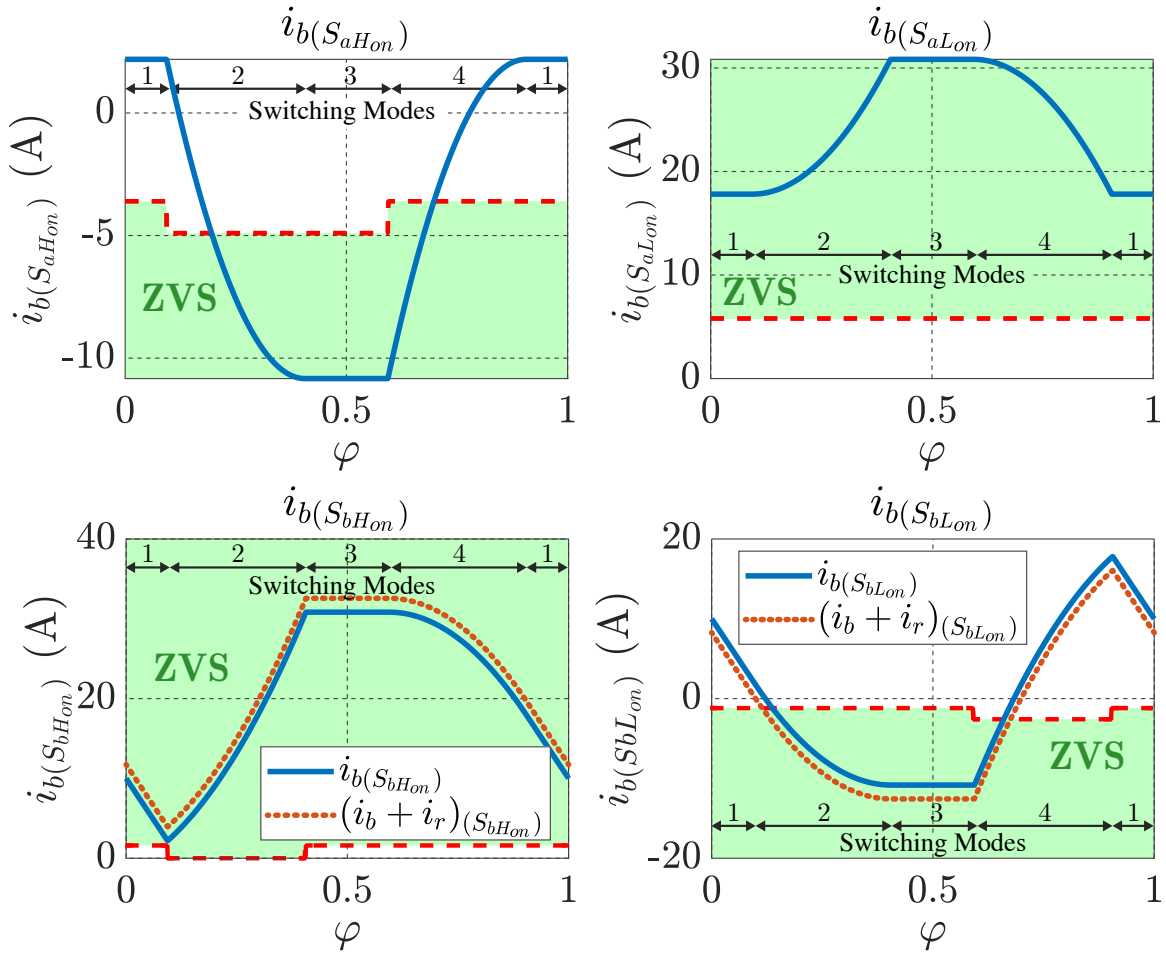


Figure 5.8: Inductor current at switching instants *versus* φ; $V_o = 250\,\text{V}$, $I_o = 10\,\text{A}$. The term $i_b + i_r$ shows the additional contribution by the magnetizing current.

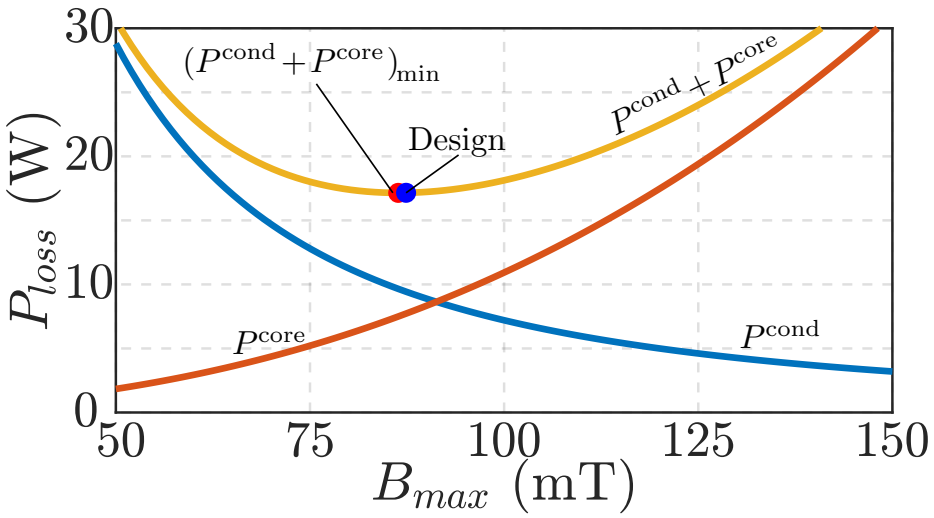


Figure 5.9: P-B plot for transformer design at $V_o^{\text{nom}} = 400\,\text{V}$ and $P_o^{\text{nom}} = 5\,\text{kW}$. The design point is obtained with two parallel litz wires $500 \times 71\,\mu\text{m}$ each and number of turns $N_p = N_s = 17$.

than:

$$\frac{V_b}{4 f_s i_{\text{ZVS}}} \tag{5.13}$$

where i_{ZVS} is the constant current needed for zero-voltage transition at the bus voltage V_b, and f_s is the switching frequency. In the considered prototype, the classical design procedure would result in $L_m \leq 90\,\mu\text{H}$ in order to fulfill ZVS constraints of the LLC leg, with consequently higher rms currents.

For what concerns the design of the resonant $L_r C_r$ tank, the transformer leakage inductance can be exploited for the implementation of the inductive part. Given the DCX-LLC operation mode, low values of L_m can be used, which is beneficial in terms of transformer design, losses, and resonant capacitor voltage stress. Interleaving is also possible for the primary and secondary-side windings to limit the leakage inductance. An estimation of the transformer leakage inductance is given in (3.26). The capacitive part can be selected on the basis of the desired resonant frequency (i.e., converter switching frequency given the DCX-LLC operation).

Transformer design procedure follows the guidelines reported in Sect. 3.3.3. Fig. 5.9 reports the results using (3.23), showing a total loss of 17 W at nominal conditions, namely, $V_o = 400\,\text{V}$ and $P_o = 5\,\text{kW}$. At the point of minimum total loss, $B_{\text{opt}} = 89\,\text{mT}$ and the to-

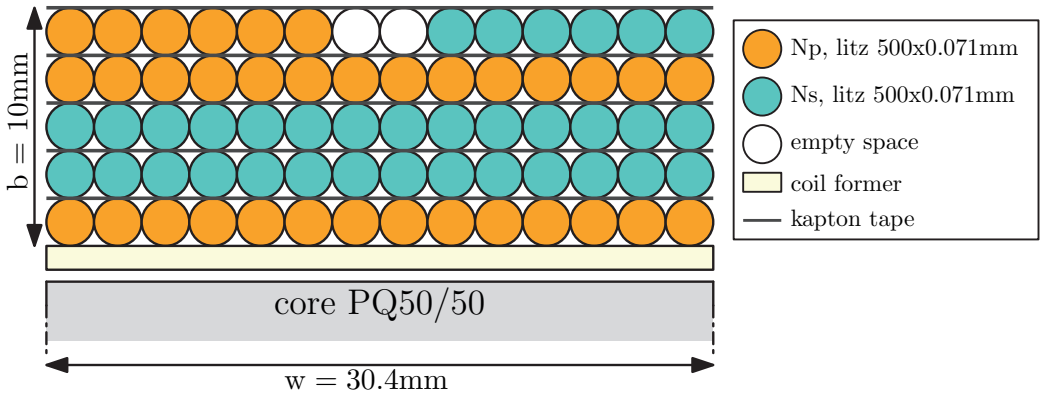


Figure 5.10: Winding layout of the designed transformer. Number of turns $N_p = N_s = 17$. Each turn is composed of two parallel litz wires $500 \times 71\ \mu\text{m}$ each.

tal loss is equally shared among winding and total losses. A prototype of the transformer is implemented using a core PQ50/50 N87 and two parallel litz wires $500 \times 71\ \mu\text{m}$, resulting in a measured total power loss of $21\,\text{W}$ at the same nominal conditions.

Fig. 5.10 depicts the winding layout of the designed transformer. The transformer has an unitary turns ratio n, current density of $J_0 = 4.3\,\text{A}/\text{mm}^2$, and number of windings per turn of $N_p = N_s = 17$, given by (3.25). Remarkably, a corresponding transformer design for a full-bridge LLC with the same $B_{\max}$ and current density J_0 would lead to a required area-product A_p higher by 10% than the obtained design, that is, to higher wire resistance and core loss.

5.4.2 Inductor Design

In order to minimize conduction losses, the inductor value is selected to minimize the rms value of the current i_b, that is, i_b^{rms}, over the entire voltage conversion range. Specifically, the inductance value is selected aiming at ZVS with minimum circulating current. Fig. 5.11 reports the required minimum phase-shift and resulting inductor rms current considering different inductor values, while always ensuring ZVS. Data are reported for different output voltage values and nominal output current. In this comparison, $L_b = 30\,\mu\text{H}$ emerges as the best overall choice in terms of rms current for the output voltage range in the considered application, and shown in Table 5.2. The inductor design procedure is reported in Sect. 3.3.3. It is worth reporting that, a wider output voltage range would require an

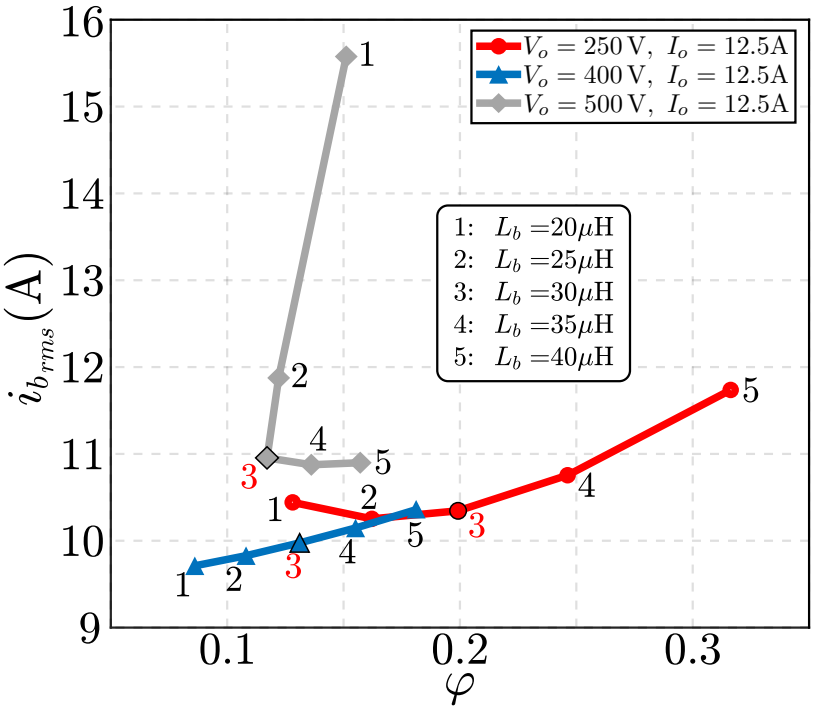


Figure 5.11: Selection of the optimal inductance value, at maximum output current $I_o = 12.5\,\mathrm{A}$. ZVS is always achieved for each point.

inductor with larger core and wire sections in order to satisfy thermal constraints.

5.5 Experimental Results

The experimental prototype displayed in Fig. 5.12 of a $5\,\mathrm{kW}$ module with parameters in Table 5.2 is implemented to validate the reported analysis, modulation, and design choices. The design parameters adhere to those presented in Sect. 1.3, specifically tailored for EV applications.

5.5.1 Switches Zero-Voltage Turn-on

Operation at $\varphi = 0.25$, output voltage of $250\,\mathrm{V}$, and output current of $10\,\mathrm{A}$ is evaluated experimentally and shown in Fig. 5.13. At this operating point, ZVS is verified for all the switches. Notably, according to Fig. 5.6, ZVS can be achieved with phase-shift values between $\varphi = 0.16$ and $\varphi = 0.65$. At the boundary condition for ZVS of $\varphi = 0.16$ the inductor conduction losses are 35% lower than the losses at the operating point in Fig. 5.13,

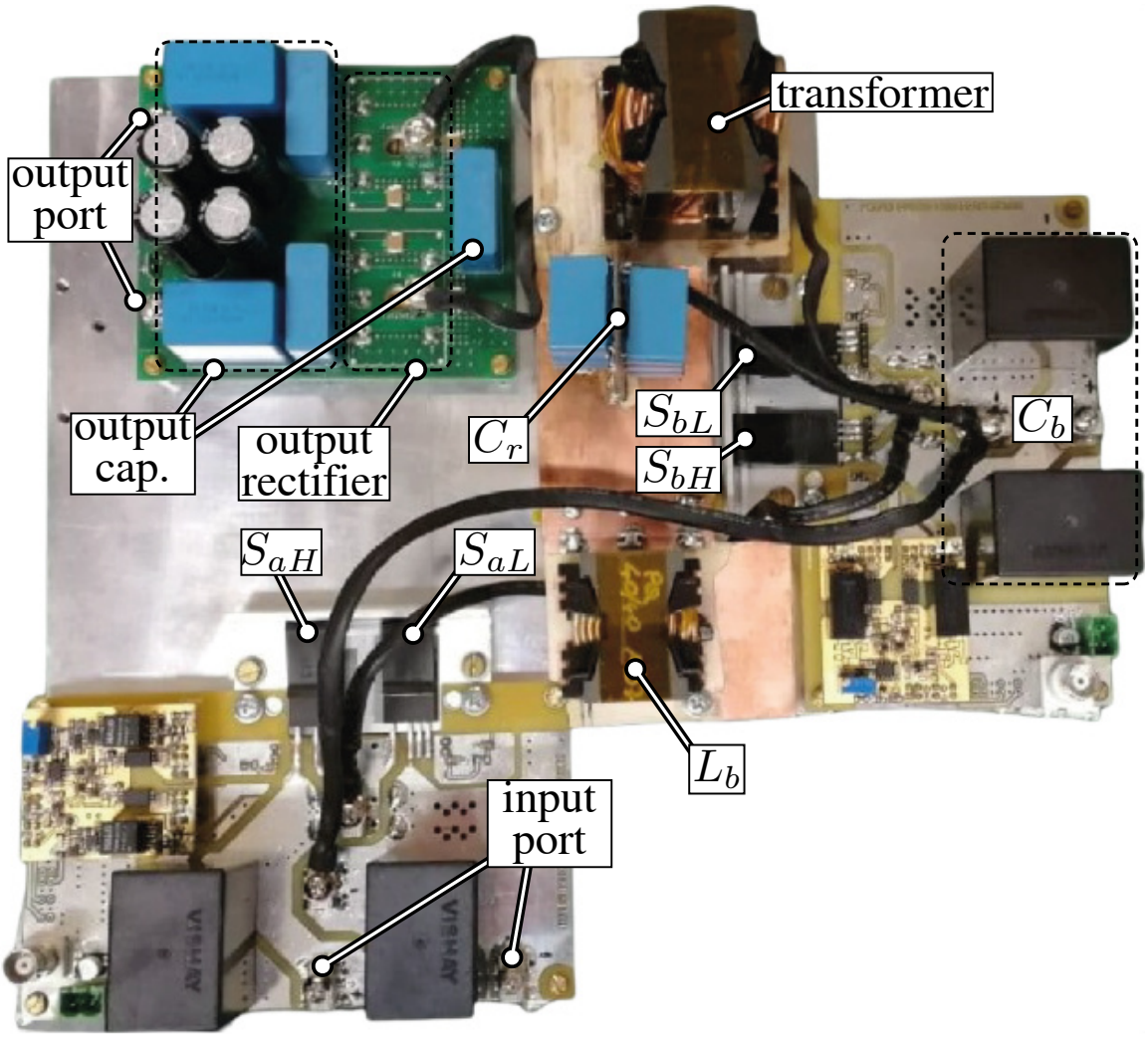
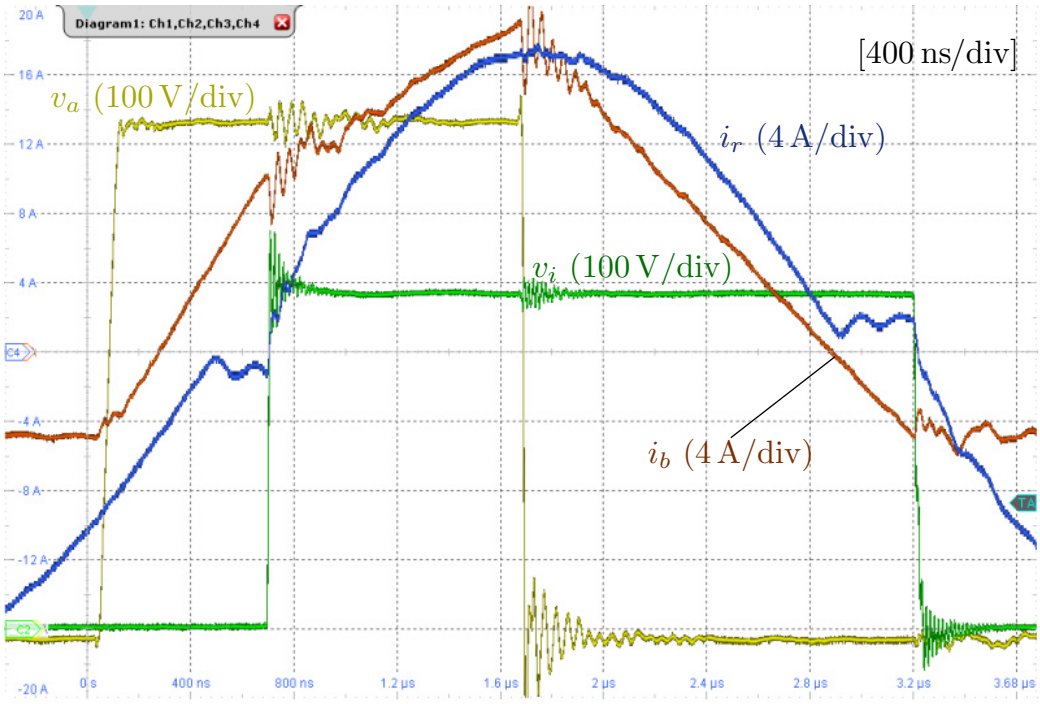
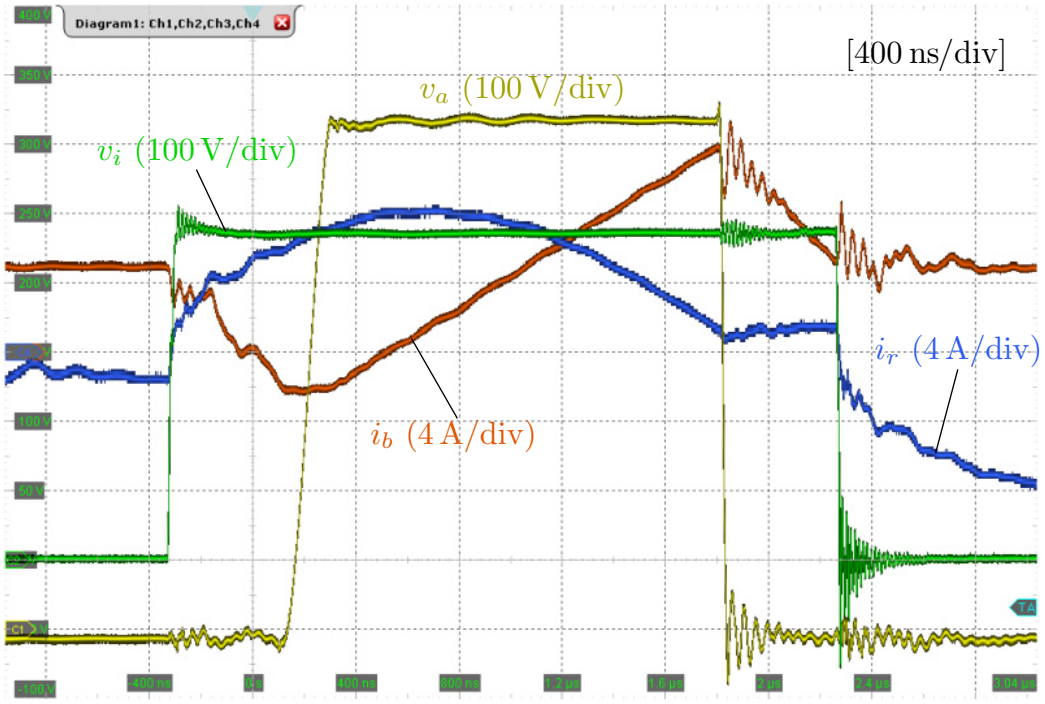


Figure 5.12: Photo of the implemented experimental prototype of BB-LLC.



(a) ZVS for all switches at $\varphi = 0.25$ (SM 2), $V_o = 250\,\mathrm{V}$, $P_o = 2.5\,\mathrm{kW}$



(b) Non-ZVS for S_{bL} at $\varphi = 0$ (SM 1), $V_o = 250\,\mathrm{V}$, $P_o = 1.1\,\mathrm{kW}$

Figure 5.13: Experimental waveforms at $V_o = 250\,\mathrm{V}$ during (a) ZVS operation at $\varphi = 0.25$, $P_o = 2.5\,\mathrm{kW}$, (b) non-ZVS operation at S_{bL}, $\varphi = 0$, $P_o = 1.1\,\mathrm{kW}$.

Table 5.2: BB-LLC prototype parameters.

Parameter	Symbol	Value	
Input voltage	V_g	750	V
Output voltage	V_o	250 - 500	V
Nominal power	P_o^{nom}	5	kW
Switching frequency	f_s	200	kHz
Leakage inductance	L_r	1.8	µH
Magnetizing inductance	L_m	180	µH
Inductance	L_b	30	µH
Turns ratio	n	1	-
Resonant capacitance	C_r	290	nF
S_{aH}, S_{aL}	SCT3040KR, SiC MOSFETs		
S_{bH}, S_{bL}	G3R30MT12K, SiC MOSFETs		
Output Rectifier	SK20KDD12SCp, SiC diodes		

with $\varphi = 0.25$.

With $\varphi = 0$, non-ZVS transitions for S_{bL} occur at low power levels, as expected based on simulation models. This precludes operation at output powers higher than $1.1\,\mathrm{kW}$, due to excessive switching loss in S_{bL}. Converter operation at such an operating point is displayed in Fig. 5.13a (i.e., $\varphi = 0$, $V_o = 250\,\mathrm{V}$, $I_o = 4.4\,\mathrm{A}$). At this point, S_{bL} experiences non-ZVS transitions, while ZVS is achieved for all the other switches. An increase of delivered output power with $\varphi = 0$ leads to higher switching and conduction loss and to non-ZVS transitions for switch S_{aH} too.

The thermometric images in Fig. 5.14 show significant differences in case temperature of S_{bL} while at the two operating points considered above. In spite of the lower transferred power, operation with $\varphi = 0$ gives temperatures of about 70°C, indicating significantly high losses on the transistor. Such a dissipation is not observed after properly adjusting φ, which is the degree of freedom available for modulation. By exploiting φ, ZVS for all the switches is achieved, allowing higher output power with overall lower losses, as shown by comparing Fig. 5.14a and Fig. 5.14b.

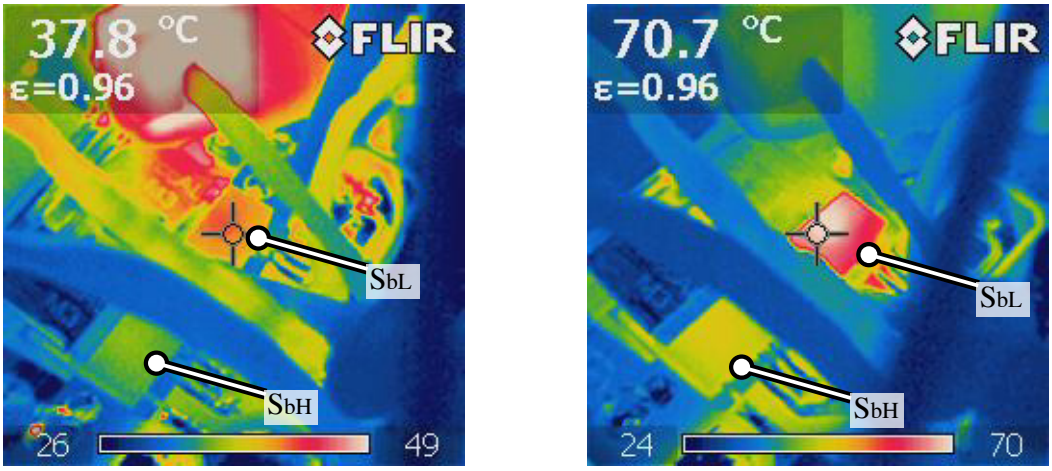


Figure 5.14: Thermography of S_{bH}-S_{bL} at $V_o = 250\,\mathrm{V}$ during (a) ZVS operation at $\varphi = 0.25$ and $P_o = 2.5\,\mathrm{kW}$; and (b) non-ZVS operation at S_{bL}, $\varphi = 0$, and $P_o = 1.1\,\mathrm{kW}$.

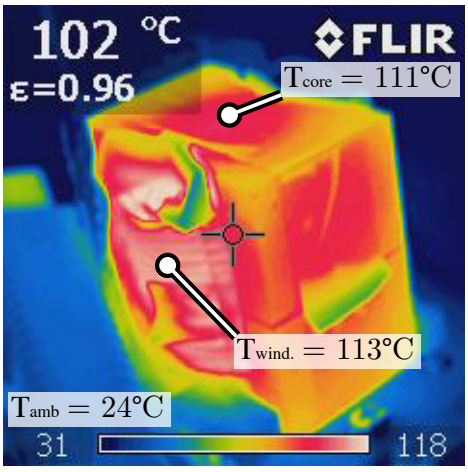


Figure 5.15: Thermography of the transformer at $V_o = 400\,\mathrm{V}$, and $P_o = 5\,\mathrm{kW}$.

5.5.2 Power Losses Measurement

Power loss measurements are conducted following the methodology described in Sect. 3.5. Fig. 5.15 shows the thermal figure of the transformer at the nominal design conditions in Fig. 5.9. The estimated power loss of the prototype is about $21\,\mathrm{W}$. Fig. 5.15 also reports core and windings temperatures, showing a uniform temperature profile for the component.

Power dissipation is measured based on thermal measurements of the magnetic component at thermal steady-state. Approaches based on similar principles and applications can be found adopted, for example, in [112]. For the results presented herein, in particular, the thermal resistance of the component is evaluated first, by means of a test consisting in the measurement of the average temperature of the component at thermal steady-state while stimulated by a constant dc current. Temperature measurements are performed through thermal couples positioned at four different points on the component surface, two on the windings and two on the core. A thermal resistance of about $4\,\mathrm{W/°C}$ is estimated as the average of different tests at different dc currents. Then, once the component-to-ambient thermal resistance R_θ is estimated, power dissipation could be computed. Other, more advanced, thermometric approaches are possible and described in the literature, like, for example, [111]. Similar considerations can be done for the inductor losses measurement.

A similar approach is applied to estimate the power dissipation of the switches. Switches temperatures are taken considering the spot at higher temperature on the case of the devices (see, e.g., Fig. 5.14). Thermal resistances of $1.6\,\mathrm{W/°C}$ and $1.8\,\mathrm{W/°C}$ are estimated for the left-leg and the right-leg MOSFETs, respectively. Then, referring to Fig. 5.14, it is possible to estimate losses of the devices: temperatures in Fig. 5.14a of S_{bL} correspond to about $9\,\mathrm{W}$, temperatures in Fig. 5.14b of S_{bL} correspond to about $26\,\mathrm{W}$.

5.5.3 Efficiency and Loss Breakdown

Fig. 5.16 shows the converter efficiency measured at the minimum, nominal, and maximum output voltage, that is, $250\,\mathrm{V}$, $400\,\mathrm{V}$, and $500\,\mathrm{V}$, respectively. Efficiency measurements are performed by means of a Keysight PA2203A power analyzer. The measured peak efficiency at minimum output voltage is 97.25%, while at maximum output voltage is 97.9%,

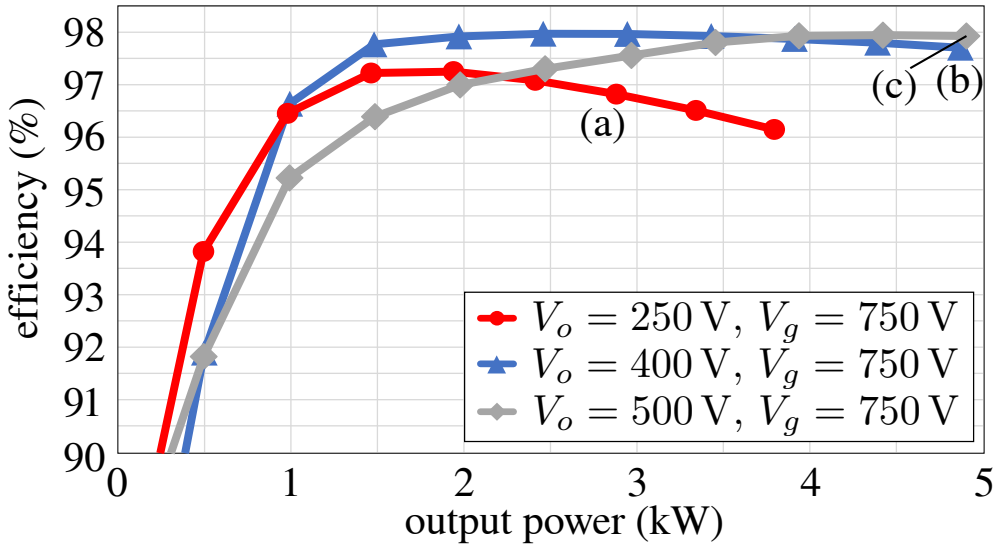


Figure 5.16: Measured efficiency at minimum, nominal, and maximum output voltage.

which are both very close to the absolute maximum efficiency of 98.0% measured in nominal conditions. Notably, there are some efficiency degradations due to the high reactive currents in light-load conditions and maximum output voltage region. A loss breakdown over the considered wide output voltage range of operation is reported in Fig. 5.17. The loss breakdown is performed based on the models presented in the previous sections, which are validated experimentally by means of the thermal measurements discussed in Sect. 5.5.2. The total discrepancy among estimations based on the described models and the collected measurements resulted lower than about 10% of the measured total power loss.

Finally, to prove ZVS operation achieved by exploiting the derived phase-shifts φ based on the analyses and considerations in Sect. 5.3, Fig. 5.18 shows the converter waveforms at other relevant points of operation. Remarkably, ZVS for all the switches is achieved with minimum phase-shift of 0.2 for $V_o = 250\,\mathrm{V}$ and $P_o = 3\,\mathrm{kW}$, of 0.12 for $V_o = 400\,\mathrm{V}$ and $P_o = 5\,\mathrm{kW}$, and of 0.24 for $V_o = 500\,\mathrm{V}$ and $P_o = 5\,\mathrm{kW}$, as expected based on the discussion in Sect. 5.3.3. The complete set of minimum phase-shifts for ZVS is reported in Fig. 5.6a at minimum output voltage, in Fig. 5.6c at nominal output voltage.

Compared with the state-of-the-art LLC converter designed for the same wide output voltage range, the converter proposed in Fig. 5.1 with efficiency performances in Fig. 5.16 shows an inherent better controllability at minimum output voltage, down to light load,

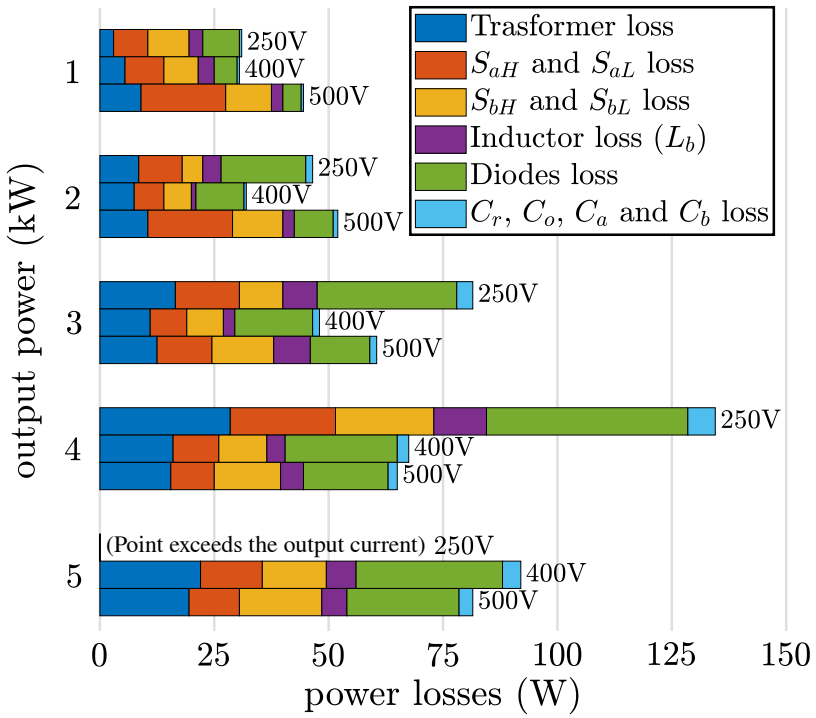
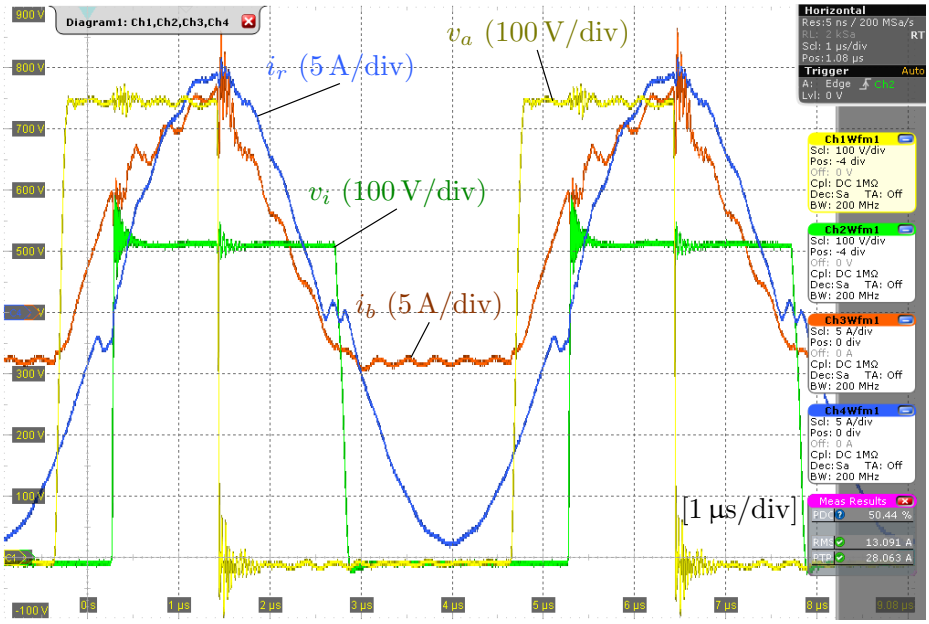


Figure 5.17: Loss breakdown at different output power and minimum, nominal, and maximum output voltages.

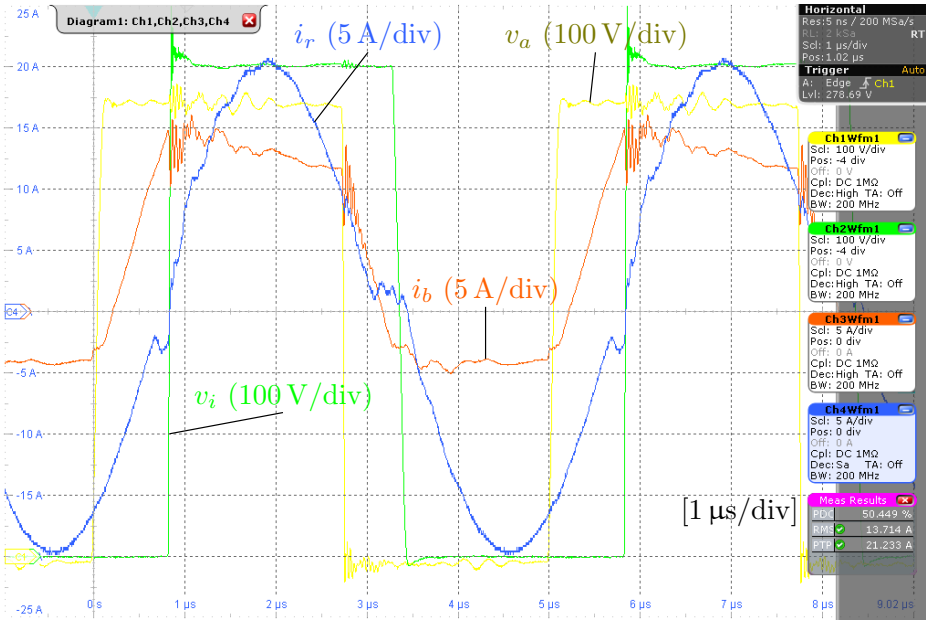
without the need of burst mode control strategies that can introduce electromagnetic interference (EMI) issues, high-frequency oscillations and issues in the control strategy [39]. However, some efficiency drawbacks remains in light-load conditions and maximum output voltage region.

5.6 Summary

This chapter delved into a comprehensive analysis and experimental validation of the proposed BB-LLC converter, which is introduced in Sect. 2.3.1 and previously subjected to simulation-based evaluation in Sect. 4.4.2. The BB-LLC represents a two-stage isolated structure that integrates a pre-regulation stage with a half-bridge LLC stage. The second stage operates at resonance to ensure high efficiency, while the pre-regulation stage ensures the desired input-to-output voltage conversion and facilitates ZVS operation of the switches. The two stages share part of the switching components. It is shown that, by a coordinated operation of the two stages, the switched currents can advantageously com-

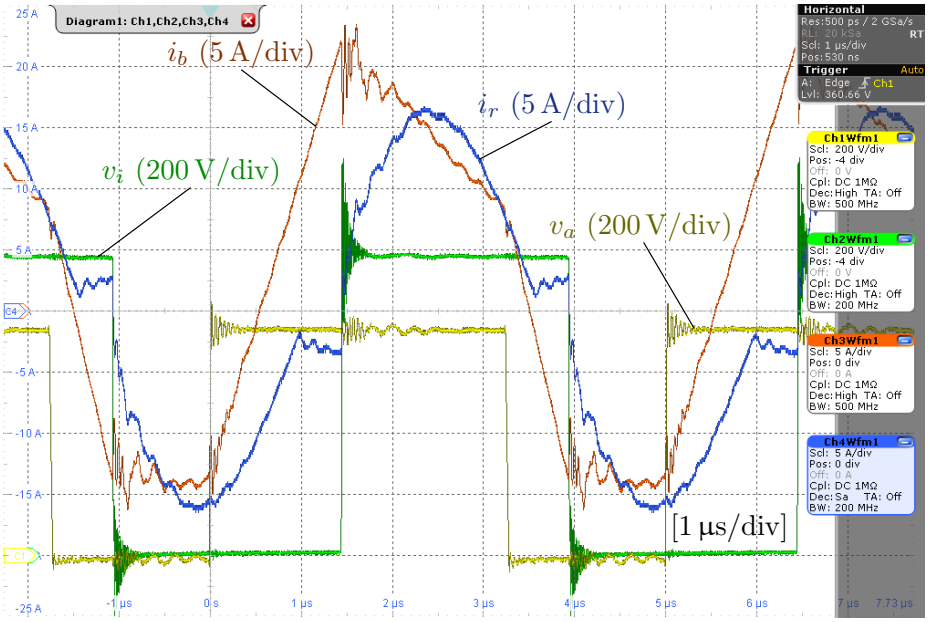


(a) Converter waveforms at $V_o = 250\,\text{V}$, $P_o = 3\,\text{kW}$. Soft-switching transitions, $\varphi = 0.2$.



(b) Converter waveforms at $V_o = 400\,\text{V}$, $P_o = 5\,\text{kW}$. Soft-switching transitions, $\varphi = 0.12$.

Figure 5.18: Converter waveforms for (a) $V_o = 250\,\text{V}$, $P_o = 3\,\text{kW}$; (b) $V_o = 400\,\text{V}$, $P_o = 5\,\text{kW}$; and (c) $V_o = 500\,\text{V}$, $P_o = 5\,\text{kW}$. Such points refer to those ones labeled in Fig. 5.16. ZVS is achieved at minimum phase-shift and, then, at minimum rms currents.



(c) Converter waveforms at $V_o = 500\,\mathrm{V}$, $P_o = 5\,\mathrm{kW}$. Soft-switching transitions, $\varphi = 0.24$.

Figure 5.18: Converter waveforms for (a) $V_o = 250\,\mathrm{V}$, $P_o = 3\,\mathrm{kW}$; (b) $V_o = 400\,\mathrm{V}$, $P_o = 5\,\mathrm{kW}$; and (c) $V_o = 500\,\mathrm{V}$, $P_o = 5\,\mathrm{kW}$. Such points refer to those ones labeled in Fig. 5.16. ZVS is achieved at minimum phase-shift and, then, at minimum rms currents.

bine to have ZVS over a wide range of output voltages, while limiting rms currents. As a result, a modulation scheme is derived for high-efficiency operation, aiming at ZVS with minimum rms currents. This configuration allows for efficient operation, targeting battery charging applications with a wide range of operating voltages.

The chapter started by providing an in-depth exploration of the converter's structure and operation. Subsequently, a detailed analysis of its performance characteristics is presented, encompassing discussions on the design considerations for the magnetic components. The chapter then present the experimental validation of the converter's performance. The results confirmed that ZVS is crucial in order to achieve minimum total loss, which can be obtained by the derived modulation scheme. The experimental prototype is designed to connect a $750\,\mathrm{V}$ dc-link to an output bus featuring a nominal voltage range of $250\,\mathrm{V}$ - $500\,\mathrm{V}$, accordingly to the application requirements in Sect. 1.3. The considered output voltage range may be easily extended by the series connection of more modules. The realized module, rated at $5\,\mathrm{kW}$, exhibited a peak efficiency of 98.0% when operating at an output power of $3\,\mathrm{kW}$.

By merging theoretical insights with practical verification, this chapter aimed to provide a comprehensive understanding of the operational behavior and potential advantages of the BB-LLC converter. The experimental results showcased its efficiency performances and broad controllability range, all achieved with the same component count as a conventional LLC converter. The unique structure of the BB-LLC, featuring the integration of a half-bridge LLC stage with a boost structure that shares switches, contributes to a reduction in the number of switching devices compared to other two-stage configurations (refer, for example, to Sect. 4.5). However, the utilization of the boost stage for voltage regulation, along with its associated high conduction losses, significantly impacts efficiency, particularly in the maximum output voltage region and in light-load conditions.

Chapter 6

CLLC + Twin-Bus Buck Converter

Chapter in Brief

In this chapter, a detailed analysis and experimental validation of the proposed CLLC + twin-bus buck (TBB) converter, introduced in Sect. 2.3.3 and previously evaluated through simulations in Sect. 4.4.4, is presented. The TBB is a two-stage isolated dc-dc converter that employs a first two-output isolation stage with CLLC resonant structure and a second two-input buck regulator. The transformer of the first stage is designed such that its two output voltages correspond, ideally, to the minimum and maximum expected voltage to be supplied to the battery. Then, the second stage combines the voltages provided by the previous isolation stage to regulate the output voltage of the whole converter. The first stage is always operated at resonance, with the only function of providing isolation and fixed conversion ratios with minimum losses, whereas the second stage allows output voltage regulation over a wide range of battery voltages. Overall, it is shown that the solution features high conversion efficiency over a wide range of output voltages. This chapter comprehensively describes the solution, including modeling, analyses, design considerations for the main circuit components (e.g., magnetics, switches), and modulation choices. Experimental results are reported considering a converter module prototype rated $10\,\mathrm{kW}$, input voltage $800\,\mathrm{V}$, and output range $250\,\mathrm{V}$ to $500\,\mathrm{V}$, employing silicon-carbide and gallium-nitride semiconductors. Input and output voltages are compliant with those introduced in Sect. 1.3 for the considered EV charging application.

6.1 Introduction

Output voltage regulation emerges as an exceedingly promising solution tailored for EV applications. To enhance the performance of the LLC resonant dc-dc converter across a wide output-voltage range, a two-stage conversion structure in which the second stage per-

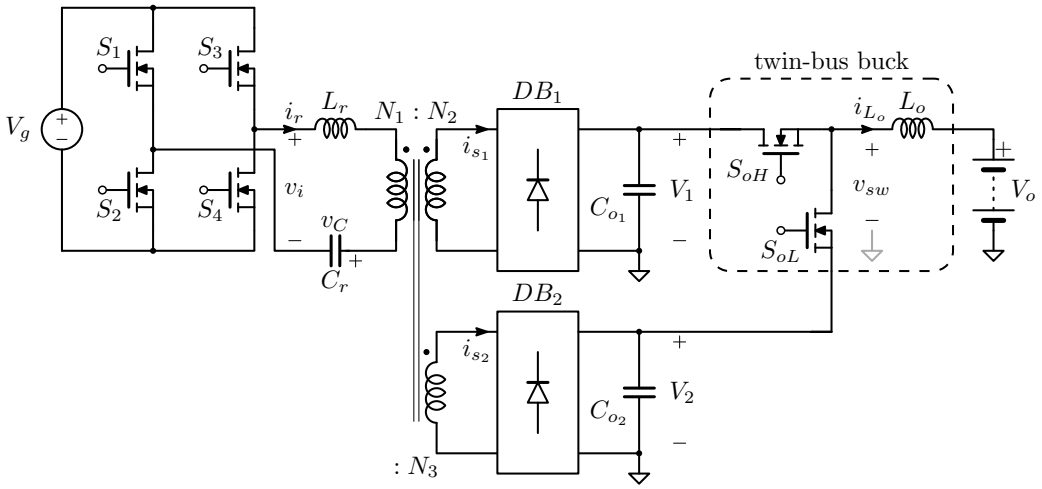


Figure 6.1: Two-stage converter with two-output DCX-LLC & TBB post-regulator.

forms the post-regulation of the output voltage is introduced in this chapter. The structure is re-proposed in Fig. 6.1 for ease of documentation. The post-regulation stage is directly connected to intermediate dc-links (i.e., V_1 and V_2), supplied by an isolation stage based on a resonant LLC-like structure with dual outputs. The underlying principle of this solution is to operate the input isolation stage at peak efficiency and employ the post-regulation stage to perform output voltage regulation with minimal voltage stresses. Operating the second stage with constrained voltage stresses holds the potential for achieving low conversion losses across the extensive range of output voltages relevant to EV battery charging. Remarkably, this converter structure also exhibits characteristics reminiscent of PPP, where only a portion of the rated power is processed by the buck post-regulator, thereby augmenting overall efficiency. Accordingly to the application specifications in Sect. 1.3, herein the solution is demonstrated with reference to a dc-dc conversion module rated $10\,\mathrm{kW}$ with a nominal input voltage of $800\,\mathrm{V}$ and output voltage ranging from $250\,\mathrm{V}$ to $500\,\mathrm{V}$. With its features and better efficiency characteristics in Sect. 4.5, this topology is a promising candidate for addressing the efficiency challenges associated with the dc-dc conversion structures for EV charging applications.

Part of the content of this chapter has been published in [25, 80, 119].

6.2 Operating Principle

6.2.1 Converter Configuration

Several configurations of two-stage dc-dc converters exploiting a voltage post-regulator are described in the literature [57, 77, 78]. As shown in Fig. 6.1, the proposed two-stage converter consists of a first isolation stage based on an LLC resonant converter, and a second post-regulator stage based on a buck converter. Such a post-regulator is responsible of the output voltage regulation and it is supplied by means of a high-efficiency two-output DCX converter, with secondary voltages V_1 and V_2. From Fig. 6.1, it is clear that the voltage stress of the post-regulator, namely, $V_1 - V_2$, is lower that the output voltage V_o, which consequently allows switching devices with smaller on-resistance as well as lower switching losses.

6.2.2 Operation

The two-output LLC resonant converter is designed for a constant voltage conversion ratio, independent from the actual load. In such an operating condition the LLC behaves as two-output DCX converter and its voltage gains can be defined as follows:

$$\begin{aligned} G_1 &= \frac{V_1}{V_g} = \frac{N_2}{N_1} = n_1 \\ G_2 &= \frac{V_2}{V_g} = \frac{N_3}{N_1} = n_2 \end{aligned} \tag{6.1}$$

where N_1, N_2, and N_3 are the number of turns of the three windings of the transformer, as indicated in Fig. 6.1.

The two-input post-regulator, herein referred to as twin-bus buck (TBB) converter, is highlighted in Fig. 6.1 while its main waveforms are displayed in Fig. 6.2. It is based on a two-input buck topology [120, 121], designed to operate in quasi-square wave, that is, with a peak-to-peak inductor current ripple higher than twice the average load current. This allows zero-voltage turn-on of both the switches S_{oH} and S_{oL}. The TBB is responsible of the output voltage regulation of the whole converter. The output voltage V_o is a function of

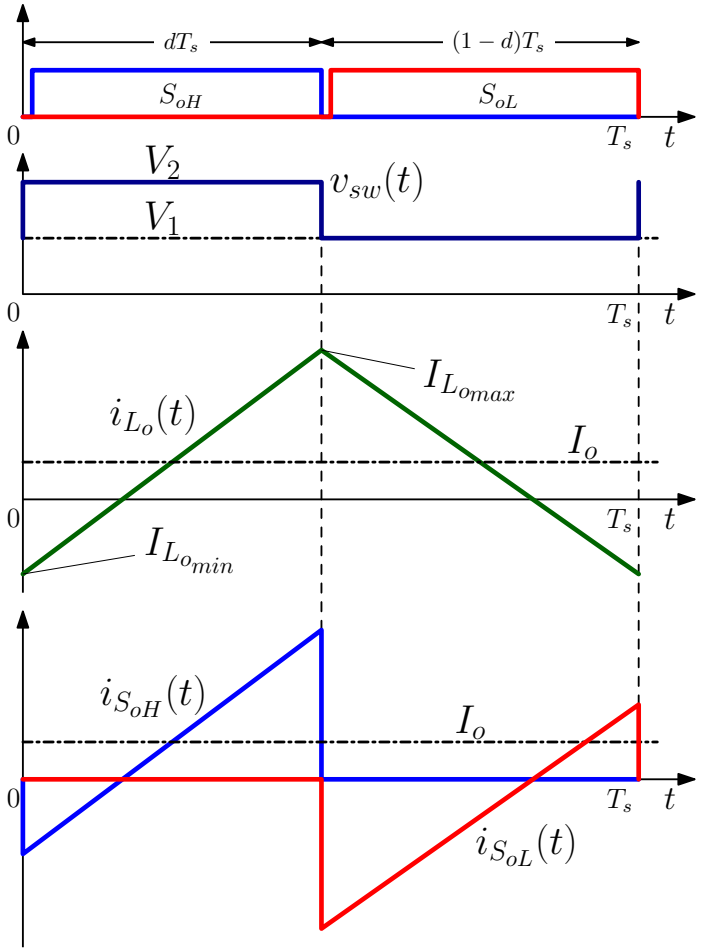


Figure 6.2: Main waveforms of TBB stage shown in Fig. 6.1. In order: gate driver signals including dead times, switching node voltage of TBB, L_o inductor current and S_{oH}, S_{oL} switch currents.

the TBB input voltages V_1 and V_2, with $V_1 > V_2$, and the duty cycle d of the upper switch S_{oH}:

$$V_o = d\,V_1 + (1-d)\,V_2 \tag{6.2}$$

Therefore, the voltage gain of the converter in Fig. 6.1 results:

$$G = \frac{V_o}{V_g} = d\,n_1 + (1-d)\,n_2 \tag{6.3}$$

For fixed input voltages V_1 and V_2, the minimum and maximum output voltages can be

defined as:

$$\begin{aligned} V_o^{\min} &= d^{\min} V_1 + (1 - d^{\min}) V_2 \\ V_o^{\max} &= d^{\max} V_1 + (1 - d^{\max}) V_2 \end{aligned} \tag{6.4}$$

with $d^{\min}$ and $d^{\max}$ the minimum and maximum duty cycles of S_{oH}, corresponding to $V_o^{\min}$ and $V_o^{\max}$ in Table 6.1, respectively. Their value must guarantee the zero-voltage switching operation of S_{oH} and S_{oL} at the respective output voltage levels. Thus the needed input voltages V_1 and V_2 provided by the DCX stage, can be calculated from (6.4) as:

$$\begin{aligned} V_1 &= \frac{V_o^{\max}(1 - d^{\min}) - V_o^{\min}(1 - d^{\max})}{d^{\max} - d^{\min}} \\ V_2 &= \frac{V_o^{\min} d^{\max} - V_o^{\max} d^{\min}}{d^{\max} - d^{\min}} \end{aligned} \tag{6.5}$$

and the voltage gains (6.1) of the DCX-LLC can be derived.

By using (6.5), the maximum voltage stress of the switches can be computed as:

$$V_1 - V_2 = \frac{V_o^{\max} - V_o^{\min}}{d^{\max} - d^{\min}} \tag{6.6}$$

which is always lower than the voltage stress of the switches of a full-power converter that requires a supply voltage higher than the maximum output voltage. In order to minimize such voltage stress, and the related switching loss, the duty-cycle excursion $d^{\max} - d^{\min}$ should be maximized; then, for example, by imposing $d^{\min} = (1 - d^{\max}) = 5\%$. Consequently, the converter in Fig. 6.1 with voltage ratings $V_o^{\max} = 2\,V_o^{\min} = 500\,\mathrm{V}$ presents a voltage stress on the switching devices of $V_1 - V_2 = 278\,\mathrm{V}$, allowing the use of devices of low rated-voltages, which typically implies lower losses [55, 56].

Once the duty-cycle range of the TBB stage is defined, ZVS can be achieved with a proper selection of the output inductor value and the switching frequency, for the whole output voltage range. As shown in Fig. 6.2, the TBB is operated in continuous conduction

mode (CCM) and the inductor current at switching instants can be computed as:

$$\begin{aligned} I_{L_{o_{max}}} &= I_o + \frac{V_1 - V_2}{2 f_s L_o} d\,(1-d) \\ I_{L_{o_{min}}} &= I_o - \frac{V_1 - V_2}{2 f_s L_o} d\,(1-d) \end{aligned} \tag{6.7}$$

In order to achieve zero-voltage switching, these current values should satisfy the minimum switched current conditions for ZVS. A similar procedure to that one presented in Sect. 5.3.1 is adopted for the optimal inductance selection. In Ch. 7 is presented an on-line approach to select the optimal switching frequency ot the TBB stage. The inductor current value and the switching frequency of the TBB stage are key parameters for the converter design and operation over the whole range of output voltages and powers.

6.3 DCX Stage Design Considerations

The converter structure is shown in Fig. 6.1. When the LLC resonant tank is operated at the resonance frequency, the voltage conversion ratio becomes ideally independent from the actual load. In other words, the LLC converter maintains a constant voltage conversion ratio and adjusts its current automatically, according to the load conditions, behaving as a DCX. In this operating condition, the LLC shows its maximum efficiency, with a minimum flow of reactive power and ZVS and ZCS conditions always satisfied [55]. Notably, the DCX operation of the LLC does not require an external resonant inductor, because the conversion gain is fixed. An equivalent solution based on a resonant FB-LLC designed to operate over the same wide range of output voltages shows higher losses than the LLC in permanent DCX conditions, as demonstrated in Sect. 4.4.1.

6.3.1 Transformer Design

From (6.1) and (6.5) and considering $d^{\min} = (1 - d^{\max}) = 5\%$, the transformer turns ratio can be calculated as $n_1 = N_2/N_1 = 0.642$ and $n_2 = N_3/N_1 = 0.295$ to make the LLC converter operate at the resonant frequency f_s at input voltage $V_g = 800\,\mathrm{V}$ and output bus voltages V_1 and V_2 as in (6.5).

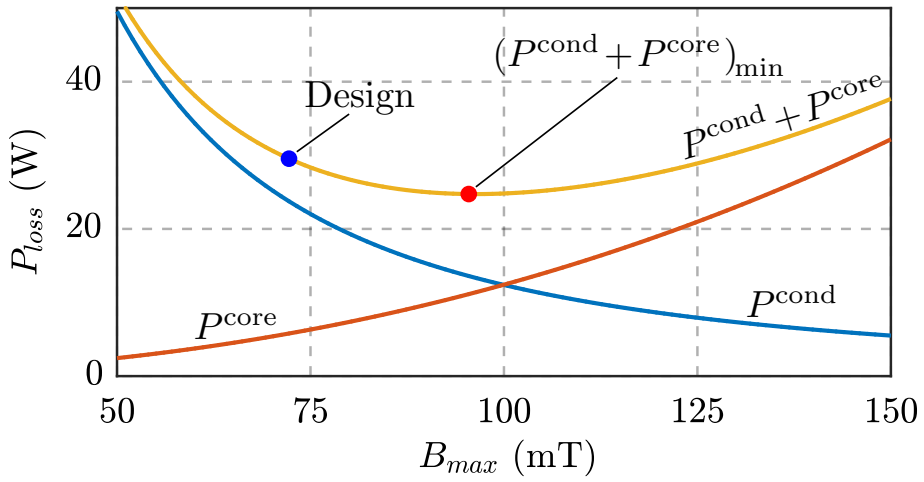


Figure 6.3: P-B plot for transformer design at $V_o = 400\,\text{V}$ and $P_o = 10\,\text{kW}$.

Transformer design procedure follows the guidelines reported in Sect. 3.3.3. Fig. 6.3 reports the results of the calculated transformer losses, showing a total loss of $24\,\text{W}$ at nominal conditions, namely, $V_1 = 514\,\text{V}$ and $V_2 = 236\,\text{V}$, and $P_o = 10\,\text{kW}$. According with Fig. 6.3, the selected design point is more conservative in terms of core losses with respect to the optimal point, this is due to a trade-off between the desired magnetizing inductance and the discrete conductor sections.

Fig. 6.4 depicts the winding layout of the designed transformer of Fig. 6.5a. The designed transformer presents turns ratio $n_1 = 0.625$ and $n_2 = 0.292$, current density $J_0 = 5\,\text{A/mm}^2$, number of turns per winding $N_1 = 24$, $N_2 = 15$, $N_3 = 7$.

6.3.2 Resonant Tank Design

For what concerns the design of the resonant L_rC_r tank, the transformer leakage inductance can be exploited for the implementation of the inductive part. Given the DCX operation mode of the LLC, low values of L_m can be used, which is beneficial in terms of transformer design, losses, and resonant capacitor voltage stress. With the aimed DCX operation, the value of the magnetizing inductance L_m is typically chosen to ensure a sufficiently high magnetizing current to allow ZVS for all the switches of the main converter. A classical design for a DCX-LLC with voltage ratings of Table 6.1 requires a magnetizing inductance of about $200\,\mu\text{H}$ (see, for example, [26, 35, 55]). The designed transformer in Fig. 6.5a

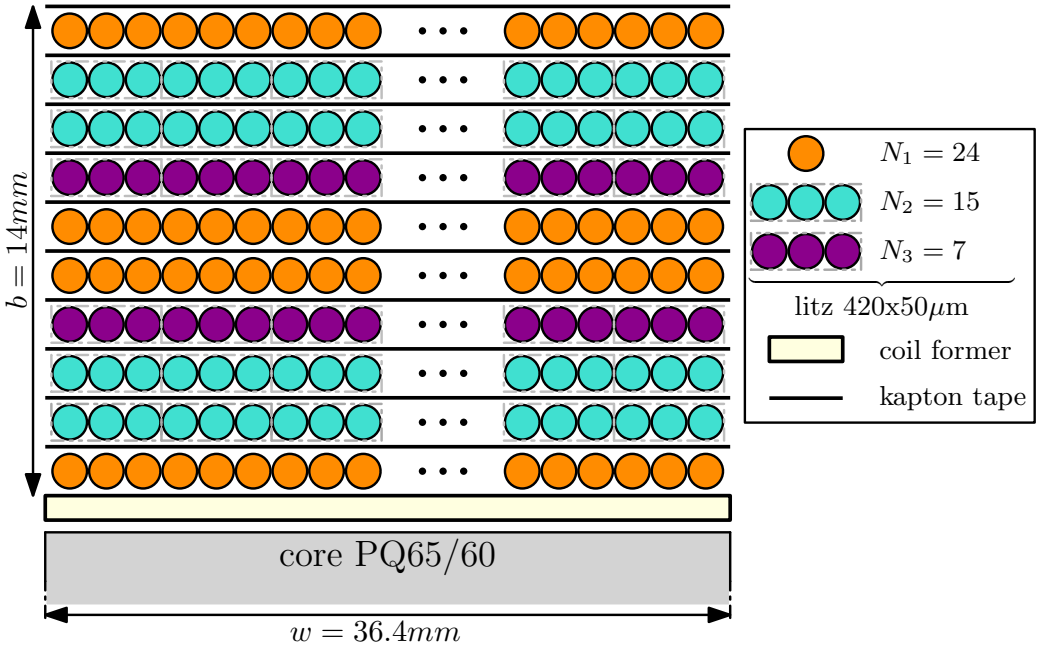
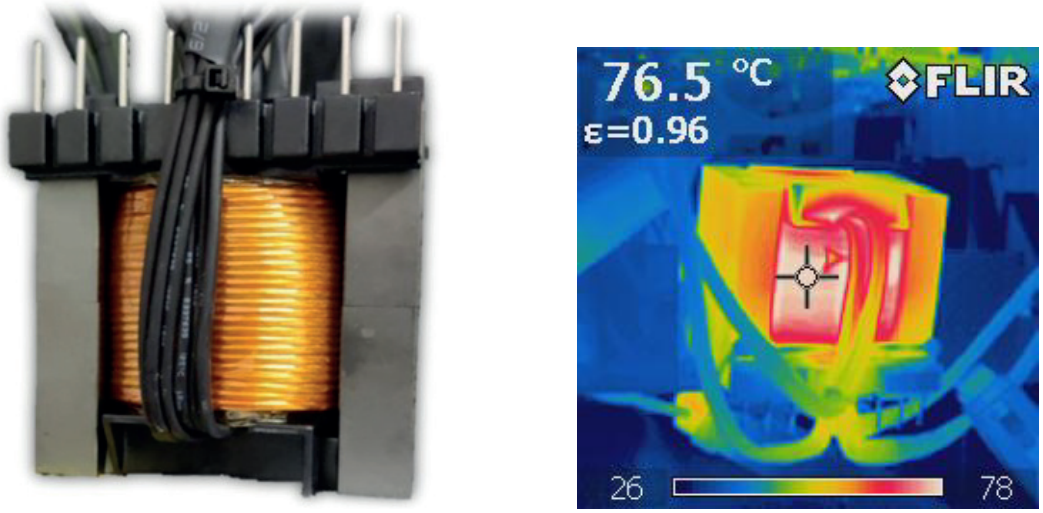


Figure 6.4: Winding arrangement at the design point in Fig. 6.3.



(a) **(b)**

Figure 6.5: (a) Transformer prototype; and (b) thermography at the design point in Fig. 6.3, namely, $V_o = 400\,\mathrm{V}$ and $P_o = 10\,\mathrm{kW}$, natural convection conditions.

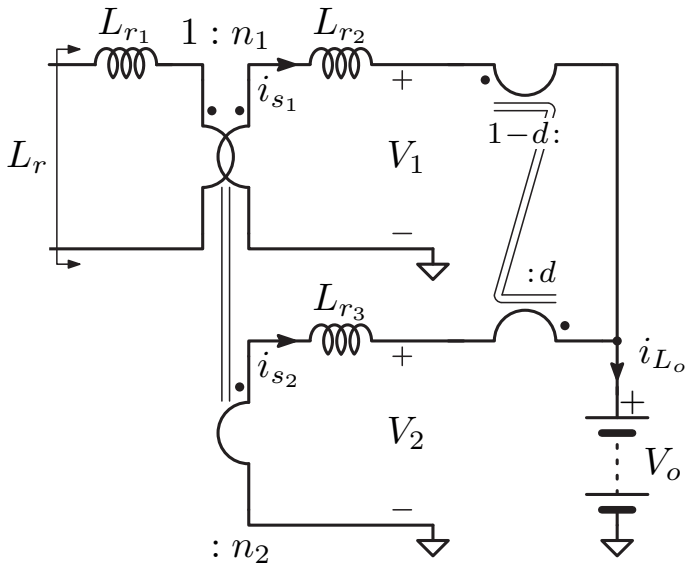


Figure 6.6: Equivalent circuit model for the estimation of resonant inductance at the primary side of the transformer, namely L_r in Fig. 6.1.

achieves the design target, with a magnetizing inductance of about $215\,\mu\mathrm{H}$.

The capacitive part of the resonant tank can be selected on the basis of the desired resonant frequency (i.e., converter switching frequency at DCX-LLC operation). The winding arrangement of the designed transformer in Fig. 6.3 is shown in Fig. 6.4. The interleaving of the primary and secondary-side windings is an effective solution to limit the leakage inductance and winding losses [90]. The experimental prototype in Fig. 6.5a, which results from the design in Fig. 6.3 and winding arrangement in Fig. 6.4, presents values of leakage inductances $L_{r_1} = 795\,\mathrm{nH}$, $L_{r_2} = 445\,\mathrm{nH}$, and $L_{r_3} = 271\,\mathrm{nH}$ for the input, high-voltage, and low-voltage windings, respectively. The secondary windings leakage inductances L_{r_2} and L_{r_3} affect the overall resonance frequency proportionally to the normalized conduction interval of the respective diode bridge rectifier. In fact, these inductances come into play only when the corresponding rectifying diodes are conducting, and these intervals are related to the duty-cycle of the TBB stage, as well as to the load current. The TBB stage imposes a strict relationship between the average charge transferred through each output ports of DCX-LLC stage with respect to the output voltage V_o and current I_o. Then, the stage can be modelled as shown in Fig. 6.6. The series-equivalent inductance L_r of the

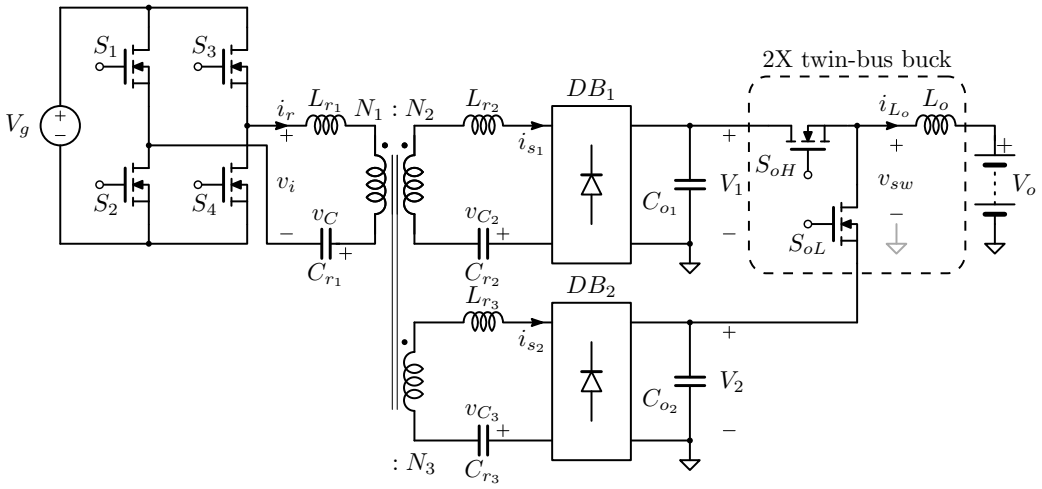


Figure 6.7: Overall circuit schematic of the solution described herein, composed of a DCX-CLLC stage plus two interleaved twin-bus buck stages.

resonant tank referred to the primary side of Fig. 6.6 can be calculated as:

$$L_r = L_{r_1} + \frac{d^2 L_{r_2} + (1-d)^2 L_{r_3}}{[n_1 d + n_2(1-d)]^2} \tag{6.8}$$

which is a function of the converter operating point, according to (6.2). The validity of (6.8) is shown in Sect. 6.3.3 referring to a specific operating point. In order to remove the dependence of the resonance frequency from the load, two additional resonant capacitors are connected in series with the two output ports of the transformer, as shown in Fig. 6.7. At resonance, the capacitive part of each of the series-resonant impedances $L_{r_i} C_{r_i}$ cancels out with the corresponding inductive part. $C_{r_1} = 796\,\mathrm{nF}$, $C_{r_2} = 1.42\,\mu\mathrm{F}$ and $C_{r_3} = 2.34\,\mu\mathrm{F}$ are then calculated as proper values for the resonant capacitances in order to achieve a continuous resonant current operation, where the resonant frequency of the CLLC stage becomes independent from the duty-cycle and the output current of the TBB stage, as otherwise shown in (6.8). The proposed post-regulated converter is then shown in Fig. 6.7.

6.3.3 Continuous Resonant Current Operation

A converter topology with parameters reported in Table 6.1 is considered for validation. Based on the considerations reported in Sect. 6.3, herein are reported the simulation results focused on demonstrating the continuous resonant current operation of the DCX stage.

Table 6.1: Implemented TBB converter parameters.

Parameter	**Symbol**	**Value**	
Input voltage	V_g	800	V
Output voltage	V_o	250 - 500	V
Nominal output voltage	V_o^{nom}	400	V
Maximum output current	I_o^{max}	25	A
Nominal power	P_o^{nom}	10	kW
Switching freq. of CLLC	f_s	200	kHz
Switching freq. of TBB	f_{s_o}	50 - 400	kHz
Turns ratio N_2/N_1	n_1	0.625	-
Turns ratio N_3/N_1	n_2	0.292	-
Intermediate bus V_1	V_1	500	V
Intermediate bus V_2	V_2	234	V
Magnetizing inductance	L_m	215	µH
	L_{r_1}	795	nH
Leakage inductances	L_{r_2}	445	nH
	L_{r_3}	271	nH
TBB inductor	L_o	30	µH
Transformer	Core: PQ65/60, material: N87		
Inductor	Core: PQ40/40, material: N97		
	C_{r_1}	796	nF
Resonant capacitances	C_{r_2}	1.42	µF
	C_{r_3}	2.34	µF
S_{a_1}, S_{a_2}, S_{b_1}, S_{b_2}	G3R30MT12K, 1.2 kV SiC MOSFETs		
S_{oH}, S_{oL}	LMG3422R030, 600 V GaN FET		
Output rectifier DB_1	UJ3D06560KSD, 650 V SiC diodes		
Output rectifier DB_2	STTH100W04CW, 400 V Si diodes		

First, the operation of the converter in Fig. 6.1 is considered with a single resonant capacitor C_r and, then, the operation of the proposed converter in Fig. 6.7 is considered. Converters in Fig. 6.1 and Fig. 6.7 are simulated and the resonant currents are shown in Fig. 6.8. Different operating points at the maximum output current $I_o = 25\,\mathrm{A}$ and minimum, nominal, and maximum output voltage V_o (i.e., $250,\ 400,\ 500\,\mathrm{V}$) are considered. Figs. 6.8(a)-(c) shows the resonant currents i_r, i_{s_1}, and i_{s_2}, and the magnetizing current i_m of the circuit in Fig. 6.1 with resonant capacitance $C_r = 174\,\mathrm{nF}$. Such a value is designed to have the desired resonance frequency f_s, with $L_r = 3.64\,\mu\mathrm{H}$ given by (6.8) at $V_o = 250\,\mathrm{V}$. Indeed, the current i_{s_2} is resonant only in such an operating point. While, Figs. 6.8(d)-(f) shows the resonant currents considering the circuit in Fig. 6.7 with resonant capacitances C_{r_i} in Table 6.1. Simulation results show that the resonance conditions are satisfied, for the whole wide output voltage range, only in this later case. Furthermore, conduction losses are minimized only if the resonance conditions are satisfied. Based on the obtained results, the CLLC solution is considered for the investigations in the following.

6.4 Experimental Results

Fig. 6.9 displays the experimental prototype implementation of a module rated $10\,\mathrm{kW}$, with parameters in Table 6.1, used to validate the reported analysis, design choices, and feasibility of the proposed converter, in Fig. 6.7. Fig. 6.10 shows the measurement and control setup built around the proposed converter in order to collect the experimental results reported herein. Additional details related to the implemented hardware can be found in App. D. Fig. 6.11 shows the experimental validation of the considerations discussed in Sect. 6.3.3. In particular, Figs. 6.11(a), (c), (e) show the measured resonant currents at the same operating points of the simulated waveforms in Figs. 6.8(d), (e), (f), respectively. It is possible to appreciate that the current waveforms are very close to the continuous resonant current operation of the DCX-CLLC. The measured waveform amplitudes correspond to the expected values. The switching frequency is set to $f_s = 200\,\mathrm{kHz}$ and dead-time to $t_d = 260\,\mathrm{ns}$. If needed, additional refinements to match the true resonance frequency may be performed by adjusting the values of the resonant capacitors or the used operating

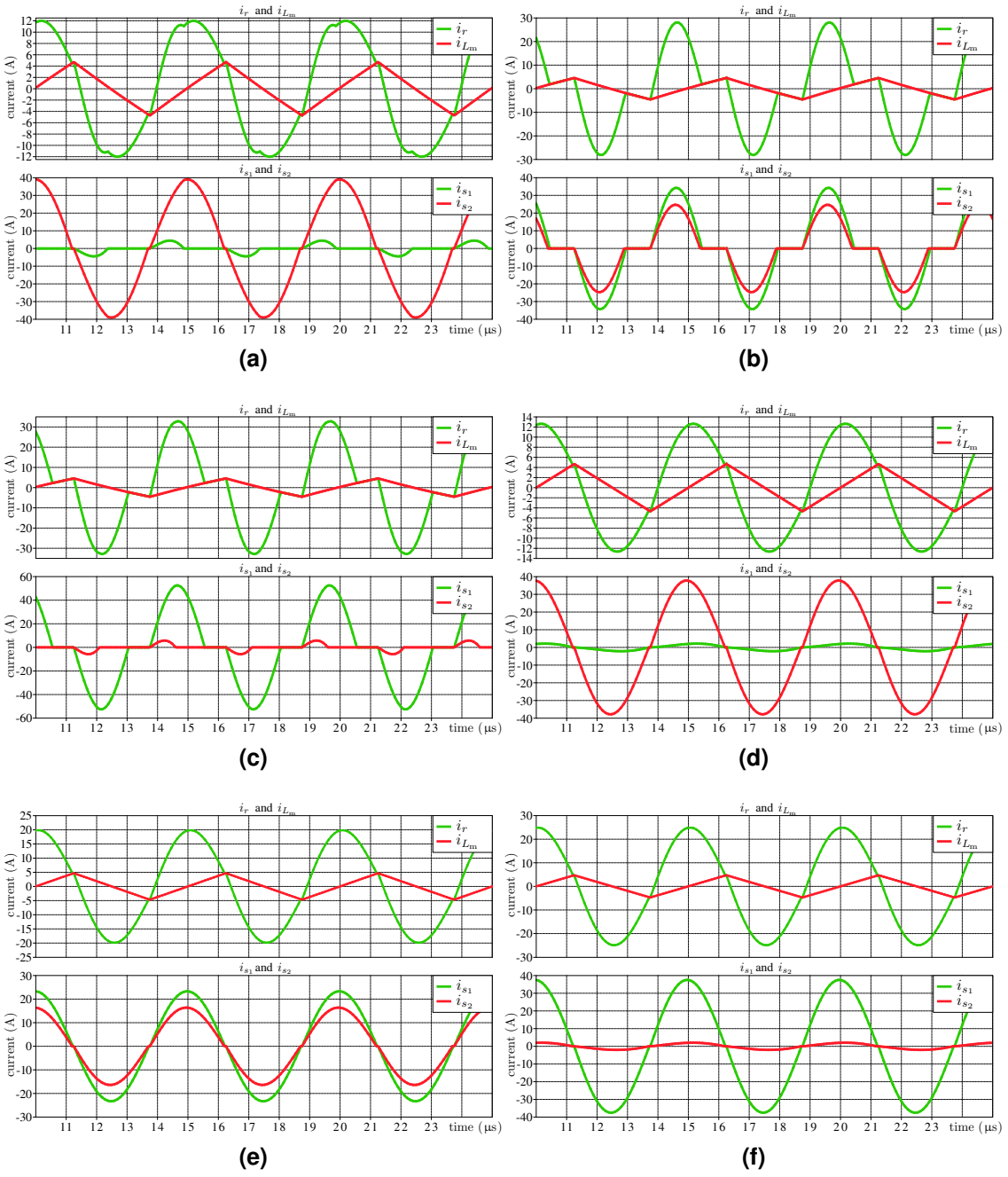


Figure 6.8: Simulation results for LLC with different resonant tank designs, (a)-(c) refer to Fig. 6.1; and (d)-(f) refer to Fig. 6.7. (a),(d) $V_o = 250\,\mathrm{V}$; (b),(e) $V_o = 400\,\mathrm{V}$; and (c),(f) $V_o = 500\,\mathrm{V}$. $I_o = 25\,\mathrm{A}$. Converter parameters are reported in Table 6.1.

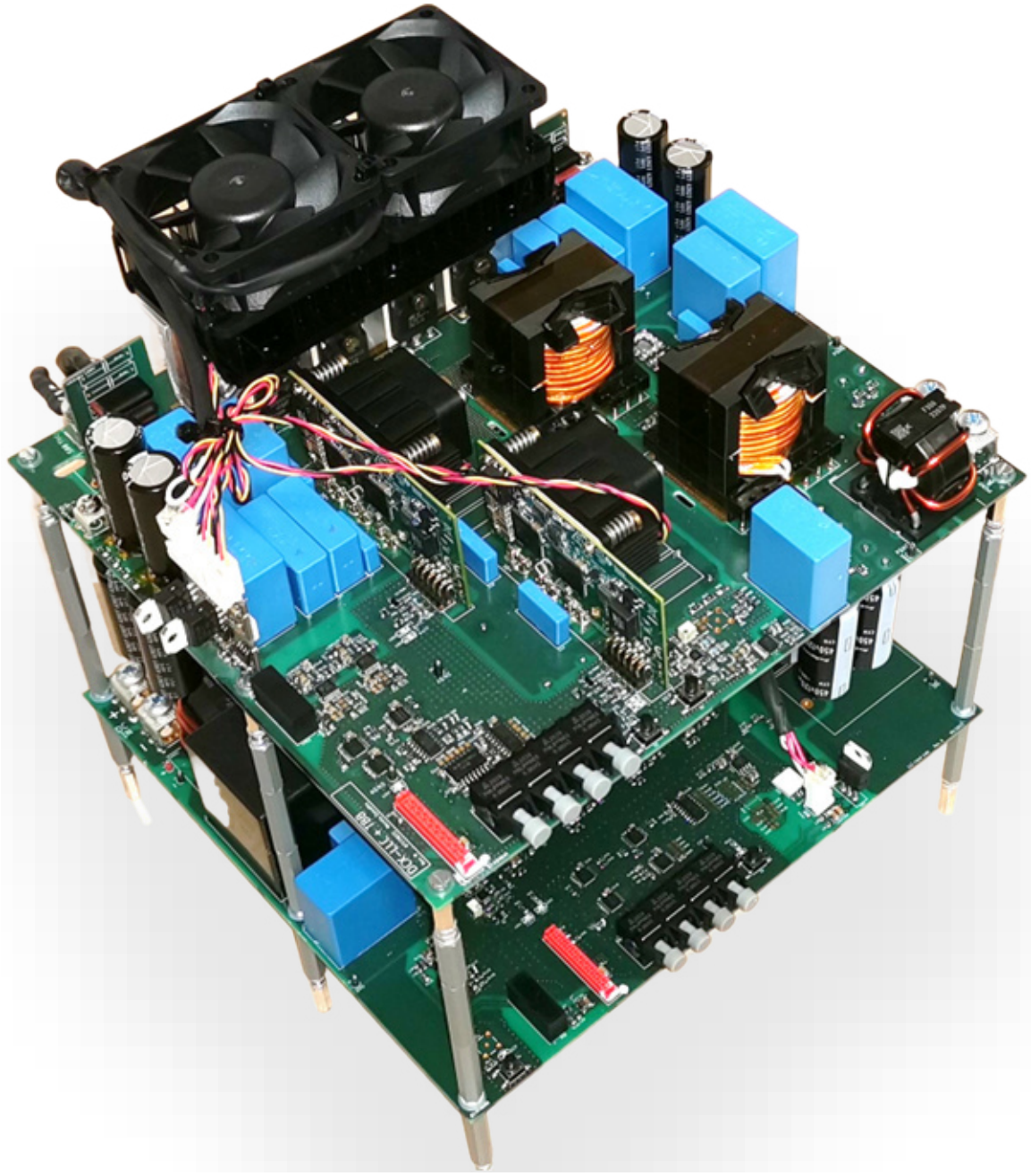


Figure 6.9: DCX-CLLC + twin-bus buck converter prototype.

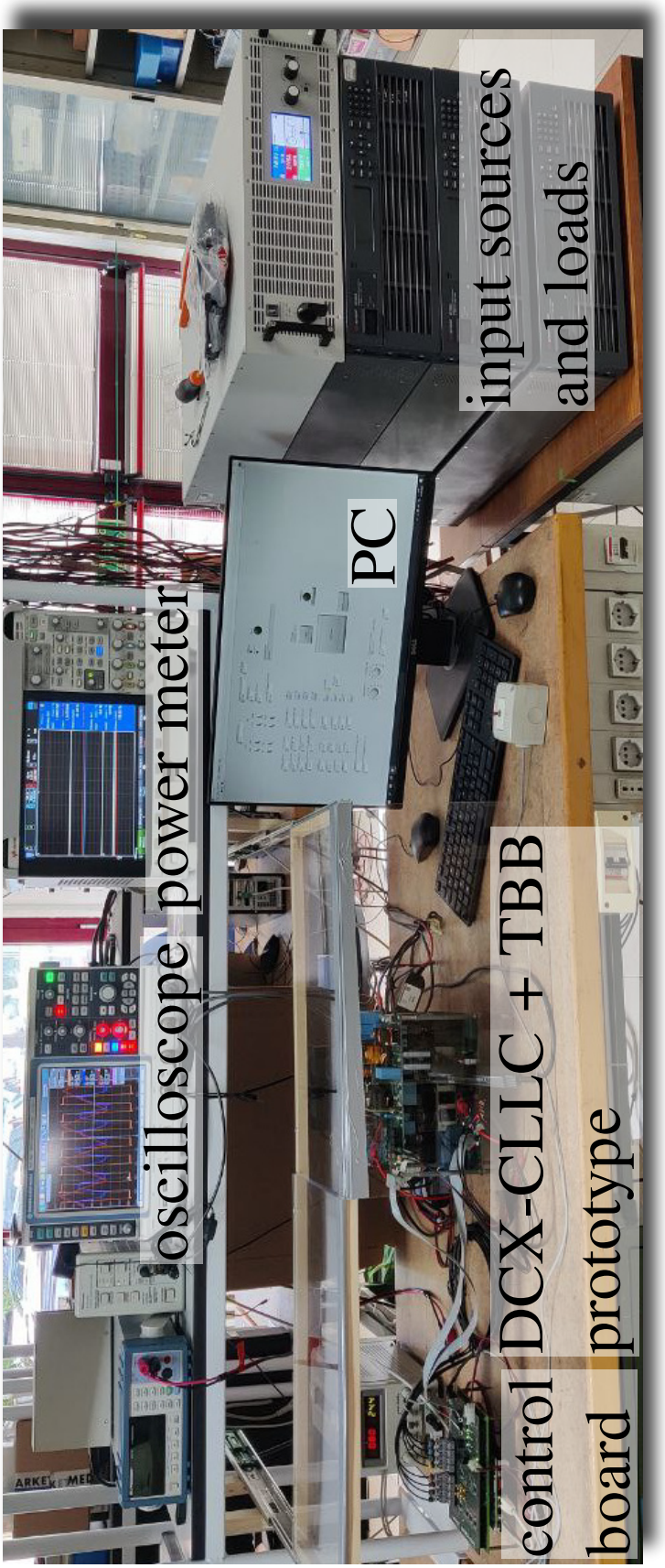


Figure 6.10: Experimental setup for validation.

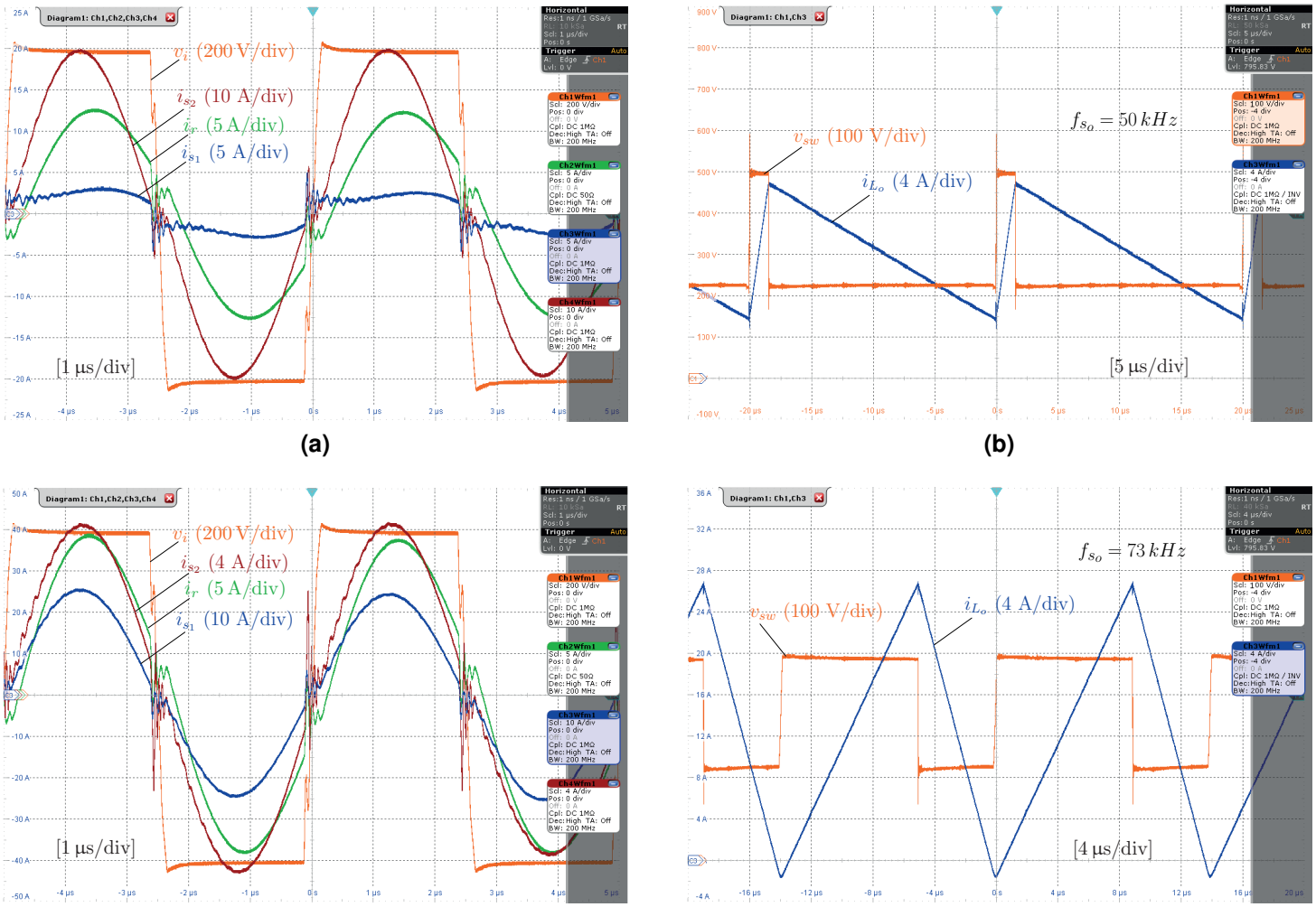


Figure 6.11: Experimental results of the proposed converter in Fig. 6.7 at $I_o = 25$ A. (a),(b) $V_o = 250$ V; (c),(d) $V_o = 400$ V; and (e),(f) $V_o = 500$ V. (a), (c), (e) are the experimental validations of the simulations in Figs. 6.8(d), (e), (f), respectively.

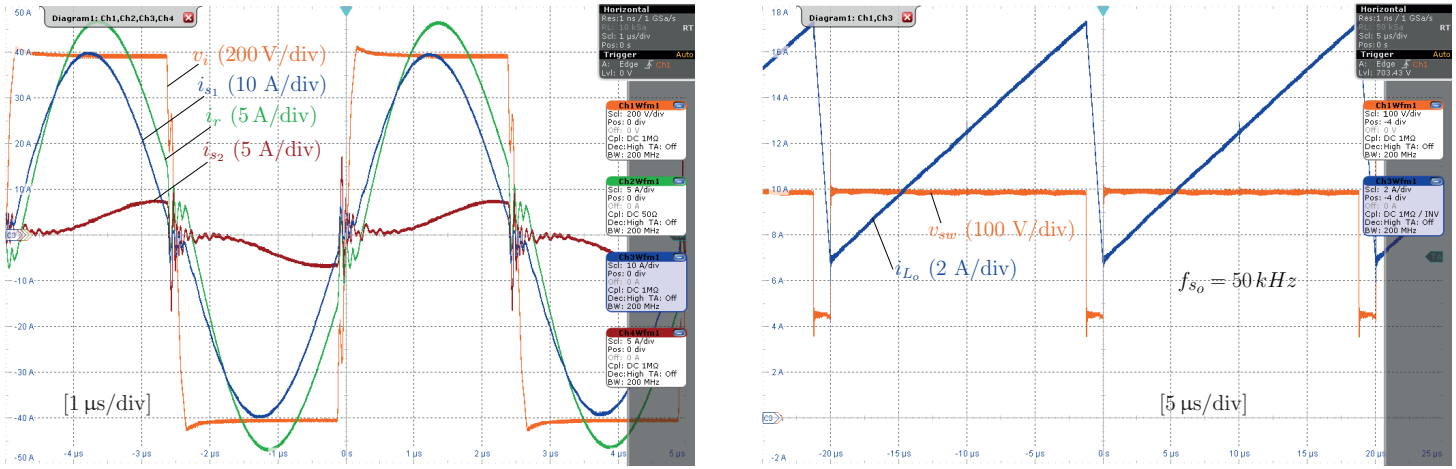


Figure 6.11: Experimental results of the proposed converter in Fig. 6.7 at $I_o = 25$ A. (a),(b) $V_o = 250$ V; (c),(d) $V_o = 400$ V; and (e),(f) $V_o = 500$ V. (a), (c), (e) are the experimental validations of the simulations in Figs. 6.8(d), (e), (f), respectively.

frequency in the controller [35, 122, 123].

Figs. 6.11(a), (b) show the converter waveforms at minimum output voltage $V_o = 250\,\mathrm{V}$ and output current $I_o = 25\,\mathrm{A}$. The duty-cycle of the TBB is set to 7%, and the switching frequency to the lower limit of $f_{s_o} = 50\,\mathrm{kHz}$. Such a lower limit comes from a trade-off between the dc-link capacitances and the output voltage ripple. The conversion efficiency in such an operating point is about 97.6%. For $V_o = 250\,\mathrm{V}$ ZVS conditions are not satisfied for average output currents higher than about $10\,\mathrm{A}$. Remarkably, the typical charging profile of a battery requires a constant current mode charging when the battery is discharged (i.e., at low battery voltages). In this condition, the charging current is maximum and equals to the output current $I_o^{\max}$ at the nominal output power (see, e.g., [3]), namely, $25\,\mathrm{A}$ at $10\,\mathrm{kW}$ in the considered case.

Figs. 6.11(c), (d) show the converter waveforms at nominal output voltage $V_o = 400\,\mathrm{V}$ and output current $I_o = 25\,\mathrm{A}$. The duty cycle of TBB is set to 65% and the switching frequency of the TBB is $f_{s_o} = 73\,\mathrm{kHz}$ in order to achieve ZVS. The conversion efficiency in such a point is about 98.4%.

Figs. 6.11(e), (f) show the converter waveforms at maximum output voltage $V_o = 500\,\mathrm{V}$ and output current $I_o = 25\,\mathrm{A}$. The duty cycle of the TBB is set to 95%, the switching frequency to the lower limit of $f_{s_o} = 50\,\mathrm{kHz}$. The conversion efficiency in such a point is about 98.5%. For $V_o = 500\,\mathrm{V}$, ZVS conditions are not satisfied for output currents higher than about $10\,\mathrm{A}$. Remarkably, the loss of ZVS in heavy load conditions and extreme duty-cycle is the direct consequence of the selected inductance L_o. Indeed, the selected value allows to achieve ZVS in light-load conditions and with a switching frequency of the TBB limited to $f_{s_o} = 400\,\mathrm{kHz}$. Optimal switching frequencies for the TBB stage are achieved using an on-line efficiency tracking algorithm, which is discussed in detail in Ch. 7.

Some ringing at the commutations of the input full-bridge current is visible in Figs. 6.11 (a), (c), (e). The ringing appears during the dead-times and is generated by resonances between the transformer leakage inductances and the devices output capacitances. These resonances may bring partial ZVS and ZCS conditions and eventually cause increased switching losses. This aspect is investigated in [35], which also proposes a method to reduce the related switching loss based on switching frequency and dead-time perturbations.

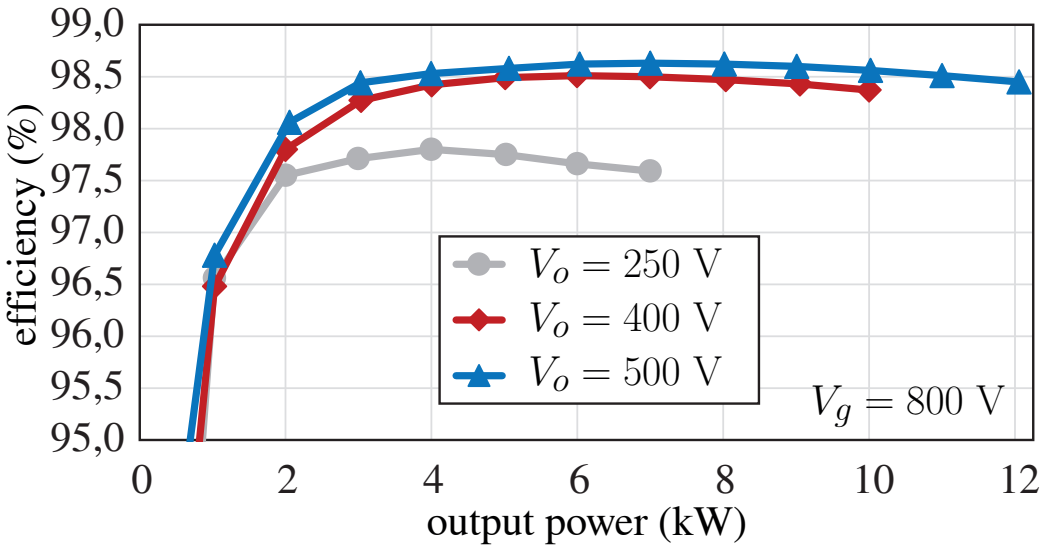


Figure 6.12: Measured TBB efficiency at minimum, nominal and maximum output voltage.

Finally, Fig. 6.12 shows the converter efficiency measured at the minimum, nominal, and maximum output voltage. Efficiency measurements are performed by means of a Keysight PA2203A power analyzer. The measured peak efficiency at minimum output voltage is 97.8%, while at nominal output voltage is 98.51%, which is very close to the absolute maximum efficiency of 98.63% measured at maximum output voltage conditions. Such values are very close to the estimations performed by the tuned simulation shown in Sect. 4.4.4.

6.5 Summary

This chapter delved into a comprehensive analysis and experimental validation of the proposed TBB converter, which is introduced in Sect. 2.3.3 and previously subjected to simulation -based evaluation in Sect. 4.4.4. The novel conversion structure, previously unexplored in the context of EV battery charging applications, is conceptualized, designed, and practically demonstrated within this chapter. The TBB represents a two-stage isolated structure that integrates a DCX-CLLC and a buck post-regulator. The DCX-CLLC converter always operates at its optimal operating point and the additional post-regulator based on a two-input buck converter is used to regulate the output voltage. In such a post-regulator, the stress of the switches is a fraction of the rated voltages. Hence, the efficiency of the pro-

posed configuration, compared with standard dc-dc converters processing full power, can be improved.

The chapter started by providing an in-depth exploration of the converter's structure and operation. Subsequently, a detailed analysis of its performance characteristics is presented, encompassing discussions on the design considerations for the magnetic components. Simulation results of the resonant two-output CLLC are reported. The chapter then present the experimental validation of the converter's performance. The reported analysis and the experimental characterizations and tests are performed on a $10\,\mathrm{kW}$ prototype module based on SiC devices and GaN devices.

The experimental results showcased its impressive efficiency performances and wide controllability range, confirming the simulation results in Sect. 4.5, all achieved at the cost of an increased component count compared to the conventional LLC converter. The reported experimental performances, aligned with the application prerequisites detailed in Sect. 1.3, demonstrated exceptional efficiency across a wide range of operating conditions. The efficiency record a remarkable 98.63% at an output voltage of $500\,\mathrm{V}$ and a transferred power of $7\,\mathrm{kW}$. Consequently, the TBB converter emerges as a promising topology, striking an optimal balance between component utilization and efficiency performance. Superior performances compared to the BB-LLC in Ch. 5 is demonstrated for a wider range of output voltages, in line with the simulation predictions in Ch. 4. In final applications, series or parallel connections of multiple modules can be considered for scaling the voltage or current ratings of the final implementation, thanks to the isolated output.

The forthcoming Ch. 7 delves into an in-depth exploration of the on-line efficiency tracking algorithm employed to identify the optimal switching frequency for the TBB stage. The primary objective of this algorithm is to seek the maximum efficiency across all operating conditions.

Chapter 7

On-line Efficiency Optimization of TBB Converter

Chapter in Brief

This chapter introduces an extremum seeking control (ESC) technique for determining the optimal modulation parameters, function of the operating points, of the TBB converter analyzed in Ch. 6. The TBB converter features several modulation parameters, such as the switching frequencies of the CLLC stage and of the TBB post-regulator, which impacts the overall conversion efficiency. The benefit of off-line optimization techniques is limited due to the difficulties in modeling accurately the converter behavior and the dependence on the actual operating point. Then, a model-free on-line search method based on the ESC technique is investigated and applied herein to find the optimal switching frequency of the TBB converter stage. For future implementations, the modulation of the switching frequency of the CLLC stage can also be incorporated, utilizing a two-dimensional ESC technique. The originality of the proposed approach lies in the utilization of small frequency perturbations that generate minimal effects on the objective variable, allowing for system optimization. Notably, the approach shown remarkable effectiveness in dealing with noisy measurements, which is important in this efficiency optimization application, where the related loss reduction bring to minimal variation of total input power. The approach is useful for on-line optimization or for an initial converter optimization applied before the final deployment of the converter. The effectiveness of the proposed search is then verified in the TBB prototype presented in Ch. 6.

7.1 Introduction

The pursuit of enhanced efficiency in power conversion systems remains a pivotal concern in various applications, including electric vehicles, renewable energy systems, and industrial processes. Achieving optimal efficiency is not merely about the initial design but also about dynamically adapting to changing operating conditions. Traditional off-line optimization techniques, while effective to a certain extent, often fall short due to the dependency on the actual operating points and operating conditions, and the inherent challenges in precisely modeling the converter dynamics. Consequently, a dynamic approach is useful to continuously optimize efficiency in on-line.

This chapter delves into the application of a method known as extremum seeking control (ESC) to address the efficiency optimization of the TBB converter, which is discussed in Ch. 6. The TBB converter exhibits some degrees of freedom in modulation parameters, including the switching frequencies of its CLLC stage and of the TBB post-regulator. These modulation parameters do not affect the voltage conversion gain, but they influence overall conversion efficiency. In particular, the TBB switching frequency could be carefully calibrated for minimizing both the switching losses of the switching devices and the inductor losses. The accuracy of the estimates provided by models is affected by the complex and actual behavior of semiconductor devices and magnetic elements, as well as the actual operating point. *To overcome this limitation, a model-free on-line search methodology based on the principles of ESC is explored and employed in this chapter to identify the optimal switching frequency of the TBB converter stage.* Furthermore, the potential integration of a two-dimensional ESC technique for modulating the switching frequency of the CLLC stage can be considered for future implementations.

Central to the effectiveness of this approach is the utilization of small frequency perturbations. These perturbations induce minimal disturbances on the objective variable, thereby enabling the optimization of the system without causing instability or excessive disruption. The chapter demonstrates the feasibility and effectiveness of this approach. It begins by showcasing the feasibility of the approach through simulations. Then, the efficacy of the approach is validated within the experimental prototype of the TBB converter introduced

in Ch. 6, showing its effectiveness in a practical context.

Part of the content of this chapter has been published in [124].

7.2 Extremum Seeking Control

7.2.1 Fundamentals

The ESC is a model-free adaptive control technique used in control systems characterized by non-linear plants or control objectives with local extrema. ESC techniques have historically employed various methods to locate extrema. These include stepping regulators, which perturb a control variable in discrete steps like perturb-and-observe algorithms; static-slope regulators, utilizing differentiation or test signals to determine perturbation direction; and peak-holding regulators, using the discrepancy between extremum and current state to guide seeking [125, 126]. ESC found applications in diverse fields such as maximum power point tracking (MPPT) in photovoltaic panels and wind energy conversion systems, or for the optimization of automotive powertrains [125, 127, 128]. In [128, 129] three-dimensional ESC technique was applied to triple-active-bridge (TAB) to optimize the converter efficiency. Remarkably, the ESC is capable to dynamically optimize the objective function on-line, without relying on explicit system models, that is, it is a "model free" approach.

7.2.2 Application to the TBB Converter

A classical ESC system diagram involves a non-linear, time-invariant system where the input variable represents the control variable and the output variable denotes the objective function.

In our case, the TBB is characterized by a maximum efficiency condition, varying the switching frequency, defined by a not known a priori minimum of power losses, as represented in Fig. 7.1, keeping fixed the input/output voltages and output power. The minimum loss condition is detected by measuring the input dc current $i_{DC_{in}}$ and assuming a controlled, constant output voltage V_o. A dynamic feedback law incorporating filters and per-

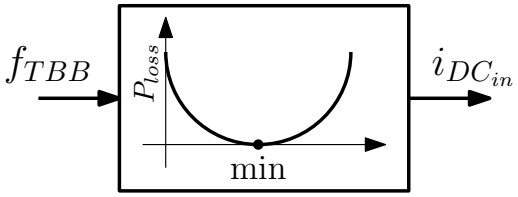


Figure 7.1: ESC system diagram considering the TBB converter. $i_{DC_{in}}$ is a convex objective function, it represents the losses of the system. f_{TBB} is an input of the system and is a control degree of freedom for the TBB.

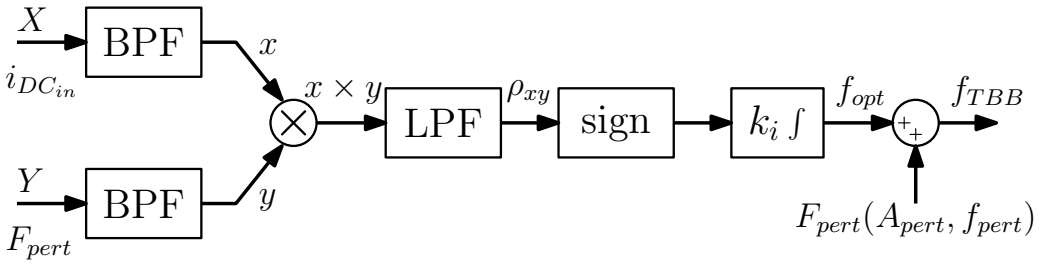


Figure 7.2: ESC description.

turbation signals estimates the minimum loss condition, as shown in Fig. 7.2. The feedback law in Fig. 7.2 is designed to ensure that the switching frequency converges to a neighborhood around the optimal. Notably, the convergence is influenced by the amplitude and reciprocal frequency of the perturbation signals.

Assuming a perturbation signal Y with amplitude A_{pert} and frequency f_{pert} applied on the switching frequency, the cost function x exhibits an ac amplitude $G(A_{pert})$, a fundamental frequency component at f_{pert} and a phase-shift φ introduced by the system's dynamics. The band-pass filters (BPFs) are designed with cut-off frequencies one-tenth and ten times the perturbation frequency, to isolate the desired frequency component f_{pert}. The product between the filtered cost function and the controlled variable results:

$$x \times y = \frac{1}{2} G(A_{pert}) A_{pert} [\cos(\varphi) - \cos(2\omega_{pert} t + \varphi)] \tag{7.1}$$

By applying a low-pass filter (LPF) with a cut-off frequency lower than f_{pert}, the desired current amplitude can be extracted. In particular, if $\rho_{xy}(A_{pert}) > 0$, the controlled variable Y should be reduced to reduce the cost function X. Conversely, if $\rho_{xy}(A_{pert}) < 0$, the controlled variable Y should be increased to reduce the cost function X. If $\rho_{xy}(A_{pert}) = 0$, it means that the system is operating at an extrema, therefore, no actions are required. The

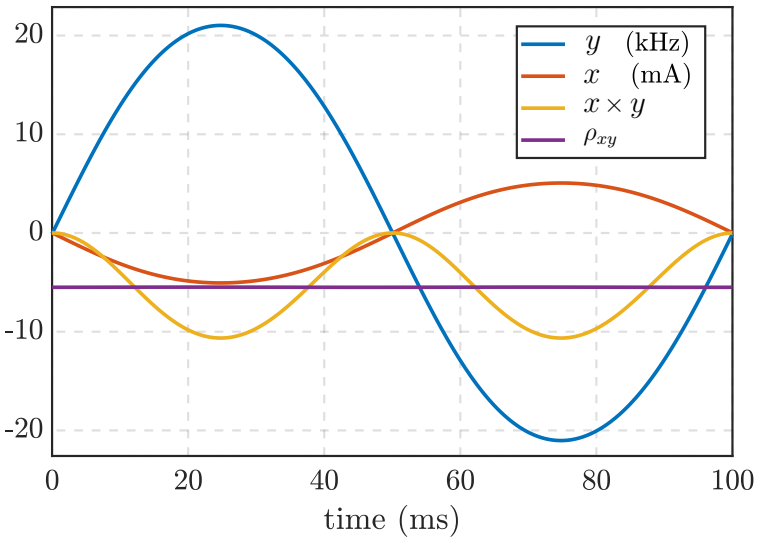


Figure 7.3: PLECS® simulation of ESC in Fig. 7.2 at TBB switching frequency $f_{TBB} = 100\,\text{kHz}$. Amplitude of the frequency perturbation $A_{pert} = 20\,\text{kHz}$ with frequency $f_{pert} = 10\,\text{Hz}$. Output power $P_o = 6\,\text{kW}$, and output voltage $V_o = 400\,\text{V}$.

sign of ρ_{xy} is then employed in Fig. 7.2 with an appropriate integral gain and then used to adjust the value of the perturbation, resulting in lower dc current, and then, losses. Stable operation is guarantee if f_{pert} dynamics are much slower than the plant's dynamics.

7.3 Simulation Results

Fig. 7.3 shows one simulation period of the ESC applied to the TBB converter at TBB switching frequency $f_{TBB} = 100\,\text{kHz}$. The implemented simulation in PLECS®+Simulink®

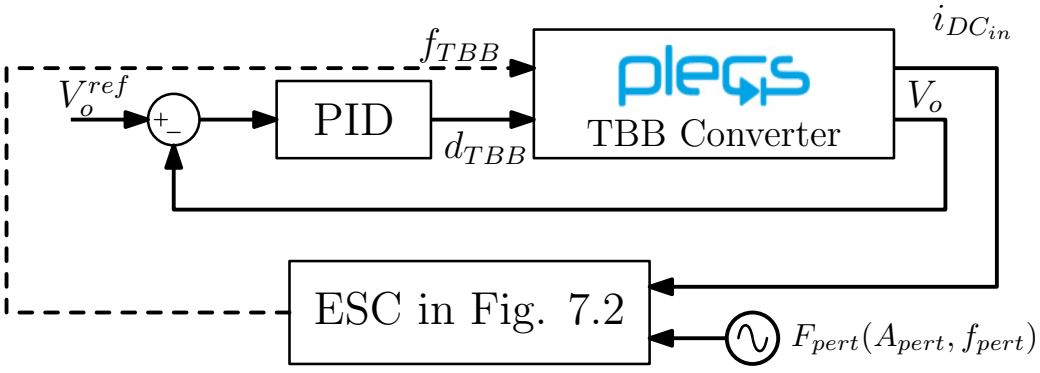


Figure 7.4: ESC implementation in PLECS®/Simulink®.

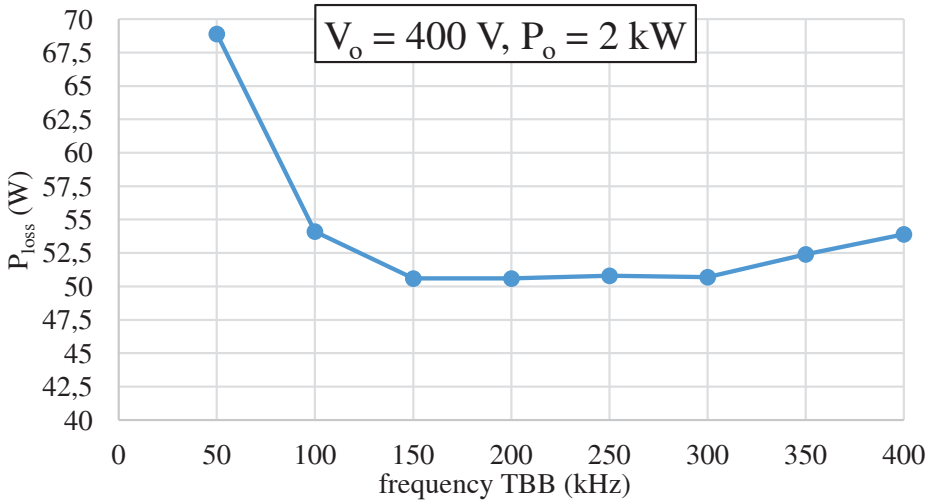
environment is depicted in Fig. 7.4, where a proportional-integral-derivative (PID) controller regulates the output voltage to $V_o = 400\,\mathrm{V}$. The amplitude of the frequency perturbation is $A_{pert} = 20\,\mathrm{kHz}$ with frequency $f_{pert} = 10\,\mathrm{Hz}$ and output power $P_o = 6\,\mathrm{kW}$. The simulated input dc current presents an amplitude of $5\,\mathrm{mA}$ and is counter-phase to the perturbation signal. It means that, in this operating condition, the absorbed input current reduces as the switching frequency of the TBB increases. At the considered conditions, the power loss variation corresponding to the injected switching frequency perturbation is about $4\,\mathrm{W}$.

Fig. 7.5 illustrates the total losses of the TBB converter as a function of the switching frequency, simulated within the PLECS®/Simulink® environment. The simulation setup corresponds to the schematic depicted in Fig. 7.4. It's important to note that these simulations didn't account for transformer and inductor losses, which explains the less distinct presence of a singular minimum in Fig. 7.5. Furthermore, it's important to highlight that such an off-line method exhibits limited precision in estimating the peak efficiency due to the modeling inaccuracies. As a result, the adoption of an on-line method becomes necessary. The ESC algorithm can succeed in converging to the optimal operating point thanks to its intrinsic noise rejection and averaging properties. Overall, the application of ESC to the TBB can be a powerful approach for optimizing the efficiency of the converter.

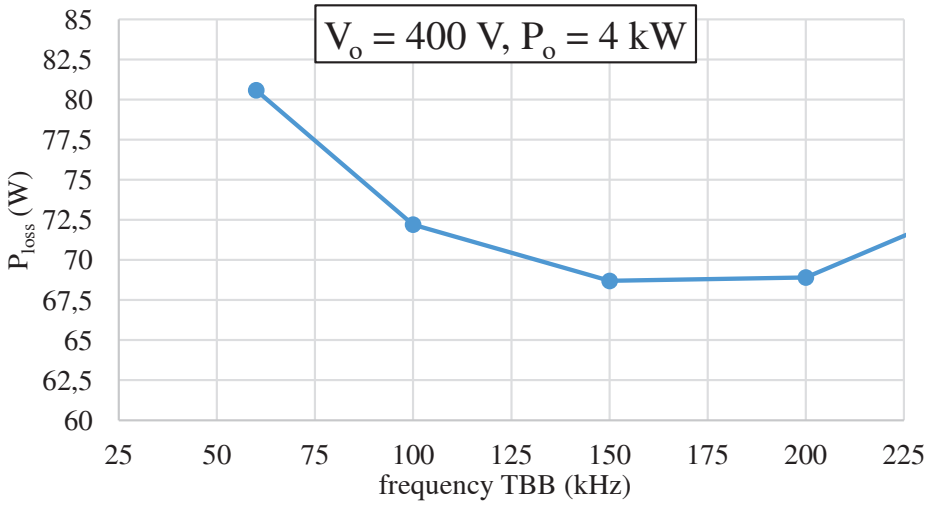
7.4 Experimental Results

Fig. 7.6 shows the measurement of total loss at $V_o = 400\,\mathrm{V}$ and output power $P_o = 2\,\mathrm{kW}, 4\,\mathrm{kW}$ and $6\,\mathrm{kW}$ for different switching frequencies of the TBB stage. Measurements are performed on the experimental prototype of TBB in Fig. 6.9 with parameters in Table 6.1. Efficiency measurements are performed by means of a Keysight PA2203A power analyzer. The objective function exhibits an absolute minimum, which can be detected through the gradient-based approach in Fig. 7.2.

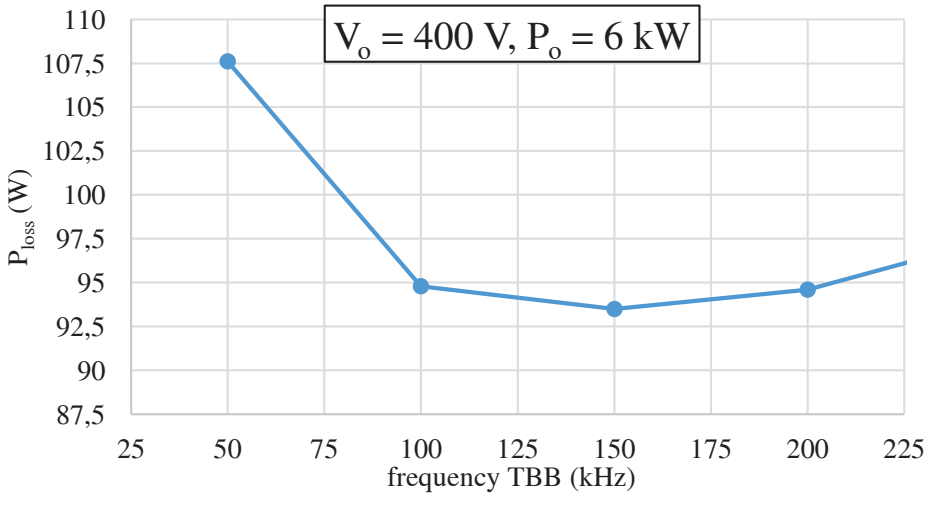
Experimental Validation. Fig. 7.7 shows the schematic diagram of the ESC implementation within the real-time controller of the TBB converter. Further details are reported in



(a)



(b)



(c)

Figure 7.5: Total loss simulations at constant output voltage $V_o = 400\,\mathrm{V}$ and power (a) $P_o = 2\,\mathrm{kW}$; (b) $P_o = 4\,\mathrm{kW}$; and (c) $P_o = 6\,\mathrm{kW}$, at different switching frequencies of the TBB stage.

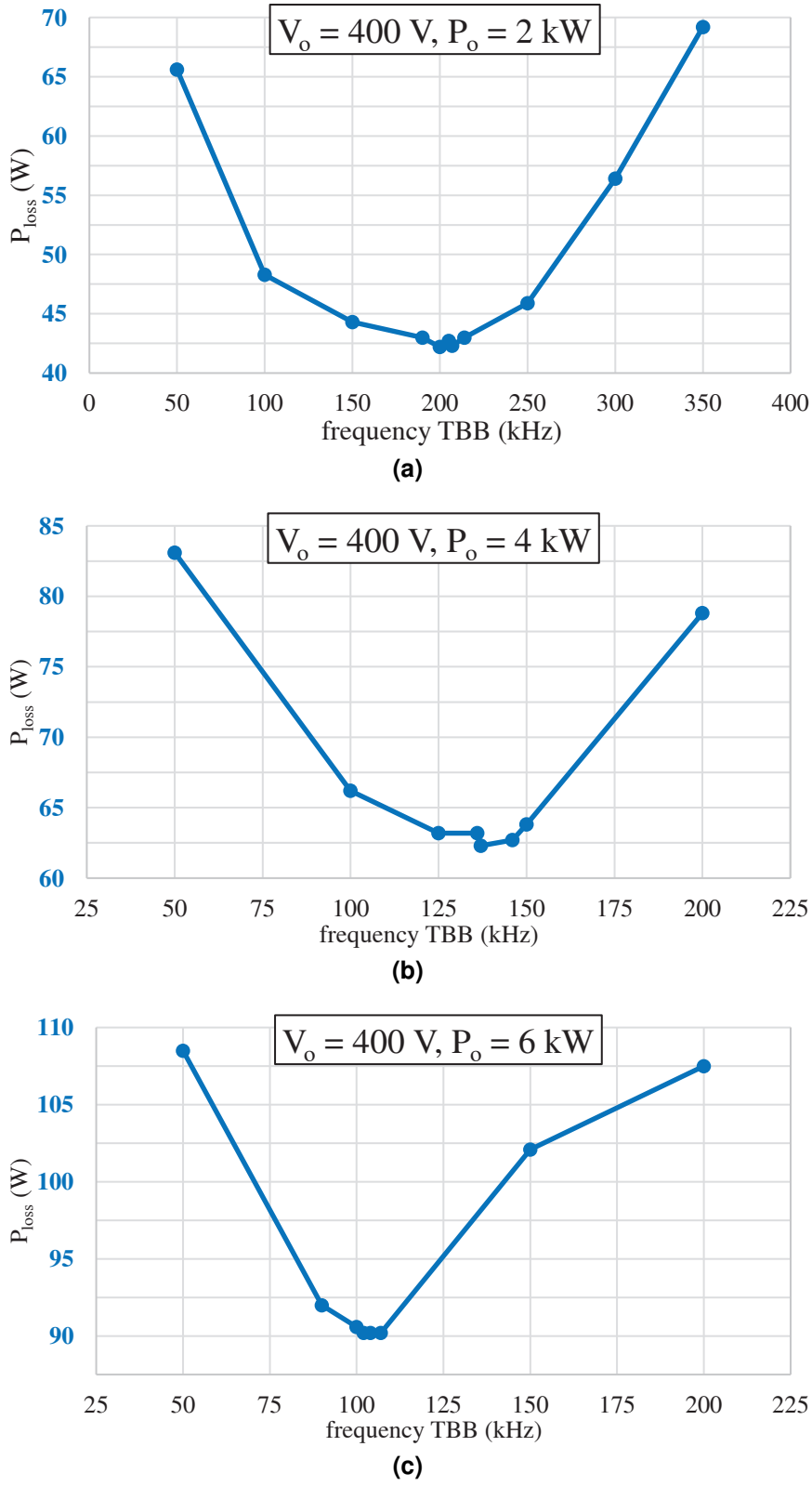


Figure 7.6: Total loss measurement at constant output voltage $V_o = 400\,\mathrm{V}$ and power (a) $P_o = 2\,\mathrm{kW}$; (b) $P_o = 4\,\mathrm{kW}$; and (c) $P_o = 6\,\mathrm{kW}$, at different switching frequencies of the TBB stage. Minimum losses at (a) $f_{s_o} = 207\,\mathrm{kHz}$; (b) $f_{s_o} = 137\,\mathrm{kHz}$; and (c) $f_{s_o} = 104\,\mathrm{kHz}$.

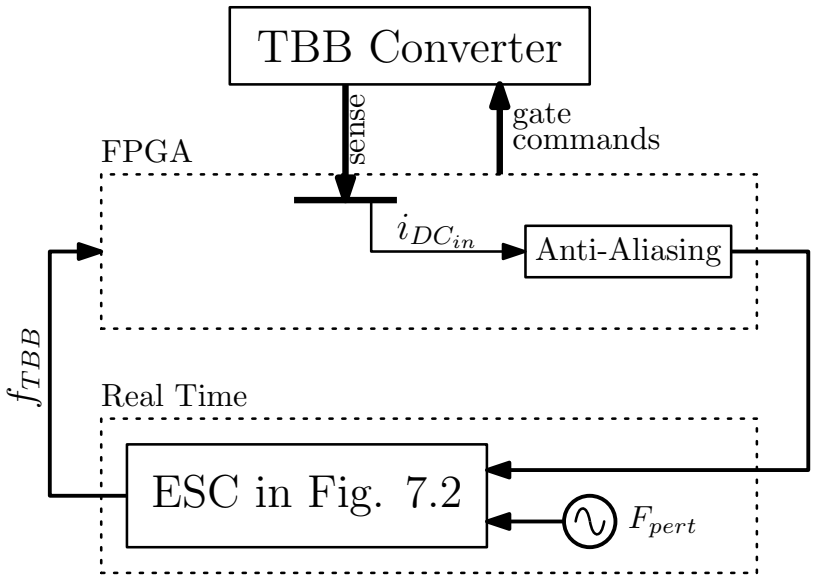


Figure 7.7: ESC implementation in the considered TBB converter. Hardware details can be found in App. D.

App. D.

Fig. 7.8 displays the optimum switching frequencies obtained at different output powers by applying the ESC in the output voltage full range. The actual TBB switching frequencies cover the range 30 - $300\,\mathrm{kHz}$. The achieved optimal efficiencies of the TBB converter in Fig. 6.7 with parameters in Table 6.1 are presented in Fig. 6.12. Discrepancies in power losses relative to the actual minimum losses are reported in Fig. 7.9. The relative error in losses is limited to a maximum of 4.5%.

Transient Response. Fig. 7.10b shows the response of the ESC algorithm to a load variation with $V_o = 400\,\mathrm{V}$ and output power transitioning from 2 to $6\,\mathrm{kW}$. Steady-state frequencies found by the ESC algorithm are $f_{s_o} = 207\,\mathrm{kHz}$ in Fig. 7.6a at $P_o = 2\,\mathrm{kW}$, and $f_{s_o} = 104\,\mathrm{kHz}$ in Fig. 7.6b at $P_o = 4\,\mathrm{kW}$, with efficiencies 97.96% and 98.44%, respectively, accordingly to Fig. 6.12. Fig. 7.10a and Fig. 7.10c shows the transient responses to a load step variation $1.5 \rightarrow 3\,\mathrm{kW}$ at $V_o = 280\,\mathrm{V}$ and $2 \rightarrow 4\,\mathrm{kW}$ at $V_o = 480\,\mathrm{V}$.

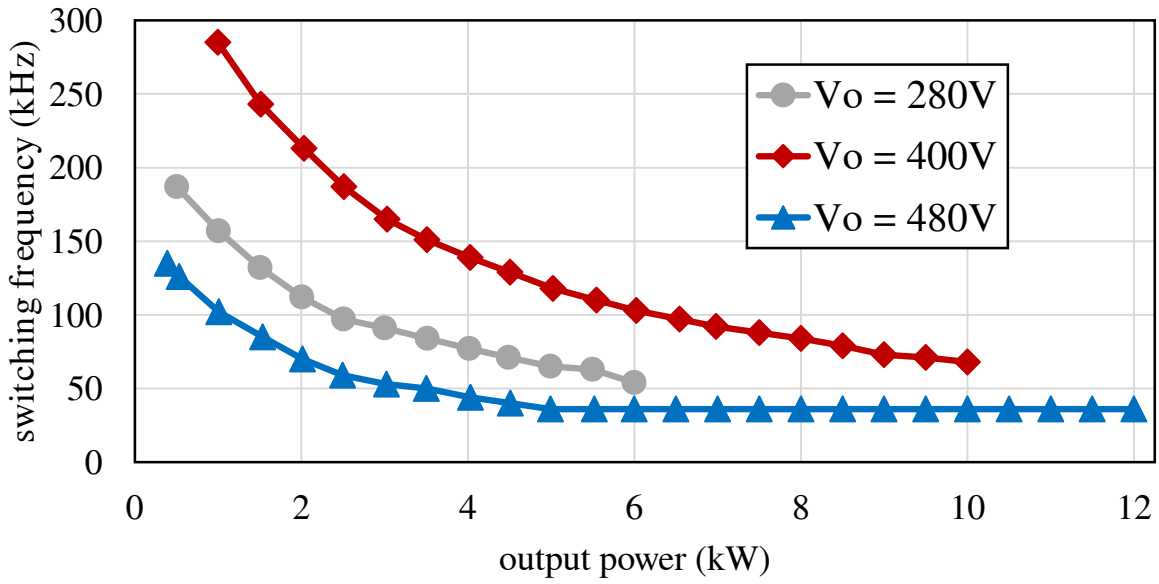


Figure 7.8: Switching frequencies found by closed-loop ESC in Fig. 7.7, at values at different output voltage values V_o and power P_o.

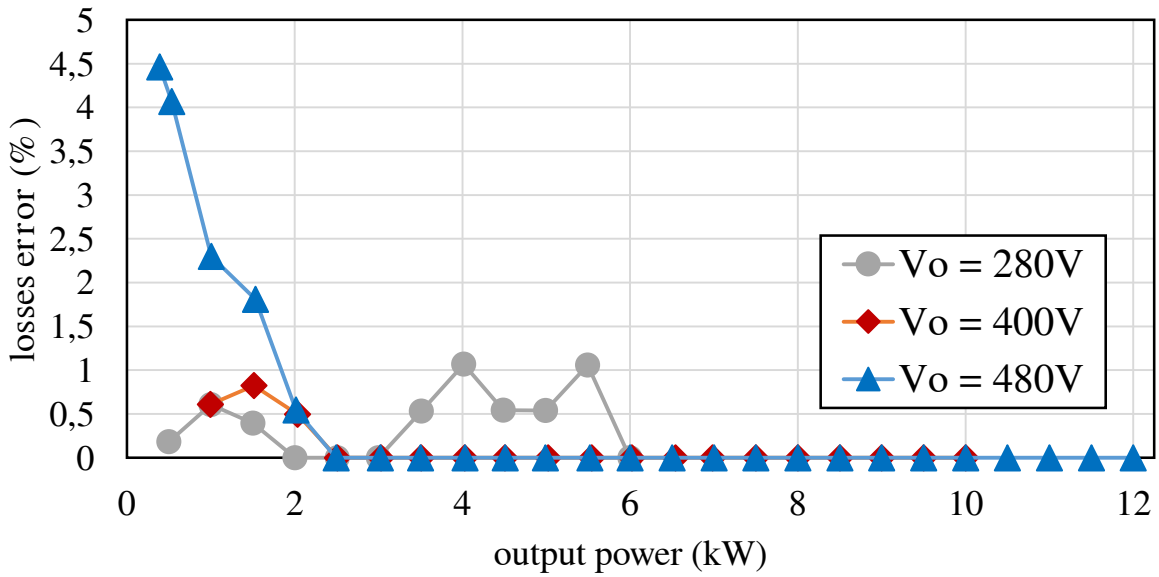


Figure 7.9: Distribution of errors in the converter losses obtained with the proposed optimization method, at different output voltage values V_o and power P_o. The actual maximum efficiency points are determined through a manual exploration of the switching frequency.

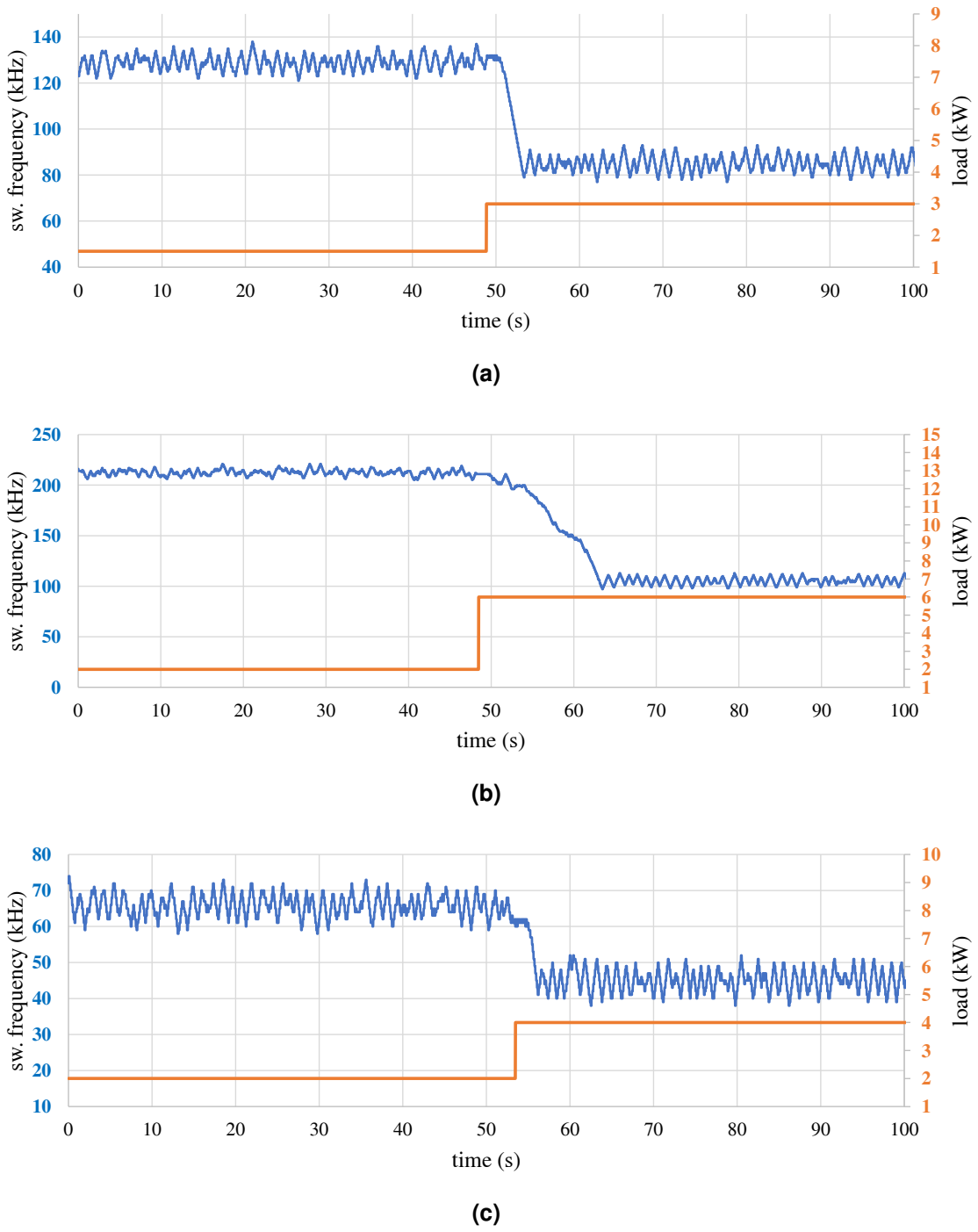


Figure 7.10: Transient response of the implemented ESC to a load step variation. (a) $V_o = 280\,\mathrm{V}$, $P_o = 1.5 \rightarrow 3\,\mathrm{kW}$; (b) $V_o = 400\,\mathrm{V}$, $P_o = 2 \rightarrow 6\,\mathrm{kW}$; and (c) $V_o = 480\,\mathrm{V}$, $P_o = 2 \rightarrow 4\,\mathrm{kW}$.

7.5 Summary

This chapter introduced an ESC technique for determining the optimal operating points of the TBB converter analyzed in Ch. 6. The TBB presents several modulation parameters that have a notable impact on the overall conversion efficiency. Off-line optimization methods have limitations due to their strong dependence on the models of semiconductor devices and magnetic elements, as well as the operating points and temperatures involved. In response, this study introduces a model-free on-line search approach based on the ESC technique. This method is employed to identify the optimal switching frequency for the TBB converter stage. A unique aspect of this work is the utilization of small frequency perturbations that induce minimal effects on the objective variable while enabling efficient system optimization.

Simulation and efficiency experimental results obtained with the presented approach are reported. The results are collected considering the $10\,\mathrm{kW}$ TBB prototype module presented in Ch. 6. Conversion performances reported with the adopted on-line method and covering the whole power and voltage ranges are reported experimentally, showing high efficiency over a wide range of operating conditions. Additionally, future implementations could extend this concept to modulate the switching frequency of the CLLC stage using a two-dimensional ESC technique.

Remarkably, the algorithm succeeds in converging to the optimal operating point thanks to its intrinsic noise rejection and averaging properties. Overall, the application of ESC to the TBB demonstrates a valuable approach for optimizing the efficiency of the converter. This approach can be applied to the converter as a pre-calibration step, before the final deployment on the actual application. This study contributes to the advancement of converter optimization methods by offering a practical and effective strategy for on-line performance enhancement.

Chapter 8

Conclusions

This dissertation explored the significant challenges and opportunities in the domain of high-power dc-dc converters for EV XFC systems. These converters represent a critical component in the context of widespread EV adoption, specifically addressing a paramount concern for prospective EV owners: charging time. This concluding chapter provides a summary of the key findings and contributions of this work.

Converter modeling and analysis: a comprehensive review of existing dc-dc converter topologies suitable for EV XFC systems is conducted. The primary aim is to transcend the limitations of resonant converters and explore multi-stage configurations capable of achieving high efficiency across a wide range of output voltages. Moreover, novel two-stage converter topologies are introduced as potential solutions. To facilitate a comprehensive understanding and guide potential improvements, loss models of the converter components are provided. Loss models enables in-depth simulations to estimate losses and identify topological variations with possible efficiency improvements. A simulation-based comparison of multi-stage dc-dc converter topologies is performed to identify the most promising converter solution for efficient EV charging. Two noteworthy solutions emerged, namely, the BB-LLC and the TBB, both displaying promising performances for a wide range of output voltages. Subsequently, these promising topologies are subjected to experimental investigations to validate their performances.

Converter design and prototyping: a comprehensive design procedure is outlined for the two selected topologies. Detailed practical design aspects of the experimental dc-dc converter module are presented. These topologies are subjected to experimental investigations to validate their performance. Furthermore, a calorimetric method is introduced and employed to evaluate power losses and validate loss distribution across the converter's components. The TBB converter, in particular, demonstrates superior efficiency performances, in line with the simulation predictions. Notably, the reported analysis and the experimental characterizations and tests are performed considering a converter module prototype rated $10\,\mathrm{kW}$, input voltage $800\,\mathrm{V}$, and output range $250\,\mathrm{V}$ to $500\,\mathrm{V}$, employing SiC and GaN semiconductors. Conversion performances of the TBB covering the whole power and voltage ranges are reported experimentally, showing high efficiency over a wide range of operating conditions. The recorded peak efficiency is 98.63% at $500\,\mathrm{V}$ output voltage and $7\,\mathrm{kW}$ transferred power.

Converter on-line optimization: a model-free on-line search method using ESC technique, free from complex modeling requirements, is proposed to explore and maximize the efficiency performances of the TBB, a especially promising converter solution suitable for EV charging applications. This approach contributes to the advancement of converter optimization methods by offering a practical and effective strategy for on-line performance enhancement.

In conclusion, the TBB converter topology identified and explored in this dissertation can serve as a pivotal solution for achieving efficient and rapid EV charging. By addressing the efficiency challenges associated with EV extreme fast charging, this research contributes to the broader goal of widespread EV adoption, ultimately leading to a more sustainable and environmentally friendly transportation ecosystem.

Appendix A

LTspice® Simulation for Switching Losses Estimation

In the following, the LTspice® simulation for the switching losses estimation is explored, and the obtained results are discussed. A single switching action of a switching leg, as shown in Fig. 3.1, can be used for the switching energy loss evaluation. LTspice® schematic is shown in Fig. A.1. The equivalent inductance seen from the switching node is treated as a constant current generator I_1, with a value equal to the switched current of the converter at the instant in which the switching losses are estimated. Switching losses are function of the switched current and dc bus voltage, I_1 and V_{in} in Fig. A.1, respectively. Gate driving circuits components and values emulate a real application of driving circuit for the considered Wolfspeed C3M0032120K. Switching devices SPICE model is provided by the manufacturer. Estimates of the parasitic inductances of the connection paths are included. Fig. A.2 presents the simulation results during a switching leg action, specifically the turn-off transient of the lower switch U_2 followed by the turn-on transient of the upper switch U_1. A dead-time of $160\,\mathrm{ns}$ is applied, and the switched current is set to $I_1 = -2\,\mathrm{A}$. The figure displays, in sequence, the drain-source voltage of the devices, the instantaneous dissipated power, and the gate-source voltages. As observed, the considered switching current I_1 determine a zero-voltage turn-on transition for the upper switch U_1. The switching losses are calculated by integrating of the dissipated power associated to the switching transition shown in Fig. A.2. Doing so, switching energy losses in Fig. 3.2 are found. Notably,

this approach accounts also for the energy losses associated with body diode conduction, which is beneficial for the approach adopted within PLECS® simulation environment for the topology comparisons.

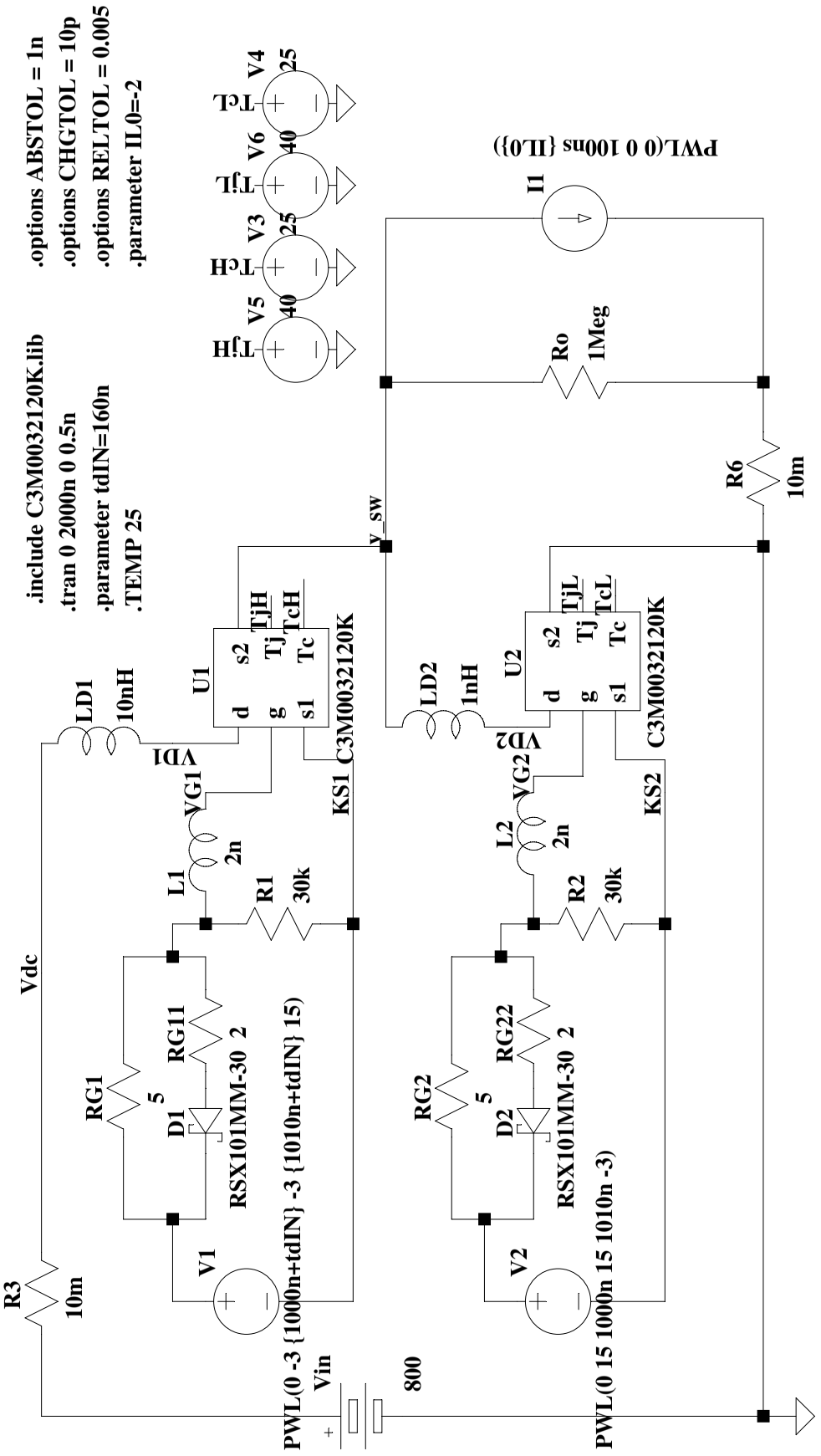


Figure A.1: LTspice® simulation for switching losses estimation.

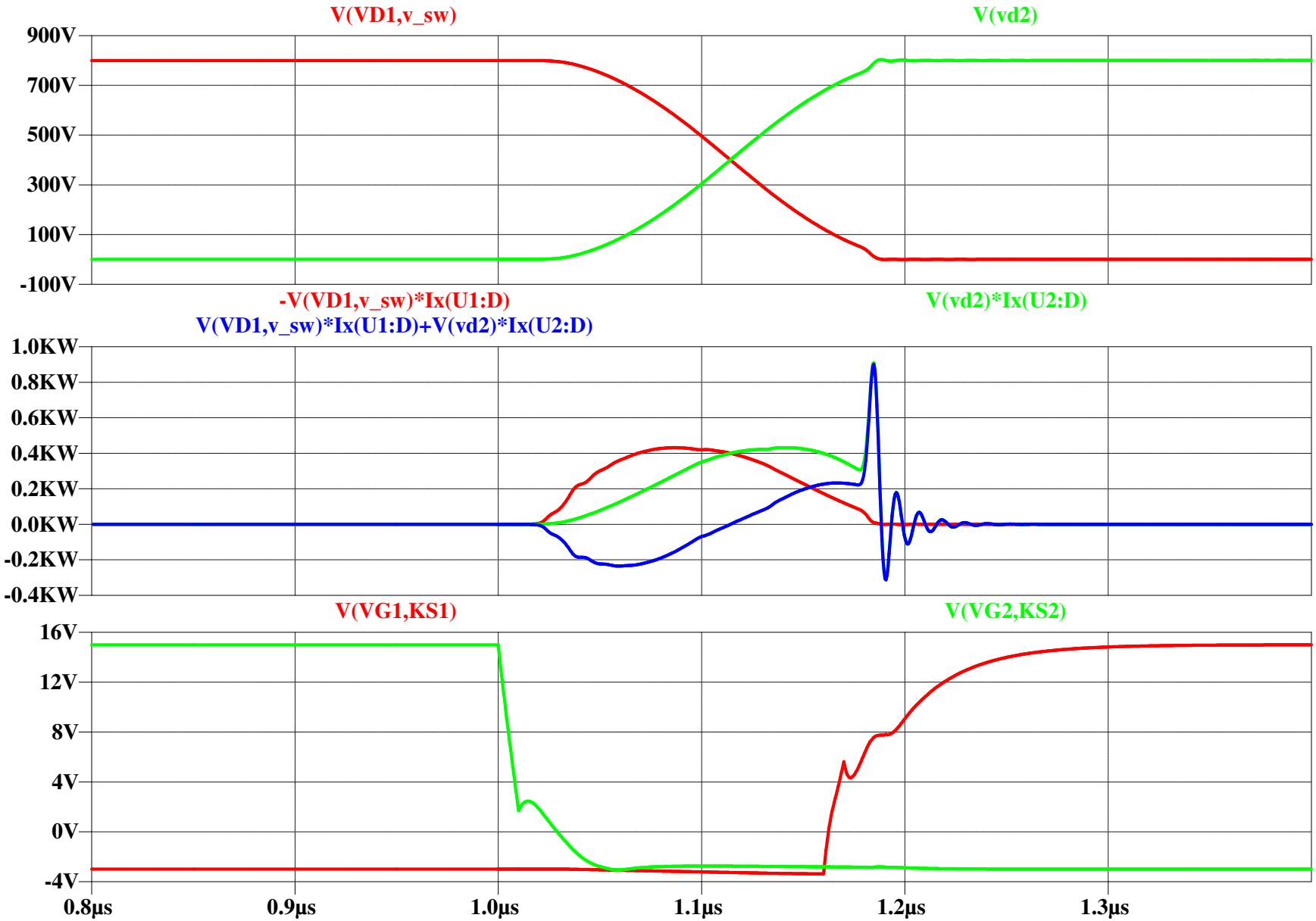


Figure A.2: Simulation results for switching losses estimation.

Appendix B

Steinmetz Parameters Extraction

The Steinmetz parameters K_c, α and β are extracted from the datasheet of the selected core material N97 [107], which is used for the construction of transformers and inductors in this dissertation. Fig. B.1 depicts the power losses per unit volume of the N97 material as a function of magnetic induction B and frequency f at a temperature of $100°$C. From this graph, the loss values are extracted, and the Steinmetz parameters derived. The obtained values are: $K_c = 1.18$, $\alpha = 1.96$, and $\beta = 2.346$.

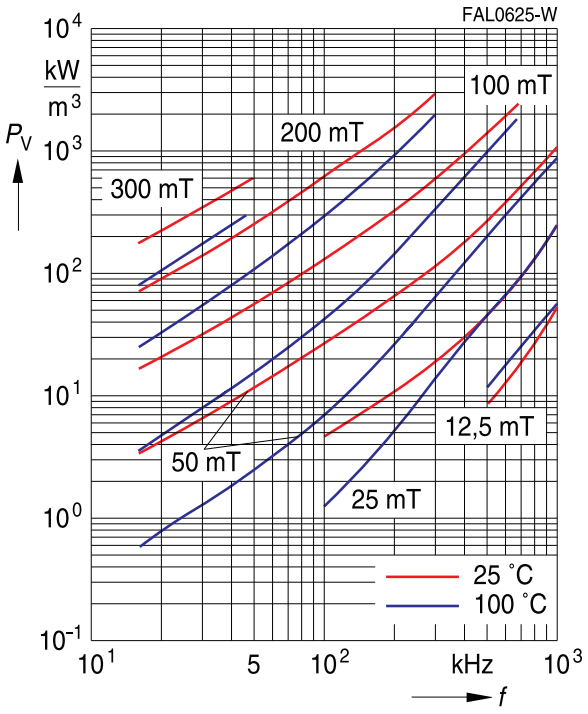


Figure B.1: Power losses per unit volume of the core material N97 from datasheet [107].

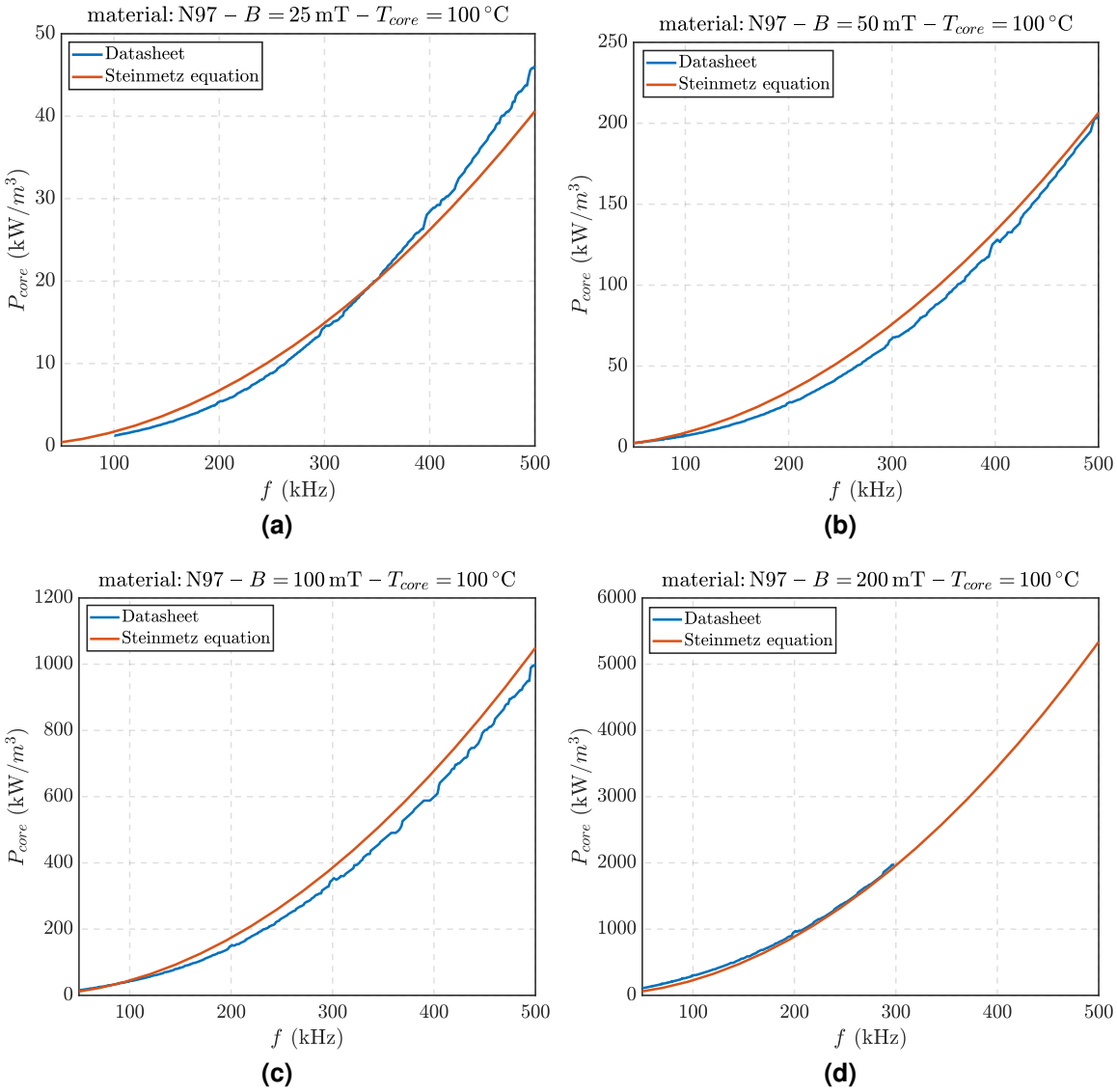


Figure B.2: Power losses per unit volume of the core material N97: comparison between datasheet data [107] and results from Steinmetz parameters $K_c = 1.18$, $\alpha = 1.96$ and $\beta = 2.346$. Frequency range: 50-400 kHz; (a) $B = 25\,\mathrm{mT}$; (b) $B = 50\,\mathrm{mT}$; (c) $B = 100\,\mathrm{mT}$; and (d) $B = 200\,\mathrm{mT}$.

Subsequently, in Fig. B.2, a comparison is presented between the losses of the N97 material obtained from the datasheet [107] and the results obtained using the Steinmetz equation (3.3). The comparison demonstrates an excellent fit between the two curves, within the ranges of B between 25 and 200 mT and frequency f between 50 and 500 kHz. These derived parameters are then utilized to model the core losses in the topologies comparison of Ch. 4.

Appendix C

Simulation Example of LLC Converter

As an example, the implementation of the LLC simulation setup in the PLECS®/Simulink®+ MATLAB® environment is provided herein. This example serves to demonstrate how the circuit models are constructed and how the simulations are executed.

Fig. C.1 present the PLECS® simulation circuit of the LLC in Fig. 4.1 with parameters detailed in Table 4.2. Fig. C.2 shows the output capacitors bank within such a circuit. Components currents, voltages, and powers are extracted and sent to Simulink® environment as shown in Fig. C.3. Within Simulink® these signals are treated for the waveforms visualization, and the relevant signals, following the models outlined in Sect. 3.3, are transmitted to the MATLAB® workspace. This data transfer occurs after the simulation reaches a steady state, enabling the estimation of the losses.

The MATLAB® code is therefore reported in Sect. C.1. From this MATLAB® code, multiple simulations can be launched in parallel to explore different operating conditions of the converter, thereby reducing simulation times. Each parallel simulation runs on an individual CPU core and it is initialized from its dedicated MATLAB® instance, called from the main code in Sect. C.1. If eight are the CPU cores, a maximum of eight MATLAB® instances can be executed in parallel, each called from the main. Sect. C.2 provides details on one such MATLAB® instance executed on a core, which initiates its Simulink® simulation (Fig. C.3) at a specific operating point of the converter. It manages the simulation results and it transmits them to the main MATLAB® instance in Sect. C.1. This approach facilitates the implementation of parallel simulations using the PLECS® circuit simula-

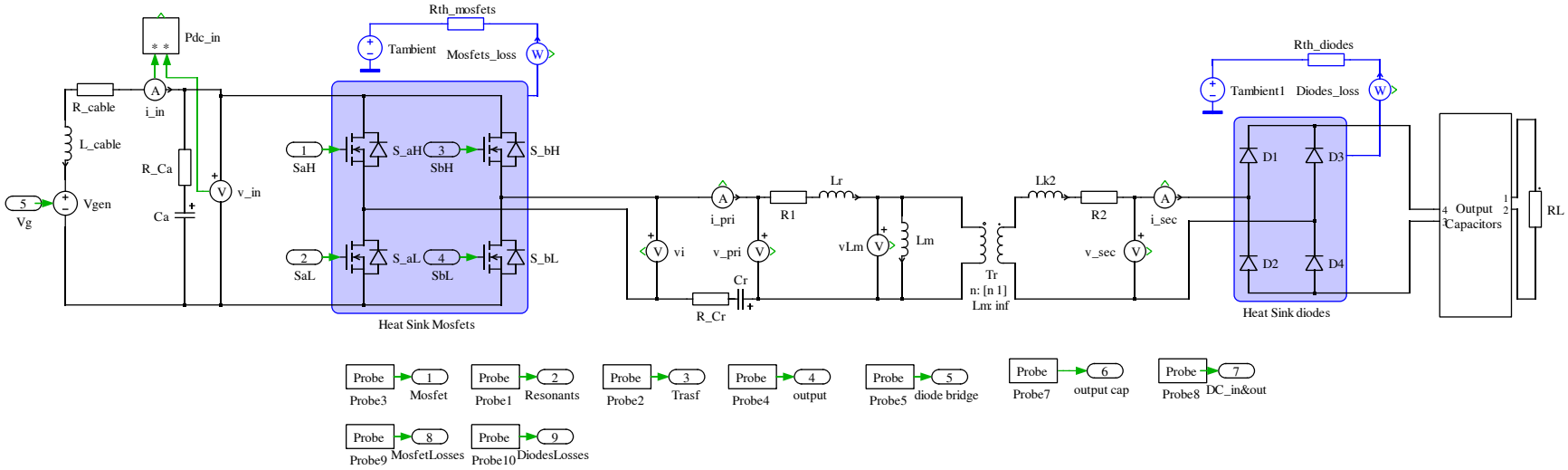


Figure C.1: PLECS® simulation circuit of the LLC in Fig. 4.1 with parameters in Table 4.2.

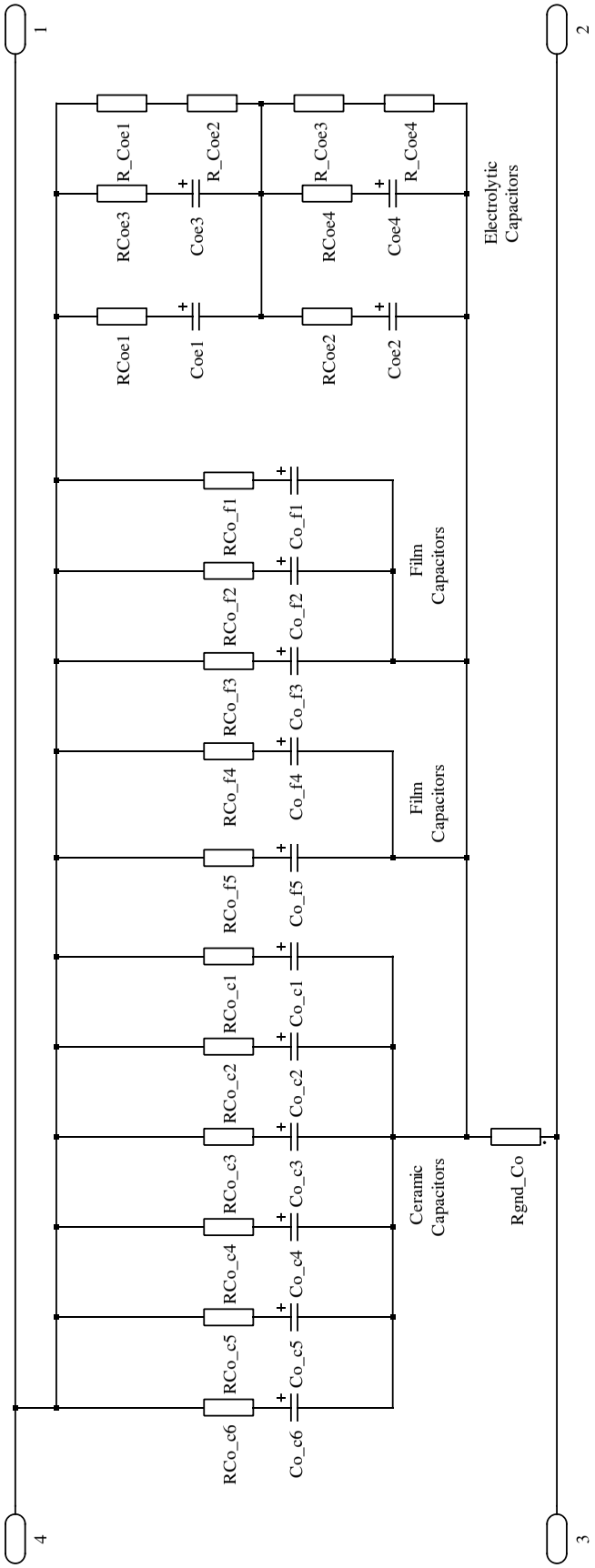


Figure C.2: Output capacitors of the PLECS® simulation circuit in Fig. C.1.

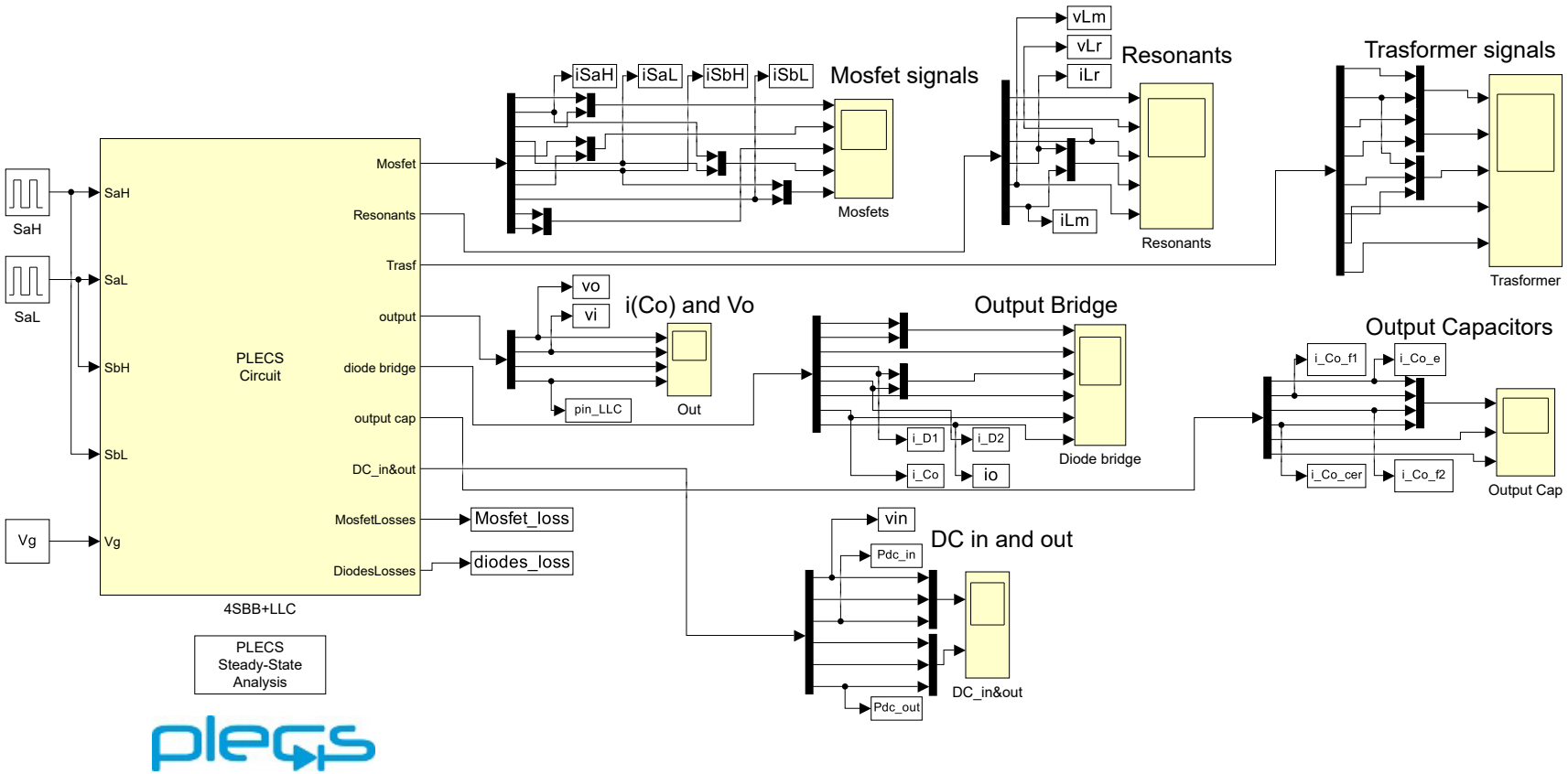


Figure C.3: Simulink® code, which includes the PLECS® schematic in Fig. C.1.

tor, as such simulations are not supported by the parallel simulation toolbox provided by MATLAB®.

C.1 MATLAB® main code

Herein is reported the MATLAB® main code of the LLC simulation for the losses investigation.

```
%--------------ZANATTA NICOLA - nicola.zanatta.2@phd.unipd.it--------------%
%% -----Initialization file for the Plecs simulation of the 10 kW LLC-----%
%% ------------------------------10kW LLC-------------------------------%
%-------------------------------------------------------------------------%
% close all;
clear all;clc;
tic

%% LLC parameters-----------------------------------------------------
Vg_n = 800;              %nominal input voltage
Vg = Vg_n;               %input voltage

f0 = 200e3;              %resonance frequency
Po_n = 10e3;              %nominal output power
Tamb = 45;               %ambient temperature

Vo_n = 400;              %nominal output voltage
Vo_min = 250;            %minimum output voltage
Vo_max = 500;            %maximum output voltage

%-------------------------------------------------------------------------
Vo_vet = [Vo_max];       %output voltage LLC -- CHANGE ME
Io_vet = [1e3 2e3 3e3 4e3 5e3 6e3 7e3 8e3 9e3 10e3]./500;            %output current --
    CHANGE ME
%-------------------------------------------------------------------------
% %-----------------------------------------------------------------------
% Vo_vet = [Vo_n];       %output voltage LLC -- CHANGE ME
% Io_vet = [1e3 2e3 3e3 4e3 5e3 6e3 7e3 8e3 9e3 10e3]./400;            %output current --
    CHANGE ME
% %-----------------------------------------------------------------------
% %-----------------------------------------------------------------------
% Vo_vet = [Vo_min];       %output voltage LLC -- CHANGE ME
% Io_vet = [4e3 5e3 6e3 7e3 8e3]./250;            %output current -- CHANGE ME
% %-----------------------------------------------------------------------

% %-----------------
% Vo_vet = Vo_n;
% Io_vet = [2e3]./Vo_vet;
% %---------------

Mi_th_vet = Vo_vet/Vg;          %voltage gain LLC

% BB input capacitor-------------------------------------
Ca = 20e-6;              %BB input capacitor
R_Ca = 9.3e-3/2;             %Ca ESR

```

```
%LLC output cap-------------------------------------
Co_e = 7.5e-6;              %LLC output capacitor (100u dc) 7.5u @400kHz
R_Co_e = 330e-3;            %Co ESR 400kHz
R_Coe_par = 178e3;          %resistive divider electrolytic cap.s
Co_film_1 = 2e-6;         %3* film capacitor 400kHz
R_Co_film_1 = 35e-3;       %3* ESR Co film 400kHz
Co_film_2 = 5e-6;         %2* film capacitor 400kHz
R_Co_film_2 = 15e-3;       %2* ESR Co film 400kHz
Co_cer = 100e-9;            %5* Co ceramic
R_Co_cer = 50e-3;           %5* ESR Co ceramic 400kHz

% Sa and Sb leg ------------------------------------------
Ron_b = 29.87e-3;           %on resistance leg b
Ron_a = Ron_b;
alpha_Ron = 1.51e-3;       %temperature coefficient
deltaT_Ron = Tamb - 25;
d_Sb = 0.5;               %duty cycle of LLC leg. Fixed value
td_Sb = 200e-9*0;         %dead time leg b

% LLC resonants--------------------------------------
Lr = 32e-6;             %resonant inductance
Nsi = 2;                  %number of series inductors;
Cr = 1/(Lr*(2*pi*f0)^2);             %resonant capacitor
R_Cr = 7e-3;              %Cr ESR

% resonant inductor----------------------------------------
R_Lr = 2*28e-3 + 71e-3;                  %ac resistance at fondamental frequency
load('Rac_Magnetics');

mu_0 = 1.256637e-6;      %magnetic field constant
mu_eff_gap = 27.7071;    %relative magnetic field constant - N=15 PQ4040
N_Lr = 15;                %number of turns - inductor2 N=15 PQ4040
lcore_Lr = 93e-3;       %magnetic length - inductor2 N=15 PQ4040
Vcore_Lr = 17580e-9;     %magnetic volume PQ4040
Kc_Lr = 0.0015;           %Steinmetz- N=15 PQ4040
alpha_Lr = 1.9618;        %Steinmetz- N=15 PQ4040
beta_Lr = 2.3462;         %Steinmetz- N=15 PQ4040
mult_losses_Lr = 1.5;    %multiplicative factor core losses transformer

% transformer----------------------------------------
R1 = R_Lr/2;                %winding resistance
R2 = R_Lr/2;                %winding resistance
alpha_copper = 4e-3;       %temperature coefficient of copper
deltaTcopper = 65;        %mean temperature increment
Lm = 150e-6;              %magnetizing inductance
N1 = 24;                  %number of turns N1
N2 = 12;
n = N1/N2;                    %transformer turn ratio
Acore_tr = 577.64e-6;          %core cross-sectional area - trasformer1 PQ65/60
Vcore_tr = 71437e-9;        %magnetic volume - trasformer1 PQ65/60
alpha_tr = 1.862;        %Steinmetz - trasformer1 N=17 PQ65/60
beta_tr = 2.5719;         %Steinmetz - trasformer1 N=17 PQ65/60
Kc_tr = 0.0098;           %Steinmetz - trasformer1 N=17 PQ65/60
mult_losses_tr = 2;       %multiplicative factor core losses transformer

% diodes-----------------------------------------------
%C5D50065D - values at Tj=Tamb
Vf = 0.9947-Tamb*0.0013;                  %diode forward voltage
Ron_d = 9.3e-3+Tamb*7e-5;              %diode on resistance

% load-----------------------------------------------
```

```
106 RL_vet = Vo_vet./Io_vet;          %nominal load
107 Req_vet = 8*n^2*(RL_vet+R2+2*Ron_d)/pi^2;     %equivalent load
108
109 %initial conditions----------------------------------
110
111 f = [140e3:1e3:400e3];
112 idxf0 = find(f==f0);
113 Rs = R1 + R_Cr + 2*Ron_a;
114
115 vCo_ic_vet = Vo_vet;
116 iLm_ic = 0;                          %initial condition on magnetizing current
117 iLk2_ic = 0;                         %ic on scecondary side current
118 iLr_ic = 0;                          %ic on primary side current
119 vCr_ic = 0;                          %ic on resonant capacitor voltage
120
121 %-----------------------------------------------------------------------
122 %% Plecs simulation-----------------------------------------------------
123 %parameters initialization - parametric simulation
124
125 if length(Vo_vet) > 1
126     iterations = length(Vo_vet);
127     variableToBeIterated = 1;   %1 assigned to Vo
128     if length(Io_vet) < length(Vo_vet)
129         Io = Io_vet(1);
130         if length(Io_vet) ~= 1
131             warning('Number of Io elements doesn''t match Vo elements!!')
132         end
133     end
134 elseif length(Io_vet) > 1
135     iterations = length(Io_vet);
136     variableToBeIterated = 2;   %2 assigned to Io
137     Vo_th = Vo_vet(1);
138     vCo_ic = vCo_ic_vet(1);
139     Mi_th_vet = Mi_th_vet*ones(1,length(Io_vet));
140 else
141     iterations = 1;
142 end
143
144 param = ws2struct();
145
146 % %variables inizialization-------------------------------------------
147 out.empty = zeros(iterations,1);
148 %-----------------------------------------------------------------------
149
150 %simulation settings-------------------------------------------------
151 N = 20;                              %period cycles Steady-State analysis
152 Tol = 2e-4;                          %Steady-State tolerance
153 t_max_step_size = 1e-9;              %max step size
154 % T_stop = 500*Ts;                       %stop transient simulation
155 %-----------------------------------------------------------------------
156 currFolder = pwd;
157 pauseTime = 6;
158
159 if iterations > 1
160     %commands for parallel simulations----------------------------------
161     iterFlag = 1;
162     ErrorSimulink = 0;
163     Go = 0;Stop = 0;Finish = 0;
164     TimeOneSimulation = 30;
165     tempFolder = 'C:\Users\Nicola\Documents\MATLAB\.tempParallelCPU';
166     %-------------------------------------------
```

```
167 %     numCores = feature('numcores');%numCores = 5
168       numCores = round(iterations/2);
169       %-----------------------------------------------
170       if numCores > 8
171           numCores = 8;
172       end
173       tsCore1 = uint64(0);tsCore2=tsCore1;tsCore3=tsCore1;tsCore4=tsCore1;tsCore5=tsCore1;
              tsCore6=tsCore1;tsCore7=tsCore1;tsCore8=tsCore1;
174       tStopCore1 = tsCore1;tStopCore2=tsCore1;tStopCore3=tsCore1;tStopCore4=tsCore1;
              tStopCore5=tsCore1;tStopCore6=tsCore1;tStopCore7=tsCore1;tStopCore8=tsCore1;
175       calculate = 0;cont_iter_processed = 1;
176       tMaxExecution = 300;
177
178       wsCore1=struct();wsCore2=struct();wsCore3=struct();wsCore4=struct();
179       wsCore5=struct();wsCore6=struct();wsCore7=struct();wsCore8=struct();
180       cd([currFolder,'\.temp']);save('temp','tempFolder','currFolder','pauseTime');
181       %-----------------------------------------------------------------------
182
183       %first inizialization of cores-----------------------------------------
184       for c=1:1:min(numCores,iterations)
185           switch c
186               case 1
187                   wsCore1.Go=1;wsCore1.Stop=0;wsCore1.Finish=0;wsCore1.iterFlag=iterFlag;
188               case 2
189                   wsCore2.Go=1;wsCore2.Stop=0;wsCore2.Finish=0;wsCore2.iterFlag=iterFlag;
190               case 3
191                   wsCore3.Go=1;wsCore3.Stop=0;wsCore3.Finish=0;wsCore3.iterFlag=iterFlag;
192               case 4
193                   wsCore4.Go=1;wsCore4.Stop=0;wsCore4.Finish=0;wsCore4.iterFlag=iterFlag;
194               case 5
195                   wsCore5.Go=1;wsCore5.Stop=0;wsCore5.Finish=0;wsCore5.iterFlag=iterFlag;
196               case 6
197                   wsCore6.Go=1;wsCore6.Stop=0;wsCore6.Finish=0;wsCore6.iterFlag=iterFlag;
198               case 7
199                   wsCore7.Go=1;wsCore7.Stop=0;wsCore7.Finish=0;wsCore7.iterFlag=iterFlag;
200               case 8
201                   wsCore8.Go=1;wsCore8.Stop=0;wsCore8.Finish=0;wsCore8.iterFlag=iterFlag;
202               otherwise
203                   error('Too much cores!!!')
204           end
205           iterFlag = iterFlag + 1;
206       end
207       cd(tempFolder);save('SharedWorkspace');save('SharedWorkspace');
208       save('wsCore1_Results','Finish');save('wsCore2_Results','Finish');save('
              wsCore3_Results','Finish');save('wsCore4_Results','Finish');
209       save('wsCore5_Results','Finish');save('wsCore6_Results','Finish');save('
              wsCore7_Results','Finish');save('wsCore8_Results','Finish');
210       cd([currFolder,'\.temp']);
211       %first start command--------------------------------------------------
212       for c=1:1:min(numCores,iterations)
213           switch c
214               case 1
215                   tsCore1 = tic;
216                   !"C:\Program Files\MATLAB\R2023a\bin\matlab.exe" -r "LLC_Plecs_init_Core1"
217               case 2
218                   tsCore2 = tic;
219                   !"C:\Program Files\MATLAB\R2023a\bin\matlab.exe" -r "LLC_Plecs_init_Core2"
220               case 3
221                   tsCore3 = tic;
222                   !"C:\Program Files\MATLAB\R2023a\bin\matlab.exe" -r "LLC_Plecs_init_Core3"
223               case 4
224                   tsCore4 = tic;
```

```
225                 !"C:\Program Files\MATLAB\R2023a\bin\matlab.exe" -r "LLC_Plecs_init_Core4"
226             case 5
227                 tsCore5 = tic;
228                 !"C:\Program Files\MATLAB\R2023a\bin\matlab.exe" -r "LLC_Plecs_init_Core5"
229             case 6
230                 tsCore6 = tic;
231                 !"C:\Program Files\MATLAB\R2023a\bin\matlab.exe" -r "LLC_Plecs_init_Core6"
232             case 7
233                 tsCore7 = tic;
234                 !"C:\Program Files\MATLAB\R2023a\bin\matlab.exe" -r "LLC_Plecs_init_Core7"
235             case 8
236                 tsCore8 = tic;
237                 !"C:\Program Files\MATLAB\R2023a\bin\matlab.exe" -r "LLC_Plecs_init_Core8"
238             otherwise
239         end
240         pause(pauseTime)
241     end
242     pause(TimeOneSimulation)
243     %-----------------------------------------------------------------------
244
245     while 1
246         pause(pauseTime)
247         load_n=1;
248         while 1
249             try
250                 cd(tempFolder);
251                 wsCore1 = load('wsCore1_Results');wsCore2 = load('wsCore2_Results');
                        wsCore3 = load('wsCore3_Results');wsCore4 = load('wsCore4_Results');
252                 wsCore5 = load('wsCore5_Results');wsCore6 = load('wsCore6_Results');
                        wsCore7 = load('wsCore7_Results');wsCore8 = load('wsCore8_Results');
253                 cd([currFolder,'\.temp']);
254                 break
255             catch
256                 pause(pauseTime+load_n);fprintf(['Load attempt ',num2str(load_n),' failed
                        ...\n']);load_n=load_n+1;
257                 if load_n == 15
258                     error('Unable to read')
259                 end
260             end
261         end
262         pause(pauseTime)
263         for c=1:1:min(numCores,iterations)  %first start
264             switch c
265                 case 1
266                     if wsCore1.Finish == 1;
267                         temp = wsCore1;calculate=1;tsCore1 = tic;clear wsCore1;
268                         Finish = 0;cd(tempFolder);save('wsCore1_Results','Finish');cd([
                                currFolder,'\.temp']);%no collisions here
269                         wsCore1.Go=0;
270                         if iterFlag <= iterations
271                             wsCore1.Go=1;wsCore1.Stop=0;wsCore1.iterFlag=iterFlag;iterFlag
                                    = iterFlag + 1;
272                         else
273                             wsCore1.Stop=1;
274                         end
275                         save_n = 1;
276                         while 1
277                             try
278                                 cd(tempFolder);save('SharedWorkspace','wsCore1','-append')
                                        ;cd([currFolder,'\.temp']);
279                                 break
280                             catch
```

```
281                             pause(pauseTime+save_n);fprintf(['Saving attempt ',num2str
                                    (save_n),' failed...\n']);save_n=save_n+1;
282                             saveCheck(save_n)
283                         end
284                     end
285                     break
286                 end
287             case 2
288                 if wsCore2.Finish == 1;
289                     temp = wsCore2;calculate=1;tsCore2 = tic;clear wsCore2;
290                     Finish = 0;cd(tempFolder);save('wsCore2_Results','Finish');cd([
                            currFolder,'\.temp']);%no collisions here
291                     wsCore2.Go=0;
292                     if iterFlag <= iterations
293                         wsCore2.Go=1;wsCore2.Stop=0;wsCore2.iterFlag=iterFlag;iterFlag
                                = iterFlag + 1;
294                     else
295                         wsCore2.Stop=1;
296                     end
297                     save_n = 1;
298                     while 1
299                         try
300                             cd(tempFolder);save('SharedWorkspace','wsCore2','-append')
                                    ;cd([currFolder,'\.temp']);
301                             break
302                         catch
303                             pause(pauseTime+save_n);fprintf(['Saving attempt ',num2str
                                    (save_n),' failed...\n']);save_n=save_n+1;
304                             saveCheck(save_n)
305                         end
306                     end
307                     break
308                 end
309             case 3
310                 if wsCore3.Finish == 1;
311                     temp = wsCore3;calculate=1;tsCore3 = tic;clear wsCore3;
312                     Finish = 0;cd(tempFolder);save('wsCore3_Results','Finish');cd([
                            currFolder,'\.temp']);%no collisions here
313                     wsCore3.Go=0;
314                     if iterFlag <= iterations
315                         wsCore3.Go=1;wsCore3.Stop=0;wsCore3.iterFlag=iterFlag;iterFlag
                                = iterFlag + 1;
316                     else
317                         wsCore3.Stop=1;
318                     end
319                     save_n = 1;
320                     while 1
321                         try
322                             cd(tempFolder);save('SharedWorkspace','wsCore3','-append')
                                    ;cd([currFolder,'\.temp']);
323                             break
324                         catch
325                             pause(pauseTime+save_n);fprintf(['Saving attempt ',num2str
                                    (save_n),' failed...\n']);save_n=save_n+1;
326                             saveCheck(save_n)
327                         end
328                     end
329                     break
330                 end
331             case 4
332                 if wsCore4.Finish == 1;
333                     temp = wsCore4;calculate=1;tsCore4 = tic;clear wsCore4;
```

```
334                     Finish = 0;cd(tempFolder);save('wsCore4_Results','Finish');cd([
                            currFolder,'\.temp']);%no collisions here
335                     wsCore4.Go=0;
336                     if iterFlag <= iterations
337                         wsCore4.Go=1;wsCore4.Stop=0;wsCore4.iterFlag=iterFlag;iterFlag
                                = iterFlag + 1;
338                     else
339                         wsCore4.Stop=1;
340                     end
341                     save_n = 1;
342                     while 1
343                         try
344                             cd(tempFolder);save('SharedWorkspace','wsCore4','-append')
                                    ;cd([currFolder,'\.temp']);
345                             break
346                         catch
347                             pause(pauseTime+save_n);fprintf(['Saving attempt ',num2str
                                    (save_n),' failed...\n']);save_n=save_n+1;
348                             saveCheck(save_n)
349                         end
350                     end
351                     break
352                 end
353             case 5
354                 if wsCore5.Finish == 1;
355                     temp = wsCore5;calculate=1;tsCore5 = tic;clear wsCore5;
356                     Finish = 0;cd(tempFolder);save('wsCore5_Results','Finish');cd([
                            currFolder,'\.temp']);%no collisions here
357                     wsCore5.Go=0;
358                     if iterFlag <= iterations
359                         wsCore5.Go=1;wsCore5.Stop=0;wsCore5.iterFlag=iterFlag;iterFlag
                                = iterFlag + 1;
360                     else
361                         wsCore5.Stop=1;
362                     end
363                     save_n = 1;
364                     while 1
365                         try
366                             cd(tempFolder);save('SharedWorkspace','wsCore5','-append')
                                    ;cd([currFolder,'\.temp']);
367                             break
368                         catch
369                             pause(pauseTime+save_n);fprintf(['Saving attempt ',num2str
                                    (save_n),' failed...\n']);save_n=save_n+1;
370                             saveCheck(save_n)
371                         end
372                     end
373                     break
374                 end
375             case 6
376                 if wsCore6.Finish == 1;
377                     temp = wsCore6;calculate=1;tsCore6 = tic;clear wsCore6;
378                     Finish = 0;cd(tempFolder);save('wsCore6_Results','Finish');cd([
                            currFolder,'\.temp']);%no collisions here
379                     wsCore6.Go=0;
380                     if iterFlag <= iterations
381                         wsCore6.Go=1;wsCore6.Stop=0;wsCore6.iterFlag=iterFlag;iterFlag
                                = iterFlag + 1;
382                     else
383                         wsCore6.Stop=1;
384                     end
385                     save_n = 1;
386                     while 1
```

```
387                         try
388                             cd(tempFolder);save('SharedWorkspace','wsCore6','-append')
                                    ;cd([currFolder,'\.temp']);
389                             break
390                         catch
391                             pause(pauseTime+save_n);fprintf(['Saving attempt ',num2str
                                    (save_n),' failed...\n']);save_n=save_n+1;
392                             saveCheck(save_n)
393                         end
394                     end
395                     break
396                 end
397             case 7
398                 if wsCore7.Finish == 1;
399                     temp = wsCore7;calculate=1;tsCore7 = tic;clear wsCore7;
400                     Finish = 0;cd(tempFolder);save('wsCore7_Results','Finish');cd([
                            currFolder,'\.temp']);%no collisions here
401                     wsCore7.Go=0;
402                     if iterFlag <= iterations
403                         wsCore7.Go=1;wsCore7.Stop=0;wsCore7.iterFlag=iterFlag;iterFlag
                                = iterFlag + 1;
404                     else
405                         wsCore7.Stop=1;
406                     end
407                     save_n = 1;
408                     while 1
409                         try
410                             cd(tempFolder);save('SharedWorkspace','wsCore7','-append')
                                    ;cd([currFolder,'\.temp']);
411                             break
412                         catch
413                             pause(pauseTime+save_n);fprintf(['Saving attempt ',num2str
                                    (save_n),' failed...\n']);save_n=save_n+1;
414                             saveCheck(save_n)
415                         end
416                     end
417                     break
418                 end
419             case 8
420                 if wsCore8.Finish == 1;
421                     temp = wsCore8;calculate=1;tsCore8 = tic;clear wsCore8;
422                     Finish = 0;cd(tempFolder);save('wsCore8_Results','Finish');cd([
                            currFolder,'\.temp']);%no collisions here
423                     wsCore8.Go=0;
424                     if iterFlag <= iterations
425                         wsCore8.Go=1;wsCore8.Stop=0;wsCore8.iterFlag=iterFlag;iterFlag
                                = iterFlag + 1;
426                     else
427                         wsCore8.Stop=1;
428                     end
429                     save_n = 1;
430                     while 1
431                         try
432                             cd(tempFolder);save('SharedWorkspace','wsCore8','-append')
                                    ;cd([currFolder,'\.temp']);
433                             break
434                         catch
435                             pause(pauseTime+save_n);fprintf(['Saving attempt ',num2str
                                    (save_n),' failed...\n']);save_n=save_n+1;
436                             saveCheck(save_n)
437                         end
438                     end
439                     break
```

```
                end
            otherwise
                error('Stop=1 not found!')
        end
    end

    %simulation data manipulation---------------------------------------
    if calculate == 1
        if temp.ErrorSimulink == 0
            out = calc(out,temp,temp.iterFlag,param,t_max_step_size);
        end
        calculate = 0;
        cont_iter_processed = cont_iter_processed+1;
        clear temp
    end
    if cont_iter_processed > iterations
        break
    end

    %time limit error---------------------------------------------------
    for c=1:1:min(numCores,iterations)
        switch c
            case 1
                if toc(tsCore1) > tMaxExecution %someting goes wrong in such core
                    warning('Core 1 is stopped... Result Lost')
                    Finish = 1;
                end
            case 2
                if toc(tsCore2) > tMaxExecution %someting goes wrong in such core
                    warning('Core 2 is stopped... Result Lost')
                    Finish = 1;
                end
            case 3
                if toc(tsCore3) > tMaxExecution %someting goes wrong in such core
                    warning('Core 3 is stopped... Result Lost')
                    Finish = 1;
                end
            case 4
                if toc(tsCore4) > tMaxExecution %someting goes wrong in such core
                    warning('Core 4 is stopped... Result Lost')
                    Finish = 1;
                end
            case 5
                if toc(tsCore5) > tMaxExecution %someting goes wrong in such core
                    warning('Core 5 is stopped... Result Lost')
                    Finish = 1;
                end
            case 6
                if toc(tsCore6) > tMaxExecution %someting goes wrong in such core
                    warning('Core 6 is stopped... Result Lost')
                    Finish = 1;
                end
            case 7
                if toc(tsCore7) > tMaxExecution %someting goes wrong in such core
                    warning('Core 7 is stopped... Result Lost')
                    Finish = 1;
                end
            case 8
                if toc(tsCore8) > tMaxExecution %someting goes wrong in such core
                    warning('Core 8 is stopped... Result Lost')
                    Finish = 1;
```

```
501                     end
502                 otherwise
503             end
504         end
505         %-----------------------------------------------------------------
506         if Finish == 1
507             break
508         end
509
510         fprintf('Waiting...\n')
511     end
512     pause(TimeOneSimulation);
513 %     delete 'SharedWorkspace.mat'
514     clear wsCore1 wsCore2 wsCore3 wsCore4 wsCore5 wsCore6 wsCore7 wsCore8
515     cd(tempFolder);save('SharedWorkspace','-struct','out');
516     clear out
517     load('SharedWorkspace');cd(currFolder);
518     table = [Pout' Io_mean' Vo_mean' fsw' M_total' Ploss' Eff' P_loss_MOS' Pcond_loss_MOS'
          PTrasf_loss' PTrasf_cond_loss' PLr_loss' PLr_cond_loss' Pd_cond_loss'
          PCo_tot_loss'+PCa_loss'+PCr_loss']
519 else
520     cd(currFolder)
521     Vo_th = Vo_vet(1);Io = Io_vet(1);vCo_ic = vCo_ic_vet(1);RL = RL_vet(1);
522     %1
523     s = tf('s');
524     for z=1:1:length(f)
525         Mvet = (s^2*Lm*Req_vet(1)*Cr)/(s^3*Cr*Lr*Lm + s^2*Cr*Lr*Req_vet(1) + s^2*Cr*Lm*
              Req_vet(1)+ s^2*Cr*Lm*Rs + s*Cr*Rs*Req_vet(1) + s*Lm + Req_vet(1));   %
              theoretical voltage gain
526         M(z) = abs(evalfr(Mvet,i*2*pi*f(z)))/(n);
527     end
528     if Mi_th_vet(1) < 1/(n)
529         [r idx] = min(abs(M(idxf0:length(M)) - Mi_th_vet(1)));
530         fs = f(idx+length(M(1:idxf0))-1) + round(0.24*(f0-f(idx+length(M(1:idxf0))-1))*1e
              -3)*1e3;
531     else
532         [r idx] = min(abs(M(1:idxf0) - Mi_th_vet(1)));
533         fs = f(idx) + round(0.1*(f0-f(idx))*1e-3)*1e3;
534     end
535     if fs == max(f)
536         error('Not able to regulate this operating point')
537     end
538
539     clear s Mi_th_vet Req_vet Mvet M
540     Ts = 1/fs;
541     T_stop = 500*Ts;                          %stop transient simulation
542     %run Plecs
543     run LLC_Plecs;
544     plsteadystate('LLC_Plecs/Steady-State Analysis','TimeSpan',Ts,'Tolerance',Tol,'NCycles
          ',N);
545     temp = ws2struct();
546     out = calc(out,temp,1,param,t_max_step_size);
547     table = [out.Pout out.Io_mean out.Vo_mean fs out.M_total out.Ploss out.Eff out.
          P_loss_MOS out.Pcond_loss_MOS out.PTrasf_loss out.PTrasf_cond_loss out.PLr_loss
          out.PLr_cond_loss out.Pd_cond_loss out.PCo_tot_loss+out.PCa_loss+out.PCr_loss]
548 end
549
550
551 fprintf('Done\n');
552 toc
553
554
```

```
555 %Losses calcultion and results estraction---------------------------------
556 %-------------------------------------------------------------------------
557 function out = calc(out,temp,j,param,t_max_step_size)
558     try
559     out.Pin(j) = mean(temp.Pdc_in.signals.values);          %Input power
560     out.Pout(j) = mean(temp.Pdc_out.signals.values);        %Output power
561     out.PinLLC(j) = mean(temp.pin_LLC.signals.values);      %Input power LLC
562     out.Vo_mean(j) = mean(temp.vo.signals.values);          %Output voltage
563     out.fsw(j) = temp.fs;
564     out.DVo(j) = findpeaks(temp.vo.signals.values,'NPeaks',1,'SortStr','descend')+
            findpeaks(-temp.vo.signals.values,'NPeaks',1,'SortStr','descend');    %DeltaVo
565     out.Io_mean(j) = mean(temp.io.signals.values);          %Output current
566     out.DIo(j) = findpeaks(temp.io.signals.values,'NPeaks',1,'SortStr','descend')+
            findpeaks(-temp.io.signals.values,'NPeaks',1,'SortStr','descend');    %DeltaIo
567     out.Vin_mean(j) = mean(temp.vin.signals.values);          %Vin
568     out.DVin(j) = findpeaks(temp.vin.signals.values,'NPeaks',1,'SortStr','descend')+
            findpeaks(-temp.vin.signals.values,'NPeaks',1,'SortStr','descend'); %DeltaVin
569     out.iD_mean(j) = mean(temp.i_D1.signals.values);        %Diodes mean current
570     out.M_total(j) = out.Vo_mean(j)/out.Vin_mean(j);
571     out.DiLr(j) = findpeaks(temp.iLr.signals.values,'NPeaks',1,'SortStr','descend')+
            findpeaks(-temp.iLr.signals.values,'NPeaks',1,'SortStr','descend');    %DeltaILr
572     out.iLr_rms(j) = rms(temp.iLr.signals.values);          %rms current iLr
573     out.iSaH_rms(j) = rms(temp.iSaH.signals.values);        %rms current SaH
574     out.iSaL_rms(j) = rms(temp.iSaL.signals.values);        %rms current SaL
575     out.iCa_rms(j) = rms(temp.i_Ca.signals.values);         %rms current Ca
576     out.iD_rms(j) = rms(temp.i_D1.signals.values);          %rms current Diodes
577     out.iCo_e_rms(j) = rms(temp.i_Co_e.signals.values);         %rms current output Cap
578     out.iCo_cer_rms(j) = rms(temp.i_Co_cer.signals.values);         %rms current output
            Cap
579     out.iCo_film1_rms(j) = rms(temp.i_Co_f1.signals.values);         %rms current output
            Cap
580     out.iCo_film2_rms(j) = rms(temp.i_Co_f2.signals.values);         %rms current output
            Cap
581     out.iLr_pk(j) = findpeaks(abs(temp.iLr.signals.values),'NPeaks',1,'SortStr','descend')
            ;          %pk current iLr
582     out.iSaH_pk(j) = findpeaks(abs(temp.iSaH.signals.values),'NPeaks',1,'SortStr','descend
            ');        %pk current SaH
583     out.iSaL_pk(j) = findpeaks(abs(temp.iSaL.signals.values),'NPeaks',1,'SortStr','descend
            ');        %pk current SaL
584     out.iLm_pk(j) = findpeaks(temp.iLm.signals.values,'NPeaks',1,'SortStr','descend');
                  %pk current iLm
585     out.vLr_pk(j) = findpeaks(temp.vLr.signals.values,'NPeaks',1,'SortStr','descend');
                  %pk voltage vLr
586     out.P_loss_MOS(j) = mean(temp.Mosfet_loss.signals.values);       %total losses legs
587     out.Pd_cond_loss_Cree(j) = mean(temp.diodes_loss.signals.values);       %(cond) losses
            diodes
588
589     %Frequency analysis: ------------------------------------------------
590     L = length(temp.Pdc_in.signals.values);
591     Nfft = 2^nextpow2(L);
592     f_fft = 1/t_max_step_size/2*linspace(0,1,Nfft/2);
593     f_fft_res = f_fft(2);
594
595     %Loss contributions: ------------------------------------------------
596     %
597     %Lr+ trasf losses-----
598     harms = temp.fs*[1 2 3 4];
599     iLr_harm = harmonics(temp.iLr, harms, f_fft_res, L, Nfft);        %current harmonics
            extraction
600     for i=1:1:length(harms)
601         [val idx] = min(abs(param.Inductor16uFfor10kWLLC(:,1)-harms(i)));
602         R_Lr_ac_harm_ind(i) = param.Inductor16uFfor10kWLLC(idx,2);
603         [val idx] = min(abs(param.TrasformerFor10kWLLC(:,1)-harms(i)));
```

```
604             R_Lr_ac_harm_tr(i) = param.TrasformerFor10kWLLC(idx,2);
605         end
606         out.PLr_cond_loss(j) = (1+param.alpha_copper*param.deltaTcopper)*sum(param.Nsi*
                R_Lr_ac_harm_ind(:).*iLr_harm(:).^2);    %Inductor conduction losses
607         out.PLr_fe_loss(j) = param.Nsi*param.mult_losses_Lr*param.Vcore_Lr*param.Kc_Lr*temp.fs
                ^param.alpha_Lr*(out.DiLr(j)*param.mu_0*param.mu_eff_gap*param.N_Lr/2/param.
                lcore_Lr)^param.beta_Lr;
608         out.PLr_loss(j) = out.PLr_cond_loss(j) + out.PLr_fe_loss(j);       %Inductor total
                losses
609
610         %MOSFET losses-----
611         out.Pcond_loss_MOS(j) = 2*(1+param.alpha_Ron*param.deltaT_Ron)*param.Ron_a*(out.
                iSaH_rms(j)^2+out.iSaL_rms(j)^2);
612
613         %DC link cap losses------
614         out.PCa_loss(j) = param.R_Ca*out.iCa_rms(j)^2;
615
616         %Trasformer losses---------
617         out.PTrasf_cond_loss(j) = (1+param.alpha_copper*param.deltaTcopper)*sum(
                R_Lr_ac_harm_tr(:).*iLr_harm(:).^2);      %conduction losses Trasformer
618         out.Ptrasf_fe_loss(j) = param.mult_losses_tr*param.Vcore_tr*param.Kc_tr*temp.fs^param.
                alpha_tr*(out.Vo_mean(j)/(4*temp.fs*param.N2*param.Acore_tr))^param.beta_tr;
619         out.PTrasf_loss(j) = out.PTrasf_cond_loss(j) + out.Ptrasf_fe_loss(j); %total losses
                Trasformer
620
621         %Resonant cap losses-------
622         out.PCr_loss(j) = param.R_Cr*out.iLr_rms(j)^2;
623
624         %Diodes losses--------
625         out.Pd_cond_loss(j) = out.Pd_cond_loss_Cree(j);          %diodes (cond) losses from
                Cree plecs model
626
627         %Output cap losses--------
628         out.PCo_e_loss(j) = 4*(param.R_Co_e*out.iCo_e_rms(j)^2) + out.Vo_mean(j)^2/(4*param.
                R_Coe_par);
629         out.PCo_cer_loss(j) = 6*(param.R_Co_cer*out.iCo_cer_rms(j)^2);
630         out.PCo_film_1_loss(j) = 3*(param.R_Co_film_1*out.iCo_film1_rms(j)^2);
631         out.PCo_film_2_loss(j) = 2*(param.R_Co_film_2*out.iCo_film2_rms(j)^2);
632         out.PCo_tot_loss(j) = out.PCo_e_loss(j)+out.PCo_cer_loss(j)+out.PCo_film_1_loss(j)+out
                .PCo_film_2_loss(j);
633
634         %Total losses---------
635         out.Ploss(j) = out.PCa_loss(j)+out.PLr_loss(j)+out.P_loss_MOS(j)+out.PTrasf_loss(j)+
                out.PCr_loss(j)+out.Pd_cond_loss(j)+out.PCo_tot_loss(j);       %Total losses
636
637         %Efficiency----------
638         out.Eff(j) = out.Pout(j)/(out.Pout(j)+out.Ploss(j))*100
639
640         catch ME
641             fprintf('Error in the post processing! The message was:\n%s',ME.message);
642         end
643     end
644     %--------------------------------------------------------------------------
645     %--------------------------------------------------------------------------
646
647
648     %--------------------------------------------------------------------------
649     function res = harmonics(val, nHarm, f_fft_res, L, Nfft)
650         val_fft = fft(val.signals.values,Nfft)/L;
651         for i=1:1:length(nHarm)
652             res(i) = 2*max([abs(val_fft(round(nHarm(i)/f_fft_res))),abs(val_fft(round(nHarm(i)
                    /f_fft_res)-1)),abs(val_fft(round(nHarm(i)/f_fft_res)+1))])/sqrt(2);
653         end
```

```
654 end
655 %--------------------------------------------------------------------------
656
657 %--------------------------------------------------------------------------
658 function WStruct = ws2struct()
659     WSVARS = evalin('caller', 'who');
660     for wscon=1:size(WSVARS,1)
661         thisvar=evalin('caller', WSVARS{wscon});
662         THEWORKSPACE.(WSVARS{wscon})=thisvar;
663     end
664     WStruct=THEWORKSPACE;
665 end
666 %--------------------------------------------------------------------------
667
668 %--------------------------------------------------------------------------
669 function saveCheck(save_n)
670     if save_n >= 15
671         error('I can''t save :(')
672     end
673 end
674 %--------------------------------------------------------------------------
```

C.2 MATLAB® slave code

Herein is reported the MATLAB® code executed on a single CPU core for one of the parallel simulations.

```
1  %--------------ZANATTA NICOLA - nicola.zanatta.2@phd.unipd.it--------------%
2  %% -------------------------Core 1 simulation-----------------------------%
3  %--------------------------------------------------------------------------%
4  clear;clc;
5
6  while 1
7      %waiting loop-------------------------------------------------------
8      load('temp');
9      core = 1;
10     while 1
11         pause(pauseTime+core)
12         %Read from the shared workspace-------------------------------------
13         load_n=1;
14         while 1
15             try
16                 cd(tempFolder);load('SharedWorkspace');cd([currFolder,'\.temp']);
17                 break
18             catch
19                 pause(2*pauseTime+core*load_n)
20                 fprintf(['Load attempt ',num2str(load_n),' failed...\n'])
21                 load_n=load_n+1;
22                 if load_n == 15
23                     error('Unable to read')
24                 end
25             end
26         end
27         %actions-----------------------------------------------------------
```

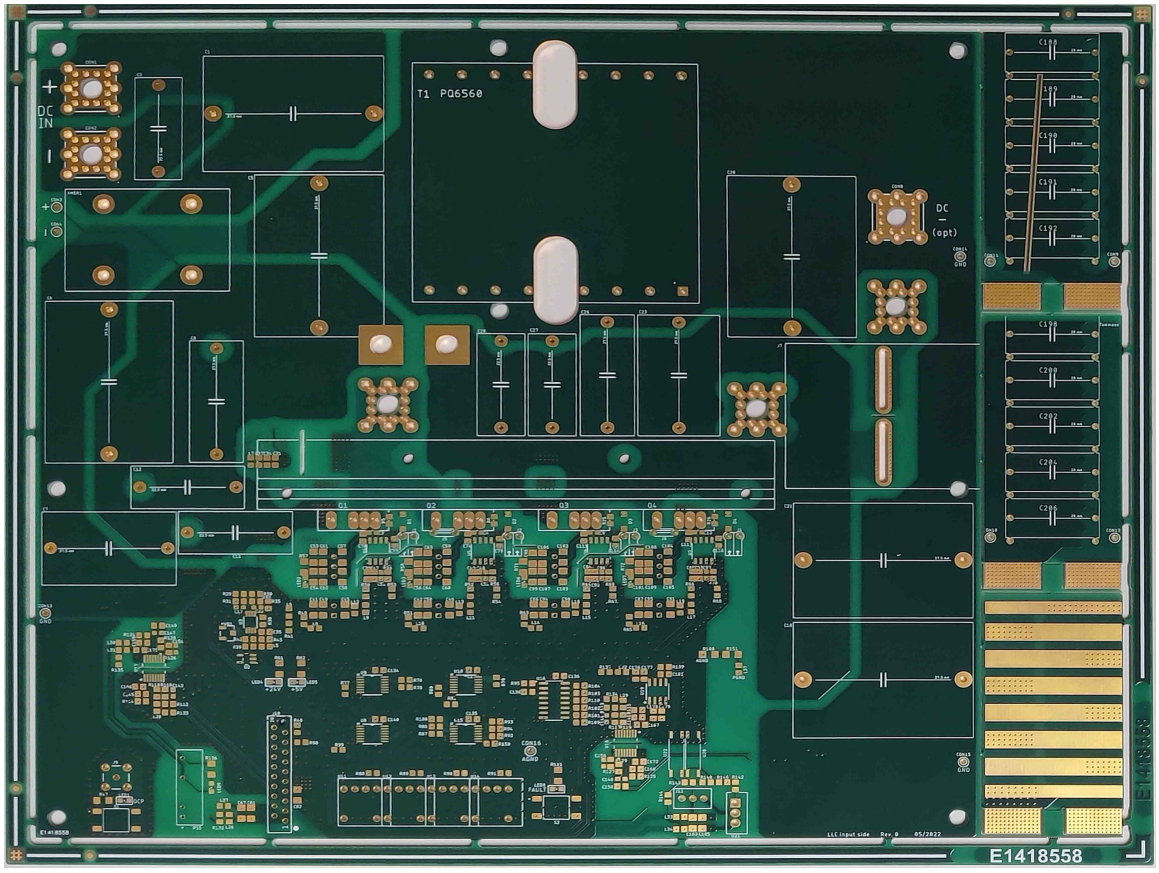
```
28          if wsCore1.Stop == 1
29              quit
30          elseif wsCore1.Go == 1      %if Go=1 the main has updated the variables in the
                wsCore1 structure!!
31              Go = 0;
32              break
33          else
34          end
35          fprintf('Waiting...\n')
36      end
37
38      %simulation settings-------------------------------------------------
39      iterFlag = wsCore1.iterFlag;
40      switch variableToBeIterated
41          case 1      %1 assigned to Vo
42              Vo_th = Vo_vet(wsCore1.iterFlag);
43              vCo_ic = vCo_ic_vet(wsCore1.iterFlag);
44              RL = RL_vet(wsCore1.iterFlag);
45              if length(Io_vet) > 1
46                  Io = Io_vet(wsCore1.iterFlag);
47              end
48          case 2      %2 assigned to Io
49              Io = Io_vet(wsCore1.iterFlag);
50              RL = RL_vet(wsCore1.iterFlag);
51          otherwise
52              error('Error in the variables of this core!!!')
53      end
54
55      s = tf('s');
56      for z=1:1:length(f)
57          Mvet = (s^2*Lm*Req_vet(wsCore1.iterFlag)*Cr)/(s^3*Cr*Lr*Lm + s^2*Cr*Lr*Req_vet(
                wsCore1.iterFlag) + s^2*Cr*Lm*Req_vet(wsCore1.iterFlag)+ s^2*Cr*Lm*Rs + s*Cr*
                Rs*Req_vet(wsCore1.iterFlag) + s*Lm + Req_vet(wsCore1.iterFlag));   %
                theoretical voltage gain
58          M(z) = abs(evalfr(Mvet,i*2*pi*f(z)))/(n);
59      end
60      if Mi_th_vet(wsCore1.iterFlag) < 1/(n)
61          [r idx] = min(abs(M(idxf0:length(M)) - Mi_th_vet(wsCore1.iterFlag)));
62          fs = f(idx+length(M(1:idxf0))-1) + round(0.24*(f0-f(idx+length(M(1:idxf0))-1))*1e
                -3)*1e3;
63      else
64          [r idx] = min(abs(M(1:idxf0) - Mi_th_vet(wsCore1.iterFlag)));
65          fs = f(idx) + round(0.1*(f0-f(idx))*1e-3)*1e3;
66      end
67      Ts = 1/fs;
68      T_stop = 500*Ts;                            %stop transient simulation
69
70      clear wsCore2 wsCore3 wsCore4 wsCore5 wsCore6 wsCore7 wsCore8 s Mvet M
71
72      %simulate-----------------------------------------------------------
73      try
74          %run Plecs
75          run ../LLC_Plecs;   %open_system('LLC_Plecs')
76          plsteadystate('LLC_Plecs/Steady-State Analysis','TimeSpan',Ts,'Tolerance',Tol,'
                NCycles',N)
77      catch ME
78          fprintf('There was an error! The message was:\n%s',ME.message);
79          ErrorSimulink = 1;
80      end
81      clear xSteadyState out param tout
82
83      %store results-----------------------------------------------------
```

```
84      Finish = 1;
85  %     wsCore1 = ws2struct();
86      wsCore1.Go = 0;
87      save_n = 1;
88      while 1
89          try
90              cd(tempFolder);save('SharedWorkspace','wsCore1','-append');save('
                    wsCore1_Results');cd([currFolder,'\.temp']);
91              break
92          catch
93              pause(pauseTime+core*save_n);fprintf(['Saving attempt ',num2str(save_n),'
                    failed...\n']);save_n=save_n+1;
94              if save_n == 15
95                  error('Unable to save')
96              end
97          end
98      end
99      fprintf('Done\n');
100     clear
101 end
102
103 %--------------------------------------------------------------------------
104 function WStruct=ws2struct()
105 WSVARS = evalin('caller', 'who');
106 for wscon=1:size(WSVARS,1)
107     thisvar=evalin('caller', WSVARS{wscon});
108     THEWORKSPACE.(WSVARS{wscon})=thisvar;
109 end
110 WStruct=THEWORKSPACE;
111 end
```

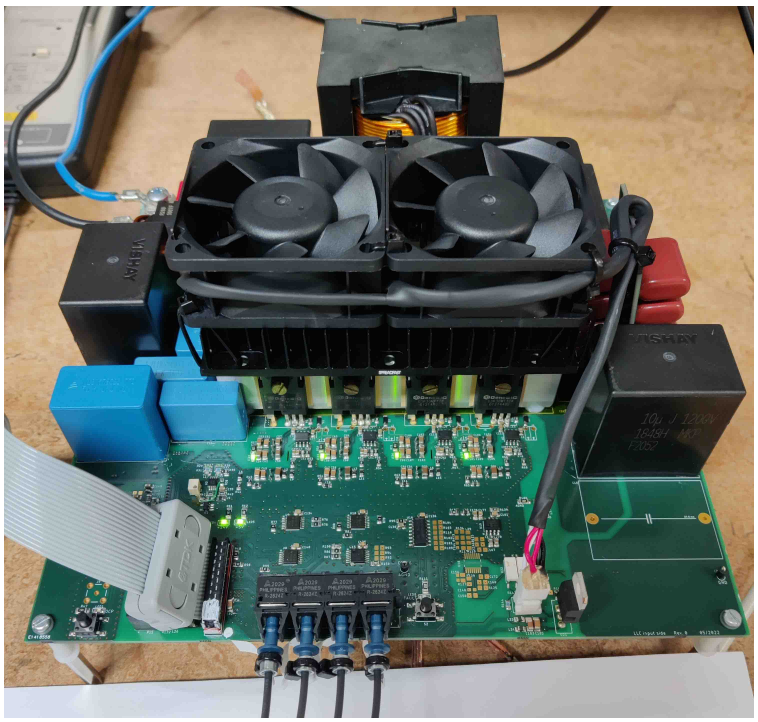
Appendix D

TBB Prototype Documentation

Herein is provided the documentation of the TBB converter prototype analyzed in Ch. 6. The TBB converter is shown in Fig. 6.7 and the hardware demonstrator is shown in Fig. 6.9. In particular Sect. D.1 provides the schematics of the power stage, divided into two boards. The first board includes the transformer and components upstream, while the second board includes components downstream of the transformer. In Sect. D.2 is provided the schematic of the interface board between the power stages and the control board. In Sect. D.3 is provided the code implemented in the control board and remote computer for testing and experimental results in Ch. 6 and Ch. 7. Notably, the prototype is designed in two power stages to simplify the project, and test the parts separately. Additionally it allows topology modifications, and it ensures safety through circuital redundancies (e.g., hardware checks of gate commands and their inhibition in case of errors, and over-current protections). Remarkably, the prototype is designed with possible didactic activities in mind, which is why a significant portion of the PCB area is dedicated to the implementation of these hardware safety measures.



(a)



(b)

Figure D.1: (a) PCB of the power board 1; and (b) complete board.

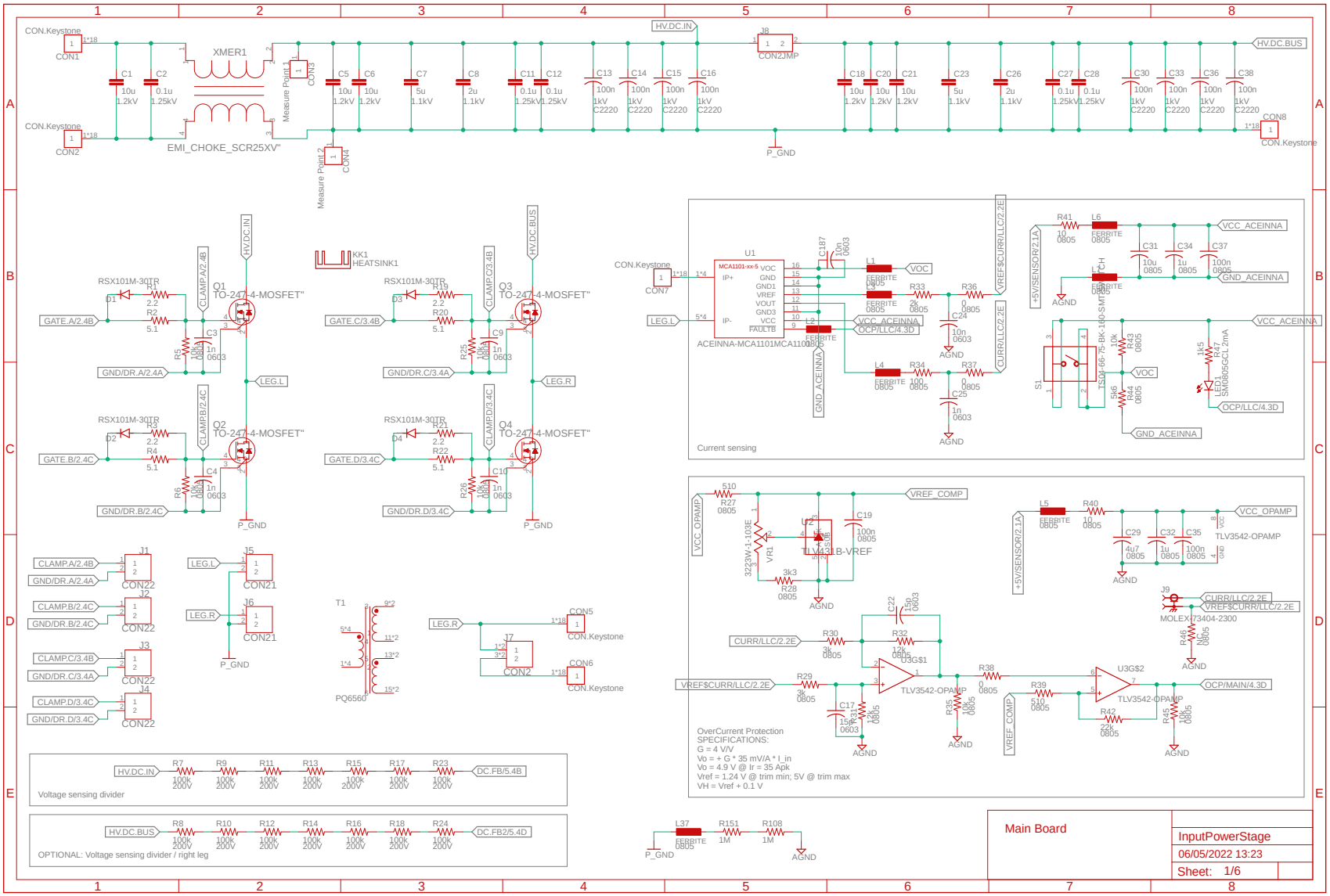


Figure D.2: (1/6) Schematics of the TBB main board 1.

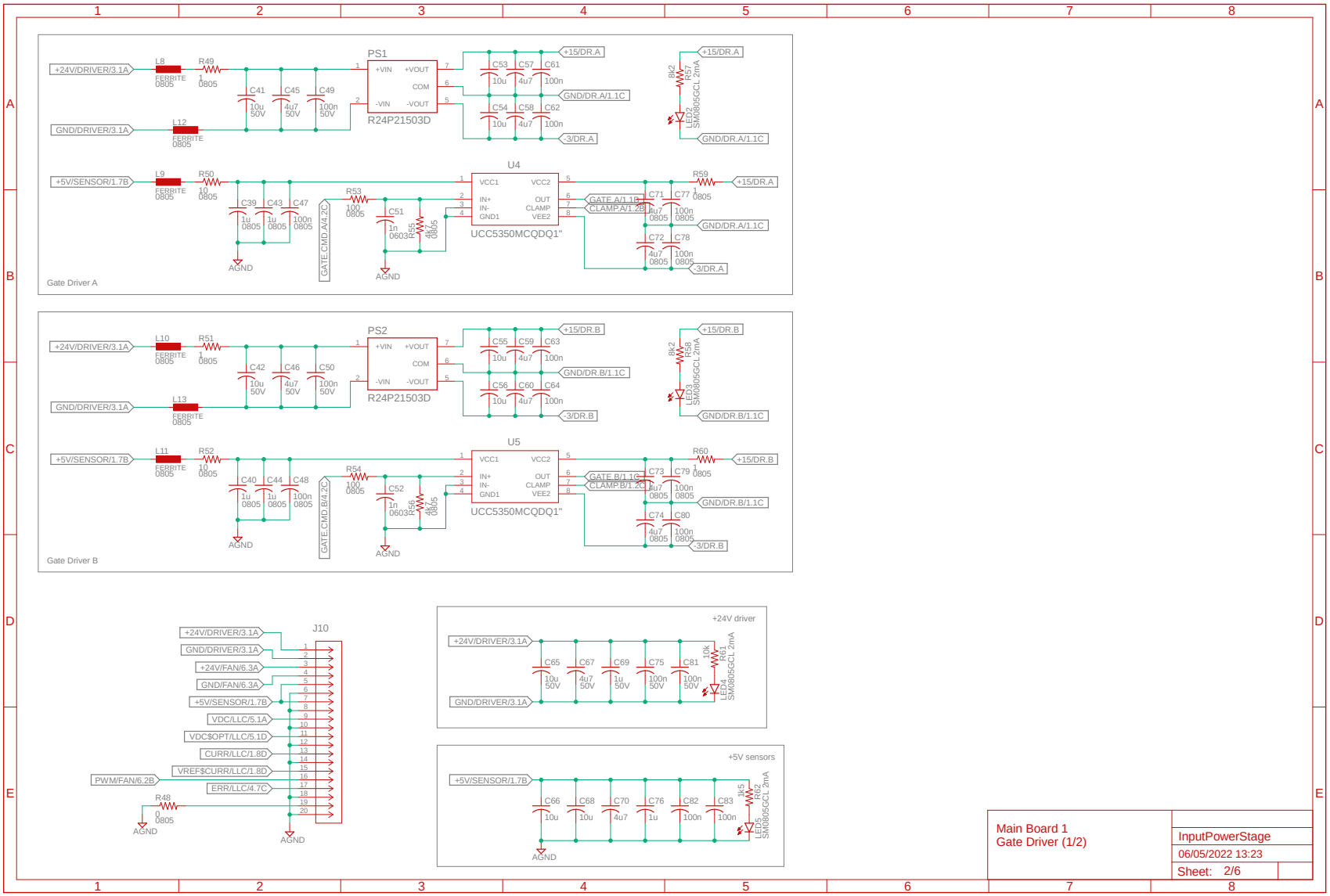


Figure D.2: (2/6) Schematics of the TBB main board 1.

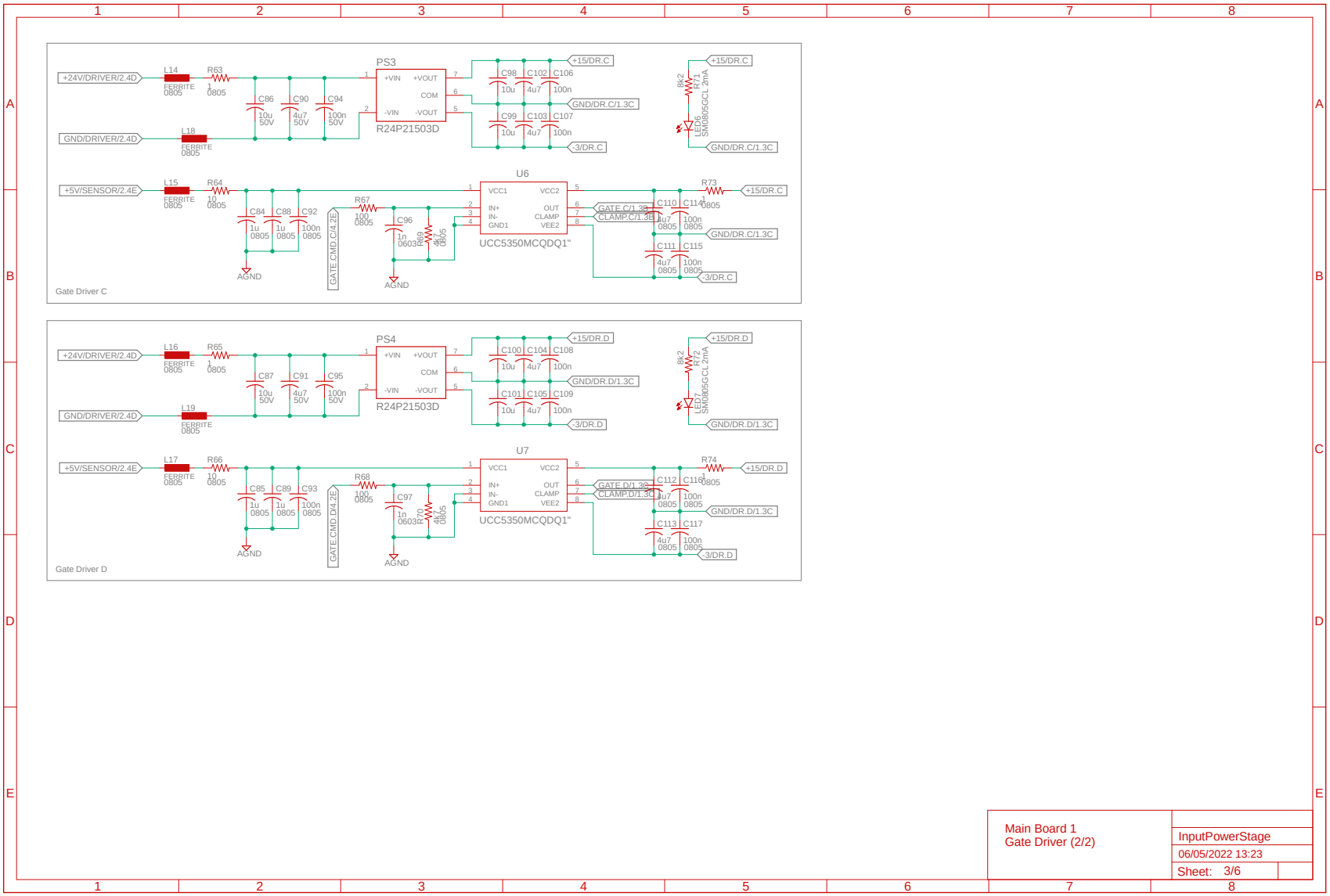


Figure D.2: (3/6) Schematics of the TBB main board 1.

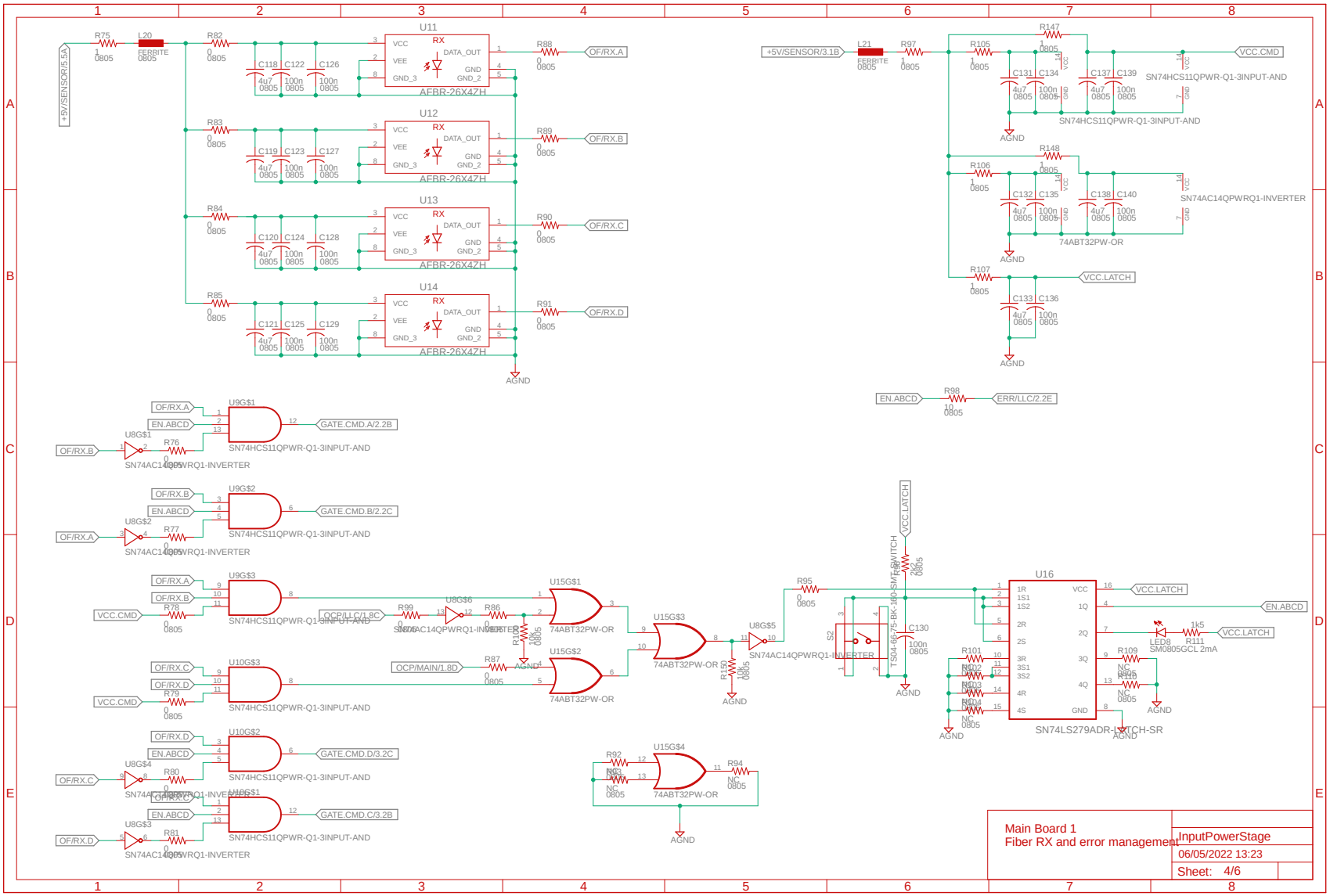


Figure D.2: (4/6) Schematics of the TBB main board 1.

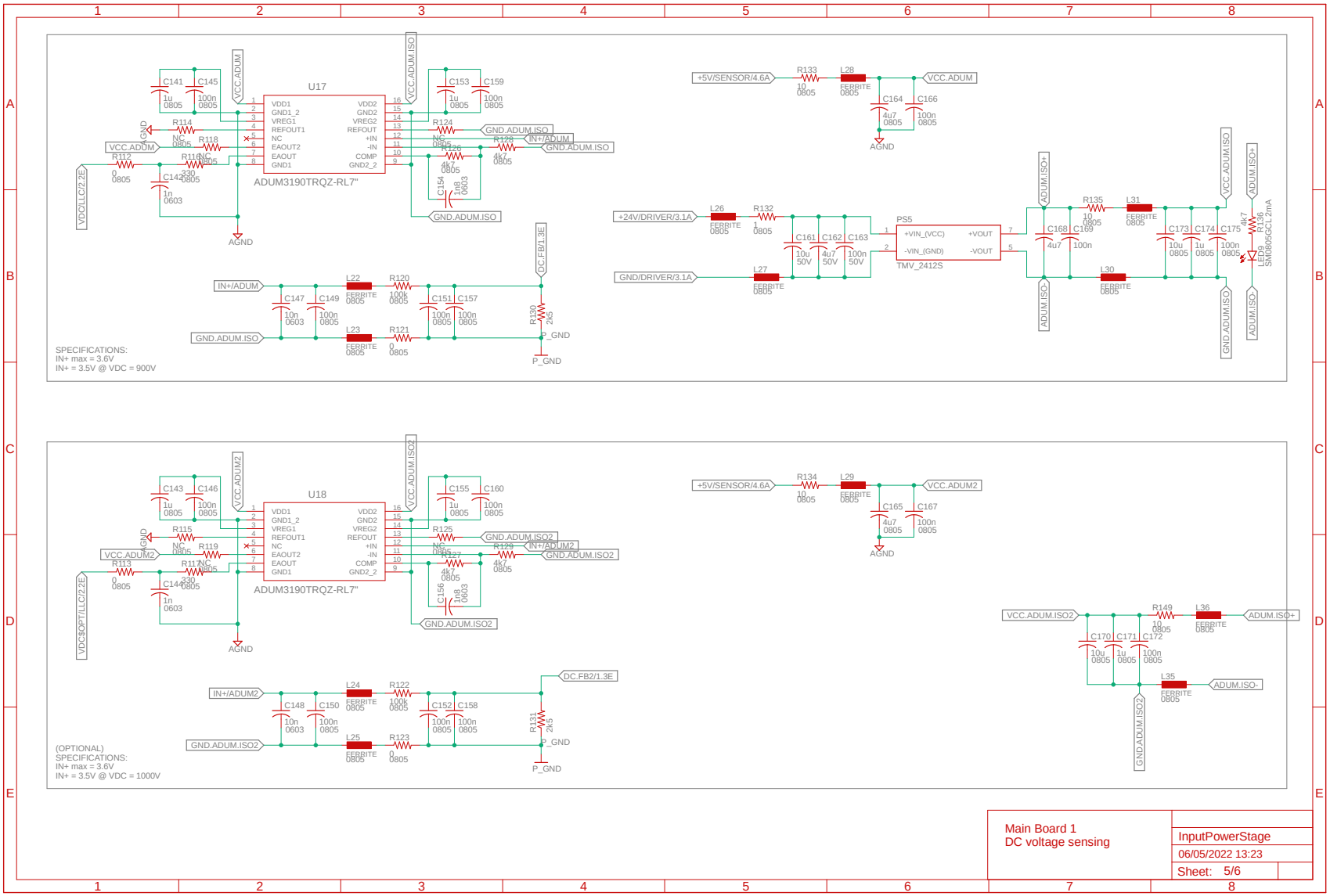


Figure D.2: (5/6) Schematics of the TBB main board 1.

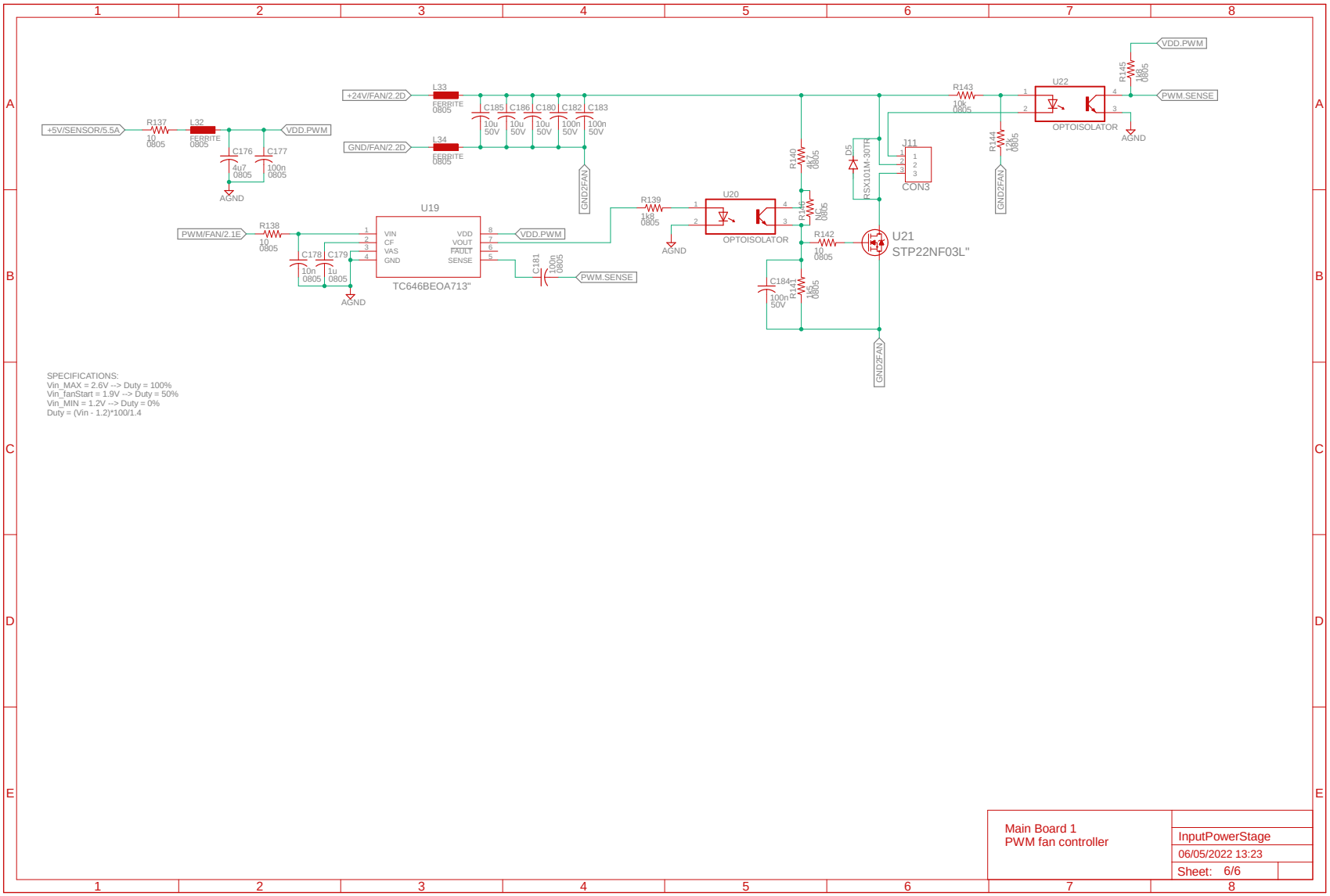


Figure D.2: (6/6) Schematics of the TBB main board 1.

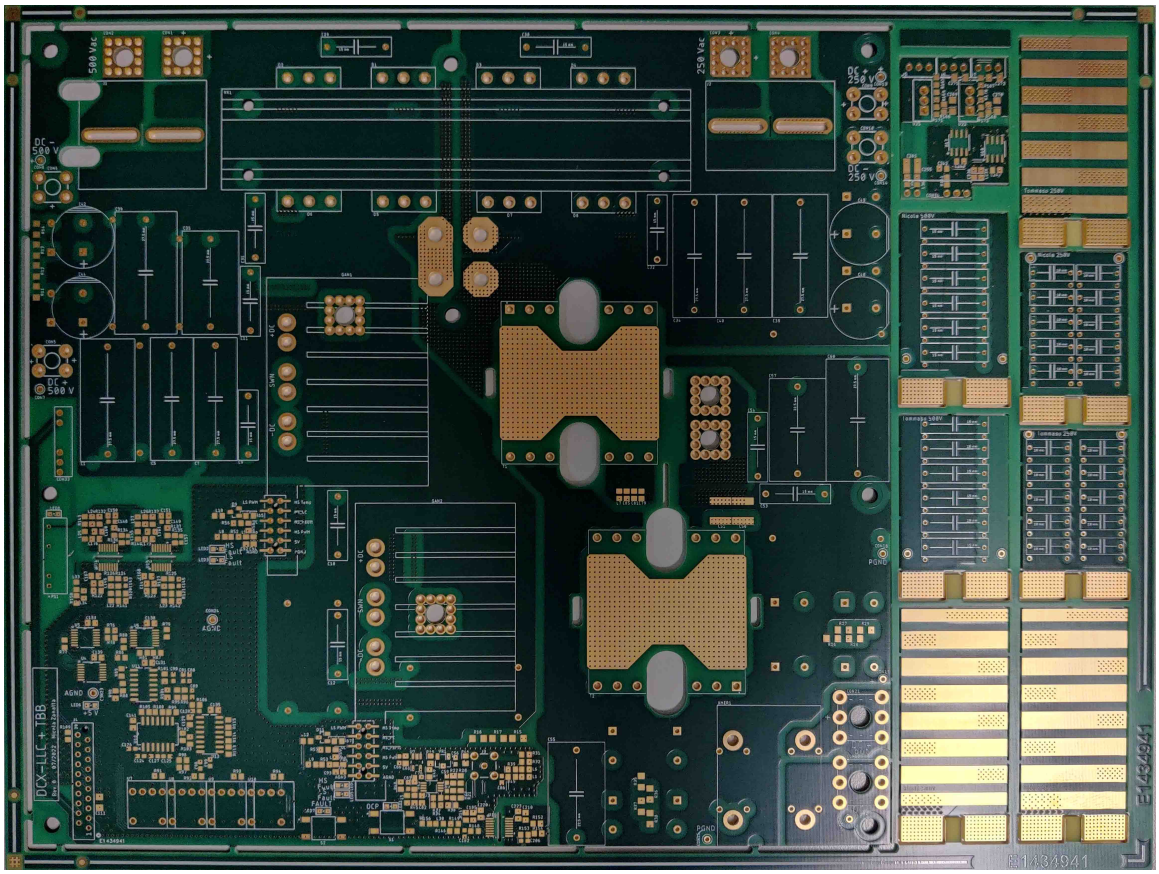
D.1 Power Stage

D.1.1 Main Board 1

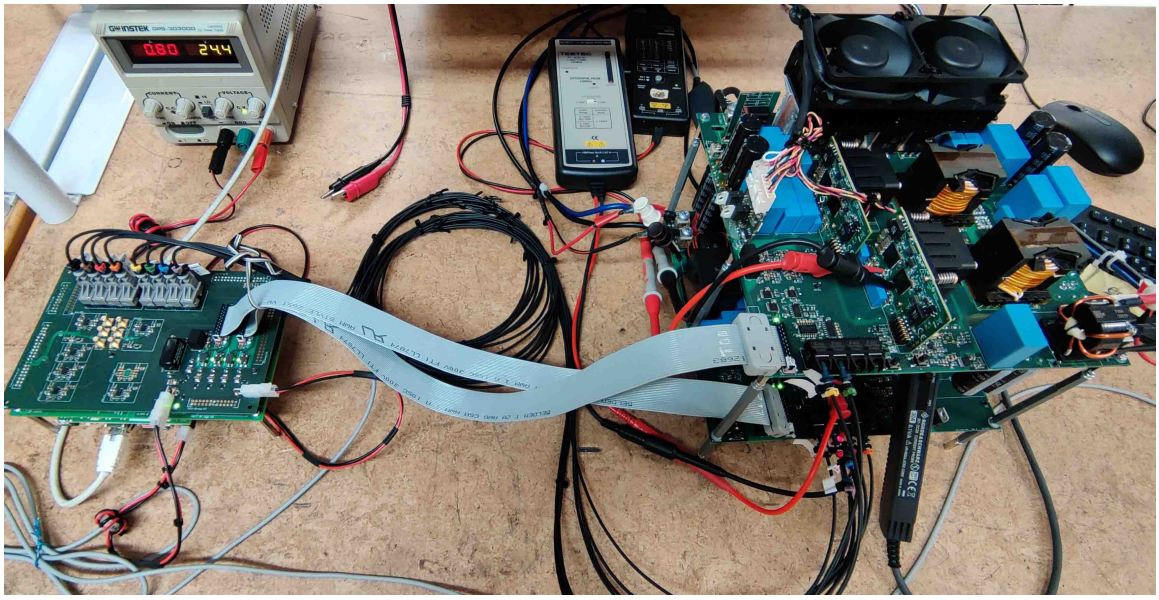
The power board 1 hosts the transformer of the TBB, shown in Fig. 6.5a, and all the components upstream of it, including the resonant capacitor C_{r_1}, the input MOSFETs including the driving circuits, and the input dc bus capacitors. Converter parameters are reported in Table 6.1. Additional circuits include a current sensor including over-current protection, hardware checks of gate commands, inhibition of gate commands in case of errors and error feedback, voltage and current sensing and filtering, and fan controller for MOSFETs ventilation. Gate commands are provided by the interface board in Sect. D.2 through optical fiber, and a flat cable serves for the low voltage power supplies, the error feedback, and measured voltage and current feedback. In Fig. D.1a is shown the realized PCB of the power board 1, while in Fig. D.1b is shown the complete board during testing. The schematics of the power board 1 are shown in Fig. D.2.

D.1.2 Main Board 2

The power board 2 hosts all the components upstream of the transformer of the TBB, including the resonant capacitors C_{r_2} and C_{r_3}, the two rectification bridges DB_1 and DB_2, the two dc bus capacitors C_{o_1} and C_{o_2}, the two boards that host the GaN devices of the interleaved post-regulator, the two inductors of the interleaved post-regulator, and the output dc bus capacitors. Converter parameters are reported in Table 6.1. Two Texas Instruments LMG3425EVM-043 boards, equipped with a heat dissipation system, accommodates the GaN devices, facilitating the development of PCBs for high switching speed GaN components. Additional circuits include a current sensor including over-current protection for i_{L_o}, hardware checks of gate commands, inhibition of gate commands in case of errors and error feedback, voltage and current sensing and filtering, and fan controllers for GaN ventilation. As for power board 1, gate commands are provided by the interface board in Sect. D.2 through optical fiber, and a flat cable serves for the low voltage power supplies, the error feedback, and measured voltages and current feedback. In Fig. D.3a is shown the



(a)



(b)

Figure D.3: (a) PCB of the power board 2; and (b) complete prototype.

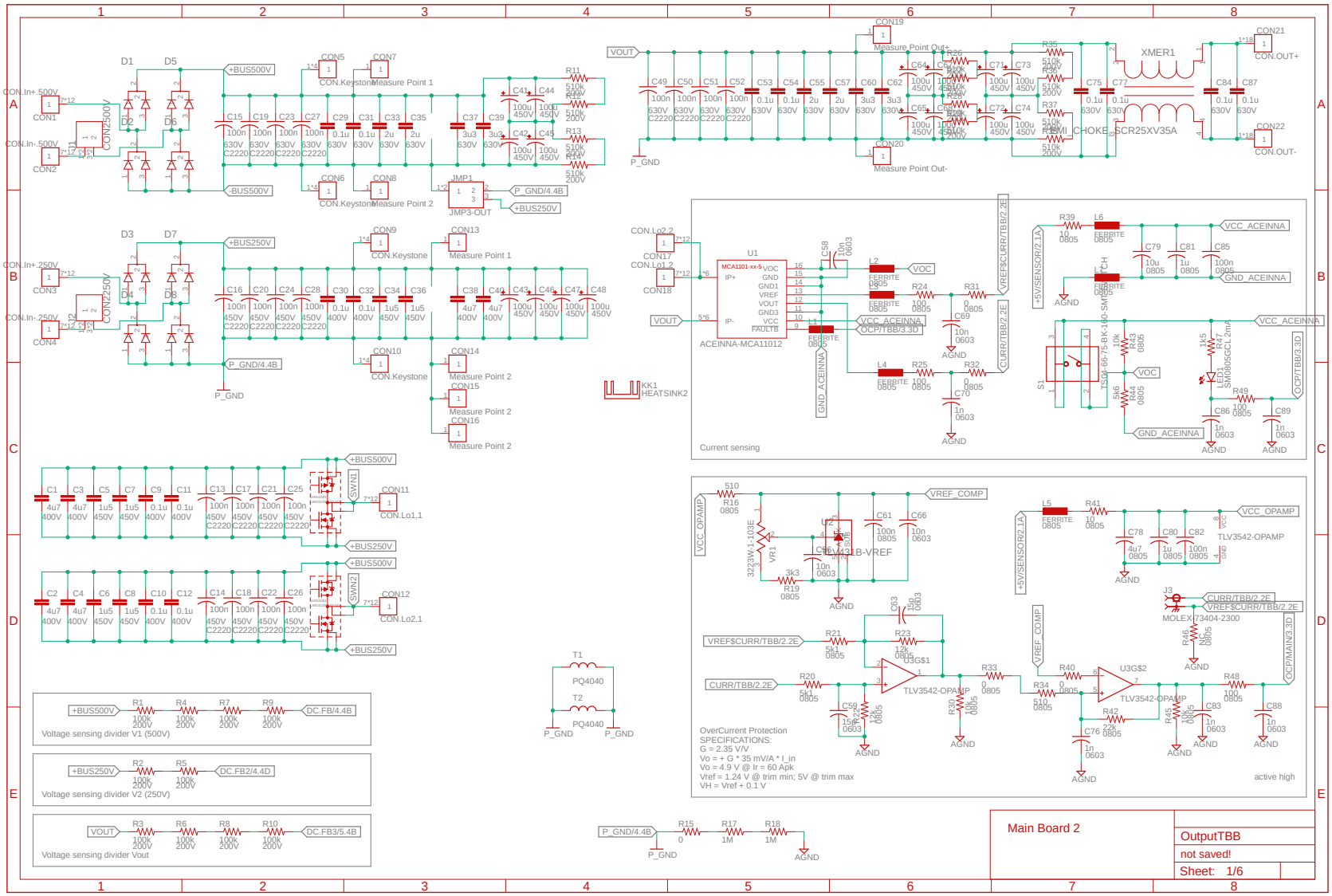


Figure D.4: (1/6) Schematics of the TBB main board 2.

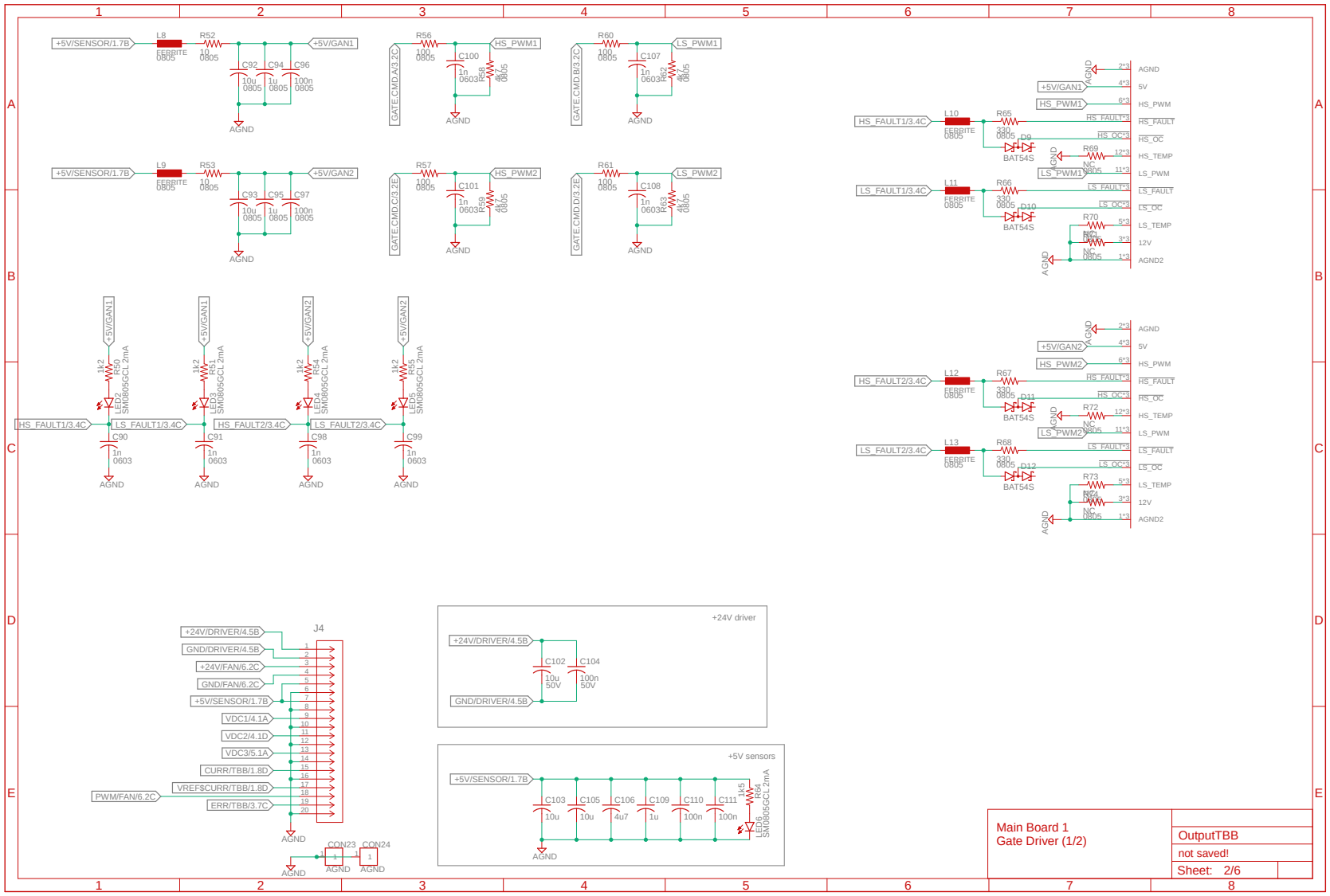


Figure D.4: (2/6) Schematics of the TBB main board 2.

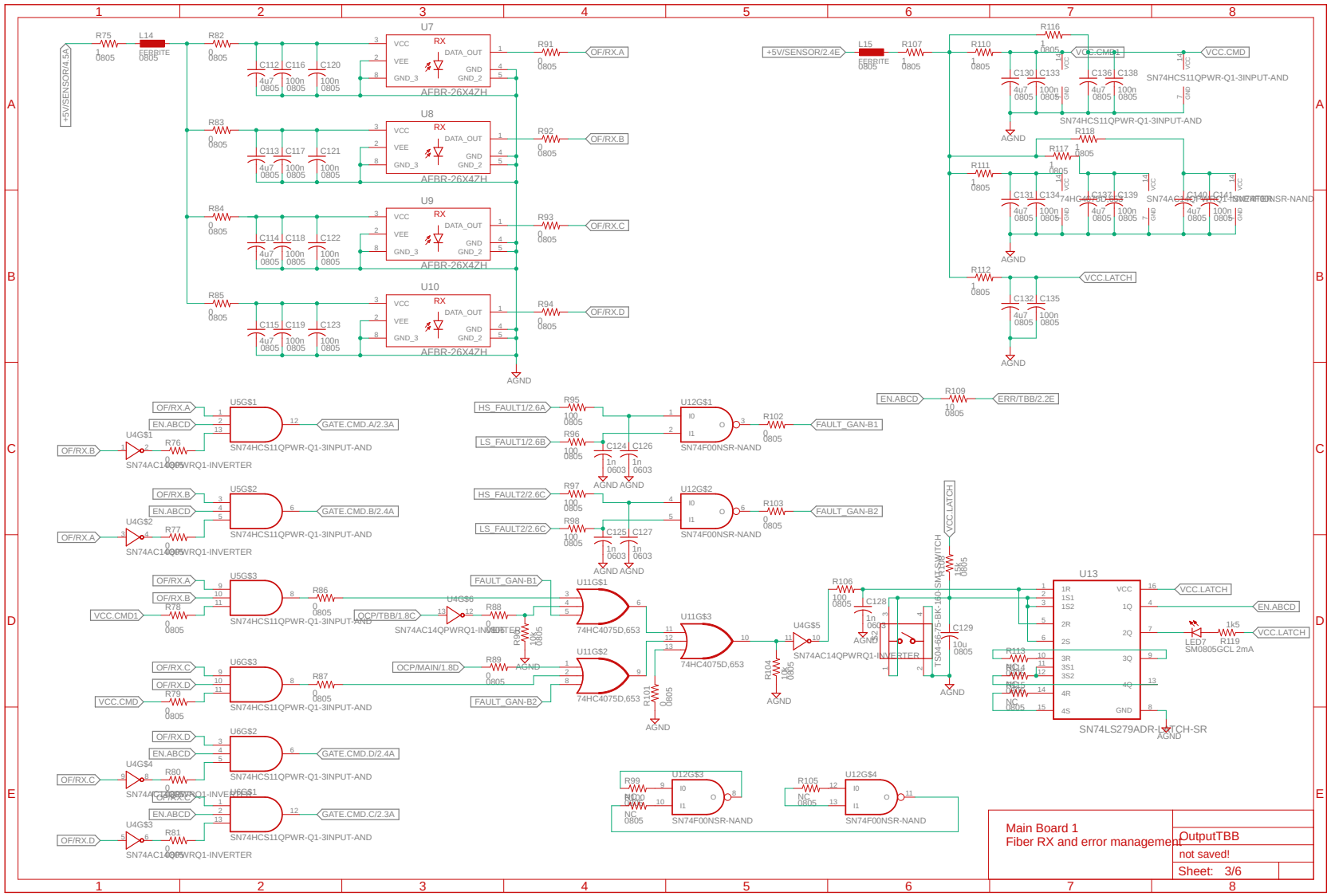


Figure D.4: (3/6) Schematics of the TBB main board 2.

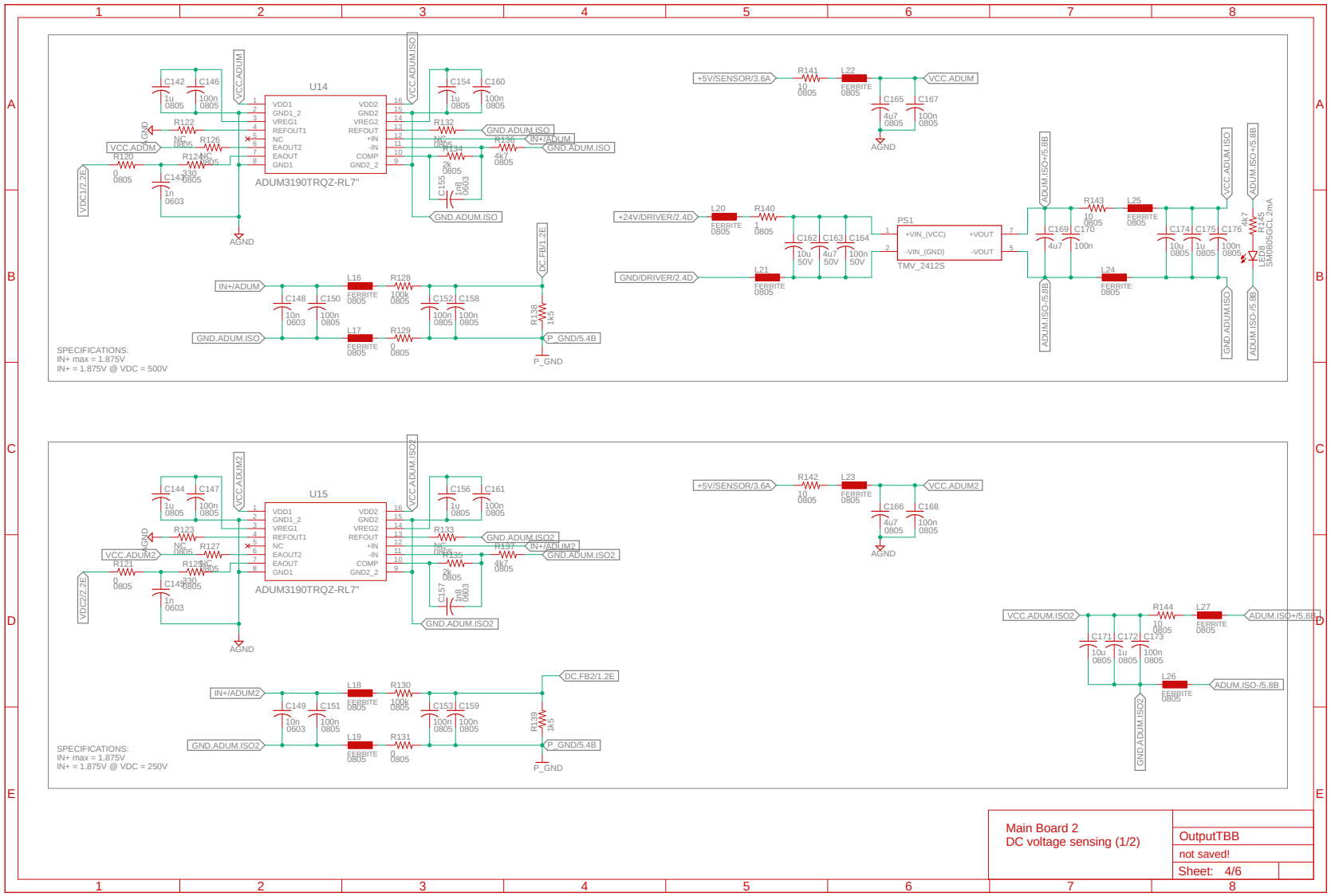


Figure D.4: (4/6) Schematics of the TBB main board 2.

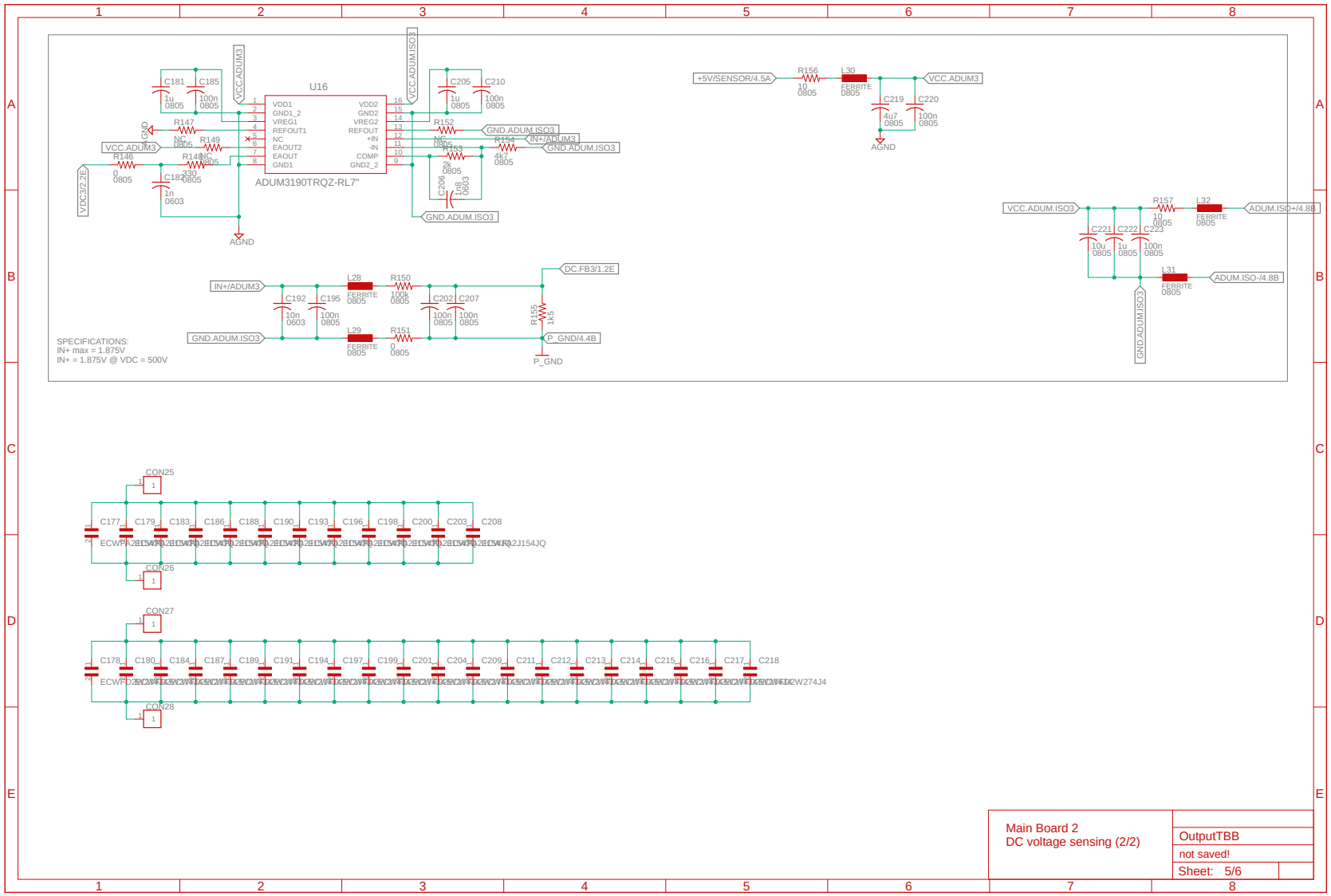


Figure D.4: (5/6) Schematics of the TBB main board 2.

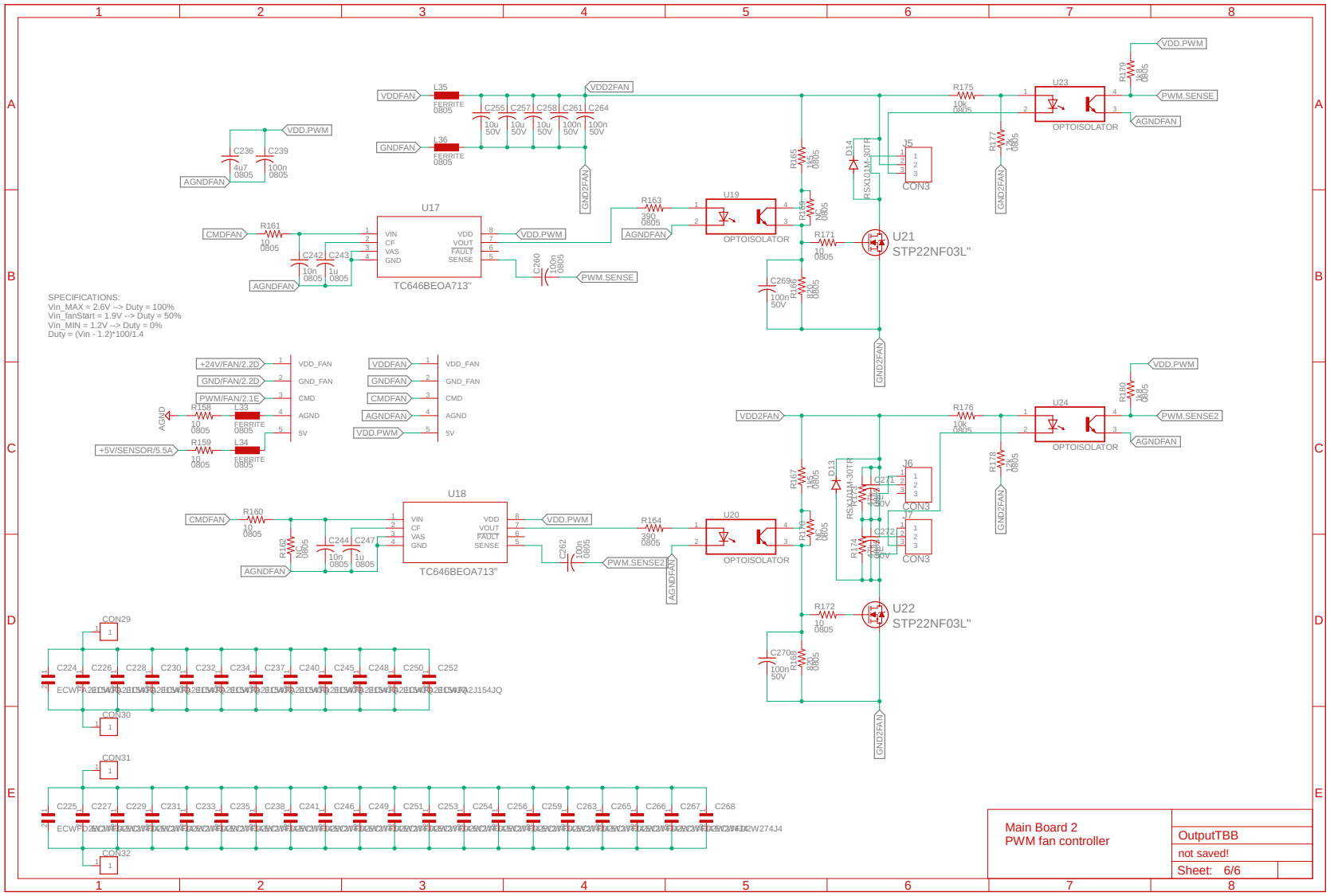


Figure D.4: (6/6) Schematics of the TBB main board 2.

realized PCB of the power board 2, while in Fig. D.3b is shown the complete converter during testing. The schematics of the power board 2 are shown in Fig. D.4.

D.2 Interface Board

The interface board serves multiple functions within the system. It supplies power to the electronics on the power boards and the control board. Additionally, it houses the fiber optic transmitters responsible for sending gate signals. This board also takes on the role of filtering the analog signals related to measured currents and voltages before these signals are acquired by the control board. The control board is based on the National Instruments sbRIO-9607, which integrates both a real-time (RT) processor and an field programmable gate array (FPGA). It is expanded with a National Instruments sbRIO-9684 mezzanine card. This card provides isolated analog inputs and isolated digital outputs, further expanding the board's functionality. The designed interface board in connected directly on top of this mezzanine card, as shown in Fig. D.3b. The realized PCB is visible in Fig. D.5 and the schematics of the interface board are shown in Fig. D.6.

D.3 LabVIEW™ Code

The programming language LabVIEW™ is utilized to program the FPGA, the RT processor, and to create a user-friendly control interface on the computer. This control interface enables users to effectively monitor and control the converter's operation, and manage the input dc source and the output load. Within the FPGA, tasks include generating gate commands for the switches and handling errors. The FPGA is chosen for these tasks due to its ability to provide fixed and predictable timing, which is critical for these operations. Meanwhile, the RT system is responsible for less time-critical operations, such as the online optimization described in Ch. 7. Furthermore, the RT system plays a crucial role in establishing the data link between the remote computer and the FPGA, which is responsible for monitoring and controlling the converter.

The FPGA is programmed using the LabVIEW™ code reported in Fig. D.7. This code

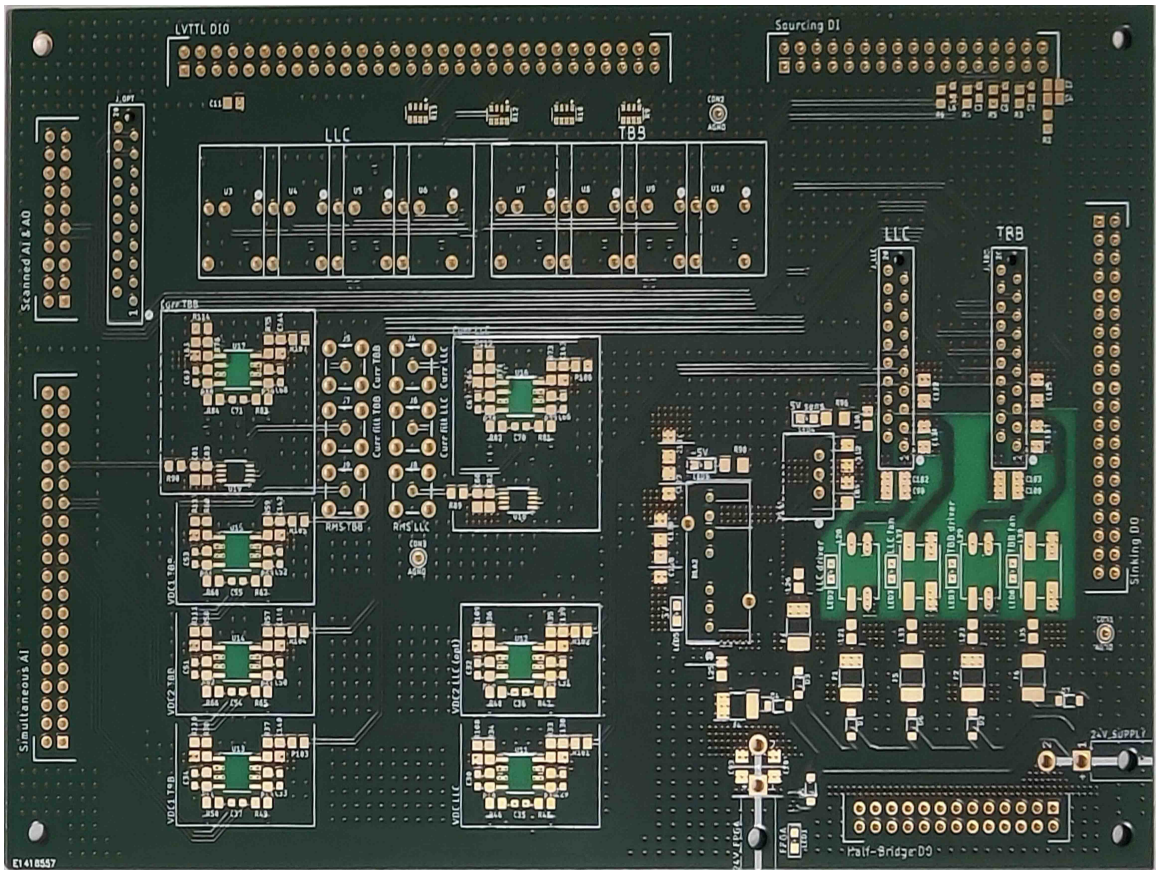


Figure D.5: PCB of the interface board.

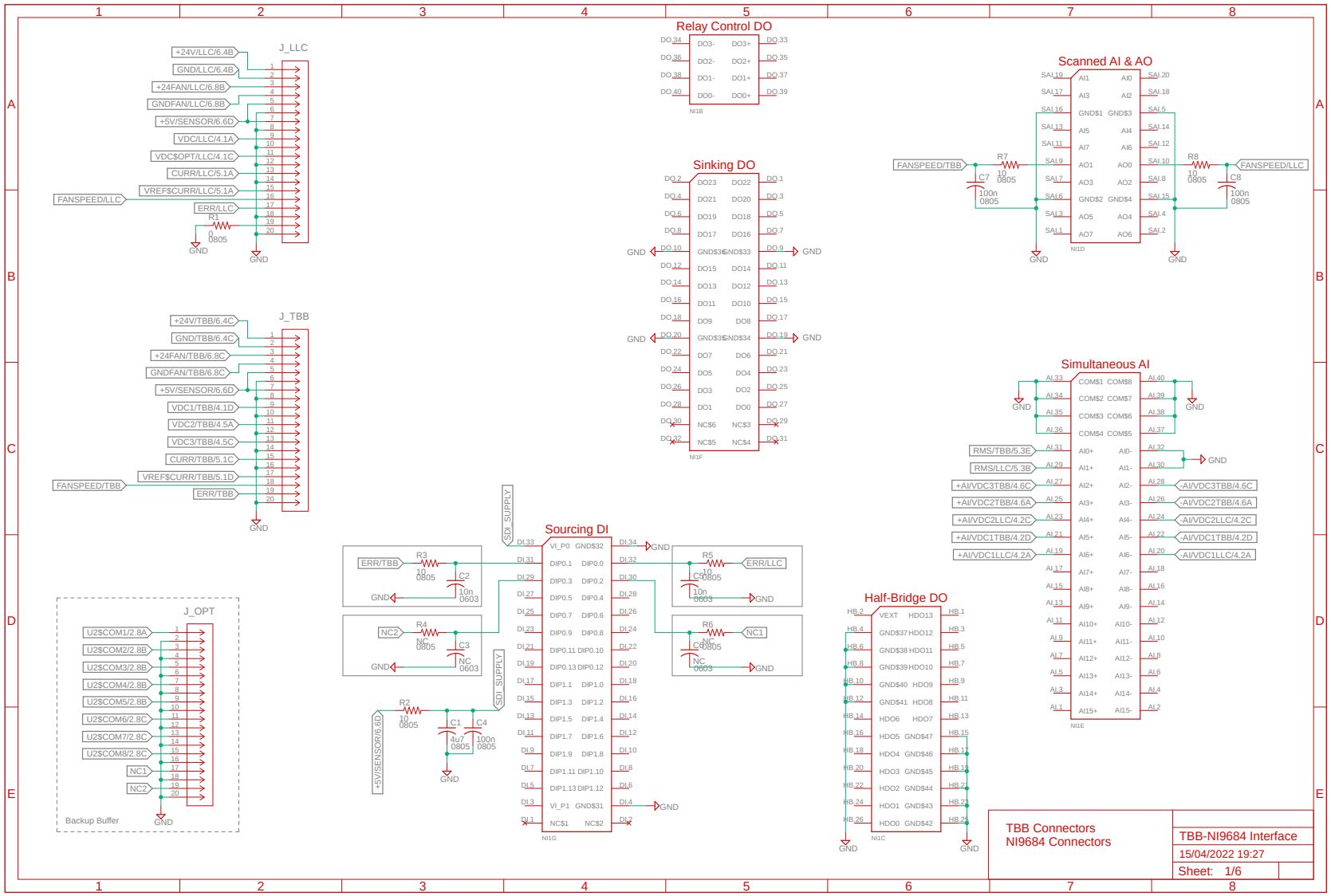


Figure D.6: (1/6) Schematics of the TBB interface board.

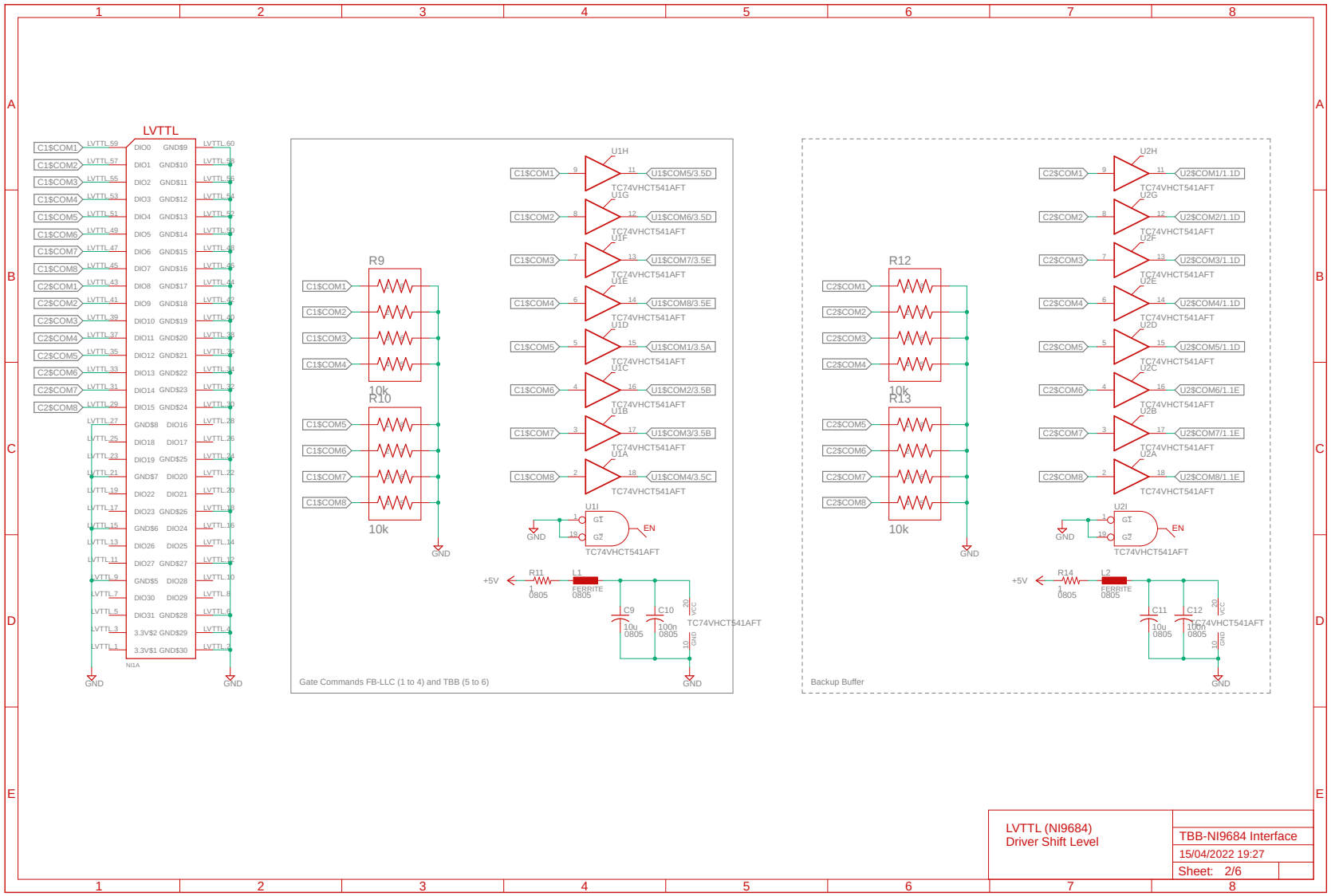


Figure D.6: (2/6) Schematics of the TBB interface board.

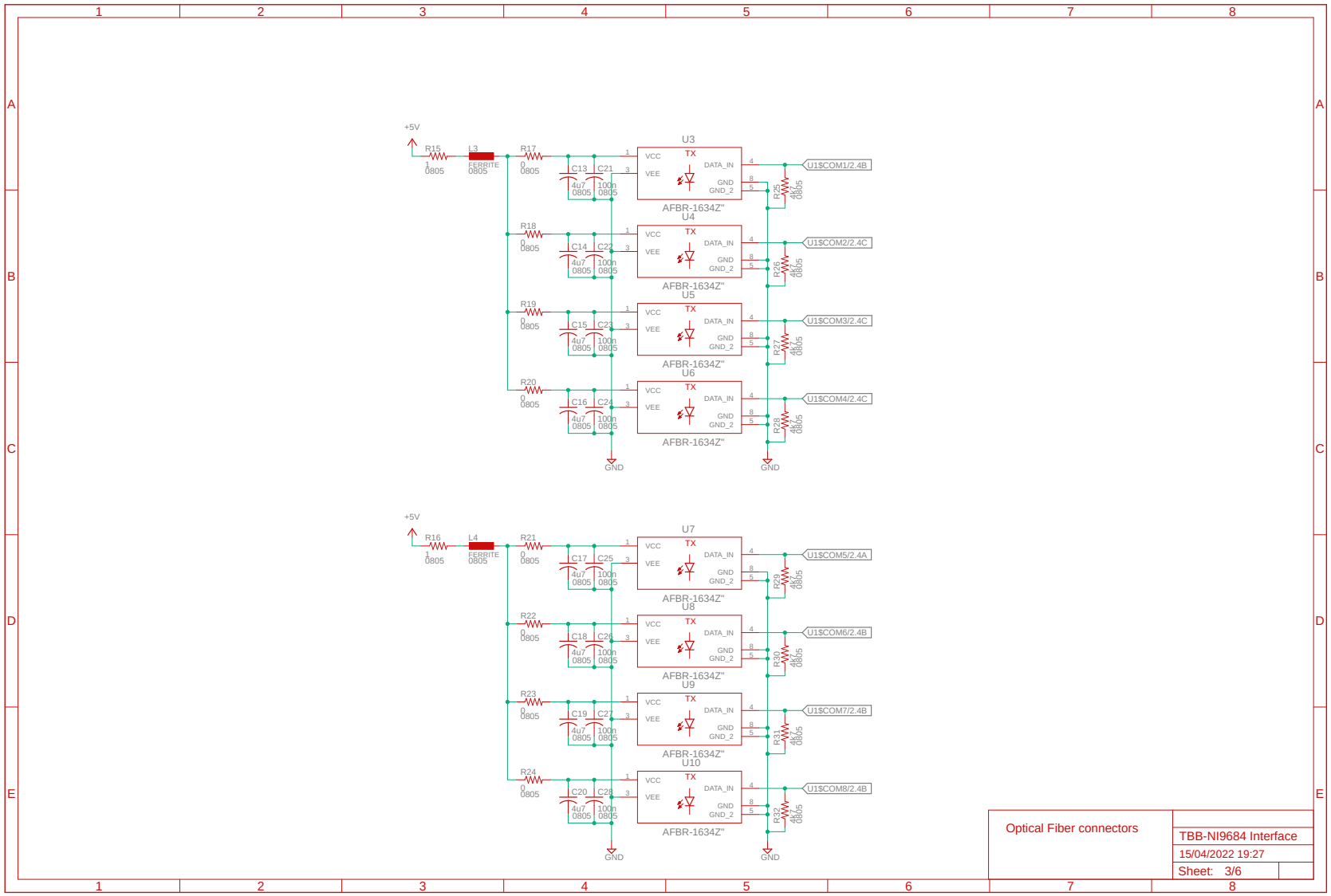


Figure D.6: (3/6) Schematics of the TBB interface board.

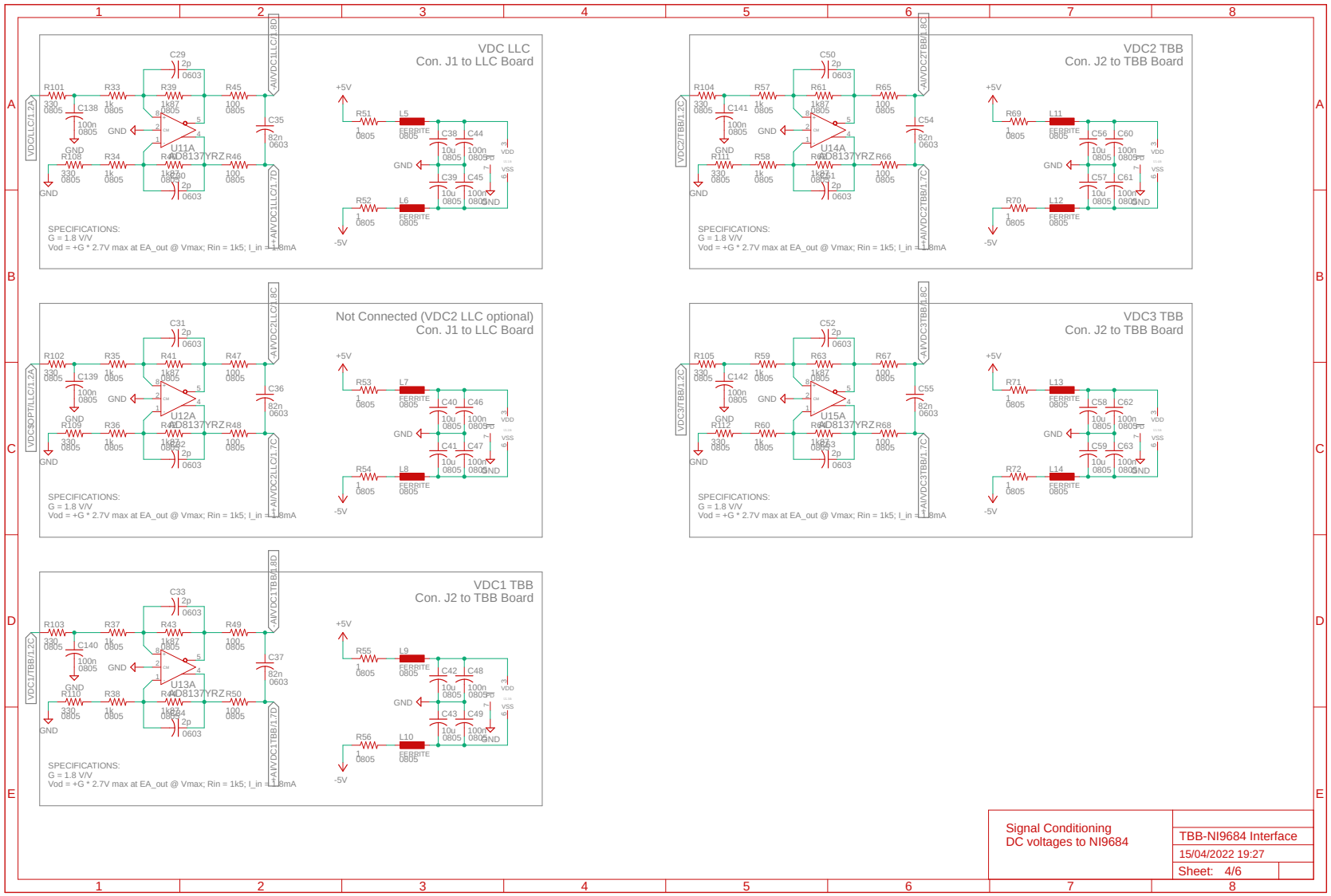


Figure D.6: (4/6) Schematics of the TBB interface board.

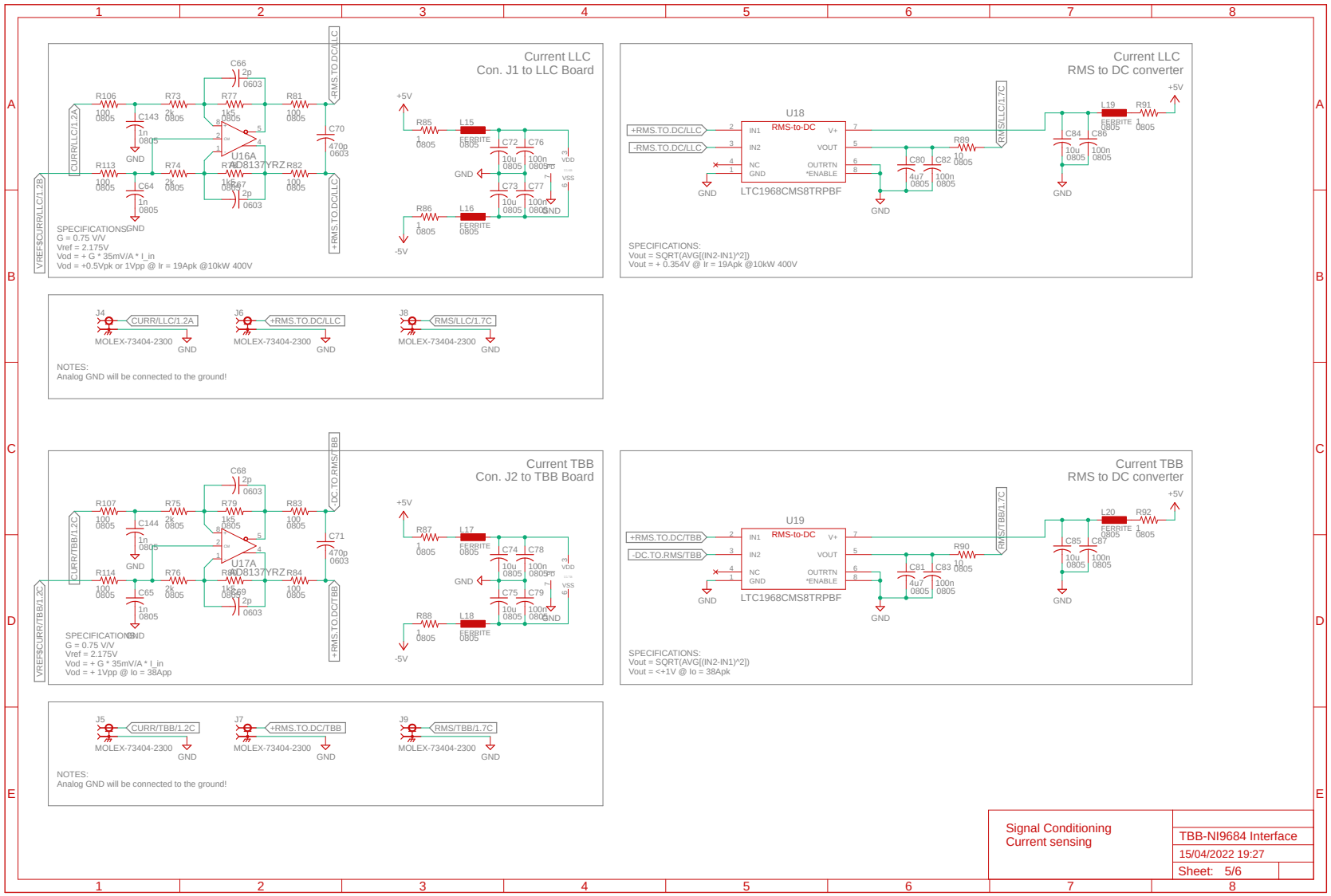


Figure D.6: (5/6) Schematics of the TBB interface board.

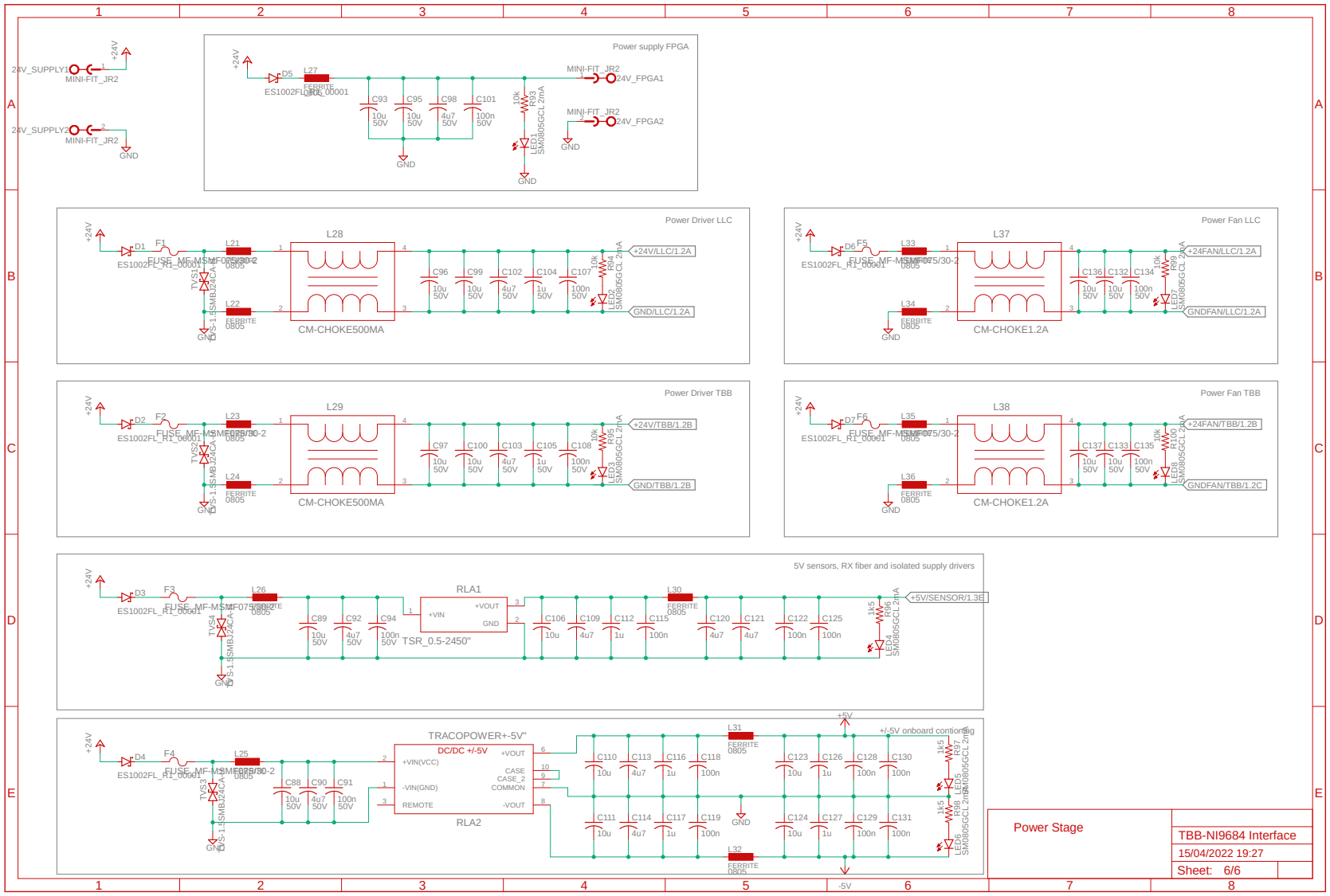


Figure D.6: (6/6) Schematics of the TBB interface board.

handles all the data connections, both analog and digital, with the TBB converter. It specifically manages gate commands with proper synchronization, acquires analog inputs properly and filters them, controls the output voltage to the desired reference value, and handles over-current and over-voltage conditions to ensure the converter operates safely.

The RT processor is programmed using the LabVIEW™ code reported in Fig. D.8. This code effectively handles all commands and data transmitted between the FPGA and the remote computer, as well as performs the efficiency optimization presented in Ch. 7.

The remote computer is programmed using the LabVIEW™ code reported in Fig. D.9, and an user-friendly control panel is displayed in Fig. D.10. Through this computer interface, users can configure various parameters including the input voltage, load settings, switching frequencies of the converter, dead times, PID controller parameters, parameters related to the ESC introduced in Ch. 7, as well as setpoints and thresholds for over-voltage and over-current protection. This interface greatly simplifies the control and monitoring of the converter system.

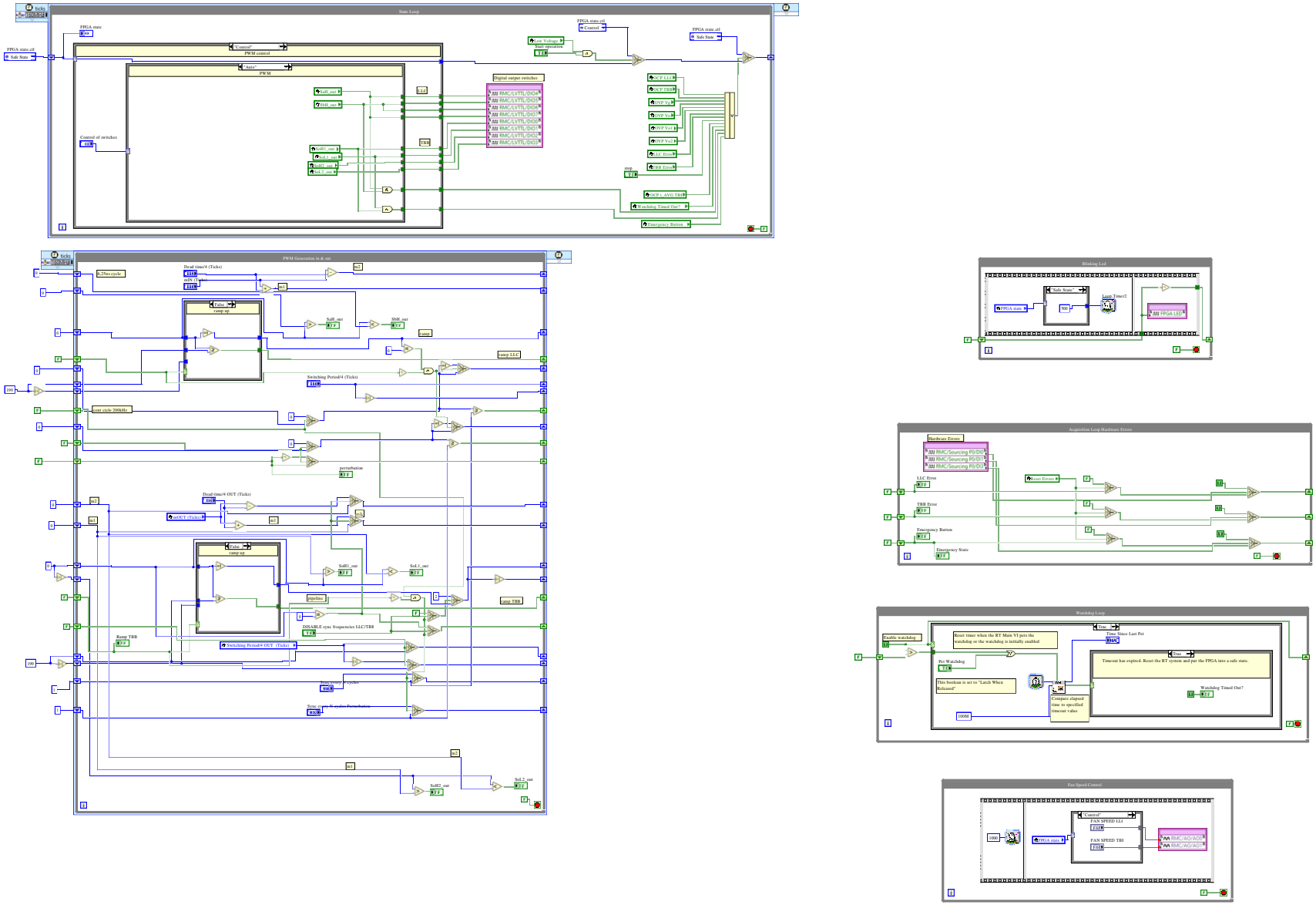


Figure D.7: (1/2) LabVIEW™ FPGA code.

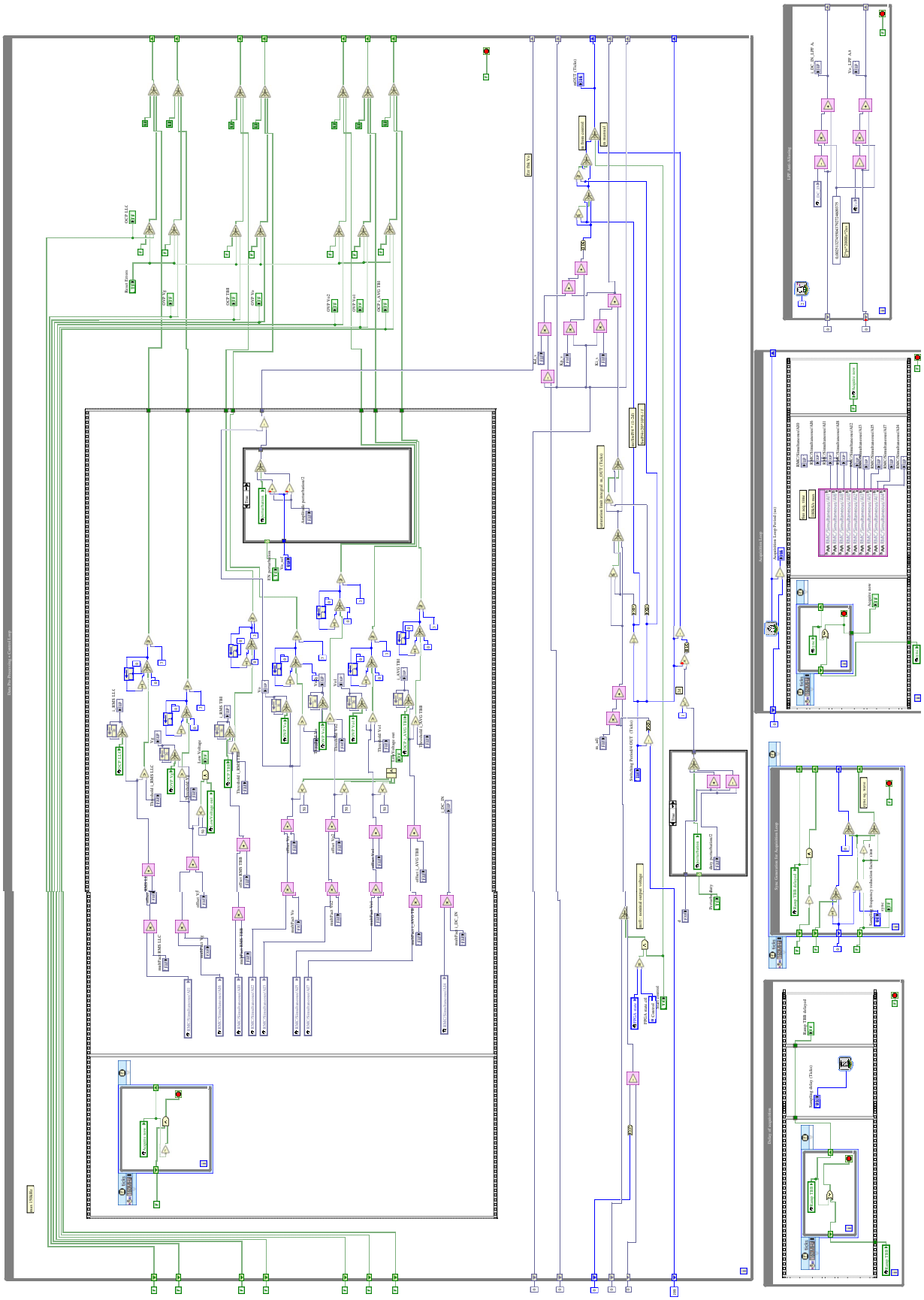


Figure D.7: (2/2) LabVIEW™ FPGA code.

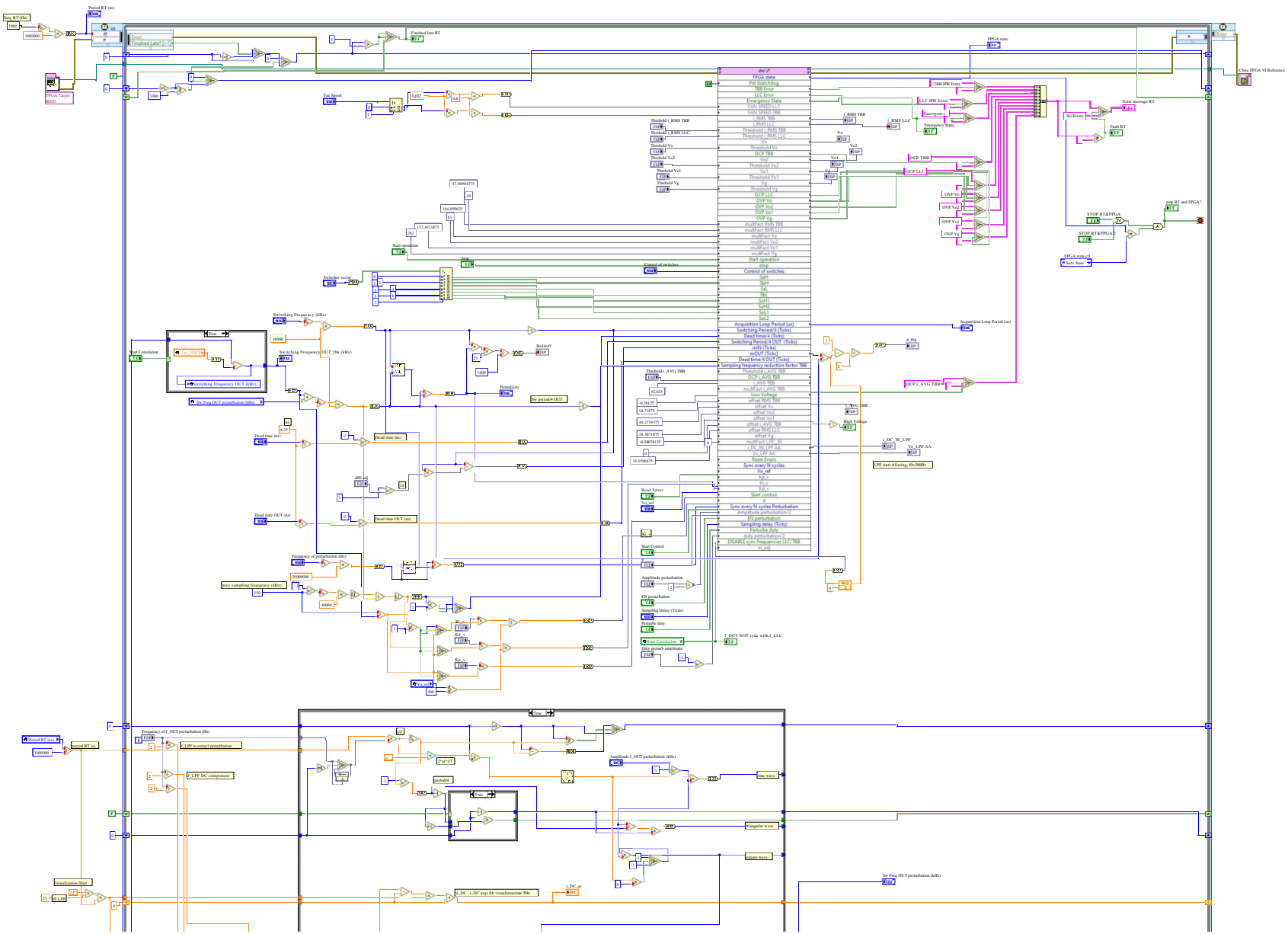


Figure D.8: (1/2) LabVIEW™ RT system code.

Figure D.8: (2/2) LabVIEW™ RT system code.

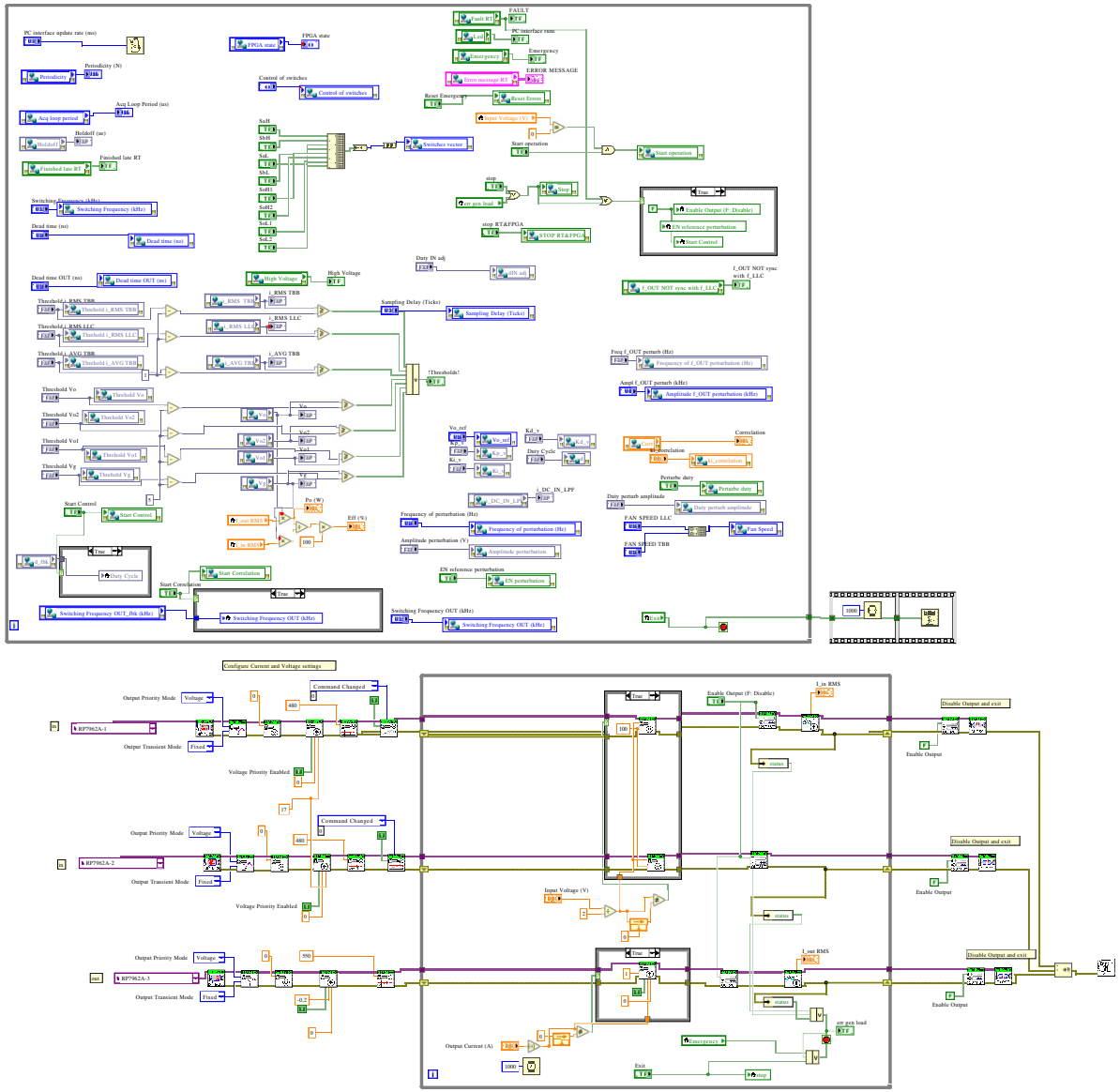


Figure D.9: LabVIEW™ computer code.

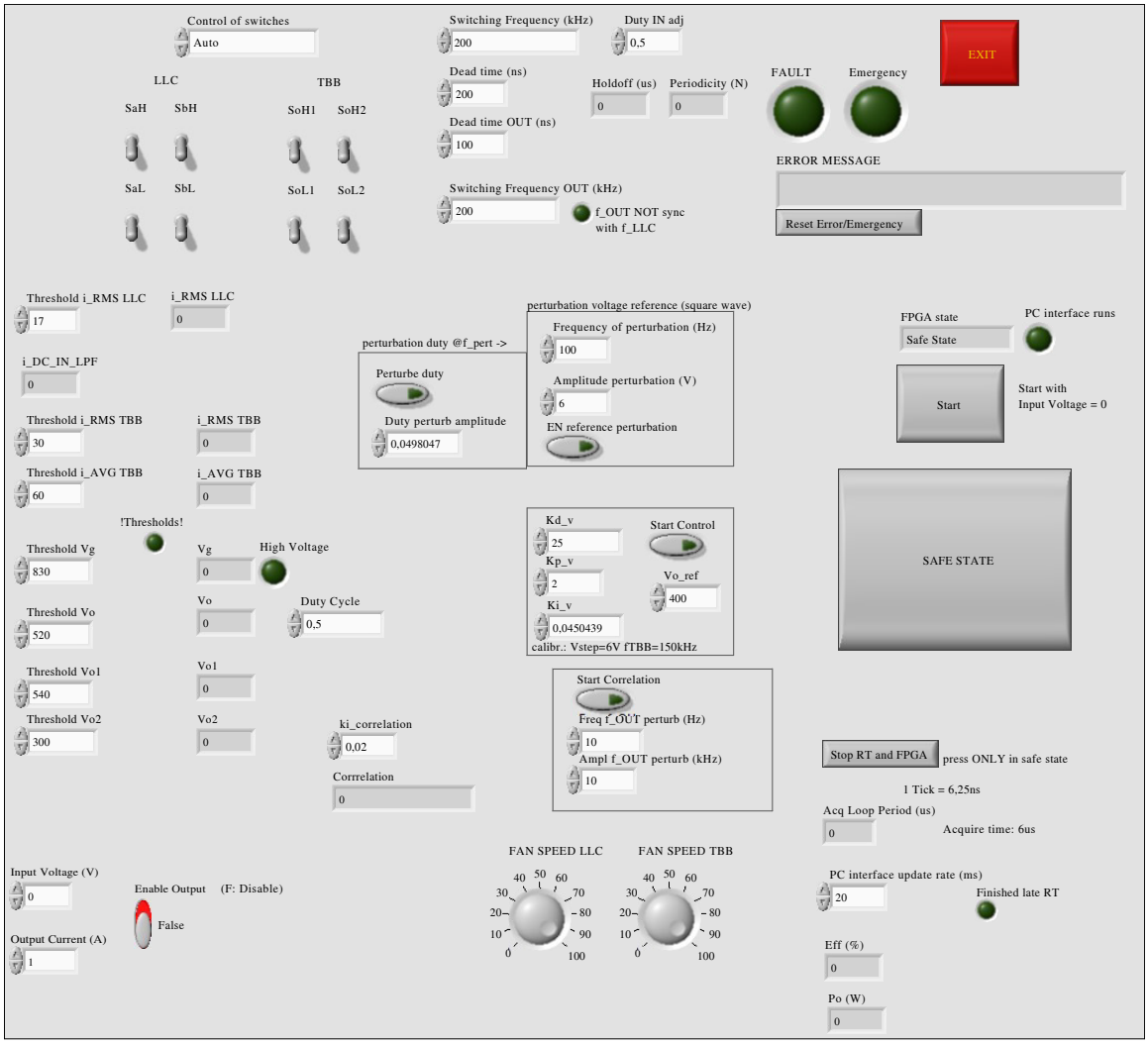


Figure D.10: Control panel on the user's remote computer.

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