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Review and Outlook on GaN and SiC Power Devices: Industrial State-of-the-Art, Applications, and Perspectives

M. Buffolo, *Member, IEEE*, D. Favero, *Graduate Student Member, IEEE*, A. Marcuzzi, *Graduate Student Member, IEEE*, C. De Santi, *Member, IEEE*, G. Meneghesso, *Fellow, IEEE*, E. Zanoni, *Life Fellow, IEEE*, and M. Meneghini, *Senior Member, IEEE*

***Abstract*— We present a comprehensive review and outlook of silicon carbide (SiC) and gallium nitride (GaN) transistors available on the market for current and next-generation power electronics. Material properties and structural differences among GaN and SiC devices are first discussed. Based on the analysis of different commercially available GaN and SiC power transistors, we describe the state-of-the-art of these technologies, highlighting the preferential power conversion topologies and the key characteristics of each technological platform. Current and future fields of application for GaN and SiC devices are also reviewed. The article also reports on the main reliability aspects related to both technologies. For GaN HEMTs, threshold voltage stability, dynamic ON-resistance, and breakdown limitation are described, whereas for SiC MOSFETs the analysis also focuses on gate oxide failure and short-circuit (SC) robustness. Finally, we give an overview on the perspective of such materials in different fields of interest. An indication of possible future improvements and developments for both technologies is drawn. The requirements for hybrid converters, along with a careful optimization of performance and the use of innovative optimization tools, are underlined.**

***Index Terms*— Gallium nitride (GaN), MOSFETs, perspectives, power electronics, reliability, silicon carbide (SiC), transistors, trapping.**

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M. Buffolo, D. Favero, A. Marcuzzi, C. De Santi, G. Meneghesso, and E. Zanoni are with the Department of Information Engineering, University of Padova, 35131 Padua, Italy (e-mail: matteo.buffolo.1@unipd.it; davide.favero.7@phd.unipd.it; alberto.marcuzzi@studenti.unipd.it; carlo.desanti@unipd.it; gauss@dei.unipd.it; zanoni@dei.unipd.it).

M. Meneghini is with the Department of Physics and Astronomy and the Department of Information Engineering, University of Padova, 35131 Padua, Italy (e-mail: matteo.meneghini@unipd.it).

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I. INTRODUCTION

NOWADAYS, the reduction in the dependency on fossil fuels represents a key target to mitigate the climate change. In this context, the efficiency of electric power converters, the use of renewable energies, and the electrification of a wide variety of vehicles and systems are playing a crucial role [1].

Specifically, the increase in the efficiency of power converters represents a way to save energy which otherwise would be lost, thus improving the overall efficiency of systems that are already widely adopted (such as power supplies, heating ventilation and air conditioning systems, etc...). This is a very cost-effective way to save a great amount of energy without investing in new infrastructures. Over the last years, a widespread tendency in electrification has been observed, especially in high-power everyday items, such as vehicles, kitchen appliances, and environmental heating systems, making this efficiency improvement even more urgent [2]. This is even more important in all fields where multiple conversion steps (from ac to dc, from dc to dc, etc.) are present, such as in automotive or photovoltaic systems. The efficiency of power converters can be substantially increased using transistors based on novel materials, having a better performance and reliability compared to the more conventional silicon devices.

A very promising way to tackle this challenge consists in the use of wide bandgap (WBG) semiconductors. Owing to their properties, these materials allow the fabrication of devices for power electronics (transistors, diodes) which outperform, in many scenarios, currently available Si-based ones. The physical properties of the most relevant WBG semiconductors and the comparison with silicon are reported in Table I. WBG materials offer a higher critical electric field if compared to silicon, allowing the realization of power converters operating at higher voltages, while offering at the same time a low

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TABLE I
MAIN MATERIAL PROPERTIES FOR MATURE AND PROMISING, RESEARCH-GRADE, SEMICONDUCTORS FOR POWER ELECTRONICS (ORDERED BY BANDGAP ENERGY, E_G). OTHER REPORTED PARAMETERS ARE: THE CRITICAL ELECTRIC FIELD (E_{crit}), THE ELECTRON MOBILITY (μ_e), THE ELECTRON SATURATION VELOCITY (V_s), AND THE THERMAL CONDUCTIVITY (κ_{th})

Material	E_G (eV)	E_{crit} (MV/cm)	μ_e (cm^2/Vs)	v_s ($\cdot 10^7$ cm/s)	κ_{th} (W/cmK)
Si	1.12	0.3	1440	1	1.3
4H-SiC	3.23	2.5	950	2	3.7
GaN	3.4	3.3	1400	2.4	2.5
β-Ga_2O_3	4.9	8	250	1.1	0.1-0.3
Diamond	5.5	10	4500	2.3	23
AlN	6.2	15	450	1.4	2.85

ON-resistance and a high thermal conductivity. Among the WBG semiconductors of interest, silicon carbide (SiC) and gallium nitride (GaN) offer great performance for the realization of high-voltage switches to be used in power converters (both dc–ac inverters and dc–dc converters), and, most importantly, have the highest level of maturity and industrialization: therefore, several commercial devices are nowadays available and have already been adopted for many applications. Beside SiC and GaN, other WB semiconductors, such as gallium oxide, diamond, and aluminum nitride, are of great interest from a research perspective, but their current maturity level is still preventing industrial investments aimed at a short-term release to the market. Nevertheless, these materials are of major interest for specific applications [3], and working devices have already been demonstrated. In the future, WB semiconductors will be more present in the power electronics market. Owing to the peculiarities of individual materials, we should expect the coexistence of different technologies, each one focused to a particular application.

In this view, this article describes the current properties of the state-of-the-art commercially available SiC and GaN power transistors. In Section II, we draw the current state of market from the discrete devices point of view, by comparing SiC and GaN transistor, mainly in the 650 V range, and by highlighting the key differences between devices built on these two materials and their silicon counterparts. In Section III, we describe the present and future applications for such semiconductor devices. In Section IV, we discuss about the open challenges in the further development of SiC and GaN, and about foreseeable fields of application. Finally, in Section V, we present the perspectives regarding the two materials.

II. COMMERCIALLY AVAILABLE DEVICES

Historically, the first WBG semiconductor that raised interest in power electronics was SiC. This is mainly due to its strong affinity with silicon, which allowed to easily replicate device structures that have already been consolidated. Furthermore, SiC has SiO_2 as native oxide, whose properties and processing technologies had already been deeply investigated from the intense and wide research performed on silicon-based electronics. Consequently, it was possible to rapidly start the development of SiC technology. Ten years after the beginning of the studies on such material in the power electronics field, i.e., around 1990, it was possible to commercialize the first SiC Schottky diode [4]. Since then, the continuous improvement of the technology brought SiC to be available in the market in the voltage range up to 1700 V, for MOSFETs, junction field effect transistors (JFETs) and diodes.

GaN started its history in the light-emitting diodes (LEDs) field, and became of interest for the power electronic field around 1990, as SiC, with the first demonstration of a GaN transistor dating back to 1991 [5], [6]. However, for GaN, there was no prior industrial knowledge, as in the case of SiC, thus raising the necessity of longer time to access and stabilize the technology. The benefits of GaN are exploited by means of the AlGaN/GaN High-Electron-Mobility-Transistor (HEMT): thanks to the presence of a native 2-D Electron Gas (2DEG), this kind of devices allows to realize low ON-resistance and high switching frequency transistors. The first commercially available GaN power FET was introduced in the market Zhong et al. [7], ten years later with respect to the first commercial SiC device. Nowadays, thanks to the continuous effort both at research and industrial levels, it is possible to find in the market GaN HEMTs rated up to 1200 V, though most of the available products have a rate voltage of 650 V or below. To the best of author's knowledge, no discrete GaN power diodes are commercially available at present day.

A. Commercial SiC and GaN Power Transistors

To be commercially available, a power transistor must fulfill three main requirements: 1) being able to sustain high enough voltage and power; 2) feature low switching and conduction losses; and 3) achieve normally-OFF operation. The intrinsic characteristics of WBG semiconductors under analysis make them suitable for the fabrication of devices compatible with first two constraints, even if the structures used to achieve such goal present significant differences between SiC and GaN.

With regard to SiC-based transistors, nowadays, the market offers two different solutions: vertical MOSFETs (either with planar or trench gate) and cascode vertical JFETs. Both structures fulfill the requirement of a normally OFF operation and are shown in Fig. 1(a)–(c), respectively.

GaN, instead, allows to realize the HEMT, as already discussed. However, an AlGaN/GaN HEMT is a normally-ON device, that is not suitable for fail-safe power applications. To achieve normally-OFF operation, two effective techniques are nowadays widely adopted: 1) the use of a p-GaN gate-stack [8], as shown in Fig. 1(d) and 2) the use of a cascode configuration [9], depicted in Fig. 1(e). Nowadays, these are the only two market available e-mode GaN FET topologies, among the many others proposed in literature [10].

The main advantages and disadvantages of these GaN and SiC topologies will be discussed in Section II-C.

B. Typical Voltage Ranges of Application

At present, SiC exploits high-voltage-oriented power transistors, covering several voltage classes: 650, 900, 1000, 1200,

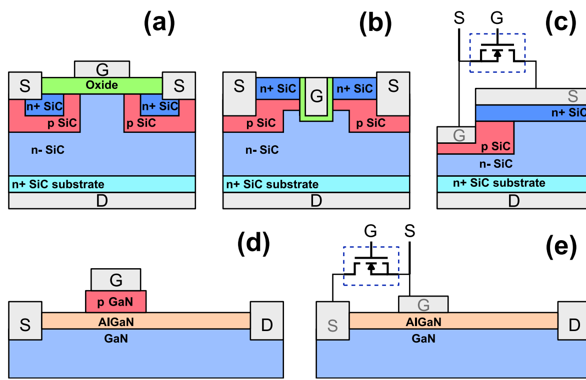

Fig. 1. Schematic representation of the different semiconductor structures used in commercial SiC and GaN power transistors. (a) SiC vertical planar-gate depletion MOSFET. (b) SiC vertical double trench MOSFET. (c) SiC vertical cascode JFET. (d) GaN p-GaN gate HEMT. (e) GaN cascode HEMT.

and 1700 V. Furthermore, vendors also offer the possibility of purchasing transistors with integrated gate driver (silicon driver in the same package) and complete power modules with temperature sensing.

GaN, instead, is covering a wide voltage range, from 15 to 1200 V. However, as far as high supply voltages are concerned, the diffusion of GaN-based devices is almost entirely limited to the 650 V range, since the market offers only one solution from one vendor for the 900 V and one solution for 1200 V class: above 900 V, SiC-based transistors still represent the preferential choice for the design of power conversion circuits. As for SiC, vendors also offer transistor with integrated gate drivers, as well as complete power modules. In addition, GaN vendors offer the possibility to purchase transistors with monolithically integrated drivers, which is of key importance [11], [12], [13]: 1) for the reduction of the gate-loop inductance (to minimize the gate stress during turn-on); 2) for the mitigation of the common-source inductance (to achieve higher slew rates); and 3) to allow the design of highly effective thermal and current protection circuits.

C. SiC and GaN Transistors in the 600/650 V Range

To get further insight and to provide a better understanding of the differences among the commercially available solutions, we decided to compare SiC and GaN discrete transistors in the 650 V range, together with some higher voltage rated products for a more complete analysis. Table II reports the main parameters of interest extracted from the datasheets of the compared devices, which were selected from different manufactures (not exhaustive list). The selection is based on the continuous drain maximum current capabilities (between 30 and 50 A) and on the typical ON-resistance value (around 50 mΩ), to allow a fair comparison.

Concerning the 650 V range, different SiC FETs, GaN FETs, and one Si MOSFET are compared. $R_{ON} \times Q_G$ figure of merit (FOM) represents a widely diffused metric for evaluating FETs efficiency, since it accounts for both conduction and switching losses. Design-wise, it is hard to reduce both ON-resistance and total gate charge at the same time, making

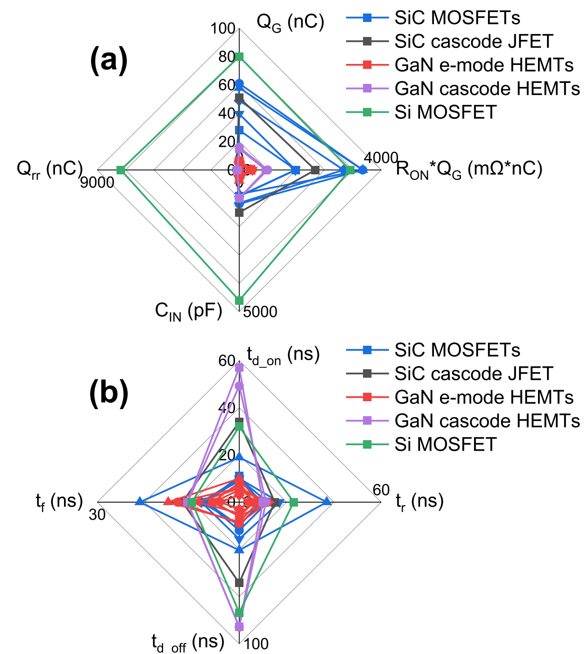

Fig. 2. Radar plots for comparison of the 650 V-rated SiC, GaN, and Si devices reported in Table II. (a) Radar plot reporting the total gate charge, the $R_{ON} \times Q_G$ FOM, the input capacitance, and the reverse recovery charge. (b) Radar plot reporting the turn-on and -off delay times and rise and fall time.

this FOM a good basis for comparison (although it cannot be the only one to rely on). Among all, GaN e-mode HEMTs show the lower $R_{ON} \times Q_G$ values, with improvements of at least a factor of four over the competitors based on other semiconductor technologies (from $R_{ON} \times Q_G > 1500$ mΩ·nC of SiC and Si devices to $R_{ON} \times Q_G > 300$ mΩ · nC). The improvement is limited to a factor of two if cascode GaN HEMTs are considered. From a dynamic standpoint, the input capacitance C_{IN} is much lower in GaN e-mode transistors (in the 200 pF range) while it is higher in GaN cascode HEMTs (due to the silicon MOSFET used to drive the normally-ON device) and in SiC transistors (above 900 pF). Silicon power MOSFETs have instead an even higher input capacitance (above thousands of pF). Furthermore, it must be noted that the reverse recovery charge is null for GaN e-mode HEMTs (due to the absence of the classical MOSFET body diode), is in the 100 nC order for SiC and GaN cascode HEMTs, whereas it is in the thousands of nC range for Si MOSFETs. A high reverse recovery charge can induce a drop in the efficiency of a converter and can cause voltage and/or current spikes during operation, indicating that a low value is desirable. A graphical comparison of the above cited parameters is reported in Fig. 2(a) by means of a radar plot, which highlights the better performance of the GaN HEMTs.

Other important parameters in the comparison of power transistors are the turn-on delay time ($t_{\text{d-on}}$), rise time (t_r), turn-off delay time ($t_{\text{d-off}}$), and fall time (t_f). They describe the capability of a transistor to be turned-on and -off in a fast way. From this point of view, the differences between the different technologies here analyzed are less prominent, though the radar plot reported in Fig. 2(b) shows that GaN

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TABLE II

Comparison of Selected Commercially-Available SiC and GaN Power Transistors in the 600/650 V Voltage Range From Different Well-Established Vendors, Sharing a Maximum Drain Current in the 30–50 A Range and Typical on-Resistance Value Around 50 mΩ. 650 and 900 V Si MOSFET are Added for Comparison, Together With SiC and GaN Devices Rated at Higher Voltages (900 and 1200 V). The Table Reports the Following Parameters: the Material, the Vendor, the Part Number, the Normally off structure Type (N-off Type), the Rated Drain-Source Voltage (V_{DS}), the Typical On-Resistance (R_{ON}), the Maximum Drain Current ($I_{D\text{-}max}$), the Total Gate Charge (Q_G), the R_{ON} Q_G FOM, the Total Input Capacitance (C_{IN}), the turn-on Delay Time ($t_{D\text{-}on}$) the Rise Time (t_r), the turn-off Delay Time ($t_{D\text{-}off}$), the Fall Time (t_f), and the Reverse Recovery Charge (Q_{rr}). This Table is Not Supposed to Represent an Exhaustive List of Commercially Available Transistors

Material	Vendor	N-OFF type	V_{DS} (V)	R_{ON} (mΩ)	$I_{D\text{-}max}$ (A)	Q_G (nC)	R_{ON}*Q_G (mΩ*nC)	C_{IN} (pF)	$t_{d\text{-}on}$ (ns)	t_r (ns)	$t_{d\text{-}off}$ (ns)	t_f (ns)	Q_{rr} (nC)
SiC	Infineon (IMZA65R057M1H)	M1 Trench MOSFET	650	57	35	28	1596	930	11	9	16.8	7	113
SiC	Onsemi (NVH4L075N065SC1)	MOSFET	650	57	38	61	3477	1200	10	12	20	7	72
SiC	Qorvo/UnitedSIC (UF3C065040B3)	Cascode	650	42	41	51	2142	1500	34	15	57	12	138
SiC	Rohm (SCT3060ALHR)	Trench MOSFET	650	60	39	58	3480	852	19	37	34	21	55
SiC	STMicro (SCT040HU65G3)	MOSFET, 3rd Gen	650	40	30	39.5	1580	920	10	17	26	8	97
SiC	Wolfspeed (E3M0060065K)	MOSFET, 3rd Gen	650	60	37	49	2940	1170	9	10	16	8	173
GaN	GaN-Systems (GS0650302L)	e-mode	650	50	30	6.7	335	235	8.2	6.3	10	5.7	0
GaN	GaNPower (GPI65030DFN)	e-mode	650	55	30	5.8	319	241	6	12	15	13	0
GaN	Infineon (IGLD60R070D1)	e-mode	600	55	15	5.8	319	380	10	8	14	15	0
GaN	Innoscience (INN650D080BS)	e-mode	650	60	29	6.2	372	225	3	4	5	4	0
GaN	Nexperia (GAN063650WSA)	Cascode	650	50	34.5	15	750	1000	57	10	88	11	125
GaN	Nexperia (GAN080650EBE)	e-mode	650	60	29	6.2	372	225	3	4	5	4	0
GaN	Rohm (GNP1070TCZ)	e-mode	650	70	20	5.2	364	200	5.9	6.9	8	8.7	0
GaN	STMicro (SGT65R65AL)	e-mode	650	49	25	5.4	264.6	286	5.2	12.5	10	5.3	0
GaN	Transphorm (TP65H050G4WS)	Cascode	650	50	34	16	800	1000	49.2	11.3	88.3	10.9	120
GaN	CGD (CGD65A055S2)	e-mode, with gate driver	650	55	27	6	330	N.A.	7	7	23	7	0
GaN	Navitas (NV6128)	with monolithic gate driver	650	70	20	N.A.	N.A.	N.A.	15	10	15	5	0
GaN	Texas Instruments (LMG3522R050)	With gate driver	650	43	44	N.A.	N.A.	N.A.	37	2.5	44	15	N.A.
Si	STMicro (STP65N045M9)	MOSFET	650	39	55	80	3120	4610	32	23	78	10	7500
SiC	Onsemi (NTHL060N090SC1)	MOSFET	900	60	46	87	5220	1770	22	33	31	11	84
SiC	STMicro (SCT040W120G3-4AG)	MOSFET, 3rd Gen	1200	40	40	56	2240	1329	12	6	34	22	100
GaN	Transphorm (TP90H050WS)	Cascode	900	50	34	15	750	1000	48	12	70	12	156
GaN	GaNPower (GPIHV30SB5L)	e-mode	1200	60	30	8.25	495	236	19	20	17	40	0
Si	Infineon (IPW90R120C3)	MOSFET	900	120	36	270	32400	6800	70	20	400	25	30000

e-mode HEMTs exhibit better performance, on average. GaN cascode HEMTs, on the other hand, show slower turn-on/-off capabilities, due to the presence of the silicon MOSFETs, if compared to GaN e-mode devices, while showing comparable performance if compared to SiC and Si power transistors. GaN power e-mode FETs can be preferable if turn-on/-off times are the metric of reference.

Higher voltage ranges are of great interests for the future of power electronics in different fields (as will be further discussed in Section III), therefore a brief comparison between devices rated for such operating regimes is worthwhile. Since at present GaN is available up to 1200 V, we compared GaN and SiC in the 900 and 1200 V range (beside the 650 V one) with the same radar plots employed in Fig. 2 for the comparison in the 650 V market segment. For this new comparison in the higher voltage segments, summarized by Fig. 3, one device per voltage range and per semiconductor technology is included. The 900 V silicon MOSFET of Table II is anyhow excluded, since its performance are not anywhere comparable with all the other products.

The radar plots of Fig. 3 highlights again the better dynamic performance of GaN transistor, even for these higher voltage ranges, confirming what previously stated for the 650 V range. Despite that, it must be highlighted that at present the performance and reliability of higher voltage GaN transistors are still under optimization (this topic will be further discussed in Section IV). Moreover, it is worth reminding that in the 900–1200 V voltage range only two GaN-based solutions are offered to the market, whereas SiC MOSFETs easily achieve 1700 V operation, with tens of choices available from many different reputable vendors.

From a cost standpoint, the differences in price of comparable discrete devices based on the two materials are limited. If we compare selling prices of 650 V devices in Table II, as of August 2023, Si-based devices are the cheapest. Price will increase of 30% for a GaN discrete transistor and of 50% for a SiC discrete transistor, while remaining below U.S. $18. For higher voltage devices, costs are more uniform, with Si devices leveling their price with SiC and GaN increasing in price of 20% (respect 650 V range). This suggests that the choice between either of the two technologies will have a limited effect on the bill-of-materials (BOMs) of a converter. However, the reasoning on the overall cost changes if we consider that some devices allow converters to be operated

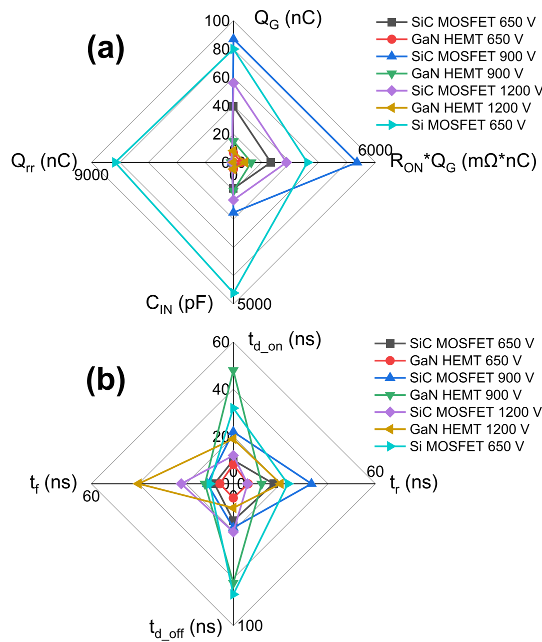

Fig. 3. Radar plots for comparison of the 650, 900, and 1200 V-rated SiC, GaN, and Si devices reported in Table II (900 V Si MOSFET presented in Table II is excluded due to its too poor performance). (a) Radar plot reporting the total gate charge, the $R_{ON} \times Q_G$ FOM, the input capacitance, and the reverse recovery charge. (b) Radar plot reporting the turn-on and -off delay times and rise and fall time.

at higher frequency, thus requiring less bulky and expensive passive components.

As general remark, the radar plots reported above help understand why in the high-voltage and high-power segments, power electronics is moving to the WBG semiconductors such as SiC or GaN.

Besides individual transistors, modules including several devices are also commercialized. These modules are designed to strongly reduce the detrimental effects of parasitic elements, which can strongly limit the performance during high-frequency operation, and to improve thermal management, ultimately allowing high-voltage and current operation at greater power densities. Those modules can contain transistors (and diodes in case of SiC) in various possible configurations, like half bridge or full bridge, to easily allow the implementation of different power converter topologies when paired with specific external components.

III. Applications

Compared to Si-based devices, SiC and GaN power transistors are smaller (reduced die area), owing to the higher breakdown field (>3 mV/cm), and can sustain higher temperatures, thanks to the wider energy bandgap. Conduction losses are also reduced, due to the lower R_{ON}, thus helping to increase the overall efficiency achievable by the power converter, which will ultimately require smaller heatsinks and cooling systems. From a dynamic point of view, a reduced input capacitance and gate charge helps ease device driving and allows for higher frequency and lower losses operation. SiC and GaN also expand the power region (and frequency) of operation of Si MOSFETs, IGBTs, and Superjunction Si MOSFETs, as reported in Fig. 4.

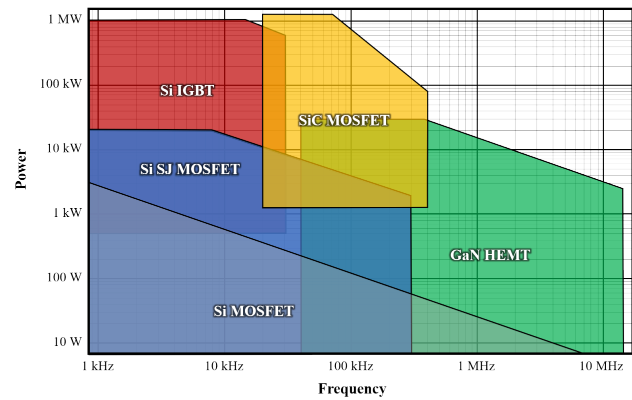

Fig. 4. Frequency and power regimes for different power device technologies. Note that SiC and GaN devices work at substantially higher frequencies and powers with respect to Si-based devices. Data based on [14].

The efficiency and miniaturization levels achievable through the adoption of SiC and GaN devices favor the development of highly efficient dc–ac and dc–dc converters, allowing to reduce the weight and volume of the electronic components, which is of great interest for battery-operated applications such as EVs, and to increase power density [10].

A. Current Applications

Although SiC- and GaN-based transistors offer several advantages from many points of views, they are not widely adopted in all the fields that would benefit from their properties. At present, such devices are playing a significant role in two different sectors. SiC-based devices are widely adopted in hybrid and electric vehicles traction inverters (Tesla uses SiC transistors since 2017 [15]), while they can also be found in lower volumes in on-board-chargers (OBCs) and traction inverters of hypercars and racing cars. SiC transistors are therefore mainly targeted at the automotive market, at present.

GaN, on the other hand, is commonly employed in the realization of power supplies and chargers for smartphones and PCs, since the higher achievable switching frequency enables higher power chargers with three time lower volume with respect to conventional Si-based ac–dc converters. GaN-based transistors can also be found lower volumes in high-end PV inverters, indicating that at present GaN power devices are more oriented towards consumer electronics.

B. Future Applications

Owing to the continuous reduction in cost and increase in maximum operating voltage, additional fields are going to benefit from the peculiar properties of SiC and GaN in the future. In particular, transistors based on the two aforementioned WBG materials are expected to further enter into sectors that are now led by silicon devices, such as MOSFETs, insulated-gate bipolar transistors (IGBTs), gate turn-off (GTOs), and silicon-controlled rectifiers. The specific field of application of either of the two technologies will of course depend on the target voltage level, as depicted in Fig. 5.

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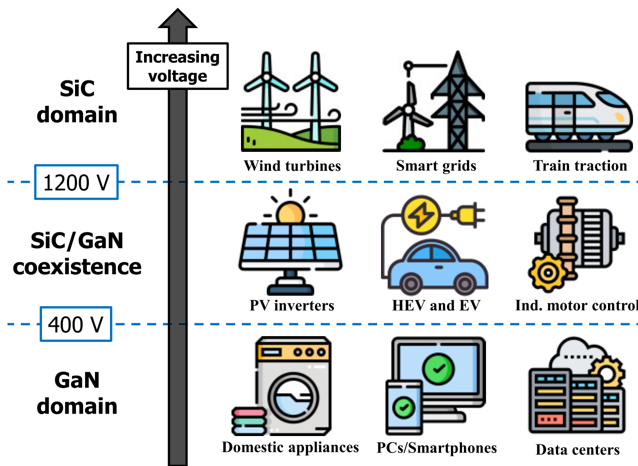

Fig. 5. Current and future fields of interest for GaN and SiC power devices. Figures partially reused from www.flaticon.com.

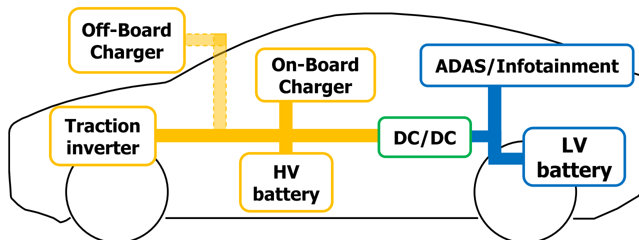

Fig. 6. Main electric and electronic building blocks of a hybrid/electric vehicle.

1) Below 400 V, GaN is expected to dominate the market. This range corresponds to the maximum household power supply voltage, considering both single-phase and three-phase systems, and involves all domestic appliances, consumer electronics (smartphones, PCs, and their chargers), and power electronics in datacenters.
2) Between 400 and 1200 V, SiC and GaN are expected to cooperate and coexist, depending on the power level handled in each application. In this voltage range, it is possible to find inverters used for renewable resources, controls for industrial motors and several applications in the automotive segment. The latter is of great interest for both semiconductors, due to the increasing interest and demand for car electrification. Inside a hybrid and/or electric vehicle, different electrical apparatuses exploit power converters, and therefore power transistors (see Fig. 6). Achieving high efficiency, low sizes and low weights of power electronics components are of key importance for the extension of vehicle range, increase in comfort and vehicle performance.
3) Above 1200 V, SiC is expected to play a fundamental role for electric train traction, wind turbines applications and smart grids. Electric train traction, at present, is extremely interesting for SiC, since the voltages of interest are in the kV range (up to 5 kV for regular trains), where SiC is almost ready to substitute silicon devices (mainly GTOs and IGBTs) and bring improved performance and efficiency. In addition to that, SiC will also play a role for systems running at even higher voltages, such as high-speed trains, which can require up to 25 kV.

C. Circuit Topologies

For current applications, different circuit topologies can be employed, depending on the voltage, power, and switching frequency requirements.

For GaN we start considering the case of USB-C adapters, the fastest adopter in the market of GaN-on-Si products [16]. Power levels can go from 33 to 250 W [16]. If we consider applications with loads lower than 70 W, where no power factor correction (PFC) is needed, the most common topology is the quasi-resonant flyback, followed by active-clamp flyback. GaN devices can reach very high frequencies, but, in these cases, they are limited to 300 kHz to avoid electromagnetic interference (EMI) issues. For higher power applications, multistage topologies are adopted, due to the need for a PFC Boost stage as frontend. The topologies of the following stages are the same describe above, but also include bridge topologies. Si-based stages can be present too, when multiple output voltages are required: in this case Si-based switches are used for the last stages responsible for dc–dc conversion. Finally, in this context, GaN-based design allows to achieve greater power densities, in the order of 1.5–1.9 W/cm^3 [17], the result at 2015 Google LittleBox Challenge, with 8.7 W/cm^3 [18]. However, care must be taken in the design of clamping circuits, better if active, and in voltage stress considerations, to provide the proper headroom and avoid drain-to-source breakdown in GaN devices.

Handling of higher powers (>250 W) is still possible with GaN, but in this case soft-switching or zero-voltage-switching (ZVS) topologies are preferred. Specifically, resonant LLC topologies are considered. In a half-bridge configuration, the use of GaN devices allows for higher frequencies and efficiencies. As already stated in Section II-C, GaN devices show a reduced gate charge, output capacitance, and reverse recovery time and charge leading to lower driving losses, switching losses, and reverse recovery losses, respectively. Moreover, GaN devices enable the possibility for a diode-free H-Bridge configuration, having reverse conduction capabilities [16]. Those are achieved also with IGBTs with a parallel diode, or using the internal body diode of Si MOSFETs, but the GaN solution is more efficient, since it features a much lower $Q_{\rm rr}$.

SiC devices are used in high-power applications and are already available in modules implementing Bridge (or Chopper for train traction) topologies. Those devices and modules are often used in inverters for high-power handling. In the PV inverter case, in particular, different topologies are considered, starting from the two-level, six-pack basic topology to more advanced three-level ones. The best choice for both efficiency and part count is the T-type neutral point clamped topology [19].

SiC transistors are also considered in high-power, transformer-free designs in the MW range: for example, they are employed in train traction systems to adapt the low-frequency ac catenary voltage to the higher frequency ac voltage required to drive the motors. This is achieved by properly cascading ac–dc, dc–dc, and dc–ac converters, using

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for example resonant LLC conversion topologies for the dc–dc part, like the 2 MW one described in [20].

The benefits of SiC can also be exploited by including SiC diodes into conventional converters. By leveraging their smaller size, fast reverse recovery, and high temperature tolerance, a hybrid design can be successfully implemented [21].

IV. Current Technological Challenges

We have seen in previous sections how SiC and GaN power devices can be adopted in a growing number of use cases, where their peculiar properties are exploited. However, as done by both academic and industrial world, a continuous research and development process is strongly required not only to improve device performance, but also their reliability. To this aim, the challenges that need to be tackled are generally different when comparing SiC and GaN devices, due to the different maturity level of the two material technologies and to the unique device structures typically adopted, as seen in Fig. 1. Specifically, attention should be drawn to the differences in how carriers are introduced and confined within the channel. For instance, the presence of an oxide in the SiC-based MOSFET structures helps reduce gate-related leakage, thus improving the confinement, but it also leads to a different charge trapping scenario with respect to the physical processes typically occurring in correspondence of the gate-stack of a GaN HEMT. Furthermore, the classic structure and doping scheme of conventional Si-based MOSFETs is not found in GaN HEMTs, where the channel is formed as a consequence of the polarization properties of GaN: this influences the response of GaN devices in specific stress scenarios as well.

The key technological challenges for the improvement of the reliability of both GaN and SiC transistors will be briefly reviewed in the following sections.

A. Threshold Voltage Shift in GaN and SiC Transistors

A crucial challenge in the development of power transistors, regardless of the material, is represented by the mitigation of undesired threshold-voltage (V_{th}) shifts, either positive or negative, occurring during operation. For example, considering a normally-OFF device, a positive V_{th} shift degrades overall device performance, since it leads to a reduced overdrive voltage. This increases the ON-resistance and can possibly trigger a premature turn-off of the device. Negative V_{th} shifts, on the other hand, may lead to even worse scenarios in which device control is partially lost, either due to false turn-on events or to the inhibition of the OFF-state. In a switching converter, such possibilities constitute a serious hazard, since they can induce the formation of short circuits (SCs) between different supply lines, eventually leading to the catastrophic failure of the system or to unsafe operating conditions.

For silicon devices, such problems have long been controlled and this maturity is testified by the robustness of cascode configurations to V_{th} shifts, in which the WBG device is controlled by a conventional Si-based one. For other types of transistors based on WBG materials, however, the issue is present and needs to be tackled. The typical methodology, or accelerated stress condition, to investigate V_{th} shifts is bias

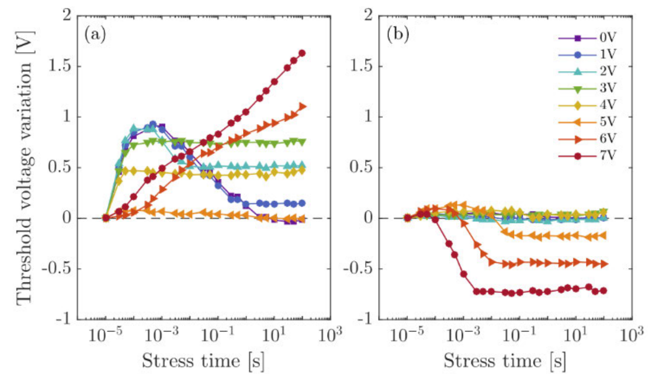

Fig. 7. (a) Positive and (b) negative threshold voltage shift induced by different mechanisms of electron and hole trapping in a p-GaN gate HEMT gate-stack. The curves are obtained after referring to the initial threshold voltage value at $t = 10$ μs. Reprinted with permission from A. Stockman et al., © 2021 IEEE [22].

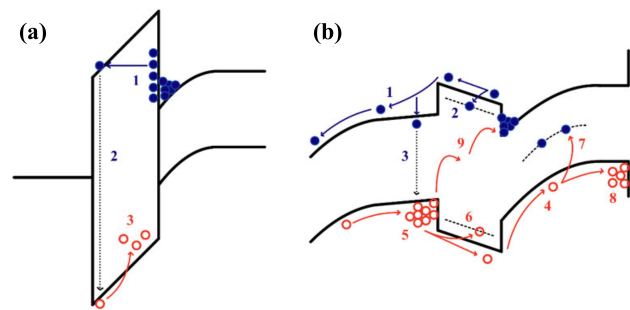

Fig. 8. Trapping mechanisms in the gate-stack of SiC (a) and GaN (b) power transistors, leading to V_{th} Shift. Note the different confinement of carriers in the channel. In SIC MOSFETs, the main mechanisms involved are: electron trapping at interface and border traps between SiC and SiO_2 (1a), hole trapping in the oxide (3a) [holes are generated through impact ionization events (2a)]. In e-mode HEMTs, the main mechanisms are: electron trapping at the AlGaN/GaN interface and in AlGaN traps (2b), hole accumulation at the p-GaN/AlGaN interface (5b) and consequent hole trapping in the AlGaN (6b), electrons and holes overcoming the AlGaN barrier (1b and 4b respectively), hole trapping in the buffer (7a) and at the interface between buffer and the strain relief layers (8a).

temperature instability (BTI), or the application of a positive (PBTI) or negative (NBTI) bias at various temperatures at the gate terminal. In the GaN world, for non-optimized e-mode HEMTs, different mechanisms can lead to both positive and negative V_{th} shifts under positive bias stress [22], as can be seen in Fig. 7.

With variations and optimizations in the gate-stack process, the different mechanisms can be balanced, enhancing or reducing electrons or holes trapping to balance positive and negative V_{th} shifts, thus leading to a stable V_{th}. V_{th} shifts are in fact caused by trapping phenomena assisted by the presence of defects located at interfaces and within different regions of the devices [23] (see Fig. 8): improvements in interfaces and material quality are therefore of primary importance to mitigate these kinds of processes [24], [25], [26].

As can be found in the literature, V_{th} instabilities can also arise from OFF-state operation. A high-drain bias can in fact induce a V_{th} shift, like the positive one found by Chen et al. [27] (up to 1 V with $V_D = 200$ V): this kind of drain-induced V_{th} shift is not widely studied and well understood, thus being an open point for future investigations.

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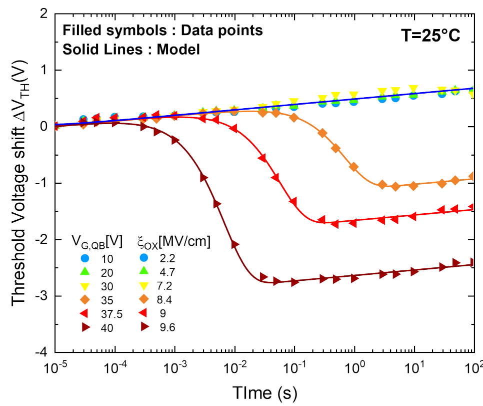

Fig. 9. Non-monotonic threshold voltage shift visible in 4H-SiC n-MOSFETs during a positive bias stress at room temperature. Reprinted from F. Masin et al., with the permission of AIP Publishing [30].

As far as trapping in proximity of the gate dielectric is concerned, SiC-based MOSFETs are advantaged, since its native oxide, stable at room temperature, is the well-known SiO_2, which has been used for decades in Si-based electronics.

The extensive studies performed on SiO_2 created a solid background for SiC MOSFETs development. Despite that, interface quality between SiC-SiO_2 is lower with respect to the one between Si-SiO_2, thus leading to more defects, more trapping, and thus bigger V_{th} variation during operation.

For 4H-SiC MOSFETs submitted to PBTI, multiple observations of a positive shift are found in literature [28], both linear and superlinear with the logarithm of stress time. The magnitude of the shift is much lower than what is observed for GaN, but becomes considerable (1–5 V) for high voltages and high temperatures. This shift is generally ascribed to electrons tunneling to near-interfacial-oxide-traps.

Other reports [29], [30], [31] show the presence of two phases in the dynamics of the shift, as shown in Fig. 9, which can be ascribed to the competition of two distinct trapping processes.

1) An initial positive shift, with a logarithmic time dependence, generally associated with trapping at the interface and described using the inhibition model.
2) A negative shift, ascribed to the generation of holes via impact-ionization within the oxide, as in Fig. 9. The time dependence observed here is exponential.

B. Dynamic On-Resistance Increase in GaN Devices

One of the most important challenges for cascode and e-mode GaN HEMTs is the recoverable increase in their ON-resistance (R_{ON}) under an OFF-state or semi-on state bias.

This is important for power transistors, since during OFF-state operation the transistor is subjected to very high drain voltages that can lead to the injection of electrons into surface states [32] and/or in buffer traps [33]. Those phenomena lead to an overall decrease in the conductivity of the channel, and therefore to an increase in R_{ON} when the device is operated at different drain bias levels, ON-resistance instability can occur due to the interplay of the electron trapping (in surface and/or buffer states) and other mechanisms, like the generation of positive charge (i.e., holes generated by the transfer of electrons from the buffer to the channel) during drain stress [34]. On-resistance increase is further enhanced during semi-on state, which represents an operating point crossed by the device during switching.

One approach to suppress the ON-resistance increase is the use of a hybrid-drain (HD) [35], where a p-GaN layer is embedded in the drain contact to inject holes during OFF-state and semi-on state operation. This allows to counteract the electron trapping, thus preserving the ON-resistance. The effectiveness of this approach has been explored by Fabris et al. [36], by carrying out a set of experiments that highlighted the ON-resistance behavior for different drain quiescent biases (QBs) in OFF-state and semi-on state operation.

C. Breakdown Mechanisms in GaN Transistors

During switching operation in a power converter, different breakdown mechanisms may take place and lead to the catastrophic failure of the solid-state switches. In general, GaN FETs must be optimized considering all breakdown mechanisms, for further technology development and increase of rated voltage and lifetime.

From the gate standpoint, considering ON-state operation, breakdown mechanisms differ between cascode and e-mode GaN FETs. In the first case, the gate corresponds effectively to the one of a Si MOSFET, which can suffer from the well-known time-dependent-dielectric-breakdown (TDDB) [37]. In the e-mode GaN FET case, there is still time-dependent degradation and breakdown due to positive bias exposure, even without any dielectric in the gate-stack [38].

Drain-to-substrate breakdown is usually present, in GaN-on-Si devices, for voltages well above the rating, not uncommonly above 1000 V [39]. However, in high voltage GaN FETs fabrication, this type of breakdown must be considered and optimized [38]. Ways to improve device robustness against this phenomenon is local substrate removal [39] or, at lower cost, the use of sapphire substrate instead of a silicon one, as demonstrated by Gupta et al. [40] with a 1200 V GaN switch.

As a final remark, a hot topic in HEMTs breakdown is related to avalanche. GaN HEMTs have much lower impact ionization coefficients with respect to Si and SiC MOSFETs; therefore, their avalanche behavior is different. Nevertheless, they are capable to sustain voltages far above their ratings, resulting in a dynamic breakdown voltage behavior (i.e., breakdown voltage depends on OFF-state pulse duration) [41], [42]. These devices also demonstrate excellent surge capabilities [43]. Such capabilities, however, need be investigated to quantify the robustness of the transistors towards the voltage overstress events that can occur during switching transients.

D. Other Challenges in GaN Transistors

Owing to the relatively early development phase [44], other factors are currently under study, such as SC and surge energy capabilities. GaN transistors, both e-mode and cascode types, when submitted to SC testing, may show different degradation and/or failure mechanisms. Surge energy in GaN HEMTs is strictly related to overvoltage robustness, and devices do

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not show avalanche capability. For Si and SiC transistors, instead, devices surge energy is generally related to avalanche energy [47]. In general, GaN HEMTs are designed with a sufficiently high dynamic breakdown voltage to sustain overvoltage transients. A comprehensive review of surge and SC mechanisms can be found in [44].

E. Gate Oxide Failure in SiC MOSFETs

A critical reliability aspect for SiC MOSFETs is represented by the breakdown of the gate oxide. There are two physical interpretations for such kind of failure [48]. The first one, which is field-driven, consists in the weakening of chemical bonds under the effect of an external field. The second one, on the other hand, is related to the flow of charge through the tunneling, which is eased with respect to Si MOSFETs due to the reduced band offset between SiO_2 and SiC. Specifically, we find Fowler–Nordheim tunneling at high field, low temperature and thermally assisted tunneling at low field, high temperature [49]. When testing device robustness against gate oxide failures, the main FOM is represented by the time-to-failure (TTF), which is then used to compute the expected lifetime of the gate dielectric under specific operating scenarios. A widely adopted method is the application of a constant stress voltage to the gate, monitoring the current until breakdown occurs [37]. This approach allows to evaluate TDDB phenomena, and therefore test times can be very long. Since lifetime scales with temperature and voltage, shortening of test times can be effectively achieved by increasing test temperature and voltage, then extrapolating data at the target operating condition of the device [29].

The existence of a failure mechanism related to the tunneling current was found to be compatible with another evaluation method, charge-to-breakdown, which relies on the evaluation of the total charge flown through the gate-stack before reaching device breakdown [49]. In this case, a constant-current stress is applied to the gate and the charge-to-breakdown is then defined as the integral of the current until breakdown time [48], or the stress current multiplied by the time-to-breakdown.

In some cases, charge-to-breakdown can lead to an overestimation of oxide lifetime [48], but this problem is present also in the TDDB-based approach, where whole generation and trapping at high fields can lead to a premature failure, and therefore to overestimation of the lifetime at low fields [48]. Also, electron trapping during tests can relax the field on the oxide, further contributing to the aforementioned overestimation [50]. Recommendations aimed at avoiding excessive trapping that can lead to overestimations are to keep the stress field under a specific threshold, under 8.5 mV/cm according to Liu et al. [29] and under 7 mV/cm according to Zheng et al. [31].

Oxide reliability can also be described by means of a safe operating area for gate dielectrics [51], which represents the stress-field-temperature space in which device performance remains within datasheet specification, accounting for oxide degradation prior to breakdown.

Gate oxide failure is an important reliability concern. For this reason, methods to detect early failures in manufactured

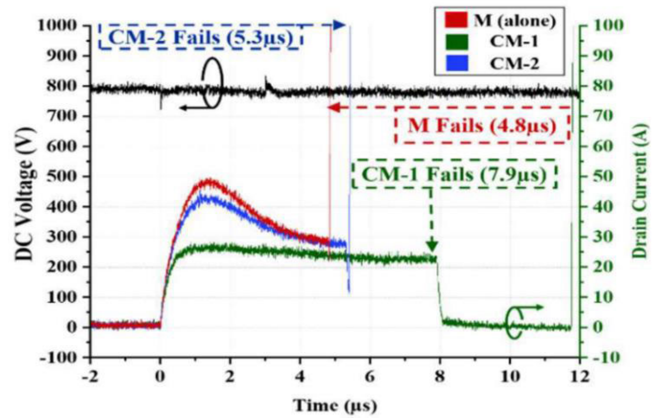

Fig. 10. Comparison between short-circuit waveforms of devices with and without a MOSFET connected as source resistance. A reduced current peak and average value can be observed in CM1 and CM2 waveforms. Reprinted with permission from A. Kanale and B. J. Baliga, © 2019 IEEE [57].

devices are strongly needed. For instance, Zheng et al. [31] proposed a voltage ramp at relatively high voltages, whereas Miki et al. [52] proposed the use of repeated V_{th} measurements, to exclude transient instabilities.

As a reference, in the automotive industry the standard oxide lifetime is in the 10^8 s range. In 2020, $t_{63\%}$ (the time at which 63% of devices failed) was found to be larger than 10^6 s at 150 °C [50]. In 2021, another study found a $t_{63\%} > 10^8$ s at 150 °C for all vendors tested [29], proving the robustness of SiC MOSFETs technology.

F. SC Robustness of SiC MOSFETs

SC robustness testing is another way to evaluate devices ruggedness, in harsh conditions that can present in real-world scenarios.

The robustness of a power device can be tested also using hard switching events at very high drain voltages, with turn-on pulses of various lengths [53]. In this view, relevant parameters to estimate are the short-circuit withstand time τ_{SC} and critical energy E_C stored in the device. Evaluation of voltage and current waveforms (see Fig. 10) leads also to the formulation of a Short-Circuit Safe-Operating-Area (SCSOA) [54].

SiC MOSFETs are meant to replace Si IGBTs, whose τ_{SC} is around 10μs. Since 2013, this mark has been reached [55], but not in a systematic way. To improve performance, the addition of a source resistance to the stressed device proved to be beneficial, if properly tuned to not affect ON-state and switching performance. Less current goes through the device, as a consequence of reduced overdrive voltage, but the initial current peak is unchanged. Such resistance can also be integrated within the device itself, as shown in [56].

More advanced mitigation techniques involve the addition of Si MOSFETs in place of the source resistance. This approach, the Baliga short-circuit improvement concept (BaSIC), improves device performance with respect to the single-source resistance approach [57], [58].

Finally, as far as short-circuit performance are concerned, trench-like structures appear to be disadvantaged with respect to planar DMOSFETs [59].

V. Perspectives

At present time, SiC and GaN devices are both at an advanced development stage. Both find commercial applications and are praised for the improvements in efficiency, robustness and power density they allow to achieve with respect to their silicon counterparts. In the future, research is expected to continue for both materials to solve the open issues, improve reliability, and further enhance their advantages.

Based on the considerations reported in the previous sections, it would be incorrect to think of a single material as the best choice for power devices, as happened with silicon for the integrated circuits industry. In fact, GaN and SiC have unique individual properties, and each can bring improvements to specific applications. For instance, SiC allows to fabricate very robust devices than enable high power switching converters. On the other hand, GaN HEMTs boast speed and superb efficiency, which are crucial to increase the power/volume ratio of low- to medium-power converters.

What we should expect from GaN in the future is the possibility to reach higher voltages, even above 1200 V. To reach this goal, innovative semiconductor structures, such as vertical GaN transistors, and suitable cost-effective substrates will be required. At present, vertical GaN transistors have not reached a maturity level suitable for wide commercialization. However, the future availability of such devices, including finFETs, MOSFETs, and JFETs, is expected to unlock the possibility to reach lower ON-resistance values with respect to their SiC counterparts, while achieving avalanche and short-circuit robustness.

For SiC, having simple structures capable of outstanding performance, that also benefit from all the cumulated knowledge of SiO_2 matured with Si-based electronics, is a very important advantage. This allows an effective control of trapping phenomena, V_{th} stability, and breakdown performance. This will open new horizons for SiC devices, being used to handle ever increasing power in known contexts, like automotive, and in more pioneeristic ones. A first example is train traction, that could be battery-operated thanks to the efficiency boost; another one is very high-voltage applications at grid level, to support innovative grid management techniques, in the smart grids field.

In the most advanced future applications, the coexistence of GaN, SiC, and even Si switches in the same converter can be crucial to obtain the maximum performance at the minimum cost. Mathematical optimization tools can be very effective in this scenario, as seen in the multi-objective optimization approach introduced by Burkart and Kolar et al. [60], that uses well-tuned compact models to optimize the choice of devices to fully leverage the advantages of all the different semiconductor materials available to power electronics.

In the most intensive applications, several devices are simultaneously used in series or parallel configuration, with the aim of sustaining higher voltages or currents. In these cases, the device-level analysis must be completed by system-level design considerations. These typically include, not being limited to, a careful management of the thermal aspects or the mitigation of current/voltage unbalances between individual devices. Such unbalances can induce static and dynamic performance variations [61] thus resulting in uneven conduction and switching losses and unequal transient currents distribution. Higher current overshoots can therefore occur, and a derating of current capability may be needed to remain within SOA limits, thus yielding to an unoptimized usage of the solid-state switches [62].

VI. Conclusion

We presented an overview on the current status of commercially available GaN and SiC power transistors. The related material properties are first discussed and the structural difference between platform-specific devices are evidenced.

The comparison among the two families of devices is first performed by comparing datasheet metrics, and by focusing on 650 V devices, a voltage range where both GaN- and SiC-based transistors coexist and Si devices are well developed. The data show that available GaN devices have the best performance when considering $R_{ON} \times Q_G$ FOM, input capacitance and reverse recovery charge. SiC devices, on the other hand, show a little worse performance on the same metrics, still exhibiting great improvement with respect to Si MOSFET technology.

Higher voltage devices are also compared. GaN shows better performance, but its development is still limited by technological and reliability issues. In this voltage/power range, SiC represents a valid alternative, considering the large market availability of many different and competitive products.

The current fields of applications of GaN- and SiC-based power devices are then analyzed, along with the main circuital topologies adopted in modern power converters. Future applications are also described. GaN devices are expected to see a widespread diffusion in power supplies for consumer electronics and data centers and in domestic appliances. GaN-SiC coexistence will be found in PV and automotive, while SiC will dominate the high-power, high-voltage smart grids and train traction applications.

Current reliability and performance challenges are then outlined, with particular focus on V_{th} instabilities and related mitigation strategies. Technology-related aspects are also described. SiC devices proved to be very stable during operation, with much lower V_{TH} shift and without suffering of dynamic ON-resistance effects. They are the perfect choice for harsh conditions since they are very close to IGBTs performance in terms of lifetime and SC capabilities. GaN, instead, presents better and faster switching, but reliability is still in optimization for the >1000 V range. GaN fully qualified devices are already available on the market, with good performance and reliability [63].

Based on the literature available on state-of-the-art GaN and SiC power devices, a clear path for future improvements in both performance and reliability emerges; we expect GaN and SiC technologies to coexist in the coming years, depending on the specific requirements of each individual application, and on the related mission profiles. The competition with silicon will also be source of further optimization, in terms of performance, reliability, and cost reduction.

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