Design of Droop Controllers for Converters in DC Microgrids Towards Reducing Bus Capacitance

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Keywords

≪DC microgrids≫, ≪*V*-*I* droop≫, ≪*I*-*V* droop≫, ≪controller design≫, ≪reduced bus capacitance≫.

Abstract

DC microgrids based on droop-controlled Distributed Energy Resources (DERs) converters tend to have large bus capacitance in order to guarantee stiff bus voltage. Large bus capacitance leads to the increase of weight, size, and cost. Indeed, since the droop control inherently allows the bus voltage to vary in a certain range, there is no need to restrict the dynamic bus voltage fluctuation to such a low level. Thus, as long as the bus voltage is maintained in the acceptable range, smaller bus capacitance can be chosen. This paper firstly gives the design criterion of the output capacitance for DERs converters. Then, the design of droop controllers are presented, so that the output capacitance can be reduced while the bus voltage is still kept in the allowable range during any transient. Since voltage-current (*V*-*I*) and current-voltage (*I*-*V*) droop control methods show different characteristics, separate design procedures are introduced for them. Finally, the proposed design methods are validated by means of experimental results performed on a dc microgrid prototype composed of two 3 kW converters.

Introduction

Distributed Energy Resources (DERs) have seen a vigorous development in recent years. Various DERs can be grouped as a microgrid together with local customers loads. Due to the dc nature of many DERs (e.g., battery energy storage systems) and loads (e.g., electric vehicles), dc microgrids show better compatibility than their ac counterparts.

In a dc microgrid, Power Electronic Converters (PECs) are utilized to interface sources and loads with the common dc bus, as shown in Fig. 1. In order to accomplish automatic load distribution among parallel sources, droop control approaches are often applied to DERs PECs. With droop control adopted, the dc bus voltage varies within a predefined acceptable range according to the load condition. For the purpose of providing a reliable bus voltage for customers loads, it is essential to always keep the bus voltage in this allowable range. To meet this objective, a very straightforward solution is to design dc microgrids with relatively bulky bus capacitors. In such a case, the dc bus voltage is so stiff that bus voltage sags and surges during load changes are small enough or even negligible [2]. Obviously, huge bus capacitance is

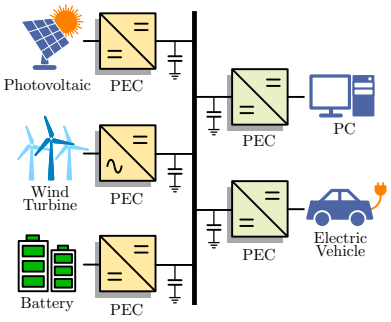
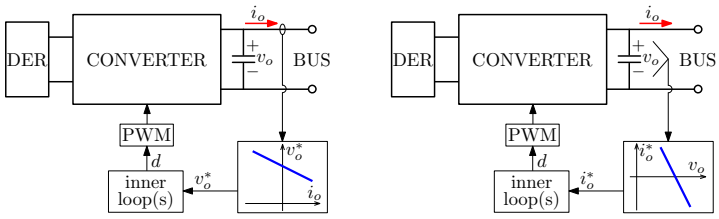


Fig. 1: An example dc microgrid.



(a) (b)

Fig. 2: Droop-controlled DERs PECs. (a) *V-I* droop; (b) *I-V* droop.

not an economic design. Besides, it increases the system weight and size, which is critical in applications like aircrafts. Moreover, large bus capacitance means a great amount of energy stored on the bus. In case of a bus short-circuit fault, high fault current can be generated, which makes fault isolation quite difficult [3]. In fact, massive bus capacitance is a pretty conservative choice. Since the droop control strategy allows the bus voltage to fluctuate in a certain range, there is no need to suppress the bus voltage dips and rises to such a low level. Hence, as long as the bus voltage do not exceed the acceptable range during any transient process, the bus capacitance can be reduced. From Fig. 1, it can be seen that the total bus capacitance comprises the output capacitance of DERs PECs and the input capacitance of loads PECs. The task of this paper is to decrease the output capacitance of every single droop-controlled PEC while its output voltage is limited in the acceptable range. To fulfill this goal, there are two main issues : the first one is how to choose appropriate output capacitance; the second one is how to design the droop controller towards successfully implementing the reduced output capacitance.

A dc microgrid featuring small PECs output capacitance is introduced in [4] and its small-signal stability is analyzed in [5]. However, in order to restrict the bus voltage drops and surges, this dc microgrid imposes constraints on the rate of change of load, which is generally unexpected and not practical. Virtual Capacitance Control (VCC) is a potential way to address the aforementioned issue. There are already many studies on this control method. In [6, 7], VCC is utilized to increase the dc microgrids inertia in large time scale. In [8, 9], VCC is used to enhance the system damping. Differently, [8] presents the small-signal stability analysis of dc microgrids, while [9] discusses the large-signal stability of a single rectifier supplying a constant power load. Also, high-frequency power and low-frequency power can be allocated to different sources by employing VCC [10]. In addition, VCC is adopted in an inverter to obtain lower output voltage distortion [11]. It can be found that VCC has been exploited for various purposes, but it has not been used for the decrease of output capacitance of droop-controlled PECs. Thus, it is necessary to further study and improve the droop controllers of PECs, for the sake of decreasing their output capacitance.

On the other hand, the implementation of droop control strategy can be categorized into two types: voltage-current (*V-I*) droop and current-voltage (*I-V*) droop, as shown in Fig. 2. One PEC employing the *V-I* droop method holds an inner current loop and an inner voltage loop, and then the droop loop is added. The droop loop generates the output voltage reference v_o^* based on the sampled output current i_o and the droop impedance, which is typically designed as a pure resistance. On the other hand, one PEC adopting the *I-V* droop control is usually designed as a current source firstly, and then the output current reference i_o^* is calculated according to the measured output voltage v_o and the droop impedance. These two droop approaches have the same steady-state behavior, but they are different in dynamic performances [12, 13]. In this case, the design methodologies of *V-I* and *I-V* droop approaches should be considered respectively.

This paper concentrates on the reduction of output capacitance of droop-controlled PECs in dc microgrids, keeping the bus voltage in the acceptable range. The main contributions of this paper can be summarized as: (1) instead of a pure resistance, a frequency-dependent impedance is considered as the droop impedance for the *V-I* droop control, so that reduced output capacitance can be implemented with

the bus voltage limited in the acceptable range; (2) one PEC implementing the *I-V* droop control approach is proposed to be designed as a voltage source rather than a current source, which gives a better view of the system stability.

Design criterion of output capacitance

This section provides the design criterion to have an initial value of the output capacitance for a droop-controlled PEC, by investigating the effect of the output capacitance on the output impedance.

Fig. 3a depicts the output impedance of a droop-controlled PEC with different output capacitance. With sufficient output capacitance C_{ol}, the output impedance Z_{ol} is equal to the static droop resistance r_d in low frequency range and then dominated by C_{ol} in high frequency range. Consequently, Z_{ol} does not go above r_d at any frequency. However, with the output capacitance declining to a small value C_{os}, the output impedance Z_{os} shows higher magnitude than r_d. With different output impedance (i.e., r_d, Z_{ol}, and Z_{os}), the output voltage variations when facing a nominal load step are presented in Fig. 3b. In the transient process, with the output impedance being r_d or Z_{ol}, when the output current i_o steps from I_{min} to I_{max}, the output voltage v_o decreases from V_{max} to V_{min} and always stays in this range. On the contrary, with the output impedance being Z_{os}, v_o shows an undershoot and goes out of the acceptable range. A similar result can be obtained when i_o steps from I_{max} to I_{min}. Hence, for each droop-controlled PEC, to ensure that the output voltage is kept in the allowable range when facing a sudden load change, the output impedance is expected to be equal to or lower than r_d in full frequency range.

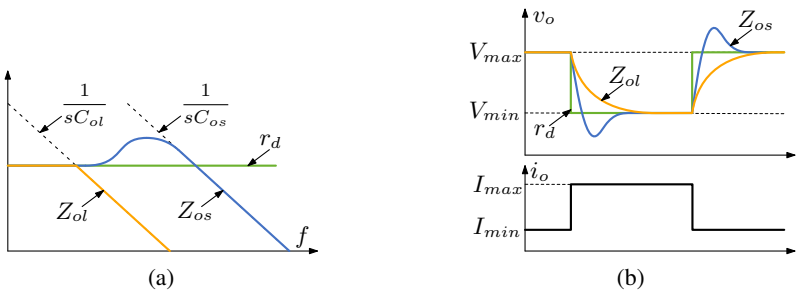
In general, the output impedance Z_{od} is complex in formula. Numerical tools are required to precisely evaluate the influence of C_o on Z_{od}. To get an initial value of C_o, the ideal shape of Z_{od} is considered herein. The ideal Z_{od} with inadequate output capacitance is presented in Fig. 4a. The structure of Z_{od} can be divided into three parts. Within the output voltage control bandwidth f_v, Z_{od} can be effectively shaped to be r_d by means of control methods. Then, from f_v to f_0, Z_{od} loses control and becomes closer to the open-loop output impedance, which shows the character of C_o in high frequency range. Above f_0, Z_{od} matches the impedance of C_o. As can be observed, Z_{od} is higher than r_d from f_v to f_{int}. f_{int} is the frequency where the impedance of C_o intersects with r_d. To mitigate the magnitude of Z_{od}, f_{int} should not exceed f_v:

$$f_{int} = \frac{1}{2\pi \cdot C_o \cdot r_d} \leqslant f_v \tag{1}$$

The proper output capacitance C_o can then be expressed as:

$$C_o = \frac{1}{2\pi \cdot r_d \cdot f_v} \tag{2}$$

The resulting output impedance is shown in Fig. 4b. In practice, the voltage control bandwidth can be firstly estimated according to the switching frequency and the control delay, then the initial output



(a) (b)

Fig. 3: The output impedance of a droop-controlled PEC and the corresponding output voltage variations. (a) the output impedance Z_{ol} with large output capacitance C_{ol} and the output impedance Z_{os} with small output capacitance C_{os}; (b) the corresponding output voltage variations under a nominal load step.

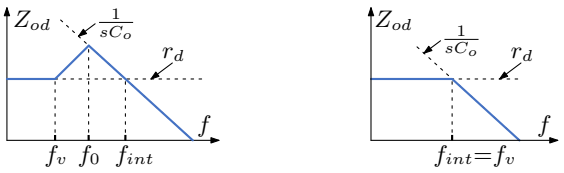


Fig. 4: The ideal shape of the output impedance. (a) with inadequate output capacitance; (b) with proper output capacitance.

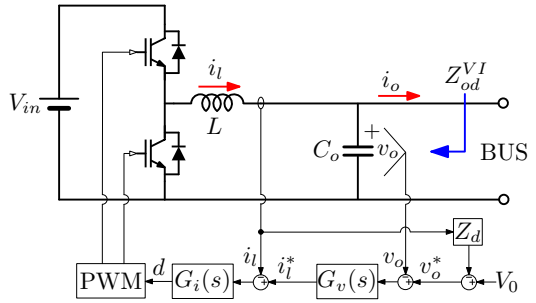


Fig. 5: Control scheme of an example *V-I* droop-controlled PEC.

Table I: System Parameters

Parameter	Symbol	Value
Input voltage	V_{in}	650 V
Nominal bus voltage	V_o	380 V
Nominal power	P_n	5 kW
Inductance	L	1.6 mH
Output capacitance	C_o	105 µF
Switching frequency	f_s	25 kHz
Voltage set point	V_0	380 V
Droop resistance	r_d	1.52 V/A

capacitance can be calculated by (2). It is worth mentioning that the output capacitance obtained from (2) is only an initial guess, it can be adjusted accordingly during the design process. Moreover, by implementing some other control techniques, like oversampling, the output feedforward technique, and the predictive control methods, the output capacitance can be further reduced.

Design of *V-I* droop controller

Using a buck converter as an example, the control scheme of the *V-I* droop-controlled PEC is shown in Fig. 5. The system parameters in this example are reported in Table I. The acceptable bus voltage range, which can be derived from the nominal output current and the droop resistance, is from 360 V to 400 V. As mentioned in the last section, the output capacitance C_o can be selected based on the voltage control bandwidth f_v. For example, f_v herein is set at 1 kHz, which is $1/25$ of f_s, then C_o is calculated as 105 µF according to (2).

The state variables $\hat{i}_l$ and $\hat{v}_o$ can be expressed as:

$$\hat{i}_l = \frac{sC_oV_{in}}{s^2LC_o+1}\cdot\hat{d} + \frac{1}{s^2LC_o+1}\cdot\hat{i}_o = G_{id}(s)\cdot\hat{d} + G_{ii_o}(s)\cdot\hat{i}_o \tag{3}$$

$$\hat{v}_o = \frac{1}{sC_o}\cdot\hat{i}_l + \left(-\frac{1}{sC_o}\right)\cdot\hat{i}_o = G_{vi}(s)\cdot\hat{i}_l + G_{vi_o}(s)\cdot\hat{i}_o \tag{4}$$

where the diacritic mark ˆ indicates the ac small signal. The linearized control block diagram of the *V-I* droop-controlled PEC is displayed in Fig. 6. The effect of $\hat{i}_o$ on $\hat{i}_l$ can be approximately neglected, and the current control loop can be simplified as a first-order lag with a time constant τ_i, which is in the scale of switching period T_s. As a result, the simplified model can be obtained, as shown in Fig. 7. With Z_d being r_d, the output impedances found from the full-order model (see Fig. 6) and the simplified model (see Fig. 7) are shown in Fig. 8. As can be seen, the output impedances deduced from two models show minor difference and the simplified model is sufficiently accurate for the following analysis. The output

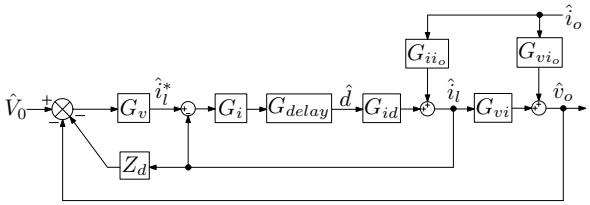


Fig. 6: The linearized control block diagram of the *V-I* droop-controlled PEC.

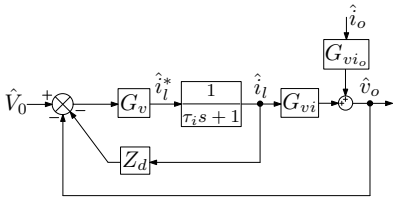


Fig. 7: The simplified control block diagram of the *V-I* droop-controlled PEC.

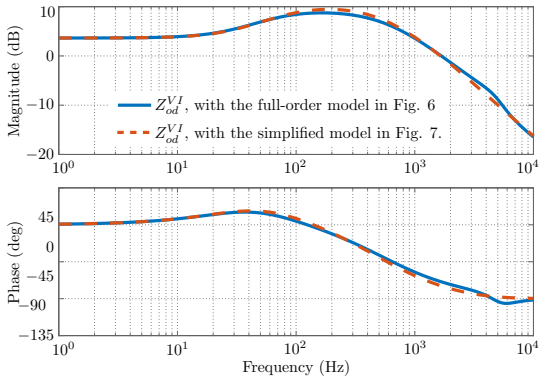


Fig. 8: Bode diagram of the output impedance found from the full-order model (see Fig. 6) and the simplified model (see Fig. 7).

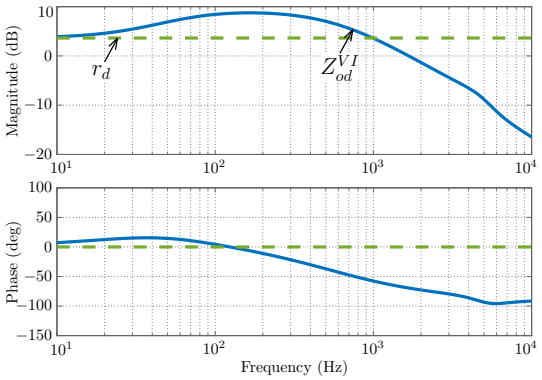


Fig. 9: Bode diagram of the output impedance Z_{od}^{VI} with droop loop closed and the output impedance Z_{ov}^{VI} with droop loop open.

impedance $Z_{od}^{VI}(s)$ is derived as:

$$Z_{od}^{VI}(s) = -\frac{\hat{v}_o(s)}{\hat{i}_o(s)} = \frac{\frac{1}{sC_o}\cdot\left(1+G_v(s)\cdot Z_d\cdot\frac{1}{\tau_i s+1}\right)}{1+G_v(s)\cdot Z_d\cdot\frac{1}{\tau_i s+1}+\frac{1}{sC_o}\cdot G_v(s)\cdot\frac{1}{\tau_i s+1}} \tag{5}$$

The *V-I* droop controller consists in a current loop, a voltage loop, and a droop loop. In terms of the controller design, generally, the current loop is designed firstly, followed by the voltage loop. In the end, the droop loop is closed. PI controllers are usually used for current regulator $G_i(s)$ and voltage regulator $G_v(s)$ to achieve zero steady-state errors. In this example, the current control bandwidth and the voltage control bandwidth are designed at 2 kHz and 1 kHz, respectively. Herein, the voltage control bandwidth is chosen based on (2). With Z_d being r_d, Fig. 9 depicts the corresponding output impedance $Z_{od\_r}^{VI}$, which is larger than r_d in a frequency range. To bring down the magnitude of the output impedance, Z_d needs to be redesigned.

Let us assume the output impedance Z_{od}^{VI} [see (5)] to be ideal, which means Z_{od}^{VI} is equal to the parallel impedance of r_d and $1/sC_o$:

$$Z_{od}^{VI}(s) = \frac{r_d}{sC_o r_d+1} \tag{6}$$

Combining (5) and (6), the droop impedance $Z_d(s)$ can be calculated as:

$$Z_d(s) = r_d - \frac{\tau_i s+1}{G_v(s)} \tag{7}$$

In the actual implementation, the transfer function of $Z_d(s)$ should be causal. For instance, in the case

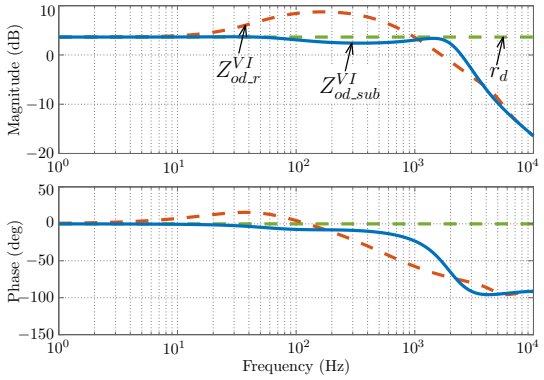


Fig. 10: Bode diagram of the output impedance $Z_{od\_sub}^{VI}$, with Z_d being $r_d - 1/G_v$.

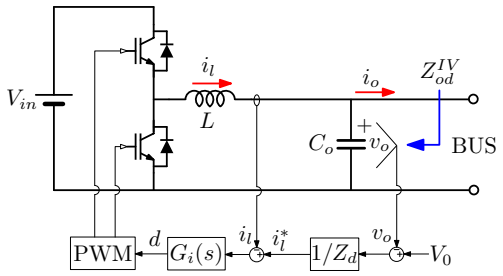


Fig. 11: Control scheme of an example *I-V* droop-controlled PEC.

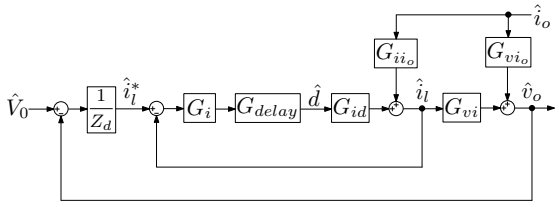


Fig. 12: The linearized control block diagram of the *I-V* droop-controlled PEC.

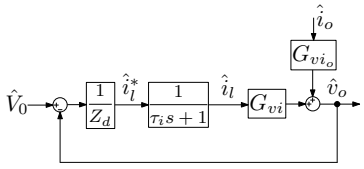


Fig. 13: The simplified control block diagram of the *I-V* droop-controlled PEC.

that $G_v s$ employs a PI controller, a first-order low-pass filter with a cutoff angular frequency of $1/\tau_1$ is utilized. Then, the droop impedance $Z_d(s)$ becomes:

$$Z_d(s) = r_d - \frac{(\tau_i s+1)\cdot s}{k_p \cdot s + k_i} \cdot \frac{1}{\tau_1 s+1} \tag{8}$$

where k_p and k_i are the proportional gain and the integral gain of $G_v(s)$. Employing such a Z_d, the resulted output impedance $Z_{od\_sub}^{VI}$ can be expressed as:

$$Z_{od\_sub}^{VI}(s) = \frac{\frac{1}{sC_o}\cdot\left(r_d \cdot G_v(s)\cdot\frac{1}{\tau_i s+1} + \frac{\tau_1 s}{\tau_1 s+1}\right)}{r_d \cdot G_v(s)\cdot\frac{1}{\tau_i s+1} + \frac{\tau_1 s}{\tau_1 s+1} + \frac{1}{sC_o}\cdot G_v(s)\cdot\frac{1}{\tau_i s+1}} \tag{9}$$

At low frequency, by eliminating the effect of $\tau_1 s/(\tau_1 s+1)$, $Z_{od\_sub}^{VI}$ can be further approximated as:

$$Z_{od\_sub}^{VI}(j\omega) \approx \frac{r_d}{j\omega \cdot C_o r_d + 1}, \quad \omega < 1/\tau_1 \tag{10}$$

It can be easily found that the design target is attained. Fig. 10 also shows the bode diagram of $Z_{od\_sub}^{VI}$, with τ_1 designed as, for example, τ_i. It can be observed that the output impedance is successfully mitigated to be equal to or lower than r_d.

In summary, for a *V-I* droop controller, its current loop and voltage loop can be designed as usual. However, the droop impedance Z_d should follow (7) rather than a pure resistance r_d.

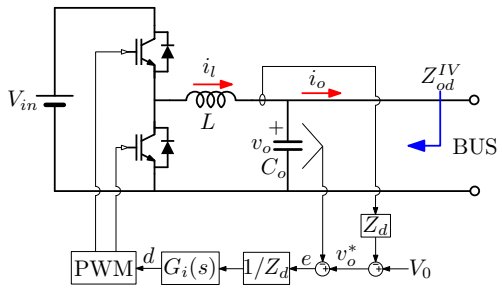


Fig. 14: The equivalent control scheme of the *I-V* droop-controlled PEC.

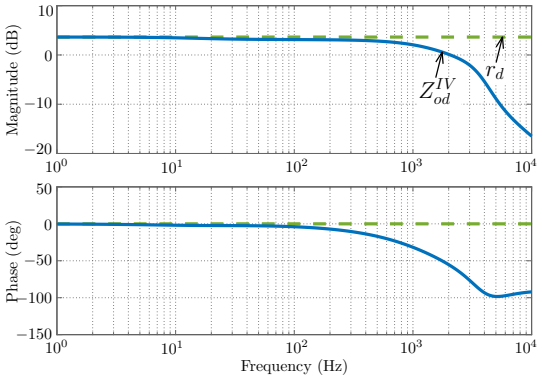


Fig. 15: Bode diagram of the output impedance Z_{od}^{IV}.

Design of *I-V* droop controller

The control scheme of a *I-V* droop-controlled PEC is shown in Fig. 11. The linearized model of this PEC is shown in Fig. 12. Similarly, By neglecting the influence of $G_{ii_o}(s)$ and approximating the current loop as a first-order lag, the simplified model is illustrated in Fig. 13. With Z_d being r_d, the output impedance $Z_{od}^{IV}(s)$ can be expressed as:

$$Z_{od}^{IV}(s) = -\frac{\hat{v}_o(s)}{\hat{i}_o(s)} = \frac{\dfrac{1}{sC_o}}{1+\dfrac{1}{r_d}\cdot\dfrac{1}{\tau s+1}\cdot\dfrac{1}{sC_o}} \tag{11}$$

Further, by considering $1/(\tau_i s+1)$ as a unit gain, the low-frequency Z_{od}^{IV} is given as:

$$Z_{od}^{IV}(j\omega) \approx \frac{r_d}{j\omega\cdot C_o r_d+1}, \quad \omega < 1/\tau_i \tag{12}$$

Compared to the *V-I* droop controller, the *I-V* droop controller inherently presents a satisfactory output impedance with a pure resistance r_d adopted as Z_d.

The *I-V* droop controller is composed of a current loop and a droop loop. As for the controller design, typically, the converter employing the *I-V* droop control is designed as a current source firstly, and then the droop loop is added. However, the external droop loop may bring instability issues since the voltage loop gain is affected by $1/Z_d$. In such a case, the stability is not guaranteed with the traditional design method. Hence, this paper proposes to directly design the *I-V* droop-controlled PEC as a voltage source. By moving the current feedback path, the equivalent control scheme is shown in Fig. 14. Then, the regulator $G_i(s)$ can be designed based on the droop loop transfer function $T_d(s)$, which is shown as below:

$$T_d(s) = \frac{\hat{i}_l\cdot r_d+\hat{v}_o}{\hat{e}} = G_i(s)\cdot V_i\cdot\frac{sC_o+1/r_d}{s^2LC_o+1} \tag{13}$$

In such a case, the output voltage stability is explicitly presented in the design process. The bode diagram of the output impedance Z_{od}^{IV} is shown in Fig. 15. By changing $G_i(s)$, $T_d(s)$ is designed to have a bandwidth of 3 kHz and a phase margin of 30°. It can be seen that Z_{od}^{IV} is always equal to or lower than r_d, and the design target is achieved.

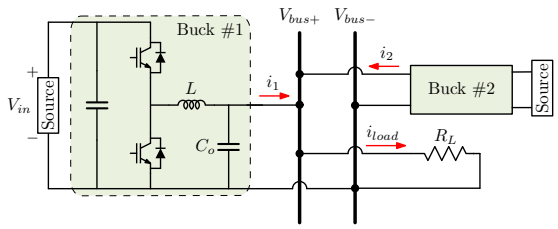


Fig. 16: Schemativ of the laboratory-scale dc microgrid prototype.

Table II: Experimental System Parameters

Parameter	Symbol	Value
Input voltage	V_{in}	380 V
Nominal bus voltage	V_o	200 V
Nominal power	P_n	3 kW
Inductance	L	1.6 mH
Output capacitance	C_o	160 µF
Switching frequency	f_s	12.5 kHz
Voltage set point	V_0	200 V
Droop resistance	r_d	1.33 V/A

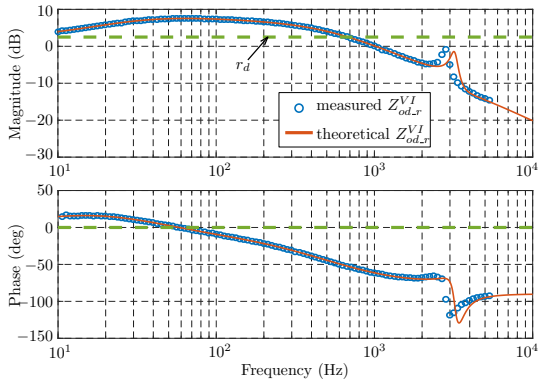


Fig. 17: The measured and theoretical output impedance $Z_{od\_r}^{VI}$ of a *V-I* droop-controlled PEC shown in Fig. 5, with Z_d being r_d.

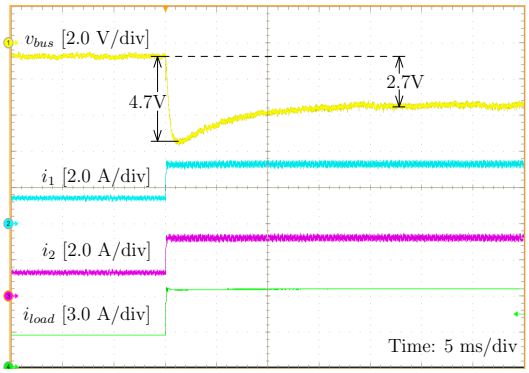


Fig. 18: Experimental results under a load step of R_L: 70 Ω ⇒ 30 Ω, with the output impedance shown in Fig. 17.

Experimental Results

Fig. 16 shows the schematic of a laboratory-scale dc microgrid prototype. The set up is composed of two same DER PECs. The experimental system parameters are reported in Table II. Since the switching frequency is 12.5 kHz, the estimated voltage control bandwidth is 750 Hz, which results in an output capacitance of 160 µF according to (2).

V-I droop controller

In this test, the *V-I* droop control shown in Fig. 5 is implemented on two DER PECs. The current loop bandwidth and the voltage loop bandwidth are designed at 1.5 kHz and 750 kHz, respectively. Firstly, the droop impedance Z_d is designed as a pure resistance r_d. The actual output impedance is measured by using the Software Frequency Response Analyzer (SFRA) library, which is provided by Texas Instruments. Fig. 17 shows the comparison between the measured and the theoretical output impedance. There are two facts can be seen: the first one is that the practical output impedance matches the theoretical one, the second one is that $Z_{od\_r}^{VI}$ has higher magnitude than r_d at some frequencies. The corresponding experimental results under a load step are presented in Fig. 18. Due to the high output impedance, the bus voltage shows a large undershoot during the transient.

To avoid the undershoot during the transient, Z_d should be reconsidered. As mentioned in the previous section, Z_d can be designed as (7). τ_1 applied in this experiment is equal to τ_i. Fig. 19 depicts the theoretical and the measured output impedance $Z_{od\_sub}^{VI}$. Both of them are below r_d. As a consequence, the voltage undershoot is successfully suppressed, as shown in Fig. 20.

I-V droop controller

In this test, the *I-V* droop control illustrated in Fig. 14 is employed by two DER PECs. The droop loop, the transfer function of which is expressed as (13), is designed to have a bandwidth of 1.8 kHz. The

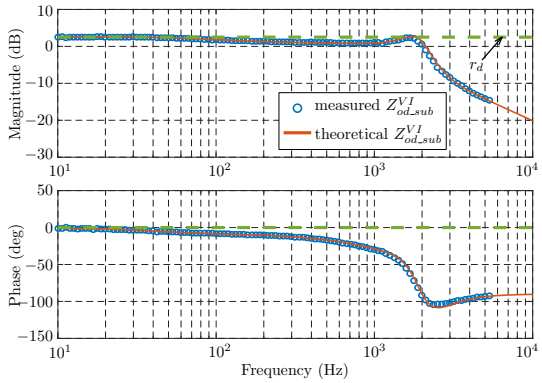


Fig. 19: The measured and theoretical output impedance $Z_{od\_sub}^{VI}$ of a *V-I* droop-controlled PEC shown in Fig. 5, with Z_d being $r_d - 1/G_v$.

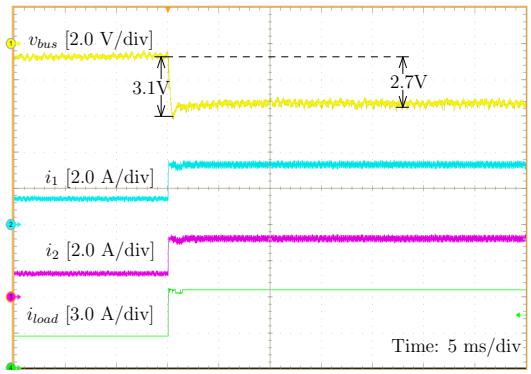


Fig. 20: Experimental results under a load step of R_L: $70\,\Omega \Rightarrow 30\,\Omega$, with the output impedance shown in Fig. 19.

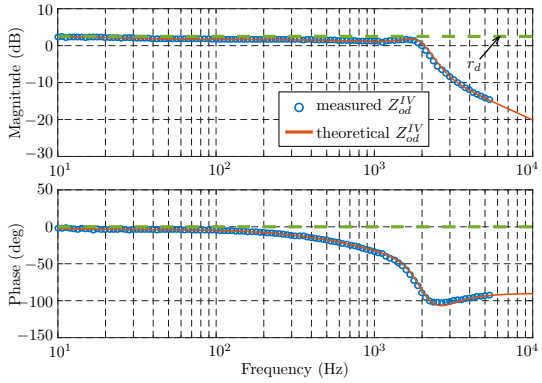


Fig. 21: The measured and theoretical output impedance Z_{od}^{IV} of a *I-V* droop-controlled PEC shown in Fig. 11, with Z_d being r_d.

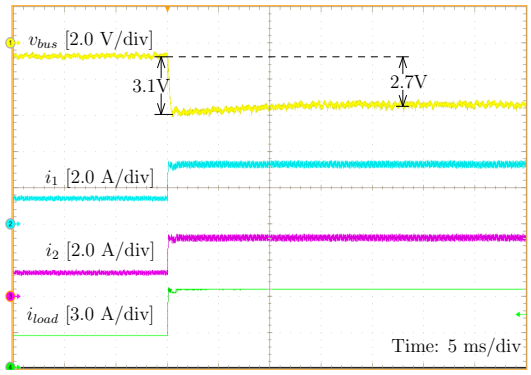


Fig. 22: Experimental results under a load step of R_L: $70\,\Omega \Rightarrow 30\,\Omega$, with the output impedance shown in Fig. 21.

resultant output impedance Z_{od}^{IV} is shown in Fig. 21, with Z_d being r_d. It can be found that Z_{od}^{IV} has smaller magnitude than r_d in full frequency range. The dynamic experimental results are displayed in Fig. 22. As can be seen, the bus voltage shows small undershoot during the transient.

Conclusion

This paper presents two design guidelines for voltage-current (*V-I*) and current-voltage (*I-V*) droop controllers in dc microgrids, respectively. Following the proposed design, the output capacitance of droop-controlled converters can be reduced, while the bus voltage is always located in the acceptable range during any transient response. For the *V-I* droop control, by designing the droop impedance as a proposed transfer function, the PECs output impedances are shaped to be equal to and lower than their static droop resistances in full frequency range. For the *I-V* droop control, this paper proposes to design the implemented converter as a voltage source rather than a current source. By doing so, the full view of the system stability is shown in the design process.The obtained advantages have been verified by experimental results performed on a laboratory-scale dc microgrid prototype.

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