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Analysis of threshold voltage instabilities in semi-vertical GaN-on-Si FETs

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We present a first study of threshold voltage instabilities of semi-vertical GaN-on-Si trench-MOSFETs, based on double pulsed, threshold voltage transient, and UV-assisted *C–V* analysis. Under positive gate stress, small negative V_{th} shifts (low stress) and a positive V_{th} shifts (high stress) are observed, ascribed to trapping within the insulator and at the metal/insulator interface. Trapping effects are eliminated through exposure to UV light; wavelength-dependent analysis extracts the threshold de-trapping energy ≈2.95 eV. UV-assisted CV measurements describe the distribution of states at the GaN/Al_2O_3 interface. The described methodology provides an understanding and assessment of trapping mechanisms in vertical GaN transistors. © 2020 The Japan Society of Applied Physics

Vertical GaN technology[1–15] is developing rapidly and, in particular, trench-MOSFETs[8–13] are attracting an ever increasing attention owing to their potential applications in the power conversion field.[16] For continued growth of this technology, the study and minimization of threshold instabilities is a fundamental step. Al_2O_3 dielectrics have emerged as a dominant choice for developing vertical MOS technologies.[17,18] Recent works[19,20] indicate three prevalent trapping locations within the Al_2O_3/GaN MOS devices, responsible for V_{th} shift: (i) states within the bulk dielectric, (ii) near-interface or border sites, and (iii) states along the oxide/GaN interface. While the presence of the former two are oxide-dependent, the interface state density (D_{it}) reflects the quality of the dielectric/semiconductor boundary, and of the process. Despite the importance of these trapping processes, these aspects have been studied only preliminarily by previous reports,[17,21,22] and a comprehensive description still needs to be published.

The aim of this paper is to contribute to an improved understanding of V_{th} shift in semi-vertical GaN devices, and to provide in-depth perspectives on the physical origin of the trapping processes. To this aim, we integrated several analytical techniques to investigate the trapping processes and the associated recovery dynamics: pulsed measurements, transient investigation, light-assisted de-trapping, capacitance–voltage measurements.

The original results obtained within this paper demonstrate that positive gate voltage stress can trigger multiple trapping mechanisms contributing to strong positive and weak negative V_{th} shifts due to trap states across the metal/Al_2O_3/GaN layers. Light energies above 2.9 eV (≈0.8 eV from E_C) are found to assist in faster recovery from semi-permanent trapping states in the bulk oxide and/or interface. Photo assisted CV measurements yield the interface trapped charge distribution (D_{it}) for the gate stress of 5 V which indicates prevalence of shallow traps, located mostly at ⩽0.3 eV from the conduction band (E_C).

The devices are normally-off GaN trench MOSFETs grown on a silicon substrate by MOCVD,[23] with a 35 nm Al_2O_3 dielectric. The epitaxial GaN layers include a stress compensation layer, a thick and lightly doped drift layer and a doped p-body (see. Fig. 1).

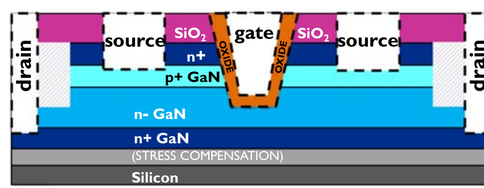

Fig. 1. (Color online) Structural schematic of the GaN-on-Si semi-vertical FET technology.

The device has a semi-vertical configuration. This term refers to the fact that the flow of current in the experimental structure is not fully vertical, since the drain current is collected laterally through a n+ layer, and not vertically through the silicon substrate. The n+ top layer (250 nm) sources the electrons which then flow vertically through the channel in the p+ GaN layer (400 nm) along the gate trench sidewalls to reach the n− GaN drift layer (750 nm). A highly doped drain n+ region is integrated in the epitaxial stack such that the current flows laterally through this layer, before being routed back to the surface through the drain metallization.

To preliminarily evaluate device dynamic behavior and stability of V_{th} under positive gate stress, we performed double pulsed measurements[24] that evaluate threshold instabilities within a short time scale (μs), thus capturing relatively fast trapping processes. The setup switches between quiescent ($V_{G,Stress}$: 0–5 V for $t_Q = 100\,\mu s$ and $V_{D,Stress} = 0$ V) and measurement ($V_{GS} = -1$ to 7 V at $V_{DS} = 8$ V, $t_{meas} = 1\,\mu s$) conditions.

Figure 2 displays the corresponding I_D–V_G behavior for the cumulative stress procedure on a typical device. The threshold voltage is defined as the voltage intercept at $I_D = 5$ mA mm^{-1} which reflects a clear trend with change in $V_{G,Q}$. The results emphasize a monotonic increase in V_{th} with higher quiescent V_G, with a maximum positive ΔV_{th} >1.2 V for $V_{G,Q} = 5$ V in Fig. 2(a). This high ΔV_{th} arises from (i) the fast pulsed measurement configuration and (ii) the absence of recovery intervals between increments in quiescent stress $V_{G,Q}$. The shifts are semi-permanent with only 10%–20% recovery after several minutes following $V_{G,Q} = 5$ V.

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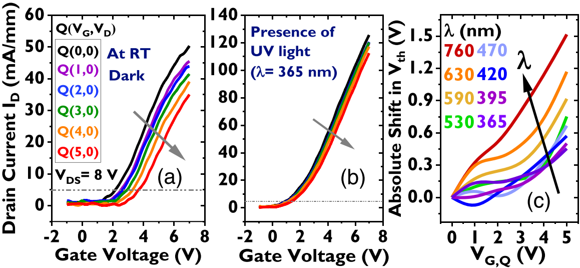

Fig. 2. (Color online) (a) Double pulsed I_D–V_G curves for various quiescent voltages at room temperature under dark conditions (b) with UV light. (c) Extracted ΔV_{th} under light of different wavelengths.

Typically, it could take from several hours to days to achieve 80%–90% recovery in V_{th}.

When the experiment was repeated under exposure to high energy photons, as presented in Figs. 2(b) and 2(c), ΔV_{th} is found to be smaller with a distinct wavelength dependence [see. Fig. 2(c)]. Under UV light, I_D–V_G drifts are reduced, and ΔV_{th} falls to a substantially smaller value, ≈0.45 V for $V_{G,Q} = 5$ V. [see. Fig. 2(b)]. These observations strongly suggest the presence of slow-emitting trap states (de-trapping times >300 s) which could be either (1) bulk states spatially located deeper within the oxide or (2) interface states energetically located deeper within the bandgap. Quick de-trapping from such states would only be possible only through external illumination.

To better investigate the semi-permanent nature of the positive V_{th} shift under high fields, we employed a versatile setup capable of accurately evaluating threshold transients in the 10 μs–100 s range,[18,25,26] and re-evaluated V_{th} transients under monochromatic light excitation. Here, a typical measurement is composed of a stress and a recovery phase of 100 s each, during which V_{th} evolution is extracted from 22 fast I_D–V_G measurements ($t_{meas} = 10\ \mu$s). Figure 3(a) presents the stress phase V_{th} transients obtained for $V_{G,Stress} \leqslant 5$ V, where stress phases are separated by recovery intervals at (V_G,$V_D = 0$ V, 0 V). To describe the energetic distribution of slow-emitting traps responsible for the positive ΔV_{th}, Fig. 3(b) illustrates recovery phase V_{th} transients at (V_G,$V_D = 0$ V, 0 V) for measurements under light of $\lambda = 365$–760 nm, following equivalent stress phases (100 s at $V_{G,Stress} = 5$ V).

From Fig. 3(a), we discern a negative V_{th} shift trend (≈0.07 V at 100 s) induced during the low gate stress of $V_{G,Stress} = 1$ V, and also weakly observed for $V_{G,Stress} = 2$ V. Similar small negative V_{th} shifts were noticed for several devices, for stress times >10 s, under $V_{G,Stress} \leqslant 2$ V conditions. This negative shift is not observable in the previous double pulsed measurements because other mechanisms (contributing to positive ΔV_{th}) probably dominate for the relatively fast stress/measurement intervals chosen [total t_{Stress} at a given $V_{G,Q}$ builds up to only $40 \times 100\ \mu s = 4$ ms for the 40 point $I_D V_G$ curves in Fig. 2(a)]. The negative ΔV_{th} trend at low stress biases can be ascribed to de-trapping of electrons from pre-existing states in the dielectric towards the metal.[17,27]

$V_{G,Stress} = 3$ V and higher induce positive V_{th} shifts, proportional to the stress bias and time. In the full time-range between 10 μs and 100 s of a single $V_{G,Stress} = 5$ V phase, a strong positive $\Delta V_{th} \sim 0.75$ V [Fig. 3(a)] is induced. Under dark conditions, this shift is only partially recoverable (calculated from negative shifts in V_{th} during the recovery phase, absolute recovery ∼0.35 V) within the 100 s recovery window following the stress (not shown). A potential mechanism has been reported in other work,[28] where the recoverable degradation component has been attributed to electron injection from GaN into border traps close to the Al_2O_3/GaN interface, aligned near E_C. On the removal of stress and restoration of the Fermi level, these traps would re-emit to the GaN layer.

However, especially for high $V_{G,Stress}$, recovery is dependent on a dominantly slow detrapping process. It can be hypothesized that under high stress fields, in addition to the contribution of border and interface traps, injected electrons from the GaN channel can travel further into the oxide or occupy energetically deeper trap states. Recovery from such traps could take days or weeks to complete, since electrons are semi-permanently stored in the insulator. To better capture this behavior, de-trapping during the recovery phase is accelerated through exposure to high energy photons, as presented in Fig. 3(b). The recovery phases for each wavelength in Fig. 3(b) are preceded by equivalent 100 s stress phases at $V_{G,Stress} = 5$ V. Thus, the recovery behavior at each λ describes the device response after an induced positive ΔV_{th} ≈0.75 V. The threshold energy for enhanced de-trapping, corresponding to the lowest energetic position of deep bulk states, appears to be 2.95 eV [420 nm, Fig. 3(c)]. A complete ΔV_{th} recovery i.e. negative V_{th} shift ≈0.75 V is achieved within 100 s with 395 nm [3.1 eV, Fig. 3(b)]. Thus, the presence of trap states between these energies: 2.9–3.1 eV (≈0.8–1.0 eV from E_C, considering a Al_2O_3/GaN E_C offset =2.16 eV[29]) can be recognized (see Fig. 4).

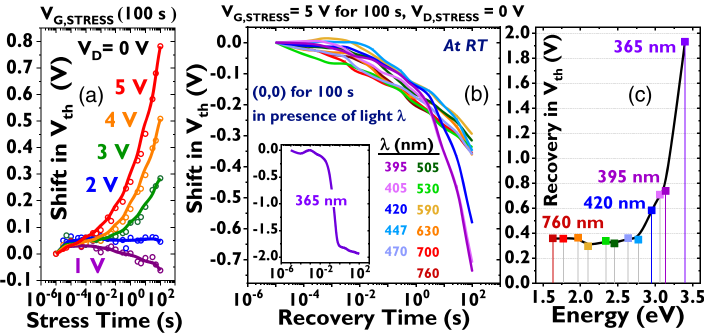

Fig. 3. (Color online) (a) Time transients V_{th} method. (a) Shift in V_{th} ($V_{th} - V_{th@10\ \mu s}$ during stress phase) during (100 s) stress and varying $V_{G,Stress}$. (b) V_{th} evolution ($V_{th} - V_{th@10\ \mu s}$ during recovery phase of 100 s), following a stress phase: 5 V for 100 s, correlation with de-trapping energies during light-assisted recovery with $\lambda = 365$–760 nm. (c) absolute V_{th} shift during recovery ($V_{th@100s} - V_{th@10\mu s}$ during recovery) under different monochromatic light.

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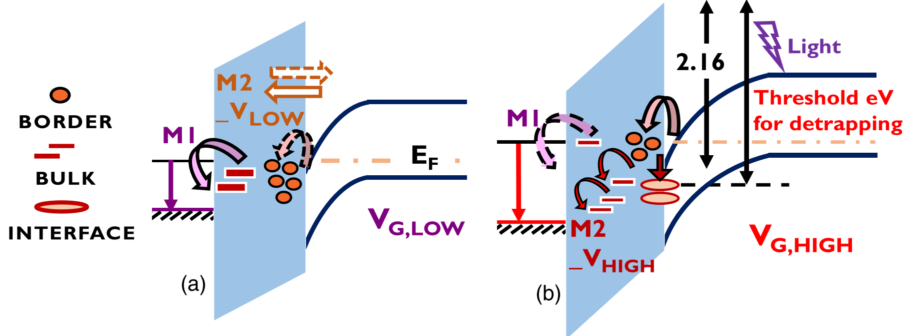

Fig. 4. (Color online) Energy band diagrams illustrating trapping locations in the Metal/Al_2O_3/GaN system (a) mechanisms activated at low V_G stress. M1: negative ΔV_{th} due to detrapped electrons from oxide towards metal. M2_V_{LOW}: moderate and recoverable positive ΔV_{th} due to injection of electrons from GaN accumulation into the border oxide traps. (b) Mechanisms strengthened at high gate stress, M2_V_{HIGH}: strong positive ΔV_{th} due to electrons injection into energetically deeper interface traps or bulk states in the dielectric. M2_V_{HIGH} causes semi-permanent trapping which requires external light energy (induce detrapping) for achieving fast recovery of V_{th}.

UV light (3.39 eV) has sufficiently high energy to remove the trapped electrons and create free carriers. It is worth noticing that the negative V_{th} shift measured with UV light [1.93 V, inset in Fig. 3(b)] overcompensates stress-induced positive drifts, indicating the de-trapping of states that—under rest conditions—are located under the Fermi level. Once dark conditions are restored, such states would gradually re-trap, corresponding to the stable device V_{th}.

Thus, from the measurements in Figs. 2–3, the mechanisms contributing to V_{th} shifts in these devices can be summarized as illustrated in Fig. 4.

(i) For low voltage ($V_G \leqslant 2$ V), a small negative V_{th} shift (<0.1 V) is attributed to the de-trapping of electrons from gate insulator towards the metal [Mechanism M1 in Fig. 4(a)].

(ii) For medium to high stress voltages (2 V < V_G < 4 V), in addition to M1, positive ΔV_{th} (≈0.2–0.3 V) due to electron trapping from the semiconductor towards border states in the dielectric [Mechanism M2_V_{LOW} in Fig. 4(a)] becomes relevant. This process is reversible on removal of the stress.

(iii) For high stress voltage (V_G > 4 V), strong positive V_{th} shifts (>0.5 V) are dominant, and recovery becomes significantly slow (several hours to days). This is attributed to the aggravation of M2 [M2_V_{HIGH} in Fig. 4(b)] under high fields, involving electron transport from the GaN channel towards the metal, inducing trapping into deep states, along the interface or in the bulk of the dielectric. Even when stress is removed, deeper trap levels remain occupied. Exposure to light with energy higher than ≈2.9 eV is essential to enable accelerated recovery.

Finally, we employ the photo-assisted capacitance–voltage or UV-CV[30] method that evaluates the distribution of interface states, D_{it}, as illustrated in Fig. 5.

Devices are exposed to UV light for 50 s in depletion in order to empty all electron traps, followed by 500 s in the dark to allow excess carriers to leave the system. Then, the de-trapped CV curve is measured [see. Fig. 5(b)] from 0 to 5 V. Bias at $V_G = 5$ V is maintained for a moderate stress time of 80 s, so as to induce charge trapping at insulator and interface but without significant alteration of the capacitance level. Finally, the C–V curve of the trapped device is measured. The D_{it} profile reported in Fig. 5(a) can be computed from the experimental data in Fig. 5(b) by using the procedure and the equations described in Ref. 30. The major parameters important for accurate calculation of D_{it} are the displacement between the detrapped and trapped C–V curves, oxide area, and the effective doping of the semiconductor channel. The difference in slope allows the extraction of D_{it} for trap energies across the entire GaN bandgap, whereas the rigid shift in the curves is proportional to the amount of charge trapped in the bulk of the oxide and/or in border traps. This paper presents a detailed investigation into the threshold voltage instability of GaN-on-Si semi-vertical FETs. Based on combined electrical and optical measurements, we identify different mechanisms as responsible for V_{th} shift: (i) at low stress voltages, a negative V_{th} shift (M1 in Fig. 4) is observed, possibly related to de-trapping of electrons from oxide states; (ii) at intermediate voltages, a moderate positive V_{th} shift (M2_V_{LOW} in Fig. 4), which is fully recoverable, has been associated to electron injection from the channel to near interface or border traps; (iii) at higher voltages, trapping might extend to deeper energy states or further into the dielectric bulk, which would yield greater V_{th} shifts (M2_V_{HIGH} in Fig. 4) with substantially longer de-trapping constants. Tests under different wavelengths were used to identify the threshold energy for de-trapping: the results identify the presence of deep-trap states within the insulator (threshold energy between 2.95 and 3.1 eV), that can be responsible for the semi-permanent trapping seen at high stress voltages. The results presented within this paper describe the dominant trapping processes for GaN-on-Si semi-vertical FETs, and general guidelines for the analysis of the related mechanisms, thus complementing the current knowledge on GaN vertical stability and reliability.[31]

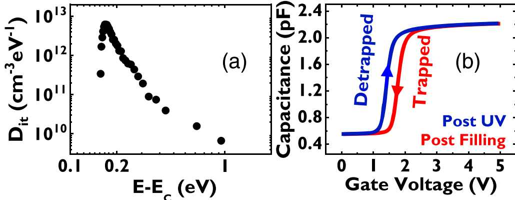

Fig. 5. (Color online) UV-CV method for D_{it} extraction. (a) Electron D_{it} versus E_G (b) C–V comparison between detrapped (after UV light) and trapped state.

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