Hysteresis Droop Controller with One Sample Delay for DC-DC Converters in DC Microgrids

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***Abstract*—Droop control is a common control strategy used in DC microgrids to manage power distribution among parallel Distributed Energy Resource (DER) converters. With droop control, the static dc bus voltage varies in a specified range according to load conditions. In order to maintain the dynamic dc bus voltage in the same range during load changes, droop-controlled DER converters usually have either large output capacitance or high voltage loop bandwidth. The latter enables the adoption of small output capacitance that improves the dc bus behaviour also during bus faults. However, with traditional control techniques, for example, the single-sampled PID controllers, the voltage loop bandwidth is limited by the control delay, including the computation time and the modulation delay. From this point of view, oversampled hysteresis control is appealing, because it reduces the modulation delay by removing the modulator. Also, the hysteretic nature allows nonlinear switching actions during transient, which further speeds up the dynamic response. Consequently, small output capacitance can be used without concerns of overvoltage and undervoltage. Moreover, hysteresis control is typically implemented on Field Programmable Gate Arrays (FPGAs). Differently, this paper focuses on the less-expensive Digital Signal Processors (DSPs) implementation. The influence of additional computation time introduced by DSP on the converter's stability is also analyzed. Simulations and experiments are carried out to verify the performance of the DSP-implemented hysteresis droop controller.**

***Index Terms*—DC microgrids, droop control, hysteresis control, output capacitance reduction, DSP implementation.**

I. Introduction

DC microgrids are composed of various Distributed Energy Resources (DERs) and customer loads [1], as shown in Fig. 1. DERs are linked to the common dc bus by means of power electronic converters. The so-called droop control is a popular decentralized control solution to address power sharing among parallel DER converters. With droop control employed, the dc bus voltage is allowed to vary in a certain range according to load conditions, that is, the dc bus voltage stays at a high level with light load and at a low level with heavy load [2]. In some critical applications, the dc bus voltage is required to be maintained inside this range not only in steady state but also during transient. In such a case, the dynamic dc bus voltage should be tightly regulated without any overshoots or undershoots during load changes, as shown in Fig. 2(a).

This project has received funding from the Electronic Components and Systems for European Leadership Joint Undertaking under grant agreement No 737434. This Joint Undertaking receives support from the European Unions Horizon 2020 research and innovation programme and Germany, Slovakia, Netherlands, Spain, Italy. G. Liu is funded by China Scholarship Council.

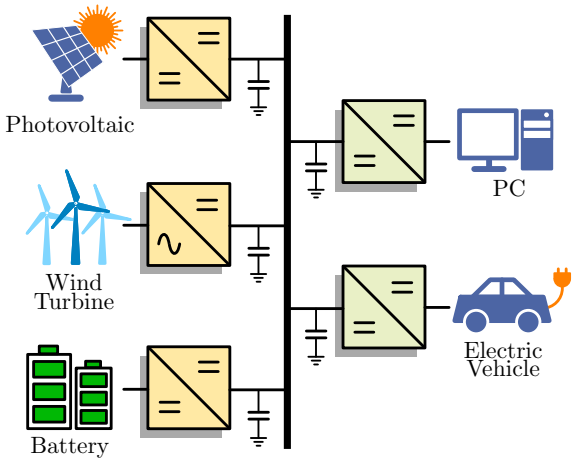

Fig. 1. Example of dc microgrids, including DERs and customer loads.

Otherwise, the dc bus voltage would exceed the limitations, as shown in Fig. 2(b).

DC bus voltage spikes or dips in case of load changes are determined by two factors: the output capacitance, and the dynamic response speed of the voltage control loop [3]. For the first factor, the output capacitors serve as energy buffers to smooth the output voltage. Under a certain load step, a larger output capacitance means a lower rate of change in the output voltage, thus, securing more time for the controller to function. For the second factor, the voltage control loop enforces the output voltage to track its reference value. Hence, a faster response of the voltage loop ensures a smaller voltage deviation. These two factors clearly suggest that, for a given voltage tolerance band, pushing the voltage control bandwidth facilitates the reduction of the output capacitance, which not only decreases the system cost, weight, and size, but also results in a lower short-circuit current during bus short-circuit faults, making faults isolation easier [4]. However, with typical single-sampled Proportional-Integral-Derivative (PID) controllers, the control bandwidth is limited by the control delay introduced by the computation time and the Digital Pulse Width Modulation (DPWM) modulator [5]. For example, considering a computation time of one switching period and the triangular carrier-based PWM, the control loop would have a total time delay of one and a half of the switching cycle, which causes about -54° phase lag at $1/10$ of the switching frequency.

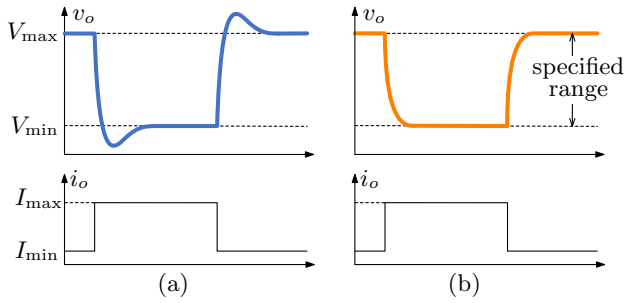

Fig. 2. The dynamic output voltage of a droop-controlled DER converter in case of load changes. (a) Undesired case: the output voltage goes out of the acceptable range during transient; (b) Desired case: the output voltage is tightly regulated inside the acceptable range.

To reduce the time delay in control loops, a possible way is to adopt the oversampling technique, in which, the signals are acquired for multiple times in one switching period [5]–[7]. By doing so, the computation time and the modulation delay can be significantly lowered to a fraction of the original value. The oversampling technique are applied to different types of control solutions, including, but not restricted to, oversampled PID control, hysteresis control [8], sliding mode control [9], and finite-control-set model predictive control [10]. The oversampled PID control is directly developed from the single-sampled one, and it features easy design and application. On the other hand, the other three control methods are nonlinear solutions that are expected to advance the linear PID controller in aspects like dynamic response. It is worth mentioning that, while the oversampled PID controller still needs a modulator, these three control methods operate without modulators, thus, totally eliminating the modulation delay.

The oversampling-based control approaches are usually implemented on Field Programmable Gate Arrays (FPGAs) to guarantee an acceptable computation time, since analog-to-digital conversions of sampled signals and relevant data post-processing must be completed within sampling intervals. Nowadays, Digital Signal Processors (DSPs) are becoming more and more powerful, showing potential capability to handle the time-critical calculation tasks. DSPs are highly integrated with various peripherals and are, in general, cheaper than FPGAs. Nevertheless, the use of DSPs inevitably introduces additional computation time and increases the control delay.

This paper extends the hysteresis controller described in [8], [11] to droop-controlled DER converters and presents the digital realization on DSP. The influence of additional computation time on the voltage loop gain is analyzed. The introduced hysteresis droop controller allows tight voltage regulation in case of load changes, thus, enabling the use of small output capacitance. The effectiveness of the hysteresis droop controller is verified by simulation results and experimental results that are carried out on a 3 kW boost-type DER converter.

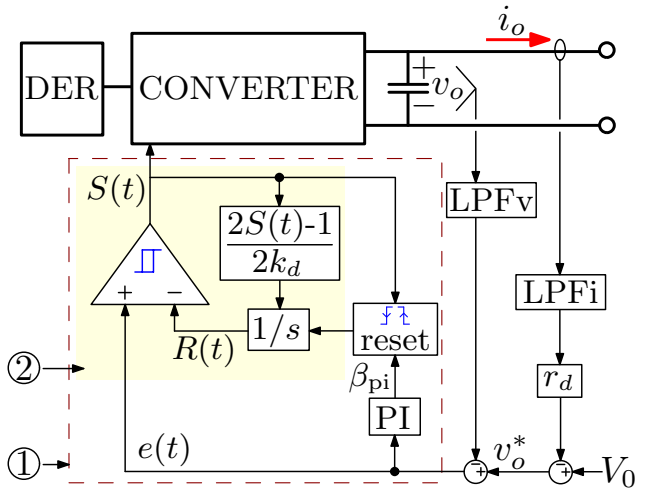

Fig. 3. Control scheme of the hysteresis droop controller. (1) The hysteresis regulator; (2) The hysteretic differentiator.

II. Hysteresis Droop Controller

In this section, the principle of the hysteresis droop controller is introduced. The control scheme of this controller is presented in Fig. 3. It consists of two loops, an inner voltage control loop and an external droop control loop. The voltage loop regulates the output voltage v_o to track its reference v_o^*. A first-order low-pass filter LPFv, which is usually needed in oversampling control approaches, is used to attenuate high-frequency noises. On top of the voltage loop, the droop loop is added to adjust the voltage reference v_o^* according to the output current i_o, achieving the droop function:

$$v_o^* = V_0 - i_o \cdot r_d \cdot G_{\text{LPFi}}(s) \tag{1}$$

where V_0 is the voltage set point under no-load condition, r_d is the droop coefficient, and $G_{\text{LPFi}}(s)$ is a first-order low-pass filter to slow down the rate of change of v_o^* [12].

The hysteresis regulator, as shown in the dashed box in Fig. 3, distinguishes the hysteresis droop controller from others. It is constructed on the basis of a hysteretic differentiator and a Proportional-Integral (PI) controller. These two elements are responsible for rapid dynamic response and zero steady-state error, respectively. Details of these two components are discussed below.

A. Hysteretic differentiator

The hysteretic differentiator, which is composed of a comparator and an integrator, is the heart of the proposed control method, as illustrated in Fig. 3. In fact, this hysteretic differentiator emulates the behavior of a derivative term, providing leading phase for the voltage loop gain and ensuring fast dynamic response.

The relevant waveforms are displayed in Fig. 4 to show the operation principle. The switching signal $S(t)$ is generated by

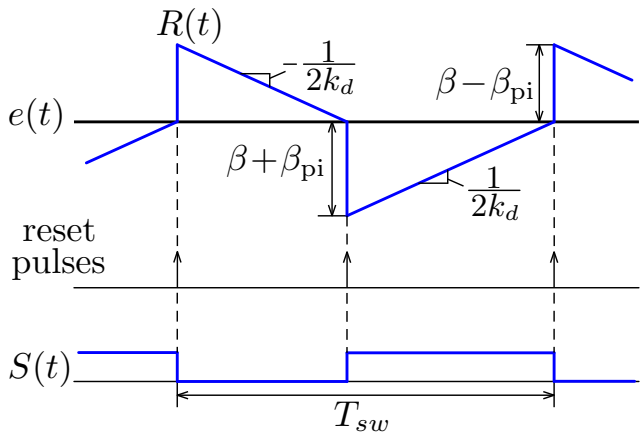

Fig. 4. Operation principle of the hysteresis droop controller.

comparing the error signal $e(t)$ and the ramp state $R(t)$, and it has two possible states, 0 and 1.

$$S(t)=\begin{cases}0, & \text{if } e(t)<R(t)\\ 1, & \text{else}\end{cases} \tag{2}$$

In terms of $R(t)$, it is ramped down at a slope of $-1/2k_d$ when $S(t)=0$, while it is ramped up at a slope of $1/2k_d$ when $S(t)=1$. At the moment that $R(t)$ crosses $e(t)$, $R(t)$ is reset. The reason to implement this reset action will be explained later. By choosing proper control parameters, $R(t)$ would oscillate around $e(t)$ within a certain hysteresis band, as can be seen in Fig. 4.

An approximated small-signal model of the hysteretic differentiator is derived as below. Let us approximately assume that $e(t)$ has the same average value as $R(t)$, which is a common supposition in the analysis of hysteresis loops. Then, there is:

$$\hat{e}(s)\approx\hat{R}(s)=\frac{\hat{S}(s)}{sk_d}\quad\Rightarrow\quad\hat{S}(s)\approx\hat{e}(s)\cdot sk_d \tag{3}$$

It is clear that the hysteretic differentiator behaves like a traditional differentiator in the sense of small signal. From the perspective of large-signal variations, the hysteretic differentiator shows nonlinear actions which improve the transient response.

This hysteretic differentiator also stabilizes the switching frequency, which is accomplished by the *reset* block in Fig. 3. When a rising edge is detected in $S(t)$, $R(t)$ is reset downward by $\beta+\beta_{\rm pi}$, where β is a constant value and $\beta_{\rm pi}$ is the output of the PI controller. On the other hand, when a falling edge is detected in $S(t)$, $R(t)$ is reset upward by $\beta-\beta_{\rm pi}$. Therefore, the switching frequency is only decided by the total hysteresis window height, which is equal to 2β, and the slope of $R(t)$, which is equal to $1/2k_d$. As a consequence, the switching frequency is fixed in steady state and can be expressed as:

$$f_{sw}=1/(4\beta k_d) \tag{4}$$

It should be noticed that, (4) is based on the condition that $e(t)$ and $\beta_{\rm pi}$ have negligible variations in one switching cycle. Otherwise, (4) no longer holds.

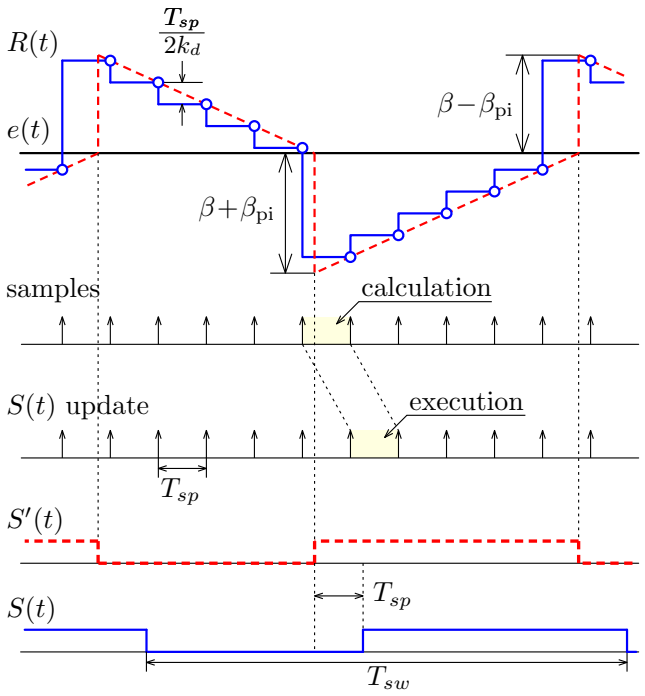

Fig. 5. Operation principle of the hysteresis droop controller in DSP implementation. $R(t)$ emulates the analog waveform, and the actual switching signal $S(t)$ is delayed for one sampling period T_{sp} compared to the ideal one $S'(t)$.

B. PI controller

A PI controller is adopted here to force the output voltage v_o to follow its reference value v_o^* in steady state. Its output $\beta_{\rm pi}$ is used to adjust the relative position of $R(t)$ and $e(t)$. For example, considering the case that v_o is smaller than v_o^*, $e(t)$ is larger than zero. Then, under the function of the PI controller, $\beta_{\rm pi}$ increases. The position of $R(t)$ moves downward relative to $e(t)$, which means that more time is allocated to the switching state $S(t)=1$. In such a case, v_o increases until reaching v_o^*.

III. DSP IMPLEMENTATION

The operation waveforms shown in Fig. 4 can only be realized in analog implementation. When migrated to digital platform, the operation principle changes. In this section, the implementation of the hysteresis droop controller having one sample delay is discussed.

A marked difference between analog and digital implementation is that the sampling frequency in digital implementation is finite and limited by the analog-to-digital conversion time and the computation time. Especially, when applied to DSP-based control system, computation takes a significant amount of time. Fig. 5 depicts the key waveforms of the digital hysteresis droop controller. As can be seen, $R(t)$ becomes a series of discrete points instead of a smooth curve. Importantly, $R(t)$ should be updated in a way that every point is located on the continuous curve, so that the digital controller's behavior exactly follows the analog one.

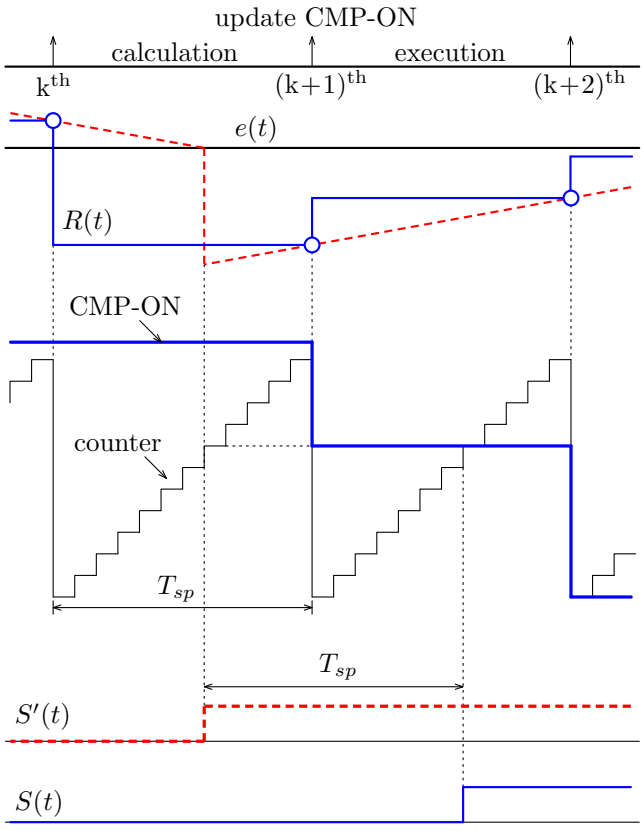

Fig. 6. The switching signal $S(t)$ is generates by comparing a counter clocked at the system frequency and a variable CPM-ON, for the purpose of enhancing the resolution.

Another phenomenon which should be noticed is that the DSP implementation induces non-negligible calculation time. In this case, registers that decide the switching actions are updated one sampling period T_{sp} after the corresponding sampling instant. As a result, the actual switching signal $S(t)$ is delayed for one T_{sp} compared to the ideal one $S'(t)$. The influence of this additional delay will be studied in Section IV by simulation results.

The switching actions are directly decided by the hysteresis droop controller without any modulator. However, the controller operates at the sampling frequency, which is only several times of the switching frequency. Thus, the switching actions should not be synchronized by the sampling frequency. Otherwise, the resolution of duty cycle is too low. For instance, if the sampling frequency is 10 times of the switching frequency, the synchronized duty cycle has a resolution of 10 %. To solve this problem, a counter clocked at the system frequency is generated inside DSP and is exploited to trigger the sampling and to increase the resolution, as shown in Fig. 6. At the k^{th} instant, the voltage and currents are acquired and processed in the following sampling period. The moment when $R(t)$ crosses $e(t)$ is predicted, and the required compare value CMP-ON is calculated so that it intersects with the counter at the same moment. Then, at the $(\mathrm{k}+1)^{\mathrm{th}}$ instant, CMP-ON is updated and the switching state is changed in the following

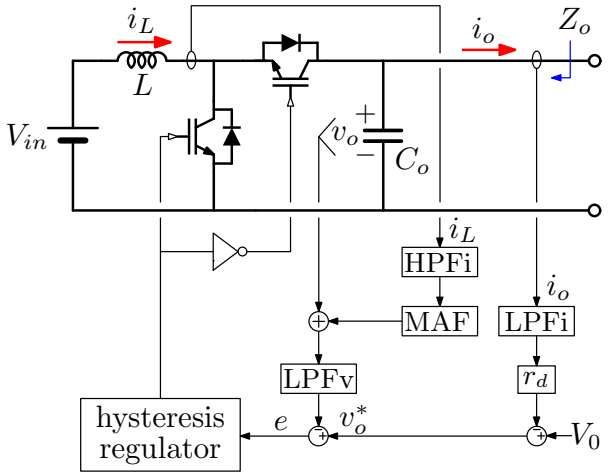

Fig. 7. The boost-type DER converter considered in simulation with the hysteresis droop controller. The structure of the hysteresis regulator can be found in Fig. 3.

sampling period. Inevitably, the real switching signal $S(t)$ shows one sampling period delay compared with the ideal signal $S'(t)$.

IV. Simulation Results

To verify the effectiveness of the hysteresis droop controller, a model of boost-type DER converter is built in Matlab/Simulink. The control scheme is presented in Fig. 7. Compared to the control structure in Fig. 3, the model considered in simulation takes the inductor current i_L as an additional feedback signal. This is a particular modification only for the boost converter to suppress the effect of the right-half-plane zero. A high-pass filter HPFi and a moving average filter MAF are inserted into the path to remove the dc component and the switching ripple, respectively. The system parameters are reported in Table I. The nominal power is 3 kW and the output capacitance is only 50 µF. The acceptable range for the output voltage is from 360 V to 400 V. The nominal switching frequency f_{sw} is 20 kHz and the sampling frequency f_{sp} is fixed at 200 kHz, which is ten times more than f_{sw}.

A. Effect of one sampling period delay

The effect of the one sampling period delay introduced by the DSP implementation is studied herein, by evaluating the open voltage loop gain $T_{\mathrm{v}}(s)$, which is expressed as:

$$T_{\mathrm{v}}(s)=\frac{G_{\mathrm{Li}}(s)r_d\cdot\hat{i}_o+G_{\mathrm{Lv}}(s)[G_{\mathrm{Hi}}(s)G_{\mathrm{M}}(s)\cdot\hat{i}_L+\hat{v}_o]}{\hat{e}} \quad (5)$$

where $\hat{e}$ is the error signal marked in Fig. 7. The frequency response of $T_{\mathrm{v}}(s)$ is measured in simulation by injecting small-signal sinusoidal perturbations at different frequency points. Cases with and without the time delay are both evaluated. The measurement results are shown in Fig. 8. The voltage loop has a crossover frequency of 3500 Hz, which is around $1/6$ of the switching frequency. Although the time delay introduced by the DSP implementation brings a lagging phase of $-10°$, the phase margin is still as large as $74°$. Therefore, from the

TABLE I
SYSTEM PARAMETERS

Parameter	Symbol	Value
Input voltage	V_{in}	200 V
Nominal bus voltage	V_o	380 V
Nominal Power	P_n	3.0 kW
Inductance	L	1.0 mH
Output capacitance	C_o	50 µF
Switching frequency	f_{sw}	20 kHz
Sampling frequency	f_{sp}	200 kHz
Droop coefficient	r_d	2.53 V/A
Cutoff frequency of LPFi	ω_{Li}	$2\pi \cdot 100$ rad/s
Cutoff frequency of HPFi	ω_{Hi}	$2\pi \cdot 300$ rad/s
Cutoff frequency of MAF	ω_{M}	$2\pi \cdot 20000$ rad/s
Cutoff frequency of LPFv	ω_{Lv}	$2\pi \cdot 20000$ rad/s
Proportional gain of PI	k_p	0.35
Integral gain of PI	k_i	0.0015
Ramp slope	k_d	0.45
Hysteresis window height	β	5.56

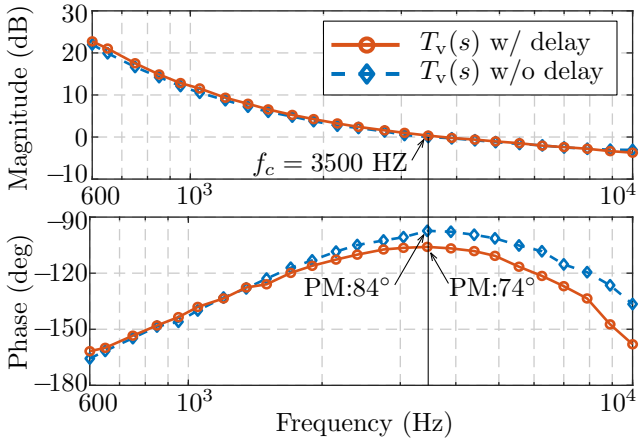

Fig. 8. The open-loop gain $T_v(s)$ with and without the one sampling period delay.

point of view of small-signal stability, the influence of the one sampling period delay is acceptable.

B. Output impedance measurement

The output impedance Z_o of the boost-type DER converter with the hysteresis droop controller is measured in simulation, by stimulating the system at different frequency points. The measurement result is shown in Fig. 9. A magnitude valley appears around 200 Hz. Below this frequency, v_o follows its reference v_o^*, and Z_o is dominated by the droop function (1). The overall magnitude of Z_o is equal to or lower than the droop coefficient r_d in full frequency range. Hence, from small-signal perspective, the output voltage stays within the allowable range when facing a load change.

C. Steady-state simulation result

The steady-state waveforms under nominal load are presented in Fig. 10. The output voltage v_o is stably regulated

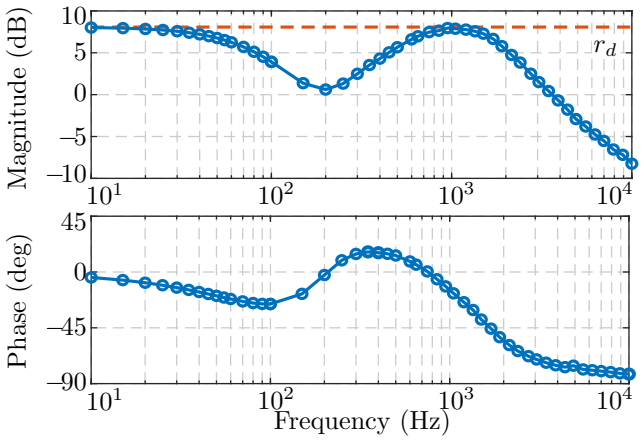

Fig. 9. Measured output impedance Z_o of the boost-type DER converter with the hysteresis droop controller.

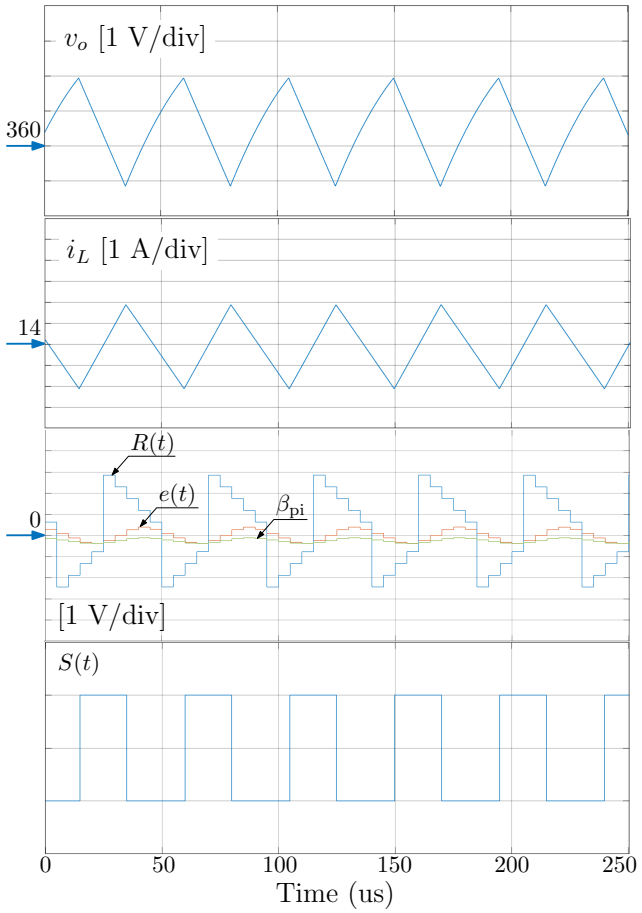

Fig. 10. Steady-state simulation result of the boost-type DER converter with the hysteresis droop controller.

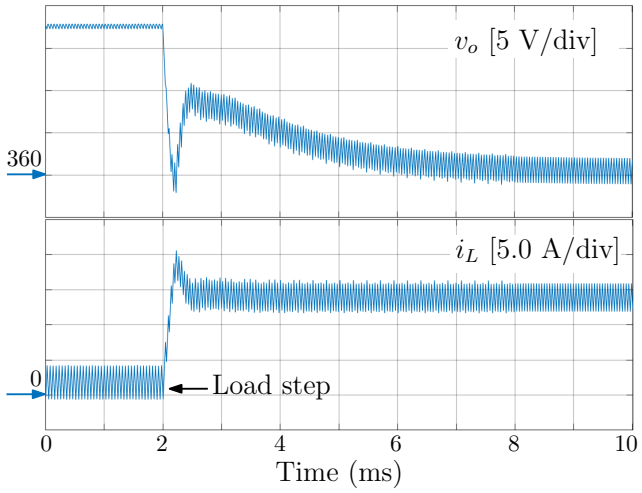

Fig. 11. Dynamic simulation result of the boost-type DER converter with the hysteresis droop controller.

and shows a switching ripple of 3 V, which is about 0.8% of the nominal value. The inductor current i_L has a switching ripple of 4 A, accounting for 30% of the nominal value. Due to these switching ripples, the error signal $e(t)$ is not constant in steady-state and presents switching-frequency fluctuation, which is about 15% of the ramp height. Regardless of the switching ripple in $e(t)$, the switching signal $S(t)$ still has a constant duty cycle. However, the actual switching frequency is affected and is 1.1 times as much as the nominal one. In order not to further amplify the switching ripple, the derivative gain (i.e., the ramp slope k_d) cannot be increased any more. It is worth mentioning that the nominal load condition is the worst case since v_o has a largest switching ripple.

D. Dynamic simulation result

The dynamic waveforms in case of a load change are displayed in Fig. 11. Remarkably, when load steps from 10% up to 100%, the average value of v_o is not lower than 360 V during transient and is strictly confined to the acceptable range.

V. Experimental Results

To experimentally demonstrating the performance of the hysteresis droop controller, a 3 kW boost-type DER converter, which is exactly the same as Fig. 7, is setup. The system parameters are listed in Table I. The DSP utilized in this prototype is TMS320F28379D, with a system clock frequency of 200 MHz.

The dynamic experimental results, in case of load step up and step down, are depicted in Fig. 12 and Fig. 13, respectively. Notably, in both cases, v_o does not present any overshoot or undershoot during transient, verifying the feasibility of the hysteresis droop controller. Moreover, in steady state, v_o and i_L present little fluctuations, which means that the proposed controller is not amplifying the sample noises due to the oversampling operation. This characteristic is obtained, in our case, by the low-pass filters, especially LPFv, used in the controller.

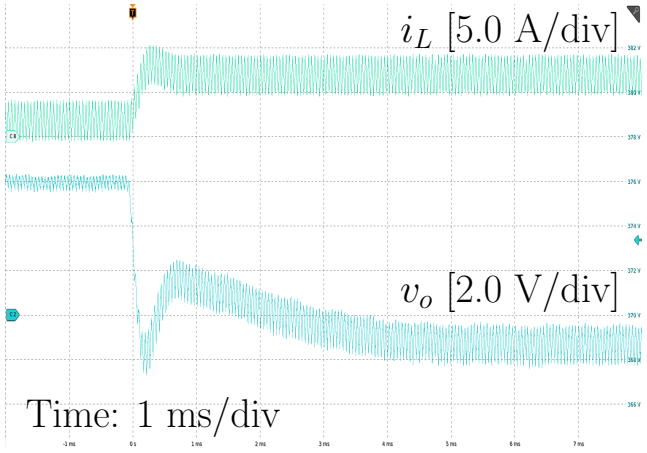

Fig. 12. Load step-up experiment result of the boost-type DER converter with the hysteresis droop controller. v_o offset: 370 V.

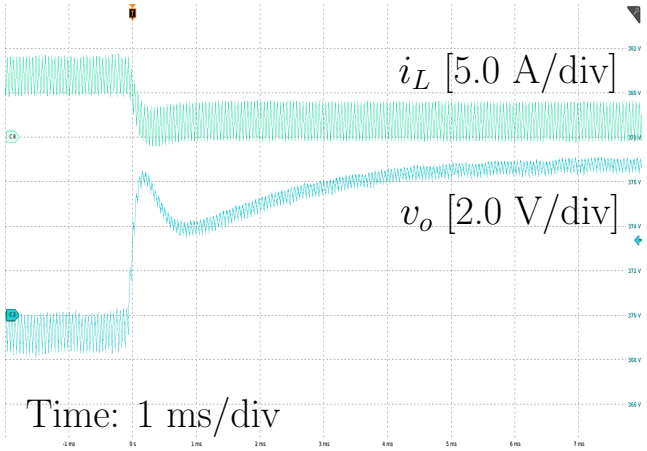

Fig. 13. Load step-down experiment result of the boost-type DER converter with the hysteresis droop controller. v_o offset: 370 V.

VI. Conclusion

This paper presents the digital application of the hysteresis droop controller on DER converters in DC mcirogrids. This controller removes the PWM modulator used in the traditional PID controller, so the time delay in the voltage control loop is reduced. As a consequence, the loop bandwidth can be further increased, for example, it is designed at 1/6 of the switching frequency in this paper. Moreover, the proposed controller features nonlinear behaviour in case of large-signal perturbations, speeding up the large-signal dynamic response. Thanks to these two advantages, the hysteresis droop controller reduces the output voltage variations under load changes. In such a case, a small output capacitance can be used while always keeping the output voltage within the tolerance band. This control method is implemented on a DSP-based 3 kW boost-type DER converter with a sampling frequency of 200 kHz. Although the DSP implementation brings one sampling period delay, it does not shows a relevant influence on the small-signal stability. Simulation and experiment results validate the feasibility of the proposed controller.

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