Single Event Upsets Induced by Direct Ionization from Low-Energy Protons in Floating Gate Cells

Marta Bagatin, Simone Gerardin, Alessandro Paccagnella, Angelo Visconti, Ari Virtanen, Heikki Kettunen, Alessandra Costantino, Véronique Ferlet-Cavrois, and Ali Zadeh

***Abstract*— Floating gate cells in advanced NAND Flash memories, with single-level and multi-level cell architecture, were exposed to low-energy proton beams. The first experimental evidence of single event upsets by proton direct ionization in floating gate cells is reported. The dependence of the error rate versus proton energy is analyzed in a wide energy range. Proton direct ionization events are studied and energy loss in the overlayers is discussed. The threshold LET for floating gate errors in multi-level and single-level cell devices is modeled and technology scaling trends are analyzed, also discussing the impact of the particle track size.**

***Index Terms*— Flash memories, floating gate devices, protons, single event effects.**

I. Introduction

THE miniaturization of transistors dictated by Moore's law is making electronic chips more and more sensitive to external disturbances, among which the effects of ionizing radiation, in particular Single Event Upsets (SEUs). The threshold LET for heavy-ion induced upsets in CMOS technology is decreasing as the device dimensions are scaled down and bit flips from proton direct ionization have been reported on 65-nm SOI latches and SRAM cells for the first time in 2007 by IBM researchers [1], [2]. Today the effects of low-energy protons are a hot topic: the importance of these particles as a potentially relevant source of errors in space has been recently highlighted [3] and the criticalities of the related testing have been discussed in literature [4], [5].

NAND Flash memories, using charge-based Floating Gate (FG) cells, are among the most aggressively scaled technologies in the semiconductor market and the leading solution for non-volatile storage. In addition, these chips are extremely attractive for space designers, to store large amounts of information on satellites and spacecrafts [6], due to the lack of rad-hard memories able to match the features of commercial NAND Flash, in terms of memory size and performances.

Manuscript received July 7, 2016; revised September 12, 2016; accepted October 24, 2016. Date of publication December 8, 2016; date of current version February 28, 2017. This work was supported in part by ESA under contract 4000103347/11/NL/PA. *(Corresponding author: Marta Bagatin.)*

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Digital Object Identifier 10.1109/TNS.2016.2637571

Unfortunately, Flash memories are not immune from the effects of ionizing radiation. In old technologies (about one decade ago), single event upsets due to heavy-ion strikes on FG cells could happen only at very high LET values [6]. Then, the threshold LET for FG errors has been decreasing more and more, as the cell size has been shrunk and the number of electrons on which FG transistors rely has become smaller and smaller [7], [8]. The first Flash device that was reported to be sensitive to alpha particles was a 50-nm MLC NAND Flash [8], [12], whereas, to our knowledge, SLC NAND Flash have not yet reported to be sensitive to alphas (down to the 34-nm node) [13].

Several papers have been published during the last decade on the effects of the recoils induced by high-energy protons on FG cells [14], [15]. Leaving aside the effects on the peripheral circuitry, the main conclusions are that the dependence of FG error cross section on proton energy may be significantly different depending on the studied devices. A FG error rate increasing with proton energy was observed in 34-nm SLC devices, whereas the opposite was reported for 25-nm MLC devices [14]. Possible reasons for this difference were attributed to the different LET and angular distributions of proton-induced secondaries, combined with different device responses to heavy ions. However, still no evidence has been reported on single event upsets induced in FG cells by low-energy protons.

The purpose of this work is to analyze the response of state-of-the-art NAND Flash memories to low-energy protons, understanding if, and to what extent, these devices are sensitive to proton-direct-ionization induced SEUs. The trends with proton energy are studied in a wide range of energies, the mechanisms are elucidated, the threshold LETs are modeled, and predictions for future technologies are discussed.

The paper is organized as follows: details on the experimental set up and irradiations are described in Section II. Experimental results on proton error rates are discussed in Section III. Section IV presents the analysis, simulations, and modeling focused on direct ionization events and threshold LET evolution with technology scaling. Finally, Section V concludes the paper.

II. Devices and Experimental Details

For this work we used 25-nm NAND Flash memories with Single-Level Cell (SLC) and 2-bits-per-cell Multi-Level Cell (MLC) architecture, all manufactured by Micron Technology, with part numbers MT29F32G08ABAAAWP and

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TABLE I
NAND FLASH MEMORIES STUDIED IN THIS WORK

Part number	Package marking	Die marking	Organization	Node [nm]	Size [Gbit]
MT29F32G08ABAAAWP	I306 2-2	N/A	SLC	25	32
MT29F32G08CBACAWP	I352 I-7	Intel L73A 2009 AC	MLC	25	32

TABLE II
DETAILS ON PROTON BEAMS USED FOR THIS WORK

Energy [MeV]	Surface LET [MeVcm^2/mg]	Range [µm]	Facility
0.6	0.23	7.75	RADEF
0.8	0.2	8.69	RADEF
1	0.18	9.67	RADEF
1.2	0.16	11.74	RADEF
1.5	0.14	13.97	RADEF
4	0.07	148.4	TANDEM
7	0.05	383.1	TANDEM
29.5	-	4760	TSL
44.4	-	9860	TSL

MT29F32G08CBACAWP, respectively. The parts were bought on the open market. A description of the studied devices is summarized in Table I.

Irradiations with protons in different energy ranges and in the following facilities were performed: RADEF facility at the University of Jyväskylä, Finland; TANDEM accelerator at Uppsala University, Sweden; The Svedberg Laboratory, TSL, Sweden. The features of all the proton beams used for this work are detailed in Table II.

At RADEF, irradiations were performed in vacuum and the plastic package was etched to allow the particles to penetrate into the active region. At the TANDEM accelerator at Uppsala University, exposures were also performed in a vacuum chamber on delidded samples. On the contrary, irradiations at TSL with protons at higher energies were carried out in air on packaged samples. In all cases the beam was delivered perpendicularly to the chip surface and all irradiations were performed at room temperature.

Before exposure, MLC samples were programmed with FG cells equally distributed in the four levels (L0, L1, L2, and L3) and the SLC samples were programmed with all the cells in the program level ('0', i.e., L1). All irradiations were carried out on unbiased devices, as the purpose of this work was to study effects in FG cells. For all irradiation runs, proton fluences were carefully chosen in order to minimize the delivered total ionizing dose (these samples are quite sensitive to TID effects [16]) and, at the same time, to hit a significant number of FG cells in the memory array. After irradiation, the memories were read again and the number of floating gate errors was recorded together with their address location. When needed, reference, non-irradiated samples were also kept to evaluate the error rate due to extrinsic and intrinsic mechanisms different from radiation.

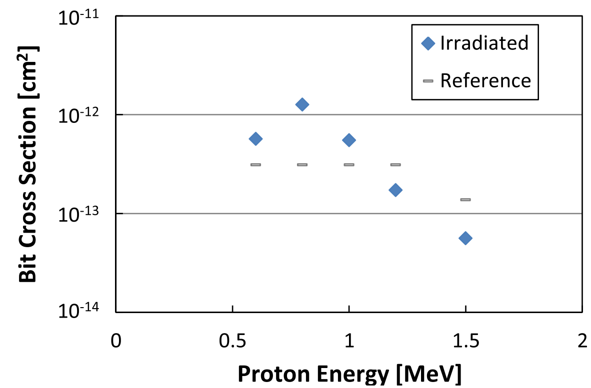

Fig. 1. FG error bit cross section (averaged on all four levels) versus energy for 25-nm MLC NAND Flash memories irradiated with low-energy protons at RADEF. The cross section for errors not due to radiation in reference devices is also shown (calculated as the number of errors divided by the fluence received by the part irradiated at the corresponding energy and by the number of irradiated bits). Error bars are smaller than the symbols.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Low-energy (0.6-1.5 MeV) protons

The low-energy proton experimental campaign was carried out at the RADEF facility, exposing MLC and SLC NAND Flash devices in unbiased conditions to proton beams with energies 0.6-1.5 MeV. Remarkably, in 25-nm MLC memories, some proton-induced errors were detected after irradiation. Fig. 1 shows the bit cross section for FG errors as a function of proton energy, averaged on all four levels. The devices were measured a few days after irradiation, so the cross section for errors in reference, non-irradiated devices, programmed and read at the same time as irradiated samples, is also shown. Cross sections for reference devices were calculated as the number of errors divided by the fluence received by the part irradiated at the corresponding energy and by the number of irradiated bits. Note that the cross section for reference devices is not the same for all energies because different fluences were used. For all experimental points in Fig. 1, error bars (calculated considering a Poisson process at one standard deviation) are smaller than the symbols.

Total dose effects can be certainly ruled out as the cause for FG errors in Fig. 1, as in all irradiation runs the memories only received few rad(Si). In fact, errors due to TID in these samples show up above 15 krad(Si) [16].

Probability calculations show that, with the used proton fluence, the number of double strikes on a single FG cell is negligible: overall, $3 \cdot 10^{10}$ bits were measured and only 0.0006% cells received double strikes, i.e. 2 or 3 cells in total, whereas the number of observed errors is in the order of several thousands. This is evidence that FG cells in 25-nm NAND MLC are sensitive to SEUs by proton direct ionization. The direct ionization induced by protons produces a shift in the cell threshold voltage (V_{th}), which is large enough to result in a bit flip. As seen in Fig. 1, the energy at which the effect is maximum is 0.8 MeV, whereas protons with energy 0.6 MeV and 1 MeV or larger induce negligible effects, or at least below our observation threshold (i.e., upsets generated by protons may be covered by errors due to other mechanisms

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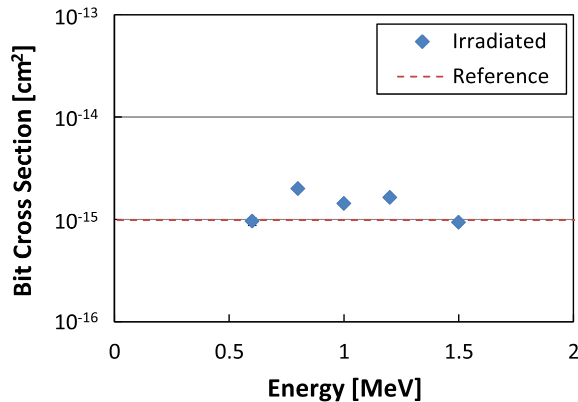

Fig. 2. FG error bit cross section (for programmed cells) versus energy for 25-nm SLC NAND Flash memories irradiated with low-energy protons at RADEF. The cross section for errors not due to radiation in reference devices is also shown.

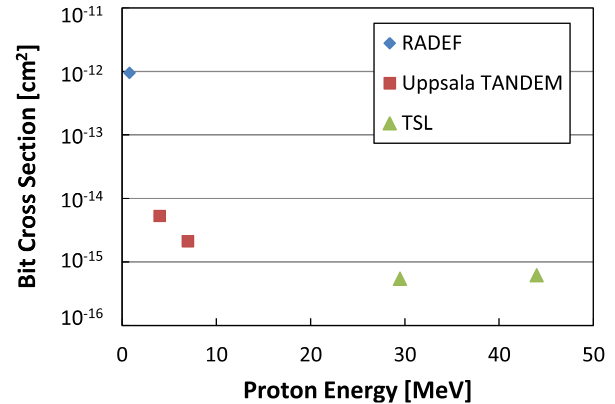

Fig. 3. FG error bit cross section (averaged on all four levels) versus energy for 25-nm MLC NAND Flash memories irradiated with protons at RADEF, Uppsala University, and TSL.

not related to radiation, such as random telegraph signal noise, read disturb, etc. [17]).

Different from MLC devices, in 25-nm SLC NAND Flash samples no errors attributable to low-energy protons were observed after irradiations at the RADEF facility. This is shown in Fig. 2: although a slight increase (less than a factor of 2) in the error rate is observed in samples irradiated with 0.8-MeV protons, the increase is too small to be attributed to radiation. We therefore conclude that, for SLC 25-nm samples, the V_{th} shift induced by proton direct ionization in this energy range is not high enough to generate raw bit FG errors.

B. Middle-energy (4-7 MeV) and high-energy (29-44 MeV) protons

The middle-energy proton irradiation campaign was performed at the TANDEM accelerator at Uppsala University, with 4-MeV and 7-MeV protons. In this case, different from the samples irradiated at RADEF, the memories were measured only few minutes after the exposure, so reference devices are not needed because errors not due to radiation were measured prior to the exposure and subtracted afterwards (and they do not change significantly in few minutes).

The cross section for FG errors in 25-nm MLC samples is shown in Fig. 3 with squares. In the same plot, the TANDEM data are compared with RADEF data at lower energies (diamonds) discussed in the previous section, after removing FG errors not due to radiation. As seen in Fig. 3, the FG error cross sections for samples exposed to 4-MeV and 7-MeV protons are significantly lower (2-3 orders of magnitude) than those exposed to the lowest energies, but still relevant. Because of the much higher fluence used (up to $2.5 \cdot 10^9$ p/cm^2), the total dose delivered during the TANDEM irradiation is larger than at RADEF. The TID in Silicon delivered during our experiments as a function of proton energy is illustrated in Fig. 4. Different from the doses delivered with low-energy protons at RADEF, for 4-MeV protons and higher energies the doses exceed 1 krad(Si). However, these doses are still too low to induce FG errors in these samples, at least after gamma ray exposure [16], [18]. This opens the door to two possible scenarios:

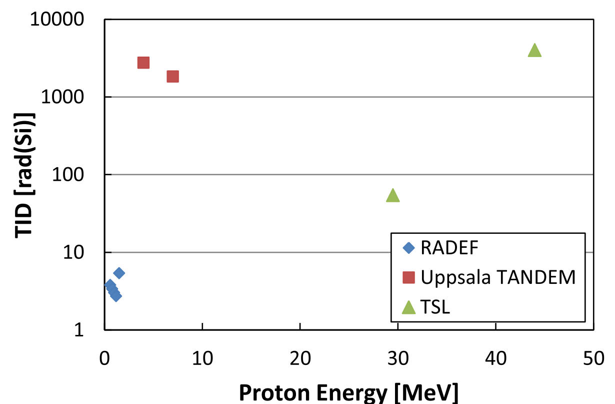

Fig. 4. TID delivered during proton irradiations as a function of energy.

(i) either the memories are sensitive to indirect proton ionization down to energies smaller or equal to 4 MeV;
(ii) or the observed errors are the results of multiple strikes on the same FG cells.

The results of irradiations with protons at even higher energies can be helpful to evaluate the first possibility. Fig. 3 also shows the FG error cross section for 25-nm MLC samples exposed to protons with energies up to 44 MeV. As seen, at 29 MeV and 44 MeV, where the errors are due to proton indirect ionization, the bit cross section is in the order of 10^{-16} cm^2. Based on these values, it is extremely unlikely that protons at 4 and 7 MeV may induce indirect ionization with a cross section one order of magnitude larger than that induced by 44-MeV protons [19].

Let us now examine the second hypothesis, i.e. multiple strikes. With the fluences used for 4- and 7-MeV proton irradiations ($2.5 \cdot 10^9$ p/cm^2) and the size of the cells, probability calculations show that about 0.78% of the cells have been hit twice. This results in a number of double strikes about one order of magnitude larger than the number of FG errors after irradiation, compatible with the fact that one proton strike is not enough to produce an observable effect. Therefore we can conclude that multiple strikes may be necessary to induce a bit flip. We can imagine that, depending on the initial V_{th} of

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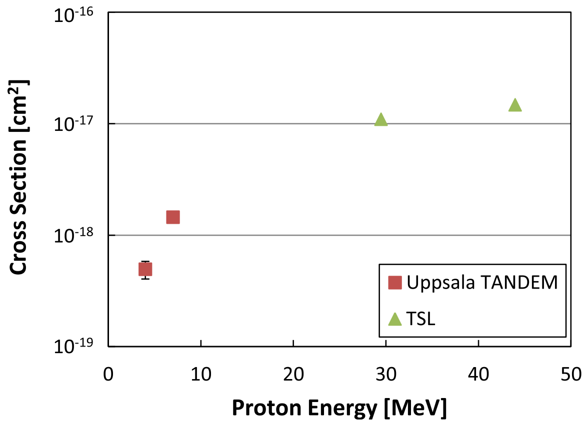

Fig. 5. FG error bit cross section (for programmed cells) versus proton energy for 25-nm SLC NAND Flash memories irradiated with protons at Uppsala University and TSL.

the cell, the shift induced by two 4-MeV proton hits on that same cell can or cannot bring the V_{th} below the read voltage, causing or not a FG error. This leads us to conclude that 4-MeV and 7-MeV protons are not able to induce SBUs in this 25-nm MLC NAND technology.

Concerning 25-nm SLC devices, protons at 4 MeV and above are able to induce FG errors, which cross sections are illustrated in Fig. 5, for devices irradiated at Uppsala TANDEM and TSL facilities. The values for the FG cross sections are smaller than those of MLC devices (Fig. 3) and, even more interesting, we observe an opposite trend as a function of proton energy: whereas for MLC samples the cross section decreases going from 7 MeV to 29 MeV, for SLC it increases. This behavior can be attributed to the larger error margins in SLC: two hits, even three hits, on the same cell are not enough to induce a shift able to bring the cell below the read margin (cumulative effect). The errors induced by protons at 7 and 4 MeV are compatible with proton indirect ionization, with a nuclear reaction cross section decreasing about 1 order of magnitude with respect to 29 MeV, in agreement with nuclear reaction cross sections in [19]. We note that this indirect ionization component is likely present also in MLC samples, but it is masked by the multiple strikes we discussed before. The SLC error rates are also in line with data for 34-nm SLC devices tested at PIF facility with high-energy protons [14]. Also in [14], increasing (for 34-nm SLC) and decreasing (for 25-nm MLC) trends of proton cross sections versus energy were observed at higher energies; these different behaviors were attributed to different LET and angular distributions of proton-induced secondaries, together with the different heavy-ion responses.

IV. Analysis and Modeling

In the rest of the paper we will focus on the lowest part of the energy range, i.e., on protons with energies below 2 MeV, to better study the proton-direct-ionization component.

A. TRIM and SRIM simulations

To properly evaluate the energy loss in the chip overlayers above the FG electrode, we performed TRIM simulations

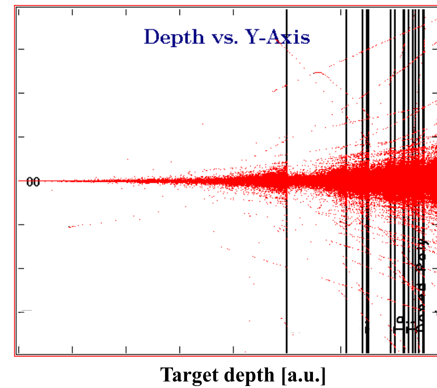

Fig. 6. Example of a TRIM simulation for 0.8-MeV protons crossing the stack above the floating gate electrode.

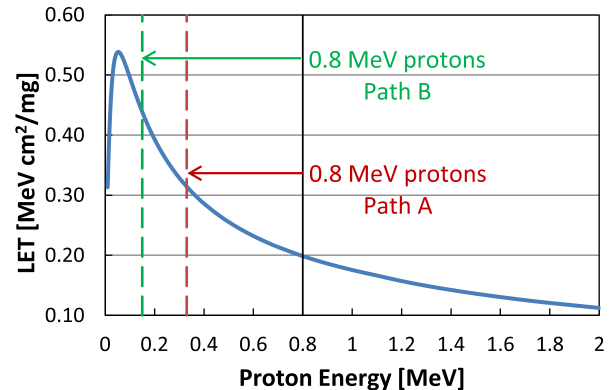

Fig. 7. LET as a function of energy for protons impinging on Silicon and visualization of the energy lost by 0.8-MeV protons reaching the FG through two different paths. Protons travelling through Path B cross two metal layers more than Path A. Data were obtained through TRIM simulations.

using an approximate cell structure. Fig. 6 illustrates an example run, simulating 10^4 protons with energy 0.8 MeV, impinging on a FG cell and crossing the overlayers located above the floating gate electrode. For 0.8-MeV and higher energies, practically all impinging protons reach the FG. On the contrary, for the lowest energy (0.6 MeV), the simulations highlight that a significant number of protons stop before reaching the active area; this explains why the error rate for 0.6-MeV protons is negligible.

Fig. 7 depicts the LET versus energy curve for protons impinging on Silicon. The Bragg peak is located around 0.06 MeV.

Let us now focus on the energy loss for 0.8-MeV protons, i.e., those inducing a large error rate in MLC samples. Different scenarios were simulated, depending on the path travelled by protons in the chip (e.g., how many metal layers they cross). This is relevant, as metal layers are not uniformly distributed on the surface of a chip. As seen in Fig. 7, 0.8-MeV protons may reach the FG with energy between 0.15 and 0.33 MeV, for Path A and Path B, respectively. Particles travelling through Path A cross two metal layers less than those travelling through Path B. These two paths were chosen to simulate the worst and best cases, as far as energy loss is concerned. Similarly, Fig. 7 shows the energy loss for 1-MeV protons, for different

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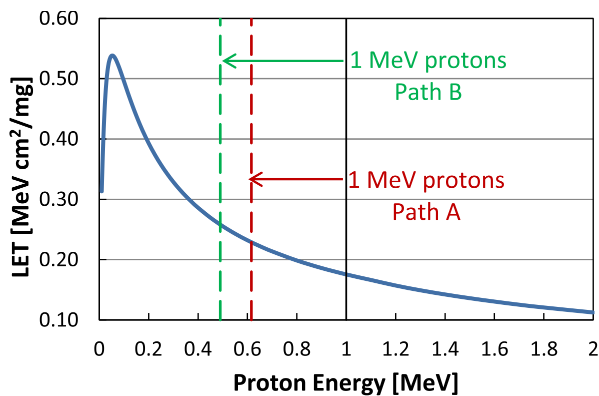

Fig. 8. Same as Fig. 7, but for 1-MeV protons reaching the FG through two different paths. Protons travelling through Path B cross two metal layers more than Path A.

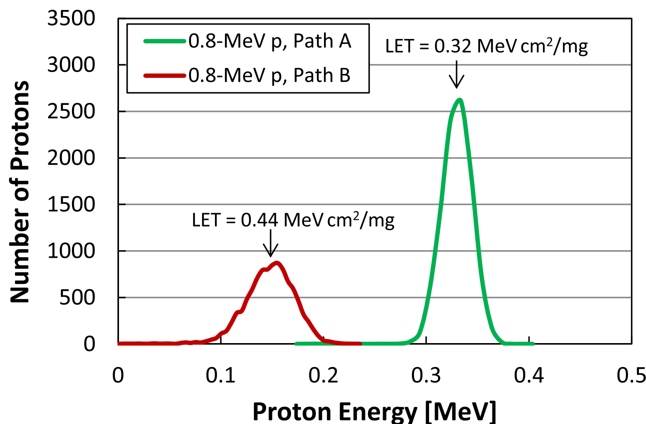

Fig. 9. Histogram of the energy of 0.8- MeV protons when they reach the FG through two different paths. Protons travelling through Path B cross two metal layers more than Path A.

stacks of materials crossed before reaching the FG. As 1-MeV protons did not induce a relevant number of errors in our MLC devices (see Fig. 1), Fig. 8 gives indications on the threshold LET.

It is also interesting to look at the energy spread of protons reaching the FG. Fig. 9 illustrates the energy distributions for 0.8-MeV protons reaching the FG through Path A and Path B (for a simulation run with 10^4 protons). As seen, the energy of protons travelling through Path B is more spread with respect to those travelling Path A. Remarkably, these differences in the travelled paths may lead to protons reaching the active area with LET values that may differ up to 50%. This highlights that care is needed when evaluating SEU from proton direct ionization and predicting the corresponding error rate in space, as already shown in recent papers [3]–[5]. When possible, the physical removal of layers above the sensitive region would be of course the ideal solution [4], but also simulations can greatly help to gain insight into energy loss in the overlayers, if details on the die stack are available.

Similar considerations were applied to alpha particles emitted by an Americium source. Based on the results of TRIM simulations, the LET of alphas reaching the FG (relevant to find the threshold LET for SLC NAND Flash samples) was determined.

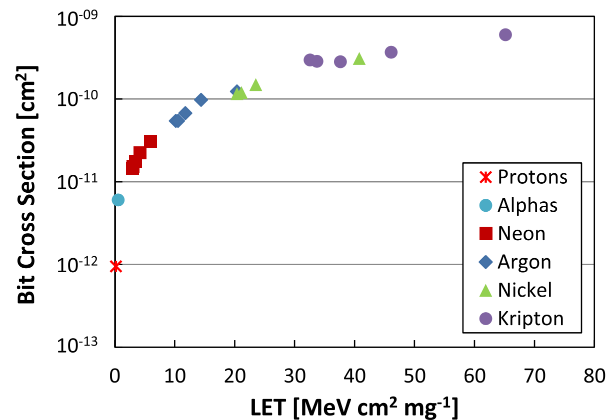

Fig. 10. FG error bit cross section versus LET for 25-nm MLC Flash NAND cells irradiated with 0.8-MeV protons (RADEF), heavy ions (HIF), and alpha particles (Am source). Different points for the same ion species were obtained varying the angle of incidence.

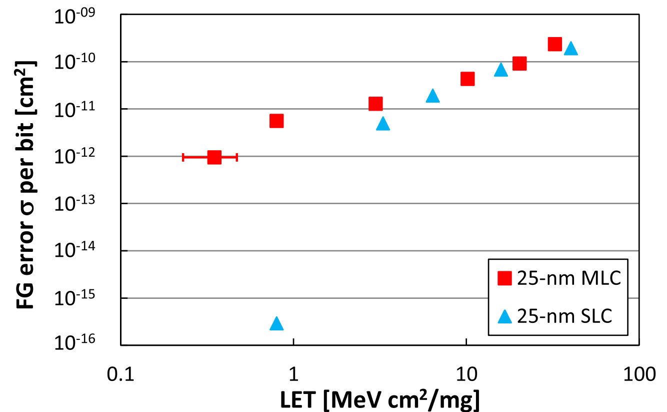

Fig. 11. FG error bit cross section versus LET in a log-log scale, for 25-nm Flash NAND cells (MLC and SLC) irradiated with protons (RADEF), heavy ions at normal incidence (HIF), and alpha particles (Am).

B. Threshold LET evolution with scaling

Now that we discussed energy loss and LET variation for low-energy protons, it is interesting to plot proton data together with heavy-ion ones [20].

Fig. 10 plots the heavy-ion FG error cross section per bit versus LET, in a log-lin scale, for 25-nm MLC NAND Flash devices irradiated at both normal incidence and tilted angles. The cross section at the lowest LET obtained with RADEF 0.8-MeV protons nicely fits the heavy-ion Weibull cross section curve.

To better study the part at very low LET, Fig. 11 plots the FG error cross section in a log-log scale. The horizontal error bar for the lowest LET point (0.8-MeV protons), based on the analysis in the previous section, is observable in the graph and it highlights the LET spread of protons reaching the FG electrode.

Cross sections are also plotted for 25-nm SLC NAND samples, with the point at the lowest LET obtained with alpha particles (LET ~0.8 MeV cm^2/mg). Remarkably, 25-nm node is the first SLC NAND technology node to be sensitive to alphas. As seen in Fig. 11, the trends are quite

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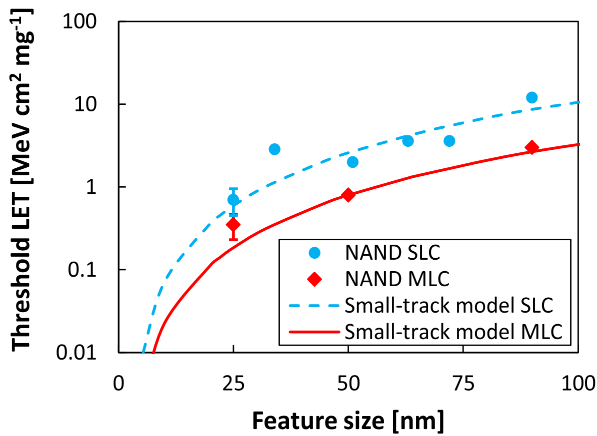

Fig. 12. Threshold LET as a function of the cell feature size, for MLC and SLC NAND Flash memories. The symbols illustrate experimental points (minimum LET at which FG errors were observed), whereas the lines show the LET_{th} model, considering a small track (<25-30 nm). Data for previous technology nodes were adapted from [8]–[11], [13].

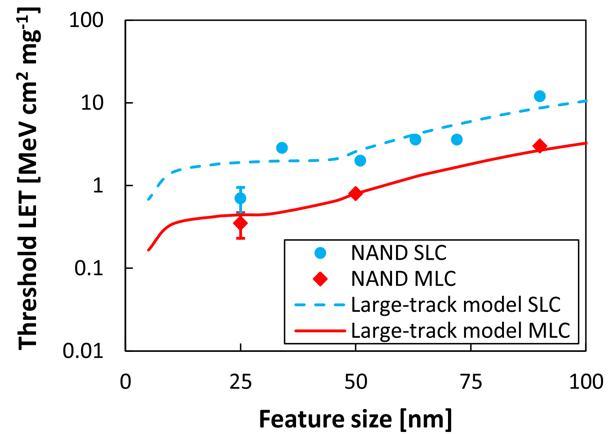

Fig. 13. Threshold LET as a function of the cell feature size, for MLC and SLC NAND Flash memories. The symbols illustrate experimental points (minimum LET at which FG errors were observed), whereas the lines show the model adapted to account for large ion tracks (>25-30 nm). Data for previous technology nodes were adapted from [8].

different for MLC and SLC devices in the low-LET region, whereas they tend to overlap for higher LET values (above 10 MeV cm^2/mg). This can be attributed to the fact that, as the saturation region is approached (this occurs at increasingly lower LET as the cell size is shrunk), the cross section tends to match the FG cell area, which is the same for SLC and MLC devices. Actually, we observe that the saturation cross section is well above (more than one order of magnitude) the FG area; in fact, it is not necessary that the particles pass through the FG to induce an error in these advanced technologies, as an ion strike outside the FG, and even outside the cell, may deposit enough charge (e.g., through delta electrons [21]) to shift enough the cell V_{th}, causing an error.

It is then relevant to study the threshold LET (LET_{th}) for FG errors. Experimental data on the LET_{th}, for both MLC and SLC arrays, are plotted with symbols in Fig. 12 as a function of the FG feature size, considering the LET_{th} as the lowest LET able to induce upsets during our irradiation experiments. Data on previous technology nodes are based on previous reports [8]–[11], [13]. As seen, LET_{th} values monotonically decrease as technology shrinks. The reason for this is that lower and lower values of charge deposited by ions are enough to induce FG errors, as less electrons are stored in programmed FGs with feature size reduction. MLC samples have a lower LET_{th} compared to SLC ones, due to the smaller error margins between adjacent levels. In other words, the same V_{th} shift (i.e., the same number of electrons lost from the FG electrode) induces a larger number of errors in MLC than in SLC devices.

It has been shown in previous works that the discharge of the FG can be modeled as the discharge of a Resistor-Capacitor (RC) network [8]. The resistance of the network is inversely proportional to the LET of the impinging ion, whereas the capacitance is proportional to the FG cell capacitance. Although different physical interpretations were proposed to describe the discharge of the FG [22], [23], we assume that the main driver for charge loss is the onset of a transient resistive leakage path across the tunnel oxide, temporarily connecting the FG and the channel, and acting immediately after a heavy-ion strike [24]. A direct measurement of this leakage path through the tunnel oxide is of course impossible, so assumptions have to be made about the duration of the transient conductive path, according to the estimations in [24]. Then, using an RC network to mimic the FG cell discharge, the LET_{th} can be calculated as a function of the cell feature size, as it is inversely proportional to the maximum resistance of the leakage path causing an error.

The model has also been refined to take into account the size of the ion track: if the track size is considerably larger than the FG (i.e. larger than 25/30 nm of radius), not all the charge generated by the ion strike might be collected by the cell [13].

The LET_{th} model predictions are compared with experimental data in Fig. 12 and Fig. 13, respectively, for the small-track model and for the large-track model, with a solid line for NAND with MLC architecture and a dashed line for those with SLC architecture.

As seen, there is not a clear answer on which of the two models better describes the experimental data. In fact, for 25-nm MLC samples, the small-track model better fits the lower limit of the error bar for the 0.8-MeV proton point, whereas the large-track model fits the upper limit of the error bar. Concerning SLC NAND Flash devices, small-track model predicts more accurately the experimental point obtained with alphas, with respect to the large-track model, which seems to slightly overestimate the LET_{th} for SLC 25-nm cells.

Based on the results of track size calculations with Monte Carlo methods, the radial extension of low-energy proton and alpha particle track [25] is expected to be smaller than that of more energetic heavy ions [26]. Therefore, from a theoretical point of view, the small-track model should apply.

The small-track model (Fig. 12) predicts that single-level cell NAND Flash memories should be sensitive to SEUs induced by proton direct ionization likely from a feature size of 16 nm.

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V. Conclusion

We showed the first experimental evidence that the latest generations of NAND MLC Flash memories have become sensitive to low-energy protons. In particular, 25-nm MLC NAND Flash memories show errors attributable to single event upsets induced by 0.8-MeV proton direct ionization. On the contrary, SLC NAND Flash cells in the same technology are still not sensitive to low-energy protons. The dependence of MLC and SLC device sensitivity on proton energy was analyzed in a broad energy range (up to 44 MeV) and the origin of the observed upsets was studied. To deepen the analysis of proton direct ionization, we then discussed the results of TRIM simulations and highlighted the uncertainty in the LET of particles reaching the floating gate. Based on the energies in the sensitive volume predicted by simulations, the threshold LET was then studied and modeled as a function of scaling, discussing the implications of considering particles with different track size for SLC and MLC devices. Concerning single level cell NAND Flash memories, 25-nm is the first node to be sensitive to alpha particles and our model predicts that SLC devices should be sensitive to SEU from proton direct ionization from a feature size of 16 nm.

Acknowledgments

The authors would like to kindly acknowledge Elke Passoth and Björn Gålnander from TSL for their invaluable support during proton irradiations in Uppsala facilities.

References

[1] D. F. Heidel *et al.*, "Low energy proton single-event-upset test results on 65 nm SOI SRAM," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3394–3400, Dec. 2008.

[2] K. P. Rodbell, D. F. Heidel, H. K. Tang, M. S. Gordon, P. Oldiges, and C. E. Murray, "Low-energy proton-induced single-event-upsets in 65 nm node, silicon-on-insulator, latches and memory cells," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2474–2479, Dec. 2007.

[3] N. A. Dodds *et al.*, "The contribution of low-energy protons to the total on-orbit SEU rate," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 2440–2451, Dec. 2015.

[4] N. A. Dodds *et al.*, "New insights gained on mechanisms of low-energy proton-induced SEUs by minimizing energy straggle," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 6, pp. 2822–2829, Dec. 2015.

[5] J. A. Pellish *et al.*, "Criticality of low-energy protons in single-event effects testing of highly-scaled technologies," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 2896–2903, Dec. 2014.

[6] G. Cellere, P. Pellati, A. Chimenton, J. Wyss, A. Modelli, L. Larcher, and A. Paccagnella, "Radiation effects on floating-gate memory cells," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 6, pp. 2222–2228, Dec. 2001.

[7] F. Irom, D. N. Nguyen, G. R. Allen, and S. A. Zajac, "Scaling effects in highly scaled commercial nonvolatile flash memories," in *Proc. IEEE Radiat. Effects Data Workshop (REDW)*, Jul. 2012, pp. 103–108.

[8] M. Bagatin, S. Gerardin, A. Paccagnella, and A. Visconti, "impact of technology scaling on the heavy-ion upset cross section of multi-level floating gate cells," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 3, pp. 969–974, Jun. 2011.

[9] H. Schmidt, D. Walter, F. Gliem, B. Nickson, R. Harboe-Sorensen, and A. Virtanen, "TID and SEE tests of an advanced 8 Gbit NAND-flash memory," in *Proc. IEEE Radiat. Effects Data Workshop*, Jul. 2008, pp. 38–41.

[10] T. R. Oldham *et al.*, "SEE and TID characterization of an advanced commercial 2Gbit NAND flash nonvolatile memory," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3217–3222, Jun. 2006.

[11] H. Schmidt, D. Walter, M. Bruggemann, F. Gliem, R. Harboe-Sorensen, and P. Roos, "Annealing of static data errors in NAND-Flash memories," in *Proc. RADECS*, Sep. 2007, pp. 224–228.

[12] M. Bagatin, S. Gerardin, A. Paccagnella, and V. Ferlet-Cavrois, "Alpha-induced soft errors in floating gate flash memories," in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2012, pp. 3C.2.1–3C.2.7.

[13] S. Gerardin, M. Bagatin, A. Paccagnella, V. Ferlet-Cavrois, A. Visconti, and C. D. Frost, "Neutron and alpha single event upsets in advanced NAND flash memories," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 4, pp. 1799–1805, Aug. 2014.

[14] M. Bagatin *et al.*, "Proton-induced upsets in SLC and MLC NAND flash memories," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 6, pp. 4130–4135, Dec. 2013.

[15] S. Gerardin, M. Bagatin, A. Paccagnella, J. R. Schwank, M. R. Shaneyfelt, and E. W. Blackmore, "Proton-induced upsets in 41-nm NAND floating gate cells," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, pp. 838–844, Aug. 2012.

[16] S. Gerardin, M. Bagatin, A. Paccagnella, and V. Ferlet-Cavrois, "Degradation of sub 40-nm NAND flash memories under total dose irradiation," *IEEE Trans. Nucl. Sci.*, vol. 59, no. 6, pp. 2952–2958, Dec. 2012.

[17] N. Mielke *et al.*, "Bit error rate in NAND flash memories," in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr./May 2008, pp. 9–19.

[18] M. Bagatin *et al.*, "Sample-to-sample variability and bit errors induced by total dose in advanced NAND flash memories," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 2889–2895, Dec. 2014.

[19] E. L. Petersen, "Soft error results analysis and error rate prediction," in *Proc. IEEE NSREC Short Course Notebook*, Jul. 2008.

[20] M. Bagatin, S. Gerardin, A. Paccagnella, and V. Ferlet-Cavrois, "Single and multiple cell upsets in 25-nm NAND flash memories," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2675–2681, Aug. 2013.

[21] S. Gerardin *et al.*, "Heavy-ion induced threshold voltage tails in floating gate arrays," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3199–3205, Dec. 2010.

[22] N. Butt and M. Alam, "Modeling single event upsets in floating gate memory cells," in *Proc. IEEE Int. Rel. Phys. Symp.*, May 2008, pp. 547–555.

[23] M. J. Beck *et al.*, "The role of atomic displacements in ion-induced dielectric breakdown," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3210–3217, Dec. 2009.

[24] G. Cellere, A. Paccagnella, A. Visconti, M. Bonanomi, and A. Candelori, "Transient conductive path induced by a single ion in 10 nm SiO_2 layers," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3304–3311, Dec. 2004.

[25] M. Murat, A. Akkerman, and J. Barak, "Ion track structure and dynamics in SiO_2," in *Proc. Radiat. Effects Compon. Syst. (RADECS)*, Sep. 2007, pp. 1–9.

[26] M. Murat, A. Akkerman, and J. Barak, "Electron and ion tracks in silicon: Spatial and temporal evolution," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3046–3054, Dec. 2008.

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