A Two-Stage Isolated Resonant DC-DC Converter for Wide Voltage Range Operation

Nicola Zanatta
Dept. of Management and Engineering
University of Padova
Vicenza, Italy
nicola.zanatta.2@phd.unipd.it

Tommaso Caldognetto
Dept. of Management and Engineering
University of Padova
Vicenza, Italy
tommaso.caldognetto@unipd.it

Giorgio Spiazzi
Dept. of Information Engineering
University of Padova
Padova, Italy
giorgio.spiazzi@unipd.it

Paolo Mattavelli
Dept. of Management and Engineering
University of Padova
Vicenza, Italy
paolo.mattavelli@unipd.it

***Abstract*—This paper proposes a high-efficiency two-stage isolated dc-dc converter for applications with wide variations of output voltages. It employs a first, pre-regulation stage and a second stage based on an LLC converter, integrated with the first. The second stage is always operated at resonance, ensuring maximum efficiency. The first pre-regulation stage is in charge of *i*) achieving the desired overall conversion ratio and of *ii*) always achieving soft-switching operation of all the switches, even in presence of wide output voltage variations. This allows to tackle the typical challenge of keeping conversion loss low even with input or output port voltages that may vary in a wide range. In this paper, the considered conversion structure is shown considering a preliminary experimental prototype that interfaces a 750-V dc-link with an output bus of nominal voltage in the range 250 V to 500 V, which is common in electric vehicle battery-charging applications. The considered preliminary prototype is rated 5 kW and achieves a peak efficiency of 97.5% at 3 kW output power.**

***Keywords*—battery charger, buck-boost, dc-dc converter, fast-charging, pre-regulation, resonant LLC, soft-switching.**

I. Introduction

DC-DC converters with galvanic isolation are crucial in the development of high-performance electric-vehicle battery charging systems [1]–[4]. These converters typically interface a power source, such as the output of a power factor correction stage connected to the mains, and a high-voltage battery pack.

The resonant LLC converter is commonly employed in these applications for its high power-density and high efficiency around resonance at nominal input and output voltages. However, performance significantly degrade at input or output voltage levels that do not allow near-resonance operation, which is often the case in the considered application [5], [6].

In this paper, a two-stage conversion structure is considered, analyzed, and experimentally evaluated. The structure is composed of a first, pre-regulation stage and a second stage based on the LLC resonant converter. The principle is to operate the second stage at a specific condition that ensures maximum efficiency, namely, at resonance, and exploit the pre-regulation stage to impose such optimal operating condition for the second, LLC stage. The pre-regulation stage can also help in achieving zero-voltage turn-on (ZVS) of the switches that drive the second stage over a wide range of output voltages [2], [6]. Despite of the presence of an additional stage, some valuable characteristics are highlighted and shown herein in terms of overall conversion efficiency.

In the reminder of the paper, Sect. II described the converter topology and operation. The main loss contributions and how to tackle their reduction by means of modulation is discussed in Sect. III and demonstrated in Sect. IV. Finally, Sect. V reports the obtained experimental results considering a 5-kW rated prototype. Sect. VI concludes the paper.

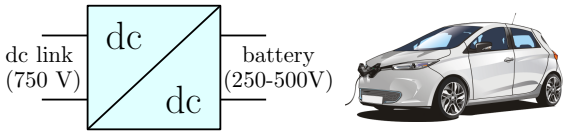

Fig. 1: DC-DC converter in EV-charging application.

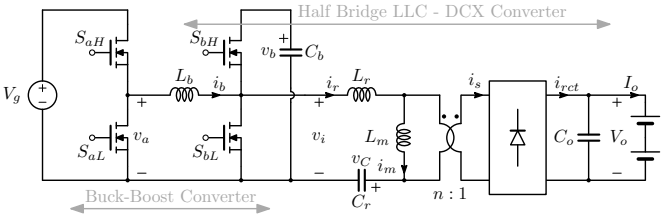

Fig. 2: Two-stage converter with pre-regulation and LLC stage.

II. Converter Structure and Operation

A. Topology Description

The converter scheme is shown in Fig. 2. It is a two-stage topology, the second stage is an LLC resonant converter, while the first stage is a buck-boost stage. The peculiarity of this topology is the integration of the two power switches

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S_{bH} and S_{bL} of the buck-boost stage as primary switches of the half-bridge LLC topology [7]–[10].

In order to exploit the high performance of the LLC stage working as dc-transformer (DCX) [11], the right-leg (S_{bH} and S_{bL}) duty cycle is fixed at 50%. Whereas, the two remaining degrees of freedom, that is, the duty cycle d of the left-leg (S_{aH} and S_{aL}) and the phase shift φ between the driving signals of the two legs, can be used to adjust *i*) the inductor current at switching instants, which is important for ZVS constraints, and *ii*) the output voltage, which is important to keep resonance operation of the LLC stage.

B. Operation

First, the total voltage gain of the structure can be computed as the product of the voltage gain M_{BB} of the pre-regulation buck-boost and the half-bridge LLC working as DCX. From the volt-second balance on L_b, it yields:

$$d \cdot V_g - \frac{V_b}{2} = 0 \quad \Rightarrow \quad M_{BB} = \frac{V_b}{V_g} = 2d \tag{1}$$

Considering the half-bridge LLC working as DCX:

$$M_{LLC} = \frac{V_o}{V_b} = \frac{1}{2n} \tag{2}$$

Combining (1) and (2), the whole converter voltage gain is:

$$M = \frac{V_o}{V_g} = M_{BB} \cdot M_{LLC} = \frac{d}{n} \tag{3}$$

Notably, the voltage gain is a function of the duty-cycle d of the left leg only. Whereas, the phase-shift φ represents a degree of freedom that can be used to properly shape the piece-wise linear current i_b to ensure ZVS of the four switches.

Two main operation modes are distinguished, namely, boost mode, when $d > 0.5$, and buck mode, when $d < 0.5$. For each operation mode, phase shift variations give rise to four different shapes of the inductor current i_b, herein refereed to as switching modes (SM). A total of eight SM depending on the values of d and φ are then present, displayed in Fig. 3.

For the purpose of the analysis, it is worth to observe that for each SM the inductor i_b current can be described by four linear segments delimited by their corresponding switching instants. The corresponding boundary phase shift φ values and switching instants are reported in Table Ib and Table Ia for buck and boost mode, respectively. Time instants t_0 and t_4 are 0 and 1, respectively, where time instants are considered normalized by the switching period $T_s = 1/f_s$.

C. Inductor Current Derivation

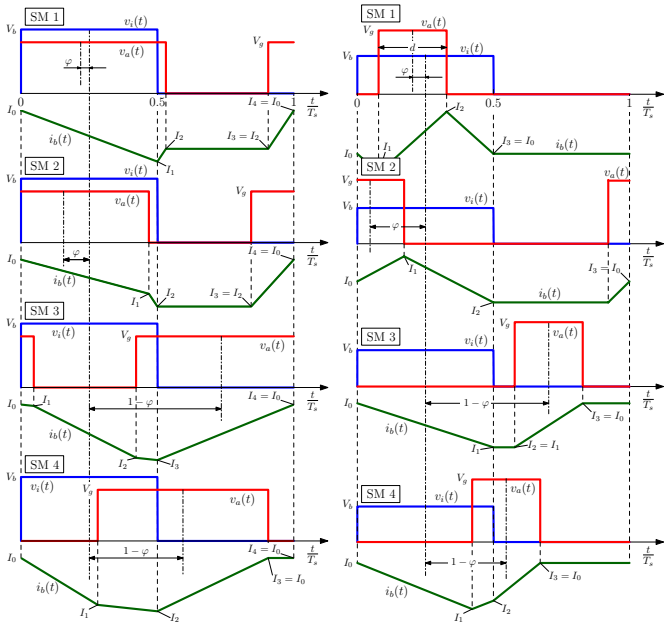
The equivalent circuit in Fig. 4 can be referred to for the derivation of the current i_b through the inductor L_b. Source voltages v_i and v_a model the voltage imposed by the half-bridges in Fig. 2 according to Table I.

The instantaneous inductor current i_b in the time domain can be computed as:

$$i_b(t) = I_0 + \frac{1}{L_b} \int_{t_0}^{t} \left(v_a(\tau) - v_i(\tau)\right) \mathrm{d}\tau \tag{4}$$

where $I_0 = i_b(t_0)$ is the initial value of the inductor current, $t_0 < t$. Being the inductor current waveform piecewise linear, (4) can be computed as:

$$i_b(t) = i_b(t_{k-1}) + \frac{v_{L_b}(t)}{L_b} \cdot (t - t_{k-1}) \ , \quad t \in [t_{k-1},\, t_k) \tag{5}$$



(a) (b)

Fig. 3: Main converter waveforms for different phase shift values. (a) Boost case; (b) buck case.

TABLE I: Boundaries and corresponding switching instants.

(a) Boost operation mode (i.e., $d \geq 0.5$)

SM	Boundaries	Switching instants $4 \cdot t_1/T_s$	$4 \cdot t_2/T_s$	$4 \cdot t_3/T_s$
1	$\frac{1-2d}{4} \leq \varphi < \frac{2d-1}{4}$	2	$1-4\varphi+2d$	$5-4\varphi-2d$
2	$\frac{2d-1}{4} \leq \varphi < \frac{3-2d}{4}$	$1-4\varphi+2d$	2	$5-4\varphi-2d$
3	$\frac{3-2d}{4} \leq \varphi < \frac{1+2d}{4}$	$1-4\varphi+2d$	$5-4\varphi-2d$	2
4	$\frac{1+2d}{4} \leq \varphi < \frac{5-2d}{4}$	$5-4\varphi-2d$	2	$5-4\varphi+2d$

(b) Buck operation mode (i.e., $d < 0.5$)

SM	Boundaries	Switching instants $4 \cdot t_1/T_s$	$4 \cdot t_2/T_s$	$4 \cdot t_3/T_s$
1	$\frac{2d-1}{4} \leq \varphi < \frac{1-2d}{4}$	$1-4\varphi-2d$	$1-4\varphi+2d$	2
2	$\frac{1-2d}{4} \leq \varphi < \frac{1+2d}{4}$	$1-4\varphi+2d$	2	$5-4\varphi-2d$
3	$\frac{1+2d}{4} \leq \varphi < \frac{3-2d}{4}$	2	$5-4\varphi-2d$	$5-4\varphi+2d$
4	$\frac{3-2d}{4} \leq \varphi < \frac{3+2d}{4}$	$5-4\varphi-2d$	2	$5-4\varphi+2d$

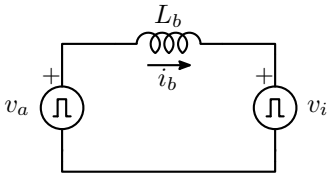


Fig. 4: Equivalent circuit for inductor current analysis.

for $k = 1, 2, 3, 4$, let us call I_k the inductor current values $i_b(t_k)$ and v_{L_k} the constant inductor voltage in $[t_{k-1},\, t_k)$. The initial value $I_0 = i_b(t_0)$ is calculated imposing the capacitor charge balance during the conduction phase of S_{bH}, between $t = 0$ and $t = T_s/2$, thus:

$$I_o = \frac{n}{T_s}\int_0^{T_s/2} i_b(t)\,\mathrm{d}t = \frac{n}{2T_s}\sum_{k=1}^{N}\Delta t_k(I_{k-1} + I_k) \qquad (6)$$

where $\Delta t_k = t_k - t_{k-1}$ and $N = 1, 2$ or 3 number of current piecewise in the considered half-period, depending on the SM. Observing that $I_k = I_{k-1} + v_{L_k}\Delta t_k/L_b$ and $\sum_{k=1}^{N}\Delta t_k = T_s/2$, (6) yields:

$$I_o = n\frac{I_0}{2} + \frac{n}{2L_bT_s}\sum_{k=1}^{N} v_{L_k}\Delta t_k(\Delta t_k + 2\Delta t_{k+1} + 2\Delta t_{k+2}) \qquad (7)$$

with $\Delta t_k = 0$ for $k > N$. Equation (7) allows to determine the initial value I_0, once the output current is known.

An additional parameter worth computing is the inductor rms current:

$$i_b^{\mathrm{rms}} = \sqrt{\frac{1}{T_s}\int_0^{T_s} i_b^2(t)\,\mathrm{d}t} = \sqrt{\frac{1}{T_s}\sum_{k=1}^{4}\int_{t_{k-1}}^{t_k} i_{b_k}^2(t)\,\mathrm{d}t} \qquad (8)$$

where $i_{b_k}(t) = I_{k-1} + \dfrac{v_{L_k}}{L_b}t$, $t \in [t_{k-1},\, t_k)$, it yields:

$$i_b^{\mathrm{rms}} = \sqrt{\frac{1}{T_s}\sum_{k=1}^{4}\left[I_{k-1}^2\Delta t_k + \frac{I_{k-1}v_{L_k}}{L_b}\Delta t_k^2 + \left(\frac{v_{L_k}}{L_b}\right)^2\frac{\Delta t_k^3}{3}\right]} \qquad (9)$$

The equations reported above can be used numerically (e.g., by MATLAB) and help to properly define the modulation parameter φ, as demonstrated in the following sections.

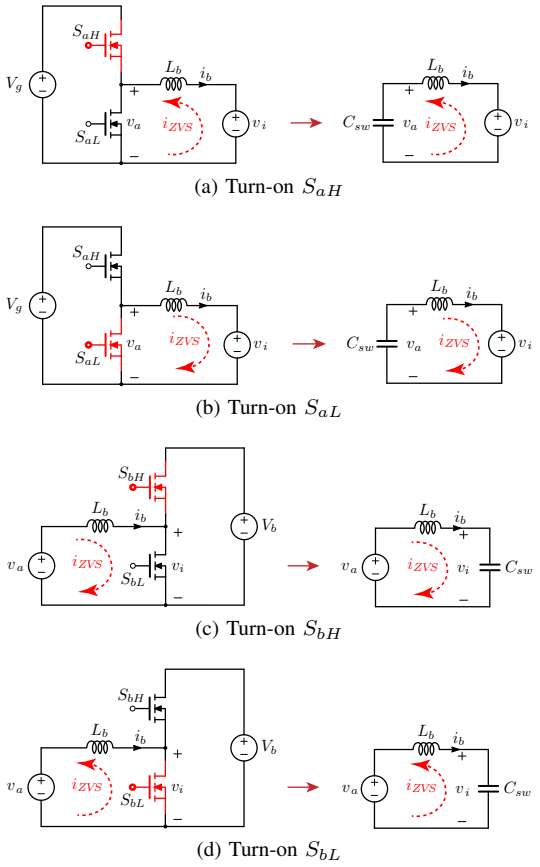
III. Main Loss Contributions

The main loss contributions include conduction losses due to switches on-resistances, losses due to the winding resistances of inductor and transformer, core losses of the main transformer, and switching losses. Phase shift φ modulation has a significant effect on inductor losses and switching losses. Instead, the transformer loss of the LLC stage is not affected by φ variations. Besides, optimal design for maximum efficiency is eased for the LLC stage transformer by the fixed operation at nominal conditions ensured by the pre-regulation stage.

The conduction losses of the inductor can be modeled considering its dc losses, related to the windings dc resistance R_b^{dc} and the dc value of i_b^{dc}, and its ac losses, which can be approximately estimated by considering the rms of the ac component i_b^{ac} and the inductor resistance at the switching frequency:

$$P_{cond} = R_b^{\mathrm{dc}}\cdot i_b^{\mathrm{dc}\,2} + R_b^{\mathrm{ac}}\cdot(i_b^{\mathrm{rms}\,2} - i_b^{\mathrm{dc}\,2}) \qquad (10)$$

Switching losses mainly depend on the switches output capacitance C_{oss}, the inductor current at switching instants $t_{0\div4}$, and the chosen dead-times. To minimize such a loss contribution ZVS at turn-on is necessary [12]. ZVS can be achieved by ensuring a sufficiently intense current of appropriate sign entering in the switching node during the dead-time t_{dead} [12]. This poses minimum switched current constraints for ZVS, which can be determined as discussed in [12]–[14].



(a) Turn-on S_{aH}

(b) Turn-on S_{aL}

(c) Turn-on S_{bH}

(d) Turn-on S_{bL}

Fig. 5: Equivalent circuits for i_{ZVS} calculation with required current direction for ZVS.

Fig. 5 shows the equivalent circuits that can be derived from the switching patterns depicted in Fig. 3. Generators v_b, in Fig. 5a and Fig. 5b, and v_i, in Fig. 5c and Fig. 5d, are set as per the considered SM, resulting in different minimum current conditions function of the input and output voltages.

The proper current directions for ZVS are indicated in the equivalent circuits of Fig. 5. By applying the method in [13], [14], the minimum current condition for the ZVS of the left leg (refer to Fig. 5a and Fig. 5b) can be calculated by solving iteratively the expression for $t_{ZVS} \le t_{dead}$:

$$t_{ZVS} = \int_0^{V_g} \frac{C_{sw}(v_a)}{\sqrt{i_{ZVS}^2 + \dfrac{2}{L_b}\displaystyle\int_0^{v_a} C_{sw}(v)(v_b - v)\,\mathrm{d}v}}\,\mathrm{d}v_a \qquad (11)$$

where t_{ZVS} is the duration of the transition with an initial inductor current i_{ZVS}, and C_{sw} is the equivalent charge capacitance at the switching node [13]. Equation (11) can be adapted to the equivalent circuits in Fig. 5c and Fig. 5d by substituting V_g with V_b and v_i with v_a.

Notably, especially in absence of ZVS, the switching losses typically account to a predominant portion of the total converter loss in the considered high-voltage application [15]. For this reason we focus herein in achieving ZVS, especially at low output voltages, where state-of-the-art LLC topologies present significant efficiency degradations due to the loss of ZVS [2].

In the next Sect. IV the modulation map of the converter at the lower output voltages is presented, showing the soft-switching capability of the converter even at low output voltages. This is experimentally verified in Sect. V.

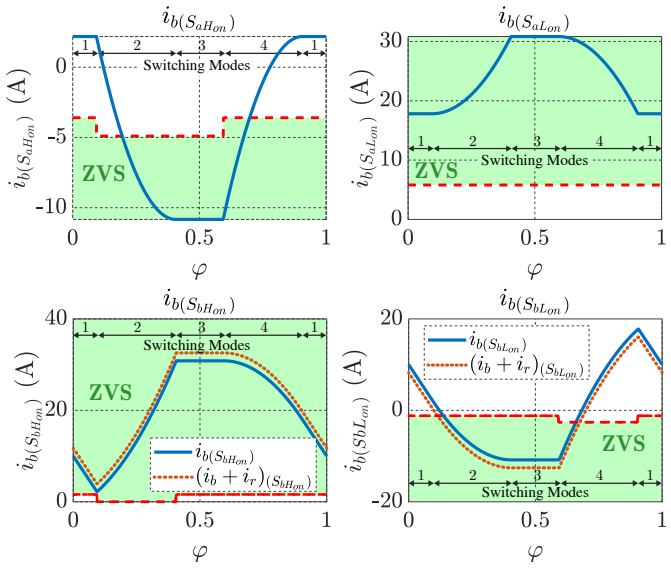


Fig. 6: Inductor current at switching instants *versus* φ; $V_o = V_{o_{min}} = 250\,\mathrm{V}$, $I_o = 10\,\mathrm{A}$, $P_o = 2.5\,\mathrm{kW}$. The term $i_b + i_r$ shows the additional contribution by the magnetizing current.

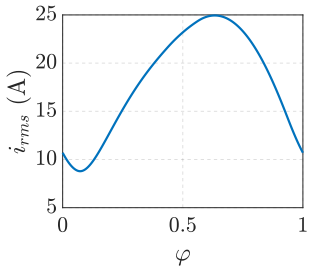


Fig. 7: Inductor rms current, $V_o = 250\,\mathrm{V}$ and $I_o = 10\,\mathrm{A}$.

IV. Simulation Results

Based on Sect. III and the switching patterns presented in Sect. II, modulation maps with different duty cycle d and phase shift φ can be defined aiming at minimizing the identified main loss contributions. Let us consider, for example, the operating point $V_o = 250\,\mathrm{V}$ and $I_o = 10\,\mathrm{A}$. Fig. 6 shows the values at the switching instants of the current i_b *versus* the phase shift φ. The same figure shows highlighted the regions where ZVS for all the transitions is achieved. The red-dotted line at the boundary represents the minimum absolute current to achieve ZVS. Noticeably, the current requirements change with the modes presented in Fig. 3. For example, with $\varphi = 0$, only two transitions out of four present ZVS, while ZVS for all the transitions is achieved if φ is set to about 0.25 to 0.6. Some contribution for ZVS can be given by the magnetizing current i_r too when considering S_{bH}-S_{bL}, which is though negligible in the considered case.

Finally, for a proper selection of φ, the information in Fig. 6 should be completed with the information of the i_b rms current values *versus* φ. This is given in Fig. 7, based on (9). Then, it is possibile to select the phase shift that satisfies ZVS conditions for all the switches with the minimal amount of circulating rms current. In this example, $\varphi = 0.25$ appears the optimal choice. Higher φ would achieve ZVS but with higher rms currents.

Fig. 8a and Fig. 8b display the current and voltage waveforms resulting from simulation considering $\varphi = 0$ and

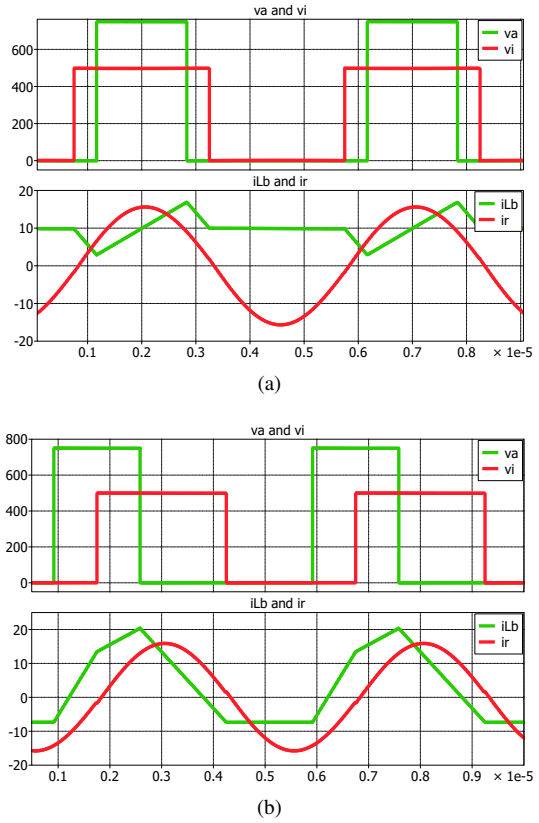


Fig. 8: Simulation results for $V_o = V_{o_{min}} = 250\,\mathrm{V}$, $I_o = 10\,\mathrm{A}$, and $P_o = 2.5\,\mathrm{kW}$ with (a) $\varphi = 0$; (b) $\varphi = 0.25$.

$\varphi = 0.25$, respectively. With $\varphi = 0$, at the turn-on of S_{bL} (i.e., falling edge of v_i) and S_{aH} (i.e., rising edge of v_a) the inductor current has an opposite sign than the required for ZVS, indicated in Fig. 5: a hard-switching transition is expected. With $\varphi = 0.25$, the inductor current at the turn-on of the above mentioned switching instants shows proper direction and intensity, making ZVS possible for all the switches.

Similar considerations are applicable to the whole operation range of the converter with the aim of determining a virtually optimal modulation scheme securing ZVS for all the switches, with minimal rms currents.

V. Experimental Results

The prototype shown in Fig. 9 with parameters reported in Table II has been considered for validation. In order to demonstrate ZVS and high-efficiency capability of the topology, the reported results focus on the worst case of having a low output voltage.

Converter operation at the operating point $\varphi = 0.25$, output voltage of 250 V, and output current of 10 A has been validated experimentally and shown in Fig. 10. Measured waveforms correspond to the predicted behavior in simulation shown in Fig. 8b. Specifically, full ZVS is verified for all the switches. With $\varphi = 0$, non-ZVS transitions for S_{bL} occur since low power levels, as expected by simulation models. This precludes operation at output power higher than 1.1 kW due to excessive switching loss in S_{bL}. Converter operation at such operating point is displayed in Fig. 11 (i.e., , $\varphi = 0$, $V_o = 250\,\mathrm{V}$, $I_o = 4.4\,\mathrm{A}$,). At this point, S_{bL} experiences non-ZVS transitions, while ZVS is achieved for all the other switches. An increase of delivered output power with $\varphi = 0$

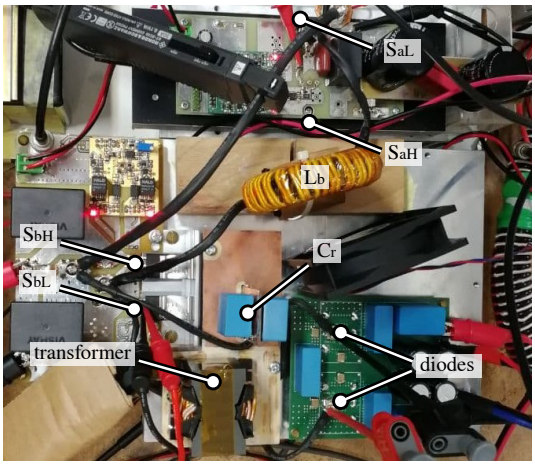


Fig. 9: Experimental prototype.

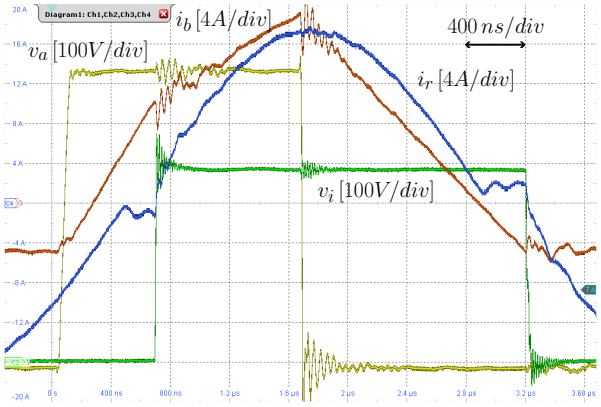


Fig. 10: ZVS for all switches at $\varphi = 0.25$, $P_{out} = 2.5\,\text{kW}$.

TABLE II: Prototype parameters

Parameter	**Symbol**	**Value**	
Input voltage	V_g	750	V
Output voltage	V_o	250-500	V
Nominal power	$P_{o,n}$	5	kW
Switching frequency	f_s	200	kHz
Leakage inductance	L_r	1.8	µH
Magnetizing inductance	L_m	180	µH
Inductance	L_b	30	µH
Turns ratio	n	1	-
Resonant capacitance	C_r	290	nF
SiC MOSFETs S_{aH}, S_{aL}	SCTW100N120G2AG		
SiC MOSFETs S_{bH}, S_{bL}	IMZ120R060M1H		
SiC Bridge Rectifier	SK20KDD12SCp		

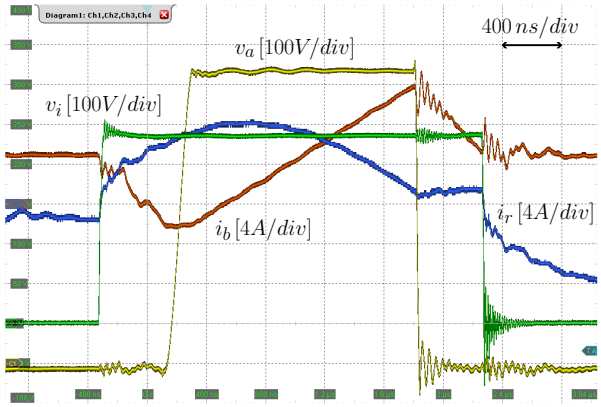
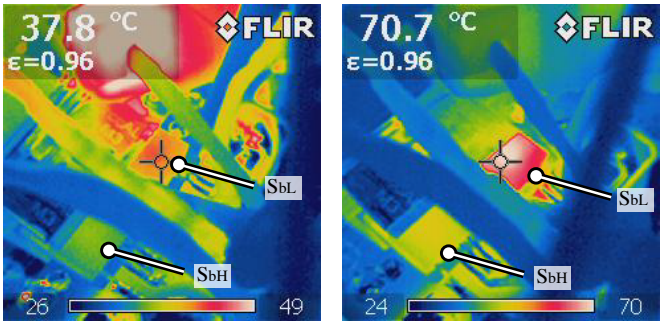


Fig. 11: Non-ZVS for S_{bL} at $\varphi = 0$, $P_{out} = 1.1\,\text{kW}$.

would lead to higher switching and conduction loss and to non-ZVS transition of switch S_{bH} too.

The thermometric image in Fig. 12 shows a significant difference in case temperature of S_{bL} while operating at the two points considered above. Despite of the lower transferred power, operation with $\varphi = 0$ gives temperatures of about 70 °C, indicating significantly high losses on the transistor. Such significant dissipation is not observed after properly adjusting φ, the degree of freedom available for modulation. By exploiting φ, ZVS for all the switches is possible, allowing to reach higher output power with overall lower dissipated power, as evident by comparing Fig. 12.a with Fig. 12.b.

The efficiency curves of the presented prototype are shown in Fig. 13. Such prototype shows a peak efficiency of 96.3% at the lowest output voltage value, very close to the peak efficiency of 97.5% at nominal conditions. It is worth to report that the considered prototype presents no specific optimization in the design of the inductor L_b, which may improve overall efficiency.



(a) (b)

Fig. 12: Thermography of S_{bH}-S_{bL} during (a) ZVS operation at $\varphi = 0.25$, $P_{out} = 2.5\,\text{kW}$, (b) non-ZVS operation at S_{bL}, $\varphi = 0$, $P_{out} = 1.1\,\text{kW}$.

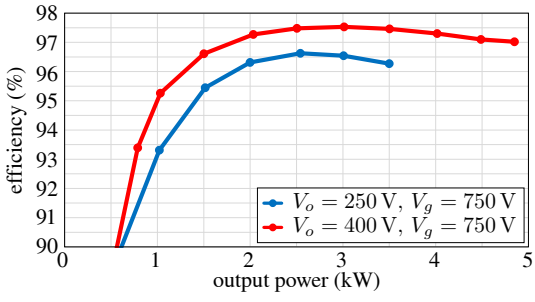


Fig. 13: Efficiency of the topology.

VI. Conclusion

In this paper, a two-stage topology for battery charger applications is considered and analyzed. The topology is composed of a pre-regulation stage with buck-boost characteristics and a second stage based on the LLC topology. The two stages share part of the switching components. Besides the related power density improvements, this calls for an

appropriate modulation of the switches of the converters to ensure optimal operation. This is analyzed in this paper. Specifically, it is shown that by a coordinated operation of the two stages the switched currents may advantageously combine to achieve extended ZVS operation over a wide range of output voltages. ZVS conditions for the modulation parameters have been derived and demonstrated by means of simulation and experimental results. The results have been validated considering a preliminar experimental prototype rated $5\,\mathrm{kW}$ and achieving a peak efficiency of 97.5% at $3\,\mathrm{kW}$ output power.

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