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Development of High-efficiency Modular Multilevel Converters for Renewable Energy Sources

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List of Acronyms

AC Alternating Current.

ANPC Active Neutral-Point-Clamped.

CHB Cascaded H-Bridge.

CM Common-Mode.

DC Direct Current.

DCM Discontinuous Conduction Mode.

DM Differential-Mode.

EMI Electromagnetic Interference.

FACTS Flexible AC Transmissions Systems.

FC Flying Capacitor.

GaN Gallium Nitride.

HV High-Voltage.

HVDC High-Voltage Direct-Current.

IGBT Insulated Gate Bipolar Transistor.

LSCs Level-Shifted Carriers.

LV Low-Voltage.

MMC Modular Multilevel Converter.

MOSFET Metal–Oxide–Semiconductor Field-Effect Transistor.

MV Medium-Voltage.

NLC Nearest Level Control.

NPC Neutral-Point-Clamped.

PF Power Factor.

PI Proportional-Integral.

PR Proportional-Resonant.

PS Phase-Shifted.

PSCs Phase-Shifted Carriers.

PV Photovoltaic.

RRF Rotating Reference Frame.

SiC Silicon Carbide.

SM Submodule.

SRF Stationary Reference Frame.

SST Solid-State Transformers.

THD Total Harmonic Distortion.

Abstract

The global market for commercial and residential systems, as well as research interest in Photovoltaic (PV) systems, has been steadily increasing for years. Low-Voltage (LV) ($< 1.5\,\mathrm{kV}_{dc}$) medium-power (a few hundreds of kW) PV systems have witnessed rapid growth in the global electricity market as they are widely accepted and easy to install and implement. Therefore, the high penetration of LV PV systems in electricity distribution networks requires highly efficient and reliable power conversion units.

Two alternatives are being considered for PV inverters: a) Two-level with a 1.7 kV or higher semiconductors and b) three-level inverter with a 1.2 kV or lower semiconductors. Multilevel topologies, especially the three-level ones such as Neutral-Point-Clamped (NPC) and Flying Capacitor (FC) structures, have become highly competitive alternatives to the two-level hard switching inverters due to their advantages such as lower switching losses, higher power quality, smaller filters, and lower Electromagnetic Interference (EMI). The potentially usable semiconductors are: a) 650 V and 1.2 kV Insulated Gate Bipolar Transistors (IGBTs); b) 650 V, 900 V, or 1.2 kV Silicon Carbide (SiC) Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs), and c) Gallium Nitride (GaN) MOSFETs. Accordingly, for low voltage applications, the optimal choice is to use 650 V or 1200 V components.

Three-level topologies are associated with a major drawback due to the inevitable leakage inductance that can cause over-voltages in the semiconductor devices and consequently limit the operation when a high current or a large variation of current (di/dt) is used. This issue becomes more critical with a load Power Factor (PF) different from unity or when operating in the rectifier mode where the current and voltage have opposite signs. On the other hand, the standard MMC topology can solve these issues. Since each module can be assembled with two switches and a capacitor, parasitic inductance can be minimized quite easily, even with a standard and inexpensive module assembly. Moreover, the switches are always modulated and not just half-wave. As a result, the switches dissipate the same amount of loss,

resulting in a more uniform temperature operation. Unfortunately, the enormous amount of capacitance and, in turn, the energy stored in module capacitors limits the use of classic MMC topology in LV applications.

The main focus of this work is to evaluate the MMC for LV PV applications, reduce the MMC capacitance requirements, and propose a high efficiency, cost-effective, and compact three-phase MMC structure. This work starts with the evaluation of the MMC for a low voltage PV system, the sizing and design of the different components, and the investigation of possible modulation and control schemes. Then, an improved modulation scheme for a modified MMC structure is proposed, which is shown - analytically and experimentally - to reduce the capacitance requirement of this structure. To further reduce the capacitance requirement of the MMC, a three-level MMC topology with an optimized capacitor size is proposed. The proposed structure is designed and optimized to have relatively lower capacitance and fewer number of components than conventional MMCs. The different switching states, component design, sizing, modulation, and proposed topology control are studied. Also, capacitor voltage control is introduced to reduce the number of current sensors required. Finally, the discontinuous conduction mode is analyzed, which leads to an optimized MMC structure with low capacitance and inductance requirements.

Dedicated to my **family**, wife, **Dalia**, and my son, **Omar**.

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First and foremost, I would like to praise **Allah** the Almighty, the Most Gracious, and the Most Merciful for His blessing given to me during my study and in completing this thesis.

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I wish to express my sincere gratitude to my **father**, **mother**, **wife**, **brother**, and **sisters** for their love and support during my entire life.

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Chapter 1

Introduction

In this chapter, the basic terms and concepts of multilevel converters in general and the framework of the dissertation are introduced. Finally, the main objectives, outlines, and contributions are discussed.

1.1 Background

Electricity production is responsible for a large portion of carbon dioxide (CO_2), which leads to global warming. Therefore, more and more requirements are imposed on electricity generation, transmission, and distribution over the years to reduce these serious environmental impacts. Generating electricity from renewable energy resources and efficiently transmitting and utilizing it are of paramount importance [1].

The PV global market is increasing rapidly, over the last ten years, due to the ongoing price reductions. Fig. 1.1 shows the rapid increase in the cumulative capacity for the PV during the last decade. It reached around 760 GW in 2020, which is 22% increase compared to the total global capacity in 2019. The demand for PV systems is spreading for commercial, residential, as well as utility applications [2]. However, several challenges for becoming a major electricity resource include policy, regulatory instability, and financial challenges.

PV systems connected to an ac grid comprise, mainly, two parts: a) a PV panel or array of panels supplying the energy; and b) a Direct Current (DC)/Alternating Current (AC) inverter. Two-level inverters are typically used as an interface between a low-voltage ac grid and PV systems, while multilevel inverters are preferred for medium-voltage systems.

Multilevel inverters are drawing significant attention due to their smaller filter size [4], lower switching losses [5], reduced EMI [6], and higher power quality [7], which make them useful for a variety of applications ranging from LV applications [8, 9] to high-power High-Voltage (HV) converters for PV and wind power systems [10, 11].

Multilevel converters have several advantages such as

- ✓ Lower Total Harmonic Distortion (THD), and therefore, reduced filter size
- ✓ Reduced voltage stress (dv/dt) and EMI
- ✓ Lower switching losses due to the lower switching frequency
- ✓ Reliability and fault-tolerant capability
- ✓ Improved energy harvesting when combined with renewable energy resources such as PV

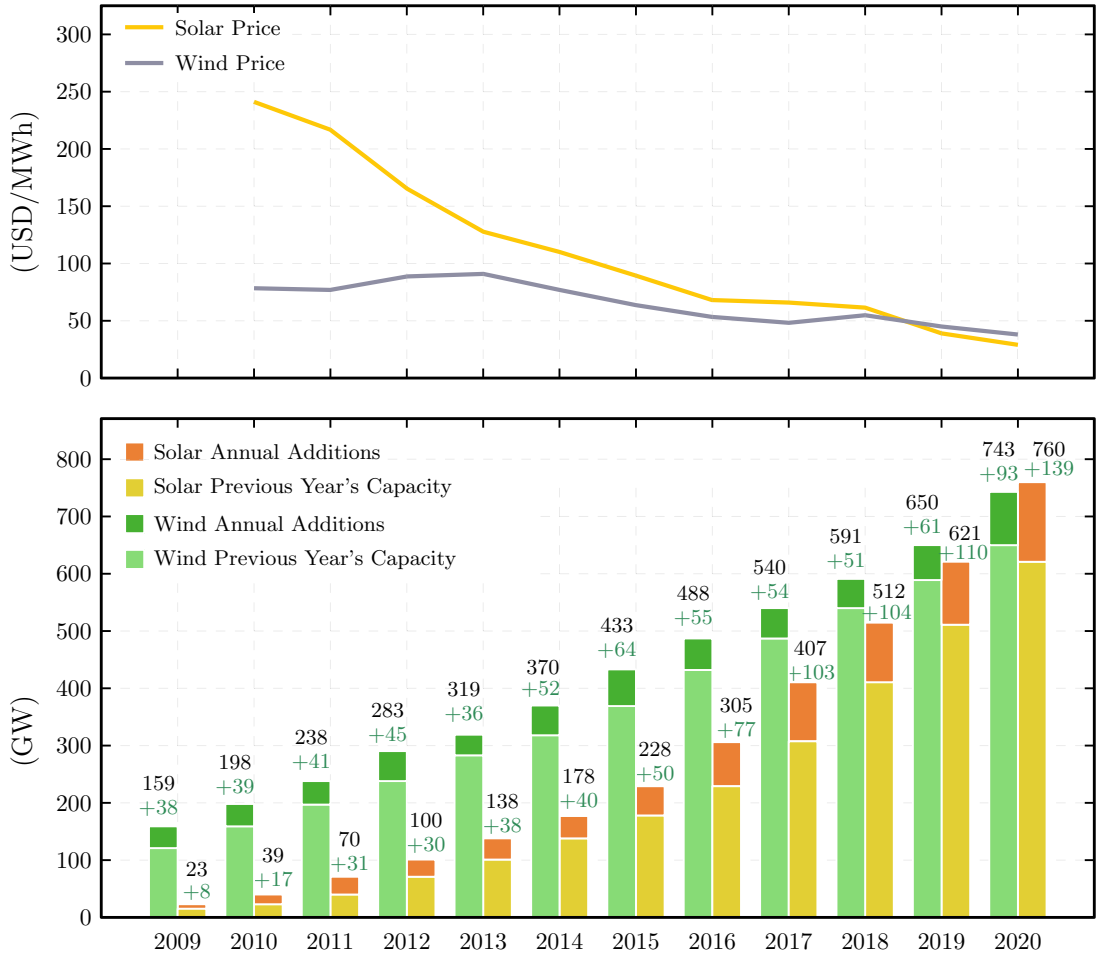


FIGURE 1.1: (a) Solar and wind average auction prices [3]; (b) Global Solar and wind capacity and annual additions from 2009 to 2020 [2].

On the one hand, it is better to increase the number of levels to produce a cleaner sinusoidal voltage. On the other hand, a more number of levels means more components, cost, and complexity. Therefore, three-level converters have paved the way for many applications. Their performance-to-cost ratio was acceptable for those applications due to the mechanical construction complexity of having more levels than three. Moreover, failure propagation of semiconductors with a higher number of levels is another critical drawback that decreases the system reliability [12].

Multilevel inverters have proved their efficacy in many applications, such as High-Voltage Direct-Current (HVDC) systems, Flexible AC Transmissions Systems (FACTS), active filters, motor drives, Solid-State Transformers (SST), motor drives, and many more [13]. Multilevel topologies are commonly classified into three main groups: NPC, FC, and cascaded topologies, which are subdivided into MMC and Cascaded H-Bridge (CHB) [8].

The basic MMC is proposed by [10]. It is abbreviated as MMC, M2C, and M^2LC was also used in the literature. A series connection of Submodules (SMs) mainly characterizes this converter. An MMC consists of six valves/arms, similar to a two-level converter and a six-pulse line commutated converter. Each arm, connecting a DC terminal to one AC terminal, comprises several series-connected independent voltage sources, called SMs, and an inductance. Each SM in the half-bridge MMC variant consists of two IGBT and a capacitor. The arm voltage is controlled by bypassing or inserting the SM's capacitor into the circuit. The current flows continuously in all six arms of the converter. Moreover, the direct current, supplied by the converter's DC link, splits equally into the three phases. The alternating current also splits equally into the upper and the lower arms of each phase.

MMCs are becoming a standard for HVDC. However, for LV applications, the FC, NPC, or a derived solution such as T-type NPC are commonly used [14]. Although, NPC topologies suffer from several drawbacks, including:

- ◇ NPC topologies with a high number of levels (more than three) are possible, but the complexity and cost cannot be justified for low-voltage industrial applications.
- ◇ The losses not only increase with the increasing number of levels but also unevenly distributed between the inner and outer devices as well [8].
- ◇ Over-voltage can appear across the switches, as the switches are not clamped directly to the dc-link capacitors. Therefore, the stray inductance (due to

the long commutation loops) can limit the operation in case of high current or high variation of current (di/dt)

In order to increase the efficiency, enhance the reliability, and reduce the EMI, MMC with several SMs can be used for low-voltage applications in order to share the voltage using lower rated components. As each SM of the MMC can be realized with a capacitor in parallel with a series connection of two switches, the stray inductance can be minimized even using a standard and relatively cheap module assembly. Moreover, as the switches are always modulated, synchronization at the zero crossing is not necessary, that improves the THD of the output voltage.

MMC has been proposed recently for LV systems [15–19]. Analysis for a five-level Si MOSFET-based MMC is presented in [15–17] as an alternative to the two-level IGBT-based Converter for LV AC distribution networks. Moreover, experimental results, provided in [19], show that the efficiency of the MOSFET-based MMC can be further improved by connecting MOSFETs in parallel. In [18], a detailed study for the different possible approaches, that can be used to reduce the required capacitance, is provided.

MMC Features:

- ✓ Enhanced reliability.
- ✓ Excellent voltage waveform quality.
- ✓ Lower semiconductor stresses.
- ✓ Higher efficiency: The switching loss contributes a considerable portion of the total converter loss, therefore, MMCs with high number of levels can reach very high efficiency due to the very low switching frequency of the SMs.
- ✓ The uniform implementation starting from a basic SM building block, which is a switching cell with two-terminals and internal capacitor, the reduced external connections, and the fact that SMs do not need a separate dc power supply, make it simpler and easier for assembling, mechanical construction and scalability.
- ✓ Wide-bandgap semiconductors is promoting the MMC topologies even further.

Unlike other multilevel structures [12]:

- ✓ the arm currents can be controlled to a specific set values that adds a degree of freedom for the converter's optimization.
- ✓ The distributed stray inductance in the converter is not a problem, on the contrary, it may be useful for limiting high-frequency arm currents.
- ✓ dc-side capacitors can be eliminated or reduced in some applications.
- ✓ dc-side short-circuits can be managed safely.

In spite of the seen merits behind the MMCs, the main challenging issues are:

- ◇ The control is more complex than that of a two-level converter.
- ◇ Balancing the SM capacitors voltage is a challenge. It requires high-speed communications between the central unit and the arm as well as a considerable computing processing power.
- ◇ The required SM capacitance is very high compared to other types of multilevel converter topologies. The SM capacitor occupies two-thirds from the overall size of the SM [20].

The most crucial issue with the MMC is the high amount of capacitance. There are many solutions, proposed in the literature, to reduce the needed amount of capacitance either by control or hardware approaches [21–31].

Regarding the control solutions, the voltage oscillation of the capacitors can be reduced by injecting fixed or optimized [22] amount of second-order order harmonics in the circulating current. The second order circulating current reference can be generated online from the instantaneous values of the output current and the modulation signal [25]. Moreover, an offset with a suitable amount can be added to the modulation signals to minimize the amplitude of oscillations [21]. As the injection of circulating currents affects the efficiency, its amplitude can be optimized to achieve minimized voltage ripple with the highest possible efficiency [26]. Beside the voltage boosting capability, Full-bridge SMs gives more capabilities to further reduce the ripple due to the negative voltage state [30] but with additional cost and size. Circulating current injection can eliminate only first-order component of the capacitor voltage in case of half-bridge SMs, but with full-bridge SMs, the second-order component can be also eliminated [28], which has a large contribution to the voltage ripple. Furthermore, third-order harmonics can contribute to the voltage ripple reduction [32].

On the other hand, modifications to the topology can reduce the total amount of capacitance. An MMC structure with a middle SM can reduce the number of SMs of a three-phase MMC by three (one in every phase) [23] for the same number of output voltage levels. The capacitance can be further reduced by connecting the outer SM from each arm in every phase of a three-phase converter to the corresponding SMs in the other two phases. This approach reduces the capacitance of one SM in each arm significantly [24]. The proposed MMC structure in [29] reduces the required capacitance but with a significant increase in the component count and control complexity. An additional full-bridge SM in the ac-side, proposed in [27], can reduce the voltage ripple by redistributing the power between the SMs.

1.2 Main objectives

The main objectives of this dissertation are:

- ➢ analysis of MMC converters;
- ➢ addressing modulation, control, and sizing of the MMC;
- ➢ development of modulation, control, and protection for MMC;
- ➢ development of a competitive high efficiency, low cost, and compact three-phase MMC structure for low-voltage applications.

1.3 Dissertation outline

Chapter 2 discusses the operation, modulation, and control of the MMC structure. Moreover, the design of the different parameters such as the SM capacitance and arm inductance are explained. The MMC structure is compared with several FC structures.

In Chapter 3, an enhanced modulation scheme is presented to reduce capacitance requirements for a five-level modified MMC where the upper and lower SMs are connected in parallel.

Chapter 4 presents the development and design of a modified MMC topology for LV applications. The proposed structure is designed and optimized to have a relatively low capacitance requirement compared with the conventional MMC

topologies. The switching states, modulation, control, and design of the different parameters are investigated in this chapter.

In Chapter 5, a capacitor voltage control scheme for the three-phase MMC structure, proposed in Chapter 4, is introduced. The proposed controller regulates the middle capacitor voltage in order to indirectly control the circulating current with fewer number of current sensors. The detailed analysis, controller design and performance of the proposed scheme are presented in this chapter.

In Chapter 6, the Discontinuous Conduction Mode (DCM) operation of the three-phase MMC structure, proposed in Chapter 4, is discussed. The switching transitions and operation modes of the topology are analyzed. Different modulation techniques and the related switching characteristics are investigated.

Finally, the main conclusions are presented in Chapter 7.

1.4 Main contributions

The main contributions of this dissertation, shown in Fig. 1.2, can be summarized as follows:

I. reviewing the operation, modulation schemes, and control strategies of the conventional MMC;

II. proposing an enhanced modulation scheme to reduce the capacitance requirement of a modified MMC structure;

III. proposing a low-capacitance MMC structure for low-voltage applications;

IV. proposing a single-sensor-based circulating current controller for the proposed low-capacitance MMC structure;

V. studying the DCM operation of the proposed low-capacitance MMC structure.

1.5 List of publications

Patent

P.1 T. Younis, P. Mattavelli, I. Toigo, and M. Corradin, “Modular multilevel converter for low-voltage application with optimized capacitor sizing,” FR1909589, Mar. 2021.

Journal papers

J.1 T. Younis, P. Mattavelli, P. Magnone, I. Toigo, and M. Corradin, “Enhanced Level-Shifted Modulation for a Three-Phase Five-level Modified Modular Multilevel Converter (MMC),” IEEE Journal of Emerging and Selected Topics in Power Electronics, p. 1, 2021.

J.2 T. Younis, P. Mattavelli, I. Toigo and M. Corradin, "Three-Phase Modular Multilevel Converter With Optimized Capacitor Sizing for Low-Voltage Applications," in IEEE Transactions on Power Electronics, vol. 36, no. 12, pp. 13930-13943, Dec. 2021.

J.3 T. Younis, P. Mattavelli, I. Toigo and M. Corradin, “Circulating Current Control for a Three-phase Modified Modular Multilevel Converter with a Reduced Number of Current Sensors” under review of IEEE Transactions on Power Electronics.

J.4 T. Younis, P. Mattavelli, I. Toigo and M. Corradin, “Three-phase Three-level Arm Inductor-less Modular Multilevel Converter” in preparation.

Conference papers

C.1 T. Younis, P. Mattavelli, P. Magnone, I. Toigo, and M. Corradin, “Three-Phase Modular Multilevel Converter (MMC) for Low-voltage Applications: Improved Modulation Technique Toward Less Capacitance Requirement,” in 2019 IEEE Conference on Power Electronics and Renewable Energy (CPERE), 2019, pp. 407–411.

C.2 T. Younis, P. Mattavelli, P. Magnone, I. Toigo, and M. Corradin, “Capacitance Requirements in Three-Phase MMCs for LV Systems: Review of Different Minimization Approaches,” in 2019 21st European Conference on Power Electronics and Applications (EPE ’19 ECCE Europe), Sep. 2019.

C.3 T. Younis, P. Mattavelli, I. Toigo, and M. Corradin, "Three-Phase Modular Multilevel Converter (MMC) for Low-voltage Applications: Improved Modulation Technique Toward Less Capacitance Requirement," in 52nd Annual Meeting of the Associazione Società Italiana di Elettronica (SIE), Trieste, Italy, 2021.

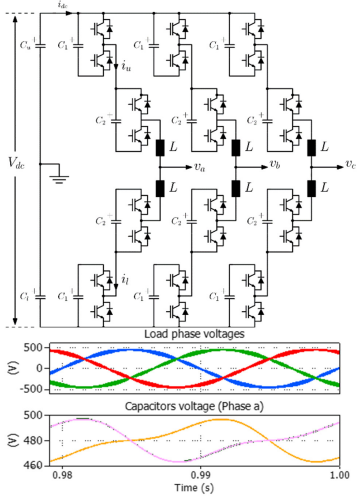
C.4 T. Younis, P. Mattavelli, I. Toigo, and M. Corradin, "A Single-Sensor-Based Circulating Current Controller for a Modified Three-level Modular Multilevel Converter," under review of APEC 2022.

C.5 T. Younis, Ahmed A. Ibrahim, P. Mattavelli, "Comparison between Two-level and Three-level Based Multi-port Converter for Interconnected MVAC Microgrids," accepted in IECON 2021.

Contribution I

1. Literature review
2. Analysis of the state of the art
3. Preparaing simulation models

Contribution II



Review, Analysis, and Simulation for MMC

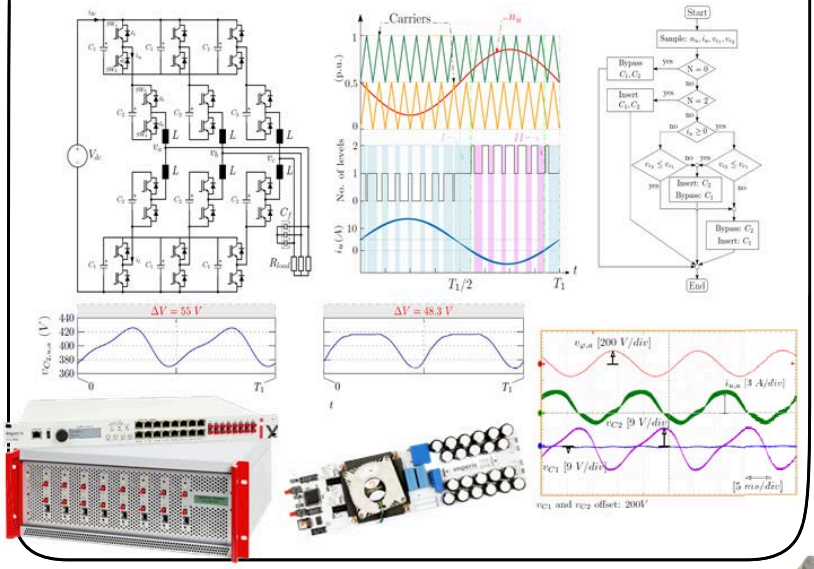
1. Sizing & design
2. Modulation & control
3. Resonace damping
4. Capacitance reduction

cons: huge capacitance requirement in comparison with other solutions such as NPC and FC

Contribution III

Enhanced Modulation for a Modified MMC

- Less capacitance due to the modified structure and the proposed modulation technique



Publications

- Patent
- conference papers
- 2 journal papers

Future work

- DCM operation
- Resonance damping
- Loss optimization

for the patent topology

Contribution IV

Low-capacitance MMC structure

- AC analysis
- Design, modulation, and control
- Study CCM operation
- Operation under different faults

Features

- Short commutation paths
- Enhanced efficiency
- More compact
- Applicable for low-voltage systems

FIGURE 1.2: A simple illustration for the different contributions proposed in this dissertation.

Chapter 2

Principle of Operation, Modulation, and Control of Modular Multilevel Converter

This chapter discusses the basic operation, steady-state analysis, modulation techniques, and control of the conventional MMC topology. The output voltage and current control are investigated. Moreover. The necessity of controlling the circulating current and the control design is discussed. Finally, a comparison between the MMC and the FC structures are discussed and simulated.

2.1 Principle of Operation and Steady-State Analysis

Fig. 2.1(a) and Fig. 2.1(b) show the MMC structure with N SMs and the principle of operation of MMC, respectively. The SMs of the upper arm is modulated to generate a sinusoidal voltage waveform as follows,

$$\begin{bmatrix} v_{u,a} \\ v_{u,b} \\ v_{u,c} \end{bmatrix} = \frac{V_{dc}}{2} + \begin{bmatrix} v_{cm,a} \\ v_{cm,b} \\ v_{cm,c} \end{bmatrix} - \hat{V_m} \begin{bmatrix} cos(\omega t) \\ cos(\omega t - 2\pi/3) \\ cos(\omega t + 2\pi/3) \end{bmatrix}, \tag{2.1}$$

where $v_{u,a}, v_{u,b}, v_{u,c}$ are the voltages between the positive terminal of the dc power supply and the ac terminals of phase a, b, and c, respectively, V_{dc} is the total dc input voltage, $\hat{V_m}$ is peak value of the phase voltages, ω is the line frequency

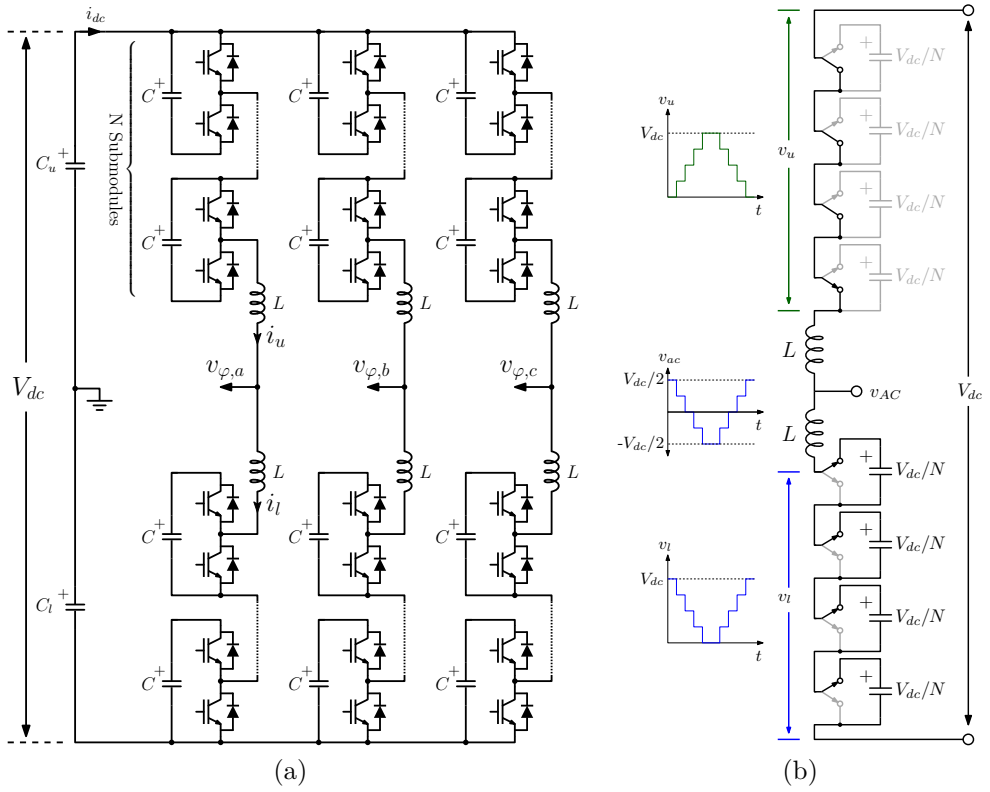


FIGURE 2.1: (a) Three-phase Modular Multilevel Converter (MMC); (b) Principle of operation of MMC.

in rad/s, and $v_{cm,a}, v_{cm,b}, v_{cm,c}$ are the common-mode voltages that are used to control the circulating currents.

Similarly, the voltage waveform across the lower arm is given by,

$$\begin{bmatrix} v_{l,a} \\ v_{l,b} \\ v_{l,c} \end{bmatrix} = \frac{V_{dc}}{2} + \begin{bmatrix} v_{cm,a} \\ v_{cm,b} \\ v_{cm,c} \end{bmatrix} + \hat{V_m} \begin{bmatrix} cos(\omega t) \\ cos(\omega t - 2\pi/3) \\ cos(\omega t + 2\pi/3) \end{bmatrix}, \tag{2.2}$$

where $v_{l,a}, v_{l,b}, v_{l,c}$ are the voltages between the ac terminal of phase a, b, and c, respectively, and the negative terminal of the dc power supply.

From (2.1) and (2.2), the output voltage can be expressed as,

$$\begin{bmatrix} v_{\varphi,a} \\ v_{\varphi,b} \\ v_{\varphi,c} \end{bmatrix} = \frac{1}{2} \left(\begin{bmatrix} v_{l,a} \\ v_{l,b} \\ v_{l,c} \end{bmatrix} - \begin{bmatrix} v_{u,a} \\ v_{u,b} \\ v_{u,c} \end{bmatrix} \right) = \hat{V_m} \begin{bmatrix} cos(\omega t) \\ cos(\omega t - 2\pi/3) \\ cos(\omega t + 2\pi/3) \end{bmatrix}. \tag{2.3}$$

In order to generate the voltages in (2.1) and (2.2) for the upper and the lower arms, the insertion index of the upper arm submodules (n_u) and the insertion index of the lower arm submodules (n_l) are expressed as

$$\begin{bmatrix} n_{u,a} \\ n_{u,b} \\ n_{u,c} \end{bmatrix} = \frac{1}{V_{dc}} \begin{bmatrix} v_{u,a} \\ v_{u,b} \\ v_{u,c} \end{bmatrix}, \quad \begin{bmatrix} n_{l,a} \\ n_{l,b} \\ n_{l,c} \end{bmatrix} = \frac{1}{V_{dc}} \begin{bmatrix} v_{l,a} \\ v_{l,b} \\ v_{l,c} \end{bmatrix}. \tag{2.4}$$

The three-phase ac-side currents are calculated from

$$\begin{bmatrix} i_{\varphi,a} \\ i_{\varphi,b} \\ i_{\varphi,c} \end{bmatrix} = \hat{I_m} \begin{bmatrix} cos(\omega t + \varphi) \\ cos(\omega t - 2\pi/3 - \varphi) \\ cos(\omega t + 2\pi/3 - \varphi) \end{bmatrix}, \tag{2.5}$$

where φ is the load power factor angle and $\hat{I_m}$ is the peak value of the phase currents.

The arm currents can be approximated by a dc, a first-order, and a second-order components as given by [33, 34]

$$\begin{aligned} \begin{bmatrix} i_{u,a} \\ i_{u,b} \\ i_{u,c} \end{bmatrix} &= \begin{bmatrix} i_{circ,a} \\ i_{circ,b} \\ i_{circ,c} \end{bmatrix} + \frac{1}{2} \begin{bmatrix} i_{\varphi,a} \\ i_{\varphi,b} \\ i_{\varphi,c} \end{bmatrix}, \\ \begin{bmatrix} i_{l,a} \\ i_{l,b} \\ i_{l,c} \end{bmatrix} &= \begin{bmatrix} i_{circ,a} \\ i_{circ,b} \\ i_{circ,c} \end{bmatrix} - \frac{1}{2} \begin{bmatrix} i_{\varphi,a} \\ i_{\varphi,b} \\ i_{\varphi,c} \end{bmatrix}, \end{aligned} \tag{2.6}$$

where

$$\begin{bmatrix} i_{circ,a} \\ i_{circ,b} \\ i_{circ,c} \end{bmatrix} = \frac{I_{dc}}{3} + \hat{I_{2\omega}} \begin{bmatrix} cos(2\omega t + \varphi_2) \\ cos(2\omega t + \varphi_2 + 2\pi/3) \\ cos(2\omega t + \varphi_2 - 2\pi/3) \end{bmatrix}. \tag{2.7}$$

2.2 Modulation techniques for the MMC

There are three main types of modulation techniques, shown in Fig. 2.2, that can be used for the MMC. They are discussed in the following sections with simulation results for comparison.

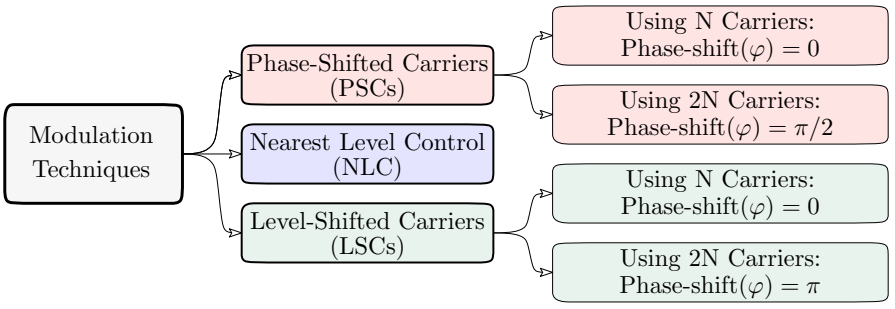


FIGURE 2.2: Modulation techniques for the Modular Multilevel Converter (MMC) [35].

2.2.1 Nearest Level Control

The main idea of the Nearest Level Control (NLC), shown in Fig. 2.3, is sampling the reference signal at a relatively high frequency, then, approximating to the nearest available voltage level. NLC is useful with a converter of high number of submodules.

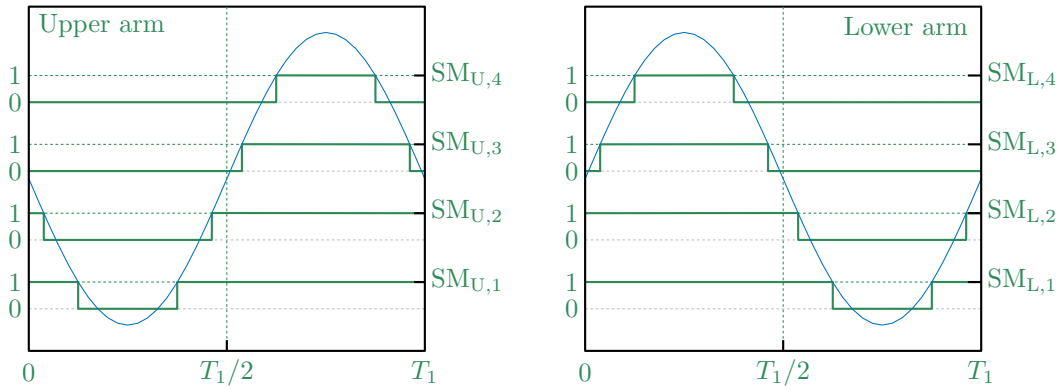


FIGURE 2.3: Implementation of the nearest level control for Modular Multilevel Converter (MMC).

2.2.2 Carrier-based Modulation

Carrier-based modulation is based on relatively high-frequency carriers. Carriers are compared with a normalized reference voltage to generate the driving signals

for SMs. Fig. 2.4 shows the different modulation techniques that can be used with the MMC. These techniques are discussed in the following sections.

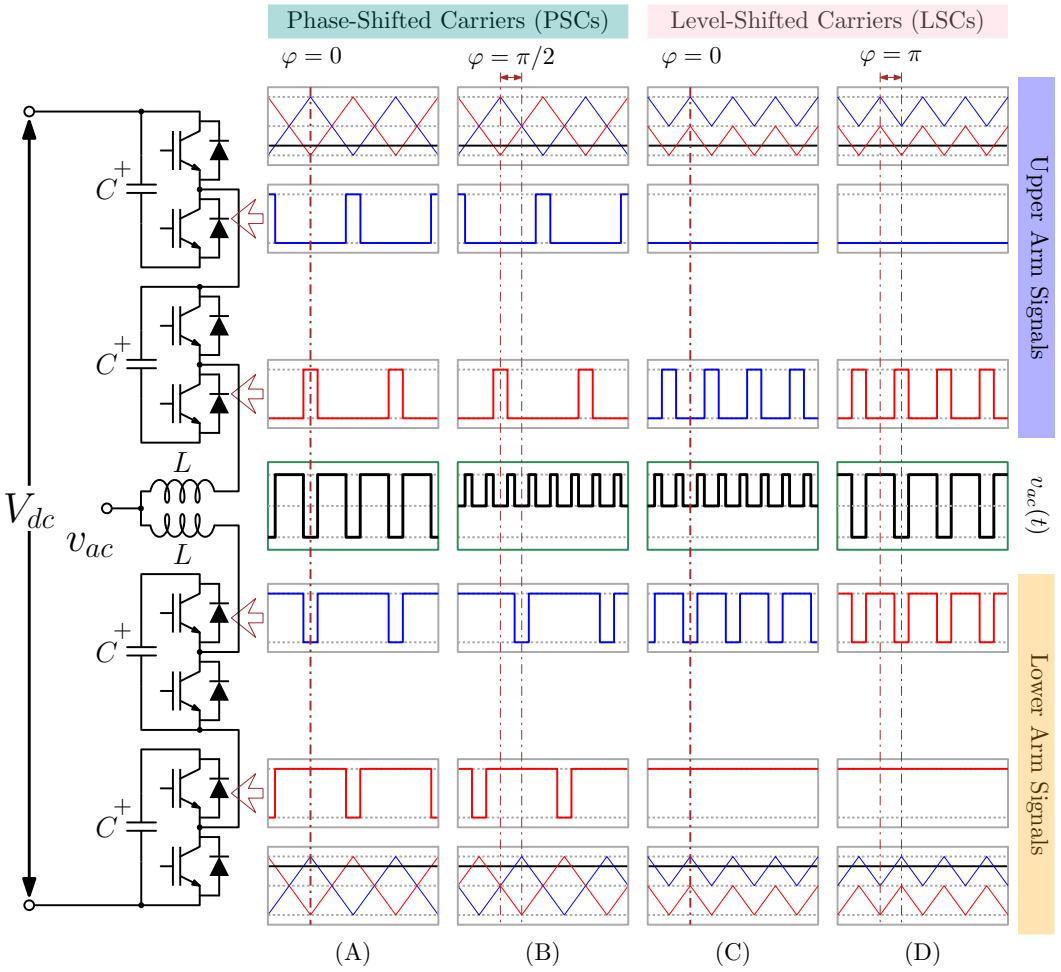


FIGURE 2.4: Comparison between the different modulation techniques used for the modular multilevel converter.

Phase-Shifted Carriers (PSCs)

In this modulation, N or 2N number of carriers with the same level but shifted from each other with a suitable phase are used to generate the switching signals. The comparison between one of these carriers and a reference voltage signal defines the diving signal for the SM. The carriers of the same arm are shifted from each other with $2\pi/N$. The same N carriers of the upper arm can be used for the lower arm, as depicted in Fig. 2.4(a), or another group of N carriers, shifted with $\pi/2$, can be used for the lower arm, which increases the effective switching frequency of the output voltage, as shown in Fig. 2.4(b).

Level-Shifted Carriers (LSCs)

In this modulation, N level-shifted carriers with the same phase shift, as shown in Fig. 2.4(c) or shifted from each other with a π phase shift, as shown in Fig. 2.4(d), are used to generate the switching signals. Zero phase shift between the group of carriers of the upper arm and the lower arm increases the effective switching frequency of the output voltage. Unlike the PSCs modulation, the LSCs requires a sorting algorithm to balance the average voltage of the SMs capacitors.

2.2.3 Simulation results

Fig. 2.5 shows simulation results for the Differential-Mode (DM) voltage with the different modulation techniques discussed above. It can be noted that, both the PSCs with π/N phase-shift between the upper and lower arm carriers and the LSCs modulation gives the lowest dv/dt and the highest effective switching frequency. Detailed comparison between the four modulation technique are listed later.

2.3 Sizing and Design

In this section, the sizing and design of the different parameters of the MMC, including the SM capacitance and the arm inductance, are discussed.

2.3.1 Submodule Capacitor Sizing

The instantaneous power delivered by the upper ($p_{u,a}(t)$) and lower ($p_{l,a}(t)$) arms can be expressed as

$$\begin{aligned} p_{u,a}(t) &= \left(\frac{V_{dc}}{2} - v_{\varphi}\right)\ i_{u,a}(t) \\ p_{l,a}(t) &= \left(\frac{V_{dc}}{2} + v_{\varphi}\right)\ i_{l,a}(t) \end{aligned} \tag{2.8}$$

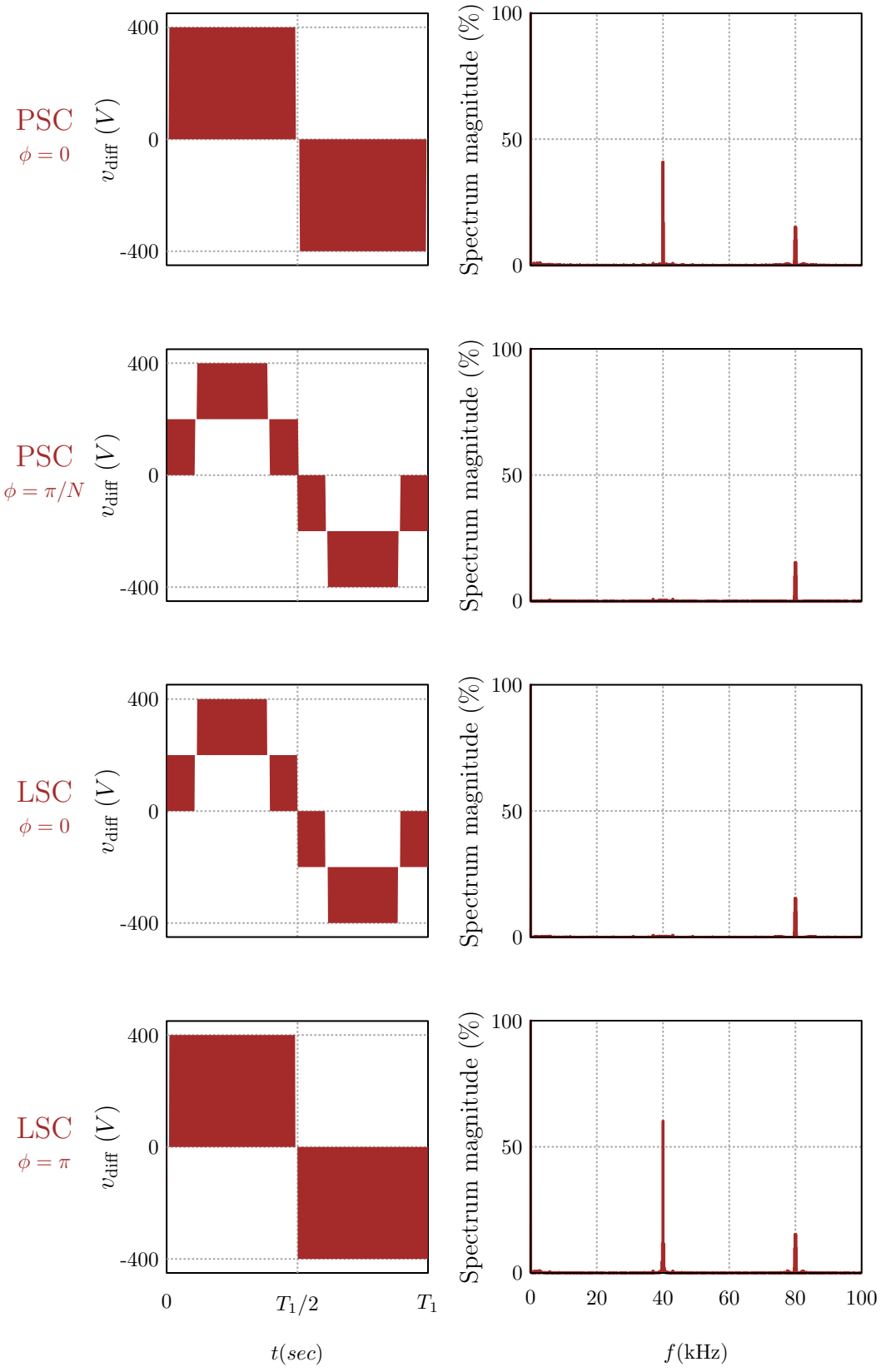


FIGURE 2.5: Simulation results using PLECS for the different modulation techniques.

By substituting (2.3), (2.5), (2.6), and (2.7) in (2.8), the instantaneous powers can be rewritten as

$$\begin{aligned} p_{u,a}(t) = &- \frac{MV_{dc}\hat{I_m}}{8}\, cos(\varphi) + \frac{V_{dc}I_{dc}}{6} + \frac{MV_{dc}\hat{I_m}}{8}\, cos(2\omega t - \varphi) \\ &- \frac{MV_{dc}I_{dc}}{6}\, sin(\omega t) + \frac{V_{dc}I_m}{4}\, sin(\omega t - \varphi) \\ p_{l,a}(t) = &- \frac{MV_{dc}\hat{I_m}}{8}\, cos(\varphi) + \frac{V_{dc}I_{dc}}{6} + \frac{MV_{dc}\hat{I_m}}{8}\, cos(2\omega t - \varphi) \\ &+ \frac{MV_{dc}I_{dc}}{6}\, sin(\omega t) - \frac{V_{dc}\hat{I_m}}{4}\, sin(\omega t - \varphi) \end{aligned} \tag{2.9}$$

The energy stored in the SM's capacitor can be expressed as

$$\begin{aligned} E_{C_{SM}} &= \frac{1}{2}\left|\int p_u(t)dt\right| \\ &= \frac{1}{2}C_{SM}\left(\frac{V_{dc}}{2} + \frac{\Delta V_c}{2}\right)^2 - \frac{1}{2}C_{SM}\left(\frac{V_{dc}}{2} - \frac{\Delta V_c}{2}\right)^2 \\ &= \frac{V_{dc}\Delta V_c}{2}C_{SM} \end{aligned} \tag{2.10}$$

From (2.10), the SM's capacitance can be calculated as follows:

$$C_{SM} = \frac{NS}{3V_{dc}^2\delta M\omega}\sqrt{\left[1 - \left(\frac{Mcos(\varphi)}{2}\right)^2\right]^3}. \tag{2.11}$$

where N is the number of modules/arm, S is the total apparent power delivered by the converter, and δ is the percentage of peak-to-peak voltage ripple of the capacitor.

2.3.2 Arm Inductor Sizing

The capacitor voltage ripple is inversely proportional to the capacitance. This voltage ripple generates a common-mode current circulating through the converter, limited by the arm inductance. Moreover, the equivalent capacitance and the arm inductances form a resonant path that can amplify the second-order harmonic naturally generated in the converter. Therefore, a circulating current regulator is usually adopted to control that current. The circulating current regulator can

control (or eliminate) the low-order harmonics in the circulating current but not the high-order harmonics as it is beyond the control bandwidth. Consequently, the arm inductance is designed to limit the switching components of the circulating current.

With the PSCs modulation, the effective switching frequency of the circulating current is N times the switching frequency. Accordingly, the arm inductance can be designed according to the following formula:

$$L = \frac{V_{dc}}{4N^2 f_s \Delta I_{circ}}, \tag{2.12}$$

where f_s is the switching frequency, and ΔI_{circ} is the peak-to-peak switching ripple of the circulating current.

The inductor may occupy a considerable space. The volume and cost of the arm inductors can be reduced by integrating the upper and the lower arm inductors in one core [36], as shown in Fig. 2.6. The differential-mode inductance is designed according to the required total harmonic distortion at the output, while the common-mode inductance (L_{cm}) is designed according to the maximum peak-to-peak circulating current switching ripple (I_{pp}). L_{cm} can be expressed as,

$$L_{cm} = \frac{N}{8\omega I_{pp} C_{SM} f_s} \sqrt{\frac{9}{16}\hat{I_m}^2 + \frac{1}{9}I_{dc}^2 - \frac{1}{2}\hat{I}_m I_{dc}} \tag{2.13}$$

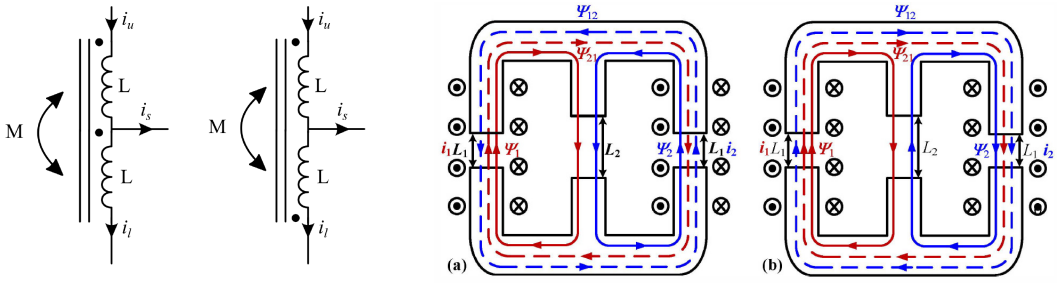


FIGURE 2.6: An integrated arm inductor using EE core [36]. (a) The magnetic field due to the differential-mode current; (b) The magnetic field due to the common-mode current.

2.4 Control Design

The output voltage and/or current control can be performed in the Stationary Reference Frame (SRF) or the Rotating Reference Frame (RRF). The SRF is used in

this dissertation. Fig. 2.7a shows a control scheme of a single-phase DC/AC MMC inverter. A linearized model for the output voltage control with an inner current control loop is shown in Fig. 2.7b, while, a linearized model for the circulating current control is shown in Fig. 2.7c.

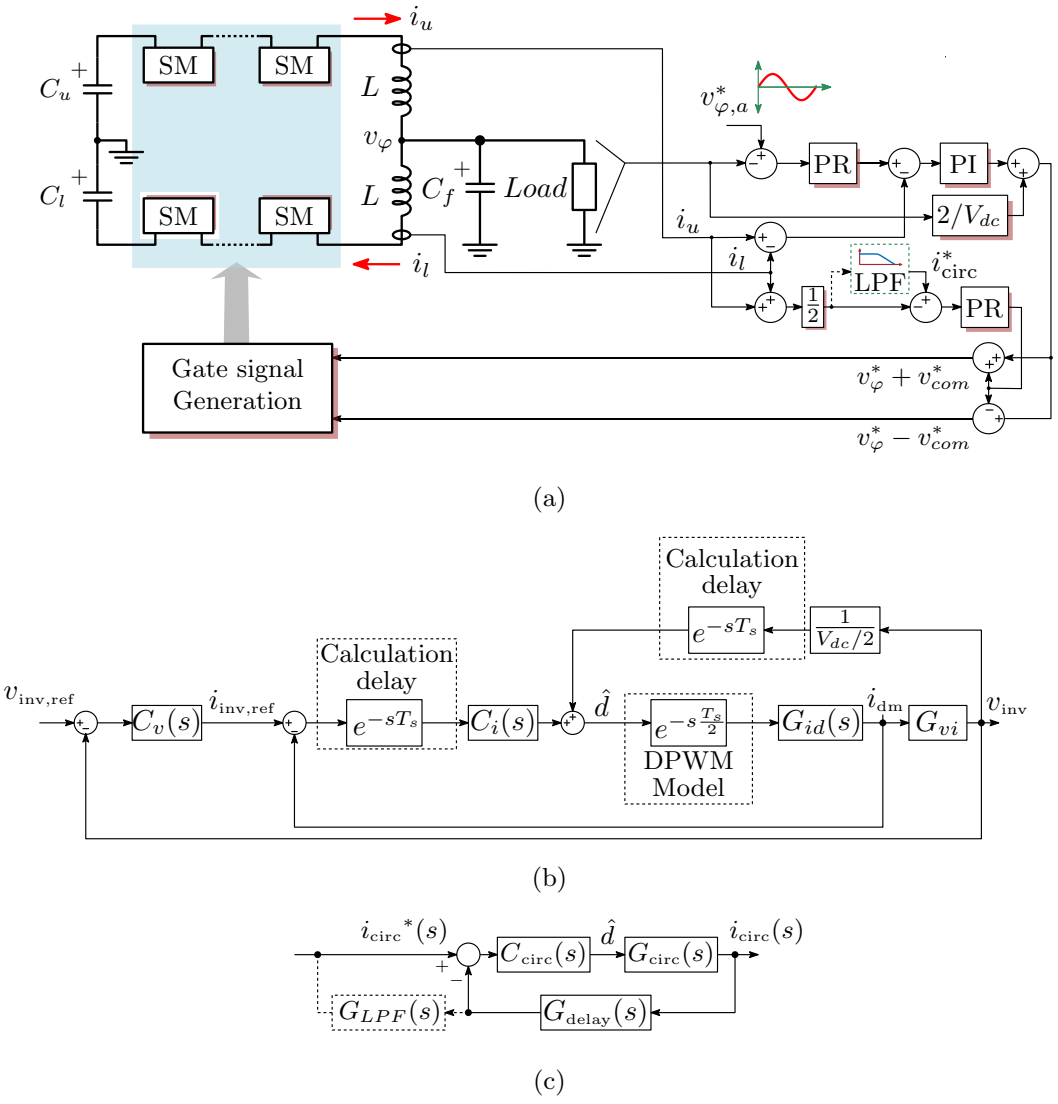


FIGURE 2.7: (a) Control scheme of the modular multilevel converter. A linearized model for the (b) output voltage controller; (c) circulating current controller.

A voltage controller is designed to regulate the output inverter voltage. A Proportional-Resonant (PR) regulator with a resonant frequency of 50 Hz is adopted, as PR regulators provide zero steady state error for sinusoidal signals. The transfer function of the output voltage PR controller is given by

$$C_{v,out} = k_{p,vout} + k_{r,vout}\frac{s}{s^2+\omega^2} \tag{2.14}$$

where $k_{p,vout}$ and $k_{r,vout}$ are the proportional and resonant gains, respectively.

Inner current controller is adopted to simplify the design and to provide over-current protection to the inverter [37]. Proportional-Integral (PI) regulator with a feed-forward from the output voltage is utilized for the inner loop. The transfer function of the PI controller is given by

$$C_{i,out} = k_{p,iout} + k_{i,iout}\frac{1}{s} \tag{2.15}$$

where $k_{p,iout}$ and $k_{i,iout}$ are the proportional and integral gains, respectively.

Circulating currents flow through the MMC arms, but they do not affect the output current. The circulating current is composed mainly of a dc-value, responsible for exchanging the energy between the dc-side and the ac-side, and a second-order component. The second-order harmonics affect not only the overall efficiency of the converter, but also the capacitors voltage ripple, therefore, it is necesseray to regulate these currents.

A circulating current controller in the *abc* frame is utilized to eliminate the second-order harmonics. Similar to the output current control, a PR regulator is also adopted with a resonant frequency of 100 Hz. A low-pass filter is used to extract the dc-value of the circulating current. The transfer function of the circulating current PR controller is given by

$$C_{i,circ} = k_{p,circ} + k_{r,circ}\frac{s}{s^2 + (2\omega)^2}, \tag{2.16}$$

where $k_{p,circ}$ and $k_{r,circ}$ are the proportional and resonant gains, respectively.

2.5 Case Study

This section provides a numerical example for the design of an MMC using specifications and parameters listed in Table 2.1.

Parameter	Symbol	Value
Rated power	S	125 kVA
Input voltage	V_{dc}	960 V
Output line voltage	V_{φ}	550 V
Line frequency	f_1	50 Hz
Switching frequency	f_s	20 kHz
Phase-shifted modulation using 2N carriers		
Circulating current is controlled		

TABLE 2.1: MMC Parameters

The modulation index of the MMC can be calculated from

$$m = \frac{550\sqrt{2/3}}{960/2} = 0.9356 \tag{2.17}$$

Assuming a 5% peak-to-peak capacitor voltage ripple, from (2.11), the SM capacitance can be expressed as

$$C_{SM} = 0.0031 \times N \sqrt{\left[1 - \left(\frac{0.9356 \times \mathrm{PF}}{2}\right)^2\right]^3}. \tag{2.18}$$

The worst case value for the SM capacitance occurs at PF = 0. In this case the capacitance can be re-written as a function of N as

$$C_{SM} = 3.1N\,\mathrm{mF} \tag{2.19}$$

The nearest values for the SM capacitor found in the EPCOS database are listed in Table. 2.2. The EPCOS capacitors are connected in series and/or parallel until fulfilling the voltage and capacitance requirement. The combinations of capacitors, the total stored energy in each arm, and the energy density in each case of N are listed in Table. 2.3 and summarized in Fig. 2.8.

N	Submodule requirement				Available capacitor (EPCOS Database)*							
	V_{SM} (V)	C_{SM} (mF)	Current ripple (A @ LF)	Current ripple (A @ HF)	Voltage (V)	C (mF)	Dia. (mm)	Height (mm)	ESR (mΩ @ 100Hz)	Current ripple (A @ 100Hz)	Volume (cm^2)	Energy (J)
2	750	6	24	26	450	12	90	221	10	29.2	1405	1215
4	375	12	24	26	450	12	90	221	10	29.2	1405	1215
6	250	18	24	26	350	18	90	221	7.4	33.4	1405	1103
8	187.5	24	24	26	250	27	90	221	5.2	40.8	1405	844
10	150	30	24	26	200	33	90	221	5.2	45.9	1405	660

* The nearest available capacitor to the required one.

TABLE 2.2: Comparison between the required submodule capacitor with different number of submodules/arm (N)

N	Number of capacitors/arm		Total volume/arm (cm^3)(1)	Total energy/arm (J)(2)	Energy/volume (mJ/cm^3)
2	4	$C = 12$mF @ 450 V, 2C series 2C	5620	4860	865
4	4	$C = 12$mF @ 450 V, 4C in series	5620	4860	865
6	6	$C = 18$mF @ 350 V, 6C in series	8430	6618	785
8	8	$C = 27$mF @ 250 V, 8C in series	11240	6752	601
10	10	$C = 33$mF @ 200 V, 10C in series	14050	6600	470

(1) Total volume/arm (cm^3) = Capacitor volume (cm^3) x Number of capacitors/arm.
(2) Total energy/arm (J) = Capacitor energy (J) x Number of capacitors/arm.

TABLE 2.3: The number of capacitors, the total volume/arm, the total energy/arm and the energy desnity with different number of submodules/arm (N)

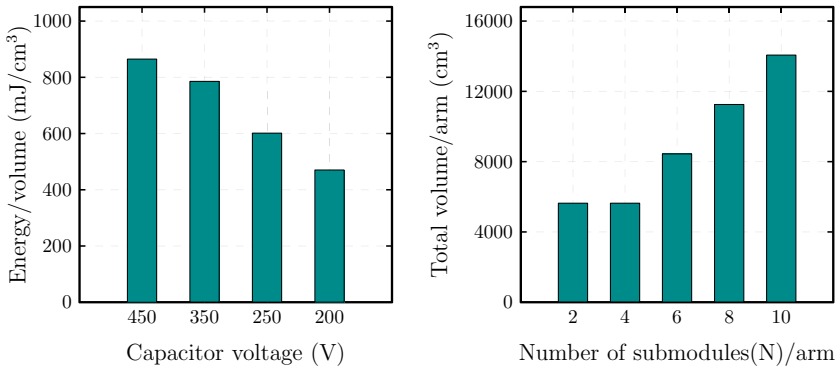


FIGURE 2.8: (a) The energy density versus the utilized capacitor voltage; (b) The total volume/arm versus the number of submodules/arm (N)

Simulation results, shown in Table. 2.4, confirm that PSCs with a $\pi/2$ phase-shift between the upper and lower arm carriers is the most suitable modulation for MMCs considering that LSCs modulation requires an additional efforts for balancing the capacitors' average voltage.

N	Modulation technique		dv/dt	DM - 1st harm. Group		CM - 1st harm. Group		$\int v_{cm}dt$
				Freq. (kHz)	Mag. (V)	Freq. (kHz)	Mag. (V)	Pk2Pk (mV)
2	PSCs	N carriers	960	$Nf_s = 40$	220.9	$Nf_s = 40$	91	1.87
		2N carriers	480	$2Nf_s = 80$	108.3	$2Nf_s = 80$	23	0.26
	LSCs	N carriers	480	$2f_s = 40$	108.3	$2f_s = 40$	23	0.526
		2N carriers	960	$f_s = 20$	365	$f_s = 20$	182.5	4.24
	LSCs	N carriers	480	$2f_{s_p} = 80$	108.3	$2f_{s_p} = 80$	23	0.263
		2N carriers	960	$f_{s_p} = 40$	365	$f_{s_p} = 40$	182.5	2.12
4	PSCs	N carriers	480	$Nf_s = 80$	108.3	$Nf_s = 40$	23	0.264
		2N carriers	240	$2Nf_s = 160$	39.53	$2Nf_s = 80$	19.76	0.132
	LSCs	N carriers	240	$2f_s = 40$	39.53	$2f_s = 40$	19.76	0.526
		2N carriers	480	$f_s = 20$	200.3	$f_s = 20$	100.16	2.35
	LSCs	N carriers	240	$2f_{s_p} = 160$	39.53	$2f_{s_p} = 80$	19.76	0.132
		2N carriers	480	$f_{s_p} = 80$	200.3	$f_{s_p} = 40$	100.16	0.6

TABLE 2.4: Simulation results: comparison between the different modulation techniques.

2.6 Choice of the Number of Submodules

For the application scenario discussed in Sec. 2.5 where $V_{dc} \approx 1\,\text{kV}$, it is possible to use higher number of submodules (e.g. 10) with MOSFETs instead of IGBTs that may reduces the semiconductor losses; however, the capacitance requirement becomes very high.

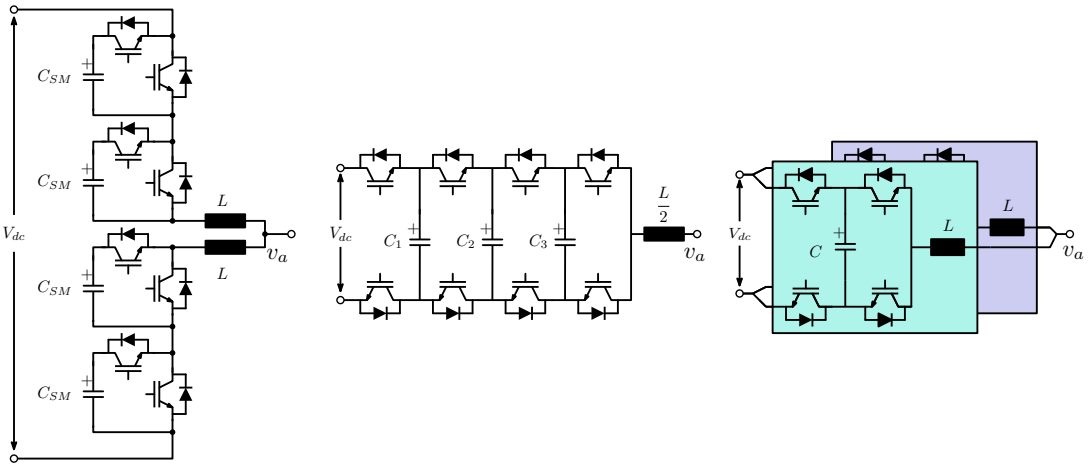
It can be noted from Fig. 2.8 that the increase of the number of SMs increases the volume of the converter since the number of capacitor increases. For a LV application, the most suitable number of modules are $N = 2$ and $N = 4$. These two test cases are compared in terms of the capacitor voltage ripple and rms current, and the semiconductor currents. The results, shown in Table. 2.5, indicate that with the increase of N from 2 to 4, the arm inductance is reduced by 75%, but the SM capacitance is doubled; therefore, two submodules per arm are chosen for this study.

		Case I	Case II
N		2	4
C (mF)		6	12
$\Delta V_{Cpk/pk}(V)$		34	17
$V_{av}(V)$		480	240
$I_{C_{SM}}(A)$	avg./pk/rms	0/139.4/35.2	0/136.5/34.9
	(LF/HF) RMS	23.9/26.2	23.8/25.6
$I_{SWt}(A)$	avg./pk/rms	10.3/55.2/20.5	10.2/53.6/20.2
$I_{dt}(A)$		10.3/139.4/28.6	10.2/136.5/28.4
$I_{SWb}(A)$		44.2/139.4/70.2	43.8/136.5/69.7
$I_{db}(A)$		1/55.2/5.8	1/53.6/5.77
$L(\mu\text{H})$		100	25
$\Delta I_L(A)$		31	31
$I_{L,max}(A)$		140	143

TABLE 2.5: Comparison between MMC with $N = 2$ and $N = 4$

2.7 Comparison between MMC and Flying Capacitor topologies

This section presents a comparison and evaluation for thee multilevel structures shown in Fig. 2.9: 1) Five-level MMC using four SMs per arm; 2) five-level FC; and 3) five-level MMC using two three-level FC structures.



(A) (B) (C)

FIGURE 2.9: (A) 2 SM-MMC (4xHB SM); (B) 5L-FC; (C) 5L-FC (2x3L-FC SM).

Table. 2.6 summarizes the comparison between the three structures in terms of the number of capacitors and the voltage of each, the number of semiconductors and the related voltage stress, the inductor peak current, and the input current.

Parameter \ Value/Phase	5L-MMC (4xHB SM)	5L-FC	5L-MMC (2x3L-FC SM)
$V_{c,avg}\,(V)$	4 x $V_{dc}/2$	1 x $0.75\,V_{dc}$ 1 x $0.5\,V_{dc}$ 1 x $0.25\,V_{dc}$	2 x $V_{dc}/2$
Switches/Diodes	8	8	8
$V_{SW,max}\,(V)$	$V_{dc}/2$	$V_{dc}/4$	$V_{dc}/2$
$I_{L,pk}\,(A)$	$I_{dc}/3 + \hat{i_\varphi}/2$	$\hat{i_\varphi}$	$\hat{i_\varphi}/2$
I_{dc}	Continuous	Discontinuous	Discontinuous

TABLE 2.6: Comparison between the 5-L MMC using 4 half-bridge submodules, 5L-FC, and 5-L MMC using two 3L-FC submodules.

Simulation results are carried out using PLECS for the three structures. Fig. 2.10 shows the voltage and current waveforms of the capacitors. The values and the voltage and current stresses of the different components are listed in Table. 2.7.

Parameter \ Value/Phase		5L-MMC 4xHB SM		5L-FC	5L-MMC using 2x3L-FC
C		4 × 6 mF		3 × 0.1 mF	2 × 0.1 mF
$V_{C,avg}$		4 × 480 V		1 × 720 V 1 × 480 V 1 × 240 V	2 × 480 V
$\Delta V_{Cpk/pk}\,(V)$		34		12.8/12.7/12.9	9
I_C (A)	Avg/pk/RMS	0/139.4/35.2		0/188.4/58.2	0/93.8/29.9
	(LF/HF) RMS	23.9/26.2		0/58.2	0/29.9
Switches/Diodes		8		8	8
$V_{SW,max}\,(V)$		497.5		253.8	484.5
I_{SW} (A)	Avg/pk/RMS	I_{SWt} (A)	10.3/55.3/20.5	51.2/188.5/87.9	25.7/93.8/44
		I_{SWb} (A)	44.2/139.4/70.2		
I_d (A)		I_{dt} (A)	10.3/139.4/28.6	7.9/188.5/30	3.9/93.8/15
		I_{db} (A)	1/55.3/5.8		
L		2 × 100 μH		1 × 50 μH	2 × 100 μH
I_L (A)	Avg/pk/RMS	43.2/139.7/78.8		0/188.5/131	0/93.6/65.8
	(LF/HF) pk/pk	185.9/29.2		363.2/10.2	64.5/1.3
I_{dc}		Cont.		Discont.	Discont.

TABLE 2.7: Simulation results for the 5-L MMC using 4 half-bridge submodules, 5L-FC, and 5-L MMC using two 3L-FC submodules.

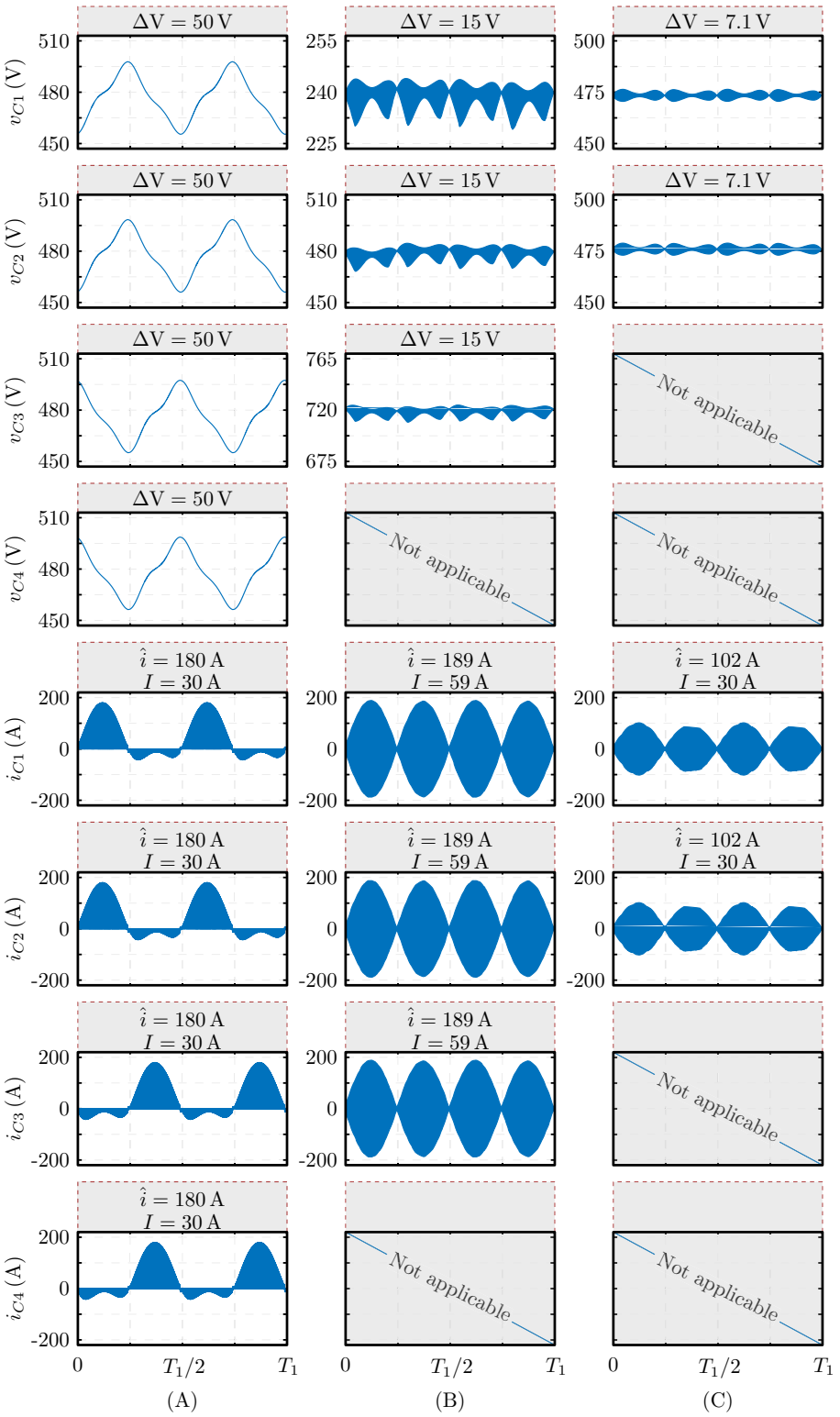


FIGURE 2.10: Simulation results. (A) 2 SM-MMC (4xHB SM); (B) 5L-FC; (C) 5L-FC (2x3L-FC SM).

2.8 Summary

In this Chapter, the basic operation, modulation, and control of the conventional MMC structure are presented. Moreover, the design of the different paramters of the MMC is discussed. The results of the analysis and simulations of the different modulation schemes indicate that the PSCs modulation is the most suitable one for the MMC giving the lowest THD and dv/dt. It is also concluded that, for a LV application, two SM per arm is recommended.

Chapter 3

Enhanced Level-Shifted Modulation for a Three-Phase Five-level Modified Modular Multilevel Converters (MMCs)

This chapter aims to reduce the five-level modified MMC capacitance requirements where the upper and lower submodules are connected in parallel. This reduction has been achieved using an improved modulation technique by minimizing the insertion time of the SMs that require higher capacitance. The proposed modulation is effective in reducing the inner SMs' capacitor voltage ripple at lower modulation indices. Instead, the circulating current injection of the second harmonics effectively reduces the voltage ripple at higher modulation indices. Thus, maximum reduction of the total capacitance requirement for the entire operating range of modulation index can be achieved by a proper combination of the two solutions. Simulation and experimental results on a lab-scaled prototype verify the validity of the proposed solution.

3.1 Principle of Operation, Modulation, and Low-frequency analysis for the Proposed MMC Structure

3.1.1 Steady-state analysis

In [24], a modified MMC topology is proposed. The capacitors of the SMs closer to the positive and negative dc power supply are connected in parallel. Fig. 3.1

shows a five-level variant of the modified MMC. Such a connection makes the three SMs acting like a three-phase inverter, where specific harmonics are cancelled. Therefore, a small capacitance can be used in the external SMs. While the remaining SMs still require relatively large capacitance calculated by (2.11). By injecting second-order harmonics in the circulating current, the ripple in the inner SMs can be reduced, but this comes with higher arm losses due to the higher rms arm currents.

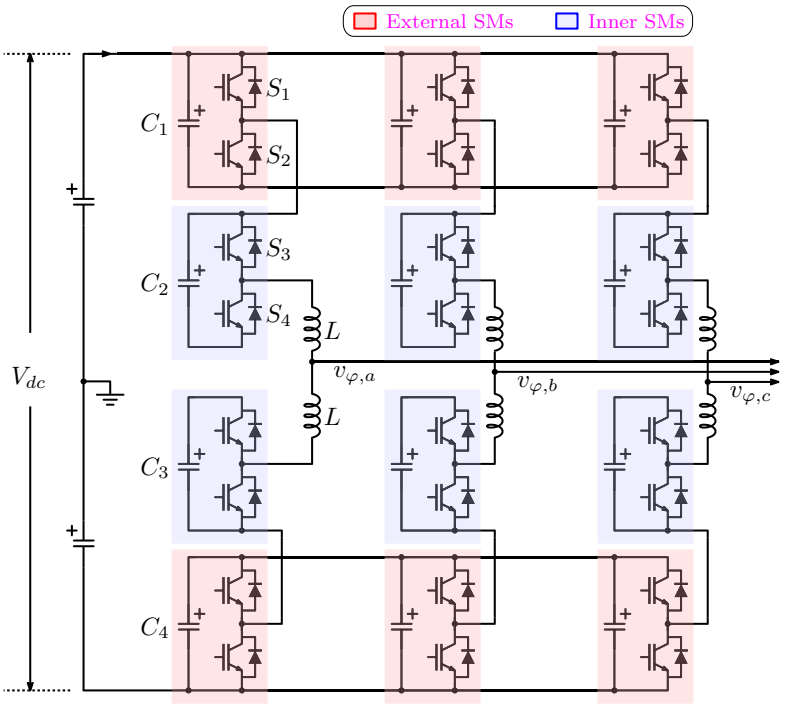


FIGURE 3.1: Three-phase five-level variant from the Modular Multilevel Converter (MMC) proposed in [24].

The arm currents can be approximated by a dc, a first-order, and a second-order components as given by [33, 34]

$$\begin{aligned}
\begin{bmatrix} i_{u,a} \\ i_{u,b} \\ i_{u,c} \end{bmatrix} &= \begin{bmatrix} i_{circ,a} \\ i_{circ,b} \\ i_{circ,c} \end{bmatrix} + \frac{1}{2} \begin{bmatrix} i_{\varphi,a} \\ i_{\varphi,b} \\ i_{\varphi,c} \end{bmatrix}, \\
\begin{bmatrix} i_{l,a} \\ i_{l,b} \\ i_{l,c} \end{bmatrix} &= \begin{bmatrix} i_{circ,a} \\ i_{circ,b} \\ i_{circ,c} \end{bmatrix} - \frac{1}{2} \begin{bmatrix} i_{\varphi,a} \\ i_{\varphi,b} \\ i_{\varphi,c} \end{bmatrix},
\end{aligned} \tag{3.1}$$

where

$$\begin{bmatrix} i_{circ,a} \\ i_{circ,b} \\ i_{circ,c} \end{bmatrix} = \frac{I_{dc}}{3} + \hat{I_{2\omega}} \begin{bmatrix} cos(2\omega t + \varphi_2) \\ cos(2\omega t + \varphi_2 + 2\pi/3) \\ cos(2\omega t + \varphi_2 - 2\pi/3) \end{bmatrix}. \tag{3.2}$$

Taking phase a as an example, if the second-order harmonic of the circulating current is controlled to be zero, the capacitor current of the external SMs of each arm becomes zero. However, if the magnitude and phase of second-order harmonic of the circulating currents are controlled to be $M\hat{I_m}/4\ cos(\varphi)$ and φ respectively, a third harmonic component appears and it is given by

$$i_{C_1} = -\frac{3M\hat{I_{2\omega}}}{4} sin(3\omega t + \varphi). \tag{3.3}$$

The second-order harmonic is cancelled in the remaining SM capacitors [18].

3.2 Proposed Modulation Scheme

In this section, the proposed modulation technique is discussed. The used structure is a five-level variant from the MMC structure proposed in [24] and shown in Fig. 3.1.

3.2.1 Proposed Modulation Scheme and Sorting Algorithm

In the case of PSCs modulation, the same reference is compared with equally spaced in time carriers to generate the driving signals for the different SMs in the same arm, as shown in Fig. 3.2(a). In a standard MMC, all the SMs and their supplying capacitors are identical. Therefore, this modulation leads to almost identical voltage ripple on the SM capacitors. This assumption is not valid for this specific MMC structure, shown in Fig. 3.1, where the external capacitors have much lower voltage ripple due to the connection between the upper and the lower capacitors. In order to maximize the utilization of the external capacitors, a modified modulation is proposed in this chapter. The basic idea is to insert the inner capacitors only when two levels are necessary to generate the arm voltage, aiming to reduce the time when the inner capacitors are inserted. Indeed, when the inner capacitors are not inserted, the capacitor current and the voltage ripple are zero during such interval.

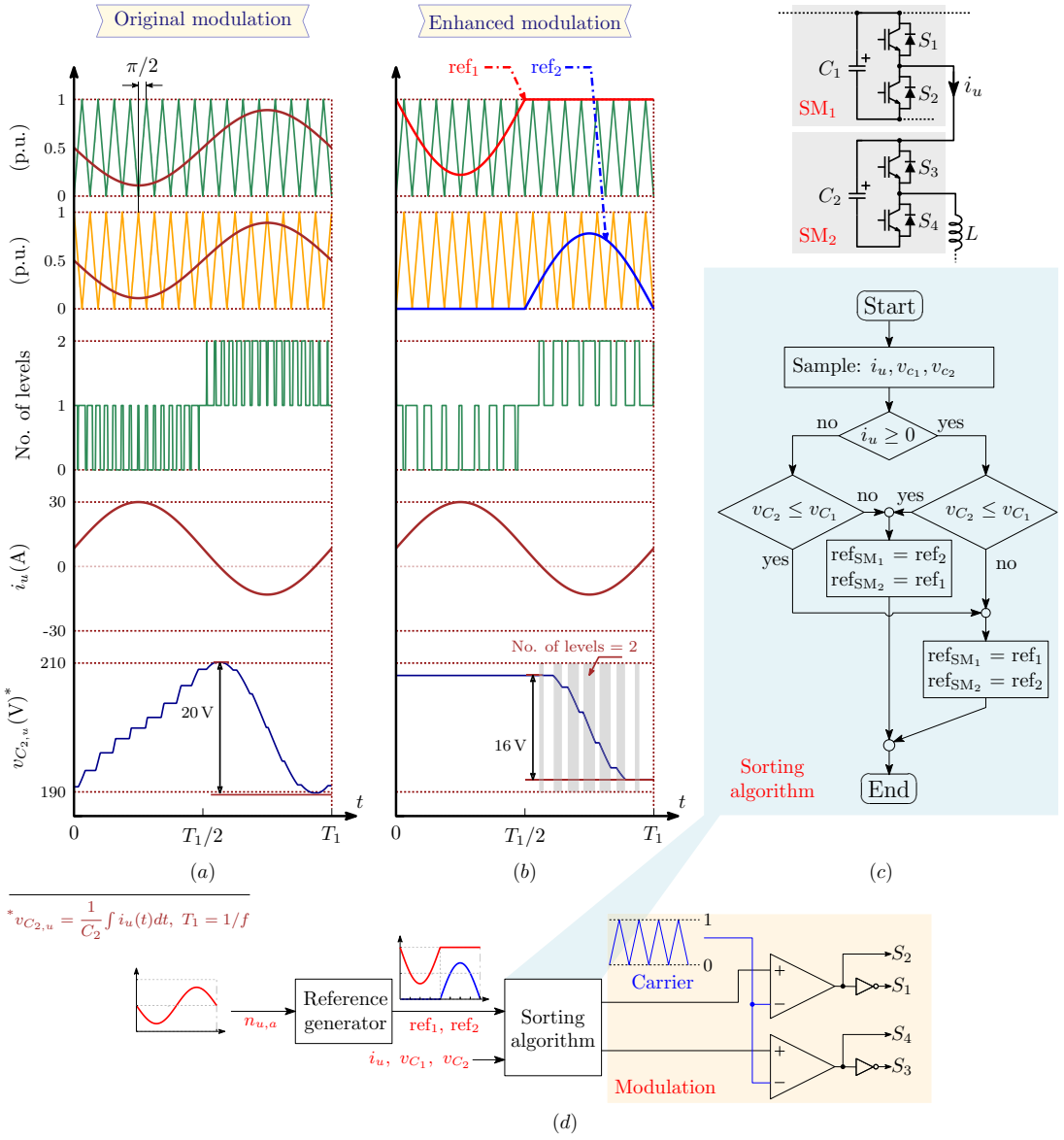


FIGURE 3.2: (a) The original phase-shifted modulation (PSC), the number of levels generated across the upper arm, the upper arm current (i_u), and the expected voltage on the inner capacitor ($v_{C_{2,u}}$), according to the system parameters in Table 3.1; (b) the enhanced modulation, the number of levels generated across the upper arm, the upper arm current (i_u), and the expected voltage on the inner capacitor ($v_{C_{2,u}}$); (c) sorting algorithm; (d) generation of the gate signals for the two SMs.

	Parameter	Symbol	Value
Specifications	Input voltage	V_{dc}	400 V
	Output phase voltage	V_{φ}	110 V_{rms}
	Line frequency	f	60 Hz
	Switching frequency	f_s	21 kHz
Parameters	Arm inductance	L	2.5 mH
	External SM capacitance	C_1	260 μF
	Inner SM capacitance	C_2	260 μF
	Filter capacitance	C_f	22.5 μF

TABLE 3.1: Three-Phase Modular Multilevel Converter (MMC) Specifications and Parameters of Components for Simulation and Experiment

The normalized instantaneous arm voltage decides how many capacitors to be inserted in the arm (none of them, only one, or both) according to the required voltage level at a specific instance. The two SMs in every arm can provide three voltage levels across the arm terminals: a) zero; b) $V_{dc}/2$; and c) V_{dc}. The two capacitors (C_1 and C_2) are bypassed if a zero voltage is needed. In order to achieve a V_{dc} voltage level, the two capacitors (C_1 and C_2) are inserted into the arm. The last case, when only one capacitor is needed to generate a $V_{dc}/2$ voltage level, gives a degree of freedom to insert any one of them. This modulation can be achieved by splitting the voltage reference signal into two reference signals, as shown in Fig. 3.2(b).

According to the direction of the arm current and the instantaneous voltage of the two capacitors, the first reference signal (ref_1) is assigned to one of the two SMs and the second reference signal (ref_2) is assigned to the other one. If the arm current is positive, the inserted SM capacitor charges; therefore, ref_1 is assigned to the SM with the lower capacitor voltage, while, ref_2 is assigned to the other SM. In case of a negative arm current, the inserted capacitor discharges, therefore, ref_1 is assigned to the SM with the higher capacitor voltage, while, ref_2 is assigned to the other SM. Fig. 3.2(c) depicts a flow chart for the algorithm described above. Assuming that the inner SMs are inserted only when two voltage levels are required, their average insertion time becomes less than with the original modulation, which does not consider the different voltage ripple of SMs. The percentage of improvement is highly affected by the modulation index (M). Fig. 3.5 explains this point. Two modulation indices ($M = 0.8$ and $M = 0.5$) and the corresponding number of levels are shown. With the increase of the modulation index, the average time of the case, where the two capacitors are inserted at the same time, increases.

Therefore, the improvement that can be gained by the proposed modulation is reduced. The average voltage of the inner capacitors can be regulated by adopting a separate controller.

Fig. 3.3 shows the average capacitor voltage regulator. A PI controller is adopted to regulate the difference between the average voltages of the inner and external capacitors.

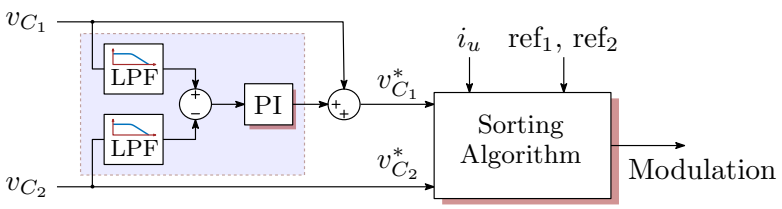


FIGURE 3.3: Average capacitor voltage control.

The voltage ripple of the inner capacitors is higher than the voltage ripple of the external capacitors; therefore, when the inner capacitor is selected to generate the $V_{dc}/2$ level instead of the external capacitor, the average voltage over a switching period becomes less than the case with the external capacitor. As shown in Fig. 3.4, in order to compensate for the inner capacitor voltage ripple, the reference signals should be corrected. According to Fig. 3.4, the corrected references are expressed as,

$$\begin{aligned} \text{ref}_{1,\text{corr}}\, v_{C_2} &= \text{ref}_1\, v_{C_1}, \\ \text{ref}_{1,\text{corr}} &= \frac{v_{C_1}}{v_{C_2}} \text{ref}_1. \end{aligned} \tag{3.4}$$

$$\begin{aligned} &\text{ref}_{2,\text{corr}}\ (v_{C_1} + v_{C_2}) + (1 - \text{ref}_{2,\text{corr}})\ v_{C_2} \\ &\quad = \text{ref}_2\ (v_{C_1} + v_{C_2}) + (1 - \text{ref}_2)\ v_{C_1}, \\ &\quad \text{ref}_{2,\text{corr}} = \frac{v_{C_2}}{v_{C_1}} \text{ref}_2 + \left(1 - \frac{v_{C_2}}{v_{C_1}}\right). \end{aligned} \tag{3.5}$$

3.2.2 Voltage Ripple Evaluation on Inner Capacitors

In order to evaluate, analytically, the amount of reduction in the voltage ripple of the inner capacitors adopting the proposed modulation, an analytical expression is presented for the voltage ripple of the inner capacitors in this subsection in case of

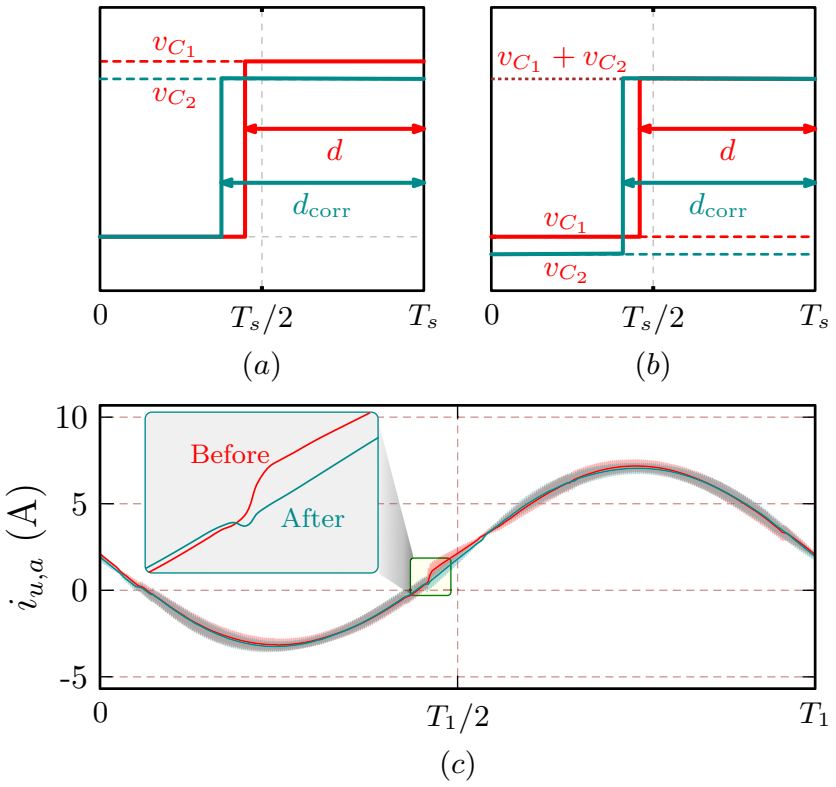


FIGURE 3.4: Commutation between: (a) 0 and $V_{dc}/2$; (b) $V_{dc}/2$ and V_{dc}; (c) the arm current with and without duty-cycle correction.

the original and the proposed modulation. From (2.5), (3.1), and (3.2), assuming a unity load power factor, the upper arm current of phase a can be rewritten as

$$i_{u,a} = \frac{M\hat{I_m}}{4} + \frac{\hat{I_m}}{2} sin(\omega t) \tag{3.6}$$

The maximum and minimum values of the capacitor voltage occur when the arm current crosses zero. The time of zero-crossing points of the arm current can be expressed as

$$t_1 = \pi + \frac{1}{\omega} sin^{-1}\left(\frac{M}{2}\right),\ t_2 = \frac{1}{\omega}\left(2\pi - sin^{-1}\left(\frac{M}{2}\right)\right) \tag{3.7}$$

The instantaneous value of the inner capacitor voltage can be expressed as

$$v_{C_{2,u}} = \frac{1}{C_{2,u}} \int n_u . i_u dt \tag{3.8}$$

3.2.2.1 The original PSC modulation

From (2.4), the insertion index of the inner SMs can be rewritten as

$$n_u = 0.5 + \frac{M}{2} sin(\omega t) \tag{3.9}$$

Substituting (3.6), (3.7), and (3.9) in (3.8), the voltage ripple of the inner capacitors can be approximated as

$$\left(\Delta V_{C_{2,u}}\right)_{Orig} \approx \frac{4S}{3V_{dc}C_{2,u}\omega}\left(\frac{1}{2M} - \frac{3}{16}M\right) \tag{3.10}$$

3.2.2.2 The proposed modulation

As shown in Fig. 3.2b, the insertion index of the inner SMs can be rewritten as

$$n_u = \begin{cases} 0 & 0 \leq \omega t \leq \pi \\ -Msin(\omega t) & \pi \leq \omega t \leq 2\pi \end{cases} \tag{3.11}$$

Substituting (3.6), (3.7), and (3.11) in (3.8), the voltage ripple of the inner capacitors can be approximated as

$$\left(\Delta V_{C_{2,u}}\right)_{Pro} \approx \frac{S}{6V_{dc}C_{2,u}\omega}(2\pi - 4M) \tag{3.12}$$

The percentage of reduction of the voltage ripple of the inner capacitors can be expressed as

$$\frac{\left(\Delta V_{C_{2,u}}\right)_{Orig} - \left(\Delta V_{C_{2,u}}\right)_{Pro}}{\left(\Delta V_{C_{2,u}}\right)_{Orig}} = \frac{8 - 4\pi M + 5M^2}{8 - 3M^2} \tag{3.13}$$

With an increase of M, the amount of reduction is reduced.

3.2.3 Control Design

Fig. 3.6 shows a control diagram of the MMC inverter. A voltage controller is designed to regulate the output inverter voltage. A PR regulator with a resonant

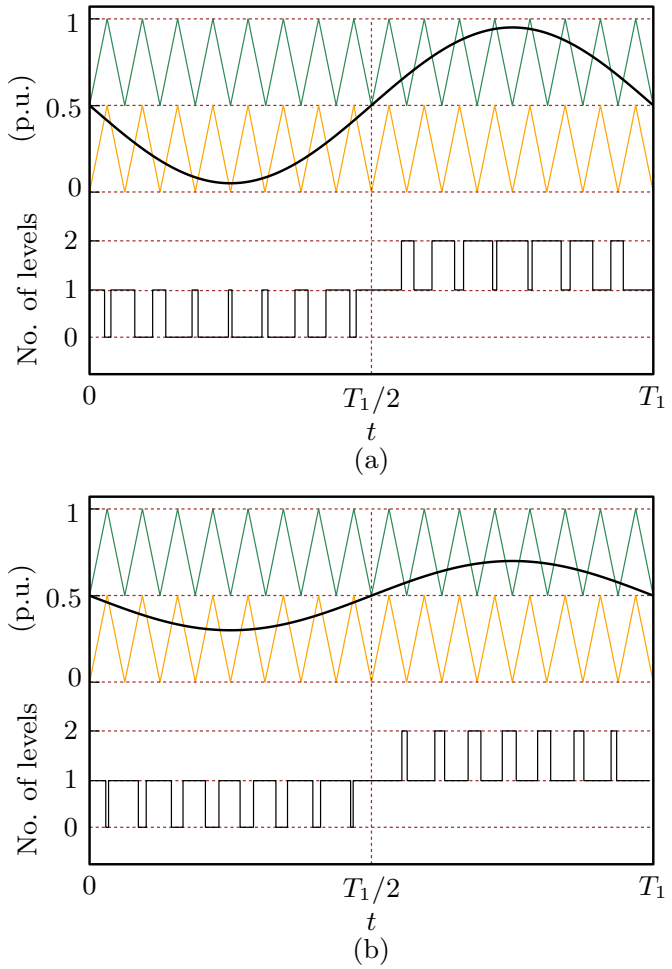


FIGURE 3.5: The number of levels in the upper arm with (a) M=0.8, (b) M=0.5.

frequency of 60 Hz is adopted, as PR regulators provide zero steady-state error for sinusoidal signals. The transfer function of the output voltage PR controller is given by

$$C_{v_\varphi} = k_{p,v_\varphi} + k_{r,v_\varphi} \frac{s}{s^2 + \omega^2} \tag{3.14}$$

where k_{p,v_φ} and k_{r,v_φ} are the proportional and resonant gains, respectively.

The inner current controller is adopted to simplify the design and to provide over-current protection to the inverter [37]. PI regulator with a feed-forward from the output voltage is adopted for the inner loop. The transfer function of the PI controller is given by

$$C_{i_\varphi} = k_{p,i_\varphi} + k_{i,i_\varphi} \frac{1}{s} \tag{3.15}$$

where k_{p,i_φ} and k_{i,i_φ} are the proportional and integral gains, respectively.

A PR circulating current regulator in the *abc* frame, with a resonant frequency of 120 Hz, is adopted to control the second-order harmonics. A low-pass filter is

used to extract the dc-value of the circulating current. The transfer function of the circulating current PR controller is given by

$$C_{i,circ} = k_{p,circ} + k_{r,circ}\frac{s}{s^2 + (2\omega)^2}, \tag{3.16}$$

where $k_{p,circ}$ and $k_{r,circ}$ are the proportional and resonant gains, respectively.

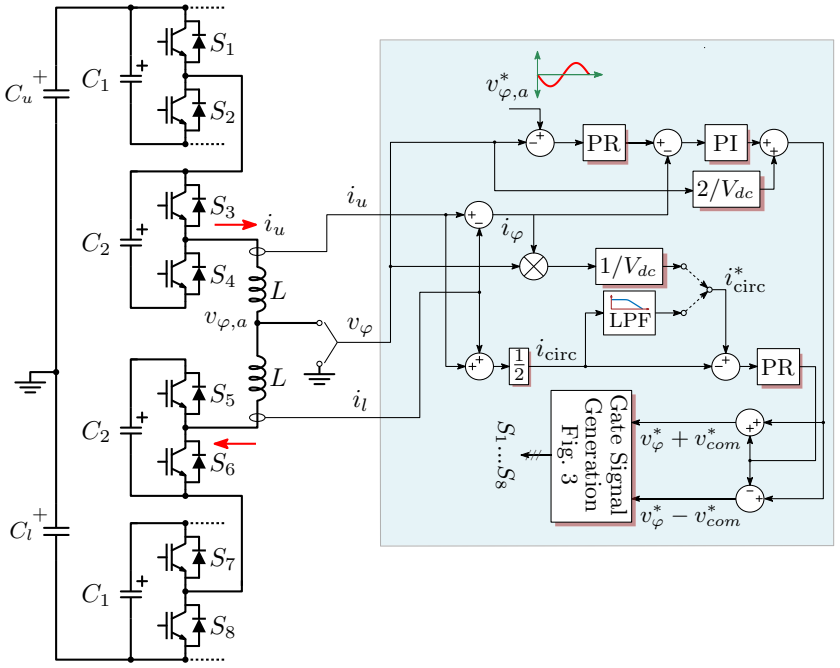


FIGURE 3.6: The control diagram of the proposed five-level modular multilevel converter.

3.3 Simulation Results

To validate the proposed enhanced modulation scheme, a down-scaled MMC prototype has been implemented as shown later in Sec.3.4. Simulation results with the same parameters as the experiment is presented in this section. A three-phase five-level 110 V_{rms}, 2.4 kVA, 60 Hz MMC with two SMs per arm was simulated in PLECS simulation environment. The system parameters are shown in Table. 3.1. The capacitance of the inner SMs is designed based on (2.11) with a 20% peak-to-peak ripple. Both the original PSCs-based modulation scheme and the enhanced one are simulated to show the reduction in the total capacitance requirement. Fig. 3.7(a) and Fig. 3.7(b) depicts simulation results for the original modulation with constant circulating current and controlled second-order injection in the circulating current, respectively. Furthermore, simulation results using the proposed

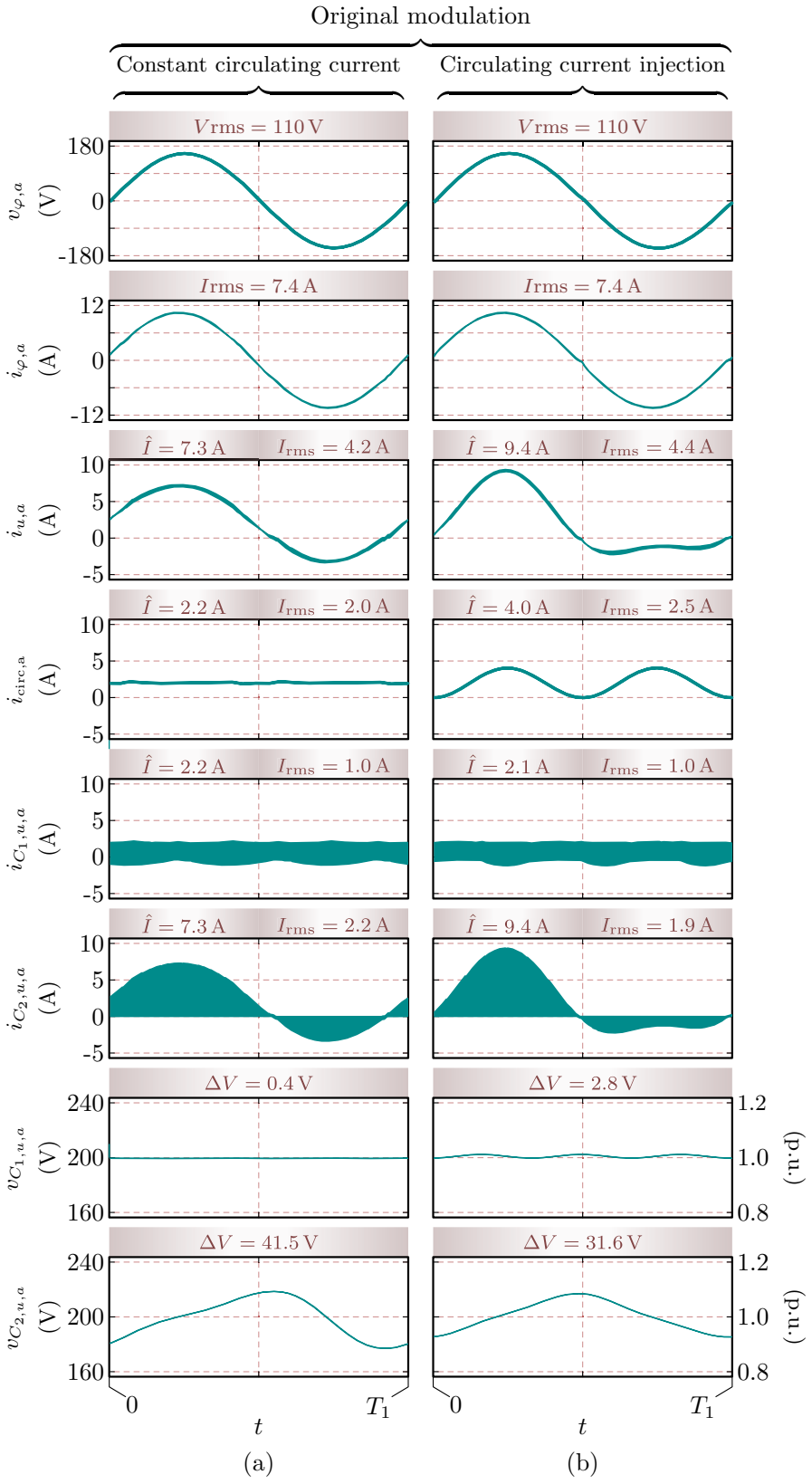


FIGURE 3.7: Simulation results for the original modulation scheme using PLECS with (a) a constant circulating current; (b) a second-order harmonic injection in the circulating current.

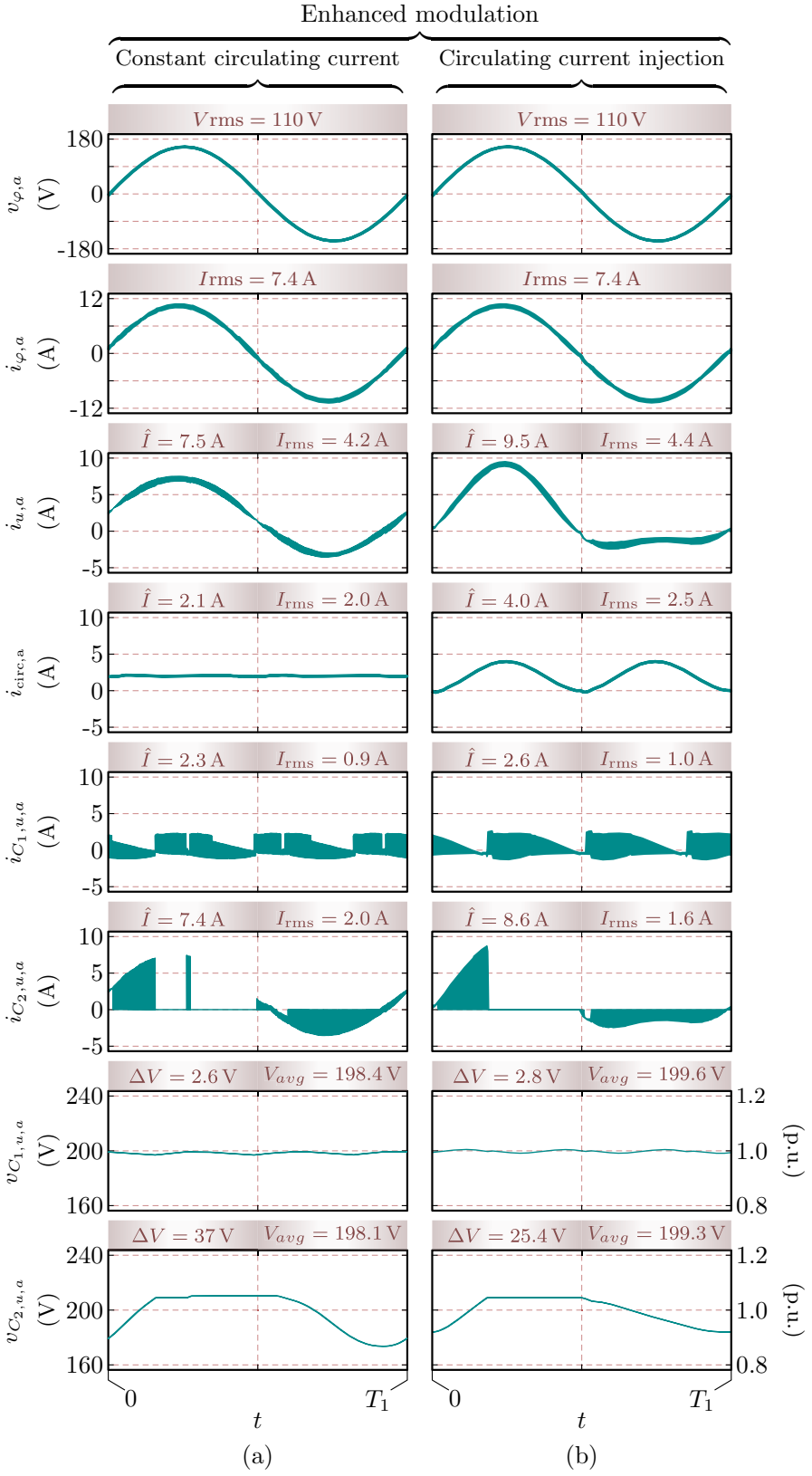


FIGURE 3.8: Simulation results for the proposed modulation scheme using PLECS with (a) a constant circulating current; (b) a second-order harmonic injection in the circulating current.

modulation are shown in Fig. 3.8(a) and Fig. 3.8(b), respectively. The dc-side input voltage is supplied from a constant 400 V dc voltage source. The same capacitors are used for the four cases. A 22.5 μF capacitor with the equivalent ac-side inductance, which is half the arm inductance, form an ac-side LC filter. The ac-side load is a three-phase wye-connected resistance of 15 Ω/phase.

3.3.1 Capacitors Voltages and Currents

The first case study, shown in Fig. 3.7(a), is the one with the original modulation and a constant circulating current that needs to be improved. The circulating current injection solution can reduce the voltage ripple and the rms current of the inner capacitor by 24% and 13.6%, respectively, as shown in Fig. 3.7(b); however, the rms and peak arm current increase by around 4.8% and 28.8%, respectively. The voltage ripple of the external capacitors increases from 0.4 V to 2.8 V. Moreover, the peak value of the inner capacitor current increases by 28.8%.

With the proposed modulation, the reduction of the voltage ripple and the rms current of the inner capacitor are about 11.3% and 9.1%, respectively, as shown in Fig. 3.8(a). In this case, the voltage ripple of the external capacitor increases to 2.5 V, which is less respect to the circulating current injection method. Moreover, the increase in the peak value of the arm current and the inner capacitor current is lower with respect to the circulating current injection.

Fig. 3.8(b) shows the last case study when the two solutions are used simultaneously. The minimum voltage ripple and rms current of the inner capacitor are achieved with a reduction of 40% and 27.3%, respectively. The voltage ripple of the external capacitor increases from 0.4 V to 2.8 V. The peak and rms values of the arm current are almost the same as the original modulation with a circulating current injection.

3.3.2 Semiconductor Power Losses and Currents

In order to evaluate the effect of the proposed modulation technique on the distribution of semiconductor losses, the switching and conduction losses of the switches are calculated using an IGBT model of MMIX1Y100N120C3H1 using PLECS.

Fig. 3.9(a) and Fig. 3.9(b) show the power loss of each IGBT in the upper arm of phase a and the total semiconductor losses in the converter, respectively. It can be noted that since the submodules are not modulated all the time like the

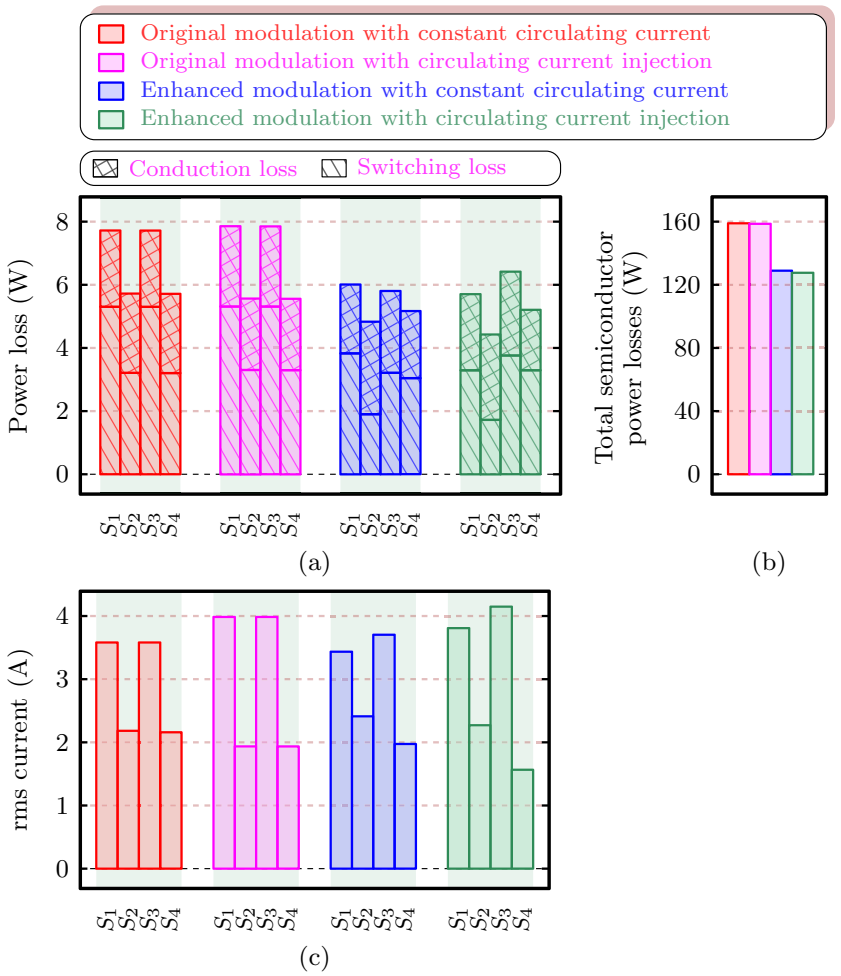


FIGURE 3.9: (a) Distribution of the semiconductor losses in one arm; (b) The total semiconductor losses in the converter; (c) rms current of the different switches in one arm.

original modulation, the semiconductor power losses are reduced and become more uniform with the proposed modulation.

A comparison between the rms currents of the four switches (S_1, S_2, S_3, and S_4) for the upper arm in phase a is shown in Fig. 3.9(c).

With injecting a second-order harmonic in the circulating current, the rms current of the two switches (S_1 and S_3) increases, while the the rms current of the two switches (S_2 and S_4) decreases. By using the proposed modulation without injecting a second-order circulating current, the rms current of the switches is very close to the original modulation.

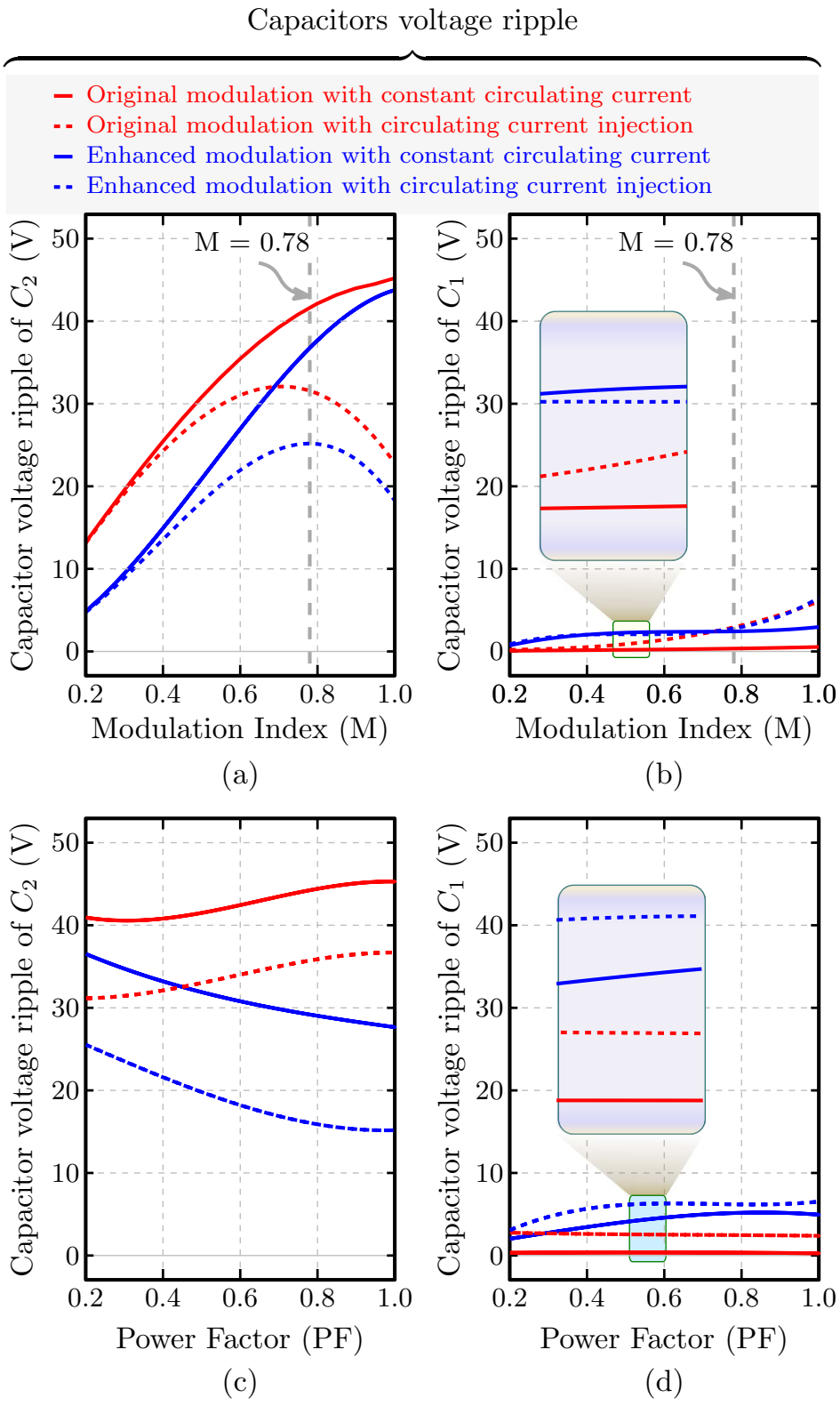
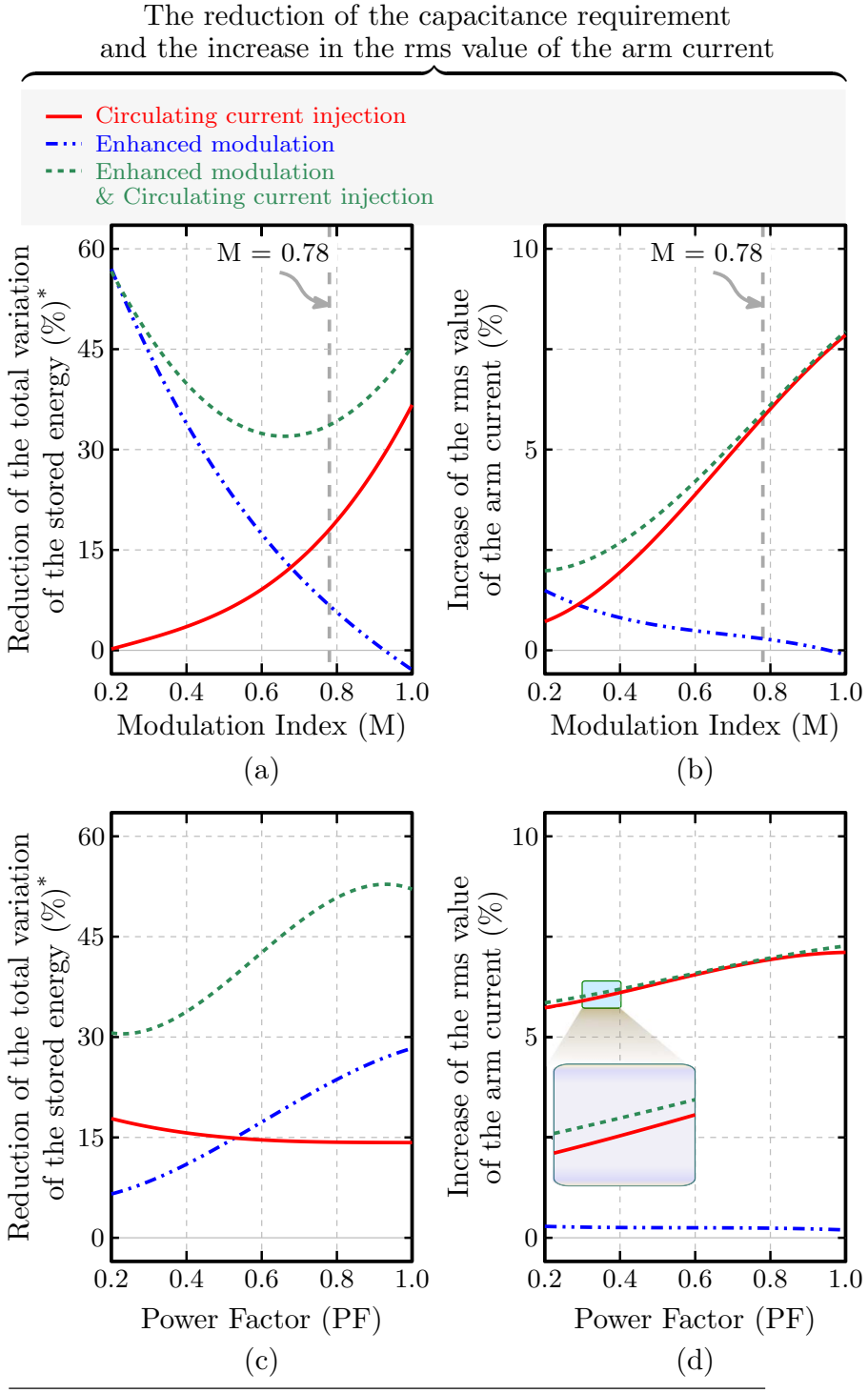


FIGURE 3.10: Comparison between the voltage ripple of the external and inner capacitors under different values of the modulation index and the power factor using the original and the proposed modulation. (a) and (c) The voltage ripple of the inner capacitor; (b) and (d) the voltage ripple of the external capacitor.



* The total variation of the stored energy

$$= \frac{V_{dc}}{2} \sum_{i=a,b,c} \left(C_{1,u,i} \Delta V_{C_{1,u,i}} + C_{2,u,i} \Delta V_{C_{2,u,i}} + C_{1,l,i} \Delta V_{C_{1,l,i}} + C_{2,l,i} \Delta V_{C_{2,l,i}} \right)$$

FIGURE 3.11: Comparison between the overall reduction of the stored energy variation, and the rms value of the arm current under different values of the modulation index and the power factor using the original and the proposed modulation. (a) and (c) The voltage ripple of the inner capacitor; (b) and (d) the voltage ripple of the external capacitor.

3.3.3 The effect of the modulation index

The energy variation of a capacitor during a line period can be expressed as

$$\begin{aligned}\Delta E_C &= \frac{1}{2}C\left(V_{C,av}+\frac{\Delta V}{2}\right)^2-\frac{1}{2}C\left(V_{C,av}-\frac{\Delta V}{2}\right)^2 \\ &= C\,V_{C,av}\Delta V_C.\end{aligned} \tag{3.17}$$

The total variation of the stored energy in the converter is taken as an index on the capacitance requirement reduction [14]. It can be expressed as

$$\begin{aligned}\Delta E = \frac{V_{dc}}{2}\sum_{i=a,b,c}(&C_{1,u,i}\Delta V_{C_{1,u,i}}+C_{2,u,i}\Delta V_{C_{2,u,i}} \\ &+C_{1,l,i}\Delta V_{C_{1,l,i}}+C_{2,l,i}\Delta V_{C_{2,l,i}})\end{aligned} \tag{3.18}$$

assuming that the average voltage of the capacitors is equal to $V_{dc}/2$.

Fig. 3.10(a) summarizes the relationship between the voltage ripple of the inner capacitor (ΔV_{C_2}) and the modulation index (M). As discussed in Sec. 3.2.1, the reduction of ΔV_{C_2}, achieved by the proposed modulation, decreases with an increase of M. As shown in Fig. 3.10b, the voltage ripple of the external capacitors (ΔV_{C_1}) increases with the decrease of M; however, the total variation of the stored energy, shown in Fig. 3.11(a), decreases with the decrease of M as the stored energy in the inner capacitor is dominant. On the other hand, second-order injection in the circulating current is more effective in reducing ΔV_{C_2} and the total energy stored variation of the converter with higher M, as shown in Fig. 3.10(a) and Fig. 3.11(a), respectively. The enhanced modulation and the injection of second-order harmonic can be used simultaneously to achieve a low capacitance requirement on a wide range of operation. Fig. 3.11(b) shows the percentage of increase of the rms value of the arm current in each case. The effect of the proposed modulation on the arm current rms value is negligible for the whole range of operation. However, injecting second-order harmonic in the circulating current increases the arm current rms value with an increase of M.

3.3.4 The effect of the load power factor

The reduction of the total capacitance requirement is also analyzed at different load PF. Fig. 3.10(c) and Fig. 3.10(d) summarizes the relationship between the load PF and the voltage ripple of the inner and the external capacitors, respectively.

As shown in Fig. 3.11(c), the reduction of total energy variation, achieved by the circulating current injection, slightly changes with the load PF with a minimum of 14%. On the other hand, the proposed modulation is highly affected by the load PF.

In conclusion, the minimum variation of the stored energy (minimum capacitance requirement) can be achieved, for the whole range of load power factor and up to 0.85 modulation index, by adopting the proposed modulation and the circulating current injection simultaneously.

3.3.5 Transient response

Fig. 3.12(a) and Fig. 3.12(b) show the transient response of the three-phase MMC in the case of the original and the proposed modulation, respectively. The load is suddenly changed from 30 Ω (half-load) to 15 Ω (full-load) at $t = 0.5\,s$.

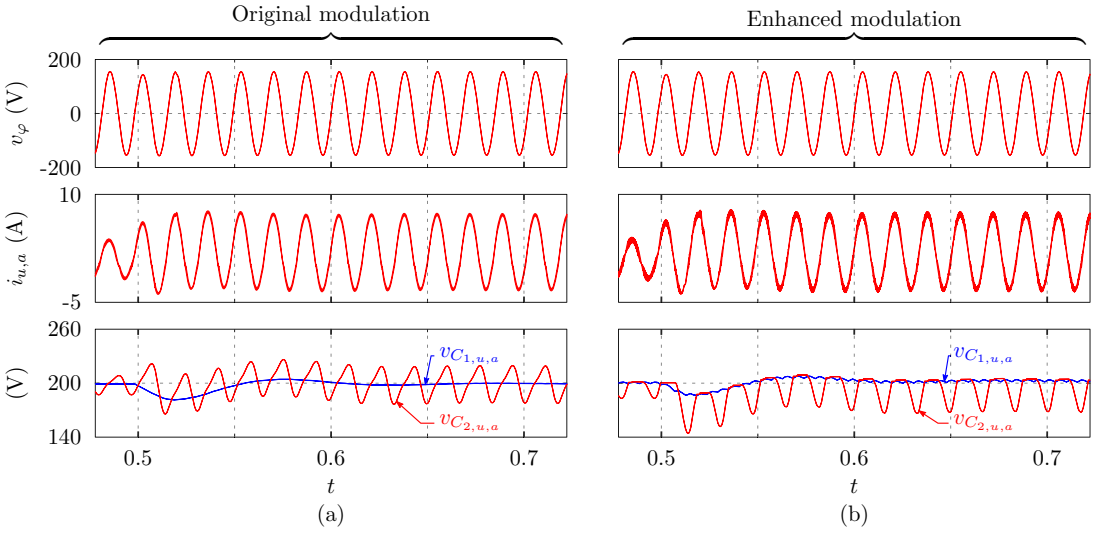


FIGURE 3.12: Transient response of the three-phase five-level Modular Multilevel Converter (MMC) with (a) the original modulation; (b) the proposed modulation.

3.4 Experimental Results

In order to verify the capacitance reduction that can be achieved using the enhanced modulation scheme, a down-scaled three-phase MMC prototype has been implemented, as shown in Fig. 3.13. The software part is running on the BoomBox control platform from IMPERIX. The MMC structure has been built using twelve PEB 8032-A modules from the same company. Each module contains a half-bridge

(two MMIX1Y100N120C3H1 IGBTs and a 260 μF capacitor). The modules are connected as depicted in Fig. 3.1. The converter is supplied from a dc voltage source set to 400 V to get an output phase voltage of 110 V_{rms}. A three-phase wye-connected resistive load of 15 Ω/phase is used. The neutral point of the load and the filter capacitor bank (C_f) are connected to the middle point of the dc bus. The circuit parameters are shown in Table. 3.1.

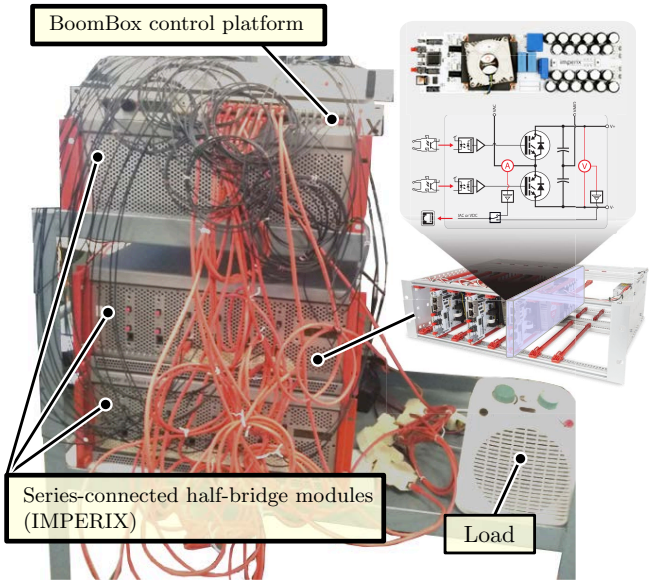
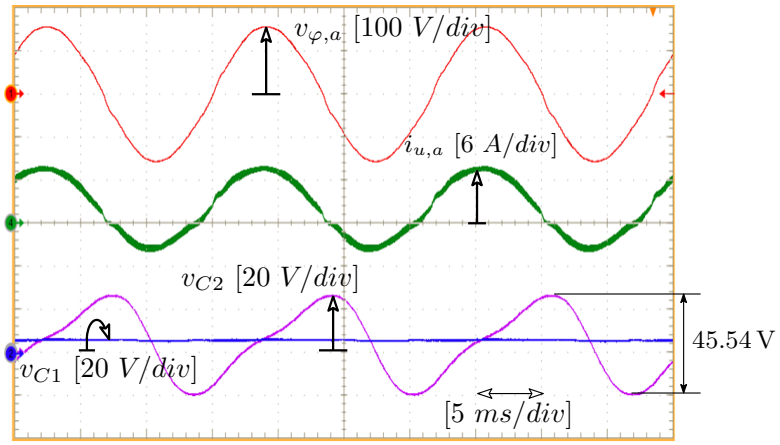


FIGURE 3.13: Photo of the experimental Modular Multilevel Converter (MMC) prototype.

The six arm currents are sampled in order to control the output (differential-mode) current and the circulating (common-mode) current. The circulating current is controlled to be constant by suppressing the second-order harmonic. A PR controller is adopted for both the output and the circulating current loop, as discussed in section 3.2.3. The twelve SM capacitor voltages are measured and sampled to balance the voltages of the capacitors.

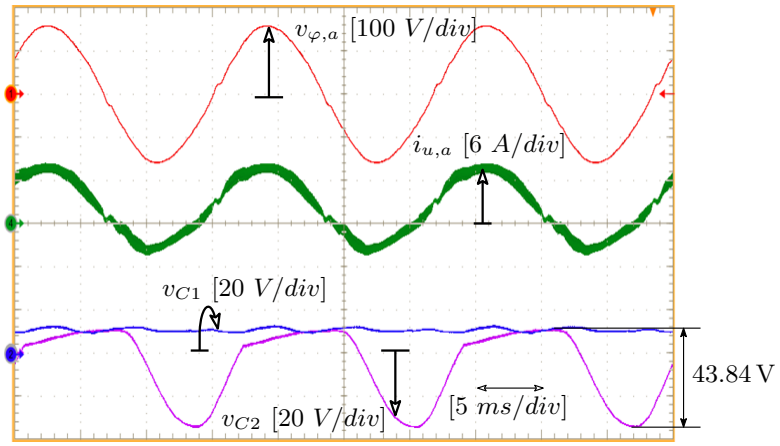
The obtained experimental results with a resistive load are shown in Fig. 3.14 for the upper arm of phase a. Fig. 3.14a and Fig. 3.14b show experimental results using the PSCs modulation and the proposed modulation, respectively.

The voltage ripple of the inner capacitor is reduced from 45.54 V to 43.84 V with a percentage of 4%. However, with a lower modulation index, the percentage of reduction increases, as shown in Fig. 3.15. For example, at a modulation index of 0.7, the reduction is around 15.4%.



v_{C1} and v_{C2} offset: 200V

(A)



v_{C1} and v_{C2} offset: 200V

(B)

FIGURE 3.14: Experimental results for the five-level modified MMC with a constant circulating current control and unity power factor. (a) with the original modulation; (b) with the proposed modulation.

Fig. 3.16 shows experimental results under leading PF operations. Fig. 3.16a and Fig. 3.16b show the results with a 50 μF capacitor is connected in parallel with the 15 Ω resistive load with the original PSCs modulation and the proposed one, respectively. In this case the PF is 0.96. The reduction of the inner capacitor is about 4.6%. Fig. 3.16c and Fig. 3.16d show the experimental results with a 100 μF capacitor connected in parallel with the 15 Ω resistive load with the original PSCs modulation and the proposed one, respectively. The reduction of the voltage ripple of the inner capacitor, in this case, is 9.8%. The load PF of this case is 0.87.

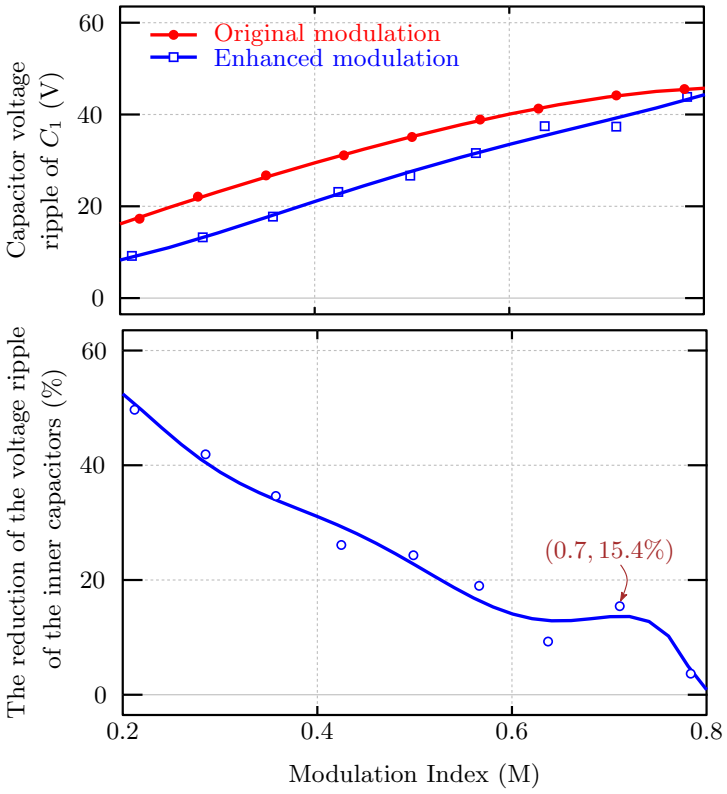


FIGURE 3.15: Experimental results: comparison between the voltage ripple of the inner capacitors with the original PSCs modulation and the proposed modulation at different modulation indices.

3.5 Summary

An enhanced modulation scheme is proposed in this chapter for a three-phase five-level modified MMC where the upper and lower SMs are connected in parallel. This modulation's primary goal is to reduce the voltage ripple of the MMC SMs that require high capacitance. The reference voltages of the various submodules are modified considering the asymmetric voltage ripple of the modified MMC. A balancing and sorting algorithm is considered in the proposed idea to keep the capacitor voltages balanced. It is known that circulating current injection is a practical approach to reduce the voltage ripple of the inner capacitors; however, it is more effective at higher modulation indices, while the proposed modulation is more effective at lower modulation indices. The maximum reduction of the total variation of the stored energy, taken as a measure of the overall capacitance requirement, for the whole range of operation, can be achieved by combining the two solutions. The reduction using the proposed modulation in this chapter, although limited to about $10 - 25\%$ in the expected range of operation, increases the feasibility of using the MMC in medium and low voltage applications as a more reliable, easily expandable, and potentially efficient solution.

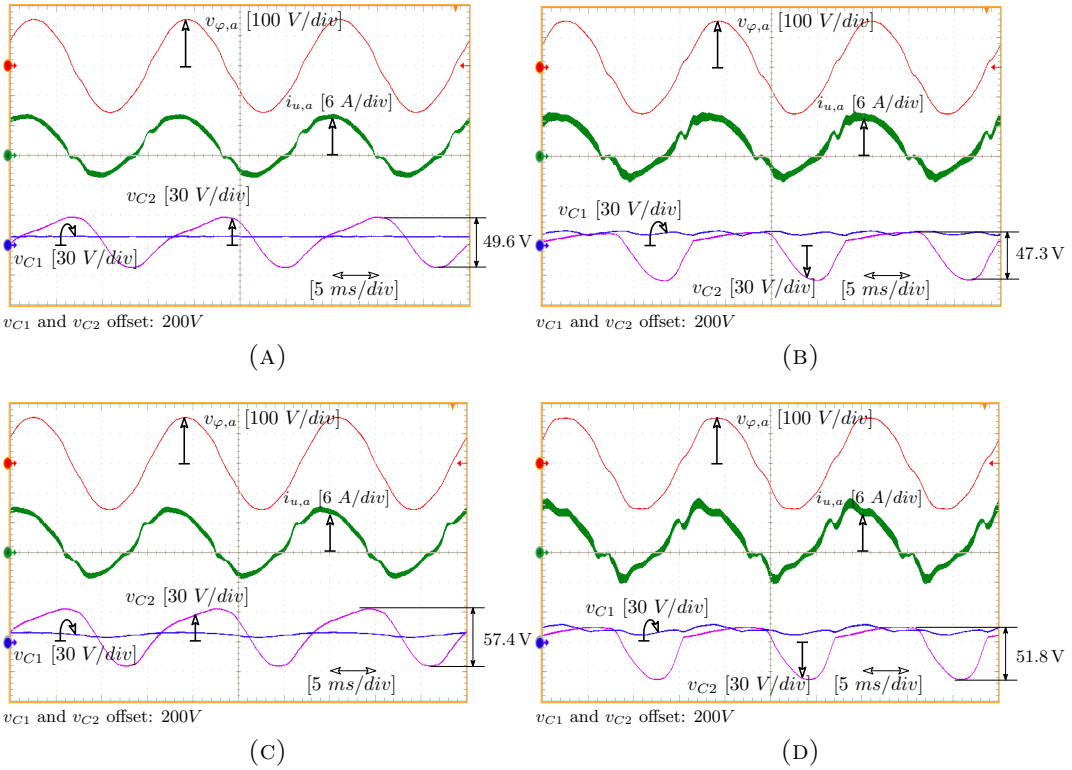


FIGURE 3.16: Experimental results for the five-level modified Modular Multilevel Converter (MMC) with a constant circulating current control. (a) The original modulation and an 0.96 leading Power Factor; (b) The proposed modulation and an 0.96 leading Power Factor; (c) The original modulation and an 0.87 leading Power Factor; (d) The proposed modulation and an 0.87 leading Power Factor.

Chapter 4

Three-phase Modular Multilevel Converter (MMC) with Optimized Capacitor Sizing for Low-Voltage (LV) Applications

This chapter presents the design procedure and development of a modified MMC topology for low voltage applications. With respect to the conventional MMC topologies, the proposed structure is designed and optimized to have a relatively low capacitance requirement. The switching states, modulation, control, and design procedure of the different parameters, including SM capacitor and arm inductor, are investigated in this chapter. Moreover, the control scheme is presented to achieve regulation of the output voltage and the circulating current. The outcomes of this study are verified by simulation and experimental results.

4.1 Principle of Operation, Modulation, and Steady-State Analysis of the Proposed MMC Converter

4.1.1 Proposed MMC Structure

A three-phase three-level MMC is reported in Fig. 4.1(a). The dc bus voltage (V_{dc}) is assumed to be fixed. Each leg of the MMC has two arms (an upper arm and a lower arm) with two SMs per arm. Each SM, in the half-bridge MMC variant, comprises two IGBT units connected in series, and a capacitor. The upper and the

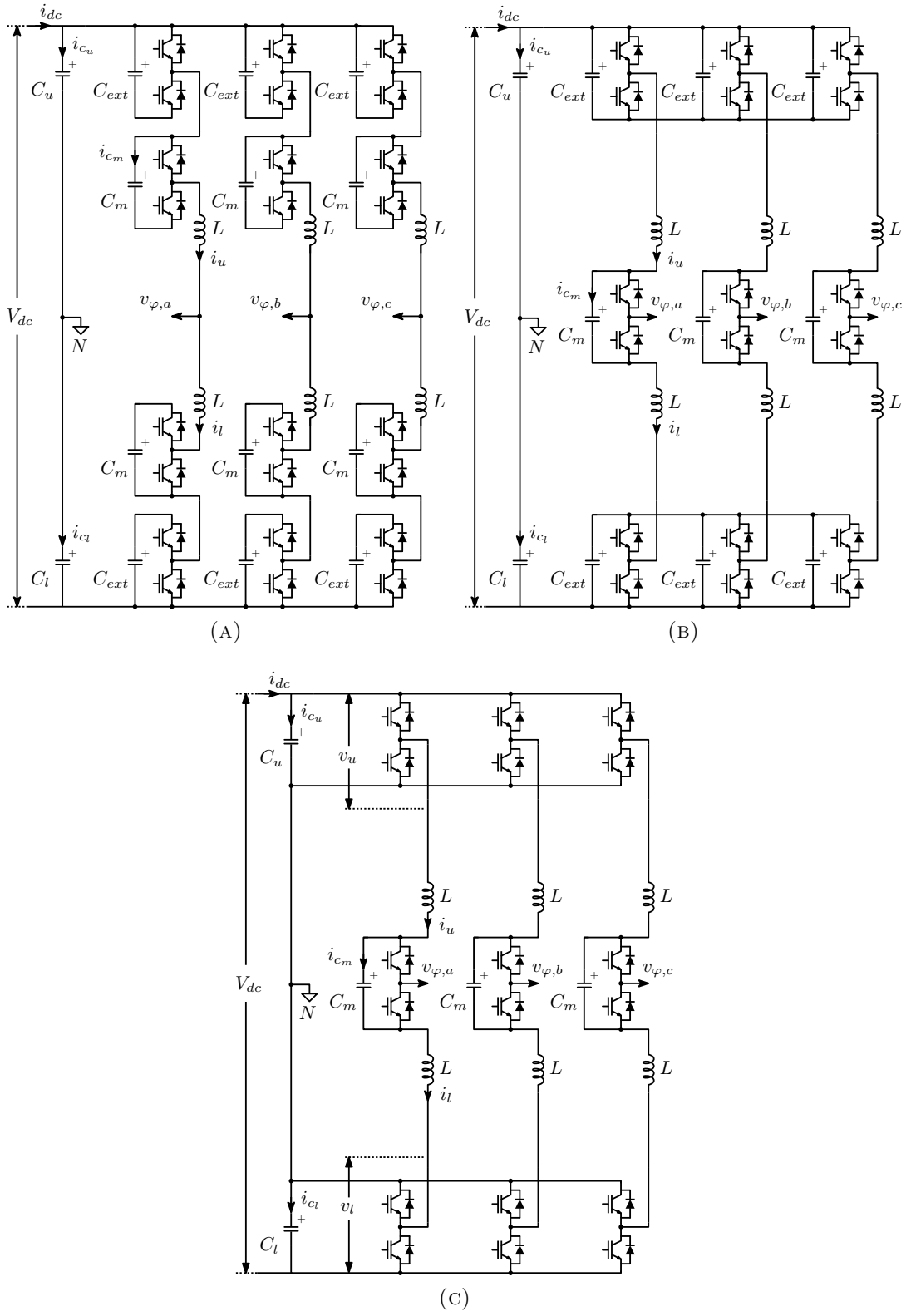


FIGURE 4.1: (a) The conventional three-phase Modular Multilevel Converter (MMC) with two Submodules (SMs) per arm; (b) a modified three-phase MMC proposed in [24] with two SM per arm and a middle SM; (c) the proposed three-phase three-level MMC.

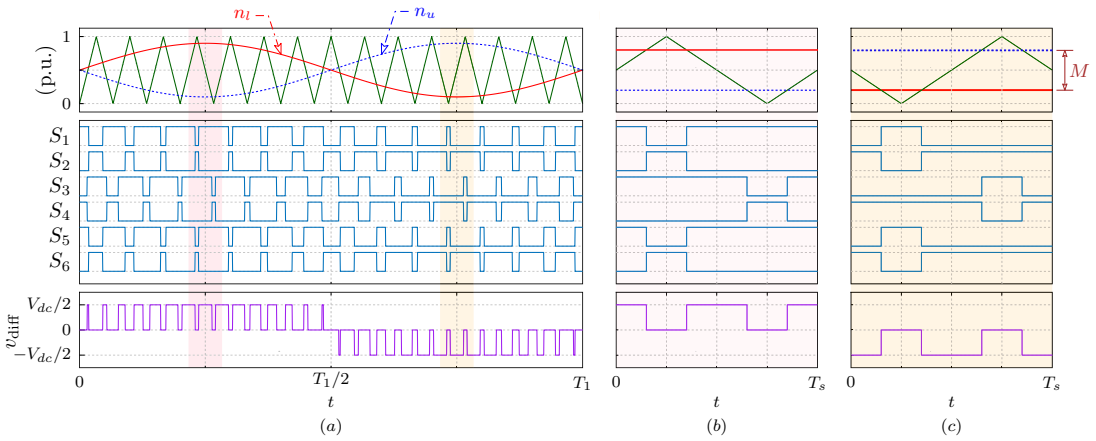


FIGURE 4.2: Modulation technique for the proposed modular Modular Multilevel Converter (MMC) topology. (a) reference, carriers, gate signals for switches S_1 to S_6, and the resultant differential voltage ($v_{\text{diff}} = v_l - v_u$); (b) zoom for one switching cycle when v_{diff} is positive; (c) zoom for one switching cycle when v_{diff} is negative.

lower arms of the same leg are coupled to an output AC terminal of the leg through the inductance (L). The arm voltage is controlled by bypassing or inserting the SM's capacitor into the circuit.

Moreover, the direct current, supplied by the converter's dc-link, splits equally into the three phases. The alternating current also splits equally into the upper and the lower arms of each phase. The number of levels of the output voltage of a three-phase inverter is three if phase voltage to neutral is considered, or five, if the line voltage is considered. In order to reduce the SM capacitance, the MMC scheme, shown in Fig. 4.1(b), is proposed in [24]. Each external capacitor (C_{ext}) in every arm of a phase is connected to the other two corresponding capacitors in the other two phases. Moreover, a middle SM is employed to reduce the required number of SMs/arm by one. The idea of employing a middle SM is originally proposed by [23]. The sum of the three currents is flowing through the external capacitors; therefore, the pulsating current is reduced. This proposed solution can significantly reduce the required capacitance of the external SM of each arm. However, the capacitance reduction obtained from those solutions does not make the MMC a feasible solution for a low voltage application, where still high capacitance relative to the existing topologies, such as FC and NPC, is required.

Motivated by the challenges mentioned above, a three-phase three-level MMC structure, shown in Fig. 4.1(c), is proposed in this chapter. Each leg is composed of three SMs, namely, an upper, a lower, and a middle SM.

The three upper SMs are supplied from the dc-link capacitor (C_u). Similarly, the three lower SMs are connected to the dc-link capacitor (C_l). This feature

is very advantageous for three-phase four-wire ($3\Phi - 4W$) systems. In this way, the two bulky dc-link capacitors, usually already present in $3\Phi - 4W$ systems, are inherently integrated into the structure. The adoption of the proposed MMC structure allows a significant reduction in the number of components and the overall converter size.

It is worth mentioning that the reduction of the capacitance requirements and the number of components either of the modified or the proposed MMC come at the expense of the converter redundancy and modularity, where the optimum choice depends on the application requirements. Moreover, increasing the number of levels beyond three by increasing the number of submodules in each arm is possible; however, each extra SM requires very large capacitance compared with the upper, lower, and middle SM.

The topology variation between the proposed Fig. 4.1(c) and Fig. 4.1(b) implies a different converter operation, as outlined hereafter.

4.1.2 Modulation

The PSCs modulation technique is the most suitable for the MMC with a low number of SMs/arm [35]. The carriers driving the SMs of the same arm are π phase-shifted. The two carriers of the upper arm are $\pi/2$ phase-shifted from the corresponding ones of the lower arm [35].

The modulation technique used to drive the three SMs in each arm, for the proposed structure, is driven from the PSCs modulation, as shown in Fig. 4.2. Two π-shifted reference signals are used. The first one is used to drive the upper and the lower SMs, while the other one is used to drive the middle SM.

4.1.3 Switching States and Gate Signal Generation

Table. 4.1 and Fig. 4.3 show the different possible switching states of the proposed MMC. The circulating current can be controlled using the upper and the lower SMs; therefore, the switching states, in which S_1 and S_2 or S_5 and S_6 are both OFF, are avoided. Accordingly, the highlighted switching states in Table. 4.1 are chosen. In order to generate an output phase voltage (v_φ) of $+V_{dc}/2$, the switches S_1, S_3, and S_5 are turned ON, while S_2, S_4, and S_6 are turned OFF, as shown in Fig. 4.3(a). The zero level can be obtained by either turning ON S_2, S_3, and S_6, or turning ON S_1, S_4, and S_5, as shown in Fig. 4.3(g) and Fig. 4.3(f), respectively.

Switching State	S_1	S_2	S_3	S_4	S_5	S_6	v_{diff}	i_{cm}
P_1	**1**	**0**	**1**	**0**	**1**	**0**	$\frac{V_{dc}}{2}$	-i_φ/2
P_2	0	0	1	0	1	0		-i_φ
P_3	1	0	1	0	0	0		0
O_1	0	0	0	1	1	0	0	0
O_2	0	1	1	0	0	0		0
O_3	**1**	**0**	**0**	**1**	**1**	**0**		i_φ/2
O_4	**0**	**1**	**1**	**0**	**0**	**1**		-i_φ/2
O_5	0	0	1	0	0	1		-i_φ
O_6	1	0	0	1	0	0		i_φ
N_1	**0**	**1**	**0**	**1**	**0**	**1**	-$\frac{V_{dc}}{2}$	i_φ/2
N_2	0	0	0	1	0	1		0
N_3	0	1	0	1	0	0		i_φ

TABLE 4.1: Switching States of the Proposed Modular Multilevel Converter (MMC) topology

For a negative level ($-V_{dc}/2$), the switches S_2, S_4, and S_6 are turned ON, while S_1, S_3, and S_5 are turned OFF, as shown in Fig. 4.3(d).

The generation of the gate signals for the six switches in each phase is shown in Fig. 4.4. The Common-Mode (CM) voltage reference (v^*_{com}) is used to control the CM circulating current, as discussed later in this section.

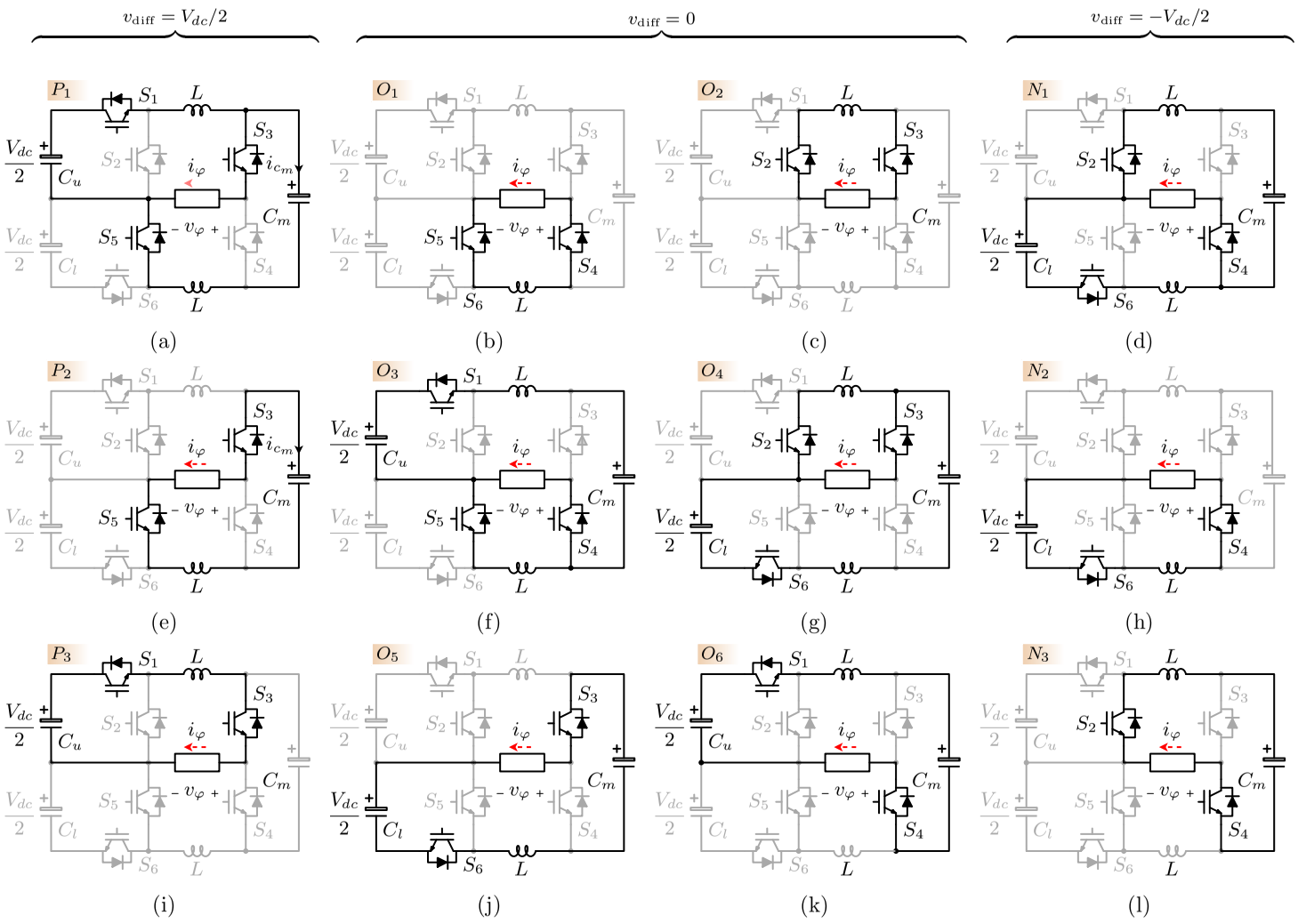


FIGURE 4.3: Switching states of the proposed three-level Modular Multilevel Converter (MMC).

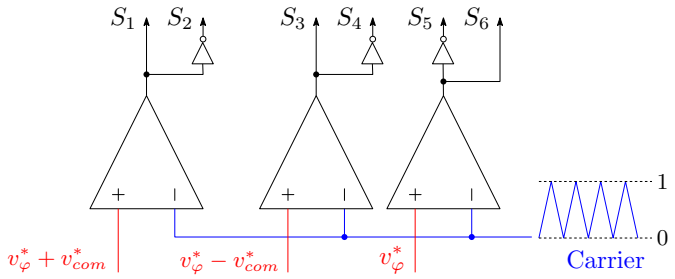
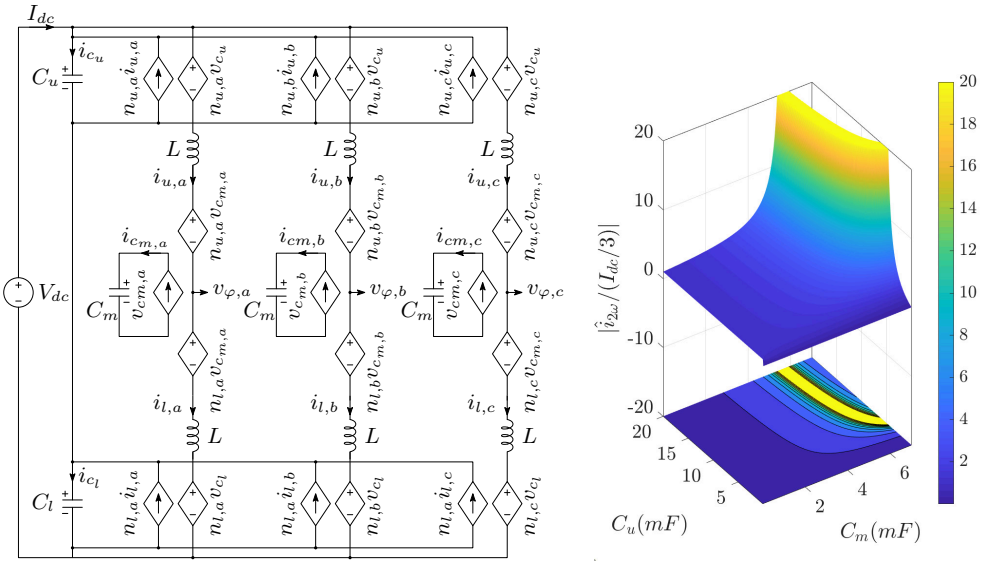


FIGURE 4.4: Gate signal generation for the six switches in each phase. Note that v_φ^* is the differential phase voltage reference, while v_{com}^* is the CM voltage reference.



(A) (B)

FIGURE 4.5: Low frequency analysis for the proposed three-phase MMC topology, (a) average model; (b) the relative amplitude of the second-order component of the circulating current as a function of the SMs capacitance.

4.1.4 Low Frequency Analysis and Design Procedure

Assuming a balanced three-phase system, the output phase voltages of the MMC $(v_{\varphi,a}, v_{\varphi,b}, v_{\varphi,c})$ are expressed by

$$\begin{bmatrix} v_{\varphi,a} \\ v_{\varphi,b} \\ v_{\varphi,c} \end{bmatrix} = \frac{MV_{dc}}{2} \begin{bmatrix} cos(\omega t) \\ cos(\omega t - 2\pi/3) \\ cos(\omega t + 2\pi/3) \end{bmatrix}, \tag{4.1}$$

where ω is the line angular frequency and M is the modulation index.

The output phase currents are expressed by

$$\begin{bmatrix} i_{\varphi,a} \\ i_{\varphi,b} \\ i_{\varphi,c} \end{bmatrix} = \hat{I}_m \begin{bmatrix} cos(\omega t - \varphi) \\ cos(\omega t - 2\pi/3 - \varphi) \\ cos(\omega t + 2\pi/3 - \varphi) \end{bmatrix}, \tag{4.2}$$

where φ is the load PF angle, and $\hat{I}_m$ is the peak value of the phase currents.

In order to generate the output voltages in (4.1), the insertion (modulation) indices of the upper arm SMs (n_u) and the ones of the lower arm (n_l) are calculated from

$$\begin{aligned} \begin{bmatrix} n_{u,a} \\ n_{u,b} \\ n_{u,c} \end{bmatrix} &= \frac{1}{2} - \frac{M}{2} \begin{bmatrix} cos(\omega t) \\ cos(\omega t - 2\pi/3) \\ cos(\omega t + 2\pi/3) \end{bmatrix}, \\ \begin{bmatrix} n_{l,a} \\ n_{l,b} \\ n_{l,c} \end{bmatrix} &= \frac{1}{2} + \frac{M}{2} \begin{bmatrix} cos(\omega t) \\ cos(\omega t - 2\pi/3) \\ cos(\omega t + 2\pi/3) \end{bmatrix}. \end{aligned} \tag{4.3}$$

The output phase current is split equally between the upper and the lower arms. Therefore, the upper arm currents and the lower arm currents are composed of two terms: a differential current, which is half the output phase current, and a CM one (i_{circ}), circulating through the converter.

Accordingly, the upper arm currents ($i_{u,a}, i_{u,b}, i_{u,c}$) and the lower arm currents ($i_{l,a}, i_{l,b}, i_{l,c}$) can be defined, noting that the circulating currents in the three MMC are negative sequence [38], as

$$\begin{bmatrix} i_{u,a} \\ i_{u,b} \\ i_{u,c} \end{bmatrix} = \overbrace{\frac{I_{dc}}{3} + \hat{I}_{circ,2\omega} \begin{bmatrix} cos(2\omega t + \varphi_2) \\ cos(2\omega t + 2\pi/3 + \varphi_2) \\ cos(2\omega t - 2\pi/3 + \varphi_2) \end{bmatrix}}^{i_{circ}} + \underbrace{\frac{\hat{I}_m}{2} \begin{bmatrix} cos(\omega t - \varphi) \\ cos(\omega t - 2\pi/3 - \varphi) \\ cos(\omega t + 2\pi/3 - \varphi) \end{bmatrix}}_{i_\varphi/2}, \tag{4.4}$$

$$\begin{bmatrix} i_{l,a} \\ i_{l,b} \\ i_{l,c} \end{bmatrix} = \overbrace{\frac{I_{dc}}{3} + \hat{I}_{circ,2\omega} \begin{bmatrix} cos(2\omega t + \varphi_2) \\ cos(2\omega t + 2\pi/3 + \varphi_2) \\ cos(2\omega t - 2\pi/3 + \varphi_2) \end{bmatrix}}^{i_{circ}} - \underbrace{\frac{\hat{I}_m}{2} \begin{bmatrix} cos(\omega t - \varphi) \\ cos(\omega t - 2\pi/3 - \varphi) \\ cos(\omega t + 2\pi/3 - \varphi) \end{bmatrix}}_{-i_\varphi/2}, \tag{4.5}$$

where I_{dc} is the total dc current drawn from the dc power supply, $\hat{I}_{circ,2\omega}$ is the amplitude of the second order component of the arm current, and φ_2 is its phase shift.

The term (I_{dc}) is dependent on the power delivered by the inverter which is the total output power (P_{out}), which can be expressed, under the assumption of unity efficiency, as

$$I_{dc} = \frac{P_{out}}{V_{dc}} = \frac{3M\hat{I_m}}{4} cos(\varphi). \tag{4.6}$$

Fig. 4.5(a) shows the average model of the proposed structure based on the model reported in [39], assuming a relatively high switching frequency.

Applying Kirchhoff's current law at the upper terminal of the capacitor C_u and substituting (4.3), (4.4) and (4.6), the capacitor current (i_{c_u}) and voltage (v_{c_u}) of the upper dc-link capacitor (C_u) are expressed as

$$\begin{aligned} i_{c_u} &= I_{dc} - (1-n_{u,a})i_{u,a} - (1-n_{u,b})i_{u,b} - (1-n_{u,c})i_{u,c} \\ &= -\frac{3M\hat{I}_{circ,2\omega}}{4}\, cos(3\omega t + \varphi_2), \\ v_{c_u} &= \frac{V_{dc}}{2} - \frac{M\hat{I}_{circ,2\omega}}{4\omega C_u}\, sin(3\omega t + \varphi_2). \end{aligned} \tag{4.7}$$

Similarly, the capacitor current (i_{c_l}) and voltage (v_{c_l}) of the lower dc-link capacitor (C_l) can be calculated from

$$\begin{aligned} i_{c_l} &= I_{dc} - (1-n_{l,a})i_{l,a} - (1-n_{l,b})i_{l,b} - (1-n_{l,c})i_{l,c} \\ &= \frac{3M\hat{I}_{circ,2\omega}}{4}\, cos(3\omega t + \varphi_2), \\ v_{c_l} &= \frac{V_{dc}}{2} + \frac{M\hat{I}_{circ,2\omega}}{4\omega C_l}\, sin(3\omega t + \varphi_2). \end{aligned} \tag{4.8}$$

From (4.7) and (4.8) it can be noted that the capacitor voltage of the upper and the lower SMs, beside the dc component, have only a third-order component which depends on the magnitude of the circulating current ($\hat{i}_{2\omega}$).

The middle capacitor current (i_{c_m}) and voltage (v_{c_m}) are expressed as

$$\begin{aligned} i_{c_m} &= \hat{I}_{circ,2\omega} cos(2\omega t + \varphi_2) - \frac{M\hat{I}_{\varphi}}{4}\, cos(2\omega t - \varphi), \\ v_{c_m} &= \frac{V_{dc}}{2} + \frac{\hat{I}_{circ,2\omega}}{2\omega C_m}\, sin(2\omega t + \varphi_2) - \frac{M\hat{I}_m}{8\omega C_m}\, sin(2\omega t - \varphi). \end{aligned} \tag{4.9}$$

From the average model shown in Fig. 4.5(a), the circulating current (i_{circ}) can be calculated from

$$i_{circ} = \frac{1}{2L}\int \left(V_{dc} - n_{u,a}v_{c_u} - v_{c_m} - n_{l,a}v_{c_l}\right) dt. \tag{4.10}$$

By substituting (4.3), (4.7), (4.8) and (4.9) in (4.10), the amplitude and the phase of the second order component of the circulating current can be calculated from

$$\hat{I}_{circ,2\omega} = \left[\frac{1}{\left(\frac{M^2}{4}\frac{C_m}{C_u} - 8C_m L\omega^2\right) + 1}\right]\frac{M\hat{I}_{\varphi}}{4}, \tag{4.11}$$

$$\varphi_2 = -\varphi, \tag{4.12}$$

where the upper SMs capacitance (C_u) and the lower SMs capacitance (C_l) are assumed to be equal.

Substituting (4.12) in (4.7), (4.8), and (4.9), the peak-to-peak voltage ripple of the upper (ΔV_{c_u}), the lower (ΔV_{c_l}), and the middle (ΔV_{c_m}) capacitors can be expressed as

$$\begin{aligned} \Delta V_{c_u} &= \Delta V_{c_l} = \frac{M\hat{I}_{circ,2\omega}}{2\omega C_u}, \\ \Delta V_{c_m} &= \frac{1}{\omega C_m}\left|\hat{I}_{circ,2\omega} - \frac{M\hat{I}_m}{4}\right|, \end{aligned} \tag{4.13}$$

where $|.|$ denotes absolute value.

From (4.11) and (4.13) it can be noted that, in the absence of circulating current control, both the arm inductance and the SM capacitance values influence the circulating current and, accordingly, the capacitor voltage ripple. Moreover, a resonance could happen at certain values. Fig. 4.5(b) shows the relative amplitude of the second-order circulating current as a function of C_u and C_m using the parameters adopted in Table 4.3

In order to limit the amplitude of the second-order circulating current, it has to be controlled. In this case, its amplitude and phase depend on the adopted control strategy.

According to (4.13), two extreme cases for the second-order component of the circulating current ($\hat{I}_{circ,2\omega}$) can be identified. On the one hand, if $\hat{I}_{circ,2\omega}$ is controlled to be zero, the peak-to-peak capacitor voltage ripple for the upper and

$i_{circ,2\omega}$	ΔV
0	$\Delta V_{c_u} = \Delta V_{c_l} = 0$ $\Delta V_{c_m} = \frac{M\hat{I}_m}{4\omega C_m}$
$\frac{M\hat{i}_m}{4} cos(2\omega t - \varphi)$	$\Delta V_{c_u} = \Delta V_{c_l} = \frac{M^2\hat{I}_m}{8\omega C_u}$ $\Delta V_{c_m} = 0$

TABLE 4.2: The Relationship Between The Circulating Current of Phase a and The Voltage Ripples of The Different Capacitors

the lower SM capacitors becomes, theoretically, zero, while the one of the middle SM capacitor reaches its maximum. On the other hand, if $\hat{I}_{circ,2\omega}$ is controlled to be $M\hat{I}_m/4$, the peak-to-peak capacitor voltage ripple for the upper and the lower SM capacitors reaches its maximum, while the one of the middle SM capacitor becomes, theoretically, zero. From the capacitor requirement standpoint, this is the most interesting solution as the two bulky capacitors at the dc side are already present in $3\Phi - 4W$ systems. Table. 4.2 summarizes the relationship between the circulating current and the voltage ripple. The circulating current can be controlled to achieve an optimum solution for SM capacitance and losses (i.e., the peak value of the arm current).

4.1.5 Control Design

Fig. 4.6(a) depicts the control diagram used to control the output phase voltage and the circulating current control. A single-loop voltage regulator is possible; however, multi-loop voltage control with an inner current loop can actively damp the output filter resonance oscillation [40]. Moreover, it provides over-current protection during faults or abnormal conditions [37].

The voltage control loop includes an inner current loop with a simple PI regulator and a feed-forward from the output voltage in order to damp the resonance oscillation. The difference between the upper arm current (i_u) and the lower arm current (i_l) is utilized as a feedback for the inner current loop. The transfer function of the PI regulator is

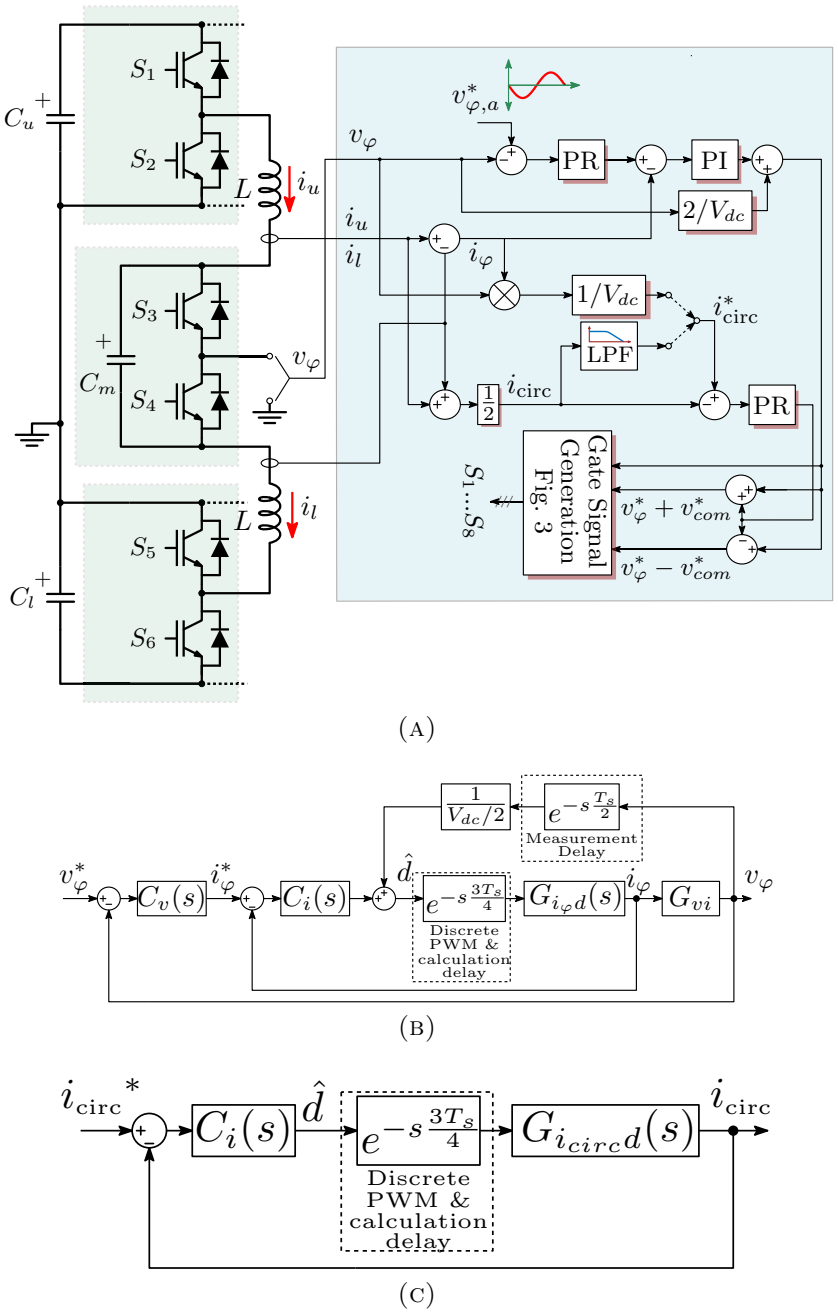


FIGURE 4.6: Closed-loop control diagram for the proposed MMC. (a) A control scheme of the proposed topology; (b) a block diagram for the linearized model of the output voltage loop; (c) a block diagram for the linearized model of the circulating current loop.

$$C_{i_\varphi} = k_{p,i_\varphi} + k_{i,i_\varphi}\frac{1}{s}, \tag{4.14}$$

where k_{p,i_φ} and k_{i,i_φ} are the proportional and the integral gains, respectively.

In a stationary reference frame, a simple PI regulator is not enough to eliminate

the steady-state error of a sinusoidal reference; therefore, a PR regulator is used with a resonant frequency at the line frequency (f_1). The transfer function of the PR regulator can be expressed as

$$C_{v,v_\varphi} = k_{p,v_\varphi} + k_{r,v_\varphi}\frac{s}{s^2+\omega_1^2}, \tag{4.15}$$

where k_{p,v_φ} and k_{r,v_φ} are the proportional and the resonant gains, respectively. The control parameters are designed according to the linearized model shown in Fig. 4.6(b).

As discussed in Sec. 4.1.4, the circulating current affects the converter's efficiency and the capacitor voltage oscillation; therefore, it has to be controlled. Similar to the output voltage control, as the PI regulator does not provide enough gain at the double line frequency, a PR regulator in the stationary reference frame with a resonant frequency at $2f_1$ is adopted. The transfer function of the circulating current PR regulator is expressed as

$$C_{i,circ} = k_{p,circ} + k_{r,circ}\frac{s}{s^2+(2\omega_1)^2}, \tag{4.16}$$

where $k_{p,circ}$ and $k_{r,circ}$ are the proportional and the resonant gains, respectively. The control parameters are designed according to the linearized model shown in Fig. 4.6(c).

As seen in Table 4.2, for maximum efficiency (minimum arm current), the second-order harmonic of the circulating current has to be eliminated. In this case, the voltage ripple of the middle capacitor reaches its maximum. On the other hand, for minimum voltage ripple (less middle capacitance), a second-order harmonic needs to be injected.

The single-phase apparent power can be written as

$$\begin{aligned} S_{ph} = v_\varphi i_\varphi &= \frac{v\hat{V}_m\hat{I}_m}{2}\,cos(\varphi) + \frac{\hat{V}_m\hat{I}_m}{2}\,cos(2\omega t-\varphi) \\ &= \frac{MV_{dc}\hat{i}_\varphi}{4}\,cos(\varphi) + \frac{MV_{dc}\hat{I}_m}{4}\,cos(2\omega t-\varphi), \end{aligned} \tag{4.17}$$

By substituting (4.6) and (4.12) in (4.4), the circulating current can be rewritten as

Rated power (S)	30 kVA
Input voltage (V_{dc})	800 V
Output line voltage (V_{φ})	400_{rms} V
Line frequency (f_1)	50 Hz
Switching frequency (f_s)	10 kHz
Arm inductance (L)	240 μH
Upper SM capacitance (C_u)	12 mF
Lower SM capacitance (C_l)	12 mF
Middle SM capacitance (C_m)	300 μF
Output filter capacitance (C_f)	325 μF

TABLE 4.3: Specifications of The Simulated Three-Phase MMC Converter

$$i_{circ} = \frac{M\hat{I}_m}{4}\, cos(\varphi) + \hat{I}_{circ,2\omega}\, cos(2\omega t - \varphi). \tag{4.18}$$

By inspection of (4.17), (4.18) and Table 4.2, it can be noted that the reference current of the circulating current in the second-order injection mode can be generated from the instantaneous value of the single-phase apparent power divided by V_{dc}. If a constant circulating current is required, only a low-pass filter for the circulating current is needed as shown in Fig. 4.6(a).

4.2 Simulation Results

A 230 V_{rms} 30 kVA simulation model with the parameters listed in Table 4.3 has been developed to verify the performance of the proposed topology, in which an output voltage control is implemented. Three different conditions are considered for the circulating current control: a) control disabled; b) current reference generated from the output phase voltage, as previously discussed in Sec. 4.1.5; c) constant circulating current. The three case studies are discussed in details below.

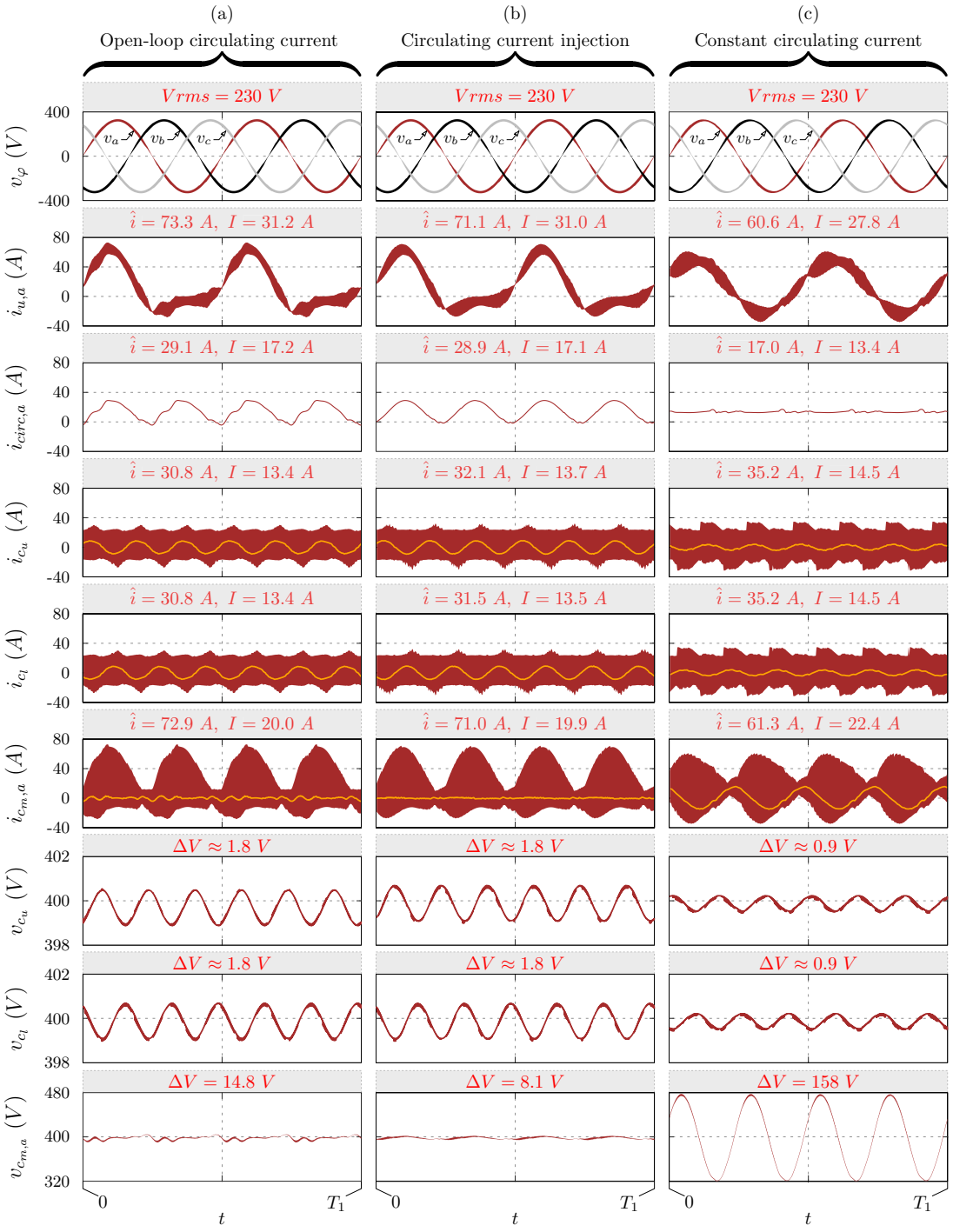


FIGURE 4.7: Simulation results for the proposed topology. Note that ΔV, I, $\hat{I}$ are the peak-to-peak voltage ripple, the rms current, and the peak current, respectively. T_1 is the fundamental period of the output voltage. The orange waveforms are the low-frequency components.

4.2.1 Open-loop Circulating Current Control

Fig. 4.7(a) shows the simulation results with a disabled circulating current control. The arm current is mainly composed of a first-order harmonic and a dc component, as well as an uncontrolled second-order harmonic. As discussed before, the magnitude and phase of first-order harmonic are directly related to the output current. However, the magnitude of the second-order component is related to the circuit parameters, i.e. the arm inductance (L), the dc-side capacitance (C_u) and the middle capacitance (C_m). The peak value of the circulating current can be estimated as the sum of the dc-component reported in Fig. 4.7(a) (i.e. 17.2 A) and the amplitude of the second-order component calculated with (4.11), where parameters listed in Table. 4.3 are adopted. An analytical value of 30 A is obtained, which is very close to the results obtained by the simulation (i.e. 29.1 A). It is clear also from the simulation results that the capacitor current of the upper and the lower capacitors is composed mainly of high-frequency components, as well as a third-order harmonic with the amplitude calculated from (4.7).

4.2.2 Circulating Current Injection Control

With an enabled circulating current control, similar results can be obtained by injecting a second-order harmonic where the reference current is generated by (4.17) divided by V_{dc}. Simulation results for this mode of operation are shown in Fig. 4.7(b). The reference current can be multiplied by a factor ranging from 0 to 1.0 to have a specific voltage ripple in the middle capacitance. By lowering the amplitude of second-order harmonic, the peak arm current becomes lower, but the voltage ripple in the middle capacitor increases, hence, a larger capacitance is needed.

4.2.3 Constant Circulating Current Control

The minimum arm current amplitude is obtained by setting the amplitude of the second-order component to 0. In this case, the voltage ripple of the middle capacitor becomes maximum. Simulation results for this mode of operation are shown in Fig. 4.7(c). By considering relationship (4.13), the peak-to-peak voltage ripple is found to be around 155 V. The error between the analytical calculation and the obtained results is only about 2%.

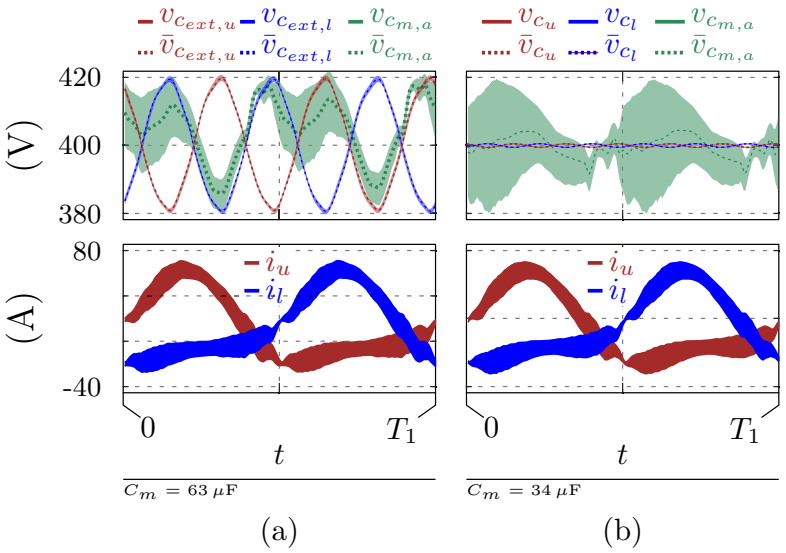


FIGURE 4.8: Comparison between the voltage ripple of the middle capacitor with a second-order injection in the circulating current of a) the modified MMC; b) the proposed MMC.

4.2.4 Energy Storage Requirement

The middle capacitor's voltage ripple in the modified MMC is higher due to the higher voltage ripple of the external capacitors. For example, with a second-order injection in the circulating current, the load is supplied mostly from the upper arm during the positive half cycle, as shown in Fig. 4.8; therefore, the external capacitor's voltage ripple of the upper arm is reflected on the middle capacitor's voltage. Similarly, the external capacitor's voltage ripple of the lower arm is reflected on the middle capacitor's voltage during the negative half cycle of the load. As the upper and lower SMs of the proposed MMC is supplied from the dc-link capacitors, the middle capacitor's voltage ripple is minimal.

MMC's energy storage requirements depend on the amplitude of the second-order component injected in the circulating current. Fig. 4.9 shows a comparison between the three topologies: the conventional, the modified, and the proposed MMC using a simulation with the same input and output parameters. The capacitor voltage ripple is kept 10% of the average capacitor voltage in all the cases. Fig. 4.9(a) shows the variation of the required capacitance for the external SMs (C_{ext}), in the conventional and the modified MMC, versus the circulating current injection ratio ($k_{circ,2\omega}$), where $k_{circ,2\omega} = \hat{I}_{circ,2\omega}/(M\hat{I}_{\varphi}/4)$. Fig. 4.9(b) shows the variation of the required capacitance for the middle SMs (C_m) with the variation of $k_{circ,2\omega}$. According to Table. 4.2, which is also applicable for the modified MMC, with the increase of the circulating current injection ratio, the voltage ripple of the capacitors supplying the external SMs increases, while the voltage ripple of the

middle capacitors decreases. For the same voltage ripple, the proposed topology requires less middle capacitance compared with the modified one; for example, at $k_{circ,2\omega} = 1$, a capacitance of $63\mu F$ is needed in the modified capacitance while a $34\mu F$ is required for the proposed one. Fig. 4.9(c) and Fig. 4.9(d) show the rms and peak values of the arm currents, respectively. The rms and peak values of the arm currents increase with the increase of $k_{circ,2\omega}$. The total stored energy, excluding the dc-link capacitors, is taken as a measure of the overall capacitance requirements in the case of the modified and the proposed MMC topologies respect to the conventional MMC. The total stored energy of the three topologies is expressed as

$$\begin{aligned} E_{\text{conv}} &= 6\left(\frac{1}{2}C_m\left(\frac{V_{dc}}{2}\right)^2\right) + 6\left(\frac{1}{2}C_{ext}\left(\frac{V_{dc}}{2}\right)^2\right), \\ E_{\text{modified}} &= 3\left(\frac{1}{2}C_m\left(\frac{V_{dc}}{2}\right)^2\right) + 6\left(\frac{1}{2}C_{ext}\left(\frac{V_{dc}}{2}\right)^2\right), \\ E_{\text{proposed}} &= 3\left(\frac{1}{2}C_m\left(\frac{V_{dc}}{2}\right)^2\right). \end{aligned} \tag{4.19}$$

where it has been assumed that the bulky dc capacitors are already present in the system and they are not included in the comparison, as present in all three solutions. The reduction of the total stored energy is shown in Fig. 4.9(e). At constant circulating current ($k_{circ,2\omega} = 0$), a relatively small capacitance is required for (C_{ext}) in the case of the modified MMC; therefore, the reduction achieved by the modified and the proposed MMC topologies respect to the conventional one are close to each other (86.7% and 87.3%, respectively). With the increase of $k_{circ,2\omega}$, more capacitance is needed for the external SMs while less capacitance is required for the middle ones. Accordingly, the reduction obtained by the proposed topology becomes more with an increase of $k_{circ,2\omega}$. The obtained reduction of the total stored energy is 90%, at $k_{circ,2\omega} = 1$, concerning the modified MMC and 99.5% with respect to the conventional one. It is worth mentioning that the number of components is also significantly reduced from 9 capacitors to 3 capacitors. Determining a solution that minimizes the capacitance and the rms current (converter losses) requires a tradeoff where the performance indexes are weighted according to a specific application and design requirements.

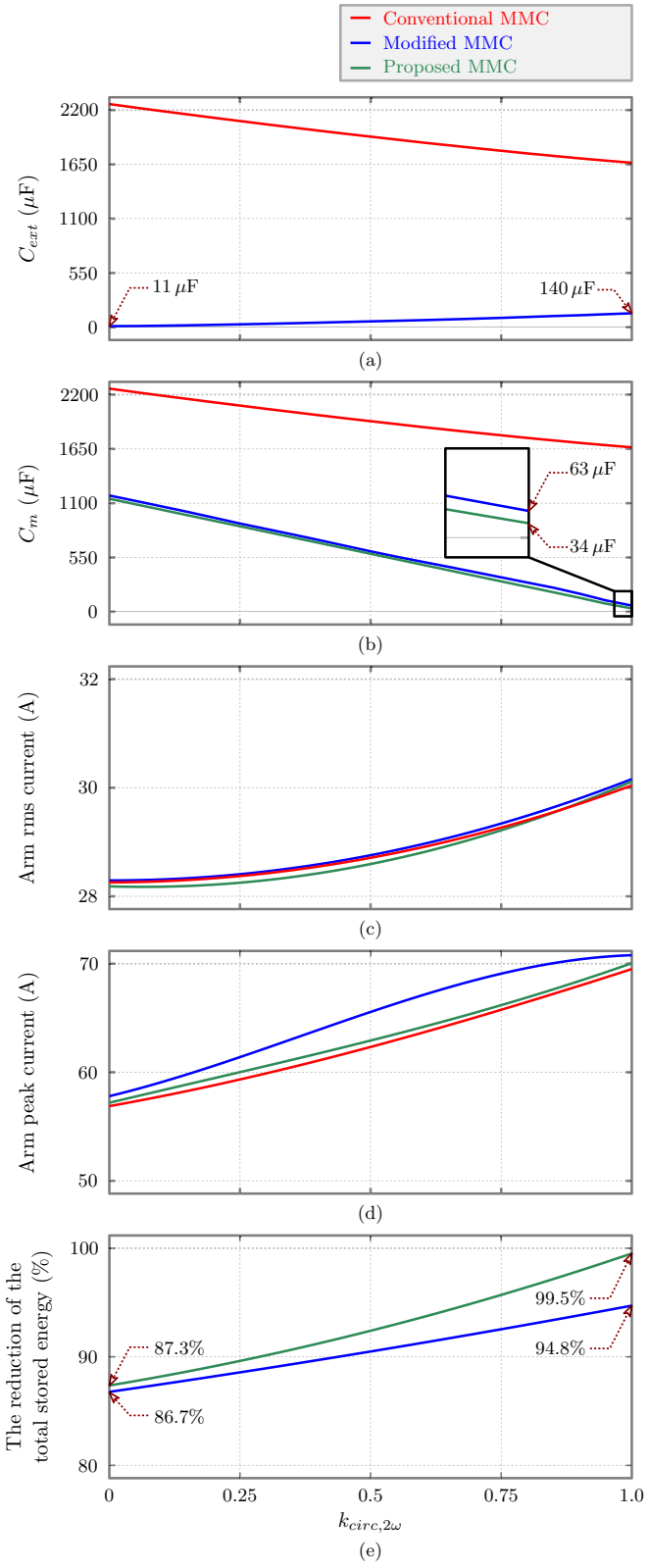


FIGURE 4.9: Comparison between the three topologies: conventional, modified, and proposed topologies. (a) The external capacitance (C_{ext}); (b) The middle capacitance (C_m); (c) The arm rms current; (d) The arm peak current; (e) the reduction of the total stored energy of the modified and the proposed topologies respect to the conventional one.

4.2.5 Comparison with state-of-the-art LV topologies

The stray inductance of long commutation loops in the three-level topologies such as 3L-NPC, 3L-FC, and T-type impose a practical limitation on application to LV high current applications. Due to the long commutation loop, potentially destructive high voltage overshoots appear across the semiconductor devices [41, 42].

The main interesting characteristic of the proposed structure is the smaller commutation loops compared to 3L-NPC, 3L-FC, and T-type. This feature reduces the voltage overshoot over the switches, reduces the converter EMI, and increases the power capability due to the smaller loop inductance. However, it is worthy to compare the number of passive and active components of the proposed topology to the state-of-the-art LV topologies. Table. 4.4 shows a comparison between different three-level topologies considering the number of switches, capacitors, inductors, and maximum switch voltage.

The proposed structure requires the same number of semiconductors as the NPC. It should be noted that the switches of the ANPC must be overrated due to the voltage overshoot. One more inductor is required for the proposed MMC; however, these two inductors reduce the input current ripple and limit the current in case of fault. Moreover, the peak current of the arm inductors is lower in the case of the proposed MMC, as shown in Table. 4.4.

	3L T-type	3L-FC	3L-ANPC	Proposed MMC
No. of switches	4	4	6	6
Max. switch voltage	V_{dc}	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
No. of capacitors	2	3	2	3
No. of inductors	1 (61 A_{pk})	1 (61 A_{pk})	1 (61 A_{pk})	2 (43 A_{pk})

TABLE 4.4: Comparison between 3L-ANPC, 3L T-type, 3L-FC and the proposed MMC

4.3 Experimental Validation

The experimental setup, aimed at validating the performance of the proposed topology, is shown in Fig. 4.10. Fig. 4.11 shows the relationship between the dc-side capacitance and the relative amplitude of the second-order component of the circulating current substituting the simulation parameters in Table. 4.5 into (4.11). It can be noted that the effect of increasing the dc-side capacitance,

above the 12 mF used in the simulation, is minimal. Therefore, the analysis and simulation results reported in this chapter can be validated using a single-phase MMC prototype using two fixed dc voltage sources.

A low-voltage single-phase prototype of the proposed MMC converter has been developed to experimentally validate the analytical analysis and simulations. The inverter is supplied with a dc voltage of 800 V and an output resistive load is considered. The parameters are listed in Table. 4.5. As shown in Fig. 4.6(a), the phase includes three half-bridge SMs. Each SM consists of a SEMIKRON SSEMiX402GB066HDs IGBT Module rated at 600 V and 400 A, and a capacitor. Two voltage sources, 400 V each, are used to supply the upper and the lower SMs, while, a 300 μF is used to supply the middle one. A DSP-based board is used

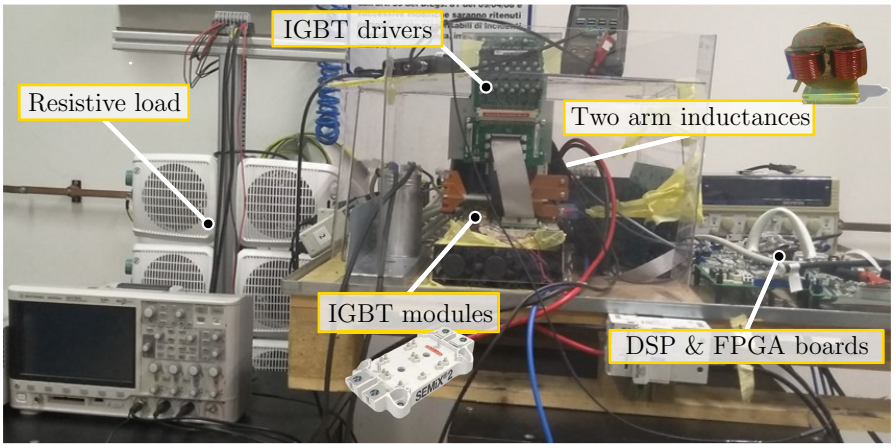


FIGURE 4.10: A picture of the single-phase prototype.

Input voltage (V_{dc})	600 V
Output phase voltage (V_{φ})	150_{rms} V
Line frequency (f_1)	50 Hz
Switching frequency (f_s)	10 kHz
Arm inductance (L)	240 μH
Middle SM capacitance (C_m)	300 μF
Output filter capacitance (C_f)	325 μF

TABLE 4.5: Specifications of The Single-phase MMC Experimental System

for implementing the controllers and generating the references and the switching signals for the three SMs, while an FPGA board is used to generate the switching signals for every single IGBT with an appropriate dead-time. The output voltage

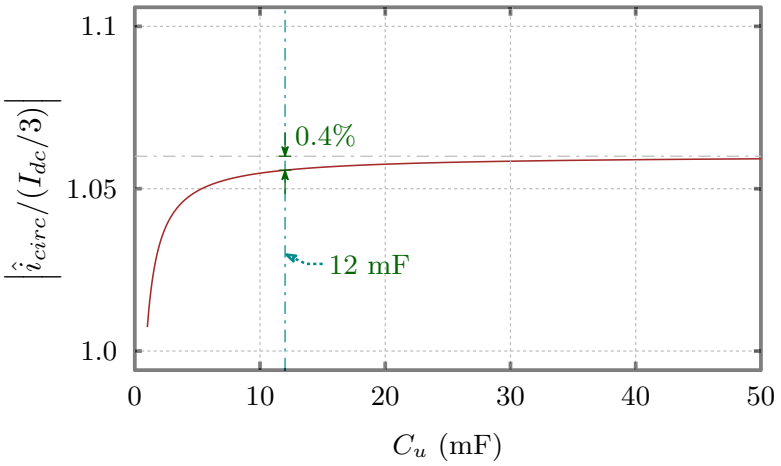


FIGURE 4.11: The relationship between the dc-side capacitance and the relative amplitude of the second-order component of the circulating current.

and the arm currents are measured, sampled and sent to the DSP board for control and protection purposes.

The three modes of operation, discussed using simulation in Sec. 4.2, are experimentally validated. The adopted output voltage control is reported in Fig. 4.6(b). Unlike the simulation results, the voltage of the upper and the lower SMs are fixed as they are directly supplied from the dc supply; therefore, their voltage ripples are negligible. The dc-side capacitance, for DC/AC converters, is mostly designed to have a large capacitance; therefore, the most critical design factor for this topology is the middle capacitor.

Two test cases are considered; 1) unity load factor where a $25\,\Omega$ resistor is utilized; 2) 0.79 lagging PF where a $25\,\Omega$ in parallel with a $100\,\mu$F capacitor are used. Fig. 4.12(a) shows the experimental results in the case of disabled circulating current control. The voltage ripple of the middle capacitors is close to what is expected from the simulation. Fig. 4.12(b) shows the experimental results with the controlled constant circulating current. The experimental results with injecting controlled second-order harmonics in the circulating current are reported in Fig. 4.12(c). The voltage ripple of the middle capacitor, the peak and rms value of the arm current and, consequently, the converter efficiency are affected by the circulating current control. Fig. 4.12(d), Fig. 4.12(e), and Fig. 4.12(f) show the experimental results with open-loop , constant, and second-order injection of circulating current, respectively, at 0.79 load power factor.

The peak-to-peak voltage ripple of the middle capacitor, calculated from (4.13), is around 43.6 V and 55.4 with the unity and 0.79 lagging PF, respectively, which are close to the values 47.25 V and 57.6 V obtained in Fig. 4.12(b) and Fig. 4.12(e).

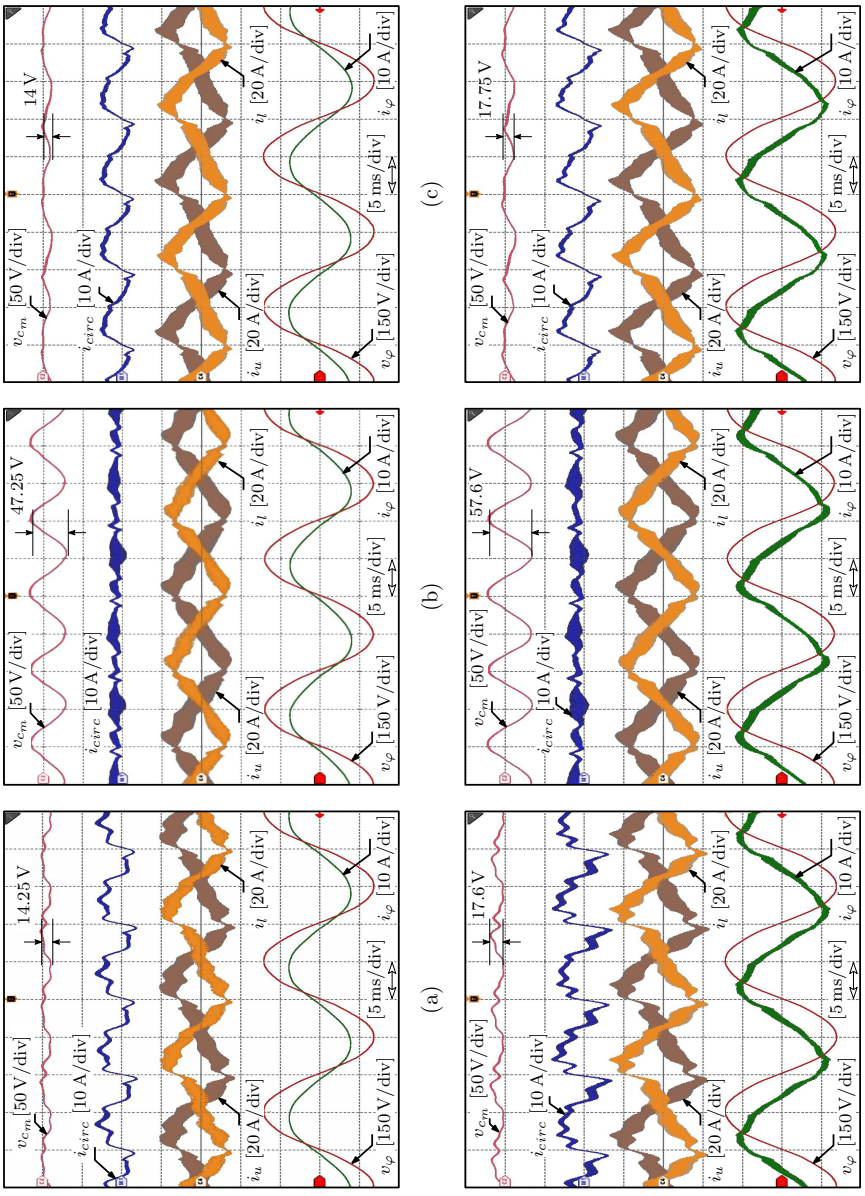


FIGURE 4.12: Experimental results: unity PF with (a) a disabled circulating current control; (b) constant circulating current; (c) a second-order circulating current injection; 0.79 lagging power factor with (d) a disabled circulating current control; (e) constant circulating current; (f) a second-order circulating current injection.

4.4 Summary

This chapter has introduced a modified MMC topology for low-voltage applications. The MMC topology is known to be an efficient one for HV applications and some Medium-Voltage (MV) ones. However, the main issue is the large capacitance requirement. Therefore, this chapter aims to reduce the capacitance requirement while keeping the benefits of the MMC structure. The effectiveness of the proposed topology and the provided analysis and design procedure are confirmed by simulation and experimental results. It is proved that the capacitance requirement of the proposed topology is significantly smaller. Instead of twelve capacitors as in the conventional MMC or nine capacitors as in a modified MMC topology, only three capacitors are needed, if it is assumed that the two bulky dc-link capacitors are already present in $3\Phi - 4W$ system. Moreover, the middle capacitance is reduced in the proposed topology respect to the modified one (about half in the case of circulating current injection). Furthermore, the operation can be optimized between the two extreme points, that is, the minimum capacitance and the maximum efficiency by proper injection of second-order harmonics in the circulating current.

In the case of injecting a second-order harmonic in the circulating current, excluding the two dc-link capacitors, only 3 capacitors of $34\,\mu F$ are needed instead of the 12 capacitors of $2260\,\mu F$ required in the conventional MMC. Accordingly, the total stored energy is reduced up to 99.5% with respect to the conventional MMC and 90% concerning the modified one.

Chapter 5

Circulating Current Control for a Three-phase Modified Modular Multilevel Converter (MMC) with a Reduced Number of Current Sensors

In this chapter, a capacitor voltage control scheme for a three-phase MMC with optimized capacitor sizing is implemented. Unlike the existing circulating current control, the proposed controller uses the middle capacitor voltage to control the second-order harmonic component of the circulating current. Therefore, it is not necessary to measure the two arm currents; only one voltage sensor is required. The proposed control can effectively control the circulating current to be constant or inject second-order harmonics to optimize the capacitor sizing. The detailed analysis, controller design and performance of the proposed scheme are presented in this chapter. The effectiveness of this study is confirmed by simulation and experimental results.

5.1 Principle of Operation of the Modified MMC Converter

5.1.1 The modified MMC Structure

Fig. 5.1 shows the three-phase three-level modified MMC reported in Chapter 4. To reduce the capacitance requirement of a $3\Phi - 4W$ system, instead of supplying each SM from a separate capacitor, the three upper SMs are supplied from the same capacitor, that is, the upper dc-link capacitor (C_u). Similarly, the three-lower SMs are supplied from the lower dc-link capacitor (C_l). In this way, a significant reduction of the converter size and the number of components is achieved due to integrating the two bulky dc-link capacitors into the structure.

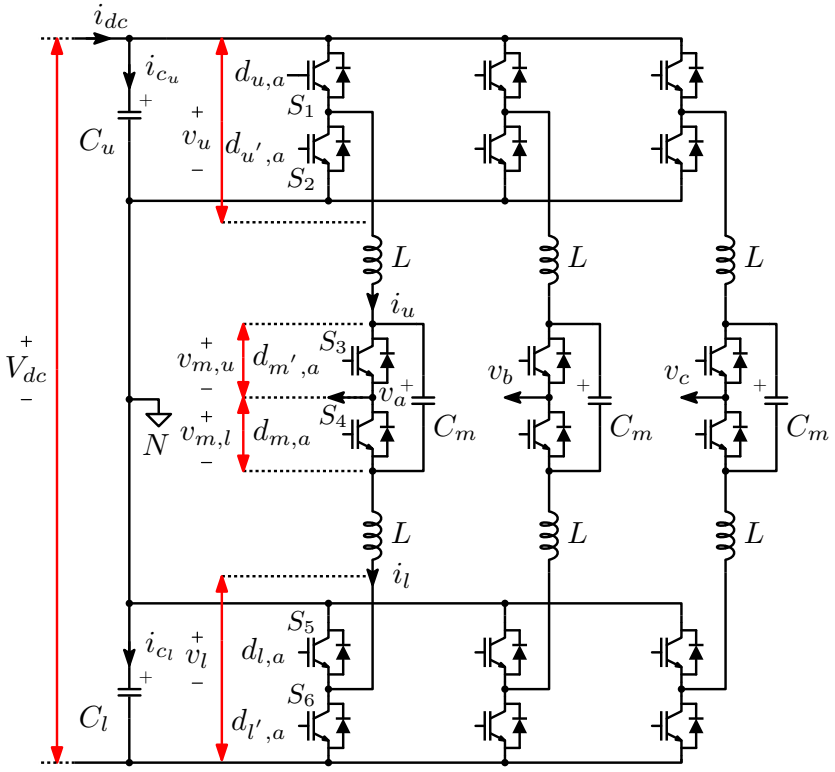


FIGURE 5.1: The three-phase three-level Modular Multilevel Converter (MMC) with optimized capacitor sizing.

From (4.9) and (4.13), the middle capacitors voltage (v_{C_m}) are expressed as

$$\begin{aligned} v_{C_m,a} &= V_{dc}/2 + \hat{V}_{C_m,2\omega}\, sin(2\omega t - \varphi), \\ v_{C_m,b} &= V_{dc}/2 + \hat{V}_{C_m,2\omega}\, sin(2\omega t + 2\pi/3 - \varphi), \\ v_{C_m,c} &= V_{dc}/2 + \hat{V}_{C_m,2\omega}\, sin(2\omega t - 2\pi/3 - \varphi), \end{aligned} \tag{5.1}$$

where

$$\hat{V}_{C_m,2\omega} = \frac{1}{2\omega C_m}\left(\hat{I}_{circ,2\omega} - \frac{\hat{V}_a \hat{I}_a}{2V_{dc}}\right). \tag{5.2}$$

Therefore, the peak-to-peak voltage ripple of the middle capacitors (ΔV_{C_m}) can be expressed as

$$\Delta V_{C_m} = \frac{1}{\omega C_m}\left|\hat{I}_{circ,2\omega} - \frac{\hat{V}_a \hat{I}_a}{2V_{dc}}\right|, \tag{5.3}$$

where $|.|$ denotes absolute value.

On the one hand, according to (5.3), a lower capacitor voltage ripple (lower capacitance) for the middle SM can be obtained by injecting a second-order component ($\hat{I}_{circ,2\omega}$) in the circulating current. On the other hand, suppressing $\hat{I}_{circ,2\omega}$ increases the middle SM capacitance requirement and decreases the rms value of the arm current. An optimum point between the two extreme values can be achieved by proper control of $\hat{I}_{circ,2\omega}$.

5.2 Modulation and Small Signal Analysis

As shown in Fig. 5.1, the three-phase MMC structure is symmetric; therefore, one phase is analyzed in the following subsections. The power switches, inductors, and capacitors are assumed ideal.

Assuming a negligible voltage ripple on the dc-side capacitors (C_u and C_l), the voltages v_u, v_{m_u}, v_{m_l}, and v_l across the the switches S_1, S_3, S_4, and S_6, respectively, can be expressed as

$$\begin{aligned} \bar{v}_u = \bar{d}_u\, V_{dc}/2,\ \bar{v}_l = \bar{d}_l\, V_{dc}/2 \\ \bar{v}_{m,u} = \bar{d_m}\, v_{C_m},\ \bar{v}_{m,l} = (1-\bar{d}_m)\, \bar{v}_{C_m} \end{aligned} \tag{5.4}$$

where the bar indicates averaging over the switching period.

The DM voltage (v_{DM}) and the CM voltage (v_{CM}) can be defined as

$$\begin{aligned} v_{\mathrm{DM}} &= \frac{(v_l + v_{m,l}) - (v_u + v_{m,u})}{2} \\ v_{\mathrm{CM}} &= \frac{(v_l + v_{m,l}) + (v_u + v_{m,u})}{2} \end{aligned} \tag{5.5}$$

In order to control the DM voltage (v_{DM}), that is generating the phase voltage, the DM modulation reference (m_{DM}) can be defined as

$$m_{\mathrm{DM},a} = \frac{v_a^*}{V_{dc}/2} = \hat{M}_{\mathrm{DM},a}\, cos(\omega t) \tag{5.6}$$

where v_a^* and $\hat{M}_{\mathrm{DM},a}$ are the reference voltage of v_a and the amplitude of $m_{\mathrm{DM},a}$, respectively.

In order to control the CM voltage (v_{CM}), that is controlling the circulating current, the CM modulation reference (m_{CM}) can be defined as

$$m_{\mathrm{CM},a} = \frac{v_{\mathrm{CM,a}}^*}{V_{dc}/2} = \hat{M}_{\mathrm{CM},a}\, cos(2\omega t) \tag{5.7}$$

where $v_{\mathrm{CM,\,a}}^*$ and $\hat{M}_{\mathrm{CM},a}$ are the reference voltage of $v_{\mathrm{CM,\,a}}$ and the amplitude of $m_{\mathrm{CM},a}$, respectively.

5.2.1 Modulation

The differential voltage is generated by modulating the upper and lower SMs with a π-phase-shifted modulation reference with respect to the modulation reference of the middle SM; while the common-mode modulation reference is applied only to the upper and lower SMs.

The modulation technique utilized to drive the three SMs of each leg is shown in Fig. 5.2. Assuming that a triangular carrier oscillating between 0 and 1 is utilized, the duty cycles of the upper (d_u), middle (d_m) and lower (d_l) SMs can be expressed as a function of the modulation references as follows:

$$\begin{aligned} d_u &= 0.5 + 0.5(\,+m_{\mathrm{DM}} + \,m_{\mathrm{CM}}),\\ d_l &= 0.5 + 0.5(\,+m_{\mathrm{DM}} - \,m_{\mathrm{CM}}).\\ d_m &= 0.5 + 0.5(\,-m_{\mathrm{DM}}), \end{aligned} \tag{5.8}$$

where the circulating current is assumed to flow downward.

Fig. 5.2(a) shows the waveforms when $\hat{M}_{\mathrm{CM}}$ is zero. In this case, the duty cycles of the upper (d_u) and lower (d_l) SMs are equal. If the common-mode voltage reference is not equal to zero ($\hat{M}_{\mathrm{CM}} \neq 0$), d_u and d_l become different as shown in Fig. 5.2(b).

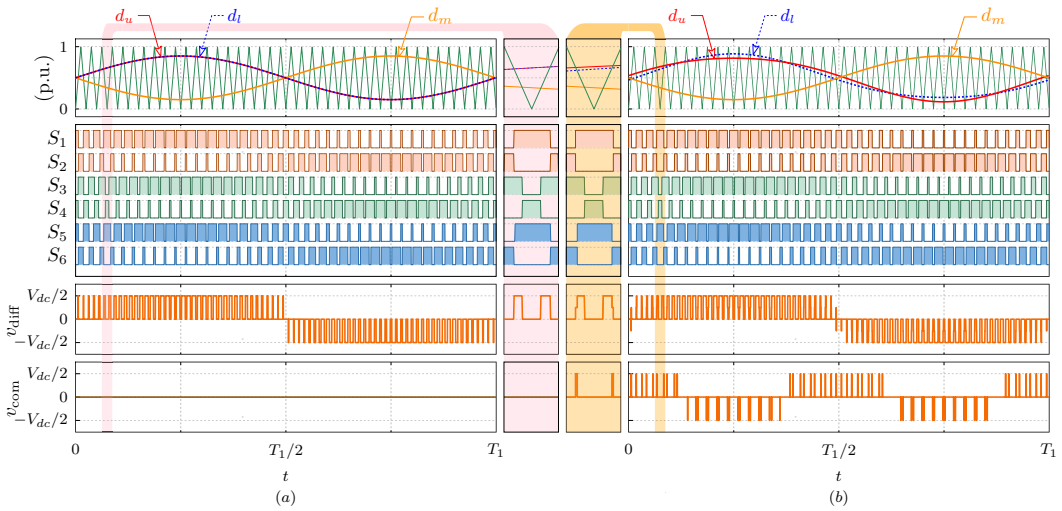


FIGURE 5.2: Modulation technique for the modified Modular Multilevel Converter (MMC) topology. Reference, carriers, gate signals for switches S_1 to S_6, and the resultant DM (v_{diff}) and CM (v_{com}) voltage; where $v_{\text{diff}} = v_l - v_u$, v_a^* is the differential phase voltage reference, while v_{com}^* is the CM voltage reference.

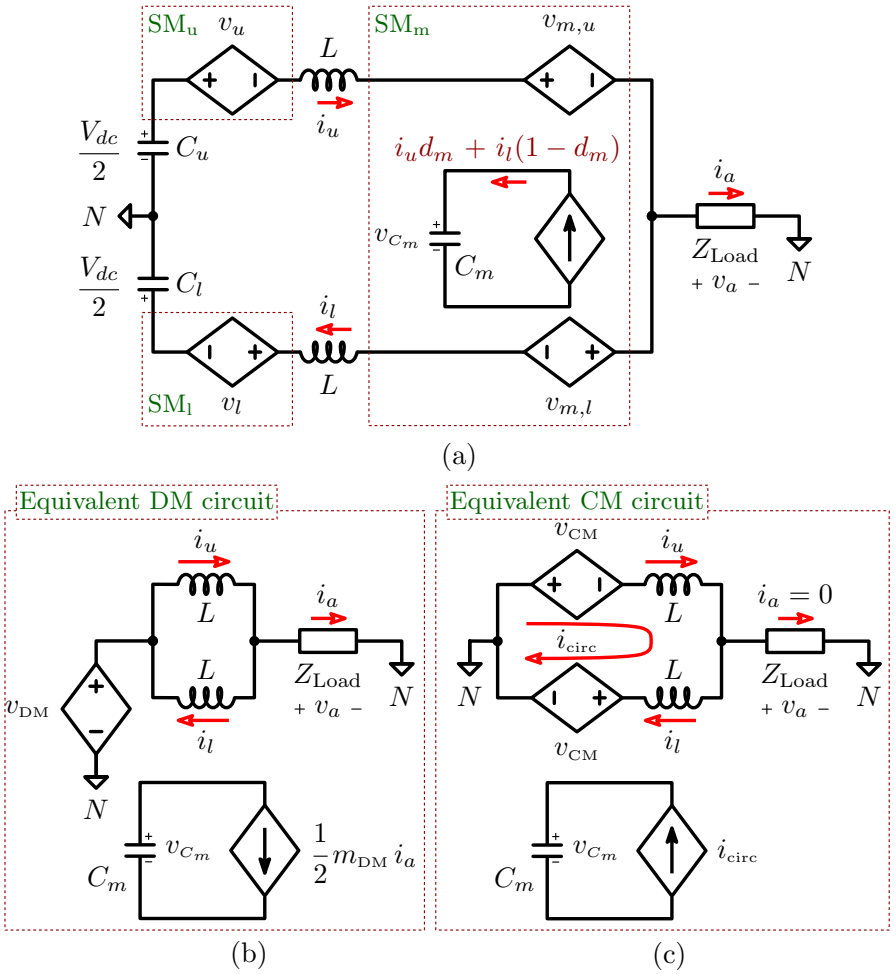


FIGURE 5.3: (a) Average model of the modified Modular Multilevel Converter (MMC) topology; (b) equivalent DM circuit; (c) equivalent CM circuit.

5.2.2 Averaged Model of the Modified MMC

Fig. 5.3(a) shows an average model of phase a of the modified MMC. The averaged model of the MMC can be separated into a DM and CM averaged circuits [43] as shown in Fig. 5.3(b) and Fig. 5.3(c), respectively.

The DM (v_{DM}) and CM (v_{CM}) voltages can be redefined as a function of the DM (m_{DM}) and CM (m_{CM}) modulation references as follows:

$$\begin{aligned} v_{\text{DM}} &= \frac{1}{2} m_{\text{DM}} \frac{V_{dc}}{2} + \frac{1}{2} m_{\text{DM}} v_{C_m} \\ v_{\text{CM}} &= \frac{1}{2}(1 - m_{\text{CM}}) \frac{V_{dc}}{2} + \frac{1}{2} v_{C_m} \end{aligned} \tag{5.9}$$

From Fig. 5.3(a), the middle capacitor current can be expressed as

$$i_{C_m} = i_u d_m + i_l(1 - d_m) = i_{\text{circ}} - \frac{1}{2} m_{\text{DM}}\, i_a \tag{5.10}$$

By applying kirchhoff voltage and current laws in the circuit shown in Fig. 5.3(c) and substituting for v_{CM} using (5.9), the following relationships are obtained:

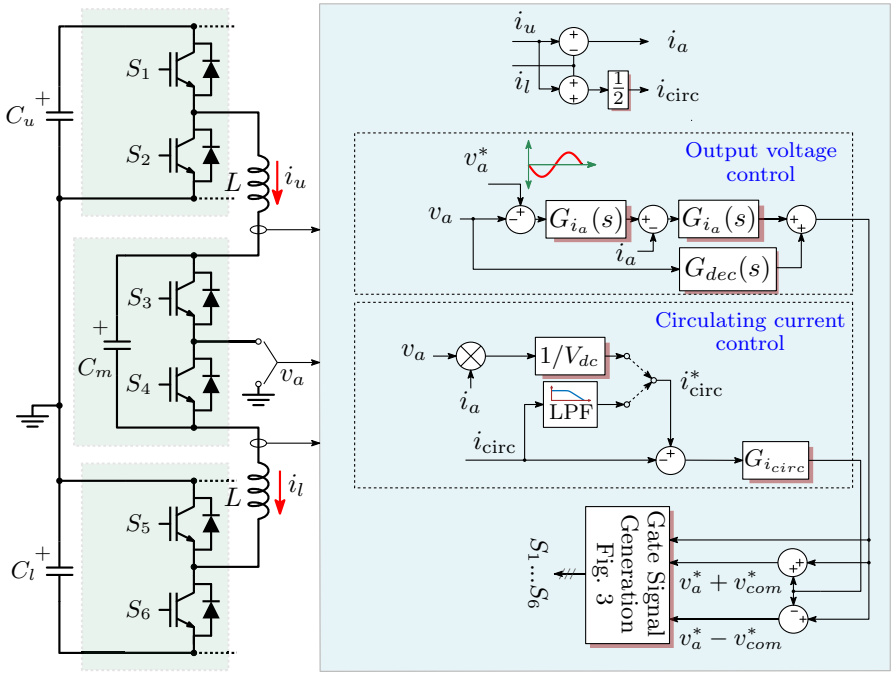
$$\begin{aligned} L\frac{di_{circ}}{dt} &= -\frac{1}{2}(1 - m_{\text{CM}}) \frac{V_{dc}}{2} - \frac{1}{2} v_{C_m} \\ C_m \frac{dv_{C_m}}{dt} &= i_{circ} \end{aligned} \tag{5.11}$$

The stability properties of the circulating current and the middle capacitor voltage can be assessed by perturbing (5.11) around a steady-state operation trajectory as follows:

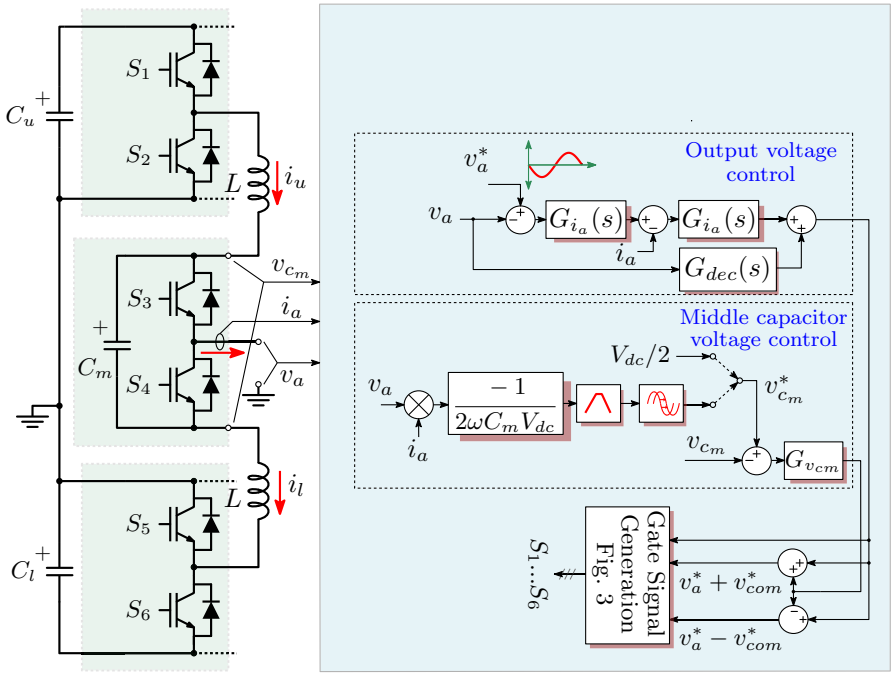
$$L\frac{d\tilde{i}_{circ}}{dt} = -\frac{1}{2}\tilde{v}_{C_m} - \frac{1}{2}\tilde{m}_{\text{CM}} \frac{V_{dc}}{2},\; C_m \frac{d\tilde{v}_{C_m}}{dt} = \tilde{i}_{circ} \tag{5.12}$$

Applying Laplace in (5.11), the following transfer functions can be obtained:

$$\begin{bmatrix} \tilde{i}_{circ}(s) \\ \tilde{v}_{C_m}(s) \end{bmatrix} = \frac{V_{dc}/2}{1 + 2LC_m s^2} \begin{bmatrix} sC_m \\ 1 \end{bmatrix} \tilde{m}_{\text{CM}}(s) \tag{5.13}$$



(A)



(B)

FIGURE 5.4: Closed-loop control diagram for the modified Modular Multilevel Converter (MMC). (a) A control scheme with the existing circulating current controller; (b) a control scheme with the proposed middle capacitor voltage controller.

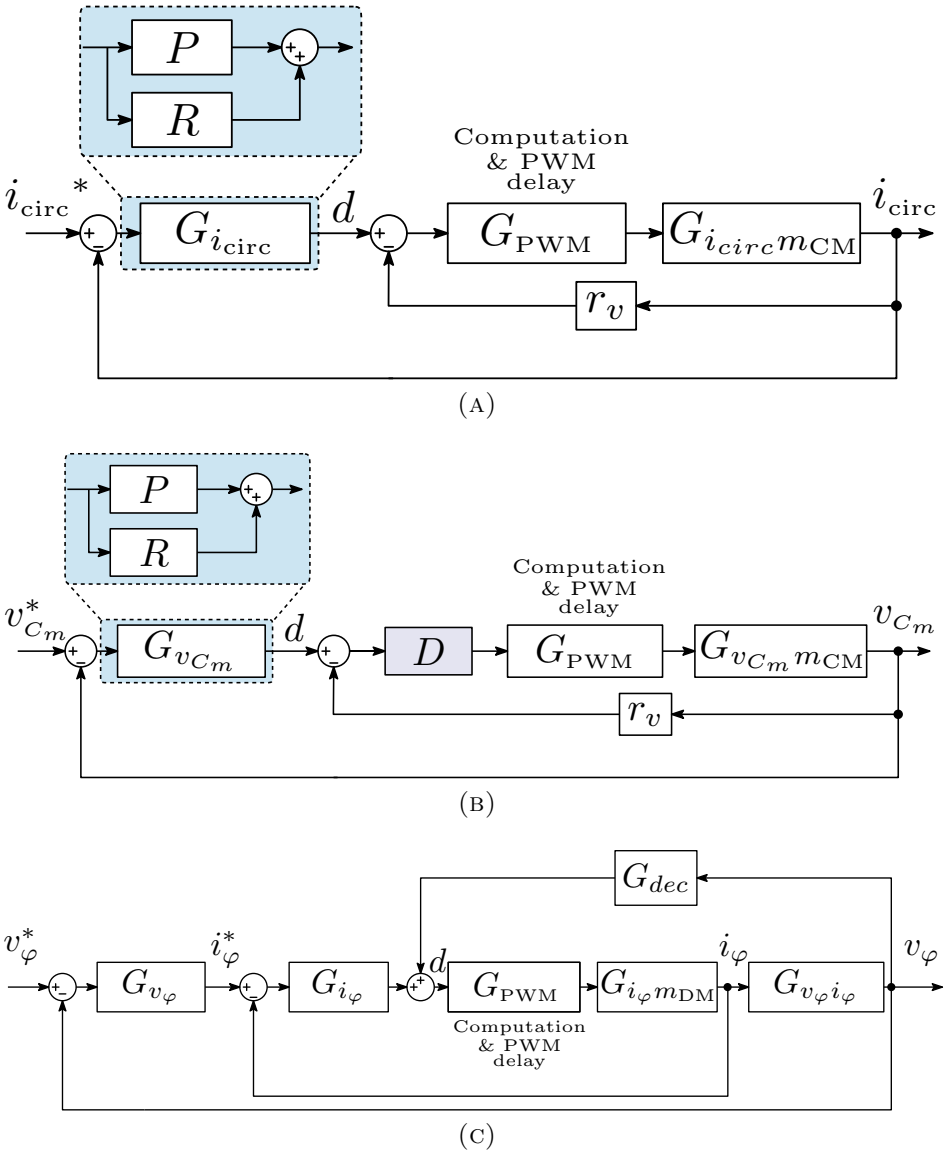


FIGURE 5.5: (a) a block diagram for the linearized model of the circulating current loop; (b) a block diagram for the linearized model of the middle capacitor voltage loop; (c) a block diagram for the linearized model of the output voltage loop.

5.2.3 Control Design

The existing and the proposed control schemes are depicted in Fig. 5.4(a) and Fig. 5.4(b), respectively. In both cases, the output voltage is regulated by a multi-loop voltage controller, where an inner current loop is adopted to simplify the design, actively damping the output filter resonance [40], and providing over-current protection during abnormal conditions [37]. The equivalent small-signal transfer function of the computation delay and PWM modulator, considering a

double sampling digital control, can be approximated by [37]

$$\begin{aligned} G_{\text{PWM}}(s) &= \overbrace{e^{-s\frac{T_s}{2}}}^{\text{computation delay}} \cdot \overbrace{e^{-s\frac{T_s}{4}}}^{\text{PWM delay}} = e^{-s\frac{3T_s}{4}} \\ &\cong \frac{1-(3T_s/8)s}{1+(3T_s/8)s}. \end{aligned} \tag{5.14}$$

5.2.3.1 Output voltage control

Voltage-source inverters are usually equipped with an LC filter. In MMC topologies, the equivalent value of the two arm inductors, which is half of the arm inductance, constitutes with the ac-side capacitor (C_f) an LC filter for the output. Fig. 5.5(c) shows a block diagram for the closed-loop system. The ac-side voltages (v_a , v_b, v_c) are controlled to follow a given sinusoidal voltage references (v_a^* , v_b^*, v_c^*).

A PI regulator ($G_{i_a}(s)$) is adopted for the inner current loop with a state feedback voltage decoupling [44]. In the existing circulating current control, the feedback of the inner current loop is calculated from the difference between the upper (i_u) and the lower (i_l) arm currents, while the phase current is used in the proposed controller. In a stationary reference frame, a PI regulator ($G_{v_a}(s)$) is adopted to obtain a large bandwidth voltage controller [37].

The open-loop transfer function of the inner current loop is expressed by

$$\text{T}_{\text{OL},i_a}(s) = G_{i_a}(s)G_{\text{PWM}}(s)\overbrace{G_{i_a m_{\text{DM}}}(s)}^{\tilde{i}_a(s)/\tilde{m}_{\text{DM}}(s)} \tag{5.15}$$

where $G_{i_a m_{\text{DM}}}(s)$ is the transfer function from m_{DM} to i_a, respectively.

The open-loop transfer function of the output voltage loop is expressed by

$$\text{T}_{\text{OL},v_a}(s) = G_{v_a}(s)\text{T}_{\text{CL},i_a}(s)Z_f(s), \tag{5.16}$$

where $\text{T}_{\text{CL},i_a}(s)$, and $Z_f(s)$ are the closed-loop transfer function of the inner current loop, and the impedance of the output filter capacitor (C_f), respectively.

5.2.3.2 Circulating current control

As the PI regulator does not provide enough gain at the double line frequency, a PR regulator in the SRF is adopted. The transfer function of the circulating

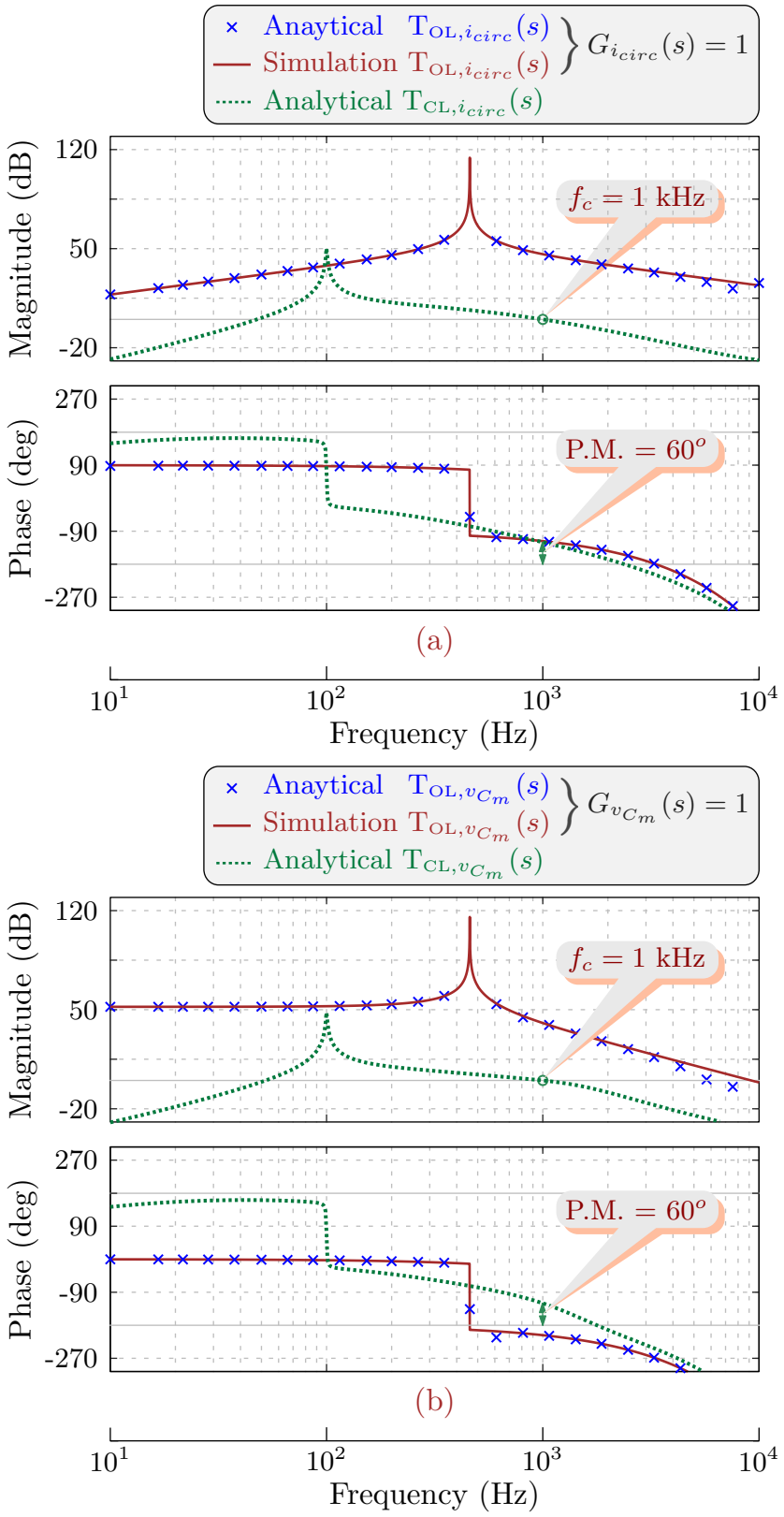


FIGURE 5.6: Bode diagram of (a) the open-loop and closed-loop circulating current control; (b) the open-loop and closed-loop middle capacitor voltage control.

current PR regulator is expressed by

$$G_{i,circ}(s) = P(s) + R(s), \tag{5.17}$$

where

$$\begin{cases} P(s) & = k_{p,i_{circ}}, \\ R(s) & = k_{r,i_{circ}} \dfrac{s}{s^2 + 2\omega_c s + (2\omega_1)^2}, \end{cases} \tag{5.18}$$

where $k_{r,i_{circ}}$, $k_{r,i_{circ}}$ and ω_c are the proportional gain, the resonant gain, and the cut-off frequency respectively. The control parameters are designed according to the linearized model shown in Fig. 5.5(a).

The open-loop transfer function of the circulating current loop is expressed by

$$\mathrm{T}_{\mathrm{OL},i_{circ}}(s) = G_{i_{circ}}(s) G_{\mathrm{PWM}}(s) \overbrace{G_{i_{circ} m_{\mathrm{CM}}}(s)}^{\tilde{i}_{circ}(s)/\tilde{m}_{\mathrm{CM}}(s)} \tag{5.19}$$

where $G_{i_{circ} m_{\mathrm{CM}}}(s)$ is the transfer function from m_{CM} to i_{circ}.

5.2.3.3 Middle capacitor voltage control

Similar to the circulating current control, a PR regulator ($G_{v_{cm}}(s)$) in the SRF is adopted. The control parameters are designed according to the linearized model shown in Fig. 5.5(b).

A low-pass filtered derivative controller ($D(s)$) is used in the middle capacitor voltage control to compensate for the phase lag induced by the capacitor voltage. The derivative term is expressed as

$$D(s) = k_{d,v_{cm}} \frac{s}{s + \omega_z}, \tag{5.20}$$

where $k_{d,v_{cm}}$ and ω_z are the derivative gain and the cut-off frequency of the low-pass filter.

The open-loop transfer function of the middle capacitor voltage loop is expressed by

$$\mathrm{T}_{\mathrm{OL},v_{cm}}(s) = G_{v_{cm}}(s) D(s) G_{\mathrm{PWM}}(s) \overbrace{G_{v_{C_m} m_{\mathrm{CM}}}(s)}^{\tilde{v}_{C_m}(s)/\tilde{m}_{\mathrm{CM}}(s)} \tag{5.21}$$

where $G_{v_{C_m} m_{\mathrm{CM}}}(s)$ is the transfer function from m_{CM} to v_{C_m}.

An ac sweep analysis using PLECS is performed to verify the obtained transfer functions. Fig. 5.6(a) shows Bode diagrams for the analytical results and those obtained by PLECS simulation for the circulating current control. Similar diagrams are shown in Fig. 5.6(b) for the proposed voltage control. It can be observed that the analytical results agree well with the simulation results.

The reference signal for the circulating current is generated from the single-phase apparent power as follows [45]:

$$\begin{aligned} {i_{\text{circ}}}^* &= \frac{S_{ph}}{V_{dc}} = \frac{v_a i_a}{V_{dc}} \\ &= \frac{\hat{V}_a \hat{I}_a}{2V_{dc}}\, cos(\varphi) + \frac{\hat{V}_a \hat{I}_a}{2V_{dc}}\, cos(2\omega t - \varphi). \end{aligned} \tag{5.22}$$

Similarly, the reference signal for the middle capacitor voltage is generated from the single-phase apparent power, as shown in Fig. 5.4(b), by dividing S_{ph} by V_{dc} and multiplying by the middle capacitor impedance. Then, a band-pass filter and an orthogonal signal generator are adopted to generate (5.1).

5.3 Simulation Results

A 230 V_{rms} 30 kVA simulation model with the parameters listed in Table 5.1 has been developed to verify the performance of the proposed controller. As shown in Fig. 5.7, two cases are considered for the circulating current control: a) constant circulating current, and b) circulating current injection. Similarly, two cases are considered for the middle capacitor voltage control: a) constant middle capacitor voltage, and b) middle capacitor voltage injection, as discussed in the following subsections.

5.3.1 Constant Circulating Current

The circulating current can be controlled to be constant either by a circulating current control with a constant reference signal (two current sensors case), shown in Fig. 5.7(a) or by injecting a proper amount of second-order harmonic in the middle capacitor voltage (one current sensor case), shown in Fig. 5.7(b). This operation mode leads to less rms and peak arm current while high middle capacitance requirement (maximum ripple). The peak-to-peak value of the middle capacitor

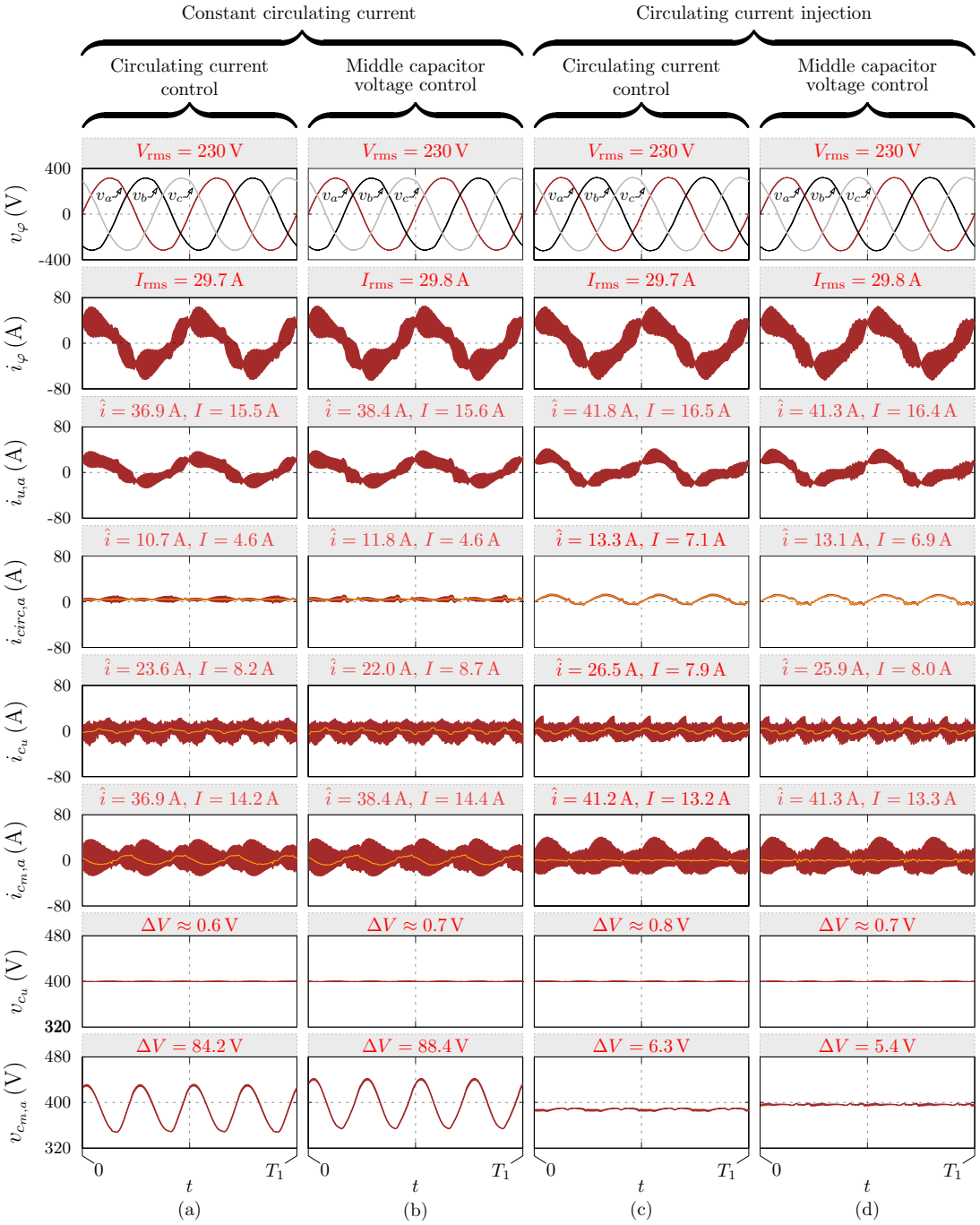


FIGURE 5.7: Simulation results for the proposed topology. Note that ΔV, I, $\hat{I}$ are the peak-to-peak voltage ripple, the rms current, and the peak current, respectively. T_1 is the fundamental period of the output voltage. The orange waveforms are the low-frequency components.

	Parameter	Symbol	Value
Specifications	Rated power	S	10 kVA
	Input voltage	V_{dc}	800 V
	Output line-to-line voltage	V_{L-L}	400_{rms} V
	Line frequency	f_1	50 Hz
	Switching frequency	f_s	10 kHz
Parameters	Arm inductance	L	200 μH
	Upper SM capacitance	C_u	12 mF
	Lower SM capacitance	C_l	12 mF
	Middle SM capacitance	C_m	300 μF
	Output filter capacitance	C_f	325 μF

TABLE 5.1: Specifications of The Simulated Three-Phase Modular Multilevel Converter (MMC) Converter

voltage can be calculated analytically using the relationship (5.3), as

$$\begin{aligned}\Delta V_{c_m} &= \frac{\hat{V}_a \hat{I}_a}{2\omega C_m V_{dc}} \\ &= \frac{230\sqrt{2}\,\mathrm{V} \times 29.7\sqrt{2}\,\mathrm{A}}{2 \times 2\pi \times 50\,\mathrm{Hz} \times 300.10^{-6}\,\mathrm{F} \times 800\,\mathrm{V}} \\ &\cong 90\,V\end{aligned} \tag{5.23}$$

It can be noted from the simulation results that, ΔV_{C_m} is around 84.2 V in the case of circulating current control, Fig. 5.7(a), with an error of around -6.4% from the analytical value. In the case of middle voltage control, ΔV_{C_m} is around 88.4 V, Fig. 5.7(b), with an error of around -1.8%

5.3.2 Constant Middle Capacitor Voltage

Constant middle capacitor voltage can be achieved using a current control of the circulating current with injecting a proper amount of second-order component, as shown in Fig. 5.7(c). As discussed earlier, this technique requires two current sensors for the upper and lower arm current. Alternatively, a voltage control for the middle capacitor can achieve this operation mode with a constant reference using one voltage sensor for the middle capacitor. Fig. 5.7(d) shows the simulation results for this mode of operation. The voltage ripple of the middle capacitor is reduced from 6.3 V to 5.4 V also with a reduced deviation for the average voltage from the nominal value 400 V.

5.3.3 Transition Between Circulating Current Injection and Constant Circulating Current

Fig. 5.8 shows the transition between the two operation modes of the converter: a) Circulating current injection (constant middle capacitor voltage), and b) constant circulating current (middle capacitor voltage injection). Fig. 5.8(a) and Fig. 5.8(b) show the transition with the circulating current control and with the middle capacitor voltage control, respectively. It can be noted that the transition between the two operation modes is smooth. Moreover, the voltage waveform shows better dynamics with the middle capacitor voltage control due to the direct control of the voltage.

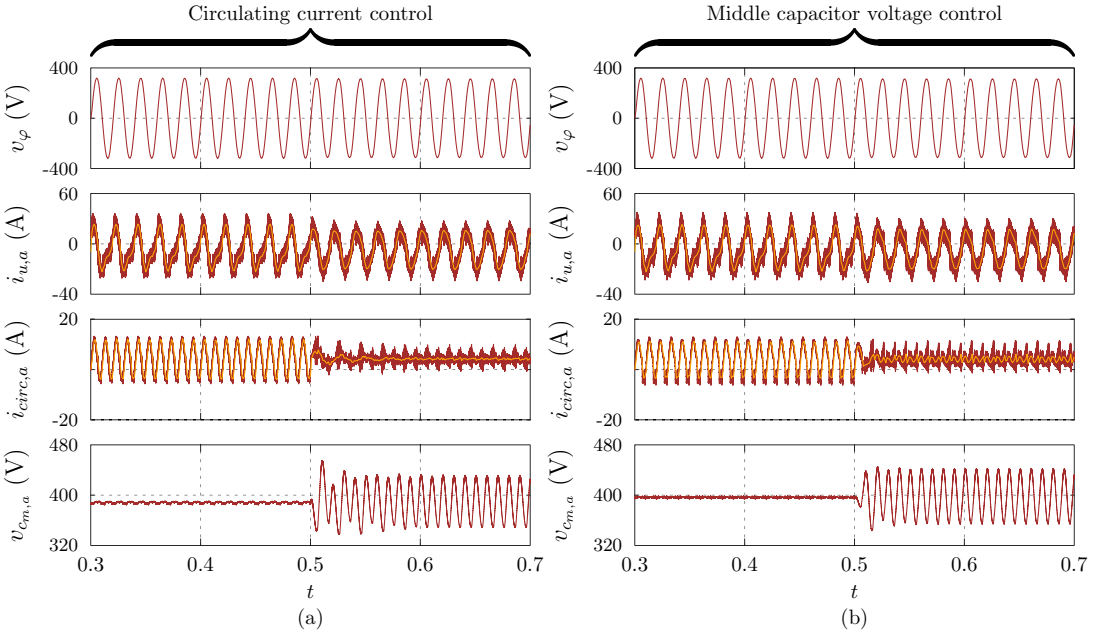


FIGURE 5.8: Simulation results with a transition between circulating current injection and constant circulating current using (a) circulating current control; (b) middle capacitor voltage control; The transition is activated at $t = 0.5\,s$

5.4 Experimental Validation

A LV single-phase prototype of the proposed MMC converter has been developed to experimentally validate the analytical analysis and simulations. The experimental setup is shown in Fig. 5.9. The inverter is supplied with a dc voltage of 200 V, and an output resistive load is considered. The parameters are listed in Table 5.2. As shown in Fig. 5.4, the phase includes three half-bridge SMs. Each SM consists of a SEMIKRON SSEMiX402GB066HDs IGBT Module rated at 600 V

400 A, and a capacitor. Two voltage sources, 100 V each, are used to supply the upper and the lower SMs, while a 300 μF is utilized to supply the middle one.

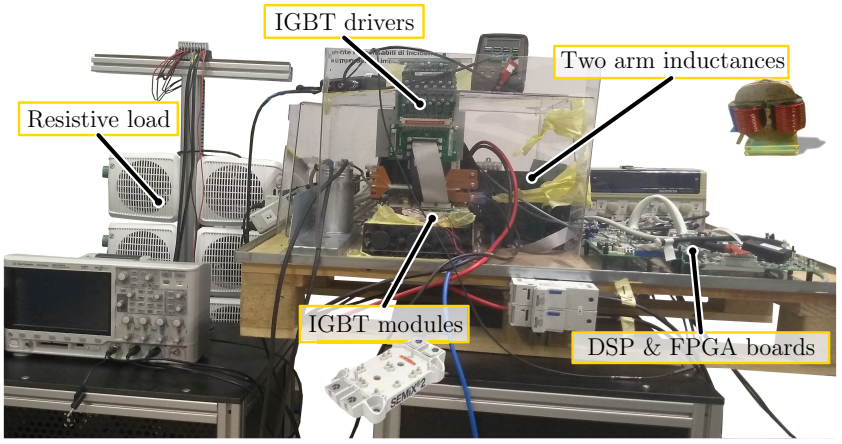


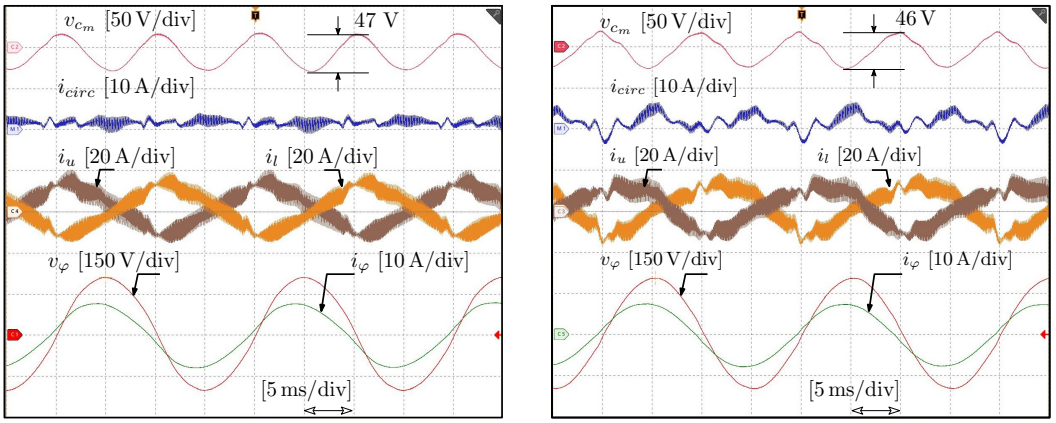
FIGURE 5.9: A picture of the single-phase prototype.

Parameter	**Symbol**	**Value**
Input voltage	V_{dc}	600 V
Output phase voltage	V_a	150_{rms} V
Line frequency	f_1	50 Hz
Switching frequency	f_s	10 kHz
Arm inductance	L	200 μH
Middle SM capacitance	C_m	300 μF
Output filter capacitance	C_f	325 μF

TABLE 5.2: Specifications of The Single-phase MMC Experimental System

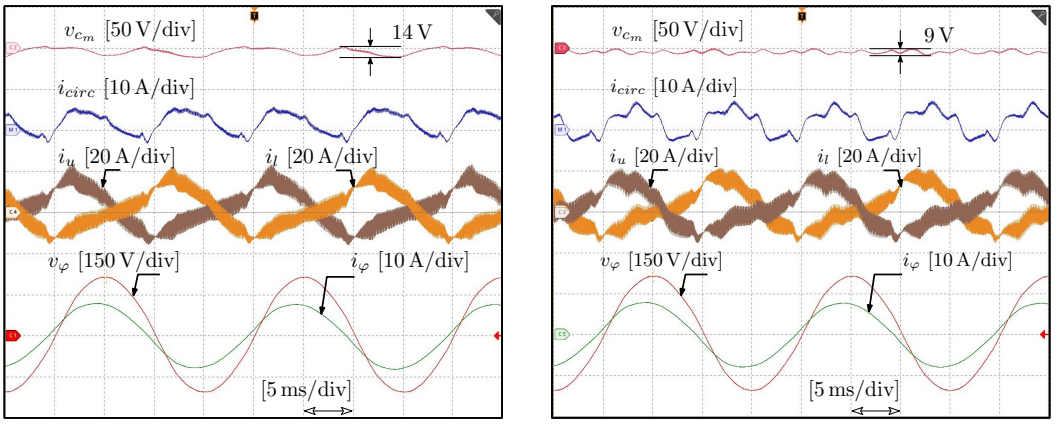
The two modes of operation for the existing and proposed controllers, discussed using simulation in Sec. 5.3, are experimentally validated. The adopted output voltage control is reported in Fig. 5.5c. The dc-side capacitance for DC/AC converters is mostly designed to have a large capacitance; therefore, this topology's most critical design factor is the middle capacitor.

Fig. 5.10 shows the experimental results with a constant circulating current. In Fig. 5.10(a) a circulating current regulator is used, while in Fig. 5.10(b) a middle capacitor voltage regulator is used. The experimental results of the circulating current injection mode are shown in Fig. 5.11(a), while Fig. 5.11(b) shows the results when a middle capacitor voltage regulator is used. It can be seen that the two modes can be achieved using a single voltage sensor instead of two current sensors, saving three current sensors in the three phases. In addition, the peak-to-peak ripple of the middle capacitor is lower with capacitor voltage regulation.



(A) (B)

FIGURE 5.10: Experimental results. Constant circulating current using: a) Circulating current control; b) middle capacitor voltage control.



(A) (B)

FIGURE 5.11: Experimental results. Circulating current injection using: a) Circulating current control; b) middle capacitor voltage control.

5.5 Summary

In this chapter, a voltage regulator for the middle capacitor of a modified MMC topology is presented, with a detailed analysis of the MMC. It is demonstrated that the various modes of operation of the MMC topology, including constant circulating current and circulating current injection, can be achieved by voltage regulating the middle capacitor instead of the existing circulating current regulation. In this way, the three-phase MMC structure requires three current sensors (one per phase) instead of six current sensors. Finally, the effectiveness of the proposed voltage regulator is verified and demonstrated by simulating a three-phase MMC converter and experimental results on a single-phase MMC prototype.

Chapter 6

Three-phase Three-level Arm-Inductor-less Modular Multilevel Converter (MMC)

A three-level inductor-less MMC topology is proposed in this chapter as an alternative to ANPC topology for LV applications. The proposed topology is derived from the three-level MMC with the upper and lower SMs are connected to a common capacitor. The switching transitions and operation modes of the topology are analyzed. Different modulation techniques and the related switching characteristics are investigated. The phase voltage and current, switching loss, capacitor voltage ripple and rms current are compared by simulation results. Experimental results are presented to confirm the theoretical analysis and simulation results.

6.1 Introduction

ANPC topology has been introduced as an alternative to the NPC since the distribution of semiconductor junction temperature is more uniform [46]. Stray inductance within the same power module is relatively low. However, the stray inductance of the busbars that are commonly used to connect the power modules in high power converters is a major concern in the design of ANPC converters [47–50]. Voltage overshoots across the switches may occur due to the stray inductance of long commutation loops and can lead to damage of the power devices, increased EMI, and limit the semiconductors switching frequency and the converter power [48].

Different modulation techniques and switching modes for the ANPC are analyzed in [51]. In [52], a modified modulation scheme is proposed for a three-level ANPC in order to reduce the switching stress of some devices and distribute the loss more evenly. An analytical model has been developed in [50] for the switch over-voltage of ANPC considering the non-linearity of the switch output capacitance .

This chapter proposes a three-phase three-level arm inductor-less MMC (3L-AIMMC) for low-voltage applications. Three possible modulation schemes are discussed and compared for the proposed topology. Phase voltage and current, switching loss, capacitor voltage ripple and rms current are compared by simulation and experimental results.

The chapter is organized as follows: the operating principle and main switching states of the proposed topology are presented in Sec. 6.2. Simulation results are reported in Sec. 6.3. Experimental validation is presented in Sec. 6.4. Lastly, a conclusion is presented in Sec. 6.5.

6.2 Principle of Operation and Modulation Techniques

In this section, the operation principle of the proposed 3L-AIMMC is introduced. Three different modulation techniques are investigated: i) Phase-Shifted (PS); ii) inner; and iii) outer modulation.

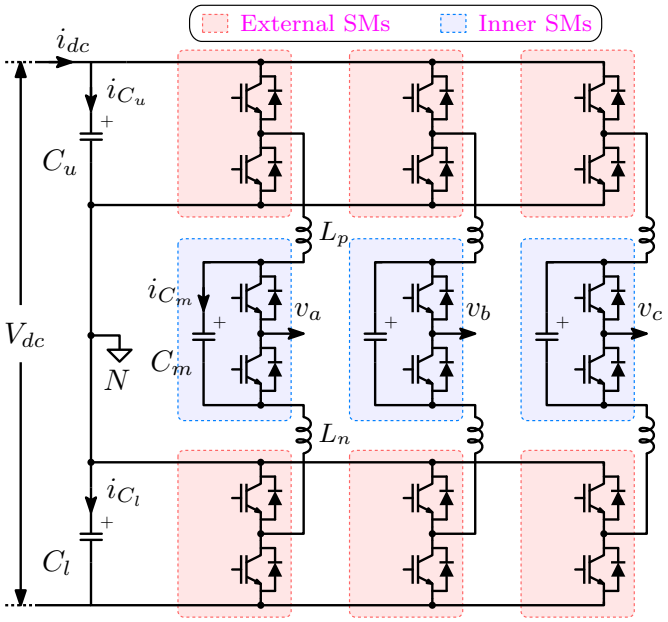


FIGURE 6.1: The proposed three-phase three-level Modular Multilevel Converter (MMC).

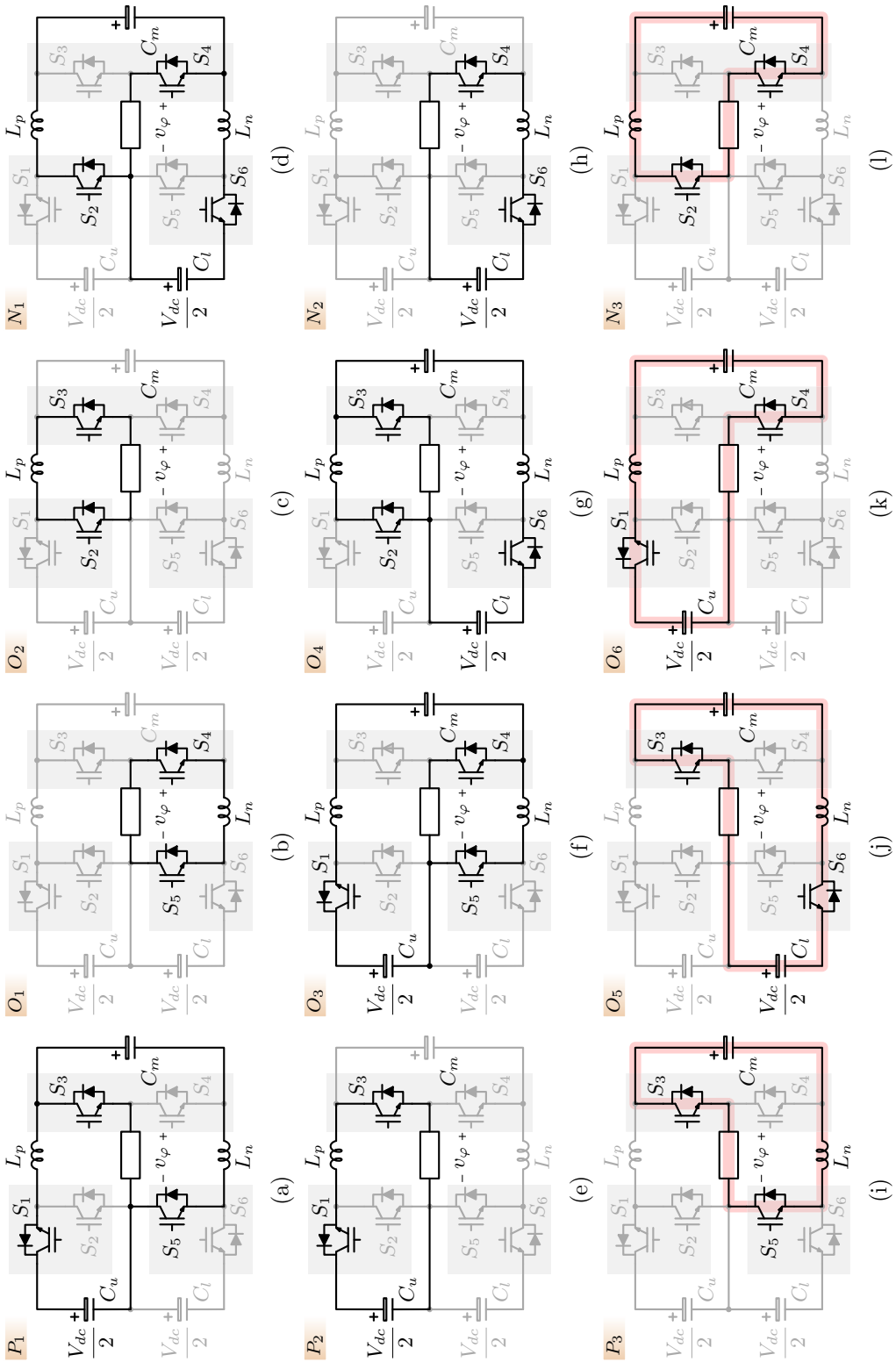


FIGURE 6.2: Possible switching states of the proposed three-level Modular Multilevel Converter (MMC)

6.2.1 Principle of Operation

As shown in Fig. 6.1, the proposed 3L-AIMMC is assembled by three half-bridge SMs denoted as an upper, middle, and lower SMs. Each SM is composed of two IGBTs. Each IGBT has to block half of the dc-link voltage. The bus-bar inductance connecting the upper SM to the middle one and the inductance of the bus-bar connecting the middle SM to the lower one are assumed equal and denoted by L_p and L_n, respectively. The upper and lower SMs are supplied from the upper (C_u) and lower (C_l) dc-link capacitors, respectively. The upper and lower dc-link voltages are assumed constant. The capacitance (C_m) represents the middle SM capacitance. The three-phase voltages (v_a, v_b and v_c) are referred to the neutral point N. The dc input voltage is denoted by V_{dc}.

6.2.2 Switching States

The switching signals are S_i, where the subscript i represents the switch number. There are six control signals for each phase. The 3L-AIMMC switching states are introduced in Table. 6.1. The circuit diagrams of each switching state are depicted in Fig. 6.2. The phase voltage v_a can be either $V_{dc}/2$, 0 or $-V_{dc}/2$. The $V_{dc}/2$ level can be achieved by turning ON S_1 and S_3, while S_5 can be either turned ON or OFF as shown in Fig. 6.2(a) and Fig. 6.2(e), receptively. The $-V_{dc}/2$ level can be achieved by turning ON S_4 and S_6, while S_2 can be either turned ON or OFF as shown in Fig. 6.2(d) and Fig. 6.2(h), receptively. There are four possible switching states by which the zero level can be achieved as depicted in Fig. 6.2(b), Fig. 6.2(c), Fig. 6.2(f) and Fig. 6.2(g). The load current flows through the middle capacitor during the switching states of Fig. 6.2(i)-Fig. 6.2(l); therefore, these switching states are not used since they would result in a large voltage ripple over the middle capacitor C_m.

6.2.3 Commutation loops

Fig. 6.3 shows the typical steady-state waveforms during switches commutations. The commutation between S_1 and S_2 or S_5 and S_6 does not initiate a resonance since the phase current does not commutate between the upper and lower arms. During the commutation between S_3 and S_4, the phase current commutate between the upper and lower stray inductance; therefore, a resonance between the middle capacitor C_m and the two stray inductance L_p and L_n is initiated. The peak-to-peak voltage of the middle capacitor ΔV_{C_m} depends on the phase current, the

State	S_1	S_2	S_3	S_4	S_5	S_6	v_a
P_1	1	0	1	0	1	0	$\frac{V_{dc}}{2}$
P_2	1	0	1	0	0	0	
P_3	0	0	1	0	1	0	
O_1	0	0	0	1	1	0	0
O_2	0	1	1	0	0	0	
O_3	1	0	0	1	1	0	
O_4	0	1	1	0	0	1	
O_5	0	0	1	0	0	1	
O_6	1	0	0	1	0	0	
N_1	0	1	0	1	0	1	$-\frac{V_{dc}}{2}$
N_2	0	0	0	1	0	1	
N_3	0	1	0	1	0	0	

TABLE 6.1: Switching States of the Proposed Discontinuous Modular Multilevel Converter (DMMC) topology

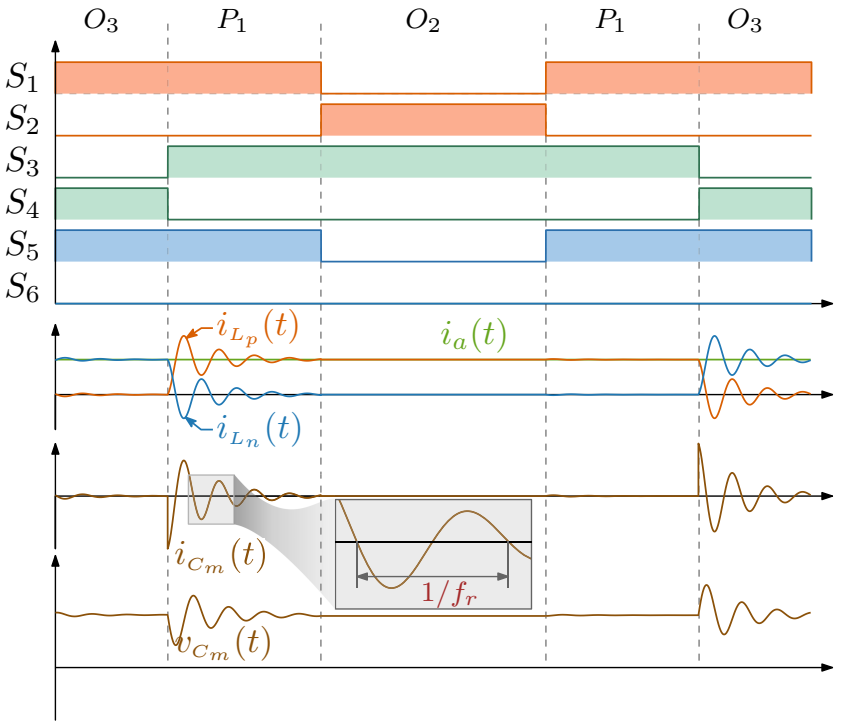


FIGURE 6.3: Steady-state waveforms during switches commutation.

stray inductance of the upper and lower arms, and the middle capacitance. The worst case value of ΔV_{C_m} occurs at the peak value of the phase current as follows:

$$\Delta V_{C_m} = \hat{I}_a \sqrt{\frac{L_p + L_n}{C_m}} \tag{6.1}$$

It can be noted from (6.1) that the higher the stray inductance of the long commutation loop, the higher the required capacitance for the middle SM for the same peak-to-peak voltage.

6.2.4 Modulation Techniques

6.2.4.1 PS modulation

The switching signals and voltage waveform for the PS modulation scheme are depicted in Fig. 6.4. The external SMs switches S_1, S_2, S_5, and S_6 commutate with the carrier signal according to the reference signal ref_1. The reference signal (ref_2) for the inner SM switches S_3 and S_4 is π phase-shifted from the reference signal of the external SMs. In order to reduce the switching losses, S_1 is turned OFF during the negative voltage half cycle while S_6 is turned OFF during positive voltage half cycle. The effective switching frequency of the output voltage in this

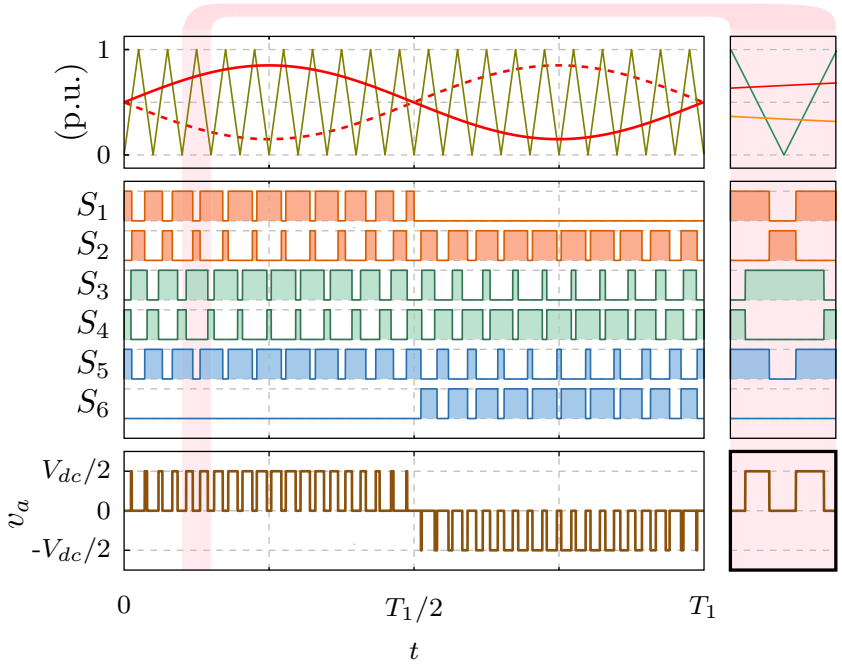


FIGURE 6.4: Phase-shifted (PS) modulation technique.

case is two times the switching frequency of SMs. The interleaving between the outer and inner SMs is producing this multiplication effect.

During the positive half-cycle, the switching state P_1, shown in Fig. 6.2(a), is utilized to generate the positive voltage. The load current flows through S_1 and S_3. The zero voltage state is generated, alternately, by the switching states O_2 and O_3. As the transition between the switching states P_1 and O_3 involves commutation of the inner SM, the resonance is initiated due to the commutation of load current from the upper arm to the lower arm.

During the negative half-cycle, the switching state N_1 generates the negative voltage at the output, while, the zero voltage is achieved by O_1 and O_4 switching states. The resonance is initiated during the transition between N_1 and O_4 as it requires commutation of S_4 and S_3.

6.2.4.2 Inner modulation

The waveforms for the inner modulation scheme is depicted in Fig. 6.5. The upper SM is inserted during the positive voltage half cycle by turning ON S_1 while S_2 is turned OFF. The lower SM is bypassed during the positive voltage half cycle by turning ON S_5 while S_6 is turned OFF. Similarly, S_2 and S_6 are turned OFF during the negative voltage half cycle while S_1 and S_5 are turned OFF. S_3 and S_4 of the middle SM commutate with the carrier signal according to the reference

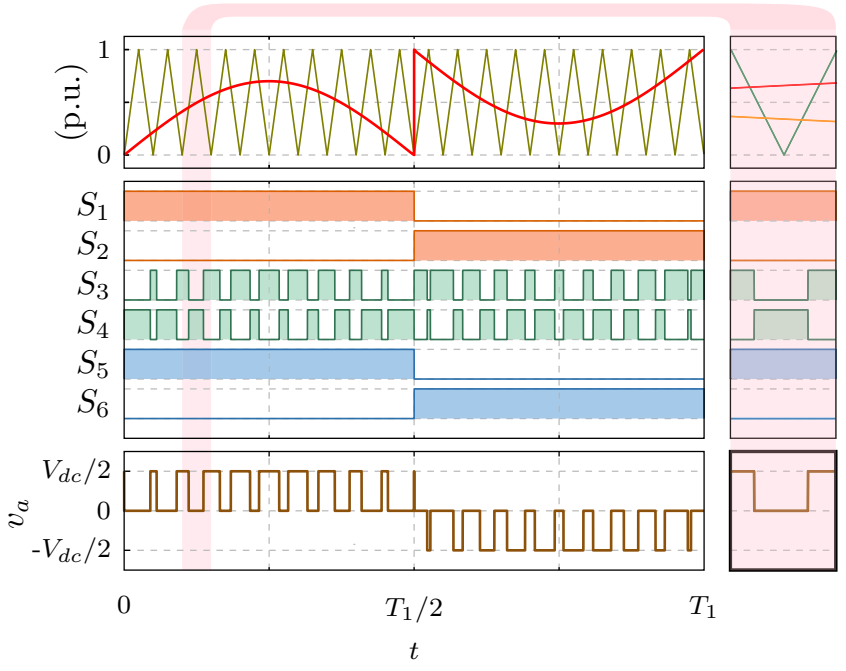


FIGURE 6.5: Inner modulation technique.

signal v_a^*. In this case, the effective switching frequency of the output voltage is equal to the switching frequency of submodules.

The positive and zero voltage states are generated using the switching states P_1 and O_3, respectively, during the positive half-cycle. During the negative half-cycle, the switching states N_1 and O_4 are generating the negative and zero voltage states, respectively.

6.2.4.3 Outer modulation

Fig. 6.6 shows the waveforms of the outer modulation scheme. The middle SM is commutated only every cycle half; therefore, the rms current of the middle capacitor in this case is the minimum between the three modulation schemes. S_3 is turned ON during the positive voltage half cycle while S_4 is switched ON during the negative half-cycle. The external SMs switches S_1, S_2, S_5, and S_6 commutate with the carrier signal according to the reference signal (ref). Similarly to the inner modulation scheme, the effective switching frequency of the output voltage is equal to the switching frequency of SMs. During the positive half-cycle, the positive and zero voltage states are generated by P_2 and O_2, respectively. The switching states N_2 and O_1 generate the negative and zero voltage states, respectively, during the negative half-cycle.

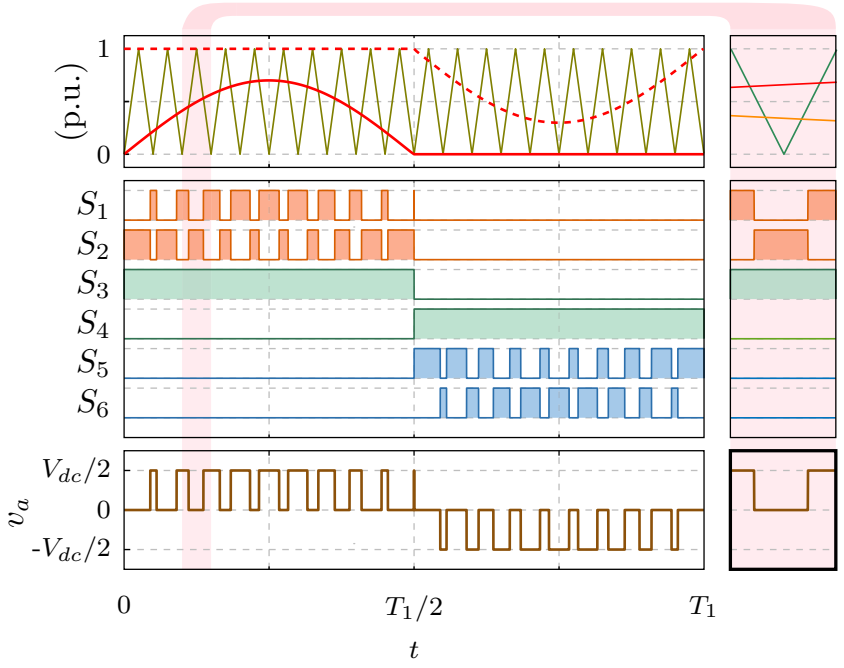


FIGURE 6.6: Outer modulation technique.

6.3 Simulation Results

To validate the performance of the proposed 3L-AIMMC, a 230 V_{rms} 30 kVA simulation model has been developed using PLECS with the parameters listed in Table. 6.2. The three modulation schemes discussed in Sec. 6.2 have been simulated. Fig. 6.7 shows the simulation results in steady-sate.

	Parameter	Symbol	Value
Specifications	Nominal power	P	30 kVA
	Input voltage	V_{dc}	800 V
	Output phase voltage	V_{φ}	230 V_{rms}
	Line frequency	f	50 Hz
	Switching frequency	f_s	20 kHz
Parameters	Stray inductance	L_p, L_n	85 nH
	Inner SM capacitance	C_m	3.18 μF
	Filter inductance	L_f	120 μF
	Filter capacitance	C_f	325 μF

TABLE 6.2: Three-Phase 3L-AIMMC Specifications and Parameters for Simulation and Experiment

6.3.0.1 Middle capacitor voltage and current

As shown in Fig. 6.7(g) and Fig. 6.7(h), the inner capacitor rms current of the PS and inner modulation schemes are approximately equal as they both invloves commutation of the load current. The minimum voltage ripple and rms current of the inner capacitor can be achieved using the outer modulation scheme.

6.3.0.2 Output performance

The peak-to-peak current ripple of the phase current (i_a) is doubled in the inner and outer modulation schemes, as depicted in Fig. 6.7(e) and Fig. 6.7(f) which means that the output inductance has to be doubled to have the same output current ripple achieved by the PS modulation.

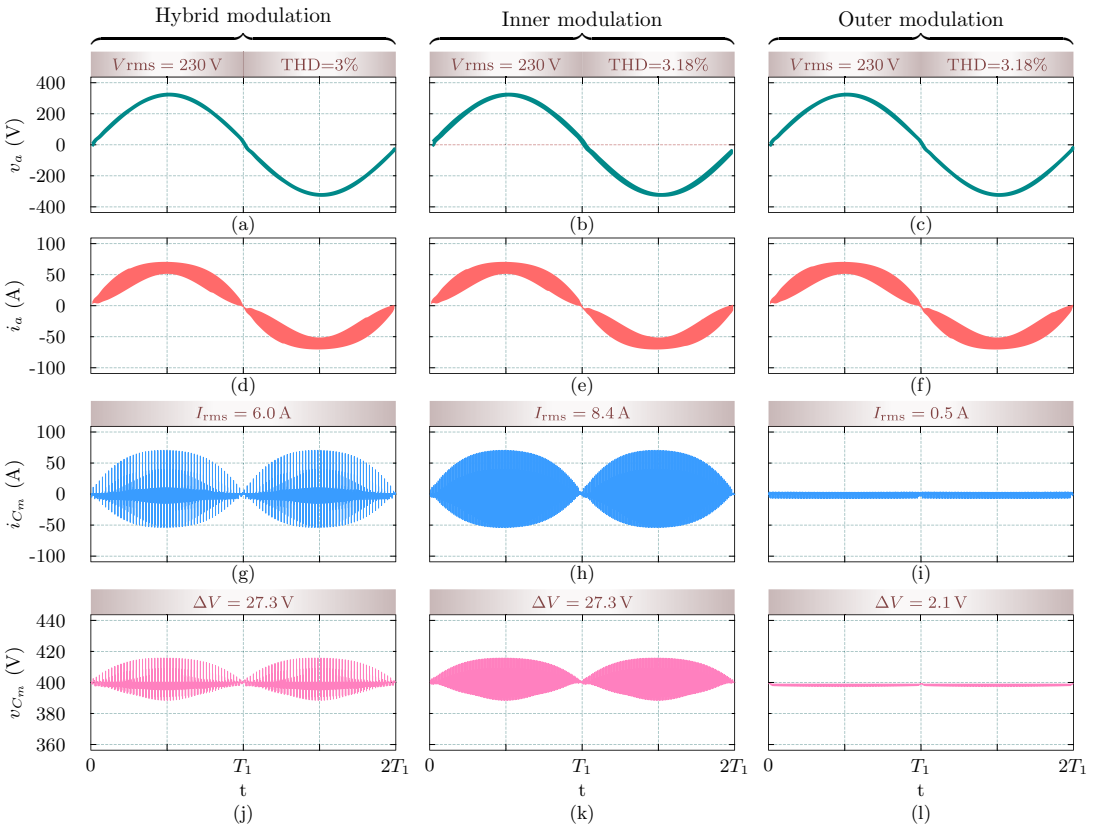


FIGURE 6.7: Simulation results for the proposed 3L-AIMMC.

6.3.0.3 Semiconductor loss

Fig. 6.8(a) shows the conduction and switching loss of the different IGBTs using the three modulation schemes. The conduction loss of the three cases are approximately equal. The switching losses of S_1, S_2, S_5, and S_6 are almost zero in the case of the inner modulation. The switching losses of S_3 and S_4 is almost zero in the outer modulation. It can be noted from Fig. 6.8(b) that the PS modulation has the highest total semiconductor losses since it involves high frequency commutation of all the six IGBTs.

6.3.0.4 Comparison between the 3L-ANPC and the proposed 3L-AIMMC

Fig. 6.9 shows comparison between the 3L-ANPC and the proposed 3L-AIMMC. It can be noted that the over-voltage across the switch S_3 in case of the 3L-ANPC is more than two times the average value.

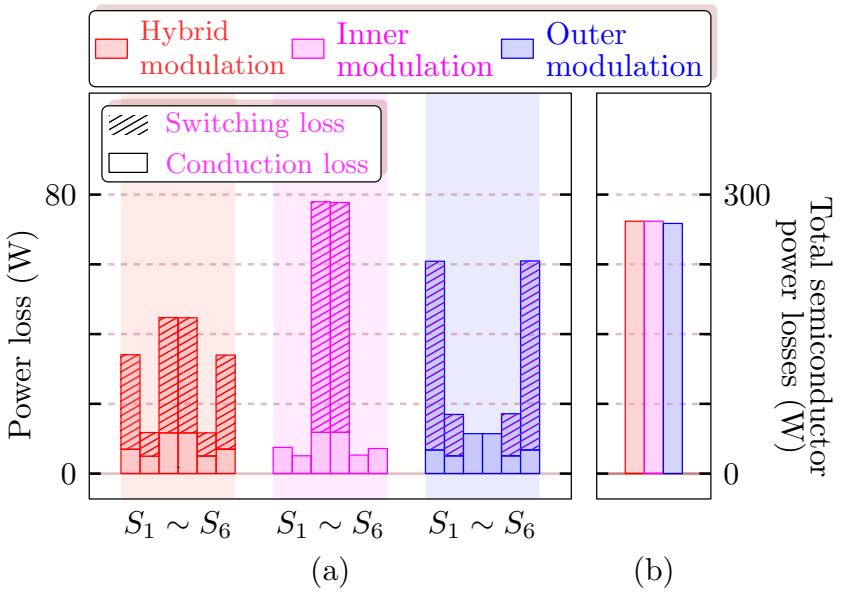


FIGURE 6.8: (a) The conduction and switching losses of the different IGBTs using the PS, inner, and outer modulation; (b) The total semiconductor power losses.

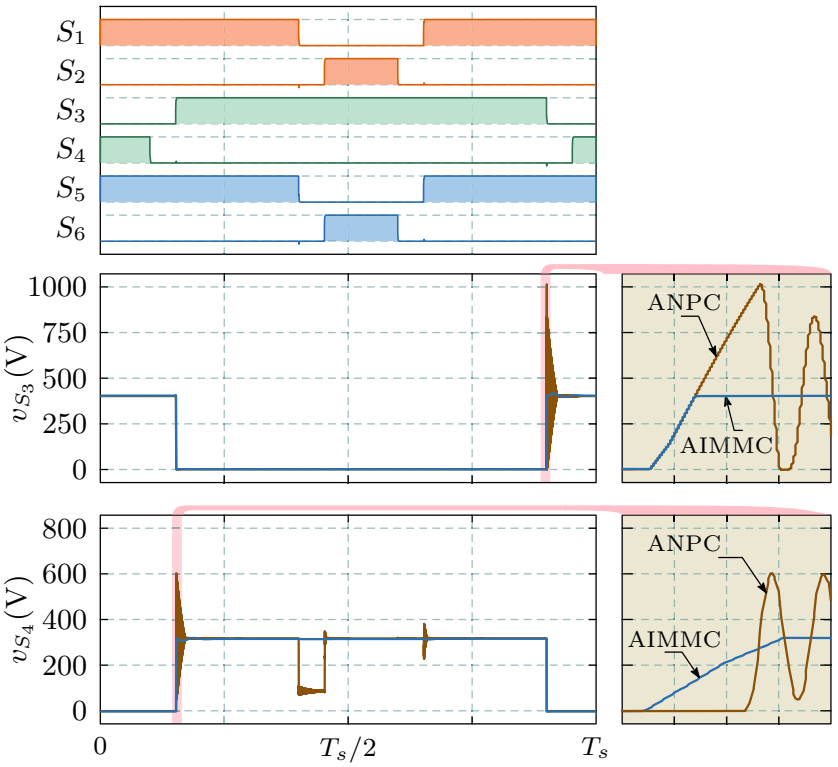


FIGURE 6.9: Simulation results using LTspice: comparison between the 3L-ANPC and the proposed 3L-AIMMC.

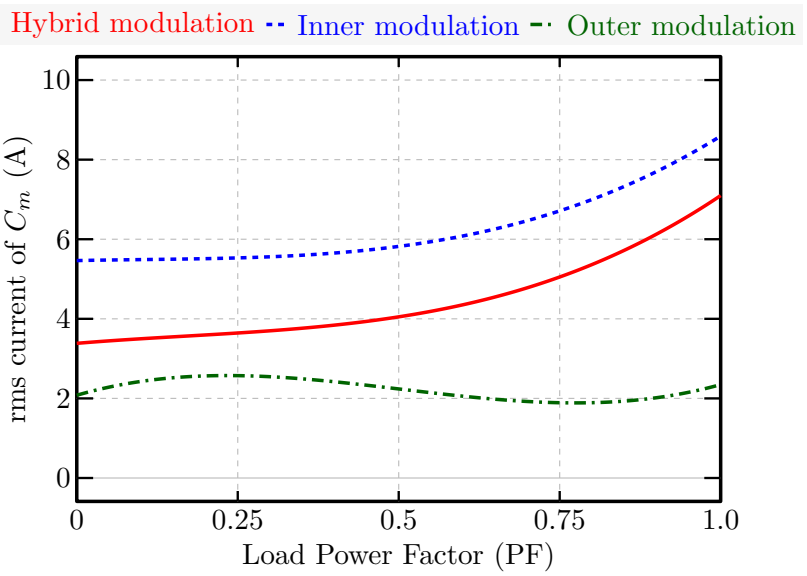


FIGURE 6.10: The effect of the load power factor (PF) on the rms current of the middle capacitor.

6.3.0.5 Non-unity power factor operation

Fig. 6.10 reports the rms current of the middle capacitor with different PF values. As the load power factor (PF) decreases, the rms current of the middle capacitor decreases.

6.4 Experimental Validation

To validate the proposed topology and the different modulation schemes, the topology implementation and the main experimental results are presented in this section.

Experimental results are obtained from the single-phase 3L-AIMMC prototype shown in Fig. 6.11 designed according to the specifications and parameters listed in Table. 6.2. The 3L-AIMMC structure has been built using three SEMIKRON SEMiX402GB066HDs IGBT modules rated at 600 V 400 A. The inverter is supplied from an 600 V dc supply. A 3.18 μF is used for the middle SM. The control part and the reference signals are generated by a DSP-based board while generating the switching signals for each IGBT is achieved by an FPGA board.

The double-pulse test, shown in Fig. 6.12, is conducted to show the switching performance of the long commutation loop and to estimate the stray arm inductance. While S_1 is switched ON, S_3 is turned ON at $t = t_1$ then turned OFF at

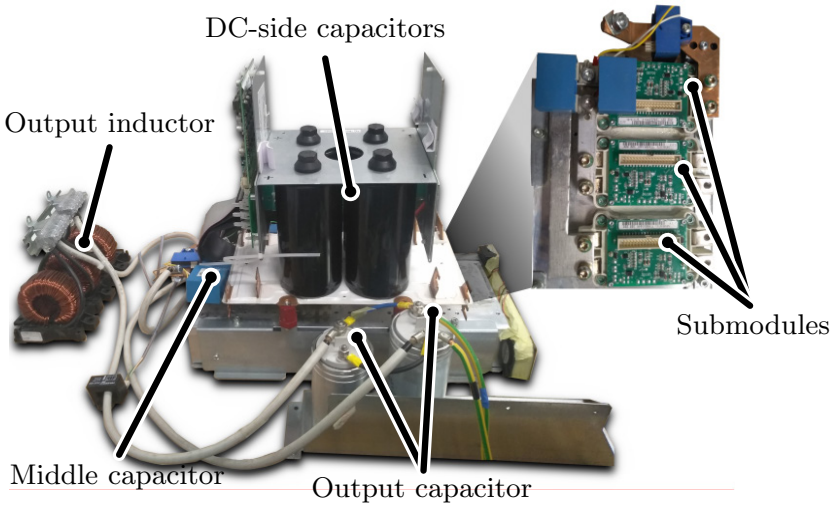


FIGURE 6.11: Photo of the experimental MMC prototype.

$t = t_2$. It can be noted that the resonance circuit is initiated with a frequency f_r and an amplitude proportional to the load current. Assuming that the stray inductances of the upper and lower arms are identical, the stray inductances of the upper L_p and lower L_n arms can be estimated from the middle capacitance and the resonance frequency as follows:

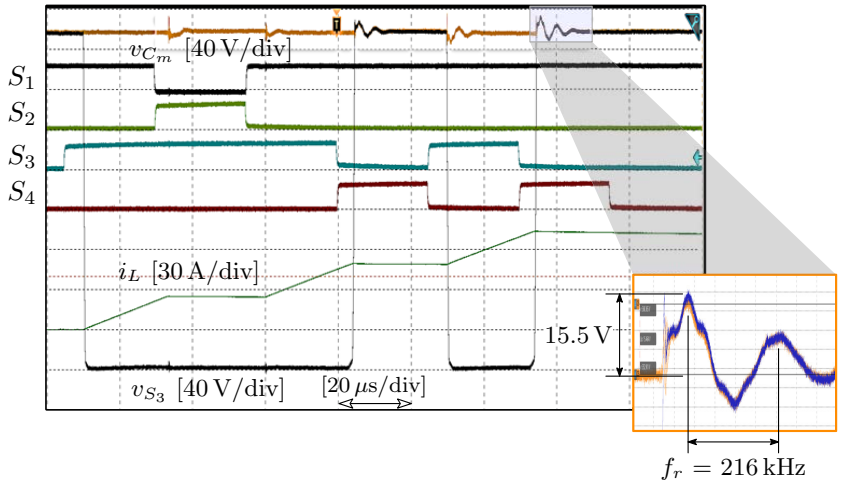


FIGURE 6.12: Double-pulse test for commutations of the different switches in the proposed 3L-AIMMC.

$$L_p = L_n = \frac{1}{2} \cdot \frac{1}{4\pi^2 f_r^2 C_m} = 85\,\text{nF} \tag{6.2}$$

The middle SM capacitance can be designed to limit the voltage overshoot as follows:

$$C_m = \frac{\hat{I}_a^2(L_p + L_n)}{\Delta V_{C_m}^2} \tag{6.3}$$

Fig. 6.13 shows the experimental results for the three modulation schemes. It can be noted that, the lowest rms current of the middle can be achieved by the outer modulation.

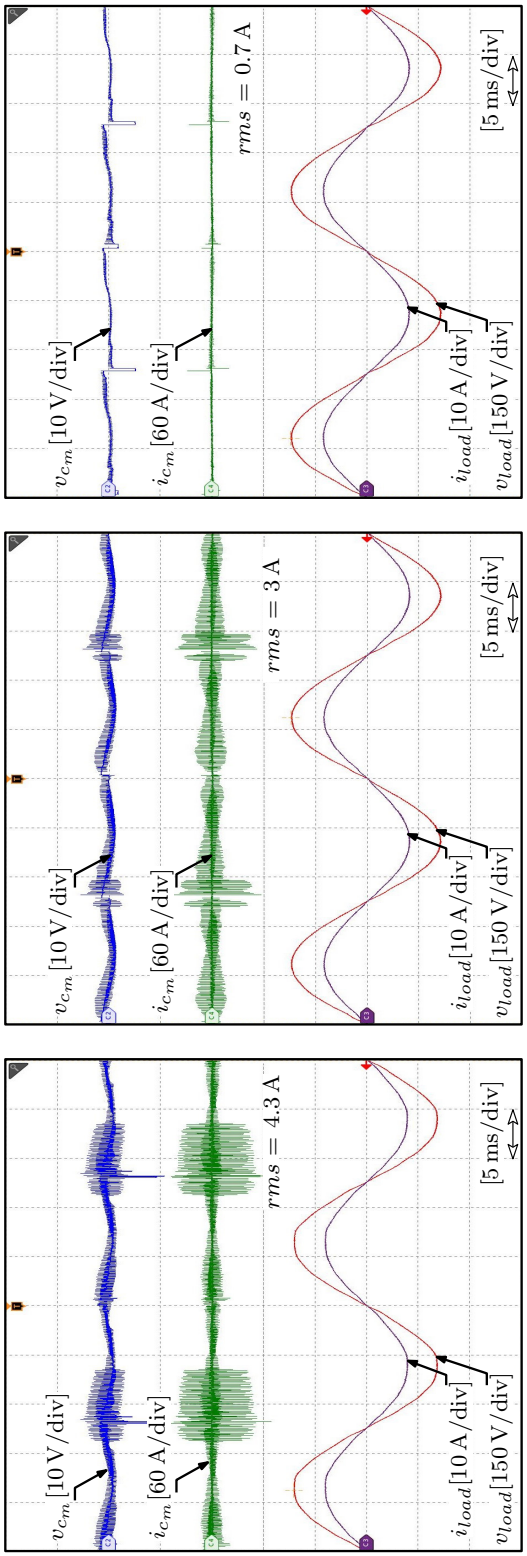


FIGURE 6.13: Experimental results. a) Phase-shifted (PS), b) inner, and c) outer modulation.

6.5 Summary

A three-phase three-level arm inductor-less MMC is proposed in this chapter. Different from the existing MMC topologies, the capacitance requirement is very small. Three different modulation schemes are discussed for the proposed topology. Simulation and experimental results show that the minimum middle capacitor voltage ripple and rms current can be achieved by applying the outer modulation scheme. On the other hand, the highest output voltage/current quality can be achieved by applying PS modulation scheme.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

In this thesis, the application of MMCs in Low-Voltage (LV) Photovoltaic (PV) systems is investigated. Based on the results obtained in this work, the proposed MMC is a suitable converter to be used in LV PV applications. The main contributions of this work are summarized below.

- An enhanced modulation scheme for a three-phase five-level MMC is proposed in which the upper and lower submodules are connected in parallel. By using this modulation scheme, a reduction of about $10-25\%$ in the required capacitance has been achieved. The proposed modulation scheme, together with the circulating current control, is capable of reducing the ripple of the capacitor voltage over a wide operating range.
- A modified MMC topology for LV applications is proposed. While maintaining the advantages of the MMC structure, the capacitance requirements for a three-phase four-wire system are greatly reduced. The effectiveness of the proposed topology and the proposed analysis and design procedure is confirmed by simulation and experimental results. The capacitance is reduced from 12 capacitors in the conventional MMC to three capacitors. Not only the number of capacitors is reduced, but also the capacitance of each capacitor is greatly reduced.
- A voltage controller is proposed for the modified MMC structure as an alternative to control the circulating current with a reduced number of current sensors. Instead of six current sensors, only three are used. The proposed approach is validated by simulation and experimental results.

- The DCM of the proposed MMC is investigated, resulting in a three-level arm inductor-less MMC with very low inductance and capacitance requirements. Different modulation schemes are investigated for this topology.

7.2 Future work

There are some research aspects to be considered in the future such as:

- Using SiC devices instead of the Si ones can highly reduce the losses of the conveter; therefore, adopting SiC devices to enhance the efficiency of the proposed MMC is an interesting point to study.
- The appication of MMC topologies in the multi-port converters and solid-state transformers where a large number of cascaded converters are needed is also an interesing topic to investigate.

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