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An investigation of defects and reliability issues on Gallium Nitride devices

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An investigation of defects and reliability issues on Gallium Nitride devices

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Alla mia Famiglia.

Abstract

In this thesis a extensive study of devices based on AlGaN/GaN heterostructure is reported. The work is fundamentally divided in two main topic: the first part is related to the investigation of traps and defects and their effects on the device performances; the second part is instead related to the reliability studies of this type of devices.

The investigation of trapping effects is based on pulsed measurements of output characteristic and transcharacteristic of the device under test. The measurements carried out on High Electron Mobility Transistors (HEMT) with different gate materials (Ni/Au/Ni or ITO) and absence or presence of the surface passivation layer have shown how this technique can be used as a rapid and effective method to distinguish between the trapping phenomena occurring in the region under the gate and those occurring in the gate - drain access region. In particular we have seen that unpassivated devices have a transconductance peak dispersion, which can be ascribed to the presence of surface traps (absent in passivated devices). On the other hand the presence of a threshold voltage shift (found in the ITO samples) is related to traps below the gate electrode. The presence of traps under the ITO contact has been confirmed by low frequency capacitance - voltage measurements. Also the pulsed measurements have been correlated to electroluminescence characterization of the transistor showing the role of traps in limiting the maximum gate-drain electric field and, consequently, the intensity of the emitted light, related to the equivalent electron temperature. The combined dynamic IV - electroluminescence measurement technique has been also used in the analysis of state of the art GaN-HEMTs on Silicon substrate. The measurements carried on samples with different gate recess width and same gate length show better performances (in terms of frequency dispersion and gate - drain electric field) for transistors with shorter recess width.

The analysis of defects in GaN-based devices has been carried out also by means of low frequency noise measurements. The purpose of the work on noise was to find a correlation between the intensity of the measured noise and the performances of the device (in particular the breakdown). Several devices have been tested (transistors and *transmission line model* - TLM) with different realization technology (aluminum content, ohmic contact annealing temperature, composition of ohmic contact electrode).

A real correlation between noise in the conductive channel and breakdown has not been found; while measurements on the TLM show a possible relation between ohmic contact specific resistance and noise.

The reliability of several samples has been investigated by means of both long-term stress (1000 h DC life-test) and short-term stress (2 min step-stress).

The long - term stress has been carried out on AlGaN/GaN HEMTs processed on composite SopSiC substrate developed within the European HYPHEN project. These substrates have been realized through the transfer of a thin single crystal silicon layer on the top of a thick polycrystalline silicon carbide wafer. The aim of this project is to provide a valid and less expensive substrate for GaN - based devices in respect to the traditional bulk-SiC substrates. Three stress conditions (different DC biases and different ambient temperatures) have been selected for the test. The results at the end of the stress present good device stability and promising performance; reliability issues found in few samples are linked to the high levels of gate leakage current reached during the stress. This proves that devices failure can be ascribed to the technology used for the realization of transistors and does not appear correlated to the nature of the composite substrate.

With concern the short-term stress, we have studied the influence of gate reverse bias test on the overall behavior of the transistor. This type of accelerated test usually brings to the definition of a critical voltage beyond that the gate leakage current increases drastically up to the failure of the device. In literature the phenomenon is called *inverse piezoelectric effect* and it is considered related to the lattice strain occurring during the stress. Our study was based on a split wafer experiment adopting passivated AlGaN/GaN HEMTs with different gate metallizations: Ni/Au/Ni, ITO, Ni/ITO. The results obtained suggest that the critical voltage is not related only to the piezoelectric strain, but also the initial gate leakage current of the fresh device plays a role in the degradation process. Moreover the dynamic of the degradation during the test seems to indicate that the ageing process can be ascribe to a defect percolation process in the AlGaN barrier layer.

Sommario

L'argomento esposto in questa tesi riguarda uno studio approfondito di dispositivi su eterostruttura AlGaN/GaN. Questo lavoro può essere suddiviso in due argomenti principali: la prima parte riguarda lo studio di trappole e difetti e il loro effetto sulle prestazioni del dispositivo; la seconda parte è invece dedicata allo studio dell'affidabilità di questo tipo di dispositivi.

L'analisi degli effetti trappola è basata sulla misurazione impulsata della caratteristica di uscita e della transconduttanza del dispositivo in esame. Le misure eseguite su transistor con diversa composizione dell'elettrodo di gate (Ni/Au/Ni o ITO) e presenza o assenza dello strato di passivazione hanno mostrato come questa tecnica può essere utilizzata come rapido e valido sistema per distinguere tra gli effetti di trappole presenti nella regione sottostante il gate e quelli di trappole nella regione di accesso gate - drain. In dettaglio si è visto che dispositivi non passivati presentano una diminuzione del picco della transconduttanza, fenomeno riconducibile alla presenza di trappole superficiali; mentre nel caso di variazione della tensione di soglia (dispositivi con elettrodo di gate in ITO) le trappole sono localizzate nella regione al di sotto del contatto di gate. La presenza di trappole sotto il contatto in ITO è stata inoltre confermata da misure di capacità vs. tensione a bassa frequenza. Le misure impulsate sono state poi messe in relazione con le misure di elettroluminescenza effettuate sui transistor: questo confronto ha mostrato come le trappole presenti nel dispositivo limitino il massimo campo elettrico tra gate e drain e quindi l'intensità della radiazione emessa. Questa metodologia è stata poi applicata per l'analisi di dispositivi GaN su silicio caratterizzati da identica lunghezza del contatto di gate ma diversa ampiezza del recesso di gate. Dai risultati ottenuti si può vedere che le prestazioni migliori, in termini di dispersione in frequenza e massimo campo elettrico, si hanno nei dispositivi con recesso più piccolo.

L'analisi dei difetti presenti nei dispositivi su GaN è stata effettuata anche per mezzo di misure di rumore a bassa frequenza. Lo scopo di questa parte di attività era di trovare una correlazione tra il livello di rumore misurato e le caratteristiche elettriche del dispositivo (in particolare il breakdown). Diversi dispositivi sono stati testati (transistor e *transmission line model* - TLM) con differenti tecnologie di realizzazione (percentuale di alluminio, temperatura di processo, composizione dell'elettrodo

dei contatti ohmici). Una correlazione rumore del canale conduttivo e breakdown non è stata trovata; mentre le misure sulle TLM hanno mostrato un possibile legame tra rumore e resistenza specifica del contatto ohmico.

L'affidabilità dei dispositivi stata studiata per mezzo di prove di stress a breve (2 min step - stress) e lungo termine (1000 h).

Lo stress a lungo termine è stato eseguito su dispositivi AlGaN/GaN processati su substrato composito di tipo SopSiC sviluppato nell'ambito del progetto europeo HYPHEN. Questi substrati sono realizzati tramite il trasferimento di un sottile strato di Silicio monocristallino su uno strato più spesso di Carburo di Silicio policristallino, il loro scopo è di rappresentare una valida ed economica alternativa ai substrati in Carburo di Silicio monocristallino. Per questo esperimento sono state individuate tre condizioni a differente polarizzazione e temperatura; i risultati finali presentano una buona stabilità dei dispositivi ed inoltre mostrano come i problemi riscontrati durante il test siano riconducibili agli elevati livelli di corrente di perdita del gate. Il degrado dei dispositivi è quindi strettamente legato alla tecnologia del processo utilizzato per la realizzazione del transistor e non è legata alla natura del substrato.

Per quanto riguarda la prova di stress accelerato, si è studiato l'effetto sulle prestazioni del dispositivo di elevate tensioni negative applicate al contatto di gate. Questo tipo di test solitamente porta all'individuazione di una tensione critica oltre la quale si verifica un brusco aumento della corrente di gate. Nella letteratura scientifica questo fenomeno è indicato come *effetto piezoelettrico inverso* (*inverse piezoelectric effect*) ed è associato alla creazione di difetti nel reticolo cristallino sottoposto a sollecitazione durante lo stress. Lo studio si è basato su un wafer con differenti metallizzazioni di gate (Ni/Au/Ni, ITO, Ni/ITO) e con passivazione dei dispositivi. I risultati ottenuti suggeriscono che la tensione critica non sia legata solo alla tensione che si induce nel reticolo; infatti anche il livello iniziale della corrente di perdita del gate sembra giocare un ruolo nel processo di degradazione. Inoltre l'evoluzione del degrado durante il test sembra indicare che il processo di invecchiamento avvenga per filtrazione dei difetti all'interno della barriera di AlGaN (*percolation process*).

Contents

List of Publications

Journals

1. M. Meneghini, N. Ronchi, A. Stocco, G. Meneghesso, U. K. Mishra, Yi Pei, E. Zanoni, "Investigation of trapping and hot-electron effects in GaN HEMTs by means of a combined electro-optical method", *IEEE Transactions on Electron Devices*, Vol. 58, Issue 9, Sept. 2011

2. M. Meneghini, A. Stocco, N. Ronchi, F. Rossi, G. Salviati, G. Meneghesso, and E. Zanoni, "Extensive analysis of the luminescence properties of AlGaN/GaN high electron mobility transistors", *Applied Physics Letters*, Vol. 97, Issue 6, 2010

3. G. Meneghesso, M. Meneghini, A. Tazzoli, N. Ronchi, A. Stocco, A. Chini and E. Zanoni, "Reliability issues of Gallium Nitride High Electron Mobility Transistors", *International Journal of Microwave and Wireless Technologies*, Vol. 2, Issue 01, Feb. 2010, pp 39-50

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2. F. Rampazzo, A. Stocco, R. Silvestri, M. Meneghini, N. Ronchi, D. Bisi, F. Soci, A. Chini, G. Meneghesso, and E. Zanoni, "Impact of Hot Electrons on the Reliability of AlGaN/GaN High Electron Mobility Transistors", 20^{th} *European Heterostructure Technology meeting (HETECH) 2011*, Lille, France, 7-9 Nov. 2011

3. E. Zanoni, G. Meneghesso, M. Meneghini, A. Stocco, F. Rampazzo, R. Silvestri, I. Rossetto, N. Ronchi, "Electric-field and thermally-activated failure mechanisms of AlGaN/GaN High Electron Mobility Transistors", 220^{th} *ECS Meeting*, Boston, Massachusetts, 9 - 14 Oct. 2011

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1

Introduction

When the request of more efficient and powerful devices for wireless communications systems (portable phones, satellite communication, wireless networks, intelligent transportation systems - ITS, etc.) has started to drastically increase, the telecommunications industry has moved its research from silicon technology, which physical limits have been reached, to the compound semiconductor technology.

The scientific research on compound semiconductors, such as GaAs and InP, has brought to the realization and the industrial production of electronic devices able to work at very high frequency; but still the power that this kind of devices can handle is lower than the effective requirements of the telecommunication market. For this reason the research is now focused on the study of gallium nitride based devices: GaN shows high breakdown voltage and good electron mobility, resulting as the ideal candidate for the realization of microwave-power transistors [1].

In table 1.1 we present some physical properties of the gallium nitride compared with those of other semiconductors. In literature is really common to refer to the Johnson's figure of merit (JFOM), which describes the potential of particular technology independently of design details but only considering the material properties. The JFOM is defined as:

$$JFOM = \left(\frac{E_{bk} v_s}{2\pi} \right) \tag{1.1}$$

where E_{bk} is the breakdown electrical field and v_s the saturation velocity. Generally the JFOM is expressed as the ratio between the calculated FOM and the FOM of a reference material (in this case silicon). As one can see, the gallium nitride is the best semiconductor compared to the others.

The same concept is clearly shown in Fig. 1.1, where the different working regions for electronic devices fabricated with different semiconductors are reported: gallium nitride results again the best choice for high-power and high-frequency applications.

Property	Units	Si	GaAs	4-SiC	GaN
Bandgap	eV	1.1	1.42	3.26	3.39
Relative dieletric constant	-	11.8	13.1	10	9
Electron mobility	$cm^2/V\,s$	1350	8500	700	1200-2000
Break down field	10^6 V/cm	0.3	0.4	3.0	3.3
Saturation electron velocity	-	1.0	1	2.0	2.5
Thermal conductivity	W/cm K	1.5	0.43	3.3-4.5	1.3
JFOM	-	1	2.7	20	27.5

Table 1.1: Physical properties and figures of merit of widely used semiconductors [2].

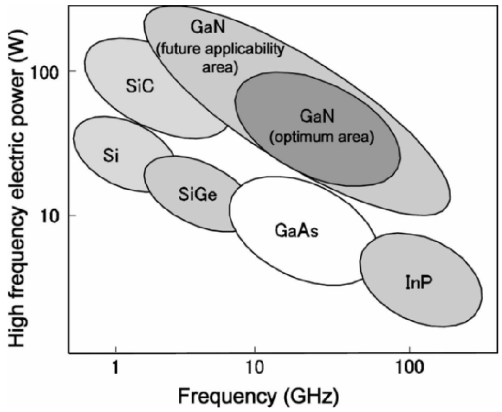


Figure 1.1: Operating frequencies and output power of electron devices fabricated using different semiconductors [3].

A particular characteristic of GaN is that it can be used to form heterojunctions device with high performances: the AlGaN/GaN heterostructure is employed in the realization of transistors with very high carrier density in the conductive channel, high mobility (close to the one of the intrinsic material) and high saturation velocity. This device are indicated as High-Electron Mobility Transistors (**HEMTs**), to highlight the fact that they are designed to work at high frequency. GaN HEMTs are characterized by high current densities, low channel and access resistances, better noise figure than MESFETs realized on SiC or GaN. Moreover they do not need external doping to enhance carrier concentrations: channel charge is due to internal spontaneous polarization and piezoelectric polarization which depend on the realization process.

The continuous efforts directed to the improvement of GaN-based HEMTs have made possible the realization of devices for high-power, high-frequency, and high-temperature applications. Thanks to the research efforts, devices with cut-off frequency f_T = 181 GHz on a transistor with 30 nm gate length, a power-added efficiency (PAE) of 60% at 4 GHz, and output power density in excess of 40 W/mm have been recently

demonstrated [4, 5].

Despite the excellent potential of GaN-HEMTs, their performance can still be limited by dispersion effects related to the presence of trap states; furthermore the ageing mechanism that reduce the useful life of the devices are not completely understood yet. In this thesis an analysis of these two important aspects is presented. The work is organized in the following main arguments.

- The gallium nitride physical properties and the HEMTs working principles are explained from a theoretical point of view, including a brief description of the main trap-related and reliability aspects studied in the scientific literature.

- A new measurement technique is presented, this methodology results from the combination of double-pulsed current-voltage measurements with electroluminescence measurements. The advantage of this technique is that it allows a rapid evaluation of the trapping and hot-electron-related characteristics, providing information on the presence of traps in the region under the gate and information about their effect on the electric field and on the equivalent electron temperature.

- The low-frequency noise measurement is analyzed from the theoretical point of view, also a detailed study of the measurement system is presented. The technique is applied to GaN-based devices (transistors and TLMs) in order to study the behavior of low-frequency noise in these samples.

- The results of a DC-life test carried out on AlGaN/GaN samples are presented. The stress is carried out at different junction temperature and at different bias in order to define the most ageing condition for the devices.

- The final chapter describes the results of a short-term stress on GaN-HEMTs focusing on the effect of a particular type of test (the *step-stress*) and, by comparing different technologies, the possible degradation mechanisms are analyzed.

2

Material and Device Properties

In this chapter we will present the behavior of a GaN-based HEMT, starting from the material properties to the traps and reliability issues related to this type of devices.

The basic structure of a HEMT is shown in Fig. 2.1; in this simplified form we can see a generic substrate where three main layers are grown by epitaxial techniques: a nucleation layer (NL), a thick GaN layer (typically $\sim 2\,\mu m$), indicated as the *buffer* or *channel* layer and a thin AlGaN layer ($\sim 20\,nm$), called *barrier* layer. A conductive channel is formed at the AlGaN/GaN interface, that connects drain to source; the voltage bias applied to the gate allows the modulation of the channel resistance and, therefore, the current through the channel. In the AlGaN/GaN HEMT the conductive channel, constituted by a high carrier density ($n_s \sim 10^{13}\,cm^{-2}$), is called 2DEG (*two dimensional electron gas*). Normally GaN-HEMTs are depletion transistors: for zero bias applied to the gate ($V_G = 0$) the 2DEG is formed and if a voltage is applied between source and drain the current can pass through the channel (normally-on). If the gate bias is decreased to negative values, the electrical field modulates the 2DEG density and the channel resistance starts to increase, resulting in a lower drain current. When V_G is lower than the negative threshold voltage ($V_{TH} < 0\,V$) the transistor is turned-off (depletion-mode transistor).
In recent years the research has moved to the realization of enhanced-mode HEMTs, with ($V_{TH} > 0\,V$), but still further efforts are required to stabilize this new technology [6].

In the following we focus on the materials properties and on the 2DEG formation.

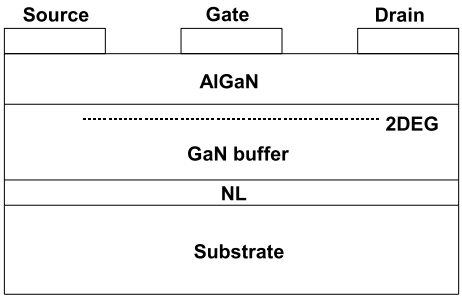
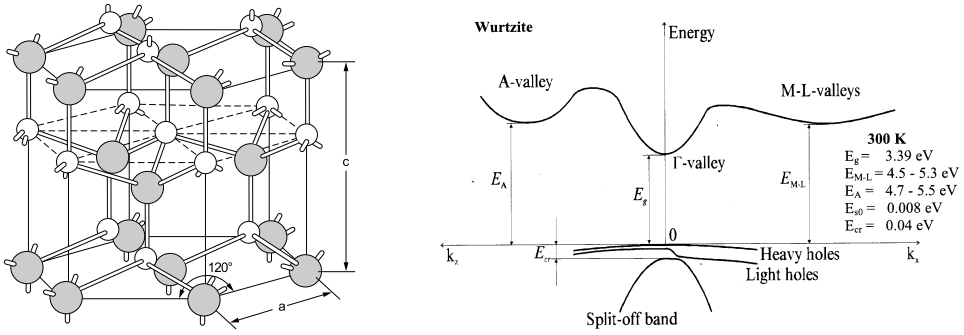


Figure 2.1: Cross-sectional diagram of an AlGaN/GaN HEMT (not in scale) [7].

2.1 The Gallium Nitride

The Gallium Nitride is a compound semiconductor formed by two elements from the 3^{rd} group (Ga) and the 5^{th} group (N) of the periodic table. It can be found in two different crystal structures: Wurtzite and Zincblende. Since Zincblende phase is not stable, only the Wurtzite phase is used for electronic devices. GaN is a direct band-gap material: the minimum of the conduction band correspond to the maximum of the valence band, which means that direct band-to-band transitions of carriers are possible by emission or absorption of light radiation; physical mechanism used in the realization of optical device. The energy band gap (E_g) at T = 300 K is 3.44 eV for Wurtzite phase. In Fig. 2.2a the crystal structure of the Wurzite lattice is shown, while Fig.2.2b shows the energy band for the Wurzite GaN phase.

Another property of GaN is the *spontaneous polarization* (P_{sp}): materials such as GaN, InN and AlN present a low-symmetry in their ground state. Spontaneous polarization is due to the asymmetry of the crystal structure (a difference in the bond



(a) Wurtzite lattice [8]. **(b)** Wurtzite energy band diagram.

Figure 2.2: GaN lattice in Wurzite-phase and related energy band diagram.

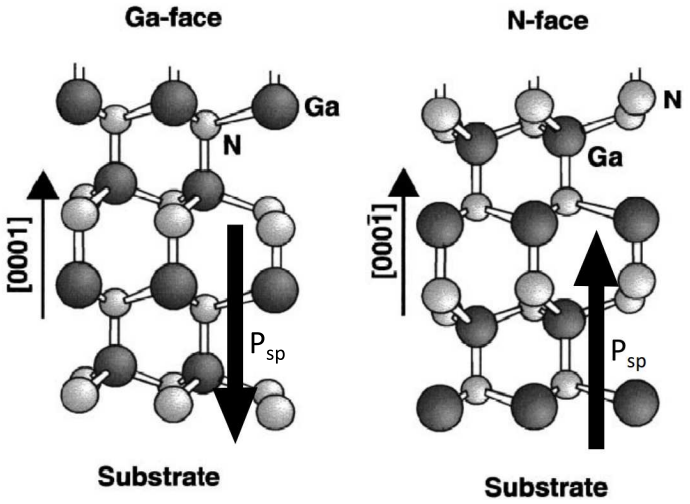


Figure 2.3: Ga-face and N-face in wurtzite structure GaN [9].

lengths) that causes a loss of balance in the distribution of the electric charge. For this reason the lattice exhibits a dipole moment and consequently a built-in polarization. The orientation of P_{sp} depends on the polarity of the GaN surface: if it is a Ga-face P_{sp} points to the substrate, else with a N-face it points in the opposite direction, see Fig. 2.3. As we will see later, the spontaneous polarization is a fundamental property for the realization of HEMTs on gallium Nitride.

2.2 The AlGaN/GaN Heterostructure

An heterostructure is formed when a semiconductor material is grown with epitaxial techniques on the top of another semiconductor material. The most common heterostructure is the AlGaAs/GaAs system; other types of structures have been studied, like InGaAs/InP, SiGe/Si and AlGaN/GaN.

The heterostructure bases its behavior on the difference between energy gaps (E_g) of the constituent semiconductors: when the heterostructure is formed, by means of epitaxial growth of a semiconductor on the top of another one, at the interface of the two material a discontinuity on the energetic bands is created. Also the differences in the lattice constants between the two materials must be taken into account. If the specific of the AlGaN/GaN heterostructure, when the AlGaN is grown on the top of the GaN layer, the AlGaN layer adopts in the growth process the lattice constant of the adjacent semiconductor. In order to accommodate the mismatch between the lattice constants, the thin AlGaN epitaxial layer becomes internally strained. This internal accommodation works only if the thickness of the strained AlGaN layer is below a

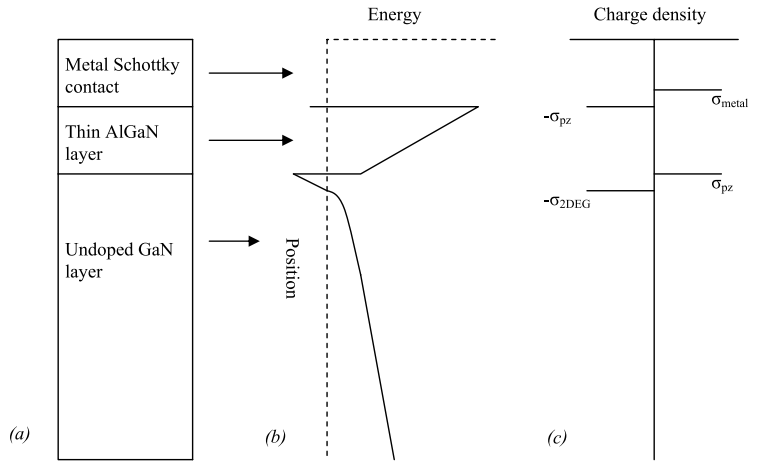


Figure 2.4: (a) Device structure; (b) energy band diagram; (c) charge density [10].

specific limit; above this limit the mismatch is accommodated by the formation of dislocations and defects at the interface.

Material such the AlGaN can show a strain-induced polarization field, a physical mechanism called *piezoelectric effect*. This polarization field is used to modify the electrical field and, consequently, the charge distribution inside the heterostructure without using doping. In fact, if we look to the simplified HEMT structure reported in Fig. 2.4, the AlGaN layer results strained on the top by a Schottky metal gate contact and on the bottom by the GaN buffer, the result is a strain-induced polarization field which creates, at both interfaces, a polarization charge density (σ_{pz}). Then σ_{pz} induces a compensating charge density at both interfaces: metal/AlGaN layer (σ_{metal}) and AlGaN/GaN layer (σ_{2DEG}). Notice that at this point the electron concentration in the GaN layer at the heterointerface is increased significantly without any doping. The negative charge accumulated at the interface (σ_{2DEG}) bends the energy bands creating a quantum well, see Fig. 2.4b. Since electrons in the quantum well are spatially confined, they induce the formation of energy subbands where they can move along two directions (the GaN surface), but not in the vertical direction; for this reason the charge at the interface is called *Two Dimensional Electron Gas* (2DEG).

Another phenomenon can be used to increase the carrier concentration at the heterointerface: the spontaneous polarization of GaN. As mentioned earlier, GaN presents a polarization which arises even in the absence of strain. To increase the 2DEG density the spontaneous polarization (P_{sp}) and the piezoelectric polarization (P_{pz}) must be aligned, in this way the total polarization (P) is the addition of the other two:

$$P = P_{pz} + P_{sp} \tag{2.1}$$

The P_{pz} orientation depends on the type of strain: in compressive-strain P_{pz} and P_{sp} are opposed, in tensile-strain they are aligned [9, 11].

At this point it is clear what is the advantage of a heterostructure: a conductive channel in a undoped semiconductor layer (the GaN buffer have been obtained, where the mobility is the same of the intrinsic material and there are no scattering phenomenons due to the introduction of impurities in the semiconductor.

As explained, the negative charge forming the 2DEG is attracted at the interface AlGaN/GaN by the polarization fields induced in the heterostructure. In [12] an hypotheses is proposed to explain where this charge comes from. In this work it is suggested that the surface states of the AlGaN layer are donor-like states; when the strain-induced polarization field is sufficiently high to alter the band profile and the charge distribution, the electrons are attracted from the surface to the AlGaN/GaN heterointerface forming the 2DEG. In figure 2.5 a schematic representation of band profiles is shown, in Fig. 2.5a the AlGaN layer thickness is less than the critical one (t_{CR}) for the formation of 2DEG and surface donor state are still full; when the layer thickness reaches and exceeds the critical thickness (Fig. 2.5b) the donor energy is over the Fermi level and electrons can migrate to the empty conduction band levels forming the electronic gas. The value of t_{CR} is calculated by the following formula [12]:

$$t_{CR} = \frac{(E_D - \Delta E_C)\,\epsilon}{q\sigma_{pz}} \tag{2.2}$$

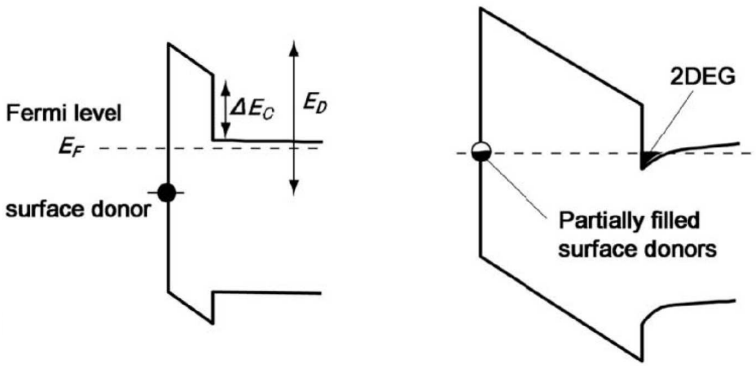
where E_D is the energy of the surface states, ΔE_C the AlGaN/GaN conduction band offset and ϵ the AlGaN relative dielectric constant.

The offset between the AlGaN and the GaN bands depends on the aluminum content in the AlGaN layer; in fact the aluminum percentage is the parameter that controls the energy band gap ($E_{gap-AlGaN}$) between valence (E_v) and conduction (E_c) band. An empirical expression is used to calculate the energy gap:

$$E_{gap-AlGaN} = xE_{gap(AlN)} + (1-x)\,E_{gap(GaN)} - bx\,(1-x) \tag{2.3}$$

where $E_{gap(AlN)} = 6.1\,\text{eV}$, $E_{gap(GaN)} = 3.4\,\text{eV}$, x the Al percentage and b the bowing parameter, which is usually considered equals to $1.0\,\text{eV}$ [13].

The 2DEG density (n_s) depends on the AlGaN layer thickness: the charge density increases with increasing the thickness over the critical value. In Fig. 2.6 n_s is plotted in relation with the AlGaN thickness (from [14]): for little increment of thickness the charge density increases fast, while for greater increments it tends to saturate to a constant value.



(a) AlGaN layer thickness less than critical thickness.

(b) AlGaN layer thickness greater than critical thickness.

Figure 2.5: Schematic representation of band profiles, E_D is the energy of the surface states and ΔE_C the AlGaN/GaN conduction band offset [12].

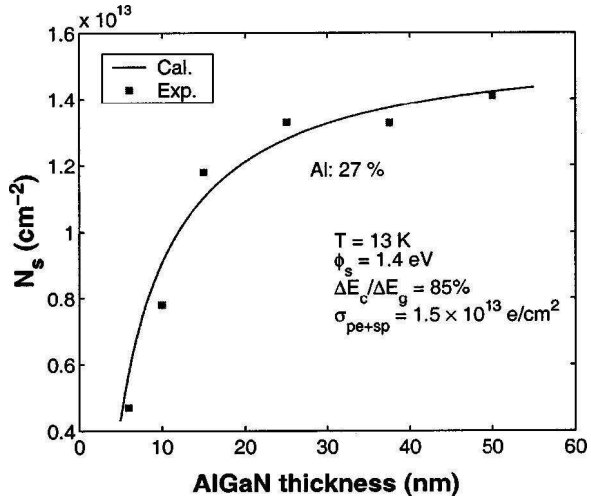


Figure 2.6: 2-D sheet charge density as a function of AlGaN thickness; points represent experimental data, line represents calculated values [14].

2.3 The Substrate

Since a specific technique to grow bulk GaN crystals does not exist; the realization of GaN-based devices requires the epitaxial growth of the GaN layer on a carrier substrate of different material. The three substrates are typically used for the growth of epitaxial GaN layers are sapphire (Al_2O_3), silicon carbide (SiC) and silicon (Si). New processes (HVPE-hydride vapor phase epitaxy and high-pressure growth) allow the realization of thick GaN layer that can be used without the carrier substrate; but the process still needs the presence of a initial substrate where it is possible to start the epitaxial

deposition.

For this reason the use of a nucleation layer (AlN or AlGaN) between the substrate and the GaN buffer is necessary in order to accommodate the mismatch between the two different crystal structures and to allow the growth of a high quality GaN-layer.

A brief description of each substrate used in GaN technology is presented in the following list.

- Sapphire: used to produce high resistivity, low cost, and large area substrate; the disadvantage is a poor thermal conductivity that easily induces the device self-heating, making the sapphire inappropriate for high power applications. Also, the GaN and sapphire have a ~15% lattice mismatch [15].

- Silicon Carbide: high thermal conductivity, low lattice mismatch with the GaN (3%). SiC substrates, unfortunately, has high realization costs, low controllability on resistivity and high dislocation density. Monocrystalline SiC wafers are commercially available with a maximum diameter of 3 inches: this means a less throughput of devices per wafer.

- Silicon: it has a very large lattice mismatch with GaN; but it is very cheap and growth processes are well know; second it is available in high quality and large diameter wafers. Finally Si-based and GaN-based devices can be realized on the same wafer.

In table 2.1 the main characteristics of the three substrates are reported.

Property	Unit	Al_2O_3	6H-SiC	Si
Simmetry	-	hexagonal	hexagonal	cubic
Lattice constant a	Å	4.765	3.08	5.431
Lattice constant c	Å	12.982	15.117	-
Thermal conductivity	W/cm K	0.25	3.8	1.56
Lattice mismatch with GaN	%	15	3.1	17

Table 2.1: Properties of the different substrates used for GaN epitaxy [15].

In recent years a new type of substrate, called hybrid substrate, have been studied as a possible alternative to the traditional substrate [16, 17]. These substrates are composed by a thick carrier substrate in poly-crystalline silicon carbide and a thin layer, called seed, of mono-crystalline material, which can be both silicon or silicon carbide. The two composite substrate are indicated as **SiCopSiC** (**SiC o**n **p**olycrystalline **SiC**)

and **SopSiC** (**S**i **o**n **p**olycrystalline **SiC**). The advantage in using the poly-crystalline SiC as carrier substrate is that the thermal conductivity is high(3 W/cm K), close to the one of mono-crystalline SiC (3.8 W/cm K), but it is less expensive and easy to produce. Below the different advantages of both composite substrate are listed:

- SiCopSiC: a single crystal SiC is used as the seed layer, therefore the wafer presents a high quality surface where GaN can be grown with small lattice mismatch and moreover the costs are improved thanks to the inexpensive substrate.
- SopSiC: Si as seed layer presents a large diameter substrate for realizing of GaN HEMT (4~6 inches) and the poly-SiC substrate provide a better thermal conductivity than bulk silicon.

The technique adopted to produce composite substrates derives from SMART-CUT^{TM} technology developed by SOITEC to fabricate SOI systems [18]: the two wafer, one in poly-SiC and the other one in Si or SiC, are bonded by the contact between the two oxidized surface. Then, by annealing process, the seed wafer, previously submitted to implantation of hydrogen ions, is split into two along the layer of micro-cavities formed by the ion implantation. Finally the top of the wafer (that could be a Si or SiC) is polished by a chemical-mechanical procedure to remove the surface roughness caused by the splitting. The residual of the seed wafer can be used for another process cycle.

2.4 Metal Contacts

In AlGaN/GaN transistors there are two kinds of metal-semiconductor junction: gate rectifying contact and source/drain ohmic contacts.

Rectifying contact

The gate is a rectifying contact formed by deposition of a metal layer on top of the AlGaN barrier. Metals with high work function (Φ_m) are generally used to provide a high junction barrier and, consequently, to reduce as much as possible the gate leakage current. Nichel (Ni - Φ_m=5.15 eV), platinum (Pl - Φ_m=5.65 eV) and palladium (Pd - Φ_m=5.12 eV) are generally used for gate contact. The metal contact is not formed by a single metal level: another level is used to provide more high conductivity, like aluminum or gold, in order to prevent the contact oxidation; also a titanium layer is often used between the two metal levels in order to increase the thermal stability of the contact [19].

Often the gate contact is realized in a trench formed by etching the barrier layer. This trench, indicated as *gate recess*, is usually few nanometers deep; transistors realized by means of this technique have shown a lower gate leakage current [20] and improved RF performances [21].

Ohmic contact

The ohmic contact in AlGaN/GaN HEMTs is generally realized by the deposition of a multi-layer structure with different metal; for example titanium (Ti), gold (Au), aluminum (Al), molybdenum (Mo) are often used for drain and source contacts. The deposition is then followed by a rapid thermal annealing, that create an alloy among the different materials and improve the contact conductivity. The bottom layer, the one that realizes the ohmic junction, is realized in Ti, which presents a low work function (Φ_m=4.3 eV). The mechanism of the contact formation is not clear yet, but it seems that the the presence of the titanium layer is fundamental, because it combines with nitrogen atoms crating a TiN layer which is in contact with the GaN-channel and allows the carriers passage [22, 23].

The use of a gold top layer is very common in order to obtain low contact resistance, [24, 25]; but it can represent an issue for the processing of transistors on large diameter GaN-on-Si wafer. In fact gold represents a contaminant element in Si-fabs; therefore 6-inch GaN wafer cannot be processed inside traditional silicon-processing lines. For this reason, the research is now focused on the study of new gold-free contacts in order to find a new technology compatible with silicon processing [26].

2.5 Trapping Effects

The presence of trapping states in an electronic device is a deleterious effect that can heavily affect its performances and electrical behavior. In fact, especially in transistors for RF-power amplification, traps can cause a variation on the number of free carriers in the device, with a consequently decrease on the output power and a possible distortion of the output signal. In AlGaN/GaN HEMTs the presence of traps can be related to various mechanisms: defects in the crystal lattice originated during the growth processes; mismatch between the surfaces of the heterostructure; surface damages due to process treatments; impurities incorporated in the crystalline structure during the processing. Traps can also be generated during particular stressing conditions of the device, like high electrical field and presence of high-energetic hot-electrons in the channel.

In Fig. 2.7 the schematic representation of an AlGaN/GaN HEMT cross section is presented where the possible locations of trap levels are indicated. In the follows we describe two of the most common and widely studied trap-related issues on GaN-based HEMTs: the *current collapse* and the *kink effect*.

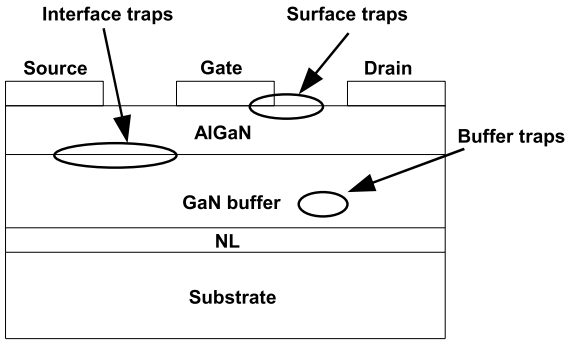


Figure 2.7: Trapping-state in the AlGaN/GaN HEMT.

2.5.1 Current Collapse

The current collapse effect indicates a specific behavior of a transistor when it is biased in a certain working point and a RF signal is applied to the gate: in presence of this effects the drain current is lower then the expected value from the DC characteristics of the sample. Moreover the decrease of the drain current leads to a decrease of the output power and of the power added efficiency (PAE).

The origins of the current collapse has been indicated in the presence of slow surface state that can catch carries inducing a variation of the charge in the GaN-channel [27]. The collapse can be easily detect by comparing the $I_D - V_{DS}$ measurements carried out in DC state with those obtained by applying a brief voltage pulse that switches the device from OFF-state condition to ON-state conditions, see Fig. 2.8.

When the transistor is biased in pinch-off, the surface traps capture electrons from the gate electrode, which is biased at negative values; thus the donor-like surface states become neutral, causing a variation on the charge balancing in the entire heterostructure. Since the 2DEG results unbalanced, the conductive channel goes through an extension of the depleted region outside the area covered by the gate, see Fig. 2.9.
If the turning-ON gate pulse is sufficiently short, the slow surface traps do not release the trapped charge behaving like a *virtual gate*, which keeps the channel partially turned-OFF [27, 28]. In this way the channel resistance remains high and the drain current experiences a decrease (the "*collapse*").

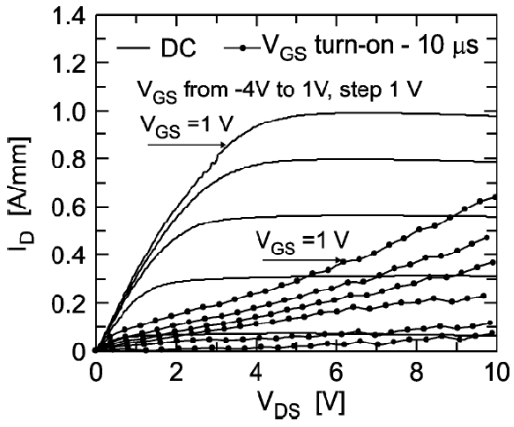
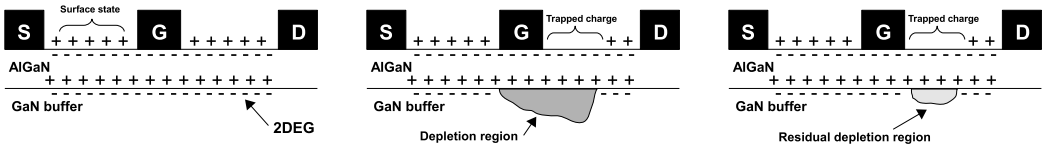


Figure 2.8: Comparison between DC and pulsed $I_D - V_{DS}$ characterization of a AlGaN/GaN HEMT showing current collapse.



(a) (b) (c)

Figure 2.9: Schematic representation of current collapse. (a) On-state: surface donors are positively charged. (b) Off-state: surface donors are electrically neutral because they have captured electrons. (c) On-state: the captured electrons are still causing a persistence of the depletion region [7].

Two main techniques are used in order to reduce the current collapse: the surface passivation and the engineered design of the gate electrode. The passivation is a layer of a dielectric material, generally silicon nitride (Si_3N_4), that covers the surface states and prevents electrons to be caught by traps. On the other hand, the gate electrode can be designed in complex configuration in order to redistribute the electric field between gate and drain. Common gate shapes are the T-gate and the Γ-gate: both of them consist in an extension of the upper part of the gate over the near gate-source and/or gate-drain regions. The purpose of these configurations, that take the name of *field plates*, is to decrease to peak of the electrical field at the edge of the gate especially when drain and gate are biased at high voltage and the transistor is in OFF-condition, therefore the resulting electric field is lower and a smaller quantities of electrons are attracted from the surface states [29]. Also more complex field-plate structures are realized to improve the radio-frequency device performance, like metallic shield that cover the drain-gate region connected to the source but isolated from the gate [2].

2.5.2 Kink Effect

The kink effect a is sudden increase of the drain current that happens at a specific drain voltage ($V_{DS-kink}$), see Fig. 2.10; it also provokes a increase of the output conductance (g_{DS}). This effect is usually related to the presence of slow traps in the AlGaN barrier or in the GaN buffer [30, 31]: in fact an easy way to detect the presence of the kink effect is to carry out simple DC measurements adopting different integration time. In Fig. 2.10 two $I_D - V_{DS}$ characterizations made with different integration time are compared: when fast measurements are carried out, carriers are not trapped in the device and the drain current does not show any abnormal behavior (continuous line in the graph). On the other hand, with slow measurements, trap can capture carriers during the first part of the $I_D - V_{DS}$ characterization; these carriers are then released after the overcoming of a certain V_{DS} value (dashed line in the graph).

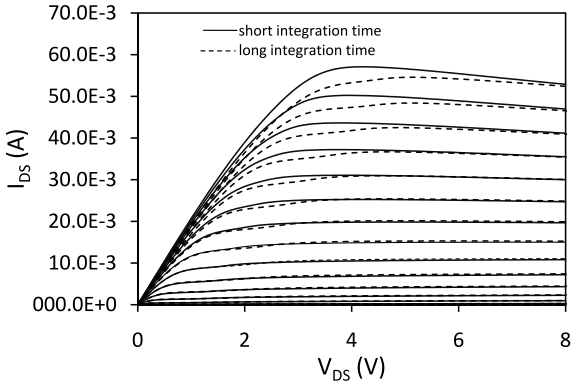


Figure 2.10: $I_D - V_{DS}$ DC characterization of a AlGaN/GaN HEMT carried out with two different integration time: continuous line = short integration time; dashed line = long integration time. V_{GS} from 0 V to −4 V, step −0.2 V.

Despite the kink effect has been found and studied in transistors processed on different semiconductors (such as SOI, AlGaS/GaS and AlGaN/GaN), a real explanation of its origin is not available yet. As explained in [32], the possible origins can be *i*) accumulation of holes, created by channel impact ionizations, with consequently change in the channel potential; *ii*) trapping-detrapping phenomenons which involve deep-level traps; *iii*) a combination of effect *i* and *ii*. While the probability of impact ionization is higher in narrow-band semiconductors and it can be used to explain the kink effect in SOI and AlGaS/GaS device; in AlGaN/GaN transistors the impact-ionization has not been clearly proved yet. On the other hand, in GaN HEMTs the kink has shown dependence on illumination and temperature; suggesting a relation with the presence of traps in the buffer or in the barrier layer below the gate electrode [30, 31].

2.6 GaN HEMT Reliability

The reliability of AlGaN/GaN transistors is a crucial aspect for the use of this technology in the field of the high power density devices and high efficiency amplifiers. In fact GaN-based device are expected to work at high current and high voltage bias; a not-well established technology, from the reliability point of view, is useless for all the possible applications. For this reason, the studies on ageing effects and failures are very important for the complete characterization of a new type of devices.

In GaN HEMTs several degradation effects have been found and studied; in the follows the main mechanisms are reported with a brief explanation.

- Degradation of ohmic and Schottky contacts.
  Metal contacts on HEMTs are generally studied by thermal-storage tests; in this type of experiments the main degradation mechanism consists in the inter-diffusion of the metallic elements from the electrode to the semiconductor material, here these elements combine with the atoms of the semiconductor lattice creating inter-metallic compounds. In [33], the diffusion of Au-atoms from the ohmic contacts to the semiconductor and also the diffusion of Ga-atoms from the semiconductor to the contacts are indicated as the main degradation mechanisms which leads to the increase of the contact resistance and the formation of surface bubbles and crack in the passivation layer. On the other hand, gate Schottky contact are reported to be generally stable if submitted to thermal-storage [34]; but more studies in this field are certainly required.

- Hot-electron induced damages.
  Degradation in GaN HEMTs has been also related to failure mechanisms induced by the presence of hot-electrons. When a transistor is biased in on-state condition at high drain-source voltages, the electrons in the channel are accelerated by the high electrical field, acquiring energies greater than the equilibrium value. In this way the carriers becomes "hot": they can overcome the energy barriers and they can collide with the crystalline structure loosing energy; collisions can generate defects or damage the lattice bonds inducing the creation of traps and deep states [35]. Moreover the energy released by hot-electrons can promote relaxation on the strained AlGaN layer [36]. In AlGaAs/GaAs HEMTs the presence of hot-electrons is usually detected by measuring the gate current generated by impact-ionization [37]; since impact-ionization in GaN-based transistors is negligible and the gate current is dominated by tunneling mechanisms,

the measurement of electroluminescence is used as an alternative methodology to study the hot-carriers in GaN-HEMTs and their dependence on the applied bias. In section 3.3.3 a description of this methodology based on electroluminescence measurement is reported.

- Gate reverse-bias induced damage.
  Several authors have identified a specific failure of the device when it is subjected to an off-state accelerated life test with negligible channel current. The degradation observed consists in a drastic increase of the gate leakage current, traps generation and charge trapping, with consequent decrease in I_{DSat}, g_m, and increase in the access region resistance (e.g. R_D and R_S). A specific hypothesis has been formulated by Joh and Del Alamo in order to explain this phenomena [38, 39]: the applied electric field in the gate-drain region increases the strain in the AlGaN/GaN heterojunction (*inverse piezoelectric effect*) eventually resulting in strain relaxation and crystallographic defect formation. This would compromise carrier transport properties and electron concentration in the access region, thus increasing R_D and reducing g_m; gate leakage current is then increased due to the higher trap-assisted tunneling phenomena in the AlGaN. This hypothesis also predict that the inverse piezoelectric effect occurs at a specific critical gate voltage, indicated as V_{critic} (see Fig. 2.11).

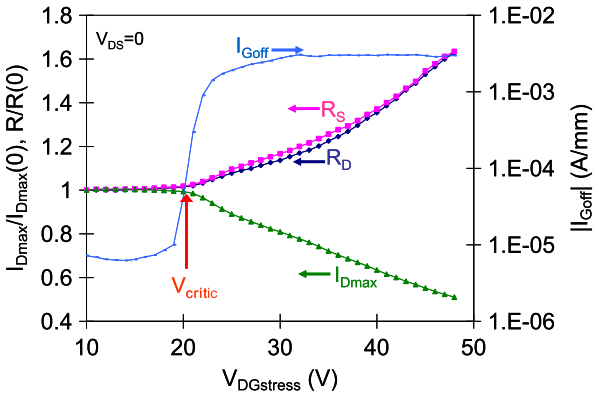


Figure 2.11: Typical results of a reverse-bias step-stress from [39]. It is possible to see the changes on I_{Dmax}, R_D and R_S, while the sudden increase of the gate leakage defines the critical voltage.

On the other hand other authors [40, 41] ascribe this type degradation effects to the presence of pre-existing defects that can enhance the gate leakage current. In recent studies [42, 43], the same degradation effects have been measured after a stress carried out at constant gate bias lower than the $|V_{critic}|$ measured with the

same technique proposed by Joh *et al.* [38]. The authors of [42, 43] propose the existence of a *time-to-breakdown*, which depends on the applied voltage, and they ascribe the degradation of the device to the generation of defects along the gate edge, then followed by the percolation of a growing number of defects through the AlGaN layer, resulting in a low-resistance current path.

From this brief exposition, it is clear that the reliability of GaN-based HEMTs is still to be completely explained and more efforts are needed in order to improve this technology and make it available for the market demand.

3

Trapping and Hot-Electron Effects Investigation

As explained in Section 2.5, the presence of traps is a serious issue that can compromise the high performances of GaN-based HEMT. In this chapter we present a methodology for a rapid evaluation of the trapping and hot-electron-related characteristics of GaN-based HEMTs. The proposed method is based on combined electrical and optical measurements and it directly provides the following information:

1. presence of traps in the region under the gate;
2. characterization of the effects of traps located in the gate-drain access regions;
3. effect of traps on the electric field and equivalent electron temperature.

With a limited measurement overhead, the proposed method provides a first rapid evaluation of the effects and location of traps in AlGaN/GaN HEMTs. This methodology can be easily integrated in a standard characterization setup and can be used for the validation and comparison of different growth and processing procedures.

3.1 The Combined Electro-Optical Method

Trapping effect analysis is generally based on the measurement of the basic electrical quantities (current and voltage) in different conditions; in the follows a brief description is given for the most widely used techniques for the characterization of trapping phenomena.

1. Capacitance Deep-Level Transient Spectroscopy (C-DLTS), based on the analysis of the gate capacitance transient induced by a steep voltage variation. This technique provides information on the properties of the traps located under the gate of the transistors. The main disadvantage of C-DLTS is that it cannot be used when the gate area of the devices is too small for standard capacitance measurements.

2. Drain-current deep-level transient spectroscopy (I-DLTS, [44]), which is based on the analysis of drain current transients as a function of the channel temperature. This technique can provide very accurate information on the activation energy and cross section of the trap levels that limit the performance of GaN-based transistors.

3. Gate-lag and drain-lag measurements [45], based on the analysis of the delayed response of the drain current to a gate or drain voltage variation. Results of gate-drain lag measurements can provide information on the time constants of trapping phenomena and can be effectively interpreted by means of device simulation.

4. Double-pulse measurements [46, 34]: this technique is based on pulsed $I_D - V_{DS}$ measurements, which are carried out by synchronously pulsing the gate and drain voltage of the transistors. By double-pulse measurements, it is possible to quantitatively evaluate the current collapse in HEMT devices and to compare different devices in terms of charge trapping.

5. Current-transient multiexponential analysis [47], based on the study of the time constant spectrum of the variation of drain current induced by a gate-voltage pulse. This effective technique provides information on the cross section and activation energy of trap levels responsible for current collapse: however, as in the case of DLTS, measurements must be carried out at different temperature levels, and this can result in quite long measuring times.

The techniques previously listed provide information on the energetic levels of traps responsible for current collapse. By coupling the results with 2-D device simulations, one can get insight into trap nature and localization. However, those techniques can be time consuming and therefore not suitable for rapid characterization of GaN-based HEMTs, or for diagnostic evaluation of devices submitted to reliability tests. Faster methods, which are capable of providing a quick characterization of the localization and effect of traps in a HEMT structure, must be developed in order to be able to compare different manufacturing processes in terms of amount and position of traps.

Furthermore high electric fields may limit the reliability of GaN HEMTs, due to the generation of traps or lattice defects induced by hot electrons [34]. For the validation of a specific device technology and for the prediction of its reliability, it is therefore necessary to evaluate the amount and equivalent temperature of hot-electrons under nominal operating conditions. However, electric field (and the equivalent temperature of hot electrons) cannot be directly measured: indirect methods, including electroluminescence (EL) characterization, must be adopted.

Trapping effects and hot-electron-induced phenomena are two of the most relevant mechanisms that may affect GaN-HEMT performance and reliability. They are strictly correlated since trapped charge influences the electric field, whereas hot electrons may enhance trapping and/or generate new traps. This is the most important motivation for presenting two experimental techniques that, when correlated, can characterize both phenomena in a simple way, within the same device.

3.2 Experimental Setup

The proposed method for the evaluation of trapping effects is based on pulsed transconductance measurements [48]. In the developed setup, the transistor is connected in class-A amplifier configuration with a 50 Ω resistive load (R_{LOAD}), in Fig. 3.1 the measurement setup is shown. Drain current measurement is obtained by measuring the voltage across the drain load resistance by means of an oscilloscope (a Tektronix TD654C). Measurements are carried out, starting from an arbitrary quiescent bias point where V_{GS} and V_{DS} are chosen in order to induce or avoid trapping of carrier in the sample; then, gate and drain voltages are synchronously pulsed to different values in order to obtain the $I_D - V_{DS}$ output characteristic and the $I_D - V_{GS}$ transfer-characteristic. The gate signal (V_{GS}) is supplied by a HP8110A pulser, this signal is also used as trigger input for the other pulser and for the oscilloscope allowing the synchronization among instruments. The pulsed drain voltage (V_{DD}) is supplied by the HP8114 pulser. The oscilloscope measures V_{GS}, V_{DD} and V_{DS}, from this last measure we obtain the voltage across the resistance (V_{LOAD}) and the drain current (I_D). Ten consecutive current pulses are averaged for each measured point, adopting a 1 µs "working-state" pulse, followed by a 99 µs "quiescent-state" pulse (1% duty cycle) at the bias point V_{G-qb}, V_{D-qb}. The quiescent bias points adopted for the pulsed transconductance measurements are

- (V_{G-qb}, V_{D-qb})=(0 V, 0 V) characterized by negligible electron trapping;

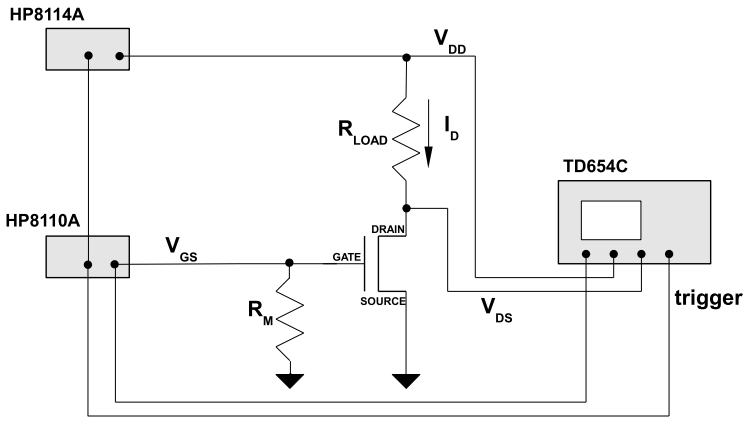


Figure 3.1: Double-pulse measurement setup. R_M is a resistance of 50 Ω used for matching the HP8110A pulser output [7].

- (V_{G-qb}, V_{D-qb})=(-4 V, 0 V), where both gate-source and gate-drain junctions are slightly reverse biased (gate-lag);
- (V_{G-qb}, V_{D-qb})=(-4 V, 10 V), where high gate-to-drain reverse bias is applied, leading to significant charge trapping at the gate-drain edge (drain-lag).

Hot electron effects are evaluated by means of EL measurements, which are carried out at different gate and drain voltage levels. EL data were acquired by means of a LUCA EMCCD (*Electron Multiplying CCD*) camera, produced by *Andor Technology*. This camera, thanks to the Electron Multiplying technology, is characterized by a very high sensitivity; moreover during the measure it is kept to −20°C to reduce the background noise. The camera is equipped with a CRI VARISPEC filter-based monochromator that is mounted on an optical microscope, the monochromator allows a spectral resolution up to 1 nm. The radiometry calibration of the whole system was carried out in the 420 – 720 nm spectral region by means of a halogen light source with known spectrum.

3.3 UCSB sample

For validating the proposed method, a specific split-wafer has been designed, in collaboration with the University of Santa Barbara - California: the sample is a GaN-HEMT wafer grown by metalorganic chemical vapor deposition on semi-insulating SiC, with the epitaxial structure described in Fig. 3.2. The gate trench has been formed by fluorine plasma etching (5 nm gate recess). The wafer has been split into two parts:

one has been processed with Ni/Au/Ni (30/250/30 nm) gates and one part has been processed with ITO (250 nm) transparent gates, as described in Fig. 3.2. Part of the wafer has been kept unpassivated, with the aim of studying the influence of surface traps on pulsed and EL measurements. Ti/Al/Ni/Au stacks have been used as the ohmic contacts and annealed at 870°C in a N_2 atmosphere [49].

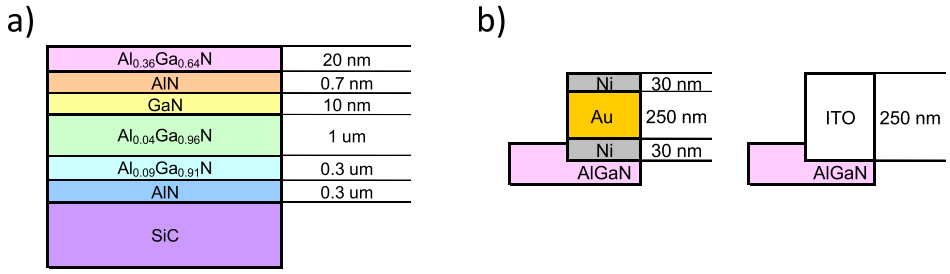


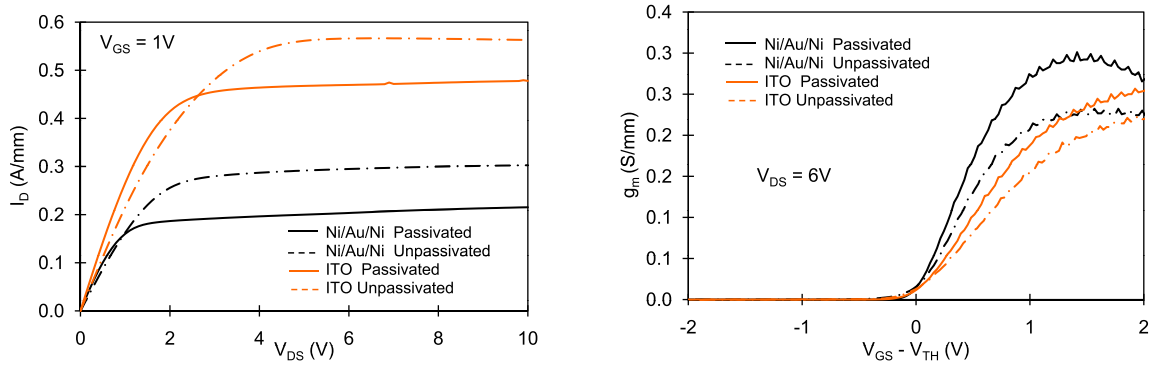
Figure 3.2: (a) Epi-layer description of the tested wafer. (b) Schematic structure of the Ni/Au/Ni and ITO-gate stacks.

3.3.1 DC Characterization

In Figure 3.3 we report the DC characteristics of representative samples from the four series: unpassivated samples show an higher on-resistance (Fig. 3.3a) and a lower transconductance peak (Fig. 3.3b), due to charge trapping in the access regions, that can determine a worsening of the static characteristics of the devices. The difference in the drain current (Fig. 3.3a) is related to the different threshold voltages (V_{TH}) that has been measured among the samples: ITO samples are characterized by more negative values of V_{TH} than Ni/Au/Ni samples; while passivation for both the two kinds of gate material moves the threshold voltage to higher values, leading to a lower I_D at the same gate bias.

3.3.2 Pulsed Transconductance Measurements

Pulsed measurements are widely used for detecting the presence of traps in HEMTs [46, 34]. In single-pulse systems, either the gate (gate-lag) or the drain (drain-lag) is pulsed, keeping the other terminals at a fixed voltage and applying a suitable load at the drain. As previously explained, in double-pulse systems the device is biased at an arbitrary quiescent bias point; then gate and drain voltages are synchronously pulsed to different values in on-state. Double pulse system allows one to define the quiescent bias point independently from the pulsed-state one. By repeating the pulsed measurement for different drain and gate values, pulsed $I-V$ device characteristic can be obtained.



(a) $I_D - V_{DS}$ at $V_{GS} = 1\,\mathrm{V}$ **(b)** $g_m - V_{GS}$ at $V_{DS} = 6\,\mathrm{V}$

Figure 3.3: Comparison among the DC characteristics of four representative samples studied in this work, one for each type available.

When a high reverse bias is applied to the gate-drain junction during the quiescent state, the high electrical field enhance the electron trapping, then a remarkable current collapse can be observed. Pulsed drain current vs. drain voltage output characteristics are usually measured and the current collapse is evaluated by comparing the values of the drain current measured using a high-reverse-bias quiescent-point, with those corresponding to a zero-bias quiescent-point that induce no trapping.

An example of the information that can be obtained from this kind of technique is reported in Fig. 3.4 where the pulse $I_D - V_{DS}$ curves of one of the analyzed HEMTs are shown, the quiescent bias points used in this measurement are (V_{G-qb}, V_{D-qb})=(0 V, 0 V), (−4 V, 0 V)) and (−4 V, 10 V). As can be noticed, the application of a quiescent bias can induce significant trapping, which may interest both the region under the gate, particularly for the (−4 V, 0 V) bias point, and the gate-drain access regions (for the quiescent bias point with a significant gate-drain voltage difference). Trapping can result in the increase in the dynamic ON-resistance of the devices and in the decrease in the maximum drain current.

Even if pulsed $I_D - V_{DS}$ measurements allow to detect and characterize current collapse, this type of measurement does not allow to obtain direct information on the location of traps in a HEMT structure. In order to achieve more accurate information on the location of traps, the pulsed transfer characteristic (I_D–V_{GS}) has been measured. Transconductance $g_m - V_{GS}$ curves were obtained by carrying out the derivative of the I_D–V_{GS} curves with respect to V_{GS}. Fig. 3.5a shows the g_m–V_{GS} pulsed characteristics of an unpassivated ITO-gate sample. Several features can be noticed by comparing the results obtained using the reference (0 V, 0 V) baseline with the others:

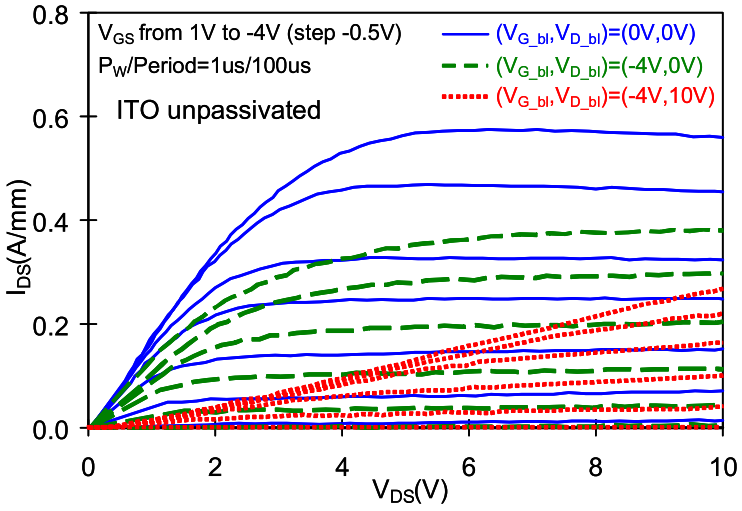
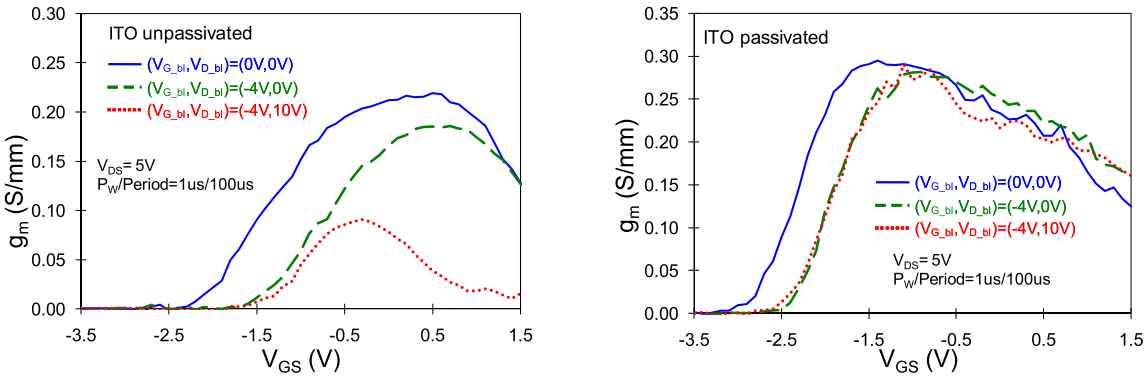


Figure 3.4: Pulsed I_D – V_{DS} characteristics of an unpassivated ITO-gate sample. Adopted quiescent bias point are indicated in the diagram.



(a) Unpassivated ITO-gate sample

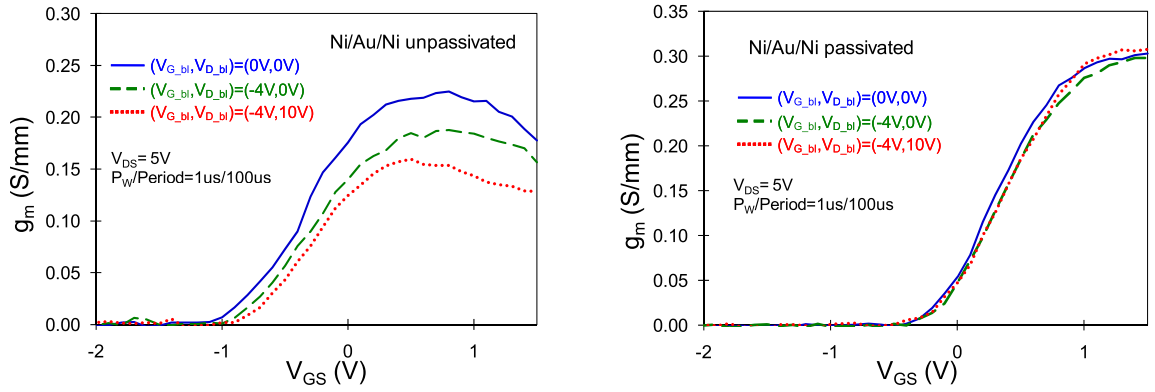
(b) Passivated ITO-gate sample

Figure 3.5: Pulsed g_m – V_{GS} characteristics at V_{DS} = 0 V of an unpassivated and a passivated ITO-gate sample. Adopted quiescent bias point are indicated in the diagram.

1. both the (−4 V, 0 V) and the (−4 V, 10 V) baselines induce a significant dynamic decrease in the absolute value of the pinch-off voltage (the curves are shifted to the left), corresponding to a reduced I_D and g_m for a given V_{GS};

2. the (−4 V, 0 V) and (−4 V, 10 V) baselines can determine a significant decrease in the transconductance peak, $g_{m_{peak}}$; this effect is more severe for the more negative gate-to-drain voltage adopted in the baseline;

3. when the (−4 V, 10 V) baseline is applied, g_m largely drops for V_{GS} approaching the positive bias.



(a) Unpassivated Ni/Au/Ni-gate sample **(b)** Passivated Ni/Au/Ni-gate sample

Figure 3.6: Pulsed $g_m - V_{GS}$ characteristics $V_{DS} = 0\,\mathrm{V}$ of an unpassivated and a passivated Ni/Au/Ni-gate sample. Adopted quiescent bias point are indicated in the diagram.

These results are then compared with the corresponding ones for a passivated ITO-gate device, Fig. 3.5b. The presence of passivation does not improve the threshold voltage shift, which remains almost unchanged; on the contrary, the dispersion of transconductance and its decrease at high V_{GS} values disappeared in passivated samples.

In unpassivated Ni/Au/Ni gate devices, a decrease in the peak transconductance value similar to the one seen on unpassivated ITO samples has been detected, as shown in Fig. 3.6a, and a sharp decrease in g_m at high V_{GS}, without any pinch-off voltage shift. Finally, no dispersion of the threshold voltage or of the transconductance maximum value is observed in passivated Ni/Au/Ni gate devices, see Fig. 3.6a.

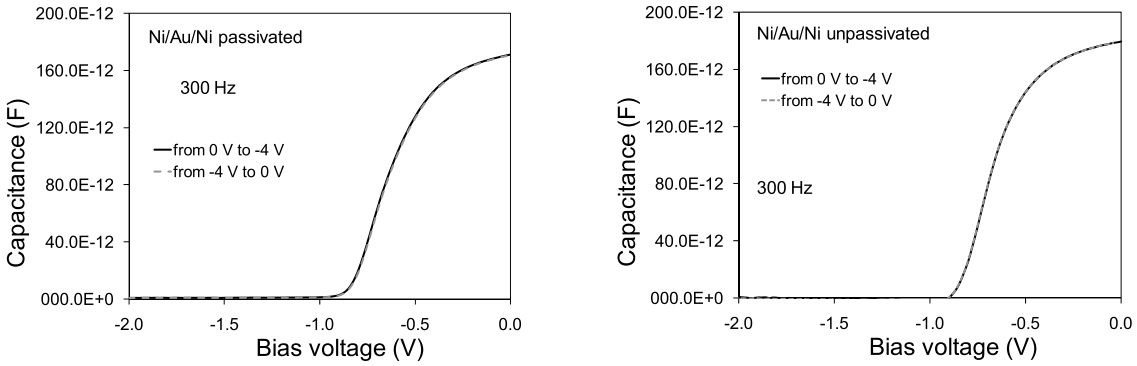
In Table 3.1 we give a summary of the results of the $g_m - V_{GS}$ measurements carried out on the different sets of analyzed samples.

At this point it is possible to give a first explanation of the observed phenomenon: surface states, present in both ITO and Ni/An/Ni unpassivated samples, lead to a decrease of the g_m peak; while the threshold voltage shift is related to another kind of traps that are not present on Ni/Au/Ni samples and are not neutralized by the passivation layer.

In order to evaluate the presence of traps or interface states within the tested structures, we carried out low-frequency $C - V$ measurements on large area (100 µm of diameter) Schottky diodes having the same metalization schemes as the gate of HEMTs. Both passivated and unpassivated Ni/Au/Ni sample did not show any hysteresis of the $C - V$ curves, see Fig. 3.7; on the contrary, on ITO-gate samples hysteresis effects have been detected with a threshold voltage shift comparable to the pinch-off voltage shift

	Shift of pinch-off	g_m peak decrease	g_m drop at high V_{GS}
ITO gate, not passivated	YES	YES	YES
ITO gate, passivated	YES	NO	NO
Ni/Au/Ni gate, not passivated	NO	YES	YES
Ni/Au/Ni gate, passivated	NO	NO	NO

Table 3.1: Summary of the results of the pulsed $g_m - V_{GS}$ measurements carried out on the four sets of analyzed devices.



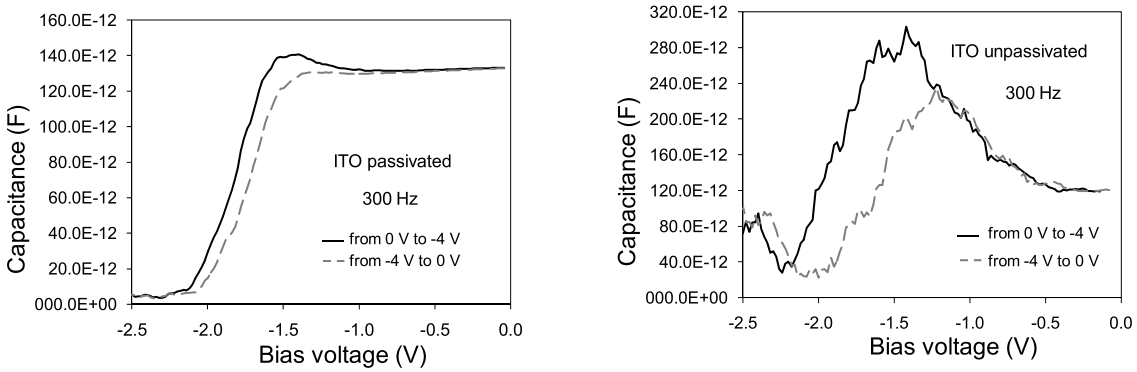
(a) Passivated Ni/Au/Ni-gate sample

(b) Unpassivated Ni/Au/Ni-gate sample

Figure 3.7: $C - V$ measurements for a passivated and unpassivated Ni/Au/Ni sample. Anode voltage is swept from 0 V to −4 V (solid line) and from −4 V to 0 V (dashed line). Modulation signal is at 300 Hz.

observed in pulsed $g_m - V_{GS}$ measurements (Fig. 3.8). This result is a confirmation of the presence of traps at the interface between the ITO layer and the semiconductor material: in fact, the hysteresis of the $C-V$ curves is usually attributed to the tunneling of electrons from the gate of the devices, due to the negative voltage applied during the execution of $C - V$ measurements [50]. Moreover, $C - V$ curves appeared to be light-sensitive: by illuminating the transparent-gate Schottky diode with monochromatic blue light (458nm), the shift in pinch-off was partially recovered (Fig. 3.9), due to photo-activated trapping/detrapping of the traps under the gate [51].

Now, with the results of the $C - V$ measurements, it is possible to better interpret the results obtained from the pulsed-transconductance measurements. In unpassivated devices (both ITO-gate and Ni/Au/Ni), significant electron trapping takes place on the surface of the access regions, due to the trapping of electrons in the region between the gate and drain, which is activated by high gate-drain voltage differences [52]. This phenomenon leads to the "virtual gate" [27] effect which mostly affects transconductance at high gate voltages, leading to a decrease in the drain current, and to the observed



(a) Passivated ITO-gate sample

(b) Unpassivated ITO-gate sample

Figure 3.8: $C-V$ measurements for a passivated and unpassivated ITO sample. Anode voltage is swept from 0 V to −4 V (solid line) and from −4 : V to 0 V (dashed line). Modulation signal is at 300 Hz.

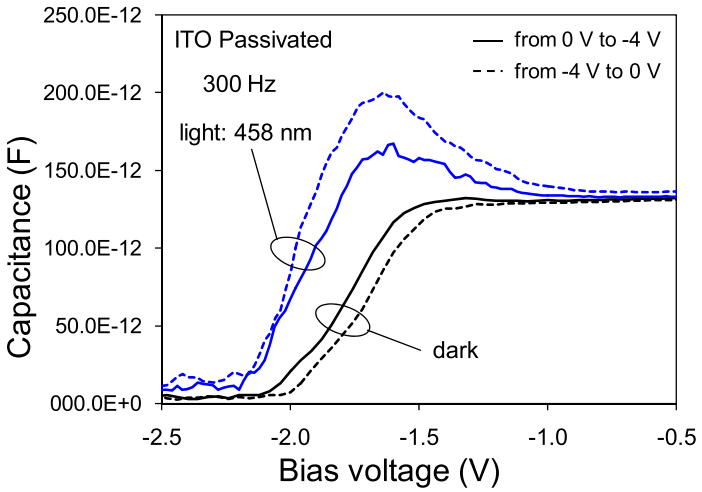


Figure 3.9: $C-V$ measurements for a representative ITO passivated diode in dark and with light illumination (458 nm). Anode voltage is swept from 0 V to −4 V (solid line) and from −4 V to 0 V (dashed line). Modulation signal frequency is 300 Hz.

decrease in g_m, see Figures 3.5a and 3.6a. This effect influences the series resistances in source and drain access regions, and is not present in passivated samples, since for these devices surface traps are neutralized by the passivation layer. In addition, devices with ITO-gate have shown a dispersion of pinch-off voltage (V_{TH}) for negative gate baselines, resulting in a lower value of $|V_{TH}|$ and, consequently, a reduced drain current when pulsed characterization is carried out, see Fig. 3.5. This effect is due to the presence of traps at the interface between the ITO and the AlGaN layer: these

traps can effectively change the pinch-off voltage of the samples, once they are charged by a negative gate-drain baseline pulse. Finally, to avoid trapping under the gate, it is necessary to improve the gate processing conditions, thus eliminating the presence of interface states. Measurement results indicate that transistors with Ni/Au/Ni gate do not show any evidence for trapping under the gate, as shown by the pulsed transconductance measurements in Fig. 3.6, and do not suffer from hysteresis in $C-V$ curves (Fig. 3.7). The only type of traps that affect the Ni/Au/Ni samples are in the surface for the unpassivated devices (see Fig. 3.6a).

3.3.3 Spatially and Spectrally Resolved EL Measurements

The second step to validate a device technology is to carry out some analysis which can give an idea on the reliability issues that one could encounter on samples realized with the selected technology. Optical measurements of device electroluminescence are a useful methodology to obtain information that concern the reliability: in fact, the intensity and spectral properties of the EL signal are directly related to the amount and energetic distribution of hot electrons that can be responsible for the degradation of HEMTs [34, 53, 54]. The description of a complete electroluminescence (EL) characterization of GaN-based HEMTs is presented in the follows, with particular attention to the evaluation of hot-electron effects.

The electroluminescence in GaN-HEMTs comes from the deceleration of carriers accelerated by the gate-drain electric field (*Bremsstrahlung* effect): hot-electrons in the channel lose the energy acquired from the applied electrical field during intraband transitions [55, 54]. This energy is then emitted by the transistor as a weak luminescence signal. If the light emission is sufficiently high, it is possible to measure it by counting the number of emitted photons and their spectral density. This information makes the evaluation of the electrical field intensity and of the presence of hot-electrons possible.

Fig. 3.10 shows the variation of the intensity of the EL signal on the gate voltage for different drain voltage levels. As can be noticed, the EL - V_G curve has a "bell-shaped" behavior, which can be explained by considering that EL intensity depends both on the amount of electrons in the channel and on the intensity of the accelerating electrical field. When the gate is increased to higher values beyond the pinch-off, the concentration of electrons in the channel (and the drain current) increases, thus leading to more scattering phenomenas and intraband transitions; which enhance the emission of photons. On the other hand, as the gate voltage is increased (beyond $0.8-1$V for the

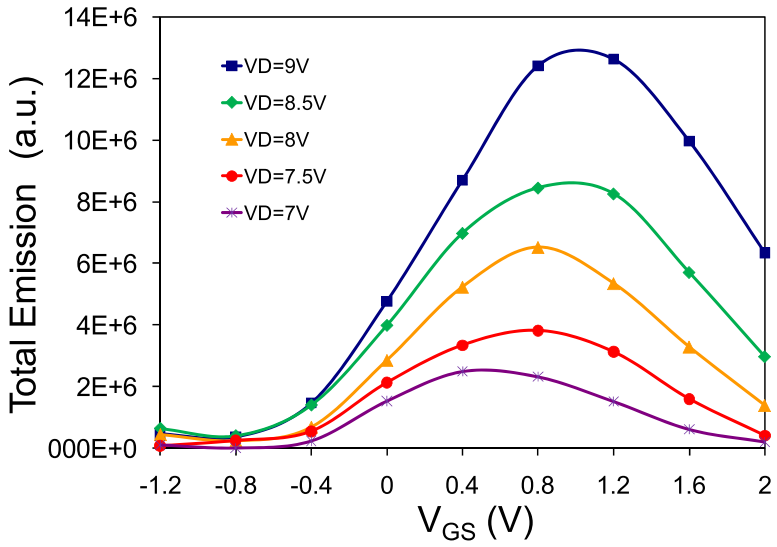


Figure 3.10: Intensity of the EL signal as a function of gate and drain voltage level on a ITO-gate sample with L_{GD} = 5 µm and W_G = 100 µm.

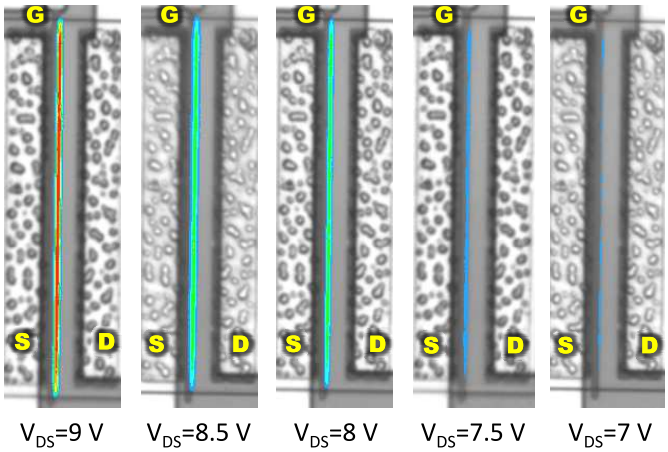


Figure 3.11: False color image reporting the distribution of EL along the gate at V_{GS} = 0.8 V and different V_{DS}.

samples under analysis), the gate-to-drain electric field decreases: electrons therefore become less energetic, and the intensity of the luminescence signal decreases.

The EL signal is maximum at the edge of the gate toward the drain, where the electric field peaks [56], as indicated by the emission images reported in Fig. 3.11.

The EL measurement is a quite important technique, since it allows the characterization of hot-electrons in GaN-base device. In fact, in the GaAs-based HEMTs, hot-electron effects are usually characterized by evaluating the device gate current I_G due to the collection of holes generated by impact ionization; technique not applicable to the GaN HEMTs, since the impact ionization is negligible in this kind of devices.

The impact-ionization in GaAs HEMTs arises only in presence of highly energetic electrons, the measurement of I_G in those devices allows one to reliably evaluate hot-electron effects [53]. In GaAs device it has been found that the $|I_G|/I_D$ ratio follows this empirical dependence (Chynoweth's law):

$$|I_G|/I_D \approx L_{eff} \exp(-1/E) \tag{3.1}$$

where L_{eff} is the effective length of the high field region and E the electrical field [34]. E is estimated as $E = (V_{DS} - V_{Dsat})/L_{eff}$, where V_{Dsat} is the saturation voltage. Thus the final expression for $|I_G|/I_D$ is

$$|I_G|/I_D \approx L_{eff} \exp(-L_{eff}/(V_{DS} - V_{Dsat})) \tag{3.2}$$

that means a straight line if $|I_G|/I_D$ is plotted versus $1/(V_{DS} - V_{Dsat})$ in a semilogarithmic diagram. It has been found that the same law can be applied to the EL/I_D ratio of GaAs devices [57] and of GaN devices (as reported in Fig. 3.12). For this reason, EL characterization is considered as a powerful tool for the investigation of hot-electron effects in GaN-HEMTs [57, 55], where other methodologies based on the evaluation of impact-ionization are not possible. Therefore from the count of emitted photons and from their spectral distribution, it is possible to extrapolate information about the energy distribution and the equivalent temperature of hot electrons in the sample. As shown in Fig. 3.13, the EL signal emitted by the devices has a Maxwell-Boltzmann spectrum, reflecting the energetic distribution of the electrons in the channel. From the slope of the semilogarithmic EL versus energy plots, it is possible to calculate the

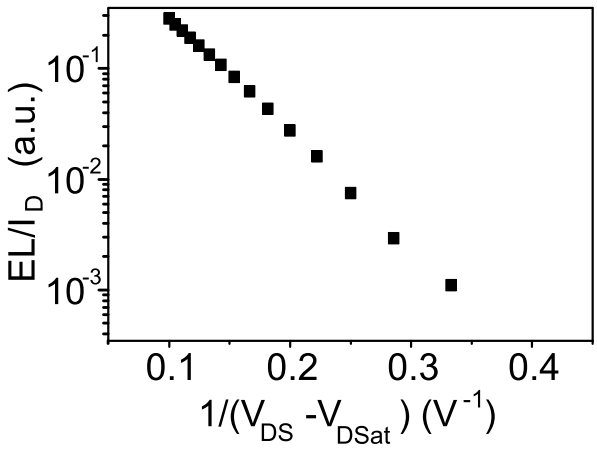


Figure 3.12: Dependence of the EL/I_D ratio on the electric field expressed as $1/(V_{DS} - V_{Dsat})$ (Chynoweth's law). EL is measured at $V_{GS} = 1$ V.

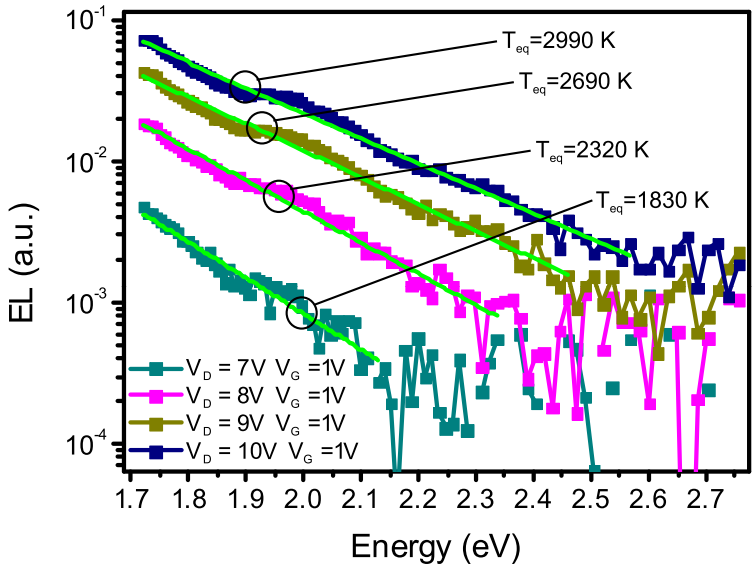


Figure 3.13: EL spectra measured for different V_{DS} levels on a ITO-gate sample. Equivalent electron temperature values are indicated in the diagram.

temperature of hot electrons using the Maxwell-Boltzmann distribution:

$$f_M(E_S) = \exp\left(-\frac{E_S}{kT_{eq}}\right) \tag{3.3}$$

where E_S is the energy of the state, k the Boltzmann's constant and T_{eq} the equivalent temperature of electrons. In Fig. 3.13 representative values obtained on one of the analyzed samples with the ITO gate are indicated. An increase in the drain voltage level determines an obvious increase in the average energy (in the equivalent temperature) of hot electrons.

As summarized, the intensity of the EL signal (Figs. 3.10 and 3.13) and the equivalent electron temperature provide information on the amount and energetic distribution of hot electrons in the channel: these two parameters can therefore be used for a comparison between the different series of analyzed samples. In particular, EL intensity depends on both the number of accelerated electrons and the intensity of the accelerating field. The effect of the electric field can be therefore appreciated by plotting the ratio between the EL intensity and the drain current (EL/I_D ratio): measurement results indicate that devices with longer gate-drain distance have a lower EL/I_D signal, as one can see in Fig. 3.14, due to the lower electric field and that devices without passivation have a significantly lower EL/I_D signal - Fig. 3.15a and 3.15b - and a lower equivalent electron temperature, Fig. 3.15c. This last result is due to the fact that unpassivated devices, during operation, can show significant trapping of negative

charge in the gate-drain access region. This may result in a "virtual gate" effect, which effectively decreases the maximum intensity of the electric field in the channel. Results indicate that, for a given device geometry, EL characterization can be effectively used for comparing different devices in terms of intensity of the electric field.

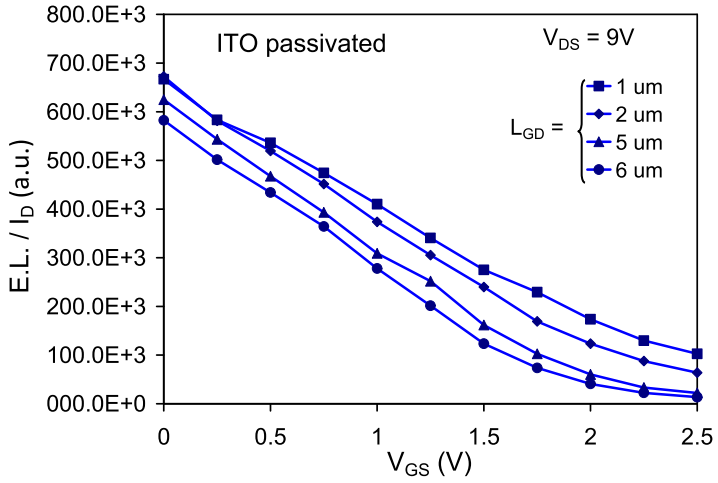


Figure 3.14: EL/I_D intensity as a function of the gate voltage level for samples with different gate-drain spacing.

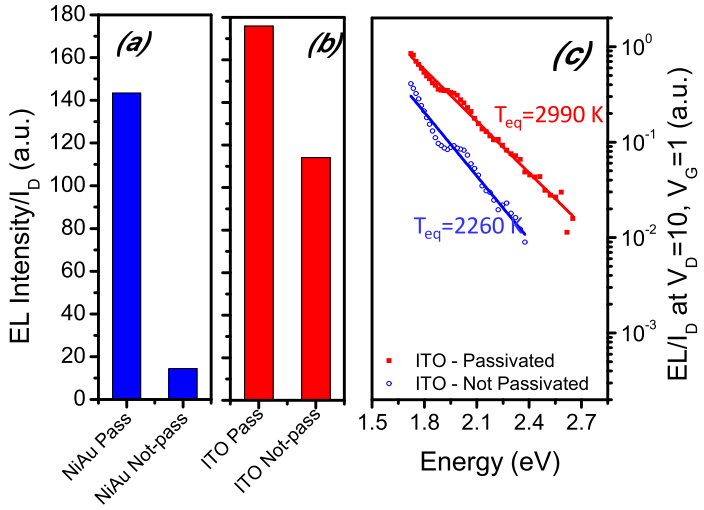


Figure 3.15: (a) and (b) intensity of the maximum EL/I_D signal for the four different series of analyzed samples. Each bar represents the average of four samples with similar characteristics. (c) EL/I_D spectra of two HEMTs with ITO gate, with and without passivation.

3.3.4 Results Discussion

The results obtained from electrical and EL measurements in this work have shown how these two techniques can provide useful and complementary information. More specifically, pulsed measurements can be used to quantify the role of traps in determining current collapse. Furthermore, as previously demonstrated, an accurate analysis of pulsed-g_m measurements allows one to investigate the localization of the traps within a HEMT structure. On the other hand, EL measurements can be used to investigate the role of traps in limiting the electric field and the equivalent electron temperature.

Obviously, results of pulsed-g_m and EL measurements must be mutually consistent. For instance, if, on the one hand, traps within the access regions may induce a significant current collapse, on the other hand they can limit the accelerating field, thus reducing the intensity of the EL signal and the equivalent electron temperature. Results of the electrical and optical measurements are therefore correlated, in the sense that the presence of traps can consistently modify the electrical and optical parameters. An example is shown in Fig. 3.16, which reports, for both passivated and unpassivated HEMTs with ITO gate, the results of pulsed-g_m measurements (more specifically, the transconductance collapse), the intensity of the EL/I_D signal under ON-state conditions, and the equivalent electron temperature. As it can be noticed, unpassivated samples show a significant transconductance collapse, a lower EL/I_D signal, and a

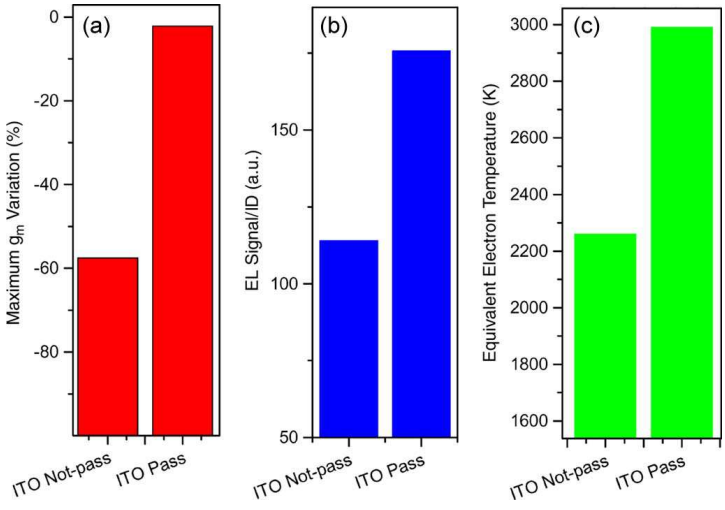


Figure 3.16: Electrical and optical parameters measured on HEMTs with ITO gate with and without passivation. (a) Transconductance collapse (relative transconductance variation induced by the use of a (V_{G-qb}, V_{D-qb})=(−4 V, 10 V) quiescent bias point with respect to (0 V, 0 V). (b) EL/I_D signal and (c) equivalent electron temperature measured at V_D = 10 V, V_G = 1 V.

lower equivalent electron temperature. This confirms the mutual consistency of the results of the pulsed-g_m and EL measurements.

Despite the important consistency between the results of pulsed-g_m and EL measurements, both techniques must be jointly used to achieve full characterization of the effect of traps on the performance of GaN-based HEMTs.

3.4 ETH Sample

In this section the results obtained by applying the electro-optical technique previously described on AlGaN/GaN HEMTs with recessed gate processed on silicon substrate are presented. The transistors on this wafer, processed at the ETH-Zurich laboratories, are characterized by a T-shaped gate electrode and by three different recess widths. The purpose of the work was to study the trapping effects in relation to the dimension of the gate recess.

3.4.1 Sample Description

Measured samples are AlGaN/GaN HEMTs fabricated on a HR-Si (111) substrate with a narrow gate recess. The layer structure is composed as follows: a nucleation/transition layer, a 1.7 µm GaN insulating buffer/channel layer and a 17.5 nm thick $Al_{0.26}Ga_{0.74}N$ barrier followed by a 2 nm GaN cap layer. Ohmic contacts are formed with a Ti/Al/Au metal stack (28/47/50 nm). Gate electrode has a T shape with a 400 nm width head and a footprint of 75 nm. The gate recess is 8 nm deep, while three different dimensions have been adopted for its width: 50, 80 and 200 nm, see Fig. 3.17. The gate metallization is a Ni/Au stack of 25/375 nm respectively. The source drain distance (L_{SD}) is 2 µm and gate contact is centered in the middle (the device is symmetric). Samples are finally passivated with 100 nm-thick PECVD SiN layer, deposited at 300°C.

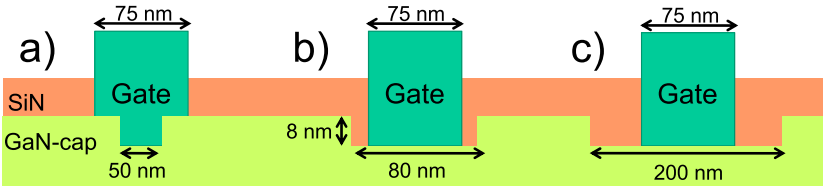
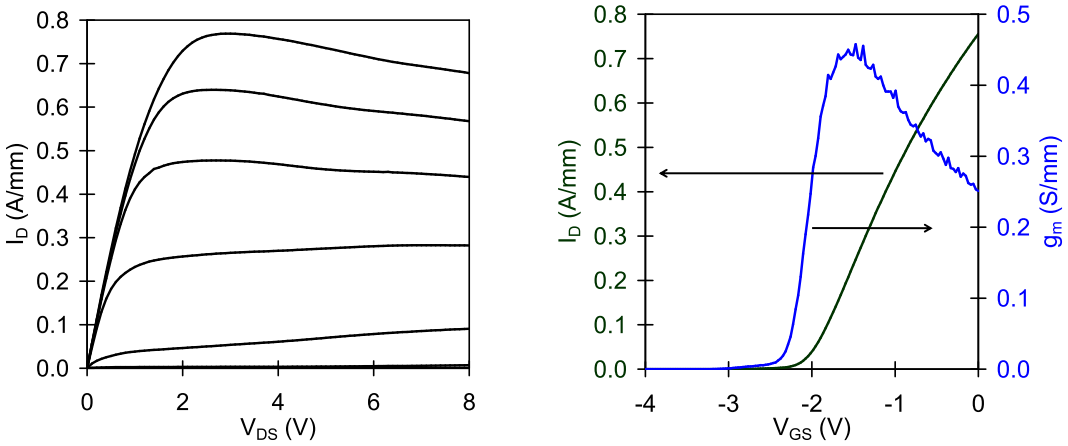


Figure 3.17: Schematic representation of gate electrode: gate footprint and recess are equals for each sample; the recess widths are 50 nm (a), 80 nm (b), 200 nm (c).

3.4.2 Electrical and Optical Characterization

Devices feature maximum current levels of about 800 mA/mm (pinch off voltage was about -2 V, see Fig. 3.18a) with a transconductance peak of 450 mS/mm (Fig. 3.18b). Furthermore, gate leakage current was fairly limited (well below 10 µA/mm at -4 V V_{GS} bias). Also these devices show a maximum f_{MAX} = 170 GHz and a cut-off frequency of f_T = 83 GHz at optimal bias condition (V_{DS} = 9.45 V, V_{GS} = −1.4 V), see Fig. 3.19. These values demonstrate a clear improvement over non-recessed devices fabricated and set a new record for f_{MAX} in fully-passivated GaN-on-silicon HEMT devices [21].



(a) $I_D - V_{DS}$ at V_{GS} from 0 to −1 V

(b) $I_D - V_{GS}$ at V_{DS} = 4 V

Figure 3.18: DC characteristics of a transistor with recess width of 50 nm.

Trapping phenomena has been investigated by means of dynamic $I - V$ measurements. Three quiescent bias points have been selected: (V_{G_qb}, V_{D_qb}) = (0 V, 0 V); (−4 V, 0 V) and (−4 V, 8 V), pulse period and pulse width have been set to 100 µs and 1 µs, respectively. Current collapse has been found to be about 20% and mainly due to surface passivation traps rather than to bulk traps (3.20). In fact, the collapsed g_m curves present only a limited threshold voltage shift and a strong g_m peak decrease (3.20b).

A parameter, called *SlumpRatio* (*S.R.*), is defined for both current and transconductance decreases in order to make possible a quantitative comparison among samples. The $\{S.R.\}_{I_D}$ is defined as the ratio between the I_D measured at V_{DS} = 2 V for the most severe bias condition and the I_D in the non trapping bias condition:

$$\{S.R.\}_{I_D} = \frac{I_D\,(-4\,\mathrm{V}, 8\,\mathrm{V})}{I_D\,(0\,\mathrm{V}, 0\,\mathrm{V})} \tag{3.4}$$

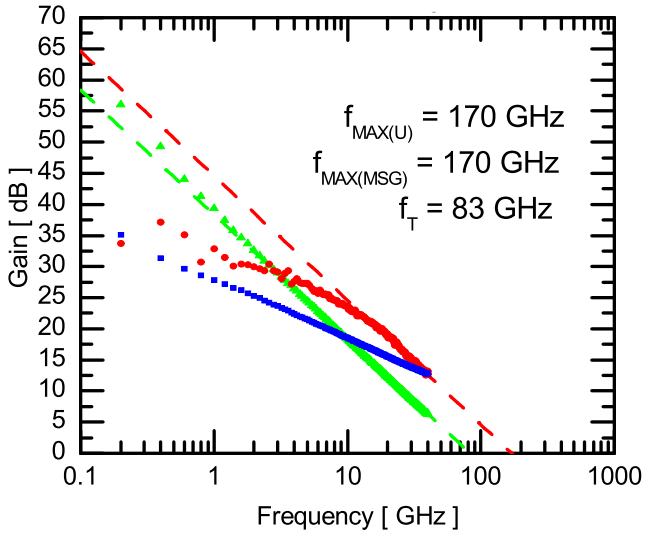
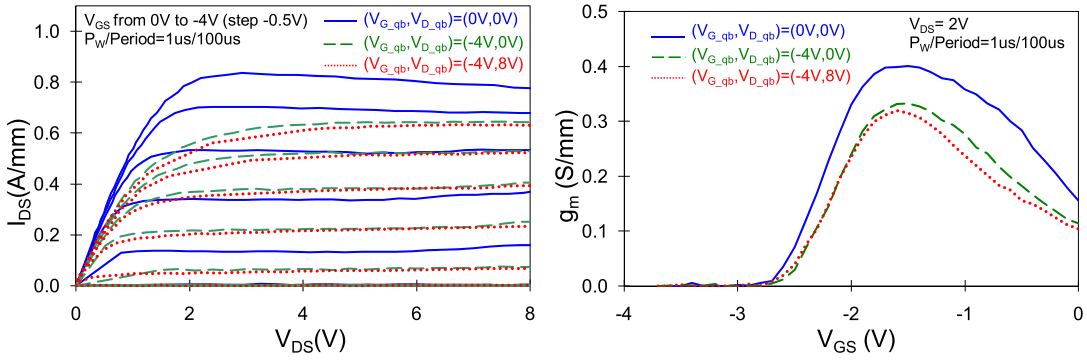


Figure 3.19: RF measurement at optimal bias (V_{DS} = 9.45 V, V_{GS} = −1.4 V); f_{MAX} = 170 GHz, f_T = 83 GHz.



(a) Pulsed $I_D - V_{DS}$ **(b)** Pulsed $g_m - V_{GS}$ at V_{DS} = 2 V

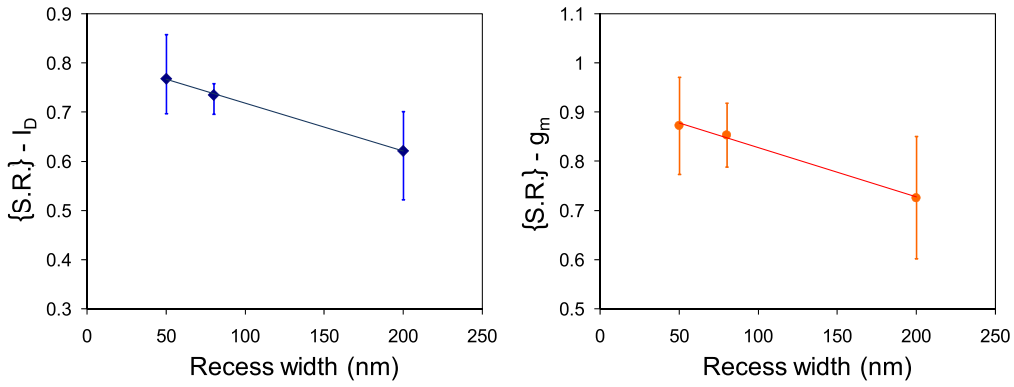
Figure 3.20: Pulsed characteristics of a representative device. Adopted quiescent bias point are indicated in the diagram.

While $\{S.R.\}_{g_m}$ is the ratio between the maximum of transconductance measured at V_{DS} = 2 V for the two bias condition:

$$\{S.R.\}_{g_m} = \frac{g_{m_{MAX}}\,(-4\,\mathrm{V}, 8\,\mathrm{V})}{g_{m_{MAX}}\,(0\,\mathrm{V}, 0\,\mathrm{V})} \tag{3.5}$$

The study of the current collapse as a function of the recess width shows an increase of the current collapse (lower values of $\{S.R.\}_{I_D}$) for longer recessed devices, see Fig. 3.21a; moreover the same identical trend is followed by the transconductance (Fig. 3.21b). This result suggests that samples with a larger recess are more sensitive to surface traps than the samples with smaller recess, likely due to a larger presence of

surface traps in the wider recess region. Also, since all the transistors have the same source-drain spacing, it is possible to assume that these traps are located prevalently in the recess area.



(a) $\{S.R.\}_{I_D}$ at V_{DS} = 2 V **(b)** $\{S.R.\}_{g_m}$ at V_{DS} = 2 V

Figure 3.21: Slump Ratio as function of recess width calculated for the output current I_D and transconductance g_m measured with double-pulsed technique.

Electroluminescence measurements have been carried out for characterizing hot-electrons in the studied short channel device: light emission at the drain edge of the gate, where the electric field is maximum, has been observed. The EL has been also used for a further comparison samples with different recess width. For the same bias condition the device with the smallest recess width has the highest EL/I_D values (see Fig. 3.22). Since the EL/I_D is an indicator of the electric field intensity in the device,

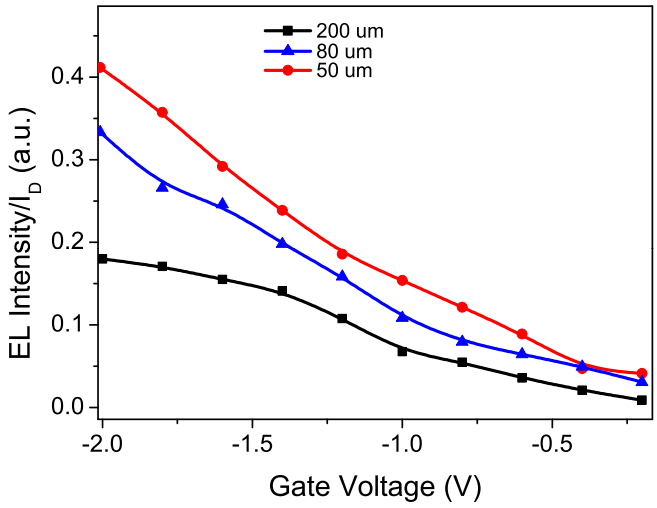


Figure 3.22: EL/I_D as function of V_{GS} at V_{DS} = 7 V. Different symbols are associated to the recess widths: squares - 200 nm, triangles - 80 nm, circles - 50 nm.

it is possible to confirm that the presence of an higher electric field with the smaller recess width. This result cannot be ascribed only to the shorter recess width, but also to the larger surface trap amount in the wider recess devices (that lowers the electric field in the gate-to-drain access regions). Furthermore the same dependency of EL from the recess width is found in the EL spectra: from Fig. 3.23 it is possible to see that the measured equivalent temperature (T_{eq}) is higher in samples with narrow gate recess, which confirms the presence of a more intense electrical field.

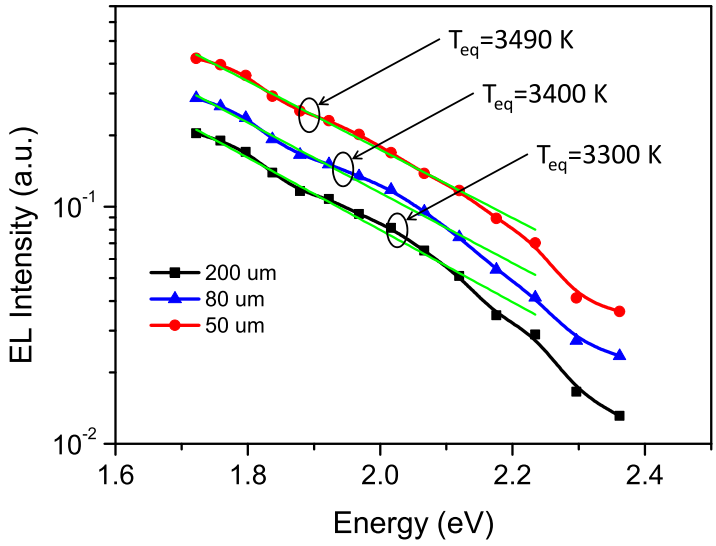


Figure 3.23: EL as function of Photon Energy at V_{DS} = 8 V and V_{GS} = −1.8 V. Different symbols are associated to the recess widths: squares - 200 nm, triangles - 80 nm, circles - 50 nm. The equivalent temperature of hot-electrons is reported in the diagram.

At the end another demonstration about the utility of the combined electro-optical measurement as a rapid and effective technique for the analysis of traps in GaN-based samples has been obtained. In fact both dynamic and EL measurements have shown that devices with recess width greater than the gate foot have a high level of surface traps nevertheless the presence of the passivation layer; presumably these traps are located at the edge of the gate electrode and behave as a Field Plate which reduces the electric field.

3.5 Conclusions

In conclusion a combined electro-optical methodology for the evaluation of trap and hot-electron related effects in GaN HEMTs has been presented. The proposed procedure is based on pulsed g_m versus V_G measurements and EL measurements; it has been

demonstrated that pulsed transconductance measurements can provide rapid characterization of a particular technological process in terms of the presence of traps under the gate of GaN-based HEMTs and the presence and effect of traps in the gate-drain access regions. Furthermore, by means of EL, it is possible to compare different devices in terms of amount and equivalent temperature of hot electrons, thus achieving indirect data on the potential reliability of the HEMTs and on the levels of electric field in the channel. The proposed measurement procedure can be easily integrated in standard characterization setups, with the aim of providing rapid comparison of different device technologies.

4

Low Frequency Noise

The Low Frequency Noise (LFN) is a well know phenomenon in electronic devices: it is a perturbation of current or voltage in the electronic circuits due to external interferences or to internal random fluctuations due to physical mechanism governing the carrier transport. Random fluctuations are interesting to study, since they are directly linked to physical phenomena occurring inside the device: in fact noise is related to the presence of defects, traps and generally to the quality of the device. For this reason the noise measurements can be used as a diagnostic tool for the analysis of semiconductor devices.

In this work the low-frequency noise is analyzed from a theoretical point of view and a detailed description of the measurement system used for the device characterization is presented. Then the results of the experimental analysis of noise carried out on AlGaN/GaN devices are reported, in particular they are measurements of TLM structures with different realization technology and measurements of transistors selected from the same wafer.

4.1 Fundamental Mechanisms of Noise

A generic signal $X(t)$ can be expressed as the sum of a constant part plus a time dependent part:

$$X(t) = \langle X \rangle + \Delta X(t) \tag{4.1}$$

where $\langle X \rangle$ is the average over a long time interval and $\Delta X(t)$ represents the fluctuations. Since the noise is a random process, it can be studied by means of probability theory, as shown in [58], in [59] and in [60]. $\Delta X(t)$ can be expressed as a Fourier series:

$$\Delta X(t) = \sum_{n=-\infty}^{n=+\infty} a_n e^{(j2\pi f_n t)} \tag{4.2}$$

where $n = 0, \pm1, \pm2...$ and a_n is calculated as:

$$a_n = \frac{1}{T}\int_0^T \Delta X(t)\, e^{(-j2\pi f_n t)} dt \tag{4.3}$$

The average noise measured at frequency f_n is $\langle \Delta X_n \rangle = 0$, while the squared mean value can be expressed as: $\left\langle (\Delta X_n)^2 \right\rangle = 2\, \langle a_n a_n^* \rangle$, where $*$ denotes the complex conjugate of a_n.
Now it is possible to define the power spectral density (PSD) as

$$S_X(f) = \lim_{T\to\infty} 2T\, \langle a_n a_n^* \rangle \tag{4.4}$$

The PSD is used to describe the distribution with the frequency of the power intensity of the signal; where the power is intended to be the squared of the signal amplitude, i.e. $\langle a_n a_n^* \rangle$ at a specific frequency f_n. We define the autocorrelation function $\varphi_X(t)$:

$$\varphi_X(t) = \langle \Delta X(t_0)\, \Delta X(t_0 + t) \rangle \tag{4.5}$$

then $S_X(f)$ can be calculated from the Wiener-Khintchine theorem:

$$S_X(f) = 4\int_0^\infty \varphi_X(t) \cos(2\pi f t)\, dt \tag{4.6}$$

Therefore we will refer the noise as a PSD (Power Spectral Density), with units V^2/Hz if we consider the voltage fluctuations - $S_V(f)$ - and A^2/Hz for current fluctuations - $S_I(f)$.

At low frequency (from few Hz to MHz range) there are four main type of noise in semiconductors:

- thermal noise,
- shot noise,
- generation - recombination (g-r) noise,
- $1/f$ noise;

the first two are called also *white noise*, because their PSD is constant for each frequency; while g-r and $1/f$ noise depend on the frequency. In Fig. 4.1 a schematic representation of a generic $S_X(f)$ is shown: it is possible to see how the different noise quantities play a role in defining the final shape of the low frequency noise. The different noise sources will be discussed in details in the following paragraphs.

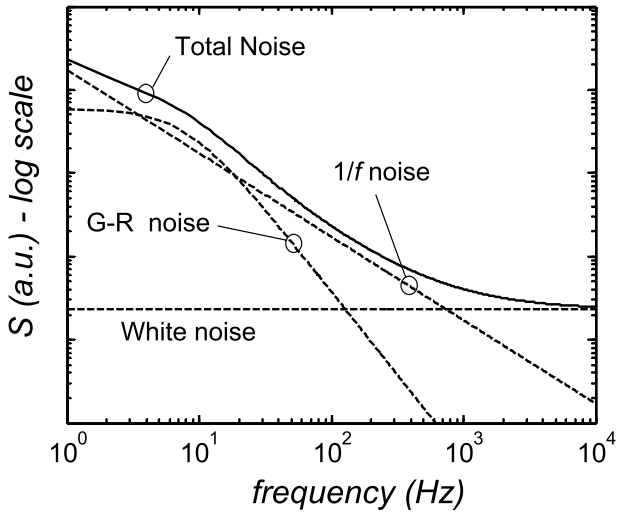


Figure 4.1: A generic PSD of low frequency noise. Dashed curves represent the decomposition of total noise in different excess noise components [58].

4.1.1 Thermal Noise

Thermal noise comes from random thermal motion of charge carriers in the material: scattering phenomenon occurring in the material change the electron velocity and direction, causing local fluctuations of the flowing current. Any material with resistance R shows spontaneous current fluctuations [61] and the PSD of the thermal noise can be calculated as:

$$S_I = \frac{4kT}{R} \quad \text{or} \quad S_V = 4kTR \tag{4.7}$$

where T is the material temperature and k the Boltzmann's constant ($k = 8.617 \cdot 10^{-5}$ eV/K).

4.1.2 Shot Noise

Shot noise in semiconductors appears when the current is flowing across a potential barrier. Since the current is not a continuous stream but it is formed by discrete elements with elementary charge q, the shot noise is generated when electrons randomly cross the barrier crating a fluctuation in the current. When a current with average value I crosses a potential barrier, the PSD of the shot noise is given by:

$$S_I = 2qI \tag{4.8}$$

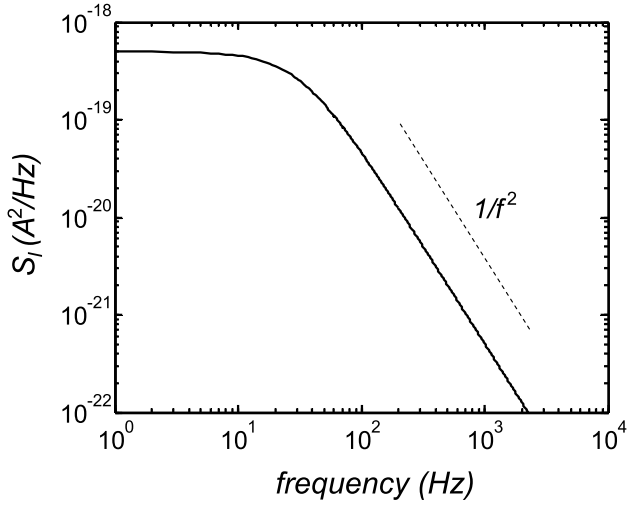


Figure 4.2: A schematic representation of PSD for g-r noise [58].

4.1.3 Generation-Recombination Noise

Generation-Recombination noise is a fluctuation of number of carriers due to the presence of traps in the semiconductor. If we consider a certain number of traps with the same relaxation time constant τ, the continuous trapping/detrapping process between conduction or valence band and the traps creates fluctuations in the number N of free charges in the semiconductor. The PSD of the fluctuation (ΔN) of carriers number is

$$S_N(f) = 4\overline{\Delta N^2}\frac{\tau}{1+(2\pi f)^2\tau^2} \tag{4.9}$$

The shape of g-r noise is called *Lorentzian* and it is represented in Fig. 4.2.

A particular case of g-r noise is the Random-Telegraph-Signal (RTS) noise: it occurs when a few traps are present in the semiconductor. In the time domain it is displayed as finite switching events between two (or more) levels. Each event corresponds to the capture or the release of a carrier. In Fig. 4.3 a simplified example of a MOSFET is reported: the drain current I switches between two levels when an electron moves from traps in the oxide to the channel and vice versa; the resulting fluctuations is similar to a telegraph signal. By studying time durations of lower state τ_l and higher state τ_h, it is possible to extract information about the type of traps involved.

4.1.4 *1/f* Noise

The $1/f$ noise, also called *flicker noise*, is a generic name for fluctuations that show a PSD proportional to $1/f^\gamma$, where γ is close to 1 (usually $0.7 \leq \gamma \leq 1.3$). The general

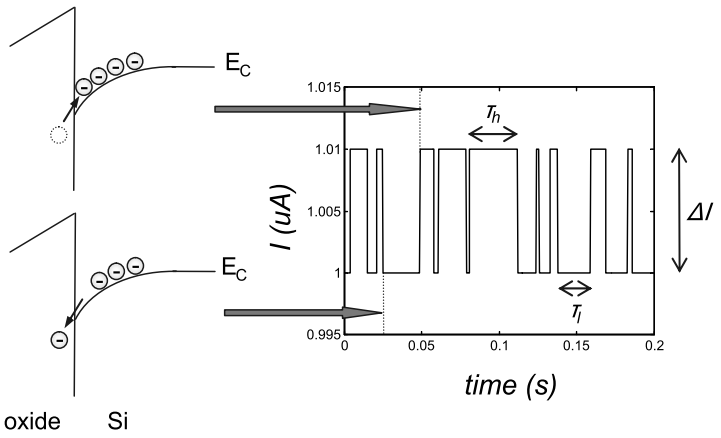


Figure 4.3: A schematic representation of RTS noise in a MOSFET: drain current I switches between two levels following the trap/detrap process of a carrier in the oxide [58].

expression (considering current fluctuations) is

$$S_I = \frac{K \cdot I^{\beta}}{f^{\gamma}} \tag{4.10}$$

where K is a constant related to the intensity of the noise and β the current exponent (usually ≈ 2). The presence of $1/f$ noise has been experimentally proved in a wide range of materials and semiconductor devices, from 10^{-5} Hz to 10^{7} Hz; but a complete explanation of its origin has not been found yet [62].

Two are the basic physical mechanisms which can produce a fluctuations in the current:

- fluctuations in the mobility μ;
- fluctuations in the number of carriers N.

Fluctuations in the carrier number

If we consider a large number of traps with different time constant distributed as

$$g(\tau) = \frac{1}{\ln(\tau_2/\tau_1)\,\tau} \tag{4.11}$$

for $\tau_1 < \tau < \tau_2$, while $g(\tau) = 0$ elsewhere.

Then the superposition of all power spectral density is equal to

$$S_{tot} = \int_0^{\infty} g(\tau)\, S_{g-r}(\tau)\, d\tau \approx \frac{B}{4 \ln(\tau_2/\tau_1)\, f} \tag{4.12}$$

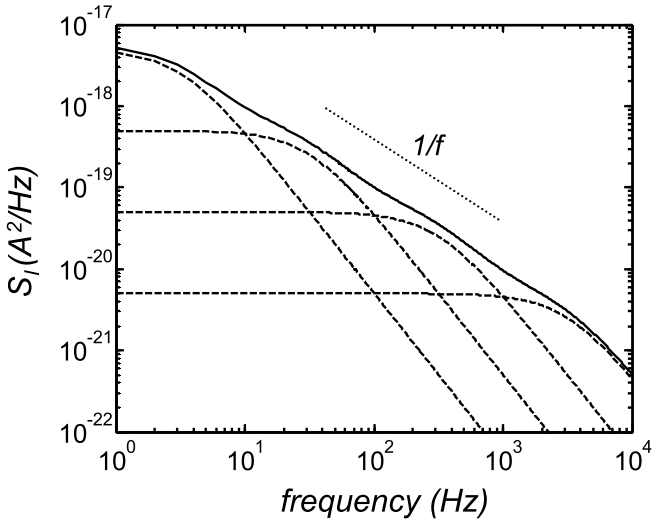


Figure 4.4: Superposition of different g-r noise, giving a $1/f$ trend [58].

The diagram in Fig. 4.4 shows how the final shape of S_{tot} recalls the $1/f$ trend.

Fluctuations in the mobility

According to the empirical model proposed by Hooge, the PSD of resistance fluctuations is defined as

$$\frac{S_R}{R^2} = \frac{\alpha_H}{N}\frac{1}{f} \tag{4.13}$$

where α_H is dimensionless and takes the name of Hooge's parameter. At the beginning of its discovery, α_H was supposed constant and equal to $\approx 2 \cdot 10^{-3}$; then other studies have shown that α_H can assume different values, lower or higher, depending on the quality of the semiconductor crystal.

The real origin of the $1/f$ phenomena is still argument of debate; most of the authors think that both models are correct and the noise is a combination of the two sources [63]. Only for simplicity reasons, in this thesis we will consider prevalently the Hooge's model: in fact,the parameter α_H represents an easy way to compare samples from different technologies and with values reported in literature.

4.1.5 Equivalent Noise Circuits

The low frequency noise in a device can be easily extracted by measuring the current or voltage fluctuations when biased in ohmic region; moreover the following relations are valid and they allow to directly compare measurements taken in different conditions [59]:

$$\frac{S_I(f)}{I^2} = \frac{S_V(f)}{V^2} = \frac{S_R(f)}{R^2} = \frac{S_G(f)}{G^2} \tag{4.14}$$

the generic quantity $S_X(f)/X^2$ (where $X = I$, etc.) is called *normalized noise*.

Since the noise is a signal superimposed to the DC components, the noisy device can be represented in a small-signal equivalent circuit as the ideal element (noiseless) and a signal generator with power spectral density equal to the noise PSD. Depending on which model we are considering, fluctuations in the voltage or in the current, the generator can be in series (S_V - voltage noise source) or in parallel (S_I - current noise source) to the noiseless element, see Fig. 4.5.

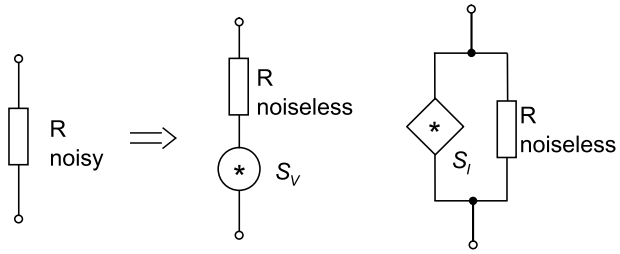


Figure 4.5: Schematic representation of the equivalent circuit of a noisy device.

4.2 The Measurement System

Measuring low frequency noise requires a very good experimental setup with low-noise instrumentation and good device and equipment shielding from external disturbances [64]. A schematic representation of the experimental setup is reported in figure 4.6, where each box represents the external metal chassis or the prober shielding. The semiconductor parameter analyzer is a HP4142, with two medium power and two high power Source/Monitor Unit (SMU); this instrument is used for the standard DC characterization of the device and as DC-source bias during the noise measurement. The power spectral density is measured with a HP35665A dynamic signal analyzer. Since the DC bias must be "clean" as much as possible, RC-filters are used for screening the signal from noise coming from the power line, like the 50 Hz component. Moreover the voltage or current fluctuations are usually very low to be measured directly with the dynamic signal analyser; therefore an amplifier unit is required in order to obtain valid measurements. These two functions are both implemented in the BTA9812B Amplifiers/Unit; a detailed description of this unit is reported in the following section. The Device Under Test (DUT) is inside a shielded probe station connected to ground. Connections between the different equipments are made by biaxial or triaxial cables. Great care of connections and groundings must be taken: the cables must be chosen as short as possible, to avoid antenna effects. Distributed ground connections increase the

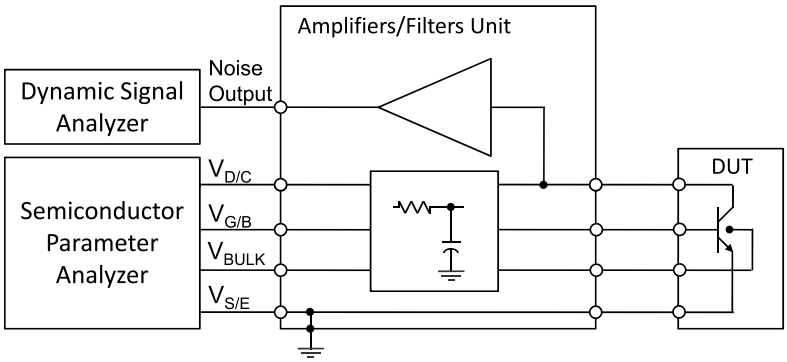


Figure 4.6: Schematic representation of the noise measurement system.

probability to create a ground-loop, so it is preferable to have only one ground point, in our case the prober shield. Also connectors between cables and instrumentations represent a way for the external noise to get inside the system. Using direct connections is the best case, but sometimes (especially in not-dedicated system) it is not possible. So in these cases all precautions are mandatory to obtain reliable measurements. All the aforementioned instruments are connected by a IEEE-488 (GPIB) cable to the BTA9812B Controller Unit and to a PC equipped with the *NoisePro* software from ProPlus Inc.

4.2.1 The BTA9812B Amplifiers/Filters Unit

As discussed in the previous section, the power line filters and the amplifier circuits are both implemented in the BTA9812B Unit. A simplified representation of the circuit is reported in Fig. 4.7. It is possible to distinguish a voltage and a current pre-amplifier (V_{amp} and I_{amp}), a load resistor (R_L), an input resistor (R_B) and the RC filters for the DC bias.

A short description of each element is now presented (from [65]).

DC bias filters

The filter resistors are R_{BF}, for the device base/gate, R_{CF}, for the collector/drain, R_{BULK}, for the bulk. It is possible to use three different values for these resistors: each value corresponds to a specific cut-off frequency as reported in table 4.1. Long filter time-constants give higher accuracy on the noise measurement, but require longer measurements time.

Voltage pre-amplifier

The voltage pre-amplifier is used for devices with low output impedance. It has a bandwidth of $0.5\,\mathrm{Hz} - 1\,\mathrm{MHz}$ and a noise floor of $1.4\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. In Fig. 4.8 the equivalent

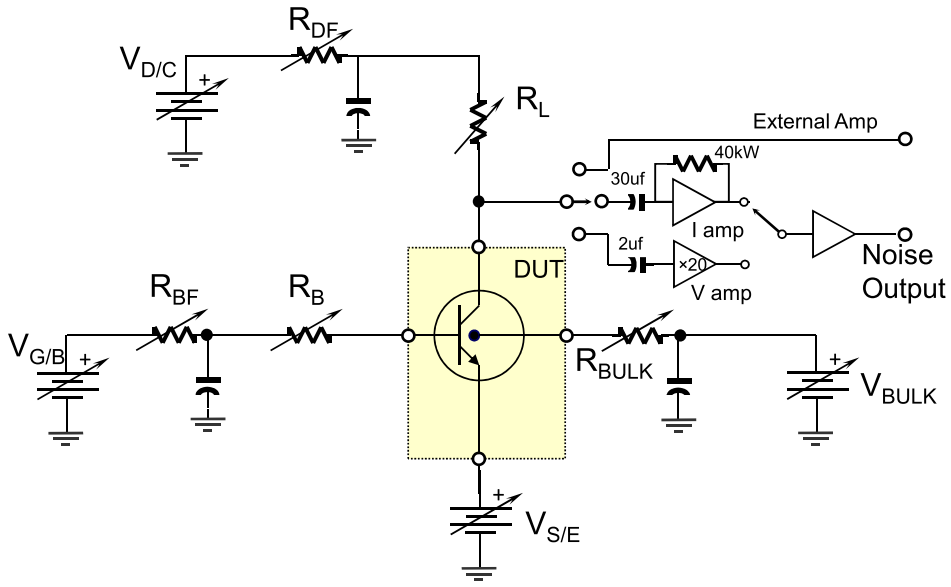


Figure 4.7: Schematic representation of the BTA 9812B Amplifiers/Filters Unit.

Cut-off frequency (3 dB)	R_{BF}	R_{CF}	R_{BULK}
1 Hz	1 kΩ	300 Ω	300 Ω
0.3 Hz	3 kΩ	1 kΩ	1 kΩ
0.1 Hz	10 kΩ	3 kΩ	3 kΩ

Table 4.1: Values for filter resistors and associated cut-off frequencies.

small-signal circuit for the voltage amplifiers is presented: in this circuit the DUT is modeled as a noiseless resistor (R_{out}) with its noise current source ($\tilde{I}_x$). The other elements of the circuit are also considered with their own noise source: the load resistor R_L with thermal noise $\tilde{I}^2_{RL} = 4kT/R_L$; the amplifier with input resistance $R_{in} = 1\,\mathrm{M\Omega}$ and gain $A = 500$, with a voltage ($\widetilde{V}_n$) and a current ($\tilde{I}_n$) noise sources.
The amplifier output V_{out} is calculated as:

$$V^2_{out} = A^2 R^2_{ref}\left(\tilde{I}^2_x + \tilde{I}^2_n + \frac{4kT}{R_L}\right) + A^2\widetilde{V}^2_n\left(\frac{R_{in}}{R_{in} + R_L//R_{out}}\right)^2 \tag{4.15}$$

where $R_{ref} = R_L//R_{out}//R_{in}$ and all the squared quantities represent the PSD of the signal.

Current pre-amplifier

The current pre-amplifier is used for devices with high output impedance. Its bandwidth is 0.5 Hz – 1 MHz and the noise floor is $0.5\,\mathrm{pA}/\sqrt{\mathrm{Hz}}$. In Fig. 4.9 the equivalent small-signal circuit is presented: the noise source are the same of the voltage pre-amplifier plus a feedback resistor R_a and the associated noise source $\tilde{I}_a$. The amplifier

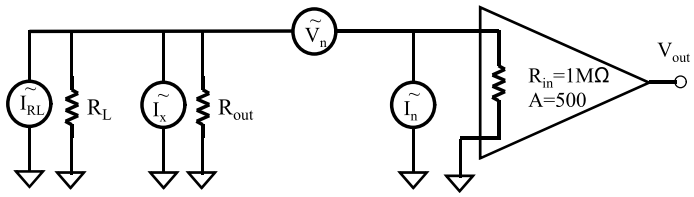


Figure 4.8: Schematic representation of the voltage pre-amplifiers.

output V_{out} is calculated as:

$$V_{out}^2 = R_a^2 \left[\tilde{I}_x^2 + \tilde{I}_n^2 + 4kT \left(\frac{1}{R_L} + \frac{1}{R_a} \right) + \tilde{V}_n^2 \left(\frac{1}{R_L} + \frac{1}{R_{out}} \right) \right] \tag{4.16}$$

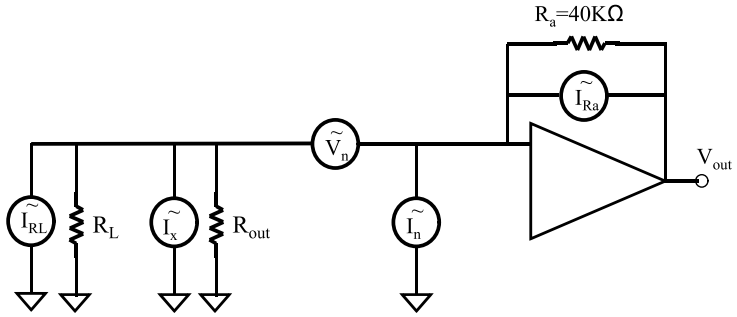


Figure 4.9: Schematic representation of the current pre-amplifiers.

4.2.2 R_L Selection

The working bias condition of the DUT is set by choosing the appropriate values of R_B and R_L. Allowed values of R_B are 0, 100 Ω, 1 kΩ, 10 kΩ, 100 kΩ, 1 MΩ, 10 MΩ, 10 MΩ, 100 kΩ. The input resistor is usually required only for bipolar transistor.

The values of R_L are 100 Ω, 333 Ω, 1 kΩ, 3.3 kΩ, 10 kΩ, 100 kΩ, 1 MΩ. The selection of the correct value of R_L is not an easy task: in fact the load resistor affects not only the DC bias point but also the lowest noise level that can be measured and the bandwidth of the system.

The total cut-off frequency (f_T) of the system can be calculated with the following formula:

$$f_T = \frac{1}{2\pi C_T R_{in} // R_L} \tag{4.17}$$

where C_T is the total parasitic capacitance coming from cables, probe tips, wafer chuck, connectors; R_{in} is the amplifier input resistance (1 MΩ for the voltage amplifier and 40 kΩ for the current amplifier). Therefore a large R_L leads to a lower f_T and low values are preferable for a large bandwidth, especially for the voltage amplifier.

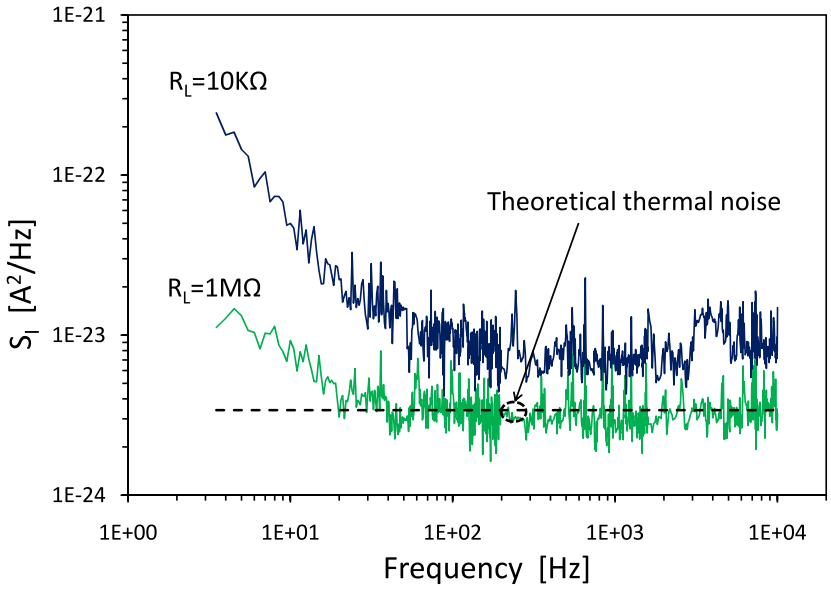


Figure 4.10: Noise PSD for a 4.8 kΩ metallic resistor. Bias condition are 8 mV for R_L = 1 MΩ and 40 mV for R_L = 10 kΩ

On the other hand, the value of R_L drastically affects the noise floor of the entire system. For better understanding how the best load must be chosen, let us consider the following example: the theoretical value of the thermal noise of a metallic resistor of value $R = 4800\Omega$ is, according to (4.7), $3.4{\cdot}10^{-24}\,\mathrm{A^2/Hz}$. This resistor is measured using two different R_L values. i.e. 10 kΩ and 1 MΩ. Fig. 4.10 illustrates the experimental values of $S_I(f)$. For R_L = 1 MΩ the experimental white noise matches the theoretical one. For R_L = 10 kΩ the measured white noise is almost two times higher.

These results are explained in Fig. 4.11, where all the terms of (4.15) are plotted as function of R_{out}: the triangles are the theoretical thermal noise of the DUT calculated as

$$\blacktriangle: \quad A^2 R_{ref} \frac{4kT}{R_{out}} \tag{4.18}$$

the squares indicate the sum of the amplifier current noise and the load noise:

$$\blacksquare: \quad A^2 R_{ref} \left(\frac{4kT}{R_L} + I_n^2 \right) \tag{4.19}$$

the circles are the amplifier voltage noise, calculated as

$$\bullet: \quad A^2 V_n^2 \left(\frac{R_{in}}{R_{in} + R_L // R_{out}} \right)^2 \tag{4.20}$$

The PSD of the noise sources of the amplifier can be measured with a specific software function: $V_n^2 \approx 6 \cdot 10^{-18}\,\mathrm{V^2/Hz}$, $I_n^2 \approx 1.5 \cdot 10^{-25}\,\mathrm{A^2/Hz}$.

The continuous line represents the output power spectral density $[V_{out}^2]$, in other words the sum of the three components just described.
The graph shows that the total output signal (solid line) is close to the DUT signal (triangles) only for $300\,\Omega < R_{out} < 5\,\mathrm{k}\Omega$. In this range the total output signal is two times higher than the DUT signal. In fact, the measured thermal noise of Fig. 4.10 is two times higher ($\approx 7 \cdot 10^{-23}\mathrm{A}^2/\mathrm{Hz}$) than the theoretical one. While with $R_L = 1\,\mathrm{M}\Omega$ the output signal and the DUT noise are practically coincident when a different R_{out} range is used, i.e. $500\,\Omega < R_{out} < 30\,\mathrm{k}\Omega$, see Fig. 4.12.

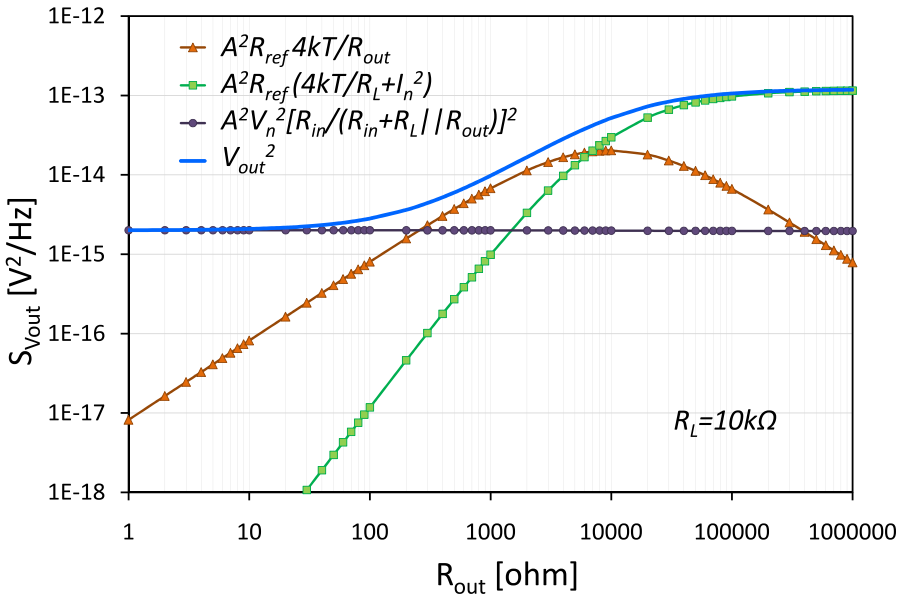


Figure 4.11: Calculated PSD of the total output as function of R_{out} (continuous line) for $R_L = 10\,\mathrm{k}\Omega$. Triangles represent theoretical DUT thermal noise; squares represent the sum of the amplifier current noise and the load resistor noise; circles represent the amplifier voltage noise.

The selection of R_L depends also on the bias applied to the DUT: in fact the device under test is the last element of a series of three, where the other two elements are R_{DF} and R_L, see Fig. 4.7 Consequently the bias applied to the DUT is the result of the voltage divider between $R_{DF} + R_L$ and R_{out}. If the R_L is too high it is possible that the system cannot apply the desired bias to the DUT because the output voltage required to the SMU is higher than its compliance. An example is shown in Fig. 4.13 where the two load-lines for $R_L = 1\mathrm{M}\Omega$ and $R_L = 10\mathrm{k}\Omega$ are reported with $R_{out} = 4.8\,\mathrm{k}\Omega$. With the same SMU output voltage, the SMU current is higher when $R_L = 10\mathrm{k}\Omega$ is used than the use of $R_L = 1\mathrm{M}\Omega$, resulting into a higher applied bias to the DUT.

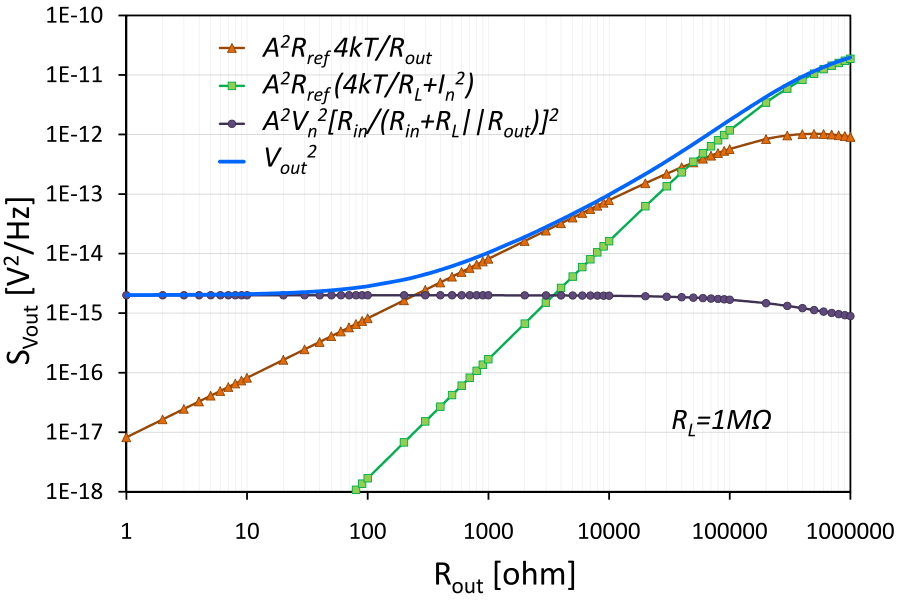


Figure 4.12: Calculated PSD of the total output as function of R_{out} (continuous line) for R_L = 1 MΩ. Triangles represent theoretical DUT thermal noise; squares represent the sum of the amplifier current noise and the load resistor noise; circles represent the amplifier voltage noise.

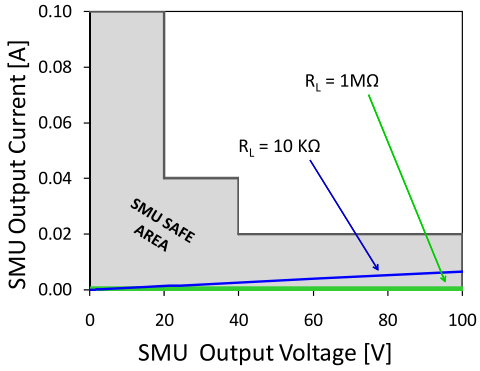


Figure 4.13: HP4142 - SMU power compliance (grey area); load line for R_F = 300 Ω, R_{out} = 4.8 kΩ with R_L = 10kΩ and R_L = 10kΩ are indicated.

In conclusion it is clear that the measurement condition depends on the characteristics of the DUT and at which bias the noise shall be measured. Therefore the conditions on bias and load shall be decided and verified carefully in order to obtain a reliable and repeatable noise measurement. All the measurements we will show have been performed with the voltage pre-amplifier. The current pre-amplifier was not used, but the same consideration on the bias condition and on the R_L selection can be done.

4.3 Measurements on TLM

The Transmission Line Model (TLM) is a simple planar structure that allows the extraction of two fundamental parameters for the characterization of a sample: the *specific contact resistance* (ρ_C^*) and the *sheet resistance* (R_{sh}). The purpose of the noise measurement on AlGaN/GaN TLM was to analyze which type of noise sources are present in these devices and try to separate the noise coming from the the contact from the noise related to de conductive channel. Also samples from wafers with different ohmic contact processing (with or without gold in the electrode stack and different annealing temperatures) have been measured in order to find a possible correlation between the ρ_C^*, R_{sh} and the noise level measured.

4.3.1 Noise Sources on TLM Structures

The circuit model for a TLM is a series of three resistors, i.e. two identical contact resistors (R_C) and a channel resistor (R_{CH}) [66], as reported in Fig. 4.14a. The total resistance is $R_T = R_{CH} + 2R_C$. By measuring samples with different spacing (L_x) but same contacts area $W \times D$ (see Fig. 4.14b) it is possible to separate the contribution of the channel resistance, which varies with L, from the contact resistance, that remains constant (Fig. 4.14.c). This technique is called *transfer length method* [67, 68] and leads to the following definition:

$$R_T = R_{CH} + R_C = R_{sh}\frac{L}{W} + 2\frac{\rho_C^*}{W} \tag{4.21}$$

From a noise point of view, we can consider two different noise sources in the TLM:

- $S_{R_{CH}}$ related to the channel,

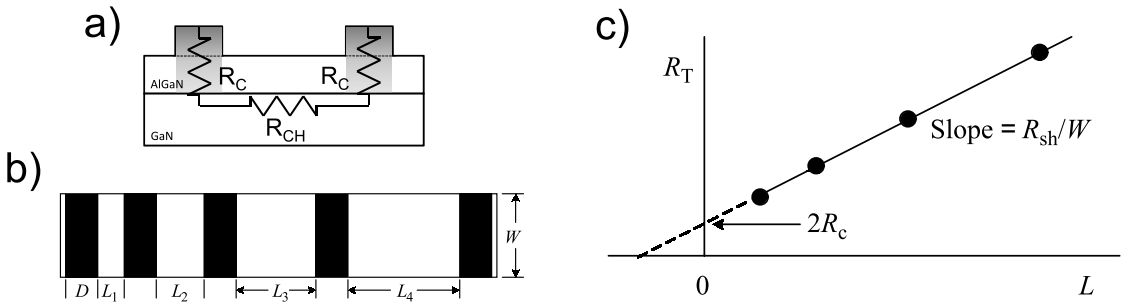


Figure 4.14: TLM layout and IV measurements: a) schematic cross section of a single TLM: R_C-contact resistance, R_{CH}-channel resistance; b) layout of a TLM: L-TLM length, $W \times D$-contact area; c) example of a R_T vs. L.

- S_{R_C} related to both the contact resistances.

Since the two quantities are assumed to be uncorrelated [69, 70], and the device is measured in ohmic region [71, 72], the following formula can be written:

$$\frac{S_I}{I^2} = \frac{S_{R_T}}{R_T^2} = \frac{S_{R_{CH}} + S_{R_C}}{\left(R_{CH} + R_C\right)^2} \tag{4.22}$$

where S_{R_T} is the total noise of the sample. The number of carriers in the channel can be expressed as follows:

$$N_{CH} = \frac{L^2}{q\mu_{CH} R_{CH}} \tag{4.23}$$

where μ_{CH} is the electron mobility in the channel. Then it is possible to apply the Hooge's model (eq. 4.13) to the channel resistance:

$$\frac{S_{R_{CH}}}{R_{CH}^2} = \frac{\alpha_{CH}\, q\, \mu_{CH}\, R_{CH}}{L^2} \frac{1}{f} \tag{4.24}$$

where α_{CH} is the Hooge's parameter for the conductive channel. The same mathematical approach is not possible for S_{R_C}/R_C^2, because the number of carrier in the contact (N_C) is unknown. One possibility is to define a new parameter λ, as in [73], that allows to write a similar expression for S_{R_C}:

$$\frac{S_{R_C}}{R_C^2} = \lambda R_C \frac{1}{f} \tag{4.25}$$

Combining (4.22), (4.24) and (4.25), the following model for the noise in TLM structures is derived:

$$\frac{S_I}{I^2} = \frac{1}{\left(R_{CH} + R_C\right)^2} \frac{1}{f} \left(\lambda R_C^3 + \frac{\alpha_{CH}\, q\, \mu_{CH}\, R_{CH}^3}{L^2} \right) \tag{4.26}$$

The quantity λ depends on the contact area (see Fig. 4.14), while α_{CH} is dimensionless. Therefore, to compare device with different contact geometries, a normalization of λ by the contact area $W \times D$ is required.

Finally eq. 4.26 can be rewritten including the definition of R_{CH} and R_C:

$$\frac{S_I}{I^2} = \frac{1}{W\left(R_{sh} L + 2\rho_C^*\right)^2} \frac{1}{f} \left(\lambda \left(2\rho_C^*\right)^3 + \alpha_{CH}\, q\, \mu_{CH}\, R_{sh}^3\, L \right) \tag{4.27}$$

4.3.1.1 Samples and Measurements

TLM structures from three different wafers with gold-free ohmic contacts (**MP10-02**, **MP10-03**, **MP11-03**) and from a wafer with gold-based contacts (**G021-B**) have been characterized. Fitting have been applied to the obtained noise spectra, according to (4.27), allowing the calculation of α_{CH} and λ for the two different technologies.

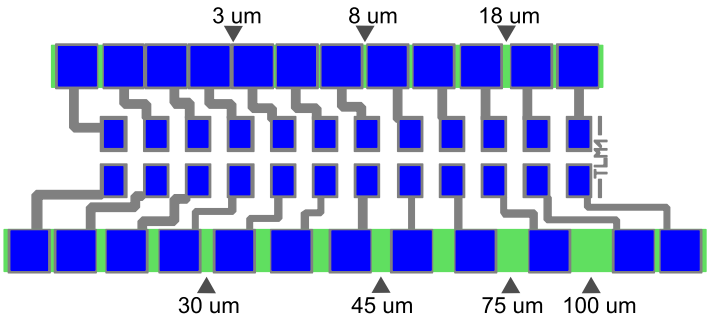


Figure 4.15: Mask layout of the TLM structure; lengths of measured sample are indicated.

4.3.1.2 MP10-02

The MP10-02 is a 6-inch GaN on Si wafer, devices have single AlGaN barrier and Al_2O_3 as gate dielectric. The epi-layer was grown by Metal Organic Chemical Vapor Deposition (MOCVD) on a Czochralski 6-inch Si (111) substrate. The buffer layers (18% AlGaN, 40% AlGaN and 70% AlGaN) have been grown at 1080°C; the GaN, AlGaN and in-situ Si_3N_4 have been grown at 1130°C. The spacer (AlN) was grown at 1130°C for 4 s. An overview of the epi-layers is shown in table 4.2.

6" Wafer Name	MP10-02
In-situ Si_3N_4 (nm)	120
18% AlGaN (nm)	10
GaN (nm)	150
18% AlGaN (nm)	1126
40% AlGaN (nm)	749
70% AlGaN (nm)	469
AlN (nm)	211
Si (111) (µm)	950
TBuffer (nm)	2555
Ohmic metalization (nm)	Ti/Al/W (20/100/20)
Ohmic metalization anneal	650°C, 1 min
Al_2O_3 deposition (nm)	12 , TMA+H_2O

Table 4.2: MP10-02 epi-layer description.

Figure 4.15 shows the layout of the TLM structure; the arrows indicate the 7 different samples selected for the noise characterization. The respective lengths (contact-to-contact distances) are 3, 8, 18, 30, 45, 75 and 100 µm; the ohmic contact is a 100×100 µm square.

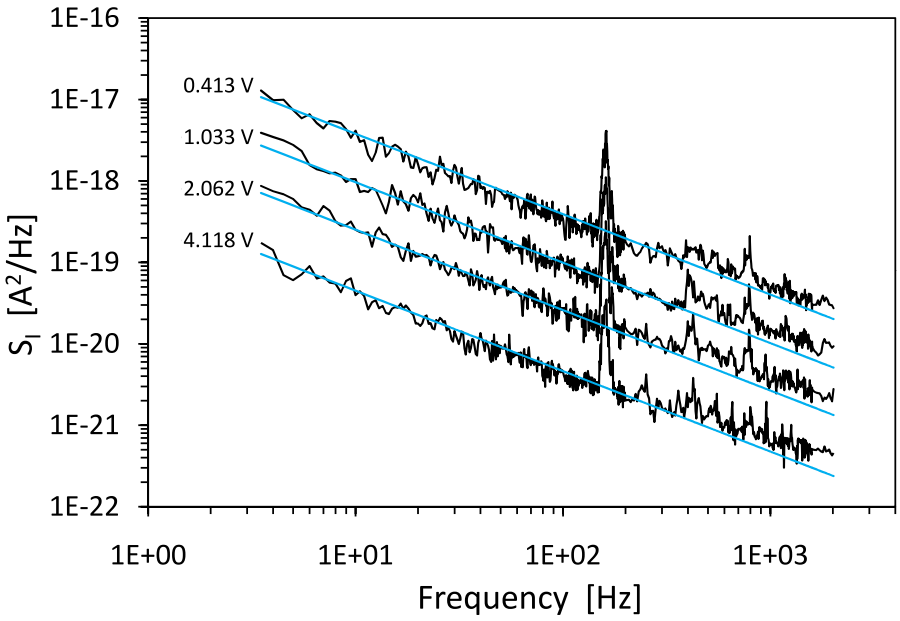


Figure 4.16: PSD of current fluctuations at different biases measured in a $L = 100\mu$m TLM device.

We first consider the sample with $L = 100\,\mu$m from the cell (2,2); the wafer map is reported in figure 4.19a. The device presents a total resistance of $R_T = 523\,\Omega$; the noise measurements have been carried out with $R_L = 3300\,\Omega$ and applying a several voltage bias points between 0.4 V and 4 V. The measurement results are shown in figure 4.16. As expected the noise level increases with the bias. The straight lines correspond to the fitting function $S_I = C/f^{\gamma}$, where γ is found to be very close to 1 ($\gamma = 0.98$) and C is a generic constant related to the applied bias. Notice that the peak measured around 170 Hz is not related to the device. It is an external signal with a fixed frequency that crosses the filters and/or the metallic shielding and it is measured by the system; this has been measured in other occasions with other samples and it does not depend on the applied bias. Since its source has not been found in order to definitively remove it, the noise data corresponding to the peak are ignored during the elaboration and the fitting parameter calculation.

From the literature on noise it is expected that $S_I \propto I^2$ and $C = S_I$ at $f = 1$ Hz. Therefore C is plotted versus I^2; results are shown in figure 4.17. The line slope is the parameter K of equation (4.10); this parameter can also be considered as the normalized power spectral density (S_I/I^2) of the noise at $f = 1$ Hz.

The same procedure has been applied to the other samples with shorter lengths in the cell (2,2). For all of them the found γ is in the range of 0.96 - 1.07 and S_I is proportional to I^2. In figure 4.18 the experimental data of the normalized noise at

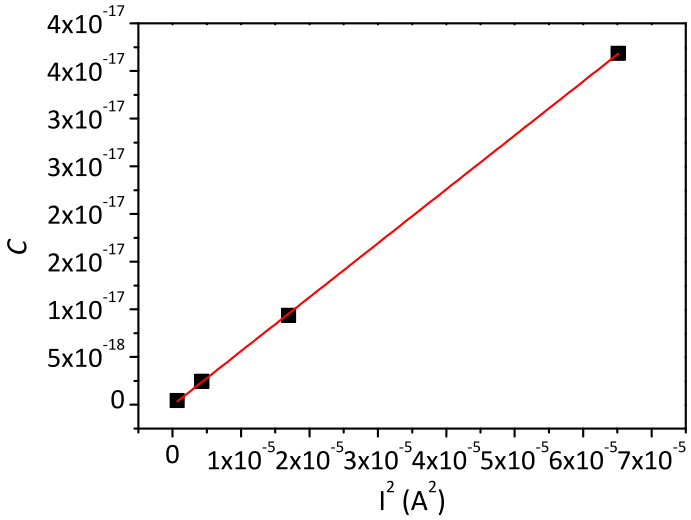


Figure 4.17: C vs. I^2 at 1 Hz; the symbols represent experimental data, the line is the fitting.

Wafer Name	MP10-02
ρ_C^* (Ωmm)	0.95
R_{sh} (Ω/□)	459
n_s (cm^{-2})	0.835·10^{13}
μ_{CH} (cm^2/Vs)	1840

Table 4.3: MP10-02 Hall measurement data.

1 Hz as function of L are reported. These data are then elaborated using (4.27). The constant values used in the equation are reported in table 4.3.

From the fitting $\alpha_{CH} = 5.33 \cdot 10^{-4}$ and $\lambda_{norm} = 5.9 \cdot 10^{-16}$ are obtained, where λ_{norm} is the parameter λ normalized by the contact area. In Fig. 4.18 the solid curve represents the resulting fitted curve. The two components of the total noise are also reported: the dotted line is the noise coming from the contact $S_{R_C}/(R_C + R_{CH})^2$ while the dashed line is the noise from the channel $S_{R_{CH}}/(R_C + R_{CH})^2$. It is possible to see that for $L > 40$ µm the noise is coming prevalently from the channel, while for $L < 20$ µm the noise from the contact is the main component in the total noise.

The analysis has been also extended to two other cells in the wafer (see Fig. 4.19.a) in order to see a possible correlation between the noise and the breakdown of the device (V_{bd}). In fact breakdown measurements show non-uniform breakdown voltage. In particular, low breakdown is observed over the wafer. Only the left part or the wafer has some devices with high breakdown voltage (see see Fig. 4.19.b). The V_{bd} in the cell (2, 2) previously measured is $V_{bd} < 100$ V; the other two cells selected for the noise

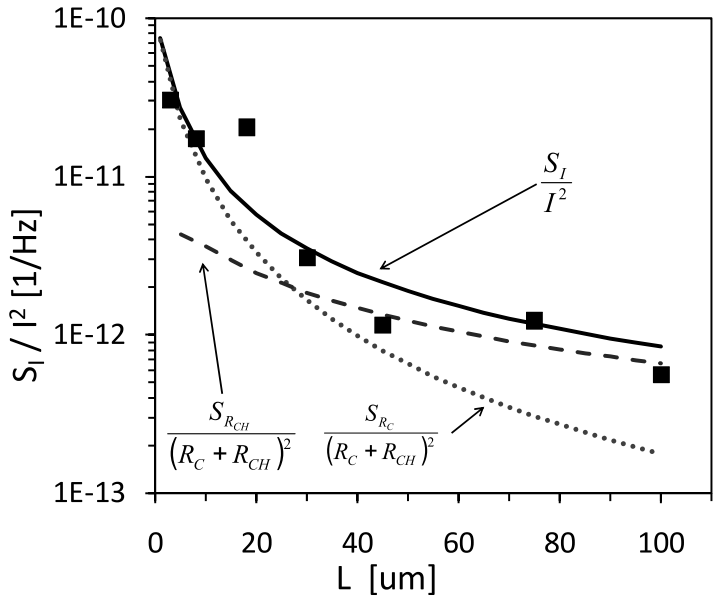


Figure 4.18: Normalized noise vs. TLM length at 1 Hz. Squares represent the experimental data, the continuous line represents the normalized total noise, the dotted line is the contact noise, the dashed line is the channel noise.

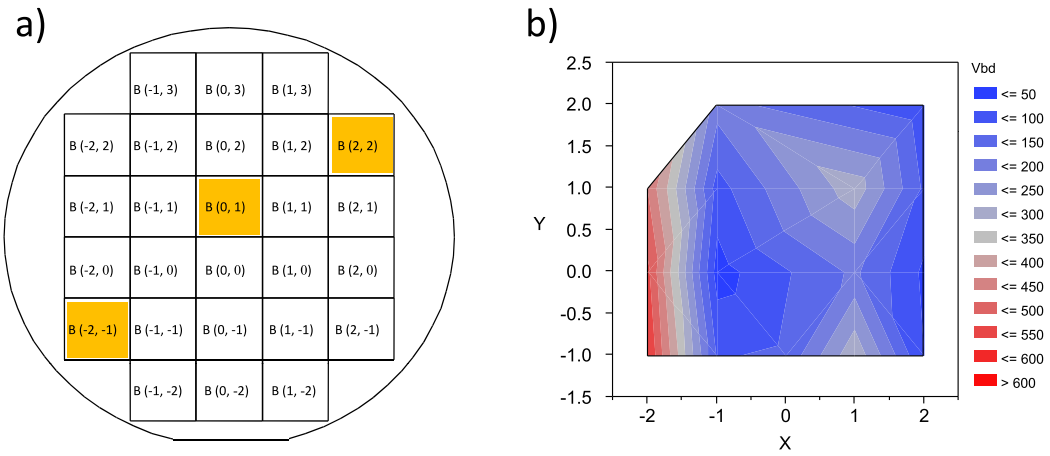


Figure 4.19: MP10-02 map: a) cell coordinates; b) Contour plot for V_{bd}, devices measured are transistors with L_G = 1.5 µm, L_{GD} = 32 µm, W_G = 100 µm.

measurements are (-2, -1), with V_{bd} < 400 V, and (0, 1), with V_{bd} < 250 V. Voltage breakdown has been measured by biasing the devices in pinch-off mode (V_{GS} = −10 V); the drain voltage has been swept until 1 mA/mm.

Results from the noise measurements are reported in Fig. 4.20, where the symbols represent the experimental data of S_I/I^2 and the curves the fitted functions. A significant difference among fitting parameters of the three cells is not visible (see Tab. 4.4); suggesting a weak correlation between the noise level in the measured TLMs and

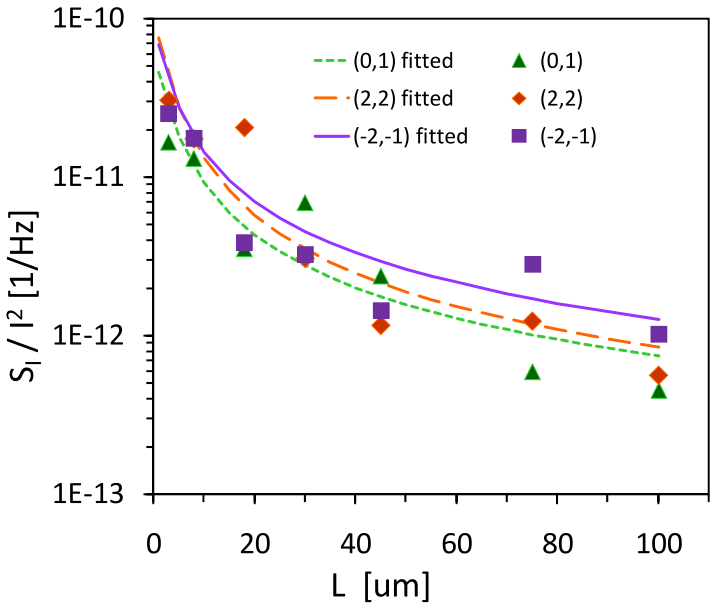


Figure 4.20: Normalized noise vs. TLM length at 1 Hz for three different sample of MP10-02 wafer. Symbols represent the experimental data, the continuous lines represent the results from the fitting function.

Cell Name	λ_{norm}	α_{CH}
(-2,-1)	$5.14 \cdot 10^{-16}$	$8.94 \cdot 10^{-4}$
(0,1)	$3.50 \cdot 10^{-16}$	$5.10 \cdot 10^{-4}$
(2,2)	$5.90 \cdot 10^{-16}$	$5.33 \cdot 10^{-4}$

Table 4.4: Fitting parameters (λ_{norm} and α_{CH}) for wafer MP10-02. λ_{norm} is the parameter λ normalized by the contact area, unit [$1/\Omega\mu m^2$].

the transistor breakdown. A possible explanation could be that the noise measured in TLM is related only to the ohmic contact and to the channel in the GaN layer; while the causes that are at the breakdown origin seem to be not measurable in TLM structures by means of the low frequency noise technique.

4.3.1.3 MP10-03 and MP11-03

Other two wafers with gold-free contacts have been characterized: MP10-03 and MP11-03. The MP10-03 has the same epi-layers and processing as MP10-02, except the ohmic alloy annealing temperature: 700°C instead of 650°C (see table 4.5). In the wafer MP11-03 devices are processed with a Al_2O_3 gate dielectric on top of the AlGaN layer. The epi-layer has been grown by Metal Organic Chemical Vapor Deposition (MOCVD) on a Czochralski 6-inch Si (111) substrate. The buffer layers (18% AlGaN,

40% AlGaN and 70% AlGaN) have been grown at 1080°C; the GaN, AlGaN barrier and in-situ Si_3N_4 have been grown at 1130°C. The spacer (AlN) was grown at 1130°C for 4 s. The overview of the epi-layers is shown in table 4.2. Electrical parameter from TLM and Hall structure are reported in table 4.6.

6" Wafer Name	MP10-03	MP11-03
In-situ Si_3N_4 (nm)	120	120
AlGaN (nm)	10 (18% Al)	10 (35% Al)
GaN (nm)	150	150
18% AlGaN (nm)	1018	1122
40% AlGaN (nm)	656	790
70% AlGaN (nm)	486	484
AlN (nm)	214	215
Si (111) (µm)	950	950
TBuffer (nm)	2374	2611
Ohmic metalization (nm)	Ti/Al/W (20/100/20)	Ti/Al/W (20/100/20)
Ohmic metalization anneal	700°C, 1 min	600°C, 1 min
Al_2O_3 deposition (nm)	15 , TMA+H_2O	15 , TMA+H_2O

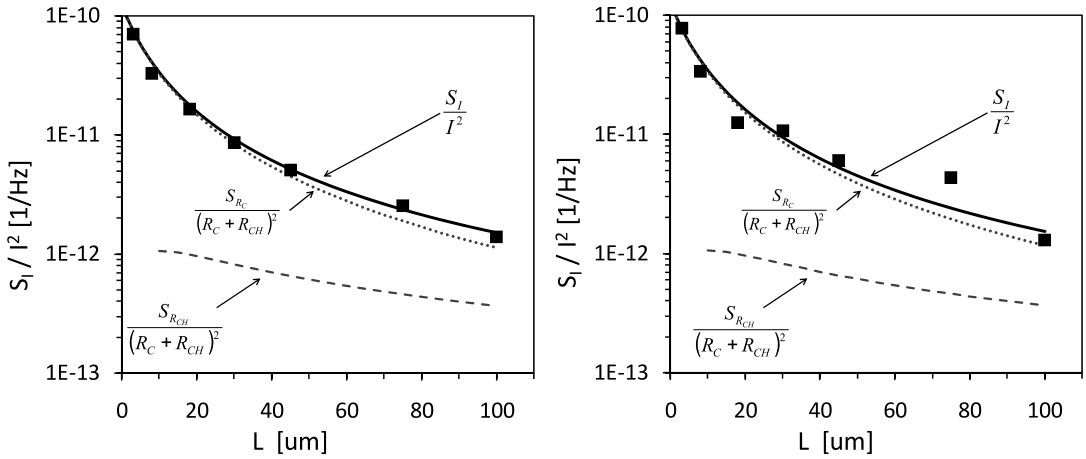
Table 4.5: MP10-03 and MP11-03 epi-layer description.

Wafer Name	MP10-03	MP11-03
ρ_C^* (Ωmm)	2.39	2.39
R_{sh} (Ω/□)	450	369
n_s (cm^{-2})	$0.81{\cdot}10^{13}$	$1.5{\cdot}10^{13}$
μ_{CH} (cm^2/Vs)	1837	1172

Table 4.6: MP10-03 and MP11-03 Hall measurement data.

The same measurements explained in the previous section have been repeated on these two wafers. For each wafer three TLM structures have been selected in different regions. Noise measurements have been performed at different bias on seven devices for each TLM structure. No devices have shown unexpected behavior: the normalized PSD of the noise is proportional to I^2 at constant frequency and γ is close to 1 for all the samples.

The results are reported in figure 4.21, where each experimental point (the squares in the graph) is calculated as the average of measurements on the tree regions of the wafer (as seen in MP10-02, also MP10-03 and MP11-03 do not present differences in



(a) MP10-03 **(b)** MP11-03

Figure 4.21: Normalized noise vs. TLM length at 1Hz for a) MP10-03 and b) MP11-03. Squares represent the experimental data, the continuous line represents the total noise, the dotted line is the contact noise, the dashed line is the channel noise.

the TLM noise along the wafer). It is interesting to notice that in both wafers the noise is coming prevalently from the ohmic contact: in fact the solid line, that represents S_I/I^2, has the same trend of the dotted line, representing $S_{R_C}/(R_C + R_{CH})^2$. The parameters derived from the fitting are reported in table 4.7.

Wafer Name	λ_{norm}	α_{CH}
MP10-03	$2.56 \cdot 10^{-16}$	$3.40 \cdot 10^{-4}$
MP11-03	$2.64 \cdot 10^{-16}$	$5.33 \cdot 10^{-4}$

Table 4.7: Fitting parameters (λ and α_{CH}) for wafer MP10-03 and MP11-03. λ_{norm} is the parameter λ normalized by the contact area, unit [$1/\Omega\mu m^2$].

4.3.1.4 GO21-B

The GO21-B is a piece of a GaN on Si wafer; the epi-layer was grown by Metal Organic Chemical Vapor Deposition (MOCVD) on a Czochralski 6-inch Si (111) substrate. The buffer layers, the GaN layer, the AlGaN barrier and the in-situ nitride have been grown at 1130°C. In table 4.8 the epi-layer structure is reported. Electrical parameter measured on TLM structures and Hall structures are reported in table 4.9. A particularity of this wafer is that both the ALD and the nitride under the gate have been removed before the gate processing; however this detail does not affect the measurements, since only TLM structures are considered (where there is no gate).

6" Wafer Name	MP10-03
In-situ Si_3N_4 (nm)	5
25% AlGaN (nm)	10
GaN (nm)	150
18% AlGaN (nm)	1064
40% AlGaN (nm)	835
70% AlGaN (nm)	454
AlN (nm)	219
Si (111) (µm)	950
TBuffer (nm)	2572
Ohmic metalization (nm)	Ti/Al/Mo/Au (30/60/35/50)
Ohmic metalization anneal	800°C, 1 min
Al_2O_3 deposition (nm)	10 , TMA+H_2O

Table 4.8: GO21-B epi-layer description.

Wafer Name	MP10-03
ρ_C^* (Ωmm)	0.68
R_{sh} (Ω/□)	411
n_s (cm^{-2})	$0.82 \cdot 10^{13}$
μ_{CH} (cm^2/Vs)	1804

Table 4.9: GO21-B Hall measurement data.

The GO21-B wafer has a different mask layout with different TLM lengths from the mask used for MP10-02, MP10-03 and MP11-03 wafers, as shown in Fig. 4.22. In this case the ohmic contact is 100×130 µm; the lengths selected for the measurements are 4, 5, 6, 8, 16, 32 µm.

TLM structures have been measured on different regions of the wafer (in total four samples). The devices have been biased at different voltages, to verify the relation $S_I \approx I^2$ and the $1/f$-trend (in this case $0.936 \leq \gamma \leq 1.17$). In figure 4.23 the normalized noise S_I/I^2 as a function of the TLM length is presented; the empirical data in the graph represent the average values for the different TLM structures (no relevant difference has

Figure 4.22: Wafer GO21-B mask layout of TLM structure; ohmic contacts are $W \times D$ = 100×130 µm.

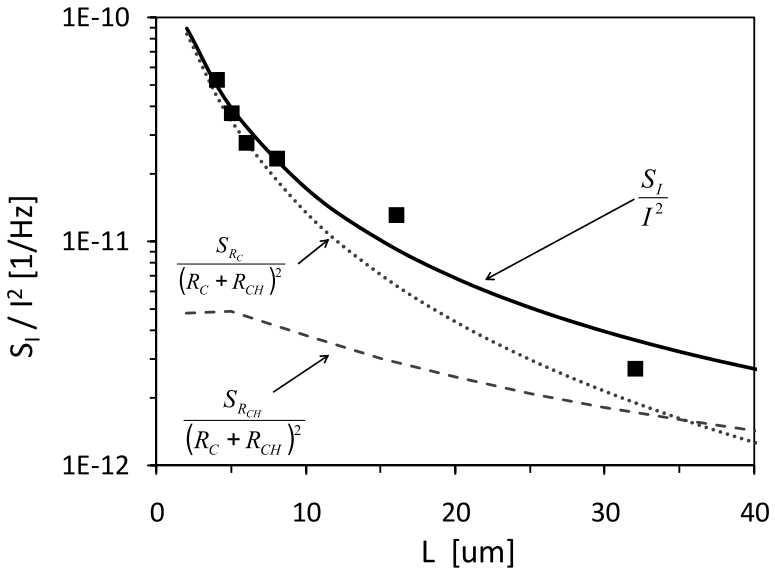


Figure 4.23: Normalized noise vs. TLM length at 1 Hz for wafer GO21-B. Squares represent the experimental data, the continuous line represents the total noise, the dotted line is the contact noise, the dashed line is the channel noise.

been found in samples coming from different regions of the wafer). From the fitting the two parameters are $\alpha_{CH} = 5.68 \cdot 10^{-4}$ and $\lambda_{norm} = 1.23 \cdot 10^{-15}$. In the graph also the two noise components are presented: $S_{R_C}/(R_C + R_{CH})^2$ dotted line and $S_{R_{CH}}/(R_C + R_{CH})^2$ dashed line.

4.3.1.5 Results discussion

In table 4.10 all the resulting parameters (λ_{norm} and α_{CH}) from the elaboration of the experimental data are reported, with the corresponding values of ρ_C^* and R_{sh} obtained from the IV measurements. We can see a slight variation of α_{CH} among the wafers, but it is not so relevant and not enough to give information about the quality of the wafers. A different observation can be done for the parameter λ: high values of λ correspond to low values ρ_C^* (see GO21-B), while low λ values correspond to high ρ_C^* (MP10-03 and MP11-03). The difference between the two λ is almost a order of magnitude.

Wafer name	ρ_C^* (Ωmm)	R_{sh} ($\Omega/\square$)	λ_{norm}	α_{CH}
MP10-02	0.95	459	$4.85 \cdot 10^{-16}$	$6.46 \cdot 10^{-4}$
MP10-03	2.39	450	$2.56 \cdot 10^{-16}$	$3.40 \cdot 10^{-4}$
MP11-03	2.39	369	$2.64 \cdot 10^{-16}$	$5.30 \cdot 10^{-4}$
G021-B	0.68	411	$1.23 \cdot 10^{-15}$	$5.68 \cdot 10^{-4}$

Table 4.10: Fitting parameters (λ and α_{CH}) for all measured wafers.

To explain this the following assumption can be done: hypothetically a good ohmic contact (low ρ_C^*) is characterized by a presence of defects in the transaction region between the metallic electrode and the semiconductor [22], defect that help the transit of carriers from the contact to the channel, but at the same time these defects create more fluctuations in the current and, therefore, more noise. On the other hand, poor ohmic contacts, where there are less defects, show a better quality in terms of noise.

4.4 Measurements on Transistors

A transistor is a more complicated structure than the TLM to analyze from the point of view of low-frequency noise measurements: the presence of the gate electrode introduces a different equivalent circuit for the channel and adds a new variables, i.e. the gate voltage, that can be used to change the conductivity of the channel. Moreover the gate current noise can be measured separately and also confused with the channel noise: in fact what seems to be fluctuations of the drain current I_D can simply be noise from I_G which is amplified. This situation is typical when studying bipolar transistors, where the base current is not negligible. In our case the presence of the dielectric under the gate drastically reduces the leakage current ($\approx 10^{-11}$ A); moreover $I_G/I_D < 10^{-4}$ when the device is biased close to the pinch-off, corresponding to the lowest drain current. In this condition the presence of the gate current can be ignored and it is possible to assume that the measured noise is due only to fluctuations in the channel [74].

The noise sources in the channel of a transistor are modeled as follows (see Fig. 4.24):

- S_{2R_C}: it represents the noise from the contact resistances R_C (assumed as only one noise source);
- S_{R_G}: it is the noise from the gated part of the channel (R_g);
- S_{R_d} and S_{R_s}: they represent the PSD of the noise from the two resistances in the ungated regions of the channel (R_d and R_s respectively).

Assuming uncorrelated noise sources, the total expression of the fluctuations in I_D is

$$\frac{S_I}{I^2} = \frac{S_{R_{tot}}}{R_{tot}^2} = \frac{S_{2R_C} + S_{R_d} + S_{R_s} + S_{R_g}}{(2R_C + R_d + R_s + R_g)^2} \tag{4.28}$$

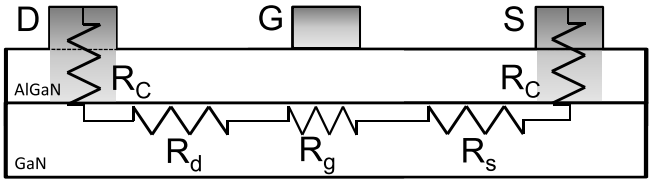


Figure 4.24: Schematic cross section of a transistor, resistances indicates are considered as noise sources: contact resistances R_C, gated channel resistances R_g, ungated channel resistances R_d and R_g.

While contact and ungated resistances are constant, R_g depends on the voltage V_{GS} applied to the gate [75]. The expression for R_{tot} becomes:

$$R_{tot} = R_U + \frac{L_G |V_{th}|}{W q n_s (V_{GS} - V_{th})} \tag{4.29}$$

where $R_U = 2R_C + R_d + R_s$, L_G and W are gate length and gate width, n_s the sheet carrier density in the channel, V_{th} the threshold voltage. The same consideration can be done on the total power spectral density:

$$S_{R_{tot}} = S_{R_U} + S_{R_g} \tag{4.30}$$

where S_{R_U} is the PSD of fluctuations from the ungated regions and contacts and it is a constant quantity; instead S_{R_g} depends on the carrier density in the channel under the gate, or, in other words, on the gate voltage. Experimental studies carried out in [63, 75] show that $S_I/I^2 \propto {V_G}^m$, where $V_G = V_{GS} - V_{th}$ and m is a coefficient that depends on the region where the transistor is biased. Four different regions are observed, as shown in Fig. 4.25:

1. $m = -1$: for bias close to the pinch-off, in this condition the total resistance and the $1/f$ noise are dominated by the resistance under the gate, ($R_g > R_U$) and by the channel resistance fluctuations ($S_{R_g} > S_{R_U}$);

2. $m = 2$: it is a particular condition where $R_g > R_U$ but the overall noise is dominated by the ungated region $S_{R_U} > S_{R_g}$, it usually indicates very poor connection technology;

3. $m = -3$: moving from the pinch-off to the ON condition the R_g starts to decrease ($R_U > R_g$) but the main source of noise is still the region under the gate ($S_{R_g} > S_{R_U}$);

4. $m = 0$: the channel is almost completely open ($R_U > R_g$) and the noise from ungated regions dominates ($S_{R_U} > S_{R_g}$).

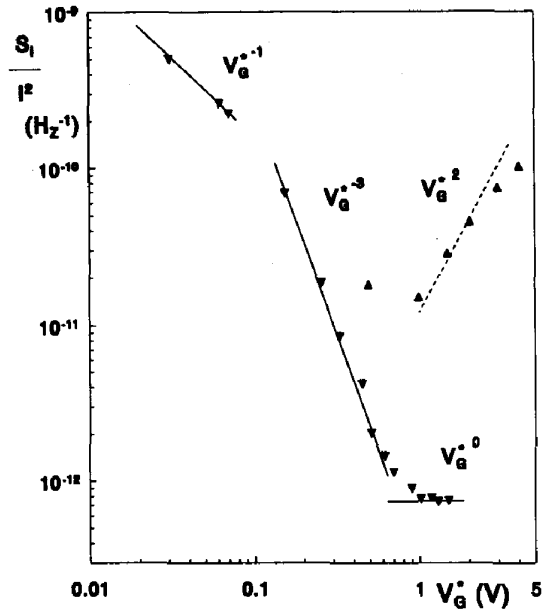


Figure 4.25: Normalized $1/f$ noise in the drain current at 20 Hz; ▼ symbols represent a MODFET with $L_G = 0.5\,\mu m$; ▲ symbols represent a n-channel MOS [63].

Case 1) and 4) are of particular interest for our analysis. When $m = -1$

$$\frac{S_I}{I^2} = \frac{S_{R_{tot}}}{R_{tot}^2} \approx \frac{S_{R_g}}{R_g^2} = \frac{\alpha_g}{N_g} \cdot \frac{1}{f} \tag{4.31}$$

where N_g is the number of channel carriers under the gate electrode; applying the same mathematical procedure see in eq. 4.24 we can calculate the Hooge's parameter for the gated channel region:

$$\alpha_g = f \frac{S_I}{I^2} \frac{L_G^2}{q\mu_{CH} R_g} \tag{4.32}$$

where R_g is proportional to V_{GS} as seen in (4.29).
When $m = 0$ the main sources of noise are located in the ungated/contact region; here a direct distinction between contact noise and ungated channel noise is not possible. Many authors simply consider negligible the noise from contacts having previously demonstrated with measurements on TLM that the $1/f$ noise is dominated by the channel component, see [76]. In this condition it is possible to find a Hooge's parameter for the ungated channel:

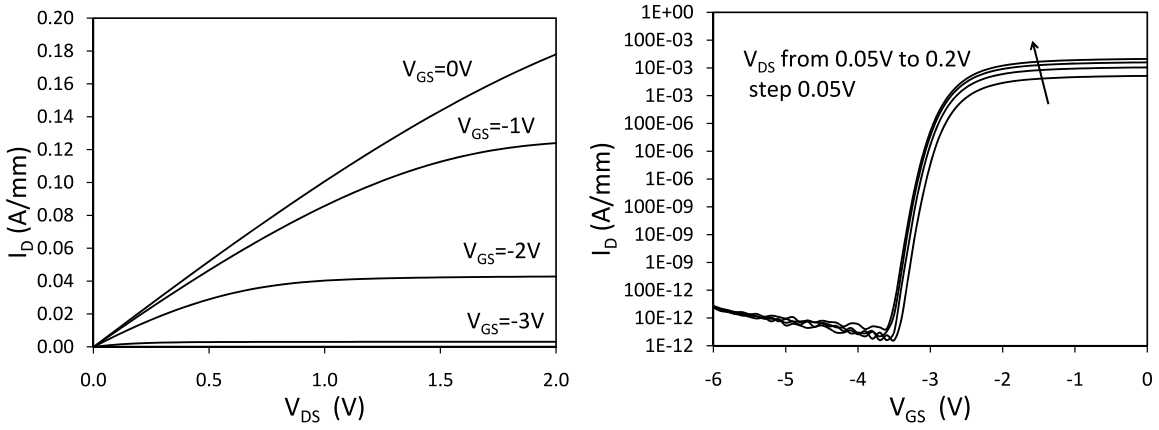
$$\alpha_U = f \frac{S_I}{I^2} \frac{(L_{SD} - L_G)^2}{q\mu_{CH} R_U} \tag{4.33}$$

where L_{SD} is the distance between source and drain.

4.4.1 Measurements on MP10-02

The devices selected for the noise measurements are one-finger transistors with the following dimensions: L_G = 2 µm, L_{GS} = L_{GD} = 6 µm, W = 100 µm. Three devices are selected form cells (-1, 2), (-2, 0) and (-2, 1).

Transistor have been biased at very low drain voltage, V_{DS} = 0.15V, in order to keep the device in ohmic behavior also for gate bias close to the pinch-off. The threshold voltage V_{th} is defined as the V_{GS} at I_D = 1 mA/mm, and it is almost equal for all the devices measured (≈ −2.75 V). I_G is in the order of magnitude of 10^{-11} A and $I_G/I_D < 10^{-5}$, since the lowest I_D at which the noise is measured is 100 µA, according to the definition of the threshold voltage. In figure 4.26a and 4.26b an example of the DC characteristics is reported.

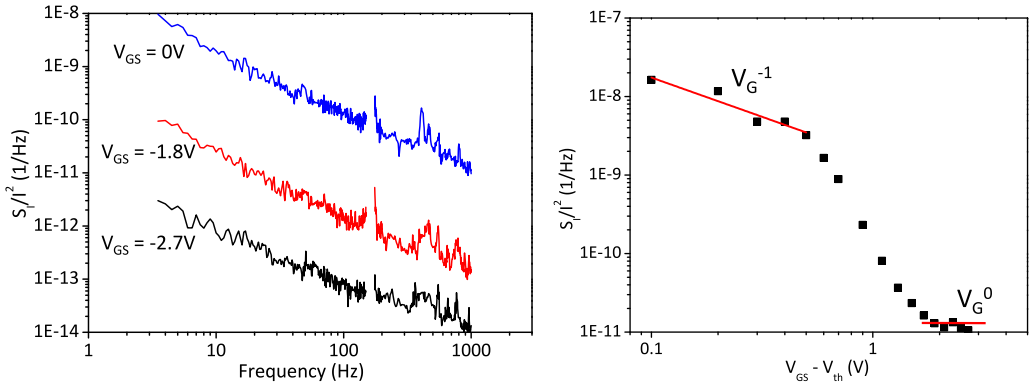


(a) $I_D - V_{DS}$ **(b)** $I_D - V_{GS}$

Figure 4.26: DC characteristics of the transistor from cell (-2, 0).

Figure 4.27 shows an example of noise measurement: on the left one see the S_I/I^2 vs. f for three different V_{GS} values (i.e. ON condition, semi-ON condition, near the pinch-off). The right graph shows the normalized noise S_I/I^2 at 1 Hz. The two parameters of interest are extracted from the V_G^{-1} and V_G^0 regions, obtaining $\alpha_g = 1.05 \cdot 10^{-2}$ and $\alpha_U = 6.27 \cdot 10^{-4}$. The Hooge's parameter for the ungated region is in the same order of magnitude of the one found for the TLM structures, see Tab. 4.4. This is a confirmation of the validity of the measurement. The same procedure has been repeated for two other transistors from cell (1, 2) and (-2, 1), see Fig. (4.28).

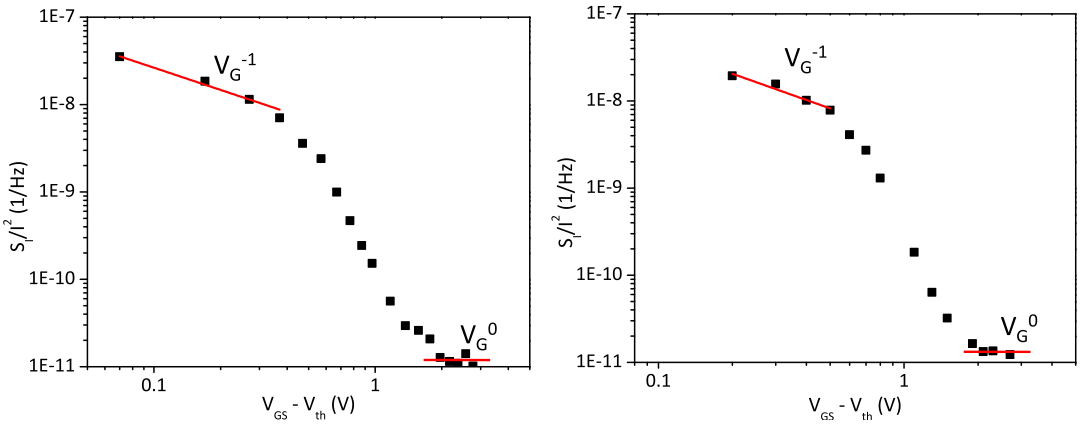
In table 4.11 all the values from the data elaboration are reported; as seen for TLM, a relevant difference between transistors from different cells does not exist, this is a confirmation of homogeneity along the wafer of the channel/barrier layer quality in



(a) Normalized $1/f$ noise for three different V_{GS} at V_{DS} = 0.15 V.

(b) S_I/I^2 at 1 Hz as a function of V_{GS} at V_{DS} = 0.15 V; V_{th} = 2.7 V.

Figure 4.27: Dependence of $1/f$ noise as a function of V_G in a one finger transistor from cell (-2, 0).



(a) S_I/I^2 at 1 Hz as a function of V_{GS} at V_{DS} = 0.15 V; V_{th} = 2.77 V

(b) S_I/I^2 at 1 Hz as a function of V_{GS} at V_{DS} = 0.15 V; V_{th} = 2.7 V

Figure 4.28: Dependence of $1/f$ noise as a function of V_G in a one finger transistor from cell (1, 2) on the left and from cell (-2, 1) on the right.

Cell	α_g	α_U
(1,2)	$1.48 \cdot 10^{-2}$	$6.24 \cdot 10^{-4}$
(-2,0)	$1.05 \cdot 10^{-2}$	$6.27 \cdot 10^{-4}$
(-2,1)	$2.54 \cdot 10^{-2}$	$7.28 \cdot 10^{-4}$

Table 4.11: Fitting parameters (α_g and α_U) for all measured transistors from wafer MP10-02.

terms of noise. Looking to the average value of $\overline{\alpha_U} = 6.6 \cdot 10^{-4}$) it is possible to see that it is comparable to the average value found for the TLM structures $\overline{\alpha_{CH}} = 6.46 \cdot 10^{-4}$ (see Tab. 4.10), which means that in transistors the noise from the contacts is negligible in respect to the noise from the ungated part of the channel.

The fact that a correlation between drain current fluctuations and device breakdown has not been probed may be related to the distance of the channel from where the traps are effectively located. If the trapping states (or defects) which cause the premature breakdown of the device are located at the interface gate-dielectric/AlGaN-barrier, a 10 nm AlGaN barrier is too thick to allow the interaction between channel carriers and trapping states (for example by tunneling of electrons from the channel to the interface states). Thus the fluctuations of the channel current do not suffer from the eventual presence of these defects and in this case the noise measurement cannot be used as a diagnostic tool.

4.5 Gate Current $1/f$ Noise

Finally a technique to measure the noise related to the gate leakage current I_G is presented. The measurement is carried out by biasing the gate in reverse condition, keeping both source and drain or only one of them connected to the ground. The power spectral density of the fluctuations in the current (S_{I_G}) have been measured as done for the channel current. In [77] a figure of merit for the quality of MOS gate contact is proposed:

$$GNP = \frac{S_{I_G}}{I_G^2} fA \tag{4.34}$$

where GNP is the Gate Noise Parameter, I_G the gate current and A the gate area. The GNP has a double meaning: it is an empirical parameter (as the Hooge's parameter a_H) that describe the intensity of the noise, as well as a theoretical parameter related to the trap density in the dielectric under the gate or at the interface dielectric/barrier layer [78]. Measuring the I_G noise can be very interesting since it allows a diagnostic of traps located near the gate and therefore too far from the channel to induce fluctuations on I_D.

Measurements have been carried out on two samples of MP10-02 wafer; since the system requires a current of ≈ 100 nA in order to obtain a reliable noise measurement, transistors with a big area ($A = 500 \times 1.5$ µm) have been selected and the gate bias between −1 V and −7 V have been applied. Results are shown in Fig. 4.29, where the GNP is plotted as function of I_G.

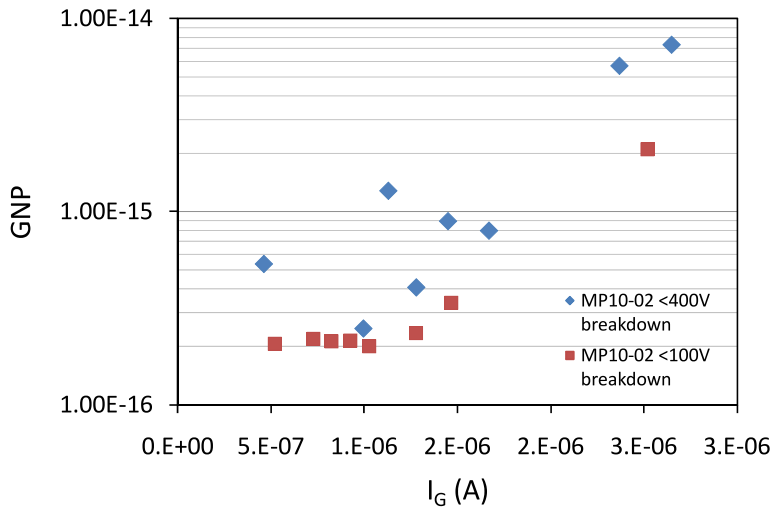


Figure 4.29: Gate noise parameter (GNP) for two samples from MP10-02 wafer; diamonds represent experimental data for the device with $V_{bd} < 400\,\text{V}$, squares represent experimental data for the device with $V_{bd} < 600\,\text{V}$.

The two samples are taken one from a cell with high breakdown voltage and the other from a cell with low breakdown voltage. A slight difference between the two samples can be noticed, but it does not allow to make hypothesis to explain the difference. In fact measured samples are only two, selected among other for their high leakage: normally transistors from MP10-02 wafer have a $I_G \approx 10\,\text{pA}$, a level too low to be measured by the system.

4.6 Conclusions

Measurements on TLM have shown that the measured noise can be divided in the two components: one coming from the channel and one from the ohmic contact. A parameter (λ) has been defined to characterize the quality of ohmic contact. By measuring different samples with different contact resistances it has been seen that high values of λ (meaning high levels of noise coming from the contacts) correspond to low values of the specific contact resistance (ρ_C^*), while low λ values correspond to high ρ_C^*. The hypothesis made to explain this difference is that a good ohmic contact is characterized by a presence of defects at the interface metallic electrode/GaN channel which help the transit of carriers, but at the same time these defects create more fluctuations in the current and, therefore, more noise. Obviously this explanation needs a deeper investigation. On the other hand measurements on HEMTs have shown the typical behavior described in literature for the field-effect transistors; allowing the calculation

of the Hooge's parameters for the gated region and the ungated region of the channel.

5

Long Term Stress

In this chapter we will present the results of a DC-life test carried out on AlGaN/GaN samples. The reliability is an important aspect for the complete characterization of a device and it allows the identification of the degradation mechanisms that accelerate the ageing of the sample. Many of recent studies on HEMT reliability are carried out by means of accelerated step-stress, as it will be shown on the next chapter; but they do not allow a complete and clear explanation of the degradation physical process, often causing a debate on the scientific community. For this reason the long term stress remains a very useful reliability test, since mechanisms involved in the sample degradation can be identify with more accuracy than an accelerated test [41, 42, 43].

Several transistors have been submitted to a 1000 h stress at three different bias conditions and at three different junction temperatures. The issues identified during the work are clearly related to the high levels of gate leakage current reached during the stress.

5.1 The HYPHEN Research Project

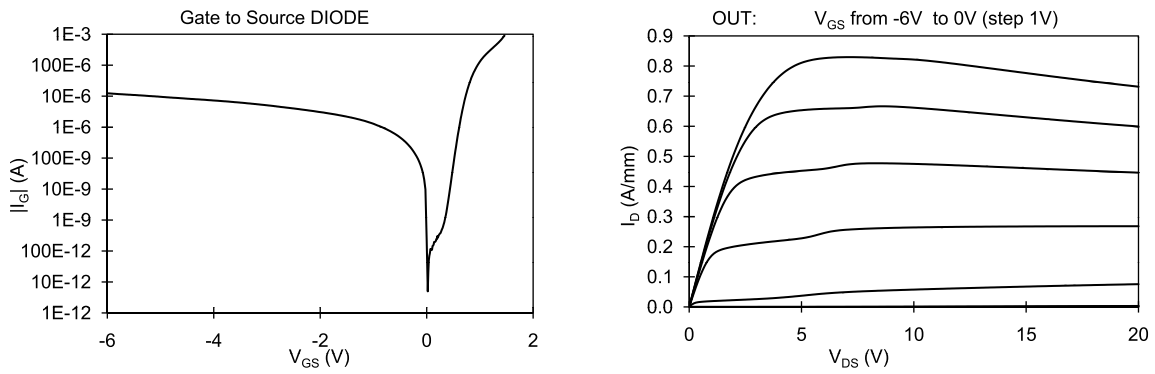
The wafer used in this experiment is realized with a SopSiC substrate (Silicon on polycrystalline SiC, see section 2.3) developed in the frame of the European HYPHEN Project [79]. The aim of this project was to *"develop and evaluate a new type of composite substrate based on silicon and silicon carbide materials, able to provide a cost efficient solution that will leverage the use of advanced high power devices in wireless communication systems"*. As partner of this project, some of the characterization activities have been carried out at the Department of Information Engineering in Padova; the main activities were about DC characterization, trapping effects analysis, measurement of the power efficiency and evaluation of the overall reliability and the degradation

mechanisms. Several wafers have been tested, with both SopSiC and SiCopSiC substrates; following the evolution and the assessment of this new technology [7, 80]. The experiment shown in this chapter is one of the main experiment on reliability of AlGaN/GaN HEMTs carried out during the project.
The final target of the HYPHEN project was to demonstrate that the use of a hybrid substrate does not affect the performance of the devices; in fact the reliability results presented in the follows are related only to the epitaxial process and they are independent from the adopted substrate.

5.2 Sample Description and Electrical Characterization

The tested devices are passivated AlGaN/GaN HEMTs grown by Molecular Beam Epitaxy (MBE) on SopSiC substrate. The multilayer structure is composed by a GaAlN nucleation layer, a GaN buffer layer (1.5 nm), an AlGaN barrier layer (23 nm thickness with 31% of Al content) and finally a GaN cap layer (2 nm).

DC and pulsed $I-V$ measurements have been carried out on the devices to fully characterize the device performances. The DC characterization shows good drain current levels ($\approx$ 0.8A/mm) and a gate leakage currents in the order of 10 – 100µA/mm, see Fig. 5.1. The typical threshold voltage is about −4.5 V. The pulsed characterization not shows presence of current collapse due to trapping phenomena on the tested devices, see Fig. 5.2; the slump ratio calculated at V_{DS} = 5 V is $\{S.R.\}_{I_D}$ = 0.95.



(a) Gate to Source diode.

(b) $I_D - V_{DS}$ at V_{GS} from 0 to −1 V.

Figure 5.1: Electrical DC characteristics of a representative device with L_G = 0.7 µm, W_G = 0.7 µm and L_{shield} = 1.3 µm (length of the elongation over the gate-drain region of the Γ-gate electrode).

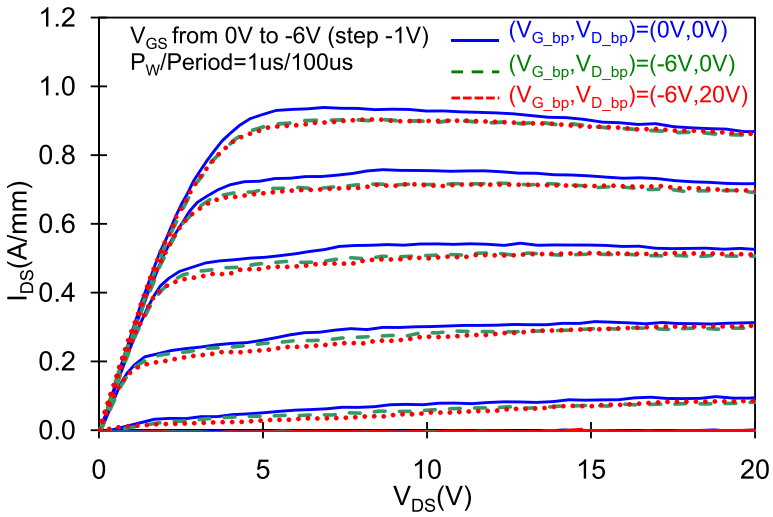


Figure 5.2: I_D vs V_{DS} output curves measured in pulsed condition for a representative device, L_G = 0.7 µm, W_G = 0.7 µm and L_{shield} = 1.3 µm. Three different quiescent bias point are adopted: (0 V, 0 V), (−6 V, 0 V) and (−6 V, 20 V).

RF power measurements have been carried out to evaluate the Power Added Efficiency (PAE) of the HEMT devices. Measurements have been carried out by means of a load-pull system based on an Agilent PNA Vector Network Analyzer and a PAF Dragon Load-Pull System. Measurements have been carried out at *Università di Modena e Reggio Emilia*. Power measurements have been performed in continuous wave (CW) behavior at 2 GHz on selected devices; the bias condition adopted was V_{DS} = 20 V and I_D = 10%I_{DSat}. Devices periphery were W_G = 320 µm and L_G = 0.3 µm. Tested devices presented very high PAE and output power density: PAE=54.3% and P_{out} = 4.1W/mm; see Fig. 5.3 for a representative device. These results are very good and encouraging, since they represent an improvment of this new GaN-technology on hybride substrates; in fact others recent researches on this subject have presented devices with PAE=28% and power density of 1.15 W/mm in [81] and PAE=34.7%, P_{out} = 5 W/mm in [82].

5.2.1 Thermal Resistance Evaluation

A measurement of the thermal resistance (R_{th}) has been carried out on selected devices by means of a custom technique. The measurement has been performed in two steps: a) calibration measurement and b) junction temperature measurement [83]. During the calibration the device has been kept in a temperature-controlled oven in order to measure the I_D at V_{GS} = 0 V for different ambient temperature (T_{amb}). The output characteristic has been obtained by biasing the sample with a pulsed V_{DS} from 0 to

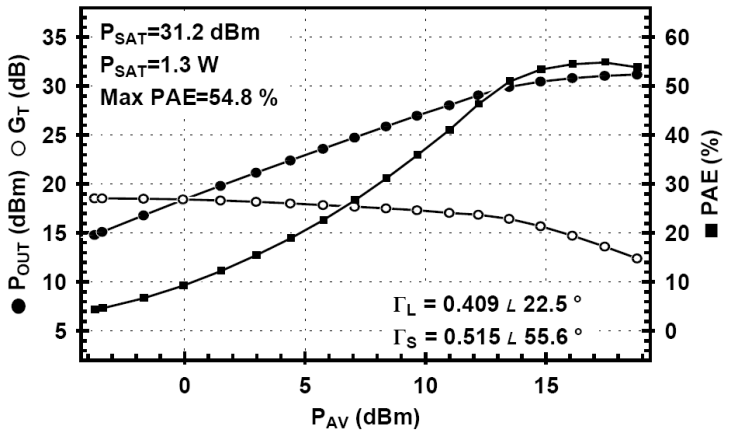
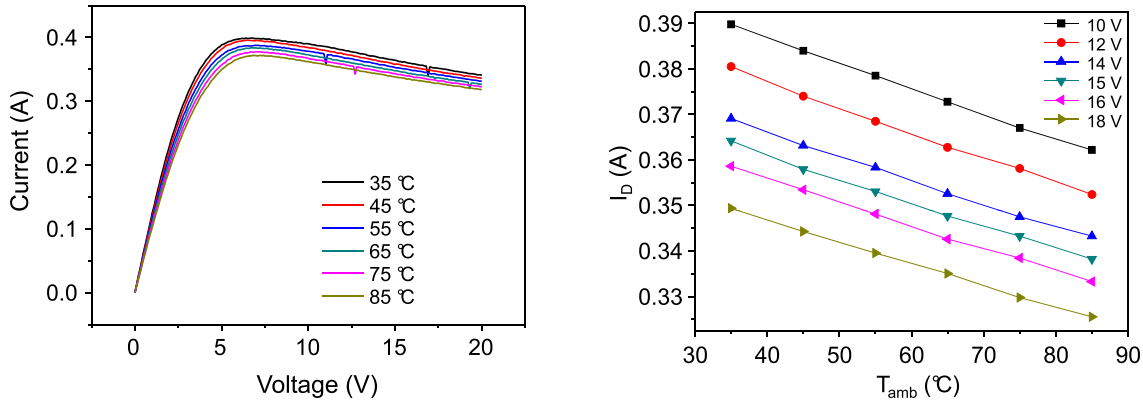


Figure 5.3: Load pull measurement for a representative device. The output power is 4.1 W/mm at V_{DS} = 20 V and I_D = 10%I_{DSat}.



(a) I_D vs. V_{DS} at V_G = 0 V for T_{amb} from 35°C to 85°C, step 10°C.

(b) I_D vs. T_{amb} at V_{GS} = 0 V for different V_{DS} from 10 V to 18 V

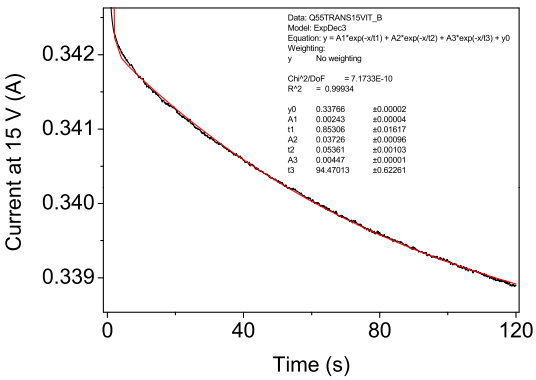
Figure 5.4: First step of R_{th} measurement - calibration. Drain current is measured at different T_{amb} conditions.

20 V at different temperature (from 35°C to 85°C, 10°C step); the pulse width was kept at 100 µs with a duty-cycle of 10% to reduces the self-heating of the device and, with a certain approximation, the junction temperature (T_j) can be considered equal to T_{amb}; the result of the measurements is shown on Fig. 5.4a. From obtained data the I_D vs. T_{amb} diagram is drawn to show the relation between these two quantities, see Fig. 5.4b. The relation is very close to linear and it can be fitted by the equation: $I_D = A + B \cdot T_{amb}$ where A and B are fitting parameters.

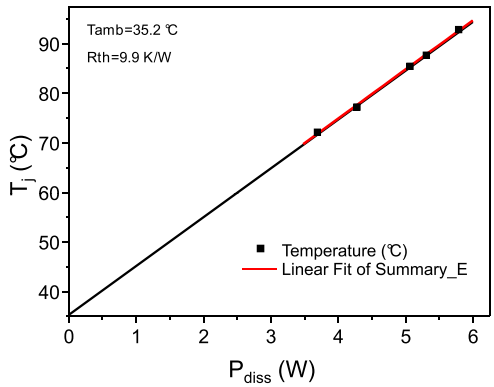
For the second step (junction temperature measurement) the device has been biased with a constant V_{DS} at fixed ambient temperature (35°C) and the drain current

transient has been extrapolated. As shown in Fig. 5.5a, the I_D decrease follows an exponential trend and reaches a final operative value. This decrease is due to the self-heating of the device, therefore the final value of drain current is related to the final junction temperature. At the end, from the relation written above, it is possible to calculate the junction temperature of the device. Since the current transient is quite long, the operative value of I_D is found by an exponential fitting of the 3^{rd} order.

Five I_D transients have been measured for five different V_{DS} values, for each of these the related T_j has been calculated. The results are shown in Fig. 5.5b, where for the x-axis represents the dissipated power and for y-axis the temperature. On the same diagram a linear fit is shown; the evaluated R_{th} is 9.9 K/W. Also extending the linear fit to the y-axis (black line) it is possible to see that the temperature at P_{diss} = 0 W is equal to 35°C, close to the ambient temperature (35.2°C). This could be considered as an indication of the accuracy of measurements. By the way, the pulse width used for the calibration measurement is not very short to ensure the absolute absence of self-heating of the device. In addition thermal measurements have been performed on a home-made copper base plate while the DC life-test has to be performed in a burn-in system bench, hence the thermal conductivity could be different. Therefore the calculated R_{th} could be underrated and in order to adopt a more reasonable value we have finally set the R_{th} value to 15 K/W.



(a) Transient of I_D at V_{GS} = 0V and V_{DS} = 15 V. Black line: measured data, red line: exponential fit.



(b) T_j vs. P_{diss}; red line: linear fit, black line: extension of linear fit; R_{th} = 9.9K/W

Figure 5.5: Second step of R_{th} measurement - junction temperature measurement.

5.2.2 Preliminary Reliability Evaluation

A preliminary short-term stress experiment has been carried out in order to evaluate in first approximation the robustness of the transistors and to identify the correct biasing point for the following long-term DC life test. In this experiment the device has been biased in a three different conditions: with completely open-channel ($V_{GS} = 0\,\mathrm{V}$), semi open-channel ($V_{GS} \approx V_{th} + 1\,\mathrm{V}$) and closed channel ($V_{GS} < V_{th} - 2\,\mathrm{V}$). The drain voltage has been increased from a initial value of 16 V up to 30 V with a step of 2 V each hour of stress (8 h of stress); complete DC characterization have been carried out at the beginning end after each hour of stress, before the application of the new bias condition. The selected devices submitted to the step-stress test have 0.3 µm and 0.5 µm gate length, 100 µm of gate width (two fingers transistors), the gate electrode is a Γ-gate. In the follows the results of the stress are presented.

"*Open channel*" condition ($V_{GS} = 0\,\mathrm{V}$)

Device submitted to this test condition does not show any important variation on the main DC characteristics (gate leakage, maximum drain output current, transconductance peak and threshold voltage shift); but all tested devices failed the experiment when the drain voltage was brought up to 28 V and in other cases to 30 V, moreover the drain current shows a decreasing trend before the device failure, see Fig. 5.8a where $I_{D-stress}/I_{D-virgin}$ represents the ratio between the drain current measured after the single step of stress ($I_{D-stress}$) and the drain current measured on the fresh device ($I_{D-virgin}$). Certainly the high power dissipated in these two last bias conditions and the fact that the device temperature was not kept under control have caused the failure of the sample. On thew other hand the variation of the gate current during the stress does not show heavy degradation, see Fig. 5.6b where $I_{G-stress}/I_{G-virgin}$ represents the ratio between the gate current measured after each step of stress ($I_{G-stress}$) and the initial gate current ($I_{G-virgin}$).

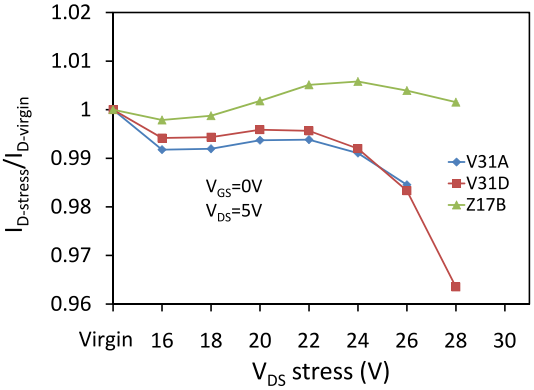
"*Semi-open channel*" condition ($V_{GS} \approx V_{th} + 1\,\mathrm{V}$)

No relevant degradation effects are visible on the samples submitted to this stress condition; all the DC measurements carried out at the end of the stress show very little variation (as example, see the drain current in Fig. 5.7a). On the other hand one of the three device shows a large increase on the gate leakage current, six times higher than the initial value, see Fig. 5.7b.

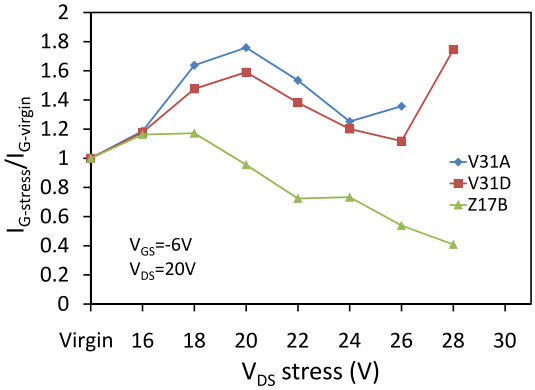
"*Closed channel*" condition ($V_{GS} < V_{th} - 2\,\mathrm{V}$)

All the samples show an increase on the gate leakage (from four to six times higher than the starting value, see Fig. 5.8b), while the others parameters are closed to the initial values of the fresh device (drain current is reported as example in Fig. 5.8a).

The high leakage found at the end of the stress can be related to the high electrical field applied to the device.

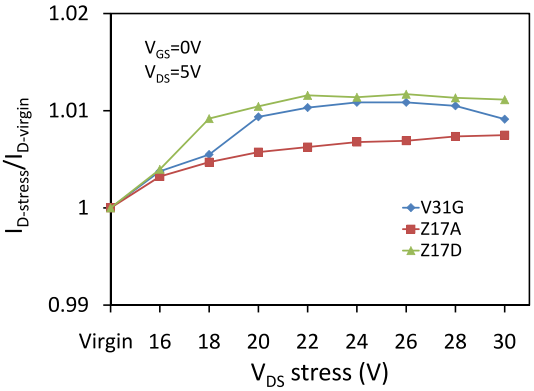


(a) Normalized I_D at V_{DS} = 5V, V_{GS} = 0V.

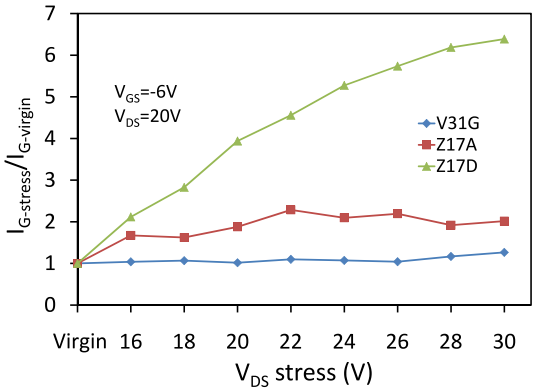


(b) Normalized I_G measured at V_{DS} = 20 V, V_{GS} = −6 V.

Figure 5.6: Variation during the short-term stress experiment of the drain current and the gate leakage for three different transistors submitted to "open channel" condition stress (V_{GS} = 0 V). V_{DS} is increased of 2 V each hour. Measured parameters are normalized to the initial value of the untreated device.

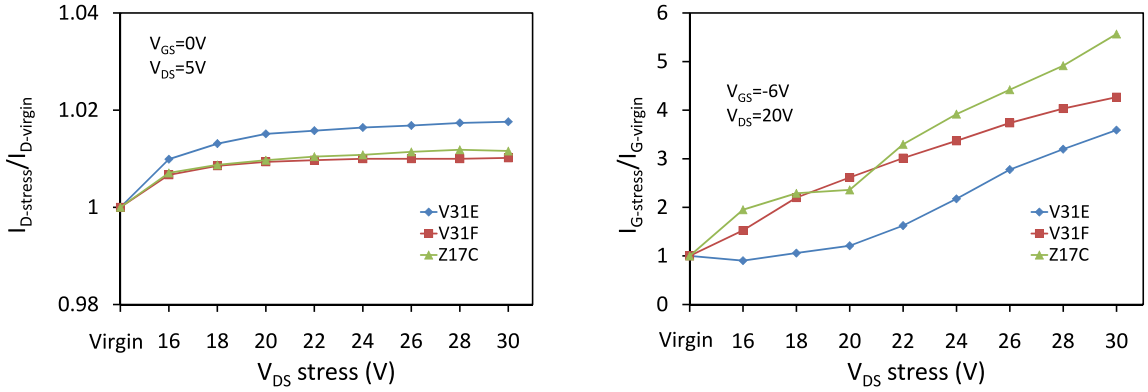


(a) Normalized I_D at V_{DS} = 5V, V_{GS} = 0V.



(b) Normalized I_G measured at V_{DS} = 20 V, V_{GS} = −6 V.

Figure 5.7: Variation during the short-term stress experiment of the drain current and the gate leakage for three different transistors submitted to "semi-open channel" condition stress ($V_{GS} \approx V_{th} + 1$ V). V_{DS} is increased of 2 V each hour. Measured parameters are normalized to the initial value of the untreated device.



(a) Normalized I_D at V_{DS} = 5V, V_{GS} = 0V.

(b) Normalized I_G measured at V_{DS} = 20 V, V_{GS} = −6 V.

Figure 5.8: Variation during the short-term stress experiment of the drain current and the gate leakage for three different transistors submitted to "closed channel" condition stress ($V_{GS} < V_{th} - 2$ V). V_{DS} is increased of 2 V each hour. Measured parameters are normalized to the initial value of the untreated device.

5.3 DC-Life Test

The long-term DC life test consists in submitting devices to an electrical stress combined with a thermal stress. Having in mind the results obtained from the step-stress experiment and the R_{th} measurements, three bias conditions with the respective junction temperature have been selected (see Tab. 5.1):

- ON-state (V_{DS} = 15 V, $I_D = I_{Dsat}/2$, T_j = 180°C) corresponds to the situation in which devices are subjected to high channel temperature but with restrained electric fields;
- SEMI ON-state (V_{DS} = 30 V, $I_D = I_{Dsat}/4$, T_j = 180°C) presents the same power dissipation of the ON-state condition and also the same junction temperature

Channel stress condition	V_{DS} (V)	I_{Dsat} (A)	% of I_{Dsat} (%)	P_{DISS} (W)	R_{th} (°C/W)	Baseplate temp (°C)	T_j (°C)
ON	15	0.195	50.8	2.925	15	140	184
SEMI ON	30	0.0975	25.4	2.925	15	140	184
OFF	40	0.024	6.3	0.96	15	80	94

Table 5.1: Adopted bias and thermal condition for 1000 h DC-life test. The final junction temperature is determined by the dissipated power an by the temperature of the baseplate where the device is mounted: $T_j = P_{DISS} \cdot R_{th} + Baseplate\ temp$.

but in this case the gate-to-drain electric field is bigger and hence also the gate leakage current;

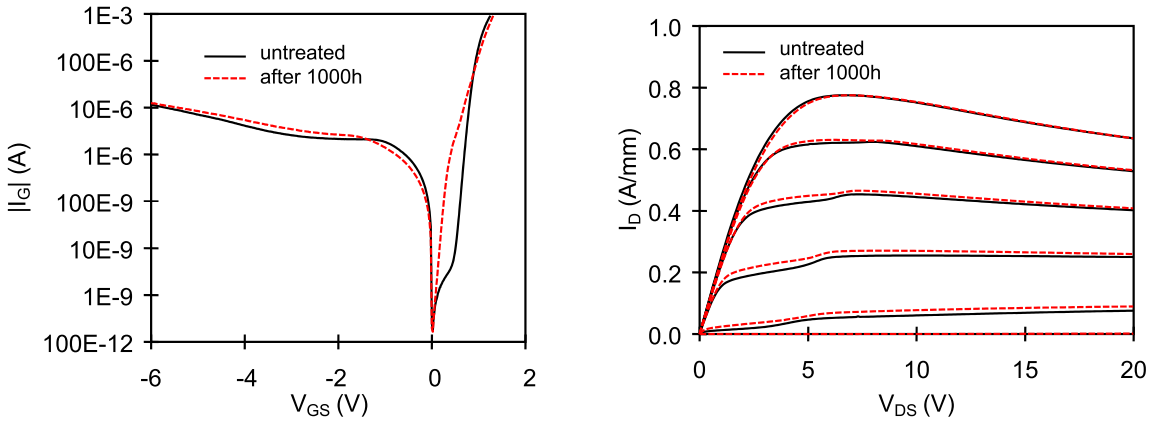
- OFF-state (V_{DS} = 40V, $I_D = I_{Dsat}/16$, T_j = 94°C) corresponds to the case in which drain current is very low and hence the power dissipation but, on the other hand, is subjected to very high electric fields.

Devices have been submitted to a total of 1000 hours of stress; intermediate DC measurements have been undertaken at the 1^{st}, 5^{th}, 10^{th}, 100^{th}, 500^{th} and 1000^{th} hour of stress. Measured devices are 8 fingers transistors with the following peripheries: width (W_G) of 480 µm, gate length (L_G) equal to 0.3 µm and a field plate length (L_{shield}) of 1.3 µm. The tested transistors were mounted and bonded in a EGIDE package. A set of four devices have been selected for the ON-state, other four for the SEMI ON-state, and six for the OFF-state. Two remaining samples have been left unstressed as backup.

5.3.1 Results and Discussion

ON-state stress (V_{DS} = 15 V, $I_D = I_{Dsat}/2$, T_j = 180°C)
After 1000 h of ON-state stress no remarkable DC degradations are present. In Fig. 5.9 the gate to source diode characteristics and the drain current output characteristics are reported. All devices submitted to ON-state bias condition have reached the end of the 1000 h DC life test.

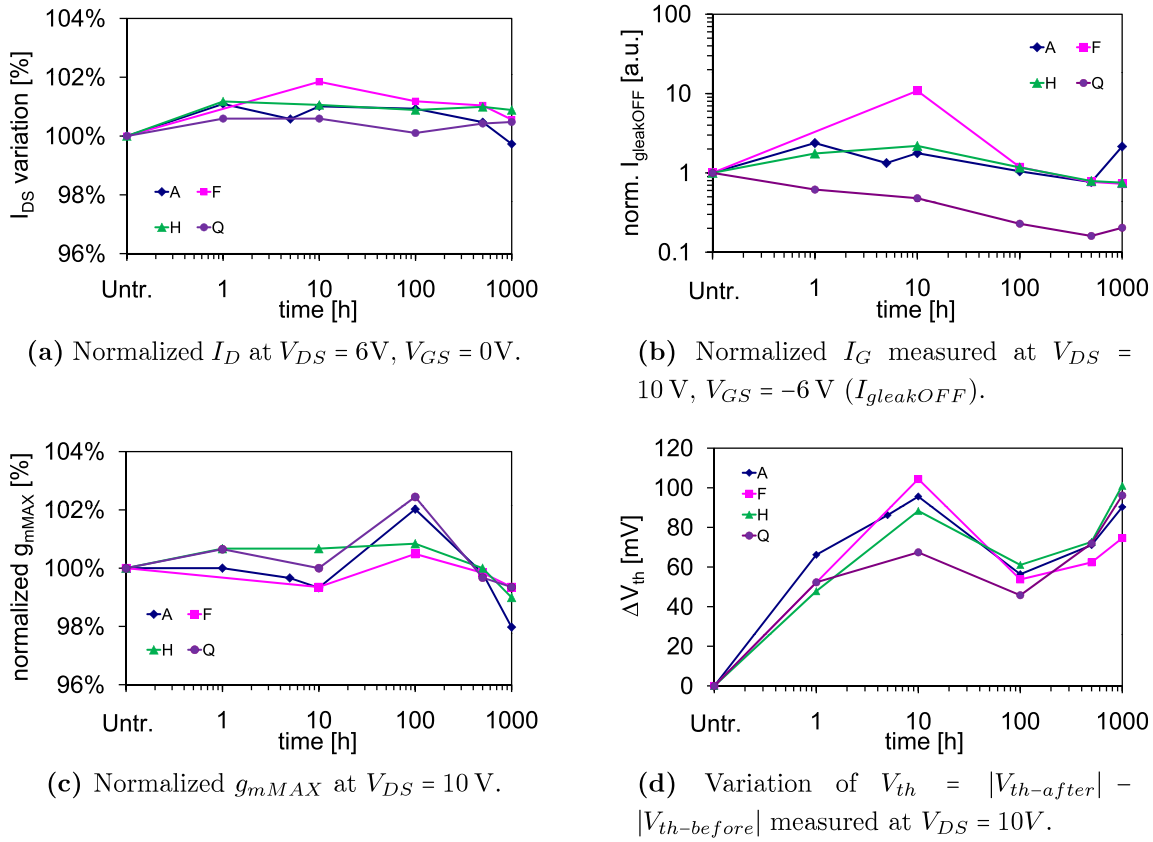
In the following diagrams, the main DC characteristics measured for each device submitted to ON-state stress are reported. Devices show a slight increase of the drain



(a) Gate to Source diode.

(b) $I_D - V_{DS}$ at V_{GS} from 0 to −1 V.

Figure 5.9: Electrical characteristics of a representative device before (continuous lines) and after (dashed lines) 1000h of ON-state stress at I_D = 0.195A and V_{DS} = 15V. Junction temperature was kept at 184°C during the stress.



(a) Normalized I_D at V_{DS} = 6V, V_{GS} = 0V.

(b) Normalized I_G measured at V_{DS} = 10 V, V_{GS} = −6 V ($I_{gleakOFF}$).

(c) Normalized g_{mMAX} at V_{DS} = 10 V.

(d) Variation of V_{th} = $|V_{th-after}|$ − $|V_{th-before}|$ measured at V_{DS} = 10V.

Figure 5.10: Variation during the stress experiment of the main DC parameters for the transistor submitted to ON-state stress (the letters indicate the different samples). Measured parameters are normalized to the initial value of the untreated device.

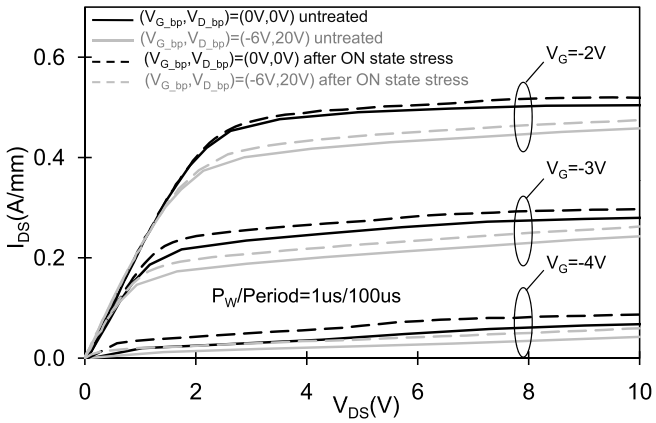
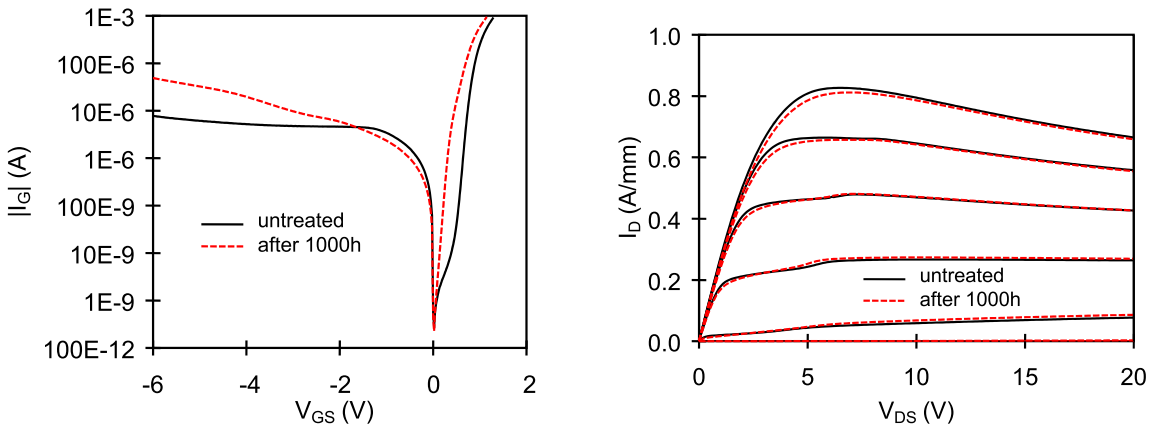


Figure 5.11: I_D vs V_{DS} output curves measured in pulsed condition for a representative device. Two different quiescent bias points are adopted: (0 V, 0 V) and (−6 V, 20 V). Continuous lines represent the measurement before stress, dashed line after the 1000 h ON-state DC life test.

current, lower than 2% of the initial current, see Fig. 5.10a. No relevant degradation on the gate leakage current is visible, see Fig. 5.10b. Moreover on some device a decrease of the leakage is measured, only device "A" shows a relevant increase on the I_G leakage. The peak of transconductances ($g_{m_{MAX}}$) measured at V_{DS} = 10 V (Fig. 5.10c) does not show high variation (less than 3%). During the stress a little voltage threshold shift occurs, less than 120mV, Fig. 5.10d, where ΔV_{th} is calculated as the difference between the value after ($V_{th-after}$) and before stress ($V_{th-before}$). Dynamic characterizations have been also carried out. Results obtained for a representative device are reported on Fig. 5.11. As already observed from the DC characterisation, there is a slight increase in drain current; but no worsening of the current collapse effect is visible, which means that the stress does not induce the creation of trapping-states.

OFF-state stress (V_{DS} = 40 V, $I_D = I_{Dsat}/16$, T_j = 94°C)
After 1000 h of OFF-state stress the drain current is practically unchanged, see Fig. 5.12b. On the other hand, it has been found high degradation on the gate leakage current levels, Fig. 5.12a. Also only 3 of the 6 devices submitted to this test have reached the total of 1000 h of stress: failures of devices happened after 32 h (device "G"), 111 h (device "R") and 226 h (device "C").

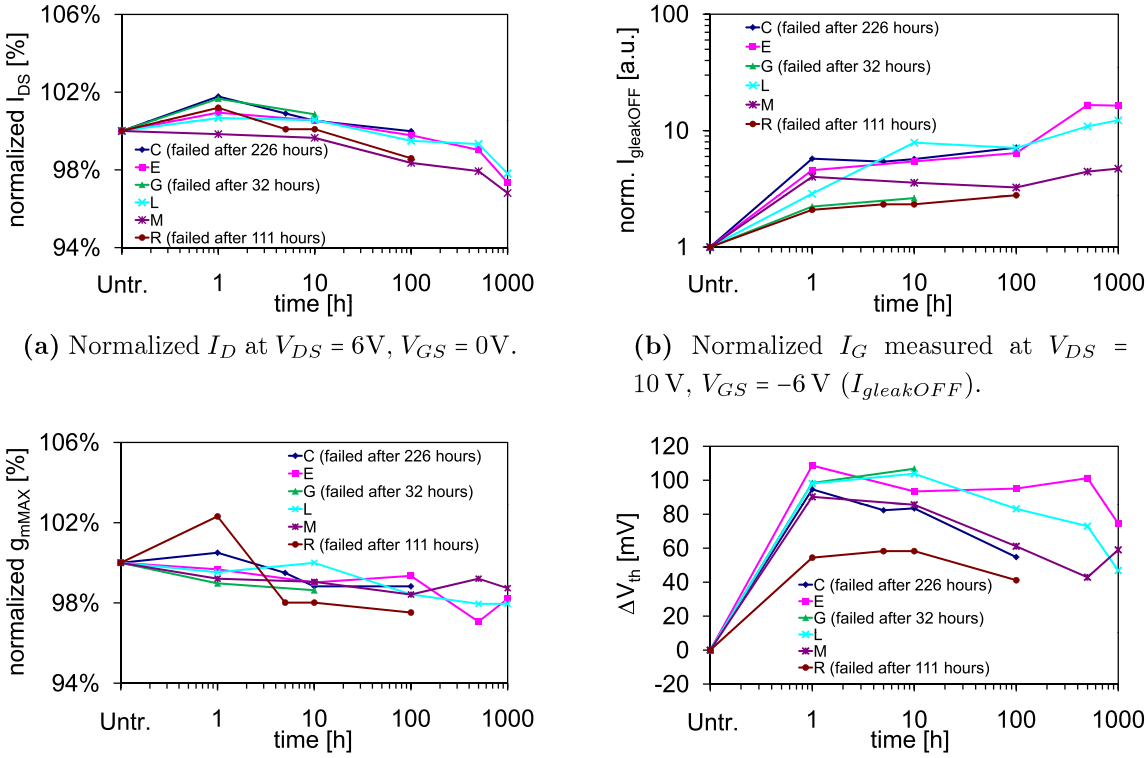
In the following diagrams, the main DC characteristics measured for each device submitted to OFF-state stress are reported. In this case the drain current shows a very low degradation during the stress, more pronounced in the knee region (see Fig. 5.13a). Transconductance measured at V_{DS} = 10 V (see Fig. 5.13c) shows a small



(a) Gate to Source diode.

(b) $I_D - V_{DS}$ at V_{GS} from 0 to −1 V.

Figure 5.12: Electrical characteristics of a representative device before (continuous lines) and after (dashed lines) 1000 h of OFF-state stress at I_D = 0.024 A and V_{DS} = 40 V. Junction temperature was kept at 94°C during the stress.



(a) Normalized I_D at V_{DS} = 6V, V_{GS} = 0V.

(b) Normalized I_G measured at V_{DS} = 10 V, V_{GS} = −6 V ($I_{gleakOFF}$).

(c) Normalized g_{mMAX} at V_{DS} = 10 V.

(d) Variation of V_{th} = $|V_{th-after}|$ − $|V_{th-before}|$ measured at V_{DS} = 10V.

Figure 5.13: Variation during the stress experiment of the main DC parameters for the transistor submitted to OFF-state stress (the letters indicate the different samples). Measured parameters are normalized to the initial value of the untreated device.

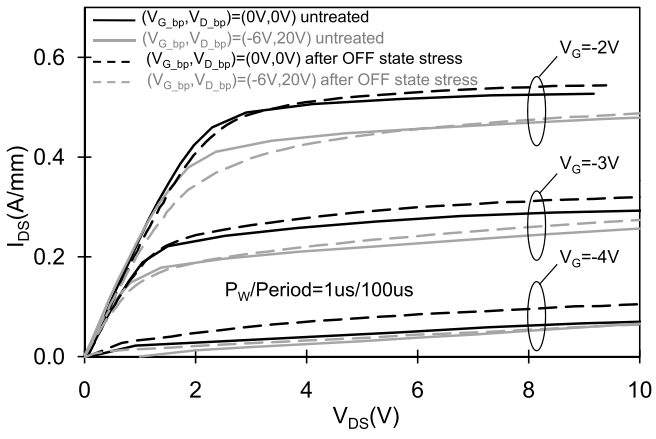


Figure 5.14: I_D vs V_{DS} output curves measured in pulsed condition for a representative device. Two different quiescent bias points are adopted: (0 V, 0 V) and (−6 V, 20 V). Continuous lines represent the measurement before stress, dashed line after the 1000 h OFF-state DC life test.

variation closed to the initial values (less than 3%). The gate leakage current increases for all devices (see Fig. 5.13b). Finally, as seen for the ON-state stress, a little shift of V_{th} (about 100 mV) to more negative values has been monitored, Fig. 5.13d. Dynamic characterizations have been carried out on the stressed devices: a decrease of drain current is measured in the knee region (observed also in DC characterisation), while the current slump is not affected by remarkable degradation, see Fig. 5.14.

SEMI ON-state (V_{DS} = 30 V, $I_D = I_{Dsat}/4$, T_j = 180°C)
The SEMI ON-state condition has caused irreversible damage of all the devices, see Fig. 5.15. The catastrophic failure happened at the beginning of the test, in the first hour. A possible explanation of this failure can be found considering the high gate leakage current measured when devices are biased at high drain voltage.

In Fig. 5.16a the DC characterization of a device realized at 30°C is shown. The three solid symbols represent the bias conditions selected for the stress test (black square, dark-grey diamond and light-grey triangle are ON-state, SEMI ON-state and OFF-state bias points, respectively), while the lines represent the I_D and the I_G measured near the stress bias condition. Device biased at V_{GS} = −2 V show low gate current because the drain voltage is limited at 15 V; for higher V_{DS} the gate current drastically increases: ideally extending I_G at V_G = −3 V to V_{DS} values up to 30 V (the dashed dark-grey line) the leakage current reaches −1.4 mA (about 3 mA/mm), see Fig. 5.16b. This value could be very detrimental and in this bias condition the device could not work properly. On the other hand, at V_{DS} = 40 V near to the pinch-off condition V_{GS} = −4.5 V, the gate leakage current stops at −0.7 mA (1.5 mA/mm), a value that the device can handle for a longer period.

The sudden failure observed in the SEMI ON-state was not expected if we consider the results form the previous short-term stress experiment carried out: in fact in the

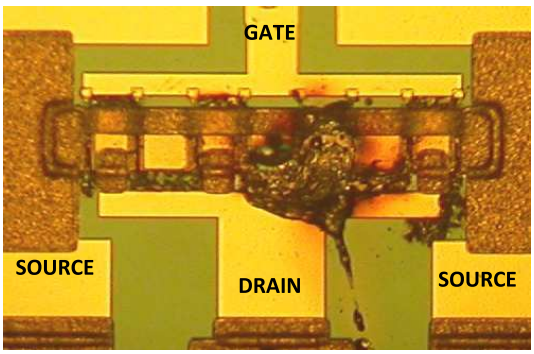
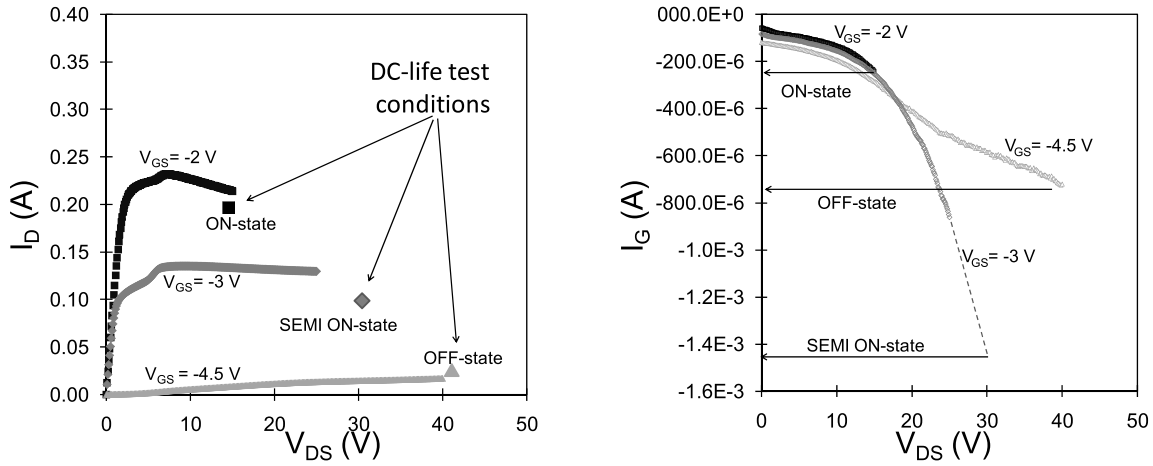


Figure 5.15: Picture of the catastrophic failure if a sample submitted to SEMI ON-state DC-life test.



(a) I_D vs V_{DS}. **(b)** I_G vs V_{DS}.

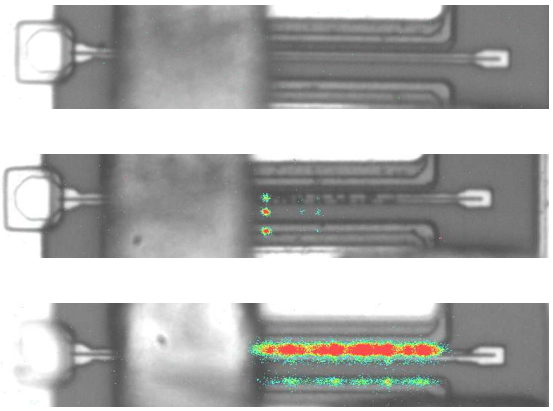
Figure 5.16: DC characteristics (left: I_D vs V_{DS}, right: I_G vs V_{DS}) of a transistor with W_G = 480 µm, L_G = 0.3 µm and L_{shield} = 1.3 µm. Gate bias is selected in order to obtain the I_D and I_G values as near as possible to the stress bias condition (black line V_{GS} = −2 V; dark gray line V_{GS} = −3 V; light gray line V_{GS} = −4.5 V). Stress bias conditions are also indicated in the figure.

"semi-open channel" condition the final bias point (V_{GS} = −3 V and V_{DS} = 30 V) is very closed to the SEMI ON-state in the DC-life experiment. A possible explanation is that in the short-term stress the highest drain bias is reached after several steps starting from a lower V_{DS}, during these steps the device may accumulate trapped charged which decrease the internal electrical field, or the strain induced by the applied voltage could be accommodate during the stress by the generation of defects, thus the device can handle higher fields without reaching destructive conditions. While in the DC-life test the sample is biased already at the beginning of the experiment with the highest drain voltage, causing the breakdown of the device.

A confirmation of the relevant issue represented by the high gate leakage current comes from the emission microscopy (EMMI) measurement carried out on the stressed devices and from the evolution during the stress of the I_G. The Fig. 5.17a shows the false colours emission map for an untreated device in closed channel condition (V_{GS} = −10 V, V_{DS} = 5 V) in comparison to the EMMI carried out on ON-state stressed devices, Fig. 5.17b, and on OFF-state devices, Fig. 5.17c. The presence of localized emission spots after ON-state stress indicates a damage on the device structure; this damage acts as a low-resistance path for the leakage current from the gate to the channel.

Moreover the formation of the damage is clearly related to the "jump" visible on

the I_G transient in Fig. 5.18. Notice that this failure is visible only on one of the four tested device submitted to the ON-state stress; it could be possible that this damage was caused by the presence of a previously existing defect; also it cannot be excluded that similar failures would have happened on the other samples if the stress would be longer than 1000 h. On the other hand, samples that have completed the OFF-state stress, without reaching the breakdown condition, show the presence of defect all along the gate edge (see Fig. 5.17c). Probably the high electrical field caused the formation of a great number of current path in order to carry out a higher leakage current, see Fig. 5.19; which, in some case, caused the device failure.



(a) Device D (untreated) emission in "closed channel" bias condition.

(b) Device A (after 1000 h of ON-state DC life test) emission in "closed channel" bias condition.

(c) Device E (after 1000 h OFF-state DC life test) emission in "closed channel" bias condition.

Figure 5.17: Emission-microscope image (in false colours) at V_{GS} = −10 V and V_{DS} = 5 V of a selected gate finger.

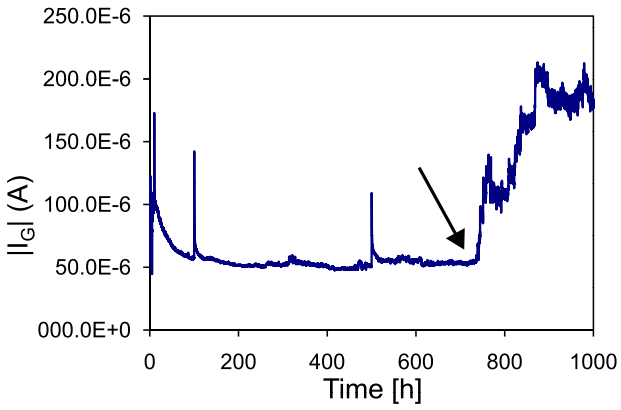


Figure 5.18: Gate current transient measured during the 1000 h DC-life ON-state stress; bias condition: V_{DS} = 15 V, I_D = 0.195 A, T_j = 184°C. Sudden increases of I_G before 600 h of stress are due to the brief interruption of the stress to carry out the DC characterization. Final jump (at ≈ 750 h, marked by the arrow) corresponds to the formation of the defect.

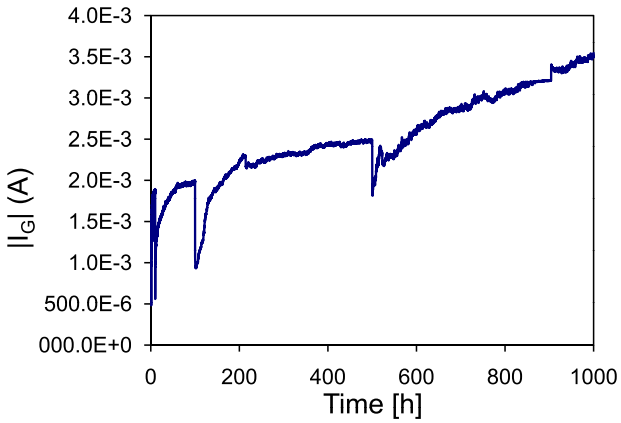


Figure 5.19: Gate current transient measured during the 1000 h DC-life OFF-state stress; bias condition: V_{DS} = 40 V, I_D = 24 mA, T_j = 94°C. Sudden decreases of I_G before 600 h of stress are due to the brief interruption of the stress to carry out the DC characterization.

5.4 Conclusions

The long-term stress presented in this chapter has shown a good stability and promising performance of GaN-based HEMTs grown on SopSiC substrate; these results are very encouraging and confirm that the composite substrates are suitable for low-cost and high performance AlGaN/GaN HEMT for RF power applications. The analysis carried out indicates how the nature of the substrate does not affect the reliability of the device; indeed the robustness of the sample seems to be concerned more to processing-related factors and to the DC characteristics of the transistor than to the substrate type. The failure of devices during the stress is clearly related to the high levels of gate leakage current: bias condition that implies high I_G caused the greater and faster degradation of the sample, in some cases leading to the catastrophic failure. Moreover the degradation is related to the creation of hot-spot and low-resistance current path at the gate-to-drain edge of the gate electrode, where the electrical field is maximum. The temperature had certainly a rule in the degradation of the samples (as seen in long, high-temperature storage stress carried out on similar devices [33]); probably, if the test was carried over the 1000 h, more ageing effects and a higher failure would been found at the end of the test.

6

Short Term Stress

In this chapter an investigation of the degradation of GaN-HEMTs induced by the reverse-bias step-stress is presented. The aim of this work on reliability was to test the devices manufactured by UCSB adopting different gate metalization and having different density of interface states on the AlGaN surface under the gate, as seen in section 3.3.

Also the same experiment has been carried out on a different wafer, with different processing and specifications, in order to have a term of comparison to better understand the type of degradation mechanisms involved in the reverse-bias step-stress.

6.1 The Step-Stress Experiment

The experiment adopted for the reliability analysis is a reverse-bias step-stress: in this experiment the gate to drain Schottky junction of the transistor is reverse biased at increasing voltage, while the source is kept floating (see the electric circuit in Fig. 6.1). The reverse bias is applied for two minutes, after each step of stress the transistor DC characteristics are completely measured. The starting voltage applied to the gate is $-10\,\mathrm{V}$, it is then decreased of $-5\,\mathrm{V}$ at each step until the achievement of a heavy degradation but not destructive condition. Since the gate-source distance is usually shorter than the gate-drain one, the stress configuration has been selected to be as close as possible to a real electrical configuration in a power application of the transistor: for example in a class-A amplifier when the device is turned off the high potential is applied between gate to drain diode than the gate to source one. Therefore the main parameter subject to degradation is the gate-drain leakage current, and it is used as a signal of the attainment of the stressed condition.

Also electroluminescence (EL) microscopy has been used in detecting localized breakdown effects and for the evaluation of the degradation mechanisms in off-state

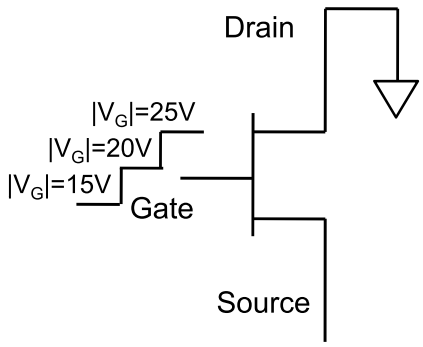


Figure 6.1: Reverse-bias gate step-stress set-up description.

stress. Two types of emission measurement have been adopted: an "ON-state" emission and a "OFF-state" emission. The ON-state is the measurement of the emitted light carried out with the device in on condition (V_{GS} = 0 V, V_{DS} = 9 V or 10 V, depending on the sample), the emission is measured for 5 s; while the OFF-state is measured with the following condition: $V_G = -10$ V, $V_D = 0$ V, source floating, emission period equal to 120 s. The OFF-state bias configuration is equal to the stress condition (source floating); because, as mentioned before, the source-gate spacing is lower than the gate-drain, meaning a high electric field between gate and source during the OFF-state emission that could "hide" the formation of defects in the gate-drain region. Summarizing a single step of the entire stress test is formed as follows:

1. 120 s reverse bias stress at increased $|V_{GS}|$;
2. complete DC characterization;
3. emission measurement in ON-state (EMI-ON);
4. emission measurement in OFF-state (EMI-OFF).

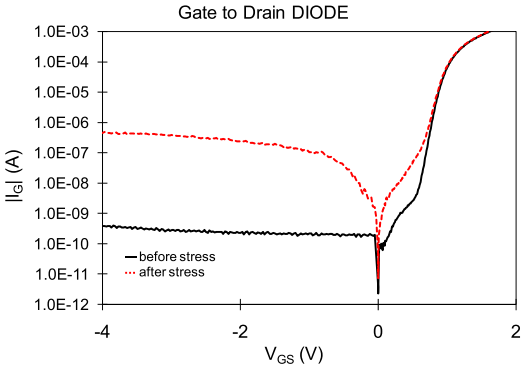
6.2 UCSB Sample

The samples used in this experiment are transistors from the wafer already presented in section 3.3; devices selected to be submitted to the ageing test are only passivated transistors, the robustness of the devices has been studied for each type of gate electrode available: Ni/Au/Ni, ITO and also Ni/ITO, a third type of gate electrode available on the wafer. The Ni/ITO gate stack is composed by a 5 nm layer of Ni that contact the AlGaN barrier followed by 250 nm of ITO, the Ni layer has been introduced in order to decrease the gate leakage current [49]. In the follows the results of a representative sample for each of the three types are shown: the measurements refer to the comparison

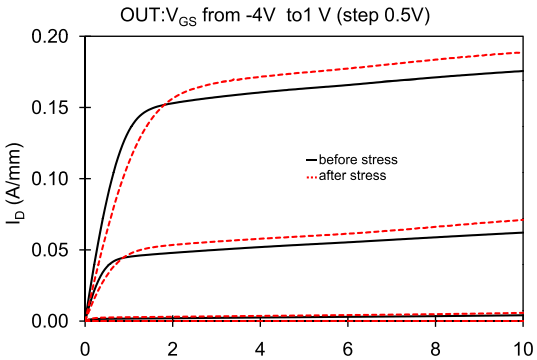
between the main DC characteristics, the trend of the I_{GD} leakage after each step, the emission images in OFF-state (indicated as EMI-OFF) and ON-state (indicated as EMI-ON); not all images for each the step are shown, but only the most relevant.

6.2.1 Ni/Au/Ni Passivated

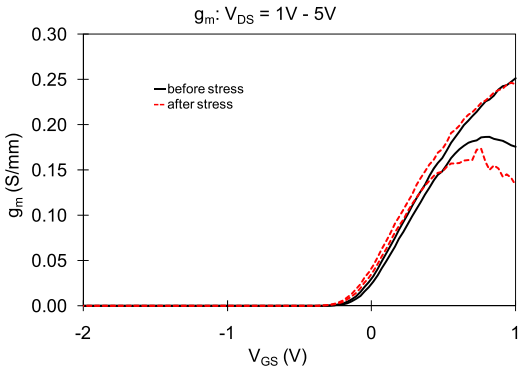
From DC characterization it is possible to see that, as expected, the highest degradation is in the gate-drain diode current, see Fig. 6.2a. In fact the gate leakage at the end of the stress is increased of more than two orders of magnitude respect to the initial value. Also the gate-source diode leakage is increased (not shown), which can be related to the formation of a damage below the gate area that works like a parasitic path for the leakage current from the gate to both drain and source contacts. Others effects of the stress are visible in the increase of the R_D and R_S values (Fig. 6.2d) and releated



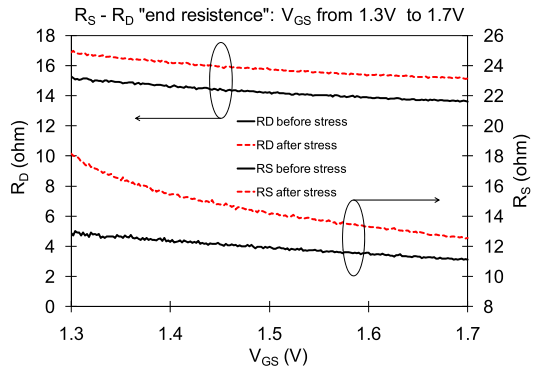
(a) Gate to drain diode characteristic.



(b) I_D vs. V_{DS} characteristic at V_{GS} from −4 V to 1 V, step 0.5 V.



(c) g_m vs. V_{GS} characteristic at V_{DS} = 1 V and 5 V.



(d) Drain (R_D) and source (R_S) end resistances.

Figure 6.2: Main DC characteristics of a stressed sample with Ni/Au/Ni gate electrode before (continuous line) and after (dashed line) the step-stress up to −60 V.

decrease of the drain current in the linear region (Fig. 6.2b). The increase of the drain output current (Fig. 6.2b) in saturation region can be explained considering the threshold voltage shift to more negative values. In fact the transconductance (g_m) after the stress (Fig. 6.2c) shows a little shift to the left: it can be ascribed to trapping phenomena that occurs when very high electrical fields are applied to the device for long time.

The gate-drain current variation measured at the end of each step of stress is very interesting for a fast explanation of the degradation mechanism: in fact, from Fig. 6.3, it is possible to see that the gate leakage is practically constant up to −40 V of reverse bias at the gate; moreover a slight decrease can be seen due to the trapping of charges. Then at the next step the current grows to higher values and continues to increase. This behaviour is in agreement with the theory of the inverse-piezoelectric effect, which suggest the existence of a critical voltage (V_{critic}), beyond that the device characteristics drastically get worse. In this case the critical voltage is V_{critic} = −45 V. The same behaviour is shown by the gate current measured during the emission OFF (see Fig. 6.4a); also, the increase of the gate leakage corresponds to the formation of a hot spot of emission, defect not visible in the virgin device (see Fig. 6.4b). This hot spot indicates the presence of a localized breakdown, which works like a low resistance path for the leakage current.

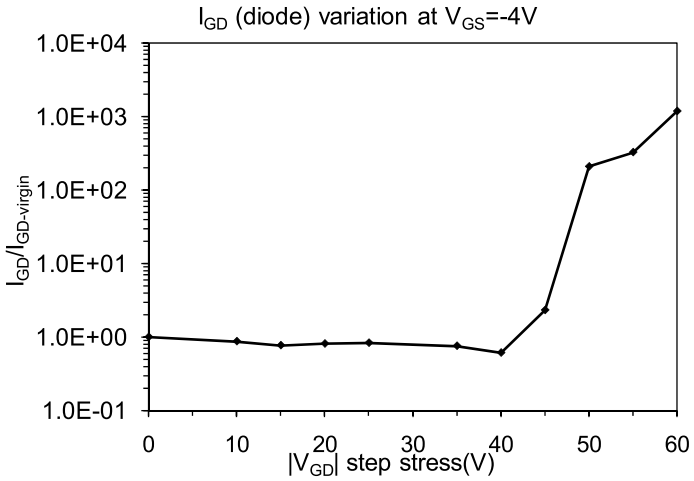
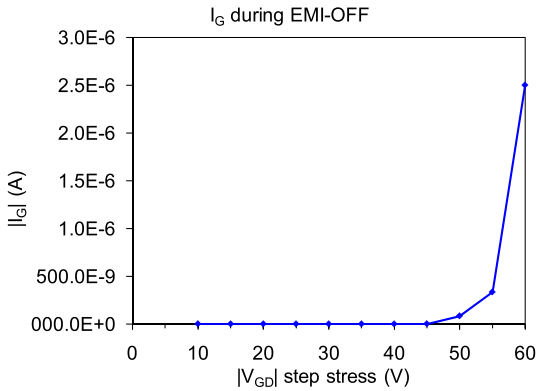
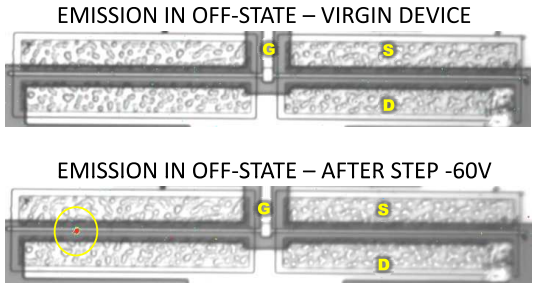


Figure 6.3: Gate-drain diode leakage-current in a representative Ni/Au/Ni gate device measured at V_{GD} = −4 V after each step of reverse-bias stress.

Current transients recorded during the reverse bias step stress test of the passivated Ni/Au/Ni sample show that at the beginning of each step, electron trapping takes place; the resulting negative charge reduces electron injection from the gate, thus resulting in a reduced gate current. The process saturates within each step, but during device



(a) Average gate to drain diode current during EMI-OFF measured after each step of the reverse-bias step.



(b) False-colours images of emission during EMI-OFF for two representative step (fresh sample and after step at −60 V). The circle indicates the hot-spot.

Figure 6.4: Emission microscopy for a representative Ni/Au/Ni gate device; emission are measured at V_{GD} = −10 V for 120 s.

characterization (carried out at the end of each step) charge detrapping occurs, so that a decreasing current transient takes place at the beginning of the next step. When the defect is created, in the case of this sample at the end of the step at V_{GD} = −45 V, a sudden increase of gate current is measured, marked by the arrow in Fig. 6.5. In the following steps, the current becomes noisy and continues to increase in small jumps.

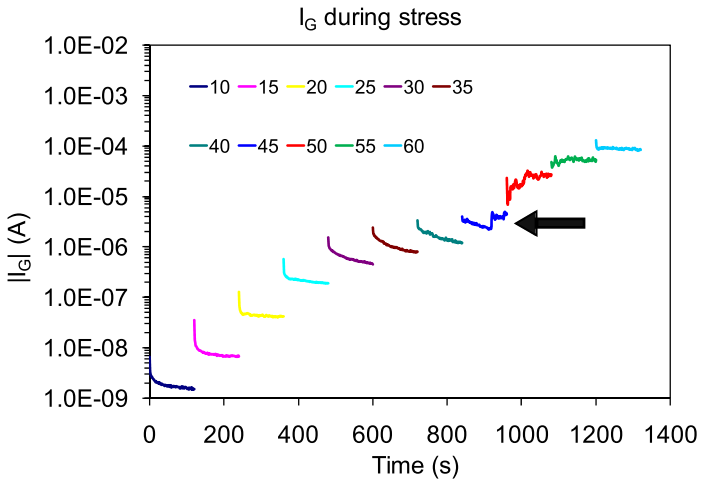


Figure 6.5: Gate current transients in a representative Ni/Au/Ni gate device measured during the reverse-bias stress.

On the other hand, the emission in ON-state does not show high variations during the test, in particular there is not a relevant difference between the initial emission value and the final value at the end of the last step of stress (see Fig. 6.6).

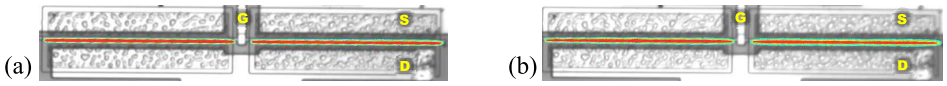
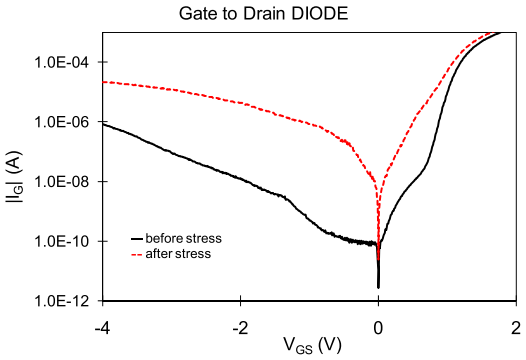


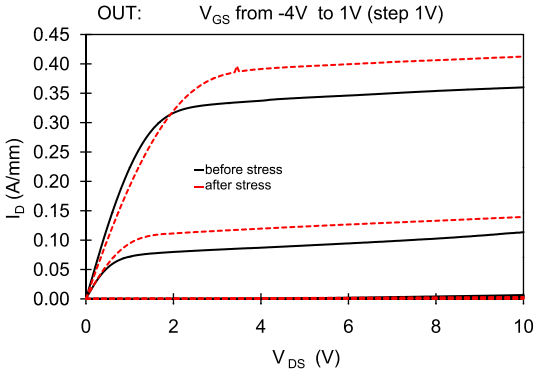
Figure 6.6: Emission in ON-state in: (a) virgin device ($count = 9.2 \times 10^6$ *a.u.*); (b) after step -70 V ($count = 8.6 \times 10^6$ *a.u.*).

6.2.2 ITO Passivated

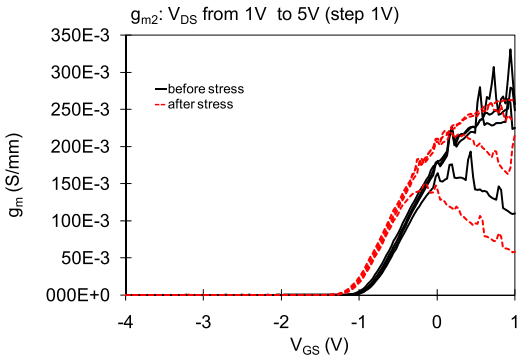
From DC characterization it is possible to see a degradation of the device behaviour similar to the one seen for the Ni/Au/Ni sample: increase of the gate-drain diode leakage (see Fig. 6.7a), increase of the R_D and R_S values (Fig. 6.7d) and the increase of the drain output current in saturation region (Fig. 6.7b), threshold voltage shift to more negative values (see Fig. 6.7c). Notice that the voltage shift is more heavy than in Ni/Au/Ni, since the amount of traps is greater in samples with ITO gate electrode.



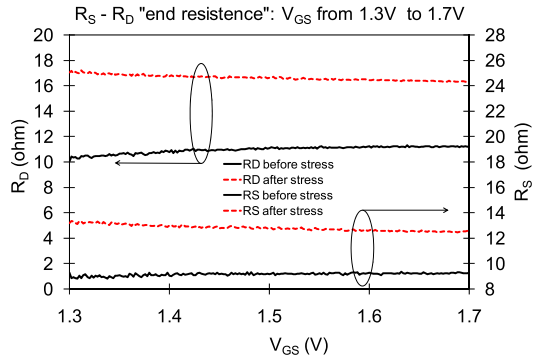
(a) Gate to drain diode characteristic.



(b) I_D vs. V_{DS} characteristic at V_{GS} from -4 V to 1 V, step 1 V.



(c) g_m vs. V_{GS} characteristic at $V_{DS} = 1$ V and 5 V.



(d) Drain (R_D) and source (R_S) end resistances.

Figure 6.7: Main DC characteristics of a stressed sample with ITO gate electrode before (continuous line) and after (dashed line) the step-stress up to -60 V.

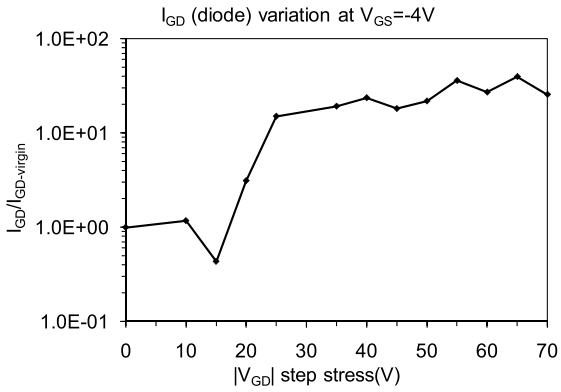
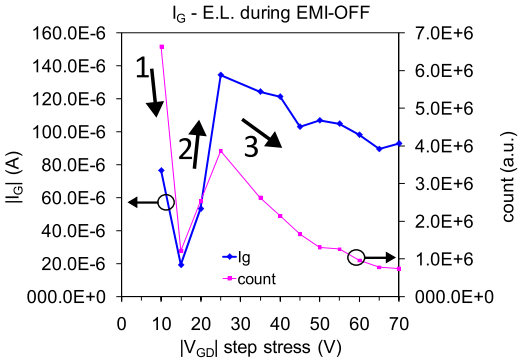
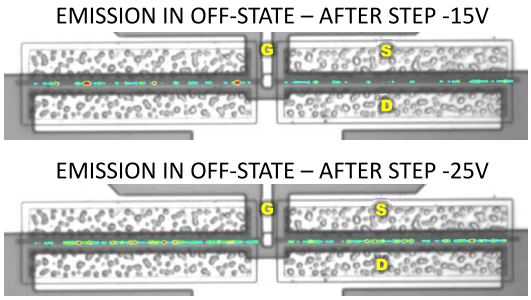


Figure 6.8: Gate-drain diode leakage-current in a representative ITO gate device measured at V_{GD} = −4 V after each step of reverse-bias stress.



(a) Average I_G and EL count during EMI-OFF measured after each step of the reverse-bias step.



(b) False-colours images of emission during EMI-OFF for two representative step (after step at −15 V and after step at −25 V).

Figure 6.9: Emission microscopy for a representative ITO gate device; emission are measured at V_{GD} = −10 V for 120 s.

On the other hand, the gate-drain current variation measured during the stress (Fig. 6.8) shows a different critical voltage value: V_{critic} = −20 V; exceeded this value the gate current increases of a order of magnitude in the next step (−25 V); then it becomes practically constant.

The same sudden increase at V_{GS} = −20 V is shown by the I_G and the emission count measured during the EL measurements in the OFF-state (see Fig. 6.9a where the "jump" is indicated by the arrow number "2"). Notice that the first point after the V_{GS} = −10 V step has not been taken into account; since the ITO samples are affected by a higher leakage current than the Ni/Au/Ni samples, which corresponds to a presence of hot spots already in the virgin device. The decrease in the EL total count after the V_{GD} = −15 V step can be easily explained by considering the trapped charges

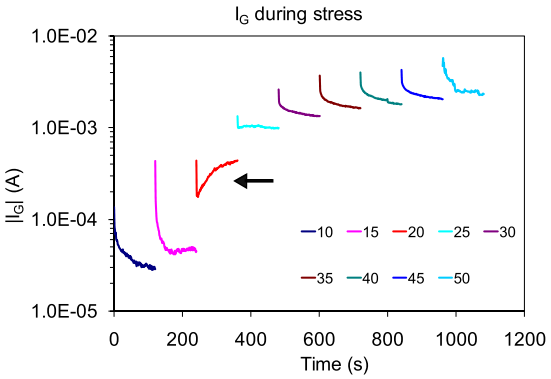
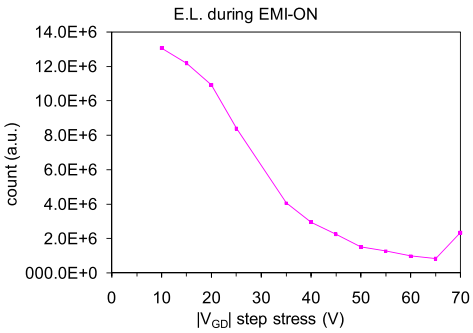
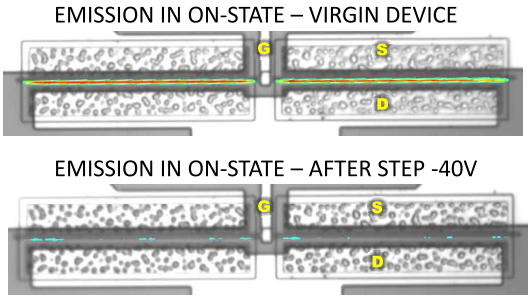


Figure 6.10: Gate current transients in a representative ITO gate device measured during the reverse-bias stress.



(a) EL count during EMI-ON measured after each step of the reverse-bias step.



(b) False-colours images of emission during EMI-ON for two representative step (fresh sample and after step at −40 V).

Figure 6.11: Emission microscopy for a representative ITO gate device; emission are measured at V_{GS} = 0 V and V_{DS} = 9 V.

during the stress (Fig. 6.9a, arrow number "1"). But, despite this, it is possible to see the same ageing behaviour found in the previous device. After the drastic increase of the gate leakage current due to the formation of defects along the gate electrode, the trapping process still proceeds bringing to the decrease of the total photon count, as indicated by the arrow number "3" in Fig. 6.9a.

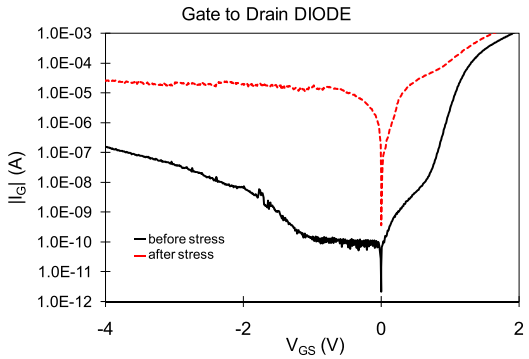
Current transients measured during the experiment show a interesting trend: in correspondence to the gate voltage which causes the damage (V_{critic} = −20 V, indicated by the arrow in Fig. 6.10) the current transient is inverted (it increases); while in the other steps it decreases. This trend could be thought as a slow but continuous creation of new defects or worsening of the previously existing ones: during this transient the defects already present on the surface (defects due to the realization processing) become

more extended along the gate edge, as shown by the increase of EL during EMI-OFF (Fig. 6.9b) and also may extend into the AlGaN layer inducing the permanent increase on the gate leakage current.

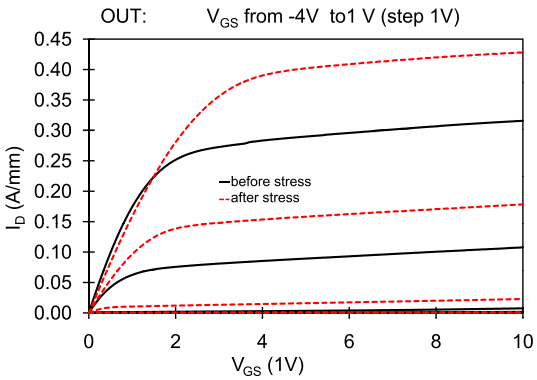
Finally the ON-state emission confirms the trapping of carriers that results in a lower electrical field and a lower photon emission (see Fig. 6.11).

6.2.3 Ni/ITO Passivated

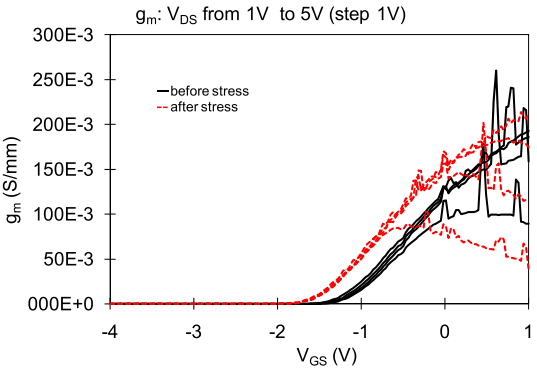
Also in the Ni/ITO the tested devices show the same results after the step stress: increase of the gate-drain diode leakage (see Fig. 6.12a), increase of the drain output current (see Fig. 6.12b), increase of the R_D and R_S values (see Fig. 6.12d), threshold voltage shift (see Fig. 6.12c) due to traps under the gate.



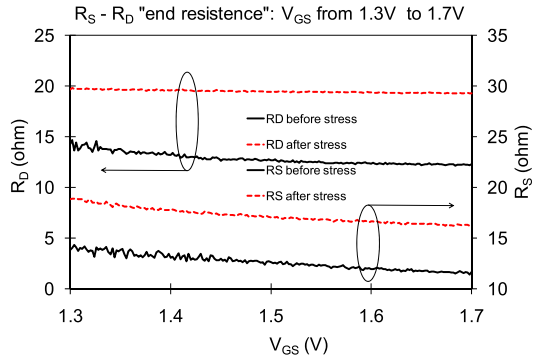
(a) Gate to drain diode characteristic.



(b) I_D vs. V_{DS} characteristic at V_{GS} from −4 V to 1 V, step 1 V.



(c) g_m vs. V_{GS} characteristic at V_{DS} = 1 V and 5 V.



(d) Drain (R_D) and source (R_S) end resistances.

Figure 6.12: Main DC characteristics of a stressed sample with Ni/ITO gate electrode before (continuous line) and after (dashed line) the step-stress up to −60 V.

The critical voltage value found from the gate-drain current variation measured

during the stress (Fig. 6.13) is similar to the value for the ITO sample: V_{critic} = −20 V; exceeded this value the gate current increases of two orders of magnitude in the following steps, becoming constant after step −30 V. The I_G and the emission count during the EL in OFF-state show the same trend of the I_{GD} during the stress: in fact from Fig. 6.14a it is possible to see that after step −20 V there is an increase of the two parameters up to the −30 V step (arrow number "2"). After this, when the gate leakage measured in the DC characterization becomes constant - Fig. 6.13, both I_G and emission count start to decrease, as seen in the ITO sample; arrow number "3" in Fig. 6.14a.

The trend of the current transients measured during the experiment is the same as

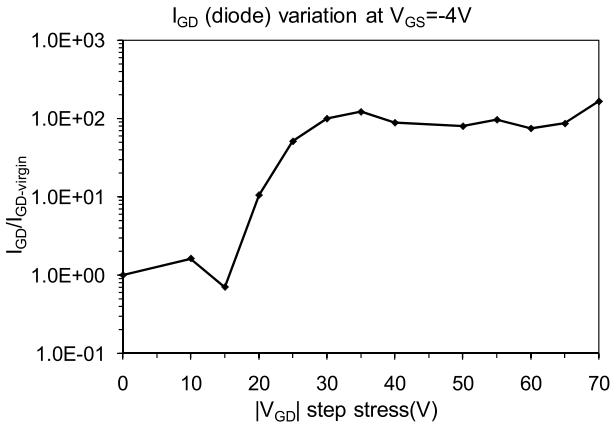
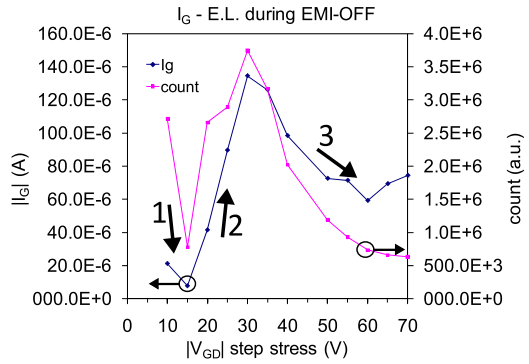
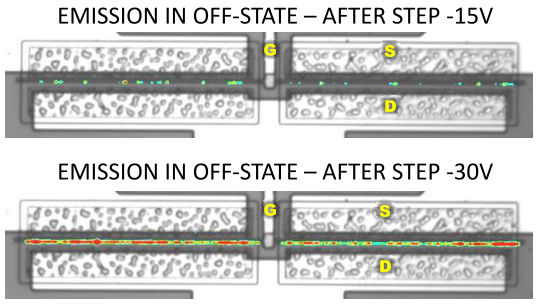


Figure 6.13: Gate-drain diode leakage-current in a representative Ni/ITO gate device measured at V_{GD} = −4 V after each step of reverse-bias stress.



(a) Average I_G and EL count during EMI-OFF measured after each step of the reverse-bias step.



(b) False-colours images of emission during EMI-OFF for two representative step (after step at −15 V and after step at −25 V).

Figure 6.14: Emission microscopy for a representative Ni/ITO gate device; emission are measured at V_{GD} = −10 V for 120 s.

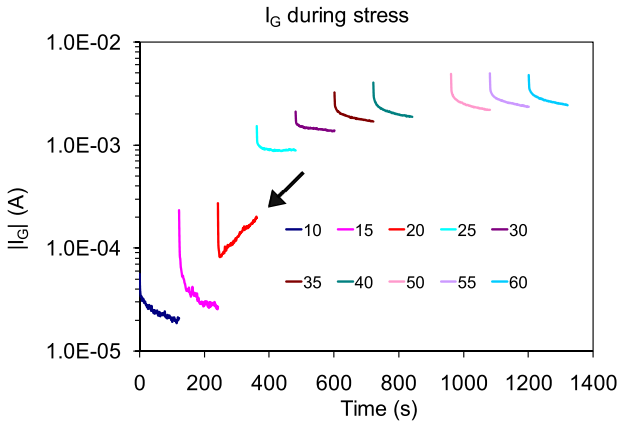
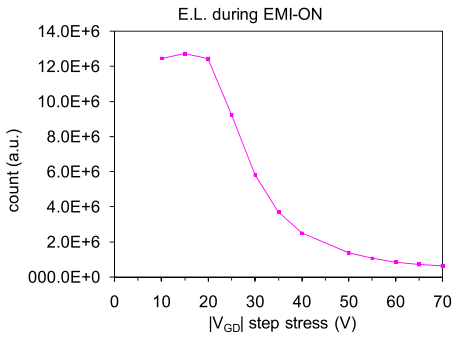
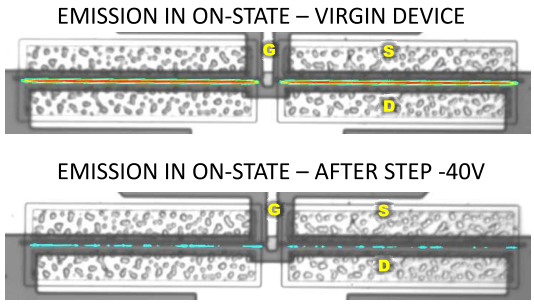


Figure 6.15: Gate current transients in a representative Ni/ITO gate device measured during the reverse-bias stress.



(a) EL count during EMI-ON measured after each step of the reverse-bias step.



(b) False-colours images of emission during EMI-ON for two representative step (fresh sample and after step at −40 V).

Figure 6.16: Emission microscopy for a representative Ni/ITO gate device; emission are measured at V_{GS} = 0 V and V_{DS} = 9 V.

measured in ITO devices: in correspondence to the critical voltage (V_{critic} = −20 V) the current transient results inverted; returning normal in the other steps, see Fig 6.15. Since emission microscopy in OFF-state shows the same non-monotonic behavior found for ITO devices (see Fig. 6.9), the degrading mechanism can be explained with the same hypothesis made for ITO samples: fresh devices already show hot spot during the initial EMI-OFF (Fig. 6.14b), than the total EL count decreases a first time due to the charge trapping. When the critical voltage is applied there is the formation of new defects and/or the worsening of the pre-existing ones. After that, when the degradation is stable, the EL start to decrease again for the trapping phenomena, as reported in Fig. 6.14a.

The ON-state emission confirms the carriers trapping that induces a lower electrical field and a lower photon emission (see Fig. 6.16).

6.2.4 Result Discussion

Finally in Fig. 6.17 the comparison among the tested devices is presented, the parameter taken into account is the gate to drain leakage current at $V_{GD} = -4\,\mathrm{V}$. It is possible to see that devices with the same type of gate material show similar critical voltage; but a great difference exists between the V_{critic} of Ni/Au/Ni samples and the one of ITO and Ni/ITO samples. This difference does not have an explanation from the inverse piezoelectric effect theory proposed in section 2.6: in fact the samples are grown on the same wafer and on the identical AlGaN barrier layer, so the strain resulting from the application of a high electric field should be the same for all the samples, resulting in an uniform V_{critic} along the entire wafer. Moreover the entity of the gate leakage on the fresh device seems to play a role in the degradation mechanism: samples with high initial gate current reach sooner the V_{critic} than samples with low gate leakage.

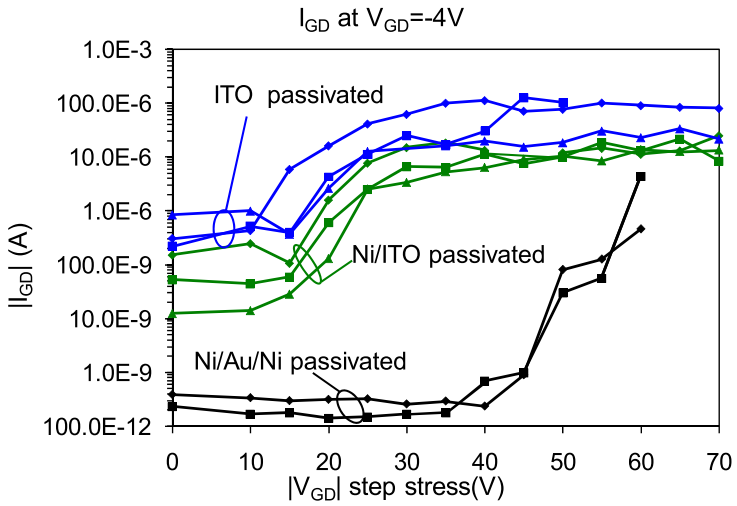


Figure 6.17: Gate-drain diode leakage-current measured at $V_{GD} = -4\,\mathrm{V}$ after each step of reverse-bias stress for the three types of measured devices.

A similar result is presented in [84], where reverse-bias step-stress is applied to samples with different gate materials but same epitaxial structure. In this case the authors explain the difference on the V_{critic} found among samples realized on the same wafer as due to difference on processing parameters and on the material composition of the gate.

In conclusions the results collected from this first step of the work on the short term stress show that the reverse-bias step-stress induces the creation of parasitic paths for

the gate leakage current. If we consider the inverse piezoelectric effect hypothesis to explain the defects formation, it seems that the gate material composition and the high initial gate leakage due to deep levels under the gate lead to a reduction in the critical voltage. The increase of defects concentration could be promoted, in case of high levels of leakage current, by a percolation process in the AlGaN layer to the GaN buffer [42].

6.3 SLX-35 Sample

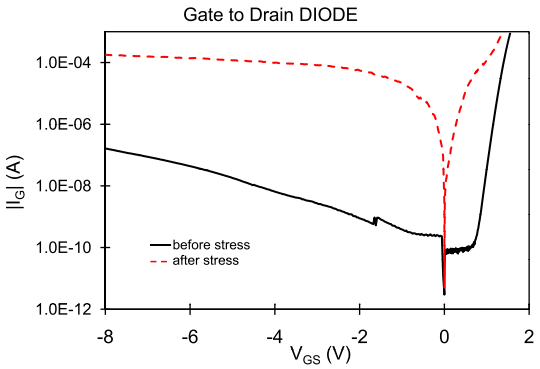
The step-stress experiment has been carried out also on transistors from the wafer "SLX-35". The AlGaN/GaN heterostructure is formed by a 1.5 µm GaN-buffer layer followed by a 22 nm AlGaN-barrier layer with 25.5% of Al content. Drain and source ohmic contacts are based on a Ti/Al/Pt/Au stack, while gate Schottky contact is formed by a Ni/Au stack (40 nm and 300nm respectively). The surface is passivated with a 90nm SiN layer. Epitaxial layers are grown on a SiC substrate. Devices tested in the SLX-35 wafer are double-finger transistors, with L_G = 0.5 µm and W_G = 200 µm; and gated-TLM, with L_G = 0.5 µm and W_G = 100 µm.

Three different stress experiments have been carried out on these samples: the "classic" voltage step-stress, in order to determine the critic voltage for this specific technology; a current step-stress, where the $|I_G|$ is increased each step of stress; and a final stress at constant gate current. The aim of these last two experiments was to study the role of the current in a reverse gate-bias stress.

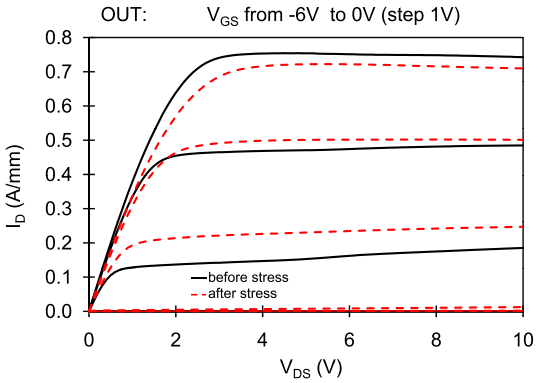
6.3.1 Voltage Step-Stress

In Fig. 6.18 the DC characteristics of a representative device submitted to the voltage step-stress are reported. It is possible to see that the ageing effects are similar to the ones previously described. The main degradation is found on the gate-drain leakage current with an increase greater than two orders of magnitude (Fig. 6.18a); the maximum drain current and the transconductance peak are lower than in the fresh sample (Figures 6.18b and 6.18c); the gate-to-drain and gate-to-source access resistance are increased at the end of the stress (Fig. 6.18d).

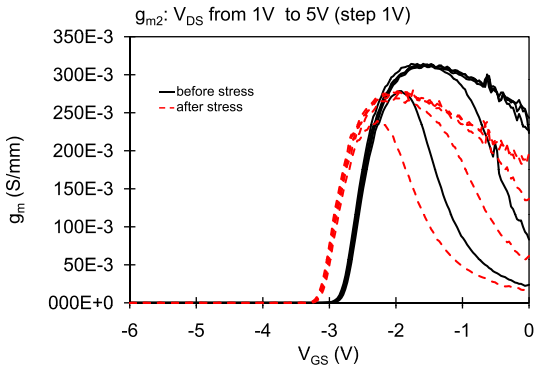
The critical voltage found for these devices is V_{critic} = −30 V, see Fig. 6.19a; moreover, as previously described, the gate current measured during the stress shows the typical noisy transient when the critical bias is applied (Fig. 6.19b). Notice that for $|V_G|$ greater than $|V_{critic}|$ the degradation of the device is still growing; effect that is visible also from the images of the electroluminescence taken during the EMI-OFF measurements after each step: in fact from Fig. 6.20b it is possible to see that the



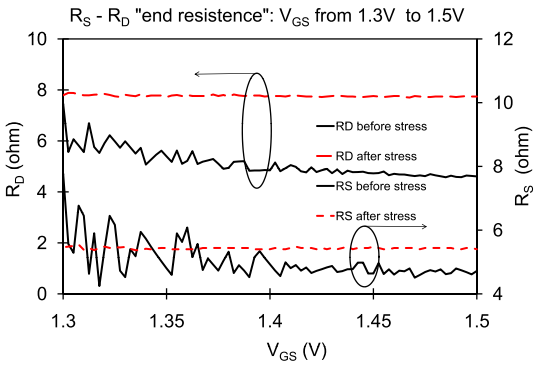
(a) Gate to drain diode characteristic.



(b) I_D vs. V_{DS} characteristic at V_{GS} from −6 V to 0 V, step 1 V.

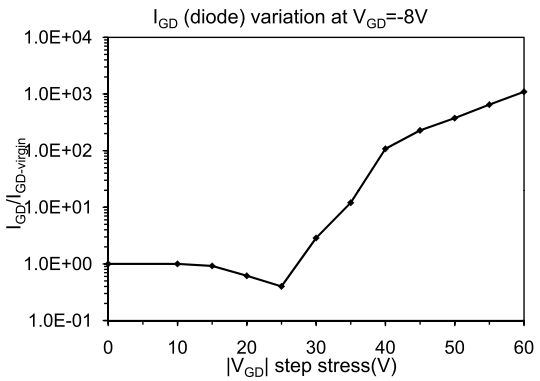


(c) g_m vs. V_{GS} characteristic at V_{DS} = 1 V to 5 V.

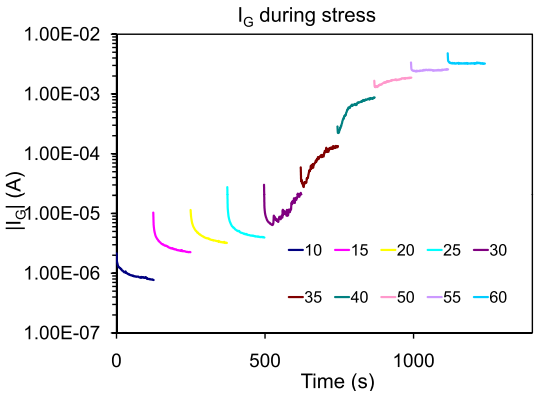


(d) Drain (R_D) and source (R_S) end resistances.

Figure 6.18: Main DC characteristics of a stressed sample before (continuous line) and after (dashed line) the step-stress up to −60 V.

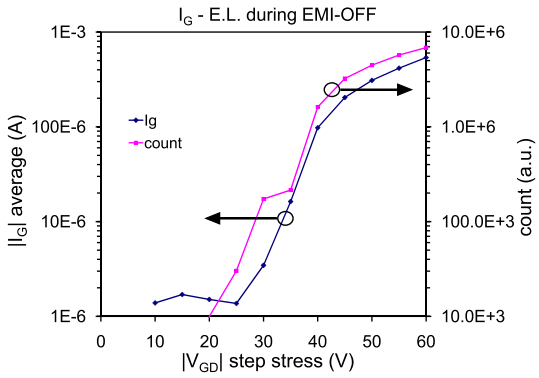


(a) I_G measured at V_{GD} = −8 V after each step of stress.

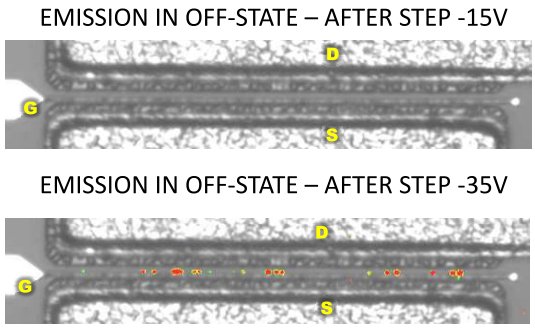


(b) I_G transients measured during the reverse-bias stress.

Figure 6.19: Variation of the gate leakage current during stress.



(a) Average I_G and EL count during EMI-OFF measured after each step of the reverse-bias step.



(b) False-colours images of emission during EMI-OFF for two representative step (after step at −15 V and after step at −35 V).

Figure 6.20: Emission microscopy for a representative device; emission are measured at V_{GD} = −10 V for 120 s.

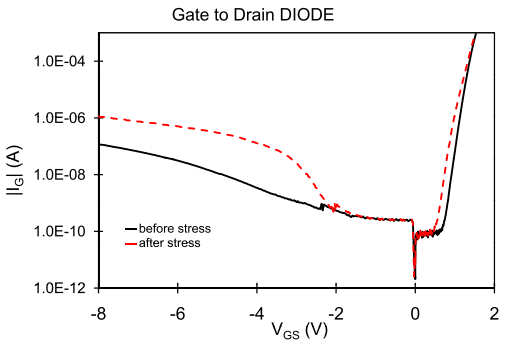
number of hot-spot and the related photon count (Fig. 6.20a) grows with the increase of the stress bias following the same trend of $|I_G|$.

6.3.2 Current Step-Stress

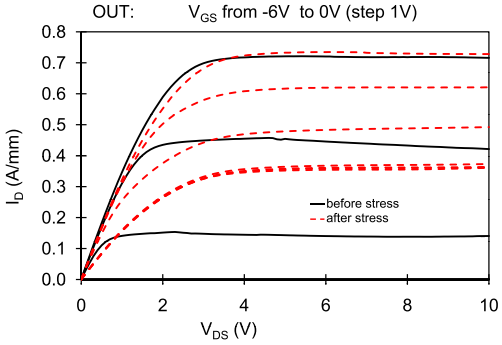
The current step-stress is carried out with the same procedure of the voltage step stress: a stress phase 2 min-long followed by a diagnostic phase (DC characterization, EMI-ON and EMI-OFF electroluminescence characterization); but in this case, instead of a constant voltage, during the stress a negative current is applied to the gate. The aim of the experiment is to find the value of I_G that induces a degradation similar to the one induced by the voltage step-stress, and if the respective V_G can be compared to the value of V_{critic}.

In the follows the results of the stress on a representative device are reported; the current values used to stress the device are −0.5 µA, −1 µA, −2 µA, −5 µA, −10 µA, −15 µA, −50 µA and −100 µA. From Fig. 6.21 it is possible to notice that at the end of the stress the degrade induced in the transistor is similar to the one obtained from the voltage step-stress, in particular the gate leakage is almost one order of magnitude higher than the initial value, see Fig. 6.21a. Moreover after the last step of stress the transistor cannot reach anymore the pinch-off condition, see Fig. 6.21b: this is a sign of a heavy damage probably located in the channel.

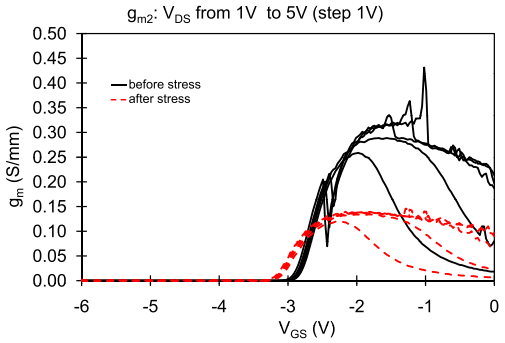
The trend of the gate voltage during the stress has been analyzed in order to compare the two types of step-stress experiments carried out: in Fig. 6.22a the average



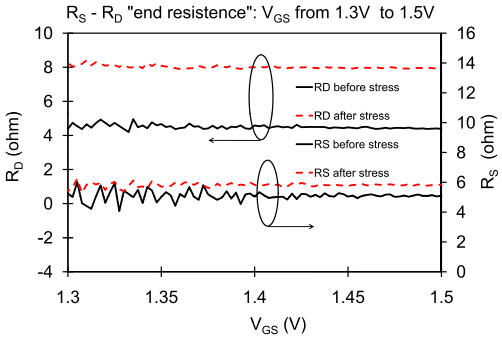
(a) Gate to drain diode characteristic.



(b) I_D vs. V_{DS} characteristic at V_{GS} from −6 V to 0 V, step 1 V.

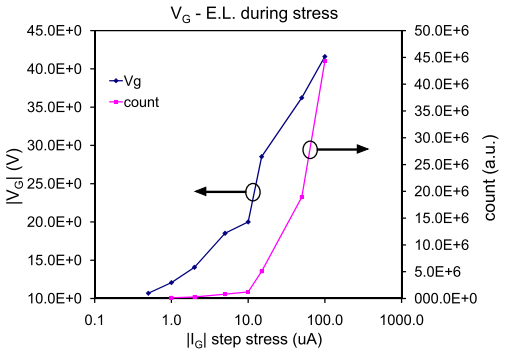


(c) g_m vs. V_{GS} characteristic at V_{DS} = 1 V to 5 V.

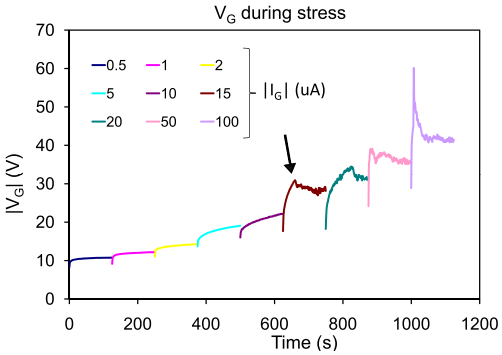


(d) Drain (R_D) and source (R_S) end resistances.

Figure 6.21: Main DC characteristics of a stressed sample before (continuous line) and after (dashed line) the current step-stress up to −100 µA.



(a) Average V_G and EL count measured during stress.



(b) $|V_G|$ transients measured during the reverse-bias stress.

Figure 6.22: Variation of the gate voltage during the stress.

value of V_G for each current step is reported, while in Fig. 6.22b the transients of V_G are reported. As expected, when the stress current is increased a relative increase of

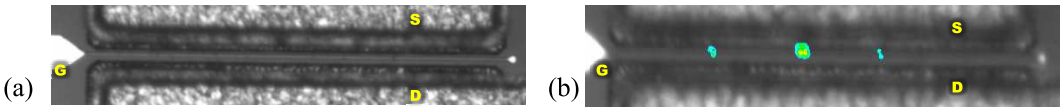


Figure 6.23: Emission during stress: (a) $I_{G_{stress}}$ = −10 µA; (b) $I_{G_{stress}}$ = −15 µA.

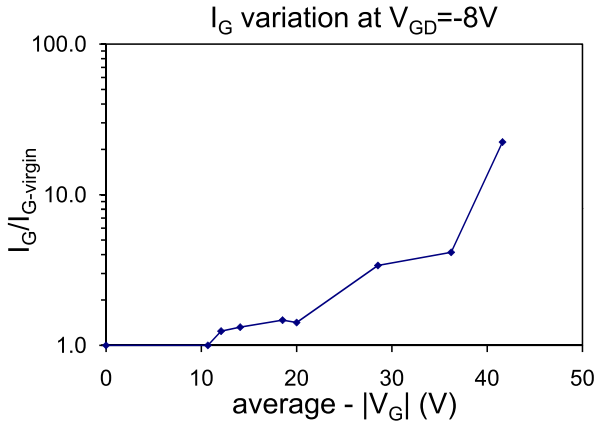


Figure 6.24: Gate-drain diode leakage-current measured at V_{GD} = −8 V after each step of reverse-bias stress.

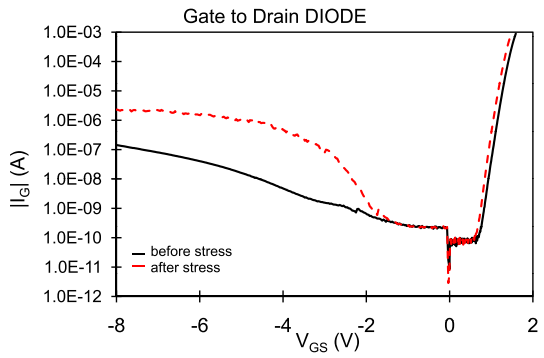
the voltage is measured (Fig. 6.22a); on the other hand the V_G transients show a more interesting behavior: when $|I_{G_{stress}}|$ = 15 µA the voltage starts to be noisy (Fig. 6.22b where the instant of the damage creation is indicated by the arrow) and some hot-spots appear on the emission image taken during the stress (Fig. 6.23). A possible explanation could be that during the stress the formation of some defects occurred in the AlGaN layer; these damage help the injection of electrons from the gate electrode to the channel (probably by trap-assisted tunneling); since it is not a continuous process, the voltage required to maintain a constant current starts to show fluctuations.

The gate current measured after the $|I_{G_{stress}}|$ = 15 µA step shows a not-recoverable increase respect to the fresh sample; the average value of $|V_G|$ during this step is −28 V (see Fig. 6.24), close to the value of V_{critic} found in the voltage step-stress.

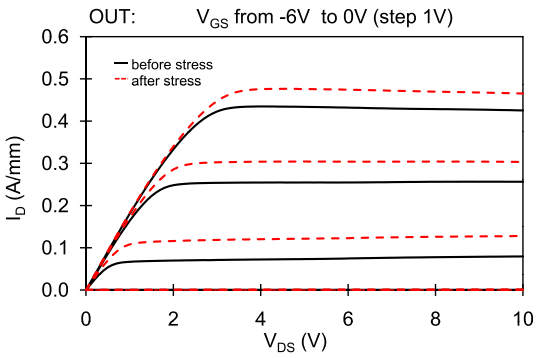
6.3.3 Constant Current Stress

A constant-current stress has been realized in order to better understand how the reverse current applied to the gate induce a damage on the device. The experiment consists in biasing the device with a negative current for 10 h; during the stress the gate bias is monitored, while complete diagnostic characterizations are carried out at logarithmic steps. Samples submitted to the stress are gated-TLM; in the follows two interesting devices are presented.

In the first sample the applied current is $|I_G|$ = 2 µm; at the end of the stress the gate



(a) Gate to drain diode characteristic.



(b) I_D vs. V_{DS} characteristic at V_{GS} from −6 V to 0 V, step 1 V.

Figure 6.25: Main DC characteristics of a stressed sample before (continuous line) and after (dashed line) the constant current stress at −2 µA.

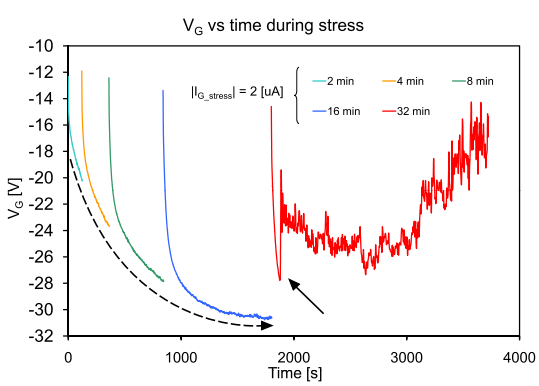
leakage current is increased of more than a order of magnitude (Fig. 6.25a), while the increase of the drain current (Fig. 6.25b) is due to the threshold voltage shift induced by trapping and hole accumulation at the interfaces [43].

The V_G variation measured during the stress shows a very long transient (≈ 1500 s), before the reaching of a stable value (≈ −30 V), see Fig. 6.26a where the real trend of the gate voltage is highlighted by the dashed arrow. This transient could be ascribed to very slow trapping phenomenons: in fact the fast transient in the correspondence of the interruptions to carry out the diagnostic measurements does not affect the total trend of the main slow transient. Furthermore the creation of the damage appears at about 31 min from the beginning of the stress, with $|V_G|$ = 28 V. From this point till the end of the stress the gate voltage starts to fluctuate moving to less negative values, see Fig. 6.26b.

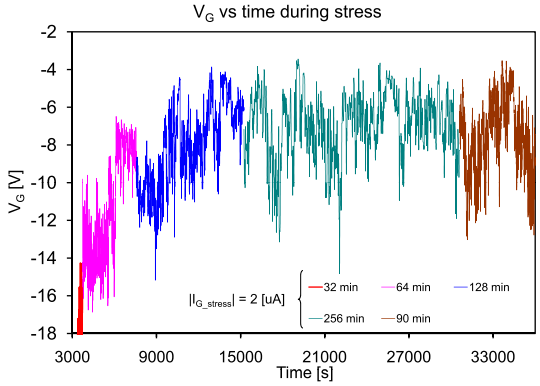
The creation of a permanent damage is proved also by the electroluminescence measurements carried out during each step: in Fig. 6.27b the EMI-OFF image taken after the 32 min-step shows the presence of a hot-spot not presents at the end of the 16 min-step (Fig. 6.27a).

As previously said, after the creation of the damage the average V_G decreases (Fig. 6.28a), because the damage works like a low-resistance path for the current; moreover hot-electrons injected from the gate electrode to the channel are less energetic, since the electrical field is lower, in this condition no further damages are created and the leakage current stabilizes around the stress value, see Fig. 6.28b.

Other samples, with equals geometries and submitted to the same type of stress, have shown a total different behavior. As example we report the results of a device submitted to a constant current of I_G = −4 µA. In Fig. 6.29 the DC characterizations



(a) First part of the $|V_G|$ variation during the stress, where the creation of the damage is visible.



(b) Second part of the $|V_G|$ variation during the stress, the gate bias increases to less negative values.

Figure 6.26: Variation of the gate bias during the constant current stress (−2 µA).

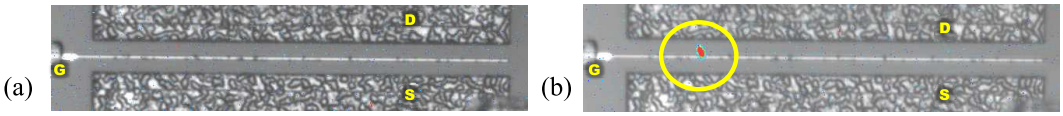
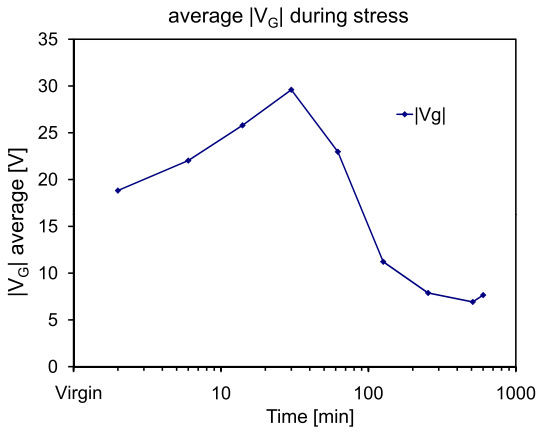
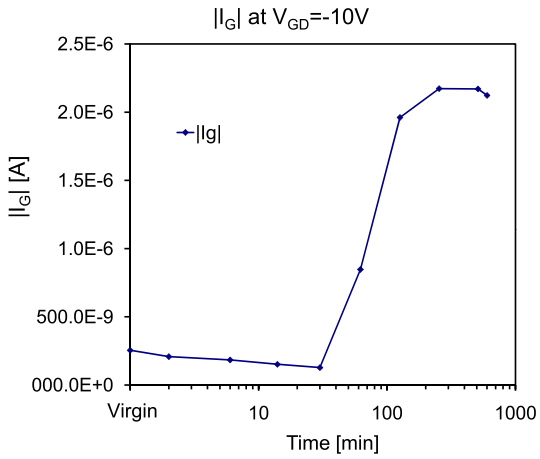


Figure 6.27: False colours images taken during EMI-OFF: before (a) and after (b) the 32 min long step. The hot-spot is highlighted by the circle.



(a) Average V_G measured during each time-step of the stress.

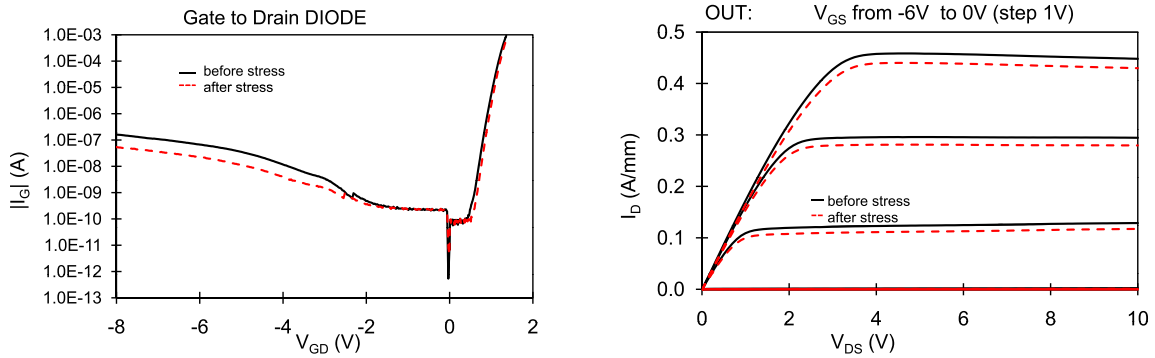


(b) I_G at V_{DS} = −10V after each diagnostic step.

Figure 6.28: Evolution of the gate bias (a) and the gate leakage during the stress.

before and after stress are reported: no significant degradation effects are visible in the gate leakage current, neither in the drain current.

The gate voltage applied during the stress increases (considering the absolute value)



(a) Gate to drain diode characteristic.

(b) I_D vs. V_{DS} characteristic at V_{GS} from −6 V to 0 V, step 1 V.

Figure 6.29: Main DC characteristics of a stressed sample before (continuous line) and after (dashed line) the constant current stress at −2 µA.

up to 40 V, see Fig. 6.30, higher than the V_{critic} previously found; also none sudden jump of the voltage is measured since there is not formation of low-resistance current path ad the edge of the gate. On the other hand, after the initial long transient where V_G arrives at −40 V, an inversion of the decreasing trend is measured and the gate voltage starts to slowly increase. This variation can be explained as follows: in the initial part of the stress slow traps catch carriers which lower the electric field and, in order to maintain a constant current, a higher $|V_G|$ is required (arrow "1" in Fig. 6.30). When all the traps are occupied, the applied bias start to degrade the sample; this degradation can be permanent with the creation of a hot-spot (as seen before), or can proceed slowly before one can measure a visible ageing effect (arrow "2" in Fig. 6.30).

6.4 Conclusions

In this chapter an extensive analysis of the degradation effects induced by the reverse-bias step-stress has been presented. The results have shown how the step-stress induces a particular degradation that involves the formation of hot-spot or low-resistance current path ad the edge of the gate, as largely reported in literature. This results have been found in samples with different gate materials but equals epitaxial structure and samples with totally different layer structure. The particularity of this work is that the mechanisms often indicate as the origin of the degradation (in particular the reverse piezoelectric effect), do not completely explain some particular ageing behavior found in the tested devices. As example the difference on the critical voltage for samples processed on the same wafer was not expected; also the trend of current/voltage bias

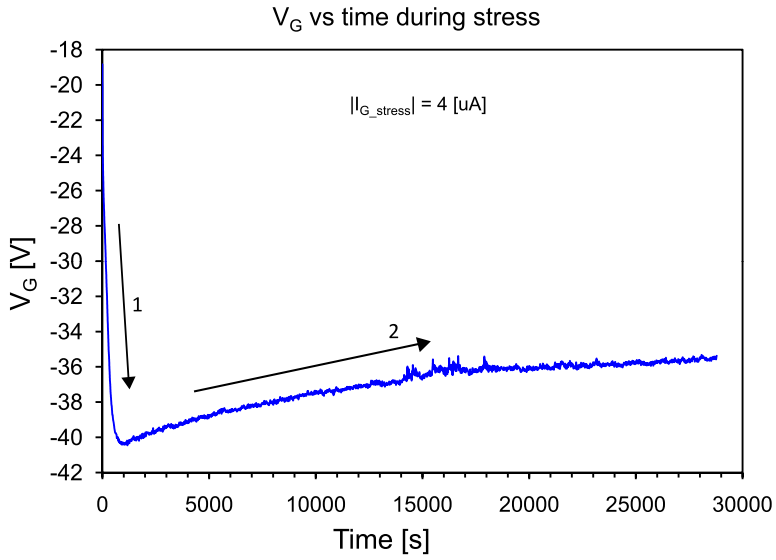


Figure 6.30: Variation of the gate bias during the constant current stress (−4 µA).

during the stress suggests a more complicated degradation mechanism occurring during the reverse-bias step-stress.

The concept highlighted by this work is that the gate degradation must be studied also with a different approach than the usual step-stress experiment. In fact the gate stack materials, the initial leakage current and the presence of defects/traps in the virgin device must be taken into account in order to correctly understand the degradation induced by the reverse biasing of the gate.

7

Conclusions

In this work an investigation of defects and reliability aspects related to GaN-based devices has been presented. The activity has been divided into four main arguments: *i)* combined electro-optical measurements, *ii)* low frequency noise measurement (both *i* and *ii* related to the analysis of defects and traps in the device), *iii)* long term stress and *iv)* short term stress (these two points related to the reliability analysis).

The main obtained results can be summarized as follows.

1. A combined electro-optical methodology has been developed for the study of traps in GaN-based HEMTs. This technique combines the pulsed measurement of the device transconductance with the measurement of the electroluminescence of the transistor. It has been demonstrated, with the aid of $C-V$ measurements, that the pulsed g_m can be easily used to detect the presence of traps in the device. Moreover it gives the possibility to identify the location of these traps (if they are in the region below the gate or at the device surface).
   Furthermore it has been shown that the EL measurement allows the comparison among different devices in terms of amount and equivalent temperature of hot electron; useful information to make a first evaluation on the device reliability.
   The proposed measurement procedure can be easily integrated in standard characterization setups, with the aim of providing rapid comparison of different device technologies.

2. The low-frequency measurements technique has been studied and applied on GaN-based TLM and transistors. Measurements on TLM have shown a possible correlation between the specific contact resistance value of the ohmic contact and the noise coming from this last one. In fact the noise measured on a TLM can be divided in the two components: one coming from the channel and one from the ohmic contact. With the measurement of different samples with different contact

resistances it has been seen that ohmic contacts with high values of the specific resistance present less fluctuations in the current than samples with low specific contact resistance. A possible explanation could be that in a good ohmic contact there is a high presence of defects at the interface metallic electrode/GaN channel which help the transit of carriers, but at the same time these defects create more fluctuations in the current and, therefore, more noise. On the other hand measurements on HEMTs have shown the typical behavior described in literature for the field-effect transistors; but a correlation between voltage breakdown and current fluctuations (the aim of this second part of the work on noise) has not been found.

3. The first analysis of the reliability of HEMTs has been carried out by means of a long-term DC-life test. The test has been based on three groups of devices biased in three different conditions and at three different junction temperatures. It has been found that the most detrimental condition is related to the presence of a high leakage current flowing through the gate electrode, specifically when the transistor is biased at medium-high drain voltage and in semi-open channel condition. In this condition the failure of the device is catastrophic and really fast. On the other hand high electrical field applied between gate and drain in closed channel condition (negligible drain current) can be handle by the transistor; but in this case the gate leakage grows at very high levels, causing the formation of several defects at the edge of the gate and in some case leading to the failure of the device.

4. The reliability has been also studied by means of a short-term reverse-bias step-stress. The purpose of this part of the work was to investigate which kind of damage the step stress induce in the samples. The obtained results show that the main effect is the creation of parasitic current path at the edge of the gate (phenomenon already seen on the long-term stress). The interesting result is that the degradation of the transistors submitted to the test is not only related to the electrical field applied between gate and drain, as often reported in literature; but other parameters, like the gate leakage current of the fresh device, the gate electrode material composition and the presence/absence of traps, can strongly influence the dynamic of the gate leakage increase.

In conclusions in this work several important aspect of the characterization of GaN-based device have been presented. Moreover the results and the argument proposed can be the starting point for further studies and analysis.
For example pulsed transconductance measurements can be extended by varying mea-

surement temperature and repeating the characterization for different V_{DS} values, with the aim of achieving a deeper understanding of trap-related processes in GaN-based HEMTs.
With concern to the low frequency noise measurements, a larger number of samples should be measured to verify the relation noise - contact resistance in TLM structures; while the measurements on transistors can be extended to other samples coming from different technologies as a diagnostic tool to detect differences and issues on the realization process.
Finally the reliability analysis has shown how the gate leakage and the electrical field are strictly correlated and they lead to the formation of defects and parasitic path at the edge of the gate: a study of the time dynamic of this degradation mechanism should be the next step to enhance the present work.

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