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Total Ionizing Dose Effects in Nanometer Scale CMOS Technologies Irradiated to Ultra-High Doses

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Dipartimento di Ingegneria dell'Informazione

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XXXIV Ciclo

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Abstract

Ionizing radiation may affect the electrical response of the electronic systems, inducing a variation in their nominal electrical characteristics and gradually degrading their performance. It is essential to study the total ionizing dose (TID) effects in electronic devices used in radiation environments such as space and avionics systems, high-energy physics experiments, and nuclear power plants. This thesis mainly focuses on the high-energy experiments, in which the large hadron collider (LHC) at CERN, especially the upgraded high luminosity-LHC, is currently expected to reach the highest TID level.

In this thesis work, I investigate the TID effects in nanometer scale CMOS technologies irradiated to ultra-high doses. The analysis of TID degradation mechanisms focuses on evaluating the measurable effects that affect the electrical characteristics of the devices and identifying the microscopic properties of the radiation-induced defects. The radiation measurements of several transistors based on the FinFET and gate-all-around FET (GAAFET) structures of different manufactures are performed with different device types, dimensions, chip layout and bias conditions, identifying the most TID sensitive parameters of the devices. The type, density, location and energy levels of the defects induced by ionizing radiation are studied through DC static characteristics and low-frequency $1/f$ noise measurements. The experimental measurements presented in this work provide a unique and comprehensive set of data, pointing out the strong effect of scaling down on the TID-induced phenomena in modern advanced CMOS technologies. All TID responses of the 16 nm bulk FinFETs and Si nanowire GAAFETs confirm the high TID tolerance of the nanoscale CMOS technologies with ultra-thin gate oxide, due to the reduced charge trapping in the gate dielectrics. However, the aggressive scale down of devices has led to new TID-induced effects related to other thick oxides and modern fabrication processes, such as shallow trench insulation (STI) oxides, spacer dielectrics, and halo implantations. Some new TID degradation mechanisms appear in 16 nm bulk FinFETs and Si nanowire GAAFETs, causing strong dependence on the irradiation bias conditions, channel length and chip layout. This thesis work identifies the weak points of FinFET and GAAFET technologies at ultra-high doses and provides chip designers with the key elements to improve their TID tolerance.

Contents

Terminology

ALICE – A Large Ion Collider Experiment

ASIC – Application Specific Integrated Circuit

ATLAS – A Toroidal LHC Apparatus

BJT – Bipolar Junction Transistors

CB – Conduction Band

CERN – European Organization for Nuclear Research

CMS – Compact Muon Solenoid

CTRW – Continuous Time Random Walk

DD – Displacement Damage

DFT – Density Function Theory

DUT – Device Under Test

ESD – Electro-Static Discharge

ELT – Enclosed Layout Transistor

EUV – Extreme Ultraviolet

GAA – Gate-All-Around

HL-LHC – High Luminosity-Large Hadron Collider

IC – Integrated Circuit

LDD – Lightly Doped Drain

LET – Linear Energy Transfer

LHC – Large Hadron Collider

LOCOS – Local Oxidation of Silicon

NW – Nano Wire

NWE – Narrow Width Effect

RINCE – Radiation-Induced Narrow Channel Effect

RISCE – Radiation-Induced Short Channel Effect

RNWE – Reverse Narrow Width Effect

RSCE – Reverse Short Channel Effect

RT – Room Temperature

RTN – Random Telegraph Noise

SEE – Single Event Effect

SCE – Short Channel Effect

SRB – Strain-Relaxed Buffer layer

SRH – Shockley Read Hall

STI – Shallow Trench Isolation

TEM – Transmission Electron Microscopy

TID – Total Ionizing Dose

VB – Valence Band

Chapter 1

Introduction

Innovations in semiconductor integrated circuits (IC) manufacturing technology have enabled transistors to scale to nanometer dimensions. Device dimensions and operating voltages of ICs are constantly shrunk to meet the ever-increasing demand for reduced power and increased operating speed of circuits. Scaling to feature sizes beyond sub-100-nanometer was made possible through innovations such as strained-Si technology, high-K gate dielectric, and transition from planar to tri-gate or FinFET device structures as well as extreme ultraviolet (EUV) lithography [1-4]. This has kept alive Moore's predictions of doubling transistor counts per IC every two years [5]. Figure 1 shows a chart of technology scaling as a function of year.

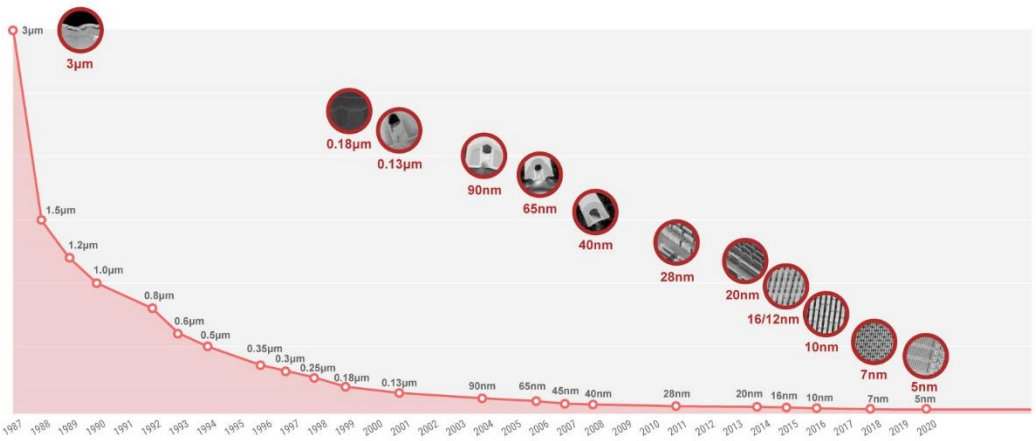


Figure 1.1: Technology scaling as a function of year. (From TSMC)

With decreasing feature sizes, reduced supply voltages, and increasing packing densities, radiation-induced effects are becoming more severe and complex threats to electronic components, capable of temporarily or permanently compromising the normal operation of circuits, applications and systems [6-11]. One famous catastrophic event caused by the effects of radiation was the failure of the communication satellite Telstar 1 in 1962. The malfunction of the satellite

control system was caused by the total ionizing dose (TID) degradation of some bipolar junction transistors (BJTs) [12]. This unexpected catastrophic event happened after a sudden increase of the radiation levels in Van Allen's belt as a result of high-altitude nuclear tests from USA and USSR [12-14].

Radiation effects in electronic circuits can be defined as interactions between particles and electronic components that can significantly affect the expected performances of the devices themselves. The sensitivity of the radiation-induced effects depends on the type of the device (e.g. MOSFETs, BJTs, diodes, etc.) and the energy and type of the incident particles (e.g. photons, protons, neutrons, electrons, heavy ions, etc.) [15, 16]. Different effects and associated physical mechanisms can be grouped into three main categories: total ionizing dose (TID) [17-19], displacement damage (DD) [20-22], and single event effects (SEEs) [23-27]. However, for the purpose of this thesis, we focus on the TID effects in modern CMOS technologies. TID effects are induced by the Coulomb interaction between the device materials and the ionizing particles, which generate charges that can be collected and trapped in some sensitive part of the device. These charges are typically stuck in the insulator materials and cause parametric shifts in the transistor electrical response [17-19]. Due to the presence of the gate oxide and other isolation oxides (SiO_2 is still widely used as main isolation material in advanced technology), CMOS technology is intrinsically sensitive to TID effects.

Electronic circuits operating in various radiation environments require different radiation tolerance, typical applications in high radiation environments include space and avionics systems, high-energy physics experiments, nuclear power plants, medical diagnostic imaging and therapy, industrial imaging and material processing. Among all the radiation environments, the large hadron collider (LHC) at the European Organization for Nuclear Research (CERN) [28], especially the upgraded high luminosity-LHC (HL-LHC) that is expected to be operational by 2025 according to the more recent schedule [29], is by far the one where the highest levels of TID are expected to be reached. Table 1.1 summaries the dose rates (rad/day) in four different radiation environments, while Figure 1.2 shows a comparison of the estimated TID levels for four different applications [8, 10, 31-39]. Compared to other radiation environments, HL-LHC is undoubtedly the harshest radiation environment in terms of the ionizing dose.

Table 1.1: Order of magnitude of the maximum dose rates in four different environments (approximately). (From [30])

	Ground level	Low Orbit	LHC	HL-LHC
rad/day	$\leq 10^{-3}$	$\sim 10^{-3}$-10^{0}	$\sim 10^{3}$	10^{5}

The LHC at CERN is housed in a tunnel of 27 km circumference and at a depth underground varying from 50 to 175 m, which is the largest and most powerful particle accelerator in the world. The LHC is built to collide two beams

of protons with a maximum energy of 7 TeV each and instantaneous luminosity of 10^{34} cm^{-2} s^{-1}. The main experiments in the 4 specific collision points are ATLAS (A Toroidal LHC Apparatus), CMS (Compact Muon Solenoid), LHCb (Large Hadron Collider beauty) and ALICE (A Large Ion Collider Experiment). This intense radiation environment poses unprecedented challenges for safe operation and performance quality of the silicon tracker detectors in the ATLAS and CMS experiments. The silicon trackers are crucial for the physics at the LHC experiments, and the inner layers, being situated only a few centimeters from the interaction point, are most vulnerable to beam-induced radiation [40].

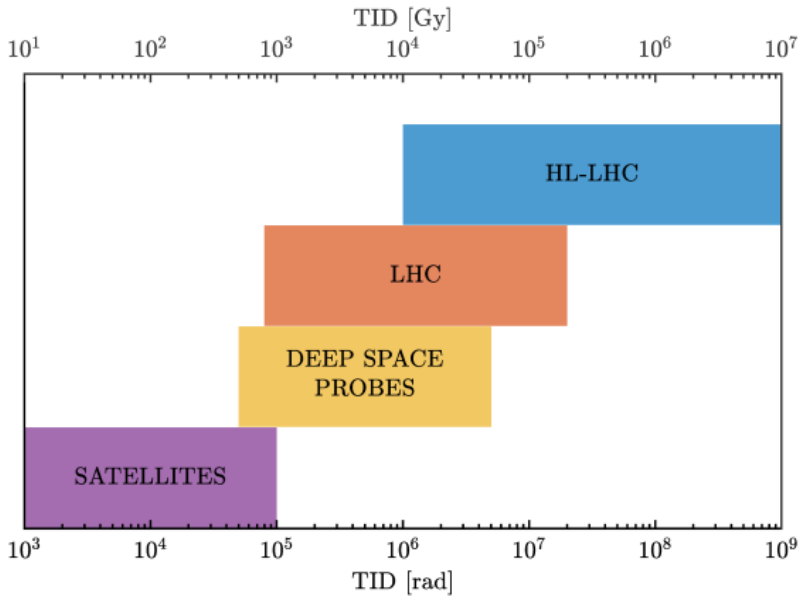


Figure 1.2: Estimated TID levels for four different applications. The maximum TID levels in HL-LHC is more than one order of magnitude higher than that in LHC and more than two orders of magnitude higher than that in deep-space probes. (From [30])

HL-LHC is the future upgrade of the LHC accelerator which aims at delivering an integrated luminosity up to 3000 fb^{-1} over about 10 years of operation, starting from 2025 [41]. The HL-LHC will reach a luminosity up to 5×10^{34} $cm^{-2}s^{-1}$, more than two times higher than LHC (2.1×10^{34} $cm^{-2}s^{-1}$). During 10 years of operation, the accumulation of ionizing dose will reach unprecedented levels, with peaks of 1 Grad(SiO_2) in the inner layer of tracker detector and an average dose rete of about 0.3 Mrad(SiO_2)/day [29, 42, 43]. Figure 1.3 shows the simulation of the TID levels expected in CMS in10 years of operation. The inner layer of tracker detectors is expected to be exposed to a TID levels ranging from 100 Mrad(SiO_2) to 1 Grad(SiO_2). These ultra-high ionizing doses will lead to very high particle fluxes and energy deposition in detector components which may cause serious damage, especially in the silicon tracker that is physically very close to the interaction point. Radiation damage could be either bulk damage, i.e., changes in the lattice structure of Si, or surface damage. The consequences would be increased leakage current, increase in the required biasing voltage and/or

reduced signal collection efficiency [40]. Therefore, present and future high-energy physics experiments require electronic circuits able to withstand ultra-high radiation levels.

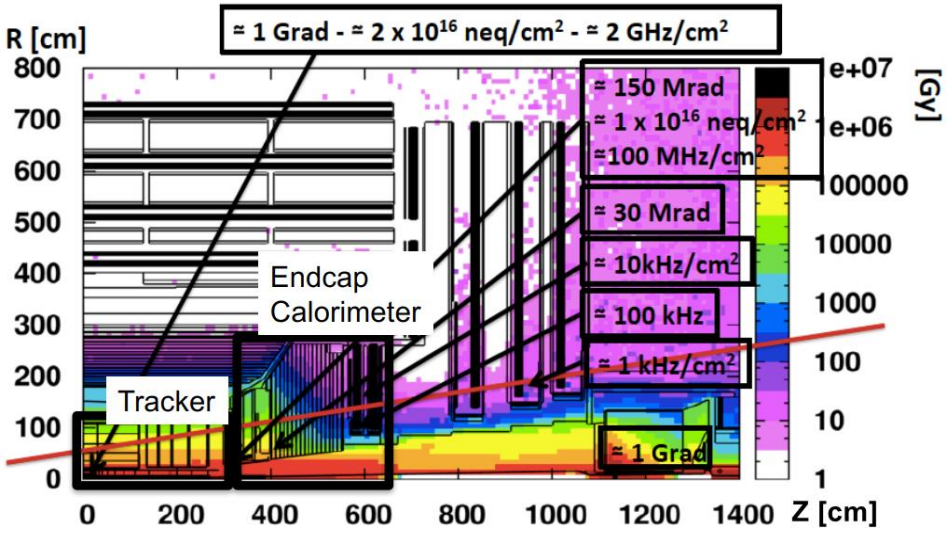


Figure 1.3: Simulation of the TID levels expected in CMS in 10 years of operation. (From [29])

The current tracker detectors in LHC use 250 nm CMOS technology, while the next generation of the application-specific-integrated-circuits (ASICs) for particle detectors in HL-LHC will be designed in more advanced technology nodes. The non-planar CMOS technologies, like 16 nm bulk Si FinFETs and Si nanowire Gate-All-Around FETs (GAAFETs), are promising candidates for the upgrade of the electronics in the tracker detectors of ATLAS and CMS experiments. The use of advanced FinFET- and GAAFET-based technology will allow greater computational power, increased functionality and better TID radiation tolerance [42, 43]. Therefore, it is very meaningful and necessary to explore how ultra-high radiation doses affect and modify the electrical characteristics of FinFETs and GAAFETs, identify the weak points of technologies, and provide designers with the key elements to improve the tolerance of technologies. In addition, since uniquely high TID levels in the LHC caused some new degradation phenomena, the identification process for electronic components designed to operate at low TID levels, such as space missions, may not be appropriate for evaluating the actual long-term degradation of components intended to be installed inside particle accelerators. Therefore, it is also very necessary to define a specific qualification procedure to ensure that the equipment produced can actually withstand the extremely high TID levels expected in the HL-LHC.

This thesis investigates the TID degradation mechanisms in 16 nm bulk FinFETs and Si nanowire GAAFETs irradiated to ultra-high doses via DC static and low-frequency noise measurements (In this thesis, we define that high doses

is 1∼10 Mrad(SiO_2) and ultra-high doses is $>$ 10 Mrad(SiO_2)). The radiation measurements are performed with different device types, dimensions, chip layout and bias conditions to identify the most TID sensitive parameters of the devices. The type, density, location and energy levels of the defects induced by ionizing radiation are studied through DC static characteristics and low-frequency noise measurements. The purpose of this work is to evaluate the qualitative responses of the tested devices and try to understand the TID degradation mechanisms. Experimental results confirm the high TID tolerance of the extremely thin gate oxides in nanoscale CMOS technologies. However, with the reduction of feature size of the device, new TID-induced effects appear in nanoscale technologies, due to the charge trapping in other thick oxides and advanced fabrication processes, such as shallow trench isolation (STI) oxides, spacer dielectrics, and halo implantations.

In order to fully interpret and analyze the experimental results, Chapter 2 presents the basic mechanisms of the TID effects in MOS transistors, focusing on the generation, transport and capture of the charges induced by ionizing radiation in the oxide and along the oxide/semiconductor interface. This chapter introduces several necessary concepts and fundamental phenomena that will be used through this thesis.

In Chapter 3, I summarize the main TID effects in modern CMOS technologies, which are related to the thick oxides and specific manufacturing processes, such as gate oxides, STI oxides, spacer dielectrics, and halo implantations.

Chapter 4 investigates the TID degradation mechanisms of 16 nm bulk Si FinFETs at ultra-high doses (1Grad (SiO_2)) for high-energy physics application. The TID effects are dominated by charge trapping in STI and its interface and also depend strongly on the channel length and bias conditions. For the first time, I observed evidence of the influence of halo implantations in FinFET devices with better TID tolerance in the shortest devices. Then I perform extensive experimental characterization by using $1/f$ low frequency noise measurements to investigate the microscopic nature, density and location of defects.

Chapter 5 shows the influence of fin- and finger-number on TID degradation of 16 nm bulk Si FinFETs at ultra-high doses for high-energy physics application. n- and p-FinFETs designed with different numbers of fins and fingers are irradiated up to 500 Mrad(SiO_2) and then performed DC static characteristics. The TID responses of nFinFETs are insensitive to fin number. However, pFinFETs show a visible fin-number dependence with worst tolerance of transistors with smallest number of fins. The fin number dependence may be related to a larger charge trapping in STI located at the opposite lateral sides of the first and last fins. In addition, both n- and p-FinFETs exhibit an almost TID insensitivity to finger-number.

In Chapter 6, I analyze the sample-to-sample variability induced by the TID

in 16 nm bulk Si nFinFETs by performing DC static measurements. A specially designed test structure consisting of several nominally identical FinFETs is used to maximize the match between transistors. The research results show a significant increase in sample-to-sample variability, which is also correlated to the initial process-dependent variability. This phenomenon is likely due to the impact of the random dopant fluctuations on TID effects.

In Chapter 7, the TID degradation mechanisms in a development-stage GAA nano-wire FET technology are explored at ultra-high doses, up to 300 Mrad(SiO_2), through DC and low frequency noise measurements. GAAFETs irradiated under different bias conditions show TID degradation that is dependent on channel type and length. Worst-case TID-induced degradation is found in p-channel devices with long channels, while n-channel devices exhibit the most favorable TID tolerance. TID effects are dominated by charge trapping in STI and spacer dielectric.

Finally, Chapter 8 summarizes all the results obtained.

Chapter 2

Basic Mechanisms of the TID Effects in MOSFETs

Ionizing radiation can induce charge accumulation at the dielectrics and dielectric/semiconductor interfaces of the devices, leading to a variation in their nominal electrical responses. The total ionizing dose (TID) effect is one of the main causes of damage to silicon-based electronic devices. It refers to the phenomenon where ionizing radiation-induced damage is long-term accumulated in electronic devices. This leads to their gradual performance degradation of MOSFET devices, such as threshold voltage shift, transconductance degradation, and leakage current increase. TID is the measure of the total energy absorbed by matter, and the most common unit used is rad (radiation absorbed dose) or the International System Unit, gray (Gy), where 1 Gy= 100 rad= 1 J/kg. Rad is typically used in the space community, as well as in this thesis.

In this chapter, the main concepts about basic mechanisms of the TID effects in MOSFETs have been extensively summarized, including the generation, transport and capture of the charges induced by ionizing radiation, as discussed in several excellent books [44, 45], articles [17, 19, 46, 47] and short courses.

2.1 Interaction of Photons with Solid Materials

Photons can interact with the matter through three main processes, including photoelectric effect, Compton scattering and pair production [48-51]. The probability of these effects occurring depends on the incident photon energy and the target material. As shown in Figure 2.1, at 10 keV, the X-ray photons interact with silicon (Z_{Si} = 14) and silicon dioxide (Z_O = 8) mainly through photoelectric effect [50, 51]. In this thesis, the spectrum of the X-ray source used in most radiation experiments reaches its maximum intensity of 10 keV.

Figure 2.2 shows a schematic representation of the photoelectric effect. The incident photon is completely absorbed by the target atom, which in turn releases

an electron. Once the electron is released, an electron-hole (e-h) is generated. At the same time, another electron coming from an external orbit will drop in the vacated state, resulting in the emission of a low-energy photon. Then the emitted electron can in turn directly ionize the surrounding material, generating e-h pairs along its path.

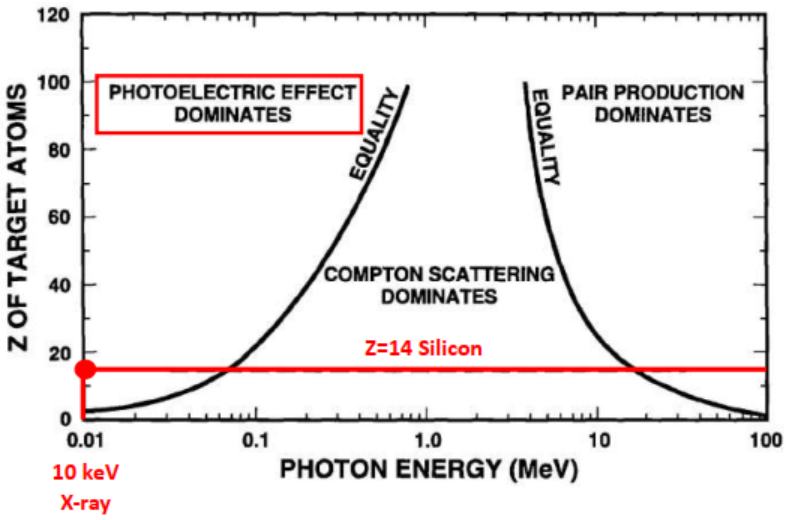


Figure 2.1: Relative weight of the main three photon-matter interaction processes at different energies and for several materials. The plot highlights in red that X-ray photons at 10 keV interact with matter through photoelectric effect. (From [48])

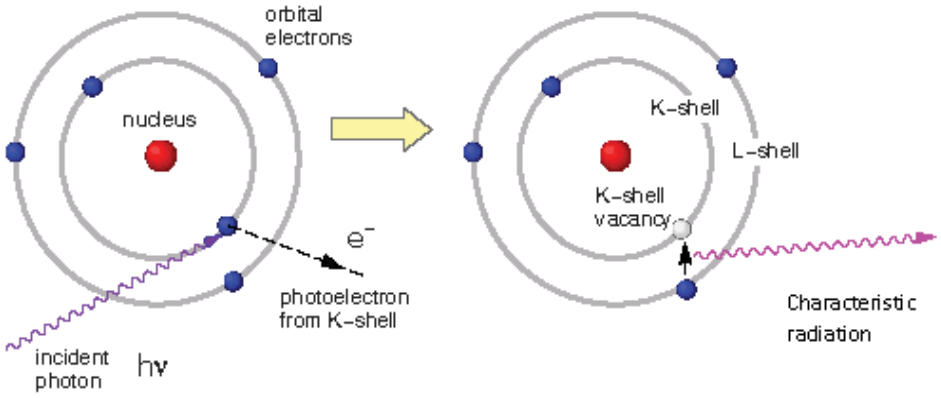


Figure 2.2: Schematic representation of the two processes of the photoelectric effect. (From [51])

The photoelectric process therefore ends with the generation of e-h pairs which is the key element for the TID-induced damage. Typically, during an X-ray exposure, most of e-h pairs are induced by ionizing electrons generated by the interaction between photons and atoms rather than the photon itself.

2.2 Transport and Capture of Charge in Oxides

When a MOS device is exposed to ionizing radiation, e-h pairs are generated in the oxides [17, 19, 46, 52, 53]. These charges can move through the oxide, where they can react with H atoms releasing H^+ ions (protons) and be trapped in the oxide traps. If these charges are not captured, they will eventually reach the oxide-silicon interface, where they can be swept out of the oxide under bias in picoseconds [54]. When the released H^+ ions reach the oxide-silicon interface, they react with Si-H, generating interface traps.

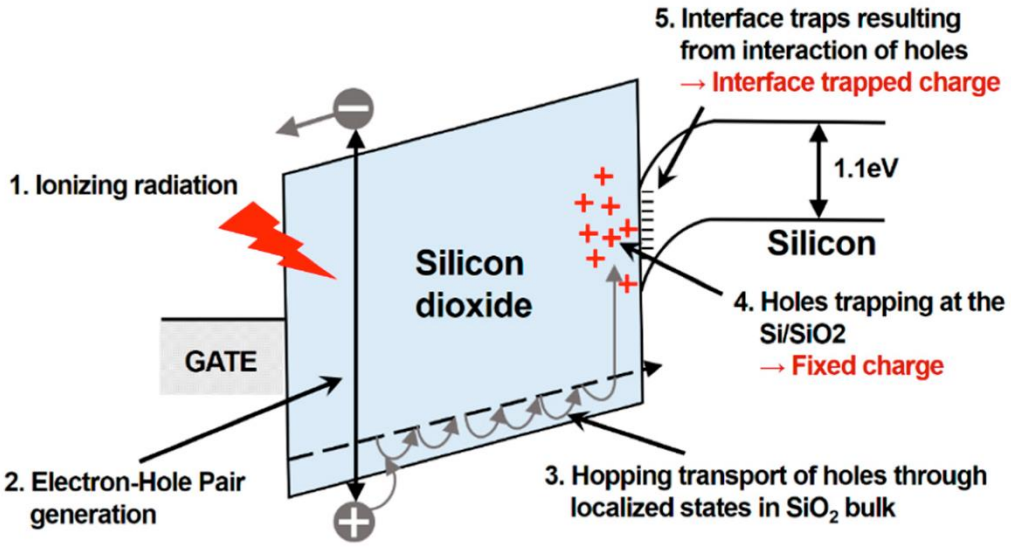


Figure 2.3: Schematic representation of the TID effects. The main processes of the TID mechanism related to the gate oxide are shown through the band diagram of a nMOSFET biased with positive voltage at the gate. (From [55])

Figure 2.3 shows a schematic representation of the energy band diagram of a nMOSFET with positive voltage at the gate under ionizing radiation. The TID degradation process includes the following stages:

1) Generation of electron-hole pairs
2) Recombination of electron-hole pairs
3) Transport of holes in gate oxide
4) Release of hydrogen ions
5) Capture of holes close to the SiO_2/Si interface
6) Formation of interface traps

In the rest of this chapter, we will analyze each of these stages in detail.

2.2.1 Generation of Electron-Hole Pairs

When photons hit a MOSFET, they can ionize the atoms in the device material, generating e-h pairs. In SiO_2, the energy required to generate an e-h pair is about 17 eV [56], and the charge pair volume density generated per rad is about 8.1×10^{12} pairs/cm^3 [17]. After the charge is generated, some of them will quickly recombined, as described in the next section.

2.2.2 Recombination of Electron-Hole Pairs

The mobility of electrons in SiO_2 is approximately 20 $cm^2V^{-1}s^{-1}$ at room temperature, with the saturation velocity about 1×10^{12} cm s^{-1} for electric field higher than 5×10^{12} V cm^{-1} [54, 57-59]. Even in an oxide with a thickness of 100 nm, electrons will be released from SiO_2 within picoseconds if the polarization voltage is high enough (> 5V in this case) to allow them to reach saturation velocity. On the contrary, the mobility of holes in SiO_2 is extremely low, several orders of magnitude lower than the mobility of electrons [52, 60-61]. Therefore, in the very fast moments after the generation of e-h pairs, the positive field applied at the gate drifts most of electrons out of the gate oxide within picoseconds with some electrons recombining with the holes. After the initial recombination, the effects due to electrons are definitely negligible compared to those induced by holes. The fraction of e-h pairs that escape the recombination is called electron-hole yield or charge yield.

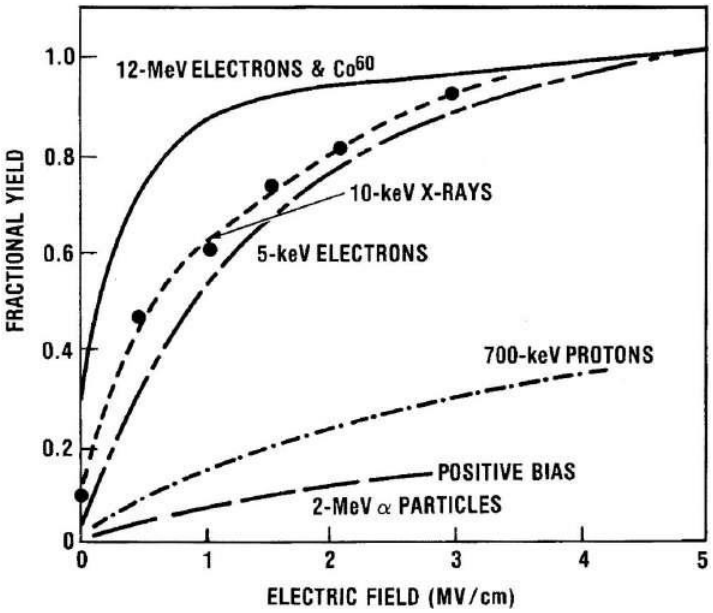


Figure 2.4: Charge yield as a function of applied electric field for different types incident particles or photons in SiO_2. (From [17])

The amount of initial recombination is highly dependent on the magnitude

of the electric field through the gate oxide and the energy and type of incident photons or particles. Figure 2.4 shows the influence of the electric field to the charge yield for α particles, low-energy protons, electrons, X-ray, and gamma rays (Co-60) [49]. For all the types of incident particles and photons, the charge yield increases with the increase of the electric yield, since the higher electric yield reduce the probability of holes recombining with electrons. Radiation with higher ionizing power forms a charge column with higher density e-h pairs, which limit the average distance between generated e-h pairs, consequently promoting the recombination of electrons and holes (higher recombination rate) [52]. On the other hand, weakly ionized particles produce relatively isolated e-h pairs, decreasing the recombination probability for neighboring pairs (lower recombination rate) [52].

There are two models to study the recombination and the charge yield, the geminate model and columnar model respectively. In the geminate model, the average distance between e-h pairs is much larger than the thermalization distance required by e-h recombination. Therefore, each e-h pair of recombination reactions is performed separately, with negligible interactions with other e-h pairs. However, in the columnar model, the distance between e-h pairs is much shorter than the thermalization distance (5 nm) [62, 63]. And compared with the geminate model, there are more electrons in the vicinity of the generated holes , leading to a greater probability of recombination [64]. Obviously, the actual recombination process for most of the materials and particles is a combination of the geminate and columnar models.

2.2.3 Transport of Holes in Gate Oxide

The holes in gate oxide are drifted slowly from the generation position to the negative electrode by the electric field. If the gate of the device is biased with a positive voltage, the trapped holes move toward the SiO_2/Si channel interface, while a negative voltage drifts them toward the gate/SiO_2 interface. The transport of holes follows the Continuous Time Random Walk (CTRW) hopping transport mechanism [49, 65, 66], in which holes in the SiO_2 are transported by polaron hopping. The term polaron refers to a situation in which a charged carrier interacts strongly with the surrounding atoms, resulting in lattice distortion in its immediate vicinity. Polarons enter the gate oxide through localized shallow trap states characterized by a random spatial distribution with an average distance of about 1 nm [65]. When a hole passes through SiO_2, the charge of SiO_2 will cause distortion of its local potential field. This local distortion increases the trap depth at the localized position, which tends to confine the hole to its immediate vicinity. As a result, holes tend to trap themselves at the localized positions.

Polaron hopping makes the hole transport dispersive, as hole transport occurs over many steps in time after a radiation pulse. Transport of holes is strongly dependent on temperature, electronic field and gate oxide thickness [67-

69]. Figure 2.5 shows the influence of temperature and electric field on the hole transport. The variation of the flat-band voltage is plotted as a function of the time needed to remove the effect of the radiation-induced trapped charge after an irradiation pulse, in different conditions of temperature and bias. The gate oxide is irradiated with a relatively fast (4 μs) 12 MeV electron pulse, in order to minimize the time between the end of the generation/recombination process and the measurements. It is worth noting that the flat-band voltage almost fully recovers to its pre-irradiation value of high temperature and/or high electric field. This means that only a small number of holes are trapped in the trapping centers (see subsection 2.2.5 for details). In addition, [17] shows that the hole transit time is proportional to the fourth power of the oxide thickness (t_{ox}), this means that in modern advanced CMOS devices with $t_{ox} \leq 10$ nm and $E_{ox} \geq 2$ MeV, all un-trapped holes can be swept out from the gate oxide few instances at room temperature after the e-h pairs generation.

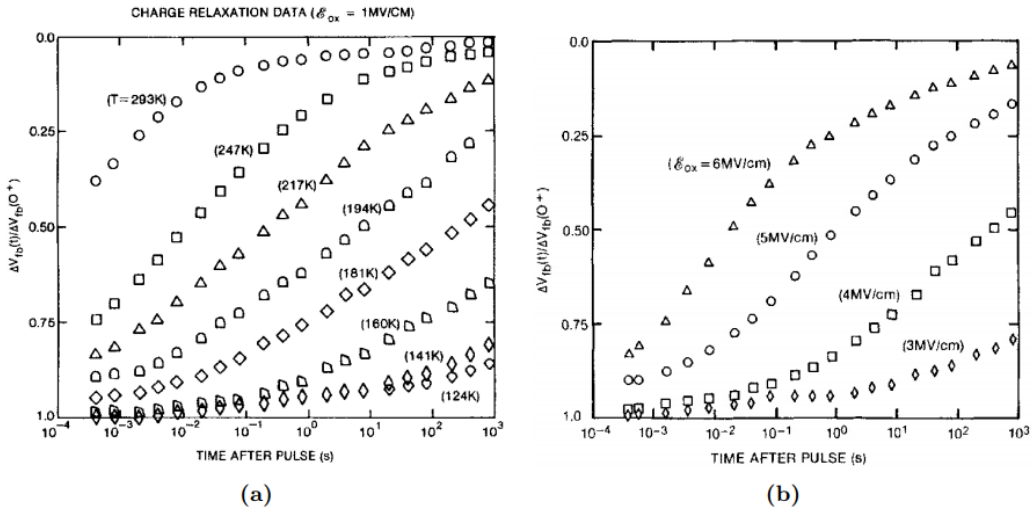


Figure 2.5: (a) Normalized flat-band voltage recovery of MOS structure (t_{ox} = 96.5 nm) after a pulsed irradiation with 12 MeV electrons. (a) Irradiations at different temperatures with 1 MV/cm of electric field in the oxide. (b) Irradiations at different electric fields at 79 K. (From [67, 68])

Although hole transport depends on temperature, electric field, and gate oxide thickness, these parameters only change the time scale of the process, not its behavior, that is therefore universal in nature [70]. As shown in Figure 2.6, the variation of the flat-band voltage is plotted as a function of the scaled time $t/t_{1/2}$ [70]. The time $t/t_{1/2}$ is defined as the time needed to the flat-band voltage to recovery of 50% ($\Delta V_{fb}(t)/\Delta V_{fb}(0^+) = 0.5$). All curves were approximately overlap one to each other, indicating the universality and dispersion of the transport. The hole transport can be well described with the continuous time random walk (CTRW) formalism, useful to model hopping transport processes, as shown by the solid line in Figure 2.6.

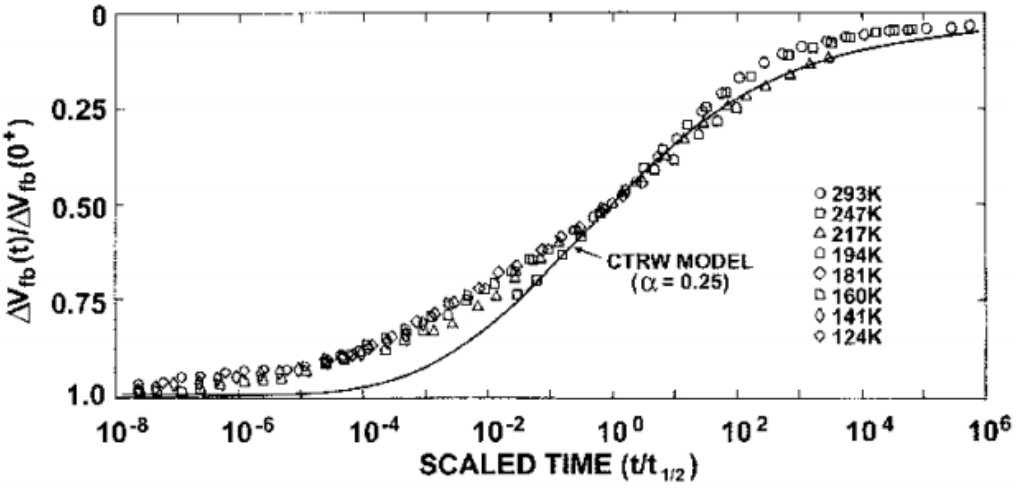


Figure 2.6: The normalized flat-band voltage shifts at different temperature and same scaled time. The behaviors are almost identical, proving the universality of the response. The solid curve presents the fitting results obtained by using the CTRW model with $\alpha = 0.25$. (From [70])

Trapped holes in the gate oxide can be neutralized by two mechanisms: tunneling of electrons from the silicon into oxide traps, and thermal emission of electrons from the oxide valence band into oxide traps [71-74]. The main phenomenon of charge neutralization depends on the spatial and energy distribution of the oxide trap. Typically, oxide traps close to the SiO_2/Si interface are neutralized by electron tunneling. On the other hand, thermal emission neutralization occurs when the energy level of the oxide traps are close to the oxide valence band [74]. Moreover, the neutralization rate can be strongly affected by temperature and electronic field.

2.2.4 Release of Hydrogen Ions

Due to the widespread use of hydrogen in the fabrication process of modern CMOS technologies, when the holes are drifted in the gate oxide by the electric field, they reacts with H present in the gate oxide, releasing hydrogen ions (H^+) [75-76]:

$$h^+ + H \text{ (in oxide)} \rightarrow H^+$$

Here h^+ stands for the hole. The hydrogen ions released in this process play an important role in the formation of interface traps (see subsection 2.2.6 for details).

2.2.5 Capture of Holes Close to the SiO_2/Si Interface

When the holes are drifted toward the SiO_2/Si interface by a positive gate bias, they can be captured by a large number of defects which are mainly caused

by the outward diffusion of oxygen atoms from SiO_2. The hole trapping defects can be identified with oxygen vacancies in the SiO_2 structure [77, 78].

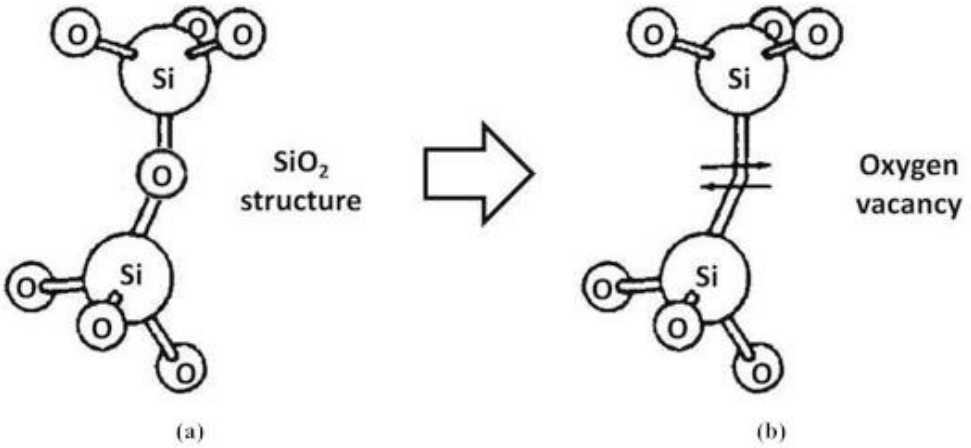


Figure 2.7: (a) Typical atomic structure of SiO_2 material layer. (b) Oxygen vacancy is missing oxygen atom, responsible for the defects called E' center. (From [77])

In the typical atomic structure of SiO_2 material layer, one Si atom is bonded to four O atoms, as shown in Figure 2.7(a). Each of this four O atoms is shared between two Si atoms. When an oxygen atom disappears (oxygen vacancy), as shown in Figure 2.7(b) and Figure 2.8 (a), the two Si atoms are weakly bonded together, a structure generally called E' center. A radiation-induced hole can easily break the weak Si-Si bond and recombine with one of the two electrons shared between the two Si atoms [77, 78]. When one electron is recombined by a hole, the other remaining electron of the Si-Si bond is shared between the two Si atoms, we refer to it as an E'_δcenter, a structure composed by a positive trapped charge Si [77, 78], as shown in Figure 2.8(b). On the other hand, if the other remaining electron is mainly associated with just one of the two Si atoms, we obtain an asymmetrical positively charged structure, generally called E'_γ center. It is generated by the positively charged Si atom and the neutral Si atom with unpaired spin [77,78]. Both E'_δ center and E'_γ center are responsible for the generation of positive trapped charges.

Positive charges trapped in the center of E' can undergo a neutralization (annealing) process, which requires the simultaneous removal of both unpaired spins and net positive charges. As shown in Figure 2.8(c), an electron can tunnel from the close Si substrate to the E' center, where it fills the half-filled orbital, neutralizes the positive net charge and eliminates the unpaired spin. If the tunneled electron recombines with the positive charged Si atom, the Si-Si bond is reformed and the annealing is permanent (Figure 2.8(c)→(a)). On the other hand, since the positively charged silicon atom has a more relaxed lattice, it is generally less attractive from an energy point of view than neutral Si atom. Therefore, the tunneled electron can also be captured by the neutral Si atom to compensate

positively charged neighboring Si atom. In this case, the bond between the two Si atoms is not reformed, and the extra electron can tunnel back out of the gate, again leaving a net positive charge, especially when a negative gate bias is applied (Figure 2.8(c)→(b)), this annealing process is reversible [77, 78].

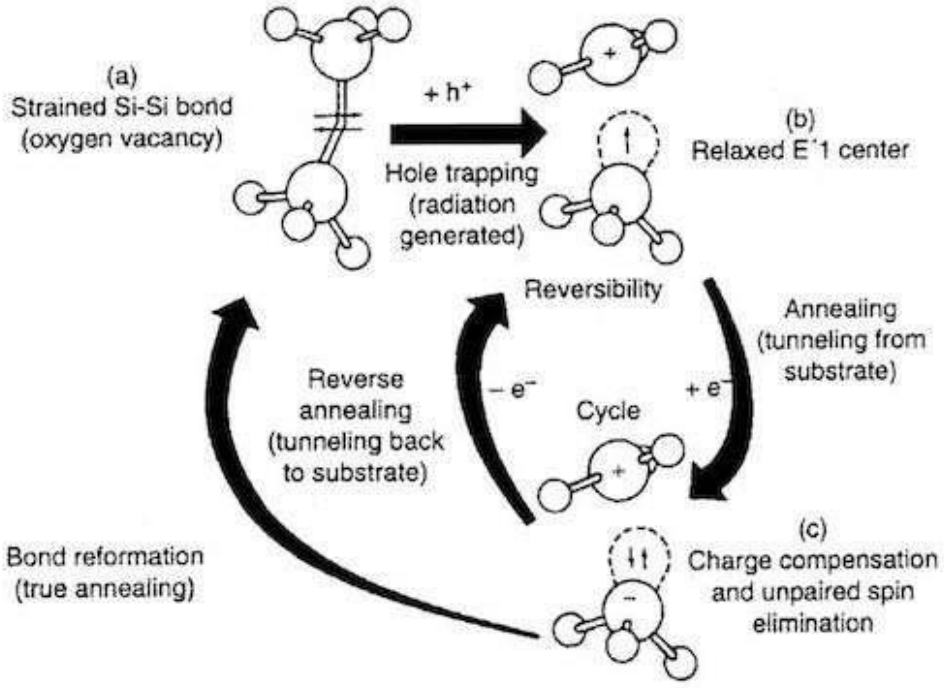


Figure 2.8: Generation and annealing of oxide trapped charge. (From [78])

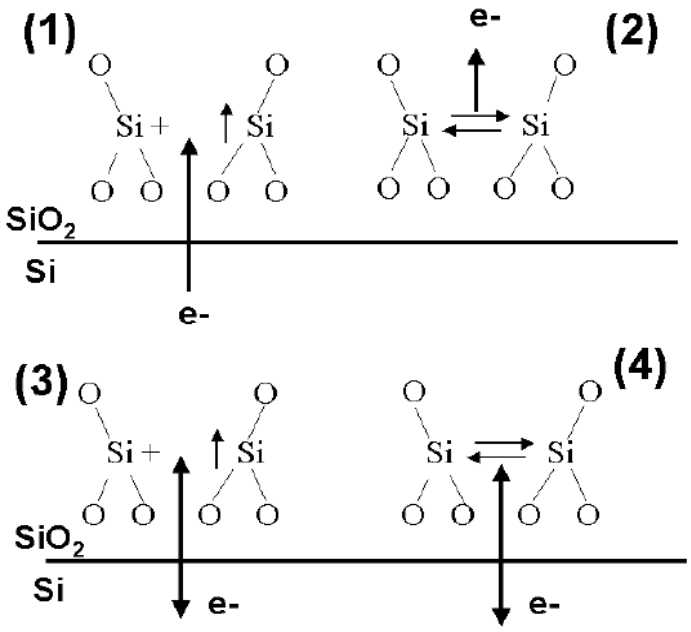


Figure 2.9: Schematic illustrations of the emission and capture of electrons in E' center contributing to hole trapping (1), (2) and low frequency $1/f$ noise (3), (4). (From [79])

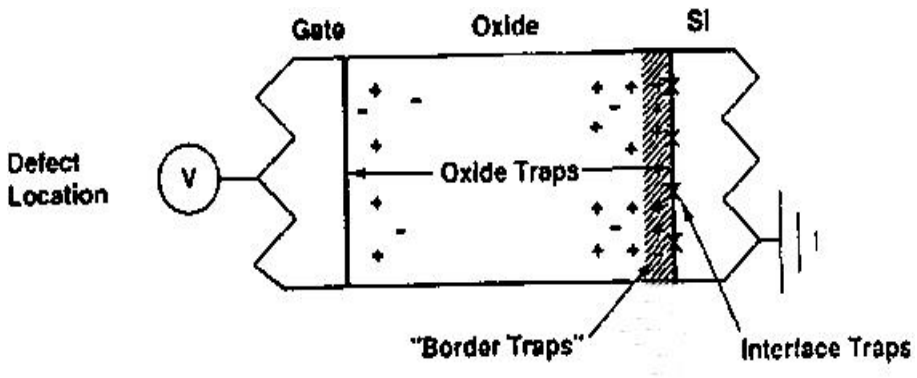


Figure 2.10: Schematic illustration of defects in MOS device: oxide traps, border traps and interface traps. (From [80])

The probability that a trapped charge in the gate oxide is neutralized by an electron coming from the Si bulk is strongly dependent on the distance between the oxide trap and the interface. The oxide traps relatively far from SiO_2/Si the interface have little possibility to be reached by electrons from the Si bulk, so the charge trapped in these defects is annealed over a relatively long period of time by electron tunneling and thermal emission [73, 74]. This more stable trap results in positive charge buildup in the gate oxides, as shown in Figure 2.9(a) and (b). On the other side, if the oxide traps are close to the SiO_2/Si interface, they can easily exchange electrons with the Si substrate in a relatively short time, depending on the applied electric field, so they can quickly react to the change of gate bias, switching back and forth from the positive charged to the neutral configuration [79]. This kind of oxide traps are defined as border traps, as a rule of thumb, all the E' center within 3 nm of the SiO_2/Si interface are typically considered as border traps [80, 81]. In addition, the border traps are responsible for hysteresis and low frequency $1/f$ noise, and the noise is caused by electrons exchange between silicon atoms and positively charged E' centers (Figure 2.9(3)) and between silicon atoms and weak Si-Si bonds (Figure 2.9(4)) [79, 82].

2.2.6 Formation of Interface Traps

The interface traps are precisely positioned at the interface between the SiO_2 and the Si substrate. Unlike border traps, when they exchange charge with the Si substrate, the capture and emission of charge in/out interface are possible with no barrier of carriers. The essence of interface traps is mainly dangling bond defects, generally called P_b center, severely affecting the carrier mobility and the recombination rate of carriers in the channel. In Si MOSFET devices, the most abundant and important of these P_b center is the P_{b0} defect, while marginal effects are typically due to the defect type, generally called P_{b1} [83, 84]. These two kinds of interface trap defects in (111), (110) and (100) Si substrate, P_{b0} and P_{b1}, are illustrated in Figure 2.11.

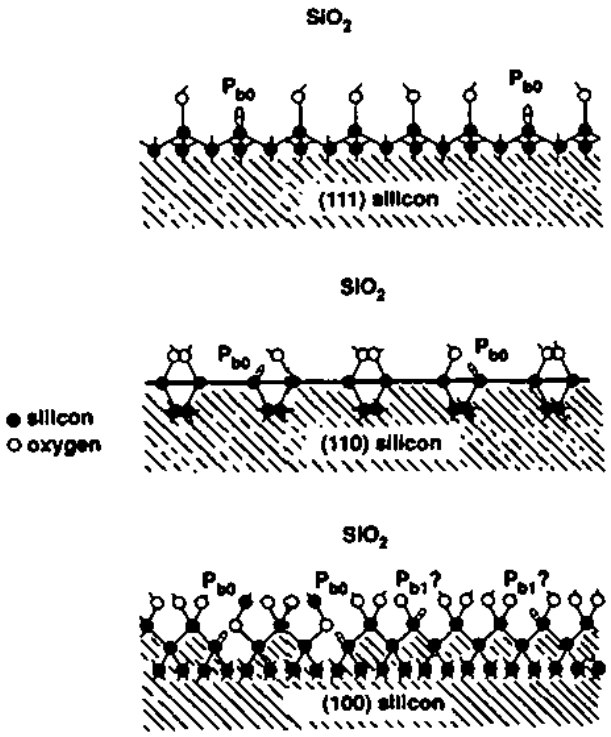


Figure 2.11: Schematic illustration of the P_{b0} and P_{b1} interface traps in (111), (110) and (100) Si substrate. (From [84])

The formation of dangling bonds depends mainly on two reactions, the first one is between the radiation-induced trapped holes and hydrogen containing oxide defects (D'H), releasing hydrogen ions (H^+) [85], as said in subsection 2.2.4. Since most interface traps are generated by H^+ around or above room temperature, the generation of P_b center mainly relies on the presence of H^+ near the interface [76, 86]. The second source of H^+ is the dopant-H complexes in the Si bulk, holes interact with the complexes leading to the creation of H^+ [87]. When H^+ diffuses to the SiO_2 interface or is drifted by the electric field to the interface, it can interact with the hydrogen of the H-passivated dangling bonds (D) [85]. The following reaction summarizes the formation of an interface dangling bond:

$$SiH + H^+ \rightarrow D^+ + H_2$$

Where D^+ is the dangling bond defect that creates P_b center.

P_b centers can either accept or donate electrons, depending on their positions relative to the Si mid-gap E_M and the Fermi E_F levels. As shown in Figure 2.12, donor-like defects are mostly at the bottom part of the band. When they sit above the Fermi level, they tend to release electrons, consequently becoming positive, while they are neutral below the Fermi level. On the other hand, acceptor-like defects are neutral above the Fermi level, and when they sit below the Fermi level, they tend to capture electrons, consequently becoming negative [88-90].

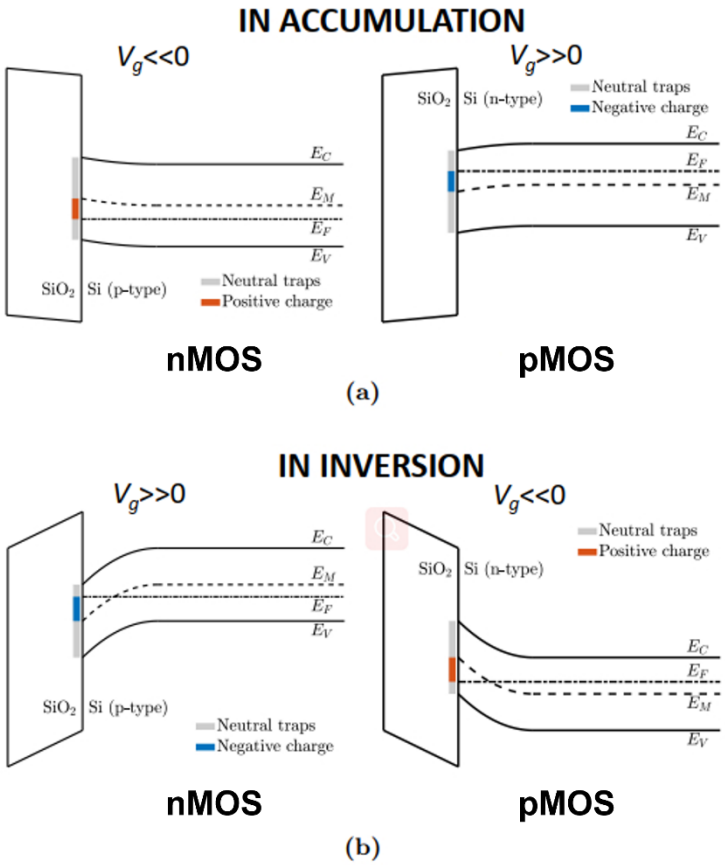


Figure 2.12: Schematic illustration of energy band of nMOS (left) and pMOS (right) devices. The sign of the net trapped charge at the interface depends on the Fermi level position at the channel surface. (a) Off-state with channel in accumulation and (b) on-state with channel in inversion. (From [30])

Therefore, while the charge trapped in the oxide is always positive, the sign of the net charge trapped at the interface is dependent on the applied gate bias, which can control the Fermi level position at the surface. For instance, in nMOS (p-type Si substrate) devices biased in inversion with $V_{gs} \gg 0$, the interface trapped charge is negative, while in pMOS (n-type Si substrate) devices biased in inversion with $V_{gs} \ll 0$, the interface traps are positively charged.

Chapter 3

Overview of the TID Effects in Modern CMOS Technologies

TID effects in MOSFETs are based on the ionization of the device materials, generating charge that can be collected in some sensitive regions of the device. Insulators are the most sensitive materials, such as gate oxides, in which ionizing radiation can induce charge trapping both inside and at their interfaces. However, with the scaling down of CMOS technology nodes, the gate oxide layers thickness shrinks to nearly 1 nm, the TID effects related to gate oxide becoming less and less problematic [17, 18, 46, 47]. This leads to new TID effects related to other thick oxides and specific fabrication processes e.g., shallow trench insulation (STI) oxides, spacer dielectrics, and halo implantations.

In this chapter, I summarize four main TID effects in modern CMOS technologies: gate-oxide related effects, STI-related effects, spacer-related effects, and halo-related effects.

3.1 Gate-Oxide Related Effects

As said in Chapter 2, the oxide-trapped charge is always positive, while the charge trapped at the interface is dependent on the gate bias. In nMOS devices, which are typically applied positive bias ($V_{gs} > 0$), the interface traps are mostly negatively charged, while in pMOS devices they are predominantly positive. The difference sign in the trapped charge results in a substantial difference in the overall ionizing radiation response of nMOS and pMOS devices, with the latter being generally more susceptible to TID damage.

The most efficient way to evaluate TID damage to transistors is to measure the DC static I_d-V_{gs} response (transfer characteristic) in linear region. Figure 3.1 shows the schematically the typical I_d-V_{gs} curves of nMOS and pMOS transistors. The black curves represent the response before the irradiation. The effect of oxide-trapped charge (positive charge) is shown by the red curves, which exhibit

a parallel shift of I_d-V_{gs} curves [17, 18, 46]. In nMOS transistors, this shift leads to a reduction of threshold voltage (V_{th}) and an increase of the off-state current I_{off} as well as the maximum drain current $I_{on\text{-}lin}$ at linear regime. In pMOS transistors, the V_{th} increases negatively, while I_{off} and $I_{on\text{-}lin}$ decrease. The threshold voltage shift induced by the positive trapped charge in the gate oxide can be calculated by the following formula:

$$\Delta V_{ot} = \frac{t_{ox}}{k_{ox}\varepsilon_0} q\Delta N_{ot}$$

where t_{ox} is the thickness of the gate oxide, k_{ox} is the dielectric constant of the gate oxide, and ε_0 is the permittivity of free space [91].

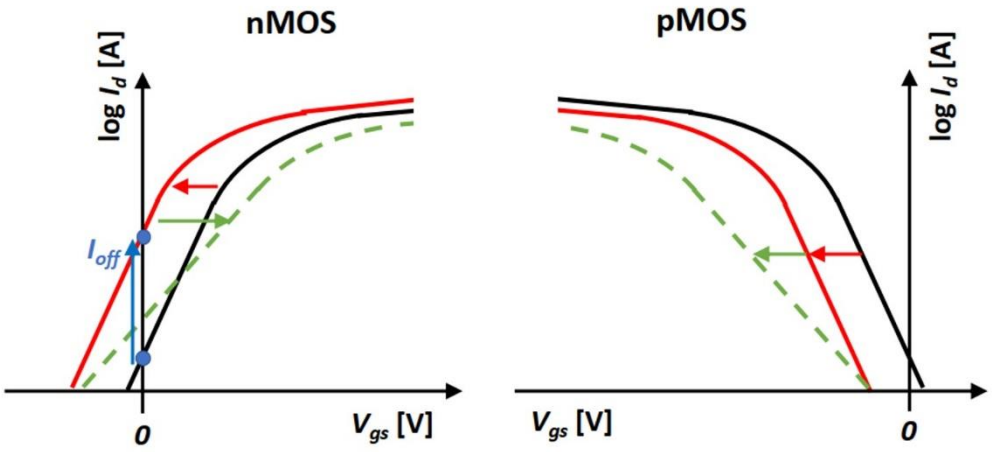


Figure 3.1: Schematic illustration of the TID effects on the I_d-V_{gs} response of nMOS (left) and pMOS (right) devices. The threshold voltage, drain current and leakage current are evidenced. In black pre-rad devices, in red the effects of charges in the oxide (typically during irradiation) and in green the effects of interface traps.

The effect of interface traps is shown by the green dotted curves, which exhibit a parallel shift of I_d-V_{gs} curves in the opposite direction. In nMOS transistors, interface traps are predominantly negative, causing a positive threshold voltage shift, and the negative charge can compensate partially or completely the effects of the oxide trapped holes. When the effect of the negative charge is dominant, a rebound effect is typically visible in the threshold voltage [17, 18, 46]. However, in pMOS transistors, the positive interface traps induce a negative threshold voltage shift, which is identical to the effect of oxide-trapped charge, so their effects accumulate due to the same charge sign [17, 18, 46].

Border traps can also change the charge state as the DC bias at the gate changes. When testing the DC static characteristics, it is difficult to distinguish the effects of interface and border traps. The key difference is the rate of charge exchange between the trap and the Si substrate. Border traps are able to capture and emit electrons at slow time rates, typically $<$ 100 Hz [82]. On the contrary,

the time rates of interface traps is typically $>$ 1 kHz [80, 61]. In general, during an experimental measurement of the I_d-V_{gs} response, the border traps can contribute to hysteresis, subthreshold stretch-out, and threshold voltage shift, depending on their emission/capture times compared to the measurement time. Traps with emission/capture rates slower than the total time for a V_{gs} sweep are able to contribute just to hysteresis and threshold voltage shift, but not to the subthreshold stretch-out. On the contrary, border traps with emission/capture rates faster than the total time for a V_{gs} sweep are able to increase the subthreshold stretch-out [79]. In addition, other measurement techniques, like low frequency $1/f$ noise, are typically used to investigate the effects of border traps, which will be discussed further in the following chapters by presenting some experimental results.

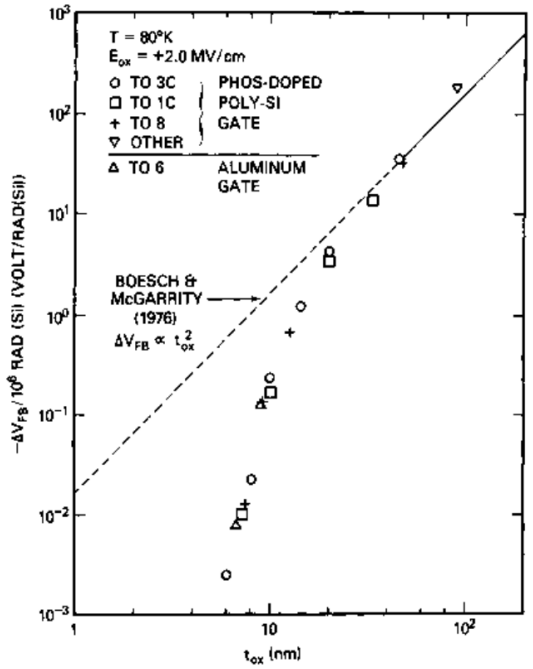


Figure 3.2: Flat-band voltage shift per unit dose as a function of gate oxide thickness in MOS capacitors irradiated at 80 K with a Co-60 γ-rays. The dashed curve indicates the assumption of t_{ox}^2 dependence for thick gate oxide. (From [92])

With the device scaling down, the TID effects related to the gate oxide have become increasingly less problematic [17, 18, 46, 47]. Figure 3.2 shows the relation between the radiation-induced charge trapping in the gate oxide and its thickness, it plots the flat-band voltage shift per unit dose of several MOS capacitors with different gate oxide thickness (t_{ox}) [92, 93]. In general, when $t_{ox} >$ 10 nm, the decreasing trend of the flat-band voltage shift per unit dose is proportional to t_{ox}^2 [94]. When $t_{ox} <$ 10 nm, the reduction of holes trapping is much more rapid than the expected t_{ox}^2 dependence visible in thick gate oxide. This sudden reduction of holes trapping is associated with the tunneling electrons that neutralize trapped holes in the approximately 3 nm range at the metal/oxide

or oxide/semiconductor interface.

The relation between the radiation-induced generation of interface traps and the gate oxide thickness follows a similar trend of the gate oxide charge. Figure 3.3 shows the density of interface traps per unit dose as a function of the gate oxide thickness in several MOS capacitors. Similarly to the oxide-trapped charge, When $t_{ox} < 10$ nm, the density of interface traps suddenly decreases. Tunneling electrons from metal/oxide or oxide/semiconductor interfaces neutralize the trapped holes in the oxide, avoiding the release of H^+ responsible for the generation of interface traps [76, 95-97]. In addition, Figure 3.3 also shows that the interface trap density of MOS devices with positive gate bias is higher than that with negative gate bias during the irradiation. This bias dependence is in agreement with the generation and release of H^+. When applied positive gate bias, H^+ can be drifted towards the gate SiO_2/Si interface, where it can interact with the hydrogen of the Si-H bonds and generate interface traps [85, 95].

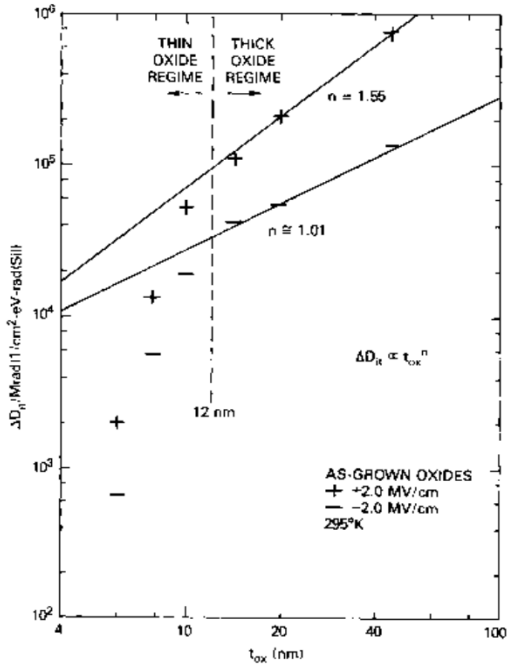


Figure 3.3: Density of interface traps per unit dose and energy D_{it} as a function of gate oxide thickness in MOS capacitors irradiated with Co-60 γ-rays in two different irradiation electric fields of ± 2 MV/cm. The values of D_{it} were estimated via the AC conductance method at 1 kHz. (From [95])

The reduction of gate-oxide related effect is of great benefit to the TID response of modern CMOS technologies [47, 98]. However, with the advent of high-k gate materials and advanced structures used in the modern CMOS technologies, the TID effects have become increasingly difficult to predict [47]. In fact, gate oxides are not the unique insulator layer in modern MOS devices. Some recent work [99-105] explores new TID degradation mechanisms related to

other two dielectrics: shallow trench isolation oxides and spacer oxides.

3.2 STI-Related Effects

Shallow trench isolation (STI), also known as box isolation technique, is an integrated circuit feature which prevents electric current leakage between adjacent semiconductor device components. STI is generally used on CMOS process technology nodes of 250 nm and smaller. Older CMOS technologies and non-MOS technologies commonly use isolation based on local oxidation of silicon (LOCOS) [106]. Typical field-oxide STI thickness is in the range of 100 nm to 1000 nm, much thicker than the gate oxide [106]. Unlike gate oxides which are typically grown by thermal oxidation, STI oxides are produced using a variety of deposition techniques, which are poorly controlled and are considerably different compared to those used for the gate oxides [71].

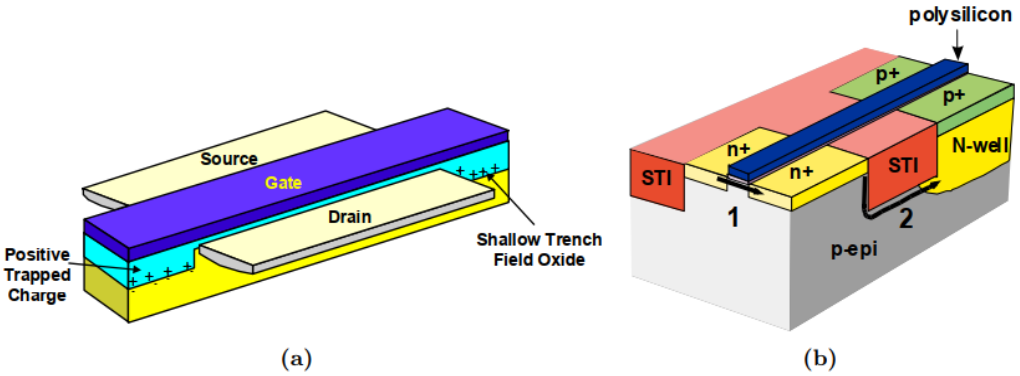


Figure 3.4: (a) Schematic illustration of a transistor with STI. (b) The two arrows indicate two possible leakage paths of the MOS device using STI. The first leakage path is at the edge of the device between the source and drain. The second leakage path occurs between the n-type source and drain regions of a nMOSFET and the n-well of an adjacent pMOSFET. (From [46] and [106])

Ionizing radiation effects related to the STI oxides are a well-known problem of the radiation hardness of CMOS devices, which is induced by the positive charge buildup in the STI oxides, as shown in Figure 3.4(a). The positive charge in the STI can significantly affect the radiation hardness of nanoscale transistors through two main degradation effects, one is increasing the radiation-induced standby currents, the other is enhancing the threshold voltage shift in narrow channel transistors, also known as radiation-induced narrow channel effect (RINCE).

The increase of the standby current is due to leakage paths induced by the radiation-induced positive charge buildup in STI [101-103,107]. The basic

mechanism of TID-induced leakage phenomena is that positive charge in STI oxides invert the adjacent P-type Si region, forming an inversion layer around the STI sidewall. When the surface inverts, a conductive path is created, significantly increasing the leakage current. Figure 3.4(b) shows two possible leakage paths of the MOS device. The first leakage path is drain-to-source leakage in a single nMOSFET, and the second one is source-to-well leakage between two devices with different channel types [46, 106]. These leakage paths will result in an increase in the static current of the integrated circuits operating in a radiation environment. Since the radiation-induced charge buildup in the STI oxides is mainly positive which can invert the adjacent p-type Si region, its effect is generally more severe on nMOS transistors [46, 101-103].

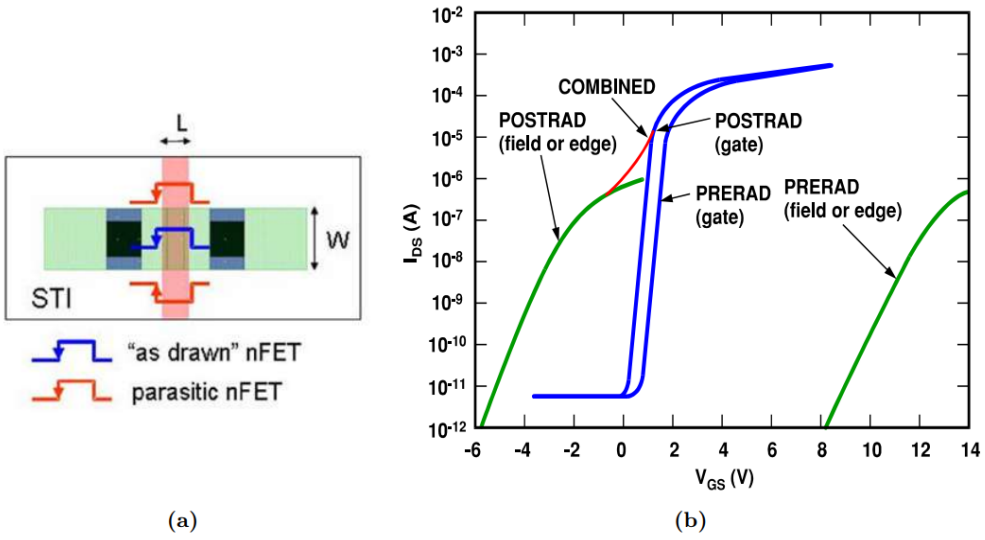


Figure 3.5: (a) The effect of STI-related standby current increase is modelled with nMOSFET with two lateral parasitic n-channel transistors. (b) Representative example of I_d-V_{gs} curves for a gate-oxide transistor and for its parasitic field-oxide transistor before and after the irradiation. The radiation-induces charge buildup in the STI oxide, shift the threshold voltage of the parasitic field-oxide transistors with a consequent increase in leakage current at $V_{gs} = 0$. (From [18] and [46])

For drain-to-source leakage, the sidewalls of the trench oxide produce a lateral leakage path, which become the dominant contributor to the off-state leakage current of nMOSFETs. As shown in Figure 3.5(a), the STI oxides form two lateral parasitic n-channel transistors [18]. At the edge of the gate transistor, the gate polysilicon extends over the field-oxide zone, as shown in Figure 3.4(a). A parasitic field-oxide transistor consists of the gate polysilicon, part of the field oxide, and the source and drain of the gate transistor. The effect of the excess leakage current from a parasitic field-oxide transistor on the total drain current of the transistor is illustrated in Figure 3.5(b) [46]. The plot presents the drain-to-source current I_{ds} versus the gate-to-source voltage V_{gs} for a nMOS transistor before and after the irradiation. The initial threshold voltage of the parasitic STI

oxide transistor is relatively large, due to the large thickness of the STI oxide. During the irradiation, positive charge is trapped in the STI oxide, leading to a large negative threshold voltage shift of the parasitic STI-oxide transistor. If the threshold voltage of the parasitic STI-oxide transistor shifts enough to negative values, it can contribute to increase the off-state leakage current, preventing the gate oxide transistor to be completely turned off.

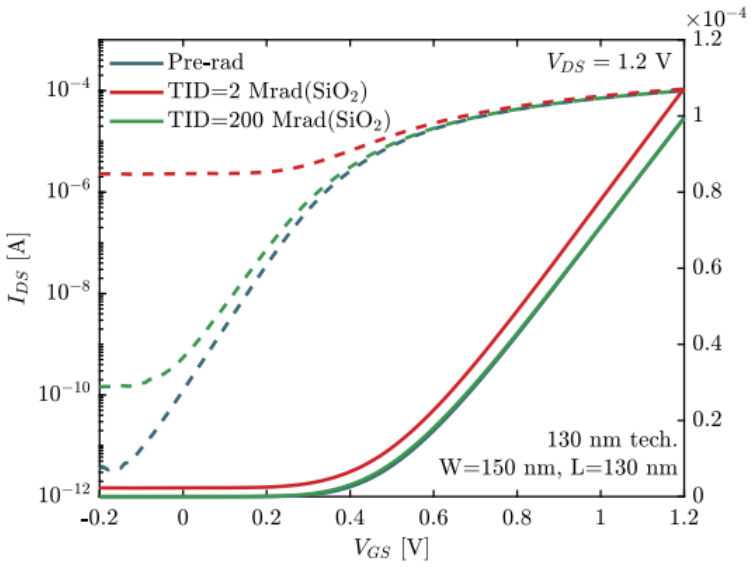


Figure 3.6: I_d-V_{gs} characteristics in saturation region (V_{ds} = 1.2 V) of 130 nm nMOS transistors. The device was irradiated with X-rays up to 200 Mrad(SiO_2). The dashed lines show the curves in logarithmic scale (left axis) while the solid lines refer to the characteristics in linear scale (right axis). (From [30])

Figure 3.6 reports an example of experimental evidences about the catastrophic effects related to charge buildup in the STI oxides. The plot shows the I_d-V_{gs} characteristics in saturation region (V_{ds} = 1.2 V) of 130 nm nMOS transistors, irradiated with X-rays up to 200 Mrad(SiO_2). The DC statics characteristics are tested before the irradiation, at 2 Mrad(SiO_2), and at 200 Mrad(SiO_2), respectively. The significant increase in the drain-to-source leakage current can be clearly noticed in the curve plotted in logarithmic scale (red dashed line, left axis) at 2 Mrad(SiO_2), about six orders of magnitude. When the $V_{gs} \leq$ 0.2 V, the leakage current is insensitive to the gate voltage, indicating that the charge responsible for the inversion of the parasitic channels is probably extending in the lower part of the STI sidewalls, far from the STI-gate corner, where the gate control is weak or completely absent [107, 108]. While at 200 Mrad(SiO_2) the leakage current decreases to the initial (pre-rad) value with a slight increase in the subthreshold swing (the inverse of the slope of the linear portion, in logarithmic scale, of the I_d-V_{gs} below the threshold voltage). These two effects suggest generation of interface traps along the STI sidewalls, which compensates the effect of the positive trapped charge in the STI oxides. This

phenomenon of the leakage current recovery is clearly shown in Figure 3.7, which plots the leakage current (I_d at V_{gs} = 0 V) as a function of the dose for 130 nm nMOS transistors with different channel dimensions. The rebound of the leakage current appears at about 2 Mrad(SiO_2), the generation of positive charge reaches saturation at this point, and the formation of negative charge trapped at the interface makes it more difficult for new positive charges to reverse the parasitic n-channels. When the total doses excess 3 Mrad(SiO_2), the interface traps begin to dominate this leakage performance.

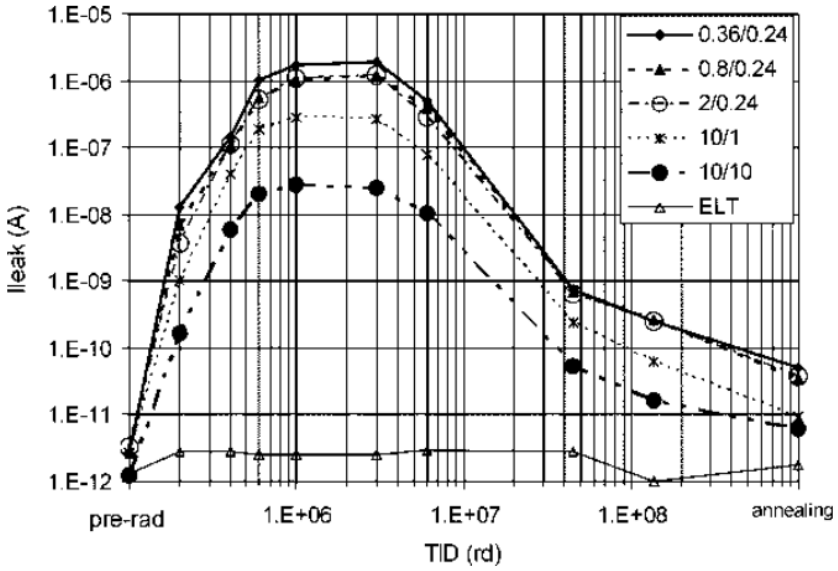


Figure 3.7: Leakage current as a function of dose for 130 nm nMOS transistors with different channel dimensions. Devices were irradiated with X-rays up to 136 Mrad(SiO_2). (Form [100])

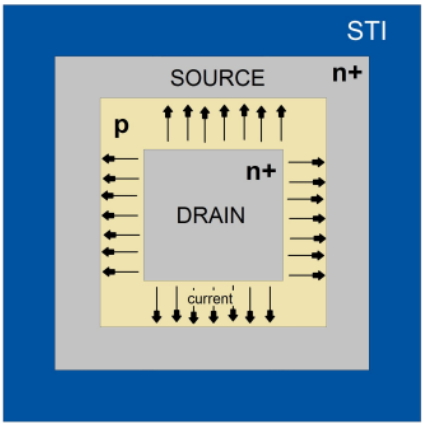


Figure 3.8: Schematic illustration of an enclosed layout transistor. The STI oxides do not face the channel and the trapped charge does not create leakage paths. (From [30])

In addition, Figure 3.7 highlights that the STI-induced leakage current is slightly dependent on the channel width, while it can be almost completely suppressed with hardness by design techniques, in particular, the enclosed layout transistors (ELT), where the STI oxides do not face the channel, resulting in that the charge trapped in the STI does not create leakage paths [100, 109-111], as schematically represented in Figure 3.8. These ELTs are clearly extremely useful for the design of electronic devices operating in radiation environments. However, there are some drawbacks that limit their use. Since ELTs occupy a larger surface than standard transistors and their behaviors are complex to accurately simulate by digital design tools, after the systematical use of ELTs for all circuits developed in 250 nm CMOS for the LHC experiments, this design is only partially adopted at 130 and 65 nm technologies for the HL-HLC.

In general, the formation of the leakage current is a complex mechanism involving both oxide-trapped and interface-trapped charge, and depends on the quality of the STI oxides and on the applied bias during the irradiation, making it difficult to predict its effect on electronic circuits.

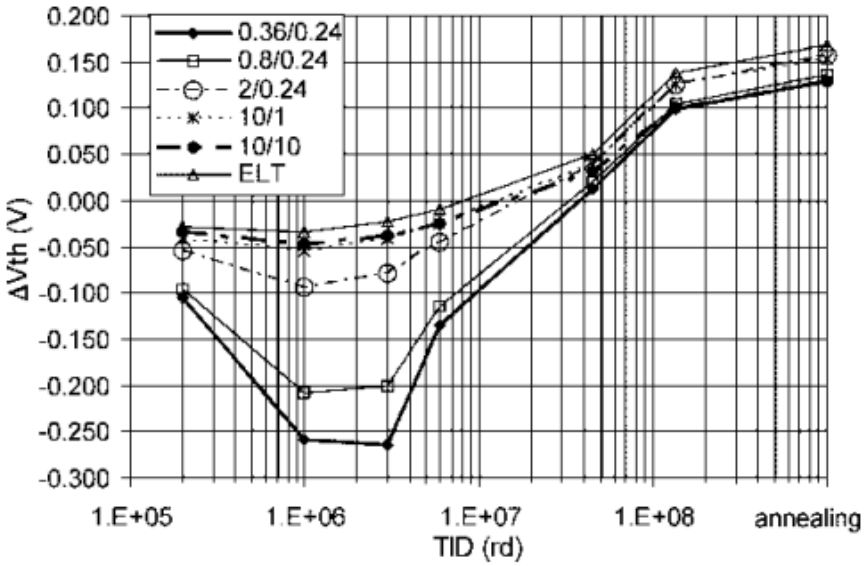


Figure 3.9: Threshold voltage shift as a function of dose for 130 nm nMOS transistors with different channel dimensions. Devices were irradiated with X-rays up to 136 Mrad(SiO_2). (Form [100])

In addition to the leakage current, charge trapping in the STI of highly scaled technologies can cause larger degradation of the threshold voltage in narrow channel transistors [30, 71, 100-102]. This effect is named radiation-induced narrow channel effect (RINCE) and it affects the TID response of nMOSFETs and mostly pMOSFETs. Figure 3.9 shows the channel width dependence of the 130 nm nMOS transistors, the plot presents the threshold voltage shift as a function of the cumulated doses for devices with different channel width. The

threshold voltage degradation of narrow channel transistors is more severe than that of wide channel transistors. In narrow channel devices, the two lateral STI are close to each other and the electronic generated by the positive trapped charge in the STI oxides can influence also the central part of the channel. Therefore, in narrow channel nMOSFETs, the positive charge in the STI oxides contributes to invert the p-type substrate, inducing a decrease in the threshold voltage with cumulated doses [71, 101]. Similarly to the rebound phenomenon appears in the leakage in Figure 3.7, a rebound of the threshold voltage occurs at about 2 Mrad(SiO_2), due to the generation of interface traps along the gate oxide and the STI sidewalls, which can compensate the positive oxide-trapped charge. When the total doses excess 100 Mrad(SiO_2), the negative interface-trapped charge begins to dominate the TID response and causes the threshold voltage to shift forward. On the contrary, in narrow channel pMOSFETs, the positive charge in STI oxides contributes to accumulate the n-type substrate, inducing a increase in the absolute value of threshold voltage [71, 101].

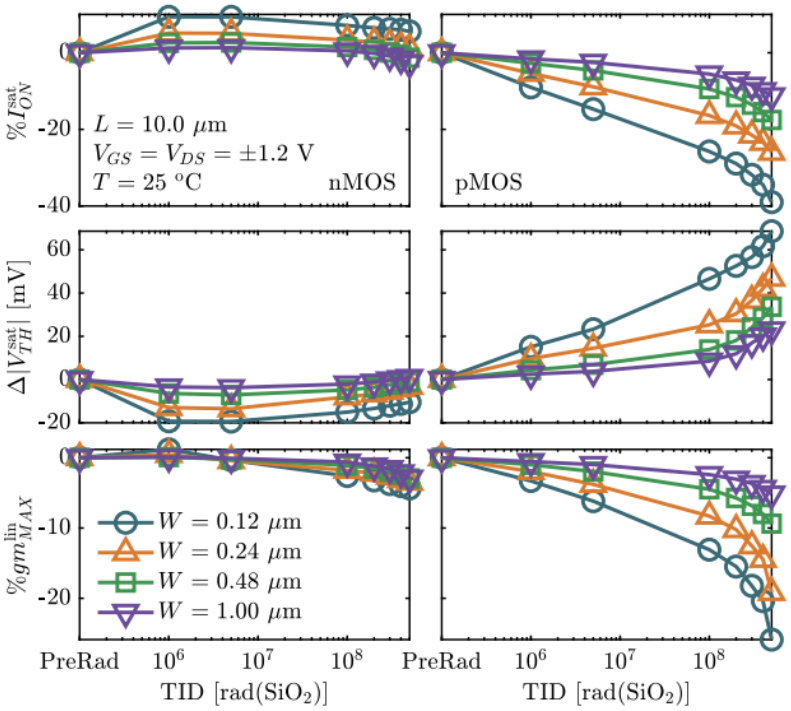


Figure 3.10: Degradation of the maximum drain current, threshold voltage, and maximum transconductance as a function of dose in nMOSFETs and pMOSFETs with identical channel length of 10 µm and different channel width. Transistors were irradiated with X-rays up to 500 Mrad(SiO_2). Devices were measured in linear region at room temperature. (From [30])

Figure 3.10 reports the degradation of the maximum drain current, threshold voltage, and maximum transconductance as a function of dose in 130 nm nMOSFETs and pMOSFETs. Transistors with four different channel width and

identical channel length of 10 μm were irradiated with X-rays up to Mrad(SiO_2). In both nMOSFETs and pMOSFETs, the TID degradation is channel-width dependent with worst-case in narrow-channel transistors. However, pMOSFETs clearly show worse TID degradation than nMOSFETs, exhibiting a strong channel-width dependent degradation, which is dominated by the collapse of drain current caused by the large degradation of transconductance and by the threshold voltage shift. The large degradation of transconductance is typical in narrow transistors affected by RINCE [101, 104, 112, 113]. In fact, the transconductance of a transistor is proportional to the effective channel width. Radiation-induced positive charge in STI oxides of P MOSFETs or negative interface-trapped charge along the STI sidewalls of nMOSFETs can deplete the lateral Si-channel regions close to the STI sidewalls, consequently reducing the effective channel width.

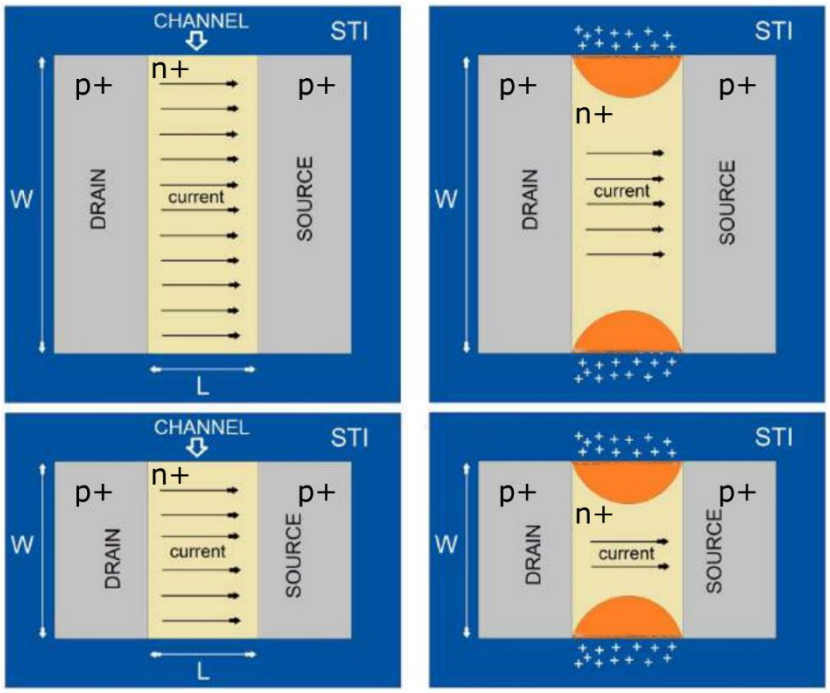


Figure 3.11: Schematic illustration of the radiation-induced narrow channel effect (RINCE) in pMOSFETs. The electric field generated by the charge trapped in the STI oxides depletes the lateral regions close to the STI sidewalls, reducing the effective channel width and mostly degrading the current flow of the narrow-channel transistor. (From [30])

The radiation-induced reduction of the effective width in pMOSFETs is schematically presented in Figure 3.11, that shows a top view of a wide transistor (top row) and a narrow transistors (bottom row) working in inversion region (on-state), before (left column) and after (right column) irradiation. Since the thickness and quality of the STI do not change with the size of the transistor, the

amount of STI-trapped charge after irradiation is more or less the same for both the narrow and the wide MOSFETs. As a result, the radiation-induced reduction of the effective width is the same for the narrow and wide transistors, the percentage of channel width influenced by irradiation is obviously higher in the narrow device. Therefore, the narrow channel transistor is proportionally much more affected by the irradiation [71, 101, 104, 114].

The STI-related effects, RINCE and the leakage current increase, can be a serious threat to the reliability of ASICs operating in radiation environments, provoking a strong variation from the nominal performance and an increase in the power consumption. Both effects can be avoided using enclosed layout transistors, which prevent the charge trapped in the STI oxides from affecting the electric field in the channel.

3.3 Spacer-Related Effects

In addition to STI oxides, spacer oxides used in the manufacturing process of modern CMOS technologies can also severely degrade the radiation hardness of MOS transistors. The recent miniaturization of devices to nanometer scale has led to the use of the lightly doped drain (LDD) regions, which is used to decrease the impact of hot carriers, eliminate breakdown, and moderate threshold voltage dependence on channel length [115]. Figure 3.12(a) shows a schematic view of a modern manufacturing process technology using LDD regions, a moderate doping implantation covering the full drain/source area is first applied to produce a shallower and more lightly doped region [71, 102].

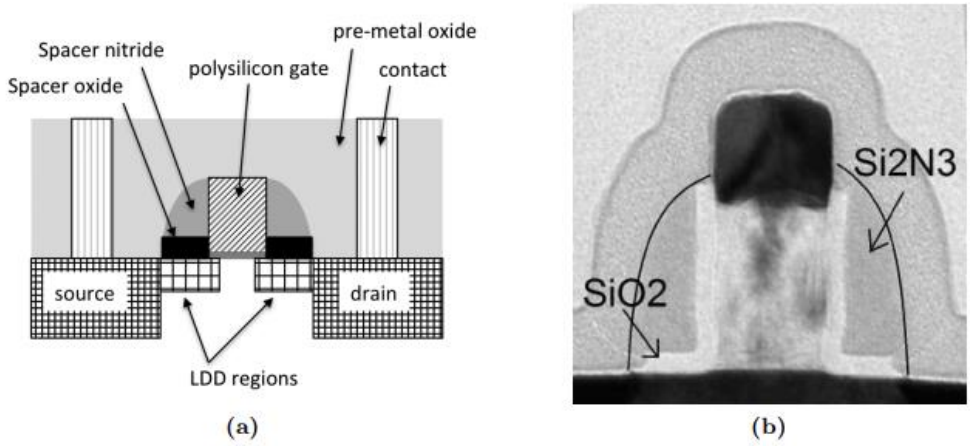


Figure 3.12: (a) Schematic view of the fabrication process of a MOS transistor with spacers used for the implantation of LDDs. (b) TEM image of a 65 nm CMOS technology node, presenting a significant volume of the spacer dielectrics. (From [101, 102])

Spacers are then grown around the gate polysilicon, and source / drain regions are implanted. The spacers prevent the high doping implants of source / drain regions to reach the proximity of the channel, allowing the formation of LDD regions characterized by a lower doping than drain/source implantations [71, 102]. As shown in the Figure 3.12 (b), a transmission electron microscopy (TEM) image of a 65 nm CMOS transistor, spacers are usually formed by a layer of 10-20 nm-thick SiO_2 surmounted by a thicker Si_3N_4 layer [115, 116]. Notably, the thickness of these insulators is significantly higher than that of the gate oxides, thus making them more sensitive to degradation induced by ionizing radiation.

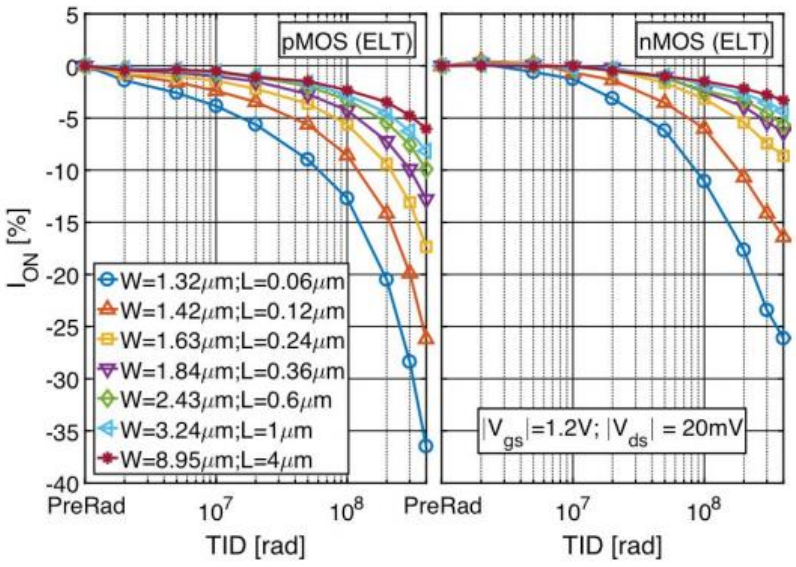


Figure 3.13: Degradation of the maximum drain current in strong inversion ($|V_{gs}|$ = 1.2 V) and in the linear regime ($|V_{ds}|$ = 20 mV) for pMOS (left) and nMOS (right) transistors designed with ELTs. Devices were irradiated with X-rays at room temperature up to 400 Mrad(SiO_2). (From [102])

Unlike the STI-related effects, the TID effects related to the spacer oxide have been reported recently by few works [30, 101, 102], and the research on its degradation mechanisms started to be investigated in the last few years, as its impact is evident only at very high doses, much higher than that of interest for space application. The Spacer-related effects has been studied mainly in 65 nm CMOS technology [30, 101]. The first clue of a possible impact of spacers on the TID response reported in Figure 3.13 was the discovery of a channel length dependence in the degradation of the drain current of irradiated devices [101]. The plot shows the percentage degradation of maximum drain current as a function of cumulated dose in pMOS and nMOS transistors designed with enclosed layout, which can completely avoid the STI-related effects. Devices are irradiated with X-rays up to 400 Mrad(SiO_2) and measurements are carried out in the linear regime at room temperature. After the irradiation, the reduction of the

maximum drain current is observed in both pMOSFETs and nMOSFETs, with the worst-case performance degradation in short channel devices. This channel length dependent phenomena is named radiation-induced short channel effect (RISCE), which is even more obvious in pMOS transistors [101].

Further research demonstrates that the channel length dependence is particularly dominant after annealing at high temperature. Figure 3.14 shows the degradation of the maximum drain current for nMOS (top row) and pMOS (bottom row) transistors in 65 nm CMOS technology with four different channel length and an identical channel width of 20 µm. Devices are irradiated with X-rays up to 400 Mrad(SiO_2) (left column) and then annealed at 100 °C for 100 h (right column). The channel of these transistors under test is wide enough to avoid any effects related to charge buildup in the STI oxides. The longest transistor has a very small degradation ($<$ 5%) after the irradiation and a negligible evolution after the high-temperature annealing, proving the extreme robustness of the gate oxide. The shortest pMOS device presents the largest TID degradation ($\sim$ 30%) after the irradiation, especially after annealing of 100 h at 100 °C, almost 60%. In addition, notably, the degradation of the drain current is almost negligible ($<$ 5%) for both nMOS and pMOS transistors at doses less than 10 Mrad(SiO_2), thus the RISCE is dominant only at ultra-high doses.

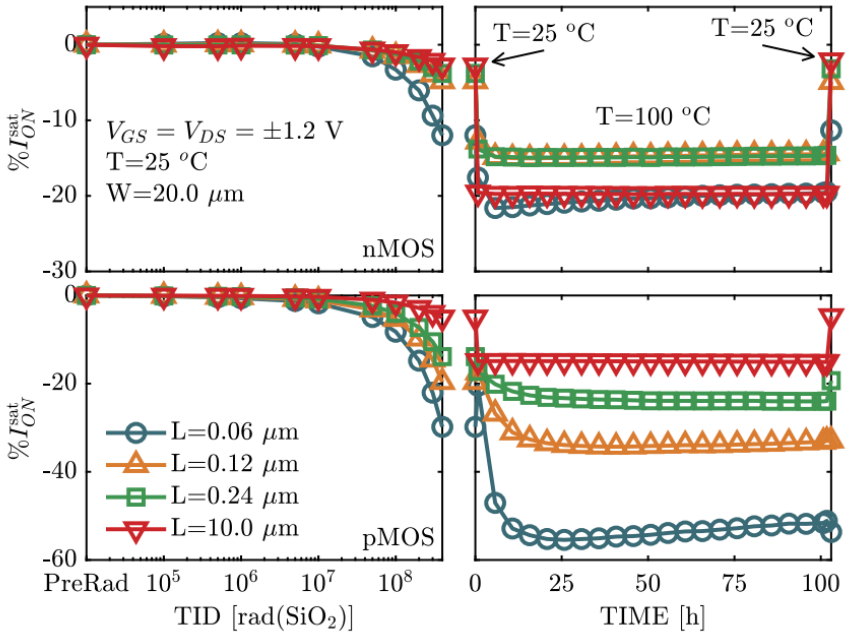


Figure 3.14: Degradation of the maximum drain current in linear regime ($|V_{ds}| = 20$ mV) for nMOS (top row) and pMOS (bottom row) devices in 65 nm CMOS technology designed with four different channel length and an identical channel width of 20 µm. Transistors are irradiated with X-rays up to 400 Mrad(SiO_2) (left column) and then annealed at 100 °C for 100 h (right column). All the measurements during the annealing test were carried out at 100 °C, except the first and the last points, which were measured

at room temperature (25 °C). (From [30])

Figure 3.15 reports the causes of such a large degradation in the short channel pMOS transistor [30]. The I_d-V_{gs} characteristics in linear regime ($|V_{ds}| = 20$ mV) is measured before exposure, after irradiation, and at the end of 21 hours annealing at 100 °C. The measurements are carried out in nominal (solid lines) and reversed (dashed lines) configurations. In the nominal mode, the I_d-V_{gs} is tested at $V_{ds} = -20$ mV, while in the reversed mode, the I_d-V_{gs} is tested at $V_{ds} = 20$ mV, which means that the drain terminal is switched with the source terminal. In Figure 3.15, the nominal and reversed curves overlap each other, indicating a symmetric TID response of the transistor. After irradiation, the degradation of the maximum drain current is caused by the increase of the series resistance of the transistor with slight threshold voltage shift and negligible variation of the subthreshold swing. After annealing, the degradation of the maximum drain current is due to an extremely large threshold voltage shift together with an increase of the subthreshold swing [30, 101].

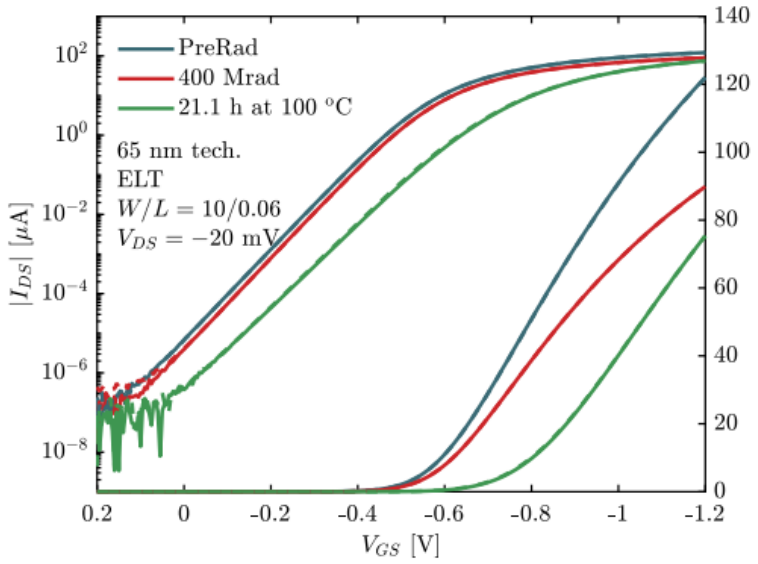


Figure 3.15: The $|I_d|$-$|V_{gs}|$ curves in linear regime at $|V_{gs}| = 20$ mV for a short channel ELT pMOS transistor. The transistor was irradiated with X-rays up to 400 Mrad(SiO_2) and then annealed at 100 °C for 21 h. Measurements were carried out in nominal mode (solid lines) with $V_{ds} = -20$ mV and reversed mode (dashed lines) with $V_{ds} = 20$ mV at room temperature, where the drain terminal is switch with the source terminal. (From [30])

The increase of the series resistance R_{sd} during irradiation is shown in Figure 3.16, which reports the R_{sd} normalized by the channel width as a function of cumulated doses in nMOS and pMOS transistors irradiated at two different temperatures. Channel with of all transistors was 20µm ,sufficient large to avoid RINCE. Consistently with larger degradation of the drain current in pMOSFETs

in linear regime, pMOS shows a larger increase of R_{sd} than nMOS device. The measurements demonstrate that the increase of R_{sd} is insensitive to the channel length. However, the effects of R_{sd} are more visible in short channel transistors, which are characterized by larger voltage drops due to the their higher drain current compared to long channel devices. The increase of R_{sd} in pMOS transistor is caused by the positive charge buildup in the spacers during irradiation. High density of positive charge in spacer oxides can reduce the number of majority carriers in the underlaying lightly p-doped regions of the LDDs. While this effect does not affect nMOSFETs, as positive charge in the spacer oxides contributes to increase the number of carriers in the n-doped LDDs [71, 101, 102].

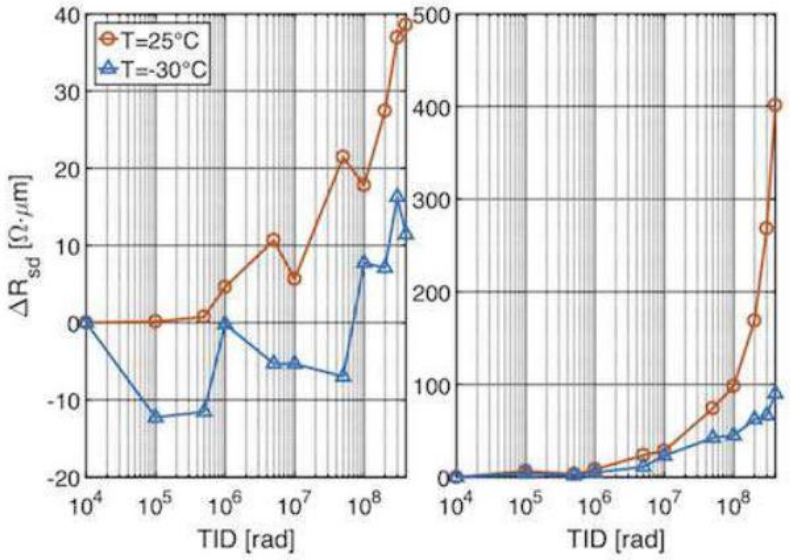


Figure 3.16: The series resistance R_{sd} normalized by the channel width as a function of cumulated doses in nMOS (left) and pMOS (right) transistors irradiated at two different temperatures. Transistors were irradiated with X-rays up to 400 Mrad(SiO_2). (From [102])

In addition, annealing measurements performed at high temperature display an enhanced positive shift of the threshold voltage in the short channel pMOS transistor. Figure 3.17 shows the I_d-V_{gs} characteristics in saturation regime ($|V_{ds}| = 1.2$ V) of the shortest pMOS device before exposure, after irradiation, and at the end of 25 hours annealing at 100 °C. Measurements were carried out in nominal mode (solid lines) with $V_{ds} = -20$ mV and reversed mode (dashed lines) with $V_{ds} = 20$ mV. The DC static characteristics are strongly asymmetric with the larger threshold voltage shift in nominal mode than in reversed mode. This asymmetry is noticeable only in the saturation region, whereas, in the linear region, the nominal and reversed DC responses overlap each other (see Figure 3.15). Both radiation-induced threshold voltage shift and asymmetry are active only at high temperature and only when the shortest device is annealed in the "diode" bias condition ($|V_{gs}| = |V_{ds}| = 1.2$ V), that means when a lateral source-to-drain field is applied during the annealing [71, 102].

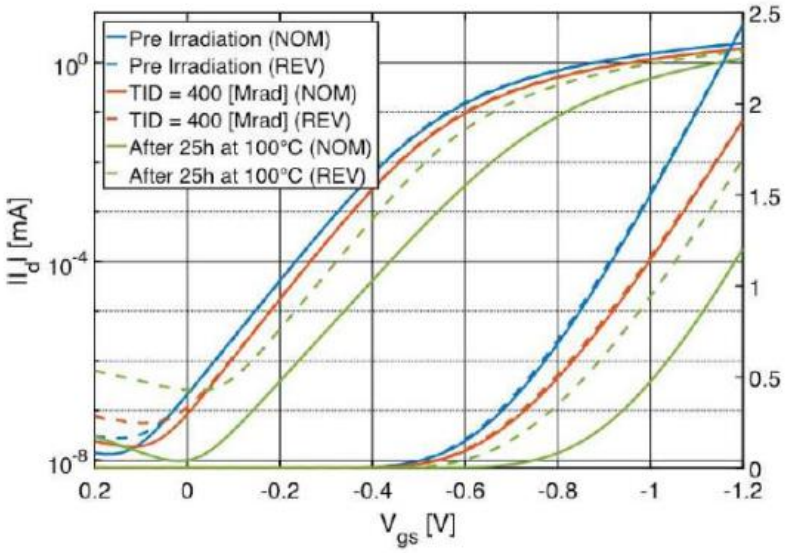


Figure 3.17: The $|I_d|$-$|V_{gs}|$ curves in linear regime at $|V_{gs}| = 20$ mV for a short channel ELT pMOS transistor. The transistor was irradiated with X-rays up to 400 Mrad(SiO_2) and then annealed at 100 °C for 21 h. Measurements were carried out in nominal mode (solid lines) with $V_{ds} = -20$ mV and reversed mode (dashed lines) with $V_{ds} = 20$ mV at room temperature, where the drain terminal is switch with the source terminal. (From [71] and [102])

In summary, devices affected by the RISCE are typically characterized by the following TID-induced effects [71]:

1) Irradiation causes an increase in the series resistance, substantially independent on applied bias and channel length.

2) The short channel devices display large threshold voltage shift, enhanced by high temperature and high electrical field in the gate oxide.

3) Asymmetric I_d-V_{gs} response is visible only in saturation region, when the device is irradiated and/or annealed with high electric field from drain to source.

Moreover, the RISCE has been explained with a model in some recent research work [101, 102]. The proposed model is represented in Figure 3.18, which explains the evolution of the spacer-related mechanisms through the following stage [71]:

(a) Ionizing radiation causes holes trapping and release of H^+ in the spacer oxides. Holes and H^+ can affect the density of majority carriers in the low-doped LDDs, consequently increasing the series resistance of the p-channel MOSFETs.

(b) High temperature can enhance the transport of the holes and H^+, and holes and H^+ are drifted from the space oxides to the gate oxides by the

applied gate bias.

(c) If the applied drain bias $|V_{ds}| \gg 0$, H^+ are drifted from one spacer into the gate oxide. H^+ de-passivates the Si-H bonds along the SiO_2/Si interface, creating a large density of interface traps at the source side (in pMOSFETs) and at the drain side (in nMOSFETs), which cause the asymmetric large threshold voltage shift.

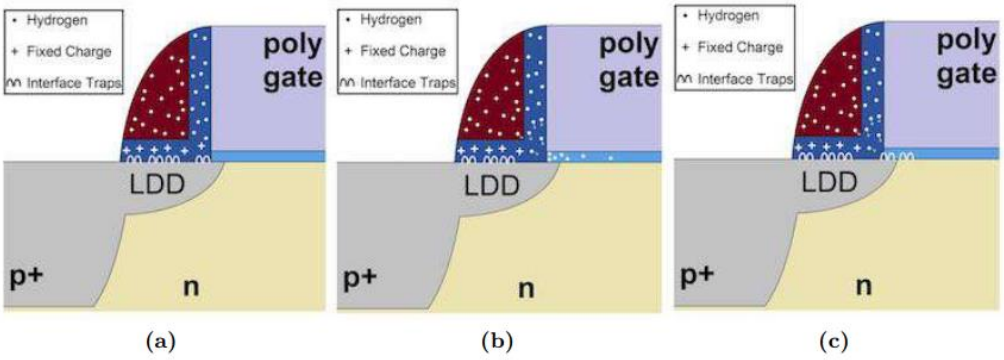


Figure 3.18: Schematic representation of the evolution of the spacer-related mechanisms. (a) Radiation-induced charge trapped in the spacers, increasing the series resistance in the LDD regions. (b) H^+ is drifted from the spacers in the thin gate oxide, the transport is strongly dependent on temperature and electric field. (c) H^+ reaches the interface, causing the formation of interface traps. (From [30])

This model has been supported by DC characteristics and low frequency $1/f$ noise measurements in [102] and fully validated by the charge pumping measurements and TCAD Sentaurus simulations in [105].

The strong asymmetric DC characteristics tested in saturation region of pMOS transistors can be understood through the drain induced barrier lowering (DIBL) with a peak density of interface traps localized close to the source region [71, 102]. DIBL is a short channel effect appearing as a modulation of the threshold voltage by the applied V_{ds}. We define:

$$V_{DIBL} = -\frac{V_{th}^{sat} - V_{th}^{lin}}{V_{sat} - V_{lin}}$$

where $V_{sat} = -1.2\,\text{V}$ and $V_{lin} = -20\,\text{mV}$, V_{th}^{sat} and V_{th}^{sat} have been extracted selecting an arbitrary drain current level in the weak-inversion range on the transistor and taking the respective V_{gs} values. Figure 3.19 shows the DIBL of three enclosed layout pMOS transistors with different channel length and identical channel width before exposure, after irradiation, and at the end of 21 hours annealing at 100 °C. Measurements were carried out in the nominal mode (NOM) and reversed mode (REV) at room temperature. The pre-irradiation value

of the DIBL is much higher in shorter transistors and practically identical in nominal and reversed mode. After 400 Mrad(SiO_2), the transistors are still symmetric with slight decrease of V_{DIBL}. However, after high temperature annealing for 21 hours, the short channel transistor becomes strongly asymmetric, with a large increase of V_{DIBL} in the reversed mode and a large decrease of V_{DIBL} in the nominal mode. This V_{DIBL} behavior also suggests that the interface traps are located at the source side.

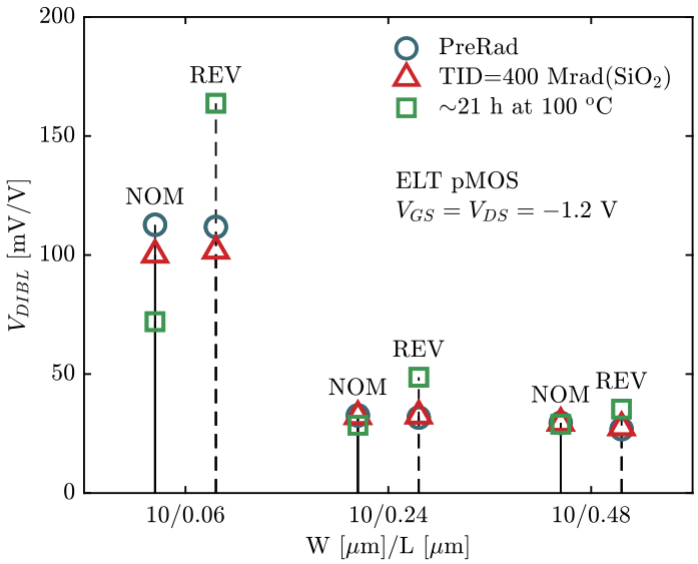


Figure 3.19: DIBL of three enclosed layout pMOS transistors with different channel length and identical channel width before exposure, after irradiation, and at the end of 21 hours annealing at 100 °C. Measurements were carried out in the nominal mode (NOM) and reversed mode (REV) at room temperature. (From [30])

Figure 3.20 schematically represents the surface potential φ_S of a pMOS transistor biased in version. (b) shows the surface potential after irradiation, while (c) and (d) exhibit the surface potential after high temperature annealing measured in the nominal mode and reversed mode, respectively. The solid lines indicate the φ_S in the linear region ($V_{ds} = 20$ mV), while dashed lines indicate the φ_S in the saturation region ($V_{ds} = -1.2$ V). At the end of the irradiation, the hydrogen ions are not yet drifted inside the gate oxide and thus no interface traps have been formed. As a result, φ_S is uniform along the channel, and the nominal V_{DIBL} is equal to reversed V_{DIBL}. As the temperature rises, the transport of hydrogen ions is accelerated. If the applied drain bias $V_{ds} \ll 0$, hydrogen ions trend to be drifted towards the gate oxide from the source spacer, with the generation of the interface traps with a peak density close to the source region. A larger gate voltage is now necessary to invert the channel region close to the source due to the positive trapped charge close to the source side, although the channel region close to the drain side is already in strong inversion. In this case, the threshold voltage is larger than before annealing, as described by the potential bump in Figure 3.20(c), the

high bias of the drain terminal has a slight effect on the maximum value of φ_S, resulting in a smaller V_{DIBL}. However, when the transistor is measured in reversed mode (d), the surface potential at the source side is reduced and the maximum φ_S is determined by the barrier close to the drain side, resulting in an increase of the V_{DIBL}. Moreover, from the data in Figure 3.20, it can be seen that the asymmetric effect occurs only in the saturated region, while in the linear region, the transistor remains symmetric [30, 71, 102].

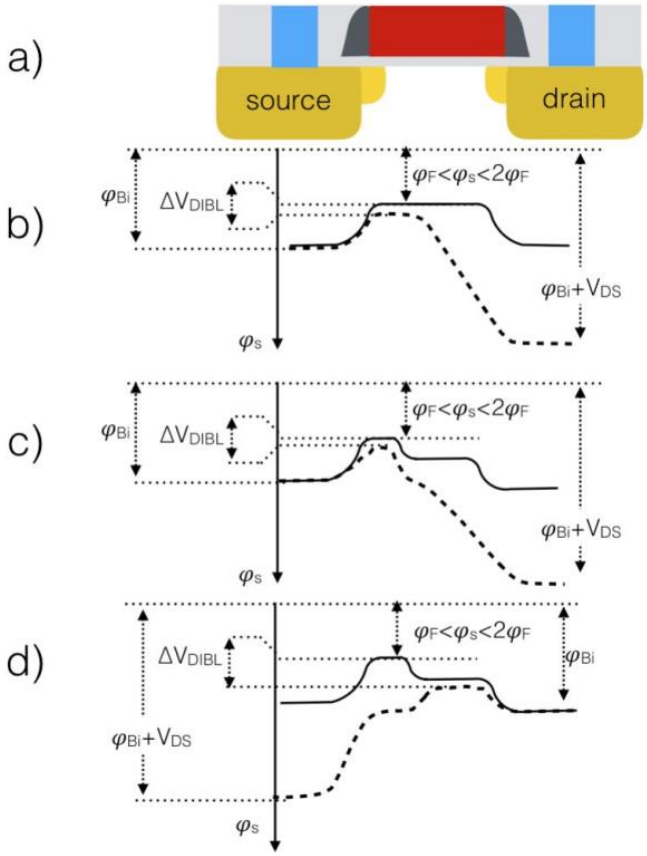


Figure 3.20: Schematic representation of the potential barrier in the nominal mode and reversed mode in an irradiated pMOS transistor, before and after the high temperature annealing. (From [102])

In the long discussion above, the research results of radiation-induced spacer-related effects have been mainly presented in pMOS transistors. The main reason for this choice is that although the phenomena present in pMOS devices are the same as in nMOS devices, nMOSFETs are complicated by the following two factors:

1) The charge trapped in oxide and interface are different in sign.
2) The transport of hydrogen ions and the consequent generation of the interface traps appears to happen already at room temperature.

Although the proposed mechanisms for describing the radiation-induced short channel effects can be applied to all the 65 nm and 130 nm technologies studied [30, 71, 101, 102, 105], this is no longer the case when moving to the 28 nm CMOS technology.

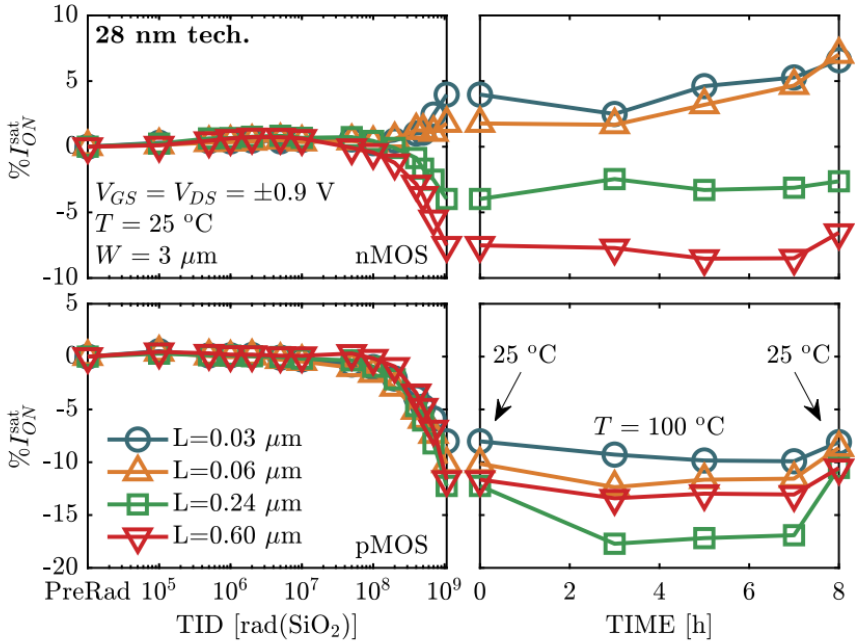


Figure 3.21: Degradation of the maximum drain current in linear regime ($|V_{ds}| = 20$ mV) for nMOS (top row) and pMOS (bottom row) devices in 28 nm CMOS technology designed with four different channel length and an identical channel width of 3 μm. Transistors are irradiated with X-rays up to 1 Grad(SiO_2) (left column) and then annealed at 100 °C for 4 h (right column). All the measurements during the annealing test were carried out at 100 °C, except the first and the last points, which were measured at room temperature (25 °C). (From [30])

Figure 3.21 shows the degradation of the maximum drain current for nMOS (top row) and pMOS (bottom row) transistors in 28 nm CMOS technology with four different channel length and an identical channel width of 3 μm. Transistors are irradiated up to 1 Grad(SiO_2) (left column) and then annealed at 100 °C for 4 hours (right column). The radiation response of this technology has a completely different channel length dependence compared to 65 nm, with the longest transistors showing the greatest degradation in both n and pMOS transistors. In fact, very similar results have also been obtained in a 28 nm CMOS technology from the same manufacturer but with a different process [112, 118-123]. Therefore, it can be said that in 28 nm CMOS technology the radiation-induced spacer-related effects is no longer of concern. In spite of this, a new TID effect related to the halo implantations appears in 28 nm CMOS technology, which will be discussed in the following subsection.

3.4 Halo-Related Effects

The continued scaling down of CMOS technology nodes has led to new limitations and problems to the performance of the modern advanced CMOS transistors. As the feature size scales, when the effective channel length is comparable to the source / drain junction depletion width, the potential distribution along the channel depends on both normal and lateral electric fields in the device [124]. Experimentally, the short-channel effect is observed to increase the leakage currents, degrade the subthreshold characteristics, and reduce the threshold voltage with decreasing effective channel length and increasing drain voltage. When the effective channel length of the MOS transistor is further reduced, the drain current finally cannot be turned off and the gate has no control over the charge. The so-called punch-through effect poses a severe problem for miniaturized devices. In order to suppress this effect, modern advanced CMOS technologies employ the halo implantations [125], which are used to prevent the expansion of the drain depletion region into the lightly doped transistor channel when the device is switched on [126, 127].

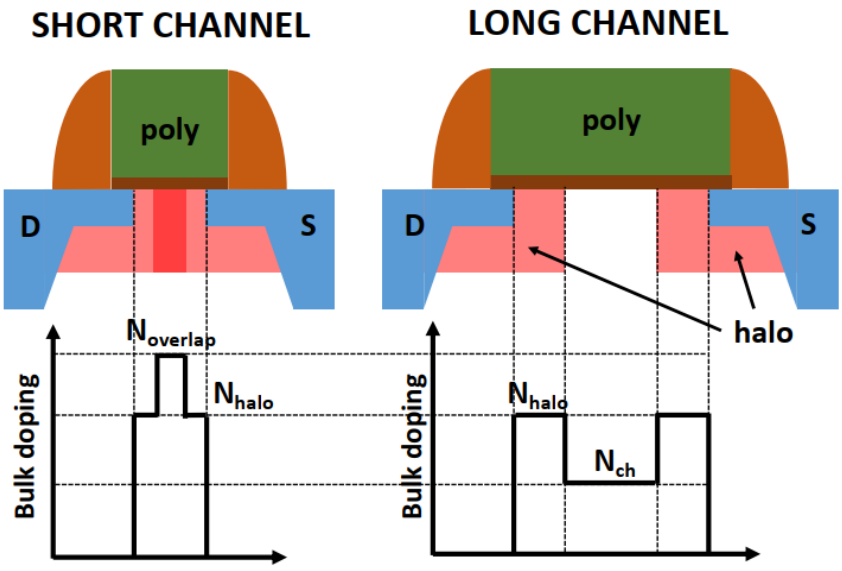


Figure 3.22: 28 nm CMOS technology structure with non-uniform doping distribution of the bulk due to the halo implantations (pink color) close to drain and source regions. In short channel transistors, halos can overlap to each other, while in long channel devices, halos are separated. (From [122])

The halo implant (also known as punch-through suppression or pocket implant) is a high-angle implant usually introduced in the same lithography step used to dope the source/drain extension regions, which is after polysilicon gate patterning but before nitride spacer formation. Halo implants need to be

performed with four 90° rotations of the wafer to ensure both sides of the differently orientated transistors are doped. The halo implant uses the same types of dopants used in the punch-through-stop implants. It creates a non-uniform channel doping profile around the source and drain extensions. By introducing halo implants, the dose need for punch-through-stop implants can be reduced, which helps to enhance carrier mobility in the channel region due to the reduction of the density of carrier scattering centers (dopants) [128].

Figure 3.22 schematically represented the 28 nm CMOS technology structure. The bulk doping along the channel is not uniform due to the halo implantations (pink color) close to drain and source region and the doping profile depends on the channel length. In long channel transistors, halos are separated. While in short channel devices, halos can overlap to each other, causing an increase in the overall channel doping [129]. Indeed, in the shortest channel transistors, the overlap of halos can lead to a doping peak in the channel center, which increases abruptly the threshold voltage [130]. The increase of the threshold voltage with decreasing channel length is named Revers short channel effect (RSCE) [131], and characterized scaled CMOS technologies with high halo doping concentration.

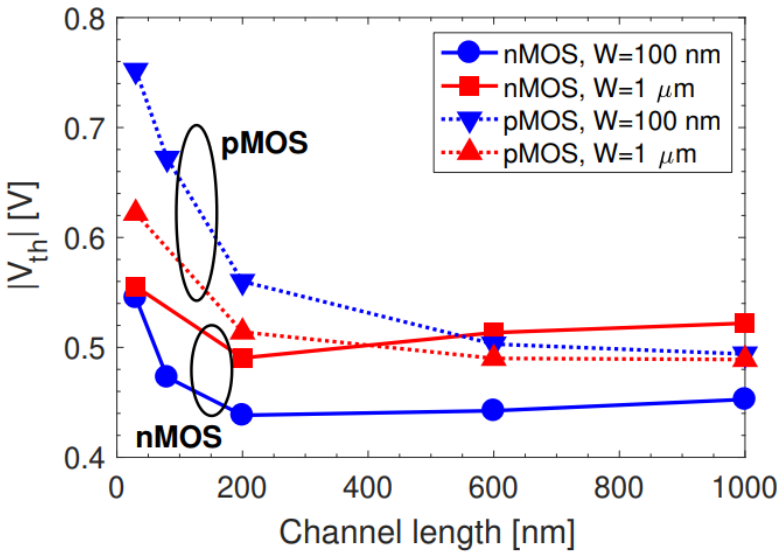


Figure 3.23: The initial threshold voltage $|V_{th}|$ of nMOS (solid lines) and pMOS (dotted lines) transistors with different channel dimensions. Measurements are carried out at room temperature in linear region ($|V_{th}| = 0.1$ V). (From [122])

Figure 3.23 shows the initial threshold voltage $|V_{th}|$ of nMOSFETs and pMOSFETs before irradiation. The $|V_{th}|$ is plotted as a function of the channel length for devices with channel width $W = 100$ nm and 3µm. The trend of the $|V_{th}| - L$ is characterized by a distinct RSCE, indicating the highly doped halo implantations and the low substrate concentration, which cause the increase of

the V_{th} in short channel transistors. The abrupt increase of the $|V_{th}|$ for $L < 100$ nm suggests that halos close to drain and source region begins to overlap to each other when L is reduced below 100 nm. The RSCE is particularly evident in the pMOS transistors with W = 100 nm, where the $|V_{th}|$ difference between the longest and the shortest channel devices is about 0.25 V, while in nMOSFETs with W = 100 nm, this $|V_{th}|$ difference is about 0.1 V. The dependence of the threshold voltage with the channel width is caused by the gate fringing field in the channel corner edge with the STI. Depending on the transistor type, fabrication process and STI design different effects can arise: the Narrow Width Effect (NWE) and the Reverse Narrow-Width Effect (RNWE) [132].

The TID effects related to the halo implantations have been reported recently by few works [71,122, 123], and the research on its degradation mechanisms started to be investigated in the last few years, as its impact is evident only at very high doses, much higher than that of interest for the space application. The halo-related TID effects has been researched mainly in the 28 nm CMOS technology [71, 122, 123].

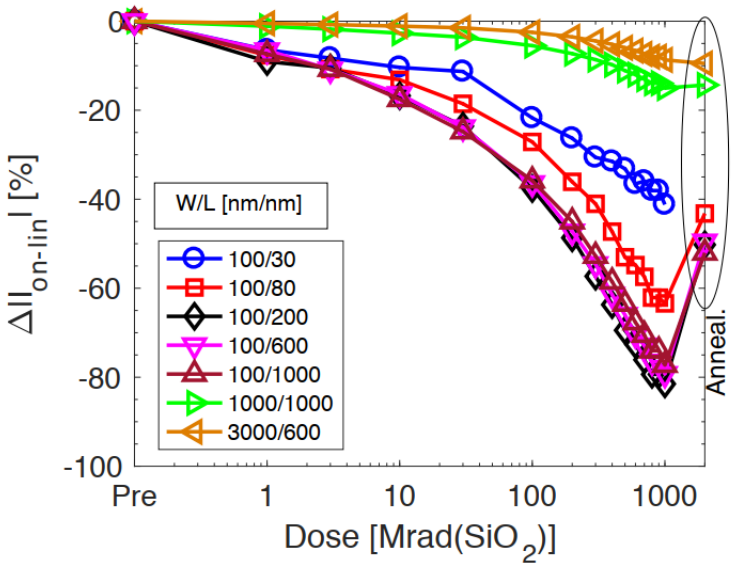


Figure 3.24: Degradation of the maximum drain current as a function of cumulate doses in 28 nm pMOSFETs with different channel dimensions irradiated up to 1 Grad(SiO_2) and then annealed at 100 °C for 24 hours. All measurements were carried out in linear region ($|V_{ds}| = 0.1$ V) and at room temperature. (From [122])

The first clue of a possible impact of halo implantations on the TID response reported in Figure 3.24 was the discovery of a channel length dependence in the degradation of the drain current of irradiated transistors [122]. The plot shows the degradation of maximum drain current as a function of cumulated dose in 28 nm pMOS transistors with different channel dimensions irradiated up to 1 Grad(SiO_2) and annealed at 100 °C for 24 hours. Narrow and long transistors with $L \geq 200$

nm degrade almost equally, $\Delta|I_{on\text{-}lin}|$ is about -80% after 1 Grad(SiO_2). However, narrow and short transistors with $L < 100$ nm exhibit the channel length dependence, with the shortest transistor ($L = 30$ nm) having the smallest degradation. Focusing on this channel length dependence of narrow transistors, after 1 Grad(SiO_2), pMOSFETs with $L = 30$ nm, 80 nm and 100 nm exhibit respectively $\Delta|I_{on\text{-}lin}|$ degradation of -40%, -65% and -85% [122]. This phenomenon is visible at high doses (10 Mrad(SiO_2)), and is dominant at ultra-high doses ($>$ 100 Mrad(SiO2)). This channel length dependent effect is shown more clearly in the figure below.

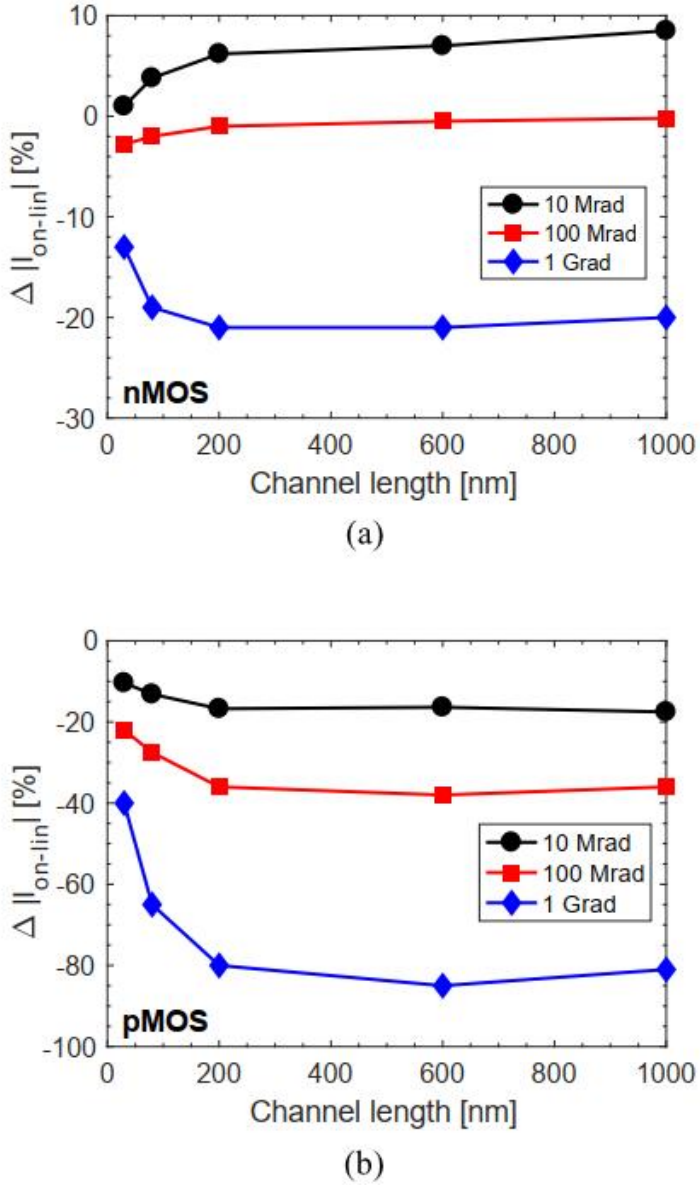


Figure 3.25: Degradation of the maximum drain current as a function of channel length in 28 nm nMOSFETs (a) and pMOSFETs (b) irradiated with X-rays up to 1 Grad(SiO_2). Transistors have narrow channel with $W = 100$ nm. The I_{on-lin} current is defined as the drain current when $|V_{gs}| = 1$ V and $|V_{ds}| = 0.1$ V. (From [123])

Figure 3.25 shows the degradation of maximum drain current as a function of cumulated dose in 28 nm nMOS and pMOS transistors with narrow channel $W = 100$ nm irradiated with X-rays up to 1 Grad(SiO_2).

In nMOS transistors irradiated up to 10 Mrad(SiO_2), $\Delta|I_{on\text{-}lin}|$ is channel length dependent. The worst-case is found in the longest device, with $\Delta|I_{on\text{-}lin}| = 9\%$, while the degradation of the shortest device is negligible, $< 1\%$. At 100 Mrad(SiO_2), $\Delta|I_{on\text{-}lin}|$ of the nMOSFETs decreases by less than 2%, regardless of channel length. Above 100 Mrad(SiO_2), the degradation of the $\Delta|I_{on\text{-}lin}|$ is negative and shows a clear channel length dependence. The shortest transistor exhibits the most tolerant TID response, with $\Delta|I_{on\text{-}lin}| = -12\%$, vs. $\Delta|I_{on\text{-}lin}| = -20\%$ of the longest channel device.

In pMOS transistors, $\Delta|I_{on\text{-}lin}|$ is always negative and channel length dependent, which increases with increasing dose. Short channel pMOSFETs exhibit higher TID tolerance than longer channel devices. At 1 Grad(SiO_2), the $\Delta|I_{on\text{-}lin}|$ of the shortest transistor degrades about -40%, while the longest channel device degrades about -80%. However, p-channel transistors with $L > 200$ nm do not show any channel-length dependence, showing a constant degradation around -80%. This short-channel effect is visible only in narrow channel transistors at both very high doses (10 Mrad(SiO_2)) and ultra-high doses (> 100 rad(SiO_2)). These effects are related to the influence of halo implantations, as explained in the next pages.

One possible explanation of the decreased sensitivity at short channel length is the influence of the halo implantations used in modern CMOS processes [133]. Large implant doses and energies in the halo regions can induce a positive $|V_{th}|$ shift, known as V_{th} roll-off [134]. This effect is evident in short channel transistors, where the halo implantations can slightly overlap each other, increasing the average doping of the channel region. By analyzing the pre-rad $|V_{th}|$ of 28 nm pMOSFETs (Figure 3.23), the V_{th} roll-off is visible, and it increases abruptly on the MOSFETs with $L < 100$ nm, indicating that in these transistors the halo implantations increase the overall channel doping [71].

In recent studies based on device simulation [135, 136], it was demonstrated that the doping of the bulk regions close to the STI edge can drastically modify the TID tolerance of nMOS transistors. In nMOSFETs the positive trapped charges in the STI invert the lateral edges of the transistor channel, forming a parasitic n-channel FET [100]. An increase of the bulk doping in the regions close to the STI edge can lead to an improvement of the TID response of nMOSFETs, as the electrical field generated by the trapped charge in the STI is not able to invert the lateral channel regions. As a consequence, in the short channel nMOSFETs with overlapping halo implantations and high channel doping, the off-state leakage current and the V_{th} degradation decreases [71].

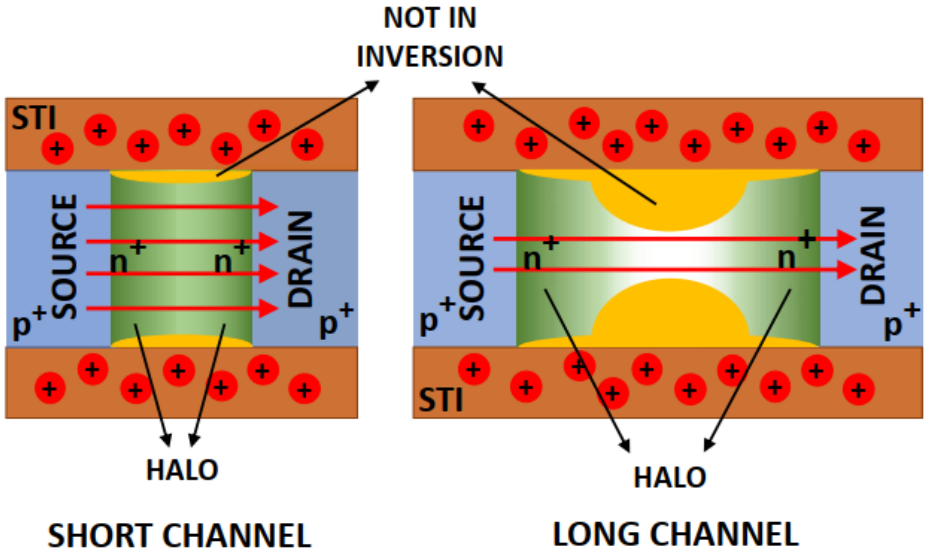


Figure 3.26: Schematic view of the influence of the halo regions on the TID response of short and long channel pMOSFETs. (From [122])

In pMOSFETs the increase of the bulk doping in the regions close the STI edge can reduce the depleted lateral region responsible for RINCE. Consequently, the width reduction of the irradiated transistor is limited, leading to an increase of the TID tolerance of the pMOSFETs. Figure 3.26 shows a schematic top view of narrow pMOSFETs in the channel region. The green regions represent the STI oxides, filled by the buildup of positive trapped charges. The color gradient in the yellow regions denotes the halo implantations, which almost overlap in the short-channel transistors. The dark-blue areas are the regions which do not reach strong inversion due to the influence of the STI trapped charges and are responsible of the reduction of the effective transistor width.

The halo-related effects on the radiation response of MOS transistors have only been studied recently. Further research on the influence of halo implantations in FinFET technology will be given in the fourth chapter through the discussion of new experimental results, which were obtained during this thesis work and have been recently published in [137, 138].

Chapter 4

TID Degradation Mechanisms in 16 nm Bulk FinFETs

This chapter investigates the total ionizing dose (TID) degradation mechanisms of 16 nm bulk Si FinFETs at ultra-high doses. nFinFETs and pFinFETs with several channel lengths are irradiated up to 1 Grad(SiO_2) and then annealed for 24 h at 100 °C. Irradiated devices show significant degradation in the maximum drain currents, transconductance and off-state leakage currents with slight subthreshold stretch-out and negligible threshold voltage shifts. At doses up to 10 Mrad(SiO_2), the TID response is dominated by the positive trapped charge in the shallow trench isolation (STI). At ultra-high doses approaching 1 Grad(SiO_2), the DC static and low-frequency *1/f* noise measurements suggest the generation of trapped charge at the STI/Si interface and/or at the corner between the STI and the gate dielectric. The TID sensitivity depends on the bias condition and channel length. Halo implantations fortuitously increase the radiation tolerance of short-channel FinFETs due to the increased channel doping caused by the overlap of source and drain halos. The worst degradation is found when a high electric field is applied to the gate during irradiation.

Future high energy physics experiments will require chips able to withstand ultra-high ionizing doses. A CMOS Si-based 16 nm FinFET commercial technology is a promising candidate for the upgrade of the electronics in the tracker detectors of a toroidal LHC apparatus (ATLAS) and compact muon solenoid (CMS) experiments. The use of an advanced FinFET-based technology will improve the performances of the tracker readout electronics with high granularity and bandwidth [42, 43].

At the state-of-the-art, the TID effects at ultra-high doses has been explored only in planar technologies. Studies at 1 Grad(SiO_2) on 65 nm MOSFETs [101-103, 139] and on 28 nm MOSFETs [113, 121-123] have revealed two main dominating TID mechanisms. The first phenomenon, called radiation-induced narrow-channel effect (RINCE) [101], was related to charge buildup in shallow

trench isolation (STI) oxide and its interfaces. STI trapped charge increases the off-state leakage current in n-channel MOSFETs and induces parametric drifts in narrow n and p-channel MOSFETs [101, 103, 139]. The second effect, called radiation-induced short-channel effect (RISCE) [99, 101], was related to charge buildup in the spacer oxides and the overlying silicon nitride layers above the lightly doped drain (LDD) extensions [101, 102]. RISCE degrades short channel devices by increasing the parasitic series resistance and by reducing the drive current [101, 102]. In addition, sub-micron technology nodes employ halo implantations to reduce the undesired effect of drain-induced barrier lowering in short transistors [140, 141]. Recent works [122, 123] have reported that halo implantations of planar MOSFET devices fortuitously improve the TID tolerance of the short-channel devices, as a consequence of the increased bulk doping caused by overlapping halos [107, 122, 123].

TID effects in bulk FinFET technologies have been investigated at doses much lower than 1 Grad(SiO_2) (< 2 Mrad(SiO_2)) [142]-[147]. Recent works have shown that the TID response of Si-based FinFETs irradiated up to about 1 Mrad(SiO_2) were dominated by charge buildup in the shallow trench isolation (STI) [143, 144]. While III-V-based FinFETs have shown large densities of radiation-induced defects in the gate dielectrics [145]. However, the TID response of Si-based FinFETs at ultra-high doses is still unknown.

In this chapter, the TID degradation mechanisms in 16 nm bulk Si FinFET technology are explored at ultra-high doses, up to 1 Grad(SiO_2), by performing DC static and low-frequency *1/f* noise measurements. FinFETs irradiated and annealed under different bias conditions show TID degradations dependent on the channel length and bias conditions. In addition, for the first time, evidence of the influence of halo implantations is reported in FinFET devices with better TID tolerance in the short-channel transistors.

The work presented in this chapter has been carried out within the FinFET16v2 experiment funded by the National Institute for Nuclear Physics - INFN, in a collaboration with: University of Bergamo, Bergamo, Italy; University of Milano Bicocca, Milano, Italy; and École polytechnique fédérale de Lausanne, Lausanne, Switzerland.

Most of the results and figures presented in this chapter have been published and/or submitted in the following peer-reviewed publications:

- [137] T. Ma, S. Bonaldo, S. Mattiazzo, A. Baschirotto, C. Enz, A. paccagnella and S. Gerardin, "TID degradation mechanisms in 16 nm bulk FinFETs irradiated to ultra-high doses". *IEEE Transactions on Nuclear Science*, vol. 68, no. 8, pp. 1571-1578, Aug. 2021.
- [138] S. Bonaldo, T. Ma, S. Mattiazzo, A. Baschirotto, C. Enz, A. paccagnella and S. Gerardin, "TID degradation and low-frequency noise in 16 nm bulk FinFETs irradiated to ultra-high doses," *IEEE*

Transactions on Nuclear Science. (Accepted for RADECS 2021 conference, Austria, Vienna, and currently submitted for publication in IEEE Transactions on Nuclear Science.)

Moreover, the results in this chapter have been presented at the following international conference:

- Radiation Effects on Components and Systems - RADECS 2020, online event, 19th October - 20th November 2020, oral presentation about "TID degradation mechanisms in 16 nm bulk FinFETs irradiated to ultra-high doses". (I was the presentation author)
- Radiation Effects on Components and Systems - RADECS 2021, online event, 13th - 17th September 2021, oral presentation about "TID degradation and low-frequency noise in 16 nm bulk FinFETs irradiated to ultra-high doses".

4.1 Devices and Experiments

4.1.1 Devices Description

The FinFETs under test were fabricated in a commercial 16 nm bulk Si CMOS technology using high-*k* gate dielectric and most likely halo implantations [141, 148]. The devices are intended for core applications with standard threshold voltage and nominal operating voltage of 0.85 V. Figure 4.1 shows a 3D schematic view of the bulk FinFETs with two fins, while a digital picture of a die containing the array of transistors is shown in Figure 4.2. The devices were provided in an array structure of nFinFETs and pFinFETs with channel lengths ranging from 16 to 240 nm and 2 fins. All the transistors have the same fin width and fin height (i.e. same effective channel width).

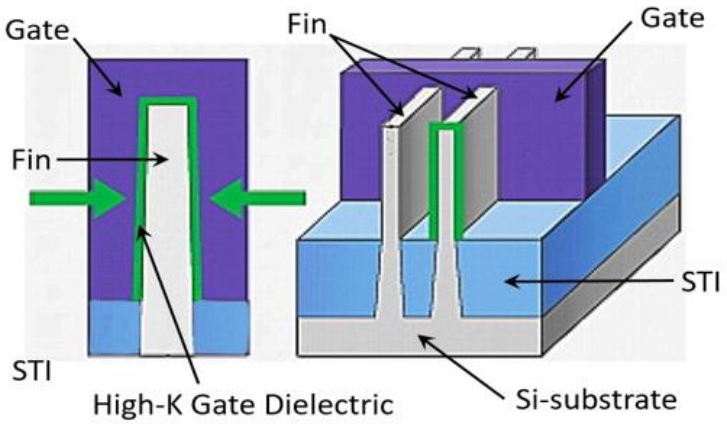


Figure 4.1: 3D Schematic view of the bulk FinFETs with 2 fins. (From [137])

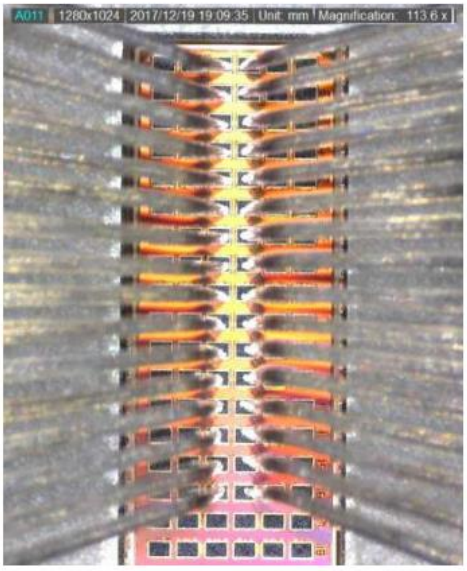


Figure 4.2: Digital photo at 113x magnification of the probe card tips over the pads of transistors in the array structure.

The transistors of the same channel type shared source and bulk contacts with separated drain and gate contacts. The gate terminals were protected by electro-static discharge (ESD) protections designed in a two-diodes configuration. A customized probe-card allowed twelve different transistors to be biased and measured at the same time.

4.1.2 Irradiation Conditions and Measurements Details

The irradiation was conducted at room temperature using 10 keV X-rays produced by a Seifert Model RP 149 X-ray irradiator at the University of Padova, Italy. The dose rate was checked, before irradiation, by a calibrated diode [149]. For this irradiation campaign the dose rate was set at 4.7 Mrad(SiO_2) / h (corresponding to 8.5 Mrad(Si)/h) for a total exposure time of about 9 days to reach 1 Grad(SiO_2). Exposures at lower dose rates may enhance the TID degradation of the transistor performances, as shown in previous MOSFET technologies [139]. All ionizing doses and dose rate are referred to equilibrium doses in SiO_2 for consistency in calibration and to facilitate comparison with other work [19].

Figure 4.3 shows the irradiation setup with probe card station, X-ray tube and instruments used during the evaluation of the 16 nm bulk FinFETs. The radiation exposure was stopped at several steps, and each device was immediately measured once per step interval using a switching matrix. During these intervals, devices that were not actively being measured were left in the “off” condition. After the exposure, devices were annealed at 100 °C for about 24 hours. During the X-rays irradiation and the annealing, all transistors of the array structure were

measured with three different bias conditions: "off" condition ($|V_{gs}| = 0$ V and $|V_{ds}| = 0$ V), "on" condition ($|V_{gs}| = 0.9$ V and $|V_{ds}| = 0$ V), and "diode" condition ($|V_{gs}| = 0.9$ V and $|V_{ds}| = 0.9$ V).

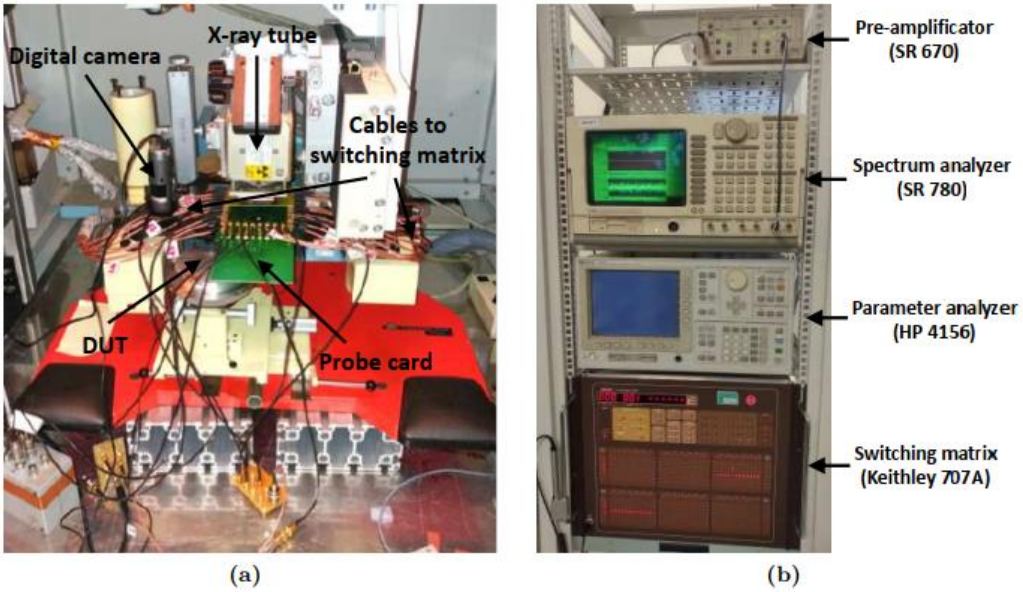


Figure 4.3: Experimental setup for the evaluation of the TID response of the 16 nm bulk FinFETs. (a) Probe card station inside the X-ray facility. (b) Instruments used for the measurements of the DC static characteristics and the low frequency *1/f* noise.

The DC static responses of the transistors were measured at room temperature in the linear regime ($|V_{ds}| = 50$ mV) before exposure, after irradiation and after high-temperature annealing with a semiconductor parameter analyzer (HP4156). Low frequency 1/f noise measurements were carried out at room temperature by the use of a pre-amplifier (SR 570) and a spectrum analyzer (SR 780). The low frequency noise [150] was tested in a frequency span between 0.5 Hz and 1 kHz at $|V_{ds}| = 50$ mV and at several values of $V_{gt} = V_{gs} - V_{th}$. Measurements were performed on more than 100 devices. Under all experimental conditions, at least three devices of each type and size have been evaluated.

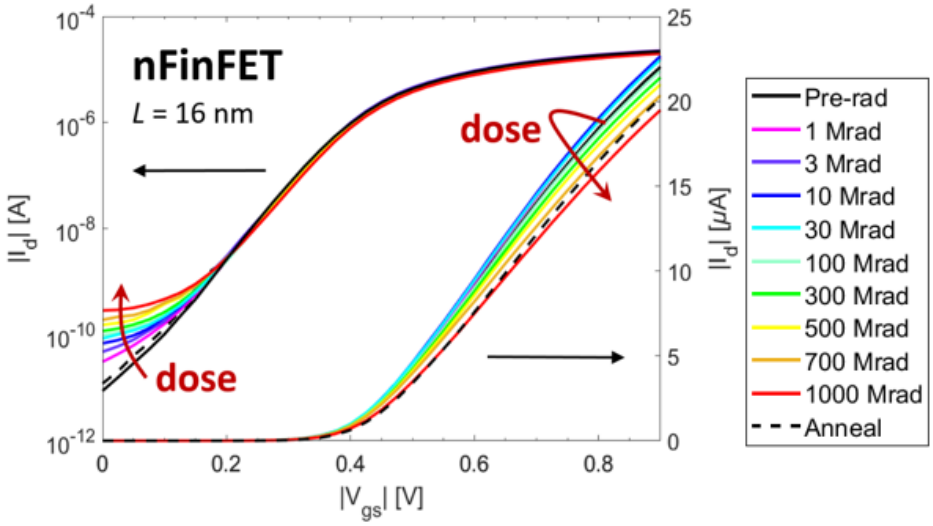
4.2 Experimental Results

In the following section, the TID responses of FinFETs are reported by measuring the DC static characteristics and extracting the main parameters: maximum drain current variation ($\Delta I_{on\text{-}lin}$), threshold voltage shift (ΔV_{th}), degradation of the transconductance (Δg_m) and subthreshold swing variation (ΔSS). The $I_{on\text{-}lin}$ current is defined as the drain-to-source current in linear region ($|V_{ds}| = 50$ mV) when the channel is in strong inversion at $|V_{gs}| = 0.9$ V. The threshold voltage V_{th} is extracted by the linear region (ELR) method [151], as the

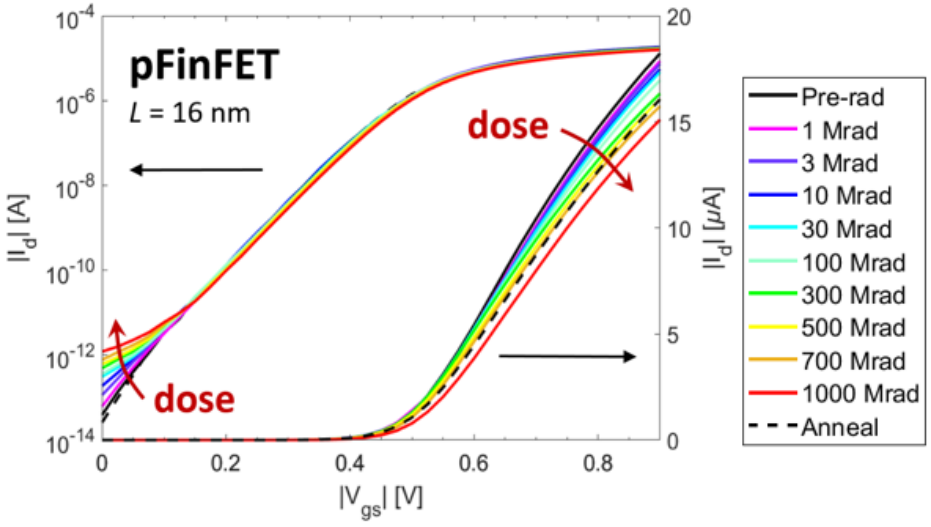
gate voltage axis intercept of the linear extrapolation of the I_d-V_{gs} characteristics at its maximum first derivative point. Nominally identical devices irradiated and annealed under the same conditions show DC static characteristics shifts that typically vary by less than $\pm$ 5%. Representative results are shown below.

4.2.1 DC Statics Response

Figure 4.4 plots the $|I_d|$-$|V_{gs}|$ curves at $|V_{ds}| = 50$ mV for (a) shortest nFinFET with $L = 16$ nm, (b) shortest pFinFET with $L = 16$ nm, (c) longest nFinFET with $L = 240$ nm, and (d) longest pFinFET with $L = 240$ nm. The DC responses are shown at several irradiation steps and after 24 hours of annealing at 100 °C with devices biased in "diode" condition.



(a)



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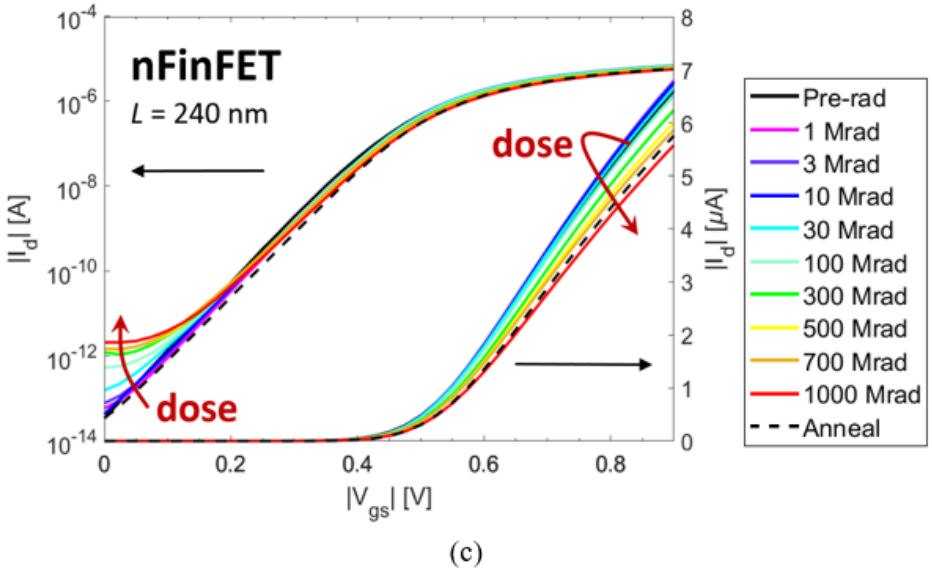
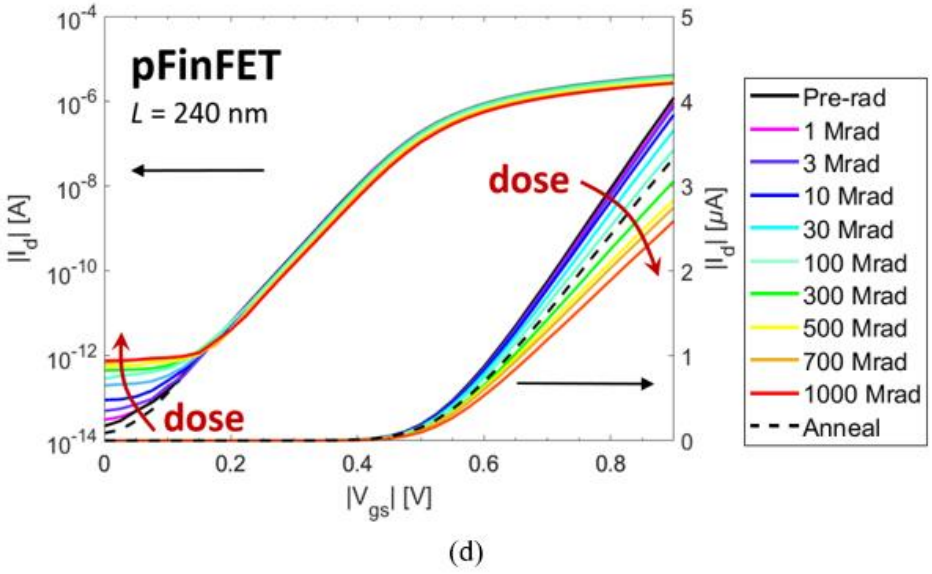


(c)



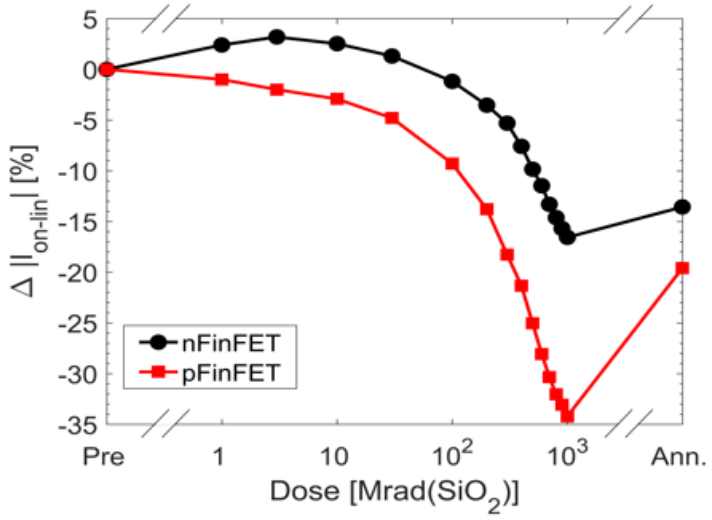
(d)

Figure 4.4: $|I_d|$-$|V_{gs}|$ curves in the linear region ($|V_{ds}| = 50$ mV) of FinFETs. Devices were irradiated up to 1 Grad(SiO_2) and then annealed for 24 h at 100 °C in the "diode"-bias condition. (a) Shortest nFinFETs with $L = 16$ nm, (b) shortest pFinFETs with $L = 16$ nm, (c) longest nFinFETs with $L = 240$ nm, and (d) longest pFinFETs with $L = 240$ nm. (From [137])

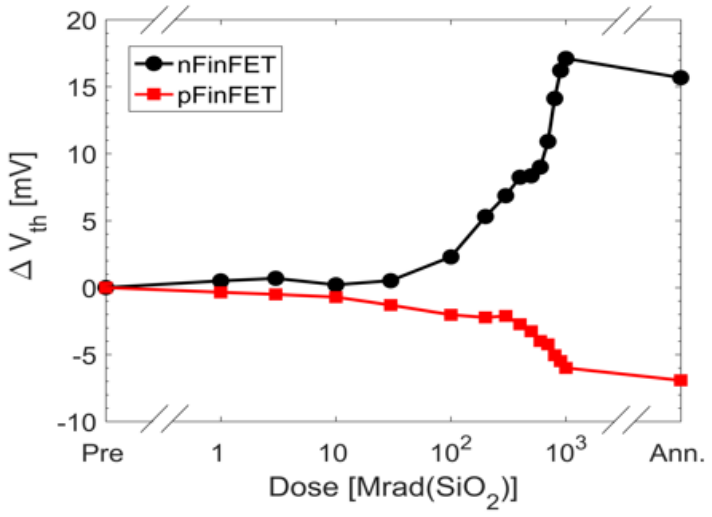
In general, nFinFETs show a better TID tolerance than pFinFETs, while the longest FinFETs exhibit worse TID degradation than the shortest devices. After 1 Grad(SiO_2), the $I_{on\text{-}lin}$, defined as the maximum drain current at $|V_{gs}| = 0.9$ V and $|V_{ds}| = 50$ mV, decreases by -19% for the shortest pFinFET vs. -35% for the longest pFinFET. Both nFinFETs and pFinFETs exhibit significant decreases in transconductance (g_m) with dose, but only slight threshold voltage (V_{th}) shifts and slight degradation of the subthreshold slope (SS). The off-state

leakage current ($I_{off\text{-}lin}$), defined as the drain current at $|V_{gs}| = 0$ V and $|V_{ds}| = 50$ mV, increases with the cumulated dose in nFinFETs and pFinFETs. It is worth noting that $I_{off\text{-}lin}$ increases by two order of magnitude in both n- and pFinFETs after the irradiation up to 1 Grad(SiO_2). However, the $I_{off\text{-}lin}$ degradation undergoes to an almost complete recovery during the high temperature annealing and may be a marginal issue for integrated circuit applications working at the ultra-high doses [103, 113].

nFinFETs are characterized by a rebound effect of the electrical response in terms of $I_{on\text{-}lin}$ [19] at 10 Mrad(SiO_2). Below 10 Mrad(SiO_2), the $I_{on\text{-}lin}$ increases with dose, while very slight V_{th} variation is observed. Above 10 Mrad(SiO_2), $I_{on\text{-}lin}$ decreases with dose, while V_{th} shifts to more positive values, with larger g_m degradation.



(a)



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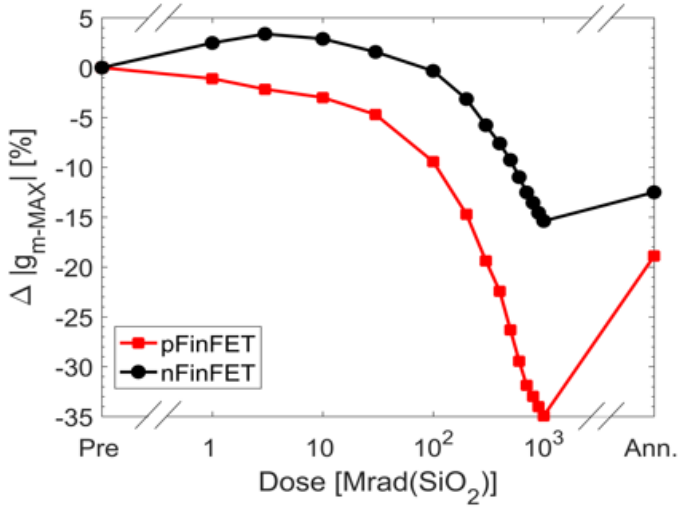
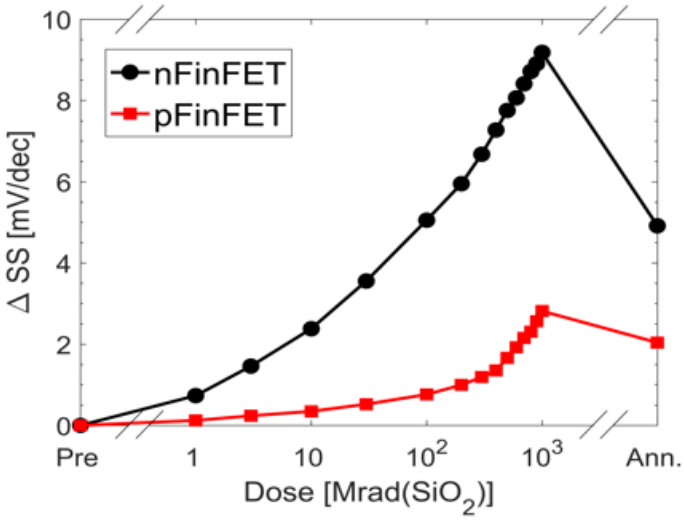


(c)



(d)

Figure 4.5: Degradation of (a) maximum drain current $\Delta|I_{on\text{-}lin}|$, (b) threshold voltage ΔV_{th}, (c) maximum transconductance $\Delta|g_{m\text{-}MAX}|$, and (d) subthreshold swing ΔSS as a function of dose for the longest channel devices ($L = 240$ nm) in nFinFETs and pFinFETs. Transistors were irradiated up to 1 Grad(SiO_2) and then annealed for 24 h at 100 °C in the "diode"-bias condition. Measurements are carried out at room temperature in the linear region ($|V_{ds}| = 50$ mV). (From [137])

After 24 hours annealing at high temperature (100 °C), pFinFETs show a substantial recovery of their DC response, suggesting neutralization of the TID-induced trapped charge. The longest pFinFET recovers from $\Delta|I_{on\text{-}lin}| = -35\%$ at 1 Grad(SiO_2) to -19% after annealing. While nFinFETs slightly recover during the annealing, showing a $\Delta|I_{on\text{-}lin}| = -16\%$ at 1 Grad(SiO_2) to -13% after annealing, for the longest one.

Figure 4.5 shows the radiation-induced degradation of the main DC parameters: (a) maximum drain current $\Delta|I_{on\text{-}lin}|$, (b) threshold voltage ΔV_{th}, (c) maximum transconductance $\Delta|g_{m\text{-}MAX}|$, and (d) subthreshold swing ΔSS. These values are for the longest channel devices ($L = 240$ nm), irradiated up to 1 Grad(SiO_2) and then annealed for 24 h at 100 °C in the "diode" condition.

pFinFETs show the worst-case degradation of $I_{on\text{-}lin}$ (35%), which is twice that of nFinFETs (16%) at 1 Grad(SiO_2). On the contrary, the variation of V_{th} is negligible in pFinFETs (< 7 mV) and slight in nFinFETs (< 17 mV), mostly caused by irradiation doses > 10 Mrad(SiO_2). The relatively small shifts in the V_{th} suggests a robust gate dielectric to TID effects. Interestingly, comparing Figure 3(a) and Figure 3(c), the degradation of $|g_{m\text{-}MAX}|$ is very similar to $\Delta|I_{on\text{-}lin}|$, indicating that the decrease of $|I_{on\text{-}lin}|$ is mostly dominated by the degradation of g_m. ΔSS increases slightly with dose, less than 10 mV/dec for nFinFETs and 3 mV/dec for pFinFETs after 1 Grad(SiO_2).

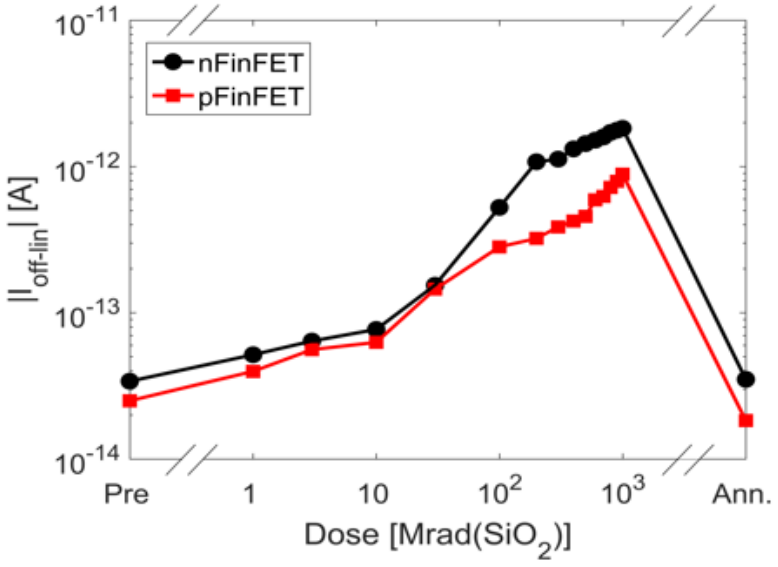


Figure 4.6: Increase of the leakage drain current $|I_{off\text{-}lin}|$ as a function of dose in nFinFETs and pFinFETs with $L = 240$ nm in linear regime ($|V_{ds}| = 50$ mV). Devices were irradiated and annealed for 24 h at 100 °C in the "diode" condition. (From [137])

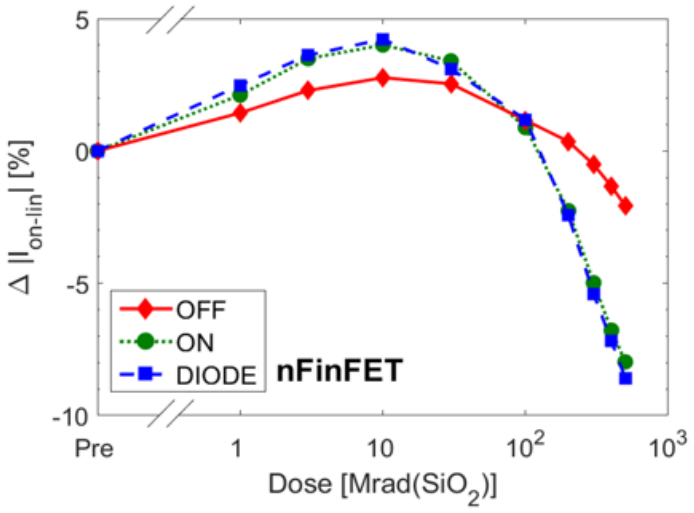
Figure 4.6 is related to Figure 4.4 and it evidences the increase of the off-state drain leakage current $|I_{off\text{-}lin}|$ for the longest n-channel and p-channel FinFETs ($L = 240$ nm). In nFinFETs, the drain leakage current increases with increasing doses, due to the activation of the parasitic transistor close to the STI sidewalls [101]. A similar trend is also shown in pFinFETs, the increase of the leakage current in pFinFETs, nearly two orders of magnitude at 1 Grad(SiO_2), is a little less than that in nFinFETs. The increase of the leakage current in pFinFETs is due most likely to interface trap buildup at the channel/dielectric interface and/or drain/body interface. At high doses, high density of interface traps can be

generated at the intersection of the depletion region and the STI sidewalls, inducing an increase of the peripheral drain to substrate junction leakage current [152, 153]. However, after the high temperature annealing, the degradation of the off-state drain currents in both n- and p-FinFETs almost completely recovered.

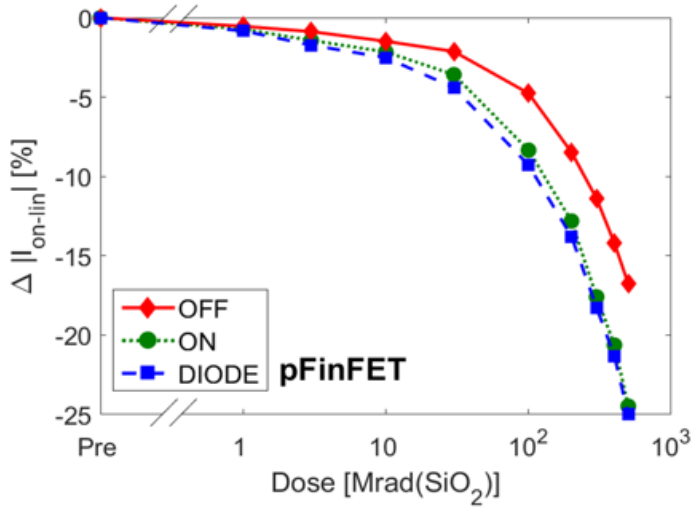
4.2.2 Influence of the Irradiation Bias Condition

Figure 4.7 evidences the influence of the TID sensitivity to the bias condition applied during the irradiation. The $\Delta|I_{on\text{-}lin}|$ is measured at several doses in FinFETs irradiated in the "off", "on" and "diode" conditions. The irradiations are carried out up to 500 Mrad(SiO_2), due to the long time required to reach 1 Grad(SiO_2). In both nFinFETs and pFinFETs, the TID responses of "diode"-biased devices overlap the ones of "on"-biased devices, indicating an insensitivity of the TID response to lateral drain-to-source electric fields. At 500 Mrad(SiO_2), nFinFETs biased in the "diode" conditions shows a $\Delta|I_{on\text{-}lin}|$ of -8.6% vs. -8% of "on"-biased devices, while pFinFETs show a $\Delta|I_{on\text{-}lin}|$ of -25% vs. -24.5%, respectively.

On the other side, the devices irradiated in the "off" condition show the highest TID tolerance. At 500 Mrad(SiO_2), "off"-biased nFinFETs show a $\Delta|I_{on\text{-}lin}|$ of -2% vs. -8.6% for devices irradiated in the "diode" condition, while pFinFETs show -16% vs. -25%, respectively. This highest tolerance of the "off"-bias condition is most probably related to the limited charge yield when low electric fields are applied during the irradiation [19],[154].



(a)

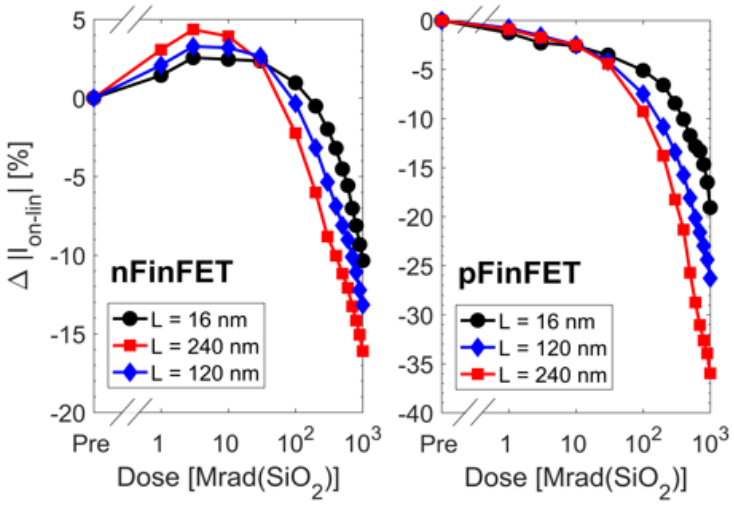


(b)

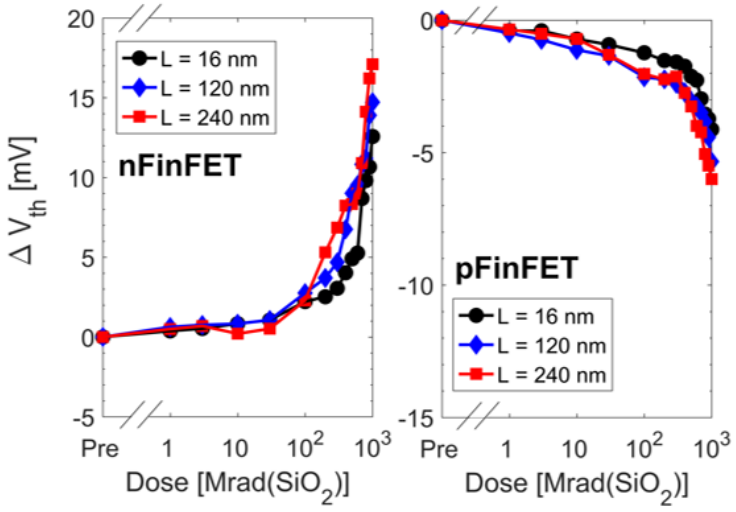
Figure 4.7: Degradation of maximum drain current $\Delta|I_{on\text{-}lin}|$ of FinFETs irradiated up to 500 Mrad(SiO_2) in different bias conditions: "off", "on", or "diode". Devices (a) nFinFETs and (b) pFinFETs have $L = 240$ nm, and are measured in the linear region ($|V_{ds}| = 50$ mV) at room temperature. (From [137])

4.2.3 Channel Length dependence

Figure 4.8 shows the TID degradation of (a) maximum drain current $|I_{on\text{-}lin}|$, (b) threshold voltage V_{th} of nFinFETs and pFinFETs with three different channel lengths ($L = 16$, 120 and 240 nm) at several irradiation steps in the "diode"-bias condition.



(a)



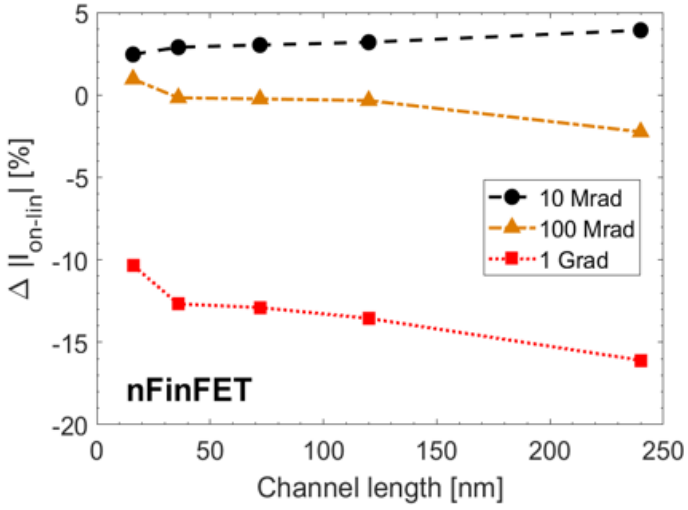
(b)

Figure 4.8: Degradation of (a) maximum drain current $\Delta|I_{on\text{-}lin}|$ and (b) threshold voltage ΔV_{th} as a function of dose for three representative channel lengths: $L = 16$ nm in blue (shortest channel), $L = 120$ nm in black, and $L = 240$ nm in red (longest channel). nFinFETs and pFinFETs were irradiated up to 1 Grad(SiO_2) in the "diode"-bias condition. The measurements are carried out at room temperature in the linear region ($\Delta|V_{ds}| = 50$ m V). (From [137])

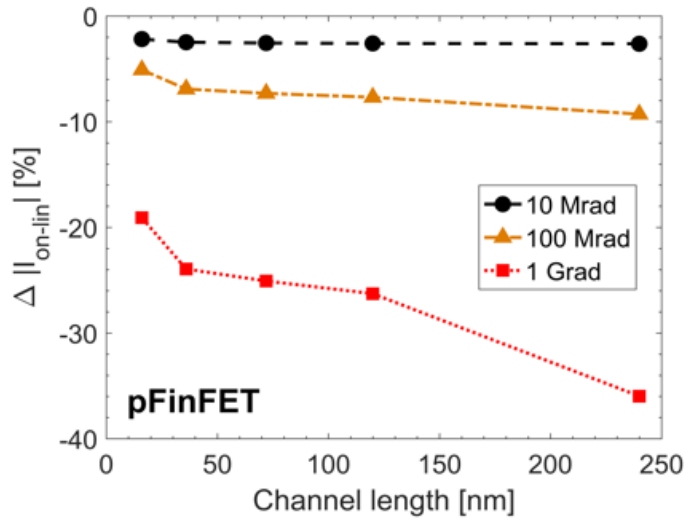
Both nFinFETs and pFinFETs exhibit a channel length dependent TID sensitivity of $|I_{on\text{-}lin}|$, where the longest transistor has the worst degradation. pFinFETs with the channel length $L = 16$, 120, and 240 nm exhibit, respectively, a $|I_{on\text{-}lin}|$ degradation of -19%, -26%, and -35% after 1 Grad(SiO_2). The length dependent effect of pFinFETs begins to be clearly visible at the dose over 30 Mrad(SiO_2), while in nFinFETs, the length dependent effect is visible at all cumulate doses.

However, as shown in Figure 4.8(b), the degradation of V_{th} is minimal and insensitive to channel length. This suggests that the TID degradation mechanisms related to the $\Delta|I_{on\text{-}lin}|$ and ΔV_{th} are different.

The channel length dependence is even more clear in Figure 4.9, where the degradation of $|I_{on\text{-}lin}|$ is plotted as a function of channel length for nFinFETs and pFinFETs at several irradiation steps in the "diode"-bias condition. In nFinFETs irradiated up to 10 Mrad(SiO_2), $\Delta|I_{on\text{-}lin}|$ is positive with a slight channel length dependence. At 100 Mrad(SiO_2), the $\Delta|I_{on\text{-}lin}|$ of nFinFETs is almost negligible, while, above 100 Mrad(SiO_2), the degradation of the $|I_{on\text{-}lin}|$ is negative and shows a more clear channel length dependence. The longest transistor exhibits the worst radiation tolerance, with $\Delta|I_{on\text{-}lin}| = -16\%$, vs. $\Delta|I_{on\text{-}lin}| = -11\%$ of the shortest channel transistor.



(a)



(b)

Figure 4.9: Influence of the channel length to the TID sensitivity. The $\Delta|I_{on\text{-}lin}|$ with $\Delta|V_{ds}| = 50$ mV is plotted as a function of channel length in (a) nFinFETs and (b) pFinFETs irradiated up to 1 Grad(SiO_2) in the "diode"-bias condition. (From [137])

In pFinFETs, the $|I_{on\text{-}lin}|$ degradation is always negative. At 10 Mrad(SiO_2), $\Delta|I_{on\text{-}lin}|$ is almost insensitive to channel length. While above 100 Mrad(SiO_2), $\Delta|I_{on\text{-}lin}|$ shows a clear channel-length dependence. The longest channel FinFETs exhibit the highest radiation sensitivity, with the $\Delta|I_{on\text{-}lin}| = -35\%$ vs. $\Delta|I_{on\text{-}lin}| = -19\%$ of shortest device. This channel-length dependence has been reported in some previous works based on bulk Si MOSFET technologies [122, 123] and is related the influence of halo implantations on the TID degradation. In short channel MOSFETs, the overlap of source and drain halos leads to an overall increase of the channel doping. As a result, the higher channel doping reduces the

lateral depletion regions caused by the positive charges trapped in the STI [101], thereby resulting in a better TID tolerance of the shortest devices [122]. Interestingly, the halo implantation has an opposite effect compared to the RISCE, where the shortest devices have the worst tolerance MOSFET devices in [101, 102].

4.2.4 Low Frequency Noise Measurements

Additional insights into the microscopic nature and densities of the defects contributing to the charge trapping can be obtained through the low-frequency noise measurements [79, 123, 150, 155-160]. The dependence of the noise with applied gate voltage can provide further details about the effective energy distribution of the defects [161-164]. The low frequency noise can be parameterized by the expression as follows [161-164]:

$$S_{vd}(f, V_{ds}, V_{gs}) = \frac{K \cdot V_{ds}^2}{f^{\alpha} \cdot (V_{gs} - V_{th})^{\beta}} \tag{4.1}$$

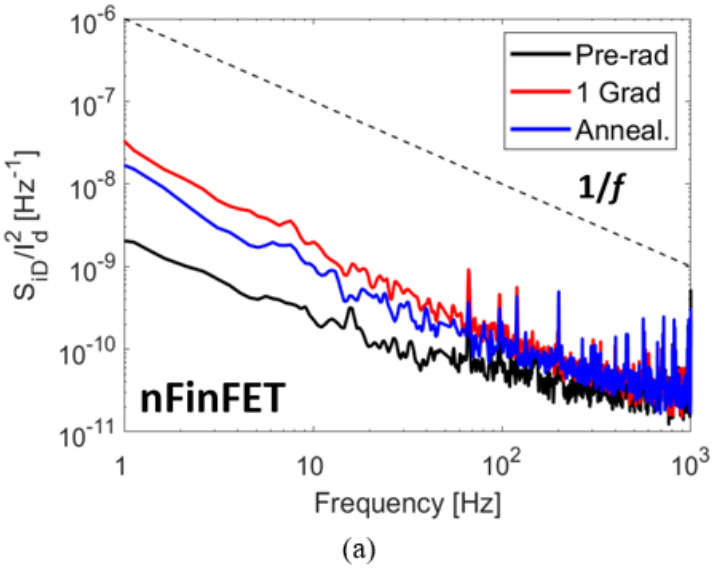
where S_{vd} is the excess drain-voltage noise power spectral density; f is the frequency; V_{ds}, V_{gs}, and V_{th} are the drain, gate, and threshold voltages; K is a constant factor indicating the normalized noise magnitude; α represents the frequency dependence, $\alpha = \partial \log S_{vd} / \partial \log f$; and β represents a measure of the gate-voltage dependence with $\beta = \partial \log S_{vd} / \partial \log |V_{gs} - V_{th}|$ In the linear region of the device response, S_{vd} is related to the drain-current noise power spectral density S_{id} by the relation [161-165]:

$$S_{vd} = R_{ch}^2 S_{id} = \frac{V_{ds}^2}{I_{ds}^2} S_{id} \tag{4.2}$$

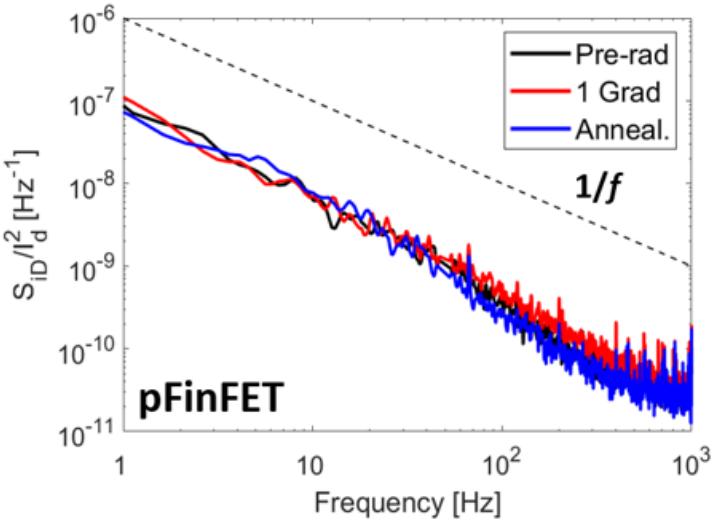
So, Eq. (4.1) can be rewritten equivalently as:

$$\frac{S_{id}}{I_{ds}^2}(f, V_{gs}) = \frac{K}{f^{\alpha} \cdot (V_{gs} - V_{th})^{\beta}} \tag{4.3}$$

The low frequency noise of the MOS devices is mainly caused by the fluctuation of the number of carriers [79, 123, 150, 155-160]. Normally, traps contributing to noise are distributed uniformly in space throughout the gate oxide and in energy in the Silicon bandgap, with the characteristics of $\alpha \approx 1$ and $\beta \approx 2$ [161-165]. In contrast, significant deviations from $\alpha \approx 1$ and $\beta \approx 2$ indicate non-uniform defect-energy distributions in energy and/or space [161-165]. When $\beta > 2$, the effective density of the border traps is increasing toward the mid-gap. As a comparison, when $\beta < 2$, the distribution of border traps is increasing toward the semiconductor conduction band for n-channel devices or the valence band for p-channel devices [161, 162].



(a)



(b)

Figure 4.10: Low-frequency noise magnitudes for (a) nFinFETs and (b) pFinFETs with $L = 240$ nm, irradiated up to 1 Grad(SiO_2) in the "diode"-bias condition. The noise is measured at $|V_{ds}| = 50$ mV and $|V_{gs}| = 0.85$ V at room temperature. (From [138])

Figure 4.10 shows the low frequency noise for (a) nFinFETs and (b) pFinFETs with $L = 240$ nm, before irradiation, at 1 Grad(SiO_2) and after high temperature annealing. Both nFinFETs and pFinFET are characterized by the typical $1/f$ low frequency noise dependence. In nFinFETs, the low frequency noise magnitude increases with the dose, indicating generation of border traps along the gate dielectric/bulk interface. The following decrease of the noise magnitude after the high temperature annealing indicates their partial neutralization [79, 150, 165]. On the contrary, the noise responses of pFinFETs, which have larger noise magnitudes than nFinFETs, are insensitive to the

cumulated dose, as the blue, red and black curves overlap each other. This characteristic is consistent with Figure 4.5(b) and Figure 4.8(b) (the variation of V_{th} is slight in nFinFETs and negligible in pFinFETs), which suggests that the FinFETs under test exhibit a robust gate dielectric to TID.

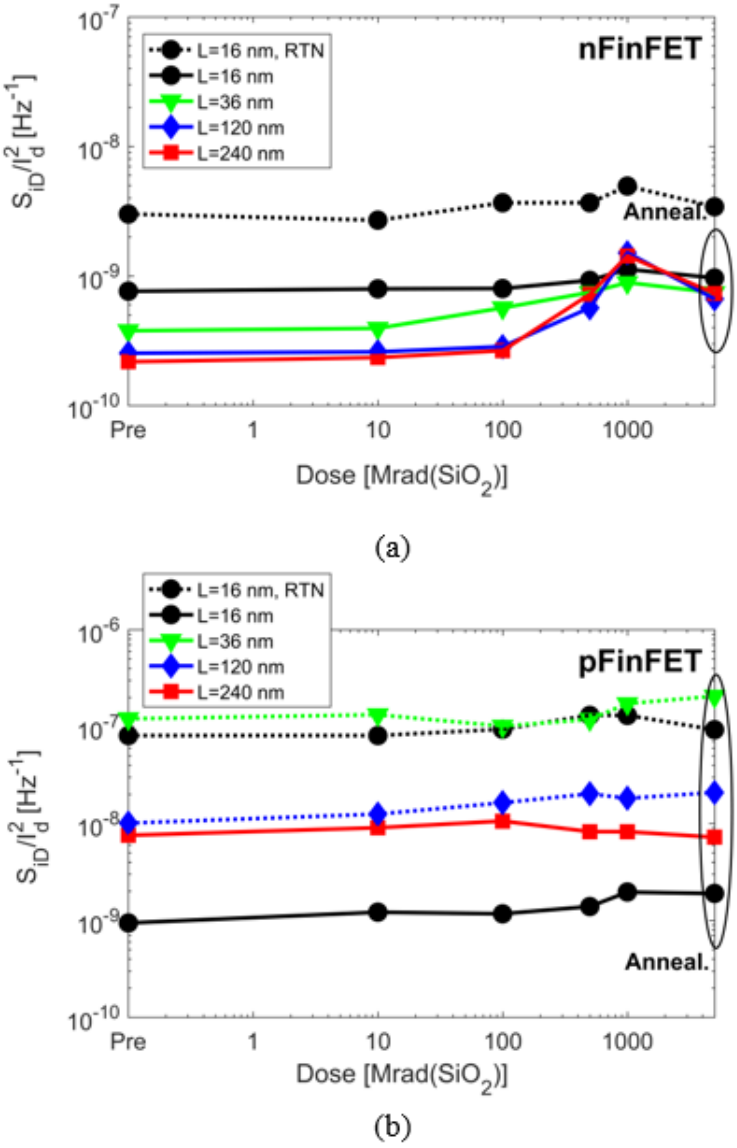


Figure 4.11: Low-frequency noise magnitudes at $f = 10$ Hz vs. dose for (a) nFinFETs and (b) pFinFETs with different channel lengths, irradiated up to 1 Grad(SiO_2) and then annealed for 24 h at 100 °C in the "diode" bias condition. Noise measurements are carried out at $|V_{ds}| = 50$ mV and $|V_{gs}| = 0.85$ V. (From [138])

Moreover, this agrees with a model where the trap activation is due to electric field-driven drift of H^+ ions; in pFinFETs, the electric field favors the H^+ to drift from the gate dielectrics to the gate metallization, while in nFinFETs, the electric field favors the H^+ ions to drift from the gate dielectrics to the interface

with the Si bulk [19, 101].

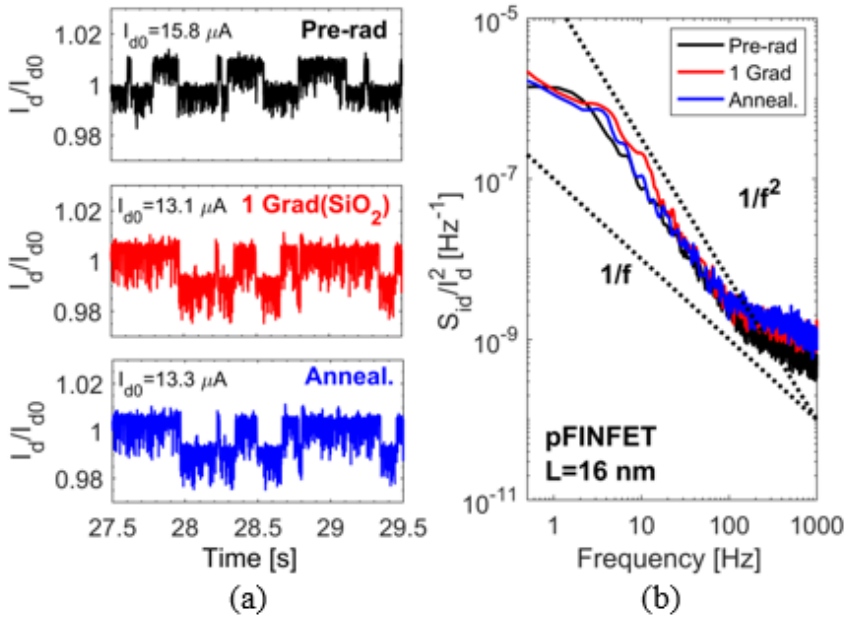


Figure 4.12: Random telegraph noise for a pFinFET $L = 16$ nm, irradiated up to 1 Grad(SiO2) in the "diode"-bias condition. (b) Low frequency noise for the device of (a). The noise is measured at $|V_{ds}| = 50$ mV and $|V_{gs}| = 0.85$ V at room temperature. (From [138])

Figure 4.11 plots the low-frequency noise at 10 Hz as a function of dose in nFinFETs and pFinFETs with four different channel lengths ($L = 16$, 36, 120 and 240 nm). The noise magnitude of nFinFETs scales inversely with gate area [19] and increases with dose. nFinFETs typically exhibit the ~$1/f$ low frequency dependence, except for some short channel devices that exhibit $1/f^2$ noise at low frequencies, when Random Telegraph Noise (RTN) [166] dominates in the time domain. The low-frequency noise magnitude of long channel FETs increases substantially after 100 Mrad(SiO_2), similarly to the V_{th} increase in Figure 4.8(b). These increments may suggest traps generation along the gate dielectric/bulk interface and/or at the upper corner of the STI [107, 138]. Previous studies report that STI-trapped charge contribute to the noise increase of n-channel MOS devices irradiated up to ultra-high doses [166, 167]. Moreover, [167] reported that a lower degradation in the noise response was detected in I/O devices, which uses higher bulk doping. The channel length dependence of FinFETs visible in Figure 4.11(a) may be related to the increased bulk doping induced by the overlapping of halo implantations.

On the other hand, as processed pFinFETs show larger noise magnitudes than nFinFETs, and the S_{id}-f slopes and S_{id} magnitudes depend on channel length. Generally, the noise response of pFinFETs with $L \leq 120$ nm can vary from device to device, as short-channel devices may exhibit Lorentzian noise,

characterized by $\sim 1/f^2$ slopes at low frequency [150, 165, 168]. Indeed, the noise response of the pFinFETs indicated by the dotted curves of Figure 4.11(b) is characterized by RTN [166] in the time domain (see Figure 4.12(a)). RTN is visible only in the small devices, due to the alternate capture and emission of carriers at individual defect sites, which generate discrete switching in the device channel resistance [150, 165]. Figure 4.12(a) shows a dominant trap present before irradiation, with unique amplitude and capture/emission times. This defect causes the Lorentzian power spectra of the Figure 4.12(b) with corner frequency at ~ 8 Hz.

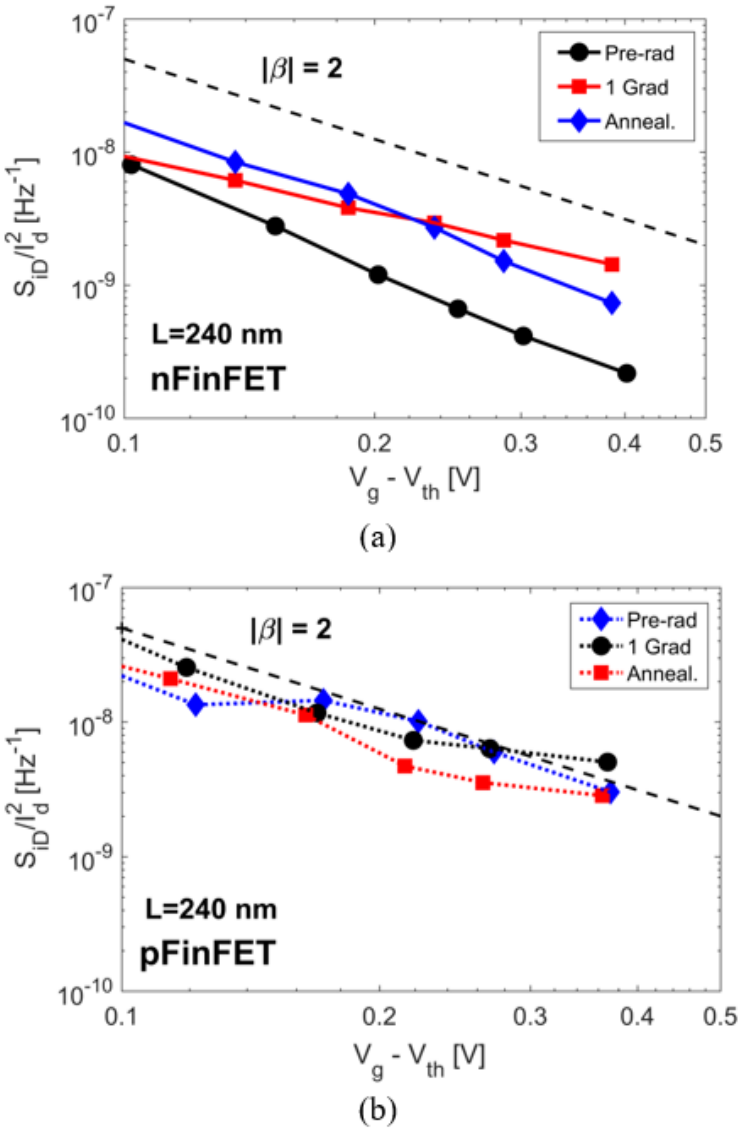


Figure 4.13: $1/f$ noise magnitudes at $f = 10$ Hz vs. $|V_{gs}\text{-}V_{th}|$ at $|V_{ds}| = 50$ mV for FinFETs with $L = 240$ nm. Transistors were irradiated in the "diode" bias condition with the noise measured before exposure, at 1 Grad(SiO_2) and after 24 hours annealing at 100 °C: (a) nFinFET, and (b) pFinFET. (From [138])

In Figure 4.13, the low frequency noise magnitude at 10 Hz is plotted as a function of $|V_{gs}\text{-}V_{th}|$ for the longest nFinFETs and pFinFETs, before irradiation, at 1 Grad(SiO_2) and after annealing. Referring to the expression (4.2), when $\beta > 2$, the effective density of the border traps increases toward mid-gap, while at $\beta < 2$ the distribution of border traps increases toward the conduction band for n-channel devices and valence band for p-channel devices [150, 162, 165].

In nFinFETs, the slope $|\beta|$ of $S_{id}\text{-}|V_{gt}|$ before the irradiation is ~ 2, indicating approximately uniformly distributed defects in space throughout the gate oxide and in energy in the silicon band gap. After the exposure to 1 Grad(SiO_2), the magnitude increases and the slope $|\beta|$ decreases to values < 2, indicating the generation of traps with a distribution that increases toward the semiconductor conduction band. After high temperature annealing, the slope $|\beta|$ is back to ~ 2, indicating a re-configuration in the space and energy distribution of border traps. The increase of the noise levels, the g_m rebound, and the V_{th} increase after the irradiation indicate generation of border/interface traps at the upper corner between the STI and the gate oxide.

On the other hand, in pFinFETs, the slope $|\beta|$ of $S_{id}\text{-}|V_{gt}|$ is ~ 2, indicating uniformly distributed and stable distributed defects before irradiation, after the exposure and after the annealing.

4.3 Discussion

The DC static measurements of FinFETs up to ultra-high doses highlight that the TID sensitivity depends on bias conditions and channel lengths. The slight shifts of V_{th} and the negligible degradation of *SS* suggest the high tolerance of the gate stack to the TID effects [17, 18, 47]. The marginal increase of V_{th} of nFinFETs suggests few effects related to border and interface traps in the gate oxide. Meanwhile, the large degradation of g_m and the increase of $I_{off\text{-}lin}$ in nFinFETs and pFinFETs indicate the buildup of large densities of trapped charge in the STI oxides [101, 118, 123]. In addition, the very similar trends of the degradation of $I_{on\text{-}lin}$ and $g_{m\text{-}MAX}$ indicate that the decrease of $I_{on\text{-}lin}$ is mostly due to the degradation of g_m.

Figure 4.14 shows the evolution of the TID degradation mechanisms related to the STI for nFinFETs and pFinFETs. The TID-induced effects are analyzed in transistors at high ($\sim$ 1-10 Mrad(SiO_2)) and ultra-high doses ($>$ 10 Mrad(SiO_2)), when the devices are ON, i.e. biased with $|V_{gs}| = 0.9$ V.

At high doses, the positive trapped charge in the STI of nFinFETs dominates the TID response by inverting the lateral bulk regions, generating deep drain-to-source parasitic paths, and increasing the $I_{off\text{-}lin}$ leakage current [18, 101, 118]. In pFinFETs, the positive trapped charge in STI dominates the TID degradation by depleting the channel regions close to the upper corner of the STI (yellow regions

of Figure 4.14). This causes a reduction of the effective channel width (or channel height), consequently degrading the g_m of pFinFETs [101, 123]. The increase of the leakage current of pFinFETs is probably due to the peripheral drain to substrate junction leakage current. This current is associated with the surface generation at the intersection of the depletion region and the STI sidewalls, where a high density of interface traps is located [152, 153].

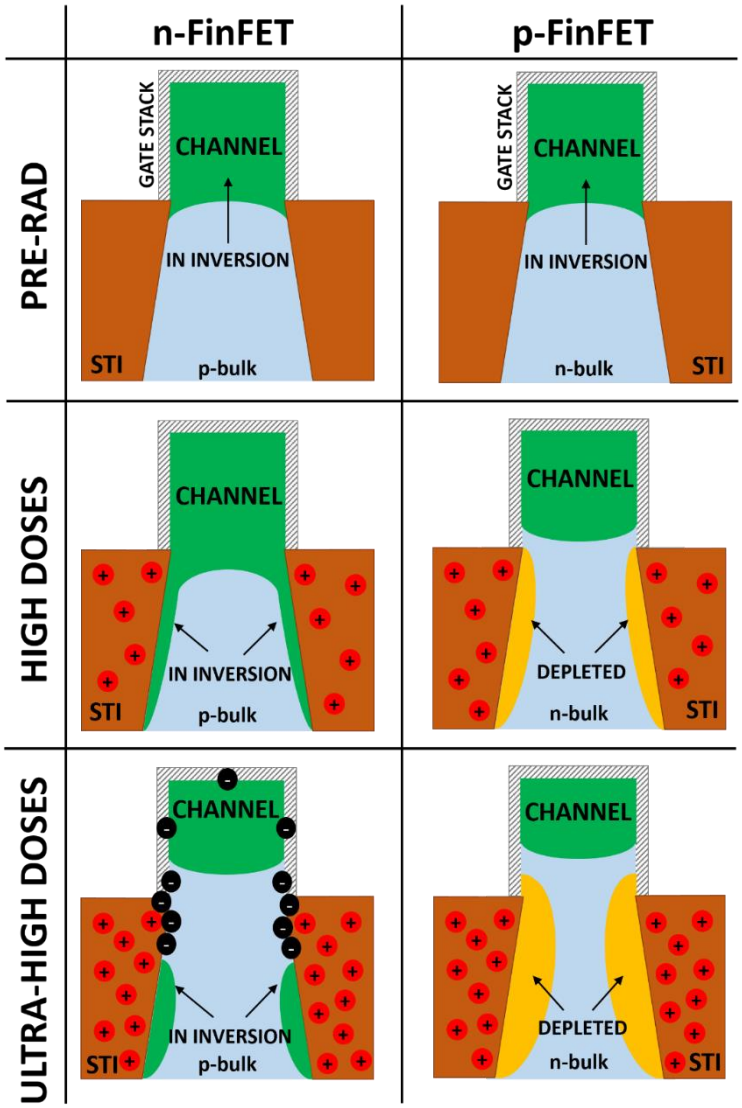


Figure 4.14: The degradation mechanism in nFinFETs and pFinFETs is shown schematically through a vertical cut-plane normal to the channel fin. TID-induced effects are illustrated when devices are biased in inversion ($|V_{gs}| = 0.9$ V) at high ($\sim$ 1-10 Mrad(SiO_2)) and ultra-high doses ($>$ 10 Mrad(SiO_2)). The green colored regions are inverted regions of the Si bulk, while the yellow-colored ones identify the depleted (or non-inverted) regions. Positive trapped charges are indicated with "+", while "−" indicated the interface traps that are negatively charged.

At ultra-high doses, TID effects differ for nFinFETs and pFinFETs. In nFinFETs, the increase of the drain leakage current suggests a continuous buildup of positive charge in the deep oxide regions of the STI. However, the rebound of the g_m at 10 Mrad(SiO_2) indicates a large generation of interface traps at the corner between the STI and the gate oxide [17, 18, 47, 107, 108, 118, 165, 169], which can deplete the lateral regions and reduce the effective channel width. The slight increase of the V_{th} could be caused by a slight increase of the interface traps at the gate dielectric/channel interface. In pFinFET, the strong degradation of the g_m indicates that more positive charge is trapped in the STI combined to positive trapped charge at the interface of STI/Si [121, 141].

In both nFinFETs and pFinFETs irradiated at ultra-high doses, the "off" bias condition exhibits the highest TID tolerance, most likely due to enhanced electron-hole recombination in the STI at lower electric fields [149, 154, 169]. The difference of the TID degradation between "diode" and "on" bias condition for nFinFETs and pFinFETs is almost negligible, showing the insensitivity of the TID response of these devices to lateral drain-to-source electric fields. The high degradation in "on" and "diode" bias conditions of nFinFETs agrees with a model where the interface trap activation is due to electric field-driven drift of H^+ ions; the electric field favors the drift the H^+ ions from the oxides to the SiO_2/Si interfaces [108, 142, 169].

The absence of RISCE suggests that the degradation of the LDD spacers is minimal or that its impact is minor compared to other technologies [99, 101, 102]. In fact, the TID tolerance of short channel FinFETs is higher in these devices than in the longer channel transistors, showing an opposite channel length dependence compared to some 65 nm MOSFET technologies. The improved responses of the shortest channel transistors are related to the halo implantations [107, 122, 123]. This effect has been studied in 28 nm planar MOSFET devices [122, 123], and is here shown also to affect the FinFET-based technology. The overlapping of halo doping for the sources and drains of short channel devices increases the effective channel doping, limiting the lateral depleted region and consequently attenuating the degradation of the g_m, as shown in Figure 4.8 and Figure 4.9.

4.4 Conclusions

In this chapter, for the first time, a 16 nm bulk FinFETs technology has been evaluated at ultra-high doses. Negligible variation of V_{th} and *SS* and small variations in the low frequency *1/f* noise confirm the high TID tolerance of the gate stack. The TID response of FinFETs irradiated up to 1 Grad(SiO_2) is dominated by the trapped charge buildup in STI with large degradation of the transconductance. At doses up to 10 Mrad(SiO_2), the dominant degradation mechanism is the trapping of positive charge in the STI. At ultra-high doses (> 10 Mrad(SiO_2)), the effects of interface traps at the corner between the STI and

the gate oxide and along the interface of STI/Si can become more significant in nFinFETs.

The TID sensitivity depends on the bias condition and channel length. The worst TID tolerance is observed in transistors irradiated in “diode” or “on” conditions, as a result of the increased charge yield. Short channel devices have a better TID tolerance than long channel ones, thanks to the influence of halo implantations, which improve the TID tolerance of short channel transistors.

Chapter 5

Influence of Fin- and Finger-Number on TID Degradation

In this chapter, the fin- and finger-number dependence of the total ionizing dose (TID) degradation in 16 nm bulk Si FinFETs is investigated at ultra-high doses. n- and p-FinFETs designed with different numbers of fins and fingers are irradiated up to 500 Mrad(SiO_2) and then annealed for 24 hours at 100 C. The TID responses of nFinFETs are insensitive to fin number, as dominated by the border and interface traps generation in STI and / or gate oxide. However, pFinFETs show a visible fin-number dependence with worst tolerance of transistors with smallest number of fins. The fin number dependence may be related to a larger charge trapping in STI located at the opposite lateral sides of the first and last fins. In addition, both n- and p-FinFETs exhibit almost TID insensitivity to the finger-number. During the design of integrated circuits, the TID tolerance of electronic systems can be enhanced by preferably using transistors with higher number of fins than fingers.

The exploration of the TID effects at ultra-high doses has just started in FinFET technologies. Our previous work [137] (shown in detail in Chapter 4) about the 16 nm bulk Si FinFETs irradiated up to 1 Grad(SiO_2) evidenced strong TID-induced effects related to the charge buildup in the STI oxides. Irradiated FinFETs suffered by large transconductance degradation with an enhanced tolerance of short channel devices [137]. The improved responses of shortest channel transistors have been related to halo implantations, similarly to the 28 nm planar MOSFETs [113, 122, 123]. However, the previous work [137] was limited to the investigation of the TID mechanism and its dependence with the applied bias and channel length. However, recent studies [143, 165, 171, 172] at lower doses have identified that the TID sensitivity of FinFET devices can depend on the geometry and number of fins. The fin-number and finger-number dependence of the TID response of Si-based FinFET transistors at ultra-high doses is still unknown and is of great interest to enhance the TID tolerance of IC systems during the design.

In this chapter, for the first time, the TID-induced effects in the 16 nm bulk Si FinFET technology are explored at ultra-high doses in the devices having different numbers of fins and fingers. Transistors performances are almost identical for transistors having the same multiplication $n_{fin} \times n_{finger}$. The static DC measurements of FinFETs irradiated up to 500 Mrad(SiO_2) highlight a clear fin-number dependent TID effect, which improves the TID tolerance of pFinFETs using high fin-numbers. On the other side, the TID response of n- and p-FinFETs is insensitive to the number of fingers. Therefore, during the design of integrated circuits (IC), the TID tolerance of electronics can be enhanced by preferably using transistors with high number of fins respect than fingers.

The work presented in this chapter has been carried out within the FinFET16v2 experiment funded by the National Institute for Nuclear Physics - INFN, in a collaboration with: University of Bergamo, Bergamo, Italy; University of Milano Bicocca, Milano, Italy; and École polytechnique fédérale de Lausanne, Lausanne, Switzerland.

Most of the results and figures presented in this chapter have been published and/or submitted in the following peer-reviewed publications:

- [170] T. Ma, S. Bonaldo, S. Mattiazzo, A. Baschirotto, C. Enz, A. paccagnella and S. Gerardin, "Influence of fin- and finger-number on TID degradation of 16 nm bulk FinFETs irradiated to ultra-high doses". *IEEE Transactions on Nuclear Science*. (Accepted for NSREC 2021 conference, Ottawa, Canada, and currently submitted for publication in IEEE Transactions on Nuclear Science.)

Moreover, the results in this chapter have been presented at the following international conference:

- Nuclear and Space Radiation Effects Conference - NSREC 2021, online event, 19th - 23rd July 2021, oral presentation about "Influence of fin- and finger-number on TID degradation of 16 nm bulk FinFETs irradiated to ultra-high doses". (I was the presentation author)

5.1 Devices and Experiments

5.1.1 Devices Description

The devices under test (DUTs) were fabricated in a CMOS Si-based 16 nm FinFET commercial technology using a high-*k* metal gate structure and halo implantations [141, 148]. The transistors were designed for core applications with standard threshold voltage and nominal operating voltage of 0.85 V. DUTs were provided in an array structure, containing n- and p-channel FinFETs with different numbers of fins n_{fin} (2, 4, 5, 10 and 20) and fingers n_{finger} (1, 2, 5, 10 and

100). Figure 5.1 shows a schematic view of the layout of FinFET devices designed in two configurations: (a) 5 fins and 1 finger, and (b) 5 fins and 2 fingers. As the worst effects are often observed in long channel devices [137], the transistors analyzed in this paper have the channel length of $L = 240$ nm, and same fin width and height (i.e. same effective channel width).

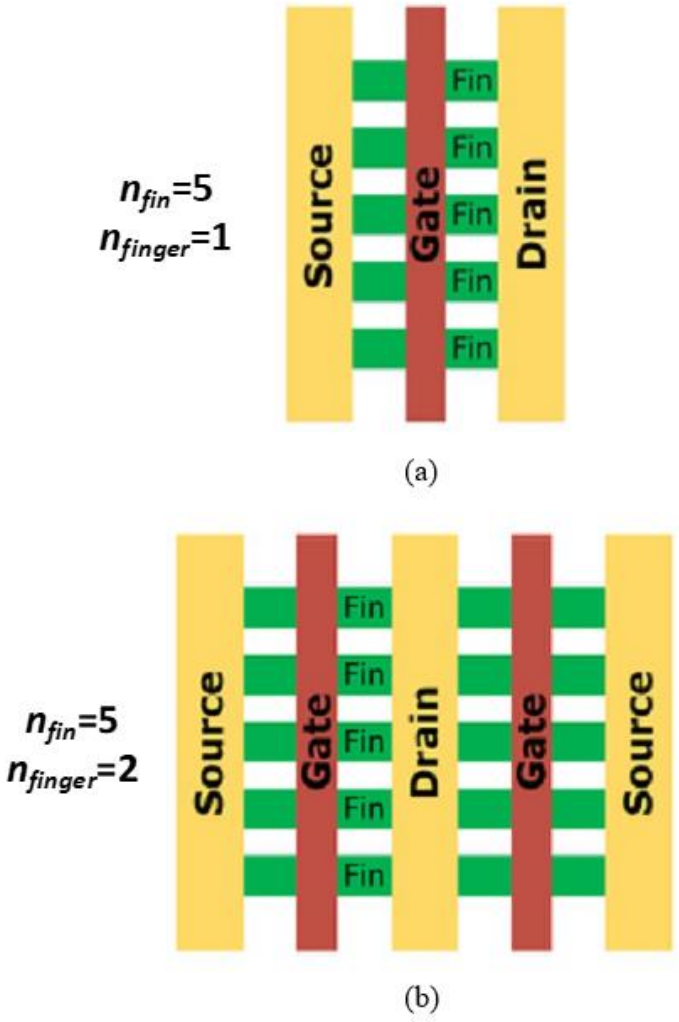


Figure 5.1: Schematic layout of FinFETs designed in two different configurations: (a) $n_{fin} = 5$ and $n_{finger} = 1$, and (b) $n_{fin} = 5$ and $n_{finger} = 2$. (From [170])

The transistors of the same channel type shared source and bulk contacts with separated drain and gate contacts. The gate terminals were protected by electro-static discharge (ESD) protections designed in a two-diodes configuration. A customized probe-card allowed twelve different transistors to be biased and measured at the same time.

5.1.2 Irradiation Conditions and Measurements Details

The irradiation was conducted at room temperature using 10 keV X-rays produced by a Seifert Model RP 149 X-ray irradiator at the University of Padova, Italy [149]. The dose rate was set at 4.7 Mrad(SiO_2)/h for a total exposure time of about 5 days to reach 500 Mrad(SiO_2). The radiation exposure was stopped at several irradiation steps, each device was immediately tested once per step interval using a switching matrix. After irradiation, transistors were annealed at 100 ℃ for about 24 hours. Congruentl y with our previous work [137], the irradiations and annealing tests were performed in the worst bias condition, i.e. "on" ($|V_{gs}| = 0.9$ V and $|V_{ds}| = 0$ V). The DC characteristics of the devices were tested at room temperature in the linear regime ($|V_{ds}| = 50$ mV) before exposure, after irradiation and after high-temperature annealing.

Measurements were performed on more than 100 transistors, and at least three devices of each type and size were evaluated. Nominally identical devices irradiated and annealed under similar conditions show DC parameter shifts that typically vary by less than $\pm$ 5%. Representative results are shown below.

5.2 Experimental Results

In the following section, the TID responses of FinFETs are reported by measuring the DC static characteristics and extracting the main parameters: maximum drain current variation ($\Delta I_{on\text{-}lin}$), threshold voltage shift (ΔV_{th}), degradation of the transconductance (Δg_m) and subthreshold swing variation (ΔSS). The $I_{on\text{-}lin}$ current is defined as the drain-to-source current in the linear region ($|V_{ds}| = 50$ mV) when the channel is in strong inversion at $|V_{gs}| = 0.9$ V. The threshold voltage V_{th} is extracted by the linear region (ELR) method [151], as the gate voltage axis intercept of the linear extrapolation of the I_d-V_{gs} characteristics at its maximum first derivative point.

5.2.1 Pre-rad Performance

It is firstly interesting to analyze the performances of pristine transistors when designed with different number of fins and fingers, but same total number of channels n_{ch}. The total number of channels n_{ch} is defined as the multiplied value of fin-number and finger-number:

$$n_{ch} = n_{fin} \times n_{finger}$$

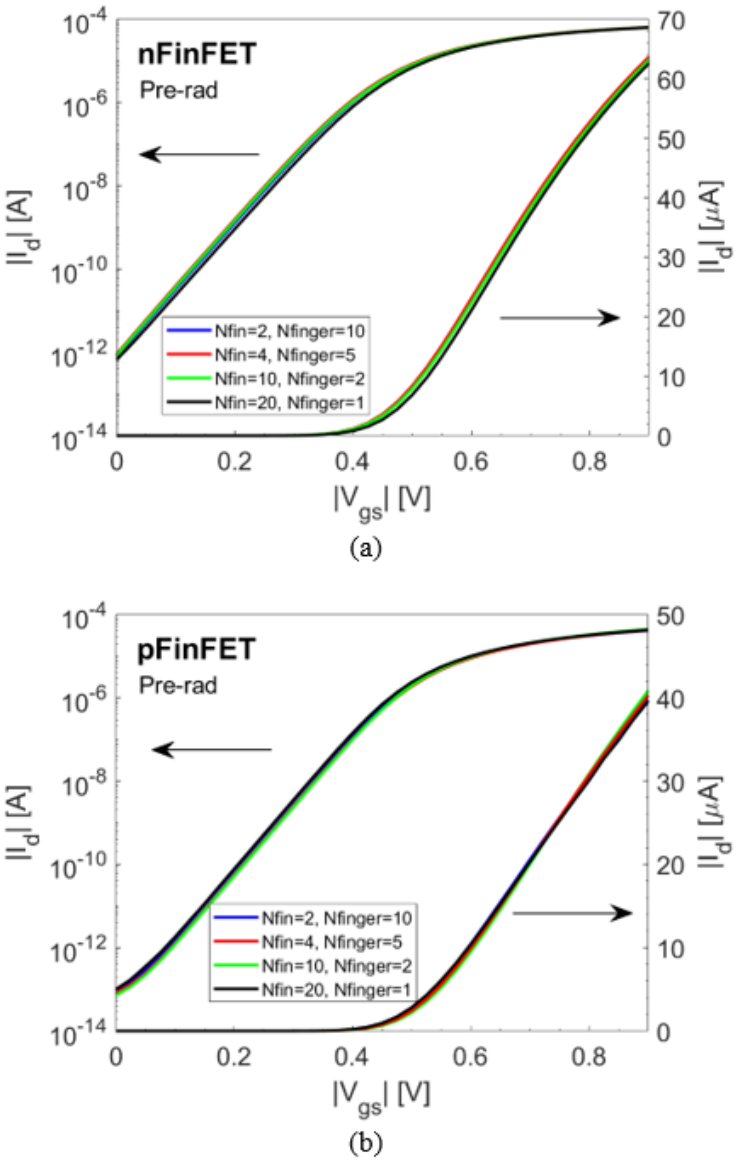


Figure 5.2: $|I_d|$-$|V_{gs}|$ characteristics of (a) nFinFETs and (b) pFinFETs with $L = 240$ nm, 20 channels and different numbers of fins and fingers before the irradiation. Measurements are carried out at room temperature in the linear region ($|V_{ds}| = 50$ mV). (From [170])

Figure 5.2 shows the $|I_d|$-$|V_{gs}|$ characteristics of pristine (a) nFinFETs and (b) pFinFETs designed with $n_{ch} = 20$ several numbers of fins and fingers. The DC responses overlap one to each other, indicating that almost identical DC performances are retrieved when nFinFETs and pFinFETs are designed with a constant value of n_{ch}.

5.2.2 TID Sensitivity

During the design of IC systems, the possibility to choose transistors with

different layouts but same performances may be extremely interesting. Indeed, in order to ensure the highest TID tolerance by design, the designer may employ transistors with the best TID tolerance. For this reason, the following Figure5.3, 5.4 and 5.5 analyze the TID response of transistors with same $n_{ch} = 20$, i.e. same DC performances as shown in Figure 5.2.

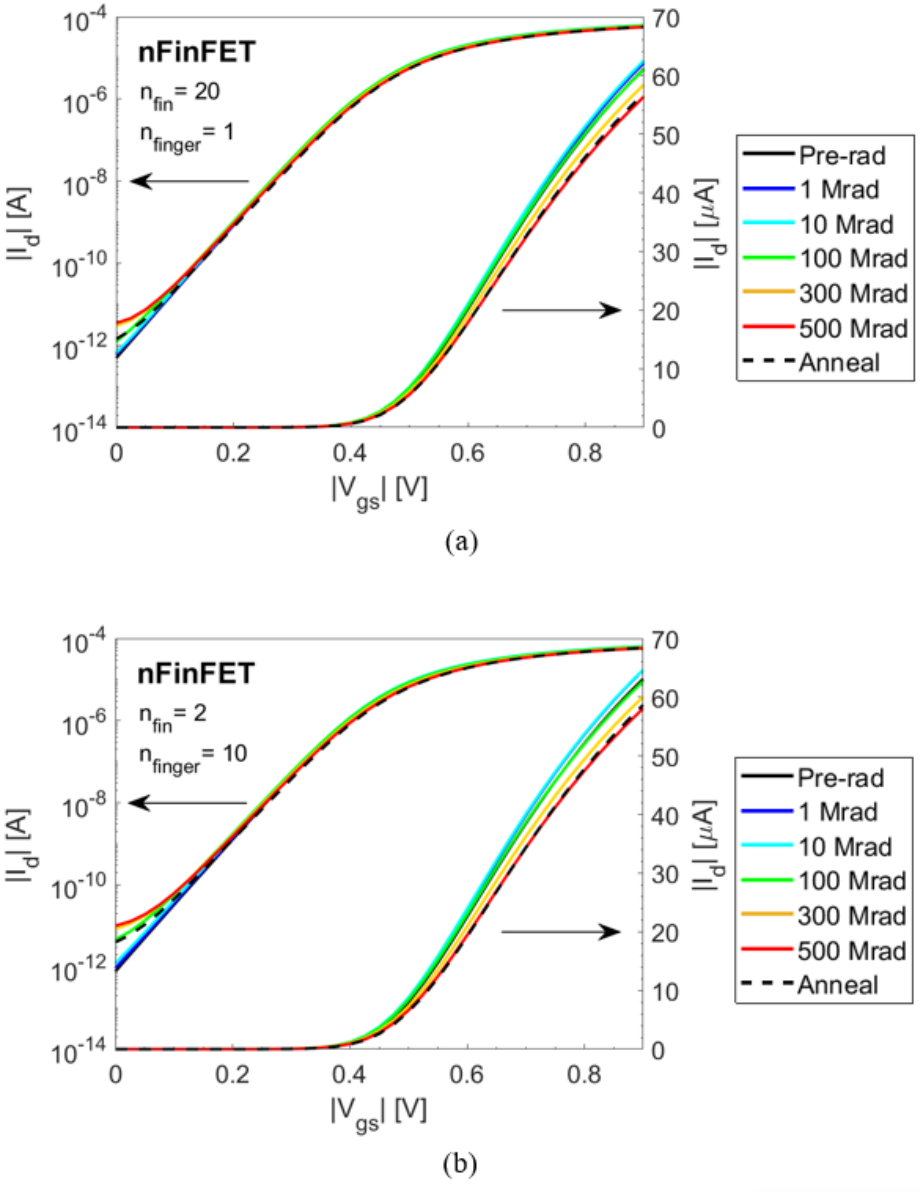
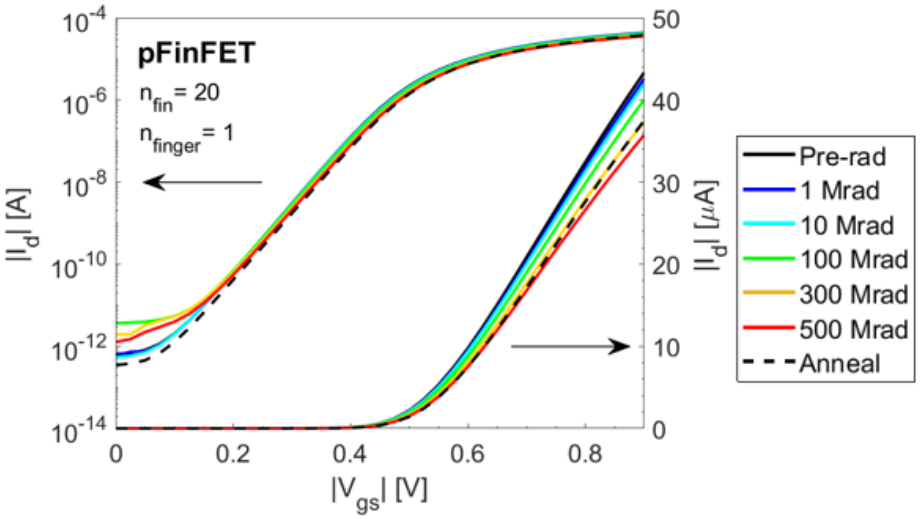


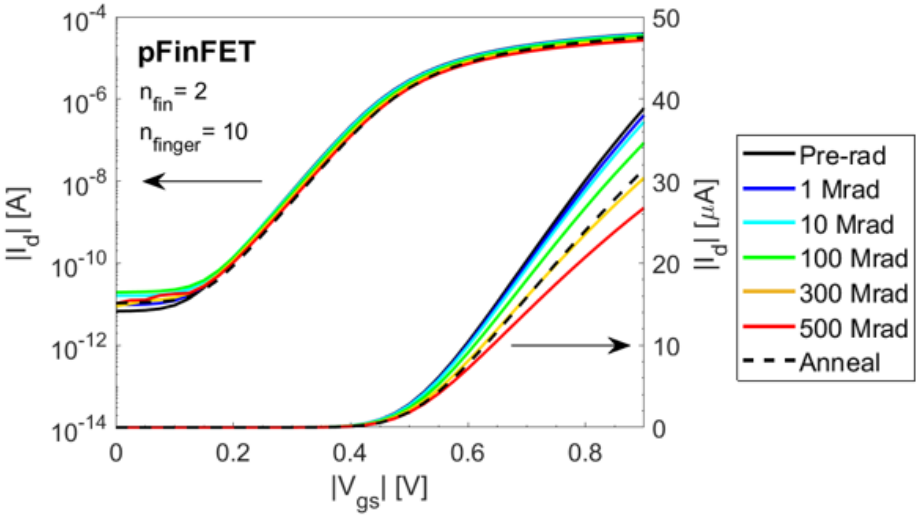
Figure 5.3: $|I_d|$-$|V_{gs}|$ curves in the linear region ($|V_{ds}| = 50$ mV) of nFinFETs with $L = 240$ nm. Devices were irradiated up to 500 Mrad(SiO_2) and then annealed for 24 h at 100 ℃ in the "on"-bias condition. (a) $n_{fin} = 20$, $n_{finger} = 1$, and (b) $n_{fin} = 2$, $n_{finger} = 10$. (From [170])

Figure 5.3 plots $|I_d|$-$|V_{gs}|$ curves at $|V_{ds}| = 50$ mV for nFinFETs designed with (a) $n_{fin} = 20$, $n_{finger} = 1$, and (b) $n_{fin} = 2$, $n_{finger} = 10$. The TID responses are shown at several irradiation steps and after 24 h of annealing at

100 °C in "on"-bias condition. After 500 Mrad(SiO_2), the $I_{on\text{-}lin}$ defined as the maximum drain current at $|V_{ds}| = 0.9$ V and $|V_{ds}| = 50$ mV, decreases by about 7.8% (a) and 7.9% (b), while the off leakage current at $V_{gs} = 0$ V increases of less than an order of magnitude. The 24 hours annealing at high temperature causes a negligible recovery of their DC responses. The TID response of nFinFET (a) has very similar TID degradation to that of (b), evidencing the TID insensitivity of nFinFETs to the fin- and finger-number.



(c)

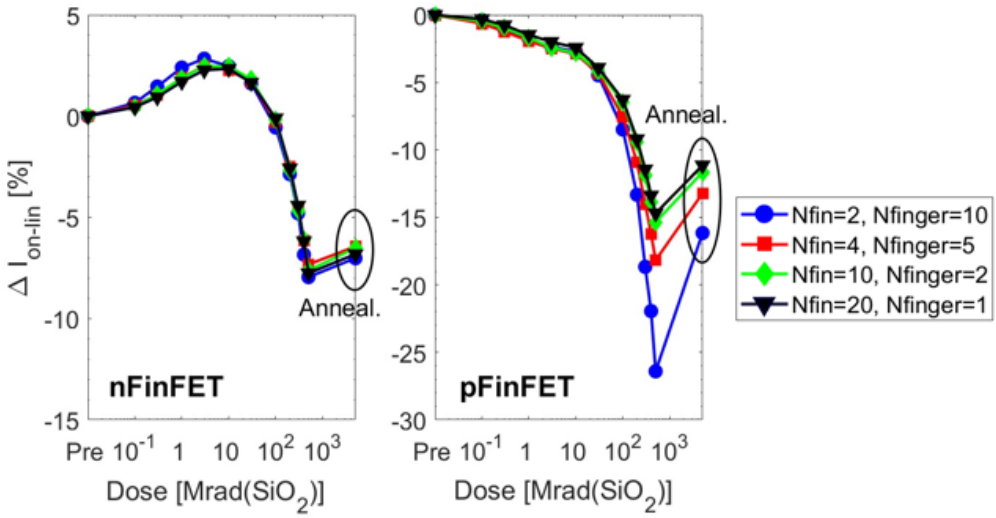


(d)

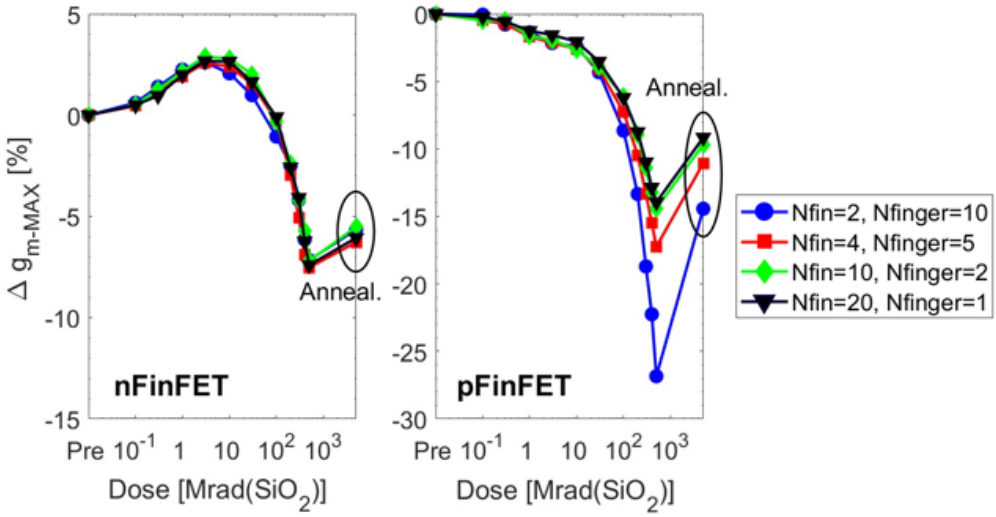
Figure 5.4: $|I_d|$-$|V_{gs}|$ curves in the linear region ($|V_{ds}| = 50$ mV) of pFinFETs with $L = 240$ nm. Devices were irradiated up to 500 Mrad(SiO_2) and then annealed for 24 h at 100 ℃ in the "on"-bias condition. (a) $n_{fin} = 20$, $n_{finger} = 1$, and (b) $n_{fin} = 2$, $n_{finger} = 10$. (From [170])

Similarly to Figure 5.3, Figure 5.4 shows the $|I_d|$-$|V_{gs}|$ characteristics at

$|V_{ds}| = 50$ mV of pFinFETs irradiated up to 500 Mrad(SiO_2) and then annealed for 24 h at 100 °C: (a) $n_{fin} = 20$, $n_{finger} = 1$, and (b) $n_{fin} = 2$, $n_{finger} = 10$. pFinFETs exhibit a larger degradation compared to nFinFETs, due to a large transconductance degradation related to charge buildup in the STI [137]. pFinFETs in Figure 5.4(b) with the lowest fin-number and highest finger-number exhibits the worst TID degradation. At 500 Mrad(SiO2), the (b) device shows a $\Delta I_{on\text{-}lin}$ of -26.4% vs. -14.7% of (a) device. After 24 hours annealing at 100 °C, both pFinFETs show a slight recovery of their DC static characteristics, e.g. the pFinFETs (a) shows a $\Delta I_{on\text{-}lin}$ recovery from -26.4% at 500 Mrad(SiO_2) to -16.2% after annealing.



(a)



(b)

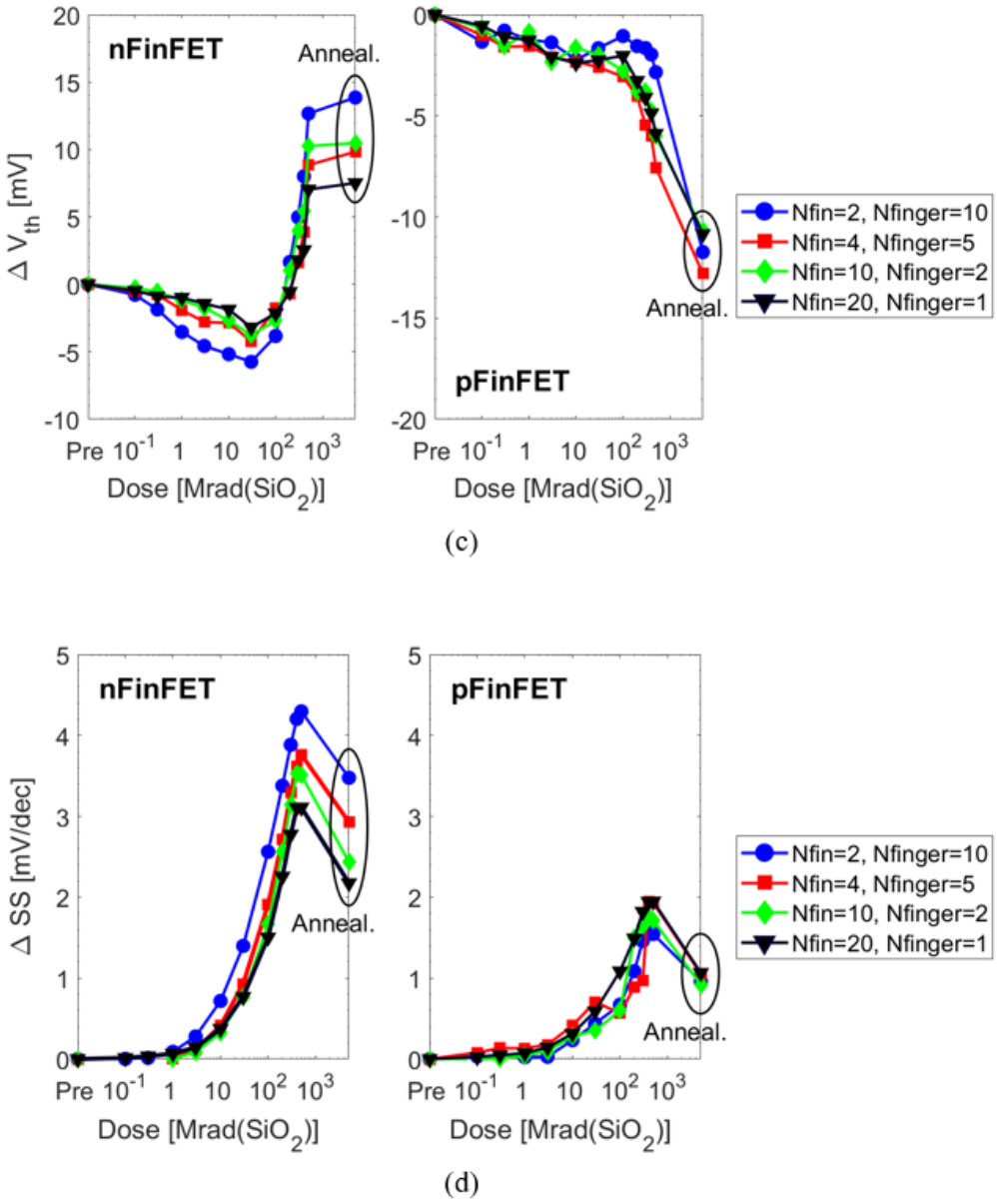


Figure 5.5: Degradation of (a) maximum drain current $\Delta I_{on\text{-}lin}$ (b) maximum transconductance $\Delta g_{m\text{-}MAX}$, (c) threshold voltage ΔV_{th}, and (d) subthreshold swing ΔSS as a function of dose in nFinFETs and pFinFETs with 20 channels and varying numbers of fins and fingers. Transistors were irradiated up to 500 Mrad(SiO_2) and then annealed for 24 h at 100 °C in the "on" bias condition. Measurements are carried out at room temperature in the linear region ($|V_{ds}| = 50$ mV). (From [170])

Looking in more details to the DC degradation parameters, irradiated nFinFETs and pFinFETs exhibit significant decreases in transconductance with dose, but only slight threshold voltage shifts and slight degradation of the subthreshold slope after 500 Mrad(SiO_2). This is evidenced by Figure 5.5, which reports the TID degradation of the main DC static parameters as a function of the dose: (a) maximum drain current $\Delta I_{on\text{-}lin}$, (b) maximum transconductance $\Delta g_{m\text{-}}$

$_{MAX}$, (c) threshold voltage ΔV_{th} and (d) subthreshold swing ΔSS of nFinFETs and pFinFETs with different numbers of fins and fingers, but same numbers of channels $n_{ch} = n_{fin} \times n_{finger} = 20$. The $I_{on\text{-}lin}$ of nFinFETs with varying numbers of fins and fingers degrade almost equally, showing a $\Delta I_{on\text{-}lin}$ of about -8% after 500 Mrad(SiO_2). On the contrary, pFinFETs with the smallest fin-number and largest finger-number show the highest I_{on} degradation (-26.4%), which is almost twice that of devices with the large fin-number and small finger-number (-14.7%) at 500 Mrad(SiO_2).

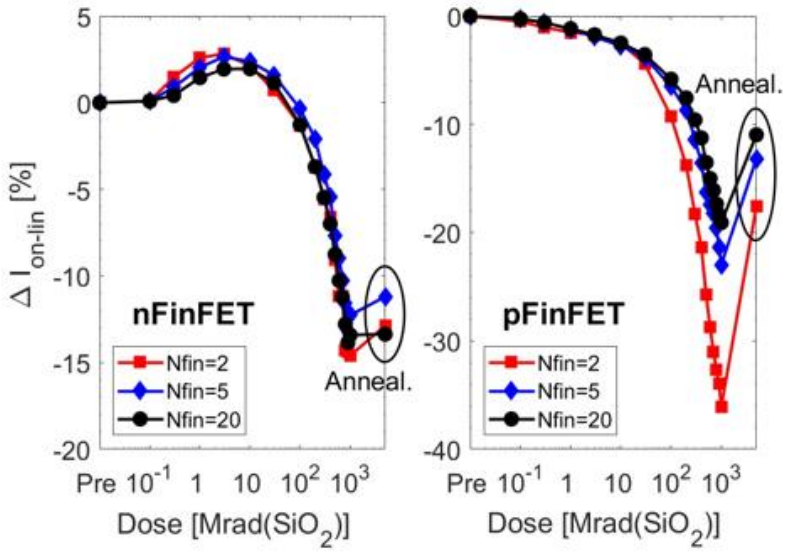


Figure 5.6: Influence of the number of fins to the TID sensitivity. The $\Delta I_{on\text{-}lin}$ with $|V_{ds}| = 50$ mV is plotted as a function of the dose for nFinFETs and pFinFETs with three representative number of fins ($n_{fin} = 2$, 5 and 20) and the same number of fingers ($n_{finger} = 1$). Transistors were irradiated up to 1 Grad(SiO_2) and then annealed at 100 °C for 24 hours in the "on" bias condition. (From [170])

Comparing Figure 5.5(a) and Figure 5.5(b), the $\Delta g_{m\text{-}MAX}$ degradation follows the trend of $\Delta I_{on\text{-}lin}$, indicating that $I_{on\text{-}lin}$ decrease is mostly dominated by the $g_{m\text{-}MAX}$ degradation. The concurrent degradation of $I_{on\text{-}lin}$ and $g_{m\text{-}MAX}$ is related to the buildup of large densities of trapped charge in the STI oxides [122, 123, 137], which decrease the effective channel width of p-channel devices. Compared with the pre-rad parameters ($|V_{th}|$ is $\sim$0.55 V, SS is $\sim$62 mV/dec), after 500 Mrad(SiO_2), the V_{th} shift and the SS variation are slight in nFinFETs (< 13 mV and < 5 mV/dec, respectively) and negligible in pFinFETs (< 8 mV and < 2 mV/dec, respectively), suggesting few effects related to border and interface traps in the gate oxide of the transistors.

5.2.3 Fin-Number Dependence

In order to understand the source of the fin- and finger-number dependence of the TID sensitivity, irradiation tests in Figure 5.6 and Figure 5.7 were carried out on nFinFETs and pFinFETs designed with three representative number of fins (n_{fin} = 2, 5 and 20) and three representative number of fingers (n_{finger} = 1, 10 and 100).

Figure 5.6 reports the $\Delta I_{on\text{-}lin}$ for nFinFETs and pFinFETs with 2 fins, 5 fins and 20 fins, but the same finger-number (n_{finger} = 1). In agreement with Figure 5.5, the TID response of all three n-channel devices almost overlap one to each other, confirming the practical insensitivity of the TID response to fin-number in nFinFETs. On the contrary, in pFinFETs, the degradation of I_{on} shows a visible fin-number dependence. Experimental results show that transistors with minimum number of fins have the highest TID degradation (red curve). After 1 Grad(SiO_2), the $\Delta I_{on\text{-}lin}$ is -36.1% for devices with 2 fins, vs. -19.1% for devices with 20 fins. The I_{on} degradation is comparable to the g_m degradation, buildup of large densities of trapped charge in the STI oxides [122, 123. 137], similar to Figure 5.5(a) and Figure 5.5(b).

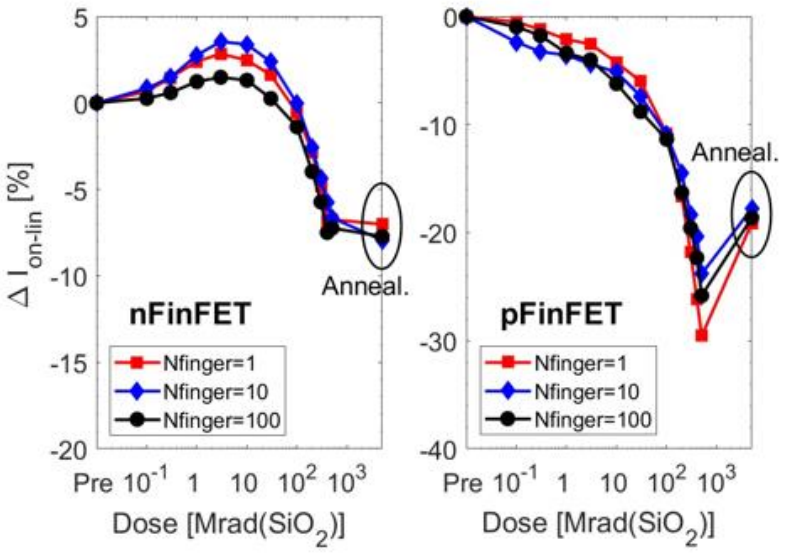


Figure 5.7: Influence of the number of fins to the TID sensitivity. The $\Delta I_{on\text{-}lin}$ with $|V_{ds}|$ = 50 mV is plotted as a function of the dose for nFinFETs and pFinFETs with three representative number of fingers (n_{finger} = 1, 10 and 100) and the same number of fins (n_{fin} = 2). Transistors were irradiated up to 1 Grad(SiO_2) and then annealed at 100 °C for 24 hours in the "on" bias condition. (From [170])

5.2.4 Finger-Number Dependence

Figure 5.7 shows the influence of the number of fingers on the TID response of FinFETs. The degradation $\Delta I_{on\text{-}lin}$ is plotted as a function of the dose for nFinFETs and pFinFETs with three different number of fingers ($n_{finger} = 1, 10$ and 100) and same number of fins ($n_{fin} = 2$). The TID responses of nFinFETs are clearly insensitive to finger-number. Similarly, irradiated pFinFETs with 1 finger shows a I_{on} degradation at 500 Mrad(SiO_2) of -29.6%, which is comparable to -27.7% of the transistor with 100 fingers.

The insensitivity of the TID responses to finger-number evidenced by Fig. 7 confirms that the fin/finger dependence visible in Figure 3, 4 and 5 is related to a fin-dependent TID mechanism.

5.3 Discussions

The TID degradation mechanism in nFinFET is insensitive to fin/finger number, as it is related to border and interface trap buildup at the upper corner of STI and in gate oxide [137]. In contrast, the TID mechanism in pFinFETs is related to positive charge trapping in STI with TID sensitivity depending on the number of fins [137]. The DC static measurements of pFinFETs up to ultra-high doses highlight that the TID sensitivity depends on the number of fins. A similar fin-number dependence of the TID sensitivity was reported by Chatterjee at al. in [171] in n-channel FinFETs, where devices with the larger fin-number have the highest TID tolerance.

The nature of the TID fin-dependent mechanism may be related to high densities of trapped charge in STI. Figure 5.8 shows the evolution of the fin-number dependence mechanisms related to the STI in pFinFETs, when are working in linear regime, i.e. with a flowing source-to-drain current at $|V_{gs}| = 0.9$V and $|V_{ds}| = 50$ mV. The TID-induced effects are analyzed in transistors with one finger and different fin-numbers (2 fins and 10 fins), before the irradiation and at ultra-high doses. The violet color indicates the STI, while the thickness of the red arrows indicates the source-to-drain current intensity for each fin-channel.

Before the exposure, pFinFETs have uniform source-to-drain current in each fin, indicated in Figure 5.8 with uniform thickness of the red arrows. After ultra-high doses (500 Mrad(SiO_2)), the TID response of pFinFETs degrades due to the large transconductance degradation related to positive charge buildup in the STI and at the interface of STI/Si [137, 141], which decreases the $I_{on\text{-}lin}$ [137]. The fin-dependence visible in Figure 5.6 may suggest that more positive charges buildup in the STI of the lateral fins on both sides, inducing a not-uniform degradation of the current flowing in each fin-channels. The higher number of

charges in the lateral STI may be related to a higher density or to a larger STI oxide thickness of the first and last fins. As a consequence, the source-to-drain current of lateral fins decreases more than one of central fins. The degradation of the source-to-drain current of the lateral fins is evidenced in Figure 5.8 by the thinner red arrows on the lateral fins. Therefore, p-FinFETs with the smaller fin-number have the worse TID tolerance. The fin pitch of the devices under test is constant, but it may play an important role on the fin-dependence effect. Larger fin-spacing means thicker middle STI oxides, thus causing more positive charges trapped in the middle STI oxides. If the middle STI are large enough to be comparable to the thickness of the first-last STI, the TID-induced fin-dependent effect may result less visible.

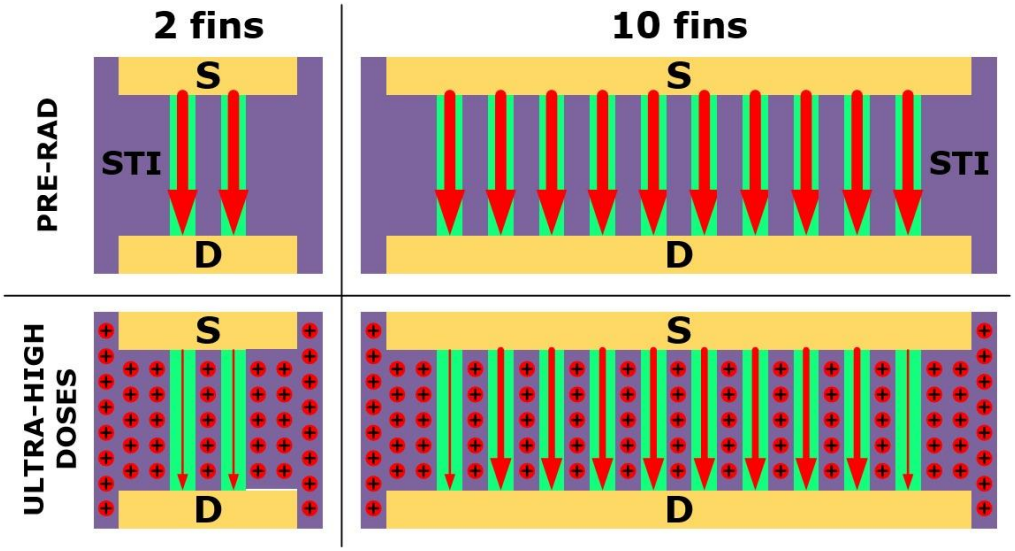


Figure 5.8: The fin-number dependence mechanisms in pFinFETs with 2 fins and 10 fins are shown schematically from a top view. TID-induced effects are illustrated when the devices are biased in "on" condition before the exposure and at ultra-high doses (500 Mrad(SiO_2)). Source and drain are in yellow, STI is in purple, fins are in green, and positive trapped charges in STI are indicated with "+". Red arrows represent the source-to-drain current in each fin when the device is working in the linear region ($|V_{ds}| = 50$ mV). (From [170])

Compared with pFinFETs, nFinFETs show an invisible fin-number dependence, due to the higher TID tolerance of n-channel devices. Some possible reasons are as follows: (1) Different bulk doping can affect the TID responses of transistors [107], as higher doping concentrations in the p-well bulk of nFinFETs can significantly reduce the effects of positive charge buildup in the STI [107, 154]. (2) The interface trapped charge along the sidewall of the STI and in the gate dielectric in nFinFETs is negative, compensating the influence of the positive charge in the STI [19, 102]. (3) In pFinFETs, the negative electric field in the gate dielectric which is opposite direction in nFinFETs field can facilitate net hole trapping in the high-*k* gate dielectric [108]. (4) In nFinFETs, positive charges in

STI invert lateral regions close to the STI. The extension of these inverted regions is limited to the proximity of the STI sidewalls, and do not significantly affect the central channel region. In contrast to these mitigating trends, in pFinFETs, the positive charges in STI deplete a larger fraction of the channel, inducing enhanced transconductance degradation in narrow transistors [101, 102, 104].

5.4 Conclusions

In this chapter, the fin- and finger-number dependence of the TID degradation in bulk Si FinFETs have been evaluated at ultra-high doses. The TID responses of nFinFETs are insensitive to both fin- and finger-numbers. While pFinFETs exhibit a TID sensitivity that visibly depends on the number of fins: worst TID degradation is found in transistors designed with the lowest number of fins, due to the larger TID effects on the lateral fins at both sides. Therefore, for IC applications, the TID tolerance of IC systems can be enhanced by preferably using transistors with higher number of fins than fingers.

Chapter 6

Sample-to-sample Variability Due to Total Dose Effects

In this chapter, we investigate the sample-to-sample variability induced by total ionizing dose (TID) in 16 nm bulk nFinFETs at ultra-high doses, using specially designed test structures and procedures aimed at maximizing matching between transistors. The sample-to-sample variability increases significantly at ultra-high doses ($>$ 100 Mrad(SiO_2)), due to the impact of random dopant fluctuations. The variability of the irradiated transistors is correlated to the initial process-dependent variability.

With CMOS technology scaling at 22 nm and beyond, the semiconductor industry has successfully transitioned to FinFETs due to the excellent gate control and reduced short channel effects over the planar CMOS technologies [173-176]. However, the continuous reduction of the technological feature size brings many problems related to the process variation and layout. Sample-to-sample variability has become a significant issue and one of the most frequently studied subjects in the microelectronic chip research [177-182]. Fewer and fewer atoms are used to fabricate more advanced generations of transistors, and even the present or absence of a single-dopant atom can currently induce a relatively large effect, so that random statistical fluctuations in the manufacturing process play an increasingly important role in integrated circuits [182].

A number of contributions have been presented on origins of variability in MOSFETs and FinFETs, summarizing various sources of the performance variability. The main sources include random dopant fluctuations, surface orientation, line edge roughness, polysilicon grain size, oxide thickness variations and work function variations [178, 179, 181, 183]. However, the impact of variability on the total ionizing dose (TID) response of transistors has rarely been explored. Simone *et al.* showed that there is no any clear increase in sample-to-sample variability in the TID degradation of 65 nm nMOSFETs, and the variability in pMOSFETs is also practically unaffected at doses smaller than 10

Mrad(SiO_2), whereas at doses up to tens of Mrad(SiO_2), variability in the maximum drain current is enhanced without any correlation to pre-rad variability [182]. To our knowledge, no reports exist on the impact of variability on the TID response of FinFETs.

At the state-of-the-art, a CMOS Si-based 16 nm FinFET commercial technology is being evaluated as a promising candidate for the upgrade of the electronics in ATLAS and CMS experiments at CERN, Switzerland [42]. The exploration of the TID effects at ultra-high doses in 16 nm bulk FinFET technologies has just started. Sample-to-sample variability has also a strong impact on the radiation hardness assurance and makes the evaluation of TID effects an increasingly complex and costly problem [184]. Due to the increasing variability, the test of just a limited number of transistors might not be sufficient to get an accurate evaluation of the TID-induced performance degradation of specific devices or circuits. Therefore, in order to more accurately investigate the TID degradation mechanisms in FinFETs and not incur in misleading results, it is essential to evaluate the variability associated to TID effects.

In this chapter, the impact of the sample-to-sample variability on total dose effects in the 16 nm bulk nFinFET technology is explored by performing DC static characteristics measurements. We use specially designed test structures containing several nominally identical FinFETs aimed at maximizing matching between transistors. Our research results show that the variability in nFinFETs is practically unaffected at the doses smaller than 100 Mrad(SiO_2), whereas the cumulate doses up to 100 Mrad(SiO_2), a significant increase in the sample-to-sample variability occurs with an evident correlation to the initial process-dependent variability.

The work presented in this chapter has been carried out within the FinFET16v2 experiment funded by the National Institute for Nuclear Physics - INFN, in a collaboration with: University of Bergamo, Bergamo, Italy; University of Milano Bicocca, Milano, Italy; and École polytechnique fédérale de Lausanne, Lausanne, Switzerland.

Most of the results and figures presented in this chapter have been published and/or submitted in the following peer-reviewed publications:

- [186] T. Ma, S. Bonaldo, S. Mattiazzo, A. Baschirotto, C. Enz, A. paccagnella and S. Gerardin, “Enhancement of sample-to-sample variability induced by total ionizing dose in 16 nm bulk nFinFETs”. *IEEE Transactions on Nuclear Science*. (Accepted for RADECS 2021 conference, Austria, Vienna, and currently submitted for publication in IEEE Transactions on Nuclear Science.)

Moreover, the results in this chapter have been presented at the following international conference:

- Radiation Effects on Components and Systems - RADECS 2021, online

event, 13th - 17th September 2021, oral presentation about "Enhancement of sample-to-sample variability induced by total ionizing dose in 16 nm bulk nFinFETs". (I was the presentation author)

6.1 Devices and Experiments

6.1.1 Devices Description

The devices under test (DUTs) were fabricated in a CMOS Si-based 16 nm FinFET commercial technology using a high-k metal gate structure and most likely halo implantations [141, 148]. Transistors were designed for core applications with standard threshold voltage and nominal operating voltage of 0.85 V. DUTs were designed with special test structure, including six nominally identical nFinFETs and six nominally identical pFinFETs with channel length of 16 nm and 2 fins on the same silicon die. This choice of geometry was made in order to maximize variability among the transistors, which is exacerbated in minimum-size devices. All the transistors have the same fin width and fin height (i.e. same effective channel width). In addition, all the possible methods to optimize matching between them were applied: the devices are oriented in the same way and spacing between the devices is minimum.

DUTs of the same channel type shared source and bulk contacts with separated drain and gate contacts. The gate terminals were protected by electro-static discharge (ESD) protections designed in a two-diodes configuration. A customized probe-card allowed twelve different transistors to be biased and measured at the same time.

6.1.2 Irradiation Conditions and Measurement Details

The irradiation was conducted at room temperature using 10 keV X-rays at the University of Padova, Italy. The dose rate was set at 4.7 Mrad(SiO_2)/h for a total exposure time of about 5 days to reach 500 Mrad(SiO_2) [149]. The radiation exposure was stopped at several irradiation steps, each transistor was immediately measured once per step interval using a switching matrix. No systematic variations due to the measurement order have been observed. Congruently with our previous work [137, 170], the irradiations measurements were performed in the worst bias condition, i.e. "on" (V_{gs} = 0.9 V and V_{ds} = 0 V). The DC characteristics of the devices were tested at room temperature in the linear regime (V_{ds} = 0 V) before and after the irradiation.

6.2 Experimental Results

In the following section, the TID responses of FinFETs are reported by measuring the DC static characteristics and extracting the main parameters: maximum drain current variation ($\Delta I_{on\text{-}lin}$), threshold voltage shift (ΔV_{th}), degradation of the transconductance (Δg_m) and subthreshold swing variation (ΔSS). The $I_{on\text{-}lin}$ current is defined as the drain-to-source current in the linear region ($|V_{ds}| = 50$ mV) when the channel is in strong inversion at $|V_{gs}| = 0.9$ V. The threshold voltage V_{th} is extracted by the linear region (ELR) method [151], as the gate voltage axis intercept of the linear extrapolation of the I_d-V_{gs} characteristics at its maximum first derivative point.

6.2.1 Consistency of Pre-rad Performances

In order to avoid the introduction of unwanted systematic variations, the experimental results on irradiated devices will be shown only for devices irradiated at the same time on the same test chip.

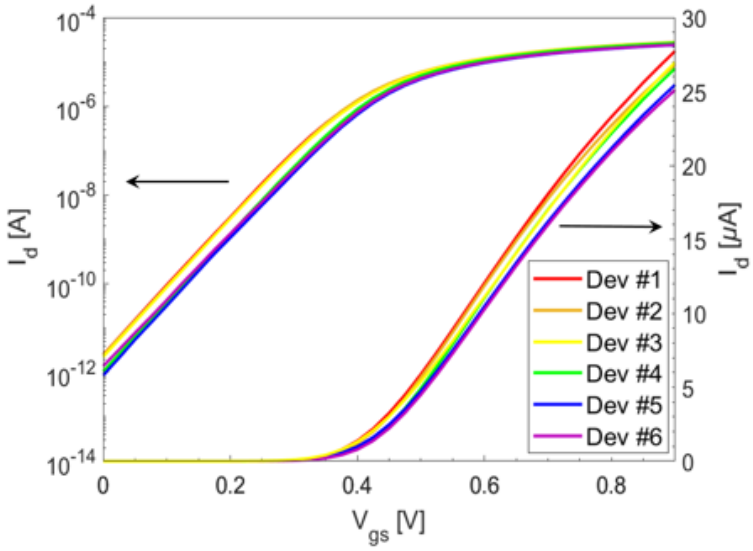


Figure 6.1: I_d-V_{gs} curves in the linear region ($V_{ds} = 50$ mV) of 6 nFinFETs (#1 to #6) with $L = 16$ nm and 2 fins on the same test chip. (From [186])

Figure 6.1 compares the I_d-V_{gs} characteristics at $V_{ds} = 50$ mV for 6 nFinFETs with $L = 16$ nm and 2 fins on the same test chip. The I_d-V_{gs} curves form an almost continuous band, clear differences are still visible in these nominally identical transistors due to the variations induced by process, although the layout has been optimized for matching. The $I_{on\text{-}lin}$, defined as the maximum drain current at $V_{gs} = 0.9$ V and $V_{ds} = 50$ mV, varies clearly between 25 μA

and 28 µA, about 12% variation from maximum to minimum, which reflects the pre-rad sample-to-sample variability. The threshold voltage (V_{th}), off state leakage current ($I_{off\text{-}lin}$), and transconductance (g_m) also vary considerably, while the subthreshold swing (SS) is almost identical in the 6 tested samples, indicating a high quality of the gate dielectric/channel interface.

6.2.2 Consistency of Post-rad Performances

Figure 6.2 plots I_d-V_{gs} curves at V_{ds} = 50 mV for the nFinFET with L = 16 nm and 2 fins. The DC static characteristics are shown at several irradiation steps with devices biased in "on" condition. After 500 Mrad(SiO_2), $I_{on\text{-}lin}$ decreases by about 5% and the $I_{off\text{-}lin}$ increases more than two orders of magnitude. No obvious degradation in the subthreshold slope is visible.

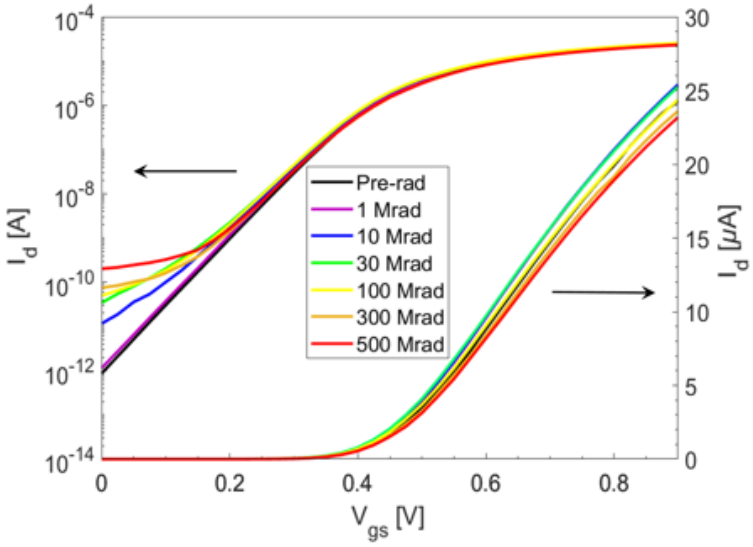


Figure 6.2: I_d-V_{gs} curves in the linear region (V_{ds} = 50 mV) of nFinFETs with L = 16 nm and 2 fins. Devices were irradiated up to 500 Mrad(SiO_2) in the "on"-bias condition. (From [186])

Figure 6.3 compares the I_d-V_{gs} characteristics at V_{ds} = 50 mV for 6 nFinFETs with L = 16 nm and 2 fins irradiated up to 500 Mrad(SiO_2) in "on" bias condition. The 6 transistors belong to the same test chip and were irradiated at the same time. It is evident that sample-to-sample variations after the irradiation become larger than those before the exposure. The $I_{on\text{-}lin}$ decreases a little bit on average and spans between 23 µA and 27 µA, almost 18% variation from maximum to minimum. Interestingly, the DC characteristics after the irradiation do not completely correlate with those before the exposure, for instance, the transistor with the smallest $I_{on\text{-}lin}$ in Figure 6.1 is not the one with the smallest $I_{on\text{-}lin}$ in Figure 6.3.

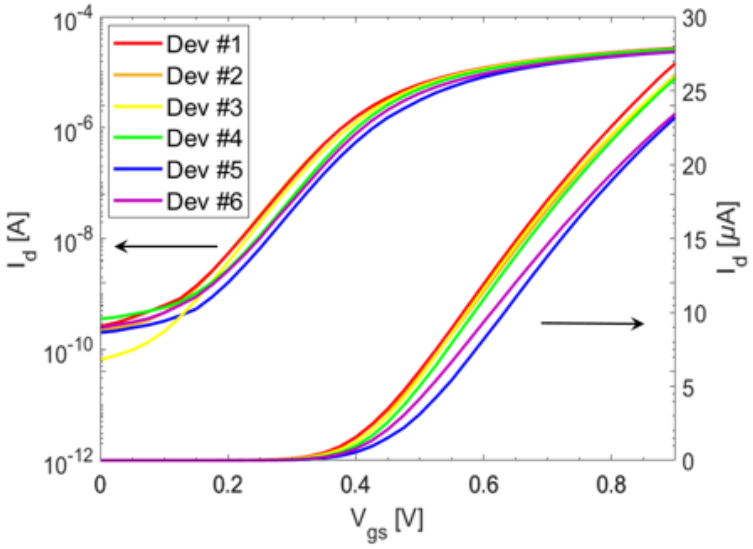
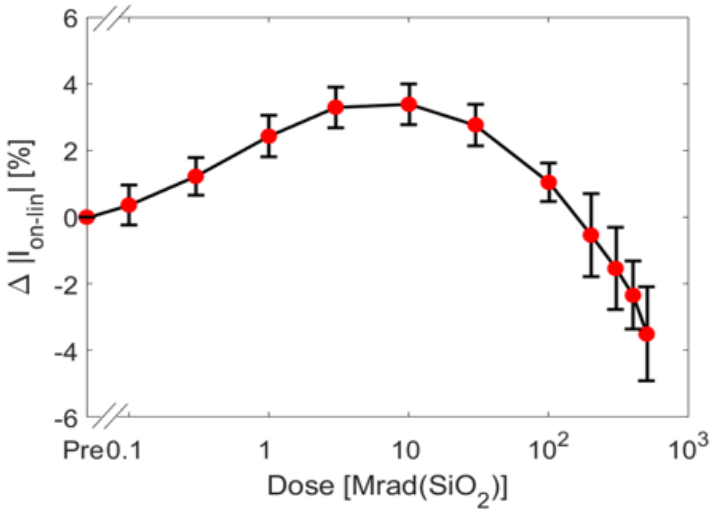


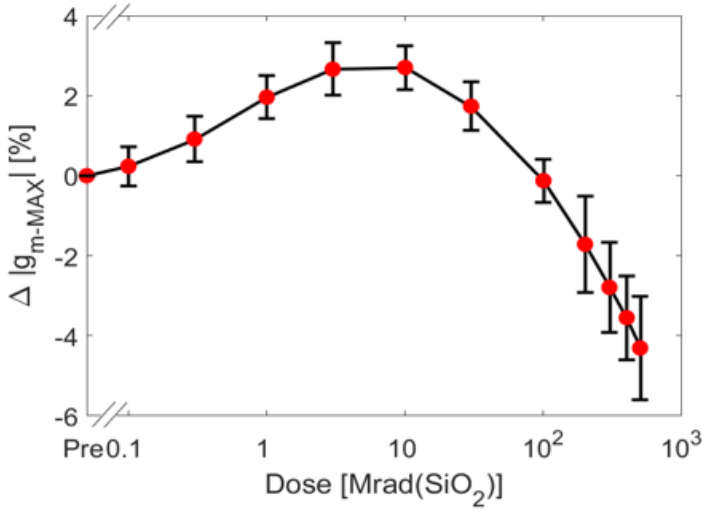
Figure 6.3: I_d-V_{gs} curves in the linear region (V_{ds} = 50 mV) of 6 nFinFETs (#1 to #6) with L = 16 nm and 2 fins on the same tested chip after exposure to a total dose of 500 Mrad(SiO_2) in the "on"-bias condition. (From [186])

6.2.3 Sample-to-Sample Variability

Figure 6.4 shows the radiation-induced average degradation of the main DC static characteristics of the DUTs: (a) maximum drain current $\Delta I_{on\text{-}lin}$ and (b) maximum transconductance $\Delta g_{m\text{-}MAX}$, as a function of the cumulate doses. These values are for 6 tested nFinFETs on the same test chip with L = 16 nm and 2 fins, irradiated with X-rays up to 500 Mrad(SiO_2) at the same time in "on" bias condition.



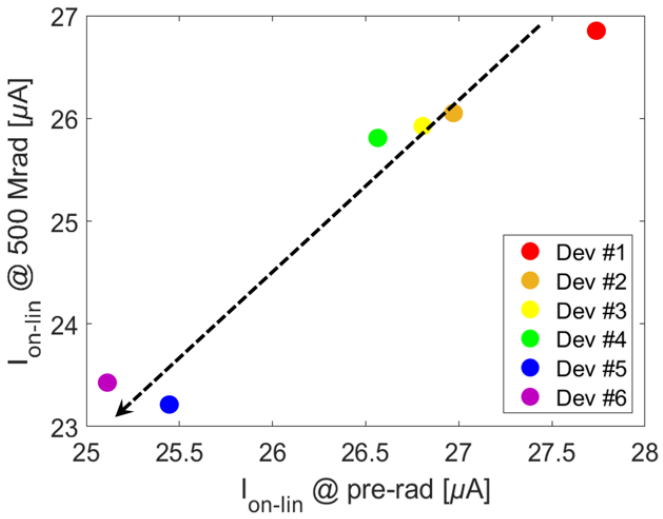
(a)



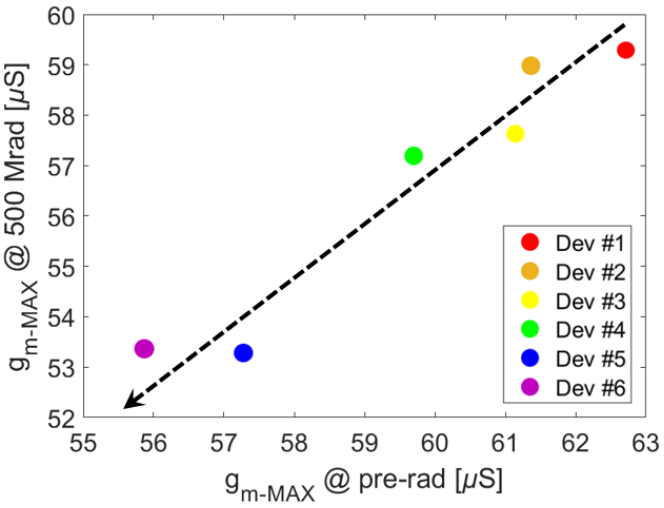
(b)

Figure 6.4: Average degradation of (a) maximum drain current $\Delta I_{on\text{-}lin}$, and (b) maximum transconductance $\Delta g_{m\text{-}MAX}$, as a function of dose across 6 tested nFinFETs belonging to a same chip. Error bars represent one standard deviation on the tested population. (From [186])

Error bars in the figure represent one standard deviation on the tested population. Up to 100 Mrad(SiO_2) of total dose, the standard deviations in the two figures (a) and (b) do not change appreciably, and are stable at about 0.6% and 0.6%, respectively. However, when the total dose exceeds 100 Mrad(SiO_2), the standard deviations of $\Delta I_{on\text{-}lin}$ and $\Delta g_{m\text{-}MAX}$ increase considerably by a factor of two, up to about 1.2% and 1.2%, respectively.



(a)



(b)

Figure 6.5: Scatter plot of (a) maximum drain current $I_{on\text{-}lin}$, and (b) maximum transconductance $g_{m\text{-}MAX}$ of 6 nFinFETs (#1 to #6) on the same test chip before irradiation and after 500 Mrad(SiO_2). (From [186])

Even robust designs that rely on matching between transistors, rather than on the absolute value of the electrical parameters, may fail due to this increase. It must be noted that all the tested transistors were irradiated on the same bias condition and at the same time. Applications where MOSFETs are not biased in the same way (e.g. on state, off state, diode state, etc.) will likely experience even greater variations. In addition, comparing Figure 5.4 (a) and Figure 5.4(b), the average degradation and standard deviation of $g_{m\text{-}MAX}$ is very similar to $\Delta I_{on\text{-}lin}$, indicating again that the decrease of $I_{on\text{-}lin}$ is mostly dominated by the degradation of g_m.

Figure 6.5 shows a scatter plot of the maximum drain current $I_{on\text{-}lin}$ and maximum transconductance $g_{m\text{-}MAX}$ of 6 nFinFETs on the same test chip before irradiation and after 500 Mrad(SiO_2). There is a good correlation between pre-rad and post-rad values, indicating that the larger the initial drain current, the larger current after the irradiation, the same is true for the transconductance. This analysis suggests that the sample-to-sample variability of irradiated nFinFETs is correlated to the initial process-dependent one.

6.3 Discussion

The degradation of 16 nm bulk nFinFETs irradiated to ultra-high doses is dominated by the trapped charge buildup in STI. At doses up to 10 Mrad(SiO_2), the dominant degradation mechanism is the trapping of positive charges in the STI. At ultra-high doses ($>$ 10 Mrad(SiO_2)), the effects of interface traps at the

corner between the STI and the gate oxide and along the interface of STI/Si can become more significant [137].

The main sources of process-related variability in FinFETs include random dopant fluctuations, surface orientation, line edge roughness, and polysilicon grain [178, 179, 181]. All these factors may have an impact on the TID degradation, for instance, due to a different placement of polysilicon grains or different surface orientation, changes in the electric field in the STI directly affect the amount of charge trapping and interface state generation.

Variations in the number and distribution of dopant atoms in the silicon channel which were earlier identified as the most likely source of the observed sample-to-sample variability in CMOS transistors, can also give rise to changes in the TID degradation. Because the number of available carriers in the channel of transistors is larger around than on top of dopant atoms (red dots in Figure 6.6) [185], the conduction occurs preferentially around the position of the dopant atoms, leading to typical non-uniformity of the conduction in the channel. Thinner arrows correspond to smaller currents in the Figure 6.6. Depending on the position of these "preferential conductive path" in the channel, the TID degradation may vary. For instance, net positive charge and the interface traps in the STI closer to the more conductive parts of the transistors will induce a larger degradation. Due to random statistical fluctuations, there are more dopants in the center of the device channel relative to the edge, which might increase sensitivity to TID [182]

Figure 6.6 shows the evolution of the TID degradation mechanisms related to the STI for nFinFETs. At high doses ($<$10 Mrad(SiO_2)), the positive trapped charge in the STI dominates the TID response by inverting the lateral bulk regions, generating deep drain-to-source parasitic paths, which does not affect the effective channel height. Therefore, the TID degradation is barely affected by the random dopant fluctuations and the amount of variability among the tested transistors is constant. At ultra-high doses ($>$ 10 Mrad(SiO_2)), the increase of the drain leakage current suggests a continuous buildup of positive charge in the deep oxide regions of the STI. However, the rebound of the g_m at 10 Mrad(SiO_2) indicates a large generation of interface traps at the corner between the STI and the gate oxide, which can deplete the lateral regions and substantially reduce the effective channel height. As a result, the random dopant fluctuations will begin to affect the TID effects, increasing the sample-to-sample variability. In addition, as the effective channel height decreases, the interface traps will move closer to the center of the lateral channel, inducing a larger impact on TID degradation.

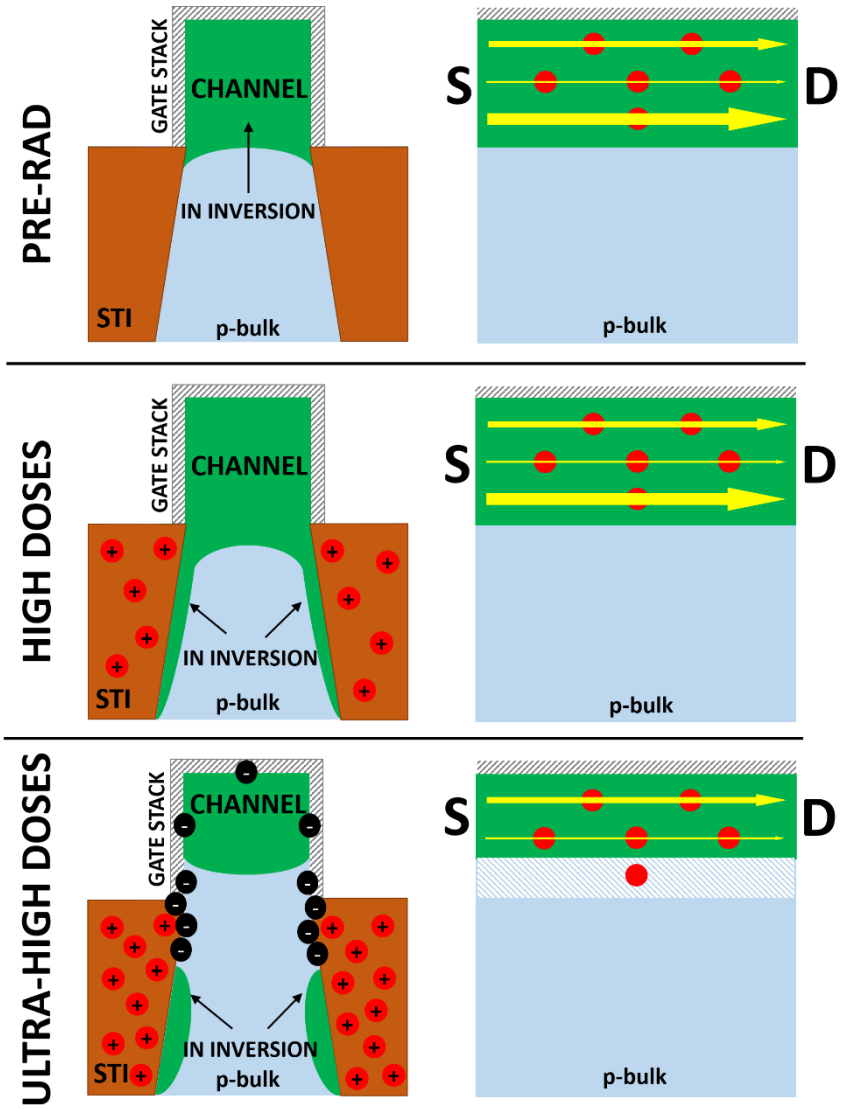


Figure 6.6: The degradation mechanism in nFinFETs is shown schematically through a vertical cut-plane normal. TID-induced effects are illustrated when devices are biased in inversion (V_{gs} = 0.9 V) at high (~ 1-10 Mrad(SiO_2)) and ultra-high doses (> 10 Mrad(SiO_2)). The green colored regions are inverted regions of the Si bulk, Positive trapped charges are indicated with "+", "−" indicated the interface traps that are negatively charged, dopant atoms are indicated with red dots. (From [186])

Figure 6.4 illustrates the standard deviations of $\Delta I_{on\text{-}lin}$ and $\Delta g_{m\text{-}MAX}$ begin to increase significantly after 100 Mrad(SiO_2) instead of 10 Mrad(SiO_2). It is possible that the amount of interface traps at the corner between the STI and the gate oxide is not large enough and the reduction of the effective channel height is slight, so that the random dopant fluctuations barely affect the TID effects, and only the process-induced variability is visible for doses lower than 100 Mrad(SiO_2).

6.4 Conclusions

In this chapter, the sample-to-sample variability as a function of the total dose in a 16 nm bulk nFinFETs technology was investigated, focusing on minimum size transistors. At doses smaller than 100 Mrad(SiO_2), the TID degradation does not show any clear increase in sample-to-sample variability due to the exposure. Whereas at ultra-high doses up to 100 Mrad(SiO_2), a significant increase in sample-to-sample variability occurs, which is also correlated to the initial process-dependent variability. The phenomenon is likely due to the impact of random dopant fluctuations on total ionizing dose effects.

Chapter 7

TID Effects in Si Nanowire GAA-FETs at Ultra-High Doses

In this chapter, the total-ionizing-dose (TID) effects are investigated in a highly-scaled Gate-All-Around FET technology using Si nano-wire channels of 8 nm diameter. n- and p-FETs are irradiated up to 300 Mrad(SiO_2) and annealed at room temperature. TID effects are negligible up to 10 Mrad(SiO_2). At ultra-high doses the TID degradation depends on the irradiation bias condition, with more severe effects observed in longer channel devices. The worst-case irradiation condition is when positive bias is applied to the gate. Threshold-voltage shifts are caused by H^+-driven generation of interface traps at the oxide/channel interface. In contrast, FETs irradiated under negative gate bias are dominated by transconductance loss and increases of low-frequency noise, suggesting activation of border traps. Enhanced off-state leakage current is observed in n-FETs due to charge trapping in shallow-trench isolation, and in p-FETs due to trap-assisted recombination at STI sidewalls and / or spacer dielectrics at drain/bulk junctions.

In previous works, TID effects at ultra-high doses have been investigated in planar and FinFET Si-based technologies [101-105, 113, 121-123, 137-139]. Studies at 1 Grad(SiO_2) on 65 nm MOSFETs [101, 102, 105, 139], on 28 nm MOSFETs [113, 121-123] and 16 nm FinFETs [137, 138, 170] have revealed two main dominating TID mechanisms. The first phenomenon is related to charge buildup in shallow trench isolation (STI) oxide and its interfaces [101, 104, 113, 121-123]. STI trapped charge increases off-state leakage current in n-channel FETs and induces parametric drifts in narrow n and p-channel FETs [101, 104]. The second effect, called radiation-induced short-channel effects (RISCE) [101], is related to charge buildup in spacer oxides and overlying silicon nitride layers above the lightly doped drain extensions [101, 102, 105, 139]. RISCE degrades short channel devices by increasing parasitic series resistance and reducing the drive current [101, 102, 105]. Sub-micron technology nodes may employ halo implantations to reduce drain-induced barrier lowering in short transistors [122,

140, 188]. Recent works [122, 123, 137, 138, 170] have reported that the halo implantations may fortuitously improve the TID tolerance of the shortest devices, as a consequence of the increased bulk doping caused by overlapping halos.

With advancing technology nodes, CMOS transistors are increasingly built with new layouts and materials [142-145, 172, 189-195]. Gate-All-Around (GAA) nano-wire (NW) FETs have been proposed as promising candidates for sub-7 nm technological nodes [143, 191-194]. The layouts of GAA FETs allow high electrostatic control of the channel with a significant reduction of short-channel effects [191]. Recent studies have pointed out the high TID tolerance of Si- and III-V semiconductor-based GAA devices when irradiated at doses up to 10 Mrad(SiO_2) [143, 149, 191-195]. Si-based GAA FETs similar to the ones used in this work have been tested up to 1 Mrad(SiO_2); GAA FETs exhibited an almost negligible threshold voltage shift (<20 mV) and slight on-current degradation (<5%) [194]. The high TID tolerance of GAA FETs is related to the highly effective gate control and limited charge buildup in ultra-thin gate dielectrics [143, 191-195]. Moreover, GAA FETs are generally insensitive to TID effects related to the charge trapping in the shallow trench isolation (STI) [194]. However, the TID responses of GAA FETs at ultra-high doses have not yet been investigated.

In this chapter, TID mechanisms are explored at doses up to 300 Mrad(SiO_2) in a development-stage GAA nano-wire FET technology through DC and low frequency noise measurements. Irradiated FETs show TID degradation that depends on channel type, bias condition, and channel length. Worst-case TID-induced degradation is found in p-channel devices with long channels; n-channel devices exhibit the most favorable TID tolerance.

The work presented in this chapter was supported in part by the Air Force Office of Sponsored Research through its Hi-REV program, in a collaboration with: University of Vanderbilt, Nashville, USA; University of Bergamo, Bergamo, Italy; and IMEC, Leuven, Belgium.

Most of the results and figures presented in this chapter have been published and/or submitted in the following peer-reviewed publications:

- [187] S. Bonaldo, M. Gorchichko, E. X. Zhang, T. Ma, S. Mattiazzo, M. Bagatin, A. paccagnella, S. Gerardin, R. D. Schrimpf, R. A. Reed, D. Linten, J. Mitard and D. M. Fleetwood, "TID effects in highly scaled gate-all-around Si nanowire CMOS transistors irradiated to ultra-high doses," *IEEE Transactions on Nuclear Science*. (Accepted for RADECS 2021 conference, Austria, Vienna, and currently submitted for publication in IEEE Transactions on Nuclear Science.)

Moreover, the results in this chapter have been presented at the following international conference:

- Radiation Effects on Components and Systems - RADECS 2021, online event, 13th - 17th September 2021, poster presentation about "TID effects

in highly scaled gate-all-around Si nanowire CMOS transistors irradiated to ultra-high doses".

7.1 Devices and Experiments

7.1.1 Devices Description

The GAA FETs under test were fabricated with horizontal silicon nano-wires (NWs) by IMEC, Belgium [191]. Each transistor has four fins, and each fin contains two vertically stacked horizontal Si NWs with a diameter of 8 nm. Transistors with different channel lengths are available. Short devices having channel lengths of L = 26-34 nm are labeled as L = 30 nm. p-channel devices also are available with long channels, L = 250 nm and 1 µm. Figure 7.1(a) shows cross-sectional images of the GAA NW FETs under test. The gate stack is composed of 1.8 nm of HfO_2 over a thin layer SiO_2 (see Figure 7.1(b)). Threshold voltage matching of nFET and pFET devices is obtained through a dual-work-function metal integration technique [191].

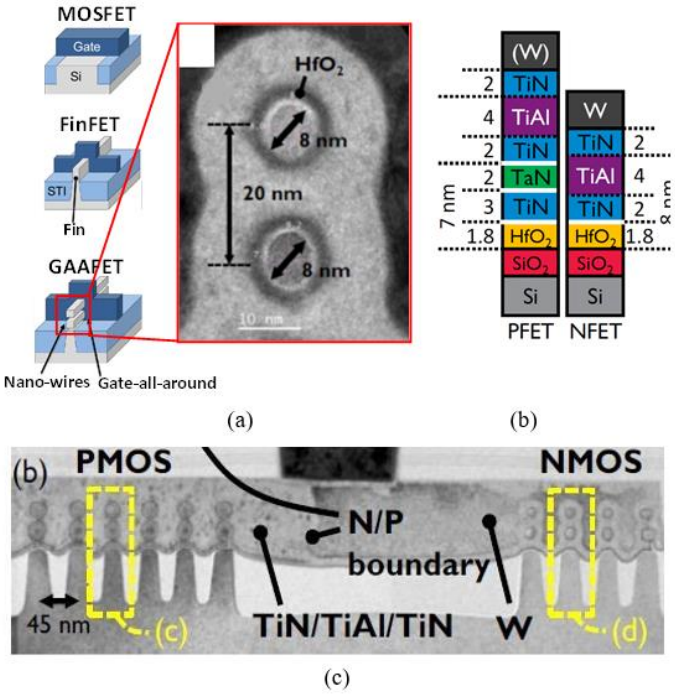


Figure 7.1: The devices under test are GAA nano-wire FETs. (a) Cross-sectional TEM image of the channel region composed by two nano-wires. (b) The structure of gate stack. (c) Cross-sectional TEM image of GAA-based CMOS circuit with a nFET and a pFET. (From [187])

7.1.2 Irradiation Conditions and Measurements Details

The irradiation was conducted using a 10-keV X-ray irradiator at a dose rate of 3.8 Mrad(SiO_2)/h [149]. The total exposure time was ~79 hours (~3.5 days) to reach 300 Mrad(SiO_2). All doses and rates are referred to equilibrium doses in SiO_2 for consistency in calibration and to facilitate comparison with other work [145]. Devices were tested with wafer probes positioned to prevent shadowing of X-rays (see Figure 7.2). After exposure, devices were annealed at room temperature for 24 hours.

During the irradiation and annealing, each device was biased in one of the bias conditions listed in Table 7.1: *GND*, $GND+V_d$, $+V_g$, and $-V_g$, showing the bias configurations applied at the gate and drain terminals during the exposure and annealing, the bulk and source terminals of both n- and p-FETs were always biased at 0 V. Some bias conditions are not typically used in nominal working condition, i.e. $-V_g$ for nFETs and $+V_g$ for pFETs, but they are useful to understand the TID degradation phenomena.

At least two devices of each type were evaluated for all experimental conditions with DC parameter degradations that typically vary by less than ±5%. Typical results are shown below.

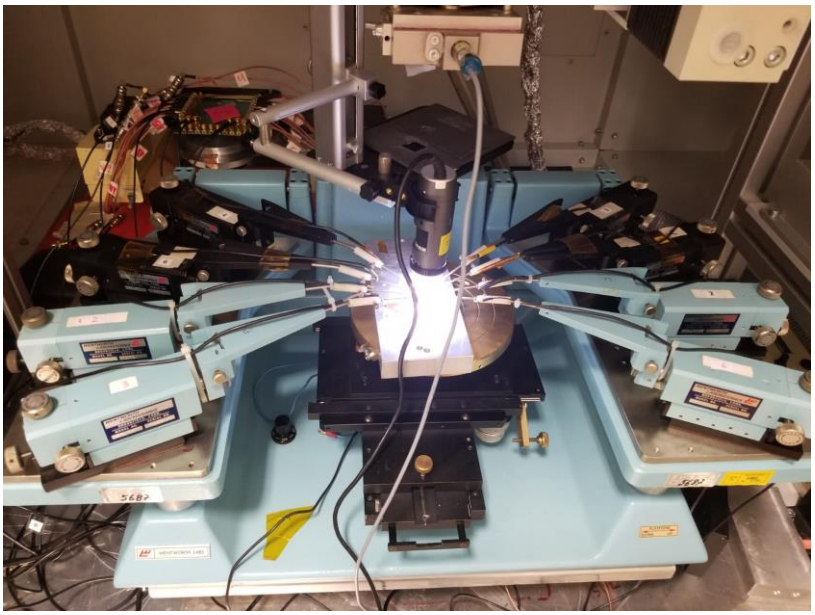


Figure 7.2: Photo of the manual probe station used for the irradiation test.

Table 7.1: Bias conditions during irradiation and annealing.*

Bias conditions	nFETs		pFETs	
	V_g [V]	V_d [V]	V_g [V]	V_d [V]
GND	0	0	0	0
GND+V_d	0	+0.8	0	−0.8
+V_g	+0.8	0	+0.8	0
−V_g	−0.8	0	−0.8	0

*Bulk and source terminals of n- and p-FETs are always biased at 0 V.

Transistor DC static responses were measured with a semiconductor parameter analyzer at room temperature before exposure and at several irradiation steps. The threshold voltage V_{th} is calculated as $V_{gs\text{-}int} - V_{ds}/2$, where $V_{gs\text{-}int}$ is extracted in the linear mode of device response ($V_{ds} = 50$ mV) as the gate-voltage axis intercept of the linear extrapolation of the I_d-V_{gs} curve at the point of maximum first derivative. The low-frequency noise was measured between 1 Hz and 1 kHz in the linear mode of device response ($V_{ds} = 50$ mV) at several gate voltages, $V_{gt} = V_{gs} - V_{th}$ [150].

7.1.3 Evaluation of Electrical Stress Effects

Irradiations up to 300 Mrad(SiO_2) requires about 79 hours of exposure with biased transistors in one of the bias conditions shown in Table 1. In order to distinguish the degradation induced by electrical stress from the one induced by radiation, GAA FETs were tested under bias conditions of Table 1 for the same amount of time required for devices to be irradiated up to 300 Mrad(SiO_2), ~79 hours. Both types of GAA NW FETs show excellent stability, with threshold voltage shifts ΔV_{th} of less than 2 mV for each examined bias condition. The worst conditions were found when positive or negative bias were applied to the gate terminal, as shown in Figure 7.3. After ~79 hours, nFETs biased in "+V_g" condition show a decrease of the maximum drain current of 1%, while pFETs biased in "−V_g" show a decrease of the maximum drain current of 3%. These stress-induced effects are almost negligible compared to the radiation-induced effects shown in the next subsections.

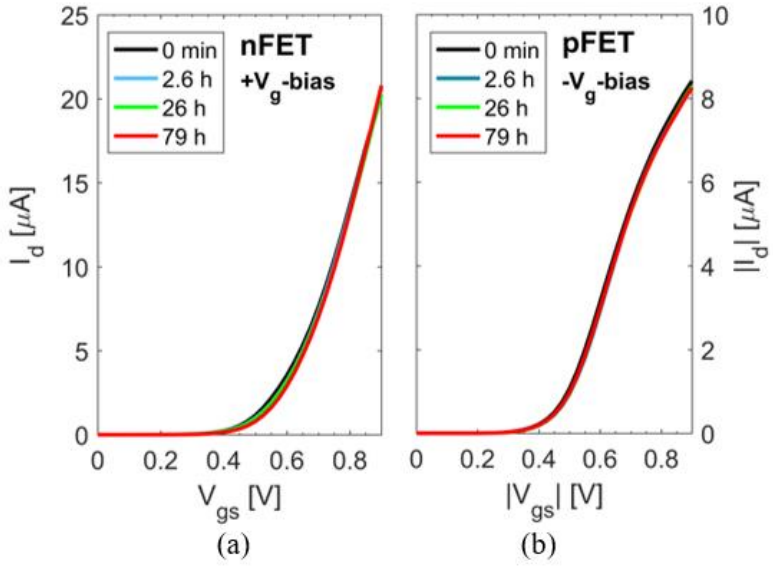


Figure 7.3: Electrical stress-induced degradation of $|I_d|$-$|V_{gs}|$ curves in the linear regime ($|V_{ds}| = 50$ mV) for GAA devices with L=30 nm. (a) nFET and (b) pFET were respectively biased in the "+V_g" and "−V_g" bias conditions for ~79 hours, in order to evaluate the degradation induced by the electrical stress without any X-ray exposure. (From [187])

7.2 DC Static Characterization

7.2.1 N-Channel GAA-FETs

Figure 7.4 shows DC characteristics in the linear regime ($V_{ds} = 50$ mV) for nFETs with minimum channel length, $L = 30$ nm. The nFETs were irradiated and annealed in the "$+V_g$" and "*GND*" bias conditions. The worst TID-degradation is for the "$+V_g$"-biased nFET, which exhibits a positive threshold-voltage shift, increase in off-state leakage current, and loss of transconductance. The subthreshold slope *SS* increases by 15 mV/dec in the "$+V_g$"-biased nFET after 300 Mrad(SiO_2). 24 hours annealing at high temperature causes a slight recovery of DC performances. The "*GND*"-biased nFET shows outstanding tolerance to ultra-high doses, with variations of less than 3% in the drain current and $\Delta SS < 2$ mV/dec after 300 Mrad(SiO_2).

The influence of bias conditions on the TID sensitivity has been tested for all the bias-configuration reported in Table 7.1. Figure 7.5 shows the degradation of: (a) the drain current $I_{on\text{-}lin}$, (b) the threshold voltage V_{th}, and (c) the maximum transconductance $g_{m\text{-}MAX}$. The $I_{on\text{-}lin}$ is defined as the maximum drain current at $|V_{gs}| = 0.9$ V and $|V_{ds}| = 50$ mV.

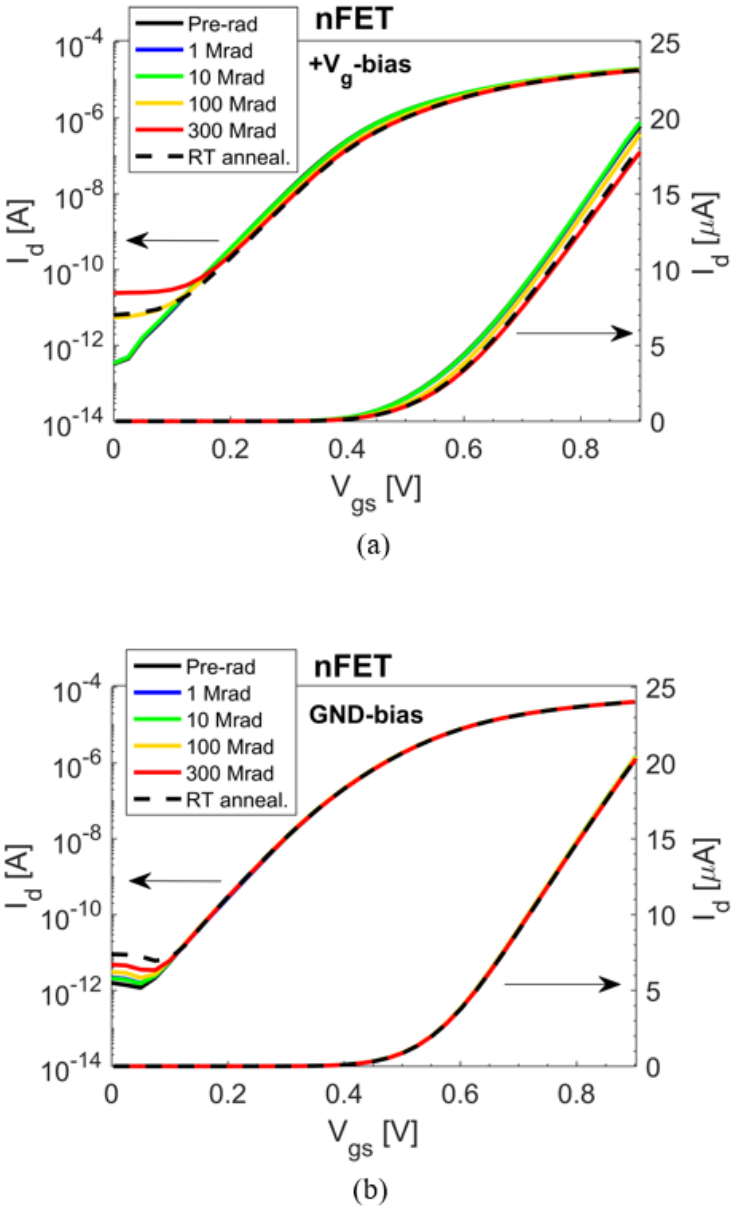
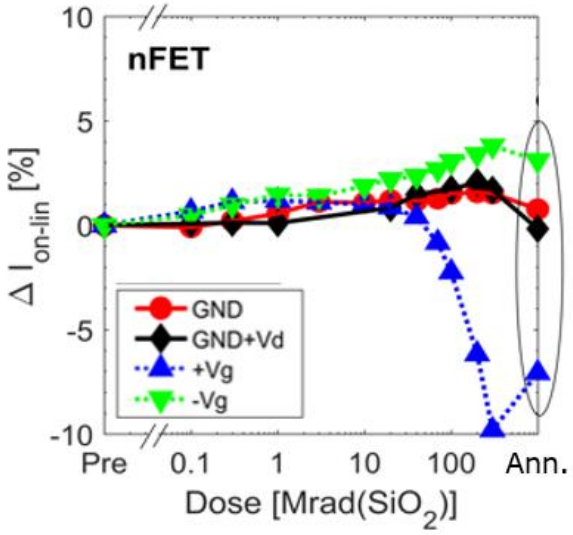


Figure 7.4: Radiation-induced degradation of I_d-V_g curves in the linear regime (V_{ds} = 50 mV) for nFET with L = 30 nm. The devices were irradiated and annealed in (a) "+V_g"-bias condition and (b) "GND"-bias condition. (From [187])

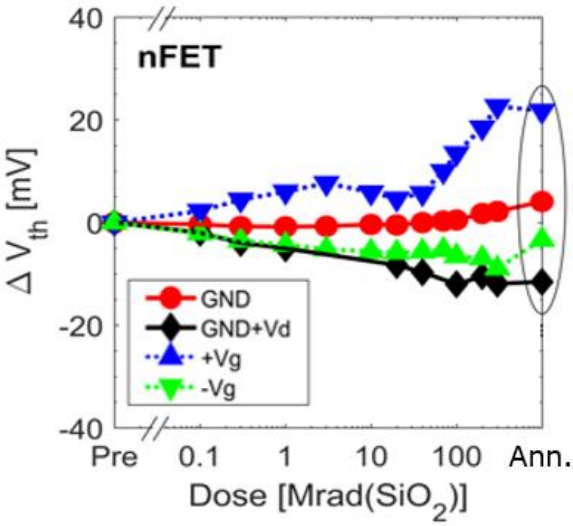
As shown in Figure 3(a), nFETs irradiated under grounded bias conditions or in the "$-V_g$"-bias condition have the highest TID tolerance with less than 4% of $I_{on\text{-}lin}$ variation. In contrast, "$+V_g$"-biased nFETs show noticeable TID-induced effects starting from 30 Mrad(SiO_2). At 300 Mrad(SiO_2), the negative V_{th} shift of 25 mV and the 8% g_m degradation cause an overall $I_{on\text{-}lin}$ decrease of about 10%, confirming the relatively high tolerance of the GAA nFETs, compared to previous planar CMOS technologies [101, 102, 113, 123].

The variation of the TID sensitivity between transistors irradiated under different bias conditions is caused by the magnitude and the direction of electric

field applied during the irradiation [169, 197-199]. The highest tolerance of "*GND*"- and "$GND+V_d$"-biased nFETs is caused by the reduced charge yield when low electric fields are applied to the gate oxides [19],[154]. In contrast, high potentials at the gate terminal enhance the charge yield [154]. The "$+V_g$" and "$-V_g$" biases lead to opposite degradations of $I_{on\text{-}lin}$. The "$+V_g$"-irradiated nFETs are characterized by positive shifts in threshold voltage, subthreshold swing, and g_m degradation. The TID-degradation is most likely due to the buildup of interface traps induced by the electric field-driven drift of H^+ ions to the SiO_2/Si interface [86, 96, 97]. We now discuss the pMOS transistor response.



(a)



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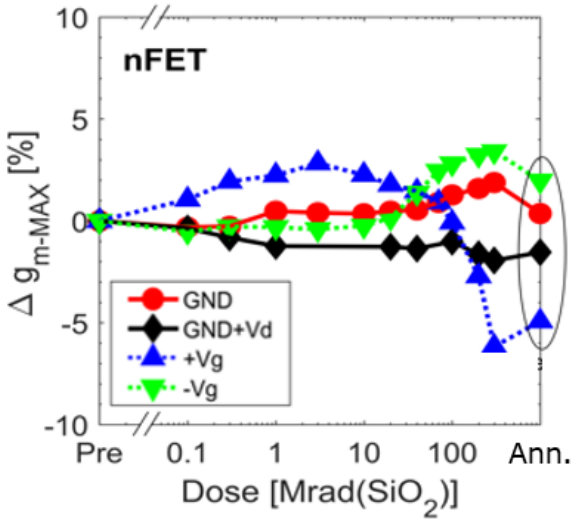


(c)

Figure 7.5: Performance degradation of nFETs as a function of accumulated dose: (a) maximum drain current $\Delta I_{on\text{-}lin}$, (b) threshold voltage ΔV_{th}, and (c) maximum transconductance $\Delta g_{m\text{-}MAX}$. Transistors were irradiated up to 300Mrad(SiO_2) and then annealed at several bias conditions. Measurements were carried out at room temperature in the linear region (V_{ds} = 50 mV). (From [187])

7.2.2 P-Channel GAA-FETs

Figure 7.6 shows the DC characteristics in the linear regime ($V_{ds} = -50$ mV) for pFETs with $L = 30$ nm. P-channel FETs irradiated in "$-V_g$" and "*GND*" bias conditions exhibit increases of leakage current, threshold voltage shifts, and losses of transconductance. After 100 Mrad(SiO_2), the maximum drain current of "$-V_g$"-biased pFETs decreases by 28%, the drain current of "*GND*"-biased pFETs decreases similarly. 24 hours of room temperature annealing induces a slight recovery in transistor performance. For all bias conditions, the subthreshold swing variation is negligible (< 3 mV/dec), except for "$+V_g$"-biased devices, which exhibit ΔSS = 14 mV/dec after 300 Mrad(SiO_2).

The TID-induced shifts of DC parameters of pFETs irradiated under different bias conditions are shown in Figure 7.7: (a) the drain current $I_{on\text{-}lin}$, (b) the threshold voltage V_{th}, and (c) the maximum transconductance $g_{m\text{-}MAX}$. The $I_{on\text{-}lin}$ of pFETs starts to degrade noticeably after 10 Mrad(SiO_2), due to negative V_{th} shifts combined with $g_{m\text{-}MAX}$ degradation and/or increases of series resistance. The $I_{on\text{-}lin}$ degradation is almost insensitive to the applied bias. However, Figure 7.7(b) and (c) show that the nature of the TID mechanisms differ: "*GND*"-, "$GND + V_d$"-, and "$-V_g$"-biased pFETs are dominated by the degradation of transconductance, while "$+V_g$"-biased pFETs are dominated by increases of threshold voltage.

Similar to nFETs, the TID sensitivity of transistors is influenced by the transport of H^+ [86, 96, 97, 101]. Both n- and p-FETs exhibit the worst V_{th} shift and *SS* increase when irradiated in "$+V_g$", in agreement with the electric field-driven drift of H^+ toward the oxide/channel interface, which activates interface traps at the gate Si/SiO_2 interface. The transconductance degradation in grounded and "−Vg"-bias conditions are due most likely to charge trapping in STI or spacer oxides, which contribute to decreased numbers of carriers in access regions [101, 102, 105, 123, 138].

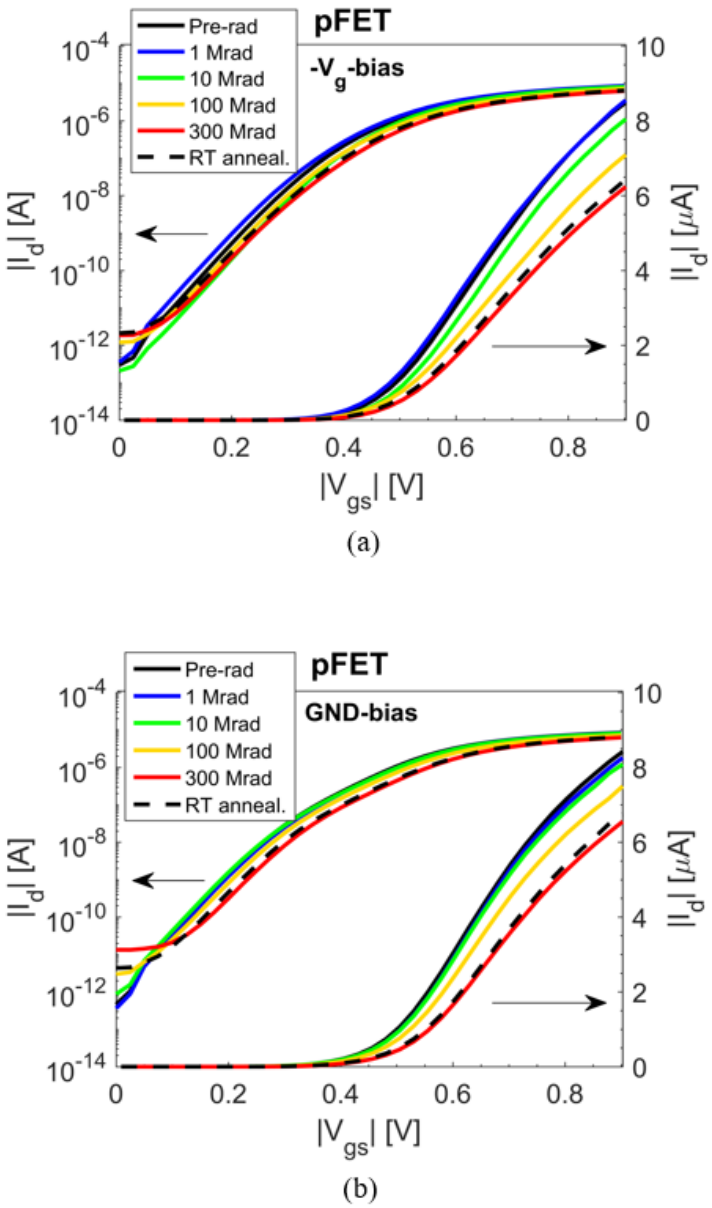
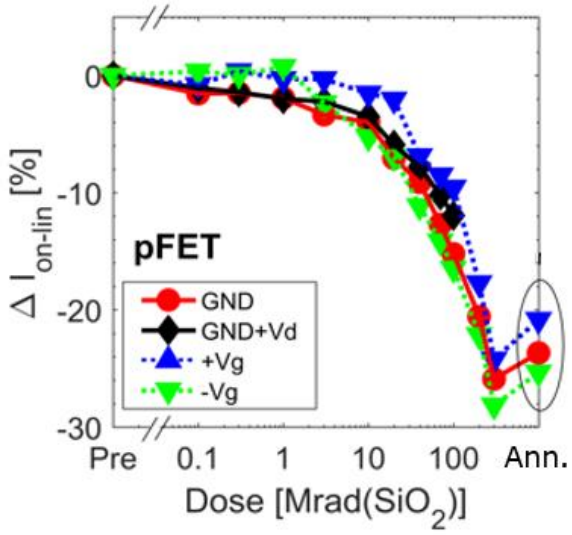
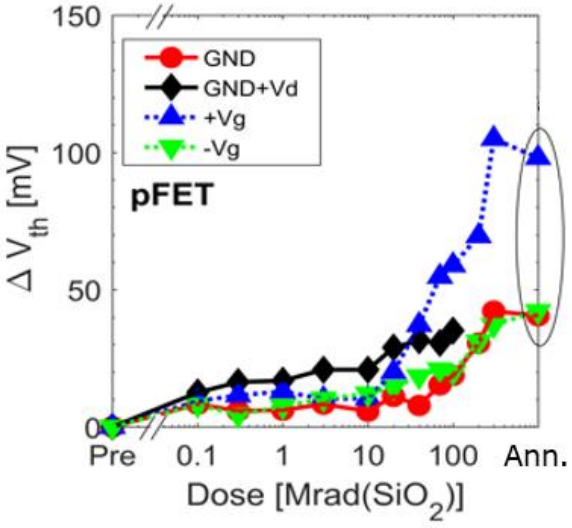


Figure 7.6: Radiation-induced degradation of $|I_d|$-$|V_g|$ curves in the linear regime (V_{ds} = −50 mV) for pFET with L = 30 nm. The devices were irradiated and annealed in (a) "−V_g"-bias condition and (b) "GND"-bias condition. (From [187])

Comparing Figure 7.4 and 7.6, it is clear that nFETs exhibit higher TID tolerance than pFETs. This higher radiation tolerance of nFETs occurs most likely because: (1) different doping levels of the nano-wire can vary the sensitivity of devices to TID effects [107], and (2) in nFETs, interface traps can capture negative charge, compensating effects of the positive charge trapped in gate and STI dielectrics [123, 137,138].



(a)



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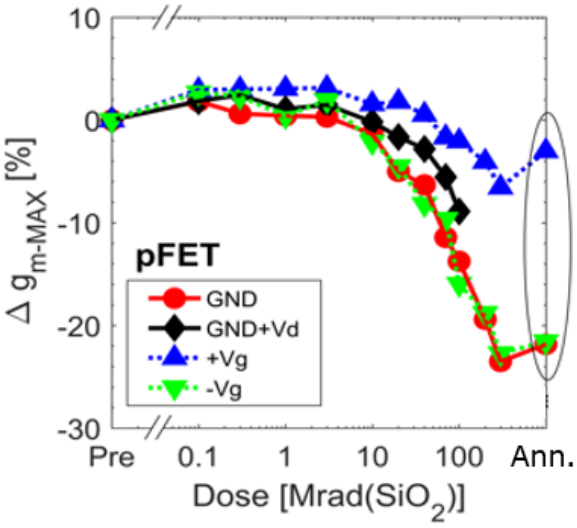
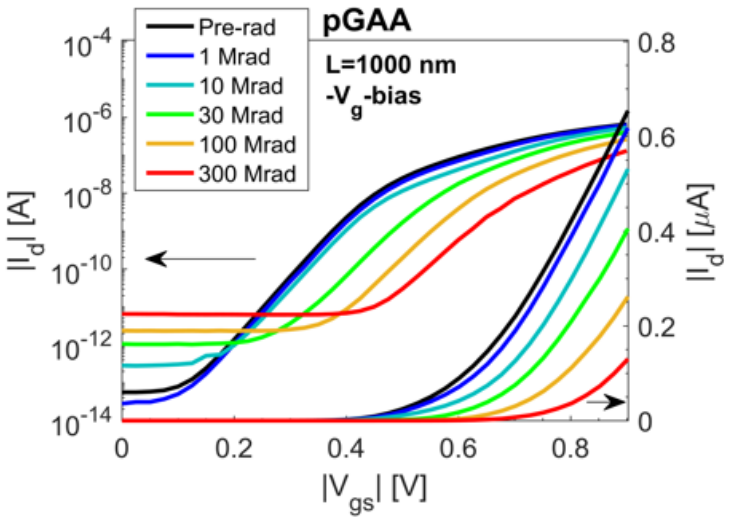


(c)

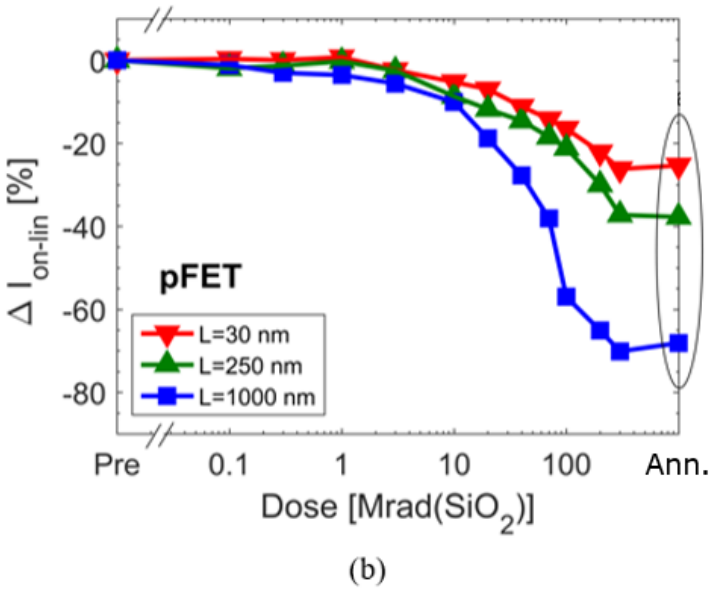
Figure 7.7: Performance degradation of pFETs as a function of accumulated dose: (a) maximum drain current $\Delta I_{on\text{-}lin}$, (b) threshold voltage ΔV_{th}, and (c) maximum transconductance $\Delta g_{m\text{-}MAX}$. Transistors were irradiated up to 300Mrad(SiO_2) and then annealed at several bias conditions. Measurements were carried out at room temperature in the linear region ($V_{ds} = -50$ mV). (From [187])

7.2.3 Channel Length Dependence of pFETs

Figure 7.8(a) shows $|I_d|$-$|V_g|$ characteristics for the longest pFETs, with channel length of 1μm, irradiated in the "$-V_g$"-bias condition. The TID degradation is severe in long channel transistors; the threshold voltage shift is ~140 mV after 300 Mrad(SiO_2).



(a)



(b)

Figure 7.8: (a) Radiation-induced degradation of $|I_d|$-$|V_g|$ curves in the linear regime ($V_{ds} = -50$ mV) for pFET with long channel $L = 1000$ nm. The device was irradiated in "$-V_g$"-bias condition. (b) Comparison of maximum drain current $\Delta I_{on\text{-}lin}$ degradations of pFETs with different channel lengths. All devices were irradiated up to 300 Mrad(SiO_2) and then annealed in "$-V_g$"-bias condition. (From [187])

Figure 7.8(b) compares the TID-induced $I_{on\text{-}lin}$ degradation for three devices having different channel lengths: 30 nm, 250 nm, and 1 µm. The TID sensitivity scales with channel length; the shortest pFETs exhibit the highest TID tolerance. At 300 Mrad(SiO_2), the shortest devices (red line) exhibit a decrease in $\Delta I_{on\text{-}lin}$ of 28%, in contrast to the 70% decrease of the longest devices (blue line). The channel-length-dependent increase in V_{th} shifts for longer-channel devices may result from a decrease in electrostatic gate control with increasing length [143, 189], consistent with the results of Riffaud, et al. [198].

7.2.4 Off-Leakage drain current

Figure 7.9 shows the off-state leakage current $I_{off\text{-}lin}$ flowing through the drain terminal when $V_{gs} = 0$ V and $V_{ds} = 50$ mV, consistent with the results of Figure 7.4. The $I_{off\text{-}lin}$ in Figure 7.9(a) for nFETs is a drain-to-source current. Historically, the increase of the drain-to-source leakage current in planar MOS technologies is related to positive charge buildup in the STI oxides [101, 113, 121, 123]. In GAA FETs, even if the layout is optimized for enhanced control of the gate on the Si nano-wire channels [191], the Si-bulk region below the Si nano-wires may still be sensitive to STI-related effects. Positive charges in STI may slightly invert this p-doped region, generating parasitic lateral channels and increasing the $I_{off\text{-}lin}$ of the transistor.

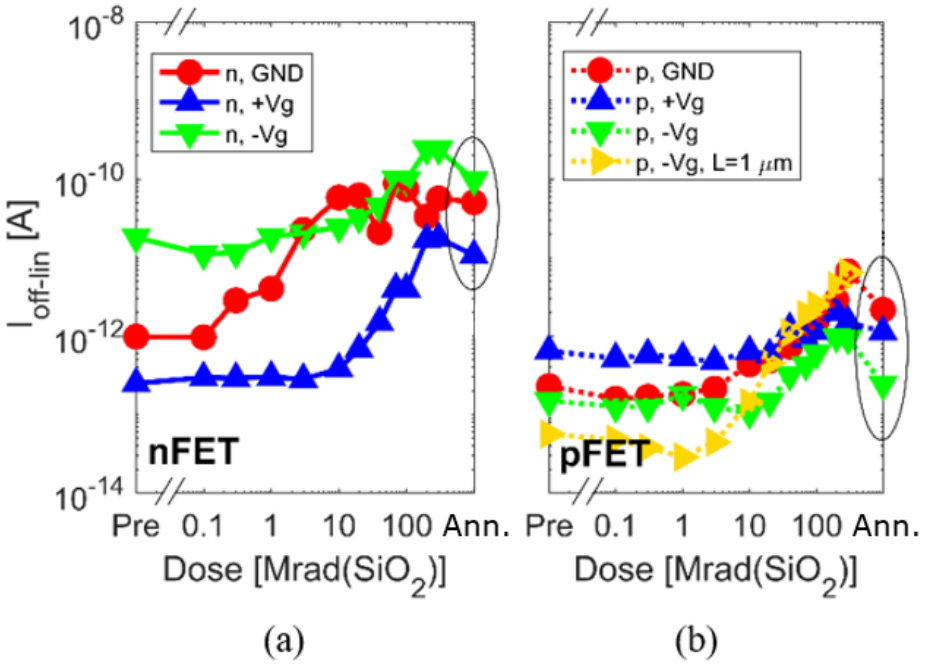


Figure 7.9: Increase of drain leakage current $|I_{off\text{-}lin}|$ in the linear regime as functions of dose and applied bias; $|V_{ds}| = 50$ mV for (a) nFETs and (b) pFETs. The channel length is 30 nm, except for the $L = 1$ µm (yellow) curve in (b). (From [187])

Interestingly, p-channel GAA FETs also show an increase of off-leakage current in Figure 7.9(b). An equal and opposite increase of $I_{off\text{-}lin}$ was measured at the bulk terminal, indicating a drain-to-bulk leakage. The drain-to-bulk $I_{off\text{-}lin}$ is most likely induced by trap-assisted recombination current inside the depletion regions [152, 200, 201]. TID activates traps at STI sidewalls and/or spacer dielectrics adjacent to the pn drain/bulk junctions, which function as electron-hole recombination sites through the Shockley-Read-Hall (SRH) mechanism [152, 200, 201].

7.3 Low Frequency Noise Measurements

Additional insights into the TID mechanism and densities of the defects contributing to the charge trapping are obtained through low-frequency noise measurements [79, 150, 162, 163, 165, 202]. The excess drain-voltage noise power spectral density S_{vd} can be parameterized as:

$$S_{vd}(f, V_{ds}, V_{gs}) = \frac{K \cdot V_{ds}^2}{f^{\alpha} \cdot (V_{gs} - V_{th})^{\beta}} \tag{7.1}$$

where S_{vd} is the excess drain-voltage noise power spectral density; f is the frequency; V_{ds}, V_{gs}, and V_{th} are the drain, gate, and threshold voltages; K is a constant factor indicating the normalized noise magnitude; α represents the

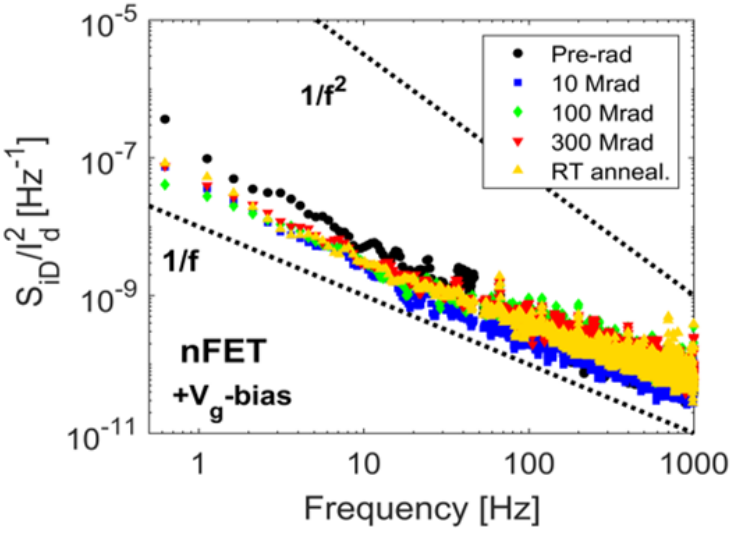
frequency dependence, $\alpha = \partial \log S_{vd} / \partial \log f$; and β represents a measure of the gate-voltage dependence with $\beta = \partial \log S_{vd} / \partial \log |V_{gs} - V_{th}|$ In the linear region of the device response, S_{vd} is related to the drain-current noise power spectral density S_{id} by the relation [161-165]:

$$S_{vd} = R_{ch}^2 S_{id} = \frac{V_{ds}^2}{I_{ds}^2} S_{id} \tag{7.2}$$

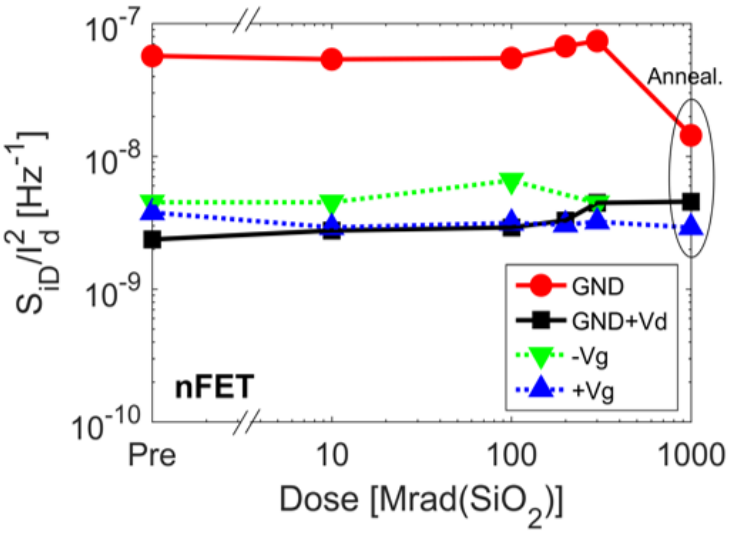
So, Eq. (7.1) can be rewritten equivalently as:

$$\frac{S_{id}}{I_{ds}^2}(f, V_{gs}) = \frac{K}{f^{\alpha} \cdot (V_{gs} - V_{th})^{\beta}} \tag{7.3}$$

The low frequency noise of the MOS devices is caused primarily by the fluctuation of the number of carriers [79, 150, 162, 163, 165, 202]. Normally, traps contributing to noise are distributed uniformly in space throughout the gate oxide and in energy in the Silicon bandgap, with the characteristics of $\alpha \approx 1$ and $\beta \approx 2$ [161-165]. In contrast, significant deviations from $\alpha \approx 1$ and $\beta \approx 2$ indicate non-uniform defect-energy distributions in energy and/or space [161-165]. When $\beta > 2$, the effective density of the border traps is increasing toward the mid-gap. As a comparison, when $\beta < 2$, the distribution of border traps is increasing toward the semiconductor conduction band for n-channel devices or the valence band for p-channel devices [161, 162].



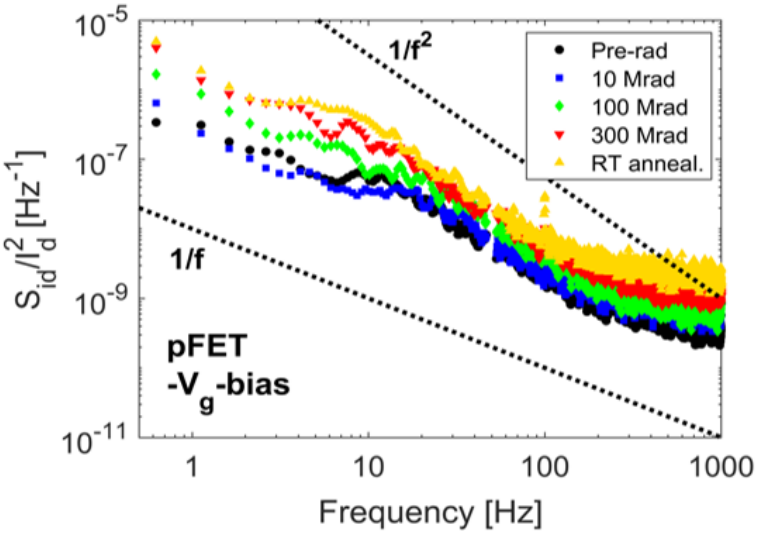
(a)



(b)

Figure 7.10: (a) Low-frequency noise magnitudes at V_{gs} = 0.8 V and V_{ds} = 50 mV of a typical nFET with L = 30 nm. The device was irradiated and annealed in the "+V_g"-bias condition. (b) Noise magnitudes at f = 10 Hz vs. dose for nFETs with L = 30 nm, irradiated and annealed in different bias conditions. Noise measurements are carried out at V_{gs} = 0.8 V and V_{ds} = 50 mV. (From [187])

Figure 7.10(a) shows the low-frequency noise for the shortest nFET. All tested nFETs were characterized by the typical $1/f$ low-frequency noise dependence before and after exposure. Figure 7.10(b) shows the variation of the noise magnitude at 10 Hz as a function of dose. The low-frequency noise of nFETs is insensitive to TID regardless of the applied bias condition during irradiation, confirming the high radiation tolerance of nFETs.



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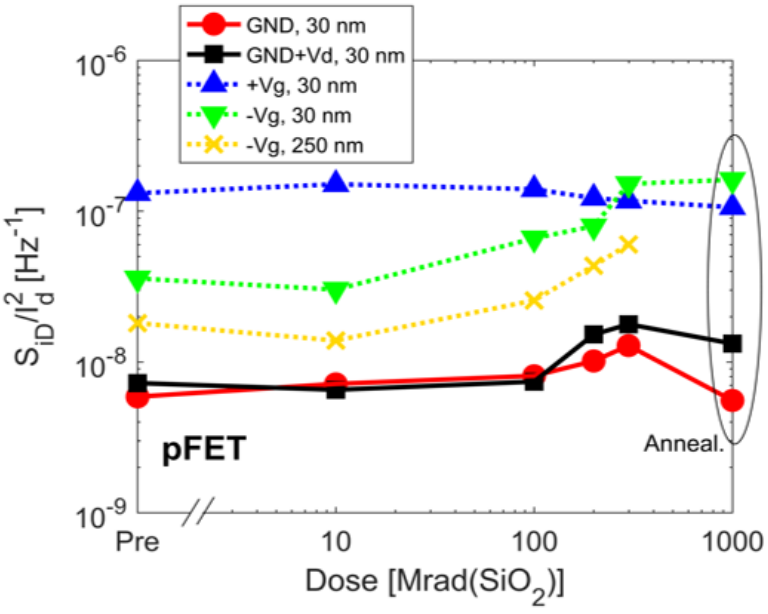
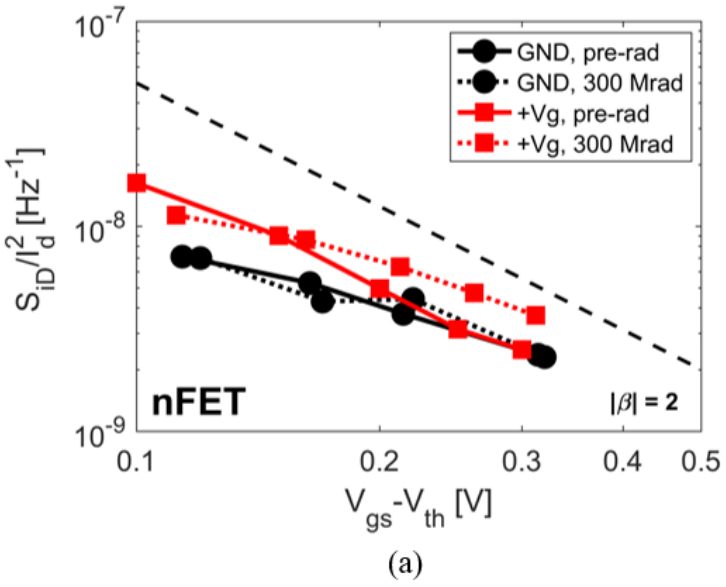


(b)

Figure 7.11: (a) Low-frequency noise magnitudes at $V_{gs} = -0.8$ V and $V_{ds} = -50$ mV of a typical pFET with $L = 30$ nm. The device was irradiated and annealed in the "$-V_g$"-bias condition. (b) Noise magnitudes at $f = 10$ Hz vs. dose for pFETs with $L = 30$ nm, irradiated and annealed in different bias conditions. Noise measurements are carried out at $V_{gs} = -0.8$ V and $V_{ds} = -50$ mV. (From [187])

On the other hand, pFETs show variations of the low-frequency noise vs. cumulative dose, channel length, and bias condition. Figure 7.11(a) shows the low-frequency noise of a pFET with $L = 30$ nm irradiated in the "$-V_g$"-bias condition. pFETs are characterized by a combination of $1/f$ noise and $1/f^2$ low frequency noise, caused by random telegraph noise (RTN) of pre-existing traps [150, 168, 194]. Figure 7.11(b) illustrates the variations of noise magnitude at 10 Hz as a function of dose. The increase of the noise magnitude with dose is visible in all devices, except for the "$+V_g$"-biased pFETs, which show unusually high noise for the as-processed devices. The increased in noise with cumulative dose is particularly evident in the "$-V_g$"-biased devices, indicating enhanced generation of border traps. In addition to the higher initial noise density, which reduces the sensitive of the "$+V_g$"-biased pFETs to TID-induced increases, we note that H^+ drifts toward the oxide/channel interface for "$+V_g$"-biased pFETs, thus favoring activation of interface traps at the SiO_2/Si interface [86, 96, 97]. Interface traps are fast traps, contributing to shifts in threshold voltage without modifying the noise response of devices [165, 199]. This may also account for the lack of increased noise for nFETs in Figure 7.11(a). In contrast, for "$-V_g$"-bias conditions, the H^+ can drift into the HfO_2 oxide, thus activating border traps [165, 203] and increasing the low frequency noise.



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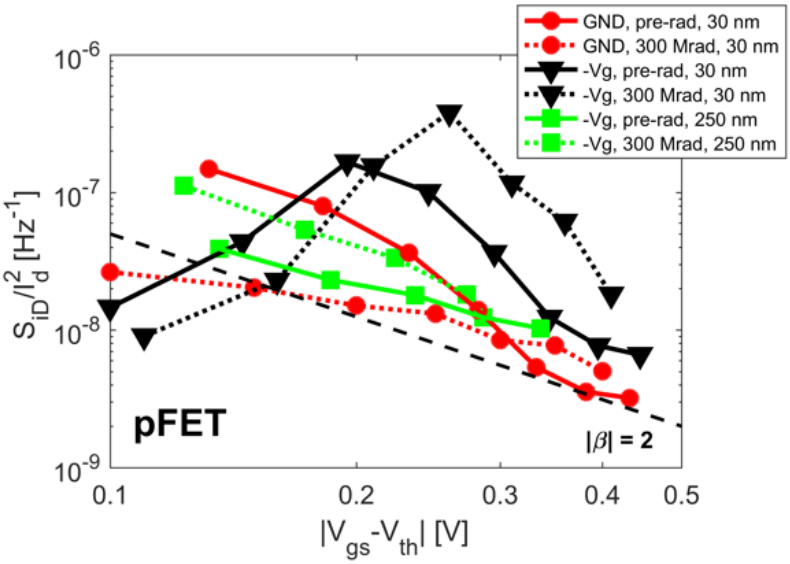

(b)

Figure 7.12: $1/f$ noise magnitudes at $f = 10$ Hz vs. $|V_{gs}\text{-}V_{th}|$ at $|V_{ds}| = 50$ mV for FETs with $L = 30$ nm and $L = 250$ nm. The noise is measured before and after transistors were irradiated under several bias conditions to 300 Mrad(SiO_2): (a) nFETs, and (b) pFETs. (From [187])

To investigate the density distributions in space and energy of the border traps, the low-frequency noise magnitude at 10 Hz is plotted as a function of $V_{gt} = |V_{gs} - V_{th}|$ in Figure 7.12. Referring to expression (7.2), when $\beta = 2$, the effective density of the border traps is uniform in space and energy [79, 162, 163, 165, 202]. Values of $\beta > 2$ indicate an increased effective density of border traps toward mid-gap, while at $\beta < 2$ the distribution of border traps increases toward the conduction band for n-channel devices and valence band for p-channel

devices [79, 162, 163, 165, 202]. In nFETs, the slope $|\beta|$ of S_{id}-V_{gt} before irradiation is $\sim$1.8, indicating an almost uniform spatial distribution of traps. After exposure (dotted lines), the trap density is unchanged in the "*GND*"-bias condition and slightly increases in "$+V_g$"-biased devices. This result agrees with the DC parametric shifts in Figure 7.5, confirming the strong TID tolerance of nFETs.

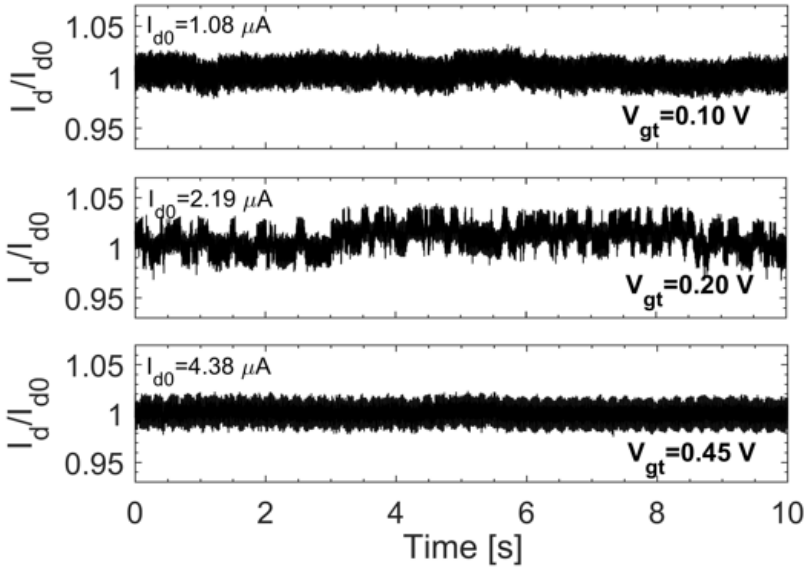

Figure 7.13: Drain current fluctuations in the time domain for as-processed pFETs with $L = 30$ nm for the continuous black curve in Figure 7.12(b). Random telegraph noise is visible at $V_{gt} = 0.2$ V (middle curve above), generating the peak of continuous black curve in the continuous black curve at $V_{gt} = 0.2$ V in Figure 7.12(b). (From [187])

Figure 7.12(b) shows peaks in the noise curves of the "$-V_g$"-biased pFET with $L = 30$ nm (black curves). In general, the noise response of as-processed pFETs can substantially vary from device to device, as devices often exhibit Lorentzian noise. At $V_{gt} = 0.2$ V, for example, the $1/f$ curve of the pFET with L=30 nm exhibits Lorentzian noise, characterized by a $\sim 1/f^2$ power law dependence in the frequency domain, and random telegraph noise (RTN) [168, 194, 196] in the time domain (Figure 7.13). The RTN is visible due to the alternate capture and emission of carriers at individual prominent defect sites, which generate discrete switching in the resistance of the channel and/or of access regions [194, 196]. In contrast, the pFET with $L = 250$ nm presents a S_{id}-V_{gt} response that increases with increasing dose and is characterized by a more uniformly distributed traps, as $|\beta| \sim 1.9$ before irradiation, and $|\beta| \sim 2$ after 300 Mrad(SiO_2).

7.4 Conclusions

In this chapter, GAA nano-wire FETs show outstanding TID tolerance at ultra-high doses up to 300 Mrad(SiO_2). DC static measurements and low-frequency noise measurements show negligible changes in nFET devices. Worst-case degradation is visible when positive bias is applied to the gate with less than 10% drain-current degradation. In contrast, pFETs visibly degrade at doses above 10 Mrad(SiO_2) due to TID mechanisms that depend on irradiation bias condition and channel length. The worst-case bias is when positive potential is applied to the gate during the irradiation. DC characteristics under positive bias exhibit shifts in the threshold voltage caused by the H^+-driven generation of interface traps at the oxide / channel interface. pFETs under negative gate bias are dominated instead by transconductance loss. Longer-channel pFETs show increased degradation with TID, most likely as a result of decreasing gate control. Low-frequency noise measurements in pFETs show significant increases in noise magnitude and enhanced random-telegraph noise due to the activation of high densities of border traps and prominent defects in the gate dielectrics.

In addition, the off-state leakage current increases in both n- and p-channel FETs with dose. In nFETs, the Si-bulk region below the Si nano-wires can be sensitive to STI trapped charge, inducing the activation of parasitic drain-to-source channels near the STI sidewalls. In pFETs, the off-state leakage current increases due to trap-assisted recombination in STI sidewalls and / or spacer dielectrics at the pn drain/bulk junctions.

Chapter 8

Conclusions

In this thesis, we investigate the TID degradation mechanisms in nanometer scale CMOS technologies exposed to ultra-high levels of ionizing doses, comparable to those that tracker detectors in HL-LHC will have to withstand. Devices from different manufacturers were irradiated with X-rays up to doses of 300 - 1000 Mrad(SiO_2), and then annealed at high temperature. The TID-induced electrical responses of the transistors were analyzed by DC statics characteristics and low frequency *1/f* noise measurements, allowing to investigate the nature, locations and energetic levels of the TID-induced defects. The TID degradation mechanisms were evaluated in 16 nm bulk FinFETs and Si nanowire GAAFETs of different types, dimensions and layout.

The obtained experimental results show different dominating TID effects, strongly depending on the irradiation bias conditions, channel length and chip layout. Due to the ultra-thin thickness of the gate dielectric of nanoscale CMOS technologies, the density of trapped charge in the gate oxides is decreased, leading to a high TID tolerance. However, with the reduction of feature size of the device, new TID-induced effects appear in nanoscale technologies, due to the charge trapping in other thick oxides and advanced fabrication processes, such as shallow trench isolation (STI) oxides, spacer dielectrics, and halo implantations.

In 16 nm bulk FinFETs irradiated up to 1 Grad(SiO_2), devices show significant degradation in the maximum drain currents, transconductance and off-state leakage currents with slight subthreshold stretch-out and negligible threshold voltage shifts. TID effects are dominated by the trapped charge buildup in STI and its interface with large degradation of the transconductance. The TID sensitivity is strongly dependent on the irradiation bias conditions, channel length and fin-number. The worst degradation is observed in transistors irradiated in "diode" or "on" conditions, as a result of the increased charge yield. Short channel transistors have a better TID tolerance than long channel ones, thanks to the influence of halo implantations, increasing the channel doping in short channel devices. The TID responses of nFinFETs are insensitive to both fin- and finger-

numbers, while pFinFETs designed with the lowest number of fins show worst TID degradation due to the larger TID effects on the lateral fins at both sides. In addition, we investigate the TID-induced sample-to-sample variability, sample-to-sample, which increases significantly at ultra-high doses ($>$ 100 Mrad(SiO_2)), due to the impact of random dopant fluctuations, the variability of the irradiated transistors is correlated to the initial process-dependent variability.

Technology nodes	Dominating TID effects			
	Gate Stack	STI	Spacer	Halo
150 nm Si MOSFET	Medium	High	Low	Medium
65 nm Si MOSFET	Low	High	High	Low
28 nm Si MOSFET with high-*k* gate	Low	High	Low	High
16 nm Si FinFET with high-*k* gate	Low	High	Not used	High

Figure 8.1: Dominating TID-induced degradation mechanisms are related to: gate dielectrics, shallow trench insulations (STI), spacers, and halo implantations. The table indicates how much each element influences the TID electrical responses of four bulk Si CMOS technology nodes. (From [71])

In the Si nanowire GAAFET technology, at ultra-high doses up to 300 Mrad(SiO_2), transistors show outstanding TID tolerance compared to previous planar CMOS technologies. DC static measurements and low-frequency noise measurements show negligible changes in nFET devices. Worst-case degradation is visible when positive bias is applied to the gate with less than 10% drain-current degradation. In contrast, pFETs visibly degrade at doses above 10 Mrad(SiO_2) due to TID mechanisms that depend on irradiation bias condition and channel length. The worst-case bias is when positive potential is applied to the gate during the irradiation. DC characteristics under positive bias exhibit shifts in the threshold voltage caused by the H^+-driven generation of interface traps at the oxide/channel interface. pFETs under negative gate bias are dominated instead by transconductance loss. Longer-channel pFETs show increased degradation with TID, most likely as a result of decreasing gate control. Low-frequency noise measurements in pFETs show significant increases in noise magnitude and enhanced random-telegraph noise due to the activation of high densities of border traps and prominent defects in the gate dielectrics. In addition, the off-state leakage current increases in both n- and p-channel FETs with dose. In nFETs, the

Si-bulk region below the Si nano-wires can be sensitive to STI trapped charge, inducing the activation of parasitic drain-to-source channels near the STI sidewalls. In pFETs, the off-state leakage current increases due to trap-assisted recombination in STI sidewalls and/or spacer dielectrics at the pn drain/bulk junctions.

In conclusion, each CMOS technology node is influenced by one or multiple TID degradation mechanisms, which can influence the TID electrical responses of the devices at different levels. Figure 8.1 summarizes the dominating TID-induced degradation mechanisms in four bulk Si CMOS technology nodes, from 150 nm ~ 16 nm. The continuous scaling down of the advanced CMOS technologies requires new and advanced materials, geometries, layouts, and manufacturing process, including both advantages and disadvantages to the TID sensitivity of devices, which maybe lead to new and complex TID mechanisms. In addition, the desire to further improve our understanding of fundamental particle physics lead to the design and development of colliders with performances, in terms of energy and intensity, even higher than those planned the HL-LHC, which will pose unprecedented challenges to electronic systems. The unpredictable trend in the TID effects requires continuous efforts to measure, evaluate and authenticate the electronic devices, which keeps high the interest of the scientific community into the research of TID effects on modern advance CMOS technologies.

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Also, I would like to express my sincere gratitude to my co-supervisor, Dr. Stefano Bonaldo, for his patient and almost hand on hand guidance from the experimental setup to data analysis to how to write a high-quality paper during the three years, for many times to help me revise my papers until midnight, and for his concern and help to my life in Italy. I learned a lot from him, and he is like my brother, I was very happy and satisfied to be able to work in the same office with him for three years.

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