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DOCTORAL THESIS

Ultra-Low Noise Oscillators enabling Frequency Generation for Radar Systems in Scaled CMOS Technologies

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Abstract

In those systems where it is important to synthesize a precise frequency signal, such as the carrier of a transmission system, phase noise is certainly one of the most important aspects that define the performance.

Because of the ever increasing data rate in modern communication systems (5G), the interest of low phase noise frequency synthesizer is high. Radar systems are another example in which the phase noise has an important role: by exploiting the Doppler effect, informations on distance and speed of the target are obtained by comparing the frequency of the transmitted and received signal. Radar systems are precise but also expensive due to their complexity. As an example, radar are used in air plane to detect perturbations. In recent years, however, radar systems have also been spreading in the automotive field, as advanced driving assistance systems (ADAS). Although this is not new: the first car to have a radar system appeared in the market in 1990, only luxury models were employing radar. Nowadays, ultra-scaled CMOS technology has made the widespread deployment of radar on low-cost cars economically advantageous. The challenge is to obtain good performances comparable with bipolar technology.

For this reason, oscillators, which are the heart of a frequency synthesizer, in CMOS technology, are the main topic of this thesis.

After a brief introduction about the operating principle of a typical car radar, we enter into the merits of the design of an analog circuit by developing a methodology to identify the optimum oscillation frequency, that is, the frequency that allows us to obtain the best performance.

Then the designs of two oscillator topologies are described, both operating at 20GHz: the first is a hybrid class B/D oscillator, while the second one a class C. The latter in particular proves to be effective in reducing the contribution of the flicker noise from the active devices, one of the biggest limitations of modern CMOS technologies.

Finally, a method to extract the fourth harmonic from the class C oscillator is presented. This allows to employ the class C oscillator for automotive radar application, as described by regulations.

Sommario

In qualunque sistema in cui sia necessario generare una segnale di frequenza preciso, come ad esempio la portante di un sistema di trasmissione, il rumore di fase è certamente uno degli aspetti più importanti che definiscono le prestazioni dell'apparato.

L'interesse per sistemi a basso rumore di fase è al giorno d'oggi grande vista la diffusione di sistemi di comunicazione 5G. Un'altra applicazione in cui questo è importante è nei sistemi radar, dove sfruttando l'effetto Doppler, le informazioni su distanza e velocita del bersaglio vengono ottenute dal confronto tra frequenza del segnale trasmesso e ricevuto. Il radar è un apparato di misura preciso ma anche complesso e perciò costoso; in ambito civile trova applicazione soprattutto a bordo di aerei per individuare, ad esempio, perturbazioni meteo. Negli ultimi anni però, si sta assistendo alla diffusione di sistemi radar anche nel campo automibilistico, come sistemi di aiuto alla guida, i così detti ADAS. Per quanto questo non sia nuovo, la prima auto ad avere un sistema radar è comparsa nel mercato nel 1990, solo modelli di lusso montavano questi sistemi. Ora la tecnologia CMOS ha raggiunto una maturità tale da rendere econimicamente vantaggiosa la diffusione su larga scala di radar anche su auto a basso costo. La sfida è quella di ottenere prestazioni da tecnologie digitali CMOS comparabili a quelle a bipolari.

Per questo motivo, questa tesi, tratta di oscillatori, che sono il cuore di un sintetizzatore di frequenza, realizzati in tecnologia CMOS.

Dopo una breve introduzione su quello che è il principio di funzionamento di un tipico radar per auto, si entra nel merito del design di un circuito analogico sviluppando una metodologia per individuare la frequenza di oscillazione ottima, cioè quella frequenza che consente di ottenere le prestazioni migliori.

Dopodiché vengono descritti i design di due topologie di oscillatori entrambi operanti a 20GHz: il primo è un ibrido classe B/D, il secondo un classe C. Quest'ultimo in particolare si dimostra essere efficace a ridurre il contributo del rumore flicker dei dispostivi attivi, uno dei più grossi limiti delle tecnologie CMOS moderne.

Infine viene mostrato un metodo per estrarre una componente di quarta armonica, ovvero a 80 GHz, dall'oscillatore in classe C cosicché il radar possa operare a frequenze concesse dalle normative.

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Chapter 1

Introduction

The interest for low phase noise frequency synthesizer covers many application: from 5G communication systems, imaging radar, anti-collision systems and optical network. Phase noise can affect the performance of systems where an accurate frequency signal is needed. Phase locked loop (PLL) are customary employed as frequency synthesizer because it's able to filter most of the low frequency phase noise from the local oscillator, which is the core of a PLL.

Because of the ever increasing data rates in modern communication systems and high accuracy needed in new generation of radar, operating frequencies in the millimeter-wave range are required, as shown in Fig. 1.1. It is often preferred to design the oscillator to work at lower frequency, taking advantage of better quality factor and, thus, better phase noise; and then use a frequency multiplier to obtain the desired frequency.

For high performance, compound technologies, like SiGe, are often employed. CMOS technologies, on the other hand, are economically more convenient as allow for highly integration. The downside is that ultra-scaled CMOS technologies suffer from large flicker noise, which can be upconverted in phase noise by the oscillator. This requires special attention during the design.

A system that is becoming more popular these days is the radar system; radar stands for "radio detection and ranging". While the first patent about radar system date back to 1904 by Christian Hulsmeyer [1], its uses was limited to military application, navigation or for scientific purposes as it allows for precise measurements of distance and speed. But, because of the diffusion of driving assistance systems, radar technology is now becoming increasingly present in everyday life.

In the following, a brief introduction about radar system will be given.

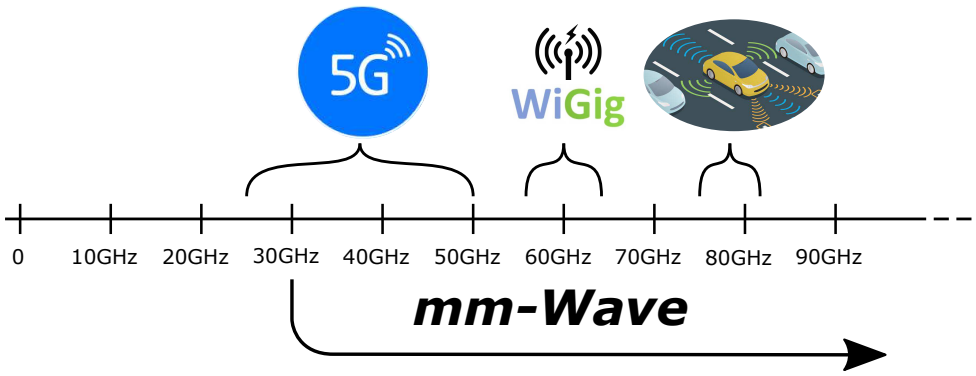


FIGURE 1.1: Frequency allocation in the spectrum.

1.1 Radar Overview

Radar systems are used in a wide range of applications, that span from civilian, scientific to military applications. The main application of a radar are:

- civilian:
  - Weather radar (Fig. 1.2)
  - Altimetry
  - Security alarms
  - Airport surveillance
  - Geographic mapping
  - Air and marine navigation
  - Automotive
- scientific:
  - Astronomy
  - Mapping and imaging
  - Precision distance measurement
  - Remote sensing of the environment
- military:
  - Detection and tracking of aircraft, missiles, and spacecraft
  - Intelligence data collection
  - Weapon guidance and control
  - Air and marine navigation

FIGURE 1.2: Weather radar antenna.

1.1.1 Radar Equation

A radar detects the presence of objects and locates their position in space by transmitting electromagnetic energy and observing the returned echo. Figure 1.3 shows an example of radar system: the target is radiated at a distance d_1 from the transmitting antenna, the receiving antenna is at a distance d_2 from the target.

If the transmitter radiates a power P_t through an antenna of gain G_t, the power density incident on the target, assuming that is in the main beam direction of the antenna, is:

$$S_t = \frac{P_t G_t}{4\pi d_1^2}, \tag{1.1}$$

where d_1 is the distance of the target. The incident power will be scatter in different direction from the target. The ratio of the scattered power in a given direction to the incident power density is defined as the radar cross section, σ, of the target:

$$\sigma = \frac{P_s}{S_t}, \tag{1.2}$$

where P_s is the total power scattered by the target, and S_t is the power

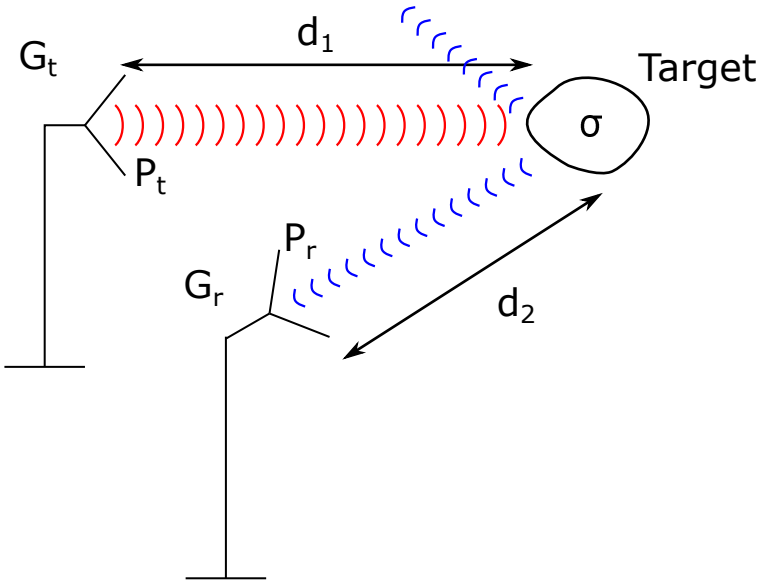


FIGURE 1.3: Radar system.

density incident on the target. The radar cross section is measured in square meters and depends on the angles and polarization of incident and reflected waves

The power density of the scattered radiated field from the target decay as $1/(4\pi d^2)$ away from the target. Thus the power density of the scattered field back at the receive antenna must be:

$$S_r = \frac{P_t G_t \sigma}{(4\pi)^2 d_1^2 d_2^2}, \tag{1.3}$$

The portion of energy intercepted by the received antenna is given by the effective aperture of the antenna, and it's defined as:

$$A_r = \frac{G_r \lambda^2}{4\pi}. \tag{1.4}$$

Assuming $G = G_t = G_r$, and also $d = d_1 = d_2$ the received power is given by the radar equation:

$$P_r = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 d^4}. \tag{1.5}$$

The received power decays as $1/d_4$, which implies that a high-power transmitter and a sensitive low-noise receiver are needed to detect targets at long ranges.

The presence of noise at the antenna receiver, determine the minimum detectable power that can be discriminated by the receiver. This noise is due

the transmitter and disturbance in medium; the noise of the receiver contribute as well. The figure of merit that is often employed to describe the performance of a radar is the signal-to-noise ratio, that can be derived using 1.5 as:

$$SNR = \frac{P_r}{P_N} = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 d^4 k T_0 B F_N L}, \tag{1.6}$$

where: k is the Boltzman's constant, T_0 is the reference temperature in Kelvin, B is the effective noise bandwidth of the radar, F_n is the radar noise figure and L takes into account for losses associated with radar and environment.

This equation can be inverted to derive the maximum range:

$$d_{max} = \left(\frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 k T_0 B F_N L \cdot SNR} \right)^{(1/4)}, \tag{1.7}$$

However, the above results seldom describe the performance of an actual radar system. Signal processing, propagation effects, the statistical nature of the detection process, and external interference often influence the usable range of a radar system.

1.1.2 Radar Waveform

The waveforms that a radar transmits and receives determine its capabilities for target detection, and particularly, for measurements and observations. An important class of radar is the pulse radar. Based on the transmitted waveforms, a pulse radar can be distinguished in: continuous wave pulses, chirp pulses, phase-coded waveforms, and pulse bursts [2].

In a pulse radar, the transmitter send a short burst of electromagnetic energy; after that, the receiver is turned on to listen for the echo. The echo indicates the presence of a target, but also the distance from the transmitter from the time elapses between the transmission of the pulse and the receipt of the echo.

The continuous wave (CW) pulse is the simplest pulsed-radar waveform, as they are easy to generate and to process in the receiver. For this reason is often employed. The CW pulse consists of a constant-frequency, constant-amplitude pulse of duration τ (Fig. 1.4 (a)); thus, the range resolution is $\Delta d = c\tau/2$, with c the speed of light.

The principle of operation of a radar is based on the Doppler effect. It a common knowledge from acoustics and also optics that, if either the source

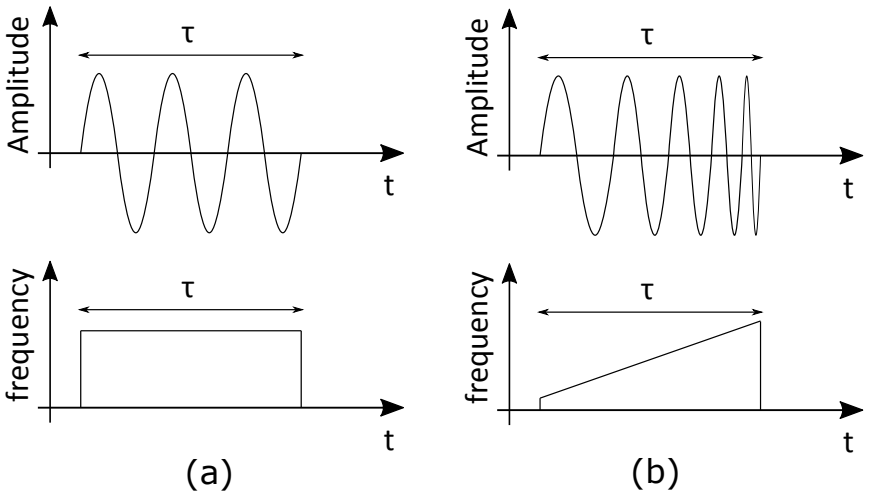


FIGURE 1.4: (a) CW pulse, (b) chirp pulse.

or the observer are in motion, an apparent shift on the transmitted signal frequency appears. Measuring this shift it is possible to obtain the speed of the target.

For CW pulses, the Doppler-frequency resolution, f_R is taken to be equal to $1/\tau$, which is also approximately equal to the signal bandwidth. This results in a radial-velocity resolution $\Delta v = \lambda/(2\tau)$, where λ is the wave-length of the transmitted signal. The major limitation of the CW pulse is , therefore, the difficulty in obtaining both good range and good radial-velocity resolution.

Another type of pulsed radar waveform is the linear frequency modulated chirp pulse radar; in which, as shown in Fig. 1.4 (b), the transmitted signal frequency is made to vary linearly. This allows to increase the bandwidth compare to a simple CW radar, therefore, to increase the radial velocity resolution.

Phase-coded waveforms employ a series of subpulses, each transmitted with a particular relative phase. These are processed in the receiver matched filter to produce a compressed pulse having a time resolution equal to the subpulse duration, τ_s, and a frequency resolution equal to $1/\tau$, where τ is the total waveform duration. Therefore the range resolution is $\Delta d = c\tau_s/2$ and the velocity resolution is $\Delta v = \lambda/(2\tau)$. A common form of phased-coded waveform, called a binary phase-coded or phase-reversal waveform, employs subpulses having either 0 or 180 degree relative phase (Fig.1.4). The advantage is that it doesn't require a linear sweep of the frequency, which can be difficult to obtain.

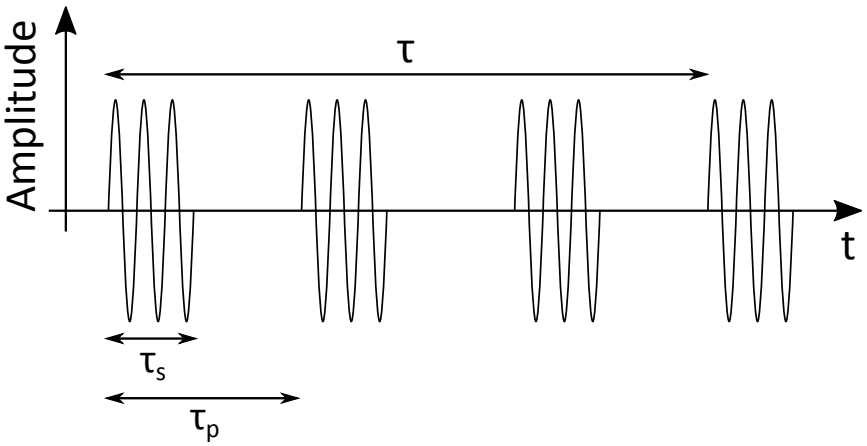


FIGURE 1.6: CW pulse burst.

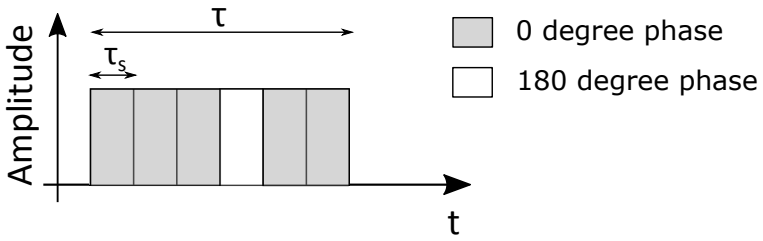


FIGURE 1.5: Binary phase-code.

Finally, the Pulse-burst waveforms consist of a train of pulses separated in time. A common pulse-burst waveform consists of n_S identical pulses having duration τ_S, and spaced in time by τ_P. The time resolution is determined by the subpulse bandwidth B_S. For CW subpulses (Fig.1.6), $B_S = 1/\tau_S$. The frequency resolution is determined by the total waveform duration, and is equal to $1/\tau$ or $1/[(n_S - 1)\tau_P]$.

Another important class of radar is the frequency modulated continuous wave (FMCW) radar. In contrast to pulse-based radar they transmit a continuous electromagnetic wave rather than a time-limited pulse and receive simultaneously while transmitting.

The principle of operation of pulse radar is based on time separation between the transmitted and reflected signal; and measurement of the time interval between transmitted and received pulses. In FMCW radar, because continuous radiation is used, separation of transmitted and reflected signals in time is impossible. Therefore, to obtain information about distance, it is necessary to modulate the transmitted signal. In practice, amplitude modulations are not used as it would be impossible to distinguish the modulation from the background noise and interference.

On the other hand, frequency modulations are suitable for this operation. By employing a mixer, that multiply the transmitter and received signals,

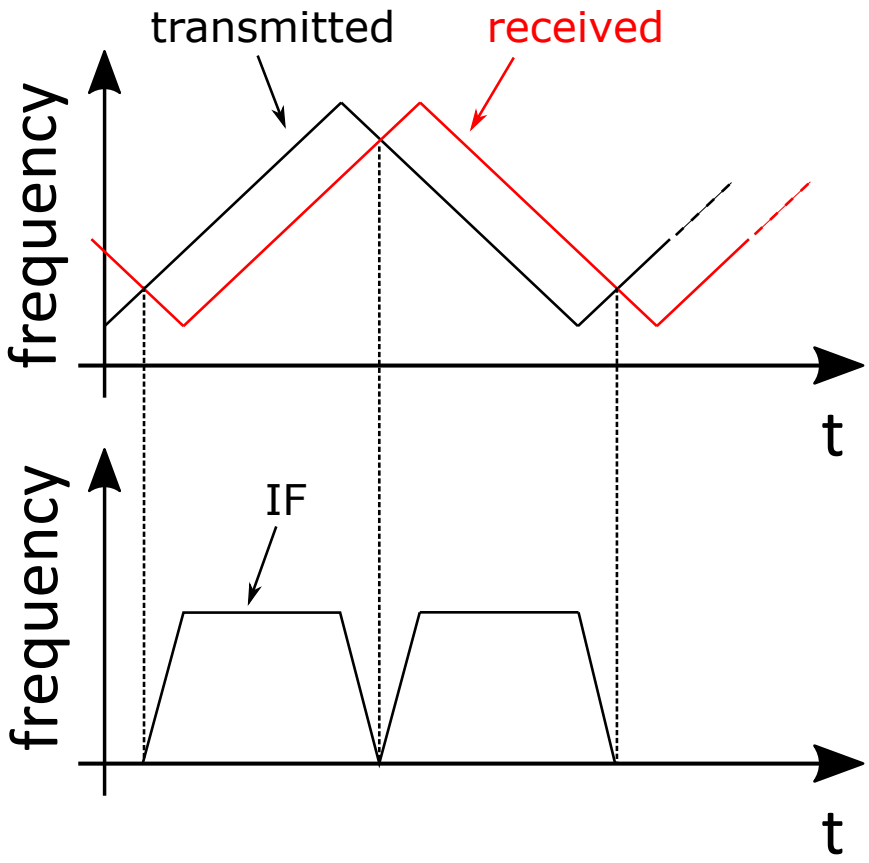


FIGURE 1.7: Linear frequency modulated continuous wave.

the difference component of the input signals, that bear the information of distance and speed of the target, can be obtained. This signal is called intermediate frequency (IF) signal. On the other hand, the sum component is not necessary and can be easily filtered out.

A frequently used modulation is the linear frequency modulated continuous wave (LFMCW) (Fig.1.7). The frequency is made to vary linearly, which is generally called a frequency sweep, or chirp. The slope of the sweep can either be positive or negative, which is then called upchirp or downchirp, respectively.

When the radar is used for single target only, as in the radio altimeter, the linear modulation waveform is not often employed. Sinusoidal or almost sinusoidal frequency modulation have the advantage of being easier to obtain with practical equipments than linear modulations. The beat frequency obtained with sinusoidal modulation is not constant over the modulation cycle as it is with linear modulation. However, it can be shown that the average beat frequency measured over a modulation cycle gives the correct value of target range. Any reasonable-shape modulation waveform can be used to measure the range, provided the average beat frequency is measured.

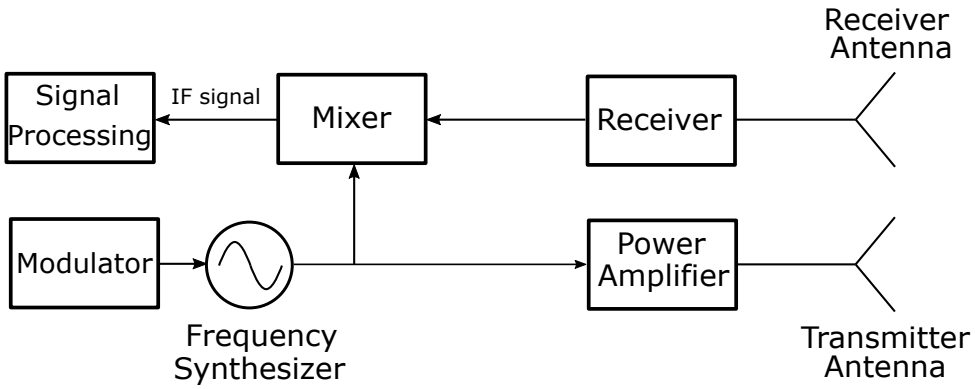


FIGURE 1.8: Block diagram of FM radar.

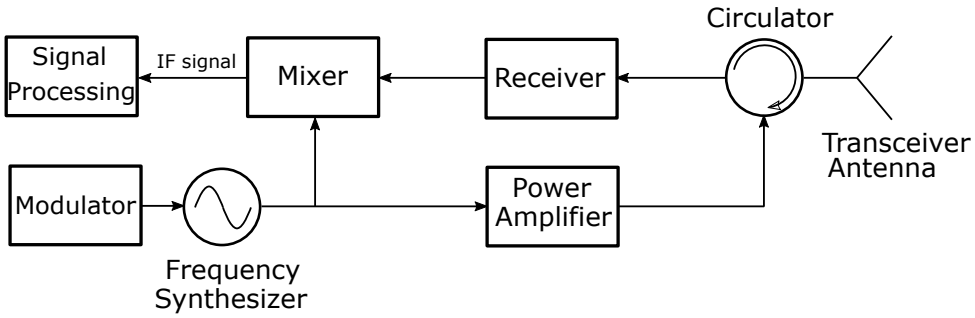


FIGURE 1.9: Block diagram of FM radar with single transceiver antenna.

1.1.3 Block Diagram of FM Radar

The block diagram of a frequency modulated continuous wave radar is presented in Fig.1.8. The frequency synthesizer generates a sinusoidal signal whose frequency value is given by the modulator. This signal is then amplified and transmitted by the antenna. The received signal, after being amplified by the receiver, is compared by the mixer with the transmitted signal. The resulting IF signal is then processed in order to obtain information of distance and speed of target. Because the mixer compares basically the same signals, where the received signal is just a time delayed version of the transmitted signal, this receiver is called *homodyne*.

This diagram requires two antenna, which in some applications might not be feasible due to area constraints. Therefore, Fig.1.9 shows an diagram block that employs one transceiver antenna and a circulator. The rest of operation is identical as in the previous diagram.

1.1.4 Automotive Radar

An important application of radar system that is becoming popular this days is the automotive radar.

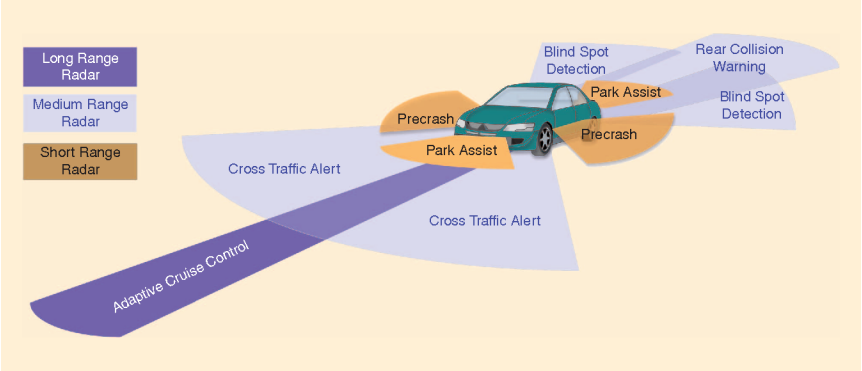


FIGURE 1.10: Radar system in car.

Making driving on the streets more safe and convenient has been one of the key promises for any new car generation in the last three decades. The goal is to relieve the driver from the combination of monotonic tasks and split-second decisions within complex traffic scenarios to improve safety and comfort. This functionality is nowadays called advanced driver assistance system (ADAS).

Those systems can be divided in passive or active driver assistance. Passive assistance don't influence the vehicle motion but rather act in certain scenario, for instance, providing additional information during parking. Active driver assistance, on the other hand, can directly influence the vehicle dynamic, for example, the adaptive cruise control can accelerate or decelerate the car based on the traffic.

Different kind of sensors are used in the automotive environment: radar, lidar, camera and ultrasound. Radar can measure radial distance and velocity of remote objects very precisely. Using more transmitter/receiver channel as in Fig.1.8 or Fig.1.9 allows to obtain additional information about angular position and speed. Compared to other sensors, radar is robust against environmental influences such as extreme temperatures, bad light or weather conditions. Due to these reasons, radar has been identified as the most promising technology for a number of driver assistance functions, as showed in Fig.1.10.

1.2 Frequency Regulation

Given the widespread use of radar systems, in 2003, European Commission (EU) issued a mandate to the European Conference of Postal and Telecommunications Administrations (CEPT) to harmonise the radio spectrum among the member of the European Union, and to facilitate a coordinated introduction of the automotive radar. As a result: the 77 GHz range band has been identified as the long term operating frequency for automotive application [3].

However, automotive short-range radar technology in the 77 GHz range band was still under development and not immediately available on a cost-effective basis.

Therefore, to enable the early introduction of automotive radar, as a temporary solution, EU allowed the use of the 24 GHz band since technology was considered sufficiently mature for operation in that band. Being the 24 GHz band shared for other scientific purposed (i.e. earth exploration and radio astronomy services), automotive radar systems are only allowed to use this band if they follow detailed regulatory restrictions to protect other users. Therefore, the maximum mean power density is set to 41.3 dBm/MHz effective isotropic radiated power and also the total amount of vehicle equipped with radar is 7% [3].

It was expected that, by 2013, new generation of automotive radar would have been available and that the 24 GHz band could be phase out. However, the research on 77 GHz radar system has experienced a significant delay, and it has become clear that new systems with 77 GHz technology would not be mature enough for commercial deployment in cars by 2013.

In order to bridge the technological gap, the European Commission evaluated different solutions and decided to prolong the period in which 24 GHz radar could be placed in new cars [4, 5]. The new deadline was set to 1 January 2018. It was also decided to extend by a further 4 years (until 1 January 2022) the possibility of mounting 24 GHz radar equipment in cars where approval was granted before 1 January 2018 [6].

For this reason, in litterature many examples of radar operating in the 77 GHz band have been presented [7–12] in the last 2 decades. A very important issue is worldwide harmonization of the frequency allocation: USA [13], Canada, Russia, Japan, China and Korea have also adopted the 77 GHz band and is expected the other to join.

The International Telecommunication Union (ITU) specified the system

characteristics of automotive radars operating under the radiolocation service in the frequency band 76-81 GHz [14].

Based on functional and safety requirements, ITU divided automotive radar systems in two categories:

- **categories A**: adaptive cruise control (ACC) and collision avoidance (CA) radar, for measurement ranges up to 250 metres the typical technical characteristics are listed in Table 1.1 as Radar A. For these applications, a maximum continuous bandwidth of 1 GHz is required. Such radars are considered to add additional comfort functions for the driver, giving support for more stress-free driving;

- **categories B**: sensors for high resolution applications such as blind spot detection, lane-change assist and rear-traffic-crossing-alert, detection of pedestrians and bicycles in close proximity to a vehicle, for measurement ranges up to 100 metres the typical technical characteristics are listed in Table 1.1 as Radar B, Radar C and Radar D. For these high resolution applications, a necessary bandwidth of 4 GHz is required. Such radars directly add to the passive and active safety of a vehicle and are therefore an essential benefit towards improved traffic safety. The increased requirements for active and passive vehicle safety are already reflected in the requirements for vehicle testing. Radar E operates with a higher field of view to enable high-resolution applications such as pedestrian detection, parking-aid, and emergency braking at low speed (< 30 km/h).

TABLE 1.1: Automotive radar characteristics in the frequency band 76-81 GHz

Parameter	**Units**	**Radar A Front app**	**Radar B High-Res Front**	**Radar C High-Res Corner**	**Radar D High-Res**	**Radar E High-Res Short range**
Sub-band used	GHz	76-77	77-81	77-81	77-81	77-81
Typ operating range	m	Up to 250	Up to 100	Up to 100	Up to 100	Up to 50
Range resolution	cm	75	7.5	7.5	7.5	7.5
Typ emission type		FMCW, Fast-FMCW	FMCW, Fast-FMCW	FMCW, Fast-FMCW	FMCW	FMCW, Fast-FMCW
Max necessary bandwidth	GHz	1	4	4	4	4
Chirp bandwidth	GHz	1	2-4	2-4	2-4	2
Typical sweep time	s	10-40m 10-40u	10-40m 10-40u	10-40m 10-40u	2-20m	10-40m 10-40u
Maximum e.i.r.p.	dBm	55	33	33	45	33
Maximum transmit power to antenna	dBm	10	10	10	10	10
Max power density of unwanted emission	dBm/MHz	–30	-30	-30	-13	-30

TABLE 1.1: Automotive radar characteristics in the frequency band 76-81 GHz

Parameter	**Units**	**Radar A Front app**	**Radar B High-Res Front**	**Radar C High-Res Corner**	**Radar D High-Res**	**Radar E High-Res Short range**
Receiver IF bandwidth (–3 dB)	MHz	0.5-1	10	10	10	10
Receiver sensitivity	dBm	–115	–120	–120	–120	–120
Receiver noise figure	dB	15	12	12	12	12
Equivalent noise bandwidth	kHz	25	16	16	16	16
Antenna main beam gain	dBi	Typ 30 Max 45	TX: 23 RX: 16	TX: 23 RX: 13	TX: 35 max. RX: 35 max	TX: 23 RX: 13
Antenna azimuth 10 dB beamwidth	degrees	TX/RX: ±10	TX: ±22.5 RX: ±25	TX: ±23 RX: ±30	TX: ±30 RX: ±30	TX: ±50 RX: ±50
Antenna azimuth -3 dB beamwidth	degrees	TX/RX: ±5	TX: ±12.5 RX: ±13.5	TX: ±12.5 RX: ±16	TX: ±16 RX: ±16	TX: ±27 RX: ±27
Antenna elevation -3 dB beamwidth	degrees	TX/RX: ±3	TX/RX: ±5.5	TX/RX: ± 5.5	TX/RX: ± 5.5	TX/RX: ± 5.5

1.3 Conclusions

Radar systems can precisely measure distance and speed of a target. For this reason it is employed in a number of different applications: such as, detection and tracking of aircraft, mapping and remote sensing of environment. Due to its robustness against environmental influences, radar technology is also suited for automotive application.

Phase noise produced by the frequency synthesizers can limit the performance in many systems, including radar, as the measurement of distance and speed is based on the comparison between the transmitted and received signal frequencies.

In chapter 2 of this thesis, the principle of operation of a frequency modulated continuous wave radar will be presented.

From chapter 3 the topic is harmonic oscillators and, in particular, in this chapter a methodology to find the optimal operation frequency that minimize the phase noise for a given technology is discussed.

Chapter 4 deals with flicker noise upconversion. In this chapter, two different topologies of CMOS oscillator are discussed: an hybrid class B/D and a class C. Both oscillators operate at 20 GHz.

Due to regulations, automotive radar operates in E band; for this reason, a frequency multiplication by four is required. Therefore, in chapter 5, a technique to extract the fourth harmonic in class C oscillator is presented.

Chapter 2

FMCW Radar

In this chapter, the principle of operation of a frequency modulated continuous wave radar is presented. The following is based on the block diagram in Fig.2.1, that represent a homodyne radar transceiver with a single antenna.

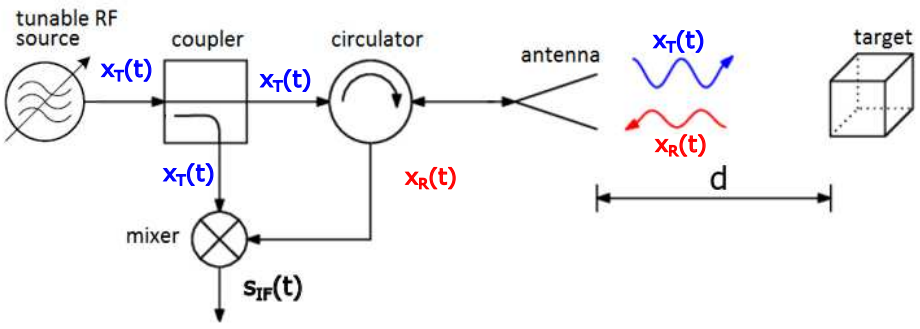


FIGURE 2.1: Block diagram of FM radar with single transceiver antenna.

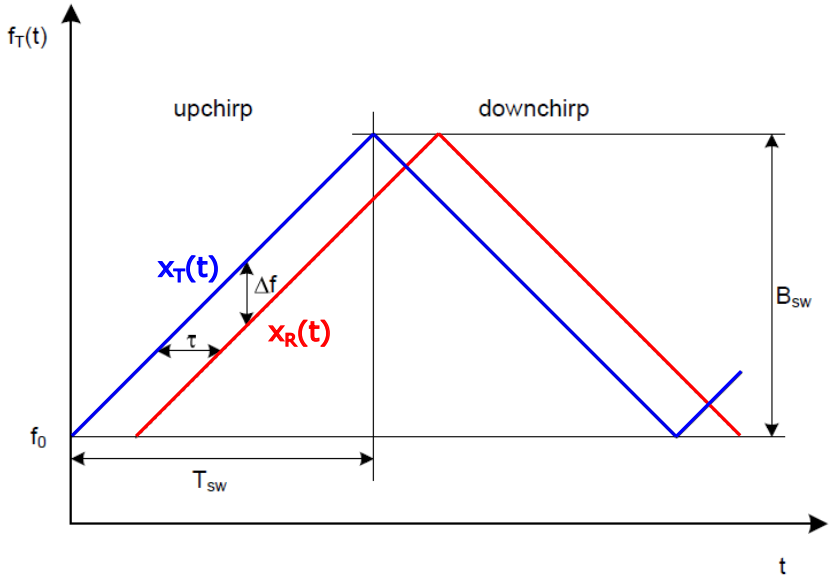


FIGURE 2.2: Block diagram of FM radar with single transceiver antenna.

2.1 Principle of Operation of a FMCW radar

In a FMCW radar, the transmitted signal is a sinusoid with amplitude A_T and a time dependent phase $\phi_T(t)$.

$$x_T(t) = A_T \cos(\phi_T(t)). \tag{2.1}$$

If the frequency of the transmitted signal is made to vary linearly (Fig.2.2), then:

$$f_T(t) = f_0 + mt. \tag{2.2}$$

for t = 0 to T_{Tsw}, with f_0 being the start frequency, m the slope of the frequency chirp in Hz/s, and T_{Tsw} the sweep duration.

If B_{sw} is the covered bandwidth of the frequency sweep, the slope of the sweep is:

$$k = \frac{B_{sw}}{T_{Tsw}}, \tag{2.3}$$

The instantaneous phase of the transmitted signal can be obtained integrating the frequency:

$$\phi_T(t) = 2\pi \int_0^t f_t(\tau)d\tau + \phi_0 = 2\pi f_0 t + \pi m t^2 + \phi_0, \tag{2.4}$$

which, inserted in 2.1, gives:

$$x_T(t) = A_{\mathrm{T}} \cos(2\pi f_0 t + \pi m t^2 + \phi_0). \tag{2.5}$$

Where $\phi_0(t)$ is the initial phase at the beginning of the sweep. When the radar beam encounters an object it gets scattered, and a portion of beam return back. The received signal is damped and time-delayed version of the transmitted waveform. The time τ that takes to the transmitted signal to return back can be computed as:

$$\tau = \frac{2d}{c}, \tag{2.6}$$

with d the distance between the radar and the target and c the speed of the electromagnetic wave.

The reflected signal at the receiver input is modelled as:

$$x_R(t) = \alpha A_{\mathrm{T}} \cos(\phi_T(t-\tau)) = \alpha A_{\mathrm{T}} \cos(2\pi f_0 (t-\tau) + \pi m (t-\tau)^2 + \phi_0), \tag{2.7}$$

where α takes into account the attenuation due to the path and reflection losses. The transmitted and received signals are then processed by the mixer: using the simple multiplicative model of the mixer, it calculates the product of $x_R(t)$ and $x_T(t)$, which results in an IF signal:

$$x_{IF}(t) = x_T(t) x_R(t) = \alpha A_{\mathrm{T}}^2 \cos(\phi_T(t)) \cos(\phi_T(t-\tau)). \tag{2.8}$$

Using the trigonometric identity:

$$\cos(a)\cos(b) = \frac{1}{2}\left[\cos(a-b) + \cos(a+b)\right], \tag{2.9}$$

equation 2.8 can be recast as:

$$x_{IF}(t) = x_{IF-}(t) + x_{IF+}(t). \tag{2.10}$$

The first term in 2.10, $x_{IF-}(t)$, represents the phase difference between transmitted and received signal:

$$x_{IF-}(t) = A_{\mathrm{IF-}} \cos(\phi_{IF-}(t)) = A_{\mathrm{IF-}} \cos(2\pi m t \tau - \pi m t^2 + 2\pi f_0 \tau), \tag{2.11}$$

The initial phase ϕ_0 cancels and therefore does not affect the measurement result.

Computing the derivative of $\phi_{IF-}(t)$, the instantaneous frequency of this $x_{IF-}(t)$ can be obtained:

$$f_{IF-}(t) = \frac{1}{2\pi}\frac{\mathrm{d}}{\mathrm{d}x}(\phi_{IF-}(t)) = m\tau \tag{2.12}$$

Therefore, the frequency of $x_{IF-}(t)$ is directly proportional to the time that takes the transmitted signal to return back and the chirp slope. We conclude that the distance of the target can be evaluated from instantaneous frequency of $x_{IF-}(t)$ as:

$$d = \frac{c}{2m} f_{IF-}(t) \tag{2.13}$$

This also show the importance of the sweep linearity: a static target would give a constant distance only if the slope of the chirp is also constant.

The second, additive term in 2.10, $x_{IF+}(t)$, generates an additional cosine component in $x_{IF}(t)$:

$$x_{IF+}(t) = A_{\mathrm{IF}+}\cos(2\pi(2f_0 - k\tau)t + 2\pi k t^2 + \pi m\tau^2 - 2\pi f_0\tau + 2\phi_0), \tag{2.14}$$

The instantaneous frequency is:

$$f_{IF+}(t) = 2f_0 - m\tau + 2mt, \tag{2.15}$$

which is around twice the starting frequency of the transmit sweep and can be filter before the valuation of the frequency of $x_{IF-}(t)$.

In conclusion, in a FMCW radar, the output signal of the mixer $x_{IF-}(t)$ is a sinusoidal signal which frequency bear the information on the target distance.

2.1.1 Discrete time domain

In a modern FMCW receiver, the signal $x_{IF-}(t)$ is digitized and the frequency content is usually computed using Fourier transform. An analog-to-digital converter (ADC) samples $x_{IF-}(t)$ at a constant rate $f_s = 1/T_s$, with T_s the corresponding sampling period. Setting $t = nT_s$, the sampled $x_{IF-}(t)$ signal is:

$$x_{IF-}[n] = A_{\mathrm{IF}-} \cos(2\pi m \tau n T_s + \phi_0), \tag{2.16}$$

where n is the sample index and ranges from $n = 0$ to $N - 1$. N is the total number of digitized samples. Then, normalizing the frequency to the sample frequency, $\psi_0 = f_0/f_s = f_0 T_s$, gives:

$$s_{IF}[n] = A_{\mathrm{IF}} \cos(2\pi k \psi n + \phi_0), \tag{2.17}$$

2.1.2 Maximum measurable distance

According to Nyquist theorem, only frequencies below half the sampling frequency can be represented unambiguously. Frequencies higher than $f_s/2$, after the sampling process are folded in the range from 0 to $f_s/2$. To avoid aliasing, a low pass filter with cut-off frequency at $f_s/2$ is used. This limits the maximum measurable distance. Hence, the choice of the sampling frequency $f_s/2$ in combination with the slope of the transmit frequency sweep m, determine the maximum measurable range d_{max} :

$$d_{max} = \frac{f_s}{m} \frac{c}{4}. \tag{2.18}$$

2.1.3 Resolution

If multiple targets are located within the radar beam, then the minimum achievable target resolution Δd becomes an important parameter. Basically, the problem of target resolution is a problem of resolving multiple frequencies in the FMCW output spectrum. Therefore the achievable resolution mainly depends on the frequency estimation algorithm used. For the discrete Fourier transform (DFT) the frequency resolution equals approximately one DFT bin, which is the frequency difference $\Delta f_{FFT} = f_s/N$ of two adjacent spectral lines in the discrete DFT magnitude spectrum

$$\Delta d = \frac{f_s}{N} \frac{c}{2m}. \tag{2.19}$$

With $k = B_{sw}/T_{sw} = B_{sw}/(NT_s) = (B_{sw} f_s)/N$ this simplifies to

$$\Delta d = \frac{c}{2} \frac{1}{B_{sw}}. \tag{2.20}$$

As a note, above results are valid only, if no data windows are used for computation of the DFT spectrum. If data windows are applied, their effect has to be considered, especially for the target resolution, as they broaden the target spectrum, which decreases the achievable resolution. It is possible to go beyond the resolution limit $\Delta\tau$, if model-based high resolution algorithms are applied. MUSIC and ESPRIT are only two examples that are well known in literature [15–18]. Nevertheless, the DFT is by far the most common and widest used evaluation method, due to its computational efficiency and widespread availability on many signal processing systems.

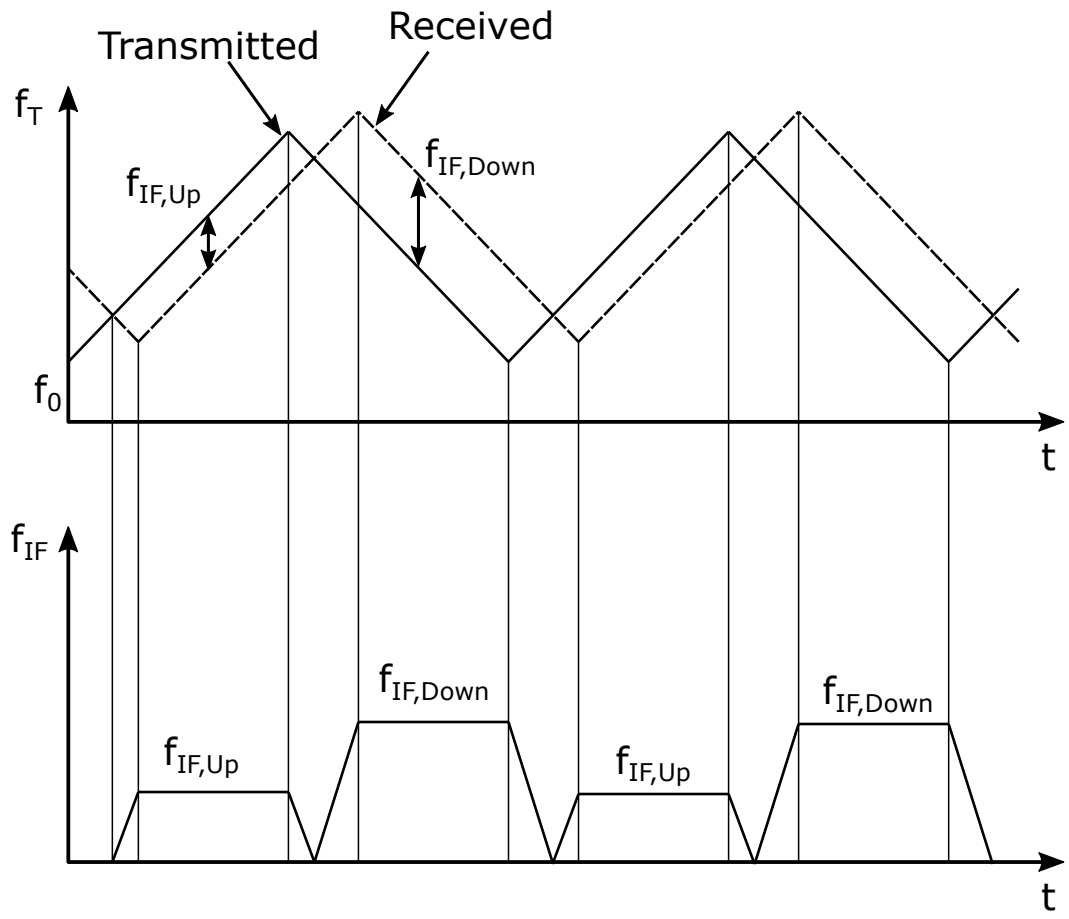


FIGURE 2.3: Transmit waveform and baseband signal of an FMCW radar.

2.2 Doppler Shift

In many application, as well in automotive, the measure of the speed of a target is an important task. A straightforward way to implement this is to use the information on two consecutive chirp cycle.

Considering a linear modulation of up and down chirps (Fig. 2.3); for a static target, the IF frequency would be the same in both interval. Instead, if the target is moving at a constant velocity v, the received signal is affected by the Doppler shift.

The Doppler shift f_D differently affects the IF frequency for up and downchirp:

$$f_{IF,up} = f_{IF,static} - f_D, \tag{2.21}$$

$$f_{IF,down} = f_{IF,static} + f_D, \tag{2.22}$$

where $f_{IF,static}$ is the IF frequency for zero velocity. Thus, combining the up and down chirp measurements, both target distance and speed can be obtained:

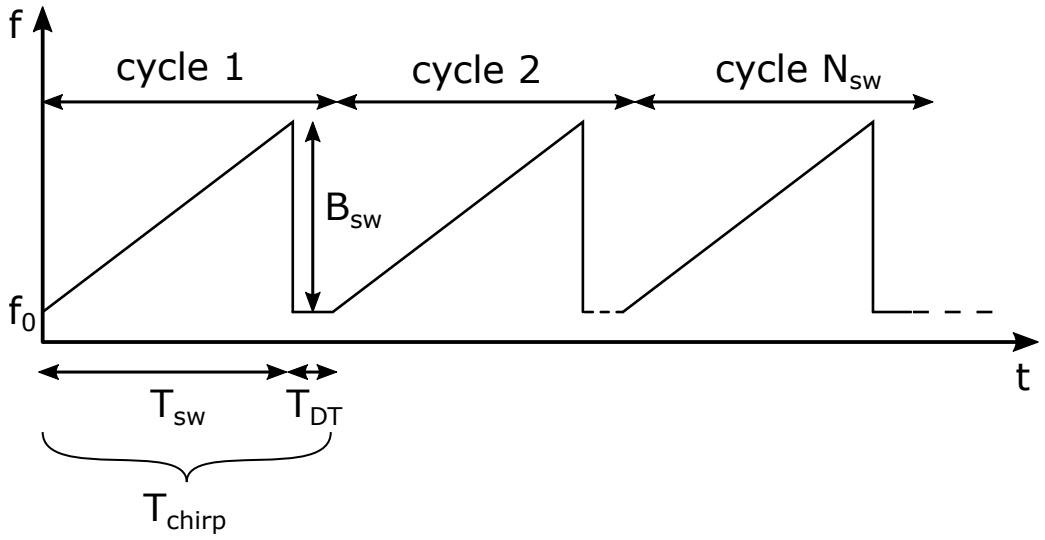


FIGURE 2.4: Weather radar antenna.

$$f_{IF,static} = \frac{f_{IF,up} + f_{IF,down}}{2}, \tag{2.23}$$

$$f_D = \frac{f_{IF,up} - f_{IF,down}}{2}, \tag{2.24}$$

Since the target distance changes during the measurement, this results in an average position estimate.

2.3 Range-Doppler Map

A different approach to measure the speed of a target uses the so called Range-Doppler Map. For range-Doppler processing, a sequence of N_{sw} consecutive up- or downchirps is used to interrogate the target scenario. A typical sequence is shown in Fig. 2.4, where, in a practical application, the sweep time ,T_{sw}, is followed by a dead time T_{DT} needed for the reset of the system; the total chirp period is $T_{chirp} = T_{sw} + T_{DT}$. The calculation of the range and velocity information using a range-Doppler map is done in a two-step process, using 2-dimensional DFT processing.

For a target moving at a constant speed the round trip delay time (RTDT) change during the observation period, as:

$$\tau(t) = \tau_0 + \frac{2v}{c}t \tag{2.25}$$

with τ_0 the initial RTDT at initial distance d_0. If we insert this into 2.11 and expand the terms we obtain:

$$\begin{aligned}\phi_{IF}(t) =& 2\pi\left(m\tau_0 - m\frac{2v}{c}\tau_0 + f_0\frac{2v}{c}\right)t + \\ &+2\pi m\left(\frac{2v}{c} - 2\left(\frac{2v}{c}\right)^2\right)t^2 + 2\pi f_0\tau_0 - \pi m\tau_0^2.\end{aligned} \tag{2.26}$$

For v«c, can be approximate as:

$$\phi_{IF}(t) \approx 2\pi\left(m\tau_0 + f_0\frac{2v}{c}\right)t + 2\pi m\left(\frac{2v}{c}\right)t^2 + 2\pi f_0\tau_0, \tag{2.27}$$

thus, the IF frequency is:

$$f_{IF}(t) \approx m\tau_0 + f_0\frac{2v}{c} + 2m\frac{2v}{c}t, \tag{2.28}$$

where:

- $m\tau_0$ gives the distance at the of the start chirp cycle;
- $f_0\frac{2v}{c}$ is the Doppler frequency f_D
- $2m\frac{2v}{c}t$ describes the linear change of the RTDT due to the movement of the target during the interrogation sweep.

Thus, the IF signal consist of a constant frequency $f_{0,IF}$, which is set by the range-dependent component $m\tau$ and the Doppler frequency f_D, and a chirping term caused by the movement during the interrogation sweep. It can be shown that this last term is negligible compared to the Doppler frequency; the maximum IF offset caused by the chirping component is at the end of chirp period, when $t = T_{sw}$:

$$f_{chirpmax} = 2m\frac{2v}{c}T_{sw}. \tag{2.29}$$

Then:

$$f_D > f_{chirpmax} \iff f_0 > 2B_{sw}. \tag{2.30}$$

which is commonly fulfilled in practice.

In summary, neglecting the second order terms, the frequency term of the extended signal model for moving targets contains the average distance info (average position of the target during the sweep) and the average Doppler frequency due to the target movement.

A range-Doppler map is calculated from a sequence of N_{sw} single FMCW sweeps as shown in Fig. 2.4, acquiring N data samples in each frequency

sweep. In the first step the IF data is arranged in form of a 2D data matrix $X[n,m]$, with the single sweep data vectors $x_i[n]$ as column elements.

Now, for each data vector x_i, the complex-valued spectrum y_i is calculated via DFT, as if evaluating N_{sw} single FMCW radar measurements. From the individual spectrum, the position of the targets can be obtained, this is called the range compression. The complex-valued result vectors y_i are, then, arranged in matrix form $Y[k,l]$. In practice, due to the zeropadding, the dimension of Y can be larger than X.

In the second step of the range-Doppler processing the velocity information is extracted from the range-compressed result. Therefore the phase difference of the consecutive sweeps is evaluated. Whereas the IF frequency – consisting mainly of the target range and Doppler shift – is almost equal on all sweeps, the phase information is much more sensitive on the small position changes in subsequent sweeps.

From 2.27 we can write the expression of the IF signal:

$$x_{IF}(t) = A_{IF}\cos\left(2\pi\left(m\tau_0 + f_0\frac{2v}{c}\right)t + 2\pi f_0\tau_0\right) \tag{2.31}$$

Each entries in the range compression map is in the form:

$$Y[k,l] = A_{k,l}exp(j\Phi_{0,k,l}) \tag{2.32}$$

with $A_{k,l}$ the magnitude and $\Phi_{0,k,l}$ the phase value of the corresponding spectral sample. According to 2.31, the initial phase, at the starting of the chirp cycle, now depends only on τ_0. From 2.25 the difference of the RTDT between two consecutive chirp cycle, $\Delta\tau_0$, is given by:

$$\Delta\tau_0 = \frac{2}{c}vT_{chirp} \tag{2.33}$$

Therefore, the phase offset of the target response is:

$$\Delta\Phi_0 = 2\pi f_0\Delta\tau_0 = 2\pi\frac{2f_0v}{c}T_{chirp} \tag{2.34}$$

Inverting this relation we estimate the velocity of the target:

$$v = \frac{\Delta\Phi_0 c}{4\pi f_0\Delta\tau_0 T_{chirp}}, \tag{2.35}$$

Unfortunately, since the phase is 2π ambiguous, this formula can give erroneous results if only single phase are evaluated. Instead, the phase variation is investigated in all N_{sw} measurements. If in the range compressed

matrix, $Y[k,l]$ the data row ζ containing the target response is analyzed, this row:

$$Y[\zeta,l] = [A_{\zeta,1}\exp(j\Phi_{0,\zeta,1})A_{\zeta,2}\exp(j\Phi_{0,\zeta,2})\dots A_{\zeta,N_{sw}}\exp(j\Phi_{0,\zeta,N_{sw}})] \quad (2.36)$$

can be interpreted as a complex exponential vector

$$z[m] = A_\zeta \exp(j\Delta\Phi_0 m) = A_\zeta \exp(j2\pi\frac{2f_0v}{c}T_{chirp}m). \quad (2.37)$$

Here, A_ζ is the magnitude of the target cell in the range compressed result, which is assumed to be equal on all interrogation sweeps. Then, the normalized frequency is given by:

$$\psi_\zeta = \frac{2f_0v}{c}T_{chirp}, \quad (2.38)$$

and is evaluated by DFT. Finally, the velocity calculates to

$$v = \psi_\zeta \frac{c}{2f_0vT_{chirp}}. \quad (2.39)$$

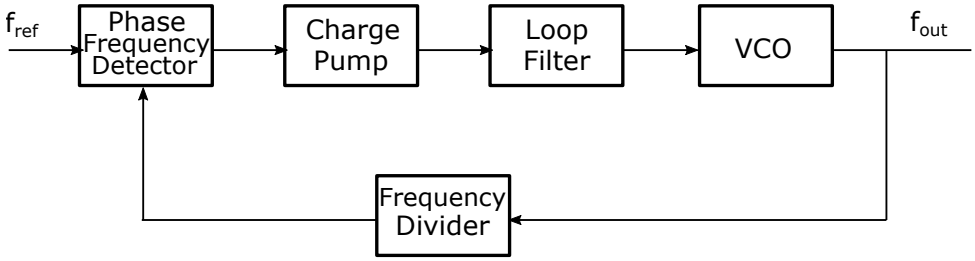


FIGURE 2.5: Block diagram of a phase-locked loop.

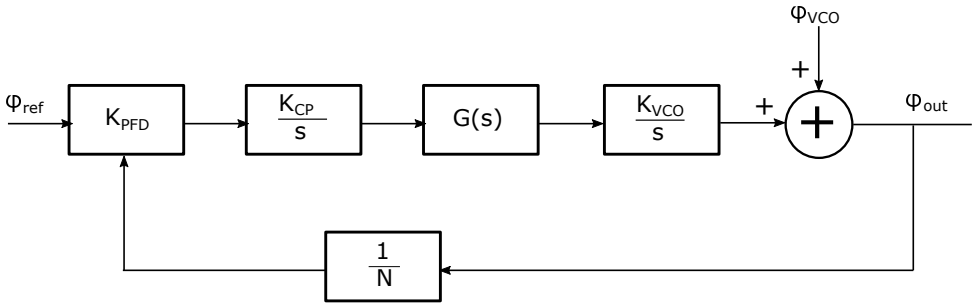


FIGURE 2.6: Linearised model a phase-locked loop.

2.4 Frequency Synthesizer

Because of the phase noise performance, frequency synthesizers are customary realized as phase-locked loop. Figure 2.5 shows the block diagram of a Type 2 PLL with charge pump.

It is possible to derive a linearised model of the PLL, as in Fig.2.6 where ϕ_{VCO} is the noise introduced by the VCO.

The transfer function between ϕ_{VCO} and the output is in the form:

$$\frac{\phi_{out}}{\phi_{VCO}}(s) = \frac{1}{N}\frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.40}$$

The effect of the loop on the VCO noise is showed in Fig.2.7. So it's clear that outside the loop bandwidth, defined by the loop filter, the noise of the VCO is not altered.

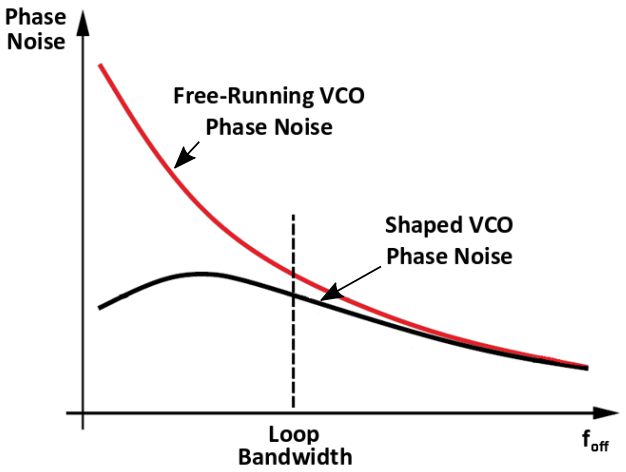


FIGURE 2.7: Shaped VCO phase noise in a PLL.

2.5 Conclusions

The principle of operation of a linear frequency modulated continuous waveform radar has been presented.

It is important to reduce the phase noise of the voltage controlled oscillator as this leads to an uncertainty of the oscillation frequency, thus an error in the measurements of the radar.

Chapter 3

Optimal Operation Frequency to Minimize Phase Noise in Integrated Harmonic Oscillators

3.1 introduction

The minimization of the phase noise in integrated oscillators is a key goal in the design of many systems, covering applications that span from wireless and wireline communications to radar, sensing, imaging, etc. To achieve higher spectral purity, LC harmonic oscillators are costumarily preferred over ring or relaxation oscillators [19–23]. With the development of the 5G cellular network, the increasing interest in anticollision, security, and imaging radars, and the ever increasing data rate of optical networks, the need for frequency synthesizers in the mm-wave range is compelling [24–28]. The question then arises whether, for a target local oscillator (LO) frequency f_{LO}, it is preferable, in the perspective of phase noise minimization, to design a fundamental oscillator at f_{LO}, as shown in Fig. 3.1(a), or, rather, to run the oscillator at a lower frequency $f_{\mathrm{osc}} = f_{\mathrm{LO}}/N$, and then use a frequency multiplier by N to obtain the desired LO frequency, as illustrated in Fig. 3.1(b).

In this chapter, we study the most appropriate frequency of operation for the oscillator, as well as the optimal selection of the tank components to minimize the circuit phase noise for a given technology. We develop a simple, yet fairly accurate scalable model of the LC tank, that takes into account the dependence of the main parasitic elements on the inductance value, allowing to investigate their impact on the oscillator performance as f_{osc} is swept. Moreover, this chapter highlights that a design for minimum phase noise and a design aimed at optimizing the oscillator figure-of-merit (i.e. minimizing the power consumption for a given phase noise level) are not always coinciding. In particular, it shows that the maximization of the tank quality factor may

not be the best option if phase noise is to be minimized regardless of power consumption. This is the opposite of what is pursued in most oscillator designs, that typically aim at the optimization of the tank quality factor as a primary design goal.

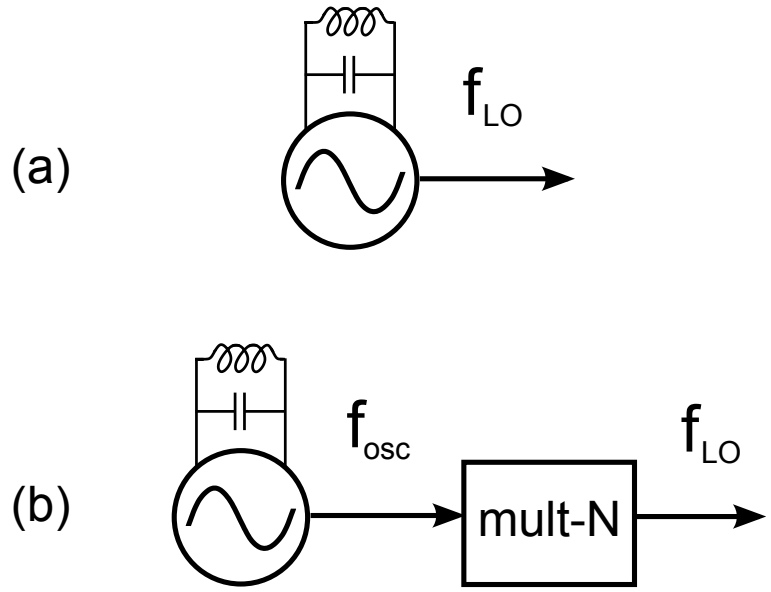


FIGURE 3.1: Different architectures to synthesize frequency f_{LO}: (a) fundamental oscillator; (b) oscillator followed by a frequency multiplier.

3.2 Phase Noise Optimization

To keep the analysis effective, we focus our study on the phase noise due to the upconversion of the white noise generated by the tank losses and by the active devices in the oscillator, neglecting the $1/f$ noise sources. Further, we assume that the frequency multiplier introduces negligible noise in the system. The phase noise requirement for the LO at an offset frequency Δf is then [29–33]:

$$\mathcal{L}(\Delta f) = 10 \log_{10} \left[\frac{kTF}{V_0^2} \frac{R_T}{Q_T^2} \left(\frac{f_{LO}}{\Delta f} \right)^2 \right], \tag{3.1}$$

where Q_T is the overall tank quality factor, R_T is the equivalent parallel tank resistance at resonance, V_0 is the amplitude of oscillation and F is the oscillator excess noise factor.

As we reduce the oscillator frequency from f_{LO} to f_{osc}, all other oscillator parameters being the same, the phase noise decreases by a factor N^2, as the explicit frequency dependence in (3.1) shows. However, after the frequency multiplication necessary to recover f_{LO}, the N^2 advantage is lost. In conclusion, the term in parenthesis in (3.1) does not impact the oscillator performance as f_{osc} is changed. The oscillator excess noise factor F depends, at first order, only on the oscillator topology, and thus it is also independent on f_{osc}. A large amplitude of oscillation is clearly instrumental to minimize the phase noise. As a consequence, we assume that the oscillator is designed to

maximize V_0 for the given supply voltage, independently of the frequency of operation.

In conclusion, the only term that changes with f_{osc} in (3.1), and is to be minimized, is R_T/Q_T^2. This parameter depends only on the tank components, and can be interpreted as a resistance that, set in series to the tank inductance, accounts for all the tank losses, both inductive and capacitive. The tank losses are dominated by the inductor at low frequency, and by the capacitor at higher frequency, such that there is an optimal choice of f_{osc} that minimizes the phase noise.

To complete the picture, it is worth reminding that the oscillator performance is also usually gauged by the power-frequency-normalized figure-of-merit (FoM) [19, 29]:

$$\begin{aligned} FoM &= \mathcal{L}(\Delta f) - 10\log_{10}\left[\frac{1}{P_{\text{DC}}}\left(\frac{f_{\text{LO}}}{\Delta f}\right)^2\right] \\ &= -174\text{dBc/Hz} - 10\log_{10}\left(\frac{2Q_T^2\eta_P}{F}\right), \end{aligned} \tag{3.2}$$

where P_{DC} is the LO power consumption normalized to 1 mW, and η_P is the efficiency of the dc to rf power conversion. For a well designed oscillator, the power efficiency is independent on f_{osc}. In case $f_{\text{osc}} < f_{\text{LO}}$, the power consumption of the required frequency multiplier by N will of course decrease η_P, in a way that, however, cannot be trivially related to f_{osc}. Nonetheless, a larger frequency multiplication ratio is expected to result in a larger multiplier power consumption. For sure, the FoM benefits of a larger tank quality factor, such that we will study the dependence of Q_T on f_{osc} to investigate how the FoM varies with f_{osc}.

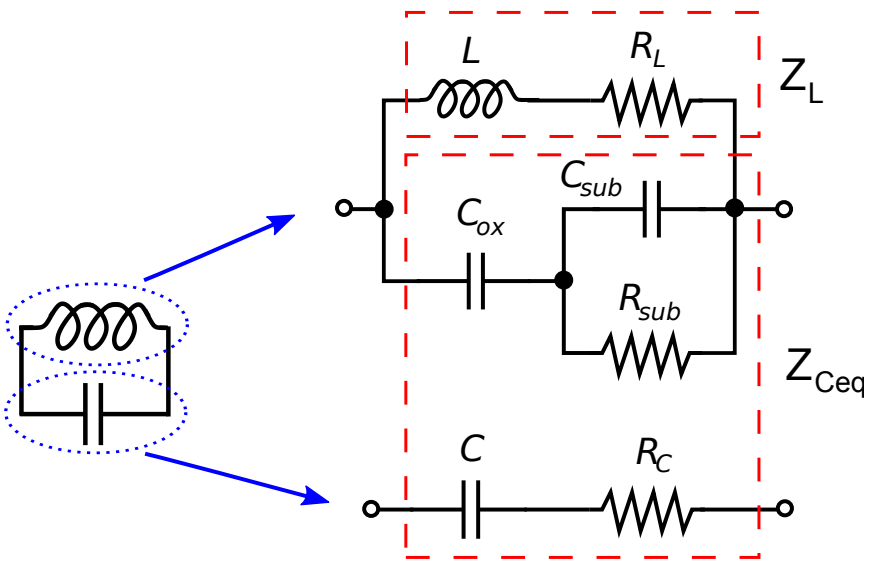


FIGURE 3.2: Proposed scalable tank model.

3.3 Scalable Tank Model

The operation frequency of the oscillator, f_{osc}, is related to the tank capacitance C and inductance L as

$$f_{\text{osc}} = \frac{1}{2\pi\sqrt{L(C+C_p)}} = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{\delta^2-1}{\delta^2}}, \tag{3.3}$$

where $\delta = f_{\text{srf}}/f_{\text{osc}}$ is the ratio between the inductor self resonance frequency, $f_{\text{srf}} = 1/(2\pi\sqrt{LC_p})$, and the oscillation frequency. C_p is the inductor parasitic capacitance. For a given value of f_{osc} the choice of L and C is not unique. Therefore, in order to investigate the trade-offs related to the choice of the tank components, it is necessary to develop a simple model that captures the dependence of the parasitic elements of the tank on the selected values of L and C.

The proposed scalable model for the tank is depicted in Fig. 3.2. The inductor equivalent circuit is a simplification of a conventional 9-element π-model [34]. It is made of two parallel branches. The inductive branch, L-R_L, takes into account the desired inductive behavior of the component and the trace losses. The capacitive branch, made of C_{ox}, C_{sub} and R_{sub}, models the capacitive coupling of the inductor to the substrate, and the related losses.

The resistance R_L takes into account the losses associated to the inductor trace. Since the trace length increases with L, so must R_L. Moreover, due to the skin effect, R_L must increase with frequency. The proposed model for R_L

is:

$$R_L = \alpha_1 R_{\text{ref}} \left(\frac{L}{L_{\text{ref}}}\right)^{\alpha_2} + \\ + (1-\alpha_1) R_{\text{ref}} \left(\frac{L}{L_{\text{ref}}}\right)^{\alpha_3} \left(\frac{f_{\text{osc}}}{f_{\text{ref}}}\right)^{\alpha_4}, \tag{3.4}$$

where R_{ref} and $\alpha_{1,\dots,4} \leq 1$ are fitting parameters. The first term in (3.4) is the dc resistance of the inductor, while the second models the skin effect. Equation (3.4) is written such that, for a reference inductance L_{ref} at a reference frequency f_{ref}[1], the parameter α_1 represents the ratio of the dc resistance over the overall loss resistance R_{ref}.

The capacitive coupling to the substrate is assumed to scale linearly with the inductance value. Therefore:

$$C_{ox} = K'_{c_{ox}} L \tag{3.5}$$

and

$$C_{sub} = K'_{c_{sub}} L. \tag{3.6}$$

Likewise, the resistance modeling the substrate losses is assumed to be inversely proportional to L:

$$R_{sub} = \frac{K'_{r_{sub}}}{L}. \tag{3.7}$$

$K'_{c_{ox}}$, $K'_{c_{sub}}$ and $K'_{r_{sub}}$ in (3.5)–(3.7) are fitting parameters. The parasitic capacitance setting the inductor self-resonance frequency is consequently estimated as

$$C_p \approx \frac{C_{\text{ox}} C_{\text{sub}}}{C_{\text{ox}} + C_{\text{sub}}} = \frac{K'_{c_{sub}} K'_{c_{ox}}}{K'_{c_{sub}} + K'_{c_{ox}}} L = \gamma\, L. \tag{3.8}$$

The explicit tank capacitor[2] is simply modelled as a C-R_C branch (see Fig. 3.2), that takes into account the limited quality factor of the capacitor. The capacitor quality factor is assumed to be independent from the capacitance value. Hence, the product $\tau_C = R_C\, C$ is constant with respect to the value of the tank capacitance.

[1] Both L_{ref} and f_{ref} can be chosen arbitrarily.

[2] The explicit capacitor may be fixed or variable (e.g. made of a varactor or a switched capacitor bank).

3.4 Choice of Tank Components

As underlined in the foregoing discussion, the choice of the tank parameters, L and C, for a given frequency of oscillation is crucial. Moreover, once a design choice is made for a given value of f_{osc}, a scaling strategy must be devised to adapt the tank components as f_{osc} is changed. Since the tuning range, along with the phase noise and FoM, is an important aspect of the design of an oscillator, we consider designs where the maximum achievable tuning range is preserved while the operation frequency is changed. As a consequence, we assume that the ratio between the inductor self-resonance frequency, f_{srf}, and the frequency of oscillation, f_{osc}, that is the parameter δ in (3.3), is kept constant. For any value of δ, then, the tank inductance and capacitance values are chosen using (3.3), and considering (3.8), as:

$$L = \frac{1}{2\pi f_{\text{osc}}\,\delta\,\sqrt{\gamma}} \tag{3.9}$$

and

$$C = \gamma\,L\,(\delta^2 - 1), \tag{3.10}$$

where γ is implicitly defined by (3.8). Equations (3.9) and (3.10) show that if the oscillation frequency is increased by M times, both the tank inductance and capacitance are to be decreased by M.

3.4.1 Tank Quality Factor and Equivalent Resistance

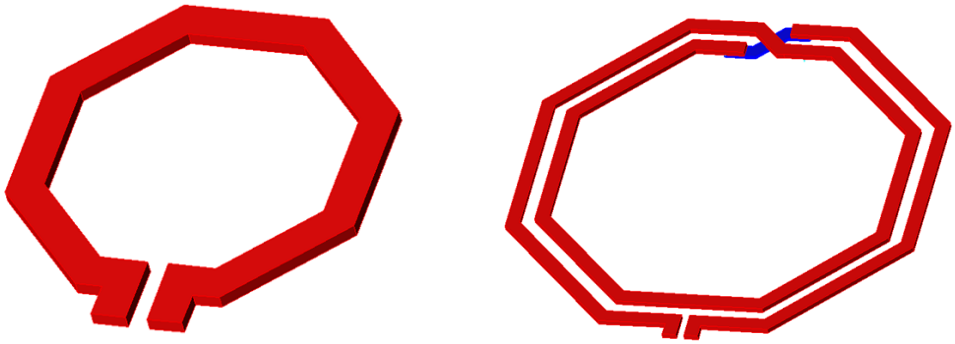
To correctly compute the tank quality factor and the equivalent parallel resistance, it is useful to separate the capacitive from the inductive reactances. In fact, for an impedance with only one type of reactive behavior the quality factor is simply the ratio between its imaginary and real part [35, 36]. Consequently, the tank equivalent circuit is split, as shown in Fig. 3.2, in Z_L, that takes into account the inductive portion of the tank (and its losses), and Z_{Ceq}, which combines the explicit tank capacitor and the inductor parasitic capacitance. Once the quality factor of Z_L, Q_L, and of Z_{eqC}, Q_{eqC}, are estimated, the overall tank quality factor is obtained as:

$$Q_T = \left(\frac{1}{Q_L} + \frac{1}{Q_{\text{eqC}}}\right)^{-1}. \tag{3.11}$$

Similarly, the equivalent parallel tank resistance is given by:

$$R_T = \left[\frac{1}{R_L(1+Q_L^2)} + \frac{1}{R_{\mathrm{Ceq}}(1+Q_{\mathrm{eqC}}^2)} \right]^{-1}. \tag{3.12}$$

where R_{Ceq} is the real part of Z_{Ceq}.



(A) (B)

FIGURE 3.3: A) Single turn (L: 41÷622pH) and B) double turn inductors (L: 949÷1860pH).

3.5 Discussion of a Case Study

As a case study, an ultra-scaled digital CMOS technology has been investigated. A set of inductors has been designed and electro-magnetic simulations have been carried out, as showed in Fig.3.3. The inductors are implemented in the top metal layer, and have an octagonal shape with trace width of 10 μm. There are two sets of inductors. The first is made of single-turn coils with an external diameter that spans from 50 to 160 μm in 10 μm steps, plus two coils with a 200 and 300 μm diameter. The corresponding inductance values range from 41 to 622 pH. The second set is made of two-turn coils with 10 μm inter-turn spacing, and 200, 250, and 300 μm diameter, corresponding to 949, 1380, and 1860 pH inductance.

The parameters of the scalable equivalent model discussed in Section 3.3 have been extracted by means of nonlinear fitting, and are reported in Table 3.1. The reference frequency and reference inductance (whose choice is entirely arbitrary) are $f_{\text{ref}} = 10\,\text{GHz}$ and $L_{\text{ref}} = 150\,\text{pH}$.

Figure 3.4 compares the values of R_L obtained by means of electro-magnetic simulations with those given by (3.4), showing good agreement.

The quality factor of the available capacitors has been assessed using the technology design kit: the parameter τ_C has been estimated to be equal to $\tau_C = 4 \cdot 10^{-13}\,\text{s}$, corresponding to a quality factor of 40 at 10 GHz for the capacitor.

The sizing approach discussed in Section 3.4 has been applied leveraging the extracted model parameters. The obtained values of tank inductance and capacitance are shown in Figs. 3.5a and 3.5b, respectively, for different values of the parameter δ spanning from 3 to 15. As previously discussed, both tank inductance and capacitance are scaled down as the frequency of operation is

TABLE 3.1: Extracted parameters for the proposed scalable model.

α_1	α_2	α_3	α_4
0.29	0.81	0.49	0.67

R_{ref} [Ω]	$K'_{c_{ox}}$ [F/H]	$K'_{c_{sub}}$ [F/H]	$K'_{r_{sub}}$ [Ω· H]
0.42	$4.24 \cdot 10^{-5}$	$1.28 \cdot 10^{-5}$	$1.65 \cdot 10^{-7}$

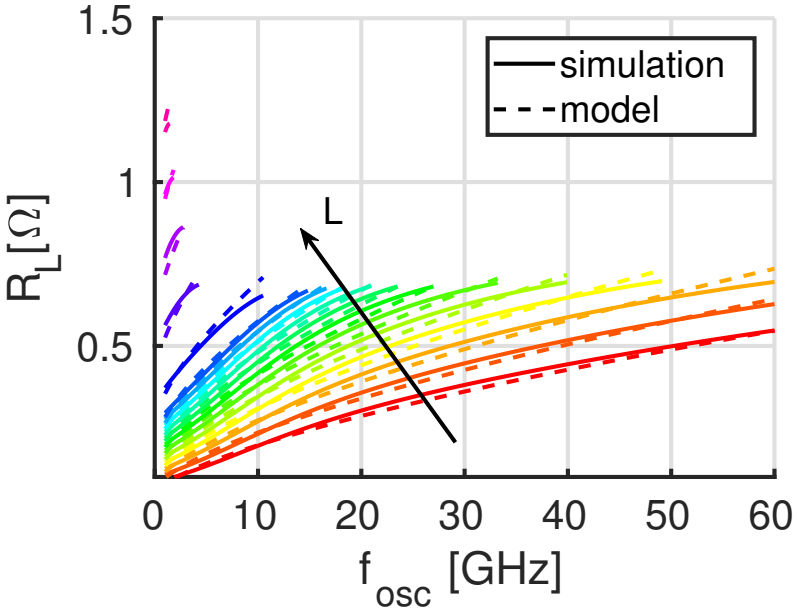


FIGURE 3.4: Estimated trace loss resistance of the designed inductors: electro-magnetic simulation (solid line), and proposed scalable model (dashed line).

increased. Next, the parasitic elements of the tank components are computed based on (3.4)–(3.7). Finally, R_T and Q_T are derived using (3.11) and (3.12).

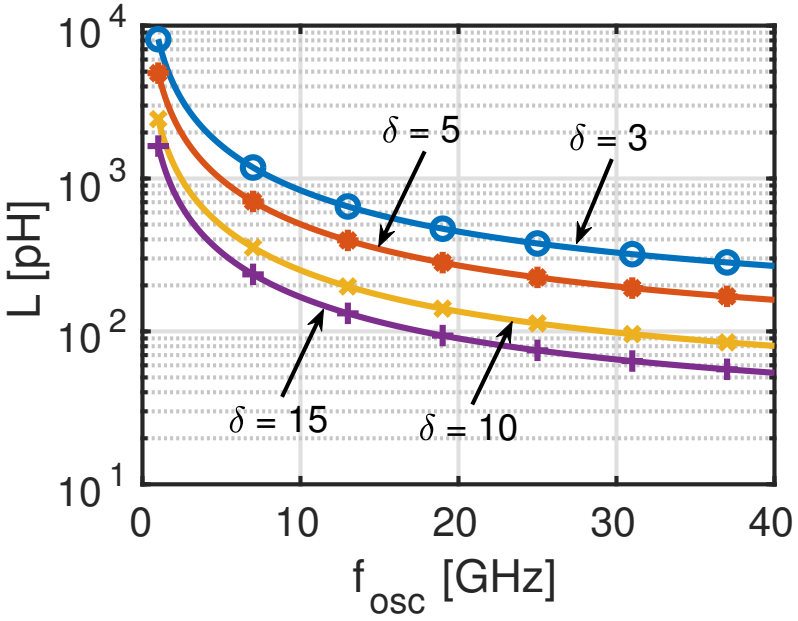
Figure 3.6 shows R_T/Q_T^2 as a function of f_{osc} for different values of δ in a logaritmic scale. All the curves reach a minimum in the neighborhood of an operating frequency of 5 GHz. This suggests that the frequencies around 5 GHz are the optimal range where the oscillator should operate to minimize phase noise for the considered technology. It must be noted, however, that the phase noise degradation resulting from moving to higher frequencies, say 20 GHz, is limited to some 3 dB, and can be compensated by designing for lower inductance values, i.e. higher values of δ. Clearly, there is a limit to the minimum inductance value achievable in practice.

A comparison between the results of the proposed scalable model (solid lines) and circuit-level simulations (markers) is also reported in Fig. 3.6. In the circuit-level simulations the results of the electro-magnetic simulations of the designed coils are combined with the design kit models of the capacitors. In Fig. 3.6, a good agreement between calculations and simulations is observed, which validates the proposed scalable model.

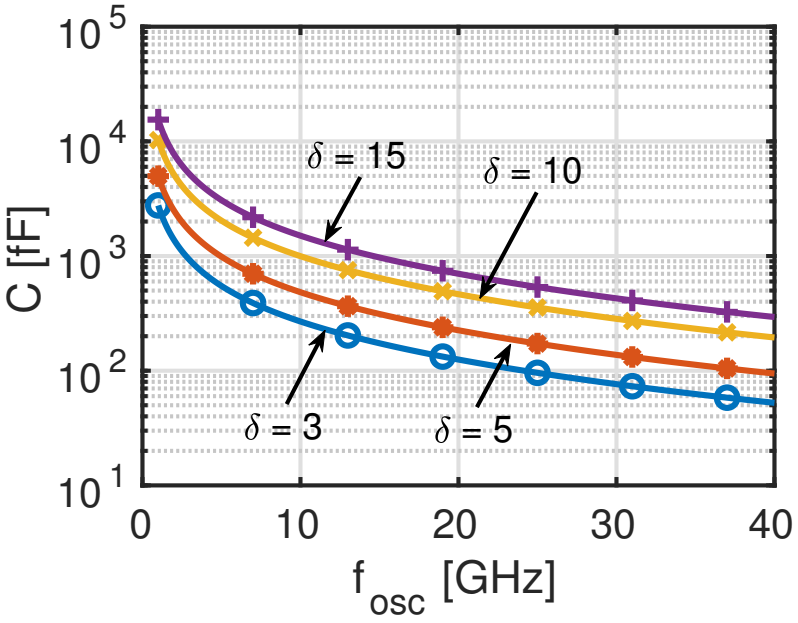
The estimated tank quality factor, obtained using the scalable equivalent model, is illustrated in Fig. 3.7 as f_{osc} is swept, having δ as a parameter. Q_T has a peak that, for all considered values of δ with the notable exception of $\delta = 3$, is close to 5 GHz, confirming that this frequency must be the sweet spot for the technology used in this case study.

A comparison between the proposed model and circuit-level simulations is reported in Fig. 3.8, where the estimated Q_T is compared in the two cases. The solid lines refer to the calculations using the scalable model, while the markers are the simulation results. For clarity, only the results for two values of δ are illustrated, namely $\delta = 5$ in Fig. 3.8(a), and $\delta = 15$ in Fig. 3.8(b). The good agreeement between calculations and simulations confirm that, despite its simplicity, the proposed scalable model is able to capture the tank behaviour as f_{osc}, and thus the values of tank inductance and capacitance, are changed.

In Fig. 3.7, it must be observed that Q_T, and thus the FoM, tends to improve with larger values of inductance (that is smaller values of δ), such that in a design where low power consumption is the primary goal the inductance value should be maximized, in the limit of the constraints set by the required tuning range. The losses associated with the inductor coupling to the substrate set another limit to the maximum inductance value. At large inductance values they become dominant, leading to a Q_T degradation. This is



(A)



(B)

FIGURE 3.5: Tank components for different values of $\delta = f_{srf}/f_{osc}$: (a) inductance; (b) capacitance.

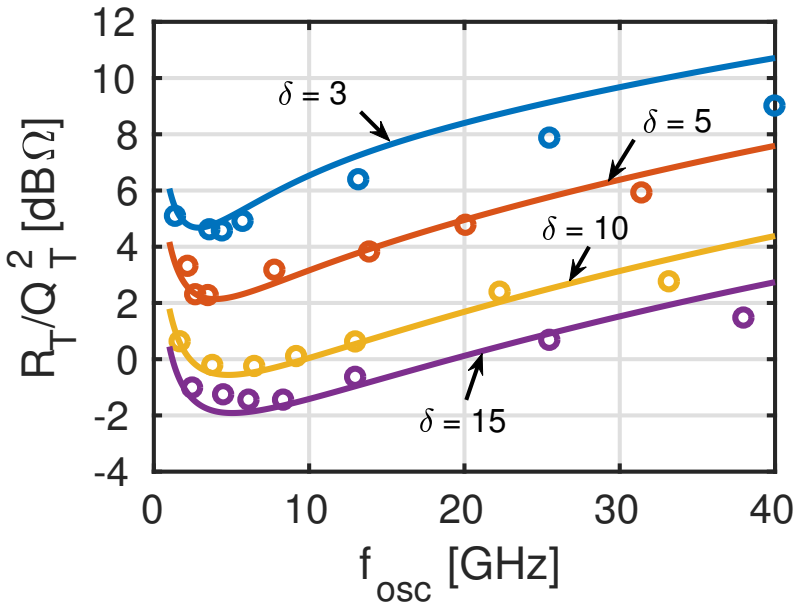


FIGURE 3.6: Plot of R_T/Q_T^2 for different values of δ=f_{srf}/f_{osc}: calculation using the proposed model (solid lines) and simulation (markers).

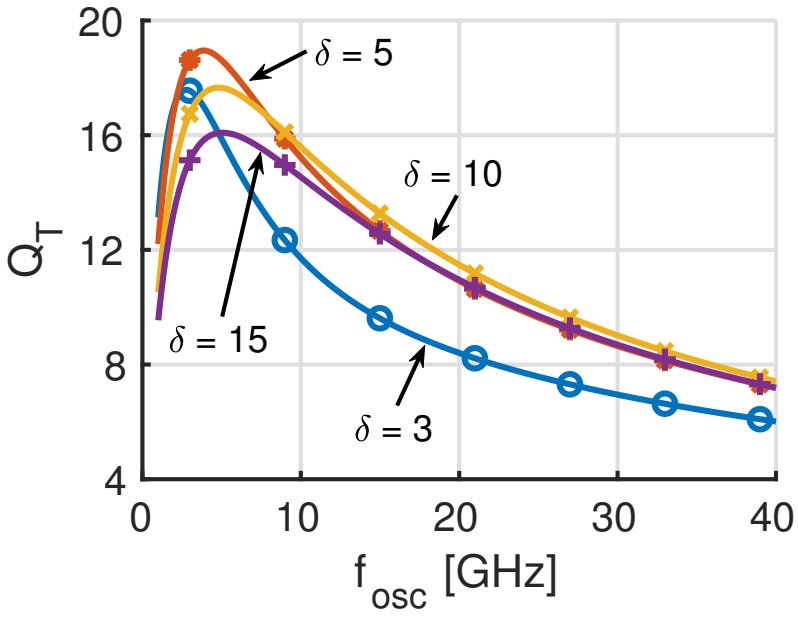
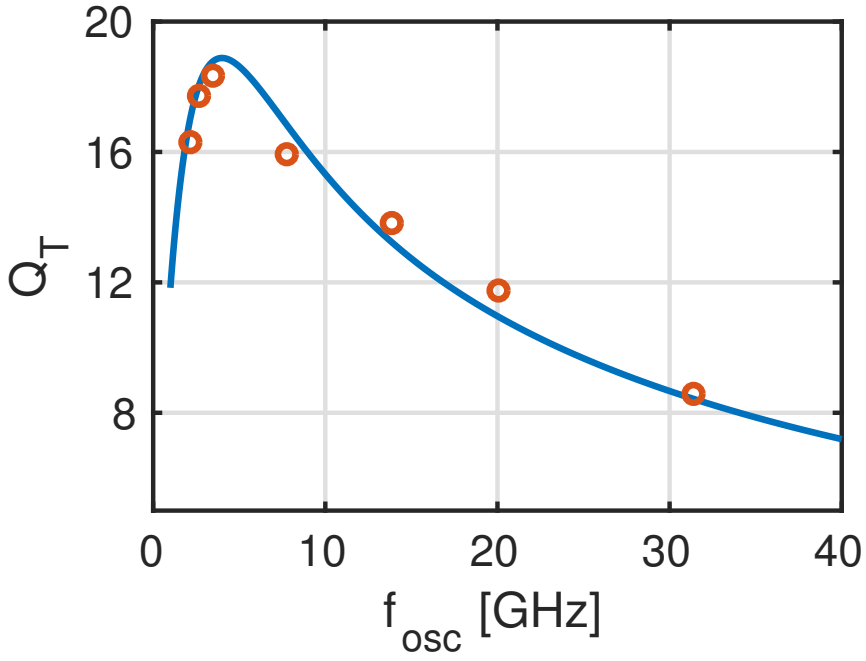


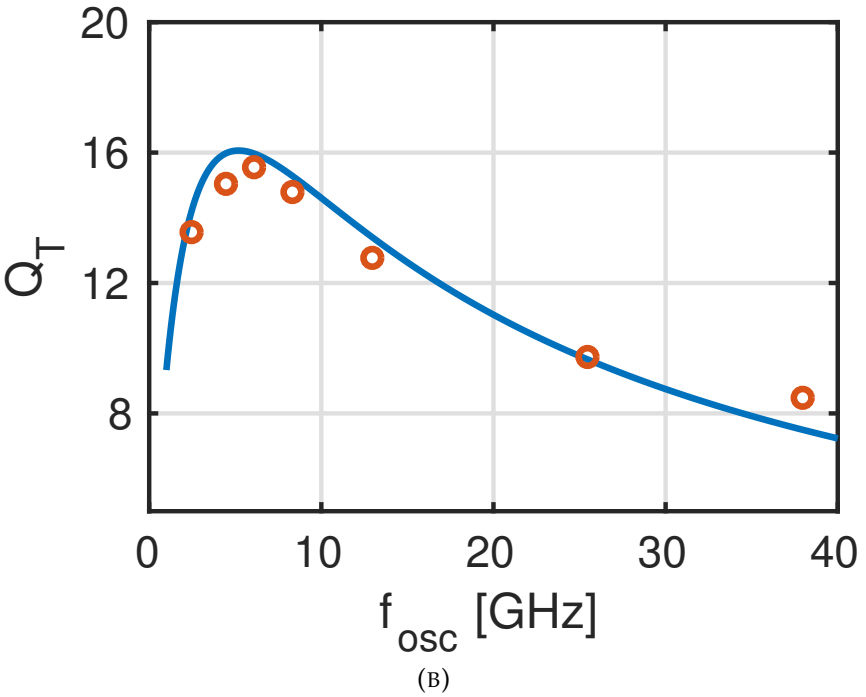
FIGURE 3.7: Plot of the quality factor Q_T for different values of δ=f_{srf}/f_{osc}.

the case of the curve with $\delta = 3$ in Fig. 3.7. If minimum phase noise is sought, instead, R_T/Q_T^2 is to be minimized, designing for low inductance values (and higher values of δ). Therefore, for minimum phase noise low inductances are to be selected, even if this leads to a decrease in the (peak) Q_T.

This apparently obvious result is in contrast with common design approaches finalized at FoM optimization, even when minimum phase noise is needed. The underlining assumption of such a strategy is that once the FoM is optimized, any phase noise level can be achieved by trading it for higher power consumption. This is indeed true if the oscillator is operating in the current-limited regime, that is if the amplitude of oscillation (V_0) is lower than the maximum attainable. In that condition, the tank values are kept constant, and lower phase noise is achieved by increasing the oscillator bias current (consequently increasing V_0). However, in a low noise design, V_0 is set to its maximum, limited by the voltage supply and by the oscillator topology. Hence, the only way to decrease the phase noise is to decrease the tank inductance, even if this results in a degradation of Q_T. The results in Figs. 3.6 and 3.7 show that this approach (i.e. designing for higher δ) is indeed effective, despite it leads to lower values of Q_T.



(A)



(B)

FIGURE 3.8: Quality factor Q_T comparison as calculated using the proposed model (solid lines) and simulation (markers): (a) $\delta = 5$; (b) $\delta = 15$.

3.6 Conclusions

A methodology to single out the optimal frequency of operation to minimize phase noise in harmonic integrated oscillators is discussed in this chapter. It is based on a scalable model of the resonator that takes into account the dependance of the parasitic elements on the inductance value, and on a strategy to scale the tank components as the frequency of operation is changed. A case study, based on an ultra scaled CMOS technology, points out 5 GHz to be such an oscillation frequency for minimum phase noise. Moreover, has been shown that a design for minimum phase noise and a design for best FoM are not always coincident, contrary to common belief and practice. As a matter of fact, the optimization of the tank quality factor may not be the ultimate goal, if phase noise minimization is the priority.

Chapter 4

VCOs Design: Class-B/D and Class-C

In chapter 3 we have developed a methodology to find the optimal operation frequency for an harmonic oscillator. At this frequency, the phase noise due to white noise sources is minimized. With the technology available to us, this frequency is around 5 GHz. As we saw, due to regulations, the band allocation for next generation of automotive radar is between 76 to 81 GHz (76-77 GHz for the long range radar while 77-81 GHz for the short and medium range). Therefore, an oscillator working at 5 GHz would require a frequency multiplication by a factor of 16. The design of such multiplier can be difficult, it may occupies large area and dissipates lot of power. Furthermore, it generates many harmonic spur signals that can potentially invalidate the operation of nearby circuits. For this reason, as compromise between complexity of the design and phase noise performance, 20 GHz has been chosen as the center frequency for VCO. This would require a frequency multiplication of 4.

In this chapter a class-B/D oscillator will be presented first. Then, based on the measurement results, and the results of a comparison between a class-B and class-C oscillators about flicker noise upconversion, the design of a class-C oscillator will be presented.

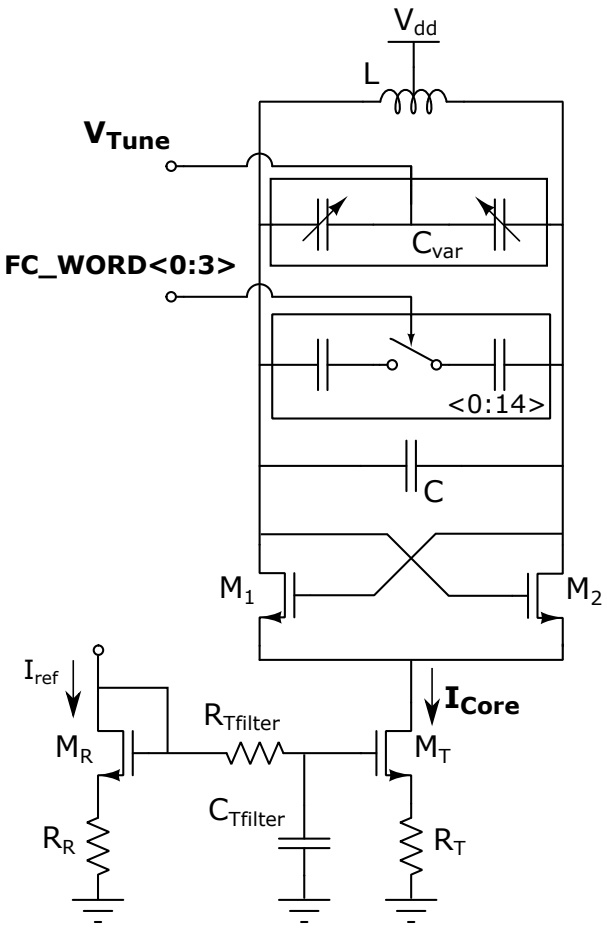


FIGURE 4.1: Schematic of the proposed class-B/D oscillator.

4.1 Class-B/D VCO

4.1.1 Design

In an effort to design a 20 GHz voltage-controlled oscillator an hybrid class-B/D has been designed.

Figure 4.1 shows the schematic of the proposed oscillator. The schematic resembles that of a class-B oscillator with a nMOS cross-couple pair, but with a notable difference: the resistive degeneration of the tail current generator; which has been added to reduce the noise of the tail generator.

When the oscillator is biased with a low I_{Core} current, both M_{T} and M_{R} are biased in saturation region, providing high impedance of the source of the cross-coupled pair to ground, therefore, the oscillator operates in class-B. As I_{Core} is increased, the voltage drop on R_{T} and the common source voltage push M_{T} in triode region, therefore, reducing its output resistance. The tail generator degenerates in the combination of a MOS switch and a resistor, and the cross-coupled pair operates in class-D, helped in that by the large

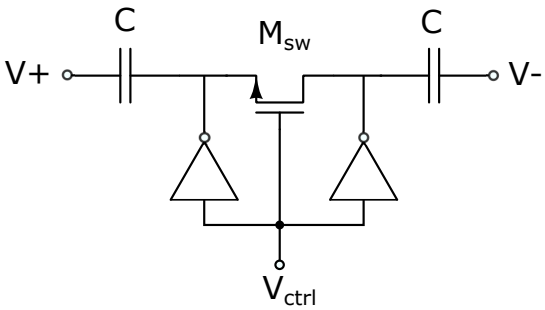


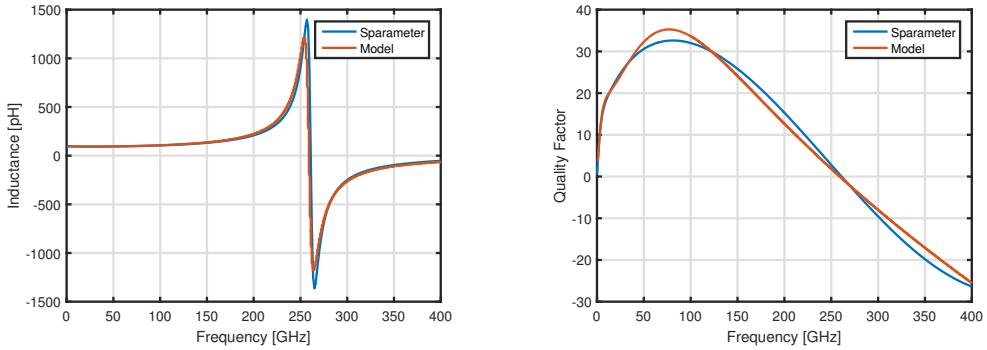
FIGURE 4.2: Schematic of the capacitor bank unit cell.

parasitic capacitance at its common source node. The name class-B/D stems from this behaviour.

The class-D operation allows to maximize the oscillation amplitude (up to three times the supply voltage [37]) which is beneficial to minimize the phase noise in the $1/f^2$ region. So the best phase noise performance are expected in this condition.

The tank has been sized in order to minimize the ratio $R_{\text{Tank}}/Q^2_{\text{Tank}}$, as seen in Chapter 3. The inductor has been drawn using the top level metal; the width was chosen as a compromise between the parasitic resistance and capacitance. Electromagnetic simulation shows an inductance value of 90 nH and a quality factor of 22 at 20 GHz. To gain more flexibility on the design and robustness of the time domain simulations, a lumped model of the inductor has been used ; Fig.4.3 shows a comparison of the computed inductance and quality factor using the S-parameters and the model, proving the validity and accuracy of the inductor model. Appendix B describes the double π lumped model used for the inductor.

The capacitive part of the tank consists of a bank of 16 binary weighted switched capacitor cells, for coarse tuning, and a MOS varactor for fine tuning. The capacitor bank is controlled by the 4-bit digital word FC_ WORD. The schematic of the switched capacitor cell is showed in Fig.4.2. The width of the transistor M_{sw} has been chosen as a compromise between the quality factor of the capacitor cell, and the tuning range. The larger is the switch, the higher is the quality factor, but the lower is the on/off capacitance ratio of the switched capacitor unit-cell. The two inverters set the dc voltage at the drain and at the source of M_{sw} to ensure it turns on appropriately. The capacitance value of the cell range from 16.5 fF, when the control voltage is "high", to 9.5 fF, when it's "low"; at the same time the quality factor goes from 27 to 44. A small varactor has been chosen to minimize AM-PM conversion. As the signal V_{Tune} varies from 0 to vdd, the varactor continuously tune the oscillation frequency ensuring band overlapping in all sub-band. When V_{Tune} is 0, the simulated capacitance is 17 fF with a quality factor of 18 at 20 GHz;



(A) (B)

FIGURE 4.3: Comparison between inductor model and simulated Sparameters: (a) inductance; (b) quality factor.

while, when V_{Tune} is equal to *vdd*, the capacitance and quality factor are 17 fF and 8 respectively.

The thin oxide nMOS transistor M_1 and M_2 are sized with minimum length of 30 nm and width of 240 μm to minimize the nonlinear capacitance while ensuring the minimum transconductance to start the oscillations. Instead, the tail transistor are made with large area to reduce the flicker noise (M_{T}: W = 5.76 mm, L = 400nm; M_{R}: W = 360 μm, L = 400nm). To filter the noise from M_{R}, a low pass filter has been used, with a cut-off frequency of 200 kHz.

4.1.2 Measurements Results

A prototype of the class-B/D oscillator has been fabricated in a bulk 28 nm CMOS technology; core area is approximately 0.036 mm^2. The supply voltage is 0.9 V. The measured frequency span from 20 to 22.1 GHz. The chip has been placed inside a package.

The measurement setup consists of a board, on which the package is placed, a phase noise analyzer and power supplies connected to the board. By means of serial interface, the chip is programmed in order to control the switch of the capacitor bank.

The phase noise of the oscillator has been measured for different bias current I_{Core}. Due to an error in the design of ESD protection, it was not possible to increase I_{Core} enough to make the oscillator work in class-D.

Figure 4.4 shows the noise sideband at f_0 = 20 GHz for I_{Core} = 3.4 mA and 17 mA where the oscillator works in class-B. At I_{Core} = 3.4 mA, the measured phase noise is -60 dBc/Hz at 100 kHz offset frequency, -94 dBc/Hz at 1 MHz

and -118 dBc/Hz at 10 MHz. Noise summary shows that, at offset lower than 100 kHz, the noise is dominated by the flicker noise of the current tail generator. Between 100 kHz and 10 MHz offset frequency, the noise sideband change slope as effect of the tail filter. Above 1 MHz the noise is dominated by the flicker of the cross-coupled pair.

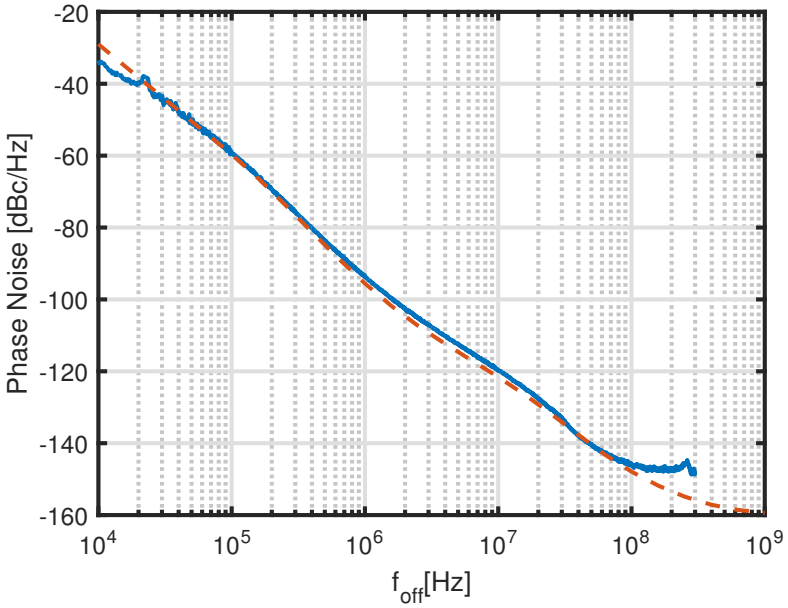
As the bias current increases, the flicker noise of the cross-coupled pair becomes dominant also at lower frequencies, as the noise summary show for I_{Core} = 17 mA. At I_{Core} = 17 mA, the measured phase noise is -70 dBc/Hz at 100 kHz offset frequency, -98 dBc/Hz at 1 MHz and -125 dBc/Hz at 10 MHz; with a $1/f^3$ corner of 900 kHz.

Figure 4.5 shows the simulated phase noise sideband for I_{Core} = 40 mA; the phase noise is -104 dBc/Hz at 1 MHz offset, and flicker corner is around 7 MHz.

4.1.3 Conclusions

A class-B/D oscillator has been presented. The measured phase noise is -98 dBc/Hz at 1 MHz with a power consumption of 15 mW. Despite the poor performance, the area occupation is only 0.036 mm^2.

From the measurement and simulation data, two main problems emerged: the flicker noise from the tail current generator a low offset frequency and the flicker noise from the core transistor at high current. The first one can be solved designing the the tail filter with a lower cut-off frequency and increasing the area of the transistors. The second one, instead, is more problematic and will be addressed in the following section.



(A)

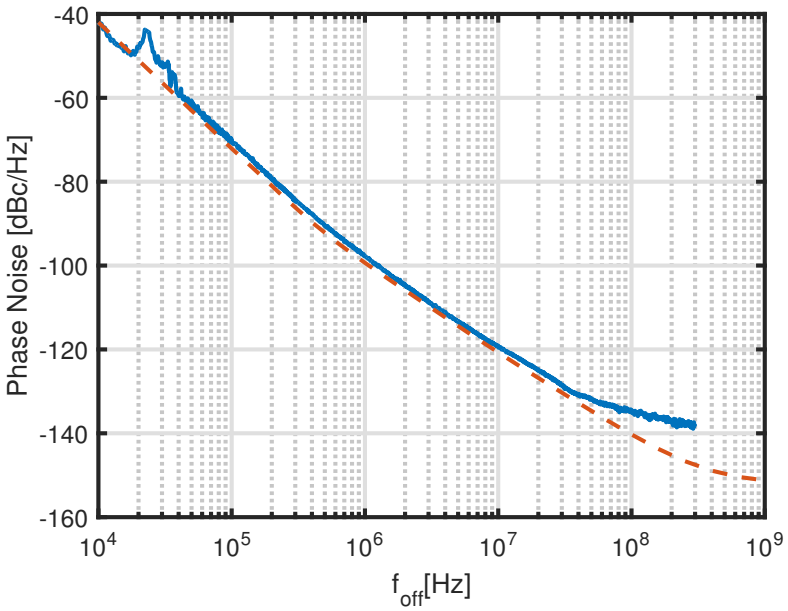


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FIGURE 4.4: Measured (solid lines) and simulated (dashed lines) phase noise sideband for different values of I_{Core} : (a) 3.4 mA; (b) 17 mA.

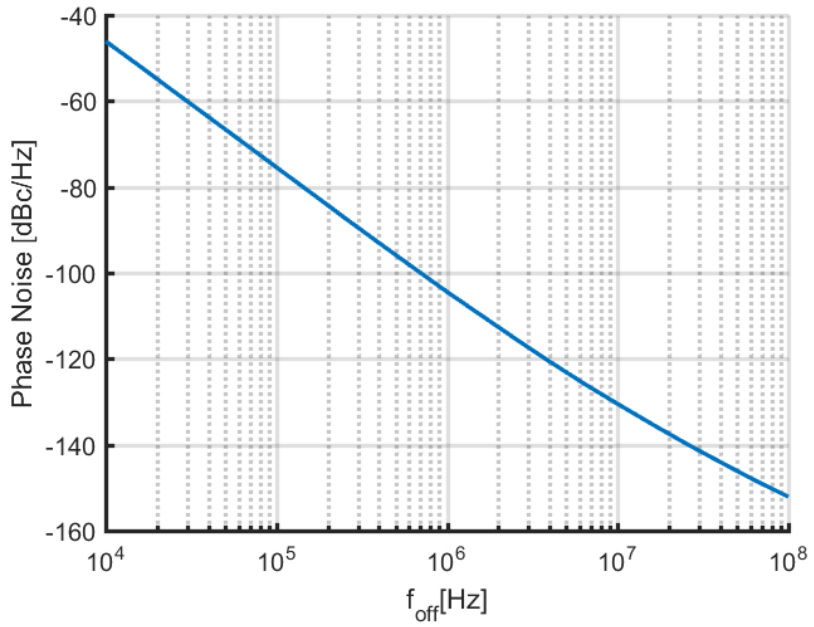


FIGURE 4.5: Simulated phase noise with $I_{\text{Core}} = 40\,\text{mA}$.

4.2 1/f Noise Upconversion: Class-B vs Class-C Operation

Measurements and simulations on the class-D oscillator have shown that the flicker noise from the cross-coupled pair can be the main source of phase noise. In this section, a comparison between class-B and class-C about the upconversion of flicker noise in phase noise is carried out.

In the literature, e.g., [38–40], it has been pointed out that in class-B oscillators, as well as in class-F and derivative topologies, setting the common-mode tank impedance to resonate at the second harmonic of the oscillation frequency results in a reduction of the upconversion of the 1/f noise of the core devices sustaining the oscillation. While this approach is effective, it is also narrowband, and therefore requires tuning. On the other hand, it has been show that single-ended Colpits oscillator are immune to flicker noise upconversion from the core transistor, provide that the voltage-current characteristic is quadratic [41].

Class-B and class-C oscillators basically share the same circuit topology, with one key difference. In Fig. 4.6a, the schematic of a typical class-B oscillator is shown. The capacitance C_{tail} represents the parasitic output capacitance of the tail current generator and the parasitic source capacitance of the transistors of the cross-coupled pair. The presence of C_{tail} is known to degrade the oscillator performance [42, 43]. In the class-C oscillator, instead, C_{tail} is

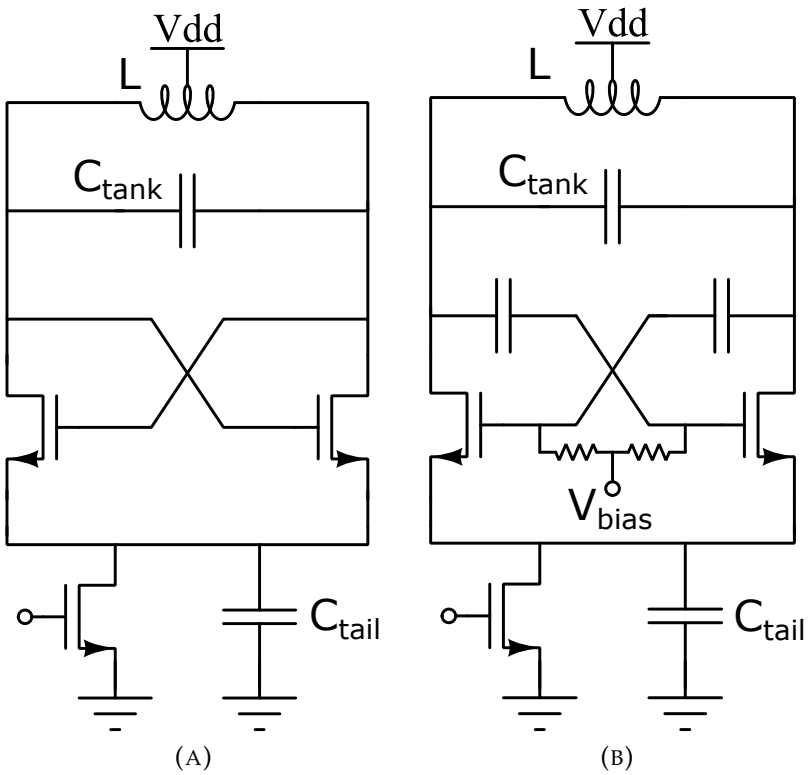


FIGURE 4.6: Oscillator topologies: (a) class-B; (b) class-C.

deliberately made large, and the transistors of the cross-coupled pair are ac-coupled to the tank to enable class-C operation (see Fig. 4.6b). Hence, in this case C_{tail} is a desired, and in fact crucial, part of the circuit [43].

In ultra-scaled CMOS technologies, the upconverted 1/f noise may dominate the phase noise sidebands up to large frequency offsets. The upconversion of the 1/f noise from the tail current source is similar in class-B and class-C oscillators, and so is the 1/f noise upconversion due to nonlinear capacitances. Moreover, while these sources of 1/f noise upconversion can be minimized, at least to a large extent, the 1/f noise generated by the cross-coupled pair is much more troublesome, and merits a more detailed study. To this aim, behavioral simulations have been carried out − the qualitative conclusions, however, do not change with silicon-level simulations. The transistors have been modeled in Verilog-A usign the drain current equations in [44] for both long and short channel. In saturation region:

- long-channel:

$$I_d = \frac{\beta}{2} V_{ov}^2, \tag{4.1}$$

- short-channel

$$I_d = \frac{\beta}{2} V_{sat}^2; \tag{4.2}$$

while in triode region:

- long-channel:
$$I_d = \frac{\beta}{2}\left[2V_{\text{ov}} - V_{ds}^2\right], \tag{4.3}$$
- short-channel
$$I_d = \frac{\beta}{2(1+\theta V_{DS})}\left[2V_{\text{ov}} - V_{ds}^2\right], \tag{4.4}$$

where
$$V_{\text{sat}} = \frac{1}{\theta}\left(\sqrt{1+2\theta V_{\text{ov}}} - 1\right), \tag{4.5}$$

$V_{\text{ov}} = V_{gs} - V_t$ is the overdrive voltage and the parameter θ accounts for so-called short channel effects.

The LC resonator is the same for both oscillators in Fig. 4.6, with $L = 120\,\text{pH}$ and $C_{\text{tank}} = 530\,\text{fF}$, for an oscillation frequency of $20\,\text{GHz}$. No frequency tuning mechanism or nonlinear capacitances are considered. The bias current is set in order to have the same amplitude of oscillation in both oscillators, i.e. the maximum amplitude still keeping the oscillator in the current-limited regime, while avoiding that the class-C cross-coupled pair enters the linear region of operation. The phase noise at 10 kHz offset due to the 1/f noise of the cross-coupled pair is assessed as C_{tail} is changed. The results are reported in Fig. 4.7, where the phase noise is normalized to the maximum observed value.

If C_{tail} is zero, there is no 1/f noise upconversion into phase noise in the class-B oscillator; this is in agreement with the analysis carried out in [41]. In practice, C_{tail} will not be zero, as there will always be some parasitic capacitance. The results in Fig. 4.7 show that as soon as $C_{\text{tail}} \neq 0$, there is a substantial $1/f^3$ phase noise due to the transistors of the cross-coupled pair. However, such a contribution vanishes if C_{tail} is such that the common-mode tank impedance resonates at twice the carrier frequency (where Fig. 4.7 shows the characteristically narrow notch), as predicted by the analysis in [45], and discussed in [38–40]. Notice that the presence of short-channel effects has only a marginal impact.

Turning now to the class-C topology, it has been shown in [41] that ideal class-B oscillators (i.e., with $C_{\text{tail}} = 0$) and single-ended Colpitts oscillators are immune to any upconversion of 1/f noise from the core transistor(s), provided that the voltage-to-current characteristics of the MOS transistor is the (ideal) quadratic one. It is laborious, but devoid of any major difficulty, to

show that this property still applies to a general class-C oscillator – provided, of course, that the core devices never enter the linear region of operation.

It is important to recognize that the particular value of C_{tail} is immaterial for this remarkable property. If C_{tail} is small compared to the tank capacitance, the oscillator exhibits a behavior between class-B and class-C, possibly with a clearly asymmetric current waveform from each core transistor – nevertheless, no 1/f noise upconversion takes place. This is, we believe, worth observing explicitly, as the symmetry of the current waveforms is sometimes assumed to be a necessary condition for 1/f noise upconversion minimization.

Fig. 4.7 confirms that 1/f noise upconversion in a class-C oscillator with ideal long-channel MOS devices is nonexistent (within the limits of numerical simulation tolerances) for any C_{tail}.

In ultra-scaled CMOS technologies, however, short channel effects are not negligible. Their impact on 1/f noise upconversion can be appreciated from Fig. 4.7: while the 1/f noise upconversion in the class-C oscillator is no longer nil, it is still low enough to make the class-C oscillator a very attractive architecture, since this performance is achieved in a robust way. The class-B oscillator, on the other hand, while it is in principle capable of an even lower 1/f noise upconversion, is dependent on the delicate tuning of the common-mode impedance of its tank at twice the oscillation frequency, as also shown in Fig. 4.7 (we remark that the positions of maxima and minima in 1/f noise upconversion for both class-B and class-C topologies depend on the nature of the tank impedances at even, and primarily at the 2^{nd}, harmonics).

Building on the above results, in the next section, the class-C oscillator topology is proposed as a means to minimize the upconversion of the 1/f noise of the cross-coupled pair without the need of any tuning. Moreover, as in class-C oscillators the precise value of C_{tail} is not critical (as long as it is not so large as to cause squegging [43]), the tail current source can be realized with long and wide devices, in order to minimize this source of $1/f^3$ phase noise as well, while keeping the dc voltage drop across its channel at a reasonable value.

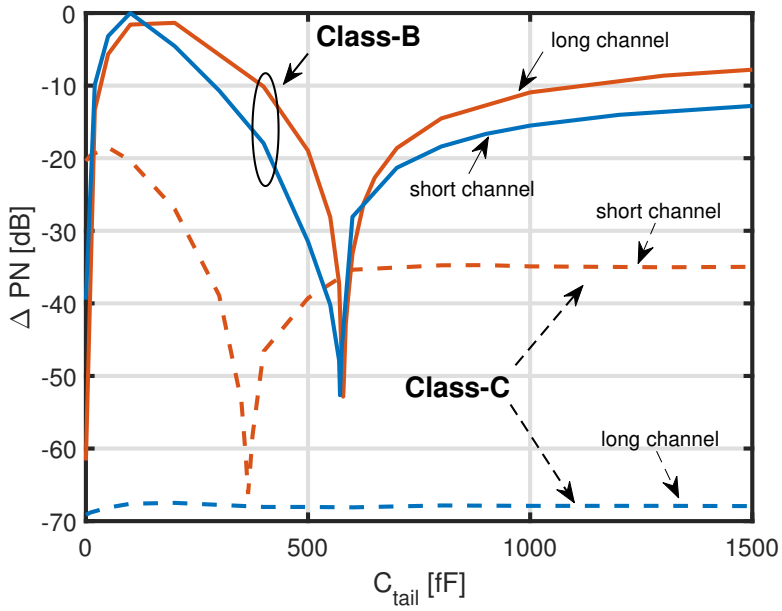


FIGURE 4.7: Simulated normalized phase noise due to the 1/f noise of the cross-coupled pair of the class-B and class-C oscillators. The transistor parameters are: $\beta = 200\,\mathrm{mA/V^2}$ (class-B) or $\beta = 350\,\mathrm{mA/V^2}$ (class-C); $\theta = 2\,\mathrm{V^{-1}}$ (short channel) or $\theta = 0\,\mathrm{V^{-1}}$ (long channel).

4.3 Class-C VCO

4.3.1 Design

The schematic of the proposed class-C oscillator is shown in Fig. 4.8. To minimize the 1/f noise, pMOS transistors are preferred over nMOS devices. The peculiar characteristic of the class-C oscillator is the large tail capacitance, C_{tail}. The selected capacitance value is 5 pF, large enough to provide the current impulses to the cross-coupled pair, while maintaining the voltage at the common source terminal (V_{CS}) almost constant, but still small enough to avoid squegging [43].

The tank has been sized in order to minimize the phase noise by minimizing the ratio between the equivalent tank parallel resistance and the square of the tank quality factor, as shown in Chapter 3, even at the expense of a slight penalty in the oscillator figure-of-merit. A magnetic transformer is used to ac-couple the gates of the cross-coupled transistors to the tank, as the transformer passive voltage gain reduces the contribution of the active devices to the $1/f^2$ phase noise [43]. The primary inductor, $L_1 = 50\,\mathrm{pH}$ with a quality factor of 17, is connected to the drains of the transistors of the cross-coupled pair, while the secondary, $L_2 = 90\,\mathrm{pH}$ with a quality factor of 21, to their

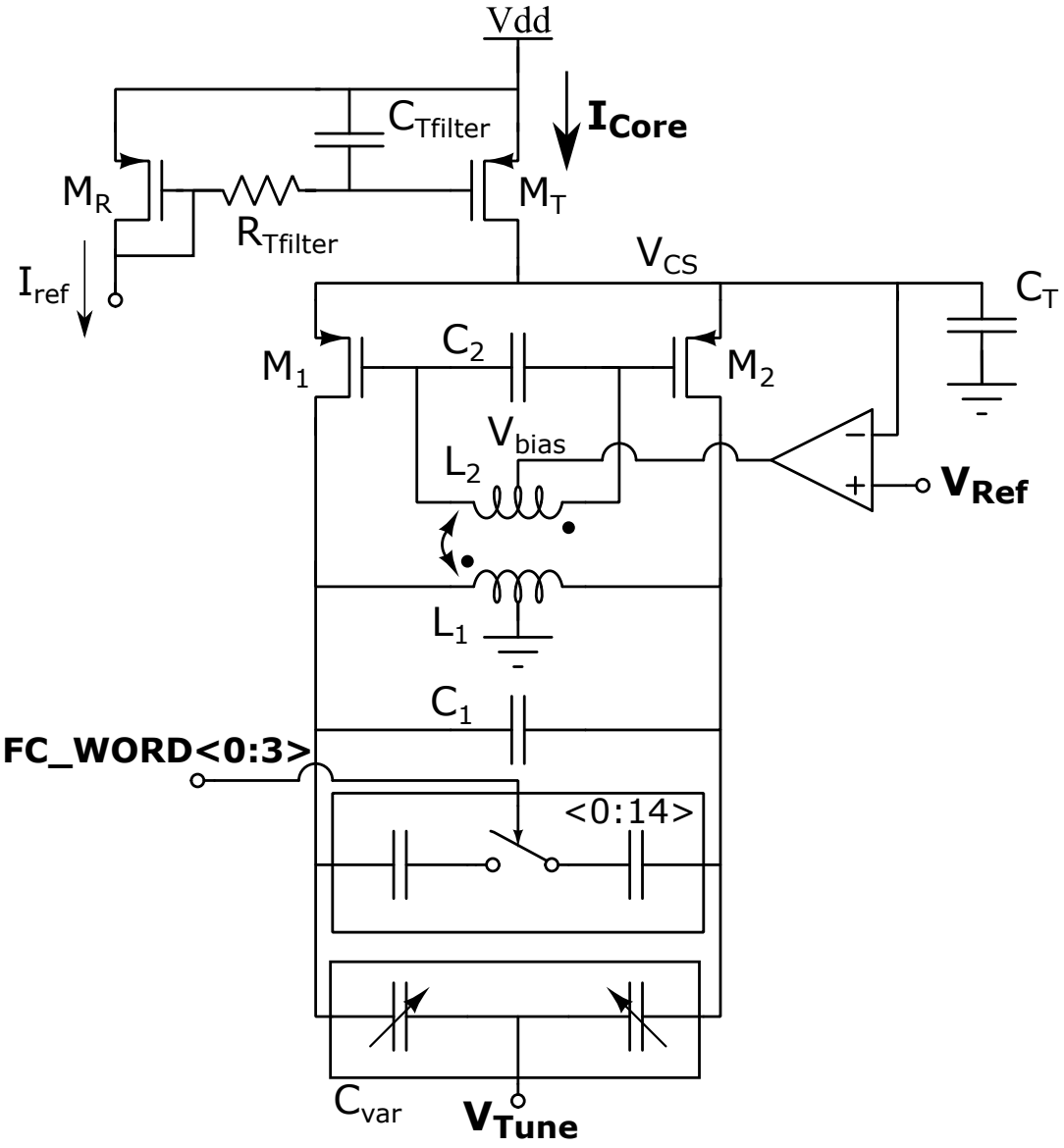


FIGURE 4.8: Schematic of the proposed class-C oscillator.

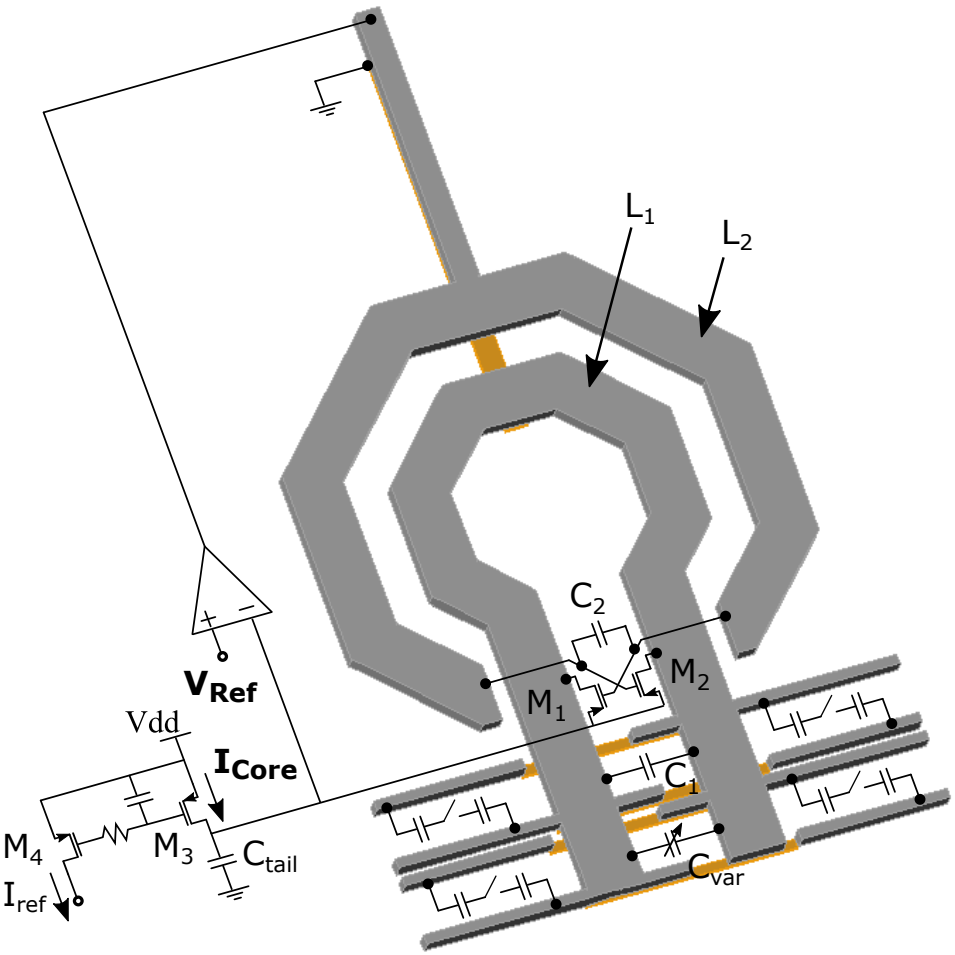


FIGURE 4.9: 3D view of the transformer.

gates. Both coils are single-turn. The magnetic coupling is $k = 0.35$. Figure 4.9 shows the 3D view of the transformer.

The capacitive part of the tank consists of MOM capacitors $C_1 = 200fF$ and $C_2 = 350fF$, and of a variable capacitance. The variable capacitance is used to tune the oscillation frequency. It is made of a 4-bit bank of binary weighted switched capacitor cells for coarse tuning, and a MOS varactor for fine tuning. A small varactor is chosen to minimize the AM-PM conversion.

The tail current source uses pMOS thick oxide devices with a large gate area to reduce $1/f$ noise. To reduce the noise coming from the reference branch, an RC filter with a large time constant is used: the resistance value is $R_{\text{Tfilter}} = 6\,\text{M}\Omega$ and the capacitance is $C_{\text{Tfilter}} = 22\,\text{pF}$. To ensure a reliable start-up of the oscillations, and provide the bias voltage to the gate of the cross-coupled pair, a dynamic-bias loop is used [46]. The loop controls

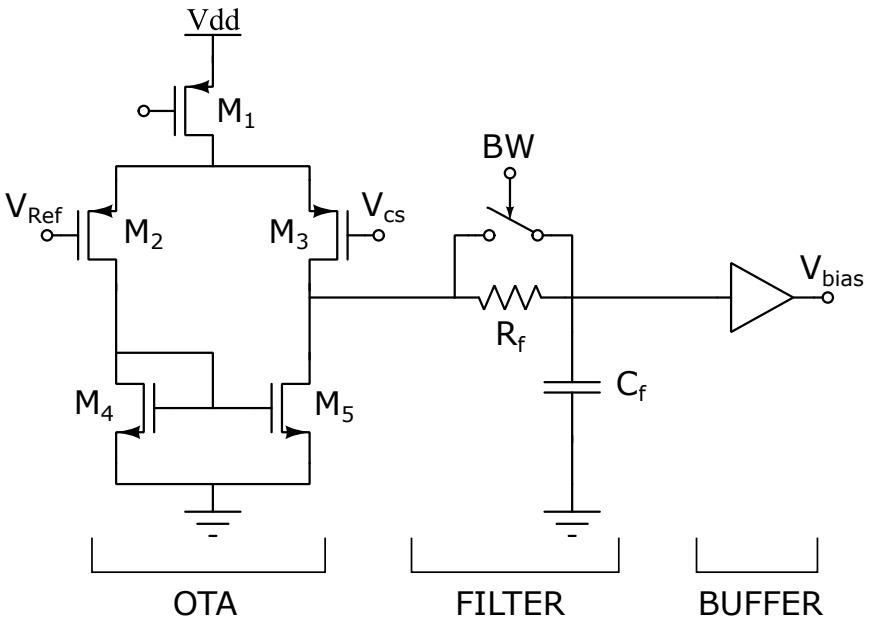


FIGURE 4.10: Schematic of the op-amp used in the dynamic-bias loop.

the voltage at the source of the cross-coupled pair; the reference value is selected in order to leave enough headroom for the tail generator to operate in the saturation region. Figure 4.10 shows the schematic of the op-amp used in the dynamic-bias loop. Since the noise of the op-amp can be a dominant contribution in the oscillator phase noise at low offsets from the carrier, the dynamic-bias loop bandwidth is kept low by cascading a passive RC filter with a large time constant ($R_f = 4\,\mathrm{M\Omega}$ and $C_f = 12\,\mathrm{pF}$) to a single-stage OTA with 33 dB gain (see Fig. 4.10). An output voltage buffer based on a common-drain stage is then used to provide the leakage current to the transistors of the cross-coupled pair, since they are thin oxide devices. Simulations show that the loop transmission has band of 2.5 kHz and a gain of 26db with a phase margin of 86 at 35 kHz due to the dominant pole introduced by the op-amp filter. Therefore, the loop stability is ensured also for PVT variations. The signal BW controls a switch that can bypass R_f to increase the loop bandwidth and, therefore, reduce the settling time at the oscillator start-up.

4.3.2 Measurements Results

In this section the measurements of class-C oscillator are compared with the post-layout simulations. Prototypes of the proposed class-C oscillator were fabricated in a bulk 28 nm CMOS technology. The die photograph is shown in Fig. 4.11. The core area is approximately 0.07 mm^2. The chip has been placed inside a package.

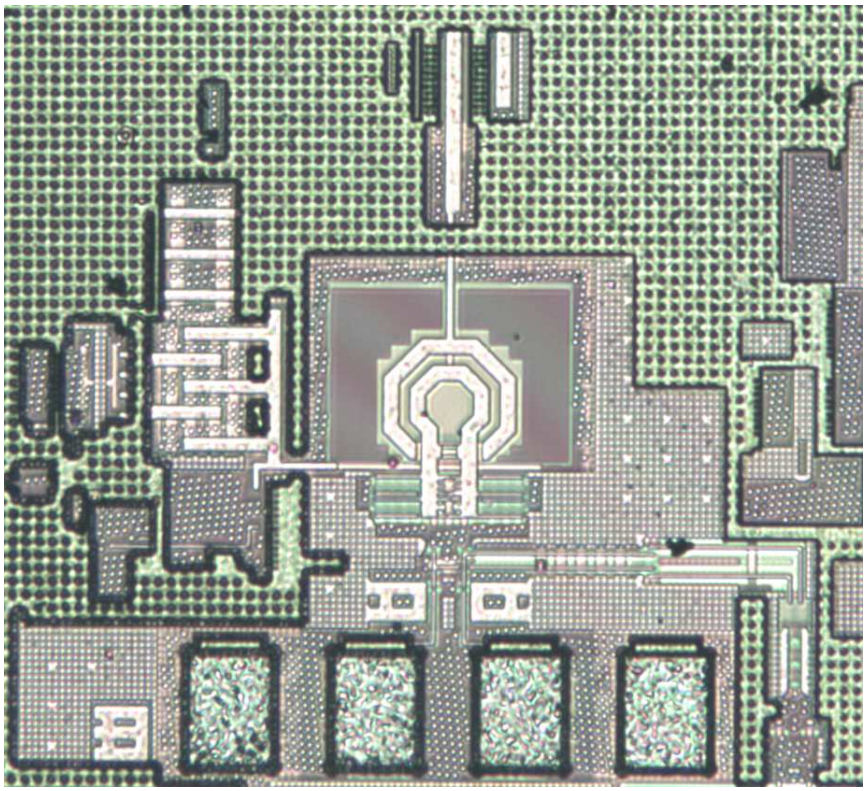


FIGURE 4.11: Die photograph. Core area is ≈0.07 mm^2.

The measurement setup consists of a board, on which the package is inserted, a phase noise analyzer and power supplies connected to the board. By means of serial interface, the chip is programmed in order to control the IDAC of the current tail generator and the control word of the capacitor bank.

The supply voltage of the oscillator is $V_{dd} = 0.9\,\text{V}$, while for for the opamp is 1.8 V . The measured frequency of oscillation spans from 18.4 GHz to 20.7 GHz (coarse tune), covering a 12% tuning range. Figure 4.12 shows the measured and simulated frequency as the digital control word of the capacitance bank is changed. Due to parasitic capacities, the measured tuning range is less than the simulated one; moreover, it is also not monotonic. This problem can be corrected by repositioning the capacity bank cells.

The phase noise of the oscillator was measured for different values of the bias current I_{Core}, of the reference voltage of the dynamic-bias loop, V_{Ref}, and of the oscillation frequency f_0. Figure 4.13 shows the measured phase noise for $I_{\text{Core}} = 16\,\text{mA}$, with $f_0 = 19.5\,\text{GHz}$, $V_{\text{Tune}} = V_{dd}$, and $V_{\text{Ref}} = 0.6\,\text{V}$. At 1 MHz frequency offset the measured phase noise is -108.5 dBc/Hz, while at 100 kHz frequency offset it is -83 dBc/Hz; the $1/f^3$ corner frequency is slightly larger than 300 kHz.

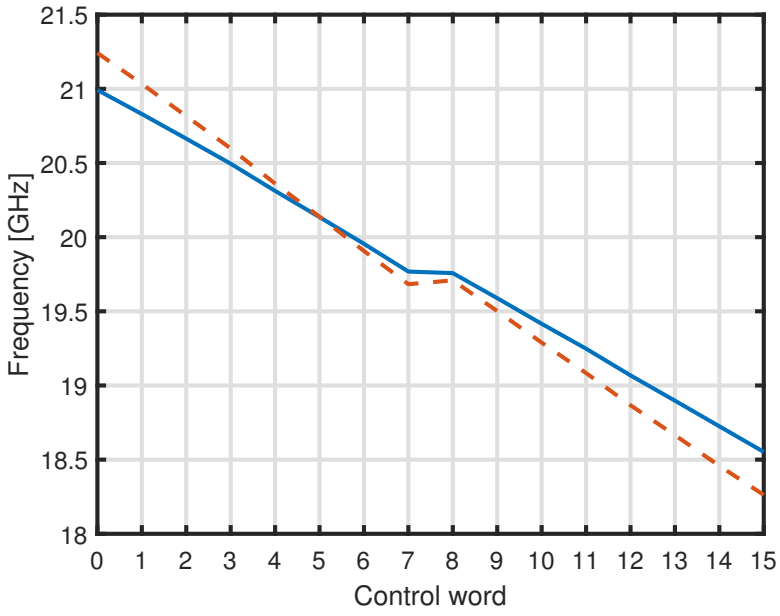


FIGURE 4.12: Measured (solid lines) and simulated (dashed lines) oscillation frequency versus digital control word (coarse tune).

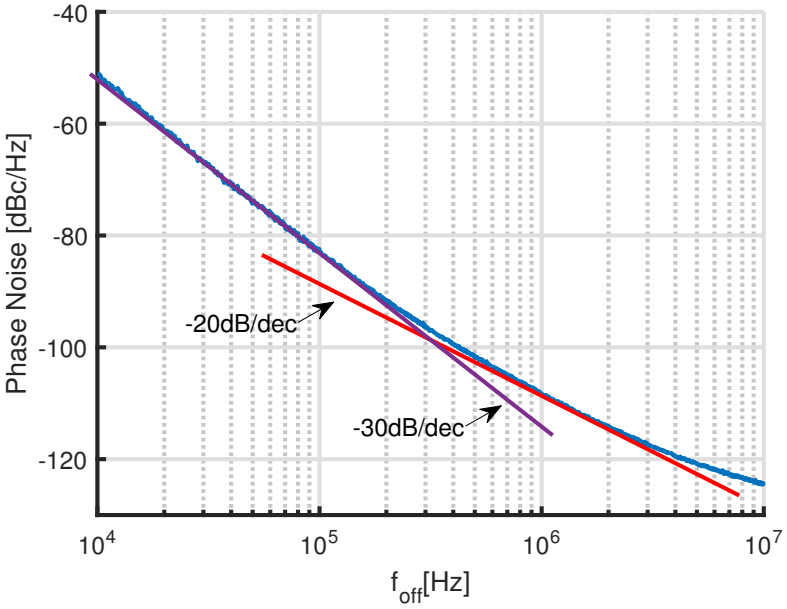


FIGURE 4.13: Measured phase noise versus offset frequency for $I_{\text{core}} = 16\,\text{mA}$ at $f_0 = 19.5\,\text{GHz}$ and $V_{\text{ref}} = 0.6\,\text{V}$.

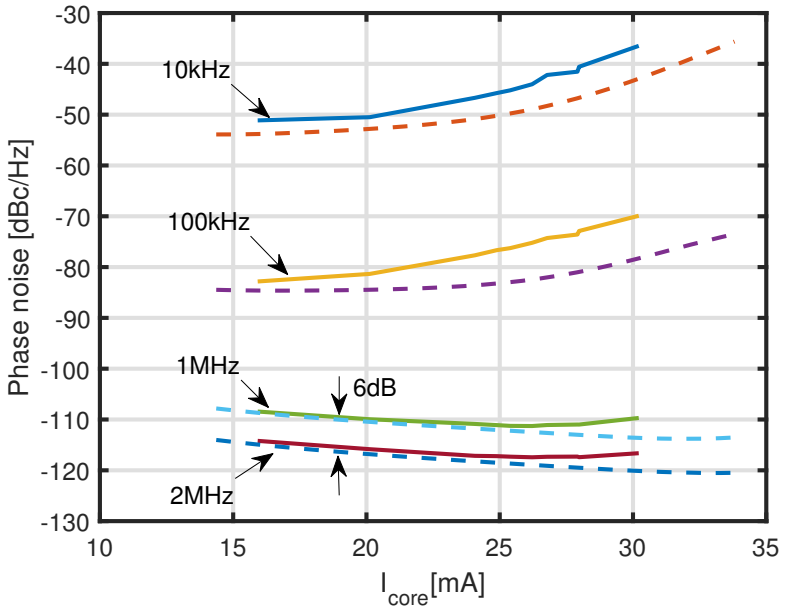


FIGURE 4.14: Measured (solid lines) and simulated (dashed lines) phase noise versus I_{Core} for different offsets from the 19.5 GHz carrier frequency with $V_{\text{Ref}} = 0.6$ V and $V_{\text{Tune}} = V_{dd}$.

In Fig. 4.14, phase noise measurements (solid line) and post-layout simulations (dashed lines) are compared, for a set of offset frequencies, as I_{Core} is changed. In the $1/f^2$ noise region, the measurements are in agreement with the simulations in the limit of the accuracy of the phase noise analyzer. In the $1/f^3$ noise region, there is a fair agreement between measurements and simulations for lower values of I_{Core}, while there is a substantial difference for larger values of I_{Core} and, thus, of the oscillation amplitude. It is interesting to note that increasing I_{Core} to 24 mA with respect to the nominal 16 mA results in a 2.5 dB improvement in the $1/f^2$ region, while, at lower offsets, the phase noise is severely degraded. The phase noise improvement at large offsets is due to the increased amplitude of oscillation; conversely, the noise increase at lower offsets is due to an increased noise contribution from the op-amp in the dynamic-bias loop. The reason for this is twofold: first, as I_{Core} increases, the output resistance of the tail current source decreases, and the input-referred op-amp noise, which is copied to V_{CS} by the loop, is more efficiently converted into a noise current that adds to the intrinsic tail source noise current. Second, as I_{Core} (and, consequently, the oscillation amplitude) increases, the sensitivity of f_0 to I_{Core} also increases, such that the upconversion into phase noise of any disturbance on the bias current is magnified. At the increased I_{Core} value of 24 mA, the difference between measured and simulated phase noise at 10 kHz offset is 4 dB.

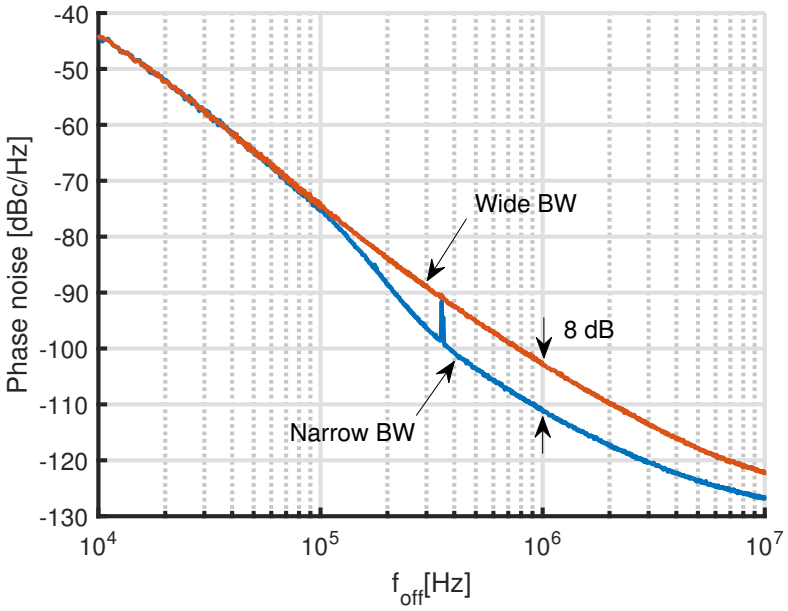


FIGURE 4.15: Comparison between measured phase noise with wide and narrow dynamic-bias loop bandwidth at $I_{\text{core}} = 26\,\text{mA}$, $f_0 = 19.5\,\text{GHz}$ and $V_{\text{ref}} = 0.6\,\text{V}$.

The experimental evidence that the op-amp noise becomes the dominant phase noise contributor at lower offsets for large values of I_{Core} is the sharp rolloff in the phase noise sideband observed in Fig. 4.13 at offsets equal to the dynamic-bias loop bandwidth, i.e. 150 kHz. If the bandwidth of dynamic-bias loop is increased (acting on the signal BW), a strong increase (up to 8 dB) of the phase noise is observed at offsets $> 150\,\text{kHz}$ (see Fig.4.15). This further confirms that the op-amp noise upconversion dominates the phase noise at lower offsets, and that a careful design of the dynamic-bias loop is required to avoid impairing the oscillator performance.

Increasing the reference voltage, V_{Ref}, to 0.7 V reduces the voltage headroom for the tail current source, but allows to increase the oscillation amplitude while keeping the VCO at the edge of the current-limted regime. This results in a slight improvement in the phase noise performance (1 dB at 1 MHz offset and 3 dB at 10 kHz offset), which nevertheless requires to increase I_{Core} to 28 mA.

The VCO phase noise performance across the tuning range is shown in Fig. 4.16, with $I_{\text{Core}} = 26\,\text{mA}$, $V_{\text{Ref}} = 0.6\,\text{V}$ and $V_{\text{Tune}} = V_{dd}/2$. In the white noise region there is a good agreements between simulation and measurement; the measured phase noise variation is less than 2 dB. Instead, at small offset, the degradation is larger. A possible explanation to this behaviour is that, changing the frequency, and thus the configuration of the capacitor

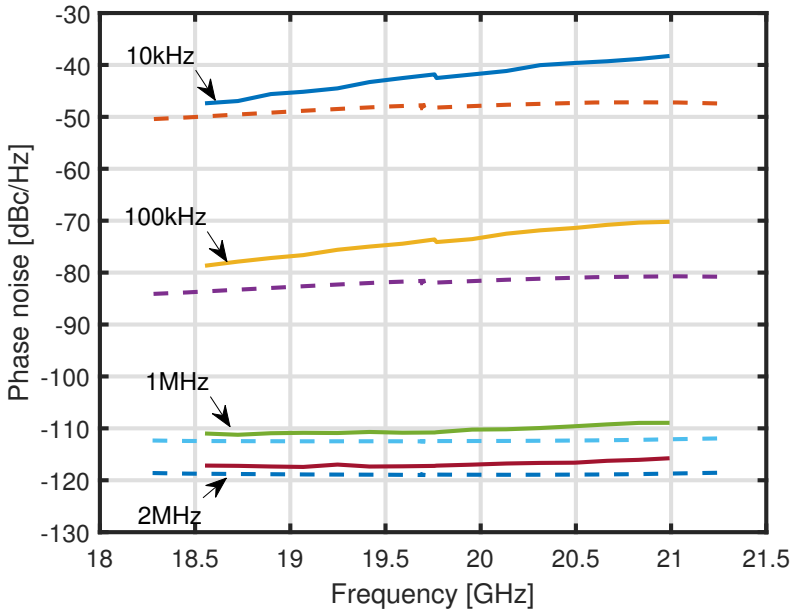


FIGURE 4.16: Measured (solid lines) and simulated (dashed lines) phase noise versus f_0 for different offsets frequency with $I_{\text{Core}} = 26\,\text{mA}$, $V_{\text{Ref}} = 0.6\,\text{V}$ and $V_{\text{Tune}} = V_{dd}/2$.

bank, the equivalent tank parallel resistance change. Therefore, for the same value of tail current, the amplitude of the oscillation change, forcing the transistors to enter the deep triode region and degradating the performance.

4.3.3 Comparison with the State-Of-The-Art

The performance of the proposed class-C VCO is summarized in Table 4.1, and compared to the state-of-the-art; for a fair comparison phase noise performance has been normalized to a 19.5 GHz carrier. Both the phase noise performance and the figure-of-merit is in line with those of the other reported mm-wave VCOs. The main difference of this design is that no particular tuning of the second-harmonic tank impedance is required.

4.3.4 Conclusions

A class-C voltage controlled oscillator in a bulk 28 nm CMOS technology has been presented. The circuit achieves a low phase noise of -108.5 dBc/Hz at 1 MHz offset and -83 dBc/Hz at 100 kHz from the 19.5 GHz carrier, drawing 16 mA from a supply voltage of 0.9 V, while featuring a 12% tuning range. The measurements show that, even in an ultra-scaled design, where short-channel effects seriously impact the behavior of the MOS device, the class-C

TABLE 4.1: Performance summary and comparison with previously published VCOs in 28 nm CMOS technologies.

	JSSC 2017 [38]	JSSC 2016 [47]	JSSC 2018 [40]	VLSI 2017 [48]	JSSC 2018 [49]	**This Work**
Topology	Class-B Implicit resonance	Class-F	Class-$F_{2,3}$	Pulse taill feedback	Class-B	**Class-C**
Tech. [nm]	28	40	28	180	40	**28**
V_{dd} [V]	0.9	0.7	1.0	1.2	0.95	**0.9**
Freq. [GHz]	3.33	57.8	27.3	4.55	25	**19.5**
Tuning range [%]	27	25	14	5.5	26	**12**
Power [mW]	6.8	24	12	1.35	16	**14.4**
Phase noise @1 MHz [dBc/Hz]	-130	-100	-106	-123	-110	**-108.5**
Eq. phase noise referred to 19.5 GHz @1 MHz [dBc/Hz]	-114	-109.5	-109	-110.8	-112	**-108.5**
Phase noise @100 kHz [dBc/Hz]	-105	-73	-83	-103.6	-83	**-83**
Eq. phase noise referred to 19.5 GHz @100 kHz [dBc/Hz]	-89	-82.5	-86	-91	-85	**-83**
FoM [dBc/Hz]	-192	-181	-184	-195	-196	**-183**
Core area [mm^2]	0.19	0.13	0.15	NA	0.1	**≈0.07**

oscillator is able to largely suppress the upconversion of the 1/f noise from the cross-coupled transistors into phase noise.

At small offsets, the phase noise is degraded by the op-amp in the dynamic bias loop – an undesider effect that can be fixed with a a careful redesign.

4.4 Class-C: Redesign

As showed in Fig. 4.14, the best phase noise performance in the white region (i.e. at offset frequency above 1 MHz), is for bias current I_{Core} around 25 mA; while, due to the op-amp noise, in the flicker region the phase noise is severely degraded even at low bias current. Therefore, to get the intrinsic performance of the class-C operation, a redesign is required. This is done in two steps: first an ultra-low noise op-amp is designed; second, to filter the residual noise due to the tail generator, the polysilicon resistor of the tail filter is substituted with a MOS resistor with higher value of resistance.

4.4.1 OP-AMP Redesign

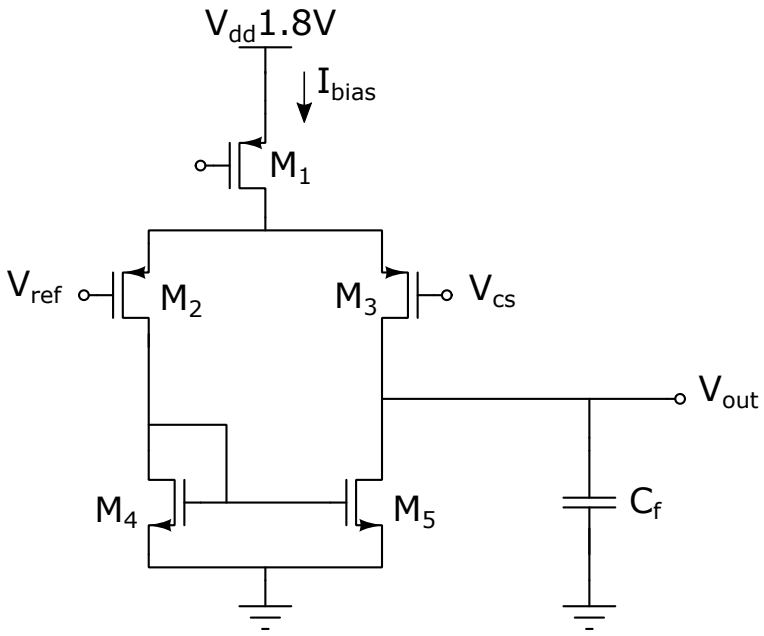
Two version of the op-amp have been designed: the schematic are presented in Fig.4.17. *Design A* consists of a single stage ota with capacitive load; while *Design B* also include a voltage buffer at the output. Compared to the original design, the filter resistance has been removed. The ota is identical in both design, and the value of $C_f = 40pF$ as well.

The power spectral density of flicker noise in MOS transistors is inversely proportional to the gate area and dependent to the bias current. Therefore, in both new designs of the op-amp, the width and length of the transistors of the differential pair are chosen larger than the previous version. Moreover, the bias current, I_{Bias}, has been reduced to 10 nA. Consequently, the transistors of the differential pair are biased in weak inversion. In weak inversion, the MOS behave like a bipolar transistor; therefore, the transconductance is independent on the overdrive voltage and depends only on the bias current and the thermal voltage. At room temperature, the simulated g_{m} is 165 nS.

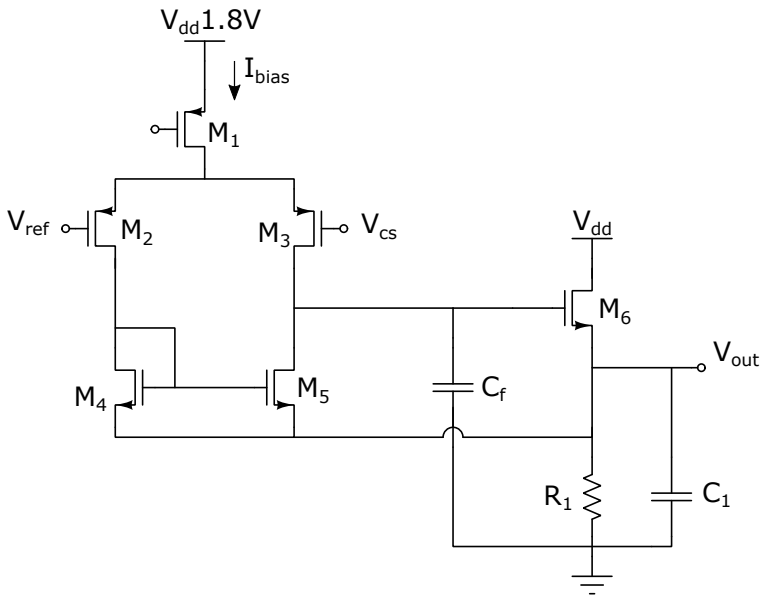
The unity gain frequency is given by $g_{\text{m}}/C_{\text{f}}$. To reduce the start-up time, a possible solution is to increase the bias current, and therefore the g_{m} of the transistors.

4.4.2 Tail Filter Redesign

At low offset frequency, simulations show a residual contribution from the diode connected transistor of the tail generator. Therefore, it is necessary to reduce the cut-off frequency of the tail filter. Both resistance and capacitance can be made larger, at expense of the area. To keep the occupation of area limited, the polysilicon resistor has been substituted by a MOS resistance.



(A) *Design A*



(B) *Design B*

FIGURE 4.17: Schematic of the op-amp used in the dynamic-bias loop.

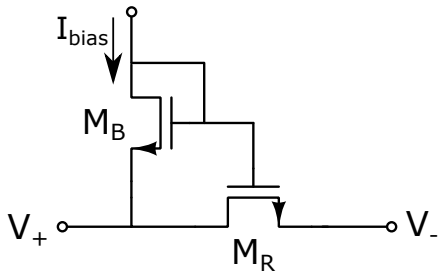


FIGURE 4.18: Schematic of the MOS resistance and bias circuit.

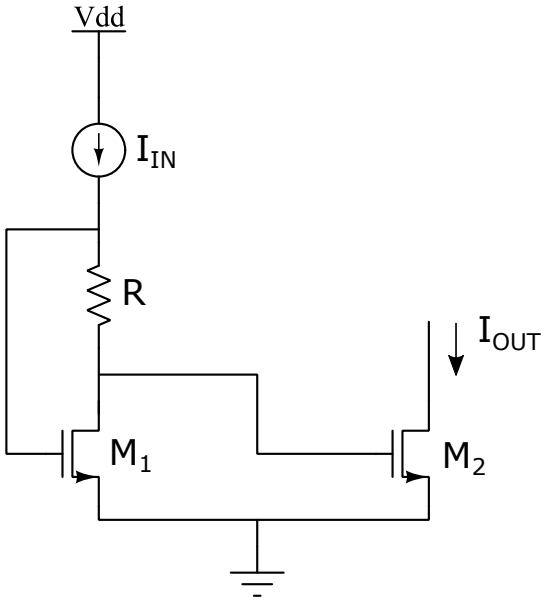


FIGURE 4.19: Schematic of the peaking current source.

Figure 4.18 shows the schematic of the MOS resistance with the bias circuit. Transistor M_B is use to bias the transistor M_R so that the gate-source voltage, and therefore the resistance of M_R, is kept constant. The bias current I_{bias} is 250 nA, low enough to bias both transistor in weak inversion; the simulated resistance is around 20 MΩ.

The filter capacitance is $C_{Tfilter} = 40\,pF$.

4.4.3 Bias Current Generator

Both redesign of the op-amp require a bias current of 10 nA, moreover, the MOS resistance of the tail filter requires a bias current of 250 nA. To realize a current in the order of nanoampere, the peaking current source, shown in Fig. 4.19, can be used.

Assuming that both M_1 and M_2 operate in the active region, then, applying the kirchhoff voltage law at the gate-source loop gives:

$$V_{GS1} - I_{IN}R - V_{GS2} = 0 \tag{4.6}$$

Since the desired output current is small, M_2 usually operates in weak inversion where the drain current is an exponential function of gate-source voltage:

$$I_D = \frac{W}{L} I_t \exp\left(\frac{V_{GS} - V_{th}}{nV_t}\right)\left[1 - \exp\left(\frac{V_{DS}}{V_T}\right)\right] \tag{4.7}$$

Then, depending on input current and form factor, M_1 can operates in weak or strong inversion.

If M_1 is biased in weak inversion, applying 4.7 and assuming $V_{DS1} > 3V_T$ to M_1 and substituting into 4.6 gives:

$$V_{GS2} - V_{th} \simeq nV_T \ln\left(\frac{I_{IN}}{(W/L)_1 I_t}\right) - I_{IN}R \tag{4.8}$$

If also $V_{DS2} > 3V_T$, substituting 4.8 into 4.7 gives:

$$I_{OUT} \simeq I_{IN}\frac{(W/L)_2}{(W/L)_1}\exp\left(-\frac{I_{IN}R}{nV_T}\right) \tag{4.9}$$

where I_t represents the drain current of M_2 with $V_{GS2} = V_t$, $(W/L)_2 = 1$ and $V_{DS} \gg V_T$. The plot of 4.9 is shown in Fig.4.20 for different values of R, $n = 1.5$, $T = 25\,^{\circ}\mathrm{C}$ and $(W/L)_1 = (W/L)_2$. When the input current is small, the voltage drop on the resistor is small, and $I_{OUT} \simeq I_{IN}$. As the input current increases, V_{GS1} increases more slowly than the drop on the resistor. As a result, increases in the input current eventually cause V_{GS2} to decrease. The output current reaches the maximum when V_{GS2} is maximum.

Conversely, if M_1 is biased in strong inversion:

$$V_{GS2} - V_{th} = V_{ov1} - I_{IN}R \tag{4.10}$$

where $V_{ov1} = \sqrt{2I_{IN}/[k'(W/L)_1]}$.

Therefore, the output current becomes:

$$I_{OUT} \simeq I_{IN}(W/L)_2 \exp\left(\frac{V_{ov1} - I_{IN}R}{nV_T}\right) \tag{4.11}$$

Figure 4.21 shows the output current when M_1 is in strong inversion, with $(W/L)_2 = 10$, $I_t = 100nA$ and $k' = 200\mu A/V^2$. The transfer characteristic is quite different compared to the previous case as the output current now is a monotonic function of the input current.

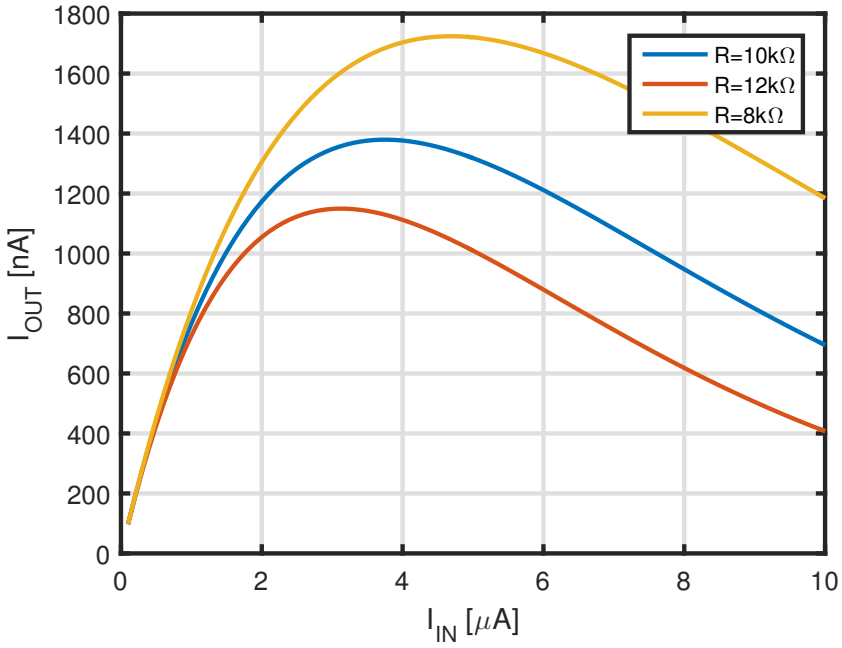


FIGURE 4.20: Output characteristics of the peaking current source when M_1 operates in weak inversion

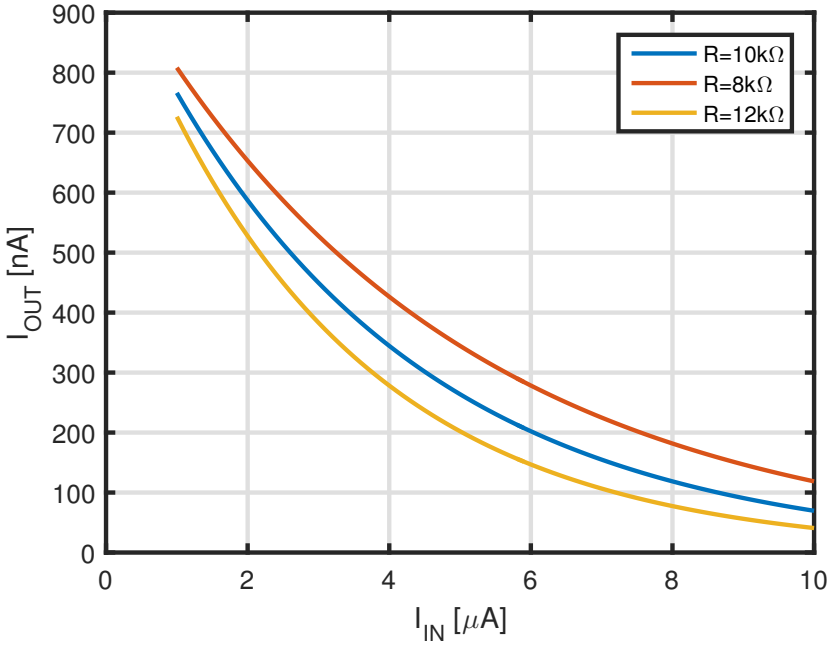


FIGURE 4.21: Output characteristics of the peaking current source when M_1 operates in strong inversion

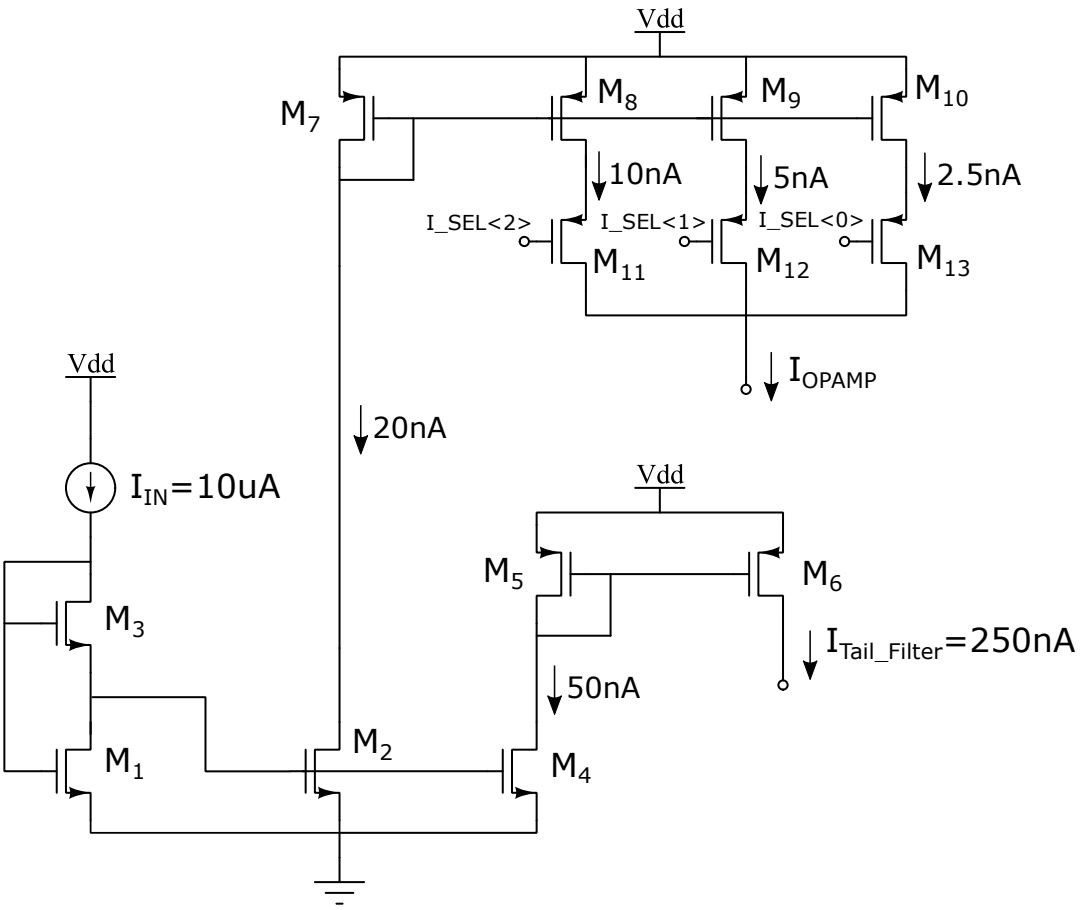


FIGURE 4.22: Proposed current bias generator

The problem of this circuit is that, either with M_1 in strong or weak inversion, process variation of the selected value of the resistance strongly affect the output current. To mitigate this problem Fig.4.22 shows the proposed circuit for the biasing of the OPAMP and the tail filter resistance. The input current I_{IN} is assumed to be equal to $10\mu A$; the drain current of M_2, in nominal condition, is $20nA$ and it is used as reference for the 3 bit current-digital-to-analog converter (IDAC). By changing the control word I_SEl, the OPAMP bias current can be made to vary from $2.5nA$ to $17.5nA$ with step of $2.5nA$ in order compensate the effect of process variation. The bias current of the tail resistance filter is obtained using the drain current of M_4 as reference for the current mirror composed by M_5 and M_6. The nominal value of the output current is $250nA$.

In Fig 4.22, the resistance R has been replaced with the transistor M_3. If M_2 and M_3 operate in weak inversion and M_1 in strong inversion, the drain current of M_2 is:

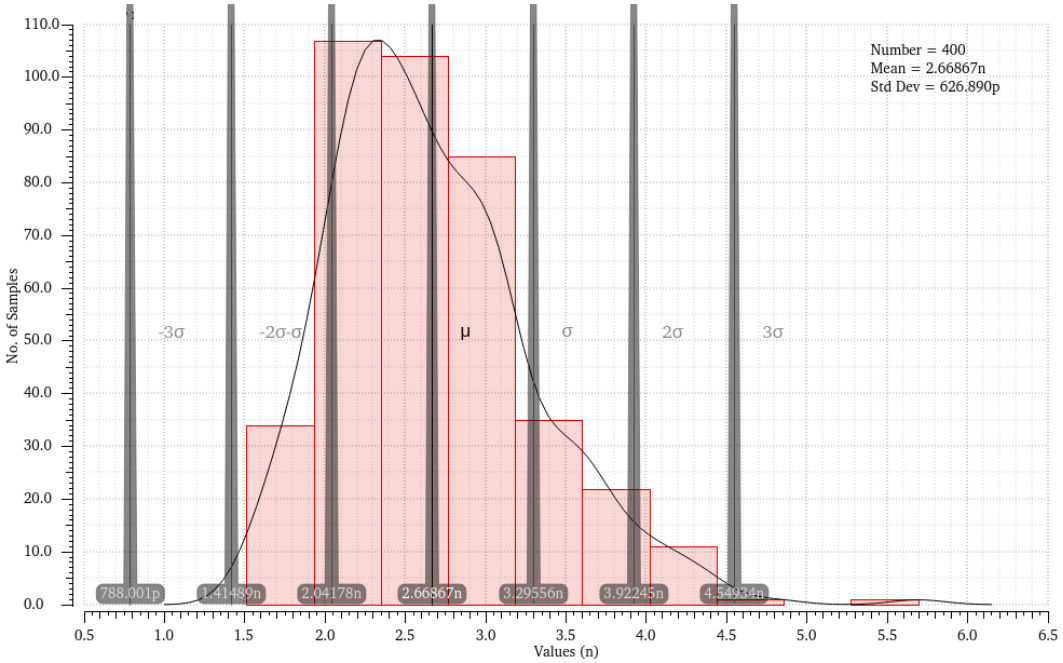
$$I_D = \left(\frac{W}{L}\right)_2 \left(\frac{W}{L}\right)_3 I_t^2 \exp\left(\frac{V_{ov1} - V_{th}}{nV_T}\right) \frac{1}{I_{IN}} \tag{4.12}$$

TABLE 4.2: Summary of the Monte Carlo and DC simulations of the bias current generator

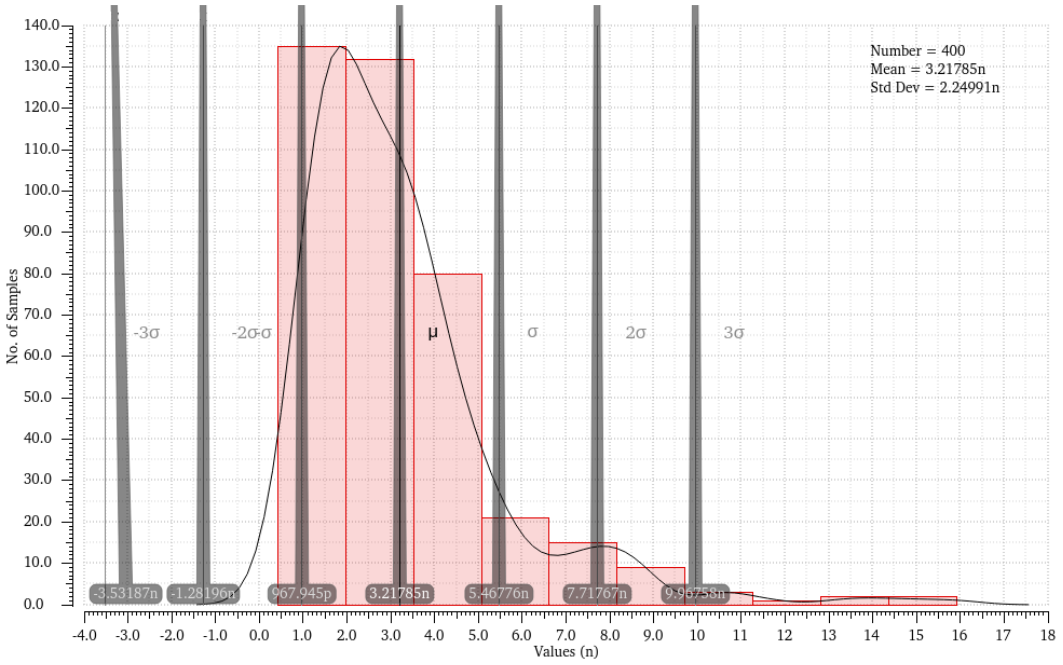
		With Transistor			With Resistance		
Output	I_SEL	Dc [nA]	Mean [nA]	Std. Dev. [nA]	Dc [nA]	Mean [nA]	Std. Dev. [nA]
I_{OPAMP}	000	0	0	0	0	0	0
	001	2.6	2.6	0.6	2.6	3.21	2.2
	010	5.2	5.3	1.1	5.3	6.4	4.5
	011	7.8	8	1.6	7.9	9.6	6.5
	100	10.4	10.6	2.2	10.6	12.8	8.8
	101	13	13.3	2.7	13.3	16	10.7
	110	15.6	15.9	3.2	15.9	19.2	13
	111	18.3	18.6	3.7	18.6	22.4	15
$I_{TailFilter}$		260	262	54	261	318	216

In Fig.4.23, a Monte Carlo simulation of the output current of the IDAC least significant bit shows that the solution using the transistor instead of the resistance has a lower standard deviation. Table 4.2 summarizes the results of the Monte Carlo simulation, on 400, for all output current of the bias generator and combination of the control word *I_SEL*. In the solution with the transistor, the mean value of the output current of the Monte Carlo simulation is similar to that of the value from the Dc simulation. Conversely, using the resistance, the average value of the current differs significantly from the Dc value. This may be due to the exponential dependence of the current on the resistance value, as showed 4.9 in and 4.11. The same justification can be given for the standard deviation, which is 4 times larger in the case with the resistance than with the transistor.

In conclusion, the proposed current generator for the op-amp and tail filter resistance bias current, showed in Fig. 4.22, that use a transistor instead of a resistance to generate a current in the nanoampere range and an IDAC as a mean to compensate the effect of process variation is considered suitable for the application.

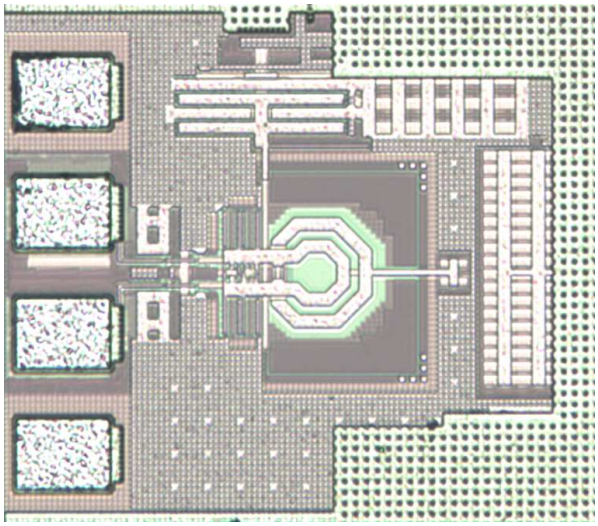


(A) *With transistor*

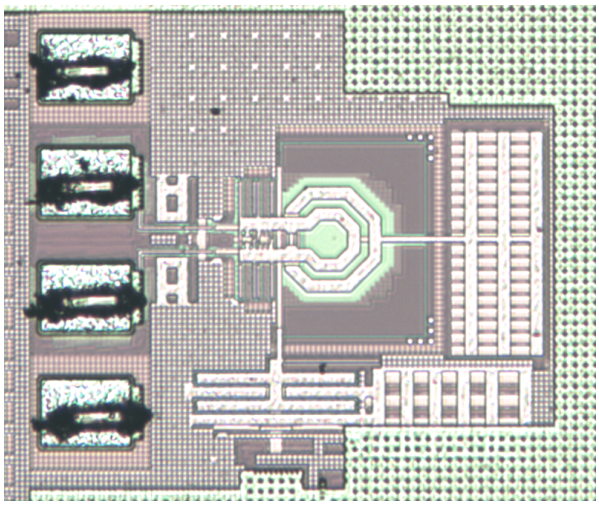


(B) *With resistance*

FIGURE 4.23: Montecarlo simulation of the LSB current of the IDAC



(A) *Redesign A*



(B) *Redesign B*

FIGURE 4.24: Die photograph. Core area is ≈0.07 mm^2.

4.4.4 Measurements Results

In this section the measurements of both redesign of class-C oscillator are compared with the post-layout simulations. Prototypes of the proposed class-C oscillator, with the improved op-amp, were fabricated in a bulk 28 nm CMOS technology. The die photographs are shown in Fig. 4.24. The core area is approximately 0.07 mm^2 for both design.

The chip has been placed in a printed circuit board that is used to provide dc supplies and control signals to the chip; probes are used to contact the pads connected to the output buffer of the oscillator. By means of serial interface, the chip is programmed in order to control the IDAC of the current tail generator and the control word of the capacitor bank. The supply voltage of the oscillator is $V_{dd} = 0.9$ V , while for for the op-amp is 1.8 V.

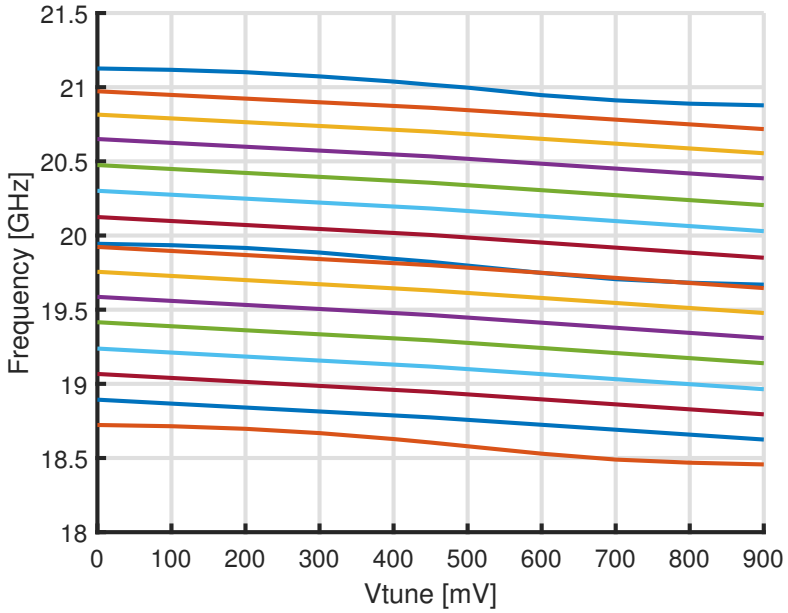


FIGURE 4.25: Measured frequency against the varactor tuning voltage for all the sub-band (coarse tune).

Design A

In the *Design A*, the op-amp in Fig 4.24a is used. Figure 4.25 shows the measured frequency as the digital control word of the capacitance bank and the tuning voltage,V_{Tune}, of the varactor are changed. The measured frequency of oscillation spans from 18.5 GHz to 21.1 GHz, covering a 12% tuning range.

The phase noise of the oscillator was measured for different values of the bias current I_{Core}, and of the oscillation frequency f_0. Figure 4.26 shows the measured phase noise for $I_{\text{Core}} = 22.3\,\text{mA}$, with $f_0 = 19.5\,\text{GHz}$, $V_{\text{Tune}} = V_{dd}$, and $V_{\text{Ref}} = 0.6\,\text{V}$. At 1 MHz frequency offset the measured phase noise is -111.5 dBc/Hz, while at 100 kHz frequency offset it is -85 dBc/Hz; the $1/f^3$ corner frequency is around 450 kHz.

In Fig. 4.27, phase noise measurements (solid line) and post-layout simulations (dashed lines) are compared, for a set of offset frequencies, as I_{Core} is changed. In the $1/f^2$ noise region, the measurements are in agreement with the simulations in the limit of the accuracy of the phase noise analyzer. As the current increases, the phase nose improves due to the increase of the amplitude of the oscillation. Doubling the current, from 10 mA to 20 mA lead to an improvement of 6 dB, as expected from the Leeson's formula. Also in the $1/f^3$ noise region, for low values of I_{Core}, there is a good agreement between measurements and simulations, while there is a substantial difference for larger values of I_{Core} and, thus, of the oscillation amplitude. This can

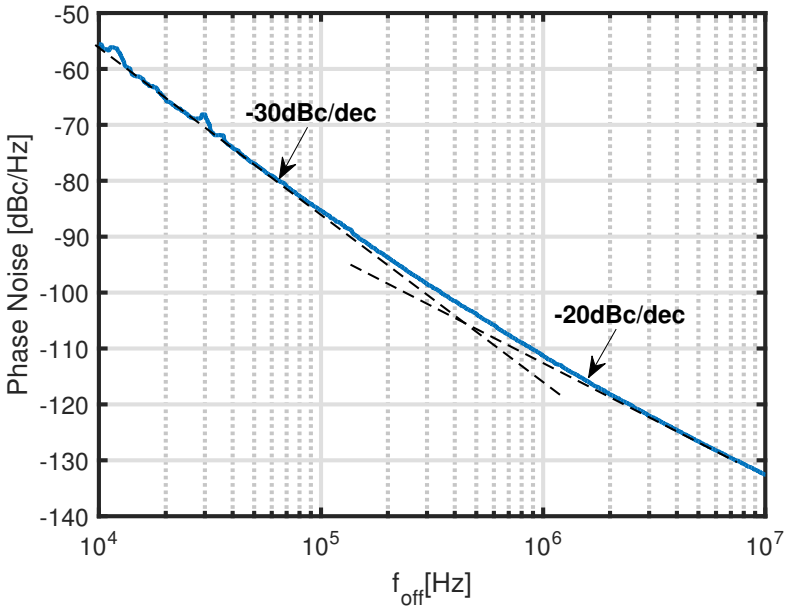


FIGURE 4.26: *Design A*, measured phase noise versus offset frequency for $I_{\text{core}} = 22.3\,\text{mA}$ at $f_0 = 19.5\,\text{GHz}$, $V_{\text{ref}} = 0.6\,\text{V}$, and $V_{\text{Tune}} = V_{\text{dd}}$.

be attributed to a bad modelling of flicker noise of the transistors in triode region.

The VCO phase noise performance across the tuning range is shown in Fig. 4.28, with $I_{\text{Core}} = 22.3\,\text{mA}$, $V_{\text{Ref}} = 0.6\,\text{V}$ and $V_{\text{Tune}} = V_{dd}$. There is a good agreements between simulation and measurement: in the white noise region the measured phase noise variation is less than 1 dB, while in the flicker region the variation is around 3 dB. The larger variation at small offset can be attributed to AM-PM conversion: changing the frequency, and thus the configuration of the capacitor bank, the ratio between fixed capacitance and non-linear capacitance change, therefore, making the oscillator more sensitive to amplitude noise.

The VCO phase noise performance has been evaluated also across all the sub-band. Figure 4.29 shows the measured (solid line) and simulated (dashed line) phase noise, at different offset frequency, against the tuning voltage V_{Tune}, with $I_{\text{Core}} = 22.3\,\text{mA}$, $V_{\text{Ref}} = 0.6\,\text{V}$ and f_0 around 19.5 GHz. While in the white noise region there is a good agreement between measurement and simulation, in the flicker region, especially in the middle of the tuning voltage range, the discrepancy is considerable. The reason for this behaviour is that, around $V_{\text{Tune}} = V_{dd}/2$, the variation of the capacity with the tuning voltage is maximum, making the oscillation frequency more sensitive to noise and external disturbances. In Fig. 4.30 the measured phase noise

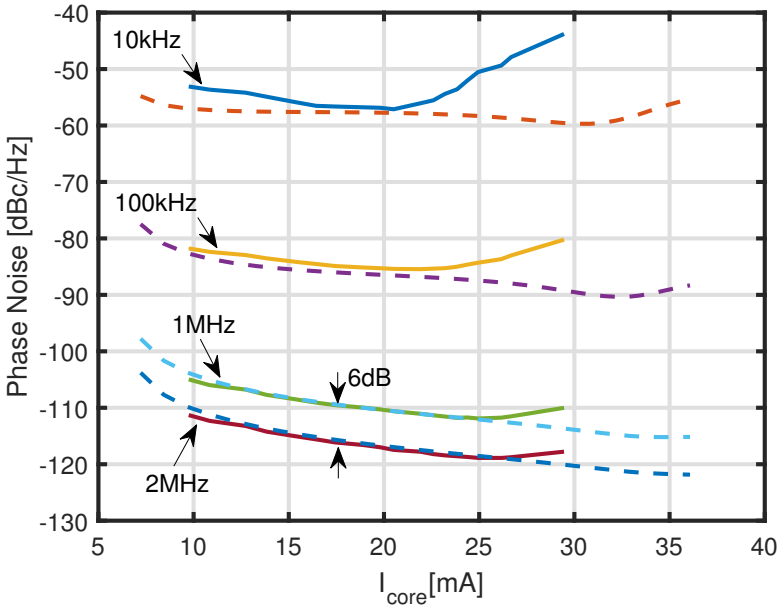


FIGURE 4.27: *Design A*, measured (solid lines) and simulated (dashed lines) phase noise versus I_{Core} for different offsets from the 19.5 GHz carrier frequency with $V_{\text{Ref}} = 0.6\,\text{V}$ and $V_{\text{Tune}} = V_{dd}$.

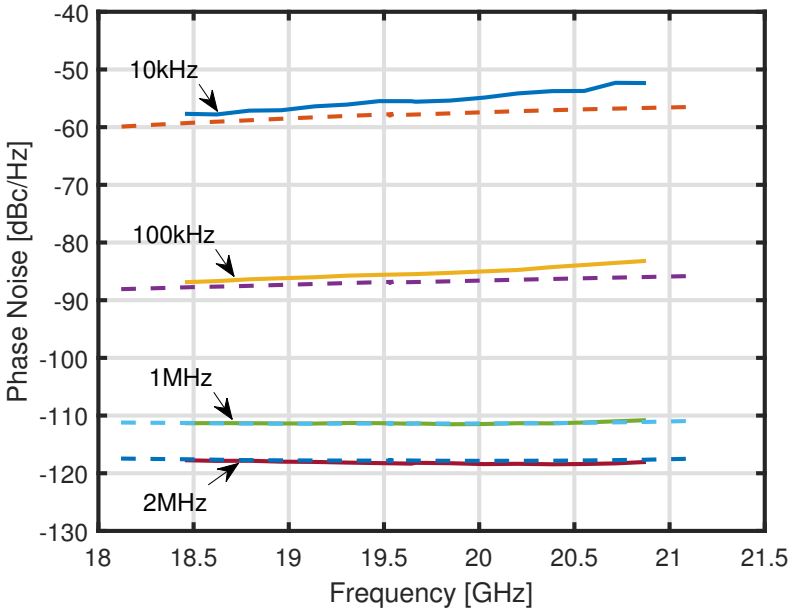


FIGURE 4.28: *Design A*, measured (solid lines) and simulated (dashed lines) phase noise versus f_0 for different offsets frequency with $I_{\text{Core}} = 22.3\,\text{mA}$, $V_{\text{Ref}} = 0.6\,\text{V}$ and $V_{\text{Tune}} = V_{dd}$

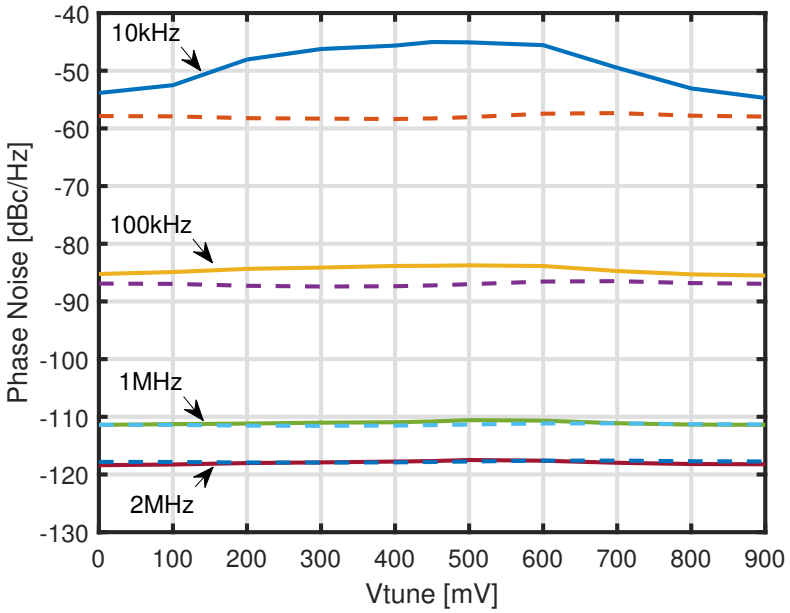


FIGURE 4.29: *Design A*, measured (solid lines) and simulated (dashed lines) phase noise versus V_{Tune} for different offsets frequency with $I_{\text{Core}} = 22.3\,\text{mA}$, $V_{\text{Ref}} = 0.6\,\text{V}$

sideband, with $I_{\text{Core}} = 22.3\,\text{mA}$, $V_{\text{Ref}} = 0.6\,\text{V}$ and $V_{\text{Tune}} = V_{dd}/2$, is showed; it is possible to notice spur frequencies, coming from the supply, at 12 kHz, 30 kHz and 100 kHz.

And finally we compare this new version of the oscillator with the old design. In Fig. 4.31, phase noise measurements of the new design (solid line) and old design (dashed lines) are compared, for a set of offset frequencies, as I_{Core} is changed. The improvement is significant, especially at low offset frequency, where the phase noise is up to 10 dB lower. This show again, the importance of careful design of the op-amp.

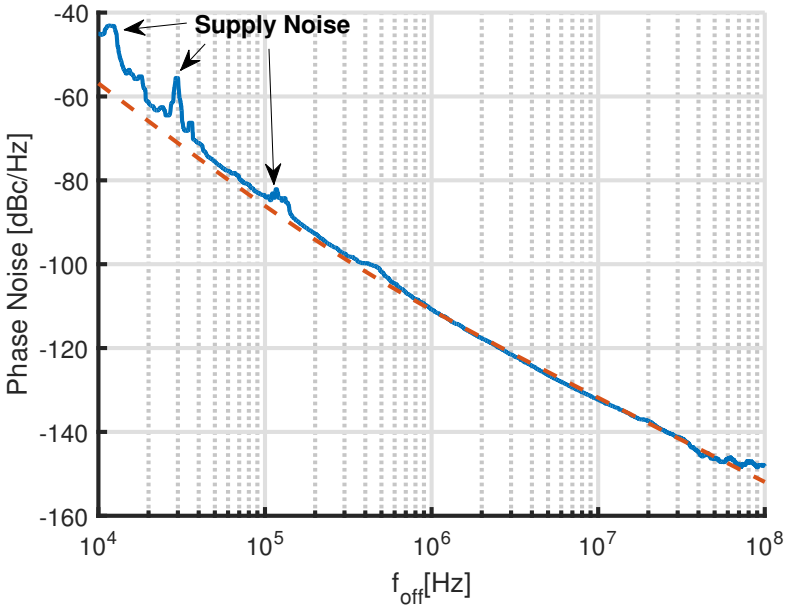


FIGURE 4.30: *Design A*, measured phase noise versus offset frequency for $I_{\text{core}} = 22.3\,\text{mA}$ at $f_0 = 19.5\,\text{GHz}$, $V_{\text{ref}} = 0.6\,\text{V}$, and $V_{\text{Tune}} = V_{\text{dd}}/2$.

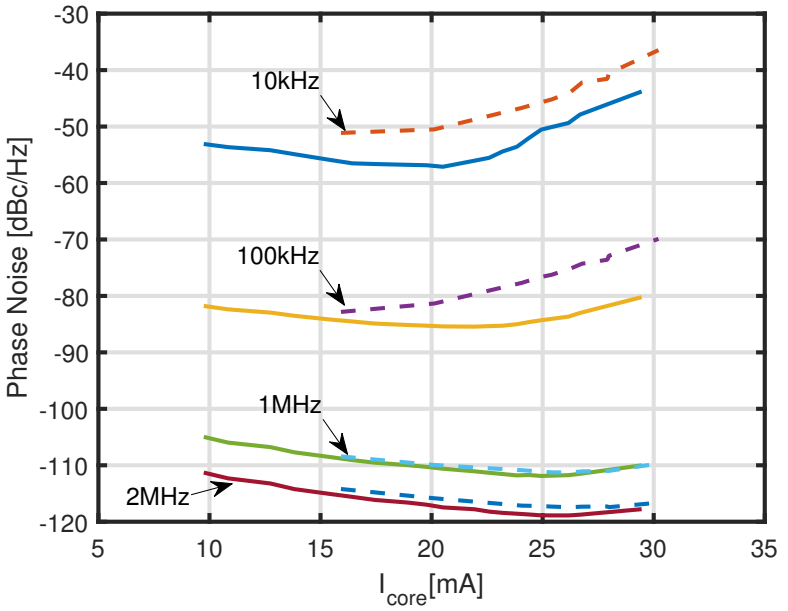


FIGURE 4.31: Measured phase noise of the *Design A*(solid lines) and old design (dashed lines) versus I_{Core} for different offsets from the 19.5 GHz carrier frequency with $V_{\text{Ref}} = 0.6\,\text{V}$ and $V_{\text{Tune}} = V_{dd}$.

Design B

In the *Design B*, the op-amp in Fig. 4.24b is used. Since the core of the oscillator is the same as in the original design and in *Design A* as well, the tuning characteristic (Fig.4.25) is also valid for this design.

The phase noise of the oscillator was measured for different values of the bias current I_{Core}, and of the oscillation frequency f_0. Figure 4.26 shows the measured phase noise for $I_{\text{Core}} = 23\,\text{mA}$, with $f_0 = 19.5\,\text{GHz}$, $V_{\text{Tune}} = V_{dd}$, and $V_{\text{Ref}} = 0.6\,\text{V}$. At 1 MHz frequency offset the measured phase noise is -112 dBc/Hz, while at 100 kHz frequency offset it is -86 dBc/Hz; the $1/f^3$ corner frequency is around 500 kHz.

In Fig. 4.33, phase noise measurements (solid line) and post-layout simulations (dashed lines) are compared, for a set of offset frequencies, as I_{Core} is changed. While, the phase noise across the tuning range (coarse tuning) is presented in Fig. 4.34. Also in this design, there is a good agreement between measurements and simulations, therefore, the considerations made for *Design A* are also valid here.

In Fig 4.35 a comparison of the phase noise versus I_{Core} between *Design B* and the old design is shown. The improvement is about 10 dB in the flicker region and 2 dB in the white noise region for 25 mA.

Finally Fig. 4.36 show a comparison between the measured phase noise of the *Design A* and *Design B* against the I_{Core} for different offset frequency. At low current, the two design show the same performance, while there is a large discrepancy, 6 dB at 10 kHz, for current above 25 mA. It is not straightforward to trace the reason for this behaviour since, in simulation, both designs show almost the same performance. Therefore, this discrepancy can be attributed either to process variation or to a bad modelling of the transistors. A possible explanation can be found in the leakage current of the cross-coupled pair.

The leakage current is provided by the ota. This results in a steady state error between the reference voltage V_{REF} and the voltage at the common source of the cross-coupled pair V_{cs}. In simulation this error is considered acceptable. Other than the dimension of the transistor, the leakage current depends on the gate-source voltage of the transistor, and therefore on I_{Core}. The transistor model might not be accurate at high values of I_{Core}, thus underestimates the leakage current. The current that the ota in Fig. 4.24a can provide is limited, therefore the dynamic bias might not work correctly. This can explain why the *Design B* with the voltage buffer shows better performance as it can deliver higher leakage current and, thus, operates at higher

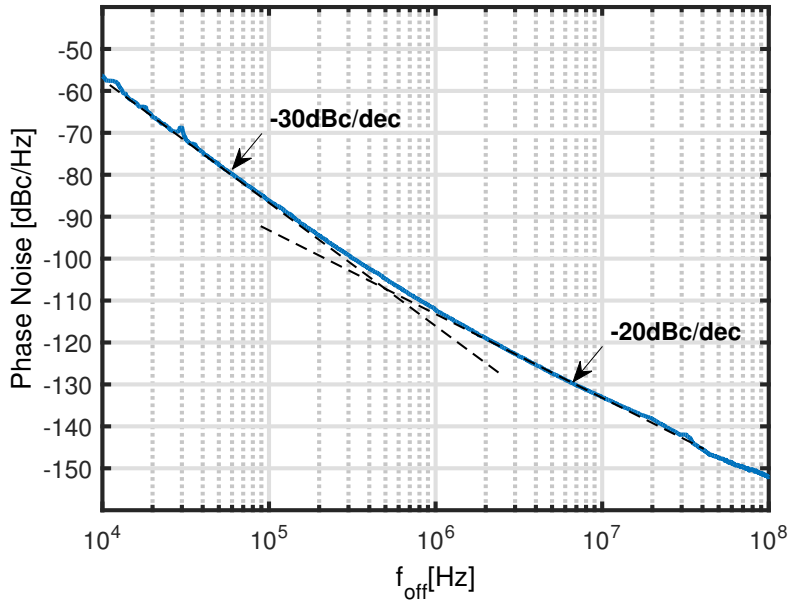


FIGURE 4.32: *Design B*, measured phase noise versus offset frequency for $I_{\text{core}} = 23\,\text{mA}$ at $f_0 = 19.5\,\text{GHz}$, $V_{\text{ref}} = 0.6\,\text{V}$, and $V_{\text{Tune}} = V_{\text{dd}}$.

bias current.

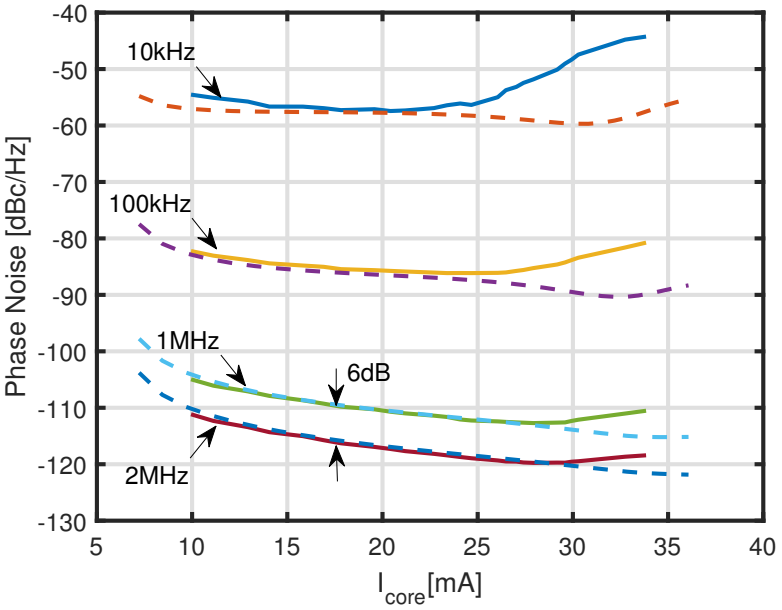


FIGURE 4.33: *Design B*, measured (solid lines) and simulated (dashed lines) phase noise versus I_{Core} for different offsets from the 19.5 GHz carrier frequency with $V_{\text{Ref}} = 0.6\,\text{V}$ and $V_{\text{Tune}} = V_{dd}$.

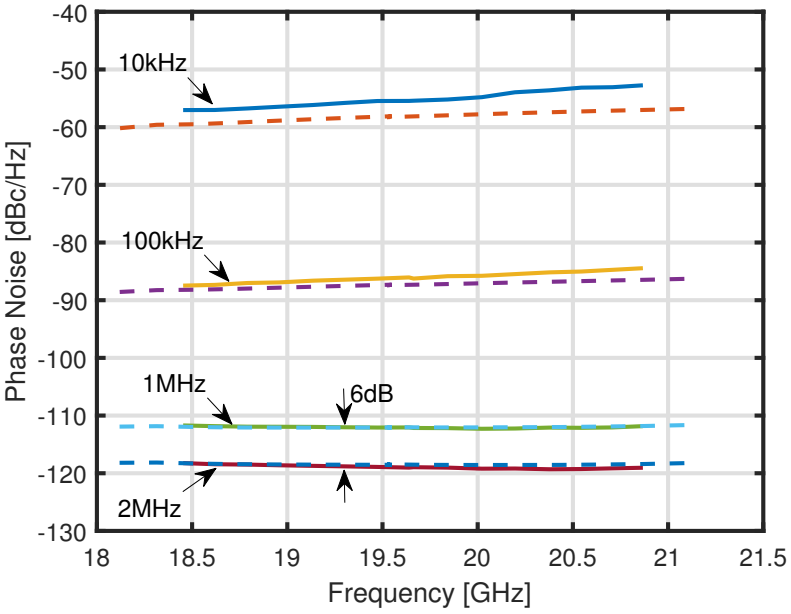


FIGURE 4.34: *Design B*, measured (solid lines) and simulated (dashed lines) phase noise versus f_0 for different offsets frequency with $I_{\text{Core}} = 23\,\text{mA}$, $V_{\text{Ref}} = 0.6\,\text{V}$ and $V_{\text{Tune}} = V_{dd}$

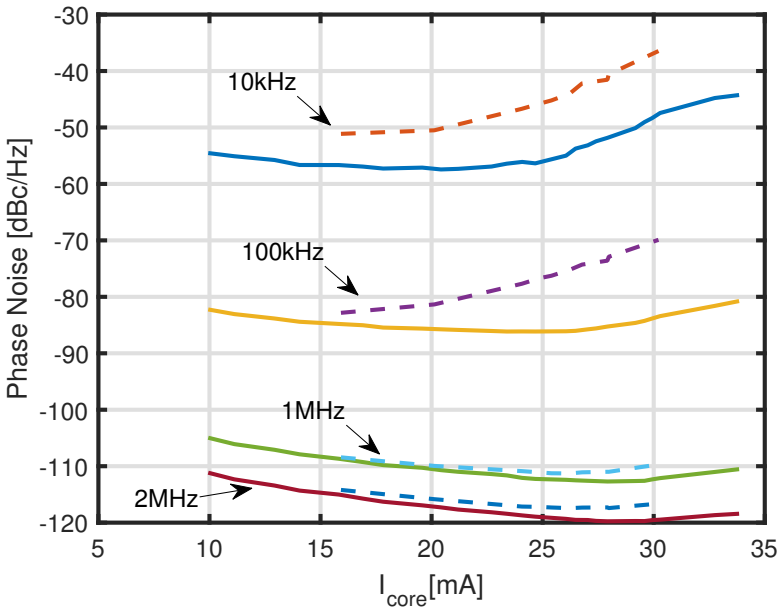


FIGURE 4.35: Measured phase noise of the *Design B* (solid lines) and old design (dashed lines) versus I_{Core} for different offsets from the 19.5 GHz carrier frequency with $V_{\text{Ref}} = 0.6\,\text{V}$ and $V_{\text{Tune}} = V_{dd}$.

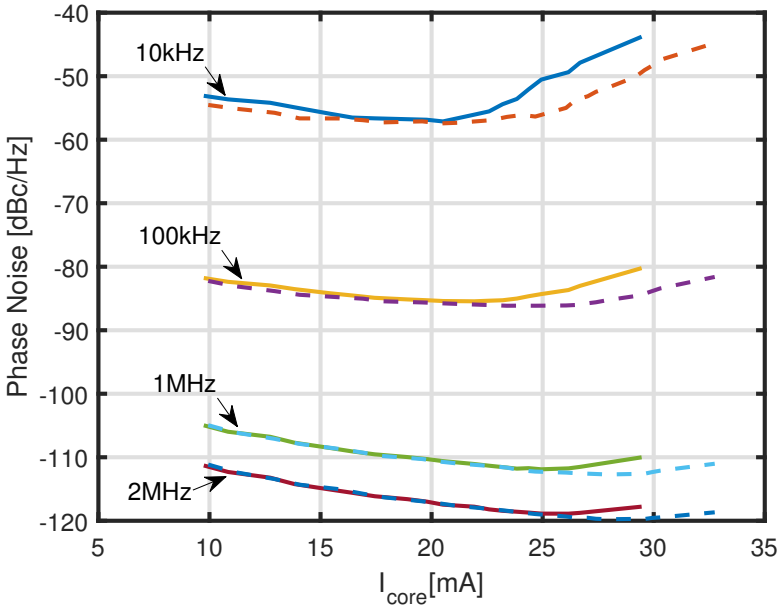


FIGURE 4.36: Comparison between the measured phase noise of the *Design A* (solid lines) and *Design B* (dashed lines) versus I_{Core} for different offsets from the 19.5 GHz carrier frequency with $V_{\text{Ref}} = 0.6\,\text{V}$ and $V_{\text{Tune}} = V_{dd}$.

4.4.5 Comparison with the State-Of-The-Art

The performances of the proposed Class-C VCOs are summarized in Table 4.3, and compared to the state-of-the-art; for a fair comparison phase noise performance has been normalized to a 19.5 GHz carrier. Both the phase noise performance and the figure-of-merit is in line with those of the other reported mm-wave VCOs. In particular, if we consider other two mm-Wave design [40, 47], the performance in the flicker region are very similar, while in the white region Class-C phase noise is 3 dB lower. The main difference of this design is that no particular tuning of the second-harmonic tank impedance is required.

TABLE 4.3: Performance summary and comparison with previously published VCOs in 28 nm CMOS technologies.

	JSSC 2017 [38]	JSSC 2016 [47]	JSSC 2018 [40]	VLSI 2017 [48]	JSSC 2018 [49]	**This Work**	**This Work**	**This Work**
Topology	Class-B Implicit resonance	Class-F	Class-$F_{2,3}$	Pulse taill feedback	Class-B	**Class-C**	**Class-C Design A**	**Class-C Design B**
Tech. [nm]	28	40	28	180	40	**28**	**28**	**28**
V_{dd} [V]	0.9	0.7	1.0	1.2	0.95	**0.9**	**0.9**	**0.9**
Freq. [GHz]	3.33	57.8	27.3	4.55	25	**19.5**	**19.5**	**19.5**
Tuning range [%]	27	25	14	5.5	26	**12**	**12**	**12**
Power [mW]	6.8	24	12	1.35	16	**14.4**	**20**	**20**
Phase noise @1 MHz [dBc/Hz]	-130	-100	-106	-123	-110	**-108.5**	**-111.5**	**-112**
Eq. phase noise referred to 19.5 GHz @1 MHz [dBc/Hz]	-114	-109.5	-109	-110.8	-112	**-108.5**	**-111.5**	**-112**
Phase noise @100 kHz [dBc/Hz]	-105	-73	-83	-103.6	-83	**-83**	**-85**	**-86**
Eq. phase noise referred to 19.5 GHz @100 kHz [dBc/Hz]	-89	-82.5	-86	-91	-85	**-83**	**-85**	**-86**
FoM [dBc/Hz]	-192	-181	-184	-195	-196	**-183**	**-185**	**-185**
Core area [mm^2]	0.19	0.13	0.15	NA	0.1	**≈0.07**	**≈0.07**	**≈0.07**

4.5 Conclusions

In this chapter, two millimeter-Wave voltage- controlled oscillators have been presented. Both fabricated in a 28 nm bulk CMOS technology with a supply voltage of 0.9 V.

The first one, an hybrid Class-B/D, showed a phase noise of -98 dBc/Hz at 1 MHz offset frequency from a carrier of 20 GHz with a power consumption of 15 mW. In this design is noticeable the presence of a large flicker noise upconversion. Simulations pointed out that this contribution is mainly due to the cross-couple pair and the tail generator transistors.

An analysis, carried out using verilog-A model for the transistor, showed that, when long channel transistor are used, the Class-C operation is able to prevent the upconversion of flicker noise from the cross-coupled pair transistors. This analysis also showed that short channel effect are the main reason why, in practice, when AMPM is not the dominant source of noise, flicker noise still appears in the phase noise sideband.

On the other hand, Class-B oscillator are also able to prevent the upconversion of flicker noise provided that the common mode impedance is made to resonate at the second harmonic. Nevertheless, modelling the common mode return path can be a challenging task at mm-Wave frequencies.

For this reason, despite the short channel effect, a Class-C oscillator has been designed. Due to its intrinsic property of preventing the upconversion of flicker noise from cross-coupled pair, Class-C oscillator is a robust and wideband alternatives to Class-B topology as it doesn't require tuning of the common mode impedance.

The first design of the Class-C, here presented, showed a phase noise of -83 dBc/Hz at 100 kHz and -108.5 dBc/Hz at 1 MHz from an 19.5 GHz carrier while absorbing 14.4 mW from the supply, it also feature a 12% of tuning range.

In this design, the performance are limited by op-amp of the dynamic bias loop. The dynamic bias loop is an important part of the circuit as it allows to maximize the amplitude of oscillation, which is instrumental for low phase noise performances, while ensuring a reliable start-up of the oscillator. It is therefore fundamental to design an op-amp with low noise performance.

In the last section of this chapter, two redesigns of the op-amp are presented. The aim was to reduce the flicker noise of the differential pair of the op-amp. This was done by biasing the transistor in weak inversion with a large gate area and low bias current.

The difference between *Design A* and *Design B* is that the second one also includes a voltage buffer at the output.

Being the core of the oscillator the same for both redesigns and original design, the oscillation frequency is the same as the control word of the capacitor bank or the tuning voltage are changed.

Since the oscillator core is the same for the redesigns and the original design, they all feature the same tuning range of 12%.

In both redesign, the measured phase noise improvements of the Class-C oscillator compared to the original design are significant: almost 10 dB in the flicker region.

Design A achieves a phase noise of -111.5 dBc/Hz at 1 MHz offset and -85 dBc/Hz at 100 kHz from the 19.5 GHz carrier, drawing 22.3 mA from the supply voltage; while for the *Design B*, the phase noise is -112 dBc/Hz and -86 dBc/Hz at 1 MHz and 100 kHz respectively with 23 mA of I_{Core}.

The comparison with the other state-of-the art shows that, despite the short channel effect, the performance of the Class-C, also taking in account the different supply voltages and oscillation frequencies, compares very well with other topologies. We conclude that Class-C oscillator is a valid alternative to other topologies that employ common-mode resonance.

It also worth to mention that, despite the large filter capacitance of the op-amp, the total area of the oscillator is only 0.07 mm^2.

Chapter 5

Class-C: 4^{th} Harmonic Extraction

As seen in the chapter 1 , the allocated band for the future generation of high performance automotive radar is is between 76 GHz and 81 GHz. In chapter 4, the class-C oscillator has been designed to work around 20 GHz, therefore, a frequency multiplication by a factor of 4 is needed.

In this chapter, after a brief review of frequency multiplication circuits, a method for extracting the 4^{th} harmonic from the class-C oscillator is be presented.

5.1 Review of Frequency Multiplication Circuits

Several multiplier circuits in mm-wave are introduced in [50], that can be divided in three categories:

1. mixer based [51, 52];
2. device nonlinearity based [53, 54];
3. injection-lock based [50, 55, 56].

Figure 5.1a shows the conceptual diagram of a mixer-based doubler. In this approach, a Gilbert mixer is often employed, where both RF and LO port are driven by same input signal; the resulting output signal has a component at twice of the input frequency. The advantage of this solution is the wide frequency range of operation. On the other hand, the large DC component generated at the output may saturate the mixer and, therefore, limit the conversion gain. Moreover, in order to suppress the fundamental component, a double balance mixer topologies are employed, with the drawback of large capacitance at the input port that limit the maximum operation frequency.

An alternative approach uses a nonlinear active device to generate the harmonics of the input signal, then, the desired frequency is selected by

means of an band pass LC filter. A simple schematic of this approach is depicted in Fig. 5.1b. Biasing the device to operate in class-B or class-C reduces the conduction angle of the MOS and, therefore, maximize the conversion efficiency. Nevertheless, the amplitude of the fundamental is much larger than its harmonics and, achieving adequate suppression, by means of integrated LC filters, is troublesome due to the low quality factor. A common solution to cancel out the fundamental frequency at the output, known as push-push pair [57, 58], is shown in Fig.5.1c. With balanced inputs, the fundamental component of the total drain current is at twice the input signal frequency. As a drawback, while the input is differential, the output is single ended. At high frequency, differential signals are preferred over single ended ones to avoid the need to accurately model the current return path. Moreover, the gain conversion could be low if a high order harmonic is selected.

In a injection-lock approach, Fig. 5.1d, a nonlinear device is also used to generate the harmonics of the input signal. After that, the desired harmonic will inject to lock the VCO with free-running frequency close to that of the harmonic. Compared to a simple push-push multiplier, a differential output can be easily obtained by selecting a differential oscillator topology and the trade-off between device size and output swing is mitigated, being the amplitude of the output signal primarily determined by the DC biasing current of the oscillator instead of the 2nd harmonic component of the driving push-push pair. The output swing is also at first order independent of the input signal swing. The drawback is that bandwidth is limited by the locking-range of the VCO which is usually quite narrow; moreover, outsidethe locking-range the phase noise is dominated by the VCO, that is, in general, higher than the input signal [59].

More complex approaches use a combination of the techniques listed above: for instance using a push-push pair combined to a mixer to obtain the third harmonic as in [60, 61], or a chain of two push-push frequency doublers for the fourth harmonic [62].

In principle, all of these techniques can be applied to obtain the 4th harmonic of the class-C oscillator. A smarter solution, depicted in Fig. 5.2, uses the common nodes of the oscillator to extract the second harmonic of the fundamental frequency. The operating principle is the same as a push-push based multiplier; therefore, these oscillator are commonly known as push-push VCO [63–66]. Coupling the tail filter in a class-B oscillator, to form a transformer, also enables the extraction of the second harmonic [67, 68].

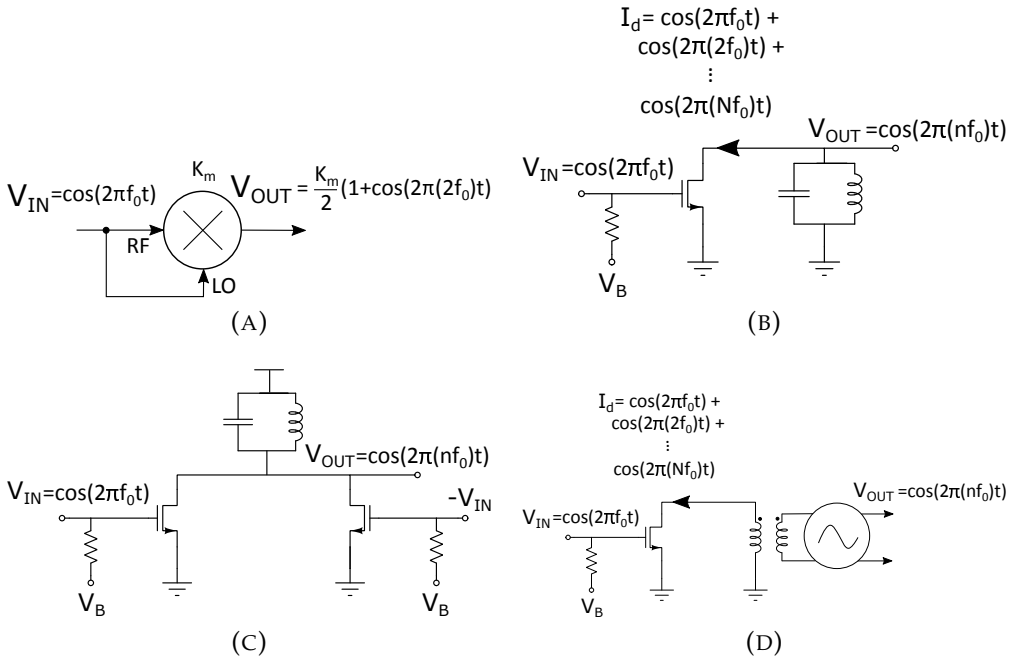


FIGURE 5.1: Frequency multiplier based on a mixer(A). Frequency multiplier based on device nonlinearity(B), push-push configuration to suppress the fundamental component and odd harmonics(C) and injection lock approach(D).

Another example of harmonic extraction is [40]: the tank of class-F oscillator is designed to resonate also at the second and third harmonic, allowing to reduce the flicker upconversion from the cross-coupled pair, then, using a passive ac-coupling circuit and a two stage power amplifier, the third harmonic is obtained.

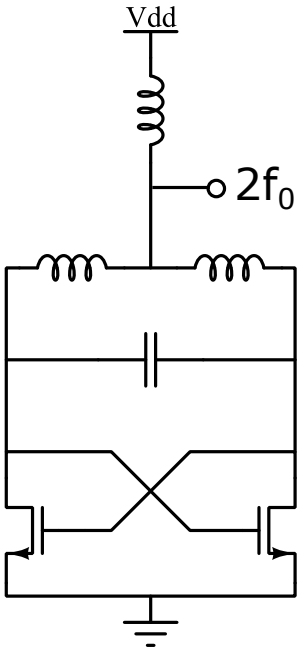


FIGURE 5.2: Schematic of a conventional push-push cross coupled oscillator.

5.2 4th Harmonic Extraction

One of the main characteristic of a class-C oscillator is the large tail capacitance (C_{tail}). This capacitance is composed of: 1) the parasitic output capacitance of the tail current generator; 2) the parasitic source capacitance of the transistors of the cross-coupled pair and 3) explicit capacitance. If the transistors of the cross-coupled pair are biased in order to not work in triode region throughout the oscillation period, the current going out the tail capacitance consists of a train of impulses, whose period, being a common mode path, is half of the fundamental period. This train of current impulses is rich of even order harmonic. Therefore, we want to extract the 2^{th} harmonic of this current.

The common mode path of the current has an inductive behavior that filters high order harmonics of the current; despite that, the simulations shows, in the worst case, a 4th harmonic current of around 300 uA. The idea is to exploit part of the ac current path, that, as stated before, has an inductive behavior, and couple it with an inductor to make up a magnetic transformer.

Figure 5.3 shows the proposed solution for the 4^{th} harmonic extraction.

L_{P1} is the parasitic inductance of the path that connects the tail capacitance to the common source of the cross-couple pair; while L_{P2} connects the common source to the primary side of the transformer made by L_3 and L_4.

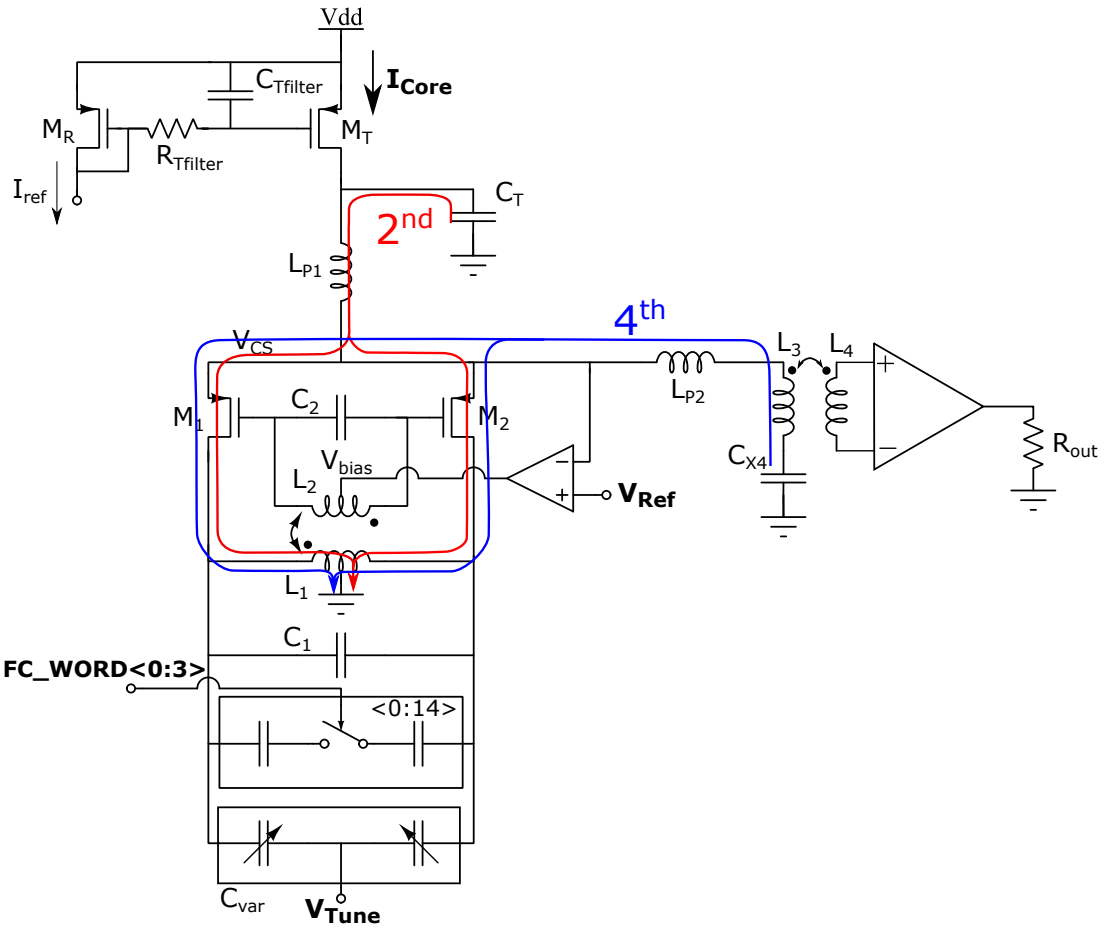


FIGURE 5.3: Schematic of the class-C oscillator with the proposed solution for the extraction of the 4^{th} harmonic.

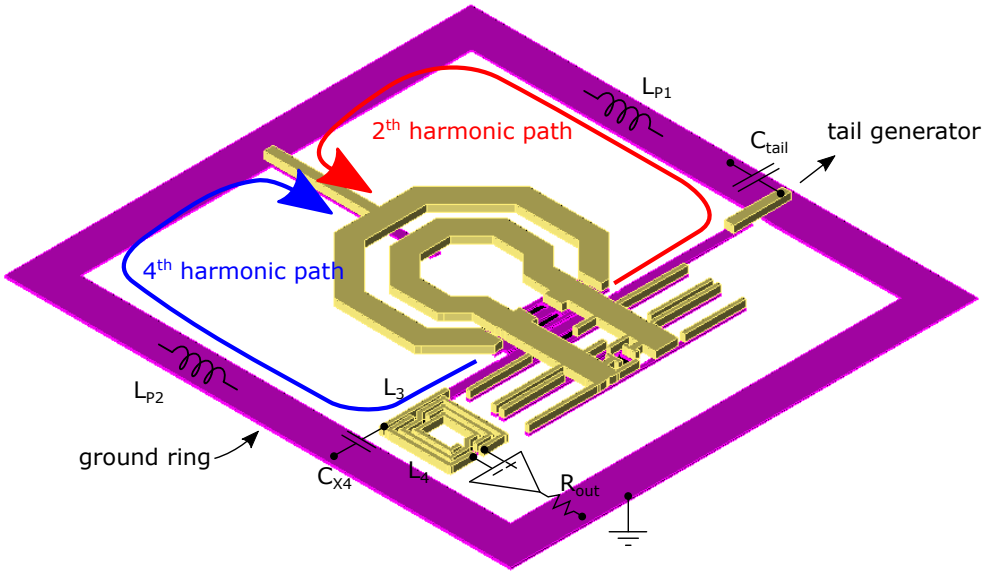


FIGURE 5.4: 3D view of the class-C oscillator with transformer for the 4th harmonic extraction.

In this solution the path for the harmonics of current has been split. The second harmonic is provided by the tail capacitance; while the fourth harmonic comes from C_{x4}. In this way, selecting the appropriate value for C_{x4}, it is possible to make the path that consists of C_{x4}, L_3, L_{P2} and the common mode of the tank, to resonate at the 4th harmonic, thus providing a low impedance path for current. This in turn increases the magnitude of the output voltage at the secondary side of the transformer.

Figure 5.4 shows the 3D view of the oscillator with the path of the second and fourth harmonic of the tail current and the transformer for the the fourth harmonic extraction.

The simulated inductance value for the primary side of the transformer is $L_3 = 16\,\text{pH}$, with quality factor $Q_3 = 16$ at 80 GHz; while at the secondary side, $L_4 = 180\,\text{pH}$ and $Q_4 = 12$ at 80 GHz. The coupling factor is 0.25.

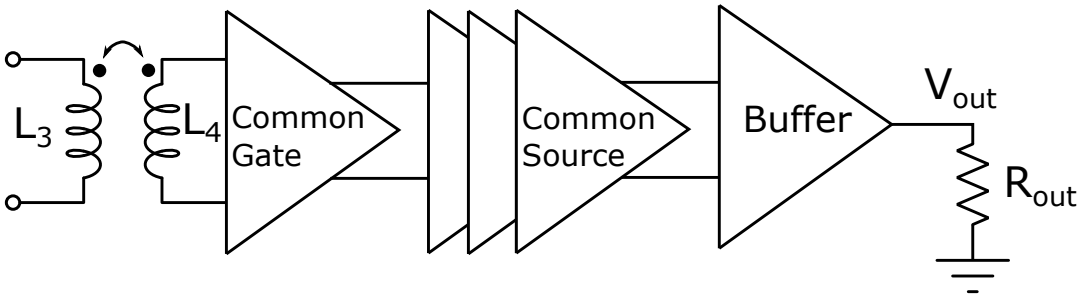


FIGURE 5.5: Block diagram of the amplifier.

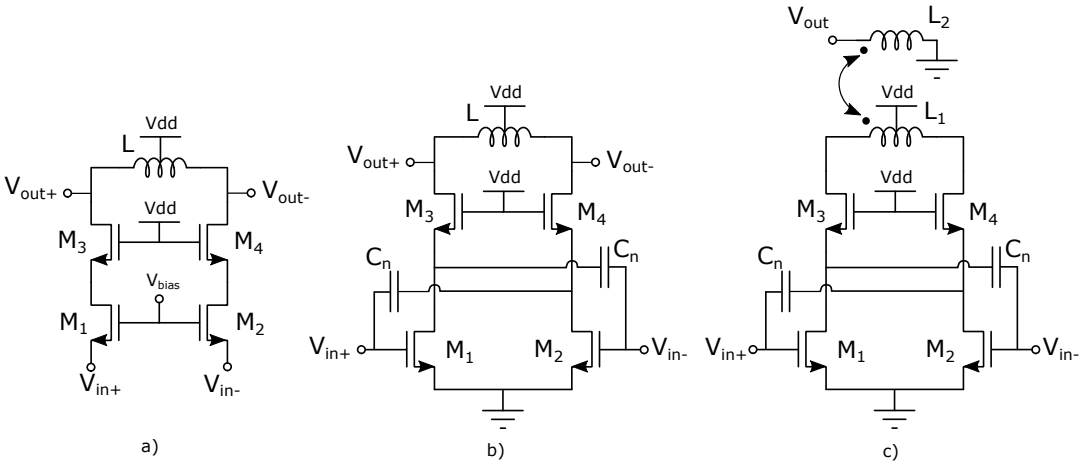


FIGURE 5.6: Schematics of: a) common gate stage, b) common source stage, c) common source buffer stage.

5.3 80 GHz Amplifier

The secondary side of the transformer is connected to an amplifier that drives the 50 Ω input resistance of the subsequent stage or, as in this case, of the phase noise analyzer.

A differential approach has been chosen for the amplifier design; Fig. 5.5 shows block diagram of the amplifier. The general idea is to disturb the operation of the oscillator as little as possible; for this reason, the first stage of the amplifier is a differential common gate cascode Fig.5.6a). The input resistance of the amplifier is 125 Ω with 6 mA of bias current. The mosfets are sized with a minimum channel length of 30 nm and a width of 12 um. Figure 5.7 shows the voltage at input of the common gate from a post-layout simulation of the oscillator and the amplifier considering also the interconnections and pads.

The subsequent 3 stages are pseudo-differential common source cascode stages with a resonant load Fig.5.6b). All the transistors are sized with minimum channel length and increasing width and bias current along the stages. Therefore, the differential pair of the first common source stage has a width

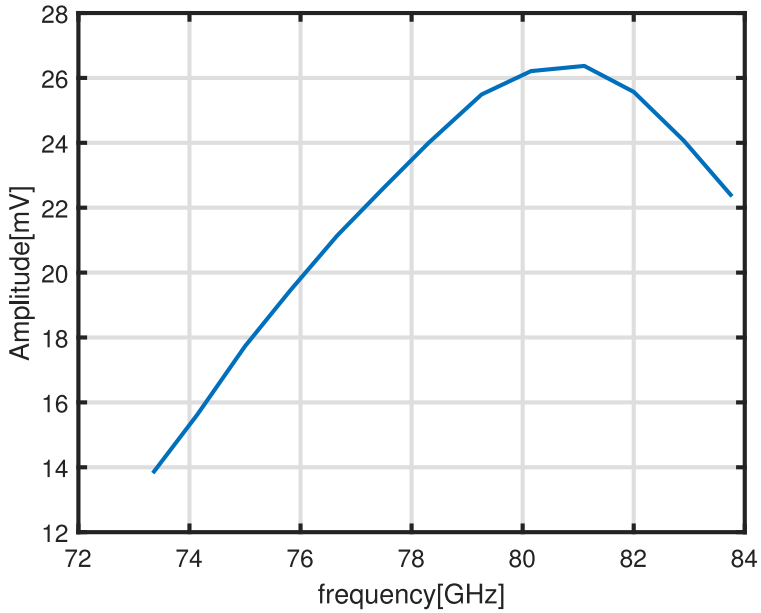


FIGURE 5.7: Differential input voltage of the common gate stage.

of 10 um and a total bias current of 5.6 mA, the second stage has a width of 14 um and a bias current of 7.6 mA while the third one has a width of 28 um and a current of 12 mA. Simulations show the negative effect of the coupling between the output and the input of each stage caused by the gate-drain capacitance. Therefore, to ensure the stability of the amplifier and to increase the gain, neutralization capacitances are included. The cascode transistors also help increase the reverse isolation and to increase the output resistance. Finally, a common source stage drives the 50 Ω input resistance of the phase noise analyser, Fig.5.6c). This stage is designed to behave as a voltage buffer so it has a unitary voltage gain and it is biased with 13 mA. The resonant load of this stage consists of a transformer used for the impedance matching and for differential to single-ended conversion.

The amplifier has been tested for stability, both with small signal and large signal analysis, and has not shown any unstablility.

Figure 5.8 shows the simulated small signal gain of the amplifier, while Fig.5.9 the amplitude of the voltage at the load (post layout simulation). From Fig. 5.9 we can notice that the amplifier has a bandwidth of around 10 GHz which is not enough for the automotive radar if also process variations are considered. Nevertheless, it is possible to increase the bias current of the oscillator and, therefore, the 4th harmonic to increase the output voltage, and ease the measurements in case of a shift of the amplifier pass-band.

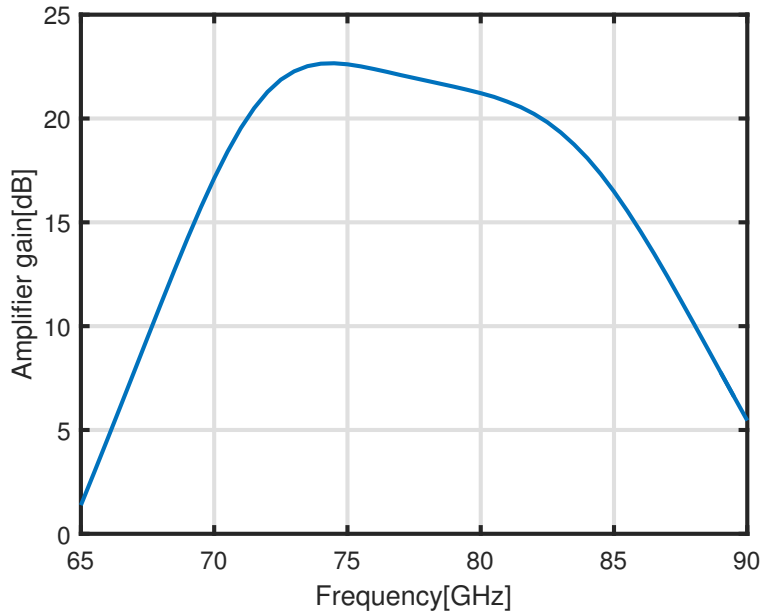


FIGURE 5.8: Voltage gain of the amplifier with load resistance of 50 Ω.

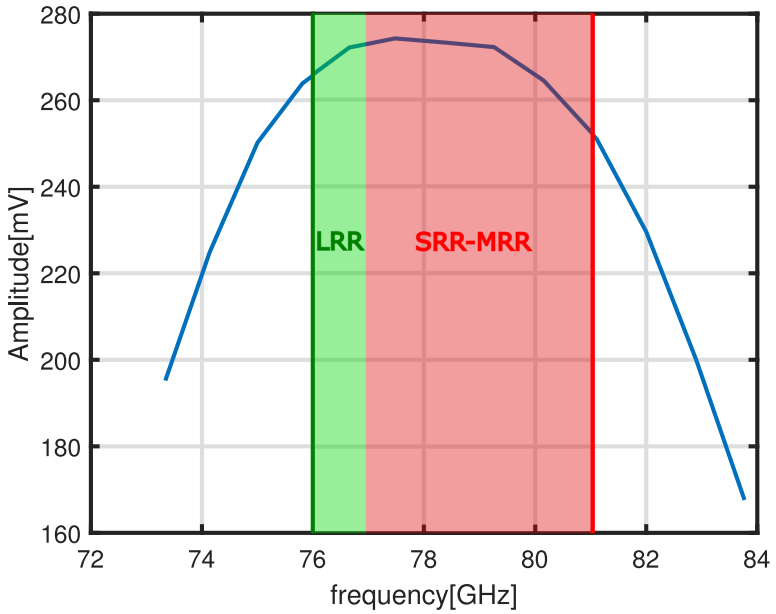


FIGURE 5.9: Output voltage at the 50 Ω resistance, in the band of the long-range radar (LRR) and short/middle range radar (SRR-MRR).

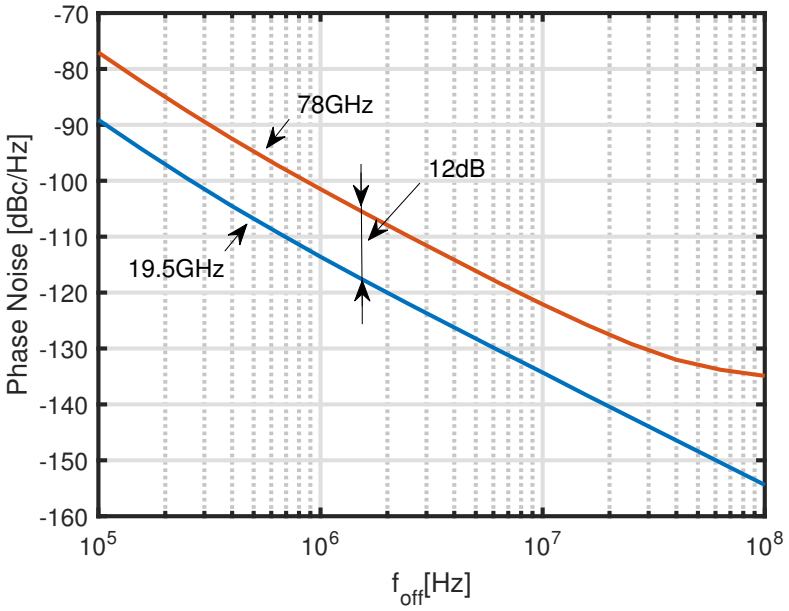


FIGURE 5.10: Simulated phase noise sideband from a 20 GHz and 80 GHz carrier.

Finally, Fig.5.10 shows the phase noise sideband of the oscillator at 20 GHz output and at the amplifier output. As expected, the amplifier introduces a noise floor, that is however negligible at offset frequencies below 40 MHz. The difference between the two curves, as showed by Leeson's formula [69], is $20log(80/20) = 12dB$.

5.3.1 Further Improvements

To increase the bandwidth, one possible solution could be to use of a transformer as a matching network between the amplifier stages [70]. With a coupling factor of 0.5, that is typical for a coplanar transformer, the bandwidth should be large enough to also cover process variation. Moreover, this should solve the problem of interstage connections that introduce parasitic capacitances resulting in a smaller load inductor, thus a smaller voltage gain, for a given resonance frequency, for each stage of the amplifier.

5.4 Conclusions

In this chapter, a way extract the 4^{th} harmonic of a class-C oscillator has been presented. One of the characteristic of a class-C oscillator is the high

harmonic content of the tail generator current. Using a capacitor to series-resonate the common mode path and transformer, the 4^{th} signal can be extracted. Moreover, an amplifier has been designed in order to measure the 4^{th} signal. The total area of the amplifier and the transformer is $0.05\,mm^2$, while power consumption of the amplifier is $40\,mW$.

Chapter 6

Conclusions

In this thesis the focus is on the design of integrated mm-Wave voltage-controlled oscillators (VCO). VCOs are commonly used for a variety of different applications: spanning from communication, to radar, sensing and imaging. In a radar system, the transmitted signal is generated using a phase-locked loop (PLL). One of the components of a PLL is the VCO. The performance of the radar, in terms of distance and angular resolution, are strictly linked to the phase noise produced by the VCO. Therefore, the study of low noise oscillators is of a great interest these days as systems for the autonomous driving employing radar are becoming widespread.

In chapter 1 an overview of radar system was given. It has been discussed about the different waveforms of a radar system and about frequency regulation for automotive application.

In chapter 2, the principle of operation of a frequency modulated continuous wave radar was discussed. The reference radar system is the homodyne transceiver with single antenna.

In chapter 3, a methodology to single out the optimal frequency of operation to minimize phase noise in harmonic integrated oscillators is discussed. It is based on a scalable model of the resonator that takes into account the dependance of the parasitic elements on the inductance value, and on a strategy to scale the tank components as the frequency of operation is changed. A case study, based on an ultra scaled CMOS technology, points out 5 GHz to be such an oscillation frequency for minimum phase noise. Moreover, has been shown that a design for minimum phase noise and a design for best FoM are not always coincident, contrary to common belief and practice. As a matter of fact, the optimization of the tank quality factor may not be the ultimate goal, if phase noise minimization is the priority.

In chapter 4, two millimeter-Wave voltage- controlled oscillators have been presented. Both fabricated in a 28 nm bulk CMOS technology with a supply voltage of 0.9 V. The first one, an hybrid Class-B/D, showed a phase

noise of -98 dBc/Hz at 1 MHz offset frequency from a carrier of 20 GHz with a power consumption of 15 mW. In this design is noticeable the presence of a large flicker noise upconversion. Simulations pointed out that this contribution is mainly due to the cross-couple pair and the tail generator transistors. An analysis, carried out using verilog-A model for the transistor, showed that, when long channel transistor are used, the Class-C operation is able to prevent the upconversion of flicker noise from the cross-coupled pair transistors. This analysis also showed that short channel effect are the main reason why, in practice, when AMPM is not the dominant source of noise, flicker noise still appears in the phase noise sideband. For this reason, despite the short channel effect, a Class-C oscillator has been designed. Due to its intrinsic property of preventing the upconversion of flicker noise from cross-coupled pair, Class-C oscillator is a robust and wideband alternatives to Class-B topology as it doesn't require tuning of the common mode impedance. *Design A* achieves a phase noise of -111.5 dBc/Hz at 1 MHz offset and -85 dBc/Hz at 100 kHz from the 19.5 GHz carrier, drawing 22.3 mA from the supply voltage; while for the *Design B*, the phase noise is -112 dBc/Hz and -86 dBc/Hz at 1 MHz and 100 kHz respectively with 23 mA of I_{Core}. The comparison with the other state-of-the art shows that, despite the short channel effect, the performance of the Class-C, also taking in account the different supply voltages and oscillation frequencies, compares very well with other topologies. We conclude that Class-C oscillator is a valid alternative to other topologies that employ common-mode resonance.

Finally, in chapter 5, a way extract the 4^{th} harmonic of a class-C oscillator has been presented. Moreover, an amplifier has been designed in order to measure the 4^{th} signal. The total area of the amplifier and the transformer is $0.05\,\text{mm}^2$, while power consumption of the amplifier is 40 mW.

Appendix A

VerilogA MOS model

Below is the code used in the chapter for the behavioural simulation of the class-B and class-C oscillators. This code implements the MOSFET equations, long channel model or short channel, found in [44].

By selecting the variable "mosmodel"=0, the long channel equations are used. Instead, with "mosmodel"=1 short channel equations are used.

```
‘include "constants.vams"
‘include "disciplines.vams"

module nMosmodel(G,D,S);
inout D,S;
input G;
electrical G,D,S;

parameter real vt=0.27, kf=0, beta = 200E-3, theta = 0;
parameter integer  mosmod=0;
real vod,vds,vgs,vdssat, ids, flag;
real gm, kn;

    analog begin

  flag = V(D) > V(S) ? 1 : -1;
  vgs = flag==1? V(G,S) : V(G, D);
  vds = flag==1? V(D,S) : V(S,D);

  if(mosmod == 0) //long channel model
    begin
      vod = vgs-vt > 0 ? vgs-vt : 0;
      vdssat = vod;
```

```
      ids =  vod > 0 ? (vds > vdssat ? ...
           ... 0.5*beta*vod*vod : beta*(vod-vds/2)*vds) : 0;
      gm = beta*vod;

    end

  else       //short channel model
    begin
      vod = vgs-vt > 0 ? vgs-vt : 0;
      vdssat = (sqrt(1+2*vod*theta)-1)/theta;
      ids =  vod > 0 ? (vds > vdssat ?...
        ... 0.5*beta*vdssat*vdssat : beta*(vod-vds/2)*vds/(1+ vds*th

    end


  I(D) <+ flag*(ids  + flicker_noise(kf*pow(abs(ids),1),1));
  I(S) <+ -I(D);

   end

endmodule
```

Appendix B

Inductance Lumped Model

The parameters of an inductor that are of interest in the design of an integrated circuit are: the inductance value (L), the quality factor (Q_L)and the self-resonance frequency (f_{srf}). These parameters depend on the geometry of the inductor and also on the technology. To obtain these values, a solution is to use an electromagnetic filed simulator to get the S-parameters. Circuit simulators allow to simulate, in the frequency domain, schematics containing elements described by S-parameters. On the other hand, since S-parameters describe a component in the frequency domain, simulations in the time domain are often critical and may not converge. For this reason, a lumped model of the inductor is often employed.

The most common lumped-element equivalent circuit for spiral inductors is the π model, showed in Fig.B.1, which was introduced first in [71].

The model includes the total inductance (L_s), the series resistance of the inductor metal (R_s), the fringing capacitance between the inductor turns (C_p), the shunt capacitance of the oxide layer ($C_{ox1,2}$), the shunt capacitance of the substrate ($C_{sub1,2}$) and the shunt resistance to model the ohmic losses in the substrate ($R_{sub1,2}$). Every component in the topology has a physical meaning, therefore, the values of the lumped-elements can be calculated from the geometry and material constants of the inductor [34, 72]. However, accurate process parameters are hard to obtain and the performance of fabricated inductors may differ significantly from the predicted values.

A different approach use the S-parameters from measurements or electromagnetic simulations. A fully analytic extraction methodology ensures that the values of the equivalent circuit elements are physical. In this way, no process parameters have to be assumed during extraction and thus, the influence of process variations on the circuit performance is diminished. For the π model a methodology to extract the value of the model can be found in [73].

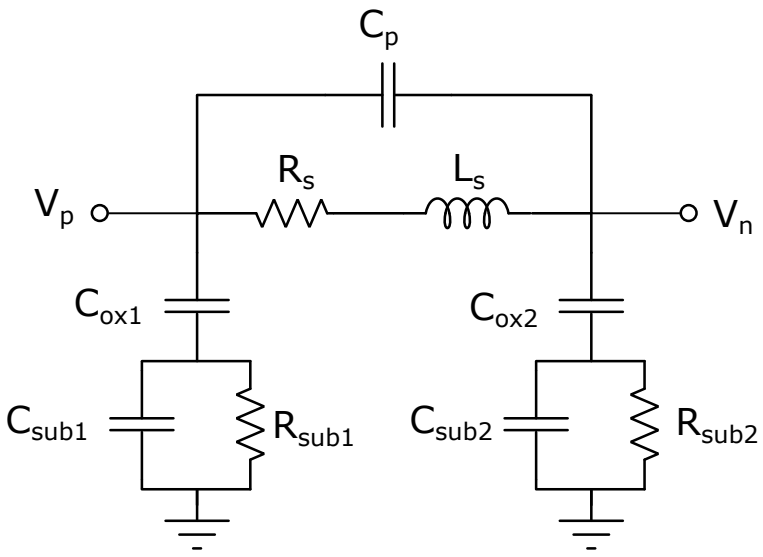


FIGURE B.1: π model of the inductor.

The π model usually provides a good description of integrated inductor at low frequency, below f_{srf}. At mm-Wave operating frequency other effects, for example, skin effect, current crowding effect as well as eddy currents in the substrates, need to be considered. Moreover, the distributed nature of an inductor at high frequency is insufficiently modelled using the simple π model.

For these reasons, a more elaborate double-π structure was introduced in [74], Fig.B.2 .

In this model, a ladder network is introduced in the series branch of the circuit. This ladder network captures the frequency dependent behavior of the inductance and the series resistance due to the non-uniform current distribution in the conductor. At low frequency, the current is uniformly distributed inside the spiral conductor. Hence, it is represented by L_s and R_s in series. As the frequency increases, the current is pushed towards the surface of the conductor. The surface layer resistance and inductance is represented by the L_f-R_f branch, which is connected in parallel to the series resistance R_s. This way, the different current density layers are modelled. The distributed characteristics of an on-chip spiral inductor are captured by expanding the model with a further substrate network, consisting of C_{ox3},C_{sub3} and R_{sub3}, in the middle. The capacitance C_p represents the total inter-winding capacitance of the inductor. The substrate coupled network made of the inductor and the resistor models the eddy currents, taking care of the losses generated in both the horizontal and vertical directions [75]. The center tap is modelled as series of L_{CT} and R_{CT}, in this way it is also possible to model the

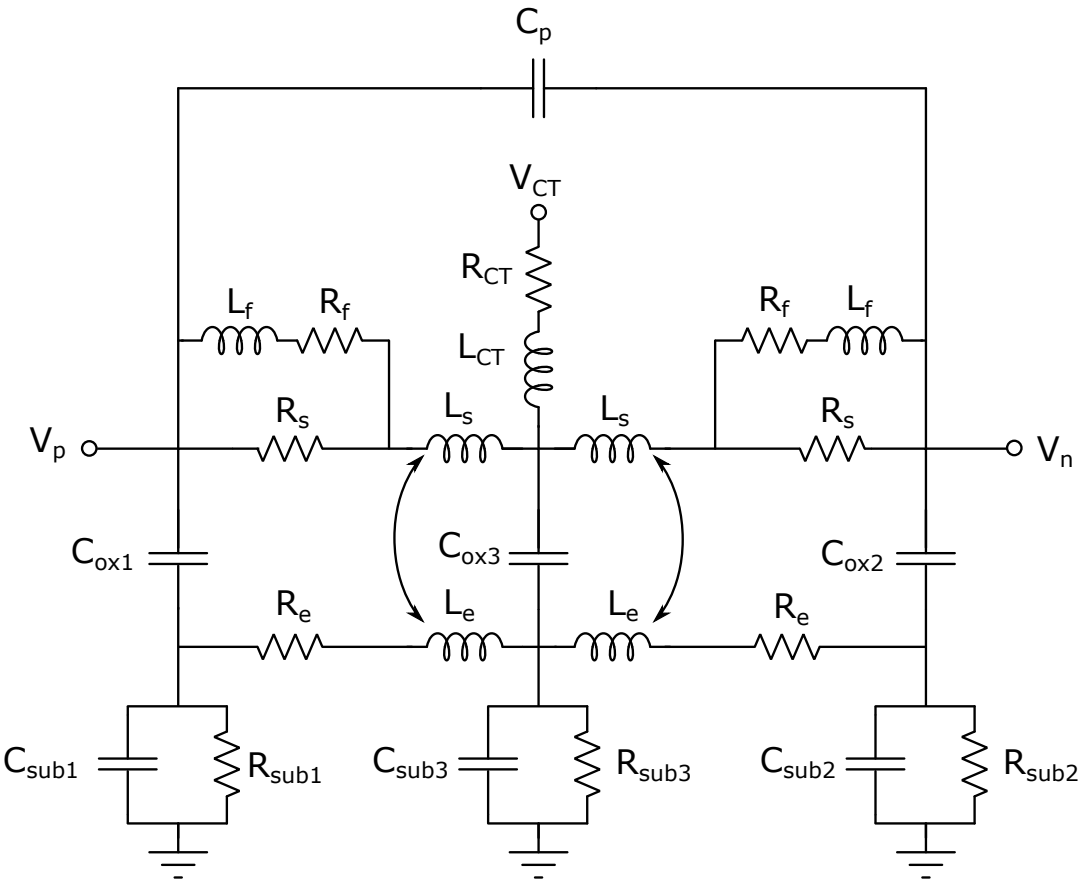


FIGURE B.2: Double π model of the inductor.

common-mode behaviour.

The downside of the double-π model is the increased complexity in extracting the values of the model parameters from the EM simulation data. The extraction can be done by fitting using the Agilent Advanced Design System (ADS) optimizer tool.

Figure 4.3 in Chapter 4 confirms the validity of the double-π model for a large set of frequency.

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