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THESIS TITLE

SOLID STATE TRANSFORMER

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CHAPTER 1

Introduction

During the last decades, the increase of the environment pollution and of the fossil fuel cost has promoted the diffusion of the distributed energy sources (DES), in particular of the smaller power plants that use renewable energy resources. The growth scenario of the energy sources exploitation is shown in Fig. 1.1. The connection of a large number of DES to the grid has led to deep changes in the electric distribution system. For example, the power flow that in the past was only unidirectional, from the conventional power station to the consumers, nowadays is becoming bidirectional. The consumer can become active actor and inject power into the electric grid. This leads to the necessity to change drastically the management of the electric system for fully exploit the electric power producible by the renewable energy resources. Then, the future electric systems, also called smart grids, must be more flexible and controllable; to realize this, innovative equipment with new functionalities are required. The power electronics, coupled with other new technologies, is becoming more and more important to realize equipment able to satisfy the requests of the electric systems. The power electronic devices, in particular the power converters, have a wide application range in both distribution and transmission power systems; for example, in high voltage DC transmission systems, in flexible AC transmission systems devices, such as static VAR compensator, static synchronous compensator, unified power flow controller, and in renewable energy systems, such as solar and wind plants. One of the solution of major interest, also known as power electronic transformer or intelligent universal transformer, is the Solid State Transformer (SST).

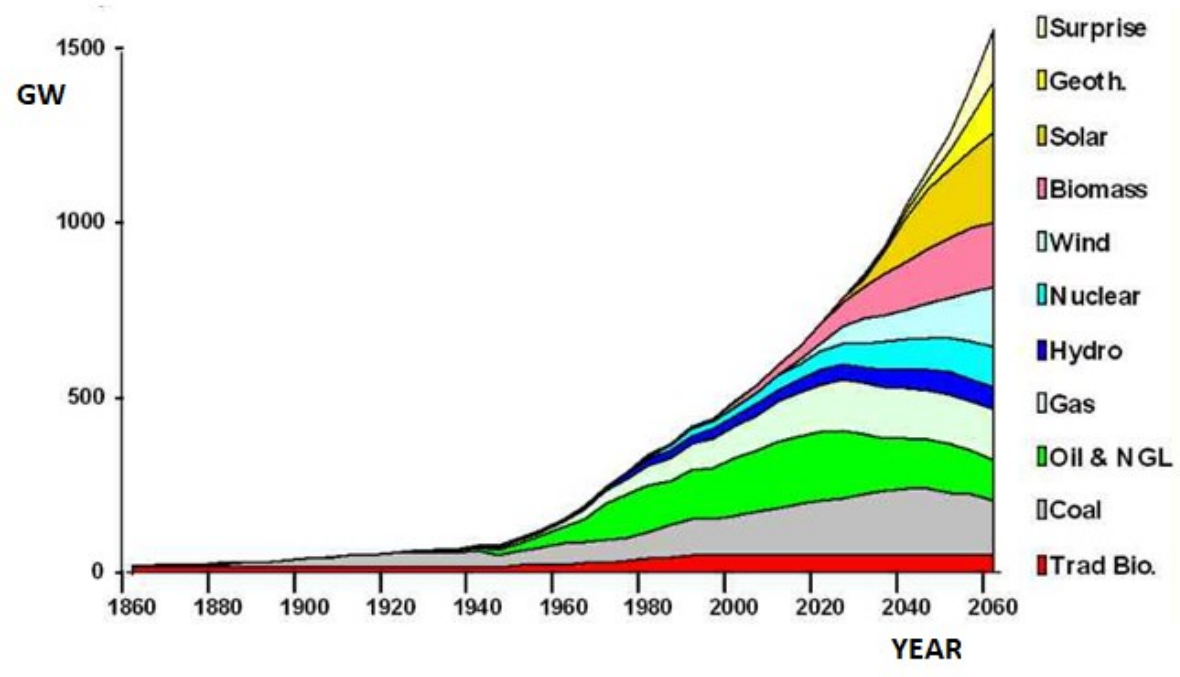


Fig. 1.1 Growth scenario of the energy sources exploitation

1.1 SST concept

The SST is an emerging solution that can advantageously substitute the conventional transformer, thanks to its capabilities. Furthermore, it is a multi-functional equipment that offers:

- conditioning of the power flow, whether of DC or AC form;

- reduced size and weight thanks to the high frequency transformer;

- good voltage regulating capabilities;

- no diffusion of voltage swell or sag thanks to the DC link (if any);

- power factor correction;

- fast fault detection and protection;

- capability to maintain the output feed for a time (hold up time) thanks to the DC link capacitors;

Moreover, it offers the conventional transformer properties:

- galvanic isolation between input and output;

- step up/down of the input voltage;

The SST capabilities make this technology an important solution to solve the current and future issues of the grid [1]-[4]. The reduced weight and size allow getting high performances in the traction systems. The bidirectional power flow capabilities allow the connection and management of renewable energy sources (RES) with the grid and different loads, connected to AC side or, if present, to DC link.

In addiction to the advantages above described, in the recent years the costs of the power electronics components is decreased and more reliable and efficient devices are available. Furthermore, new devices suitable for high power and high operating frequency have been developed. The many capabilities, the feasible cost of the components and the mature technology lead to consider the SST one of the solutions of most interest to satisfy the request of the future electric grid and the new applications.

The SST consists of two or more static converters coupled with a transformer that operates at frequencies considerably higher than that of the grid. A representation of the SST concept is shown in Fig.1.2.

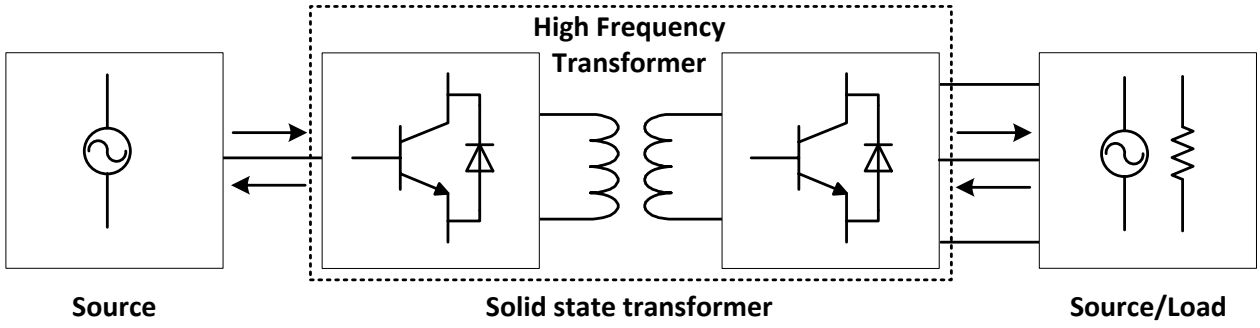


Fig. 1.2 SST concept.

1.2 Research Objectives

The research objectives of this PhD thesis are:

- Study and analysis of the thematic related to the SST technology, investigation of the architectures and topologies available highlighting the advantages and disadvantages of each one.

- Comparison of the architectures available as a function of the application of interest.

- Evaluation of several conversion stages suitable for the different architectures presented and their detailed analysis, considering both steady-state and dynamic behaviour.

- Investigation of the soft-switching capabilities of the conversion stages treated.

- Comparison of the conversion stages studied in term of design characteristics and capabilities for different applications.

- Validation of the studies and analysis done through simulations realized with the software PSIM and tests on the prototype realized at reduced scale.

1.3 Thesis overview

The thesis is organised as follow:

Chapter 1 introduces the motivations for the development of the research activity. It highlights the need of new studies in new equipment necessary to satisfy the requests of the future electric grid. It also introduces the SST concept and presents the research objectives of the thesis. It is concluded with an overview of the chapters of the thesis.

Chapter 2 presents an overview of the SST architectures. Strengths and weaknesses of each one are discussed. Several topologies of converters are described for the different conversion stages composing the SST. A comparison of the reviewed architecture is performed. A short recall of the high frequency transformer characteristics has been done. At the end of the chapter, an investigation of the SST applications is presented; in particular, two applications of interest are treated in detail.

Chapter 3 presents and analyses the Single Active Bridge converter (SAB), a two port DC-DC conversion stage used in a three stage SST. A thorough analysis of the steady-state operation and the dynamic model is reported. Its characteristics, needed for the project design, are calculated. Further, its soft-switching capabilities are investigated to improve the converter efficiency. A simulation project is realized to validate the performed mathematical analysis done. At the end of the chapter, the description of experimental setup, realized at reduced power, and the obtained results are reported.

Chapter 4 presents a different topology of a two port DC-DC converter, the Dual Active Bridge (DAB). As for the SAB, the steady-state operation and the dynamic model are studied. Its design characteristic and soft-switching capabilities are calculated and investigated. A comparative analysis between the SAB and DAB converter is discussed. A simulation project is realized to validate the analytical analysis done. At the end of the chapter, the description of experimental setup, realized at reduced power, and the obtained results are reported.

Chapter 5 presents an isolated three-port DC-DC converter (TPC). Its analysis is carried out starting from the studies done for the DAB and, in particular, for the SAB converter. The TPC power capabilities and control characteristics are investigated for different operation modes and working situations. More precisely, the chapter is focused on two Discontinuous Conduction Modes (DCMs) operations of the TPC, namely: i) full DCM (FDCM), with all the ports operating in DCM, and ii) mixed discontinuous conduction mode (MDCM), with one port operating in DCM and the other ports operating in Continuous Conduction Mode (CCM). Moreover, two working situations are analyzed, i) two ports deliver power to the third one, and ii) one port delivers power to the other two. At the end of the chapter, the analytical results are validated through simulation and experimental tests.

Chapter 6 presents a review of several AC-DC conversion stages suitable for the use in a SST. In particular the study is focused on several boost Power Factor Correction (PFC) rectifier topologies, illustrating for each of them the single-phase version and the three-phase counterpart, with an analysis of their operation and features. Among the topologies reviewed, a boost classical PFC rectifier has been analyzed and realized for the AC-DC conversion stage that is connected to the grid.

Chapter 7 summarizes the performed activities and concludes the thesis. Furthermore, it presents a proposal for the future activities on the SST.

CHAPTER 2

State of art

Many architectures and topologies with different characteristics and capabilities have been studied in the past and are still under development [5], [6]. The first studies on the SST, which was initially called electronic transformer, date back to 1970. Among the first topologies studied, the SSTs with a direct AC-AC conversion stage have attracted more interest, but, due to the hardware limitation, in particular because of the immature semiconductor technologies, these topologies did not provide an advantageous solution during that time. The SST basic schematic is shown in Fig. 2.1.

In the last decades, new SST architectures, composed of more stages, have been proposed, and in particular, many studies have been done on the DC-DC stage, which comprises the high frequency transformer [7], [8]. Furthermore, large improvements have been made in the construction of the high frequency transformer. In particular, new materials employed to build the magnetic core and new methods of manufacturing the windings have been developed. With the development of new high voltage semiconductor devices based on silicon carbide (SiC), SST technology has achieved higher performance and become competitive with conventional systems [9]. In addition, due to the increase of the voltage and current requirements, advanced multilevel topologies have been introduced in recent years. Among the most important recent projects, there are the MEGACube and MEGALink projects of the ETH Zurich, the FREEDM project (Future Renewable Electric Energy Delivery and Management), the ABB projects that develop SST topologies for traction applications, the UNIFLEX (Universal and Flexible Power Management) which develops SST for smart grid applications, and the projects of GE (General Electric Company) that proposes topologies suitable for substation applications [10]-[15].

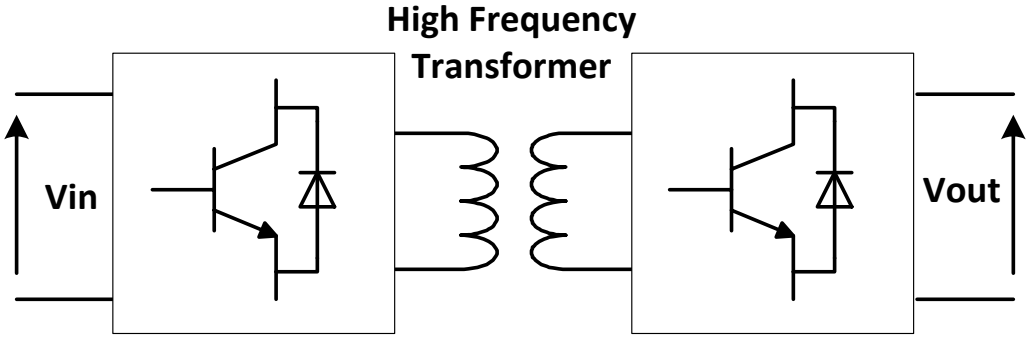


Fig.2.1 Solid State Transformer schematic.

2.1 Overview of SST architectures

There are many SST architectures, having different design characteristics, circuit complexity and performances. These architectures may be classified in four groups: a) single stage without a DC link,

b) two stages with a low voltage DC link (LV DC link), c) two stages with a medium voltage DC link (MV DC link) and, d) three stages with a low and medium voltage DC links. Fig. 2.2 shows the four architectures.

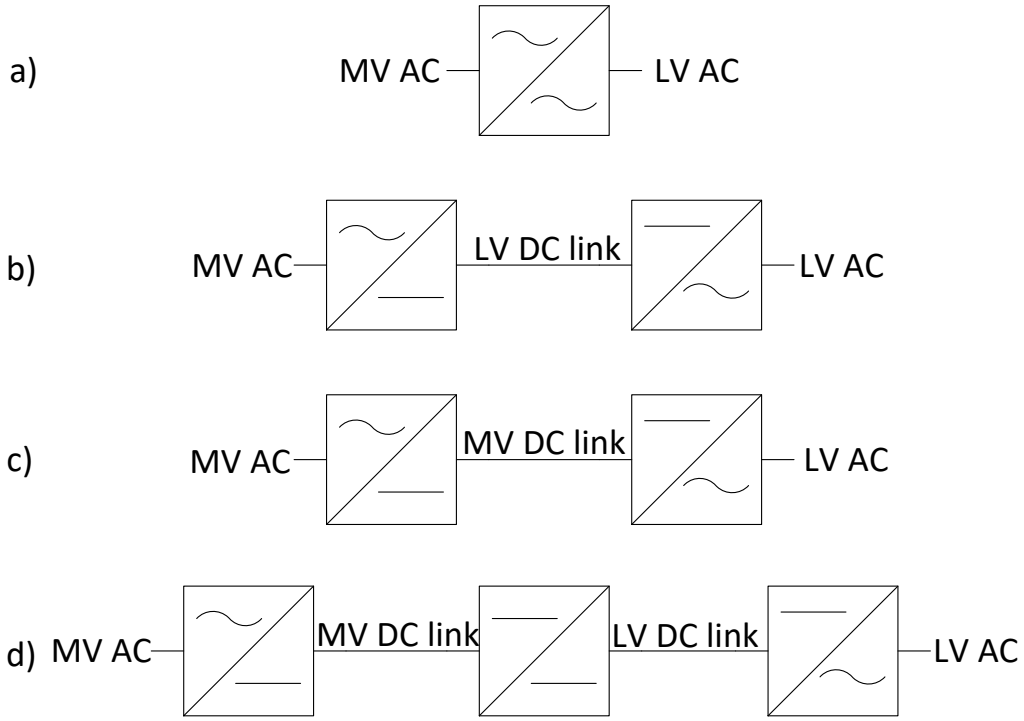


Fig.2.2 Schemes of SST architectures: a) single stage, b) two stages with LV DC link, c) two stages with MV DC link, d) three stages with two DC link.

Considering the current applications, the SSTs are often connected at medium voltage grid, therefore high voltage power switches are required. Adopting new high voltage power switches in conventional architectures has the advantage of using topologies and control methods widely developed and known. The main disadvantages are the cost of the new generation components and the issues due to the selection and sizing of the high voltage filters.

Another solution is based on the multilevel converters, which allow using of the conventional semiconductors technology [16]-[18]. The advantages of multilevel converters are higher power rating, lower common mode voltages, higher efficiency, smaller input-output filter and reduction of harmonic content. On the other hand, the circuit complexity and number of power switches increase. In addition, due to the limitation of power switches and magnetic components, more SSTs modules are connected together, forming a Modular Multilevel Converter (MMC). The three possible connections, as shown in Fig.2.3, are input series output parallel (ISOP), input parallel output parallel (IPOP) and input series output series (ISOS). Modular implementation of two stages and three stages SST are shown in Fig.2.4.

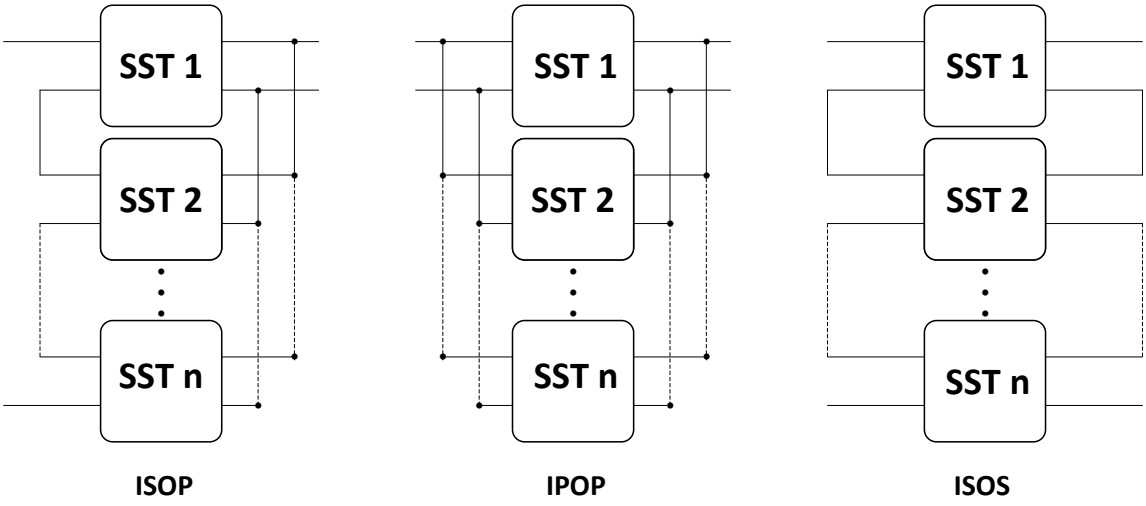


Fig.2.3 Modular Multilevel Converter connections.

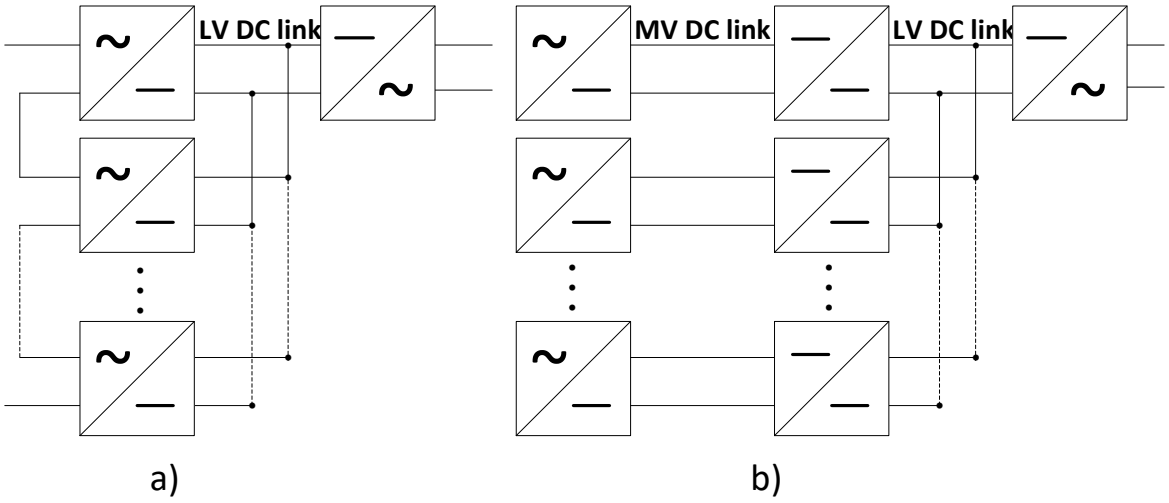


Fig.2.4 Modular implementation of a) two stages and b) three stages SST.

2.1.1 Single stage

The single stage architecture is composed of a direct AC-AC converter with a high frequency transformer that guarantees the isolation between the medium and low voltage grid. Fig. 2.5 shows a single stage AC-AC full bridge converter [19]-[23]. Due to the input and output alternating voltages, the switches must be able to block the voltage in both polarities. Additionally, the switches must be chosen to allow a bidirectional power flow. Thus, four quadrant power switches are needed, where each switch cell is composed of two IGBT-diode modules connected in antiseries. The first bridge converts the low frequency input voltage into high frequency. After that the second bridge reconverts the high frequency voltage into low frequency. To obtain correct operation of the SST, the two bridges must be synchronized. Each switch cell receives a single command that turn on alternately one of the two IGBTs, internal to the cell, when the input voltage is positive or negative. The voltage waveform at output of the first bridge, has the same amplitude of the input voltage and only the frequency is changed. These operations generate harmonics that require insertion of filters at input and output of

converter. The method most used for the control of the two bridges is the phase shift modulation. The advantages of this architecture are the simple control, the reduced number of active and passive components, the low cost and the light weight. The major drawback is the lack of the DC link that prevents the implementation of several functionalities such as, for example, the control of the reactive power. Another disadvantage is that, unlike the configuration with DC link, disturbances on one side, such as voltage sag or harmonics, could affect the other side. Single stage SST is not suitable for high voltage operation where soft switching capabilities can not be guaranteed so that losses cannot be reduced leading to lower efficiency and difficulties in thermal dissipation of switches. The multilevel topologies could be a solution but currently is not easily applicable in high voltage side.

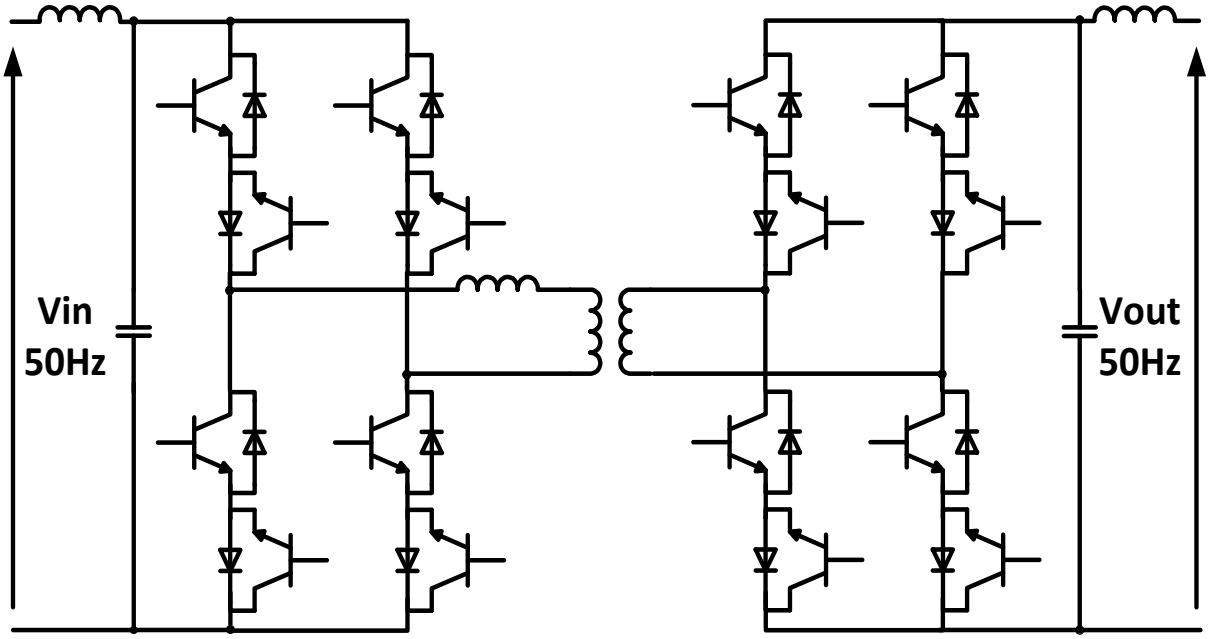


Fig.2.5 Single stage AC-AC full bridge converter.

2.1.2 Two stage with LV DC link

This architecture is composed of two conversion stages, an AC-DC conversion stage with a high frequency transformer and a DC-AC conversion stage, as shown in Fig.2.6 [24], [25]. Unlike the single stage architecture, the two stages SST has a low voltage DC link, which allows many functionalities. Like for the single stage architecture, the switch cells on the medium voltage side must be composed of two IGBT-diode modules to allow the bidirectional power flow and to sustain the bipolar voltage. At low voltage side the use of a single IGBT-diode module is sufficient. For the DC-AC conversion stage a traditional full bridge converter is used. The first-bridge of the AC-DC stage is controlled, like the bridge of the single stage SST, using a single command for each switch cell which turns on alternatively the two IGBTs. The second bridge of the AC-DC and the full DC-AC conversion stage are controlled using the Pulse Width Modulation (PWM).

This architecture allows the reactive power compensation and it is suitable, thanks to the DC link at low voltage side, to interfacing with distributed energy sources, such as photovoltaic plants, energy storage systems, wind plants, and DC loads capable of bidirectional power flow. The output voltage regulation is good and, unlike the single stage topology, the input current is adjustable. The disadvantages are the need to use different control algorithms when the power flow goes from

medium to low voltage side or vice versa, a high ripple current in the DC link, and the same issues of the single stage for the high voltage applications at the medium voltage side.

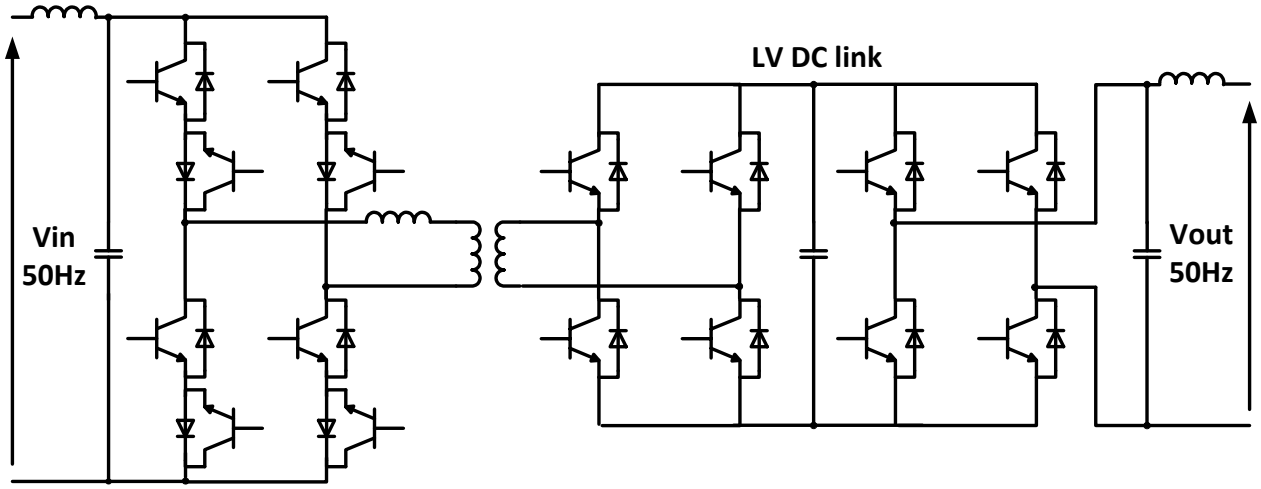


Fig.2.6 Two stage SST with LV DC link.

2.1.3 Two stage with MV DC link

The two stage SST with MV DC link has the same architecture as the last discussed SST with the difference that the DC link is at medium voltage side. Unlike the last architecture, this is not so suitable for integration of the DES. Instead, thanks to MV DC link, it is suitable for applications in the distribution grid.

2.1.4 Three stage

The three stages architecture is the most suitable for a SST [26]-[29]. It is composed of an AC-DC conversion stage, a DC-DC conversion stage with a high frequency transformer, and a DC-AC conversion stage, as shown in Fig. 2.7. The two DC links decouple the medium voltage side from the low voltage side, avoiding the disturbances propagation between the two sides and allowing a better control of the currents and voltages on both the sides. It offers high performance and many capabilities, such as bidirectional power flow, reactive power compensation and sag compensation. Furthermore, thanks to the LV DC link, it is suitable for the integration of distributed energy sources. The AC-DC and DC-AC conversion stages are controlled using the PWM, and the DC-DC conversion stage is controlled using the phase shift modulation. In the next subsections, a review of several topologies used for the three stages architecture is presented.

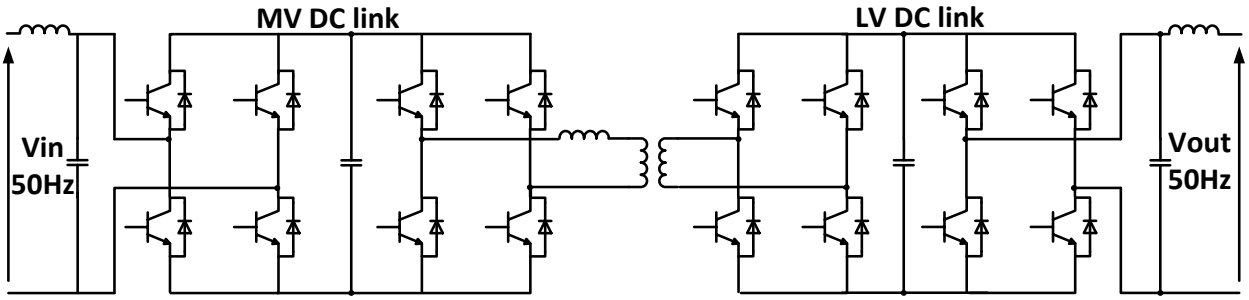


Fig.2.7 Three stage SST.

2.2 Overview of the conversion stages

2.2.1 AC-DC conversion stage

The AC-DC conversion stage connects the MV AC side with the MV DC link. To allow the use of this topology in medium voltage applications the multilevel technology is adopted. Among the available multilevel topologies, the most suitable for the SST applications are:

- cascade H-bridge;
- neutral point clamped(NPC) or diode-clamped;
- flying capacitor converter.

The cascade H-bridge converter is the most used topologie. It is composed of many single phase H-bridge converters, as shown in Fig. 2.8. This topology allows a wide rating of output voltage and power because the output voltages of each single H-bridge can be combined to satisfy the requirements of the application. Furthermore, the topology allows modularized layout and easy packaging because each level has the same structure. The DC buses can be connected in parallel or series to form the modular converter configurations previously presented. The disadvantages are that the maximum DC link voltage of each module is limited by the voltage rating of its components and each module requires an isolated voltage source.

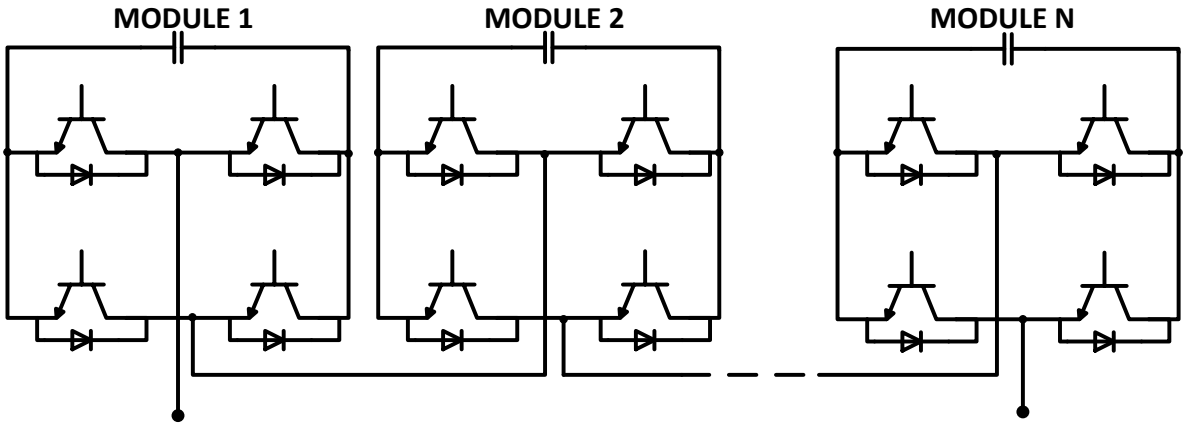
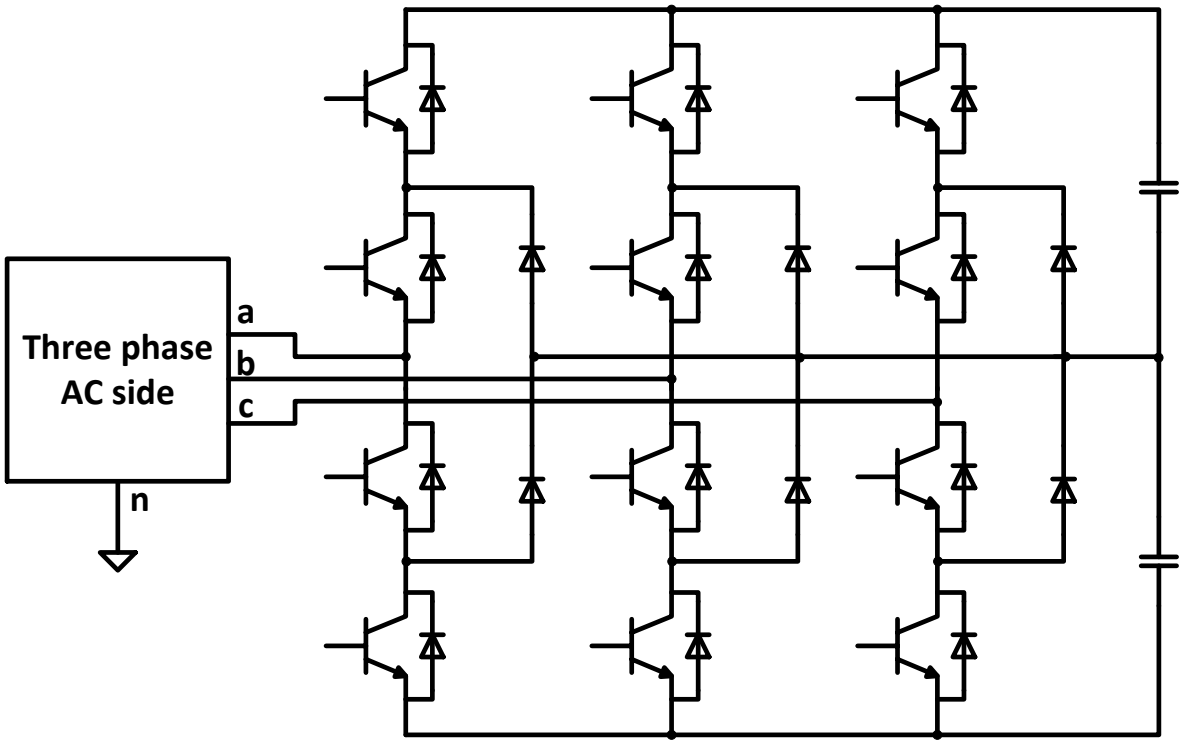
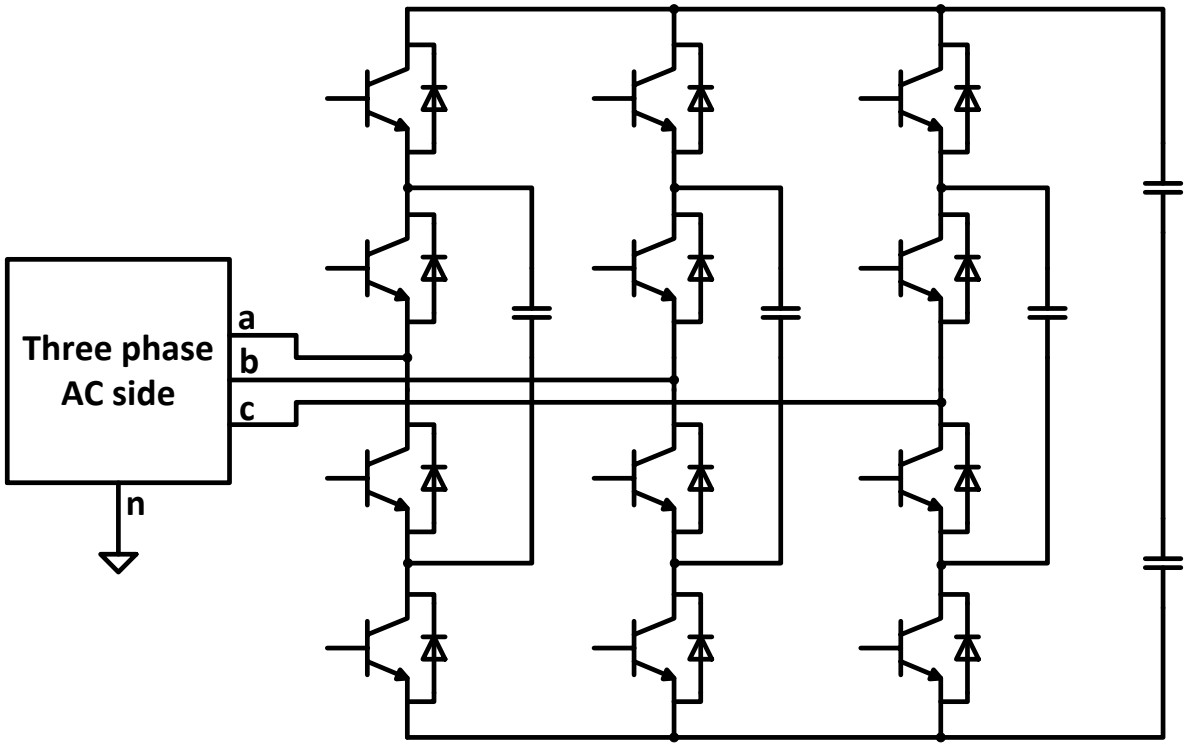


Fig.2.8 Cascade H-bridge AC-DC converter.



a)



b)

Fig.2.9 a) Neutral Point Clamped and b) flying capacitor AC-DC converters.

The neutral point clamped converter, also known as diode clamped converter, is shown in Fig.2.9a). It is composed of many two-level voltage source inverters that are connected together through the clamping diodes forming the neutral point that splits into half the DC link voltage. Thanks

to the neutral point the power switches forming the converter have to sustain only half of the DC link voltage. The advantages of this topology are that all the phases share the same DC bus, thus reducing the capacitor requirements, the pre-charge of the capacitors is simple and the reactive power flow is controllable. The main disadvantages are:

- the number of clamping diodes increases with the square of the number of voltage levels, so this topology is not suitable for systems with high number of levels.
- the rms current flowing through the switches are different because certain switches conduct for a longer time than other.
- the control of real power flow is difficult due to the overcharge or discharge of the DC link capacitors which do not allow an accurate control.

The structure of the flying capacitor converter is similar to that of the neutral point clamped with the difference that the diodes are replaces by capacitors. The advantages are that the reactive power is controllable and, thanks to the large number of capacitors, the converter maintains its operability during short outages and deep voltage sags. The disadvantages are that the large number of capacitors leads to having a bulky, expensive and difficult to package system, the pre-charging of the capacitors is complex and the efficiency, compared with other topologies, is poor. A three phase flying capacitor converter is shown in Fig. 2.9 b).

2.2.2 DC-DC conversion stage

The DC-DC conversion stage is the core of the SST. This stage is composed of three parts:

- a DC-AC converter;
- a high frequency transformer;
- an AC-DC converter.

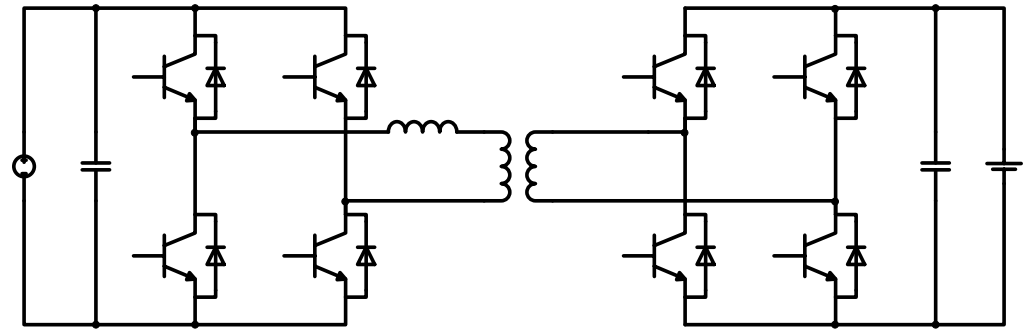
Many topologies, with different circuit complexity, operating characteristics and performance can be used to set up this stage. The more suitable for the SST technology are the dual active bridge converter, the bidirectional isolated current doubler converter and the LLC resonant converter.

The dual active bridge converter consists of two H-bridges with a high frequency transformer in the middle, as shown in Fig.2.10 a). The leakage inductance of the transformer is used as energy storage device, needed to control the current. External inductance may be connected in series to the transformer if its leakage inductance is not sufficient. This topology offers high performance and good soft switching properties but suffers of large harmonic content in the input and output current that imposes the use of big capacitors, in particular on the secondary side, to contain the voltage oscillations of the DC links.

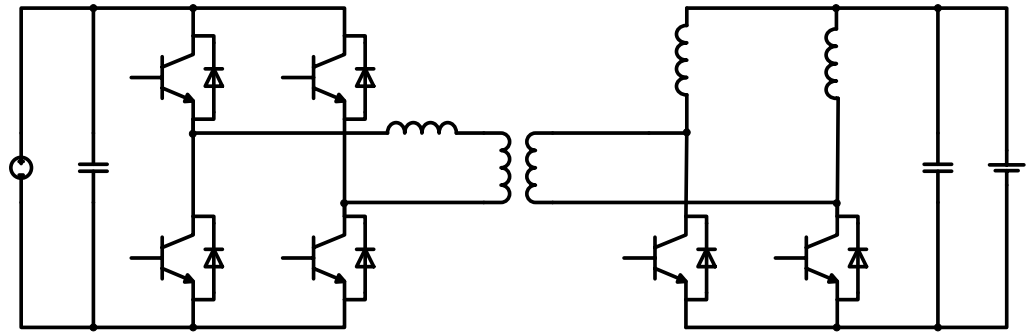
The bidirectional isolated current doubler converter is similar to the dual active bridge with the difference that the two upper switches of the secondary bridge are replaced by inductors, as shown in Fig.2.10 b). This topology achieves lower conduction losses and higher controllability of current. Its main disadvantages are that the transformer must be sized with larger power rating. It also requires two large inductors for the secondary side.

Like the bidirectional isolated current doubler, also the LLC resonant converter is derived from dual active bridge topology; one or more capacitances are connected in series or in parallel to the leakage inductances of the transformer, to form a resonant circuit, as shown in Fig.2.10 c). Because of the resonance, the current in AC link is quasi sinusoidal and switches commutate with lower losses. This allows reaching higher power density and higher operating frequency compared with dual active

bridge topology; moreover, the additional capacitor filters the DC content of the primary current thus avoiding the saturation of the core of the transformer. The disadvantages of LLC resonant converter are the requirement of large inductor and capacitance and the high sensitivity to the variation of H-bridge switching frequency. In particular, it could become uncontrollable without load.



a)



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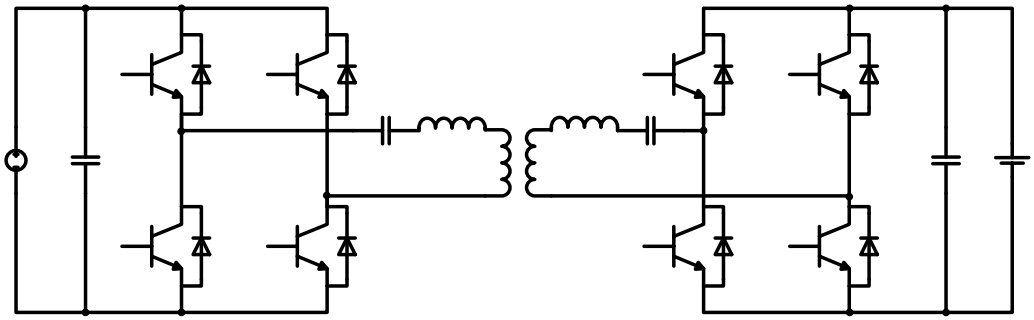


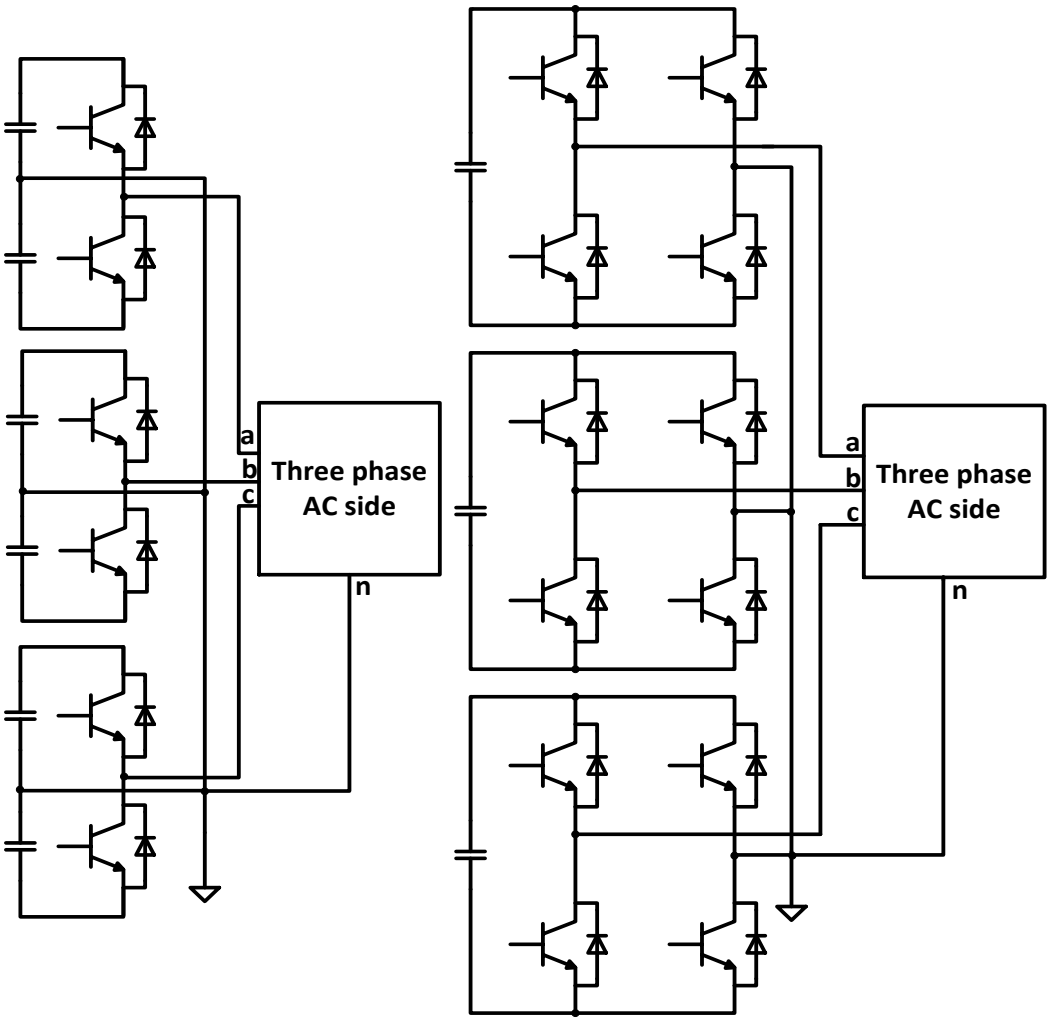
c)

Fig.2.10 Schemes of DC-DC converters: a) dual active bridge, b) bidirectional isolated current doubler, and c) LLC resonant converter.

2.2.3 DC-AC conversion stage

The last stage of the SST performs a DC-AC conversion of the output side DC link voltage, sustained by the DC-DC converter, in AC output voltage. Unlike the conversion performed at the AC-DC stage, in the DC-AC conversion only low voltage is involved, irrespectively on the grid operating voltage, and therefore the use of multilevel converter is not necessary. The topologies more used in this stage are half bridge and full bridge inverters. If required, the half bridge or full bridge inverters may be connect in parallel to form multi-phase converters as shown in Fig.2.11. In the case

of topologies of Fig. 2.11 a) and b), the DC buses can be connected in parallel or, in the case of a modular DC-DC conversion stage, the singular half bridge or full bridge can be connected to different DC-DC converters, which provide an isolated DC bus thanks to the high frequency transformer.



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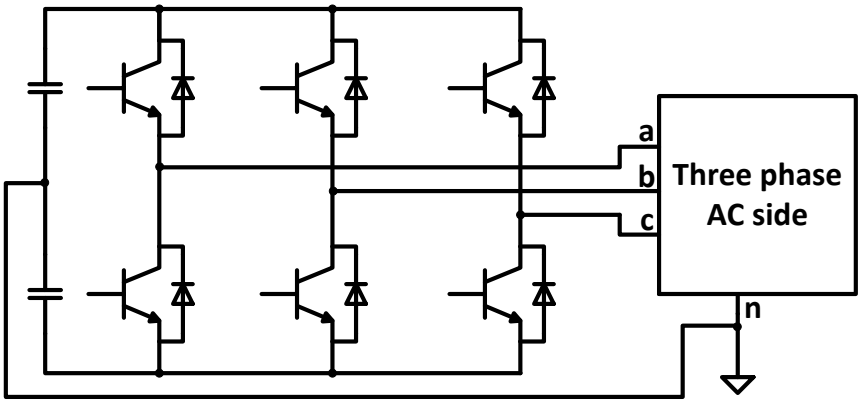


c)

Fig. 2.11. Schemes of DC-AC converters: a) single phase half bridge, b) single phase full bridge, c) three phase converter.

2.3 SST architectures comparison

Let us analyse and compare the architectures reviewed in the previous sections. The comparison is done evaluating the available functionalities, the limitations and possible applications.

The single stage SST allows the bidirectional power flow but, due to the lack of the DC link, does not allow several functionalities, such as the reactive power compensation. The lower number of active semiconductor components allows to having low losses and high efficiency. Then this architecture is suitable in the application which do not requires particular functionalities but high efficiency and simple schematic.

The two stages SST has intermediate characteristics, compared to the single and three stage SSTs. Thanks to the DC link at MV or LV, it allows many functionalities, such as the reactive power compensation, input current regulation, overvoltage protection, limitation of voltage sags and of harmonics propagation and so on. The stages have independent operating frequency. The control becomes more complex than for single stage SST.

The three stages SST allows the same functionalities of the two stages SSTs with better performance in the currents and voltages control. This architecture is the most suitable for integration of renewable energy sources, in particular thanks to the two DC links at different voltage level. A summary of the architectures capabilities is reported in Tab.2.1.

Tab. 2.1. Capabilities provided by SST architectures.

Capability	**Single stage**	**Two stages**	**Three stages**
Bidirectional	Yes	Yes	Yes
Reactive power compensation	No	Yes	Yes
Sag-harmonic limitation	No	Yes	Yes
Independent frequency	No	Yes	Yes
Output voltage regulation	Low	Average	Good
Input current regulation	No	Good	Good
Losses	Low	Average	Average
DER applications	No suitable	Suitable	Suitable
Grid applications	Suitable	Suitable	Suitable

2.4 High frequency transformer

The high frequency transformer is the central component of DC-DC conversion stage [30], [31]. It guarantees the galvanic isolation between the input and output conversion stages. The design of this device is more complex than a normal transformer because it operates at high frequency and, in the case of medium voltage grid, it is connected to high voltage. In particular, the winding configuration and structure influence the efficiency of transformer at high frequency, and for this reason suitable design arrangements must be chosen.

The magnetic materials used in traditional transformers are not suitable to achieve high power and low losses at high frequency because of hysteresis losses and eddy current losses. Hysteresis losses are produced by the reversal magnetization in the transformer core. As shown in Fig. 2.12, in the hysteresis cycle of a ferromagnetic material the energy supplied to the core during the magnetizing phase is not fully returned during the demagnetization phase. At every cycle a quantity of energy, proportional to the area between the two curves, remains stored in the magnetic core.

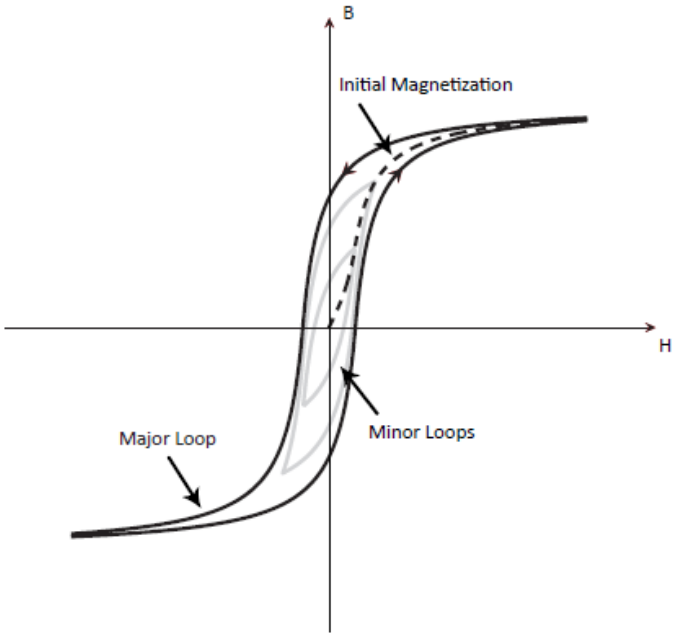


Fig. 2.12. Hysteresis cycles of a ferromagnetic material with different values of H_{max}.

The power lost to magnetize the material is given by (2.1)

$$P_h = K_h f B_M^{\alpha} \tag{2.1}$$

where K_h is a constant that depend from the material used, f is the frequency, B_M is the maximum magnetic flux density and α is the Steinmetz coefficient (equal to 1.6 for B_M<1T and equal to 2 for B_M>1T). The power loss results proportional to the frequency and depends on the magnetic characteristics of the material used for the core.

Eddy current losses are produced by currents circulating in the core, caused by the voltage induced by the variable magnetic flux density. Eddy currents are proportional to the square of the flux density magnitude and frequency. They can be reduced by laminating the core; this technique, however, becomes impracticable at high frequency so that materials with high resistivity must be selected for the core.

Power lost because of eddy currents is given by (2.2)

$$P_f = K_f f^2 B_M^2 \quad (2.2)$$

where K_f is a constant that depend from the material used.

Several magnetic materials are suitable for high power transformers, such as silicon steel, ferrite, amorphous and nanocrystalline materials. Selection of the best fitted material for the given application must take into account its characteristics of saturation flux density, Curie temperature and maximum operative temperature. Tab. 2.2 shows a comparison between different magnetic materials. Among the more diffuse and interesting materials there are:

- **Silicon steel:** it has high saturation flux density and permeability but the losses, at high operating frequency, are high. Therefore, it is not so much suitable for high frequency application. An advanced silicon steel material allows lower losses. The ferrite has moderate losses and its costs is low; its major disadvantage is the low saturation flux density.

- **Fe-amorphous alloy**: it has better characteristics than the high performance ferrite. The losses are similar but the saturation flux density is three times higher. Its value reaches 1.56 T. Another alternative is the Co-amorphous alloys that offer lower losses compared to the materials above considered but a limited saturation flux density.

- **Nanocristalline alloys:** they are the best materials to use in the SST. The saturation flux density is higher than Co-amorphous alloys and ferrite, and the losses are lower than silicon steel and ferrite. Therefore, they offer high power density and efficiency performances. The two major disadvantages of this material are high cost, due to the new technology, and the limited selection of available core shapes.

Tab.2.2 Comparison of magnetic materials.

Material	Loss [W/kg] (20 kHz, 0.2 T)	Saturation B_{sat} [mT]	Permeability [H/m] (50 Hz)	Max working Temp. [°C]
Grain oriented silicon Steel	>1000	2000	2k-35k	120
Advanced silicon steel	40	1300	16k	130
High performance ferrite	17	500	1.5k-15k	100/120
Fe-amorphous alloy	18	1560	6.5k-8k	150
Co-amorphous alloy a	5	550	100k-150k	90/120
Co-amorphous alloy b	5.5	820	2k-4.5k	120
Co-amorphous alloy c	6.5	1000	1k-2.5k	120
Nanocrystalline alloys I	4	1230	20k-200k	120/180
Nanocrystalline alloys II	4.5	1350	20k-200k	120/180
Nanocrystalline alloys III	8	1450	100k	120/180

As for the material selection, the choice of transformer structure is important. It influences the power density and efficiency. Mainly there are two types of winding structures: solenoidal and coaxial. The solenoidal is the most used thanks to its easier design and manufacturing and lower costs. To satisfy the high power and high operating frequency required by the SST applications, for both the structures a multiple cores set up is used.

Two effects must be considered: the skin effect and the proximity effect. The skin effect is the tendency of an alternating electric current to distribute within a conductor such that the current density is largest near the surface of the conductor, and decreases with greater depths in the conductor. The electric current flows mainly at the "skin" of the conductor, between the outer surface and a level called the skin depth. The skin effect causes the effective resistance of the conductor to increase at higher frequencies where the skin depth is smaller, thus reducing the effective cross-section of the conductor. At 60 Hz in copper, the skin depth is about 8.5 mm. At high frequencies the skin depth becomes much smaller. The current density J trend is given by

$$J = J_s e^{-d/\delta} \tag{2.3}$$

where J_s is the current density on the surface, d the distance from surface and δ the skin depth, defined as the depth below the surface of the conductor at which the current density has fallen to $1/e$ (about 0.37) of J_s. Its equation is

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \tag{2.4}$$

where ρ is the resistivity of the conductor and $\mu = \mu_r \mu_0$ its permeability.

From (2.4) it is clear that the skin effect is higher increasing the operating frequency.

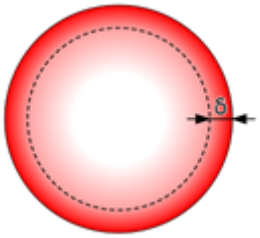


Fig. 2.13. Skin depth in a section of a conductor.

The proximity effect occurs when more conductors are nearby and they are carrying an alternating current. If the currents are flowing through one or more other nearby conductors, such as within a closely wound coil of wire, the distribution of current within the first conductor will be constrained to smaller regions. The resulting current crowding is termed as the proximity effect. This crowding gives an increase in the effective resistance of the circuit, which increases with frequency.

(a) (b)

Fig. 2.14. Proximity effect of two conductors with the opposite (a) and the same (b) current direction.

A solution for reducing the losses in the windings is the use of the Litz wire. It consists of many thin wire strands, individually insulated and twisted or woven together, often in several levels. It attenuates both effects above described because, if the wires that make up the conductor are of very small cross section, comparable to the depth of penetration, the high-frequency current will flow across approximately the entire section of a single wire and therefore of the entire conductor. This leads to a reduction of the skin effect which occurs in a single conductor of equivalent section. In addition, thanks to the twisted and woven wire, the proximity effect is minimized.

Fig. 2.15. Structure and example of Litz wire used in high frequency applications.

2.5 SST applications

SST can be used in many electrical systems where its advantages and functions can be useful. Existing SSTs are typically used in the distribution grid, with a voltage range from some kV up to tens of kV. Several application fields are:

Smart Grids : In future power systems the usage of renewable energy resources will require an energy management of the power flow between sources and loads. The SST, thanks to its functionalities, may match the request. The low voltage DC link has the function of common bus to connect the distributed energy sources while the whole SST operates as an energy router with the function of coordinate the power flow among the energy sources, the grid and the loads.

Distributed energy generation systems : For example in the offshore generation plants, use of SST reduces weight and size of the equipment and leads to advantages in efficiency and arrangement of the platforms.

Traction systems : SST can provide a significant reduction in train weight improving the traction efficiency and power density. Indeed the SST has been initially studied for the railway traction system.

Power quality : Several SST topologies have the capabilities to improve the power quality of the electric system. Among the most important ancillary services provided there are the compensation of the reactive power and the filtering of the currents harmonics. In addition, the SST can provide, using suitable control functions, fault isolation and limitation capabilities.

In addition to the above listed application fields, two applications of particular interest are presented more in detail in the following subsections: application of SST as a domestic interface and application of the SST as MV/LV interconnection [32]-[36].

Application of the SST as domestic interface

A sensible electricity demand rise is expected at the domestic level in the next future due to the transition of traditional uses from fossil fuels to the electrical domain, as space heating, vehicles supplying and cooking. This will allow an overall efficiency improvement of domestic end-users, increased safety and pollution abatement in urban contexts.

Nowadays the electrical main grid is managed in AC due to the i) hierarchical top-down approach for transmission and distribution grid, with voltage level depending on line length; ii) use of synchronous generators and asynchronous motors; iii) use of transformers to connect systems operating at different voltage levels; iv) easy interruption of alternative currents making use of traditional switches. However, the recent evolution of power converters is modifying this traditional approach while the number of power conversion stages between the grid and the load is increasing drastically. Among the main reasons there are:

- an increasing number of devices, such as led lighting, TVs, DVDs, computers, sensors, etc., that are supplied in DC current and are connected to the grid through an AC-DC conversion stage;
- several domestic appliances, such as machine drives, modern refrigerators, induction cooking systems, need variable output frequency to achieve better results in terms of quality and efficiency and, consequently, are connected to the AC through a rectifier followed by an inverter;
- local generation operating at DC (e.g. photovoltaic) has transformed passive end-users in active actors interacting with the grid and the electricity market;
- storage systems and electrical vehicles are going to become more and more diffused at the domestic level.

Many DC systems have been studied in recent years, both as new distribution network paradigm and as an opportunity related to end-users typical electrical loads [13][14][15]. From the power system point of view, the main advantages of DC networks are well known: i) lower conversion losses; ii) enhancement of line capability; iii) no reactive power flow and power factor management; iv) reduction of the variable electromagnetic field and increased safety, positively impacting on human health. As compared with AC traditional networks, DC distribution systems show an improved control of voltage at each appliance plug and power quality is sensibly increased also during disturbances. On the other side, emerging issues have to be considered, as the galvanic insulation with the main network (i.e. required in case of specific PV technologies).

In this context, the SST is a promising technology. Considering that electrical appliances can be composed by different power stages with proper electrical specs, a single SST would be able to electrically connect the different power stages in an optimized and coordinated way, avoiding the use of multiple converters with reduced efficiency. As regards to other solutions operating at industrial frequency, the SST, taking advantage by the high frequency internal transformer, guarantees the galvanic insulation without a dramatic impact on domestic spaces, being easily installable close to the energy meter and the end-user main protection.

Additionally, the power management capabilities of the static converters enable the SST to ensure the required domestic network flexibility while the energy efficiency is maximized thanks to the optimal integration of several components/appliances. At the same time, the SST operates as equivalent aggregator in supplying ancillary services to the grid (i.e. harmonic filtering and voltage balancing). An example of the domestic SST concept is reported in Fig. 2.16.

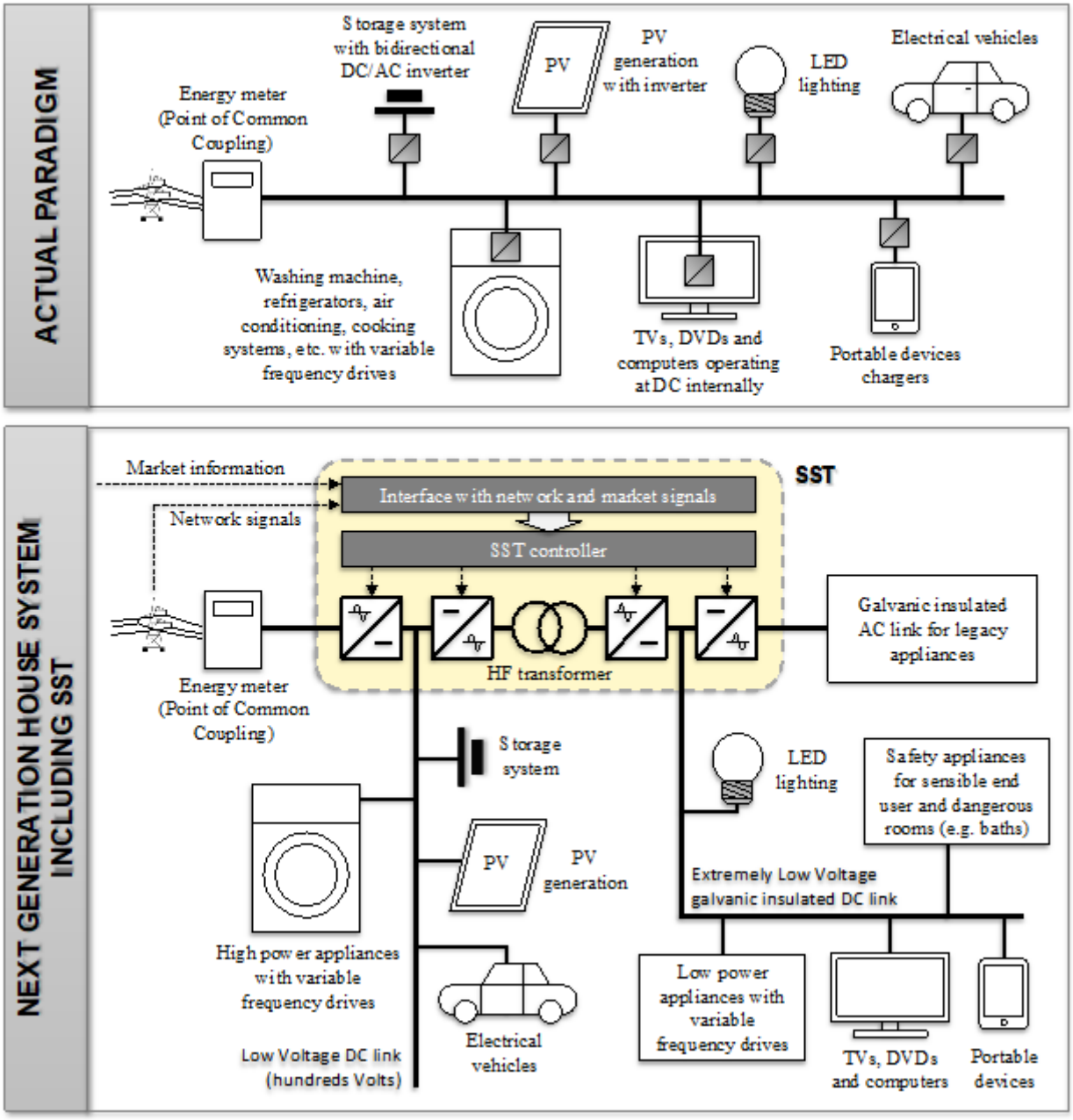


Fig. 2.16 Example of the SST in integrating sources and appliances at the domestic level.

The proposed structure of the domestic multi-link distribution scheme is composed by:

- an AC network interface (single-phase 230 V), with traditional distribution to internal loads without galvanic insulation;
- a low voltage DC link, with rated value of few hundreds Volts, for the supply of high power devices, as principal loads (e.g. washing machines, induction cooking systems, air conditioners,

heat pumps, etc.), local generation systems (e.g. photovoltaic, domestic wind plants, fuel cells, etc.), battery storage systems and bidirectional chargers for electrical vehicles;

- an extremely low voltage galvanic insulated DC link for lighting, safety appliances and specific rooms supply, as bathrooms, children rooms, etc.;
- a low voltage galvanic insulated AC link, with rated value equal to main network specifications to supply loads requiring separation from the main grid and to guarantee a progressive evolution of present houses to future smart domestic systems.

The distribution topology and each component of the SST chain will have to be studied in order to allow bidirectional power exchanges between the different internal links, allowing the maximum flexibility in the end-user behaviour.

From the power system perspective, the optimal design of the SST aims to maximize the AC/DC domestic distribution advantages, both in terms of main structure and rated values (which means primarily the voltage levels of all the AC/DC links). This can be done by considering: i) the ongoing evolution trends of main appliances, local generators, storage systems and electrical vehicles exploitation; ii) the overall efficiency of the entire domestic domain; iii) the health protection, safety and electromagnetic pollution.

A general supervisor will control the complete domestic system, being directly in connection with the distribution grid manager in order to make available the exchange of ancillary services between the network and the intelligent end-user. Furthermore, market signals will be considered by the supervisor in order to maximize the economic benefit for the domestic end-user: renewable exploitation, storage resources optimization (also including electrical vehicles) and load response are functions easy to be integrated in the SST management.

Several advantages in comparison with the traditional domestic plant are easily identifiable:

- The DC system advantages combined with the galvanic insulation are perfectly exploited in terms of voltage and frequency stability for the supplied appliances, both in DC and in AC. Network perturbations, as voltage drops, transient phenomena and over-voltages, can be filtered in order to enhance the Power Quality for sensible appliances;

- Adopting an increased voltage level (few hundreds Volts) for the main DC link supplying the high power appliances and devices, network losses are reduced by both the reduction of circulating currents and the rejection of the reactive component;

- An Extra Safety DC section is introduced for reducing the human exposition to the electrical risk in case of critical appliances, end-users or rooms. A drastic reduction of the short circuit currents are attended since they are limited by the electronic converters in a very short time;

- Various systems can be integrated, allowing the domestic plant to operate as a unique entity as regards to the main grid and the market. A perfect control of the active and reactive power exchanged with the distributions system is guaranteed by the converter controllers. On the end-user side, the SST can operate as energy gateway in accordance with the home automation environment.

Application of the SST as MV/LV interconnection

With the growing number of dispersed generators connected to the MV e LV networks, some issues in the distribution networks operation have to be faced. In this field, the SST adoption in alternative to traditional industrial frequency transformer can represent an interesting solution. A conceptual representation of the SST application is shown in Fig. 2.17.

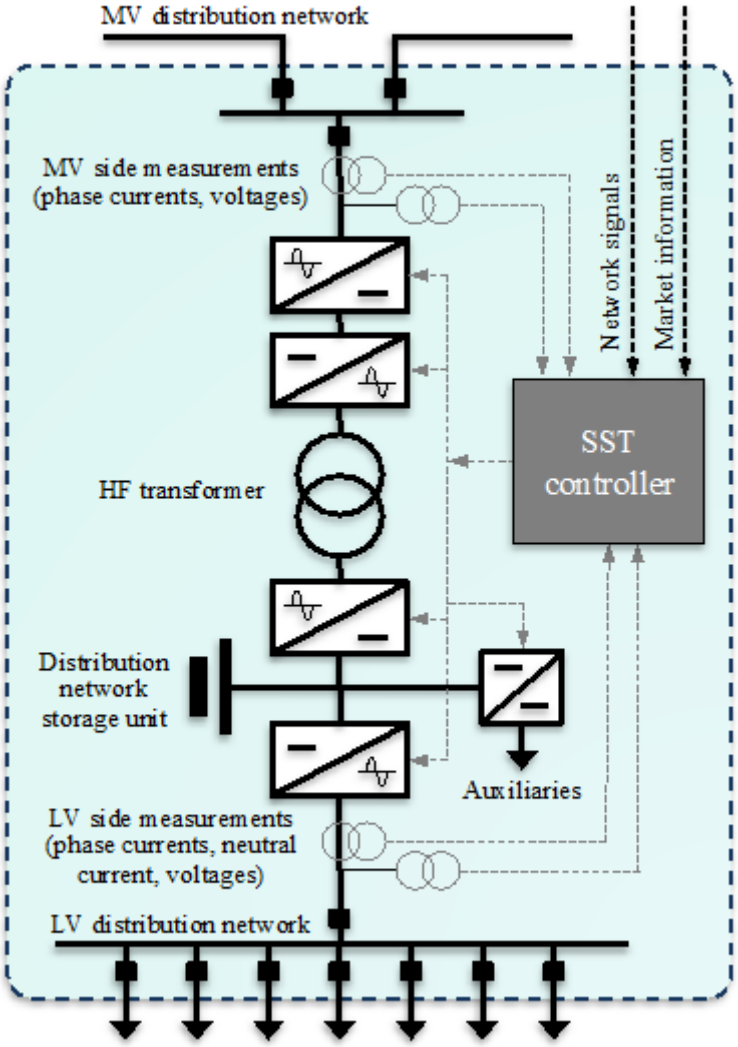


Fig. 2.17 Application of the SST concept as MV/LV interconnection

Several advantages of the use of the SST as MV/LV interconnection are reported below.

• Advantages in terms of supplied voltage and frequency stability, power quality and heartlessness to network events and perturbations. In particular, in case the MV system is managed with earthed or compensated neutral, the over-voltages in the MV system caused by phase-to-ground faults are not reflected in the LV network, preserving end-user appliances from damages. Also the benefits in terms of size and weight can be very interesting if the available space is limited, e.g. in urban contexts in case of network reinforcement.

• A SST can regulate the MV/LV ratio in accordance with the network operating conditions, facilitating the voltage control of the LV system independently from the MV voltage level. A sort of dynamic On Load Tap Changer (OLTC) is obtained. The voltage ratio, independently adjustable phase by phase, can be set in wide and continuous range of values in accordance with the voltage regulation issues or to obtain a partial regulation of the load consumption.

• Considering three-phase circuits, the current balancing of each phase can be regulated independently. Speaking about the LV side, the single-phase regulation of the voltage ratio, combined with a real-time controller, is able to enhance the system balancing in particular when the MV/LV station supplies a large number of single-phase end-users with high penetration of daily-variable

generation (e.g. PVs). From the MV system point of view, the unbalance in the LV networks is not reported in the MV distribution network. Furthermore, the SST can intentionally absorb unbalanced currents to equilibrate the MV network and regulate its reactive power exchange to participate to the MV network management, in accordance with the grid operator requirements.

- The short circuit currents in case of fault in the LV network strongly depends on the SST main characteristics, both in terms of components and controllers. Then, the short circuit current can be easily contained and eliminated in a short time by integrating the protection function in the MV/LV SST, without requiring external breakers.

- An intelligent device introduced in the MV/LV interconnection can operate as virtual aggregator of the LV end-users and operate accordingly to the MV system operator in exchanging ancillary services.

CHAPTER 3

Single Active Bridge converter

The Single Active Bridge converter (SAB) is composed of two H-bridges: an active input bridge, which performs the DC to AC conversion, and a passive output bridge, which performs the AC to DC conversion [37]-[40]. Between the two bridges, there is a high frequency transformer that guarantees the galvanic isolation between the input and output. The SAB converter has the circuit schematic of Fig. 3.1.

The bridge supplied by the DC voltage source (input bridge) is set up with four switches S_1-S_4, each composed of a transistor paralleled by a diode. The bridge feeding the load (output bridge) is set up with diodes D_5-D_8. The transformer has the voltage ratio n, hereafter set at 1 for simplicity, and a total leakage inductance L. Then the AC link can be represented by the inductance L. Adjustment of the output voltage V_o is achieved by the control of phase of the input bridge legs, with V_o that does not exceed the input voltage V_i. The analysis is carried out for converters supplied by a DC voltage source, loaded with a resistance and impressing a DC voltage across the load. The output filter, which smoothens the DC voltage applied to the load, is in cascade to the output bridge and consists of the capacitor C_o. The load is constituted by the resistance R_L. The input filter, which is not drawn in Fig. 3.1, consists of a LC filter that smoothens the current drawn from the DC voltage source.

Due to the diode output bridge, SAB converters allow for a unidirectional power flow of buck type (apart from the transformer turn ratio) whilst DAB converters, which are presented in the next chapter, allow for a bidirectional power flow of buck-boost type.

The bridges operate at high frequency; this consistently shrinks the passive components (transformer, input and output filters) of the SAB converter so that it stands out for its high values of power density and specific power.

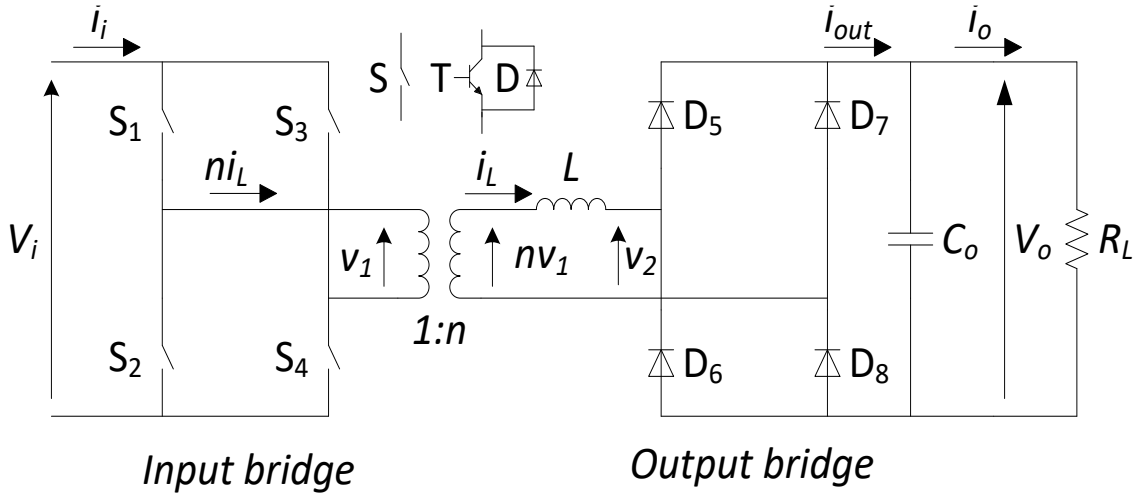


Fig. 3.1 SAB converter circuit schematic.

3.1 Steady-state operation

A SAB converter operates in two modes: Discontinuous Conduction Mode (DCM) and Continuous Conduction Mode (CCM). DCM and CCM are separated by the so-called Boundary Mode (BM). Below, operation of a SAB converter is analyzed in steady-state. The effects of the parasitic resistances are neglected so that inductance current is assumed piecewise linear.

3.1.1 Discontinuous conduction mode (DCM)

Figs. 3.2 (a)-(c) plot voltages and currents, together with the conducting devices, for the SAB converter operating in DCM. From the traces it emerges that voltages and currents have half-wave symmetry. The input bridge is commanded over π as follows: at $\theta = 0$ transistors T_1 and T_4 are turned on; at $\theta = \alpha$ transistor T_4 is turned off and transistor T_3 is turned on. The phase angle α plays the role of command variable. The voltage v_1 impressed by the input bridge across the AC link is plotted in Fig. 3.2 (a) with solid line.

Until $\theta = \alpha$ the current i_L through the inductance L increases; afterwards it decreases up to vanish at $\theta = \beta$ as shown in Fig. 3.2 (b). During the interval from 0 to β diodes D_5 and D_8 conduct and the voltage v_2 impressed by the output bridge across the AC link has the waveform plotted in Fig. 3.2 (a) with dotted line.

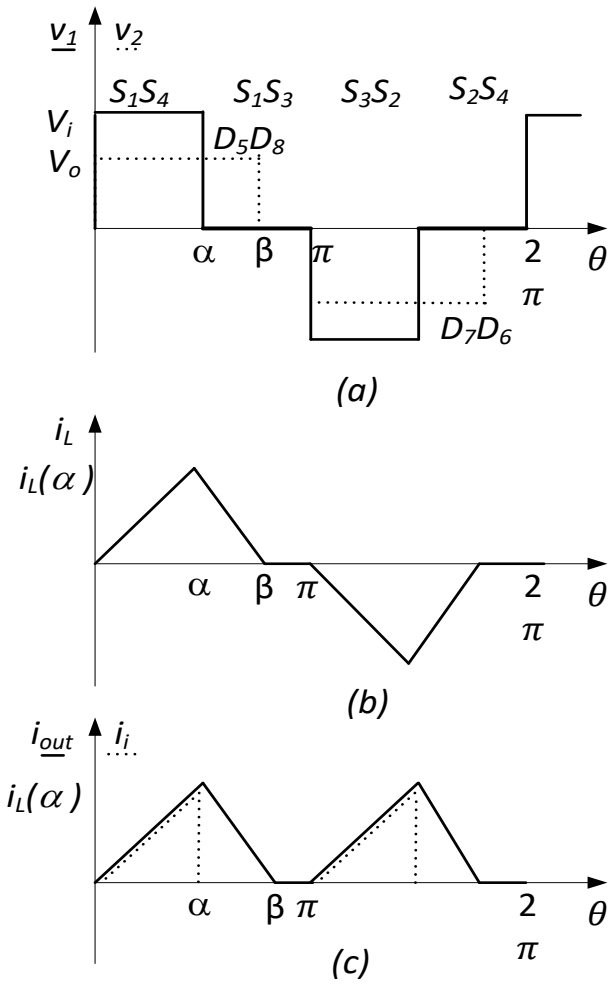


Fig. 3.2. SAB converter current and voltage waveforms in DCM.

Looking at Figs. 3.2, three intervals can be recognized over π, namely $0 \div \alpha$, $\alpha \div \beta$ and $\beta \div \pi$, with different values of the voltage (v_1-v_2) applied across the inductance L. Current i_L at the extremities of the intervals is given by

- $[0 \div \alpha]$

$$i_L(\alpha) = i_L(0) + \int_0^{\alpha} \frac{V_L}{\omega L} d\theta = 0 + \frac{V_i - V_o}{\omega L}\alpha \tag{3.1}$$

- $[\alpha \div \beta]$

$$i_L(\beta) = i_L(\alpha) + \int_{\alpha}^{\beta} \frac{V_L}{\omega L} d\theta = i_L(\alpha) - \frac{V_o}{\omega L}(\beta - \alpha) = 0 \tag{3.2}$$

Solving the circuit equations at steady-state, it results that i_L at $\theta = \alpha$ is equal to

$$i_L(\alpha) = \frac{V_i}{\omega L}\pi\left(1 - \frac{V_o}{V_i}\right)\frac{\alpha}{\pi} \tag{3.3}$$

where ω is the angular frequency, and the angle where i_L vanishes is

$$\frac{\beta}{\pi} = \frac{V_i}{V_o}\frac{\alpha}{\pi} \tag{3.4}$$

For a SAB converter to operate in DCM, β must be less than π, which yields the following condition:

$$\frac{\alpha}{\pi} < \frac{V_o}{V_i} \tag{3.5}$$

The output current i_{out} and the input current i_i of a SAB converter are plotted in Fig. 3.2 (c) with solid and dotted line, respectively. Because of the capacitor filter, the load current i_o is given by the average value I_o of i_{out}. Its expression is

$$I_{o,DCM} = \frac{1}{\pi}\left(\frac{i_L(\alpha)\cdot\alpha}{2} + \frac{i_L(\alpha)\cdot(\beta-\alpha)}{2}\right) = \frac{V_i}{\omega L}\frac{\pi}{2}\frac{\alpha^2}{\pi^2}\left(\frac{V_i}{V_o} - 1\right) \tag{3.6}$$

The active power delivered is obtained multiplying the average current by the output voltage that it is assumed constant.

$$P_{o,DCM} = \frac{V_i V_o}{\omega L}\frac{\pi}{2}\frac{\alpha^2}{\pi^2}\left(\frac{V_i}{V_o} - 1\right) \tag{3.7}$$

From (3.6), the output voltage V_o, for a generic load R_L, is given by:

$$V_{o,DCM} = V_i\frac{R_L}{4\pi}\frac{\alpha^2}{\omega L}\left[-1 + \sqrt{1 + \frac{8\pi\omega L}{R_L\alpha^2}}\right] \tag{3.8}$$

3.1.2 Continuous conduction mode (CCM)

Figs. 3.3 (a)-(c) plot voltages and currents, together with the conducting devices, for the SAB converter operating in CCM. Compared to DCM, the basic difference is that, over π, i_L is negative in the interval $0 \div \varphi$, the latter angle being termed current shift angle. During this interval, diodes D_6 and D_7 of the output bridge conduct, and the voltage v_2 impressed by the output bridge across the AC link is $-V_o$. From (3.5), the condition for operation in CCM is

$$\frac{\alpha}{\pi} > \frac{V_o}{V_i} \tag{3.9}$$

Looking at Figs. 3.3, three intervals can be recognized over π, namely $0 \div \varphi$, $\varphi \div \alpha$ and $\alpha \div \pi$, with different values of the voltage (v_1-v_2) applied across the inductance L. Current i_L at the extremities of the intervals is given by

- $[0 \div \varphi]$

$$i_L(\varphi) = i_L(0) + \int_0^{\varphi} \frac{V_L}{\omega L} d\theta = i_L(0) + \frac{V_i + V_o}{\omega L}\varphi = 0 \tag{3.10}$$

- $[\varphi \div \alpha]$

$$i_L(\alpha) = i_L(\varphi) + \int_{\varphi}^{\alpha} \frac{V_L}{\omega L} d\theta = 0 + \frac{V_i - V_o}{\omega L}(\alpha - \varphi) \tag{3.11}$$

- $[\alpha \div \pi]$

$$i_L(\pi) = -i_L(0) = i_L(\alpha) + \int_{\alpha}^{\pi} \frac{V_L}{\omega L} d\theta = i_L(\alpha) - \frac{V_o}{\omega L}(\pi - \alpha) \tag{3.12}$$

By exploiting the half-wave symmetry of i_L over π, the values of i_L at $\theta = 0$ and at $\theta = \alpha$ are readily calculated in

$$i_L(0) = -\frac{V_i}{\omega L}\frac{\pi}{2}\left(1 + \frac{V_o}{V_i}\right)\left(\frac{\alpha}{\pi} - \frac{V_o}{V_i}\right) \tag{3.13}$$

$$i_L(\alpha) = \frac{V_i}{\omega L}\frac{\pi}{2}\left(1 - \frac{V_o}{V_i}\right)\left(\frac{\alpha}{\pi} + \frac{V_o}{V_i}\right) \tag{3.14}$$

In turn, the current shift angle is calculated in

$$\varphi = \frac{\pi}{2}\left(\frac{\alpha}{\pi} - \frac{V_o}{V_i}\right) \tag{3.15}$$

and the load current I_o in

$$I_{o,CCM} = \frac{1}{\pi}\left[\frac{-i_L(0)\cdot\varphi}{2} + \frac{i_L(\alpha)\cdot(\alpha-\varphi)}{2} + \frac{\left(i_L(\alpha)+i_L(\pi)\right)\cdot(\pi-\alpha)}{2}\right] =$$

$$= \frac{V_i}{\omega L}\frac{\pi}{2}\left[\frac{\alpha}{\pi} - \frac{1}{2}\left(\frac{\alpha}{\pi}\right)^2 - \frac{1}{2}\left(\frac{V_o}{V_i}\right)^2\right] \tag{3.16}$$

The active power delivered is obtained multiplying the average current by the output voltage which is assumed constant.

$$P_{o,CCM} = \frac{V_i V_o}{\omega L}\frac{\pi}{2}\left[\frac{\alpha}{\pi} - \frac{1}{2}\left(\frac{\alpha}{\pi}\right)^2 - \frac{1}{2}\left(\frac{V_o}{V_i}\right)^2\right] \tag{3.17}$$

The output voltage V_o, for a generic load R_L, is given by:

$$V_{o,CCM} = V_i \frac{2}{\pi}\frac{\omega L}{R_L}\left[-1 + \sqrt{1 + \left(\frac{2\alpha}{\pi} - \frac{\alpha^2}{\pi^2}\right)^2\left(\frac{\pi}{2}\frac{R_L}{\omega L}\right)^2}\right] \tag{3.18}$$

Eqs. (3.6) and (3.16) show that, in both DCM and CCM, the load current I_o depends on the output voltage V_o, besides on the command variable α. The relationship between I_o and α is plotted in Fig. 3.4 for different values of V_o, where here and in the following figures the dashed traces refer to DCM and the solid ones to CCM. Moreover, the variables in the plots of this paragraph and in the following paragraphs are normalized to the base values:

$$I_{base} = \frac{V_i}{\omega L}, \quad \alpha_{base} = \pi, \quad V_{base} = V_i$$

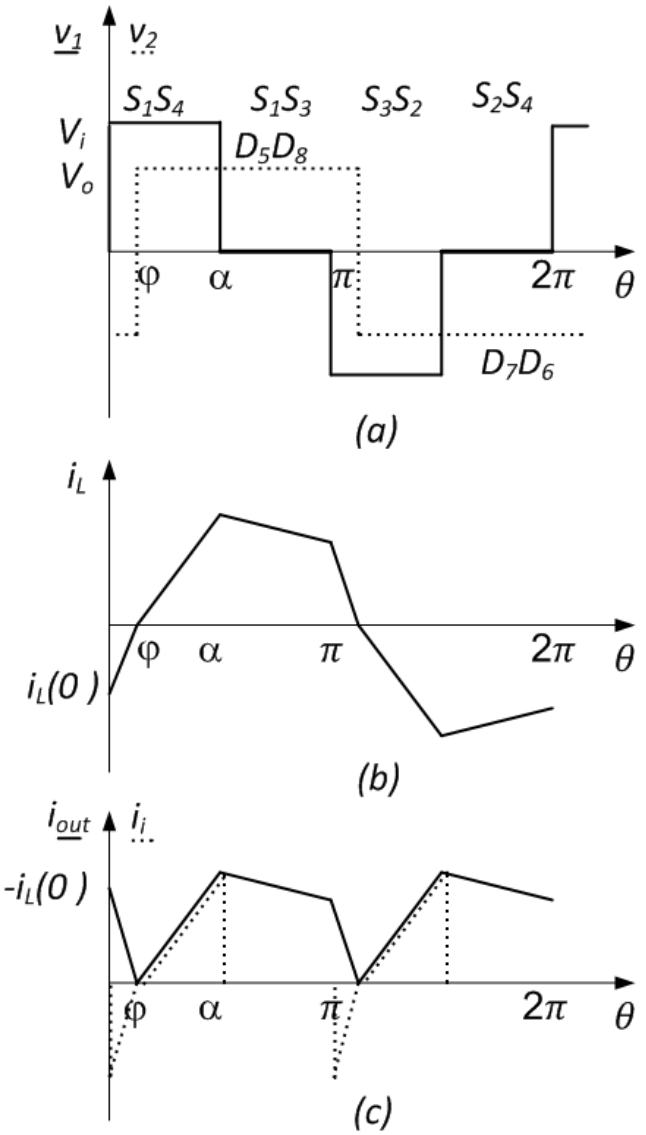


Fig. 3.3. SAB converter current and voltage waveforms in CCM.

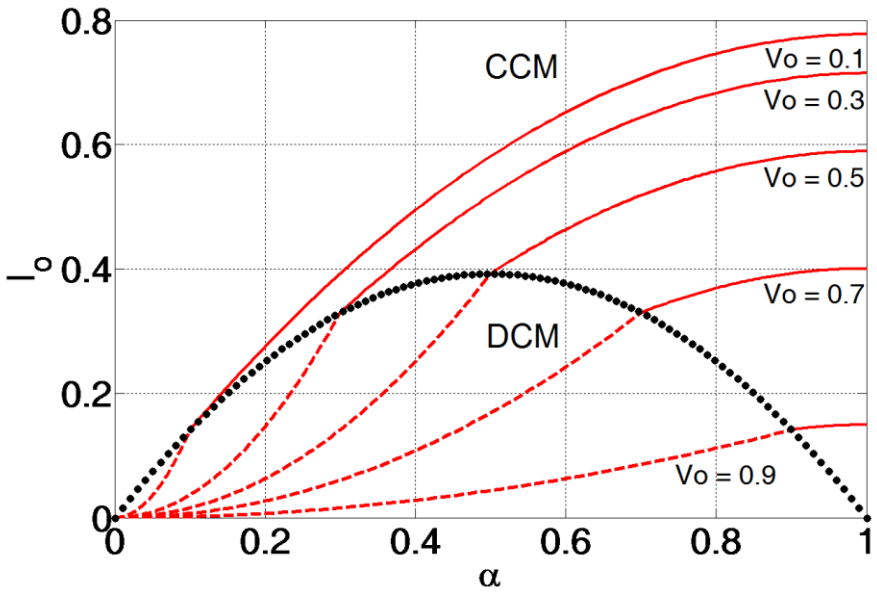
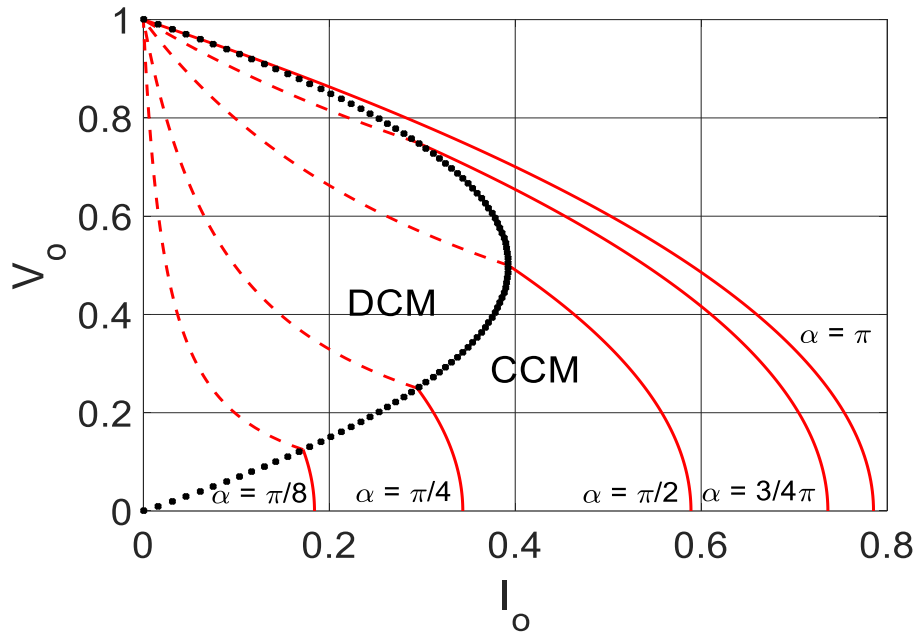


Fig. 3.4. SAB converter load current vs. command variable.

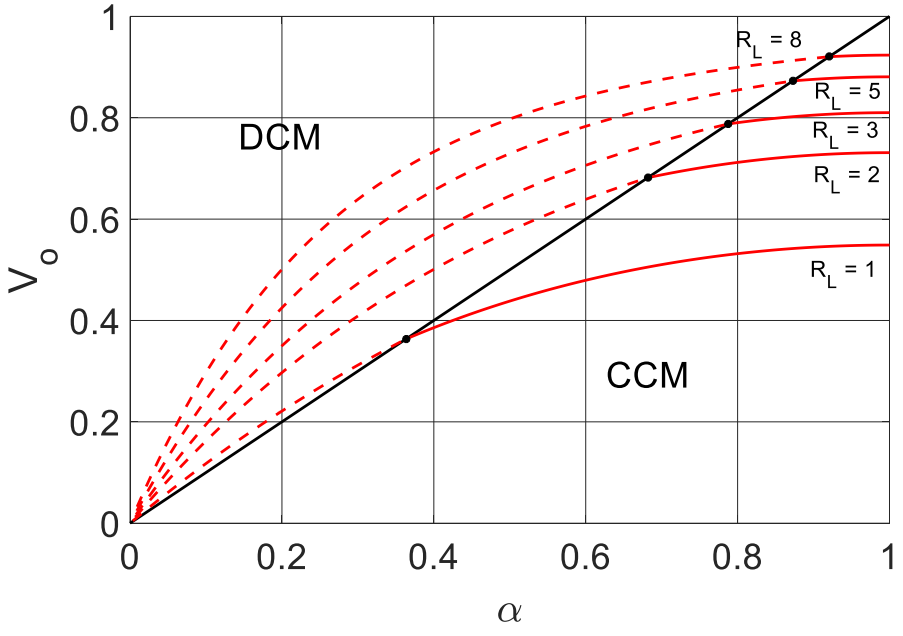
The traces of Fig. 3.4 outline that, as V_o increases, i) the current deliverable to the load decreases, and ii) both the ranges of current and α in CCM decrease. BM operation is obtained by setting $\alpha/\pi=V_o/V_i$ in (3.6) or in (3.16), leading to

$$I_{o,BM} = \frac{V_i}{\omega L}\frac{\pi}{2}\frac{\alpha}{\pi}\left(1-\frac{\alpha}{\pi}\right) \tag{3.19}$$

Eq. (3.19) shows that the locus of BM is a downward concave parabola with the vertex at $I_o=0.39$, $\alpha=0.5$. The parabola is plotted in Fig. 3.4 with dotted line.



(a)



(b)

Fig. 3.5. SAB output voltage vs. load current (a) and command variable (b).

The output voltage is plotted as a function of the output current in Fig. 3.5 (a) and the command variable in Fig.3.5 (b).

Fig. 3.5 (a) highlights that the maximum current deliverable by the converter, obtainable for $\alpha = \pi$ (SAB operates in square wave) and $V_o = 0$ (short circuit condition) is given by:

$$I_{o,max} = \frac{1}{4}\left[2\pi - \frac{\pi^2}{\pi}\right] = \frac{\pi}{4} \approx 0.79 \tag{3.20}$$

Fig. 3.5 (b) highlights that increasing the load resistance ("load more light") the achievable voltage is higher and the converter operates in CCM for a smaller interval of the control variable α.

3.2 Design characteristics

In the next subparagraphs, the design characteristics, helpful in sizing the input and output filters, switches and diodes of the converters, are calculated.

3.2.1 Output current alternating component rms value

The current entering into the output capacitor C_o coincides with the alternate component of i_{out}. The rms value of this component is calculated in

$$I_{rms,o} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_L(\theta)^2 d\theta - I_o^2} \tag{3.21}$$

Looking at Fig. 3.6 (a) the calculation of the rms value in DCM, considering the two areas, is the following.

1)

$$\frac{\theta-0}{\alpha-0} = \frac{i_L(\theta)-0}{i_L(\alpha)-0} \qquad => \qquad i_L(\theta) = i_L(\alpha)\frac{\theta}{\alpha}$$

$$\int_0^{\alpha} i_L(\theta)^2\, d\theta = i_L(\alpha)^2 \frac{\alpha}{3} \tag{3.22}$$

2)

$$\frac{\theta-\alpha}{\beta-\alpha} = \frac{i_L(\theta)-i_L(\alpha)}{0-i_L(\alpha)} \qquad => \qquad i_L(\theta) = i_L(\alpha) - i_L(\alpha)\frac{\theta-\alpha}{\beta-\alpha}$$

$$i_L(\theta)^2 = i_L(\alpha)^2 + i_L(\alpha)^2\frac{(\theta-\alpha)^2}{(\beta-\alpha)^2} - 2i_L(\alpha)^2\frac{\theta-\alpha}{\beta-\alpha}$$

$$\int_{\alpha}^{\beta} i_L(\theta)^2\, d\theta = i_L(\alpha)^2 \frac{\beta-\alpha}{3} \tag{3.23}$$

From the eqs. (3.22) and (3.23) the rms value of the alternating component of the output current in DCM is

$$I_{rms,o,DCM} = \sqrt{\frac{1}{3} i_L(\alpha)^2 \frac{\beta}{\pi} - I_o^2} \tag{3.24}$$

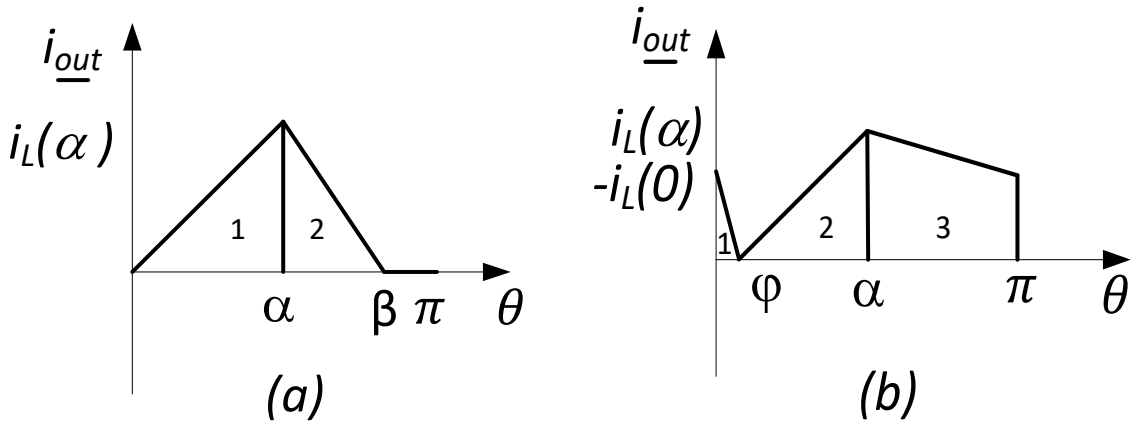


Fig.3.6. waveform of the output current in DCM (a) and CCM (b).

Looking at Fig. 3.6 (b) the calculation of the rms value in CCM, considering the three areas, is the following.

1)

$$\frac{\theta-0}{\varphi-0}=\frac{i_L(\theta)+i_L(0)}{0+i_L(0)} \quad => \quad i_L(\theta)=-i_L(0)+i_L(0)\frac{\theta}{\varphi}$$

$$i_L(\theta)^2=i_L(0)^2+i_L(0)^2\frac{\theta^2}{\varphi^2}-2i_L(0)^2\frac{\theta}{\varphi}$$

$$\int_0^{\varphi} i_L(\theta)^2\,d\theta=i_L(0)^2\frac{\varphi}{3} \tag{3.25}$$

2)

$$\frac{\theta-\varphi}{\alpha-\varphi}=\frac{i_L(\theta)-0}{i_L(\alpha)-0} => \quad i_L(\theta)=i_L(\alpha)\frac{\theta-\varphi}{\alpha-\varphi}$$

$$\int_{\varphi}^{\alpha} i_L(\theta)^2\,d\theta=i_L(\alpha)^2\frac{\alpha-\varphi}{3} \tag{3.26}$$

3)

$$\frac{\theta-\alpha}{\pi-\alpha}=\frac{i_L(\theta)-i_L(\alpha)}{-i_L(0)-i_L(\alpha)} \quad => \quad i_L(\theta)=i_L(\alpha)-[i_L(0)+i_L(\alpha)]\frac{\theta-\alpha}{\pi-\alpha}$$

$$i_L(\theta)^2=i_L(\alpha)^2+[i_L(0)+i_L(\alpha)]^2\frac{(\theta-\alpha)^2}{(\pi-\alpha)^2}-2i_L(\alpha)[i_L(0)+i_L(\alpha)]\frac{(\theta-\alpha)}{(\pi-\alpha)}$$

$$\int_{\alpha}^{\pi} i_L(\theta)^2\,d\theta=i_L(\alpha)^2(\pi-\alpha)+[i_L(0)+i_L(\alpha)]^2\frac{(\pi-\alpha)}{3}-i_L(\alpha)[i_L(0)+i_L(\alpha)](\pi-\alpha) \tag{3.27}$$

From the eqs. (3.25) - (3.27) the rms value of the alternating component of the output current in CCM is

$$I_{rms,o,CCM}=\sqrt{\frac{1}{3}\left[\Lambda_{SAB}-\frac{\varphi}{\pi}i_L(\alpha)^2+\frac{\varphi}{\pi}i_L(0)^2\right]-I_o^2} \tag{3.28}$$

where

$$\Lambda_{SAB}=i_L(\alpha)^2+i_L(0)^2\left(1-\frac{\alpha}{\pi}\right)-i_L(\alpha)i_L(0)\left(1-\frac{\alpha}{\pi}\right)$$

The relationship between $I_{rms,o}$ and I_o is plotted in Fig. 3.7, where, like in the other figures of this chapter, the black dots denote operation in BM.

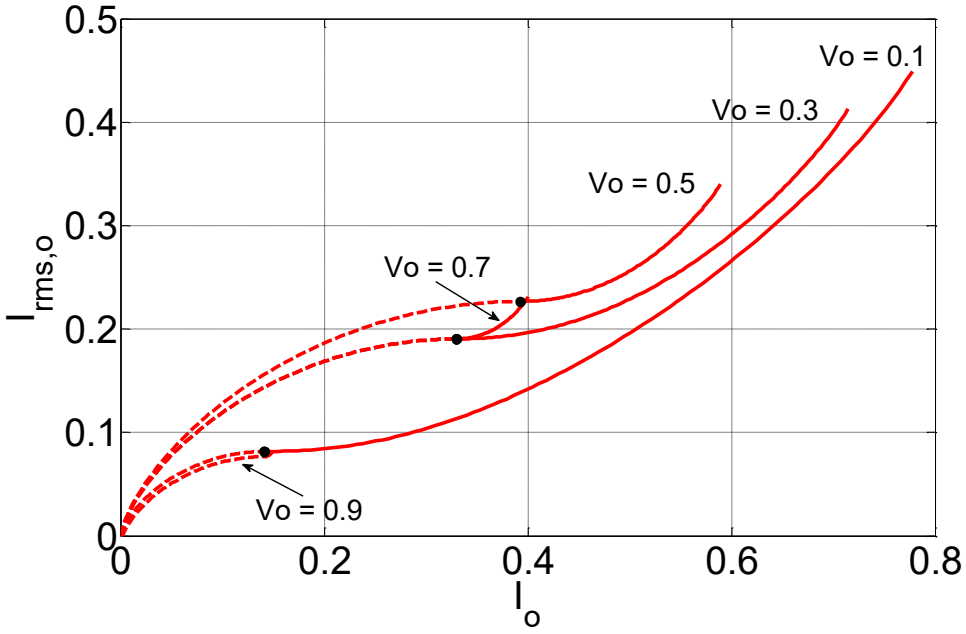


Fig. 3.7. SAB rms value of the alternating component of the output current vs. load current.

3.2.2 Output current ripple

The peak-to-peak ripple R_o of the output current is given by $i_L(\alpha)$. Then R_o is equal to (3.3) in DCM, i.e. to

$$R_{o,DCM} = \frac{V_i}{\omega L}\pi\left(1 - \frac{V_o}{V_i}\right)\frac{\alpha}{\pi} \tag{3.29}$$

and to (3.14) in CCM, i.e. to

$$R_{o,CCM} = \frac{V_i}{\omega L}\frac{\pi}{2}\left(1 - \frac{V_o}{V_i}\right)\left(\frac{\alpha}{\pi} + \frac{V_o}{V_i}\right) \tag{3.30}$$

The relationship between R_o and I_o is plotted in Fig. 3.8.

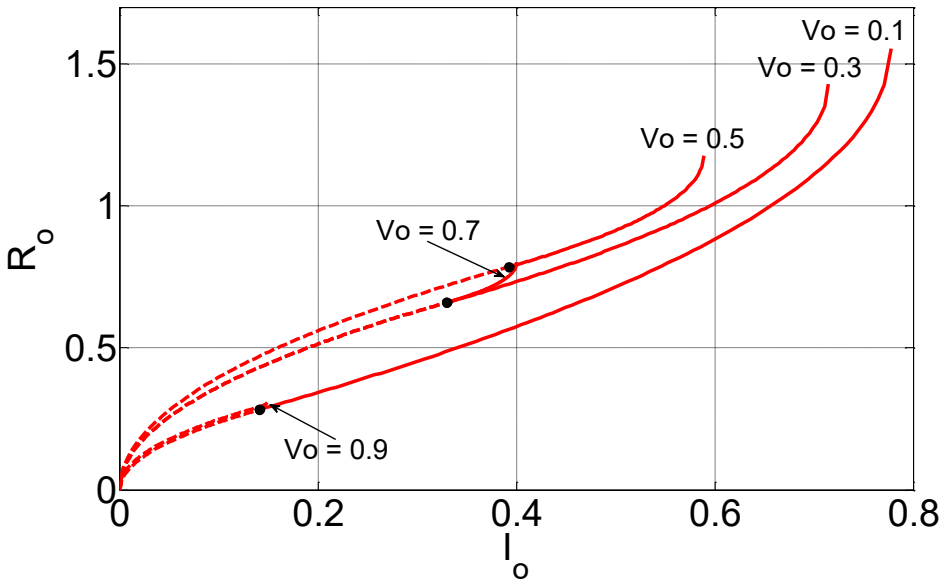


Fig. 3.8. SAB converter output current ripple vs. load current.

3.2.3 Input current average value

By equating the average power at the input of the SAB converter to the one at the output, the average value I_i of the input current can be readily found in

$$I_i = \frac{V_o}{V_i} I_o \tag{3.31}$$

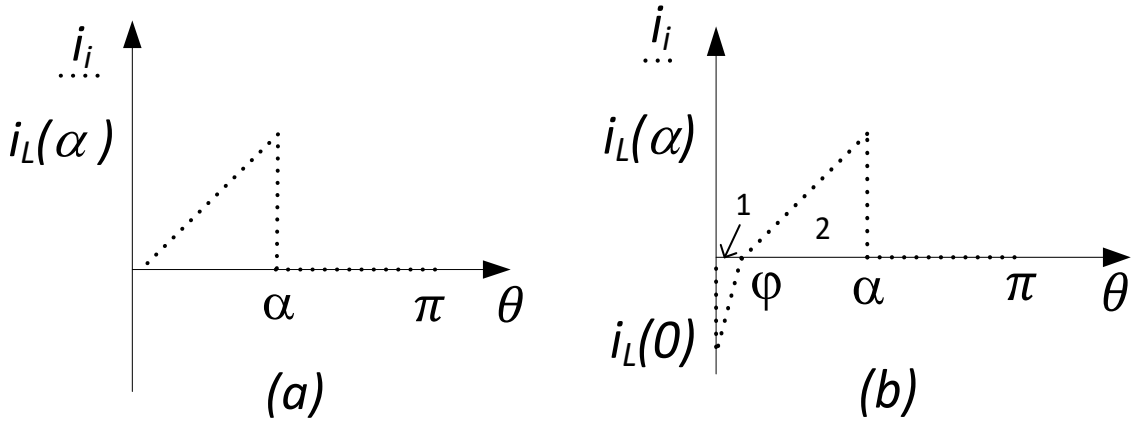


Fig.3.9. waveform of the input current in DCM (a) and CCM (b).

3.2.4 Input current alternating component rms value

The rms value of the alternating component of the input current is calculated in

$$I_{rms,i} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_L(\theta)^2 d\theta - I_i^2} \tag{3.32}$$

Looking at Fig. 3.9 (a) the calculation of the rms value in DCM is the following.

$$\frac{\theta - 0}{\alpha - 0} = \frac{i_L(\theta) - 0}{i_L(\alpha) - 0} \Rightarrow \quad i_L(\theta) = i_L(\alpha)\frac{\theta}{\alpha}$$

$$I_{rms,i,DCM} = \sqrt{\frac{1}{\pi}\int_0^{\alpha} i_L(\theta)^2 d\theta - I_i^2} = \sqrt{\frac{1}{3} i_L(\alpha)^2 \frac{\alpha}{\pi} - I_i^2} \qquad (3.33)$$

Looking at Fig. 3.9 (b) the calculation of the rms value in CCM, considering the two areas, is the following.

1)

$$\frac{\theta-0}{\varphi-0} = \frac{i_L(\theta)-i_L(0)}{0-i_L(0)} \quad \Rightarrow \quad i_L(\theta) = i_L(0) - i_L(0)\frac{\theta}{\varphi}$$

$$i_L(\theta)^2 = i_L(0)^2 + i_L(0)^2 \frac{\theta^2}{\varphi^2} - 2 i_L(0)^2 \frac{\theta}{\varphi}$$

$$\int_0^{\varphi} i_L(\theta)^2 \, d\theta = i_L(0)^2 \frac{\varphi}{3} \qquad (3.34)$$

2)

$$\frac{\theta-\varphi}{\alpha-\varphi} = \frac{i_L(\theta)-0}{i_L(\alpha)-0} \Rightarrow \quad i_L(\theta) = i_L(\alpha)\frac{\theta-\varphi}{\alpha-\varphi}$$

$$\int_{\varphi}^{\alpha} i_L(\theta)^2 \, d\theta = i_L(\alpha)^2 \frac{\alpha-\varphi}{3} \qquad (3.35)$$

From the eqs. (3.34) and (3.35) the rms value of the alternating component of the input current is

$$I_{rms,i,CCM} = \sqrt{\frac{1}{3}\left[i_L(\alpha)^2\left(\frac{\alpha}{\pi} - \frac{\varphi}{\pi}\right) + i_L(0)^2 \frac{\varphi}{\pi}\right] - I_i^2} \qquad (3.36)$$

The relationship between $I_{rms,i}$ and I_o is plotted in Fig. 3.10.

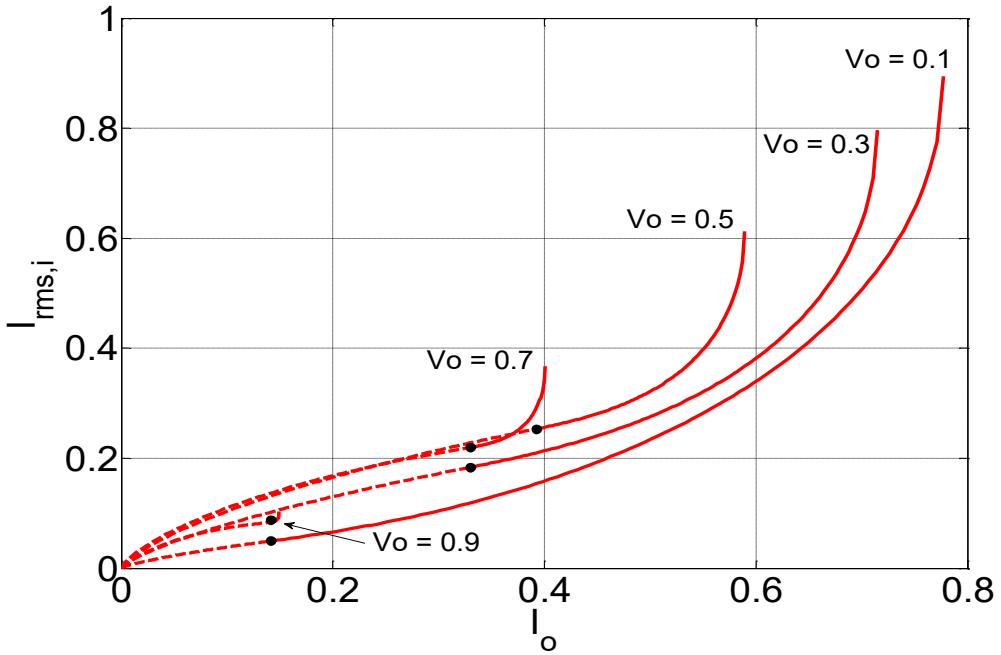


Fig. 3.10 SAB rms value of the alternating component of the input current vs. load current.

3.2.5 Input current ripple

The peak-to-peak ripple R_i of the input current is the same as R_o. Then it is still given by (3.29) in DCM and by (3.30) in CCM, and therefore its plot as a function of I_o is still given by Fig. 3.8.

3.2.6 Bridge device currents

The current is not equally distributed in the devices that constitute the switches of the input bridge. Specifically, the transistors of the leg 1-2 (i.e. T_1 and T_2) and the diodes of the leg 3-4 (i.e. D_3 and D_4) conduct for a longer time interval than the other devices. Since the sizing of the input bridge is tailored to the most solicited devices, the average and rms values of current are evaluated for these devices.

In DCM, i_L flows into transistor T_1 from 0 to β, and in diode D_3 from α to β. In CCM, i_L flows into transistor T_1 from φ to π and in diode D_3 from α to π+φ. The conduction times of transistor T_2 and diode D_4 are respectively equal to those of T_1 and D_3. With regard to the diodes of the output bridge, the current i_L flows in diodes D_5 and D_8 when positive and in diodes D_6 and D_7 when negative.

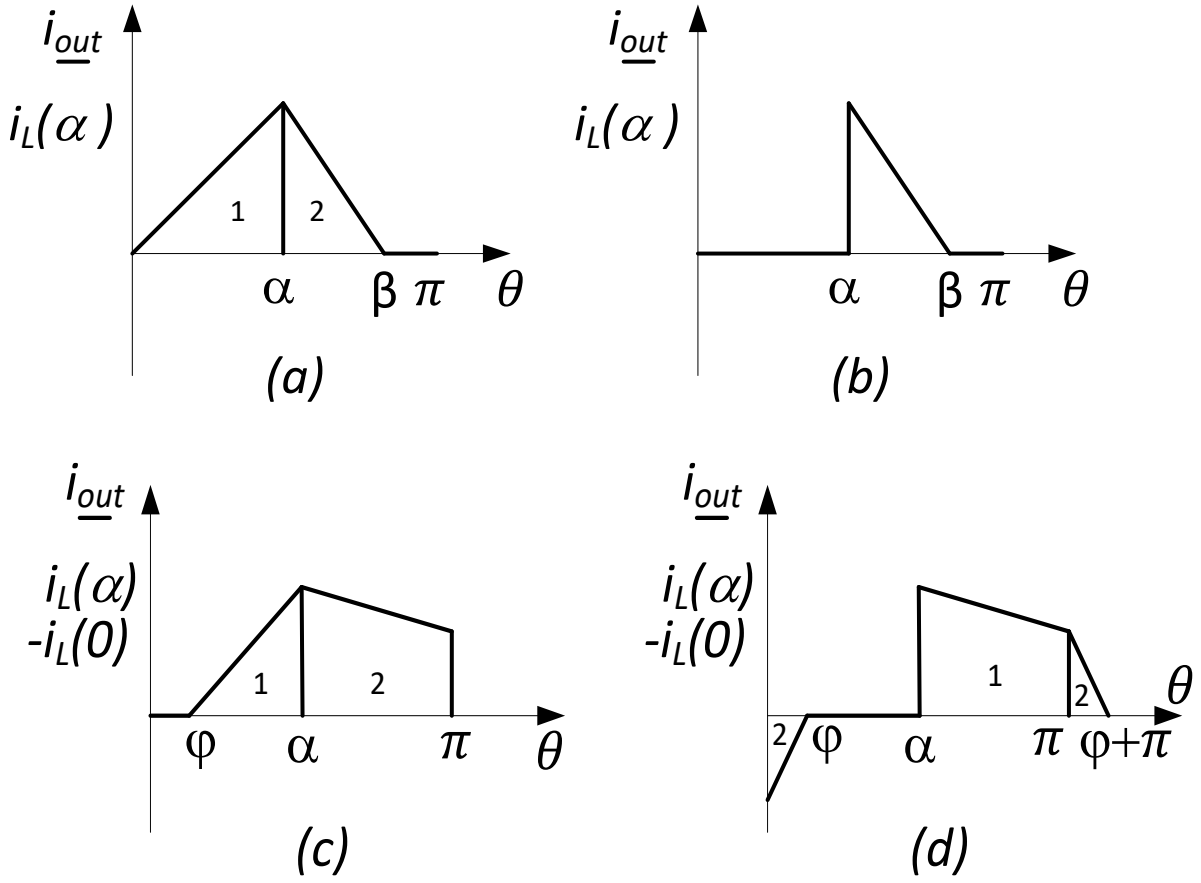


Fig. 3.11. Conduction intervals of the transistors (a) and diodes (b) in DCM, and conduction intervals of the transistors (c) and diodes (d) in CCM of the transistors of the leg 1-2 and diodes of the leg 3-4 of the input bridge.

3.2.7 Device peak currents

The currents in the transistors and diodes of the input bridge ($I_{p,T,ib}$, $I_{p,D,ib}$), and in the diodes ($I_{p,D,ob}$) of the output bridge have an equal peak value. It is given by (3.3) in DCM and by (3.14) in CCM, and therefore its plot as a function of I_o is still given by Fig. 3.8.

3.2.8 Device average currents

Looking the Figs. 3.11 (a)-(b), in DCM the average currents in the transistors of the leg 1-2 and in the diodes of the leg 3-4 of the input bridge are calculated in

$$I_{av,T,ib,DCM} = \left[\alpha\frac{i_L(\alpha)}{2} + (\beta-\alpha)\frac{i_L(\alpha)}{2}\right]\frac{1}{2\pi} = \frac{\pi V_i}{4\omega L}\frac{\alpha^2}{\pi^2}\left(\frac{V_i}{V_o}-1\right) \quad (3.37)$$

$$I_{av,D,ib,DCM} = (\beta-\alpha)\frac{i_L(\alpha)}{2}\frac{1}{2\pi} = \frac{V_i}{\omega L}\frac{\pi}{4}\frac{\alpha^2}{\pi^2}\left(1-\frac{V_o}{V_i}\right)\left(\frac{V_i}{V_o}-1\right) \quad (3.38)$$

whilst, looking the Figs. 3.11 (c)-(d), they are calculated in

$$I_{av,T,ib,CCM} = \left\{i_L(\alpha)\frac{(\alpha-\varphi)}{2} + [-i_L(0)+i_L(\alpha)]\frac{(\pi-\alpha)}{2}\right\}\frac{1}{2\pi} =$$

$$= \frac{V_i}{\omega L}\frac{\pi}{16}\left[\left(1-\frac{V_o}{V_i}\right)\left(\frac{\alpha}{\pi}+\frac{V_o}{V_i}\right)^2 + 4\left(\frac{\alpha}{\pi}-\frac{{V_o}^2}{{V_i}^2}\right)\left(1-\frac{\alpha}{\pi}\right)\right] \quad (3.39)$$

$$I_{av,D,ib,CCM} = \left\{-\frac{i_L(0)}{2}\varphi + [-i_L(0)+i_L(\alpha)]\frac{(\pi-\alpha)}{2}\right\}\frac{1}{2\pi}$$

$$= \frac{V_i}{\omega L}\frac{\pi}{16}\left[\left(1+\frac{V_o}{V_i}\right)\left(\frac{\alpha}{\pi}-\frac{V_o}{V_i}\right)^2 + 4\left(\frac{\alpha}{\pi}-\frac{{V_o}^2}{{V_i}^2}\right)\left(1-\frac{\alpha}{\pi}\right)\right] \quad (3.40)$$

Eqs. (3.37) -(3.40) are plotted in Fig.3.12 as a function of I_o.

The average currents in the diodes of the output bridge is simply equal to half of I_o, where I_o is given respectively by (3.6) in DCM and by (3.16) in CCM.

3.2.9 Device rms currents

Looking the Fig. 3.11 (a), in DCM the rms current in the transistors of the leg 1-2 of the input bridge, considering the two areas, is calculated as following.

1)

$$\frac{\theta-0}{\alpha-0} = \frac{i_L(\theta)-0}{i_L(\alpha)-0} \Rightarrow \quad i_L(\theta) = i_L(\alpha)\frac{\theta}{\alpha}$$

$$\int_0^{\alpha} i_L(\theta)^2\, d\theta = i_L(\alpha)^2\frac{\alpha}{3} \quad (3.41)$$

2)

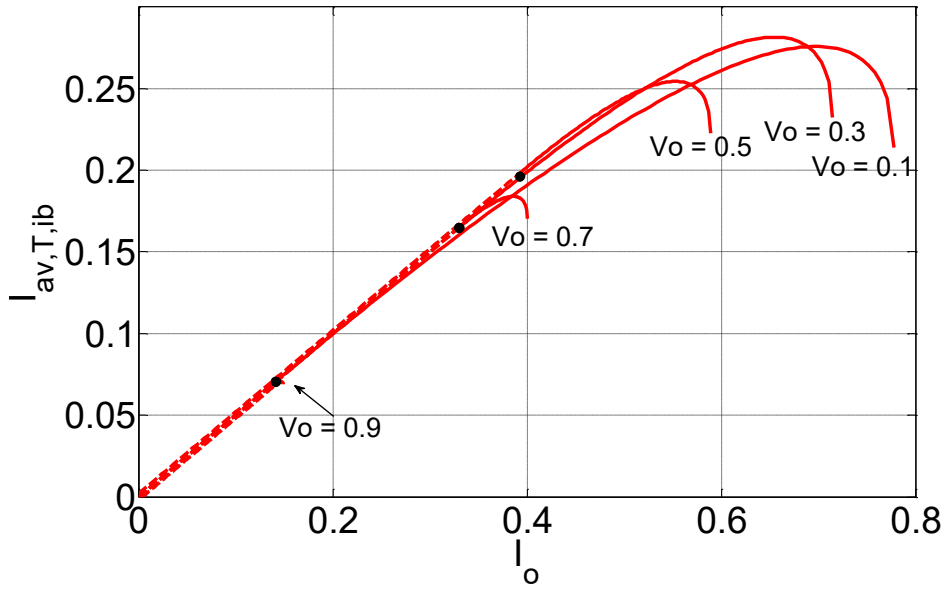
$$\frac{\theta-\alpha}{\beta-\alpha} = \frac{i_L(\theta)-i_L(\alpha)}{0-i_L(\alpha)} \quad \Rightarrow \quad i_L(\theta) = i_L(\alpha) - i_L(\alpha)\frac{\theta-\alpha}{\beta-\alpha}$$

$$i_L(\theta)^2 = i_L(\alpha)^2 + i_L(\alpha)^2\frac{(\theta-\alpha)^2}{(\beta-\alpha)^2} - 2i_L(\alpha)^2\frac{\theta-\alpha}{\beta-\alpha}$$

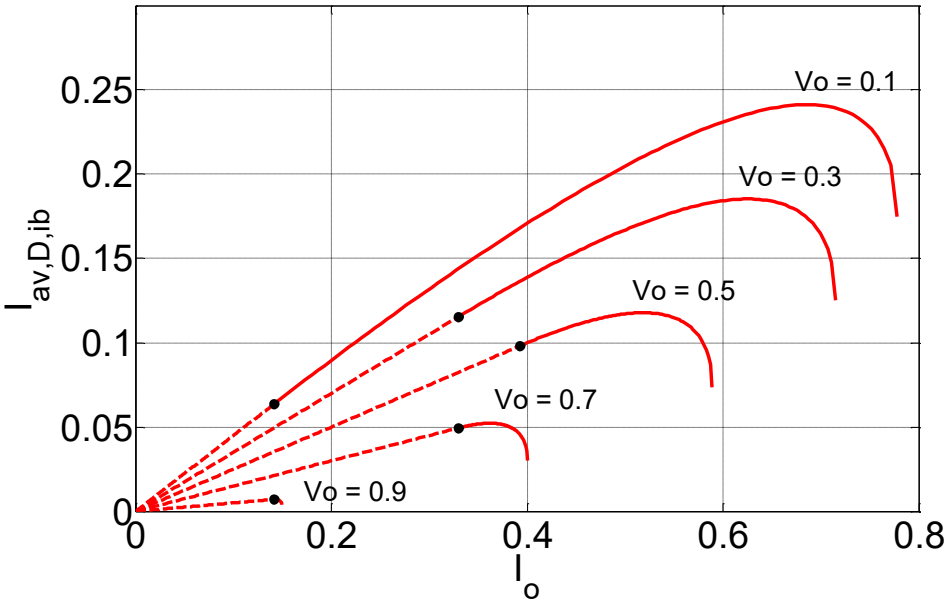
$$\int_{\alpha}^{\beta} i_L(\theta)^2\, d\theta = i_L(\alpha)^2\frac{\beta-\alpha}{3} \quad (3.42)$$

From the eqs. (3.41) and (3.42) the rms current in T_1 or T_2 is

$$I_{rms,T,ib,DCM} = \sqrt{\frac{1}{6}i_L(\alpha)^2\frac{\beta}{\pi}} \quad (3.43)$$



(a)



(b)

Fig. 3.12. SAB converter average current in the transistors of the leg 1-2 (a) and in the diodes of the leg 3-4 of the input bridge (b) vs. load current.

Looking the Fig. 3.11 (b), in DCM the rms current in the diodes of the leg 3-4 of the input bridge is calculated as following.

$$\frac{\theta-\alpha}{\beta-\alpha} = \frac{i_L(\theta)-i_L(\alpha)}{0-i_L(\alpha)} \quad \Rightarrow \quad i_L(\theta) = i_L(\alpha) - i_L(\alpha)\frac{\theta-\alpha}{\beta-\alpha}$$

$$i_L(\theta)^2 = i_L(\alpha)^2 + i_L(\alpha)^2\frac{(\theta-\alpha)^2}{(\beta-\alpha)^2} - 2i_L(\alpha)^2\frac{\theta-\alpha}{\beta-\alpha}$$

$$\int_\alpha^\beta i_L(\theta)^2\, d\theta = i_L(\alpha)^2\frac{\beta-\alpha}{3}$$

$$I_{rms,D,ib,DCM} = \sqrt{\frac{1}{6} i_L(\alpha)^2 \left(\frac{\beta}{\pi} - \frac{\alpha}{\pi}\right)} \quad (3.44)$$

Looking the Fig. 3.11 (c), in CCM the rms current in the transistors of the leg 1-2 of the input bridge, considering the two areas is calculated as following.

1)

$$\frac{\theta-\varphi}{\alpha-\varphi} = \frac{i_L(\theta)-0}{i_L(\alpha)-0} \Rightarrow \quad i_L(\theta) = i_L(\alpha)\frac{\theta-\varphi}{\alpha-\varphi}$$

$$\int_{\varphi}^{\alpha} i_L(\theta)^2 \, d\theta = i_L(\alpha)^2 \frac{\alpha-\varphi}{3} \quad (3.45)$$

2)

$$\frac{\theta-\alpha}{\pi-\alpha} = \frac{i_L(\theta)-i_L(\alpha)}{-i_L(0)-i_L(\alpha)} \Rightarrow \quad i_L(\theta) = i_L(\alpha) - [i_L(0) + i_L(\alpha)]\frac{\theta-\alpha}{\pi-\alpha}$$

$$i_L(\theta)^2 = i_L(\alpha)^2 + [i_L(0) + i_L(\alpha)]^2 \frac{(\theta-\alpha)^2}{(\pi-\alpha)^2} - 2i_L(\alpha)[i_L(0) + i_L(\alpha)]\frac{(\theta-\alpha)}{(\pi-\alpha)}$$

$$\int_{\alpha}^{\pi} i_L(\theta)^2 \, d\theta = i_L(\alpha)^2(\pi-\alpha) + [i_L(0) + i_L(\alpha)]^2 \frac{(\pi-\alpha)}{3} - i_L(\alpha)[i_L(0) + i_L(\alpha)](\pi-\alpha) \quad (3.46)$$

From the eqs. (3.45) and (3.46) the rms current in T_1 or T_2 is

$$I_{rms,T,ib,CCM} = \sqrt{\frac{1}{6}\left[\Lambda_{SAB} - \frac{\varphi}{\pi} i_L(\alpha)^2\right]} \quad (3.47)$$

where

$$\Lambda_{SAB} = i_L(\alpha)^2 + i_L(0)^2\left(1 - \frac{\alpha}{\pi}\right) - i_L(\alpha)i_L(0)\left(1 - \frac{\alpha}{\pi}\right)$$

Looking the Fig. 3.11 (d), in CCM the rms current in the diodes of the leg 3-4 of the input bridge, considering the two areas, is calculated as following.

1)

$$\frac{\theta-\alpha}{\pi-\alpha} = \frac{i_L(\theta)-i_L(\alpha)}{-i_L(0)-i_L(\alpha)} \Rightarrow \quad i_L(\theta) = i_L(\alpha) - [i_L(0) + i_L(\alpha)]\frac{\theta-\alpha}{\pi-\alpha}$$

$$i_L(\theta)^2 = i_L(\alpha)^2 + [i_L(0) + i_L(\alpha)]^2 \frac{(\theta-\alpha)^2}{(\pi-\alpha)^2} - 2i_L(\alpha)[i_L(0) + i_L(\alpha)]\frac{(\theta-\alpha)}{(\pi-\alpha)}$$

$$\int_{\alpha}^{\pi} i_L(\theta)^2 \, d\theta = i_L(\alpha)^2(\pi-\alpha) + [i_L(0) + i_L(\alpha)]^2 \frac{(\pi-\alpha)}{3} - i_L(\alpha)[i_L(0) + i_L(\alpha)](\pi-\alpha) \quad (3.48)$$

2)

$$\frac{\theta-\pi}{\pi+\varphi-\pi} = \frac{i_L(\theta)+i_L(0)}{0+i_L(0)} \Rightarrow \quad i_L(\theta) = -i_L(0) + i_L(0)\frac{\theta-\pi}{\varphi}$$

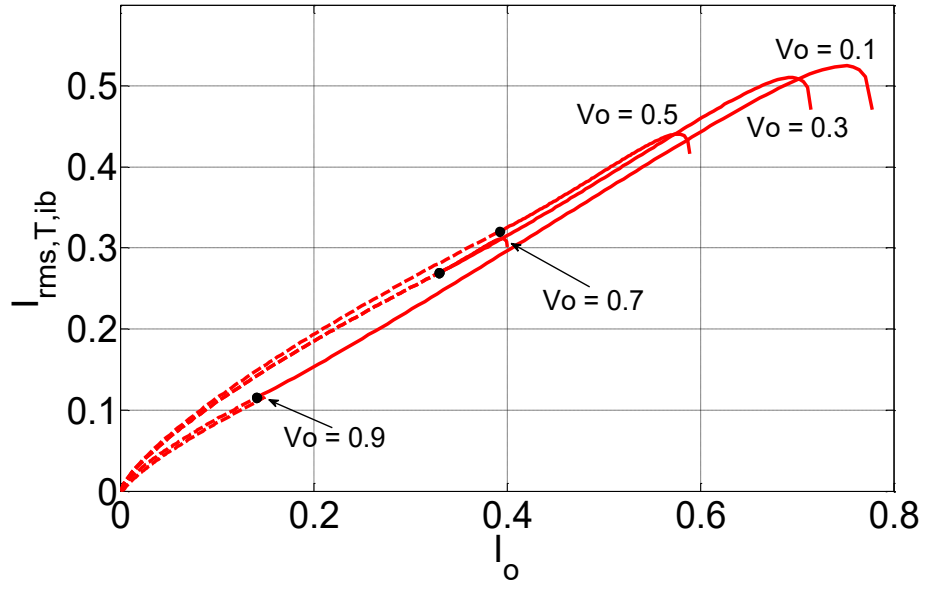
$$i_L(\theta)^2 = i_L(0)^2 + i_L(0)^2 \frac{(\theta-\pi)^2}{\varphi^2} - 2i_L(0)^2 \frac{\theta-\pi}{\varphi}$$

$$\int_{\pi}^{\pi+\varphi} i_L(\theta)^2 \, d\theta = i_L(0)^2 \frac{\varphi}{3} \quad (3.49)$$

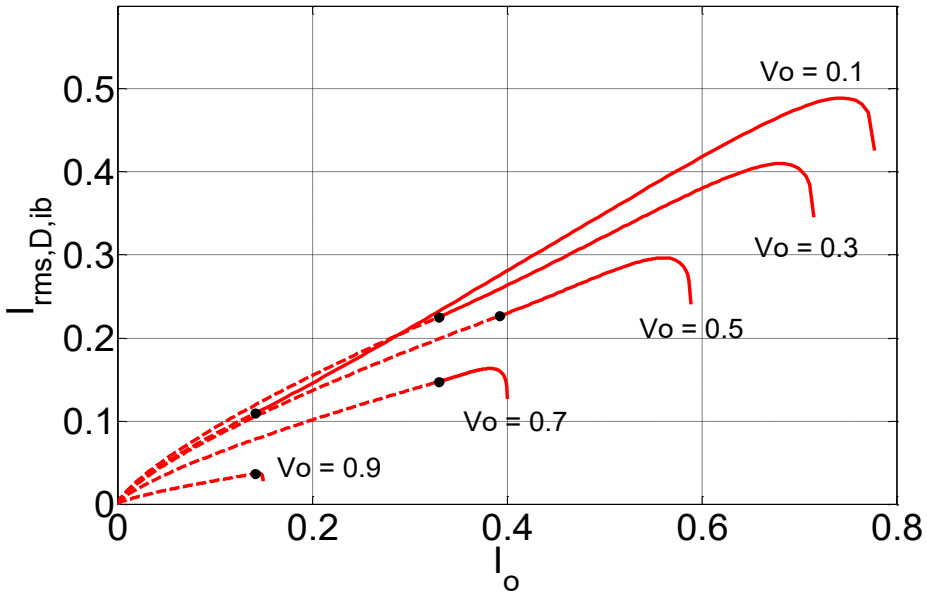
From the eqs. (3.48) and (3.49) the rms current in D_3 or D_4 is

$$I_{rms,D,ib,CCM} = \sqrt{\frac{1}{6}\left[\Lambda_{SAB} - \frac{\alpha}{\pi} i_L(\alpha)^2 + \frac{\varphi}{\pi} i_L(0)^2\right]} \quad (3.50)$$

Eqs. (3.43), (3.44), (3.47) and (3.50) are plotted in Fig.9 as a function of I_o.



(a)



(b)

Fig. 3.13. SAB converter rms current in the transistors of the leg 1-2 and in diodes of the leg 3-4 of the input bridge vs. load current.

3.3 Soft-switching capabilities

Considering that operation at high-switching frequency of the isolated DC-DC converter is the key to shrink SST volume and weight, the need of commutating softly its switches is crucial to improve the efficiency. Soft-switching is the technique by which the switching losses of a switch are greatly reduced by commutating it either at zero voltage or at zero current; the relevant techniques are termed zero voltage switching (ZVS) and zero current switching (ZCS), respectively. Soft-switching is commonly attained by the insertion of additional active and/or passive elements in the converter circuitry [41]-[43]. In the analytical analysis of this thesis, the soft-switching is implemented using capacitors connected in parallel to the switches.

The circuitry of the SAB converter is redrawn in Fig. 3.14 including soft-switching capacitors; waveforms of current and voltage for DCM and CCM are drawn in Figs. 3.15 (a) and (b), derived from Figs. 3.2 and 3.3, respectively.

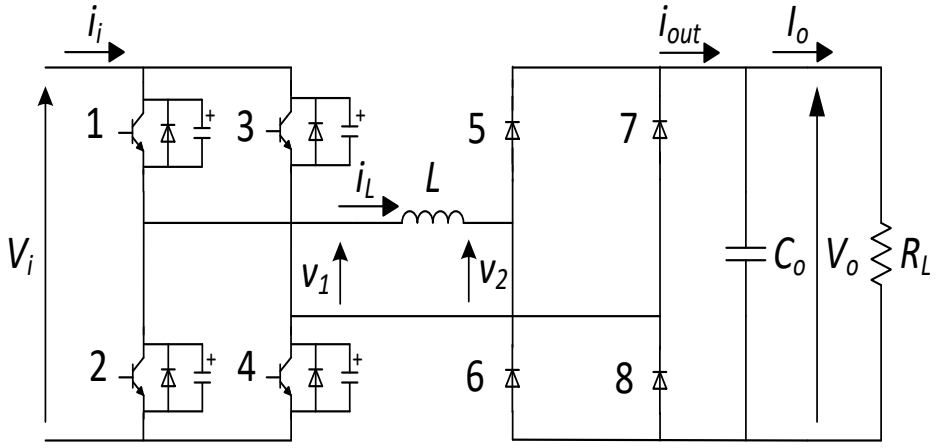


Fig. 3.14. SAB converter circuitry with soft-switching capacitors.

In the SAB converter the soft-switching capacitors can be inserted in the input bridge in two ways. In case#1 the capacitors are inserted only in one leg whilst in case#2 they are inserted in both the legs. Case#1, in turn, allows for two possibilities, namely case#1(a), with the capacitors inserted in leg 1-2, commonly termed as leading leg, and case#1(b), with the capacitors inserted in leg 3-4, commonly termed as lagging leg.

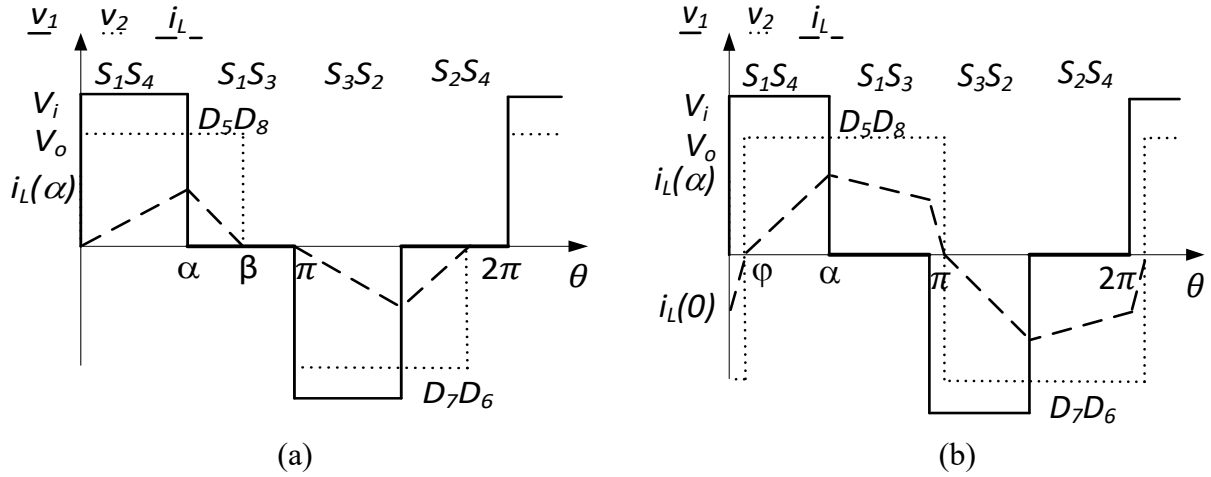


Fig. 3.15. SAB current and voltage waveforms in (a) DCM, (b) in CCM.

3.3.1 DCM

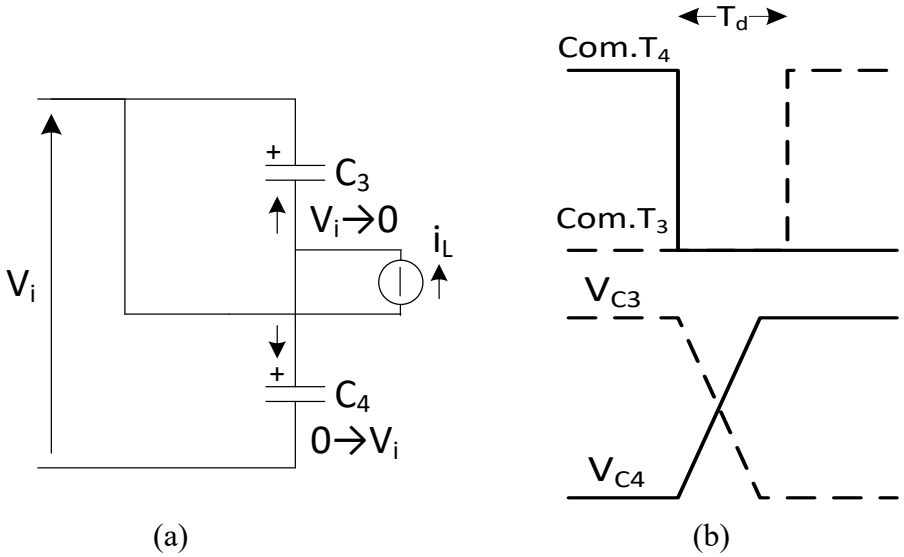
Let us consider the two cases in DCM. For a SAB converter operating in DCM, the angle β where the current i_L vanishes is less than π. Then, the current is zero for an interval π-β during each half period.

Case#1(a)

In this case the capacitors are inserted in the leading leg. Just before $\theta = 0$, there is no current in the input bridge and T_2 is commanded in the on-state while T_1 is in the off-state. The voltages across C_1 and C_2 are V_i and 0, respectively. At $\theta = 0$, T_2 is turned off and its commutation is soft of Zero Current Switching (ZCS) type because it is not flown by any current. At the end of the dead-time, C_1 is still charged and the turn-on of T_1 short-circuits it, giving rise to an unacceptable pulse of current trough T_1. The same problem occurs at $\theta = \pi$ for T_2. Hence, the insertion of capacitors in the leading leg is not feasible.

Case#1(b)

In this case the capacitors are inserted in the lagging leg. At $\theta = 0$, the same situation as in case#1(a) occurs for T_2 and then its commutation is soft. At the end of the dead-time, T_1 is turned on and its commutation is hard since a voltage equal to half of V_i is dropping across it. At $\theta = \alpha$, T_4 is turned off and its commutation is soft of Zero Voltage Switching (ZVS) type thanks to C_4 that is discharged at that time and keeps voltage across T_4 near to zero during the commutation. During the dead-time, C_4 charges at V_i while C_3, which at $\theta = \alpha$ was charged at V_i, discharges. At the end of the dead-time, T_3 is turned on and its commutation is of ZVS type because the current is flowing through diode D_3 so that voltage across T_3 is already zero. Current flow and voltage transients across the capacitors are shown in Figs. 3.16 (a) and (b). The commutations at $\theta = \pi$ and at $\theta = \pi + \alpha$ occur with the same mechanism as at $\theta = 0$ and at $\theta = \alpha$.



(a) (b)

Fig. 3.16. (a) current flow and (b) voltage transients across the capacitors during the dead-time at $\theta = \alpha$.

Case#2

In this case the capacitors are inserted in parallel to each switch. The situation at $\theta = 0$ is identical to case#1(a). Turn-off of T_2 is of ZCS type but the successive turn-on of T_1 produces an unacceptable

pulse of current through it due to the discharge of C_1. The same problem occurs at $\theta = \pi$ for T_2. Hence, the insertion of capacitors in parallel to each switch is not feasible.

As a result, soft-switching of the SAB converter operating in DCM can be obtained with the insertion of capacitors only in the lagging leg, i.e. with case#1(b). Furthermore, soft-switching is incomplete as only the switches in the leg endowed with the capacitors experience soft commutations at both turn-on and turn-off. Transistor commutation and their type of switching in DCM for case#1(b) are summarized in Tab. I.

Tab. I. DCM switching for case#1(b)

	θ=0	θ=α	θ=π	θ=π+α
Turn on	T_1 HARD	T_3 ZVS	T_2 HARD	T_4 ZVS
Turn off	T_2 ZCS	T_4 ZVS	T_1 ZCS	T_3 ZVS

3.3.2 CCM

Let us consider the two cases in CCM. For a SAB converter operating in CCM, the current i_L is zero only for the instant when it changes direction.

Case#1(a)

In this case, the capacitors are inserted in the leading lag. At $\theta = 0$, T_2 is turned off and its switching is soft thanks to capacitor C_2 that is discharged. At the end of the dead-time, T_1 is turned on and its switching is soft because diode D_1 is already conducting. At $\theta = \alpha$, T_4 is turned off and its switching is hard because the voltage across it jumps to V_i while the current is still flowing through it. At the end of the dead-time, T_3 is turned on and its switching is soft because the the diode D_3 is already conducting. The commutations at $\theta = \pi$ and at $\theta = \pi + \alpha$ occur with the same mechanism as at $\theta = 0$ and at $\theta = \alpha$. Hence, the insertion of capacitors in the leading leg allows for a soft turn-on of all the switches but not for a soft turn-off of T_3 and T_4. Transistor commutation and their type of switching in CCM for case#1(a) are summarized in Tab. II.

Tab. II. CCM switching for case#1(a)

	θ=0	θ=α	θ=π	θ=π+α
Turn on	T_1 ZVS	T_3 ZVS	T_2 ZVS	T_4 ZVS
Turn off	T_2 ZVS	T_4 HARD	T_1 ZVS	T_3 HARD

Case#1(b)

In this case the capacitors are inserted in the lagging leg. By duality with respect to case#1(a), it turns out that the insertion of capacitors in the lagging leg allows for a soft turn-on of all the switches but not for a soft turn-off of T_1 and T_2. Transistor commutations and their type of switching in CCM for case#1(b) are summarized in Tab. III.

Tab. III. CCM switching for case#1(b)

	$\theta=0$	$\theta=\alpha$	$\theta=\pi$	$\theta=\pi+\alpha$
Turn on	T_1 ZVS	T_3 ZVS	T_2 ZVS	T_4 ZVS
Turn off	T_2 HARD	T_4 ZVS	T_1 HARD	T_3 ZVS

Case#2

In this case, the capacitors are inserted in parallel to each switch. At $\theta = 0$, T_2 is turned off and its switching is soft thanks to C_2. At the end of the dead-time, T_1 is turned on and its switching is soft because the diode D_1 is already conducting. At $\theta = \alpha$, T_4 is turned off and its switching is soft thanks to C_4. At the expiration of the dead-time, T_3 is turned on and its switching is soft because the diode D_3 is already conducting. The commutations at $\theta = \pi$ and at $\theta = \pi + \alpha$ occur with the same mechanism as at $\theta = 0$ and at $\theta = \alpha$. Hence the insertion of the capacitors in parallel to each switch ensures full soft-switching capabilities.

As a result, soft-switching of the SAB converter operating in CCM is obtained whether the capacitors are inserted in one leg or in both the legs. However, in the first case the soft-switching is incomplete whilst in the second case it is full.

3.3.3 Soft-switching capacitor design

When soft-switching is feasible, i) the voltage across the capacitors should stay at zero during the transistor turn-off time t_{off}, and ii) the charging to V_i should take place entirely within the dead-time T_d so that, the discharging to zero of the capacitor in parallel to the other transistor of the same leg is completed before the turn-on of the transistor. In practice, there is a certain change of voltage during t_{off}, which must be restricted at a fraction of V_i. To get this restriction, a minimum time $a \cdot t_{off}$ is fixed for the capacitor to charge from 0 to V_i, where a is a factor >1; the factor a guarantees that the increase of the capacitor voltage during t_{off} is V_i/a, under linear voltage transients.

Let us denote with T_s the capacitor voltage transients time from 0 to V_i. For both the schemes of Figs. 3.15 and 3.16 (b), the current i_L divides into two equal parts when entering into the capacitors. For a current i_L enough high, as it occurs at $\theta = \alpha$, the current can be assumed constant during T_s and the relationship between C, i_L and T_s is

$$V_i C = \frac{i_L T_s}{2} \tag{3.51}$$

A quite different situation arises when i_L is small as it occurs at $\theta = 0$ when CCM approaches DCM. In this situation, a more accurate description of the capacitor voltage transients must account for the linear behavior of i_L during T_s, and the relationship between C, i_L and T_s becomes

$$V_i C = \frac{i_L T_s}{4} \tag{3.52}$$

Let us now select a capacitor in order that, for the maximum value of $i_{L,max}$ of the current $i_L(\alpha)$, the commutation takes place in at_{off}, with a=3. Then

$$C = \frac{i_{L,max} 3 t_{off}}{2 V_i} \tag{3.53}$$

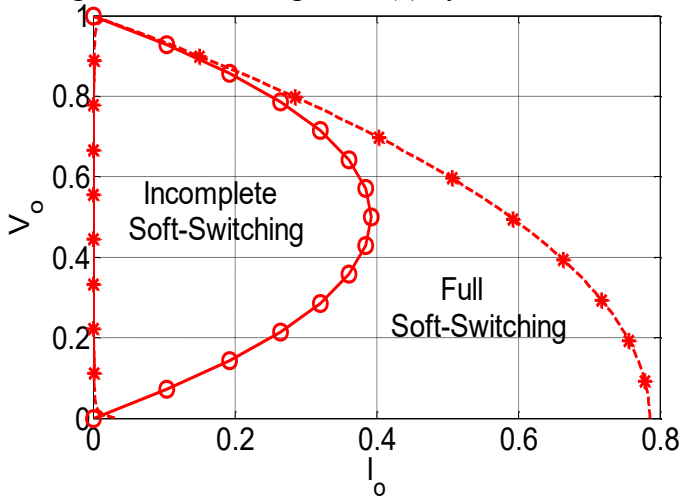
By imposing that T_s does not exceed T_d, (3.52) yields a minimum value $i_{L,min}$ of the current $i_L(\alpha)$ for the SAB converter to commutate softly. It is the minimum current that allows the charge or discharge of the capacitor within the time permitted. It is given by

$$i_{L,min} = \frac{i_{L,max} 3 t_{off}}{2 T_d} \tag{3.54}$$

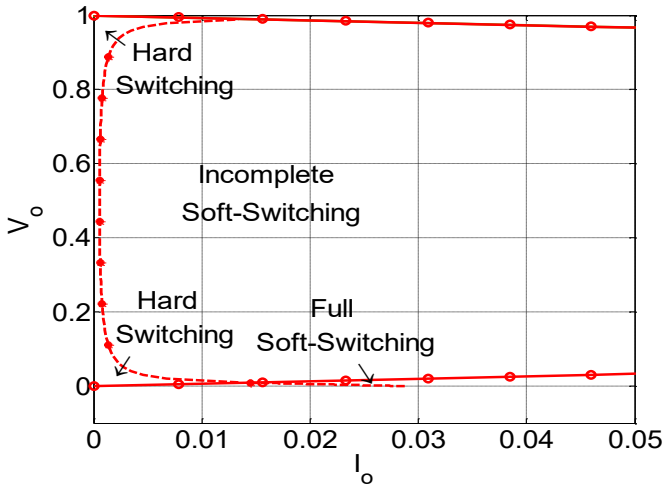
Eq. (3.54) restricts even more the incomplete soft-switching zone of the SAB converter, as shown in the Fig. 3.17 with the curve near the ordinate axis.

3.3.4 Conclusive remarks

Putting together the above findings, it comes out that admissible operation of the SAB converter is within the zone subtended by the line marked with stars in Fig. 3.17 (a). Full soft-switching is here delimited by the (3.5), which is the boundary condition between DCM and CCM (line marked with circle). Expressed in terms of output voltage, (3.5) imposes a lower limit to the load current to achieve full soft-switching. The limit is obtained by combining (3.5) with (3.6) or with (3.16), and is shown in Fig. 3.17 (a) by the line marked with rounds; below the limit, incomplete soft-switching occurs. The load current limit takes a maximum for an intermediate value of the output voltage and decreases both at high and low output voltages. Maximum load current is obtained with $\alpha=\pi$; its plot as a function of the output voltage is shown in Fig. 3.17 (a) by the line marked with stars.



(a)



(b)

Fig. 3.17. (a) SAB converter soft-switching limits; (b) magnification of the limits near Io=0.

3.4 Dynamic model

The models used for the power electronic systems are mainly classified in two types: switching models and average value models (AVMs).

The first are typically used in commercial simulators software where the models of the components, such as resistors, inductors, capacitors, diodes and transistors, can also include parasitic parameters to increase the accuracy of the simulation. The disadvantage of these models is that are not very suitable for analysis of a system in time and frequency domains [44].

The second ones are computationally more efficient because the average values in the switching period of the state variables are considered, so that the switching is removed.

The AVMs are classified in reduced-order and full-order models. The full-order models have more information in the high frequency region but are more complicated due to their higher order. The reduced-order models are simpler and maintain the main behaviour of the system. A common method used to obtain the AVMs is the state-space averaging (SSA).

The SAB is a particular type of DC-DC converter because provide the galvanic isolation between input and output using a high frequency transformer. Then an AC stage is present in the middle. The state-space averaging method can be used if the current ripple can be considered negligible with respect to its DC component [45]-[46]; consequently, the AVM is a simple method to calculate the approximated transfer functions of the SAB but others methods must be used to calculate an accurate model. For simplicity in this thesis, the state-space averaging method is used to derive the small-signal model and calculate the transfer functions.

The circuit of the SAB converter is analysed during each switching interval. However, the analysis of only half of the waveform is necessary because the voltage waveform in the transformer is symmetrical. The transfer functions of the system are calculated for the DCM, where three intervals are present in half period, and for the CCM, where only two intervals are present.

3.4.1 DCM SAB model

Looking at Fig. 3.18 within half period three intervals t_1, t_2 and t_3 are present.

Let us consider the interval t_1. The SAB schematic for this interval is shown in Fig. 3.19 (a). Its equivalent circuit, considering a transformer ratio equal to 1 is shown in Fig. 3.19 (b).

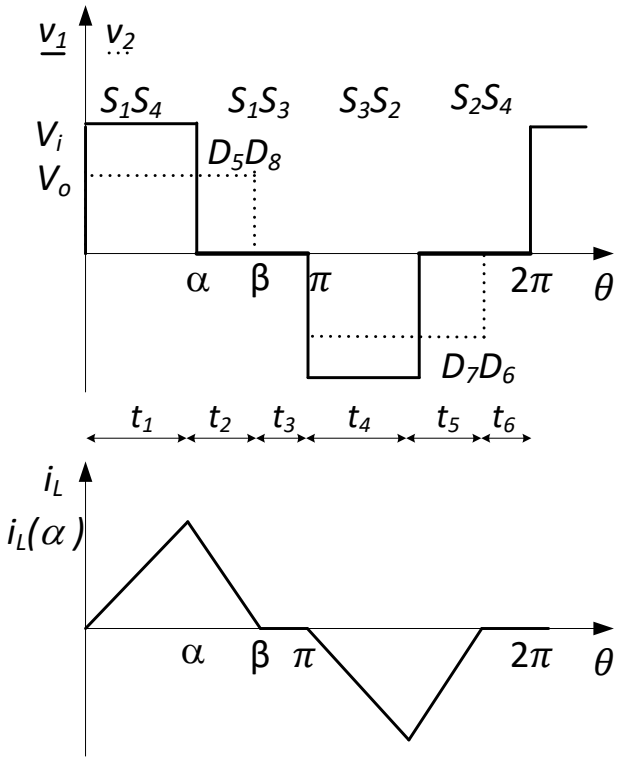
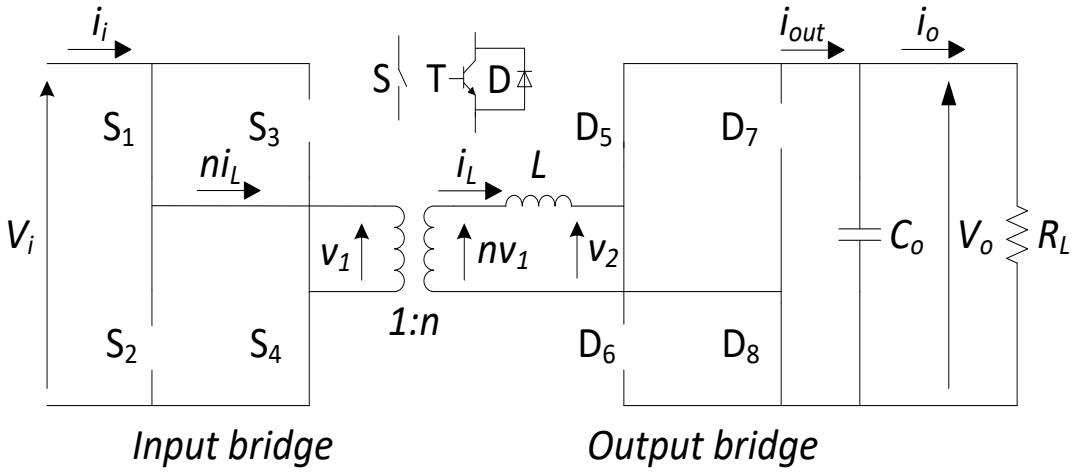
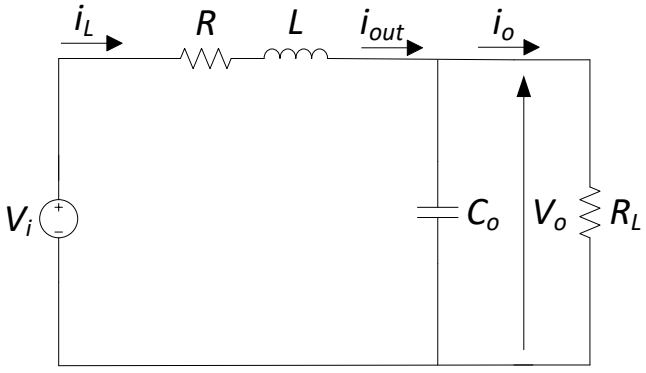


Fig. 3.18. SAB converter current and voltage waveforms in DCM



(a)



(b)

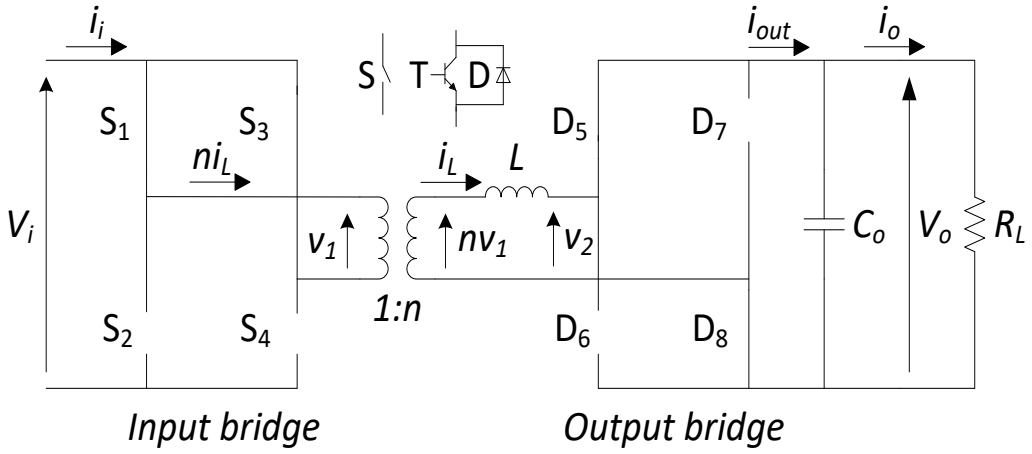
Fig. 3.19 SAB schematic (a) and its equivalent circuit (b) during the interval t_1.

Appling the Kirchhoff laws KVL and KCL to the circuit of Fig. 3.19 (b) the derived equations are:

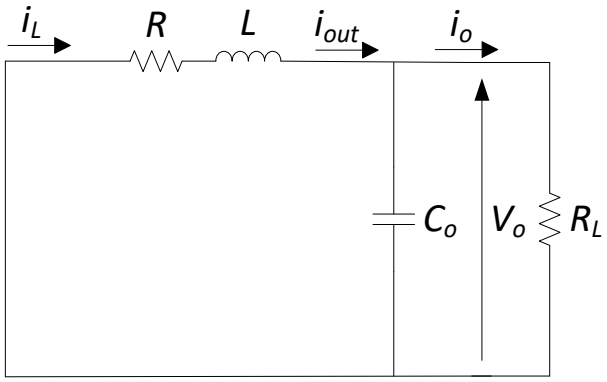
$$v_i - L\frac{di_L}{dt} - Ri_L - v_o = 0 \tag{3.55}$$

$$C_o\frac{dv_o}{dt} + \frac{v_o}{R_L} - i_L = 0 \tag{3.56}$$

Let us consider the interval t_2. The SAB schematic for this interval is shown in Fig. 3.20 (a) and its equivalent circuit is shown in Fig. 3.20 (b).



(a)



(b)

Fig. 3.20 SAB schematic (a) and its equivalent circuit (b) during the interval t_2.

The equations derived from the circuit of Fig. 3.20 (b) are:

$$L\frac{di_L}{dt} + Ri_L + v_o = 0 \tag{3.57}$$

$$C_o\frac{dv_o}{dt} + \frac{v_o}{R_L} - i_L = 0 \tag{3.58}$$

Let us consider the interval t_3. During this interval, the SAB schematic is the same of Fig. 3.20 (a) but the inductance current is zero. Therefore, the SAB equivalent circuit is composed only by the output capacitor and the load as shown in Fig. 3.21.

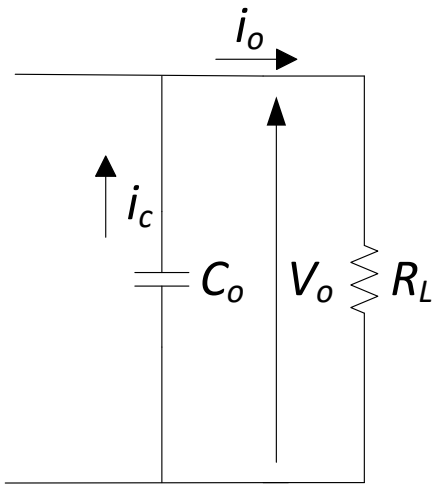


Fig. 3.21 SAB equivalent circuit during the interval t_3.

The equations derivable from the circuit of Fig. 3.21 are:

$$v_o = v_c \tag{3.59}$$

$$C_o \frac{dv_o}{dt} + \frac{v_o}{R_L} = 0 \tag{3.60}$$

The eqs. (3.55)-(3.60) can be expressed in matrix form as following. The vector with the state variables, which are the inductance current and the capacitor voltage, is indicated with x. The lowercase letter, e.g. v_i, is used to indicate the steady-state value plus a small variation. The capital letter is used to indicate the steady-state value. A bar superscript indicates the small variation value.

INTERVAL 1

$$\frac{dx}{dt} = A_1 x + B_1 v_i$$

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_o \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix}\begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_i \tag{3.61}$$

$$A_1 = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix} \qquad B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{3.62}$$

INTERVAL 2

$$\frac{dx}{dt} = A_2 x + B_2 v_i$$

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_o \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix}\begin{bmatrix} i_L \\ v_o \end{bmatrix} \tag{3.63}$$

$$A_2 = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix} \qquad B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{3.64}$$

INTERVAL 3

$$\frac{dx}{dt} = A_3 x + B_3 v_i$$

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_o \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_L C_o} \end{bmatrix}\begin{bmatrix} i_L \\ v_o \end{bmatrix} \quad (3.65)$$

$$A_3 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_L C_o} \end{bmatrix} \qquad B_3 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad (3.66)$$

The average behaviour of the circuit, using the duty cycle d, is given by

$$\frac{d}{dt}x = [A_1 d_1 + A_2 d_2 + A_3 d_3]x + [B_1 d_1 + B_2 d_2 + B_3 d_3]v_i =$$

$$= [A_1 d_1 + A_2 d_2 + A_3(1 - d_1 - d_2)]x + [B_1 d_1 + B_2 d_2 + B_3(1 - d_1 - d_2)]v_i \quad (3.67)$$

where $d_1 = \frac{t_1}{T/2} = d$, $d_2 = \frac{t_2}{T/2}$ and $d_3 = \frac{t_3}{T/2} = 1 - d_1 - d_2$

The small signal model for the SAB operating in buck mode is obtained:

- Introducing small variations of the state space variables $\tilde{x}$, independent variables $\tilde{v}$ and duty cycle $\tilde{d}$. For example, x=X+$\tilde{x}$ where the capital letter is referred to steady state.
- Separating the alternating component from the continuous component (putting equal to zero the steady state components because their derivative is zero).
- Neglecting terms containing products of small variations.

$$\frac{d}{dt}\tilde{x} = \tilde{x}[A_1 d_1 + A_2 d_2 + A_3(1 - d_1 - d_2)] + \widetilde{d_1}[(A_1 - A_3)X + V_i B_1] + \widetilde{d_2}(A_2 - A_3)X \quad (3.68)$$

$$A = A_1 d_1 + A_2 d_2 + A_3 d_3 = (A_1 - A_3)d_1 + (A_2 - A_3)d_2 + A_3 \quad (3.69)$$

$$B = B_1 d_1 + B_2 d_2 + B_3 d_3 = (B_1 - B_3)d_1 + (B_2 - B_3)d_2 + B_3 \quad (3.70)$$

$$\frac{d}{dt}\tilde{x} = A\tilde{x} + B\tilde{v} + \widetilde{d_1}[(A_1 - A_3)X + B_1 V_i] + \widetilde{d_2}[(A_2 - A_3)X] \quad (3.71)$$

Using the Laplace transform:

$$s\tilde{x} = A\tilde{x} + B\tilde{v} + \widetilde{d_1}[(A_1 - A_3)X + VB_1] + \widetilde{d_2}[(A_2 - A_3)X] \quad (3.72)$$

Then, substituting the eqs. (3.62), (3.64) and (3.66) in (3.69) and (3.70)

$$A = (A_1 - A_3)d_1 + (A_2 - A_3)d_2 + A_3 = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & 0 \end{bmatrix}(d_1 + d_2) + \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_L C_o} \end{bmatrix} \quad (3.73)$$

$$B = (B_1 - B_3)d_1 + (B_2 - B_3)d_2 + B_3 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} d_1 \quad (3.74)$$

From the coefficient matrix above calculated it is obtained eq. (3.75), where the variation of the input voltage $\tilde{v_i}$ is neglected.

$$s\begin{bmatrix}\widetilde{i_L}\\ \widetilde{v_o}\end{bmatrix}=\begin{bmatrix}-\frac{R}{L}(d_1+d_2) & -\frac{1}{L}(d_1+d_2)\\ \frac{1}{C_o}(d_1+d_2) & -\frac{1}{R_LC_o}\end{bmatrix}\begin{bmatrix}\widetilde{i_L}\\ \widetilde{v_o}\end{bmatrix}+\begin{bmatrix}-\frac{R}{L} & -\frac{1}{L}\\ \frac{1}{C_o} & 0\end{bmatrix}\left(\widetilde{d_1}+\widetilde{d_2}\right)\begin{bmatrix}i_L\\ v_o\end{bmatrix}+\begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix}V_i\widetilde{d_1} \quad (3.75)$$

$$s\widetilde{i_L}=\left(-\frac{R}{L}\widetilde{i_L}-\frac{1}{L}\widetilde{v_o}\right)(d_1+d_2)+\left(-\frac{R}{L}i_L-\frac{1}{L}v_o\right)\left(\widetilde{d_1}+\widetilde{d_2}\right)+\frac{1}{L}V_i\widetilde{d_1} \quad (3.76)$$

$$s\widetilde{v_o}=\frac{1}{C_o}(d_1+d_2)\widetilde{i_L}-\frac{1}{R_LC_o}\widetilde{v_o}+\frac{1}{C_o}\left(\widetilde{d_1}+\widetilde{d_2}\right)i_L \quad (3.77)$$

Unlike the CCM, in DCM the inductor current starts at zero at the beginning of every switching period and falls to zero before the switching period has completed. Consequently, the current in one period is not influenced by the current behaviour or command variable of the previous one; from this condition it can be deduced that in DCM the inductor current does not behave as a true state-space variable and that its dynamic equation can be reduced to a static equation introducing the constraints

$\frac{di}{dt}(T_s)=\frac{i(T_s)-i(0)}{i(T_s)}=0.$

This reduces by one the order of the basic state-space averaged model.

The output current to DC voltage transfer function is obtained from eq. (3.77) with the hypothesis that the variations of the input voltage and the duty cycle are zero ($\widetilde{v_i}=\widetilde{d_1}=\widetilde{d_2}=0$).

$$G_{v_o-i}=\frac{\widetilde{v_o}}{\widetilde{i_L}}=\frac{R_L(d_1+d_2)}{1+sR_LC_o} \quad (3.78)$$

These hypotheses are realistic because the input voltage is imposed and supposed fixed ($\widetilde{v_i}=0$); duty cycles d_1 and d_2 are computed by the control algorithm and set up at the beginning of the switching period and can not be changed until the end of the period so that their variations $\widetilde{d_1}$ and $\widetilde{d_2}$ are zero.

3.4.2 CCM SAB model

Looking at Fig. 3.22 within half period, two intervals t_1 and t_2 are present.

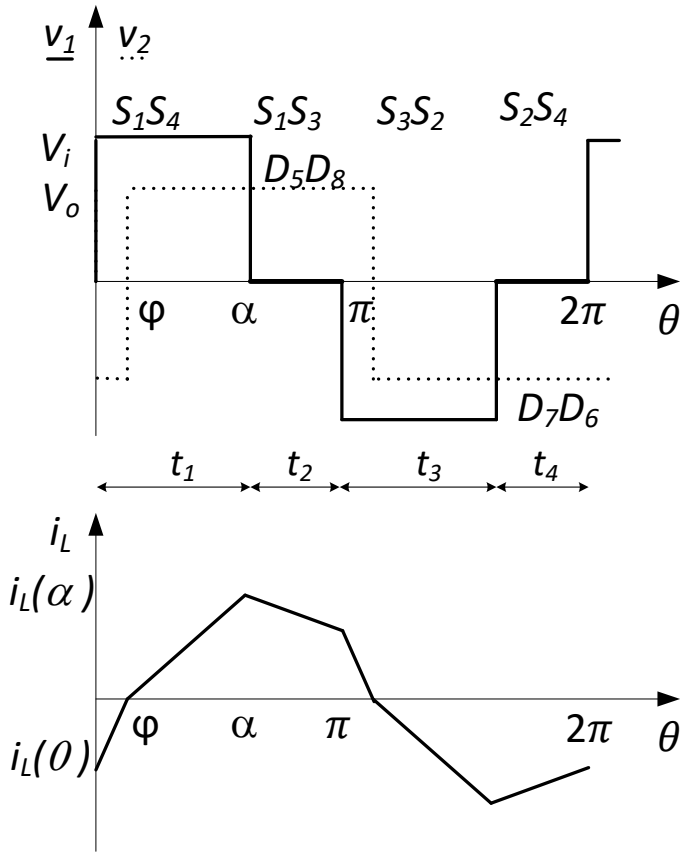


Fig. 3.22. SAB converter current and voltage waveforms in CCM

The SAB schematic and equivalent circuit for both intervals are the same of SAB in DCM operating mode and are shown in Figs. 3.19 and 3.20. Then, the equations of the equivalent circuits are (3.61)-(3.64).

The average behaviour of the circuit is given by

$$\frac{d}{dt}x = [A_1 d_1 + A_2 d_2]x + [B_1 d_1 + B_2 d_2]v_i =$$

$$= [A_1 d + A_2(1-d)]x + [B_1 d + B_2(1-d)]v_i \qquad (3.79)$$

where $d_1 = \frac{t_1}{T/2} = d$ and $d_2 = \frac{t_2}{T/2} = 1 - d_1 = 1 - d$.

As for DCM, the small signal model for the SAB operating in buck mode is obtained:

- Introducing small variations of the state space variables $\tilde{x}$, independent variables $\tilde{v}$ and duty cycle $\tilde{d}$. For example, x=X+$\tilde{x}$ where the capital letter is referred to steady state.
- Separating the alternating component from the continuous component (putting equal to zero the steady state components because their derivative is zero).
- Neglecting terms containing products of small variations.

$$\frac{d}{dt}\tilde{x} = \left[A_1 D\tilde{x} + A_1\tilde{d}X + A_2\tilde{x} - A_2 D\tilde{x} - A_2\tilde{d}X)\right] + \left[B_1 D\tilde{v} + B_1\tilde{d}V + B_2\tilde{v} - B_2 D\tilde{v} - B_2\tilde{d}V\right]$$

$$\frac{d}{dt}\tilde{x} = [A_1 D + A_2(1-D)]\tilde{x} + A_1\tilde{d}X - A_2\tilde{d}X + [B_1 D + B_2(1-D)]\tilde{v} + B_1\tilde{d}V - B_2\tilde{d}V$$

$$A = A_1 D + A_2(1 - D) \tag{3.80}$$

$$B = B_1 D + B_2(1 - D) \tag{3.81}$$

$$\frac{d}{dt}\tilde{x} = A\tilde{x} + (A_1 - A_2)X\tilde{d} + B\tilde{v} + (B_1 - B_2)\tilde{d}V$$

$$\frac{d}{dt}\tilde{x} = A\tilde{x} + B\tilde{v} + [(A_1 - A_2)X + (B_1 - B_2)V]\tilde{d}$$

Using the Laplace transformation:

$$s\tilde{x} = A\tilde{x} + B\tilde{v} + [(A_1 - A_2)X + (B_1 - B_2)V]\tilde{d} \tag{3.82}$$

Then, substituting the eqs. (3.62) and (3.64) in (3.80) and (3.81)

$$A = A_1 D + A_2(1 - D) = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix} \tag{3.83}$$

$$B = B_1 D + B_2(1 - D) = D\begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{3.84}$$

and (3.62), (3.64), (3.83) and (3.84) in (3.82) it is obtainable eq. (3.85) of the system under analysis.

$$s\begin{bmatrix} \widetilde{i_L} \\ \widetilde{v_o} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix}\begin{bmatrix} \widetilde{i_L} \\ \widetilde{v_o} \end{bmatrix} + \begin{bmatrix} D\frac{1}{L} \\ 0 \end{bmatrix}\widetilde{v_i} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_i \tilde{d} \tag{3.85}$$

$$s\widetilde{i_L} = -\frac{R}{L}\widetilde{i_L} - \frac{1}{L}\widetilde{v_o} + D\frac{1}{L}\widetilde{v_i} + \frac{1}{L}V_i\tilde{d} \tag{3.86}$$

$$s\widetilde{v_o} = \frac{1}{C_o}\widetilde{i_L} - \frac{1}{R_L C_o}\widetilde{v_o} \tag{3.87}$$

The control to output current transfer function is obtained from eq. (3.86) with the hypothesis that the variations of the input and output voltages are zero ($\widetilde{v_o} = \widetilde{v_i} = 0$).

$$G_{i-d} = \frac{\widetilde{i_L}}{\tilde{d}} = \frac{V_i}{R + sL} \tag{3.88}$$

The output current to DC voltage transfer function is obtainable from eq. (3.87) with the hypothesis that the variations of the input voltage and of the duty cycle are zero ($\widetilde{v_i} = \tilde{d} = 0$).

$$G_{v_o - i} = \frac{\widetilde{v_o}}{\widetilde{i_L}} = \frac{R_L}{1 + sR_L C_o} \tag{3.89}$$

Also in this case, these hypotheses are realistic because the current loop is much faster than voltage loop.

3.5 Simulation and experimental results

In order to realize a prototype of SST, a SAB converter prototype is realized to validate the analysis done in the previous paragraphs. The use of the SAB topologies in an SST technology assumes that the actual application requires an unidirectional power flow and only a buck operation mode. The implementation of the SAB is realized at full power in the simulation and at reduced power in the experimental setup.

3.5.1 Simulation results

The sizing specifications and the parameters of the design are listed in Tab. IV. The system is supplied by a PFC rectifier that converts the 220 Vrms AC feed into 370 Vpeak DC. The SAB output voltage is chosen to be used in a variety of applications, in particular battery chargers or light DC loads. The transformer parameters are reported in Appendix A. The inductance L is composed by the transformer leakage inductance and an extra inductance inserted in series to the primary winding to reduce the ripple current. The quantities referred to secondary side (low voltage side) of the transformer are indicated with mark ″.

TAB. IV. SAB CONVERTER PARAMETERS

Parameter	Value	Unit
V_i	370	V_{peak} DC
V''_o (referred to secondary)	60	V_{peak} DC
P_{o_max}	1	kW
f_{sw}	10	kHz
L	100u	H
C_o	1000u	F
Transformer ratio n	5.71	-
V_o (referred to primary)	343	V_{peak} DC
V_o / V_i	0.926	-

- Load resistance

$$R_o = \frac{V''_o{}^2}{P_o} = 3.6\ \Omega$$

- Output currents calculation

Considering the design specifications and the parameters, at $\alpha = \pi$, the maximum theoretical output current can be obtained by (3.16) and results in

$$I_{o,CCM,max} = \frac{V_i}{\omega L}\frac{\pi}{2}\left[\frac{\alpha}{\pi} - \frac{1}{2}\left(\frac{\alpha}{\pi}\right)^2 - \frac{1}{2}\left(\frac{V_o}{V_i}\right)^2\right] = 6.59\ A$$

$$I''_{o,CCM,max} = 37.63\ A$$

However, considering the maximum power listed in Tab. IV, the maximum current is limited to

$$I''_{out\_max\_load} = \frac{P_{out\_max}}{V_{out}} = 16.7\ A$$

$$I_{out\_max\_load} = 2.92\ A$$

that is obtained, while the SAB operates in DCM, setting α to

$$\alpha = \sqrt{\frac{\omega L}{V_i}\frac{2}{\pi}\pi^2 I_{o,DCM}\frac{1}{\left(\frac{V_i}{V_o}-1\right)}} = 1.97\ rad$$

The rms value of the alternating component of the output current in DCM is

$$I_{rms,o,DCM,max\_load} = \sqrt{\frac{1}{3} i_L(\alpha)^2 \frac{\beta}{\pi} - I_o^2} = 2.86\ A$$

$$I''_{rms,o,DCM,max\_load} = 16.3\ \text{A}$$

with $i_L(\alpha)_{max\_load} = 8.59\ A$ and $\beta = 2.13$ rad.

The peak-to-peak output current ripple R_{o,DCM,max_load} in DCM is equal to $i_L(\alpha)_{max\_load}$ (referred to primary).

- Input current calculation

The average value I_i of the input current

$$I_{i,max\_load} = \frac{V_o}{V_i} I_{o,max\_load} = 2.7\ A$$

The rms value of the alternating component of the input current is

$$I_{rms,i,DCM,max\_load} = \sqrt{\frac{1}{3} i_L(\alpha)_{max\_load}^2 \frac{\alpha}{\pi} - I_{i,max\_load}^2} = 2.85\ A$$

The peak-to-peak ripple R_i of the input current is the same as the output current.

- Devices current calculation

The average currents in the transistors of the leg 1-2 and in the diodes of the leg 3-4 of the input bridge are

$$I_{av,T,ib,DCM,max\_load} = \left[\alpha \frac{i_L(\alpha)_{max\_load}}{2} + (\beta - \alpha) \frac{i_L(\alpha)_{max\_load}}{2}\right] \frac{1}{2\pi} = 1.457\ \text{A}$$

$$I_{av,D,ib,DCM,max\_load} = (\beta - \alpha) \frac{i_L(\alpha)_{max\_load}}{2} \frac{1}{2\pi} = 0.109\ A$$

The rms current in the transistors of the leg 1-2 and diodes of the leg 3-4 of the input bridge are

$$I_{rms,T,ib,DCM,max\_load} = \sqrt{\frac{1}{6} i_L(\alpha)_{max\_load}^2 \frac{\beta}{\pi}} = 2.89\ A$$

$$I_{rms,D,ib,DCM,max\_load} = \sqrt{\frac{1}{6} i_L(\alpha)_{max\_load}^2 \left(\frac{\beta}{\pi} - \frac{\alpha}{\pi}\right)} = 0.79\ A$$

- PI controller coefficients calculation

For the calculation of the PI controller coefficient of the current and voltage loops the bandwidths are set $f_{BWi} = 500\ Hz$ and $f_{BWv} = 30\ Hz$, and the phase margin $m_\varphi = 70°$. In the calculation of the current loop parameters it is also considered the output current 2nd order low pass filter whose parameters are

$$K_f = 1 \qquad f_{cut-off} = 2000\ Hz \qquad \xi = 0.7$$

It has the function to filter out the alternating part of the output current to improve the control performance. Indeed, the current sensor has been inserted upstream the output capacitor in order to be able to maintain the control of the system and to prevent excessive current in the devices also when the load is disconnected, as shown in Fig. 3.23. The choice of the cut-off frequency must be done considering the sampling frequency.

The parameters used are:

$$K_i = 0.798e-3 \qquad t_i = 0.225\ ms \qquad K_v = 0.334 \qquad t_i = 0.0519$$

The power and control circuits implemented in the simulation are shown in Fig. 3.23; the component used in the simulation are ideal. In the software of simulation PSIM, if the output of a PI block is connected to a limiter, the anti-windup is implemented automatically.

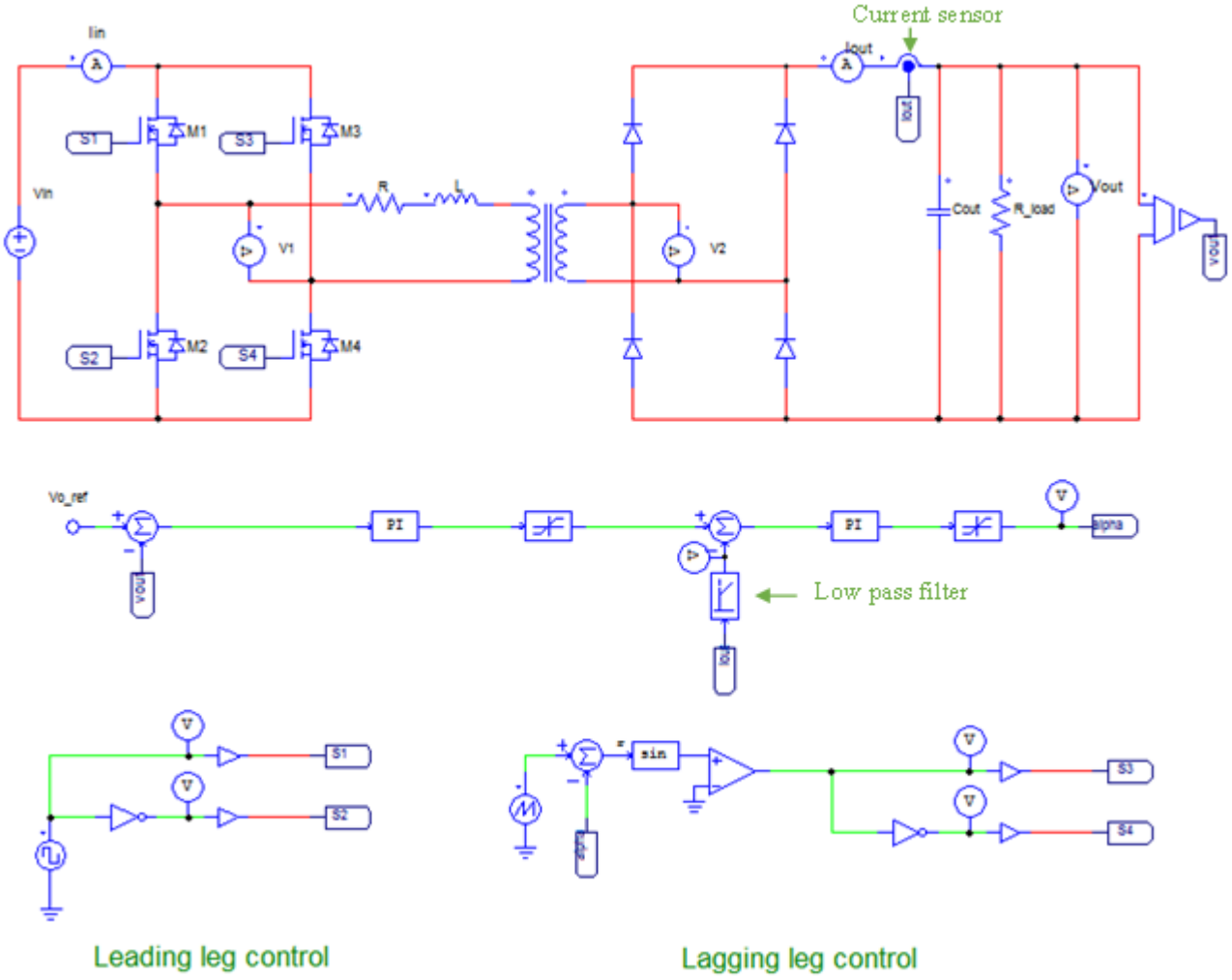
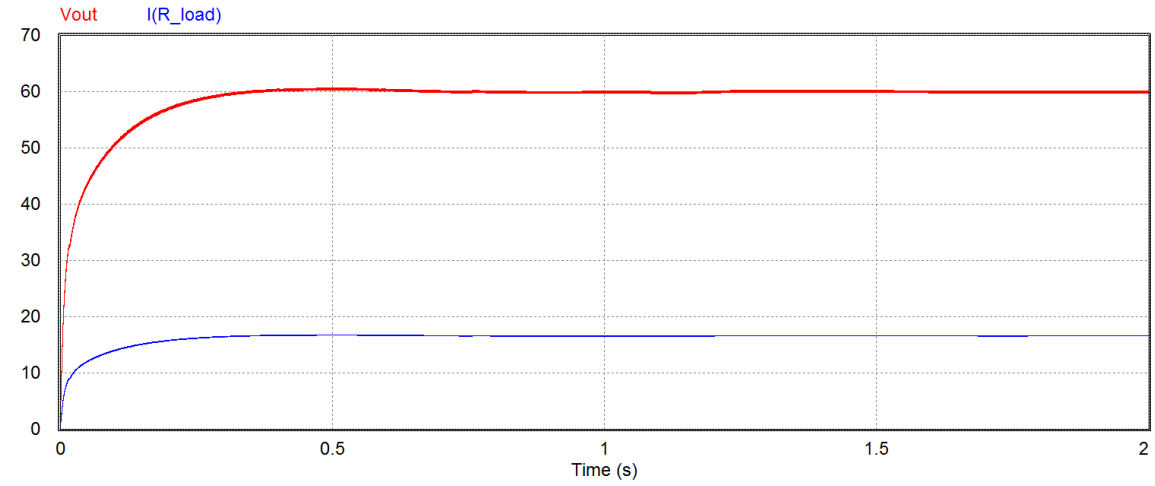
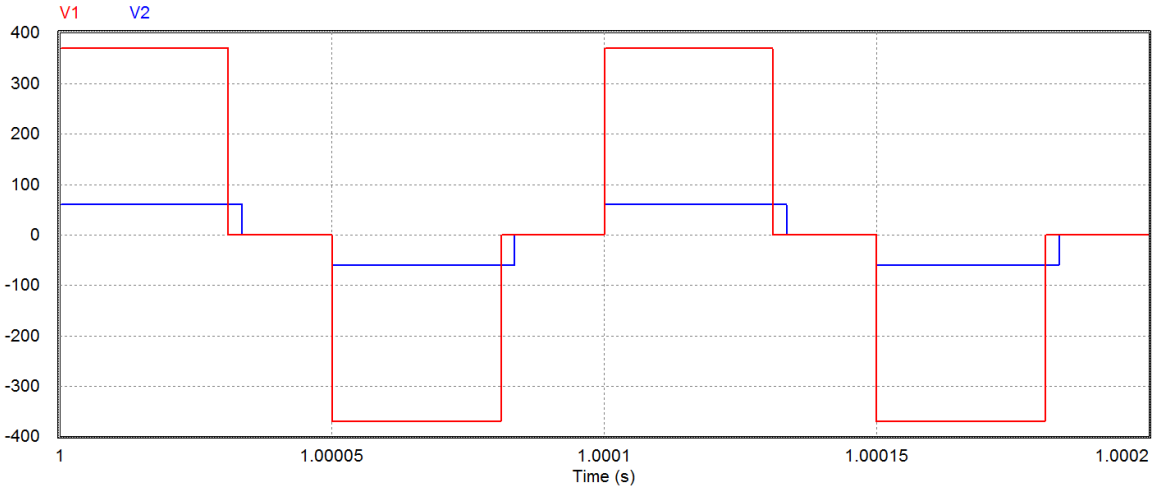


Fig.3.23 SAB power and control circuits

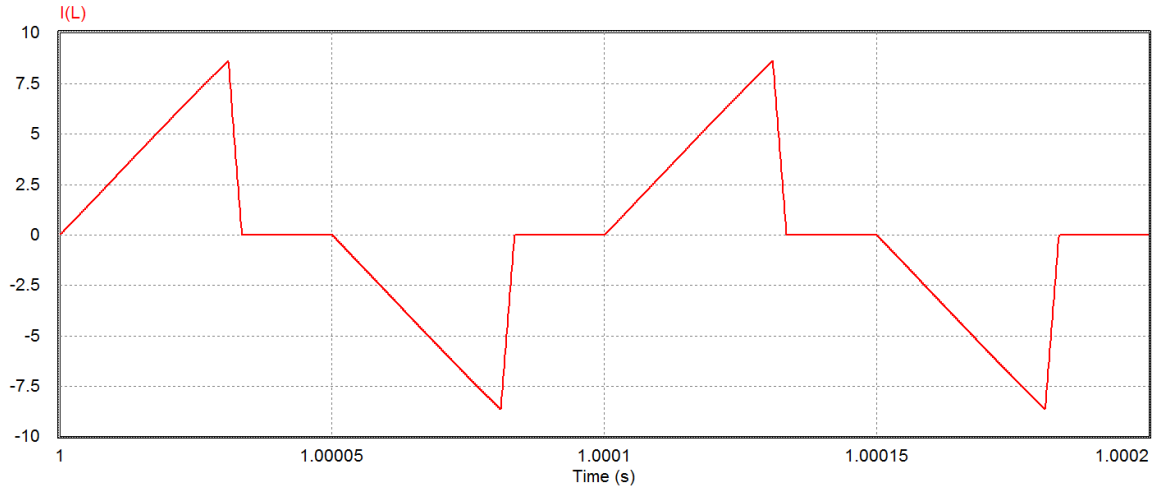
The results of the simulation are reported in Figs. 3.24 and 3.25. Fig.3.24(a) shows the output voltage and current and highlights that the control operates properly. Fig. 3.24(b) and (c) show the voltages applied to the transformer and inductance and the inductance current referred to primary. The input, output and inductance currents are shown in Fig.3.25. In conclusion, the simulation results validate the analytical analysis done in the previous paragraphs.



(a)



(b)



(c)

Fig.3.24 (a) Output voltage and current, (b) voltages before (V1) and after (V2) the high frequency transformer and added inductance (c) inductance current.

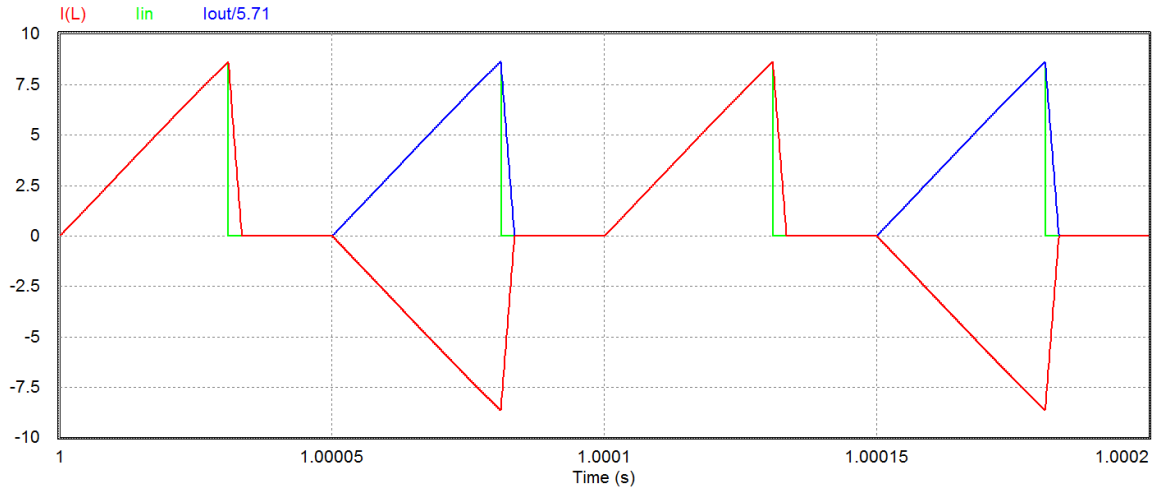


Fig.3.25 Input current (green), inductance current (red) and output current referred to primary(blue).

3.5.2 Experimental results

The experimental setup of the SAB converter is realized at reduced power scale. The printed circuit board (PCB) of the active and passive bridge are designed using the software Design Spark. The current sensor LTSP 25-NP manufactured by LEM is used to measure the inductance current. The switches used in the active bridge are the MOSFET STP35N65M5 produced by STMicroelectronics. The diodes used in the passive bridge are the diode VS-HFA30TA60C-N3 produced by Vishay. Voltage and current rating of MOSFET reported in the data sheet are 650 V and 27 A (continuously), while the diode has 600 V and 30 A. The MOSFET drivers used are the Dual MOSFET driver NCP5304PG produced by ON semiconductor. The isolation between the bridges and the control circuit is guarantee using the isolation amplifier MAX942CPA produced by Broadcom, the isolated dc-dc converters V_{in} 5V-V_{out} 5V (RBE-0505S) and V_{in} 5V-V_{out} 15V (RE-0515S) produced by RECOM, and the Optocoupler HCPL-7721-000E produced by Broadcom. The high frequency transformer used is the same three winding transformer used for the three port converter experiments reported in chapter 5. For the SAB experiments only two windings are connected. The active bridge is connected to one of the high voltage winding (400V) and the passive bridge to the low voltage winding (70V); the other high voltage winding is left open. The turn ratio between the high and the low voltage windings is 5.71. The inductance measured at low voltage winding with the high voltage winding short-circuited is around 1.55uH. Considering the high value of the magnetizing inductance this can be considered equal to the leakage inductance. To contain the current peak, an inductance of 1.22uH is added in series to the low voltage winding of the transformer. The inductance has been inserted in low voltage winding because in order to prevent the secondary current from reaching zero before the primary current when the voltage V_1 is zero: this condition leads to the circulation of a residual primary current with a slope dictated by the magnetizing inductance and hence very small. The unique disadvantage of connecting the additional inductance to the secondary winding is that its parasitic resistance is multiplied by n^2 when it is reflected to the primary of the transformer. After the connection of the additional inductance, the total inductance is 2.77 uH referred to secondary (low voltage side) and around 92 uH referred to primary side (high voltage side), and the total parasitic resistance 0.041 Ω referred to secondary and 1.31 Ω referred to primary. Two electrolytic capacitors of 1000 uF, 450 Vcc produced by EPCOS, are used at the output and input DC side. The system is fed using a PFC rectifier connected to the grid through a VARIAC and an isolation transformer. The

control algorithm is implemented using the Digital Signal Processor (DSP) TMS320F28335 produced by Texas Instruments. The integrated development environment Code Composer Studio (CCS) v6, which is provided by Texas Instruments, is used for the development of the firmware and the programming of the processor. The soft switching capacitors have been used only in the tests relevant to the TPC because for the operating conditions under test the inherent capitance of the freewheeling diodes are enough to obtain the required performance. The experimental setup of the SAB prototype is shown in Fig. 3.26.

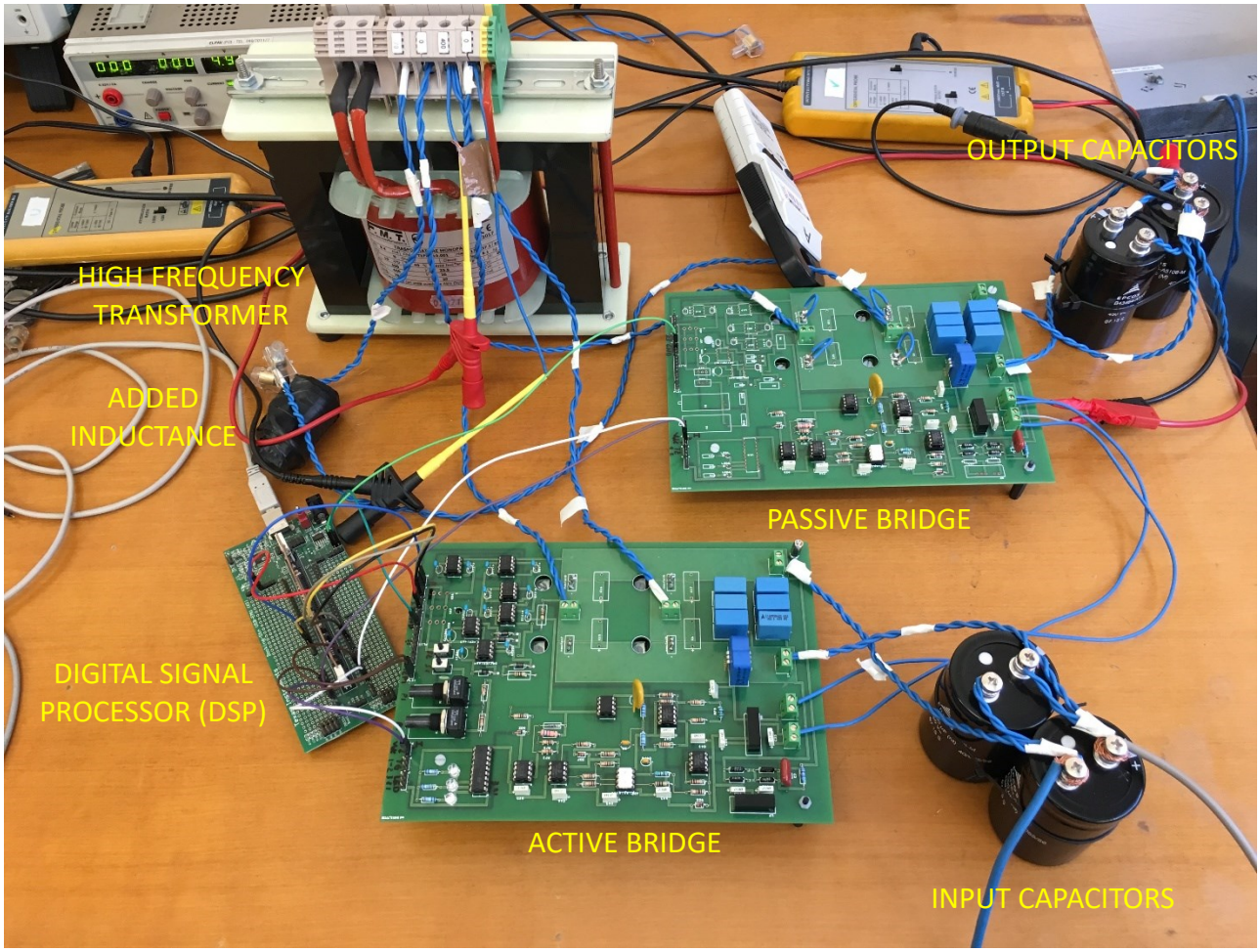
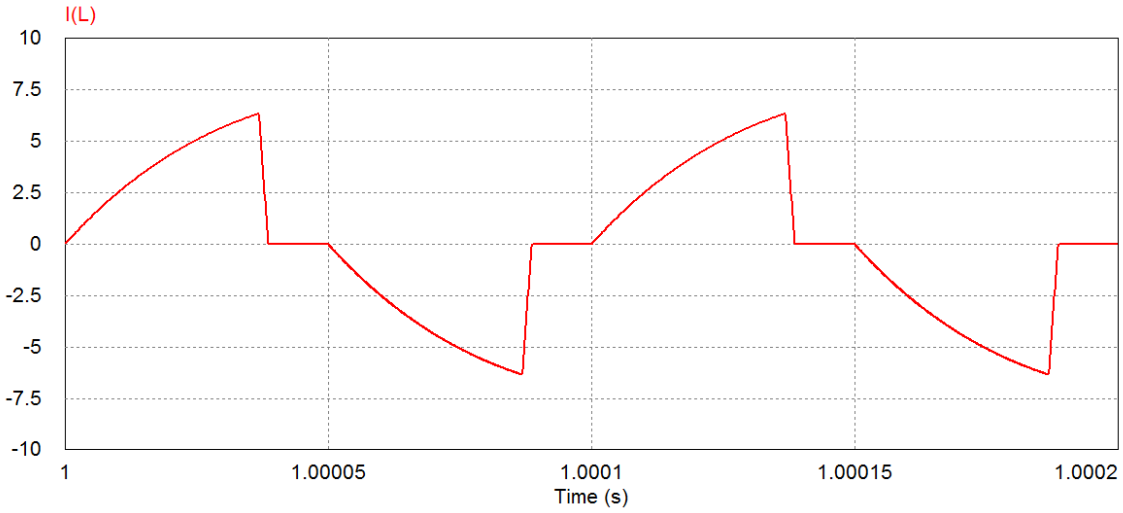


Fig. 3.26. Experimental setup of the SAB converter.

The input DC voltage, due to the limitation of the diode rectifier, is set 155 V_{peak}. The load has been simulated using a resistor of 5.6 Ω. The output voltage reference is set to 24 V to have a power transfer of about 100 W. The experimental results are shown in Fig. 3.27(a). It shows the voltage at the output of the active bridge before the high frequency transformer (violet), the inductance current at low voltage side (light blue), the output voltage (green) and current (yellow). The AC voltage is slightly lower than the supply voltage because of the voltage drops across the MOSFETs and the cables. The command variable α is around 2 rad and the peak current is 9 A. Its value is lower than the value calculable by analytical equations due to the parasitic elements. The input and output voltages of the simulations and experiment are not the same; however, the command variable and the ratio between input and output voltage are about the same, so that a comparison can be done. The difference between the shape of the current obtained by simulation and experiment is due to the parasitic resistances. Indeed, Fig. 3.27 (b) shows that, increasing the parasitic resistance R in the simulated circuit, the current waveform becomes similar to that obtained by experiment.

(a)



(b)

Fig.3.27 (a) voltage at the output of the active bridge (violet), inductance current at low voltage side (light blue), output voltage (green) and current (yellow), and (b) inductance current obtained by simulation with the parasitic resistance increased.

As shown in Fig. 3.27 (a), the value of the output voltage is approximately 24V as requested by the control system. The output current value is 4.3 A. Then, the power transfer is about 103 W. The peaks in the output current are disturbances measured by the current probe that very likely are not present in the actual output current. The efficiency of the SAB converter, operating under the tested conditions, is around 93-94%.

CHAPTER 4

Dual Active Bridge converter

The Dual Active Bridge converter (DAB) is composed of an active input bridge, a high frequency transformer and an output active bridge [47]-[52]. It has the circuit schematic of Fig.4.1: the bridge supplied by the DC voltage source (input bridge) is set up with transistors paralleled by diodes and executes a DC-AC conversion. The bridge feeding the load (output bridge) is set up also with transistors paralleled by diodes and executes an AC-DC conversion. The interposed transformer constitutes an isolated AC link connecting the two bridges. Downstream the output bridge and in parallel to the load, the converter has a capacitive filter that smoothens the DC voltage applied to the load. In turn, upstream the input bridge it has an inductive-capacitive filter that smoothens the current drawn from the DC voltage source. This filter is not reported in the circuit schematic.

Adjustment of the load voltage V_o is achieved by the control of phase between the two bridges. Unlike the SAB converter, the DAB converter, thanks to the two active bridges, can support a bidirectional power flow of buck-boost type. When the power flows from the input to the output bridge, the operation is called forward mode; instead, when the power flows from the output to the input bridge the operation is called backward. In this chapter, the steady state operation of the DAB is analyzed for the different working condition but the design characteristics and the soft-switching capabilities are analyzed only for the forward mode of buck type to obtain its characteristics and operability under the same working condition of the SAB converter.

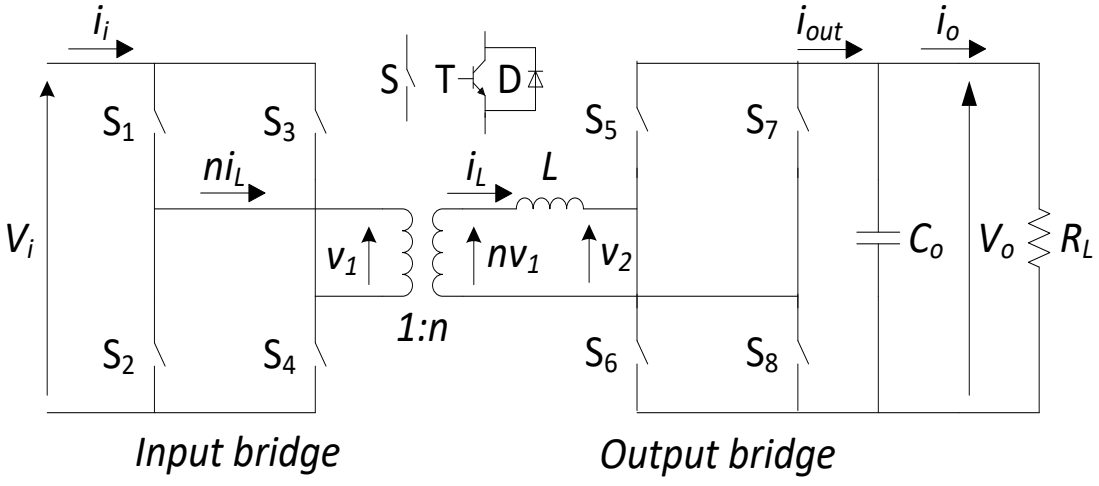


Fig.4.1 DAB converter circuit schematic.

4.1 Steady-state operation

4.1.1 Forward mode

Figs.4.2 (a)-(c) plot voltages and currents, together with the conducting devices, of the DAB converter operating at steady-state in buck mode. Fig.4.2 (a) shows that both the bridges impress a

square-wave voltage across the AC link and that the two voltages are shifted by the phase angle α, which plays the role of command variable. From the figure it comes out that the DAB converter, unlike the SAB converter, i) operates only in CCM, and ii) has only two intervals over π with different values of the voltage (v_1-v_2) applied across the inductance L, namely $0 \div \alpha$ and $\alpha \div \pi$. Like the SAB converter, voltages and currents of the DAB converter, have half-wave symmetry.

According to the applied command variable, the inductance current $i_L(\alpha)$ at α can be positive, as shown on the left side of Fig. 4.2 (b), or negative, as shown on the right side of Fig. 4.2 (b). If $i_L(\alpha) > 0$ the angle φ, which is the angle where the current crosses the zero, is lower than α; vice versa, if $i_L(\alpha) < 0$ the angle φ is higher than α. The command variable that define the boundary between these two cases is denoted as α'.

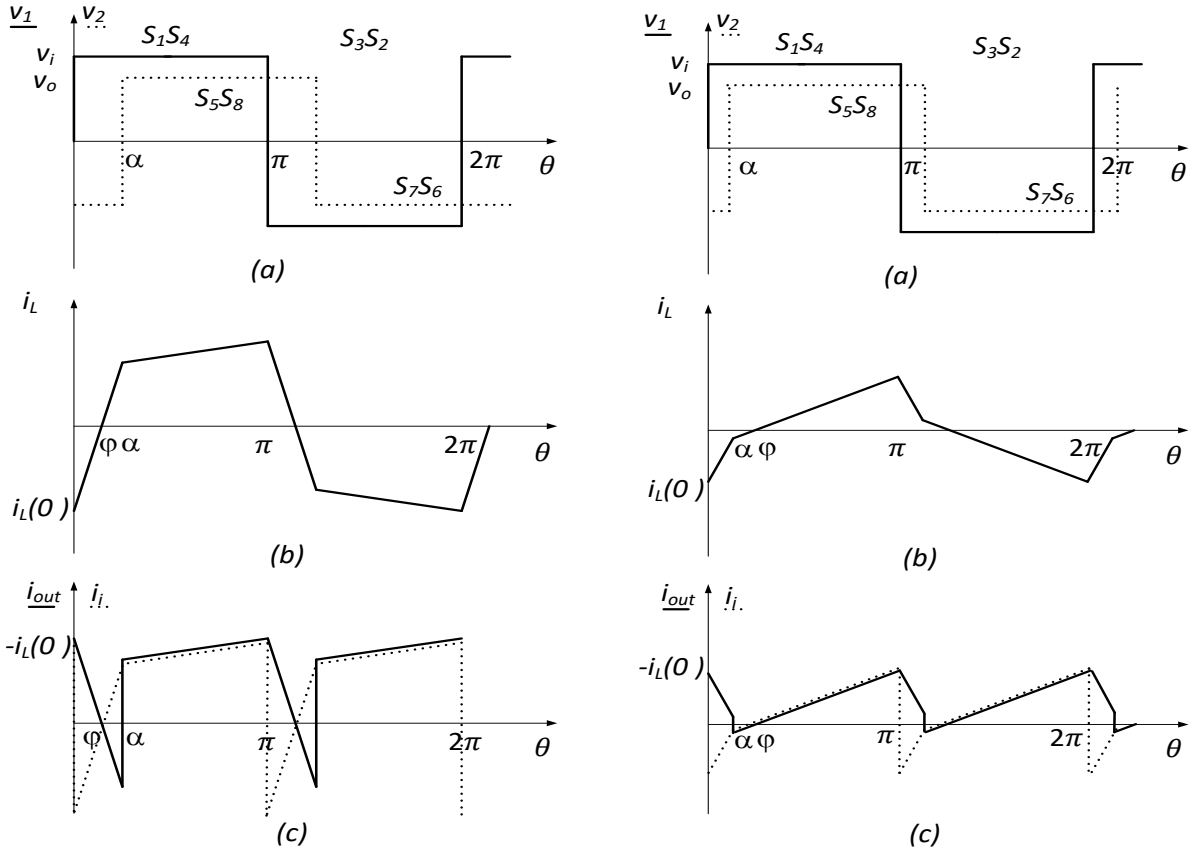


Fig.4.2. DAB converter current and voltage waveforms with α > α' (left side) and α < α' (right side) in buck mode

Let us start with the case when the inductance current at α is positive and α > α'. The currents during the intervals $0 \div \varphi$, $\varphi \div \alpha$ and $\alpha \div \pi$ are the following.

- $[0 \div \varphi]$

$$i_L(\varphi) = i_L(0) + \int_0^{\varphi} \frac{V_L}{\omega L} d\theta = i_L(0) + \frac{V_i + V_o}{\omega L}\varphi = 0 \qquad (4.1)$$

- $[\varphi \div \alpha]$

$$i_L(\alpha) = i_L(\varphi) + \int_{\varphi}^{\alpha} \frac{V_L}{\omega L} d\theta = 0 + \frac{V_i + V_o}{\omega L}(\alpha - \varphi) \qquad (4.2)$$

- $[\alpha \div \pi]$

$$i_L(\pi) = -i_L(0) = i_L(\alpha) + \int_{\alpha}^{\pi} \frac{V_L}{\omega L} d\theta = i_L(\alpha) + \frac{V_i - V_o}{\omega L}(\pi - \alpha) \quad (4.3)$$

By exploiting the half-wave symmetry of i_L, the values of i_L at $\theta = 0$ and at $\theta = \alpha$ are readily calculated in

$$i_L(0) = -\frac{V_i}{\omega L}\frac{\pi}{2}\left[\left(2\frac{\alpha}{\pi} - 1\right)\frac{V_o}{V_i} + 1\right] \quad (4.4)$$

$$i_L(\alpha) = \frac{V_i}{\omega L}\frac{\pi}{2}\left(2\frac{\alpha}{\pi} - 1 + \frac{V_o}{V_i}\right) \quad (4.5)$$

and the current shift angle φ is calculated in

$$\varphi_{GR} = \pi\left(\frac{1}{2} - \frac{1}{2}\frac{V_o}{V_i} + \frac{\alpha}{\pi}\frac{V_o}{V_i}\right)\frac{1}{\left(1+\frac{V_o}{V_i}\right)} \quad (4.6)$$

where the subscript GR indicates the case when the current at α is greater than zero.

The boundary condition α' is calculated setting $i_L(\alpha) = 0$ and is given by:

$$\alpha' = \frac{\pi}{2}\left(1 - \frac{V_o}{V_i}\right) \quad (4.7)$$

The load current I_o, given by the average value of i_{out}, is

$$I_o = \frac{1}{\pi}\left[-\frac{i_L(0)\varphi_{GR}}{2} - \frac{i_L(\alpha)(\alpha-\varphi_{GR})}{2} + \frac{(i_L(\alpha)+i_L(\pi))(\pi-\alpha)}{2}\right] =$$

$$= \frac{V_i}{\omega L}\pi\frac{\alpha}{\pi}\left(1 - \frac{\alpha}{\pi}\right) \quad (4.8)$$

Eq. (4.8) shows that, unlike the SAB converter, the load current does not depend on the output voltage V_o but only on the command variable α. Its behavior is the same as a current generator. Regarding the dependence on α, I_o increases with α up to a maximum that is reached for $\alpha = \pi/2$ and then decreases. Therefore, for statically stable operation of the DAB converter, α must be less than π/2. The relationship between I_o and α in the operating range is plotted in Fig.4.3.

The delivered active power is given multiplying the average current and the output voltage, which is assumed constant.

$$P_o = \frac{V_i V_o}{\omega L}\pi\frac{\alpha}{\pi}\left(1 - \frac{\alpha}{\pi}\right) \quad (4.9)$$

The output voltage V_o, for a generic load R_L, is given by:

$$V_o = R_L\frac{V_i}{\omega L}\pi\frac{\alpha}{\pi}\left(1 - \frac{\alpha}{\pi}\right) \quad (4.10)$$

Eq. (4.10) shows that the output voltage depends on the load resistance R_L. The relationships between the output voltage, the output current and the command variable for different values of the load resistance are plotted in Figs. 4.4 and 4.5.

Considering that the boundary condition between the buck and boost operation modes is $V_o = V_i$, the buck mode is present only for heavy loads (small R_L) and the boundary condition is given by:

$$R_{L,B} = \frac{\omega L}{\alpha\left(1-\frac{\alpha}{\pi}\right)} \quad (4.11)$$

For R_L higher than $R_{L,B}$ the DAB operates in boost mode. Its current and voltage waveforms are shown in Fig. 4.6. The equations are the same as the DAB operating in buck mode. In boost mode $i_L(\alpha)$ is always positive during the positive half wave of the current.

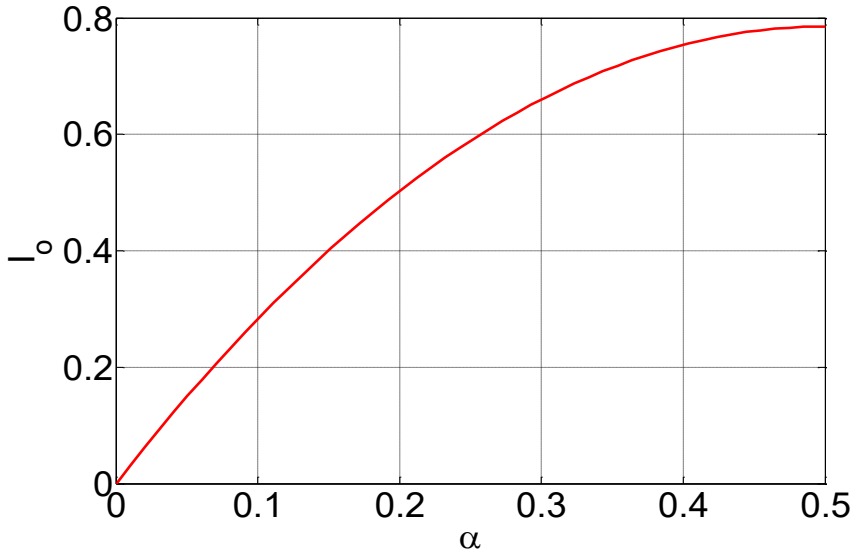


Fig.4.3. DAB converter load current vs. command variable in forward mode.

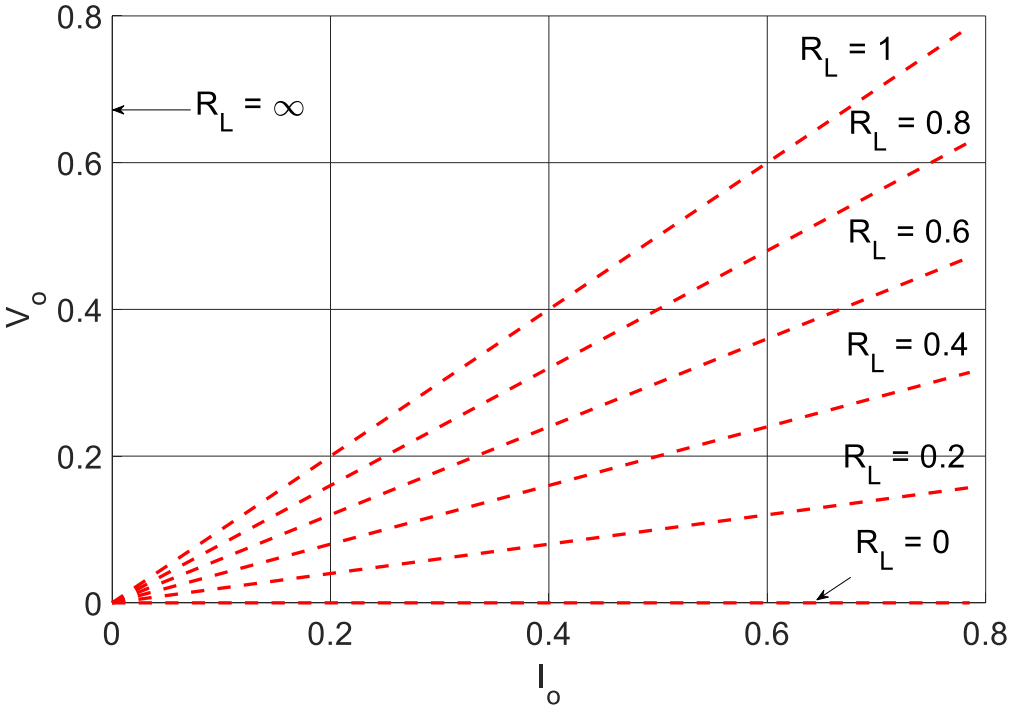


Fig.4.4. DAB converter load current vs. output voltage for different values of load resistance (expressed in Ohm) in forward mode.

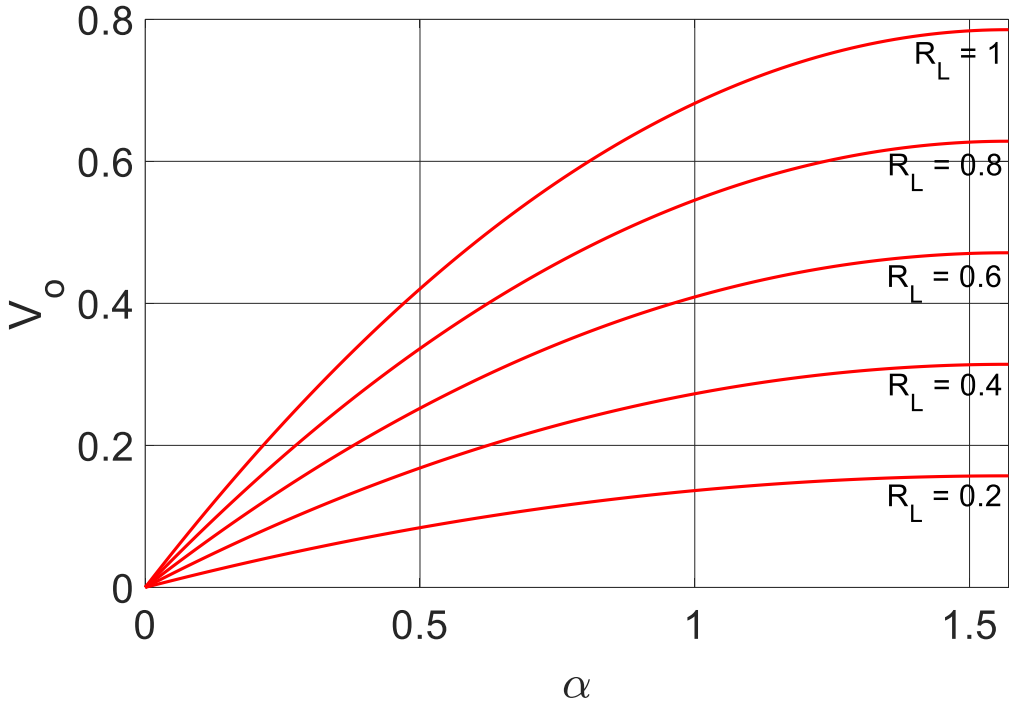


Fig.4.5. DAB converter output voltage vs. command variable in forward mode.

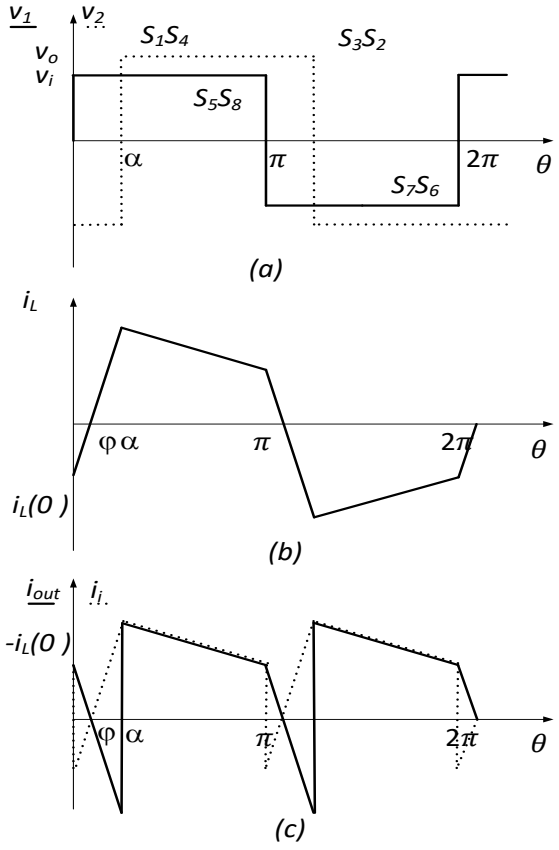


Fig.4.6. DAB converter current and voltage waveforms in boost mode

Let's consider the case when the inductance current at α is negative and α < α'. The currents during the intervals 0 ÷ α, α ÷ φ and φ ÷ π are the following.

- $[0 \div \alpha]$

$$i_L(\alpha) = i_L(0) + \int_0^{\alpha} \frac{V_L}{\omega L} d\theta = i_L(0) + \frac{V_i + V_o}{\omega L}\alpha \quad (4.12)$$

- $[\alpha \div \varphi]$

$$i_L(\varphi) = i_L(\alpha) + \int_{\alpha}^{\varphi} \frac{V_L}{\omega L} d\theta = i_L(\alpha) + \frac{V_i - V_o}{\omega L}(\varphi - \alpha) = 0 \quad (4.13)$$

- $[\varphi \div \pi]$

$$i_L(\pi) = -i_L(0) = i_L(\varphi) + \int_{\varphi}^{\pi} \frac{V_L}{\omega L} d\theta = 0 + \frac{V_i - V_o}{\omega L}(\pi - \varphi) \quad (4.14)$$

By exploiting the half-wave symmetry of i_L, the equations of i_L at $\theta = 0$ and at $\theta = \alpha$ are the same found for the case with $\alpha > \alpha'$. The load current I_o, given by the average value of i_{out}, is

$$I_o = \frac{1}{\pi}\left[\frac{(-i_L(0) + i_L(\alpha))\alpha}{2} - \frac{i_L(\alpha)(\varphi_{LE} - \alpha)}{2} + \frac{i_L(\pi)(\pi - \varphi_{LE})}{2}\right] =$$

$$= \frac{V_i}{\omega L}\pi\frac{\alpha}{\pi}\left(1 - \frac{\alpha}{\pi}\right) \quad (4.15)$$

and the current shift angle φ is calculated in

$$\varphi_{LE} = \pi\left(\frac{1}{2} - \frac{1}{2}\frac{V_o}{V_i} - \frac{\alpha}{\pi}\frac{V_o}{V_i}\right)\frac{1}{\left(1 - \frac{V_o}{V_i}\right)} \quad (4.16)$$

where the subscript LE indicates the case when the current at α is lower than zero.

From eq. (4.16) it is appears that the equation of the average current does not change in the two cases. Therefore, the equation of the output average voltage and power are the same as (4.9) and (4.10).

Note that the condition $\alpha = \alpha'$corresponds to a load current I_o' given by

$$I_o' = \frac{V_i}{\omega L}\frac{\pi}{4}\left(1 - \frac{{V_o}^2}{{V_i}^2}\right) \quad (4.17)$$

4.1.2 Backward mode

Figs.4.7 (a)-(c) plot voltages and currents, together with the conducting devices, of the DAB converter operating at steady-state in backward buck mode. Fig.4.7 (a) show that, as for the forward mode, both the bridges impress a square-wave voltage across the AC link and the two voltages are shifted by the phase angle α. Unlike in the forward mode, where voltage v_2 lags voltage v_1, in backward mode v_2 leads v_1 so that the command variable α is negative.

As for the forward mode, when the DAB is operating in buck mode the inductance current $i_L(\alpha)$ can be positive or negative. As for the forward mode, the equations of the average current and power are the same in the two cases. Then, only the case with $i_L(\alpha) > 0$ is reported for the backward mode.

The currents during the intervals $0 \div (\pi + \alpha)$, $(\pi + \alpha) \div \varphi$ and $\varphi \div \pi$ are the following:

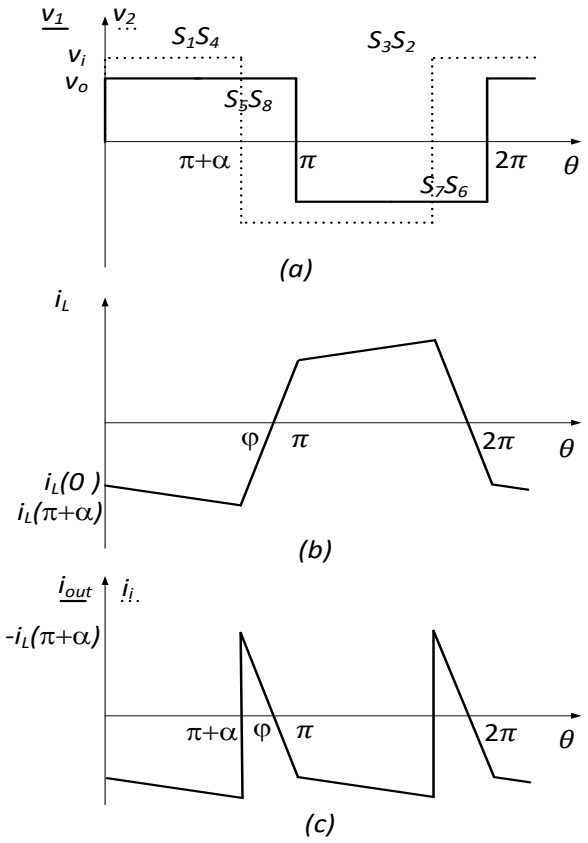


Fig.4.7. DAB converter current and voltage waveforms in backward buck mode.

- $[0 \div (\pi + \alpha)]$

$$i_L(\pi + \alpha) = i_L(0) + \int_0^{\pi+\alpha} \frac{V_L}{\omega L} d\theta = i_L(0) + \frac{V_i - V_o}{\omega L}\varphi \quad (4.18)$$

- $[(\pi + \alpha) \div \varphi]$

$$i_L(\varphi) = i_L(\pi + \alpha) + \int_{\pi+\alpha}^{\varphi} \frac{V_L}{\omega L} d\theta = i_L(\pi + \alpha) - \frac{V_i + V_o}{\omega L}\big(\varphi - (\pi + \alpha)\big) = 0 \quad (4.19)$$

- $[\varphi \div \pi]$

$$i_L(\pi) = -i_L(0) = i_L(\varphi) + \int_{\varphi}^{\pi} \frac{V_L}{\omega L} d\theta = 0 - \frac{V_i + V_o}{\omega L}(\pi - \varphi) \quad (4.20)$$

By exploiting the half-wave symmetry of i_L, the values of i_L at $\theta = 0$ and at $\theta = \alpha$ are readily calculated in

$$i_L(0) = \frac{V_i}{\omega L}\frac{\pi}{2}\left[\left(2\frac{\alpha}{\pi} + 1\right)\frac{V_o}{V_i} - 1\right] \quad (4.21)$$

$$i_L(\pi + \alpha) = \frac{V_i}{\omega L}\frac{\pi}{2}\left(2\frac{\alpha}{\pi} + 1 - \frac{V_o}{V_i}\right) \quad (4.22)$$

The load current I_o and the output power are given by:

$$I_o = \frac{V_i}{\omega L}\pi\frac{\alpha}{\pi}\left(1 + \frac{\alpha}{\pi}\right) \quad (4.23)$$

$$P_o = \frac{V_i V_o}{\omega L}\pi\frac{\alpha}{\pi}\left(1 + \frac{\alpha}{\pi}\right) \quad (4.24)$$

The equations (4.23) and (4.24) are valid also when $i_L(\alpha) < 0$ in buck mode and when the DAB operates in boost mode. The backward mode is possible only when an active load is connected to the output bridge. Therefore, considering that the voltage is impressed by a source connected to the output port, the equation of the output average voltage is not relevant.

The equations of the currents, power and voltage are summarized in Tab 4.1.

Tab 4.1. DAB equations in forward and backward mode

Forward mode	$i_L(0) = -\frac{V_i}{\omega L}\frac{\pi}{2}\left[\left(2\frac{\alpha}{\pi} - 1\right)\frac{V_o}{V_i} + 1\right]$
	$i_L(\alpha) = \frac{V_i}{\omega L}\frac{\pi}{2}\left(2\frac{\alpha}{\pi} - 1 + \frac{V_o}{V_i}\right)$
	$I_o = \frac{V_i}{\omega L}\pi\frac{\alpha}{\pi}\left(1 - \frac{\alpha}{\pi}\right)$
	$P_o = \frac{V_i V_o}{\omega L}\pi\frac{\alpha}{\pi}\left(1 - \frac{\alpha}{\pi}\right)$
	$V_o = R_L\frac{V_i}{\omega L}\pi\frac{\alpha}{\pi}\left(1 - \frac{\alpha}{\pi}\right)$
Backward mode	$i_L(0) = \frac{V_i}{\omega L}\frac{\pi}{2}\left[\left(2\frac{\alpha}{\pi} + 1\right)\frac{V_o}{V_i} - 1\right]$
	$i_L(\pi + \alpha) = \frac{V_i}{\omega L}\frac{\pi}{2}\left(2\frac{\alpha}{\pi} + 1 - \frac{V_o}{V_i}\right)$
	$I_o = \frac{V_i}{\omega L}\pi\frac{\alpha}{\pi}\left(1 + \frac{\alpha}{\pi}\right)$
	$P_o = \frac{V_i V_o}{\omega L}\pi\frac{\alpha}{\pi}\left(1 + \frac{\alpha}{\pi}\right)$

The waveform of the output average current in both the modes is shown in Fig. 4.8. The maximum current is reached for $\alpha = \pm\frac{\pi}{2}$ and its maximum normalized value is $I_{o,max} = \frac{\pi}{4} \approx 0.79$. As for the forward mode, for statically stable operation of the DAB converter, α must be higher than -π/2. Then, the operation range of the command variable is $-\frac{\pi}{2} < \alpha < \frac{\pi}{2}$.

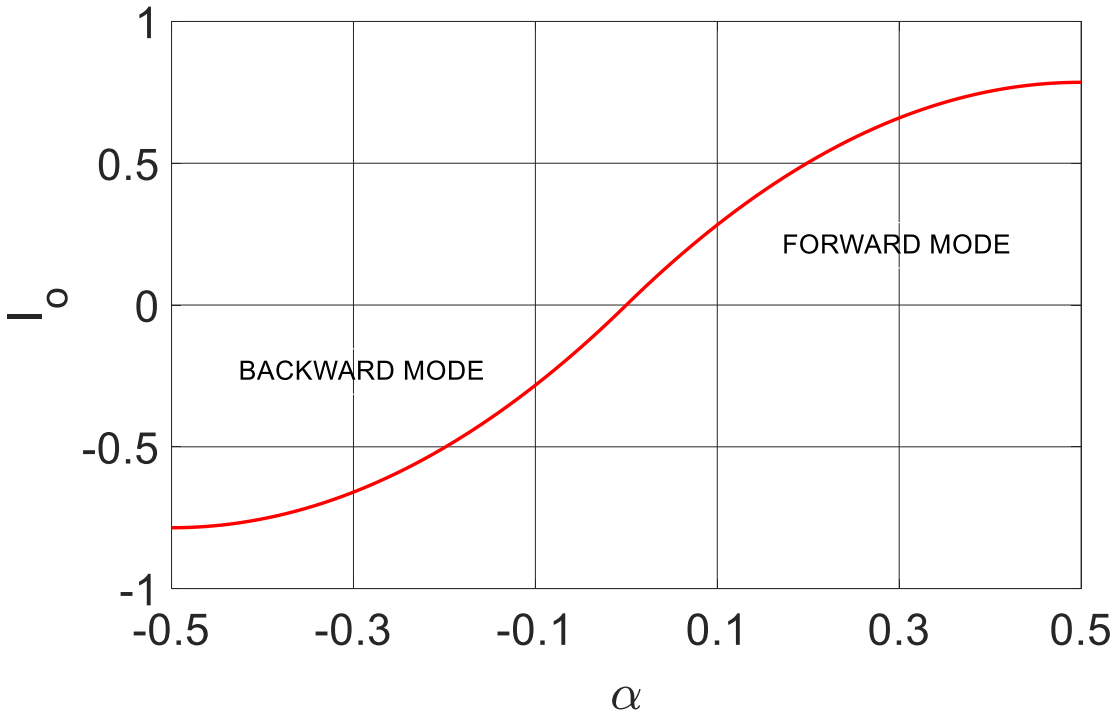


Fig.4.8. DAB converter load current vs. command variable in forward mode.

4.2 Design characteristics

The design characteristics are calculated only for the DAB operating in forward mode of buck type. This choice has been made because this operating condition is the most important for the applications of interest. In addition, its deep analysis allows a full comparison with the SAB converter characteristics. The same reasoning is applied for the remaining part of chapter 4.

4.2.1 Output current alternating component rms value

For $I_o<I_o'$ the rms value of the alternating component of the output current is calculated in

$$I_{rms,o,LE} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_L(\theta)^2 d\theta - I_0^2} \tag{4.25}$$

Considering the three areas highlighted in Fig. 4.9 (a), the calculation is performed as follows:

1)

$$\frac{\theta-0}{\alpha-0} = \frac{i_L(\theta)+i_L(0)}{-i_L(\alpha)+i_L(0)} \quad => \quad i_L(\theta) = -i_L(0) + [-i_L(\alpha) + i_L(0)]\frac{\theta}{\alpha}$$

$$i_L(\theta)^2 = i_L(0)^2 + [-i_L(\alpha) + i_L(0)]^2\frac{\theta^2}{\alpha^2} - 2i_L(0)[-i_L(\alpha) + i_L(0)]\frac{\theta}{\alpha}$$

$$\int_0^{\alpha} i_L(\theta)^2\, d\theta = i_L(0)^2\alpha + [-i_L(\alpha) + i_L(0)]^2\frac{\alpha}{3} + -i_L(0)[-i_L(\alpha) + i_L(0)]\alpha \tag{4.26}$$

2)

$$\frac{\theta-\alpha}{\varphi-\alpha} = \frac{i_L(\theta)-i_L(\alpha)}{0-i_L(\alpha)} \quad => \quad i_L(\theta) = i_L(\alpha) - i_L(\alpha)\frac{\theta-\alpha}{\varphi-\alpha}$$

$$i_L(\theta)^2 = i_L(\alpha)^2 + i_L(\alpha)^2 \frac{(\theta-\alpha)^2}{(\varphi-\alpha)^2} - 2i_L(\alpha)^2 \frac{\theta-\alpha}{\varphi-\alpha}$$

$$\int_\alpha^\varphi i_L(\theta)^2 \, d\theta = i_L(\alpha)^2 \frac{\varphi-\alpha}{3} \tag{4.27}$$

3)

$$\frac{\theta-\varphi}{\pi-\varphi} = \frac{i_L(\theta)-0}{-i_L(0)-0} \quad \Rightarrow \quad i_L(\theta) = -i_L(0)\frac{\theta-\varphi}{\pi-\varphi}$$

$$\int_\varphi^\pi i_L(\theta)^2 \, d\theta = i_L(0)^2 \frac{\pi-\varphi}{3} \tag{4.28}$$

From eqs. (4.26)-(4.28), the rms value of the alternating component of the output current is

$$I_{rms,o,LE} = \sqrt{\frac{1}{3}\left[i_L(\alpha)^2 \frac{\varphi_{LE}}{\pi} + i_L(0)^2\left(1 - \frac{\varphi_{LE}}{\pi} + \frac{\alpha}{\pi}\right) + i_L(\alpha)i_L(0)\frac{\alpha}{\pi}\right] - I_o^2} \tag{4.29}$$

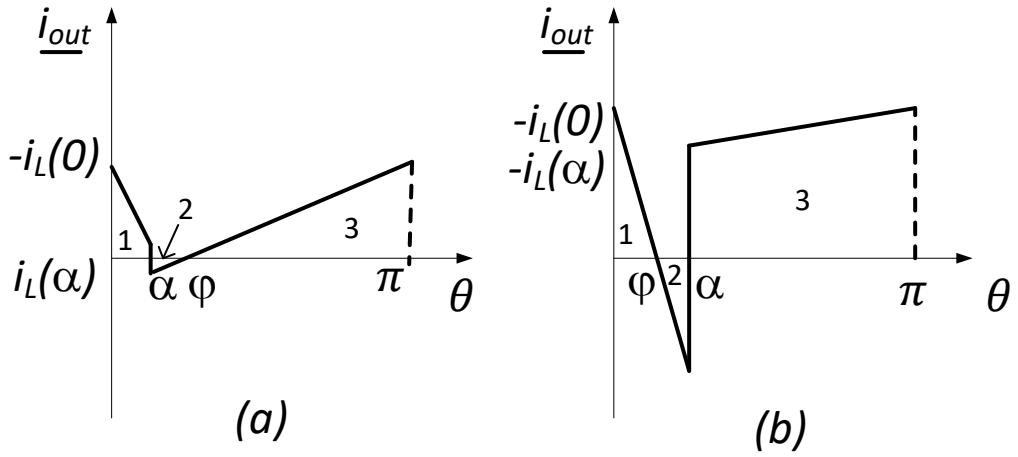


Fig.4.9. waveform of the output current for $i_L(\alpha) < 0$ (a) and $i_L(\alpha) > 0$ (b).

From analysis of Fig. 4.9 (b) it emerges that the same reasoning can be done for $I_o > I_o'$.

1)

$$\frac{\theta-0}{\varphi-0} = \frac{i_L(\theta)+i_L(0)}{0+i_L(0)} \quad \Rightarrow \quad i_L(\theta) = -i_L(0) + i_L(0)\frac{\theta}{\varphi}$$

$$i_L(\theta)^2 = i_L(0)^2 + i_L(0)^2 \frac{\theta^2}{\varphi^2} - 2i_L(0)^2 \frac{\theta}{\varphi}$$

$$\int_0^\varphi i_L(\theta)^2 \, d\theta = i_L(0)^2 \frac{\varphi}{3} \tag{4.30}$$

2)

$$\frac{\theta-\varphi}{\alpha-\varphi} = \frac{i_L(\theta)-0}{-i_L(\alpha)-0} \quad \Rightarrow \quad i_L(\theta) = -i_L(\alpha)\frac{\theta-\varphi}{\alpha-\varphi}$$

$$\int_\varphi^\alpha i_L(\theta)^2 \, d\theta = i_L(\alpha)^2 \frac{\alpha-\varphi}{3} \tag{4.31}$$

3)

$$\frac{\theta-\alpha}{\pi-\alpha} = \frac{i_L(\theta)-i_L(\alpha)}{-i_L(0)-i_L(\alpha)} \quad \Rightarrow \quad i_L(\theta) = i_L(\alpha) - [i_L(0) + i_L(\alpha)]\frac{\theta-\alpha}{\pi-\alpha}$$

$$i_L(\theta)^2 = i_L(\alpha)^2 + [i_L(0) + i_L(\alpha)]^2 \frac{(\theta-\alpha)^2}{(\pi-\alpha)^2} - 2i_L(\alpha)[i_L(0) + i_L(\alpha)] \frac{(\theta-\alpha)}{(\pi-\alpha)}$$

$$\int_\alpha^\pi i_L(\theta)^2 \, d\theta = i_L(\alpha)^2(\pi - \alpha) + [i_L(0) + i_L(\alpha)]^2 \frac{(\pi-\alpha)}{3} - i_L(\alpha)[i_L(0) + i_L(\alpha)](\pi - \alpha) \quad (4.32)$$

From eqs. (4.30)-(4.32), the rms value of the alternating component of the output current is

$$I_{rms,o,GR} = \sqrt{\frac{1}{3}\left[i_L(\alpha)^2\left(1 - \frac{\varphi_{GR}}{\pi}\right) + i_L(0)^2\left(1 + \frac{\varphi_{GR}}{\pi} - \frac{\alpha}{\pi}\right) - i_L(\alpha)i_L(0)\left(1 - \frac{\alpha}{\pi}\right)\right] - I_o^2} \quad (4.33)$$

Eqs. (4.29) and (4.33) are plotted in Fig.4.10 as a function of I_o. In Fig. 4.10 and in the following figures the dot marks denote operation at I_o=I_o'.

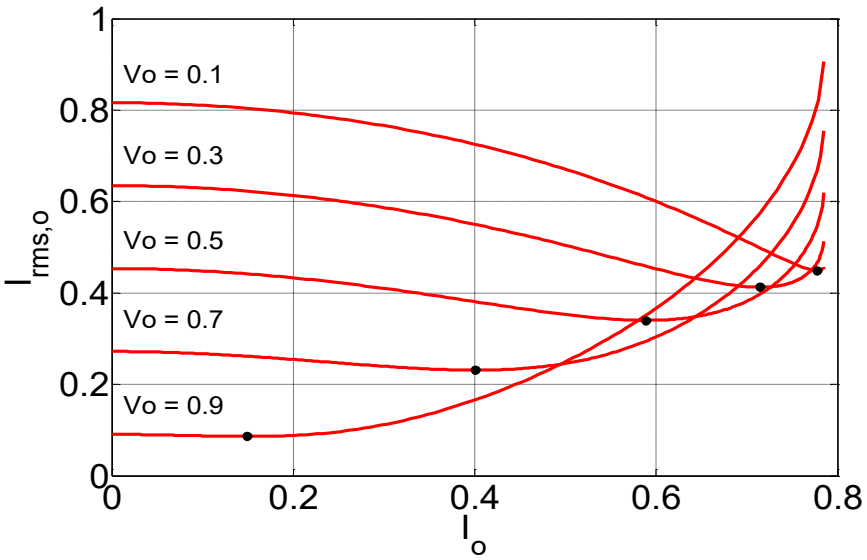


Fig.4.10. DAB converter rms value of the alternating component of the output current vs. load current.

4.2.2 Output current ripple

The peak-to-peak ripple R_o of the output current can be expressed as follows, independently of the value of I_o:

$$R_o = -i_L(0) + |i_L(\alpha)| = \frac{V_i}{\omega L}\frac{\pi}{2}\left[1 + \frac{V_o}{V_i}\left(2\frac{\alpha}{\pi} - 1\right) + \left|-1 + \frac{V_o}{V_i} + 2\frac{\alpha}{\pi}\right|\right] \quad (4.34)$$

Eq. (4.34) is plotted in Fig.4.11 as a function of I_o. It can be observed that for I_o<I_o' the ripple decreases whilst for I_o>I_o' it increases.

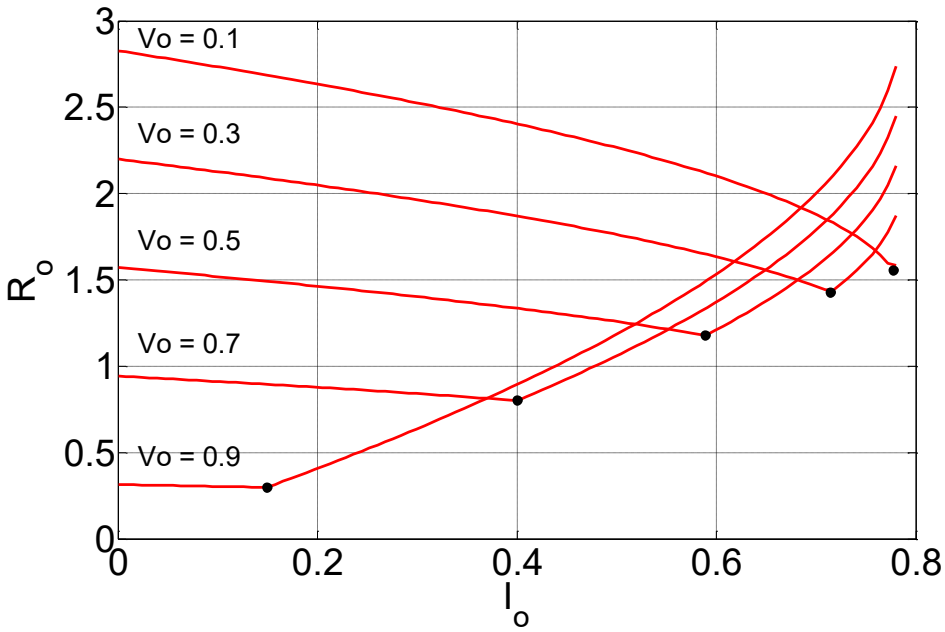


Fig.4.11 DAB converter output current ripple vs. load current.

4.2.3 Input current alternating component rms value

For $I_o<I_o'$ the rms value of the alternating component of the output current is calculated in

$$I_{rms,o,LE} = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_L(\theta)^2 d\theta - I_i^2} \qquad (4.35)$$

Looking at Fig. 4.12 (a) the calculation, considering the three areas, is performed as follows:

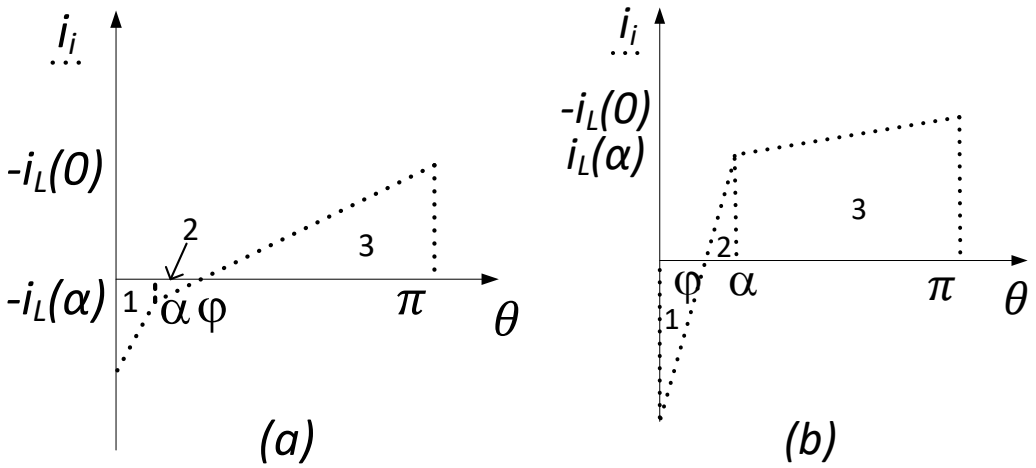


Fig.4.12. waveform of the input current for $i_L(\alpha) < 0$ (a) and $i_L(\alpha) > 0$ (b).

1)

$$\frac{\theta-0}{\alpha-0} = \frac{i_L(\theta)-i_L(0)}{-i_L(\alpha)-i_L(0)} \quad => \quad i_L(\theta) = i_L(0) + [i_L(\alpha) - i_L(0)]\frac{\theta}{\alpha}$$

$$i_L(\theta)^2 = i_L(0)^2 + [i_L(\alpha) - i_L(0)]^2\frac{\theta^2}{\alpha^2} + 2i_L(0)[i_L(\alpha) - i_L(0)]\frac{\theta}{\alpha}$$

$$\int_0^{\alpha} i_L(\theta)^2\, d\theta = [i_L(\alpha) - i_L(0)]^2 \frac{\alpha}{3} + i_L(0) i_L(\alpha)\alpha \tag{4.36}$$

2)

$$\frac{\theta-\alpha}{\varphi-\alpha} = \frac{i_L(\theta)-i_L(\alpha)}{0-i_L(\alpha)} \quad \Rightarrow \quad i_L(\theta) = i_L(\alpha) - i_L(\alpha)\frac{\theta-\alpha}{\varphi-\alpha}$$

$$i_L(\theta)^2 = i_L(\alpha)^2 + i_L(\alpha)^2 \frac{(\theta-\alpha)^2}{(\varphi-\alpha)^2} - 2 i_L(\alpha)^2 \frac{\theta-\alpha}{\varphi-\alpha}$$

$$\int_{\alpha}^{\varphi} i_L(\theta)^2\, d\theta = i_L(\alpha)^2 \frac{\varphi-\alpha}{3} \tag{4.37}$$

3)

$$\frac{\theta-\varphi}{\pi-\varphi} = \frac{i_L(\theta)-0}{-i_L(0)-0} \quad \Rightarrow \quad i_L(\theta) = -i_L(0)\frac{\theta-\varphi}{\pi-\varphi}$$

$$\int_{\varphi}^{\pi} i_L(\theta)^2\, d\theta = i_L(0)^2 \frac{\pi-\varphi}{3} \tag{4.38}$$

From eqs. (4.36)-(4.38) the rms value of the alternating component of the input current is

$$I_{rms,i,LE} = \sqrt{\frac{1}{3}\left[i_L(\alpha)^2 \frac{\varphi_{LE}}{\pi} + i_L(0)^2\left(1 + \frac{\alpha}{\pi} - \frac{\varphi_{LE}}{\pi}\right) + i_L(\alpha) i_L(0)\frac{\alpha}{\pi}\right] - I_i^2} \tag{4.39}$$

Looking at Fig. 4.12 (b), the same reasoning is done for $I_o > I_o'$.

1)

$$\frac{\theta-0}{\varphi-0} = \frac{i_L(\theta)-i_L(0)}{0-i_L(0)} \quad \Rightarrow \quad i_L(\theta) = i_L(0) - i_L(0)\frac{\theta}{\varphi}$$

$$i_L(\theta)^2 = i_L(0)^2 + i_L(0)^2 \frac{\theta^2}{\varphi^2} - 2 i_L(0)^2 \frac{\theta}{\varphi}$$

$$\int_0^{\varphi} i_L(\theta)^2\, d\theta = i_L(0)^2 \frac{\varphi}{3} \tag{4.40}$$

2)

$$\frac{\theta-\varphi}{\alpha-\varphi} = \frac{i_L(\theta)-0}{i_L(\alpha)-0} \Rightarrow \quad i_L(\theta) = i_L(\alpha)\frac{\theta-\varphi}{\alpha-\varphi}$$

$$\int_{\varphi}^{\alpha} i_L(\theta)^2\, d\theta = i_L(\alpha)^2 \frac{\alpha-\varphi}{3} \tag{4.41}$$

3)

$$\frac{\theta-\alpha}{\pi-\alpha} = \frac{i_L(\theta)-i_L(\alpha)}{-i_L(0)-i_L(\alpha)} \quad \Rightarrow \quad i_L(\theta) = i_L(\alpha) - [i_L(0) + i_L(\alpha)]\frac{\theta-\alpha}{\pi-\alpha}$$

$$i_L(\theta)^2 = i_L(\alpha)^2 + [i_L(0) + i_L(\alpha)]^2 \frac{(\theta-\alpha)^2}{(\pi-\alpha)^2} - 2 i_L(\alpha)[i_L(0) + i_L(\alpha)]\frac{(\theta-\alpha)}{(\pi-\alpha)}$$

$$\int_{\alpha}^{\pi} i_L(\theta)^2\, d\theta = i_L(\alpha)^2(\pi-\alpha) + [i_L(0) + i_L(\alpha)]^2 \frac{(\pi-\alpha)}{3} - i_L(\alpha)[i_L(0) + i_L(\alpha)](\pi-\alpha) \tag{4.42}$$

From eqs. (4.40)-(4.42) the rms value of the alternating component of the input current is

$$I_{rms,i,GR} = \sqrt{\frac{1}{3}\left[i_L(\alpha)^2\left(1 - \frac{\varphi_{GR}}{\pi}\right) + i_L(0)^2\left(1 - \frac{\alpha}{\pi} + \frac{\varphi_{GR}}{\pi}\right) - i_L(\alpha) i_L(0)\left(1 - \frac{\alpha}{\pi}\right)\right] - I_i^2} \tag{4.43}$$

Eqs. (4.39) and (4.43) are plotted in Fig. 4.13 as a function of I_o.

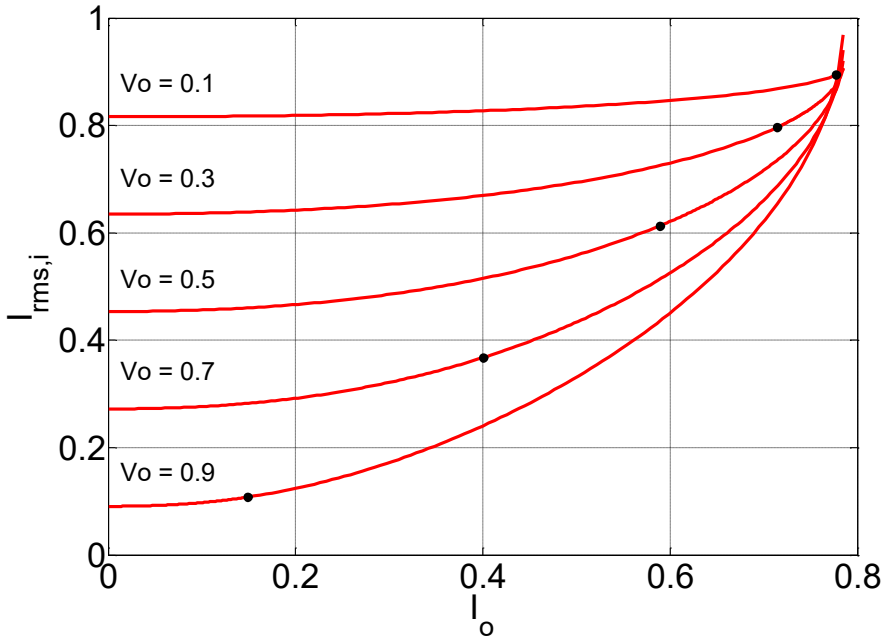


Fig.4.13 DAB rms value of the alternating component of the input current vs. load current.

4.2.4 Input current: average value and ripple

The same considerations expounded for the SAB converter can be applied to the DAB converter. By equating the average power at the input of the DAB converter to that one at the output, the average value I_i of the input current can be readily found in

$$I_i = \frac{V_o}{V_i} I_o \tag{4.44}$$

and its peak-to-peak ripple R_i is equal to $2i_L(0)$.

4.2.5 Bridge device currents

In the DAB converter, the transistors of each bridge as well as their diodes conduct for an equal time interval. Furthermore, the conduction intervals of the transistors of the input bridge are equal to those of the diodes of the output bridge. The same occurs for the diodes of the input bridge and the transistors of the output bridge. Therefore the analysis is executed only for transistor T_1 and diode D_1 of the input bridge, where T_1 conducts from φ to π and D_1 from 0 to φ, as shown in Fig.4.14.

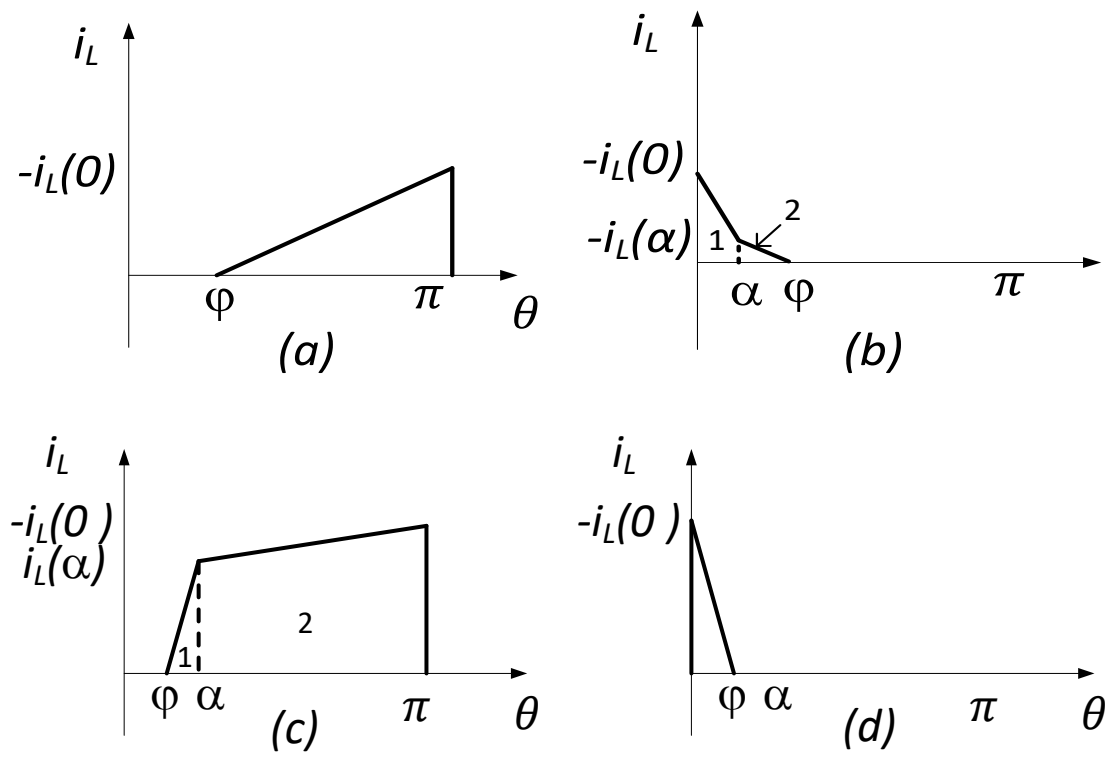


Fig.4.14. Conduction intervals of the transistor and diodes of the input bridge for $I_o<I_o'$ (transistors (a), diodes (b)) and for $I_o>I_o'$ (transistors (c), diodes (d)).

4.2.6 Device peak currents

The peak current I_p in transistor T_1 is equal to $i_L(\pi)$. Its value, which is the opposite of $i_L(0)$, is plotted in Fig.4.15 as a function of I_o (and for different values of V_o). The traces show an increase of the peak current for small values of V_o. When the current I_o rises, the difference of the peak current for different values of V_o tends to become smaller.

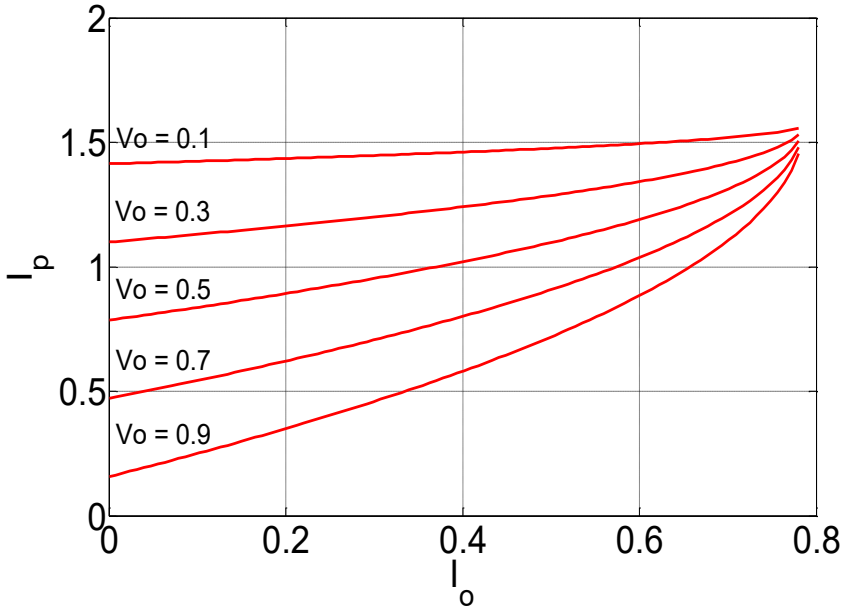


Fig.4.15. DAB converter device peak current vs. load current for different output voltages.

4.2.7 Device average currents

Looking the Figs. 4.14 (a)-(b), for $I_o<I_o'$ the average currents in transistor T_1 and diode D_1 are calculated in

$$I_{av,T,ib,LE} = -\frac{i_L(0)}{2}(\pi-\varphi)\frac{1}{2\pi} = \frac{V_i}{\omega L}\frac{\pi}{16}\left[1-\frac{V_o}{V_i}(1-2\frac{\alpha}{\pi})\right]^2\frac{1}{1-\frac{V_o}{V_i}} \quad (4.45)$$

$$I_{av,D,ib,LE} = \left\{-[i_L(0)+i_L(\alpha)]\frac{\alpha}{2} - i_L(\alpha)\frac{(\varphi-\alpha)}{2}\right\}\frac{1}{2\pi} =$$

$$= \frac{V_i}{\omega L}\frac{\pi}{16}\left\{\left[-1+2\frac{\alpha}{\pi}+\frac{V_o}{V_i}\right]^2\frac{1}{1-\frac{V_o}{V_i}} - 4\frac{\alpha}{\pi}\left(1-\frac{\alpha}{\pi}\right)\left(1-\frac{V_o}{V_i}\right)\right\} \quad (4.46)$$

whilst, looking the Figs. 4.14 (c)-(d), for $I_o>I_o'$ they are calculated in

$$I_{av,T,ib,GR} = \left\{i_L(\alpha)\frac{(\alpha-\varphi)}{2} + [-i_L(0)+i_L(\alpha)]\frac{(\pi-\alpha)}{2}\right\}\frac{1}{2\pi} =$$

$$= \frac{V_i}{\omega L}\frac{\pi}{16}\left\{\left[-\left(1-\frac{V_o}{V_i}\right)+2\frac{\alpha}{\pi}\right]^2\frac{1}{1+\frac{V_o}{V_i}} + 4\frac{\alpha}{\pi}\left(1-\frac{\alpha}{\pi}\right)\left(1+\frac{V_o}{V_i}\right)\right\} \quad (4.47)$$

$$I_{av,D,ib,GR} = -\frac{i_L(0)}{2}\varphi\frac{1}{2\pi} = \frac{V_i}{\omega L}\frac{\pi}{16}\left[1-\frac{V_o}{V_i}\left(1-2\frac{\alpha}{\pi}\right)\right]^2\frac{1}{1+\frac{V_o}{V_i}} \quad (4.48)$$

Eqs. (4.45) -(4.48) are plotted in Fig. 4.16 as a function of I_o.

4.2.8 Device rms currents

Looking the Fig. 4.14 (a), for $I_o<I_o'$ the rms current in T_1 is calculated as following.

$$\frac{\theta-\varphi}{\pi-\varphi} = \frac{i_L(\theta)-0}{-i_L(0)-0} \quad => \quad i_L(\theta) = -i_L(0)\frac{\theta-\varphi}{\pi-\varphi}$$

$$I_{rms,T,ib,LE} = \sqrt{\frac{1}{2\pi}\int_\varphi^\pi i_L(\theta)^2\,d\theta} = \sqrt{i_L(0)^2\frac{(\pi-\varphi)}{3}\frac{1}{2\pi}} = \sqrt{\frac{1}{6}i_L(0)^2\left(1-\frac{\varphi_{LE}}{\pi}\right)} \quad (4.49)$$

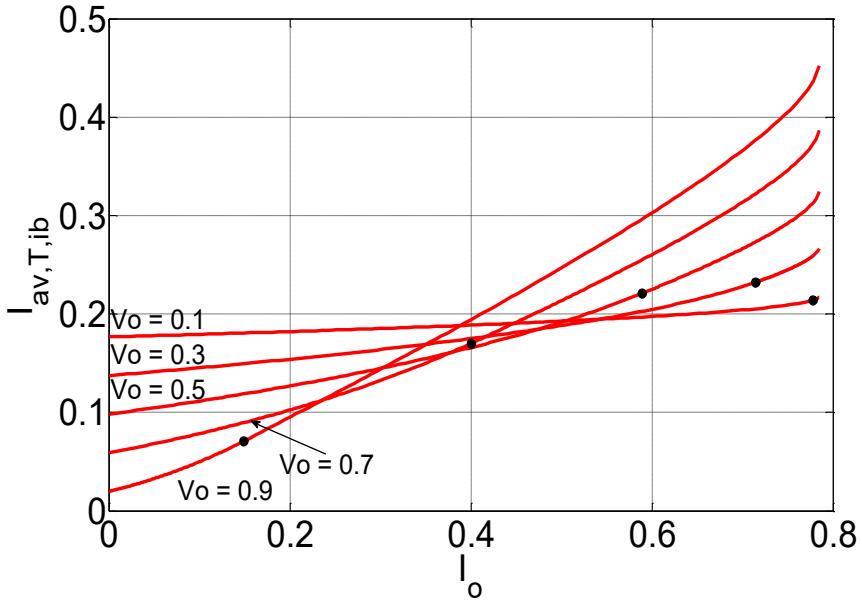
Looking the Fig. 4.14 (b), for $I_o<I_o'$ the rms current in D_1 is calculated as following.

1)

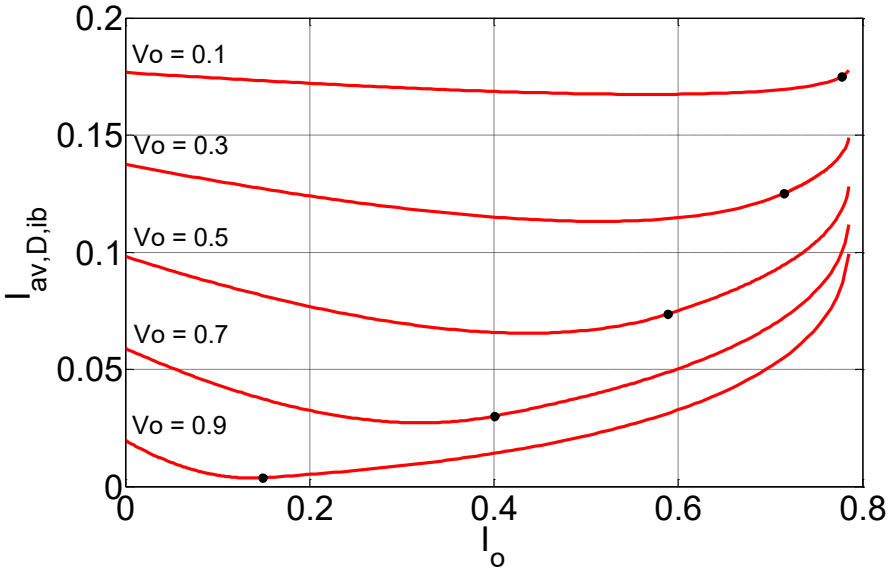
$$\frac{\theta-0}{\alpha-0} = \frac{i_L(\theta)-i_L(0)}{-i_L(\alpha)-i_L(0)} \quad => \quad i_L(\theta) = i_L(0)+[i_L(\alpha)-i_L(0)]\frac{\theta}{\alpha}$$

$$i_L(\theta)^2 = i_L(0)^2 + [i_L(\alpha)-i_L(0)]^2\frac{\theta^2}{\alpha^2} + 2i_L(0)[i_L(\alpha)-i_L(0)]\frac{\theta}{\alpha}$$

$$\int_0^\alpha i_L(\theta)^2\,d\theta = [i_L(\alpha)-i_L(0)]^2\frac{\alpha}{3} + i_L(0)i_L(\alpha)\alpha \quad (4.50)$$



(a)



(b)

Fig.4.16. DAB average currents in transistors (a) and diodes (b) of the input bridge vs. load current.

2)

$$\frac{\theta-\alpha}{\varphi-\alpha}=\frac{i_L(\theta)-i_L(\alpha)}{0-i_L(\alpha)} \quad \Rightarrow \quad i_L(\theta)=i_L(\alpha)-i_L(\alpha)\frac{\theta-\alpha}{\varphi-\alpha}$$

$$i_L(\theta)^2=i_L(\alpha)^2+i_L(\alpha)^2\frac{(\theta-\alpha)^2}{(\varphi-\alpha)^2}-2i_L(\alpha)^2\frac{\theta-\alpha}{\varphi-\alpha}$$

$$\int_\alpha^\varphi i_L(\theta)^2\,d\theta=i_L(\alpha)^2\frac{\varphi-\alpha}{3} \qquad (4.51)$$

From eqs. (4.50) and (4.51) the rms current in D_1 is

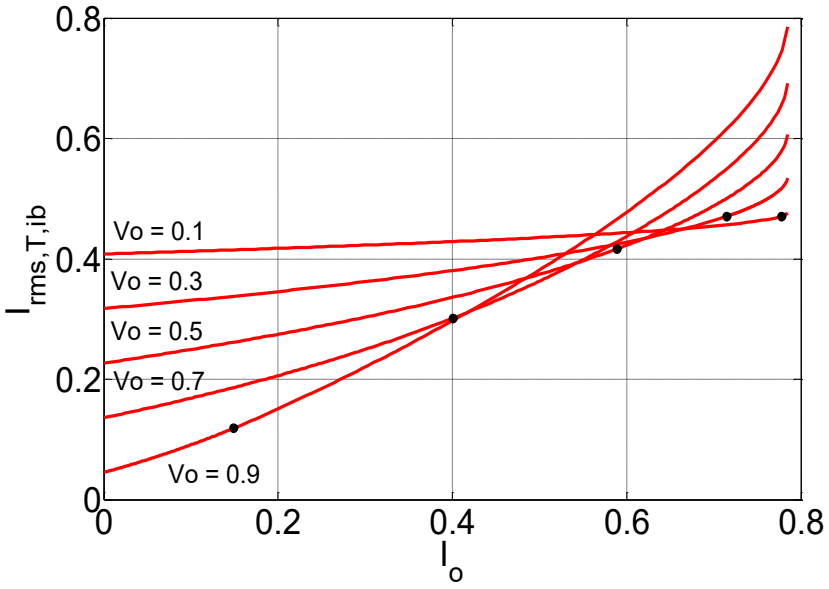
$$I_{rms,D,ib,LE} = \sqrt{\frac{1}{6}\left[i_L(\alpha)^2\left(\frac{\varphi_{LE}}{\pi} - \frac{\alpha}{\pi}\right) + (i_L(\alpha)^2 + i_L(0)^2)\frac{\alpha}{\pi} + i_L(\alpha)i_L(0)\frac{\alpha}{\pi}\right]} \qquad (4.52)$$

Looking the Fig. 4.14 (c), for $I_o > I_o$' the rms current in T_1 is calculated as following.

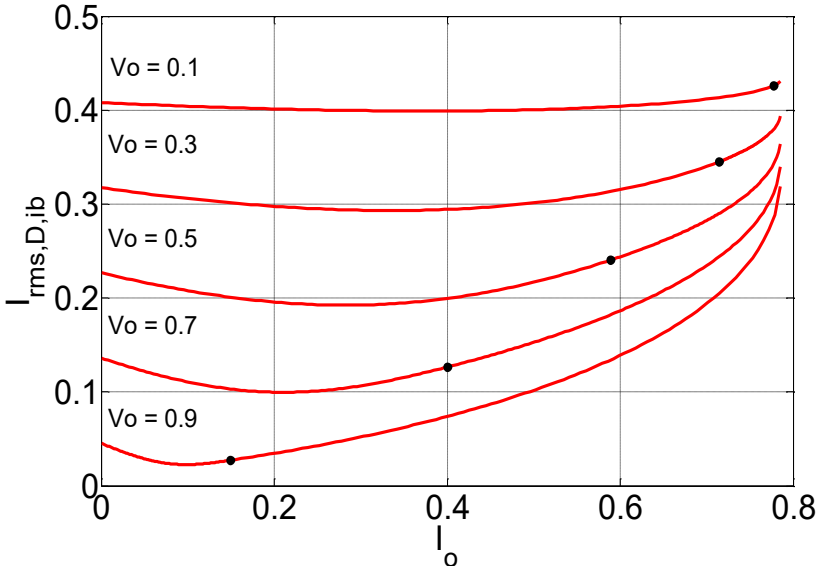
1)

$$\frac{\theta-\varphi}{\alpha-\varphi} = \frac{i_L(\theta)-0}{-i_L(\alpha)-0} \qquad => \qquad i_L(\theta) = i_L(\alpha)\frac{\theta-\varphi}{\alpha-\varphi}$$

$$\int_{\varphi}^{\alpha} i_L(\theta)^2\, d\theta = i_L(\alpha)^2\frac{\alpha-\varphi}{3} \qquad (4.53)$$



(a)



(b)

Fig.4.17. DAB rms currents in the transistors (a) and the diodes (b) of the input bridge vs. load current.

2)

$$\frac{\theta-\alpha}{\pi-\alpha}=\frac{i_L(\theta)-i_L(\alpha)}{-i_L(0)-i_L(\alpha)} \quad => \quad i_L(\theta)=i_L(\alpha)-[i_L(\alpha)+i_L(0)]\frac{\theta-\alpha}{\pi-\alpha}$$

$$i_L(\theta)^2=i_L(\alpha)^2+[i_L(\alpha)+i_L(0)]^2\frac{(\theta-\alpha)^2}{(\pi-\alpha)^2}-2i_L(\alpha)[i_L(\alpha)+i_L(0)]\frac{\theta-\alpha}{\pi-\alpha}$$

$$\int_\alpha^\pi i_L(\theta)^2\,d\theta=i_L(\alpha)^2(\pi-\alpha)+[i_L(\alpha)+i_L(0)]^2\frac{(\pi-\alpha)}{3}-i_L(\alpha)[i_L(\alpha)+i_L(0)](\pi-\alpha) \quad (4.54)$$

From eqs. (4.53) and (4.54) the rms current in T_1 is

$$I_{rms,T,ib,GR}=\sqrt{\frac{1}{6}\left[i_L(\alpha)^2\left(\frac{\alpha}{\pi}-\frac{\varphi_{GR}}{\pi}\right)+(i_L(\alpha)^2+i_L(0)^2)\left(1-\frac{\alpha}{\pi}\right)-i_L(\alpha)i_L(0)\left(1-\frac{\alpha}{\pi}\right)\right]} \quad (4.55)$$

Looking the Fig. 4.14 (d), for $I_o>I_o$' the rms current in D_1 is calculated as following.

$$\frac{\theta-0}{\varphi-0}=\frac{i_L(\theta)-i_L(0)}{0-i_L(0)} \quad => \quad i_L(\theta)=i_L(0)-i_L(0)\frac{\theta}{\varphi}$$

$$i_L(\theta)^2=i_L(0)^2+i_L(0)^2\frac{\theta^2}{\varphi^2}-2i_L(0)^2\frac{\theta}{\varphi}$$

$$I_{rms,D,ib,GR}=\sqrt{\frac{1}{2\pi}\int_0^\varphi i_L(\theta)^2\,d\theta}=\sqrt{\frac{1}{6}i_L(0)^2\frac{\varphi_{GR}}{\pi}} \quad (4.56)$$

Eqs. (4.49), (4.52), (4.55) and (4.56) are plotted in Fig. 4.17 as a function of I_o. The traces of Figs. 4.16 and 4.17 show that both the average and the rms values of the current in the transistors of the input bridge surpass those of the current in the diodes, with the exception for $I_o=0$ where the two currents are equal.

4.3 Soft-switching capabilities

The circuitry of the DAB converter, including the soft-switching capacitors, is drawn in Fig. 4.18. The converter operates in continuous conduction mode; then, both the input and output voltages across the inductance L have a square waveform [53]-[55]. The soft switching capabilities are analyzed only for the DAB operating in forward mode of buck type.

Waveforms of voltage and current, and the switches that are conducting for the DAB converter are drawn in Figs. 4.19 (a) and (b). It is visible that the commutations are at $\theta=0$ and $\theta=\pi$ for the input bridge, and at $\theta=\alpha$ and at $\theta=\alpha+\pi$ for the output bridge. In the second half period, the commutations are the same present in the first half period $[0\div\pi]$. Therefore, the analysis can be limited to the first half period; in particular to the instant $\theta=0$ for the input bridge, when T_1 and T_4 are turned off and T_2 and T_3 are turned on, and to the instant $\theta=\alpha$ for the output bridge, when T_6 and T_7 are turned off and T_5 and T_8 are turned on. As reported in Tab. 4.1, at steady-state, the current i_L at $\theta=0$ and at $\theta=\alpha$ is:

$$i_L(0)=-\frac{V_i}{\omega L}\frac{\pi}{2}\left[\left(2\frac{\alpha}{\pi}-1\right)\frac{V_o}{V_i}+1\right] \quad (4.57)$$

$$i_L(\alpha)=\frac{V_i}{\omega L}\frac{\pi}{2}\left[2\frac{\alpha}{\pi}-1+\frac{V_o}{V_i}\right] \quad (4.58)$$

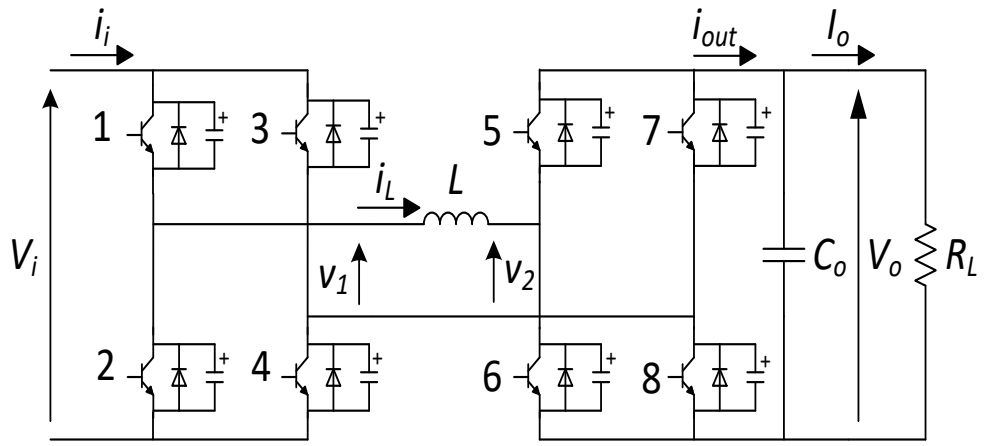


Fig.4.18. DAB converter circuitry with soft-switching capacitors.

Unlike the SAB, the current at the instant when the switches are commutated can be positive or negative. Then both the cases have to be analyzed.

Considering the operative situation under investigation, at $\theta = 0$ the current i_L is always negative while at $\theta = \alpha$ it is positive for

$$\frac{\alpha}{\pi} > \frac{1}{2}\left(1 - \frac{V_o}{V_i}\right) \tag{4.59}$$

Both the cases are analyzed for the output bridge.

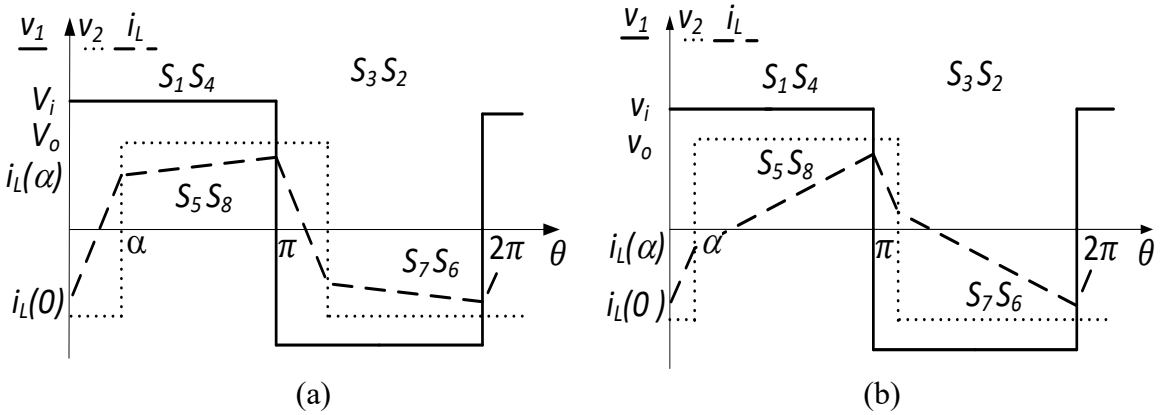


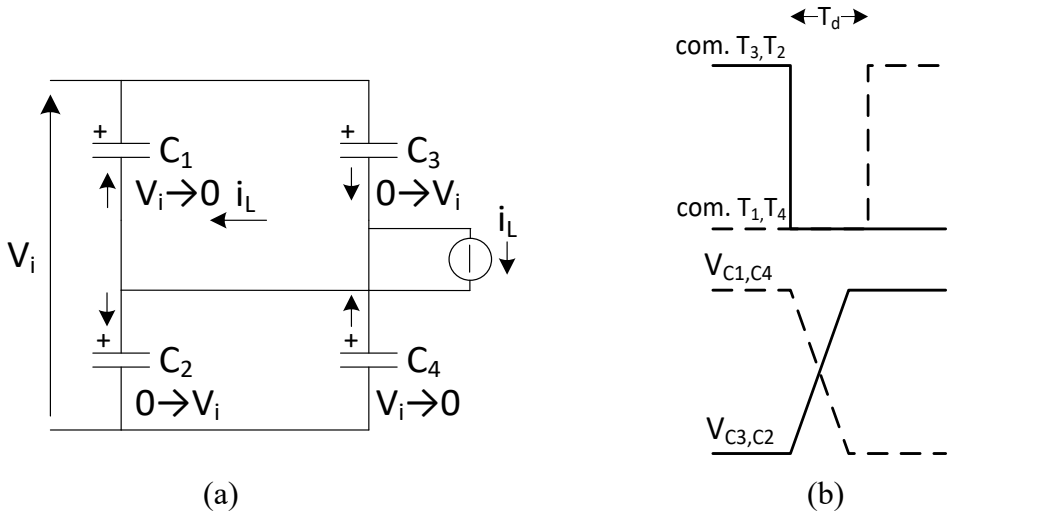
Fig.4.19. DAB current and voltage waveforms: (a) for $i_L(\alpha) > 0$ and (b) for $i_L(\alpha) < 0$.

4.3.1 Input bridge switching

Let us examine the commutations of the input bridge. At $\theta = 0$, T_3 and T_2 are turned off and their commutation is soft thanks to C_3 and C_2 which are discharged. The commutation is hence of ZVS type. Within the dead-time, C_3 and C_2 charge at V_i while C_1 and C_4, which at $\theta = 0$ were charged at V_i, discharge according to the scheme of Fig. 4.20 (a), where the inductance L behaves as a current source of value i_L.

During the dead-time, the current i_L enters into C_3 and C_2, and exits from C_1 and C_4. Since the change of voltage across C_1 equates that across C_4 and the same takes place for C_2 and C_3, an equal current, given by half of i_L, flows in the capacitors. By assuming that i_L is constant during the capacitor voltage transients, the latter ones are linear as illustrated in Fig. 4.20 (b). The capacitor voltage transients

must complete within the dead-time T_d. At the end of the dead-time, T_1 and T_4 are turned on and their commutation is also soft because the current i_L is negative and, by flowing into diodes D_1 and D_4, keeps low the voltage across T_1 and T_4. Hence the commutations at $\theta = 0$ are of ZVS type for all the transistors of the input bridge. The commutations at $\theta = \pi$ occur with the same mechanism as at $\theta = 0$, with the role of switches and capacitors exchanged. Therefore, the input bridge exhibits soft-switching capabilities.



(a) (b)

Fig.4.20. (a) current flow and (b) voltage transients across the capacitors during the dead-time at $\theta = 0$.

4.3.2 Output bridge switching

Let us analyze the commutations of the output bridge under the condition $i_L(\alpha) > 0$. At $\theta = \alpha$, T_7 and T_6 are turned off and, at the end of the dead-time, T_5 and T_8 are turned on. Both the commutations are soft since they occur under the same conditions as for the input bridge. An equal situation occurs for the commutations at $\theta = \pi + \alpha$. Therefore, for $i_L(\alpha) > 0$, the output bridge exhibits soft-switching capabilities as well.

Let us now analyze the commutations of the output bridge under the condition $i_L(\alpha) < 0$. At $\theta = \alpha$, T_7 and T_6 are turned off and their commutations are still soft thanks to diodes D_7 and D_6. However, during the dead-time, diodes D_7 and D_6 are conducting so that C_7 and C_6 stay discharged and C_5 and C_8 do not discharge. Therefore, at the end of the dead-time, T_5 and T_8 are turned on with charged capacitors connected in parallel; this causes high peaks of current across the transistors so that this working condition must be avoided. Hence, the insertion of capacitors is not feasible. An equal situation occurs for the commutation at $\theta = \pi + \alpha$. Therefore the output bridge does not exhibit soft-switching for $i_L(\alpha) < 0$. The summary of the output bridge commutations is reported in Tab. 4.2.

As a result, it comes out that condition (4.59) must be met to achieve soft-switching for both the bridges of the DAB converter (termed as full soft-switching). Otherwise soft-switching is achieved only for the input bridge (termed as partial soft-switching). Condition (4.59), expressed in terms of output voltage, imposes a lower limit to the load current to get full soft-switching. The limit is shown in Fig. 4.21, where, here and later on, output voltages and currents in the figures are normalized to V_i and $V_i/\omega L$, respectively. According to Fig. 4.21, the limit of the load current increases as the output voltage decreases.

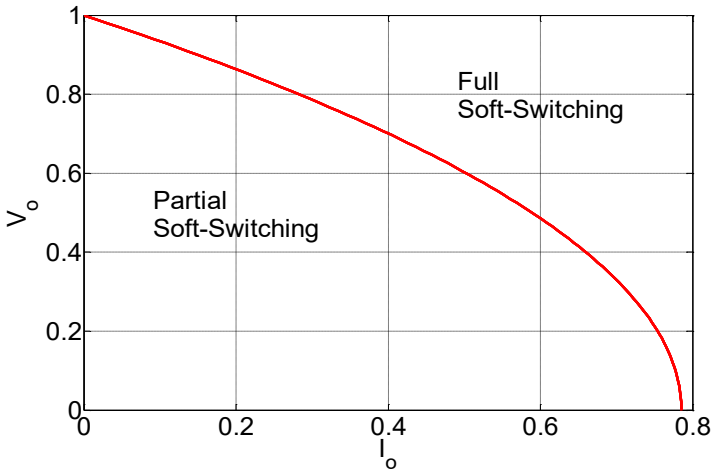


Fig.4.21. DAB converter soft-switching limit.

Tab 4.2. Summary of the output bridge commutations

	$i_L(\alpha) < 0$		$i_L(\alpha) > 0$	
	$\theta = \alpha$	$\theta = \alpha + \pi$	$\theta = \pi$	$\theta = \alpha + \pi$
T_5	HARD	ZVS	ZVS	ZVS
T_6	ZVS	HARD	ZVS	ZVS
T_7	ZVS	HARD	ZVS	ZVS
T_8	HARD	ZVS	ZVS	ZVS

4.4 Comparative analysis between SAB and DAB

A comparative analysis of the design characteristics derived for the SAB and DAB converters in this and in the previous chapter is here executed. With regard to the output current, Figs. 3.7, 3.8, 4.10 and 4.11 point out that the SAB converter exhibits better characteristics than the DAB converter since both the rms value and the ripple of the alternating component of the output current are lower along the load current range. In particular, these values of current become zero at zero load current while they remain appreciable for the DAB converter. The reason is due to the fact that the output current of the SAB converter takes only positive amplitudes while it takes both positive and negative amplitudes in the DAB converter.

A similar outcome is obtained for the input current. As Figs. 3.10 and 4.13 show, the SAB converter has a lower rms value of the alternating component of the input current along the load current range than the DAB converter. Like for the output current, with the SAB converter this value becomes zero at zero load current.

With regard to the current solicitations in the devices, Figs. 3.12, 3.13, 4.16 and 4.17 show that transistors and diodes of the SAB converter are less solicited at low load currents whilst those of the DAB converter are less solicited at high load currents even if only a little difference exists.

As a conclusion, for applications where unidirectional power flow of buck type is required, the results indicate that the design characteristics of the SAB converter outdo completely those of the DAB converter. However, the SAB converter suffers from the shortcoming of being unable to

deliver high load currents at high output voltages, while the DAB converter is able to operate also in these conditions. This is a consequence of the larger operating interval at high output voltages where the SAB converter operates in the discontinuous current mode. Actually, as Figs. 3.4 and 4.3 show, only when the output voltage is a small fraction of the input voltage, the SAB converter delivers to the load a current that is comparable to the DAB converter.

4.5 Dynamic model

The average state method AVG, as already described for the SAB, is used to find the model of the DAB converter. The circuit of the DAB converter is analysed during each switching interval. However, the analysis of only half of the waveform is necessary because the voltage waveform in the transformer is symmetrical. Even if other methods more accurate are present in literature [56],[57], this method is simpler and enough for the analysis under evaluation.
Then, looking at Fig. 4.22, which refers to the DAB operating in buck mode, only the intervals t_1 and t_2 are considered.

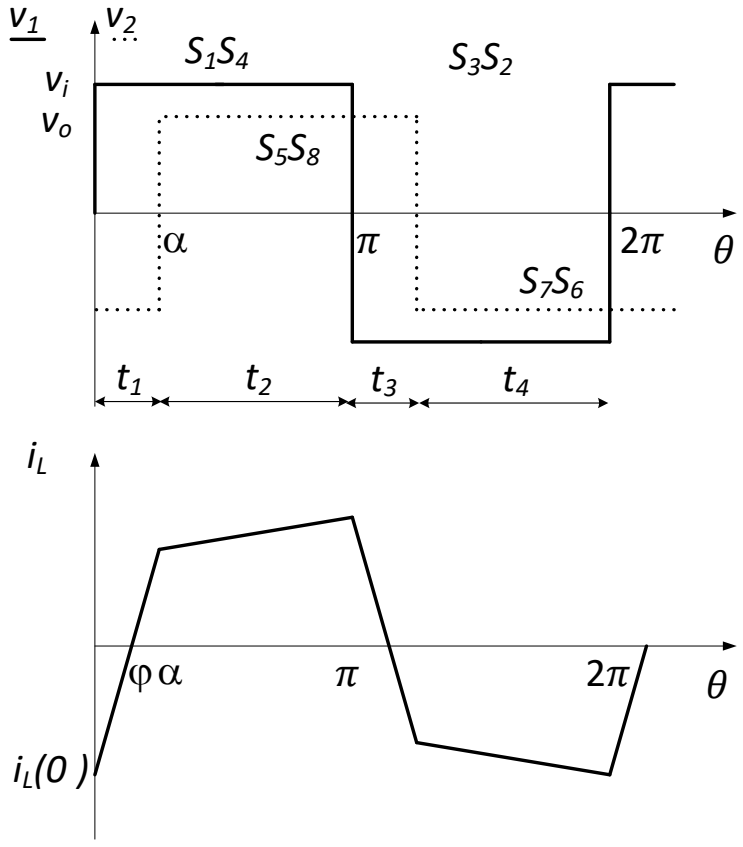
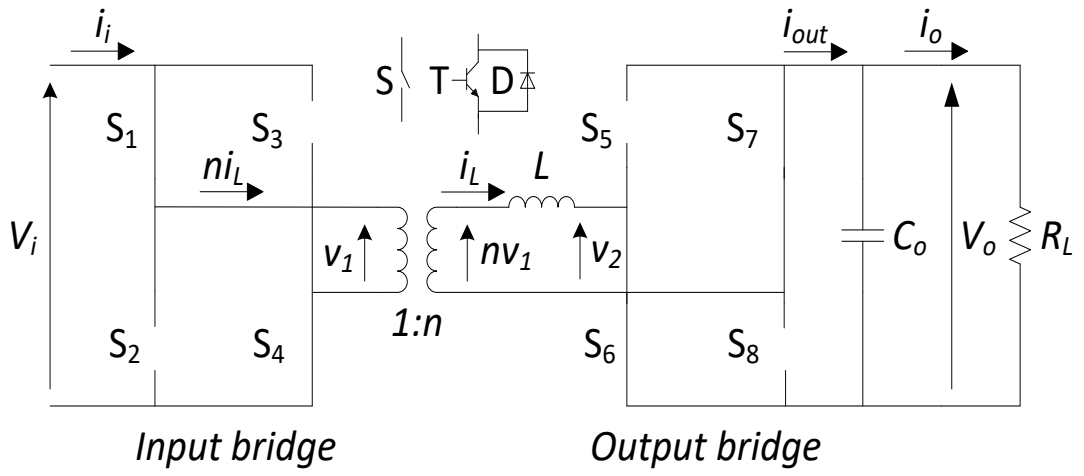
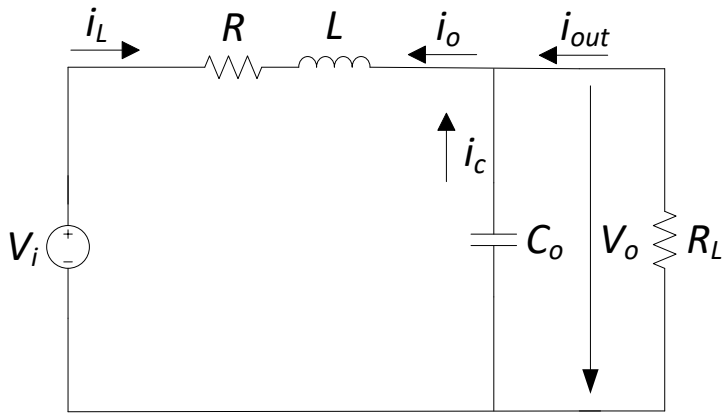


Fig. 4.22. DAB converter current and voltage waveforms with α > α' in buck mode

Let us consider the interval t_1. The DAB schematic for this interval is shown in Fig. 4.23 (a). Its equivalent circuit, considering a transformer ratio equal to 1, is shown in Fig. 4.23 (b).



(a)



(b)

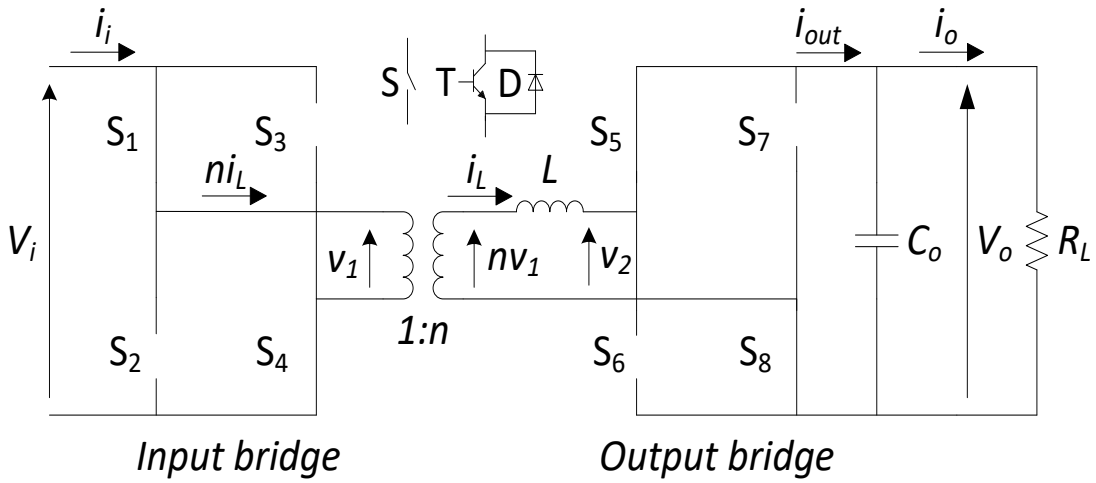
Fig. 4.23 DAB schematic (a) and its equivalent circuit (b) during the interval t_1.

Appling the Kirchhoff laws KVL and KCL to the circuit of Fig. 4.23 (b) the derived equations are:

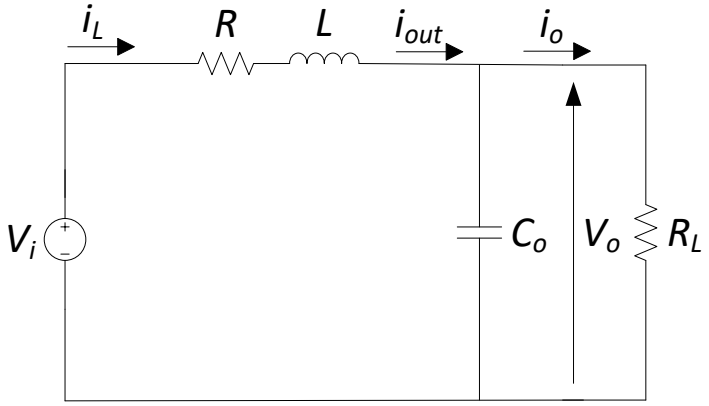
$$v_i - L\frac{di_L}{dt} - Ri_L + v_o = 0 \tag{4.60}$$

$$C_o\frac{dv_o}{dt} + \frac{v_o}{R_L} + i_L = 0 \tag{4.61}$$

Let us consider the interval t_2. The DAB schematic for this interval is shown in Fig. 4.24 (a) and its equivalent circuit is shown in Fig. 4.24 (b).



(a)



(b)

Fig. 4.24 DAB schematic (a) and its equivalent circuit (b) during the interval t_2.

The equations derived from the circuit of Fig. 4.24 (b) are:

$$v_i - L\frac{di_L}{dt} - Ri_L - v_o = 0 \tag{4.62}$$

$$C_o\frac{dv_o}{dt} + \frac{v_o}{R_L} - i_L = 0 \tag{4.63}$$

Eqs. (4.60)-(4.63) can be expressed in matrix form as it follows.

INTERVAL 1

$$\frac{dx}{dt} = A_1 x + B_1 v_i$$

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_o \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \frac{1}{L} \\ -\frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix}\begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_i \tag{4.64}$$

$$A_1 = \begin{bmatrix} -\frac{R}{L} & \frac{1}{L} \\ -\frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix} \qquad B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{4.65}$$

INTERVAL 2

$$\frac{dx}{dt} = A_2 x + B_2 v_i$$

$$\frac{d}{dt}\begin{bmatrix} i_L \\ v_o \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix}\begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_i \tag{4.66}$$

$$A_2 = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix} \qquad B_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{4.67}$$

where the vector with the state variables, which are the inductance current and the capacitor voltage, is indicated with x. The lowercase letter, e.g. v_i, is used to indicate the steady-state value plus a small variation. The capital letter is used to indicate the steady-state value. A bar superscript indicates the small variation value.

The average behaviour of the circuit, using the duty cycle d, is given by

$$\frac{d}{dt}x = [A_1 d_1 + A_2 d_2]x + [B_1 d_1 + B_2 d_2]v_i =$$

$$= [A_1 d + A_2(1-d)]x + [B_1 d + B_2(1-d)]v_i \tag{4.68}$$

where $d_1 = \frac{t_1}{T/2} = d$ and $d_2 = \frac{t_2}{T/2} = 1 - d_1 = 1 - d$

The small signal model for the DAB operating in buck mode is obtained:

- Introducing small variations of the state space variables $\tilde{x}$, independent variables $\tilde{v}$ and duty cycle $\tilde{d}$. For example, x=X+$\tilde{x}$ where the capital letter is referred to steady state.
- Dividing the alternative component from the continuous component (putting equal to zero the steady state components because their derivative is zero).
- Neglecting terms containing products of small variations.

$$\frac{d}{dt}\tilde{x} = \left[A_1 D\tilde{x} + A_1\tilde{d}X + A_2\tilde{x} - A_2 D\tilde{x} - A_2\tilde{d}X)\right] + \left[B_1 D\tilde{v} + B_1\tilde{d}V + B_2\tilde{v} - B_2 D\tilde{v} - B_2\tilde{d}V\right]$$

$$\frac{d}{dt}\tilde{x} = [A_1 D + A_2(1-D)]\tilde{x} + A_1\tilde{d}X - A_2\tilde{d}X \; + [B_1 D + B_2(1-D)]\tilde{v} + B_1\tilde{d}V - B_2\tilde{d}V$$

$$A = A_1 D + A_2(1-D) \tag{4.69}$$

$$B = B_1 D + B_2(1-D) \tag{4.70}$$

$$\frac{d}{dt}\tilde{x} = A\tilde{x} + (A_1 - A_2)X\tilde{d} \; + B\tilde{v} + (B_1 - B_2)\tilde{d}V$$

$$\frac{d}{dt}\tilde{x} = A\tilde{x} + B\tilde{v} + [(A_1 - A_2)X + (B_1 - B_2)V]\tilde{d}$$

Using the Laplace transformation:

$$s\tilde{x} = A\tilde{x} + B\tilde{v} + [(A_1 - A_2)X + (B_1 - B_2)V]\tilde{d} \tag{4.71}$$

Then, substituting eqs. (4.65) and (4.67) in (4.69) and (4.70)

$$A = A_1 D + A_2(1 - D) = \begin{bmatrix} -\frac{R}{L} & \frac{2D-1}{L} \\ -\frac{2D+1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix} \tag{4.72}$$

$$B = B_1 D + B_2(1 - D) = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{4.73}$$

and (4.65), (4.67), (4.72) and (4.73) in (4.71) it is obtainable eq. (4.74) of the system under analysis.

$$s\begin{bmatrix} \widetilde{i_L} \\ \widetilde{v_o} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \frac{2D-1}{L} \\ -\frac{2D+1}{C_o} & -\frac{1}{R_L C_o} \end{bmatrix}\begin{bmatrix} \widetilde{i_L} \\ \widetilde{v_o} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}\widetilde{v_i} + \begin{bmatrix} \frac{2V_o}{L} \\ -\frac{2I_L}{C_o} \end{bmatrix}\tilde{d} \tag{4.74}$$

$$s\widetilde{i_L} = -\frac{R}{L}\widetilde{i_L} + \frac{2D-1}{L}\widetilde{v_o} + \frac{1}{L}\widetilde{v_i} + \frac{2V_o}{L}\tilde{d} \tag{4.75}$$

$$s\widetilde{v_o} = -\frac{2D+1}{C_o}\widetilde{i_L} - \frac{1}{R_L C_o}\widetilde{v_o} - \frac{2I_L}{C_o}\tilde{d} \tag{4.76}$$

The control to output current transfer function is obtainable from eq. (4.75) with the hypothesis that the variations of the input and output voltages are zero $\widetilde{v_o} = \widetilde{v_i} = 0$.

$$G_{i-d} = \frac{\widetilde{i_L}}{\tilde{d}} = \frac{2V_o}{R+sL} \tag{4.77}$$

The output current to DC voltage transfer function is obtainable from eq. (4.76) with the hypothesis that the variations of the input voltage and the duty cycle are zero $\widetilde{v_i} = \tilde{d} = 0$.

$$G_{v_o-i} = \frac{\widetilde{v_o}}{\widetilde{i_L}} = \frac{R_L(1-2D)}{1+sR_L C_o} \tag{4.78}$$

The hypotheses assumed are valid for the same reasons explained for the SAB.

4.6 Simulation and experimental results

In order to realize a prototype of SST, a DAB converter prototype is realized to validate the analysis done in the previous paragraphs. The use of the DAB topologies in an SST technology assumes that the application of interest requests a bidirectional power flow, unlike in the SAB converter where an unidirectional power flow is considered. In addition, even if in this analysis only the buck operation mode is considered, the DAB converter can operate in boost operation mode. The functioning of the DAB has been considered at full power in the simulation while the experimental setups has been designed to operate at reduced power with the DAB operating in forward mode.

4.6.1 Simulation results

The system is supplied by a PFC rectifier which convert the 220 Vrms AC grid voltage into a 370 Vpeak DC bus voltage. The DAB output voltage is chosen to be used in a variety of applications, in particular battery chargers or light DC loads. The transformer parameters are reported in Appendix A. The inductance L is composed by the transformer inductance and an extra inductance inserted to reduce the current ripple.

Let us consider the same requirements and parameters used to design the SAB converter. Their values are listed in Tab. 4.3.

TAB. 4.3. DAB CONVERTER PARAMETERS

Parameter	Value	Unit
V_i	370	V_{peak} DC
V''_o (referred to secondary)	60	V_{peak} DC
P_{o_max}	1	kW
f_{sw}	10	kHz
L	100u	H
C_o	1000u	F
Transformer ratio n	5.71	-
V_o (referred to primary)	343	V_{peak} DC
V_o/ V_i	0.926	-

- Load resistance

$$R_o = \frac{V''_o{}^2}{P_o} = 3.6\ \Omega$$

- Output currents calculation

Considering the requirements of the project and the parameters, at $\alpha = \pi/2$, the maximum current results in

$$I_{o,max} = \frac{V_i}{\omega L}\pi\frac{\alpha}{\pi}\left(1 - \frac{\alpha}{\pi}\right) = 46.25\ A$$

$$I''_{o,max} = 264.8\ A$$

However considering the maximum power listed in Tab. IV the maximum current is

$$I''_{out\_max\_load} = \frac{P_{out\_max}}{V_{out}} = 16.7\ A$$

$$I_{out\_max\_load} = 2.92\ A$$

which corresponds to an α equal to

$$\alpha = \frac{\pi - \sqrt{\pi^2 - 4\frac{\omega L\pi}{V_i} I_{out,max\_load}}}{2} = 0.05\ rad$$

Then, considering the command variable α, it is clear that the DAB converter is not properly used for this type of applications. Compared to the maximum operating range of α, only a small part is used.

Therefore, the DAB converter is more suitable for other type of applications where, for example, the output current is higher and the converter transfers more power with equal output voltage or, the input voltage is lower with equal output power.

Then, considering also the experimental setup that will be presented in the next paragraph, a new application is treated. The input is supplied at reduced DC voltage and the output is kept at the same voltage as the previous application. The transformer ratio is set to 1. The converter operates in buck mode and the voltage ratio is 0.4. The new requirements and parameters are listed in Tab.4.4.

TAB. 4.4. DAB CONVERTER PARAMETERS

Parameter	Value	Unit
V_i	150	V_{peak} DC
V_o	60	V_{peak} DC
P_{o_max}	1	kW
f_{sw}	10	kHz
L	100u	H
C_o	1000u	F
Transformer ratio n	1	-
V_o/ V_i	0.4	-

- Load resistance

$$R_o = \frac{V''_o{}^2}{P_o} = 3.6\ \Omega$$

- Output current calculation

Considering the specifications of the project and the parameters, at $\alpha = \pi/2$, the maximum current derivable is

$$I_{o,max} = \frac{V_i}{\omega L}\pi\frac{\alpha}{\pi}\left(1-\frac{\alpha}{\pi}\right) = 18.75\ A$$

However considering the maximum power listed in Tab. IV the maximum current is

$$I_{out\_max\_load} = \frac{P_{out\_max}}{V_{out}} = 16.7\ A$$

which corresponds to an α equal to

$$\alpha = \frac{\pi - \sqrt{\pi^2 - 4\frac{\omega L\pi}{V_i} I_{out,max\_load}}}{2} = 1.05\ rad$$

The rms value of the alternating component of the output current is

$$I_{rms,o,GR} = \sqrt{\frac{1}{3}\left[i_L(\alpha)^2\left(1-\frac{\varphi_{GR}}{\pi}\right) + i_L(0)^2\left(1+\frac{\varphi_{GR}}{\pi}-\frac{\alpha}{\pi}\right) - i_L(\alpha)i_L(0)\left(1-\frac{\alpha}{\pi}\right)\right] - I_o^2} = 9.2\ A$$

with $i_L(\alpha)_{max\_load} = 2.58\ A$, $i_L(0)_{max\_load} = -32.53\ A$ and $\varphi_{GR} = 0.97$ rad.

The peak-to-peak output current ripple is $R_{o,max\_load} = -i_L(0) + |i_L(\alpha)| = 35.11\ A$.

- Input current calculation

The average value I_i of the input current is

$$I_{i,max\_load} = \frac{V_o}{V_i} I_{o,max\_load} = 6.68\ A$$

The rms value of the alternating component of the input current is

$$I_{rms,i,GR} = \sqrt{\frac{1}{3}\left[i_L(\alpha)^2\left(1-\frac{\varphi_{GR}}{\pi}\right) + i_L(0)^2\left(1-\frac{\alpha}{\pi}+\frac{\varphi_{GR}}{\pi}\right) - i_L(\alpha)i_L(0)\left(1-\frac{\alpha}{\pi}\right)\right] - I_i^2} = 17.86\ A$$

The peak-to-peak ripple R_i of the input current is $2i_L(0) = 65.06\ A$.

- Devices current calculation

The average currents in transistor T_1 and diode D_1 of the input bridge are

$$I_{av,T,ib,GR} = \left\{i_L(\alpha)\frac{(\alpha-\varphi)}{2} + [-i_L(0) + i_L(\alpha)]\frac{(\pi-\alpha)}{2}\right\}\frac{1}{2\pi} = 5.86\ \text{A}$$

$$I_{av,D,ib,GR} = -\frac{i_L(0)}{2}\varphi\frac{1}{2\pi} = 2.51\ \text{A}$$

The rms currents in T_1 and D_1 are

$$I_{rms,T,ib,GR} = \sqrt{\frac{1}{6}\left[i_L(\alpha)^2\left(\frac{\alpha}{\pi}-\frac{\varphi_{GR}}{\pi}\right) + (i_L(\alpha)^2 + i_L(0)^2)\left(1-\frac{\alpha}{\pi}\right) - i_L(\alpha)i_L(0)\left(1-\frac{\alpha}{\pi}\right)\right]} = 11.29A$$

$$I_{rms,D,ib,GR} = \sqrt{\frac{1}{6}i_L(0)^2\frac{\varphi_{GR}}{\pi}} = 7.38\ A$$

- PI coefficients calculation

For the calculation of the parameters of the PI regulators for current and voltage loops, the bandwidths are set equal to $f_{BWi} = 800\ Hz$ and $f_{BWv} = 30\ Hz$, respectively while the phase margin $m_\varphi = 70°$ has been set for both the loops. As for the SAB converter, in the calculation of the current loop parameters it is also considered the 2nd order low pass filter applied to the transduced output current which has the parameters

$$K_f = 1 \qquad f_{cut-off} = 2000\ Hz \qquad \xi = 0.7$$

The PI parameters are computed in:

$$K_i = 4e-3 \qquad t_{i,i} = 0.051\ ms \qquad K_v = 0.0821 \qquad t_{i,v} = 0.0013$$

The power and control circuits implemented in the simulation are shown in Fig. 4.25.
The components used in the simulation are ideal.

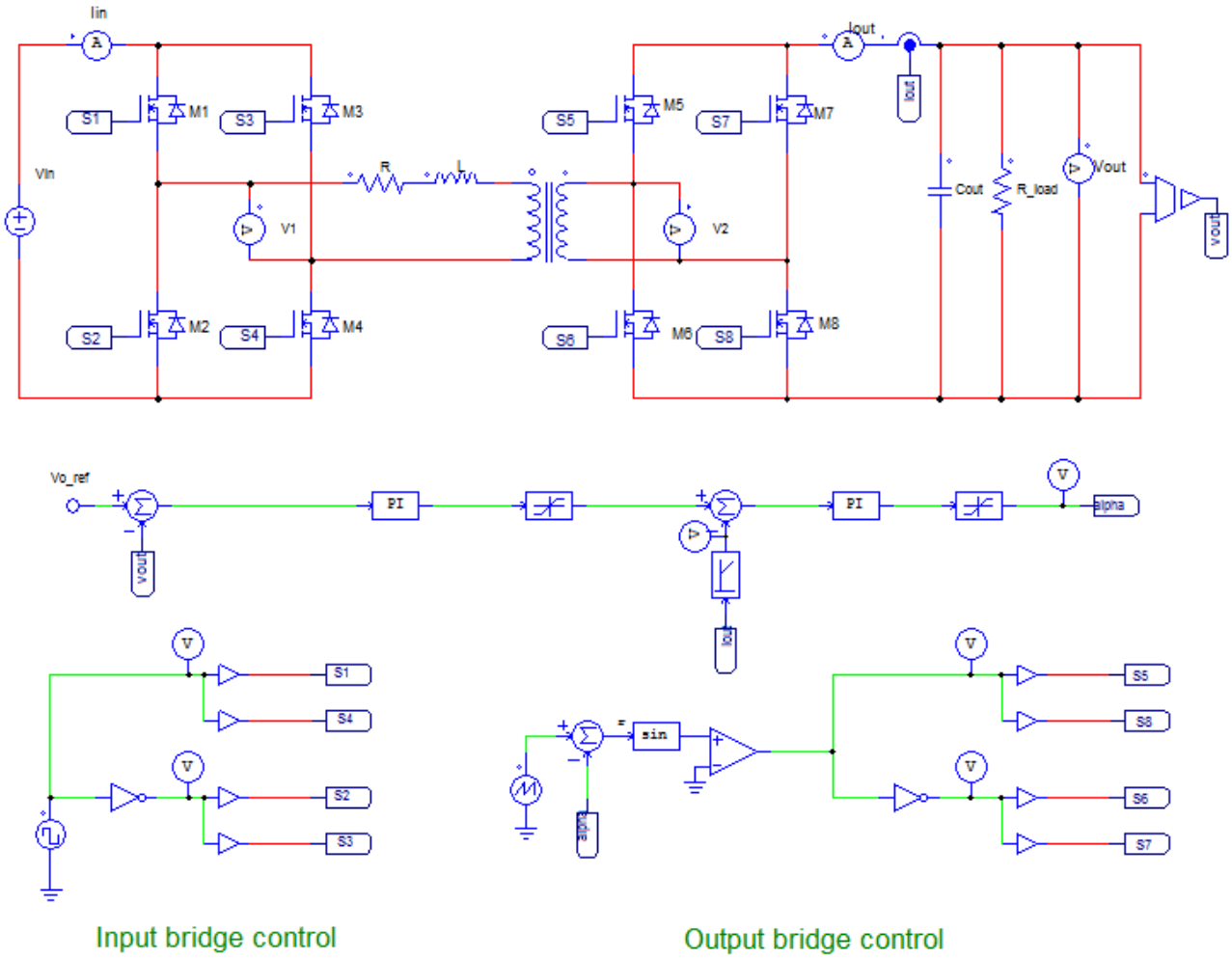
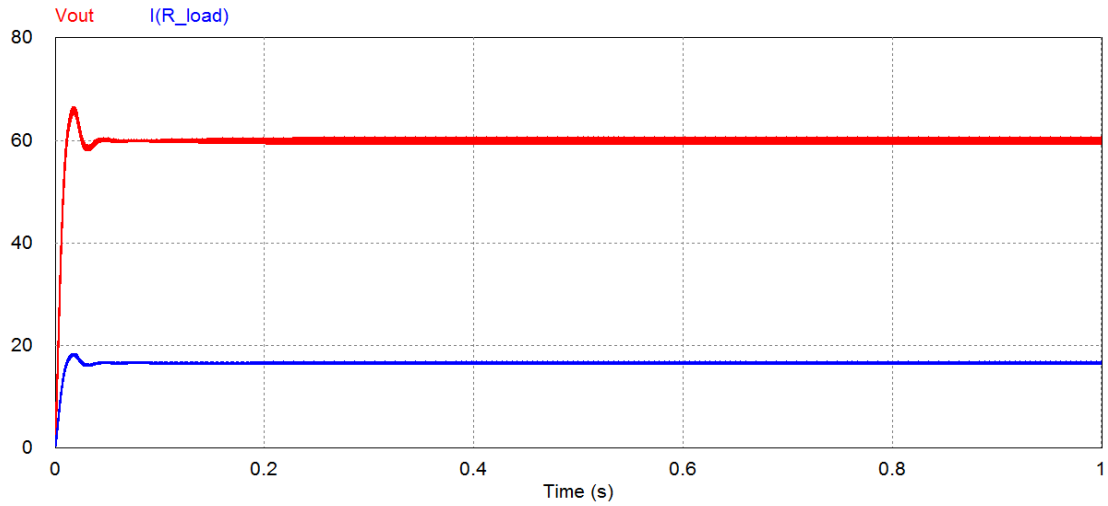
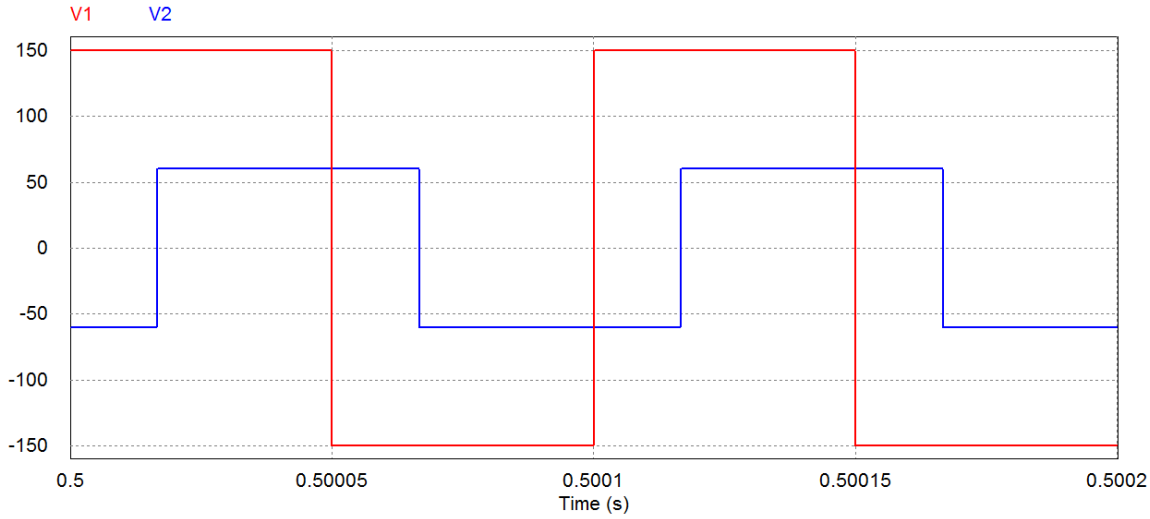


Fig.4.25 DAB power and control circuits

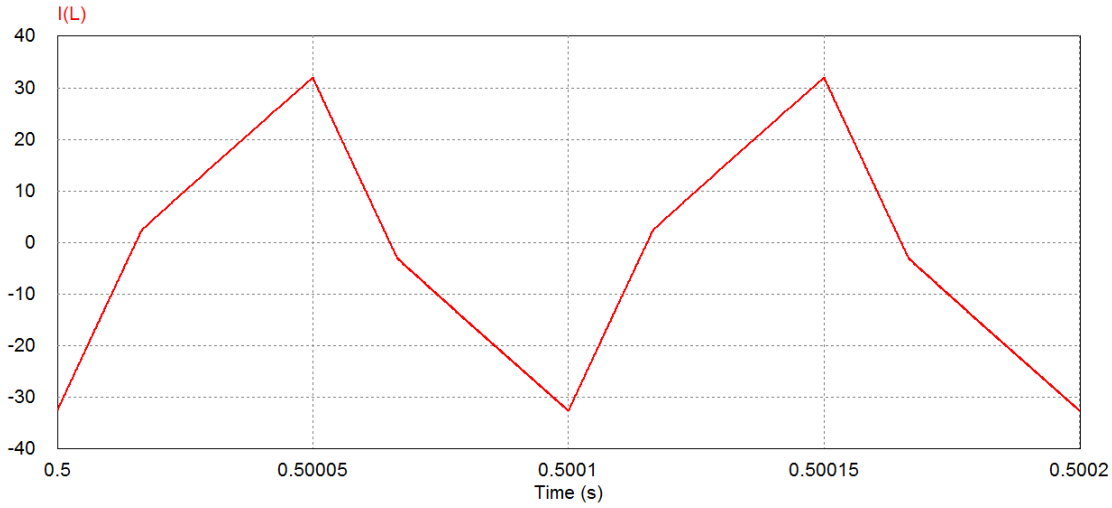
The results of the simulation are reported in Figs. 4.26 and 4.27. Fig.4.26(a) shows the output voltage and current and highlights that the control operates properly. Figs. 4.26(b) and (c) show the voltages applied to the transformer and the inductance current. The input, output and inductance currents are shown in Fig.4.27. In conclusion, the simulation results validate the mathematical analysis reported in the previous paragraphs.



(a)



(b)



(c)

Fig.4.26 (a) Output voltage and current, (b) voltages before (V1) and after (V2) the high frequency transformer and added inductance (c) inductance current.

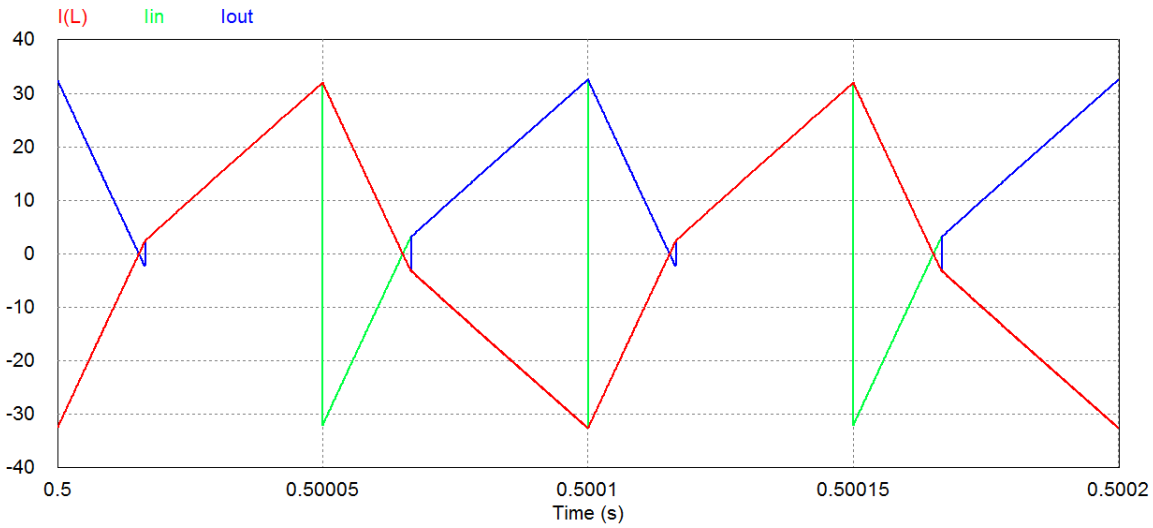


Fig.4.27 Input current (green), inductance current (red) and output current (blue).

4.6.2 Experimental results

The PCB of the input bridge is the same used as active bridge in the SAB prototype. The PCB used in the output bridge is designed in the same way as the PCB used in the input bridge. The characteristics of the components used are described in paragraph 3.5.2. The high frequency transformer used is the three winding transformer used for the three port converter experiments reported in chapter 5. As for the SAB converter only two windings are used. Both the bridges are connected to the high voltage windings and the turn ratio is 1. The inductance measured at one of the high voltage winding with the other high voltage winding short-circuited and the low voltage winding open is 14.6 uH and the resistance is 0.1 Ω. Unlike the SAB where the added inductance is inserted at low voltage side to avoid the circulating of a residual current, in the DAB converter it can be inserted in any of the two sides because the secondary bridge is active and the current circulates continuously. The added inductance is of 65 uH. Then, the total inductance is about 80uH and the parasitic resistance of 0.3 Ω. Two electrolytic capacitors of 1000 uF, 450 Vcc produced by EPCOS, are used at the input and output DC side. The system is feed using the DC power supply 6012B of HP. The power flow is controlled varying the phase shift between the legs of the input and the output bridge. The control algorithm is implemented using the Digital Signal Processor (DSP) TMS320F28335 produced by Texas Instruments. The experimental setup is shown in Fig. 4.28.

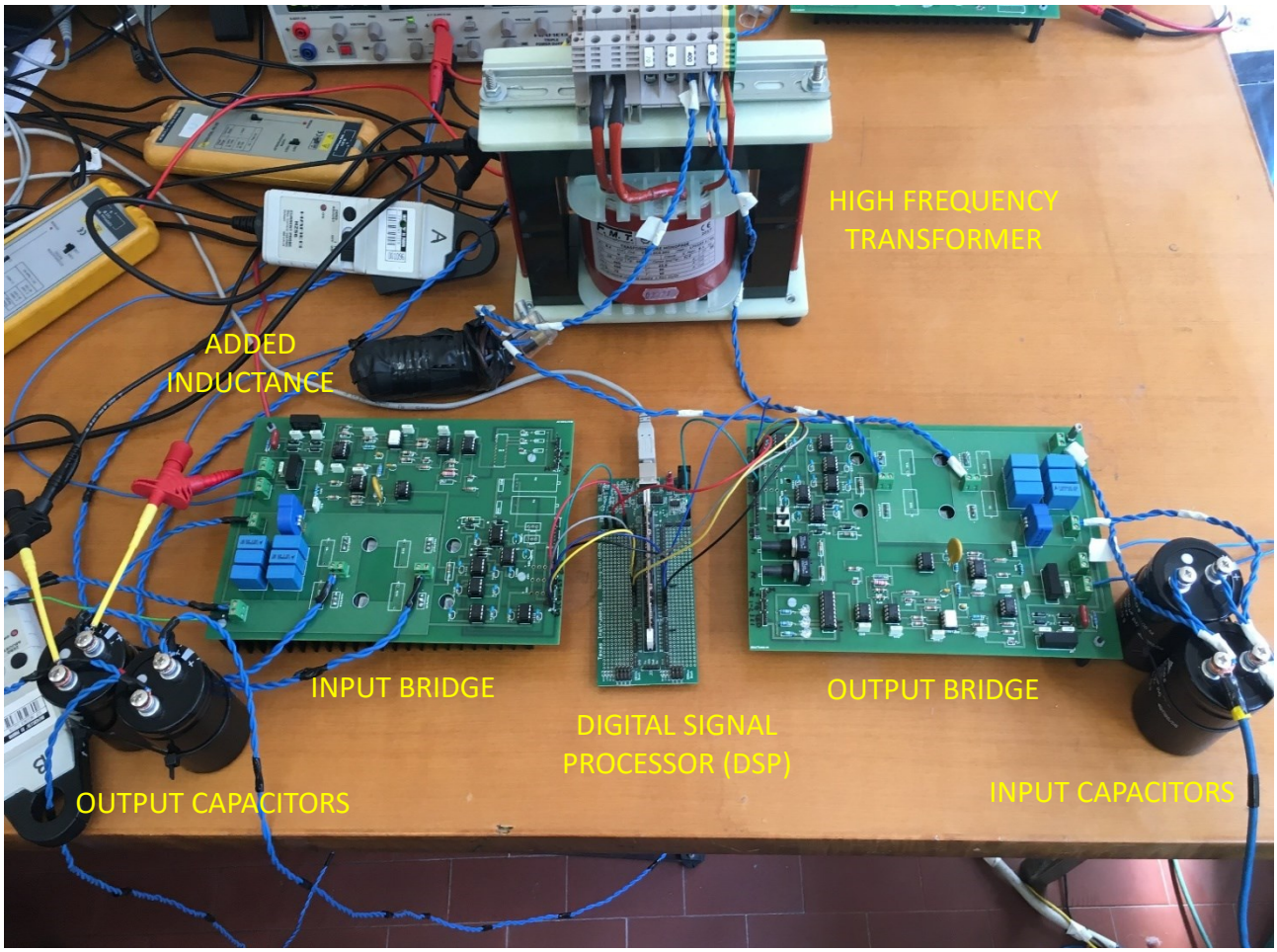


Fig. 4.28. Experimental setup of the DAB converter.

As for the SAB experiment the load resistance is of 5.6 Ω and the voltage reference is set to 24 V to have a power transfer of about 100 W. The input is feed at 42 V, a voltage low enough to get a reasonable use of the converter, as explained in the previous paragraph. The experimental results are shown in Figs.4.29 and 4.30. Fig. 4.29 shows the voltage V_1 at the output of the input bridge (violet), voltage V_2 at the input of the output bridge (green) and the inductance current (light blue). The voltage V_1 is slightly lower than the supply voltage because of the voltage drop across the MOSFETs and the connections. Looking the waveform of the voltage V_2, it has a small step when the diodes starts to conduct. This is due to the different voltage drop of the MOSFETs and the diodes. From the duration of the phase shift between the two voltage waveforms, the command variable α is computed in around 0.67 rad. The peak current is of 7.5 A. Its waveform is almost linear and it matches with the simulation results more than the SAB inductance current because in DAB the parasitic resistance is 4-5 times lower.

Fig.4.29 Voltage V_1 at the output of the input bridge (violet), voltage V_2 at the input of the output bridge (green) and inductance current(light blue).

The output voltage (green) and current (yellow) are shown in Fig. 4.30. The value of the voltage is 24 V as requested by the control. The current value is nearly 4.4 A. Then, the transferred power is about 106 W. The peaks in the current are disturbances that affect the current probe and due to the switching of the MOSFETs. The efficiency of the DAB, operating under the testing conditions, is 91-92%. The computed efficiency is a little lower than the SAB efficiency. The main reason of this difference is that, considering the command variables of the two converters under the same output operating conditions, the DAB converter is operating at light load. In addition, it must be considered that in DAB the switching losses are higher because it requires 8 switches to operate while the SAB requires only 4 switches.

Fig.4.30 Output voltage (green) and current (yellow), voltage V_1 (violet) and inductance current (light blue).

In conclusion, both the converters highlight an high efficiency, over 90%, in the tested operating condition. However, considering an equal input voltage and turn ratio of the transformer, the SAB converter is more suitable because nearly its full operative range can be exploited. Instead, the DAB converter is more suitable for applications where the output current is very high or for applications where it is required a boost operation mode or a bidirectional power flow, which can not be achieved with the SAB converter.

CHAPTER 5

Three Port Converter

The Isolated multiport DC-DC power converters (MPCs) are emerging as an effective solution to integrate a variety of energy delivery elements (EDEs), whether they are renewable energy sources (RESs) or energy storage devices (ESDs) or the mains, while keeping them isolated by means of a transformer operated at high frequency. Moreover, they accommodate for different loading patterns of the EDE-connected ports by implementing a centralized controller. For these reasons, MPCs are expected to be used in many applications such as when RESs are intended to supply the loads and are supported by either ESDs or the mains or both to ensure an uninterruptible service [58]-[64].

Even if MPCs could be thought of as a composition of a number of isolated two-port DC-DC converters (2PCs) such as Single Active Bridge (SAB) and Dual Active Bridge (DAB) converters, their overall functioning is somewhat more complex than 2PCs, with some ports powered by EDEs and commonly termed as inputs, and other ports feeding the loads and commonly termed as outputs. In principle, all the ports can be active in the sense that they can be equipped with active bridges, i.e. with DC-AC converters that are bidirectional and able to control the power flow. However, ports connected to loads that do not require a bidirectional energy flow can be passive in the sense that they can be equipped with passive bridges, i.e. with diode rectifiers. Most of RESs, like PV fields and wind plants, are also unidirectional EDEs but the relevant ports are active to control the power flowing out of them.

MCPs with passive ports can operate in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM), depending on whether all the ports are flowed by current continuously or not. By accounting for the fact that RESs deliver a maximum power that varies in a somewhat large range and that there is the convenience of utilizing all the power they make available, MCPs that integrate RESs often operate in DCM. Operation in DCM of an active port, moreover, has the merit of reducing the switching losses of the associated converter as its switches commutate at zero current.

Functioning and characteristics of MPCs operating in CCM can be found in the literature. Less attention, instead, has received the study of MPCs operating in DCM. It is the purpose of this chapter to face such an issue by investigating the power and control characteristics of an isolated three-port DC-DC converter (3PC) with two ports connected to EDEs, respectively to a RES and an ESD, and a port connected to the load through a passive bridge. More precisely, the chapter is focused on two DCM operations of 3PC, namely: i) full DCM (FDCM), with all the ports operating in DCM, and ii) mixed discontinuous conduction mode (MDCM), with the ESD-connected port operating in DCM and the other ports operating in CCM. Moreover, two working situations are analyzed, namely i) both EDEs deliver power to the load, and ii) RES concurrently delivers power to ESD and the load. The port power is defined as the average value of the power through the port over the supply period. The analysis of the two DCM operations is treated in the same way of the SAB and DAB converter. It is important to highlight that if both the port operates in CCM, considering the current waveforms, the analysis can be performed considering the fundamental harmonics as in literature is usually done.

Simulations conducted to verify the error between the real quasi piece linear current waveform and the first harmonic confirm that the approximation when both the ports are operating in CCM is acceptable.

5.1 SAB converter basics

The SAB converter is here reviewed as its functioning and characteristics provide the basics for investigating 3PC. The schematic of a SAB converter is drawn in Fig 3.1, where V_i is the direct voltage applied by an EDE to the input port of the SAB converter, S_j with j=1, 2, 3, 4 are the switches of the active input bridge (each of them made of transistor T_i and diode D_i in antiparallel), v_1 and v_2 are the terminal voltages of the transformer, L is the total leakage inductance of the transformer, i_1 is the current flowing in L, n is the turn ratio of the transformer, D_k with k=5, 6, 7, 8 are the diodes of the passive output bridge, i_{out} is the current at the output port of the SAB converter, C_o is a capacitor that filters i_{out}, V_o is the load voltage, R_L is the load and i_o is the load current.

The review of the SAB converter is carried out under some hypotheses and conditions. The hypotheses are i) n equal to 1, ii) negligible magnetizing current of the transformer, and iii) capacitor C_o great enough to fully filter the harmonics of i_{out}. Therefore, the transformer can be represented by L, i_o is equal to the DC component of i_{out}, and V_o is direct; moreover, for the input port to deliver power to the load, it must be $V_i > V_o$. The conditions are i) steady-state operation, ii) adjustable value of V_o and fixed of V_i, and iii) half-wave odd symmetry for the voltage/current waveforms.

As illustrated in the chapter 3, the SAB voltage and current waveforms in DCM and CCM are shown in Fig. 5.1.

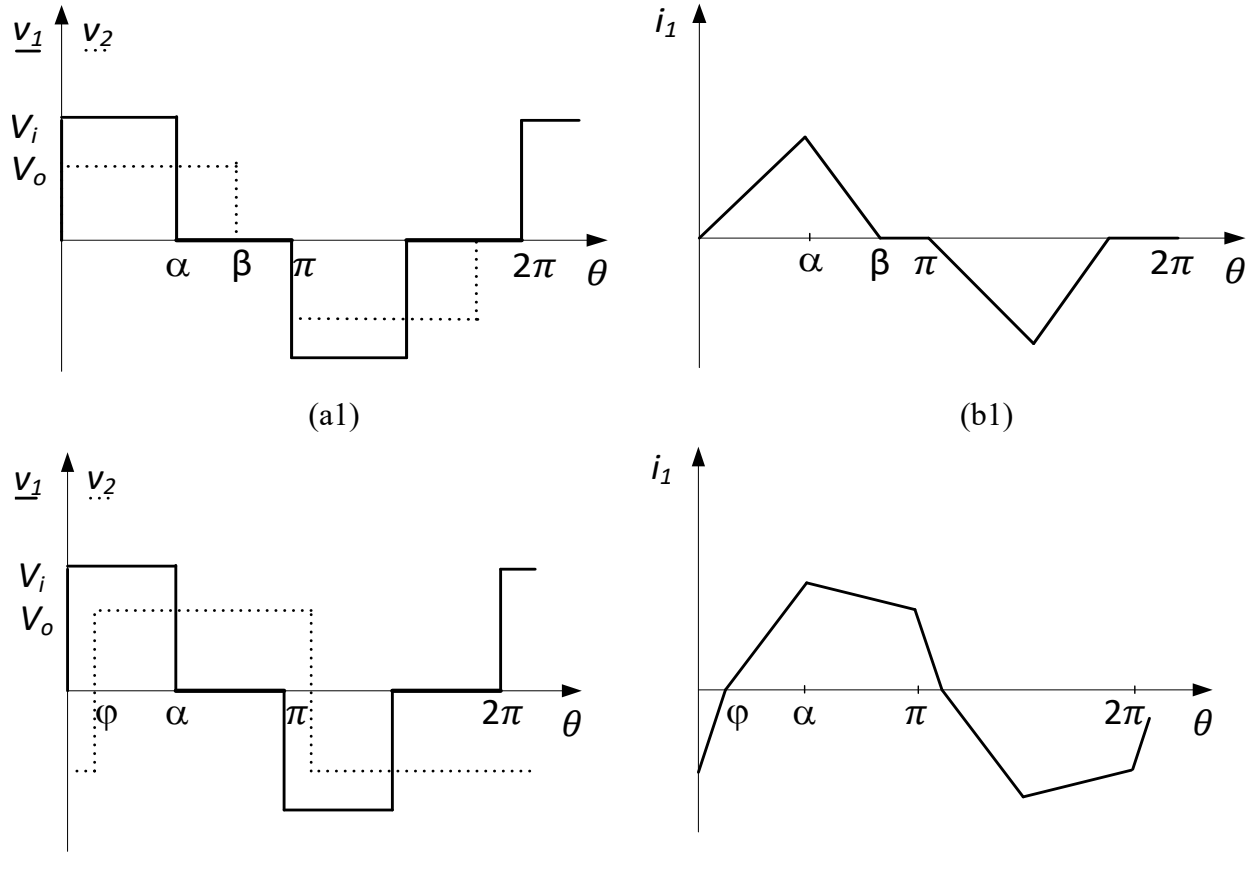


Fig. 5.1. SAB converter: (a) voltages and (b) currents in (1) DCM and (2) CCM.

From the analysis carried out in the chapter 3, the equations of the power and angles useful for the investigation of the 3PC are in DCM:

$$i_{\mathrm{L}}(\alpha) = \frac{1}{\omega L}(V_i - V_o)\alpha \tag{5.1}$$

$$\beta = \frac{V_i}{V_o}\alpha \tag{5.2}$$

$$\pi \leq \frac{V_i}{V_o}\alpha \tag{5.3}$$

$$P_{o,DCM} = \frac{V_i^2}{2\pi\omega L}\left(1 - \frac{V_o}{V_i}\right)\alpha^2 \tag{5.4}$$

and in CCM:

$$\mathrm{i_L}(0) = -\frac{\mathrm{V_i}}{\omega \mathrm{L}}\frac{\pi}{2}(1 + \frac{\mathrm{V_o}}{\mathrm{V_i}})(\frac{\alpha}{\pi} - \frac{\mathrm{V_o}}{\mathrm{V_i}}) \tag{5.5}$$

$$\mathrm{i_L}(\alpha) = \frac{\mathrm{V_i}}{\omega \mathrm{L}}\frac{\pi}{2}(1 - \frac{\mathrm{V_o}}{\mathrm{V_i}})(\frac{\alpha}{\pi} + \frac{\mathrm{V_o}}{\mathrm{V_i}}) \tag{5.6}$$

$$\varphi = \frac{\pi}{2}\left(\frac{\alpha}{\pi} - \frac{V_o}{V_i}\right) \tag{5.7}$$

$$P_{o,CCM} = \frac{V_i^2}{2\pi\omega L}\left[(\alpha^2 - 2\alpha\varphi)\left(1 - \frac{V_o}{V_i}\right) - 2\frac{V_o}{V_i}\varphi^2\right] \tag{5.8}$$

The maximum load power is given by (5.9); it is reached at $\alpha=\pi$ and depends on V_o.

$$P_{o,M} = \frac{V_i V_o}{4\omega L}\pi\left[1 - \left(\frac{V_o}{V_i}\right)^2\right] \tag{5.9}$$

The power at the boundary between CCM and DCM is expressed as

$$P_{o,B} = \frac{V_o^2}{2\omega L}\pi\left(1 - \frac{V_o}{V_i}\right) \tag{5.10}$$

and, for a given value of V_o, establishes the maximum load power in DCM and the minimum in CCM.

The relationships in (5.4) and (5.8) between P_o and α in both DCM and CCM are drawn in Fig. 5.2 for various values of V_o. Here and later on, the graphs are normalized to the following base values:

$$I_{base} = \frac{V_i}{\omega L}, \qquad \alpha_{base} = \pi, \qquad V_{base} = V_i, \qquad P_{base} = V_{base}\, I_{base}$$

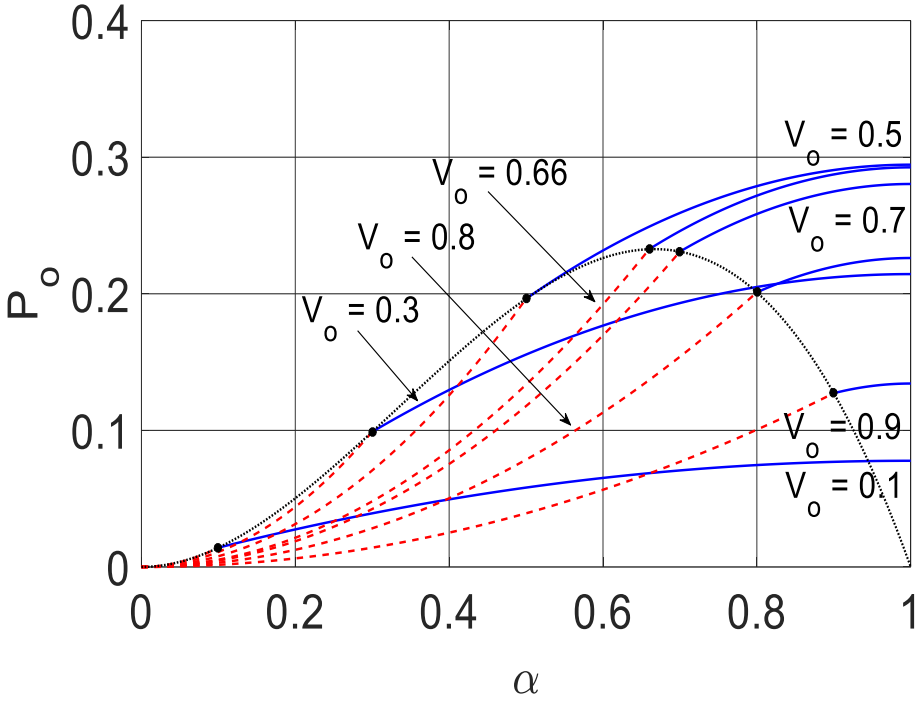


Fig. 5.2. SAB converter: load power vs. control angle (the red dashed lines refer to DCM, the blue solid lines to CCM and the grey solid line to the boundary).

Fig. 5.2 shows that i) in DCM, in agreement with (5.10), the maximum load power increases with Vo up to V_o=0.66 and then decreases, and ii) in CCM, in agreement with (5.9), the maximum load power increases with V_o up to V_o=0.5 and then decreases.

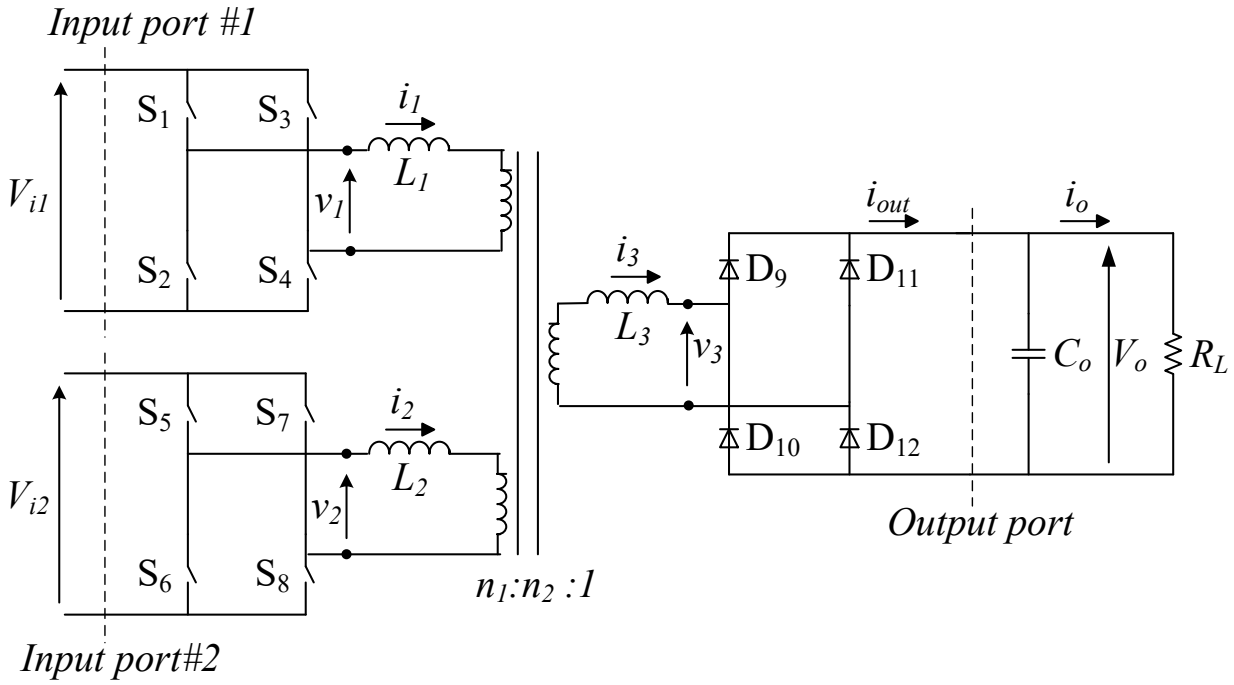
5.2 Isolated three-port DC-DC converter

The schematic of the 3PC under investigation is drawn in Fig. 5.3 (a). Differently from the SAB converter, it has an extra input port, equipped with an active bridge and denoted with #2, and a transformer with a corresponding extra winding. The input ports are supplied with the direct voltages V_{i1} and V_{i2}, respectively. The turn ratios of the windings of the transformer connected to the input ports are n_1 and n_2, and the leakage inductances of its three windings are L_1, L_2 and L_3. A very common setting for 3PC of Fig. 5.3 (a) is with one input port, let it be port #1, connected to a RES and port #2 connected to an ESD.

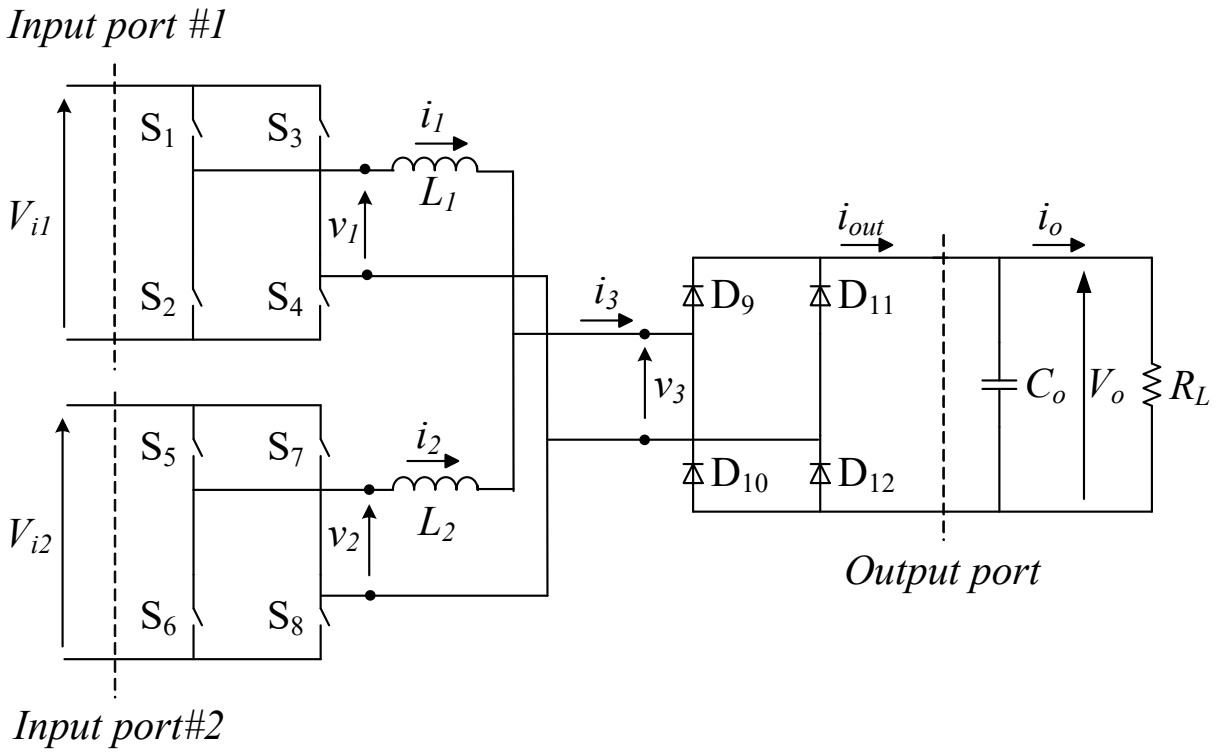
Functioning as well power and control characteristics of 3PC operating in DCM are investigated under the same conditions as the SAB converter and the following hypotheses for the transformer: i) n_1 and n_2 equal to 1, ii) negligible magnetizing current and iii) equal values of L_1 and L_2, denoted with L. Furthermore, to have the minimum ripple current, it is necessary to add an external inductance to the leakage inductances of the two windings connected to the two active ports. Therefore, considering the values of the leakage inductances of the high frequency transformers present on the market and the reasonable values of the additional inductance based on the applications of interest, the inductance L_3 can be neglected. Considering the worst case with transformer ratio equal to 1 the error of this approximation is of few per cent. In this chapter, the leakage inductance of the transformer and the additional inductance are considered together and are indicated with L_1 and L_2. As a consequence, the equivalent circuit of 3PC becomes as in Fig. 5.3 (b). Moreover, it is assumed

that the two input voltages V_{i1} and V_{i2} have equal amplitude, denoted with V_i. Again, for the input ports to deliver power to the load, it must be $V_o<V_i$.

The control variables of 3PC are i) the control angles α_1 and α_2 of the two input bridges, and ii) the shift angle, denoted with γ, between the control angles of the two input bridges.



(a)



(b)

Fig. 5.3. (a) 3PC schematic, (b) equivalent circuit.

5.3 TPC under FDCM

5.3.1 Load power delivery from both the input ports

In the case that 3PC operates in FDCM and both the input ports deliver power to the load (termed as case A), the input bridges are activated and successively deactivated at angles α_1 and α_2 within a half period of conduction, and i_1 and i_2 vanish within the half period. Employment of a shift angle does not change the delivery of power to the load and it is set at 0. Therefore, the activation angles of both the input bridges are placed at $\theta = 0$. An example of voltage and current waveforms for case A is drawn in Fig. 5.4. Note that during the interval $\beta_1 \div \beta_2$ where i_1 is zero, v_1 tracks v_3 and the latter one is equal to V_o because the diode rectifier (through D_9 and D_{12}) is still conducting i_2. A similar behavior for v_1 occurs also in Fig. 5.5 in the next Subparagraph.

The maximum load power is two times the power $P_{o,B}$ calculated in eq. 5.10. It is given by

$$P_{o,FDCM,max} = \frac{V_o^2}{\omega L}\pi\left(1 - \frac{V_o}{V_i}\right) \tag{5.11}$$

and is equally delivered by the two inputs.

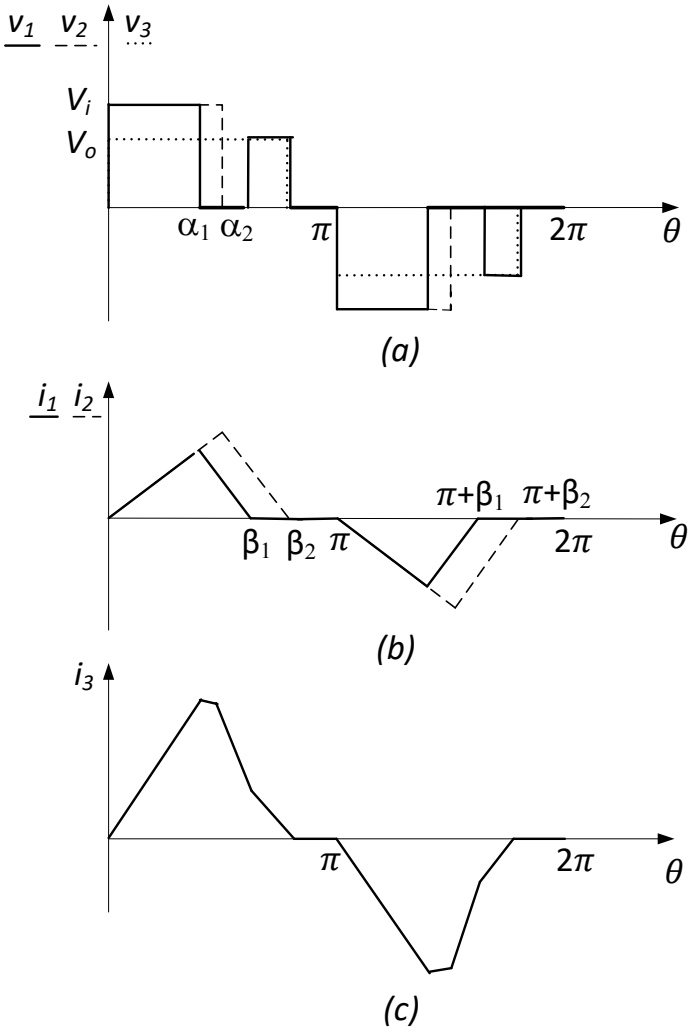


Fig. 5.4. Voltage and current waveforms for case A.

For specified values $P_{i1,DCM}$ and $P_{i2,DCM}$ of power delivery assigned to the two input ports, provided that both $P_{i1,DCM}$ and $P_{i2,DCM}$ are lower than $P_{o,B}$, angles α_1 and α_2 can be calculated from (5.4) and are expressed as

$$\alpha_1 = \pi \sqrt{\frac{2\pi\omega L}{V_i^2} \frac{1}{1-\frac{V_o}{V_i}} P_{i1,FDCM}} \tag{5.12}$$

$$\alpha_2 = \pi \sqrt{\frac{2\pi\omega L}{V_i^2} \frac{1}{1-\frac{V_o}{V_i}} P_{i2,FDCM}} \tag{5.13}$$

5.3.2 Concurrent power transfer to port #2

In the case that 3PC operates in FDCM and port #1 transfers a portion of power to port #2 and the remaining one to the load (termed as case B), bridge #1 is activated at $\theta = 0$ and deactivated at α_1, as for case A. For port #2 to absorb power, bridge #2 is activated before i_1 vanishes, i.e. before β_1.

Activation here refers to the energization of L_2, obtained by switching on T_7 (or T_6) or T_8 (or T_5) depending of the current direction. Consequently, i_2 flows into L_2 and enters into T_7 and D_5 (or T_6 and D_8) or into T_8 and D_6 (or T_5 and D_7); since v_2 is zero, i_2 increases in modulus. Bridge #2 is successively deactivated at α_2, where deactivation here refers to the de-energization of L_2 with the corresponding recovery of the stored energy into input #2. Considering the case with the T_7 on, this is achieved by switching off T_7 so that i_2 enters into input #2 through D_5 and D_8; during recovery, v_2 is equal to V_i and the modulus of i_2 decreases until to vanish at β_2. Note that input #1 delivers uninterruptedly power to the load during its conduction interval only if i_3 is positive, i.e. if the modulus of i_2 is less than i_1.

The investigation of case B is directed to find out the maximum power transferred to port #2 for a given value of α_1. The 3PC characteristics depend on whether V_o/V_i is greater or lower than 0.5; then, case B is split into two sub-cases.

$V_o/V_i<0.5$ (termed as case B1)

When $V_o/V_i<0.5$, the rate of change of i_1 is $(V_i-V_o)/L$ and that of the modulus of i_2 is V_o/L. To maximize the transfer of power to port #2, bridge #2 is activated at $\theta = 0$. Energization of L_2 goes on until the modulus of i_2 equates i_1, as drawn in the graph in Fig. 5.5. When this happens (at α_2), bridge #2 is deactivated and the modulus of i_2 decreases faster than i_1 since its rate of change is higher: $(V_i-V_o)/L$ against $-V_o/L$. Thus, angle β_2, where i_2 vanishes, is lower than β_1.

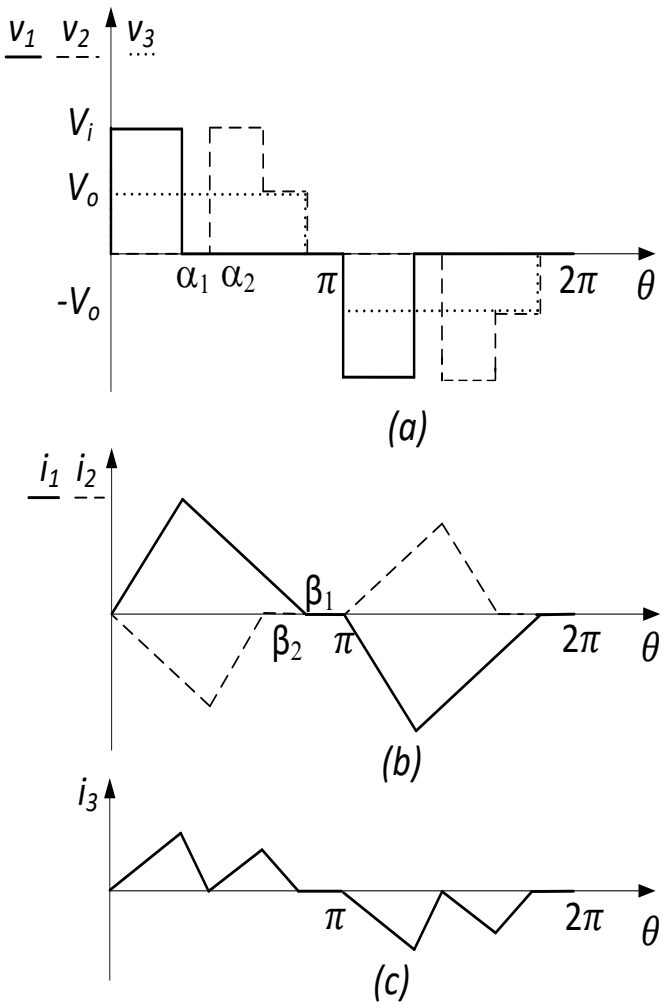


Fig. 5.5. Voltage and current waveforms for case B1.

Looking at Fig. 5.6 the angles α_2 and β_2 are calculated as following.

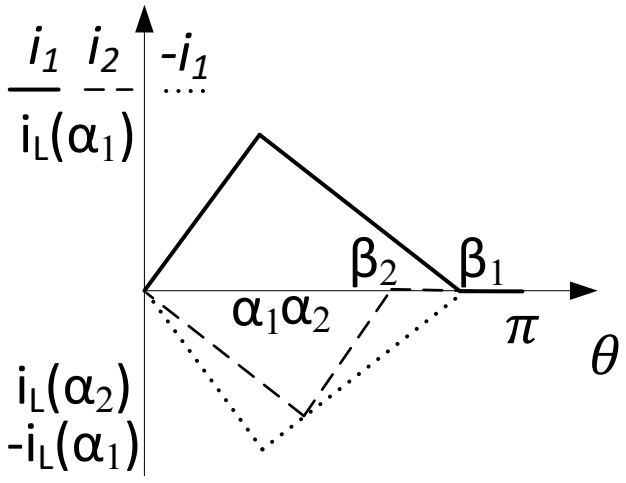


Fig. 5.6. Current waveforms for case B1.

$$\begin{cases} \frac{\theta-\alpha_1}{\beta_1-\alpha_1} = \frac{i_L(\theta)-(-i_{L1}(\alpha_1))}{0-(-i_{L1}(\alpha_1))} \\ \frac{\theta-0}{\alpha_2-0} = \frac{i_L(\theta)-0}{i_{L2}(\alpha_2)-0} \end{cases}$$

Substituting $\theta = \alpha_2$, that is the point where the two currents are equal, the system becomes

$$\begin{cases} \frac{\alpha_2-\alpha_1}{\beta_1-\alpha_1} = \frac{i_{L2}(\alpha_2)+i_{L1}(\alpha_1)}{i_{L1}(\alpha_1)} \\ i_L(\theta) = i_{L2}(\alpha_2) \end{cases}$$

Considering that $i_{L2}(\alpha_2)$ and $i_{L2}(\beta_2)$ are given by

$$i_{L2}(\alpha_2) = 0 + \frac{-V_o}{\omega L}(\alpha_2 - 0)$$

$$i_{L2}(\beta_2) = 0 = i_{L2}(\alpha_2) + \frac{(V_i - V_o)}{\omega L}(\beta_2 - \alpha_2)$$

and $i_{L1}(\alpha_1)$ is expressed by (5.1), the angles α_2 and β_2 are

$$\alpha_2 = \frac{V_i}{2V_o}\alpha_1 \tag{5.14}$$

$$\beta_2 = \frac{V_i}{2V_o\left(1-\frac{V_o}{V_i}\right)}\alpha_1 \tag{5.15}$$

Further to (5.14) and (5.15), the power transferred to input #2 is

$$P_{\#2,FDCM} = \frac{i_{L2}(\alpha_2)(\beta_2-\alpha_2)V_i}{2\pi} = \frac{V_i^2}{8\pi\omega L\left(1-\frac{V_o}{V_i}\right)}\alpha_1^2 \tag{5.16}$$

and the load power, obtained by subtracting (5.16) from (5.4), is

$$P_{o,FDCM} = \frac{V_i^2}{8\pi\omega L}\frac{\left[4\left(1-\frac{V_o}{V_i}\right)^2-1\right]}{\left(1-\frac{V_o}{V_i}\right)}\alpha_1^2 \tag{5.17}$$

The relations of the powers in (5.16) and (5.17) to α_1 are plotted with the red dashed lines in Figs. 5.9 and 5.10, respectively, for various values of V_o. By (5.3), their maximum values are achieved for $\alpha_1 = \frac{V_o}{V_i}\pi$ and are given by

$$P_{\#2,FDCM,max} = \frac{V_o^2\pi}{8\omega L\left(1-\frac{V_o}{V_i}\right)} \tag{5.18}$$

$$P_{o,FDCM,max} = \frac{V_o^2\pi}{8\omega L}\frac{\left[4\left(1-\frac{V_o}{V_i}\right)^2-1\right]}{\left(1-\frac{V_o}{V_i}\right)} \tag{5.19}$$

<u>$V_o/V_i>0.5$</u> (termed as case B2)

When $V_o/V_i>0.5$, the rate of change of i_1 is lower than that of the modulus of i_2. Then, input #1 delivers uninterruptedly power to the load during its conduction interval, provided that bridge #2 is activated at γ, as drawn in the graph on the right hand side of Fig. 5.7. Energizing of L_2 goes on until the modulus of i_2 reaches i_1. When this happens (at α_2), bridge #2 is deactivated and the modulus of

i_2 decreases slower than i_1. To maximize the power transferred to port #2, angles γ and α_2 are chosen so that i_2 vanish at the same time as i_1, i.e. so that β_2 is equal to β_1.

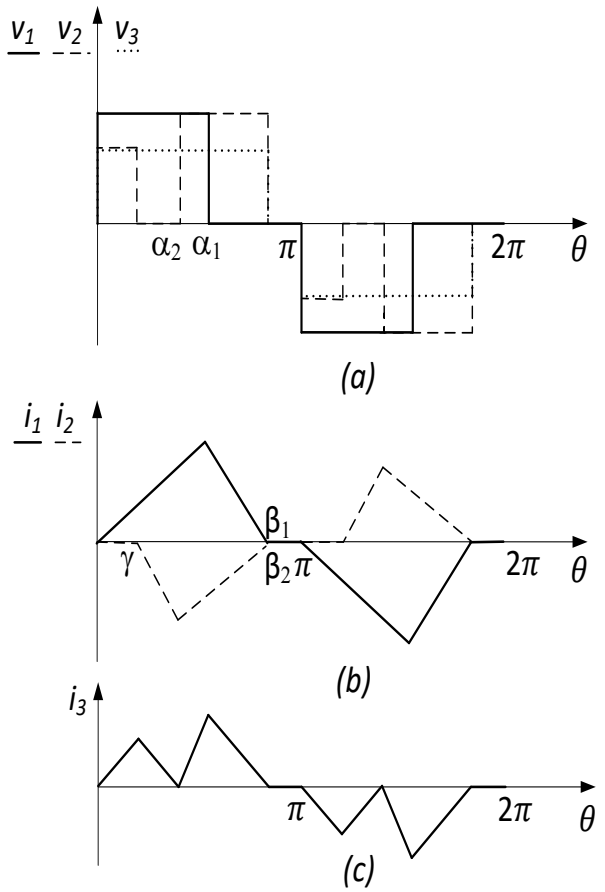


Fig. 5.7. Voltage and current waveforms for case B2.

Looking at Fig. 5.8 the angles γ and α_2 are calculated as following.

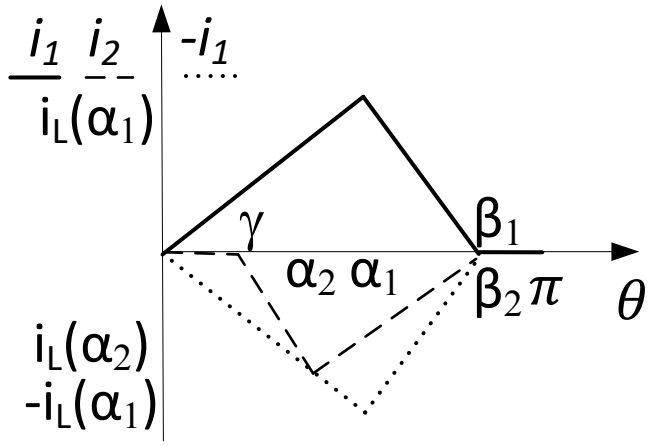


Fig. 5.8. Current waveforms for case B2.

$$\begin{cases} \frac{\theta-0}{\alpha_1-0} = \frac{i_L(\theta)-0}{-i_{L1}(\alpha_1)-0} \\ \frac{\theta-\alpha_2}{\beta_2-\alpha_2} = \frac{i_L(\theta)-i_{L2}(\alpha_2)}{0-i_{L2}(\alpha_2)} \end{cases}$$

Substituting $\theta = \alpha_2$, that is the point where the two currents are equal, the system becomes

$$\begin{cases} \frac{\alpha_2}{\alpha_1} = \frac{i_{L2}(\alpha_2)}{-i_{L1}(\alpha_1)} \\ i_L(\theta) = i_{L2}(\alpha_2) \end{cases}$$

Considering that $i_{L2}(\alpha_2)$ and $i_{L2}(\beta_2)$ are given by

$$i_{L2}(\alpha_2) = -\frac{V_o}{\omega L}(\alpha_2 - \gamma)$$

$$i_{L2}(\beta_2) = 0 = i_{L2}(\alpha_2) + \frac{(V_i - V_o)}{\omega L}(\beta_2 - \alpha_2)$$

and $i_{L1}(\alpha_1)$ is expressed by (5.1), the angles γ and α_2 are

$$\gamma = \frac{V_i}{V_o}\left(1 - \frac{1}{2}\frac{V_i}{V_o}\right)\alpha_1 \tag{5.20}$$

$$\alpha_2 = \frac{V_i}{2V_o}\left(\frac{V_i}{V_o} - 1\right)\alpha_1 \tag{5.21}$$

Further to (5.20) and (5.21), the power transferred to input #2 is

$$P_{\#2,FDCM} = \frac{i_{L2}(\alpha_2)(\beta_2-\alpha_2)V_i}{2\pi} = \frac{V_i^2}{8\pi\omega L}\left(\frac{V_i}{V_o}\right)^2\left(1 - \frac{V_o}{V_i}\right)\alpha_1^2 \tag{5.22}$$

and the load power is

$$P_{o,FDCM} = \frac{V_i^2}{8\pi\omega L}\left(1 - \frac{V_o}{V_i}\right)\left[4 - \left(\frac{V_i}{V_o}\right)^2\right]\alpha_1^2 \tag{5.23}$$

The relations of the powers in (5.22) and (5.23) to α_1 are plotted with the red dashed lines in Figs. 5.9 and 5.10, respectively, for various values of V_o. By (5.3), their maximum values are achieved for $\alpha_1 = \frac{V_o}{V_i}\pi$ and are given by

$$P_{\#2,FDCM,max} = \frac{V_o^2\pi}{8\omega L}\left(\frac{V_i}{V_o}\right)^2\left(1 - \frac{V_o}{V_i}\right) \tag{5.24}$$

$$P_{o,FDCM,max} = \frac{V_o^2\pi}{8\omega L}\left(1 - \frac{V_o}{V_i}\right)\left[4 - \left(\frac{V_i}{V_o}\right)^2\right] \tag{5.25}$$

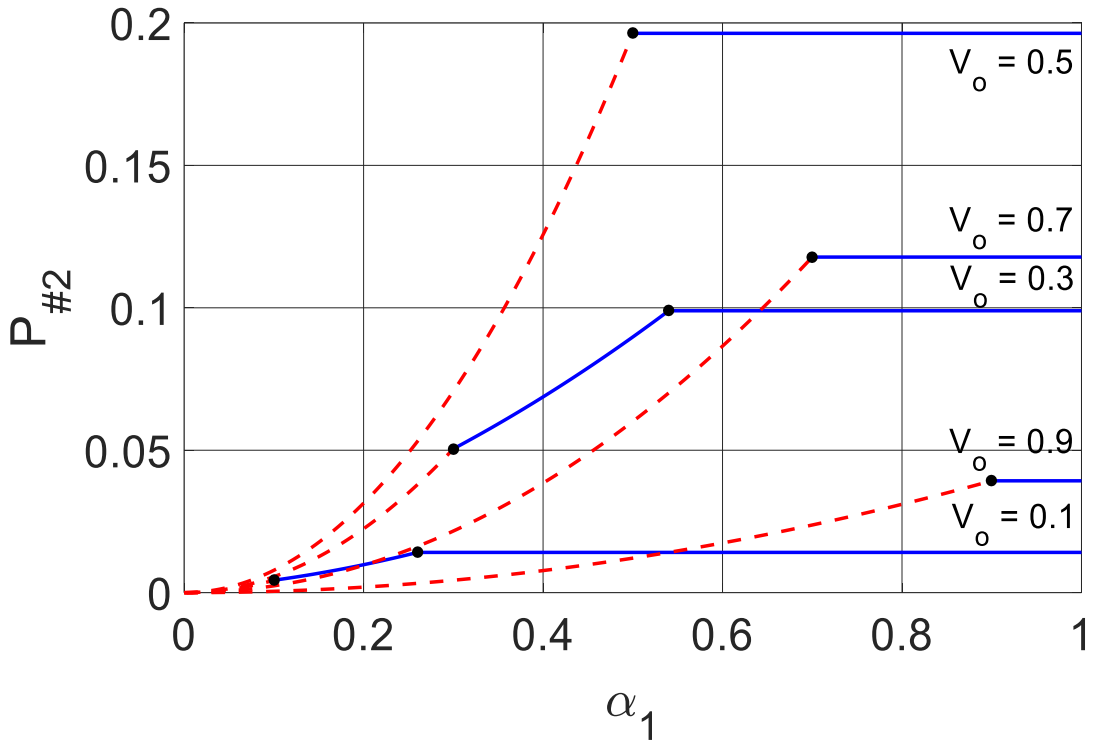


Fig. 5.9. Power transferred to port #2 vs. α1 in FDCM and MDCM.

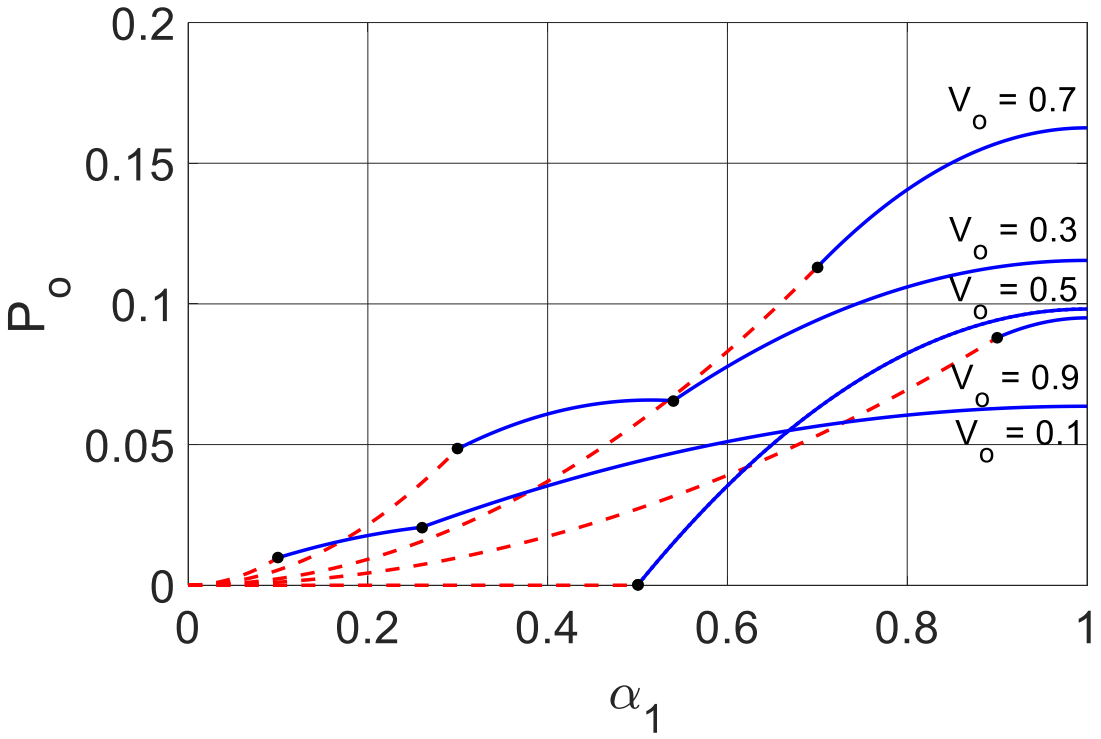


Fig. 5.10. Load power vs. α1 under power transferred to port #2 in FDCM and MDCM.

5.4 TPC under MDCM

5.4.1 Load power delivery from both the input ports

The case that TPC operates in MDCM and both the input ports deliver power to the load is termed as case C. Let port #1 be operating in CCM and port #2 in DCM. With no loss of generality, bridge #1 is activated at θ=0. Activation of bridge #2 is appropriately done along the half period of conduction of bridge #1 to reduce the effort of the two inputs in delivering power to the load. Then, γ is set at φ_1, and α_2, defined with respect to φ_1, must be chosen so that i_2 vanishes before the completion of the half period of conduction of bridge #1, i.e before $(\pi + \varphi_1)$. An example of voltage and current waveforms for case C is drawn in Fig. 5.11.

The maximum load power is obtained from (5.9) and (5.10), and is expressed as

$$P_{o,MDCM,max} = \underbrace{\frac{V_i V_o}{4\omega L}\pi\left[1-\left(\frac{V_o}{V_i}\right)^2\right]}_{P_{o,M}} + \underbrace{\frac{V_o^2}{2\omega L}\pi\left(1-\frac{V_o}{V_i}\right)}_{P_{o,B}} \tag{5.26}$$

The relationship in (5.26) between $P_{o,MDCM,max}$ and V_o resembles at large an inverted parabola with the vertex at about V_o/V_i=0.65.

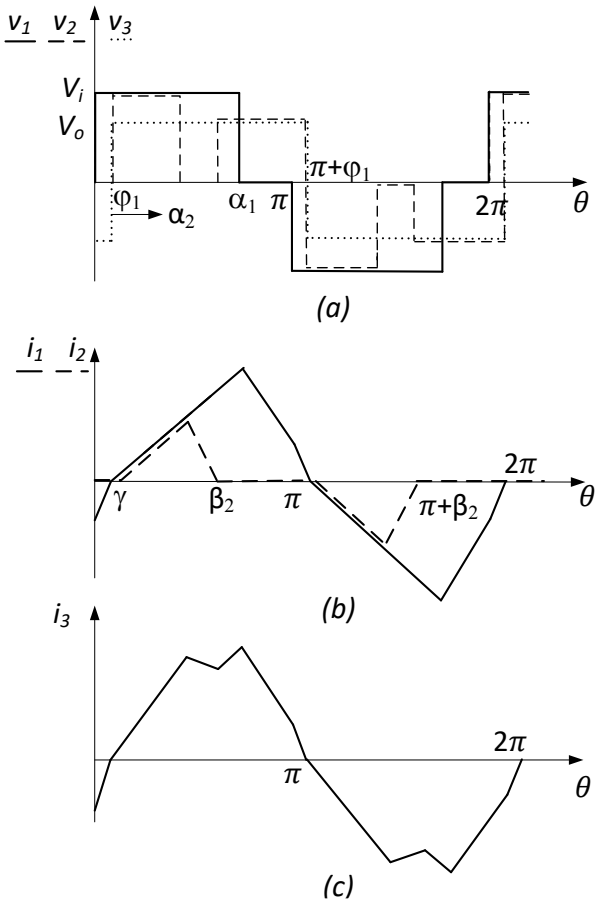


Fig. 5.11. Voltage and current waveforms for case C.

For specified values $P_{i1,}$ and P_{i2} of power delivery assigned to the two inputs, with $P_{o,B}<P_{i1,MDCM}<P_{o,M}$ and $P_{i2,DCM}<P_{o,B}$, α_1 is calculated from (5.8) and is given by (5.27), whilst α_2 is still given by (5.13)

as long as $P_{i2,DCM}$ is replaced with $P_{i2,MDCM}$.

$$\alpha_1 = \pi\left\{1 - \sqrt{1 - \left[\left(\frac{V_o}{V_i}\right)^2 + \frac{\omega L}{V_i V_o}\frac{4}{\pi}P_{i1,MDCM}\right]}\right\} \tag{5.27}$$

5.4.2 Concurrent power transfer to port #2

In the case that TPC operates in MDCM and port #1 transfers a portion of power to port #2 (termed as case D), bridge #1 is activated at θ=0 as for case C. Energization of L_2 is done along the half period of conduction of bridge #1 so that γ is equal or greater than φ_1. Also in this case the investigation is directed to find out the maximum power transferred to port #2 for a given value of α_1. The TPC characteristics depend on whether V_o/V_i is greater or lower than 0.5; thus, case D is split into two sub-cases.

V_o/V_i <0.5 (termed as case D1)

The power transferred to port #2 is maximum if bridge #2 is activated with γ equal to φ_1. Energizing of L_2 goes on until the modulus of i_2 either equates i_1 or is forced to vanish at angle $(\pi + \varphi_1)$. Then, case D1, in turn, is split into two sub-cases.

- **$\alpha_1 < \pi\frac{V_o}{V_i}\left(3 - 4\frac{V_o}{V_i}\right)$ (termed as case D1a).**

Voltage and current waveforms for case D1a are drawn in Fig. 5.12. When the modulus of i_2 equates i_1, bridge #2 is deactivated for input #1 to deliver uninterruptedly power to the load.

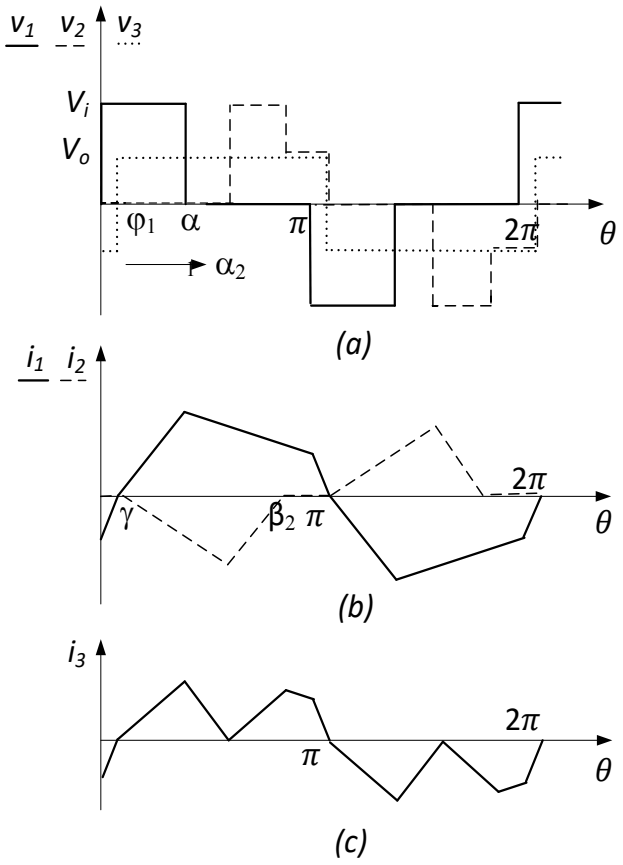


Fig. 5.12. Voltage and current waveforms for case D1a.

Looking at Fig. 5.13 the angles α_2 and β_2 are calculated as following.

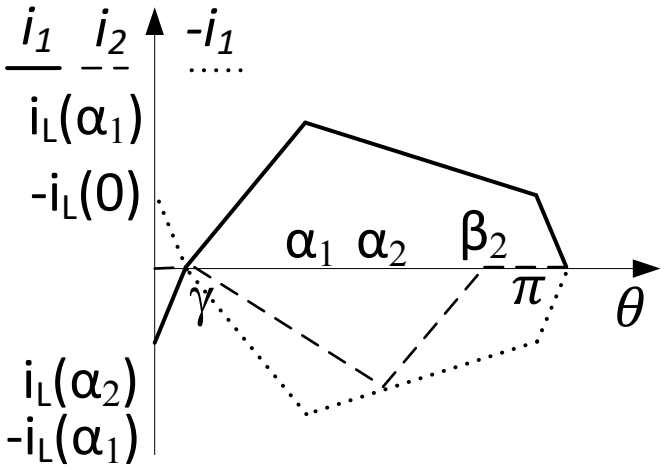


Fig. 5.13. Current waveforms for case D1a.

$$\begin{cases} \frac{\theta-\alpha_1}{\pi-\alpha_1} = \frac{i_L(\theta)-(-i_{L1}(\alpha_1))}{-i_{L1}(\pi)-(-i_{L1}(\alpha_1))} \\ \frac{\theta-\varphi_1}{\alpha_2-\varphi_1} = \frac{i_L(\theta)-0}{i_{L2}(\alpha_2)-0} \end{cases}$$

Substituting $\theta = \alpha_2$, that is the point where the two currents are equal, the system becomes

$$\begin{cases} \frac{\alpha_2-\alpha_1}{\pi-\alpha_1} = \frac{i_L(\theta)-(-i_{L1}(\alpha_1))}{-i_{L1}(\pi)-(-i_{L1}(\alpha_1))} \\ i_L(\theta) = i_{L2}(\alpha_2) \end{cases}$$

Considering that $i_{L2}(\alpha_2)$ and $i_{L2}(\beta_2)$ are given by

$$i_{L2}(\alpha_2) = 0 + \frac{-V_o}{\omega L}(\alpha_2 - \varphi_1)$$

$$i_{L2}(\beta_2) = 0 = i_{L2}(\alpha_2) + \frac{(V_i - V_o)}{\omega L}(\beta_2 - \alpha_2)$$

and $i_{L1}(\alpha_1)$ is expressed by eq. 5.1, the angles α_2 and β_2 are

$$\alpha_2 = \varphi_1 + \frac{V_i}{2V_o}(\alpha_1 - \varphi_1) \tag{5.28}$$

$$\beta_2 = \varphi_1 + (\alpha_1 - \varphi_1)\frac{V_i}{2V_o}\frac{1}{\left(1-\frac{V_o}{V_i}\right)} \tag{5.29}$$

Further to (5.28) and (5.29), the power transferred to port #2 is

$$P_{\#2,MDCM} = \frac{i_{L2}(\alpha_2)(\beta_2-\alpha_2)V_i}{2\pi} = \frac{V_i^2}{8\pi\omega L}\frac{1}{\left(1-\frac{V_o}{V_i}\right)}(\alpha_1 - \varphi_1)^2 \tag{5.30}$$

and the load power is

$$P_{o,MDCM} = \frac{V_i^2}{8\pi\omega L}\left[\frac{4(\alpha_1^2-2\alpha_1\varphi_1)\left(1-\frac{V_o}{V_i}\right)^2 - 8\frac{V_o}{V_i}\varphi_1^2\left(1-\frac{V_o}{V_i}\right)-(\alpha_1-\varphi_1)^2}{\left(1-\frac{V_o}{V_i}\right)}\right] \tag{5.31}$$

- $\boldsymbol{\alpha_1 > \pi \frac{V_o}{V_i}\left(3 - 4\frac{V_o}{V_i}\right)}$ **(termed as case D1b).**

Voltage and current waveforms for case D1b are drawn in Fig. 5.14. Here bridge #2 is deactivated in order that i_2 vanishes at $(\pi + \varphi_1)$.

Considering that $i_{L2}(\alpha_2)$ and $i_{L2}(\beta_2)$ are given by

$$i_{L2}(\alpha_2) = 0 + \frac{-V_o}{\omega L}(\alpha_2 - \varphi_1)$$

$$i_{L2}(\beta_2) = i_{L2}(\pi + \varphi_1) = 0 = i_{L2}(\alpha_2) + \frac{(V_i - V_o)}{\omega L}(\pi + \varphi_1 - \alpha_2)$$

the angle α_2 is calculated in

$$\alpha_2 = \pi\left(1 - \frac{V_o}{V_i}\right) + \varphi_1 \tag{5.32}$$

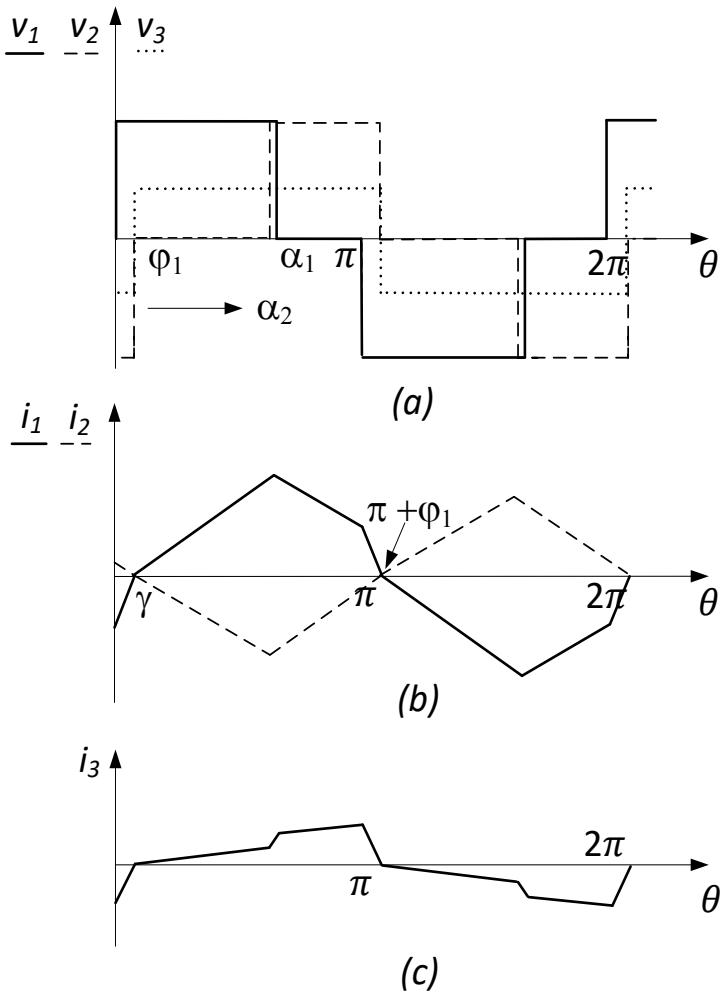


Fig. 5.14. Voltage and current waveforms for case D1b.

Further to (5.32), the power transferred to port #2 is

$$P_{\#2,MDCM} = \frac{i_{L2}(\alpha_2)(\beta_2 - \alpha_2)V_i}{2\pi} = \frac{V_o^2 \pi}{2\omega L}\left(1 - \frac{V_o}{V_i}\right) \tag{5.33}$$

i.e. it depends only on V_o and not on α_1. This can be easily recognized since, when the conduction angle of bridge #2 is π, α_1 does not play any role in controlling the transfer of power to input #2.

The load power, obtained by subtracting (5.33) from (5.8), is

$$P_{o,MDCM} = \frac{V_i^2}{2\pi\omega L}\left[\left(\alpha_1^2 - 2\alpha_1\varphi_1 - \pi^2\frac{V_o^2}{V_i^2}\right)\left(1-\frac{V_o}{V_i}\right) - 2\frac{V_o}{V_i}\varphi_1^2\right] \quad (5.34)$$

The maximum value of (5.34) is achieved for $\alpha=\pi$ and is given by

$$P_{o,MDCM,max} = \frac{V_o^2\pi}{4\omega L}\left(1-\frac{V_o}{V_i}\right) \quad (5.35)$$

The relations of the powers in (5.30) and (5.33), and in (5.31) and (5.34) to α_1 are plotted with the blue solid lines in Figs. 5.9 and 5.10, respectively, for various values of V_o.

V_o/V_i >0.5 (termed as case D2)

Voltage and current waveforms for case D2 are drawn in Fig. 5.15. As in case B2, bridge #2 is activated at γ and is deactivated as soon as the modulus of i_2 equates i_1. To maximize the power transferred to port #2, γ and α_2 are chosen so that i_2 vanishes at the same time as i_1, i.e. so that β_2 is equal to $(\pi + \varphi_1)$.

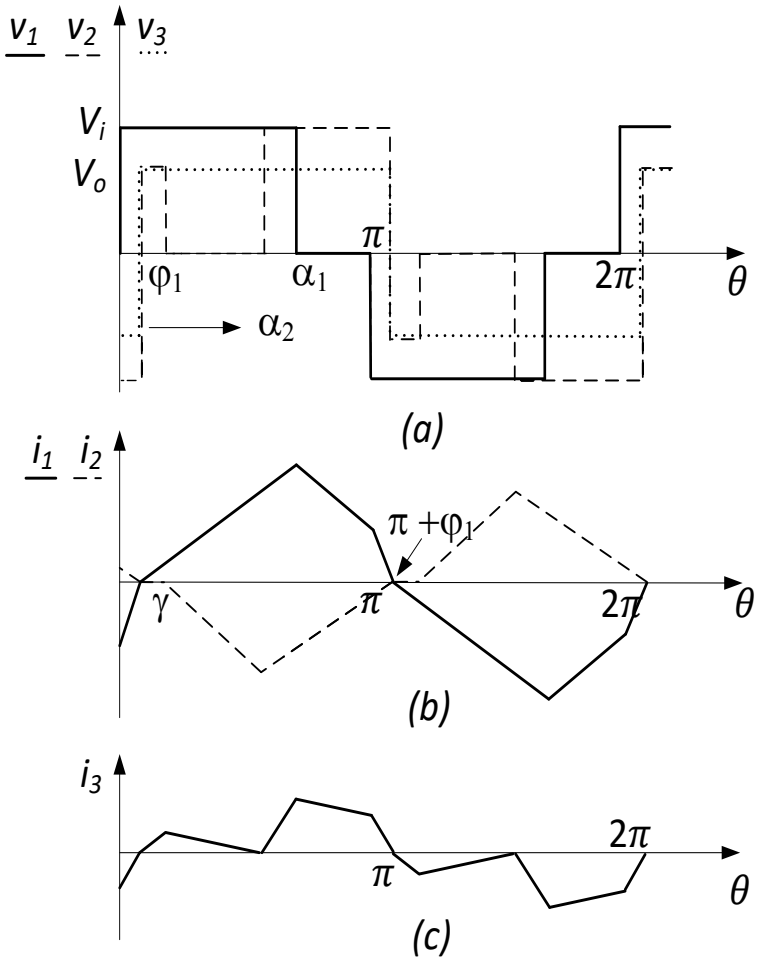


Fig. 5.15. Voltage and current waveforms for case D2.

Looking at Fig. 5.16 the angles γ and α_2 are calculated as following.

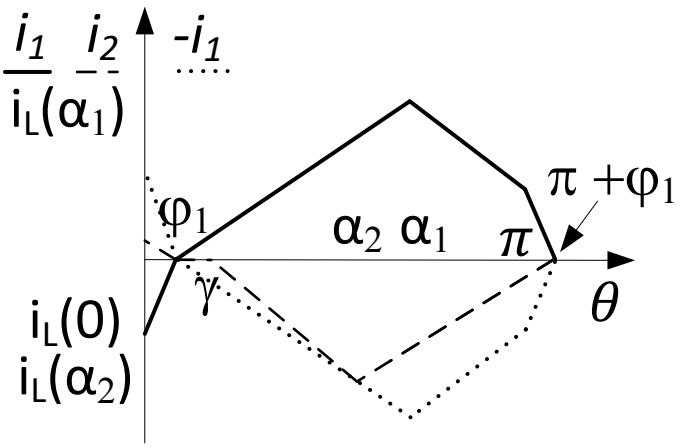


Fig. 5.16. Current waveforms for case D2.

$$\begin{cases} \frac{\theta-\varphi_1}{\alpha_1-\varphi_1} = \frac{i_L(\theta)-0}{-i_{L1}(\alpha_1)-0} \\ \frac{\theta-\alpha_2}{\pi+\varphi_1-\alpha_2} = \frac{i_L(\theta)-i_{L2}(\alpha_2)}{0-i_{L2}(\alpha_2)} \end{cases}$$

Substituting $\theta = \alpha_2$, that is the point where the two currents are equal, the system becomes

$$\begin{cases} \frac{\alpha_2-\varphi_1}{\alpha_1-\varphi_1} = \frac{i_L(\theta)}{-i_{L1}(\alpha_1)} \\ i_L(\theta) = i_{L2}(\alpha_2) \end{cases}$$

Considering that $i_{L2}(\alpha_2)$ and $i_{L2}(\beta_2)$ are given by

$$i_{L2}(\alpha_2) = 0 + \frac{-V_o}{\omega L}(\alpha_2 - \gamma)$$

$$i_{L2}(\beta_2) = i_{L2}(\pi + \varphi_1) = 0 = i_{L2}(\alpha_2) + \frac{(V_i - V_o)}{\omega L}(\pi + \varphi_1 - \alpha_2)$$

the angles γ and α_2 are calculated in

$$\gamma = \varphi_1 + \pi\left(1 - \frac{V_i}{2V_o}\right) \tag{5.36}$$

$$\alpha_2 = \frac{\pi}{2} + \varphi_1 \tag{5.37}$$

Further to (5.36) and (5.37), the power transferred to port #2 is

$$P_{\#2,MDCM} = \frac{V_i^2 \pi}{8\omega L}\left(1 - \frac{V_o}{V_i}\right) \tag{5.38}$$

and the load power is

$$P_{o,MDCM} = \frac{V_i^2}{2\pi\omega L}\left[\left(\alpha_1^2 - 2\alpha_1\varphi_1 - \frac{\pi^2}{4}\right)\left(1 - \frac{V_o}{V_i}\right) - 2\frac{V_o}{V_i}\varphi_1^2\right] \tag{5.39}$$

The relations of the powers in (5.38) and (5.39) to α are plotted with the blue solid lines in Figs. 5.9 and 5.10, respectively, for various values of V_o. The maximum value of (5.39) is achieved for $\alpha_1=\pi$, and is given by

$$P_{o,MDCM,max} = \frac{V_i^2}{4\pi\omega L}\left[\pi^2\left(1 - \frac{V_o}{V_i}\right)\left(\frac{V_o^2}{V_i^2} + \frac{V_i}{V_o} - \frac{1}{2}\right)\right] \tag{5.40}$$

5.5 Dynamic model

Among the more significant problems in the dynamic analysis of the multiport converters, there is the computational complexity of the system equations used to find the transfer functions due to the high number of the state variables. The dynamic analysis of the TPC under study is relatively simplified thanks to the control strategy adopted and presented in the previous section. As already mentioned, the TPC can be seen as a SAB or a DAB converter, according to its the working situation.

Let us consider the case when the load power is delivered by both the input ports. Thanks to the control strategy, the currents of the two input ports are independent and are equal to the SAB currents. Therefore, if the command variable of one port is kept constant, a small variation of the command variable of the other port does not introduces a variation of the current of the first port but only a variation of its own current and of the output current. In other words, the dynamics of the two input ports are independent and the relevant dynamic equations and the transfer functions are the same as the SAB converter.

Let us consider the case when port #1 transfers a portion of power to port #2 and the remaining to the load. Considering the case with port #1 connected to a RES, it delivers all the available power to the other ports independently from their control strategy. In this case, its control strategy is the same as the SAB converter while those of the other active port are different. Practical examples of this case are, for example, when the power delivered by the RES exceeds the request of the load or when, fixed the power delivered by the RES, there is a request of power from the sources connected to port #2. Let us consider the first case. If there is an exceed of the power delivered by port #1 the output voltage increases. Thanks to the control strategy, port #2 detects the higher voltage and start to absorb power to bring back the voltage to its reference value. As mentioned in the previous paragraphs, the control of the bridge is actuated acting on only one transistor: as explained in the paragraph 5.3, the energization of L_2 is obtained by switching on T_7 (or T_6) or T_8 (or T_5) depending on the current direction. Period after period, a different transistor can be selected to energize the inductance to reduce the stress of the components. To simplify the analysis, the switching of only a branch is considered (T_7 and T_8 or T_6 and T_5).

Analysis is performed considering an energy storage system connected to the DC link V_{i2} that is recharged by a portion of the energy delivered by port #1. The energy storage system is representable through an equivalent parallel branch formed by a resistance and a capacitor, as shown in Fig. 5.18 a). Supposing that the TPC operates in case B1, within half period, three intervals t_1, t_2 and t_3 are recognized in the waveform of current i2, as reported in Fig. 5.17.

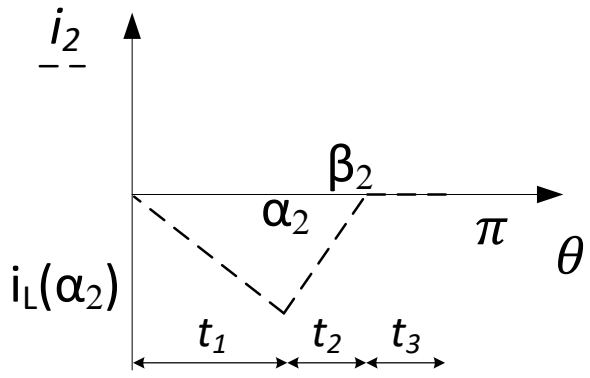
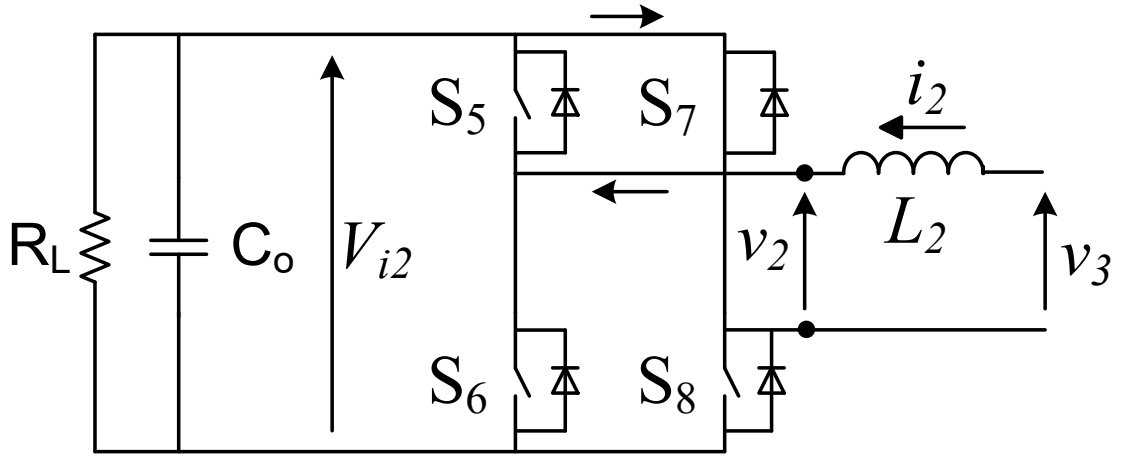
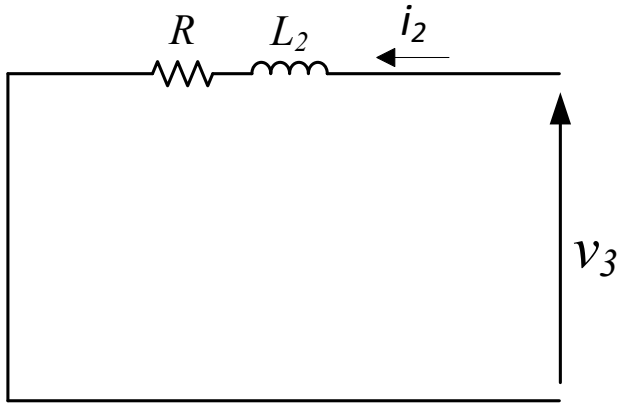


Fig. 5.17 Current waveforms of port #2 for case B1.

Let us consider the interval t_1. Port #2 schematic for this interval is shown in Fig. 5.18 (a). Its equivalent circuit is shown in Fig. 5.18 (b). The current flows through D_5 and T_7. R represents the parasitic resistance of the inductances and wire connections.



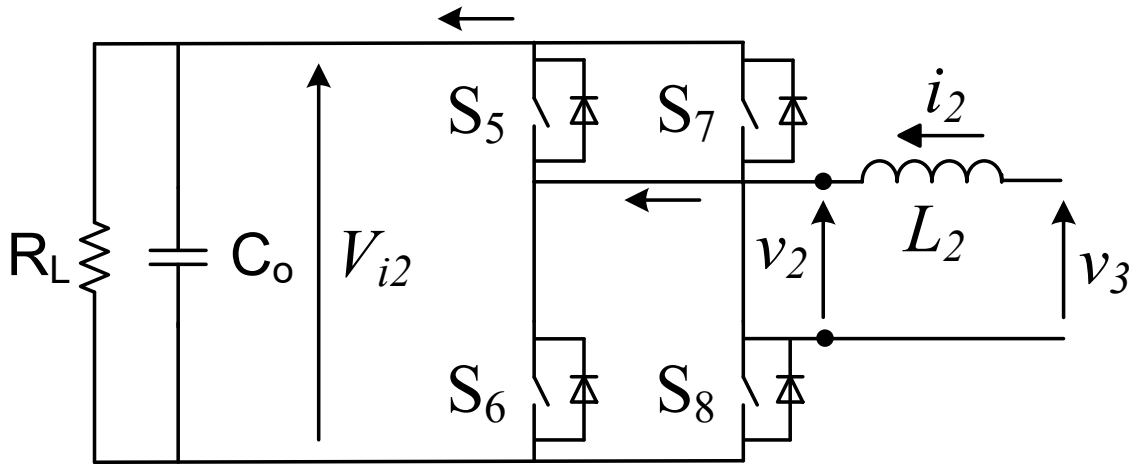
(a)



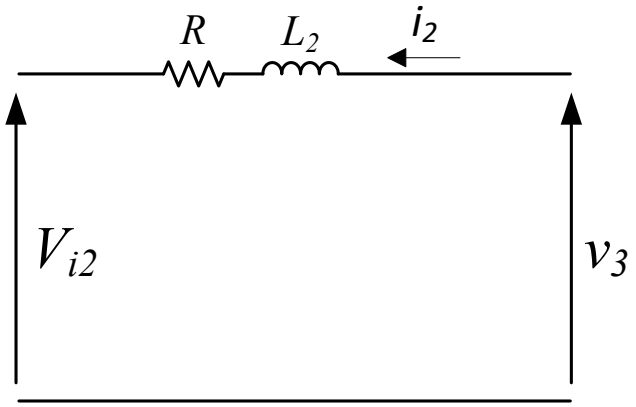
(b)

Fig. 5.18 Port #2 schematic (a) and its equivalent circuit (b) during the interval t_1.

Let us consider the interval t_2. Port #2 schematic for this interval is shown in Fig. 5.19 (a). Its equivalent circuit is shown in Fig. 5.19 (b).



(a)



(b)

Fig. 5.19 Port #2 schematic (a) and its equivalent circuit (b) during the interval t_2.

Looking the circuits of Figs. 5.18(b) and 5.19(b) the equations derivable are, for the interval t_1:

$$v_3 - L_2 \frac{di_L}{dt} - Ri_L = 0 \tag{5.41}$$

$$C_o \frac{dV_{i2}}{dt} + \frac{V_{i2}}{R_L} = 0 \tag{5.42}$$

and for the interval t_2

$$v_3 - L_2 \frac{di_L}{dt} - Ri_L - V_{i2} = 0 \tag{5.43}$$

$$C_o \frac{dV_{i2}}{dt} + \frac{V_{i2}}{R_L} - i_L = 0 \tag{5.44}$$

During the interval t_3 the inductance current is zero and the only equation is (5.44).

Appling the same approach used for the SAB converter within half period, the small signal model equations are

$$s\widetilde{i_2} = \left(-\frac{R}{L}\widetilde{i_2} + \frac{1}{L}\widetilde{v_3}\right)(d_1 + d_2) + \left(-\frac{R}{L}i_2 + \frac{1}{L}v_3\right)\left(\widetilde{d_1} + \widetilde{d_2}\right) - \frac{1}{L}V_{i2}\widetilde{d_2} \quad (5.45)$$

$$s\widetilde{v_{i2}} = -\frac{1}{R_L C_o}\widetilde{v_{i2}} + \frac{1}{C_o}\left(\widetilde{d_2}i_2 + \widetilde{i_2}d_2\right) \quad (5.46)$$

As for the SAB converter, in DCM the inductor current does not behave as a true state-space variable. Considering that the current restarts from zero at each switching period, the current in one period is not influenced by the current behaviour or the command variable of the previous one. The constrain due to the inductor current is $\frac{di}{dt}(T_s) = \frac{i(T_s)-i(0)}{i(T_s)} = 0$ with $T_s = t_1+t_2+t_3$. Considering the current loop much faster than the voltage loop, the input voltage is assumed $\widetilde{v_3} = 0$. Then, the control to output current transfer function is a constant obtainable by equation (5.45).

The output current to DC voltage transfer function is obtained from eq. (5.46) with the hypothesis that the variations of the duty cycle are zero $\widetilde{d_1} = \widetilde{d_2} = 0$ because the voltage loop is much slower than current loop.

$$G_{v_{i2}-i2} = \frac{\widetilde{v_{i2}}}{\widetilde{i_2}} = \frac{R_L d_2}{1+sR_L C_o} \quad (5.47)$$

The hypotheses assumed are valid because the current loop is much faster than voltage loop.

Let us consider the case when the load connected to the passive port is disconnected. In this case, only the two active ports are used and the schematic assumes the same configuration of the DAB converter. Then, the same considerations, regarding the control and dynamic model, performed for the DAB converter are applicable. Another solution is to turn off all the transistor of port #2. In this case, thanks to the diode in parallel to the transistor, the system operates like a SAB.

5.6 Simulation and experimental results

In order to realize a prototype of SST, a TPC is designed and built for validating the analysis done in the previous paragraphs. Its function is to substitute the more classical two port converter used in the central part of the SST. Thanks to its more complex structure, the TPC offers more functionalities than the two port DC-DC converter. The project presented in the next paragraphs is focused on the TPC with port #1 connected to the main source, which can be the grid or a RES, port #2 connected to an ESD and the output port connected to a resistive load. Both the sources are connected to the DC links through other conversion stages that are needed, for example, to charge or discharge the battery at constant voltage or current, or for the implementation of an optimization algorithm, such as MPPT for a photovoltaic plant. The TPC is studied at full power in the simulations while the prototype is sized for a reduced power.

5.6.1 Simulation results

The specifications and the parameters of the project are listed in Tab. 5.1. Port #1 is supplied by the main source, such as a RES, and its DC link voltage is set at 150 V. Port #2 is connected to an ESD and its DC link voltage is set to 26 V. The voltage of the output port is chosen to be used in a variety of applications, in particular battery chargers or light DC loads and it is set to 60 V. The transformer parameters are reported in Appendix A. The inductances L_1 and L_2 are composed by the transformer inductance and an extra inductance inserted in series to the windings to reduce the ripple current. The values of the additional inductances used are the same of the two used in the SAB and DAB

prototypes. More in detail, the inductance of 1.22uH is connected to low voltage side and the inductance of 65uH is connected to high voltage side. The total inductances result 3uH (98uH referred to high voltage side) and 76uH. The resulting inductances are not equal and this causes two different slopes of the two input current (current slope of port #2 is lower). However, this effect practically does not influence the analysis done for the operating range of the converter. In fact, the aim of the control is to keep the current of port#2 inside the shape of port#1 current. Then, considering that the slope of port#2 current is lower, the focus of the control is achievable more easily.

TAB. IV. SAB CONVERTER PARAMETERS

Parameter	Value	Unit
V_{i1}	150	V_{peak} DC
V_{i2} (ref. to low voltage side)	26	V_{peak} DC
V_o	60	V
$P_{o\_max\_port\#1}$	1	kW
f_{sw}	10	kHz
L_1	76u	H
$L_2 \cdot n^2$	98u	H
C_o (used for all dc link)	1000u	F
Transformer ratio n	5.71	-
Load resistance	10÷4	Ohm

The system is designed around the maximum power deliverable by port #1 and the studied working situations are

1) load power delivery by both the active ports;
2) port #1 transfers more power of the necessary to the output port and to keep the output voltage constant port #2 absorbs the part in surplus.

For simplicity, the three H-bridges forming the active ports are equal and are the same used for the SAB and the DAB converter prototypes.

For the calculation of the PI parameters of the current and voltage loops the bandwidth are set $f_{BWi} = 500\,Hz$ and $f_{BWv} = 30\,Hz$, while for both of them phase margin is $m_\varphi = 70°$. The regulators parameters are:

$$K_i = 2e-3 \qquad t_i = 0.225\,ms \qquad K_v = 0.115 \qquad t_v = 2.6\,ms$$

In the calculation of the current loop parameters the influence of a low pass filter applied at the output of the current sensor is also considered; the filter is of the 2nd order and has the following parameters

$$K_f = 1 \qquad f_{cut-off} = 2000\,Hz \qquad \xi = 0.7$$

It is used to filter out the alternating component of the DC currents acquired by the current sensor; indeed, the latter one is inserted before the output capacitor in order to manage the case relevant to an open load.

After an evaluation of the possible parameters for all the operation range and for the different working situations, considering that the parameters do not change deeply, the same parameters values are used for the different cases. The simulations validate this choice.

The power circuit implemented in the simulation is shown in Fig. 5.20.

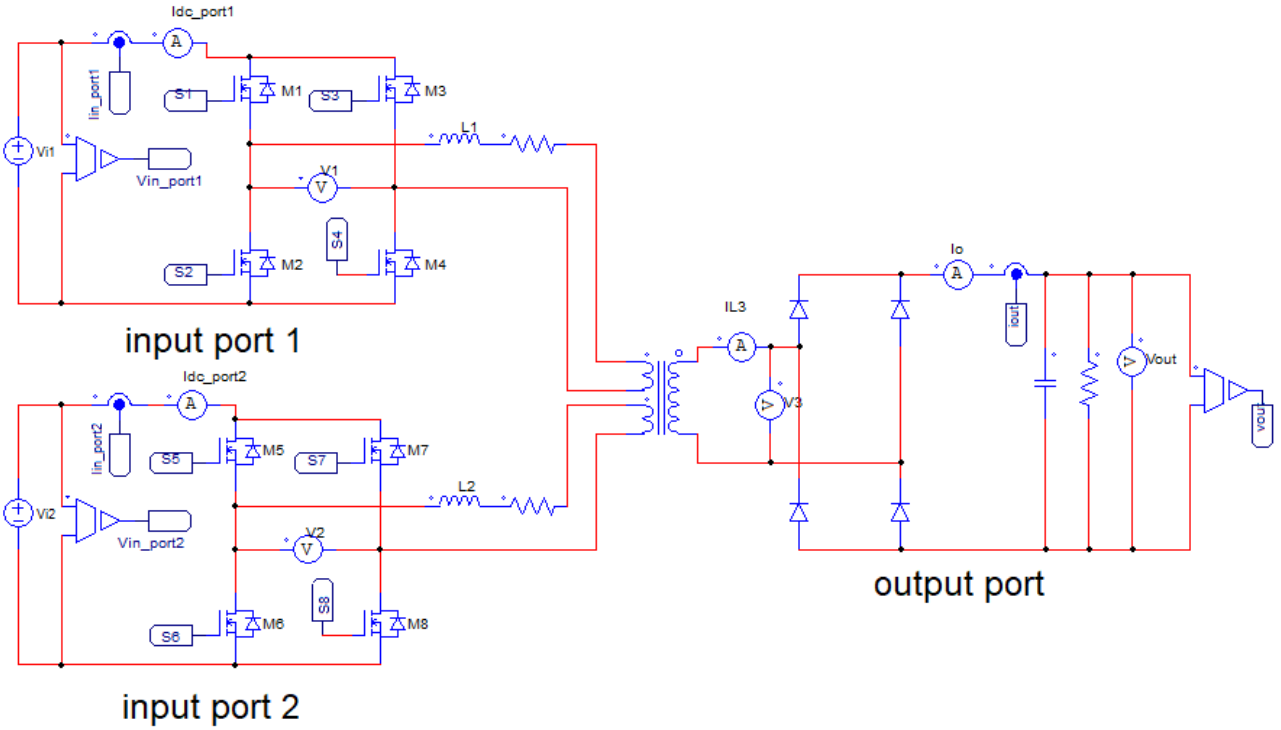


Fig. 5.20 TPC power circuit.

The same regulators are used for the two working situations and the two operation. The control scheme of port #1 is shown in Fig. 5.21. The scheme is based only on the current control loop because the source connected to port #1 is assumed to deliver all the power available. The voltage loop is disabled and only the value of the reference current I_1 (DC) is changed to simulate a shortage or an abundance of power delivered by port #1. The control of the output voltage is a task of port #2.

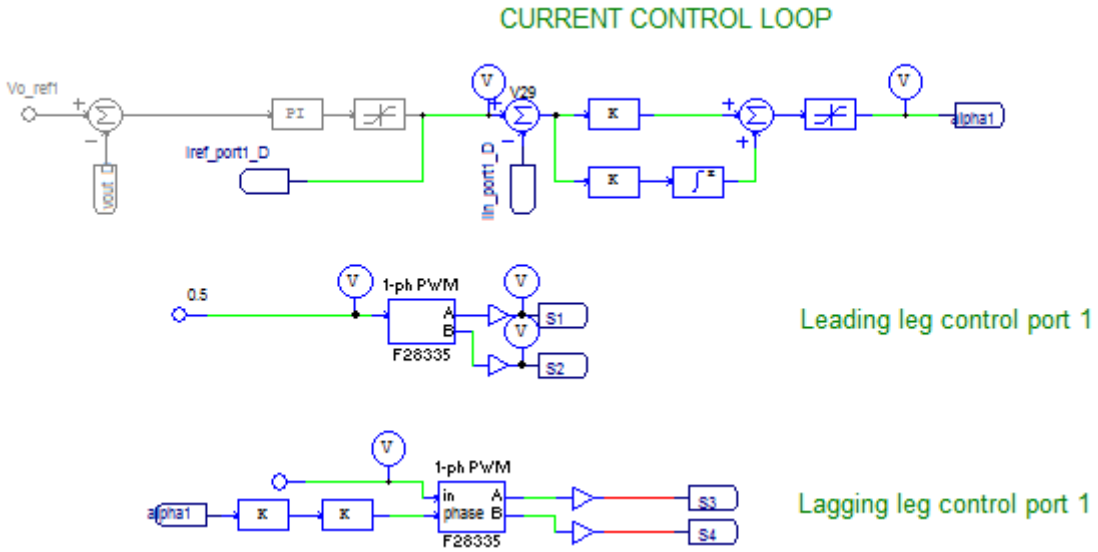
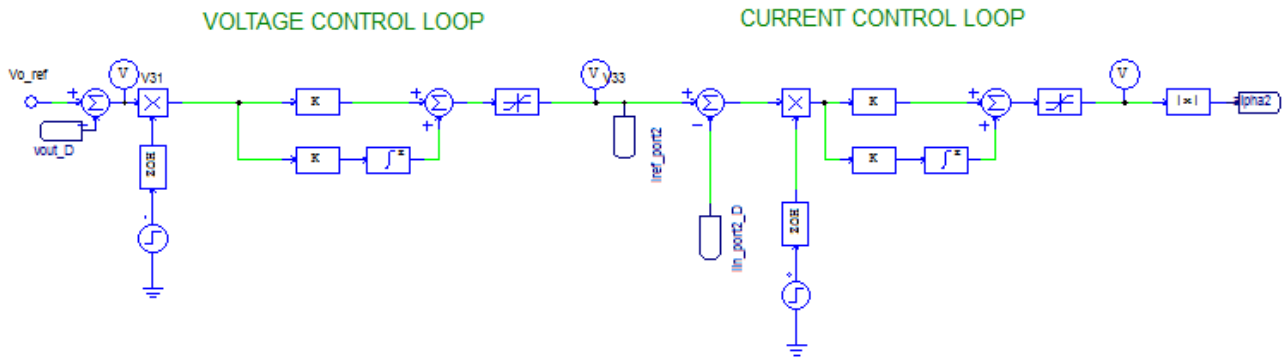


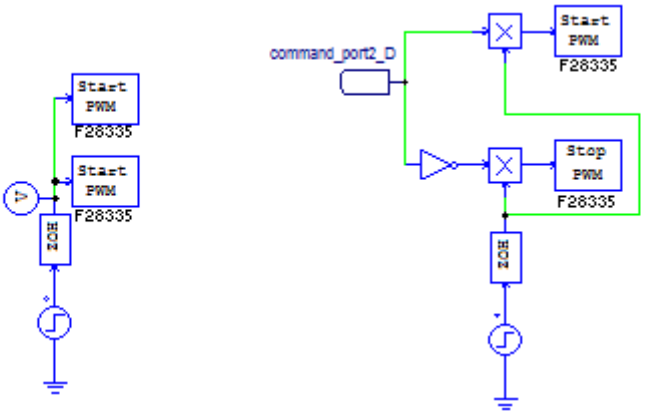
Fig. 5.21 Port #1 control circuit.

Port #2 control circuits are shown in Figs. 5.22 and 5.23. In this port both the control loops of voltage and current are present. The voltage loop has the function to keep the output voltage at the reference value. Then, if port #1 delivers too much power, port #2 starts to absorb power to prevent the output voltage from exceeding the reference. Vice versa, if port #1 does not deliver enough power, port #2

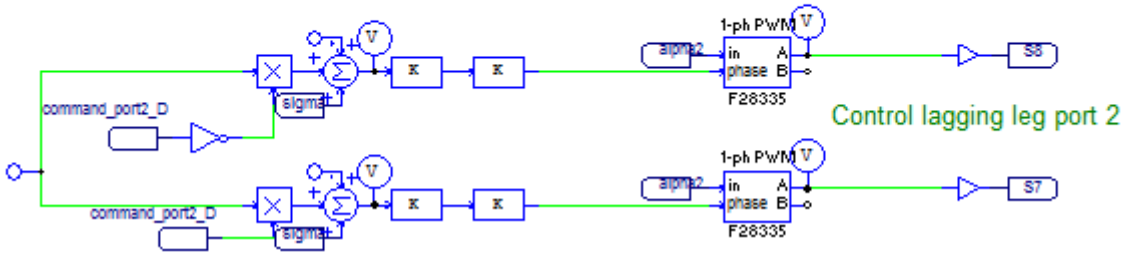
starts to deliver power to the output to sustain the output voltage. Both the ports are endowed with current control loops shown in Fig. 5.22 (a). The gate signals of port #2 are conditioned using the scheme of Fig. 5.22 (b), required to turn on the PWM of port #2 only after the initial start up of port #1, and to turn on-off the PWM of some transistors during the switching between the different working situations. Furthermore, in the lower part of Fig. 5.22(b), the lagging leg control scheme of port #2 is reported; the leading leg control is shown in Fig. 5.23 togerher with the phase shift calculation circuit.



(a)



COMMAND ON-OFF PWM PORT 2



(b)

Fig. 5.22 Port #2 control loops (a) and lagging leg control (b).

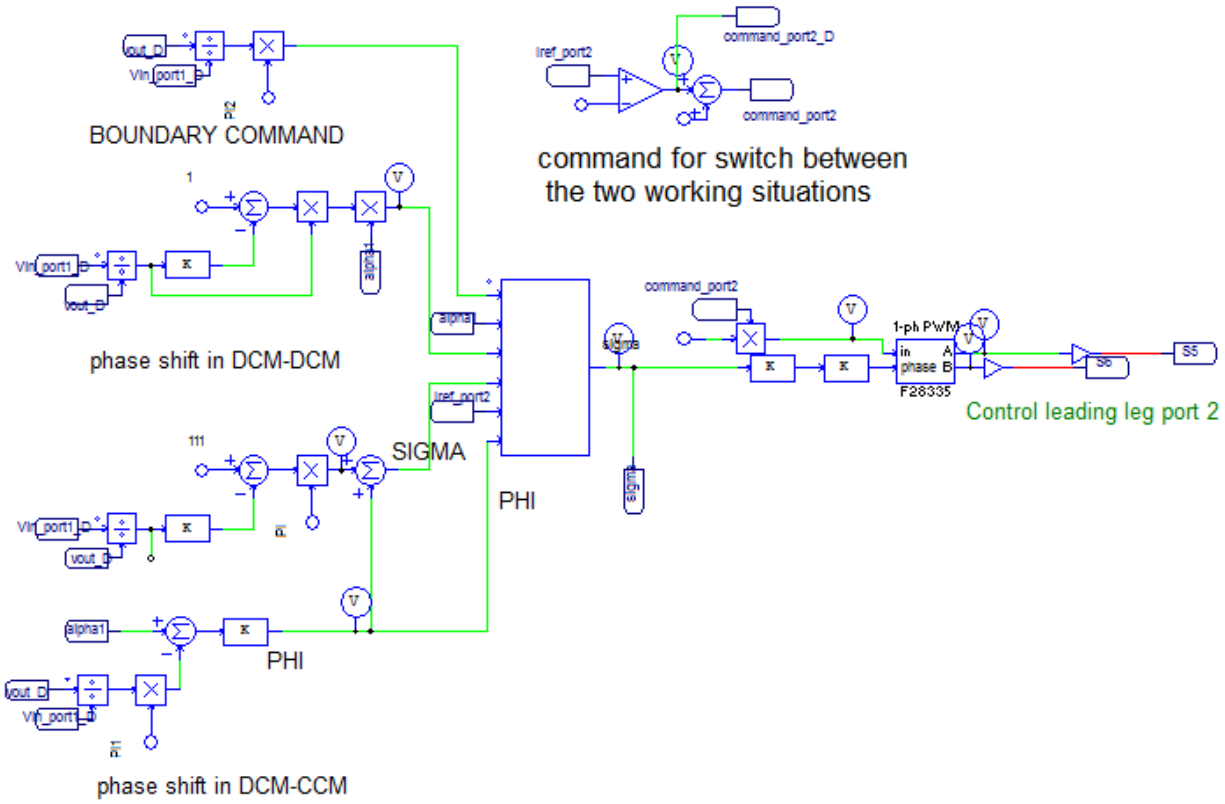


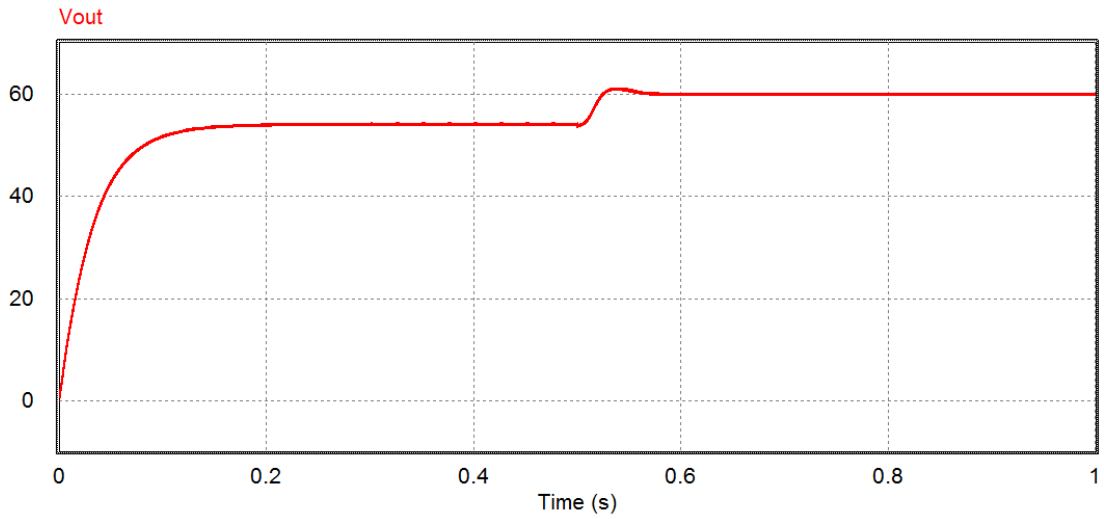
Fig. 5.23 Port #2 phase shift calculation circuit and leading leg control.

The two working situations are analysed using different load resistances to check the correct operation of the TPC in both the conduction modes; the load resistance is set to 10 Ω in FDCM while operation in MDCM has been tested with load resistances of 4Ω and 4.2 Ω.

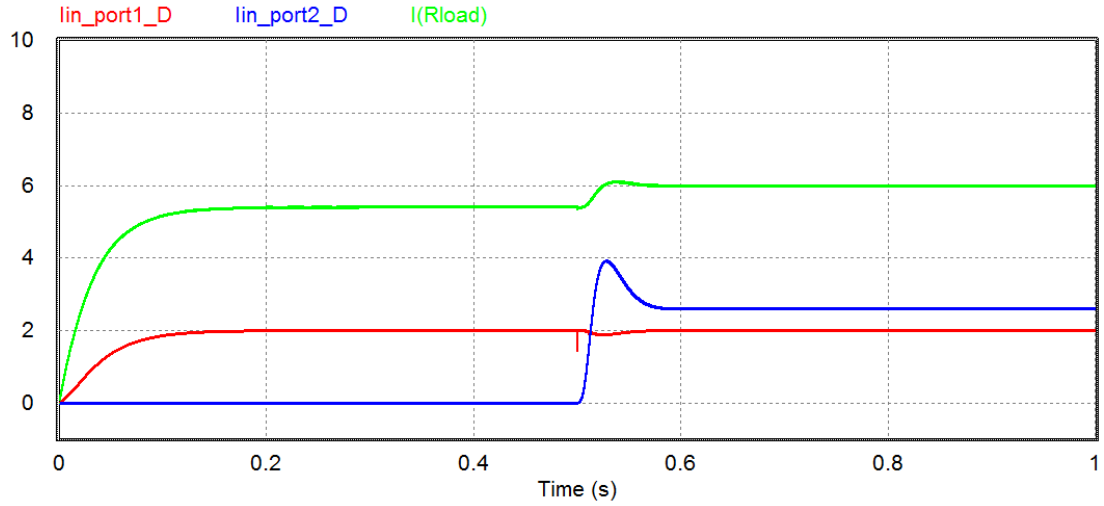
1) Load power delivery by both the active ports

FDCM

Let us consider the case when the load power is delivered by both the ports in FDCM. The current reference of port #1 is set to 2 A. Port #2 PWM and control is turn on after 0.5 s. The output voltage and the DC current of the three ports are shown in Fig. 5.24 (a) and Fig. 5.24 (b) respectively. Fig. 5.24 (a) shows that the output voltage reaches about 54 V with only port #1 operating. At 0.5 s port#2 starts to operates and increases the voltage to 60 V, which is the reference value. Fig. 5.24 (b) shows the DC current of the input port #1 (red) that follows the reference value of 2 A, the DC current of the input port #2 (blue), which is of 2.6 A, and the output DC current that reaches 6 A after turning on of port #2. The power transferred to output is 360 W of which 300 W from port #1 and 67.7 W from port #2; of the supplied 367.7W, 7.7 W are wasted in the parasitic resistances. The simulation results highlight the proper operation of the control system.



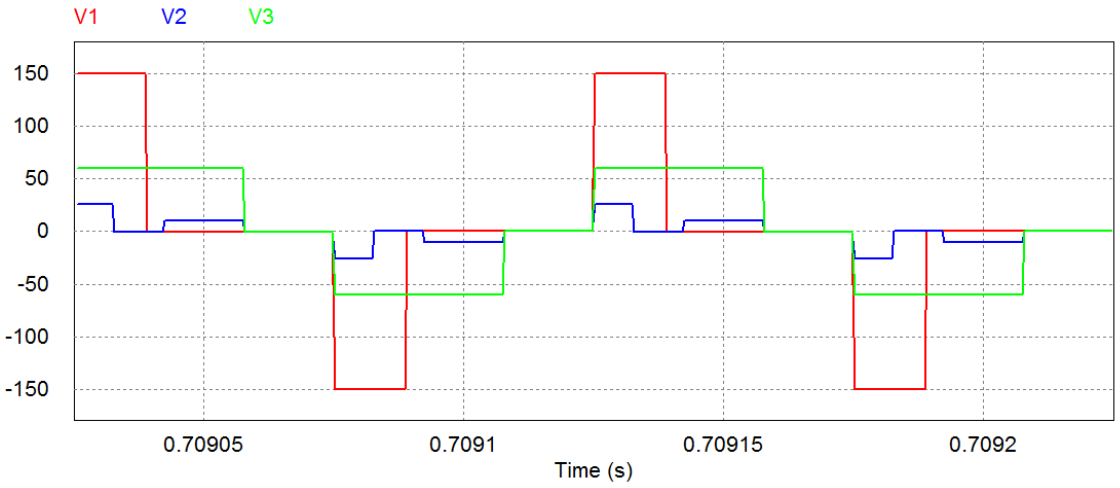
(a)



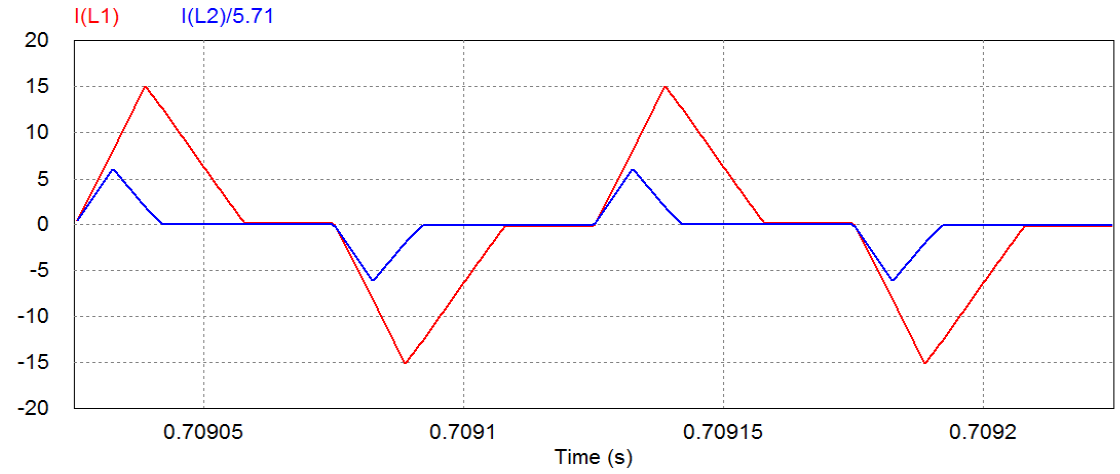
(b)

Fig. 5.24 Output voltage (a) and, input (red and blue) and output (green) DC currents.

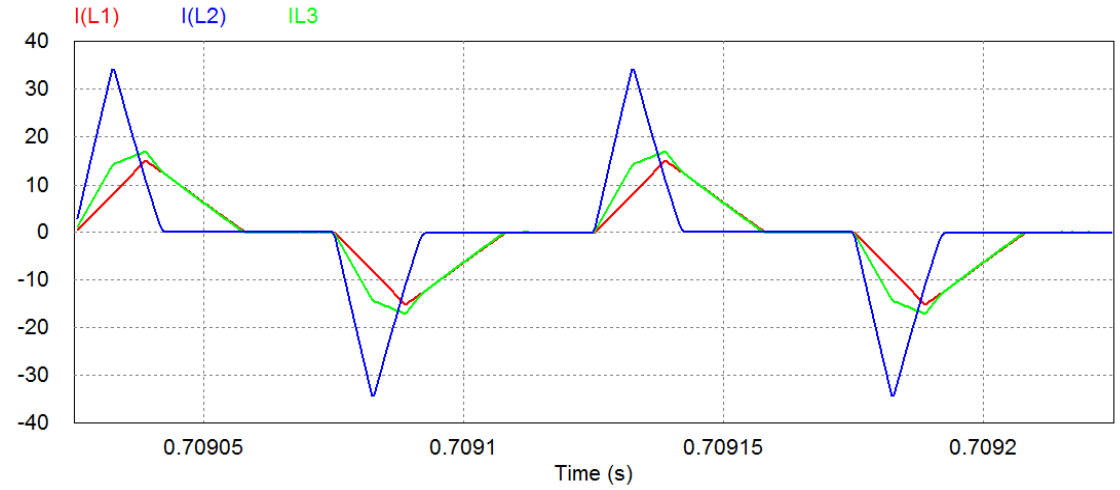
The waveforms of the voltages and current at the transformer side are shown in Fig. 5.25. The waveforms of the voltages in Fig. 5.25 (a) validate those illustrated in the previously done analysis. Fig. 5.25 (b) shows the two input port currents referred to high voltage side of the transformer. As already mentioned, the slope of the port #2 current is lower due to the total inductance, which is a bit higher than that of the other port. However, this does not influence the shape of the currents which are the same of the SAB converter operating in DCM. Then, the considerations done during the mathematical analysis are validated. Fig. 5.25 (c) shows the two input currents, referred to their ports, and the output current at the transformer side.



(a)



(b)

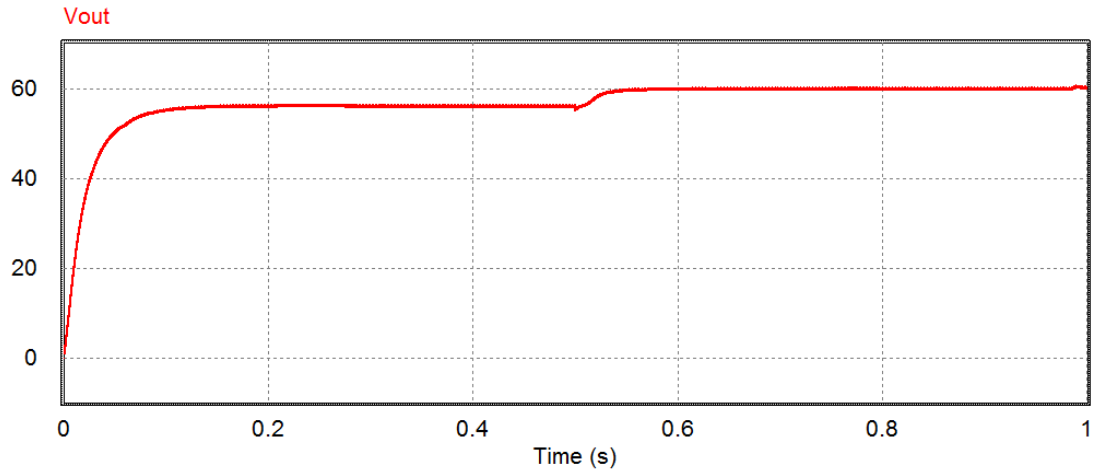


(c)

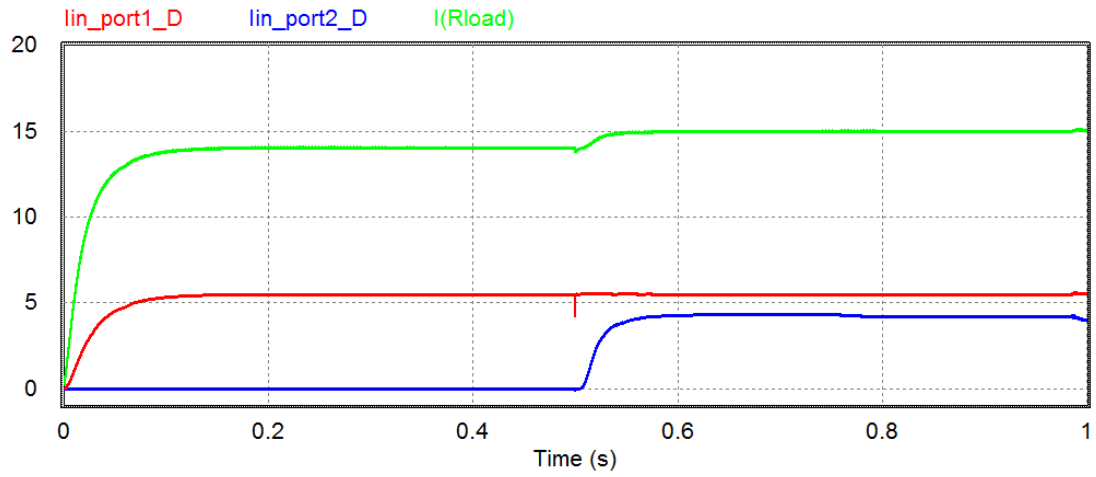
Fig. 5.25 Port voltages at transformer side (a), input port currents referred to high voltage side (b) and port currents at transformer side (red: port#1, blue:port#2,green:output port).

MDCM

Let us consider the case when the load power is delivered by both the ports in MDCM. The current reference of port #1 is set to 5.5 A. The load resistance is 4 Ω. The port #2 PWM and control are turned on after 0.5 s. The output voltage and the DC current of the three ports are shown in Fig. 5.26 (a) and (b) respectively. Fig. 5.26 (a) shows that the output voltage reaches about 56 V with only port#1 operating. At 0.5 s port#2 starts to operate and increases the voltage to 60 V, which is the reference value. Fig. 5.26 (b) shows the DC current of the input port #1 (red) that follows the reference value of 5.5 A, the DC current of the input port #2 (blue) which is 4.3 A, and the output DC current of 15 A after the turning on of port #2. The power transfer to output is 900 W of which 825 W from port #1 and 112 W from port #2. In this case, 37 W are lost in the parasitic resistances. The results highlight that the control is working properly.



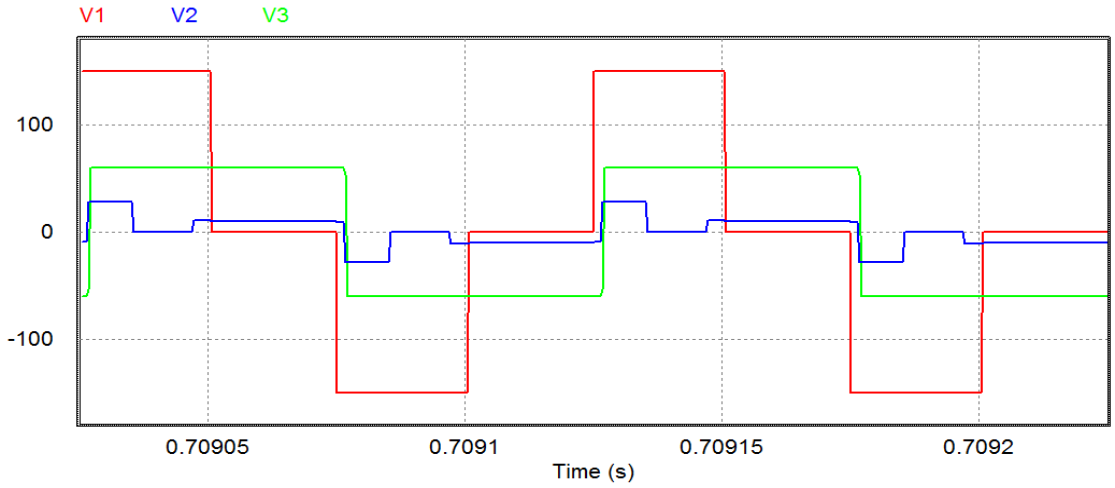
(a)



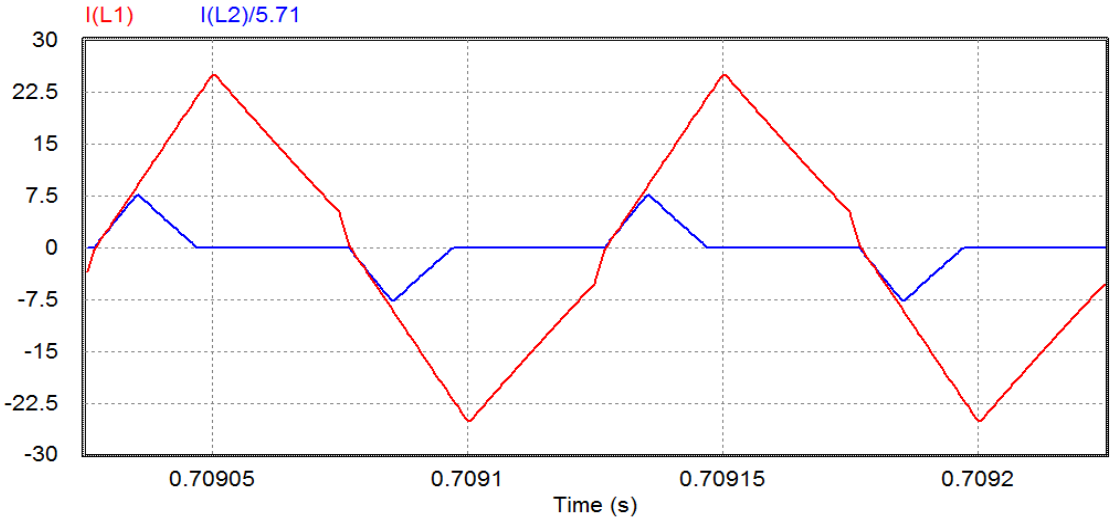
(b)

Fig. 5.26 Output voltage (a) and, input (red and blue) and output (green) DC currents.

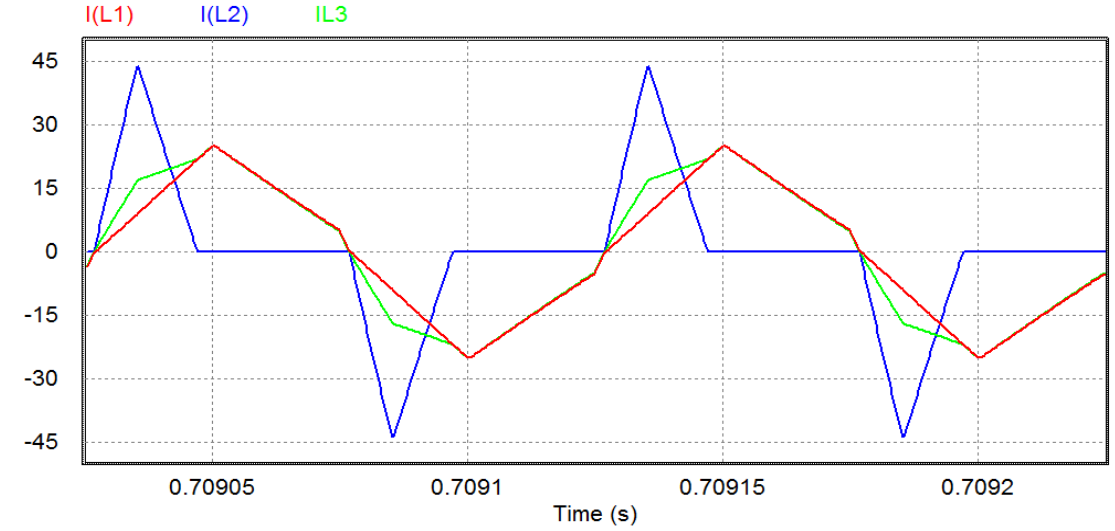
The waveforms of the voltages and currents at transformer side are shown in Fig. 5.27. The waveforms of the voltages in Fig. 5.27 (a) validate those illustrated in the previously done analysis. Fig. 5.27 (b) shows the two input currents referred to the high voltage side. The phase shift γ of the bridge #2 commands is set equal to φ_1. Fig. 5.27 (c) shows the two input currents, referred to their ports, and the output current at transformer side. The results validate the mathematical analysis done.



(a)



(b)



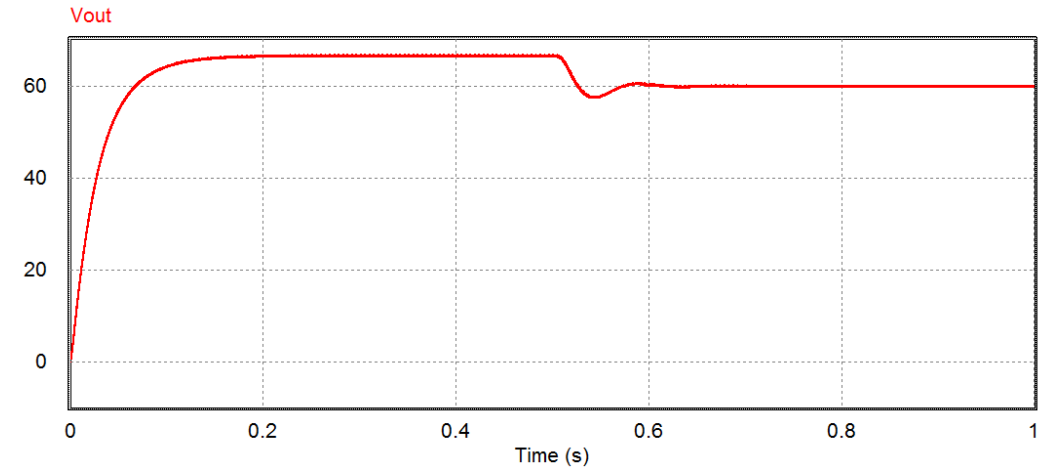
(c)

Fig. 5.27 Port voltages at transformer side (a), input port currents referred to high voltage side (b) and port currents at transformer side (red: port#1, blue:port#2,green:output port).

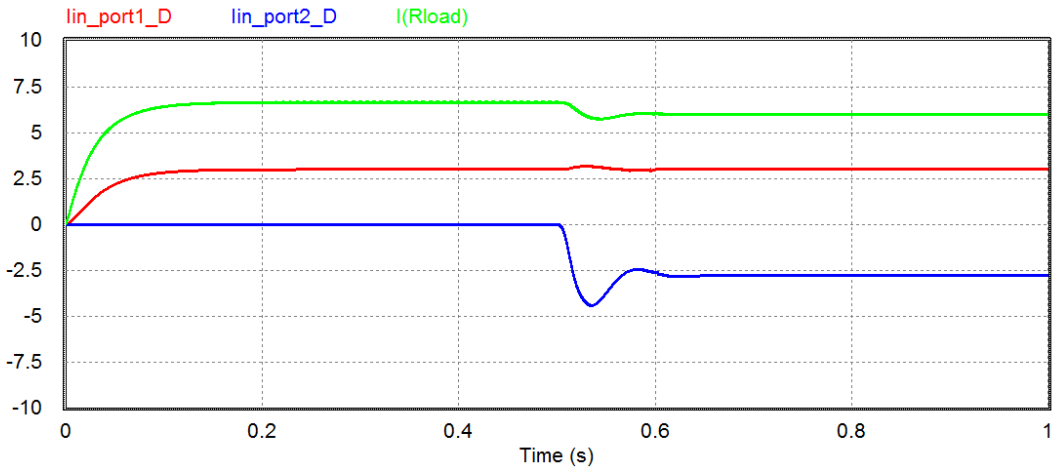
2) ***Port #1 transfers power to load and port #2***

FDCM

Let us consider the case when port #1 transfers more power of the necessary to the output port so that to keep the output voltage constant port #2 absorbs the surplus. Considering the project specifications, the voltage ratio is $V_o/V_i<0.5$ and the simulation falls in the case B1. The current reference of port #1 is set to 3 A. To avoid a not desirable switching between the two working situations under analysis due to the ripple of the output voltage or current, a small hysteresis for the switching of the control strategy is set. The port #2 PWM and control are turned on after 0.5 s. The output voltage and the DC current of the three ports are shown in Fig. 5.28 (a) and Fig. 5.28 (b) respectively. Fig. 5.28 (a) shows that the output voltage reaches about 66.6 V with only port #1 operating. At 0.5 s port#2 starts to operate and decreases the voltage to 60 V, which is the reference value. Fig. 5.28 (b) shows the DC current of the input port #1 (red) that follows the reference value of 3 A, the DC current of the input port #2 (blue), which is of -2.75 A, and the output DC current of 6 A after the turn on of port #2. The power delivered from port #1 is 450 W, of which 360 W are delivered to the output port and 71.5 W are absorbed by port #2. In this case, 18.5 W are lost in the parasitic resistances. The results highlight that the control is working properly.



(a)

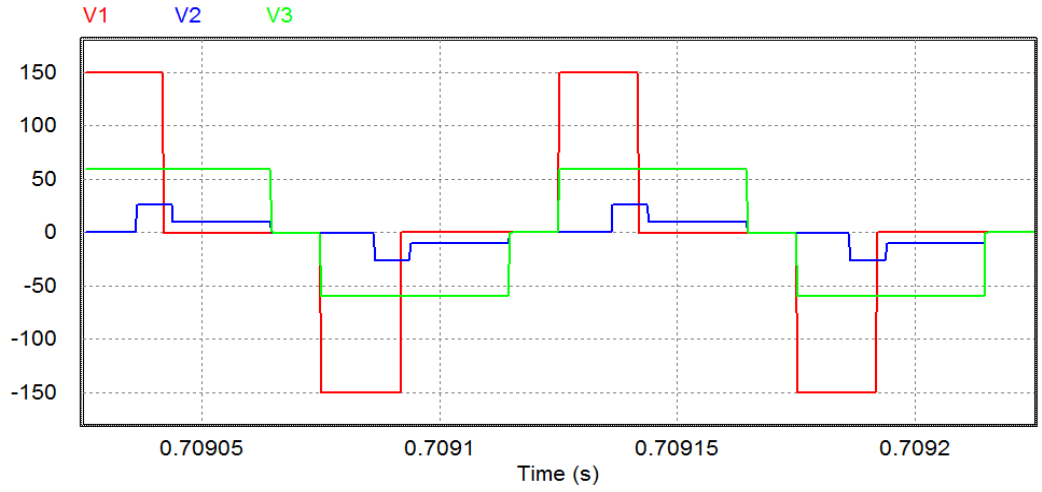


(b)

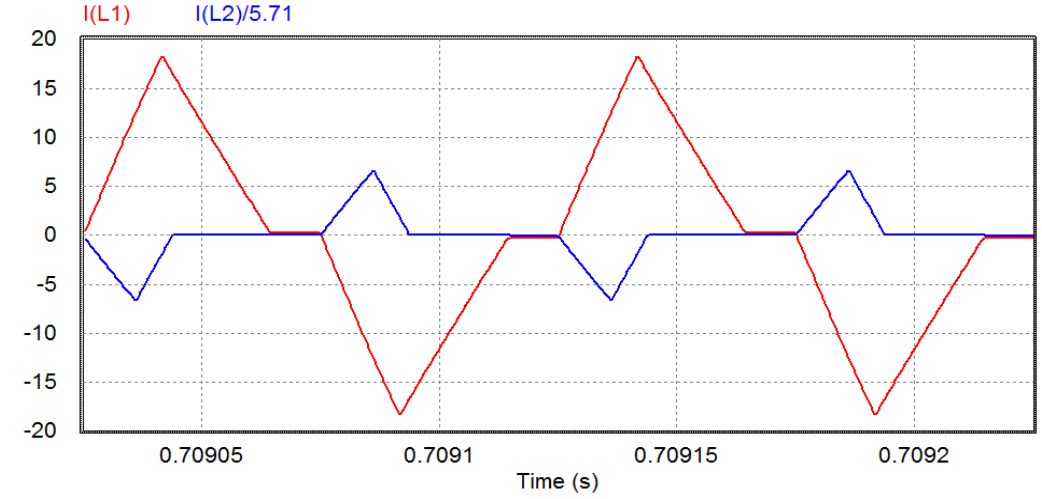
Fig. 5.28 Output voltage (a) and, input (red and blue) and output (green) DC current.

The waveforms of the voltages and currents at transformer side are shown in Fig. 5.29. The waveforms of the voltages in Fig. 5.29 (a) validate those illustrated in the previously done analysis.

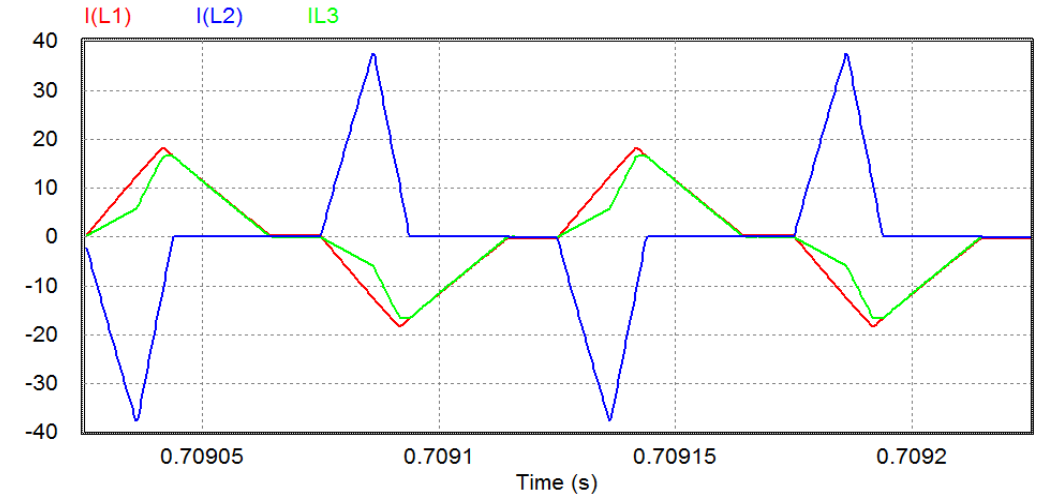
Fig. 5.29 (b) shows the two input currents referred to high voltage side. As mentioned for the case B1 with $V_o/V_i<0.5$, port#2 is activated at $\theta=0$ (the phase shift γ is zero). Then, the considerations done during the mathematical analysis are validated. Fig. 5.29 (c) shows the two input currents, referred to their port, and the output current at high frequency side.



(a)



(b)

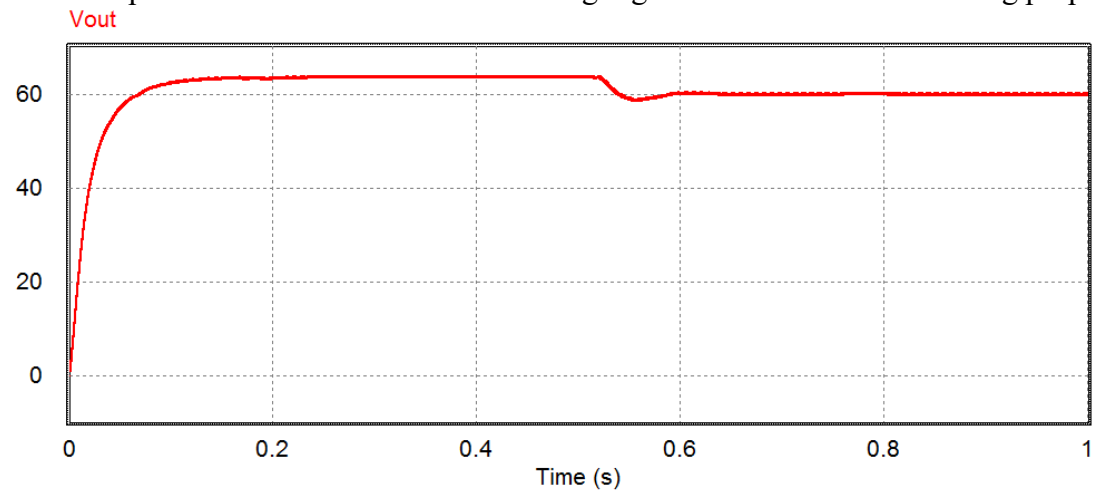


(c)

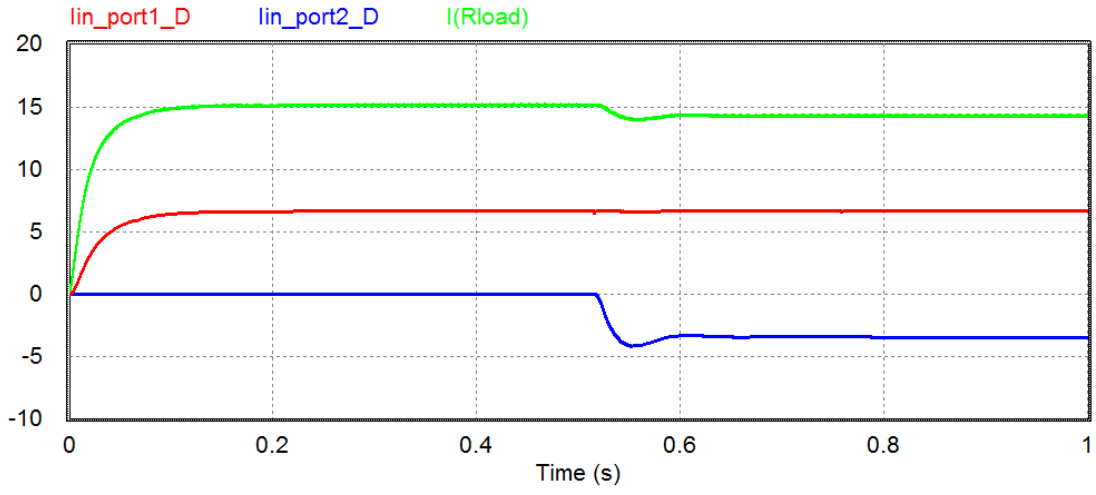
Fig. 5.29 Port voltages at transformer side (a), input port currents referred to high voltage side (b) and port currents at transformer (red: port#1, blue:port#2,green:output port).

MDCM

Let us consider the case when port #2 absorbs the surplus power and port #1 is operating in CCM. The load resistance is 4.2Ω. Considering the voltages of the ports $V_o/V_i<0.5$ and the command variable α_1 around 1.9 rad, the simulation falls in the case D1b. The current reference of port #1 is set to 6.67 A, which corresponds to the maximum power chosen for the design of port #1. The port #2 PWM and control is turned on after 0.5 s. The output voltage and the DC current of the three ports are shown in Fig. 5.30 (a) and Fig. 5.30 (b) respectively. Fig. 5.30 (a) shows that the output voltage reaches about 64 V with only port #1 operating. At 0.5 s port#2 starts to operate and decreases the voltage to 60 V, which is the reference value. Fig. 5.30 (b) shows the DC current of the input port #1 (red) that follows the reference value of 6.67 A, the DC current of the input port #2 (blue) which is -3.5 A, and the output DC current of 14.3 A after the turn on of port #2. The power delivered from port #1 is 1 kW, of which 858 W are delivered to the output port and 91 W are absorbed by port #2; 51 W are lost in the parasitic resistances. The results highlight that the control is working properly.



(a)

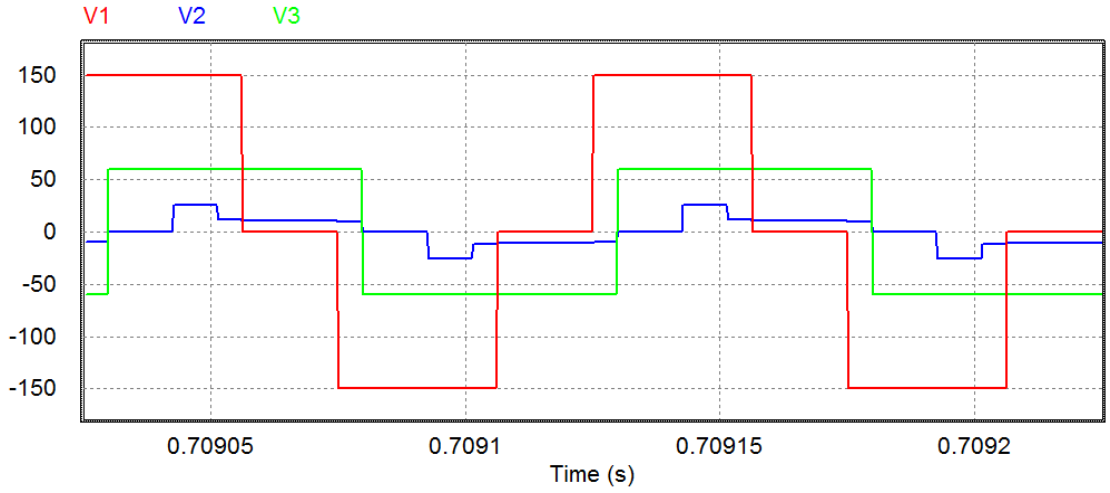


(b)

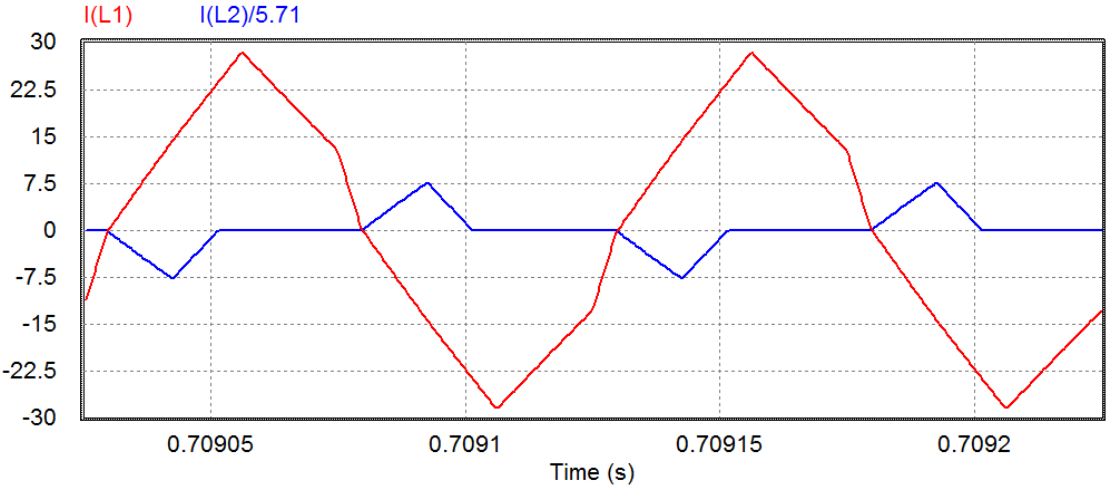
Fig. 5.30 Output voltage (a) and, input (red and blue) and output (green) DC current.

The waveforms of the voltages and currents at transformer side are shown in Fig. 5.31. The waveforms of the voltages in Fig. 5.31 (a) validate those illustrated in the previously done analysis. Fig. 5.31 (b) shows the two input currents referred to high voltage side. As mentioned for the case D1b with $V_o/V_i<0.5$ and $\alpha_1>1.758$ rad, the phase shift γ set is equal to φ_1. Fig. 5.31 (c) shows the two

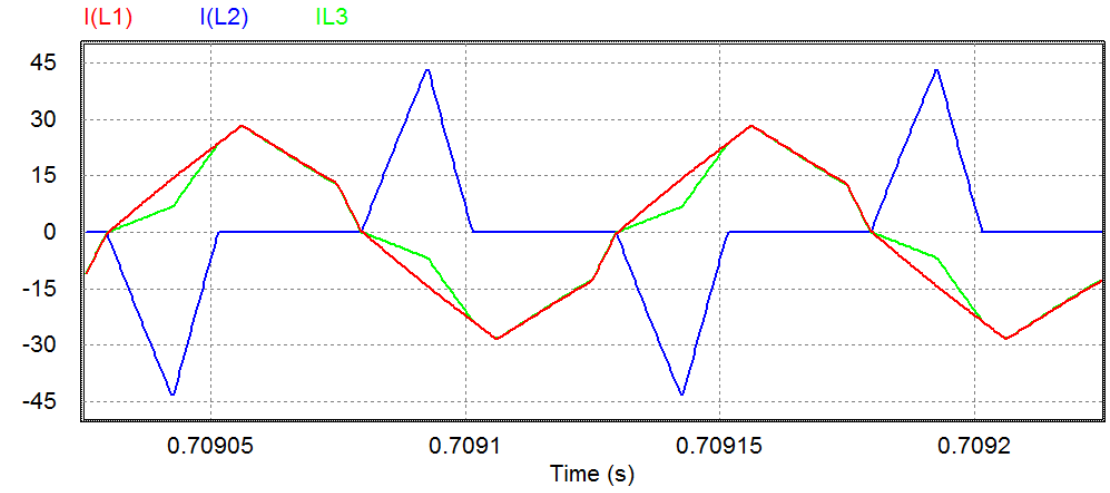
input currents, referred to their port, and the output current at transformer side. The simulation results validate the mathematical previously done analysis.



(a)



(b)



(c)

Fig. 5.31 Port voltages at transformer side (a), input port currents referred to high voltage side (b) and port currents at transformer side (red: port#1, blue:port#2,green:output port).

5.6.2 Experimental results

The experimental setup of the TPC is realized using the H-bridge converters used for the SAB and DAB experiments. The only difference between the three ports is the insertion of the diodes instead the MOSFET's in the passive port. Also in this case, the experiments are performed at reduced power. The components characteristics and description are reported in the subparagraph 3.5.2 of the SAB chapter. The active port #1 is connected to one of the two high voltage windings of the transformer through an additional inductance of 65μH (65uH+11uH(transformer)=76uH). In the same way, the active port #2 is connected to the low voltage winding through an additional inductance of 1.22uH ($1.22u*5.71^2$+58u(transf.)=98uH). Instead, the output port is connected directly to the other high voltage winding. The insertion of the additional inductances has the main function to limit the ripple of the currents and their values are selected to obtain more or less, considering the transformer inductances, two equal total inductances. As mentioned in the previous paragraph, the two resulting inductances are not perfectly equal being that one connected to port #2 a bit higher. This results is a lower slope of the current of port #2 at the transformer side. Furthermore, as for the SAB converter, the presence of the parasitic resistance of the additional inductances coils smoothens current waveforms. However, these differences does not influence the results of the experiments.

Two electrolytic capacitors of 1000 uF, 450 Vcc produced by EPCOS, are used at DC side of each port. The system is feed using the DC power supply 6030A of the Agilent for port #1 and three battery cells of 4 V for the port #2. A variable resistance is connected to the output port.

As for SAB and DAB, the control algorithm is implemented using the Digital Signal Processor (DSP) TMS320F28335 produced by Texas Instruments. The software Code Composer Studio (CCS) v6, which is provided by Texas Instruments, is used for the programming of the processor.

To implement the soft-switching capabilities analyzed for the SAB and DAB converters, the equations for the capacitor design reported in paragraph 3.4.1 are used. For port #1 a capacitance of 23.5nF is used in the MOSFET's of the lagging leg; in the leading leg a capacitance of 20.4nF in series to a resistance of 41 Ω. The resistance is inserted to limit the current due to the capacitor discharge when the bridge operates in DCM. A better solution can be obtained using a diode in parallel to the resistance but in this experiment it is not implemented. The values of the capacitances used for the leading and lagging legs are different because their values depends on the maximum peak current reachable that it is different for the two legs. It results higher for the lagging leg. The computed capacitance for port #2 is 100nF. However, port #2 has a function of support to port #1 and it often operates in DCM with low currents, making unpractical the use of the soft-switching capacitor alone, so they are not used in port #2 for the experiments relevant to the TPC reported in this chapter. The experimental setup of the TPC is shown in Fig. 5.32.

As for the previous subparagraphs, two working situations are tested, each in FDCM and MDCM. Port #1 is supplied at 69 V, port #2 is connected to three battery cells of 4 V for a total of 12V and the voltage reference of the output port is set to 24 V. A test with the voltage reference set to 48V is done to evaluate the variation of the efficiency with different values of current and voltage. The load resistance is changed to get the different operation conditions under testing. The sequence of the experiments follows the same of the simulations.

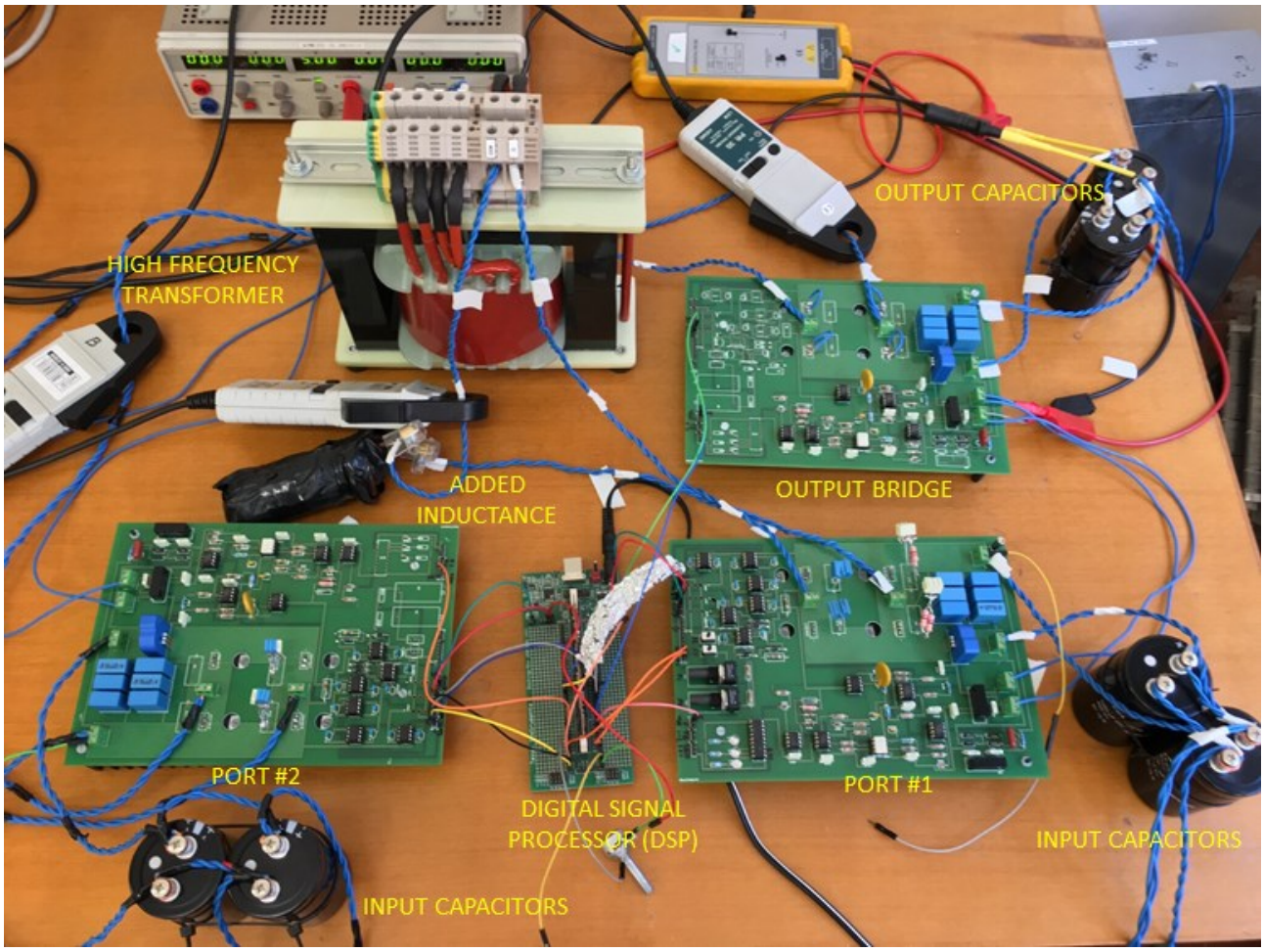


Fig. 5.32 Experimental setup of the TPC converter

1) Load power delivery by both the active ports

FDCM

Let us consider the case when the load power is delivered by both the ports in FDCM. The current reference of port #1 is set to 1.6 A. The output voltage reference is set to 24 V and the load resistance is 5.6 Ω. The output voltage and current and the three currents at transformer side are shown in Fig. 5.33 (a) and (b) respectively. Fig. 5.33 (a) shows that the output voltage (green line) reaches the 24 V set in the control. The output current is 4.3A and the power transferred to the load is 103 W. Fig. 5.33 (b) shows the output current (yellow line), the current of port #1 (violet line) and the current of port #2 (blue light line) at low voltage side. It is visible that the difference in the areas between the output current and the current delivered by port #1 correspond to the part delivered by port #2. Since the port #1 operates in DCM, the phase shift between the commands of the two bridges is zero and the currents start at the same instant. The DC input current of port #1 is 1.6 A, as imposed by the control, and the DC current of port #2 is 2.7 A. The AC peak current is 8.5 A and about 14 A for port#1 and 2, respectively. The total power delivered by the input ports is 143 W and the efficiency is 72-73%. It results low because the system is working at low power and the operating conditions of low voltages and high currents lead an increase of the losses in the wirings and in the power switches. A subsequent test performed at higher voltage output conditions validates this statement. The input currents with the current of port #2 referred to high voltage side are shown in Fig 5.34.

(a)

(b)

Fig. 5.33 (a) output voltage (green) and current (yellow), and (b) current at transformer of port #1 (violet), port #2 (light blue) and output port (yellow).

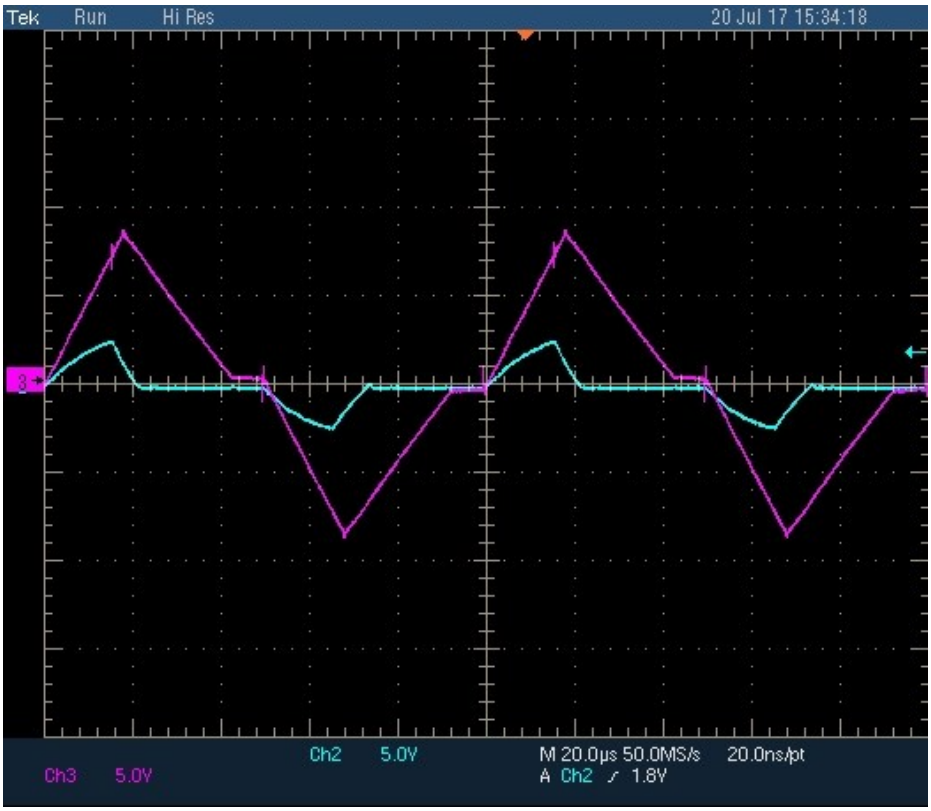
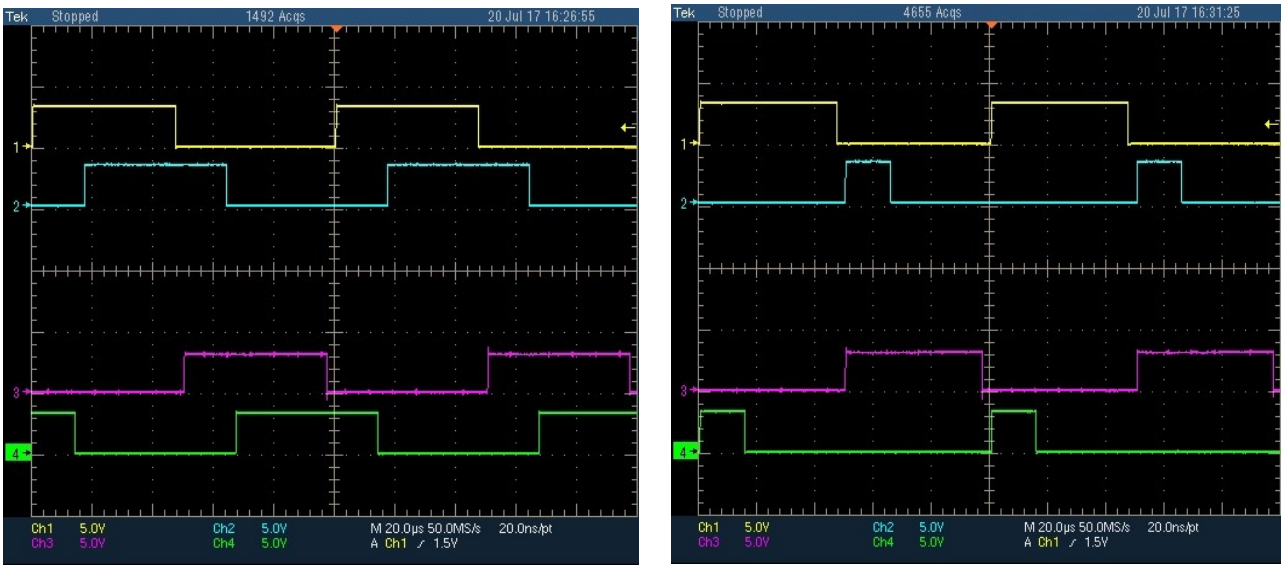


Fig. 5.34 Current at transformer side of port #1 (violet) and port #2 (light blue) referred at high voltage side.

The MOSFET commands of port #1 and port #2 are reported in Fig. 5.35 (a) and (b) respectively. It is visible that the MOSFET of the lagging leg of port #2 (light blue and green) are turned off after the phase shift to avoid the reflow of the current between the two ports after the zero crossing of the port #2 current.

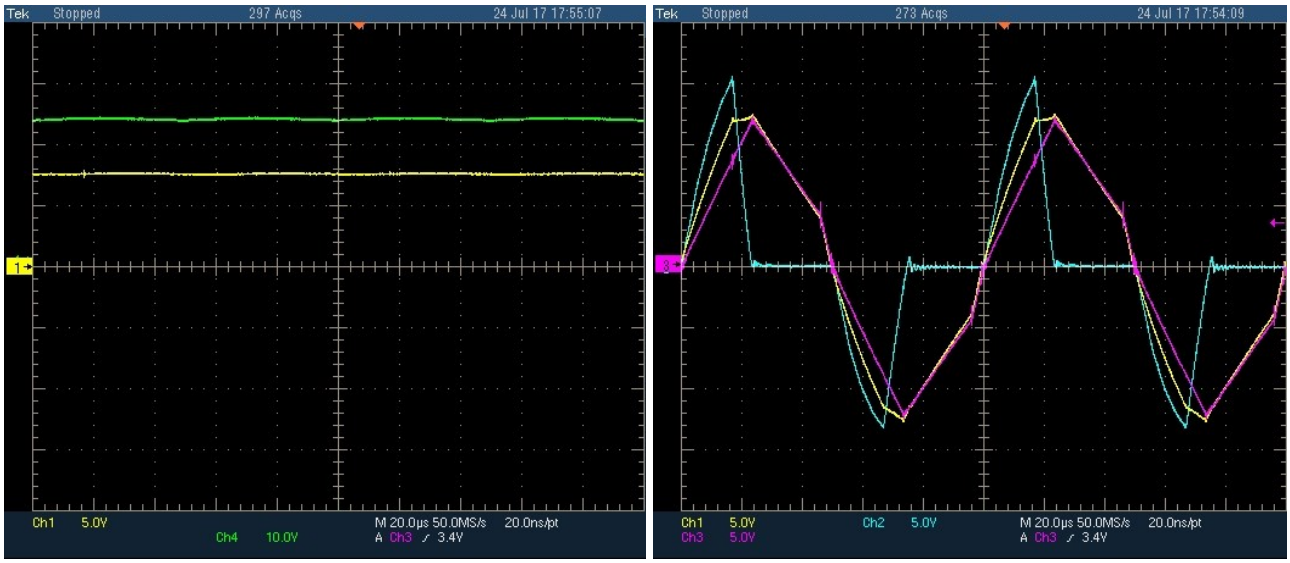


(a) (b)

Fig. 5.35 (a) Commands of upper (S_1-yellow, S_3-light blue) and lower (S_2-violet, S_4-green) MOSFETs of port #1 and, (b) commands of upper (S_5-yellow, S_7-light blue) and lower (S_6-violet, S_8-green) MOSFETs of port #2.

MDCM

Let us consider the case when the load power is delivered by both the ports in MDCM. The current reference of port #1 is set to 3 A. The output voltage reference is set to 24 V and the load resistance is 3.2 Ω. The output voltage and current and the three currents at transformer side are shown in Fig. 5.36 (a) and (b) respectively. Fig. 5.36 (a) shows that the output voltage (green line) reaches the 24 V set in the control. The output current is 7.5 A and the power transferred to the load is 180 W. Fig. 5.36 (b) shows the output current (yellow line), the current of port #1 (violet line) and the current of port #2 (blue light line) at low voltage side. Because port #1 operates in CCM there is a phase shift between the commands of the two bridges and the current of port #2 starts when the current of port #1 crosses the zero. The DC input current of port #1 is 3 A, as requested by the control, and the current of port #2 is 3 A. The AC peak current is 12 A and about 15 A for port#1 and 2, respectively. The total power delivered by the input ports is 243 W and the efficiency is around 74-75%, a bit higher than in the previous case. The input currents with the current of port #2 referred to high voltage side are shown in Fig 5.37.



(a) (b)

Fig. 5.36 (a) output voltage (green) and current (yellow), and (b) current at transformer side of port #1 (violet), port #2 (light blue) and output port (yellow).

Fig. 5.37 Current at transformer side of port #1 (violet) and port #2 (light blue) referred at high voltage side.

The MOSFET commands of port #1 and port #2 are reported in Fig. 5.38. It is visible that between the MOSFET commands of port #1 and port #2 there is a phase shift, which is necessary to maintain each current independent from the other.

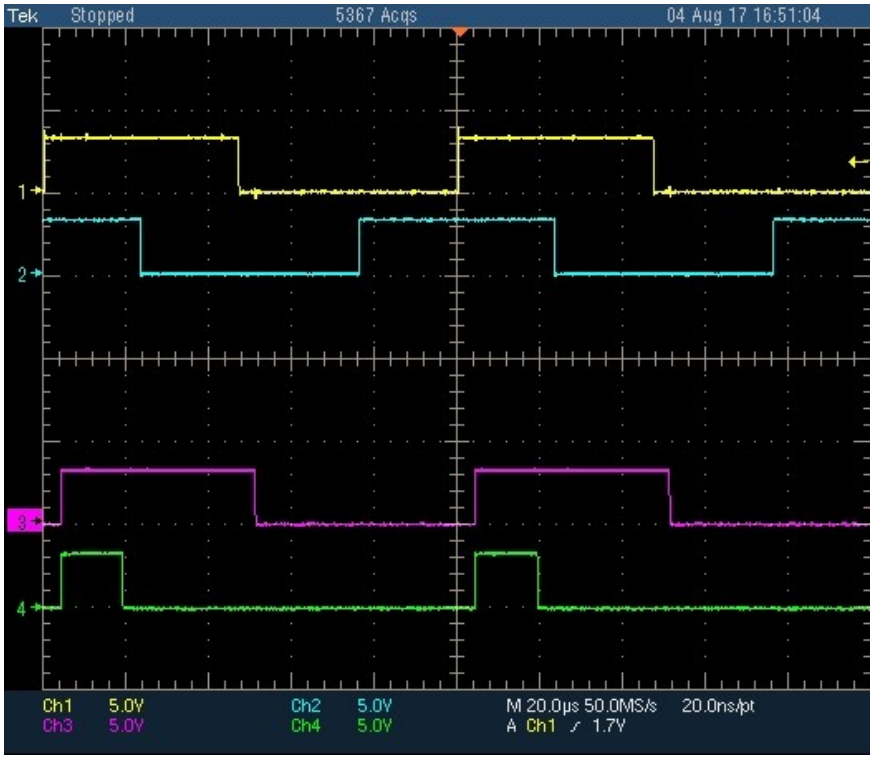
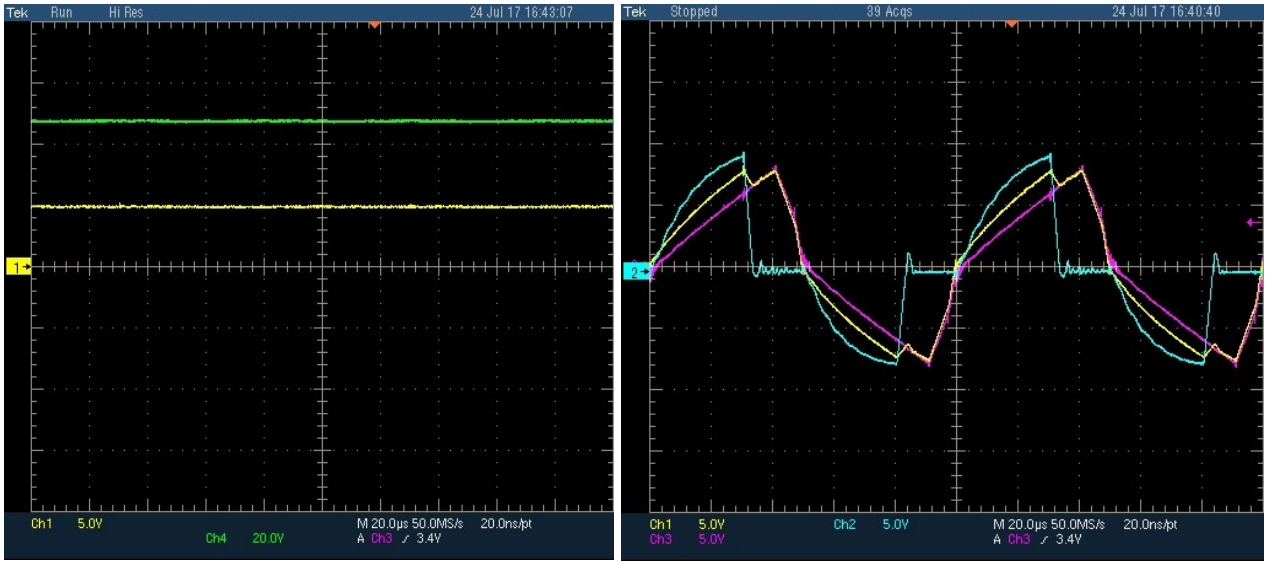


Fig. 5.38 Commands of port #1 (S_1-yellow, S_4-light blue) and commands of port #2 (S_5-violet, S_8-green) in MDCM.

Let us consider the case when the load power is delivered by both the ports in MDCM but with the output voltage reference set to 48V instead of 24V. The current reference of port #1 is set to 3.5 A. The load resistance is 9.6 Ω. The output voltage and current and the three currents at transformer side are shown in Fig. 5.39 (a) and (b) respectively. Fig. 5.39 (a) shows that the output voltage (green line) reaches the 48 V set in the control. The output current is 5 A and the power transferred to the load is 240 W. Fig. 5.39 (b) shows the output current (yellow line), the current of port #1 (violet line) and the current of port #2 (blue light line) at low voltage side. The DC input current of port #1 is 3.5 A, as requested by the control, and the current of port #2 is 3.6 A. The AC peak current is 7.8 A and about 9 A for port #1 and 2, respectively. The total power delivered by the input ports is 285 W and the efficiency is around 84-85%. As previous discussed, the efficiency increases working with higher voltages and lower currents. Considering SAB and DAB performances, the measured efficiency is aligned with their efficiencies, which were around 80-90%. The input currents with the current of port #2 referred to high voltage side are shown in Fig 5.40.



(a) (b)

Fig. 5.39 (a) output voltage (green) and current (yellow), and (b) current at transformer side of port #1 (violet), port #2 (light blue) and output port (yellow).

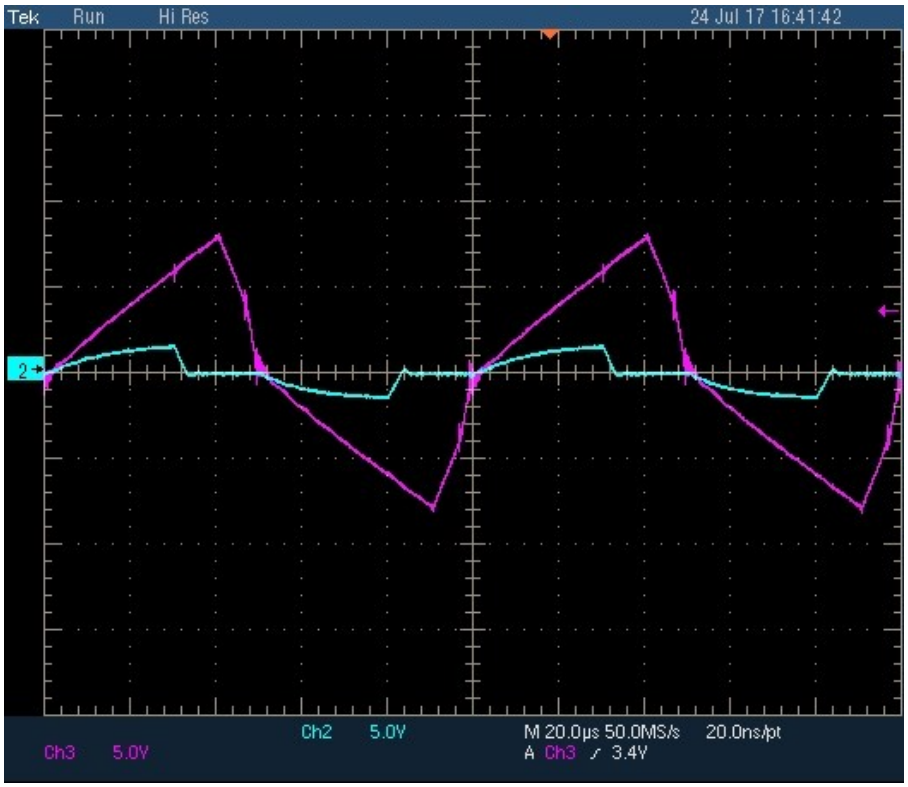
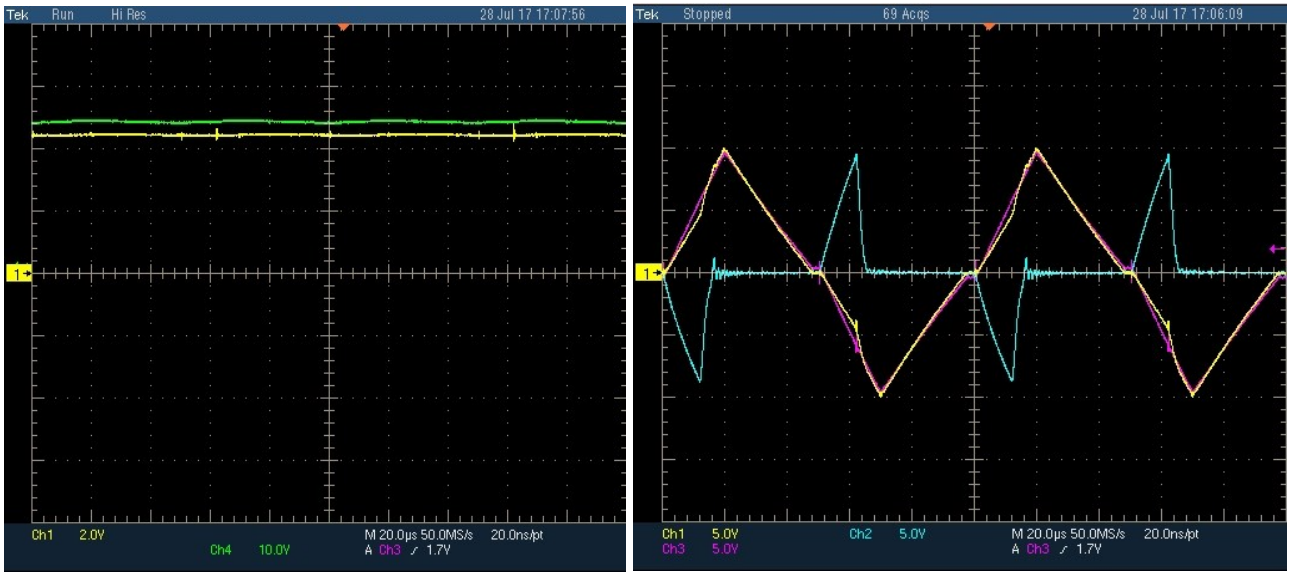


Fig. 5.40 Current at transformer side of port #1 (violet) and port #2 (light blue) referred to high voltage side.

2) Port #1 transfers power to load and port #2

FDCM

Let us consider the case when port #1 transfers more power than the required to the output port and port #2 absorbs the part in surplus to keep the output voltage constant. The current reference of port #1 is set to 2 A. The output voltage reference is set to 24 V and the load resistance is 5.5 Ω. The output voltage and current and the three currents at transformer side are shown in Fig. 5.41 (a) and (b) respectively. Fig. 5.41 (a) shows that the output voltage (green line) reaches the 24 V set in the control. The output current is 4.4 A and the power transferred to the load is 105 W. Fig. 5.41 (b) shows the output current (yellow line), the current of port #1 (violet line) and the current of port #2 (blue light line) at low voltage side. Since port #1 operates in DCM, the phase shift between the commands of the two bridges is zero and the currents start at the same instant. The AC peak current is 10 A and about 9 A for port #1 and 2, respectively. The DC input current of port #1 is 2 A, as imposed by the control, and the current of port #2 is -0.6 A. Then, the power delivered by port #1 is about 140 W and the power absorbed by port #2 is 7 W. The efficiency, considering the total output power given by the sum of the power delivered to the load and the power absorbed by port #2, is around 79-80%. It is higher than in the previous cases with 24 V at output because in port #2 only a MOSFET is commutated and therefore the switching losses are lower. The input currents with the current of port #2 referred to high voltage side are shown in Fig 5.42.



(a) (b)

Fig. 5.41 (a) output voltage (green) and current (yellow), and (b) current at transformer side of port #1 (violet), port #2 (light blue) and output port (yellow).

Fig. 5.42 Current at transformer side of port #1 (violet) and port #2 (light blue) referred to high voltage side.

The MOSFET commands of port #1 and port #2 are reported in Fig. 5.43. It reports the commands of S_1 and S_4 of port #1, and S_7 and S_8 of port #2. The commands of S_2 and S_3 of port #1 are complementary to those of the switches S_1 and S_4. On the other hand, the commands of the two switches S_5 and S_6 of port #2 are always kept low.

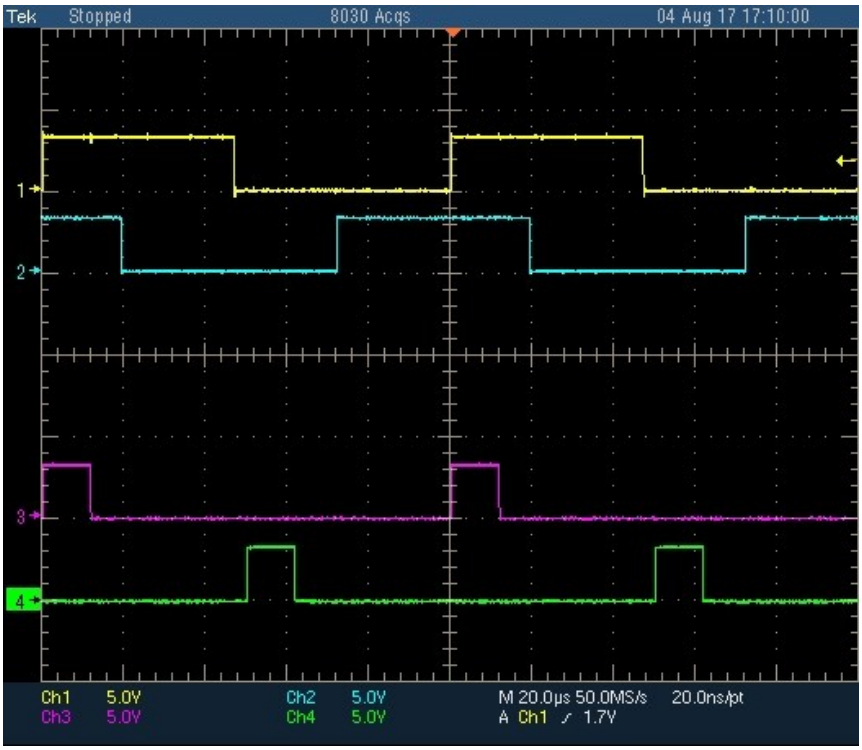
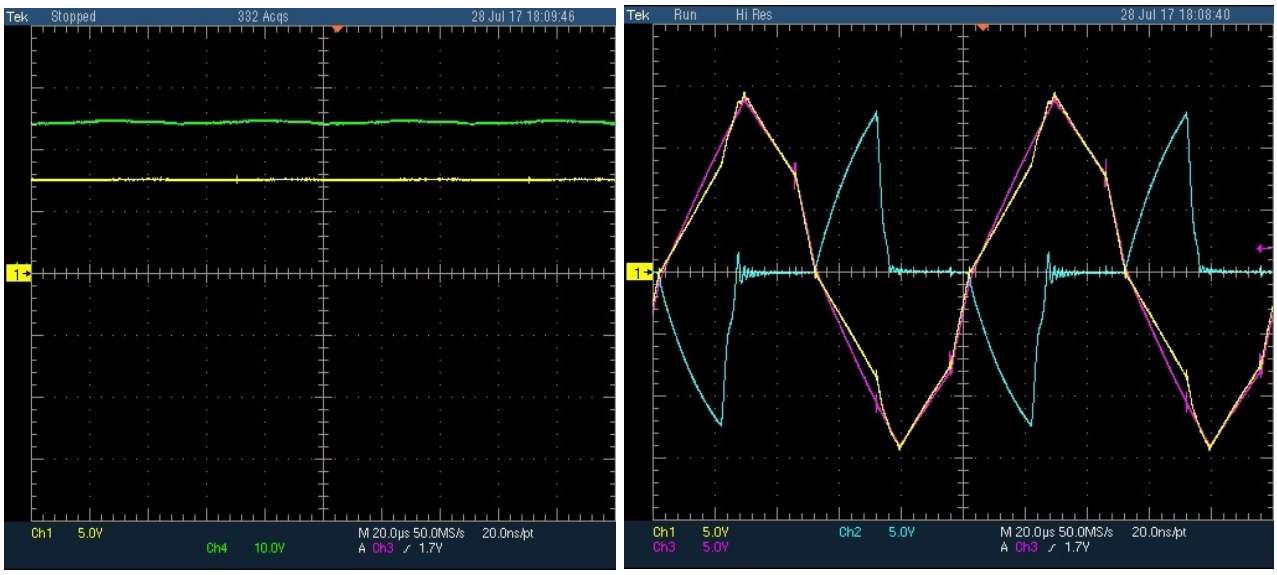


Fig. 5.43 Commands of port #1 (S_1-yellow, S_4-light blue) and commands of port #2 (S_7-violet, S_8-green) in FDCM.

MDCM

Let us consider the case when port #1 transfers more power of the necessary to the output port and port #2, operating in MDCM, absorbs the part in surplus to keep the output voltage constant. The current reference of port #1 is set to 3.6 A. The output voltage reference is set to 24 V and the load resistance is 3.2 Ω. The output voltage and current and the three currents at transformer side are shown in Fig. 5.44 (a) and (b) respectively. Fig. 5.44 (a) shows that the output voltage (green line) reaches the 24 V set in the control. The output current is 7.5 A and the power transferred to the load is 180 W. Fig. 5.44 (b) shows the output current (yellow line), the current of port #1 (violet line) and the current of port #2 (blue light line) at low voltage side. Because port #1 operates in CCM, there is a phase shift between the commands of the two bridges and the current of port #2 starts when the current of port #1 crosses the zero. The AC peak current is 14 A and about 12.5 A for port #1 and 2, respectively. The DC input current of port #1 is 3.6 A, as requested by the control, and the current of port #2 is around -1.25 A. Then, the power delivered by port #1 is about 250 W and the power absorbed by port #2 is 15 W.

The efficiency, considering the total output power given by the sum of the power delivered to the load and the power absorbed by port #2, is around 78-79%. It is still higher than the tests of case 1) with 24 V at output but, considering the previous test of case 2) in FDCM, it is a bit lower because the increasing of the currents increases the losses. The input currents with the current of port #2 referred to high voltage side are shown in Fig 5.45.



(a) (b)

Fig. 5.44 (a) output voltage (green) and current (yellow), and (b) current at transformer side of port #1 (violet), port #2 (light blue) and output port (yellow).

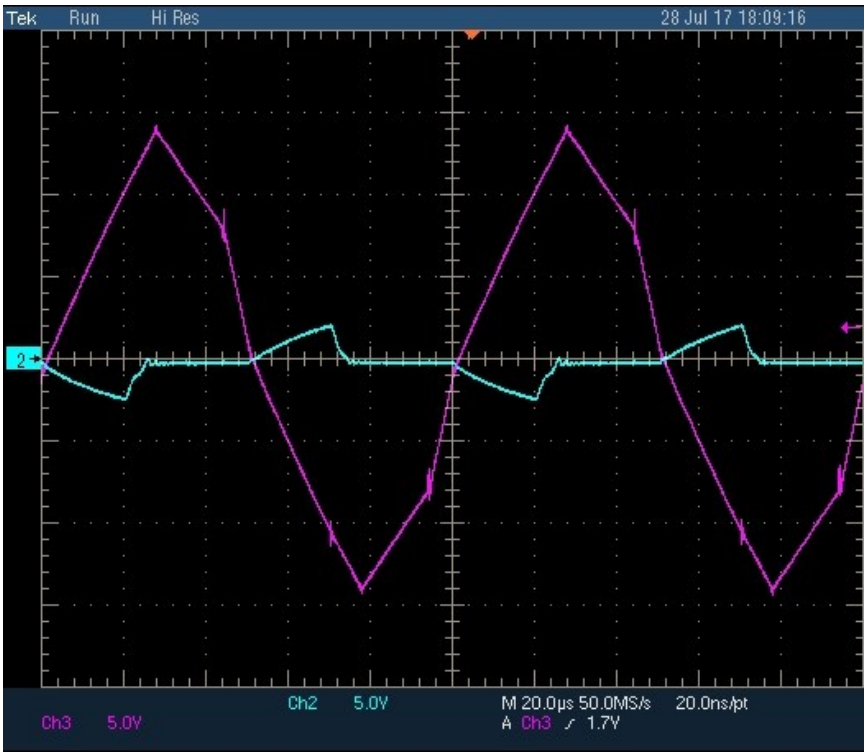


Fig. 5.45 Current at transformer side of port #1 (violet) and port #2 (light blue) referred to high voltage side.

The MOSFET commands of port #1 and port #2 are reported in Fig. 5.46. It is visible that between the MOSFET commands of port #1 and port #2 there is a phase shift, which is necessary to maintain the currents independent.

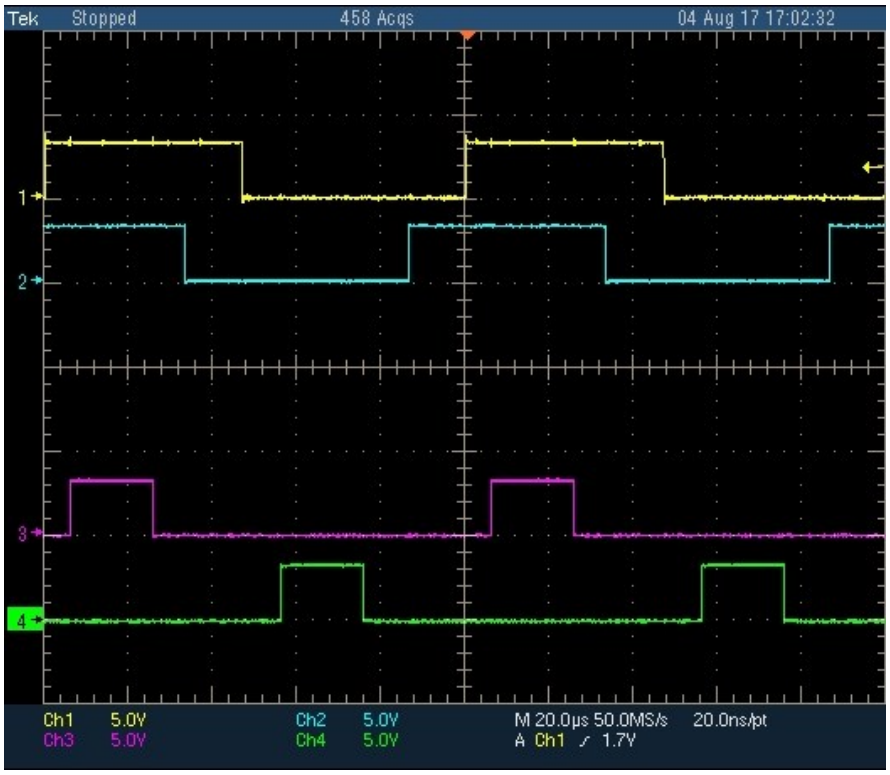


Fig. 5.46 Commands of port #1 (S_1-yellow, S_4-light blue) and commands of port #2 (S_7-violet, S_8-green) in MDCM.

CHAPTER 6

AC-DC conversion stage

Power supply systems for many applications need rectification of the grid voltage that, if done with diode rectifiers, injects harmonics of current into the grid. They impair the power quality of the grid service by distorting the delivered voltage. Such a voltage feeds in an improper way the connected equipment, overheating it and causing its malfunctioning or even making it unworkable. The issue of the power quality has led to standards that limit the admissible current harmonics that a rectifier, or an equipment with a rectifier as an input stage, can draw from the grid.

Compliance of the grid rectifiers with the power quality demands can be evaluated in terms of power factor (PF) of the current absorbed from the grid, which is defined as the ratio between the real power P and the apparent power S. For a sinusoidal voltage source, the PF is given by

$$Power\ Factor\ (PF) = \frac{P}{S} = \frac{V_S I_{S1} \cos\varphi_1}{V_S I_S} = \frac{I_{S1}}{I_S}\cos\varphi_1 = K_p \cdot DPF \qquad (6.1)$$

where

-I_{s1} is the current component referred to the fundamental frequency

-$K_p = \frac{I_{S1}}{I_S} = \frac{1}{\sqrt{1+THD_i{}^2}}$ is the distortion factor, with $THD_i = \frac{I_{harm}}{I_{S1}}$ the Total Harmonic Distortion of the current.

-$DPF = \cos\varphi_1$ is the Displacement Power Factor, with φ_1 the angle between the fundamental component of the current and the voltage.

PF, in turn, depends on the total current harmonic distortion and the current displacement factor. The modern approach to meet the power quality demands consists in paralleling the rectifiers with power conditioning converters that filter the current harmonics and compensate for the displacement factor. However, the use of additional converters makes the approach complex and costly. The solution aimed at preserving the power quality of the grid service without recourse to additional converters is the PF-compliant rectifier.

Among the various families of PF-compliant rectifiers, the ones based on the power factor correction (PFC) have received more attention for applications requiring a unidirectional energy flow [65]-[72]. They are controlled converters, operated in the way of forcing the current absorbed from the grid to have the same waveform of the voltage and the phase with the grid voltage to be zero.

In literature several papers present reviews of the PFC topologies most widespread and used in applications. A review of single-phase PFC topologies is presented in [73], [74]. In particular, an overview of the PFC topologies based on boost converter is treated in [75]-[77]. A review of three-phase PFC topologies is presented in [78]-[82]. A comparative analysis of the basic circuits for PFC is reported in [83]-[88]. Several examples of high power applications of the PFC circuits, such as telecommunications applications, electric vehicle battery charger, wind power system, permanent magnet generator, application in high temperature, and so on… are reported in [89]-[96].

Among the several studied topologies, the first analysed and implemented are the classical PFC circuits composed by a single-phase or three-phase diode rectifier and a single-switch [97]-[104]. Afterwards, new topologies of PFC, without the diode rectifier, have been studied to reduce the

number of components and losses in order to improve the efficiency of the conversion stage [105]-[110]. In the recent years, from the combination of the single and three-phase diode rectifiers and classical boost converters, new topologies of PFC with higher complexity and new performance have been developed [111]-[112].

To improve the efficiency and performances of the SST, the PFC circuits are adopted in the AC-DC and DC-AC conversion stages. This chapter presents an excursus on the boost PFC rectifier topologies, illustrating for each topology the single-phase version and the three-phase counterpart, with an analysis of their operation and features. In particular, a boost PFC has been analyzed and realized as the AC-DC conversion stage of the SST port connected to the grid.

In the subsequent analysis of the PFC topologies, the following notations are used: lower-case symbols denote instantaneous quantities, lower-case symbols with a bar as superscript denote space phasors, upper-case symbols denote DC quantities or specific values of the variable quantities and the symbol q stays for a generic quantity.

Diagrams of quantities are obtained from a computer-assisted analysis and are referred to data of a possible application. They are normalized as follows: the currents to their peak value, the voltages to the DC side voltage, and the time to the grid period.

6.1 PFC converter basics

The schematic of a diode rectifier for the supply of a DC load is shown in Fig. 6.1. Its circuit is composed of four diodes which compose the full bridge, an inductance, which acts as a current filter, and the output capacitor, which acts as a voltage filter and reduces the ripple of the DC voltage.

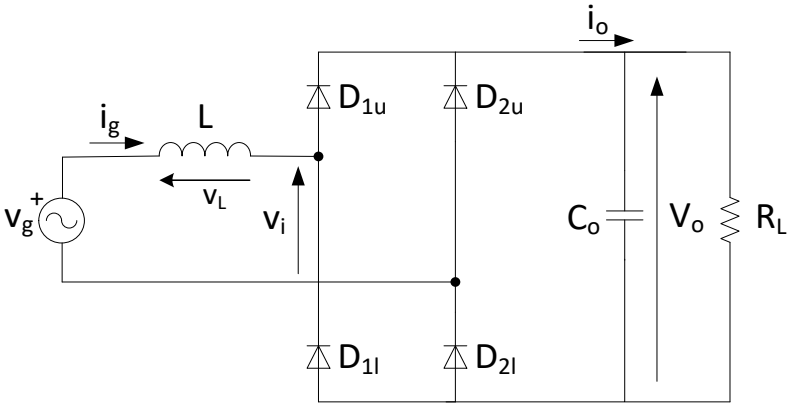
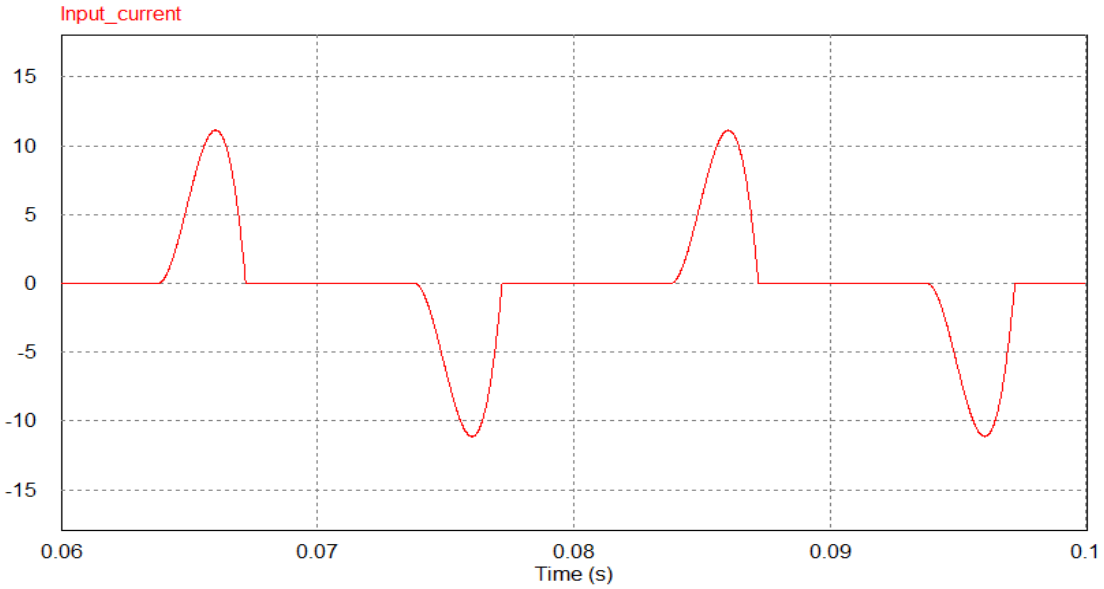
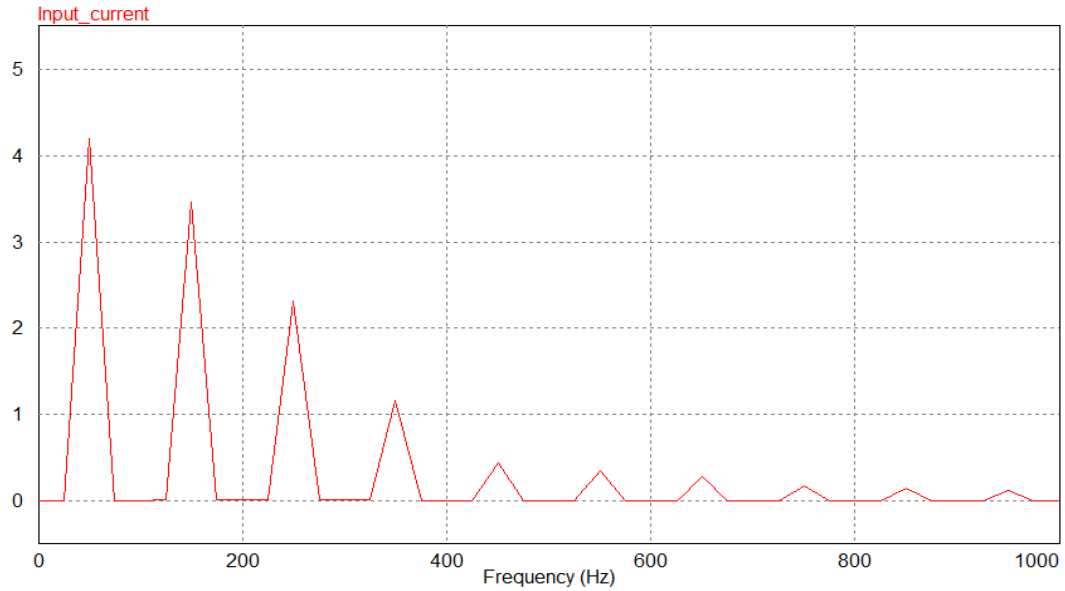


Fig. 6.1. Diode rectifier.

The input current i_g is highly distorted. As shown in Figs. 6.2 (a) and (b), it is a pulsating current with a high harmonic content. The spectrum shows that the frequency of the harmonics is multiple of the fundamental component at 50 Hz. Furthermore, due to the half-wave symmetry only the odd harmonics are present.



(a)



(b)

Fig. 6.2. Input current waveform (a) and spectrum (b).

The classical PFC rectifier with the inductor in the AC side has the scheme of Fig. 6.3. The output stage of the scheme includes load resistance RL, capacitor Co and diode D that prevents short-circuit of the capacitor when transistor T is on. The capacitor keeps constant voltage V_o across RL by filtering the harmonics of output current i_o of the PFC rectifier.

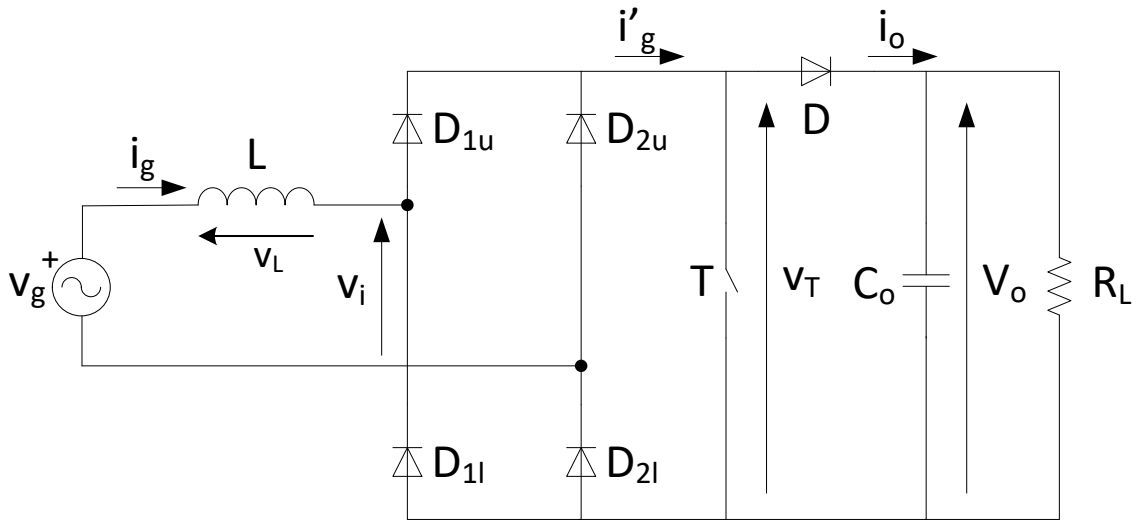


Fig.6.3. AC side inductance PFC rectifier.

For single-phase systems, a fictitious α,β transformation is defined to represent voltages and currents in an effective manner. The α component of the transformation is the single-phase quantity whilst the β component is the single-phase quantity taken with a delay of π/2. Therefore, the space vector is defined as

$$\bar{q} = q(\theta) + jq\left(\theta - \frac{\pi}{2}\right) \tag{6.2}$$

For three-phase systems with no neutral connection, the conventional α,β transformation, given in (6.3), is utilized to represent voltages and currents.

$$\begin{bmatrix} q_\alpha \\ q_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} q_a \\ q_b \\ q_c \end{bmatrix} \tag{6.3}$$

The relevant space vector is

$$\bar{q} = q_\alpha + jq_\beta \tag{6.4}$$

Let us consider the single-phase circuit of Fig. 6.4(a), where v_g is the grid voltage, i_g is the grid current, L is an inductor and v_i is a sinusoidal voltage source controlled in both magnitude and initial phase. Expressions of v_g and v_i are

$$v_g = V_g\, sin(\theta), \quad v_i = V_i\, sin(\theta - \delta), \quad \theta = \omega t \tag{6.5}$$

where θ and ω are the instantaneous phase and the angular frequency of the grid voltage.

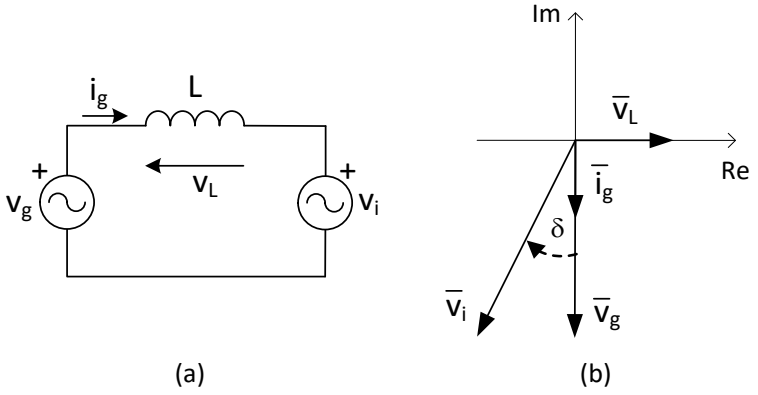


Fig.6.4. (a) PFC principle and (b) space vector diagram.

The space vector diagram of the circuit at $\theta = 0$ is traced in Fig. 2(b), where the actual quantities are the projections of the vectors on the real (Re) axis. The diagram shows that i) v_i lags i_g of an angle δ expressed as in (6.6), and ii) V_i must be greater than V_g since it has to balance, in addition to V_g, the voltage drop V_L across the inductor.

$$\delta = arctg = \frac{\omega L I_g}{V_g} \tag{6.6}$$

Let v_i be obtained by a sinusoidally modulated bridge AC-DC converter whose DC voltage is V_0. Under linear modulation, it is $V_i \leq V_0$. In all, it is

$$V_g < V_o \tag{6.7}$$

Let us consider a three-phase circuit where the three sinusoidal voltage sources with controlled magnitude and initial phase are the line-to-line voltages v_{ll} of a three-phase AC-DC converter whose DC voltage is V_0. Their peak value V_{ll} must be greater than $\sqrt{3}V_g$ to balance the voltage drop across the inductors. Moreover, for v_{ll} obtained with space vector modulation, it is $V_{ll} \leq V_o$ under linear modulation. In all, it is

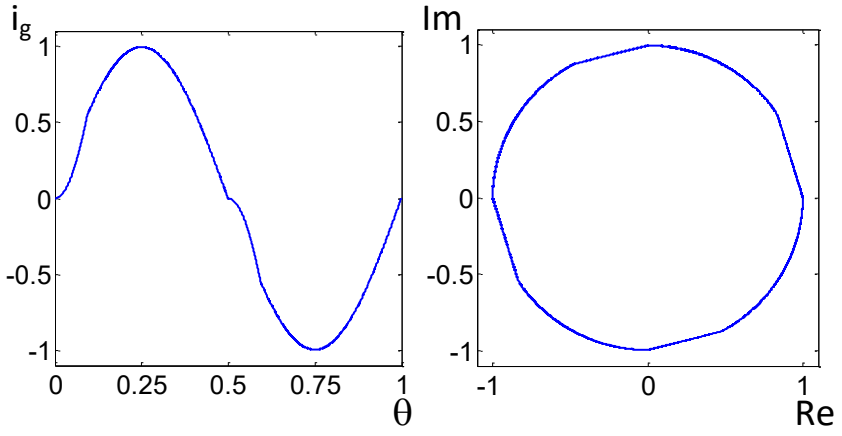
$$\sqrt{3}V_g < V_o \tag{6.8}$$

As shown by (6.7) and (6.8), the PFC circuits set up with AC-DC converters exhibit an inherent boost behavior.

Looking at Fig. 6.3, let transistor T be switched in the way of modulating sinusoidally the voltage v_i at the input of the PFC rectifier to reproduce the operation of the circuit of Fig. 6.4 (a). As a matter of fact, the circuit of Fig. 6.3 is not able to execute this action all along the grid period. Indeed, current and voltage at the input of the PFC rectifier have at each instant the same sign, while -as it can be recognized from Fig. 6.4 (b) by projecting the relevant space vectors on the Re axis- this does not occur in the angular interval from 0 to δ. Indeed, during this interval, $\bar{\imath}_g$ is positive while the required $\bar{v}_i$ is negative. To facilitate the rise of current i_g, T is kept closed so that voltage v_i is zero and current i_g is impressed by the grid voltage. Its equation is

$$i_g = \frac{V_g}{\omega L}\int_0^{\theta} sin\,(\alpha)\,d\alpha = \frac{V_g}{\omega L}[1 - cos(\theta)] \qquad 0 < \theta < \delta \tag{6.9}$$

leading to a certain distortion of current. For $\theta > \delta$, $\bar{v}_i$ becomes positive and current i_g resumes the sinusoidal waveform. This situation occurs also at the beginning of the negative half-period of the grid voltage. The resulting plot of the grid current is traced in Fig. 6.5 (a) and the trajectory of its space vector in Fig. 6.5 (b).



(a) (b)

Fig.6.5. (a) Grid current and (b) space phasor trajectory.

The classical PFC rectifier, due to its structure, is a unidirectional power converter. The duty cycle of the switch T is obtained by the need of shaping the input current in a sinusoidal waveform in phase

with the voltage. When T is turned on, the energy delivered by the voltage source is stored in the inductor and the energy required by the load is supplied by the output capacitor. When T is turned off, the diode becomes forward biased and the inductor stored energy is transferred to the output capacitor and load. The two situations are shown in Fig 6.6 (a) and (b). The switch operates at high switching frequency to reduce the size of inductor. A lower switching frequency results in lower switching losses and EMI but requires a higher inductor size.

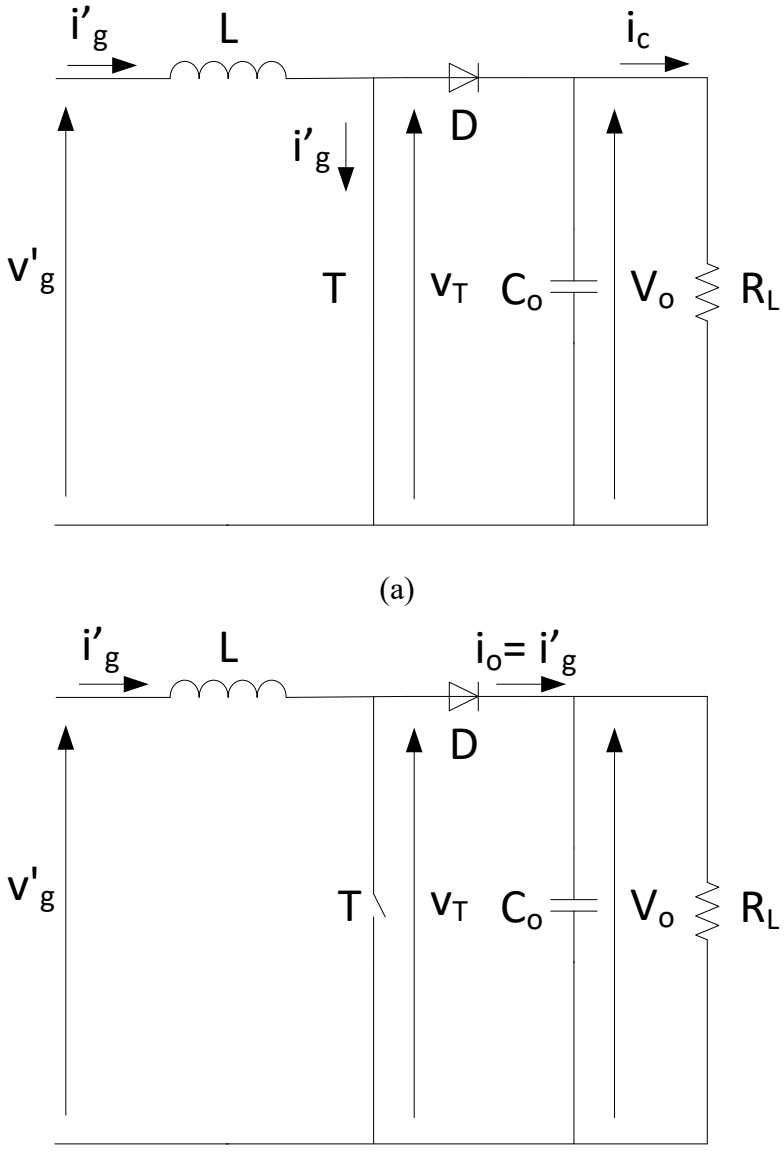


Fig.6.6. PFC equivalent circuit with T turned on (a) and T turned off (b).

The control system of a boost PFC is usually composed of two loops, an inner current loop that has a bandwidth 10-20 times lower than the switching frequency, and an outer voltage loop that has a bandwidth lower than the current loop. The higher bandwidth of the inner loop must be chosen to guarantee the stability of the system and to ensure that the current waveform responds to grid voltage changes rapidly thereby maintaining control over the shape of the current waveform.

Considering the input current, the PFC can operate in three modes: discontinuous conduction mode DCM, continuous conduction mode CCM and boundary conduction mode BCM, which is the boundary operation between the DCM and CCM. As shown in Fig. 6.7 in DCM the current is zero for an interval of the switching period, in CCM the current is higher than zero during all the switching period, and in BCM the current is zero only for a time instant during the whole switching period.

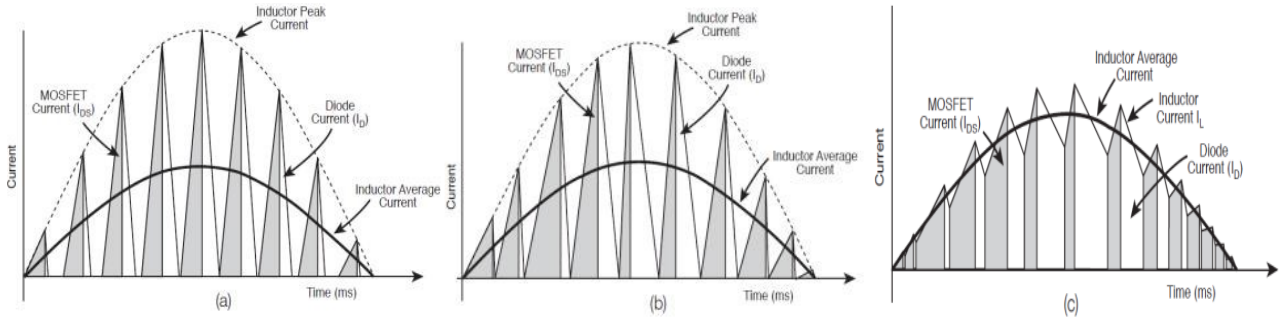


Fig.6.7. PFC current in DCM (a), BCM (b) and CCM (c).

In DCM the peak current, compared to the average current, is high and this leads to higher switching and conduction losses in the switch. Furthermore, the peak to peak current is higher and this leads to higher hysteresis losses in the inductor. The DCM is preferable in the cases where the application requires operating with a wide range of load, such as the renewable energy applications. BCM has the same disadvantages of the DCM.

In CCM the peak current, compared to the average current, and the peak to peak current are lower than in DCM. Therefore, the switch and the 3inductor losses are lower. Then, the CCM is a preferred choice for a wide range of low, medium and high power PFC applications.

6.2 Half-controlled PFC rectifier

6.3.1 Single-phase

The circuit of the single-phase half-controlled (SH) PFC rectifier with the transistors inserted in the lower side of the legs is drawn in Fig. 6.8 [113]-[115]. Its topology can be thought as made of a pair of PFC circuits (i.e. D_{1u}, T_1, D_{2l} and D_{2u}, T_2, D_{1l}), each of them controlling the waveform of the current when entering into the middle point of the respective leg. F.i., during the positive half-period of v_g, the desired current is entering in the middle point of leg 1. Then T_1 is commanded to shape sinusoidally the grid current: when it is closed the current flows through T_1 and D_{2l} while when it is open the current flows through D_1 and D_{2l}, supplying power to the load. Note that the continuous flow of current through diode D_{2l} during the positive half-period precludes any control operation from transistor T_2. During the negative half-period of v_g, the two PFC circuits exchange their role. As with the classical PFC rectifier, at the beginning of the grid period the grid current is distorted. The grid current waveform and the trajectory of the space phasor are the same as in Fig. 6.5.

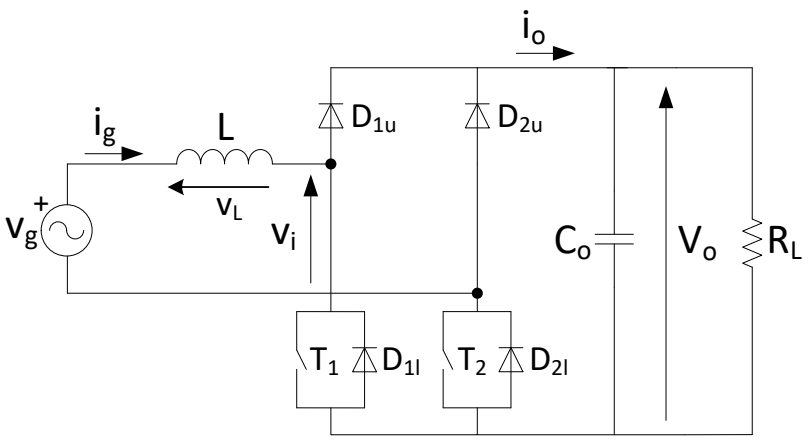


Fig. 6.8. SH PFC rectifier.

Equal results are obtained by inserting the transistors either in the upper side of the legs or in the upper and lower side of one leg, where the upper PFC circuits control the waveform of the current when leaving the middle point of the respective leg.

Compared to the classical PFC rectifier, the SH PFC rectifier has higher efficiency because only two devices are conducting (depending on the status of the switches, they are either two diodes or one diode and one transistor), while in the classical PFC rectifier three devices are conducting; the ensuing improvement in the efficiency is of few percent. As a counterpart, the SH PFC rectifier uses two transistors instead of one.

6.2.2 Three-phase

The three-phase homologue of the SH PFC rectifier, denoted with TH PFC rectifier, is drawn in Fig. 6.9 [116]-[118]. Its topology can be thought as made of three PFC circuits (i.e. D_{1u}, T_1, D_{2l} or D_{3l}, D_{2u}, T_2, D_{1l} or D_{3l}, D_{3u}, T_3, D_{1l} or D_{2l}). Since each of them controls the waveform of the currents when entering into the middle point of the respective legs, they work either in pair or alone depending on whether two grid voltages or only one is positive.

The grid voltages in a period and the currents in the first half period are traced in Fig. 6.10 (a) and (b), respectively. Explanation of the current waveforms is as follows.

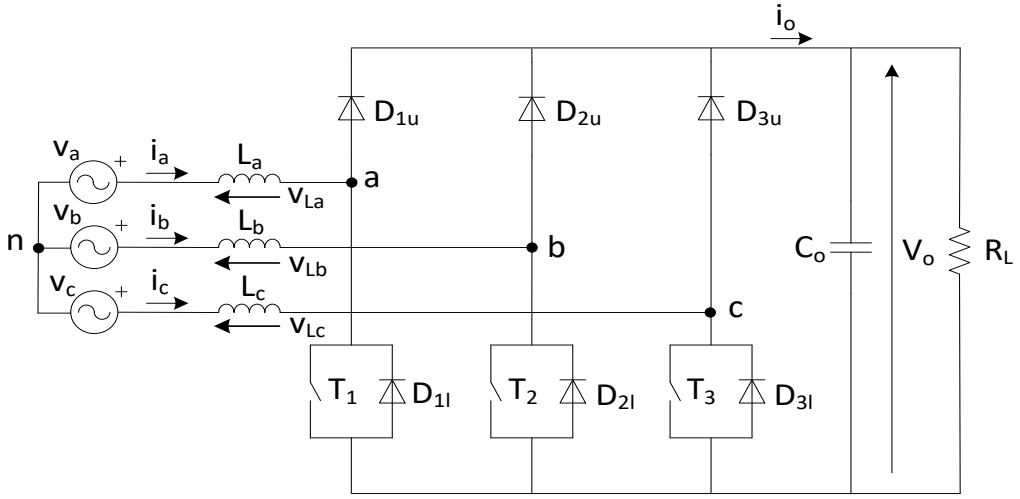


Fig.6.9 TH PFC rectifier.

Let us consider first the interval [0-π/3] where $v_a>0$, $v_b<0$ and $v_c>0$. In this interval, currents i_a and i_c enter into the middle point of the respective legs and transistors T_1 and T_3 are commanded to shape their waveforms sinusoidally. Instead, grid current i_b leaves the middle point of leg 2, flowing in diode D_{2l}. Since currents i_a and i_c are sinusoidal, the same happens for i_b.

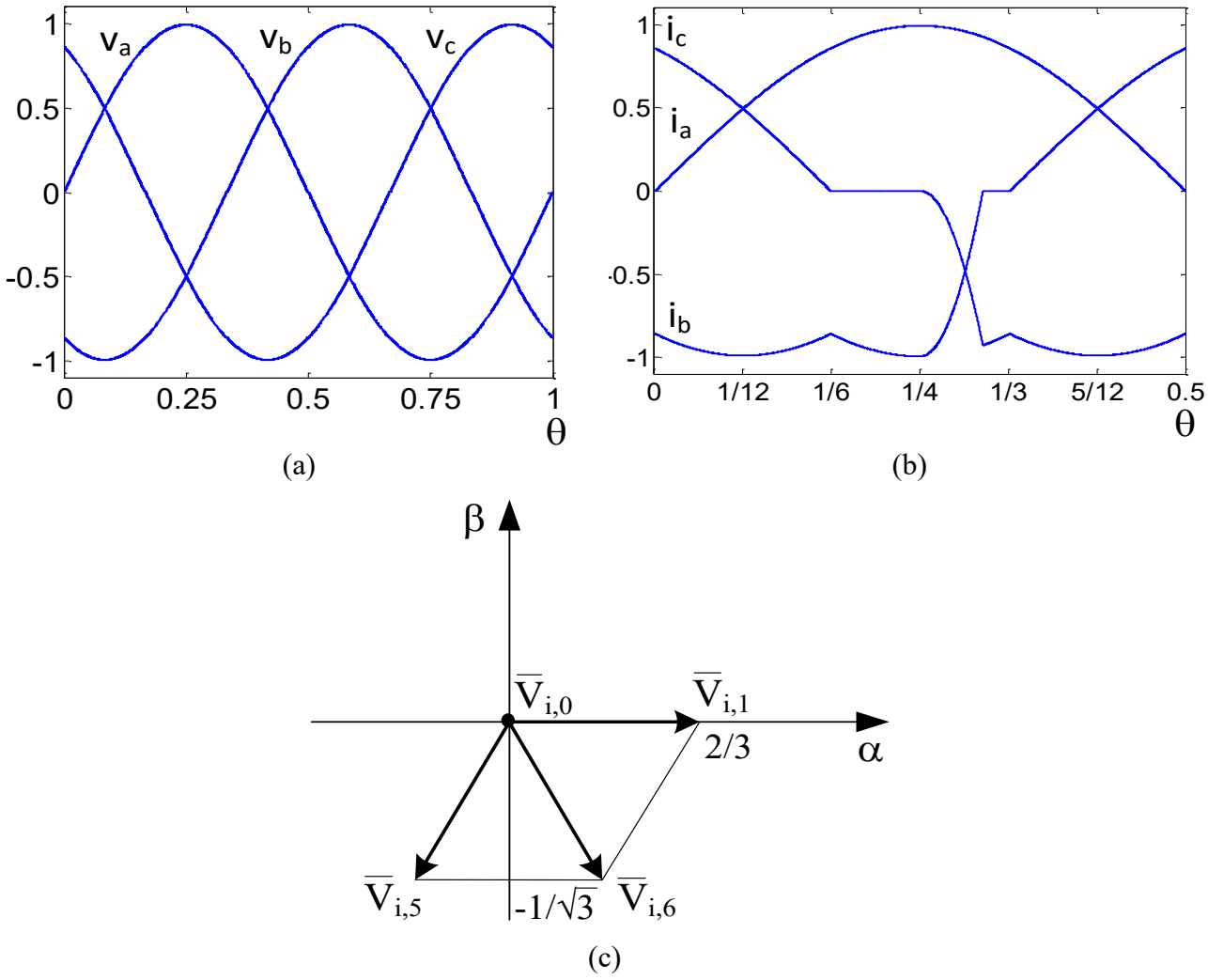


Fig.6.10. (a) Grid voltages during the period, (b) currents during half period, and (c) PFC rectifier input space vectors during the interval [0-T/6].

Differently from the SH PFC rectifier, here current i_a does not suffer from the initial distortion because voltage $\bar{v}_i$ can take a negative component even when $\bar{\imath}_g$ has a positive component. Indeed, under this current flow situation, the possible space vectors at the PFC rectifier input are as shown in Fig. 6.10 (c), where $V_{i,5}$, $V_{i,6}$, $V_{i,1}$ and $V_{i,0}$ correspond respectively to the on states of the switches: (T_1, D_{2l}, D_{3u}), (D_{1u}, D_{2l}, D_{3u}), (D_{1u}, D_{2l}, T_3) and (T_1, D_{2l}, T_3). So, the full or partial application of $V_{i,5}$ enables the achievement of a space vector $\bar{v}_i$ with negative component. However, the limited angular value between the negative semi-axis of Im and $V_{i,5}$ bounds the lagging angle δ at π/6 and, by (6.6), the maximum value of I_g at

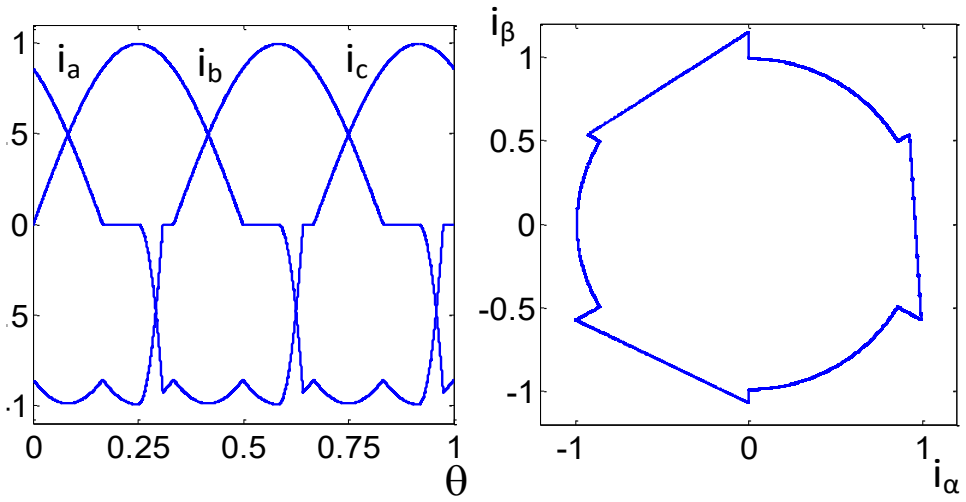
$$I_g \leq \frac{\sqrt{3}V_g}{\omega L} \tag{6.10}$$

In the interval [π/3-2π/3], it is $v_a>0$, $v_b<0$ and $v_c<0$. During this interval, transistor T_1 is commanded to shape sinusoidally the grid current i_a. The currents of the other two phases flow through diodes D_{2l} and D_{3l}; they can no more be shaped and become distorted, while their sum remains equal to the opposite of i_a. In particular, during the interval [π/3-π/2] voltage v_b is more negative than v_c and current i_c, which at π/3 is equal to zero, remains at zero because diode D_{3l} is inversely polarized by v_b, applied to its anode through diode D_{2l}. As a consequence, current i_b is the opposite of i_a.

In the interval [π/2-2π/3] voltage v_c becomes more negative than v_b, pushing diode D_{3l} to become on. Then, current i_b is forced to zero whilst current i_c drops to $-i_a$. Because of the inductors L, transition of i_b to zero as well that of i_c to $-i_a$ is not instantaneous but takes a finite commutation interval during

which all the three phases conduct. At the end of the commutation interval, i_b is zero, i_c is opposite to i_a and this situation prolongs up to $2\pi/3$. During the commutation time, both i_b and i_c leave the middle points of their respective legs through diodes D_{2l} and D_{3l} and the mesh made of v_b, L_b, L_c and v_c is short-circuited. Then, the commutation is forced by the two grid voltages. By writing the mesh voltage equation, finding out the time instant when i_c is equal to $-i_a$ and imposing that this instant is less than $2\pi/3$ when v_c becomes positive, it turns out that I_g must fulfill the same condition as (6.9).

The waveform of the currents over the period can be simply obtained by extending the previous analysis over the period. They are traced in Fig. 6.11 (a); the commanded transistors and the controlled grid currents during the various intervals are reported in Tab. I. The trajectory of the space vector of the grid currents is drawn in Fig. 6.11 (b). It is an arc when all the currents are sinusoidal, a radial segment when one current is zero, and nearly linear during the commutations. The results in Fig. 6.11 (a) clearly show that the TH PFC rectifier is not able to absorb currents with low distortion from the grid.



(a) (b)

Fig.6.11 (a) Grid currents and (b) space vector trajectory.

TAB. I. OPERATING TRANSISTORS AND CONTROLLED CURRENTS

0-π/3	π/3-2π/3	2π/3-π	π-4π/3	4π/3-5π/3	5π/3-2π
T_4,T_6	T_4	T_4,T_5	T_5	T_5,T_6	T_6
i_a, i_c	i_a	i_a, i_b	i_b	i_b, i_c	i_c

Another way of operating the TH PFC rectifier consists in controlling the current of the positive grid voltage with lower absolute value and the current of the negative voltage. The third is obtained as result from the other two. As an example, in the interval $[0\text{-}\pi/6]$, where $v_a>0$, $v_b<0$ and $v_c>0$, and $v_c<v_a$, the commanded transistors are T_2 and T_3. In the subsequent interval $[\pi/6\text{-}\pi/3]$, where $v_a>0$, $v_b<0$ and $v_c>0$, and $v_a<v_{ac}$, the commanded transistors are T_1 and T_2. And so on. The disadvantage of this operating way is the change of one of the two commanded transistors every $\pi/6$ instead of $\pi/3$.

Equal current shaping results are obtained by inserting the transistors in the upper side of the legs, the only difference being that the PFC circuits operate when two grid voltages are negative.

6.3 Full-controlled PFC rectifier

6.3.1 Single-phase

The circuit of the single-phase full-controlled (SF) PFC rectifier is drawn in Fig.6.12. It has the same topology as a single-phase active (or PWM) rectifier, but here the analysis is focused on its operation as a PFC rectifier. From this perspective, the SF PFC rectifier can be though of as a completion of the SH PFC rectifier in Fig. 6.8 with the insertion of the transistors in the upper legs. Such an insertion makes it possible the application of an input voltage with sign opposite to the current on account of the capability of this topology of handling a bidirectional power flow, thus enhancing the performance of the SH PFC rectifier.

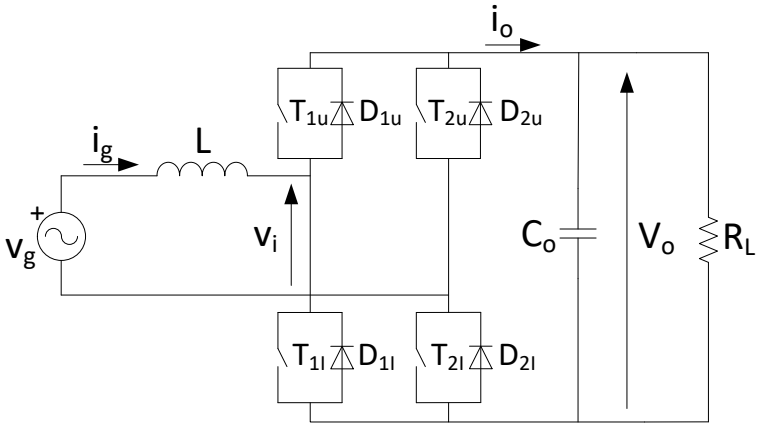


Fig.6.12. SF PFC rectifier.

Let us consider as an example the positive half-period of v_g. As shown in the Half-controlled PFC rectifiers, the PFC circuit D_{1u}, T_{1l}, D_{1l} leaves the current i_g distorted in the interval [0-δ]. Now, switching on T_{2u} while T_{1l} is conducting allows for the application of a negative input voltage v_i, thus eliminating the current distortion. For the remaining part of the half-period, the PFC circuit D_{1u}, T_{1l}, D_{1l} alone shapes the current sinusoidally. A dual operating mode occurs during the negative half-period of v_g, with the PFC circuit D_{2u}, T_{2l}, D_{2l} that resorts to T_{1u} in the interval [π+δ] to eliminate the current distortion. As a result, the SF PFC rectifier makes current absorbed by the grid sinusoidal all along the period.

The SF PFC rectifier has the inconvenience that, if implemented in a commercial pack, the transistors have an equal size while the transistors of the SF PFC rectifier have a different current solicitation. To overcome this inconvenience, it is useful to look at the SF PFC rectifier as a combination of two SH PFC rectifiers, one with the transistors in the lower legs as in Fig. 6.8 and the other one with the transistors in the upper legs; in turn, each PFC rectifier is made of two PFC circuits. Then, the operation of the SF PFC rectifier can be cycled among the four PFC circuits every quarter of period, thus balancing the current solicitation of the transistors. Specifically, in the first quarter of period, operation is as explained above: PFC circuit D_{1u}, T_{1l}, D_{1l} shapes the current sinusoidally, with the help of T_{2u} in the interval [0-δ]. In the second quarter of period, instead, PFC circuit D_{2i}, T_{2u}, D_{2u} only operates all along the interval. A dual operating mode occurs during the successive third and fourth quarters of period. By this operation, the transistors are equally solicited, with the exception of the transistors T_{2u} and T_{1u} for interval δ.

Compared to the active rectifier, where the pairs of transistors T_{1u}-T_{2l} and T_{1i}-T_{2u} are switched on and off simultaneously all along the grid period (in case of bipolar PWM control), the SF PFC rectifier requires switching of the transistors for a quarter of period under cycled operation and switching of the pair T_{1u}-T_{2u} only for interval δ. Then, the switching losses in the transistors are much less.

Compared to the SH PFC rectifier, the SF PFC rectifier utilizes two more transistors. As a return, it absorbs a fully undistorted current from the grid, needs transistors with nearly half current ratings under cycled operation, and offers the possibility to redirect the power flow, if requested.

6.3.2 Three-phase

The three-phase counterpart of the SF PFC rectifier, denoted with TF PFC rectifier, is drawn in Fig.6.13. Like the single-phase counterpart, the TF PFC rectifier has the same topology as a three-phase PWM rectifier, but here the analysis is focused on its operation as a PFC rectifier. From this perspective, the TF PFC rectifier can be thought as a combination of two TH PFC rectifiers, one with the transistors in the lower legs as in Fig. 6.9 and the other one with the transistors in the upper legs. The lower-leg PFC circuits are D_{1u}, T_{1i}, D_{1i}; D_{2u}, T_{2i}, D_{2i}; and D_{3u}, T_{3i}, D_{3i} whilst the upper ones are D_{1i}, T_{1u}, D_{1u}; D_{2i}, T_{2u}, D_{2u}; and D_{3i}, T_{3u}, D_{3u}.

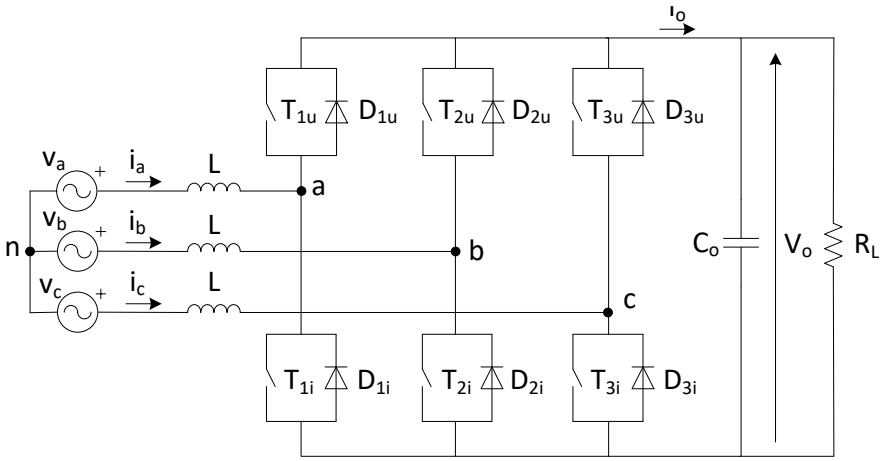


Fig. 6.13. TF PFC rectifier.

This topology makes it possible to shape the currents sinusoidally also when two grid voltages are negative. Indeed, the TH PFC circuit, with the switches inserted in the inferior side, shapes the currents sinusoidally when two grid voltages are positive whilst the TH PFC, with the switches in the upper sides, do it when the grid voltages are negative. Since shaping of two currents forces shaping of the other one, only two PFC circuits operates simultaneously and the pair changes each $\pi/3$.

As an example, in the interval $[0\text{-}\pi/3]$ $v_a>0$, $v_b<0$ and $v_c>0$, and the lower-leg PFC circuits D_{1u}, T_{1i}, D_{1i} and D_{3u}, T_{3i}, D_{3i} operate. During the interval $[\pi/3\text{-}2\pi/3]$ $v_a>0$, $v_b<0$ and $v_c<0$, the upper-leg PFC circuits D_{2i}, T_{2u}, D_{2u} and D_{3i}, T_{3u}, D_{3u} operate. And so on.

Compared to the active rectifier, where all the six transistors of the legs are switched on and off alternatively along the period, in the TF PFC rectifier only two transistors are switched simultaneously, thus reducing the switching losses of the converter substantially. This advantage is maintained even when the active rectifier uses the bus clamped modulation and limits to four the transistors that are switched on and off alternatively.

6.4 BB switch PFC rectifier

In this paragraph, the graphic symbol used for the bidirectional and bipolar (BB) switches is drawn in Fig. 6.14. Note that the circuital scheme of the BB switch is one of the possible implementations.

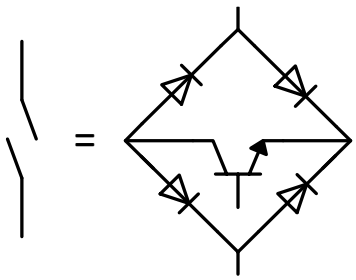


Fig. 6.14. Graphic symbol of the BB switch.

6.4.1 Single-phase

The circuit of the bidirectional and bipolar switch (SBB) PFC rectifier is drawn in Fig.6.15 [120],[121]. The BB switch is inserted between the input terminals of the diode rectifier and it is commanded to shape sinusoidally the grid current in both half-period: when it is closed, the current flows only through it, while when it is open the current flows through D_{1u} and D_{2l} during positive half-period and through D_{1l} and D_{2u} during the negative half-period. As with the classical PFC rectifier, at the beginning of the grid period the grid current is distorted. The grid current waveform and the trajectory of the space vector are the same as in Fig. 6.5.

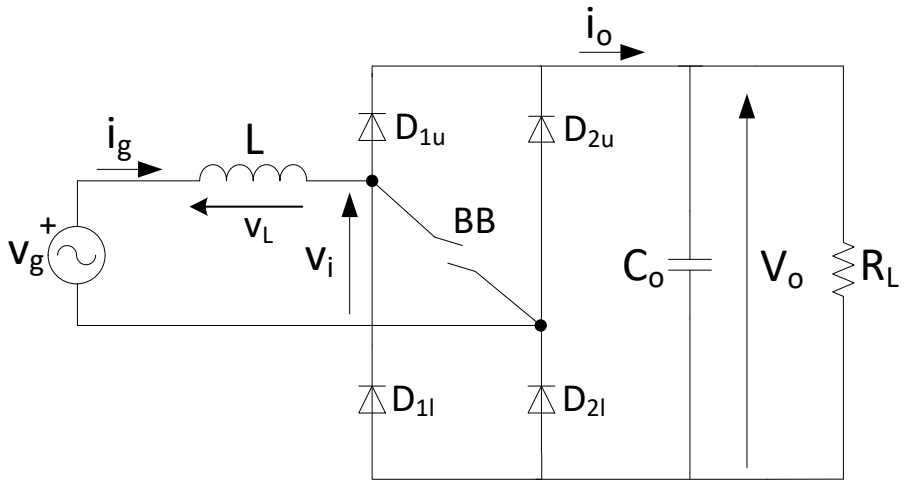


Fig.6.15. SBB PFC rectifier.

Compared to the classical PFC rectifier, the SBB PFC rectifier has slightly higher efficiency because when the BB switch is open only two diodes are conducting, while in the classical PFC rectifier three diodes are conducting. When BB switch is closed the conductive devices are the same. The improvement of the efficiency is of few percent. Instead, compared to the SH PFC rectifier, the SBB PFC has lower efficiency because when the commanded switches are closed in the SH PFC rectifier only one diode is conducting, while in the SBB PFC rectifier two diodes are conducting.

6.4.2 Three-phase

The circuit of the TBB PFC rectifier, known as Vienna rectifier, is drawn in Fig.6.16 [122]. Its schematic is composed of a diode rectifier and three BB switches connected between the points a,b,c of the legs and the common point m. The TBB PFC rectifier can be thought as a combination of two TH PFC rectifiers because the BB switches perform the same operation of the two switches connected to the upper or lower side in the TH PFC rectifier.

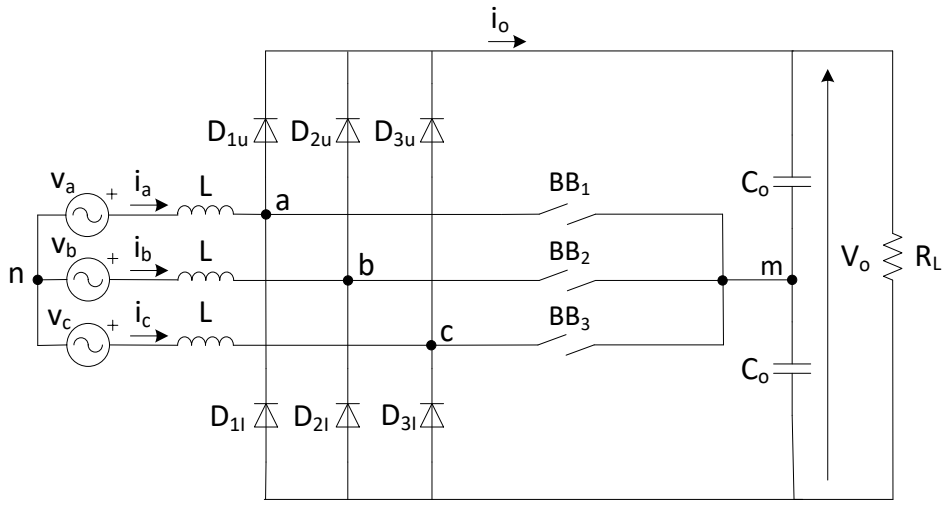


Fig.6.17 Vienna rectifier

The commutation of the switches is not executed following the same reasoning applied in the half-controlled topology because, due to the structure of the circuit, commutating the two switches where the current is entering into the middle point of leg or the two switches connected to the leg where the current is outgoing, shaping the grid currents is not possible for the entire period. For example, during the interval [0-π/3] $v_a>0$, $v_b<0$ and $v_c>0$, the switches BB_1 and BB_3 are commutated and the current i_a and i_c are not shaped until the conditions (6.11) and (6.12) are not satisfied. Then, to shape the grid currents for the entire period, a different commutation of switches is required.

$$v_a + L\frac{di_a}{dt} + v_b + L\frac{di_b}{dt} > \frac{V_o}{2} \tag{6.11}$$

$$v_c + L\frac{di_c}{dt} + v_b + L\frac{di_b}{dt} > \frac{V_o}{2} \tag{6.12}$$

Let us consider the interval [0-π/6] when $v_a>0$, $v_b<0$ and $v_c>0$ with $v_a<v_c$. The switches commutated are BB_1 and BB_2 and the conditions to satisfy, for shaping the grid currents during the entire interval, are:

$$v_a + L\frac{di_a}{dt} - v_b - L\frac{di_b}{dt} > 0 \qquad BB_1 \text{ and } BB_2 \text{ closed} \tag{6.13}$$

$$v_a + L\frac{di_a}{dt} - v_b - L\frac{di_b}{dt} > v_o \qquad BB_1 \text{ and } BB_2 \text{ open} \tag{6.14}$$

$$-v_b - L\frac{di_b}{dt} + v_c + L\frac{di_c}{dt} > v_o \qquad BB_1 \text{ and } BB_2 \text{ open} \tag{6.15}$$

Let us consider the interval [π/6-π/3] when $v_a>0$, $v_b<0$ and $v_c>0$ with $v_c>v_a$. The switches commutated are BB_2 and BB_3 because commutating BB_1, instead of BB_3, the condition (6.15) is not satisfied for the entire interval. Therefore, the pair of switches to commutate are changed every π/6 and are: the switch whose phase has a sign different from the others two and the switch whose absolute value of the phase voltage is lower than other of the same sign. For example, during the interval [π/3-π/2] when $v_a>0$, $v_b<0$, $v_c<0$ and $|v_b|>|v_c|$ BB_1 and BB_3 are commutated while, during the interval [π/2-4π/6] when $v_a>0$, $v_b<0$, $v_c<0$ and $|v_b|<|v_c|$ BB_1 and BB_2 are commutated. As in the TF PFC rectifier, during each interval only two switches are commutated to get the three grid currents sinusoidal for the entire period.

The main differences of the TBB PFC rectifier compared to the TF PFC rectifier are:

- Its circuit allows only the unidirectional power flow, unlike the TF PFC rectifier, whose circuit, changing the switches commutation, allows the bidirectional power flow.
- Switching losses are lower because the voltage on the switches is half. Considering the losses of the semiconductors and the auxiliary control circuits the reduction of total losses can reach 20%.

- Thanks to its circuit, a short circuit of the dc-link, due to a faulty control of the switches, is not possible.
- It requires an accurate control of the voltage at the common point m.
- It is a three level converter, unlike the TF PFC rectifier, which it is a two level converter. Three level converters have lower current ripple than two level converters. Therefore, the required inductances are smaller, reducing the total volume of the converter.

6.5 Simulation and experimental results

In order to realize a prototype of SST, one of the PFC circuits presented in the previous paragraphs is adopted to realize the AC-DC conversion stage of the port that must be connected to the grid. For simplicity of realization the topology selected is the classical PFC rectifier. The implementation is realized at full power in the simulation and at reduced power in the experimental setup.

6.5.1 Classical PFC rectifier – simulation results

The specifications of the project are listed in Tab. 2.

TAB. II. PARAMETERS OF THE CLASSICAL PFC CIRCUIT

Parameter	Value
$V_{in,rms}$	220 V
$V_{in\_min,rms}$	207 V
$V_{in\_max,rms}$	253 V
V_{out}	370 V
$V_{out,min}$	350 V
$V_{out,max}$	390 V
P_{out}	1000 W
f_{sw}	8 kHz
η	0.92
PF	0.99
I_{ripple}	10%
V_{ripple}	6%

- Currents calculation

$$I_{out,max} = \frac{P_{out}}{V_{out}} = 2.7\ A$$

$$I_{in,max,rms} = \frac{P_{out}}{\eta V_{i,min,rms} PF} = 5.3\ A$$

$$I_{in,max,peak} = \sqrt{2} I_{in,max,rms} = 7.5\ A$$

$I_{in,max,avg} = \frac{2}{\pi} I_{in,max,peak} = 4.77\ A$

- Input capacitor calculation

This capacitor is inserted after the diode bridge as shown in Fig. 6.18. It is not shown in Fig. 6.3 because it is not essential for the operation of the circuit. However in practice it is often used to filter the noises produced by PFC.

$I_{ripple} = 10\% I_{in,max,peak} = 0.75\ A$

$V_{in,min,peak} = \sqrt{2} V_{in,min,rms} = 292.7\ V$

$V_{in,ripple,max} = 6\% V_{in,min,peak} = 17.56\ V$

$C_{in} = \frac{I_{ripple}}{8 f_{sw} V_{in\_ripple\_max}} = 0.667\ uF$

- Inductance calculation

$I_{L,max,peak} = I_{in,max,peak} + \frac{I_{ripple}}{2} \cong 8\ A$

$\text{D (duty cycle)} = \frac{V_{out} - V_{in,min,peak}}{V_{out}} = 0.209$

$L = \frac{V_{out} D(1-D)}{f_{sw} I_{ripple}} \cong 10\ mH$

- Output capacitor calculation

$C_{out} = \frac{2 P_{out} t_{holdup}}{{V_{out}}^2 - {V_{out,holdup}}^2} \cong 1mF$

t_{holdup} is the amount of time, measured in milliseconds, that a power supply unit can maintain output within the specified voltage range after a loss of unit power. Values from 10 to 20 ms are typically used. In this project it is set 20 ms.

$V_{out,holdup}$ is the lowest permissible output voltage of the PFC at the end of holdup time. It is set 311V.

Considering the capacitor selected, the output voltage ripple is approximated

$V_{out,ripple} = \frac{I_{out,max}}{\pi 2 f_{grid,min} C_{out}} \cong 8.6\ V$

that it is lower of the maximum ripple permissible ($f_{grid,min} = 47Hz$).

The load resistance used in the simulation is

$R_o = \frac{{V_{out}}^2}{P_{out}} = 137\ \Omega$

- PI coefficients calculation

For the calculation of the PI parameters of the current and voltage loops the bandwidth are set $f_{BWi} = 2000\ Hz$ and $f_{BWv} = 10\ Hz$, and the phase margin $m_\varphi = 70°$.The parameters used are:

$$K_i = 0.16 \qquad t_i = 0.00022 \qquad K_v = 0.05 \qquad t_i = 0.03$$

The power and control circuits implemented in the simulation are shown in Fig. 6.18.

The component used in the simulation are ideal.

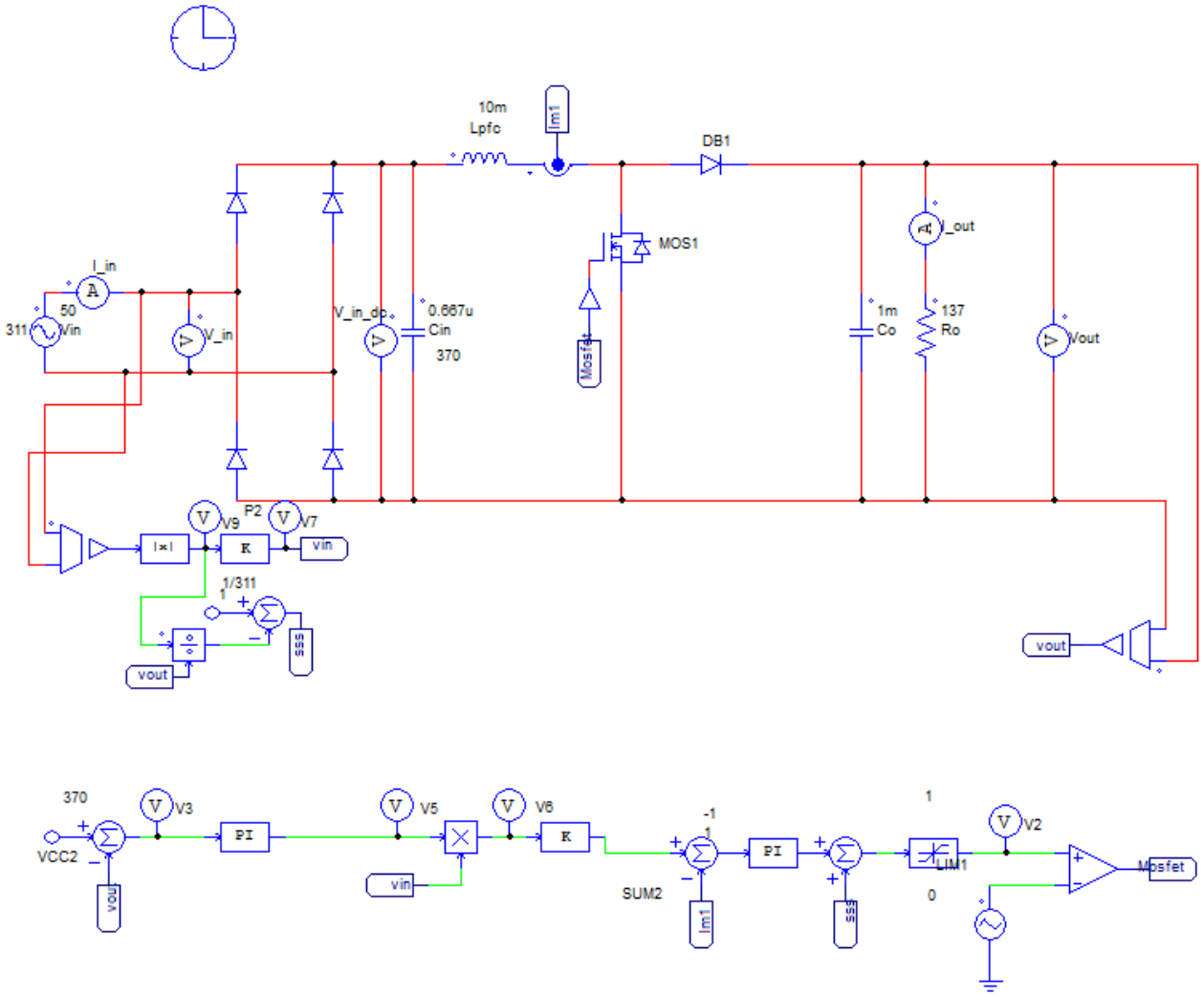
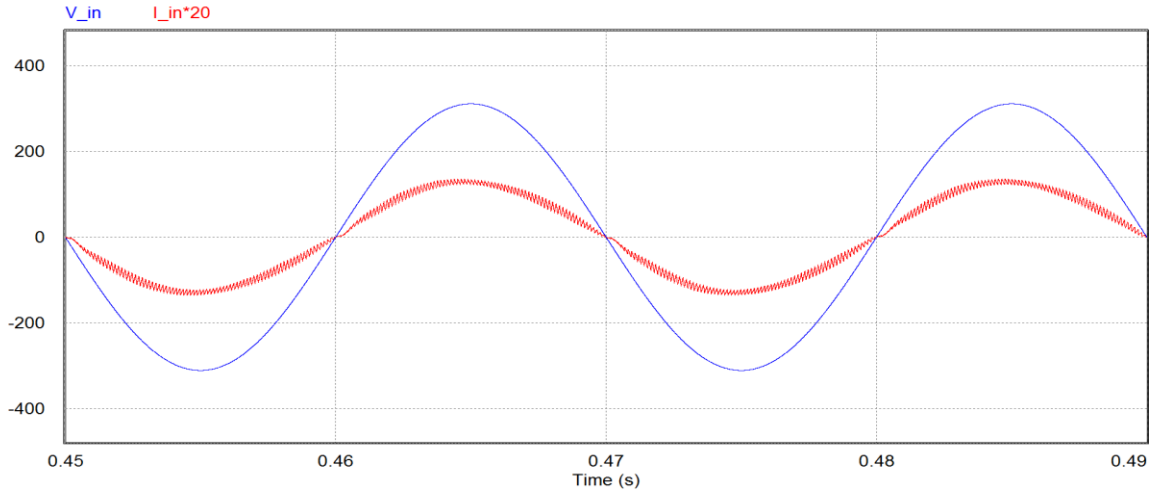
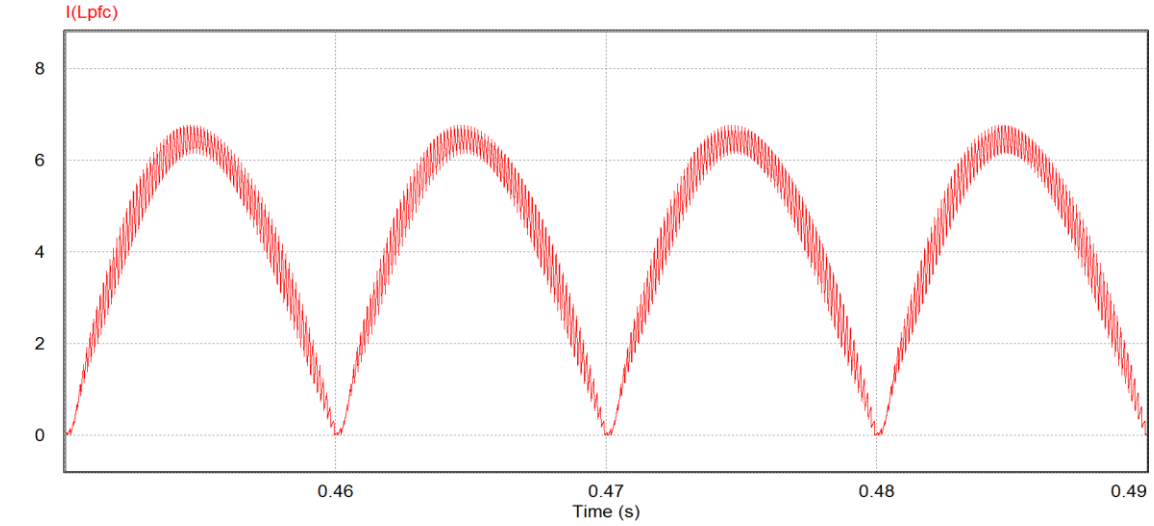


Fig.6.18 Classical boost PFC power and control circuits

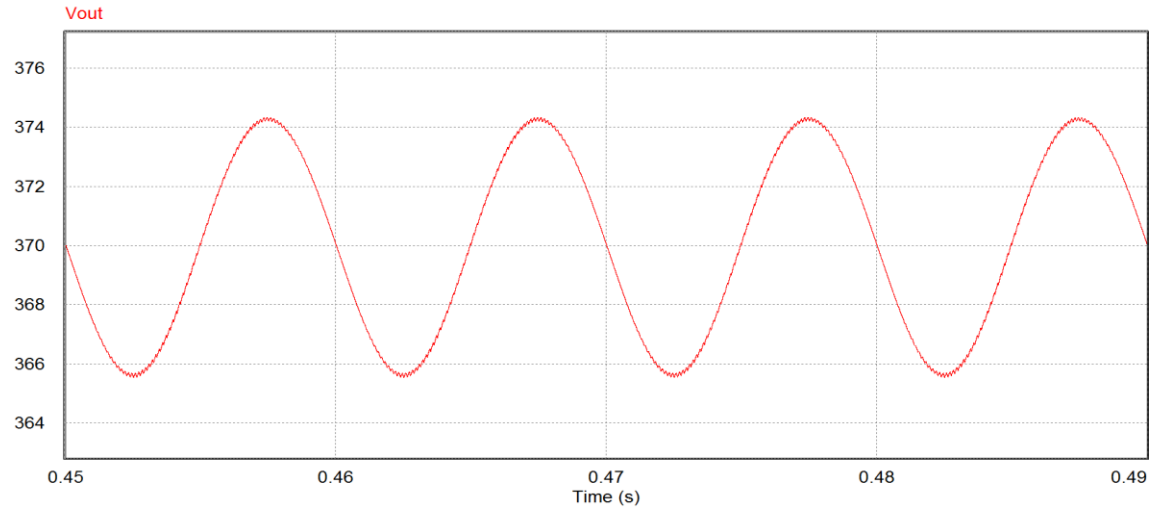
The results of the simulation are shown in Figs. 6.19 and 6.20. Fig. 6.19 (a) shows that the current is in phase with the grid voltage and the circuit operates correctly. In addition, at the start of each half period it is visible the phenomena described in the section 6.1 and represented in Fig. 6.5. In Fig 6.19 (b) it is reported the inductance current. Its ripple is 0.6 A, which is lower than the maximum ripple allowed by specifications. Fig. 6.19 (c) shows the output voltage. Its average value is 370 V and the ripple is 4.3 V, which is lower than the maximum value allowed by specifications. Fig. 6.20 shows the spectrum of the input current. It is visible that, compared to the spectrum of the input current of the diode rectifier shown in Fig. 6.2, the harmonic content is drastically reduced.



(a)



(b)



(c)

Fig.6.19 (a) Input voltage and current (multiply by 20 for better comparison of the two waveforms), (b) inductance current and (c) output voltage.

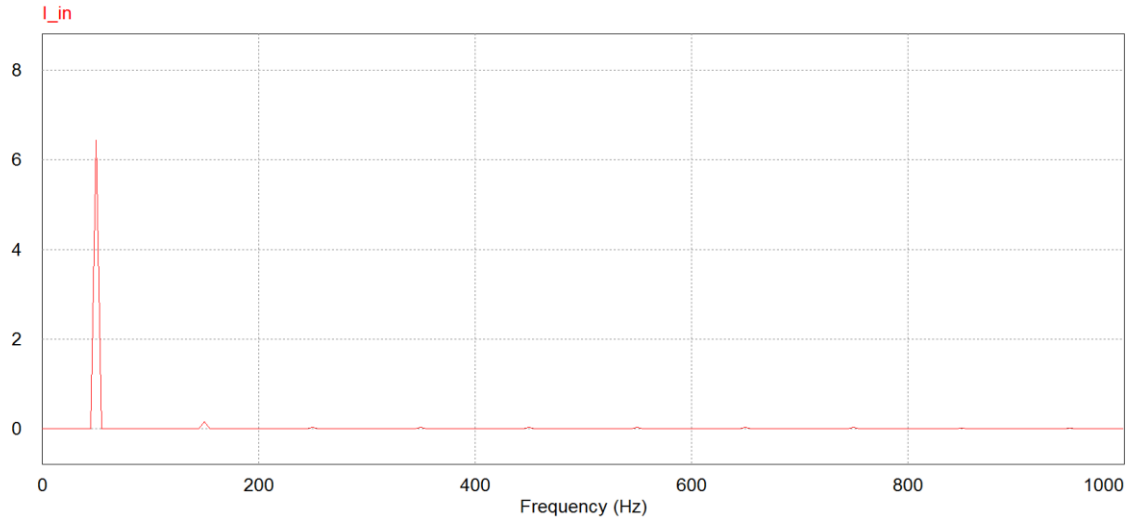


Fig. 6.20. Input current spectrum.

6.5.2 Classical PFC rectifier - experimental results

The experimental setup of the classical PFC rectifier is realized at reduced scale. The control algorithm is implemented using the Digital Signal Processor (DSP) TMS320F28335 produced by Texas Instruments. The software Code Composer Studio (CCS) v6, which is provided by Texas Instruments, is used for the programming of the processor. The current sensor LTSP 25-NP manufactured by LEM is used to measure the inductance current. The switch and diode used for the boost section of the PFC are the SiC MOSFET SCT2120AF and the SiC Schottky diode SCS220AE2. These devices have good switching performance, high breakdown voltage and high temperature limits. Voltage and current rating of MOSFET reported in the data sheet are 650 V and 29 A (continuously), while the diode has 650 V and 10 A. The MOSFET driver used is the TC1411N. The inductance used is of 3 mH. Two electrolytic capacitor of 680 uF are used at the output. A resistance of 10 Ω is used as load. The diode bridge rectifier is the KBPC606 produced by Vishay. Its maximum dc current is 6 A. The experimental setup of the designed circuit is shown in Fig. 6.21.

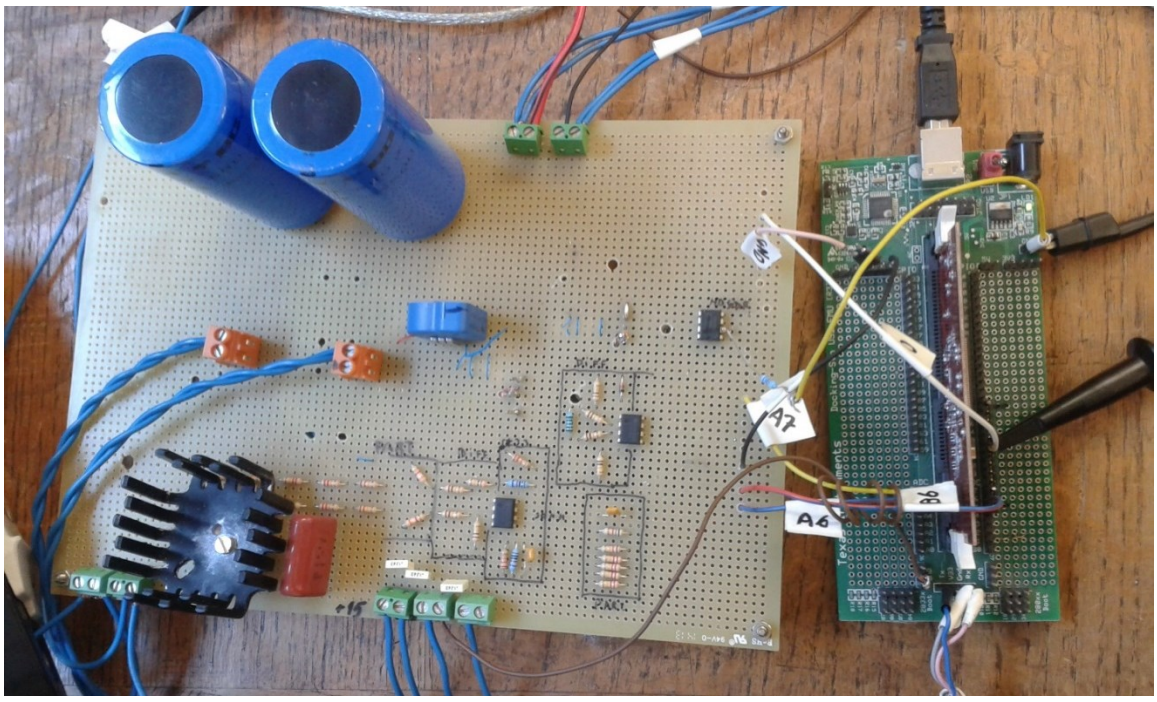
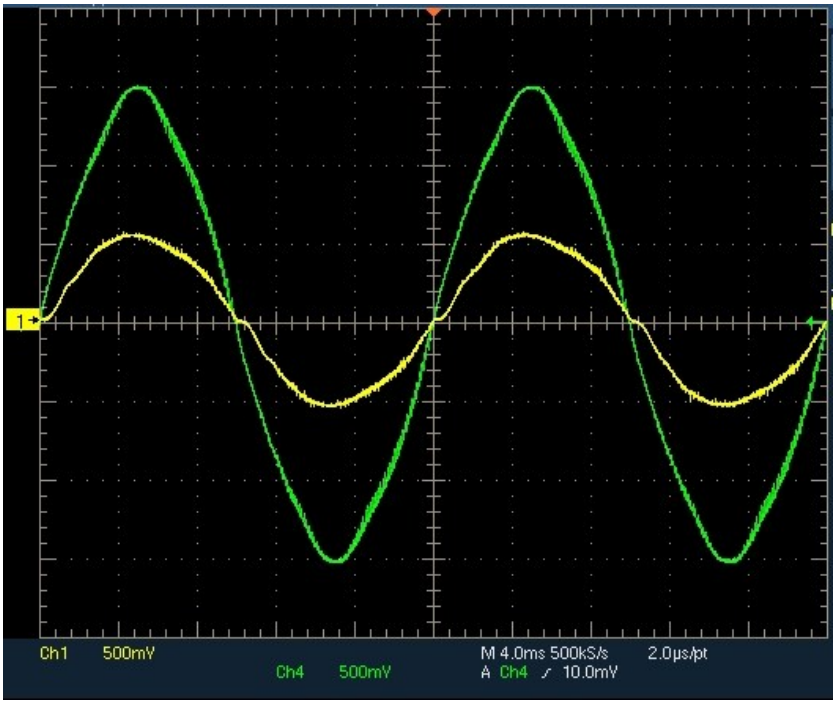
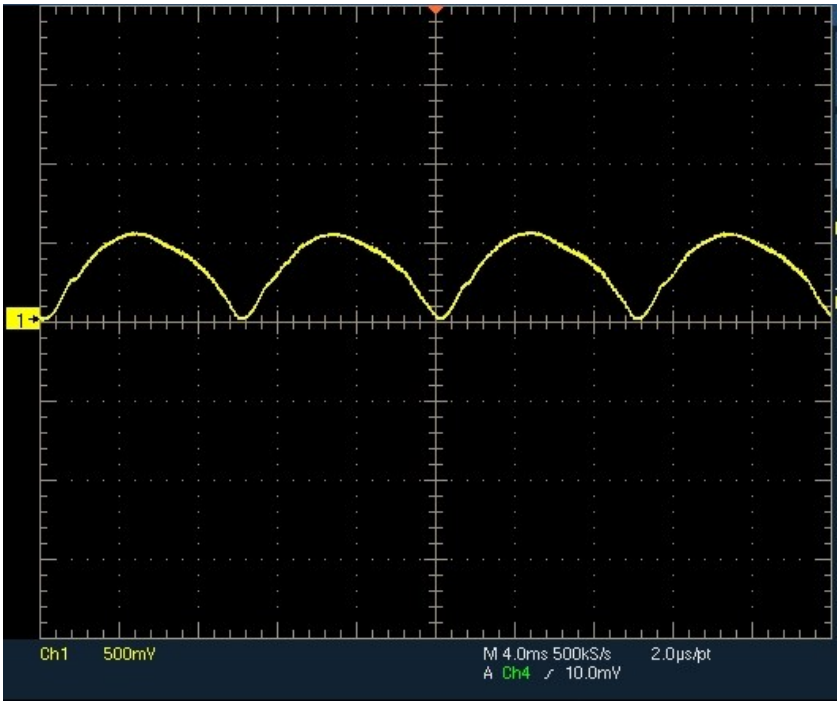


Fig. 6.21. Experimental setup of classical boost PFC with DSP interface.

The system is fed using an autotransformer and an isolation transformer. The peak of the input voltage is set at 30 V. The waveforms of quantities relevant to the functioning of the PFC are shown in Figs. 6.22 and 6.23. Fig. 6.22 (a) shows that the input voltage (green) and current (yellow) are in phase; therefore the system operates correctly. At the beginning of each period it is visible the current distortion analyzed in the previous subchapters and through simulations. The voltage waveform due to the autotransformer has a third harmonics component that is more visible when operating at low voltages, as shown in Fig. 6.22 (a). The inductor current is shown in Fig. 6.22 (b). Its peak value is 6A.

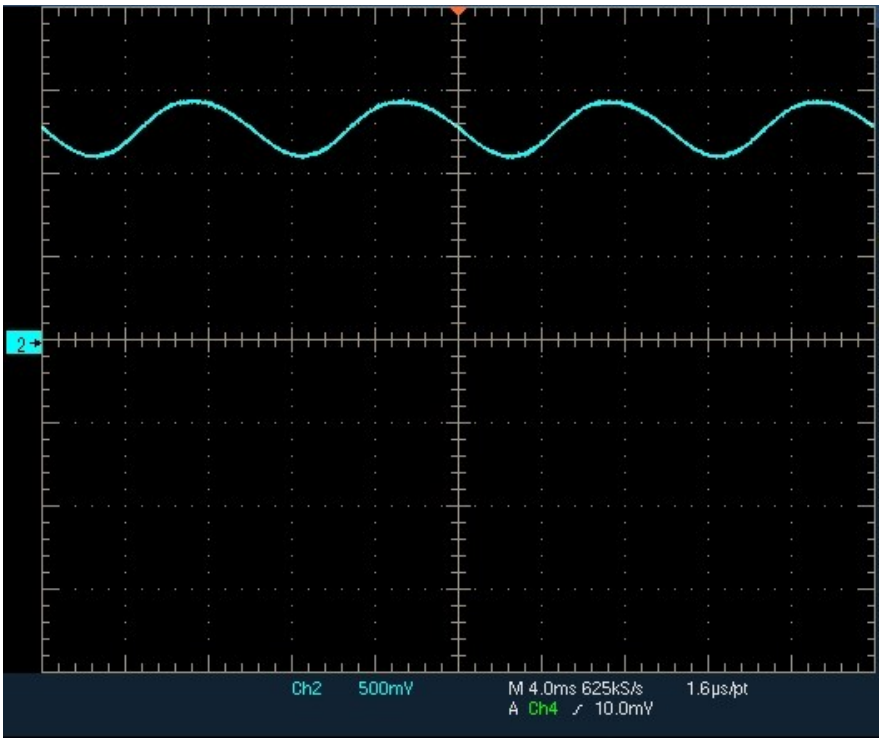


(a)



(b)

Fig.6.22 (a) Input voltage (green) and current (yellow) and (b) inductance current.



(a)

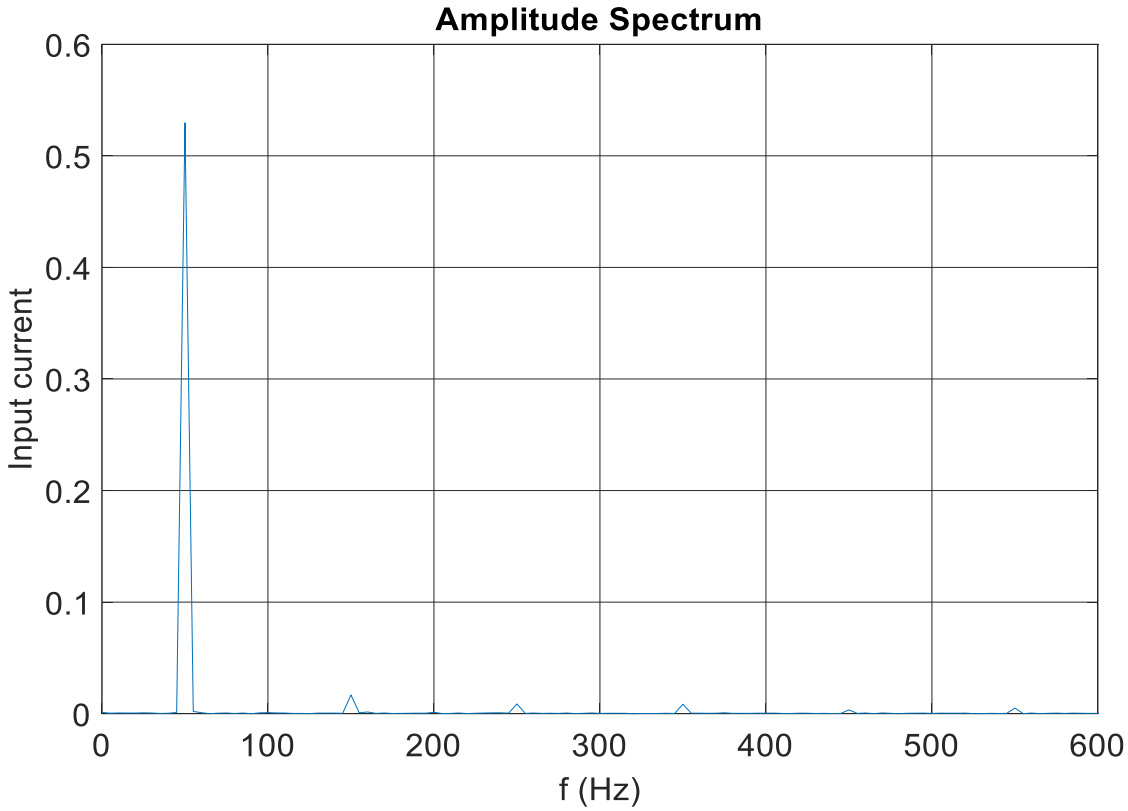
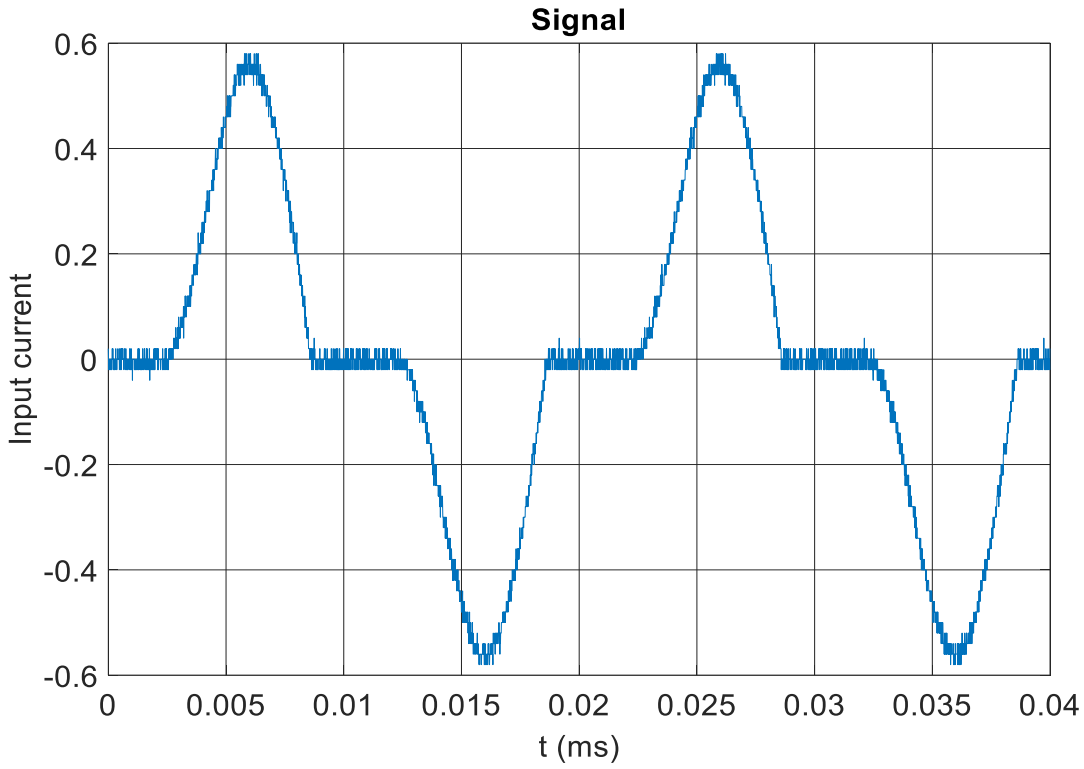


Fig.6.23 (a) output voltage and (b) input current spectrum.

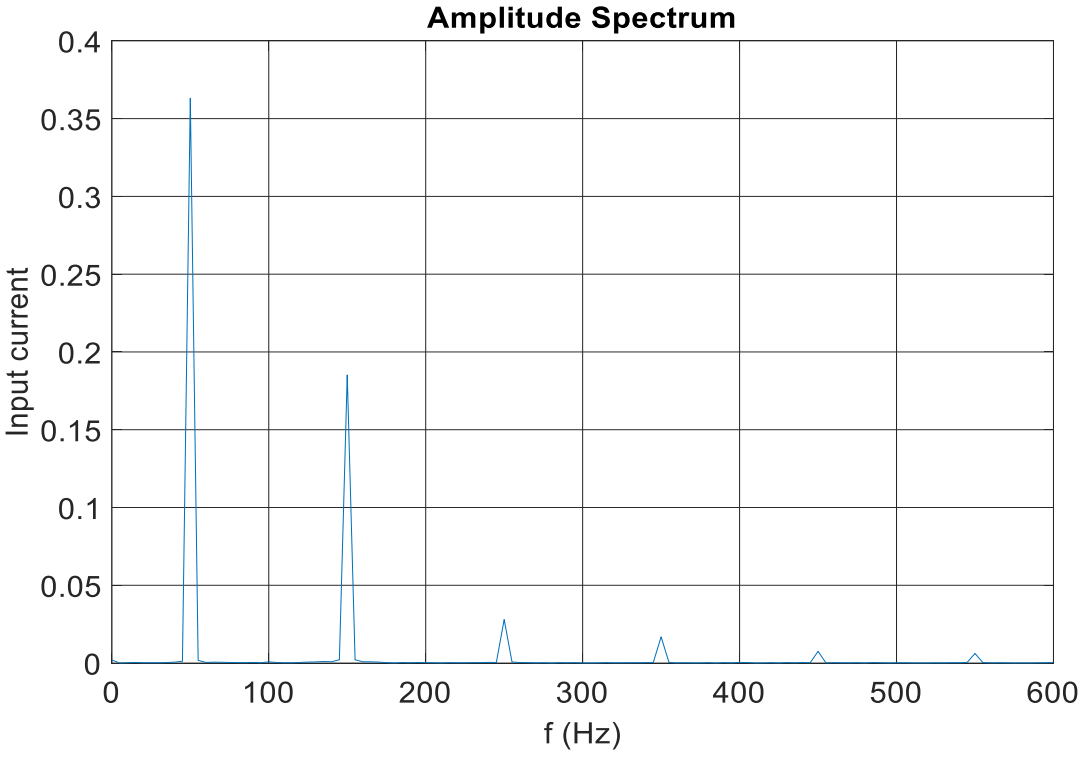
Fig. 6.23 (a) shows the output voltage. Its average value is around 27 V and the ripple is relatively high because the system is operating at low voltage with respect to the design values. Fig. 6.23 (b) shows the spectrum of the input current.

To highlight the system improvement given by PFC, another test has been performed turning off the MOSFET and maintaining the same input voltage and load resistance. In these conditions, only the

diode rectifier operates, obtaining the input current waveform and spectrum shown in Fig. 6.24. Comparing the two spectra of Fig 6.23 (b) and Fig. 6.24 (b), it is clear that the PFC drastically reduces the harmonic content of the input current.



(a)



(b)

Fig.6.24 input current waveform (a) and spectrum (b).

CHAPTER 7

Conclusions and future works

The aim of this thesis was to study and analyse the topics related to the SST technology, evaluating different architectures and selecting the most suitable for the applications of interest such as battery charger or integration of renewable energy sources. For this architecture, the conversion stages have been analysed in detail, considering both steady-state and transient functioning. The results of the analysis have been validated through simulations and experimental tests performed on the prototype. This thesis has been developed in chapters that investigate the SST technology and the different conversion stages that compose the SST.

Chapter 1 and 2 review the SST basic concepts and the SST architectures presented in literature. A deeper analysis has been performed for the singular conversion stages that compose the SST. The topologies have been discussed and compared to evaluate the best suited for the considered applications. Then, the choice is fallen on the three stages architecture. The successive chapters analyse several of the more interest solutions for different stages of the selected architecture.

Chapter 3 and 4 analyse two DC-DC conversion topologies, the SAB and DAB converter, respectively. For both topologies, a steady-state analysis is performed to find out the design characteristics needed to size the prototype. The analysis has continued studying the dynamic of the circuits and working out the transfer functions of the system, used for the calculation of the regulator parameters. In addition, the soft-switching capabilities of both topologies are investigated for the different operation modes. In chapter 4, the two topologies are compared to evaluate the differences, strengths and weaknesses of each one. The results highlight that for applications where unidirectional power flow of buck type is required, the performance of the SAB converter outdo as a whole those of the DAB converter. However, the SAB converter suffers from the shortcoming of being unable to deliver high load currents at high output voltages while, opposed to it, the DAB converter is able to operate also in this region. This is a consequence of the larger operating interval at high output voltages where the SAB converter operates in the discontinuous current mode. Moreover, the SAB operates as a voltage generator while the DAB operates as a current generator. Consequently, the selection of the best topology is a function of its capabilities and of the application requirements, in terms of voltage and current specifications. The simulations and the experimental results confirm this statement: as discussed in chapter 4, using the two topologies in the same application, the DAB converter results not suitable because its characteristics are only partially exploited so that it works in worse conditions than the SAB converter at the same transferred power, managing higher peaks of current. These considerations are dealt with more details in chapter 4 where, on their basis, the specifications of the DAB converter used for the simulations have been adjusted to find a reasonable operative condition. The mathematical analysis and the proposed control strategy have been validated through simulations while the correct operation of the two converters have been checked through experimental tests performed on a small scale prototype.

Chapter 5 deals with an isolated three-ports DC-DC converter (TPC). It has been analysed applying the results achieved from the study of the SAB and DAB converters to a topology composed of two active ports and a passive port. The TPC power capabilities and control characteristics are investigated for different operation modes and working situations. Starting from the SAB and DAB results, a short analysis of the TPC dynamic have been addressed. After that, an example of application has been studied mathematically and several computer simulations and tests on the prototype have been executed to validate the obtained results. The considered working situations are i) power delivery by both the active ports to the load though the passive port, and ii) active port #1 transferring more power than the required to the output port so that the active port #2 absorbs the power in surplus to regulate the output voltage. The correct operation in the two working situations have been tested in both FDCM and MDCM. The results about the power capabilities of the TPC obtained from the simulation and the experimental activity validate those obtained analytically. Indeed, analysis of the obtained current waveforms confirm that using the proposed control strategy, the two active ports behave as two independent SAB converters so that the equations developed to express the average current and the transferred power of the SAB converter can be used also for the TPC, thus simplifying its analysis. Finally, the efficiency of the TPC has been assessed performing experimental tests at different power levels finding that working at higher power level fully exploits the converter reaching efficiencies around 90%.

Chapter 6 analyses the operation and the features of different AC-DC conversion stages suitable for the SST technology. After that, a classical PFC rectifier has been studied though simulations and then a prototype have been realized, designed to operate as input stage of the SAB, DAB and TPC prototypes described in the previous chapters. Also in this case the experimental results validate the results obtained by the mathematical analysis.

Most of the activity performed during the three years project has been focused on the design and control characteristics of the DC-DC conversion stage of a SST. However, there are still significant aspects for further research on this technology. Among the more relevant possible future works, some are listed below.

- High frequency transformer: due to the focus of the thesis on the converter architecture, the attention on the design of the magnetic components have been limited. Then, many improvements and a deeper study can be done on the design of the high frequency transformer and inductances.
- Control techniques: the developed control strategies are based on the phase shift control. In literature there are many others control techniques that can be implemented and compared. In addiction, more complex dynamic analysis can be done to work out a more detailed model of the system.
- DC-DC converter: in addition to the DC-DC SAB and DAB converters, in literature much attention is addressed to the resonant converters. A comparison between the resonant and no resonant converters can be done for different operating conditions, such as CCM and DCM, considering the achievable efficiencies and power density.

Appendix A

High frequency transformer

In this appendix, the data plate and the measurement results of the high frequency transformer are reported.

Tab. I. High frequency transformer data plate

Parameter	Value	Unit
Nominal power	9.4	kVA
Frequency	10	kHz
Isolation/thermic class	F/F	-
Voltage winding 1	400	V
Current winding 1	23.5	A
Voltage winding 2	70	V
Current winding 2	20	A
Voltage winding 3	400	V
Current winding 3	20	A
Turn ratio	5.71	-

The measurements of the leakage inductance and winding resistance is executed by means of a RLC meter connected to the terminals of a winding keeping another winding open and the third shorted. The measurement given by the instrument corresponds to the sum of the winding resistances and leakage inductances of the winding connected to the RLC meter and of the shorted winding. In the table some of the several obtained results are reported.

Tab. II. High frequency transformer measurement results

Measurements conditions			Resistance	Inductance
Winding 1	Winding 2	Winding 3		
Connected	Open	Shorted	R13 = 0.1 Ω	L13 = 14.9 uH
Shorted	Open	Connected	R31 = 0.1 Ω	L31 = 14.6 uH
Shorted	Connected	Open	R21 = 0.066 Ω	L21 = 1.55 uH
Open	Connected	Shorted	R23 = 0.063 Ω	L23 = 2.2 uH

From the measurement results, under the hypothesis of neglecting the effects of the magnetizing inductance and resistance, the leakage inductances of the windings are about L1 = 3÷4 uH , L2 = 1.4÷1.8 uH and L3 = 11 uH. These values are not very accurate because of the assumed hypothesis and the small values of the leakage inductances compared to the inductances of the cables connecting the instrument and the transformer; however, for the purpose of the experimentation, an higher accuracy is not required.

List of pubblications

G. Buja, M. Bertoluzzo and C. Fontana, “Reactive power compensation capabilities of V2G-enabled electric vehicles,” *in IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9447-9459, Dec. 2017.
doi: 10.1109/TPEL.2017.2658686

C. Fontana, G. Buja, M. Bertoluzzo, K. Kumar, and Q. Wang, " Power and control characteristics of an isolated three-port DC-DC converter under DCM operations," Industrial Electronics Society, IECON 2016 - 42st Annual Conference of the IEEE, Florence, 2016, pp. 4211-4216.
doi: 10.1109/IECON.2016.7794126

F. Bignucolo, M. Bertoluzzo and C. Fontana, "Applications of the solid state transformer concept in the electrical power system," 2015 AEIT International Annual Conference (AEIT), Naples, 2015, pp. 1-6.
doi: 10.1109/AEIT.2015.7415235

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doi: 10.1109/OPTIM.2015.7427025

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