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PhD Thesis

Reliability and failure mechanisms of GaN HEMT devices suitable for high-frequency and high-power applications

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Abstract

This thesis reports the main reliability results and failure mechanisms analysis on Gallium Nitride High Electron Mobility Transistors (GaN-HEMTs) obtained during the three years of PhD activity. The activity has been focused *(i)* on the main reliability issues of GaN HEMTs for both high frequency applications, like telecommunication or satellite applications, and high power applications, like high-power switching, *(ii)* on the failure analysis study of the critical device degradation under high electric-field bias conditions, *(iii)* and on the deep analysis of few parasitic effects that influence the static and dynamic behaviour of this technology. The work has followed the ending of the European project KorriGaN and few research collaborations with European research centers and private companies, exploiting the possibility of understanding what critical issues are actually considered the main threat of each specific application, with the opportunity of using the acquired knowledge on the other GaN transistor's operating fields.

The first part of the thesis reports all the activity performed inside the last task of the reliability sub-project of the European project **KorriGaN** (Key ORganisation for Research on Integrated circuit in GaN technology), called *Task-Force* project. The purpose was to define the most critical working conditions over the last set of devices developed with the knowledge acquired along the project, and to study the failure mechanisms that reduce the main performances on short and long time period, on devices with different substrate quality. OFF-state reliability tests have shown the improved robustness of the technology with critical failure voltages beyond 100V, much better than older devices developed during the previous batches of KorriGaN project, underlining the great influence of a good device processing which can overcome poor quality of the epitaxial or the substrate layers. Looking at the possible dominant failure mechanisms in on-state conditions, and the related degradation accelerating factors of this robust technology, further analysis have highlighted a failure mechanism accelerated by hot-electron effects in the on-state medium-term reliability, with a negligible effect of the temperature. This

result is one of the first reported study where the hot electrons clearly accelerate the performance degradation of GaN-HEMT devices.

Similar reliability activities have been performed within the research collaboration with the *European Space Agency*. In particular, the work has been accomplished both with the activity performed inside the Padova microelectronic laboratories and with 5 cumulative months of placement at the *ESA-ESTEC* research center in the Netherlands. The studies on a quite stable technology of GaN-HEMT devices suitable for space applications have highlighted a good stability of the main static and RF performances with temperature. From the storage and the reliability analysis, the following results have been observed: good thermal stability of all the main parameters up to a quite critical temperature ($T = 350°C$), beyond which diode degradation happens even during the first hours of test; optimal robustness capabilities above 100V of drain voltage during short-term tests at ambient temperature and at higher temperatures; stable behaviour of the space-designed devices even during high junction-temperature long-term DC stress.

Following previous activities carried out on older devices of KorriGaN project, the next part of the thesis describes a deep analysis on the off-state reliability of GaN devices. Many efforts have been spent to better understand the failure mechanisms involved on the critical gate degradation of previous technologies of AlGaN/GaN HEMTs, due to some open questions that literature has still not completely explained. Despite the common acceptance of the last years on the *"critical voltage"* definition, some different results have been obtained testing the gate reverse-bias behaviour of GaN HEMTs, suggesting a failure mechanism correlated with the initial defectivity of the device under test. Further analysis with fixed negative gate bias have shown the same failure mechanism even below the estimated *critical voltage*. Failure analysis tools, guided by the electroluminescence emission images (EL), have been used for a deeper investigation on the physical evolution of the damage, following few failure analysis studies reported in the literature. Results have allowed to verify the presence of pre-existent defects and only sometimes to identify the appearance of stress-induced defects, highlighting the big difficulty and sometimes the impossibility to locate material cracks with

nanometer-scale size on the semiconductor, at least at the early stages of the device degradation.

On the last part of the thesis, some deep investigations on parasitic effects have been reported, with a special focus on the *kink effect* and on the *current collapse effect*. These activities have been performed inside the "Preliminary deep levels characterization in materials and test structures" work-package of the European project **MANGA** (Manufacturable GaN). Studying devices coming from old technologies, it has been possible to correlate the presence of the kink effect with a parasitic EL increase of the emission spectrum in the range of the yellow-red band, even correlated with a yellow broad-band peak founded during cathodoluminescence measurements (CL). These results well support a previous work that assumes the channel electrons interaction with two parasitic levels inside the GaN energy-gap as the origin of the kink effect. Studying AlGaN/GaN devices with different composition and doping of the barrier and the buffer layer respectively, it has been possible to correlate the presence of iron doping in the GaN buffer layer with an increase of the current collapse effect at the high electric-field quiescent points, identifying the activation energy of the trap responsible of this dynamic degradation. Furthermore, the combined use of Secondary Ion Mass Spectroscopy measurements (SIMS) and numerical simulations have allowed to provide a better physical demonstration of the experimental trend, confirming the measured results obtained on both the current collapse measurements and the trap activation-energy analysis.

Sommario

Questa tesi riassume i principali risultati ottenuti nello studio dell'affidabilità e dei principali meccanismi di guasto nei transistor ad alta mobilità basati su Nitruro di Gallio (GaN-HEMT). L'attività di ricerca dei tre anni di dottorato è stata incentrata *(i)* sulle principali problematiche affidabilistiche degli HEMT su GaN adatti sia alle applicazioni ad alta frequenza, come il campo delle telecomunicazioni o satellitare, sia alle applicazioni ad alta potenza, come il campo degli switch per alta potenza, *(ii)* sull'analisi fisica del degrado causato dall'applicazione di alti campi elettrici, *(iii)* e sull'analisi approfondita di alcuni effetti parassiti che influenzano le caratteristiche statiche e dinamiche di tale tecnologia. Il lavoro ha seguito le ultime fasi del progetto europeo KorriGaN e alcune collaborazioni con centri di ricerca europei e aziende private, integrando la possibilità di capire quali possano essere le problematiche attualmente considerate più critiche in ogni specifica applicazione degli HEMT su GaN, con l'opportunità di trasferire le conoscenze acquisite anche all'interno degli altri campi operativi.

La prima parte della tesi riassume tutta l'attività svolta all'interno del progetto *Task-Force*, attività conclusiva del settore affidabilità del progetto europeo **KorriGaN** (Key ORganisation for Research on Integrated circuit in GaN technology). Scopo del progetto era individuare le condizioni di funzionamento più critiche nell'ultimo set di dispositivi sviluppati a partire dai risultati ottenuti durante i precedenti anni di progetto, dando particolare importanza ai meccanismi di guasto responsabili della riduzione delle principali prestazioni nel breve e nel medio periodo, e ai diversi comportamenti indotti dalle diverse qualità dei substrati utilizzati nella crescita di tali dispositivi. I test di affidabilità a canale chiuso hanno dimostrato un significativo miglioramento della robustezza rispetto ai dispositivi sviluppati nei precedenti anni di progetto, con tensioni critiche di rottura oltre i 100V. Tali risultati sono stati confermati in tutti i wafer, indipendentemente dalla qualità del substrato, sottolineando come un buon processing dei dispositivi possa completamente mascherare la scarsa qualità dell'epitassia o dei substrati utilizzati.

A canale aperto invece, l'analisi dei principali meccanismi di guasto e dei fattori di accelerazione del degrado ha mostrato un particolare meccanismo di degradazione accelerato dagli elettroni caldi (hot electrons) presenti all'interno del canale, con una trascurabile influenza della temperatura di test. Questo risultato è uno dei primi che mostra chiaramente l'influenza degli elettroni caldi nei meccanismi di degrado degli HEMT basati su Nitruro di Gallio.

Analoghi studi su affidabilità e meccanismi di guasto sono stati eseguiti all'interno dell'attività di collaborazione con l'*Agenzia Spaziale Europea*. In particolare, l'attività è stata sviluppata sia all'interno dei laboratori di microelettronica di Padova, sia presso il centro di ricerca dell'Agenzia Spaziale *ESA-ESTEC* in Olanda, per un periodo complessivo di mobilità di 5 mesi. Gli studi sono stati eseguiti su una tecnologia di dispositivi ormai abbastanza consolidata, adattata alle esigenze specifiche delle applicazioni satellitari. I risultati hanno mostrato una buona stabilità delle principali perfomance DC e RF dei dispositivi al variare delle temperatura, e una buona stabilità nei test di storage fino ai 350°C, temperatura critica alla quale i diodi di gate cominciano rapidamente a degradare. Una significativa affidabilità è stata inoltre rilevata sia nei test a breve termine, con ottima stabilità oltre i 100V di tensione di drain a temperatura ambiente e ad alte temperature, sia nei test a lungo termine, eseguiti sui dispositivi designati per l'applicazione spaziale con test ad elevate temperature di giunzione.

La successiva parte della tesi tratta un'analisi approfondita dell'affidabilità a canale chiuso dei transistor su GaN, seguendo precedenti lavori volti allo stesso scopo. Molti studi sono stati eseguiti per comprendere meglio quali siano i meccanismi di guasto coinvolti nella degradazione del gate delle precedenti tecnologie di GaN-HEMT, a causa di alcune questioni ancora irrisolte sulle quali la letteratura non ha ancora dato una completa chiarificazione. Nonostante la definizione di *"critical voltage"* (*tensione critica*) ormai comunemente accettata, alcuni test sul comportamento del gate in polarizzazione inversa hanno evidenziato risultanti contrastanti, suggerendo un diverso meccanismo di guasto correlato alla difettosità iniziale del campione. Altre analisi in polarizzazione costante hanno mostrato lo stesso meccanismo di guasto a tensioni di gate ben al di sotto della *tensione critica*.

In seguito, su alcuni campioni sono state eseguite approfondite indagini di guasto per meglio comprendere l'evoluzione fisica del meccanismo di rottura, seguendo alcuni studi recentemente riportati in letteratura. Guidati dalle misure di elettroluminescenza (EL) precedentemente ottenute, tali analisi hanno permesso di verificare la presenza di difetti pre-esistenti e solo in certi casi di identificare la comparsa di alcuni difetti indotti dallo stress, evidenziando l'enorme difficoltà e talvolta l'impossibilità di localizzare dei difetti con dimensioni di scala nanometrica nei diversi strati di semiconduttore (cracks), almeno durante le prime fasi di degrado del campione.

L'ultima parte della tesi riporta alcune indagini approfondite su specifici effetti parassiti presenti negli HEMT su GaN, in particolar modo analizzando l'*effetto kink* e il *collasso di corrente* (current collapse). Questi studi sono stati svolti all'interno del progetto europeo **MANGA** (Manufacturable GaN), nel settore dedicato all'indagine dei livelli energetici responsabili degli effetti parassiti. Studiando alcuni dispositivi appartenenti a tecnologie meno recenti, è stato possibile correlare la presenza dell'effetto kink con un aumento inusuale dello spettro di elettro-luminescenza nel range della banda rosso-gialla, a sua volta correlato con un largo picco di emissione nel giallo rilevato durante misure di catodo-luminescenza negli stessi dispositivi. Tali studi confermano un precedente lavoro in cui si assume che l'effeto kink sia originato dall'interazione degli elettroni nel canale con due livelli energetici parassiti presenti all'interno dell'energy gap del GaN. Studiando invece alcuni dispositivi HEMT basati sull'eterostruttura AlGaN/GaN, ma con differenti composizioni dello strato barriera e drogaggio dello strato buffer, è stato possibile correlare la concentrazione del ferro, usato come drogante all'interno del buffer, con un incremento del current collapse nei punti di polarizzazione a maggior campo elettrico, identificando poi l'energia di attivazione della trappola responsabile di tale degrado delle caratteristiche dinamiche. L'uso combinato di misure SIMS (Secondary Ion Mass Spectroscopy) e simulazioni numeriche hanno permesso di dare una dimostrazione fisica dell'effetto osservato nelle misure di laboratorio, confermando sia i risultati ottenuti in termini di collasso di corrente, sia la valutazione sperimentale dell'energia di attivazione della trappola.

List of Publications

Journal papers

- M. Meneghini, N. Ronchi, A. Stocco, G. Meneghesso, U. K. Mishra, Y. Pei, and E. Zanoni, “Investigation of Trapping and Hot-Electron Effects in GaN HEMTs by Means of a Combined Electrooptical Method”, *IEEE Transaction on Electron Devices*, vol. 58, issue 9, pp. 2996-3003, 2011;

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- A. Zanandrea, F. Rampazzo, A. Stocco, E. Zanoni, D. Bisi, F. Soci, A. Chini, P. Ivo, J. Wuerfl, and G. Meneghesso, "DC and Pulsed Characterization of GaN-based Single- and Double-Heterostructure Devices", 20th *European Heterostructure Technology meeting (HeTech 2011)*, 7-9 Nov 2011, Lille - France;

- E. Zanoni, G. Meneghesso, M. Meneghini, A. Stocco, F. Rampazzo, R. Silvestri, I. Rossetto, and N. Ronchi, "Electric-field and thermally-activated failure mechanisms of AlGaN/GaN High Electron Mobility Transistors", invited paper at 220th *ECS Meeting and Electrochemical Energy Summit*, 9-14 Oct 2011, Boston - Massachusetts;

- A. Stocco, N. Ronchi, G. Meneghesso, E. Zanoni, F. Roccaforte, and V. Raineri, "Electrical and reliability investigation of AlGaN/GaN HEMTs grown on 8° off-axis 4H-SiC", 35th *Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE 2011)*, pp. 153-154, 29 May-1 Jun 2011, Catania - Italy;

- M. Meneghini, N. Ronchi, A. Stocco, F. Rampazzo, G. Meneghesso, U. K. Mishra, Y. Pei, and E. Zanoni, "Combined electro-optical analysis of trapping effects in AlGaN/GaN HEMTs", *International Symposium on Compound Semiconductor (ISCS 2011)*, 22-26 May 2011, Berlin - Germany;

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Contents

Abstract **I**

Sommario **V**

List of Publications **IX**

Contents **XIII**

Introduction **1**

1 Gallium-Nitride HEMTs **5**

1.1 GaN: material properties 5

1.1.1 Piezoelectric properties 8

1.2 GaN High Electron Mobility Transistors 9

1.2.1 RF power amplifiers 14

1.2.2 Power-switching devices 19

1.3 Trapping effects 22

1.3.1 The *kink* effect 24

1.3.2 The *current collapse* 25

1.4 Reliability issues 29

1.4.1 Reverse bias gate degradation 30

1.4.2 Hot-electrons degradation effect 35

1.5 Outline of the thesis 37

2 Reliability evaluation of GaN HEMTs in Task-Force project **41**

2.1 Task-Force project 42

2.2 DC and dynamic performances 45
2.3 Short term reliability tests 47
2.3.1 Reverse-bias gate step-stress 48
2.3.2 Three-terminal reliability 48
2.4 Medium term reliability tests 53
2.4.1 *Hot-Electrons* induced failure mechanism 56
2.5 Conclusions and future activities 64

3 Reliability assessment of GaN HEMTs in ESA project 67

3.1 Preliminary characterization 68
3.2 Short-term reliability tests 71
3.2.1 Failure mechanisms in High-Voltage step-stress tests 79
3.3 Long-term reliability tests 87
3.3.1 High temperature storage tests 88
3.3.2 Long term DC life-tests 92
3.4 Conclusions and future activities 94

4 Gate-edge degradation in AlGaN/GaN HEMTs 99

4.1 Reverse bias gate step-stress 101
4.2 Reverse bias DC stress 104
4.2.1 Constant gate reverse-current tests 104
4.2.2 Constant gate reverse-voltage tests 106
4.3 Failure analysis 114
4.4 Conclusion and future activities 118

5 Parasitic effects in GaN HEMTs 123

5.1 Kink effect analysis 125
5.1.1 Electro-luminescence investigation 126
5.2 Current collapse effect in Fe-doped HEMTs 135
5.2.1 Dynamic measurements 136
5.2.2 SIMS measurements and numerical simulations 141
5.3 Summary and conclusions 146

6 Conclusions **149**

Bibliography **153**

Introduction

In recent years, the expansions of wireless communication market, and the gradual continuous progress of the traditional military applications, have increased the interest on the microwave transistors and on the research aimed at the development of technologies that suit the ever-increasing performances requirement. Wider bandwidth and improved speed and efficiency are required for future wireless or portable communication systems, while satellite based systems and TV broadcasting need amplifiers that can work at higher frequencies and higher power, in order to reduce the size of the antenna for the final user.

At this stage, semiconductor devices based on Silicon (Si) technology are nowadays working close to their limit or already beyond, exhibiting devices with poor efficiency and with complicated cooling systems. As a consequence, many research activities have been invested in the development of different device technologies or based on different semiconductor materials. In spite of Gallium-Arsenide (GaAs) device technology are currently the most powerful semiconductor technology for the high-power high-frequency applications, it does not seem to fulfill all the performance requirements that the actual and the future applications demand. Therefore, there is an increased interest in new wide band-gap materials and new device topologies, which can potentially suit these requirements thanks to the superior inherent material properties, including the high breakdown electric field, the high electron mobility and saturation carrier velocity, and moreover the high thermal conductivity suitable for high-power purposes.

At this point, Gallium-Nitride (GaN) technology offers higher power densities and higher operating efficiencies relative to the GaAs technology, and promises to become dominant for many commercial, space and military applications of

power devices, ranging from S-band to millimeter wavelengths. Moreover, the AlGaN/GaN heterostructure provides the basis for the current generation of the high electron mobility transistors (HEMTs), devices which show excellent properties in term of current density and output power. Due to their large polarization fields, high thermal conductivity and high saturation drift velocity, GaN-based HEMTs have great potential for high-power and high-frequency applications [1], demonstrating devices with output power density of 40 W/mm [2], power-added efficiencies higher than 53% at 10 GHz [3], and maximum operating frequency close to 100 GHz [4]. Moreover, thanks to the high band-gap and the high chemical stability, GaN HEMTs can even adapt to space applications and all harsh-environment purposes. The really high breakdown-field have further allowed the introduction of this technology in the high-power switching application [5], showing very promising results.

Despite the excellent results and the enormous progress reported in the last 15 years, GaN-based devices for high-frequency and high-power applications still have to reach their maturity. In fact, many issues limit the device performances, like dispersion effects or other parasitic effects, or reduce the device reliability limiting the long-term stability.

The trapping effects are typically responsible of the reduction of the dynamic performances, in term of maximum current or high-frequency gain, and can severely limit the device capabilities on both the high-frequency and the high-power device operations. The analysis of the transient characteristics and the knowledge on the traps position allow to validate the adopted process and to give an rapid feedback for the improvement of the growth and the processing parameters.

On the other hand, many other factors cause permanent degradations on the HEMT performances on short and long time tests, like the gate-edge degradation, thermally-induced damages, or hot electrons trap-generation mechanisms, but the lack of information concerning failure modes and mechanisms, not always compatible with other previous technologies, and the continuous evolution of the adopted processes, prevent a reliable evaluation of the device life-time by means of suitable extrapolation laws, and the correlation between the processing procedures and each

particular failure mechanism. For these reasons, current devices are not operating at the theoretical potential, but typically down rated at lower performances. Consequently, many activities are focused to improve the device robustness and to understand the accelerating factors leading to the device degradation, to provide a meaningful evaluation of the long-term reliability and to rapidly approach the current market requirements.

As a result, this thesis analyzes the trapping effects and the reliability behaviour of GaN-HEMT devices with the objective of understanding the main failure mechanisms, and the related accelerating factors, that are limiting the device performances and reducing the long-term life-time. Particular efforts have been spent on the evaluation of the off-state robustness and on a deeper understanding of the gate-degradation mechanism, following previous researches in the same topic and literature reports of the last years. On this issue, the *critical voltage* definition reported *Joh et al.* in [6] has been widely examined, obtaining interesting results that suggest different failure mechanisms involving the device defect concentration. Other more recent technologies have demonstrated improved robustness with respect to this failure mechanism, giving the possibility of further investigations on the long-term reliability of these devices, and increasing the knowledge on the accelerating degradation laws that lead the GaN-HEMT robustness, with interesting results about the hot-electron influence on the HEMT reliability. Few parasitic effects analysis conclude the work, showing meaningful correlations between the physical position of the traps and the observed transient behaviour, strongly influenced by the layer quality or by particular processing steps.

Chapter 1

Gallium-Nitride HEMTs

The work of this thesis has been focused on Gallium-Nitride based devices. Thanks to the excellent material properties of this semiconductor, it is possible to create devices with excellent capabilities from RF to high-power performances, that seem to fit the current requirement of the semiconductor device's market: current densities higher than Silicon or Gallium-Arsenide technology, high voltage level with breakdown limits nowadays in the order of thousand volts, and maximum operating frequency up to 100GHz. All these outstanding device properties come from the excellent physical and electrical properties of the semiconductor. In this chapter, it will be shown the main material properties origin of these capabilities, and the main characteristics of the device subject of this thesis. Finally, the last section will be focused on the issues that reduce device performances, in term of trapping effects and reliability concerns.

1.1 GaN: material properties

Gallium-Nitride (GaN) is a compound semiconductor on the Nitride-group, with high energy-gap and high carrier velocity saturation. The wide band-gap of the material typically reflects on higher breakdown voltages, due to the high electric-field required for band-to-band impact ionization (see table 1.2). These two properties are typically combined to extract the *Johnson's figure of merit (JM)*, an important index that gives the power and frequency limit of a material based only on the

physical properties, making Gallium-Nitride an excellent semiconductor for both high-power and high-frequency applications. Furthermore, the high energy-gap make this material less prone to radiation effects, opening the possibility for future space applications.

$$JM = \frac{E_{br} * v_{sat}}{2\pi}$$

	Si	GaAs	4H-SiC	GaN
Johnson's figure of merit	1	2.7	20	27.5

Table 1.1: *Johnson's figure of merit* of the most important semiconductors for high-frequency and high-power operations [1]. The abbreviation refers to: Silicon (Si), Gallium-Arsenide (GaAs), Silicon Carbide (4H-SiC), and Gallium Nitride (GaN).

As reported in table 1.1, this index places GaN beyond the typical semiconductors used for digital, high-power and high-frequency electronics (Silicon and Gallium-Arsenide), and quite close to Silicon-Carbide [7]. The great advantage that makes GaN a more attractive material compared to SiC consist in its ability to form the heterostructures. This ability allows the construction of the *High Electron Mobility Transistors (HEMTs)* characterized by better carrier concentration and channel mobility, whereas SiC can only be used to build Metal-Semiconductor Field-Effect Transistors (*MESFETs*) [1, 8].

Looking at the internal structure of the semiconductor, *wurtzite* is the thermo-

	Si	GaAs	InP	4H-SiC	GaN	Diamond
$E_g(eV)$	1.1	1.42	1.35	3.26	3.39	5.45
ε_r	11.8	13.1	12.5	10.0	9.0	5.5
$\mu_n(cm^2/Vs)$	1350	8500	5400	700	1200-2000	1900
$v_{sat}(10^7 cm/s)$	1.0	1.0	1.0	2.0	2.5	2.7
$E_{br}(MV/cm)$	0.3	0.4	0.5	3.0	3.3	5.6
$\theta(W/cmK)$	1.5	0.43	0.7	3.3-4.5	1.3	20

Table 1.2: Electrical properties of various materials [1].

dynamically stable crystal structure of the Gallium-Nitride. Due to this particular hexagonal lattice structure and to the difficulties in easily growing low-cost GaN bulk substrates, GaN layers are typically grown on a foreign substrate, with compatible lattice constant and thermal expansion coefficients.

Especially at the beginning of the GaN technology development, but even on more recent technologies, the substrate choice is one of the most critical issue to solve, in order to obtain good epitaxially layers with low defects concentration. As reported in table 1.3, Silicon Carbide is the best solution in term of lattice matching, thermal expansion, and typically even for the very good thermal conductivity (useful for high-power applications), but not in term of wafer cost. For this reason, different substrate approaches, like Sapphire or Silicon, offer worse epi-layer characteristics due to the higher lattice mismatch, but with a significant reduction of the substrate cost. Furthermore, with the introduction of other thin layers before GaN deposition (better explained on the next section), it could be reduced the defects propagation from the substrate to the active area by means of a gradual variation of the lattice parameters. Another substrate option comes from the hybrid substrates, which consist of a thin layer of Si or SiC supported by a thick layer of polycrystalline Silicon Carbide. The advantage of this kind of substrate is the high thermal conductivity at low-cost, typical for poly-SiC layers, with a cheaper lattice-matched thin SiC layer or with a single-crystal low-cost large diameter silicon wafer, grown on top of it [9–12].

	Lattice Constant (Å)	Lattice Mismatch (%)	Thermal Exp. Coefficient ($10^{-6} K^{-1}$)	Thermal Mismatch (%)	Thermal Conductivity (W/cmK)
GaN	3.19	0	5.6	0	1.3
Al_2O_3	4.75	15	7.5	33.9	0.5
SiC	3.08	-3.5	4.46	-20.3	5
Si (111)	5.43	17	3.59	-35.8	1.5

Table 1.3: Substrate properties useful for GaN epitaxial growth [13, 14].

1.1.1 Piezoelectric properties

The different electronegativity between Gallium and Nitrogen atoms induces a polar behaviour in each Gallium-Nitride crystal, and in general in every III-Nitride compound. In our case, each layer of GaN, or of its alloy, is characterized by a spontaneous polarization vector that strongly affects the electrical properties of any device processed on top of this layer. The higher the Aluminum content, the higher the polarization vector. As a consequence, the polar nature of the material creates different physical properties depending on the choice of the direction of the crystal growth: layers grown starting from Ga-atoms that end with a surface of N-atoms, are typically called *N-face* GaN layers; on the contrary, layers grown on the opposite direction, starting from N-atoms that end with a Ga-surface, are typically called *Ga-face* layers (the most used configuration; see figure 1.1). Layer growth and device processing are completely different depending on the upper face, including the different electrical properties that can be obtained choosing one or the other solution.

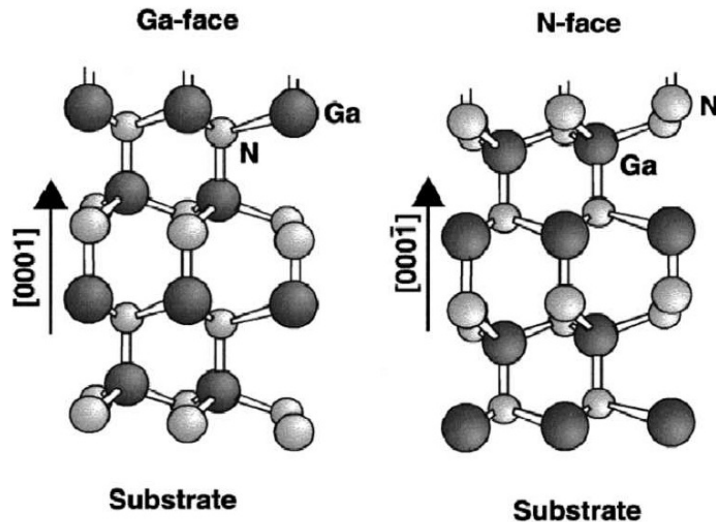


Figure 1.1: Schematic drawing of the crystal structure of wurtzite *Ga-face* and *N-face* GaN layer [15].

Furthermore, the epitaxial growth of other GaN-based layer on top of a GaN layer, induces other polarization vectors with a direction depending on the crystal strain and on the surface face (see table 1.4). On the following sections, the most

used layer structures will be shown, especially for *Ga-face* configuration, considering both the induced advantages and the critical issues coming from the polar nature of the GaN materials.

Wurtzite	AlN	GaN	InN
$a_0(A)$	3.112	3.189	3.54
$c_0(A)$	4.982	5.185	5.705
c_0/a_0	1.601	1.627	1.612
$P_{sp}(C/m^2)$	-0.081	-0.029	-0.032

Table 1.4: Lattice constant and spontaneous polarization of the main III-V compound semiconductors [16].

1.2 GaN High Electron Mobility Transistors

High Electron Mobility Transistors (HEMTs) are devices based on an heterostructure between high-energy gap materials, that allows the combination of the high carrier concentration coming from a doped-layer, with the high mobility of a channel located on a intrinsic semiconductor. In fact, the first HEMT devices were based on a AlGaAs-GaAs heterostructure with an n-doped AlGaAs layer on top, the *barrier layer*, and a GaAs intrinsic layer on the bottom, the *buffer layer*. The advantage of the heterostructure is the possibility of exploiting the high electron concentration, coming from the n-doped layer, flowing into a thin quantum-well at the heterostructure interface, typically called *two dimensional electron gas* (*2DEG*), with the higher mobility provided by the un-doped buffer layer (see figure 1.2).

The major advantage of the GaN HEMTs arises from the possibility of inducing a very high concentration 2DEG without any layer doping, but only with the epitaxial growth of an AlGaN layer on top of a GaN buffer, removing all the problems related to the intentional doping of GaN or GaN-alloys layers. The origin of this spontaneous generation of a high concentration 2DEG comes from the high polarization contributions of each single layer and of the heterostructure. In fact, as previously reported, the growth of polar layer on top of a buffer layer

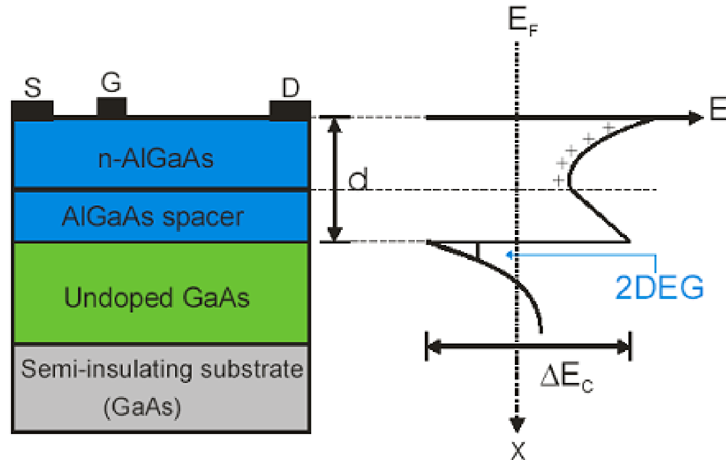


Figure 1.2: Layer structure and band diagram of a GaAs HEMT [17].

with a different crystal lattice, induces another polarization vector, the *piezoelectric polarization*, with a magnitude depending on the lattice mismatch. Depending on the choice of the buffer layer orientation (and as a consequence of the surface face), it is possible to align the two polarization contributions. Therefore, the high positive charge created at the lower interface of the barrier can automatically induce a very high-concentration electron channel just at the upper interface of the buffer. The small quantum well generated by the band bending, and the high electron concentration induced by the strong polarization vectors, create a two dimensional electron gas with high mobility (better than GaN bulk) and high carrier concentration, that can drive very high current even in high frequency conditions (see figure 1.5 (c)).

As reported in figure 1.3, not all possible layer combinations are allowed, but only one solution for *Ga-face* and one for *N-face* topology induce the electron channel with the highest carrier concentration. As a consequence, these topologies are the actual layer stacks typically used for *Ga-face* and *N-face* HEMT development: for *Ga-face*, the AlGaN barrier layer on top of the GaN buffer layer, with a tensile strain on the AlGaN that induces, with the spontaneous polarization, a two dimensional electron gas on the GaN upper interface; for *N-face*, a thin AlGaN barrier layer sandwiched between the GaN buffer layer, on the bottom, and the GaN channel layer, on top, with a tensile strain on the AlGaN layer that induces,

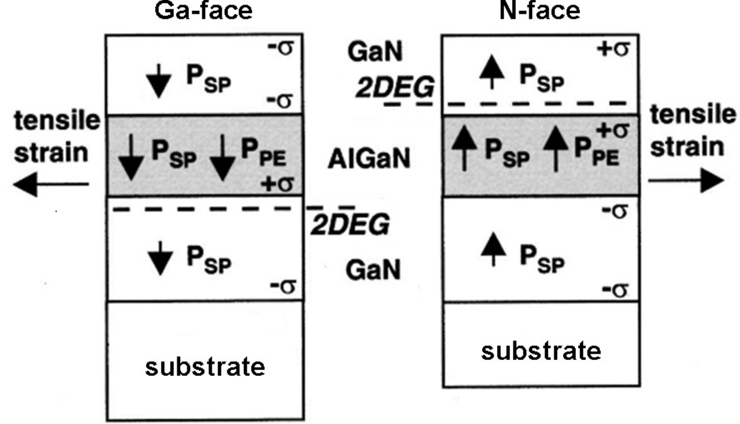


Figure 1.3: Spontaneous (P^{SP}) and piezoelectric (P^{PE}) polarization vectors and induced interface charge with Ga-face and N-face GaN topology [16].

with the spontaneous polarization, a two dimensional electron gas on the lower interface of the GaN channel layer [16]. Actually, the most used configuration is the *Ga-polar* HEMT, and all the following consideration will deal with this topology, but many studies and very interesting results are recently coming even from *N-face* structures [18].

Both polarization contributions (spontaneous (P^{sp}) and piezoelectric (P^{pz})) can be estimated considering the Aluminum content of the GaN alloy and lattice constant of both materials. *Fiorentini at al.* [20] calculates the nonlinear polarization vectors of an arbitrary nitride alloy, giving the opportunity of a better estimation of the final sheet charge induced by the epitaxially growth of these two polar layers.

$$P^{sp}_{Al_xGa_{1-x}N} = -0.090x - 0.034(1-x) + 0.019x(1-x)$$

$$P^{pz}_{AlN} = -1.808\varepsilon - 7.888\varepsilon^2$$

$$\text{with} \quad \varepsilon = [a_{sub} - a(x)]/a(x) \quad \text{and} \quad a_{Al_xGa_{1-x}N}(x) = 0.31986 - 0.00891x$$

The polarization charge (and the resulting 2DEG concentration) is strictly correlated to the spontaneous polarization of each material and to the lattice mismatch between the two layers of the heterostructure: the higher the vectors, the higher the 2DEG concentration (see figure 1.4).

Figure 1.5 shows the typical layer stack, charge distribution, and band profile of a Ga-face AlGaN/GaN heterostructure. The net charge Q_π of each layer is given

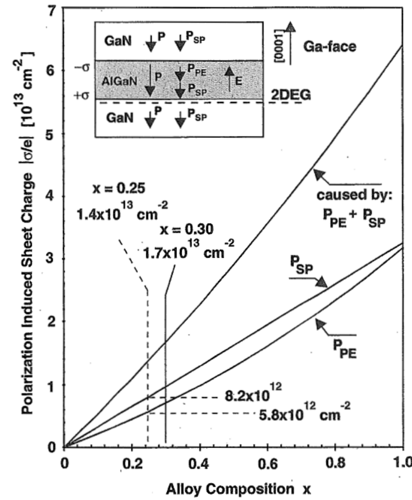


Figure 1.4: Calculated sheet charge density caused by spontaneous and piezoelectric polarization at the lower interface of a *Ga-face* GaN/AlGaN/GaN heterostructure vs. alloy composition of the barrier [15].

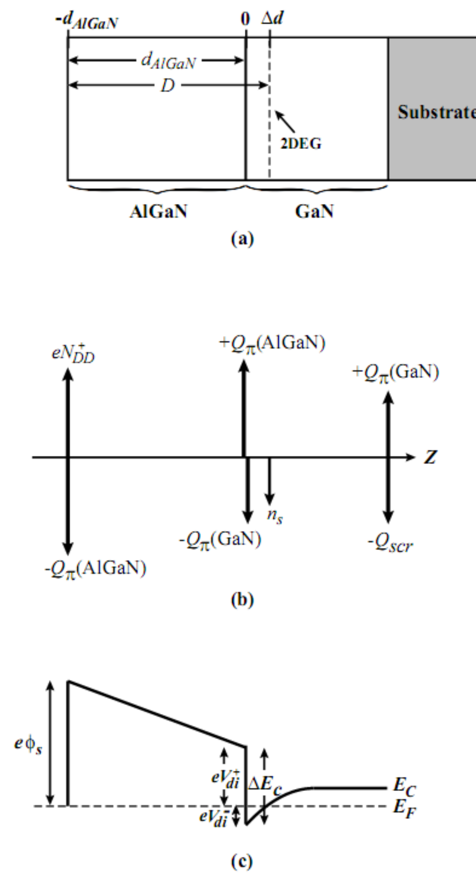


Figure 1.5: (a) Typical AlGaN/GaN heterostructure used in Ga-face HEMT technology, along with (b) the charge distribution and (c) the band diagram of the structure [19].

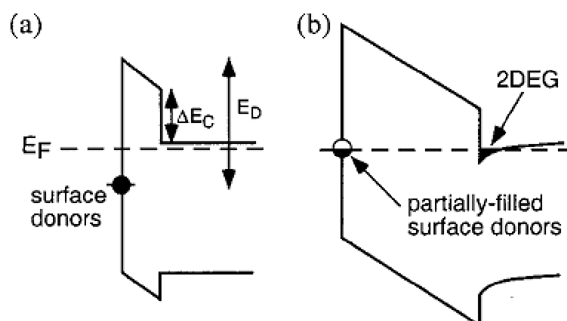


Figure 1.6: Band diagram that shows the absence of the electron channel below the critical thickness of the AlGaN layer (a), and the ionization of the surface donor level that induces the 2DEG formation after the critical thickness (b) [21].

by the sum of spontaneous and piezoelectric polarizations. As there reported, to balance the high positive charge induced on the heterostructure interface of the AlGaN layer, there must exist a distribution of electrons in the GaN layer near the interface [19]. But the origin of this negative charge is not so clear, due to the absence of any intentional doping on the AlGaN layer. The most accepted physical explanation consist in the presence of a surface donor state that can supply the negative charge to the electron gas. With this assumption, increasing the thickness of the barrier, the internal electric field remains constant (due to the fixed polarization charge) keeping the same band bending, and the energy level of the donor state gradually approaches the Fermi level. After a critical thickness, depending of the band bending and consequently on the polarization contributions, the donor state crosses the Fermi level and, as a consequence, it starts to ionize the surface traps, leading to an equal electron concentration which drifts to the heterostructure interface. As a results, the electron accumulation at the band discontinuity balances the positive charge of the empty donor states at the surface, creating the two-dimensional electron gas suitable for the carriers flowing in HEMT devices (see figure 1.6).

The presence of two external contacts connected to the heterostructure's 2DEG via a low-resistance path, gives the possibility of controlling the current flow simply applying a voltage between the two terminals. These two terminals are called drain and source. Placing a gate metal contact on top of the AlGaN layer allows to

modulate the 2DEG concentration by depleting or enhancing the charge density below the contact. In figure 1.7, it is possible to observe the classical layer stack of a *Ga-face* AlGaN/GaN HEMT structure. The substrate on the bottom, the epitaxial growth of the heterostructure in the middle, and the three contacts on top.

Typically, the contact's composition is not so simple, but it has to take into account the work function of the metal for the suitable contact type, and other issues like contact resistance (Al, Au) or thermal stability (Ti). For these reasons, contacts are typically made by a stack a different metals: for example Ti/Al/Ni/Au for the *ohmic contacts* (drain and source), annealed at high temperature to reach the optimal channel connection, and Ni/Au for the *Schottky contact* (gate).

Looking at figure 1.7, it is worth to observe the presence of other two thin nucleation layers placed at the substrate-buffer interface, and in the middle of the heterostructure. The first layer placed between the substrate and the GaN layer allows to reduce the defects propagation from the substrate to the active area, due to the different lattice characteristics [8]. The structure and the composition of this layer is one of the most critical aspects and, consequently, associated to each foundry depending on the substrate used for the GaN epitaxial-growth. The upper nucleation layer, located at the heterostructure interface, allows to reduce the residual scattering caused by the interface roughness. The introduction of about 1 nm of AlN nucleation layer allows to improve the electron confinement and to increase the channel mobility above $1000 cm^2/Vs$ [22].

Thanks to the excellent physical properties of GaN and GaN alloys, the GaN-HEMT architecture can be used both for high-frequency device implementation, e.g. RF amplifiers, and for high-power device applications, e.g. power-switching devices, with different operative targets that have to be considered during device precessing (see figure 1.8).

1.2.1 RF power amplifiers

For RF application, the GaN HEMT architecture allows to increase the theoretical high-frequency performances and the maximum operating frequency, thanks to the

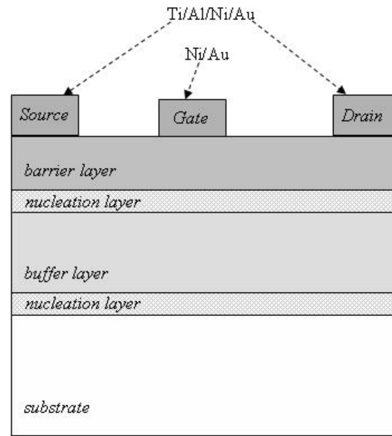


Figure 1.7: Typical layer structure of an AlGaN/GaN HEMT

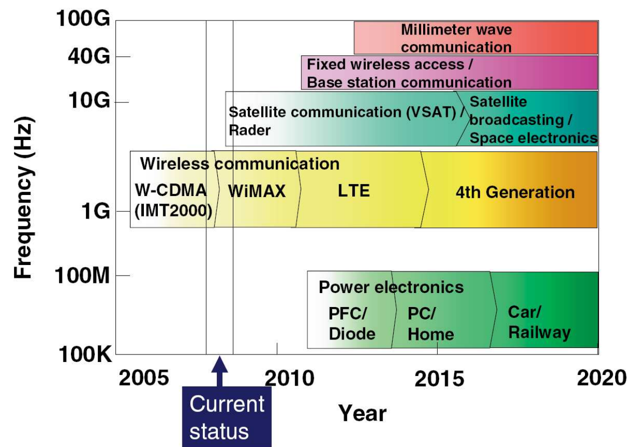


Figure 1.8: Commercialization roadmap of GaN HEMT for several frequency related applications [23].

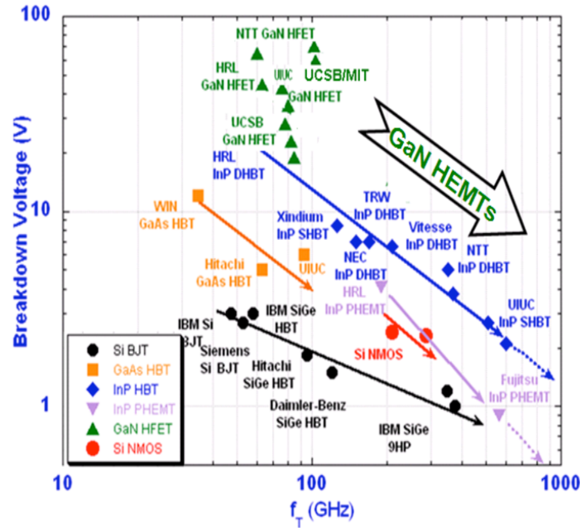


Figure 1.9: Breakdown voltage vs. cut-off frequency of the actual semiconductor technologies [25].

reduced access resistances, to the big transconductance values, and to the reduced parasitic capacitances. The high electron concentration of a channel located all along the heterostructure interface and the high velocity saturation, allow to increase the transconductance and to keep very low access resistances. The high current capabilities and the high breakdown field allow to reduce the device size, to decrease the parasitic capacitances, and to have an easier network matching. As previous shown with the *Johnson's figure of merit*, the GaN materials and the HEMT topology give a optimum alternative choice for the actual RF technologies, keeping the high-frequency operation of the GaAs devices but enabling a significant increase of the operating voltage (see figure 1.9). Looking at the *cut-off frequency* f_τ, the frequency at which the short-circuit current gain of the transistor has unit magnitude [24], it is possible to understand that high values of transconductance (g_m), high values of the saturation velocity and low gate capacitances, as previously stated, allow to reach really high cut-off frequency values.

$$f_\tau = \frac{g_m}{2\pi C_G} \equiv \frac{v_s}{2\pi L}$$

Moreover, the device's scaling will theoretically allow even higher f_τ, due to the inverse correlation with the gate length L, keeping an high aspect ratio between the gate length and the gate-to-channel distance. On the contrary, it will introduce

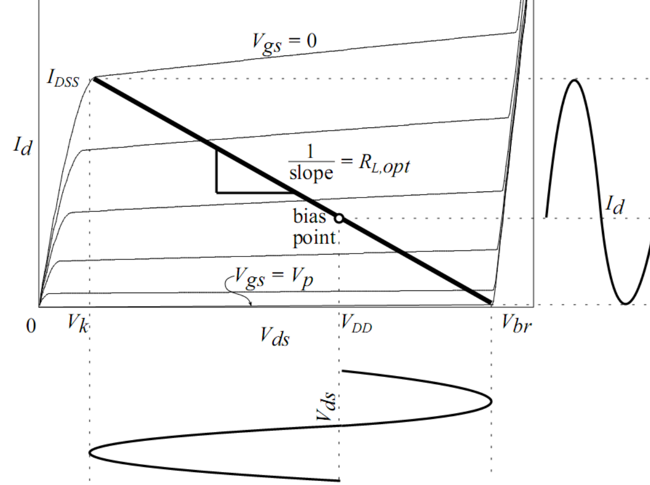


Figure 1.10: Device bias point and load-line for a class-A operation RF amplifier [19].

many other non-idealities that can reduce the intrinsic device performances, like short-channel effects or poor channel confinement. Nevertheless, to overcome these issues, a common solution (even used on the actual long-gate devices) is placing a back-barrier layer just below the channel region for better channel confinement, using a thin layer of different materials.

The typical high-frequency application of the GaN HEMT is the use as RF amplifier, in class-A operation for better linearity and bandwidth performances, or in class-AB or B operation, for higher efficiency and lower DC consumption.

In class-A, the device is biased in the middle of the IV characteristic, with an ideal load-line that goes from the pinch-off in high-voltage conditions, to the knee-voltage in high current conditions (see figure 1.10).

$$P_{out-max} = \frac{1}{2} \cdot \frac{1}{2} (V_{br} - V_{knee}) \cdot \frac{1}{2} (I_{DSS}) \equiv \frac{(V_{br} - V_{knee})^2}{8R_{L-opt}}$$

In GaN devices, increasing the maximum pinch-off voltage, and reducing the knee voltage (by reducing the on-state resistance), allow to increase the available RF output power ($P_{out-max}$). The drawback of this configuration is the high DC consumption, due to a bias point located on the high-power region. For this reason the efficiency drop down, leading to a maximum value of 50%.

$$PAE\% = \frac{P_{out} - P_{in}}{P_{DC}} \cdot 100\% = \frac{P_{out}}{P_{DC}} \cdot \left(1 - \frac{1}{G}\right) \cdot 100\%$$

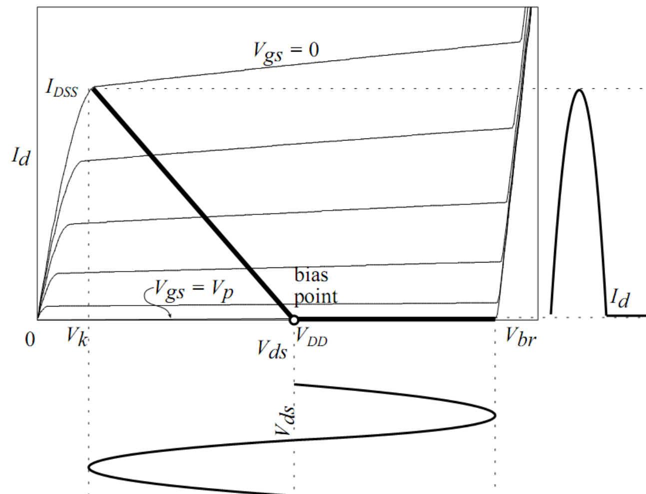


Figure 1.11: Device bias point and load-line for class-B operation RF amplifier [19].

The Power Added Efficiency (PAE) is defined as the ratio between the difference in the RF output to input power (the net output power) and the total DC power drawn from all bias supplies.

It is clear that the class-B or AB operation (see figure 1.11) allows better efficiency values, due to the theoretical zero-power consumption of the bias point. But the increase of the output efficiency comes with the reduction of the system linearity, and with the necessity of a push-pull configuration to amplify even the other phase of the input signal.

On both amplifier configurations, and especially on class-B operation, the good pinch-off characteristics and the low gate-leakage values of GaN devices allow to reduce the DC power consumption and the input power losses. Moreover, the high thermal conductivity and the general better thermal management of the GaN structures [26], allow to handle high output-power densities with an easier device cooling.

All these requirements make SiC the best substrate choice, due to the reduced heterostructures defects on the RF GaN devices, useful for the high mobility requirement in high-frequency operation, and due to the optimal thermal conductivity. Nevertheless, other lower-cost substrates, like Silicon, can be used taking into account the slightly lower performance achievement, in term of thermal management and layers quality.

RF performances of GaN devices have been widely reported on literature, with optimum performances concerning the maximum power capabilities (approximately one order of magnitude better than Ga-As technology), and comparable maximum operating frequency. The best power performances have been demonstrated by *Wu el al.*, with a 30 W/mm at 2.1 GHz [27] and 40 W/mm at 4 GHz [27] GaN-on-SiC single device. *Maekawa et al.* [28] have shown a 500 W power amplifier for L-band application, whereas *Johnson et al.* [29] and *Hoshi et al.* [30] have demonstrated important RF performance even with GaN-on-Si devices, with output power around 12 W/mm at 2.14 GHz. Increasing the operative frequency, *Shigematsu et al.* [3] have demonstrated hybrid two-chip configurations giving 340 W output power with 53% PAE in C-band (at 4.8 GHz) and 100 W output power with 53% PAE in X-band (at 9.8 GHz). At the extreme frequency, *Heying et al.* [31] have recently demonstrated a V-band (55 GHz) circuit with 1.13 W of output power (2.83 W/mm) and 23.3% of PAE. Furthemore, *Micovic et al.* [4] have presented results on W-band GaN MMICs operating at 88 GHz with 842 mW output power and 14.8% PAE, the highest output power ever reported at this frequency for any solid-state MMIC amplifier.

1.2.2 Power-switching devices

The very large critical electric fields of GaN-based devices, makes this technology attractive even for the high-power switching application. On DC-DC converter, or any other power switching circuit, there exist electronic devices which switch from an high-voltage low-current condition to a low-voltage high-current condition. Therefore, the ideal device should be a switch with zero power dissipation in both open-condition (i.e. low leakage current and good pinch-off) and closed-condition (i.e. high current with negligible voltage drop), and even during the switching events. On the real devices, this requirements reflect into very good pinch-off characteristics for a low-power bias-point in off-state, high subthreshold slope, and low on-state resistances with a low *knee voltage* to reduce the on-state power consumption. On dynamic operation, fast switching times are required.

Due to the actual breakdown voltages reported for GaN based devices, the

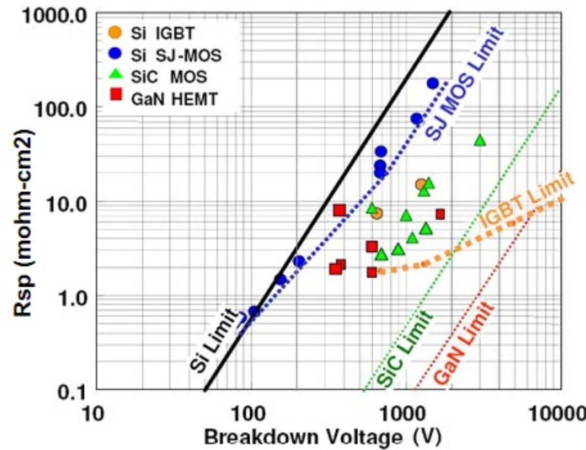
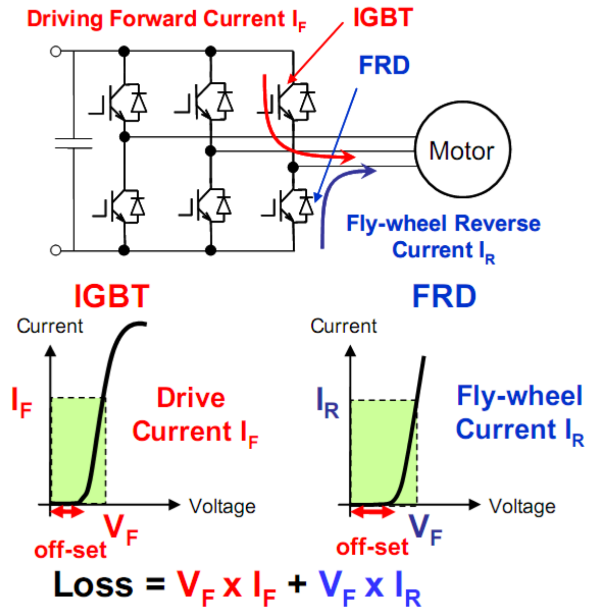


Figure 1.12: Specific ON-state resistance vs. breakdown voltage for typical high-power switching technologies based on different semiconductors; theoretical data (line) and experimental results (dots) [32].

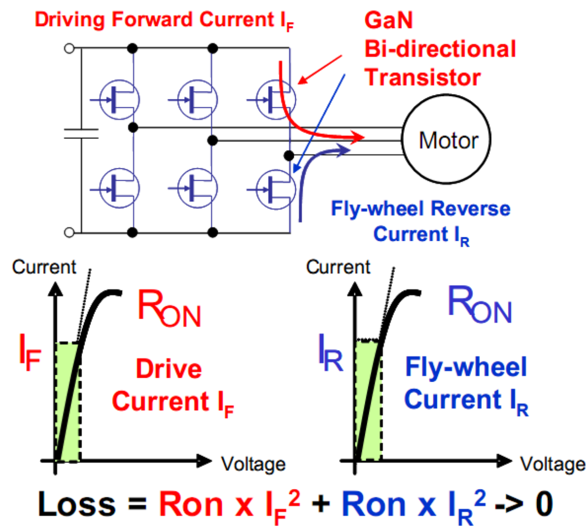
same technology, previously described for the high-frequency application, can be adapted for the application on the high-power switching. In fact, GaN HEMTs can sustain very high breakdown-voltages with low current leakages, can drive very high-currents with low voltage drops (low on-resistance) and, due to the high-frequency nature of this technology, they can work with very fast switching times, giving the possibility of increasing the operating frequency, with the advantage of shrinking all the passive components.

The typical electrical parameters used for device comparison are the breakdown-voltage limit correlated with the device on-resistance, due to the inverse co-relation between this two parameters. As reported in figure 1.12, comparing GaN technology with the other standard technologies used on power-conversion circuits, GaN shows theoretical limits quite above the standard Si technology and even beyond SiC technology. Due to the intrinsic high concentration and high mobility of the 2DEG, the on-resistance is quite low, and the switching times are faster compared to other standard FET with the same device active area. Keeping a smaller area allows to further increase the switching transients with a big reduction of the dynamic losses, as shown in figure 1.13.

On the high-power switching application, the requirements for the switching performance, in term maximum frequency or dynamic losses, are not as severe as



(a)



(b)

Figure 1.13: Forward and reverse conduction losses in inverter systems using IGBTs (a) and GaN transistors (b) [33].

for RF amplifier, making the cheaper Silicon substrates the best candidate for all high-power GaN switches. In fact, all the high-power GaN devices reported on the literature have been grown on Si substrates.

The biggest issue that still prevents GaN device market is the negative threshold voltage. Due to the spontaneous formation of the electron channel, GaN devices are depletion-mode devices, whether typical high-power devices are enhancement-mode devices, for the safety reason of avoiding any current flow at zero-bias operation. Several techniques have been developed to positively shift the threshold voltage, but all these methods do not allow vary high positive gate values due to the intrinsic nature of the Schottky gate contact [34–36].

The most interesting results come from different HEMT structures, using particular interlayer on top of the heterostructure below the gate contact, to change the threshold voltage behaviour and to enhance the positive swing of the gate terminal. Addressing this last requirement, GaN-based devices suite all the current needs of high-power switching devices, but reaching better performances compared to the other Si-based technology. *Uemoto et al.* [5] have presented a normally-off GaN transistor with 800V of breakdown voltage and $2.6m\Omega \cdot cm^2$ of on-state resistance, whereas *Huang et al.* [37] have shown a MOS-GaN switch which integrates a n-channel lateral GaN MOSFET with a Schottky diode, with 770V of blocking voltage. Moreover, *Niiyama et al.* [38] have presented a +3V threshold-voltage GaN MOSFET, with a breakdown voltage higher than 1550V and *Kanamura et al.* [39] have shown a triple cap layer with recessed-gate structure, e-mode, MIS-HEMT, with +3V of threshold voltage and 320V of OFF-state breakdown. Finally, *Chen et al.* [40] have presented a prototype of switch-mode DC-DC Boost converter with normally-off GaN-on-Si transistors with 470V breakdown voltage.

1.3 Trapping effects

Trapping effects are one of the major limiting factor of the AlGaN/GaN high electron mobility device performances, especially in the past at the early stages of GaN technology. In fact, the first processed devices showed huge reduction of

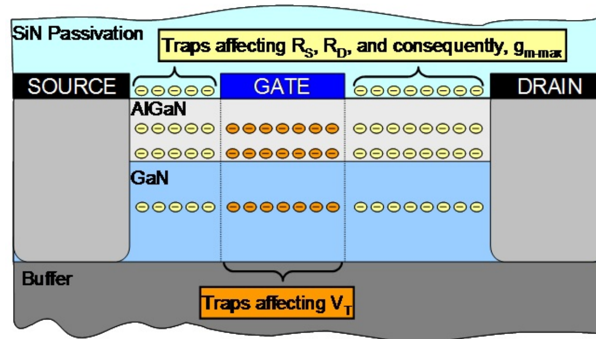


Figure 1.14: Different possible traps position inside the AlGaN/GaN HEMT layer structure.

the theoretical output power estimated with the DC data, due to the enormous reduction of the drain current from DC condition to pulsed or RF conditions [41].

The explanation of these DC-to-RF current compression can be found on the parasitic traps located in the surface or inside each layer of the HEMT heterostructure. In fact, the presence of material defects due to the growth on a lattice-mismatched substrate, or the interruption of the crystal uniformity like on the heterostructure interface, create available energy-states inside the energy-gap that can act as traps for electrons or holes. The charge trapping inside these levels origins different parasitic effects that limit the device performances both on DC and RF operation. The different position of the trap inside the HEMT structure causes different parasitic effects that can reduce the DC performances (drain current or threshold voltage), the dynamic transconductance, or the RF output power. Actually, it is not completely understood the exact correspondence between the parasitic effect and the traps position, but many paper shown consistent results correlating the parasitic effect with the traps location, as reported in figure 1.14.

In particular, the trapping effects that are mainly limiting the GaN-HEMT performances and that are focusing the attention of the research activities are the *kink effect*, a slow parasitic effect that reduces the channel current at low drain-voltages, and the *current collapse*, the common parasitic effect that reduces the RF output current and, as a consequence, the RF performances, compared to the DC current.

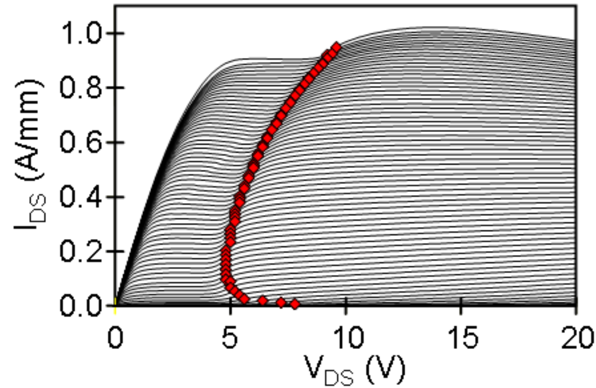


Figure 1.15: Long integration time output characteristics of a kink-affected device. Red diamonds correspond to the maximum of the output conductance (V_{kink}) [42].

1.3.1 The *kink* effect

The *kink* effect is a slow trapping effect that induces a reduction of the drain current at low drain voltages (V_{DS}). After a certain voltage not always fixed at each gate voltage, the drain current rapidly increases, the threshold voltage slightly shifts to the left, and the kink effect disappears (see figure 1.15). The enhancement of this low-V_{DS} current reduction is still not completely clear, at least due to the different trapping/detrapping behaviour reported on different device structures [42, 43]. Nevertheless, the effect seems to be correlated to slow transients caused by traps located in the GaN buffer. Concerning the parameter variations, kink effect can cause dynamic performance reduction, transconductance compression, on-resistance increase, and possibly output-conductance increase.

The physical origin of this effect seems to be the electron interaction with two GaN deep levels responsible of the kink effect, as deeply investigated on the last chapter of this thesis: at low $V_{DS}\,(< V_{kink})$, a deep acceptor state can capture channel electrons causing the right shift of the threshold voltage and the reduction of the drain current; at high $V_{DS}\,(> V_{kink})$, electron detrapping or compensation by holes can occur, causing a left threshold voltage shift and the sudden increase of the drain current. The non-monotonic dependence of the drain kink voltage (V_{kink}) at different gate voltages, suggests a impact-ionization de-trapping mechanism caused by channel hot electrons [42], feasible at this voltage level. The strong dependence with the environmental light or with the ambient temperature supports

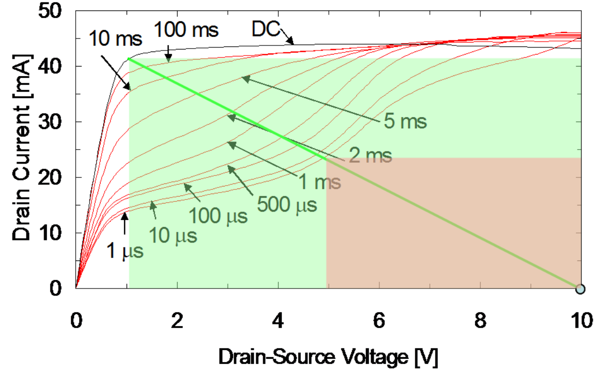


Figure 1.16: Schematic representation of the current-collapsed output characteristics measured decreasing the sample time.

the previous explanation. The different kink enhancement on the different HEMT structures, as reported on the aforementioned papers, can be possibly explained by the same trapping mechanisms but with a completely different trade-off between trapping transient and de-trapping transient.

1.3.2 The *current collapse*

Current collapse is the commonly reported parasitic effect that reduces the RF output power at high frequency. It is also described as *current compression* or *DC-to-RF dispersion* and it causes a reduction of the dynamic saturation current compared to the DC-one, an increase of the access resistances (in particular on the drain side) and, as a consequence, a reduction of the dynamic transconductance, which reduces the RF gain and the output RF power. As reported in figure 1.16, the increase of the drain access resistance, the shift of the knee voltage, and the reduction of the saturation current, cause a significant reduction of the maximum available RF power, from the green area to the red area. Furthermore, the effect increases the high-frequency distortion and reduces the efficiency.

$$P_{OUT} = \Delta V \cdot \Delta I = (V_{br} - V_{knee}) \cdot I_{DSAT}$$

The effect is typically correlated with the accumulation of negative charge on the surface traps. Electrons coming from the gate, due to the high electric-field

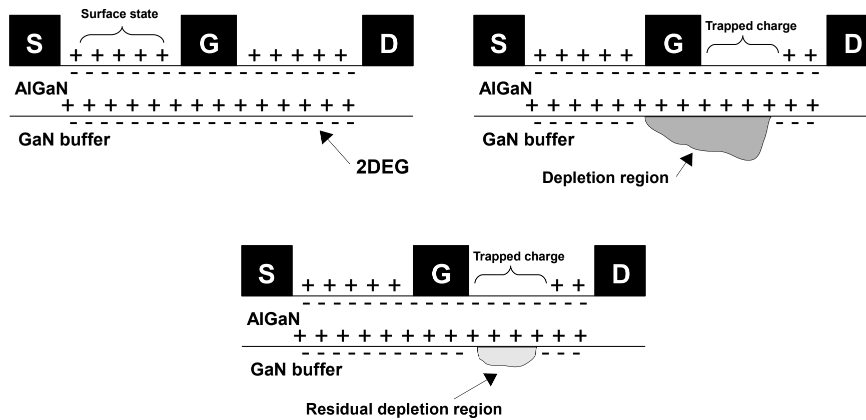


Figure 1.17: Schematic explanation of the current collapse trapping effect [12].

typically located at the drain edge of the gate, can fill the donor states located on the surface close to the gate terminal. It is important to remember that these positive-charged states are useful to balance the negative charge of the channel electrons; for this reason, the absence of a positive charge close to the gate edge will deplete the correspondent part of electron channel.

As clearly visible in figure 1.17, the extension of the depletion region acts as negative biased virtual gate [44] that depletes part of the channel. In this condition, the current along the channel is controlled by two gates: the official-one, controlled by the applied gate-bias, and the virtual-one, controlled by the amount of charge trapped on the surface states. The turning-on of the real gate opens the channel below the gate, but not below the virtual gate, which acts with a delay depending on the de-trapping transient of the surface traps. In this way, considering the normal high-frequency operation, if the electric-field is high enough to fill the surface traps, the device will work with a maximum current depending on the slowest phenomena between the RF-sweep and the trapping/detrapping transients of these traps, and not at the maximum DC performances. In pulsed operation, the device will be affected by the trapping condition induced by the bias-point, and by the de-trapping transient reached after the on-state pulse [45]. It is worth to mention that the surface-state trapping, that partially depletes the channel, slightly reduces the gate-to-drain electric-field as well, resulting in a reduction of the leakage current and a self-limitation of the charge trapping effect.

As previously observed, current collapse effect can hugely reduce the dynamic performance of GaN-devices for RF application, but even the high-power switching devices can be affected by important performance reductions. Indeed, the increase of the drain access resistance and the increase of the knee-voltage can dramatically increase the dissipated power in the closed-switch configuration. Furthermore, compared to the RF counterpart, the electric-field that accelerates the electron trapping is really much bigger, due the higher voltage that the drain terminal has to sustain (greater than 600V). For this reason, the current collapse can affect both the RF and the high-power applications, and needs to be controlled in both cases.

To prevent the dynamic performance degradation induced by the current collapse, many techniques can be applied, from surface *passivation*, to different processing improvements like the *field-plate* of the *gate recess.* The *passivation* consists in the deposition of a insulating material that neutralizes the net surface charge of the AlGaN surface and the surface states associated with material defects or dangling bondings, creating a near-optimal dielectric-semiconductor interface that prevents electron access to the surface traps hence drastically reducing the current collapse effect [41] (see figure 1.18). Due to the different quality, composition and processing steps, each foundry tends to have its passivation recipe; however the most widely passivation dielectric is actually Silicon-Nitride (Si_3N_4).

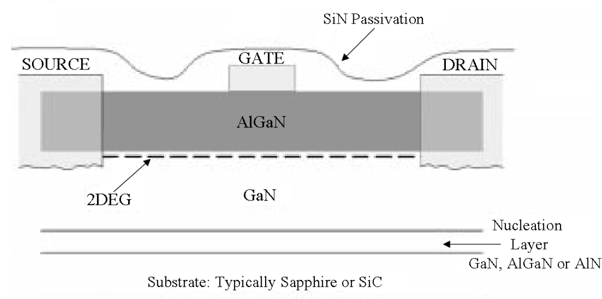


Figure 1.18: Basic GaN HEMT structure with surface SiN passivation [8].

The *field-plate* (FP) consists in the growth of a gate terminal with a different shape compared to the normal rectangular shape. The use of a Γ-*gate* or a *T-gate* with a gate-overhang toward the drain allows to laterally extend the electric-field region reducing its peak, typically located at the drain-edge of the gate, keeping the

same electric-field integral (due to the same voltage drop between the gate and the drain), as reported in figure 1.19 [1, 46, 47]. The peak reduction decreases the gate electron energy and consequently its ability to fill the surface traps, preventing the increase of the current collapse effect. As for the passivation, different field-plate schemes exist depending on the final application of the device: gate-connected FP, the standard configuration, source-connected FP, to reduce the gate-drain capacitance useful for RF performances, or multi FP structures [1].

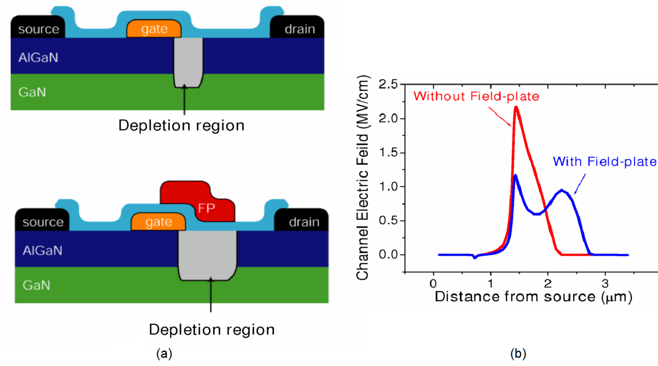


Figure 1.19: (a) Schematic diagrams of HFET structure with and without gate-terminated field-plates. (b) Electric field profiles within the depletion region along the channel on both devices [19].

The *gate recess* technique consists in the deposition of other GaN or GaN-alloys layers on top of the heterostructure, increasing the distance between the channel and the surface. The further the surface from the channel, the smaller the effect of the surface traps on the channel. Then, the gate contact is realized by means of a recess on the upper layers, to reach the AlGaN surface (see figure 1.20).

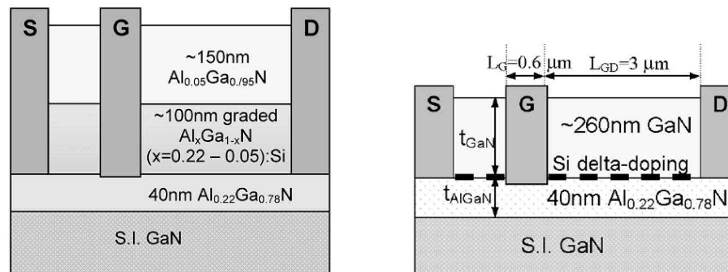


Figure 1.20: Device structure of two deep-recessed GaN-HEMT architectures: with an AlGaN cap (left) or with a GaN cap (right) [1, 48].

Especially Field-Plate technique, but sometimes even particular passivation [49] or recess methods, have important effects even on the reliability behaviour of these devices. For example, these techniques can reduce the electric-field peak and consequently all the high field-driven degradation mechanisms, can reduce the gate leakage currents and the leakage degradations, can avoid relaxation phenomena and mechanical strength of the layer structure, or they can passivate surface defects and their propagation. For these reasons, the same techniques provide significant improvement on both the dynamic dispersion and the high-field reliability of GaN-based devices, making their design a not-trivial step for both RF and high-power applications.

1.4 Reliability issues

The recent development of GaN-HEMT technology has highlighted the very good material properties and the excellent device performances for both RF and high-power switching applications, as seen on the previous sections. Despite the large effort spent in the last few years, and the increased number of published papers concerning device's robustness, reliability has still to be fully demonstrated, partly due to the continuous evolution of the adopted process and technologies, and partly due to the lack of information concerning failure modes and failure mechanisms.

Conventional approaches for commercial semiconductor technologies use the three-temperature accelerated life-tests to extract the life-time of a device. On these tests, devices are biased on the real operative point and, using the temperature as degradation accelerating factor, it is possible to build an *Arrhenius-plot*, a diagram that provides the estimation of the life-time of a device at the real temperature and bias operation, starting from the failure times extracted by the previous tests. Actually, failure mechanisms on GaN devices do not allow to completely rely on these conventional approaches, due to the different degradation modes and to the absence of clearly defined degradation accelerating factors or degradation laws. Indeed, many papers show not thermally activated failure mechanisms or negative temperature correlated failure mechanisms. Furthermore, many of these

mechanisms happen during the first hours of test ("infant mortality"), placing the failures just in the first part of the typical failure-rate curve of any electronic device, sign of a technology still not mature.

In the following figure 1.22 are reported the main failure mechanisms plaguing the GaN-HEMT performances and reducing the device's reliability. From the literature, temperature has been identified as an accelerating factor for passivation stability and for contacts degradation (metal diffusion on the semiconductor or inter-mixing of the metal layers, which respectively cause variation of the Schottky barrier and of the ohmic contact), hot-electrons have been associated to trapping effects on the surface or within the semiconductor layers, and other rather new effects, typical of GaN materials and of the polar nature of the device structure, have been correlated with the gate-edge degradation or with bulk-trap generations.

In particular, during the PhD activity, two mechanisms have been deeply investigated, the reverse-bias gate degradation and the hot-electron induced degradation, to improve the understanding on the involved failure mechanisms and to increase the knowledge of the laws leading to GaN HEMT reliability.

1.4.1 Reverse bias gate degradation

Due to the high breakdown field of Gallium Nitride, high voltages can be applied at the drain terminal on real HEMT application, increasing the power capabilities of these devices, but causing worrying high electric-field values at the drain edge of the gate, in the order of few MV/cm. Several studies of the last years have shown important degradations of the gate performances enhanced by the gate-drain voltage, or the electric-field, increase. In particular it has been show that decreasing the gate voltage, keeping fixed the drain and/or the source voltage, the gate leakage starts to abruptly increase after a "*critical voltage*" typical of the tested wafer. The few order of magnitude non-recoverable increase of the gate leakages is followed by an increase of dispersion phenomena, an increase of the access resistances, and a decrease of the drain current [51], as reported in figure 1.23.

After this first result, many other research groups have observed the same effect,

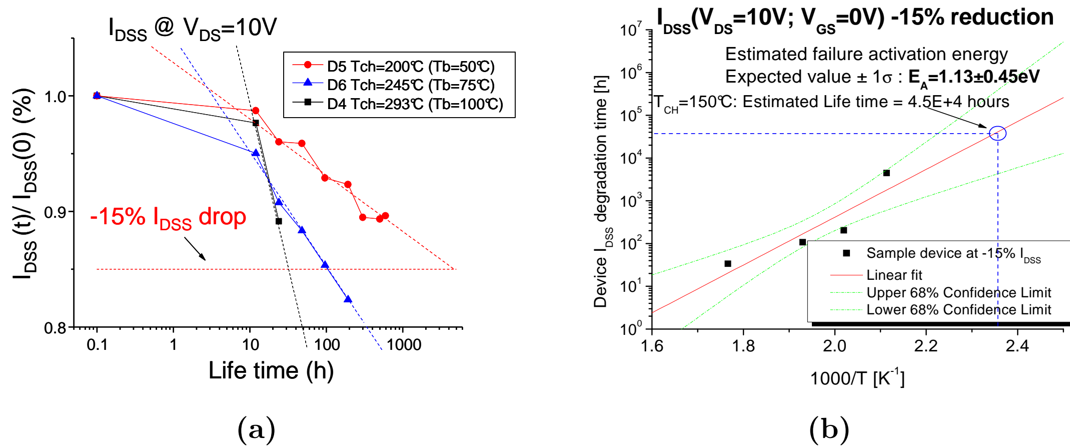


Figure 1.21: Experimental example of drain current degradation during a three temperature life-test (a) and the corresponding Arrhenius plot (b).

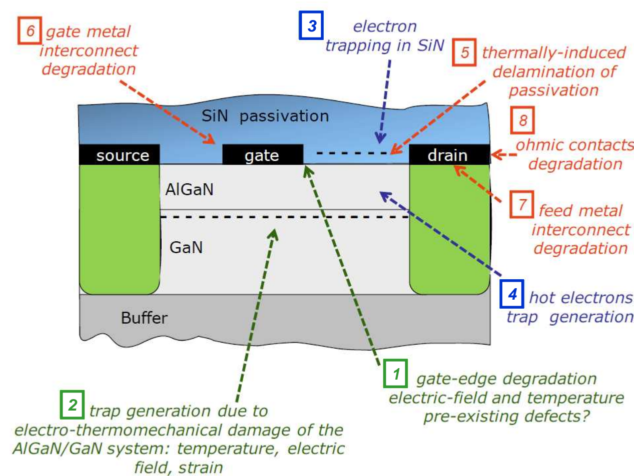


Figure 1.22: Failure mechanisms recently identified on GaN HEMTs. In red, thermally-activated mechanisms; in blue, mechanisms related to the presence of hot electrons, which are common to all high-voltage Field-Effect-Transistors; in green, mechanisms which are peculiar to GaN devices, due to the polar and piezoelectric nature of this semiconductor material [50].

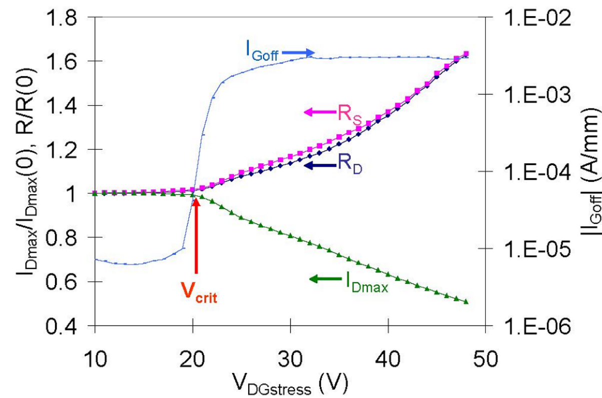


Figure 1.23: Change in the main electrical parameters during a reverse bias step-stress test [51].

with few small differences but with the same big increase of the gate current after a wafer-defined failure voltage [6, 51–55]. The increase of the gate leakage and the increase of the dispersion effects suggest the creation of new traps probably within the AlGaN layer close to the gate-edges, the region mainly affected by the highest electric-field. The explanation of this failure mechanism has been proposed by *Joh et al.* [6], using the concept of the *converse piezoelectric effect*. The model takes into consideration the piezoelectric nature of GaN and AlGaN materials and the extremely high vertical electric field within the barrier layer in the normal HEMT application (see figure 1.24). Indeed, the latter is subjected to significant in-plane tensile stress (with stored elastic energy) due to the polarization contributions, spontaneous and piezoelectric, even without bias. When a reverse bias is applied, the vertical component of the electric field at the gate-edge sharply increases, thus enhancing the tensile strain and the stored elastic energy, particularly at the edge of the gate where the field reaches its maximum value. Once a certain critical level of stored elastic energy or strain is reached, crystallographic defects can be produced in the AlGaN especially at the points where the sum of the intrinsic and the applied field is maximum. These defects can then promote the injection of electrons from the gate into the AlGaN barrier layer, through a trap-assisted tunneling mechanism, inducing parasitic paths for the leakage current increase. Consequently, defects can degrade the electrical characteristics of the transistors by affecting transport properties or by inducing trapping effects.

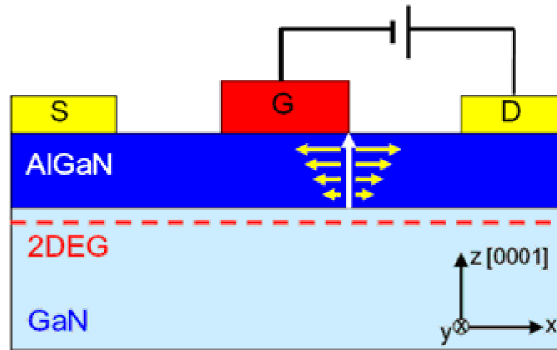


Figure 1.24: Illustration of GaN HEMT under reverse bias between gate and drain. Mechanical tensile stress (yellow) is induced by the vertical electric field (white) through inverse piezoelectric effect [56].

Creation of new vertical leakage paths has been confirmed by *Zanoni et al.* [54] showing a good correlation between the appearance (and the growth) of few emission "hot-spots" at the gate edges and the increase of the gate current, as reported in figure 1.25. In fact, once injected into the AlGaN layer, electrons can reach extremely high energy values and, once reached the channel, they can relax their energy generating light due to intra-band transitions. Each jump of the gate stress current typically corresponds to the appearance or the increase of a hot-spot, suggesting the creation of a new parasitic leakage path. For this reason, the emission analysis by means of electroluminescence measurements can be a useful tool for monitoring and predicting the gate failure behaviour, just checking the presence or the appearance of new hot-spots at the gate edge. Moreover, from the polar nature of the GaN materials, the aforementioned failure mechanism should be influenced by each factor that contributes on the electric-field increase at the gate-edge, like material properties (AlGaN composition, thickness, defectivity), surface characteristics (passivation efficiency) and processing characteristics (gate-length and field-plate structure).

Due to the crystal defects caused by the strain relaxation on the "weakest" points of the gate-edge, many research groups have introduced failure analysis techniques, in particular Transmission Electron Microscopy analysis (TEM), to try to confirm the failure mechanism with a clear signature of the material defect

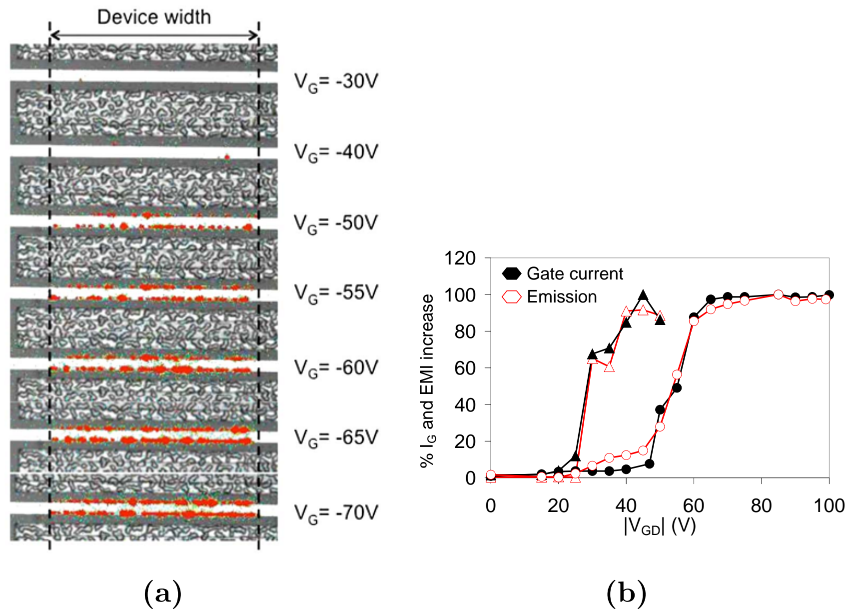


Figure 1.25: Electroluminescence microscopy images of a representative gated-TLM HEMT sample submitted to reverse-bias gate step-stress, taken at a fixed bias (a), and correlation between the relative increase in gate current and electroluminescence intensity on the same TLM structure of two different wafers (b) [54].

creation. TEM analysis performed after long-term tests in high-voltage conditions have revealed the formation of pit-shaped defects near the drain side of the gate contact, with nanometer-scale depth, and of thin cracks extending into the AlGaN barrier layer, sometimes starting from the bottom of a pit defect. Temperature has been found to enhance this pit formation and, on the extreme cases, to promote gate metalization diffusion into these cracks [57, 58]. Therefore, TEM and in general Destructive Physical Analysis (DPA) can be powerful tools for a better understanding of the physical failure evolution, especially in heavy-degraded devices, but sometimes it could be not so easy to detect nanometer-size cracks during the early stage of device degradation.

It is worth to mention that the high voltage used in the previous tests, and the induced high electric-field inside the HEMT structure, can promote electron trapping on the surface states. The trapped charge decreases step-by-step the internal electric-field limiting the strain increase and consequently the defects formation. For this reason, the step-stress approach on a trapping-prone device can give a

rather overoptimistic definition of the failure threshold value, with respect to an experiment where a high gate-drain voltage is directly applied on a fresh device.

1.4.2 Hot-electrons degradation effect

Device aging due to hot-electrons effect is another failure mechanism that can be invoked to explain degradation of GaN HEMTs. The high-voltage breakdown and the high current capabilities can allow device operation with the simultaneous presence of very high electric-field and high channel electron concentration. The channel electrons accelerated by the high electric-field, especially in submicron-gate devices, can reach energies much higher than the equilibrium value, becoming *"hot electrons"*. The hot electrons can overcome energy barriers, can dissipate their extra energy in collision with the crystal, and they can create defects or dangling bonds which may act as deep levels or traps. For these reasons, hot electron can be the origin of degradation processes and trapping phenomena within the passivation or GaN layers, as described in figure 1.26. The interaction with the AlGaN layer can indeed enhance the crystal defect propagation and increase the vertical leakage paths, as described on the previous section, but up to now there is no clear evidence that hot electrons can be unambiguously ascribed as the origin, or the accelerating factor, of GaN-HEMT performance degradations.

The reason comes also from the negligible impact-ionization effects inside the GaN materials, due to the extremely wide band-gap compared to other technologies like Gallium-Arsenide. In GaAs HEMT, the lower energy-gap allows hot electrons to reach energies high enough to induce impact-ionization phenomena, and thus the hot-carrier effect can be simply measured by monitoring the gate current increase caused by the collection of the holes generated by impact-ionization [59]. The hot-electron's index can be used to derive field-acceleration laws for the failure time of AlGaAs/GaAs HEMTs submitted to hot electron tests in different bias conditions [60]. In GaN-HEMT technology, the negligible impact-ionization rate and the gate current, usually dominated by tunneling injection mechanisms, prevent the use of this current as a hot-electron indicator. An alternative method for hot electron evaluation comes from the *electroluminescence measurements* (EL).

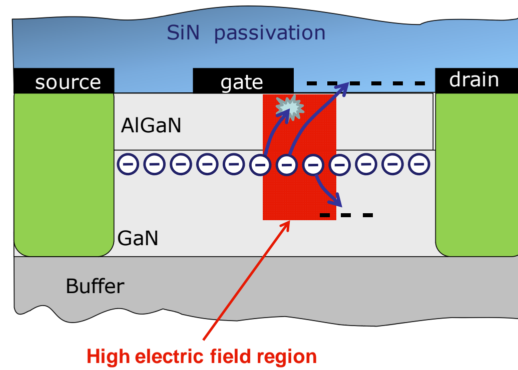


Figure 1.26: Schematic cross-section of an AlGaN/GaN HEMT, identifying the gate-drain high electric-field region where electrons can achieve high energy and become "hot". Hot electrons can generate crystallographic damage; overcoming the AlGaN barrier, they can be trapped within the SiN passivation or in the AlGaN, or in deep levels within the GaN layer [50].

Luminescence in HEMT is usually due to intra-band transitions of highly energetic electrons. In GaN devices, this is not due to band-to-band recombination, but typically associated with hot-electrons accelerated by the high longitudinal electric-field in the channel, which scatter with charged centers releasing the energy in the form of photons [61, 62]. Measuring the electroluminescence as a function of gate voltage (V_{GS}), keeping V_{DS} constant, the EL intensity shows a non-monotonic behaviour typical of hot-electron effects, as reported in figure 1.27. At low V_{GS} below the pinch-off voltage, the drain-to-gate voltage is maximum inducing the maximum electric-field; but, due to the absence of electron in the channel, the emission intensity is zero. Increasing the gate voltage, the carriers start flowing and are simultaneously accelerated by the high electric-field in the gate-drain region, thus increasing the light emission in particular at the drain-edge of the gate, the region subjected to the highest electric-field. But at the same time, the increase of the gate voltage causes the decrease of the drain-to-gate voltage and consequently of the electric-field. When the carrier increase can no longer balance the electric-field reduction, the emission intensity starts to decrease. Increasing the drain voltage, the EL keeps the same bell-shaped behaviour, but it increases its intensity with a near-exponential trend, and it slightly shifts the V_{GS} corresponding to the EL-peak,

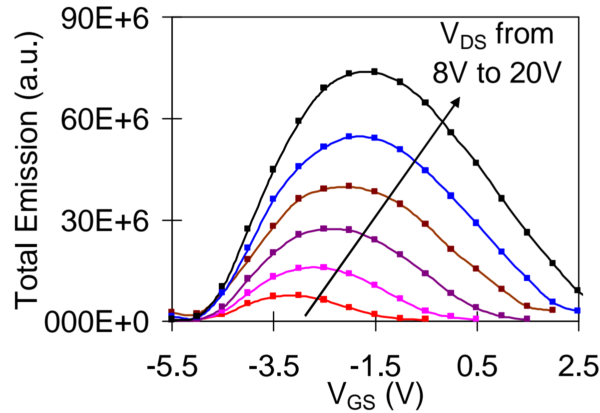


Figure 1.27: EL intensity in a 1 µm gate-length device as a function of V_{GS}, from pinch-off to open channel condition, at various V_{DS}. A non-monotonic behavior typical of hot carrier induced phenomena is observed [63].

depending on the different trade-off between electron concentration and electric-field intensity at higher drain voltages. Therefore, the electro-luminescence measurements at different gate voltages gives an efficient method for the hot-electrons evaluation.

In the recent years, hot-electron degradation has been proposed as the dominant failure mechanism on GaN-HEMTs just in few works. *Coffie et al.* [64] have presented a RF-power degradation with a negative activation energy, typical of hot-electron induced degradation. *Meneghesso et al.* [63] have shown bigger performance reduction on semi-ON state stress with respect to ON-state (higher temperature) and OFF-state (higher electric field) stress, followed by a remarkable slow-trapping phenomena especially at the highest current tests.

1.5 Outline of the thesis

After this first analysis of the GaN-HEMT capabilities and of the main issues that reduce the performances of these devices, in a recoverable (trapping effects) or non-recoverable (degradation effects) way, following chapters summarize the targets of the thesis and the main results obtained during the three years of PhD activity. The first two chapters analyze the reliability behaviour of GaN-HEMT

devices of two different projects and technologies, but with the same target of understanding the failure mechanisms that mainly limit the device performances in the real application, with a special focus on the high-field reliability. The following chapter deals with the gate robustness and with the mechanism that leads this failure, to understand if it is caused only by the voltage (and the electric-field) applied on the gate-drain region, or if other factors, like the gate leakage, can be important on the device failure. Finally, chapter 5 shows the study of two particular trapping effects and the physical correlation between the trap's position and the electrical effect. In particular:

- *chapter 2* shows the results obtained during the last reliability activity inside the European KorriGaN project, named *Task-Force* project. The purpose was to define the most critical working conditions over the last set of devices developed within the project, and to study the failure mechanisms that reduce the main device performances on short and long time period, obtaining an important result concerning hot-electron induced degradation;

- *chapter 3* shows the results obtained testing the robustness of space-designed GaN-HEMT devices. The objective was to define the reliability behaviour of this technology and to identify the main degradation mechanisms that can reduce the device performances in the real long-term operating conditions, testing the high temperature stability, the high high-voltage robustness, and the combination of these two effects;

- *chapter 4* describes a deep analysis of the OFF-state reliability of GaN HEMTs, in particular studying the failure mechanism leading to the gate degradation. Despite the common acceptance on the *critical voltage* definition, some different results suggest a failure mechanism correlated with the initial defectivity of the device under test;

- *chapter 5* describes two deep investigations on typical parasitic effects of GaN-HEMT devices, performed inside the European MANGA project. In the first part, a combined electro-optical analysis allows to better understand the origin of the kink effect, correlating this effect with the electron

interaction with the GaN-traps responsible of the yellow-luminescence. On the second part, a brief analysis on particular Fe-doped GaN devices allows to correlate the presence of Fe-doping with an increase of the current collapse effect especially at the high electric-field bias points;

- finally, *chapter 6* summarizes the activity of the thesis, underling the main results and possible future studies starting from the achieved results.

Chapter 2

Reliability evaluation of GaN HEMTs in Task-Force project

This chapter reports all the activity performed inside the last task of the reliability sub-project of the European project *KorriGaN* (Key ORganisation for Research on Integrated circuit in GaN technology), called *Task-Force project*. KorriGaN has been a large-scale European joint Research and Technology Project performed within the European framework, aiming at the development of microelectronic components. With the contribution of seven nations and a 29-partners consortium, it has provided all the necessary competence in key areas dedicated to semiconductor technologies such as substrate growth, device processing, circuit design and modeling, circuit packaging and integration. The main objective of KorriGaN project has been to develop a stand alone European supply chain for GaN-HEMT technology, providing all major European defence industries with reliable state-of-the-art GaN foundries services. The key objectives of the last reliability task have been:

- to analyze existing and future data on tested wafers/PCM/devices in order to identify possible correlations between device reliability and substrate, epitaxy or processing;
- to collect and correlate the experiments carried out by the various foundries that are aimed at identifying the influence on reliability of specific and well defined process changes;

- to design and manage specific experiments aimed at identifying the effect of substrates on device reliability, by correlating the measured “quality” of *Cree* and *Norstel* SiC substrates with subsequent measurements on processed wafers and devices.

With these targets, the Task-Force activity has been focused on the identification of substrate or epitaxy correlated issues, by means of characterization measurements and reliability tests. These tests have been carried out on 4 wafers characterized by a completely different quality of the substrate and epi-layers, but with the same device processing, to complete the database that correlates the reliability behaviour with the different adopted processes.

2.1 Task-Force project

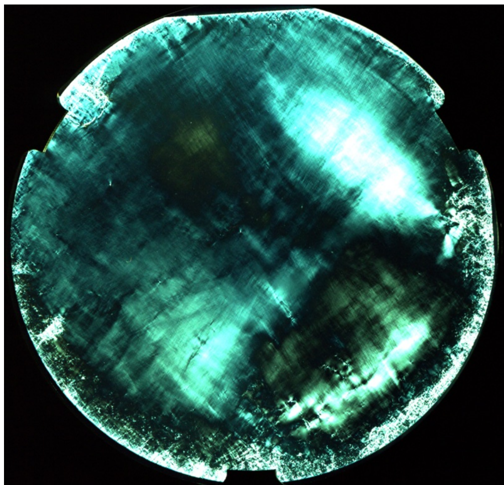
The purpose of the project has been to define the most critical working conditions over the last set of KorriGaN devices and to study the failure mechanisms that reduce the main device performances on short and long time period. In particular, the failure mechanisms and the degradation accelerating factors had to be correlated with the different substrate quality of the used wafers or to the different defects concentration of the epitaxial layers.

For these reasons, four wafer have been processed exploiting the knowledge acquired along the project, with a common epitaxial process performed by Picogiga, but starting from substrates with different quality coming from different foundries: *Cree* and *Norstel*. From each foundry, the best and the worst substrate has been chosen giving the name to the final processed wafer, as it can be seen in table 2.1 and in figure 2.1. The final device processing has been performed by Chalmers University, including all the processing improvements acquired during the project, using the same mask layout for all the wafers.

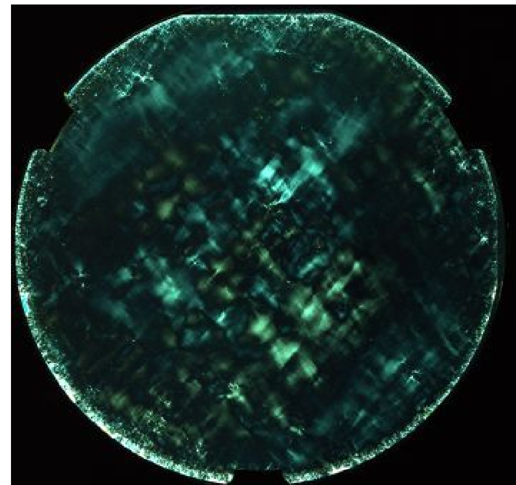
In figure 2.2 the device layer structure is reported. As previously indicated, different quality SiC substrates have been used for the device processing. Two wafer from *Cree* and two from *Norstel*, with different defects density: two with low defects concentration (the “good”-ones) and two with high defects concentration

Substrate ID	Substrate supplier	comment	Epi ID	Epi house	Process wafer no.
D2002-16	Norstel	"poor Norstel"	L1474	Picogiga	W1
D079-09	Norstel	"good Norstel"	L1477	Picogiga	W2
HK0293-29	Cree	"good Cree"	L1478	Picogiga	W3
RC0009-14	Cree	"poor Cree"	L1479	Picogiga	W4

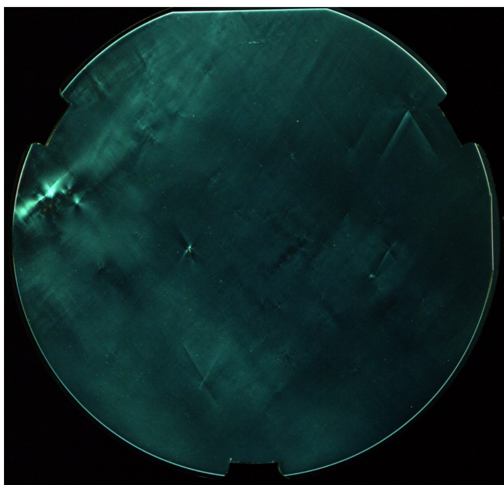
Table 2.1: Process details of the four Task-Force wafers



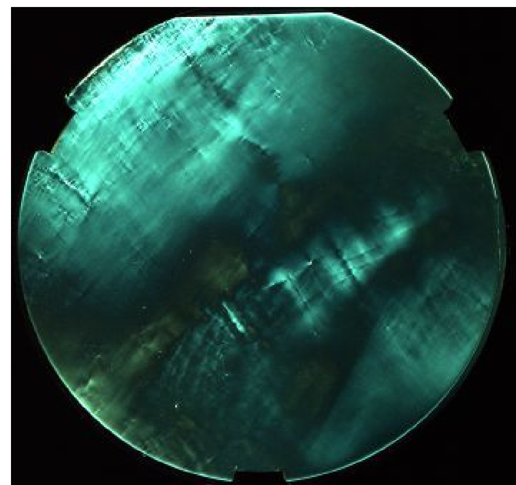
(a) L1474 - poor Norstel



(b) L1477 - good Norstel



(c) L1478 - good Cree



(d) L1479 - poor Cree

Figure 2.1: Xpol images of the 4 Task-Force wafer substrates. The light intensity refers to the defects concentration: the lighter the region, the higher the defects concentration.

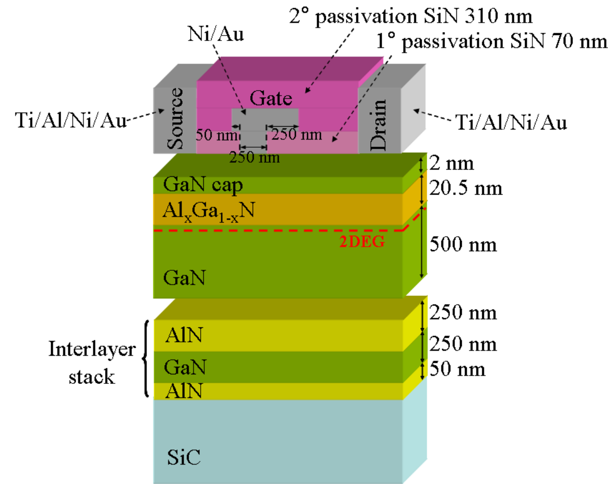


Figure 2.2: Schematic cross-section of the Task-Force AlGaN/GaN HEMT devices.

(the "poor"-ones), as reported in figure 2.1. Before the GaN buffer deposition, an interlayer stack has been grown on top of the SiC substrate to reduce the strain and the defects propagation; the stack is formed by an AlN layer (50 nm), a GaN layer (250 nm) and finally another AlN layer (250 nm). Then a GaN buffer has been deposited with a thickness of about 500 nm. On top, the AlGaN barrier has been realized (20.5 nm thick, Al content between 24.8% and 26.7%). Finally a GaN cap layer of 2 nm has been grown on top of the structure. Processed samples have been two- and eight-fingers transistors ($W_G = 200$ μm and 800 μm respectively) with a 250 nm recessed gate defined by an e-beam process into a first passivation layer, and with a field plate that extends 250 nm toward the drain and 50 nm toward the source. The first passivation layer has been located beneath the field plate and the second passivation layer has been used to cover the gate; both passivation layers on SiN. The process has been realized with a combination of stepper and e-beam lithography. All tests have been performed on 2×100 μm gate-width devices, and only in few cases on gated-TLM structures, with the same layer stack but with a gate-length $L_G = 5$ μm and a gate-width $W_G = 100$ μm.

Due to a processing problem on the ohmic contact deposition, many devices of the "poor Norstel" wafer have been short-circuited on the gate-ohmic junction, making these devices completely unusable. As a consequence, this wafer has not been subjected to many studies, but only to the preliminary characterization phase.

2.2 DC and dynamic performances

At the beginning of the reliability analysis, a complete static and dynamic characterization has been performed on many devices of the four wafers, to extract the most important performance parameters as a first indicator of the DC and of the dynamic behaviour of the transistors.

The DC measurements have been carried out by means of a standard parameter analyzer. Table 2.2 summarizes the main DC parameters averaged on a set of 10 sample per wafer. Devices show a quite homogeneous behaviour and good electrical performances all along the wafer. The output current is around 0.8-0.9 A/mm (below 20% variation inside the wafer), with a transconductance peak above 0.3 S/mm. Only the leakage current shows rather high values above 100 μA/mm, due a quite high reverse diode leakage. Among wafers, DC characteristics are quite similar, with differences connected with a limited variation of the threshold voltage.

WAFERS	$\mathbf{I_{DSS0}}$ $\mathbf{V_D=10V\ V_G=0V}$ **(A/mm)**	$\mathbf{g_{mMAX}}$ $\mathbf{V_D=5V}$ **(S/mm)**	$\mathbf{\lvert I_{GLEAKOFF} \rvert}$ $\mathbf{V_D=10V\ V_G=-6V}$ **(A/mm)**	$\mathbf{V_{TH}}$ $\mathbf{V_D=5V}$ **(V)**
L1474	0.71	0.315	1.89E-04	-2.37
L1477	0.90	0.310	4.71E-04	-3.23
L1478	0.81	0.301	5.37E-04	-3.00
L1479	0.89	0.312	5.75E-04	-3.36

Table 2.2: Main parameters extracted from the DC characterization on the Task-Force wafers.

Looking at the dynamic performances, the 4 wafers have shown a very similar dynamic behaviour, with low dispersion effects. The current collapse has been measured with a custom double-pulser system similar to the commercial Dynamic IV Analyzer (DIVA). The system is able to provide synchronized pulses at the gate and the drain of the device under test starting from arbitrary quiescent points, to investigate the parasitic phenomena due to the presence of surface or buffer

traps, and to evaluate and compare the current collapse among different wafers. In particular, in our case, pulse width and pulse period have been set to 1 μs and 100 μs respectively. Using different quiescent points, it is possible to obtain a output or trans- characteristics with different dynamic behaviours: starting from a quiescent point of $V_G = 0V$ and $V_D = 0V$, it is possible to observe a trap-free characteristic, avoiding the self-heating effect induced by the high power density inside the active area; starting from a negative gate voltage or from a high V_{DG} quiescent point, it is possible to induce trapping below the gate or within the surface, observing the current collapse induced by the transient behaviour of these traps. Observing the output drain current extracted from the trapped and the un-trapped curves, it is possible to compare and quantify the dispersion induced by the traps, and to associate the collapse to a specific trap's location [65]. For this reason, in order to compare the dynamic performances of the different tested devices, it is useful to extract a parameter, called *Slump Ratio* (S.R.), which takes into account the current compression induced by the trapping effects. The S.R. parameter is typically defined as follow:

$$S.R. = \frac{I_{DS0(Vg<Vth,Vd=Vdd)}}{I_{DS0(Vg=0V,Vd=0V)}} \quad \text{with } I_{DS0} = I_{DS} \text{ in saturation}$$

In the following table 2.3 are reported the averaged Slump Ratio values extracted from the dynamic measurements performed on each Task-Force wafer. The parameter has been extracted from the ($V_G = 0V$,$V_D = 0V$) quiescent point and a ($V_G = -6V$,$V_D = 10V$) trapped quiescent point. All devices show a very good and stable dynamic behaviour, with consistent S.R. values around 0.9, quite uniform even among the four wafers.

The low presence of traps has also been confirmed by RF power measurement carried out at 2 GHz with a load-pull system, in collaboration with the University of Modena and Reggio Emilia. Devices have been biased in class A condition, with $V_{DD} = 25V$, $I_{DS} = I_{DS-Sat}/2$, and a load impedance matched to obtain the maximum RF output power. The obtained results are promising and very consistent inside the wafer and among wafers: devices yielded a continuous-wave power density of about 4.6 W/mm with 51% of power added efficiency (PAE) peak.

	Slump Ratio S.R.
L1474	0.903
L1477	0.914
L1478	0.913
L1479	0.901

Table 2.3: Averaged Slump Ratio extracted from the dynamic measurements on the Task-Force wafers.

2.3 Short term reliability tests

After the preliminary measurements aimed to check the DC and dynamic behaviour of the devices and the homogeneity of the performances along the wafers, it has been possible to start a first reliability campaign to investigate the more severe conditions to test the devices. From this point, all the tests have been performed on three wafers, excluding wafer L1474 "poor Norstel" due to the small number of working devices.

The first reliability assessment has consisted on short-term stress on the small $2 \times 100\,\mu$m gate-width devices, with the main objective of defining the more interesting conditions to stress the devices on future long-term tests, and to understand the main degradation mechanisms and the related accelerating factors.

The improved robustness of these devices compared with the other previous devices processed inside KorriGaN project, especially in high-field conditions, have suggested further investigations at different bias conditions, much more similar to the real device application. As reported in the following section, the focus of the reliability tests has been moved from the off-state robustness, and its correlation with the substrate quality, to the dominant failure mechanisms in on-state conditions and the related accelerating factors. This target change has been defined after the first reliability assessment, considering the negligible influence of the substrate or the epi-layers quality on the device robustness, as reported on the following parts.

2.3.1 Reverse-bias gate step-stress

Starting from the experience of previous KorriGaN reliability tests, many tests especially at the beginning of the campaign has been focused on the OFF-state robustness. Two-minutes reverse bias step-stress tests, with source floating, and the gate-drain junction reverse-biased from -15V to -100V (step -5V) have been used to test the gate diode robustness submitted to high-electric fields. As previously reported, this type of stress has become really interesting in the last years due to the common gate degradation mechanism, quite consistent on all GaN-HEMT technologies, and to the great interest of many research groups on this failure mode. The tests have been performed on the 2×100 μm gate-width devices and even on the gated-TLM with 5 μm of gate length, to have comparable results with the other HEMT devices previosly tested inside the project. On the last structure, due to the gate processed in the middle of the drain-source distance, the stress has been applied on both gate-diodes, forcing both the drain and the source to ground.

As reported in figures 2.3 and 2.4, devices have reached very high negative gate biases (-200V for the gated-TLM and -100V for the $2{\times}100\mu$m transistors) compared to the older KorriGaN wafers (see figure 2.5), without showing the expected gate degradation, always visible on the other wafers: the gate leakage shows limited variation or only a small decrease after each step of stress, with no emission spots in the OFF-state images taken at a fixed bias condition ($V_G = -10V$ and $V_D = 0V$; $V_S = 0V$ only on gated-TLMs), sign of the absence of any gate contact damage [54] (see inset in figures 2.3 and 2.4). The other electrical parameters have shown limited variations correlated to a small threshold voltage shift. This behaviour has been observed on both type of devices and on all tested wafers, suggesting a negligible influence of the substrate quality on the final high-field device robustness, maybe due to an improved layer growth or device processing.

2.3.2 Three-terminal reliability

A similar kind of stress has then been used to analyze the robustness on the two-fingers transistors. Two types of stress have been performed to check the maximum voltage limitations, by means of a fast step-stress, and the static performance

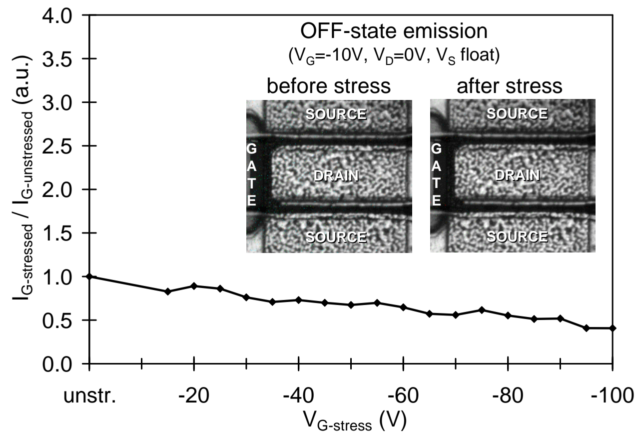


Figure 2.3: Transistor I_{GD} diode leakage (at $V_{GD} = -8V$) variation during reverse bias gate-drain step-stress. Inset graph: OFF-state emission images before and after the step stress.

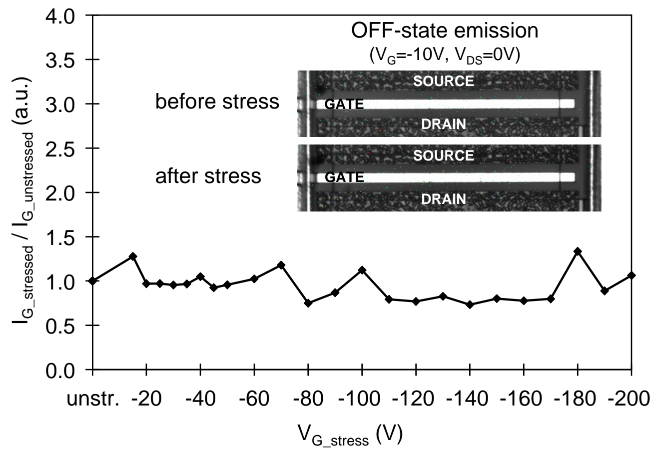


Figure 2.4: Gated-TLM I_{GS} diode leakage (at $V_{GS} = -8V$) variation during reverse bias gate step-stress. Inset graph: OFF-state emission images before and after the gate bias step stress.

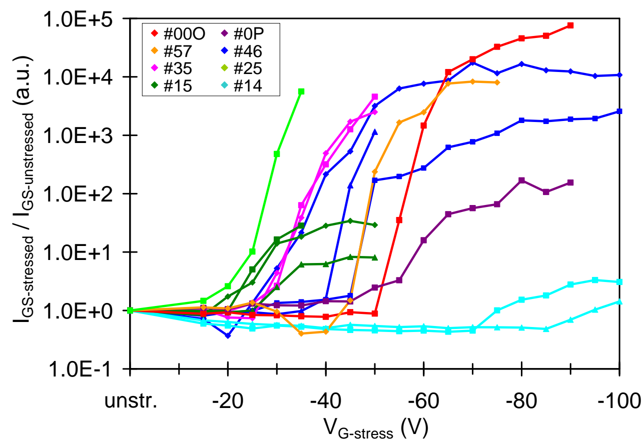


Figure 2.5: 5 μm gated-TLM I_{GS} diode leakage (at $V_{GS} = -8V$) variation during reverse bias gate step-stress on other previous KorriGaN wafers.

degradation, after 1-hour of DC stress. In particular, the employed tests have been:

- two-minutes drain voltage step-stress test up to device failure (limited at 100V, 5V step), at V_{GS} = -1V, -2V, -5V;
- 1 hour DC stress at three bias points based on a 50 Ω load-line, with a $V_{DD} = 30V$: ON-state, semi ON-state, OFF-state. The semi ON state has been chosen as the point corresponding to the peak of the emission intensity.

Two minutes drain voltage step-stress have shown different results depending on the gate bias condition, but uniform among the wafers. The OFF-state step-stress have shown negligible device degradation until 100V, with only a small negative shift of the threshold voltage followed by a small increase of output current (I_{DSS0}) and of the transconductance peak (g_{mMAX}; see figure 2.6). In the other gate bias conditions ($V_{GS} = -2V$), the stress has caused a gradual degradation of drain current and transconductance of the tested device, until a certain V_{DS} (60V for L1477 and 70V for L1478-L1479); at this voltage, the device failed due to the high leakage that breaks the gate-source junction. Further increase of the gate voltage has induced the same behaviour but with a slightly lower drain failure voltage.

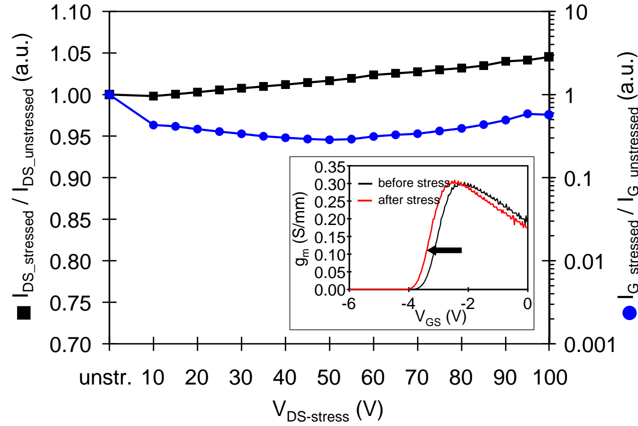


Figure 2.6: Transistor I_{GS} diode leakage (at $V_{GS} = -6V$) and I_{DS} drain current (at $V_{GS} = 0V$ and $V_{DS} = 10V$) variation during 1-hour OFF-state drain step-stress. Inset graph: g_m-V_{GS} (at $V_{DS} = 10V$) before and after the step stress.

The other 1-hour long DC stress have generally caused very small device degradation in all three bias conditions, and on all wafers. The ON-state stress has caused a small positive V_{TH} shift, with a small reduction of the main performances (I_{DSS0} and g_m), whereas the OFF-state stress has caused a more pronounced negative V_{TH} shift, with a small increase of I_{DSS0} and g_m. Leakage currents have shown a stable behaviour with only a small reduction in ON-state tests and a small increase in OFF-state tests, but without causing any device damage or device failure. The tests have been performed even increasing the V_{DD} of the load-line ($V_{DD} = 40V$), but with very similar results. Therefore, devices have generally suffered a variation of the performance parameters within 5-10%, with a threshold voltage shift correlated to the gate bias: the ON-state tests have typically shown a small positive V_{TH} shift whereas the OFF-state tests have shown a negative V_{TH} shift more pronounced at higher drain-to-gate voltages.

The same high-field tests (reverse-biased gate and three-terminal OFF-state) have been performed even on few devices processed above substrate or epi defects, recognized by the superimposition of the XPol images of the substrate or the epi-layers with the pictures of the processed devices. And even in these devices, the high electric field has not induced any bigger device degradation compared to the

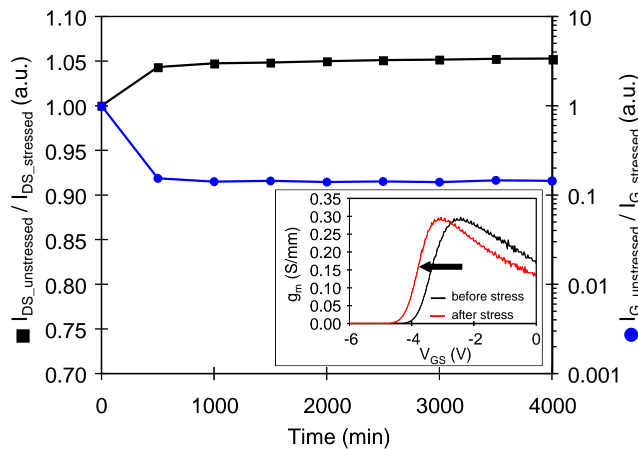


Figure 2.7: Transistor I_{GS} diode leakage (at $V_{GS} = -6V$) and I_{DS} drain current (at $V_{GS} = 0V$ and $V_{DS} = 10V$) variation during a 67 hours OFF-state DC stress. Inset graph: g_m-V_{GS} (at $V_{DS} = 10V$) before and after the DC stress.

other "non-defected" devices, but only the common threshold voltage shift.

Summarizing, the OFF-state tests have underlined a very good device robustness after all the different kind of stress, in three-terminal OFF-state tests and in reverse-biased gate tests. Furthermore, three-terminal OFF-state tests, repeated for longer time stress, have shown a very stable behaviour even after 60 hours of stress, with only the already seen negative threshold voltage shift (see figure 2.7).

Only the semi ON and ON-state tests have shown a limited degradation of the device performances, a bit more pronounced only on wafer L1477, but quite smaller compared to other GaN devices of the same project (at least after 1 hour of test). From these tests, the permanent failure seems to be correlated only with the high gate leakage and not with the other parameter's degradation, possibly caused by the high temperature that increases the gate leakage and, after a critical point, suddenly breaks the gate-to-source junction. In fact, further tests performed at other gate voltages have shown a failure voltage that seems to follow a power-law dependence on V_{DS}, with critical voltages always around 5 W of dissipated power (the red curve in figure 2.8), supporting the previous explanation. This result makes the dissipated power one of the most important degrading factors for this technology, at least for the critical diode failure. But, at this point, it is still

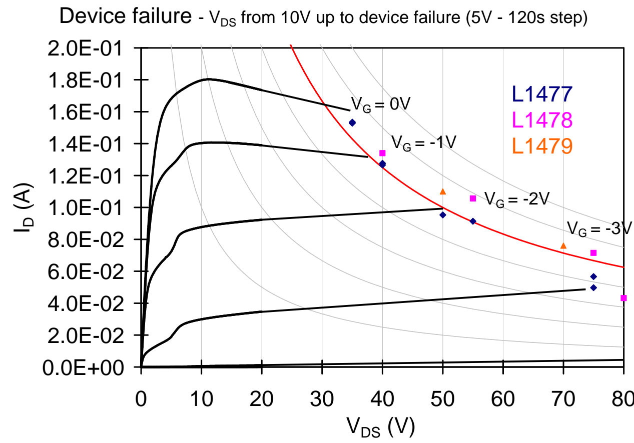


Figure 2.8: Position of the drain step-stress failure voltages at different gate bias, and on the three tested wafers. The colored dots correlate the diode failure voltage (V_{DS}) with the drain current during the last step of stress where the diode starts to fail. All the dots seem to lie on the 5 W curve (the red-one on the diagram), suggesting a power correlated diode failure.

unclear what element drives the device degradation along the time, due to the very limited parameters variation observed in all ON or semi ON-state tests.

In conclusion, all the results obtained from the short-term tests have shown a big improvement on the device robustness compared to the previous KorriGaN wafers, independently on the substrate quality or on the defects concentration, especially in high-field conditions. This suggests that an improved layer structure, with a particular stack of nucleation layers, and an improved device processing, thanks to the field-plate and to the GaN cap-layer, can achieve unexpected device robustness reducing the influence of the defects concentration or of the poor layer quality.

2.4 Medium term reliability tests

Due to a significant increase of the high-field robustness of Task-Force devices, at this point it would be interesting to better understand the reliability behaviour in ON-state condition, and to understand which are the dominant failure mechanisms

and the related accelerating factors that limits the device performance in these bias conditions. For similar robust technologies, few literature results report failure mechanisms correlated with electron trapping [66] or with hot-electrons induced degradation [64].

Therefore, considering all the results obtained from the short-term reliability tests, it has been decided to perform an intense medium-term reliability campaign in order to distinguish which is the most important degrading factor of this technology. Using an approach similar to the failure mechanism evaluation reported by *Dieci et al.* in [60], it has been defined a wide set of stress bias points and a fixed stress structure longer than 1 hour (due to the very limited parameter variations seen on the previous short tests). For practical issues, the stress duration has been fixed at 14 hours, stopped at regular intervals (after an experimentally defined relaxation time to avoid slow trapping effects) to monitor all the electrical and sometimes the optical parameter variations along the stress, and to keep under control all the possible degrading factors.

Due to the impossibility of using the gate current as an hot-electron index like on the GaAs technology, it has been exploited the GaN electroluminescence properties. In fact, it has been observed that EL intensity represents a reliable estimate of channel hot-electron effects for this technology: it has a non-monotonic dependence on V_{GS}, typical of hot-carrier effects (see figure 2.9) and it follows the usual phenomenological *Chynoweth's law* [67], especially at high drain-source voltages (see figure 2.10):

$$EL/I_D \sim exp\left(\frac{-1}{V_{DS} - V_{DSAT}}\right)$$

EL intensity has been characterized by means of EL measurements versus V_{GS} and V_{DS}, showing the non-monotonic behaviour as a function of V_{GS}, since hot-electron population first increases (as the channel opens) and then decreases (due to the electric field decrease). As can be seen in figure 2.10, the logarithm of the EL intensity/I_D ratio has a linear dependence on the reciprocal of $(V_{DS} - V_{DSAT})$, a measurable quantity which is directly proportional to the accelerating electric-field [68]. This result is commonly considered as a signature of the fact that the

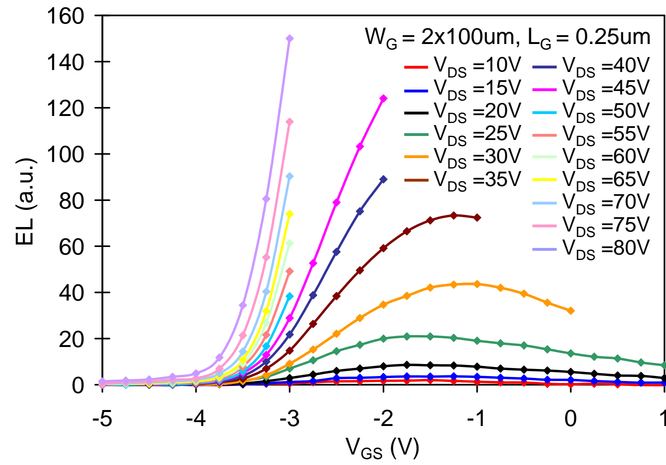


Figure 2.9: EL intensity vs. V_{GS} for various V_{DS} in an untreated sample, which shows the typical bell-shaped behaviour on V_{GS}. The curves at high V_{DS} have been interrupted for power issues.

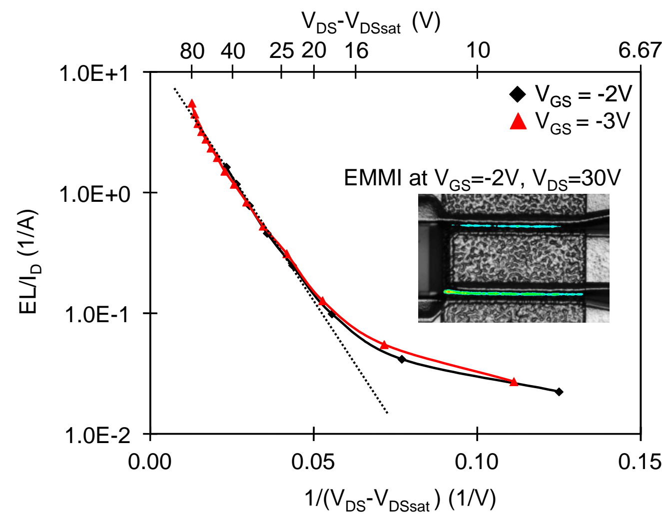


Figure 2.10: $log(EL/I_D)$ vs. $1/(V_{DS} - V_{DSAT})$ plot showing that EL follows the phenomenological *Chynoweth's law*, typical of hot-electron effects. Inset: EL micrograph of a two-fingers HEMT at $V_{DS} = 30V$ and $V_{GS} = -2V$.

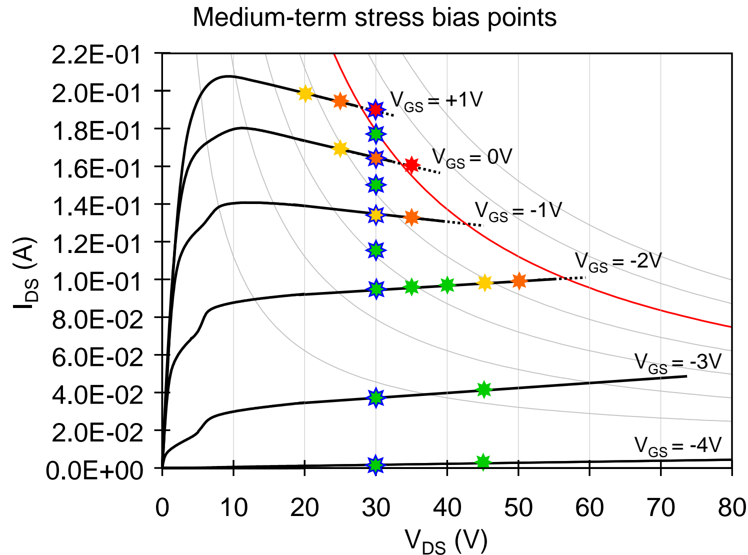


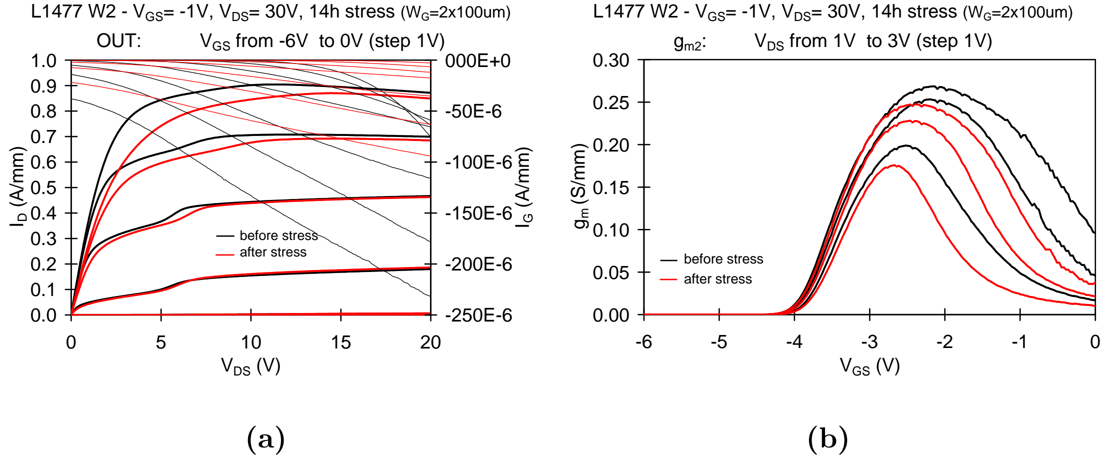
Figure 2.11: Position of all the bias points used for the medium-term 14-hours tests, with respect to the standard output curves of a $2 \times 100\ \mu$m gate-width Task-Force device. In yellow, orange and red, the iso-power points chosen for the first reliability tests. In green, the other points chosen keeping a constant V_{GS} or V_{DS}. With the blue contour, the points useful for the analysis at fixed V_{GS}, where the number of the available stress points along the bell are the maximum ($V_{GS} = 30V$).

luminescence signal is generated by hot electrons and, in our case, it represent a clear signature of hot-electron effects (HEE) taking place at the chosen bias conditions.

All the tests have been performed on the $2 \times 100\ \mu$m gate-width devices only on wafer L1477, due to the slightly bigger degradation observed during the first short reliability tests.

2.4.1 ***Hot-Electrons*** induced failure mechanism

In order to discriminate the accelerating factor for the device degradation (temperature T_j, electric field, hot electrons or a combination), it has been carried out DC tests at constant dissipated power (almost constant T_j) and at different V_{GS} and V_{DS} (different values of electric field or presence of hot electrons), as reported in figure 2.11. More than 50 devices have been submitted to these 14-hours long DC tests.



(a) **(b)**

Figure 2.12: I_D vs. V_{DS} characteristics (a) and transconductance g_m vs. V_{GS} characteristics in knee region (b) of a AlGaN/GaN HEMT transistor before and after a 14-hours ON-state stress at $V_{DS} = 30V$ and $V_{GS} = -1V$.

Tests at the same output power, with a gate voltage from almost pinch-off (-2V) to complete open channel condition (+1V), have shown a non-recoverable decrease of the drain current I_{DS}, in particular in the knee region of the $I_{DS} - V_{DS}$ curves (see figure 2.12 (a)); the I_{DS} degradation corresponds to a decrease of the transconductance without big pinch-off voltage changes (see figure 2.12 (b)). Moreover, I_{DS} decreases exponentially with time, accompanied by an increase of the on-state resistance (see figure 2.13). The gradual increase of the on-resistance is mainly caused by an increase of the drain access resistance R_D, which increases up to 40%, while the maximum source resistance increase is around 10%. At the same time, the EL intensity, the EL/I_D ratio and the gate leakage current (I_G) decrease (see figures 2.14 (a), 2.14 (b) and 2.13 respectively), thus indicating a decrease of the gate-drain electric field. I_{DS} and EL show the same exponential decrease, as reported on figure 2.14 (b), with a slope which depends on the bias condition.

From these first results, it has been possible to understand the common exponential decrease of all the main parameters possibly due to an electric-field reduction especially in the gate-to-drain access region, but it has not been possible to clearly discriminate the effect of the output power, from the electric-field or the

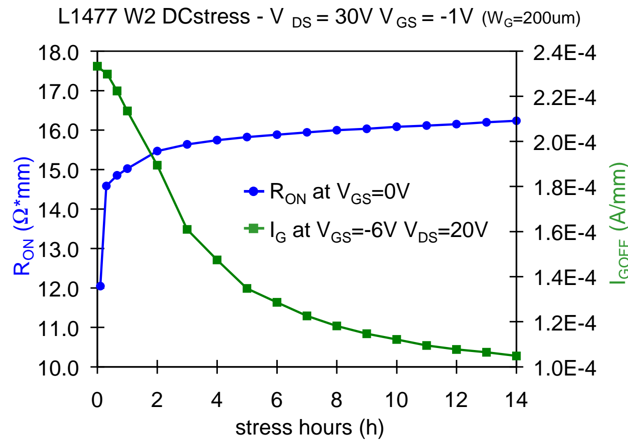


Figure 2.13: Increase of the on-state resistance R_{ON} at $V_{GS} = 0V$ and decrease of the gate leakage I_G at $V_{DS} = 20V$ and $V_{GS} = -6V$ as a function of time, during a 14-hours test at $V_{DS} = 30V$ and $V_{GS} = -1V$.

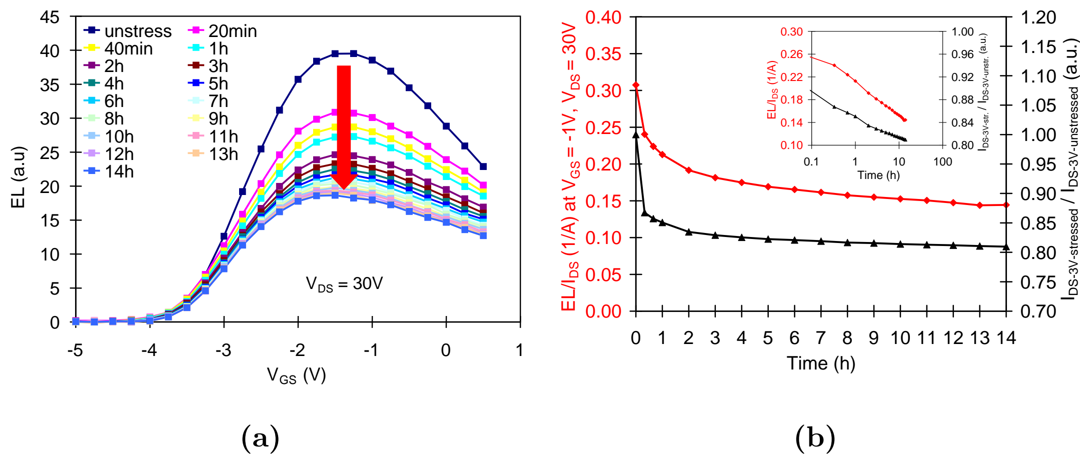
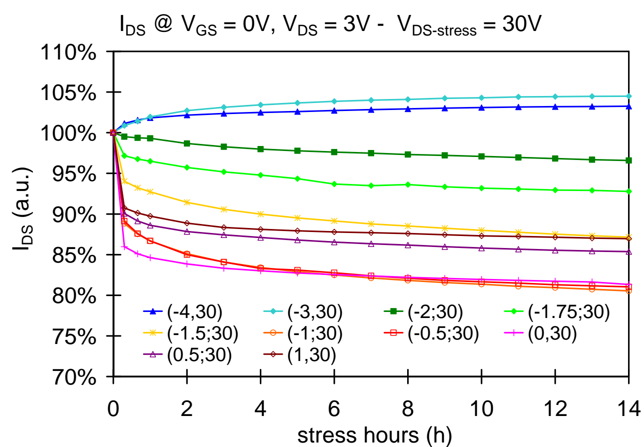


Figure 2.14: (a) EL intensity as a function of V_{GS} measured during the intermediate analysis on a test at $V_{DS} = 30V$ and $V_{GS} = -1V$. For more positive V_{GS}, the decrease in electric field prevails and the EL decreases. (b) Decrease of EL/I_D during test and percentage decrease of drain current measured at $V_{DS} = 3V$ and $V_{GS} = 0V$ as a function of time, during a test at $V_{DS} = 30V$ and $V_{GS} = -1V$. Inset: same quantities as a function of log(t).

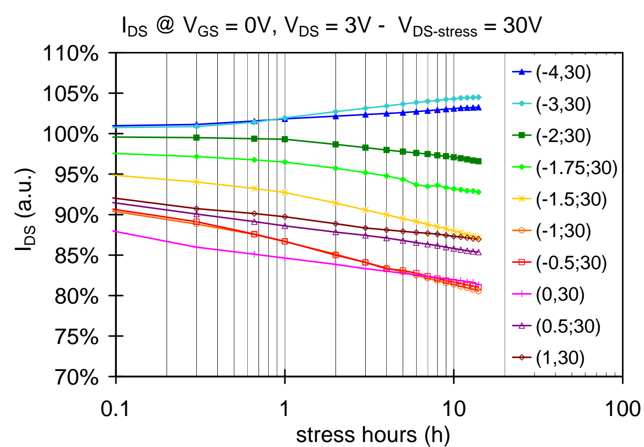
hot electrons. As a consequence, it has been studied the degradation as a function of V_{GS} at constant V_{DS}, showing a particular non-monotonic dependence on V_{GS} as the EL intensity. For V_{GS} values close to pinch-off, it has been observed an increase of the I_{DS} current and a decrease of the on-resistance due to a small negative pinch-off shift, demonstrating again the optimal robustness of this technology against the high electric-fields. As V_{GS} increases, I_{DS} reaches a maximum of the device degradation (around 20%) and then decreases, despite the highest dissipated power and the highest junction temperature for $V_{GS} > 0V$, see figures 2.15 and 2.16 (a). The consistency of the slope of the drain current degradation has been verified even for longer time tests (not shown), showing the same identical slope of the 14-hours tests. The peak of the device degradation almost correspond to the peak of the EL intensity, with a small shift probably due to the simultaneous shift of the threshold voltage that changes, step by step, the reference values. Furthermore, the same tests performed at higher ambient temperatures ($T = 75°C$ and $125°C$) have shown comparable or negligible degradation, see figure 2.16. These results allow to rule out electric field and temperature as possible failure accelerating factors, suggesting a failure mechanism driven by the hot-electron presence inside the channel. Moreover, no current collapse increase has been found, i.e. no new traps has been generated during tests, ruling out defect generation in the semiconductor consequent to the electric field.

Coming back to the previous tests at the same dissipated power, it is possible to see that even in this case the degradation is correlated with the intensity of the EL signal during the tests, and it is not affected by the power dissipation even changing the output power level, see figure 2.17. The output power seems to influence only the first sharp decrease of the drain current, maybe due to a contact damage or a contact annealing after the first seconds of test, and the catastrophic degradation of the gate diodes that destroys the gate-to-channel capability.

As a consequence of the previous described results, a model for this failure mechanism can be proposed. At high V_{DS}, channel hot electrons can achieve an energy sufficient *(i)* to induce generation of electron traps in the access region, or *(ii)* to be injected in the AlGaN, at the SiN/AlGaN interface, or in the GaN buffer,

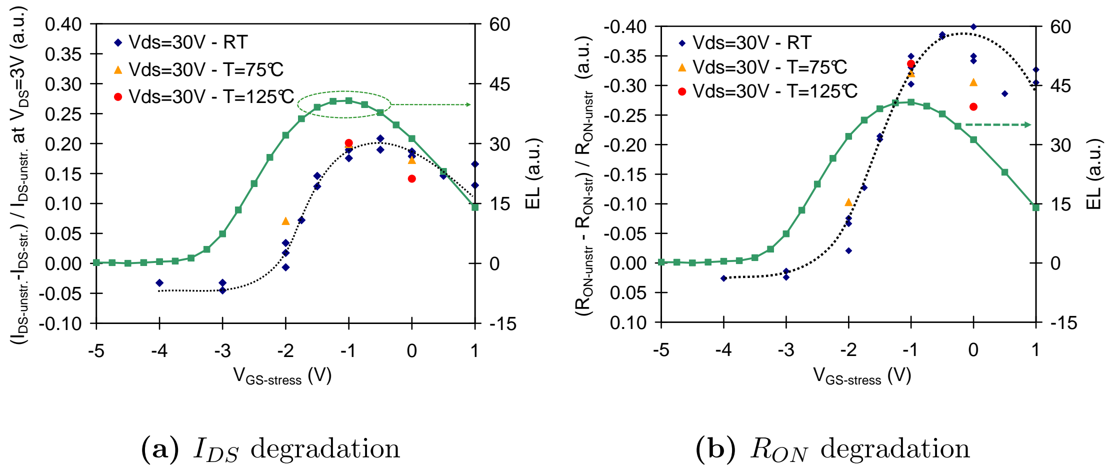


(a)



(b)

Figure 2.15: I_{DS} degradation vs. stress time for various bias points at $V_{DS} = 30V$ as a function of V_{GS}, in linear (a) and in log scale (b).



(a) I_{DS} degradation **(b)** R_{ON} degradation

Figure 2.16: Non-monotonic behaviour of I_{DS} degradation (a) and R_{ON} degradation (b) as a function of V_{GS}, at $V_{DS} = 30V$. Degradation is insensitive to temperature, as reported by the orange and the red points.

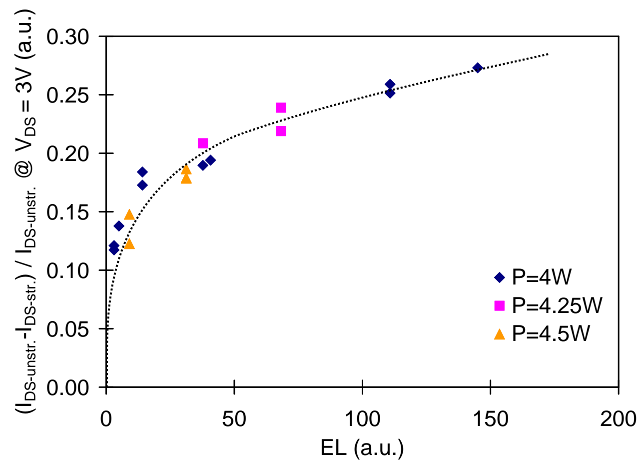


Figure 2.17: Correlation between drain current degradation and EL intensity, for various tests at different values of DC dissipated power.

eventually remaining trapped there; trapped negative charge induces an increase in drain resistance and a decrease in the electric field, leading to a decrease of the I_{DS} current, the EL/I_D, and the I_G leakage.

Afterward, a *Time-to-failure* (TTF) has been defined as the time for a 10% increase of R_{ON}. Figure 2.18 shows the dependence of the logarithm of the TTF on V_{GS}, for various V_{DS}; the shortest TTF roughly corresponds to the EL intensity peak (see figure 2.9), i.e. to the bias point with the most intense hot-electrons effect, thus confirming the proposed mechanism.

In the reported paper, *Dieci et al.* [60] adopted the gate current to evaluate the hot-electron effects (HEE) in GaAs HEMTs and to derive an acceleration law. In this case, the EL intensity has been used as the best index to evaluate and quantify the hot-electron effects. As a results, using the data extracted from the previous tests, a linear relationship has been verified between log(TTF) and 1/EL, see figure 2.19, defining the corresponding acceleration law for hot-electron effects in GaN HEMTs:

$$TTF = A \cdot \left(\frac{1}{EL}\right)^B$$

where A and B are fitting parameters which depend on the robustness of the technology, but also on the adopted failure criteria (10% increase of R_{ON}) and on the EL integration time. In this case, the extracted fitting parameters are A=0.0016 and B=1.433.

An argument that supports the hot-electrons-induced degradation has been shown by *Pantelides et al.* [69], which have tried to physically explain the defects creation or the electron trapping caused by the hot-electron presence inside the active area. Starting from the consideration that electrons, even with several electron volts of energy, can not create a stable point defect in an otherwise perfect crystal, the authors have analyzed the origin of trap generation in terms of H removal from hydrogenated point defects, caused by high energy electrons. First-principles quantum mechanical calculations have been used to derive defect properties with the aim of identifying specific defects and processes that can cause the degradation of GaN-based HEMTs. In author's words, the key result is that, during high-temperature growth under equilibrium conditions, when the Fermi energy is

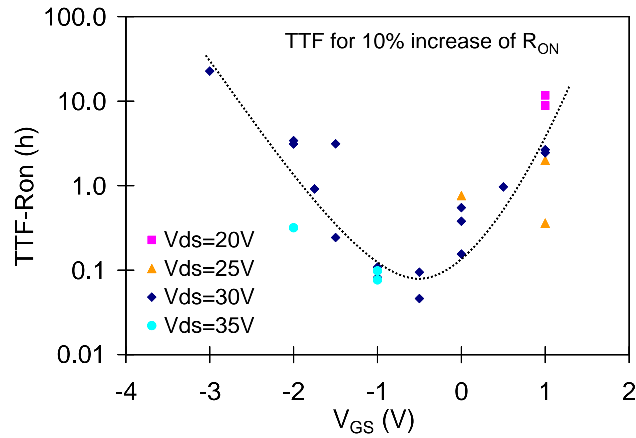


Figure 2.18: Non-monotonic behaviour of logarithm of the time-to-failure (TTF) as a function of V_{GS} for various V_{DS}. TTF has been defined as the time for a 10% increase of R_{ON}.

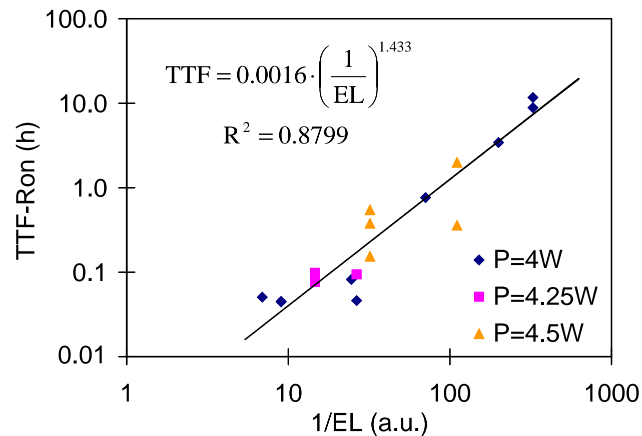


Figure 2.19: Exponential dependence of TTF on 1/EL. The derived acceleration law is $TTF = A \cdot (1/EL)^B$; for these data the fitting parameters A and B are 0.0016 and 1.433 respectively.

in the mid-gap region, neutral triply hydrogenated Ga vacancies (electrically benign) are the dominant defect under either N-rich or Ga-rich growth conditions. Therefore, hot carriers can provide energy to release one, two, or three hydrogen atoms, leaving behind negatively-charged defects, thus giving rise to yellow and blue luminescence (more bare Ga vacancies) and to current and transconductance degradation due to Coulomb scattering. Consistent with previous removal energy calculations, an energy of 2.2 eV is needed to remove a hydrogen from a triply hydrogenated vacancy and place the atom into an H_2 molecule.

2.5 Conclusions and future activities

The reliability evaluation on the Task-Force wafers have shown a significant improvement of the device technology with respect to the previous HEMT technologies in KorriGaN project, and really interesting results regarding the high electric-field robustness and the on-state degradation, which can be important and useful for other future technologies. In particular:

- the engineered layer structure have allowed to mitigate the poor quality of the substrate and of the epitaxial layers, by means of a particular nucleation layer stack that has reduced the defects propagation from the substrate to the active area, making the three wafers really comparable in term of output performances and device reliability;

- the improved device processing, made up by the GaN cap layer and the gate field-plate, has reduced the electric-field intensity and the common gate degradation mechanism always visible in the previous technologies, allowing devices which can withstand drain-to-gate voltages up to 100V without showing any significant performance variation, even if processed on top of substrate or epi defects;

- the on-state medium-term tests on this homogeneous set of devices have demonstrated a failure mechanism due to hot-electron effects (HEE). All tests have shown a non-recoverable degradation of both main electrical parame-

ters and electroluminescence signal (EL); degradation rate has been found to have a strong dependence on the EL signal emitted by the devices during stress, and a negligible dependence on the temperature. Therefore, the degradation mechanism has been ascribed to defect generation and electron trapping induced by hot electrons in the gate-drain access region.

- by adopting EL intensity as a measure of the stress accelerating factor, it has been developed a methodology for the evaluation of HEE, and it has been derived one of the first acceleration law for GaN-HEMT hot-electron degradation, similar to the one presented in [60] for GaAs devices.

Nevertheless, few elements of the explained theory are still not completely clear, like the threshold voltage influence on the device degradation or the degradation dependence on the dissipated power. For these reasons, it is possible to suggest other future activities to further confirm the obtained results and the extracted acceleration law. In particular, it can be tested the effectiveness of the acceleration law for all the bias points characterized by a low drain current and an extremely high electric-field (close to the pinch-off condition at high V_{DS}), or the real effect of the dissipated power extracting the junction temperature behaviour at the different bias points.

Chapter 3

Reliability assessment of GaN HEMTs in ESA project

In this chapter it will be summarized the main activities performed within the on-going research collaboration with the European Space Agency (ESA), with topic *"GaN HEMT Reliability Assessment and Identification of Degradation Mechanisms"*, and the main results which have been obtained up to now. The target of the project is the identification of the main failure mechanisms that reduce the required performances on devices designed for satellite or in general space applications. The preliminary tests aimed at identifying the extreme operative conditions where devices can still work, in term of temperature stability and maximum drain voltages, to allow the setting-up of a significant long-term reliability campaign, on both DC and RF conditions, which will give a meaningful evaluation of the device reliability in the real application. Devices subjected of these reliability tests have been AlGaN/GaN HEMTs grown with a stable and robust technology defined during the last years of $GREAT^2$ project, a project aimed at establishing a reliable and space compatible GaN-HEMT technology ready for ESA space evaluation at the end of the project.

The activity has been accomplished inside both the microelectronic laboratories of the University of Padova and inside the *ESA-ESTEC* research center in the Netherlands, for 5 cumulative months of placement. As a consequence, the following results refer to the work carried out inside the two laboratories exploiting the

facilities of both part for a common project target. At the moment the activity is still in progress, especially regarding the long-term DC reliability tests and the storage tests. For this reason, this chapter will report the most interesting results reached up to now, concerning the high-voltage capabilities and the high temperature stability extracted from the short-term tests, and concerning the intermediate available results regarding the long-term stability of the space designed GaN devices. As on the previous chapter, the reliability tests have been adapted in order to better understand the failure mechanisms that are mainly affecting the device performances, especially in high-voltage conditions, improving the knowledge on the degradation mechanisms, and on the related accelerating factors, that reduce the device properties or that cause catastrophic failures in this GaN technology.

3.1 Preliminary characterization

At the beginning of each reliability campaign, a preliminary set of measurements need to be performed in order to identify and quantify the main performances of the technology, and to assess the most important parameters that have to be checked and followed during the reliability tests. Due to measurements carried out on both research laboratories, and due to the necessity of a correct data exchange without any misunderstanding, part of the work has been devoted to better understand the differences of the two setups used for the data extraction, and to redefine few measurement details essential for a correct data exchange, creating a standardization of the measurement procedure useful for all the following reliability analysis.

The preliminary measurements consisted of the standard DC and dynamic measurements:

- the DC measurements, to extract the main static performance parameters as the saturation drain current, the transconductance peak, the threshold voltage and the leakage currents;
- the dynamic measurements, to extract the dynamic behaviour and to identify and quantify the trapping effects that reduce the device's dynamic performances.

These preliminary analysis has been performed on the standard $GREAT^2$ Core PCM processed by UMS (United Monolithic Semiconductors), the common PCM used by all the partners of the $GREAT^2$ project. This standard PCM consists of several test structures for the evaluation of the main electrical parameters of the AlGaN/GaN architecture, and of 6 devices with different layout structures, that have been used for the characterization analysis and for the following reliability activities (see figure 3.1).

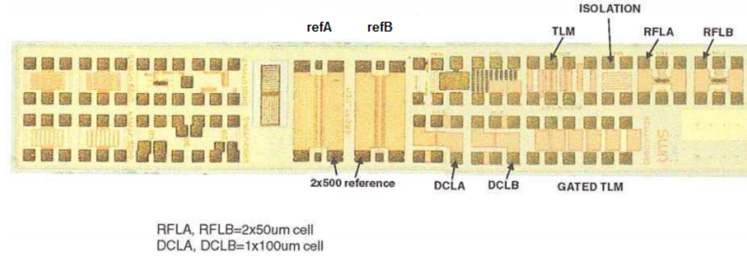


Figure 3.1: Structure of the standard UMS Core PCM.

The 6 devices can be divided in 3 groups with different layout characteristics and, as a consequence, with different operative purposes:

- DCL devices (DCLA and DCLB): 100 μm single-finger devices, with a DC layout, suitable for L-band operation (1-2 GHz);
- RFL devices (RFLA and RFLB): $2 \times 50\,\mu m$ double-finger devices, with a RF layout, suitable for L-band operation;
- ref devices (refA and refB): $2 \times 500\,\mu m$ bigger devices, with a RF layout, as reference.

All devices exhibit the same small Γ gate, with a gate-length of 0.5 μm, but only -A devices have been processed with another source-connected field-plate that ends in the middle of the gate-drain region, in order to reduce the gate-drain parasitic capacitance and to improve the high-frequency performances of these devices, especially regarding the cut-off frequency f_{τ}.

From the DC characterizations, tested devices have shown a very similar behaviour, with a rather low drain saturation current at $V_{GS} = 0V$ (0.28 A/mm for 100 μm devices and 0.22 A/mm for 1 mm devices) and a low transconductance

peak (0.22 S/mm for 100 μm devices and 0.19 S/mm for 1 mm devices), compared to standard AlGaN/GaN HEMT devices. On the contrary, samples have shown low leakage currents ($\sim$ 20 μA/mm) with a very good pinch-off behaviour. Threshold voltage is in the -2/-1.5V range for all tested devices. The presence of the source-connected field-plate have not significantly changed the main DC performances.

From the dynamic measurements, the dynamic behaviour has been quite uniform, but affected by important trapping effects at the high V_{DG} quiescent point used for the dynamic evaluation ($V_G = -7V$ and $V_D = 50V$). The observed current collapse effect has been caused by a big right threshold voltage shift followed by a small transconductance reduction, with final Slump Ratio values around 50-60% in the knee region and around 60% in saturation region.

The comparison of the DC data extracted in both laboratories from the same samples, have allowed to highlight the different influence of few parasitic effects depending on the instrument setup. For example the influence of the kink effect on the DC measurements, important in one case and negligible in the other-one, has suggested a change of the parameters typically used for the devices comparison, shifting the V_{DS} extraction point completely above the kink-region, to avoid any inconsistency on the data sharing. From the dynamic comparison, the use of a high V_{DG} quiescent point for the trapped curves extraction ($V_G = -7V$ and $V_D = 50V$) has allowed to better understand the slow parasitic effect that plagues this device technology, defining the best measurement procedure and the best Slump Ratio's extraction point independently on the different used setup.

This first activity has been necessary for a correct data exchange, avoiding any inconsistency only due to the different used setup. In particular it has been fundamental on the following reliability assessment, giving the possibility of a simple and direct comparison between results obtained in ESA laboratories with results obtained in Padova labs.

3.2 Short-term reliability tests

The first short-term reliability activity has been performed on the small 100 μm gate-width devices (mainly on DCL devices), with the objective of understanding the drain voltage robustness of these devices in different bias conditions, in order to gain a complete view of the useful operating area, and to define the best testing conditions for the long-term reliability evaluation. For this first reliability analysis, three-terminal step-stress tests have been used: devices have been biased at a fixed gate bias, increasing the drain voltage from 20V up to failure, step by step; 1-hour long steps, with 10 minutes of relaxation time after each stress phase (to avoid fast trapping phenomena or stress induced self-heating effects on the following characterization measurements).

Three main test conditions have been used, to investigate both the robustness in pinch-off condition, looking at the possible gate-degradation effects (as reported on the previous chapter), and the robustness in ON-state condition, investigating which factor mainly causes the device degradation or the final device's failure. In particular:

- step-stress tests in **deep-OFF state** condition ($V_{GS} = -7V \ll V_{TH}$), to test the OFF-state robustness for longer times compared to the faster breakdown tests;
- step-stress tests in **semi ON-state** condition (1% - 2% and 5% I_{DS} at $V_{DS} = 15V$), to test the reliability of these devices at low-current levels but in high voltage conditions;
- step-stress tests in **ON-state** condition ($V_{GS} = 0V$), to test the reliability in high-power conditions.

The main purpose and the great interest in the semi ON-state stress comes from the practical application of these devices, defined by ESA targets as RF amplifiers in class AB condition, with a $V_{DD} \simeq 50V$ and a I_{DS} bias point of 50 mA/mm. In fact, working as a RF amplifier in class AB condition, the ideal load-line where the device should work is the green line of the following diagram (see figure 3.2),

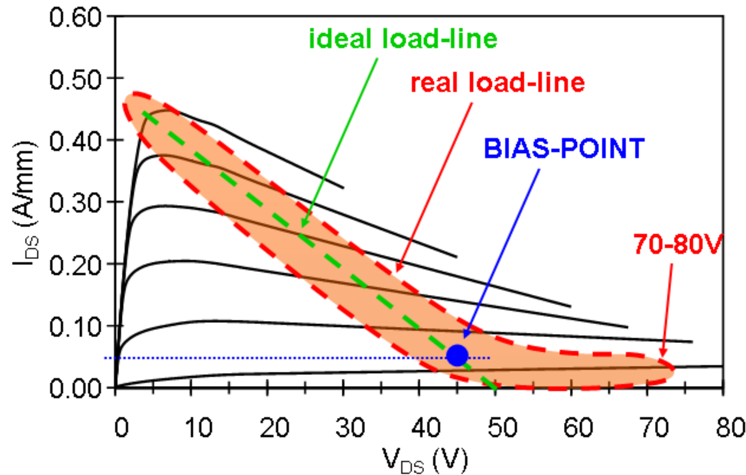
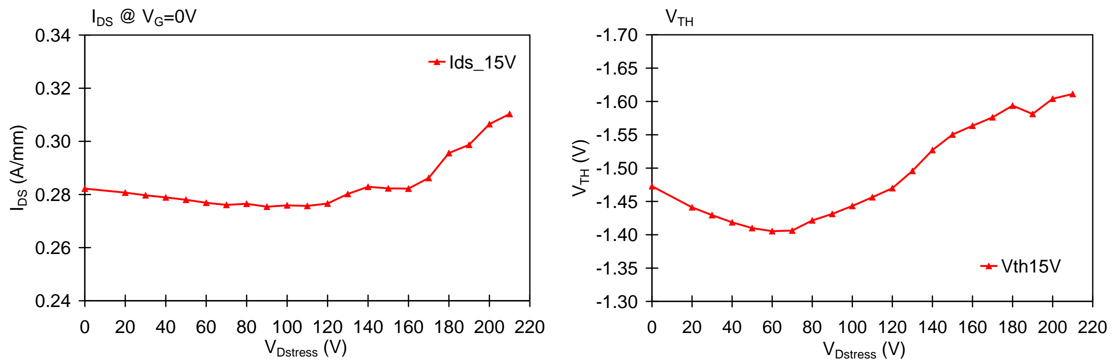


Figure 3.2: Graphical representation of the real operation of ESA devices, as RF amplifiers in class AB condition: in green the ideal load-line; in red a schematic representation of the real dynamic load-line.

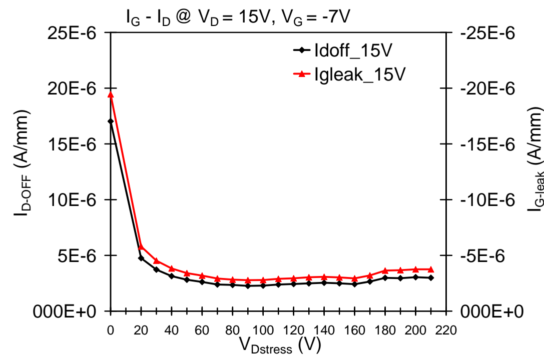
going from the pinch-off condition at high V_{DS}, to the knee region at low V_{DS} and high drain current. Actually, the simulated dynamic load-line is different, and mainly extended on the region close to pinch-off, toward higher drain voltages (70-80V, see red curve in figure 3.2). For this reason, it has been decided to test the reliability of these devices below the I_{DS} bias point but at higher drain voltages, to understand if, in this operative condition, the robustness and the breakdown of the tested devices is similar to the OFF-state breakdown or significantly reduced.

Preliminary breakdown , available from $GREAT^2$ tests on the same devices, showed the three-terminal OFF-state breakdown around 220-230V. For this reason, all the tests and the instrument setup have been adapted in order to handle this voltage levels, not typical for a standard parameter analyzer system, from the hardware, the software and the safety point of view.

Moreover, due to the intrinsic destructive nature of the step-stress test, and due to the limited availability of devices to test, it has not been possible to statistically verify the reliability behaviour of the ESA devices. Nevertheless, due to the really stable and homogeneous device processing, many interesting results have been gathered even from the limited number of tested devices, and important details about the device failure mechanisms can be identified.



(a) I_{DS} at $V_G = 0V$ variation **(b)** V_{TH} variation

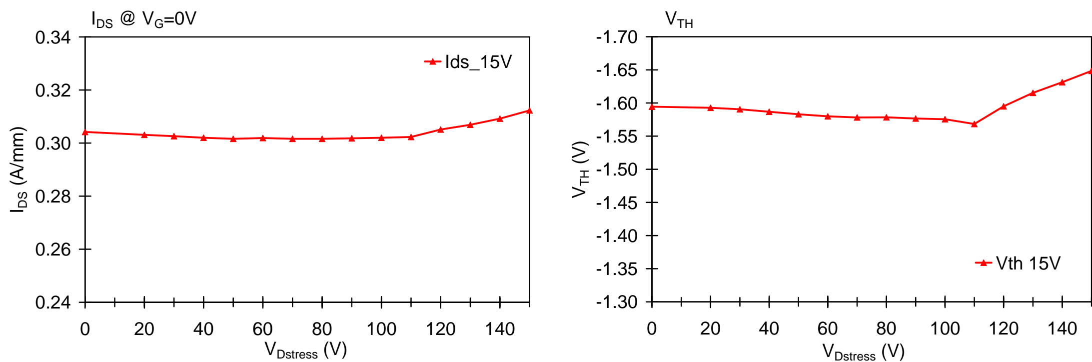


(c) Off-state leakages variation

Figure 3.3: Electrical parameters evolution during the 1-hour *deep OFF-state* step-stress on a typical device.

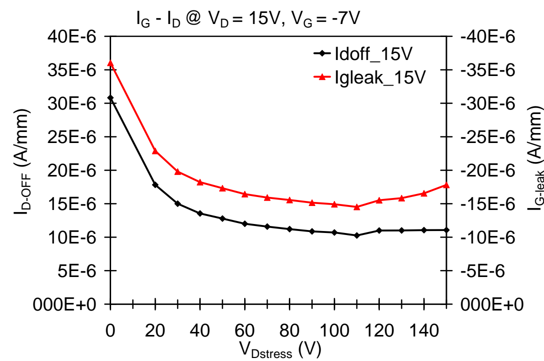
As reported in figure 3.3, during the *OFF-state step-stress*, devices have shown a quite stable behaviour of the leakage current values, with only an initial decrease possibly due to charge trapping (consistent with the R_{ON} increase during the first steps) or to a simple burn-in effect during the first seconds of stress. Consistent with the previous breakdown values, around 220-230V devices failed completely, creating a short mainly on the gate-drain region (from visible inspection after device failure). During the previous steps, it can only be observed a small increase of the leakage at V_{DS}=15V around 150V, but not in HV drain condition ($V_{GS} = -7V$ and $V_{DS} = 50V$), ruing out the presence of any gate-degradation effect. The other performance parameters are only affected by a strange variation of the threshold voltage (V_{TH}): during the first steps (up to 70-80V) the V_{TH} shifts on the positive direction, slightly reducing the I_{DS} and increasing the R_{ON}; from 130-150V, the V_{TH} changes its behaviour starting to shift on the negative direction, this time increasing the I_{DS} and decreasing the R_{ON}. The onset for the negative shift of the threshold voltage is well correlated to the increase of the drain current during the stress, as reported in figure 3.6 (a) (possible channel opening at high V_{DS} even in really deep pinch-off conditions). Looking at the diode characteristics, it can only be observed a small negative shift of the forward characteristics starting more or less from the same point. The same stress effects have been observed with shorter (12 minutes) and longer (2.5 hours) time steps, with only small differences on the trapping behaviour. No reliability or parameter evolution differences have been noticed between devices with the source-terminated FP and device without this FP.

From the *semi ON-state step stress* at 1%, 2% and 5% of the drain current, devices have shown a quite similar behaviour compared to the OFF-state stress, consistent on all tested samples and in all testing conditions, exhibiting only a general smaller variation of all the electrical performances, as reported in figure 3.4. Stable behaviour of the leakage current values even in HV condition (at $V_{GS} = -7V$ and $V_{DS} = 50V$), with only an initial decrease possibly due to charge trapping (consistent with the R_{ON} increase during the first steps) or to a simple burn-in effect during the first seconds of stress. The most significant difference



(a) I_{DS} at $V_G = 0V$ variation

(b) V_{TH} variation



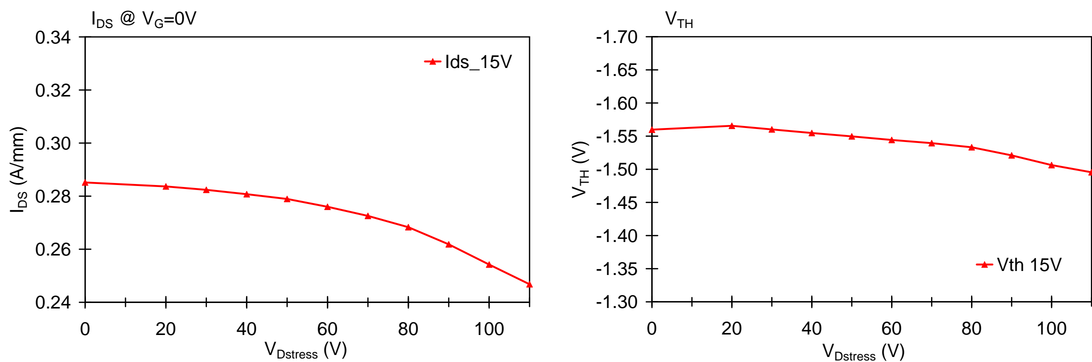
(c) Off-state leakages variation

Figure 3.4: Electrical parameters evolution during the 1-hour *semi ON-state* step-stress on a typical device.

comes from the big reduction of the failure voltgae, here located around 150-160V, with more or less the same permanent degradation happening on the gate-drain region (from visible check after device failure). During the previous steps, it can be observed a very small increase of the leakages at V_{DS}=15V around 110V (no gate-degradation effects). As on the previous stress, the threshold voltage shows the same shifting behaviour (reduced in intensity), with an initial small positive shift, followed by a negative shift starting from 110-120V. Even on these tests, the onset of the negative shift of the threshold voltage, of the small leakage increase, and of the very small negative shift of the diode forward characteristic, are well correlated to the increase of the drain current during the stress, as reported in figure 3.6 (b) (possible increase of the channel current at high V_{DS}). The same degradation effects have been observed with shorter time steps (10 minutes), useful for the following failure mechanism analysis. Even on these tests, no reliability or parameter evolution differences have been observed between devices with or without the source-terminated FP.

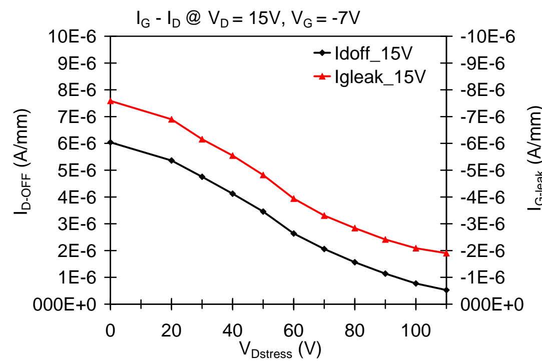
During the *ON-state step stress*, devices have shown a more pronounced degradation of the electrical parameters, maybe due to the influence of the higher dissipated power (see figure 3.5). As on the previous stress, no increase of the leakage currents can be observed, but only a gradual step by step decrease. Moreover, the breakdown voltage further decreases to 120-140V, causing even on this case a permanent failure of the gate diodes. Concerning the threshold voltage, it is not possible to see the same double-trend as on the previous tests, maybe due to the higher stress current or maybe due to the smaller failure voltage. It can only be observed a small right V_{TH} shift especially during the last steps. This variation can partially explain the 10-15% degradation of the drain current, mainly in the knee-region, but it can not explain the decrease of the tranconductance (5%). In this bias condition, the failure seems to be more influenced by the higher dissipated power, but it can not be excluded a possible contribution of the high-electric field or of the highly energetic carriers.

At the end of these preliminary analysis, few important results have been observed, underlining the very good OFF-state robustness of this technology with



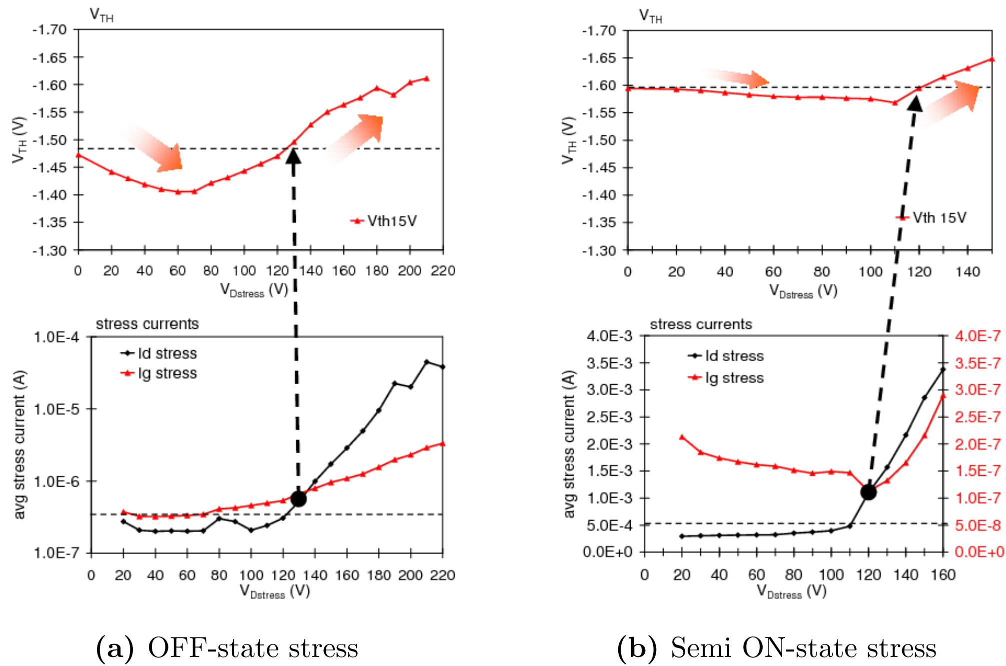
(a) I_{DS} at $V_G = 0V$ variation

(b) V_{TH} variation



(c) Off-state leakages variation

Figure 3.5: Electrical parameters evolution during the 1-hour *ON-state* step-stress on a typical device.



(a) OFF-state stress

(b) Semi ON-state stress

Figure 3.6: Correlation between the threshold voltage variation (upper diagrams) and the average drain stress current (lower diagrams), during the 1-hour step-stress tests.

a breakdown voltage around 220-230V even for longer stress times, that does not show any clear sign of gate-edge degradations (at least with this stress duration), but that suffers of an important robustness reduction just increasing a little bit the channel current. Only during the ON-state tests, the failure seems to be mainly driven by the higher device's dissipated power. Nevertheless, even considering the high internal electric-field or the high power dissipation, devices have not suffered very pronounced performance degradations (especially in low current tests), indicating a really high stability of this technology at voltages lower than the failure. No reliability differences have been observed between devices with or without the source-connected FP, suggesting the limited influence on the reliability behaviour of this processing improvement.

From these results, important information about the device extreme operating conditions have been understood, but it is still unclear what failure mechanism is leading the device failure, and if it is somehow correlated with all the three different bias condition's failures. For this reason, further tests have been carried out in

semi ON-state condition, the most interesting bias point for the final device application, investigating the temperature behaviour of the failure mechanism and the position of the failure points on the tested device (by means of emission microscopy measurements).

3.2.1 Failure mechanisms in High-Voltage step-stress tests

Semi ON-state stress have been repeated under different test temperatures, to investigate the temperature behaviour of the failure mechanism. The test temperature has been kept all along the stress test, including the relaxation time and the characterization phase, due to a possible real application of the tested devices in high temperature conditions. Moreover, the repeatability of the DC characterization at high temperatures has been tested before the stress, to avoid any degradation only caused by the high-power intermediate DC measurements. As on the previous room temperature tests (RT tests), these step-stress have been performed on the small 100 μm gate-width devices, tested at 1% and 5% I_{DS} conditions, and at three different test temperatures: 75°C, 115°C and 150°C.

As reported in figure 3.7, the high temperature semi ON-state step-stress have shown very similar results compared to the RT tests, but with a general reduction of all the parameter variations, possibly due to a lower trapping effect induced by the higher ambient temperature. The two I_{DS} bias conditions have shown more or less the same results, sign of a common stress evolution and stress failure. As on the RT tests, these devices have shown a quite stable behaviour of the leakage current values, with only an initial decrease possibly due to charge trapping (less pronounced than RT tests), and a very limited variation of all the performance parameters. The only difference comes from the breakdown voltage values, that have shown an sufficiently uniform increase correlated with the increase of the test temperature: from a failure voltage of 150-160V for RT tests to a failure voltage of 190-200V for 150°C tests (see figure 3.8). The positive temperature correlation suggests an avalanche induced failure mechanism, maybe due to impact ionization inside the channel. In fact, the mobility reduction induced by the higher test temperature requests higher electron energy and, consequently, higher drain-to-

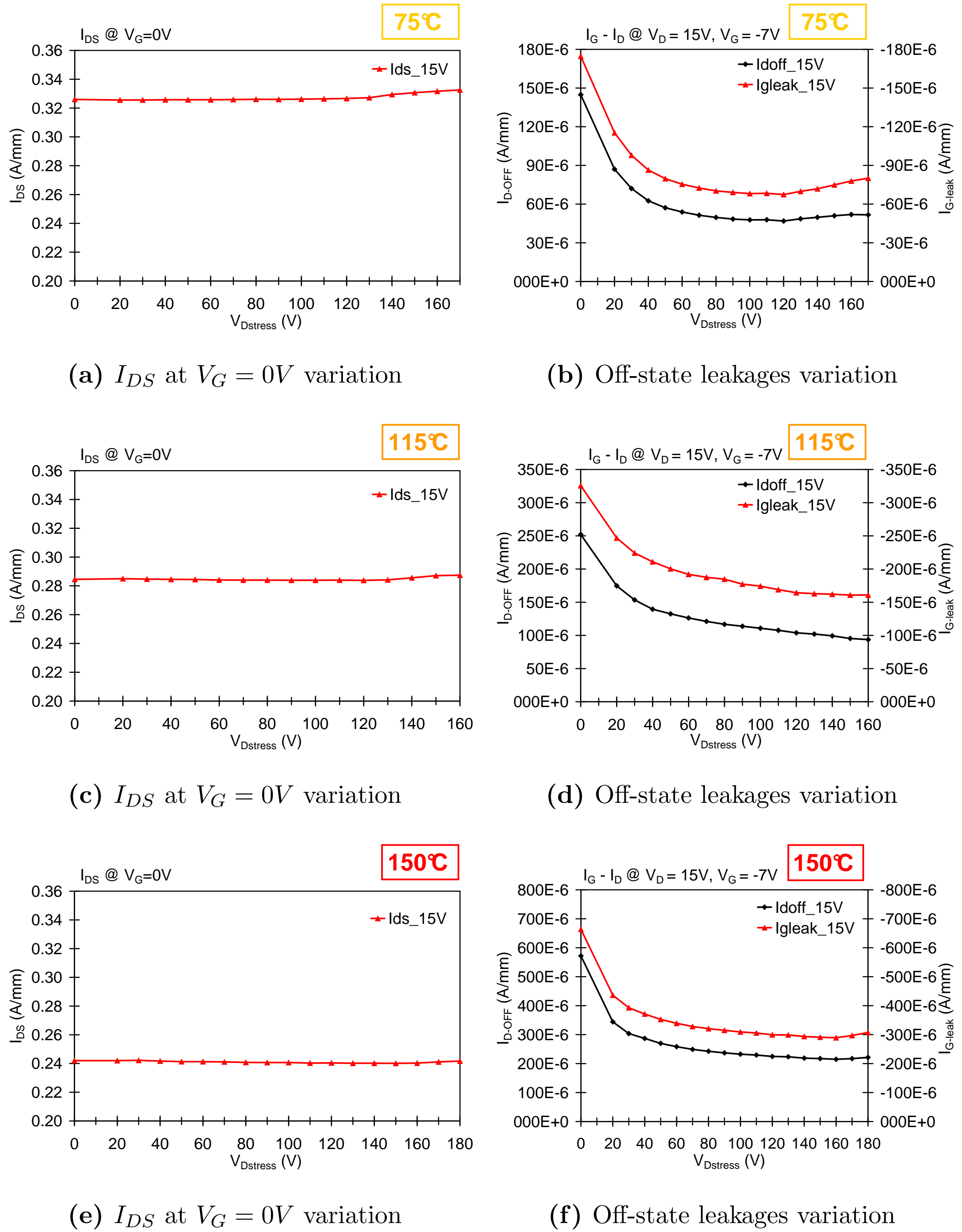
gate voltages to start the impact ionization phenomenon, explaining the positive shift of the breakdown. On the contrary, during a surface breakdown mechanism, the transport by means of the hopping conduction through surface states would be significantly enhanced by the temperature increase, hence showing a negative temperature dependence.

Only one single test has been performed in deep OFF-state condition at 150°C. And even in this case, the test has shown a remarkable increase of the breakdown voltage, from 220V at RT to 260V at 150°C, despite the different observed results in term of diode stability and main performance degradation.

In the following diagrams (see figure 3.8), it can be noticed the increase of the breakdown voltage with temperature on the semi ON-state stress. Due to the very low statistics and to the different approaches used for the device testing, there is still a big spread of the failure voltages. Nevertheless, increasing the test temperature, it is sufficiently visible a positive trend of the breakdown voltage, which suggests an avalanche driven failure mechanism. At this stage, due to the increase of the breakdown voltage even on the deep OFF-state test at 150°C, it is not clear if the failure mechanisms of the two stress are the same, but an avalanche failure mechanism induced by the channel impact ionization could explain both the temperature dependence of the breakdown and also the big reduction of the breakdown voltage from the OFF-state to the semi ON-state tests. The latter is explained by the fact that the increase of the carrier concentration needs less carrier energy (i.e. electric-field or drain voltage) to begin the impact ionization phenomena.

Furthermore, in figure 3.9 is reported the drain stress current just before the device failure, in particular for semi ON-state stress, for all test temperatures. From this diagram it is possible to notice an interesting linear correlation between the failure drain current and the temperature, suggesting the important role of the drain current (and of the dissipated power as well) on the final breakdown.

Concerning the particular threshold voltage (V_{TH}) shift seen on the RT tests, with a first positive trend followed by a negative trend (starting from the increase of the drain stress current), it is still possible to notice that the negative shift of



(a) I_{DS} at $V_G = 0V$ variation

(b) Off-state leakages variation

(c) I_{DS} at $V_G = 0V$ variation

(d) Off-state leakages variation

(e) I_{DS} at $V_G = 0V$ variation

(f) Off-state leakages variation

Figure 3.7: Electrical parameters evolution during the 1-hour semi ON-state step-stress at different test temperatures.

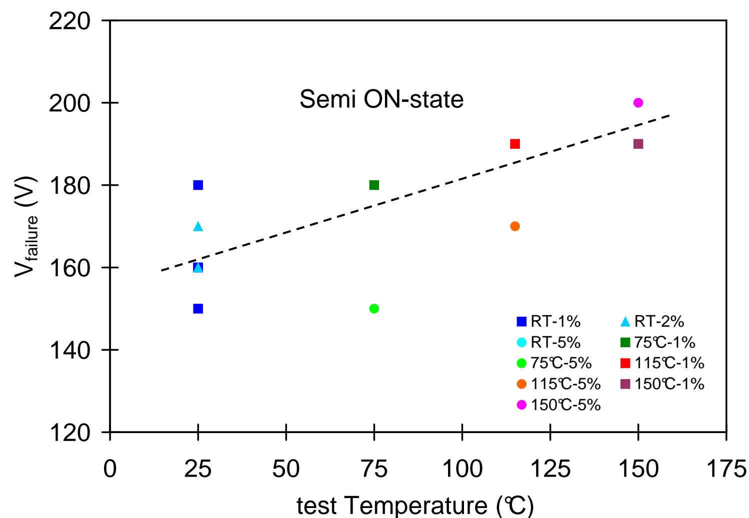


Figure 3.8: Failure voltage vs. stress temperature in the semi ON-state step-stress tests.

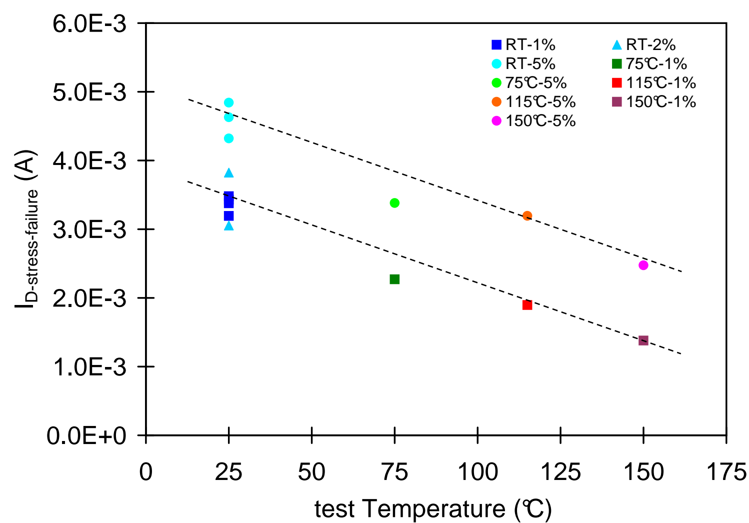


Figure 3.9: Correlation between the drain stress current just before the device failure and the test temperature, in the semi ON-state step-stress tests.

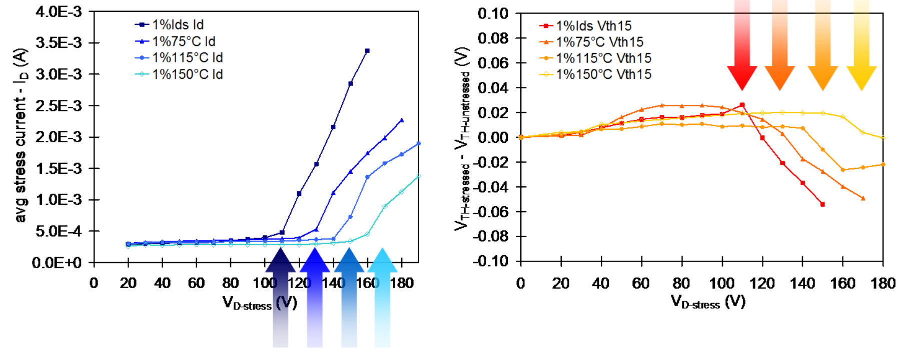


Figure 3.10: Correlation between the threshold voltage variation (right) and the average drain stress current (left), during the 1-hour step-stress at different test temperatures.

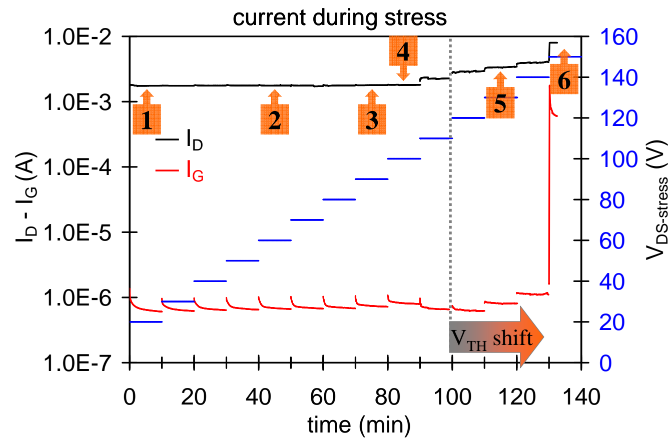
the V_{TH} starts more or less when the drain stress current starts to raise, despite the very small variation of the threshold during the high temperature stress. In particular, due to the increase of the V_{DS} at which the drain stress current starts to raise, it still is possible to identify a similar trend even on the V_{TH} negative-shift onset, as reported in figure 3.10. This particular behaviour will become really interesting on the following tests under the emission microscope.

To improve the understanding on this failure mechanism, few step-stress tests have been performed on an emission microscope probe-station, equipped with a cooled CCD camera in order to capture the photons emitted by the device under test. Due to the different probe station, and to the absence of a remote and automatic control of the camera, the duration of the stress step has been decreased to 10 minutes, with 10 minutes relaxation time. In spite of the different measurement setup and the reduced step duration, these tests have shown very similar results compared to the standard step-stress tests (1h step). For this reason, it is possible to correlate the emission images taken during these short tests with all the other 1-hour tests, to have a more deep understanding on the device behaviour along the stress and at the final failure. Due to the very limited increase of the leakages during the stress, suggesting a negligible gate-edge degradation, it has been decided to collect the emission images just during the stress, to avoid further changes of the stress setup (for example, collecting the EL images at a fixed bias after each step of stress, typical of other less robust technologies).

Looking at the emission images taken during the stress (see figure 3.11), during the first steps the device under tests is characterized by an homogeneous emission at the drain edge of the gate, as usually happens on AlGaN/GaN HEMT devices, together with few preferential paths where the current flows (emission spots clearly visible from the step at V_{DS} = 60-70V). From the step at V_{DS} = 100V, it is possible to notice a strange effect: the emission starts to shift from the gate side of the device to the drain side, not necessarily following the same current hot spots observed at the gate side. This change of the emission behaviour is quite close to the threshold voltage onset; thus, for this reason, the two effects could be correlated. After that V_{DS} value, the emission at the drain ohmic contact further increases, showing an homogeneous emission superimposed to few "hot" emission points where the current, or the hot-electrons, seems to focus. At step 150V, the device failed showing a physical damage located at the same positions of few gate-drain "hot spots", as previously reported. From this combined measurements, it is possible to confirm that the failure happens only on few weak points where the currents is focusing, or where few defects are located, but maybe not only on the gate-side of the tested device. This images suggests a possible failure role of the ohmic contact that has not been considered up to now.

The same peculiar emission behaviour has been observed during the short version of the OFF-state step-stress performed under the emission microscope (10 minutes step; see figure 3.12). At the beginning of the test, negligible light is emitted by the active area, due to the very small carrier density; as the drain voltage increases, one or few spots start to emit especially when the gate current starts to be noisy, highlighting that the current is mainly focused on that points (see step at 70V in figure 3.12); during steps from 130V to 150V, quite close to the threshold voltage onset, few other spots appear, and the emission starts to shift from gate side to drain side of the device; from step at 160V, it is clearly visible a drain-side emission focused on few "hot spots", not completely on the same position of the gate hot spots (see step at 200V in 3.12).

At this stage, considering all the results obtained from the short-term reliability analysis, many information about the device robustness and the device failure have



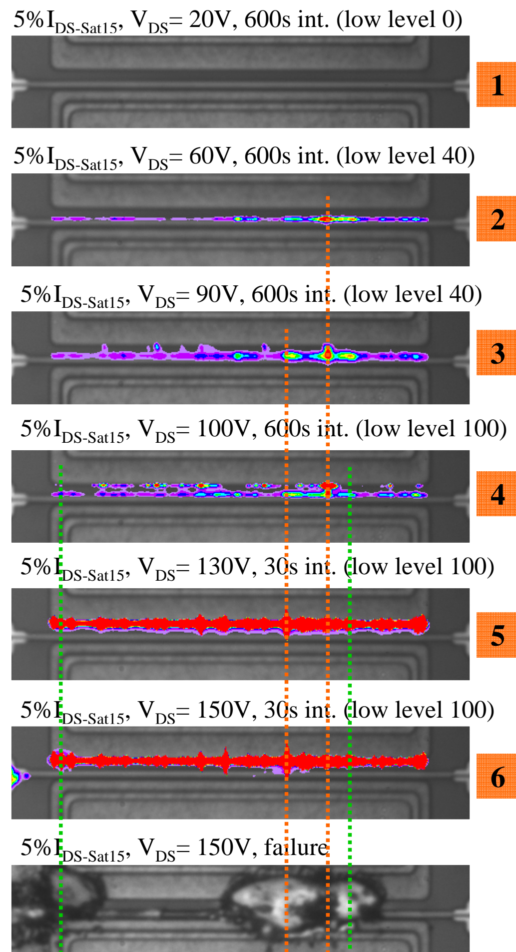


Figure 3.11: Average stress currents (up) and corresponding false-colors emission microscope images (bottom) collected during a 10-minutes semi ON-state step-stress. The orange lines follow the position of the gate-side spots; the green lines follow the position of the drain-side spots, underlining the not complete correspondence.

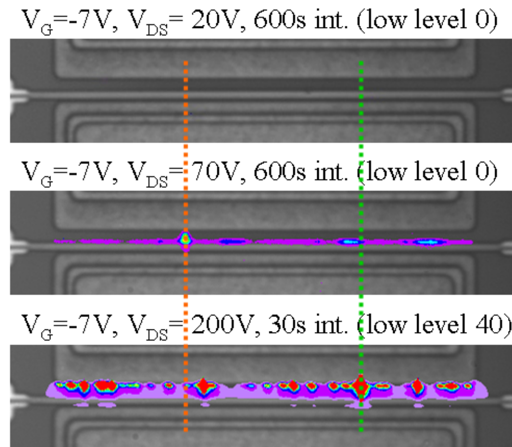


Figure 3.12: Three representative false-colors emission microscope images taken during a 10-minutes OFF-state step-stress. The orange lines follow the position of the gate-side spots; the green lines follow the position of the drain-side spots.

been gathered. It has been verified the very good OFF-state robustness of this technology, with a really stable behaviour of all the electrical parameters up to the final catastrophic failure, around 220V, with a negligible influence of the source-connected field-plate. The semi ON and the ON-state tests have underlined a big reduction of the failure voltage, with a noticeable performance degradations only on the high-power tests. The positive temperature correlation of the breakdown voltage have suggested an impact-ionization induced failure mechanism, that can furthermore explain the failure voltage reduction of the mid-current tests with respect to the zero-current tests. From the emission microscopy measurements carried out during the stress, the shift of the emission profile from the gate-side to the drain-side can suggest a possible failure role of the ohmic contact that has not been considered up to now.

This effect has been reported on the literature only a couple of times, suggesting the quite strange behaviour of the tested devices, or the rather new application of the emission microscope techniques to high-power GaN devices. In particular *Ohno et al.* [70] have explained the shift of the emission profile from the gate-edge to the drain as a strong virtual-gate effect, that completely depletes the channel below the drain access region causing a large potential drop at the drain ohmic contact. In this paper, the final breakdown has been correlated to the impact ionization in

the channel, which has been triggered by electrons tunneling from the gate to the channel.

On the previously described step-stress tests, the failure mechanism seems to be quite similar, due to the same positive correlation with the test temperature, but the comparison between the device leakage current and the breakdown voltage has not shown the expected trend. However, in this case the failure seems to start from one or few “weak points” where the current or, more exactly, the hot electrons are focused. Consequently, after a critical V_{DS} value, the high electron-energy focused on that points can induce the avalanche that breaks the device.

Despite these assumptions, further analysis need to be done to better understand the role of few other elements, like the temperature, the stress duration, or the hot-electron presence in a region, like the ohmic contact, not so considered during the reliability studies. Moreover, it has not been verified the presence of the virtual-gate effect, studying for example the transient behaviour of the drain-side emission, or the electrical parameter changes due to a parasitic charge accumulation in the drain access region (due to the long relaxation time and to threshold voltage variation that can false the exact evaluation of the drain access resistance).

3.3 Long-term reliability tests

Following the short-term reliability tests and the very meaningful information coming out from these analysis, several long-term tests have been started and are still in progress, to investigate the long term performance variations of the ESA GaN-HEMT devices. In particular two type of tests are in progress:

- **storage tests** at different test temperatures, 300°C, 350°C and 375°C, to analyze the extreme temperatures that the device can withstand, and the variation of the internal static and dynamic performances only caused by the high temperature presence;

- **DC life-tests**, an accelerated life-test at three different bias conditions (ON, semi ON and OFF-state) but at the same estimated device junction temperature T_j, to investigate the effect of the combined presence of high-temperature

and high-voltage along the time, and to understand which condition or which element limits the device reliability on long-term tests.

All these tests have the objective of reaching 1000 hours test, stopped at regular logarithmic intervals (starting from 1 hour) and at the failure criteria. This criteria has been defined as the composition of three events: 20% decrease of the saturation drain current I_{DSS}, 20% decrease of the transconductance peak g_{mMAX} and an increase of 10 times of the leakage currents. Each of these events is actually a failure criteria, keeping the threshold voltage and the diode characteristics under control at each measurement step. As previously stated, the tests are still ongoing, and the following results will refer to intermediate data available up to now. Nevertheless, from these data it is possible to understand the temperature limit of this technology and important characteristics regarding the long-term robustness.

3.3.1 High temperature storage tests

The goal of the storage tests is to understand the highest temperature that this technology can withstand without showing any variation of the device performances, and how these performances degrades along the time at different temperatures. For this reason, the test investigates the stability of the contacts and of the heterostructure submitted only to a high junction temperature T_j, without the carriers flowing or the high electric-field presence, with the purpose of using the measured temperature limit as a junction temperature limit for the accelerated life-tests. Actually, it is typically difficult to directly correlate the maximum stable storage temperature with the maximum stable T_j on a biased device, but on this quite robust technology, useful indication can be gathered.

From the stable results obtained from few preliminary tests, it has been decided to use really high storage temperatures, higher than 250°C. For this reason, three temperatures have been used: 300°C, 350°C and 375°C. The interruption of the high-temperature tests at regular logarithmic internals have allowed to follow the electrical parameter variations and to continuously check the failure criteria events. 3 PCM, with a slightly different mask layout, have been submitted to each storage test.

As reported in figure 3.13, just after few hours of storage it is possible to observe important variations of the device parameters, especially regarding the diode stability. The diode leakage suffers the really high temperature just after 1 or 3 hours of test at 375°C and 350°C respectively (see figures 3.13 (a) and (b)). For the storage at 375°C, 1-hour of test has been long enough to induce a big increase of the reverse diode leakage from 5 to 60 times. Despite the big spread of the leakage increase, more than 80% of tested samples have reached or exceeded the failure criteria. For the storage at 350°C, more than 50% of tested samples have reached the failure after 3 hour of test, with a slightly slower degradation of the smaller devices. In both tests, the forward part of the diode has not suffered the same big variation, exhibiting only a small left shift of the characteristic (see figures 3.14 (a) and (c)). Concerning the other electrical parameters, the diode damage has induced a significant increase of all the gate leakages in pinch-off condition (sometimes higher than 1 mA/mm) and a limited left threshold voltage shift (correlated with the forward diode shift), but the other performances, like the saturation current or the transconductance, have not suffered the high temperature application, with a general variation within 5% (see figures 3.14 (b) and (d)). Negligible variation of the dynamic perfomances.

Concerning the storage at 300°C, in this case devices have not suffered a huge degradation of the diode performances during the first hours of test, but only a general limited increase attested from 1 to 3 times after 25-hours of test (on the gate leakages as well), with only few damaged samples (see figure 3.13 (c)). As on the previous tests, the main device performances have not shown big variations, with a average reduction around 5% for the drain current, the transconductance and the on-resistance (see figures 3.14 (e) and (f)).

Therefore, up to now, the storage tests have underlined the really strong influence of the diode stability on the test temperature, making the 350°C a critical temperature for the gate robustness and, as a consequence, for all the device's leakages. Although the limited variation of the other performances, and the stable dynamic behaviour, this temperature has to be considered dangerous and beyond any maximum operative junction temperature, to avoid a really fast reduction of all

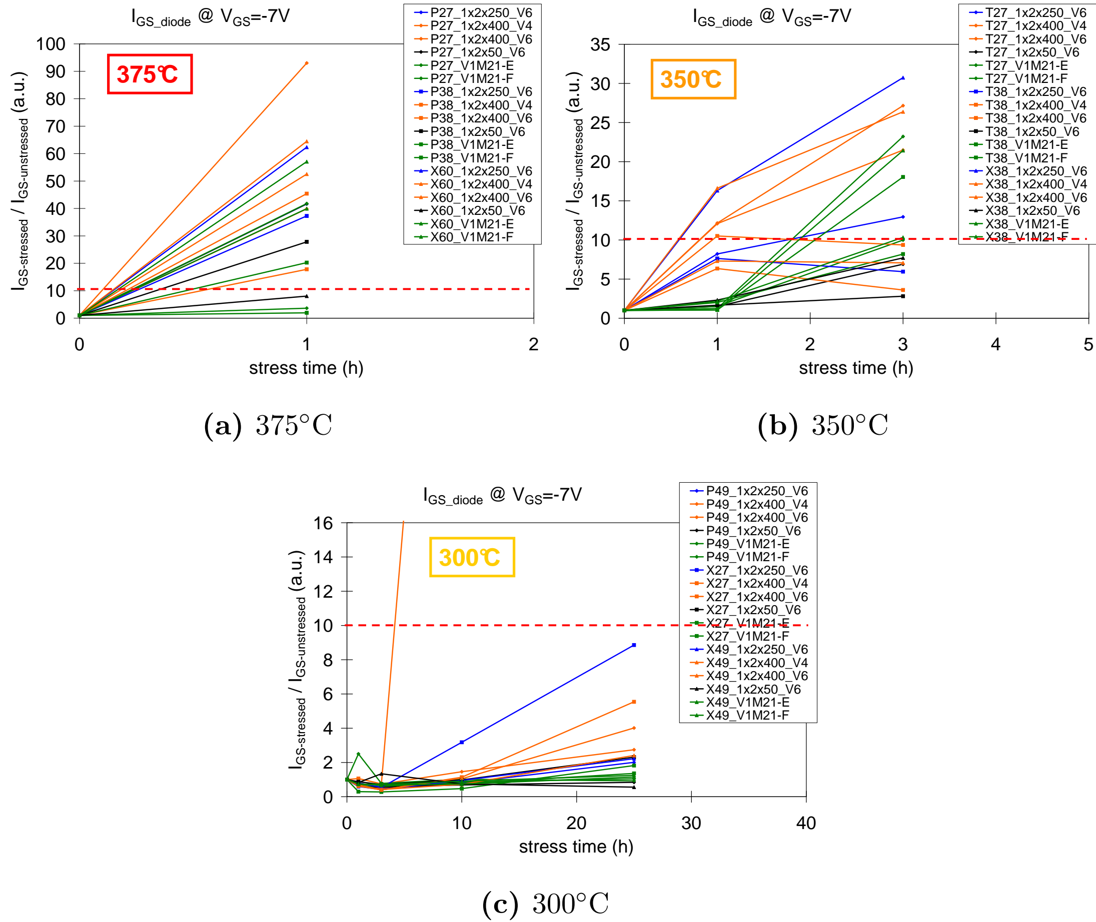
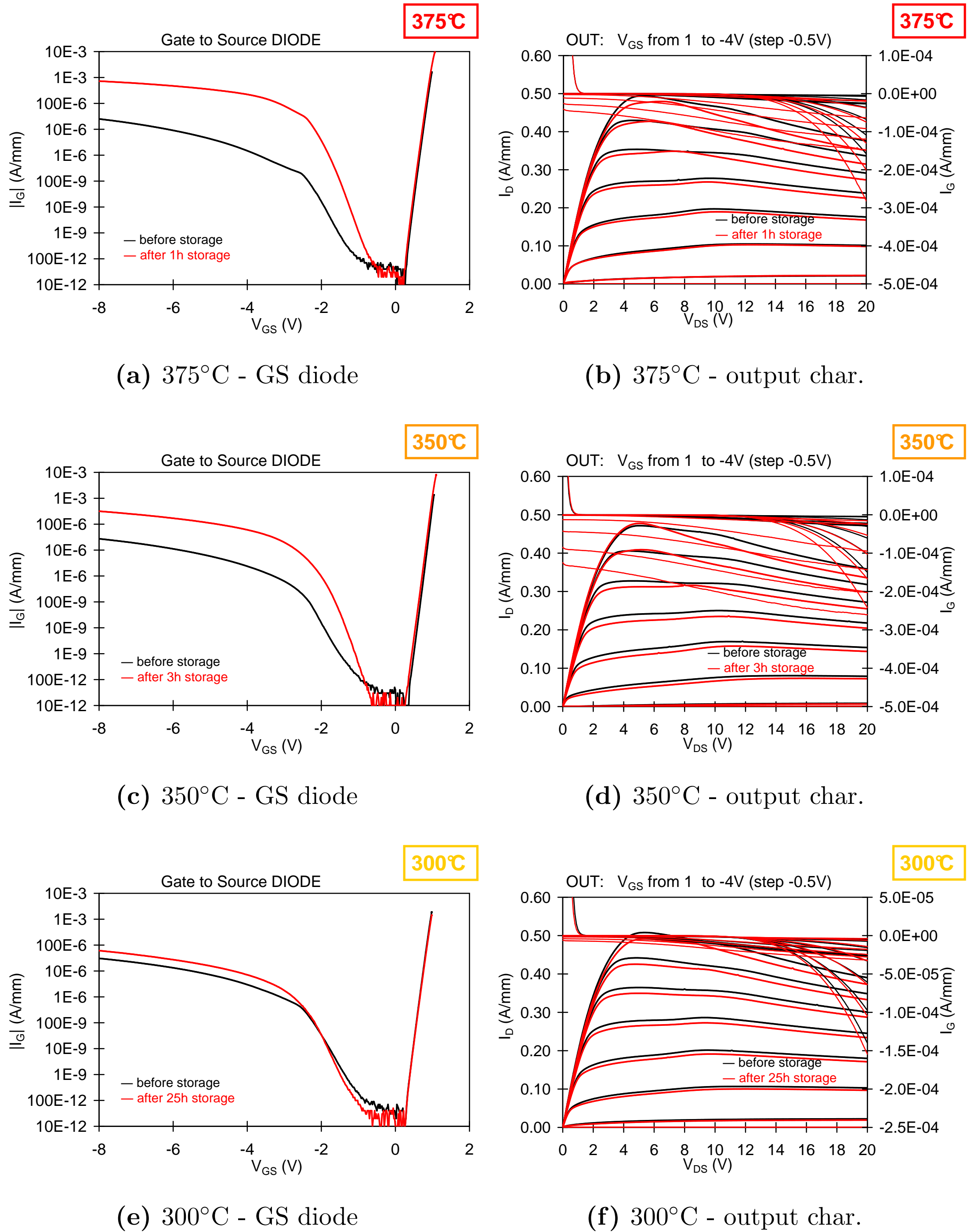


Figure 3.13: Diode leakage variation on all tested samples during the first hours of storage test at 375°C (a), 350°C (b), and 300°C (c); diode leakage extracted at $V_{GS} = -7V$.



(a) 375°C - GS diode

(b) 375°C - output char.

(c) 350°C - GS diode

(d) 350°C - output char.

(e) 300°C - GS diode

(f) 300°C - output char.

Figure 3.14: GS-diode and output characteristic comparisons before and after the storage tests on one typical device for each temperature: (a - b) 1-hour at 375°C, (c - d) 3-hours at 350°C, and (e - f) 25-hours at 300°C.

gate capabilities. Due to the rather short storage duration, it needs to further investigate the long-term effect of the high-temperatures on the device performances, for example of the 300°C or of an intermediate temperature like 325°C, to see if other degradation mechanisms are activated by the high-temperature condition, or if the 300°C is indeed a really stable and robust working condition even for thousand hours of test.

3.3.2 Long term DC life-tests

A DC life-test is typically a long-term test where the degradation effects, induced by the bias condition, are accelerated by the high test temperature, in order to obtain a faster degradation of the device performances, and to estimate the device life-time in any real operating condition. In this case, the DC life-tests have been used to investigate the different behaviour of the space designed devices depending on the applied bias conditions, with the purpose of better understanding the factors that limit the reliability of this technology along the time.

In these life-tests, three bias points have been chosen, in ON-state, semi ON-state (close to pinch-off), and OFF-state, following the RF ideal load-line defined for the real device application, as reported in the short-term test section. The devices designed for this life-test have been the $4 \times 400\ \mu m$ gate-width devices, soldered inside the RF package suitable for the real application as RF amplifier. Due to the different power dissipation of the three bias points, and to avoid a different acceleration of the failure mechanisms induced by the different device temperatures, the junction temperature has been kept constant by means of hot base-plates, especially for the low-power tests. As a results, in table 3.1 are reported the three calculated bias conditions.

The target bias-points has been defined along an ideal load-line that goes from the pinch-off condition at $V_{DD} = 50V$ to complete open channel condition, at low V_{DS} and high I_{DS}. Due to a specific real application as RF amplifier in class AB, the points has been chosen *(i)* in the middle of the output characteristic (ON-state), *(ii)* next to the RF bias point, 300mV above the threshold voltage (semi ON-state), *(iii)* and below the pinch-off voltage, at high $V_{DS} = 75V$ (OFF-state).

	$\mathbf{V_{GS}}$ (V)	$\mathbf{V_{DS}}$ (V)	$\mathbf{T_{plate}}$ (°C)	$\mathbf{I_{DS-meas}}$ (mA)	$\mathbf{R_{TH}}$ (°C/W)	$\mathbf{P_{meas}}$ (W)	$\mathbf{T_{j-estim}}$ (°C)
ON-state	0	25	30	400	14.5	10	175
semi ON-state	$\simeq V_{TH}$	50	145	40	14.5	2	174
OFF-state	-4	75	175	0.21	14.5	0.021	175.3

Table 3.1: DC life-test bias points

Bias points have been slightly adapted to each device, in order to keep the same drain current (and consequently the same output power) for all devices at the same test condition. The junction temperature T_j has been fixed at the same value equal to 175°C for all the three bias conditions, chosen considering the thermal resistance estimation of the devices under test (14.5 °C/W), and the temperature limitations of the DC life-test system.

At this point, it worth to mention that the estimation of the real device junction temperature T_j has been one of the most difficult task, and it is actually one on the most challenging activity for packaged devices. At the moment, many techniques exit for the thermal resistance evaluation, based on electrical measurements [71–73], on optical measurements [74], or on infrared thermography, but each of them suffers of few limitations like the temperature accuracy, the poor lateral resolution, or simply the measurement repeatability. Furthermore, many of these techniques require a different device layout, or in general prevent the evaluation of the thermal resistance directly on the plate where the life-test is performed, the place where the real thermal resistance should be estimated, making the estimated value not completely reliable. In this case, the thermal resistance has been estimated by means of Raman thermal analysis, but almost the same value has been verified by means of pulsed electrical measurements (see figure 3.15) using the technique described by *Joh et al.* in [71].

Up to now, 400 life-test hours have been performed and tested devices are showing very stable performances at each bias condition, as reported in figure 3.16. The main characteristics, like the drain saturation current, the transconductance peak and the on-resistance, are very stable, with a general degradation within 5%.

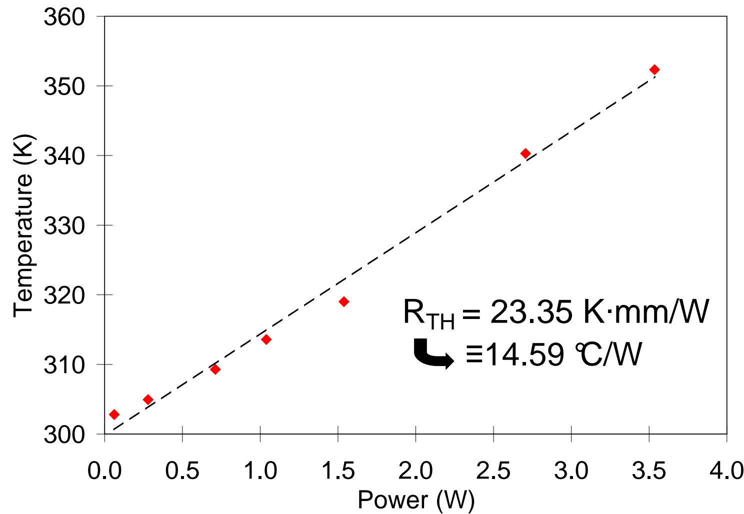


Figure 3.15: Thermal resistance evaluation by means of pulsed electrical measurements, with the method described by *Joh et al.* in [71].

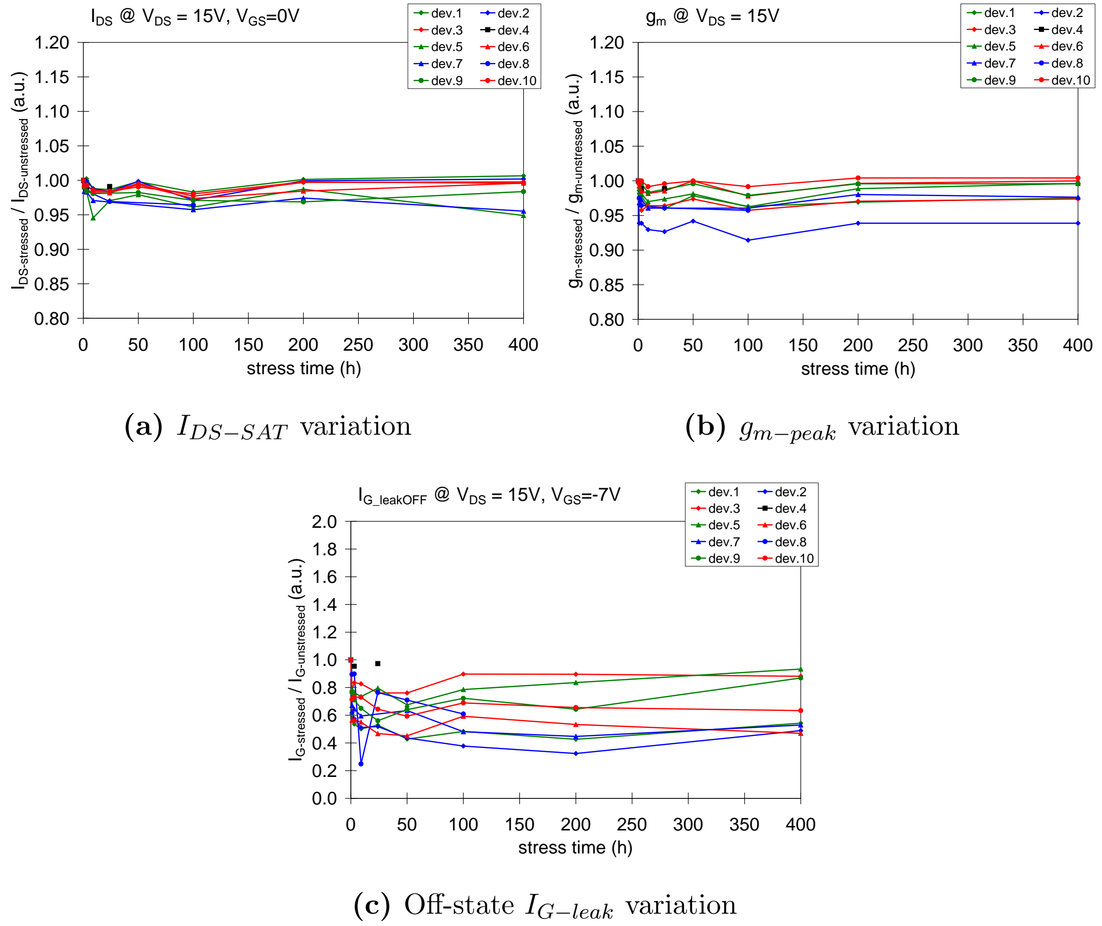
Threshold voltage has shown a small negative shift at the beginning of the test but, after 50-hours, the measured values seem quite stable. For the leakage currents, a general leakage reduction has been observed during the first hours of test, but after 50-100 hours, the leakages seem to recover or further increase, expecially on the high power bias points. Negligible variation of the dynamic behaviour has been observed up to now.

At this intermediate point of the DC life-test, it is further confirmed the robustness of this GaN technology at the bias points close to the real device application and, at least, at this junction temperature. However, it has still to be verified if the simultaneous presence of high temperature and high voltage will reduce the device reliability for longer stress times.

3.4 Conclusions and future activities

The first reliability evaluation of the ESA samples have underlined a very stable and robust technology on both the high voltage and the high temperature point of view:

- the high-voltage step-stress have shown the very good OFF-state robustness of this technology, with a really stable behaviour of all the electrical param-



(a) I_{DS-SAT} variation

(b) g_{m-peak} variation

(c) Off-state I_{G-leak} variation

Figure 3.16: Main electrical performance variations along the DC life-tests (ratio between the stressed and the un-stressed values). In red the ON-state tests, in green the semi ON-state tests, and in blue the OFF-state tests (in black the reference device).

eters up to the final catastrophic failure around 220V;

- the positive temperature dependence of the breakdown voltage and the non-negligible reduction of the breakdown voltage at higher-current tests have suggested an impact-ionization induced failure mechanism. But despite the big breakdown reduction, the critical failure is still quite far from the real device operating region;
- up to now, the storage test have shown a stable behaviour of the main performances up to 350°C, temperature at which the diode characteristic starts to degrade dramatically just after few hours of test. Limited variation of all the other static and dynamic performances;
- finally, the simultaneous presence of high temperature and high voltage in the DC life-tests has not induced any noticeable degradation on the bigger devices, those designed for the final space application, at least up to 400 hours of test at 175°C of T_j.

Nevertheless, further tests can be performed to clearly assess the reliability of this GaN technology, demonstrating the robustness required by the space applications. Storage tests can be used to confirm the high-temperature stability, especially on the gate diodes, even for longer time tests. Furthermore, life-tests can be used to better understand the long-term stability of the biased-devices at higher junction temperatures, approaching the 300°C "safe" temperature, as defined on the previous storage analysis. These tests will give a much more complete overview of the long-term behaviour of these devices at high temperatures and, eventually, of the presence of thermally accelerated failure mechanisms.

Concerning the short-term tests, it will be interesting to further investigate the high voltage behaviour of these devices, as suggested by the emission microscopy measurements, to better understand the shift of the emission profile and the possible role of the drain ohmic contact on the device's failure. The role of the temperature, of the stress duration, and of the hot-electron presence in the ohmic region can be studied, with a special focus on the difference induced by the same tests performed on the real bigger devices. Moreover, it has not been verified the

transient behaviour of the drain-side emission, as suggested on the reported paper, neither the electrical parameter changes due to a parasitic charge accumulation in the drain access region.

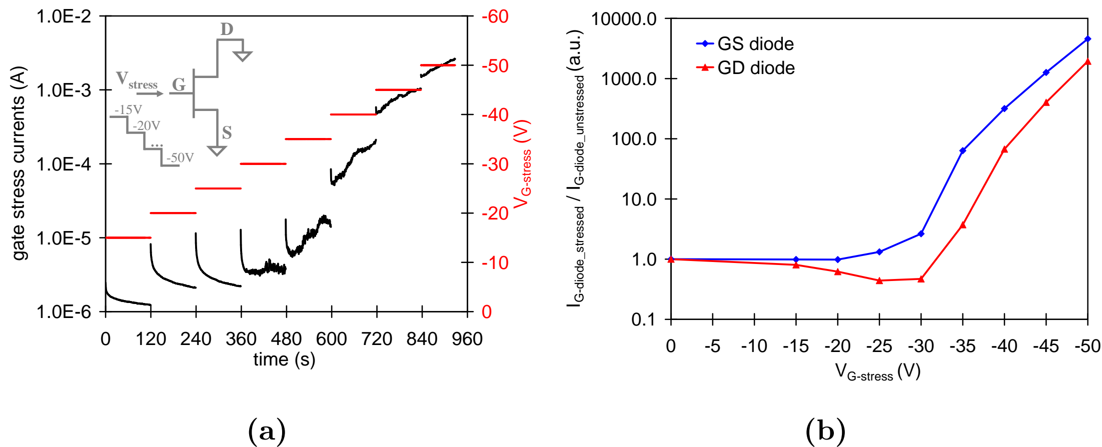
This issue can be interesting not only for RF applications, but also for high-power applications. Indeed, the higher pinch-off voltages used in high-power switching applications can really enhance this phenomenon (despite the low carrier presence) and can cause a strong increase of the drain access-resistance with a huge reduction of the dynamic performances and, as a consequence, of the dynamic efficiency.

Chapter 4

Gate-edge degradation in AlGaN/GaN HEMTs

Despite the recent technological improvements, the robustness of the AlGaN/GaN HEMT devices at high reverse biases is still a challenge. As reported in chapter 1, in 2007 *Joh et al.* [51] have assumed that there exists a "critical" drain-to-gate voltage beyond which the gate diode degrades, suggesting that degradation is related to crystallographic defect formation through converse-piezoelectric effect. According to this hypothesis, degradation mainly interests the drain edge of the gate, and occurs when a critical elastic energy is reached, due to the mechanical strain produced by the electric field. After the first observation, many other groups have reported the same effect, summarized on a big increase of the gate leakage starting from a quite uniform "critical" point, an enhancement of the current collapse or in general of the trapping effects, and sometimes a worsening of the main DC performances.

A simple way to verify the presence of this failure mechanism consists in carrying-out a reverse-bias step-stress experiment, increasing the gate negative voltage step by step, either with the device in off-state condition or with the drain and the source contact at ground. When a certain reverse voltage is reached, typically defined as *"critical voltage"*, the gate leakage current increases substantially, reaching sometimes 10^4 times the initial value. The *critical voltage* depends on the wafer technology, and it is typically consistent for all devices inside the same wafer.



(a) (b)

Figure 4.1: Summary of one typical step-stress experiment: (a) gate stress current at each step of stress and (b) measured gate diode leakages ($V_G = -8V$) after each step of stress. On this device technology, the *critical voltage* is defined around -35V of V_G, as reported by the non-recoverable increase of the diode gate currents from step at $V_G = -35V$ and beyond. Inset in (a): schematic representation of the adopted stress conditions.

During the tests, localized damage points are created, inducing sudden "jumps" in the leakage current; each jump corresponds to the creation of a new breakdown point and is followed by an increase of the leakage current [63]. Adopting electro-luminescence (EL) microscopy measurements as a tool to identify localized reverse current injection points and damaged areas [54], it is possible to correlate each jump of the leakage current with the appearance of a new localized emission point. As the reverse voltage increases, the gate leakage increases, followed by an increase in the density of the defect points observed by means of the EL images.

The gate degradation and the following *critical voltage* identification have really often been evaluated by means of the step-stress experiment, for example even on the previous chapters, on both the Task-Force and the ESA device reliability assessment. Moreover, the use of the step-stress experiment is justified by the gate degradation mechanism proposed in [51], which assumes the creation of crystallographic defects in the AlGaN layer only beyond a critical electrical-field hence voltage. Therefore, following the basis of this theory, a device can theoretically operate at voltages below this *critical voltage* without showing any degradation for

an infinite period of time. In a more recent study of 2010, *Marcon et al.* [75] have shown that degradation can occur even below the *critical voltage* for sufficiently long stress times, suggesting that gate degradation is a time-dependent mechanism which depends on the stress voltage level, with a weak dependence on the temperature.

This result highlights that the step-stress experiment is not sufficient to understand the gate degradation mechanism of a device, due to the absence of a long-term evaluation of the gate robustness. Furthermore, the previous definition of a safe operating voltage-range below the *critical voltage* can not be further considered, and different approaches for the evaluation of the gate degradation needs to be used.

To improve the knowledge on this topic, and on the parameters involved on this failure mode, this chapter presents a deep analysis of the physical mechanisms responsible for the reverse-bias degradation of GaN HEMTs, providing a model that explain both the recoverable and the permanent modifications of the electrical parameters occurring during stress time. In particular, the results have demonstrated that recoverable degradation of gate-current and threshold voltage is due to the simultaneous accumulation of negative charge in the AlGaN layer, and of holes at the interface between AlGaN and GaN, respectively. Then, through an extensive analysis of the degradation kinetics, it has been observed that permanent gate-current degradation proceeds through a defect generation and percolation process, that initially determines an increase in the noise of gate current, and then eventually results in the generation of localized leakage paths. The defect density's dependence of the time-to-breakdown has been confirmed correlating the device failure time with the initial leakage current, a representative index of the initial device's defectivity.

4.1 Reverse bias gate step-stress

All the following studies have been carried out on GaN-HEMT devices grown on 4H-SiC substrate. Wafer vertical structure consists of a GaN buffer layer 2 μm

thick, and a 22 nm AlGaN (barrier) layer, with a 26% Aluminum content. Drain and source ohmic contacts are based on Ti/Al/Ni/Au. Gate Schottky contact is based on Ni/Au (40 nm and 300 nm for Ni and Au respectively). Finally, devices have been passivated with a 400 nm SiN layer. Gate-length is 0.5 μm and gate-width is 400 μm. Devices have a gate-source distance of 1.15 μm and a gate-drain distance of 2.05 μm. Gated-TLM structures have also been analyzed, with a 5 μm gate-length, a 100 μm gate-width, and with gate-source and gate-drain distances equal to 5 μm. A schematic structure of the analyzed samples is reported in figure 4.2.

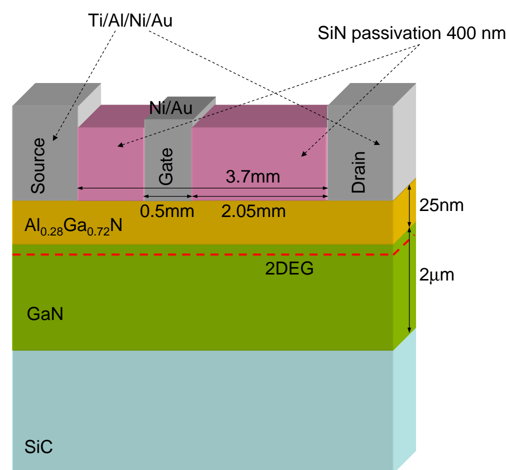


Figure 4.2: Schematic representation of the structure of the analyzed samples.

To characterize the time and voltage-dependence of the degradation process, devices have been submitted both to reverse-bias step-stress experiments (similarly to [51]), and to constant-bias stress tests. At different stages of the stress experiment, samples have been fully characterized by means of electrical measurements, of time-resolved Electroluminescence Measurements, and of spectrally-resolved EL analysis. EL measurements have been based on a cooled CCD camera, a monochromator (only for the EL spectra), and an optical microscope. By means of this system, it has been possible to measure micro-EL patterns with 1 μm optical resolution in a very short time (in the order of 0.5-5 seconds), giving the possibility of performing time-resolved analysis of the EL pattern of the device submitted to reverse-bias stress.

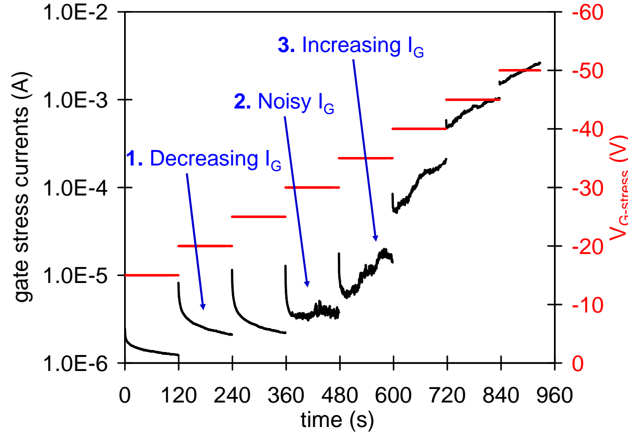


Figure 4.3: Summary of one of the step-stress experiments carried out within this activity. During stress at moderate gate voltage levels (for $|V_G| < 30V$), gate current decreases monotonically during each step. At a certain step (for $V_G = -30V$) gate current becomes noisy, indicating that the device is about to degrade. After this step, degradation starts to happen, detected as a non-recoverable increase in gate current (see step at $V_G = -35V$ and beyond).

In figure 4.3 are reported the results of a typical step-stress experiment carried out on a gated-TLM structure. In this test, drain and source are grounded, and a negative voltage is applied for 120 seconds to the gate. During the stress, gate current and EL signal are continuously monitored. Every 120 s, gate voltage is decreased by 5 V, until failure is reached. Looking at the diagram, three different behaviours can be observed, depending on the applied stress voltage level:

1. for low stress voltage levels (i.e. for $|V_G| < 30V$), gate current shows a recoverable monotonic decrease during stress time (marker 1 in figure 4.3);

2. before failure takes place ($V_G = -30V$), gate current becomes noisy, indicating that a permanent damage is about to occur (marker 2 in figure 4.3);

3. when a "critical voltage" is reached, devices show a permanent degradation (marker 3 in figure 4.3), i.e. a non-recoverable increase in gate leakage current (here beyond $V_G = -35V$).

With this experiment, it is possible to have a first indication of the voltage limitation of a device technology, and to identify the *critical voltage* as described on

the previous section. In particular, for this technology the *critical voltage* is around -35V. Nevertheless, the presence of three different behaviors indicate that several mechanisms occur during stress time, and the use of a step-stress experiment prevents a better understanding of each single mechanism. Variously, in the 400 μm gate-width devices, tests have been carried out only on the gate-drain junction, due to the asymmetrical position of the gate contact. Despite these differences, devices have shown the same gate damage as well as the same *critical voltage*.

4.2 Reverse bias DC stress

To better understand the origin of the gate degradation and the physical mechanisms leading to each different behaviour, devices have been submitted to constant reverse-bias gate stress, monitoring the electrical and optical characteristics by means of time-resolved EL and electrical measurements. As on the step-stress experiments, most tests have been performed in gated-TLM structures, on both gate diodes due to the symmetrical position of the gate contact. For the 400 μm gate-width devices, tests have been performed only on the gate-drain junction.

Furthermore, in each reverse current or reverse voltage gate-bias stress, the device failure time (or time-to-breakdown) has been defined as the time when the first clear jump happens on the gate stress voltage (or current respectively), with a step larger than an experimentally defined value.

4.2.1 Constant gate reverse-current tests

First tests have been constant gate reverse-current tests. With these tests, it has been investigated the effects of the gate current on the gate degradation phenomenon, trying to correlate the final failure voltage with the *critical voltage* identified on the previous tests. As a results, the constant current tests have not shown a clear correlation between the stress current and the failure time (as reported in figure 4.4 (a) and (b)), but only a big variation of the failure times from hundreds of seconds to more than one hour. Nonetheless, few important information can be drawn.

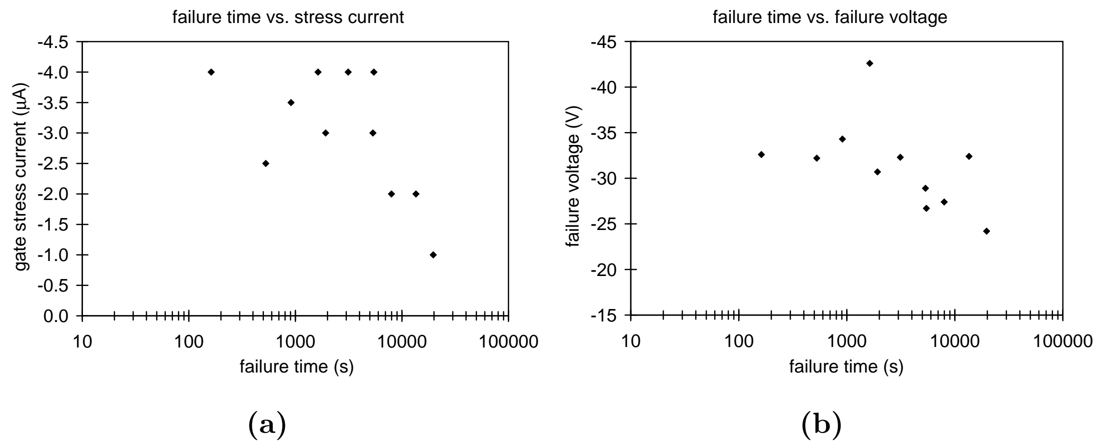


Figure 4.4: Correlation between failure time and stress current (a) and between failure time and gate voltage (b), of each constant reverse-current test performed on these devices.

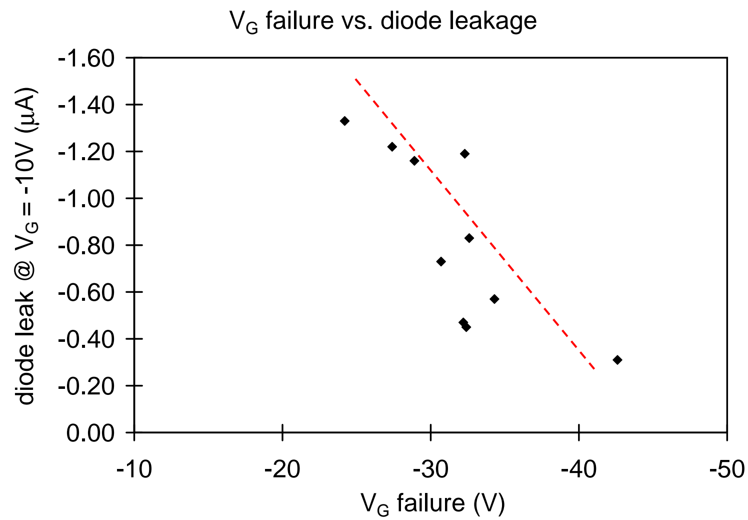


Figure 4.5: Correlation between the initial gate leakage current and the gate failure voltage during constant reverse-current tests performed on these devices. The red line is only a guide for the eye.

If the gate stress current has not exhibited a strong influence on the gate failure, it seems to accelerate the degradation process, due to the fact that the mean failure time at -4 μA of stress current is lower than that at -2 μA. Moreover, the gate failure voltage is not fixed at the previously defined *critical voltage*, but it spreads from about -25V to -35V, with few extreme points around -40V.

Looking at the initial gate leakage measured on the gate-drain diodes before the stress, it is possible to observe a limited trend between this current and the failure voltage, suggesting a dependence of the critical failure on the initial level of leakage (see figure 4.5). But due to the different gate stress currents used along the tests and to the limited statistics, it is difficult to understand if the trend is connected to a real dependence on the initial gate leakage, or if it is just a coincidence.

4.2.2 Constant gate reverse-voltage tests

To better understand the different mechanisms involved on the reverse-bias gate step-stress, and to clarify the results obtained on the constant-current tests, constant gate reverse-voltage stress have been performed on the same samples.

In figure 4.6 the typical results obtained during these tests are summarized. At the beginning of the constant voltage stress, gate current and threshold voltage show a nearly exponential decrease (figures 4.6 (a) and (c)), while the amplitude of gate current noise is relatively low (figure 4.6 (b), before 300 s). During this initial phase, devices emit a weak luminescence signal, which is uniformly distributed along the channel (see the second frame of figure 4.7, labeled as "10 s"). Device luminescence has a Maxwellian spectrum (figure 4.8), indicating that EL originates from the relaxation of highly energetic electrons injected from the gate into the buffer [68]. Increasing the reverse gate-voltage level, a broad yellow peak appears superimposed to the main Maxwellian spectrum, maybe related to the presence of the donor-acceptor pair in the buffer, which is considered to be responsible for the yellow luminescence in GaN (see figure 4.9; for better details, see following chapter 5).

After a certain period of time, the gate current starts to increase, leading to the non-recoverable degradation of the gate diodes. In particular, permanent device

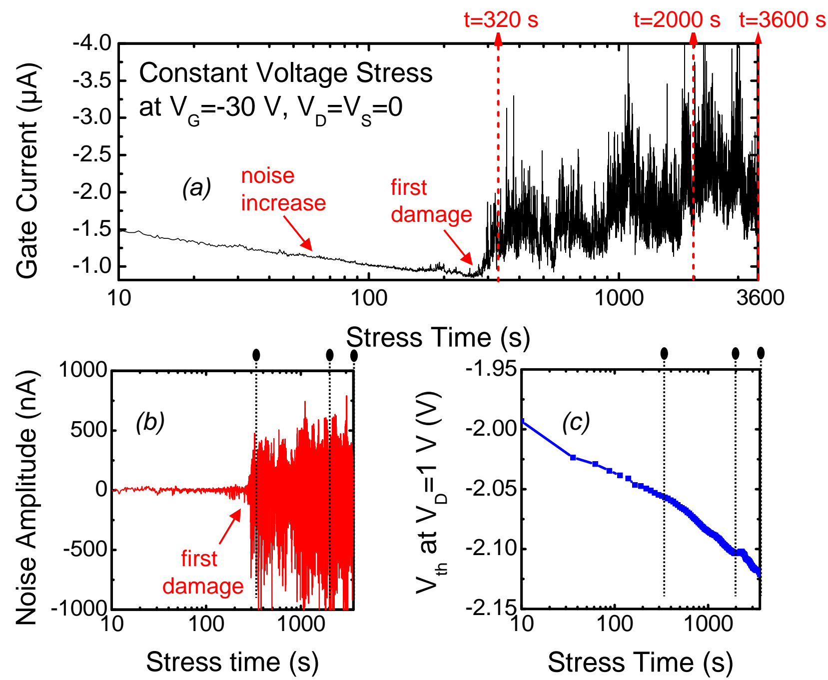


Figure 4.6: Results of a constant-voltage reverse-bias test at $V_G = -30V$ and $V_D = V_S = 0V$. The three graphs report the variation of (a) gate current, (b) amplitude of the noise on gate current, (c) and threshold voltage during stress time.

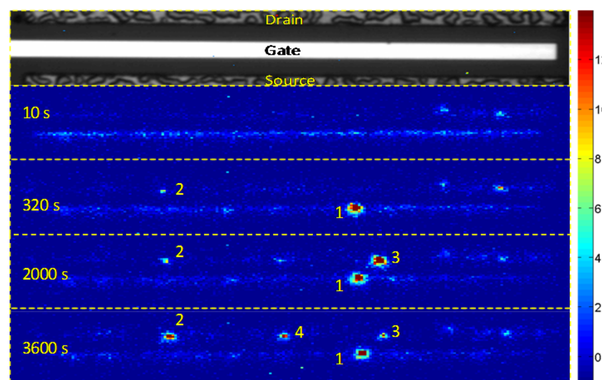


Figure 4.7: Results of the time-resolved EL measurements carried out during stress at $V_G = -30V$ and $V_D = V_S = 0V$ (same test as in figure 4.6). The figure on the top represents a schematic micrograph of one of the analyzed samples. The frames below are false-color images reporting the distribution of device luminescence for increasing stress times.

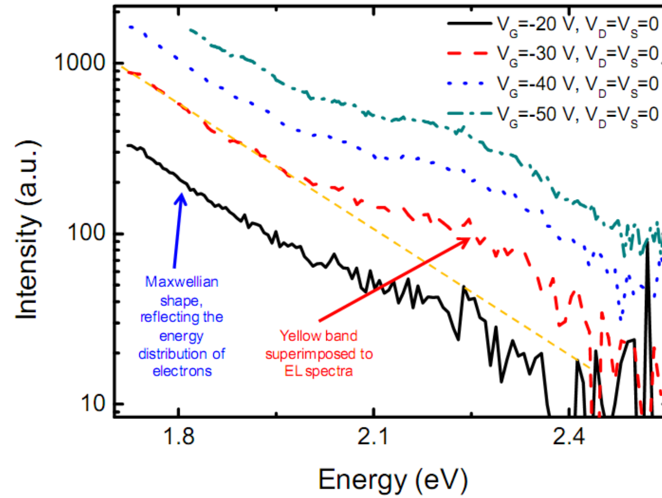


Figure 4.8: EL spectra measured under reverse-bias conditions on one of the analyzed HEMT devices. For $V_G < -30V$, EL spectrum is constituted by the superposition of a Maxwellian curve and a broad yellow peak, centered around 2.2 eV.

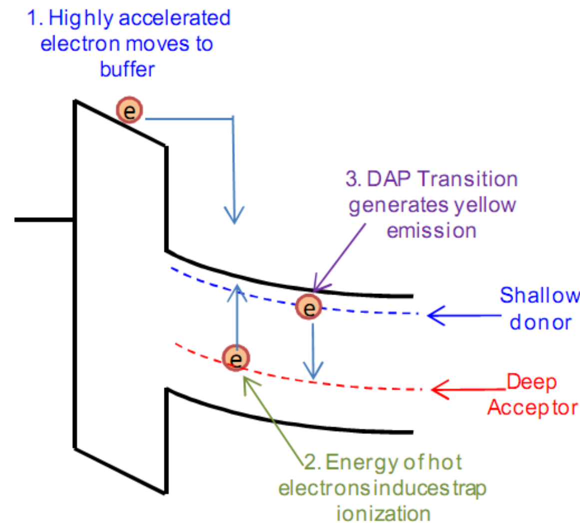


Figure 4.9: Schematic explanation of the reverse-bias EL process on the tested AlGaN/GaN samples.

degradation consists in a sudden increase of the gate current (in this particular case occurring after 300 s of stress for the device in figure 4.6 (a)), corresponding to the generation of a luminescent spot in the micro-EL images (see the third frame of figure 4.7, labeled as “320 s”). This hot spot indicates the generation of a damaged region, i.e. of a preferential path for leakage current conduction. It is worth noticing that device degradation is preceded by an increase in the amplitude of the noise superimposed to gate current (see figure 4.6 (b)).

Time-resolved EL analysis indicates that by leaving a device for a long time under stress, degradation may continue through the generation of further leakage paths, identified as luminescent “hot-spots”, that appears in the micro-EL images one after the other (see figure 4.7). Even if current becomes noisy after degradation, measurements indicate that every time a new luminescent spot is generated, gate current shows a step-like increase, as it can be observed comparing figure 4.6 (a) with figure 4.7).

Remarkably, stress tests have indicated that the generation of permanent leakage paths, and consequently of luminescent hot spots, can occur even for stress voltage levels smaller than the *critical voltage* identified by means of the step-stress tests, which is equal to -35 V for the samples under investigation. For instance, for a stress voltage level of -15 V, permanent degradation occurs approximately 10^5 s (27 hours) after the beginning of the stress test, with an increase of the gate current noise well before the failure (see figure 4.10).

Based on the experimental evidence collected within this work, the following model is proposed to explain the recoverable and the permanent modifications of the electrical characteristics of the HEMT devices submitted to reverse-gate stress (see figure 4.11). The model considers that within the buffer there exists a deep acceptor level, located around 0.9 eV above the valence band, which is responsible for the yellow luminescence of GaN [76, 77]. When a reverse-bias is applied to the gate, a leakage current (see figure 4.6 (a)) flows through the AlGaN layer, for example via trap-assisted tunneling. Trap levels at the surface or in the AlGaN layer become negatively charged, and this determines a recoverable decrease in the gate current during constant voltage stress. Charging of the trap states can

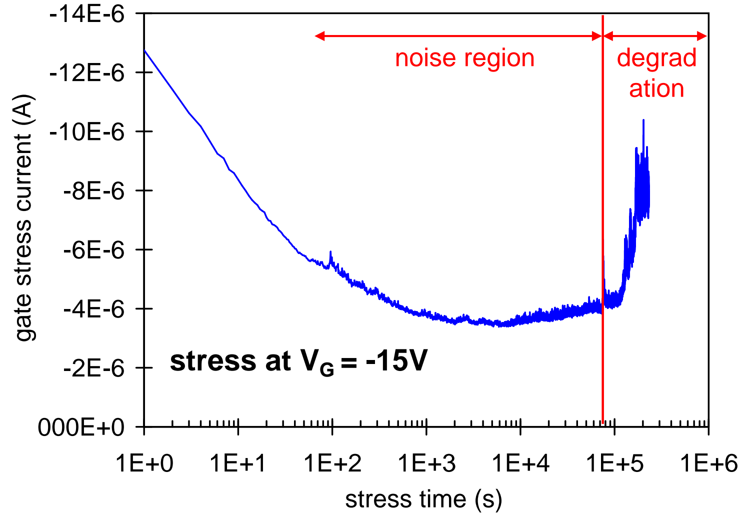


Figure 4.10: Variation of gate current during constant voltage stress, at $V_G = -15V$ and $V_D = 0V$. During the initial phase of the stress test, gate current decreases monotonically. The first permanent damage occurs about 10^5 seconds (27 hours) after the beginning of the stress experiment.

be modeled as a RC network, as demonstrated by the exponential dependence of gate current on stress time. Due to the high electric field, electrons in the AlGaN tunnel into the buffer (phase 1 in figure 4.11), where they go through energy relaxation emitting light due to intraband transitions [61] (phase 2 in figure 4.11). The Maxwellian shape of the EL spectrum (see figure 4.8) reflects the energetic distribution of the carriers. For sufficiently high reverse voltage levels, electrons may achieve enough energy having two possible consequences: *(i)* electrons can ionize the deep acceptor level located 0.9 eV above the valence band in the buffer (phase 3 in figure 4.11), thus generating the yellow luminescence signal detected by the EL measurements (phase 4 in figure 4.11), due to a radiative recombination of electrons from the conduction band (or from a shallow donor state) to the available deep acceptor level; (ii) electrons can promote the transfer of an electron from the valence band to the deep acceptor level (phase 5 in figure 4.11)), thus leading to the generation of a free hole close to the AlGaN/GaN heterointerface (phase 6 in figure 4.11)).

Generated holes are accumulated at the AlGaN/GaN interface or trapped into the AlGaN layer, due to the high negative voltage applied to the gate, determining

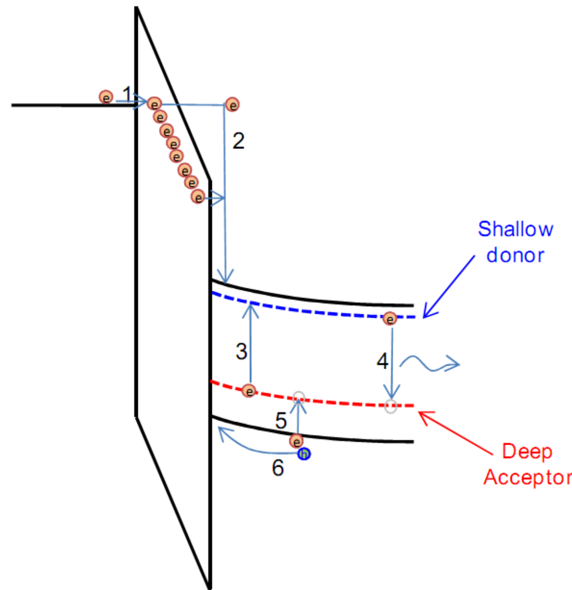


Figure 4.11: Schematic representation of the model used to explain the recoverable modifications in gate leakage current and threshold voltage on the tested AlGaN/GaN samples, submitted to reverse-bias tests

a shift of the threshold voltage towards more negative values (see figure 4.6 (c)). Consistency of this model has been verified by means of 2D simulations, showing good agreement with the experimental data.

For sufficiently long stress times, even at moderate voltage levels, defects are randomly generated within the AlGaN layer. Defect generation can be due either to converse piezoelectric effect [51], to atom displacement due to the high applied field [54], or to electrochemical reaction or diffusion [23, 78]. As reported in figure 4.12, when defect concentration increases, possibly due to a percolation process which can be accelerated at high electric-fields, traps may randomly overlap, thus increasing the noise on the gate current (see figures 4.6 (b) and 4.10). Moreover, for longer stress times, these defects may generate a conductive path between the gate and the channel, thus leading to a localized and permanent degradation identified by means of electroluminescence imaging.

Based on the model described above, degradation is ascribed to a defect generation and percolation process. Under this assumption, devices with higher initial defect density should exhibit a time-to-breakdown significantly lower than identical devices with lower defect density. As a consequence, to better understand the

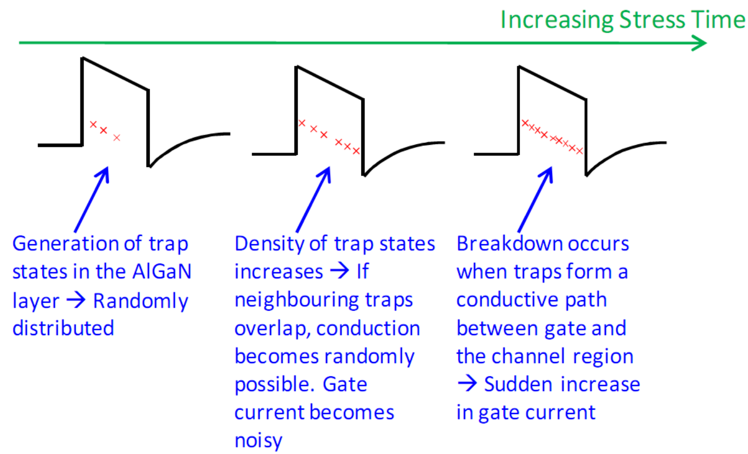


Figure 4.12: Schematic description of the model used to explain permanent degradation of AlGaN/GaN HEMTs submitted to reverse-bias stress.

consistency of this theory, tests at the same gate reverse-bias but with different initial leakage levels have been performed.

In figure 4.13 is shown the failure time of each sample stressed at a constant reverse-bias, correlated with the correspondent stress voltage. From this diagram, a trend between the stress voltage and the failure time is not clearly visible, due to the really large failure-time range at the same stress voltage, that spread for about six order of magnitude, and even due to the limited test statistics. But on a deeper analysis of the particular points correspondent to each device tested at -30V of gate voltage (the red circle in figure 4.13), it has been observed that the large failure voltage range is due to the extremely different initial leakage level of the tested devices. In particular, devices with lower initial leakage exhibit longer failure times (or time-to-breakdown t_{BD}), whereas devices with higher initial leakage exhibit shorter t_{BD}, showing a clear power-law dependence between the initial leakage and the failure, as reported in figure 4.14.

These results further confirm the previous hypothesis of the percolation process. In fact, devices with high initial gate leakage have shown a time-to-breakdown significantly lower than identical devices with low gate leakage (with a power-law dependence), due to a higher initial defect concentration that allows a faster overlapping of the generated defects (randomly distributed) and consequently a faster generation of a conductive path between the gate and the buffer.

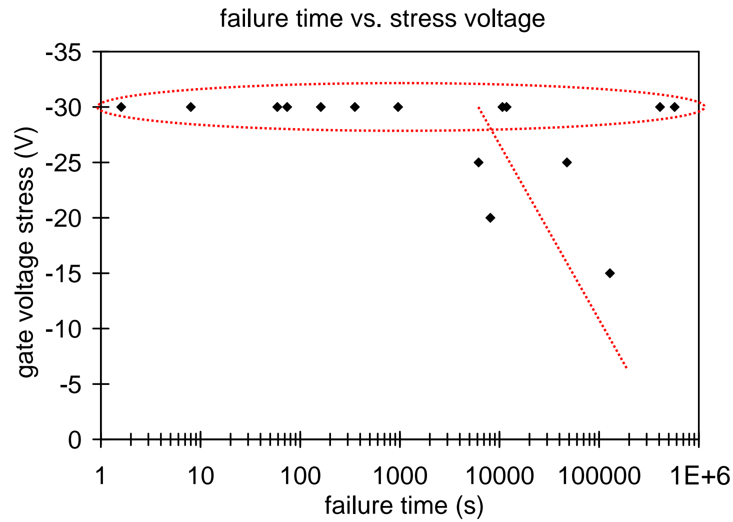


Figure 4.13: Correlation between time-to-failure and stress voltage during constant reverse-voltage tests performed on these devices. The red line is only a guide for the eye, trying to correlate the failure time with the stress bias.

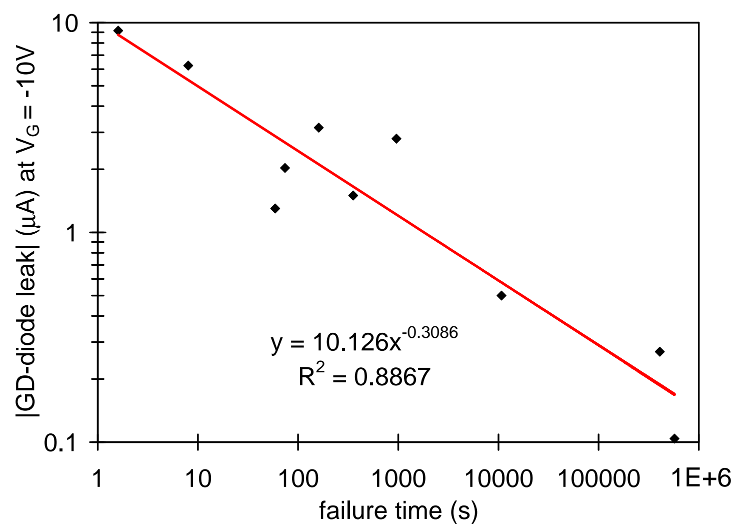


Figure 4.14: Dependence of failure time on the initial leakage current, for devices with different initial leakage current levels aged at $V_G = -30V$ and $V_D = 0V$ (those within the red circle in figure 4.13).

In conclusion, experimental evidence collected within this tests suggests that different mechanisms can occur when a negative gate bias is applied to a GaN HEMT, as indicated by the trends of the gate current and the threshold voltage in figure 4.6. Furthermore, it has been observed that even if a *"critical voltage"* of a specific technology can be determined by the method described in [51], failure can occur at voltage levels significantly smaller than the critical one for sufficiently long stress times (consistently with [75]). The gate failure has consequently been ascribed to a defect-percolation process enhanced by the defect density concentration, reliably identified by means of the initial gate leakage level.

4.3 Failure analysis

As described in chapter 1, several failure analysis techniques have been often employed to observe the physical damage induced by the reverse bias tests, trying to identify which physical mechanism leads this device degradation. In recent literature papers, Transmission Electron Microscopy (TEM) observations at the drain side of the gate on devices submitted to high electric-field tests have shown the presence of pit-shaped defects and cracks [58, 79]; Scanning Electron Microscopy (SEM) and Atomic Force Microscopy (AFM) analysis after de-metalization process have revealed pits at the gate edges of devices which have been tested beyond the *critical voltage*, with size and density correlated with the stress voltage and the test duration [80].

Following these results, several TEM analysis have been performed on many cross-sections coming from different samples submitted to reverse-bias tests. These tests have been carried out on gated-TLM structures belonging to different wafers, from the wafer used on the previous gate-degradation analysis to other wafers coming from previous batches of KorriGaN project. Before focused-ion-beam (FIB) milling, devices have typically been step-stressed with the standard step-stress procedure, as described on the previous part, following the variation of the electrical parameters and even of the micro-EL signal. In this way, using the aforementioned model, it is possible to have a clear map of the positions of the stress-induced

damage points, following the hot-spots visible on the EL images. Indeed, unlike the TEM investigations on stressed devices reported in the literature, where the site selection has been either randomly or systematically chosen, this TEM analysis utilized EL images as a guide for the defects location.

In spite of this new skill for the localization of the damaged area position, with a resolution around 1 μm, the TEM analysis have highlighted the extreme difficulty on the detection of material cracks or defect chains with nanometer-scale size, that extends vertically from the gate-edge through the AlGaN/GaN heterojunction, especially at the early stages of degradation. Nevertheless, few important considerations about the physical gate-degradation can be drawn from the obtained results, here reported on a highly-defected wafer and on a low-defected wafer respectively.

The first analysis reports two TEM cross-sectional samples of a highly-defected device submitted to a reverse-bias test, see figures 4.15 and 4.16. This device showed a really high gate leakage current at the beginning of the test, confirmed by the presence of few native spots already visible at the gate-edge (see 4.15-untreated). Due to the high initial leakage level, the stress has not induced a significant degradation of the leakage performances. But despite the different starting point, the gate degradation has proceeded in the same way as on the low-leakage devices, showing an increase on the emission points and the appearance of few new hot-spots after a critical voltage consistent for all the devices tested on this wafer.

The biggest “hot-spots”, correspondent to a pre-existing defect (point (a) in figure 4.15) and a stress-induced defect (point (b) in figure 4.15) identified by means of the micro-EL images, have been cross-sectioned to gain more information about the physical nature of both type of defects.

As reported in figure 4.16 (a), a V-shaped defect, associated with a threading dislocation (TD) from the underlying GaN layer, has been observed directly beneath the gate edge, in correspondence of the point (a). This defective zone could easily represents a path for the gate leakage, leading to the hot carrier injection previously observed in the EL images. On the other damaged region (b), several attempts have been made to find V-type defects or other type of defects or cracks

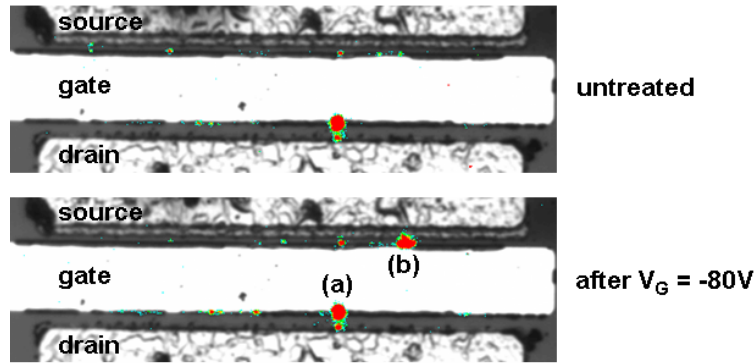


Figure 4.15: Electroluminescence emission micrographs of a 15 μm gate-length TLM HEMT of the highly-defected wafer. Emission images taken at $V_G = -10V$ and $V_D = V_S = 0V$ before and after a reverse-bias gate step-stress from -15V to -80V (false-colors correspond to the emission intensity), superimposed to the picture of the device under test. Point marked with (a) corresponds to a pre-exiting defect; point marked with (b) corresponds to a test-induced defect.

(see figure 4.16 (b)), even at other locations along the gate finger, but without success.

The second investigation reports the same failure analysis made, this time, on a low-defected wafer, in particular to find clear evidences of the stress-induced material defects. But despite the significant damage observed by means of the EL measurements, it has been really difficult to visibly identify any stress induced defect, even using the guide provided by the EL images. Moreover, the same results have been obtained even trying to cross-section a large porting of the gate, parallel to the finger and in correspondence of the gate-edge.

In the following is reported the only clear crack-damage observed thanks to the TEM analysis (see figure 4.18). The device depicted in figure 4.17 has been sectioned perpendicularly to the gate finger and various lamellas have been lifted-out across the major hot spots visible after the step at $V_G = -45V$. As shown in the bottom image of figure 4.17, the entire device width consisted of “hot spots”, with a high density of defects created by the high gate reverse-voltages. The image exhibits a vertical spike about 50 nm from the drain edge of the gate, that crosses the AlGaN layer and penetrated into the GaN (see figure 4.18). The diameter of this spike is on the order of 5 nm, a size not comparable with the best resolution

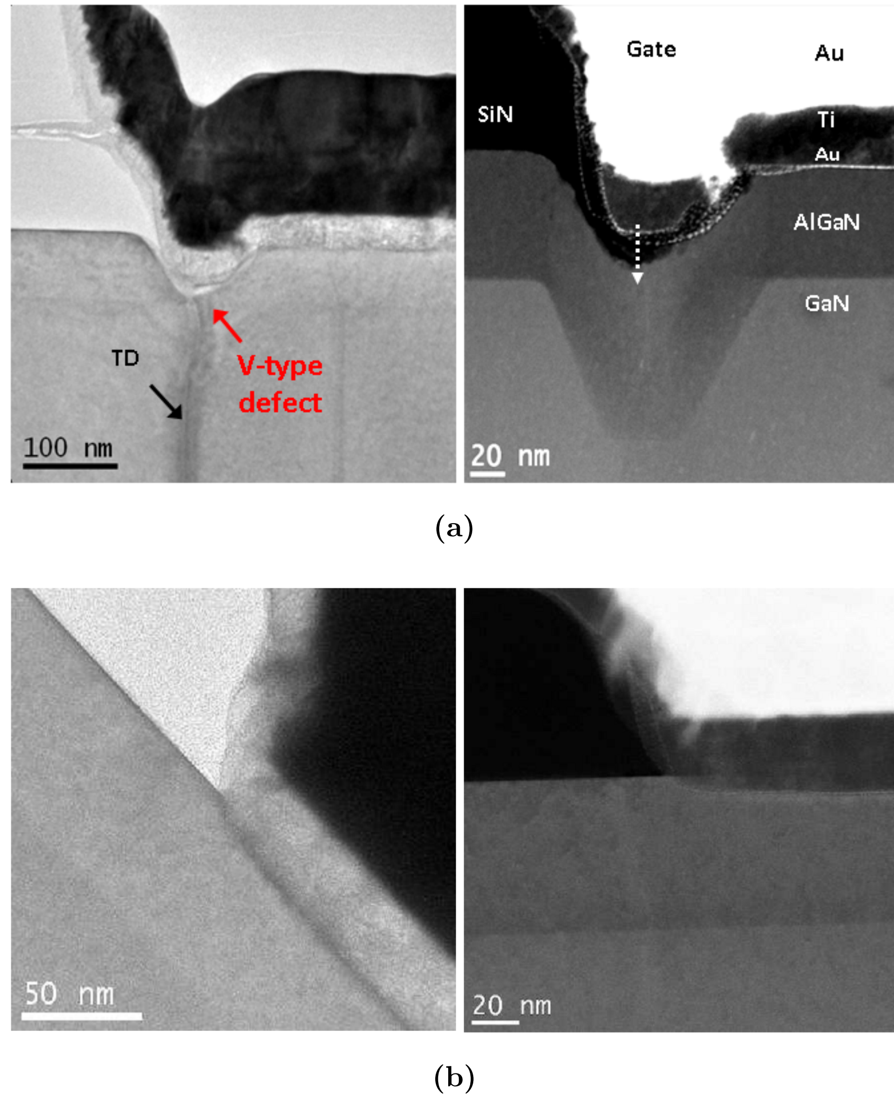


Figure 4.16: (a) Bright-field and dark-field TEM images of the cross-section at the gate edge corresponding to point (a) in the previous figure 4.15. A V-type defect associated with a threading dislocation (TD) is clearly visible. (b) Bright-field and dark-field TEM images of another section, at the gate edge corresponding to point (b) in the previous figure, where no defects are visible.

of the micro-EL images.

Other analysis aimed at detecting the presence of cracks or pit-shaped defects by means of SEM or AFM techniques, as described by *Makaram et al.* in [80], have not produced the expected results, due to the really small size of the induced defects at the early stages of degradation, and to the poor quality of the semiconductor surface after a de-metalization process.

Summarizing, the reported results have shown that the mechanism leading to the huge increase of gate leakage is the same in low- and high- defective materials (the latter probably presenting a remarkably lower *critical voltage*), suggesting that the gate degradation proceeds in the same way independently on the material quality. TEM observations have shown that EL emission can take place in correspondence of native V-type structural defects on top of dislocations in the AlGaN/GaN epitaxial structure, or in correspondence of stress-induced nm-size vertical cracks close to the edge of the gate. Few spikes or cracks have been detected by TEM analysis only on highly degraded devices. Nevertheless, the observation of these spikes is rare, and it is quite impossible to locate any of them in moderately degraded samples. In fact, the nanoscale size of these defects makes them extremely difficult to locate, even when using the EL images as a guide for the FIB cross-sectioning, which has a 20-nm accuracy in positioning of the cut region. Therefore, the correlation with EL micrographs, which have optical resolution around 1 μm, is almost impossible.

Nonetheless, the presented results refer to devices at the early stages of degradation, with test durations shorter than 10 hours at room temperature. Further tests using longer stress times or higher test temperatures could enhance the gate degradation increasing the possibility of a physical damage detection, as reported on the literature papers.

4.4 Conclusion and future activities

In this chapter it has been investigated the failure mechanisms involved on the critical off-state degradation of previous technologies of AlGaN/GaN HEMTs, due

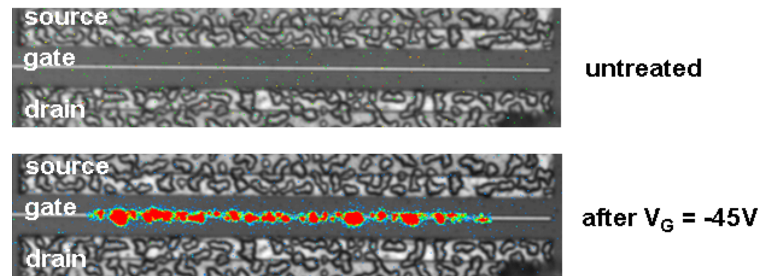


Figure 4.17: Electroluminescence emission micrograph of a 0.5 μm gate-length TLM HEMT of the low-defected wafer. Emission images taken at $V_G = -10V$ and $V_D = V_S = 0V$ before and after a reverse-bias gate step-stress from -15V to -45V (false-colors correspond to the emission intensity), superimposed to the picture of the device under test.

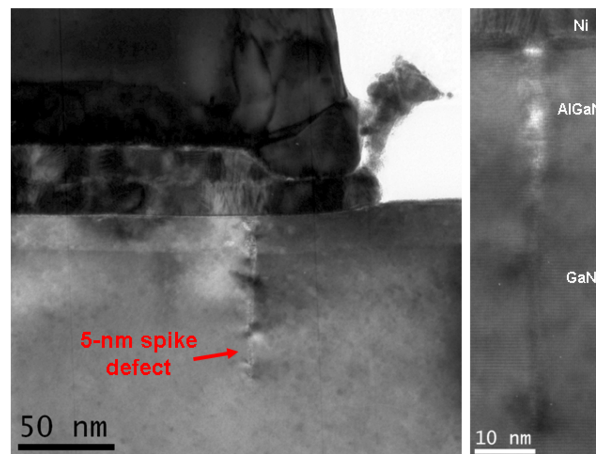


Figure 4.18: Bright-field TEM image of the gate-edge area, with objective aperture inserted to increase the image contrast, on a cross-section from the tested sample shown on the previous figure 4.17. A crack is visible beneath the gate near the gate edge (red arrow). The picture on the right shows an enlargement of the crack at the gate edge.

to some open questions that literature has still not completely explained. Despite the common acceptance over the last years on the *"critical voltage"* definition, a reverse-voltage at which the gate starts to degrade, it has been shown that gate failure can occur even for voltage levels significantly smaller than the critical one, just using sufficiently long stress times.

In particular, the experimental results have demonstrated that exposure to reverse-bias may induce:

- recoverable changes in the gate leakage and the threshold voltage, due to the accumulation of negative charge within the AlGaN layer, and of positive charge at the AlGaN/GaN interface, respectively;
- permanent gate degradation, due to the generation of parasitic paths for the leakage current conduction, clearly visible in EL images by means of the appearance of localized "hot" emission points at the gate-edge, at each increase of the leakage current.

Several findings support the hypothesis that permanent degradation is due to a defect generation and percolation process:

- for sufficiently long stress times, degradation occurs even below the *"critical voltage"* estimated by step-stress experiments;
- before permanent degradation occurs, gate current becomes noisy, indicating an increase in defect concentration in the AlGaN layer;
- time-to-breakdown strongly depends on the initial defectiveness of the samples, which enhances the creation of localized conductive paths.

From the explained model, the time-to-breakdown depends both on the applied stress voltage, and on the initial gate leakage level, that enhances the percolation process. In fact, devices with high initial defect density have shown a failure time significantly lower than identical devices with low defect density, exhibiting a power-law dependence between the time-to-breakdown and the initial gate leakage current. Moreover, the combined use of electrical and optical measurements have

allowed to follow the defects creation process and to better understand the traps involved in the recoverable performance changes, suggesting a relevant role of the donor-acceptor pair responsible for the yellow luminescence in GaN.

Failure analysis tools, guided by the electroluminescence emission images (EL), have also been used for a deeper investigation on the physical evolution of the damage, following recent results reported in the literature. The TEM analysis have allowed to verify the presence of pre-existent defects and only sometimes to identify the appearance of stress induced defects, highlighting the big difficulty and sometimes the impossibility to locate material cracks with nanometers-scale size on the semiconductor, at least at the early stages of device degradation, even using the guide provided by the EL images.

In conclusion, the collected evidences have confirmed the proposed model for the gate degradation and all the processes that lead the recoverable and non-recoverable variation of the device parameters, suggesting the reduced importance of the step-stress test evaluation and of the *critical voltage* definition.

But despite these meaningful results, few details needs to be further investigated, in particular to clarify the role of the temperature on this failure mechanism. Few authors have suggested a negative correlation between the gate degradation and the test temperature, whereas others have shown a small positive correlation. Nevertheless, independently on the trend, these results indicate that the conventional evaluation of the device life-time based on the three temperature-accelerated life-test is not appropriate for assessing this important degradation mechanism, due to the small or negligible temperature dependence of this damage that is visible even at room temperature. Therefore, despite the obtained results, further studies need to be performed to clearly understand this failure mechanism, and to unambiguously identify a criteria for the life-time evaluation suitable for all GaN-based HEMTs which take into account even the gate-degradation mechanism.

Moreover, to confirm both the model that explains the time-dependent behavior of the GaN HEMTs, and the dependence of the failure time with the initial defect density, the statistics of the tested samples can be increased trying to check the power-law dependence even for devices with different layout (for example with

different gate-length or gate-width). In fact, if the leakage current is only due to a vertical leakage component and not to parasitic surface leakage paths, the increase of the gate area will lead to an increase of the leakage current, and consequently will probably increase the defect density that enhances the defect generation and percolation process.

Chapter 5

Parasitic effects in GaN HEMTs

In the previous chapters it has been analyzed the reliability behaviour of different GaN-HEMT technology, with the aim of identifying the degradation mechanisms that permanently reduce the device performances and consequently decrease the predicted maximum life-time. Next to these non-recoverable mechanisms, there exist many other recoverable effects that can affect the static or the dynamic performances already in the untreated devices, or that can reduce the dynamic characteristics along the time due to the severe stress conditions at which device is working on. All these effects, called *trapping effects* or *parasitic effects*, are caused by the presence or the generation of available energy-states in the semiconductor energy-gap, that act as traps for electrons or holes coming from the channel and from the gate contact. These traps are typically associated to crystal imperfections or interruptions, like on the hetero-interfaces, and to atom displacement or impurity presence inside each layer of the GaN-HEMT structure.

The presence of these energy-states in regions where the carriers are flowing, or in regions that can be reached thanks to the operative electric-field condition, creates trapping-detrapping mechanisms that can deeply degrade the device performances. Depending on the time constant of the trapping and of the detrapping process, the parasitic effect can be really slow, affecting even the DC characteristics of the device, or quite fast, reducing only the dynamic or the RF performances. On the other hand, a slow effect can have negligible consequences on the RF behaviour of a device, due to the impossibility of the traps to follow the fast sweep of the

applied voltage or current.

The correlation between a parasitic effect and the trap responsible of this particular parasitic effect is typically not so simple, in term of both the identification of the exact trap activation-energy inside the energy gap, and the identification of the exact position inside the GaN-HEMT structure. Nevertheless, deep investigations using electrical measurements, optical measurements, and thermal analysis, allow to identify the trap behaviour, associating the final electrical parasitic effect with a particular trap location.

In fact, during this PhD activity, several times the use of combined electrical, optical or spectroscopy techniques have allowed to better understand the transient behaviour associated with a particular trapping effect, native on a device technology, or induced by a particular stress condition. In particular, in this chapter it will be shown the results gathered from two deep investigations of typical GaN-HEMT parasitic effects, the *kink effect* and the *current collapse effect*. These activities have been performed before and during the first part of the European project *MANGA* (Manufacturable GaN), inside the *"Preliminary deep levels characterization in materials and test structures"* work-package. This project follows the objectives of the previous KorriGaN project, sustaining the industrial development of semi-insulating silicon carbide substrates (Semi-Insulating SiC) and proving the industrial capability of Europe to deliver GaN-HEMT and MMIC foundries with state-of-the-art GaN HEMT epitaxial wafers on SI-SiC substrates. The aforementioned work-package, in particular, aimed at evaluating the correlation between these parasitic effects and particular epitaxy or processing procedures.

More precisely, the first part of the chapter will show a combined electro-optical analysis which have allowed to better understand the origin of the *kink effect*, correlating this effect with the electron interaction with the GaN-traps responsible of the yellow-luminescence. In the second part, a brief analysis on particular Fe-doped GaN devices have allowed to correlate the presence of Fe-doping in the buffer layer with an increase of the *current collapse effect*, especially at the high electric-field bias points.

5.1 Kink effect analysis

The *kink effect* is a slow trapping effect that induces a reduction of the drain current at low drain voltages (V_{DS}). This effect is typically originated by a buildup (at low V_{DS}) and subsequent release (at high V_{DS}) of negative charge, resulting in a shift of the pinch-off voltage toward more negative voltages and in a sudden increase of the drain current. This variation of the DC output characteristic can cause a degradation of other main parameters (like the transconductance or the on-resistance) and can even affect the dynamic behaviour, causing a strong dynamic compression depending on the chosen bias point.

In this work, a combined electro-optical analysis has been used to better understand the origin of the kink effect and the physical correlation with the traps responsible of this effect. In particular, investigating the physical mechanisms responsible for the luminescence of the AlGaN/GaN HEMTs, it has been observed a strong correlation between the kink appearance and few parasitic luminescence bands superimposed to the electroluminescence (EL) Maxwellian spectrum.

Tests have been performed on a not recent GaN-HEMT technology, particularly affected by the kink effect. Devices have been grown on a 4H-SiC wafer, with a standard AlGaN/GaN heterostructure: GaN buffer layer of 1.2 μm, followed by an AlGaN barrier layer of 30 nm, with 28% Al content. Contacts have been based on Ti/Al/Pt/Au for the Ohmic contacts at drain and source, and on Ni/Au for the Schottky contact at the gate. Finally, devices have been passivated with 90 nm of SiN, deposited by plasma-enhanced chemical vapor deposition (PECVD). Tested device have a gate length of 0.6 μm, a gate width of 100 μm, a drain-source distance of 5 μm, and a gate-drain distance of 3.4 μm. The significant results on the *kink analysis* have been achieved by the introduction, next to the standard electrical characterization, of spectrally resolved EL measurements, carried out by means of a cooled charge-coupled device camera equipped with a filter-based monochromator, mounted on an optical microscope. The whole system has been calibrated in the 420-720 nm spectral region.

5.1.1 Electro-luminescence investigation

Recently, it has been shown that electroluminescence (EL) measurements can constitute a powerful tool for the investigation of the properties of AlGaN/GaN HEMTs: HEMTs can emit a weak EL signal when they are submitted to on-state operation [61, 62], as it has already seen and considered on the reliability analysis on previous chapter 2. The analysis of the EL signal can provide important information on the distribution and the intensity of the electric field [81], and on the energetic distribution of the electrons in the channel [63]. Furthermore, the EL signal can be analyzed before and after aging tests, in order to achieve information on the physical mechanisms responsible for the degradation of GaN HEMTs [54, 63].

Luminescence in HEMTs is usually ascribed to intra-band transitions involving highly energetic electrons, as proposed by *Shigekawa et al.* in [61] and [62]. In particular, these reports point out that EL in GaN HEMTs is not due to band-to-band recombination, while it is generated by hot electrons accelerated by the longitudinal electric field present in the channel. Radiation is hence emitted through *Bremsstrahlung process*, due to the deceleration of electrons at charged centers.

The output characteristic (drain current versus drain voltage) of the tested samples is shown in figure 5.1. In this diagram it can be observed that the maximum drain current, measured at $V_{GS} = 0V$, is around 1 A/mm, with a threshold voltage of -5.2 V. As underlined by the two blue vertical lines, this GaN technology exhibits a visible *kink effect* that decreases the drain current at voltage lower than a certain V_{DS} value. The first blue line (at $V_{DS} = 6V$) is placed in the region before the *kink-knee*, here located around $V_{DS} = 8V$, whereas the second line (at $V_{DS} = 12V$) is placed completely above the *kink-knee*.

The emission behaviour at different gate voltages and drain voltages is shown in figure 5.2 and figure 5.3 respectively, confirming that GaN HEMTs emit a weak luminescence signal when biased in on-state condition. The EL intensity has been obtained by integrating the EL signal on the whole active area; this area corresponds, more or less, to the region visible in figure 5.4.

Figure 5.4 reports the false-color luminescence map of the EL emission peak superimposed to the optical picture of the device active area. This figure shows

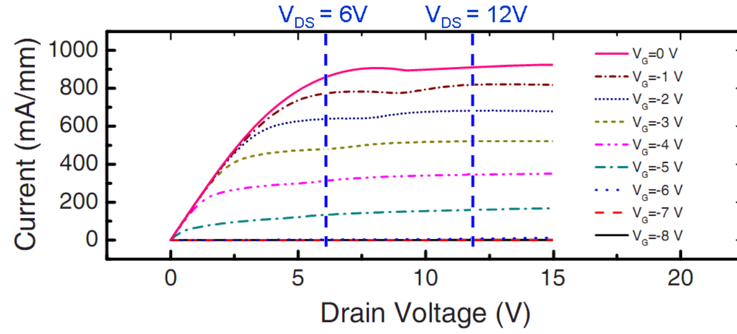


Figure 5.1: $I_D - V_D$ output characteristic of one of the analyzed samples. *Kink-knee* located around $V_{DS} = 8V$.

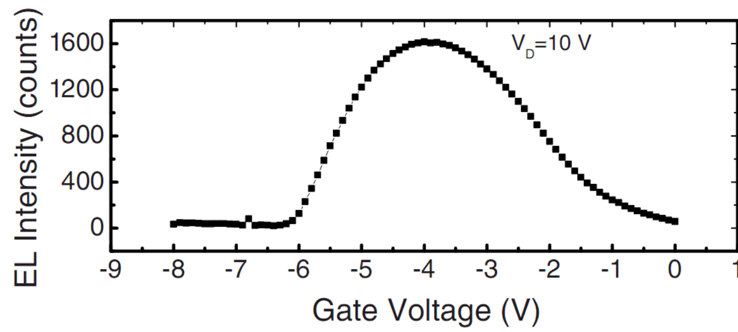


Figure 5.2: Integrated EL intensity vs. gate voltage, measured with a drain voltage $V_{DS} = 10V$ on one of the analyzed samples.

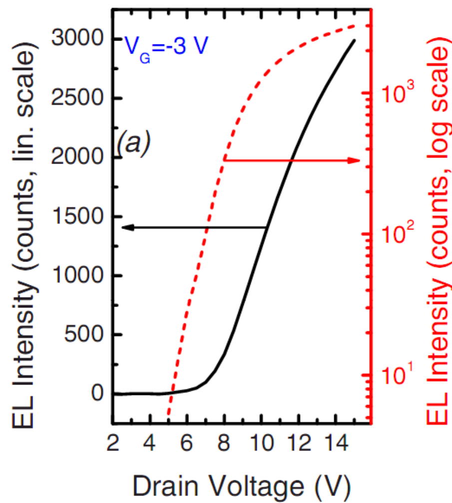


Figure 5.3: Integrated EL intensity as a function of drain voltage, for one of the AlGaN/GaN HEMTs analyzed within this work. In particular, the left axis refers to the linear-scaled curve (black curve) and the right axis refers to the log-scaled curve (the red curve). Measurements have been taken at a gate voltage $V_{GS} = -3V$.

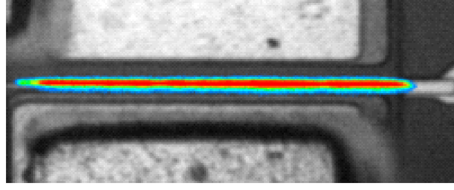


Figure 5.4: False-colors emission microscopy image of one of the analyzed devices, showing the distribution of EL intensity along the channel. The two contacts on top and on bottom of the gate are the drain and the source contacts respectively.

that the EL signal is generated all over the width of the gate finger, in proximity of the edge of the gate located toward the drain, the region where the electric field in the channel is maximum, and consequently where the hot-electron effects are more pronounced. The intensity of the luminescence signal is proportional to the number of electrons flowing into the channel (and therefore to the drain current), and to the probability of each carrier to emit a photon, which is a function of the maximum electric field.

As already described on the theory chapter, figure 5.2 shows the bell-shaped behaviour of the EL signal at different gate voltage levels V_{GS}, highlighting the influence and the opposite contribution of carrier density and electric-field on the emission process. To explain the effect, this diagram can be divided in three main regions:

1. for gate voltage levels smaller than -6V, no current flows through the channel (negligible contribution of the carrier density) and the EL signal is, therefore, absent;

2. for gate voltages between -6V and -4V, current starts flowing in the channel (increasing the carrier density contribution) and hot-electron luminescence signal increases with the gate-voltage level, linearly with the drain current level;

3. further increasing the gate voltage beyond -4V, the accelerating electric-field starts decreasing, due to the reduction of the drain-to-gate voltage, inducing a significant decrease in the EL signal.

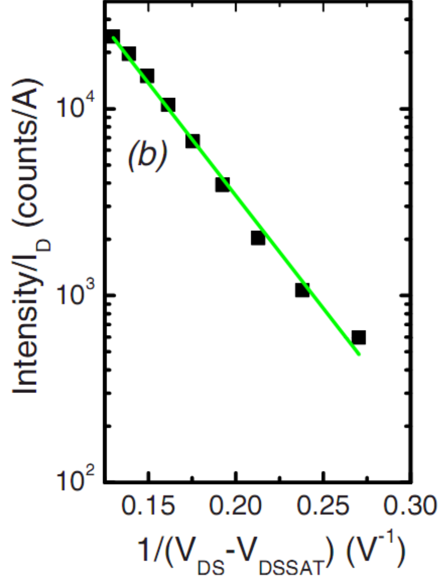


Figure 5.5: EL-Intensity/I_D ratio plotted as a function of $1/(V_{DS} - V_{DSsat})$. Measurements taken at $V_{GS} = -3V$.

These opposite contributions create the typical bell-shaped behaviour, with a peak strongly dependent on the device technology, here located at V_{GS} from -4 to -3V.

Looking at the dependence of the EL intensity versus the drain voltage, as shown in figure 5.3, it can be noticed a well different behaviour, indicating the strong influence of the drain voltage, and in particular of the drain-gate voltage, on the EL signal. The dependence of the luminescence intensity on the accelerating field is better described by the diagram in figure 5.5, that reports in a semilogarithmic scale the ratio between the intensity of the EL signal and the drain current (Intensity/I_D ratio) as a function of the reciprocal of $(V_{DS} - V_{DSsat})$: the first represents a quantity related to the probability of electrons to emit photons, whereas the second represents a measurable quantity which is directly proportional to the accelerating field $\mathcal{E}$ (V_{DSsat} is the saturation drain voltage at the particular V_{GS}).

As can be noticed, the logarithm of the Intensity/I_D ratio has a linear dependence on the reciprocal of the accelerating field.

$$log(Intensity/I_D) \sim -1/\mathcal{E}$$

This result is consistent with previous reports [63, 67, 82], and is commonly considered as a signature of the fact that the luminescence signal is generated by hot

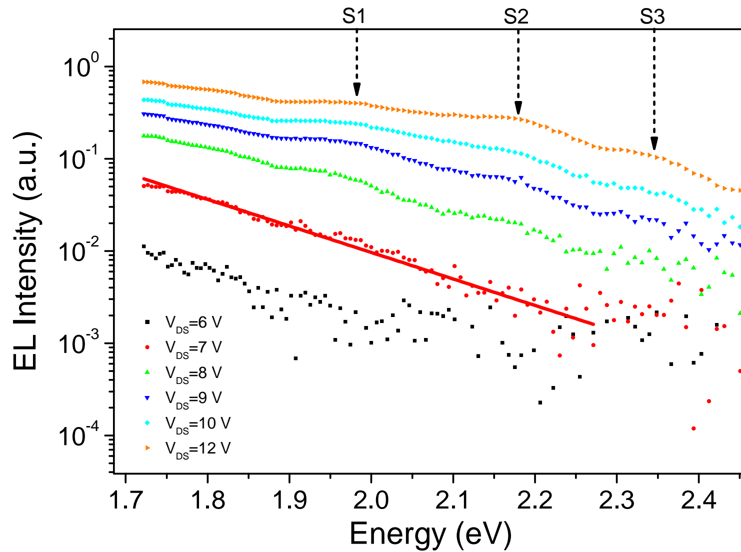


Figure 5.6: EL spectra measured on one of the analyzed HEMTs at different drain voltage levels, with a gate voltage $V_{GS} = -3V$.

electrons.

Following analysis have been focused on the electroluminescence spectra measured on one of the previous analyzed devices, using different drain voltages and fixing the gate voltage at -3V close to the peak of the emission intensity. As reported in figure 5.6, the EL spectra show two different behaviours, depending on the applied drain voltage level. For low drain voltages ($V_{DS} < 8V$), correspondent to the region before the *kink*, the EL spectra have a Maxwellian shape, i.e. the EL intensity has an exponential dependence on photon energy. A Maxwellian spectrum is typical for hot-electron luminescence, since it reflects the energy distribution of the accelerated electrons in the channel, following the physical relation $exp(-E/kT)$, where E is the electron energy, k is the Boltzmann constant, and T represents the temperature [63, 82]. From the slope of the semilogarithmic EL versus Energy curve, it is possible to extrapolate the equivalent temperature of the electrons in the channel. As an example, for the device in figure 5.6, the electron temperature at the drain voltage of 7V is equal to 1900 K (see the red line).

For drain voltages greater than 8V (the region above the *kink*), the EL spectra of the devices show a more interesting feature, represented by the increase in the emission intensity in the yellow-red spectral range, the spectral region between 2

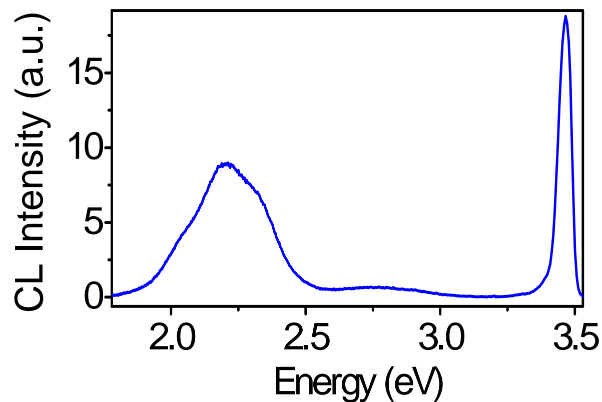


Figure 5.7: Cathodo-luminescence CL spectrum measured at 77 K on one of the analyzed samples. The peak at the highest energy (at 3.47 eV) is related to the near band-edge emission of Gallium Nitride; on the left, the broad peak centered around 2.2 eV is related to the parasitic yellow emission band of GaN.

and 2.4 eV. This is particularly evident for the curves measured with a drain voltage of 10 and 12V reported in figure 5.6, the light-blue and orange curves respectively.

In order to understand the origin of this behavior, Cathodo-luminescence (CL) measurements have been carried out on the devices under analysis, by means of a Cambridge S360 Scanning Electron Microscope, equipped with a Gatan MONOCL2 system and a multialkali photomultiplier. The CL spectrum of the analyzed devices consists in three main peaks, as reported in figure 5.7. The peak at the highest energy, centered at 3.47 eV, is related to the near band-edge emission of Gallium Nitride. On the other hand, the peak centered at 2.75 eV represents the characteristic blue emission band of GaN. Finally, the broad peak centered around 2.2 eV is related to the parasitic yellow emission band of GaN, which is usually attributed to the radiative transition between a shallow donor state and a deep acceptor state located about 0.9 eV above the valence band [76, 77].

The presence of such a pronounced yellow luminescence peak suggests the following interpretation for the measured EL data reported in figure 5.6: when an HEMT is biased in on-state, with a moderate drain voltage ($V_{DS} < 8V$), the device emits light due to hot-electron effects, and the EL spectrum has a Maxwellian shape. When the drain bias is increased above a certain threshold value quite close

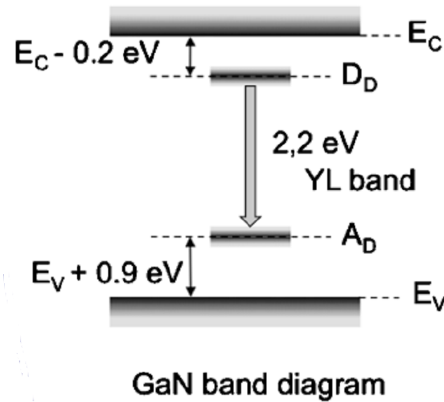


Figure 5.8: Schematic GaN band diagram indicating the deep donor levels (D_D) and the deep acceptor levels (A_D) involved in the electron transitions responsible of the yellow luminescence [77].

to the *kink-knee* ($V_{DS} > 8V$ for the technology under analysis), electrons in the channel can achieve enough energy to induce the detrapping, by impact ionization, of the deep acceptor level responsible for the yellow luminescence, which is normally filled with electrons [42] (see figure 5.8). As a consequence, for high drain voltage levels, the occurrence of radiative yellow recombination can be favored due to the availability of free acceptor states, explaining the presence of a broad yellowish emission superimposed to the Maxwellian distribution coming from the hot electrons. This effect should be obviously more pronounced for HEMTs grown on wafers showing a strong yellow cathodoluminescence or photoluminescence signal, and is therefore related to the quality of the epitaxial process.

Moreover, the yellow luminescence band in figure 5.6 seems to show the presence of three characteristic sub-bands, referred to S1, S2, and S3 in this figure. These features are also visible in the CL diagram in figure 5.9, where the sum of three gaussian contributions fit the experimental broad yellow peak. This result can be explained by the fact that yellow luminescence is due to the superposition of more than one radiative transition between 2 and 2.3 eV, involving deep acceptor states with similar energies, possibly related to the presence of gallium vacancies [69, 76], or to carrier-phonon interaction processes [83].

In summary, the EL analysis of *kink-affected* AlGaN/GaN HEMT devices have shown that for low drain voltage levels, HEMTs can shown a weak luminescence sig-

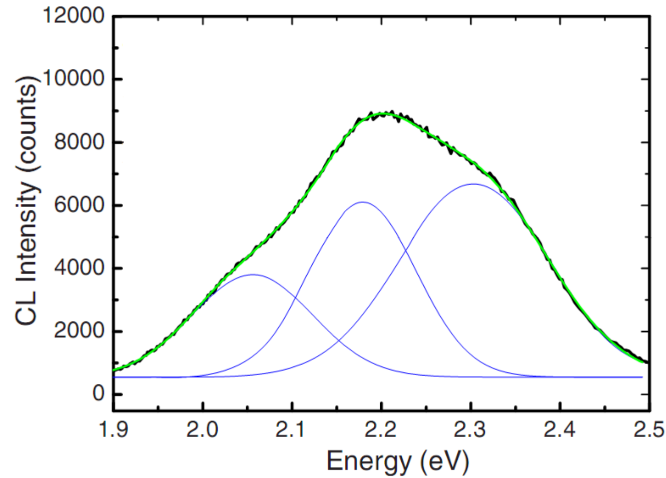


Figure 5.9: Enlargement of the CL spectrum measured at 77 K on one of the analyzed samples, for the spectral region between 1.9 and 2.5 eV. The black curve reports the experimental data, while the green curve represents a three-peaks Gaussian fit of the experimental data (the individual Gaussian functions are plotted in blue in the graph).

nal which is related to the presence of hot electrons, as described by the Maxwellian shape of the EL spectra. Moreover, by the analysis of this spectrum it is possible to extrapolate the equivalent temperature of the electrons in the channel. On the other hand, for high drain voltage levels, the EL spectra show the presence of parasitic luminescence bands, superimposed to the Maxwellian spectrum generated by the hot carriers. The parasitic luminescence bands have been correlated with the presence of highly-accelerated carriers that can promote the occurrence of parasitic radiative transitions, possibly as a consequence of de-trapping of the acceptor-like states responsible for the yellow luminescence in GaN. This hypothesis is supported by the comparison between measured EL and CL data. A direct consequence of the measured spectra is that for high drain voltage levels the shape of the EL spectrum is significantly modified with respect to the conventional Maxwellian shape, and the evaluation of the equivalent electron temperature can not be carried out by the simple analysis of the slope of the semilogarithmic EL versus Energy plot.

Due to the strong correspondence between the change of the EL spectrum and the *kink* event, it can be suggested that the occurrence of the *kink* is strongly related to the presence of this parasitic bands. As a consequence, when the drain

voltage is increased above a certain voltage depending on the traps position and on the local electric-field intensity, the electrons in the channel can achieve enough energy to induce detrapping of the deep acceptor levels responsible for the yellow luminescence in the GaN layer, causing the sudden threshold-voltage left shift and the occurrence of the *kink* in the drain current. With this assumption, more intense yellow-contribution on the EL signal corresponds to a more pronounced kink effect in the drain current output characteristic.

Therefore, a deep analysis of the luminescence properties of this devices have allowed to physically explain the parasitic kink effect in the output curves, suggesting a simple technique for the characterization of the trapping effect by means of the electroluminescence spectra, and for the evaluation of the wafer quality even at the early stages of device processing, by means of the cathodoluminescence (CL) or photoluminescence (PL) analysis.

5.2 Current collapse effect in Fe-doped HEMTs

The *current collapse* is a trapping effect that causes a reduction of the maximum dynamic drain current and, as a consequence, a decrease of the RF performances of the tested device. It is typically associated, mainly in the early generations of GaN-HEMT devices, to the accumulation of negative charge on the surface traps and following depletion of the channel region below these traps, with an effect similar to a virtual gate located next to the real gate but controlled by the traps charge [44]. The transient effect can be quite slow or pretty fast depending on the dept of the traps and of its location in the HEMT structure. But in the recent device technologies, this effect has been really much reduced thanks to improved passivation processing, which creates a near-optimal dielectric-semiconductor interface preventing electron access to the surface traps, or to different field-plate topologies, which reduce the electric-field peak at the gate-edge decreasing the electron energy required to reach the surface traps.

Despite the technology improvements, the continuous growth of the drain voltage maximum capability increases the electric-field peak and therefore requires device processing step by step more robust against the current collapse effect. Furthermore, the really high electric-field existent in the active area and, in particular, in the channel region, can give enough energy to channel electrons for being trapped even in the buffer layer.

In particular, in this work it has been analyzed the parasitic effect induced by the iron-doping (Fe-doping) in the GaN buffer layer. In fact, iron is often used as a dopant in the GaN layer in order to obtain the semi-insulating GaN. Semi-insulating buffers are important in any lateral device, like GaN HEMTs, to achieve good pinch-off characteristics, low output conductances and low parasitic currents or leakage currents. For example, *Heikman et al.* [84] have shown that iron can be effectively used in order to form semi-insulating GaN layers. Nevertheless, the drawback of a doping material in a region close to the channel is that it can induce parasitic traps that can be filled by the highly-energetic electrons flowing in the 2DEG. *Desmaris et al.* [85] have shown that GaN HEMTs fabricated on Fe-doped GaN buffer can suffer from severe performance degradation when compared to

those fabricated on undoped GaN layers. However, this report does not exhibit any activation-energy extraction neither a study on the dependence of the current collapse from the Fe-doping profile.

The availability of different wafers with the same processing but with different doping concentrations allows to investigate the dependence of the current collapse in GaN HEMTs from the profile of the Fe-doped semi-insulating GaN buffers, demonstrating the correlation between the Fe-doping profile and the magnitude of the drain current compression.

Tests have been performed on six wafers processed inside the *"deep-level identification"* work-package of *MANGA* project. The wafers have been grown with different heterostructure characteristics, but with the same device processing, made by Selex Sistemi Integrati. As reported in table 5.1, wafers have been divided in two groups: the first has a thicker AlGaN barrier and a higher Aluminum content, compared with the second group. All wafers have a Fe-doped GaN layer, with different dopant concentrations and profiles, unless the last wafer of the following list. Moreover, wafers of the first group are nominally and experimentally identical; on the other hand, wafers of the second group have been grown with decreasing Fe concentration (from 4×10^{17} cm^{-3} to 0 cm^{-3}) based, more or less, on the same AlGaN/GaN heterostructure. Tested devices have a gate-length of 0.5 μm, gate-source distance of 1.25 μm, and gate-drain distance of 2.25 μm. All wafers present the same SiN surface passivation.

5.2.1 Dynamic measurements

To understand the trapping effect induced by the different buffer doping, dynamic tests have been performed by means of a custom double-pulse measurement system. This system is able to provide synchronized pulses at the gate and at the drain of the device under test starting from arbitrary quiescent points, in order to evaluate and compare the current collapse among different wafers. Pulse width and pulse period have been set to 1 μs and 100 μs respectively. In particular, multiple quiescent points, or baselines, have been used:

- the baseline at $V_G = 0V$ and $V_D = 0V$, that does not enhance any trapping

ID Selex	SiC type	d AlGaN (nm)	AlGaN (Al%)	d buffer (μm)	Fe-doping (cm^{-3})
SLX CA-04	4H	26	0.29	1.8	1E+18
SLX CA-02	4H	26	0.29	1.8	1E+18
SLX IA-01	6H	20	0.25	1.9	4E+17
SLX ID-01	6H	20	0.25	1.9	2E+17
SLX IC-01	6H	20	0.25	1.9	1E+17
SLX NC-03	4H	20	0.25	2.4	0

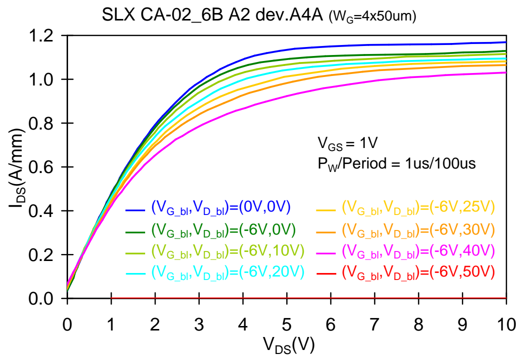
Table 5.1: Characteristics of the MANGA tested wafers, in term of heterostructure composition and buffer doping.

process, due to the absence of any electric field at the quiescent point;

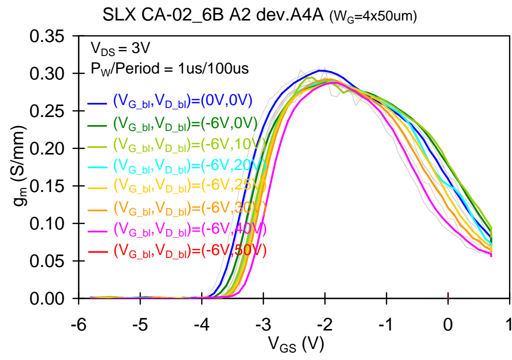
- a baseline at $V_G = -6V$ and $V_D = 0V$, an intermediate baseline that increases the trapping especially in the gate region;
- other baselines at fixed $V_G = -6V$ but at increasing V_D values (from 10V to 40V), that enhance the trapping effect due to the increase of the drain-to-gate electric-field.

In figure 5.10 are reported the pulsed output and the pulsed transconductance characteristics of one typical sample of the first group of wafers (SLX CA-02), and two samples coming from the second group. In particular one from the middle-doped wafer (SLX IA-01) and one from the un-doped wafer (SLX NC-03).

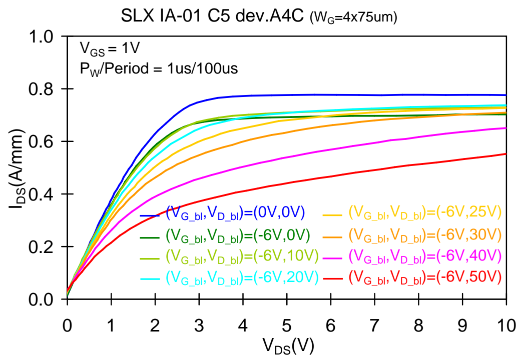
Despite the highest Fe-doping concentration, CA wafers (first group) have shown a limited current collapse effect, comparable to the un-doped wafer. On the other hand, the three wafers named SLX IA-01, SLX IC-01 and SLX ID-01 have shown a significant reduction of the dynamic output current, quite uniform inside the wafer (see figure 5.10). Moreover, even in this case, the different Fe-doping concentration are not correlated with the different observed current collapse effect. The main cause of the collapse is a threshold voltage shift toward more positive values, as reported by the dynamic transconductance curves in figures 5.10 (b), (d) and (f). This shift is exhibited by all the tested wafers, sign of traps principally



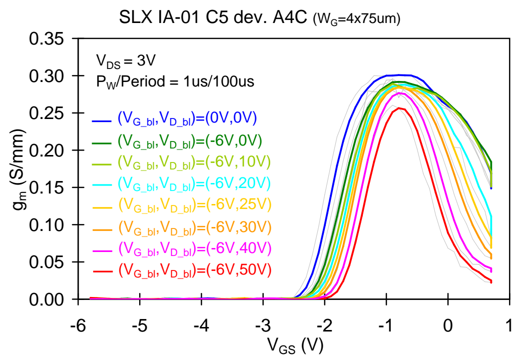
(a) pulsed output characteristic



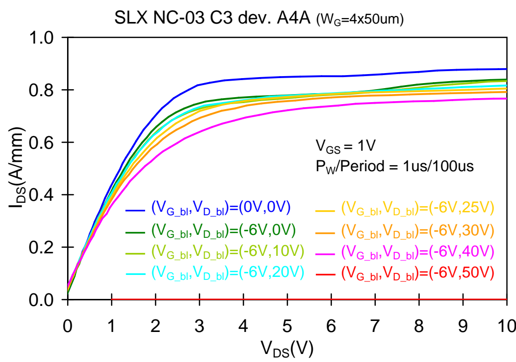
(b) pulsed transconductance



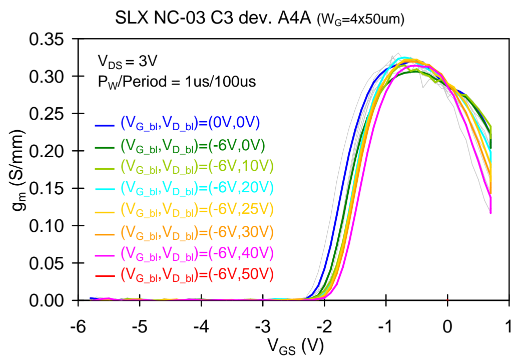
(c) pulsed output characteristic



(d) pulsed transconductance



(e) pulsed output characteristic



(f) pulsed transconductance

Figure 5.10: Pulsed characteristics at different V_D baselines on a typical device of wafer SLX CA-02 of the first group ((a) and (b)), and of wafers SLX IA-01 ((c) and (d)), and SLX NC-03 ((e) and (f)) of the second group. Output curves at $V_G = 1V$ and transconductance curves at $V_D = 3V$.

placed below the gate [65], maybe correlated to the device processing. On the contrary, only on wafers SLX IA-01, SLX IC-01 and SLX ID-01 the transconductance shows a reduction of its characteristic at high V_{GS}, suggesting trapping in the access region; only sometimes it is visible a reduction of the transconductance peak as well. The bigger the transconductance reduction at high V_{GS} values, the worse the pulsed characteristics.

As already described in the previous chapters, to quantify and compare the current collapse effect on different wafers, it can be extracted a parameter called *Slump Ratio* (S.R.), obtained by the ratio between the drain current of a "trapped" quiescent point and the drain current of the "un-trapped" quiescent point ($V_G = 0V$, $V_D = 0V$). This parameter give the residual drain current in pulsed conditions, while the amount of the collapse is given by $1 - S.R.$.

$$S.R. = \frac{I_{DSsat}(V_G = -6V, V_D = Vdd)}{I_{DSsat}(V_G = 0V, V_D = 0V)} \quad \text{with } I_{DSsat} \text{ at } V_{GS} = 1V \text{ and } V_{DS} = 10V$$

As shown in figure 5.11, devices from wafers SLX IA-01, SLX IC-01 and SLX ID-01 show the highest collapse, with a Slump Ratio from 55 to 70%. On the other hand, devices from wafers SLX CA (CA-02 and CA-04) show a lower collapse (S.R.≈80%), quite similar to devices of the last un-doped wafer (SLX NC-03), which show more or less the same current collapse effect (S.R.≈78%). These results suggest that the mechanism causing the observed different current compression is probably related to the device material rather than the fabrication process (identical in all wafers). The latter can be only responsible of the small threshold voltage shift visible on all the wafers.

To better understand the reason of the increased collapse only on the three SLX_I wafers (IA-01, IC-01 and ID-01), a detailed analysis has been carried out in collaboration with the University of Modena and Reggio Emilia, by means of an estimation of the activation energy of the trap responsible of this parasitic effect, and subsequent numerical simulations to confirm the experimental results. In particular, tests have mainly been carried out on wafer SLX CA-02, representative of the first wafers group, and on wafer SLX IA-01, which has shown a middle

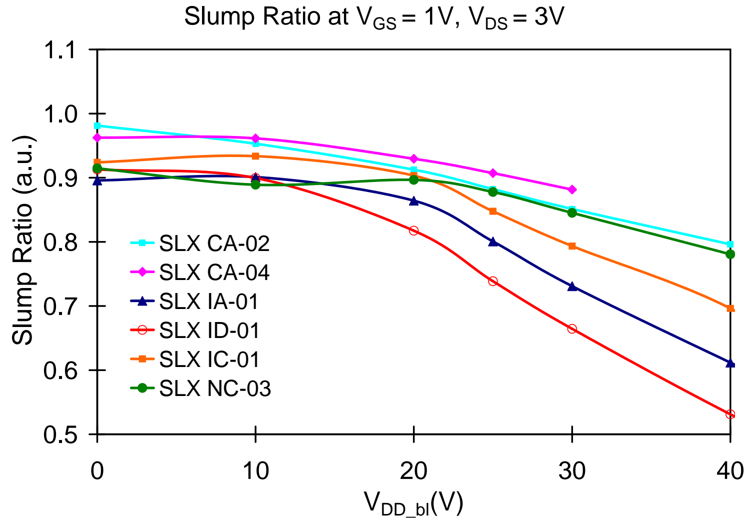


Figure 5.11: Slump ratios extracted at $V_{GS} = 1V$ and $V_{DS} = 3V$, for all tested wafers. All the measurements have been performed at the same gate baseline ($V_{Gbl} = -6V$) and at increasing drain baselines (reported on the x axis).

behaviour among SLX_I wafers.

The first step has consisted in a deep study of the trapping behaviour of collapsed devices by recording the turn-on transient obtained when pulsing the device from pinch-off condition, at different drain biases, to open channel condition. As can be seen in figure 5.12, the drain current transient is dominated by a trap level with a time constant in the order of 0.1 ms - 1 ms. Current transients recorded at different temperatures and mathematical fittings on the obtained curves yielded to an activation energy (E_A) of 0.57 eV for the trap responsible of the observed phenomenon, as reported in figure 5.13. Such activation energy has already been extracted in Fe-doped GaN devices and it has been associated to the presence of iron-doping within the GaN [86, 87]. A similar procedure applied to devices of wafer SLX NC-03 yielded a lower E_A of 0.3eV, while the level at 0.57 eV has not been observed, confirming the previous hypothesis.

Very similar results have been obtained in Padova tests, measuring the turn-on transients on devices from the same wafer SLX IA-01, with a final extracted activation energy of 0.602 eV, quite close to the previous reported 0.57 eV (see figure 5.14). As a consequence, it seems that the current collapse in wafers SLX CA and SLX_I is caused by the presence of iron in the GaN buffer layer and that the

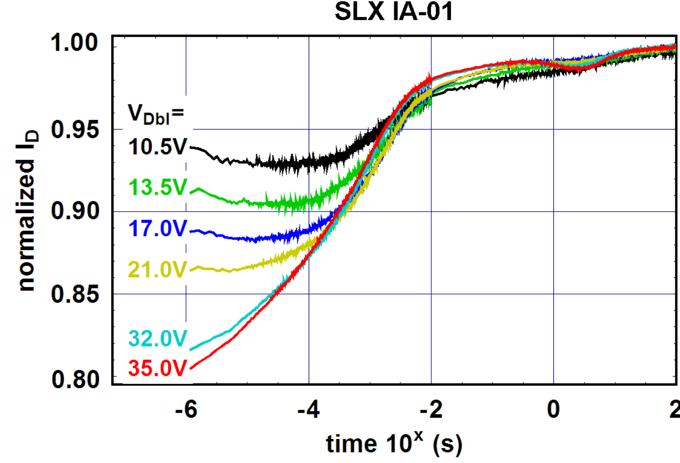


Figure 5.12: Typical drain current turn-on transients obtained from devices of wafer SLX IA-01. Currents are normalized with respect to the steady-state drain current level measured at $V_{DS} = 5V$ and $V_{GS} = 0V$. Current transient is dominated by a trap level with time constants in the 0.1 ms - 1 ms range.

difference between these wafers might be related to different iron-doping profiles instead of the different iron-doping concentrations.

5.2.2 SIMS measurements and numerical simulations

To investigate the correlation between the collapse and the doping profile, Secondary Ion Mass Spectroscopy (SIMS) measurements have been thus carried out on wafer SLX CA-02 and SLX IA-01, in order to evaluate the real iron-doping profiles. From these analysis, it has been observed that the maximum concentrations of the dopant are 4-times higher than the previous stated iron-doping concentrations. Moreover, looking at the iron profiles, wafer SLX IA-01 shows a maximum concentration of approximately 1.6×10^{18} cm^{-3} at the bottom of the GaN buffer, which slowly decays moving towards the hetero-interface to approximately 3×10^{16} cm^{-3} (see figure 5.15). On the other hand, wafer SLX CA-02 presents an higher iron concentration approximately of 4×10^{18} cm^{-3}, that remains quite constants from the bottom of the GaN buffer layer until approximately 800 nm from the AlGaN/GaN interface. From this point, the concentration sharply decays when moving towards the AlGaN/GaN interface, where the iron concentration goes below the SIMS detection limit, as reported in figure 5.16.

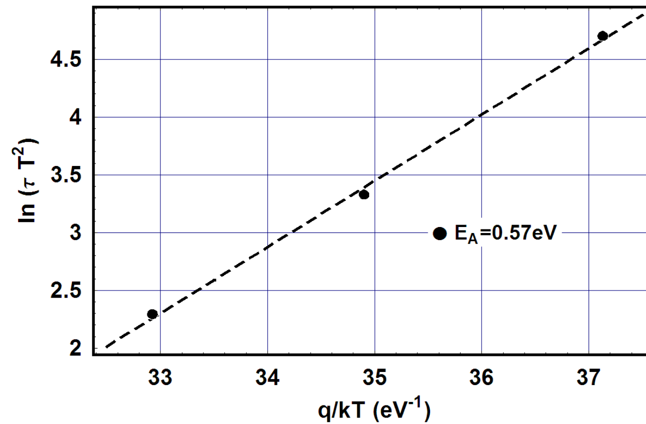
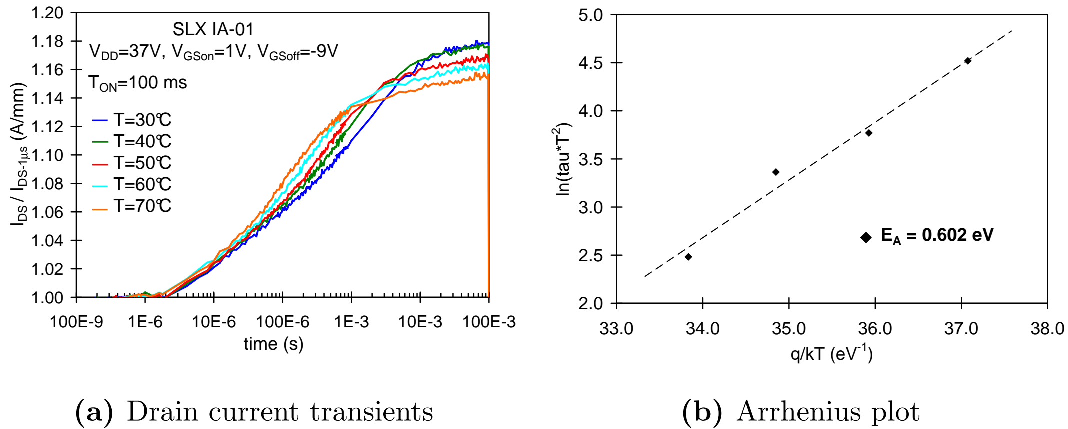


Figure 5.13: Arrhenius plot extracted from drain current turn-on transient at different temperatures, carried out on devices of wafer SLX IA-01. An activation energy of 0.57 eV is extracted and it has been associated to the iron which has been used to dope the GaN buffer layer in wafers SLX_I and wafers SLX CA.



(a) Drain current transients

(b) Arrhenius plot

Figure 5.14: Drain current turn-on transients (a) and corresponding Arrhenius plot (b) obtained from devices of wafer SLX IA-01, in Padova measurements. Currents are normalized with respect to the initial drain current level at T = 1 μs measured at $V_{DS} = 4V$ and $V_{GS} = 1V$. An activation energy of 0.602 eV is extracted.

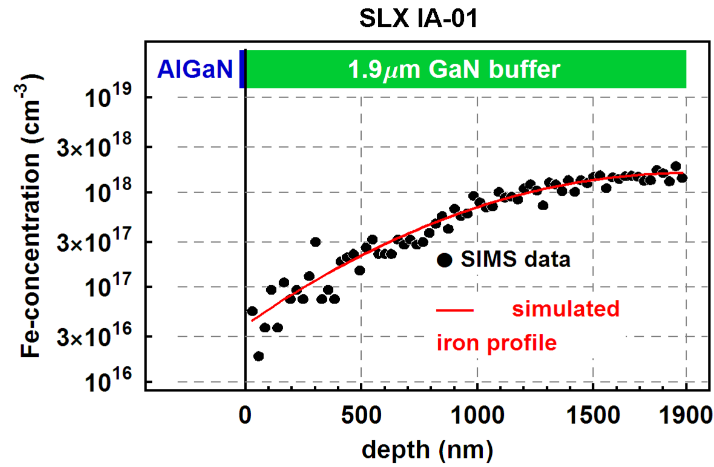


Figure 5.15: Iron concentration profile within the GaN buffer layer of wafer SLX IA-01. Closed symbols represents the experimental data obtained by SIMS measurements, while the red line represents the concentration profile used during numerical simulations of the devices from this wafer.

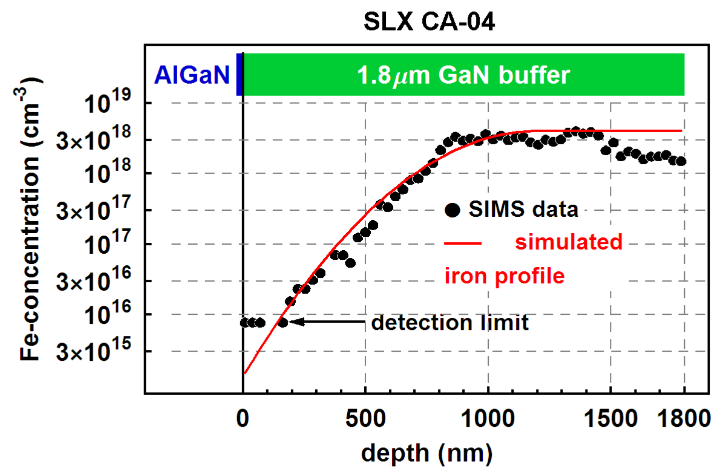


Figure 5.16: Iron concentration profile within the GaN buffer layer of wafer SLX CA-02. Closed symbols represents the experimental data obtained by SIMS measurements, while the red line represents the concentration profile used during numerical simulations of the devices from this wafer.

These results confirm the previous hypothesis. In fact, the higher Fe-doping concentration in SLX CA-02 wafer is not reflected into a higher iron presence in the channel region, explaining the very similar dynamic behaviour of this wafer compared with the un-doped wafer. On the other hand, wafer SLX IA-01 starts from a lower Fe-doping concentration at the bottom of the GaN buffer, but it keeps a higher Fe concentration close to the channel, suggesting a possible role of the dopant in the increase of the current collapse effect.

To support this hypothesis, the measured SIMS profiles have been used inside numerical simulation analysis, in order to physically explain the correlation between the different Fe-doping presence in the GaN buffer with the different dynamic performances, in term of transient behaviour and pulsed characteristics. Iron doping has been simulated as an acceptor trap located at 0.57 eV from the conduction band, with a concentration that has been tailored in order to fit the experimental SIMS data, as reported on the red lines in figures 5.15 and 5.16. In figure 5.17 is depicted the normalized drain current transients obtained for the two different wafer options, starting from the same bias point used for the turn-on transient experimental measurements ($V_{GS} < V_{TH}$ and $V_{DS} = 40V$). As reported on this diagram, simulated device of wafer SLX IA-01 exhibits a larger drain current collapse (approximately 22%), compared to the simulated device of wafer SLX CA-02, which experienced approximately a 12% of drain current compression. Furthermore, comparing the simulated complete dynamic characteristics (starting from the same high-field quiescent point) with the static ones, it can be noticed that both devices from wafer SLX IA-01 and SLX CA-02 experience some current collapse effects, although these phenomena are more severe for devices of the first wafer (see figure 5.18).

These simulations demonstrate that devices of wafer SLX IA-01 are affected by a larger current collapse effect with respect to those of wafer SLX CA-02, in agreement with the measured data, underlining the role of the Fe-doping profile in the device dynamic characteristics, and the importance of a correct control of that profile on semi-insulating GaN buffers, in order to obtain high performance GaN HEMTs.

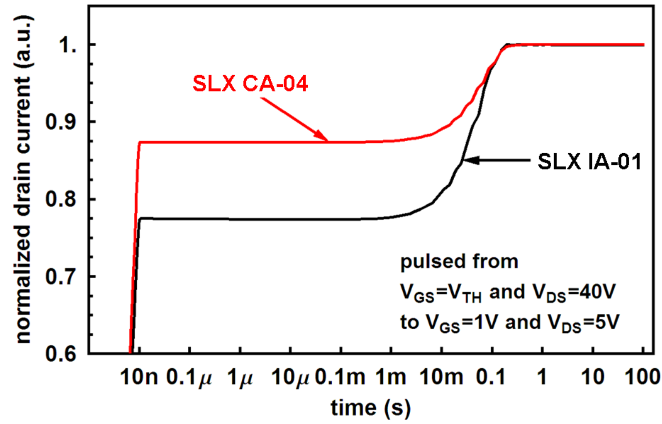


Figure 5.17: Normalized drain current transients obtained when pulsing both the gate and the drain terminal from $V_{GS} = V_{TH}$ and $V_{DS} = 40V$, to $V_{GS} = 1V$ and $V_{DS} = 5V$. The two voltage pulses are applied simultaneously to the simulated device, with a rise-time of the voltage pulse of 10ns.

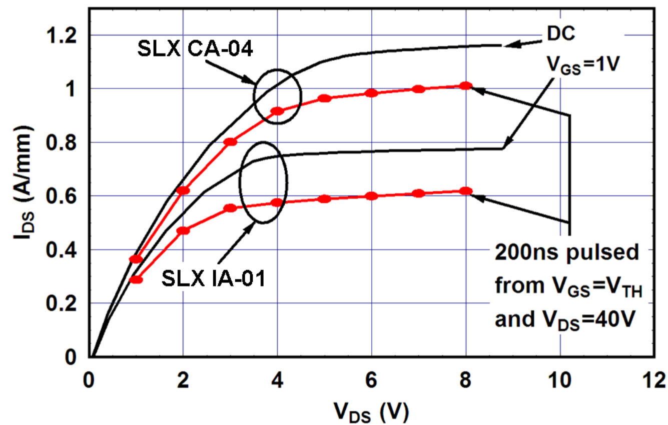


Figure 5.18: Comparison among simulated DC characteristics at $V_{GS} = 1V$ (solid lines), and simulated dynamic characteristics obtained by pulsing both gate and drain terminals from a high-trapping quiescent point ($V_{GS} = V_{TH}$ and $V_{DS} = 40V$; 200 ns pulses) (closed symbols-red line), for a device from wafer SLX IA-01 and one from wafer SLX CA-02.

In conclusion, it has been shown that AlGaN/GaN HEMTs grown on a Fe-doped GaN layer can be affected by reduced dynamic performances. The use of simple transient measurements at different temperatures have allowed to understand the activation energy of the trap responsible of the current collapse, suggesting a possible role of the iron-doping close to the channel, as reported by other studies in the literature. Nevertheless, it has been observed that the only dopant concentration value available from the epi-supplier is not sufficient to understand or to predict the dynamic behaviour of tested devices. SIMS measurements combined with numerical simulations (and the activation energy extracted on the previous analysis) have provided a better physical demonstration of the experimental data and have moreover been able to predict the experimental trend. At this point, the following step can be the execution of the same analysis on the other Fe-doped wafers, in particular on the remaining SLX_I wafers, in order to complete and confirm the experimental results and the theoretical assumptions, and to quantitatively correlate the doping profiles with the different Slump Ratio values measured during the pulsed tests.

As a result, simulation and doping-profile analysis have demonstrated to be very important tools both to design high-performance GaN HEMTs with excellent semi-insulating buffer layers, and to minimize the current collapse phenomena associated with the introduction of a dopant material, like iron in this case, in order to increase the insulating performances of the buffer layer.

5.3 Summary and conclusions

In this chapter, two deep investigations on parasitic effects have been reported, with a special focus on the *kink effect* and on the *current collapse effect*, respectively. The previous results have been accomplished by means of different techniques, using electrical measurements, optical measurements, spectroscopy analysis, and even numerical simulations, suggesting the necessity of different techniques and sometimes the combination of adapted capabilities in order to understand the particular behaviour of a slow trap, and the place where this trap is located.

In the first part, an electro-optical analysis of devices affected by the kink effect have allowed to correlate the presence of the *kink* with a parasitic increase of the EL emission spectrum in the range of the yellow-red band, correlated with a similar yellow broad-band peak in the cathodoluminescence measurements. The physical explanation of this emission feature is the following: when the drain voltage is increased above a certain voltage defined as the *kink-knee* voltage, the electrons in the channel can achieve enough energy to induce detrapping of the deep acceptor level responsible of the yellow luminescence in the GaN layer, causing the increase of a yellow-red parasitic band superimposed to the expected Maxwellian spectrum generated by the hot electrons. This detrapping can be the origin of the sudden threshold-voltage left shift and the subsequent occurrence of the *kink* in the drain current. Furthermore, this analysis have suggested a simple technique for the kink effect evaluation by means of the electroluminescence (EL) or cathodoluminescence (CL) spectra. In fact, testing the presence of yellow parasitic bands in CL or EL analysis allows to confirm the presence of this trapping effect even at the early stages of wafer processing, due to the assumption that the more intense is the yellow component, the more pronounced will be the kink effect in the drain current output characteristic.

In the second part, a deep analysis of the current collapse effect on Fe-doped AlGaN/GaN devices have allowed to correlate the increase of this effect (at the high electric-field quiescent points) with the presence of the iron doping in the GaN buffer layer, identifying the activation energy of the trap responsible of this dynamic degradation. In particular, the combination of dynamic measurements, doping-profile evaluation by means of SIMS analysis, and numerical simulations, have demonstrated the influence of the doping profile on the reduction of the dynamic performances, and the limited importance of the doping concentration value, providing better physical predictions of the dynamic behaviour consistent with the experimental results. Furthermore, this analysis have demonstrated the importance of the numerical simulation close to a deeper investigation of the traps location inside the buffer, in order to design high-performance GaN HEMTs with excellent semi-insulating buffer layers, minimizing the presence of dopant-induced

parasitic effects, like the current collapse.

In conclusion, trapping effects are parasitic effects that plague each GaN-HEMT technology, and that can enormously reduce the dynamic performances of particular devices, as previously reported. For this reason, it is really important a reliable evaluation of these effects, understanding the traps position, the transient behaviour, and the physical elements responsible of this phenomenon, in order to design devices with reduced trapping effects or completely avoiding it. Due to the different characteristics of each trapping effect, these evaluation are often not so simple, and require different techniques or custom setups in order to obtain consistent results and reliable demonstrations, as shown in this chapter. Furthermore, the dynamic behaviour of these effects increases the importance on the timing of the test procedure, especially during the analysis of slow traps, forcing a careful definition of the measurement sequence, and a fixed duration of each single step possibly affected by the traps transient evolution.

Moreover, the techniques here used for the evaluation of particular kink or current collapse effects can suggest many other techniques suitable for the evaluation of other parasitic effects, just adapting the aforementioned instrument setups, or even other instruments, to detect and locate the traps responsible of the parasitic effect under analysis.

Chapter 6

Conclusions

This thesis has widely analyzed the main issues concerning the reliability and the trapping effects that reduce the performances of AlGaN/GaN HEMT devices suitable for both high-frequency and high-power applications. During this PhD, the activity has been focused on many project and on many device technologies, exploring the capabilities of devices adapted for the RF operation on both terrestrial and space applications, and for high-power operation, with the main objective of understanding the degradation mechanisms that limit the device performances along the time or reduce the predicted life-time, preventing the real application of these technologies and a possible introduction in the market.

As observed in chapter 2 and chapter 3, the improved device processing and a quite stable technology have produced devices with excellent reliability performances, showing optimal characteristics in high-voltage off-state conditions, even for long times. Compared to other older GaN-HEMT technologies, where the gate-degradation mechanisms were always the first reliability concern even at low reverse voltages, in this case an optimization of the layer structure and a careful management of the electric-field, by means of improved gate depositions and particular field-plate structures, are demonstrating the maturity of these last technologies that seem to fit the performances and the stability requirements even, for example, for the space applications.

On this robust technologies, as a consequence, it is raising the interest on what other failure mechanisms plague these devices, for example in on-state conditions

or in high-temperature conditions, and which accelerating factors can be used for a accurate and reliable life-time prediction. In particular, in chapter 2, it has been shown that hot electrons have a strong influence on the long-term reliability of Task-Force devices, permanently reducing the device performances (electrical and optical) by means of a defect generation and electron trapping process, induced by hot electrons in the gate-drain access region. Moreover, the use of the EL intensity as a measure of the stress accelerating factor, have allowed to derive an acceleration law for GaN HEMT hot-electron degradation, finding a power-law dependence between the hot-electron presence and the time-to-failure.

In chapter 3, despite the really good robustness of ESA devices in both high-voltage and high-temperature operations, the technology have shown a significant reduction of the failure voltage moving from the zero-current off-state step-stress to the mid-current semi ON-state step-stress. This result, correlated with the positive dependence between the temperature and the breakdown voltage, have suggested an impact-ionization failure mechanism, strictly connected with the hot-electron presence in the channel or in the gate-drain region. Even on this case, the hot-electron presence seems to have an important influence on the device degradation or on the device failure, similar to other quite consolidated technologies for microwave devices, suggesting an improved maturity of GaN technology that starts to follows more “standard” failure mechanisms.

Despite these reliability improvements, many issues concerning degradation modes and trapping effects can reduce the device performances in a not predictable way, due to the absence of a complete understanding on the physics that leads these mechanisms, even from the literature. In particular, the gate-edge degradation still represents an important and not completely explained failure mechanism. In chapter 4, a deeper analysis of the time-dependence of this phenomenon has allowed to propose a new model for the gate-degradation evolution on GaN-HEMT devices, suggesting the reduced importance of the step-stress test evaluation and of the *critical voltage* definition, due to failures clearly visible even well below the *critical voltage*. From the explained model, the gate failure has consequently been ascribed to a defect-percolation process, enhanced by the defect density concentration and

by the applied stress voltage. The use of time-resolved and spectrally-resolved EL measurements have been used not only to further confirm the model and the leakage path creations, but also to identify the traps responsible of the recoverable parasitic effects happening during the reverse-bias process.

The same techniques, exploited on a different device technology, have provided significant information about the *kink effect* and its correlation with the buffer traps responsible of the yellow luminescence in GaN, as described in chapter 5.

At this stage, few interesting results have been gathered on the reliability assessments and on the parasitic effects evaluation, underlining the continuous improvement of the GaN-HEMT technology, which is becoming really feasible for both the RF application and for the high-power application. Nevertheless, further studies need to be done to fully demonstrate the reliability of these devices, and influence of the trapping effects on the ever-increasing performances. For this reason, some future work can be particularly interesting to perform in order to follow the same targets.

- From the results on the Task-Force reliability analysis, it can be better evaluated the effectiveness of the acceleration law for all the bias points characterized by a low drain current and an extremely high electric-field (close to the pinch-off condition at high V_{DS}), and the real effect of the dissipated power on the performance degradation, by extracting the junction temperature behaviour at the different bias points.

- From the results on the ESA high-voltage tests, it can be interesting to optically investigate the high voltage behaviour of these devices, and in general of all the highly-robust devices (especially for the high-power switching applications), to better understand the shift of the emission profile and, as a consequence, *(i)* the possible role of the drain ohmic contact on the permanent device failure, *(ii)* or the transient behaviour of the drain-side emission and its influence on the dynamic performances reduction.

- From the gate-degradation analysis, it can be clarified the role of the temperature on this failure mechanism, unambiguously identifying a criteria for

the life-time evaluation suitable for all GaN-based HEMTs, which take into account even the gate-degradation mechanism. In fact, the conventional techniques for the life-time evaluation, which use the temperature as unique accelerating factor of each degradation mechanism, does not consider the gate-degradation effect already visible at room temperature, providing a not reliable or over-optimistic estimation of the device life-time.

- From the iron-doping analysis, it can be concluded the SIMS analysis on the doping profiles of the different GaN buffers, in order to complete and confirm the experimental results and the theoretical assumptions about the dependence of the current-collapse intensity on the Fe-doping presence, and to quantitatively correlate the doping profiles with the different Slump Ratio values measured during the pulsed tests.

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