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High Efficiency Power Converters for Vehicular Applications

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ABSTRACT

The use of power electronics in the electrical propulsion systems leads to the optimal and efficient utilization of the traction motors and the energy sources (batteries and/or fuel cells) through the recourse to suitable power converters and their proper control. Power electronics is also used for implementing the multiple conversions of the energy delivered by the sources to feed the various loads, most of them requiring different waveforms of voltage (ac or dc) and/or different levels of voltage. This work focuses on the solutions aimed at improving the efficiency of power converters for vehicular applications, which is of great importance because of the limited amount of energy that can be stored in the electric vehicles. The study takes into consideration both the traction applications and the battery charging applications whether it is done by conductive means or by wireless power transfer (WPT) systems. The improvement in traction drive efficiency results in an increment of the drivetrain efficiency of the vehicle, leading to an extension in the driving range, while the employment of efficient power converters is required to charge batteries with increasingly large capacity. The losses of power devices are even more significant when they operate at high frequencies to compact the size of the filter elements and/or the transformers. The losses of power devices can be minimized by making the commutation soft or by replacing the conventional devices with the new generation devices based on wide bandgap (WBG) semiconductor materials. In this work, the properties of the WBG semiconductor materials are illustrated and the operation of the devices based on these materials are analyzed to grasp better their characteristics and performance. The losses of individual devices (i.e. diode, IGBT, MOSFET) as well as the operation of power converters for various applications are examined in detail.

To evaluate the performance of the SiC devices in electric vehicle applications, an AC traction drive for the propulsion of a typical compact C-class electric car has been considered. Two versions of the inverter have been investigated, one built up with conventional Si IGBTs and the other one with SiC MOSFETs, and the losses in the semiconductor devices of the two versions have been found along the standard New European Driving Cycle (NEDC). By comparing the results, it is emerged that the usage of the SiC MOSFETs reduces the losses in the traction inverter of about 5%, yielding an equal increase in the car range. To complete the study, calculation of the efficiency has been extended to the whole traction drive, including the traction motor and the gear.

Afterwards, a power factor correction (PFC) circuit, which is commonly used to mitigate the distortion in line current, has been studied. The study is started by considering the basic and the interleaved PFC configurations and by defining their circuit parameters. After selecting the interleaved configuration, the magnitude of voltages and currents in the PFC rectifier has been determined and the values obtained have been verified by a power circuit

simulation software. The digital signal processing (DSP) has been also studied as it is used for the control operation of the PFC. At last, a prototype of PFC rectifier with interleaved configuration is designed. The design process and the specification of the components are described in brief.

A prototype of synchronous rectifier (SR) is designed for the output stage of a WPT system. With respect to conventional rectifiers, in SRs the diodes are replaced by MOSFETs with their antiparallel diodes. MOSFETs are bidirectional devices that conduct with a low voltage drop. During the dead time, the diodes in antiparallel to the MOSFETs are conducting. At the end of dead-time, signals are applied at the MOSFET gates that make conducting all along the remaining period, thus reducing the conduction losses. The dead-time length is optimized by using fast switching devices based on SiC semiconductor materials. The prototype is designed and tested at the line frequency. The experimental results obtained from the prototype corroborate both the analytical results and the simulation results. As SR exhibits is working with high efficiency at the line frequency, it is expected that at the higher operating frequencies of the WPT systems, the performance of SR will be even better.

A DC-DC isolated power converters used to setup the battery charger through wire system are studied. Two topologies of DC-DC converters, i.e. Dual Active Bridge (DAB) and Single Active Bridge (SAB) converters, are considered. For both the topologies operation are described at steady state. For SAB converter, two possible modes of operation are examined: discontinuous current conduction (DCM) and continuous current conduction (CCM). Soft-switching operation of both SAB and DAB converters, obtained by the insertion of auxiliary capacitors, is analyzed. Moreover, the soft-switching operating zone for the two converters are found as a function of the their output voltages and currents. Finally, the comparative analysis of soft-switching operation of SAB versus DAB converter is presented.

The thesis work has been carried out at the Laboratory of "Electric Systems for Automation and Automotive" headed by Prof. Giuseppe Buja. The laboratory belongs to the Department of Industrial Engineering of the University of Padova, Italy.

SOMMARIO

L’utilizzo dell’elettronica di potenza nei sistemi di propulsione elettrica porta all'utilizzo ottimale ed efficiente dei motori di trazione e delle sorgenti di energia (batterie e/o celle a combustibile) attraverso il ricorso a convertitori statici e al loro controllo. L’elettronica di potenza è utilizzata anche per implementare più conversioni dell’energia fornita dalle sorgenti per alimentare i vari carichi, la maggior parte delle quali richiede forme d'onda di tensione diverse (AC o DC) e/o diversi livelli di tensione. Questo elaborato si concentra sulle soluzioni volte a migliorare l'efficienza dei convertitori di potenza per applicazioni veicolari, tema che è di grande interesse per la limitata quantità di energia accumulabile a bordo. Sono prese in considerazione sia le applicazioni di trazione che le applicazioni di ricarica degli accumulatori realizzate con mezzi conduttivi o con i sistemi di trasferimento di potenza senza fili (WPT). Il miglioramento dell’efficienza degli azionamenti di trazione produce un incremento dell'efficienza dell’intero powertrain del veicolo, che si traduce in un incremento dell’autonomia del veicolo, mentre l’impiego di convertitori di potenza efficienti si rende necessario per la ricarica di batterie con capacità sempre maggiori. Le perdite dei dispositivi di potenza sono ancora più significative quando operano ad alte frequenze di lavoro per compattare le dimensioni degli elementi filtranti e/o dei trasformatori. Le perdite nei dispositivi di potenza possono essere minimizzate rendendo la commutazione soft o sostituendo i dispositivi convenzionali con i dispositivi di nuova generazione basati su materiali semiconduttori con ampia banda proibita (WBG). Nell’elaborato, sono illustrate le proprietà dei materiali semiconduttori WBG e si analizza il funzionamento dei dispositivi basati su questi materiali per comprendere le loro caratteristiche e prestazioni. Le perdite di singoli dispositivi (come diodi, IGBT, MOSFET) nonché il funzionamento di convertitori di potenza per varie applicazioni sono esaminati in dettaglio.

Per valutare le prestazioni dei dispositivi SiC quando vengano impiegati nei veicoli elettrici, è preso in esame un azionamento di trazione in AC impiegato per la propulsione di una tipica automobile elettrica di classe C. Due versioni di invertitore sono esaminate, una costruita con convenzionali Si IGBT e l'altra con MOSFET SiC, ed è calcolata la potenza persa nei dispositivi a semiconduttore delle due versioni di invertitore mentre l’automobile percorre il ciclo normalizzato di guida europeo (NEDC). Dal confronto dei risultati è emerso che l'utilizzo dei MOSFET SiC riduce le perdite nel convertitore di trazione di circa 5%, ottenendo un uguale incremento dell’autonomia dell’automobile. Per completare lo studio, si è successivamente esteso il calcolo dell’efficienza all’intero azionamento di trazione, comprendente il motore e il riduttore.

Si è quindi studiato un raddrizzatore con circuito di correzione del fattore di potenza (PFC), utilizzato per ridurre la distorsione di corrente in linea. Lo studio è iniziato

considerando sia la configurazione di base che quella interleaved e individuando i parametri circuitali. Dopo aver scelto la configurazione interleaved, sono determinate le ampiezze delle tensioni e delle correnti presenti nel raddrizzatore PFC e i valori ottenuti sono verificati mediante un software di simulazione di circuiti di potenza. E' anche studiato un dispositivo per l'elaborazione digitale dei segnali (DSP) nel quale implementare il controllo del raddrizzatore PFC. Infine è progettato un prototipo di raddrizzatore PFC con configurazione interleaved. Il processo di progettazione e le specifiche dei componenti sono brevemente descritti.

Un prototipo di rettificatore sincrono (SR) è stato sviluppato per lo stadio di uscita di un sistema WPT. In confronto con i raddrizzatori convenzionali, in un SR i diodi sono sostituiti da MOSFET con diodi in antiparallelo. I MOSFET sono dispositivi bidirezionali caratterizzati da una bassa caduta di tensione e dalla direzionalità nel condurre la corrente. Durante il tempo morto, entrano in conduzione i diodi in antiparallelo ai MOSFET. Al termine del tempo morto, ai MOSFET sono applicati segnali di comando che li portano in conduzione per tutta la restante parte del semiperiodo, riducendo così le perdite di conduzione. La durata del tempo morto è ottimizzata utilizzando dispositivi di commutazione veloci basati su materiali semiconduttori SiC. Il prototipo è stato progettato e sperimentato alla frequenza di rete. I risultati sperimentali ottenuti hanno confermato sia i risultati analitici che le simulazioni. L'elevato valore di efficienza ottenuto sul prototipo operante alla frequenza di rete fanno prevedere che il suo impiego alle alte frequenze operative dei sistemi WPT possa dare risultati ancora migliori.

Si sono studiati i convertitori isolati di potenza DC-DC impiegati nei caricabatteria di tipo conduttivo per veicoli elettrici. Si sono prese in considerazione due topologie di convertitori DC-DC, il convertitore con doppio ponte attivo (DAB) e quello con un unico ponte attivo (SAB). Per entrambe le topologie è analizzato il funzionamento in condizioni di regime. Per il convertitore SAB sono esaminate due possibili modalità di funzionamento: conduzione discontinua di corrente (DCM) e conduzione di corrente continua (CCM). Si è analizzato il funzionamento in soft-switching, ottenuto con l'inserzione di condensatori ausiliari, sia del convertitore SAB che di quello DAB. E' individuata la zona di funzionamento in soft-switching per i due convertitori in funzione delle tensioni e delle correnti di uscita. Infine, è stata eseguita un'analisi comparativa del funzionamento in soft-switching dei due convertitori.

Il lavoro di tesi è stato realizzato presso il Laboratorio di "Sistemi Elettrici per l'Automazione e Automotive" diretto dal Prof. Giuseppe Buja. Il laboratorio fa parte del Dipartimento di Ingegneria Industriale dell'Università degli Studi di Padova, Italia.

Dedicated to

My Parents

and

Respected Teachers

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LIST OF ACRONYMS

DC	Direct Current
AC	Alternating Current
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
JFET	Junction Field Effect Transistor
BJT	Bipolar Junction Transistor
LCJFET	Low Channel Junction Field Effect Transistor
BGJFET	Buried Grid Field Effect Transistor
EMVTJFET	Enhancement Mode Vertical Trench JFET
DGVTJFET	Double Gate Vertical Channel Trench JFET
DMVTJFET	Depletion Mode Vertical Trench JFET
EMVTJFET	Enhancement Mode Vertical Trench JFET
MOSHFET	Metal Oxide Semiconductor Hetero-Structure FET
Si	Silicon
WBG	Wide Band Gap
SiC	Silicon Carbide
GaN	Gallium Nitride
PFC	Power Factor Correction
SR	Synchronous Rectifier
WPT	Wireless Power Transfer
PMSM	Permanent Magnet Synchronous Motor
NEDC	New European Driving Cycle
DSP	Digital Signal Processing
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching
SVM	Space Vector Modulation
DCM	Discontinuous Conduction Mode
CRM	Critical Conduction Mode
CCM	Continuous Conduction Mode
SAB	Single Active Bridge
DAB	Dual Active Bridge

Chapter 1

Introduction

1.1 Overview

Power converter is the heart of power electronics that process and control the flow of electrical energy by supplying voltages and currents in a form that optimally suited for the user loads. Power electronics involves the optimal and efficient utilization of the traction motors and the energy sources (batteries and/or fuel cells) through the recourse to suitable power converters and to their proper control. Power electronics is also used for implementing multiple conversions of the energy delivered by the sources to feed the various loads, most of them requiring different waveforms of voltage (ac or dc) and/or different levels of voltage. Due to the number of reasons like the limited energy amount stored onboard the battery-powered electric vehicles, the convenience of keeping low the losses in the power converters, especially in the semiconductor devices, for their operation to be reliable and the demands of high overall performance for the electric powertrain, the power converters onboard the electric vehicles must be as much efficient as possible and, at the same time, must carry out the energy conversion in an accurate way both at steady-state and during transients. Therefore, the development of power converters together with their design and experimentation is a major task that needs a dedicated exploration in the field of power circuitry, semiconductor devices and converter control.

High-efficiency in power converters are mainly obtained by reducing the switching losses. This can be achieved by implementing the soft-switching techniques, that consist in forcing to a low value (ideally, to zero) either the voltage across or the current through the device during its turning off (i.e. its commutation from the on state to the off state) and turning on (i.e. its commutation from the off state to the on state). The two approaches are commonly denoted with zero voltage switching (ZVS) and zero current switching (ZCS) techniques. By making soft the switching, the relevant losses of the semiconductor devices are greatly reduced and the energy conversion becomes efficient. This result could also be exploited to increase the switching frequency of the power converters to the benefit of the performance of the supplied load.

Efficiency of the power converters can be evaluated in the design stage by computing the losses in the semiconductor devices of a power converter, starting from an analysis of the operation of the power converters and the embedded devices, and using the specs of the devices available from their data sheet. Efficiency can be measured in the experimental stage by either calorimetric or electric methods. By the first-type methods, the losses are detected in the power converters through the measure of the heat that they produce. By the second-

type methods, the electric powers are measured at the input and the output of the power converter by means of the modern power analyzers that are effective in doing the measure for switched power converters too.

Moreover, an appropriate investigation is required for a given application in order to find which of them have the best performance in reducing losses in order to design an efficient high-frequency power converter. The switching behavior of the devices for the wide range of frequency and power is analyzed. The evaluation of the switching losses and conduction losses has been carried out analytically and by means of numerical programs. The study was mainly devoted to the working principle and characteristics of the last generation switching devices to utilize the advantage of their performances in designing the power converters. In present scenario, the power devices based on the wide bandgap (WBG) semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN), resulted the most prominent candidates because of their low switching losses as well as low conduction losses. The close examination of properties and applications of the SiC and GaN based MOSFETs and diodes, are investigated in details together with the design procedure of various high efficiency converters.

1.2 Power Converters Requirement

The most important types of power converters required for vehicular applications are the traction inverter for the propulsion system and to charge the battery by the means of wireless charging system or wired charging system.

1.2.1 Traction Inverter

Three-phase traction inverter is required for the propulsion system of EVs. Three-phase Permanent Magnet Synchronous Motor (PMSM) has been selected for the case of study. The schematic diagram of propulsion system is shown in Fig. 1.1. Three-phase voltage source inverter (VSI) consists three legs, each leg having two transistors with their antiparallel diodes are connected in parallel.

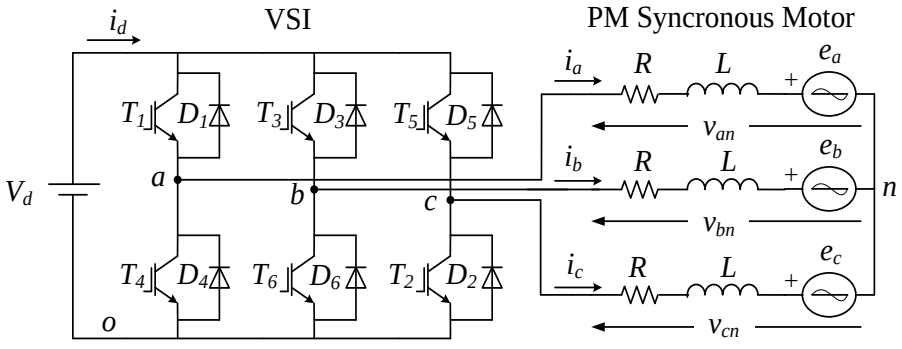


Fig. 1.1 Diagram of traction drive

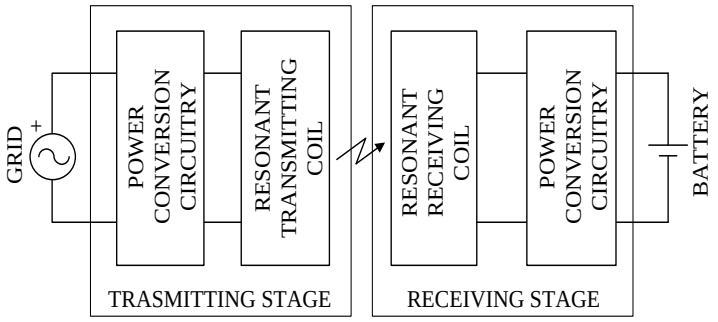


Fig. 1.2 General scheme of battery wireless charging system

1.2.2 Power converters for wireless charging

Wireless power transfer systems (WPTSs) supply a load with the electric energy absorbed by the grid without requiring any wired connection between load and grid. WPT is one of the application, where the resonant power converter can be used to supply the power in primary coil. The operating frequency of WPTSs is very high i.e. 85 kHz that helps to reduce the size of the coil.

Schematics of a battery wireless charging (BWC) system is drawn in Fig. 1.2. It is made of two stages, transmitter and receiver, with the transmitter that is fed by the grid and the receiver that charges the PEV battery. In addition to the resonant coil, each stage includes a power conversion circuitry connected to the respective resonant coil. The power conversion circuitry of the transmitting stage consists of a rectifier and a high-frequency inverter. Due to the filtering action of the resonant transmitter coil, the power conversion circuitry behaves as a power source with sinusoidal voltage for the BWC system. The power conversion circuitry of the receiving stage consists of another rectifier that can charge the battery either directly or through a chopper, whose input voltage is kept constant.

1.2.3 Power converters for wired charging

The power electronics circuitry for wired battery chargers consists of an AC-DC converter followed by a DC-DC converter. The AC-DC converter rectifies the AC voltage from the power grid to a DC voltage. The DC-DC controls the voltage/current supplied to the battery according to its charging profile. In most of commercially available battery charger (BC), the two stages are separated by an insulation stage formed by a high-frequency

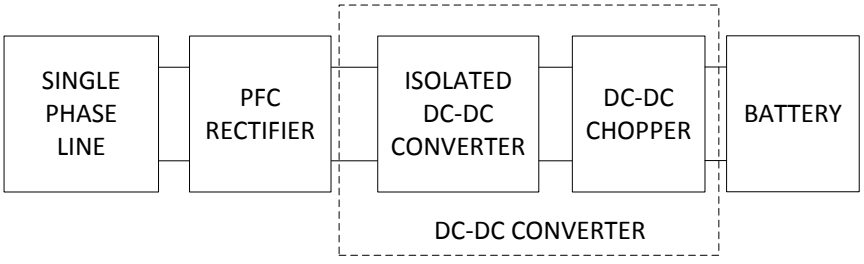


Fig. 1.3 Wired charging system

inverter, a coupling transformer and a high-frequency rectifier.

The simplest AC-DC power converter uses diodes as rectifying components. However, the currents drawn from the grid are highly distorted and additional input filters are required to comply with the rules about harmonic injection in the grid. For high power battery charger the use of input filters is not viable and hence more sophisticated AC-DC converter must be used. The general scheme of wired charging system is shown in Fig. 1.3. The PFC rectifier is incorporated for the AC-DC conversion and isolated DC-DC converter followed by chopper can be used to obtain the voltage and current profile required to charge the battery.

1.3 Motivation and Objective

The main objective of this research is to develop high efficiency power converters for the vehicular applications. The power converters required for the propulsion of electric vehicles are the DC-AC type while in the battery charging process power converters required of DC-DC, DC-AC and AC-DC types. To improve the efficiency of power converter seeking the implementation of advance technique in commutation to reduce the switching losses and/or utilization of new generation semiconductor devices (i.e. WBG devices) to reduce the overall power losses. The research focused on investigating the losses and size of the components in design procedure of power converters in which switching frequency plays an important role. The main challenge is to have the proper procedure realized in computer software which makes it possible to be implemented in system architecture evaluation and comparison.

The primary objective of this work is to study and demonstrate the maximum achievable conversion efficiency in power converters for EVs applications. In view of the requirements for battery charging and traction inverter applications, the work focuses on solutions that provide power transfer from one form to another form with a proper control maintaining very high efficiency. Special consideration has to be given to achieving high conversion efficiency in the case of high operating frequency i.e. 85 kHz for the WPT system. A second objective is to analyze and implement the soft switching technique for the commutation in order to minimize the switching losses of the power converters.

1.4 Problem Formulation

Efficiency of power converter depends on the losses consumed by the power devices and passive components. The main losses in power devices are conduction losses and switching losses. The conduction losses contribute significantly to the overall power losses of a diode rectification circuit, especially in low output-voltage applications. In the diode, the conduction losses depend on the forward voltage drop, the diode resistance and the magnitude of current that passes through the devices while in a MOSFET the conduction losses depend on the on resistance ($R_{DS,on}$) of the MOSFET and the current that passes through the devices. The switching losses mostly influence by the operating frequency. For the case of study for the WPT system, works at very high frequency to compact the size of

the system that requires special attention to maintain the optimum efficiency. Moreover, driving losses are also a part of the losses in a MOSFET but they are negligible compared to the total power losses up to frequencies of hundreds of kHz.

The other problem in the high frequency operation is to design the control circuit that is quite difficult to operate through the micro controller or digital signal processor circuit. Because of the fast switching operation of WBG based devices, required advanced driving circuit as compare to driving circuit of the conventional devices.

1.5 Research Contributions

The research contributions of this thesis work are summarized as follows:

- WBG devices are investigated in details for the designing of power converters for the battery charger as well as the traction inverter of Electric Vehicles.
- Loss analysis of semiconductor devices is illustrated to calculate the efficiency of power converters.
- Efficiency of the traction inverter is analyzed and comparative analysis has been performed for two versions of inverter: built up with Si IGBTs, to that of a traction inverter having the same ratings but built up with SiC MOSFETs. In addition, the Si-IGBTs inverter efficiency as well as drive train efficiency has been verified through the data collected from compact C-class electric car.
- A Power Factor Correction Circuit has been designed that can be implemented to feed the power supply to the high frequency inverter for WPT system as well as to feed the power supply in wired battery charging which is based on Single Active Bridge (SAB) converter.
- A Synchronous Rectifier has been designed and tested successfully at line frequency that will be used in secondary side of wireless power transfer (WPT) system, to convert the secondary coil AC voltage in to DC voltage maintaining high efficiency.
- Isolated DC-DC Power Converters have been analyzed and the soft-switching capabilities have been investigated for two versions of converter i.e. Dual Active Bridge (DAB) and Single Active Bridge (SAB) converters.

1.6 Thesis Outlines

Chapter 2 illustrates the WBG semiconductor materials (i.e. SiC and GaN) and their importance. The structure of materials and their electrical properties (i.e. energy bandgap, electrical field, drift velocity, thermal conductivity, and electric breakdown) are discussed in this chapter. The SiC material has different polytypes (i.e. 2H-SiC, 4H-SiC and 6H-SiC) and GaN has two types of crystal structures (i.e. zincblende and wurtzite) are explained with their performance characteristics. Finally, energy band diagram and comparative analysis of silicon (Si), SiC, and GaN materials are presented; the comparative results have

accomplished that why SiC and GaN materials are dominating the semiconductor markets over Si materials.

Chapter 3 demonstrates the SiC based devices that include SiC diodes, SiC transistors and driving circuit of different transistors. The construction, working principle together with static (i.e. conduction losses) and dynamic characteristics (i.e. switching losses) of diodes are discussed. In addition, the SiC transistors (i.e. SiC JFET, SiC BJT, and SiC MOSFET) with their construction details and working principle have explained in details. The various characteristics of the SiC transistors and a comparative analysis with Si devices have been explained, the results confirm the eminence of SiC devices over Si. Moreover, the driving circuit of the normally on SiC JFET, normally off SiC JFET, and SiC MOSFET are discussed which show that the performance of SiC devices even more better with modern driving circuit.

Chapter 4 presents the GaN based semiconductor devices and their driving circuits. The complete structure with the different substrates and various characteristics of GaN MOSFET are presented. GaN device possesses high breakdown voltage and low conduction resistance characteristics that enable high-speed switching and miniaturization, are briefly discussed in this chapter. Moreover, the different driving circuits are explained for GaN devices that imply the requirement of novel driving circuits for the better performance of GaN devices compared to conventional Si devices.

Chapter 5 describes the loss analysis of different power devices as well as different power converters. A general lay out structure of power loss for power devices is discussed in details. The loss models for each devices i.e. diode, IGBT, and MOSFET are formulated and the variation in switching losses as well as in conduction losses with the change of voltage and current are presented. As conduction losses and switching losses are the major losses of the devices, these two losses are examined closely to have the exact idea of power losses in the converters. Finally, the comparison of losses among the Si, SiC and GaN devices are presented.

Chapter 6 deals a three-phase DC-AC traction inverter and the importance of SiC devices. To evaluate the performance of the SiC devices in electric vehicle applications, a traction inverter drive for the propulsion of a typical compact C-class electric car has been considered. Two versions of the inverter have been investigated; one built up with conventional Si IGBTs and the other one buit with the same rating of SiC MOSFETs, and the losses for the two inverter versions have been found along the standard New European Driving Cycle (NEDC). To determine the losses along the driving cycle, current and voltage requirements posed by the traction motor have been first obtained. Then a proper loss modeling of the Si and SiC devices has been set up and a three-dimension matrix has been assessed by help of a Matlab code, which gives the losses for the two inverter versions as a function of the current and the duty-cycle in each SVM period. Moreover, the loss matrix has been used to calculate the cumulative inverter losses along the driving cycle. Comparison

of the results has shown that the usage of the SiC MOSFETs in the traction inverter leads to the great reduction in losses yielding an equal increase in the car range.

Furthermore, the work is extended for the calculation of combined drive train efficiency for the steady state condition. The efficiency of combined drive train system is calculated by the multiplication of inverter efficiency with the motor efficiency for both type of devices. The efficiency of PMSM is taken from literature. As discussed above, loss models of both types of inverters have developed on the same theoretical basis; model of IGBT inverter has been validated using experimental data taken by a commercial electric car of C-class thus indirectly validating the SiC MOSFETs model as well. Finally, the comparative analysis has been performed between two types of inverters as well as between their combined traction drives over the entire range of torque and speed. Comparison results show that the use of SiC MOSFETs improves the efficiency of the inverter as well as of the combined traction drive.

Chapter 7 explains the power factor correction (PFC) circuit which consists a rectifier circuit and interleaved boost converter. The main objective to design a PFC circuit is to eliminate the distortion in the voltage supply. The distortion in grid voltage occurs due to the undesired harmonics currents at frequency higher than the fundamental frequency and the non-linear loads that are connected to the grid. This influences the loads as transformers and motors that are connected to the lines, which are operated under a distorted supply voltage, by increasing their losses. Moreover, this chapter emphasizes the operation of boost converter through interleaved mechanism that give the better performance as compared to normal boost converter. A prototype for PFC circuit is designed and the design procedure is explained in brief. The SiC MOSFETs and diodes are used for the interleaved boost converter that have low losses lead to maintain the overall efficiency of the system.

Chapter 8 highlights the details circuit structure and working principle of Synchronous Rectifier (SR). It is modeled by replacing all four diodes through the four MOSFETs of a diode rectifier to improve the efficiency of the rectifier. The investigation is extended to the superior characteristics of MOSFETs over diode, that the forward voltage drop of a standard pn-junction diode causes significant conduction losses as compared to MOSFET for the similar type of material (i.e. Si or SiC). Moreover, the generation of gate drive signals for the MOSFETs and the working principle of SR are explained in this chapter. A prototype of SR is designed with their control circuits. The results obtained through the prototype strongly validate the simulation results. This chapter also describes the basic methodology of design and utilization of SR for the WPT system.

Chapter 9 describes the Isolated DC-DC converter for the Single Active Bridge (SAB) as well as for the Dual Active Bridge (DAB). The analysis is started with the characteristics of SAB and DAB for the different operating conditions. For SAB converter, the characteristics are analyzed for the discontinuous conduction mode (DCM) as well as for the continuous conduction mode (CCM). The basic difference between SAB and DAB converters is

presented with their proper circuit arrangement. The design parameters are investigated in details for SAB and DAB converters. For the design purposes, all the parameters are calculated as a function of the load current and output voltage along the operating range. Furthermore, the soft switching capabilities are investigated for SAB as well as DAB converters. To make the commutation soft, auxiliary capacitor is required to connect acroos the switches of converter. The different possibilities of auxiliary capacitor connection have been investigated to achieve maximum soft switching operation zone. The results show that SAB converter can work in incomplete soft switching or in full soft switching zone while DAB converters can work in partial soft switching or full soft switching zone. Finally, the design procedure of auxiliary capacitor and application of SAB converter is presented.

Chapter 10 concludes the thesis and discusses the scope of future work in the field of power converters for vehicular applications.

Chapter 2

Semiconductor Materials

2.1 Silicon Carbide

2.1.1 Introduction

Silicon Carbide (SiC) has several superior characteristics over silicon (Si). In particular, due to wide bandgap characteristics of SiC semiconductor devices are expected to have high temperature, high speed and high voltage operation capabilities [1]. These advantages cannot all be obtained with conventional Si-based semiconductor devices. The main focus of this analysis were the high temperature operation capability of SiC devices and their switching characteristics in power converters. The high breakdown electric field of SiC allows for the voltage blocking layers to be designed in such a way that on-state resistance is reduced with respect to Si. When a Si device is compared with the same current rating of SiC device, the active area of the latter one results much smaller, thus decreasing the device capacitance and promoting the higher switching frequencies. The wide band gap properties allow for higher junction temperatures, high thermal conductivity and low coefficient of thermal expansion (CTE), which makes the packaging of SiC power devices more reliable across a wide range of temperature. The binding energy between Si atom and C atom is 6.34 eV while the binding energy between two atoms of silicon is 4.63 eV. Therefore, the link between Si and C is much stronger which makes SiC a resistant material from various points of view and useful for various applications including electronics. Moreover, SiC is chemically resistant as well as temperature resistant. Therefore, overall benefits of using SiC as the basic materials for the manufacture of components for power devices can be listed as follows:

- Rise of voltage
- Rise in temperature
- Reducing the size
- Minimizing losses
- Increasing frequency
- Rising power

The rise of voltage, rise in temperature and reduction in size are the most important key factors at component level, that decide the area of use and the range of application of the SiC devices. SiC allows for the consideration of a greater density of system integration with smaller components whether active or passive and the advantage of less complex systems.

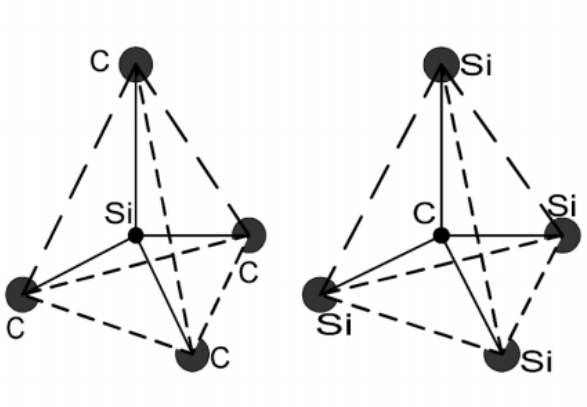


Fig. 2.1 Tetrahedral lattice structure of silicon carbide

2.1.2 Lattice structure of silicon carbide

SiC molecules are made by arrangement of covalently bonded tetrahedral Si and C atoms with either a carbon atom bonded to four Si atoms or a Si atom bonded to four carbon atoms as shown in Fig. 2.1. SiC has many polytypes, which are made up of equal parts of silicon and carbon. Both silicon and carbon are period IV elements, so they prefer a covalent bonding. Each carbon atom is surrounded by four silicon atoms, and vice versa. Fig. 2.1 shows the schematic diagram of lattice structure of SiC.

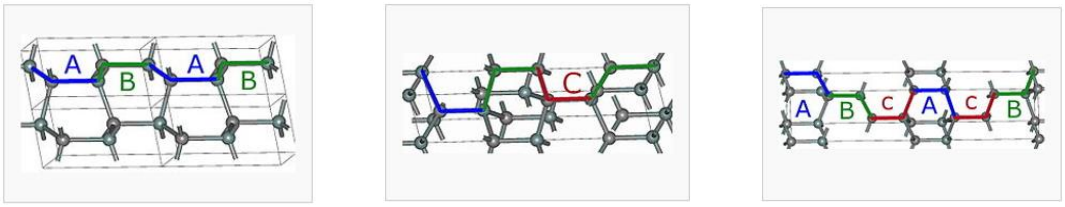
2.1.3 Properties of silicon carbide

The most important properties of SiC compared with other semiconductor materials are listed in Table 2.1.

The 6H-SiC and 4H-SiC are the two SiC polytypes. Both the polytypes have hexagonal wurtzite structure. Where number indicates the layer and letter indicates the Bravais

Table 2.1: Properties of various semiconductors [2], [3]

Property	**Si**	**6H-SiC**	**4H-SiC**	**GaN**
Bandgap Eg(eV)	1.1	3.03	3.26	3.45
Dielectric Constant, Ɛr	11.9	9.66	10.1	9
Breakdown Field, Ec(kV/cm)	300	2500	2200	2000
Electric mobility, μn (cm^2/V-s)	1500	500	1000	1250
Hole mobility, μn (cm2/V-s)	600	101	115	850
Thermal Conductivity, λ (W/cm-K)	1.5	4.9	4.9	1.3
Thermal Expansion ($x10^{-6}$)/^{0}K	2.6	3.8	4.2	5.6
Saturated E-Drift velocity, Vsat (x107cm/s)	1	2	2	2.2



(a) 2H-SiC (b) 4H-SiC (c) 6H-SiC

Fig. 2.2 Structure of major SiC polytypes

structure. The difference between these two polytypes, which are nothing but only the multiple layers of 2H-SiC, is explained as follows. The 2H-SiC structure is equivalent to that of wurtzite and is composed of only elements A and B stacked as ABABAB. The 4H-SiC unit cell is twice longer, and the second half is twisted compared to 2H-SiC, forming the ABCB stacking. The 6H-SiC cell is triple that of 2H, and the stacking sequence is ABCACB. The structure of major polytypes are shown in Fig. 2.2.

2.1.3.1 Wide bandgap

Silicon carbide is classified as a wide band gap material ($E_g = E_c - E_v$), where E_c is conduction band energy, E_v is valence band energy, and E_g is band gap as shown in Fig. 2.3. The high saturation velocity and thinner drift region associated with the high band gap make the device operating at higher frequency. Due to high band gap, silicon carbide has reduced drift region width, and hence a short conduction zone. Therefore, the on-resistance of silicon carbide devices is lower and results in lower conduction loss compared to other devices. Figure 2.4 shows the specific on-resistance vs. the designed breakdown voltage of Si, 4H-SiC and 6H-SiC. The breakdown voltage is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the source and drain

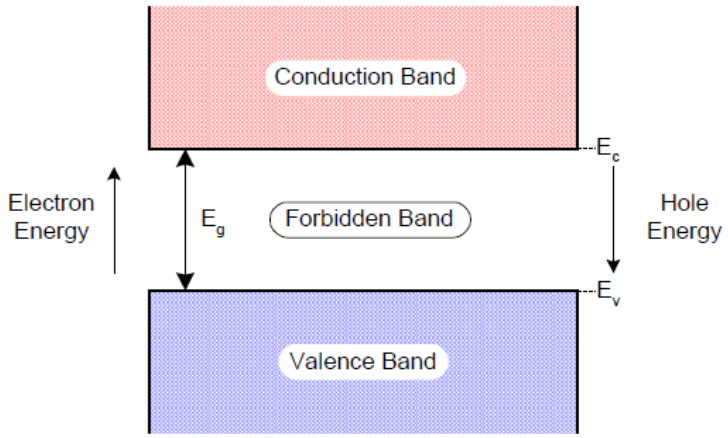


Fig. 2.3 Simplified diagram of the energy bands of a semiconductor

by an avalanche multiplication process, while the gate and source are shorted. For most power devices, the current is conducted through the substrate. Wider energy band gap also supports in reducing leakage currents and provides higher operating temperatures.

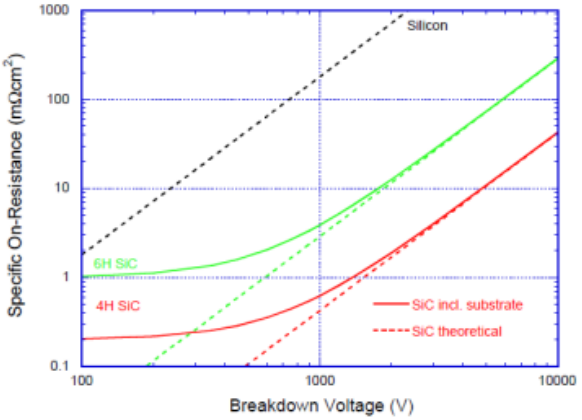


Fig. 2.4 Specific on-resistance vs. the designed breakdown voltage of silicon carbide

2.1.3.2 Critical electric field

The idea with a semiconductor device is that they can either block a voltage, or conduct a current with low power loss. The schematic diagram along the depletion region width W, of the electric field distribution inside the device is shown in Fig. 2.5. Most of the depletion region spreads into the lowest doped part of the junction. The basic equations for the calculation of breakdown voltage and on-resistance are given as follows.

$$V_B = \frac{WE_B}{2} \tag{2.1}$$

$$W \approx \sqrt{\frac{2\varepsilon V_B}{qN_D}} \tag{2.2}$$

$$N_D = \frac{2\varepsilon V_B}{qW^2} = \frac{\varepsilon E_B^2}{2qV_B} \tag{2.3}$$

$$R_{on} = \frac{W}{q\mu_N N_D} = \frac{4V_B^2}{\varepsilon\mu_N E_B^3} \tag{2.4}$$

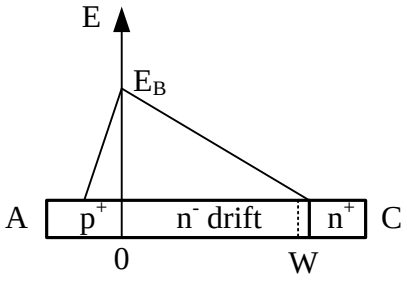


Fig. 2.5 Electric field distribution in semiconductor materials

$$\frac{V_B^2}{R_{on}} = \frac{\varepsilon \mu_N E_B^3}{4} \tag{2.5}$$

where q is the charge of an electron, N_D is the doping density, V_B is the breakdown voltage, ε is the dielectric constant, E_B is the electric breakdown field, μ_N is the electron mobility and R_{on} is the on resistance. From equation (2.1), the voltage supported by this depletion region can be calculated, which is the area under the graph. The lower critical electric field makes lower the on resistance and the switching losses as calculated from equation (2.2) to (2.4). When the device is not blocked, it will conduct large currents with small voltage drop (power loss). Equation (2.5) shows that the higher electric field leads to higher doping which produce a lower on-resistance in the devices. The minority carrier charge has to be removed before the device can block a voltage and this will result in a switching loss. The total losses is the sum of on-state losses and switching losses. Higher critical electric field means that blocking layers of the devices can be thinner and with higher doping concentrations; this contributes to lower the on-resistance values compared to the equivalent silicon devices [3]. Fig. 2.6 shows the comparison of intrinsic concentration versus temperature for various semiconductor materials.

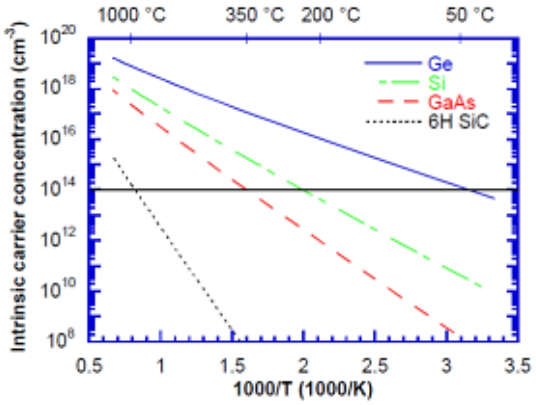


Fig. 2.6 Intrinsic concentration vs. temperature for various semiconductor materials

2.1.3.3 High saturated drift electric field

The electron and hole mobility shows how quick an electron/hole can move through a semiconductor. In a solid, electrons/holes move around randomly without any applied electric field. At low fields, the drift velocity is proportional to the electric field, so mobility μ is constant. Therefore, due to the higher electric field, the drift regions of SiC are thinner, and hence lead to higher operating frequencies. Moreover, the reverse recovery current passing through the wide bandgap semiconductor will be smaller, and hence the recovery time will be shorter.

2.1.3.4 High thermal conductivity

Thermal conductivity is the property that allow a material to conduct heat. Higher thermal conductivity (e.g., SiC and diamond) improves heat spreading or transfer and allows operation at higher power densities [4]. With respect to the higher thermal conductivity and low coefficient of thermal expansion ($4.0 \times 10{-}6/K$), SiC has better heat dissipation than Si, and thus requires less heat sink. Due to the low intrinsic carrier concentration and wider band gap, SiC has an intrinsic temperature of 900 ^{o}C while Si has 200 ^{o}C. High thermal conductivity enables SiC devices to operate at high power levels and still dissipate the large amount of excess heat. Therefore, the cost of cooling accessories like heat sink will be much less than silicon devices.

2.1.3.5 High electric breakdown field

SiC has a higher breakdown field than silicon because of the wide bandgap. The electron-hole pair generation due to ionization impact is difficult because of the wide band gap, and hence SiC can withstand higher electric fields compared to silicon. The high electric breakdown field allows the device to have less thick layers compared to silicon and therefore less drift region resistance reducing the on-state losses.

2.1.4 Summary of the advantages of SiC

In summary, SiC has the following advantages over Si:

- Wide band gap → Reduce carrier concentration → High temperature
- Wide band gap → High electric field → Reduce drift region widths → Low on-resistance → Block higher voltage
- High velocity saturation → Faster switch, high frequency
- High thermal conductivity → High power and better heat dissipation
- Smaller size and weight

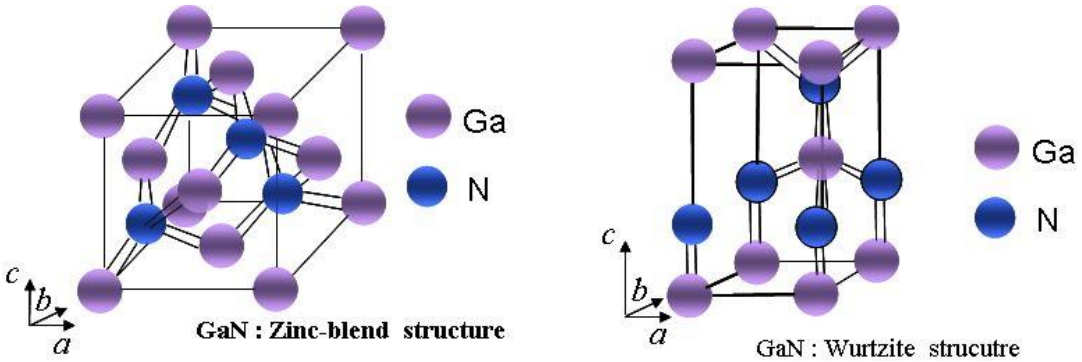
The most important advantage of SiC is the high electric field, which is good for all devices. Wide band gap materials exhibit greater electron mobility with larger applied fields compared to Si. Intrinsic parameters translate to enhanced operation at high switching frequencies with high breakdown voltage. Silicon has an almost three times smaller band gap than the SiC material. However, there is about a ten times wider critical electric field for breakdown that makes the huge difference.

2.2 Gallium Nitride

2.2.1 Introduction

Gallium Nitride (GaN) is a wide bandgap semiconductor material similarly like SiC, currently used in optoelectronics (i. e. the study and application of electronic devices that source, detect and control light, usually considered a sub-field of photonics) applications because of their variable-color light emission and high-density integration properties. GaN

devices are expected to offer inherently superior efficiency and greater design freedom simultaneously to achieve higher performance compared to other competing devices. GaN is the only hetero structure amongst the three WBG semiconductors i.e. GaN, SiC and Diamond. Recent developments in GaN devices have made it possible to realize switch-mode amplifiers design with high power and high efficiency at high frequencies. GaN has truly remarkable characteristics but there are many challenges to be overcome in developing GaN semiconductor technology. For GaN, optoelectronics applications are the dominant market drives, but the market suffers of the high costs and reliability. One of the major difficulties with GaN which is still matter of research is that the lack of a suitable substrate material lattice-matched and thermally compatible with GaN.



(a) (b)

Fig. 2.7 Schematic diagram of crystal structures of GaN

The equilibrium crystal structure for GaN is shown in Fig. 2.7. There are two types of crystal structures i.e. zincblende structure and wurtzite structure when grown on a cubic substrate. Zincblende is characterized as a cubic closet packing (ccp), also known as face-centered cubic structure. Wurtzite has a hexagonal closest packing structure (hcp), which is characterized by 12 ions in the corners of each unit that create a hexagonal prism. The ccp structures are more dense than hcp structures. Since density tends to decrease as temperature increases zincblende slowly transforms to wurtzite due to thermodynamic stability.

2.2.2 Electrical properties of GaN

GaN has very high breakdown voltages, high electron mobility and very high saturation velocity as compared to Si. The details of properties are listed in Table 2.1 in previous section. These tremendous advantages made it an ideal candidate for high-power and high-temperature applications. The large band gap means that the performance of GaN transistors is maintained up to higher temperatures than silicon transistors. The first gallium nitride metal semiconductor field-effect transistors (GaN MESFET) were experimentally demonstrated in 1993 and they are being actively developed. In 2010 the first enhancement mode gallium nitride transistors became commercially available. These devices were

designed to replace power MOSFETs in applications where switching speed or power conversion efficiency is critical. These transistors, also called eGaN FETs, are built by growing a thin layer of GaN on top of a standard silicon wafer. This allows the eGaN FETs to maintain costs similar to silicon power MOSFETs, but with the superior electrical performance GaN. As GaN electronic devices have shown various applications for high-power and high-frequency applications, growing concerns about the reliability of GaN-based power electronic devices have been raised in the past few years. For example, when these devices are under operation, the self-heating problem severely limits their performance and lifetime. It is of great importance to prudently assess the device heating problem if a reliable power electronic device is to be developed. Fig. 2.8 shows the on-resistance versus blocking voltage capability for silicon, silicon carbide and gallium nitride. The on resistance of the power devices play important role for measuring the conduction losses.

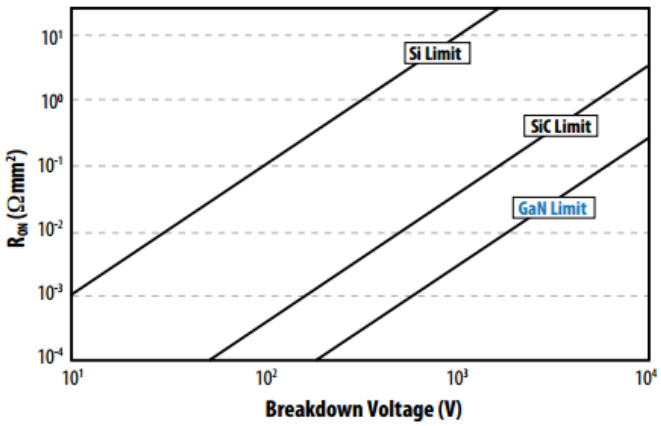


Fig. 2.8 On-resistance vs blocking voltage capability for silicon, silicon-carbide, and gallium nitride

From Table 2.1 it can be observed that GaN is the most dominating material for the power devices, which can provide the wider range of voltages and operating temperature. The GaN is more advantageous over silicon and silicon carbide to reduce the power loss as compared.

2.2.3 Summary of the advantages of GaN

Most of the properties are similar as discussed in SiC Section, because GaN is also a wideband gap material as like SiC with few superior advantages. Therefore, the following advantages of GaN over Si are summarized as follows:

- Wide band gap → Reduce carrier concentration → High temperature
- Wide band gap → High critical field → Reduce drift region widths → Low on-resistance
- Wide band gap → High electric field → Block higher voltage
- High velocity saturation → Faster switch, high frequency
- High thermal conductivity → High power and better heat dissipation

- Smaller size and weight

The most important advantage of GaN is the high electrical field, which is good for all devices. Wide band gap materials exhibit greater electron mobility with larger applied fields compared to Si. Intrinsic parameters translate to enhanced operation at high switching frequencies with high breakdown voltage. In some respects, GaN is a better material than SiC. GaN has an almost three and half times larger band gap than the Si materials.

2.3 Comparative Properties of Wide Bandgap Semiconductors

The different parameters of several semiconductor materials are shown in Table 2.1, that clearly shows how wide bandgap semiconductor materials are more advantageous over Si. Among all the semiconductors, GaN has the widest bandwidth and it also has the highest electric breakdown field. Between SiC and GaN devices, there is tradeoff GaN is better for high mobility operation while SiC provides high thermal performance. Moreover, as compared to SiC devices, GaN devices are most suitable for low power operation and provides higher cost solution for applications demanding higher performance with reduced sensitivity to the cost. GaN has truly remarkable characteristics but there are many challenges need to be overcome in developing GaN semiconductor technology. Due to the wider bandgap, SiC and GaN semiconductor devices require higher activation energy so that they can operate at very high temperature. From Table 2.1, it is clear that SiC and GaN devices have very high Electric Breakdown Field as compared to Si. Therefore, these devices can generate the carriers through impact mechanism. The on resistance of SiC polytypes and GaN is significantly lesser than of Si devices that results in lower conduction losses. Therefore, overall efficiency of converters based on SiC and GaN devices is very high as compared to Si devices. These wider bandgap devices can be operated at very high frequency due to very high saturation drift velocity, which is directly proportional to the switching frequency. The WBG devices have higher thermal conductivity that allow to transfer the heat efficiently and yields lower junction temperature.

2.4 Summary

WBG semiconductor materials (i.e. SiC and GaN) and their impact on power devices are summarized in this chapter. The structure of materials and their characteristics are discussed in details. The different polytypes of SiC (i.e. 2H-SiC, 4H-SiC, and 6H-SiC) and the crystal structure of GaN (i.e. zincblende and wurtzite) are explained with their performance characteristics. Finally, energy band diagram of the semiconductor and the comparative analysis of Si, SiC, and GaN materials are presented. Comparative results confirm the eminence of the WBG devices over Si devices.

Chapter 3

Silicon Carbide Devices

3.1 Silicon Carbide Diodes

3.1.1 Introduction

A Schottky diode has a low forward voltage drop and a very fast switching action. There is a small voltage drop across the diode terminals when current flows through a diode. This lower voltage drop provides better system efficiency and higher switching speed. In a Schottky diode, a semiconductor–metal junction is formed between a semiconductor and a metal, thus creating a Schottky barrier. The SiC Schottky Barrier Diodes (SBD) have a number of advantages over Si diodes. The SiC SBD is commercially available in the 600-1200V /1-10A range. The main advantage of a high voltage SiC SBD comprises in its superior dynamic performance. The reverse recovery charge in the SiC SBD is extremely low (< 20 nC) and is the result of junction capacitance, not stored charge. Moreover, unlike the Si diode, it is independent of di/dt, forward current and temperature. A SiC Schottky diode has about 40 times lower reverse leakage current compared with p-n silicon Schottky diodes. Silicon carbide has a high thermal conductivity and temperature has little influence on its switching and thermal characteristics. With special packaging, it is possible to have operating junction temperatures of over 500K, which allows passive radiation cooling in aerospace applications. Standard silicon diodes have a forward voltage drop of about 0.6V and germanium diodes 0.3V. SiC technology delivers these benefits because no reverse recovery charge accumulates during the diode's conduction period. When a conventional

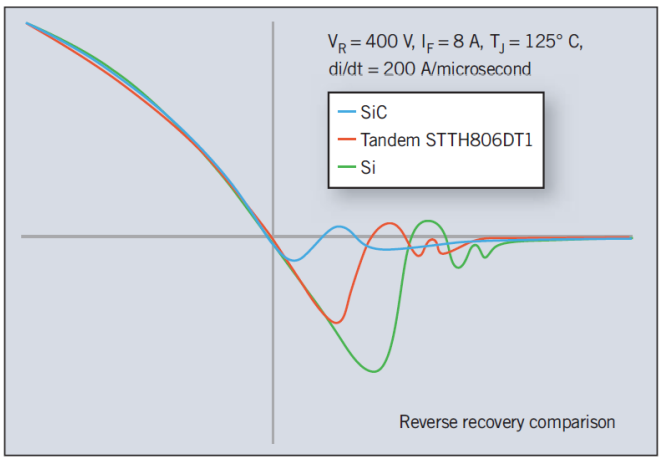


Fig. 3.1 The graph for reverse recovery comparison between a typical p-n Si-Schottky diode, ultra-fast STTH806DTI p-n Schottky diode and an STPSC606D SiC Schottky diode

bipolar silicon diode is turned off, this charge must be dispelled by recombination between groups of charge carriers close to the diode junction. The current flowing during this recombination period is called the reverse recovery current. This undesired current, when combined with the voltage across associated semiconductor power switches, generates heat that will be dissipated by the switches. By eliminating this reverse recovery charge, SiC Schottky diodes have much lower switching losses leading to higher efficiency and lower heat dissipation. Fig. 3.1 compares the reverse recovery of conventional p-n Schottky diode, an ultra-fast recovery silicon diode and an SiC Schottky diode.

3.1.2 Static Characterization

The main objective of carrying out the measurements for static characteristics is to determine the conduction loss of the specific devices, which help in designing the power converters. Fig. 3.2 shows the circuit diagram of a set up with test diodes in a temperature-controlled oven to obtain the characteristics of the diodes at different operating temperatures [5]. The variable dc supply voltage is provided, and the forward voltage and current of diode are measured at different load currents and several temperature values of up to 250 ^{o}C (the temperature limit of the oven). The curves obtained as a result of this test for both Si p-n and SiC Schottky diodes are given in Fig. 3.3 [5], in which it can be seen that the forward voltage of the SiC diode is higher than that of the Si diode. This is expected because of SiC's wider bandgap. The other difference between these two diodes is their high-temperature behavior.

As the temperature increases, the forward characteristics of the Si diode change severely, while those of the SiC diode stay confined to a narrow region. Note that the Si p-n diode has negative temperature coefficients while the Schottky diode has positive for on-state resistance; that is why the slope of the curve at higher currents is increasing in the case of Si diode and decreasing in the case of SiC diode with the increase in temperature. Only at low temperatures, SiC diodes have low on-resistance than that of Si diodes. However, Si diode has a lower voltage drop, which also decreases with temperature. Lower on-resistance and lower voltage drop imply lower conduction loss for the Si diode.

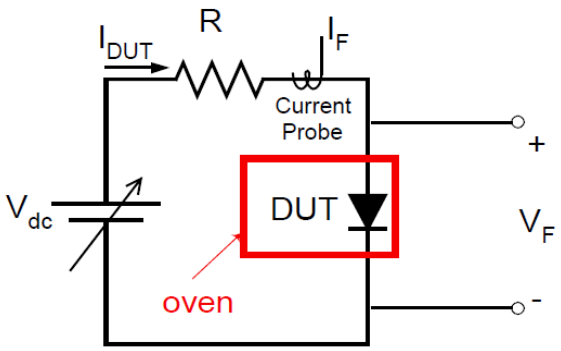


Fig. 3.2. Circuit diagram for V-I characterization of a diode

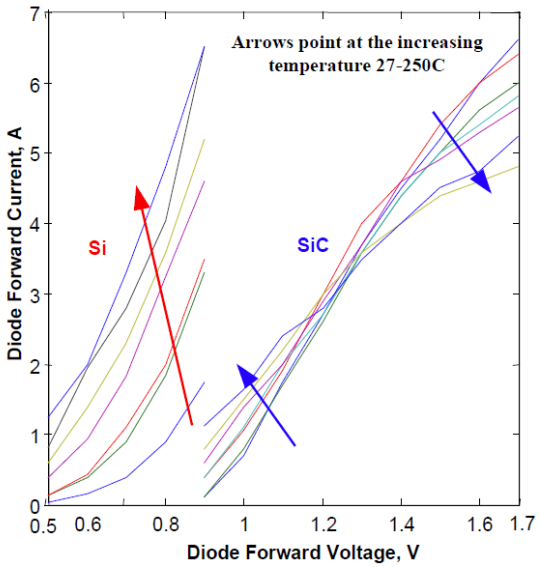


Fig. 3.3 Experimental V-I characteristics of the Si and SiC diodes in an operating temperature range of 27 ^{0}C to 250 ^{0}C

3.1.3 Dynamic Characterization

The dynamic characteristics of semiconductors, namely the switching losses information and switching behavior of the semiconductor devices are very important factor for the operation of power converters. The most important part of the diode switching losses is the reverse recovery loss. The rest of the losses are very less and can be neglected. The energy lost during reverse recovery has been calculated experimentally and reported in [5]. The SiC Schottky diodes, unlike p-n diodes, do not have reverse recovery behavior because they do not have minority carriers; however, they still show some reverse recovery effects. The main reason for these effects is the oscillation due to the parasitic device capacitance and the

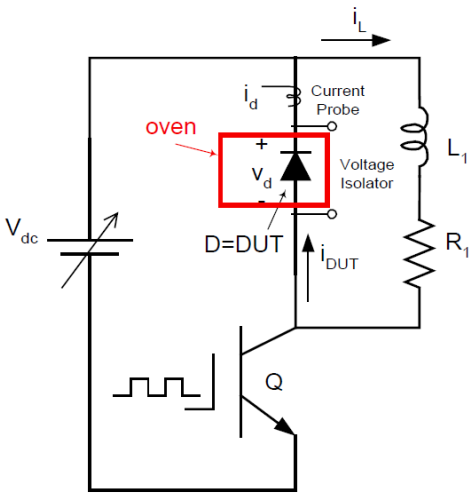


Fig.3.4 Circuit diagram for reverse recovery loss measurement

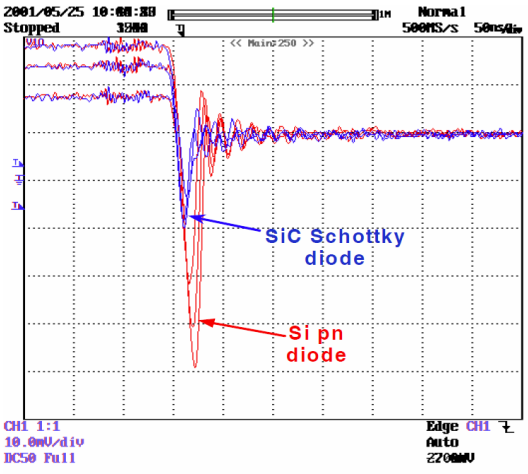


Fig. 3.5 Typical reverse recovery waveforms of the Si p-n and SiC Schottky diode for three different forward currents (2 A/div.)

inductances in the circuit. For this test, the chopper circuit in Fig. 3.4 was set up with test diodes in a temperature-controlled oven. The main switch is turned on and off at 1 kHz with a duty ratio of 75%. The typical Si and SiC diode turn-off waveforms are given in Fig. 3.5 for three different forward currents. These experimental waveforms show that the Si diode switching losses are almost three times more than those of the SiC diode. The peak reverse recovery current, and the reverse recovery current-time integral of the diodes are measured at different operating temperatures with varying load currents. The peak reverse recovery current with respect to the forward current at different temperatures is plotted in Fig. 3.6. The reverse recovery current of the Si diode is higher than that of the SiC diode at any

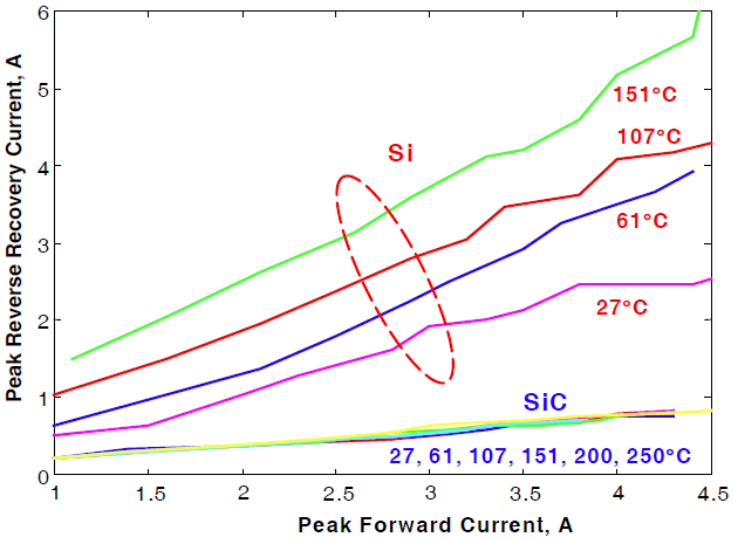


Fig. 3.6 Peak reverse recovery values with respect to the forward current at different operating temperatures

operating temperature. As the temperature increases, the difference increases because the reverse recovery current of the Si diode increases with temperature, but that of the SiC diode stays constant.

The reverse recovery current-time integral can be used to calculate the reverse recovery losses, and thus the diode switching losses. Assuming the diode sees a constant reverse voltage when it is off and it is switched at constant frequency, then

$$P_{rr} = f_s V_R \int_a^b i_d dt \tag{3.1}$$

Using the experimentally measured values in (3.1), reverse recovery losses for a 20 kHz operation with a 300 V reverse voltage are plotted in Fig. 3.7. As observed in this figure, the SiC Schottky diode switching losses, unlike those of the Si p-n diode, do not change much with temperature.

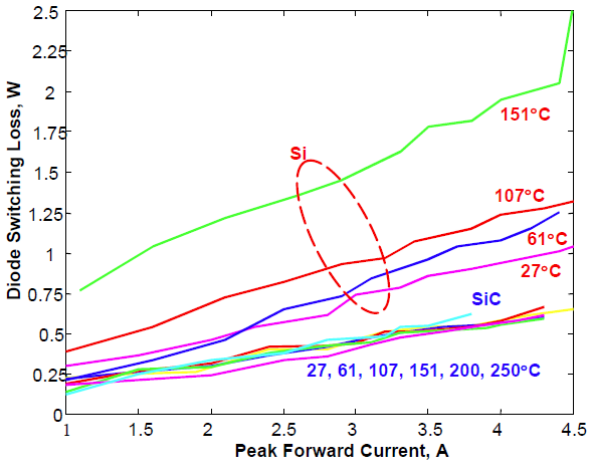


Fig. 3.7 Switching loss of Si and SiC diodes with respect to peak forward current at different operating temperatures

3.2 Silicon Carbide Power Transistors

Silicon carbide (SiC) offers several advantages as a semiconductor material over conventional Si. The SiC materials allow to develop a high capacity, low loss power transistor devices. The power converters that are designed by SiC devices are able to reduce the significant amount of losses as compared to conventional one. The SiC devices have the advantages like high efficiency, high operating frequency and wide range of operating temperature, which permit to think beyond the range of conventional devices. The SiC transistors are unipolar devices such as the junction field effect transistor (JFET), metal oxide silicon filed effect transistor (MOSFET) and bipolar junction transistor (BJT). The latter may seem to be a bipolar device, but from experiments, it is found that available 1,200-V SiC BJTs behave as unipolar devices in the sense that there are practically no dynamic

effects associated with build up or removal of excess charges. The reason for this is that the doping levels of 1200 V SiC transistors are so high that any considerable carrier injection is superfluous for the conduction mechanism. The market of the SiC devices is still on growing stage and today available SiC switches are the JFET, BJT and MOSFET only. There is no mass production for SiC devices for commercial purposes. Therefore, the cost of these devices is more as compared to Si devices. The driver circuit for these devices must be design in such manner that devices can be used for high efficient power converters.

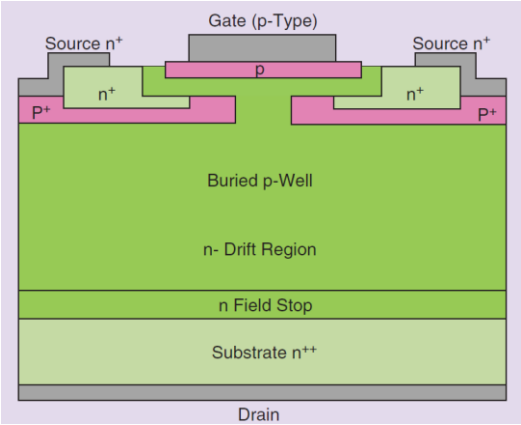


Fig. 3.8 Cross section of the normally on SiC LCJFET

3.2.1 SiC JFET

The SiC JFET was fabricated in early stage to realize the performance of SiC devices. There was so many drawbacks with these devices in early stage like low transconductance (i.e. the slope of the transfer characteristics in the active region) values, low channel mobilities and difficulties in the fabrication process. Later on the improvement on the SiC material and fabricated with the advance technology and first prototype samples of SiC JFETs were released in the market.

The modern designs of SiC JFET, which is named as lateral channel JFET (LCJFET) is shown in Fig. 3.8 [6]. The SiC JFET is a normally on device and to make it turn off require to feed a negative gate to source voltage. By applying a negative gate-source voltage, a certain space charge region develops, and hence width of channel is decreased and reduction in current is obtained. The specific value of gate-source voltage is called pinch-off voltage and under this voltage, the device current equals zero. The normal range of pinch-off voltages of this device is between -16 V and -26 V. The SiCED (Infineon) already released these types of SiC devices few years ago and it will be commercial in near future.

The Semisouth Laboratories released second type of available commercial SiC JFET that is vertical trench (VTJFET) in 2008. The schematic diagram of SiC VTJFET is shown in Fig. 3.9. The SiC VTJFET can be work either in normally off i.e. enhancement mode vertical trench junction field effect transistor (EMVTJFET) or in normally on i.e. depletion mode

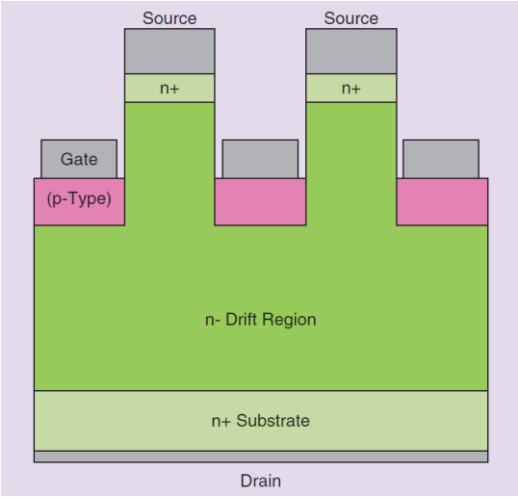


Fig. 3.9 Cross section of the SiC VTJFET

vertical trench junction field effect transistor (DMVTJFET) devices. The working function of devices depends on the thickness of the vertical channel and the doping levels of the structure. For the normally on JFET, a negative gate-source voltage is required to make it turn off. Once devices turned off, very low current is required to keep the JFET in off state. The pinch-off voltage for the DMVTJFET equals approximately -6V, while the positive pinch-off voltage for the normally off devices (EMVTJFET) is slightly higher than 1V.

The other additional SiC JFET designs are shown in Figs. 3.10 and 3.11. There are two different types of design, which are more commercial in the market. The schematic diagram of the cross section of buried grid JFET (BGJFET) is shown in Fig. 3.10, in which small cell pitch has been used which contributes to the low specific on state resistance and high saturation current densities. Moreover, the inherent similarities in the gate drive and the wide design window for the channel length, width, and level of doping make these devices more suitable for the power converters. The basic two disadvantages in designing this device as

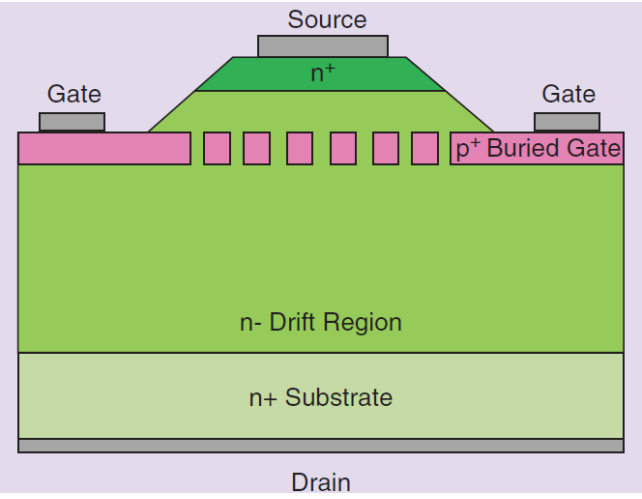


Fig. 3.10 Cross section of the SiC BGJFET

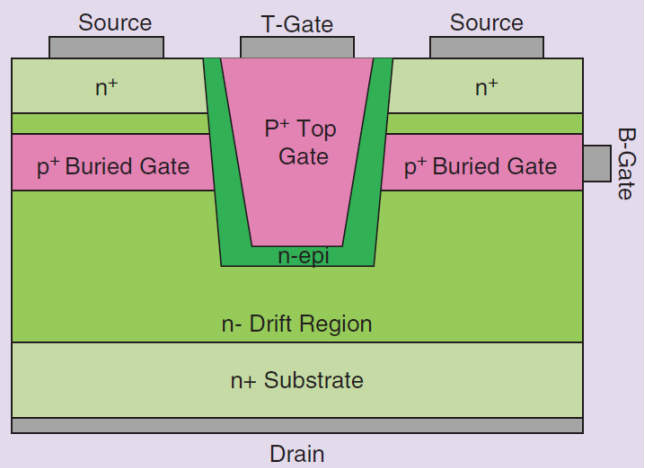


Fig. 3.11 Cross section of the SiC DGVTJFET.

compared to LCJFET, first is that they are more difficult to fabricate and other one is the absence of antiparallel body diode. In the case of implanted grid, the use of high doping in the channel is limited by the necessity to compensate the high-doped n-layer on top of the drift layer by the p-grid implant. The level of doping for the channel is limited by the tolerances of the photolithography and the trench etching process.

The double gate vertical channel trench JFET (DGVTJFET) is shown in Fig. 3.11, which is the combination of advantages of LCJFET and the BGJFET designs. The DGVTJFET offers the high current rating capabilities for normally off mode operation. Because of the small cell pitch and double gate control, this design is able to combine fast switching capability due to the low gate-drain capacitance with low specific on-state resistance. Normally off devices have high saturation current level because of the double gate driver and wide design window for the channel optimization. Moreover, due to the possibilities of using highly doped channels, the negative temperature dependence of the saturation current is reduced. Hence, these devices have advantages of the BGJFET, but the performance of BGJFET can surpass them due to the larger design window for the channel doping and width. Therefore, the gate to drain body p-n diode can be used in this process, but it is a matter of trade off with the possible saturation current density.

The SiC JFETs are commercially available of the rating of 1200V to 1700V. The normally on JFETs have the current rating up to 48A and on state resistances of 100, 85, 45 mΩ at the room temperature. Similarly, the normally off JFETs (EMVTJFETs) are available in market with the current rating up to 30A and on state resistances of 100 and 63 mΩ. Fig. 3.12 shows the on state voltage versus blocking voltage for various unipolar and bipolar SiC and Si power devices, in which there is a huge difference between the Si and SiC devices. Fig. 3.13 shows specific on-state resistance with the variation of temperature for different JFET structures. It can be observe that normally off devices have a weaker temperature dependence compared to the normally on devices [7]. The specific R_{on} of the normally off devices is dominated to a large extent by the channel resistance.

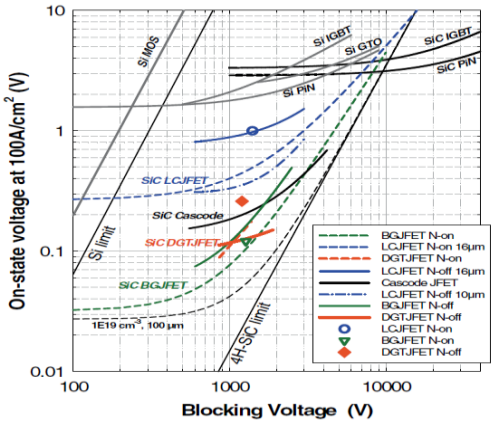


Fig. 3.12 On-state voltage versus blocking voltage for various unipolar and bipolar SiC and Si power devices

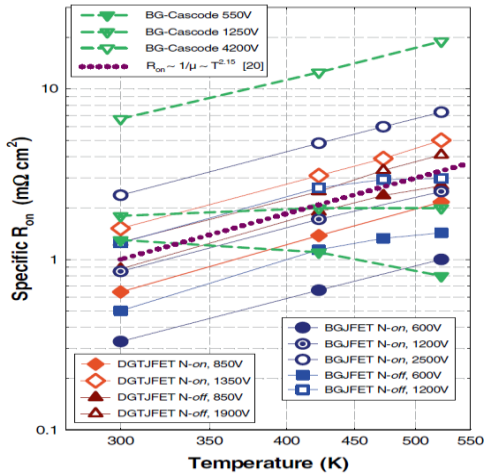


Fig. 3.13 Temperature dependence of the specific on-state resistance for different JFET structures

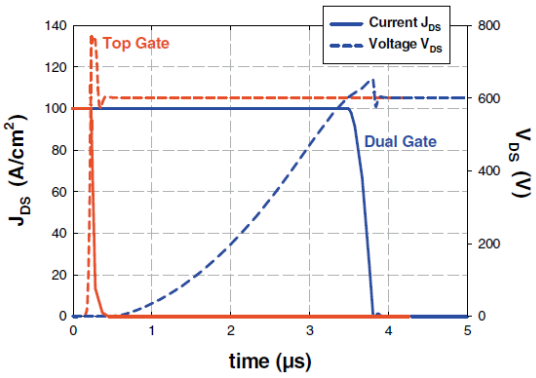


Fig. 3.14 Comparison of the top gate (red line) and double gate (blue line) switching characteristics of the normally-on LCJFET structure with 16 µm cell pitch

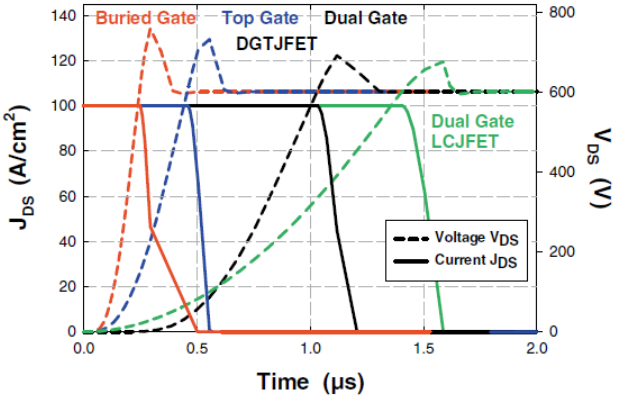


Fig. 3.15 Comparison of the switching characteristics of the normally-off DGTJFET using the buried gate (red line), the top gate (blue line), and both gates (black line) with a normally-off LCJFET with 10 µm cell pitch and double gate control (green line)

Fig. 3.14 shows the comparison of the top gate (red line) and double gate (blue line) switching characteristics of the normally on LCJFET structure with 16 µm cell pitch. The gate charge and turn-off losses have the high values in the top gate control as compared to double gate control, while the driving condition is the same for both cases. It can be observed from Fig. 3.14, the normally off LCJFET will necessarily suffer from slow switching speed since it needs double gate control in order to pass reasonable forward currents. The same comparison is shown in Fig. 3.15 for the normally off DGVTJFET structure and normally off LCJFET structure with cell pitch of 10 µm [7]. The overall turn off switching comparison shows that the sacrifice of the switching speed is much less severe for the DGVTJFET structure due to the much smaller cell pitch and thus the smaller Miller capacitance attributed to both the buried and top gates, respectively.

3.2.2 SiC BJT

The SiC bipolar junction transistor is a bipolar normally off device, which has many benefits such as low on-state voltage drop, high switching speed and high maximum

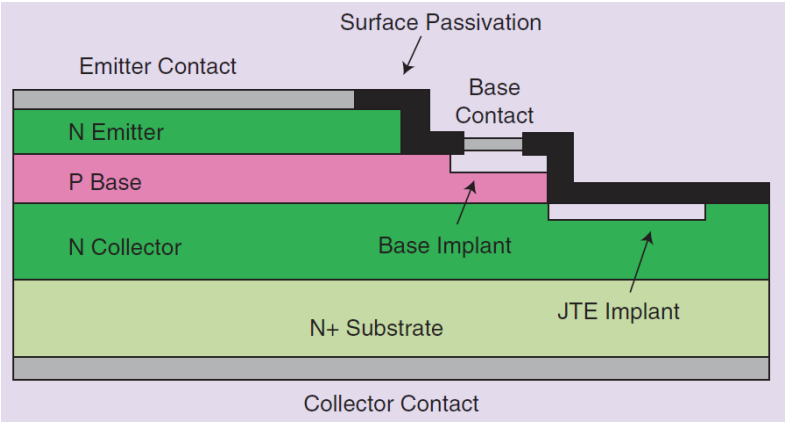


Fig. 3.16 Cross section of the SiC BJT

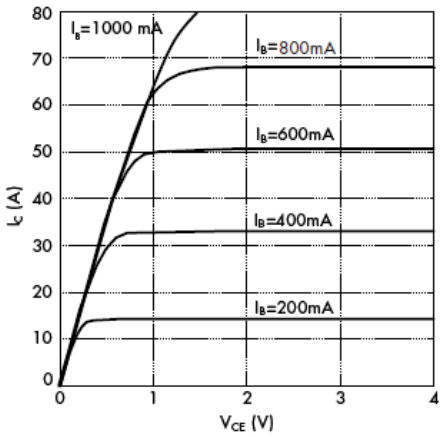


Fig. 3.17 Waveform of typical I-V Characteristics of SiC BJT

operating temperature. This is a current controlled device and hence there is a specific current is required to turn on the device. This is a major disadvantage of these devices, because it increases the power requirement of the driver circuit compared to voltage controlled devices like MOSFETs and IGBTs. The schematic diagram of cross section of SiC BJT is shown in Fig. 3.16, for an NPN configuration. Due to the cancellation of the base-emitter and base-collector junction voltages, the on-state voltage drop observed is very low. The voltage rating of SiC BJT available in market is of 1.2kV and the current ratings are in the range of 6-40A while the current gain at room temperature is of the order of 70.

Moreover, SiC BJT will be very favorable for application under a high ambient temperature, such as aerospace and military usage due to free of gate oxide. Therefore, a special base drive is required based on the properties of SiC BJT. For the proper operation of BJT device, a sufficient high pulse base current provides during turn on to minimizing the delay time and turn on switching losses. Hence, a base current required to be maintain in proportional to the collector current to ensure safety operation and reduced device on-state voltage drop. For obtaining faster turn off speed, the device should avoid getting into deep saturation region and a negative base current is required.

The Fig. 3.17 shows the V-I characteristics of SiC BJT at room temperature. In the saturation region, the SiC BJT exhibits ohmic region property as the Si MOSFET does. Since it has a positive thermal coefficient, SiC BJTs can be connected in parallel to handle very high current. The turn-on and turn-off characteristics with their wavforms are discussed in [8] for Si BJT and SiC BJT, Overall low switching losses have been observed in SiC BJT as compared to Si BJT, because of several advantages of wide gap semiconductor SiC devices.

3.2.3 SiC MOSFET

After a several years of research done on SiC MOSFET, the fabrication and stability of the oxide layer is still a challenging task for the manufacturers as well as researchers. The schematic diagram of cross section of SiC MOSFET is shown in Fig. 3.18. The normally off behavior of this device make it more favorable for designers of power electronics converters.

But there are trouble for these devices like the low channel mobilities that cause additional on-state resistance of the devices resulting in more on state power losses. Moreover, the reliability and stability of oxide layer, mainly for long periods and at elevated temperature have not been confirmed yet. The SiC MOSFETs are unipolar device that are capable of blocking a reverse voltage of more than 1 kV with a low resistance drift. Moreover, these devices have a wider forbidden band. Therefore, the concentration of charge carriers is much lower as compared to silicon and a specific on-resistance equal to 1 percent of that of silicon is obtained, thus helping to have a lower leakage current at higher temperatures. It also does not have tail current and the recovery time is extremely short. Therefore, it allows a more efficient operation at high frequencies and a reduction in size and volume resulting in decreased material costs.

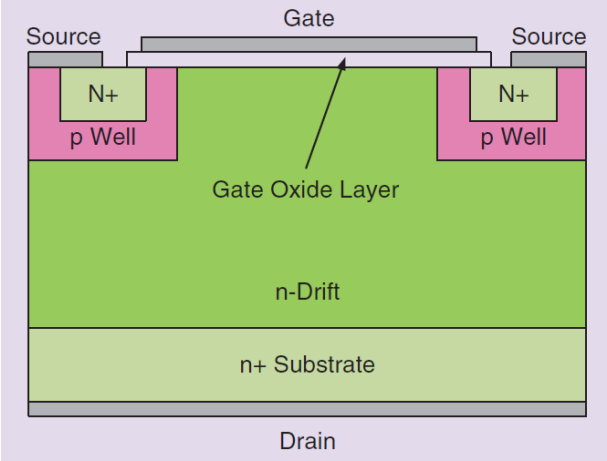


Fig. 3.18. Cross section of the SiC MOSFET

The SiC MOSFET is a voltage-controlled and normally off type device, which does not require continuous driving current to maintain the conduction state. Compared to a Si MOSFET, SiC MOSFETs have unique operating characteristics that should be considered when designing the gate drive circuit. The waveforms of I_D vs. V_{DS} of SiC MOSFET at different temperature is shown in Fig. 3.19. The waveform shows the variation in voltage and current when temperature changes from 25 ^{0}C to 135 ^{0}C. Fig. 3.20 demonstrates how the nominal threshold voltage is around 2.5V, and the device is not fully on until the V_{GS} is above 16V. Thus, the recommended on-state V_{GS} is 20 V for its full performance, whereas the recommended off-state V_{GS} is between -2 V to -5 V since the V_{GS} threshold has a low noise margin [9]. The important key point is that the temperature coefficient of the on resistance of the SiC JFET is smaller than that of the Si MOSFET. The on-resistance of the SiC MOSFET increases by about 20 percent when the junction temperature increases from 25°C to 135°C, whereas that of the Si MOSFET increases by 250 percent. The cause of this advantage results from the wide bandgap. Another important temperature related characteristic is that the zero gate leakage current of the SiC MOSFET does not rise much

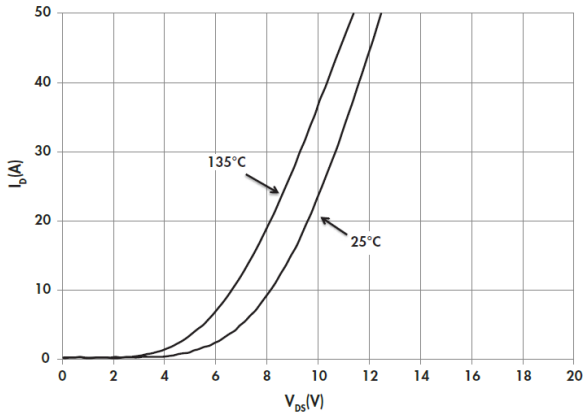


Fig. 3.19 Waveform of I_D vs. V_{DS} of SiC MOSFET for temperature at 25 ^{0}C and 135 ^{0}C

with temperature, whereas that of its Si counterpart increases around 100 times when the junction temperature increases from 25°C to 135°C.

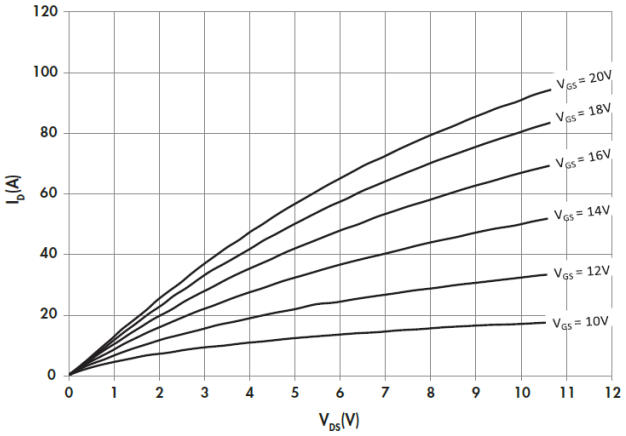


Fig. 3.20 Typical Transfer Characteristics of SiC MOSFET

3.3 Driver Circuit for SiC Devices

The special driver circuits are required for the advantageous performance of SiC devices as compared to Si devices. The driver circuit for the SiC devices must be design in such a manner that gate and base drivers should be able to provide fast switching performance with maintaining low consumtion of power. Considering the capability of SiC devices, to operate at high temperature, the drivers required proper investigation. The various driver circuits for SiC devices are discussed as follows.

3.3.1 Normally on SiC JFET gate driver

As well known the normally on SiC JFET is a voltage-controlled device. Therefore, a negative gate source voltage, which is less than the pinch-off voltage, is required to keep this device in the off state. The most widely used gate driver is shown in Figure 3.21. The circuit

has a parallel connected network consists of a high-value resistor R_p, a diode D and a capacitor C, while the gate resistor R_g is connected in series with the gate as discussed in [6].

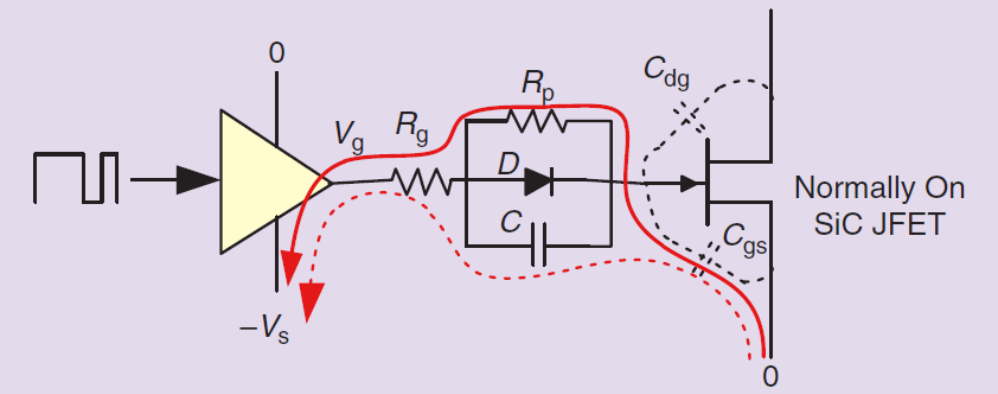


Fig. 3.21 Gate driver of the normally on SiC JFET

For the on duration of SiC JFET the output voltage of the buffer V_g is 0V, and the device is conducting the current. Once the JFET is turned off, buffer voltage V_g is changed from 0V to $-V_s$. At this instant a high peak current is given to the gate source junction of the JFET through the capacitor C and the gate resistor R_g as indicated by dashed line in the Fig. 3.21. Therefore, the parasitic capacitor across the gate to source C_{gs} is charged, and the voltage drop across the capacitor C is the voltage difference between $-V_s$ and breakdown voltage of the gate. Now only very low current is required to maintain the JFET in off mode. This current can be provided through the resistor R_p as shown by solid line in Fig. 3.21. The value of R_p must be chosen carefully to avoid the breakdown of the gate source junction. The switching performance can be regulate by changing the value of gate resistor R_g. The switching performance of this gate driver, when it used with a SiC low channel junction field effect transistor (LCJFET) is discussed in details in [6].

There are lot of advantages of normally on SiC JFET but still this device has a main problem of destructive shoot through, when the power supply for the gate is lost. Therefore, it is necessary to design a smart driver circuit to overcome such problems.

3.3.2 Normally off SiC JFET gate driver

The normally off SiC enhancement mode vertical trench junction field effect transistor (EMVTJFET) is a voltage control device. Therefore a substantial gate current is required during the conduction state to achieve a reasonable on state resistance. Moreover, high peak gate current is required to fast charging for the gate-source capacitance, so that operation of the device will be faster. A two stage gate driver with suitable resistor is shown in Fig. 3.22 for a 1200 V/ 30 A normally off JFET. The driver circuit consists of two stage, one is dynamic and other one is static. The dynamic stage has a standard driver with a resistor R_{B2}, which provides high voltage and hence high current peaks during a short time period to turn the JFET on and off rapidly. Once the dynamic stage has completed then second stage starts

working. The second stage is static one with dc/dc step down converter, a BJT, and a resistor R_{B1}. The auxiliary BJT is turned on when the dynamic stage is completed. This stage is able to provide a gate current of approximately 200 mA during the on state of the JFET. The biggest advantage of this driver is that there is no need of speed-up capacitor, which might cause duty ratio limitations because of the associated charging and discharging times.

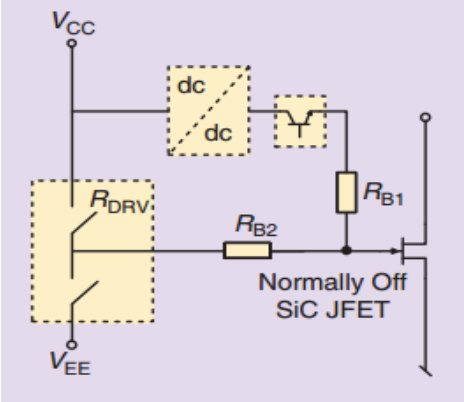


Fig. 3.22 Circuit diagram for two-stage gate-driver for normally off SiC JFETs [6]

The device ultimately limits transition speed, turn-on and turn-off times of the SiC JFET. Moreover, the performance of the gate driver can affect this speed considerably. Specific to the SiC VTJFET are two main requirements that must be satisfied by the gate driver; (i) delivery/removal of dynamic gate charge and (ii) sustainability of dc gate voltage and resulting gate-source current during the conduction period. The ability of the gate driver to quickly deliver/remove the necessary gate charge required by the internal gate-source and Miller capacitance of the device is the main factor that affects the time it takes for the device to transit between states. The gate drivers should also be designed to efficiently maintain the steady state dc gate voltage and gate current required to maintain minimum $R_{DS(ON)}$ during conduction.

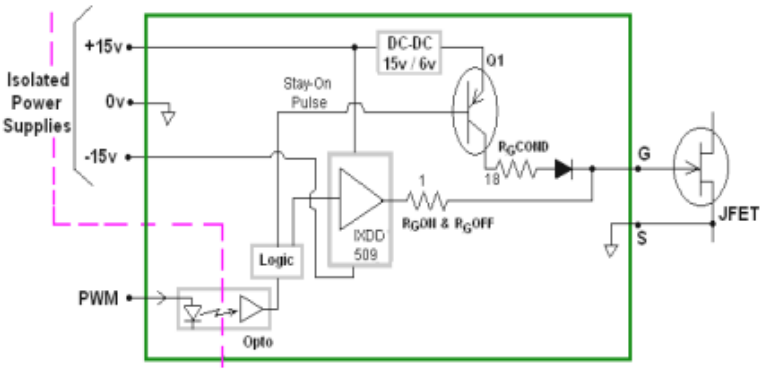


Fig. 3.23 Isolated, two-stage gate driver for SJEP120R050 [10]

Another type of gate driver circuit is shown in Fig. 3.23, which is the isolated two stage gate driver circuit for SiC JFET (SJEP120R050). It requires three user inputs; an isolated +/- 15V voltage supply and a user input PWM control pulse. An optocoupler is included at the input such that the necessary isolation is achieved if using this circuit in the high side position. The output of this optocoupler is then passed to a logic/timing circuit that generates the timing signals for the first and second driver stages. A short duration on pulse (typically ~100ns) is input to first driver stage. An IXYS IXDD509 driver IC is used to deliver the high peak current (+/- 9A) necessary for quickly charging the device input capacitance thus quickly turning on the device. The output of the IXDD509 is connected to the gate by a series low-ohm gate resistor (typically ~1-5 ohm). A second pulse that matches the full duration of the user input control pulse is inverted and applied to the base of a small PNP transistor used to provide the required on-state gate current of <200mA for maintaining a low $R_{DS(ON)}$ during the conduction period. The gate current is set by the value of a second gate resistor based on Equation (3.1).

$$R_G = \frac{V_0 - V_G}{I_{G(@VG)}} \tag{3.1}$$

The switching losses for the SJEP120R050 SiC JFET using the optimized two-stage dc coupled gate driver circuit and Typical switching waveforms are illustrated in details in [10].

3.3.3 Gate driver for SiC MOSFET

The gate driver circuit is also the most important component after the semiconductor for the better performance of the devices. Driving SiC power semiconductors with not properly selected or tailored drivers would mean losing the possible performance enhancement that SiC devices can provide. Therefore, it is necessary that each semiconductor device must be tested with the driver circuit that can properly highlights the performance of the device. The typical gate driver circuit for SiC MOSFET is shown in Fig. 3.24. A simple gate driver that drives the device under test (DUT) with two voltage levels (e.g. + 15 V and 0 V or hv_gnd) through a gate resistor. This driver and its variants (different voltage levels) are used for

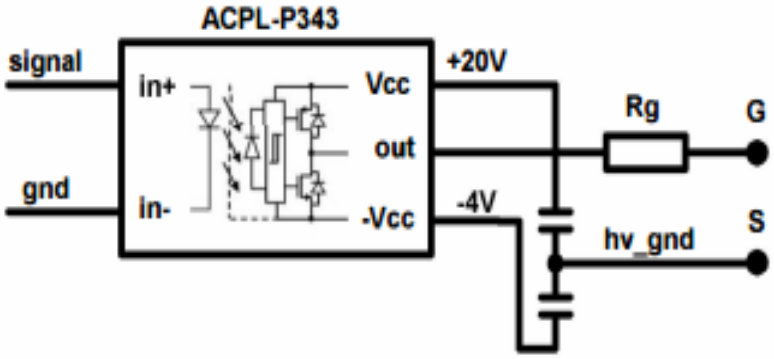


Fig. 3.24 Gate driver circuit for SiC MOSFET [11]

driving SiC MOSFETs. In this case, the gate driver components are reduced minimizing also the complexity and cost of the circuitry

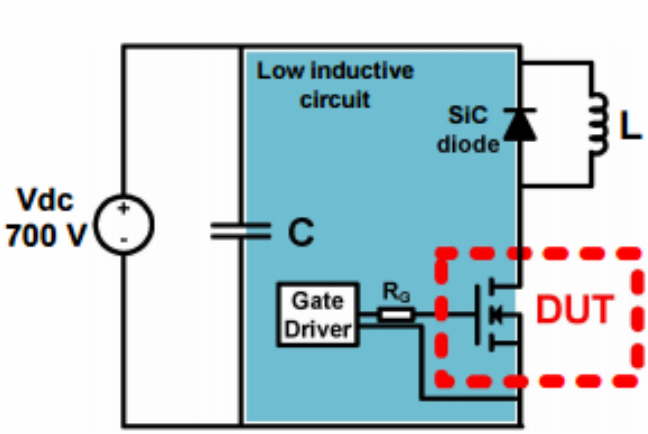
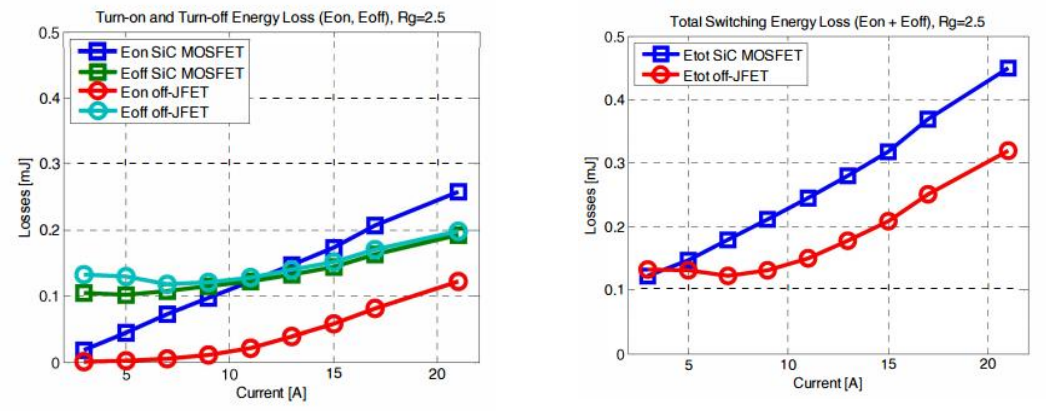


Fig. 3.25 Inductive clamp test circuit used for testing the devices [11]

The test setup based on the inductive clamp circuit is shown in Fig. 3.25. This test applies two short current pulses to measure the turn-on and turn-off behavior of the devices under tests (DUTs). The pulse duration is small (1-10 µs) and the overall energy dissipated during the pulses is not sufficient to increase the device temperature. The detail analysis of the switching behaviour for the SiC MOSFET with the above driver circuit is discussed in [11]. The graphs for turn on losses, turn off losses and total switching losses with the variation of currents are shown in Fig. 3.26. The graph also shows the comparison between SiC MOSFET and SiC JFET with current range 3-21 A, MOSFET and SiC JFET with current range 3-21 A, dc-link voltage 700 V and scale of losses 0-0.5 mJ.



(a) Turn-on and turn-off losses (b) Total switching loss

Fig. 3.26 The graph between losses and current for SiC off-JFET and SiC MOSFET current range 3-21 A, dc-link voltage 700 V, scale of losses 0-0.5 mJ [11]

3.4 Summary

Silicon carbide devices mainly diode, JFET, BJT, and MOSEFT are illustrated in this chapter. Dynamic and static characteristics of the schottky barrier diodes are described in details. Structure of various SiC devices (i.e. JFETs, BJTs, and MOSFETs) is discussed with their schematic diagram. The various characteristics of the SiC transistors and a comparative analysis with Si devices have been explained, which ensure the greatness of SiC devices over Si devices. Finally, the driver circuit of the normally on SiC JFET, normally off SiC JFET and SiC MOSFET are discussed which confirm the performance of SiC devices even more better with using modern driving circuit.

Chapter 4

Gallium Nitride Devices

4.1 Gallium Nitride Power MOSFET

The schematic diagram of Galllium Nitride (GaN) power MOSFET is shown in Fig. 4.1. Aluminum Nitride (AlN) is used between Si layer and GaN layer to isolate the device structure from the substrate. Above the AlN layer GaN is used, after that an electron generating material is applied to the GaN. This layer creates a GaN layer with an abundance of electrons just below it that is highly conductive. For turning on the transistor, a positive voltage is applied to the gate in the same manner as turning on an n-channel, enhancement mode power MOSFET.

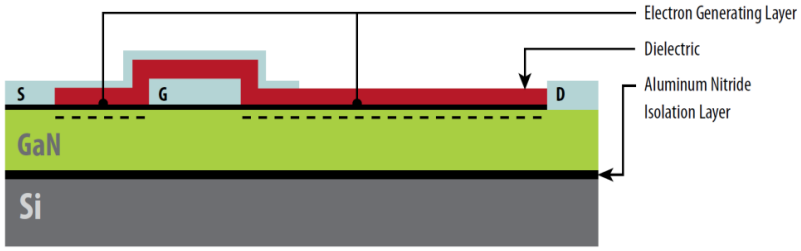


Fig. 4.1 Structure of GaN Power MOSFET

This device behaves similarly to Silicon MOSFETs with few exceptions. When a positive bias voltage V_{GS} is applied to the gate, the field is affected and attracts electrons that complete a bidirectional channel between the drain and the source. Since the electrons are pooled, as opposed to being loosely trapped in a lattice, the resistance of this channel is quite low. When the bias voltage is removed, the electrons under it are dispersed into the GaN and once again recreate the depletion region and giving it the capability to block the voltage. To model a device for high voltage application, the distance between Drain and Gate is increased. As the resistivity of the GaN pool is very low, the impact on resistance of increasing blocking voltage capability is much lower when compared with Silicon as discussed in chapter 2.

Fig. 4.2 Shows the transfer characteristics diagram for the GaN, in which the curves are plotted between Drain current I_D and Gate to Source voltage V_{GS}. The red line indicates the characteristics at 25 ^{0}C temperature while the green line for the temperature at 125 ^{0}C, the Drain to Source voltage V_{DS} is constant i.e. 3V. It means that, in spite of the wide variation of temperature, the characteristics are very similar. Fig. 4.3 shows the graph between on-

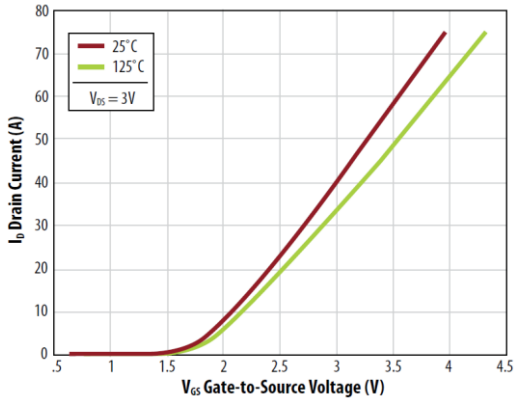


Fig. 4.2 Transfer characteristics curve for GaN

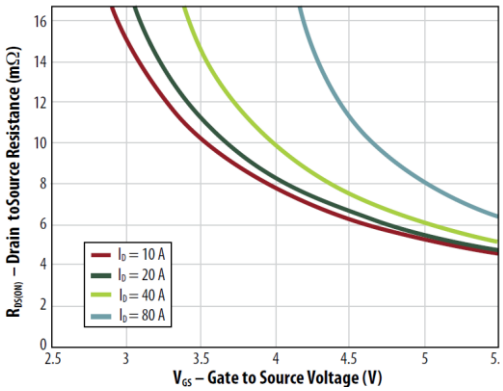


Fig. 4.3 $R_{DS(on)}$ vs. V_{GS} at various currents

resistance $R_{DS(on)}$ and Gate to Source voltage V_{GS} for different values of currents, which are similar to MOSFETs.

4.2 Driver Circuit for GaN Devices

As like SiC devices, special driver circuits are required for exploiting the advantageous performance of GaN devices. The driver circuit must be designed in such a manner so that gate and base drivers should be able to provide fast switching response for the GaN devices together with the amount of power consumption during operation must be low. In addition, considering the high operating temperature capabilities of GaN devices, the driver circuits required special attention while designing. The various driver circuits for GaN devices are discussed as follows.

4.2.1 Gate Driver for GaN Transistor

The GaN transistor has better characteristics than those of the SiC for the high frequency operation, with better efficiency even if a reverse current follows through the drain-source in FET, but it has the demerits of having a low threshold voltage. The GaN transistor is noise sensitive device particularly in the high frequency applications. Moreover, if high voltage is

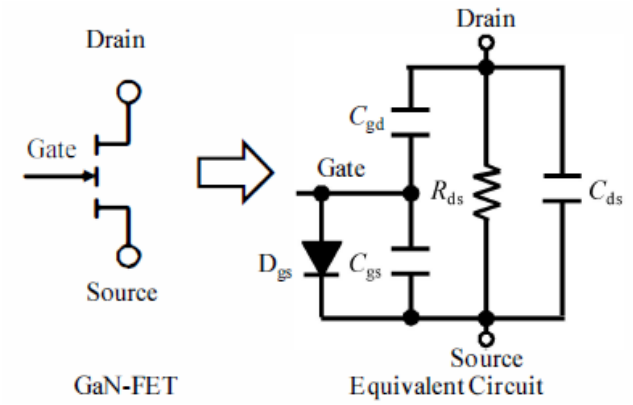


Fig. 4.4 Equivalent circuit of a GaN FET

applied across the gate-source, high current will flow between gate and source because the structure is not isolated. The equivalent circuit diagram of GaN FET is shown in Fig. 4.4.

A simple voltage divider control circuit is shown in Fig. 4.5. The GaN FET has a different kind of control circuit which is not similar to the control used by the typical MOSFET gate-source because a large current would flow and would increase the losses. In that case it must be added in parallel to the gate resistance R_{g1}, a capacitor and a further speed-up resistor. However, in the control circuit of the figure, the negative voltage is applied to the gate-source when the GaN transistor is in off-state.

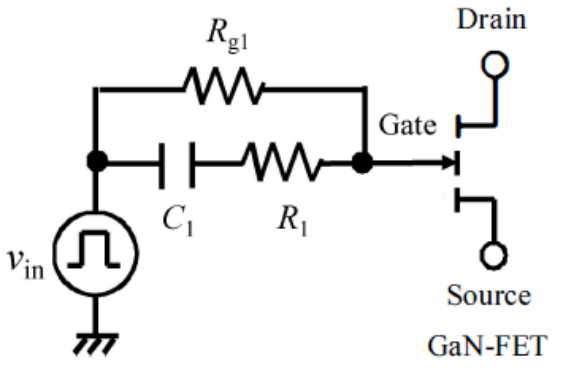


Fig. 4.5 Circuit diagram of voltage divider for GaN FET

The active dischargeable control circuit is shown in Fig. 4.6. As shown in the figure, the control voltage is added to a dividing circuit composed of a resistor, a speed-up capacitor, a p-channel MOSFET and a diode. The capacitance and additional resistance is used to control the p-channel MOSFET. With the circuit of the figure, the gate-source voltage of the transistor GaN becomes very negative at the time of turn-off and is blocked by the diode momentarily. Moreover, if required more high speed turn-off, another resistor can be put in series with the Q_1. The diode serves to limit the gate-source voltage to reduce losses during the reverse conduction but still there are some losses.

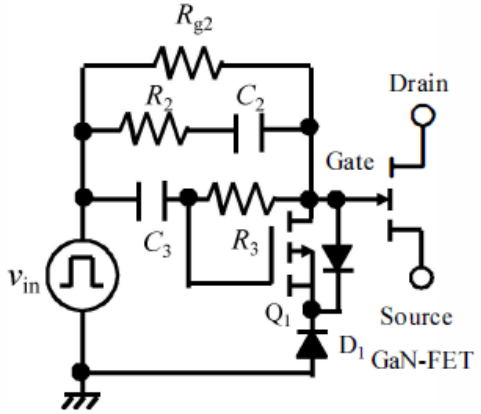


Fig. 4.6 Circuit diagram of active dischargeable unit

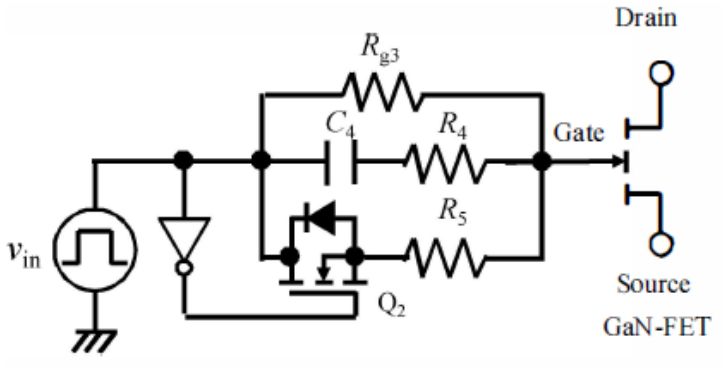


Fig. 4.7 Modified driving control circuit

The modified control circuit is shown in Fig. 4.7. In this case a logic inverter is installed with an n-channel MOSFET and a resistor in addition to the voltage dividing control circuit. The logic inverter is used to activate the additional MOSFET when the transistor GaN is brought in off-state. The resistance R_5 is used to speed up the turn-off process of the GaN FET. In this configuration, there are a diode clamp and a capacitor to adjust the auxiliary switch.

The equivalent circuit of modified control unit is shown in Fig. 4.8, the operation of this driver can be divided in six ways:

Mode 1: The capacitor C_{iss} and C_4 is charged. The gate-source voltage which is determined by quantity of the electric charge of the parasitic capacitance C_{iss} rises up until the threshold voltage V_{th} of the parasitic diode D_{gs}.

Mode 2: After completing the charging of the parasitic capacitance post of C_{iss}, current flows through the diode D_{gs} and parasitic capacitance C_4 charges until the voltage becomes v_{in}-V_{th}.

Mode 3: After completing the charging of the parasitic capacitance C_4, all the current from v_{in} flow through the resistance R_{g3}.

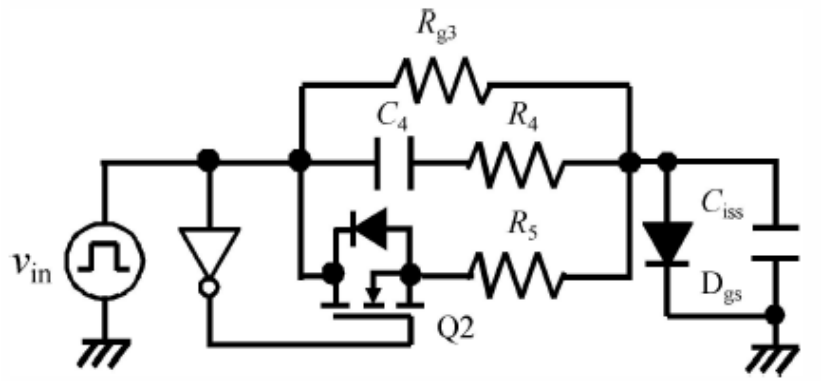
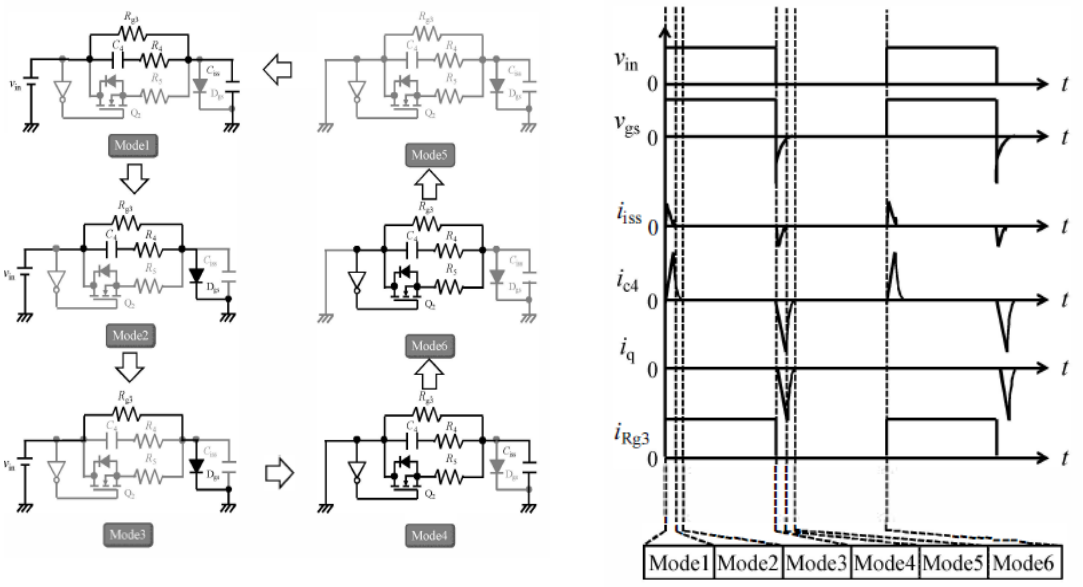


Fig. 4.8 Equivalent circuit of the modified control unit of GaN FETs [12]

Mode 4: The input is connected to ground and now Q_2 becomes turn-on because it inverts the input pulse. The parasitic capacitance C_{iss} and capacitance C_4 discharge until the voltage becomes 0.



Different modes of operation. Waveforms of the modified control circuit

Fig. 4.9 Different modes of operation and waveforms of the modified control circuit

Mode 5: After the parasitic capacitance C_{iss} is discharged, the capacitance C_4 continues to discharging through resistance R_4 and R_5. In this time, its discharge depends on the time constant of the capacitance C_4 and resistance R_4 and R_5.

Mode 6: there is no current flow because the capacitance C_4 is discharged completely.

All the modes of operation and waveforms of driver circuit are shown in Fig. 4.9. The loss of each drive circuit is compared while driving from 10 kHz to 1 MHz is shown in Fig. 4.10. Even though the loss of the active dischargeable type is almost same as the proposed type in [12], the loss proposed circuit becomes larger than the active dischargeable type at

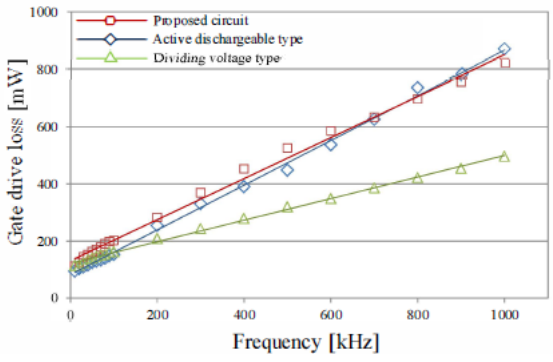


Fig. 4.10 Comparison of losses for different driving control units

the point of about 700 kHz. This is caused by not discharging the auxiliary capacitance completely.

However, it should be noted that usually the reverse conduction losses are larger than the loss of control; therefore it is better to use the voltage dividing circuit configurations, where reverse conduction does not occur.

4.2.2 Gate Driver for GaN Power MOSHFET

Designing a switch that works at high frequency is not an easy task, because these high speeds create more difficulties to maintain high efficiency. When a switch operates at very high frequency, its switching power loss increases rapidly and the overall efficiency reduces. The other challenge for GaN metal oxide semiconductor hetero-structure field effect transistor (MOSHFET) is that it needs a zero voltage to turn on and a negative voltage to turn off. Therefore, the driver circuit for the GaN-MOSHFETs must be different as compared to conventional MOSFETs. The Fig. 4.11 shows the schematic diagram of resonant drive circuit for GaN Power MOSHFET. There are two MOSFETs (P-channel and N-channel) which are connected in such a way so that both the MOSFETS can turn on or off to control the gate signal of GaN MOSHFET. The inductance L_R is directly connected to the gate so that the parasitic capacitance C_{iss} and L_R become in resonance. The waveforms of this driving circuit are shown in Fig. 4.12.

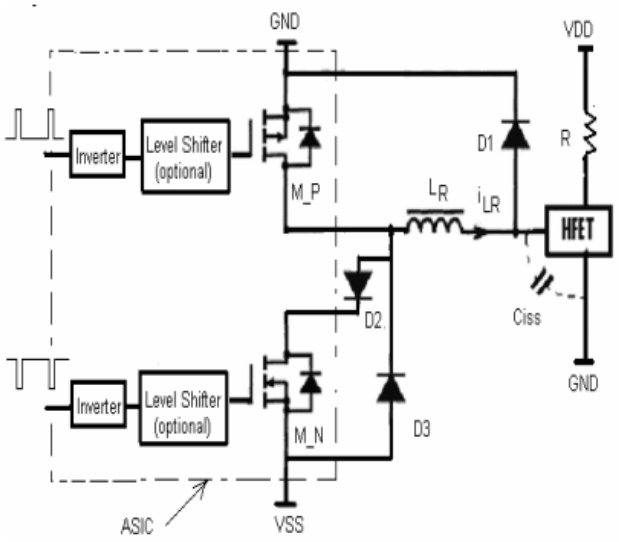


Fig. 4.11 Schematic diagram of resonant drive circuit for GaN Power MOSHFET [13]

The operation of the circuit is illustrated as follows. Let us suppose an operation beginning at the negative storage position when V_{GS}_MOSHFET is equal to V_p- and both M_P and M_N are turned off. At time t=0, when M_P turns on, the inductor current i_{L_R} starts to flow and charges the parasitic capacitor C_{iss} of the MOSHFET switch. When the voltage across the C_{iss} reaches the value slightly higher than zero at t_1, the diode D_1 conducts and

clamps V_{GS}_MOSHFET at zero, whilst the inductor current continues to flow freewheeling along D_1. At time t_2, when M_P turns off, the inductor current decreases, which makes the diode D_3 conduct. The inductor current flows through the path V_{SS}-D_3- L_R -D_1-GND and returns energy back to the voltage source.

Between t_2 and t_3, the inductor current i_{L_R} decreases from I_p to zero and the gate-source voltage of the switch remains at zero. At time t_4, transistor M_N turns on and the inductor current starts to flow in the opposite direction, discharging the MOSHFET parasitic capacitor C_{iss} until the voltage across C_{iss} reaches the maximum value V_p- at t_5.

$$V_{p-} = \frac{2V_{SS}}{\pi R_G}\sqrt{\frac{L_R}{C_{iss}}} + \frac{V_{SS}}{2} \tag{4.1}$$

At the same time, the diode D_2 prevents the opposite resonant inductor current from flowing and the voltage V_{GS}_MOSHFET remains at V_p- until the transistor M_P turns on at t_6; then the same process repeats. In equation (4.1), the effect of the diode is neglected since Schottky diodes are used and the forward voltage is very small compared to the source voltage.

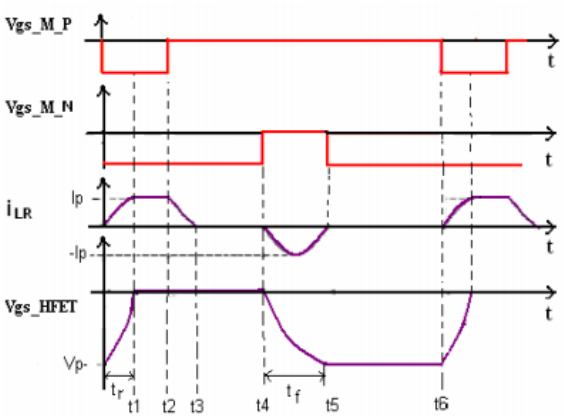


Fig. 4.12 Waveforms of resonant drive Circuit for GaN Power MOSHFET [13]

The inductor current and the power loss can be written as follows,

$$I_{L_R} = \frac{2V_{SS}}{\sqrt{4L_R/C_{iss}}} e^{-\left(\frac{R_G}{2L_R}\right)t} \sin\left(\frac{\sqrt{4L_R/C_{iss} - R_G^2}}{2L_R}t\right) \tag{4.2}$$

$$P_{loss} = \frac{R_G}{R_G + Z_o} P_{consume} \tag{4.3}$$

The equation (4.3) confirms that the power loss is depend on the parasitic gate resistance of the GaN. Where, R_G is the equivalent gate resistance, including the parasitic gate resistor of the power MOSFET switches, the on resistances of the drive transistors, and the parasitic

resistance of the inductor, among others. The C_{iss} is the parasitic capacitance of the GaN power MOSHFET. The Z_o is the *L-C* circuit characteristic impedance, can be calculated as,

$$Z_o = \sqrt{\frac{L_R}{C_{iss}}} \tag{4.4}$$

This circuit simplifies the role of the shifter circuit and reduces the overall power loss. As shown in Fig. 4.15 and equation (4.1), when M_N turns on, a negative inductor current begins to discharge the gate-source capacitor, and if the gate parasitic resistance of the GaN switch is small, the gate source voltage starts to decrease and can reach a higher-level negative peak value *Vp*. Therefore, power consumed in this circuit can be written as,

$$P_{consume} = Q_G V_{SS} f_s = C_{iss} V_{pp} V_{SS} f_s = C_{iss} \left| V_{p-} \right| V_{SS} f_s \tag{4.5}$$

where V_{pp} is the peak-peak voltage across the capacitor C_{iss}. Combining Equations (4.3) and (4.5), the power loss in this drive circuit is described by the following equation,

$$P_{loss} = \frac{R_G}{R_G + Z_o} \left(C_{iss} \left| V_{p-} \right| V_{SS} f \right) \tag{4.6}$$

Because the turn-off transient is not regulated by voltage clamp diodes, the absolute value of V_p is greater than the absolute value of V_{SS}. A small voltage source can be used to generate a higher gate-source voltage for the switch, and this function will lower the demand for a level shifter circuit and simultaneously reduce the power loss of the circuit.

4.3 Summary

This chapter explains the structure and characteristics of GaN Devices. The transfer characteristics curve at different temperature and the curve between $R_{DS(on)}$ and gate to source voltage V_{GS} at different currents are presented. Finally, the various driving circuits are discussed for GaN devices that imply the requirement of novel driving circuits for the better performance of GaN devices compared to conventional Si devices.

Chapter 5

Loss Analysis of Power Devices

5.1 Loss Structure

The total power loss of a device can be broken down as shown in Fig. 5.1. Blocking power losses are proportional to the leakage current of the device and to the applied reverse voltage; usually they are negligible with respect to the other loss components and their contribution will be disregarded. Switching and driving losses appear in the transient between one time interval and the following one, while conduction losses happens during the steady state condition along the intervals.

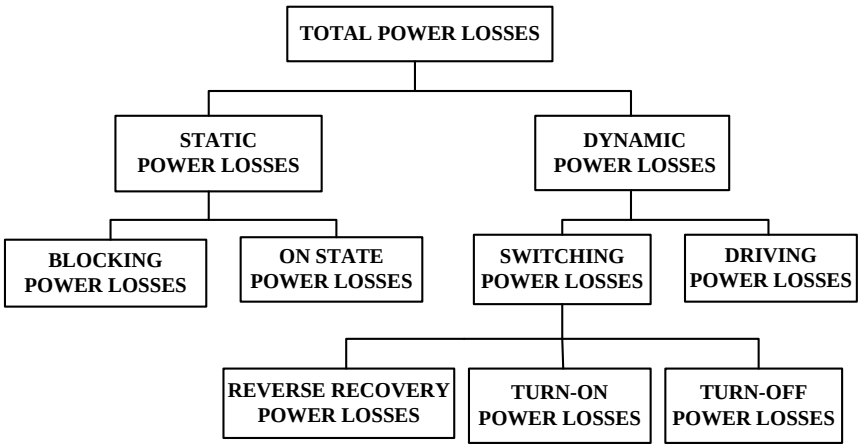
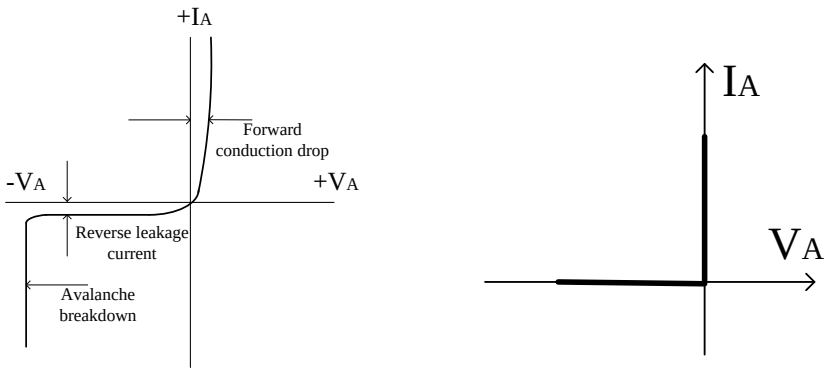


Fig. 5.1 Power losses source

The loss analysis of devices is very important factor that has the significant effects in measuring the efficiency of the power converter. Some part of the loss component as shown in Fig. 5.1 can be neglected because of their less significance based on the material of the devices.

5.2 Losses in Silicon Diodes

Diode is an uncontrolled device constructed to allow current to flow in one direction. It permits an electric current to pass in forward direction and block the current in reverse direction. The unidirectional behavior of diode is named as rectification and is used to convert alternating current to direct current. The power diodes are also used in the application such as electroplating, anodizing, battery charging, welding, power supplies, and variable frequency drives. The v-i characteristics of practical diode is shown in Fig.5.2 (a).



(a) Practical (b) Ideal

Fig. 5.2 Volt-ampere characteristics of diode

In the case of forward biased diode start to conduct with very small voltage also called forward biased voltage while in case of reverse biased very small leakage current (which is negligible) flows through the device until the reverse breakdown voltage is reached. Since diode having very small forward biased voltage in conducting state and very small leakage current in reverse biased means blocking state then the comparison of these values with the operating voltage and currents of the circuit in which diode is used, can be idealized and hence the ideal v-i characteristic of the diode is shown in Fig.5.2(b).

5.2.1 Switching characteristics

The waveforms of voltage and current of a power diode driven by currents with a specified rate of rise during turn-on and a specified rate of fall during turn-off is shown in Fig. 5.3. The turn on behaviour of the diode encompassed by the time interval t_1 and t_2. During time interval t_1, the space charge stored in the depletion region because of the large reverse-bias voltage is removed (discharged) by the growth of the forward current. While in t_2 time interval, the excess-carrier distribution in the drift region grows towards the steady-state value that can be supported by the forward diode current I_F. As discussed before conduction voltage V_{on} is very small in the forward high conduction region. At this condition, the P and N regions very near to the junction and the intrinsic semiconductor layer remain saturated with minority carriers.

If the devices left open circuited for a long time then carrier will be vanished automatically by the process of recombination. Therefore, for making turn off the devices it is necessary to apply the reverse dc voltage V_R. Fig. 5.3 shows that after applying the reverse voltage at $t=t_3$, current goes down linearly due to the series circuit inductance. During time interval t_3, current start decreasing linearly and end of t_3 it attained zero value and continue decreasing during t_4 and goes to negative and maintain the negative current slope while the minority carriers sweep out across the junction but the excess carrier concentration keeps the junction saturated. The result of the reduction in ohmic (equivalent resistance) drop the

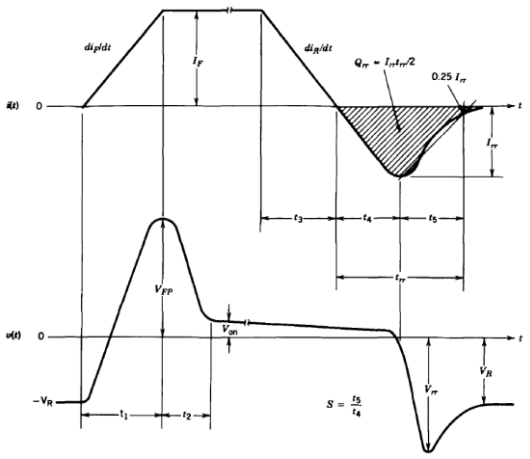


Fig. 5.3 The waveforms of voltage and current of a power diode driven by currents with a specified rate of rise during turn-on and a specified rate of fall during turn-off

conduction loss decreases during t_3 and t_4. The device sustains voltage appears at the end of t_4 and study state voltage at the end of t_5 while the during t_5 reverse currents falls partially by sweeping out and partially by recombination. Therefore, the total reverse recovery time $t_{rr}= t_4+t_5$ and the corresponding recovery charge Q_{rr} indicated by hatched area as shown in Fig. 5.3. Q_{rr} and t_{rr} both are highly affected by the process of recombination, which depends on important parameters of the diode. V_{rr} is the reverse recovery voltage and I_{rr} is reverse recovery current. V_{rrm} and I_{rrm} are the peak values of the reverse recovery voltage and reverse recovery current respectively. The reverse recovery current is responsible for additional loss which is called switching loss in the diode. From Fig. 5.3, I_{rr} can be given by

$$I_{rr} = \frac{di_R}{dt} t_4 = \frac{di_R}{dt} \frac{t_{rr}}{S+1} \tag{5.1}$$

where $t_4 = t_{rr} - t_5 = \frac{t_{rr}}{S+1}$, and S is the softness factor or snappiness factor which is defined as the ratio of the transient time t_5 to the storage time t_4,i.e. $S = \frac{t_5}{t_4}$. From Fig 5.3, $Q_{rr} = \frac{1}{2} I_{rr} t_{rr}$. Therefore,

$$Q_{rr} = \frac{di_R}{dt} \frac{t_{rr}^2}{2(S+1)} \tag{5.2}$$

From equation (5.2), the reverse recovery time is given by,

$$t_{rr} = \sqrt{\frac{2Q_{rr}(1+S)}{di_R/dt}} \tag{5.3}$$

Putting the value of t_{rr} in equation (5.1), reverse recovery current can be written as,

$$I_{rr} = \sqrt{\frac{2Q_{rr}\, di_R/dt}{(1+S)}} \tag{5.4}$$

The charge Q_{rr} represents the portion of the total charge Q_F (charge store in the diode during forward bias), which is swept out by the reverse current and not lost to internal recombination.

5.2.2 Power losses in diode

The total power loss in diode is the sum of the total conduction loss and switching loss, can be calculated as .

Total conduction loss

$$P_{cond} = P_{on} + P_{off} = V_f I_{on} + V_{off} I_{rev} \approx 0 \tag{5.5}$$

Total switching loss,

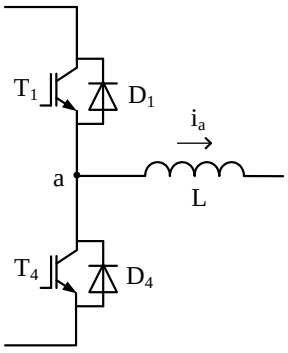
$$P_{SW} = \frac{V_{AK} f_s (t_r + t_{rr}) I_{on}}{2} \tag{5.6}$$

Total power loss,

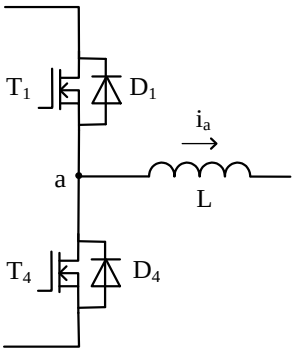
$$P = P_{cond} + P_{SW} = (V_f I_{on} + V_{off} I_{rev}) + \frac{V_{AK} f_s (t_r + t_{rr}) I_{on}}{2} \approx \frac{V_{AK} f_s (t_r + t_{rr}) I_{on}}{2} \tag{5.7}$$

5.3 Loss analysis in Si IGBT and SiC-MOSFET

Three-phase voltage source inverter have considered for the analysis of losses. Three-phase inverter has three legs and each leg has two switches. Each switch consists of one transistor and one anti-parallel diode. All the switches of inverter are controlled by the space vector modulation (SVM) technique. The loss model has been developed for the estimation of losses for the one period of SVM for one leg of the inverter. Fig. 5.4 shows the one leg of three-phase inverter with Si IGBT and SiC MOSFET. Firstly, the losses have been estimated for the inverter using IGBTs as switching devices in first case while in second case SiC MOSFETs are used as switching devices.



(a) Si IGBTs



(b) SiC MOSFETs

Fig. 5.4 One leg of three phase inverter with

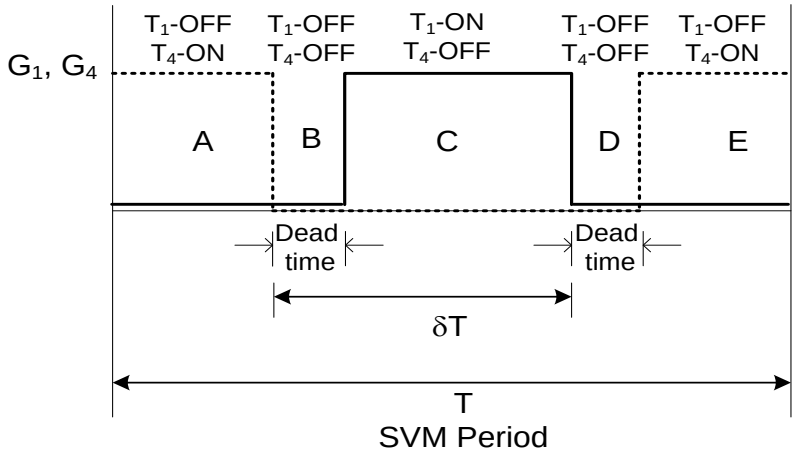


Fig. 5.5 SVM period conduction intervals

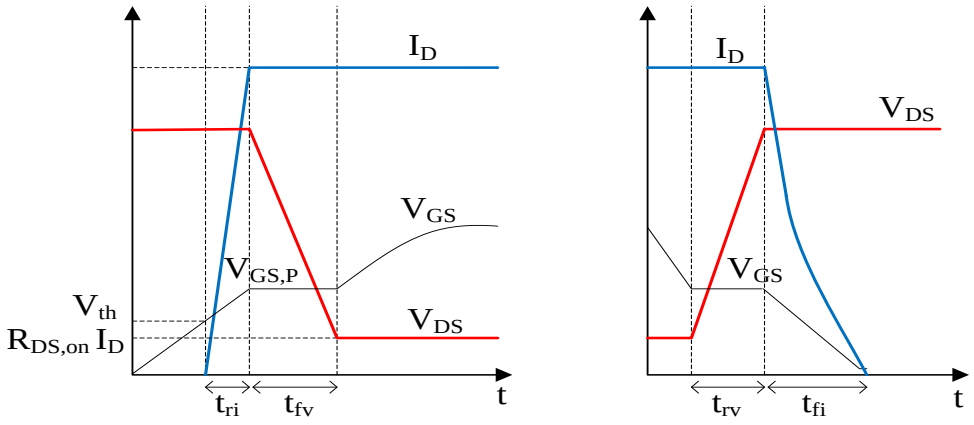
The SVM period is divided into five time intervals, each of them distinguishable for the combination of the gate signals G_1 and G_4 applied to the power transistors T_1 and T_4, respectively. Fig. 5.5 illustrates the five intervals, labeled with capital letters A to E, and plots the signal G_1 with continuous line and the signal G_4 with dashed line. When the gate signal is high, it turns on the respective power transistor. Within the intervals *B* and *D* both the gate signals are kept low to insert a dead-time that prevents the leg short-circuit during the commutations. The device actually conducting the phase current depends on the direction of the current as well as on the type of power transistor since the Si IGBTs are unidirectional while the SiC MOSFETs are bidirectional. The conducting devices are reported in Table 5.1. Note that a SiC MOSFET and its parallel diode can be both in conduction when the diode threshold voltage and the drain-source voltage of the SiC MOSFET are nearly equal.

5.3.1 Commutation process

Owing to the diode connected in parallel to the power transistors, the losses during the commutations depend on the direction of the motor phase current. For example, let the

Table 5.1: Conducting devices

Current	**Device**	**Conduction interval**				
		A	**B**	**C**	**D**	**E**
$i_a>0$	Si IGBT	D_4	D_4	T_1	D_4	D_4
	SiC MOSFET	T_4	D_4	T_1	D_4	T_4
$i_a<0$	Si IGBT	T_4	D_1	D_1	D_1	T_4
	SiC MOSFET	T_4	D_1	T_1	D_1	T_4



(a) Turn-on transients (b) Turn-off transients

Fig. 5.6 Hard-switching of a SiC MOSFET

current of the phase a be positive. For a Si IGBT, at the transition from *A* to *B* the turning off of T_4 is a soft- switching commutation at zero current because, before the transition, the current was flowing through D_4. Instead, for a SiC MOSFET the turning off of T_4 does not occur at zero current since the current was flowing through it. However, since the current during the commutation is taken by D_4, the voltage across T_4 is clamped by the threshold voltage of D_4 so that the turning-off losses of T_4 are quite small. On the contrary, during the transition from B to C, the turning-on of T_1, whether it is a Si IGBT or a SiC MOSFET, is a hard-switching commutation because it occurs when the voltage across T_1 is equal to V_d; consequently, the power losses are significant for both a Si IGBT and a SiC MOSFET.

The hard-switching turn-on and turn-off characteristics of a SiC MOSFET are shown in Figs. 5.6(a) and (b) respectively, where V_{th} is the gate-source threshold voltage. The blue trace refers to the drain current I_D, the red one to the drain-source voltage V_{DS} and the thin black line to the gate-source voltage V_{GS}. Turn-off characteristics of a Si IGBT are similar.

In both SiC MOSFETs and Si IGBTs, the turn-on switching losses take place during the current rising time t_{ri} and the voltage falling time t_{fv}; instead, the turn-off switching losses take place during the voltage rising time t_{rv} and the current falling time t_{fi}. Data sheets of the power transistors usually report t_{ri} and t_{fi} whilst t_{fv} and t_{rv} must be derived from the parameters of the devices. Application notes [14] and [15] report a procedure for deriving an approximated value of t_{fv} and t_{rv} and a confidence value of the switching losses. The procedure for a SiC MOSFET, slightly modified with respect to [14] and [15] to get a more accurate modeling, is hereafter illustrated; that one for a Si IGBT differs only in the calculation of the on-state losses.

5.3.2 Voltage transient time derivation

In both turning-on and turning-off of a SiC MOSFET, the rate of change of V_{DS} depends on the gate-drain capacitance C_{GD} that, in turn, is a function of the voltage V_{DS}. To derive t_{fv}

the waveform of the falling voltage is shaped with a four straight-line segments; the segment i with i=1, 2, 3, 4 is applicable to the fall of the voltage V_{DS} from V_i to V_{i+1}, being $V_1=V_d$ and $V_5=R_{DS,on}I_D$, where $R_{DS,on}$ is the drain-source on-resistance of the SiC MOSFET. Segment extremes V_2, V_3 and V_4 are chosen by a try and check procedure aimed at minimizing the difference between the switching losses obtained from the model and those measured in the operating condition reported in the SiC MOSFET data sheet. The segments have a time length that can be approximated as

$$t_{fv,i} \cong (V_i - V_{i+1}) R_G \frac{C_{GD,i}}{(V_{GS,d} - V_{GS,P})} \tag{5.8}$$

where R_G is the gate resistance, comprehensive of both the internal and the external resistances, $V_{GS,d}$ is the gate driving voltage applied to the external gate resistance, if any, or to the gate terminal of the SiC MOSFET, and $V_{GS,P}$ is a constant gate voltage, termed plateau voltage, that appears downstream the gate resistance while V_{DS} is decreasing and the Miller effect occurs. $C_{GD,i}$ is the gate-drain capacitance relevant to a voltage of V_{DS} equal to V_i.

By (5.8), t_{fv} is

$$t_{fv} = t_{fv,1} + t_{fv,2} + t_{fv,3} + t_{fv,4} \tag{5.9}$$

Equations like (5.8) and (5.9) can be used to find t_{rv}.

$$t_{rv,i} \cong (V_i - V_{i+1}) R_G \frac{C_{GD,i}}{V_{GS,P}} \tag{5.10}$$

Therefore, voltage rise time can be given by,

$$t_{rv} = t_{rv,1} + t_{rv,2} + t_{rv,3} + t_{rv,4} \tag{5.11}$$

5.3.3 Loss modeling

The SiC MOSFET turn-on losses are expressed as

$$E_{t-on,I_D} = \frac{1}{2}(t_{ri} + t_{fv}) V_d I_D \tag{5.12}$$

When the SiC MOSFET is turned on, the diode in parallel to the other SiC MOSFET of the same leg turns off and its junction capacitance discharges originating the reverse recovery current I_{rr} and the associated losses. The current I_{rr} flows for a time interval denoted as trr and adds to I_D. The waveform of the current I_{rr} is approximately triangular, with a peak value of

$$I_{rr,pk} = \frac{2Q_{rr}}{t_{rr}} \tag{5.13}$$

being Q_{rr} the charge stored in the diode junction. The corresponding losses in the SiC MOSFET are expressed as

$$E_{t-on,I_{rr}} = Q_{rr} V_d \tag{5.14}$$

whilst in the diode they are expressed as

$$E_{t-on,D} = \frac{1}{4} Q_{rr} V_d \tag{5.15}$$

Note that the quantity Q_{rr} and, as a consequence the loss terms in (5.14) and (5.15), is nearly proportional to the actual value of I_D.

The SiC MOSFET turn-off losses are expressed as

$$E_{t-off} = \frac{1}{2}(t_{rv} + t_{fi})V_d I_D \tag{5.16}$$

The corresponding losses of the diode in parallel to the other SiC MOSFET can be neglected.

The driving losses for turning on and off a SiC MOSFET are expressed as

$$E_{drv} = 2V_{GS,d}Q_{GS} \tag{5.17}$$

where Q_{GS} is the gate-source charge. The driving losses are usually much smaller than $E_{t\text{-}off}$ and $E_{t\text{-}on}$ and then can be also neglected.

Conduction losses can be expressed as in (5.18) and (5.19) by modeling the conducting SiC MOSFET with $R_{DS,on}$ and the conducting diode with the series of the resistance R_D and the forward voltage drop V_D.

$$E_{cnd,M} = R_{DS,on}I_D^2 T_{on} \tag{5.18}$$

$$E_{cnd,D} = (R_D I_D + V_D)I_D T_{on,D} \tag{5.19}$$

In (5.18) and (5.19), T_{on} and $T_{on,D}$ are the time intervals during which respectively the SiC MOSFET and the diode are conducting. The duration of the intervals is related to the duty-cycle and the dead-time of the gate signals.

Equal expressions, apart from (5.18), hold for the losses of a Si IGBT, provided that the drain-source quantities are substituted for by the collector-emitter quantities. Eq. (5.18) must be modified as follows to take into account the voltage drop $V_{CE,0}$ between collector and emitter when the collector current is zero:

$$E_{cnd,I} = \left(R_{CE,on}I_D + V_{CE,0}\right)I_D T_{on} \tag{5.20}$$

where $R_{CE,on}$ is the on-resistance of the Si IGBT.

The total energy losses of an inverter leg during a SVM period are the sum of the various contributions found above and are formulated in

$$E_{loss} = E_{t-on} + E_{t-on,D} + E_{t-off} + E_{cnd} + E_{cnd,D} \tag{5.21}$$

where $E_{t\text{-}on}$ are the total turning-on losses given by

$$E_{t-on} = E_{t-on,I_D} + E_{t-on,I_{rr}} \tag{5.22}$$

The loss model explained here is implemented to calculate the inverter loss. The losses of the inverter during a supply period are simply calculated by multiply the losses of a leg by three. The comparative study between two versions of inverters built with Si-IGBT devices and other one built with the same rating of SiC- MOSFET devices have been discussed in chapter 6.

5.4 Analysis of Losses for Body Diode of GaN Transistor

GaN transistor's integral diode is similar to the reverse diode in a silicon power MOSFET. However, only minority carriers are used in GaN device conduction so there is zero reverse recovery. The forward voltage of the internal diode is equal to $V_{GS(TH)}$. There are at least two ways to reduce the losses in the body diode. The most advantageous is to use a near zero dead time. If this is not practical, a Schottky diode can be used to eliminate the high forward voltage during high side turn off, and reduce it after low side turn off. A comparison of efficiencies of a DC-DC converter [16] with and without a (1 A, 100 V) Schottky diode are evaluated and observed that the loss of efficiency is very small, for this small diode and hence it is neglected. Therefore, we can conclude that the use of a Schottky diode is optional and will depend on efficiency requirements and cost.

5.5 Loss Comparison between Si-MOSFET and GaN Based Transistor

The comparison of losses between Si-MOSFET and GaN Transistor, which is also called GaN-based hetero junction field-effect transistors (GaN-HFETs) [17]-[19]. The loss calculation of above said devices have been discussed and compared by A. Nakajima et al [20]. However, a higher switching frequency causes a larger switching loss in general. To minimize the losses with increasing frequency, the wide band-gap semiconductor devices i.e. gallium nitride-based hetero junction field-effect transistors (GaN-HFETs) are promising candidates as semiconductor for the power converters. GaN has the high electric field strength over 3 MV/cm, which is ten times larger than that of the Si and high-electron mobility more than 1400 cm^2/V-s by utilizing the unique polarization properties. Table 5.2 shows the characteristics and gate-drive conditions for the considered devices i.e. GaN-HFETs and Si-MOSFET.

Table 5.2: Characteristics and gate –drive conditions for evaluated devices

Device	**Breakdown Voltage(V)**	**R_{on}(Ω)**	**$V_{GS(th)}$ (V)**	**Gate drive**	
				V_{gh}(V)	**V_{gl}(V)**
GaN-HFET	180	0.2	-2	0	-3
Si-MOSFET	200	0.3	+1.6	+5	0

Fig. 5.7 shows the characteristics of gate drain capacitance versus Drain- Source voltage V_{DS} of a GaN-HFET. The inserted fig. shows a comparison of measured capacitance values of a GaN-HFET and a Si-MOSFET in dc bias conditions. We can observe that graph for GaN-HFET has very low value as compared to Si-MOSFET.

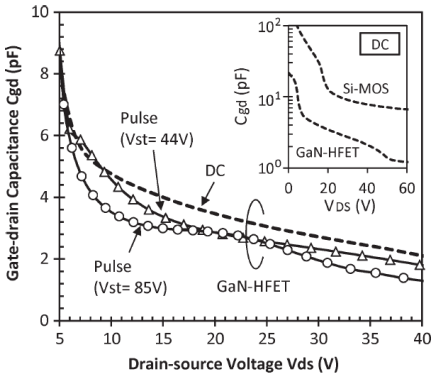


Fig. 5.7 Gate–drain capacitance values of a GaN-HFET. The inserted figure shows a comparison of measured capacitance values of a GaN-HFET and a Si-MOSFET in dc bias conditions

The Fig.5.8 shows the equivalent circuit diagram of a chopper [20], with key parasitic parameters; an equivalent resistance R_{s1} and inductance L_{s1} of the input decoupling capacitor, stray inductances (L_{s2}, L_{s3} and L_{s4}) of the circuit board and semiconductor device packages, a stray capacitance C_{s1} of the free-wheeling diode, stray capacitance values (C_{s2}, C_{s3}, and C_{s4}) of the main switch, and an internal resistance R_{s2} of the gate driver.

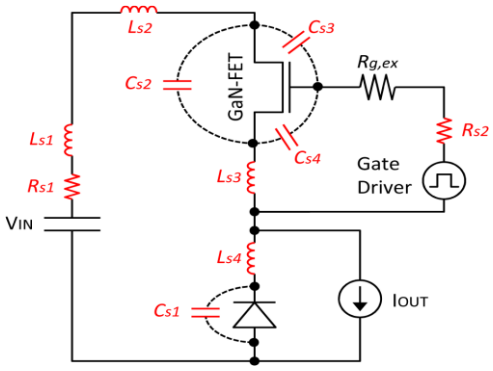


Fig. 5.8 Equivalent circuit of a dc–dc converter (chopper) with key stray parameters

For the loss calculation of GaN-HFET, it is very necessary to analyze the behavior of turn-on and turn–off characteristics. Fig. 5.9 shows the turn-on and turn-off waveforms of GaN-HFET. The total circuit loss P_{total} is given by a sum of conduction losses and switching losses i.e.,

$$\left.\begin{aligned} P_{total} &= P_{switch} + P_{diode} + P_{stray} \\ P_{switch} &= P_{sw,cond} + f(E_{on} + E_{off} + E_{gate}) \end{aligned}\right\} \tag{5.23}$$

where $P_{sw,cond}$, P_{diode}, and P_{stray} are conduction loss of the main switch, the losses in diode and the losses due to parasitic resistances, respectively; f is the switching frequency; and E_{on}, E_{off}, and E_{gate} are the turn-on energy, the turn-off energy, and the gate-drive energy of the main switch, respectively. The losses $P_{sw,cond}$, P_{diode}, and P_{stray} can be directly calculated from

the resistances and the output current I_{OUT} by the Ohm's law. As illustrated in Fig. 5.9(a), the E_{on} is divided into two parts given by

$$E_{on} = E_{on\text{-}t} + E_{on\text{-}r} \tag{5. 24}$$

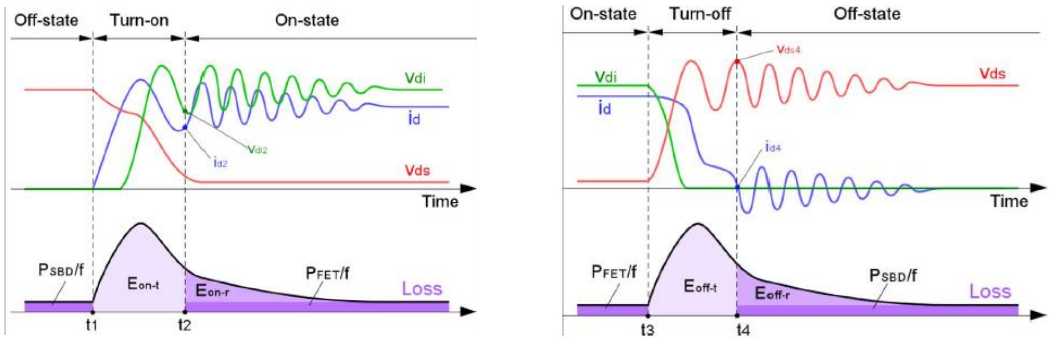
and $E_{on\text{-}t}$ is a time-dependent turn-on energy during $t = t_1$ to t_2, and $E_{on\text{-}r}$ is a residual resonance energy after $t = t_2$. From the calculated waveforms, the $E_{on\text{-}t}$ can be calculated as

$$E_{on\text{-}t} = \int_{t_1}^{t_2} i_d(t) v_{ds}(t) dt \tag{5. 25}$$

The $E_{on\text{-}r}$ is the residual energy excessively absorbed by the diode capacitance C_{di} and the stray parameters C_{s1} and L_s. It can be calculated by

$$E_{on\text{-}r} = \int_{V_{di2}}^{V_{IN}} (C_{di} + C_{s1})(V_{IN} - V_{di}) dV_{di} + \frac{1}{2} L_s (I_{out} - I_{d2})^2 \tag{5. 26}$$

where V_{di2} and I_{d2} are a diode voltage and a drain current at $t=t_2$.



(a) Turn-on periods (b) Turn-off periods

Fig. 5.9 Schematic switching waveforms of drain current i_d, drain–source voltage v_{ds}, and diode voltage v_{di} for different periods

Similarly, the turn-off energy can be calculated as

$$E_{off} = E_{off\text{-}t} + E_{off\text{-}r} \tag{5. 27}$$

where $E_{off\text{-}t}$ is the time-dependent turn-off energy, and $E_{off\text{-}r}$ is the residual resonance energy. They are given by

$$E_{off\text{-}t} = \int_{t3}^{t_4} i_d(t) v_{ds}(t) dt \tag{5. 28}$$

$$E_{off\text{-}r} = \int_{V_{ds4}}^{V_{IN}} (C_{oss} + C_{s2} + C_{s3}) V_{IN} dV_{ds} + \frac{1}{2} L_s I_{d_4}^2 \tag{5.29}$$

where V_{ds4} and I_{d4} are a drain voltage and a drain current at $t = t_4$. Finally, the gate loss can be calculated as

$$E_{gate} = \left|V_{gh} - V_{gl}\right| Q_{gate} \tag{5.30}$$

Q_{gate} is the gate charge, and V_{gh} and V_{gl} are the ON state and the OFF-state output voltages of the gate driver respectively.

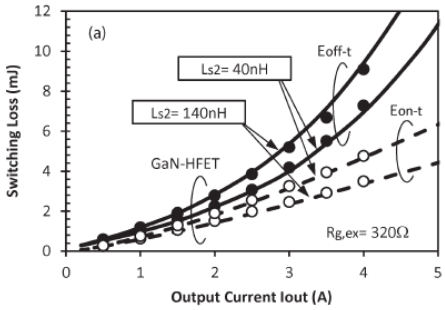


Fig. 5.10(a) Measured (Plots) and simulated (lines) switching losses of GaN-HFETs with the changing output current values

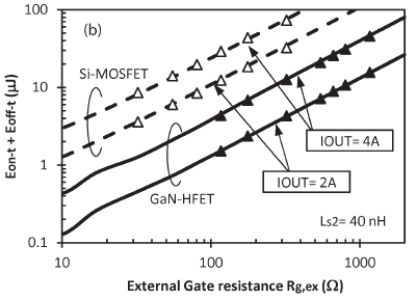


Fig. 5.10(b) Switching loss comparison between a GaN-HFET and a Si-MOSFET

Finally, the calculated results of GaN-HFET have been compared with Si-MOSFET and plotted in Fig. 5.10. Therefore, it is clear that the losses in GaN-HFET is very less as compared to Si-MOSFET.

5.6 Summary

The analysis of various losses in power devices are analyzed in this chapter. A general layout of loss structure and types of significant losses that play important roles in designing the power converters are discussed. The loss model of both types of power losses (i.e. static power loss and dynamic power loss) of diode, IGBT, and MOSFET are illustrated. In the static power loss, mainly conduction loss are investigated while in the dynamic power loss; turn-on and turn-off together with reverse recovery losses are accounted for the power devices based on conventional and WBG semiconductor materials. Finally, the comparative analysis of losses in Si, SiC, and GaN devices is expounded in details with considering the various applications.

Chapter 6

Efficiency Enhancement of a Traction Inverter by SiC MOSFETs

6.1 Introduction

In a time where awareness is growing for environment protection and energy conservation, the battery-powered electric vehicles (EVs) represent an effective solution against environmental pollution and energy consumption [21]. Regarding the environmental pollution, EVs provide local emission-free transportation. Even if one ponders the gases released in the atmosphere from the power plants generating the energy needed to recharge the battery pack of the EVs, the emissions of CO_2 are substantially reduced whilst the emissions of the other pollutants are greatly mitigated. Furthermore, the EVs offer the possibility of exploiting several kinds of renewable energies that are both amiable for the environment and effective for the energy conservation. In spite of the positive effects on environment and energy, the EV proliferation is handicapped by two main shortcomings, namely the limited driving range and the high cost of the vehicles, both of them associated to the currently available batteries [22].

An EV is equipped with a number of power converters. The role of the power converters is crucial in achieving an efficient use of the energy since almost all the energy consumed in an EV passes through them. Undoubtedly, the overwhelming majority of energy flows through the inverter that supplies the traction motor. Therefore, the efficiency of the traction inverter determines the global efficiency of an EV and, hence, the range achievable with the energy stored on-board the EV [23].

The power wasted by a power converter is due to the conduction and switching losses, which depend on the output power and the switching frequency. Several techniques have been developed to enhance the efficiency of the conventional power converters and research on this topic is still going on [24], [25]. Until few years ago, the efficiency of the power converters was increased in two ways: by improving the characteristics of the power devices with proper industry processes and by setting up circuital topologies, such as the resonant ones, able to commutate the power devices at zero voltage or current.

In this chapter, the analysis is devoted for a compact-class electric car and compares the losses as well as efficiency of its traction inverter, built up with Si IGBTs, to that of a traction inverter having the same ratings but built up with SiC MOSFETs [26]. For the comparison purposes, the standard New European Driving Cycle (NEDC) is selected. Moreover, the current and voltage profiles required by the traction motor for the electric car to track speed

and acceleration profiles of the NEDC have been analyzed. Total losses of the traction inverter along the NEDC for both the Si IGBT inverter and a SiC MOSFET inverter have been found out by utilizing the developed model for the comparison of losses as well as efficiency.

6.2 Case Study

6.2.1 Electric car

The electric vehicle considered as a study case is a compact-class hatchback electric car. The type of inverter used for the traction purposes is a voltage source inverter (VSI). VSIs are commonly used to convert active power from a DC power source to an AC load, such as an AC motor. Usually, the DC source voltage is nearly constant and the amplitude of the AC output voltage is controlled by adjusting the PWM ratio of the VSI. VSIs are also becoming widely adopted for other applications, such as grid connection for renewable energy sources, where a DC power source supplies power to an AC system with a constant frequency.

To drive the traction inverter a DC power source is required. For the study case, a lithium-ion battery pack is used for the inverter supply. The battery pack is made of two sub-packs connected in series, each of them arranged with 96 cells connected in parallel. Nominal voltage and capacity of the battery pack are 365 V and 66 A h, respectively. For the propulsion system, permanent magnet (PM) synchronous motor is used. PM motor is almost exclusively utilized in demanding applications for controlled drives because of high control performance. Indeed, if controlled with the field-oriented (FOC) technique (also referred to as vector techniques) , a PM synchronous motor has the same characteristics as a DC motor. Nowadays PM synchronous motor are use also in applications where efficiency is concerned. As the efficiency is very high in full load and part load operation range, this kind of drive is economically advantageous for the EVs.

High-performance drives are characterized by smooth rotation over the entire speed range of the motor, full torque control at zero speed, fast accelerations and decelerations. To achieve such a result, the FOC technique is used for 3-phase AC motors. The basic idea of the FOC technique is to decompose a stator current into a magnetic field component and a torque component. In PM synchronous motor, magnetic field component is used to weaken the flux of the motor PM so as to increase the operating speed beyond the nominal value. The structure of the motor controller is then as simple as that for a separately excited DC motor.

6.2.2 Traction drive

The traction drive of the study case consists of a three-phase PM synchronous motor fed by a voltage source inverter (VSI). The VSI is made of six silicon IGBTs with the relevant free-wheeling diodes. The voltage rating of the IGBTs is 600V. A schematic

diagram of the traction drive is shown in Fig. 6.1, where V_d is the battery pack voltage. Each motor phase is modeled by its resistance R, synchronous inductance L and sinusoidal back emf e. Hereafter, the phase resistance is disregarded since it is has no relevance for the subsequent analysis.

According to the FOC technique, the phase currents are controlled in order to have a sinusoidal waveform (of the required magnitude) and to be in phase with the phase back emfs at low speed so as to have the maximum torque-per-ampere ratio. In these conditions the power converted from electrical to mechanical form is

$$P = \frac{3}{2}EI = \frac{3}{2}k\omega I \tag{6.1}$$

and the torque developed by the motor is

$$T = \frac{3}{2}kI \tag{6.2}$$

The peak magnitude V of the phase voltages required to supply the motor with the current I is

$$V = \sqrt{E^2 + (\omega LI)^2} = \omega\sqrt{k^2 + (LI)^2} \tag{6.2}$$

where k is the motor constant, ω is its angular speed in mechanical radians, and I and E are the peak magnitudes of the phase current and the back-emf.

Let the inverter be controlled with the Space Vector Modulation (SVM) technique. The maximum magnitude of the peak of the phase voltages is

$$V_M = \frac{V_d}{\sqrt{3}} \tag{6.4}$$

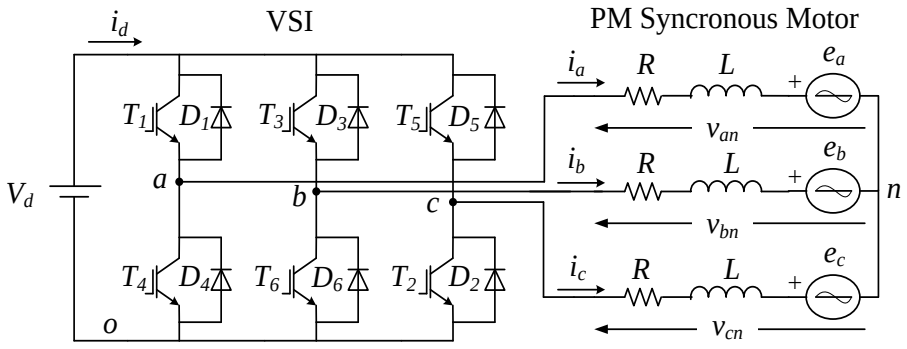


Fig. 6.1 Diagram of the traction drive

When the motor speed exceeds the nominal one, the motor is operated in the flux-weakening zone. To this end, the phase current is controlled to lead the back-emf so as to partially counterbalance the back-emf increase. Under this operation, only the current component in phase with the back-emf is effective in producing the motor torque. Consequently, the motor torque is lower than (6.2) and the drive works in the constant power region.

The main characteristics of the electric car of the case study, including those of its traction drive, are listed in Table 6.1.

Table 6.1: Case study electric car and traction drive characteristics

Parameter	Symbol	Value
Mass (with driver)	m	1550 kg
Reduced mass of wheels and motors	m_{red}	30 kg
Wheels radius	r	0.316 m
Nominal motor power	P_N	80 kW
Nominal motor torque	T_N	280 N·m
Nominal motor current	I_N	250 Arms
Motor constant	k	0.73 V·s/rad
Motor d axis inductance	L_d	3.3 mH
Motor q axis inductance	L_q	1.2 mH
Motor number of pole pairs	n_p	1
Motor efficiency	η	0.9
Battery nominal voltage	$V_{d,N}$	365 V
Range (NEDC)	R	200 km

6.3 Driving Cycle Requirements

Energy losses of the traction inverter are evaluated for the car running along the driving cycle.

A driving cycle is a fixed schedule of vehicle operation, which allows a consumption/range test to be conducted under reproducible conditions. Driving cycle is usually defined in terms of vehicle speed as function of time. A trained driver is employed to follow the driving cycle on the chassis dynamometer, and a driver's aid is provided to ensure that the driven cycle is as close as possible to the defined cycle. It is also useful to note that driving cycles may be used for a variety of purposes such as testing engine, polluting emissions or drive train durability, and may be used on attest track rather than in the laboratory.

The New European Driving Cycle (NEDC) is selected for this work. The Fig. 6.2 shows the speed profile according to NEDC. It is used in Europe for the certification of the consumption for the cars under mixed urban and extra-urban driving modes. It is clearly a highly stylized cycle with periods of constant acceleration, deceleration and speed that attempt to reproduce the real driving patterns on the road. Along the driving cycle, the car covers 10.76 km in 1180 s and reaches a maximum speed of 120 km/h.

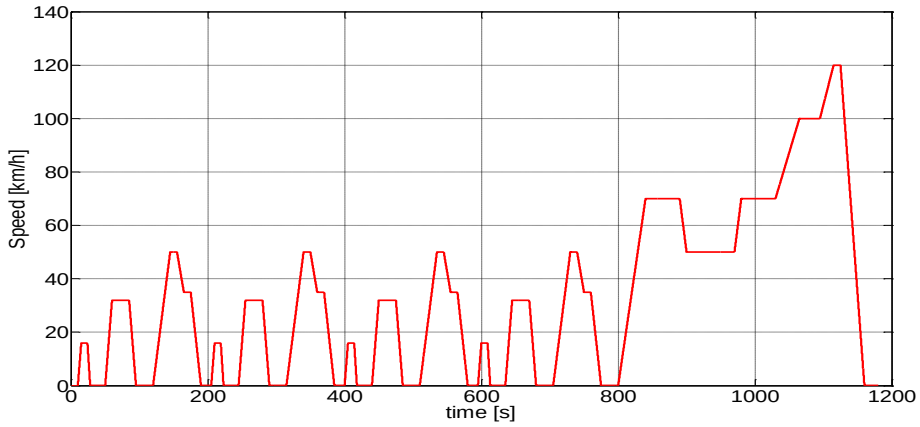


Fig. 6.2 NEDC speed profile

The force F required to propel the car along the driving cycle is calculated assuming smooth road and no wind conditions. It is expressed as

$$F = F_d + F_{roll} + am_{gen} \tag{6.5}$$

where F_d is the air drag force, F_{roll} is the rolling resistance force, a is the car acceleration and m_{gen} is the generalized mass of the car, which is equal to the sum of its gravitational mass m and of the reduced mass of its rotating elements. The air drag force is expressed as

$$F_d = \frac{1}{2} C_d \rho_{air} A_f v^2 \tag{6.6}$$

where C_d is the air drag coefficient, ρ_{air} is the air density, set at 1.167 kg/m^3, A_f is the front area of the car and v is speed of the car. The rolling resistance force is expressed as

$$F_{roll} = K_{rf} mg \tag{6.7}$$

where K_{rf} is the rolling friction coefficient and g is the gravitational acceleration. Parameters in (6.5)-(6.7) are listed in Table 6.2.

Moreover, wheel radius and gear ratio are used to go back from F and v to the torque and the angular speed of the motor along the driving cycle. The Fig. 6.3 shows the torque profile of the motor that illustrates the variation of torque with the time.

Table 6.2: Force equation parameters

Parameter	Symbol	Value
Generalized mass	m_{gen}	1580 kg
Air drag coefficient	C_d	0.28
Front area	A_f	2.23 m^2
Rolling friction coefficient	K_{rf}	0.01

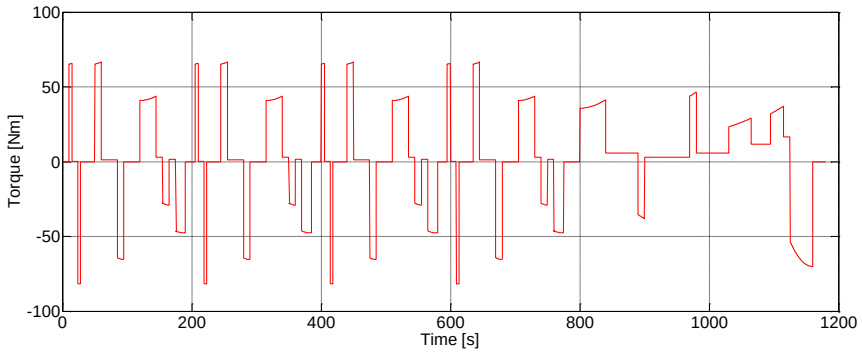


Fig. 6.3 NEDC torque profile

From Figs. 6.2 and 6.3, and using (6.1)-(6.4), requirements for the magnitude of the motor phase currents and voltages, and for their phase displacement are determined at each point of the NEDC. These data are calculated under the assumption that the motor operates in steady state at each point of the NEDC. Fig. 6.4 reports the profiles of the magnitude of current and voltage of a motor phase along the NEDC in p.u., i.e. as a fraction of the respective nominal values.

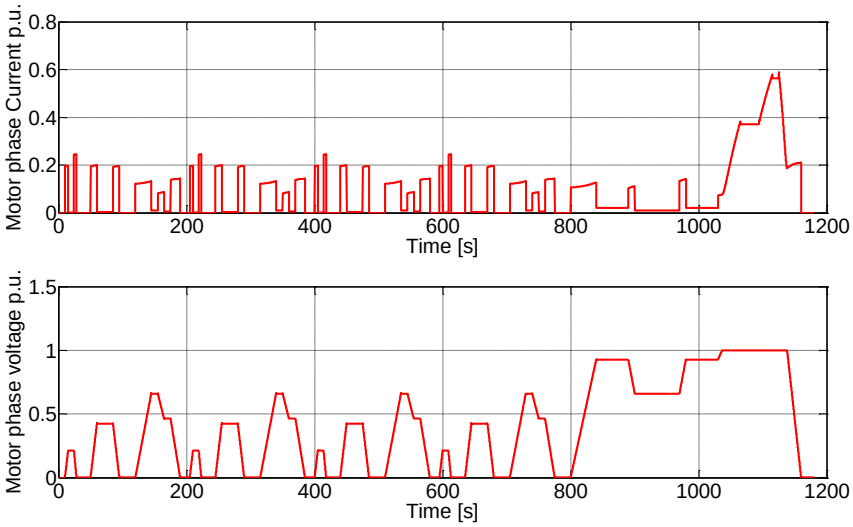


Fig. 6.4 Motor phase current and voltage along the NEDC in p.u.

Finally, the energy delivered by the inverter to the traction motor to run the car along one driving cycle is found by integrating the electrical power supplied to the motor. It has resulted in about 2 MJ.

6.4 Inverter Losses

The SVM frequency of the traction inverter is conveniently set at 20 kHz. SiC MOSFETs and Si IGBTs for the inverter are selected from commercial catalogues and have the parameters listed in Table 6.3. These two devices are chosen as per the requirements of

the current and voltage rating of the traction motor. The SiC MOSFET for the higher current ratings like hundreds of amperes are not commercially available in the market with voltage rating of 600V. Therefore, the SiC MOSFET with the voltage rating of 1200V has selected for the comparison purpose. The gate to source voltage of SiC MOSFET when switched on is 20 V because it exhibits less on-resistances only when the gate to source voltage higher than 15 volts. This unlikely Si-MOSFET and Si-IGBT which have a low on resistance with the gate to source or gate to emitter voltage ranging from 10 to 15 V. For the loss calculation of a device, it is necessary to know the voltage fall time t_{fv} and current rise time t_{ri} at the time of turn-on, and the voltage rise time t_{rv} and current fall time t_{fi} at the instant of turning-off of the device. But in the datasheet only t_{ri} and t_{fi} are reported so that it is necessary to calculate the two switching times, i.e. t_{fv} and t_{rv} , using other parameters of the devices with the help of the loss model discussed in the previous chapter. Once the time parameters are known for these devices, then it is possible to calculate the switching losses by using the voltage and current values.

Table 6.3: Si IGBT and SiC MOSFET parameters

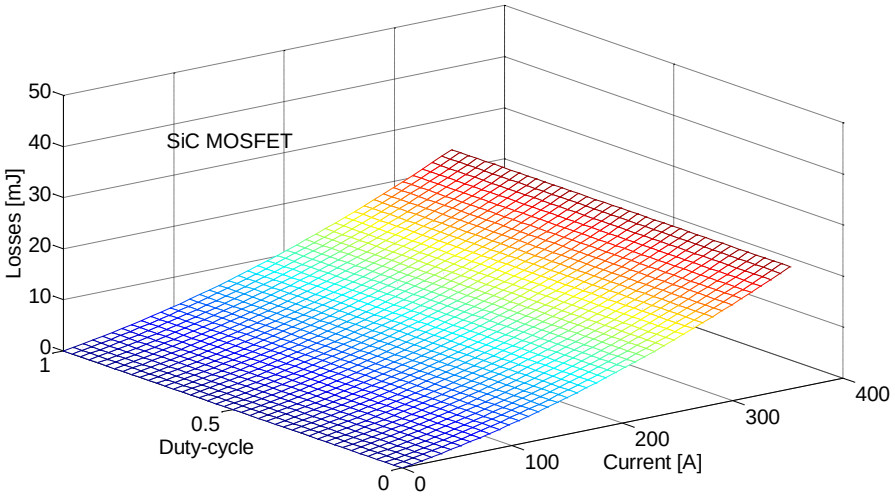
Parameters	**Si IGBT**	**SiC MOSFET**
Part Number	IXXN200N60B3H1	CAS100H12AM1
$V_{DS,max}$	600 V	1200 V
$I_{D,\ max}$	98 A @110°C	117 A @90°C
V_G	15 V	20 V
$R_{CE,on}$ - $R_{DS,on}$	5.3 mΩ	16 mΩ
$V_{CE,0}$	0.7 V	-
R_G	1.0 Ω	1.25 Ω
$V_{GS,P}$	11 V	11.5 V
t_{ri}	100 ns	76 ns
t_{fi}	110 ns	46 ns
V_D	1 V	0.9 V
R_D	8.2 mΩ	9.2 mΩ
Q_{rr}	4.7 µC	1.6 µC
t_{rr}	100 ns	47 ns

Traction motors are supplied for certain time intervals with currents as high as twice the nominal one. Going through Table 6.3, it comes out that both the Si IGBT and the SiC MOSFET, when operating at high temperature, have a rated current that is about a quarter of the nominal motor current. Therefore, each Si IGBT and SiC MOSFET of the inverter is made of eight paralleled devices. The dead-time of the commutations is fixed at 3µs for the Si IGBT legs and at 1µs for the SiC MOSFET legs.

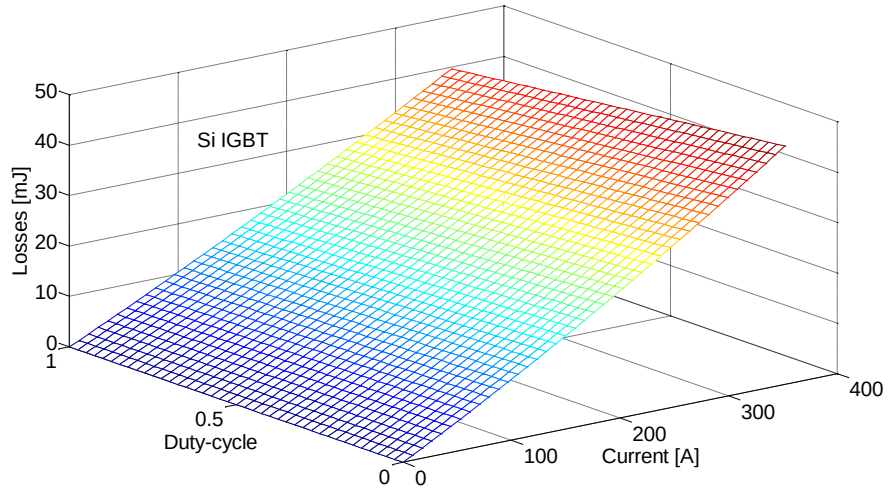
6.4.1 Loss calculation in a SVM period

The loss model of a leg and inverter is discussed in previous chapter. The energy losses of an inverter leg during one SVM period can be calculated as a function of the duty-cycle and the phase current amplitude [27]. The results are reported in Fig 6.5.(a) and (b) in the

form of 3D surfaces. The figures show that the losses of the SiC MOSFET leg are about half of its Si IGBT counterpart in all the working conditions. Regarding the dependence on the duty-cycle, the figures show that the losses of the SiC MOSFET leg are nearly independent from the duty-cycle; this is due to the fact that the diodes conduct only along the dead-times. Instead, the losses of the Si IGBT leg decreases with the duty-cycle, meaning that conduction losses are lower in the transistors than in the diodes. Regarding the dependence on the current, the figures show that the losses of the Si IGBT leg increase nearly proportionally to the current while those of the SiC MOSFET leg increase more than linearly with it; this is due to the fact that the major fraction of the conduction losses in the Si IGBTs as well in the diodes is caused by the forward voltage drop while this kind of losses are not present in the SiC MOSFETs being the conduction losses only of resistive nature.



(a) with SiC MOSFET



(b) with Si IGBT

Fig. 6.5 Inverter leg losses

6.4.2 Loss calculation in a supply period

The results found in the previous Section for the losses of an inverter leg have been implemented in an on-purpose arranged Matlab code to calculate the losses of the inverter leg during a supply period of the traction motor. The inputs to the Matlab code are the peak of the sinusoidal current flowing in a motor phase, the demanded sinusoidal voltage across the motor phase, and the phase displacement between the twos. Then, in each SVM period, from the voltage demand the duty-cycle is calculated; from the peak current and the phase displacement, the effective current is calculated. Lastly, from duty-cycle and effective current, the losses in an inverter leg are calculated. The losses calculated over all the SVM periods within the supply period are then added to obtain the losses of an inverter leg during a supply period. Finally, the total losses of the inverter (i.e. for all the three legs) during a supply period are simply calculated by multiply the losses of a leg by three.

6.4.3 Loss calculation over NEDC

The distance run along the NEDC is split into a number of segments, each of them corresponding to the space covered by the electric car while the traction motor performs one rotation. For each segment, the average car speed and acceleration are determined from the NEDC speed profile and then converted into motor phase voltage and current, by means of (6.2) and (6.3). If the motor speed is beyond the nominal value, the motor is operated in the constant power region as explained in Section 0 and the proper current value is calculated by accounting of the magnet-field component. The losses for each segment are calculated by help of a Matlab code as explained in previous section.

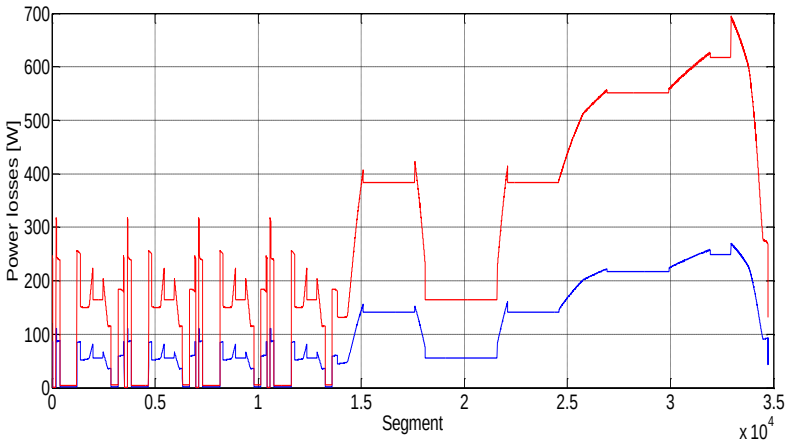


Fig. 6.6 Traction inverter power loss when based on SiC MOSFET (blue solid line) or on IGBT (red dashed line) vs. segment along NEDC

Fig. 6.6 shows the power losses along the segments of a NEDC for the two types of traction inverter: the blue solid line refers to the SiC MOSFET inverter and the red dashed line to the Si IGBT inverter.

Fig. 6.7 reports the losses cumulated along the segments of a NEDC for the two types of traction inverter: the blue solid line refers to the SiC MOSFET inverter and the red dashed line to the Si IGBT inverter. The results of Fig. 6.7 show that a SiC MOSFET inverter saves about 100 kJ per driving cycle, which is about 5% of the energy consumption. Therefore, the expected range extension ensuing from the usage of a SiC MOSFET inverter in the electric car of the case study results in about 10 km.

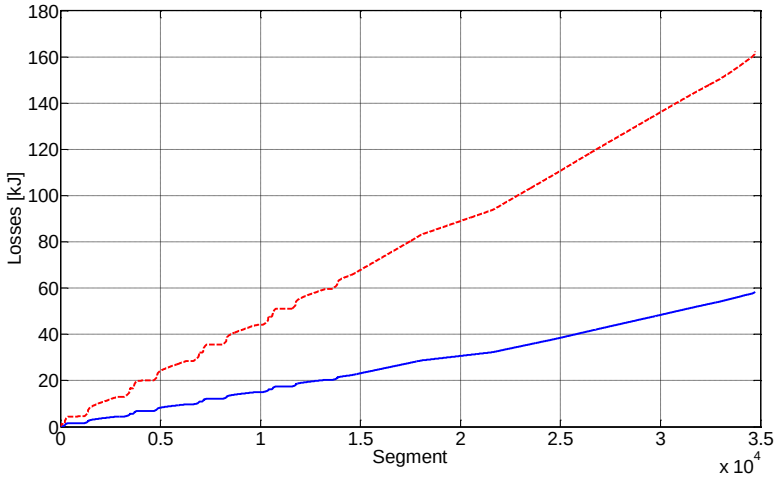


Fig. 6.7 Cumulated traction inverter losses when based on SiC MOSFET (blue solid line) or on IGBT (red dashed line) vs. segment along NEDC

6.5 Efficiency Estimation

The efficiency of the supply inverter and the propulsion motor drive system are computed using the loss formulae discussed in Loss analysis chapter for the steady state operation. Parameters of IGBTs, MOSFETs, and diodes are taken from Table 6.3 while the supply inverter DC side voltage and phase current are derived from Table 6.1. Notably, all the loss formulae are expressed in the terms of voltage and current while the efficiency maps are

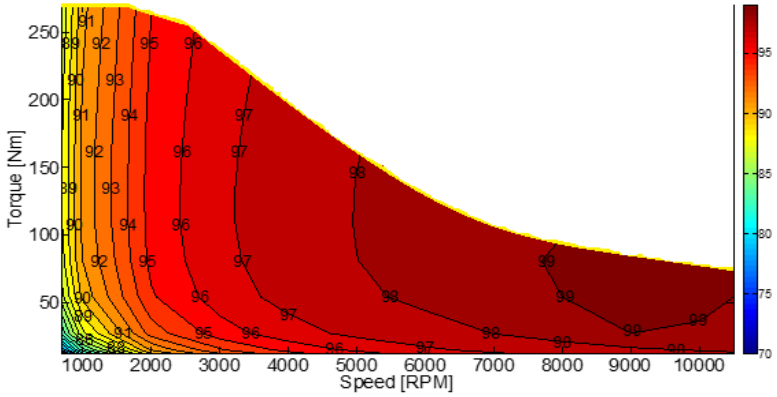


Fig. 6.8 Efficiency curve of Si- IGBT inverter

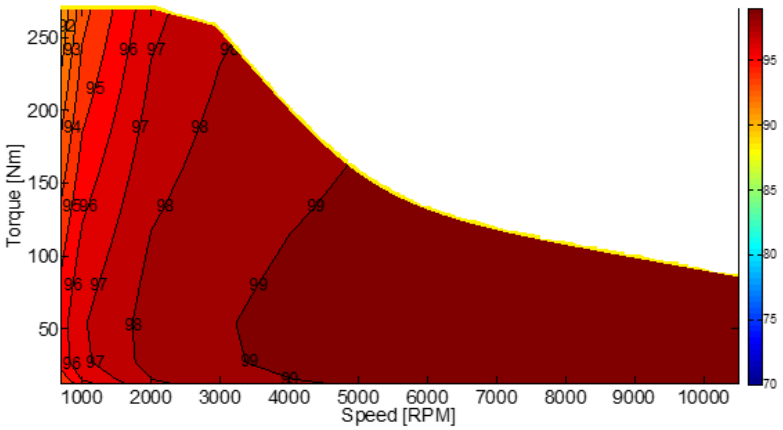


Fig. 6.9 Efficiency curve of SiC- MOSFET inverter

plotted in terms of the torque and the speed developed by the propulsion motor [28],[29]. The change in the variables has been performed by working out the voltage and current corresponding to each speed and torque pair using the motor parameters reported in Tab. 6.1 according to (6.2) and (6.3).

6.5.1 Si-IGBT inverter efficiency

The efficiency of Si-IGBT supply inverter as a function of the propulsion motor torque and speed is shown in Fig. 6.8. By inspection of the figure, inverter efficiencies exceeds 99% when operating at high speed while decreases sensibly at low speed, irrespectively from the developed torque. This is a typical behaviour because although high torque levels are produced, power levels are relatively low below 2000 rpm while switching losses are almost constant, thus decreasing the inverter efficiency.

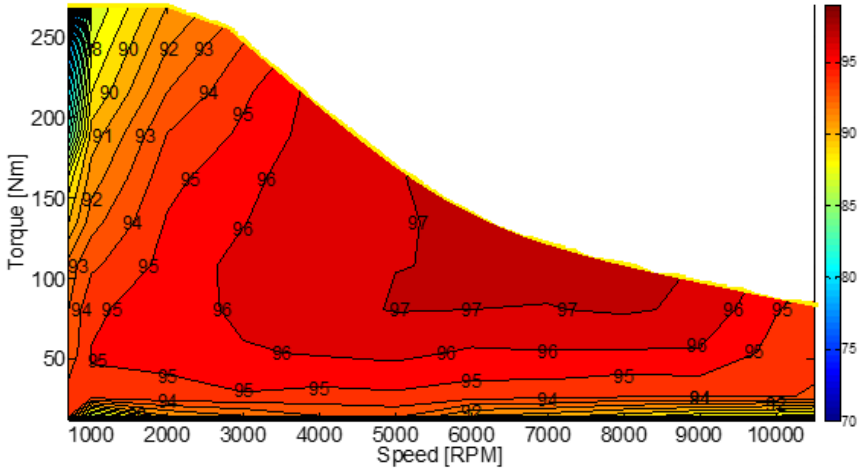


Fig. 6.10 Efficiency curve of PMSM

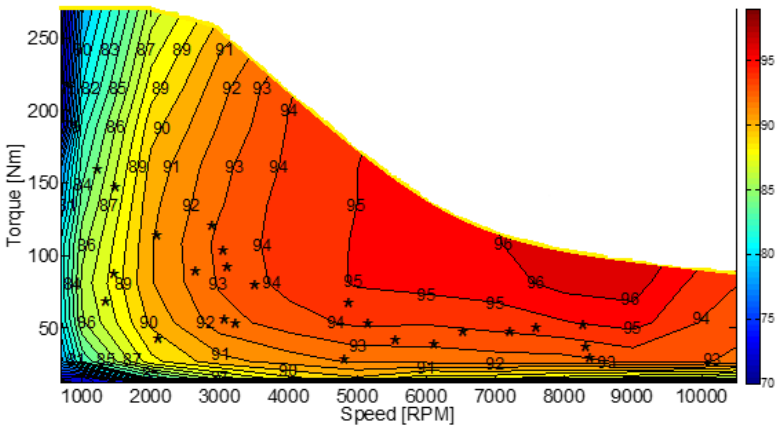


Fig. 6.11 Efficiency curve of Si-IGBT propulsion drive

6.5.2 SiC-MOSFET inverter efficiency

The efficiency of SiC MOSFET supply inverter in the same range of motor torque and speed is shown in Fig. 6.9. The maximum efficiency of the SiC MOSFET inverter exceeds 99% in the speed interval between 3200 and 10000 rpm, resulting about 2% higher than that of the Si-IGBT inverter. Also in the case of SiC-MOSFET inverter the efficiency decreases at low speed, but even in the worst case it is about 4% higher than the efficiency of the Si-IGBT inverter.

6.5.3 Propulsion drive system efficiency

The combined efficiency of the propulsion drive is computed by multiplying the motor efficiency by the inverter efficiency. The efficiency of permanent magnet synchronous motor is shown in Fig. 6.10. The propulsion drive efficiencies are calculated for both types of supply inverter.

A. Si-IGBT

The efficiency curve of the complete propulsion drive using Si-IGBT inverter is shown in Fig. 6.11. The peak efficiencies of the propulsion drive reached more than 96% between 7200 and 9500 rpm for high power levels. A large portion of map yields operational efficiencies above 90%, and drive efficiency is below 70% only for low speeds and low torques.

B. SiC-MOSFET

The efficiency map of the propulsion drive using SiC-MOSFET inverter is shown in Fig. 6.12 In this case, the peak efficiencies approached 97% around 8000 rpm for high power levels portion while decreases with lower torque and speed. For speed higher than 3000 rpm the efficiency of SiC-MSFET drive is about 1% higher than its Si-IGBT counterpart.

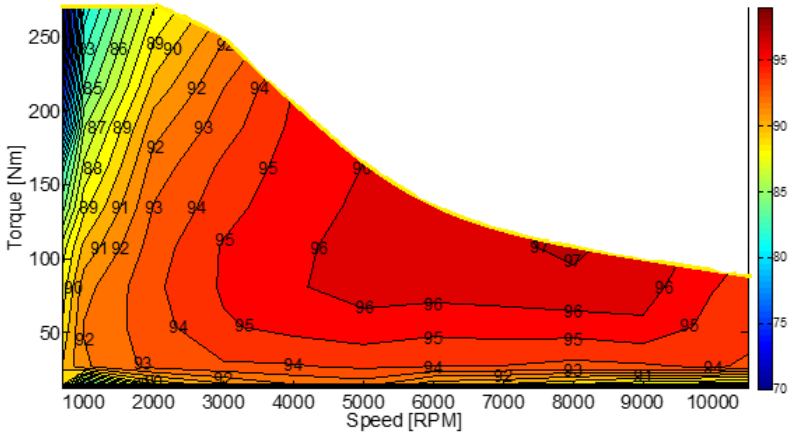


Fig. 6.12 Combined efficiency curve of SiC drive

6.5.4 Efficiency comparison of Si-IGBTs vs. SiC-MOSFETs

The difference in efficiencies between SiC-MOSFET inverter and Si-IGBT inverter is shown in Fig. 6.13. From the figure, it appears that the peak efficiency of SiC-MOSFET inverter is about 2% higher than the Si-IGBT inverter in a large region of the map; in the low speed range the advantage of the SiC-MOSFET inverter increases up to 6% and reaches 18% when very low torque and speed are considered. In the high speed and high torque region, the advantage of the SiC-MOSFET inverter reduces to 1%.

Similarly, in Fig. 6.14 the difference between the efficiency of the propulsion drive based on SiC-MOSFET and that of the Si-IGBT drive is reported. The figure shows that considering the full propulsion drive, the advantage of adopting the SiC devices is slightly reduced because of the not-ideal efficiency of the motor. In any case, SiC-MOSFET

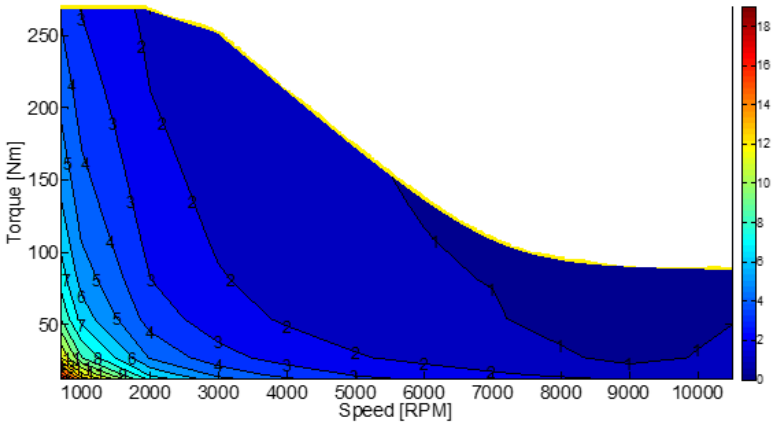


Fig. 6.13 Difference in efficiencies between SiC MOSFET-inverter and Si-IGBT inverter

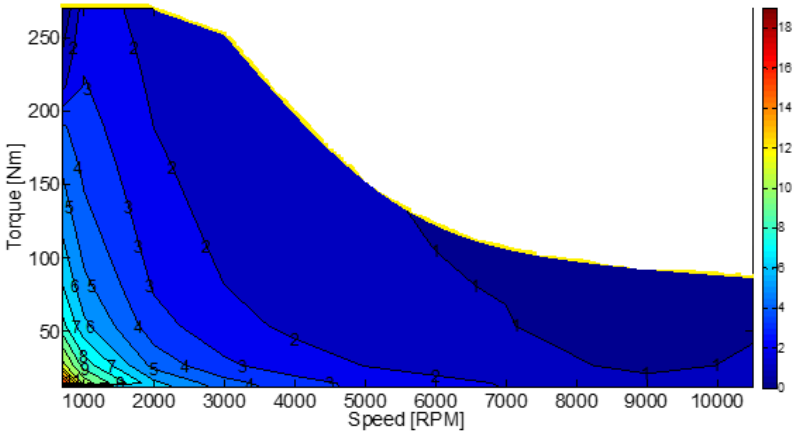


Fig. 6.14. Difference in efficiencies between SiC MOSFET propulsion drive and Si-IGBT propulsion drive

propulsion drive exhibits efficiency 2% higher of the conventional drive in large part of the operating condition and the efficiency difference is higher at low speed and torque.

6.6 Experimental Verification

The loss model developed for Si-IGBT has been validated by experimental data collected from the case study electric car. Real time data relevant to the actual vehicle speed, motor torque and speed, battery state of charge, voltage, current, and available energy and the auxiliary losses have been collected using the Advantech TREK 550 automotive PC shown in Fig. 6.15. It is connected to the car electronic diagnostic system by means of the On Board Diagnostic (OBD) port, which operates according to the SAEJ1979 document [30] and the ISO15765 standard. The details about the protocol used by manufacturer to code the different quantities are available over the internet [31]. The accuracy of the supplied data has been assessed in [32],[33], where they have been used to develop a model of the consumption and of the emissions of conventional and hybrid vehicles.

Fig. 6.15 The Advantech TREK 550 automotive PC

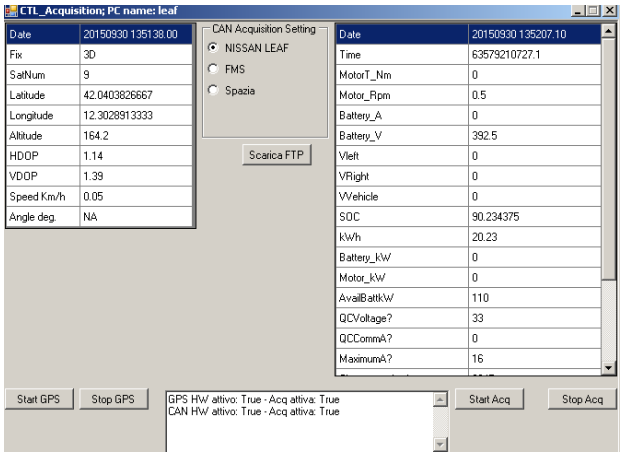


Fig. 6.16 The graphical interface

The automotive PC starts the acquisition every time the vehicle is turned on and, as soon as a Wi-Fi connection is made available, stores the acquired data together with the GPS position to a remote server. The server is equipped with a software that allows the user to inspect the saved quantities using the graphical interface shown in Fig. 6.16.

Table 6.4: Si-IGBT traction drive efficiency data

Speed (RPM)	**Torque (Nm)**	**Efficiency (Model)[%]**	**Efficiency (Experiment)[%]**
1144	154	85.25	86.63
1246	63	87.65	87.81
1376	82	88.20	88.00
1394	142	87.10	87.20
1997	108	91.10	90.42
2006	37	89.85	90.12
2549	84	92.20	91.48
2785	115	92.90	93.28
2954	98	93.20	93.31
2984	51	92.30	92.68
3020	87	93.30	93.11
3142	48	92.35	92.17
3425	74	93.75	93.63
4709	23	92.10	92.01
4786	62	94.55	94.48
5067	48	94.10	93.80
5451	36	93.20	93.05
6018	33	93.10	93.59
6436	42	93.95	94.61
7128	42	94.05	93.38
7490	45	94.20	94.35
8186	47	94.95	95.23
8232	31	93.85	93.86
8270	24	93.00	92.65

By simple elaboration of the acquired data the efficiency of the propulsion drive of the car have been computed at different torque-speed working point, highlighted with asterisks in Fig. 6.11. Some samples of the obtained results are listed in Table 6.4, together with the correspondent values mapped in Fig. 6.11 and estimated using the losses model.

Inspection of the table shows that the estimated values matches very well with the measured ones thus validating both the losses model of the Si-IGBT inverter and the efficiency map used for the motor. Losses models of the Si-IGBT and SiC-MOSFET inverters are based on the same equations so that validation relevant to Si-IGBT inverter can be extended to the other one, confirming the advantage of using SiC-MOSFETS in the propulsion drives.

6.7 Summary

In this chapter, the losses in SiC MOSFET and Si IGBT based traction inverter of a compact-class electric car have been discussed in details. Loss comparison has been carried out for the arrangement of the inverter with Si IGBTs and for its possible arrangement with the SiC MOSFETs. The complete procedure for loss calculation of inverter is explained and implemented in a Matlab code. The inverter losses have been calculated for the two inverter types when the electric car is driven along the NEDC cycle. The outcome of the calculation shows that the usage of the SiC MOSFETs reduces the losses in the traction inverter of about 5%, yielding an equal increase in the car range. The work is extended to estimate the efficiency of two versions of inverters as well their propulsion drives for the study state operation. The efficiencies of both inverters are presented through the Matlab contour plot along the speed and torque of the propulsion motor. Moreover, the efficiencies of SiC – MOSFET propulsion drive and Si –IGBT propulsion drive are calculated with the help of motor efficiency reported in literature. The efficiency of Si –IGBT propulsion drive is validated through the data collected from a commercial C-class electric car. Finally, the comparison analysis has performed between two types of inverters as well as between their combined traction drives over the entire torque and speed range. Comparison results show that the use of SiC MOSFETs improves the efficiency of the inverter as well as of the combined traction drive.

Chapter 7

Power Factor Correction

7.1 Introduction

Power factor (PF) is the ratio of real power to the apparent power. For a sinusoidal voltage source, PF is equal to the product of displacement factor (K_d) and distortion factor (K_p) of the current as shown in equation (7.1).

$$PF = \frac{V_s I_{s1}}{V_s I_s} \cos \emptyset = \left(\frac{I_{s1}}{I_s}\right) (\cos \emptyset) = K_p \times K_d \tag{7.1}$$

where

$$K_p = \frac{I_{s1}}{I_s} = \frac{1}{\sqrt{1+THD_i^2}} , \qquad K_d = \cos \emptyset , \qquad THD_i = \frac{I_{harm}}{I_{s1}} \tag{7.2}$$

The term THD_i is the total harmonic distortion of the current waveform and $\emptyset$ is the angle between the fundamental component of the current and the voltage. The current I_{s1} and I_s are shown in rms value. A front-end diode rectifier draws a current waveform, which is far from a sine wave. In addition to the demanded fundamental component, the current contains undesired harmonics at frequency higher than the fundamental frequency. This creates distortion in the voltage supply for the users (i.e. at the Point of Common Coupling) due to the line impedance. Today, the voltage supply is even more distorted due to the increased number of non-linear loads that are connected on the grid. This influences the loads as transformers and motors that are connected to the lines, which are operated under a distorted supply voltage, by increasing their losses. Therefore, power factor correction (PFC) circuits are required to improve the PF of the system [34]-[36]. There are several techniques for improvement of the PF that will be discussed in this chapter.

7.2 Basic Rectifier Circuit

The circuit diagram of a front-end diode rectifier for the DC supply of a resistive load is shown in Fig. 7.1. This rectifier circuit has four diodes connected as full bridge configuration and a capacitor connected at the output of the rectifier, which acts as a filter and reduces the ripple in the DC voltage. The resulting input current is pulsating in nature and contains several harmonics as shown in Fig. 7.2. The harmonic spectrum of the pulsating input current is shown in Fig. 7.3, and consists of the fundamental component at the supply frequency and a series of harmonics, which are multiples of the supply frequency. Since the pulsating current waveform has half-wave symmetry, the harmonic spectrum primarily consists of odd harmonics.

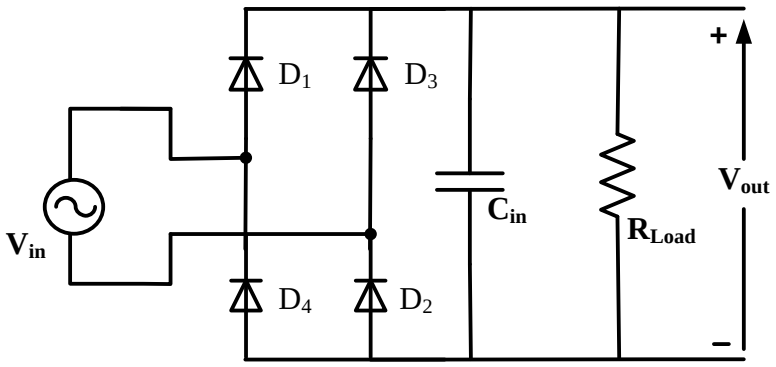


Fig. 7.1 Full wave rectifier

Therefore, as the requirements for harmonic contents have become more stringent, the front-end diode rectifier has less demand in the market. Passive PFC circuits consists in adding inductive components on the AC or DC side of the diode rectifier or more complex filter in the DC side. However, this solution is bulky and not very effective.

7.3 Active Power Factor Correction

Active PFC circuit offers better total harmonic distortion (THD), significantly smaller and lighter than a passive PFC circuit. An active PFC operates at a much higher switching frequency than the 50Hz/60Hz line frequency [37],[38].

7.3.1 Basic Boost PFC configuration

The boost converter-based PFC is the most popular and widely used PFC configuration. This configuration provides the widest conduction angle for the input current and enables design of PFC circuits that can achieve a PF close to 1.

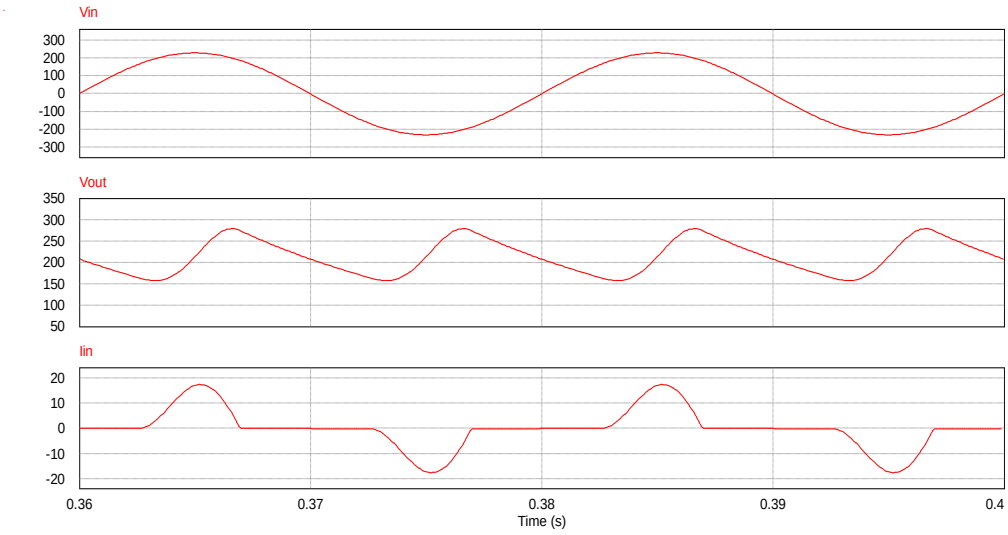


Fig. 7.2 Waveforms of basic rectifier circuit

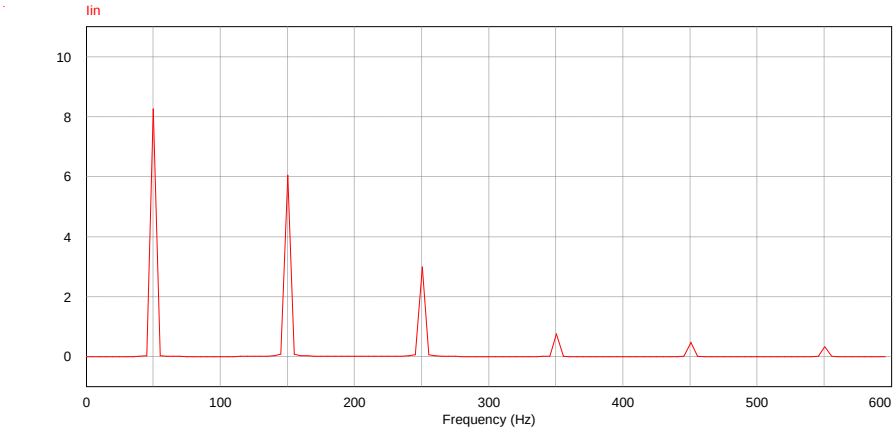


Fig. 7.3 Harmonic spectrum of input current in Full wave rectifier circuit

The basic circuit diagram of a boost PFC is shown in Fig. 7.4 [39]-[41]. This circuit requires a diode rectifier circuit, one inductor, a diode, a filter capacitor and a switching element typically a MOSFET. The output voltage of boost converter is higher than the input. Typically, boost PFC is designed such that the regulated output voltage of the converter is higher than the peak of the highest input voltage. This allows the boost PFC circuit to shape the input current waveform similar as the input voltage waveform for most of the operating input voltage range. When the MOSFET is turned ON, the energy delivered by the voltage source is stored in the inductor and the energy required by the load is supplied by the output capacitor. When the MOSFET is turned OFF, the diode D becomes forward biased and the inductor stored energy is transferred to the output capacitor and load as shown in the Fig. 7.5.

The duty-cycle of the MOSFET operation is determined by the need of shaping the input current in a sinusoidal way [42],[43]. The MOSFET is operated at high switching frequency

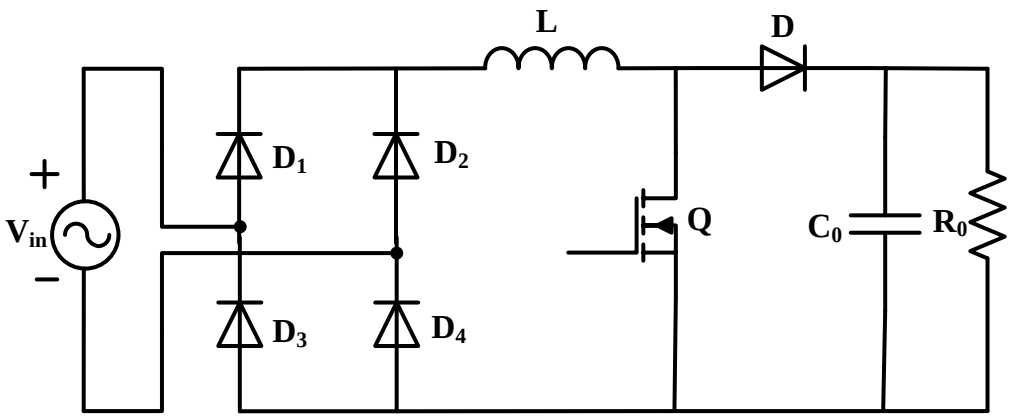
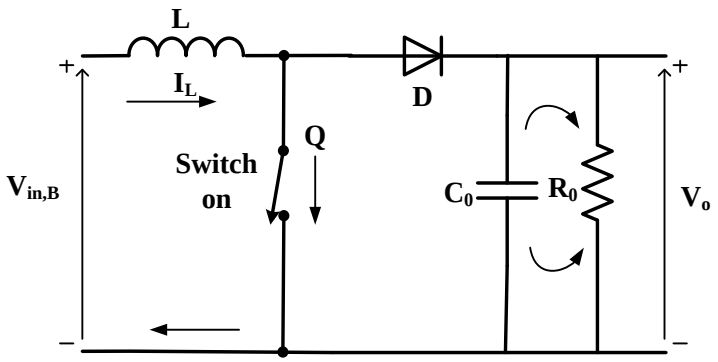
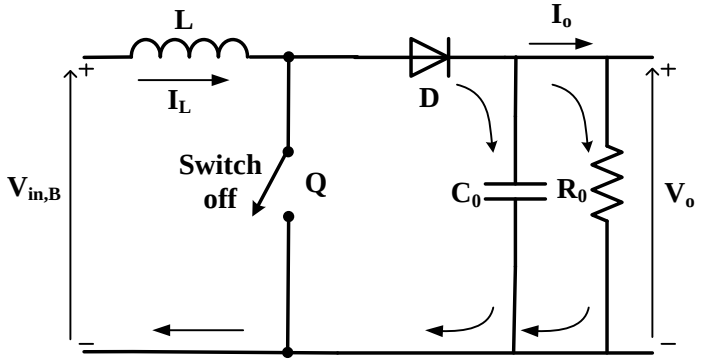


Fig. 7.4 Circuit diagram of basic Boost PFC



(a)



(b)

Fig. 7.5 Boost converter current flow when (a) switch is on and (b) switch is off

to reduce the size of inductor. A low switching frequency results in lower switching losses, EMI and in an increased inductor size.

Typically, the control system of a boost PFC has two loops i.e. (a) an inner current loop that has a high bandwidth and (b) an outer voltage loop that has a lower bandwidth. The higher bandwidth of the inner current control loop ensures that the current waveform responds to line voltage changes rapidly thereby maintaining control over the shape of the current waveform [39],[40]. The slow outer voltage loop ensures that the output voltage is constant. Because of its lower bandwidth, the outer loop does not interfere with the operation of the inner current control loop. The slow outer voltage loop may result in overshoot of the output voltage during fast load transients and often requires additional circuitry or functional blocks inside the voltage controller to limit any overshoot of the output voltage.

There are three existing modes of operation i.e. (a) discontinuous conduction mode (DCM), (b) continuous conduction mode (CCM), and (c) critical conduction mode (CRM). When all the energy stored in the inductor in each switching cycle is completely transferred

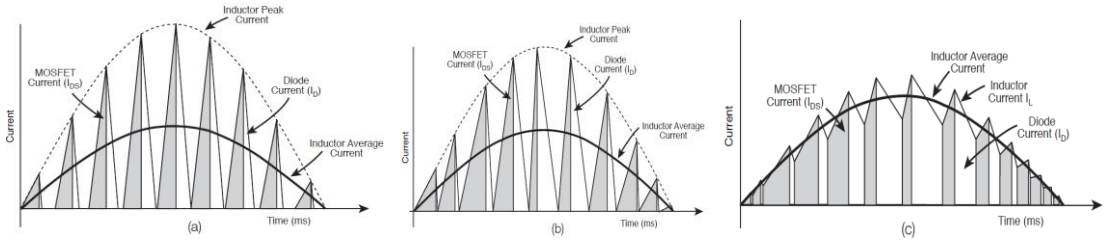


Fig. 7.6 Three modes of operation (a) DCM (b) CRM and (C) CCM

during the turned OFF period of MOSFET, the current through the MOSFET at the start of the next ON interval is zero and the circuit operates in DCM. If the stored energy in the inductor is not completely transferred to the output and there is residual energy in the inductor at start of the ON interval of the MOSFET, the current through the MOSFET starts from a non-zero value and the circuit operates in CCM. In CRM mode, the circuit operates by turning ON the MOSFET exactly at the time when all the energy stored in the inductor is transferred to the output and the inductor has no residual energy. The waveforms of all the conduction modes are shown in Fig. 7.6.

Operation in DCM results in high peak current in the MOSFET which leads to higher switching and conduction losses in MOSFET. The high peak to peak ripple current in the inductor also results in higher hysteresis loss in the inductor. Operation in CRM also has the same disadvantages as the DCM operation but it reduces EMI. Operation in CCM results in a low inductor ripple current which results in lower inductor losses. It also results in lower conducted EMI. Since the peak currents are lower than the CRM or DCM operation, MOSFET and diode conduction losses are lower in CCM mode. The only inconvenience is the peak current in the MOSFET at its turn on, due to the charge stored in the conducting diode.

Therefore, the CCM mode of operation is the preferred choice for a wide range of power for PFC applications because of the availability of ultrafast recovery diodes that have soft recovery characteristics, which is the main requirement of boost converter to work in CCM mode.

7.3.2 Commutation losses

CCM mode of operation is assumed, with the line current in phase with the input line voltage and having a sinusoidal waveform with a superimposed switching ripple.

The converter MOSFET duty cycle is denoted as δ_m and the diode duty cycle is denoted as δ_d. The two duty cycles are written as [44],[45]

$$\delta_m(\Theta) = 1 - \frac{|V_{in}(\Theta)|}{V_0} = 1 - \frac{V_p|sin\,\Theta|}{V_0} \tag{7.3}$$

$$\delta_d(\Theta) = 1 - \delta_m(\Theta) = \frac{|V_{in}(\Theta)|}{V_0} = \frac{V_p\,|sin\,\Theta|}{V_0} \tag{7.4}$$

where $V_{in}(\theta)$ is the instantaneous input voltage, V_p is the peak amplitude of the input voltage, and V_o is the output DC voltage.

The average value of the MOSFET duty-cycle is given by

$$\delta_{m,avg} = \frac{1}{\pi}\int_0^{\pi}\left[1 - \frac{V_p|sin\,\Theta|}{V_0}\right]d\Theta = 1 - \frac{2\,V_p}{\pi\,V_0} \tag{7.5}$$

If switching ripple is disregarded, the inductor current is given by

$$i_L(\Theta) = I_p|sin\,\Theta| \tag{7.6}$$

where I_p is the amplitude of the output current of rectifier or input current for boost converter.

The instantaneous MOSFET and diode currents are given by

$$i_m(\Theta) = I_p|sin\,\Theta|\ \ \delta_m(\Theta) = I_p|sin\,\Theta|\ \left[1 - \frac{V_p|sin\,\Theta|}{V_0}\right] \tag{7.7}$$

$$i_d(\Theta) = I_p|sin\,\Theta|\ \delta_d(\Theta) = I_p|sin\,\Theta|\ \frac{V_p\,|sin\,\Theta|}{V_0} \tag{7.8}$$

Then the MOSFET rms current can be expressed by

$$I_{m,rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi}[i_m(\Theta)]^2\,d\Theta} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[I_p|sin\,\Theta|\ \left[1 - \frac{V_p|sin\,\Theta|}{V_0}\right]\right]^2 d\Theta} = I_p\sqrt{\frac{1}{2} + \frac{3}{8}\left[\frac{V_p}{V_0}\right]^2 - \frac{8\,V_p}{3\,\pi\,V_0}} \tag{7.9}$$

Similarly, the boost diode rms current can be given by

$$I_{d,rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi}[i_d(\Theta)]^2\,d\Theta} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[I_p|sin\,\Theta|\,\frac{V_p\,|sin\,\Theta|}{V_0}\right]^2 d\Theta} = \sqrt{\frac{3}{8}}\ \frac{I_pV_p}{V_0} \tag{7.10}$$

And the average diode current can be given by

$$I_{d,avg} = \frac{1}{\pi}\int_0^{\pi}\left[I_p|sin\,\Theta|\,\frac{V_p\,|sin\,\Theta|}{V_0}\right]d\Theta = \frac{I_p\,V_p}{2\,V_0} \tag{7.11}$$

Equations (7.9), (7.10), and (7.11) can be evaluated and applied for any boost derived topology for the conduction loss calculation.

The losses of components are illustrated as follows

A. Boost diode losses

The used SiC diode has very less reverse recovery losses so that they have been neglected. Therefore, the conduction losses are given by

$$P_d = V_F.I_{d,avg} + r_d\,I_{d,rms}^2 \tag{7.12}$$

where V_F and r_d are the forward voltage and resistance of the boost diode, respectively.

B. Bridge rectifier diode losses

The total power losses of bridge rectifier are given by

$$P_b = 4\ (V_{F,b}.\, I_{b,avg} + r_b\ I_{b,rms}^2) \tag{7.13}$$

where $V_{F,b}$ is the forward voltage and r_b is the resistance of rectifier diode. $I_{b,avg}$ and $I_{b,rms}$ are the average and rms value of the rectifier output current respectively and are given by

$$I_{b,avg} = \frac{1}{\pi}\int_0^{\pi}\left[I_p|sin\,\Theta|\right] d\Theta = \frac{2}{\pi} I_p \tag{7.14}$$

$$I_{b,rms} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[I_p|sin\,\Theta|\right]^2 d\Theta} = \frac{I_p}{\sqrt{2}} \tag{7.15}$$

C. MOSFET losses

The MOSFET is turned-on and turned-off with hard switching, because at the instant of turning-on, the voltage across the MOSFET is equal to the full output voltage and current will flow through the MOSFET reaching the value equal to $I_{sw,max}$ $\left(i.e.\ \left(\frac{I_0}{1-\delta_{m,avg}} + \frac{\Delta I_L}{2}\right)\right)$. The similar case occurs for the turning off the MOSFET, i.e. current decreases from its maximum value $I_{sw,max}$ to zero, while voltage will increase from zero to full output voltage.

Therefore the total switching losses of MOSFET are

$$P_{m,sw} = \frac{1}{2}\ V_0\ I_{sw,max}\left(t_{s,on} + t_{s,off}\right) f_s = \frac{1}{2}\ V_0 \left(\frac{I_0}{1-\delta_{m,avg}} + \frac{\Delta I_L}{2}\right)\ \left(t_{s,on} + t_{s,off}\right) f_s \tag{7.16}$$

where $t_{s,on}$ and $t_{s,off}$ are the MOSFET turn-on and turn-off time, respectively. ΔI_L is the estimated inductor ripple current and is expressed as

$$\Delta I_L = \frac{\frac{2}{\pi} V_p\ \delta_{m,avg}}{2\pi f_s\ L} = \frac{V_p\ \delta_{m,avg}}{\pi^2 f_s\ L} \tag{7.17}$$

where $\frac{2}{\pi} V_p$ is the input voltage of the boost converter and f_s.is the switching frequency of the MOSFET. The reverse recovery losses of SiC devices are very low and have been neglected.

The MOSFET conduction losses can be given by

$$P_{m,cond} = r_{ds,on}\ I_{m,rms}^2 \tag{7.18}$$

Therefore, the total power losses in MOSFET is

$$P_{m,T} = r_{ds,on}\ I_{m,rms}^2 + \frac{1}{2}\ V_0 \left(\frac{I_0}{1-\delta_{m,avg}} + \frac{\Delta I_L}{2}\right)\ \left(t_{s,on} + t_{s,off}\right) f_s \tag{7.19}$$

7.3.3 Interleaved Boost PFC

The interleaved configurations of a boost PFC converter comprise of two or more boost converter circuits connected in parallel and located after the input rectifier. The Fig. 7.7 shows the Interleaved Boost PFC configuration that consists of two boost converters connected in parallel [46], [47].

The MOSFETs are operated in such a manner so that the current ripple is reduced and at the same time the efficiency is increased. There are various control schemes for the operation of Interleaved Boost converter circuits in CCM, DCM or CRM mode to optimize efficiency

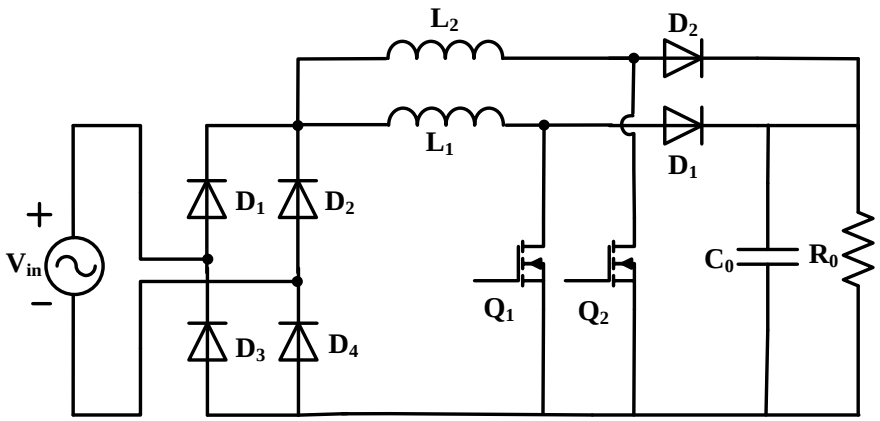


Fig. 7.7 Circuit diagram of Interleaved Boost PFC

at different load levels. With the power being distributed over multiple boost conversion circuits, losses are distributed over multiple devices, which is an advantage for their thermal design. As discussed in previous section, the CCM mode is more suitable since it has low inductor ripple current as well as low losses. For sinusoidal shape of the input current, PWM control with properly varying duty-cycle is used. The controller senses either the input current or that one at the diode rectifier output, the input voltage and the output DC voltage. The two parallel converters work with 180^0-phase delay to reduce the current ripple.

7.4 Simulation Analysis

The interleaved boost PFC circuit have been simulated for the CCM mode. The simulation scheme with the power and the control circuits is shown in Figs. 7.8. The parameters used in simulation are listed in Table 7.1.

Table 7.1: Parameters for Interleaved Boost PFC

Parameters	Value	Unit
Vin	311	Vrms
L_{pfc1}	7.9	mH
L_{pfc2}	7.9	mH
C_{in}	2.5	μF
C_o	1.2	mF
R_o	137	Ω
f_s	8	kHz

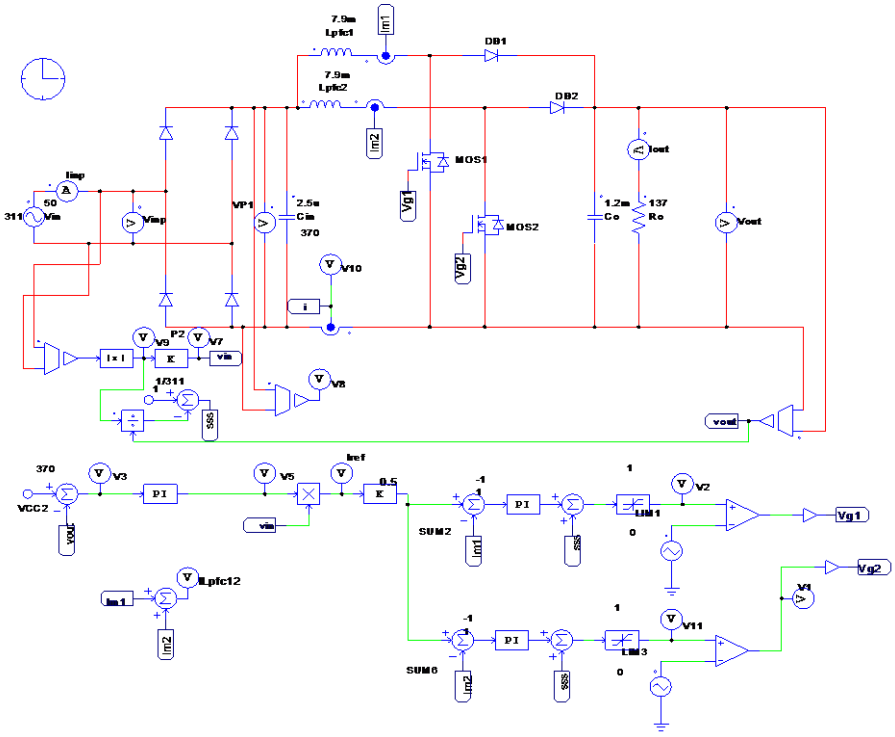


Fig. 7.8 Simulation scheme of Interleaved Boost PFC

As shown in the scheme, the error signal is generated by the output voltage of the boost converter. Error signal is processed through a PI regulator (voltage regulator) and its output is multiplied by the rectified output voltage (which is processed through the proportional gain 1/311 to reduce the amplitude to 1) to give the reference current. The reference current and the two inductor currents (i.e. I_{m1} and I_{m2}) generate two error signals that are processed

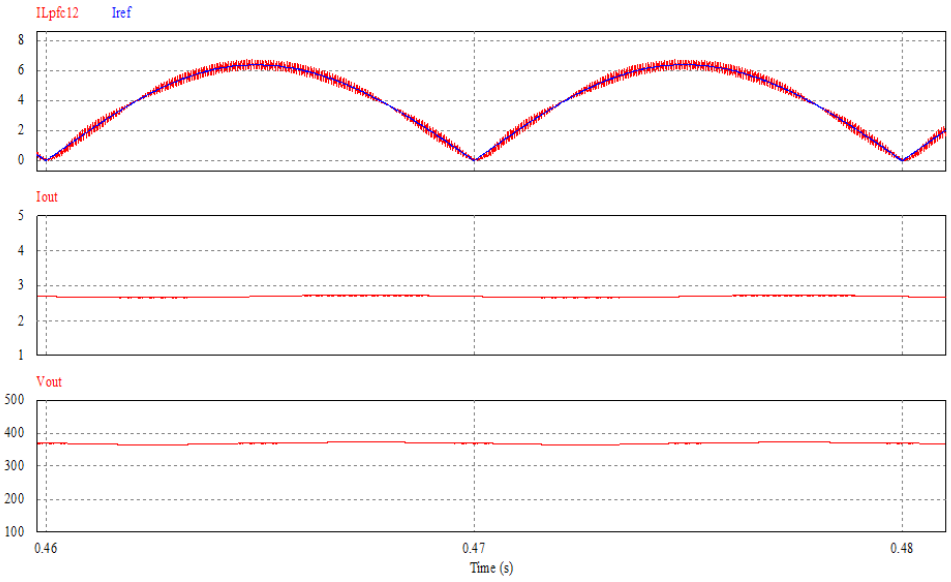


Fig. 7.9 Current and voltage waveforms of Interleaved Boost PFC

through other two PI regulators (current regulators) whose outputs are applied to limiters to limit the duty cycle references. Finally, the duty cycle references are compared with a triangular wave to generate the gate signals for the MOSFETs. The waveforms of the interleaved boost PFC are shown in Fig. 7.9.

7.5 Experimental Arrangement with DSP Interface

The experimental set up has designed for the interleaved boost PFC and for CCM mode operation. For the DSP programming, C-code has been used. The prototype of the designed circuit is shown in Fig. 7.10. As discussed before, two boost converters are connected in parallel. Two current sensors (i.e. one for each inductor) are used to sense the currents that pass through the inductors and the sensed signals are sent to the DSP. Based on the inductor current and output voltage, DSP generates the gate signals for two switches. To avoid a pulse of current at the start an input resistor has been placed in series with the diode rectifier; a relay is connected in parallel with the resistor to bypass it. At the starting time, relay is off, the current passes through the input resistor and charges the output capacitor with limited current. As soon as the voltage across the output capacitor approximates the grid peak, relay is switched on and input resistance is short-circuited.

7.5.1 Relay

A high capacity low profile relay model number G2RL-14 manufactured by OMRON corporation is shown in Fig. 7.11. The rated dc voltage and current of the coil of the relay

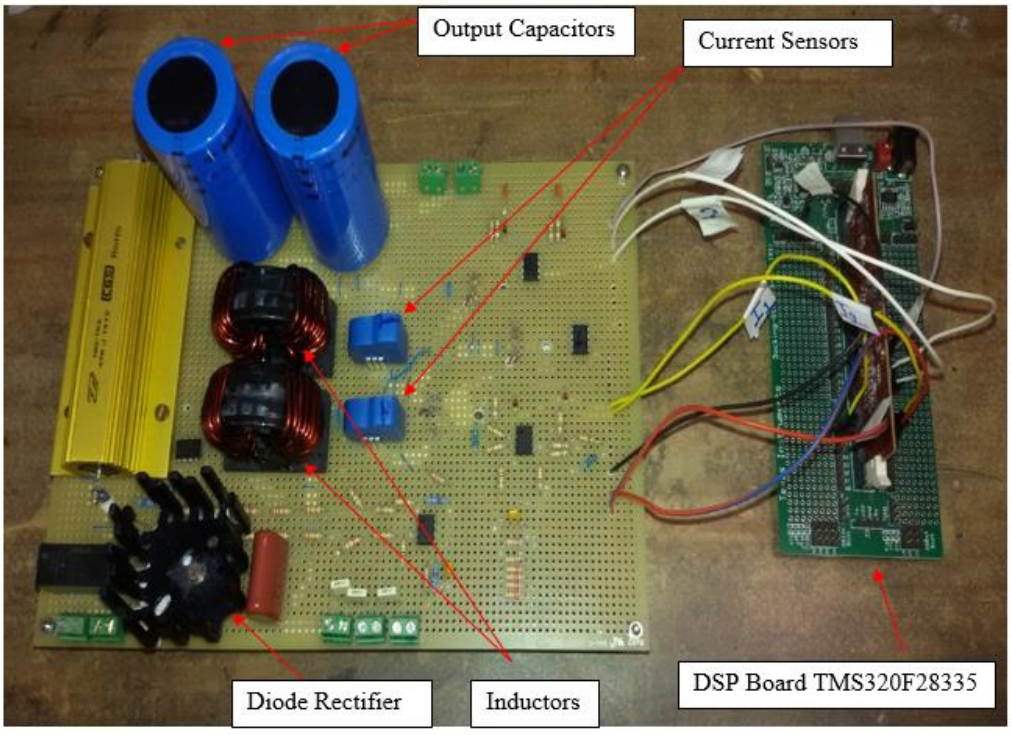


Fig. 7.10 Experimental setup of Interleaved Boost PFC with DSP interface

are 5V and 80 mA, respectively. As discussed before, relay is required to bypass the resistance which is connected in parallel. The relay is controlled by the DSP firmware.

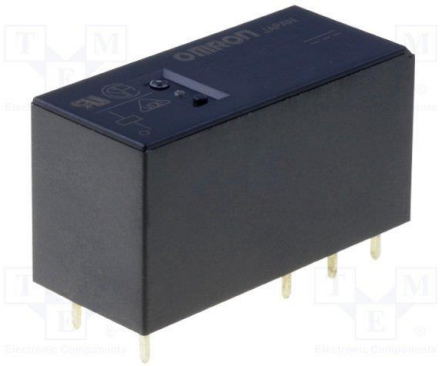


Fig. 7.11 Schematic of G2RL-14 Relay

7.5.2 Current sensor

A current sensors model number LTSP 25-NP manufactured by LEM technology is shown in Fig. 7.12. The primary nominal rms current is 25 A per turn while the secondary nominal rms current is 12.5 mA. In primary connection, there are three input points through that current will enter and three output points through that current will come out. Proper connection is required to adjust the number of turn for the device to the full-scale measured current. There are four terminals in secondary side, as shown in Fig. 7.12, to supply the device and to collect the output signal that corresponds to the sensed current. This sensor is suitable for the case where good accuracy, good linearity, low temperature drift and wide frequency band width is required.

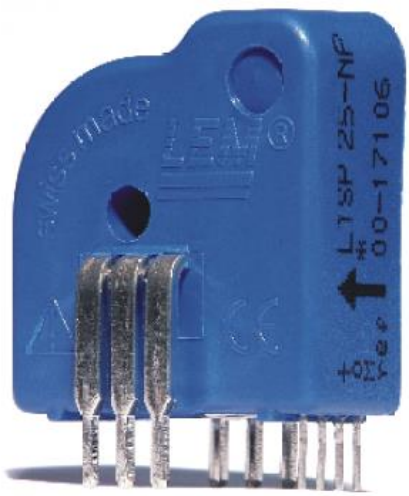
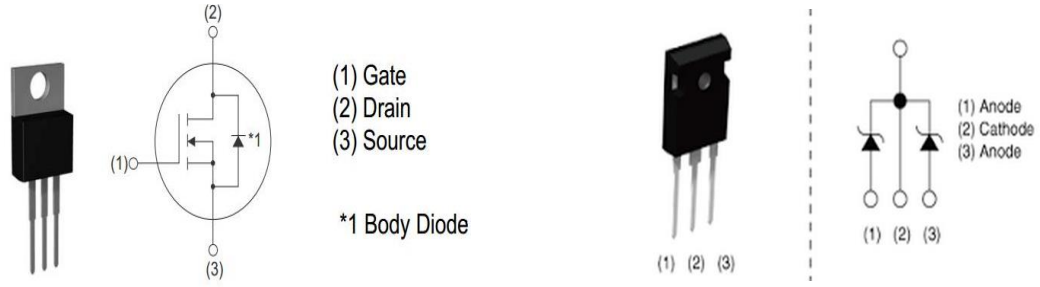


Fig. 7.12 Schematic of current sensor

7.5.3 Diode and MOSFET

Two SiC MOSFETs and one module (consists of two diodes) of SiC Schottky barrier diode, shown in Fig. 7.13, are used in the circuit. These devices have good switching performance, high breakdown voltage and high temperature limit. Voltage and current ratings of MOSFET reported in the data sheet are 650 V and 29 A, while the diode has the same voltage rating but different current rating, i.e. 10 A.



(a) SiC MOSFET (SCT2120AF)

(b) SiC Schottky barrier diode (SCS220AE2)

Fig. 7.13 Schematic diagram of MOSFET and diode

7.5.4 MOSFET driver

Two TC1411N MOSFET drivers are used to drive the MOSFETs of the converter. Maximum output current of the driver is 1A with the possibility of 5V to 15V supply. This driver is used with +15V biasing supply. PWM outputs from the DSP at pins GPIO-00 and GPIO-02 are provided to the drivers as an input. Outputs of this driver is connected to the Gate terminal of the MOSFETs. Functional block diagram and PIN out of the driver are shown in Figure 7.14.

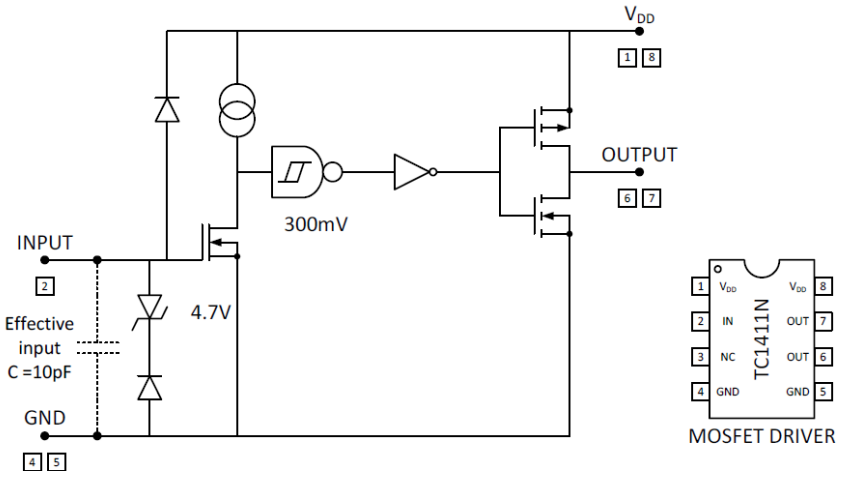


Fig. 7.14 Schematic diagram of functional block and PIN out of MOSFET driver

7.5.5 Programing in DSP

TMS320F28335 Digital Signal Controller (DSC) is used for the implementation of control algorithm for the interleaved boost PFC. Code Composer Studio (CCS) v5, which is provided by Texas Instruments (TIs), is used for the programming. Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers. The code debugging can be done with the simulator software that is part of CCS. The control algorithms are implemented in the interrupt service routine at the end of the ADC conversion. The schematic diagram of TMS320F28335 board is shown in Fig. 7.15. Assignments of input/output variables to GPIO (General Purpose Input Output) pins are listed in Table 7.2.

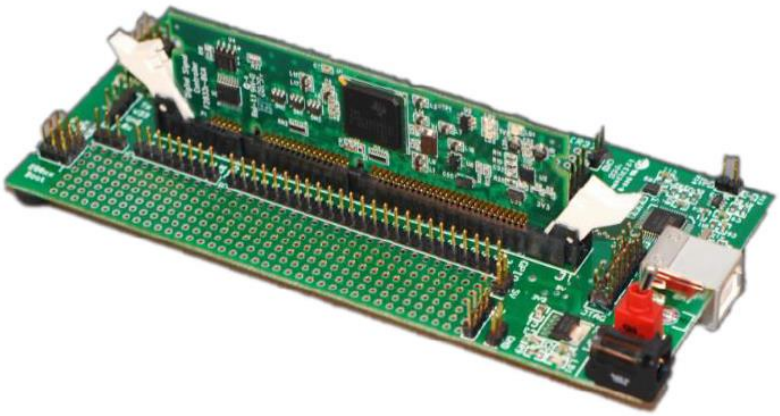


Fig. 7.15 DSP development board of the Texas F282335

Table 7.2: Input/output variables and GPIO connections

Variables	GPIO/ADC	Input/output
V_{AC}	A_6	Input
V_{DC}	B_6	Input
I_{m1}	A_7	Input
I_{m2}	B_7	Input
Relay command	GPIO-10	Output
δ_2	GPIO-02	Output
δ_1	GPIO-00	Output

7.6 Summary

The active power factor correction technique has been discussed in details in this work, which has number of advantages over passive power factor correction method in terms of size, volume and weight of the circuit elements. The active power factor correction circuit is more compact and weighs less compared to passive power factor correction circuit. A single phase interleaved PFC has been investigated very closely. The circuit operation for the CCM mode is discussed in detail and the power losses in the devices and rectifier are calculated. The circuit has been simulated with the help of PSIM software and simulation results are presented. A prototype of interleaved boost PFC circuit is designed with using SiC MOSFET and SiC diode. The procedure of design is discussed in details. To control the circuit, computer assisted DSP interface is adopted. For the DSP programming, Code Composer Studio (CCS) v5, provided by Texas Instruments is used.

Chapter 8

Synchronous Rectifier

8.1 Introduction

An SR is able to reduce the conversion losses due to the device conduction, thus leading to improvement in efficiency. The conduction losses contribute significantly to the overall power loss of a diode rectification circuit, especially in low output-voltage applications. In the diode, the conduction losses depend on the forward voltage drop, the diode resistance and the magnitude of current that passes through the devices while in a MOSFET the conduction losses depend on the on resistance ($R_{DS,on}$) of the MOSFET and the current that passes through the devices. Moreover, driving losses are also a part of the losses in a MOSFET but they are negligible compared to the total power losses up to frequencies of hundreds of kHz. Therefore, the MOSFET-based SR is widely adopted in low output voltage applications. Another possibility is the use of Schottky diodes as they have low forward voltage drop as compared to pn-junction diode but they are suffering from a number of limitations like high leakage current and lower temperature operation. Hence, a MOSFET-based SR is commonly used in place of Schottky diode-based SR. Besides being attractive for efficiency, a MOSFET-based SR is also attractive in applications sensitive to converter size (higher power densities) such as portable or handheld equipment, and thermal performance (higher operating temperature).

The on resistance ($R_{DS,on}$) of a MOSFETs can be lowered, either by increasing the size of the die or by paralleling more devices. Moreover, $R_{DS,on}$ has a positive temperature coefficient. The paralleled MOSFETs will automatically tend to share current equally, facilitating optimal thermal distribution among the devices. This improves the ability to remove heat from the components and the PCB, directly improving the thermal performance of the design. MOSFET manufacturers like Cree, Rohm, and Infineon are constantly introducing new MOSFET technologies that have lower $R_{DS,on}$ and total gate charge (Q_G), which makes it easier to implement SR in power converters.

The major difficulty in synchronous rectification is to design the driving circuit. The SR driving signal can be obtained through two ways, self-derived and external-controlled. Self-derived method develops SR driving signal by detecting either the current flowing through SR or the voltage drop across a SR. External-controlled method develops a SR drive signal from the voltage signal that exists in the switching topology and coincides with the desired drive timing [48]-[52]. Moreover, in self-derived method, the voltage driven is more attractive for its simplicity and low cost but it is topology dependent and usually only suitable for voltage feed topologies. Instead, current-driven method senses the current entering into

the SR to turn on or off the SR devices properly and hence it is topology-independent. Therefore, a current-driven SR can directly replace a diode rectifier in any topology.

8.2 Benefits of Synchronous Rectifier

As discussed above, the advantages of using MOSFET-based SRs in high-performance, high-power converters include better efficiency, lower power dissipation, better thermal performance, and inherently optimal current sharing when MOSFETs are paralleled. The downside of the MOSFET-based SRs is that they require control circuitry to ensure the devices turn on or off synchronously with the current direction, i.e. at the right time. Circuitry required for the control of the SR normally includes current detectors and drive circuity for the MOSFET devices.

8.3 Case Study

The losses of the secondary rectifier play an important role in the total efficiency of the wireless power transfer (WPT) system [53]. The rectifier is used in WPTS for supplying the DC link capacitor at the secondary. The rectifier receives high frequency AC power supply from the secondary or receiver coil as an input. This AC power, after rectification, is entered into a chopper before being fed into the battery by help of a chopper for the controlled current-voltage charging of the battery. Today WPT systems of medium power work on the inductive resonant coupling principle. They operate at high frequency i.e. 85 kHz, to get reduced current circulation in the primary and reduced size of the coupling coils. For the rectification of the secondary power, the switches of the rectifier must have low losses to improve the efficiency in the WPT system. The important parameters of the secondary of the study-case WPT system are listed in Table 8.1.

Table 8.1: Wireless power transfer system secondary parameters

Parameters	Symbol	Value
Maximum receiver coil current	I_L	10 A_{rms}
Maximum rectifier input AC voltage	V_S	65 V_{rms}
Nominal chopper input DC voltage	V_{DC}	65 V
Maximum chopper input current	I_{DC}	14A

8.4 Operation of Synchronous Rectifier

8.4.1 Power circuit and working principle

Fig. 8.1 shows the circuit diagram of an SR that consists of four transistor with their body diodes. The transistor of the circuit are MOSFETs that can conduct in both the directions. The MOSFETs used in the study case are SiC devices. They have a fast switching behaviour

that allows to have a minimum dead-time during that body diodes will conduct. The circuit is supplied by a sinusoidal voltage source with an in-series inductor.

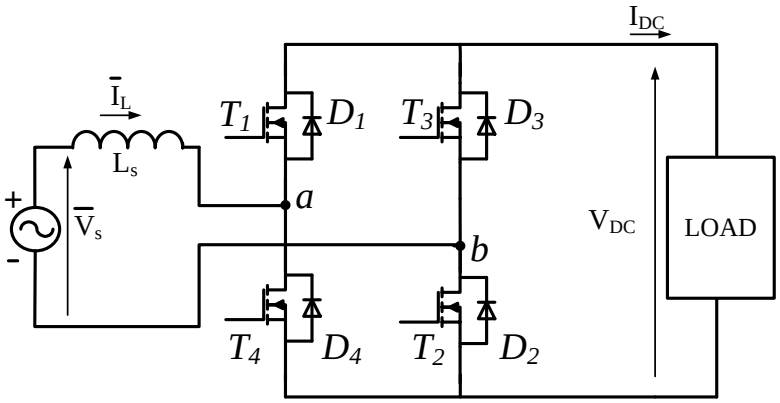


Fig. 8.1 Schematic diagram of synchronous rectifier

For the circuit above, the current-driven SR is used to generate the signal driving the gate of the MOSFET devices. As above explained, the current-driven method senses the current entering into the SR to turn-on and turn-off the MOSFETs properly.

8.4.2 Control scheme and waveform

The waveforms of input current and gate signals are shown in Fig. 8.2. For positive half-cycle of the current, the current will enter into terminal a of the rectifier. Let us start the analysis of the operation within the half-cycle. The MOSFETs T_1 and T_2 are on and remain in this state until the input current becomes zero. When the input current becomes zero, the gate signals are withdrawn to turn-off the MOSFETs T_1 and T_2 and the turn off is done by a soft switching because the current and voltage across the MOSFETs are zero. At this time, dead-time must be inserted before switching on MOSFETs T_3 and T_4. During the dead-time the current is negative and goes through the body diodes D_3 and D_4. A small negative V_{DS} appears across the MOSFETs T_3 and T_4. Just after the dead-time, the gate signals are applied to MOSFETs T_3 and T_4 and they are turned on again by a nearly soft switching because both the inrush current and the voltage across the MOSFETs are very small. The process just described repeats half-cycle after half-cycle.

Two abnormal situations can occur: (a) current has a spike and (b) current has multiple zero crossing as shown in Figs. 8.3 and 8.4 respectively. The two situations are analyzed here in the view of the circuit implementation.

Let us consider case (a) and let the spike be high enough to change the direction of the current and shorter than the dead-time. At the spike, sensor detects a negative current and MOSFETs T_1 and T_2 are turned-off and negative current flows through the body diodes D_3 and D_4. Then, the current crosses the zero level and becomes positive. If the spike length is less than the dead-time, the body diodes D_1 and D_2 start conducting for the dead-time C as

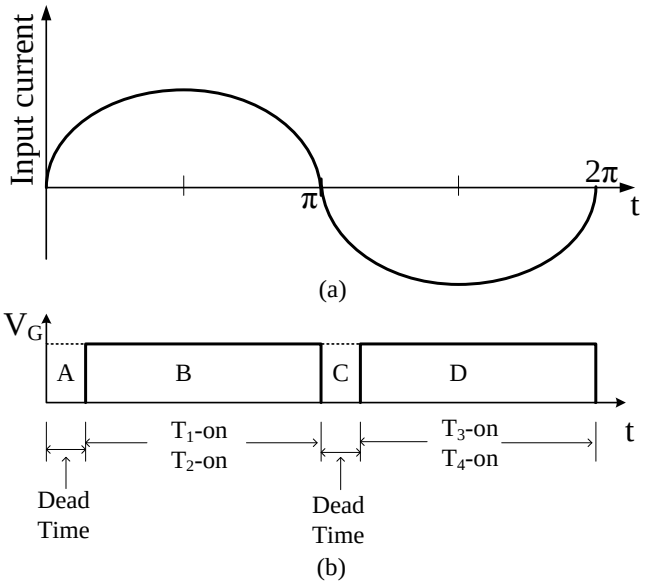


Fig. 8.2 Waveforms (a) input current and (b) gate signal

shown in Fig. 8.3. After the dead-time *C*, the MOSFETs T_1 and T_2 are turned on again as the current is positive.

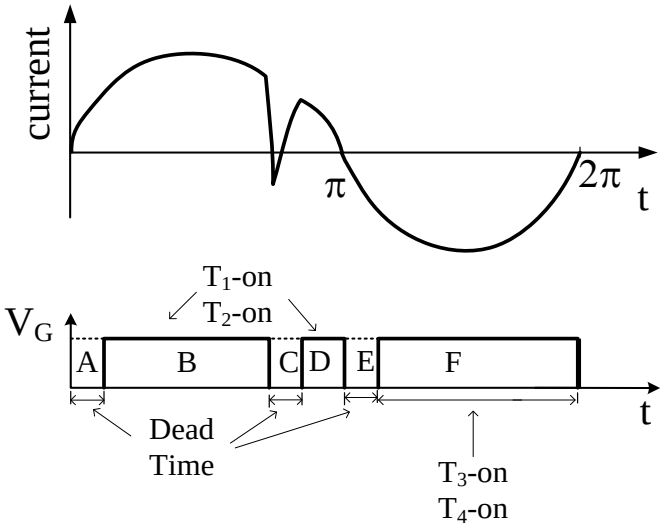


Fig. 8.3 Waveform of current spike

Let us now consider case (b) and let the multiple crossing shorter than the dead-time. When the current passes from positive to negative (i. e. at point z_1), sensor detects zero current and MOSFETs T_1 and T_2 are turned off. The negative current flows through the body diodes D_3 and D_4. At the successive zero crossing, (i. e. at point z_2) the current becomes positive and flows in the body diodes D_1 and D_2. After that the process goes on as usual.

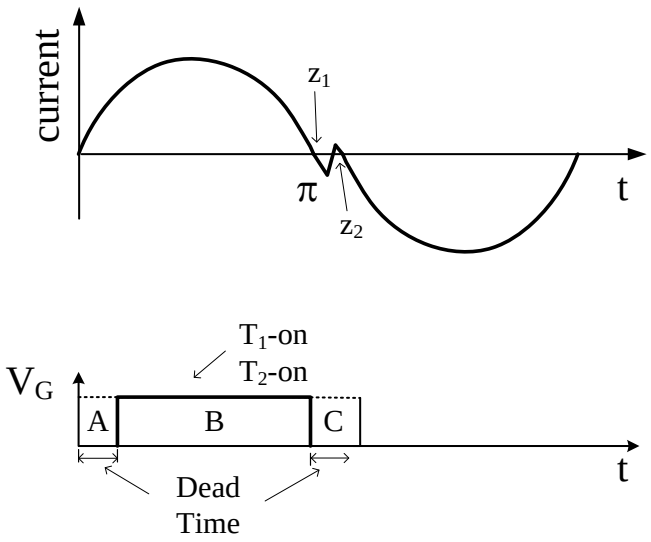


Fig. 8.4 Waveform of current with multiple zero crossing

8.5 Loss Analysis for Power Rectifier

The different types of losses in a MOSFET and in a diode have been explained in chapter 5. With the help of equations used in chapter 5, switching losses and conduction losses of MOSFET and diode can be readily calculated.

The Si-Schottky barrier diode, SiC schottky barrier diode and SiC MOSFET have been selected for the loss calculation [53],[54]. The part number and other specification of the devices are shown in Table 8.2. The total power losses have been calculated for all three rectifiers: built with Si diodes, SiC diodes and with the same rating of SiC MOSFETs.

8.5.1 Diode Rectifier

Total power loss of the diode rectifier is the sum of the conduction losses and switching losses of all the four diodes. The loss calculation for the diode rectifier is given below.

The switching losses in diode is mainly due to the reverse recovery energy (E_{rr}). Therefore, the switching losses of D_1 and D_2 can be given by

$$P_{sw,D_{12}} = 2 \cdot \left(Q_{rr} \cdot V_{Drr} \cdot f_s\right) \cdot \tag{8.1}$$

where Q_{rr} is the reverse recovery charge of the diode and the voltage across the diode during reverse recovery (V_{Drr}) is approximated to the voltage across the diode (V_{SD}).

The conduction losses of D_1 and D_2 for the positive cycle of input current i.e. (intervals A and B) can be given by.

$$P_{cond,D_{12}} = P_{cond,D_1} + P_{cond,D_2} = f_s \cdot \left[2 \cdot \left(V_{FO} \cdot I_{o,avg} + r_d \cdot I_{o,rms}^2\right) \cdot t_{A-B}\right] \tag{8.2}$$

Therefore, total power losses of D_1 and D_2 is given by

$$P_{D_{A-B}} = P_{sw,D_{12}} + P_{cond,D_{12}} = f_s \cdot \left[2 \cdot \left(Q_{rr} \cdot V_{SD}\right) + 2 \cdot \left(V_{FO} \cdot I_{o,avg} + r_d \cdot I_{o,rms}^2\right) \cdot t_{A-B}\right] \quad (8.3)$$

Similarly, the losses can be calculated for diode D_3 and D_4 which occurred in negative cycle of the input current i.e. (intervals *C* and *D*) and must be equal to the $P_{D_{A-B}}$.

Therefore, the total power loss in diode rectifier is given by

$$P_{T,D} = 2 \cdot P_{D_{A-B}} \quad (8.4)$$

Table 8.2: Parameters of Si diode, SiC diode and SiC MOSFET

Parameters	**Si-Ultrafast Diode**	**SiC Schottky Barrier Diode**	**SiC MOSFET**
Part Number	HFA15TB60	SCS220AE2	SCT2120AF
V	600V	650 V	650 V
I	15A	20A	29 A
$r_{DS,on}$	-	-	120 m Ω
R_G	-	-	13.8 Ω
$V_{GS(th)}$	-	-	1.6 V
V_{FO}	1.3	1.35 V	4.3 V
r_d	0.05 Ω	0.05 Ω	0.10 Ω
Q_{GS}	-	-	14 nC
Q_{rr}	84 nC	15 nC	53 nC
C_t	514 pF	-	-
t_{rr}	19ns	15 ns	33 ns
f_s	85 kHz	85 kHz	85 kHz

8.5.2 Synchronous Rectifier

The total power loss of the SR is the sum of the switching losses and conduction losses of the MOSFETs and the losses associated with their body diodes. The switching losses of the MOSFET are very low as the MOSFET turned-off at zero current and turned-on at very low voltage because the voltage across the MOSFET is equal to the voltage across their body diode, which is conducting. Therefore, the conduction losses have the significant effect in the total power loss of synchronous rectifier [55]-[60]. The total power losses for the SR circuit can be given by

$$P_{T,M} = P_{cond} + P_{sw} = f_s \cdot \begin{Bmatrix} 2 \cdot \left(V_{FO} \cdot I_{o,avg} + r_d \cdot I_{o,rms}^2\right) \cdot \left(t_A + t_C\right) + 2 \cdot \left(r_{ds(on)} \cdot I_{o,rms}^2\right) \cdot \left(t_B + t_D\right) + \\ 4 \cdot \frac{1}{2} \cdot \left(V_{FO} + r_d \cdot I_{o,avg}\right) \cdot I_{o,avg} \cdot t_{on} + 4 \cdot Q_{rr} \cdot V_{SD} + 8 \cdot Q_{GS} \cdot V_{GS} \end{Bmatrix} \quad (8.5)$$

The total power losses has been calculated for diode rectifier and synchronous rectifier and shown in Fig. 8.5. The result shows that the total power loss in SR is less as compared to diode rectifier with the frequency varied from 1 kHz to 85 kHz. It is clear that at 85 kHz frequency which is the operating frequency of WPT system, the power losses in synchronous rectifier is approximately half of the diode rectifier. Therefore, synchronous rectifier can increase the overall efficiency of the WPT system.

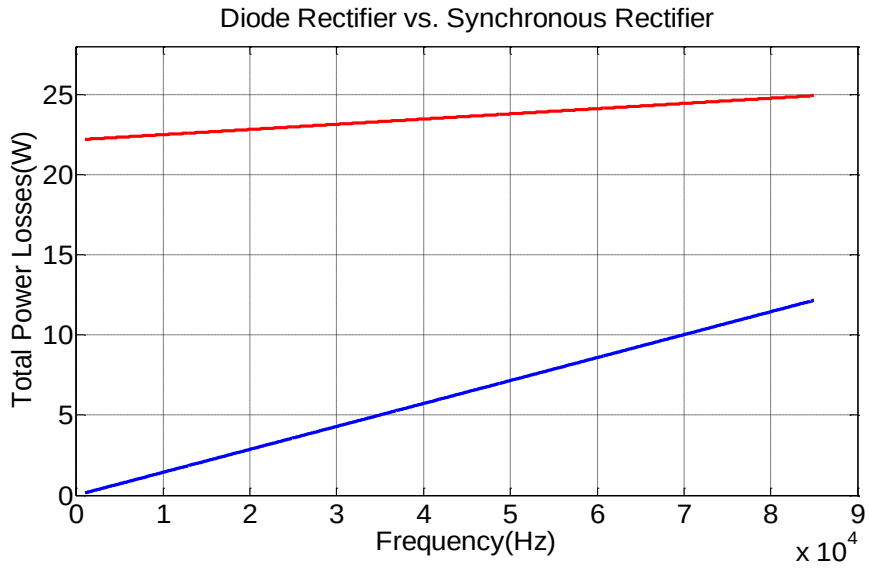


Fig. 8.5 Power loss comparison between SiC diode rectifier (red) and SiC synchronous rectifier (blue) at V_{in}=65 V_{rms}, I_{in} =7.07 A_{rms}

8.6 Simulation

The simulation circuit for SR is shown in Fig. 8.6. For simulation purposes, the input current is sensed by the current sensor and compared with a zero reference value. The gate signals for the MOSFET 1 and MOSFET 2 are generated by comparing the positive current with zero value while the gate signals for the MOSFET 3 and MOSFET 4 are generated by comparing the negative current with zero value. To implement a dead time delay circuit is used. As MOSFETs are bidirectional devices, can also conduct in reverse direction. During the dead time, body diodes of corresponding MOSFETs are conducting, at the end of dead time current starts flowing through the corresponding diagonal MOSFETs. The waveforms of current and voltage signals are shown in Fig. 8.7.

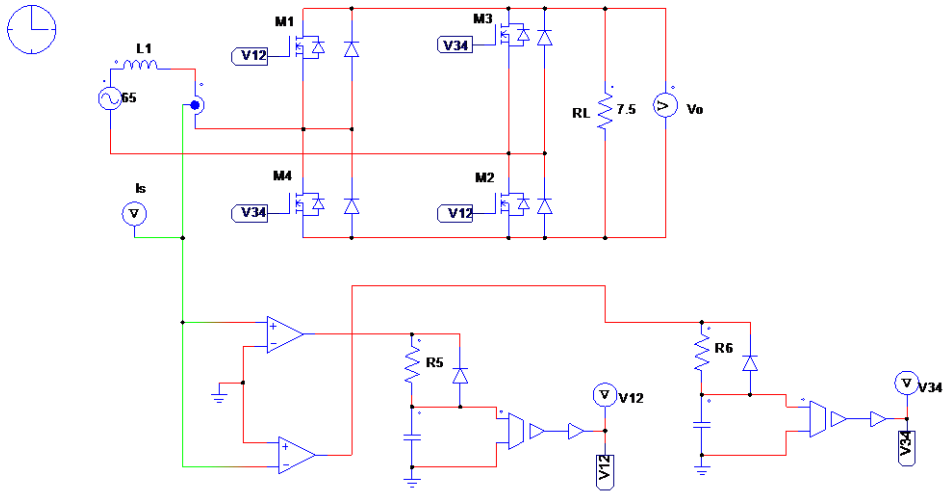


Fig. 8.6 Simulation circuit for synchronous rectifier

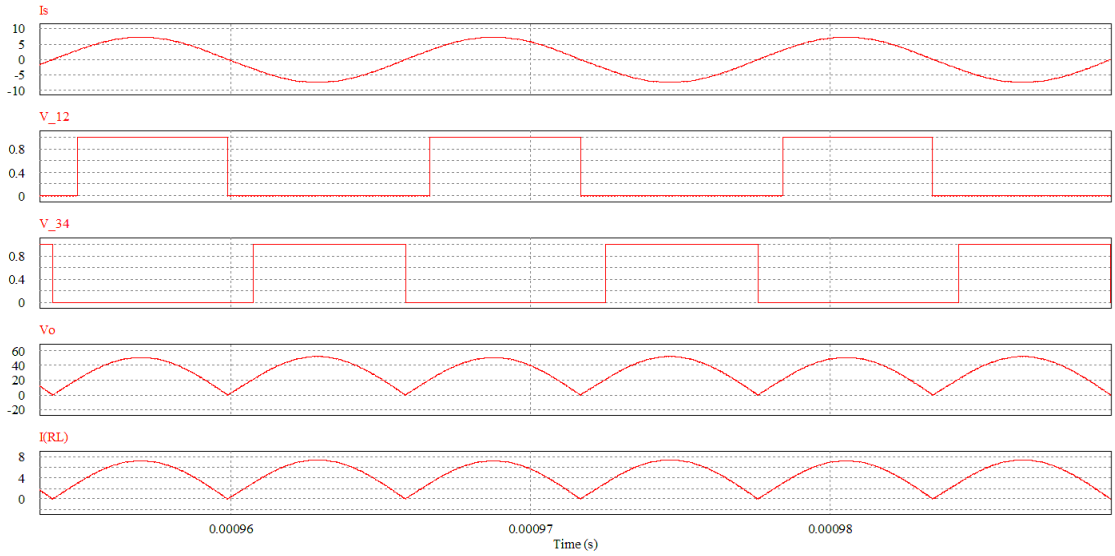


Fig. 8.7 Current and voltage waveforms for synchronous rectifier

8.7 Prototype Design

A prototype of SR is designed with using SiC MOSFETs [61]-[63]. The layout diagram of the SR is shown in Fig. 8.8. The differential amplifier circuit is used to amplify the difference between two output voltages of current sensor and it gives the output signal proportional to the sensed current. The output of differential circuit is connected with the two operational amplifier circuits for the comparison purposes. The delay circuits are used to introduce the dead time, at that period all the MOSFETs is turned off. Based on the layout diagram the of the SR, designed prototype is shown in Fig. 8.9. The prototype consists mainly four SiC MOSFETs with their antiparallel diodes, one current sensor, MOSFET drivers, operational amplifiers, and a series inductor.

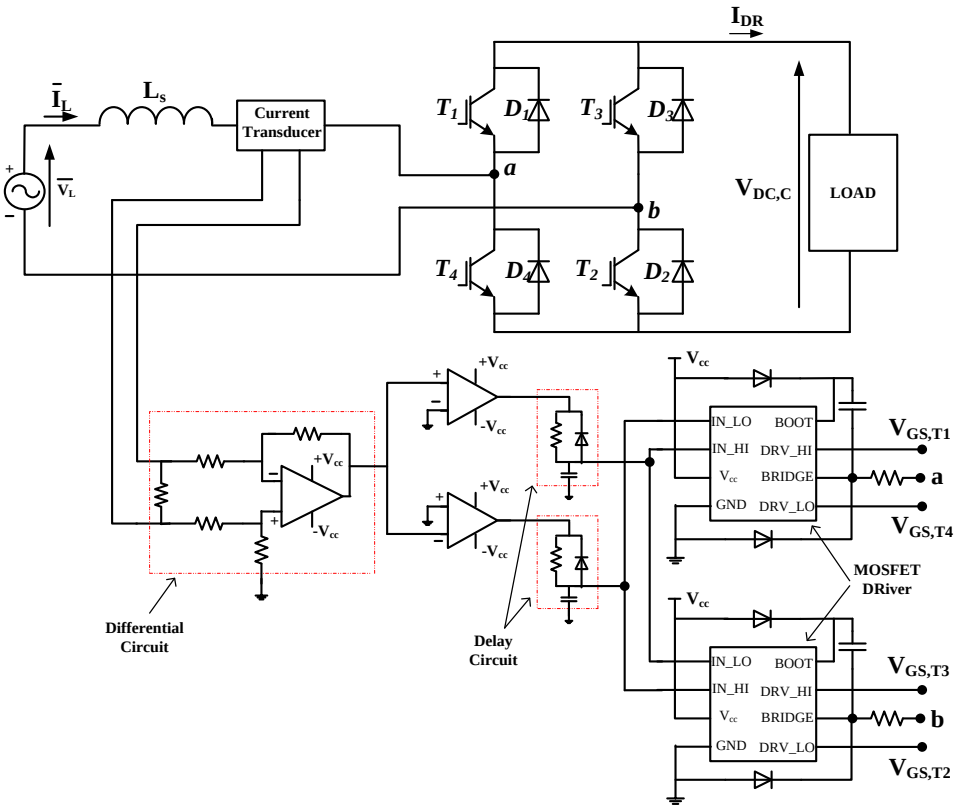


Fig. 8.8 Circuit layout of synchronous rectifier

As discussed before, the gate signals are generated by the self-derived current-driven method. The current transducer detects the input current and compares with zero value to know the zero crossing; based on that the gate signals are generated for the positive half and

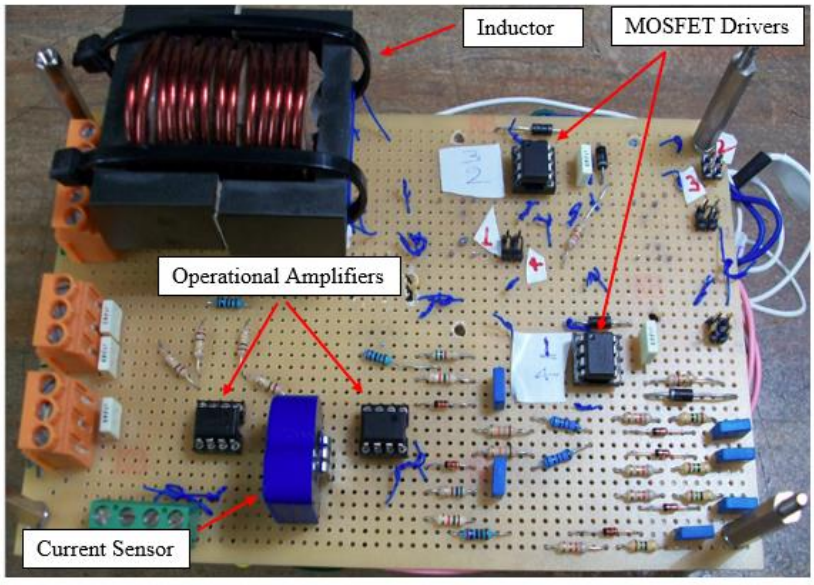


Fig. 8.9 Prototype of synchronous rectifier

negative half of the input current. The signals generated through positive half of the current are fed to the MOSFET 1 and MOSFET 2 as shown in Fig. 8.8 while signals generated through the negative half are fed to the MOSFET 3 and MOSFET 4.

The components used in this prototype are listed in Table 8.3 with their manufacturer name. The brief details of current transducer and SiC MOSFET have been explained in previous chapter. The proper drivers are used to drive the MOSFETs that can provide the signals to the high side (i.e. MOSFET 1) and low side (i.e. MOSFET 4) devices because the high side MOSFET has the floating source terminal that has the different voltage level than lower side MOSFET.

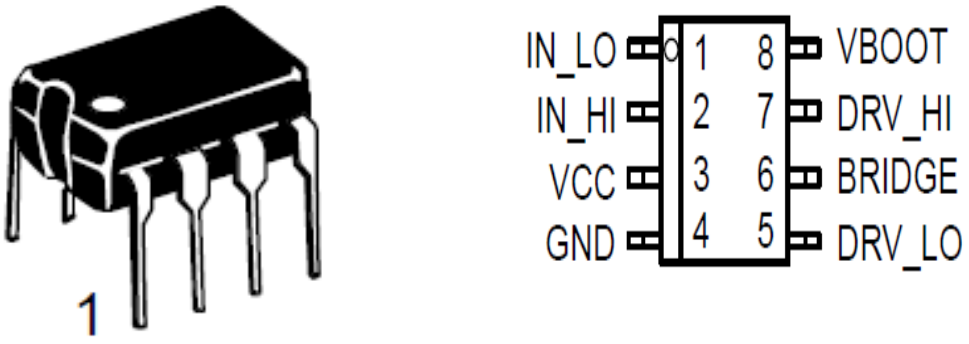
Table 8.3: List of components used for SR design

Components	Part Number	Numbers	Manufacturer
Current Transducer	LTSP-25NP	1	LEM
SiC MOSFET	SCT 2120AF	4	ROHM Semiconductor
MOSFET Driver	NCP-5304	2	ON Semiconductor
Operational Amplifier	TL072IP	2	TEXAS Instruments
Inductor	-	1	

8.7.1 MOSFET driver

The NCP5304 is a High Voltage Power gate Driver providing two outputs for direct drive of 2 N−channel power MOSFETs or IGBTs arranged in a half−bridge configuration. It uses the bootstrap technique to insure a proper drive of the High−side power switch. The driver works with two independent inputs with cross conduction protection. It has in-built internal fixed dead time of 190 ns. The main power supply voltage can vary from -0.3 to 20 volts while the maximum allowable voltage at bridge pin is 600 volts. Two output signals of this driver are connected to the gate terminal of high side and low side MOSFETs. The schematic and pinout information of the driver are shown in Fig. 8.10. The IN_LO and IN_HI are the two input signals of the driver for low side and high side MOSFETs respectively while the DRV_Hi and DRV_LO are the two output signals. The V_{cc} is the supply voltage of the driver and BRIDGE point is connected to the common point of high side and low side MOSFETs.

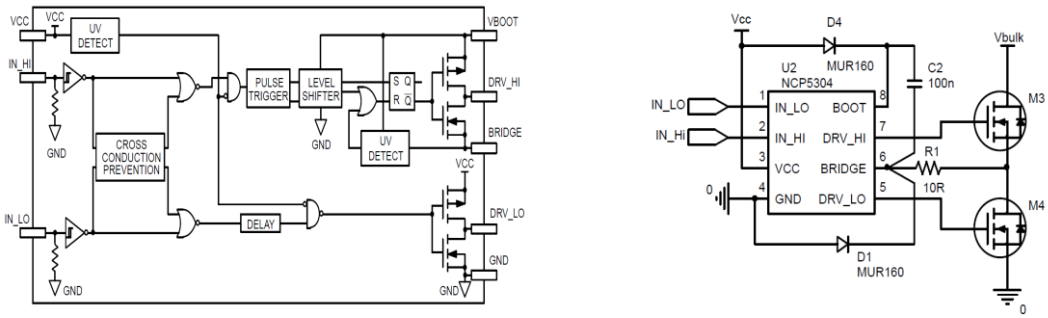
Fig. 8.11 shows the functional block diagram and half bridge connection diagram of the driver. The low-side driver is designed to drive a ground-referenced low $R_{DS(ON)}$ N-channel MOSFET. The bias to the low-side driver is internally connected to the V_{CC} supply and GND. Once the supply voltage ramps up and exceeds the undervoltage lockout (UVLO)



(a) (b)

Fig. 8.10 MOSFET driver NCP-5304 (a) Schematic (b) Pinout information

threshold (i.e. detected by UV dectector), the driver is enabled. The high-side driver is designed to drive a floating low $R_{DS(ON)}$ N-channel MOSFET. The bias voltage for the high-side driver is developed by an external bootstrap supply circuit, which is connected between the V_{BOOT} and BRIDGE pins. The bootstrap circuit comprises a diode, D_4, and bootstrap capacitor, C_2. When the NCP 5304 is starting up, the BRIDGE pin is at ground, so the bootstrap capacitor charges up to V_{CC} through D_4. Once the supply voltage ramps up and exceeds the UVLO threshold, the driver is enabled. When IN_HI goes high, the high-side driver begins to turn on the high-side MOSFET by transferring charge from C_2. As high side MOSFET turns on, the BRIDGE pin rises up to V_{bulk}, forcing the BRIDGE pin to V_{bulk}+ V_{C2}, which is enough gate-to-source voltage to hold upper MOSFET on. To complete the cycle, Upper MOSFET is switched off by pulling the gate down to the voltage at the BRIDGE pin. When the low-side MOSFET turns on, the BRIDGE pin is pulled to ground. This allows the bootstrap capacitor to charge up to V_{CC} again. When the driver is used in a half bridge configuration as shown in Fig. 8.11 (b), it is possible to see negative voltage appearing on the BRIDGE pin during the power MOSFETs transitions. To protect the negative voltage



(a) (b)

Fig. 8.11 Block Diagram of MOSFET driver NCP-5304

reaches beyond the safe operating area one resistance R_1 and a diode D_1 are connected and hence, negative voltage developed to the BRIDGE pin will be limited by D_1 and R_1 and will prevent any wrong behavior.

8.7.2 Operational amplifier

The operational amplifiers are used to control the synchronous rectifier. The amplifiers manufactured by Texas Instruments (i.e. TL072IP) have low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make these devices ideally suited for control applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip. The pin diagram of the amplifier is shown in Fig. 8.12. One TL072IP can be used for two separate sets of input/ output operation.

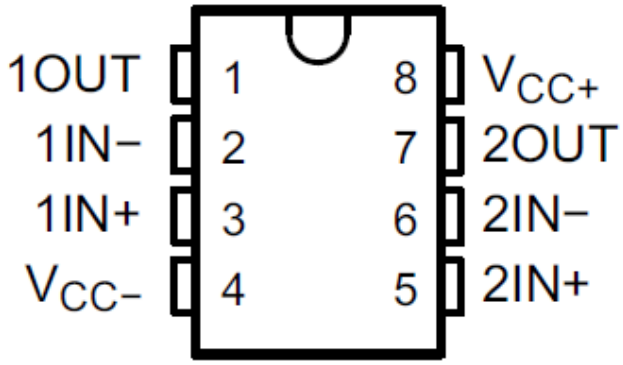


Fig. 8.12 Pin Diagram of operational amplifier TL072IP

8.7.3 Passive components

An inductor L of 369 mH is connected in series that is made from the 2.0 mm diameter and 2HG varnish coated copper wire. This inductance prevent the instantaneous change of current.

8.8 Experimental Setup

The experimental setup is shown in Fig. 8.13. A variable resistance is used as a load which is the equivalent resistance seen by the chopper for the WPT system. The resistance decreases from 11.7 Ω to 7.5 Ω during the constant current stage of the charging process because of the increasing of battery voltage and then it increases quickly up to 754 Ω during the constant voltage stage because of the decreasing of battery current. The DC power supply is used for the requirement of input supply for the amplifier, driver and other components that required low voltage DC supply. An Agilent oscilloscope is used to trace the different waveforms.

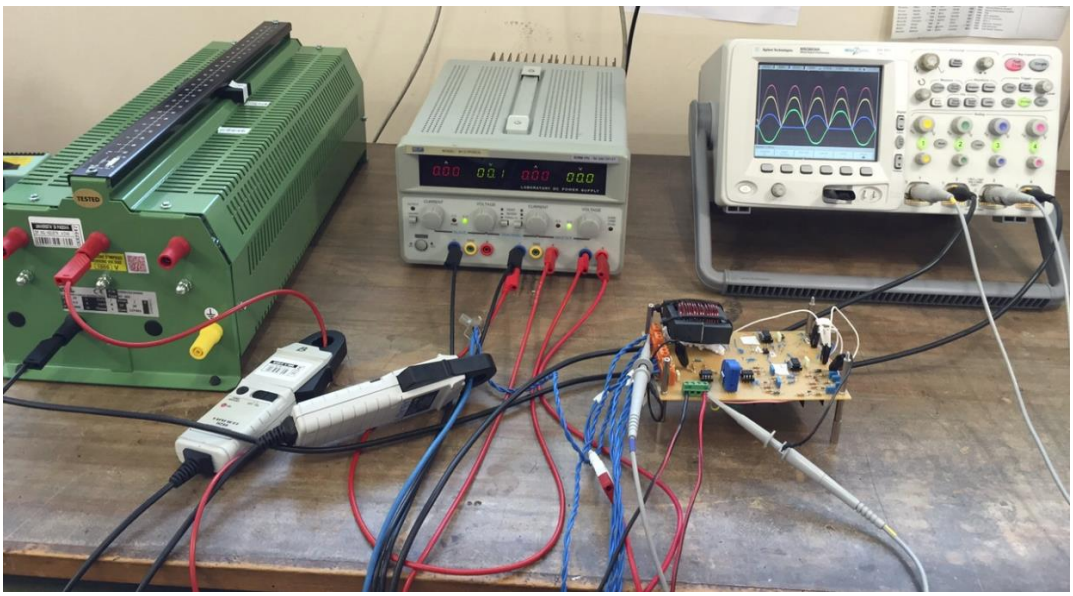
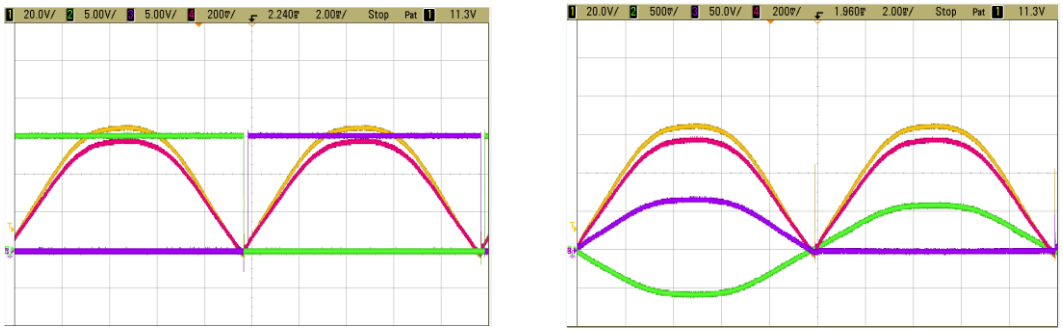


Fig. 8.13 Experimental setup of synchronous rectifier

The experiment has been performed for the different value of voltage and current to verify the estimated result. Fig. 8.14 (a) shows the waveforms of rectified voltage, current and the gate signals of the MOSFETs 1,2 and MOSFETs 3,4 at load resistance R_L=7.5 Ω.

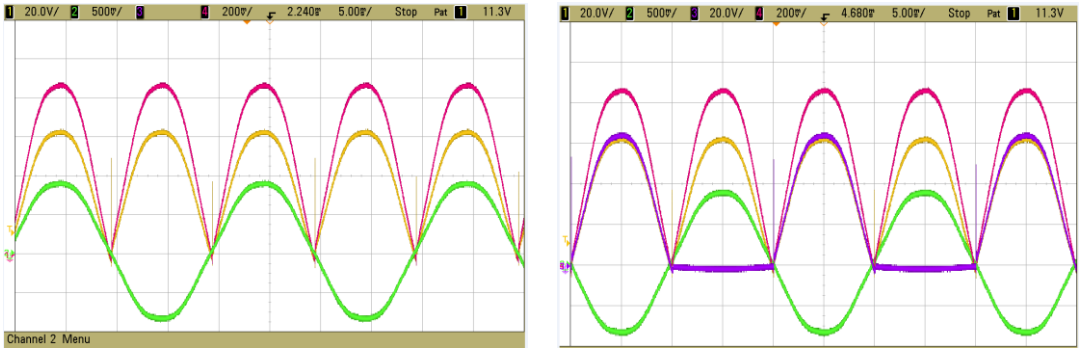


(a) (b)

Fig. 8.14 Waveforms at R_L=7.5 Ω (a) rectified voltage (yellow), current (red) and MOSFET signals (green and purple) (b) input current (green), rectified voltage (yellow), rectified current (red) and the voltage across the MOSFET (purple)

Fig. 8.14 (b) shows the waveforms of rectified voltage, current and the voltage across the MOSFET 2 at load resistance R_L=7.5 Ω. It is clear that once the MOSFET is conducting, the voltage across the switch is near zero while when MOSFET is not conducting the voltage across the switch is full-applied voltage.

Fig. 8.15 shows the waveforms of input current, rectified voltage ,rectified current and voltage across the MOSFET at load resistance R_L=11.7 Ω.



(a) (b)

Fig. 8.15 Waveforms at R_L=11.7 Ω (a) input current (green), rectified voltage (yellow), and rectified current (red) (b) input current (green), rectified voltage (yellow), rectified current (red) and the voltage across the MOSFET (purple)

Fig. 8.16 shows the voltage across the switch (purple line). It indicates that only diodes are conducting during the dead time and the voltage drop across the switch is equal to the sum of forward voltage drop and the voltage drop across the diode resistance. Once the MOSFET turned on then the voltage drop across the switch is reduced because of the MOSFET has less resistance as compared to diode.

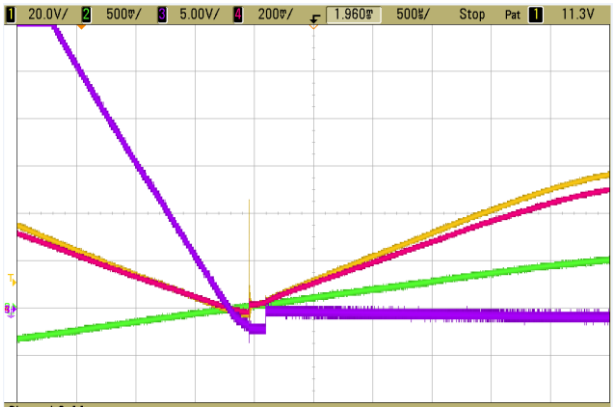


Fig. 8.16 Enlarge view of voltage waveform during diode and MOSFET conduction at R_L=11.7 Ω

8.9 Results and Discussion

The experiment has been performed at line frequency and the total power loss has been calculated for the Synchronous Rectifier. The dead time of the commutation is fixed at 1 ms for the MOSFET legs.

Therefore, the total power loss of synchronous rectifier has been calculated from equation (8.5). At V_{in}=65 Vpeak, I_{in} =6 Apeak, and R_L=11.7 Ω, the total power losses is 3.71 Watt

while at V_{in}=65 Vpeak, I_{in} =9 Apeak, and R_L=7.5 Ω, the total power loss is 5.91 watt that is shown in Fig. 8.17. It is clear that the total power loss is increased when the current is increased.

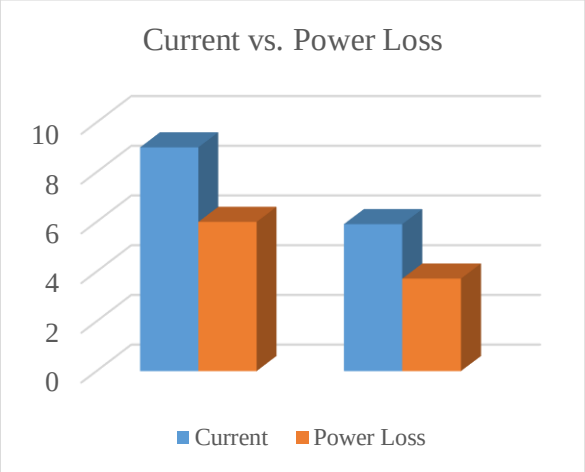


Fig. 8.17 Current vs. power loss of Synchronous Rectifier

Further, the input power and output power is measured by the power analyser YOKOGAWA model number WT 1800 to calculate the efficiency. The input voltage kept constant 65 V_{rms} and the load resistance is decreases to increase the output current. The efficiency of synchronous rectifier and diode rectifier at different output power is shown in Fig 8.18. From the Fig. 8.18, it is clear that at higher power, efficiency is decreasing because of the current is increasing that increases the significant amount of conduction losses. The red line shows the efficiency curve of diode rectifier while blue line shows the efficiency of SR which confirm that the SR is capable to enhance the efficiency of the system.

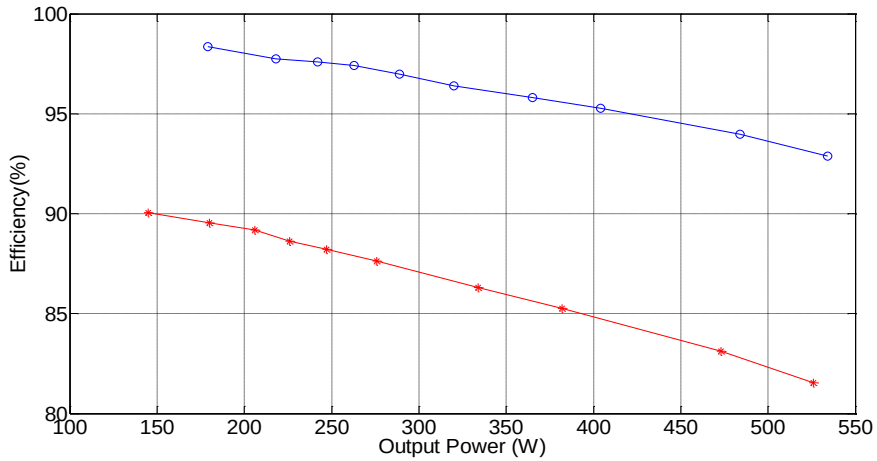


Fig. 8.18 Output power vs. efficiency of diode rectifier (red) and synchronous rectifier (blue)

8.10 Summary

Synchronous Rectifiers give better performance for low output voltage, high output current rectification applications. Ensuring the proper timing of the gate drive signals for the SRs is an important task that must be implemented to make the SR operation effective. The circuit has been simulated with the help of PSIM software and simulation results are presented. A prototype of SR circuit is designed and tested successfully at the line supply. Simulation and experimental results show that the SR is the optimal choice to replace the diode rectifier. Moreover, the SiC devices have a fast switching response that allows to keep the dead time minimum as much as possible that results in improving the efficiency.

Chapter 9

Design Characteristics and Soft-switching Analysis of Isolated DC-DC Converters

9.1 Introduction

In modern electric energy generation, the use of renewable energy sources (RESs) have spread more and more due to the growth of the environment pollution and the shortage of the fossil fuels. The management of the energy produced by RESs requires equipment with new functionalities [64], [65]. The Solid State Transformer (SST) is an emerging equipment that advantageously substitutes for a conventional transformer because of its capabilities of i) conditioning the power flow, whether in DC or AC form, ii) reducing size and weight of a conventional transformer, besides ensuring the input-to-output galvanic isolation and the step up/down of the input voltage [66], [67]. The core of an SST is an isolated DC-DC converter. Many topologies can be used to set up such a converter, differing in circuit complexity, operating characteristics and achievable performance. The isolated DC-DC power converter consists two H-bridges and an interposed transformer. If the both bridges so called input bridge and output bridge are active bridges then it is called dual active bridge (DAB) and the power flows in both the direction, hence it is called dual active bridge isolated bidirectional DC–DC converter [68]-[73]. Instead, if only input bridge is an active bridge then it is called Single Active Bridge (SAB) converter and the power flows only from input bridge to output bridge and hence it is called single active bridge isolated unidirectional DC –DC converter. In DAB converter, the direction of power flow and output voltage is controlled through a phase angle that implemented between two bridges, while in SAB converter the controlling of output voltage decided by the phase angle implemented between two legs of the input bridge.

In both the SAB and DAB converters, the bridge supplied by the DC voltage source (input bridge) is set up with diode-paralleled transistors and executes a DC-AC conversion. The bridge feeding the load (output bridge) is set up again with diode-paralleled transistors for the DAB converter and with diodes for the SAB converter; in both the converters the output bridge executes an AC-DC conversion. The interposed transformer constitutes an AC link connecting the two bridges. Due to the output bridge arrangement, a SAB converter allows for a unidirectional power flow of buck type (apart from the transformer turn ratio) whilst a DAB converter allows for a bidirectional power flow of buck-boost type.

Downstream the output bridge and in parallel to the load, both the converters include a capacitive filter that applies a smooth DC voltage to the load. In turn, upstream the input

bridge both the converters include an inductive-capacitive filter that smoothens the current flowing in the DC voltage source. The bridges operate at high frequency; this consistently shrinks the passive components (transformer, input and output filters) of the SAB and DAB converters so that they stand out for their high values of power density and specific power.

Moreover, recognizing that operation at high-switching frequency of an isolated DC-DC converter is the key to get a compact and light SST, the convenience for its switches to commutate in a soft way is of great importance to improve the SST efficiency. Soft-switching is the technique by which the switching losses of a converter are greatly reduced since the switches are commutated either at zero voltage or at zero current, the relevant technique being termed zero voltage switching (ZVS) and zero current switching (ZCS), respectively [74]-[77]. Soft-switching is commonly achieved by the insertion of additional active and/or passive elements in the converter circuitry.

While soft-switching of a DAB converter is well documented in the literature, soft-switching of a SAB converter has not yet received much attention. Therefore, another focus of this chapter to investigate such an issue by supposing to equip the SAB converter with the same additional elements used for the soft-switching of a DAB converter. They consist of capacitors connected in parallel to the switches as shown in Fig. 9.1, where the switches are made up of a transistor and an in-parallel reverse diode. At the transistor turn-on, ZVS is achieved for it if either the current is flowing through the diode or the capacitor voltage is zero. Instead, at the transistor turn-off, ZVS is achieved for it since the capacitor voltage is zero and, as per design, it is constrained not to increase too much during the transistor turn-off time; note that the ZVS turn-off is obtained irrespectively from the fact that either the transistor or the diode is conducting [78]-[81].

After investigating the soft-switching capabilities of a SAB as well as DAB converters are illustrated and the design procedure to size of the soft-switching capacitors for the SAB converter is presented.

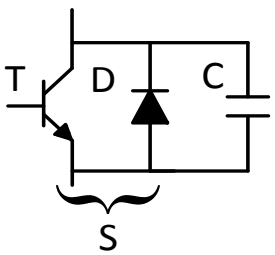


Fig. 9.1 Capacitor-paralleled switch

9.2 Design Analysis

9.2.1 SAB converter

9.2.1.1 Circuit schematic

The circuit diagram of SAB converter is shown in Fig.9.2. The input bridge is set up with the four switches S_1-S_4 whilst the output bridge is set up with the four diodes D_5-D_8. The transformer has the voltage ratio n, hereafter set at 1 for simplicity, and a total leakage inductance L. Then the AC link is represented by the inductance L. The output filter is in cascade to the output bridge and consists of the capacitor C_o. The input filter consists of a LC filter which is not drawn in Fig. 9.2. The load is constituted by the resistance R_L.

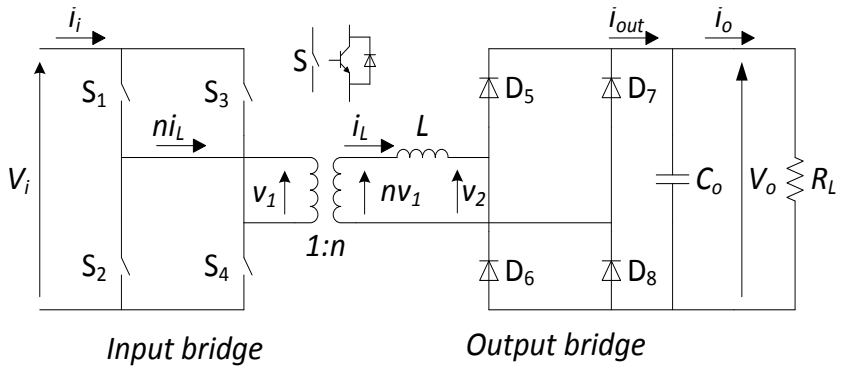


Fig. 9.2 SAB converter circuit schematic

Adjustment of the output voltage V_o is achieved by the control of the phase of the input bridge, with V_o that can not exceed the input voltage V_i.

9.2.1.2 Steady-state operation

A SAB converter can operate in two modes: discontinuous conduction mode (DCM) and continuous conduction mode (CCM) [82]. When all the energy stored in the inductor L in each switching cycle is completely transferred during the turned OFF period of diagonal switches, the current through the diagonal switches at the start of the next ON interval is zero and the circuit operates in DCM. If the stored energy in the inductor is not completely transferred to the output and there is residual energy in the inductor at start of the ON interval of the diagonal switches, the current through the diagonal switches start from a non-zero value and the circuit operates in CCM. DCM and CCM are separated by the so-called boundary mode (BM).

A. Discontinuous conduction mode (DCM)

Figs. 9.3(a)-(c) plot voltages and currents, together with the conducting devices, for a SAB converter operating at steady-state in DCM. From the waveforms shown it comes out

the half-wave symmetry of the operation. The input bridge is commanded over π as follows: at $\theta = 0$, transistors $T_1$and T_4 are turned on; at $\theta = \alpha$, transistor T_4 is turned off and transistor T_3 is turned on. Therefore, the phase angle α plays the role of command variable. The voltage v_1 impressed by the input bridge across the AC link is plotted in Fig. 9.3(a) with solid line.

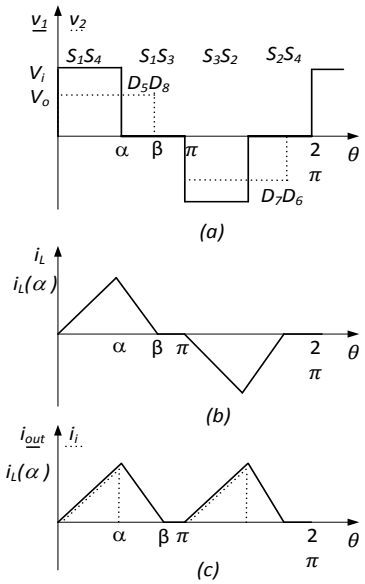


Fig. 9.3 SAB convertercurrent and voltage waveforms in DCM

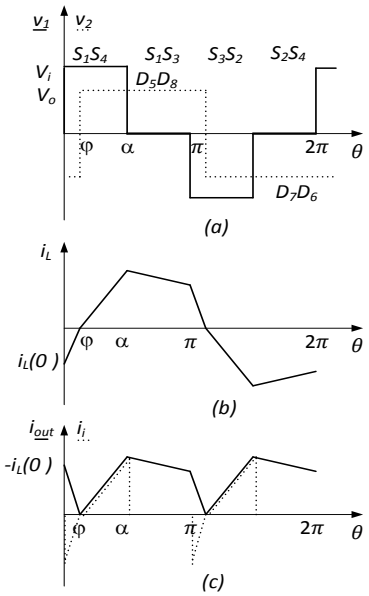


Fig. 9.4 SAB converter current and voltage waveforms in CCM

Until $\theta = \alpha$, the current through the inductance L increases; afterwards it decreases up to vanish at $\theta = \beta$, as shown in Fig. 9.3(b). During the interval from 0 to β diodes D_5 and D_8 conduct and the voltage v_2 impressed by the output bridge across the AC link has the waveform plotted in Fig. 9.3(a) with dotted line.

From the Figs. 9.3(a), (b), and (c), three intervals can be recognized over π, namely $0 - \alpha$, $\alpha - \beta$ and $\beta - \pi$, with different values of voltage (v_1-v_2) applied across the inductance L.

For the steady state operation, the voltage and current can be derived for each interval as follows.

Interval [$0 - \alpha$]

The voltage across the inductor is given by

$$v_L = V_i - V_o \tag{9.1}$$

Then the value of current at $\theta = \alpha$,

$$i_L(\alpha) = \frac{1}{\omega L}(V_i - V_o)\,\alpha \tag{9.2}$$

where ω is the angular frequency.

Interval [$\alpha - \beta$]

The voltage across the inductor is given by

$$v_{\mathrm{L}} = 0 - V_{\mathrm{o}} \tag{9.3}$$

Then the value of current at $\theta = \beta$,

$$\mathrm{i_L}(\beta) = 0 = \frac{1}{\omega \mathrm{L}}(0 - V_{\mathrm{o}})\,(\beta - \alpha) = \frac{V_{\mathrm{o}}}{\omega \mathrm{L}}\,(\alpha - \beta) \tag{9.4}$$

Interval [$\beta - \pi$]

In this interval the inductor current and voltage both are zero.

Rearranging the equation (9.2), the value of current $\mathrm{i_L}$ at $\theta = \alpha$ is equal to

$$\mathrm{i_L}(\alpha) = \frac{\mathrm{V_i}}{\omega \mathrm{L}}\pi(1 - \frac{\mathrm{V_o}}{\mathrm{V_i}})\frac{\alpha}{\pi} \tag{9.5}$$

and the angle where the current vanishes is

$$\frac{\beta}{\pi} = \frac{\mathrm{V_i}}{\mathrm{V_o}}\frac{\alpha}{\pi} \tag{9.6}$$

For SAB to operate in DCM, β must be less than π, which leads to the following condition:

$$\frac{\alpha}{\pi} < \frac{\mathrm{V_o}}{\mathrm{V_i}} \tag{9.7}$$

Because of the capacitor filter, the load current is equal to the average value $\mathrm{I_o}$ of the output current $\mathrm{i_{out}}$, plotted in Fig. 9.3(c) with solid line. Using the equations (9.2) and (9.4), the expression of $\mathrm{I_o}$ is given by

$$\mathrm{I_{o,DCM}} = \frac{\mathrm{V_i}}{\omega \mathrm{L}}\frac{\pi}{2}\frac{\alpha^2}{\pi^2}\left(\frac{\mathrm{V_i}}{\mathrm{V_o}} - 1\right) \tag{9.8}$$

B. Continuous conduction mode (CCM)

Figs. 9.4 (a)-(c) plot voltages and currents, together with the conducting devices, for a SAB converter operating at steady-state in CCM. Most considerations done for DCM can be extended to CCM. The basic difference is that now $\mathrm{i_L}$ is negative in the interval $0 - \varphi$, the latter angle being termed current shift angle. During this interval, diodes $\mathrm{D_7}$ and $\mathrm{D_6}$ of the output bridge conduct, and the voltage $\mathrm{v_2}$ impressed by the output bridge across the AC link is $-\mathrm{V_o}$. From (9.7), the condition for operation in CCM is

$$\frac{\alpha}{\pi} > \frac{\mathrm{V_o}}{\mathrm{V_i}} \tag{9.9}$$

Similarly the equation of inductor voltage and current for the intervals $0 - \varphi$, $\varphi - \alpha$, and $\alpha - \pi$, are calculated as follows

Interval [$0 - \varphi$]

The voltage across the inductor is given by

$$v_L = V_i - (-V_o) = V_i + V_o \tag{9.10}$$

Then the value of current at $\theta = \varphi$,

$$i_L(\varphi) = i_L(0) + \frac{1}{\omega L}(V_i + V_o)\,\alpha \tag{9.11}$$

From Fig. 9.4 (b), it is clear that $i_L$at $\theta = \varphi$ is zero and hence solving the equation (9.11), i_L at $\theta = 0$ is given by,

$$i_L(0) = -\frac{V_i}{\omega L}\frac{\pi}{2}\left(1 + \frac{V_o}{V_i}\right)\left(\frac{\alpha}{\pi} - \frac{V_o}{V_i}\right) \tag{9.12}$$

Interval $[\varphi - \alpha\ ]$

The voltage across the inductor is given by

$$v_L = V_i - V_o \tag{9.13}$$

Then the value of current at $\theta = \alpha$,

$$i_L(\alpha) = 0 + \frac{1}{\omega L}(V_i - V_o)\,(\alpha - \varphi) \tag{9.14}$$

Interval $[\alpha - \pi\ ]$

The voltage across the inductor is given by

$$v_L = 0 - V_o \tag{9.15}$$

Then the value of current at $\theta = \pi$,

$$i_L(\pi) = i_L(\alpha) + \frac{1}{\omega L}(-V_o)\,(\pi - \alpha) \tag{9.16}$$

By exploiting the condition of half-wave symmetry of i_L over π, the values of i_L at $\theta = 0$ and at $\theta = \pi$, are related as

$$i_L(\pi) = -i_L(0) \tag{9.17}$$

Therefore, solving the equations (9.12), (9.14), (9.16) and using the relation given by equation (9.12), the value of current i_L at $\theta = \alpha$ is equal to

$$i_L(\alpha) = \frac{V_i}{\omega L}\frac{\pi}{2}\left(1 - \frac{V_o}{V_i}\right)\left(\frac{\alpha}{\pi} + \frac{V_o}{V_i}\right) \tag{9.18}$$

and the current shift angle is calculated as

$$\varphi = \frac{\pi}{2}\left(\frac{\alpha}{\pi} - \frac{V_o}{V_i}\right) \tag{9.19}$$

The load current is equal to the average value I_o of the output current i_{out}, plotted in Fig. 9.4(c) with solid line. Using the equations (9.12), (9.16), (9.18), and (9.19), the expression of I_o is given by

$$I_{o,CCM} = \frac{V_i}{\omega L}\frac{\pi}{2}\left[\frac{\alpha}{\pi} - \frac{1}{2}\left(\frac{\alpha}{\pi}\right)^2 - \frac{1}{2}\left(\frac{V_o}{V_i}\right)^2\right] \tag{9.20}$$

Eqs. (9.8) and (9.20) show that, in both DCM and CCM, the load current I_o depends on the output voltage V_o, besides on the command variable α.

The relationship between I_o and α is plotted in Fig. 9.5 for different values of V_o, where

here and in the figures of this subsection the dashed traces refer to DCM and the solid ones to CCM. Moreover, the variables in the plots are normalized to the following base values:

$$I_{base} = \frac{V_i}{\omega L}, \quad \alpha_{base} = \pi, \quad V_{base} = V_i \tag{9.21}$$

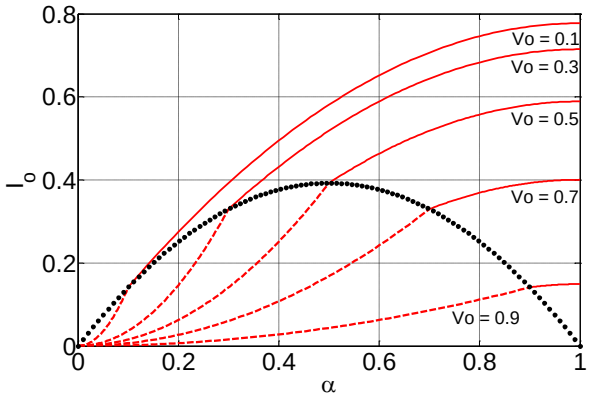


Fig. 9.5 SAB converter load current (I_o) vs. command variable (α)

The traces of Fig. 9.5 outline that, as V_o increases, i) the current deliverable to the load decreases, ii) DCM spans larger intervals of α, and iii) the current regulation in CCM becomes smaller for a fixed value of V_o. BM operation is described by setting $\alpha/\pi=V_o/V_i$ in (9.8) or in (9.20)

$$I_{o,BM} = \frac{V_i}{\omega L}\frac{\pi}{2}\frac{\alpha}{\pi}\left(1-\frac{\alpha}{\pi}\right) \tag{9.22}$$

Eq. (9.11) shows that the locus of BM is a downward concave parabola with the vertex at I_o=0.39, V_o=0.5. The parabola is plotted in Fig. 9.5 with dotted line.

9.2.2 SAB converter characteristics

A. Output current alternating component rms value

The current flowing in the output capacitor C_o coincides with the alternate component of the output current i_{out}. In DCM, the rms value of this component is equal to

$$I_{rms,o,DCM} = \frac{V_i}{\omega L}\sqrt{\frac{1}{3}i_L(\alpha)^2\frac{\beta}{\pi} - I_o^2} \tag{9.23}$$

and in CCM it is equal to

$$I_{rms,o,CCM} = \frac{V_i}{\omega L}\sqrt{\frac{1}{3}\left[\Lambda_{SAB} - \frac{\varphi}{\pi}i_L(\alpha)^2 + \frac{\varphi}{\pi}i_L(0)^2\right] - I_o^2} \tag{9.24}$$

where

$$\Lambda_{SAB} = i_L(\alpha)^2 + i_L(0)^2\left(1-\frac{\alpha}{\pi}\right) - i_L(\alpha)i_L(0)\left(1-\frac{\alpha}{\pi}\right) \tag{9.25}$$

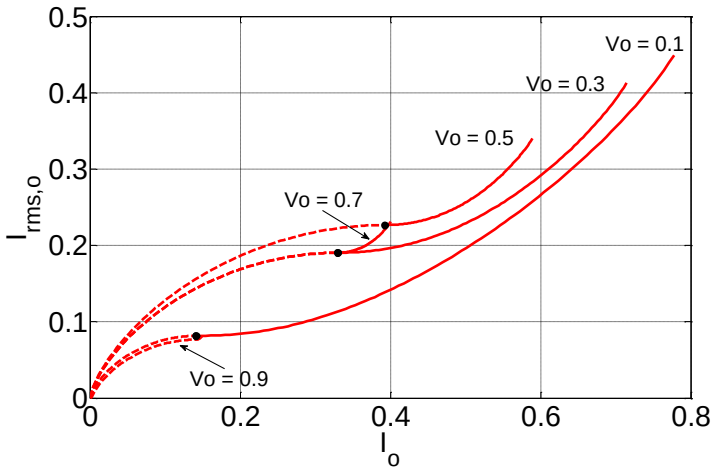


Fig. 9.6 SAB converter rms value of the alternating component of the output current vs. load current

The relationship between $I_{rms,o}$ and I_o is plotted in Fig. 9.6, where here and in the figures of this subsection the dot marks denote operation in BM.

B. Output current ripple

The peak-to-peak ripple R_o of the output current i_{out} is given by $i_L(\alpha)$. Then R_o is equal to (9.5) in DCM

$$\mathrm{R_{o,DCM}} = \frac{\mathrm{V_i}}{\omega \mathrm{L}} \pi \left(1 - \frac{\mathrm{V_o}}{\mathrm{V_i}}\right) \frac{\alpha}{\pi} \tag{9.26}$$

and to (9.18) in CCM

$$\mathrm{R_{o,CCM}} = \frac{\mathrm{V_i}}{\omega \mathrm{L}} \frac{\pi}{2} \left(1 - \frac{\mathrm{V_o}}{\mathrm{V_i}}\right) \left(\frac{\alpha}{\pi} + \frac{\mathrm{V_o}}{\mathrm{V_i}}\right) \tag{9.27}$$

The relationship between R_o and I_o is plotted in Fig. 9.7.

C. Input current average value

By equating the average power at the input of the SAB converter to that one at the output, the average value I_i of the input current can be readily found in

$$\mathrm{I_i} = \frac{\mathrm{V_o}}{\mathrm{V_i}} \mathrm{I_o} \tag{9.28}$$

D. Input current alternating component rms value

In DCM, the rms value of the alternating component of the input current is equal to

$$\mathrm{I_{rms,i,DCM}} = \frac{\mathrm{V_i}}{\omega \mathrm{L}} \sqrt{\frac{1}{3} \mathrm{i_L}(\alpha)^2 \frac{\alpha}{\pi} - \mathrm{I_i^2}} \tag{9.29}$$

and in CCM to

$$\mathrm{I_{rms,i,CCM}} = \frac{\mathrm{V_i}}{\omega \mathrm{L}} \sqrt{\frac{1}{3} \left[\mathrm{i_L}(\alpha)^2 \left(\frac{\alpha}{\pi} - \frac{\varphi}{\pi}\right) + \mathrm{i_L}(0)^2 \frac{\varphi}{\pi} \right] - \mathrm{I_i^2}} \tag{9.30}$$

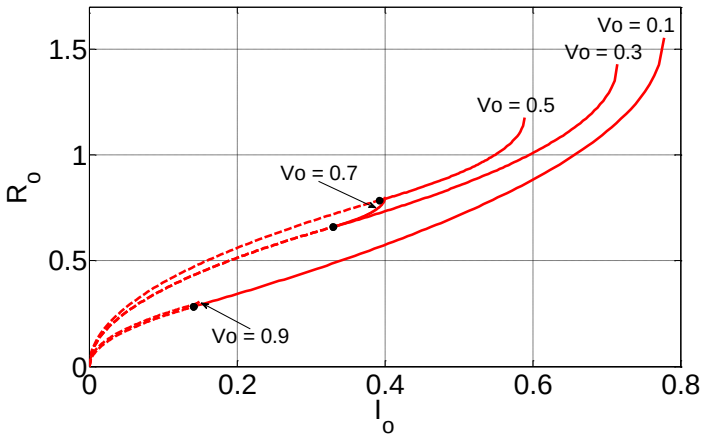


Fig. 9.7 SAB converter output current ripple (R_0) vs. load current (I_0)

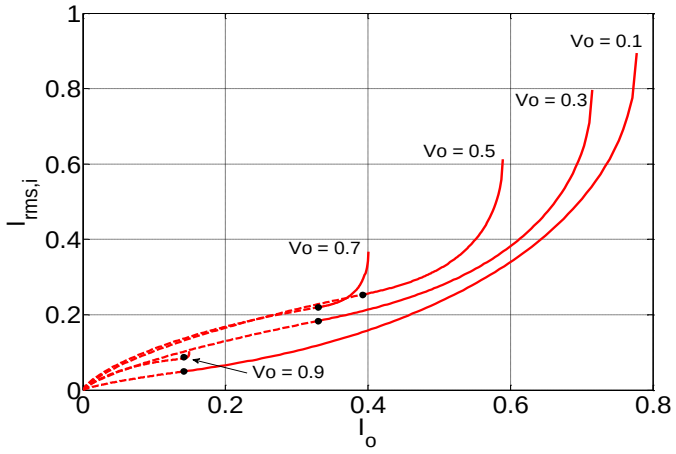


Fig. 9.8 SAB converter rms value of the alternating component of the input current vs. load current

The relationship between $I_{rms,i}$ and I_o is plotted in Fig. 9.8.

E. Input current ripple

The peak-to-peak ripple R_i of the input current is equal to R_o. Then it is still equal to (9.26) in DCM and to (9.27) in CCM, and its plot as a function of I_o is given by Fig. 9.7.

F. Bridge device currents

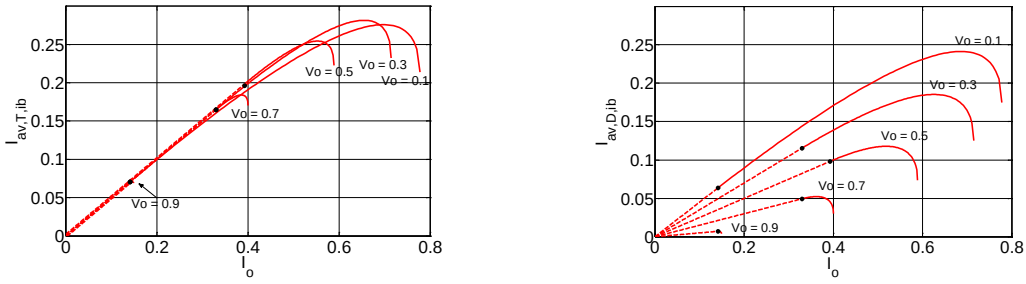
The current is not equally distributed in the devices that constitute the switches of the input bridge. Specifically, the transistors of the leg 1-2 (i.e. T_1 and T_2) and the diodes of the leg 3-4 (i.e. D_3 and D_4) conduct longer than the other devices. Since current sizing is tailored to the most solicited devices, the average and rms values of current are evaluated for them.

In DCM, i_L flows in T_1 from 0 to β, and in D_3 from α to β. In CCM, i_L flows in T_1 from φ to π and in D_3 from α to $\pi+\varphi$. The conduction times of T_2 and D_4 are respectively equal to

those of T_1 and D_3. With regard to the diodes of the output bridge, the current i_L flows in diodes D_5 and D_8 when it is positive and in diodes D_6 and D_7 when it is negative.

G. Device peak currents

The peak current is the same for both the transistors and the diodes of the input bridge ($I_{p,T,ib}$, $I_{p,D,ib}$), and for the diodes ($I_{p,D,ob}$) of the output bridge. Its value is equal to (9.5) in DCM and to (9.18) in CCM, and therefore its plot as a function of I_o is still given by Fig. 9.7.



(a) (b)

Fig. 9.9 SAB converter average current in the (a) transistors of the leg 1-2 and (b) diodes of the leg 3-4 of the input bridge

H. Device average currents

In DCM the average currents in the transistors of the leg 1-2 and in the diodes of the leg 3-4 of the input bridge are respectively equal to

$$I_{av,T,ib,DCM} = \frac{\pi V_i}{4\omega L}\frac{\alpha^2}{\pi^2}\left(\frac{V_i}{V_o} - 1\right) \tag{9.31}$$

$$I_{av,D,ib,DCM} = \frac{V_i}{\omega L}\frac{\pi}{4}\frac{\alpha^2}{\pi^2}\left(1 - \frac{V_o}{V_i}\right)\left(\frac{V_i}{V_o} - 1\right) \tag{9.32}$$

whilst in CCM they are equal to

$$I_{av,T,ib,CCM} = \frac{V_i}{\omega L}\frac{\pi}{16}\left[\left(1 - \frac{V_o}{V_i}\right)\left(\frac{\alpha}{\pi} + \frac{V_o}{V_i}\right)^2 + 4\left(\frac{\alpha}{\pi} - \frac{{V_o}^2}{{V_i}^2}\right)\left(1 - \frac{\alpha}{\pi}\right)\right] \tag{9.33}$$

$$I_{av,D,ib,CCM} = \frac{V_i}{\omega L}\frac{\pi}{16}\left[\left(1 + \frac{V_o}{V_i}\right)\left(\frac{\alpha}{\pi} - \frac{V_o}{V_i}\right)^2 + 4\left(\frac{\alpha}{\pi} - \frac{{V_o}^2}{{V_i}^2}\right)\left(1 - \frac{\alpha}{\pi}\right)\right] \tag{9.34}$$

Eqs. (9.26)-(9.29) are plotted in Fig. 9.9 as a function of I_o.

The average currents in the diodes of the output bridge is simply equal to half of I_o, where I_o is given respectively by (9.8) in DCM and by (9.20) in CCM.

I. Device rms currents

In DCM the rms currents in the transistors of the leg 1-2 and in the diodes of the leg 3-4 of the input bridge are respectively equal to

$$I_{rms,T,ib,DCM} = \frac{V_i}{\omega L}\sqrt{\frac{1}{6} i_L(\alpha)^2 \frac{\beta}{\pi}} \tag{9.35}$$

$$I_{rms,D,ib,DCM} = \frac{V_i}{\omega L}\sqrt{\frac{1}{6} i_L(\alpha)^2 \left(\frac{\beta}{\pi} - \frac{\alpha}{\pi}\right)} \tag{9.36}$$

whilst in CCM they are equal to

$$I_{rms,T,ib,CCM} = \frac{V_i}{\omega L}\sqrt{\frac{1}{6}\left[\Lambda_{SAB} - \frac{\varphi}{\pi} i_L(\alpha)^2\right]} \tag{9.37}$$

$$I_{rms,D,ib,CCM} = \frac{V_i}{\omega L}\sqrt{\frac{1}{6}\left[\Lambda_{SAB} - \frac{\alpha}{\pi} i_L(\alpha)^2 + \frac{\varphi}{\pi} i_L(0)^2\right]} \tag{9.38}$$

Eqs. (9.35)-(9.38) are plotted in Fig. 9.10 as a function of I_o.

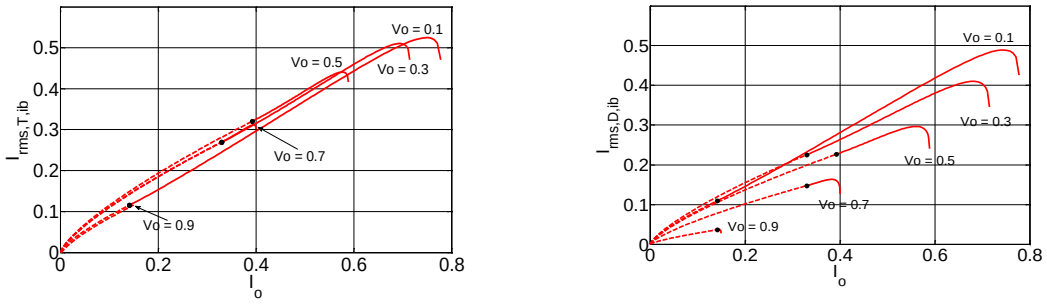


Fig. 9.10 SAB converter rms current in the transistors of the leg 1-2 (left) and in diodes of the leg 3-4 (right) of the input bridge

9.2.3 DAB converter

9.2.3.1 Circuit schematic

The circuit diagram of DAB converter is shown in Fig. 9.11, with the output bridge set up with the four switches S_5-S_8. For the rest, it has the same components as the SAB converter.

Adjustment of the load voltage V_o is achieved by the control of the phase between the two bridges. A DAB converter can support a bidirectional power flow of buck-boost type [81], [83]. Here, however, only operation with input-to-output power flow of buck type is considered to obtain the design characteristics under the same operation as the SAB converter.

9.2.3.2 Steady-state operation

Figs. 9.12(a)-(c) plot voltages and currents, together with the conducting devices, in a DAB converter operating at steady-state [84]-[86]. Fig. 9.12(a) shows that both the bridges impress a square-wave voltage across the AC link and that the two voltages are shifted by the phase angle α, which is the command variable. From the figure it comes out that a DAB converter, unlike the SAB converter, i) operates only in CCM, and ii) has only two intervals

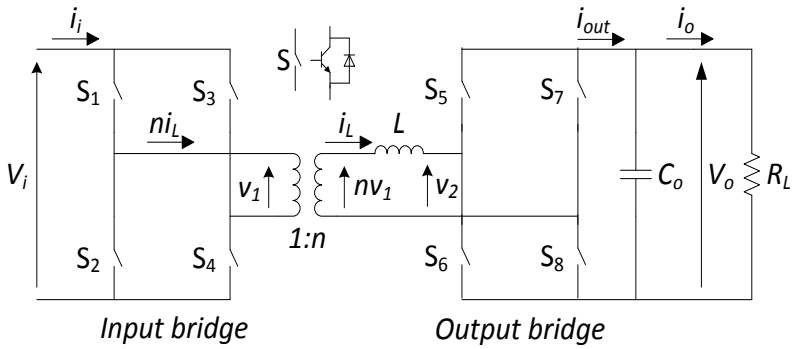


Fig. 9.11 DAB converter circuit schematic

over π with different values of voltage (v_1-v_2) across the inductance L, namely $0-\alpha$ and $\alpha-\pi$. On the other hand, a DAB converter has, like a SAB converter, half-wave symmetry operation.

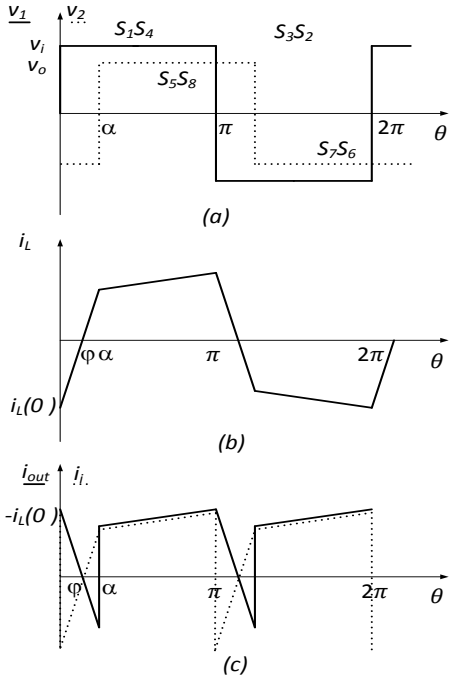


Fig. 9.12 DAB converter current and voltage waveforms

Similarly as SAB converter, by exploiting the condition of half-wave symmetry of i_L over π, the values of i_L at $\theta = 0$ and at $\theta = \alpha$, are calculated in

$$i_L(0) = -\frac{V_i}{\omega L}\frac{\pi}{2}\left[\left(2\frac{\alpha}{\pi}-1\right)\frac{V_o}{V_i}+1\right] \tag{9.39}$$

$$i_L(\alpha) = \frac{V_i}{\omega L}\frac{\pi}{2}\left(2\frac{\alpha}{\pi}-1+\frac{V_o}{V_i}\right) \tag{9.40}$$

Note that $i_L(\alpha)$ is positive for $\alpha>\alpha'$, where $\alpha'$is given by (9.41), and negative in the opposite case.

$$\alpha' = \frac{\pi}{2}\left(1 - \frac{V_o}{V_i}\right) \tag{9.41}$$

The load current I_o, given by the average value of i_{out}, is

$$I_o = \frac{V_i}{\omega L}\pi\frac{\alpha}{\pi}\left(1 - \frac{\alpha}{\pi}\right) \tag{9.42}$$

Eq. (9.42) shows that, unlike the SAB converter, the load current does not depend on the output voltage V_o but only on the command variable α. Regarding the dependence on α, I_o increases with α up to a maximum that is reached for $\alpha = \pi/2$ and then decreases. Therefore, for a statically stable control of the DAB converter, α must be not greater of $\pi/2$. The relationship between I_o and α in the operating range is plotted in Fig. 9.13.

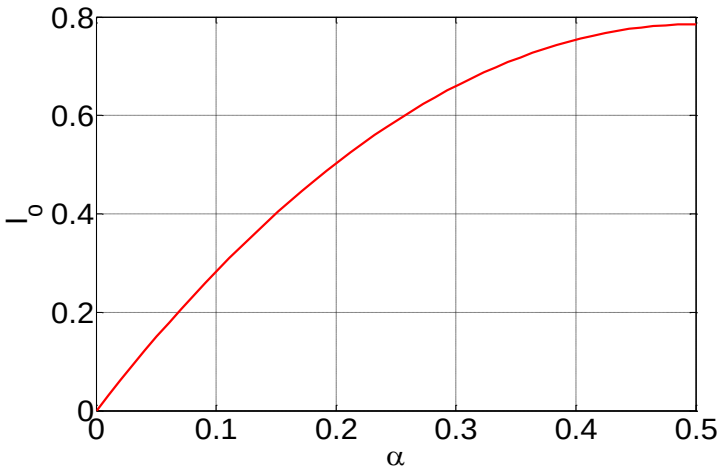


Fig. 9.13 DAB load current vs. command variable

The behavior of a DAB converter is depending on whether α is greater or less than α'. For $\alpha<\alpha'$ the expression of the current shift angle φ is

$$\varphi_{LE} = \pi\left(\frac{1}{2} - \frac{1}{2}\frac{V_o}{V_i} - \frac{\alpha}{\pi}\frac{V_o}{V_i}\right)\left(\frac{1}{1-\frac{V_o}{V_i}}\right) \tag{9.43}$$

whilst for $\alpha<\alpha'$ it is

$$\varphi_{GR} = \pi\left(\frac{1}{2} - \frac{1}{2}\frac{V_o}{V_i} + \frac{\alpha}{\pi}\frac{V_o}{V_i}\right)\left(\frac{1}{1+\frac{V_o}{V_i}}\right) \tag{9.44}$$

Note that the condition $\alpha=\alpha'$corresponds to a load current I_o' given by

$$I_o' = \frac{V_i}{\omega L}\frac{\pi}{4}\left(1 - \frac{{V_o}^2}{{V_i}^2}\right) \tag{9.45}$$

9.2.4 DAB converter characteristics

A. Output current alternating component rms value

For $I_o<I_o'$ the rms value of the alternating component of the output current is equal to

$$I_{rms,o,LE} = \frac{V_i}{\omega L}\sqrt{\frac{1}{3}\left[i_L(\alpha)^2\frac{\varphi_{LE}}{\pi} + i_L(0)^2\left(1-\frac{\varphi_{LE}}{\pi}+\frac{\alpha}{\pi}\right) + i_L(\alpha)i_L(0)\frac{\alpha}{\pi}\right] - I_o^2} \quad (9.46)$$

whilst for $I_o>I_o'$ it is equal to

$$I_{rms,o,GR} = \frac{V_i}{\omega L}\sqrt{\frac{1}{3}\left[i_L(\alpha)^2\left(1-\frac{\varphi_{GR}}{\pi}\right) + i_L(0)^2\left(1+\frac{\varphi_{GR}}{\pi}-\frac{\alpha}{\pi}\right) - i_L(\alpha)i_L(0)\left(1-\frac{\alpha}{\pi}\right)\right] - I_o^2} \quad (9.47)$$

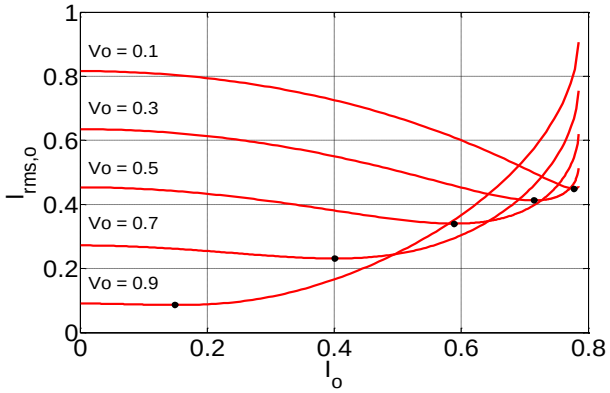


Fig. 9.14 DAB converter rms value of the alternating component of the output current vs. load current

Eqs. (9.46) and (9.47) are plotted in Fig. 9.14 as a function of I_o. In Fig. 9.15 and in the other figures of this Section the dot marks denote operation at $I_o=I_o'$.

B. Output current ripple

The peak-to-peak ripple R_o of the output current i_{out} can be expressed as follows, independently of the value of I_o:

$$R_o = \frac{V_i}{\omega L}\frac{\pi}{2}\left[1+\frac{V_o}{V_i}\left(2\frac{\alpha}{\pi}-1\right)+\left|-1+\frac{V_o}{V_i}+2\frac{\alpha}{\pi}\right|\right] \quad (9.48)$$

Eq. (9.48) is plotted in Fig. 9.15 as a function of I_o. It can be observed that for $I_o<I_o'$ the ripple decreases whilst for $Io>Io'$ it increases.

C. Input current alternating component rms value

For $I_o<I_o'$ the rms value of the alternating component of the input current is equal to

$$I_{rms,i,LE} = \frac{V_i}{\omega L}\sqrt{\frac{1}{6}\left[i_L(\alpha)^2\frac{\varphi_{LE}}{\pi} + i_L(0)^2\left(1+\frac{\alpha}{\pi}-\frac{\varphi_{LE}}{\pi}\right) + i_L(\alpha)i_L(0)\frac{\alpha}{\pi}\right] - I_i^2} \quad (9.49)$$

whilst for $I_o>I_o'$ it is equal to

$$I_{rms,i,GR} = \frac{V_i}{\omega L}\sqrt{\frac{1}{3}\left[i_L(\alpha)^2\left(1-\frac{\varphi_{GR}}{\pi}\right) + i_L(0)^2\left(1-\frac{\alpha}{\pi}+\frac{\varphi_{GR}}{\pi}\right) - i_L(\alpha)i_L(0)\left(1-\frac{\alpha}{\pi}\right)\right] - I_i^2} \quad (9.50)$$

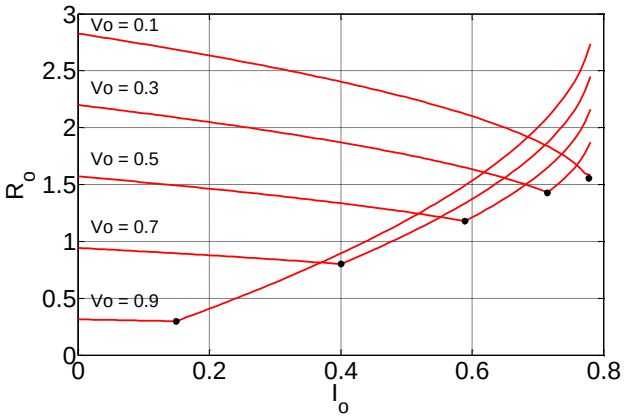


Fig. 9.15 DAB converter output current ripple vs. load current

Equations (9.49) and (9.50) are plotted in Fig. 9.16 as a function of I_o.

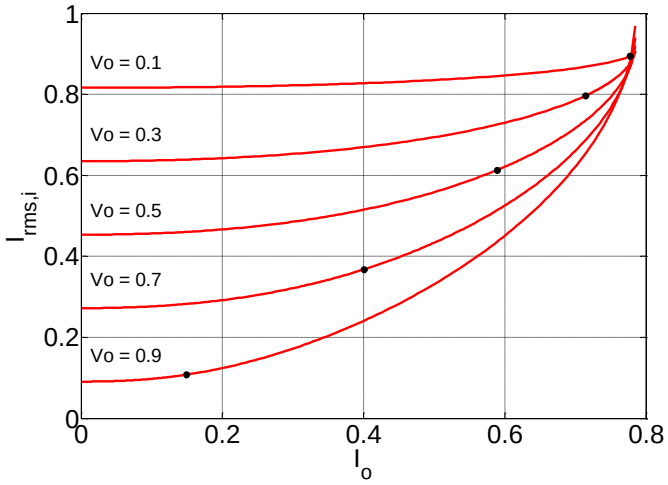


Fig. 9.16 DAB converter rms value of the alternating component of the input current vs. load current

D. Input current: average value and ripple

The same considerations expounded for the SAB converter can be applied to the DAB converter. Then the average value I_i of the input current is still given by (9.28) and its peak-to-peak ripple R_i is equal to R_o in (9.48).

E. Bridge device currents

In a DAB converter, the transistors of each bridge as well as the diodes conduct for an equal time interval. Furthermore, the conduction intervals of the transistors of the input bridge are equal to those of the diodes of the output bridge. The same occurs for the diodes of the input bridge and the transistors of the output bridge. Therefore, the analysis is executed only for transistor T_1 and diode D_1 of the input bridge, where T_1 conducts from φ to π and D_1 from 0 to φ.

F. Device peak currents

The peak current I_p in T_1 is equal to $i_L(\pi)$. Its value, which is the opposite of $i_L(0)$, is plotted in Fig. 9.17 as a function of I_o. The traces show that the peak current increases i) for small values of V_o; indeed, under this condition, the current rises in the interval from α to π, and ii) at high currents, tending to become independent on V_o.

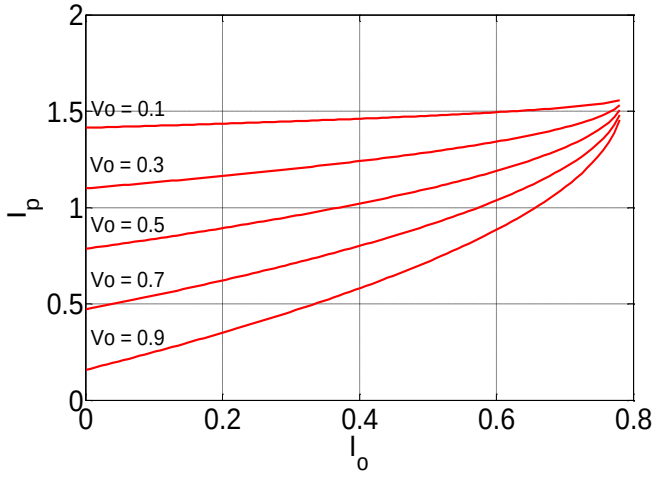


Fig. 9.17 DAB converter device peak current vs. load current

G. Device average currents

For $I_o<I_o$' the average currents in T_1 and D_1 are calculated in

$$I_{av,T,ib,LE} = \frac{V_i}{\omega L}\frac{\pi}{16}\left[1-\frac{V_o}{V_i}\left(1-2\frac{\alpha}{\pi}\right)\right]^2\frac{1}{1-\frac{V_o}{V_i}} \tag{9.51}$$

$$I_{av,D,ib,LE} = \frac{V_i}{\omega L}\frac{\pi}{16}\left\{\left[-1+2\frac{\alpha}{\pi}+\frac{V_o}{V_i}\right]^2\frac{1}{1-\frac{V_o}{V_i}}-4\frac{\alpha}{\pi}\left(1-\frac{\alpha}{\pi}\right)\left(1-\frac{V_o}{V_i}\right)\right\} \tag{9.52}$$

whilst for $I_o>I_o$' they are calculated in

$$I_{av,T,ib,GR} = \frac{V_i}{\omega L}\frac{\pi}{16}\left\{\left[-\left(1-\frac{V_o}{V_i}\right)+2\frac{\alpha}{\pi}\right]^2\frac{1}{1+\frac{V_o}{V_i}}+4\frac{\alpha}{\pi}\left(1-\frac{\alpha}{\pi}\right)\left(1+\frac{V_o}{V_i}\right)\right\} \tag{9.53}$$

$$I_{av,D,ib,GR} = \frac{V_i}{\omega L}\frac{\pi}{16}\left[1-\frac{V_o}{V_i}\left(1-\frac{\alpha}{\pi}\right)\right]^2\frac{1}{1+\frac{V_o}{V_i}} \tag{9.54}$$

Equations (9.51)-(9.54) are plotted in Fig. 9.18 as a function of I_o.

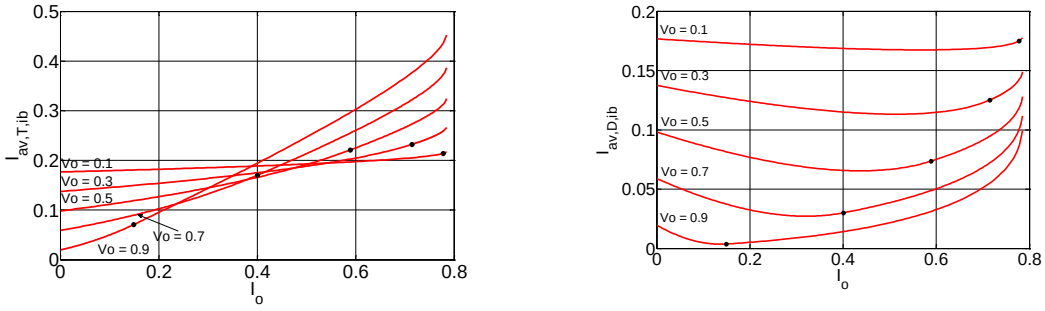


Fig. 9.18 DAB converter average currents in transistors and diodes of the input bridge

H. Device rms currents

For $I_o<I_o'$ the rms currents in T_1 and D_1 are calculated in

$$I_{rms,T,ib,LE} = \frac{V_i}{\omega L}\sqrt{\frac{1}{6}i_L(0)^2\left(1-\frac{\varphi_{LE}}{\pi}\right)} \tag{9.55}$$

$$I_{rms,D,ib,LE} = \frac{V_i}{\omega L}\sqrt{\frac{1}{6}\left[i_L(\alpha)^2\left(\frac{\varphi_{LE}}{\pi}-\frac{\alpha}{\pi}\right)+(i_L(\alpha)^2+i_L(0)^2)\frac{\alpha}{\pi}+i_L(\alpha)i_L(0)\frac{\alpha}{\pi}\right]} \tag{9.56}$$

whilst for $I_o>I_o'$ they are calculated in

$$I_{rms,T,ib,GR} = \frac{V_i}{\omega L}\sqrt{\frac{1}{6}\left[i_L(\alpha)^2\left(\frac{\alpha}{\pi}-\frac{\varphi_{GR}}{\pi}\right)+(i_L(\alpha)^2+i_L(0)^2)\left(1-\frac{\alpha}{\pi}\right)-i_L(\alpha)i_L(0)\left(1-\frac{\alpha}{\pi}\right)\right]} \tag{9.57}$$

$$I_{rms,D,ib,GR} = \frac{V_i}{\omega L}\sqrt{\frac{1}{6}i_L(0)^2\frac{\varphi_{GR}}{\pi}} \tag{9.58}$$

Equations (9.55)-(9.58) are plotted in Fig. 9.19 as a function of I_o. The traces of Figs. 9.18 and 9.19 show that both the average and the rms values of the current in the transistors of the input bridge surpass those of the current in the diode, with the exception at $I_o=0$ where the two currents are equal.

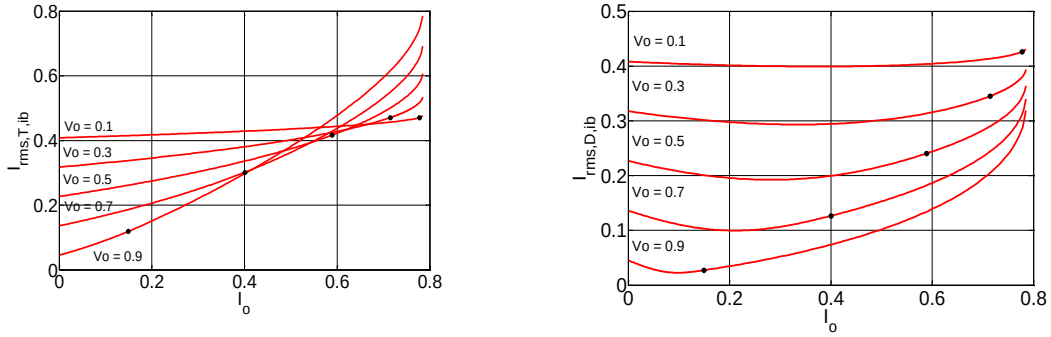


Fig. 9.19 DAB converter rms currents in the transistors and the diodes of the input bridge

9.3 Soft-switching Analysis

9.3.1 DAB converter soft-switching

The circuit diagram of a DAB converter which is shown in Fig. 9.11, is redrawn including the soft-switching capacitors is shown in Fig. 9.20. A DAB converter operates in a continuous conduction mode; then the input and output voltages across the inductance *L* have a square waveform [87],[88]. As discussed in previous section the control variable of a DAB converter is the shift angle α between the commands of the corresponding legs of the two bridges. Waveforms of current and voltage for the DAB converter are drawn in Fig. 9.21(a) and (b).

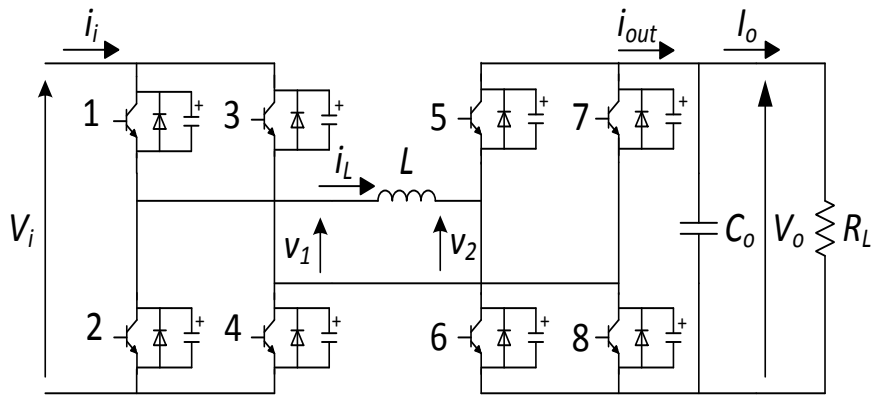


Fig. 9.20 DAB converter circuitry with soft-switching capacitors

At steady-state, the values of the current i_L at $\theta = 0$ and $\theta = \alpha$, are given in equations (9.39) and (9.40) respectively. It is clear from equation (9.39), $i_L(0)$ is always negative while $i_L(\alpha)$ is positive for

$$\frac{\alpha}{\pi} > \frac{1}{2}\left(1 - \frac{V_o}{V_i}\right) \tag{9.59}$$

and negative in the opposite circumstance, giving rise to the two current behaviors drawn in Fig. 9.21 (a) and (b).

The load current I_o, given by the equation (9.42).

9.3.1.1 Input bridge soft-switching

Let us examine the commutations of the input bridge. At $\theta = 0$, T_3 and T_2 are turned off and their commutation is soft thanks to capacitors C_3 and C_2 that are discharged. The commutation is hence of ZVS type. During the dead-time, capacitors C_3 and C_2 charge at V_i while capacitors C_1 and C_4, which at $\theta = 0$ were charged at V_i, discharge. Until their voltage is positive, diodes D_1 and D_4 are off so that the current flows through the in-parallel capacitors C_1 and C_4 according to the scheme of Fig. 9.22(a). As a result, during the dead-time the current flows only in the capacitors and is equally shared by capacitors C_1 and C_4

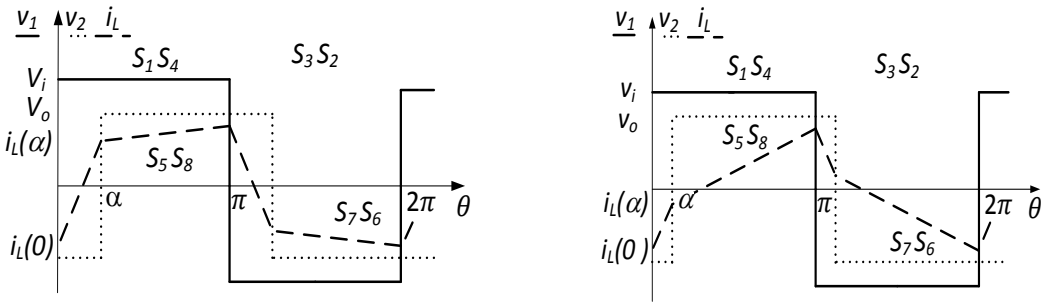


Fig. 9.21 DAB converter current and voltage waveforms: (a) for $i_L(\alpha) > 0$ and (b) for $i_L(\alpha) < 0$

with capacitors C_2 and C_3. Being the dead-time short, the flowing current can be assumed constant and impressed by the inductance L that hence behaves as a current source. The transients of voltage across the capacitors are drawn in Fig. 9.22(b), where T_d is the dead-time. Due to the constant current flowing into the capacitors, the voltage transients are linear. At the end of the dead-time, T_1 and T_4 are turned on and their commutation is also soft because the current i_L is negative and, by flowing into the reverse diodes D_1 and D_4, keeps low the voltage across T_1 and T_4. Hence the commutations at $\theta = 0$ are of ZVS type for all the transistors of the input bridge. The commutations at $\theta = \pi$ occur with the same mechanism as at $\theta = 0$, with the role of switches and capacitors exchanged. Therefore, the input bridge exhibits full soft-switching capabilities. Switching behavior and type of commutation of the transistors of the input bridge of DAB converter are summarized in Table 9.1.

Table 9.1: Input bridge transistors switching behavior and type of commutation

	Turn on		**Turn off**	
θ**=0**	T_1 ZVS	T_4 ZVS	T_3 ZVS	T_2 ZVS
θ**=**π	T_3 ZVS	T_2 ZVS	T_1 ZVS	T_4 ZVS

9.3.1.2 Output bridge soft-switching

Let us first analyze the commutations of the output bridge under the condition $i_L(\alpha) > 0$. At $\theta = \alpha$, T_7 and T_6 are turned off and, at the end of the dead-time, T_5 and T_8 are turned on. Both the commutations are soft since they occur under the same conditions as for the input bridge. An equal situation occurs for the commutations at $\theta = \pi + \alpha$. Therefore the output bridge exhibits soft-switching capabilities for $i_L(\alpha) > 0$. Switching behavior and type of commutation of the transistors of the output bridge of DAB converter for $i_L(\alpha) > 0$, are summarized in Table 9.2 (A).

Let us now analyze the commutations of the output bridge under the condition $i_L(\alpha) < 0$. At $\theta = \alpha$, T_7 and T_6 are turned off and their commutations are still soft thanks to diodes D_7 and D_6. However, during the dead-time, diodes D_7 and D_6 are conducting so that the in-parallel capacitors C_7 and C_6 stay discharged and capacitors C_5 and C_8 do not discharge. Therefore, at the end of the dead-time, T_5 and T_8 are turned on with non-zero voltage across them and their commutation is hard. An equal situation occurs for the commutation at $\theta = \pi + \alpha$. Therefore the output bridge does not exhibit soft-switching for $i_L(\alpha) < 0$. Switching behavior and type of commutation of the transistors of the output bridge for $i_L(\alpha) < 0$, are summarized in Table 9.2 (B).

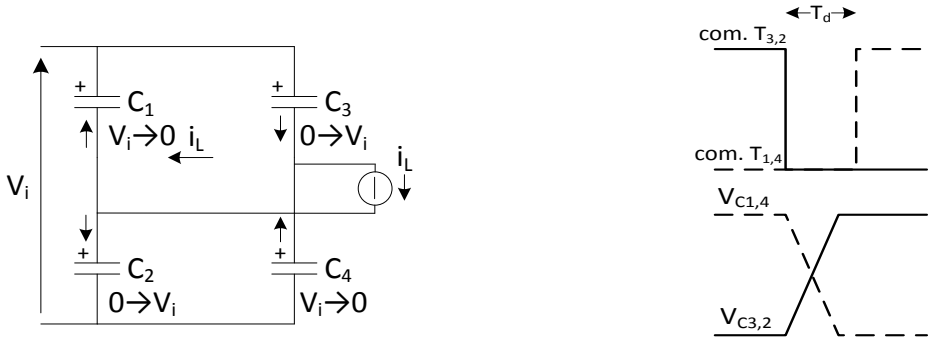
Table 9.2 (A): Output bridge transistors switching behavior and type of commutation for $i_L(\alpha) > 0$.

	Turn on		**Turn off**	
$\theta=\alpha$	T_5 ZVS	T_8 ZVS	T_7 ZVS	T_6 ZVS
$\theta=\pi+\alpha$	T_7 ZVS	T_6 ZVS	T_5 ZVS	T_8 ZVS

Table. 9.2 (B) Output bridge transistors switching behavior and type of commutation for $i_L(\alpha) < 0$.

	Turn on		**Turn off**	
$\theta=\alpha$	T_5 HARD	T_8 HARD	T_6 ZVS	T_7 ZVS
$\theta=\pi+\alpha$	T_6 HARD	T_7 HARD	T_5 ZVS	T_8 ZVS

As a result, it comes out that condition (9.59) must be met to achieve soft-switching for both the bridges of a DAB converter (termed as full soft-switching). Otherwise soft-switching only for the input bridge (termed as partial soft-switching) is achieved. Condition (9.59), expressed in terms of load current, imposes a limit to the output voltage. The limit is shown in Fig. 9.23, where -here and later on- output voltages and currents in the figures are normalized to V_i and $V_i/\omega L$, respectively. According to Fig. 9.23, the limit of the output voltage increases as the output current decreases.



(a) (b)

Fig. 9.22 (a) current flow and (b) voltage transients across the capacitors during the dead-time at $\theta = 0$

9.3.2 SAB converter soft-switching

9.3.2.1 Capacitor insertion in SAB converter

The circuitry of a SAB converter which is drawn in Fig. 9.2, is redrawn including the soft-switching capacitors connected across the transistors is shown in Fig. 9.24. A SAB converter can operate in both discontinuous conduction mode (DCM) and continuous conduction mode (CCM). As discussed before, the control variable of a SAB converter is the shift angle α between the commands of the two legs of the input bridge. Under DCM, both the bridges apply a quasi-square voltage across the inductance L whilst under CCM, the input bridge applies a quasi-square voltage and the output bridge a square voltage. Waveforms of current and voltage for the two operating modes are shown in Figs. 9.3 and 9.4 respectively.

In a SAB converter the soft-switching capacitors can be inserted in the input bridge in two ways. In case#1 the capacitors are inserted only in one leg whilst in case#2 they are

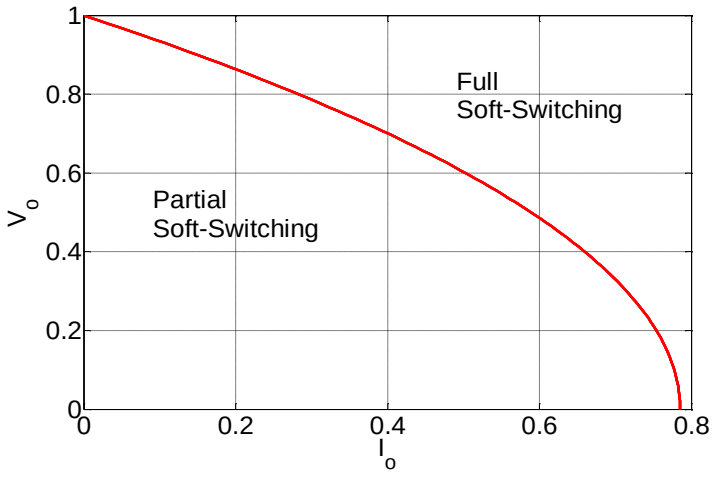


Fig.9.23 DAB converter soft-switching limit

inserted in both the legs. Case#1, in turn, allows for two possibilities, namely cases#1(a), with the capacitors inserted in leg 1-2 that is also called leading leg, and case#1(b), with the capacitors inserted in leg 3-4 (i.e. lagging leg) [89], [90].

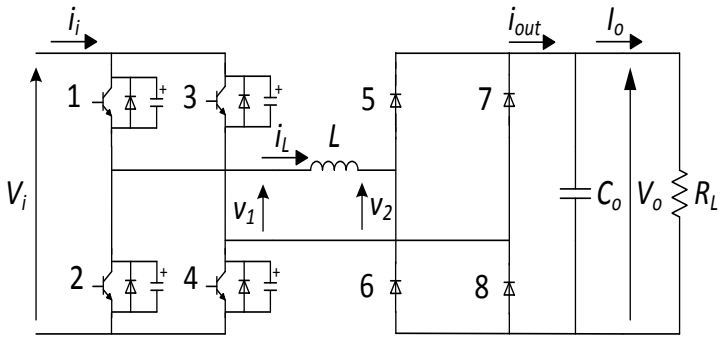


Fig. 9.24 SAB converter circuitry with soft-switching capacitors

9.3.2.2 SAB Converter operation with auxiliaries

A. Discontinuous conduction mode (DCM)

At steady-state the value of the current i_L at $\theta = \alpha$ is given by the equation (9.5) and the condition for SAB converter to operate in DCM is given by the equation (9.7). The load current, given by the average value of i_{out}, is given by the equation (9.8).

Case#1(a)

In this case the capacitors are inserted in parallel to switches S_1 and S_2 as shown in Fig. 9.25. Just before $\theta = 0$, there is no current in the input bridge and T_2 is commanded in the on-state while T_1 is in the off-state. The voltages across capacitors C_1 and C_2 are V_i and 0, respectively. At $\theta = 0$, T_2 is turned off and its commutation is soft of ZCS type because it does not bring any current. At the end of the dead-time, capacitor C_1 is still charged and the turn-on of T_1 short-circuits it, giving rise to an unacceptable pulse of current trough T_1. The same problem occurs at $\theta = \pi$ for T_2. Hence, the insertion of capacitors in leg 1-2 to achieve soft-switching is not feasible.

Case#1(b)

In this case the capacitors are inserted in parallel to switches S_3 and S_4 as shown in Fig 9.26. At $\theta = 0$, the same situation as in case#1(a) occurs for T_2 and then its commutation is soft. At the expiration of the dead-time, T_1 is turned on and its commutation is hard since a voltage of half of V_i is dropping across it, under the assumption that the supply voltage solicits each switch of the leg in an equal way. At $\theta = \alpha$, T_4 is turned off and its commutation is soft of ZVS type thanks to capacitor C_4 that is discharged at that time. During the dead-time, like for a DAB converter, capacitor C_4 charges at V_i while capacitor C_3, which was charged at V_i at $\theta = \alpha$, discharges. At the expiration of the dead-time, T_3 is turned on and its commutation is soft because the current flows in the diode D_3. Current flow and variations of voltage across

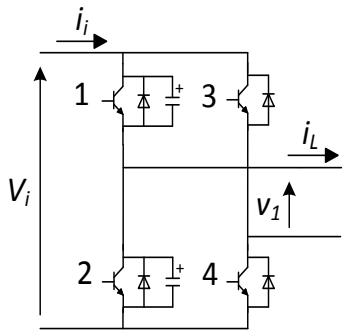


Fig. 9.25 Capacitor connection case #1(a)

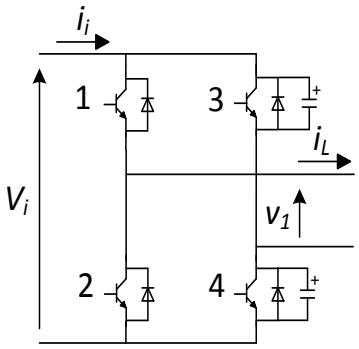
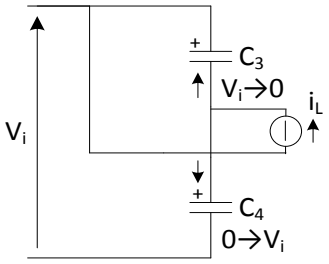
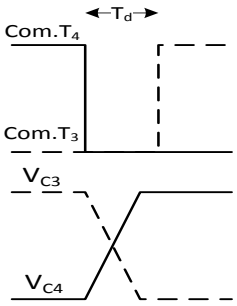


Fig. 9.26. Capacitor connection case #1(b)

the capacitors are shown in Figs. 9.27(a) and (b). The commutations at $\theta = \pi$ and at $\theta = \pi + \alpha$ occur with the same mechanism as at $\theta = 0$ and at $\theta = \alpha$.



(a)



(b)

Fig. 9.27 (a) current flow and (b) voltage transients across the capacitors during the dead-time at $\theta = \alpha$

Case#2

In this case the capacitors are inserted in parallel to each switch as shown in Fig. 9.28. The situation at $\theta = 0$ is identical to case#1(a). Turn-off of T_2 is soft of ZCS type but the successive turn-on of T_1 produces an unacceptable pulse of current through it due to the

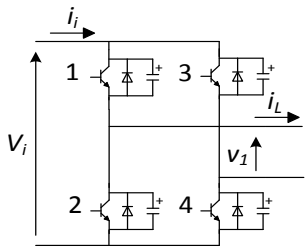


Fig. 9.28 Capacitor connection case #2

discharge of C_1. The same problem occurs at $\theta = \pi$ for T_2. Hence, the insertion of capacitors in parallel to each switch is not feasible.

As a result, soft-switching of a SAB converter operating in DCM is obtained only with the insertion of capacitors in leg 3-4; furthermore, only partial soft-switching is achieved as only the switches in the leg endowed with the capacitors experience soft commutations at both turn-on and turn-off. Transistor switching and their type of commutation are summarized in Tab. 9.3.

Table 9.3: DCM switching for case#1(b)

	θ=0	θ=α	θ=π	θ=π+α
Turn on	T_1 HARD	T_3 ZVS	T_2 HARD	T_4 ZVS
Turn off	T_2 ZCS	T_4 ZVS	T_1 ZCS	T_3 ZVS

B. Continuous conduction mode (CCM)

At steady-state the values of the current i_L at $\theta = 0$ and at $\theta = \alpha$ are given by the equations (9.12) and (9.18) respectively. The load current, given by the average value of i_{out}, is given by the equation (9.20).

As like in DCM- I_o depends on the output voltage, besides on the control variable. Maximum load current is obtained with $\alpha=\pi$; its plot as a function of the output voltage is shown in Fig. 9.29 by the line marked with stars.

Table 9.4: CCM switching for case#1(a)

	θ=0	θ=α	θ=π	θ=π+α
Turn on	T_1 ZVS	T_3 ZVS	T_2 ZVS	T_4 ZVS
Turn off	T_2 ZVS	T_4 HARD	T_1 ZVS	T_3 HARD

Case#1(a)

In this case the capacitors are inserted in parallel to the switches S_1 and S_2. At $\theta = 0$, T_2 is turned off and its switching is soft thanks to capacitor C_2 that is discharged. At the expiration of the dead-time, T_1 is turned on and its switching is soft because current flows in the reverse diode D_1. At $\theta = \alpha$, T_4 is turned off and its switching is hard because the voltage across it jumps to V_i while the current is still flowing through it. At the expiration of the

dead-time, T_3 is turned on and its switching is soft because the current flows in the reverse diode D_3. The commutations at $\theta = \pi$ and at $\theta = \pi + \alpha$ occur with the same mechanism as at $\theta = 0$ and at $\theta = \alpha$. Hence, the insertion of capacitors in leg 1-2 allows for a soft turn-on of all the switches but not for a soft turn-off of T_3 and T_4. Transistor switching and their type of commutation are summarized in Tab. 9.4.

Case#1(b)

In this case the capacitors are inserted in parallel to the switches S_3 and S_4. By duality with respect to Case#1(a), it turns out that the insertion of capacitors in leg 3-4 allows for a soft turn-on of all the switches but not for a soft turn-off of T_1 and T_2. Transistor commutations and their type of switching are summarized in Tab. 9.5.

Table 9.5: CCM switching for case#1(b)

	$\theta=0$	$\theta=\alpha$	$\theta=\pi$	$\theta=\pi+\alpha$
Turn on	T_1 ZVS	T_3 ZVS	T_2 ZVS	T_4 ZVS
Turn off	T_2 HARD	T_4 ZVS	T_1 HARD	T_3 ZVS

Case#2

In this case the capacitors are inserted in parallel to each switch. At $\theta = 0$, T_2 is turned off and its switching is soft thanks to the capacitor C_2. At the expiration of the dead-time, T_1 is turned on and its switching is soft because the current flows in the reverse diode D_1. At $\theta = \alpha$, T_4 is turned off and its switching is soft thanks to capacitor C_4. At the expiration of the dead-time, T_3 is turned on and its switching is soft because the current flows in the reverse diode D_3. The commutations at $\theta = \pi$ and at $\theta = \pi + \alpha$ occur with the same mechanism as at $\theta = 0$ and at $\theta = \alpha$. Hence, the insertion of the capacitors in parallel to each switch ensures full soft-switching capabilities as in a DAB converter. Transistor commutations and their type of switching for this case are summarized in Tab. 9.6.

Table 9.6: CCM switching for case#2

	$\theta=0$	$\theta=\alpha$	$\theta=\pi$	$\theta=\pi+\alpha$
Turn on	T_1 ZVS	T_3 ZVS	T_2 ZVS	T_4 ZVS
Turn off	T_2 ZVS	T_4 ZVS	T_1 ZVS	T_3 ZVS

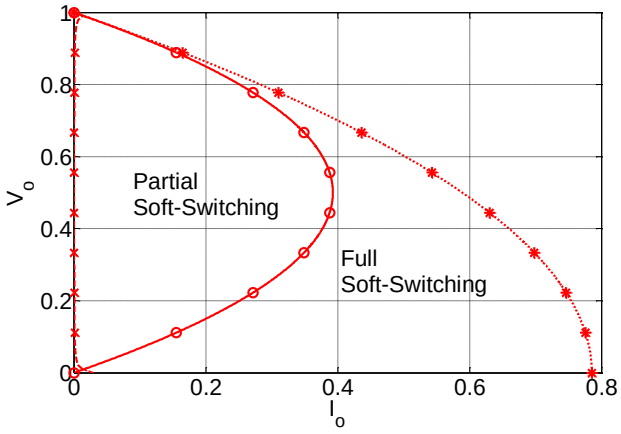


Fig. 9.29 SAB converter soft switching limits

As a result, soft-switching of a SAB converter operating in CCM is obtained whether the capacitors are inserted in one leg or in both the legs. However, in the first case the SAB converter exhibits partial soft-switching capabilities whilst in the second case it exhibits full soft-switching capabilities.

Conclusive remarks

Putting together the results of the above investigation for both the DCM and the CCM operation of a SAB converter, it emerges that, to achieve full soft-switching, the condition (9.7) must be never met. Such a condition, substituted in (9.8) or in (9.18), imposes a limit to the output current for a given value of the output voltage. The limit is shown in Fig. 9.29 by the line marked with rounds. Differently from a DAB converter, here the output current limit takes a maximum for an intermediate value of the output voltage and decreases both at high and low output voltages.

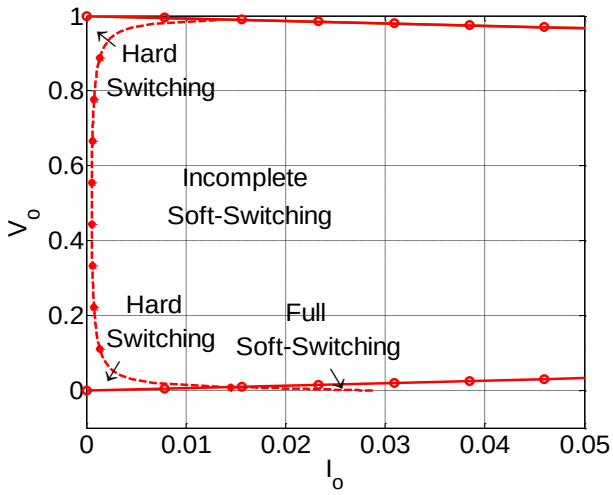


Fig. 9.30 Magnification of SAB converter soft switching limits near Io=0

Fig. 9.30 shows magnification of the limits near I_o=0. In figure it is clearly shows that there is a lower limit of current below that soft switching is not possible anymore.

9.3.2.3 Soft-switching capacitor design

When soft-switching is feasible, it requires that the voltage across the capacitors changes of V_i in a time interval that goes from at_{off}, where a is factor >1 and t_{off} is the transistor turn-off time, up to the dead-time T_d; the factor a guarantees that the increase of voltage across the transistor during its turn-off is a fraction of V_i (i.e. it is V_i/a under a linear voltage transient). Let us denote with T_s the time interval taken by the capacitor voltage to change of V_i. For both the capacitor voltage transients of Fig. 9.22(b) and 9.27(b), the current i_L divides into two equal parts when entering into the capacitors. For a current i_L enough high, as it occurs at $\theta = \alpha$, the current can be assumed constant during the voltage transients and the relationship between the capacitor value, i_L and T_s is

$$V_i C = \frac{i_L T_s}{2} \tag{9.60}$$

A quite different situation arises when i_L is small as it occurs at $\theta = 0$, when the CCM operation approaches the DCM one. In this situation, a more accurate relationship between the capacitor value, i_L and T_s can be obtained by assuming for i_L a linear behavior during T_s, leading to

$$V_i C = \frac{i_L T_s}{4} \tag{9.61}$$

Let us now select a capacitor in order that for the maximum value of $i_{L,max}$ the commutation takes place in at_{off}, where a is set at 3. Then

$$C = \frac{i_{L,max}\, 3\, t_{off}}{2V_i} \tag{9.62}$$

By imposing that the commutation completes within the dead-time, (9.61) yields a minimum value $i_{L,min}$ of the current $i_L(\alpha)$ for a SAB converter to commutate softly, given by

$$i_{L,min} = \frac{i_{L,max} 3 t_{off}}{2T_d} \tag{9.63}$$

Eq. (9.63) restricts even more the soft-switching zone of a SAB converter.

9.4 Converter Application

The study case is a portable power supply of 3.3 kW, intended to charge the battery (pack) of an electric city-car. The battery is made of 13 in-series lithium-ion batteries, each of them with a nominal voltage of 3.7 V and a capacity of 100 A·h. The power supply is fed by a single-phase 230 V line and includes a PFC rectifier with an output voltage of 355 V. The block scheme of the power supply is drawn in Fig. 9.31, where PFC is a power factor controlled rectifier and L_f decouples the output capacitor of the isolated DC-DC converter from the battery. A transformer with turn ratio of 5.5:1 is selected to adapt the input voltage to the rated output voltage. The use of SiC MOSFETs (C2M0080120D manufactured by Cree) is planned for the isolated DC-DC converter to reduce even more the switching losses.

They have drain-source voltage of 1200 V, continuous drain current of 36 A, and turn-on and -off times of 35 ns and 50 ns, respectively. Data on the isolated DC-DC converter and the battery are summarized in Table 9.7, where the subscript r stays for "referred to the primary".

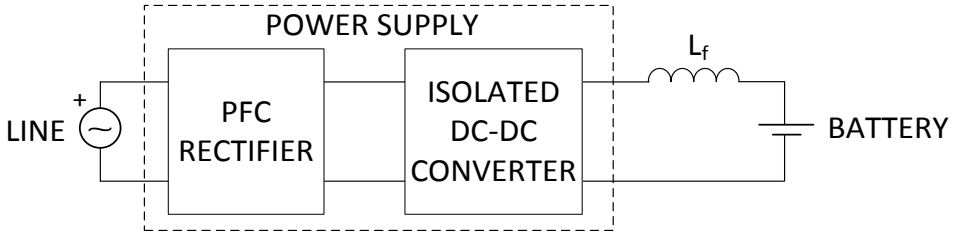


Fig. 9.31 Power supply scheme

At first, the usage of the SAB converter is analyzed. Let current $I_{r,oR}$ and voltage $V_{r,oR}$ be reached when $\alpha = \pi$; from (9.18), the inductance L results in 30 μH, which is a value compatible with the leakage inductance of the commercially available high-frequency transformers. At $\alpha = \pi$, the maximum value of i_L, given by (9.14), is equal to 20 A so that, from (9.62), soft-switching capacitors result in 4.2 nF.

During the constant current stage of the charging process, the output voltage of the SAB converter ranges from $V_{r,m}$ to $V_{r,M}$ while the output current is regulated to $I_{r,N}$. By substituting these values in (9.8) to work out α and then by means of (9.7), it comes out that the SAB converter operates in DCM along all the constant current stage. Therefore, it experiences only incomplete soft-switching, with the capacitors inserted in the lagging leg according to the analysis discussed in the previous Section.

During the constant voltage stage of the charging process, the output voltage is equal to $V_{r,M}$ while the output current is gradually reduced to the cut-off current $I_{r,C}$. Also in this case it comes out by using (9.8) and (9.7) that the SAB converter operates in DCM along all the constant voltage stage.

The minimum value of $I_{o,m}$ enabling incomplete soft-switching has been computed as a function of V_o by (9.14), (9.62) and (9.63). The relevant relationship, shown in Fig. 9.29 by the line marked with crosses, is magnified in Fig. 9.30. Note that for currents less than $I_{o,m}$ the commutations get back to be hard. When $V_{r,o}$ is regulated at $V_{r,M}$, the value of $I_{o,m}$ results in 1.5 A. Since this value is less than $I_{r,C}$, T_3 and T_4 commutate softly during all the charging process.

A DAB converter is considered, endowed with the same transformer. It operates with α=0.1 during the constant current stage of the charging process, as it is derived from (9.42); in this condition, (9.59) is not fulfilled so that the DAB converter experiences partial soft-

Table 9.7: Isolated dc-dc converter and battery data

	Quantity	Primary	Secondary
Isolated DC-DC converter	Input voltage	Vi=355 V	
	Rated output voltage	Vr,oR=330 V	VoR=60 V
	Rated output current	Ir,oR 10 A	IoR=55 A
	Switching frequency	20 kHz	
	Rated output power	3.3 kW	
	Turn-off time	toff=50 ns	
	Dead time	Td=1 μs	
Battery			
	Maximum voltage VM	Vr,M=297 V	VM=54 V
	Minimum voltage Vm	Vr,m=214 V	Vm=39 V
	Nominal charging current	Ir,N=9.1 A	IN=50 A
	Cut-off current	Ir,C=1.8 A	IC=10 A

switching. The same occurs during the constant voltage stage. Of course, also in the DAB converter the reduction of the partial soft-switching zone due to condition (9.63) has to be accounted for.

Fig. 9.32 shows the battery charging profile, where it clearly shows that in the starting of battery charging the constant current and variable voltage profile required while after reaching the battery voltage at maximum value charging profile must follow the constant voltage and variable current.

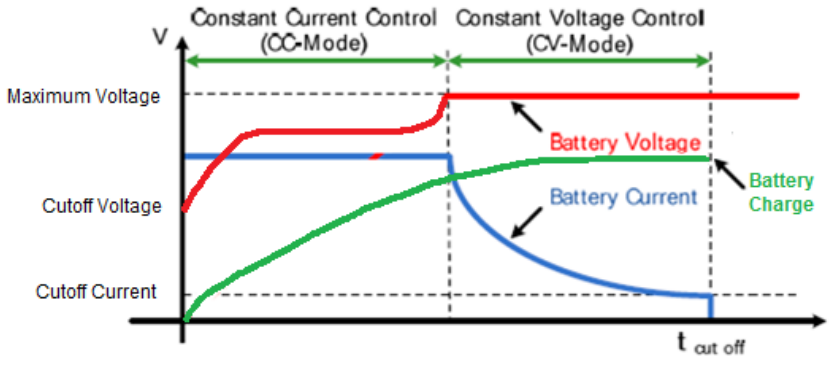
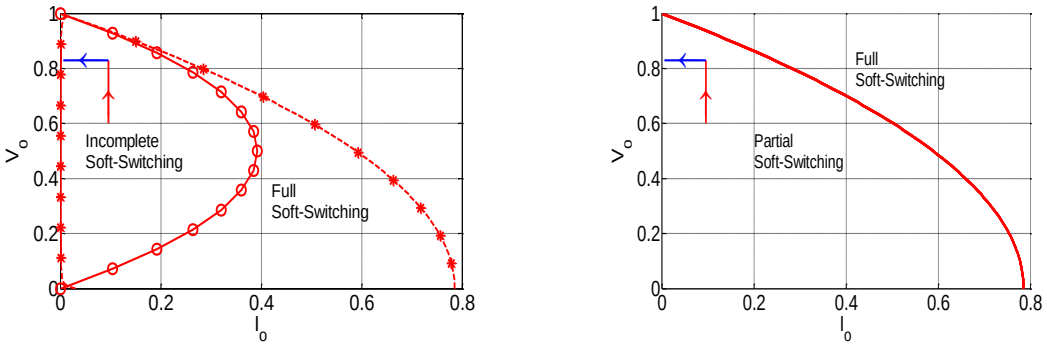


Fig. 9.32 Battery Charging Profile

The charging locus of vehicle battery through the SAB and DAB converters are shown in Figs. 9.33(a) and 9.33(b) respectively. In both the charging profiles, red solid line with arrow

is indicates the constant current and voltage increasing. Once battery voltage reached at maximum value, current start decreasing and voltage stays constant as shown by blue line with arrow.



(a) SAB Converter (b) DAB converter

Fig. 9.33 Locus of the battery charging

9.5 Summary

The design characteristics of both the SAB converter and DAB converter under unidirectional power flow of buck type have been considered. The following characteristics have been derived as a function of the load current and voltage along the operation range: i) peak-to-peak ripple and rms value of the alternate component of the output and input current, and ii) peak, average and rms values of the current flowing in the devices of the converter. The design characteristics give proper idea in the sizing of the output and input filters of the converters and to select the current ratings of the devices.

Moreover, the soft switching analysis of SAB and DAB converters have illustrated in this chapter. Soft switching of DAB converter with forward power flow of buck type only is considered because this investigation is introductory to that one of the SAB converters. The soft switching analysis of SAB converter is explain in details. The conditions for soft-switching has been established under both DCM and CCM operation for the SAB converter. It has been found that, while in CCM full soft-switching is achievable, in DCM only partial soft-switching exists: it is obtained by paralleling the switches of a specific leg of the input bridge with a capacitor. Sizing of the capacitors as well as its impact on the restriction of the soft-switching zone has been evaluated.

Chapter 10

Conclusion and Future Work

Conclusion

Power converters for vehicular applications have been analyzed and designed. To optimize the efficiency of power converters, the power losses have been investigated in details. The major power loss components: switching losses and conduction losses are minimized either replacing the new generation devices that are based on wide band gap semiconductor materials (i.e. SiC and GaN) and/or using the soft switching techniques during commutation. Electrical properties and characteristics of SiC and GaN materials as well as the devices based on these materials have been discussed in details. The loss models of switching devices (i.e. diode, IGBT, and MOSFET) are formulated that are used in various power converters, required for vehicular application.

To evaluate the performance of the SiC devices in electric vehicle applications, two versions of traction inverters of a compact C-class electric car: one is built with the Silicon IGBTs while other one is built with the same rating of SiC MOSFETs are analyzed. The loss amount has been calculated for the two inverter types when the electric car is driven along the NEDC cycle and results are compared. The compared result shows that the usage of the SiC MOSFETs reduces the losses in the traction inverter of about 5%, yielding an equal increase in the car range. In addition, the work is extended for the calculation of inverter and combined drive train efficiency for the steady state conditions along the torque and speed of the traction motor. The efficiency of Si-IGBT inverter has been validated by the data collected from a commercial electric car of C-class thus indirectly validating the SiC MOSFETs model as well.

A power factor correction (PFC) circuit with the interleaved arrangement of two boost converters connected in parallel is analyzed. The detail analyses of circuit operation and simulation results are presented. A prototype of PFC circuit is designed and the design procedure is discussed in details.

A Synchronous Rectifier (SR) circuit is designed with four active switches to rectify the secondary coil AC voltage of the wireless power transfer (WPT) systems. The circuit operation is discussed and simulation results are presented. The simulation results are validated by the experimental data taken at line frequency and same is expected for the high frequency operation in the WPT systems.

Finally, a detail analysis of the Isolated DC-DC converter using Single Active Bridge (SAB) as well as Dual Active Bridge (DAB) has been discussed. The analysis is started with

the characteristics of SAB and DAB converters for the different operating conditions and at last, soft switching operation for both versions of converters is analyzed.

Future Work

Based on the research works carried out in this thesis on the high-efficiency power converters for vehicular applications, possible subjects for further future investigations can be as follows.

Technology of GaN devices is rapidly advancing with an improvement of their characteristics, especially the operating voltage. It is expected that in the near future, due to the overall better performance of GaN over SiC devices, the GaN devices are going to be largely applied in high-efficiency power converters, in particular when they operate at very high frequency. Then, a proper loss model for GaN devices should be arranged and the efficiency of the electric car propulsion drive should be re-calculated. Comparison with the results obtained in the present work by using the SiC devices is surely of interest.

More detailed power loss analysis in SAB and DAB power converters should be executed when they commutate in both soft-switching and hard-switching way. Comparison of the results over the operation zones of the two types of power converters could lead to a thought-out selection between the twos for a given application, of course in the case that both meet the functional specifications of the application.

A prototype of SAB power converter should be set up and experimented to verify the simulation results obtained in the present work. Proper in-situ tuning of all the components of the circuitry, including the auxiliary capacitors used to achieve soft-switching, could be required as well as a careful layout of them on account of high-frequency operation of the converter.

An analysis of multiport DC/DC isolated power converters based on SAB/DAB converter topologies should be executed as nowadays they are gaining momentum not only in vehicular applications but also in industry and home appliances. Indeed, there is an increasing demand of integrating renewable energy sources and storage devices of various types with both the loads and the grid through safely connections, f.i. to supply the loads with the renewable energy sources and/or the storage devices when the grid is failing (islanding conditions). This motivates a substantial research in multiport isolated power converters devoted to optimize the exploitation of sources and devices, and to properly regulate the power delivery to loads.

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