## A GPU-ACCELERATED ADAPTIVE FSAI PRECONDITIONER FOR MASSIVELY PARALLEL SIMULATIONS

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**Abstract.** The solution of linear systems of equations is a central task in a number of scientific and engineering applications. In many cases the solution of linear systems may take most of the simulation time thus representing a major bottleneck in the further development of scientific and technical software. For large scale simulations, nowadays accounting for several millions or even billions of unknowns, it is quite common to resort to preconditioned iterative solvers for exploiting their low memory requirements and, at least potential, parallelism. Approximate inverses have been shown to be robust and effective preconditioners in various contexts. In this work, we show how adaptive FSAI, an approximate inverse characterized by a very high degree of parallelism, can be successfully implemented on a distributed memory computer equipped with GPU accelerators. Taking advantage of GPUs in adaptive FSAI set-up is not a trivial task, nevertheless we show through an extensive numerical experimentation how the proposed approach outperforms more traditional preconditioners and results in a close-to-ideal behaviour in challenging linear algebra problems.

## Keywords: Linear Algebra, Preconditioning, GPUs, CUDA, MPI

1. Introduction. The request for accurate and reliable numerical simulations of complex phenomena is growing exponentially across a wide range of scientific and engineering applications. In the automotive, aerospace or in the oil&gas industry, the use of very large computational grids is a common practice to faithfully reproduce intricate geometries and guarantee a high precision level. The size of the problems can easily reach several hundreds or even thousands of millions of unknowns up to the point that High Performance Computing (HPC) becomes a necessity. Despite of the differences in the problem at hand, there is always the need to discretize the underlying Partial Differential Equations (PDEs) to approximate the continuous problem in an algebraic system of equations whose solution is obtained numerically. In large scale simulations, the solution of linear systems of equations is often, by far, the most expensive part in terms of computational resources of the entire simulation process, taking ofen more than 90% of the total time.

The design and implementation of numerical software for the solution to large scale linear systems on massively parallel computers is not straightforward and often requires several personyears of development and testing to get a reliable code with satisfactory performance. For many years now, US national labs have been provided the scientific community with open source software for the solution of linear (and non-linear) systems of equations on distributed memory systems [2, 12, 33]. Parallelism in these packages is exploited mainly through MPI implementing suitable Krylov subspace methods preconditioned by Algebraic Multigrid [34] (AMG) techniques. It has been shown in a number of pubblications that, provided a large enough problem, the resulting codes may scale up to several thousands of CPU cores.

However, in recent years scientific computing is undergoing a major evolution. Due to the end of the golden age ruled by Moore's law, traditional multi-core CPU are, by now, supported by many-core accelerators featuring thousands of simple computing cores. This change is clearly reflected in the Top 500 ranking [32] where the first positions are occupied by systems equipped with many-core accelerators. In particular, Graphics Processing Units, devices originally proposed for their efficiency at manipulating computer graphics and image processing, are increasingly employed in general purpose numerical computing applications.

Adapting well-established software solutions, originally designed for traditional CPUs, to the use of accelerators may be not an easy task up to the point of requiring a complete rethinking of the whole implementation. First attempts to port linear solvers to the GPU hardware were based on a simple straightforward approach [24, 25]. More recently, also some AMG based solvers entirely running on a single or multiple GPUs have been proposed exhibiting a very good performance on classic linear algebra problems [3, 14, 30, 9]. However, in challenging real world problems such as those arising from structural mechanics or fluid flow in highly

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heterogeneous formations, standard AMG solvers may be slow to converge or even fail, so that more advanced approaches are needed. In particular, the use of powerful smoothers based on approximate inverses can be of great help as shown, for instance, in [31, 13].

Approximate inverse preconditioners have been thoroughly investigated in the end of the last century by several authors [5, 15, 11]. Their main advantage with respect to other preconditioners is their practically ideal suitability for being applied in parallel as they involve only sparse matrix-by-vector products. Parallel processing is more difficult to exploit in the set-up stage, but there are several approximate inverse variants able to perform well even on parallel computers. See, e.g. [6, 4] for a thorough review. Approximate inverse preconditioners are becoming popular again due to their potential in concurrent computations especially on GPU hardware [35, 10, 1, 16, 27, 26].

In this work, we focus on the Factored Sparse Approximate Inverse (FSAI) preconditioner originally introduced in [22] and further developed over the years by other authors [18]. FSAI is particularly attractive due to its natural parallelism in both set-up and application and has already been successfully ported on GPU in both its static [7] and dynamic [8] pattern variants using CUDA, the parallel computing platform and programming model developed by NVIDIA for general computing on graphical processing units. The main novelty presented here is a highly optimized hybrid implementation (CUDA+MPI) that takes advantage of multiple GPU cards to speed-up the solution of very large linear systems arising from the simulation of a number of real-world phenomena.

Due to recent changes in CUDA we had to modify some of the kernels developed in the past and to tune the new distributed implementation for exploiting at its best the state-of-the-art interconnection technology we use.

The paper is organized as follows. In Section 2, we provide some basic theory about the aFSAI preconditioner that we present. In Section 3, we briefly recall the main GPU kernels used for aFSAI set-up and their update to the most recent CUDA version, whereas in section 4 we describe the issues related to the distributed memory implementation. Extensive numerical experiments are presented in section 5. Finally, we close the paper drawing some concluding remarks.

2. Factored Sparse Approximate Inverse with dynamic pattern selection. The FSAI preconditioner has been originally introduced for SPD matrices in [22], with the aim of directly approximating the inverse of A as the product of two triangular factors:

$$M^{-1} = G^T G \simeq A^{-1} \tag{2.1}$$

In the equation 2.1, G is a lower triangular matrix whose entries are computed by minimizing the following Frobenius norm:

$$\|I - GL\|_F \tag{2.2}$$

over the set  $\mathcal{W}_{\mathcal{S}}$  of matrices having a prescribed lower triangular non-zero pattern  $\mathcal{S}$ , as the one depicted in Figure 2.1. The matrix L, explicitly appearing in (2.2), is the exact lower triangular factor of A and it is not actually needed in the computation of FSAI, since it disappears during the minimization process as shown for instance in [22]. The unknown G entries,  $[G]_{ij}$ , are computed by solving the componentwise system:

$$[GA]_{ij} = \begin{cases} 0 & i \neq j, \quad (i,j) \in \mathcal{S} \\ [L]_{ii} & i = j \end{cases}$$

$$(2.3)$$

obtained through differention of (2.2) with respect to  $[G]_{ij}$  and setting it equal to zero. In the equation above, the symbol  $[\cdot]_{ij}$  in (2.3) is used to indicate the entry in row *i* and column *j* of the matrix between square brackets. Since  $[L]_{ii}$ , the *i*-th diagonal element of *L*, is unknown, we replace it in eq. (2.3) by 1. As a consequence, in place of *G*, we compute the matrix  $\tilde{G}$  by solving:

$$[\widetilde{G}A]_{ij} = \delta_{ij} \tag{2.4}$$

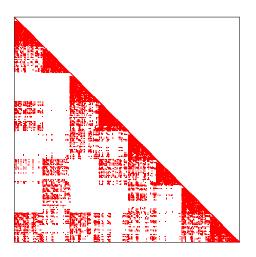


FIGURE 2.1. Example of a typical lower triangular non-zero pattern  $\mathcal{S}$ .

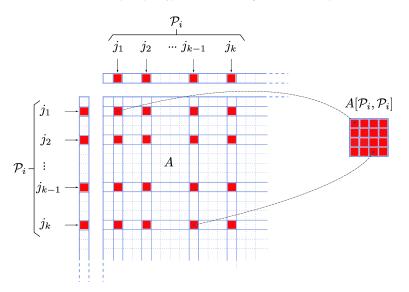


FIGURE 2.2. Schematic representation of the dense linear system gathering for a given set  $\mathcal{P}_i$  (with cardinality k).

with  $\delta_{ij}$  the Kronecker delta.

From a practical viewpoint, setting up the *i*-th row of  $\widetilde{G}$ , say  $\widetilde{g}_i^T$ , requires:

• first, the definition of the set  $\mathcal{P}_i$  collecting all the column indices that belong to the *i*-th row of  $\mathcal{S}$ , that is:

$$\mathcal{P}_i = \{j : (i,j) \in \mathcal{S}\}$$
(2.5)

- then, the gathering of the dense matrix  $A[\mathcal{P}_i, \mathcal{P}_i]$  formed with the entries of A having row/column indices in  $\mathcal{P}_i$ ;
- finally, solving the linear system:

$$A[\mathcal{P}_i, \mathcal{P}_i]\hat{G}[i, \mathcal{P}_i]^T = \boldsymbol{e}_{m_i}$$
(2.6)

with  $\widetilde{G}[i, \mathcal{P}_i]$  being the dense vector containing the non-zero entries of  $\widetilde{g}_i$  and the righthand side  $e_{m_i}$  given by the last vector of the canonical basis of  $\mathbb{R}^{m_i}$ , with  $m_i = |\mathcal{P}_i|$ .

Figure 2.2 gives an idea of the gathering process used to collect the dense linear systems  $A[\mathcal{P}_i, \mathcal{P}_i]$  given a set  $\mathcal{P}_i$ .

A more practical, although mathematical equivalent, way to implement the FSAI computation, see [18], consists in assuming  $\tilde{G}$  unitary diagonal and solving the linear system:

$$A[\overline{\mathcal{P}_i}, \overline{\mathcal{P}_i}]\widetilde{G}[i, \mathcal{P}_i]^T = -A[\overline{\mathcal{P}_i}, i]$$
(2.7)

where  $\overline{\mathcal{P}_i} = \mathcal{P}_i \setminus i$  and  $\widetilde{G}[i, \mathcal{P}_i]$  contains the *off-diagonal* non-zero entries of  $\widetilde{G}$ . A diagonal scaling is finally applied to  $\widetilde{G}$  in order to guarantee that all the diagonal entries of the preconditioned matrix are unitary:

$$\operatorname{diag}(D_G \widetilde{G} A \widetilde{G}^T D_G) = \operatorname{diag}(G A G^T) = I$$
(2.8)

where diag(·) is the operator returning the diagonal matrix having the diagonal of its argument as entries, I is the identity matrix and the  $D_G$  entries are given by:

$$D_G[i,i] = \frac{1}{A[i,i] - \widetilde{G}[i,\mathcal{P}_i]A[\overline{\mathcal{P}_i},\overline{\mathcal{P}_i}]\widetilde{G}[i,\mathcal{P}_i]^T}$$
(2.9)

Condition (2.8) ensures that G, over all the matrices  $B \in W_S$ , is the unique one minimizing the Kaporin number of the preconditioned matrix:

$$\kappa = \frac{\frac{1}{n} \operatorname{tr}(GAG^T)}{\det(GAG^T)^{\frac{1}{n}}}$$
(2.10)

which gives a measure of the PCG convergence rate [21].

The FSAI preconditioner for an SPD matrix is breakdown-free and possesses an extremely high degree of parallelism in both construction and application to a vector. However, to be competitive with other preconditioners, FSAI needs to be sparse with a non-zero pattern composed by significant entries of the true inverse factor of A. The appropriate a priori choice of S is unfortunately very difficult thus making the original FSAI unpractical in ill-conditional cases.

A better way to compute FSAI is by choosing S adaptively while computing G [17]. The basic concept in the adaptive computation of FSAI (aFSAI from now on) is the improvement of the quality of a given initial factor  $G_0$ , already satisfying equations (2.7) and (2.8), by extending its pattern with those entries that mostly contribute in reducing the Kaporin number of  $G_0AG_0^T$ . Let us define  $S_0$  the non-zero pattern of  $G_0$  and assume the identity matrix as our default initial guess. Writing explicitly the Kaporin number  $\kappa$  of  $G_0AG_0^T$ , it gives:

$$\kappa = \frac{\frac{1}{n} \operatorname{tr}(G_0 A G_0^T)}{\det(G_0 A G_0^T)^{\frac{1}{n}}} = \frac{\frac{1}{n} \operatorname{tr}(D_{G_0} \tilde{G}_0 A \tilde{G}_0^T D_{G_0})}{\det(D_{G_0} \tilde{G}_0 A \tilde{G}_0^T D_{G_0})^{\frac{1}{n}}}$$
(2.11)

and, recalling that  $G_0 A G_0^T$  has unitary diagonal entries and  $\det(\tilde{G}_0) = 1$  by construction, it follows that:

$$\kappa = \frac{1}{\det(A)^{\frac{1}{n}}} \frac{1}{\det(D_{G_0})^{\frac{2}{n}}} = \frac{\det\left[\operatorname{diag}(\widetilde{G}_0 A \widetilde{G}_0^T)\right]^{\frac{1}{n}}}{\det(A)^{\frac{1}{n}}}$$
(2.12)

Denoting by  $\widetilde{g}_{0,i}^T$  the *i*-th row of  $\widetilde{G}_0$ , we can write the numerator of (2.12) as:

$$\det\left[\operatorname{diag}(\widetilde{G}_{0}\widetilde{A}\widetilde{G}_{0}^{T})\right] = \prod_{i=1}^{n} \widetilde{\boldsymbol{g}}_{0,i}^{T} A \widetilde{\boldsymbol{g}}_{0,i} = \prod_{i=1}^{n} \psi_{0,i}$$
(2.13)

having defined  $\psi_{0,i} = \tilde{\boldsymbol{g}}_{0,i}^T A \tilde{\boldsymbol{g}}_{0,i}$ . With the above definiton, we can write a simplified expression for the Kaporin conditioning number of the preconditioned matrix:

$$\kappa = \left(\frac{\prod_{i=1}^{n} \psi_{0,i}}{\det(A)}\right)^{\frac{1}{n}}$$
(2.14)

which can be differentiated to obtain the gradient of  $\kappa$  with respect to  $\tilde{G}_0$ . Choosing the positions of the gradient corresponding to its largest entries in absolute value, allows for finding an augmented pattern  $S_1$  giving a large reduction of  $\kappa$  in equation (2.14). Since each  $\psi_{0,i}$  in (2.14) does not depend on any other row of  $\tilde{G}_0$  except the *i*-th one, the pattern expansion can be carried out on each row concurrently. The  $\psi_{0,i}$  gradient, denoted as  $\nabla \psi_{0,i}$ , is obtained by collecting its partial derivatives with respect to the components of  $\tilde{g}_{0,i}$ :

$$\frac{\partial \psi_{0,i}}{\partial [\widetilde{G}_0]_{ij}} = 2\left(\sum_{r=1}^n a_{jr} \left[\widetilde{G}_0\right]_{ir} + a_{ji}\right), \qquad \forall j = 1, \dots, i-1,$$
(2.15)

with the computational cost for its evaluation consisting in a single sparse-matrix by sparse-vector product. A new pattern  $\overline{\mathcal{P}}_i^1$  is obtained by enlarging  $\overline{\mathcal{P}}_i^0$  with the *s* positions corresponding to the largest entries of  $\nabla \psi_{0,i}$  in absolute value and finally  $\tilde{g}_{1,i}$  is computed by solving (2.7), after replacing the sub/superscript "0" with "1". Repeating the above procedure  $k_{\max}$  times allows to find all the rows of  $\tilde{G}_2$ ,  $\tilde{G}_3$ , ..., up to  $\tilde{G}_{k_{\max}}$ . It is also possible to monitor the preconditioner quality by computing the value of  $\psi_{k,i}$ . Hence it is possible to stop the adaptive procedure independently for every row when

$$\frac{\psi_{k,i}}{\psi_{0,i}} = \frac{\widetilde{\boldsymbol{g}}_{k,i} A \widetilde{\boldsymbol{g}}_{k,i}^T}{\widetilde{\boldsymbol{g}}_{0,i} A \widetilde{\boldsymbol{g}}_{0,i}^T} \le \varepsilon, \qquad (2.16)$$

being  $\varepsilon$  a user-specified tolerance. Once the approximation of  $\widetilde{G}$  is satisfactory, a diagonal scaling is applied, to ensure a unitary diagonal for  $GAG^T$ .

- Three user-specified parameters are generally used to control the aFSAI quality:
- 1.  $k_{\max},$  the maximum number of steps of the iterative procedure for each row;
- 2. s, the number of new positions added to the non-zero pattern of each row in a single step;
- 3.  $\varepsilon$ , the relative tolerance on the Kaporin number reduction used to stop the procedure.

**3.** GPU kernels for aFSAI set-up and application. A detailed description of the CUDA kernels in charge of the most demanding, from the computational viewpoint, phases of the aFSAI set-up is available in our previous works [7, 8]. Here we just recall that there are three main kernels for

- 1. the computation of  $\nabla \psi_i$ , i.e. of the *Kaporin gradient*, and selection of its most relevant components;
- 2. the collection of A entries to form  $A[\overline{\mathcal{P}}_i, \overline{\mathcal{P}}_i]$  and  $A[\overline{\mathcal{P}}_i, i]$ , that we call systems gather;
- 3. the solution to the sequence of collected dense SPD systems, carried out by means of *batch Cholesky decompositions*.

As we showed in [8], the computation of the Kaporin gradient of the input matrix is the part of the preconditioner set-up that requires more time. Although the algorithm for the evaluation of the Kaporin gradient remained the same, we had to modify its CUDA implementation due to the changes introduced in the *warp-level* primitives starting on the CUDA toolkit version 9.0. Since CUDA has been around for a while, we are not going to describe it in detail. However, we believe it is important to recall that, in the CUDA, GPUs execute warps of 32 parallel threads according to an execution model that NVIDIA calls Single Instruction Multiple Thread (SIMT), in other words, a variant of the SIMD (Single Instruction, Multiple Data) model, which is one of the four classes defined by the classic Flynn's taxonomy. CUDA toolkits prior to version 9.0 relied on the implicit assumption that the threads within a warp worked in a fully synchronous way. If this is not true, a program may show unexpected side effects up to the point of being unreliable. The point can be illustrated in a simple case based on the \_\_ballot(predicate) primitive that returns an unsigned int whose  $n^{th}$  bit is set if-and-only-if predicate evaluates as true for the  $n^{th}$  thread of the warp. In the fragment of code shown in listing 1, the CUDA compiler and the hardware should try to re-converge the threads right after the if/else block for better performance. But this re-convergence is not guaranteed in the most recent versions of the CUDA toolkit. Therefore, the **ballot\_result** variable may not contain the ballot result from *all* 32 threads.

Listing 1

Unsafe CUDA programming based on the implicit assumption that warp's threads run synchronously.

```
int result;
if (thread_id % 2) {
    result = foo();
} else {
    result = bar();
}
unsigned ballot_result = __ballot(result);
```

Starting on version 9.0, up to version 10.0 of the CUDA toolkit the legacy warp-level primitives worked synchronously (albeit with a deprecation warning at compilation time). But, starting on version 10.1, the only alternative to obtain the expected behaviour, is to employ an explicit control on the threads that participate in warp operations by using the new form of the warplevel primitives. The set of threads that participates in each primitive is specified by means of a 32-bit mask, which is always the first argument in the new syntax of the warp-level primitives. So, for instance, the new form of the \_\_ballot() primitive is \_\_ballot\_sync(mask, predicate). All the participating threads are synchronized before the execution if they are not already synchronized. In the simple case reported in listing 1, it is enough to replace the last line with unsigned ballot\_result = \_\_ballot\_sync(0xFFFFFFF, result);. Unfortunately there is not a general rule to determine what is the right value of the mask argument. The set of threads to be included in the mask is determined by the program logic, and may depend on branch conditions or other information available only at execution time. That is exactly the situation we had with the kernel for the evaluation of the Kaporin gradient that relies heavily on warp-level primitives like *shuffle* to exchange values stored in the registers among threads belonging to the same warp (as described in [8] this is the technique that makes very efficient the selection of min and max values within that kernel).

Besides the update of the kernel for the Kaporin gradient, for the present work, which includes a new multi-GPU implementation of the conjugate gradient algorithm, we developed also a new CUDA kernel for the sparse-matrix-dense-vector product. To that purpose we employ a group of threads for each row of the sparse matrix. Using a group instead of a single thread makes it possible to exploit at its best the memory bandwidth of the GPU, at least loading the elements of the matrix. We call the group of threads in charge of each row miniwarp in analogy with the group of 32 consecutive threads named warp in the CUDA jargon that we mentioned above. In particular, we consider sets (having the same number of elements) of contiguous threads with a possible cardinality of 2, 4, 8, 16 or 32. Those sets of threads are then concurrently mapped to different data like in other warp-centric kernels that use a warp to manage a block of contiguous data. The threads contained in a miniwarp are able to perform cooperative computation by exploiting efficient and fine-grained intra-warp communication primitives like the *shuffle*. During the execution of the product, each row of the sparse matrix is assigned to a single miniwarp; that is, multiple rows are concurrently executed in the same full warp of 32 threads. The size of a miniwarp is dynamically dependent on the average number of nonzeroes per row of the sparse matrix. The main advantage of this miniwarp variant is that, for matrices with few nonzero entries per row, the number of idle threads decreases. With a full warp (32 threads), if a row has, on average, only k < 32 nonzero entries, there are, always on average, 32 - k threads that remain idle. Miniwarps reduce the difference significantly by using a size that is much closer to the average number of nonzero entries per row. Fig. 3.1 shows how the miniwarp works when applied to a matrix in CSR format in the case of a sparse-matrix dense-vector multiplication.

The GPUs used during the development of the present work are NVIDIA Tesla V100 (based on the Volta CUDA architecture) equipped with 80 Stream Multiprocessors for a total of 5120 cores and 16 GByte of GDDR5 memory.

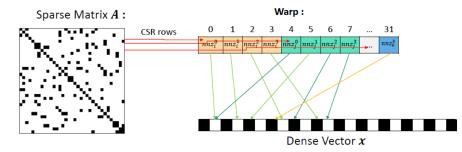


FIGURE 3.1. Each miniwarp is in charge of a row of the matrix stored in CSR format.

We show an example of the contribute of the three main kernels in the following fragment of the CUDA profiler (nvprof) output for a medium size matrix:

Time(%)	Time	Calls	Avg	Min	Max	Name
59.82%	5.12072s	400	12.802ms	698.88us	26.824ms	kapGrad_merge
27.27%	2.33450s	20	116.72ms	16.199ms	180.44ms	gatherFullSys
4.96%	424.63ms	20	21.232ms	170.02us	76.376ms	cudacholdc

The three kernels take more than 90% of the time. The remaining kernels are used to check if the convergence criterion for the refinement has been reached and to build, in the end, the preconditioner. None of them takes more than 0.5% of the total execution time and are all pretty simple.

4. Distributed memory implementation. In this section we give a detailed description of the distributed memory implementation of the aFSAI preconditioner and its use in an iterative solver as the conjugate gradient. To this aim, we firstly introduce the storage scheme adopted for the system matrix because from this scheme descends the communication pattern in both aFSAI set-up and Sparse-Matrix-by-Vector product (SpMV). We observe that the proposed storage scheme applies to the hybrid CPU-GPU implementation as well as to the pure CPU implementation that we use as a baseline for our numerical experiments. In the description that follows, we do not distinguish between the two implementations as the only difference is in the few, though computationally intensive, specific kernels introduced in section 3.

For the communication among different computational nodes we use the Message Passing Interface (MPI), whereas for intranode parallelization we use OpenMP for the CPUs and CUDA for the GPUs.

4.1. Distributed Sparse (DSMat) and Dense (DDMat) Matrix Storage Schemes. The storage scheme adopted to distribute the system matrix, referred to as DSMat, essentially consists in subdividing the sparse matrix into  $n_p$  horizontal stripes of consecutive rows, where  $n_p$  is the number of MPI processes. Each stripe is then further split vertically into rectangular blocks by applying the same subdivision, as shown in Fig. 4.1. Finally, each matrix subblock is stored according to the popular Compressed Sparse Row (CSR) matrix format.

To save memory and increase the overall efficiency, a local numbering is used within each CSR subblock, that is rows and columns of block IJ are numbered, in C notation, from 0 to  $n_{I-1}$  and from 0 to  $n_{J-1}$ , respectively, with  $n_I \times n_J$  the dimension of block IJ. This expedient allows for the use of the more favourable 4-byte integers even for very large matrices having billions of rows. Each process stores the diagonal block, which is generally the most populated one, representing the part of the matrix operating on the local unknowns, a list of "Left" and "Right" blocks representing the communication with neighboring processes having lower or higher rank, respectively. For instance, with reference to Fig. 4.1, processor 3 stores the 5 blocks highlighted in red, of which 0, 1 and 2 are denoted as left neighbors, 3 as diagonal block and 6 as right neighbor.

This blocked scheme used to store matrices is very effective in both the aFSAI computation and SpMV product because, as described in details below, it allows the use of non-blocking send/receive MPI primitives with a large overlap between computation and communication.

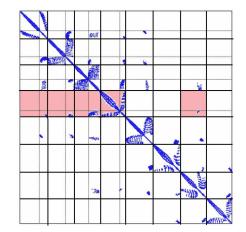


FIGURE 4.1. Schematic representation of the DSM at matrix storage scheme using 8 MPI processes. The red colored blocks are assigned to process 3.

Similarly to DSMat, we define the DDMat storage scheme for distributed dense matrices, where the matrix is partitioned into  $n_p$  horizontal stripes of consecutive rows. The entries of each stripe are stored row-wise in memory to guarantee a better access in memory during multiplication operations. This storage scheme is particularly advantageous for linear systems with multiple right-hand-sides and eigenproblems. For standard linear systems with only one rhs vector, the DDMat matrix simply reduces to one distributed vector.

## 4.2. Distributed memory Sparse-Matrix-by-Vector Product (SpMV).

The SpMV product Ay = z between a DSMat A and a DDMat y is the most expensive operation in any preconditioned iterative solver and on a distributed memory computer consists of a *communication* stage, mainly handled by the CPUs, and a *computation* stage, that can be performed either by the CPU or the GPU accelerator (or, in some implementations by both).

With reference to Fig. 4.2, processor 3 gathers the y terms highlighted in green and computes its stripe of z, highlighted in violet, as the sum of products between the extra-diagonal CSR blocks, in red, and the entries received from neighbouring processes, plus the contribution of the product between diagonal CSR blocks, in orange, and the stored y terms, in light blue. As detailed below, communication and computation can be conveniently overlapped thanks to non-blocking communications and the DSMat storage scheme:

- 1. First, local elements of  $\boldsymbol{y}$  to be sent are moved into a device buffer and copied on the host;
- 2. Then the host starts non-blocking send/receive communications to/from neighbouring processes;
- 3. in the meantime, the local component of z is initialized with the product between the diagonal CSR block and the local part of y;
- 4. each process sequentially tests all the incoming communications and as soon as some components of y are received, the corresponding buffer is copied onto the device and the local part of z is updated with the product by the off-diagonal CSR block;

It is easy to observe that the 3rd operation in the above list can be overlapped with the first two, and also the product by the off-diagonal blocks partly hides the communication latency for the transfer of non-local y components.

For an efficient execution, the SpMV algorithm requires a preliminary stage that we call *prepare*, during which each process communicates to its neighbors the list of y entries it needs to receive to perform the product by the off-diagonal blocks. Since this information does not change during the iterative solution of the system, it needs to be exchanged just once before the calculation starts.

**4.3. aFSAI set-up on a distributed memory computer.** Before calling the specific GPU kernels (briefly described in Section 3) for the aFSAI set-up on every single device, each

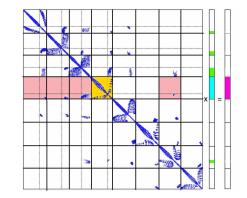


FIGURE 4.2. Schematic representation of the SpMV product.

MPI task needs to collect some information from the others. As the pattern of G is computed dynamically during the set-up, in principle each task may need matrix A entries belonging to any other task with lower rank. Obviously, such a condition cannot be satisfied in very large problems because the whole A matrix cannot be stored on a single node. On the other hand, preliminary tests showed that using only the information from neighbouring processes, as in the communication pattern of SpMV, is not enough to build a satisfactory preconditioner. So, we adopted an intermediate strategy. Let us denote by A the communication matrix of A, that is a boolean matrix of size  $n_p \times n_p$  with entries  $\widehat{A}_{ij} \neq 0$  if and only if the corresponding block ij of A contains at least one non-zero element. Then we impose that  $\widehat{G}$ , the communication graph of G, is no larger than the lower triangular part of  $\widehat{A}^k$  for a small power k, typically in the range  $1 \div 3$ , which is simply computed through a short sequence of small symbolic Sparse-Matrix-by-Sparse-Matrix products. Once G is known, we use it to guide the collection of information from other MPI tasks. With reference to Fig. 4.3, for instance, process 3 assembles locally the matrix  $A_3$ , that it uses locally to compute its own stripe  $G_3$  of G by gathering all the green blocks from its left-neighboring processes on  $\widehat{G}$ . Thanks to the symmetry, only the communication of the green blocks in the lower part is needed and the matrix in complete on site after a *transpose* operation.

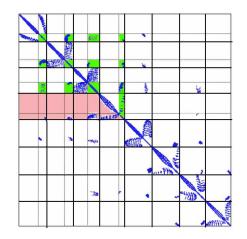


FIGURE 4.3. Schematic representation of the block collection for process 3. Green colored blocks in the lower part of the matrix A are those that need to be gathered for the assembly of  $A_3$ .

Note that, again as a positive effect of the symmetry, each process knows in advance from the pattern of  $\widehat{A}^k$  which blocks it has to receive and send to the other processes as well as the list of processes it needs to communicate with. The gathering/scattering process consists of 2 stages of communications, that can be partly overlapped by using non-blocking communication:

1. Each process sends to its right-neighboring processes (and receive from the left ones)

the sizes of the blocks that have to be exchanged;

2. Each process sends to its right-neighboring processes (and receive from the left ones) the above set of blocks;

We briefly note that, if a similar approach is extended to non-symmetric systems, each process needs to communicate to the others also the list of required blocks, which is not known, a priori, as in the symmetric case.

The communicated list of blocks can be conveniently received into a 2-dimensional array data structure with size  $(n_L + 1)^2$ , where  $n_L$  is the number of left-neighboring processes in  $\hat{G}$ . Only the block-lower part of this structure is actually filled with  $(n_L^2 + n_L)/2$  blocks received from the other processes plus the  $(n_L + 1)$  blocks already in place. Once all the communications have been completed, the 2-dimensional array of CSR matrices is copied into the full (lower plus upper) CSR matrix  $A_{I_p}$  that is the main input for the aFSAI GPU kernel. Note that, during this copy, these two large structures must coexist, becoming the main part of the memory footprint of each process, that can be quantified as ~ 1.6 the size of  $A_{I_p}$ .

As already noted in [8], the aFSAI set-up can be safely performed in single precision and, in the distributed memory context, this option is particularly advantageous. In fact, beyond reducing processing time due to the use of single-precision arithmetic, it also allows a smaller amount of data movement during the block-collection stage and the host-device copies. Two casting operations are needed in this case. The first one is performed on the matrix A at the host level: A is copied into a new matrix  $A_s$  using single precision floats for its entries,  $A_s = \text{single}(A)$ . Then, the matrix  $A_s$  is used for the aFSAI set-up, as described above. Once  $G_s$ , G with single precision entries, is computed, a second cast is performed at the device level transforming single precision floats into doubles,  $G = \text{double}(G_s)$ . This last casting operation can be conveniently overlapped with the host-device copy of the double precision A, since only  $A_s$  has been transferred before.

When both the double precision representation of A and G are present on the device, the PCG algorithm is ready to start.

5. Numerical Results. The aFSAI preconditioner is implemented as part of Chronos, a sparse linear algebra library for preconditioners and Krylov subspace iterative methods specifically designed for High-Performance computing systems [19]. For the evaluation of aFSAI performance, the Marconi100 supercomputer is used. Marconi100, the most recent cluster installed at the Italian consortium for computing, CINECA, is classified within the first ten positions of the TOP500 ranking. It is composed by 980 nodes based on the IBM Power9 architecture each equipped with two 16-cores IBM POWER9 AC922 at 3.1 GHz processors and four NVIDIA Volta V100 GPUs with Nvlink 2.0 and 16GB of memory. The benchmark matrices used for the numerical experiments are shown in Table 5.1, which provides the number of rows, n(A), the number of non-zeroes, nnz(A) and the field of application the matrices arise from. Most of the matrices have been collected over years from internal research or cooperation with other authors [23, 20, 28, 29]. In the remainder of this section, we first compare the efficiency of Chronos to that of the well-known open source package PETSc [2] in CPU-only runs to draw a baseline for the GPU experiments. Then, we compare GPU-accelerated aFSAI with the more traditional and perfectly scalable Jacobi preconditioner on our benchmark set. Finally, we provide some strong and weak scalability tests to prove the efficiency of the proposed implementation while using large scale computational resources.

5.1. Effectiveness of the DSMat storage scheme in the sparse matrix by vector **product**. In this subsection, we show how the proposed DSMat storage scheme improves the efficiency of the SpMV product in both CPU-only and GPU-accelerated runs.

To this aim, we first compare the time required by Chronos and PETSc to perform 100 iterations of Conjugate Gradient (CG) preconditioned with Jacobi using only CPUs. The choice of Jacobi is dictated by the fact that, since its implementation is straightforward, these tests allow us to directly evaluated the SpMV efficiency. Figures 5.1 to 5.3 show the comparison between PETSc, in pure CPU mode, and Chronos, in both CPU-only and GPU-accelerated mode, by increasing the computing resources from a quarter of node (8 CPUs and 1 GPU) to 4

Matrix Name	n(A)	$\operatorname{nnz}(A)$	Application field			
spe10	$3,\!410,\!693$	90,568,237	3D diffusion in heterogeneous media			
geo4m	4,224,870	335,738,340	3D geomechanics			
Finger	4,718,592	$23,\!591,\!424$	2D multiphase flow in porous media			
guenda11m	$11,\!452,\!398$	$512,\!484,\!300$	3D geomechanics			
M10	$11,\!593,\!008$	$940,\!598,\!090$	3D mechanical			
agg14m	$14,\!106,\!408$	633, 142, 730	3D mesoscale			
M20	$20,\!056,\!050$	$1,\!634,\!926,\!088$	3D mechanical			
geo61m	$61,\!813,\!395$	4,966,380,225	3D geomechanics			
Pflow73m	73,623,733	2,201,828,891	3D diffusion in heterogeneous media			
c4zz134m	$134,\!395,\!551$	10,806,265,323	3D Biomedicine			
pois198m	$198,\!076,\!032$	$1,\!384,\!390,\!392$	3D diffusion in omogeneous media			
$T_{ADID} = 5.1$						

TABLE 5.1

Benchmark matrices used in the numerical experiments. For each matrix, the size, n(A), the number of non-zeros, nnz(A), and the application field are provided.

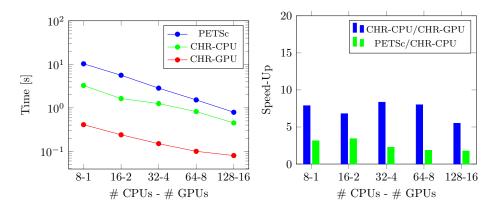


FIGURE 5.1. Scalability and Speed-Up of Jacobi preconditioned CG on the spe10 matrix. Left: total wall time in seconds for the execution of 100 iterations of Jacobi preconditioned CG. Right: Speed-Up of GPU-accelerated Chronos (CHR-GPU) over pure CPU Chronos (CHR-CPU) (blue columns) and Speed-Up of Chronos over PETSc in pure CPU runs (green columns). The computing resources vary from a quarter node to 4 nodes.

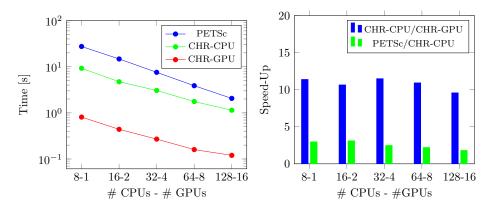


FIGURE 5.2. Scalability and Speed-Up of Jacobi preconditioned CG on the geo4m matrix. Left: total wall time in seconds for the execution of 100 iterations of Jacobi preconditioned CG. Right: Speed-Up of GPU-accelerated Chronos (CHR-GPU) over pure CPU Chronos (CHR-CPU) (blue columns) and Speed-Up of Chronos over PETSc in pure CPU runs (green columns). The computing resources vary from a quarter node to 4 nodes.

nodes (128 CPUs and 16 GPUs) on the test matrices spe10, geo4m and agg14m. The speed-up of Chronos CPU (CHR-CPU) over PETSc is on average 2.39 and reaches a maximum value of about 3.15. As expected, smaller speed-up values (about 2.00) are obtained as the computing

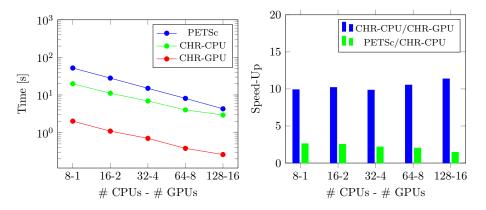


FIGURE 5.3. Scalability and Speed-Up of Jacobi preconditioned CG on the agg14m matrix. Left: total wall time in seconds for the execution of 100 iterations of Jacobi preconditioned CG. Right: Speed-Up of GPU-accelerated Chronos (CHR-GPU) over pure CPU Chronos (CHR-CPU) (blue columns) and Speed-Up of Chronos over PETSc in pure CPU runs (green columns). The computing resources vary from a quarter node to 4 nodes.

resources increase due to the communication overhead becoming significant on the overall run time. The GPU acceleration leads to a speed-up of about 10 for agg14m and geo4m matrices while it reaches a smaller value around 6 for spe10. This lower performance is easily explained by considering the lower number of non-zeroes per row characterizing spe10, which induces a worse operation over communication ratio. The use of GPU-accelerated Chronos allows an overall speed-up over CPU-only PETSc in the range from 15 to 25 on the performed test cases.

5.2. Effectiveness of aFSAI over Jacobi. The aFSAI preconditioner is much more demanding than Jacobi in term of both implementation effort and set-up time. However, the adoption of aFSAI in real world problems is fully justified by its superior effectiveness in accelerating CG convergence. Figure 5.4 shows the comparison between the total solution time, including also the set-up time, and the number of iterations necessary to reduce the initial residual of 8 orders of magnitude using CG preconditioned with Jacobi and aFSAI. We only consider the 4 smallest matrices of our set, as their solution cost though Jacobi would have been prohibitive with the largest ones. The experiments were run using the GPU-accelerated Chronos library on a single Marconi100 node and clearly show the ability of aFSAI in reducing the number of iterations. In all the tests aFSAI outperfoms Jacobi by a factor of at least 2 in the worst case up to 10 in the most ill-conditioned geo4m.

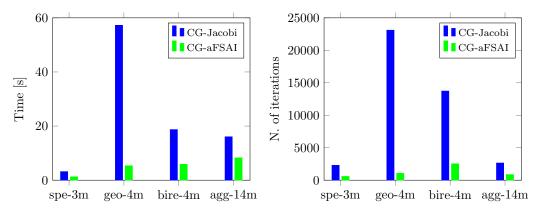


FIGURE 5.4. Comparison between the GPU-accelerated CG preconditioned with Jacobi and aFSAI using a single node of Marconi100. Left: Total solution time. Right: Number of iterations to converge.

**5.3.** Scalability of the GPU-accelerated adaptive FSAI. In this last subsection we analyze the strong and weak scalability of aFSAI preconditioned CG. We consider three different

times to evaluate scalability: the preconditioner set-up time,  $T_p$ , the iteration time,  $T_s$ , and total time,  $T_t = T_p + T_s$ . We ran strong scalability tests on the 8 largest matrices of Table 5.1, by varying the number of GPUs from the minimum necessary to store the matrix and the preconditioner to a maximum of 512, corresponding to 128 nodes. Figures 5.5 to 5.8 provide execution times and parallel efficiency vs the number of GPUs. In all tests both the set-up and solution time decrease inversely proportional to the computing resources with an almost ideal behaviour. The set-up stage is affected less than the iteration stage by efficiency reduction as communications have a lower impact in the preconditioner set-up. Regarding the parallel efficiency, Figure 5.9 shows the maximum number of GPUs such that the efficiency is, at least, 50% for the matrices arising from structural mechanics. We focused on this particular subset of matrices because all of them consists of more than 10 millions rows and have a similar number of non-zeroes per row ranging from 45 to 80. As expected, the computational resources that can be used at the same efficiency increase with the number of non-zeroes in the matrix.

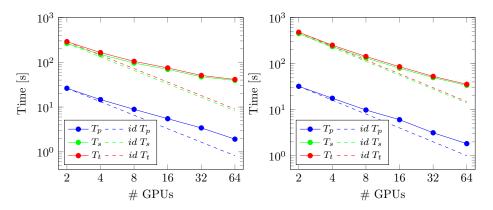


FIGURE 5.5. Strong scalability of aFSAI CG on matrices guenda11m (left) and M10 (right). aFSAI set-up time  $T_p$ , CG iteration time  $T_s$  and overall time  $T_t = T_p + T_s$  vs. number of GPUs.

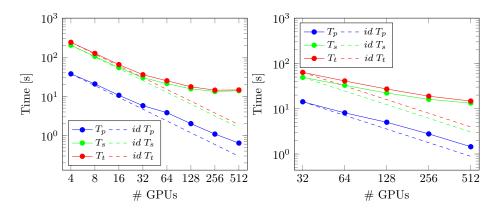


FIGURE 5.6. Strong scalability of aFSAI CG on matrices M20 (left) and geo61m (right). aFSAI set-up time  $T_p$ , CG iteration time  $T_s$  and overall time  $T_t = T_p + T_s$  vs. number of GPUs.

Finally, we test the weak scalability of our implementation using a 7-point stencil Finite Differences discretization of the Poisson problem on a cubic domain. In this experiment we keep a constant number of 1,771,561 equations for each GPU and increase the number of GPUs from 32 to 256. For larger problem sizes, the number of CG iterations increases (see Figure 5.10 upper-left), since aFSAI is not an optimal preconditioner, as for instance AMG. As a consequence, the iteration time as well as the total time correspondingly increase. However, if we focus on the set-up stage and the time required by a single CG iteration (bottom-left and bottom right of Figure 5.10, respectively) they do not change or only slightly change when the problem size increases, showing an almost perfect weak scalability.

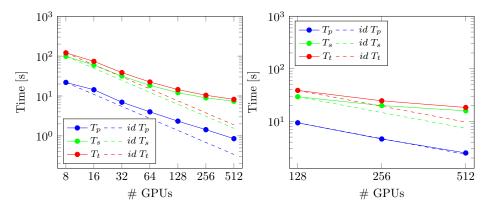


FIGURE 5.7. Strong scalability of aFSAI CG on matrices Pflow73m (left) and c4zz134m (right). aFSAI set-up time  $T_p$ , CG iteration time  $T_s$  and overall time  $T_t = T_p + T_s$  vs. number of GPUs.

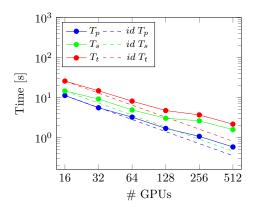


FIGURE 5.8. Strong scalability of aFSAI CG on matrix pois198m. aFSAI set-up time  $T_p$ , CG iteration time  $T_s$  and overall time  $T_t = T_p + T_s$  vs. number of GPUs.

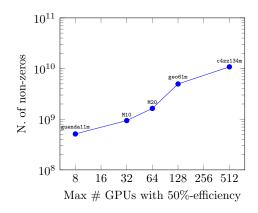


FIGURE 5.9. Maximum number of GPUs that guarantee a parallel efficiency of, at least, 50% for test matrices arising from structural mechanics.

6. Conclusions. We presented a multi-GPU implementation of the adaptive FSAI preconditioner aimed at reducing the number of conjugate gradient iterations required for the solution of large sparse linear systems originated by the discretization of PDE in a number of scientific and engineering fields. We proposed a new memory layout for the matrix that facilitates the overlap between communication and computation. We carried out an extensive set of numerical tests that show the efficiency of the proposed solution. We make available the library including both the adaptive FSAI preconditioner and the conjugate gradient solver so

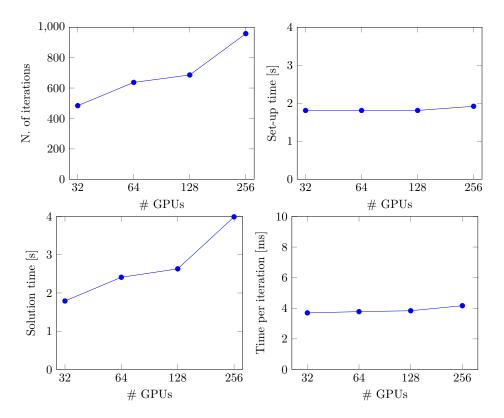


FIGURE 5.10. Weak scalability of aFSAI CG on the Poisson model problem. Number of CG iteration (top left), iteration time [s] (top right), set-up time [s] (bottom left) and time for one iteration [s] (bottom right) vs. the number of GPUs.

that other people may use it both for benchmarking and production purposes. The software is available along with the source of a sample program from https://www.m3eweb.it/chronos/. For the future we expect to develop a new version that will provide support for other forms of communication among GPU, for instance the third generation of Nvlink communication technology recently announced by Nvidia.

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