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XX Ciclo

# Analysis of the physical processes that limit the reliability of GaN-based optoelectronic devices

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# Contents

# Abstract

This thesis reports the results of an extensive analysis of the reliability of GaN-based Light-Emitting Diodes (LEDs) and Laser Diodes (LDs). The analysis has been carried out in close cooperation with the manufacturers of the devices: for this reason, we have worked on state-of-the-art LEDs, lasers and R&D samples, providing a feedback to the manufacturer on the weaknesses of adopted technology. By means of specific experiments on suitable test structures, we have been able to separately analyze *(i)* the degradation of the LEDs active region, *(ii)* the role of passivation layer in limiting LEDs reliability, *(iii)* the degradation of the ohmic contacts of the devices, *(iv)* the degradation of the properties of LEDs package and resins and *(v)* the degradation of violet laser diodes and its dependence on driving conditions.

In particular we have demonstrated that:

- Low current density stress can determine the degradation of the properties of the active layer of light-emitting devices, generating an increase of the non-radiative recombination rate, due to the modification of defects properties. Combined optical and electrical characterization can be used as an efficient tool for the analysis of the charge instabilities and of the related optical power decrease

- High temperature stress implies the degradation of the contact and semiconductor layer at the p-side of GaN-based LEDs. Degradation has been attributed to the interaction between hydrogen and the acceptor dopant, with subsequent compensation of the effective acceptor concentration and worsening of the current and emission spreading at devices surface.

- An important source of the hydrogen responsible for devices degradation is represented by the PECVD-SiN passivation layer, usually deposited on the

devices for surface leakage reduction and chip encapsulation. The use of this kind of H-rich passivation can strongly limit LEDs stability at high temperature levels. We have therefore proposed and demonstrated sputtered passivation as a more stable alternative to the conventionally adopted PECVD passivation for devices to be used in high temperature environment.

- Transmission Line Method can be efficiently used for the analysis of the degradation of the ohmic contacts on p-GaN submitted to high temperature storage. This technique provides important information on the impact of thermal treatment on the properties of metal/semiconductor interface and p-type GaN layer, because it allows to separately analyze the degradation of the semiconductor layer and of the ohmic contact properties. It has been shown that high-temperature degradation process mostly interests the semiconductor region close to the metal/semiconductor interface. Two critical parts of devices structure must be improved to obtain reliable behavior at high temperature levels: *(i)* the metal/semiconductor interface and contact and *(ii)* the passivation layer. High-temperature degradation of ohmic contact on p-GaN has been found to be reversible.

- Combined electrical, optical and microscopical analysis can be used for the evaluation of the different processes that determine the degradation of high power LEDs for lightning application. In particular, relevant information on the degradation of the contact layers and of the package/phosphors system have been obtained by means of this set of techniques. An extensive characterization of the degradation kinetics under different stress temperature levels has provided important information on the activation energy of the degradation process. These information have been used for the estimation of devices lifetime under nominal operating conditions.

- By means of a wide set of ageing tests under different driving conditions (current, optical power and temperature level) it is possible to characterize the degradation of InGaN-based laser diodes, and its dependence on the driving conditions. In particular we have shown that stress at constant current and constant optical power level can induce the increase of the threshold current of these devices, due

to an impurity diffusion process. The tests carried out within this work indicate that the degradation rate depends on stress temperature and current level, while it is not significantly influenced by the optical field in the cavity. The identified degradation process is supposed to be electro-thermally activated.

The results of the activity are described in the following chapters. This thesis reports the most important results obtained during the Ph.D. program of the candidate. Useful information on the activity can be also found in the following papers co-authored by the candidate.

# Sommario

Questa tesi descrive i risultati di un ampio studio dell'affidabilità di Diodi Emettitori di Luce (LED) e Diodi Laser (LD) in nitruro di gallio (GaN). L'analisi è stata condotta in stretta collaborazione con i costruttori dei dispositivi: ciò ha permesso di lavorare su dispositivi allo stato dell'arte e su prototipi R&D, e di fornire un feedback ai costruttori sulle debolezze tecnologiche riscontrate nel corso del lavoro.

Mediante esperimenti specifici si sono analizzati separatamente *(i)* il degrado della zona attiva di LED su GaN, *(ii)* il ruolo della passivazione nel degrado termico di LED su GaN, *(iii)* il degrado dei contatti ohmici dei dispositivi, *(iv)* il degrado di package e resine di LED bianchi di potenza e *(v)* il degrado di diodi laser Blu-Ray, al variare delle condizioni di stress.

In particolare in questo lavoro si dimostra che:

- Lo stress a basse densità di corrente può determinare il degrado della zona attiva di LED in GaN, inducendo un aumento del tasso di ricombinazione non-radiativa, a causa della generazione di difetti. L'analisi elettro-ottica delle caratteristiche dei dispositivi durante lo stress fornisce informazioni sulle instabilità del profilo di carica ed il conseguente calo di efficienza.

- Lo stress ad alte temperature determina la degradazione dei contatti ohmici al lato p di LED in GaN. La causa di questa degradazione è la compensazione del drogante accettore da parte dell'idrogeno, con conseguente peggioramento dei meccanismi di trasporto di corrente alla superficie dei LED.

- La passivazione in nitruro di silicio, usualmente deposta mediante PECVD per ridurre le correnti di perdita ed incapsulare i chip, rappresenta un'importante sorgente di idrogeno. L'uso di questo tipo di passivazione può limitare fortemente

l'affidabilità di LED ad alte temperature, a causa della compensazione del drogante accettore da parte dell'idrogeno. Per questo motivo, si è proposto l'utilizzo di passivazione SiN deposta mediante sputtering (basso contenuto di idrogeno) come alternativa alla passivazione PECVD convenzionale per la realizzazione di dispositivi affidabili anche ad alte temperature.

- Il Transmission Line Method è uno strumento efficace per l'analisi del degrado termico di contatti ohmici su p-GaN. Questa tecnica permette di analizzare separatamente il degrado dell'interfaccia metallo/semiconduttore e degli strati di p-GaN durante lo stress termico. In questo lavoro si dimostra che i trattamenti termici influenzano prevalentemente le proprietà elettriche dell'interfaccia metallo-semiconduttore, mentre non determinano un aumento significativo della resistività degli strati di p-GaN. Il meccanismo di degradazione descritto è reversibile, e dipende fortemente dal tipo di passivazione utilizzato per incapsulare i dispositivi.

- Mediante analisi elettrica, ottica e microscopica è possibile caratterizzare nel dettaglio il degrado di LED bianchi di potenza. In particolare, mediante queste tecniche è stato possibile studiare nel dettaglio il degrado del sistema package/fosfori di LED sottoposti ad invecchiamento termico, ed il conseguente peggioramento delle proprietà cromatiche dei dispositivi. Mediante stress a diverse temperature si è potuta estrapolare l'energia di attivazione del processo di degrado, parametro utile per la stima dei tempi di vita dei dispositivi in condizioni di funzionamento nominali.

- Mediante di prove di invecchiamento condotte in diverse condizioni operative (corrente, temperatura, potenza ottica) è possibile caratterizzare la degradazione di diodi laser in GaN, e la dipendenza delle cinetiche di degrado dalle condizioni di pilotaggio. In particolare, in questo lavoro si dimostra che lo stress a corrente o potenza ottica costante determinano l'aumento della corrente di soglia dei dispositivi, a causa della diffusione di una o più impurezze verso la zona attiva dei laser e del conseguente aumento del tasso di ricombinazione non-radiativa. Le prove effettuate indicano che il tasso di degrado dipende dalla temperatura

e dalla corrente di stress, ma non dall'intensità del campo ottico in cavità. Il meccanismo di degrado individuato è attivato Elettro-Termicamente.

I risultati dell'attività di ricerca sono descritti nel seguito. Questa tesi riassume i risultati più significativi ottenuti dal candidato durante il triennio di dottorato. Utili dettagli possono essere reperiti anche nei seguenti articoli.

# List of publications

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# Introduction

During the last decade, gallium nitride alloys have been shown to represent excellent materials for the development of optoelectronic devices working in the visible and UV range. The emission spectrum of these devices can be tuned almost continuously from the deep UV to the whole visible range, by varying the In and Al content in the AlInGaN alloy. This has unfolded dramatic changes in optoelectronics industry.

Semiconductor blue and white light-emitting diodes (LEDs) are characterized by smaller volumes, compatibility with automated electronic assembly techniques, better reliability with respect to conventional light sources and for these reasons are considered to be the candidates for the next generation of light sources for general lighting.

Furthermore, as a result of the recent efforts on AlGaN-alloys, efficient ultraviolet (UV) LEDs with mW power output and peak wavelength as low as 250 nm have been demonstrated [1]. UV LEDs have many important applications, including biological and chemical agent detection, air-water purification, money validation, biomedical treatment [2, 3]. In addition, using suitable phosphors these devices can be utilized to fabricate white LEDs, which are expected to replace the low-pressure mercury discharge white lamps in the future (proposed European Union rules indicate mercury as an hazardous substance, not acceptable for commercial applications). Moreover, gallium nitride-based laser diodes (LDs), emitting in the blue and violet range, are now commercially available, and represent excellent candidates for the next generation of optical data storage systems: their short wavelength and the increasing continuous wave output power will make possible the realization of low cost high density-high speed storage system in the next few years.

Despite these excellent properties, there are several factors limiting the improvement of the characteristics of GaN-based optoelectronic devices, as well as

their reliability. The most important are:

- Devices hetero (SiC, sapphire and Si) and homoepitaxial growth imply high dislocation density ($10^6 - 10^{12}\ cm^{-2}$) in the active layer [4, 5]. Such dislocation densities do not compromise LED and LD efficiencies [6], but have an impact in limiting devices lifetime, acting as diffusion channels for non-radiative defects [7]

- p-dopant (Mg) tends to form Mg-H complexes with hydrogen. Hydrogen in GaN has been extensively studied: it is incorporated in GaN during growth and subsequent processing steps; hydrogen may rapidly diffuse within GaN; thermal and current stress can generate/dissociate Mg-H complexes, therefore compromising devices reliability [8, 9]

- ohmic contacts are quite critical, with resistivities of $10^{-1} - 10^{-3}\ \Omega cm^2$ for Ni/Au and Pt contacts on p-GaN. Modifications of the contacts properties have been identified as a consequence of stress [10], with subsequent development of permanent current crowding effects [11]. However there is no systematic study of the stability of ohmic contacts and of the semiconductor material under thermal or current stress

- the high piezoelectric and spontaneous electric fields give rise to huge internal fields (1-2 MV/cm). Such electric fields produce a strong Quantum Confined Stark Effect, modifying the electron and hole recombination dynamics and decreasing the radiative recombination rate [12]. Problems related to internal fields can be partly solved by means of non-polar devices, and research is in progress in this direction [13]

- chip surface passivation is crucial for leakage current control, but its deposition may introduce contaminants that can interact with devices surface and reduce LED/LD reliability [14]

- the always higher power levels reached by the devices and the corresponding high temperatures imply reduced lifetime due to *(i)* the degradation of the transparency of the optical coating (also related to UV irradiation), epoxy package [15, 16] and laser facets [17]; *(ii)* the thermally activated interaction

between Mg-dopant and hydrogen [8, 14]; *(iii)* the thermally-enhanced metal electro- migration along threading dislocations or tube defects [18]. Thermal management at chip and system level is therefore critical, as well as the development of suitable packages, phosphors (for LEDs) and lenses (both for LEDs and LDs)

- stress can induce the growth of regions of non-radiative recombination, starting from areas of maximum power densities and/or maximum lattice strain and expanding within the device active area [19, 20]

- catastrophic failures have been also observed, and attributed to: *(i)* thermal degradation of the device optical coating, shorting the junction [21]; *(ii)* electro-thermal migration of metal coming from ohmic contacts via threading dislocations across the p-n junction; *(iii)* catastrophical optical damage at laser facets, due to high photon density and local heating [17]; (iv) Electro Static Discharge events [22].

During the last years, many works on the reliability of GaN-based optoelectronic devices have been published (see for example [21, 18, 11, 23, 24, 25, 9]). Several physical mechanisms have been identified as responsible for devices degradation such as modifications of the electrical contacts [21], changes in the local indium concentration in the quantum wells (QW) [26, 27], formation of radiative and non-radiative centers [28, 23], changes in the charge-injection mechanisms across the cladding and barrier layers (pure tunnelling, trap/phonon assisted tunnelling, thermal emission etc.) [29], aggregation or breaking of complexes mainly involving hydrogen impurities and magnesium p-dopant [30].

However, most of the studies quoted above referred to degradation processes that depend both on driving current and operating temperature, without indicating how these two driving forces separately act in determining devices degradation. Furthermore, in many stress tests, more than one process is involved in devices degradation, thus complicating the interpretation and the analysis of the degradation physics. This consideration indicates that it is important to define specific test procedures and samples with the aim of separately analyze each of the processes responsible for degradation and to evaluate the dependence of stress kinetics on the

most important degradation driving forces (current, temperature and optical power level).

Therefore, the aim of this thesis is to describe the physical mechanisms that limit the reliability of GaN-based optoeletronic devices, by separately analyzing the effect of current and of temperature on LED and laser performance during stress. Furthermore, we describe here a set of experiments that have been used to separately analyze *(i)* the degradation of the heterostructure properties, *(ii)* the degradation of the contact and p-type semiconductor layers, *(iii)* the role of passivation in determining devices degradation, *(iv)* the degradation of devices package during stress and *(v)* the degradation of the radiative properties of LDs active layer related to impurity diffusion.

The analysis has been carried out in close cooperation with the devices manufacturers: as a consequence, we have had the possibility of working on state-of-the-art devices with optimized growth and epitaxial parameters and on R&D samples specifically grown for our analysis. The results of this work have provided important information on the physics of the degradation processes, and have been used by the manufacturers as starting point for the improvement of growth and technological processes.

The analysis carried out within this work has demonstrated that:

- Low current density stress tests can be used for the analysis of the degradation of the properties of the active layer related to carrier flow. Under these stress conditions, the most significant degradation process is the increase of the non-radiative recombination rate, due to the modification of defects properties. On the other hand, no significant degradation of the properties of the contacts and dopant instabilites are induced by low current stress. In Chapter 3 it is shown that combined optical and electrical characterization can be used as an efficient tool for the analysis of charge instabilities and related optical power decrease taking place as a consequence of dc bias stress

- High temperature stress implies the degradation of the contact and semiconductor layer at the p-side of GaN-based LEDs. On the other hand, no significant modification of the radiative properties of the active layer has been detected during high temperature stress. As described in Chapter 4, degradation can be

attributed to the interaction between hydrogen and the acceptor dopant, with subsequent compensation of the effective acceptor concentration and worsening of the current and emission spreading at devices surface.

- An important source of the hydrogen responsible for devices degradation is represented by the PECVD-SiN passivation layer, usually deposited on the devices for surface leakage reduction and chip encapsulation. We have therefore proposed and demonstrated sputtered passivation as a more stable alternative to the conventionally adopted PECVD passivation for devices to be used in high temperature environment (see Chapter 4).

- Transmission Line Method (TLM) can be efficiently used for the analysis of the degradation of the ohmic contacts on p-GaN submitted to high temperature storage. As described in Chapter 5, this technique provided important information on the impact of thermal treatment on the properties of metal/semiconductor interface and p-type GaN layer. In particular, the comparison between the data on the degradation of LEDs and of TLM samples showed that high-temperature degradation process mostly interest two critical parts of LED structure that must be improved to obtain reliable behavior at high temperature levels: *(i)* the metal/semiconductor contact and *(ii)* the passivation layer.

- Combined electrical, optical and microscopical analysis can be used for the evaluation of the different processes determining the degradation of high power LEDs. In particular, information on the degradation of the optical properties of the package/phosphors system have been obtained by means of this set of techniques, as described in Chapter 6. An extensive characterization of the degradation kinetics under different stress temperature levels can finally provide important information on the activation energy and acceleration factors of the degradation process. These information have been used for the estimation of devices lifetime under nominal operating conditions.

- Constant current and constant optical power stress can induce the degradation of the optical characteristics of InGaN-based laser diodes. Stress determines the

increase of the threshold current according to the square-root of stress time, thus suggesting that a diffusion process is involved in devices degradation. As described in Chapter 7, devices degradation rate was found to significantly depend on the stress current level and on the stress temperature level, while only a weak dependence on optical field has been detected. On the basis of the tests carried out within this work, we have attributed devices degradation to an electro-thermally activated diffusion of impurities towards the active layer of the devices, with subsequent increase of the non-radiative recombination rate.

The initial two chapters of this thesis briefly describe the theoretical concepts that are necessary for the understanding of the subsequent part of the thesis. In particular Chapter 1 summarizes the basic properties of GaN-based semiconductors, while in Chapter 2 a brief overview on the electrical, optical and capacitive characteristics of GaN-based optoelectronic devices is given. The subsequent chapters describe the main results of the research activity.

Research activity has been carried out in the framework of two Italian Research Ministry (MUR) projects (PRIN), in close cooperation with the partners of the Universities of Bologna, Cagliari, Parma, Firenze. The wide set of characterization techniques used for this thesis has been available only thanks to the cooperation of the partners involved in this project. Furthermore, the results described in this thesis have been reached under strict cooperation and discussion with the colleagues and professors at the University of Padova. The author want to thank all the persons that have cooperated to this research activity.

# Chapter 1

# GaN basics

Gallium nitride and its alloys represent excellent materials, especially for the development of blue and UV light emitting diodes. The III-V nitrides, aluminum nitride (AlN), gallium nitride (GaN) and indium nitride (InN), are candidate materials for optoelectrical applications at such photon energies, because they form a continuous alloy system (InGaN, InAlN, and AlGaN) whose direct optical bandgaps for the hexagonal wurtzite phase range from 0.7 eV for InN and 3.4 eV for GaN to 6.2 eV for AlN (see Figure 1.1). High brightness visible light-emitting diodes (LEDs) are now commercially available, a development which has transformed the market for LED-based full color displays and which has opened the way to many other applications, such as in traffic lights and efficient low voltage, flat panel white light sources. Continuously operating UV laser diodes have also been demonstrated in the laboratory, exciting tremendous interest for high-density optical storage systems, UV lithography and projection displays. In a remarkably short space of time, the nitrides have therefore caught up with and, in some ways, surpassed the wide band gap II-VI compounds (ZnCdSSe) as materials for short wavelength optoelectronic devices. In this chapter we will briefly review the main properties of this material system, the most important problems and open issues related to n and p-type doping, the presence of hydrogen in GaN and the characteristics of ohmic contacts to be used for the applications. The discussion of these topics is necessary to understand the characterization and reliability studies described in the following chapters.

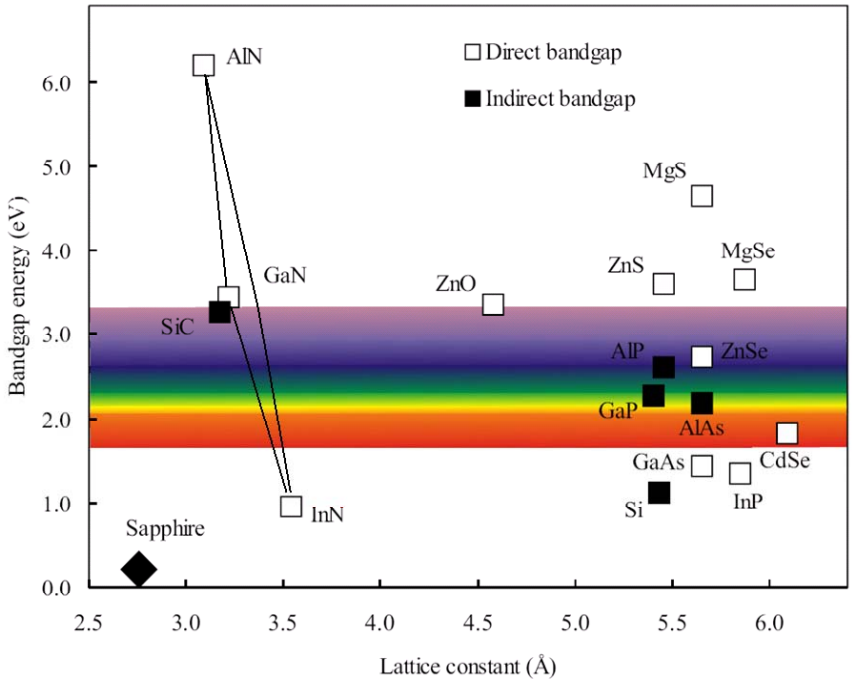



**Figure 1.1:** Bandgap energy versus lattice constant for various semiconductors including GaN and its alloys

## 1.1 Crystal and band structure

Gallium nitride and its related compounds can crystallize both in the cubic zincblende as well as in the hexagonal wurtzite structure (see Figure 1.2). These structures represent the unit cells of the GaN lattice: each of them is characterized by three lattice constants $a$, $b$, $c$, and by three angles $\alpha$, $\beta$, $\gamma$, that express the distance and the reciprocal position of the atoms in the cell. Zincblend has three identical lattice constants ($a = b = c$, $\alpha = \beta = \gamma = 90°$), while for wurtzite cell properties are defined by $a = b \neq c$, $\alpha = \beta = 90°$, $\gamma = 120°$. For gallium nitride, the wurtzite structure is more common: this fact represents a difference with respect to what happens for other widely used semiconductor materials. In fact, silicon and germanium have a diamond lattice, while other III-V semiconductors, such as GaAs and GaP, have the zincblende structure. The most important properties of gallium nitride (both for wurtzite and zincblende structure) are summarized in Table 1.1: in this table, the basic properties of GaN are compared to those of other common semiconductors. As can be noticed, the large bandgap energy of GaN results in high electric breakdown fields, which enable the

application of high supply voltages. Furthermore, it allows the material to withstand high operating temperatures and provides for improved radiation hardness. Another important advantage of GaN is its high thermal conductivity, that makes it a good choice for the realization of high power devices. These characteristics can explain the incredible attention that has been focussed on GaN-based material system during the last decade.

Calculated band structure is shown in Figure 1.3 for the wurtzite case [31, 32]. These diagrams are similar to the ones of some direct-bandgap zincblende semiconductor (such as for example GaAs), but with significant differences: the degeneracy of the valence band (levels A, B, C in Figure 1.3) is more pronounced in GaN with respect to GaAs, due to the strong electric field present in the crystal structure. However, in GaN strain has a less effective role in deforming the valence band with respect to GaAs.

| Properties (300K) | Symbol | Ge | Si | GaAs | GaP | GaN |
|---|---|---|---|---|---|---|
| Crystal structure (D=Diamond, Z=Zincblende, W=Wurtzite) | | D | D | Z | Z | W Z |
| Gap (D=Direct, I=indirect) | | I | I | D | I | D |
| Lattice constant | $a_0 = b_0$[Å] | 5.64 | 5.43 | 5.65 | 5.45 | 3.19 4.52 |
| | $c_0$ [Å] | | | | | 5.19 4.52 |
| Bandgap energy | $E_g[eV]$ | 0.66 | 1.12 | 1.42 | 2.26 | 3.44 3.3 |
| Intrinsic carriers concentration | $n_i[cm^{-3}]$ | $2\times10^{13}$ | $1\times10^{10}$ | $2\times10^{16}$ | $1.6\times10^{10}$ | $1.9\times10^{10}$ |
| Electron mobility | $\mu_n[cm^2/Vs]$ | 3900 | 1500 | 8500 | 110 | 1500 |
| Hole mobility | $\mu_p[cm^2/Vs]$ | 1900 | 450 | 400 | 75 | 30 |
| Electron diffusion constant | $D_n[cm^2/s]$ | 101 | 39 | 220 | 2.9 | 39 |
| Hole diffusion constant | $D_p[cm^2/s]$ | 49 | 12 | 10 | 2 | 0.75 |
| Electron affinity | $\chi[V]$ | 4.0 | 4.05 | 4.07 | | 4.1 |
| Refractive index | $n_{\text{opt}}$ | 4.0 | 3.3 | 3.4 | | 2.67 2.5 |
| Breakdown field | $\varepsilon_1[\times10^5$ V/cm] | 0.8 | 3 | 3.5 | | 33 |
| Thermal conductivity | $k[W(cm\ k)^{-1}]$ | 0.606 | 1.412 | 0.455 | 0.97 | 1.5 |

**Table 1.1:** Comparison between the main electrical and thermal parameters of common semiconductor materials

## 1.2 Polarity and polarization of nitrides

### 1.2.1 Piezoelectric and internal polarization fields

Because of the lack of electrons occupying the outer orbitals of the N atom ($1s^2 2s^2 2p^3$ electronic configuration), the electrons involved in the metal-nitrogen covalent bond are strongly attracted by the Coulomb potential of the N atomic nucleus. This means that this covalent bond of gallium nitride will have stronger ionicity compared to other III-V covalent bonds. This ionicity, which is a microscopic polarization, will result in a macroscopic polarization if the crystal has lack of inversion symmetry.

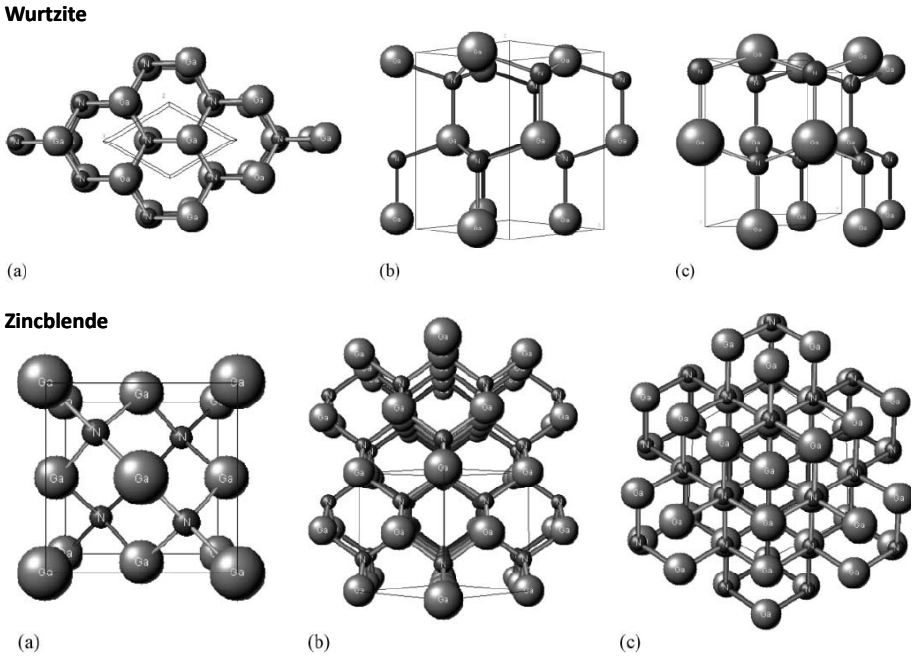



**Figure 1.2:** schematic representation of the wurtzite (top) and zincblende (bottom) unit cell. Perspective is given along various directions: (a) [0 0 0 1]; (b) [1 1 2 0]; (c) [1 0 1 0] [33]

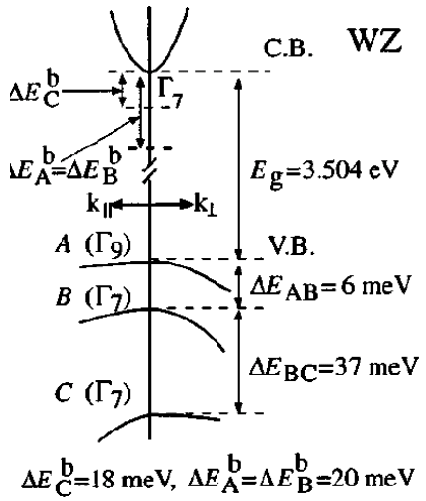



**Figure 1.3:** Calculated values of the band energy levels near the Γ point. $\Delta E_A^b$ ,$\Delta E_B^b$, $\Delta E_C^b$ are the binding energies of the A, B, and C excitons, respectively [31]

Both wurtzite and zincblende structures have lack of inversion symmetry. In particular, the bonds in the [0001] direction for wurtzite and [111] direction for zincblende are all faced by nitrogen in the same direction and by the cation in the opposite direction. This fact in combination with the strong ionicity of the metal-nitrogen bond results in a strong macroscopic polarization along the [0001] direction. Since this polarization effect occurs in the equilibrium lattice of III-nitrides at zero strain, it is called spontaneous polarization.

Both bulk and surface properties can depend significantly on whether the surface is faced by nitrogen or metal atoms. The most common growth direction of hexagonal GaN is normal to the [0001] basal plane, where the atoms are arranged in bilayers consisting of two closely spaced hexagonal layers, one with cations and the other with anions, so that the bilayers have polar faces (lack of inversion symmetry). Thus, in the case of GaN a basal surface should be either Ga- or N-faced. By Ga-faced we mean Ga on the top position of the [0001] bilayer, corresponding to [0001] polarity (Figure 1.4).

If stress is applied to the III-nitride lattice, the ideal lattice parameters of the crystal structure will change to accommodate the stress. Hence, the polarization strength will be changed. This additional polarization in strained III-nitride crystals is called piezoelectric polarization. Wurtzite is the structure with highest symmetry compatible with the existence of spontaneous polarization [34] and the piezoelectric tensor of wurtzite has three independent nonvanishing components. Therefore, polarization in GaN-based material systems will have both a spontaneous and a piezoelectric component.

In this section, we will discuss the characteristics of the internal polarization fields, and their role in determining heterostructure characteristics. As stated above, in wurtzite, both spontaneous (the polarization at zero strain) and a piezoelectric component are present.

In the absence of external electric fields, the total macroscopic polarization $P$ of a solid is the sum of the spontaneous polarization $P_{SP}$ in the equilibrium lattice and the strain-induced or piezoelectric polarization $P_{PE}$. Here we consider polarizations along the (0001) axis, because this is the direction along which standard bulk materials, epitaxial films and heterostructures are grown. Spontaneous polarization field along axis $z$ can be expressed as $P_{sp} = P_{sp}z$, on the basis of the parameters listed in Figure 1.5

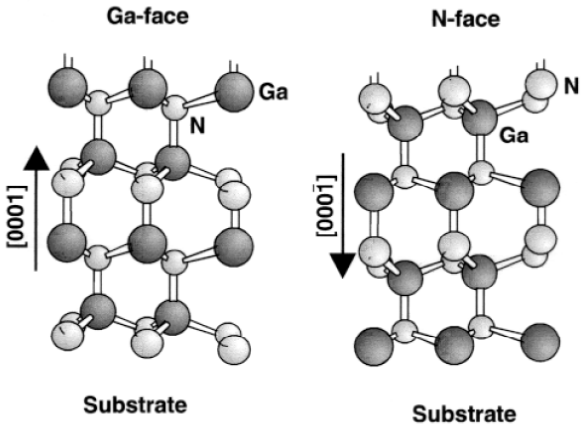



**Figure 1.4:** Different polarities (Ga- and N-faced) of wurtzite GaN.

[34]. On the other hand, piezoelectric polarization can be calculated by means of

$$P_{PE} = e_{33}\epsilon_z + e_{31}(\epsilon_x + \epsilon_y) \tag{1.1}$$

where $a_0$ and $c_0$ are the equilibrium values of the lattice parameters, $\epsilon_z = (c - c_0)/c_0$ is the strain along the c-axis,and the in-plane strain $\epsilon_y = \epsilon_x = (a - a_0)/a_0$ is assumed to be isotropic.

| Wurtzite | AlN | GaN | InN |
|---|---|---|---|
| $\mathbf{P}_{SP}$ (C m$^{-2}$) | −0.081 | −0.029 | −0.032 |
| $e_{33}$ (C m$^{-2}$) | 1.46[a]<br>1.55[b] | 0.73[a]<br>1[c]<br>0.65[d]<br>0.44[e] | 0.97[a] |
| $e_{31}$ (C m$^{-2}$) | −0.60[a]<br>−0.58[b] | −0.49[a]<br>−0.36[c]<br>−0.33[d]<br>−0.22[e] | −0.57[a] |
| $e_{15}$ (C m$^{-2}$) | −0.48[b] | −0.3[c]<br>−0.33[d]<br>−0.22[e] | |
| $\varepsilon_{11}$ | 9.0[b] | 9.5[f] | |
| $\varepsilon_{33}$ | 10.7[b] | 10.4[f] | |

**Figure 1.5:** Spontaneous polarization, piezoelectric and dielectric constants of AlN, GaN and InN.

As shown in Figure 1.6, the superposition of both spontaneous and piezoelectric

field generates the total polarization field, that is defined as

$$P = P_{SP} + P_{PE} \tag{1.2}$$

To give a numerical example of the entity of the internal fields in an AlGaN-GaN heterostructure, we refer to the data reported in [34], calculating the electric field caused by polarization inside a Ga-faced $Al_xGa_{1-x}N/GaN/Al_xGa_{1-x}N$ quantum well (see Figure 1.6). To simplify, we assume here that GaN is grown pseudomorphically on AlGaN (i.e. a(GaN)=a(AlGaN)), and that screening effects due to free carriers and surface states can be neglected. In this case, using the coefficients in Figure 1.5 and the Vegard's law, the total polarization field can be calculated to be equal to

$$P = P_{SP} + P_{PE} = (-0.029 + 0.0163x)\ Cm^{-2} \tag{1.3}$$

This polarization generates an electrical field inside the quantum well, that can be calculated as

$$E = \frac{P}{\epsilon_{GaN}\epsilon_0} = (3.6 \cdot 10^6 - 2.1 \cdot 10^6 x)\ Vcm^{-1} \tag{1.4}$$

where $\epsilon_{GaN}$ and $\epsilon_0$ are the dielectric constants of GaN and vacuum respectively. For an AlGaN/GaN heterostructure, therefore, internal electrical field can be higher than 1 $MV/cm$. For an InGaN/GaN system the order of magnitude of the internal electrical field is the same. By means of optical measurements, for example, it has been estimated that an $In_{0.15}Ga_{0.85}N/GaN$ QW system can have an internal field as high as 2.1 $MV/cm$ [35]. Such important field can have large influence on the electrical and optical properties of devices than in other III-V compounds. It is particularly important to mention here the Quantum-Confined Stark Effect, and its consequences on QW emission properties. Details are given in the following section.

### 1.2.2 Quantum-Confined Stark Effect

The strong electrical field present inside a GaN-based heterostructure or quantum-well (like the one shown in Figure 1.6), can give rise to the Quantum-Confined Stark Effect, that generates the redshift of the electroluminescence with respect to the ideal potential well. Hangleiter [36] has described in detail the impact of QCSE on the

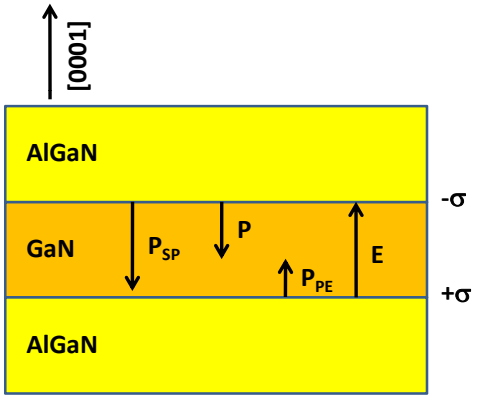



**Figure 1.6:** Polarization (spontaneous, piezoelectric and total polarization) of a $Al_xGa_{1-x}N - GaN$ heterostructure. The interface charge $\sigma$ is caused by the different total polarizations of the GaN and the AlGaN film.

emission properties of nitride-based quantum-wells. As shown in the inset of Figure 1.7, as a consequence of the high electrical field present in the structure, the bands in the quantum well are strongly tilted: as a result, electrons and holes are separated on the opposite corners of the well. This fact leads to the red-shift of the transition energy between conduction and valence band.

This phenomenon has an impact also on the recombination efficiency, since with QCSE electrons and holes are not spatially overlapped (see the inset of Figure 1.7), and recombination probability is reduced. This effect is particularly evident for wide quantum wells, where spatial separation of the carriers can imply a significant increase of lifetimes with subsequent reduction of light emission (see Figure 1.8, from [36], referred to the case of one InGaN/GaN QW). Under high excitation conditions, piezoelectric fields are screened by injected carriers. This leads to a blue-shift of the emission, the amount of which depends on the width of the quantum well and the quantum well composition [37]. Only due to this screening effect, optical gain and lasing of nitride laser structures becomes possible. If there were no screening, the extremely small oscillator strength would prevent such structures from lasing. On the other hand, under lasing conditions, the internal fields are largely screened and the full oscillator strength is almost recovered.

The screening of the internal field can be obtained also applying a bias to the heterostructure. As described by Bunker et al. [38] for an InGaN/GaN structure

(the one that is considered for this thesis), applying a reverse bias to one QW LED a blueshift of the EL peak can be observed, due to the compensation of the internal field (see Figure 1.9): this indicates that the direction of the internal field is set against the reverse bias field. By increasing the reverse bias, there is a cancellation of the piezoelectric field until flat-band conditions are reached and a further increase in the reverse bias inverts the bands and causes the redshift of the emission (see also [35]).

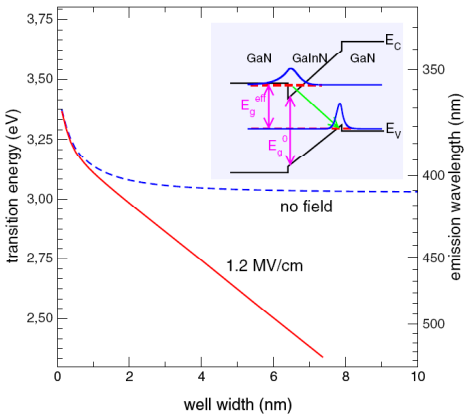



**Figure 1.7:** Effective band gap of quantum wells with and without electric field. A field of 1.2 MV/cm is typical for piezoelectric polarisation in a GaInN/GaN quantum well with 10 % In. Inset: Schematic view of a quantum well with built-in field [36]

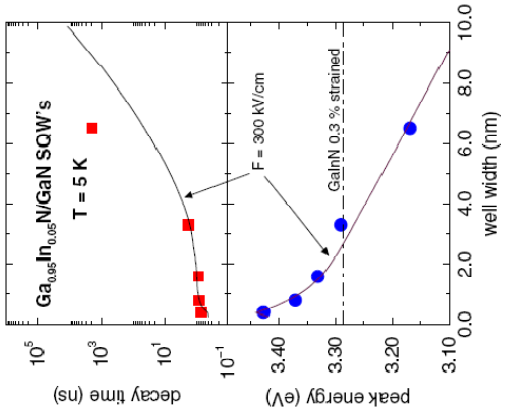



**Figure 1.8:** Measured luminescence emission energy and decay time vs. well width for GaInN/GaN quantum wells [36]

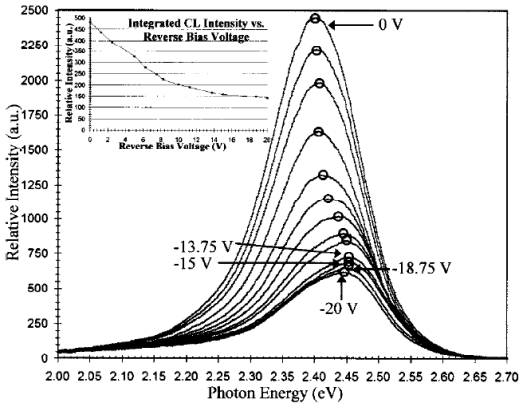



**Figure 1.9:** Room-temperature SEM-CL spectra of the InGaN MQW LED collected at several reverse biases. The CL emission peak blueshifts 52 meV nm before it begins to redshift above 15 V. The circles indicate the peak positions of the CL spectra [38]

## 1.3 Substrates for GaN growth

The first attempts to grow GaN crystals were made in the 1930s, by Johnson [39], who synthetized GaN samples by the reaction of ammonia gas with metallic Ga at high temperatures, 900-1000 °C. Several efforts have been done in the subsequent decades with the aim of growing good quality crystals, but without significant results. Hydrogen passivation and nitrogen vacancies or other unknown defects made it difficult to obtain sufficient p doping. Growth of GaN epitaxial layers using hydride VPE-HVPE was reported in the late 1960s [40]. Interest towards III-nitrides was renewed by the work of Amano and Hiramatsu, in the late 1980s and early 1990s. These authors succeeded in growing good quality GaN films, demonstrating that growth on sapphire substrates is facilitated by the use of an AlN buffer layer deposited at low temperatures [41, 42]. During the last decade several authors have worked on the growth of epitaxial layers of III-nitrides and alloys using both the MOVPE and MBE methods. The most interesting results are summarized in [43, 32] and references therein. In most cases the epilayers have been grown on sapphire and SiC substrates. During the last years, intense research has been done with the aim of obtaining low dislocation density GaN films grown on gallium nitride. A certain interest has been directed also towards the possibility of growing GaN on silicon. In this section we will briefly describe the most important characteristics of the substrates to be used for GaN growth.

### 1.3.1 Sapphire

The first experiments that have achieved efficient growth of gallium nitride used sapphire (single crystal aluminum oxide) as a substrate, despite the high lattice mismatch that this material has with GaN [41, 42, 44, 45] and its relatively low thermal conductivity (0.47 W/cmK at 300 K). Sapphire has been widely used due to *(i)* its large availability, *(ii)* its hexagonal symmetry (compatible with wurtzite-GaN), *(iii)* its stability at the high temperature and pressure levels necessary for MOVPE. Furthermore, large area good quality crystals of sapphire are easily available at low cost ($ 100 for a 2 inch wafer). This factor, together with the important improvements achieved during the years, make this substrate still competitive for the realization of electronic and optoelectronic devices. As cited above, the most critical aspect for the growth of GaN on sapphire is the lattice mismatch between the two materials, that is close to 13 %, and which leads to high dislocation density ($10^{10}$ $cm^{-2}$) [33]. These high defect densities reduce the charge carrier mobility, reduce the minority carrier lifetime, and decrease the thermal conductivity, all of which degrade device performance. Figure 1.10 gives a schematic representation of this mismatch.

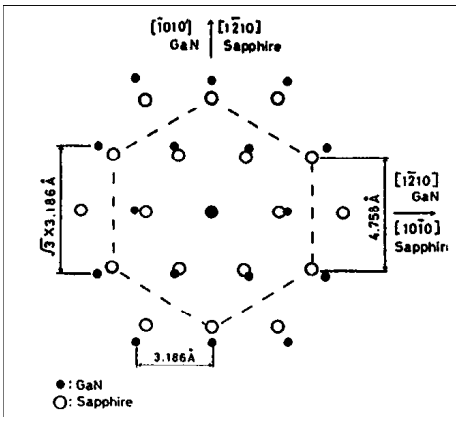



**Figure 1.10:** Schematic representation of in-plane atomic arrangement in the case of 0001 GaN film grown on 0001 sapphire

Qian et al. [46] proposed that the main sources of threading dislocations are the low angle grain boundaries, formed during coalescence of islands at the initial stages of GaN growth. In order to improve the quality of GaN films on sapphire, it became necessary to introduce a buffer layer between the substrate and the GaN film.

The first material that has been used as a buffer was AlN [41, 42]: growing the AlN buffer at low temperatures (usually about 500-550 °C for MOCVD, 400 °C for MBE, [47]), this layer become amorphous. The high temperatures subsequently used for the deposition of GaN (usually about 1100 °C for MOCVD, 700 °C for MBE, [47]) allow the AlN buffer to assume crystalline structure, generating a good base for the deposition of high quality GaN films. The use of the AlN buffer can furthermore improve the electrical properties of the devices, reducing of several (2-3) orders of magnitude the intrinsic carrier concentration of undoped material [43].

Finally, it is worth mentioning that sapphire is electrically insulating, thus, all electrical contacts must be made to the front side of the device, reducing the area available for devices and complicating device fabrication.

### 1.3.2 Silicon Carbide

Extensive work has been done on the growth of III-nitrides on SiC, since it presents many advantages with respect to sapphire. Its lattice mismatch with GaN is only 3.5 %, and with AlN, the mismatch is very small [32]. Furthermore it has an higher thermal conductivity (3.7-4.5 W/cmK) with respect to sapphire, and it is possible to prepare conductive SiC layers, that permit to grow vertical structure devices, thereby simplifying the structure compared to sapphire substrates.

However, SiC substrates are expensive, and gallium nitride epitaxy directly on SiC presents a few problems, due to poor wetting between these materials. This can be remedied by using a low temperature AlN buffer layer [48], but such layers increase the resistance between the device and the substrate. The defectivity of the GaN layer grown in this way decreases as the thickness of the layer increases, due to the annihilation of the stacking faults generated at the interface [49]. Finally, the thermal expansion coefficient of SiC is less than that of AlN or GaN, thus, the films are typically under biaxial tension at room temperature: this fact can limit devices reliability due to increased defect concentration [33].

### 1.3.3 Silicon

Silicon wafers have a low price, and are available in large size due to the mature development of technology. Therefore, an attractive option for the realization of GaN-based devices is to use silicon as a substrate for the growth of gallium nitride. Silicon has good thermal stability under GaN epitaxial growth conditions. The crystal perfection of silicon is better than any other substrate material used for GaN epitaxy and its surfaces can be prepared with extremely smooth finishes. Furthermore, telecommunications scientific community has a certain interest in the possibility of integrating optoelectronic GaN devices with Si electronic devices. [50].

To date, the quality of GaN epitaxial layers on silicon has been much poorer than that on sapphire or silicon carbide, due to large lattice constant mismatch (17 %) and thermal expansion coefficient mismatch (56 %), and the tendency of silicon to form an amorphous silicon nitride layer when exposed to reactive nitrogen sources. For this reason, buffer layers are typically deposited first on the Si substrate to enhance wetting and reduce the reactivity of the Si substrate, and to provide a better lattice constant match between the film and substrate. Furthermore, an amorphous $Si_xN_y$ layer may form at the GaN/Si interface introducing a phase mixture.

### 1.3.4 GaN substrates

During the last decade, many efforts have been done to prepare high quality GaN films to be used as homoepitaxial substrate for the growth of GaN. Homoepitaxial growth of GaN epilayers on free-standing GaN substrates offers a better control over surface morphology, defect density, and doping concentration compared to conventional heteroepitaxial growth. Furthermore, the growth procedure for nitride devices can be greatly simplified as the homoepitaxy process does not require additional steps, such as surface nitridation and low-temperature buffer growth. The defects, impurities, and stress in the epilayers would be greatly reduced, leading to improved performance, yields, and scalability to larger substrates. Devices may further take advantages of the high thermal and electrical conductivity of GaN substrates.

Hydride vapor phase epitaxy (HVPE) has recently evolved as a leading technique for growing bulk GaN materials [51, 52]. Samples grown with this technique have low

dislocation densities in ($2 \cdot 10^7$ $cm^{-2}$), several orders of magnitude below than those in the heteroepitaxial GaN [53]. Therefore homoepitaxial GaN represents an excellent perspective for the future development of high quality devices on gallium nitride.

## 1.4 Doping of gallium nitride

One of the factors that determines the possibility of obtaining high quality GaN-based devices is the capability of efficiently doping semiconductor material. Several factors have limited advances in GaN doping: at first, the absence of an ideal substrate, that implies high material defectivity. As described above, this problem has been partly solved thanks to the improvements of GaN growth technique: the use of a buffer layer, and the possibility of growing GaN on different substrates, SiC and homoepitaxial GaN, have strongly improved the quality of the films, and therefore the incorporation of the doping is easier. A second aspect that has limited the control of GaN films electron and hole doping is the high unintentional n-type doping concentration (typically in the range $2 - 10 \cdot 10^{16}$ $cm^{-3}$, which is generally attributed to the presence of nitrogen vacancies. Finally, the fact that the most commonly used acceptor dopant, Mg, can be easily compensated by hydrogen, has limited the advances in the development of high quality p-GaN films, and subsequently the realization of p-n diodes and LEDs. In this section we will summarize the properties of n and p-type dopant used for GaN, and give an indication of the open problems in this field.

### 1.4.1 n-type doping

As stated above, one of the problems of efficiently controlling the n-type doping of GaN is represented by the high un-intentional donor concentration present in gallium nitride. This problem has been detected in the 1960s by Maruska [40], and initially attributed to native defects. More recent studies [54, 43] have ascribed this effect related to the presence of nitrogen vacancies in the semiconductor. Further studies [55, 56], have indicated that intrinsic n-type doping is most likely related to the presence of unintentional impurities such as oxygen and silicon. These impurities are calculated to be shallow donors with high solubilities, and can therefore react with semiconductor material generating n-type conductivity.

Thanks to the advances obtained during the last dacade, by using advanced MOCVD is now possible to grow GaN layers with low intrinsic carrier concentration [43]. Therefore is has become possible to accurately control the n-type doping in GaN sheets. Nakamura has described in detail the possibility of using germanium and silicon as doping sources for GaN [43]. Germanium is a shallow donor in GaN with an activation energy for ionization of 19 meV, which is almost the same as for silicon [57]. Germanium doping is incorporated during growth by the reaction between $GeH_4$ and trimethilgallium and ammonia. In this way it is possible to achieve germanium concentration as high as $2 \cdot 10^{19}\ cm^{-3}$ [43].

On the other hand, silicon doping is obtained by a similar reaction, using silane ($SiH_4$) as a precursor. $Si_{Ga}$ in GaN is a shallow (0.02, as reported by Bougrov et al. in [58, 57]) effective-mass donor. It is an energetically very stable configuration, since the nitrogen substitutional site and the interstitial configurations are energetically unfavorable. This can be understood by noting that silicon has an atomic radius very similar to gallium. Thus, while easily fitting in on a Ga site, it causes a large strain if it replaces a small N atom or goes on an interstitial site [56]. For this reason, as well as for the higher efficacy of the silicon incorporation process with respect to germanium [43], silicon is the most widely used donor dopant for GaN.

### 1.4.2 p-type doping

As described above, systematical research on gallium nitride begun in the 1960s. The first technological problem that has delayed the development of GaN-based LEDs and lasers has been the difficulty of obtaining high quality p-type GaN layers. For many years it was not possible to achieve p-type doping in GaN, due partially to the often high residual n-type background resulting from nitrogen vacancies or Si or O impurities and to the high ionization energy level of most acceptor dopants. The first attempts of achieving a p-type doping have been done using several elements, like lithium, sodium, potassium, beryllium, zincum, calcium and magnesium. The behavior of the different acceptors have been compared, using two parameters as a measure of the efficient acceptor incorporation: the strength of chemical bonding between the acceptor and its neighbors (which can be assessed by comparison with existing compounds) and the

atomic size match between the acceptor and the host atom for which it substitutes. Tests have demonstrated that magnesium is the best choice, and for this reason, during the last decade many efforts have been done for the realization of stable Mg-doped GaN layers [59].

The first experiments that have shown the possibility of obtaining p-GaN layers have been done by Amano and Akasaki [41, 42, 43]. p-GaN layers were grown by means of Metal Organic Chemical Vapour Deposition (MOCVD), and using magnesium as acceptor. After growth, the Mg-doped layers had high resistivity, due to the acceptor passivation by grown-in hydrogen (generation of Mg-H bonds). Amano et al. [60] demonstrated the possibility of breaking Mg-H bonds by means of Low Energy Electron Beam Irradiation (LEEBI) treatment. In this way it was possible to obtain hole concentration of $2 \cdot 10^{16}\ cm^{-3}$, while the resistivity values were in the order of $35\ \Omega \cdot cm$. These values were too low the realization of blue LEDs or lasers: an higher hole concentration was needed to efficiently inject carriers in the active region of the devices, and the resistivity of the layer had to be lowered in order to decrease devices operating voltage and joule-heating effects.

A few years later, Nakamura et al. (see [43] and references therein) demonstrated that it is possible to obtain low-resistivity p-GaN layers using Mg as a dopant, and submitting the as-grown GaN layers to a thermal annealing in $N_2$ atmosphere (at 700 °C). In Figure 1.11 it is shown the resistivity of GaN films as obtained after post-growth annealing in $N_2$ atmosphere [43]: it can be noticed that the as-grown material had an high resistivity, in the order of $10^6\ \Omega \cdot cm$, while after treatment at 700 °C it was possible to obtain resistivity values as low as $2\ \Omega \cdot cm$.

Youn et al.[61] demonstrated that there is an optimum annealing temperature, which results in the highest hole concentration, depending on the existing defect structures in Mg-doped GaN layers. They observed that the hole concentration was constant with annealing temperature above 650 °C, but it subsequently decreased at much higher annealing temperatures. This phenomenon was interpreted as the generation of nitrogen vacancies compensating Mg at higher annealing temperatures. The possibility of defect generation or other thermal effects are also important factors to be taken into account in the discussion of the activation process of Mg acceptors.

The effect of thermal treatment is reversible. By heating the activated layers in

hydrogen atmosphere, the Mg atoms are deactivated (see Figure 1.12). More recently Gotz et al. [62] have made extensive Hall measurements on Mg-doped GaN epilayers grown by MOCVD on sapphire substrates. They also activated the Mg impurity by thermal annealing and confirmed that on thermal annealing the resistivity decreases by more than 6 orders of magnitude.

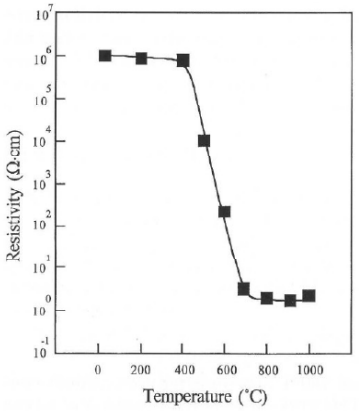



**Figure 1.11:** Resistivity of GaN-Mg layers as a function of annealing temperature in $N_2$ ambient

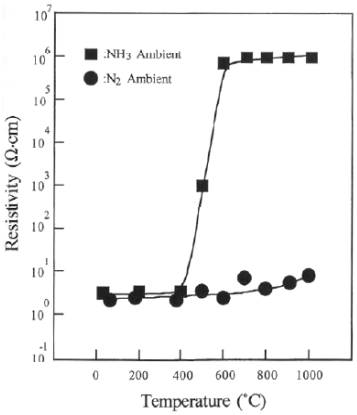



**Figure 1.12:** Variation of the resistivity of GaN-Mg layers submitted to annealing in $NH_3$ and $N_2$ ambient

Other authors (see [63] and references therein) indicated that the presence of minority carrier injection can help the activation process. They fabricated GaN p-n diodes using Si and Mg dopants. The layers were grown by MOVPE. As deposited Mg-doped layers were insulating. Different diodes were annealed under different

biasing conditions. Under forward bias, the resistance of the Mg-doped layer (and the differential resistance of the diodes, see Figure 1.13) was found to decrease at 300 °C, until saturating at a value five orders of magnitude smaller at 400 °C. Further details on the role of hydrogen will be given in a subsequent section.

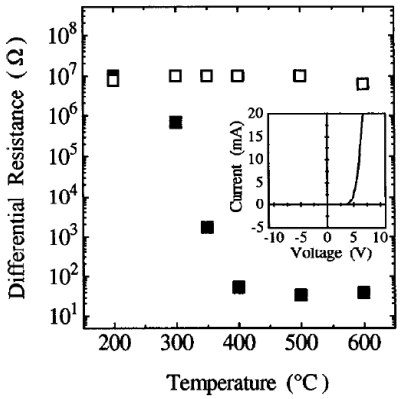



**Figure 1.13:** The differential resistance at 10 V of the diodes as a function of the temperature of the annealing under forward bias (solid squares) and in the open-circuit configuration (open squares)

Another process that limits the characteristics of Mg-doped GaN layers is self-compensation caused by the formation of a deep donor, $MgGa - V_N$, namely a nearest-neighbor association of Mg acceptor with nitrogen (N) vacancy. The nitrogen vacancy, $V_N$, acts as a donor for GaN [64]: the $V_N$ and $Mg$ acceptors, which are oppositely charged, attract each other, tending to form $Mg_{Ga-V_N}$ [65]. In order to solve this problem, it has been proposed to introduce nitrogen in the growth chamber: in this way it become possible to fill the vacancies and to increase hole concentration.

As described above, many technological improvements have made possible the realization of high quality Mg-doped GaN films. As a result, it has been recently demonstrated that it is possible to obtain Mg-doped GaN layers with ever decreasing resistivity and high hole concentration (above $5 \cdot 10^{17}\ cm^{-3}$, see for example [66]), indicating that the technology of p-GaN growth is now mature for the development of efficient LEDs and lasers.

The activation energy of the magnesium acceptor is quite high, in the range 160-200 meV [32]. This fact, together with the compensation of Mg-dopant, imply that at room temperature the effective hole concentration ($N_p$) is well below the total

magnesium concentration measured by SIMS. An analysis of the relation between the two parameters has been presented by Weimar et al. [67]: results are summarized in Figure 1.14 and 1.15, that show the variation of specific p-GaN resistance and of the hole concentration with increasing SIMS acceptor concentration. The increase of the specific resistance (see Figure 1.14) of the p-GaN-layer is due to the decrease of hole concentration with increasing Mg-doping concentration, that can be attributed to the self-compensation effect in MOVPE-grown Mg-doped p-GaN layers [68]. In such GaN-layers, the concentration range around $2 \cdot 10^{19}\ cm^{-3}$ is a limit for Mg incorporation as shallow acceptors. Further Mg-atoms form deep donors which are believed to be Mg - Nitrogen vacancy complexes. Those deep donors compensate the Mg-acceptors resulting in the decrease of free holes and therefore the increase of the specific resistance.

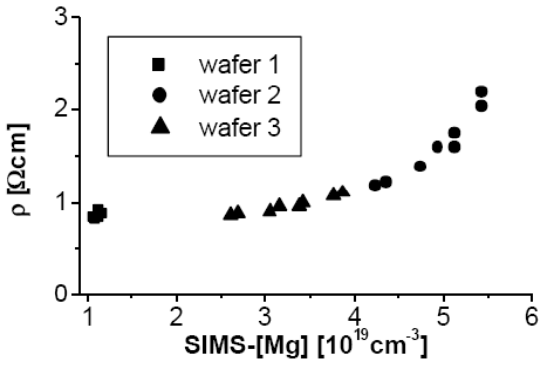



**Figure 1.14:** Specific p-GaN resistance versus Mg-concentration [67]

### 1.4.3 Role of hydrogen in GaN

Hydrogen is contained in most of the reagents and liquids used in the growth, annealing, and processing of semiconductors, and a great deal of attention has been focused on the effects of hydrogen incorporation in Si, GaAs, SiC, and other materials. It is known that molecular hydrogen is basically electrically and optically inactive in all semiconductors, and that it has a low diffusivity once formed inside the semiconductor [69]. On the other hand, atomic hydrogen (both in the $H^0, H^+, H^-$ form, depending on the position of the Fermi level) diffuses rapidly even at low temperatures (25-250 °C) and bind with dangling or defective bonds associated with point or line defects,

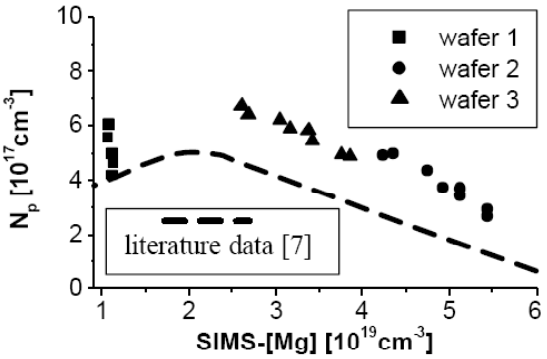



**Figure 1.15:** Hole concentration versus Mg-concentration [67]

and can also form neutral complexes with dopants, thus compensating the effect of dopant, as expressed by

$$D^+ + H^- = (DH)^0 \tag{1.5}$$

$$A^- + H^+ = (AH)^0 \tag{1.6}$$

where $D^+$ and $A^-$ represent ionized donors and acceptor respectively. These reactions manifest themselves as increases in resistivity of the semiconductor, and an increase in carrier mobility as ionized impurity scattering is reduced. A typical signature of an unintentional hydrogen passivation process is a reduction in doping density in the near-surface region ($\leq \mu m$) due to in-diffusion of atomic hydrogen from the liquid or gas in which the sample is immersed.

The key quantity that determines the properties of hydrogen is the formation energy, i.e., the energy needed to incorporate H in the host. Details on the definition of this parameter can be found in [70]. Using Density Functional Theory (DFT) it has been shown that hydrogen acts as a donor ($H^+$) in p-type GaN and as an acceptor (H-) in n-type GaN, always counteracting the prevailing conductivity (see Figure 1.16, that shows the calculated formation energy for H in GaN). In p-type material hydrogen is most stable in the positive charge state, explaining the experimentally observed passivation of acceptors. Similarly, $H^-$ in n-type material passivates donors [70].

Metal-organic chemical vapour deposition (MOCVD) of GaN occurs by the reaction

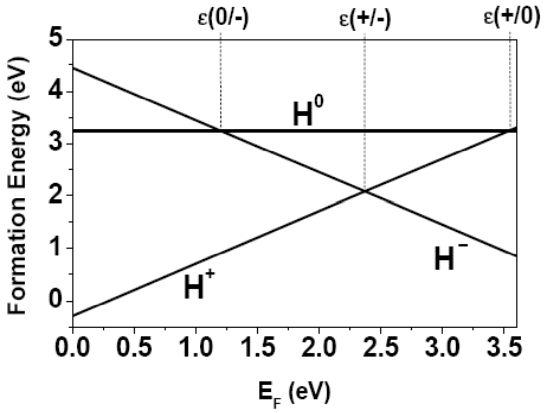



**Figure 1.16:** Calculated formation energies of interstitial hydrogen in GaN in different charge states, referenced to the energy of an $H_2$ molecule [70]

$$(CH_3)_3Ga + NH_3 \rightarrow GaN + CH_4 \uparrow + H_2 \uparrow \tag{1.7}$$

While the growth temperature is high (around 1040 °C), there is a long cooldown under a $NH_3$ ambient during which atomic hydrogen can easily diffuse into p-GaN, thus interacting with the acceptor atoms. A proof of the fact that hydrogen is trapped by the acceptor atoms is given by the fact that in as-grown MOCVD samples the concentration of hydrogen is proportional to the concentration of magnesium in the semiconductor layers (see [71] and references therein). A minor hydrogen incorporation can be obtained if growth is done by means of MBE, due to the fact that in this case $N_2$ is used as nitrogen source instead of $NH_3$.

As described above, the first method that has been used for the reactivation of the magnesium acceptor has been LEEBI, proposed by Amano [60]. However, it has been demonstrated that carrying out an annealing at high temperature levels (700 °C) is more effective for breaking the $Mg - H$ bonds [43], according to reaction

$$(Mg - H) \longleftrightarrow Mg^- + H^+ \tag{1.8}$$

The high temperature necessary for the breaking of the $Mg - H$ bonds has been justified demonstrating that there is a surface-barrier effect that limits H release during postgrowth thermal activation of H-passivated Mg acceptors [72]. As a result of the annealing process, the amount of hydrogen in the GaN layer is reduced (see Figure 1.17), and the mobility and hole concentration are increased. On the other

hand, the concentration of magnesium in the sample is stable during the annealing, and this demonstrates the stability of the acceptor atoms. However, a substantial amount of hydrogen remains in the material, probably bound at defects or internal surfaces. This residual hydrogen may give rise to effects such as current gain drift in transistors, or a dependence of apparent material resistivity on the measurement current in Hall measurements because of minority carrier reactivation of passivated acceptors.

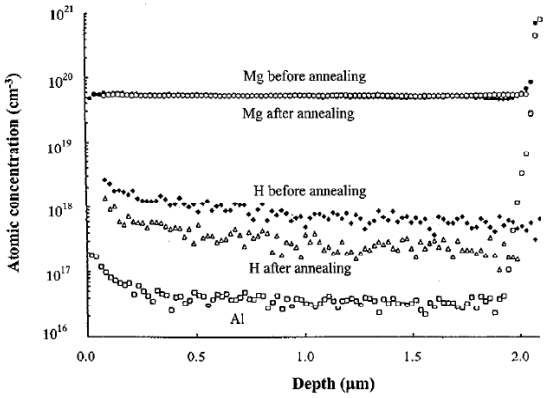



**Figure 1.17:** SIMS depth profile of MOCVD grown GaN-Mg before and after 700 °C, 60 min anneal in $N_2$ [71]

Subsequent investigations have evaluated the infuence of the atmosphere used for the high temperature annealing on the efficiency of breaking of the Mg-H bonds. In particular, the effect of annealing in nitrogen and oxygen atmosphere have been compared [72]. The results of this analysis have confirmed the surface-barrier effect that has previously been shown to limit H release during postgrowth thermal annealing. It has been shown that $O_2$ is far more effective than $N_2$ in accelerating the initial stages of release, but the enhancement is subsequently slowed by oxidation, a potential issue for the use of $O_2$ anneals in device processing.

Also the flow of minority carriers inside the p-layer can have a benefic effect and break the Mg-H bonds. This fact has been demonstrated by Pearton and Lee [73, 71]: they have analyzed the behavior of GaN-based p-n junctions submitted to annealing at 175 °C. Thermal treatment was found to induce no significant modification of the doping concentration, in the case that no bias was applied to the devices during annealing. On the other hand, they demonstrated that if p-n junction

were forward-biased during storage at 175 °C, the magnesium dopant concentration increased. After one hour of treatment almost all the p-type dopant was found to be re-activated. This phenomenon is effectively related to the flow of the carriers in the junction, since they have demonstrated that during test junction temperature was below 200 °C, and thermally-activated breaking of deep Mg-H bonds takes place only for higher temperatures [71] under no-bias conditions.

A more accurate description of the interaction between magnesium and hydrogen during forward bias has been given by Myers and Wright [74, 75, 76, 8, 72]. By applying differential equations for the concentration profiles of H species, charged dopants, and carriers with simultaneous solution of Poisson's equation, they simulated the activation/passivation process, finally demonstrating that interstitial $H_2$ is the state of the $H$ resulting from such activation. This conclusion was supported by good agreement between the predicted and observed onset temperatures for repassivation under open-circuit annealing, and by experimental tests carried out on H-containing p-n junctions. Myers and Wright therefore demonstrated that the minority flow-induced re-activation of magnesium can not be only related to breaking of Mg-H bonds, since if this was the case, free $H^+$ ions could immediatly find new acceptors to bind with. They finally demonstrated that the minority-carrier injection into the p-type region under bias leads ultimately to the formation of neutral interstitial $H_2$, that remains in the semiconductor material, according to reactions

$$MgH \rightharpoonup Mg^- + H^+ \quad (Thermal\ dissociation) \tag{1.9}$$

$$H^+ + e^{-*} \rightharpoonup H^0 \quad (Hot\ electron\ capture) \tag{1.10}$$

$$H^0 + e^{-*} \rightharpoonup H^- \quad (Hot\ electron\ capture) \tag{1.11}$$

$$H^- + H^+ = H_2 \tag{1.12}$$

where it is supposed that the breaking of the Mg-H bonds is due to the presence of hot electrons. This assumption is made bacause experimental data show that dopant re-activation does not depend on observed depth: threfore thermal electrons can not be involved in this process, since they recombine close to the junction and do not reach higher depths.

The process described in Equation 1.9 - 1.12 is reversible, by means of an annealing. In this case the reactions are

$$H_2 \rightarrow H^+ + H^- \quad (Thermal\ dissociation) \tag{1.13}$$

$$H^- + h^+ \rightarrow H^0 \quad (Hole\ capture) \tag{1.14}$$

$$Mg^- + H^+ \rightarrow MgH \tag{1.15}$$

$$Mg^0 + H^0 \rightarrow MgH \tag{1.16}$$

The processes described in Equation 1.9 - 1.12 involve reaction or diffusion energy barriers, implying a need for thermal excitation. This property may be responsible for the observed necessity of somewhat elevated temperatures for Mg activation to occur under forward bias [71, 74].

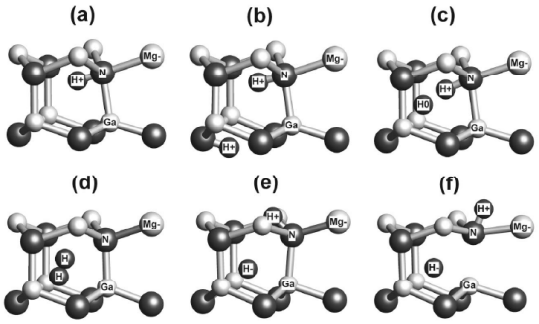



**Figure 1.18:** Atomic configurations relating to LEEBI dissociation, as calculated using density functional theory [76]

To achieve the re-activation of the Mg-bonds at room temperature one can use LEEBI treatment [76]. The efficacy of this treatment is due to the high energies of the carriers (25-30 keV), that are sufficient for the breaking of the Mg-H bonds. Dissociation can lead to the generation of $MgH_2$ complexes, that behave as shallow acceptors. A description of the dissociation of MgH bonds and subsequent generation of $MgH_2$ complexes is given in Figure 1.18. The stable MgH center in (a) is dissociated by the impinging energetic electrons, and the resultant detached $H^+$ is envisioned as migrating into the vicinity of another $MgH$ (b), where an electron capture yields $H^0$

(c), and a final electron capture enables the formation of $MgH_2$ (d). During subsequent thermal dissociation in the absence of electron injection, the dissociated $H^+$ moves through a saddle point (e) to a local energy minimum (f), and the process is rendered irreversible through hole capture by the residual $H_2$ It is important to remind here that with LEEBI it is possible to dissociate only 1/2 of the Mg-H complexes present in the semiconductor material. This is possibly due to the fact that $MgH_2$ complex is subject to electron-beam dissociation as well as the $MgH$ center, so that the system approaches a dynamic balance between the opposing reactions.

## 1.5 Ohmic contacts on GaN

GaN and related III-V nitrides have been applied to realize optoelectronic devices, such as light emitting diodes, ultraviolet photodetectors, and laser diodes. They have been employed also to produce high-power microwave devices, such as modulation doped field-effect transistors. Low resistance ohmic contacts are essential elements of these devices. In this section we will give a brief review of the most common material and structure choices for the realization of good ohmic contacts on GaN.

### 1.5.1 Contacts on n-GaN

The Schottky barrier height of a contact on n-GaN is defined as

$$q\phi_{SM} = q(\phi_M - \chi_S) \tag{1.17}$$

where $\phi_M$ is the work function of the metal, and $\chi_S$ is the electron affinity of the semiconductor. For n-GaN, the room temperature energy band-gap $E_G$ is 3.39 eV, and the electron affinity $\chi_S$ is 4.11 eV.

As evident from Table 1.2, the work function $\phi_M$ of most of the metal yields quite large Schottky barrier height $\phi_{SM}$. So, carrier transport through these contacts due to pure thermionic emission is rather remote. A similar effect takes place in the case of p-type gallium nitride. Therefore, in order to obtain low-resistivity ohmic contacts on GaN, surface doping concentration is usually increased, in order to enhance tunneling components.

Actually, both tunneling and thermionic emission contribute to carrier flow in an ohmic contact, in different proportions. Taking into account the case of n-GaN, with heavy doping, increasing number of new donor-type energy levels are created underneath the conduction band edge. Under these circumstances, the donors are so close together that the donor levels are no longer discrete and noninteracting energy levels. These are rather degenerate merging together to create an impurity band, and causing band-gap narrowing (BGN) of the conduction band. Obviously, the BGN is the highest near the M/S interface, and the lowest in the bulk, where doping concentration is lower. The effective M/S barrier height $\phi_B$ is thus reduced, as shown schematically in Figure 1.19. The sharp tip of the conduction band edge in contact with the metal

| Metal | Work function (eV) |
|---|---|
| Ga | 3.96 |
| Al | 4.25 |
| Ti | 3.95 |
| Ni | 4.50 |
| Au | 4.30 |
| Ta | 4.25 |
| Pd | 5.12 |
| TiN | 3.74 |
| TaN, ZrN, VN, NbN | $\geq 4.00$ |

**Table 1.2:** Work-function of several metals

is particularly lowered, and the new barrier height $\phi_{BE}$ becomes $\phi_{BE} = \phi_B - \Delta E_G$, where $\phi_B$ is the barrier height without BGN, and $\phi_{BE}$ is the barrier height with BGN.

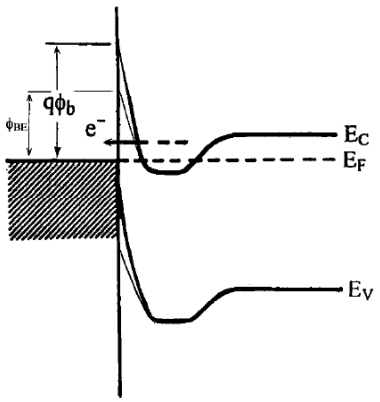



**Figure 1.19:** Schematic diagram showing the reduction of the M/S barrier height due to band-gap narrowing. Note that $\phi_B$ is the M/S barrier height without band-gap narrowing, and $\phi_{BE}$ is the M/S barrier height with band-gap narrowing.

According to thermionic emission theory, the resistivity of the M/S contact depends only on the barrier heigth, according to

$$\rho_c = \frac{k_B}{qTA^*} e^{\frac{q\phi_{BE}}{k_B T}} \tag{1.18}$$

where $A^*$ is the Richardson constant.

On the other hand, the resistivity due to tunneling is

$$\rho_c = \frac{k_B}{\pi A^* T^2} sin\left(\pi C_1 k_B T\right) e^{\frac{q\phi_{BE}}{E_{00}}} \tag{1.19}$$

where

$$E_{00} = \frac{\hbar q}{2}\sqrt{\frac{N_D}{m_n^* \epsilon_s}} \tag{1.20}$$

$$c_1 = \frac{1}{2E_{00}}\left(\frac{4\phi_{BE}}{V_p}\right) \tag{1.21}$$

$$V_p = \frac{k_B T}{q} ln\left(\frac{N_C}{N_D}\right) \tag{1.22}$$

$N_C$ is the effective density of states for electrons in the conduction band, $\hbar = h/2\pi$, and $m_n^*$ is the effective electron mass in the conduction band of n-GaN.

It has been recently demonstrated [77] that, depending on how much $\phi_B$ is lower than $\phi_{SM}$ , thermionic emission, together with tunneling, can contribute to low contact resistivity even in the tunnel contacts. If the surface treatment is very good, and the metal parameters (e.g., metal thickness, metal deposition temperature, metal work function, metal combination, etc.) are optimum, then $\phi_B$ may be significantly lower than $\phi_{SM}$, thus leading to a significant contribution also of thermionic emission to overall conduction. Therefore, the properties of the material and surface must be carefully controlled, in order to achieve a good definition of the transport properties of the M/S system.

To produce low resistivity metal/n-GaN contacts, a number of design requirements must be satisfied. As described in [77], alloyed ohmic contacts should have a barrier layer (see Figure 1.20), that must be metallic, and located immedialtly close to the n-GaN layer. This layer should have a low work function, and is called barrier because it acts as a barrier against the diffusion of the other metal layers towards n-GaN. For ohmic contacts to n-GaN, TiN, TaN, ZrN, CoN, etc., represent a good choice, because they can be conveniently formed by the solid phase chemical reaction of the barrier layer metal (for example Ti, Ta, Zr, Co) the N atoms of n-GaN. The formation of the barrier layer by this procedure can have another merit. The outdiffusion of N atoms from n-GaN to form these metallic generates N vacancies, that are known to act as n-type dopant atoms [64], that can increase tunneling probability.

Preferably the contact should have also an overlayer metal. This overlayer metal can play the catalytic role as a sink for N atoms into the barrier layer metal enhancing solid phase chemical reaction between the nitrogen atom and the metal atoms of the barrier layer. Aluminum may be a good overlayer metal as long as it does not create a large work function alloy nor a thick wide band-gap material upon alloying.

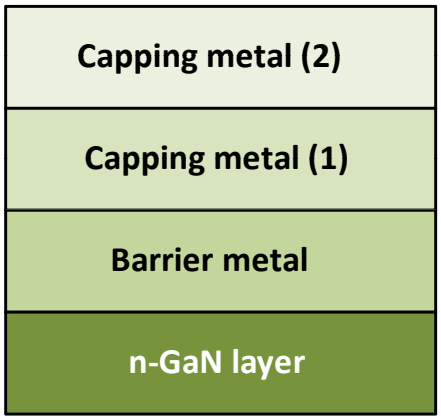



**Figure 1.20:** Schematic diagram showing barrier layers, overlayers, and cap layers as elements of the described design scheme

Another factor must be taken into account: the barrier layer metal and the overlayer metal may have high propensity for oxidation. Therefore, one or more cap can be needed, to ensure the stability of the system. In general the metal layers described above do not represent a stable system: a solid phase interfacial reaction must occur upon Rapid Thermal Annealing (RTA) causing metal interdiffusions. The reaction products will comprise thin low resistance, low work function metallic barriers and a number of robust, thermally stable intermetallic alloys on the top of the barrier layer. An optimization of the RTA time, the RTA temperature, and the metal thicknesses would be very crucial to ensure the formation of the most desirable, robust, and thermally stable intermetallic alloys, namely, the barrier layer and the cap layers. Today, it is widely believed that the formation of good ohmic contacts to n-GaN necessitates tunneling. Tunneling through metal/GaN contact is possible if n-GaN is very heavily doped with significant conduction band bending near the M/S interface. The semiconductor region at the interface thus becomes very thin allowing an unhindered flow of electrons via tunneling. This leads the resistivity of the contact to be very low. An example of this is the contact with resistivity on the order of

$10^{-9}$ $\Omega cm^2$ obtained for the n-GaN doping $N_D = 10^{20}$ $cm-3$ [78]. The real challenge to achieving low resistivity contact is, however, to use moderately doped semiconductors. Many devices do indeed need low resistivity contacts without the need of heavy doping. Therefore, important efforts have been done in order to improve the properties of ohmic contacts on n-GaN, working on the metalization and process scheme, rather than on the increase of n-type doping. Au and Al single metal contacts to n-GaN and nonalloyed Au/Ti and Al/Ti were found to have contact resistances of $10^{-3}$ to $10^{-4}$ $\Omega \cdot cm^{-2}$ (see [69] and references therein). For high temperature electronics applications, or for high reliability, it is preferable to employ refractory metal contacts such as W and $WSi_x$ [69]. Moreover, the contact resistance could be reduced if lower band gap In-containing alloys or InN were used as contact layers on GaN, much as in the case of InGaAs on GaAs. However, the In-based nitrides are less thermally stable than GaN, and a trade off between contact resistance and poorer temperature stability must be established.

However, among the many contact metallization schemes reported in the literature, Ti/Al-based contacts are the most widely used for Ohmic contact formation to n-GaN and n-AlGaN, being the most common metal scheme Ti/Al/Ti/Au [79]. As described above, Ti is reactive, and participates in the solid-state reactions at interface with the nitride, yielding thin $TiN$ or $AlTi_2N$ layers, responsible for Ohmic nature [80]. However, despite providing low contact resistances, Ti/Al-based Ohmic contacts exhibit significant limitations such as the formation of low-melting $AlAu_4$ phase, responsible for lateral flow during alloying at high temperatures (around 900 °C) [81]. Under these conditions Ti and Al diffuse, through the contact surface and towards semiconductor interface, degrading contact performances. In the last years, strategies for improving Ohmic contacts have included the employment of high melting point metals such as Mo, V, W, $WSi_x$, and Ir, acting as a metal barrier, showing very promising results [82]. These metals confer more thermal stability and reproducibility than conventional ones. Recent innovating metal schemes have confirmed the role of the barrier layer cited above: for instance, it has been demonstrated that using a Ti-W barrier, it is possible to achieve contact resistance as low as 0.29 $\Omega \cdot cm$ [83].

### 1.5.2 Contacts on p-GaN

One of the factors that have limited the development of reliable GaN-based light-emitting diodes and lasers has been the difficulty of obtaining good ohmic contacts on p-GaN. In the first experiments, due to the poor specific contact resistance, the metalization self-heating was strong, thus leading to metal migration through threading dislocations and eventual shorting of the junction. While on one hand the efforts aimed at reducing the dislocation density (i.e. with epitaxial lateral overgrowth structures) have leaded to an improvement of devices lifetime, on the other hand the study of the properties of the ohmic contacts on p-GaN has leaded to important improvements of devices technology.

The factors that limit specific contact resistance of ohmic contacts on p-GaN are:

- The absence of a metal with a sufficiently high work function (the band gap of GaN is 3.4 eV, and the electron affinity is 4.1 $eV$, but metal work functions are typically $\leq 5eV$)
- The relatively low hole concentrations in p-GaN due to the deep ionization level of the Mg acceptor (170 meV)
- The tendency for the preferential loss of nitrogen from the GaN surface during processing, which may produce surface conversion to n-type conductivity

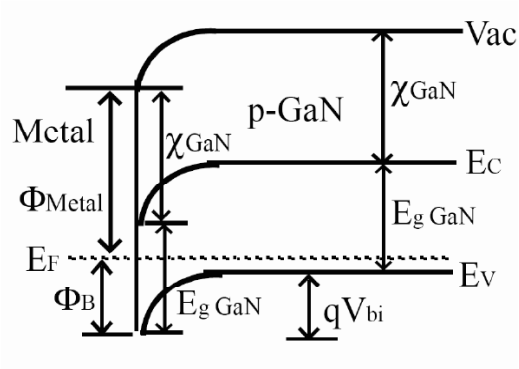



**Figure 1.21:** Schematic band diagram of a metal/p-type semiconductor junction

Typical Ohmic contacts to p-GaN are based on high work function metals, such as Pd, Pt, Ni, or Cr, with an overlayer of Au. These are annealed at 400-750° C

to increase the hole concentration of the surface through the depassivation of Mg-H complexes and formation of Ga vacancies through reaction with Au. The study of the temperature dependence of the electrical characteristics of these contacts has shown that conduction processes are dominated by tunneling [67]. Typical transmittance of this kind of contacts is around 60 %-75 % [84].The fundamental electronic properties of these contacts depend on the atomic arrangement and on the nature of chemical bonds at the metal/semiconductor interface. Specific contact resistances of $10^{-2} - 10^{-4}\ \Omega cm^2$ are obtained by annealing at 450-650 °C [85]. These contacts have stability problems at high temperature. In general, degradation of Ni/Au contacts upon aging has been demonstrated: degradation has been ascribed to the formation of an islanded contact morphology, to the formation of reactions with the GaN resulting in a modification of the doping profile, and to the intermixing of Ni and Au, leading to the oxidation on the rough Ni surface and an increase of the series resistance (see [86] and references therein). Furthermore, Omiya et al. [87] demonstrated that the initial Au/Ni/GaN structure transforms to Ni/Au/GaN with a rough Ni surface after annealing at 600 °C.

A way to prevent excessive intermixing and contact morphology degradation is to use a high-melting-point diffusion barrier in the contact stack. For instance, $TiB_2$, with a melting temperature of 3000 °C, electrical resistivity 28 $\mu\Omega cm$ and thermal conductivity 26 $Wm^{-1}K^{-1}$, and heat of formation comparable to those for silicides or nitrides, can be used as a diffusion barrier [86]. Howevewer, the transparency of such materials is low: they can be effectively uses in p-side down LEDs, and have a great impact in high power nitride electronic devices, where improved stability over Ni/Au is mandatory.

As described above, the Au-based contacts generally have poor thermal stability, leading to poor device reliability. An improvement in contact technology can be given by the use of Au-free structures. On choice is represented by thin oxides, for example Indium Thin Oxide (ITO). ITO films can have high transparency 90 % in the visible spectrum and low electrical resistivity ($\ll 5 \cdot 10^{-4}\ \Omega cm$). The ITO film can also provide high carrier concentration ($10^{20} - 10^{21}\ cm^{-3}$) and applicable mobility $25 - 50\ cm^2/Vs$ [88]. Therefore, it has been demonstrated that depositing Ni and ITO films on p-GaN by thermal evaporation and RF magnetron sputtering at room temperature respectively, a 87 % normalized transmittance of Ni/ITO film can be

reached, as well as a specific contact resistance of $5 \cdot 10^{-4}$ $\Omega cm^2$ [84]. Optical properties of these contacts are better with respect to Ni/Au ones, but are limited by the high refractive index (2.1-2.5 at 405 nm of GaN-related materials and indium tin oxide), resulting in the escape cone with a small angle for the emitted light, and so causing most of the light to experience total internal reflection. To enhance the light extraction efficiency, several methods, such as laser lift-off, GaN surface roughening, and contact layer patterning, have been introduced (see [89] and references therein). In particular, contact-layer patterning was found to be efficient in enhancing light extraction by inducing the photonic crystal effect. In flip chip LEDs (FCLEDs), it is necessary to have an highly reflective p-side metal layer. It has been shown that using a metal different from Ni/Au as a reflector, the optical properties of the LEDs can be significantly improved [90]. Among metallic reflectors, Ag is known to be the most promising material for GaN-based FCLEDs, because it gives high reflectivity in visible light and forms good ohmic contacts at temperatures below 250 °C. However, the adhesion of Ag to p-GaN is poor and Ag becomes agglomerated when annealed at temperatures of 300 °C, leading to the degradation of ohmic properties and consequently the lowering of device performance. This means that use of a single Ag contact itself may lead to the poor optical device performance and reliability. Several research groups have investigated different metallization schemes to settle the problems associated with the single Ag contact. For example, Hibbard [91] used oxidized Ni/Au bilayer contacts to obtain high-quality ohmic contacts for FCLEDs and reported that surface light emission of 70 % was obtained from the LEDs with the Ni/Au/Ag p-contact layers, which is higher than that from LEDs with the annealed Ni/Au contacts. Kim [92] introduced an indium tin oxide (ITO) layer between a Ni/Au bilayer and a Ag reflector, and showed that after annealing at 500 °C in oxygen ambient, the contacts produced reflectance of 82.5 % at a wavelength of 460 nm. Recently, Song [93] investigating a Zn-Ni solid solution/Ag p-type ohmic contacts for FCLEDs, showed that the scheme produced specific contact resistance of $10^{-4}$ $\Omega cm^2$ and reflectance of 90 % at 460 nm, when annealed at 530 °C.

## 1.6 Summary

In this chapter we have briefly summarized the characteristics of GaN-based semiconductor systems. Particular importance has been given to the aspects that influence the properties of GaN-based systems to be used in optoelectronic applications. Details on *(i)* the band structure of GaN, *(ii)* the existence of spontaneous and piezoelectric polarization fields, *(iii)* the most common substrates used for GaN growth, *(iv)* the problems related to GaN doping, *(v)* the role of hydrogen in limiting the electrical characteristics of p-doped layers, *(vi)* the solutions for the realization of good ohmic contacts have been given. These information are necessary for the understanding of the subsequent chapters.

# Chapter 2

# Properties of optoelectronic devices

In this chapter we summarize the most significant properties of the optoelectronic devices (LEDs and lasers) that must be recalled for the understanding of the following analysis. In particular, we will describe:

- the mechanisms that rule carriers radiative and non-radiative recombination in a semiconductor
- the electrical characteristics of the diode and their most significant non-idealities
- the capacitance-voltage characteristics of the diode, the method for the extrapolation of the apparent charge distribution, and the typical C-V profiles of MQW structures
- the rate equation, the optical power vs input current characteristics, and the luminescence spectrum of the LED

## 2.1 Recombination of carriers

In a semiconductor, the total carrier recombination rate is determined by several physical processes. In order to be transferred from conduction band to valence band, electrons need to transfer their excess energy to other particles (electrons, phonons, photons). Recombination processes can be radiative (and determine the emission of a photon) or nonradiative (no photon emission). The recombination processes that are most important for LEDs and lasers are described in the following.

### 2.1.1 Radiative recombination

In bulk material, the generation of photons can be

- spontaneous, if a carrier in an excited state (e.g. electron in conduction band) undergoes a transition to the ground state and emits a photon (see Figure 2.1, left)
- stimulated, if an excitated carrier (e.g. electron in conduction band), when perturbed by a photon of appropriate energy, loses energy resulting in the creation of another photon, with the same phase, frequency, polarization, and direction as the original (see Figure 2.1, right)

In bulk material, the spontaneous emission rate can be expressed as

$$R_{spont} = B\left(np - n_0 p_0\right) \tag{2.1}$$

where $n$ and $p$ represent the electron and hole concentration, while $n_0$ and $p_0$ are the equilibrium electron and hole concentration, while $B$ is usually referred to as bimolecular recombination coefficient. This parameter is often determined as the second-order coefficient $BN^2$ in a polynomial fit to measurements, as a function of average concentration N: it has typical values of $10^{-11} - 10^{-9}\ cm^3/s$ for III-V semiconductors [94]. As expressed in Equation 2.1, the net recombination rate depends on the availability of electrons in the conduction band and of holes in the valence band. Under equilibrium conditions, net recombination rate is zero. Parameter B decreases with higher temperature and with tensile strain.

As stated above, recombination can take place also as a consequence of the interaction between a photon and the semiconductor material, thus leading to the stimulated emission process. The local stimulated emission rate is proportional to the optical field intensity $I_{opt}$ (measured in $W/cm^2$) according to

$$R_{stim} = g\frac{I_{opt}}{\hbar\omega} \tag{2.2}$$

with the optical gain $g$ as a material parameter proportional to the probability that a given photon triggers an electron transition, and $\hbar\omega$ as the photon energy.

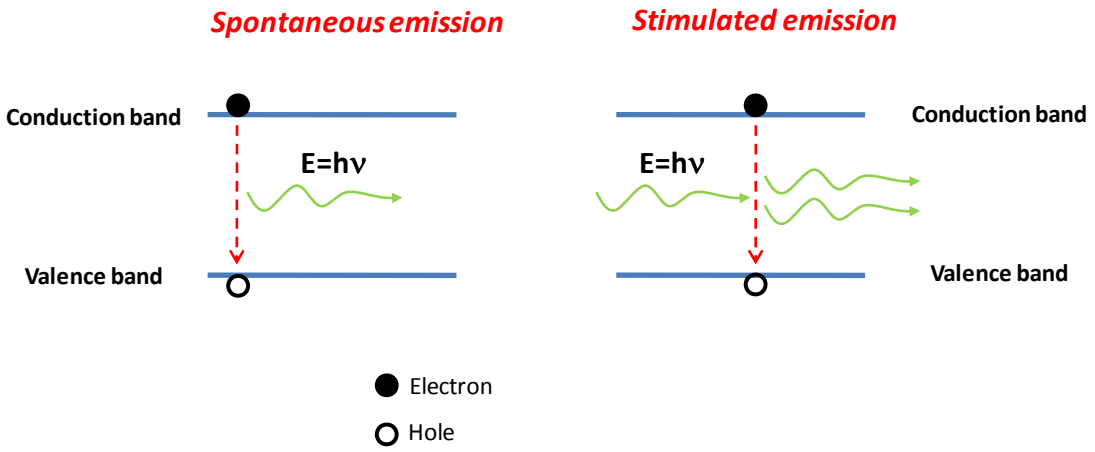



**Figure 2.1:** Schematic representation of spontaneous and stimulated emission processes

### 2.1.2 Non-radiative recombination

The two main non-radiative processes are Shockley-Read-Hall (SRH) recombination and Auger recombination. In the case of Auger recombination, the excess energy is transferred to a third electron within the valence or conduction band. After the interaction, the third carrier normally loses its excess energy to thermal vibrations. The Auger recombination rate is given by

$$R_{Aug} = (C_n n + C_p p)(np - n_0 p_0) \tag{2.3}$$

$C_n$ and $C_p$ are the Auger coefficient, that depend on temperature according to

$$C_{n,p}(T) = C_0 e^{-\frac{E_a}{k_B T}} \tag{2.4}$$

where $E_a$ is an activation energy parameter. Typical values for the Auger coefficient are $10^{-29} - 10^{-28}\ cm^6/s$ for III-V semiconductors. These values are usually determined as the third order coefficient ($CN^3$) in a polynomial fit of optical measurements at different carrier concentrations. Auger recombination reduces the luminescence efficiency of optoelectronic devices only at high carrier injection currents, due to the cubic dependence on carrier density expressed in Equation 2.3.

SRH recombination processes involve energy levels inside the semiconductor band gap that are generated by crystal defects. Such deep-level defects can capture carriers

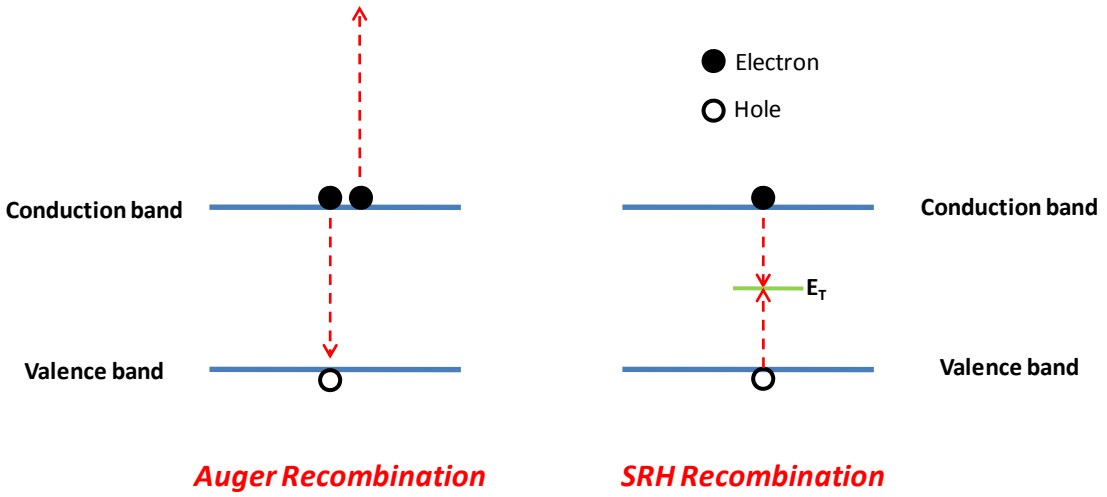



**Figure 2.2:** Schematic representation of non-radiative recombination processes

and thereby serve as recombination centers. They are characterized by capture coefficients depending on capture section, trap density $N_t$ and trap energy $E_t$. Carriers that recombine according to SRH theory release their energy by phonons.

According to SRH theory, the non-radiative recombination rate is given by

$$R_{SRH} = \frac{p_0\Delta n + n_0\Delta p + \Delta n\Delta p}{(N_t\nu_p\sigma_p)^{-1}(n_0 + n_1 + \Delta n) + (N_T\nu_n\sigma_n)^{-1}(p_0 + p_1 + \Delta p)} \tag{2.5}$$

where $\sigma_n$ and $\sigma_p$ are the capture cross sections of the traps, $\Delta n = n - n_0 = \Delta p = p - p_0$, $\nu_n$ and $\nu_p$ are the electron and hole thermal velocities and

$$n_1 = N_c e^{\frac{E_t - E_c}{k_B T}} \tag{2.6}$$

$$p_1 = N_v e^{\frac{E_v - E_t}{k_B T}} \tag{2.7}$$

are the electron and hole concentration is the Fermi level is located at the trap level ($n_1 p_1 = n_i^2$).

The non-radiative lifetime of excess electrons can be calculated considering that $R_{SRH} = \Delta n/\tau$, and is expressed as

$$\frac{1}{\tau} = \frac{p_0 + n_0 + \Delta n}{(N_t\nu_p\sigma_p)^{-1}(n_0 + n_1 + \Delta n) + (N_T\nu_n\sigma_n)^{-1}(p_0 + p_1 + \Delta p)} \tag{2.8}$$

In the case that analyzed semiconductor is p-type, the holes are the majority, i.e. $p_0 \gg n_0$ and $p_0 \gg p_1$. If deviation from equilibrium is minimum, i.e. $n - n_0 \ll p_0$,

then the minority carrier lifetime can be approximated as

$$\frac{1}{\tau} = \frac{1}{\tau_{n_0}} = N_T \nu_n \sigma_n \tag{2.9}$$

and the corresponding recombination rate, in the case of low injection conditions, is

$$R_n = \frac{n - n_0}{\tau_{n_0}} \tag{2.10}$$

In the case of n-type material, the holes lifetime and recombination rate are obtained in analogous way:

$$\frac{1}{\tau} = \frac{1}{\tau_{p_0}} = N_T \nu_p \sigma_p \tag{2.11}$$

$$R_p = \frac{p - p_0}{\tau_{p_0}} \tag{2.12}$$

As can be noticed from previous equations, SRH recombination is dominated by the more rare recombination partner (minority carrier). Semiconductor materials exhibit different types of defects depending on the fabrication process. Thus, the lifetimes are quite uncertain parameters and should be obtained from fits to measurements. Typical values are in the nanosecond to microsecond range.

The lifetime of the carriers in a semiconductor depends on all the recombination processes described above, i.e. spontaneous recombination, stimulated emission, Auger recombination and SRH recombination. The contributions of these different mechanisms give rise to the complexive carrier lifetime parameter, according to

$$\frac{1}{\tau_n} \approx \frac{R}{n} = \frac{R_{SRH} + R_{Auger} + R_{spon} + R_{stim}}{n} = \frac{1}{\tau_n^{SRH}} + \frac{1}{\tau_n^{Auger}} + \frac{1}{\tau_n^{spon}} + \frac{1}{\tau_n^{stim}} \tag{2.13}$$

### 2.1.3 Internal quantum efficiency

In this section we have described how radiative and non-radiative processes contribute to carriers recombination. These processes are in competition: in particular, even if they have a detrimental effect on the characteristics of the optoelectronic devices, non-radiative processes can not be completely avoided. Therefore, it can be useful to

define a parameter that expresses how the radiative and non-radiative processes are balanced. This parameter is the internal quantum efficiency and is defined as

$$\eta_{int} = \frac{\tau_r^{-1}}{\tau_r^{-1} + \tau_{nr}^{-1}} \tag{2.14}$$

where $\tau_r$ is the carriers lifetime associated to radiative recombination processes and $\tau_{nr}$ is the carriers lifetime associated to non-radiative recombination processes. This parameter is an expression of the ratio between the number of photons generated and the number of carriers that undergo recombination.

## 2.2 Electrical properties

In this section we will summarize the basic electrical properties of the optoelectronic devices. In the first part the current-voltage characteristics will be described, as well as the most common non-idealities. A description of the capacitive properties of the devices will be subsequently given: description will be focussed on the aspects that are of interest for the characterization and reliability study described in the subsequent chapters. For a more detailed and specific description of all the aspects concerning the characteristics of the LEDs and LDs, reader can refer to [94, 95]

### 2.2.1 Current vs Voltage characteristics

For the description of the current-voltage (I-V) characteristics of the diodes, we can consider an abrupt p-n junction, with donor concentration $N_D$ and acceptor concentration $N_A$. Assuming that all the dopant atoms are ionized, the junction is characterized by a space charge region (SCR), which is depleted of free carriers. In this situation, the only charge present in the SCR is due to the fixed donors and acceptor: this charge generates an electric field, and a built-in potential drop, that acts as a barrier for the diffusion of the carriers. This potential drop is

$$\phi_i = \frac{kT}{q} ln \frac{N_D N_A}{n_i^2} \tag{2.15}$$

where $n_i$ is the intrinsic carrier concentration of the semiconductor, and $q$ is the charge of the electron.

The width of the depletion region can be calculated starting from the Poisson equation, and is found to be equal to

$$x_d = \sqrt{\frac{2\epsilon}{q}(V - \phi_i)\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \tag{2.16}$$

where $\epsilon = \epsilon_r \epsilon_0$ is the dielectric permittivity of the semiconductor and $V$ is the voltage applied to the junction. If a positive bias is applied to the junction, the barrier that obstructs the movement of the free carriers to the other side of the diode decreases ($\phi_i \rightarrow \phi_i - V$) and carriers can diffuse to the region with opposite conductivity.

The current-voltage equation of a p-n junction, usually referred to as Schockley equation, is

$$I = qA\left(\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + \sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A}\right)\left(e^{qV/kT} - 1\right) \tag{2.17}$$

where $A$ is the area of the devices, $D$ and $D_p$ are the diffusion coefficients and $\tau_n$ and $\tau_p$ the minority carriers liferimes for electrons and holes respectively. Under reverse bias, the diode current saturates, at the value

$$I_S = qA\left(\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + \sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A}\right) \quad (\textit{saturation current}) \tag{2.18}$$

while under typical forward bias conditions, the diode voltage is $V \gg kT/q$ and therefore the relation between current and voltage becomes exponential. Using Equation 2.15, Equation 2.17 can be re-written as

$$I = qA\left(\sqrt{\frac{D_p}{\tau_p}}N_A + \sqrt{\frac{D_n}{\tau_n}}N_D\right)e^{q(V-\phi_i)/kT} \tag{2.19}$$

Therefore, for $V \gg kT/q$ current strongly increases as the diode voltage approaches the intrinsic voltage. For extrinsic and highly-doped junction, the intrinsic voltage is close to the bandgap energy divided by the electron charge (i.e. $\phi_i \approx E_g/q$). This fact indicates that the turn-on voltage of the diodes directly depends on the amplitude of the bandgap, i.e. on the semiconductor material used for the junction (see Figure 2.3).

Actually, the I-V curves of the devices deviate from the ideal behavior expressed in Equation 2.17. Usually, for the description of the I-V behavior of the devices, the following equation is used

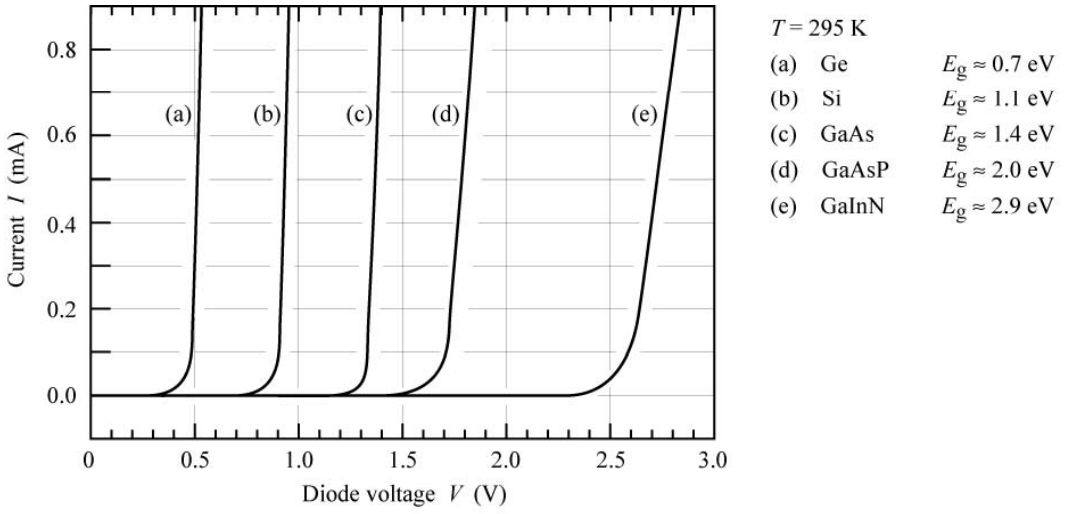



**Figure 2.3:** I-V measurements for diodes made of semiconductors with different bandgap energies, from [94]

$$I = I_s e^{\frac{qV}{n_{ideal} kT}} \tag{2.20}$$

where $n_{ideal}$ is the ideality factor of the diode. Ideally this factor is unitary. For real devices, it assumes higher values (in the range 1.1-2, according to Schubert [94]). However, in the case of quantum-well structures, this parameter can assume even higher values.

This phenomenon has been attributed to different factors:

- Cao, Dmitriev and Eliseev attributed this behavior to the fact that in heterostructure-based devices conduction is based on significant tunneling components. Since Equation 2.17 assumes that carriers cross the potential barrier and recombine at the opposite side of the junction, it represents only an approximation of the actual conduction processes, and therefore must be corrected using an appropriate parameter ([96, 97, 98]);

- Franssen observed that while in simple pn junctions recombination occurs in the neutral regions (Shockley model), in MQW structures radiative recombination takes place mostly in the middle of the depletion layer, and this is expected to give rise to an increase of the ideality factor in the I-V characteristics ([99]);

- Shah considered that real diodes are constituted by the series connection of more

junctions (ohmic contacts, the p-n junction, other heterojunctions), and all these junction contribute to the increase of the ideality factor of the devices ([100]).

Furthermore, a real diode has parasitic series resistances that is related to the intrinsic resistivity of the neutral semiconductor regions, as well as to the resistivity of the contacts. The effect of this resistive component is to decrease diodes current in the high current region. On the other hand, a parallel resistance can be caused by damaged regions or surface leakage, that generate conduction paths in parallel to the diodes. The effect of this resistance (shunt resistor) is to significantly contribute to carrier flow when the diode is not conducting, i.e. for reverse and low forward applied voltage. A description of the effects of these parasitic resistance is given in Figure 2.4. In the inset of the same figure an equivalent model for the diode with the two parasitic resistors is described. The I-V characteristic, modified taking into account the effects of the two parasitic resistive components has the following form

$$I - \frac{V - R_S I}{R_p} = I_S e^{\frac{q(V-R_S I)}{n_{ideal} kT}} \tag{2.21}$$

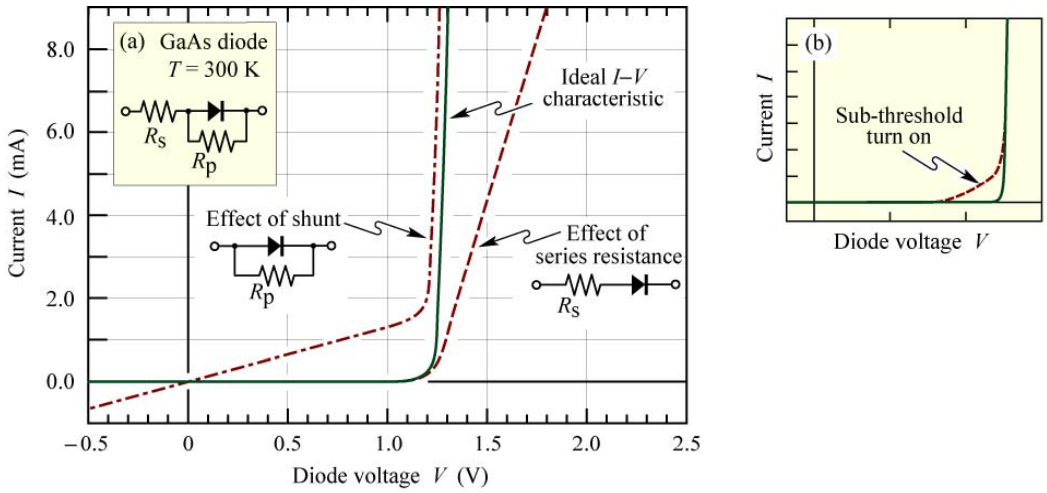



**Figure 2.4:** Effect of parasitic resistances on the characteristics of a diode

### 2.2.2 Transport processes in LEDs and lasers

As stated above, the Schockley model and Equation 2.17 can be used effectively to describe the I-V behavior of optoelectronic devices, provided that a few modifications

are introduced. In particular, we have seen how the ideality factor can be used as a parameter to adjust the exponential dependence of current on voltage in order to adapt the equation to actual diodes. These modifications must be introduced to take into account the fact that carriers transport involves other mechanisms with respect to the simple diffusion and recombination model described by Schockley. A detailed description of the mechanisms ruling carrier transport in heterostructure LEDs submitted to bias has been given by recent literature works, and will be summarized in the following.

Hirsch et al. [101] have described the I-V behavior of multi-quantum well (MQW) LEDs over temperature. Carrying out I-V characterization at different temperature levels (I-V-T measurements), they have been able to identify and describe different conduction mechanisms. Figure 2.5 shows the results of these measurements. By means of accurate modeling of the transport mechanisms, Hirsch et al. have demonstrated that:

- for low forward and reverse bias (region I in Figure 2.5), carrier transport can be described as $I \approx V/R_{sh}$, where $R_{sh}$ represents an equivalent shunt resistor, that determines similar current contributions both in forward and reverse bias. This shunt path has been attributed to hopping mechanism between next nearest neighbors electronic localized states (ELS) at low temperatures (less than 170 K) and to Poole-Frenkel mechanism, for T greater than RT.

- for intermediate bias values (region II in Figure 2.5), conduction is governed by tunneling process at low temperature values ($T \leq 250\ K$), while for higher temperatures the current injection is controlled by hole thermoionic emission from p-GaN to the nearest QW. The hole injection occurs mainly in the nearest p-GaN QW, so it does not matter whether the number of QW in the active zone is increased.

- for high current values (region III in Figure 2.5), current is limited by the resistance of the neutral n-GaN and p-GaN access zones of the diode.

When carrying out I-V-T analysis, tunneling and Schockley conduction processes can be easily distinguished, as described by [99]. According to the standard Shockley

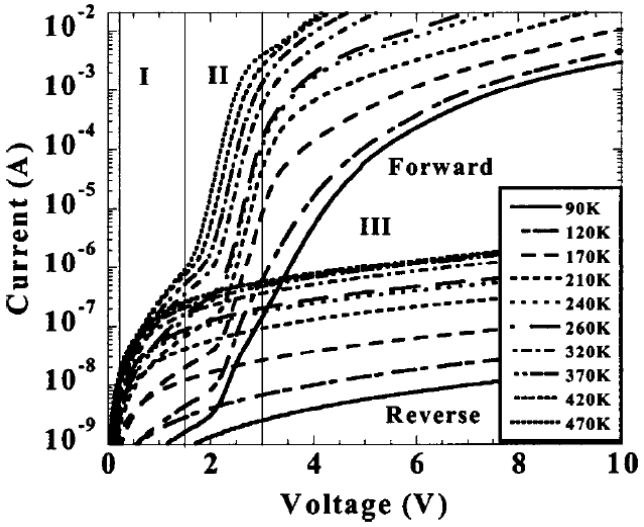



**Figure 2.5:** Typical I-V-T curves of GaN based LEDs grown by MBE for the forward and reverse biases. The presence of three conduction domains named I, II,and III is highligted

model, the I-V characteristics of a p-n junction can be described by

$$I = I_s(e^{qV/nkT} - 1) \tag{2.22}$$

On the other hand, if tunneling dominates conduction processes, current depends on voltage according to

$$I = C_1\left(e^{qV/E_T} - 1\right) \tag{2.23}$$

where $C_1$ is a constant containing the built-in potential and the density of impurity traps, and $E_T$ is an energy constant typical for tunneling process. In $p^+/n$ step junction, this energy constant is given by

$$E_T = \frac{4\hbar q\sqrt{N_D}}{\pi\sqrt{m^*\epsilon}} \tag{2.24}$$

where $N_D$ is the concentration of donors in the n-type material, $\epsilon$ is the dielectric constant of the semiconductor, $m^*$ is the effective carrier mass and $\hbar = h/2\pi$.

Thus, the slope of a semilogarithmic plot of the I-V data shows a temperature-dependent behavior in the case of the standard Shockley model, whereas it is temperature independent in the case of tunneling (see Figure 2.6).

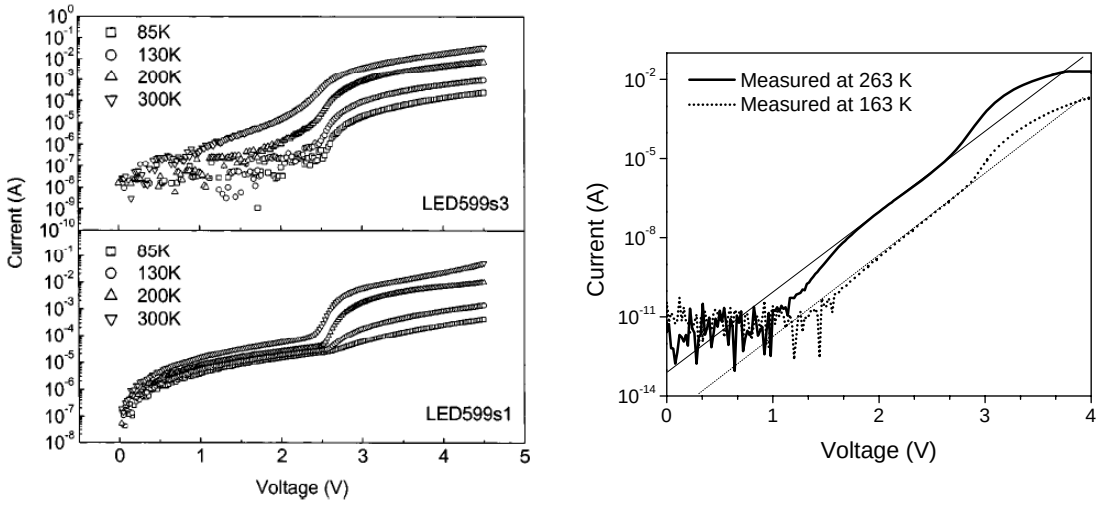



**Figure 2.6:** Left: forward bias I-V behavior of typical InGaN/GaN MQW LEDs at temperatures varying from 85 K to 300 K as reported in [99]; two regions of different behavior are clearly distinguishable. The sudden change of the slope of the semilogaritmic I-V plot around 2.5 V indicates a change of the dominant mechanism of carrier transport. Right: typical I-V curves measured on the devices described in Chapter 3, demonstrating the presence of a region of tunneling conduction (that can be distinguished for the temperature-independent slope of the I-V curves)

### 2.2.3 Reverse bias region

According to Equation 2.17, under reverse bias conditions the current of the diode should be nearly equal to the saturation current $I_S$. Measurements carried out on real devices and LEDs show that this behavior is not representative of true devices. For clarity, we show in (see Figure 2.7) the semi-logarithmic I-V measurements carried out on one of the LEDs analyzed in Chapter 3. As can be noticed, reverse current components can be significant. The two most common interpretation are described in the following.

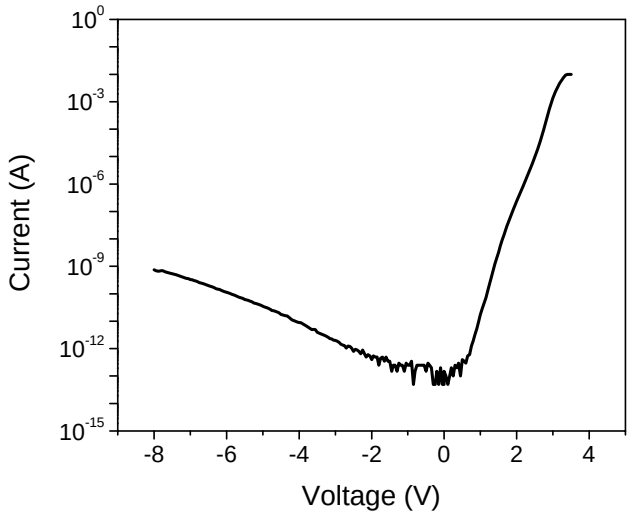



**Figure 2.7:** Typical I-V curves measured on the devices described in Chapter 3, demonstrating the presence of significant reverse-bias current, that can not be explained by means of Equation 2.17

- Cao et al. [102, 96, 103] have demonstrated that reverse dark current in the LEDs was found to scale with p-n junction area (Figure 2.8, left). This suggests that the main mechanism is bulk leakage rather than surface leakage. As can be noticed in Figure 2.8 (right), the leakage current is much higher than the classical diffusion and generation-recombination current, which should be small in magnitude in the wide band-gap materials and weakly voltage dependent. Cao attributed this high reverse current to defect-assisted tunneling, or band-to-band tunneling. At low biases, field-dependent tunneling via defects located in the space-charge region could be a major contributor. At high reverse voltages, the

data is in good agreement with band-to-band tunneling as predicted by Zener tunneling model.

- Li et al. [104] have shown that the leakage current exhibits exponential dependence on the bias voltage according to $I = I_0 e^{qV/E_0}$. For low reverse biases, the I-V behavior was attributed to leakage path through the surface states at the device mesa sidewalls. On the other hand, for high reverse bias the probability of tunneling through defect states increases and the leakage current becomes dominant. In particular, Li showed that the preexponential factor $I_0$ is proportional to the square of the density of dislocations with a screw component, and that the energy parameter $E_0$ is related to the electrical activities of dislocations with a screw component, therefore attributing the entity of the leakage to the quality of the growth process.

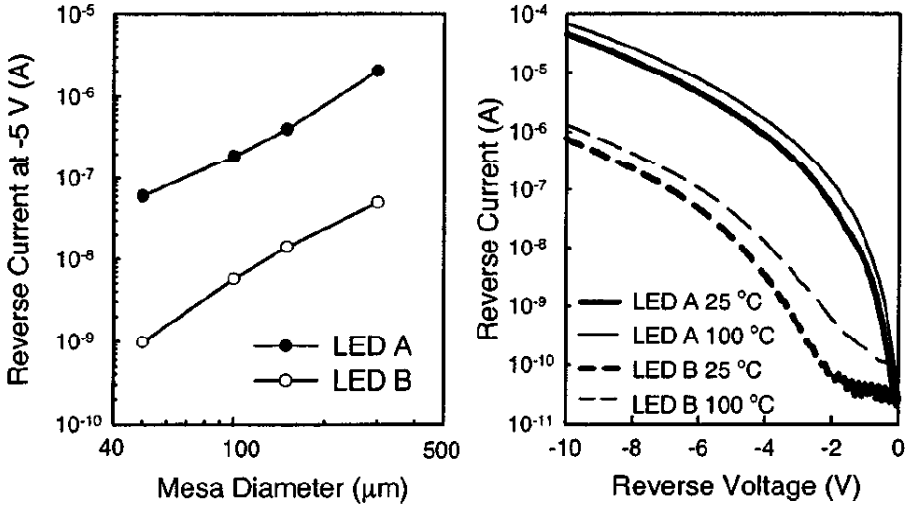



**Figure 2.8:** Left: Reverse current at -5 V in GaN/InGaN MQW LEDs as a function of mesa diameter. Right: Reverse I-V characteristics of two commercial LEDs (A and B) at 25 °C and 100 °C [102]

## 2.3 Capacitance-Voltage characterization

One of the most important characterization tools for diodes and heterostructure-based devices is the

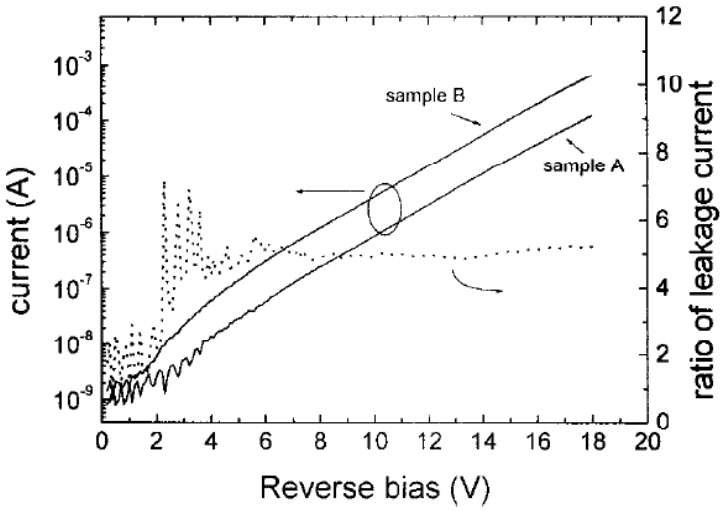



**Figure 2.9:** Reverse bias I-V curves of LED chips as reported in [104]

measurement of the junction capacitance of the devices. By means of this kind of measurement, it is possible to evaluate the distribution of charge in the proximity of the junction, information on the extension of the space charge region and band offsets and on the position of the heterointerfaces. In this section we will describe how it is possible to evaluate the charge profile in an heterostructure device starting from the results C-V measurements. Furthermore, we will describe typical C-V results obtained on GaN-based LEDs, and the corresponding literature interpretation.

### 2.3.1 p-n junction case

We can start considering an abrupt p-n junction, with acceptor and donor concentration equal to $N_A$ and $N_D$ in the two regions respectively. When the junction is formed, electrons (holes) diffuse towards the p-side (n-side) of the diode, leaving the corresponding donor (acceptor) atoms ionized. These atoms generate a distribution of fixed charge, that obstructs carriers flow, to form a fixed charge distribution in the region depleted from mobile charge (space charge region, SCR). When equilibrium is reached, the amplitude of the SCR depends on the doping level in the p and n semiconductor regions, on the characteristics of the semiconductor material and on the applied bias ($V$), according to

$$x_d = x_n + x_p = \sqrt{\frac{2\epsilon}{q}(V - \phi_i)\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \tag{2.25}$$

where $\phi_i$ is the built-in voltage, and $x_n$ ($x_p$) is the amplitude of the depleted region at the n (p) side of the diode (see Figure 2.10). It is worth noticing that a negative voltage applied to the junction implies an increase of the width of the SCR, while for forward bias the amplitude of the SCR is lower.

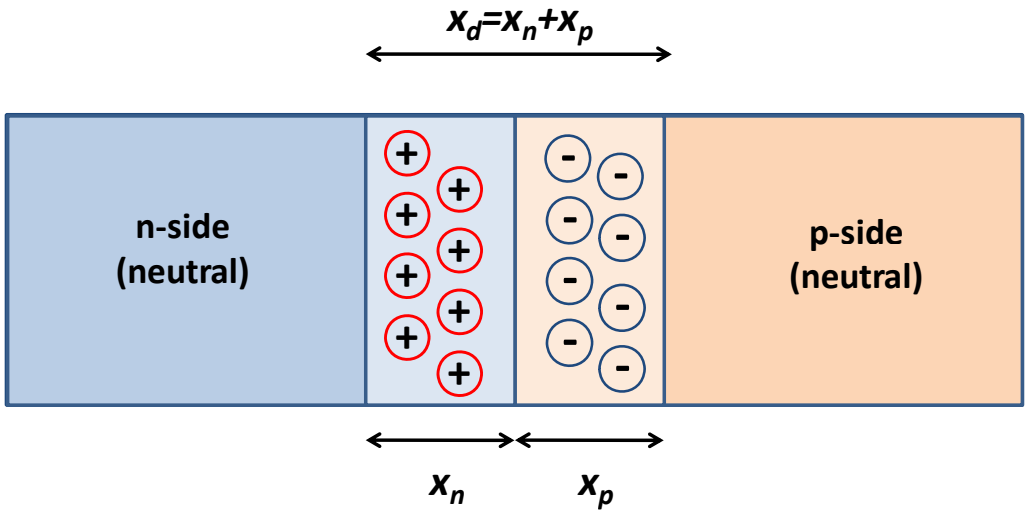



**Figure 2.10:** Schematic of the charge distribution in a p-n junction

The fixed charge (for unit of area) in the SCR is expressed by

$$Q = qN_d x_n = qN_a x_p \tag{2.26}$$

where the second equality comes from the charge neutrality principle. According to this principle, the positive charge at the n-side of the junction must be equal to the negative charge at the p-side. Since the charge Q varies with applied bias, we can define a low-signal capacitance (for unit of area) associated to the SCR, as

$$C = \frac{dQ}{dV} = qN_d\frac{dx_n}{dV} = qN_a\frac{dx_p}{dV} \tag{2.27}$$

Using Equation 2.25 - 2.27 it is possible to calculate the expression for the junction capacitance:

$$C = \sqrt{\frac{q\epsilon}{2\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(\phi_i - V)}} = \frac{\epsilon}{x_d} \tag{2.28}$$

Therefore, an increase of the applied voltage determines the narrowing of the SCR and the increase of the junction capacitance. The second equality in Equation 2.28 indicates that the diode is equivalent to a capacitor with plate separator distance equal to $x_d$ and dielectric material equal to the semiconductor. It can be demonstrated that this relation holds also for arbitrarily doped junction. In the following we will refer to the case of p-n junction with non-uniform doping distribution.

Starting from the equation

$$C = \frac{dQ}{dV} = \frac{\epsilon}{x_d} \tag{2.29}$$

we can determine the concentration of dopant in a p-n junction simply starting from the measurement of the small signal capacitance as a function of applied bias. Deriving both members of Equation 2.29 and using $x_d = x_n + x_p$ we obtain

$$\frac{dC}{dx_n} = -\frac{\epsilon}{(x_n + x_p)^2}\left(\frac{dx_p}{dx_n} + 1\right) \tag{2.30}$$

For charge neutrality equation

$$|dQ| = |qN(-x_p)dx_p| = |qN(x_n)dx_n| \tag{2.31}$$

where $dQ$ represents the charge generated as a consequence of a movement $dx_n$ ($dx_p$) of the space-charge region boundary in region n (p) around position $x_n$ ($x_p$).

From the last two equation we obtain

$$\frac{dC}{dx_n} = -\frac{C^2}{\epsilon}\left[1 + \frac{N(x_n)}{|N(x_p)|}\right] \tag{2.32}$$

that (considering the definition of capacitance) brings to

$$N(x_n) = -\frac{C^3}{\epsilon q \frac{dC}{dV}}\left(\frac{N(x_n)}{|N(-x_p)|} + 1\right) \tag{2.33}$$

that describes the concentration of charge at the boundary $x_n$ of the SCR at the n-side, once the charge concentration in $-x_p$, the junction capacitance $C$ (corresponding to an SCR amplitude equal to $x_d = x_n + x_p$) and its derivative are known.

### 2.3.2 Asymmetric junction

In the case that one of the two sides of the junction (e.g. the p-side) is more heavily doped than the n-side ($p^{++}/n$ asymmetric junction approximation), the ratio $N(x_n)/N(-x_p)$ tends to zero, and Equation 2.33 becomes

$$N(x_n) = \frac{2}{q\epsilon \frac{d\frac{1}{C^2}}{dV}} \tag{2.34}$$

For this last calculation we have considered that

$$\frac{d(1/C^2)}{dV} = -\frac{2}{C^3}\frac{dC}{dV} \tag{2.35}$$

Equation 2.34 indicates that if the junction is asymmetric, the slope of the $1/C^2$ vs V curve is directly related to the concentration of charge at the border of the SCR. Using Equation 2.34 it is therefore possible to estimate the Apparent Charge Distribution (ACD) for one asymmetric diode.

### 2.3.3 Heterostructure-based devices

For heterostructure-based devices, the presence of heterojunction can strongly influence the behavior of the capacitance-voltage curves. The main difference with respect to simple p-n junction is that in the case of heterostructure devices the bending of the conduction and valence band (due to a potential notch or to the presence of a quantum-well) can determine significant accumulation of free charge in specific regions of the devices. This free charge contributes to the capacitive behavior of the junction, as well as the fixed charge due to ionized dopant atoms. Therefore, by means of capacitance-voltage characterization of an heterostructure-based device, it is possible to extrapolate information also on the position and characteristics of the charge accumulation regions. Furthermore, a C-V analysis can provide information on the band discontinuities at heterojunction interfaces [105, 106].

For the explanation of the behavior of the C-V curves in the case of heterostructure and multi-quantum well devices, we refer to the works of Ershov [107], Moon [108, 109], and Xia [110].

Ershov has described in detail the C-V charactertistics of MQW-based LEDs

and photodetector: the devices that he has analyzed were quantum-well infrared photodetector-LEDs (QWIP-LED), and had the schematic structure shown in Figure 2.11.

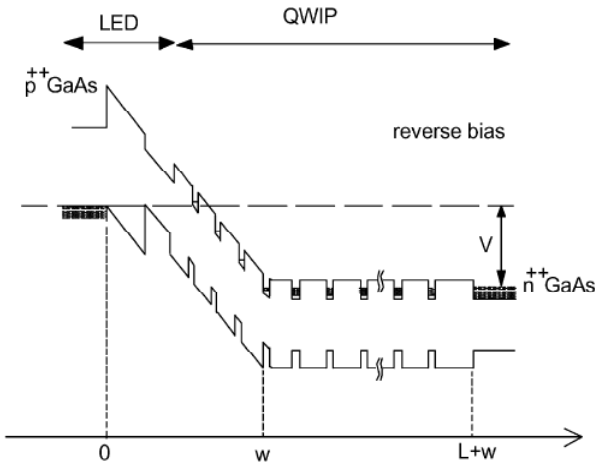



**Figure 2.11:** Schematic band structure of one of the devices analyzed by Ershov [107]

Since these devices present an high number of heterostructures, they are appropriate for describing the behavior of the C-V curves in MQW devices. The typical C-V curve for one of these devices is shown in Figure 2.12. At low frequencies, the capacitance is determined by the depletion layer capacitance. As described in the previous sections, capacitance decreases with increasing reverse bias, due to the widening of the SCR. As shown in Figure 2.12, the C-V curves present steps, that can be explained as follows. Under zero bias, the border of the SCR in the QW region is located close to the first QW, that is partially depleted of electrons. With the increase of the negative bias, the electric field in the SCR increases, and the electrons are pushed out of the first quantum well. When this happens, the boundary of the space charge region moves to the second QW, so the width of the SCR is increased by a distance equal to the separation of the QWs in the lattice. This implies a step-like behavior of the capacitance-voltage curves. This process is repeated until the last QW (the farest from the junction) is depleted. Obviously, the analysis presented by Ershov has been made under the approximation that the extension of the SCR at the p-side of the diodes is negligible with respect to the corresponding SCR amplitude at the n-side.

In Figure 2.13 we report the behavior of the $dC/dV$ curves for the corresponding

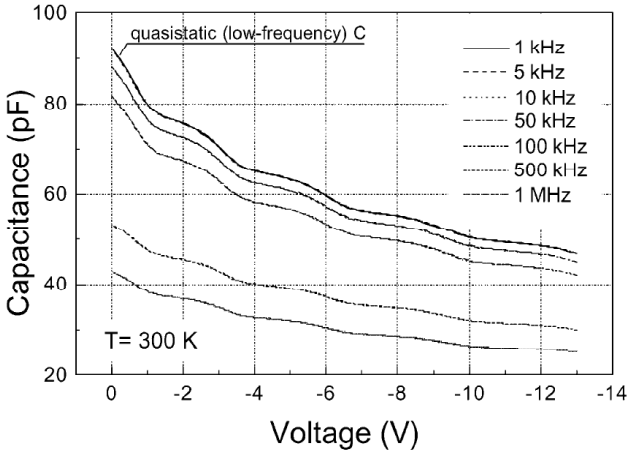



**Figure 2.12:** Capacitance-Voltage characteristics measured at various frequencies, RT, on one of the QWIP-LED analyzed by Ershov [107]

devices. The peaks of this curve correspond to the voltages at which the boundary QW is completed depleted and the space charge region jumps to the next QW. It can be shown, from electrostatics consideration, that the voltage offset between the positions of the $dC/dV$ peaks is given by $V_i - V_{i-1} = q\Sigma A/C_i$, where $V_i$ is the voltage corresponding to a complete depletion of the ith quantum-well, $\Sigma$ is the 2D charge density of the QWs and $C_i$ is low frequency capacitance of the MQW structure when the boundary of the SCR is located at the ith QW. Therefore, from the distance between two steps on the 1/C axis, it is possible to evaluate the distance between the QWs.

Xia et al. [110] correlated the step-like behavior of the C-V curves to the optical characetistics of the devices. They have used MQW structures, and measured the variation of *(i)* junction capacitance, *(ii)* photoluminescence signal and *(iii)* photocurrent signal with varying bias. They have demonstrated a correlation between the three measurements, that is described in Figure 2.14, that reports the net fixed charge concentration versus depletion width (left axis), PL spectrum (right axis), and PC as a function of depletion width deduced from the measured capacitance. The peaks of the charge profiles are attributed to the QWs, while the valleys correspond to the barriers. The step-like behavior of the PL and PC signal show a good correspondence with the peaks of the charge profile: this fact confirms that when junction bias is decreased, the boundary of the SCR is swept through the QWs and the valleys. When

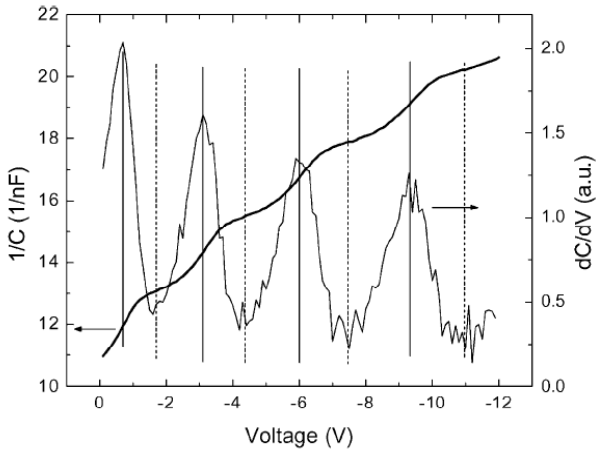



**Figure 2.13:** Inverse capacitance and capacitance derivative ($dC/dV$) measured on one of the devices analyzed by Ershov [107]

the depletion region reaches the position of one QWs, the PL intensity changes abruptly, while at the positions of the barriers, the PL intensity changes slowly. PC has the same behavior.

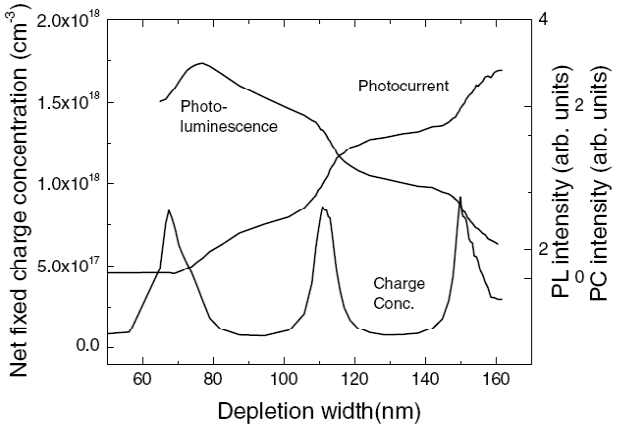



**Figure 2.14:** Net fixed charge concentration versus depletion width (left axis), PL spectrum (right axis), and PC as a function of depletion width deduced from the measured capacitance [110]

Further detail on the C-V behavior of MQW structures has been given by Moon et al. [108, 109]. Moon worked with InGaAs/GaAs SQW and MQW devices. His work was mostly concentrated in evaluating how the Free Carrier Density (FCD) and the

Apparent Carrier Density (ACD) vary when QW parameters and junction voltage are varied. In order to clarify these aspects, Moon has carried out a comparison between experimental and simulated C-V curves of MQW LEDs. Simulation have been based on the solution of the Schroedinger and Poisson equations, and took into account the Debye averaging process.

The Schroedinger equation is given by

$$\frac{\hbar^2}{2}\frac{d}{dx}\left[\frac{1}{m^*(x)\frac{d}{dx}}\right]\psi(x) + V(x)\psi(x) = E\psi(x) \tag{2.36}$$

where $\psi$ is the wavefunction, E is the energy, V is the potential, $\hbar$ is Plank's constant divided by $2\pi$ and $m^*$ is the effective mass. This equation must be solved on the entire semiconductor structure, in order to take into account the coupling effects of the QWs. On the other hand, Poisson's equation is

$$\frac{d}{dx}\left[\epsilon(x)\frac{d}{dx}\right]\Phi(x) = -q\left[N_d(x) - n(x)\right] \tag{2.37}$$

where $\phi$ is the electrostactic potential. In general, the spatial resolution of the C-V profiles is determined by the Debye screening length $L_D$, that is given by $L_D = (\epsilon kT/q^2 n)^{1/2}$, where $n$ represents the carriers concentration. The ACD profile reflects the real one only if the depth scale is greater than several Debye lengths. In a MQW structure, the Debye length is usually 20 nm at RT (for $n = 5 \cdot 10^{16}\ cm^{-3}$), and the thicnkesses of the well layer can be smaller than 3 nm. This confirms the importance of considereing Debye screening processes in simulations. Figure 2.15 show the C-V curves and corresponding charge profiles simulated for a SQW and a six-period MQW device. The C-V curves confirm the step-like behavior described above and attributed to the presence of the quantum wells. It is worth noticing that the six-fold quantum-well charge profile does not show six equivalent peaks for the six QWs, even if the same parameters have been used for the simulation. As can be noticed, the first and the last peaks are higher than the others. An explanation of this behavior can be given considering how the carriers are distributed in QW structures with different number of wells (see Figure 2.16).

As can be noticed, the distribution of the electrons is symmetric with respect to the center of the MQW and their peak height and sheet density increase as we go from the

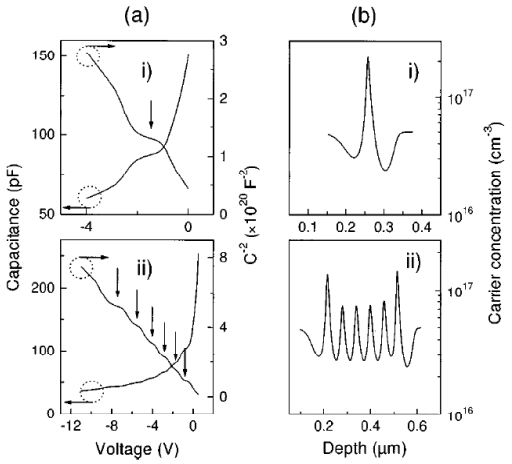



**Figure 2.15:** (a) Typical capacitance-voltage profiles and $C^2 - V$ profiles in QW structures simulated from the self-consistent numerical methods. Steplike profiles are explicitly shown. Downward arrows indicate the accumulation peak positions. (b) Concentration vs depth profiles obtained from the simulated C-V profiles. One peak in SQW and six peaks in MQW with six wells are explicitly shown [108]

inner to the outer QWs. This phenomenon can be explained by applying the Gauss theorem to the conduction band diagram in Figure 2.16. If the theorem is applied to the cube with a pair of opposite faces passing through adjacent points in barriers, where the electric field is zero, the total charges in the cube is zero. In the case of the outer QWs, the electrons in the well must compensate for the positive charges in the wide depletion region in thick top (or bottom) layer. On the other hand, the electrons in the inner QWs must compensate for the positive charges in the depletion regions formed in thin barriers. Since the depletion regions in the inner barriers are much thinner than the outmost depletion regions, the electron concentration in the inner QWs must be lower than that in the outer.

The influence of the Debye length averaging on the extrapolated carriers profiles has been analyzed by Moon et al. [108] simulating the ACD of devices with two quantum-well with different barrier thicknesses in the range 10-190 nm. Results are shown in Figure 2.17: as can be noticed, for high values of the barrier thickness $t_b$, the peaks corresponding to the two QWs are well separated. On the other hand, when $t_b$ is descreased the peaks superimpose until reaching the complete overlapping, due to

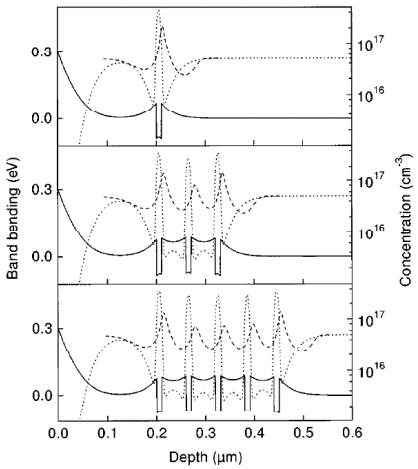



**Figure 2.16:** Self-consistently calculated band bending (solid lines), free carrier distribution (dotted lines), and apparent carrier distribution (dashed lines) of QW structures with the well number of (a) one, (b) three, and (c) five. The well width is assumed to be 10 nm [108]

the fact that the resolution of C-V profiling is defined by the Debye length, that in this last case becomes comparable to the separation of the wells.

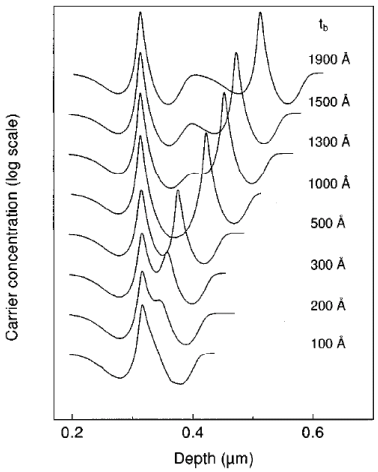



**Figure 2.17:** Self-consistently calculated ACDs for double-QW structures with different barrier thicknesses

## 2.4 Optical properties

In this section, the optical characteristics of the LEDs will be explained in detail: attention will be focussed on the rate equation for LEDs, on the dependence of optical power on injected current and on the shape of the emitted spectrum. For a more detailed and specific description of all the aspects concerning the characteristics of the LEDs and LDs, reader can refer to [94, 95]

### 2.4.1 Emission spectrum

For LEDs, the dominating recombination mechanisms ir spontaneous emission. The radiative electron-hole recombination process can be schematically described as in Figure 2.18 for a direct-bandgap semiconductor. Electrons in conduction band and holes in valence band have nearly parabolic dispersion. This means that their distribution in an $E-k$ space can be expressed as:

$$E = E_C + \frac{(h/2\pi)^2 k^2}{2m_e^*} \quad (for\ electrons) \tag{2.38}$$

and

$$E = E_V - \frac{(h/2\pi)^2 k^2}{2m_h^*} \quad (for\ holes) \tag{2.39}$$

where $m_e^*$ and $m_h^*$ qare the electron and hole effective masses, $k$ is the carrier wavenumber and $E_C$ and $E_V$ are the valence and conduction band edges respectively.

For the energy conservation principle, the energy of the emitted photon is $h\nu = E_e - E_h \approx E_g$, where $E_e$ ($E_h$) is the energy of the recombinating electron (hole). The momentum $p = \sqrt{2m^* kT}$ of the electron can not change significantly during transition to the lower state: therefore, we can assume that during radiative recombination the momentum or $k$ is the same for the electron and the hole. Under this assumption we can calculate the photon energy, and write it according to joint dispersion relation

$$h\nu = E_C + \frac{h/2\pi)^2 k^2}{2m_e^*} - E_V + \frac{(h/2\pi)^2 k^2}{2m_h^*} = E_g + \frac{(h/2\pi)^2 k^2}{2m_r^*} \tag{2.40}$$

where $m_r^*$ is the reduced mass given by

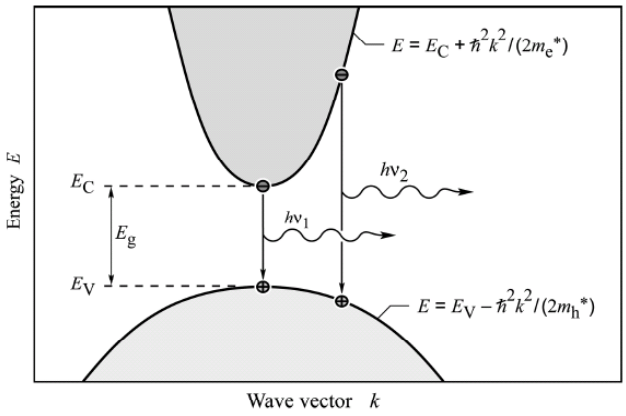



**Figure 2.18:** Schematic band diagram showing the occurrence of a spontaneous recombination event

$$\frac{1}{m_r^*} = \frac{1}{m_e^*} + \frac{1}{m_h^*} \tag{2.41}$$

Therefore, the joint density of states can be calculated as

$$\rho(E) = \frac{1}{2\pi^2}\left[\frac{2m_r^*}{(h/2\pi)^2}\right]^{3/2}\sqrt{E - E_g} \tag{2.42}$$

Since the distribution of carriers in the bands is given by the Boltzmann statistics, i.e.

$$f_B(E) = e^{-E/kT} \tag{2.43}$$

the emission intensity as a function of energy (emission spectrum), that is proportional to to the product of the two last equations, is

$$I(E) \propto \sqrt{E - E_g}e^{-E/kT} \tag{2.44}$$

that corresponds to the spectral shape shown in Figure 2.19, which is the theoretical emission spectrum for one LED. The peak emission energy is at $E = E_G + 1/2kT$.

The theoretical full-width at half maximum of the emission spectrum is

$$\Delta E = 1.8kT \tag{2.45}$$

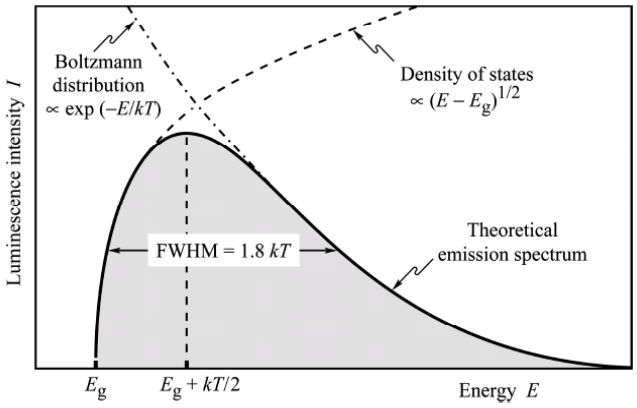



**Figure 2.19:** Theoretical intensity spectrum for a direct-bandgap semiconductor

In real cases, alloy composition fluctuations can induce the broadening of the emitted spectrum. Experimental data show that in general a Gaussian function can be used to describe the spectral power distribution, according to

$$P(\lambda) = P\frac{1}{\sigma\sqrt{2\pi}}e^{-\frac{1}{2}\left(\frac{\lambda-\lambda_{peak}}{\sigma}\right)^2} \tag{2.46}$$

where $P$ is the total light emitted by the LED. The fact that Gaussian fit represents a good match to experimental data is expressed by Figure 2.20, that shows the comparison of InGaN/GaN blue LED emission and its gaussian fit.

In most of the cases, quantum-well (QW) based structures are used for the realization of efficient optoelectronic devices. The carrier confinement length related to the small dimensions of the quantum wells (typically $t \leq 10nm$) implies that we can consider the carriers as in one-dimensional potential energy well in the x-direction (with discrete energy level), and as free carriers in the yz plane. The energy levels of the electrons in a quantum well of sizes $d$, $D_y$ and $D_z$ are given by

$$E = E_c + \frac{h^2n^2}{8m_e^*d^2} + \frac{h^2n_y^2}{8m_e^*D_y^2} + \frac{h^2n_z^2}{8m_e^*D_z^2} \tag{2.47}$$

where $n$, $n_y$ and $n_z$ are quantum numbers having the values 1, 2, 3, ... The reason for the $E_c$ in Equation 2.47 is that the potential energy barriers are defined with respect to $E_c$. These barriers are $\Delta E_c$ (conduction band offset) along $x$ and electron affinity

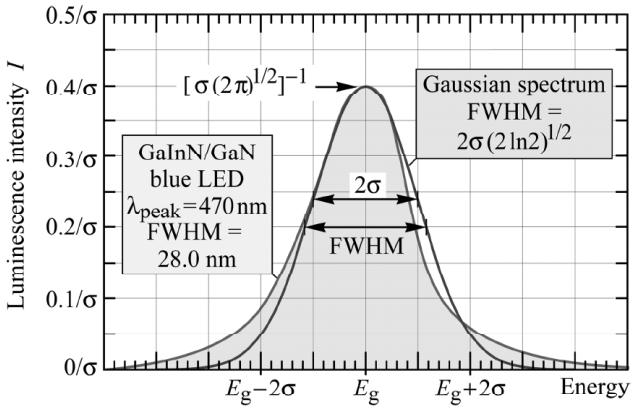



**Figure 2.20:** Theoretical emission spectrum of a semiconductor showing alloy fluctuation-related broadening

along $y$ and $z$. $D_y$ and $D_z$ are orders of magnitudes greater than $d$, and for this the minimum energy level is determined by the term

$$\frac{h^2 n^2}{8 m_e^* d^2} \tag{2.48}$$

that represents the energy associated with motion in $x$ direction. The minimum energy is obtained for $n = 1$: a schematic representation of the quantized energy levels in a quantum well is given in Figure 2.21. On the other hand, the holes in the QW are confined by the potential barrier $\Delta E_v$, and behave similarly as indicated in Figure 2.21. The electron transitions in a quantum well differ from those in bulk semiconductors, because of the quantized states formed in the wells. The electrons and holes in bulk semiconductor transit between the conduction and valence band, while in QWs the transitions occur between quantized sub-bands. Therefore, the wavelength emitted by a QW is shorter than the corresponding wavelength for corresponding bulk layers. Under excitation, transitions mainly occur between the ground energy levels ($n = 1$ in conduction and valence band), and photon energy can be rougly expressed as

$$E = E_g + \frac{h^2 n^2}{8 m_e^* d^2} + \frac{h^2 n^2}{8 m_h^* d^2} \tag{2.49}$$

The difference between bulk and QW emission wavelength can be significant: for example, in the case of a GaAs quantum well of thickness 10 nm, this difference is

equal to 35 nm.

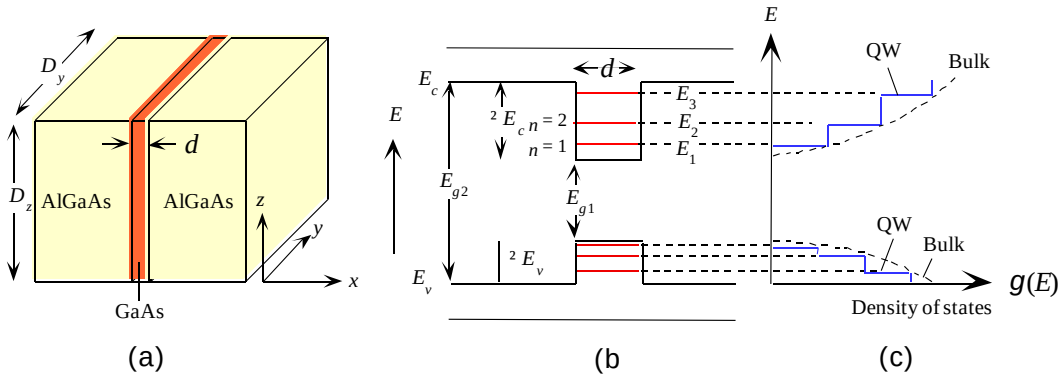



**Figure 2.21:** (a) schematic structure of a QW-based device; (b) the conduction electron in the QW are confined along x direction, so their energy is quantized; (c) density of states in a two-dimensional QW

At the beginning of this chapter we have cited the fact that the semiconductor lattice is not ideal, and contains defects. The presence of defects often results in an increase of the non-radiative recombination rate, with subsequent decrease of the efficiency of the emission process. However, a few defects can generate radiative transitions. An example is presented by GaN semiconductor layers. The luminescence of this material presents a narrow emission peak centered at 365 nm (at RT), that corresponds to the bandgap energy, and a broad yellowish emission band (centered at 550 nm) related to defects (see Figure 2.22). This yellow luminescence is usually attributed to gallium vacancies [94].

### 2.4.2 Output power vs Current curves

As described at the beginning of this chapter, carrier recombination processes may be radiative and non-radiative. Radiative processes (governed by bimolecular coefficient B) therefore take place in parallel or in series with other processes, including SRH recombination (coefficient A), Auger recombination (coefficient C), electron and hole trapping processes, $c_n$ and $c_p$ and leakage current out of the active region. A schematic representation of these phenomena is given in Figure 2.23.

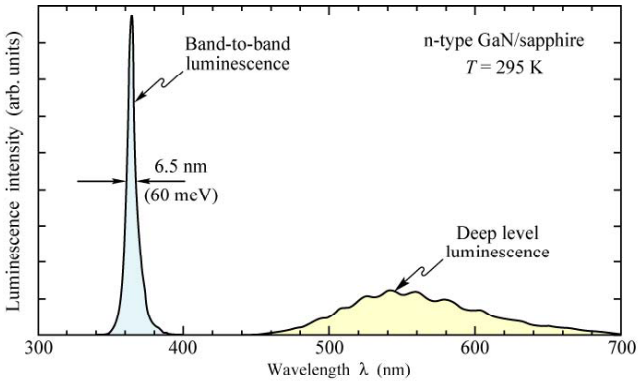



**Figure 2.22:** Photoluminescence signal measured at room temperature on a GaN sample. The main UV emission (at 365 nm) and the broad defect peak (cenetered at 550 nm) are clearly visible

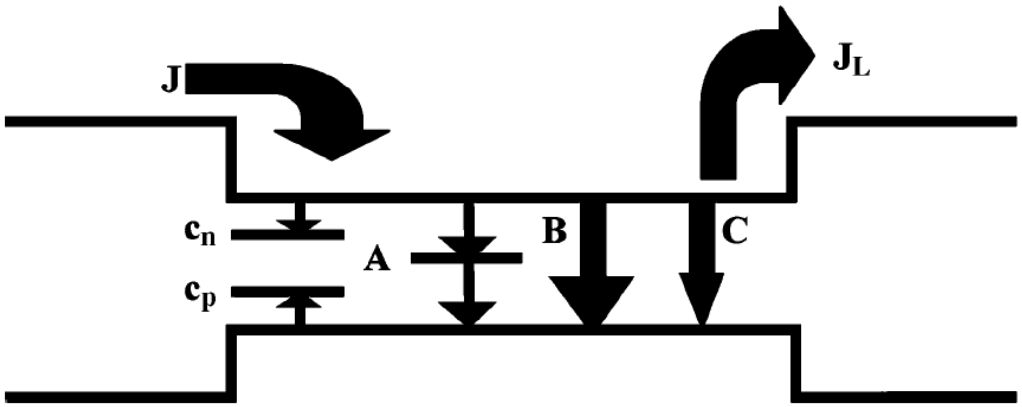



**Figure 2.23:** Schematic representation of the carriers recombination processes

The most state-of-the-art LEDs have lightly doped p and n-side. Therefore, the injected carrier concentration is higher than the background doping, and therefore we can assume that $n = p$. In this approximation, as described above, SRH, radiative and Auger recombination rate can be described by terms of the form $An$, $Bn^2$, $Cn^3$ respectively. Charge neutrality conditions impose that the rate equation can be expressed as

$$\frac{dn}{dt} = \frac{J}{ql} - An - Bn^2 - Cn^3 - \frac{J_L}{ql_1} \tag{2.50}$$

or, in other terms

$$\frac{dn}{dt} = \frac{J}{ql} - R_{SRH} - R_R - R_A - \frac{J_L}{ql_1} \tag{2.51}$$

where $J_L$ is the leakage current density out of the active region.

Converting recombination rate in lifetimes we finally obtain the following rate equation

$$\frac{dn}{dt} = \frac{J}{ql} - n\left(\frac{1}{\tau_{SRH}} + \frac{1}{\tau_R} + \frac{1}{\tau_A}\right) - \frac{J_L}{ql_1} \tag{2.52}$$

where $l$ is the thickness of the active layer, $l_i$ is the minority carriers diffusion length, $R_{SRH} = An$, $R_A = Cn^3$, $R_A = Cn^3$.

Under steady-state regime, Equation 2.52 becomes

$$\frac{J}{ql} = An + Bn^2 + Cn^3 + \frac{J_L}{ql_1} \tag{2.53}$$

Under the condition $n = p$, the term $Cn^3$ depends on bandstructure through the relationship $np = n_i^2 e^{qV/kT}$ and $n_i^2 = N_C N_V e^{-E_g/kT}$. In wide-bandgap semiconductors, the term $n_i^3$ can be small, and therefore the Auger recombination term is usually neglected. Under this assumption, the rate equation simplifies to

$$\frac{J}{ql} \approx An + Bn^2 + \frac{J_L}{ql_1} \tag{2.54}$$

Remembering the expression of the SRH recombination rate explained at the beginning of this chapter

$$R_{SRH} = \frac{p_0\Delta n + n_0\Delta p + \Delta n\Delta p}{(N_t\nu_p\sigma_p)^{-1}(n_0 + n_1 + \Delta n) + (N_T\nu_n\sigma_n)^{-1}(p_0 + p_1 + \Delta p)} \tag{2.55}$$

under the assumption that trap parameters are the same for electrons and holes and that $n = n_0 + \Delta n \approx p = p_0 + \Delta p$, i.e. that injected carrier concentration is higher than the background doping it can rewritten as

$$R_{SRH} \approx \frac{n\sigma v N_T}{2} \tag{2.56}$$

and neglecting the leakage current components we have

$$J' = qln\sigma v N_T/2 + qlBn^2 \tag{2.57}$$

At low current densities, the electron concentration $n$ is low, and therefore $An \gg Bn^2$. For an intermediate current value the radiative and non-radiative recombination terms become equal ($An = Bn^2$), and

$$J' \approx 2qlaN_1 = qln_1\sigma v N_T \tag{2.58}$$

where $n_1$ is the value of $n$ for which $An = Bn^2$. This last equation indicates that the current level necessary to saturate the non-radiative recombination components is proportional to the defect concentration. At higher current level, the quadratic term $Bn^2$ begins to dominate over the non-radiative term, leading to the complete saturation of non-radiative paths.

Light output $L$ is only related to radiative recombination and therefore is proportional to $Bn^2$. On the basis of the previous calculation we can state that

$$L \propto Bn^2 = \frac{J'}{ql} - \frac{n\sigma v N_T}{2} \tag{2.59}$$

On the other hand, for low current levels we have $An \gg Bn^2$ and

$$L \propto Bn^2 \approx \frac{B}{A^2}\left(\frac{J}{qd}\right)^2 \tag{2.60}$$

Therefore, for low injection current levels, non-radiative processes dominate and light output has a parabolic dependence on injected current. For higher current levels

non-radiative processes are saturated, and light output depends linearly on injected current. The balance between radiative and non-radiative process at the different current levels and the parabolic and linear behavior of the optical power vs injected current (L-I) curves are schematically represented in Figure 2.24 and 2.25 respectively.

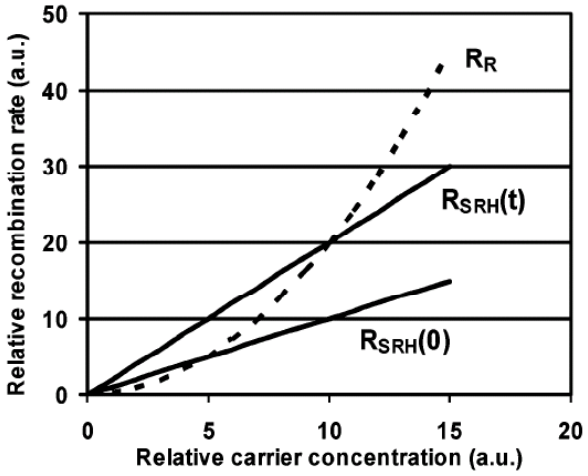



**Figure 2.24:** Schematic representation of the carriers recombination processes (radiative and non-radiative processes)

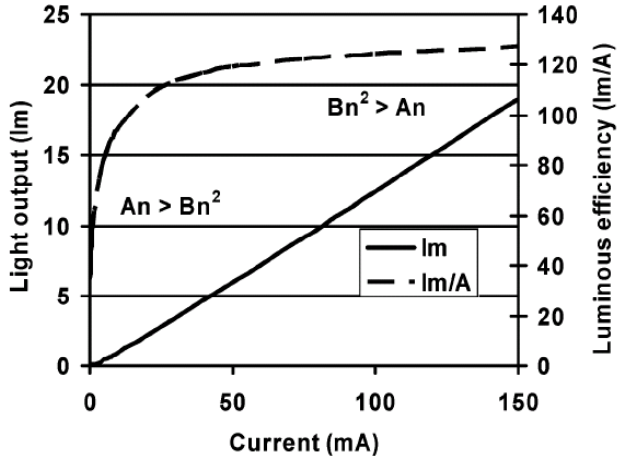



**Figure 2.25:** Schematic plot of the L-I curve of one LED, showing the parabolic and linear region. The luninous efficiency (L/I vs I) is also plotted for completness

## 2.5 Summary

In this chapter we have described the most significant electrical and optical properties of GaN-based optoelectronic devices. In particular, we have focussed the attention on:

- the mechanisms that rule carriers radiative and non-radiative recombination
- the electrical characteristics of the diode and their most significant non-idealities
- the capacitance-voltage characteristics, the methods for the extrapolation of the apparent charge distribution, and the typical C-V profiles of quantum-well structures
- the rate equation, the optical power vs input current characteristics, and the luminescence spectrum of the LED

# Chapter 3

# Analysis of heterostructure degradation

This chapter describes the analysis of the effects of low current density stress on the properties of LEDs heterostructure. The analysis has been carried out by means of combined electrical, optical and capacitive techniques. R&D samples have been used for this study. Low current density stress was found to induce the degradation of the output power emitted by the analyzed devices, mostly during the early stages of treatment. Optical power decrease was found to be correlated to modifications of the electrical and capacitive properties of the LEDs: detailed spectroscopic analysis demonstrated that carrier flow can induce the generation/modification of trap states near/within the active layer, that can be related to the generation of non-radiative recombination paths responsible for the efficiency degradation.

## 3.1 Motivation

The literature about GaN LEDs reliability indicates many mechanisms, generated by both charge flow and thermal heating processes, as responsible of LEDs degradation: modifications of the electrical contacts [21], changes in the local indium concentration in the quantum wells (QW) [26, 27], formation of radiative and non-radiative centers [28, 23], changes in the charge-injection mechanisms across the cladding and barrier layers (pure tunnelling, trap/phonon assisted tunnelling, thermal emission etc.) [29], aggregation or breaking of complexes mainly involving hydrogen impurities and

magnesium p-dopant [30].

In the last years, the failure modes responsible for the output optical power reduction have been intensively investigated, chiefly by injecting electrical currents in order to simulate the working applicative conditions of the LEDs. However, in most of the cases high driving current levels have been used, with the aim of accelerating stress kinetics and analyze ageing effects in a shorter time interval. During high current stress, a significant power is dissipated on the samples, and therefore the experimental data on the effects of carrier flow on devices degradation can be masked by contributions of thermal effects, arising from Joule dissipation. In this situation the understanding of the degradation mechanisms is difficult due to the overlapping of two different aging inputs: intense carrier flow across the active layer and high lattice temperature levels.

The purpose of the work described in this chapter is the aging of blue GaN LEDs under current values comparable or lower than those employed in normal operation modes ($20mA$, corresponding to a current density of $32A/cm^2$), in order to exclude any thermally-induced degradation (thermal maps have shown that the junction temperature never exceeds 65 °C during our stress tests). InGaN-based test structures have been electrically and optically characterized before any aging treatments (as-received samples) and then submitted to low dc current stress and examined at different aging steps.

Starting point for this work was a set of measurements demonstrating that a set of LED test structures can lose the 20-30% of their efficiency during the initial stages of ageing tests (initial 50-200 hours of stress at 20 mA), without showing significant degradation in the subsequent stress phases (up to 2000-5000 hours of operation). This short-term degradation is usually referred to as *early degradation*. Our industrial partners were strongly interested in the investigation of these short-term degradation processes, and in the identification of the technological weaknesses responsible for these phenomena, that can induce a significant optical power degradation during the very first phases of devices useful life. For this reason, the work described in this chapter is focussed on the short-term degradation processes of GaN-based LEDs. The results of this work have provided a description of the nature of the *early-degradation* process: the feedback to the manufacturer has leaded to the development of devices with stable behavior (no *early-degradation*).

In the next sections, results concerning:

- efficiency decay during stress at 20 mA
- electrical current-voltage (I-V) characteristics and capacitance-voltage (C-V) measurements
- Deep Level Transient Spectroscopy (DLTS) analysis of aged devices
- optical device emission, studied by complementary techniques of ElectroLuminescence (EL) and CathodoLuminescence (CL) in order to exploit different excitation mechanisms
- photocurrent spectroscopy of untreated and aged samples

are described and discussed.

## 3.2 Analyzed devices and stress conditions

For this analysis we have used MQW LED test structures, grown by MOCVD on SiC substrates. Vertical structure consisted in a thick n-doped GaN layer ($Si \approx 2 \cdot 10^{18}\ cm^{-3}$), a 4-period InGaN/GaN MQW ($2nm/14nm$, n-doped barriers, $Si \approx 2 \cdot 10^{18}\ cm^{-3}$) and a p-side with a $40nm$ electron-blocking $Al_{10}Ga_{90}N$ layer ($Mg \approx 2 \cdot 10^{19}\ cm^{-3}$) and a GaN contact layer ($Mg \approx 2 \cdot 10^{19}\ cm^{-3}$).

The schematic structure of the devices is reported in Figure 3.1. The devices are designed to give a blue QW-related emission at 2.72 $eV$ for an operating current of 20 mA at room temperature. The quality and thicknesses of the layers have been controlled by means of Transmission Electron Microscopy (TEM). Figure 3.2 and 3.3 show TEM images of the active region of one analyzed sample, and a detail of the active region with the fourfold quantum well system. The structure was processed in order to obtain square devices, with a 250 $\mu m$ side. The tested chips were bonded on metallic packages (*TO18*) and the ohmic cathode contact was implemented with a bi-component conductive epoxy adhesive, ensuring good electrical and thermal characteristics (see Figure 3.4). The chips were covered with a SiN passivation layer,

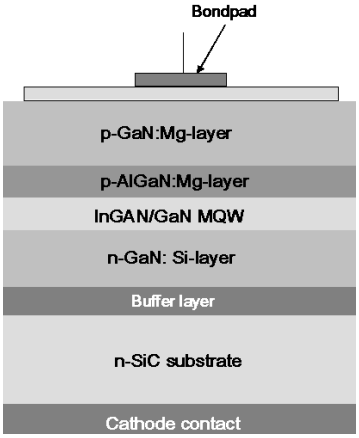



**Figure 3.1:** schematic structure of analyzed devices

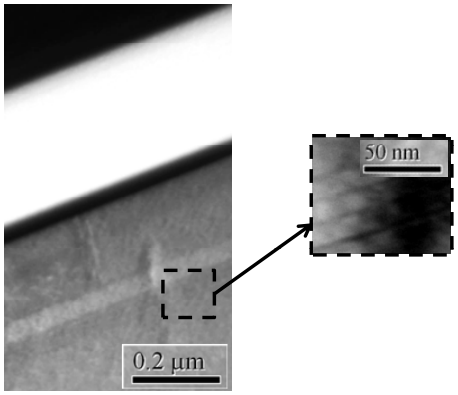



**Figure 3.2:** Transmission Electron Microscopy image of the active layer of one analyzed sample

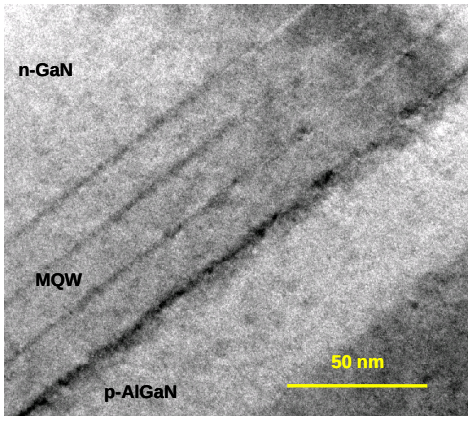



**Figure 3.3:** Transmission Electron Microscopy image of the active layer of one analyzed sample

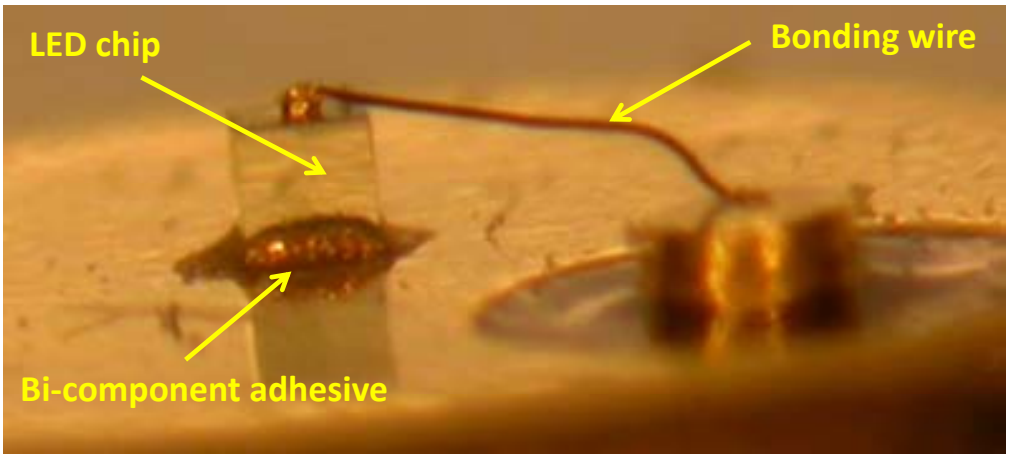



**Figure 3.4:** Micrograph of one LED chip mounted on TO18 package

in order to reduce surface leakage current components and protect the devices from environmental contamination.

After an initial characterization of a wide number of samples, we selected a set of LEDs with average characteristics, and planned a low current ageing test as described in the following. The LEDs were stressed by means of a HP4155A Semiconductor Parameter Analyzer at $20mA$ dc, room temperature. The stress current value is the nominal current of the analyzed devices: this value is sufficiently low to avoid self-heating and prevent dopant instabilities due to thermal effects [76, 8], as described in the following. In order to analyze short-term effects, the full stress had a duration of 100 hours, with logarithmic steps. At each step the samples were characterized by means of current-voltage (I-V), capacitance-voltage (C-V), capacitance-frequency (C-f) and optical power (OP) measurements. Deep Level Transient Spectroscopy (DLTS) analysis was also carried out during stress, in order to analyze the generation/modification of deep levels near/within the active layer. Optical parameters have been analyzed by means of Electroluminescence (EL), Cathodoluminescence (CL) and Photocurrent (PC) measurements during all stress time.

## 3.3 Measurements results

### 3.3.1 Thermal characterization

As described above, samples have been aged at 20 mA dc, RT. Before carrying out the ageing tests, a careful analysis of devices thermal resistance has been carried out, in order to understand if under the chosen stress conditions junction self heating is limited or if it is a significant driving force for degradation processes. Therefore, junction temperature has been evaluated by means of current-voltage thermal maps, using the method described by Xi and Schubert [111, 112].

A set of voltage measurements was carried out at different current ($I_m$ between 5 and 25 mA) and temperature ($T_o$ between 35 and 85 °C) levels in a thermal chamber. The measurements were carried out using short current pulses ($80\mu s$), in order to avoid devices self heating. Figure 3.5 shows that for each measuring current ($I_m$) level the relation between the corresponding voltage and temperature is roughly linear, and can be expressed by means of

$$V_f = A + BT_o \tag{3.1}$$

where $T_o$ is the oven temperature, A and B are fitting parameters.

The slopes of the curves in Figure 3.5 were therefore evaluated by means of linear fittings, and used as coefficients for junction temperature evaluation in the following analysis.

The chamber temperature was subsequently fixed at 35 °C, and the devices were biased for a fixed period (300 seconds) at each of the measuring current levels used before: during bias at fixed current, LEDs voltage decreased exponentially, due to junction self-heating.

For the same driving current $I_m$, a difference in forward voltage corresponds to a difference in devices operating temperature. Therefore, using the calibration data in Figure 3.5, and inverting equation 3.1 into

$$T_j = \frac{V_f - A}{B} \tag{3.2}$$

we could convert the voltage transient data into junction temperature transient data (see Figure 3.6).

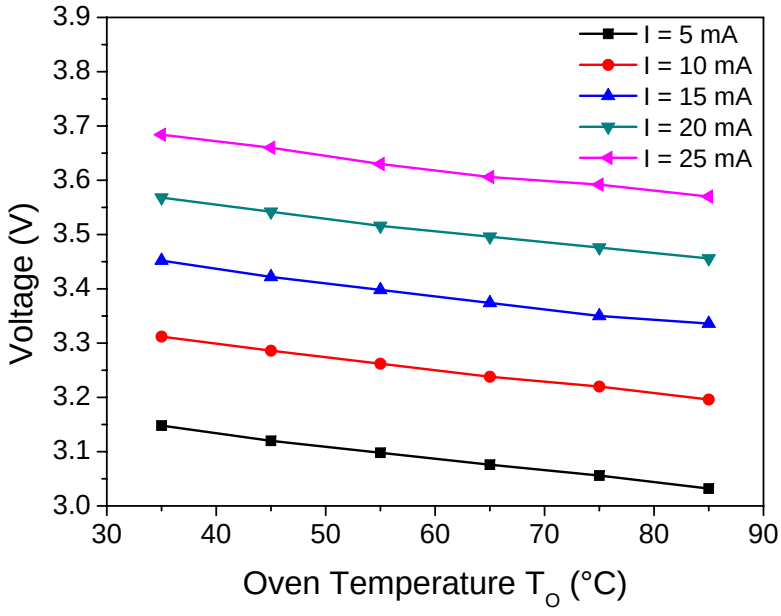



**Figure 3.5:** Junction voltage measured at different temperature and current levels by means of short current pulses

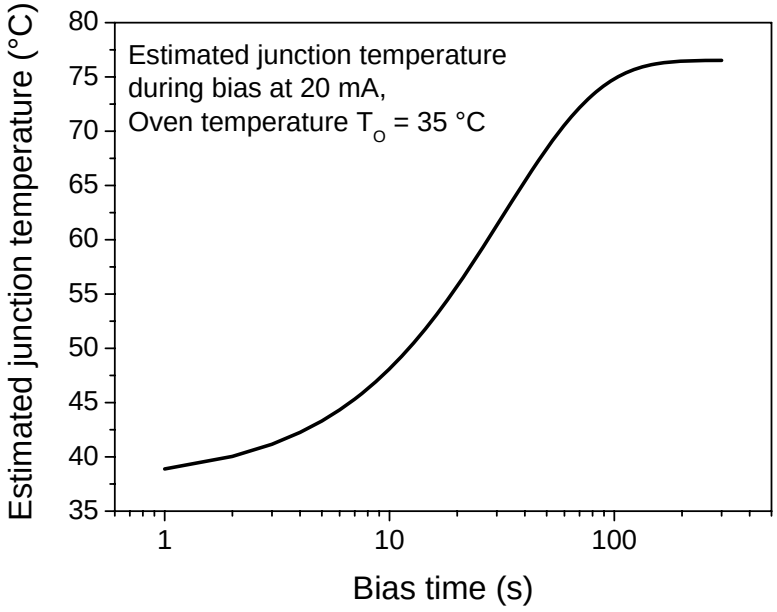



**Figure 3.6:** Estimated junction temperature during bias at 20 $mA$, Oven temperature $T_o = 35\ ^\circ C$

In this way we extrapolated the junction temperature ($T_j$) corresponding to operation at each measuring current level $I_m$. Therefore, we could plot the temperature vs electrical power diagrams for the analyzed devices: one example is reported in Figure 3.7. From this kind of diagrams, we have extrapolated the thermal resistance of the analyzed LEDs, that was found to be in the range 400-600 K/W depending on devices quality. These values are significantly high, due to the fact that they have been measured on LED chips mounted on a TO18 package with no heat sink. However, since operating current and power levels are low for these devices, we have found that during operation at 20 mA junction self heating is limited to 40 °C with respect to ambient temperature for all the analyzed devices (see Figure 3.6).

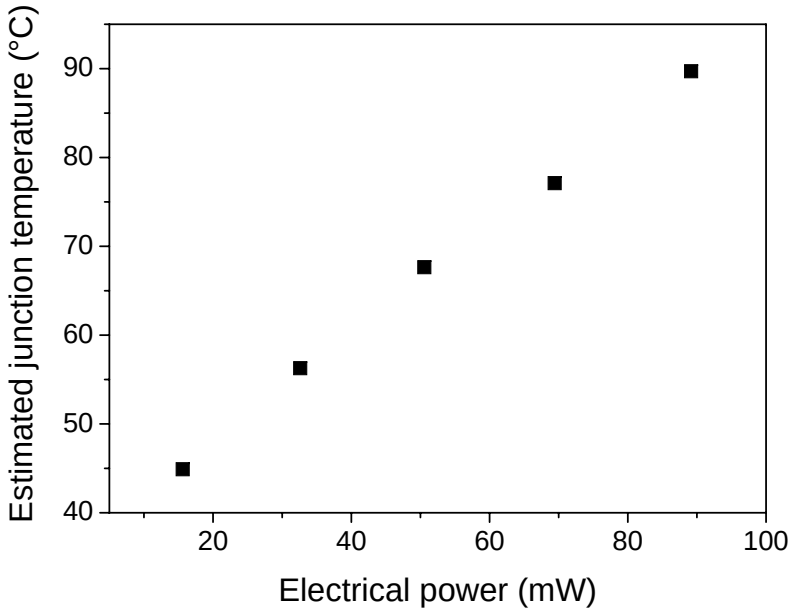



**Figure 3.7:** temperature vs electrical power diagram for one analyzed LED

Therefore, when the LEDs are operated at 20 mA dc, RT, junction temperature does not exceed 65 °C.

Considering that

- thermally activated degradation processes can have high activation energy (up to 1.55 eV in [113] and references therein)
- in short stress times ($\approx 100h$) pure thermal degradation has been reported in literature only for temperatures greater than 180-200 °C [11, 9, 14, 113]

this temperature level is too low to introduce LEDs thermal degradation and doping instabilities [76, 8]. Therefore, stress effects observed during low current ageing can be attributed to carrier flow and not to self-heating effects.

### 3.3.2 Optical power measurements

Optical power measurements were carried out using a Newport 1830C Optical Power Meter, equipped with a Newport 818-UV Photo Detector. Changes in emission intensity during the 20 mA aging test, measured at three different current levels, are shown in Figure 3.8. At the nominal current of 20 mA the power loss never exceeded 8 %, while a more significant percentage loss was measured at low currents (see the 2 mA curve in Figure 3.8). The decrease took place during the initial 20 hours. In the remaining 80 hours a stable behavior was observed.

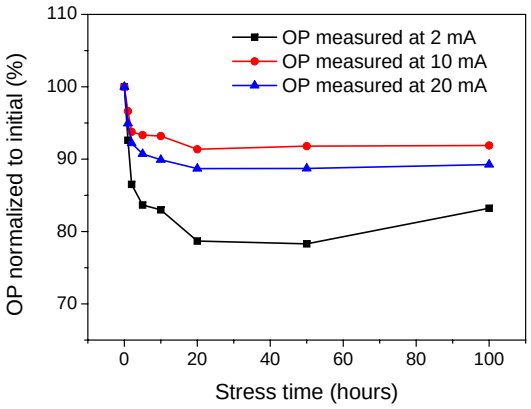
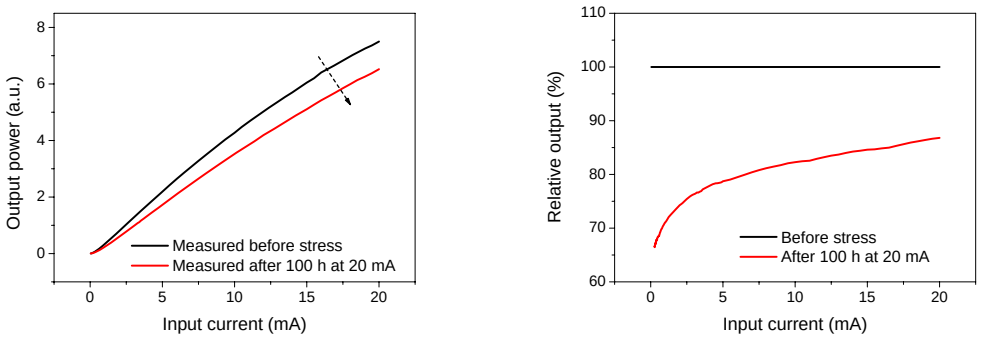



**Figure 3.8:** Normalized optical power measured at 2, 10 and 20 mA during stress at 20 mA dc

Figure 3.9(a) shows the output power vs input current (L-I) curves measured on one aged LED before and after stress. These curves can be divided in three zones: for low currents (here for $I < 2mA$) the L-I characteristic is non linear, as a result of the predominance of non radiative recombination. For intermediate current values (here for $2 < I < 10mA$) the curve is almost linear, as a result of the radiative recombination dominating in the active layer. For high current levels (here for $I > 10mA$) a sublinear zone can be identified, related to *(i)* self-heating effects, *(ii)* carrier overflow, *(iii)* radiative path saturation, that worsen the quantum well efficiency.



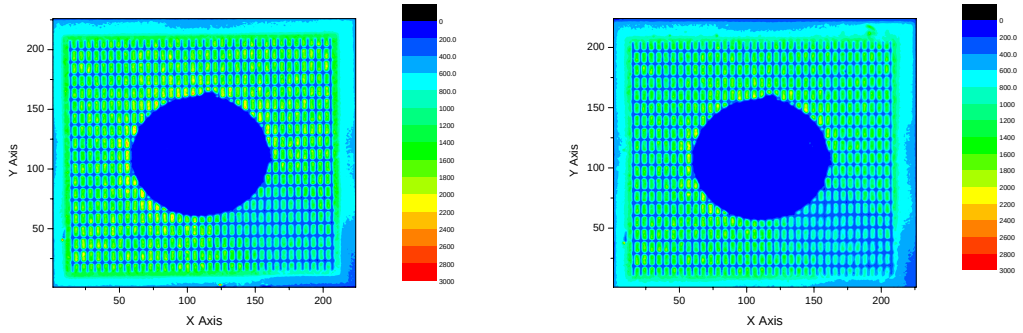

(a) (b)

**Figure 3.9:** (a) Normalized optical power measured at 2, 10 and 20 mA during stress at 20 mA dc; (b) Comparison of normalized light current (LI) characteristics of a blue LED before and after aging

Figure 3.9(b) shows the ratio between the red curve and the black curve in Figure 3.9(a), i.e. the light intensity of the aged sample normalized to the intensity measured before aging. This diagram represents the entity of the optical power decrease measured at the different current levels after the 100 hours stress test. As can be noticed, degradation effects were more prominent at low measuring current levels. This fact suggests that emission decrease is related to the generation of non-radiative recombination paths: these paths are saturated at high measuring current levels, and the effect of the increased nonradiative recombination is weaker [114, 115, 20, 116].

Figure 3.10(a) and 3.10(b) show the false color emission pattern measured at LEDs surface before and after the 100 hours stress tests. Measurements were carried out by means of a PHEMOS 1000 Light Emission Microscope. As can be noticed, both before and after stress the emission profile of the devices was uniform, indicating good current and emission spreading. No crowding of the emission around the central contact was therefore detected as a consequence of low current stress. In literature, emission crowding is usually attributed to the degradation of the resistivity of the contact and metal layers [11, 30, 9, 14]. The fact that the analyzed devices did not show any significant degradation of their emission pattern indicates that the chosen stress conditions do not affect the current and emission spreading, and suggests that stress does not imply a significant degradation of the resistivity of the semiconductor and

contact layers. The results of the I-V measurements described in the following give a confirmation in this direction, showing that stress does not imply an increase of the parasitic series resistance of the samples.




(a) (b)

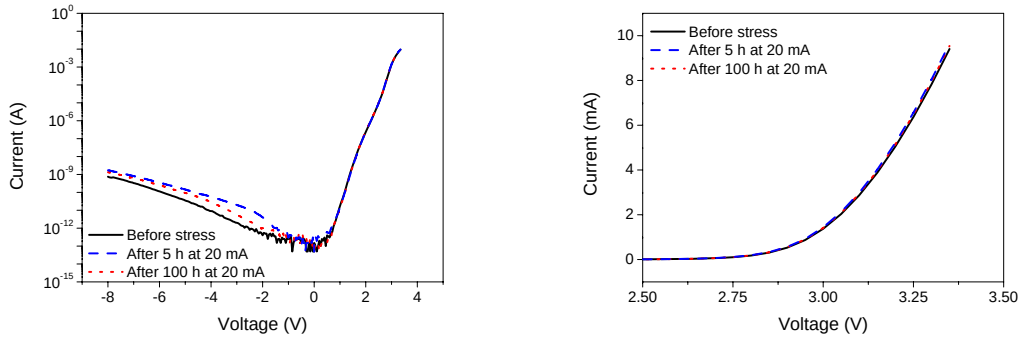
**Figure 3.10:** emission microscopy images measured at 10 mA (a) before and (b) after the 100 hours stress at 20 mA

### 3.3.3 Current-Voltage characterization

The current vs voltage (I-V) measurements were carried out by means of an HP4155A Semiconductor Parameter Analyzer, at room temperature. Before stress, the individual devices (coming from the same wafer) showed identical forward I-V curves, while the reverse current was slightly different from sample to sample, possibly due to different dislocations densities [117, 104, 103].

Stress did not modify the forward region of the I-V curves (see Figure 3.11(b)): therefore, no increase in parasitic series resistance of the samples took place as a consequence of stress. This fact suggests that the contact and semiconductor layer resistivity are not significantly affected by low current treatment. On the other hand, stress was found to induce an increase in reverse current, enhanced during the first part of the stress (see Figure 3.11(a)).

The magnitude of this reverse current increase was different for each of the analyzed LEDs: this fact suggests that this process is due to mechanisms depending on samples quality, such as generation/propagation of threading dislocations in the active region [117] and/or modifications of the surface states at the mesa sidewalls.




(a) (b)

**Figure 3.11:** Current-voltage curves measured on one LED at different steps of the 20 mA stress test. Curves are plotted in (a) semi-logarithmic and (b) linear scale

### 3.3.4 Capacitance-Voltage characterization

Capacitive measurements were carried out by means of an HP4284A LCR Meter; a parallel $C_P - G_P$ model was adopted for the heterojunction. The curve in the inset of Figure 3.12 shows the dependence of capacitance on frequency (C-f diagram), measured at -0.5 V, room temperature on one untreated sample. Two plateau regions, the low frequency and the high frequency ones, can be clearly seen in the C-f diagram. A deep level with a transition frequency of about 4 kHz can be identified [118].

The apparent charge distribution (ACD) profile of the devices can be extracted from capacitance-voltage (C-V) measurements as described in Chapter 2 and in [29, 119, 108, 109]. The model used for these LEDs assumes the junction to be unilateral, with the p-side more heavily doped ($p \gg n$) with respect to the n-side: for this reason the profile extracted from the C-V measurements is referred to the n-side. It is worth noticing that this assumption introduces a slight approximation in the determination of the apparent depths and levels, since the charge concentration at the p-side is not infinite, and the space charge region (SCR) extends both at the p and at the n side.

The C-V measurements were carried out at different frequencies: 300 Hz, 100 kHz, 1 MHz. As shown in the inset of Figure 3.12, the first value corresponds to the low frequency plateau of the C-f curves, while the other two correspond to the high frequency region: these last values gave similar results. Here we show the data

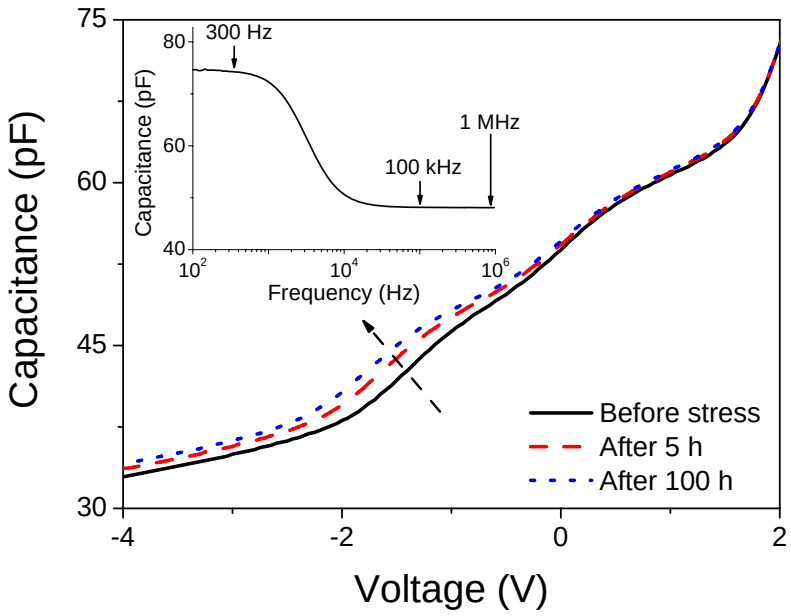



**Figure 3.12:** C-V measurements carried out at 1 MHz before and during ageing test. Inset: C-f curves measured at -0.5 V, RT

obtained with a 1 MHz measuring signal: such a high value allowed us to obtain a good signal to noise ratio and to reduce the contribution of the diffusion capacitance on the measured capacitance for forward bias values, providing reliable junction capacitance measurements also for low positive voltages [120].

In Figure 3.12 are shown the results of the C-V measurements carried out before and during the ageing test at 1 MHz. The solid curve corresponds to the untreated sample. As can be noticed, the junction capacitance shows a step-like behavior. With the decrease of the reverse bias the boundary of the space charge region is swept through the barriers and the wells: as it moves inside the wells, the capacitance changes very slowly with voltage, due to the large amount of carriers [107, 108]. This behavior is characteristic of quantum-well structures. Ageing of the LEDs induced a junction capacitance increase, more prominent for reverse bias values (see Figure 3.12): in the inset of Figure 3.13 is shown the increase of the capacitance value as measured at -1 V, 1 MHz during stress. The results of the C-V measurements were processed in order to obtain the apparent charge distribution (ACD) profiles, that are shown in Figure 3.13. For completeness, the same ACD data are plotted as a function of junction voltage in Figure 3.14.

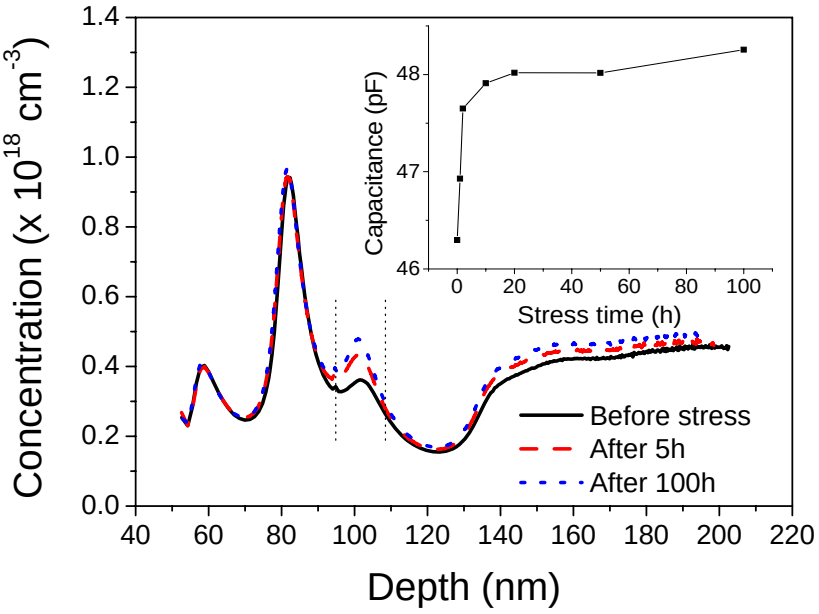



**Figure 3.13:** apparent charge profile of one LED and its variation during stress (100 h at 20 mA dc). Inset: junction capacitance measured at 1 MHz, -1 V during stress.

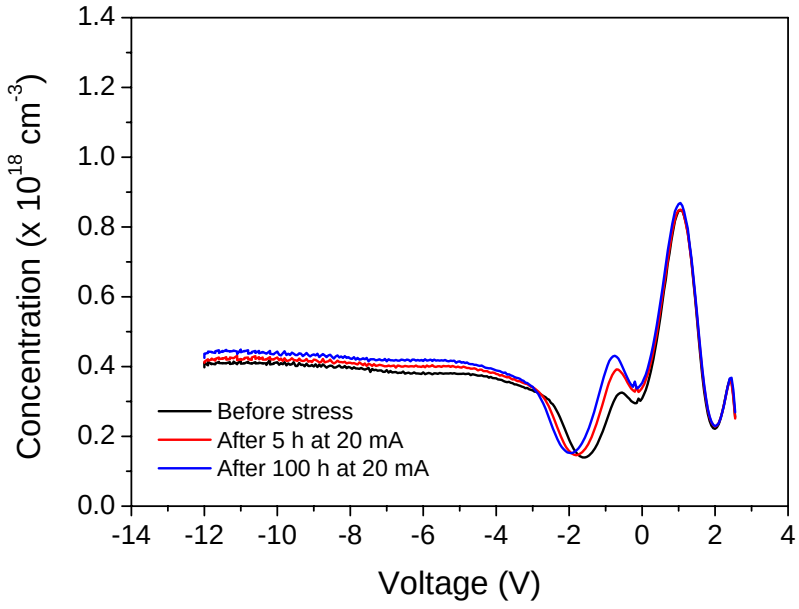



**Figure 3.14:** apparent charge profile of one LED plotted against junction voltage, and its variation during stress (100 h at 20 mA dc)

The solid curve in Figure 3.13 is referred to the untreated samples. The junction is considered to be in x=0. The spatial dependence of this charge profile suggests that during voltage sweep the SCR boundary is moved through the active region (the peaks at 60, 80 and 100 nm) and the n-side (for greater depths) [29, 119, 108, 107].

It is worth noticing that the position of the peaks does not exactly correspond to the position of the heterointerfaces in the LEDs due to the fact *(i)* that the profiles are extrapolated considering an ideally asymmetric junction ($p^{++}/n$) and *(ii)* that ACD profiles are extrapolated from high frequencies C-V measurements. At high frequencies, junction capacitance is lower than at low frequencies, due to the influence of the trap level detected by means of the C-f characterization (see the inset of Figure 3.12), and this fact introduces a further modification in the determined apparent depths of the charge profiles with respect to actual values. However, we have preferred to analyze the ACD profiles extrapolated at high frequencies since *(i)* high frequency measurements are less sensitive to noise with respect to low frequency ones and *(ii)* a change of measuring frequency implies an approximation of the relative position of the peaks, but does not affect the shape and the positions of such features in the profiles.

The changes in the C-V measurements described above are reflected by an apparent charge increase. This increase is mostly localized in one peak of the ACD (near 100 nm), suggesting that the strong changes took place near the interface between the active layer and the n-side of the diode, and/or in one of the quantum wells that compose the LEDs active region. Ageing induced also an uniform ACD increase for higher depths (greater than 140 nm).

In Figure 3.15 are shown: *(i)* the optical power decrease measured at 2 mA during stress (normalized to initial value) and *(ii)* the apparent doping increase at 100 nm (normalized to initial value). As can be recognized, during stress the kinetic of the efficiency loss is strongly related to the capacitance and ACD modifications: a connection between the optical power (OP) decrease and the changes in the charge distribution can be established.

The strong localization of the ACD increase suggests that the changes took place mainly near the border of the active region, at the interface with the n-side. These variations may be related to the generation or modification of levels or interfacial states near the border of the active region, which can locally change the charge profile,

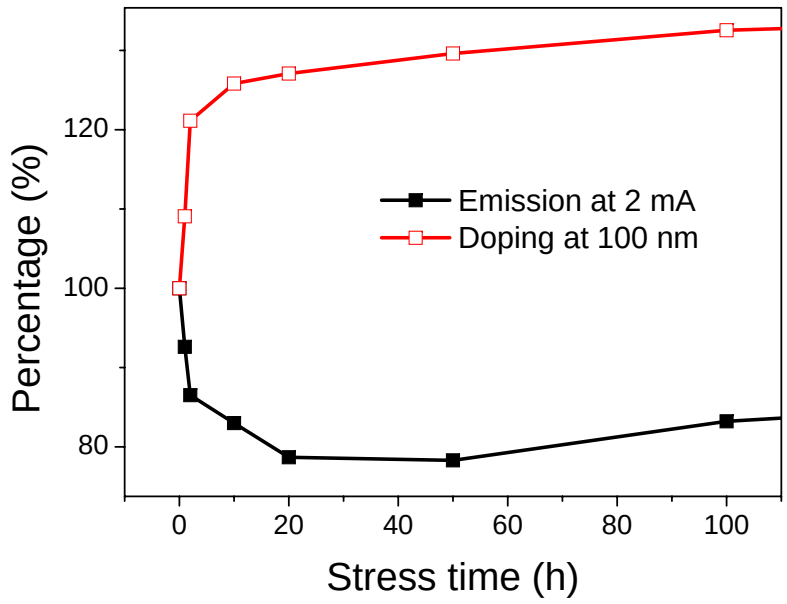



**Figure 3.15:** emission decrease (at 2 mA) and charge increase (at 100 nm) measured during stress at 20 mA

modify the the efficiency of carrier injection in the quantum-wells, and/or contribute to the generation of non-radiative paths in the bandgap. Also the slight and uniform ACD increase detected for depths greater than 140 nm (bulk region) possibly reflects a generation and propagation of defects. These hypotheses have been explored by means of Deep Level Transient Spectroscopy (DLTS).

### 3.3.5 Results of DLTS analysis

The capacitance transients were analyzed by means of a SULA Technologies Deep Level Spectrometer with an exponential correlator. DLTS analyses were performed with reverse bias and filling pulse values selected accounting for the ACD profile resulting from the C-V characteristics. The ACD profiles (see Figure 3.13) present a peak region, which could be attributed to the active quantum well layers according to literature [108]. The major changes in the ACD profile with increasing stress time were detected in correspondence of the peak on the bulk side, centered at about d=100 nm from the junction and nearly 20 nm broad. This region is swept by the Space Charge Region (SCR) boundary when the biasing voltage varies from 0 V to -1 V.

Accordingly, in the DLTS measurements reverse bias and filling pulse amplitudes were set to $V_{rev} = -1\ V$ and $V_{fill} = 0\ V$, respectively, enabling us to monitor whether the changes detected in the ACD profile correspond to modifications of deep electronic levels in the same region (between the two dotted lines in Figure 3.13) [20]. The changes occurring in the DLTS spectra as a function of the stress undergone by the LEDs are shown in Figure 3.16.

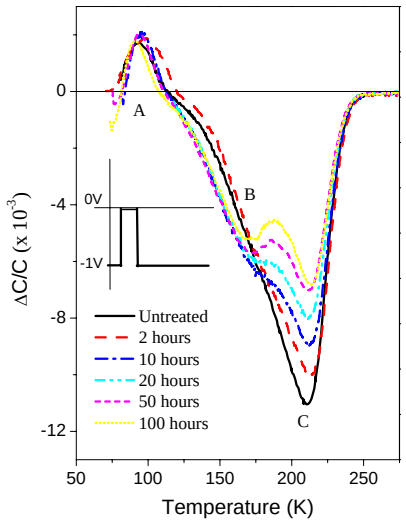



**Figure 3.16:** DLTS spectra obtained after successive stress steps. Spectra are collected with reverse bias $V_{rev} = -1V$ and filling pulse $V_{fill} = 0V$. The emission rate is $e_n = 46.5s^{-1}$

In the unstressed sample two peaks are detected, a positive peak A and a broad negative peak C, the parameters of which are listed in Table 3.1. After the first stress steps, the amplitude of peak C decreases and a shoulder on the low-temperature side of peak C becomes visible. After 50 hours stress, the initial peak C clearly splits in two, the aforementioned shoulder becoming the peak here labeled B (Table 3.1).

Meanwhile, peak A does not undergo any modification. Figure 3.17 reports the amplitude dependence of peaks B and C on the aging time. Peak C undergoes a significant amplitude reduction, about 40% after 100 h stress, while the amplitude of peak B remains almost constant after the first stress steps, and then slightly decreases after 10 h stress. The amplitude reduction of peak B does not exceed 12% with respect to its initial value even if it is difficult to state how this change is connected to the

| Deep Level | Energy (meV) | Capture section ($cm^2$) |
|---|---|---|
| A | 180 | $9 \cdot 10^{-14}$ |
| B | 180 | $5 \cdot 10^{-19}$ |
| C | 170 | $10^{-20}$ |

**Table 3.1:** Parameters of the deep levels found by DLTS in the active region of the LED

modifications occurring to peak C, whose low-temperature tail partially overlaps peak B.

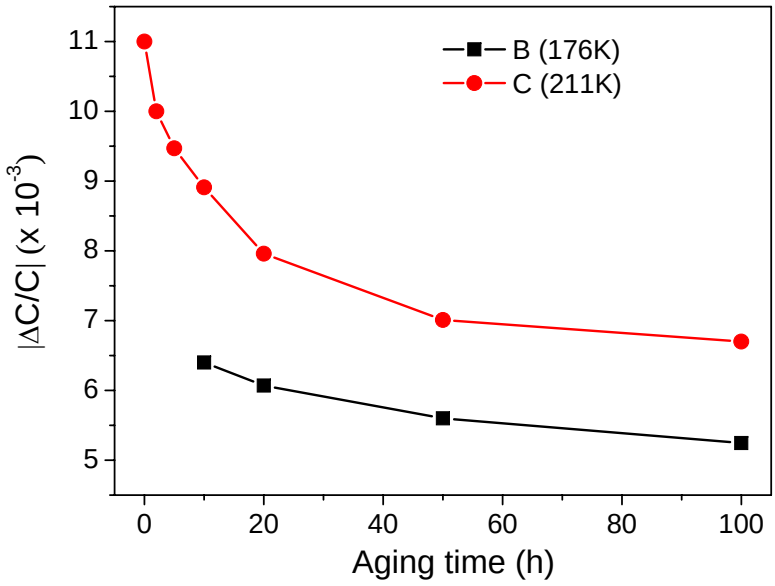



**Figure 3.17:** Evolution of the amplitude values of the DLTS peaks B and C versus the aging time

From the Arrhenius plot (Figure 3.18) it results that the activation energies of all these levels are in the range 170-180 meV, whilst the capture cross sections significantly differ from each other. It is worth noting that the negative peaks B and C are expectedly associated with majority carrier traps, while the positive sign of peak A does not mean that this peak is related to minority carrier traps. In fact, it was detected in a temperature interval where the high value of the series resistance can significantly affect the capacitance measurements. Peaks B and C are detected in a temperature interval where emission by dislocation-related states has been observed [121, 122]. Further

investigation is under way in order to ascertain whether B and C are associated with deep levels with potential barrier.

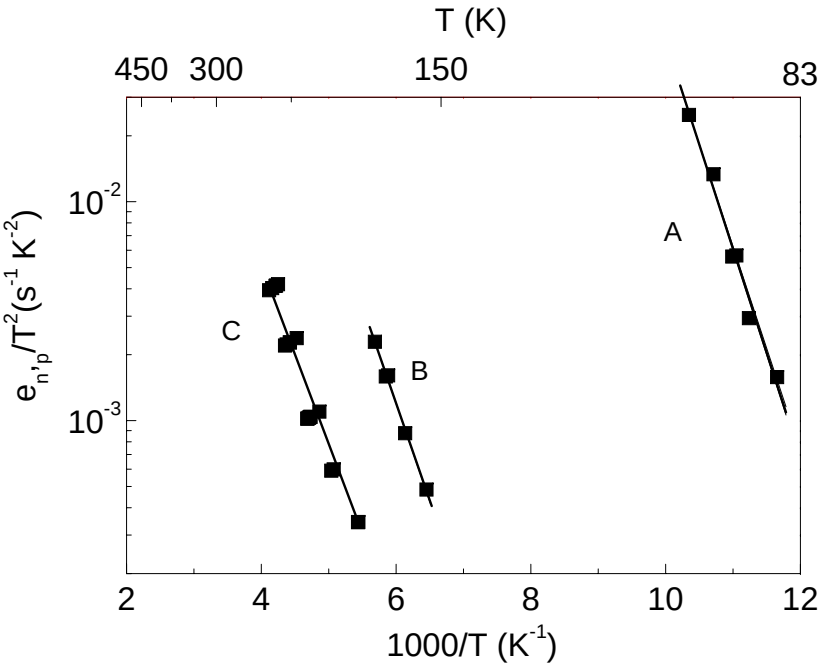



**Figure 3.18:** Arrhenius plot of the energy levels detected

These DLTS results could give rise to two different interpretations:

- the decrease of peak C is ascribed to the concentration reduction of the related deep level, possibly due to the dissolution of the relevant defect
- the decrease of peak C is due to the stress-induced introduction/generation of other deep levels associated with minority carrier traps

Further analysis is underway by differently biasing the device to establish the origin of the decrease of the amplitude of peak C and then to distinguish between these two hypotheses. Comparing the results of DLTS with the ACD profile (Figure 3.13), we can establish a connection between the net increase in the apparent charge density in the bulk side of the active region and the amplitude changes of peak C. Unfortunately, due to the device configuration (a heterostructure with quantum wells, having a strong non-uniformity of charge distribution) and to the polarizations used (aimed to probe exactly the bulk side of the active QW region), it is not possible to compare quantitatively the variations detected by C-V and DLTS. However, the dynamics appear to be quite similar for both ACD profile and trap C amplitude.

### 3.3.6 Results of the optical measurements

In order to better investigate the degradation of the optical parameters of the LEDs, we have carried out a detailed electro and cathodoluminescence analysis of the devices at each step of the ageing test. The EL spectra are dominated by a MQW-related peak, centered at about 2.72 $eV$ ($FWHM \approx 110\ meV$) for an operating current of 20 mA at RT (see Figure 3.19). At low temperature (Figure 3.19) the broadening is reduced and phonon replicas spaced by 90-100 meV, in agreement with the energy of longitudinal optical phonons, are resolved.

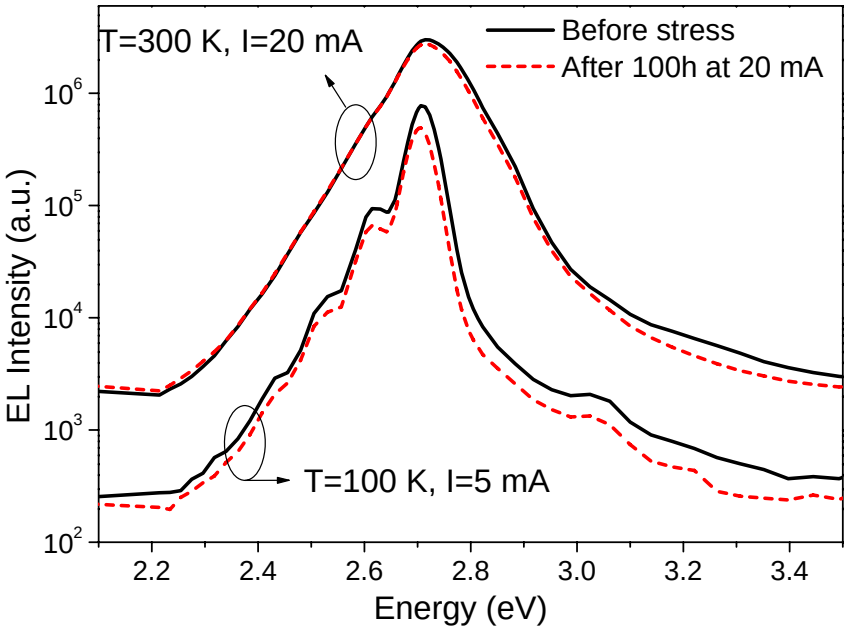



**Figure 3.19:** EL spectra before (solid line) and after (dashed line) the 100 h DC-aging, measured at: $T = 300K$ and $I = 20mA$, $T = 100K$ and $I = 5mA$

Yunovich et al. [123] proposed that the equation describing the luminescence band depends on the 2D density of states with exponential tail ($N^{2D}(\hbar\omega - E_g^{eff})$) and on Fermi functions $f_c(1 - f_v)$ according to

$$I(\hbar\omega) \approx N^{2D} f_c(1 - f_v) \tag{3.3}$$

$$N^{2D}(\hbar\omega - E_g^{eff}) = \left(1 + e^{\frac{\hbar\omega - \hbar\omega_{max} - E_0}{E_0}}\right)^{-1} \tag{3.4}$$

$$E_g^{eff} = \hbar\omega_{max} + E_0 \tag{3.5}$$

$$f_c(1-f_v) = \left(1 + e^{\frac{\hbar\omega - \hbar\omega_{max}}{E_1}}\right)^{-1} \tag{3.6}$$

where $\omega_{max}$ is the frequency of the maximum of the luminescence curve and $E_0$ and $E_1$ are fitting parameters describing the exponential fall on the low ($E_0$) and high ($E_1$) energy side of the QW peak, and can be estimated. In particular

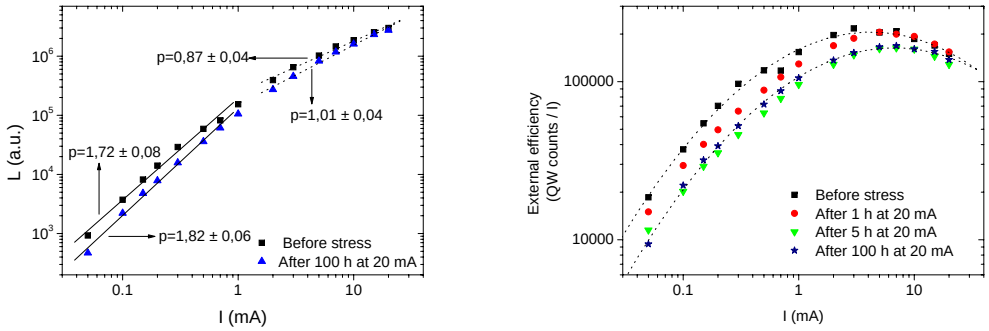
- $E_0$ is connected with interfaces' roughness, strain and microscopic potential fluctuations mainly due to alloy inhomogeneities and Coulombic impurity fields. In our samples it ranges between 50 and $60meV$, being independent of temperature and drive current between 0.5 and $5mA$ (weakly current-dependent at higher currents).

- $E_1$ shows a linear behavior as a function of temperature ($E_1 = mK_BT$) in the range $220 - 300K$ and results in $1.5 \leq m \leq 2.5$, as expected for a multiple quantum well structure. The experimental values found for $E_1$ indicate a good quality of the samples, being the hole localization near defects responsible for the high energy side of the QW line.

The electrical aging induces a reduction of the radiative optical efficiency, causing an intensity loss in the entire spectral range (Figure 3.19), likely indicating the aging affects both the QW layers and the p-layers (GaN and/or AlGaN). On the other hand, it does not affect the QW peak energy and it does not produce significant changes of the $E_0$ and $E_1$ values, as well as of the Huang-Rhys factor ($S \approx 0.14$ at $T = 100K$ for $I = 10mA$) describing the exciton-phonon coupling in the active region [99]. This fact points out that, within the sensitivity of these quantities, the stress at low dc current does not have major effects on the In distribution in the active layers.

As shown in Figure 3.8, the intensity reduction is produced mainly within the first few hours of stress. Furthermore, the intensity loss with respect to the unstressed value strongly depends on the drive current, as better evidenced in Figure 3.9(b). The low-current regime is clearly more sensitive to the aging effects. As stated above, this is consistent with the attribution of the intensity loss to an aging-induced generation of non-radiative defects, creating a recombination channel which is saturated and becomes therefore less and less effective when the drive current increases [114]. The observed aging effect modifies the light-current (L-I) and efficiency-current (L/I vs

I) characteristics. Figure 3.20(a) and 3.20(b) report these curves obtained for the unstressed and aged diode at room temperature, which is of applicative interest.




(a) (b)

**Figure 3.20:** Intensity (a) and external efficiency (b) of the test structure's QW EL emission versus the drive current, measured at different aging steps

The L-I curve (Figure 3.20(a)) follows the expected power dependence ($L \propto I^p$), with an initial non-linear part ($p \approx 2$) turning in an approximately linear ($p \approx 1$) region when the radiative recombination dominates [124]. The $p$ value in the low-current regime is often considered as indicative of the concentration of non-radiative centers, therefore the slight increase (from 1.72 to 1.82 after $100h$ of treatment) induced by the aging could suggest the creation of new defects or the increase of pre-existing center density.

It is interesting to note that the use of a different excitation source, in CL measurements, leads to similar results as for the degradation of the emission intensity. A decrease of the radiative transitions, the blue QW emission, the GaN excitonic emission and the broad defect-related yellow band, is found in the spectra acquired in the first 10 hours of aging. For the subsequent aging stages a constant value is maintained or a slight recovery is observed. Figure 3.21 shows the nearly exponential intensity decay of the QW emission as a function of the aging time. The intensity loss follows a dependence on the injected beam current of the same nature of that detected on the drive current in EL, i.e. the lower the injected current, the stronger the degradation effects.

The correspondence of the aging effects identified by means of EL and CLs rules out

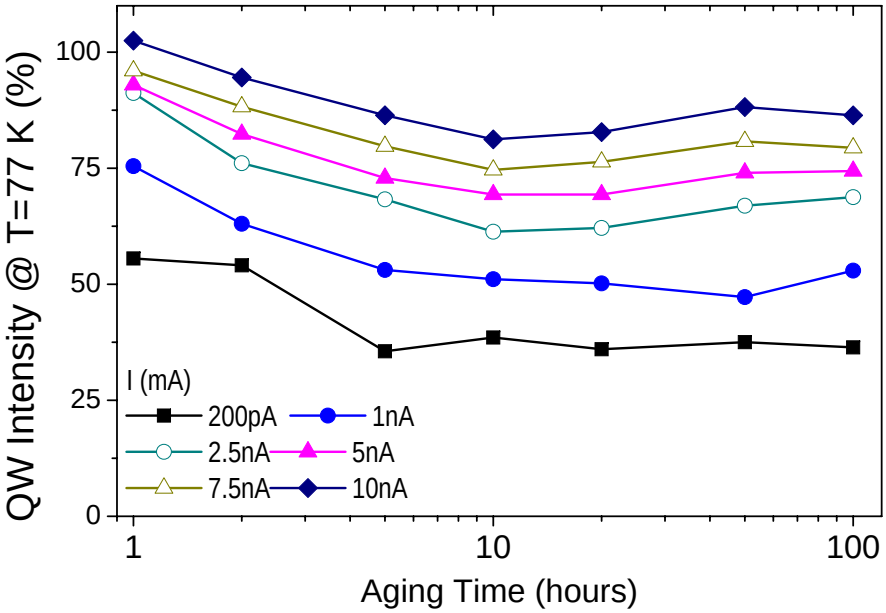



**Figure 3.21:** QW CL Intensity versus aging time ($T = 77K$), measured at different beam currents on the whole area of the sample. The beam energy is fixed to $20keV$, ensuring all the layers in the active region are excited

that the main degradation mechanisms can be ascribed to a damage of the electrical contacts. On the other hand, the CL results strengthen the attribution of the optical failure to a generation, due to the electrical stress, of non-radiative centres. This is suggested on the basis of the spectra collected at fixed injection power by varying the device temperature. As reported in Figure 3.22, the QW intensity loss, occurring mostly within the first hour of aging, strongly increases (up to even 70%) by increasing the temperature. This can be attributed to the growing role, as the sample is heated, of non-radiative recombinations, controlling the observed quenching of the QW transition for rising $T$, up to an almost complete disappearance above 250 K.

### 3.3.7 Photocurrent measurements

Measurements results described above indicate that low current stress can induce the generation of non-radiative recombination centers inside the semiconductor material. Capacitance-Voltage and DLTS measurements have indicated that these modifications take place near/within the active layer, indicating that stress worsens

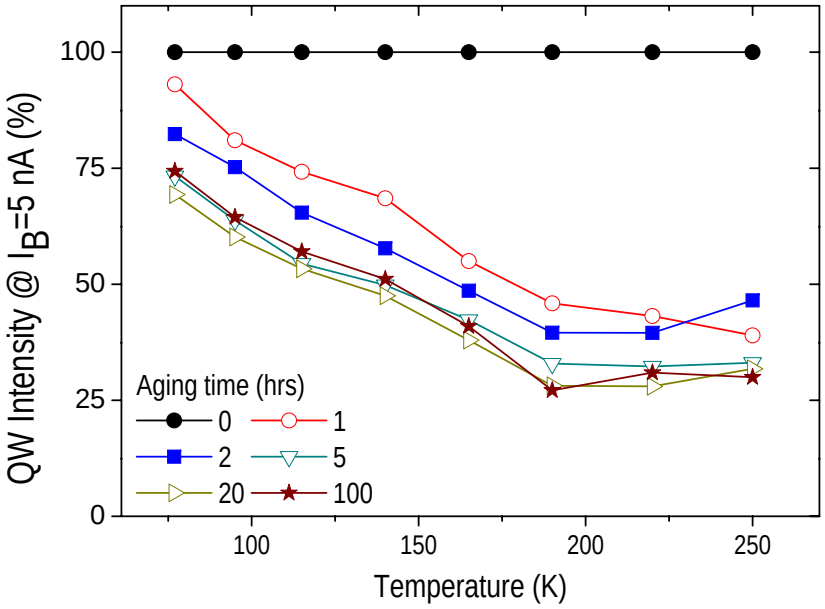



**Figure 3.22:** Temperature dependence of the QW intensity loss from CL data at several aging stages

the radiative properties of the devices. A confirmation of this fact has been obtained by means of photocurrent spectroscopy.

This technique allows to spectrally separate the contributions to the generated photocurrent into *(i)* carriers generated inside the QW system and *(ii)* carriers generated in the GaN material. The high energy part of the spectrum, above the bandgap of GaN, is due to carriers generated in GaN and in the QW (with a dominant part of GaN), whereas the low energy part of the spectrum, between the bandgap of QWs and GaN is only due to QW absorption (with exception of some band tailing effects from GaN bulk material).

Photocurrent spectra have been measured at room temperature; light from a QTH lamp with enhanced UV emission was chopped at $f = 16Hz$, monochromatized in a CornerStone 260 monochromator with spectral resolution equal to $1nm$ and shed on the sample. The photocurrent signal was collected by a SRS SR830 lock-in amplifier. In Figure 3.23 we report the PC spectra measured during stress at 20 mA on one LEDs.

As can be noticed, low current stress induces the decrease of the PC signal. From this signal, we analyzed the stress kinetics of two different spectral regions. The first region is the so-called GaN NBE peak, at $\lambda = 363nm$, corresponding to the energy

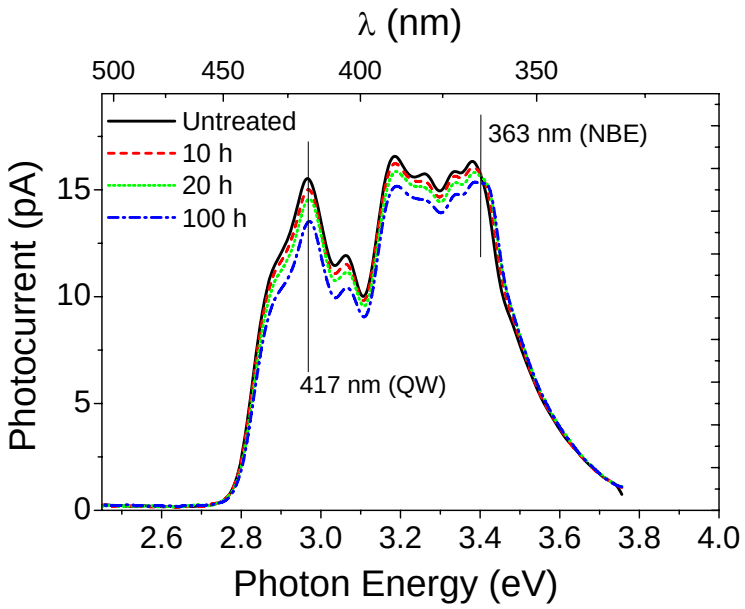



**Figure 3.23:** Photocurrent spectra collected on one aged sample at different stress times

$E_{NBE} = 3.40eV$, while the second region is the peak at $\lambda = 417nm$, which we labelled "QW" corresponding to the energy $E_{QW} = 2.95eV$. The signal at $\lambda = 363nm$ is related to carrier pairs generated both inside the QWs and in the GaN bulk material, while the signal at $\lambda = 417nm$ is related to carrier pairs generated inside the QWs only. The analysis of the stress kinetics of the different spectral components (Figure 3.24) indicates that PC collected at $\lambda = 417nm$ decreases about twice as much as PC collected at $\lambda = 363nm$.

It is thus apparent that the signal due to carrier pairs generated inside the QWs is more affected by current stress with respect to signal related to GaN transitions. Therefore, photocurrent spectroscopy indicates that the generation of non-radiative components taking place as a consequence of low current stress is mostly concentrated in the active layer of the LEDs. This fact confirms the results obtained by means of capacitive techniques, showing that stress induces modifications of the charge distribution, mostly localized close to the MQW region.

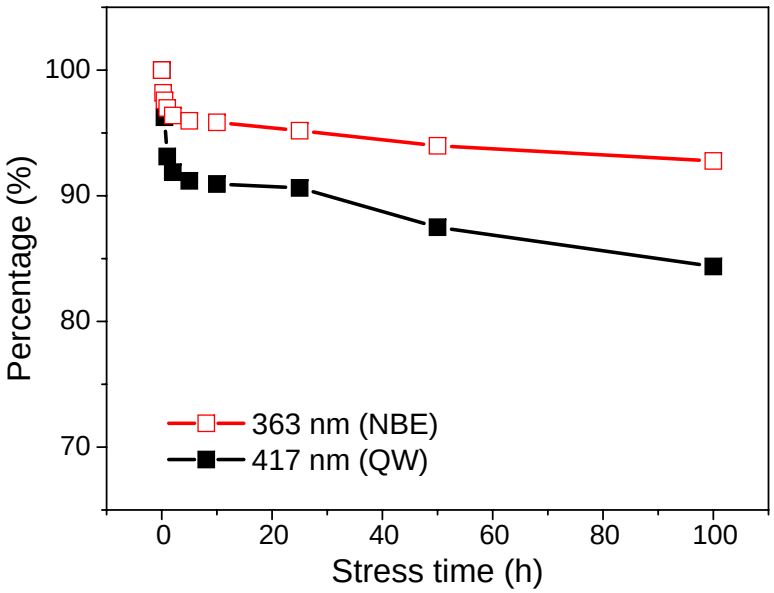



**Figure 3.24:** Time dependence of 417 and 363 nm photocurrent peak intensity during stress at 20 mA

## 3.4 Discussion and conclusions

In this chapter, we have described a detailed analysis of the effects of low current density stress on the electrical and optical properties of MQW LEDs. Analysis has been focussed on the so called *early degradation*, i.e. a rapid degradation of LEDs efficiency taking place during the initial stages of devices operation. Specific goal of this work has been the identification of the physical mechanism responsible for this phenomenon, by means of combined electro-optical analysis.

Stress was carried out at RT, biasing the devices at low current level ($32 A/cm^2$): in this way, junction temperature during stress was limited to 65°C, that is too low to induce thermally-activated devices degradation within the analyzed stress time interval. Stress effects can be therefore attributed to carriers flowing through the active layer of the LEDs, rather than to thermal mechanisms.

Stress was found to induce the decrease of the optical power emitted by the devices. OP decrease was mostly concentrated during the initial 20 hours of treatment, and was more prominent at low measuring current levels. The results of CL analysis confirm this trend: moreover, the CL characterization carried out at different temperature levels

indicated that the QW loss measured at high temperatures was stronger than at low temperatures.

The capacitance-voltage measurements showed that stress induced an apparent charge increase in the whole investigated semiconductor region, particularly pronounced at the interface between the active region and the bulk material, where during ageing a peak in the ACD profile grew. The modifications of the apparent charge profile and the optical power decrease had similar kinetics: this fact suggests that the worsening of the efficiency of the devices can be due to the degradation of the characteristics of the active layer, possibly due to the generation of defects and related trap levels. This hypothesis has been confirmed by carrying out a detailed DLTS analysis during stress.

The DLTS analysis, performed in the same region of the new ACD peak, showed, as a consequence of stress, significant modifications of the properties of traps at $170 - 180\ meV$ (traps $B$ and $C$). These localized modifications are supposed to be related to the generation of non-radiative paths, which lower the efficiency of the devices, especially at low current levels: at high current levels, these non-radiative paths saturate, thus leading to the minor OP loss shown by the EL and CL measurements.

The stronger OP loss shown at high temperatures by the CL measurements can therefore be attributed to the increase, as the sample is heated, of the non-radiative recombination rate. We believe that the generation/modification of trap levels didn't take place only at the active region boundary: an extended defect generation is supposed, since the ACD changed in all the region analysed by the C-V measurements, and the CL decrease didn't affect only the QW line, but also the GaN exciton and yellow bands. However, photocurrent spectroscopy showed that defects generation is stronger in the active region, with respect to the bulk material: this is due to the more defective structure of the QW region, that is composed by the superposition of materials with different lattice and thermal constants, and therefore can be more influenced by the ageing processes.

As previously described [125, 126], the generation/propagation of defects even at these low current densities can be related to a process of sub-threshold defect generation by hot electrons. The DLTS analysis doesn't explain all the ACD, EL and CL modifications: the generation of other defects with very deep nature can be

supposed, so that they are not detectable within the explored DLTS range, set by the need of avoiding exceeding device heating.

Finally, the modifications of the traps at the interface of the active layer (possibly contributing to tunnel-injection of the carriers inside the QWs) could also be related to changes in the capture efficiency of the active region, and thus contribute in lowering the overall LEDs efficiency. This hypothesis has to be confirmed by further measurements (e.g. I-V vs temperature), with the aim of characterizing ageing-induced variations of the transport mechanisms.

In conclusion, with this chapter we have presented a study of the degradation of the properties of the heterostructure of GaN LEDs during current stress. The analysis has been carried out by means of a capacitance-voltage, Deep Level Transient Spectroscopy, Electroluminescence, Cathodoluminescence and photocurrent study of short-term instabilities of InGaN/GaN LEDs submitted to low current stress. During the first hours of treatment, the EL and CL measurements showed an efficiency decrease, enhanced at low current levels. The ACD measurements showed an ageing-induced charge increase, well related to the OP decrease and to the deep levels changes detected by DLTS. This suggests that the efficiency loss is related to the generation of non-radiative paths, due to the generation/propagation of extended defects.

# Chapter 4

# High temperature reliability: role of passivation

This chapter describes an extensive analysis of the high-temperature reliability of GaN-based LEDs. Failure modes detected after high-temperature treatment include *(i)* optical power decrease, *(ii)* emission crowding and *(iii)* operating voltage increase. It is shown that devices degradation is related to the worsening of the properties of the LEDs ohmic contacts and p-type semiconductor layer. The efficiency degradation was found to be thermally activated, with activation energy equal to 1.3 eV. This failure mechanism of LEDs is attributed to the thermally-activated indiffusion of hydrogen from the passivation layer to p-type region of the diodes, with subsequent p-doping compensation and/or worsening of the transport properties of the p-side ohmic contact and p-type semiconductor. Furthermore, it is shown that the degradation process is reversible. In particular, passivation removal and subsequent annealing are sufficient for an almost complete recovery of the electrical and optical properties of the LEDs. Finally, it is shown that the use of a sputtered SiN passivation layer can be an effective alternative to usually adopted PECVD for the reduction of high temperature instabilities of GaN LEDs, due to its reduced hydrogen content.

## 4.1 Motivation

During the last decade, gallium nitride LEDs have shown to be very effective devices for many applications, because of their excellent properties, such as reduced energy

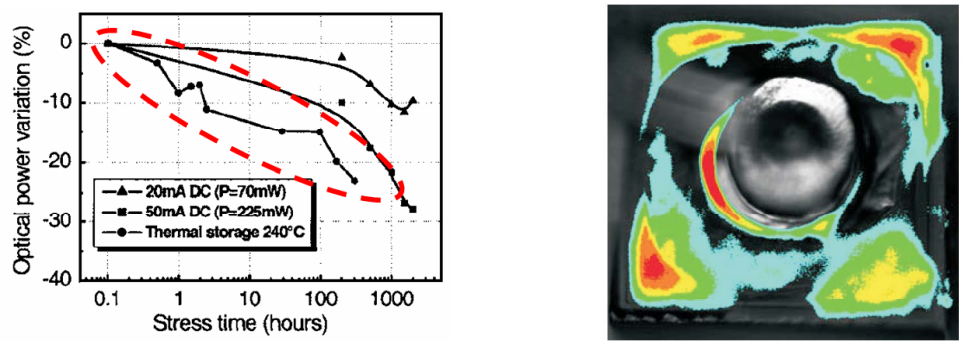
consumption, small dimensions, flexibility, fast response, high robustness and excellent lifetime (several 10000 hours). Indeed, these devices are currently used for indicators, traffic lights, store signs, automotive lights and in several other fields. In addition, advanced research indicates solid-state lighting as the most promising candidate for the next generation of light sources, for both domestic and commercial applications.

One of the factors which have limited the development of high-brightness GaN LEDs has been the difficulty of obtaining good p-type layers using magnesium as acceptor, due to the important role of the hydrogen introduced during growth process in compensating acceptor doping (see Chapter 1). Nevertheless, thanks to the intense research carried out during the last decade, the growth of high-quality p-type GaN films is now possible and well established: as widely described in literature, after growth the acceptor doping can be activated by means of low-energy electron beam irradiation (LEEBI) [60, 76] and/or an high temperature annealing [43, 71]. However, the stability of p-type GaN layers at high temperature levels is still under analysis [71, 74, 75, 8, 63], especially due to its implications in devices reliability.

During the last years a few authors have observed that GaN LEDs can fail during stress at high temperature/current levels. The main consequences of stress are:

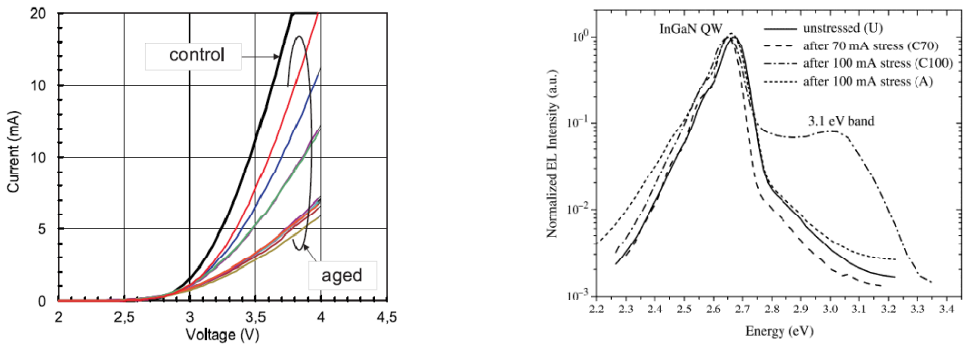
- optical power decrease, as described in [11, 9] (see Figure 4.1(a))
- emission crowding, as described in [11] (see Figure 4.1(b))
- series resistance increase, as described in [11] (see Figure 4.2(a))
- modifications of the spectral properties of the devices, as described in [25] (see Figure 4.2(b))

In these cases, temperature was considered to be a significant driving force for devices degradation. Degradation process has been attributed to the presence of hydrogen, which, at high temperature levels, can diffuse in the p-layer and generate Mg-H bonds with the acceptor atoms, thus compensating the overall active doping level and reducing device performance [71, 74, 75, 8]. Degradation of the LEDs has been therefore attributed to the worsening of the properties of the contact and semiconductor layer at the p-side of the diodes, that induce the non-uniformity of current flow (current crowding) and the subsequent reduction of the effective emissive area and OP decay.




(a) (b)

**Figure 4.1:** (a) Optical power degradation as a function of stress duration in GaN LEDs submitted to pure thermal stress and to dc stress as reported in [9]; (b) Emission microscopy taken in a LED after high current ageing as reported in [11]




(a) (b)

**Figure 4.2:** (a) I-V characteristics in linear scale of unstressed (control) and aged blue LED chips as reported in [11]; (b) Cathodoluminescence spectra measured before and after current stress as reported in [25]

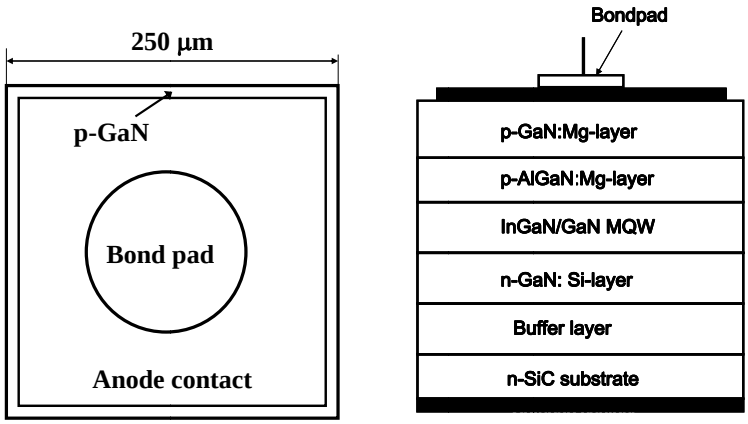
However, studies quoted above did not indicate which is the source of the hydrogen responsible of this degradation process. The aim of this chapter is therefore to show that a relevant source of the hydrogen compensating the acceptor doping during high temperature stress can be represented by the passivation layer, deposited by PECVD on the LEDs for chip encapsulation and surface leakage currents reduction. The experiments were carried out by comparing the behavior of GaN LEDs with and without a hydrogen-rich SiN passivation layer during thermal stress by means of a combined electrical and optical characterization. Furthermore, we demonstrate that the electrical and optical degradation related to passivation is completely reversible after passivation removal and subsequent annealing and that the use of sputtered SiN passivation layers can be effective in eliminating high temperature instabilities of GaN LEDs.

## 4.2 Analyzed devices and stress conditions

For this analysis we have used test structures grown by MOCVD, including MQW LEDs: the schematic structure of the samples is shown in Figure 4.3(a) and 4.3(b). The devices were grown on a silicon carbide substrate. The vertical structure consists in a buffer layer, a thick n-GaN:Si layer, an InGaN/GaN fourfold multi-quantum well, a p-AlGaN:Mg layer and a p-GaN:Mg contact layer. The structure was processed in order to obtain square devices, with a 250 $\mu m$ side. On half of the device wafer a SiN passivation layer was deposited by PECVD (and which contains hydrogen, as will discussed below), in order to enhance possible degradation effects, while the other samples were left without passivation. The tested chips were bonded on metallic packages (TO18) and the ohmic cathode contact was implemented with a bi-component conductive epoxy adhesive, ensuring good electrical and thermal characteristics.

Before stress the passivated and un-passivated structures were fully electrically and optically characterized, by means of current-voltage (I-V), capacitance-frequency (C-f), conductance-frequency (G-f) and emission microscopy measurements.

After this analysis, the devices with and without passivation were subjected to a thermal storage: equal samples were aged at different temperature levels, between 180 and 250 °C (with no applied bias). The stress duration ranged between 90 minutes and




(a) (b)

**Figure 4.3:** (a) schematic section and (b) top view of the analyzed structures

100 hours, depending on stress temperature. The steps had linear duration, and at each step the full characterization was repeated, in order to achieve a detailed description of the electrical and optical parameters during ageing, and to evaluate the different behavior shown by the samples with and without the passivation layer. Here we will describe the results obtained ageing the samples at 250 °C; the devices aged at the other temperature levels showed the same degradation mechanisms, taking place with different kinetics. The activation energy of the degradation process was calculated by comparing the different degradation kinetics shown by the samples aged at different temperature levels. After stress tests, the passivation layer was removed from the LEDs, using an $NH_4F - HF$ solution, and the devices were submitted to further thermal treatment at 250 $°C$. During this second annealing phase, the devices were characterized by means of OP, emission microscopy, and I-V measurements in order to detect possible recovery of their electrical and optical characteristics.

For the analysis described in this chapter, we have used LEDs coming from different growth and PECVD passivation processes, in order to analyze the dependence of degradation kinetics on devices technology. All analyzed samples with PECVD passivation layer showed similar degradation modes, taking place with different kinetics depending on technolgy process. The details on passivation deposition and p-layer growth are confidential, and can not be given here. However, this is not restrictive,

since the goal of this chapter is to give a physical description of the degradation processes taking place as a consequence of thermal treatment: this physical explanation has been necessary for the desing of passivation layers capable of guaranteeing stable LEDs operation at high temperature levels. The most reliable solution obtained as a consequence of this work is to use sputtering as an alternative to PECVD for the deposition of stable passivation layers: results are described in Section 4.7.

## 4.3 Measurements results

### 4.3.1 Optical power measurements

The graph in Figure 4.4 shows the integrated optical power (OP) degradation measured during thermal stress at 250 °C on the samples with and without PECVD passivation layer. As can be noticed, the high temperature stress induced a strong OP decrease only in the samples with passivation layer, which lost the 65 % of their efficiency at 10 mA after the 90 minutes test; the efficiency loss had nearly exponential time dependence, (time constant=$18 \pm 0.6$ *min* at 10 mA), and was more prominent for high measuring current values (Figure 4.4). On the other hand the un-passivated samples lost only the 5 % of their efficiency at 10 mA during the 90 minutes test (Figure 4.4).

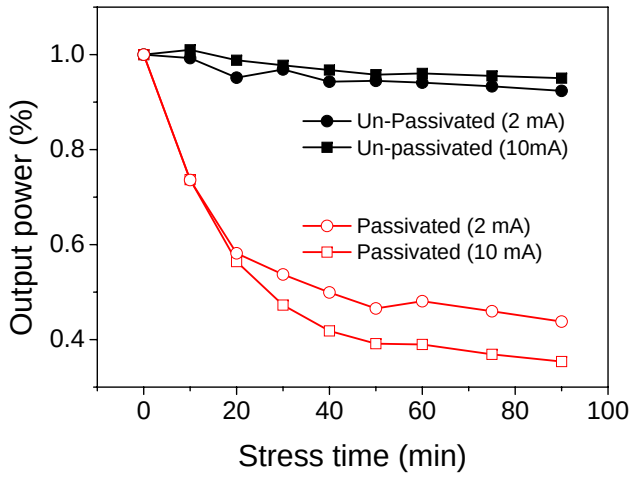



**Figure 4.4:** optical power measured at 2 and 10 mA for the passivated and un-passivated samples during the 250 °C stress

As stated above, the OP decrease was more prominent for high measuring current values. This fact is expressed also by Figure 4.5, that reports the optical power vs current (L-I) curves measured on one of the passivated LEDs during stress at 250 °C. In order to highlight the entity of the optical power (OP) decrease at each of the measuring current levels, we have normalized all the curves to the values recorded before stress.

As can be noticed, thermal treatment induced a 65 % OP decrease at the nominal measuring current of 20 mA. Degradation effects were found to be less pronounced for lower test current levels: this fact is consistent with previous studies that attribute OP loss and emission crowding to the increase of the parasitic resistance of the p-side of the diodes [9, 14]. In fact, both resistive and crowding effects are more effective in determining light output degradation at high current levels. It is interesting to notice that this behavior is exactly the opposite of the one described in Chapter 3 (see 3.9(b)), where the OP loss was more prominent at low current values, due to the fact that in that case the mechanism responsible for OP decay was the generation of non-radiative paths.

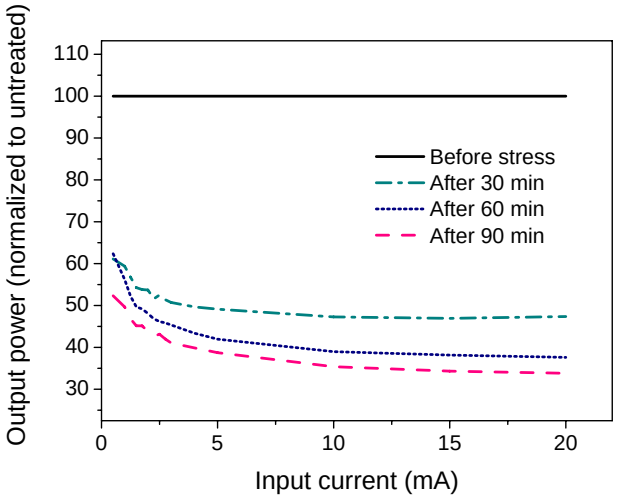



**Figure 4.5:** output power vs input current measured before and during stress on one passivated LED. Curves have been normalized to the values measured before stress

The OP degradation process was found to be thermally activated: Figure 4.6 shows the output power decay as measured on similar samples (from the same wafer) aged at different temperature levels, ranging from 180 to 250 °C. As can be noticed, for all

the stress temperature values, the OP decay has a nearly exponential behavior which can be efficiently described by

$$OP = 100 - K \cdot e^{t/\tau} \tag{4.1}$$

The value of the time constant $\tau$ of the OP degradation varied with stress temperature according to the exponential law

$$\tau \approx e^{E_A/kT} \tag{4.2}$$

Its value ranges from 18 minutes at 250 °C, to 1633 minutes at 180 °C. By plotting the value of the degradation time constant versus $q/kT$ (T=stress temperature), we obtained the Arrhenius plot shown in Figure 4.7. From this plot we estimated the activation energy of the thermally-induced degradation to be equal to $1.31 \pm 0.03eV$.

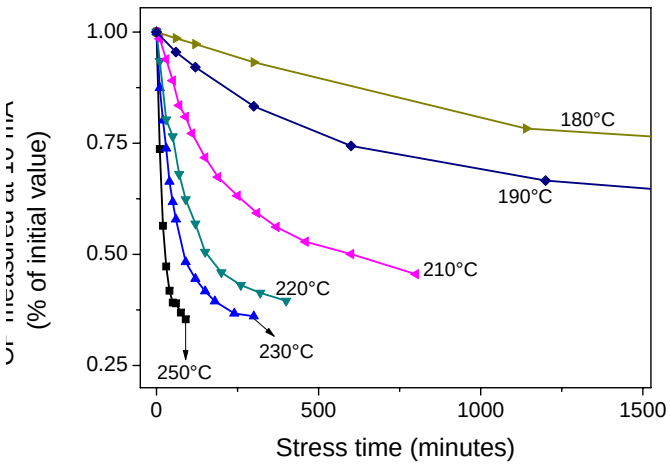



**Figure 4.6:** output power decay as measured (at 10 mA) during stress tests at different temperature levels ranging from 180 to 250 °C

The distribution of the light emitted by the surface of the LEDs was evaluated by means of a PHEMOS 200 Light Emitting Microscope. Figure 4.8(a) and 4.8(b) show the emission pattern of a passivated LED as measured before and after the 250 °C stress at 10 mA. As can be noticed, before stress the passivated LEDs showed a uniform emission distribution, indicating a good current and emission spreading. In the center of the diagram one can clearly notice the dark region corresponding to the bondpad (see the top view in Figure 4.3(a) for comparison). As can be noticed, as a

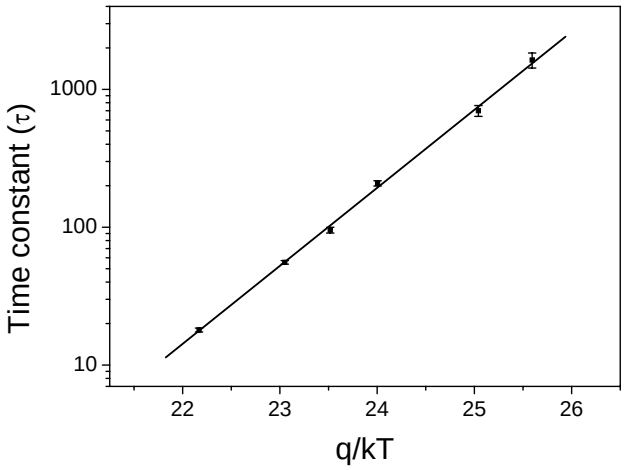
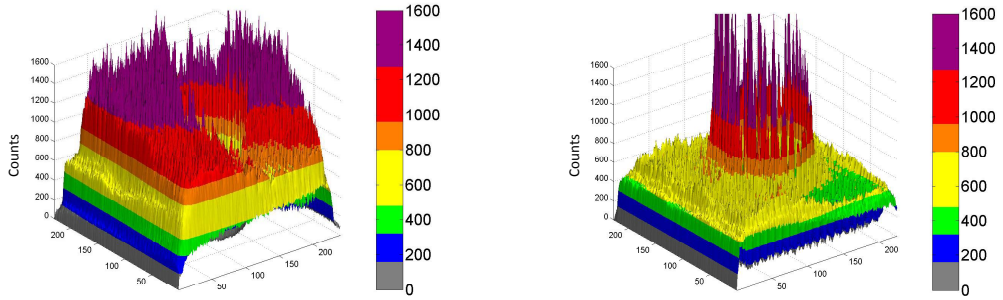



**Figure 4.7:** Arrhenius plot showing the degradation time constant (in minutes) plotted versus $q/kT$; the straight line is the linear fitting curve used for the estimation of the activation energy value

consequence of stress, the passivated LEDs showed a dramatic emission crowding: the intensity decreased far from the pad, while the emission loss was less significant near the contact. The intensity profiles of the LEDs without the passivation layer did not show any significant change as a consequence of stress.




(a) (b)

**Figure 4.8:** intensity profile of a passivated LED measured at 10 mA (a) before and (b) after the 250 °C stress

The kinetic of the changes of the emission pattern can be analyzed by measuring the intensity profiles on the median lines of the devices (linear intensity profiles): Figure 4.9 shows a schematic top view of an LED, and the region on which the intensity

profiles were evaluated. Figure 4.10(a) and 4.10(b) show the linear intensity profiles measured before and during stress at 250 °C on the passivated and un-passivated samples respectively. As described above, the intensity profiles of the untreated samples (solid lines in Figure 4.10(a) and 4.10(b)) were rather uniform; on the right hand side one can clearly notice the dark region corresponding to the bond-pad (region C in Figure 4.10(a)). Figure 4.10(a) shows the occurrence of the emission crowding phenomenon during stress: the intensity profile strongly decreased far from the pad (region A in Figure 4.10(a)), while the emission loss was smaller near the contact (region B). On the other hand, the intensity pattern of the un-passivated LEDs remained evenly distributed after stress (Figure 4.10(b)).

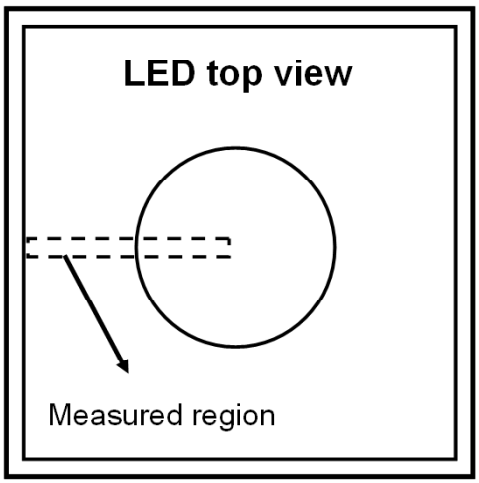
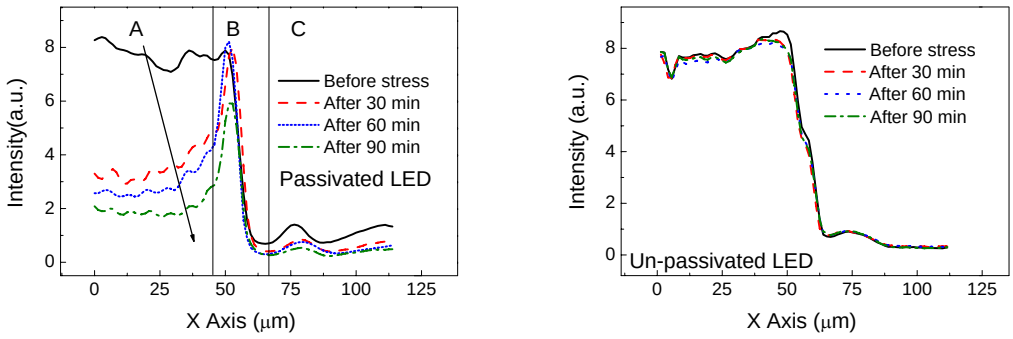



**Figure 4.9:** schematic top view of one LED, with the region on which the linear intensity profile was measured

### 4.3.2 Current-Voltage characterization

The I-V measurements were carried out by means of an HP4155A Semiconductor Parameter Analyzer. In Figure 4.11 and 4.12 are shown the forward current characteristics of one passivated sample before and during storage at 250 °C. As can be recognized, thermal overstress induced a lowering of the forward current in the medium-high voltage region ($V > 2.5\ V$). On the other hand, stress did not induce significant changes in the current-voltage curves of the samples without passivation (see the linear I-V curves in Figure 4.13).




(a) (b)

**Figure 4.10:** intensity profile emitted during stress by the region highlighted in Figure 4.9: (a) sample with passivation, (b) sample without passivation

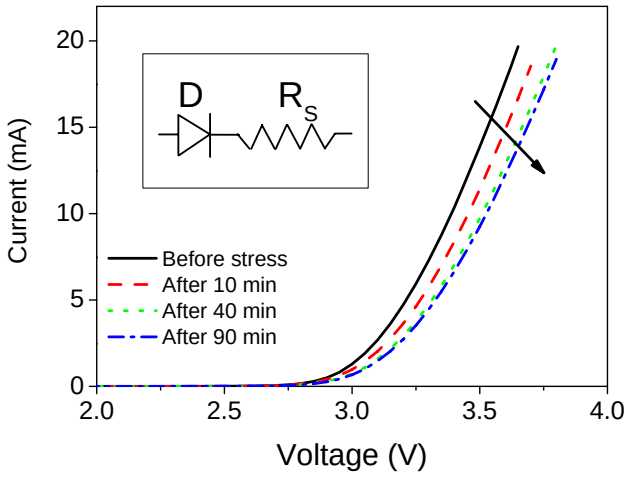



**Figure 4.11:** I-V curves measured of one LED with passivation before and during stress at 250 °C (linear scale)

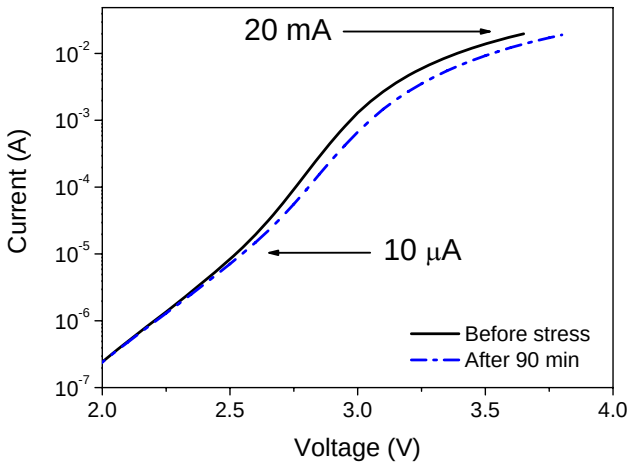



**Figure 4.12:** I-V curves measured of one LED with passivation before and after stress at 250 °C (semi-logarithmic scale)

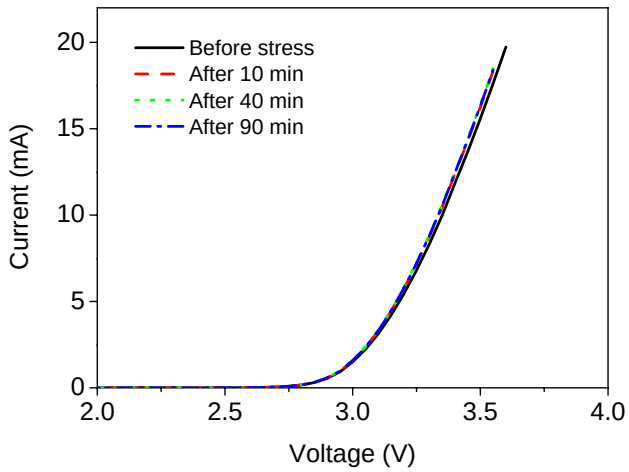



**Figure 4.13:** I-V curves measured of one LED without passivation before and during stress at 250 °C (linear scale)

In order to achieve a description of the modifications induced by stress on the electrical behavior of the samples with passivation, according to the simplified model in the inset of Figure 4.11, we estimated the series resistance $R_S$ and the ideality factor $n$ by fitting the I-V curves by means of

$$I \propto I_0 \cdot e^{\frac{q(V-R_S I)}{nkT}} \tag{4.3}$$

We carried out this analysis in the range between 10 $\mu A$ and 20 $mA$ (see the semi-logarithmic I-V plots in Figure 4.12). Figure 4.14 shows the series resistance and ideality factor modifications (normalized to initial value) measured for the passivated samples during stress: as a consequence of thermal treatment, the ideality factor was evaluated to increase from 3.48 to 3.97, while the series resistance grew from 22 to 25Ω. The modifications of $R_S$ were relatively small, and the slope of the I-V curves did not vary significantly after stress: for this reason it is reasonable to think that the stress-induced shift of the I-V curves towards higher voltages is mainly related to the variations of the ideality factor.

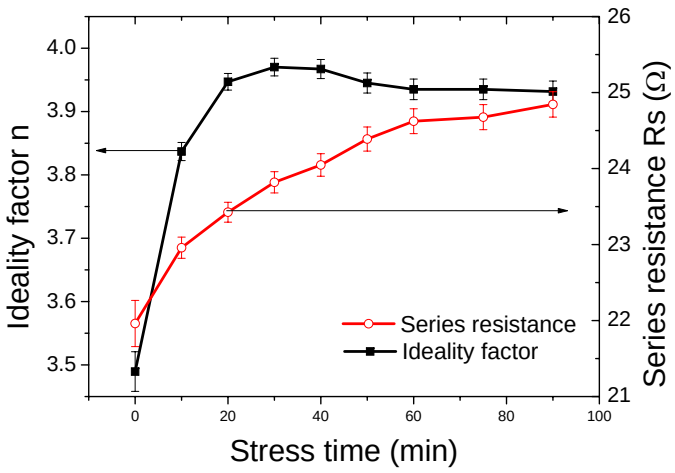



**Figure 4.14:** series resistance and ideality factor variation during the 250 °C stress (passivated samples)

As can be noticed, the ideality factor is much higher than the expected value of 1.0: these results are consistent with the data reported in literature. However, there is no agreement about the physical cause of such high values:

- Cao, Dmitriev and Eliseev attributed this behavior to tunneling ([96, 97, 98]);

- Franssen observed that while in simple pn junctions recombination occurs in the neutral regions (Shockley model), in MQW structures radiative recombination takes place mostly in the middle of the depletion layer, and this is expected to give rise to an increase of the ideality factor in the I-V characteristics ([99]);

- Shah attributed this behavior to the influence of the rectifying heterojunctions and metal-semiconductor junctions present in heterostructure diodes ([100]).

For what concerns the devices described within this work, tunneling is an important transport mechanism in the analyzed current range ([127, 128]), and can have an important role in increasing ideality factor value, as well as the efficient recombination processes taking place inside the QW region. On the other hand we cannot exclude a contribution of rectifying heterojunctions and metal-semiconductor junctions to this increase.

## 4.4 Discussion

With this work we have analyzed the high-temperature stability of GaN-based LEDs by means of combined electrical and optical characterization. In particular, we have analyzed the impact of the presence of the PECVD passivation layer on devices stability. Passivated and un-passivated LEDs have been therefore submitted to high temperature storage. As a consequence of stress, the passivated samples showed a significan efficiency loss, more prominent for high current values, together with emission crowding. On the other hand, the un-passivated diodes showed a reduced OP decrease, without emission crowding. The OP degradation was found to be thermally activated, with activation energy equal to $1.31 \pm 0.03\ eV$.The current-voltage measurements indicated that stress induced a series resistance and ideality factor increase only for the samples with the passivation layer. In summary, it was found that the presence of the PECVD SiN passivation layer can have an important role in limiting high temperature stability of GaN LEDs.

An hypothesis about the physical mechanism determining the degradation processes described above can be the following. During the PECVD passivation deposition process, the dissociation of precursors ($SiH_4$ and $NH_3$) can induce the incorporation

of hydrogen inside the passivation layer and/or at the interface between the passivation and p-GaN. Heating at $250°C$ can allow this hydrogen to interact with LEDs surface, possibly binding with magnesium and generating $Mg - H$ complexes [71, 76, 11, 9] and/or inducing the degradation of the ohmic contact at the p-side.

The ohmic contacts on p-GaN are usually obtained with high acceptor concentrations. A reduction of the active acceptor concentration, due to the interaction between hydrogen and magnesium, can worsen the properties of the anode contact, changing its transport characteristics, and vary the resistivity and injection properties of the p-layer, thus leading to the measured I-V modifications. It is worth noticing that also the anode metal layer can play a role in the measured degradation process: as described in Chapter 5, measurements carried out on ohmic contacts on p-GaN showed that stress can induce modifications of the characteristics of the contacts (i.e. rectifying behavior after stress), and slight modifications in the sheet resistance of the semiconductor. The results of this set of measurements indicate that important modifications take place near the metal/semiconductor interface, suggesting a possible role of the metal layer in the degradation process.

In the bondpad region, the presence of the thick metal layer obstructs hydrogen diffusion towards p-GaN (see Figure 4.15): for this reason, the degradation process is thought to take place mainly out of the pad region (see Figure 4.3(a)). Therefore, after stress, current should have a preferential path under the pad, and emission should be mostly concentrated in this region. This may be the mechanism concentrating the emission near the contact, and reducing the overall output power.

In order to clarify the role of hydrogen in the degradation process, we have submitted LEDs without passivation to thermal storage in different atmospheres, air and forming gas (hydrogen concentration = 5 %). As a result, we found that storage carried out in air did not induce significant degradation, while annealing in forming gas atmosphere induced optical and electrical degradation as observed on the LEDs with PECVD passivation: this is shown in Figure 4.16 which reports the output power vs input current curves measured on a LED without passivation before and after a 16 hours annealing carried out in forming gas atmosphere at 250 °C. This result confirms the important role of hydrogen in determining high temperature degradation of LEDs.

We think that passivation-related surface strain does not play an important role in

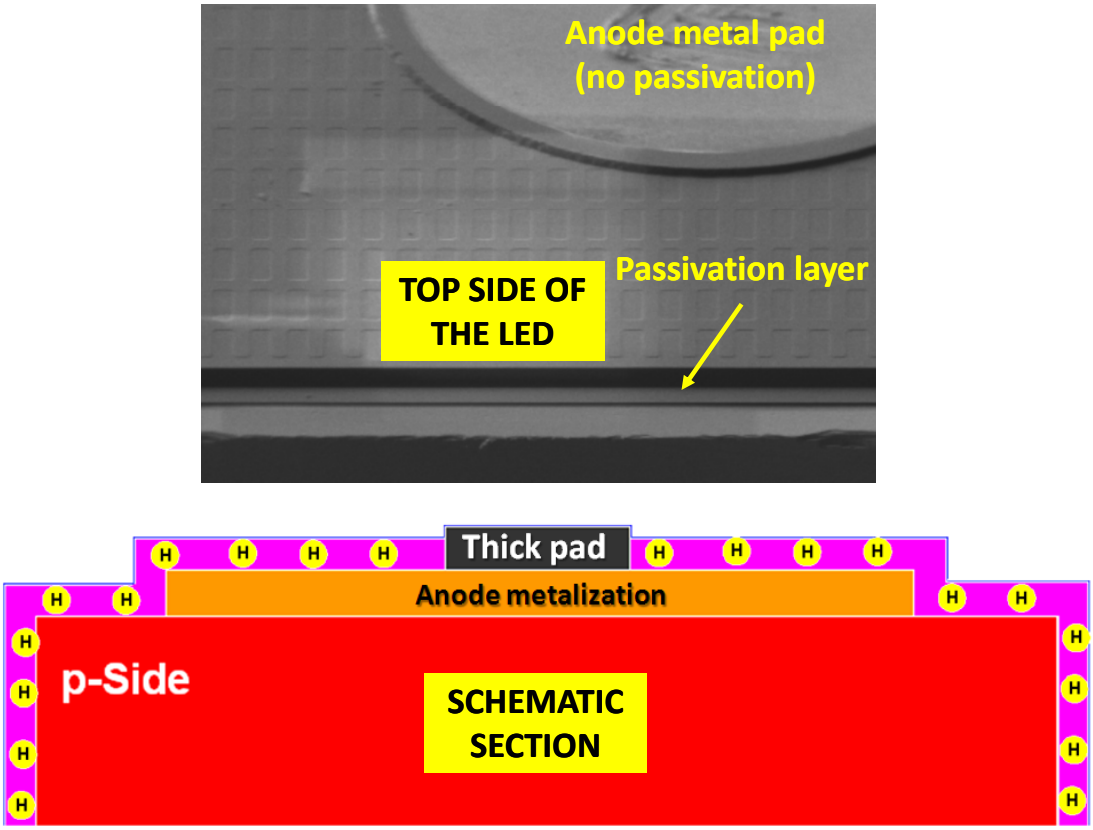



**Figure 4.15:** Top: SEM image of the top side of one of the analyzed LEDs. Bottom: schematic section of the surface region of the analyzed LEDs. It is worth noticing that the passivation layer does not cover the central pad.

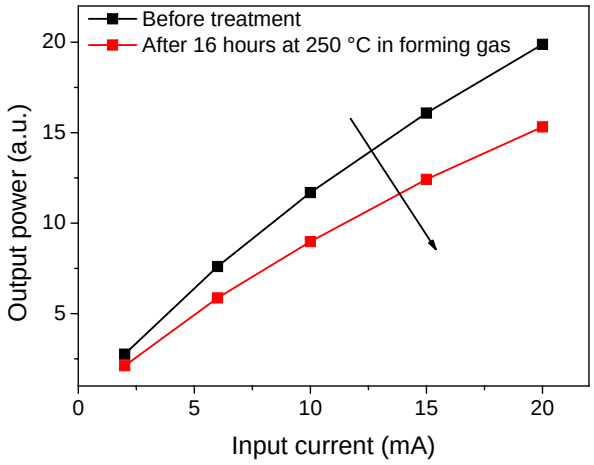



**Figure 4.16:** Output power vs Input current curves measured on an LED without passivation layer before and after a 10 h annealing at 250 °C in forming gas atmosphere

the described degradation process: a proof in this direction has been obtained removing the passivation layer from a set of aged devices. After the removal of the SiN layer (and of the related strain), the electrical and optical behavior of the degraded devices did not show any change, indicating that passivation removal is not sufficient to obtain an efficiency recovery, which was observed only after a further annealing.

## 4.5 Capacitive analysis of LEDs degradation

In the previous sections, we have indicated that a source of hydrogen responsible for this degradation process is represented by the passivation layer, usually deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) on LEDs surface, for chip encapsulation and surface leakage current reduction. The modifications of the optical power, emission profile and current-voltage characteristics have been interpreted in terms of degradation of the properties of the ohmic contact and semiconductor at the surface of the p-side of the diodes.

The properties and degradation of semiconductor and contact layers can be efficiently studied by means of capacitive and spectroscopic techniques ([108, 109, 118, 119, 20]. Therefore, in order to better understand the modifications taking place as a consequence of stress at contact/semiconductor level, we have carried out a detailed analysis of the characteristics of aged LEDs by means of capacitance-voltage, capacitance-frequency, Thermal Admittance Spectroscopy (TAS) and Deep Level Transient Spectroscopy. The analysis has been carried out on passivated samples, since high-temperature degradation effects have been detected only in presence of the PECVD passivation layer.

Figure 4.17 shows the C-V curves measured at 1 MHz before and during stress at 250 °C on one analyzed device. From these characteristics it is possible to calculate the activated donor density in the bulk, which was found to be $N_d = 4 - 5 \cdot 10^{17} cm^{-3}$ (see Section 3.3.4 and 2). As can be noticed, stress determined a capacitance decrease, mostly localized in the positive bias region. The time dependence of the capacitance decrease and of the optical power decay were found to be similar (see the inset of Figure 4.17), thus indicating a correlation between the electrical and optical degradation of the devices. These results suggest that information on the mechanism

responsible for the degradation can be extracted by means of a detailed analysis of the capacitive properties of the samples: therefore we have carried out a complete study of the properties of the deep levels in the semiconductor layer by means of DLTS and TAS, with the aim of identifying the changes arising as a consequence of stress.

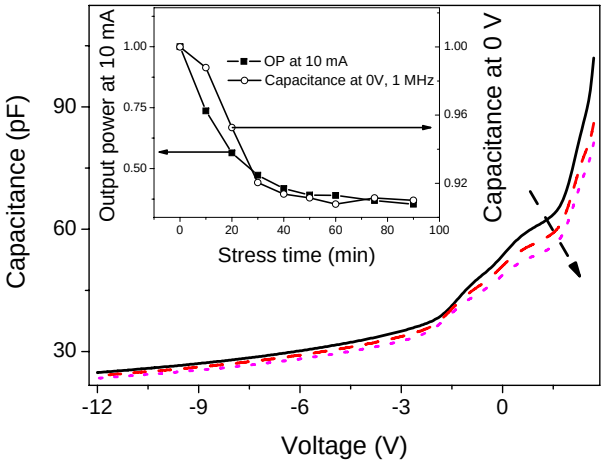



**Figure 4.17:** capacitance-voltage curves measured during stress at 250 °C at 1 MHz. Solid line = before stress, Dashed line = After 20 min at 250 °C, Dotted line = After 90 min at 250 °C. Inset: optical power (at 10 mA) and capacitance (at 0 V, 1 MHz) decrease measured during stress on one aged device

### 4.5.1 DLTS analysis

DLTS measurements (Figure 4.18) refer to the temperature interval $100 - 400\ K$, except for the measurement performed after the last stress stage, for which the temperature interval was $100 - 500\ K$; the spectra were collected with values of reverse bias $V_b$ and filling pulse $V_{fill}$ such to probe the bulk region of the n-side of the junction excluding the quantum well active region. However, very similar spectra with a similar degradation behavior were found also in regions closer to the multi-quantum well system. During the DLTS run, the capacitance level $C(V_b)$ was simultaneously measured at a meter frequency $f_{cap} = 1\ MHz$ over the whole temperature interval. We refer to this measurement as to the characteristics of capacitance versus temperature $C(T)$, omitting the dependence on the bias level $V_b$.

DLTS analysis of the samples subjected to thermal stress evidences (Figure 4.18)

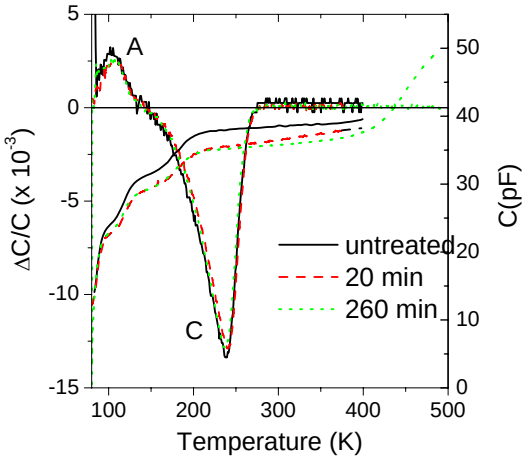



**Figure 4.18:** DLT-spectra and $C(T)$ characteristics measured at increasing stress stages. DLT-spectra refer to the emission rate $e_n = 46.5s^{-1}$, and are collected at a reverse bias level $V_b = -3\ V$ and at a filling pulse level $Vfill = -2\ V$.

the presence of two deep levels, here labeled as $A$ ($E_t = 0.15\ eV$) and $C$ ($E_t = 0.25\ eV$). The signatures of these levels are reported with squares in the Arrhenius plot in Figure 4.19. Both levels found are majority carrier levels, despite the positive sign of the peak related to $A$; this is due to the fact that at the detection temperature $< 100\ K$ the DL transient can be inverted due to the significant increase in the series resistance caused by the poor ionization of Mg dopants [20]. For this reason, it was not possible to estimate the concentration of $A$, while the concentration of deep level $C$ was found to be $N_t = 9 \cdot 10^{16} cm^{-3}$. The shape and the amplitude of the signal $\Delta C/C$ from these levels is constant at different stress times, showing that they do not change their concentration with stress. Thus, no introduction of new deep levels or modification of pre-existing deep levels takes place, at least in the considered temperature range. The DLTS analysis was performed up to 500 $K$ in the sample after the last stress stage, yielding an upper bound of 0.8 $eV$ for the possibility of a deep level with a typical cross section of about $10^{-15} cm^2$ to be detected. Therefore, no modification to the deep levels with energy between 0.15 $eV$ and 0.8 $eV$ occurs.

The characteristics of the capacitance as a function of temperature $C(T)$ evidence a gradual decrease of $C$ with increasing stress time. This observation, keeping into account the capacitance meter frequency $f_{cap} = 1\ MHz$, is consistent with the results

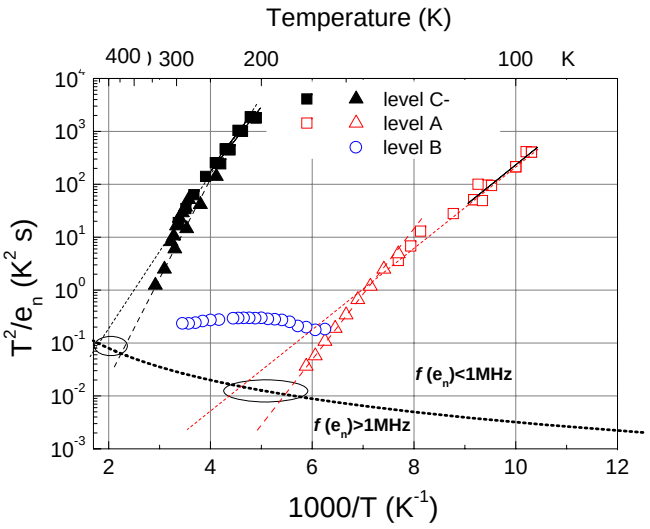



**Figure 4.19:** The Arrhenius plot of one analyzed sample, in which the signatures of levels $A$ (empty squares and triangles) and $C$ (full squares and triangles) are reported, measured by both DLTS (squares) and admittance spectroscopy (triangles). The signature of level $B$ is reported as measured by admittance spectroscopy (empty circles). The dotted curve on the plot identifies the region for which the emission rate of the deep levels is in resonance with a capacitance frequency equal to 1 $MHz$. The dashed lines are an extrapolation of the deep level signatures.

of the C-V characterization shown in Figure 4.17. As represented in Figure 4.18, the decrease of the capacitance is distributed on a wide temperature interval, and therefore it is not correlated with the introduction of new deep levels.

### 4.5.2 Thermal Admittance Spectroscopy

As described above, DLTS measurements do not give detail on the phenomenon responsible for the modification of the C-V curves indicated in Figure 4.17, since they do not indicate modification in the capacitance transient arising as a consequence of stress. We have therefore analyzed the capacitive properties of the devices using also TAS measurements. This technique consists in a set of capacitance-frequency (C-f) and conductance/frequency vs frequency (G/f vs f) measurements carried out at different temperature levels [118]. The presence of a deep level (DL) in the analyzed semiconductor determines a flex in the C-f curves, and a peak of the G/f curves, at a frequency level which is related to the emission rate of the deep level itself. Device heating (cooling) determines the increase (decrease) of DL emission rate, and therefore the shift of the C-f and G/f curves towards higher (lower) frequencies. Therefore, by means of repeated G/f measurements at different temperature levels, it is possible to evaluate the dependence of the emission rate on temperature, and therefore to extrapolate the characteristics (activation energy and capture section) of the analyzed levels. Due to the intrinsic differences of DLTS and TAS, by means of the two techniques it is possible to probe different regions of the emission rate/temperature space, obtaining a more complete Arrhenius plot describing the modification of DLs properties during stress.

Before stress, TAS revealed the presence of the two levels A and C already detected by means of DLTS (peaks shown in Figure 4.18). The signature of these levels are reported in the Arrhenius plot in Figure 4.19 by means of triangles, and are well superimposed to the squares representing the results obtained with DLTS. It is apparent that both experimental techniques, operating in two different frequency/emission rate regimes, yield matching signatures for both levels.

The Arrhenius Plot also reports the curve (dotted line on the lower part) identifying the points at which, for each $T$, the emission rate is in resonance with a capacitance

meter frequency equal to 1 MHz. The diagonal dashed lines represent the extrapolation of the deep levels signature to higher emission rate/temperature levels, which could be measured neither by DLTS nor by admittance spectroscopy. The point where the extrapolation of the deep level signatures intersects this curve yields an estimate of the temperature interval at which a step in the C(T) characteristics is expected. In the present case, deep level $A$ yields a step in the $C(T)$ curve at $T \approx 200\ K$, while deep level $C$ at $T \approx 450\ K$; both steps are clearly visible in the plot of Figure 4.18. Moreover, there was no deep level detected which could explain the variation in the C(T) characteristics, which occur on the whole temperature interval considered in the measurement.

While on one hand DLTS spectra did not indicate significant changes as a consequence of stress, on the other hand thermal treatment was found to induce modification of the G/f behavior of the devices, and therefore changes of their TAS spectrum (see Figure 4.20). The most significant changes were detected in the temperature range between 240 and 290 $K$. Before treatment, the G/f curves of the LEDs showed only one peak in this region, corresponding to level $C$ in Figure 4.18 and Figure 4.19, with activation energy equal to 0.33 $eV$. This activation energy is slightly higher than the value 0.25 $eV$ found by fitting the Arrhenius signature of the DLTS peak, and this is most likely due to a dependence of the capture cross section on temperature. After stress, a new peak was detected, centered around 100 $kHz$ (peak $B$ in Figure 4.20): comparison between G/f and capacitance-voltage characterization carried out at each stress step showed that the growth of the G/f peak took place together with the gradual decrease of the junction capacitance described in Figure 4.17, well related to the degradation of the optical properties of the devices.

The thermal analysis of peak $B$ showed that a variation of device temperature did not correspond to a significant movement of the frequency position of the peak itself (see Figure 4.20), indicating that peak $B$ can be related *(i)* to the generation of a very shallow level or *(ii)* to a non-thermally activated process that can modify the small signal capacitance/conductance of the devices.

In order to understand which is the origin of peak $B$ we have plotted its signature in the Arrhenius plot in Figure 4.19. As a result, we have found that the $T^2/e_n$ ratio for this level is substantially independent on temperature, as suggested by the small shift

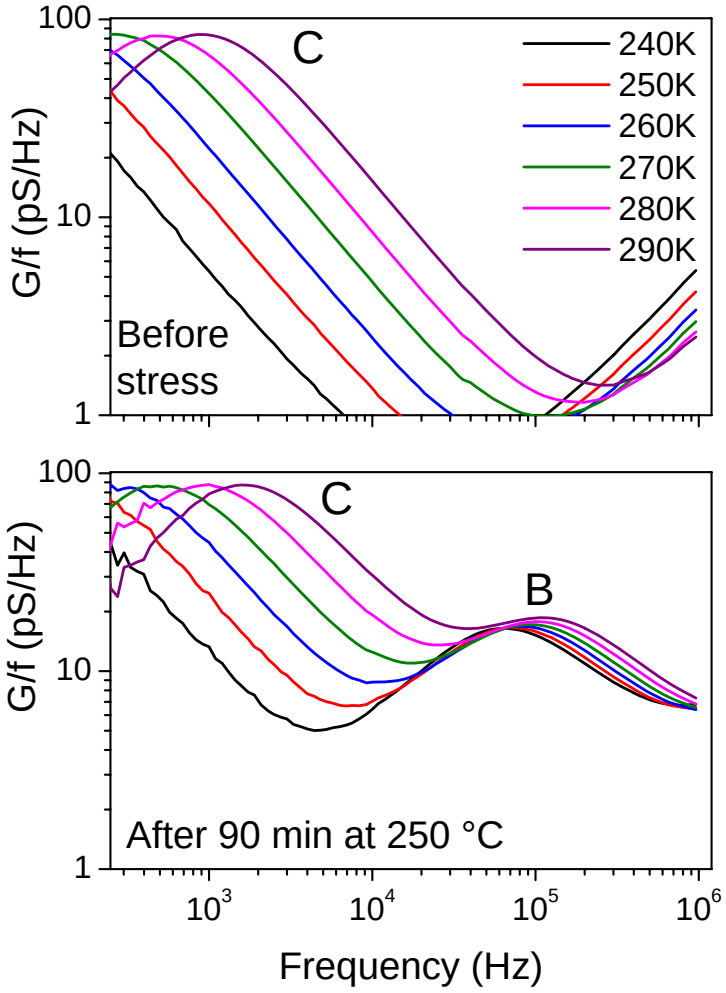



**Figure 4.20:** G/f curves measured in the temperature range $240 - 290\ K$ before and after stress at $-0.6\ V$

of the G/f curves with increasing temperature. Therefore the new peak detected after stress in the G/f characteristics of the devices cannot be ascribed to the generation of a defect state in the semiconductor material, but is related to a degradation process that has a nearly temperature-independent impact on the characteristics of the device.

As described in the previous sections, the degradation of the electrical properties of the devices is related to the interaction between hydrogen and the magnesium dopant, implying the generation of Mg-H bonds and the subsequent decrease of active acceptor concentration ([14]). Therefore devices degradation can be ascribed to the worsening of the properties of the metal-(p-GaN) contact. Analysis described in this section indicate that this process implies the modification of the capacitive characteristics of the devices. In particular:

- C-V analysis indicates that stress induces a decrease of junction capacitance, related to the optical power degradation (see inset of Figure 4.17)
- DLTS and TAS measurements indicate that these modifications are not related to the generation of defect states in the p-GaN region probed by means of these techniques, i.e. close to the active layer
- TAS analysis indicates the presence of a non-thermally activated mechanism, related to the capacitance decrease detected after stress.

Since this last mechanism is not related to the generation/modification of DLs close to the junction, it can be related to the degradation of the p-GaN layer at the surface of the devices, close to the passivation layer.

This hypothesis can be verified by analyzing the degradation of ohmic contacts on p-GaN during high temperature storage. A detailed analysis of this process is described in Chapter 5. We briefly anticipate a few results obtained in the framework of that analysis, because they can be used to explain the modifications we have detected on the capacitive measurements.

As described in Chapter 5, in order to obtain a better undestanding of the degradation of the p-GaN layer and contacts and semiconductor detected on the LEDs, we have analyzed the behavior of ohmic contacts on p-GaN during thermal stress. Analysis has been carried out by means of the Transmission Line Method (TLM)

[119]. Circular-TLM structures were submitted to thermal storage at 250 $°C$, and a complete current-voltage characterization of the pads has been carried out at each step of the thermal treatment.

Before stress, the I-V characterization revealed linear behavior of the contacts (Figure 4.21). Sheet resistance and contact resistivity were estimated to be equal to 79 $k\Omega/square$ and 6.7 $m\Omega \cdot cm^2$ respectively by means of the technique described in [119] . Stress was found to induce

- the non-linearity of the characteristics of the contacts, corresponding to a variation of the slope of the I-V curves around zero
- a slight increase of sheet and contact parasitic resistivity, corresponding to a slight variation of the slope of the I-V curves of the TLMs in the high current region (Figure 4.21)

The fact that after stress there is a strong degradation of the linearity of the contacts without significant changes in contacts and semiconductor parasitic resistance, indicates that the generation of $Mg - H$ bonds and the subsequent acceptor dopant compensation takes place mostly at the surface of the devices, close to the metal/semiconductor contact, rather than in the region near the junction. Since degradation mostly interests device surface, stress did not induce changes of DLs distribution in the space charge region, and this explains the fact that no significant variation of the DLTS spectra has been detected as a consequence of stress (Figure 4.18).

### 4.5.3 Interpretation of the results

As described above, as a consequence of thermal storage the properties of the p-side ohmic contacts of the LEDs are degraded, due to the interaction between devices surface and the passivation layer with subsequent rectifying behaviour of the contact. The p-GaN layer is covered by a semitransparent metallization. At the center of the top-side of the LED, there is a further thick metal pad, used for the bonding of the devices, that occupies the 20 % of the overall LED area (see the schematic of the top side of the devices in Figure 4.3(a)). The passivation layer is deposited on the

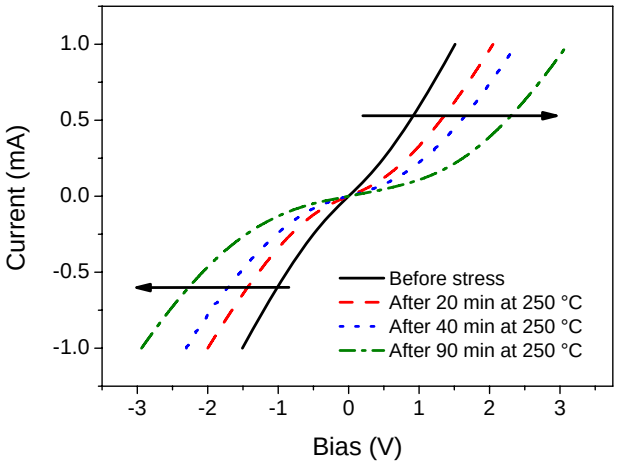



**Figure 4.21:** I-V curves measured on TLM structures before and after stress at 250 $°C$

semitransparent metal layer, while it is not present on the central pad due to the need of obtaining a good wire bonding (see Figure 4.15). Therefore, interaction between passivation layer and the metal/semiconductor junction takes place only in the area surrounding the central contact, i.e. on the 80 % of the surface of the LEDs. The remaining area is thought to be not affected by thermal treatment described in this work: as a proof it must be considered that after stress the region under the central pad keeps its efficiency unchanged, while the remaining area is affected by a strong efficiency loss (see Figure 4.8(b)) [14].

As suggested by Figure 4.21 and explained in detail in Chapter 5, after stress a rectifying barrier is generated at the metal/semiconductor interface of the devices: therefore, the impedance model of devices structure is changed, because a new parasitic impedance is placed in series with the intrinsic impedance ($C_P - R_P$) in the device portion outside the contact pad. The small-signal equivalent circuit describing these changes is reported in Figure 4.22. $C_1$ and $G_1$ are the capacitance and conductance associated with the portion of the p-n junction under the contact pad (20 % of devices area), while $C_2$ and $G_2$ refer to the portion of the p-n junction outside the pad (80 % of devices area).

These quantities are related by

$$C_1 + C_2 = C_p \tag{4.4}$$

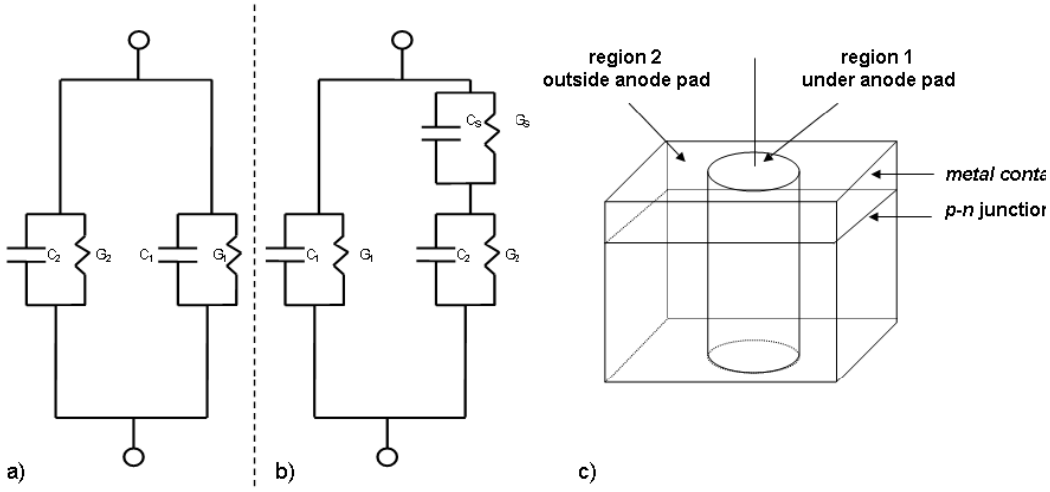



**Figure 4.22:** Small-signal equivalent circuit for the analyzed device: (a) before stress treatment; (b) after stress treatment. Part (c) is a 3D sketch of the device evidencing that subscripts 1 and 2 refer to the portion of the junction under the pad and outside the pad, respectively, while subscript s refers to the device (p-GaN)-metal interface outside the pad.

$$G_1 + G_2 = G_p \tag{4.5}$$

$$C_1 = kC_P,\ C_2 = (1-k)C_p \tag{4.6}$$

$$G_1 = kG_P,\ G_2 = (1-k)G_p \tag{4.7}$$

$k = 0.2$ being the geometric ratio between the area of the pad and the total device area. $C_p$ and $G_p$ are the quantities measured before stress, when we suppose that the block $C_s - G_s$, representing the parasitic impedance, is negligible in the calculation of the total admittance. This is equivalent with supposing a sufficiently high value for $G_s$ before stress, consistently with the hypothesis that charge transport at the metal-(p-GaN) interface occurs by tunnelling. The quantities $C_s$ and $G_s$ play a role only after stress, assuming the values $C_s = 220 \pm 20\ pF$ and $G_s = (3.4 \pm 0.3)\ 10^{-4}\ S$. These values are found by a fitting procedure and are assumed as independent of temperature and frequency, consistently with the experimental results of TAS and C(T) characterization. The admittance of the portion of the device outside the pad is thus

$$Y_M = \frac{AC + \omega^2 BD + j\omega(BC - AD)}{C^2 + \omega^2 D^2} \tag{4.8}$$

with

$$A = G_2 G_s - \omega^2 C_2 C_s \tag{4.9}$$

$$B = C_2 G_s - G_2 C_s \tag{4.10}$$

$$C = G_2 + G_s \tag{4.11}$$

$$D = C_2 + C_s \tag{4.12}$$

which yields the total device admittance as

$$Y_{tot} = Y_M + G_1 + j\omega C_1 \tag{4.13}$$

$\omega = 2\pi f$ being the measurement frequency. The results of the fitting procedure are visible in Figure 4.23. In the graphs, the experimental data showing the dependence of $C$ and $G/f$ on frequency are reported for a device before and after stress, moderately reverse-biased at $V_b = -0.6\ V$. This example shows the validity of the assumed model for the explanation of the modifications occurring upon stress. In particular, it visualizes how the C vs. f and G/f vs. f characteristics before stress go over to those after stress provided $C_s$ and $G_s$ assume the values given by the best fit.

The physical explanation for the occurrence of these changes is the following. Hydrogen impurities diffuse to the semiconductor from the passivation layer deposited on the metal contact outside the pad. The diffusion of $H$ may have two main consequences: *(i)* the reaction between H and Mg impurities in the p-GaN layer passivating the Mg dopants, *(ii)* an increase in concentration of H at the metal-semiconductor interface modifying the barrier height [129]. The strong changes detected by C-f and G/f-f characterization can be attributed to an increase in the resistive component of the admittance $Y_s$ rather than to modifications of the capacitive component. In fact, the value $C_s = 220 \pm 20\ pF$ of the capacitance associated to the Schottky metal-(p-GaN) contact after stress corresponds to an effective ionized acceptor density $N_a = 5 - 6 \cdot 10^{18} cm^{-3}$, which is about the 10 % of the overall acceptor concentration. This fact indicates that after stress the active acceptor concentration can be significantly passivated only in the immediate proximity of the metal-(p-GaN) interface, i.e. at a distance scale smaller than the width of the depletion region at the Schottky contact (calculated from the capacitance $C_s$ as $x_p = 18 \pm 1\ nm$). The

measurements performed on TLM structures confirm this hypothesis, showing that thermal treatment implies a strong increase in the contact resistivity and a minor increase in the bulk resistance.

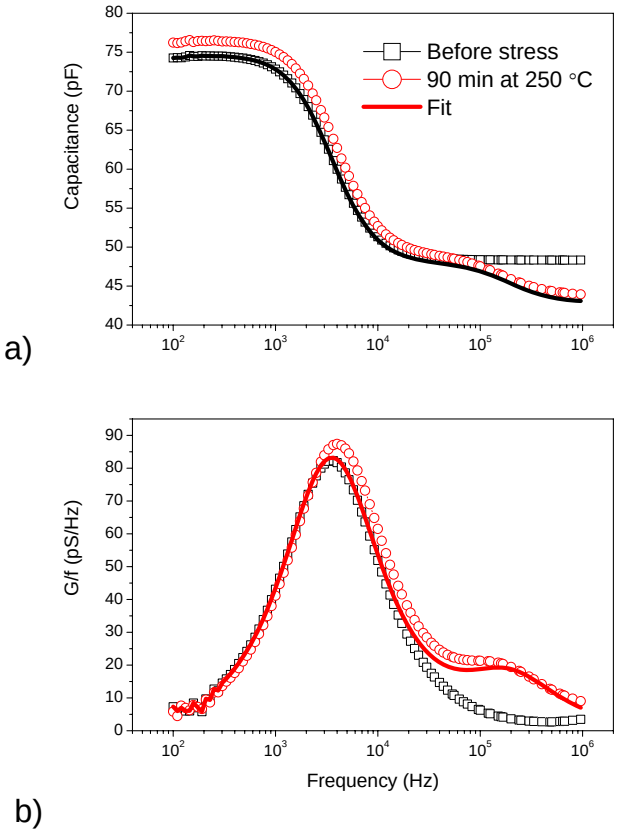



**Figure 4.23:** Evolution of capacitance (a) and conductance over frequency (b) with stress. Squares are the measured C and G/f before stress, while circles refer to the same quantities measured after 90 *min* stress at $T = 250°C$. The line is a fit which takes into account the small-signal equivalent circuit of Figure 4.22 with $C_p = C_1 + C_2$ and $G_p = G_1 + G_2$ keeping the same values measured before the stress, $C_s = 220\ pF$ and $G_s = 3.4 \cdot 10^{-4} S$. The device is biased at $V_b = -0.6\ V$.

### 4.5.4 Capacitive analysis: summary

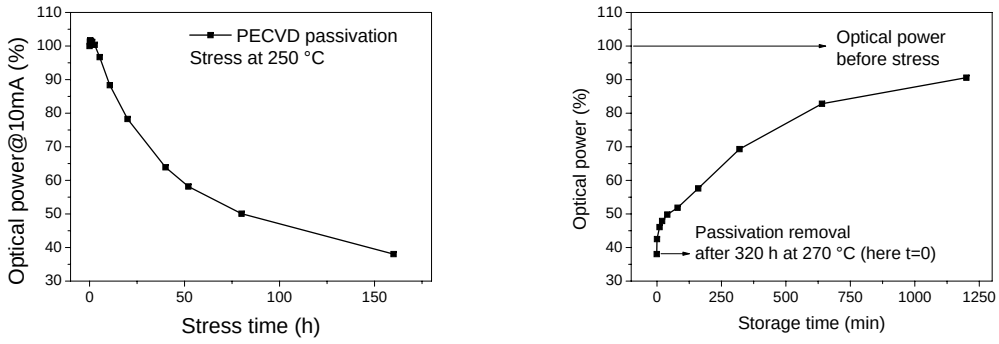
In summary, we have analyzed the degradation behavior of nitride-based multi-quantum well LEDs with hydrogen-rich passivation layer subjected to thermal stress by means of capacitive and spectroscopic techniques. Stress was found to induce a decrease in the measured capacitance of the device, which was found to be well related to the optical power decrease. By means of DLTS and TAS spectroscopies we excluded that this capacitance decrease is related to the introduction of deep levels compensating the doping density in the junction region. We also found that stress induces the growth of a peak in the G/f curves, which corresponds to a non thermally activated mechanism. TLM measurements on specific structures on p-GaN showed that the I-V characteristics assume a progressively non-ohmic behavior, with an increase of the contact resistance. We interpreted these observations as due to the diffusion of H from the passivation layer to the metal -(p-GaN) contact, with the subsequent passivation of p-type Mg doping in the immediate proximity of the interface. This modifies the contact resistivity by partially suppressing tunneling through the Schottky contact. A small signal model taking into account the increase in the resistance of the contact layer outside the pad could well reproduce the modifications occurring in the TAS spectra upon stress, and allowed us for the calculation of the effective concentration of $Mg$ activated impurities after stress, which was found to be $N_a = 5 - 6 \cdot 10^{18} cm^{-3}$, the same that would be expected before stress.

## 4.6 Recovery tests

The degradation of both the electrical and optical properties of the devices detected as a consequence of high temperature stress was found to be reversible. After the end of the ageing tests described above, the PECVD passivation layer has been removed from the LEDs (using an $NH_4F - HF$ solution), and the behavior of the devices during subsequent annealing at 250 $°C$ has been analyzed.

Results described in this section refer to samples with PECVD passivation with lower hydrogen content with respect to the ones analyzed in the previous sections: these devices showed the same degradation processes described in the previous sections, but

slower stress and recovery kinetics (this can be understood comparing Figure 4.4 to Figure 4.24(a)). For this reason, we have chosen to analyze recovery process on samples with slower kinetics, in order to achieve a better description of the phenomenon.[1]




(a) (b)

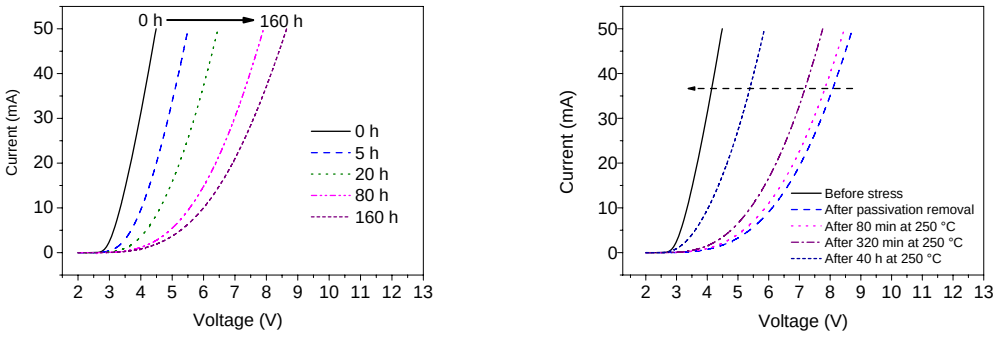
**Figure 4.24:** (a) Optical power decay measured (at 10 mA) on one LED with PECVD passivation during storage at 270 °C; (b) optical power recovery observed on an aged LED after passivation removal and subsequent thermal treatment at 250 °C. The values in this diagram are normalized to the ones of the untreated device.

During the thermal treatment following passivation removal, the optical characteristics of the LEDs showed an almost complete recovery (Figure 4.24(b)): the recovery process was found to be faster than the degradation process (degradation kinetic for this LED is shown in Figure 4.24(a)).

The electrical measurements showed also the recovery of the electrical properties of the LEDs. This is described by Figure 4.25(a) and 4.25(b), that show the I-V curves measured during the recovery experiment. The fact that the degradation process is reversible after passivation removal can be related to the fact that

- the hydrogen source (passivation layer) has been removed
- after passivation removal the hydrogen entrapped at LEDs surface can escape from the devices

[1]Note that the OP degradation kinetics shown in Figure 4.4 are almost finished after 90 minutes of treatment. For these LEDs, almost complete recovery is obtained after a 10 minutes annealing at 250 °C (after passivation removal). This time interval is too short to obtain a description of recovery kinetics.




(a) (b)

**Figure 4.25:** (a) Current-Voltage curves measured before and during stress at 270 °C on the LEDs with PECVD passivation layer; (b) Current-Voltage curves measured during recovery test on one aged LED at 250 °C. The I-V curve measured before stress is plotted for comparison

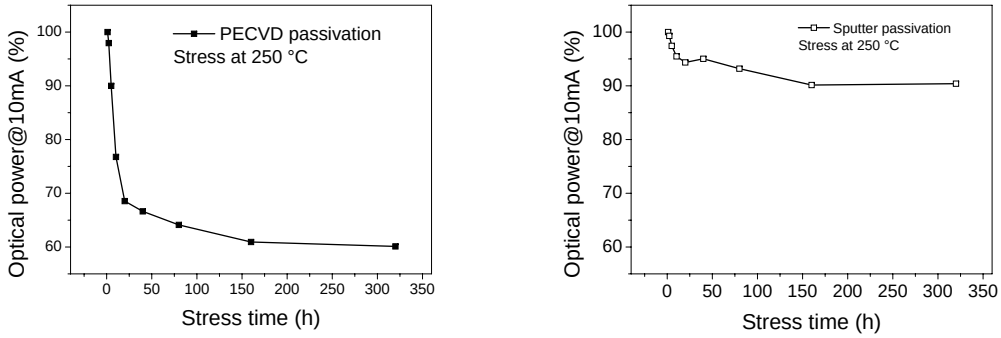
## 4.7 Proposal of a stable passivation layer

The data described above confirm that the PECVD passivation layer can play a role in limiting devices stability at high temperature levels, possibly due to the interaction between hydrogen and LEDs surface at the p-side [71, 74, 75, 8]: the comparison between the behavior of devices with and without passivation [130, 14] strengthens this result.

Therefore, the use of an hydrogen free passivation layer is expected to improve devices stability at high temperatures. In order to confirm this hypothesis and to indicate a stable passivation layer for LEDs, we have compared the behavior of a set of LEDs with PECVD and sputtered SiN passivation layer during thermal storage. All the LEDs analyzed within this comparison had identical epitaxial structure: the differences of their behavior during stress are then ascribable to the different layers used for the passivation of the devices.

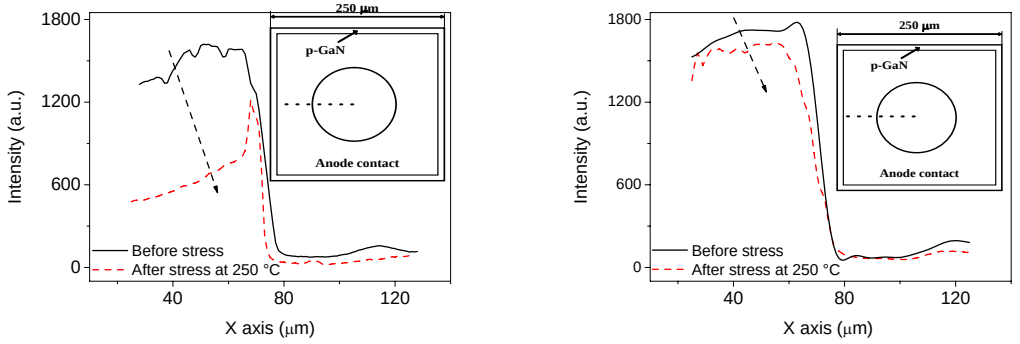
As summarized by the optical power degradation curves in Figure 4.26(a) and 4.26(b) and by the emission profiles in Figure 4.27(a) and 4.27(b), thermal storage induced only a slight degradation on the devices with sputtered passivation, with respect to what detected on the samples with PECVD passivation. Furthermore, the I-V curves (Figure 4.28(a) and 4.28(b)) of these samples did not show the significant

shift towards higher voltages detected on the corresponding LEDs with PECVD passivation, and only a slight increase of the series resistance and of the ideality factor was observed after stress (Figure 4.29(a) and 4.29(b)): this demonstrates that the use of sputtered passivation guarantees the preservation of the electrical properties of the devices even after several hundreds hours of thermal storage, and that suputtered passivation can be an efficient alternative to PECVD passivation for the realization of highly reliable LEDs.



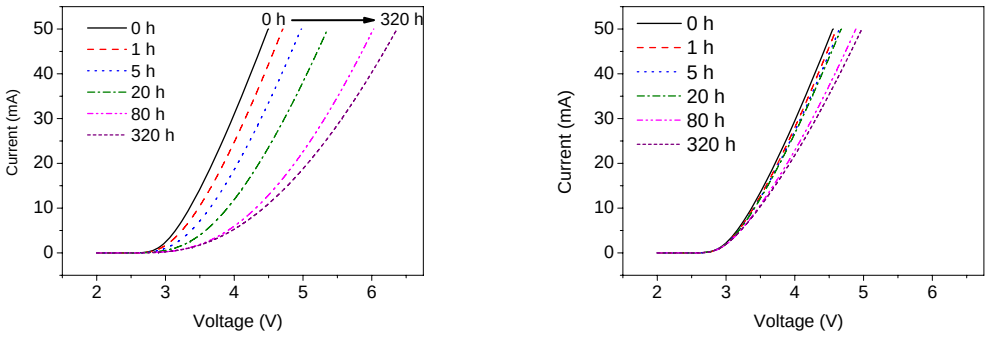

(a) (b)

**Figure 4.26:** Optical power decrease measured (at 10 mA) during stress at 250 °C on the LEDs with (a) PECVD passivation layer and (b) sputter passivation.



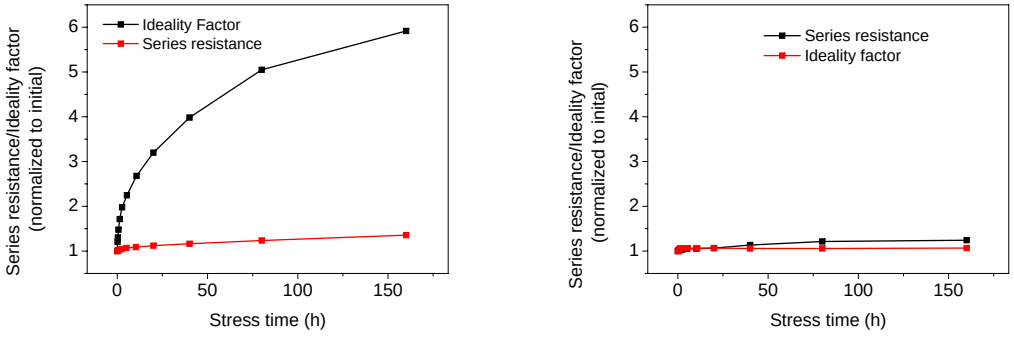

(a) (b)

**Figure 4.27:** Linear emission profiles measured (at 10 mA) during stress at 250 °C on the LEDs with (a) PECVD passivation layer and (b) sputter passivation. Inset: schematic top view of the LEDs, showing the line on which the linear intensity profiles have been measured




(a) (b)

**Figure 4.28:** Current-Voltage curves measured during stress at 250 °C on the LEDs with (a) PECVD passivation layer and (b) sputter passivation.




(a) (b)

**Figure 4.29:** Series resistance and ideality factor increase measured during stress at 250 °C on the LEDs with (a) PECVD passivation layer and (b) sputter passivation.

## 4.8 Summary

In this chapter we have described an analysis of the high temperature reliability of GaN LEDs with SiN passivation layer. Ageing tests carried out on LEDs have shown that PECVD passivation can play an important role in limiting devices stability at high temperature levels. Degradation of the electrical and optical characteristics of the devices has been attributed to the worsening of the properties of the electrical contact at the p-side of the diodes, due to the interaction between the hydrogen in the passivation layer and LEDs surface and the subsequent lowering of active acceptor concentration. Stress was found to induce also modifications of the LEDs capacitance: by means of a DLTS and TAS analysis, we could exclude that these modifications are related to the generation of new trap states inside the junction. A small-signal model taking into account the increase of the resistivity of the metal/semiconductor contact has been developed to explain the modifications detected in the capacitance measurements. The model was found to have good agreement with experimental data.

The degradation process was found to be reversible, after passivation removal and subsequent annealing. This is due to the fact that after passivation removal *(i)* the hydrogen source has been removed from the LEDs and *(ii)* hydrogen entrapped at LEDs surface can escape from the devices. A proof of the role of hydrogen in the degradation process has been given by storage tests carried out in different atmospheres: in particular, annealing in forming gas was found to induce the same degradation of the electrical and optical parameters detected during stress of samples with PECVD passivation.

Finally, relevant data indicating that a sputtered SiN passivation layer can be an effective alternative to PECVD passivation in terms of devices high-temperature reliability have been presented. Measurements results indicate that sputter passivation deposition can preserve both the optical and electrical performance of the devices over several hundreds of hours of high temperature storage.

# Chapter 5

# Analysis of contacts degradation

This chapter analyzes the high temperature long-term stability of ohmic contacts on p-type gallium nitride to be used for GaN-based LEDs. The contributions of the ohmic contacts and semiconductor material degradation are separated by means of suitable test structures adopting the Transmission Line Method (TLM). Before stress, the current vs voltage curves measured at the pads of the TLMs showed linear shape, indicating good ohmic behaviour of the contacts. Thermal treatment at 250 °C was found to induce the worsening of the electrical characteristics of the contacts: identified degradation modes consist in a shift of the I-V curves towards higher voltages, and strong non-linearity of the characteristics around zero.

This chapter shows that the high temperature instabilities of ohmic contacts on p-GaN are related to the interaction between device surface and the PECVD SiN passivation layer, usually used for chip encapsulation and for reducing the device leakage current. Hydrogen contained in the passivation layer is supposed to play an important role in the degradation process: the interaction with the acceptor dopant at the metal/semiconductor interface induces a decrease in the effective acceptor concentration. As a consequence, both the ohmic contact characteristics and the semiconductor sheet resistance are worsened. The I-V characteristics of the degraded TLM structures deviate from the ideal behaviour and become non-linear. The role of hydrogen is confirmed by several evidences: *(a)* stress of TLMs without passivation carried out in forming gas atmosphere induces the same degradation process detected on passivated samples aged at high temperatures; *(b)* degradation process was found

to be reversible, after passivation removal and subsequent annealing; *(c)* finally, the use of sputtered SiN passivation layers (with low hydrogen content) can guarantee the stability of the properties of the ohmic contacts during several tens of hours of stress at 250 °C, thus providing a suitable technique for the deposition of passivation layers, alternative to the usually adopted PECVD and stable at high temperature levels.

## 5.1 Motivation

In the previous chapter we have demonstrated that a source of the hydrogen limiting devices stability at high temperature levels is represented by the passivation layer, usually deposited by PECVD on the LEDs for chip encapsulation and surface leakage current reduction [130, 14]. Failure modes induced by the high temperature interaction between LEDs surface and passivation layer include optical power decrease, emission crowing and operating voltage increase. This process has been attributed to the degradation of the p-type region of the diodes, due to hydrogen-induced compensation of the acceptor dopant.

The analysis quoted above have been carried out on completed LEDs: those experiments have allowed us to identify the strong correlation between electrical and optical degradation of the devices during thermal treatment, but did not provide a quantitative understanding of the impact of thermal stress on the physics of degradation of electrical characteristics of the ohmic contacts and p-type semiconductor. A more detailed analysis requires the use of specific test structures for the study of contacts, such as those based on the Transmission Line Method (TLM), which can provide accurate information on the characteristics of ohmic contacts and semiconductor layers before and during stress.

Therefore, the aim of this chapter is to describe a detailed analysis of the degradation of p-type GaN contacts consequent to high temperature storage. TLM structures have been submitted to high temperature storage tests, and their electrical characteristics have been monitored during stress time in order to achieve a complete description of contacts degradation.

We demonstrate that:

- the worsening of the ohmic properties of the metal/semiconductor interface at the

p-side of the diodes (resulting in non-linear characteristics of the contacts and in a slight increase of the semiconductor sheet resistance) significantly contributes to the electrical degradation already noticed in LEDs

- degradation is reversible after passivation removal and subsequent annealing
- sputtered passivation can be used as an alternative to the conventionally adopted PECVD passivation, resulting in an improvement of the high temperature stability of ohmic contacts on p-type GaN, due to its low hydrogen content

## 5.2 Analyzed devices and stress conditions

The analysis has been carried out by means of the Transmission Line (TLM) method [131, 67, 119]. Test structures were grown on SiC substrates by MOVPE. For contact metalization, a platinum layer was deposited by vacuum evaporation (see [67] for details). Circular TLM-patterns were then defined by means of back sputtering (see Figure 5.1 and 5.2 for a schematic and micrograph of the used patterns).

The following dimensions were chosen for the TLM-patterns: inner radius equal to 50 and 100 $\mu m$; spacing equal to 2, 4, 8, 16, 32 and 64 $\mu m$. The TLMs were covered with an hydrogen rich PECVD passivation layer: characteristics of p-type layer, ohmic contacts and passivation layers were the same of previous studies on LEDs degradation (see Chapter 4), in order to achieve consistent comparison between LED and TLM degradation data.

After an initial characterization of TLM patterns, the structures were submitted to thermal storage at 250 $°C$, for 160 hours. Characterization of TLM structures was carried out by means of 4-wires current-voltage measurements, in order to reduce parasitic effects. An HP4155A Semiconductor Parameter Analyzer was used for the measurements. Data were analyzed by means of the method described in [119]. During stress, behaviour of TLMs was compared to the electrical degradation of LEDs with the same p-side and ohmic contact structure: this comparison allowed us to state that the high temperature degradation of the ohmic contacts detected in the TLMs (i.e. the degradation of the ohmic properties of the metal/semiconductor junction at the p-GaN surface) is the main responsible for the degradation of the electrical properties of LEDs

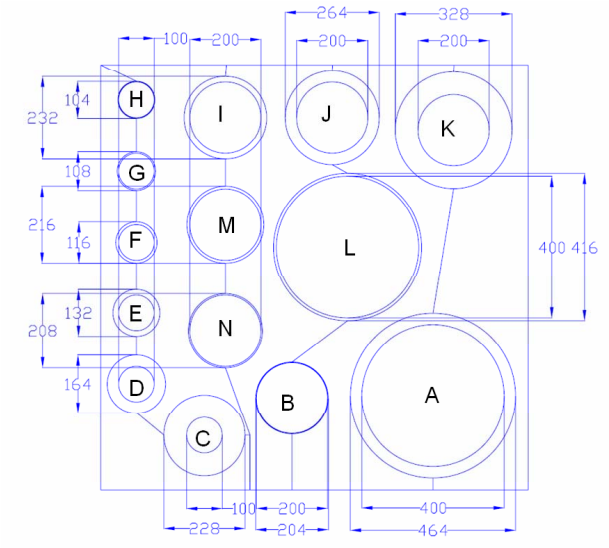



**Figure 5.1:** schematic of one of the analyzed TLMs

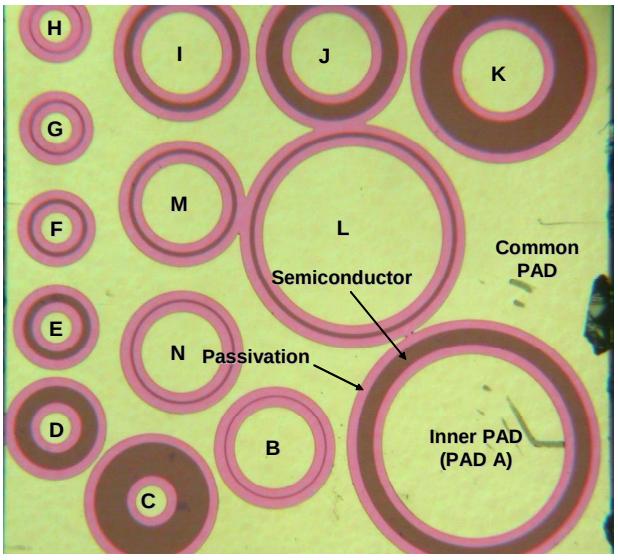



**Figure 5.2:** micrograph of one of the analyzed TLMs

under high temperature stress reported in Chapter 4 and in [11, 9, 14]. After stress tests, passivation layer was removed from the TLMs, using an $NH_4F - HF$ solution, and the devices were submitted to further thermal treatment at 250 $°C$. During this second annealing phase, the devices were characterized by means of I-V measurements in order to detect possible recovery of their electrical and optical characteristics.

## 5.3 Results of the I-V measurements

Figure 5.3 shows the I-V curves measured before stress between each of the pads of one TLM (see Figure 5.2) and the common pad. As can be noticed, all the pads showed linear behaviour: the resistance values extrapolated from these measurements are listed in Table 5.1.

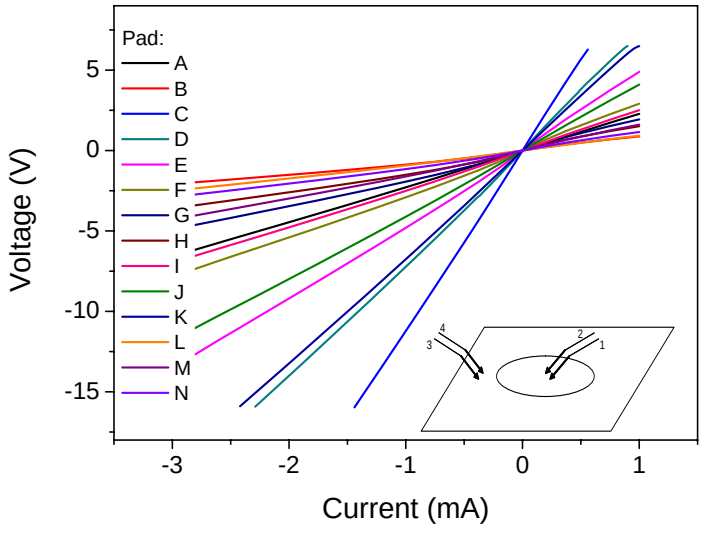



**Figure 5.3:** I-V curves measured between each of the pads and the common pad (PECVD H-rich passivation). Inset: schematic of the 4-terminals configuration: terminal 1 and 3 were used for the current source, while terminals 2 and 4 were used for voltage measurements.

As described in [119], the total resistance between the internal and the external contacts can be approximated by:

$$R_T = \frac{R_S}{2\pi}\left[L_T\left(\frac{1}{r_i}+\frac{1}{r_o}\right)+ln\left(\frac{r_o}{r_i}\right)\right] \tag{5.1}$$

| Pad | Resistance (Ω) | Error (Ω) |
|---|---|---|
| A | 2301 | 0.94 |
| B | 930 | 3.40 |
| C | 10947 | 51.37 |
| D | 7324 | 14.87 |
| E | 4959 | 8.00 |
| F | 3019 | 7.86 |
| G | 2043 | 7.65 |
| H | 1623 | 8.12 |
| I | 2556 | 3.07 |
| J | 4154 | 2.93 |
| K | 6768 | 5.24 |
| L | 945 | 1.07 |
| M | 1665 | 3.34 |
| N | 1209 | 3.61 |

**Table 5.1:** resistance measured between each pad and the common pad on one untreated TLM

where $r_i$ and $r_o$ are respectively the inner and outer radius of each pad, while $L_T$ represents the "$1/e$" distance of the curve expressing the voltage drop under the contact. This last parameter can be thought of as the averaged portion of the contact width which is really crossed by current, and is related to the sheet resistance ($R_S$) and to the contact resistivity ($\rho_c$) by the relation

$$L_T = \sqrt{\rho_c / R_s} \tag{5.2}$$

For $r_i \gg r_0 - r_i$ Equation 5.1 simplifies to:

$$R_T = \frac{R_S}{2\pi r_i} \left(r_o - r_i + 2L_T\right) C \tag{5.3}$$

Where C is the correction factor

$$C = \frac{r_i}{r_o - r_i} ln \left(\frac{r_o}{r_i}\right) \tag{5.4}$$

Figure 5.4 shows the variation of the total resistance with the gap ($r_o - r_i$) between the inner and the outer contact, as measured on the pads with $r_i = 50\ \mu m$ for all the pads of one of the TLMs. The values of $R_S$, $L_T$ and $\rho_c$ an be obtained fitting this curve by means of Equation 5.3. Average values measured for the analyzed devices were $R_S = 52913 \pm 387\ \Omega/square$, $L_T = 2.3 \pm 0.8 \mu m$, $\rho_c = 2.7 \pm 0.2\ m\Omega \cdot cm^2$.

Figure 5.5 shows the I-V curves measured before and during stress on one of the aged TLMs with hydrogen rich passivation in the range $-3 \rightarrow 1\ mA$ (measurements carried out on pad H in Fig. 1). Before stress the measured I-V curves were roughly linear, indicating a good electrical behaviour of the ohmic contacts on p-type GaN. On the other hand, thermal treatments induced a voltage increase and the non-linearity of the electrical characteristics around zero.

The behaviour of the resistance values determined by the slopes of the I -V curves in Figure 5.5 depends on the applied current: for currents greater than 1 mA extracted resistance values show only a slight increase during treatment (reaching the 140 % of initial value after stress), while the resistance values determined at currents close to 0 mA show a stronger increase with increasing storage times (reaching the 440 % of initial value after stress). While the resistances determined at the higher voltage regions reflect the spreading sheet resistances of the p-GaN epilayers, the increase of the

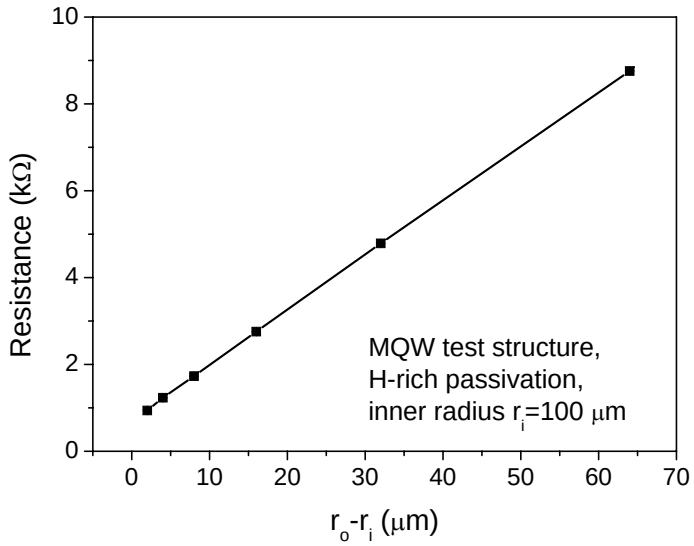



**Figure 5.4:** total resistance vs contact spacing curve measured on a TLM test structure. Curves have been corrected by factor C as indicated in Equation 5.3

differential resistance around zero indicates the deterioration of the electrical properties of the contact at the GaN/metal interface [132].

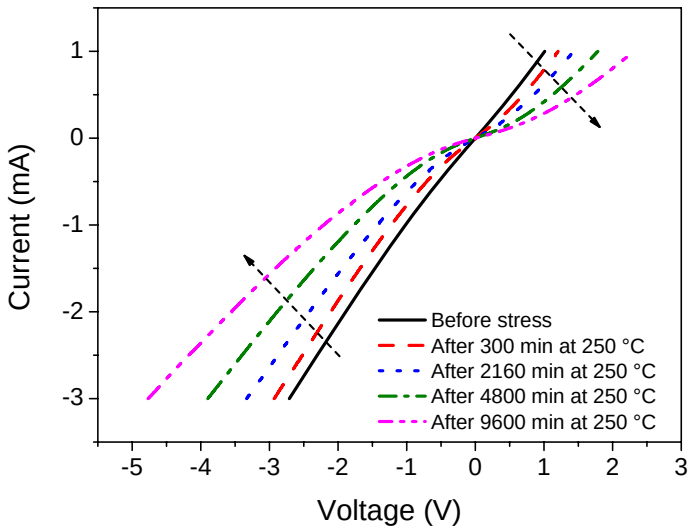



**Figure 5.5:** I-V curves measured on a TLM test structure with H-rich PECVD passivation layer during stress (PAD H in Figure 5.1 and 5.2, stress at 250 $°C$)

## 5.4 TLM parameters extrapolation

A quantitative description of the variation of the sheet resistance and of the contact resistivity during stress is given in Figure 5.6: the parameters were estimated using Equation 5.1- 5.4. As can be noticed, after stress the sheet resistance increase was limited to the 5%, while on the other hand, the contact resistivity was found to be strongly affected by the thermal treatment ($\times$ 4.8 after stress). This diagram confirms that the most important effect of stress consists in a worsening of the properties of the metal/semiconductor interface, while p-type GaN layer is only slightly affected by thermal treatment.

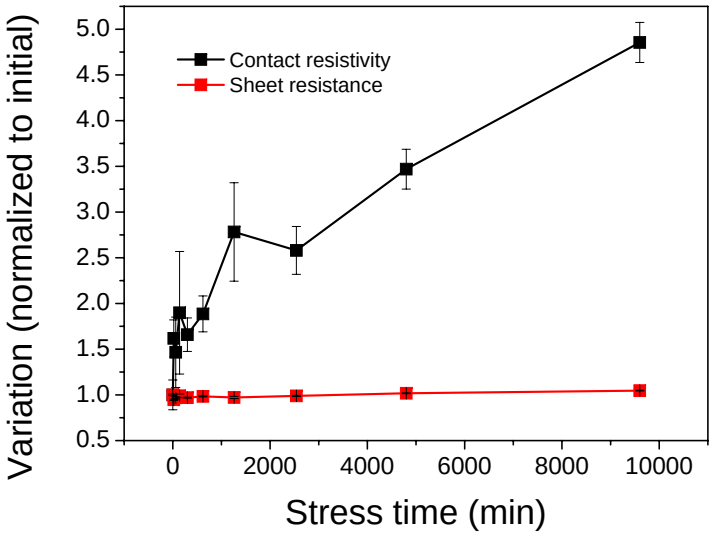



**Figure 5.6:** sheet resistance and contact resistivity variation estimated using Equation 5.1-Equation 5.4 before and during stress at 250 °C for one TLM with SiN PECVD passivation layer

Thermal storage tests carried out on GaN LEDs with the same p-layer composition and passivation showed that high temperature treatment can induce a shift of the LED I-V curves towards higher currents, without strong changes of their slope (Figure 5.7): logarithmic fitting of the I-V curves indicated that after stress the most important change in the electrical characteristics of the LEDs is the increase of the ideality factor of the diode equation, without strong modification of the series resistance of the p-GaN layer (see Chapter 4 and in particular Figure 4.14 and Figure 4.29(a)) [14, 133].

Since the characteristics of the ohmic contacts can influence the overall ideality factor of the devices [100], this results suggests that stress of the LEDs induces the degradation of the properties of the ohmic contacts, rather than a worsening of the characteristics of the p-type material. The data collected within this work confirm this hypothesis, giving a quantitative description of the amount of the sheet and contact resistance increase at the contacts (see Figure 5.6). The comparison between the electrical degradation of the TLMs and of the LEDs indicates that in both cases the most important degradation process is the worsening of the metal/semiconductor interface: on the other hand, the sheet resistance of the p-GaN layers is thought to be affected by stress test only in a minor way.

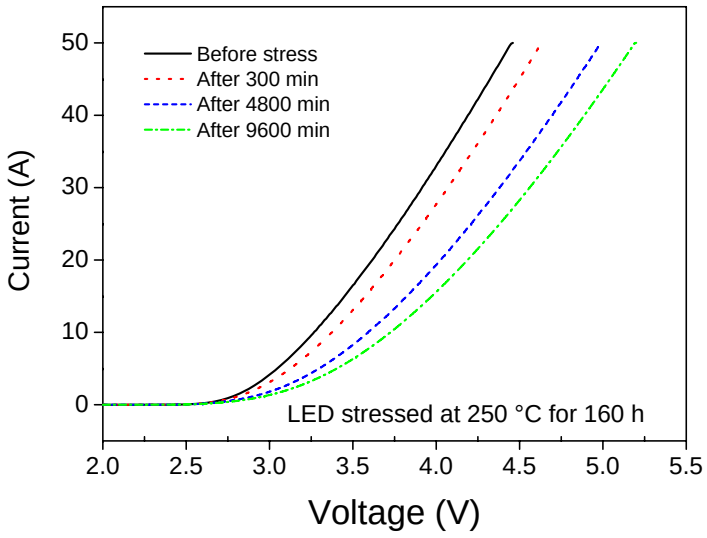



**Figure 5.7:** I-V curves measured on a LED test structure with H-rich PECVD passivation layer during stress (stress at 250 $°C$)

## 5.5 Discussion of the results

An interpretation for the detected degradation process is given in this section. On the basis of the results obtained Chapter 4, the degradation of the properties of the p-side ohmic contact and semiconductor layer can be attributed to the interaction between the passivation layer and TLMs surface [14]. As a consequence of passivation deposition process, hydrogen is incorporated at the interface between passivation and

p-GaN layer, due to the use of $SiH_4$ and $NH_3$ as precursors. During heating at 250 °C, hydrogen can interact with LEDs surface, generating bonds with the magnesium acceptor dopant, and reducing effective acceptor concentration under the contact [8, 134]. Before stress, the behaviour of the TLM contacts on p-GaN is ohmic, and their characteristic are linear. This ohmic behaviour is usually obtained by means of a tunnelling metal-semiconductor junction, with an high acceptor concentration in p-type GaN ($> 10^{19} cm^{-3}$). A reduction of the acceptor concentration or an interaction between hydrogen and the metal contact (due to the interaction with the passivation layer) can induce a variation of the Schottky barrier at the metal/GaN interface, with subsequent rectifying behaviour. The fact that after stress the contact resistivity shows important degradation while p-type GaN resistance demonstrates only a slight increase (Figure 5.6) indicates that the degradation process mostly interests the surface of the LEDs (i.e. the region immediately under the metal contact) rather than the deep p-type material: it is worth mentioning that the interaction between hydrogen and TLM surface could be facilitated by the metal material, as reported for other semiconductors in previous works [135].

In order to clarify the role of hydrogen in the degradation process, we have submitted TLMs without passivation to thermal storage in different atmospheres, air and forming gas (hydrogen concentration = 5 %). As a result, we found that storage carried out in air did not induce significant degradation, while annealing in forming gas atmosphere induced the same electrical degradation process observed on the TLM with PECVD passivation (with a different kinetic due to the different hydrogen concentration in the passivation and in the forming gas): this is shown in Figure 5.8 that reports the I-V curves measured on a TLM without passivation before and after a 3 hour annealing carried out in forming gas atmosphere at 250 $°C$. This result confirms the role of hydrogen in the degradation process analyzed within this work, as already reported for LEDs in Chapter 4.

## 5.6 Recovery tests

After the end of the ageing tests described above, we have verified that the detected degradation process is reversible. We have therefore removed the passivation layer from

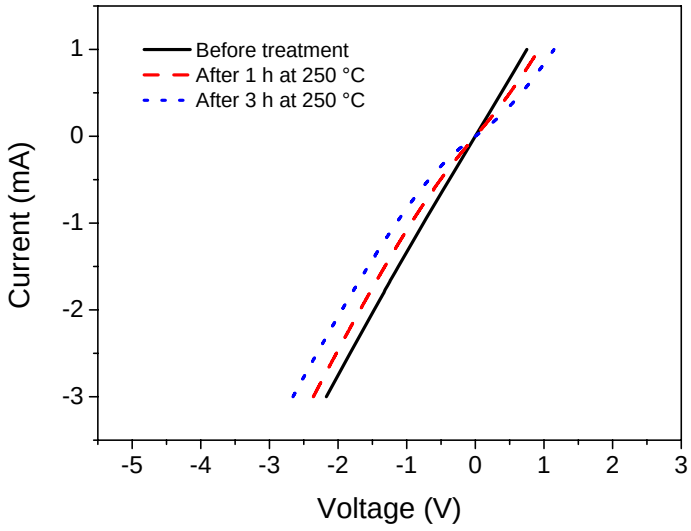



**Figure 5.8:** I-V curves measured on one of the TLMs without passivation during annealing at 250 $°C$ in forming gas atmosphere (PAD H in Figure 5.1)

the aged TLMs, and analyzed the recovery of the electrical properties during further storage at 250 $°C$.

After the removal of the passivation layer, the I-V curves of the pads constituting the TLMs did not show significant changes. Figure 5.9 shows the I-V curves measured on one aged TLM (PAD H in Figure 5.1) before and after passivation removal. These curves indicate that the removal of the passivation layer was not sufficient for the recovery of the electrical properties degraded as a consequence of stress.

The de-passivated TLMs were therefore submitted to a further thermal storage at 250 $°C$, and the I-V curves of the pads were measured at each recovery step. During this treatment, the electrical characteristics of the TLMs showed a partial recovery, as demonstrated in Figure 5.10. In this figure the I-V curve measured before stress has been plotted for comparison.

As described above, the most important modifications of the I-V measurements detected after stress were localized in the region around zero. The reciprocal of the slope of the I-V curves in this region ($R_0$ in the following) can therefore be used as a parameter to describe the kinetic of the degradation of the metal/semiconductor system. $R_0$ was evaluated by carrying out a linear fitting of the I-V curves in the region between $-0.05$ and $0.05$ $mA$.

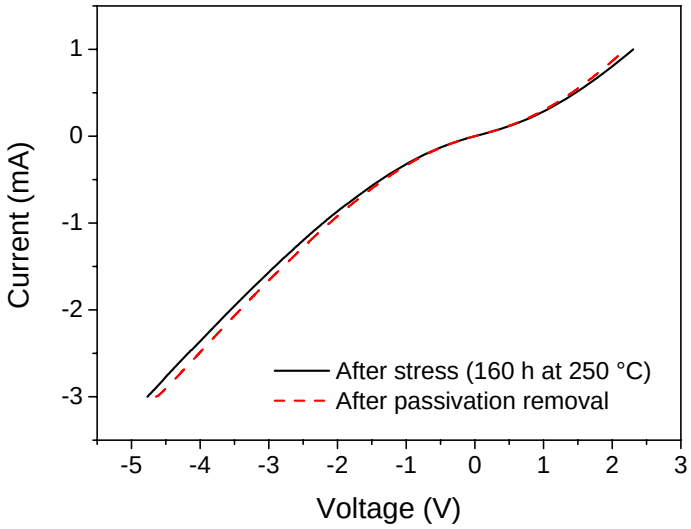



**Figure 5.9:** I-V curves measured on one aged TLM before and after passivation removal (PAD H in Figure 5.1)

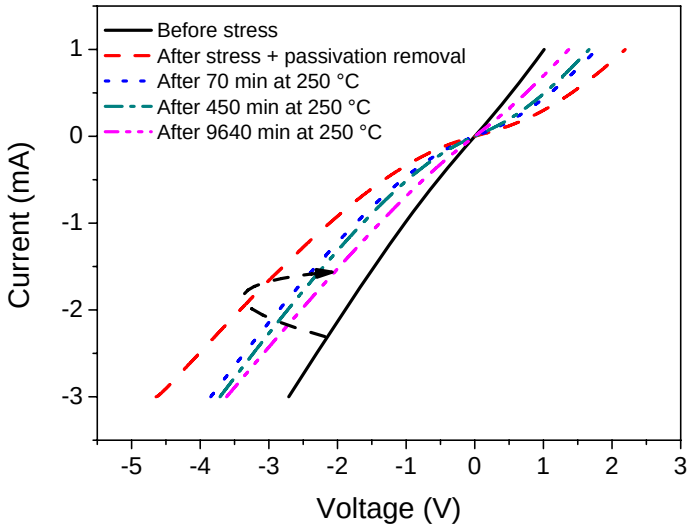



**Figure 5.10:** I-V curves measured on one aged TLM before and during the recovery test. The I-V curve measured on this device before stress is plotted for comparison (PAD H in Figure 5.1)

The kinetic of the stress and recovery processes is described in Figure 5.11, which shows the variation of the parameter $R_0$ during thermal treatment. As can be noticed, the recovery process was found to be faster than the degradation process (the ratio between the time constants of the two processes was about 6 for the analyzed samples).

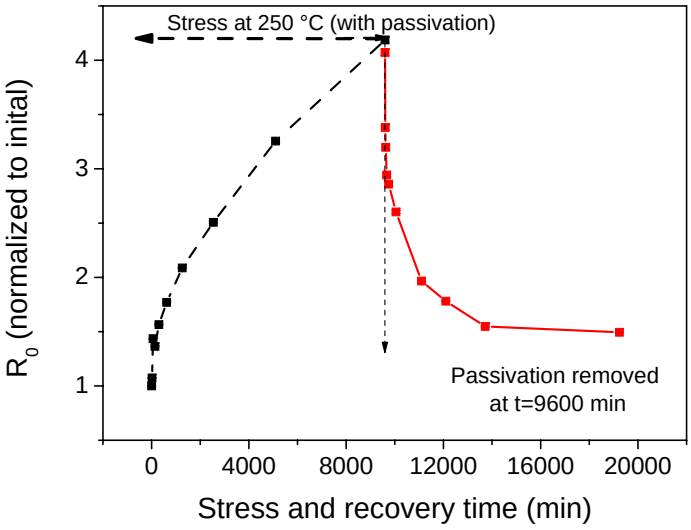



**Figure 5.11:** $R_0$ variation measured on one TLM during stress and recovery. Dashed lines are guides to the eyes. Measurements are referred to PAD H in Figure 5.1

Figure 5.10 shows that even when the recovery transient is completed, $R_0$ is not recovered to its initial value. This indicates that a second mechanism (besides the recoverable one described in this work and due to passivation) induces a permanent degradation of the ohmic contacts for long storage times [86].

This can be due to

- increased resistivity of the semiconductor material at the interface due to permanent lattice degradation
- formation of reactions with the GaN resulting in a modification of the doping profile
- generation of interface states and defects that can alter the tunnelling conduction processes

Further analysis is in progress to distinguish between these hypothesis. As indicated above, the degradation of the passivated TLMs could be ascribed to

the interaction between the hydrogen present in the passivation layer and the metal/semiconductor interface. The fact that this degradation process is reversible after devices de-passivation can be related to the fact that *(i)* the hydrogen source (passivation layer) has been removed and *(ii)* that after passivation removal hydrogen can outgas from TLMs surface.

## 5.7 Tests on TLMs with sputter passivation

The data described above confirm that the PECVD passivation layer can limit the stability of the ohmic contacts at high temperatures, due to the interaction between hydrogen and p-type material surface. Therefore, the use of an hydrogen free passivation layer is expected to improve TLMs and LEDs stability at high temperatures. In order to confirm this hypothesis and to propose a stable passivation layer to be used for LEDs, we have analyzed the behaviour of a set of TLMs with sputtered $SiN$ passivation layer during thermal storage.

By means of sputtering it is possible to deposit passivation layers with low hydrogen content. However, sputtering process could imply damage of the surface of the contacts, thus determining poor contact properties with respect to PECVD passivation deposition. Therefore, before carrying out the ageing tests, we have verified whether the use of sputtered passivation is equivalent to the use of PECVD in terms of characteristics of the contacts and devices, comparing the performance of LEDs and TLMs with PECVD and sputter passivation. As a result, we have found that there is no significant difference in the electrical and optical characteristics of TLM and LEDs with the two passivation layers (not shown here). Adopted sputtering process is therefore thought to not significantly worsen contacts properties with respect to PECVD deposition.

TLMs with sputtered passivation showed minor degradation than the PECVD ones. After stress the I-V curves measured between the pads showed only a slight non-linearity, indicating good stability of the electrical contacts (see the I-V curves measured on samples with PECVD and sputtered passivation in Figure 5.12(a) and 5.12(b)).

As can be noticed in Figure 5.13 for the TLMs with sputtered passivation also

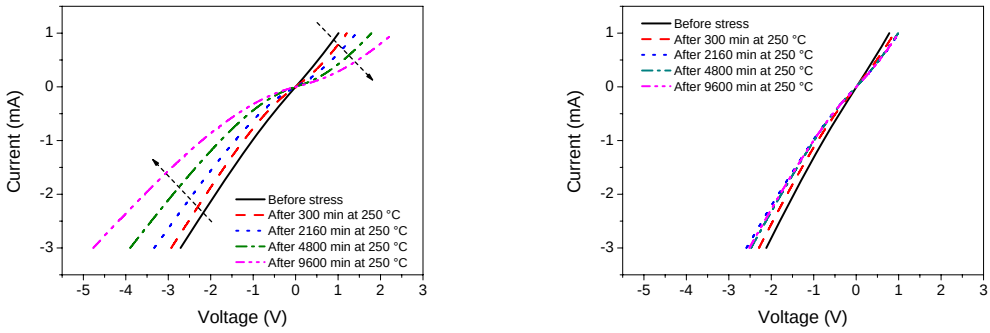



**Figure 5.12:** I-V curves measured on one TLM with (a) PECVD and (b) sputter passivation during stress st 250 $°C$

the variation of $R_0$ (x 2) during stress was less significant with respect to PECVD passivation (x 4.2). This result can be interpreted considering that the sputtered passivation has a minor hydrogen content with respect to PECVD one, because no H-containing precursor is used during sputtering. High temperature treatment has therefore a minor impact on degradation of the contacts of sputtered devices: sputtered passivation is an efficient alternative to PECVD in terms of devices stability at high temperature levels.

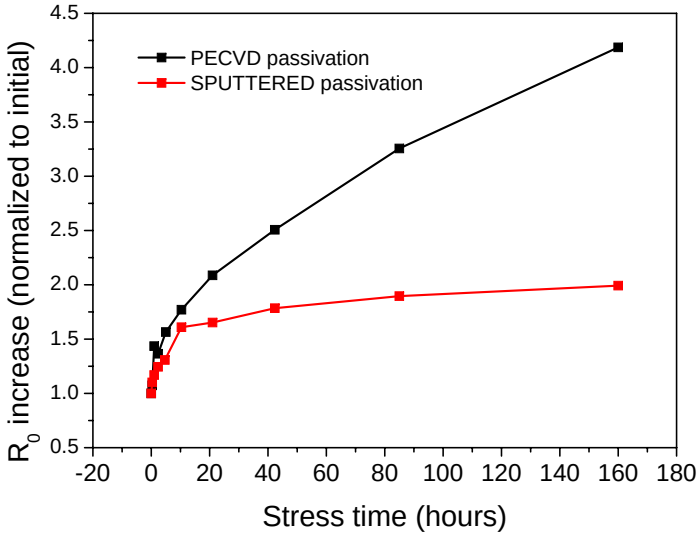



**Figure 5.13:** $R_0$ variation measured on the TLM structures with PECVD and sputtered passivation during stress at 250 $°C$ (PAD H in Figure 5.1)

## 5.8 Conclusions

This chapter provided a description of the high temperature degradation of ohmic contacts on p-type gallium nitride related to passivation. The analysis has been carried out by studying the behaviour of TLM structures with PECVD passivation during high temperature treatment. It is shown that thermal storage can induce strong modifications of the I-V characteristics of the TLMs: in particular a rectifying behaviour and a slight series resistance increase were detected as a consequence of storage.

Degradation has been attributed to the interaction between p-type semiconductor material and the hydrogen in the PECVD passivation: we have shown that the most important result of this interaction is a worsening of the ohmic properties at the metal/GaN interface, while only a slight increase of semiconductor sheet resistance is detected after stress. Results are consistent with previous findings about LED degradation at high temperatures described in Chapter 4.

Degradation process was found to be reversible, after passivation removal and subsequent annealing. Finally, the use of sputtered passivation layers has been proposed as a more stable alternative to the conventionally adopted PECVD passivation for devices to be used in high temperature environment.

# Chapter 6

# Degradation of high power LEDs

This chapter presents an experimental analysis of high brightness light emitting diodes (HBLEDs) performance and high temperature stability. Three different families of HBLEDs from three leading manufacturers have been considered. The analysis has been carried out by means of current-voltage, integrated optical power and electroluminescence measurements, and failure analysis.

After an initial characterization of the electrical, optical and thermal behavior of the devices, a set of ageing tests was carried out under high temperature stress conditions. Identified degradation modes were efficiency decrease, series resistance increase, and modifications of the emitted spectrum.

Characterization of devices behavior during thermal stress indicated that the reliability of white LEDs can be strongly limited by the degradation of the package/phosphors system, determining the worsening of the chromatic properties of the devices. Analysis carried out at different temperature levels showed that the described degradation process is thermally activated, with an high activation energy equal to 1.5 $eV$ for the analyzed devices.

## 6.1 Motivation

Gallium nitride based LEDs have recently shown to be excellent candidates for the next generation of light sources. The industrial relevance of these devices is increasing for various types of products or components: automotive applications, medical applications, indoor and outdoor lighting, decorative lighting, signals, display

backlighting. High efficiency, good robustness to ESD events and shocks, fast response, expected long lifetime (50-100,000 h) are the most important features of GaN LEDs, that have attracted the lightning community towards this kind of devices.

During the last years, many efforts have been done in order to improve devices performance: as a results, LEDs with output power of several watt are now commercially available. The development of high power LEDs strengthens the importance of devices thermal management: package thermal resistance and capacity must be optimized in order to avoid devices thermal degradation, and temperature-activated degradation processes must be carefully analyzed.

Furthermore, the ever increasing adoption of LEDs for the realization of solid-state based light sources implies a certain interest in optimizing the driving conditions for these devices in order to achieve an improvement in devices performance and reliability. In particular, two schemes are widely used in the industry for LED dimming: decreasing the forward current (continuous current reduction, CCR), or changing the duty cycle by pulse-width modulation (PWM). In general, PWM is more popular in the industry for dimming LEDs, because of its wide dimming range and the linear relationship between the light output and the duty cycle [136]. These two dimming methods imply different bias strategies: CCR is obtained using dc bias, while PWM is realized by means of square-wave current driving. Although implying a higher current stress for the device, the latter strategy is capable of offering advantages to the power supply designer. The most important fact is that the amount of passive filters required by the power supply can be considerably reduced. It is therefore important to evaluate in detail how the adoption of these two driving strategies can influence the performance and the reliability of the devices. Therefore, the first part of this chapter will report a detailed analysis of the performance of high-power LEDs submitted to dc and pulsed bias driving.

The second part of the chapter will focus on the impact of high temperature stress conditions on the reliability of high power white LEDs. During the last period, many works on LEDs degradation have been published, see for example [11, 23, 24, 30, 9, 137, 14, 16]: in most of the cases, these papers described the behaviour of power LEDs submitted to high current stress. In these cases it is difficult to distinguish whether detected degradation effects are ascribable to carrier flow or

to high temperatures reached by the junction during stress, and a model for thermal degradation of the devices can not be efficiently derived.

Therefore, the aim of the second part of this chapter is

- to study the degradation kinetics of high-power white LEDs submitted to pure temperature storage: during stress, no bias has been applied to the junction, in order to avoid carrier flow related degradation, finally describing only the degradation processes depending on temperature;
- to describe the optical and electrical degradation modes detected as a consequence of stress;
- to show that high-temperature degradation kinetics have an Arrhenius dependence on temperature, and to extrapolate the activation energy of the degradation process.

## 6.2 Analysis of LEDs performance under dc and pulsed bias

### 6.2.1 Analyzed devices and tested driving conditions

For this work we analyzed three different families (A, B, C) of commercially available white LEDs, from three leading manufacturers. The devices of family A and B are rated for a maximum electrical power of about 2 $W$, while devices of family C can reach higher power levels (5 $W$). All the devices have a similar structure: a protection diode is connected in parallel to the blue InGaN/GaN chip, and the blue-to-white light conversion is achieved by means of the deposition of a phosphorous layer on the LED chip.

If mounted on a properly sized heat sink, the devices can guarantee a low thermal resistance ($8 - 9$ $K/W$): in these conditions the operating temperature can be well below the maximum recommended value of $100 - 125°C$, and the devices are capable to show good electro-optical stability even during several thousands of hours of operation. The basic characteristics of the devices under test are summarized in Table 6.1. It is

worth mentioning that the structure of the highest power devices (Family C, 5 $W$) is constituted by the series/parallel connection of a set of LEDs: this is the reason why the typical forward voltage is higher with respect to the devices of family A and B, as well as the dissipated electrical power for the same current level.

| Device Family | Rated Power [$W$] | Rated Forward Current [$mA$] | Typical Forward Voltage [$V$] |
|---|---|---|---|
| A | 2.1 | 500 | 4.2 |
| B | 2.3 | 500 | 4.6 |
| C | 5 | 700 | 6.8 |

**Table 6.1:** Basic characteristics of the analyzed devices

A characterization of a wide set of samples was carried out by means of current-voltage (I-V), optical power (OP) and electroluminescence (EL) measurements: the devices of the three families showed uniform characteristics, demonstrating the high quality of the production process. After this preliminar characterization, we have evaluated the impact of different driving strategies on devices performance. In particular, we have compared dc and square-wave current driving in term of devices emitted power, devices efficiency and junction temperature. All the tested driving waveforms had the same average current level, in order to achieve consistent comparison. Pulsed waveforms had frequency in the range 100 Hz-700 kHz, and duty cycles in the range 10-100 % (see Figure 6.1 for a graphical representation of the concept of duty cycle): peak current was varied accordingly to keep the average current unchanged, according to

$$I_{peak} = I_{avg}/D \tag{6.1}$$

The results of the thermal and optical analysis did not show significant dependence on the frequency of the driving waveform: in the following sections we report the results obtained driving the devices with square-wave bias, with frequency equal to 200 kHz. The thermal resistance of the devices was evaluated by means of the method described by Xi and Schubert [111, 112], as explained in Section 6.2.2 (see also Section 3.3.1 for comparison). Results are explained in the following sections.

$$D = \frac{\tau}{T}$$

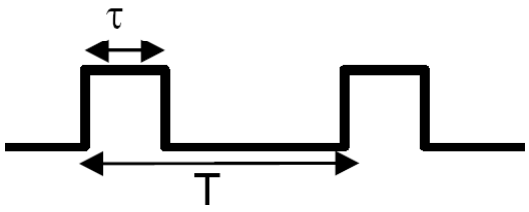



**Figure 6.1:** Representation of the concept of duty-cycle

### 6.2.2 Thermal characterization

As described above, it is important to evaluate the thermal behavior of high power LEDs to be used for lightning applications. In this section, we describe a thermal analysis of LEDs submitted to dc and pulsed bias driving. In order to better understand the effects of temperature on devices efficiency, we used a simple heat sink, consisting in a copper frame. For this reason, the thermal resistance and temperature values extrapolated by means of the measurements are higher than the ones reccomended for operation.

We evaluated the average temperature of the devices during bias using the thermal resistance value estimated by means of the method described in [111, 112]. A set of voltage measurements was carried out at different current (between 100 and 300 $mA$) and temperature (between 35 and 90 $^\circ$ $C$) levels in a thermal chamber. The measurements were carried out using short current pulses, in order to avoid devices self heating.

Figure 6.2 (referred to the devices of family A) shows that for each measuring current ($I_m$) level the relation between the corresponding voltage and temperature is roughly linear: the slopes of the curves in Figure 6.2 were therefore evaluated by means of linear fittings, and used as coefficients for junction temperature evaluation in the following analysis.

The chamber temperature was subsequently fixed at 35 $^\circ$ $C$, and the devices were biased for a fixed period (120 seconds) at each of the measuring current levels used

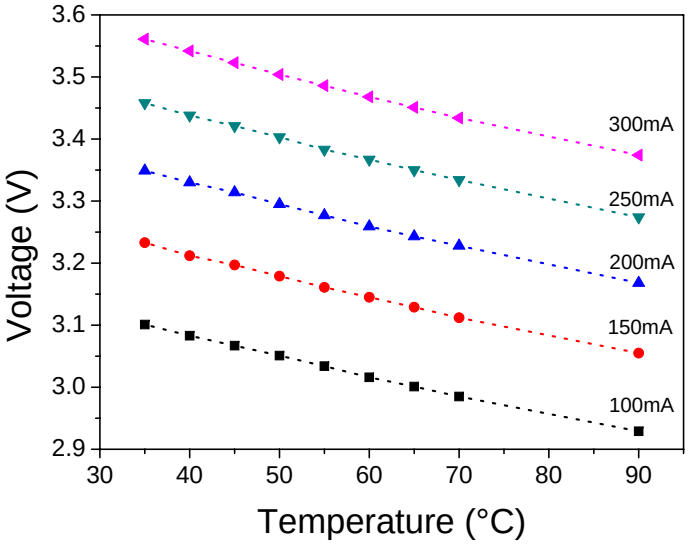



**Figure 6.2:** $V(I_m, T)$ curves measured for different $I_m$ levels between 100 and 300 $mA$

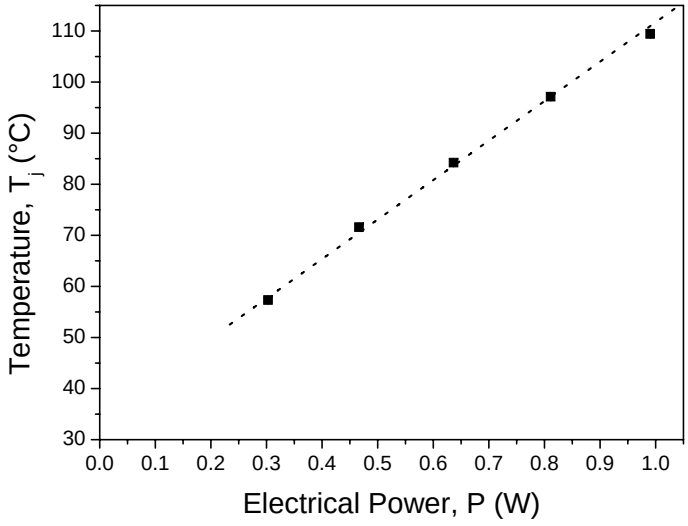



**Figure 6.3:** Junction temperature vs electrical power curve extrapolated from electrical measurements

before: the voltage reached by the LEDs at the end of this period was then measured. This voltage value corresponds to the temperature reached by the junction after the self heating transient. By means of the coefficients calculated before we extrapolated the junction temperature ($T_j$) at each measuring current level, and the temperature vs electrical power diagram reported in Figure 6.3 (family A). The same analysis was carried out for the other families of devices: thermal resistance values of 74, 63 and 67 were extrapolated for the devices of family A, B and C respectively. These values are well above the ones obtained with a properly sized heat sink, and imply a more significant self heating of the LEDs during bias.

It is worth noticing that the thermal resistance values listed above possibly slightly underestimate the actual value, due to the fact that the calibration measurements have been carried out assuming the junction temperature to be exactly equal to the temperature set in the thermal chamber, but a slight self heating can take place even during the short current pulses used for the characterization. A further approximation is related to the fact that not all the electrical power injected in the devices is converted into heat: a small portion ($5 - 15$ % depending on device) is converted into light. Therefore, in order to obtain a more accurate estimation of junction temperature, it would necessary to estimate the optical power emitted by the devices at the different current levels. However, our laboratories are not equipped with a calibrated optical power measurement system, and therefore this analysis is impossible. This fact implies a slight overstimation of the junction temperature values. The next generation of LEDs is expected to reach very high efficiency levels (close to 150 lm/W). It is expected that these devices will have a 50 % wall plug efficiency [138]: in the case of these devices the approximation of considerig the power level contributing to junction heating equal to the injected electrical power will no longer hold.

As explained above, the aim of this section is to describe the thermal and optical behavior of high-power LEDs under different bias conditions, i.e. dc and pulsed current driving. The LEDs have been therefore driven with dc and pulsed current bias, using different duty cycles ($d$) and the same average current value. For each used bias condition, the average junction temperature ($T_j$) was estimated by multiplying the extrapolated thermal resistance value for the average electrical power injected in the devices: the results are described by Figure 6.4, which shows the variation of $T_j$ with

duty cycle during pulsed bias at an average current of 400 $mA$ (results referred to family A). As can be noticed, decreasing the duty cycle (and therefore increasing the peak current value in order to keep the average current unchanged) implies an increase of the average junction temperature. The same behavior was observed for the two other families of devices: for family B (C) junction temperature was found to increase from 105 (153) to 137 (170) varying the duty cycle from 100 % (dc) to 30 %. The temperature values reported in Figure 6.4 represent the mean values reached by the junction after several periods of operation under pulsed bias: it is worth noticing that the peak temperature values reached by the junction during the on-phase of the driving pulses are higher than these average values, and temperature is expected to show a ripple when the LEDs are submitted to square-wave bias.

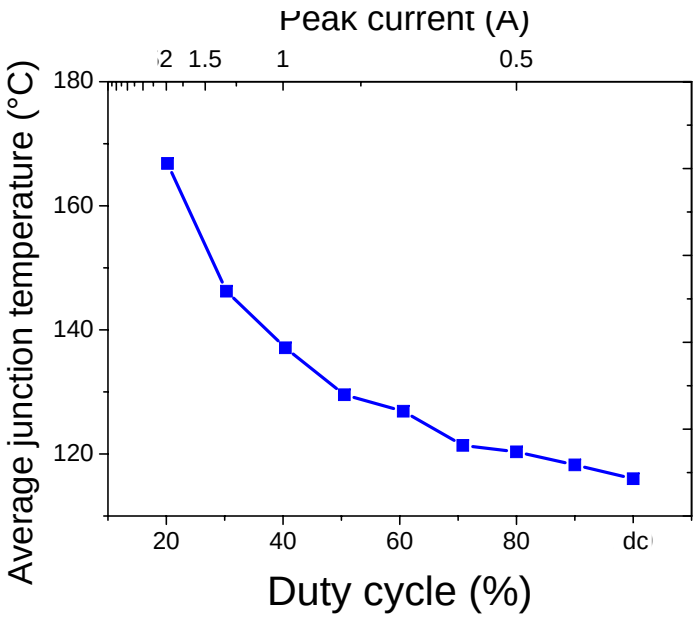



**Figure 6.4:** average junction temperature of an LED of family A driven using dc and square wave bias with a 400 $mA$ average current ($f = 200\ kHz$, different duty cycles)

### 6.2.3 Optical characterization

This section describes the the impact of duty cycle variations on LEDs efficiency: this analysis has been done by driving the samples with square-wave bias at a fixed average current level, and measuring the EL spectra for different duty cycles varying the peak current of the waveform accordingly.

Figure 6.5 shows the electroluminescence spectra of samples of Family A measured at 400 mA average current, with duty cycle varying in the range $20 - 100\%$. The EL spectra of all the analyzed samples showed two peaks centred near 460 nm (quantum well-related emission) and 565 nm (yellow phosphorous emission). As can be noticed, the decrease of the duty cycle of the driving waveform (and the corresponding increase of the peak current level in order to keep the average current equal to 400 $mA$) implies the decrease of devices efficiency. The blue emission peak showed a 50 % decrease as a consequence of a reduction of the duty cycle of the driving waveform from 100 % to 12 % (see Figure 6.6): also the intensity of the yellow peak decreased (see Figure 6.7) as a consequence of the reduction of the duty cycle of the driving waveform.

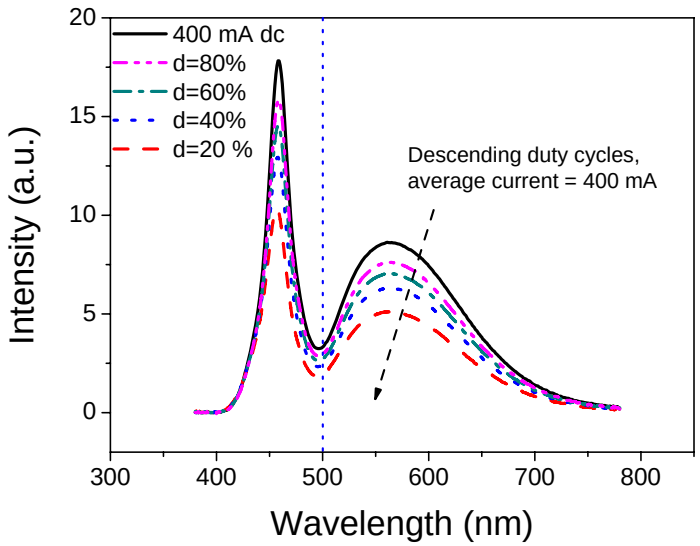



**Figure 6.5:** Electroluminescence spectra of one LED of family A driven using dc and square wave bias with a 400 $mA$ average current ($f = 200\ kHz$, different duty cycles)

Furthermore, the reduction of the duty cycle of the driving waveform implied a slight shift of the chromatic properties of the devices, corresponding to an increase of the efficiency of the blue-to-yellow conversion process. This effect can be analyzed by estimating the ratio between the integral of the yellow emission (part of the EL spectra comprised between 500 and 780 nm) and the integral of the blue emission (part of the EL spectra comprised between 380 and 500 nm) by means of

$$r = \frac{Yellow\ emission}{Blue\ emission} = \frac{\int_{500}^{780} I d\lambda}{\int_{380}^{500} I d\lambda} \tag{6.2}$$

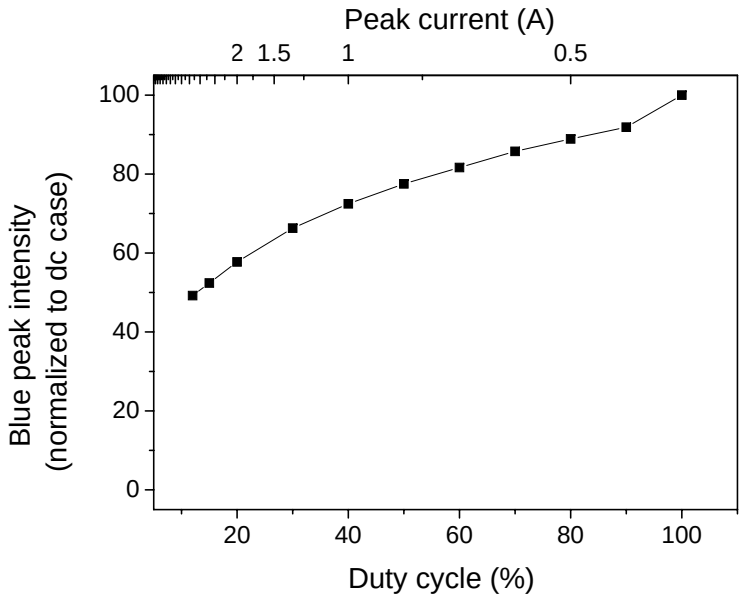



**Figure 6.6:** Intensity of the blue peak of the electroluminescence spectra of one LED of family A driven using dc and square wave bias with a 400 $mA$ average current ($f = 200\ kHz$, different duty cycles)

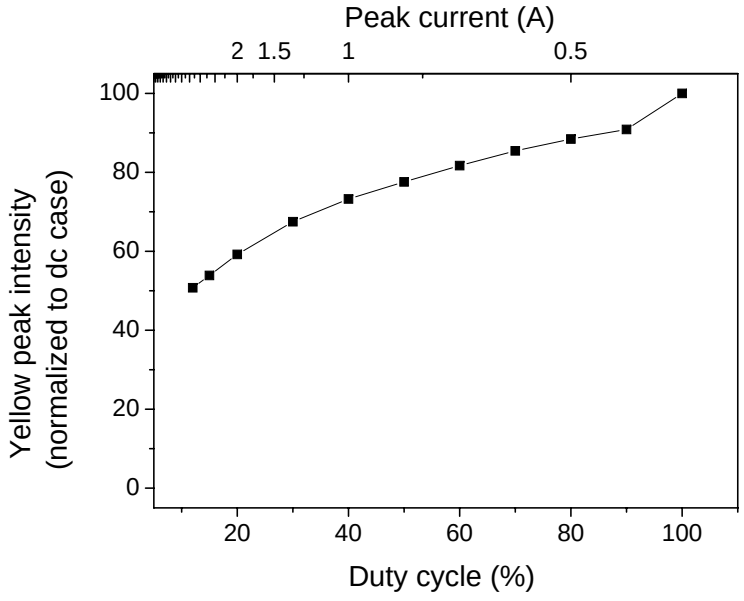



**Figure 6.7:** Intensity of the yellow peak of the electroluminescence spectra of one LED of family A driven using dc and square wave bias with a 400 $mA$ average current ($f = 200\ kHz$, different duty cycles)

as proposed in [139] (see also Figure 6.8).

In Figure 6.9 it is shown the variation of the ratio $r$ between the intensity of the yellow and blue emission corresponding to a reduction of the duty cycle of the driving waveform, for the same average current level. As can be noticed, decreasing the duty cycle from 90 % to 12 % implies a 4 % increase of the yellow/blue ratio. This effect can be understood by considering that the wavelength of the blue peak varies with decreasing duty cycle, for the same average current level (as shown in Figure 6.10). As can be noticed, a decrease of duty cycle implies the shift of the blue radiation towards shorter wavelengths. This phenomenon is due to band-filling effect and to the screening of the Quantum Confined Stark Effect (QCSE) [140, 36, 141, 142], taking place as the peak current of the driving waveform is increased. The efficiency of the phosphors strongly depends on the characteristics of the exciting radiation [143]: a blue shift of the QW-related emission peak can vary the conversion efficiency of the phosphors, and then imply a variation of the ratio $r$ as reported in Figure 6.9.

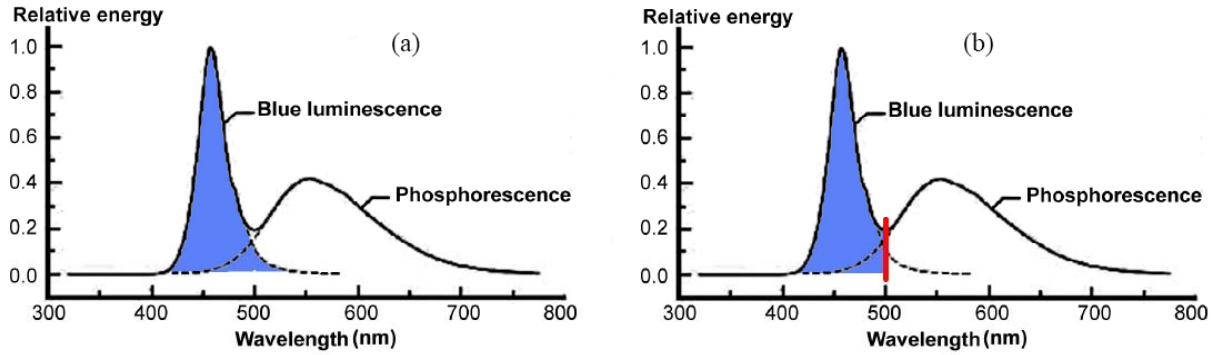



**Figure 6.8:** Electroluminescence spectra selection for analysis of yellow and blue emission intensity: (a) ideal case, (b) practical case

Figure 6.11 shows the variation of LED integrated output power with duty cycle, for the same average current level (400 mA). It is clearly noticeable that a decrease of the duty cycle implies a decrease of LEDs efficiency, even for the same average current value. This decrease is obviously related to the decrease of the blue emission peak shown in Figure 6.6. This effect is related to the fact that

- optical power is a non liner function of the bias current, so that positive increments of the bias current imply less than proportional increments of the

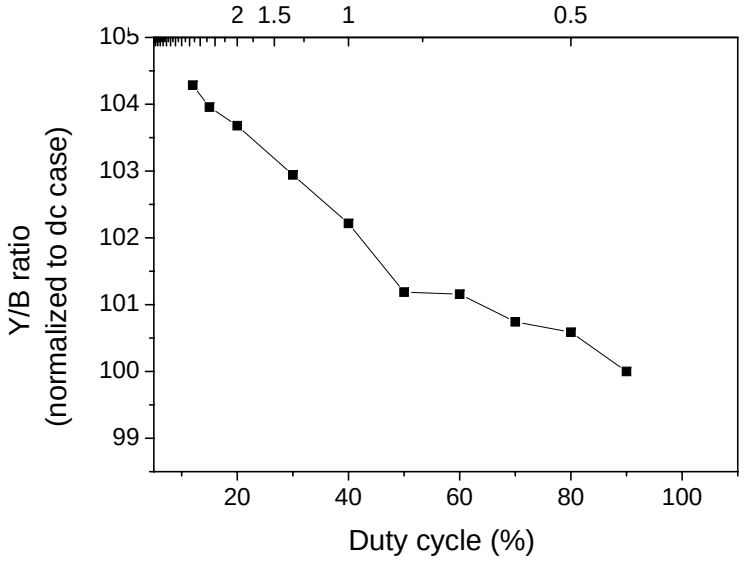



**Figure 6.9:** Ratio between the intensity of the the yellow and blue emission of one LED of family A driven using square wave bias with a 400 $mA$ average current ($f = 200\ kHz$, different duty cycles)

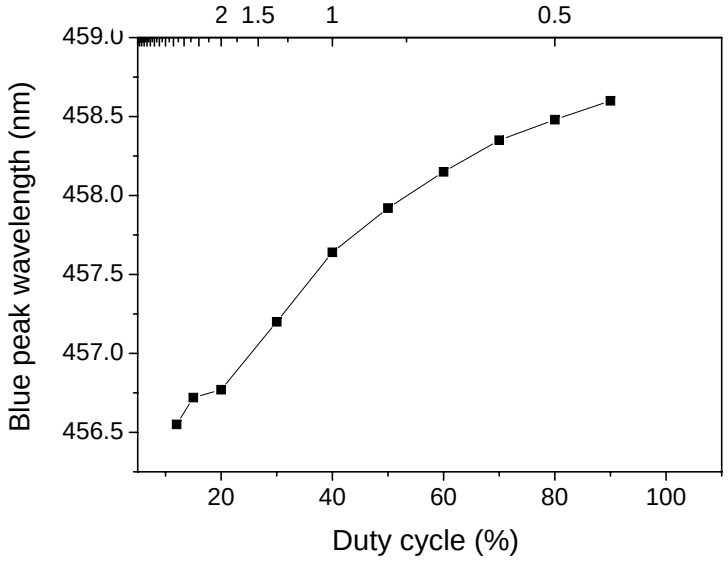



**Figure 6.10:** Variation of the wavelength of the blue peak with decreasing duty cycle measured driving one LED of family A using square wave bias with a 400 $mA$ average current ($f = 200\ kHz$, different duty cycles)

emitted power (due to carrier overflow, saturation of radiative paths, different influence of trap states, Auger recombination, ...)

- higher peak currents imply stronger self heating (see Figure 6.4 for comparison) and then a decrease of LEDs efficiency

These results suggest that driving the devices at a fixed average current with low duty cycles (e.g. lower than 40 % in this case) can imply a significant efficiency reduction (about the 30 % for d=40 %) with respect to the dc case. Therefore, pulsed bias can be a good alternative to dc bias for the same average current level, but only if duty cycle is not reduced below a certain limit (in this case 40 %) depending on the properties of the analyzed devices.

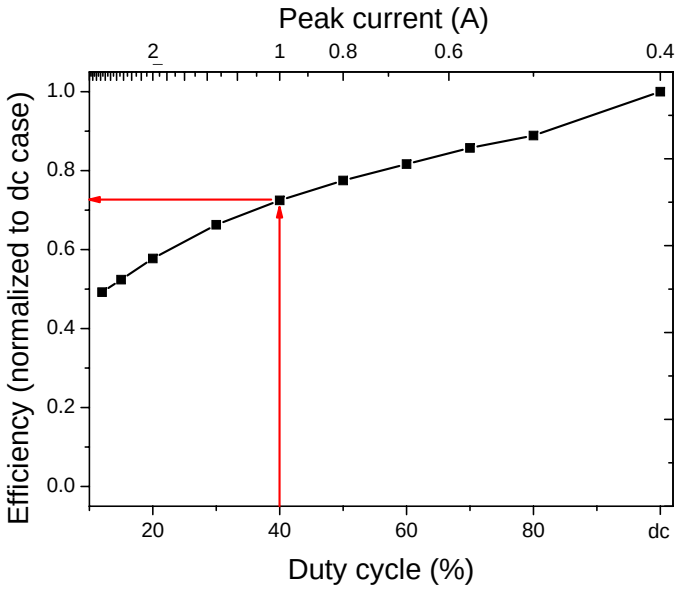



**Figure 6.11:** Variation of the efficiency of one LED of Family A with decreasing duty cycle measured driving the device using dc and square wave bias with a 400 $mA$ average current ($f = 200\ kHz$, different duty cycles)

### 6.2.4 Summary

In summary, in this section we have analyzed the dependence of the thermal and optical properties of GaN-based power LEDs on the bias conditions. In particular, we have studied the behavior of the samples under dc and square-wave current bias. All the tested driving waveforms had the same average current level, in order to obtain

consistent data comparison, but different duty cycle and peak current values. Thermal analysis showed that a reduction of the duty cycle of the driving waveform implies an increase of average junction temperature. Therefore, biasing the devices under pulsed bias implies a stronger self-heating of the devices, even for the same average current level. Furthermore, optical analysis showed that a decrease of the duty cycle of the driving waveform implies a decrease of devices efficiency, for the same average current levels. This effect has been attributed to the stronger self heating, and/or to the saturation of the radiative channels at high peak current levels. The results of these measurements show that driving power LEDs under pulsed current bias in general implies a reduction of devices efficiency with respect to dc case, even for the same average current level. Therefore, pulsed bias is a good alternative to dc bias, but duty cycle of the driving waveform must be kept high, in order to optimize devices performance.

## 6.3 Analysis of high temperature reliability of power LEDs

### 6.3.1 Analyzed devices and stress conditions

In this section we describe the effect of high temperature storage on the electrical and optical characteristics of GaN-based high power LEDs. The analysis has been carried out on two families of commercially available devices, grown by two leading manufacturers (Family A and B, see Table 6.1 for details on analyzed devices). The two families of devices showed similar behaviour as a consequence of thermal storage: for clarity, we describe in this work the results obtained on devices of Family A, which are representative also of devices of Family B. After an initial characterization of a wide number of samples, a set of devices with average characteristics has been selected for ageing tests. Devices have been stressed at temperatures ranging between 180 and 230 °C, with the aim of studying the degradation processes activated at high temperature levels. A number (3-8) of identical devices were aged at each temperature level, in order to have statistically relevant results. In this section we describe the results obtained ageing the samples at 200 °C; the devices aged at the other temperature

levels showed the same degradation mechanisms, taking place with different kinetics. Stress temperatures were significantly higher than the maximum operating temperature recommended by the manufacturer (125 and 105 °C for devices of Family A and B respectively), in order to accelerate stress kinetics. No bias has been applied to the devices during stress, in order to detect pure thermal effects, avoiding carrier flow related degradation. At each step of the storage tests, devices electrical and optical characteristics were measured, by means of current-voltage (I-V), optical power vs input current (L-I) and stress time (L-t), electroluminescence (EL) characterization.

### 6.3.2 Optical power measurements

Optical power was measured by means of a Newport 1830C Optical Power Meter, equipped with a 818-UV Photodiode and an integrating sphere. After each step of stress, devices were removed from the thermal chamber, placed at 25 °C and submitted to OP measurement. During L-I measurements, devices were biased by means of a Keithley 6221 Current Source. Stress was found to induce an optical power (OP) decrease on all the analyzed samples (Figure 6.12): devices lost the 40-60 % of their initial OP after stress, and degradation was found to be mostly concentrated in the initial part of the stress test (initial 15 hours).

### 6.3.3 Electrical measurements

Current vs voltage measurements were carried out by means of an E5263A Parameter Analyzer, using short voltage pulses, in order to avoid that self heating effects could affect measurements results. Current compliance was set to 500 mA, which is the maximum rated current for the two families of devices we have analyzed, in order to avoid electrical overstress during measurements. As shown by Figure 6.13 and 6.14, stress at 200 °C induced modifications in the I-V curves: operating voltage was found to increase during stress (nearly exponential time dependence Figure 6.15), indicating the degradation of semiconductor and/or contact properties [14]. The electrical degradation seems to be at an early stage, and is mostly explained by some fair increase (up to some 15 %) of the series resistance $R_s$. Nevertheless, the residual part of the observed electrical degradation, that cannot be related to the pure variation

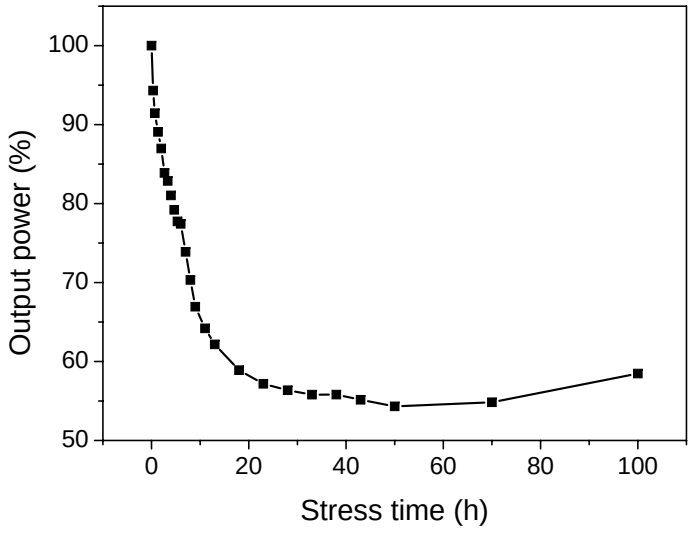



**Figure 6.12:** Optical power decrease measured (at 100 mA) during stress at 200 °C on the devices of Family A (this curve represents the average of the OP decrease measured on 4 samples aged at 200 °C)

of $R_s$, seem to prelude to other more relevant effects that have been also highlighted by means of preliminary tests at very high forward current.

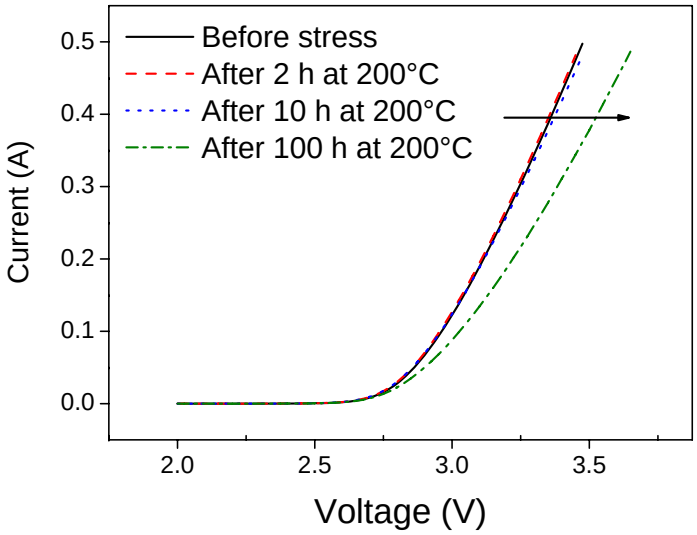



**Figure 6.13:** Current vs voltage curves measured during stress at 200 °C on one of the devices of Family A (linear current scale)

In Figure 6.16 the dc current has been (logarithmically) plotted versus the reduced

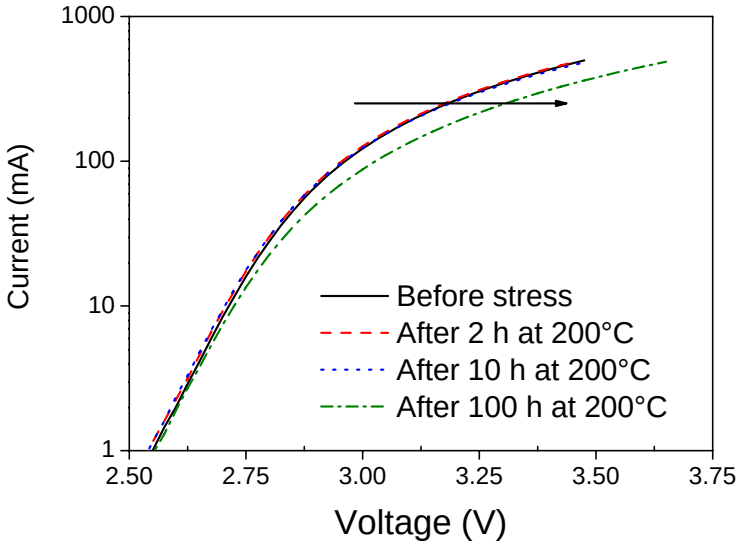



**Figure 6.14:** Current vs voltage curves measured during stress at 200 °C on one of the devices of Family A (semi-logarithmic current scale)

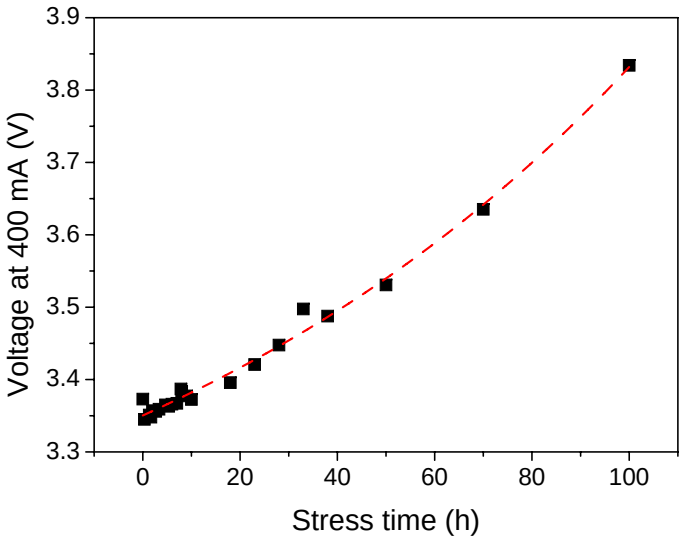



**Figure 6.15:** Forward voltage measured at 400 mA for one LED aged at 200 °C (dashed line is an exponential fitting of the data)

voltage $V - R_s I$ [144] for the initial and final states of two devices, one tested under pure thermal stress test (200 °C, no bias) and the other under high current test (400 mA dc, no heat sink). A common value of $R_s = 1.05$ allowed the two reference curves to completely overlap and jointly to display a nearly ideal exponential behaviour. The curves of the stressed samples, also drawn after removing the contribution of $R_s$, show a similar trend at the end of the two quite different tests. In both cases, nor a simple ohmic degradation (involving materials or interfaces, or both), nor a pure variation of the height of the contact barrier can give complete account for the observed slope variation in the electrical dc curves [14]. It is worth noticing that during the initial part of the stress ($t < 15$ hours), $V_F$ (and the I-V curves) was found to be nearly stable, while in the same period a strong optical power decrease was detected (see Figure 6.12). This fact suggests that the important OP decrease detected during the initial part of the stress and the worsening of chip electrical properties are not directly related.

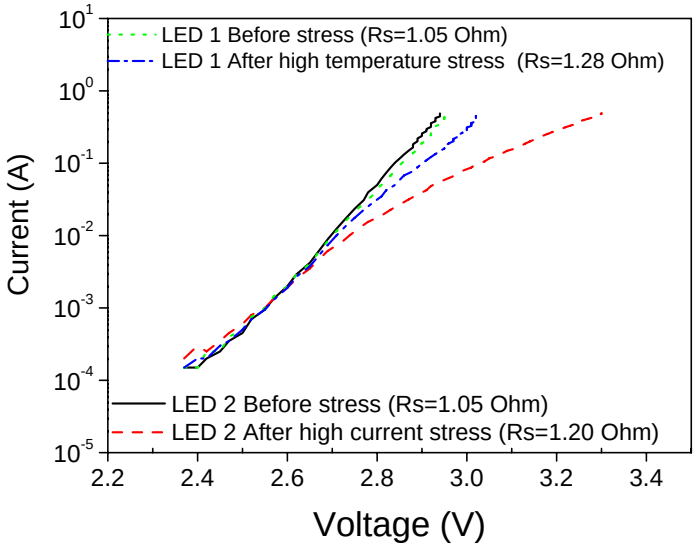



**Figure 6.16:** I-V characteristics, drawn vs. the reduced voltage $V - R_s I$, of two devices after the pure thermal test and a preliminary high current test.

### 6.3.4 Electroluminescence measurements

Results decribed in the previous section indicate that the degradation of the electrical and optical properties of the devices are not direcly related. On the other hand, optical power loss could be ascribed to modifications of the optical properties

of the devices (i.e. modification in transmissive and reflective properties of package, phosphorous layer conversion efficiency, lens, ...). In order to explore this hypothesis, and to state if modifications of the optical properties of the devices take place after stress, we have carried out measurements of the emitted spectra before and during ageing tests. In Figure 6.17 are shown the electroluminescence spectra measured during stress for one of the aged LEDs. The blue QW emission (centred around 460 nm) and the broad yellow band (centred around 560 nm) related to the phosphorous layer emission can be clearly noticed.

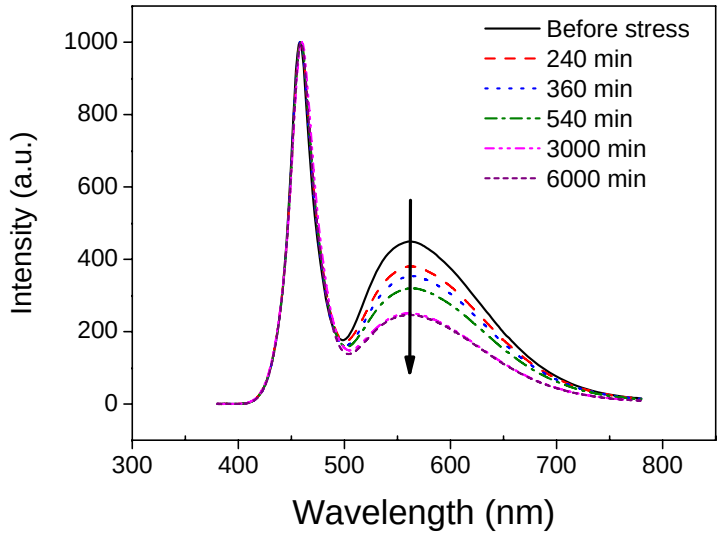



**Figure 6.17:** output spectra measured at 250 mA before and during stress at 200°C on one of the devices of Family A

The spectral data in Figure 6.17 have been normalized to the intensity of the QW peak for each stress step. Stress induced a decrease of the yellow emission, with respect to the main blue peak: the ratio $r$ between the intensity of the yellow and blue band (Y/B ratio, see 6.2) decreased from 0.45 to 0.25 as a consequence of stress (Figure 6.18). The OP decrease and the Y/B ratio variation have similar kinetics (see Figure 6.18), and this suggests that the degradation of the integrated OP of the LEDs is strongly determined by the reduction of the yellow emission: a degradation of the chromatic properties of the reflectors and lens and/or the worsening of the efficiency of the wavelength conversion process are supposed to take place as a consequence of stress, and to be strongly related to devices degradation. We have verified this hypothesis by

means of optical microscopy: results are described in the following.

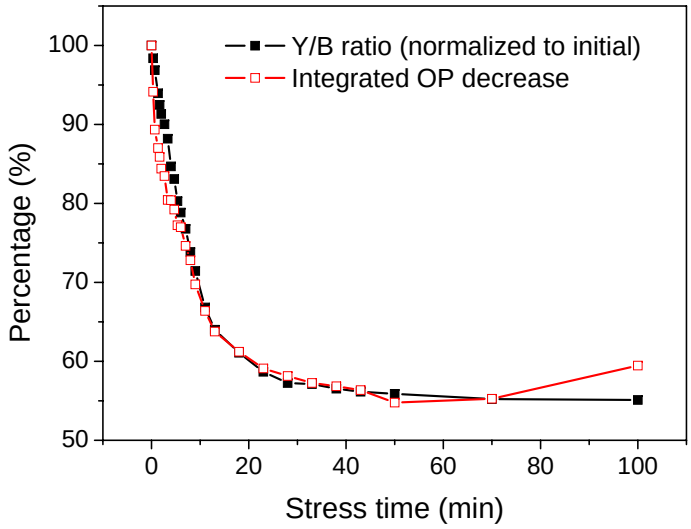



**Figure 6.18:** Y/B ratio variation measured during stress at 200°C on one of the devices of Family A. In figure is also reported the integrated OP loss kinetic shown in Figure 6.12

### 6.3.5 Analysis of package degradation

We have carried out the study of the degradation of the optical properties of the package and phosphors by means of electroluminescence and microscopy analysis. Figure 6.19 compares the Electroluminescence (EL) maps of a reference and a thermally stressed device (Family A), and refers the visible features to the cross-sectional view of the stressed device itself. The most important result is the evidence for carbonization of the white package parts. The effect of carbonization is to cancel any light reflection from the plastic ring that covers the outer edge of the copper cup that hosts the chip. A similar effect has been detected also for the devices of Family B (see Figure 6.20). However, no noticeable degradation of the epoxy lens has been detected after stress: therefore we think that the browning of the lens contributes to overall OP decrease only in a minor way.

Figure 6.21 also reveals that a third mechanism, beyond the loss of the light conversion capability and the carbonization of the white plastics, contributes to optically reduce the emitted power: the transparent thin metal layer that covers the

outward emitting surface darkens, so building an attenuating filter in front of the main emission surface of the chip.

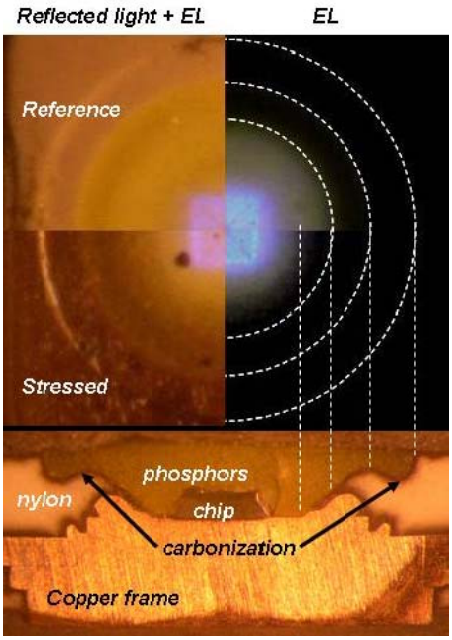



**Figure 6.19:** Comparative Electroluminescence for a reference and a stressed device of Family A, and correlation with the cross-section of the stressed specimen

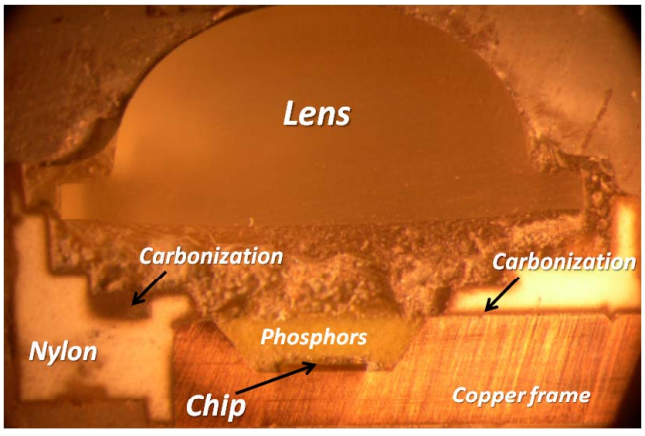



**Figure 6.20:** cross section of a stressed device of Family B, highlighting the carbonization of package surface

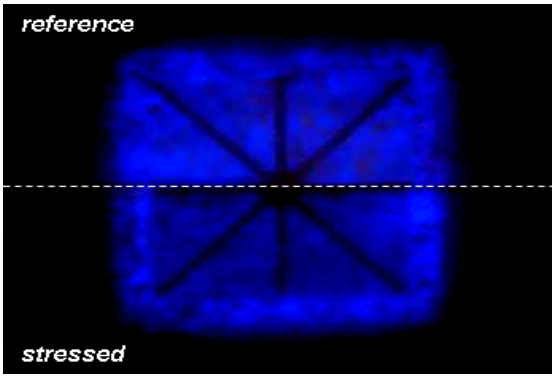



**Figure 6.21:** Comparative EL of a reference and a thermally stressed device. The thin contact layer darkens on the outward emitting surface of the stressed LED.

### 6.3.6 Activation energy of the degradation process

We have determined the dependence of degradation kinetics on stress temperature, carrying out stress tests at different temperature levels in the range 180-230 °C. The degradation of the optical properties was found to be thermally activated: an increase in stress temperature implies a decrease of the time to failure (TTF), as shown in Figure 6.22. By plotting the value of the $TTF_{70\%}$ (time necessary for a 30 % optical power decrease) vs $q/kT$ we obtained the Arrhenius plot shown in Figure 6.23, and estimated an activation energy of 1.5 eV for the thermally activated degradation process. It is worth noticing that we have analyzed a reduced number of devices for each stress temperature level: analyzed devices showed similar degradation kinetics, and the standard deviation of the analyzed parameters were small with respect to the corresponding average values. So we think that, even if the number of analyzed devices was low, measured degradation data can be representative of the statistical behavior of the devices.

### 6.3.7 Discussion and summary

With this work we have analyzed the effects of high temperature storage on the optical properties of GaN power LEDs. Stress was found to induce an optical power decrease, and an operating voltage increase. The degradation of the electrical and of the optical parameters were found to have different kinetics, suggesting that the output

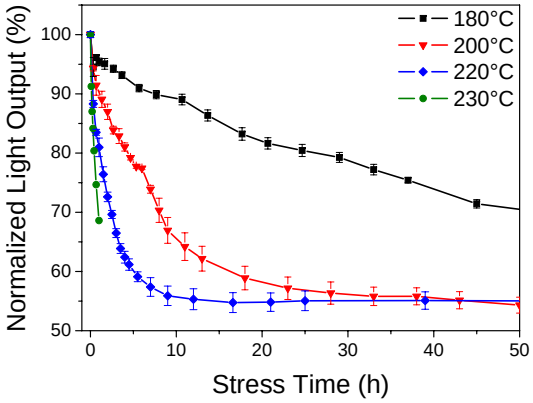



**Figure 6.22:** output power decay as measured (at 100 mA) during stress tests at different temperature levels ranging from 180 to 220 °C.

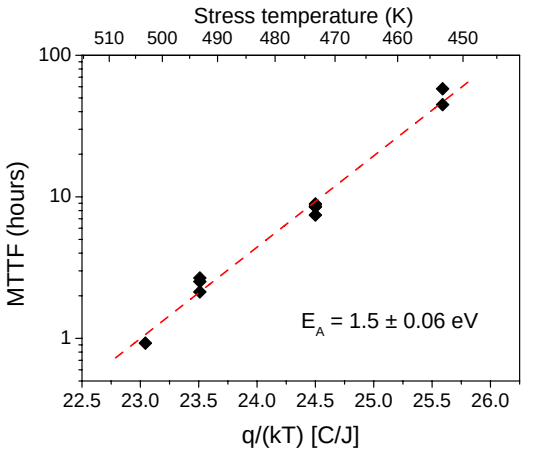



**Figure 6.23:** Arrhenius plot of the $TTF_{70\%}$ plotted versus $q/kT$; the straight line is the linear fitting curve used for the estimation of the activation energy value. Each point corresponds to the $TTF_{70\%}$ measured on one device aged at a specific temperature level

power decrease is not strongly related to the modification of the electrical properties of the LED chip. Spectral measurements indicated that thermal treatment can induce a worsening of the chromatic properties of the devices: a decrease of the yellow emission intensity was detected after stress, with subsequent shift of devices output towards bluish light.

Microscopic analysis of aged devices showed that stress induces: *(i)* the carbonization of the white plastics implying a reduction of package reflective properties; *(ii)* the darkening of the top-side contact layer. OP loss is therefore thought to be related to this set of physical degradation processes, that have a relevant impact on extraction efficiency and on LEDs spectral properties. The darkening of the plastic reflector reduces the overall phosphors volume which effectively plays a role in wavelength conversion (see Figure 6.19), thus implying the changes of the spectral properties of the LEDs: it is not excluded that stress can induce also a worsening of the conversion efficiency of the phosphorous material. On the other hand, this study did not give any information on the role of blue chip degradation on overall efficiency decrease: further work is in progress to verify whether thermal treatment determines also the degradation of the properties of the blue LED chip, and to state which is the impact of high temperature stress on the internal efficiency of the devices. Degradation process was found to be thermally activated: an activation energy equal to 1.5 $eV$ was extrapolated for the $TTF_{70\%}$ parameter, by means of thermal stress carried out at different temperature levels. This activation energy is thought to be mainly related to the degradation of the plastic package and phosphorous material. Further tests are in progress in order to state if the Arrhenius plot in Figure 6.23 can be extended to lower temperature levels, i.e. below the maximum temperature recommended by the manufacturer (105-125 °C).

## 6.4 Conclusions

In this chapter we have presented an analysis of the performance and reliability of high-power LEDs based on gallium nitride. This work has been carried out on commercial devices produced by three leading manufacturers. In the first part of the chapter we have described the thermal and optical behavior of the devices and the

dependence of the main parameters on the driving strategy. In particular, we have compared the use of dc and pulsed driving: all the used driving waveforms had the same average current level, in order to obtain consistent comparison. It has been shown that the use of pulsed waveforms implies a stronger self-heating of the devices, with respect to dc driving. Furthermore, we have shown that the use of square-wave driving implies a lower devices efficiency with respect to dc case, even for the same average current value. For this reason, we state here that driving power LEDs with pulsed waveforms can be an alternative to dc bias, provided that low duty cycle values are avoided, because they can imply a strong reduction of devices efficiency with respect to dc case (even for the same average current level).

In the second part of the chapter, we have analyzed the high temperature reliability of high power LEDs. We have shown that thermal treatment can induce optical power decrease, modifications of the electrical properties of the LEDs and changes in the emitted spectra. By means of combined optical and microscopical analysis we have demonstrated that the decrease of devices efficiency is strongly related to the darkening of the package of the devices, due to the high temperatures reached during stress. On the other hand, we have shown that the high temperature degradation of power LEDs is not strongly related to the worsening of the properties of the contacts and of the blue semiconductor chip. Furthermore, we have shown that degradation process described in this work is thermally activated: by means of ageing tests carried out at different temperature levels, we have demonstrated that the activation energy of the degradation process is equal to 1.5 eV for the analyzed devices.

# Chapter 7

# Degradation of Laser Diodes

This chapter describes an analysis of the reliability of GaN-based laser diodes: in particular, we have analyzed the the dependence of the degradation kinetics on devices operating conditions (current, optical power and temperature), by means of a wide set of ageing tests.

We demonstrate here that constant current and constant optical power stress induce the increase of the threshold current of the devices, that varies according to the square-root of time. The threshold current increase is found to be strongly correlated to the decrease of the sub-threshold emission of the devices, thus suggesting that stress determines the increase of the non-radiative recombination rate in the active layer.

Degradation rate is found to depend on stress temperature and current level, while it does not significantly depend on the optical field in the cavity. On the basis of these evidences and of previous literature results, we attribute devices degradation to the diffusion of impurity species towards the active layer, with subsequent increase of the non-radiative recombination rate. The identified degradation process is supposed to be electro-thermally activated.

## 7.1 Motivation

Blue and violet InGaN-based laser diodes (LDs) play a very important role in the new generation of optical storage systems. The properties of III-V nitrides and related alloys allow for production of high quality blue LDs, to be used in the new generation blue-ray disk systems.

Despite a rapid increase in the market for nitride based optical devices, the knowledge about physical processes occurring during operation is rather poor compared to the case of conventional GaAs-based devices. In particular, little is known about degradation mechanisms in nitride LDs. In comparison with the conventional III-V devices based on GaAs, nitride LDs are very robust in terms of cohesion and defect formation energy. Therefore, dislocation generation and propagation are not expected to be the main contributions to the device aging processes like it is in GaAs laser diodes [7].

In the first devices fabricated on GaN grown on sapphire substrates, the main cause of degradation were defects originating from the lattice mismatch between epitaxial layers and insulating substrate. Typical dislocation densities were of the order $10^8 - 10^{10}\ cm^{-2}$ [6] and the reported lifetimes of these LDs were between one second and hundred hours [43]. Indeed, since the early days of the development of nitride laser diodes, the use of dislocation filtering by lateral epitaxial overgrowth (ELOG) method, enabled the realization of more reliable devices, by lowering the density of down to the $10^6 - 10^7 cm^{-2}$ range [43, 145, 146, 4].

However, the identification of the physical mechanisms responsible for lasers degradation is difficult, due to the several factors that can contribute in limiting LDs lifetime.

Thanks to the effort of a number of groups working on LDs reliability, a few information on laser diodes degradation mechanism have been recently obtained, as summarized in the following:

- Degradation is manifested by the increase of threshold current density and the decrease of the laser gain as a consequence of Automatic Power Controlled (APC) or Automatic Current Controlled (ACC) stress [147]

- The degradation process was initially thought to be photo-activated [148], while Kummler et al. suggested that degradation can be related to current density [149]

- Tomiya et al. [7] demonstrated a very important feature of the nitride devices degradation, i.e. the lack of dislocation multiplication and dark line formation, which is characteristic for GaAs based devices

- Schoedl et al. [17] indicated the importance of the facet degradation for devices reliability, describing the important chemical activity of exposed GaN facets
- Takeya et al. [150] suggested that diffusion (probably Mg) may be responsible for the degradation, demonstrating a square root dependence with time of the degradation of laser devices
- Finally the measurements carried out by Marona et al. [151] indicated that the degradation of laser diodes occurs mostly by the increase of the threshold current due to creation of new non-radiative recombination centers and that the degradation follows a square-root law indicating the importance of diffusion processes.

Despite the important efforts that have been done to understand the mechanisms that limit LDs lifetime, from literature data it is not clear how the diffusion-related degradation process described in [7, 4, 151] depends on LDs operating conditions (operating temperature, optical field and injected current). In other words, it is not clear if this diffusion process is a purely thermal effect, or if operating current and/or the high photon density in the cavity can play a significant role in determining degradation kinetics.

Therefore, the aim of this chapter is to describe a complete analysis of the optical degradation of GaN-based LDs. By means of a wide set of stress tests carried out under different temperature, optical power and stress conditions, it is confirmed that degradation of LDs properties can be ascribed to a diffusion process. Furthermore it is demonstrated that

- degradation of the threshold current and of the sub-threshold optical power have similar kinetics, indicating that an increase of the non-radiative recombination rate is responsible for the degradation
- increasing stress temperature implies an increase of the degradation rate (even for the same optical power or current level)
- optical power (OP) level does not have a significant impact on degradation kinetics

- pure thermal stress (no bias applied to the junction) has only a minor impact on devices characteristics
- degradation rate has a nearly linear dependence on injected current

Degradation has been then attributed to an Electro-Thermally activated diffusion of impurities towards the active layer of the devices. This diffusion implies the generation of non-radiative paths, with subsequent decrease of the efficiency of the devices.

## 7.2 Analyzed devices and stress conditions

The analysis has been carried out on multi-quantum well laser diodes grown on GaN substrate by means of MOCVD. Devices vertical structure consists in a GaN buffer layer, an AlGaN cladding layer, an n-GaN guiding layer, a triple InGaN/GaN quantum-well structure, a p-AlGaN electron blocking layer, and a p-GaN contact layer. Average threshold current density and slope efficiency of the LDs were measured to be 3.2 $kA/cm^2$ (corresponding to an injected current of about 29 $mA$) and 1.6 $W/A$ respectively. A set of devices coming from the same wafer have been submitted to stress under different driving and temperature conditions.

In particular, we have aged the devices at

- fixed optical power level (65 mW CW), different temperatures (in the range 50-80 °C)
- fixed temperature level (70 °C), different optical powers (in the range 55-75 mW CW)
- fixed temperature level (180 °C), no bias,
- fixed temperature level (70 °C), different current levels (in the range 20-80 mA dc)

During stress, the case temperature of the LDs was kept constant by means of a Peltier-based temperature controlled holder: the used system has a 0.01 $°C$ resolution and a $\pm 0.1$ $°C$ accuracy, thus allowing for accurate control of LDs temperature. The junction-to-case thermal resistance was measured to be equal to 40 K/W: this

means that under typical adopted stress conditions (70 mA stress current, 70 $°C$ case temperature), junction self heating was limited to 15 $°C$ with respect to case temperature. For all the analyzed devices, stress duration was equal to 100 h.

During stress, at defined time intervals, we have measured the RT output power vs input current (L-I) characteristics of the devices, thus evaluating the degradation of the optical properties of the samples. Devices threshold current ($I_{th}$) has been evaluated by means of linear fitting of the L-I curves in the OP range 1-4 mW

For all the devices stress duration was equal to 100 h.

## 7.3 Results

### 7.3.1 Stress at fixed current level

Figure 7.1 shows the linear optical power vs injected current (L-I) curves measured (at 25 °C) before and after stress carried out at 70 mA, 70 °C on one LD. As can be noticed, stress induced the shift of the threshold current ($I_{th}$) toward higher values, without strong modifications of the slope efficiency of the devices. Furthermore, the semi-logarithmic L-I plots in Figure 7.2 show that stress induced the decrease of the emitted power of the devices also in the sub-threshold region (sub-threshold emission $OP_{sub}$).

Figure 7.3 shows the threshold current variation

$$\Delta I_{th} = \frac{I_{th}(t)}{I_{th}(0)} - 1 \tag{7.1}$$

as measured during stress at 70 mA dc, 70 °C on one aged LD. During stress the threshold current increased according to the square-root of stress time: the solid line represents a fit of the experimental data according to

$$\Delta I_{th} = I_0 + C\sqrt{t} \tag{7.2}$$

where $I_0$ is close to zero, and $C$ is a pre-factor that defines the degradation rate. As described in previous studies [145, 4, 151], this kind of dependence indicates that degradation is related to an impurity diffusion process. In Figure 7.3 we also plot the variation of the sub-threshold optical power ($OP_{sub}$) measured at 28 $mA$ (3.1 $kA/cm^2$),

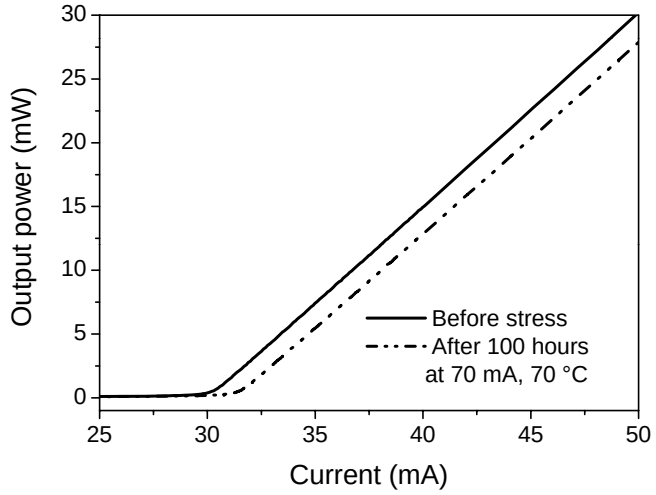



**Figure 7.1:** L-I Characteristics measured (at 25 °C) before and after stress at 70 mA CW, 70 °C (linear scale)

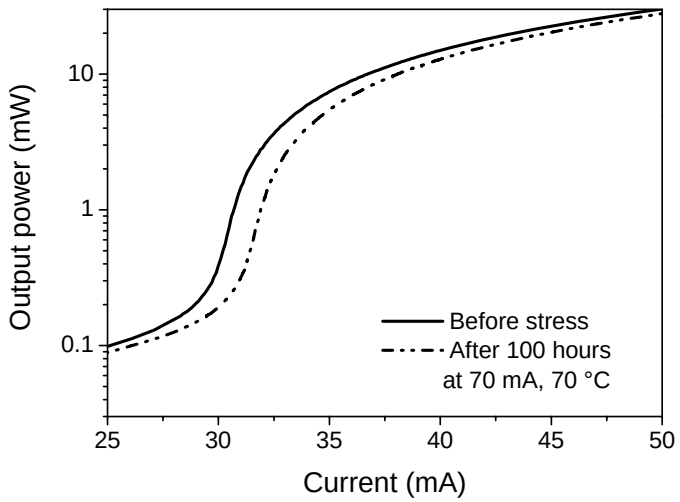



**Figure 7.2:** L-I Characteristics measured (at 25 °C) before and after stress at 70 mA CW, 70 °C (semi-logarithmic scale)

i.e. just below lasing threshold (that is about 29 $mA$ for the untreated device), during stress time: this parameter is plotted as

$$\Delta OP_{sub} = 1 - \frac{OP_{sub}(t)}{OP_{sub}(0)} \tag{7.3}$$

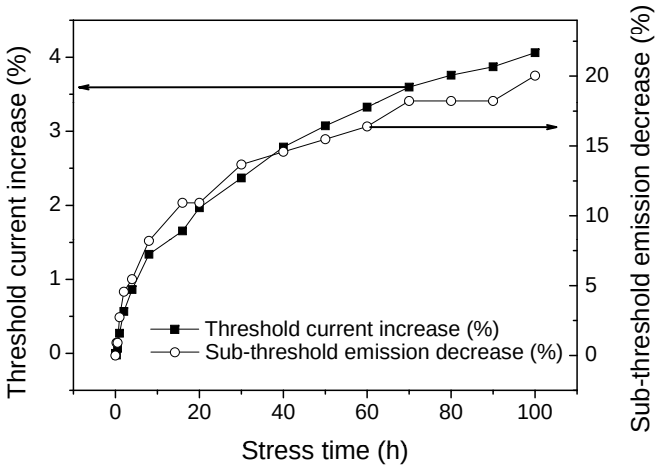



**Figure 7.3:** Threshold current increase and sub-threshold emission decrease measured on one LD during stress at 70 mA, 70 °C

As can be noticed, the threshold current increase and the sub-threshold emission decrease have similar kinetics, indicating a correlation.

A few consideration can be given considering the curves in Figure 7.3 and the basic Equations 7.4 and 7.5 that define LDs behavior at lasing threshold. Equation 7.4 indicates that the carriers recombination lifetime $\tau$ is determined by the balance between the non-radiative and radiative recombination rates ($A$ and $B$ respectively, see also [94]). In this equation, $N$ represents the carrier density in the active region. On the other hand, Equation 7.5 indicates that the threshold current $I_{th}$ is proportional to the ratio between threshold carrier density ($n_{th}$) and the carriers recombination lifetime [152].

$$\frac{1}{\tau} = A + BN \tag{7.4}$$

$$I_{th} \propto \frac{n_{th}}{\tau} = n_{th}\left(A + Bn_{th}\right) \tag{7.5}$$

Considering that:

- as described in [94, 152] both the sub-threshold optical power $OP_{sub}$ and the threshold current $I_{th}$ depend on the balance between radiative and non-radiative recombination events, and are therefore related to the carriers recombination lifetime;
- the non-radiative recombination coefficient $A$ is related to the defectivity of the active layer [94], that is supposed to increase during stress due to an impurity diffusion process [7, 4, 151]
- no change is expected after stress in the radiative recombination rate $B$

our results support the hypothesis that both $I_{th}$ and $OP_{sub}$ variation can be attributed to an impurity diffusion process [7, 4, 151], that implies the increase of the non-radiative recombination rate A, with corresponding decrease of the radiative efficiency of the devices and increase of their threshold current.

### 7.3.2 Stress at fixed OP levels, different temperatures

In order to better characterize the properties of this diffusion process, we have analyzed the dependence of stress kinetics on the operating conditions (temperature, output power and current). Stress tests carried out at fixed OP level (65 mW CW) and different temperatures indicate that degradation rate increases with increasing temperature, as highlighted by the $I_{th}$ curves reported in Figure 7.4. In Figure 7.6 and in Table 7.1 we report the variation of degradation rate $C$ (see Equation 7.2) with increasing stress temperature, for stress at constant OP level. Increasing stress temperature from 50 °C to 80 °C implies an increase of the degradation rate of a factor 2. Therefore, temperature has a significant role in defining degradation kinetics: for this, a strong increase of stress temperature is expected to speed up degradation kinetics. The log-log $I_{th}$ degradation curves of the devices aged at different temperatures have similar slopes, close to 0.5 (Figure 7.5), i.e. $I_{th}$ increases with the

square-root of stress time at all the analyzed stress temperatures. As mentioned before, this kind of kinetic is typical for diffusion-related degradation processes: this result supports the hypothesis that degradation is ascribable to the diffusion of an impurity that can generate non-radiative paths, thus changing the sub-threshold emission and $I_{th}$ value [7, 4, 151].

As a result of this set of tests we can state that temperature has a significant role in defining degradation kinetics: for this, a strong increase of stress temperature is expected to speed up degradation kinetics.

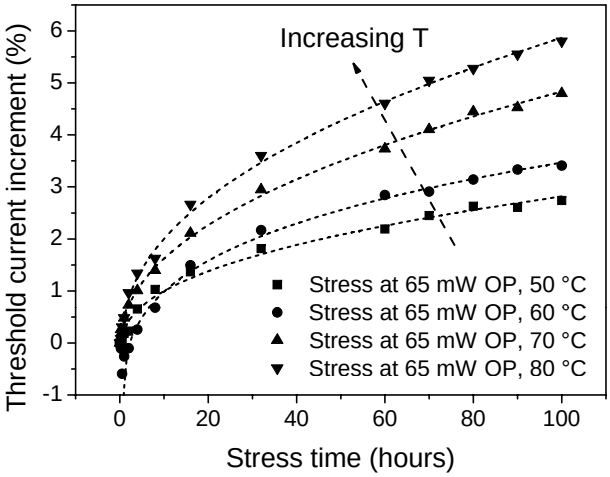



**Figure 7.4:** Threshold current increase measured on the samples aged at fixed optical power level (65 mW APC) and different temperatures in the range 50-80 °C. Dashed lines are square-root fitting curves.

### 7.3.3 Stress at high temperature levels

In order to understand if the diffusion process responsible for degradation is activated only by temperature, we have carried out stress tests at 180 °C, with no bias applied to the junction. Results indicate that temperature alone (even if high) does not induce significant degradation of LDs devices characteristics: stress at 180 °C for 100 h was found to induce only a 1.2 % $I_{th}$ increase (see Figure 7.7), that is small compared to the $I_{th}$ increase detected during stress at 65 mW, 70 °C.

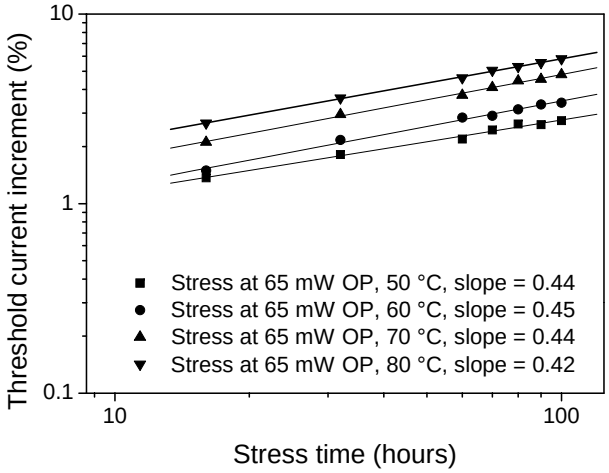



**Figure 7.5:** Threshold current increase measured on the samples aged at fixed optical power level (65 mW) and different temperatures in the range 50-80 °C (log-log scale)

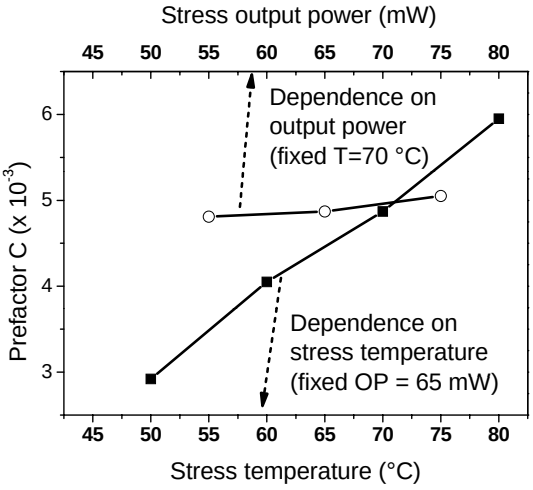



**Figure 7.6:** Empty circles: variation of the prefactor $C$ with increasing optical power level (stress at constant Temperature=70 °C). Filled squares: variation of the prefactor with increasing temperature (constant OP= 65 mW)

| Stress temperature (OP=65 mW CW) | Prefactor C ($h^{-0.5}$) | CW OP level (T=70 °C) | Prefactor C ($h^{-0.5}$) |
|---|---|---|---|
| 50 °C | $2.92 \cdot 10^{-3}$ | 55 $mW$ | $4.81 \cdot 10^{-3}$ |
| 60 °C | $4.05 \cdot 10^{-3}$ | 65 $mW$ | $4.87 \cdot 10^{-3}$ |
| 70 °C | $4.87 \cdot 10^{-3}$ | 75 $mW$ | $5.05 \cdot 10^{-3}$ |
| 80 °C | $5.95 \cdot 10^{-3}$ | - | - |

**Table 7.1:** Variation of the pre-factor C with increasing optical power level (for stress at constant temperature=70 °C) and with increasing temperature (for stress at constant OP= 65 mW)

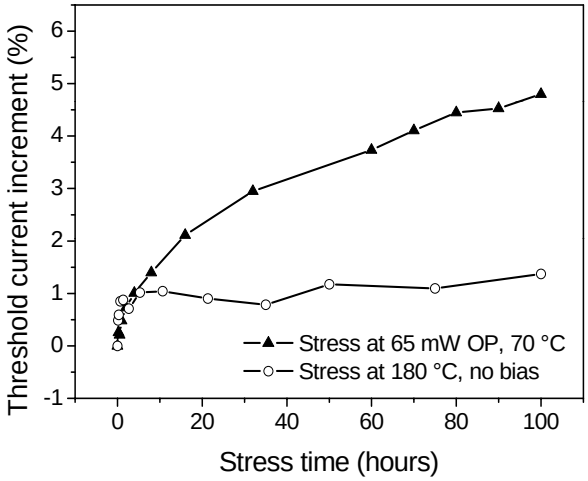



**Figure 7.7:** Threshold current increase measured on one sample aged at 65 mW, 70 °C and on one sample aged at 180 °C, no bias

### 7.3.4 Stress at different OP levels, fixed temperature

Therefore, the diffusion process responsible for LDs degradation is not purely thermally activated. Transport of carriers and/or high optical field are expected to play a significant role in degradation process. For this reason, we have analyzed the impact of stress at different optical power and different current levels on degradation kinetics, at fixed temperature (70 °C).

Results (Figure 7.8) showed that a variation of the stress OP level in the range 55-75 mW does not imply a significant change of the degradation rate, for the same stress temperature level (70 °C). The fact that the intensity of the optical field does not strongly influence degradation kinetics is expressed also by Figure 7.6 and Table 7.1, that reports the variation of the degradation rate $C$ with increasing stress OP level: as can be noticed, increasing optical power from 55 mW to 75 mW implied only a 5 % increase of the degradation rate.

Results showed that increasing stress OP level did not imply a significant increase of the degradation rate. The variation of $C$ due to an increase of optical power from 55 to 75 mW (+5 %) was significantly lower than what determined by an increase of operating temperature from 50 to 80 °C (x 2 for stress at 65 mW APC). This is described by Figure 7.8, that reports the threshold current increase measured

- on the samples aged at constant OP level (65 mW), different temperatures (50-80 °C)
- on the samples aged at fixed temperature (70 °C), different OP levels (55-75 mW)

As stated above, the square-root dependence of $I_{th}$ increase support the hypothesis that devices degradation is related to a diffusion process [7, 4, 151]. This process is not purely thermally-activated, since it is necessary to apply bias to the devices to have a significant degradation. Furthermore, we have shown here that increasing junction temperature is an effective way to accelerate LDs degradation, even for the same optical power level. On the other hand, pure thermal stress (high temperatures, no bias applied to the lasers) was found to induce only a slight increase of threshold current. Therefore, optical degradation of the LDs can be attributed to an electro-thermally activated diffusion process.

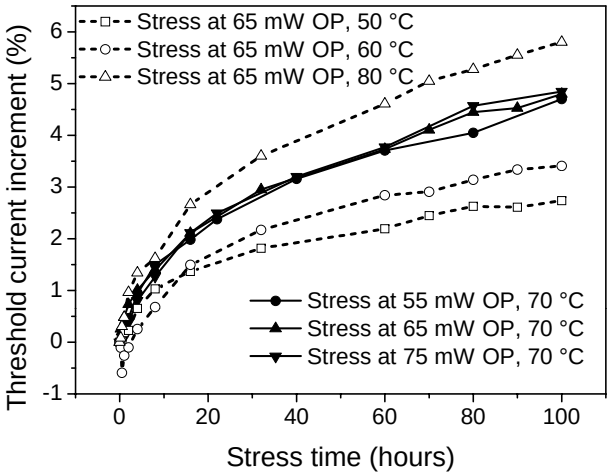



**Figure 7.8:** Solid lines: threshold current increase measured on samples aged at different OP levels (in the range 55-75 mW) and 70 °C. Dashed lines: threshold current increase measured on samples aged at different temperature levels (50-80 °C), at 65 mW OP.

### 7.3.5 Stress at different current levels, fixed temperature

In order to understand which is the role of carrier flow in determining degradation kinetics, and which is the relation between stress current and degradation rate, we have carried out stress tests at fixed temperature level (70 °C) and several input current levels.

In particular, Figure 7.9 shows the threshold current increase measured on the devices aged at different current levels, for the same temperature (70 °C). The increase of stress current implies the increase of the degradation rate, as shown also in Figure 7.10. In the same figure, we also show the optical power vs input current (L-I) curve measured on one untreated sample at the stress temperature (70 °C). It is easily recognizable that at 70 °C (stress temperature) the lasing threshold current is 40 mA.

The degradation rate vs stress current curve in Figure 7.10 shows that

- degradation takes place also below lasing threshold, i.e. without the influence of a strong optical field;
- current plays a significant role in devices degradation, since an increase of stress current (from 20 to 80 mA) implies a significant increase of the degradation rate

(+250 %).

The slope of the degradation rate $C$ vs stress current curve slightly decreases as stress current is increased above 40 mA, i.e. above the lasing threshold. This effect can be related to the fact that *(i)* above threshold, an important fraction of the total dissipated power is converted into light, and therefore self heating (and the corresponding impact on degradation) is reduced; *(ii)* above threshold, degradation rate can be reduced due to the saturation of the carriers density; *(iii)* degradation is activated by native defects and therefore, at high current levels, degradation saturates due to the limited concentration of already existing defect. Further investigation is in progress to distinguish between these hypothesis.

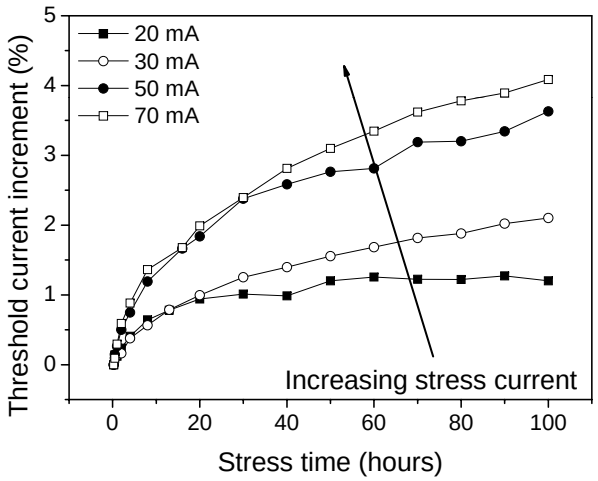



**Figure 7.9:** Threshold current increase measured on samples aged at different current levels (in the range 20-80 mA) at 70 °C

## 7.4 Discussion and conclusions

In this chapter, we have described an extensive analysis of the degradation of InGaN-based laser diodes under different operating conditions. We have shown that constant current and constant optical power stress determine the increase of the threshold current and the decrease of the sub-threshold emission of the devices. Since

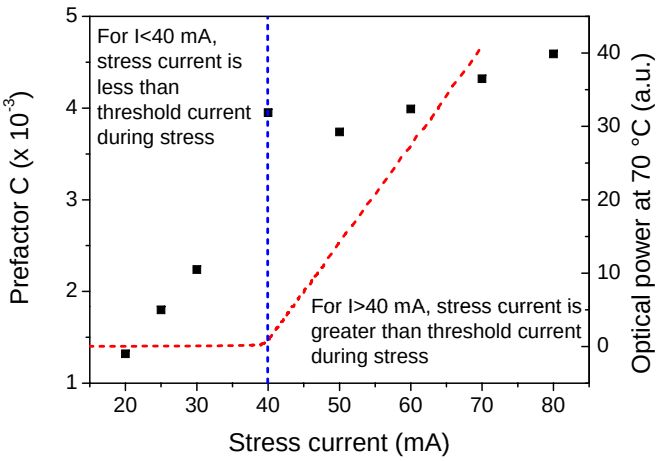



**Figure 7.10:** Scatter: Dependence of degradation rate on stress current. Dotted curve: L-I curve measured on one untreated LD at the stress temperature (70 °C)

- the sub-threshold emission decrease can be due to the increase of the non-radiative recombination rate in the active layer [94]
- the variation of these two parameters have similar kinetics (see Figure 7.3)
- both the parameters depend on the balance between radiative and non-radiative recombination events [94, 152]

we attribute also the threshold current increase to the generation of non-radiative paths in the active layer of the devices.

The fact that the threshold current and the sub-threshold emission vary with the square-root of stress time support the hypothesis that the degradation is related to a diffusion process, as previously reported. Furthermore, we have analyzed the dependence of the degradation kinetics on the LDs operating conditions: we have found that increasing stress temperature implies an increase of the degradation rate, while variations of the stress optical power level do not significantly affect degradation kinetics (for a given operating temperature). Furthermore, pure thermal stress (no bias applied to the junction) has been found to have only a minor impact on devices characteristics. Tests carried out at different stress current levels and same temperature

showed that *(i)* degradation takes place also under lasing threshold and *(ii)* degradation rate has a significant dependence on stress current.

Therefore, as a result of this work, we can state that the mechanism responsible for the degradation is an Electro-Thermally activated diffusion of impurities towards the active layer of the devices. This diffusion can increase the non-radiative recombination rate, thus decreasing the optical efficiency of the devices. Further analysis is in progress, in order to identify which is the impurity involved in diffusion process, and provide a technological feedback to improve the properties of the devices.

# Chapter 8

# Conclusions

With this work we have presented a detailed analysis of the reliability of GaN-based optoelectronic devices. The analysis has been carried out in cooperation with devices manufacturers, and has been aimed at identifying the physical mechanisms and the failure modes related with the degradation of the different parts of the devices structure. In particular, by means of specific stress tests, we have analyzed *(i)* the degradation of the heterostructure and active layer properties, *(ii)* the degradation of the p-side contact and semiconductor layer, *(iii)* the role of passivation in determining devices degradation, *(iv)* the degradation of the package and phosphorous layer, and *(v)* the degradation of the optical properties of the active region of InGaN-based laser diodes. The information on the physical mechanisms responsible for degradation have been used as a feedback for devices manufacturers, for the improvement of the technological processes. Furthermore, we have analyzed the important role of temperature in limiting devices reliability. The extrapolation of the Arrhenius plots under accelerated stress conditions provided important information for the estimation of devices useful lifetime at nominal temperature levels.

The most important achievements are summarized in this section.

## Degradation of the heterostructure properties

**Low current density stress can induce the degradation of the properties of the active layer of the LEDs, mostly due to the increase of the non-radiative recombination rate**. This effect has been studied by analyzing the behavior of

LED devices with multi-quantum well structure submitted to dc bias stress. Stress current level was limited, in order to avoid that self-heating effects could corrupt the results: in this way we have analyzed the only degradation effects related to carriers flowing across the heterostructure. Results have shown that low current density stress can induce the decrease of the efficiency of the devices, and that this effect is more prominent for low measuring current levels. This fact indicates that for this kind of stress, degradation is mostly related to the generation of non-radiative recombination centers, with subsequent decrease of the radiative efficiency. At high measuring current levels, these centres are saturated, and their effect on overall LEDs efficiency is limited. The analysis of the current-voltage curves showed that the forward-bias characteristics of the devices do not significantly degrade as a consequence of stress, thus indicating that contact and semiconductor resistivity are not altered by the flow of carriers across the device. On the other hand, constant current stress was found to induce the increase of the reverse current of the devices, whose magnitude slightly differed for each of the analyzed LEDs: this fact suggests that this process is due to mechanisms depending on samples quality, such as generation/propagation of threading dislocations in the active region and/or modifications of the surface states at the mesa sidewalls.

Capacitance-voltage characterization was found to be an excellent tool for the analysis of the degradation of the devices. In particular, we have demonstrated that current stress can induce an increase of the ACD profiles, strongly related to the efficiency decrease. This effect was found to be mostly localized in the region close to the active layer of the LEDs, thus indicating that stress at low current levels induced charge instabilities in the MQW region, possibly related to the generation/modification of defect-related levels.

This hypothesis has been explored by means of DLTS characterization, that confirmed that low-current stress can induce strong variations of the properties of levels close to the active layer. Degradation was found to be mostly related to the modification of the properties of one level with activation energy in the range 170-180 meV. The detected modifications are supposed to be related to the generation of non-radiative defects, responsible for the efficiency loss detected after stress.

At high measuring current levels, these paths can be saturated by the important flow of carriers injected in the heterojunction. For this reason, at high current levels

the effect of stress are less marked, as indicated by EL and CL characterization. The fact that no-significant spectral modification has been detected as a consequence of dc current stress confirms the non-radiative nature of the physical degradation process. The fact that degradation mostly interested the active layer has been confirmed by the photocurrent measurements carried out during stress: we have demonstrated that stress had a stronger impact on the properties of the QW-related PC band with respect to NBE emission, providing a further evidence of the fact that carrier flow can strongly limit the properties of the active layer in the MQW region.

## Role of passivation in limiting LEDs reliability

**The presence of a PECVD-SiN passivation layer can strongly limit the high-temperature reliability of GaN-based LEDs.** This fact has been demonstrated by means of a detailed characterization of the electro-optical behavior of GaN LEDs submitted to high temperature storage. LEDs with and without passivation have been used for this analysis. We have shown that the high temperature stress of LEDs with PECVD passivation can induce a nearly-exponential optical power decrease, well related to the degradation of the series resistance and ideality factor of the samples. On the other hand, the samples without passivation did not show any significant degradation after high temperature treatment.

Degradation process has been found to be thermally activated: a detailed analysis of the stress kinetics at several temperature levels indicated that the activation energy of the stress process is 1.3 eV. This information constitutes the starting point for the extrapolation of the acceleration factors and for forcasting devices lifetime.

Degradation has been attributed to the interaction between the passivation layer and the p-side surface of the LEDs. It has been supposed that at high temperature levels the hydrogen contained in the PECVD passivation can interact with the acceptor dopant, thus reducing the overall effective acceptor concentration. This implies the worsening of the properties of the semiconductor and contact at the p-side of the diodes, thus inducing the worsening of current and emission spreading at devices surface, and the subsequent optical power decrease.

This degradation process has been found to be reversible, after passivation removal

and subsequent annealing. A proof of the role of hydrogen in the degradation process has been given by storage tests carried out in different atmospheres: in particular, annealing in forming gas was found to induce the same degradation of the electrical and optical parameters detected during stress of samples with PECVD passivation.

Finally, relevant data indicating that a sputtered SiN passivation layer can be an effective alternative to PECVD passivation in terms of devices high-temperature reliability have been presented. Measurements results indicate that sputter passivation deposition can preserve both the optical and electrical performance of the devices over several hundreds of hours of high temperature storage.

## Analysis of the degradation of ohmic contacts on p-GaN

**High temperature stress can determine the degradation of ohmic contacts on p-GaN, with subsequent increase of operating voltage and worsening of the current and emission spreading.** The degradation of contact layers on p-GaN has been analyzed in detail by means of the TLM method. We have demonstrated that thermal storage can induce strong modifications of the I-V characteristics of the TLMs: in particular a rectifying behaviour and a slight series resistance increase were detected as a consequence of storage. Degradation process was found to be reversible, after passivation removal and subsequent annealing.

Degradation has been attributed to the interaction between p-type semiconductor material and the PECVD passivation: we have shown that the most important result of this interaction is a worsening of the ohmic properties of the metal/semiconductor contact, while only a slight increase of semiconductor sheet resistance has been detected after stress.

The comparison between the data on TLMs and LEDs degradation has provided important information on the localization of the damage introduced by thermal storage on the characteristics of LEDs, indicating that two critical parts of LED structure must be improved to obtain reliable behavior at high temperature levels: *(i)* the metal/semiconductor contact and *(ii)* the passivation layer. In particular, the analysis

carried out within this work has demonstrated that the use of an hydrogen-free passivation layer can significantly improve LEDs reliability at high temperature levels. We have therefore proposed and demonstrated sputtered passivation as a more stable alternative to the conventionally adopted PECVD passivation for devices to be used in high temperature environment.

## Reliability of high power LEDs: role of package degradation

**The performance and the reliability of high power LEDs are significantly affected by the high temperatures reached by the devices during operation. For this reason, a detailed thermal characterization and reliability analysis are necessary for the understanding and the improvement of the high-temperature stability of GaN-based power LEDs.**

With this aim, we have described the thermal and optical behavior of high power LEDs and the dependence of the main parameters on the driving strategy. In particular, we have compared the use of dc and pulsed driving: all the used driving waveforms had the same average current level, in order to obtain consistent comparison. It has been shown that the use of pulsed waveforms implies a stronger self-heating of the devices, with respect to dc driving. Furthermore, we have shown that the use of square-wave driving implies a lower devices efficiency with respect to dc case, even for the same average current value. For this reason, we state here that driving power LEDs with pulsed waveforms can be an alternative to dc bias, but only if low duty cycle values are avoided, because they can imply a strong reduction of devices efficiency with respect to dc case (for the same average current level).

High-temperature stress of high power LEDs has been also carried out, with the aim of evaluating the role of temperature in determining devices degradation, as well as the technological weaknesses that limit the reliability of the LEDs at high temperatures. By means of a combined optical and microscopical analysis we have demonstrated that the thermal degradation of the analyzed power LEDs is strongly related to the darkening of the package of the devices, due to the high temperatures reached during stress. This

mechanism reduces the reflectivity of the package, thus implying *(i)* the decrease of the optical power emitted by the devices and *(ii)* the decrease of the blue-to-yellow conversion efficiency with subsequent degradation of the chromatic properties of the LEDs. On the other hand, we have shown that the high temperature degradation of power LEDs is not strongly related to the worsening of the properties of the contacts and of the blue semiconductor chip.

## Degradation of InGaN-based laser diodes

**Constant current and constant OP stress can induce the increase of the threshold current of InGaN-based laser diodes, that varies according to the square-root of stress time.**

Furthermore, threshold current increase and sub-threshold emission decrease were found to have similar kinetics: these two facts indicate that both mechanisms are related to the increase of the non-radiative recombination rate, caused by the diffusion of one impurity towards the MQW region.

Stress tests carried out at different temperature levels (same stress OP level) indicated that temperature can accelerate degradation kinetics. However, pure thermal storage tests (high temperature, no applied bias) implied only a slight degradation. The two last results indicate that the diffusion process responsible for degradation is activated by both temperature and carrier flow: furthermore, the entity of the optical field was found to have only a slight impact on degradation kinetics. Therefore, degradation has been attributed to an electro-thermally activated impurity diffusion process. A confirmation of this interpretation has been given by the results of stress tests carried out at different driving current levels: it has been shown that degradation rate has a significant dependence on driving current, and that degradation takes place also below lasing threshold, therefore confirming the important role of carriers flow in determining devices degradation.

# Final summary

The results summarized above indicate that by means of specific experiments on suitable test structures it is possible to separately analyze different physical mechanisms that limit the reliability of GaN-based optoelectronic devices.

In particular.

- It has been demonstrated that low current density stress can affect the properties of the active layer, without significantly degrading the characteristics of the contacts and devices package. A combined electrical and optical characterization of the devices has been demonstrated to be an important tool for the analysis of the degradation of the heterostructure and active region properties taking place as a consequence of stress.

- High temperature storage tests can significantly affect the stability of contact layers, as well as the properties of p-type gallium nitride layers. The use of specific test structures (e.g. TLMs, passivated and un-passivated LEDs) provides important information on the worsening of the properties of the semiconductor and contact layers during thermal treatment, and on the localization of the degraded regions.

- Combined electrical, optical and microscopical analysis can be used for the evaluation of the different processes determining the degradation of high power LEDs. In particular, information on the degradation of the semiconductor chip, the contact layers, and the package/phosphors system have been obtained by means of this set of techniques. An extensive characterization of the degradation kinetics under different stress temperature levels finally provided important information on the activation energy of the degradation process. These information can be used for the estimation of devices lifetime under nominal operating conditions.

- By means of a specific set of ageing tests it is possible to evaluate the dependence of InGaN-LDs degradation kinetics on the operating conditions. In particular, we have shown that constant current and constant optical power stress can induce the increase of the threshold current of the laser diodes, according to the square-root

of time. Devices degradation has been attributed to the diffusion of one impurity towards the active layer of the devices, with subsequent decrease of the radiative efficiency and increase of the threshold current. Degradation rate was found to significantly depend on current and temperature level, and not on optical field. Devices degradation has been therefore attributed to an Electro-Thermally activated impurity diffusion process.

The results on technological weaknesses obtained within this work have been used as a feedback to the manufacturers, for the development of LEDs and lasers with improved reliability. Further work is in progress, in order to analyze with more detail the dependence of degradation rate on the different degradation driving forces, and to develop models for lifetime prediction.

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