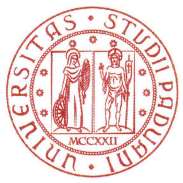

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From GaAs to GaN technology: study of limits and reliability of High Electron Mobility Transistors

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UNIVERSITA' DI PADOVA

FACOLTA' DI INGEGNERIA

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TESI DI DOTTORATO

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DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE

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Abstract

High Electron Mobility Transistors (HEMTs) are finding wide applications in many areas, including microwave power amplifiers, radars, communication and conversion fields. The high mobility, due to the reduction of scattering phenomena, and the high carrier density, due to the confinement of electrons in the so called 2DEG, allowed the achievement of a high current density and low channel resistance, thus making these devices very suitable for high frequency applications.

HEMTs are usually based on III-V materials, especially GaAs and GaN technology, as a consequence of their electrical properties. In the last years gallium nitride has become one of the most interesting and suitable material. The high direct energy gap led to better performances especially in optoelectronic devices such as Light emitting diodes, lasers and detectors. Furthermore, the high carrier saturation velocity and the high mobility demonstrated high performances in devices aimed at high frequency, such as HEMTs. Finally the high electric field breakdown and Johnson's figure of merit suggest its use for devices with high power requirements, thus overcoming in many areas gallium arsenide technology. For many applications, such as MMIC (monolithic microwave integrated circuits) structures, gallium arsenide is preferable, mainly as a consequence of excellent charge transport properties and low loss at microwave and millimetre-wave frequencies. Furthermore, especially for commercial purposes, gallium arsenide is more used due to the well-established technology.

Although the significant intrinsic properties, both gallium arsenide and gallium nitride HEMT technology are still affected by reliability issues which limit their performances in common applications. The purpose of this thesis is to study reliability topics which limit HEMT technology on the basis of materials used, namely GaAs, GaN, InAlN, in order to define corresponding limits and performances. With the aim of providing for a more complete perspective the analysis will focus not only on discrete transistors but it will be extended also on complete structures such as power amplifiers.

Within this work we present a detailed study of two main degradation mechanisms which still affect GaAs technology and limit its performances both in discrete pHEMTs and in commercial complete structures: thermal degradation and electrostatic discharge failure. Thermal degradation analysis has been firstly studied on discrete structures, namely

pseudomorphic HEMTs. A first purpose is to define main failure mechanisms and modes by means of a long term thermal stress with no bias applied. Several analysis (DC, pulsed, end resistances and barrier height evaluation) has been proposed to monitor devices behaviour. Degradation appears to be non-monotonic, i.e. drain current first decreases, then increases again, following the corresponding shifts in the threshold voltage. Although the initial decrease of drain current could be attributed to gate metal interdiffusion, or "gate sinking", leading to a positive shift of threshold voltage, it is accompanied by a variation of the maximum value of transconductance and an increase of end resistances, that suggest a concurrent degradation of ohmic contacts. A third mechanism, represented by the Schottky barrier height, counteracts the effect of gate interdiffusion and eventually prevails, leading to an opposite shift of the threshold voltage.

Devices used for high power applications can reach high junction temperatures as a consequence of the power dissipation, demonstrating the importance of accurately defining the thermal resistance, i.e. the channel temperature variation as a function of power dissipated. A second purpose of this chapter is to provide for a detailed description of different techniques (namely DC, pulsed and infrared thermal camera) to estimate channel temperature of HEMTs and to present a critical comparison among them. Differently from DC and pulsed evaluation, analysis with IR thermal camera strongly underestimates the results. With the aim of understanding the impact of inaccuracies on a high frequency application the analysis has been extended to a four stage MMIC power amplifier. The strong underestimation of IR method has been confirmed; furthermore the thermal interaction among different stages and its impact on the structure has been studied. By means of a deep analysis of thermal resistance a HTOL test has been proposed on power amplifiers, submitting the devices both to an electrical and thermal stress and confirming that no significant effect is noticed if a junction temperature lower or equal to 250°C is reached. Comparison between V_{TH} shift in HTOL and thermal stress suggests that the junction temperature has been slightly underestimated.

Electrostatic discharge robustness has been studied on a four stage MMIC power amplifier based on GaAs pHEMT technology used in commercial point to point microwave systems. The structure is characterized by a ESD protection circuit mainly defined by Schottky diodes protection structures at the gate terminals and resonant circuit protection structure at the RF input and output pads. Robustness has been analysed with a 100ns TDR-TLP. Results have been confirmed with HBM and MM tests. No failures are observed in the RF-IN, RF-OUT and Drain connections vs. GND up to ±2 kV and ±200 V HBM and MM respectively. RF pads failed with TLP analysis at about 6.5-7A, resulting in an open circuit at the inductor and a short at the capacitor of the resonant structure. Gate connections fail in correspondence of the negative HBM pre-charge value starting from -1.0 kV; MM stresses lead to the failure of the Gate connections from -50 V. Failures are due to the damage of anti-parallel Schottky diodes acting

as ESD protection structures. The auxiliary connections reveal to be the most sensitive I/Os of the entire PA, failing at 250 V and 25 V, respectively HBM and MM, due to the failure of integrated resistors.

A second part of the thesis mainly focuses on AlGaN/GaN devices. One of the main aspects which limit devices RF and power performances is the so-called current collapse and trapping effects. Therefore a detailed analysis has been proposed on devices characterized by a different iron doping in the buffer layer aimed at preventing parasitic effects and punch through phenomenon. The aim is to define a correlation between the trapping behaviour and iron doping in the buffer layer. A further purpose is to study the correlation between several degradation phenomena when a reliability stress is imposed, both in terms of DC characterization, trapping effects and light emission analysis. A comparison of the correlation between different degradation phenomena in devices with several iron doping quantities is finally proposed. Results are consistent with further investigations reported in literature which correlate the use of iron doping to a trap level with activation energy of 0.57-0.7eV.

The analysis firstly demonstrates that iron doping determines a measurable current collapse, which is related to the presence of a trap (T1) located in the buffer with time constant of 3.2ms at T=40°C. Trapping location is consistent with the amplitude significant increase with Fe-concentration in the buffer. Furthermore trap T1 reveals a lower activation energy in devices with no iron doping. The amplitude of trap T1 in devices with different structures and comparison with works reported in literature suggest that the trap is due to an intrinsic defect in the buffer layer characteristic of GaN, although its concentration strongly depends on buffer doping quantity. Results of current transients with different filling pulses applied suggest that trapping is due to line defects or point defects clustering around dislocations. A second trap, T2, is detected. According to comparison of devices with different iron doping and comparison with $g_m(f)$ analysis we can suppose that T2, characterized by a time constant of 0.25s at T=40°C, is probably located in the AlGaN layer.

Results of an electrical stress applied to the gate terminal of Fe doped devices indicate that the main consequences of the stress experiments are (i) an increase in the leakage gate current, which is strongly correlated to light emission and – beyond the critical voltage – to an increase in the current collapse and (ii) the increase in the transient signal associated with the pre-existing trap levels, without the generation of new traps. Discussion about different results related to the Fe doping buffer layer demonstrates that, when submitted to step-stress, all the devices show a significant and permanent increase in gate leakage current. Furthermore stress induces also an increase in current collapse, which is not correlated to the generation of new trap levels but originates from the increase in the signal associated with the pre-existing trap levels T1 and T2. The change in the signal of T_2 (which is supposed to be located in the AlGaN barrier) may be due to an increase in the concentration of a defect (T_2); the change of T1,

(probably located in the buffer layer) can be explained by the generation of defect-related conductive paths between the gate and the channel which enhance transfer electrons toward the trap states.

In the last part new materials to improve GaN technology performances are studied. InAlN/GaN structures are becoming very important as a consequence of the higher carrier density in the 2DEG and the possible achievement of a lattice matched structure, thus significantly improving device electrical and thermal stability. Further improvements, especially at the contacts, will be presented within this thesis. A first analysis consists of the use of a different material for the Schottky gate contact. A comparison of InAlN/GaN HEMTs with analogous structure but different gate, namely Mo/Au and Ni/Pt/Au, is studied. Despite no significant variation is noticed during DC analysis, pulsed evaluation demonstrates that the use of a Mo/Au gate contact leads to an improvement of trapping characteristics, mainly due to the process used for contact deposition. By means of a three terminals step stress it is finally proved that Mo/Au does not significantly affect device stability.

A second analysis consists of the definition of a recess before the deposition of ohmic contacts to reduce parasitic resistances. The comparison is proposed for two different wafer, characterized by a similar but not analogous structure and different Carbon doping quantity to avoid parasitic leakage current. DC analysis shows that a significant variation is noticed in I_{DSS} value, showing that a lower value corresponds to structures with recess at the ohmic contacts. This aspect is mainly due to the fact that a lower on resistance measured in linear zone is not obtained. Pulsed analysis states a high current collapse value with no significant correlation with device structure or presence of recess at the ohmic contacts. Drain current transient reveals two main traps, labelled T1 and T2. Activation energy, differently from the cross section value, is not influenced by device structure or by recess at the ohmic contacs. On the basis of drain current transients, $g_m(f)$ analysis and previous works reported in literature we can speculate that trap T2 is located in the buffer layer, differently from trap T1 which is probably in the AlGaN layer. Filling time measurements indicate that both the traps are mainly due to line defects.

Sommario

High Electron Mobility Transistors (HEMTs) sono utilizzati in molte applicazioni, tra le quali microwave power amplifiers, radars, applicazioni per telecomunicazioni e potenza. L'alta mobilità, dettata dalla riduzione dei fenomeni di scattering, e l'alta densità di portatori, dettata dal confinamento degli elettroni in una buca quantica triangolare (2DEG), hanno permesso il raggiungimento sia di un'alta densità di corrente, sia di una bassa resistenza di canale, rendendo questi dispositivi particolarmente indicati per applicazioni che richiedono alta frequenza.

Gli HEMT sono in genere composti da materiali III-V, nello specifico arseniuro di gallio (GaAs) e in nitruro di gallio (GaN), come conseguenza delle loro proprietà a livello elettrico. Negli ultimi anni il nitruro di gallio è diventato uno tra i materiali più interessanti e utilizzati. L'alto energy gap diretto permette di raggiungere prestazioni molto migliori in particolare nei dispositivi optoelettronici, come Light emitting diodes, lasers and detectors. Inoltre l'alta velocità di saturazione dei portatori e l'alta mobilità hanno condotto ad alte prestazioni anche in dispositivi che lavorano ad alte frequenze, come gli HEMT. Infine, l'alto valore di campo elettrico di breakdown e la Johnson's figure of merit ne permettono l'utilizzo in dispositivi per applicazioni di potenza, superando dunque in molti ambiti l'arseniuro di gallio. Tuttavia, per molte applicazioni, quali ad esempio strutture MMIC (monolithic microwave integrated circuits), si preferisce ricorrere all'arseniuro di gallio, principalmente per le eccellenti proprietà di trasporto di carica e le perdite minori a frequenze corrispondenti alle microonde. Inoltre, in particolare per scopi commerciali, l'arseniuro di gallio rimane un'ottima soluzione in quanto tecnologia molto stabile in termini di affidabilità.

Nonostante le significative proprietà intrinseche, gli HEMT sia in arseniuro di gallio sia in nitruro di gallio sono ancora caratterizzati da numerosi problemi in termini di affidabilità che limitano in modo significativo le loro prestazioni nella maggior parte delle applicazioni. Lo scopo di questa tesi è dunque di studiare alcuni aspetti peculiari che limitano la tecnologia HEMT. Si è voluto proporre un approccio basato sui materiali utilizzati, principalmente GaAs, GaN, InAlN, per poter definire limiti e prestazioni corrispondenti prestando particolare attenzione al materiale considerato. La scelta di voler proporre una prospettiva maggiormente

completa ha condotto a non focalizzare l'analisi solo su transistor HEMT discreti ma anche su strutture complete come amplificatori di potenza.

In questo lavoro si presenta uno studio dettagliato di due meccanismi di degrado che influenzano ancora la tecnologia in arseniuro di gallio, limitandone le prestazioni sia in dispositivi discreti che in strutture complete commerciali: degrado termico e guasti per scariche elettrostatiche. Il degrado termico è stato innanzitutto studiato su strutture discrete, ovvero su HEMT pseudomorfici. Un primo obiettivo consiste nel definire i principali meccanismi e modi di degrado in seguito ad uno stress termico accelerato senza polarizzazione. Per monitorare il comportamento dei dispositivi numerose analisi sono state proposte, ovvero caratterizzazione DC, impulsata, misura delle end resistances e calcolo dell'altezza di barriera. Durante lo stress il degrado sembra essere non monotono, in quanto la corrente di drain inizialmente cala per poi crescere nuovamente, in modo coerente con gli spostamenti corrispondenti della tensione di soglia. Nonostante la variazione iniziale di corrente si possa attribuire a interdiffusione metallurgica (gate sinking), dimostrata anche da uno shift positivo della tensione di soglia, tale fenomeno è accompagnato anche da un degrado ai contatti ohmici, come dimostrato dalla variazione del picco della transconduttanza e dall'aumento delle corrispondenti resistenze parassite (end resistances). Un terzo meccanismo, descritto dalla diminuzione dell'altezza di barriera del diodo schottky, produce un effetto opposto all'interdiffusione metallurgica, in taluni casi anche prevalendo e comportando uno shift negativo della tensione di soglia.

I dispositivi usati per applicazioni che richiedono alta potenza possono raggiungere significative temperature di giunzione come conseguenza della dissipazione in potenza, definendo così l'importanza di una corretta definizione della resistenza termica, i.e. la variazione della temperatura di giunzione in funzione della potenza dissipata. Il secondo obiettivo è dunque quello di fornire una descrizione dettagliata di diverse tecniche (DC, impulsata, infrarossi) per stimare la temperatura di canale in un HEMT e proporre, di conseguenza, un confronto tra di esse esplicitando anche i corrispondenti vantaggi e svantaggi. A differenza dell'analisi con misure DC o impulsate, l'analisi con camera a infrarossi sottostima i risultati. Per riuscire a comprendere l'effetto delle imprecisioni in un'applicazione ad alta frequenza l'analisi è stata estesa ad un amplificatore di potenza sviluppato con struttura MMIC. Si conferma la significativa sottostima del metodo infrarossi. È inoltre possibile definire il fenomeno d'interazione termica tra diversi stadi e la sua influenza nella struttura analizzata. Attraverso un'analisi dettagliata della resistenza termica è stato condotto un test HTOL sugli amplificatori di potenza, sottoponendo questi ultimi sia ad uno stress di tipo elettrico che di tipo termico e confermando il non significativo degrado quando una temperatura di giunzione inferiore a 250°C è imposta. Il confronto della variazione di tensione di soglia nel test HTOL e nel test puramente termico suggerisce che i valori di resistenza termica siano stati leggermente sottostimati.

La robustezza verso le scariche elettrostatiche è stata studiata in un amplificatore di potenza con struttura MMIC basato su una tecnologia in HEMT pseudomorfici in arseniuro di gallio, usato a livello commerciale per sistemi microonde point to point. La struttura è caratterizzata da un circuito di protezione ESD principalmente costituito da diodi Schottky in corrispondenza dei terminali di gate e circuiti risonanti agli ingressi RF. La robustezza è stata analizzata con un impulso TDR-TLP di 100ns. I risultati sono stati confermati sia da test HBM che da test MM. Non sono stati riportati guasti nelle connessioni RF e in corrispondenza dei terminali di drain fino ad una tensione di ±2 kV e ±200 V misurata rispettivamente in HBM e MM. I pad RF si rompono in corrispondenza di una corrente misurata con il TLP di 6.5-7A, risultando in un lato aperto in corrispondenza dell'induttore e in un corto circuito in corrispondenza del condensatore, entrambi appartenenti al circuito risonante di protezione. Le connessioni di gate degradano quando una tensione HBM negativa di precarica di -1kV è applicata; risultati coerenti sono riportati dalla misura MM, dimostrando degrado ad una tensione negativa di precarica pari a -75V. Il guasto è riscontrato in corrispondenza dei diodi Schottky posti in anti parallelo come struttura di protezione ESD. Le connessioni ausiliarie per incrementare le prestazioni del dynamic range risultano essere le più sensibili, con una tensione di rottura pari a ±500V e ±50V misurate rispettivamente in HBM e MM, in seguito alla rottura di resistori integrati.

La seconda parte della tesi discute i meccanismi di trapping in dispositivi AlGaN/GaN. I fenomeni di trapping, e il conseguente current collapse, risultano essere tra gli aspetti che maggiormente limitano le prestazioni RF e di potenza nei dispositivi HEMT. L'analisi è stata effettuata su dispositivi con un differente drogaggio intenzionale di Ferro nel buffer layer. Tale drogaggio è in genere utilizzato per limitare i fenomeni parassiti e di punch through. Lo scopo primo dell'analisi è definire una correlazione tra i meccanismi di trapping e l'entità di drograggio nel buffer layer. In secondo luogo si è voluto studiare e proporre una correlazione tra differenti fenomeni di degrado nel momento in cui il dispositivo è sottoposto ad uno stress di affidabilità, in termini di caratterizzazione DC, effetti di trapping e analisi di elettroluminescenza. Un confronto di tale correlazione in dispositivi con differente quantità di ferro nel buffer layer è infine proposta. I risultati ottenuti sono coerenti con studi proposti in letteratura, che correlano l'uso di drogaggio in Ferro con una trappola con energia di attivazione pari a 0.57-0.7eV.

L'analisi dimostra innanzitutto che il drogaggio in ferro determina un significativo current collapse, correlato con la presenza di una trappola (T1) presumibilmente localizzata nel buffer layer e caratterizzata da una costante di tempo pari a 3.2ms a T=40°C. La posizione della trappola è coerente con l'aumento dell'ampiezza corrispondente al variare della concentrazione di ferro nel buffer. Inoltre la trappola T1 mostra un'attivazione termica molto inferiore (0.2eV) nei dispositivi senza buffer drogato. L'ampiezza della trappola T1 in dispositivi con diversa

struttura e il confronto con lavoro precedentemente esposti in letteratura suggerisce che la trappola sia dovuta ad un difetto intrinseco nel buffer layer tipico del GaN; tuttavia la sua concentrazione varia significativamente con la presenza di ferro. L'analisi dei transienti di corrente al variare del tempo di intrappolamento ci permette di ipotizzare che l'intrappolamento non sia dovuto a difetti puntuali o comunque sia dovuta a difetti puntuali ammassati vicino alle dislocazioni. Una seconda trappola, T2, è evidenziata. L'analisi delle trappola in dispositivi con differente drogaggio e il confronto con analisi $g_m(f)$ ci permette di supporre che tale trappola, con una costante di tempo di 0.25s a T=40°C, sia situata nello strato AlGaN.

I risultati ottenuti da uno stress elettrico imposto al terminale di gate in dispositivi drogati con ferro ne definiscono gli effetti principali: (i) aumento della corrente di leakage, fortemente correlato con l'aumento di hot spot nell'elettroluminescenza e, superata la tensione critica, con un aumento del current collapse. (ii) aumento del segnale associato a segnali preesistenti senza generazione di nuovi stati trappola. L'analisi, estesa a dispositivi con differente o nullo drogaggio in ferro dimostra che, se sottomessi a uno stress di affidabilità, tutti i dispositivi mostrano una variazione della corrente di leakage. Lo stress comporta inoltre un aumento del current collaspe, non correlato alla generazione di nuovi stati trappola bensì all'aumento del segnale associato alle trappole preesistenti, chiamate T1 e T2. La variazione dell'ampiezza di segnale in T2, che si presume essere nell'AlGaN, può essere connessa ad un aumento della concentrazione del difetto; la variazione di T1, che al contrario si presume essere nel buffer layer, può essere chiarita con la generazione di difetti connessi a cammini parassiti conduttivi tra il gate e il canale, generati a causa dello stress, che favoriscono il trasferimento di elettroni verso gli stati trappola.

Nell'ultima sezione si studiano nuovi materiali per migliorare le prestazioni della tecnologia GaN. Le strutture InAlN/GaN stanno diventando importanti grazie all'alta densità di portatori nel 2DEG e alla possibilità di ottenere una struttura lattice matched, migliorandone dunque la stabilità elettrica e termica. In questa tesi nuove strutture, in particolare ai contatti, sono discusse. Una prima analisi consiste nell'uso di un differente materiale per il contatto Schottky. Si propone un confronto tra HEMT InAlN/GaN con struttura identica ma differente gate, nello specifico Mo/Au e Ni/Pt/Au. Nonostante non si noti alcuna variazione significativa nell'analisi DC, la valutazione dei fenomeni di trapping mostra che l'uso di un contatto in Mo/Au mostra un miglioramento significativo nelle caratteristiche di trapping, principalmente dettata dal processo usato per la deposizione dei contatti. L'uso di un contatto in Mo/Au, come dimostrato dai risultati di uno stress in OFF state, non influenza la stabilità del dispositivo.

Una seconda analisi presenta una struttura in cui è effettuato un recesso prima della deposizione dei contatti ohmici per ridurre le resistenze parassite. Si propone un confronto tra due wafer, caratterizzati da una struttura simile e diversa quantità di drogaggio in carbonio al loro interno per limitare il fenomeno del punch through. L'analisi DC mostra una significativa

variazione nel valore , mostrando che un valore minore di I_{DSS} corrisponde a strutture con recesso ai contatti ohmici. Questo effetto è dovuto al non raggiungimento di una resistenza in zona lineare minore. L'analisi impulsata dimostra un alto valore di current collapse senza correlazione con struttura del dispositivo o presenza di recesso ai contatti ohmici. I transienti di corrente mostrano due trappole principali, T1 e T2. L'energia di attivazione, a differenza della sezione di cattura, non è influenzato dalla struttura del dispositivo o dal recesso ai contatti ohmici. I transienti di corrente, le misure $g_m(f)$ e lavori precedentemente proposti in letteratura ci permettono di ipotizzare che la trappola T1 sia situata nel buffer layer, a differenza della trappola T1 che è probabilmente sita nello strato AlGaN. Misure al variare del tempo di trapping confermano che entrambe le trappole non sono definite da difetti puntuali.

Introduction

In the last decades we have participated to a rapid development of communication systems. This progression, supported by the strong diffusion of communication devices such as satellite TV, navigation systems and mobile phones leads to the study of new devices structures and materials to satisfy the continuous requirements imposed by the market, in terms of both high power and high frequency necessities. Due to the corresponding electrical properties and devices employed, the silicon based technology reached in many fields of application limits in the performances if efficiency and stability at high frequency are considered.

In the last decades requirements imposed by the market and development of communication systems have been partially satisfied by the introduction of new materials, such as III-V materials, characterized by a high direct energy gap and high mobility values. Silicon technology has been thus overcome by gallium arsenide and gallium nitride technology. Gallium nitride is an interesting material particularly appropriate in satisfying high frequency and high power conversion requirements, as a consequence of its electrical properties: (i) the direct and high energy gap, especially for optoelectronic devices; (ii) high mobility and high saturation velocity especially at high frequency applications; (iii) high breakdown electric field and voltage in power applications. Although GaN technology has largely overcome GaAs one, according to properties previously explained, GaAs devices are still widely used, consistently with its well established characteristics and peculiar properties at high frequency, such as low loss and charge transport properties.

III-V materials found a wide diffusion thanks to new devices typologies introduced in the market in the last decades. An example is provided by High Electron Mobility Transistors (HEMT). By means of modulation doping concept or exploiting the charge due to the piezoelectric and spontanteous polarization at the interface a triangular quantum well where electrons are confined is created, thus generating the so called bidimensional electron gas (2DEG). Therefore, through the avoiding of scattering a the hetero-interface due to the absence of dopants in the channel and through the confinement of electrons in a quantum well where they can move except for in the growth direction, two main characteristics are obtained: (i) high mobility due to the reduction of dopant scattering; (ii) high density of carriers in the channel. This last can be enhanced by the use of different materials such as InAlN.

Although good performances reached by gallium arsenide and gallium nitride technology, many reliability issues can still be reported. According to the potentiality of III-V materials and High Electron Mobility Transistor we can understand the importance of studying some partially resolved reliability aspects. Furthermore, in order to reach better performances and avoid limits imposed by technology, both in terms of device structure and device material, we can imagine how it is essential to study new materials and structure to reach further improvements.

The main purpose of the thesis is to analyse reliability aspects by focusing on several material used in order to better understand and compare limits and performances reported by the use of materials with different properties. Furthermore some innovative materials and structure to improve performances are discussed.

In the first chapter III-V materials are described. A detailed analysis of gallium nitride lattice, bandgap and electrical properties is firstly described. Therefore, in order to further discuss the operation of GaN HEMT and the generation of the 2DEG, an explanation of different polarizations mechanism is provided. A description of different substrates is finally provided, thus demonstrating how this aspect is crucial. Similarly, gallium arsenide is exhaustively described through lattice, bandgap and electrical properties definition. In the last paragraph main growth techniques, used both for gallium arsenide and gallium nitride, are explained in order to define main advantages and drawbacks. Main methods are: (i) MBE, (ii) OMVPE, (iii)HPVE.

In the second chapter an overview about devices is proposed: (i) High Electron Mobility transistor structure and operation is described in the first paragraph. A detailed analysis of polar materials properties and contacts used to enhance the performances is shown. (ii) fundamentals about power amplifiers principle and class of operation is reported.

In the third chapter thermal degradation of GaAs devices is evaluated. After a short introduction to explain main failure modes and mechanisms, these last have been explained and confirmed through two different analysis: (i) a long term thermal stress on pHEMT with no DC bias applied; (ii) a HTOL test on power amplifiers testing the device both with thermal and electrical stress. (iii) A detailed analysis to accurate estimate the channel temperature is therefore proposed.

In the fourth chapter electrostatic discharge (ESD) robustness has been demonstrated on a MMIC power amplifier. After a short introduction to describe main failure mechanisms and modes and to provide information about methods to simulate ESD phenomenon, ESD robustness is studied by means of TLP (Transmission Line Pulse), HBM (Human Body Model) and MM (Machine Model). ESD protection structures and failure mechanisms have been finally studied with Scanning Electron Microscopy (SEM).

In the fifth chapter trapping phenomena in AlGaN/GaN HEMTs are considered. After a short introduction to describe main trapping effects and main causes of degradation due to electrical stress in AlGaN/GaN HEMTs, a detailed analysis of trapping mechanisms and its correlation with iron doping in the buffer layer is reported. In the last two paragraph correlation among different degradation effects (namely DC analysis, trapping behaviour and emission microscopy) due to a reliability stress is reported. This correlation is further compared in devices with different Fe doping quantities.

In the sixth chapter improvements provided by the use of a InAlN/GaN structure are described. In the first paragraph characteristics of InAlN structures in terms of material and electrical properties are reported. Two innovative structures to improve stability and characteristics in terms of DC parameters and trapping behaviour are presented: (i) The use of a Mo/Au gate contact instead of Ni/Pt/Au conventional one; (ii) introduction of recess at the ohmic contacts to reduce parasitic resistances.

Chapter 1: III-V Materials: Gallium Arsenide and Gallium Nitride properties

1.1 Gallium Nitride (GaN)

In the last years gallium nitride became a very suitable material for the development of optoelectronics devices (Light Emitting Diodes, LASER) and of devices aimed at high frequency and power applications, such as High Electron Mobility Transistors. The interest toward the gallium nitride material is firstly due to its intrinsic electrical properties. The presence of a direct high energy gap leads to the achievement of good performances especially in optoelectronics devices such as visible and UV LED, LASER and UV detectors. Moreover, due to its high mobility, gallium nitride is used for the development of High Electron Mobility Transistors, demonstrating in many aspects higher performances than Gallium Arsenide. A further feature which suggests its use for the development of HEMTs, especially requiring high power performances, is the high electric field breakdown value.

On the other hand gallium nitride has some disadvantages, which, despite the improvements achieved, limit its performances from the reliability point of view. An issue, especially reported in the first structures developed, is represented by the difficulty of finding reliable materials to grow the GaN structure. This limit has been partially overcome by the introduction of substrates such as Silicon Carbide (SiC), sapphire (Al_2O_3) and silicon (Si) and by the employ of grown techniques mainly consisting of the Molecular Beam Epitaxy (MBE) and Chemical Vapour Deposition (OMPVE).A further problem affecting GaN devices reliability is the creation of defects and impurities during the growth; consequent effects on reliability (e.g. trapping and breakdown phenomena) affect the devices.

1.1.1 Lattice properties

Gallium Nitride is a III-V compound composed by an element from the III group of the Mendeleev Table, Gallium, and an element from the V group, Nitrogen.The compound can assume three different crystal structures: rock salt, wurtzite (Wz) or Zincblende (ZB). In the following we will discuss about the last two structures with a special attention to the second one, since it is the most used in the semiconductor devices.

The zincblende structure can be created with a stable form if thin layers are grown epitaxially in the (011) plane on substrates like Si, SiC, MgO and GaAs. The rock salt structure is hardly realizable and it is usually grown under high pressure which, decreasing the lattice

dimensions, allows the generation of ionic than covalent bonds. The gallium nitride is realizable in the rock salt form only with a pressure of 48.8 GPa, not possible with the epitaxial growth. Both in the Wurtzite and in the Zincblende structure each element has tetrahedral bonds: each gallium atom (III group) is bonded to four nitrogen atoms (V group) and vice versa. The cell of a Zincblende structure, which is usually called sphalerite, is cubic and composed by four atoms of the III and four atoms of the V group. The structure consists of two interpenetrating face-centred cubic sub-lattices, offset by one quarter of the distance along a body diagonal. Such structure is similar to the one which characterizes the diamond lattice. As it can be noticed in Figure 1.1a the lattice parameters which describe this structure are $a = b = c$ and $\alpha = \beta = \gamma = 90°$.

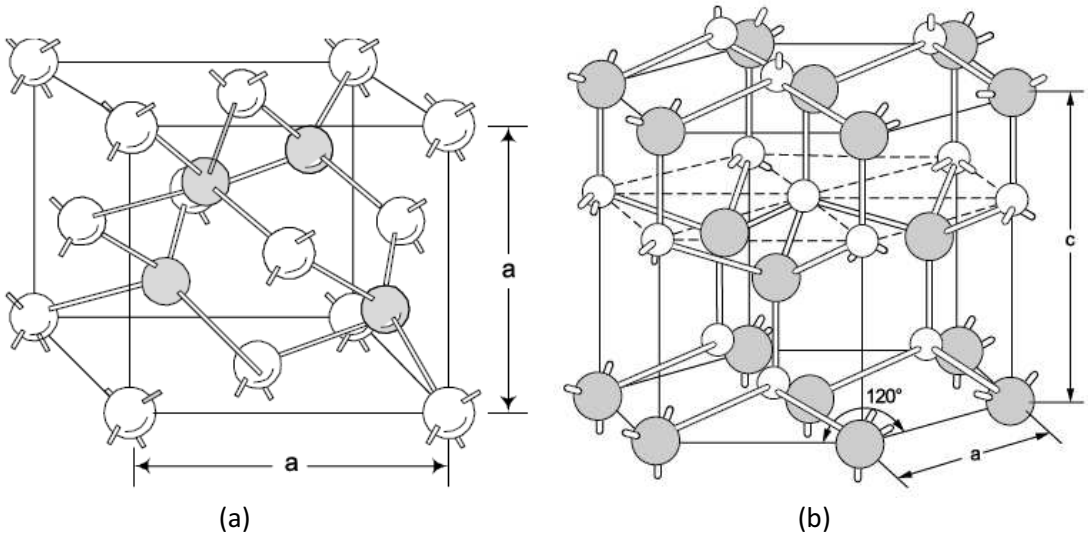


Figure 1.1: Gallium nitride lattice structure: (a) zincblende and (b) wurtzite

The wurtzite structure is characterized by a hexagonal unit cell and, thus, by two different lattice constants (which can be called a and c). The structure consists of two interpenetrating hexagonal close-packed sub-lattices, each with one type of atom, offset along the c-axis by 5/8 of the cell height i.e. (5c/8). As it can be noticed in Figure 1.1b the lattice parameters which describe the structure are $a = b \neq c$ and $\alpha = \beta = 90°, \gamma = 120°$. Since the zincblende is not stable only the Wurtzite phase can be used for optical and electronic devices.

As it will be described in the following paragraphs the lattice structure strongly influences the material electronic properties. The lattice constant, for instance, influences the energy gap value with a inversely proportional trend. The tetrahedral structure which describes gallium nitride determines strong bond of different nature between the atoms, thus influences the material stability of the device and thus leading to high performances in power applications.

1.1.2 Energy gap and band structure

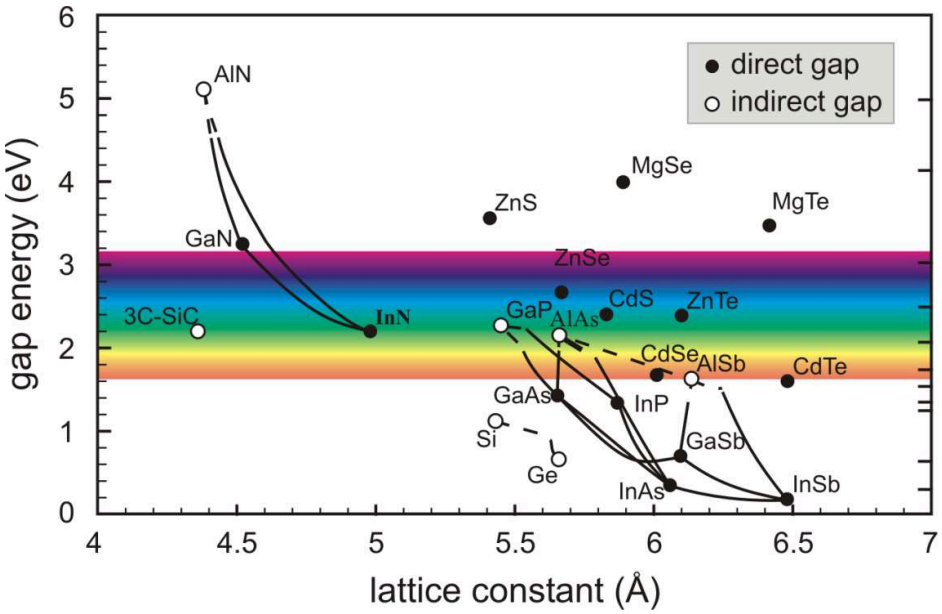
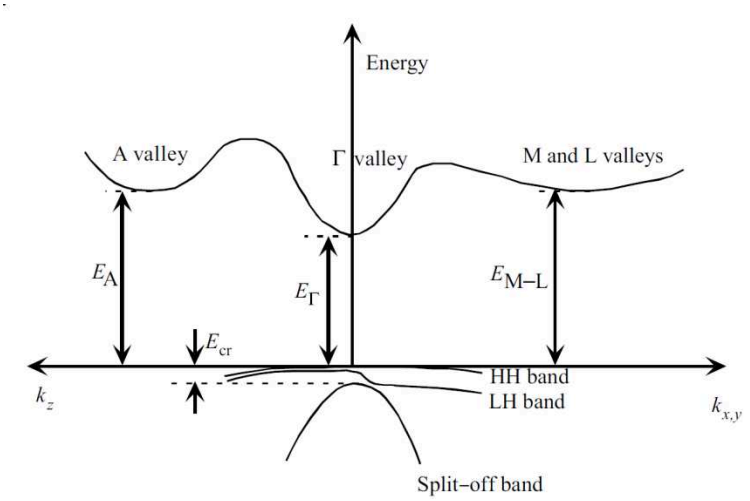


Figure 1.2: Energy gap value as a function of the lattice constant

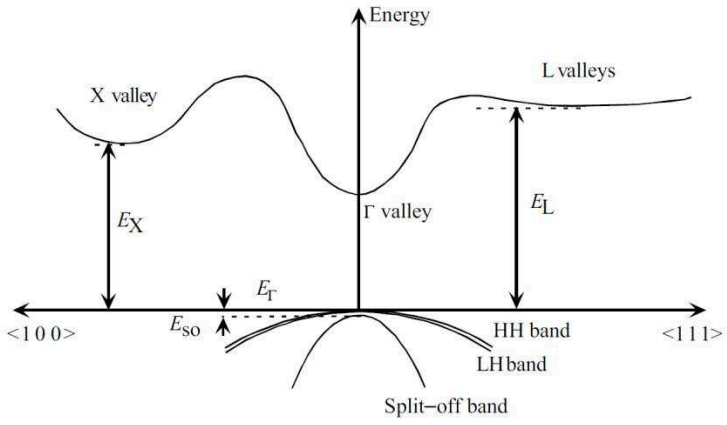
One of the most important characteristics of the gallium nitride is the energy gap; the presence of a large and direct energy gap allows the use of the GaN for optoelectronic devices, short wavelength light emitters and high power electronics. A direct energy gap characterizes GaN both in the wurtzite or the zincblende form. An element is defined with direct energy gap if the minimal moment of the conduction gap is aligned with the maximal moment of the valence band. Differently from the materials with an indirect energy gap only the use of energy is required for the transition from a band to another, without the necessity of a phonon. In all the nitrides the energy gap value varies with an inversely proportional trend than the lattice constant, as shown in Figure 1.2. Nitrides have usually band gaps ranging from 1eV to 6eV: energy gap of AlN (higher than 6eV) is much higher than the value reported in GaN (3.12eV) and in InN (about 2eV); this last reports the lowest value in nitrides binary compounds.

In Figure 1.3a and Figure 1.3b it is indicated GaN band structure in the wurtzite and zincblende form. It is possible to notice that in both the cases the energy gap is direct, since the minimum of the conduction band is aligned with the maximum of the valence band. In both the GaN forms the compound is characterized by the degeneration of the valence band in three curves, caused by the high electric field values due to the lattice structure. These curves are defined as HH (Heavy Holes), LH (Light Holes) and Split Off. In the zincblende form the HH band has similar values to the LH one. On the contrary the wurtzite form, which is the most available in nature and the most used, shows different curves for the HH and the LH band. Such difference is higher in the M-L valley.

This characteristic leads to the formation of an intrinsic strain in gallium nitride and to a lower influence to eventual external strains [1]. The presence of an intrinsic strain offers significant advantages to GaN structures, especially the so called piezoelectric polarization. However this peculiarity leads also to some disadvantages, such as the difficulty to find suitable substrates with no lattice and thermal mismatch. Figure 1.4 shows the trend of the valence band when a biaxial or not axial strain is applied on the c-plane [1]. Despite a high state density and axial symmetry is maintained, the influence of a biaxial strain generates a higher difference between HH and LH band with no generation of further significant difference. On the contrary a tensile not axial strain applied along the y direction causes a lowering of the state density on the x axis and of the y axis if the LH and the HH bands are considered, respectively. Thus a global state density lowering is determined [1].



(a)



(b)

Figure 1.3: GaN band structure in the wurtzite (a) and zincblende (b) structure [1]

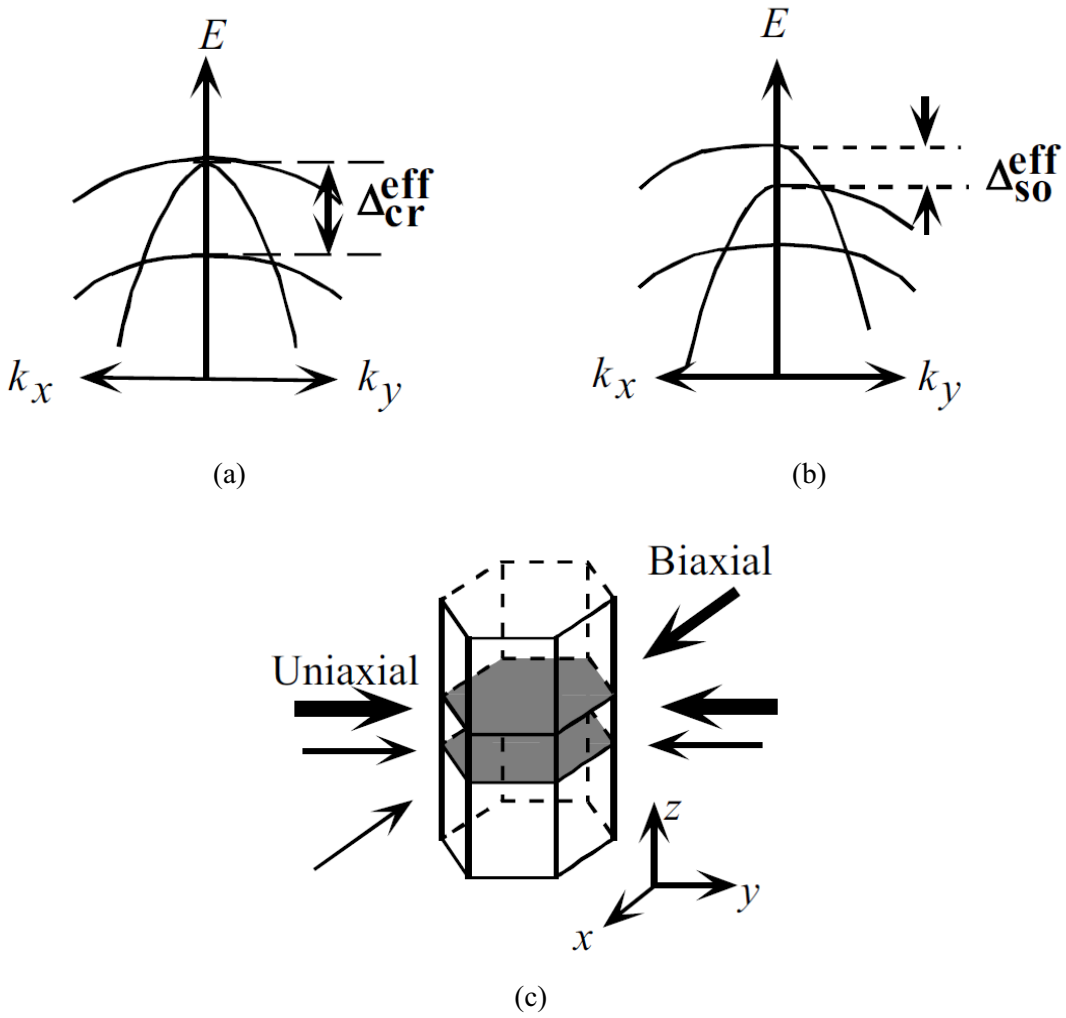


Figure 1.4: (a) biaxial and (b) not axial tensile strain. (c) definition of biaxial and unaxial strain [1]

1.1.3 Spontaneous and Piezoelectric polarization

All the compounds belonging to the III-V group are characterized by polarization effects. Gallium nitride has two typologies of polarization: spontaneous and piezoelectric polarization. The first one is due to the symmetry of the electric charges intrinsic in the structures which generate an electrical dipole and a correspondent momentum. The second typology of polarization is not intrinsic but due to mechanical stresses induced in the lattice which are caused, for instance, when a GaN layer is grown on a substrate of different nature.

Hetero-structures, such as the junction AlGaN/GaN, are always characterized by spontaneous polarization, even if no strain is reported, as a consequence of the spontaneous polarization which characterize both the structures. In these structures, as a consequence of the high difference between the spontaneous polarization coefficients of the two structures, the spontaneous polarization value is high. On the contrary, in different hetero-structures such as

InGaN/GaN the spontaneous polarization much lower. As it will be later explained, the presence of spontaneous and piezoelectrical characterization is crucial for the creation of the 2DEG in polar materials. Piezoelectric polarization constants have a value one order of magnitude higher in GaN than in different semiconductors belonging to the III-V group [1]. The piezoelectric effect is due to a strain caused partially to a lattice mismatch and partially to a thermal mismatch which is induced by the difference between the TEC (thermal expansion coefficient) of the layer grown and of the substrate used. When the GaN is grown on a substrate with a different TEC or lattice constant, a mismatch due to thermal and lattice aspects is generated. Thus a polarization is determined at the interface. The orientation of the piezoelectric polarization strongly depends on whether the generated strain is tensile or compressive

1.1.4 Electrical properties

From the chemical point of view gallium nitride has two important characteristics: high stability and material hardness. The high stability value, even if high temperatures are applied, is mainly due to the fact that atoms are connected one each other in a tetrahedral structure by means of ionic bonds. The typology of bonds between atoms which characterize the structure lead to a lower formation of dislocations and lattice defects, even if high current and temperature is applied. This property, as a consequence, limits degradation phenomena in the material and allows the use of gallium nitride especially in optoelectronic devices.

A second important property which characterizes gallium nitride is the thermal expansion coefficient (TEC). The TEC coefficient establishes the variation $\Delta x/x$ of the lattice parameters as a function of the temperature. This coefficient depends on intrinsic aspects in the material such as the stoichiometry, the presence of defects and the free carriers concentration [1] (Figure 1.5). This aspect is very important since it influences the GaN growth on different substrates. Works reported in literature clarify that, if we consider the lattice parameters variation, a higher dispersion in the TEC coefficient is measured if GaN is grown on different substrates [1], [2]. If we consider the configuration described for the Wurtzite structure in the previous paragraph, a lattice parameter variation $\Delta a/a = 5.59 \cdot 10^{-6}\ K$ is noticed in a temperature range between 300 and 900K [2]; in the same structure a lattice parameter variation $\Delta c/c = 7.75 \cdot 10^{-6}\ K$ is noticed in the same temperature range (between 300 and 900 K) while a lattice parameter variation $\Delta c/c = 3.17 \cdot 10^{-6}\ K$ is noticed in a temperature range between 300 and 700K [2]. It is important to analyse the TEC coefficient because the devices are grown at very high temperatures; furthermore it is important to remember that such coefficient is influenced by the substrate where the GaN structure is grown.

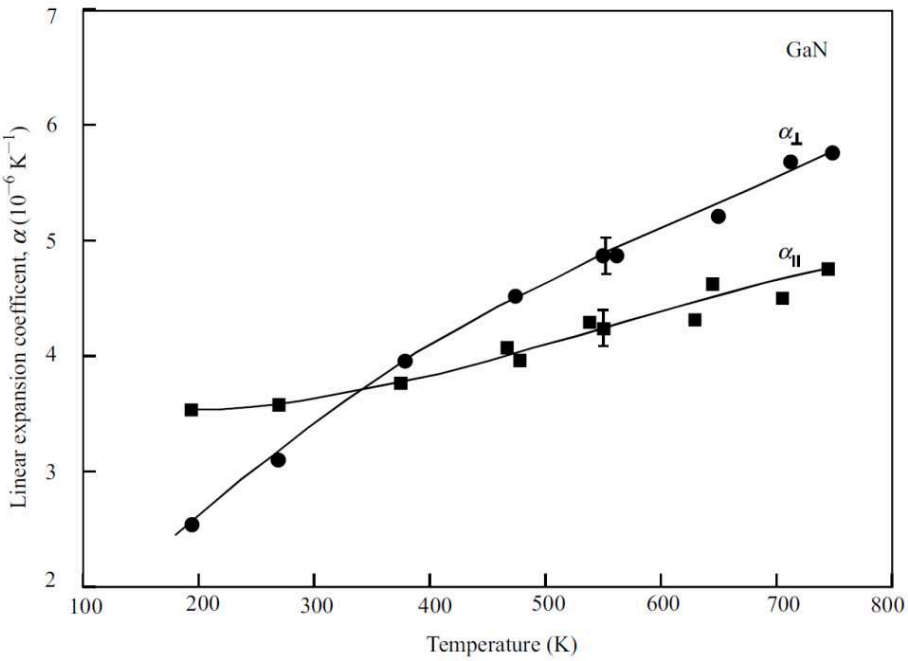


Figure 1.5: Thermal Expansion Coefficient (TEC) in GaN as a function of temperature for basal plane (a||), a parameter, and out ofthe basal plane (a⊥), c parameter, directions [3]

Gallium nitride finds wide application in devices which require high power and high frequency. It is therefore important to define a parameter which describes the performances according to both power and frequency requirements: the Johnson's figure of merit, described in (1.1), where the first term describes the output power while the second term the cut off frequency.

$$F_J = max(P_{out}, f_T) \qquad (1.1)$$

Such figure of merit is expressed as a function of the breakdown electric field E_{BK} and the saturation of the carriers velocity v_{sat}. The output power, once expressed as the product between voltage and current, can be defined as a function of E_{BK} and v_{sat} as described in(1.4). The cut-off frequency can be described as a function of the saturation velocity and of the channel length (1.5), where d is the channel thickness and ε the dielectric constant.

$$V_{max} = \frac{\varepsilon_S E_{BK}^2}{2qn} \qquad (1.2)$$

$$I_{max} = qndv_{sat} \qquad (1.3)$$

$$P_{out} = \frac{1}{2}\varepsilon_S E_{BK}^2 d v_{sat} \qquad (1.4)$$

$$f_T = \frac{v_{sat}}{2\pi L_g} \qquad (1.5)$$

If we consider the definition previously given, the Johnson's figure of merit is proportional with a quadratic trend both to the carriers saturation velocity and to the breakdown electric field. According to Table 1.1, which describes Johnson's figure of merit for several semiconductors, Gallium nitride is characterized by a value two orders of magnitude higher than similar semiconductors such as Si or GaAs. GaN Johnson's figure of merit is higher also than the one reported in InP and SiC. This confirms that GaN can reach higher performances than GaAs or Si in applications which require high power or high frequency. In Table 1.2 main electrical properties of GaN are reported.

	Si	GaAs	InP	SiC	GaN
JFOM	1	7.8	14.7	400	625

Table 1.1: Johnson's figure of merit

	Si	GaAs	InP	SiC	GaN
BandGap (eV)	1.1	1.42	1.35	3.26	3.49
Electron Mobility at T=300°C ($cm^2/V \cdot s$)	5500	8500	5400	700	1000÷2000
v_{sat} ($10^7 cm/s$)	1	1.3	1	2	1.3
Breakdown field (MV/cm^2)	0.3	0.4	0.5	3	3
Thermal conductivity ($W/cm \cdot K$)	1.5	0.5	0.7	4.5	>1.5
Dielectric constant (ε_r)	11.8	12.8	12.5	10	9

Table 1.2: Electrical properties

The energy gap value, as previously described, is very high if compared to the one of similar semiconductors such as Si, InP or GaAs. Furthermore, differently from Si, it is characterized by a direct energy gap, allowing the achievement of very good performances in optoelectronic. The breakdown electric field, as already defined with the Johnson's figure of merit, has a very high value (one order of magnitude) if compared, for instance, to GaAs or Si. Thus, according to equation (1.4), high values can be reached in the output power and cut-off

frequency. The Johnson's figure of merit is mainly influenced by the breakdown electric field. Indeed, if we compare semiconductors such as GaAs and Si with GaN, the carriers saturation velocity has similar values. The electron mobility in GaN, however, is much lower than in GaAs and similar to the one measured in Si.

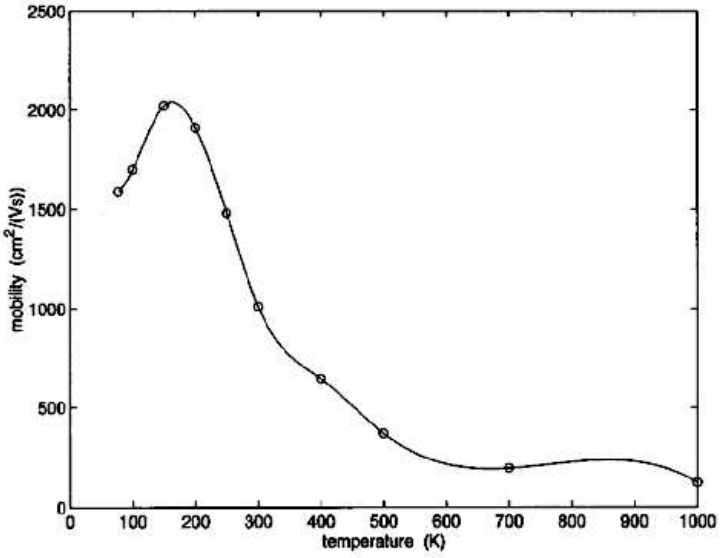


Figure 1.6: Mobility in GaN as a function of the temperature [4]

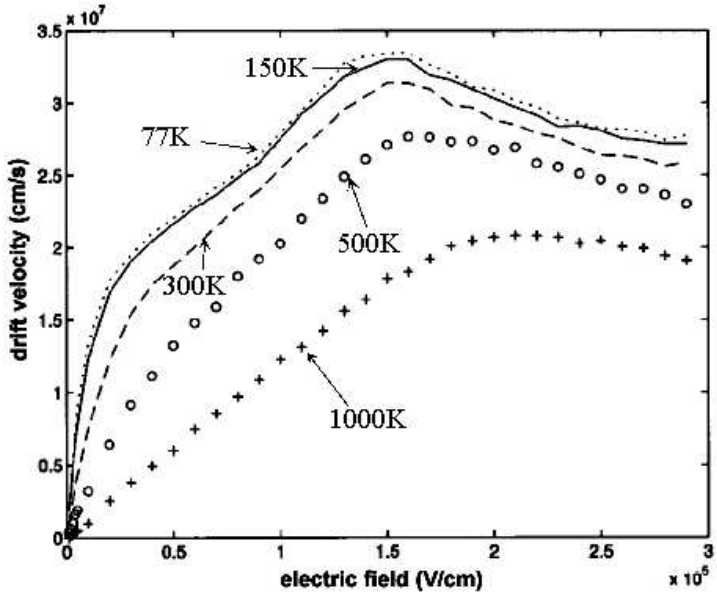


Figure 1.7: drift velocity in GaN as a function of electric field [5]

Furthermore, as shown in Figure 1.6, the mobility varies as a function of temperature reaching the highest value at 200K and decreasing with an almost exponential trend if higher

temperatures are applied [4]. One of the issues which affect device mobility is its correlation with the presence of ionizing impurities in the material. Indeed the mobility decrease strongly depends on scattering, which is significantly influenced and due to the ionizing impurities [4]. The impact of the mobility on device performances is very important, especially if we consider the high carriers concentration which characterize gallium nitride. Indeed both the aspects strongly lead to a current high density value and to a low channel parasitic resistance [4]. In Figure 1.7 it is reported the drift velocity measured in GaN doped with $N_D=10^{17}$ cm^{-3} as a function of electric field for several ambient temperatures applied [5].

1.1.5 Substrates for GaN growth

One of the most important issues which affect GaN growth is the choice of a proper substrate. All the nitrides devices show a significant difficulty in growing thin layers on substrates of the same material (homoepitaxy). As a consequence many substrates have been investigated in the growth of GaN films. According to lattice parameters and thermal characteristics the most promising results have been shown on sapphire and SiC. In addition, III–V nitrides have been grown on Si, NaCl, GaP, InP, W, ZnO, $MgAl_2O_4$, TiO_2, and MgO [1]. Other substrates as well have been used for nitride growth, including Hf and $LiAlO_2$, and $LiGaO_2$[1]. Table 1.3 reports main lattice and thermal parameters for the most common substrates. Thermal mismatch is important since it causes the epilayer to crack on cooling.

Furthermore a great importance is given to lattice parameters, too, since lattice-mismatched substrates lead to a substantial density of misfit and threading dislocations, providing for a decrease of the main parameters performances. Defects such as inversion domain boundaries and stacking faults lead to the presence of energy states in the forbidden band gap and, thus, reduce quantum efficiency and enhance scattering centres. Furthermore the creation of structural and point defects determines a decrease of electrons lateral transport and an increase of carriers vertical one [1]. A solution to the issues induced by lattice mismatch is provided by the use of a nucleation layer (mainly in AlN), a layer introduced to reduce the lattice mismatch between different materials.

Extended defects induce the generation of leakage. This aspect is crucial both in optoelectronic devices (since it leads to the formation of dark current in detectors and the reduction of quantum efficiency in emitters) and electrical structures (determining an increase of gate leakage current and output conductance in Field Effect Transistors).

Some of the substrates commonly used, such as Silicon Carbide (SiC), sapphire (Al_2O_3) and Si will be described. SiC is probably the preferable material used as substrate, as a consequence of the achievement of high resistivity SiC and SiC high thermal conductivity. Despite the lower lattice and thermal mismatch with nitrides sapphire is one of the most common materials used

as substrates, too, due to its wide availability, hexagonal symmetry and ease of handling and pre-growth cleaning. A further important property is sapphire stability at high temperature which allows the use of several epitaxial growth methods.

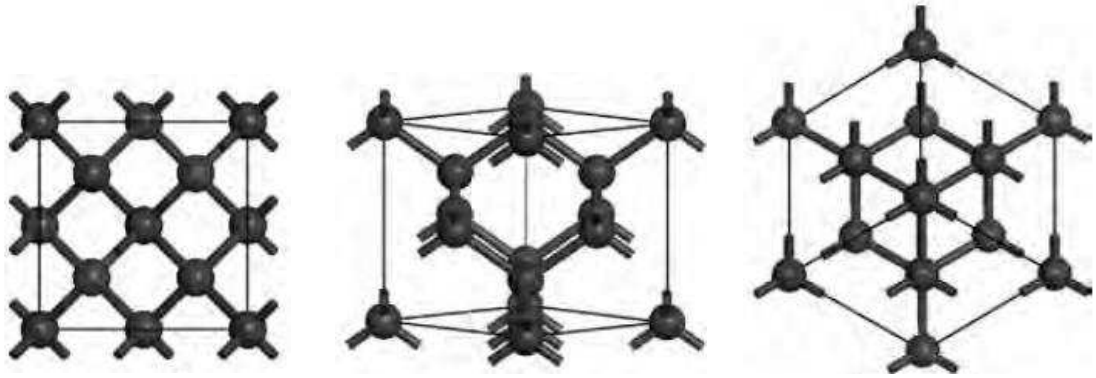
	Conventional		Thermal conducivity	Δa/a	Δc/c	mismatch
	a	c				
AlN (hexagonal)	3.104	4.966	3.2	4.2	5.3	-2.7%
GaN (hexagonal)	3.189	5.175	2.3	5.59	3.17	0%
Al_2O_3 (sapphire) (rhombocaedrical)	4.758	12.991	0.3-0.5	7.5	8.5	49% (~13%)
4H-SiC (hexagonal)	3.073	10.053				-3.63%
6H-SiC (hexagonal)	3.0817	15.1123	4.9	4.2	4.68	-3.36%
ZnO (hexagonal)	3.2496	5.2065	0.3-0.4	4.75	2.9	1.9%
Si (cubic)	5.4301		1.5	3.59		
GaAs (cubic)	5.6533		0.5	6		
B-SiC (cubic)	4.36		4.9			

Table 1.3: lattice mismatch and thermal properties of common substrates

Si

Si is a low expensive substrate with good properties for gallium nitride growth. Differently from GaAs and ZnO, Si is characterized by a good thermal stability, necessary for the GaN epitaxy growth. On the other hand Si leads to the formation of a significant number of defects, thus decreasing device performances.

Silicon has a diamond lattice structure and can be described as two interpenetrating face centred cubic sub-lattices with one sub-lattice displaced from the other by one quarter of the distance along a body diagonal of the cube. Single crystalline ingots are usually produced by the Czochralski (CZ) (85%) or Float Zone (FZ) method. When the FZ method is used the impurities are strongly reduced allowing the growth of high resistivity material. For wurtzite GaN growth (1 1 1) plane Si is used. One way for the preparation of silicon plane can consist on the removal of a thin surface level by RCA etch with hydrogenation of surface dangling bonds [1].



(a) (b) (c)

Figure 1.8: Si cell along the (a) [001], (b) [011], (c) [111] direction [1]

SiC

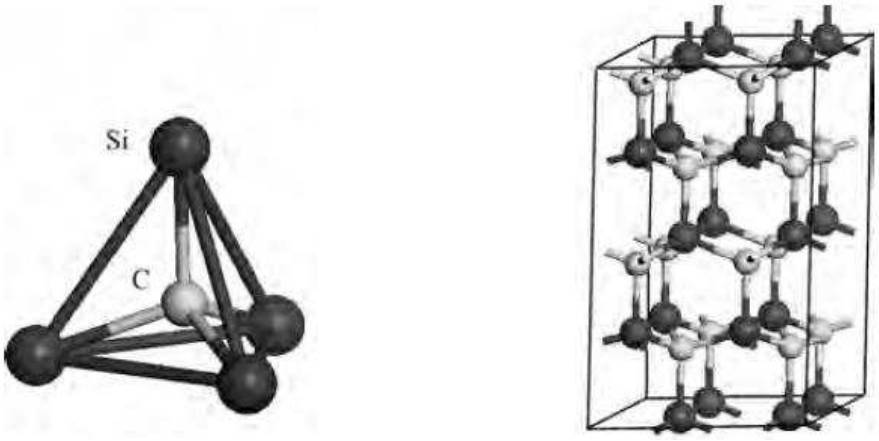
Silicon Carbide became one of the most used substrates for the epitaxy growing of both optical and electronic devices. Main advantages are due to the large thermal conductivity, the low amount of defects and the availability of high resistivity substrates. Silicon carbide lattice and thermal mismatch are, respectively 3.5% and 3.2%, revealing values much lower than the ones reported between sapphire and gallium nitride. Such aspect leads also to the lower generation of defects which characterizes the silicon carbide use for substrate. A further aspect which determine improvements induced by the use of silicon carbide is the high electrical and thermal conductivity. This characteristic allows the growth of thin layers and, thus, the use of this substrate on devices which requires high power. The material conductivity can be enhanced by the introduction of impurities inside the substrate.

The main drawbacks are represented by pre- epitaxy surface preparation, micro pipes, size and high costs. The high costs for the realization, which is mainly obtained by the HVPE technique, finds a solution in the use of new materials such as Silicon on polySic (SopSiC), silicon carbide on polySiC (SiCopSiC). Performances reached by devices grown on similar substrates not significantly differs from the ones achieved by GaN grown on Silicon Carbide.

A silicon carbide cell is a covalently bonded tetrahedron which consists of a carbon element in the centre surrounded by four silicon atoms or vice versa (Figure 1.9a). The variation of the stacking order of silicon and carbon atoms along the c direction generates several polytypes (Figure 1.9b, Figure 1.10). Polytypes are characterized by different electronic and optical properties with a bandgap value in a range between 2.39eV achieved in the 3C SiC and 3.33eV in the 2H SiC type. The most used polytypes in the GaN growth are the 4H and 6H SiC, characterized by an energy gap of 3.02 and 3.27 eV respectively. In both the 4H and 6H SiC substrates screw dislocations occur in high densities and depends on the magnitude of the Burgers vectors [1]. The core of a screw dislocation can consist on nanopipes or micropipes or

extend through the entire wafer. The first case is reported when the Burgers vector is two or more times or three times the lattice constant for 6H and 4H SiC, respectively [1].

One of the most common ways to prepare the SiC substrate, both in the case that MBE or OMPVE techniques are used, is to use a gas phase preparation of the SiC surface by exposing it in H or HCl gases at high temperature [1].



(a) (b)

Figure 1.9: (a) Tetrahedral Structure of Silicon Carbide, (b) 3D structure of 2H SiC [1]

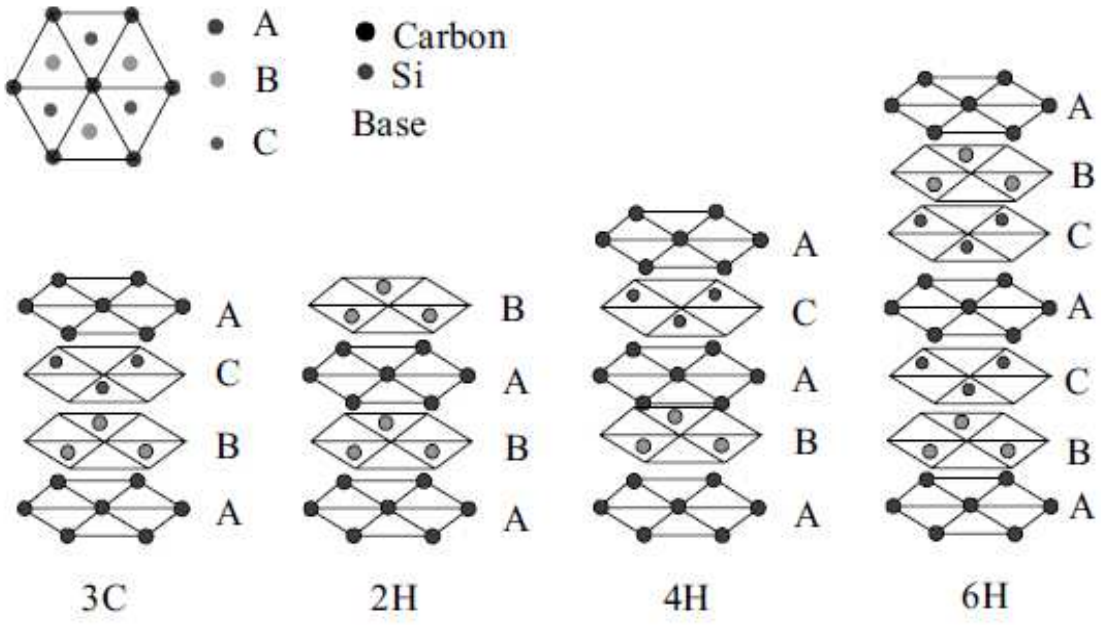


Figure 1.10: Different polytypes for Silicon Carbide structures [1]

Al_2O_3

A sapphire substrate is often used for GaN growth because of its low cost and availability in large area. Furthermore sapphire is a transparent material for most of the bandgaps of nitride alloys; as a consequence it is a very suitable material for detectors, for instance for back illumination, and for LEDs considering the lack of absorption. Sapphire has a crystal structure with hexagonal symmetry similar to the one of the GaN with wurtzite form. A comparison between the two structures is shown in Figure 1.11.

The sapphire cell can be represented by rhombohedral unit cells (Figure 1.12a) or by a hexagonal unit cell (Figure 1.12b): the rhombohedral unit cell has 10 ions in total, 4 Al^{3+} ions and 6 O^{2-} ions; the hexagonal unit cell has 30 ions in all, 12 Al^{3+} ions and 18 O^{2-} ions [1]

Major drawbacks are sapphire lattice and thermal mismatch with GaN. Such values are higher than the ones reported in SiC structures. However, significant improvements have been achieved and sapphire allows the achievement of high temperature stability and Johnson's figure of merit in GaN structures grown on it. Thus good performances have been obtained both in terms of high frequency and high power.

To prepare the sapphire substrate for epitaxy many techniques have been used, despite none of these techniques leads to a surface with no damage or scratches: examples are provided by wet chemical etching and hot etching [1]. A solution, in some cases, is defined by the use of a high temperature annealing technique after wet chemical etching of mechanically polished sapphire substrates [1].

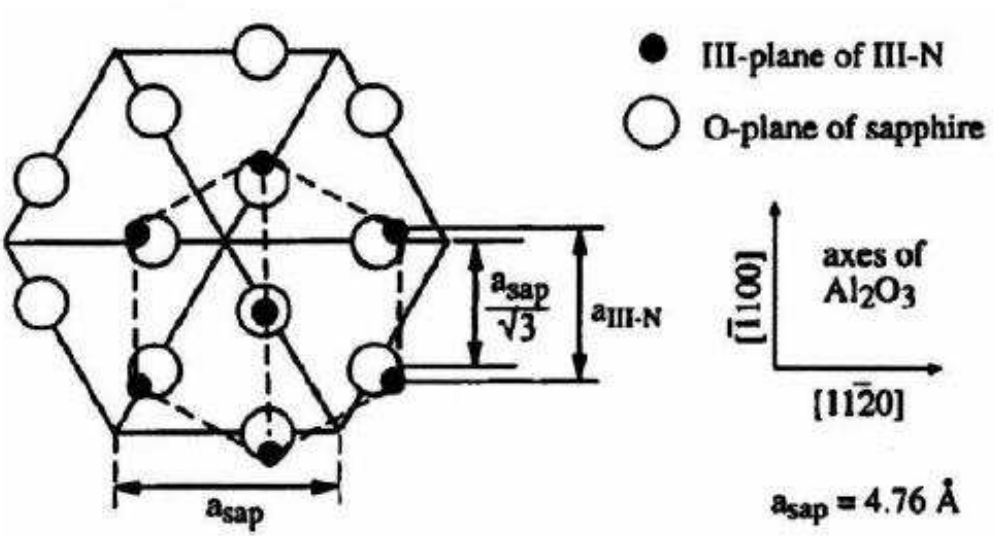
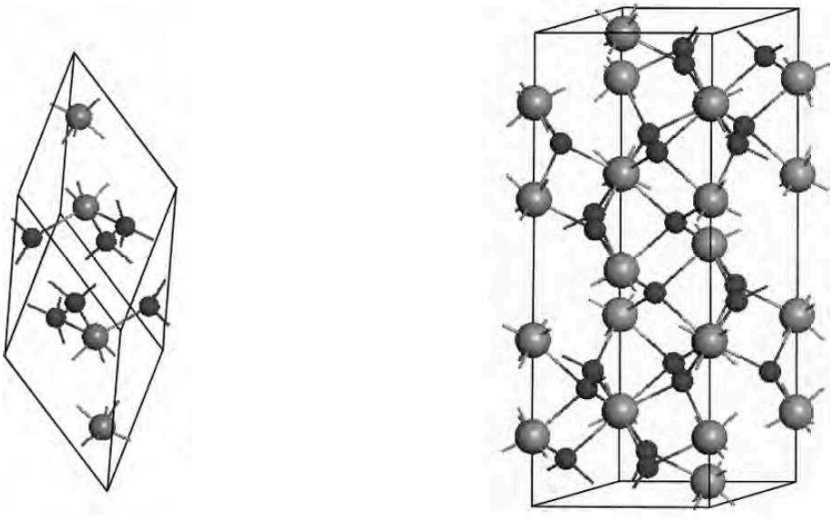


Figure 1.11: Comparison between sapphire with hexagonal form and GaN with wurtzite form [6]



(a) (b)

Figure 1.12: Sapphire structure in the (a) rhombohedral and (b) hexagonal form [1]

1.2 Gallium Arsenide (GaAs)

For decades GaAs material found a wide application on electronic devices. As a consequence of its characteristics GaAs overcome the use of silicon in several fields of application. The high mobility value and drift velocity at low electric fields allowed its wide use for applications which require high frequency performances. Furthermore GaAs, differently from Si, is characterized by a high and direct energy gap which allows a higher radiative recombination between conduction and valence band. Moreover gallium arsenide, differently from silicon, allows the possibility of generating a hetero-structure and the creation of the so called 2DEG for the channel, thus enhancing the mobility and device performances, as it will be better explained in the next chapter.

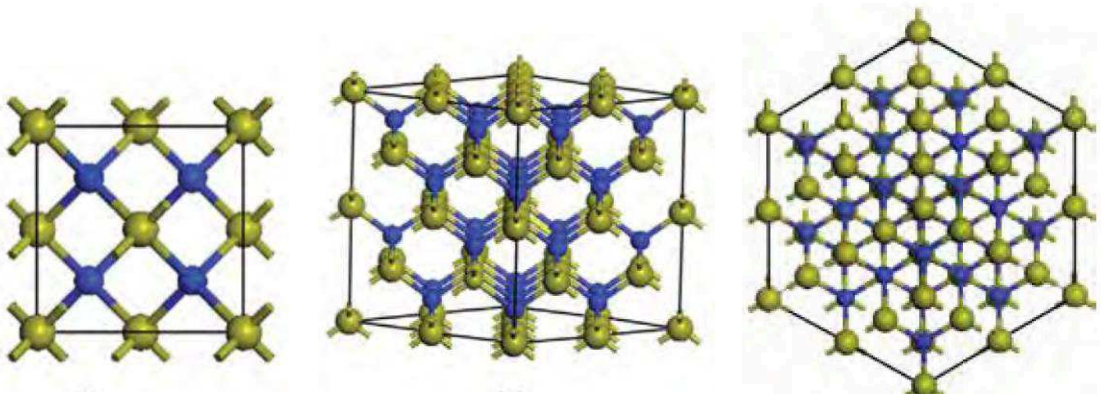
On the other hand, from the comparison between GaAs and Si properties, several aspects limited GaAs application, especially in the first years. (i) GaAs holes mobility, differently from electrons mobility, reveals no significant improvement than in Si; (ii) GaAs is characterized by a lower thermal conductivity; (iii) GaAs fragility which imposes the realization of wafers with higher thickness than Si; (iv) high fabrication costs.

In the last years GaAs has been partially overcome by the use of GaN. As a consequence of gallium nitride higher energy gap value and of its higher Johnson's figure of merit GaN found a wide application in devices with both high frequency and power requirements.

However, for many application, such as MMIC (monolithic microwave integrated circuits) gallium arsenide still remains a preferred choice, due to its excellent charge transport properties and its low loss at microwave and millimetre-wave frequencies. In some cases, for instance applications up to 3GHz, Si LDMOS offer high power and good performances. Further solutions are given by RF Si CMOS devices and SiGe bipolar devices. Gallium Nitride (GaN) technology has shown extremely high power densities and efficiencies up to microwave and mm-wave frequencies, but has limitations related to the high cost of substrates (SiC) and to possible process and reliability issues. A solution has been partially provided by very good reliability performances and reduction of costs shown by using epitaxial GaN grown on semi-insulating Si.

1.2.1 Lattice properties, Energy gap and band structure

Gallium arsenide has a zincblend crystal structure with a lattice constant of 5.6536Å. A perspective view of the GaAs crystal along different directions is provided in Figure 1.13. In Figure 1.13a [1 0 0] direction is taken into account, while in Figure 1.13b and Figure 1.13c are considered directions [1 1 0] and [1 1 1], respectively.



(a) (b) (c)

Figure 1.13: perspective view of GaAs crystal [1]

Gallium arsenide is characterized by a direct energy gap (Figure 1.14). Thus the minimum of the conduction band is aligned with the maximum of the valence band. According to Table 1.2 GaAs demonstrates a bandgap value lower than GaN, 1.42eV and 3.62eV respectively. This value is quite higher than the one reported in other materials, such as InP (1.35eV) and Si (1.12eV), which furthermore, differently from GaAs, reveals an indirect energy gap (Figure 1.14). In GaAs the minimum of the conduction band and the maximum of the valence band corresponds to the Γ point of the Brillouin zone. Gallium arsenide is characterized by two further minimum of the conduction band: the first one is placed to the *L* point and has a bandgap of 1.72eV; the second one is noticed in the *X* point and has a bandgap of 1.90eV. The Energy gap determines a different value of the intrinsic carriers density, leading to a lower value estimated in gallium arsenide (1.8×10^{6} cm^{-3}) than in silicon (1.5×10^{10} cm^{-3}) when measured at T=300K.

Similarly to GaN band structure the degeneration of the valence band leads to three different curves: split off, heavy holes (HH) and light holes (LH). No significant difference is established between HH and LH curve in the wavevector portion between *L* and *X* (Figure1.15). On the contrary a strong variation between HH and LH curve is shown when a different portion of the Brillouin zone is considered, especially the portion between the point *K* and *L*.

The trend of the conduction and valence band near the minimum and maximum value (thus correspondent to Γ), determines also the electrons (or holes) behaviour both when diffusion processes and processes influenced by the electric field are considered [7]. In the last case the electrons efficacy mass evaluated has an inverse trend proportional to the band bending. GaAs efficacy mass is $m_n^* = 0.068m_0$, four times lower than the efficacy mass in Si ($m_n^* = 0.259m_0$). Thus, their acceleration, as a consequence of the application of an electric field, is higher and correspond to a higher carrier drift velocity for lower energies [7]. This phenomenon occurs only near the main conduction minimum, because in correspondence of the two further conduction band minimum efficacy masses are much higher with a stronger influence for high electric fields [7]. The efficacy hole mass in the HH and LH curves shows no relevant difference.

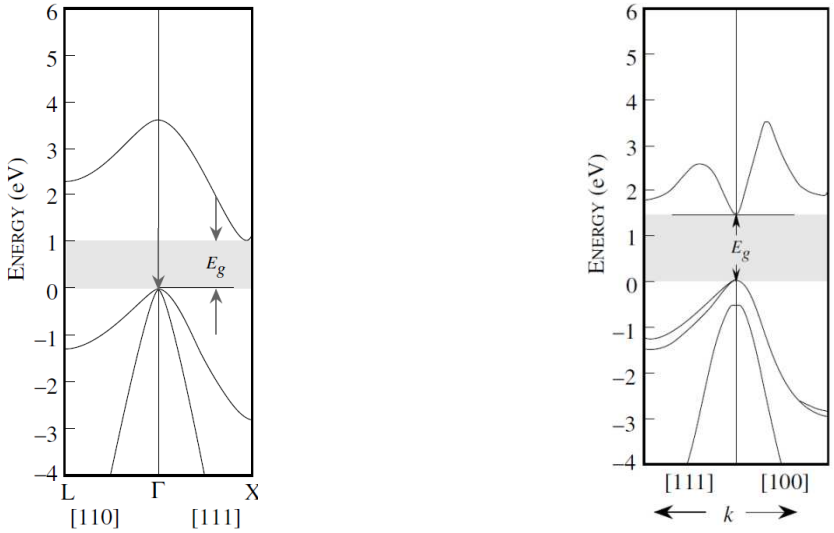


Figure 1.14: band structure of (a) Si and (b) GaAs [13]

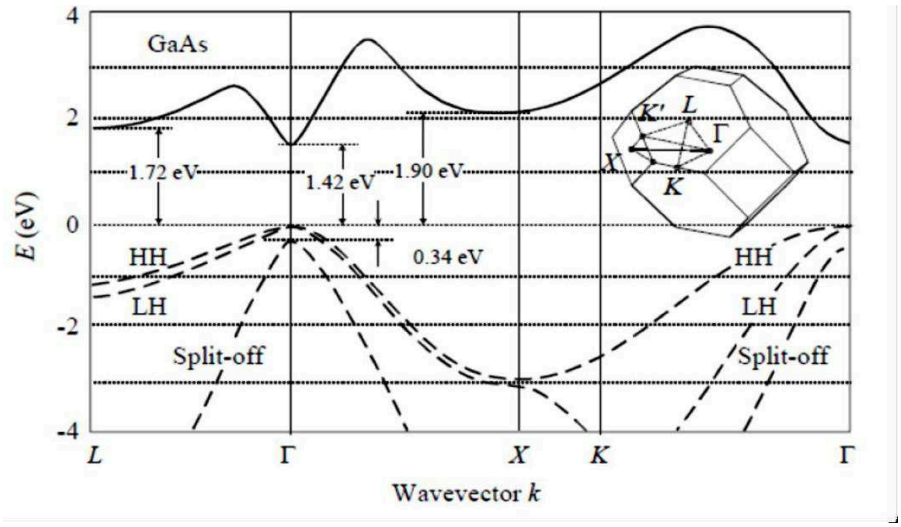


Figure1.15: Gallium Arsenide band structure

1.2.2 Electrical properties

A first important parameter to describe GaAs electrical properties is the mobility. According to Table 1.2 GaAs is characterized by an electron mobility much higher than similar compound semiconductors such as GaN or Si. At an ambient temperature T=300K a mobility of 8500cm^2/(Vs) is measured. This value is more than four times higher than GaN and Si, with a value in the range between 1000-2000 cm^2/(Vs). High mobility results in lower access resistance and rapid acceleration of channel electrons to their saturated velocity over a short distance. Both elements are important aspects in microwaves devices.

In a semiconductor the mobility can be limited by the scattering of electrons. There are several phenomena which induce the mobility decrease, as it is possible to notice in Figure 1.16, where the mobility trend is reported as a function of temperature applied [7]. According to previous studies [7], it is therefore possible to consider three different conditions: (i) for temperatures higher than 100K the mobility is mainly influenced by the electrons interaction with optical phonons; this phenomenon can be considered intrinsic to the material. In some cases, such as the growth of structures where a 2DEG is generated, the scattering due to polar optical phonons can be reduced. (ii) for temperatures near 100K the mobility reduction is due to the contribution of several phenomena: acoustic and optical phonons. (iii) for temperatures lower than 100K the mobility is mainly determined by ionized impurities, since further mechanisms can be considered as negligible at very low temperatures.

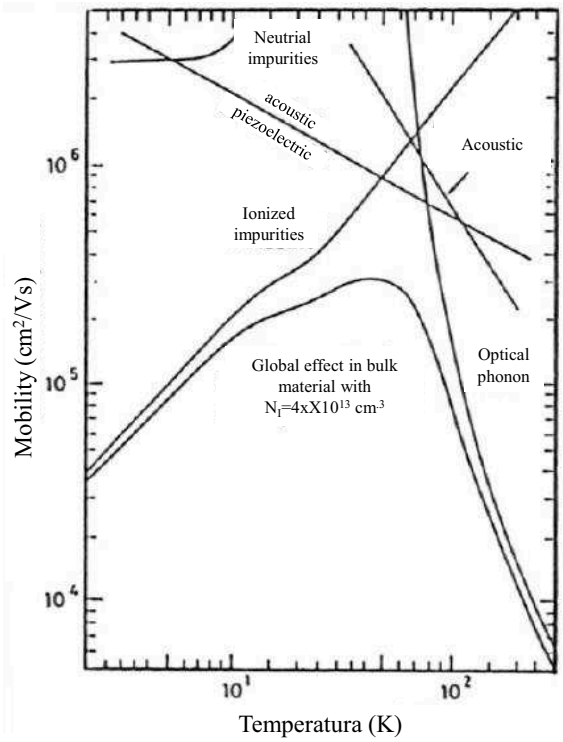


Figure 1.16: Mechanisms which affect GaAs mobility as a function of temperature [7]

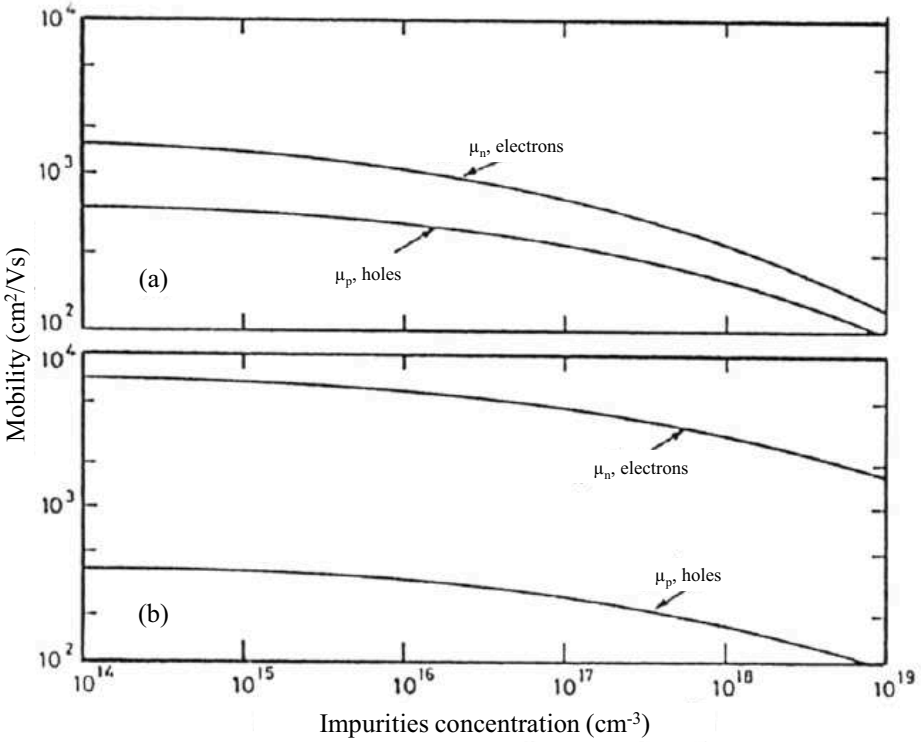


Figure 1.17: mobility as a function of impurity concentration in (a) Si and (b) GaAs [8]

In gallium arsenide the mobility of both electrons and holes is higher influenced by the increasing of impurity concentration than in Si. The trend of mobility increases as a function of impurities, mainly defined by lattice defects or ionized impurities, as a consequence of the increase of their interaction with carriers [7]. Figure 1.17 shows mobility trend measured at T=300K.

A second important parameter to consider is the drift velocity. Figure 1.18 compares this parameter as a function of electric field applied for several materials: Si, GaAs, InGaAs, InP. For low electric fields GaAs reveals a velocity drift value much higher than Si. In GaAs a maximum is achieved for electric fields of 5kV/cm, reaching a value of almost $1.8x10^7$ cm/s. If a higher electric field is applied drift velocity decreases until it reaches a constant value of about $1x10^7$ cm/s. Figure 1.18 shows as, for low electric fields, InGaAs is characterized by a lower drift velocity. In Si drift velocity values are much lower than in GaAs. Differently from GaAs, in Si the drift velocity increases with a constant trend as a function of the electric field applied until it saturates when electric fields values higher than 20kV/cm are imposed. No significant difference is established between drift velocity value measured in GaAs and GaN for higher electric fields. In both the cases a drift velocity of $1x10^7$ cm/s is evaluated.

Despite in many applications GaAs has shown better performances than Si, in many fields it has been overcome by GaN due its better properties. GaN is characterized by a breakdown electric field about one order of magnitude higher than GaAs ($3MV/cm^2$ and $0.4MV/cm^2$ respectively), making GaN preferable than GaAs for several high power applications. This

aspect is confirmed by the Johnson's figure of merit already defined in the explanation of GaN main properties. Gallium nitride is characterized by a figure of merit two order of magnitude higher than the one measured in gallium arsenide or silicon, confirming its high performances. Finally GaN has a very good thermal conductivity, similarly to Si. In both the cases GaN has a thermal conductivity one order of magnitude lower.

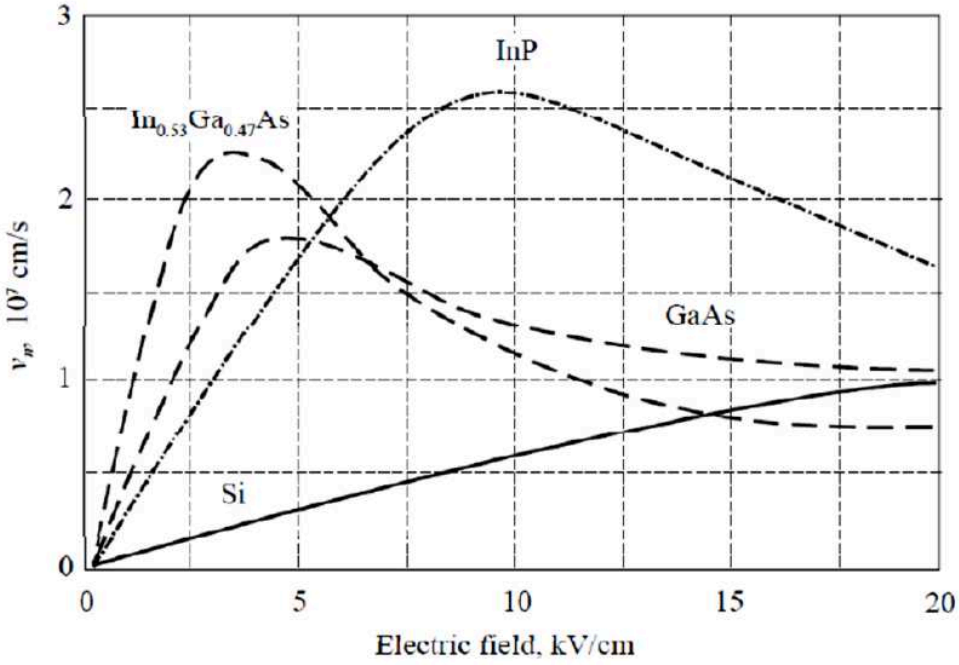


Figure 1.18: drift velocity as a function of electric field for several materials

1.3 Growth techniques

There are several techniques for the growth of gallium nitride on sapphire or silicon carbide substrates. The main goal is to provide a hetero-junction with a low number of defects. The research for improved GaN growth techniques reveals the importance of growing a structure which shows a low strain value and introduces no variation in GaN main properties, although the strong lattice and thermal mismatch between GaN and substrates used and the high temperatures required. HVPE, OMVPE, MBE are the main growth methods used for nitrides. Although HPVE is still used to produce thick GaN layers, OMPVE and MBE are probably the primary methods employed for the production of optoelectronic devices (especially OMPVE) and FETs .

1.3.1 MOCVD or OMVPE (OrganoMetallic Vapor Phase Epitaxy)

VPE has been widely employed for the growth of semiconductor structures. On the basis of the sources used many growth categories are established. Organometallic Vapor Phase Epitaxy is used in the case that a part of the sources are organic in nature. Thus, Ga, Al and In are formed by correspondent metallorganic compounds. One of the major advantages of OMVPE is that several semiconductor compounds from GaN to pure AlN are achievable by using OMVPE method.

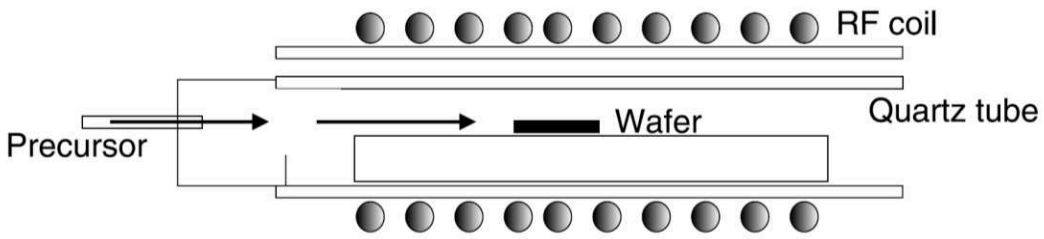


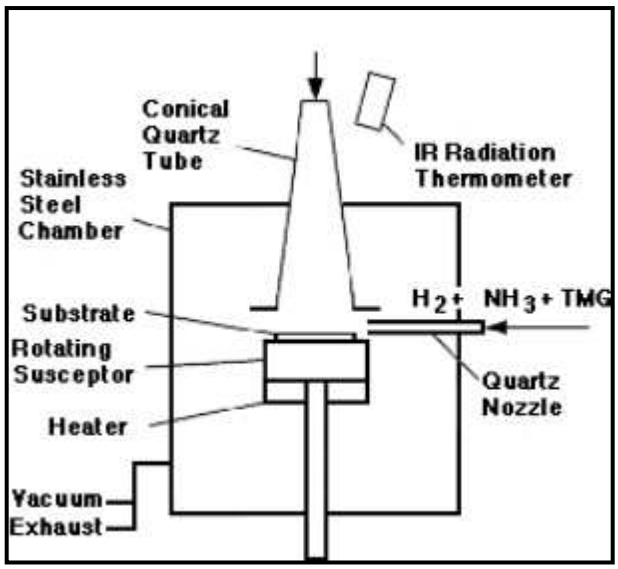
Figure 1.19: OMVPE method scheme [10]

The OMVPE (OrganoMetallic Vapor Phase Epitaxy) is a growth technique which involves gaseous reactants and a heated substrate which react chemically forming a semiconductor [1]. In the case of GaN generation the precursors mainly consist on gallium Trimethyl-Gallium

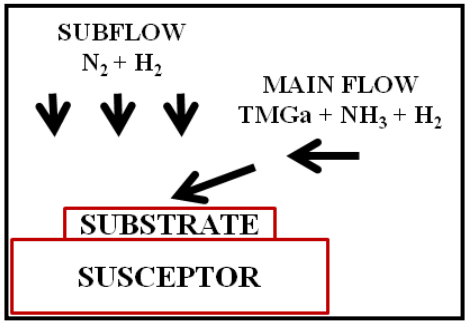
(TMGa), Trimethyl-Aluminium (TMAl) and Trimethyl-Indium (TMIn). Through their reaction with ammonia (NH_3) on the hot substrate the semiconductor is formed. In this case additional sources, such as nitrogen, silane (SiH_4), disilane (Si_2H_6) and biscyiclopentadienyl magnesium are needed (Cp_2Mg) [10] (Figure 1.19). The metallorganic compounds are carried by a gas, usually hydrogen, whose percentage depends on the pressure values [10].

In the GaN condition main reaction for the substrate growth is (1.6). For the AlN formation the same reaction is used with gallium replaced by aluminium [9]. The OMVPE technique is carried out with high velocity values and high temperatures. A temperature higher than 1000°C is usually applied to grow the structure: the substrate is put on a graphite support and heated at about 1050°C, the temperature is then decreased at about 450°C to grow the buffer layer and finally increased for the GaN growth [1].

$$Ga(CH_3)_3(v) + NH_3 \rightarrow GaN(s) + 3CH_4(v)(l) \qquad (1.6)$$



(a)



(b)

Figure 1.20: (a) Reactor and (b) operating scheme of the two flow OMPVE technique [9]

Main advantages of this technique are the high precise growth for III-V materials and the high velocity with which the layer is deposited on the substrate (typical growth rate is $2\mu mh^{-1}$) [1]. However this method has some negative aspects: as a consequence of the low electrons concentration a mobility value lower than the one reached with other methods is obtained. Furthermore, for some materials such as InGaN it is not possible to grow uniform layers, neither if characterized by a low thickness [9]. The low mobility value has been partially solved with the two flow OMVPE technique [10], described in Figure 1.20: two flows, one parallel and one perpendicular to the substrate is used [1]. The parallel flow is composed by trimethyl gallium (TMGa), ammonia (NH_3) and H_3. The perpendicular flow is constituted by nitrogen and hydrogen compounds, N_2 and H_2 respectively. With this solution the secondary (perpendicular) flow induces the primary (parallel) flow direction toward the substrate [1].

1.3.2 MBE (Molecular Beam Epitaxy)

The MBE (Molecular Beam Epitaxy) is an important technique for III-V materials growth. The growth depends on the reaction between thermal energy beams of the constituent elements of molecular, atomic or ionized typology and a heated substrate [9]. The reaction occurs in a ultrahigh vacuum.

In the case of gallium nitride and aluminium nitride the III materials (in this case Ga or Al) come from effusion cells sources. Because of the high binding energy of N_2 it is impossible to provide an elemental group V N source [9]. Nitrogen can be generated by RF plasma or ammonia sources contained in separated cells. During the growth substrates are usually rotated with a constant trend in order to obtain a better uniformity [9]. The operating scheme of the a MBE chamber is shown in Figure 1.21, according to [9]. RHEED (Reflection High Energy Electron Diffraction) is a measurement of the state diffraction carried out by means of an electronic beam [1]. During the growth the pressure is kept lower than 10^{-11} mbar while the GaN growth temperature amount about at 800°C, much lower than the one applied during HPVE or OMPVE technique [1].

Low performances are reached by GaN when grown directly on sapphire or SiC substrate. As a consequence it is necessary to introduce a buffer layer (generally Al) grown by different methods such as OMPVE between the substrate and GaN layer. Main advantages of the MBE technique are provided by the higher precision defined at the interface and by the higher polarity flexibility. MBE method can use shutter which, by reflection of molecular beams, allows an optimal control of the epitaxial layer composition and a constant monitoring of the superficial structure during the growth. Consequently to the precision provided by the presence of a shutter

and to the low temperatures applied for the growth it is possible to grow layers thicker than with OMPVE technique.

On the other hand MBE technique has many disadvantages. The low temperature applied leads to a growth characterized by a lower rate than OMPVE and HPVE technique. MBE is usually characterized by a rate of 0.5-1μmh^{-1} while OMPVE has a common rate of 2μmh^{-1}. Finally MBE technique requires a condition of high vacuum, which does not allow the introduction of high dopant values in the structure [9].

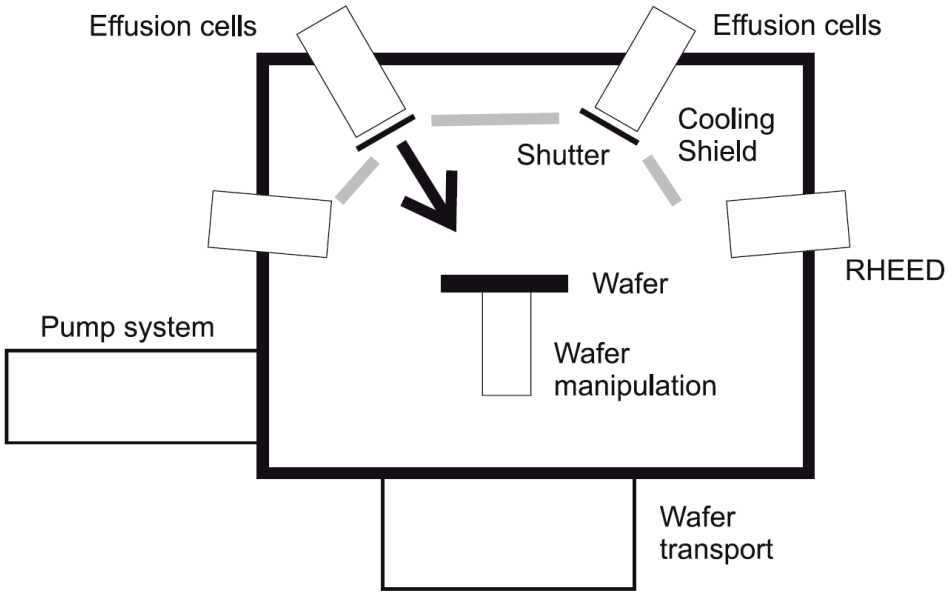


Figure 1.21: MBE (Molecular Beam Epitaxy) chamber [9]

1.3.3 HVPE (Hydride Vapor Phase Epitaxy)

The term Hydride Vapor Phase Epitaxy is used when a hydride source is employed for the element belonging to the V group. HVPE has been overcome by different techniques as a consequence of several issues demonstrated: difficulties related to uniform seeding of GaN on sapphire, high n-type background doping, large defect concentration and inability to produce p-type GaN for light emitters.

In HVPE different precursors are used for the material belonging of the III and V group. In the first case chlorides generated by flowing hydrogen chloride gas over liquid metal in a quartz tube are used. In the second case hydrides precursors are employed [9] (please refer to (1.7)). In GaN case precursors of III and V group are GaCl and NH_3, respectively. GaCl is generated through the reaction of HCl gas with molten Ga. The transport of GaCl (in vapour phase) is provided by a carrier gas (hydrogen or inert gas). Reactor chamber is surrounded by high purity

quartz tube and kept at the atmospheric pressure [9] (Figure 1.22). A furnace with multiple zone where a different temperature and pressure can be set is used. In the case reported (Figure 1.22) a different temperature should be kept in the metal source and substrate zone. Further all the precursors, such as chlorides and hydrides, should be kept with a different pressure.

A HPVE technique for GaN uses the reaction between GaCl, formed by HCl and Ga, and NH3 [9], as described in (1.7).

$$\begin{aligned} 2Ga(l) + 2HCl(g) &\rightarrow 2GaCl(g) + H_2(g) \\ GaCl(g) + NH_3(g) &\rightarrow GaN(s) + HCl(g) + H_2(g) \end{aligned} \qquad (1.7)$$

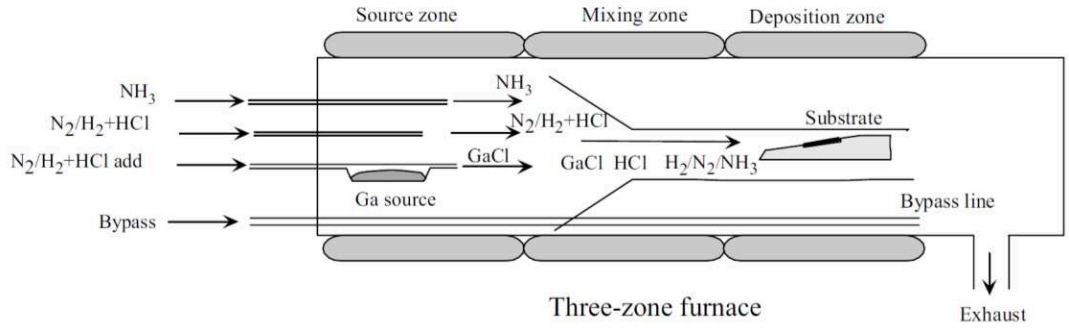


Figure 1.22: three zone furnace for nitride growth with ammonia and Ga sources

Chapter 2: An overview about devices: HEMT and Power Amplifiers

2.1 HEMT (High Electron Mobility Transistors)

HEMT (High Electron Mobility Transistors) are field effect transistors composed by a hetero-junction. This structure, called also HFET (Heterojunction Field Effect Transistor) or MODFET (Modulation doped Field Effect Transistor) is composed by semiconductors with a usually high energy gap value. In HEMT the channel is produced by the creation of a bidimensional electron gas (2DEG) through the confinement of the electrons in a triangular quantum well. The creation of the quantum well can be obtained by means of the modulation doping concept or exploiting the charge due to the piezoelectric and spontaneous polarization at the interface.

(i) One of the most important characteristics of HEMTs is their high mobility value. Differently from MESFET in HEMT the charge is not provided by dopants in the channel, thus avoiding scattering phenomenon with dopants. As a consequence the mobility in HEMT faces a significant increase and it is limited mainly by phonon scattering. For this reasons the improvement of mobility leads to a significant reduction of the source resistance (low access resistance) in HEMT but it does not determine any meaningful improvement of the transport at high fields consequently to its high correlation with phonon scattering when high electric fields are applied. (ii) Furthermore HEMTs can reach a high sheet carrier density on the basis of defined parameters, such as the doping density in the large bandgap material if modulation doping concept is used to create the bidimensional gas and the polar charge at the interface by using, for instance, semiconductors with different properties. (iii) In HEMT, as a consequence of the thin region which can be used as active channel, it is possible to use materials with high mobility without introducing a relevant number of defects. An example is provided by GaAs devices, where it is possible to use materials with very high electron mobility such as InGaAs on GaAs or InP substrate. (iv) Finally HEMT can reach high performances at low temperatures due to the avoiding of the carrier freezeout since carrier have an energy lower than the donor level in the semiconductor with higher energy gap.

As a consequence of the advantages explained HEMT can reach high voltage and current levels, thus allowing the use of HEMT for applications which require high power. Furthermore HEMT, consequently to their high mobility and carrier velocity can reach significant performances in high frequency applications.

2.1.1 Fundamentals about HEMT

An High Electron Mobility Transistor is defined by a hetero-structure composed by a buffer layer where a further layer, called barrier layer, is grown (Figure 2.1). To better understand the device principles of operation an AlGaAs/GaAs structure, defined through modulation doping, is firstly described (Figure 2.1). An undoped GaAs layer (called buffer layer) is grown on a semi insulating GaAs substrate by means of MBE or OMPVE technique. To create the hetero-structure an undoped AlGaAs is firstly deposited with the role of spacer layer; then a strongly doped AlGaAs layer is deposited. A Schottky gate contact and ohmic source and drain contacts are finally deposited (Figure 2.1).

As a consequence of doping in the barrier layer the electrons flow from the barrier layer to the buffer layer, thus creating a triangle quantum well as a consequence of the band bending. The channel is created by the electrons confined in the quantum well which are free to move in two dimensions but confined into the growth direction. The channel, also called bidimensional electron gas or 2DEG, allows the passage of a large amount of current, as a consequence of the electrons high mobility and of the reduction of scattering due to the physical separation between the electrons in the channel and the dopants in the barrier layer.

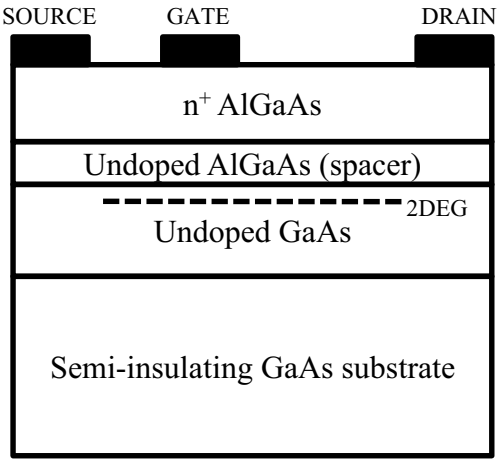


Figure 2.1: Schematic of an AlGaAs/GaAs structure

There are several ways to dope the barrier layer. As shown in (Figure 2.2), it is possible to dope the barrier layer except for a thin layer called spacer layer. Otherwise it is possible to use the so called delta doping structure: a very thin layer is strongly doped but it is separated from the channel by a large undoped AlGaAs layer, as described in (Figure 2.3). The importance of the use of a delta doping relies in the possibility of reaching a high amount of charge in the channel.

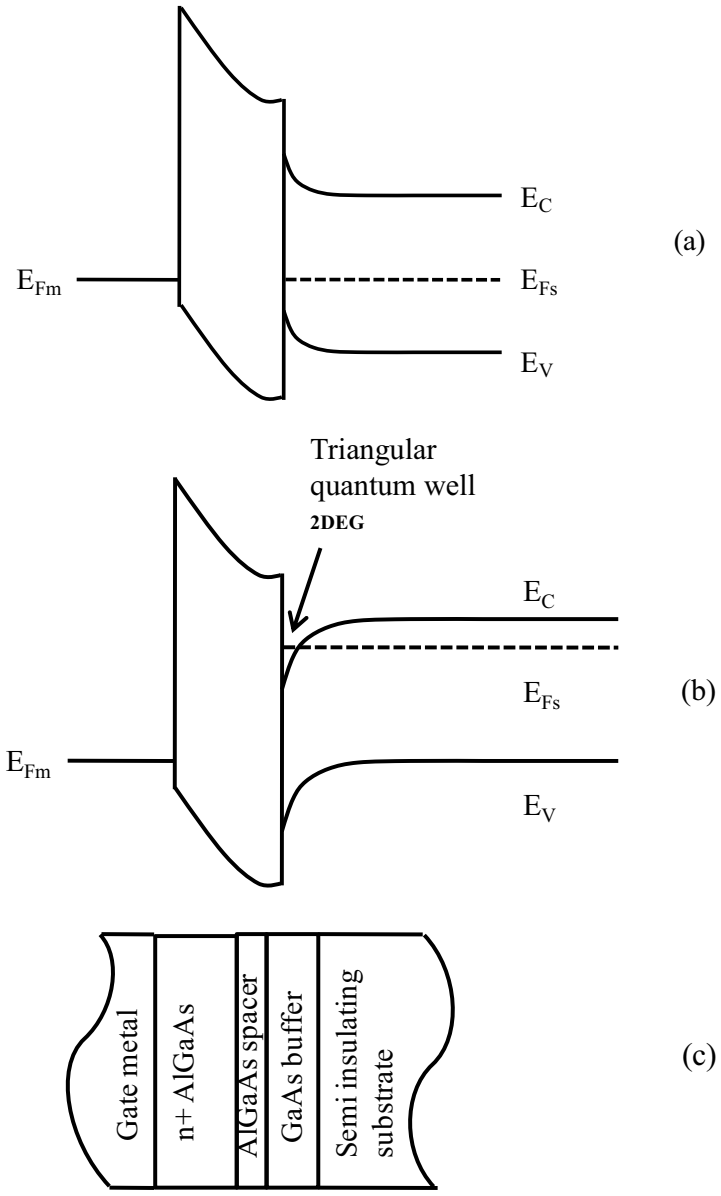


Figure 2.2: band diagram of a HEMT at (a) thermal equilibrium and at (b) threshold voltage. (c) correspondent schematic of an HEMT

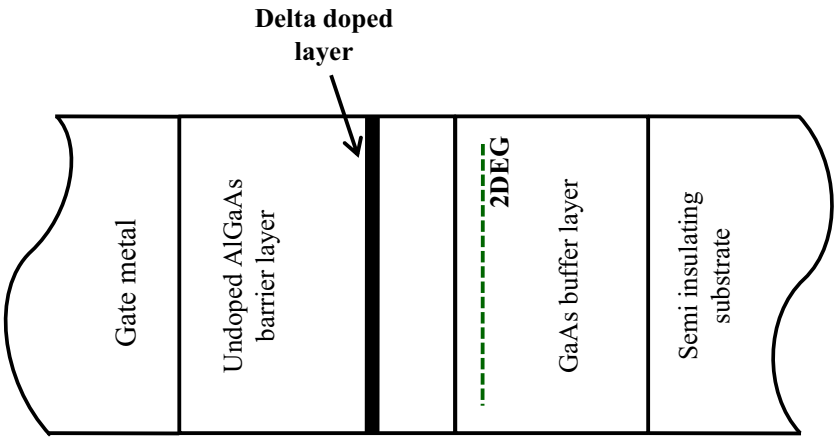


Figure 2.3: schematic of a delta doped structure

2.1.2 Pseudomorphic HEMT

A typical AlGaAs/GaAs structure usually employs the modulation doping concept. The growth of an n doped large bandgap material (n AlGaAs) over an undoped channel material (GaAs) leads to the generation, in the doped material, of electrons which flow in the undoped material, thus avoiding the carrier transport properties degradation due to scattering with doping impurities. The AlGaAs/GaAs structure is defined "lattice matched" since the AlGaAs and GaAs similar lattice constant does not lead to the creation of strain in the device.

The degradation of device performances revealed in AlGaAs/GaAs structures at moderate and high current levels led to the development of a different structure to improve the electron mobility and device's performances. In detail, above a defined carrier density a part of channel charge can move into the AlGaAs layer, as a consequence of the small conduction band discontinuity in AlGaAs/GaAs structures. In the 80s studies reported in literature presented an innovative solution to avoid this issue, consisting in the introduction of a Indium percentage in the GaAs buffer layer due to the InGaAs material smaller effective mass. This approach led to the generation of a pseudomorphic AlGaAs/InGaAs heterostructure (Figure 2.4).

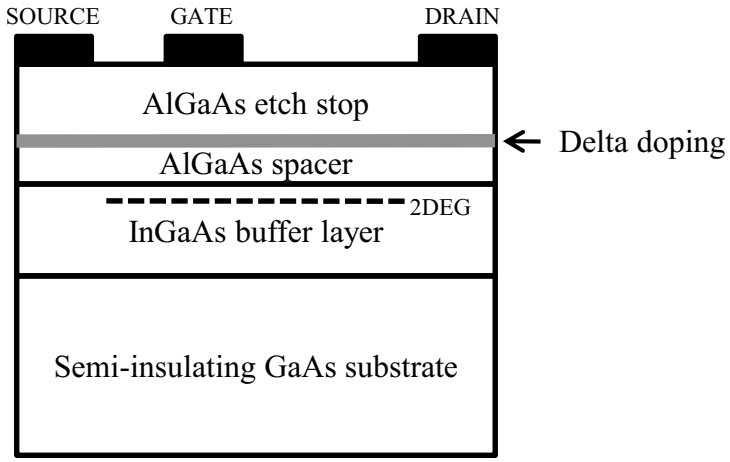


Figure 2.4: Schematic f a pseudomorphic AlGaAs/InGaAs HEMT with delta doping

The so called pseudomorphic HEMT (or pHEMT) is usually composed by a InGaAs buffer layer grown on a GaAs or InP substrate (Figure 2.4); the barrier layer can be composed by a AlGaAs or by a InAlAs barrier layer. The different AlGaAs and InGaAs lattice constant determines a device which is not lattice matched, neither between the barrier and the buffer layer, nor between the barrier and the substrate, resulting in a strained structure.

The pHEMT structure can reach better performances as a consequence of two main properties. Firstly the InGaAs has a narrower bandgap than GaAs resulting in a larger discontinuity in the conduction band. Therefore a better electron confinement is obtained

leading to a higher 2DEG density and limiting the possibility that the carriers spill into the AlGaAs layer at moderate and high current. The higher electron confinement leads to an increase of the drain current value and to the achievement of a lower source resistance. Furthermore the InGaAs is characterized by a higher mobility value than GaAs, determining better transport properties of the carriers in the channel (Figure 2.5). This aspect leads to an improvement of the transconductance value and of the modulation efficiency.

Unfortunately, since InGaAs has a larger lattice constant than GaAs, In content must be limited to avoid defects creation [12]. According to previous works reported in literature, pHEMTs on GaAs substrate can be characterized by a maximum of 35% Indium even if a percentage of almost 20% is usually preferred [13]. On the contrary unstrained pHEMTs on InP substrate usually have a In content of 53%, even if pHEMTs can contain as high as 80% [12] [13]. Despite the higher performances, pHEMTs on InP substrate are usually avoided because of the high growth cost and the high possibility of breakage during processing.

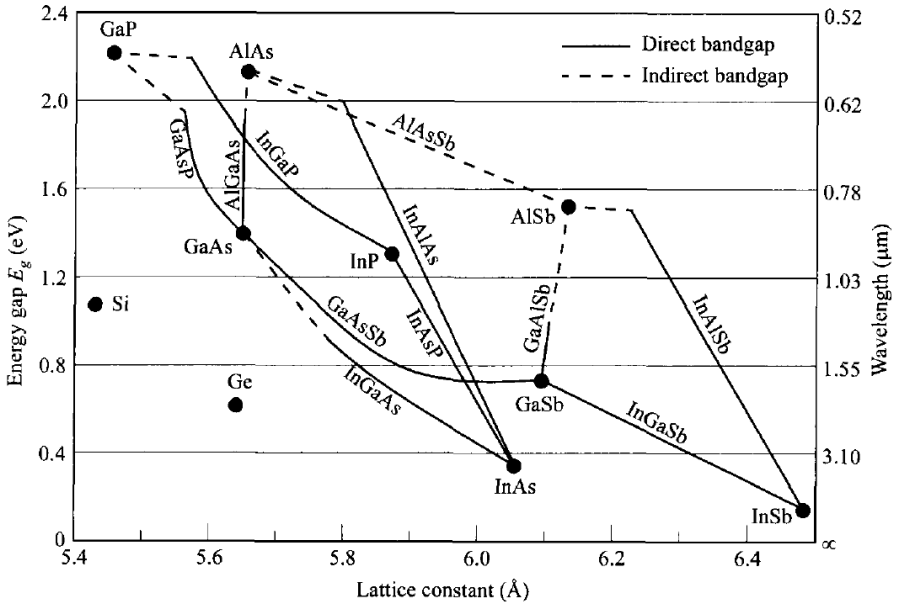


Figure 2.5: Energy gap vs lattice constant for some common elementary and binary semiconductors [1]

2.1.3 Polar materials and structures (AlGaN/GaN HEMTs)

An HEMT is an heterostructure composed by two different semiconductors, called buffer and barrier layer respectively. According to the previous section a HEMT can be made by using an AlGaAs/GaAs structure through the creation of a 2DEG by means of the modulation doping concept. The 2DEG can otherwise be formed by charge induced at the heterointerface by

spontaneous and/or piezoelectric polarization, without introducing any doping in the buffer or in the barrier layer. An example is provided by AlGaN/GaN High Electron Mobility Transistors. The use of AlGaN/GaN to generate the heterostructure is also due to the peculiar properties of gallium nitride previously described which allow a high carrier concentration in the channel despite the absence of modulation doping.

In an AlGaN/GaN HEMT two typologies of polarization are noticed: spontaneous and piezoelectric polarization. The spontaneous polarization can appear in all the structures, even if no strain is reported, as a consequence of electrons not uniform distribution. In AlGaN/GaN HEMTs the spontaneous polarization appears both in the buffer and in the barrier layer, although a higher contribution is noticed in the AlGaN layer due to the Al content. The orientation of the spontaneous polarization depends on the polarity of the GaN surface. In the case of the Ga face polarity (Figure 2.6a) the orientation of the spontaneous polarization is toward the substrate; in the case of N face polarity (Figure 2.6b) has opposite orientation [13].

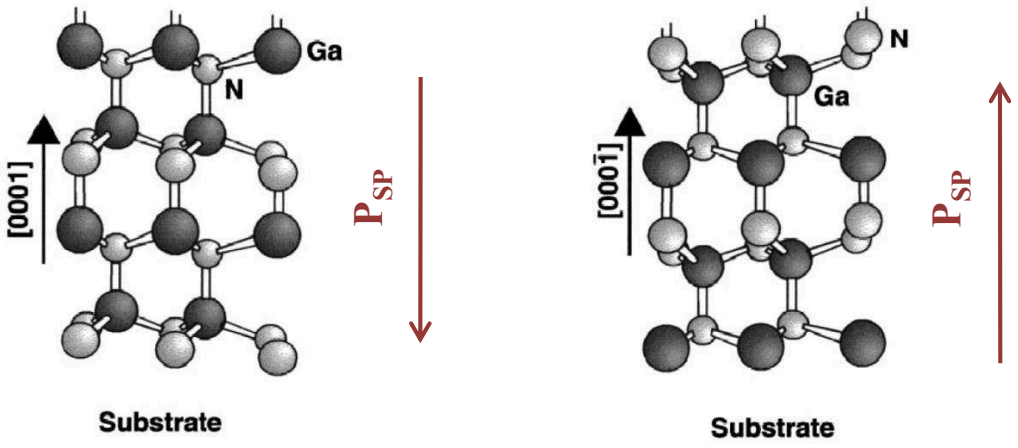


Figure 2.6: Wurzite structure of GaN and correspondent spontaneous polarization in a crystal with Ga face (a) and N face (b) [13]

A detailed study has been carried out by Dimitrov et al. [14] to explain the different localization of the 2DEG in the structure on the basis of the polarity of the GaN surface. In the first case an N face polarity has been considered while in the second case a Ga face polarity has been reported. According to the study of Dimitrov et al. the surface polarity can be chosen by introducing an AlN nucleation layer between the substrate and the buffer layer (Figure 2.7). In the case reported a sapphire substrate and a GaN buffer layer have been used. A nucleation layer, usually composed by AlN, can also be introduced between the substrate and the buffer layer with the aim of reducing the mismatch between the substrate and the buffer layer to avoid the generation of defects. In some cases it can also be used between the buffer and the barrier layer with the aim of enhancing the carrier confinement to increase the mobility.

Figure 2.7: Study of the 2DEG localization on the basis of GaN face polarity

The piezoelectric polarization is created by the strain generated when the barrier layer is grown on a semiconductor with a different lattice constant. The polarization is correlated with the strain and, thus, with the lattice mismatch reported. In the polar material structures the barrier layer (AlGaN) is strained at the edge both with the gate metal, both with the buffer layer. Consequently a charge (P_{PZ}) is created at both the edges of the barrier layer and compensated, respectively, by a charge density at both interfaces with metal and buffer layers. The orientation of the piezoelectric polarization is opposite to the spontaneous polarization if the heterostructure is characterized by a compressive strain (Figure 2.8). In the case of a AlGaN barrier layer grown on a GaN buffer layer a tensile strain is reported at the heterointerface; the total polarization is defined by the sum between the piezoelectric and spontaneous polarization. The different cases above reported are described in Figure 2.8, according to [15]

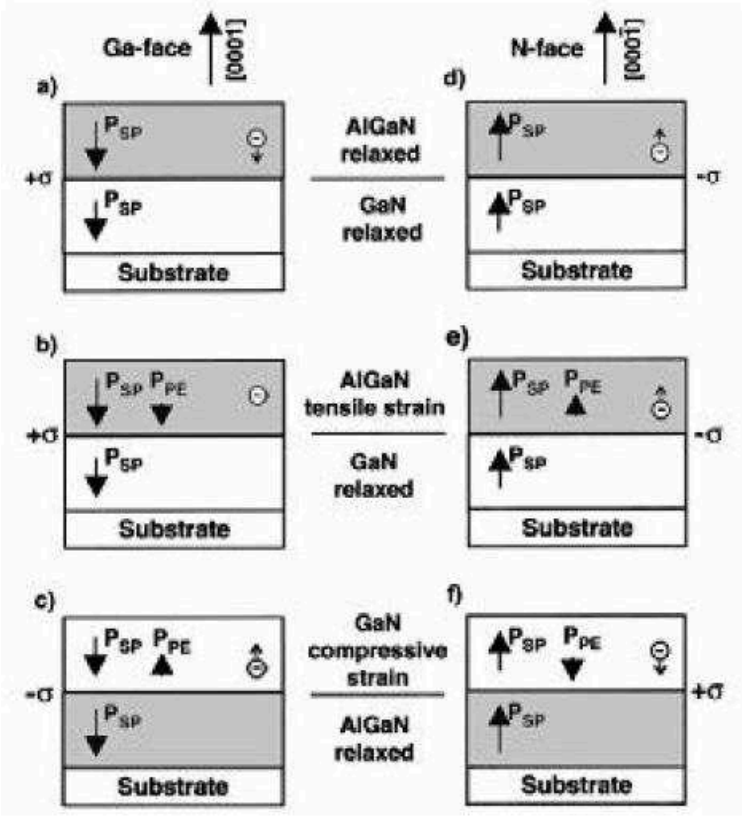


Figure 2.8: Piezoelectric and Spontaneous polarization with Ga face and N face polarity [15]

When an AlGaN barrier layer is grown over a GaN buffer layer with Ga face polarity the charge created at the interface by the sum of piezoelectric and spontaneous polarization leads to the band bending and to a high concentration of carriers in the triangle quantum well generated, although no doping has been introduced in the structure, determining a significant 2DEG. The difference in the conduction band discontinuity evaluated as a function of depth without polarization, with only piezoelectric polarization and with both typologies of polarization is shown in Figure 2.9. It is possible to notice that a significant quantum well is generated only when both spontaneous and piezoelectric polarization characterize the device.

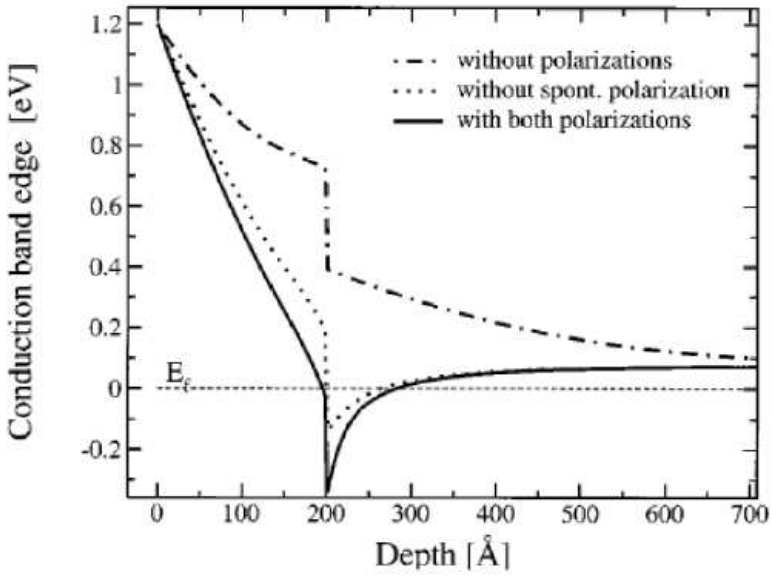


Figure 2.9: Conduction band edge when different polarization characterize the device

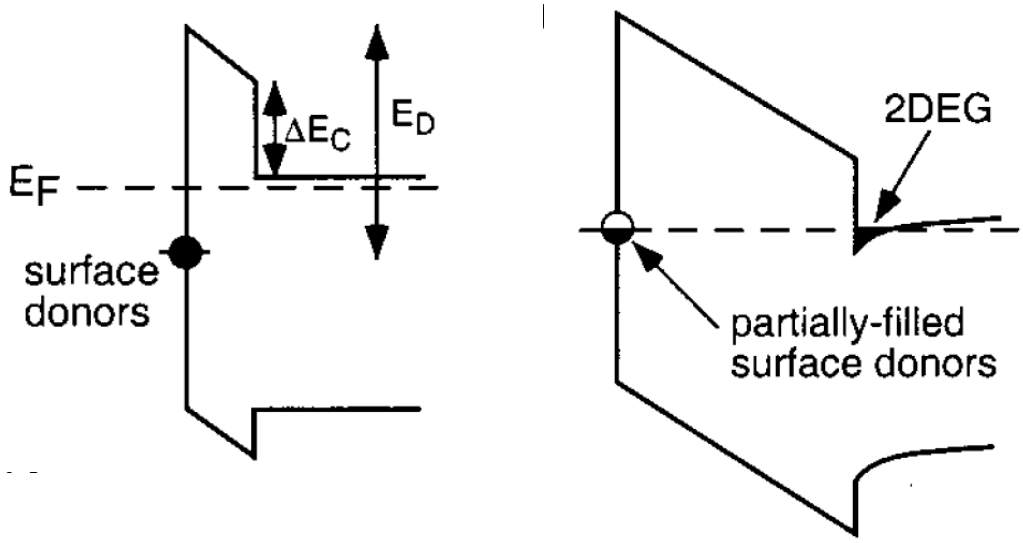


Figure 2.10: (a) AlGaN barrier layer thickness lower (a) and higher (b) than the critical value [16]

An explanation of the origin of the carriers in the 2DEG has been suggested by Ibbetson et al. [16]. Electrons are provided by surface states (Figure 2.10a). After the generation of a triangular quantum well due to the band bending determined by a significant strain induced polarization the electrons move from the surface states to the quantum well determining the 2DEG, as explained by Figure 2.10b. Ibbetson et al. suggest that a critical AlGaN layer thickness is necessary to create the 2DEG. When the barrier layer thickness is higher than the critical value the surface donor levels is under the Fermi level and electrons can migrate to the quantum well created forming the 2DEG (Figure 2.10).

Figure 2.11 reports the bidimensional sheet charge density as a function of barrier layer thickness. The analysis is the result of the experimental data reported by Ibbetson et al. in [16]. The charge density strongly increases until a AlGaN thickness of about 15nm is reached. For higher AlGaN thickness values the density saturates to a constant value.

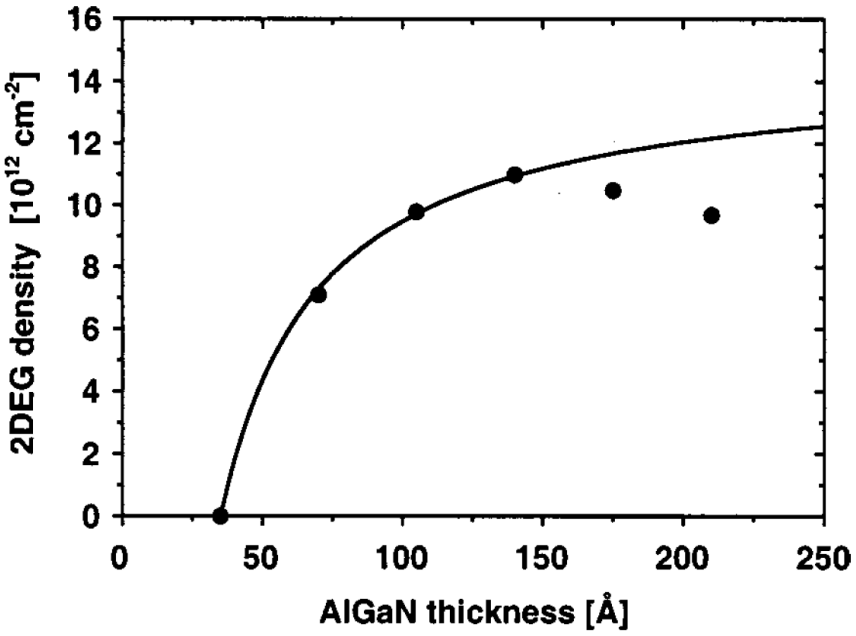


Figure 2.11: charge density as a function of barrier layer thickness [16]

It is essential to remark the importance of the Al content in the charge sheet density due to the dependence between the conduction band discontinuity and the Al percentage. On one hand the Al content increases the piezoelectric effect, thus increasing the charge sheet density in the structure. On the other hand if a Al percentage higher than 40% is used the AlGaN becomes an insulating layer. Figure 2.12 shows the increase of charge sheet density as a function of Al more fraction and barrier layer thickness, confirming that the density increases with both the aspects. The increase of the charge sheet density in Figure 2.12 is reported for several thickness: (1)

30nm, (2), 20nm, (3) 10nm, (4) 5 nm [18]. The thicker line represents the density variation for a thickness corresponding to the critical value for the creation of the 2DEG.

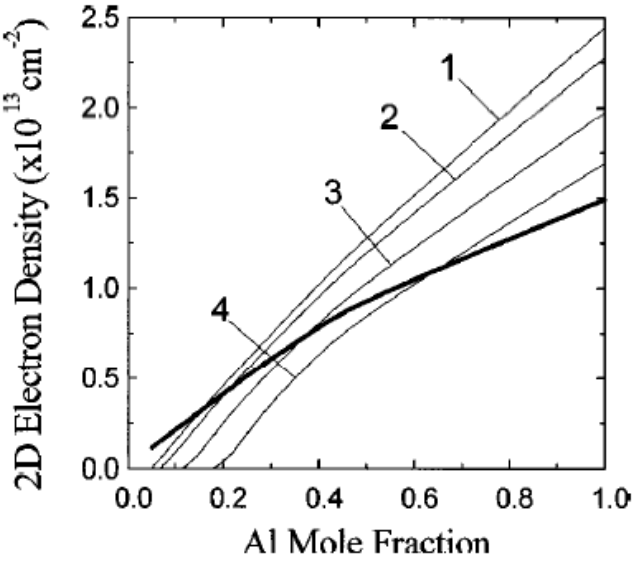


Figure 2.12: charge density as a function of Al mole fraction for several barrier layer thickness (from 5nm to 30nm and for the critical value) [18]

2.1.4 Ohmic and Schottky contacts

Two typologies of metal contacts are used in the HEMTs: a Schottky rectifying contact for the gate terminal and ohmic contacts for the drain and source terminals.

The Schottky rectifying contact is obtained through the deposition of a metal contact on the barrier layer. In this case the aim is to provide for a good channel control through the gate terminal avoiding the flowing of the leakage gate current. The reduction of the gate leakage current is usually obtained by using materials with a high work function. Furthermore the use of an alloy to create the Schottky contact is preferable to improve the thermal stability, especially in the case of GaAs structures, where the metal interdiffusion consequent to thermal aspects is an important issue which affect device stability and causes irreversible degradation.

In the case of GaAs pHEMTs gate metallization consists of a multilayer structure which needs to satisfy the following aspects, as previously explained: (i) provide a good adhesion of the contact to the semiconductor, (ii) obtain an adequate Schottky barrier height to avoid leakage gate current, (iii) reach a good stability against interdiffusion and electromigration effects. It is therefore preferable to use an alloy with materials such as Ti and Au with the aim of improving the thermal stability of the device and the contacts conductivity, respectively. In the contact layer the top gold layer is usually separated by a barrier metal layer, preventing or limiting the Au interdiffusion. In literature several gate stack have been proposed to satisfy the

aspects above. The most reliable layers are provided by the following schemes: Ti/Au, Ti/W/Au and Ti/Pt/Au. As a consequence of the material properties and results obtained in works previously reported in literature the last scheme is the most diffused. To avoid the metal semiconductor interdiffusion several approaches have been reported in literature. The most common solution implies the use of a refractory metal, such as W or WSi and WSiN as interdiffusion layer in the metal stack.

In the case of AlGaN/GaN HEMTs interdiffusion and electromigration effects are much lower than in GaAs pHEMTs. The gate stack is usually composed by materials which are characterized by a high work function in order to obtain a high barrier height value and to reduce the leakage gate current. According to Table 2.1 materials with a high work function, such as Ni ($\Phi_m = 5.15\ e$V), Pl ($\Phi_m = 5.65\ e$V), Pd ($\Phi_m = 5.12\ e$V), are adopted.

The ohmic contact is used for the source and the drain terminals. As a consequence it is important to obtain a contact with a low resistance in order to allow the carrier flow and to enhance the device conductance. In the case of both GaAs pHEMTs and AlGaN/GaN HEMTs alloys are preferred in order to obtain a contact resistance as low as possible. With the same aim it is important to choose materials with a low work function.

In the case of GaAs pHEMTs ohmic contacts are usually based on Au/Ge/Ni alloying to reach low source and drain parasitic resistances. Unfortunately the choice of the ohmic contact stack in GaAs based technology is very important as a consequence of the parasitic resistances increase which faces the structure consequently to thermal induced degradation.

	Work function (volt)
Ag (Silver)	4.26
Al (Aluminum)	4.28
Au (Gold)	5.1
Cr (Chromium)	4.5
Mo (Molybdenum)	4.6
Ni (Nickel)	5.15
Pd (Palladium)	5.12
Pt (Platinum)	5.65
Ti (Titanium)	4.33
W (Tungsten)	4.55

Table 2.1:, work function value in common metals [13]

In AlGaN/GaN HEMTs ohmic contacts stacks are usually composed by a Ti layer, according to its low work function ($\Phi_m = 4.3\ eV$), which is directly deposited on the semiconductor. Many solutions include the use of a Al layer or the use of different schemes such as Pt/Au, Ni/Au, Ti/Au. The analysis of the current value as a function of voltage in a ohmic contact composed by different materials, demonstrates that a low contact resistance is reached through the use of a Ti/Al gate stack. Previous works reported in literature demonstrate that the use of gate stacks such as Ti/Al/Ni/Au, Ti/Al/Ti/Au or Ti/Au/Nb/Au, allow the achievement of a low source and drain resistance value.

	Resistivity (μΩ-cm)
Aluminium Al (bulk)	2.7
Al (thin film)	0.2-0.3
Al alloys (%Si)	+0.7% Si
Al alloys (%Cu)	+0.3% Cu
Titanium (Ti)	40
Tungsten (W)	5.6
Ti-W	15-50
Gold (Au)	2.44
Silver (Ag)	1.59
Copper (Cu)	1.77
Platinum (Pt)	10
Silicides (PtSi)	28-35
Silicides (NiS_2)	50

Table 2.2: Resistivity for some materials used [13]

2.2 Power amplifiers

2.2.1 Fundamentals about power amplifiers

A power amplifier is an amplifier designed to reach the maximum output for a given input signal. A block diagram of a basic one stage RF power amplifier is provided in Figure 2.13. In the case proposed the power amplifier is composed by a transistor (in this case a MOSFET), an output network, an input network and an RF choke. A power amplifier can be composed by one or several stages on the basis of the output power and gain needed.

A power amplifier can operate in three main conditions: (i) as dependent current source, (ii) as a switch, (iii) in overdriven mode, i.e. partially in the first and partially in the second condition [19].

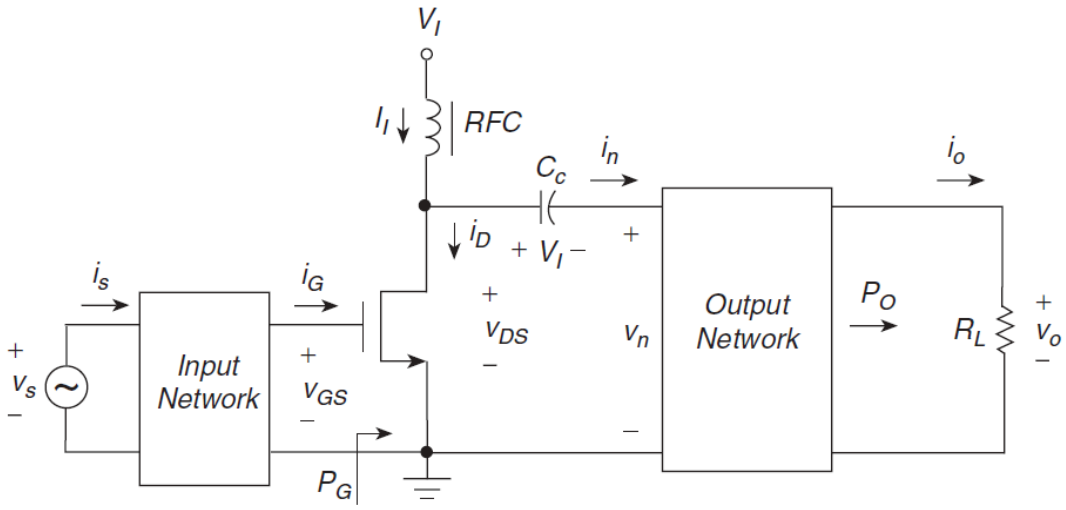


Figure 2.13: Block diagram of a RF power amplifier [19]

In the first case the drain current signal is determined by the gate to source voltage signal and the transistor operating point. The drain voltage signal is determined by the dependent current source and load network impedance. In this case the transistor has to operate in the saturation region. This condition is suitable for linear power amplifiers. Indeed the drain current and drain source voltage are proportional to the gate source voltage signal.

In the second case the switch voltage can be considered as negligible when the switch is on, leading to the determination of the drain current by the external circuit as a consequence of the

switching action of the transistor. On the other hand, when the switch if off, the drain current can be considered as negligible and the switch voltage is defined by the external circuit response. In this case the transistor should operate in the ohmic region, i.e. with a drain source voltage lower than the difference between gate source voltage and threshold voltage when the switch is on and in the cut-off region when the switch is off. Differently from the first case, when the transistor operates as a switch the drain source voltage and current value is not dependent to the gate source voltage. It is usually applied a rectangular gate to source voltage or a sinusoidal signal when high frequencies are considered. One of the most important advantages of using the power amplifier as a switch is mainly due to its high amplifier efficiency and low power loss.

In the last condition (overdriven condition) a sinusoidal voltage signal with high gate source voltage value is usually applied. In this case, it operates in the active region when the instantaneous values of gate source voltage are low and as switch when the instantaneous gate source voltage values are high.

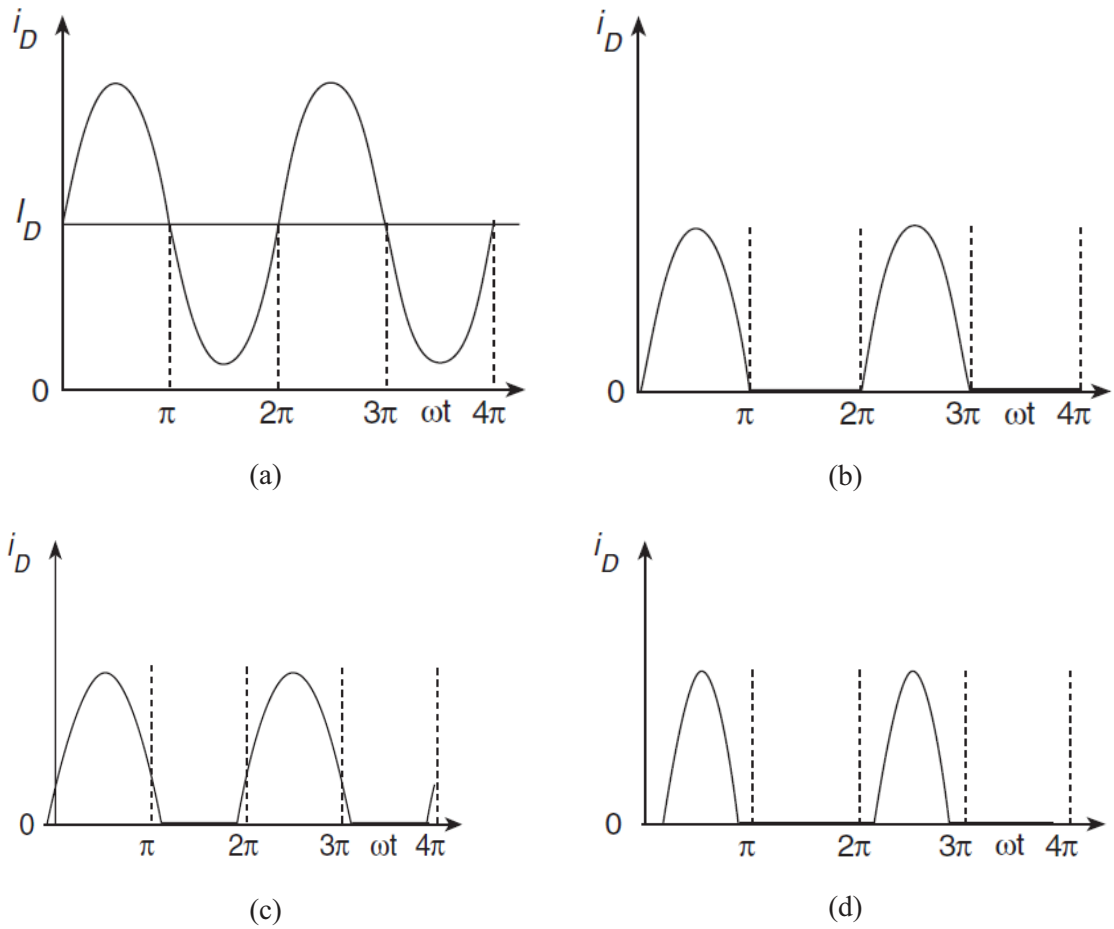
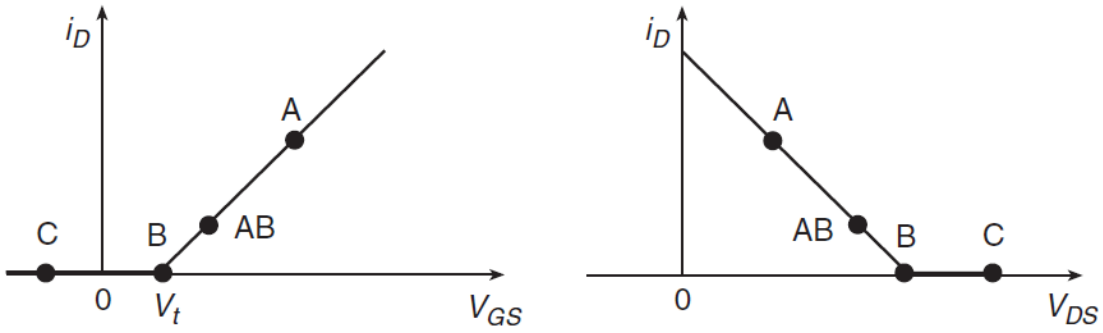


Figure 2.14: drain current value in amplifier of class (a) A, (b) B, (c) AB, (d) C

RF power amplifiers which work as a dependent current source are classified on the basis of the conduction angle $2\vartheta$of the drain current. Drain current trend for different class of power amplifiers, respectively class A, B, AB and C, are represented in Figure 2.14, while in Figure 2.15 the operating point, both considering drain current and gate source voltage, is shown.

In a class A power amplifier the period of the drain current is 2π. In this class of amplifier the operating point is characterized by a gate source voltage value higher than the threshold voltage. Thus, since the ac gate source voltage must be higher than the threshold voltage it is important to choose a dc gate source voltage quite higher, as shown in Figure 2.15. The transistor conducts during the whole cycle as a consequence of the higher value of the drain current measured in ac than the one in dc. The device is kept in the "quasi-linear" region and, to obtain a maximum power performance, the device is supplied with a dc bias current of Imax/2 and an input signal between 0 and Imax. A power efficiency of 50% is reached. Despite the low efficiency class A has some advantages: its linearity, due to the operating point in the quasi linear region, gain higher than different classes, ease of design since it does not require specific harmonic matching [20].



(a) (b)

Figure 2.15: operating point considering (a) VGS and (b) VDS in different classes of power amplifier

Class B, also called "zero bias" power amplifiers are characterized by a period of π. The transistor conducts for half cycle since the gate source voltage measured in dc corresponds to the threshold voltage, leading to a correspondent null dc drain current bias until some input signal is applied. With this condition the dc drain current corresponds to $Imax/\pi$, leading to a correspondent efficiency of 78.5%.

Class AB power amplifier has characteristics similar to A and B power amplifiers. The conduction angle is between π and 2π, with a gate source voltage applied slight higher than the threshold voltage. As a consequence the device is biased with a small drain current value measured in dc condition.

Class C power amplifiers are characterized by a conduction angle lower than π. Thus the transistor conducts for a period lower than half cycle and the drain current measured in dc is null, according to the gate source voltage value which corresponds to the cut-off region. An increase of the efficiency is obtained; such increase can reach a value of 100% for an impulsive current, as demonstrated by Figure 2.19 which shows the efficiency trend as a function of conducting angle. However, the use of a class C power amplifier induces several disadvantages: necessity of an increase of the device periphery, large drive signal required to achieve the maximum voltage and current value as a consequence of the power amplifier operating point in cut-off region, breakdown effects which occur when negative going peaks are achieved, difficulties of design due to harmonic termination [20].

2.2.2 Fundamentals about MMIC technology

MMIC (Monolithic Microwave Integrated Circuit) technology offers a good solution to satisfy the requirements introduced by the use of a power amplifier: high power and efficiency, circuit size reduction, reliability improvements and high volume applications [11]. In MMIC technology both active and passive elements are fabricated together on a semi-insulating GaAs substrate. A three dimensional example of a MMIC power amplifier is shown in Figure 2.16. Especially for high power and breakdown voltage considerations MMIC have shown much higher performances than other structures, such as silicon based RFIC (Radio Frequency Integrated Circuits), based on different technologies such as CMOS, BiCMOS, bipolar.

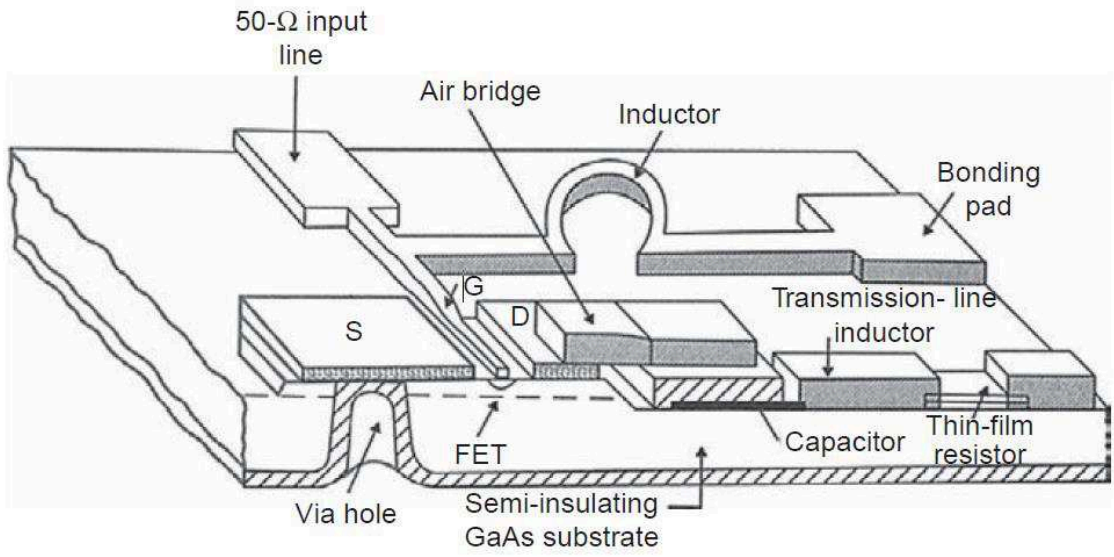


Figure 2.16: three dimensional view of a MMIC power amplifier [11]

MMIC technology found a fast development also thanks to several aspects: (i) GaAs material properties, development of GaAs material technology and application of techniques previously developed for silicon, such as photo and e-beam lithography; (ii) development of structures suitable for high power and high frequency applications, such as HEMTs, HBTs or MESFETs. Furthermore the introduction of pHEMTs device led to the possibility of improving performances if noise figure, power added efficiency, bandwidth and frequency range are considered. MMIC technology has several advantages, especially in millimetre wave applications. The first important aspect is the significant reduction of parasitic effects due to bond wire, as a consequence of the fabrication of both passive and active elements on the same substrate. Further improvements considering device performances include higher gain, especially in multi stages structures, and higher power added efficiency. Furthermore no requirements of external biasing chokes, better unit to unit amplitude and phase tracking are achieved. MMIC technology introduces improvements not only in terms of device performances but also considering device fabrication, for instance lower costs, improved reproducibility and high volume manufacturing capability. Further improvements are provided by the smaller size and weight and by the circuit design higher flexibility. MMICs usually apply microstrip and metal-insulator-metal (MIM) capacitors for matching networks, while lumped inductors and MIM capacitors are employed for low microwave frequencies. To reduce the losses and provide for low inductance ground connections metal filled via holes from the substrate to the surface are used [11].

2.2.3 Class AB power amplifiers

Class AB power amplifier has characteristics intermediate to class A and B power amplifiers. To enhance the efficiency the conducting angle is reduced to a value between π and 2π. Thus the drain current dc value is not null as in class B power amplifiers but quite higher, usually corresponding to a 10% drain current increase. This increase is determined by using a gate source voltage quite higher than the threshold voltage. For more than half period the drain current has a value higher than zero corresponding to the sinusoidal wave, while in the remaining part, being in the cut-off region, it has null value. Correspondent curve is reported in Figure 2.17 with drain source voltage measured in two conditions: with broadband resistive output termination and with short circuited harmonic termination. Drain source output voltage can be calculated through the sum of the product of each current harmonic with the correspondent output load impedance.

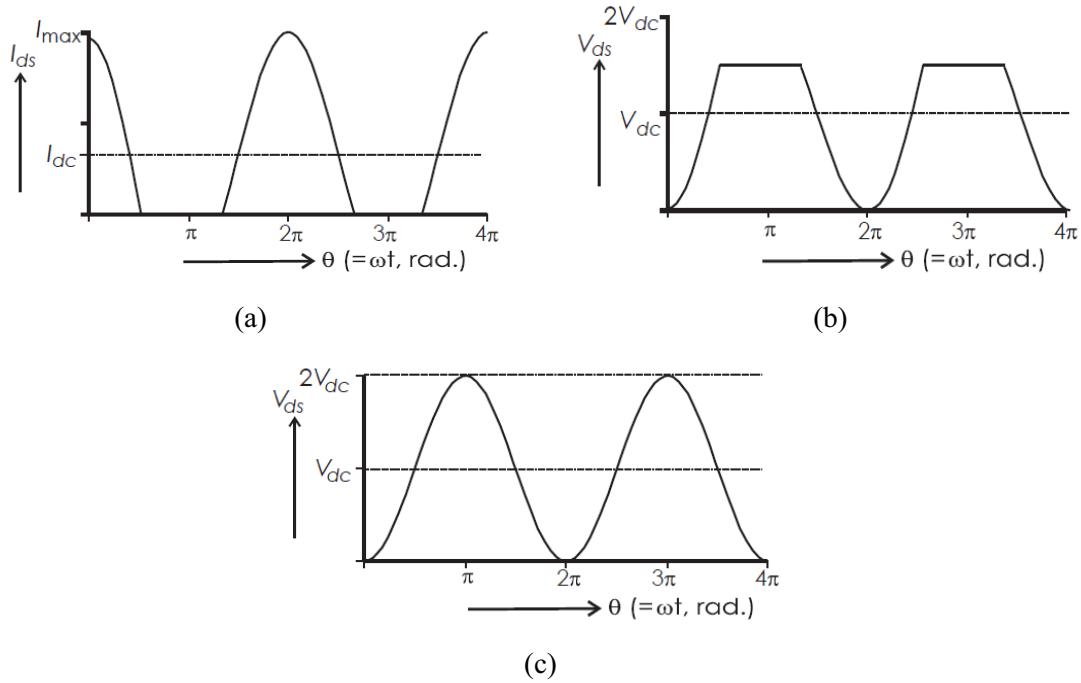


Figure 2.17: (a) current, (b) output voltage with broadband resistive output termination, (c) voltage with short-circuited harmonic termination

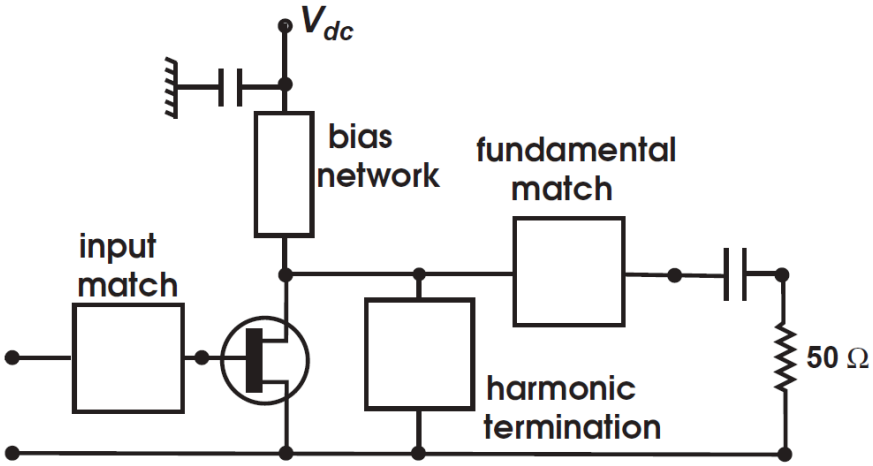


Figure 2.18: Topology of basic Class AB amplifier

In Figure 2.18 main elements of a typical class AB power amplifier for operating frequencies in the GHz range are represented. Main blocks are an input match circuit, a bias network and an output match circuit. The output match has two main functions: (i) provide for match by transforming the device load line resistance to system imprudence value, (ii) block harmonic currents. The harmonic termination usually consists in two main typologies: (i) a short circuited quarter wave stub which reports a short circuit only at even harmonics. Such method

does not allow the use of a wide bandwidth due to the high impedance induced. (ii) shunt series resonator designed according to the second harmonic [20]. Indeed it has been demonstrated than harmonics higher than the third one can be blocked by the device, by its output capacitance or by the device low pass characteristics [20]. Especially in the first case, where the harmonics are blocked by output capacitance, issues are introduced when lower frequencies or technologies characterized by lower output capacitance characteristics are employed.

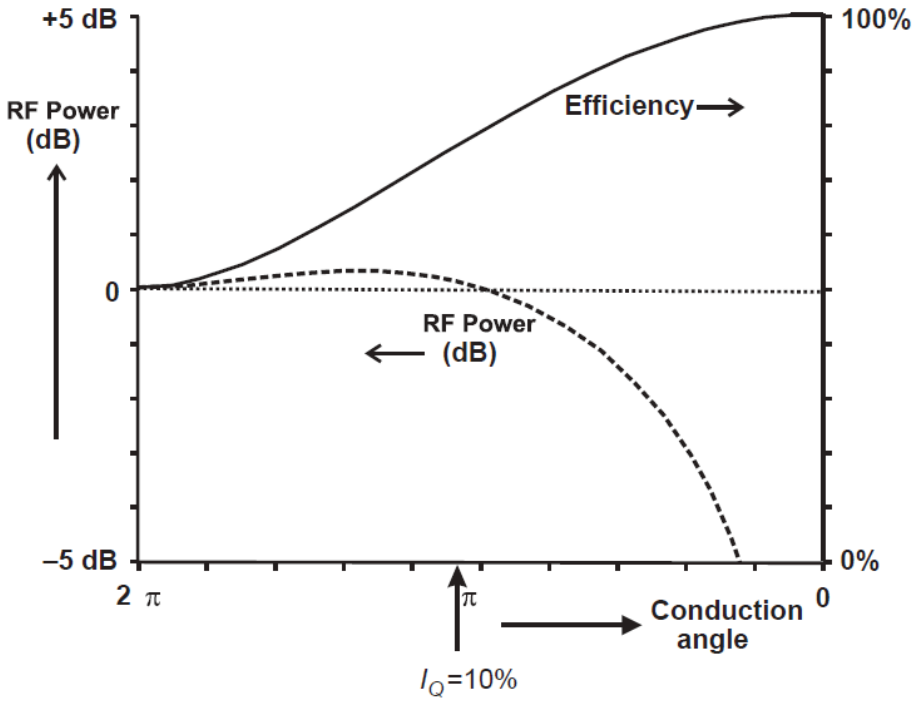


Figure 2.19: RF power and efficiency as a function of conducting angle [20]

Class AB power amplifier are characterized by a conducting angle between π and 2π. According to Figure 2.19 this typology of power amplifier leads to no significant RF power loss, maintaining a RF power similar or quite higher than the one obtained in class A power amplifiers, depending on the conducting angle achieved. Furthermore it can reach an efficiency higher than power A power amplifiers and similar to class B. Even if class C power amplifiers reach a higher efficiency, they are also characterized by a RF power strong decrease when lower conduction angles and higher efficiency values are obtained [20].

It is important to evaluate the efficiency variation as a function of input drive back-off. In a class B power amplifier, when a 6 dB PAR is considered, the efficiency at the mean power level has only dropped by a factor of two, as opposed to a factor of four in the Class A case [11]. Figure 2.20 shows the power back-off efficiency characteristics in a class AB power amplifiers for several quiescent bias point applied. It is possible to state the higher efficiency for quiescent bias points up to at least the 10% level [11].

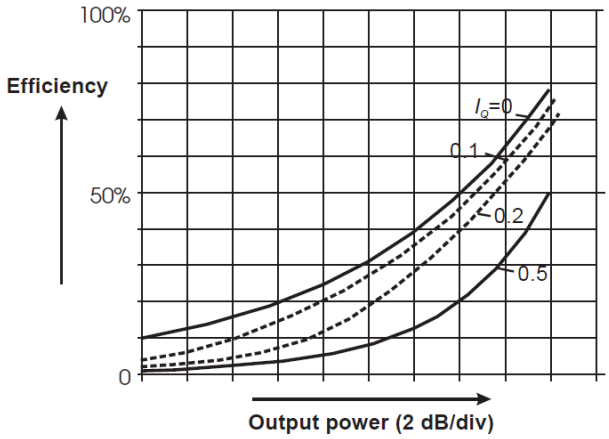


Figure 2.20: efficiency of a class AB power amplifiers as a function of output power for several quiescent bias points applied [11]

Figure 2.21 reports the DC and fundamental components of a truncated cosine wave. DC components drops when the conduction angle is reduced, leading to lower values when the angle approaches zero, corresponding to a class C power amplifier. The fundamental RF component remains almost constant with an angle between π and 2π, corresponding to the AB power amplifier [20]. Harmonics components higher than the second one, as previously explained, are much lower than in other power amplifiers typologies such as class C. A solution to the quite higher value of the second harmonic is that it can be blocked by specific circuits applied in the output matching block.

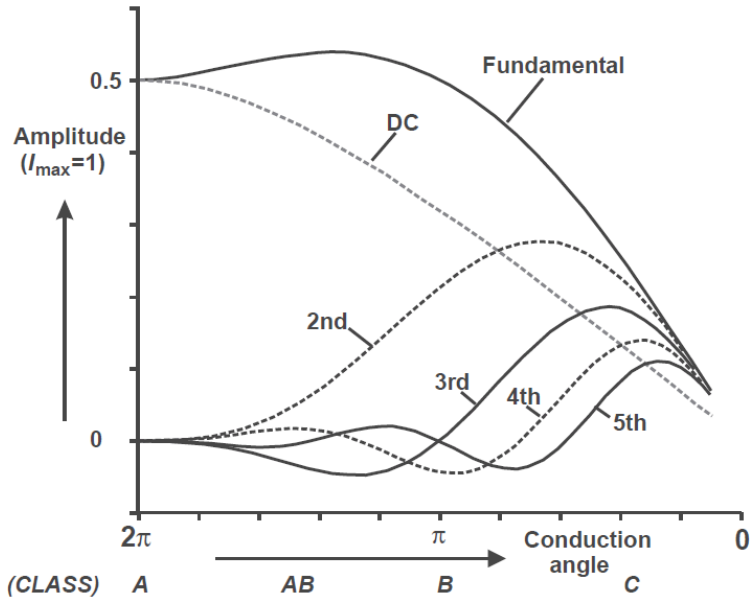


Figure 2.21: harmonic components in different power amplifiers typologies [20]

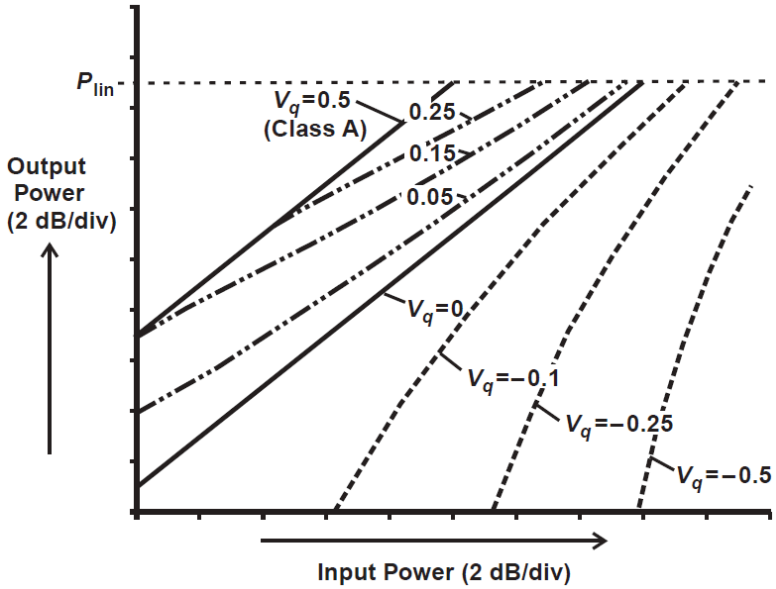


Figure 2.22: Linearity of class AB power amplifiers [11]

Class AB power amplifiers present also several disadvantages. One of the most important aspects is the significant non linearity due to the truncated sinewaves which characterize both the drain current and output drain voltages. Figure 2.22 represents the linearity of class AB power amplifiers. For specific quiescent bias point it is possible to obtain linear performances. It is possible to state that, according to Figure 2.22, as the quiescent bias point approaches the class B point, the linearity tends asymptotically toward a linear characteristic [11].

2.2.4 Power amplifier dynamic range

In order to define the power detector function it is necessary to define the concept of dynamic range. Figure 2.23 shows the output power as a function of the input power. It is possible to notice that the curve can mainly be distinguished in two regions: (i) a linear region, (ii) a non-linear region. In the first region the output power increases linearly with the input power, while in the second zone the output power saturates, leading to the so called power gain compression.

The 1 dB compression point is defined as the point at which the power gain of the nonlinear amplifier deviates from the ideal linear amplifier by 1 dB. The output power in this operating point can be determined by (2.1), on the basis of [19], where the second and the third term indicate the contribution corresponding to the 1 dB compression point and to the ideal power amplifier, respectively

$$P_{0(1dB)}(dBm) = A_{(1dB)} + P_{i(1dB)}(dBm) = A_{0(1dB)} - 1dB + P_{i(1dB)}(dBm) \quad (2.1)$$

.

The dynamic range is the difference between the output power measured at 1dB compression point and the minimum power value detectable, as shown in (2.2) [19].

$$d_R = P_{0(1dB)} - P_{0min} \quad (2.2)$$

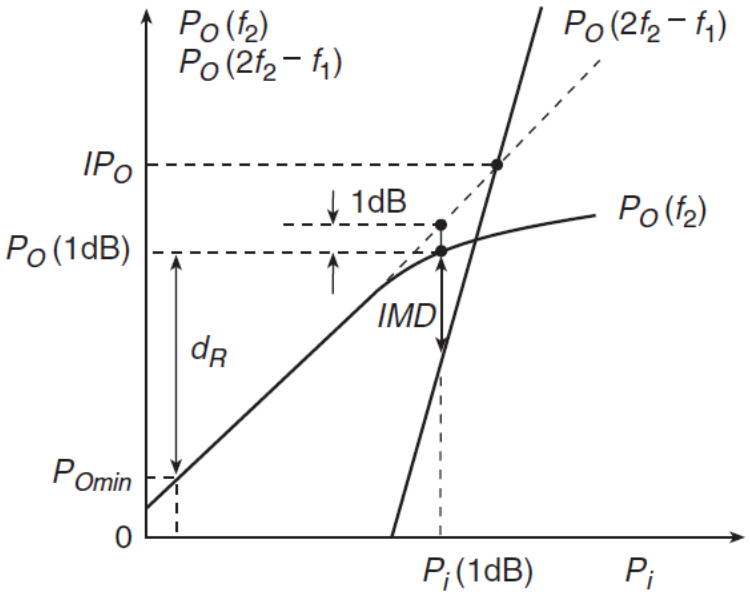
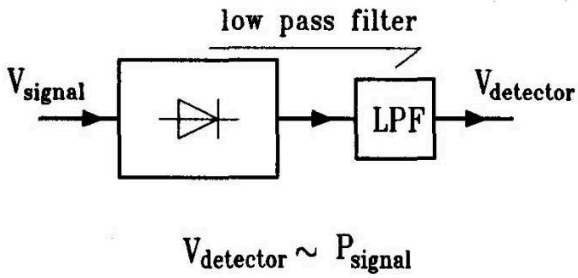


Figure 2.23: output power as a function of an input power

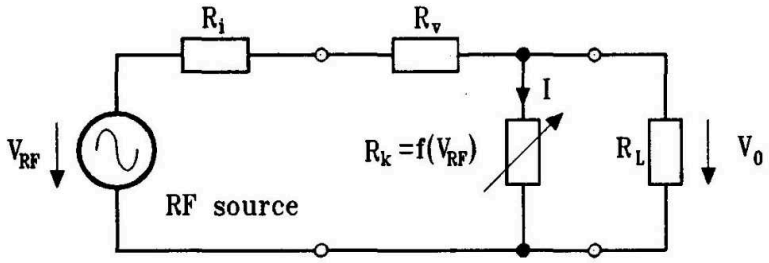
To enhance the dynamic range value power amplifiers are characterized by the presence of a detector circuit. Several works have been reported in literature concerning the design of a power detector circuit, although the most part of them deals with CMOS technology. Krekels et al. [21] describe a solution to design a power detector with GaAs FETs. Krekels et al. demonstrate that the use of FET technology instead of Schottky diode detectors commonly used can lead to significant improvements: (i) higher dynamic range; (ii) low noise characteristics, especially at low power levels; (iii) lower sensitivity to temperature, thus obtaining a more accurate circuit. The achievement of a lower noise is provided by the fact that the FET acts with passive operation, thus the lower dynamic limit is only provided by thermal noise since no significant current flows.

The principle of operation relies on the rectification of the RF signal. The signal is influenced by a voltage divider, containing two resistor; the change of the voltage divider ratio leads to a rectification of the signal. It is important to remember that the resistance which

determines the output voltage is not influenced by the detector input signal but it changes with the RF input signal. An example which describes the principle of operation of a detection principle with diodes and FET technology is shown (Figure 2.24).



(a)



(b)

Figure 2.24: power detector principle with (a) diodes and (b) FET structure

Chapter 3:Thermal degradation of GaAs devices

3.1 Fundamentals about thermal and electrical degradation on GaAs pHEMTs

In the description of thermal degradation it is firstly important to establish a difference between failure mechanisms and modes. The first describe the chemical and/or physical phenomena which originate device failures, while the second ones indicate degradation of electrical parameters.

According to literature [22] causes which determine failure mechanisms and modes can be distinguished into three main categories: (i) thermal, (ii) electrical, (iii) environmental. Nevertheless it is important to consider the difficulty of the definition of a dominant failure aspect because several mechanisms have similar properties and multiple mechanisms can act simultaneously.

Thermal reliability will be described through three main phenomena: (i) the so called gate sinking, which consists on the metallurgical interdiffusion of Schottky contacts, (ii) the metallurgical degradation of ohmic contacts, (iii) the presence of a thermally activated electron detrapping.

The electrical aspects which affect device reliability are mainly described by: (i) hot electron related phenomena which lead to trap creation on the drain access region or charge injection and trapping in the passivation layer,(ii) surface corrosion,.

Finally environmental issues can be described by: (i) hydrogen and (ii) fluorine dopant passivation. These last phenomena will be shortly summarized in the following but not discussed in detail, consistently with the experimental data presented in the chapter. Hydrogen react with the Ti present in the gate stack (usually a Ti/Pt/Au gate stack) [23], [24]. The formation of a TiH compound generates a consequent shift of the threshold voltage with an initial time evolution which follows a square root law. According to previous works reported in literature [25] this phenomenon can be reversible or prevent through the introduction of a WSi layer in the gate stack which impede the reaction between Ti and hydrogen. Fluorine was revealed only in n-InAlAs/InGaAn HEMTs through annealing at not high temperatures, demonstrating a diffusion into n-InAlAs and the formation of Si bonds [26]. n-InAlAs structures were highly used because of their transport properties and lattice matching with InP substrate. Consequent failure mode observed is an increase of both source and drain parasitic resistances.

3.1.1 Thermal Reliability

Gate Sinking

GaAs pHEMTs is characterized by a Schottky gate stack, usually defined by a Ti contact layer. Gate contact structures most commonly used are Ti/Au, Ti/W/Au and Ti/Pt/Au. The last structure is preferable since the introduction of a Pt layer can prevent Au interdiffusion.

Ti is usually preferred because of its properties, which allow both adhesion to the semiconductor and a good barrier height to limit the leakage gate current. Nonetheless, when submitted to high temperatures, Ti diffuses leading to the creation of an intermetallic layer which determines two not recoverable failure modes: a slight increase of the transconductance and shift of the threshold voltage towards positive values with a consequent decrease of the drain current [27], [28]. The last failure mode is determined by the lower barrier layer thickness as a consequence of the formation of an intermetallic compound.The degradation mechanism time evolution usually follows a square root law with an activation energy of 1.4-1.6 eV, although higher values have been also reported. In order to prevent gate sinking phenomenon several solutions have been proposed [22] and consist in the introduction of a refractory metal in the gate contact stack, such as WSi, WSiN or Mo.

Main techniques to identify metallurgical interdiffusion are: (i) the so called back etching, which consists in the analysis of the metallization once all the semiconductor has been removed, (ii) in-depth Auger composition profile, (iii) device cross section preparation and SEM (Scanning Electron Microscopy) or STEM analysis (Scanning Transmission Electron Microscopy).

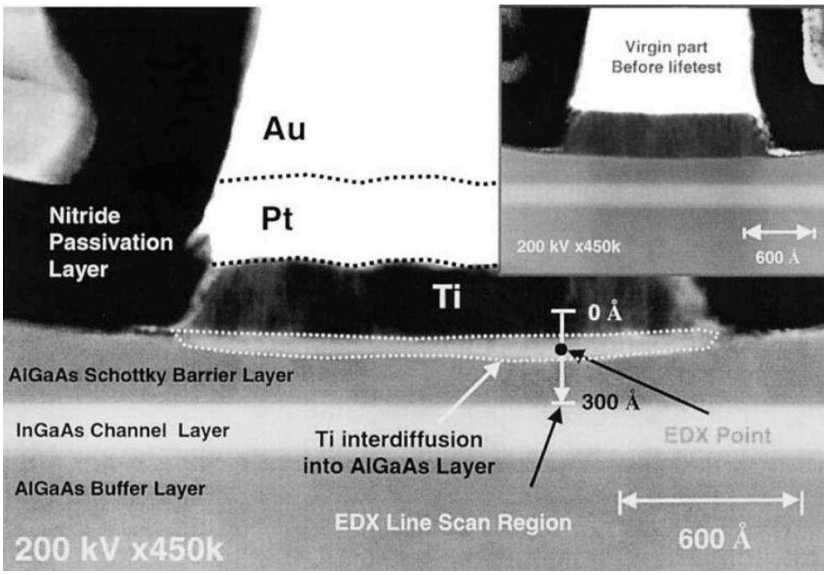


Figure 3.1: STEM image of a degraded GaAs pseudomorphic HEMt (PHEMT) with Ti/Pt/Au metallization after lifetest at Tambient = 235°C for 48 hours [27]

Metallurgical interdiffusion has been widely studied in literature [27]. According to the work reported in [27], a STEM analysis of 0.15μm GaAs pHEMT after thermal stress showing gate sinking phenomenon in the AlGaAs layer is shown in Figure 3.1. Interdiffusion evaluation reported in [27] was confirmed by energy-dispersive X-ray microanalysis Figure 3.2.

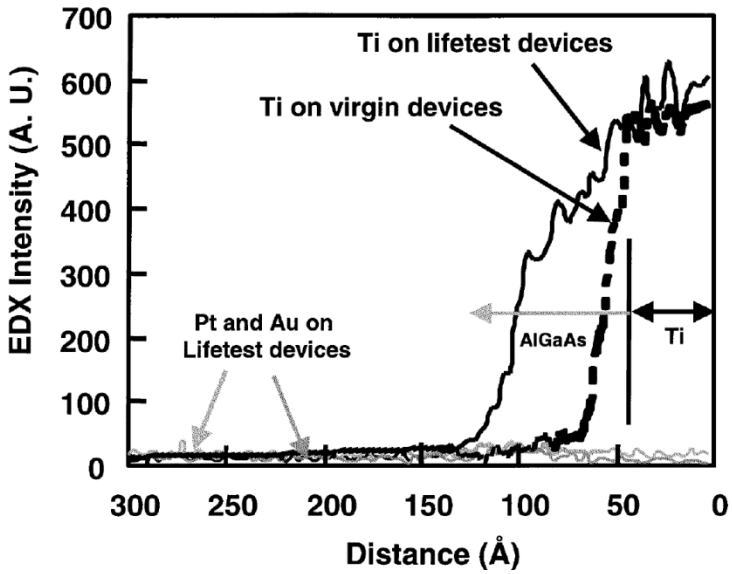


Figure 3.2: Energy Dispersive X-ray microanalysis (EDX) line scanning from Ti metal layer into AlGaAs Schottky barrier layer, indicating the presence of Ti but no Pt or Au interdiffusion into AlGaAs Schottky barrier layer [27]

Ohmic contact degradation

Ohmic contacts are usually characterized by AuGeNi alloys in order to obtain sufficiently low values of parasitic resistances in the access regions, i.e. R_D and R_S. Although good performances reached by those alloys, when thermal treatments are applied Au can diffuse in the barrier layer leading to the generation of new intermetallic compounds. This phenomenon leads to an increase of both the access regions parasitic resistances; correspondent time evolution follows a square root trend [29]. Ohmic contact decrease usually shows a decrease in the maximum transconductance value but no variation in the threshold voltage, thus demonstrating the stability of the Schottky contact. As a consequence of the high activation energy demonstrated also in the early technologies (between 1.6eV and 2eV) ohmic contact degradation is not one of the most dangerous failure mechanisms at operating temperatures, although it can mask other failure mechanisms having lower activation energy during accelerated tests at high temperatures.

Figure 3.3 reports an example of source ohmic contact degradation, showing the TEM analysis on an untreated GaAs pHEMT device and a device after stress at T=250°C. In the first condition (Figure 3.3a), although the rough interface, the channel is not influenced by the ohmic

contact. On the contrary after stress the ohmic contact reaches the InGaAs channel (Figure 3.3b) and, as explained by Figure 3.3c where a schematic section is proposed, can reach the superlattice layer [30]. Several works have been reported in literature to improve device stability. [31] studied the degradation of AuGeNi and AuGe/Pt ohmic contacts and established that the reliability of ohmic contact is significantly increased by a Pt. A further solution has been proposed by Zhang et al. [32], demonstrating that in a AuGeNi/Au system the use of a TiN interdiffusion barrier layer strongly increases the contact stability. Furthermore, ohmic contacts stability can be improved using refractory materials such as WSi or low InAs composition caps.

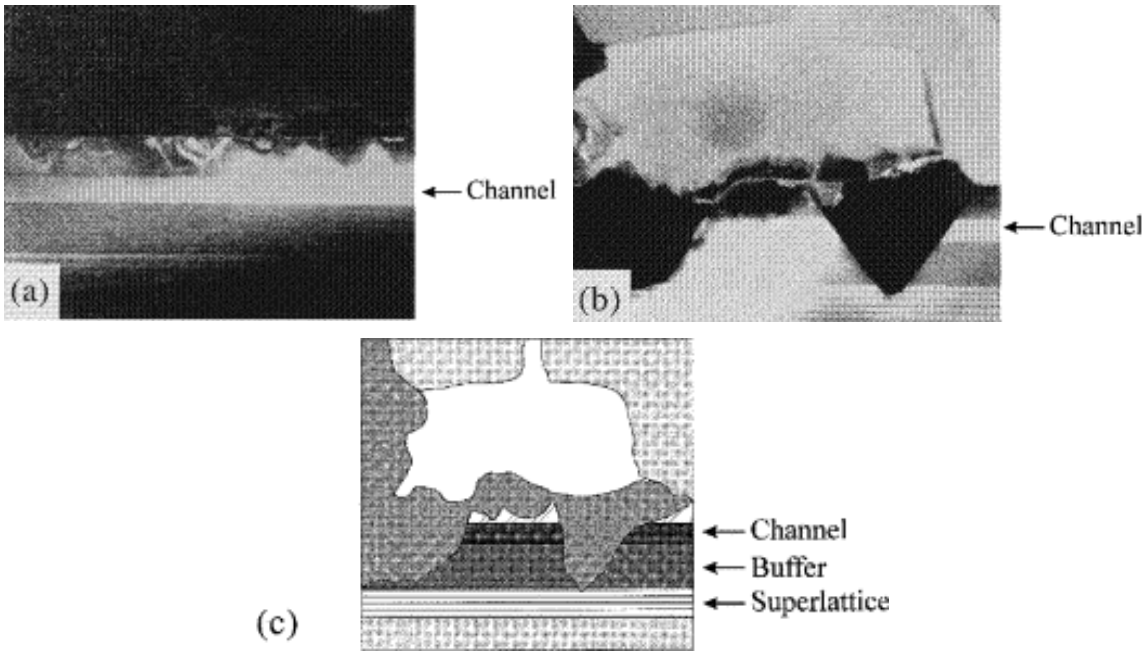


Figure 3.3: TEM analysis of a source ohmic contact in: (a) fresh device, (b) device after stress. (c) schematic of the metallic interdiffusion [30]

Electron detrapping

Thermal treatment can induce electron detrapping reversible phenomenon. A detailed description of failure mechanisms and distinction between thermal activated electron detrapping and degradation due to hot electron has been previously studied in [33]. The physical explanation provided by [33] suggests that parameters variation can be ascribed to a reduction of compensation of the trapped negative charge. Samples are characterized by deep levels partially filled with electrons. Thermal treatment can induce electron de-trapping. Differently by effects provided by hot electrons with low power dissipation and negligible device self-heating, charge de-trapping occurs both in the active channel and in the gate source and gate drain access region, leading both to a negative shift of the threshold voltage and to an increase of the parasitic source and drain resistances with a consequent decrease of the transconductance peak.

3.1.2 Electrical reliability

Hot electron related phenomena

Main issues which affect device reliability from the electronic point of view are hot electron related phenomena. Such effects are more evident in power devices or when a high voltage difference is applied between the gate and drain terminals.

The increase of the gate drain voltage leads to an acceleration of the channel electrons due to the high electric field, especially at the edge of the gate drain region, and to the consequent generation of hot electrons. Hot electrons are channel electrons no longer at thermal equilibrium with the semiconductor crystal lattice. The generation of hot electrons can cause several degradation mechanisms: (i) trapped electron recombination by means of holes generated by impact ionization [34]; (ii) generation of traps or deep levels in the barrier layer under the gate or at the surface, as a consequence of the escape of hot electrons from the potential well at the heterointerface [35]; (iii) injection of hot electrons into traps within the passivation layer [36].

The three failure mechanisms explained lead to different failure modes, both recoverable or not recoverable. In all the cases hot electrons are electrical activated effects although influenced by temperature due to the ease of energy lost at high temperatures as a consequence of the increase of interaction with phonons. The first mechanism is recoverable and leads to a threshold voltage negative shift which saturates with time as a consequence of traps emptying. Furthermore holes generated by impact-ionization drift towards the source; part of them is collected by the gate, where they give rise to an increase of (negative) gate current. Concerning the second mechanism, according to literature, failure modes can be considered not recoverable and mainly consist in a threshold voltage negative shift and in a consequent variation of the drain current. In the last case the resulting negative charge trapped reduces the channel conductivity, thus leading to an increase of parasitic drain resistance and a decrease of the transconductance peak. Further failure modes are noticed: reduction of current maximum and output power, increase of the breakdown voltage imposed in off condition. According to literature, in the early stage this phenomenon is reversible with an activation energy of 1.4eV and it is called power drift. When a further stress is induced, it generates a not recoverable situation referred as power slump. Most important factors which influence the generation of hot electrons are high electric field and current density. When both the aspects are reported, for instance in class A amplifiers, hot electrons effects are higher.

Several techniques have been reported in literature to evaluate and study hot electron related effects: measurement of the gate current and analysis of the electroluminescence, i.e. that radiation emitted by the device due to electron hole pairs generation and intra-band transition of

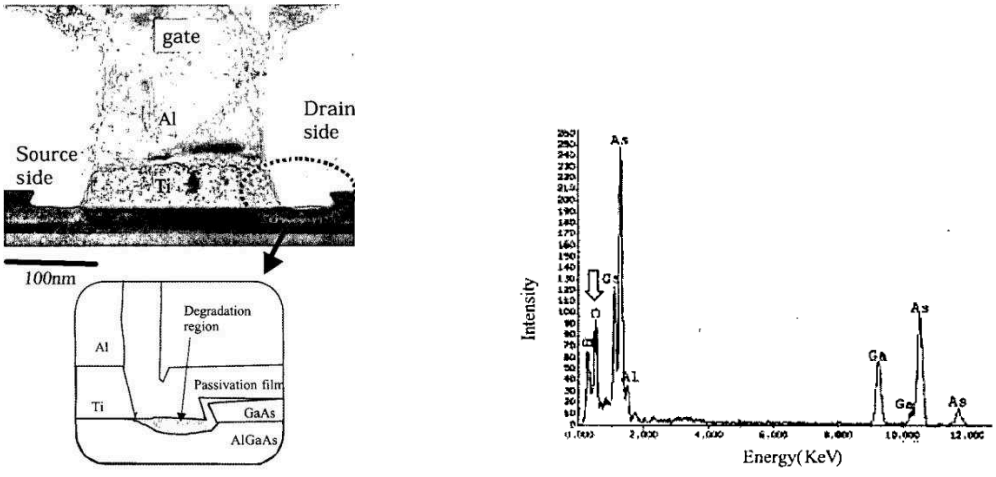
hot carriers. Furthermore several methods have been proposed in literature to describe the law which establishes the time to failure due to hot electron related effects: (i) time to failure depends exponentially on the inverse of the gate drain voltage, according to the equation (3.1) [37]; (ii) if it is confirmed that gate current depends on impact ionization it is possible to use (3.2) [37]; (iii) Finally, time to failure can be also put into relation with a "safe" operating voltage (3.3) [37]. All the constants are empirical fitting constants which are defined after a significant number of tests. An example is provided by [37].

$$t_F = C\ exp\left(\frac{D}{V_{GD}}\right) \quad (3.1)$$

$$t_F = \frac{F}{I_D(|I_G|/I_D)^m} \quad (3.2)$$

$$t_F = \frac{A}{I_G\left(V_{DG} - V_{DG}^{safe}\right)^{1/2}} \quad (3.3)$$

Surface corrosion



(a) (b)

Figure 3.4: (a) surface corrosion effect and (b) EDX analysis of the degraded region [38]

A few works which concern surface corrosion induced by electrical phenomena have been reported in literature [22], [38]. Surface corrosion occurs when electrons or holes have enough energy to overcome the AlGaAs barrier and reach the semiconductor surface, leading to the generation of an electrochemical reaction. The corrosion is due to the creation of surface oxides.

An example, provided by [38], is reported in Figure 3.4a. Furthermore the intensity of the EDX spectra of the degraded region confirms the presence of oxygen Figure 3.4b. Main not recoverable failure modes noticed are: increase of drain parasitic resistance with a consequent decrease of both transconductance peak and drain current, reduction of the output power and impact ionization.

3.2 Description of analysed devices: discrete transistors and power amplifiers

3.2.1 Discrete Transistors

Tested devices are 0.25µm gate length AlGaAs/InGaAs pHEMTs having a Ti/Pt/Au multilayer Schottky gate metallization and AuGeNi source and drain ohmic contacts. Process control monitors dies were used for testing purposes, each containing eight multi-finger discrete pHEMTs, characterized by different gate widths from 0.1mm to 0.96mm.All the devices have a gate pitch of 20-20 µm, except for devices with W_G=0.96mm, which have a gate pitch of 26µm, and devices with a periphery of 0.4mm which have two different gate pitch of 12-18 µm and 20-20 µm, respectively. Except for devices with largest periphery (0.96mm), all the devices are covered by air bridge. An image of a PCM used for the test is shown in Figure 3.5.

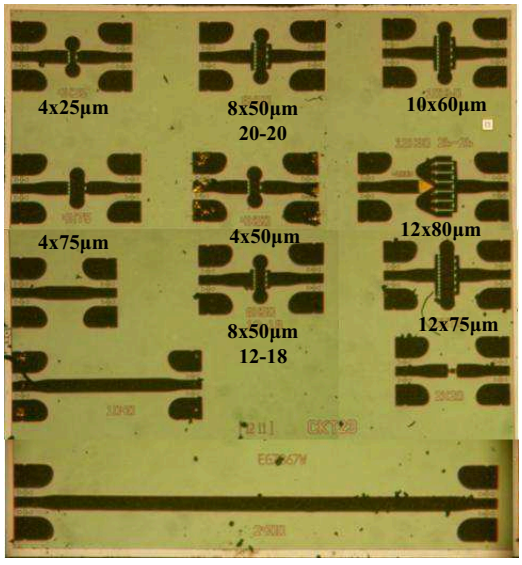


Figure 3.5: PCM for GaAs pHEMTs analysis

Devices belonging to the same technology but with different geometry are characterized by parameters with similar value if considered normalized to the gate width value. At high dissipation condition (V_{GS}=0.4V) a drain current of 0.4-0.45A/mm is reported in saturation region. A max g_m of 0.35 S/mm and 0.4 S/mm is reported in linear and saturation zone, respectively. A threshold voltage of -0.9V is noticed in all the devices. A breakdown reverse voltage of -15V has been stated. Further information are shown in the following section.

3.2.2 MMIC Power Amplifier

Tested devices are MMIC four stages power amplifiers grown on a GaAs substrate. A schematic of the power amplifier is reported in Figure 3.6. Each stage is characterized both by a load matching circuit and by a ESD protection circuit. Furthermore a power detector, with a power range of 35dB, is developed in order to enhance the power amplifier dynamic range. Except for the last stage all the power amplifiers transistors are GaAs pHEMTs characterized by a L_G=0.25 µm and a W_G=12x75µm with similar characteristics to devices belonging to the PCM previously presented. In the last stage pHEMTs have a W_G=12x80µm.All the pHEMTs are characterized by a T-shape gate to improve device performances.

Tested structure operates in AB class operating in Ku band microwaves (between 12 and 15 GHz) with a gain power at 1dB compression point of 33 dBm and a nominal power gain between 26-30 dB. All the pHEMTs are biased in saturation zone (V_{DS}=6V) with a V_{GS} near the V_{TH} value. Except for the last stage all the stages operates at V_{GS}=-0.65V revealing a I_{DSS} of 60mA in the first stage and of 460mA in the second and third stage (half part). According to the schematic shown in Figure 3.6 it is important to remember that in third and fourth stages transistors are biased by two different gate and drain terminals. A I_{DSS} of 680mA is reported in the last stage (half part).

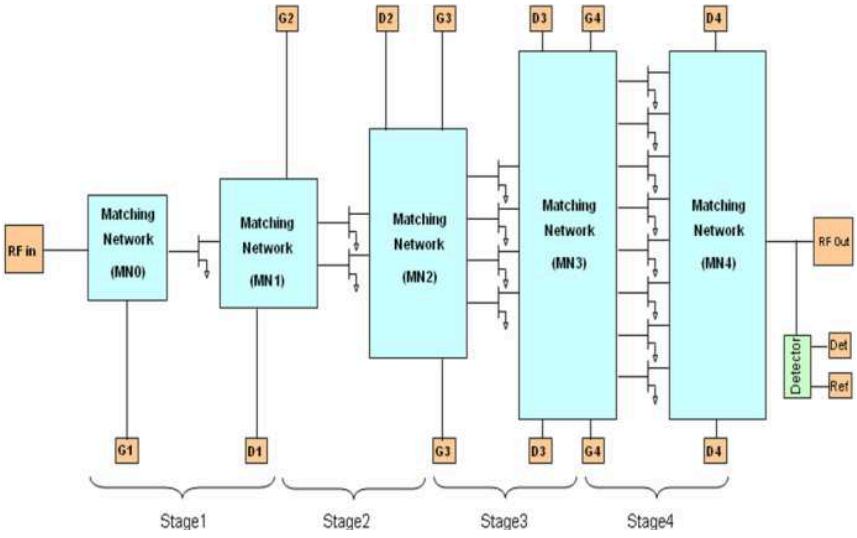
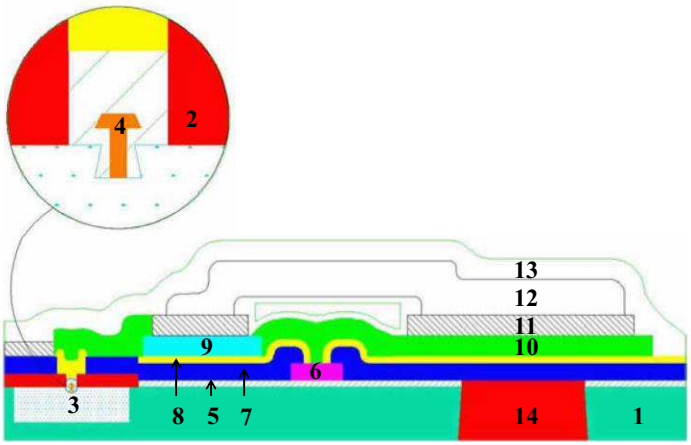


Figure 3.6: Schematic of the tested power amplifier.

The MMIC power amplifier is grown on a GaAs substrate. A schematic of a commercial structure similar to the one used is reported in Figure 3.7. Diodes used for ESD protection circuit and power detector consist on multi-finger pHEMTswith drain and source terminal

connected; pHEMTs are characterized by L_G=0.25µm and several different W_G, depending on the diode function. Diodes belonging to power detector circuit are characterized by a gate periphery from 0.02mm to 0.04mm. Diodes used for the ESD protection circuit have higher gate periphery, depending on the stage and ESD robustness required.



1:GaAs substrate
2: Ohmic metal
3: Active region
4: T shape gate
5: Nitride 0
6: TaN Resistor
7: Metal 0
8: Nitride 1
9: MIM Metal
10: Nitride 2
11: Metal 1
12: Metal 2
13: Protective overcoat
14: Via under Cap

Figure 3.7: Representative schematic of a 0.25um pHEMT technology

Capacitors are developed through MIM technology. They can be distinguished in: (i) single MIM capacitors, (ii) MIM capacitors on vias, where MIM element is aligned exactly on the top of a via for ground connection. In the technology proposed, according to different metal used, MIM capacitors can have three different dimensions. [39] describes an example of MIM capacitors and implementation with Vias technology. An example of the description of both ground Vias developed under Capacitors are there reported and described in Figure 3.8, according to the description given in Figure 3.7.

Although the technology offers the availability of developing GaAs resistors and the higher sheet resistance demonstrated by GaAs resistors, all the resistors are composed by a TaN alloy.

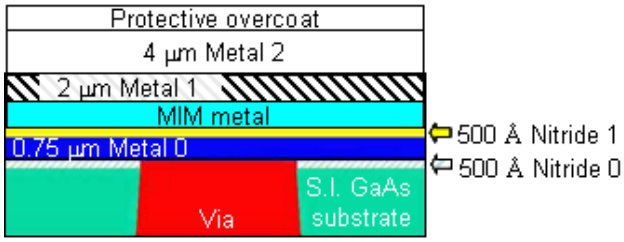


Figure 3.8: (a) ground Vias developed under Capacitors

3.3 Long term thermal stress on GaAs pHEMT

In this chapter an investigation of failure mechanisms of pseudomorphic AlGaAs/InGaAs HEMTs tested at high temperatures without bias is reported. Eight independent accelerated tests in air from 175°C to 350°C have been considered. For each temperature a number of PCMs has been tested. Degradation has been evaluated on eight different geometries, even if no significant difference has been noticed on devices with different characteristics.

Degradation appears to be non-monotonic, i.e. drain current first decreases, then increases again, following the corresponding shifts in the threshold voltage, respectively positive in the first phase and then negative in the second one. Failure was defined as a 10% decrease of drain current; an activation energy of 2.14 eV was extrapolated from the highest temperature tests.

Although the initial decrease of drain current could be attributed to gate metal interdiffusion, or "gate sinking", consistently to a positive shift of threshold voltage, the degradation is described also by a degradation of the maximum value of transconductance and an increase of end resistances, that suggest a concurrent degradation of ohmic contacts. Independently from this effect, the Schottky barrier height of the gate contact continuously decreases from 0.73 eV in the untreated devices to a minimum value of 0.59eV. This last mechanism counteracts the effect of gate interdiffusion and eventually prevails, leading to an opposite shift of the threshold voltage and a partial recovery of drain current after a defined amount of hours for highest temperatures tested.

3.3.1 Experimental details

The stress consisted of a pure thermal storage with no bias or signal applied. Eight different tests at constant ambient temperatures have been set up, from a minimum-stress condition at T_{AMB}=175°C to the highest temperature condition, with T_{AMB}=350°C, each test differing form the preceding one for a 25°C increase step in temperature. Tests have been carried out in air within environmental chamber. For each test condition a set of five dices has been used, each die containing eight transistors with different geometries. When a temperature lower than 275°C was adopted, the devices have been tested up to 2000 hours; devices stressed at 275°C, 300°C, 325°C, 350°C have been tested for 1473, 747, 176 and 28 hours, respectively.

At each step all the devices have been monitored with DC evaluation in order to define specific parameter variation and identify device failure. Moreover, in order to better define degradation mechanism, at each step the following analysis has been done Table 3.1. Detailed information about measurement are explained in the following.

Analysis	Main Parameters	Analysed mechanism
DC	I_{DSS}, I_{GSS}, I_{GLEAK}, V_{TH}, max g_m, diode current	Gate sinking, ohmic contact degradation
Pulsed	Current collapse	Trapping phenomena
End resistance	R_D, R_S	Ohmic contact degradation
Barrier height	Barrier height through GS diode I-V curve	Barrier height decrease

Table 3.1: Measurement to monitor device degradation during long term thermal stress

DC Characterization

Devices have been fully characterized by means of DC analysis through the evaluation of GS diode reverse and forward current, output I_DV_D and I_GV_D characteristic, I_DV_G and I_GV_G transcharacteristic and transconductance (g_mV_G). Devices have been measured with a parameter analyser (Agilent 5263A) and biased with RF tips inside a Karl Suss probe station.

Main parameters considered for the analysis are: (i) drain current measured in saturation zone (I_{DSS}), defined by a range from V_{DS}=2V and V_{DS}=5V, according to the I_{DS} vs V_{DS} characteristic. In order to present data in a more detailed way it has been decided to report the values at high dissipation condition at V_{GS} = 0.4V (to see the largest variation); (ii) max g_m reported in linear and saturation zone (V_{DS}=0.4V, V_{DS}=5V respectively), (iii) transistor gate leakage current measured in OFF and ON state (V_{DS}= 5V and V_{GS}= -1.2V, V_{GS}=0.4V respectively), (iv) diode current measured with reverse and forward bias applied (V_{GS}= -1.2V, V_{GS}=0.4V respectively), (v) threshold voltage (V_{TH}), evaluated as the V_{GS} value corresponding to a I_{DS} of 0.05A/mm for a V_{DS}=5V applied (saturation zone).

An example is reported for a device characterized by W_G=0.2mm in Figure 3.9. Similar results, if considered normalized to gate width, have been reported in devices with different peripheries. At high dissipation condition a drain current of 0.4-0.45A/mm is reported in saturation region. A max g_m of 0.35 S/mm and 0.37 S/mm is reported in linear and saturation zone, respectively. An absolute gate leakage current of 1.147±0.717 μA/mm and 1.517±0.125 μA/mm is measured in saturation zone when ON (V_{GS}=0.4V) and OFF state (V_{GS}=-1.2V) are considered, respectively. A threshold voltage of -0.9V is noticed in all the devices.

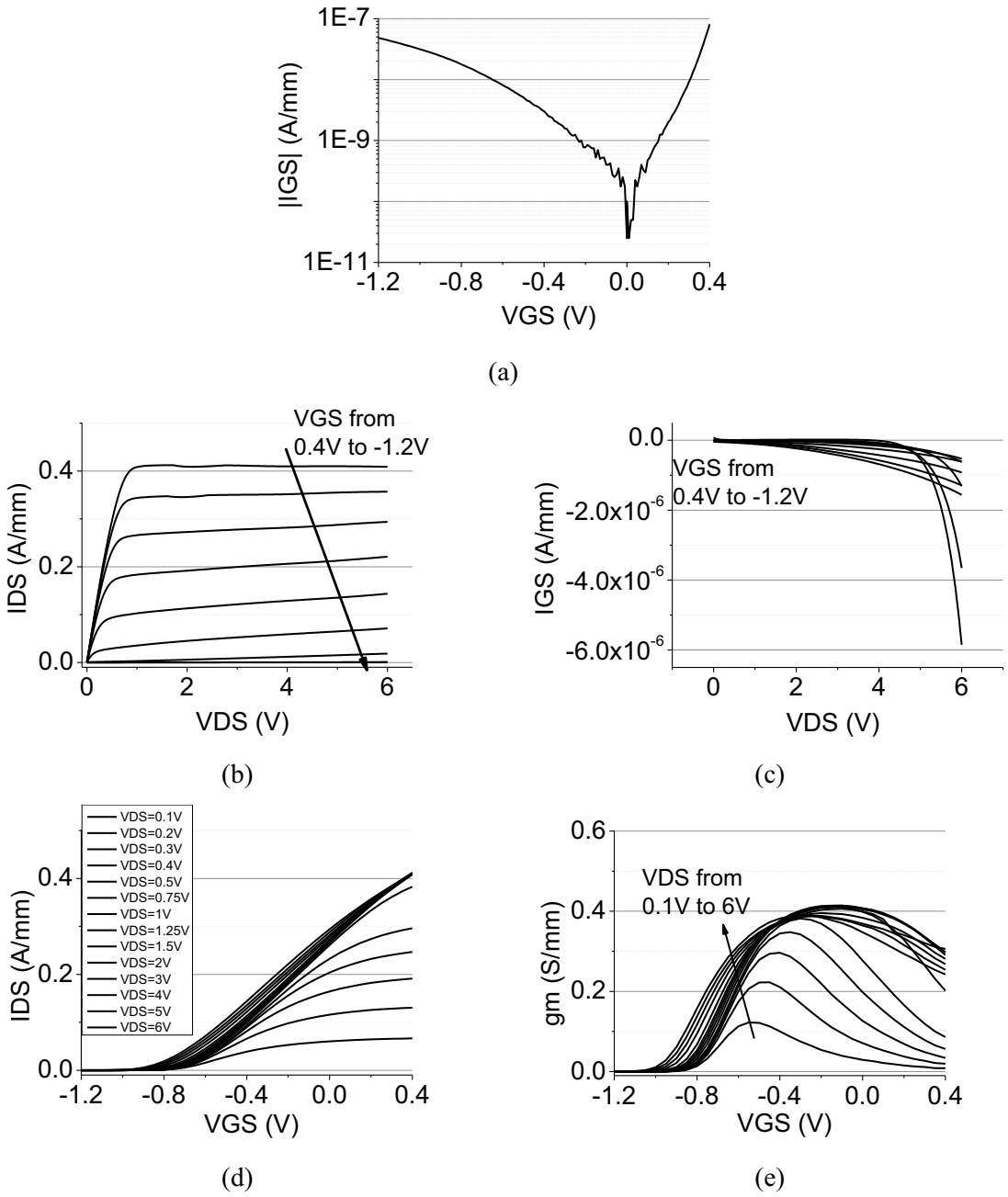


Figure 3.9: DC characterization in a GaAs pHEMT: (a) GS diode, (b) IDVD and (c) IGVD curve, (d) transcharacteristic, (e) transconductance

Pulsed Characterization

Pulsed characterization (also called double pulse measurement) has been carried out by means of a custom setup. I_DV_D curve is defined by pulsing gate and drain voltage from different bias point condition, called baseline or power dissipation level. The setup is composed by two pulser and an oscilloscope; thus a train of pulses is contemporaneously applied to the gate and

to the drain terminals. All the measurements have been carried out inside a probe station Karl Suss biasing the device with RF tips.

During baselines different conditions have been imposed: (i) both gate and drain are biased with null voltage (null power dissipation level), (ii) a "trapping condition", due to the high gate drain voltage, is applied. Current collapse is defined as the difference between the drain current measured in different power dissipation levels over the value measured in the first baseline. Slump ratio is defined as the ratio between the drain current measured in the saturation zone in the first and the second condition applied. Untreated devices show a slump ratio of 0.8% when measured in the worst condition at high dissipation condition in linear zone (V_{DS}=1V, V_{GS}=0.4V), while a slump ratio of 0.90-0.95% is noticed when measured in the same dissipation condition in saturation zone (V_{DS}=5V, V_{GS}=0.4V). An example is shown in Figure 3.10.

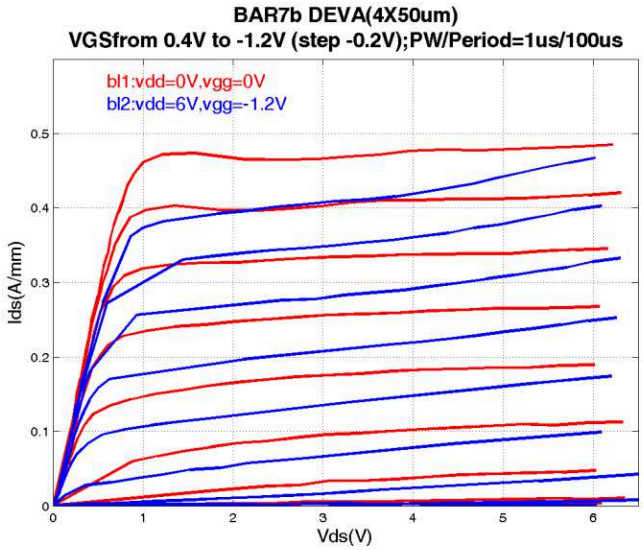
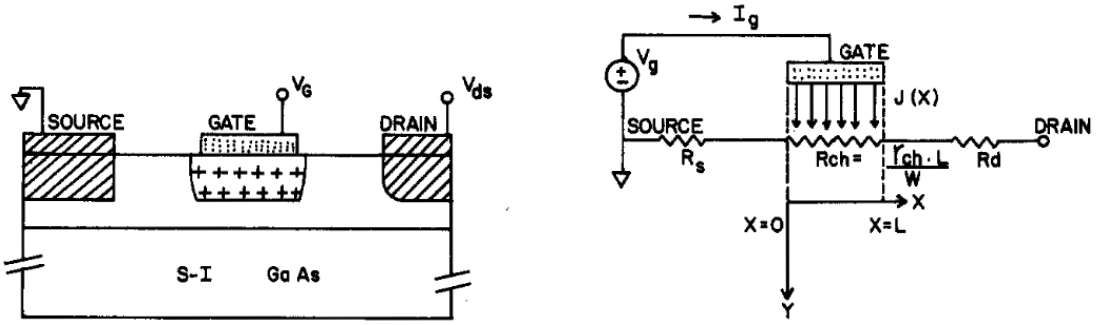


Figure 3.10: pulsed characterization

End Resistances [40]

End resistances measurement is a technique to evaluate source and drain parasitic resistances which has been described in detail in [40]. The method is simply explained by Figure 3.11. We firstly consider the source resistance evaluation. The drain portion acts as a probe since no current flows; on the contrary the current I_g defines a drop voltage across the series resistances, which can be calculated from the ratio between the drop voltage generated and the current flowing. This approach is correct only if the α coefficient is low since the drop voltage generated corresponds to (3.4). A specular approach can be used to evaluate the drain parasitic resistance.

$$V_D = I_g(R_S + \alpha R_{ch}) \quad (3.4)$$



(a) (b)

Figure 3.11: (a) schematic of a MESFET and (b) of the correspondent technique to measure the parasitic resistances [40]

Barrier height measurement

Barrier height has been measured through the gate source diode I-V characteristic measured when forward bias is applied, according to the corresponding basic equations [41].

$$I = I_s\left\{exp\left(\frac{qV}{nkT}\right) - 1\right\} \quad (3.5)$$

$$I_s = SA^{**}T^2 exp\left(\frac{q\emptyset}{kT}\right) \quad (3.6)$$

GS diode I-V characteristics have been measured for several ambient temperatures applied, from 25°C to 100°C with 5°C/step. From (3.5), once the last term can be considered as negligible, it is possible to extrapolate the ideality factor n and its trend as a function of temperature, in order to verify that the value does not change in a significant way and that has a reliable order of magnitude. From (3.6), once I_s has been defined by (3.5), it is possible to calculate the barrier height value $\emptyset$.

3.3.2 Degradation kinetics

In this chapter the variation of devices' main parameters is reported. It has been decided to report only the variation trend in devices with a gate periphery of 0.2mm, according to the low difference measured in devices with different gate periphery. Furthermore it has been decided, for each temperature imposed, to consider only the variation average value among devices,

since the standard variation can be considered as negligible. It is important to highlight that, in all the PCMs measured a good reproducibility has been noticed in all the devices tested, indifferently from temperature applied and geometry tested.

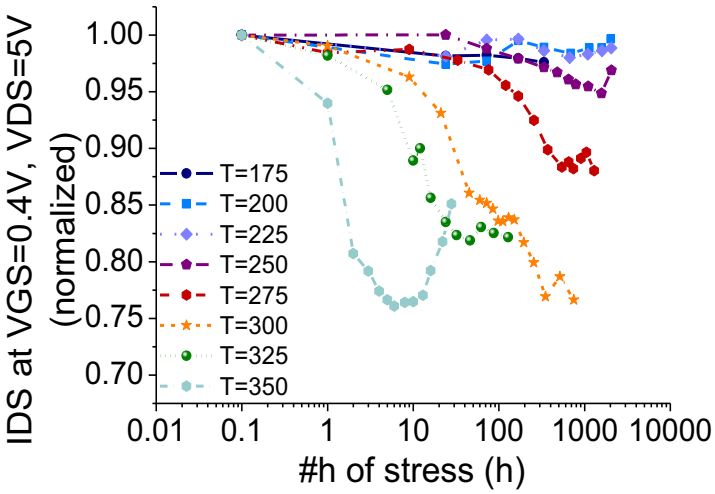


Figure 3.12: Drain current variation measured in saturation zone

When a ambient temperature lower than 275°C is imposed for 2000 hours no meaningful degradation is reported, nor in the I_{DSS} (Figure 3.12), nor in the V_{TH} (Figure 3.13). Devices stressed at T_{AMB}=275°C, 300°C, 325°C report a monotonic decrease of the I_{DSS} up to, respectively, 543h, 350h, 46h; if a further stress is applied the I_{DSS} keeps almost stable. On the contrary a not monotonic trend is noticed when an accelerated test is carried out at T_{AMB}=350°C: after a strong decrease of 24% reported until six hours of stress the I_{DSS} faces an increase, leading to a decrease of 15% (compared to the fresh device) after 28h.

The drain current not monotonic behaviour is explained by the threshold voltage (Figure 3.13), although the possibility of annealing at the contacts, due to the high temperature imposed. After six hours at T_{AMB}=350°C devices revealed a V_{TH} positive shift with a maximum average variation of 0.22V. If a further stress is applied a shift toward the opposite direction is noticed. A consistent behaviour is shown in devices stressed at T_{AMB}=325°C and 300°C.

The drain current variation has a strong impact in the pHEMT applications, especially when power amplifiers are considered. In the case considered in this document power amplifier operates in a AB class, thus it is biased with a V_{GS} near the V_{TH} value. Since the drain current decrease strongly depends on the V_{TH} positive shift, drain current variation is much higher if considered not at high dissipation condition but near the V_{TH} value. Therefore this failure mode has severe consequences when class AB power amplifiers are considered.

In (Figure 3.13) the threshold voltage has been calculated as the V_{GS} correspondent to a I_{DS} of 5mA/mm at a V_{DS}=5V (i.e. saturation zone). Analogous results are given if the V_{TH} is calculated as the intercept of the I_{DS} vs V_{GS} curve tangent with the x-axis.

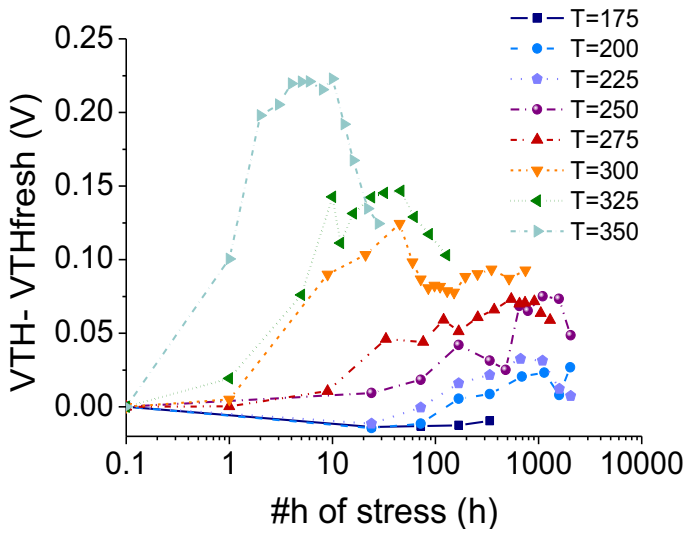


Figure 3.13: threshold voltage shift measured in saturation zone

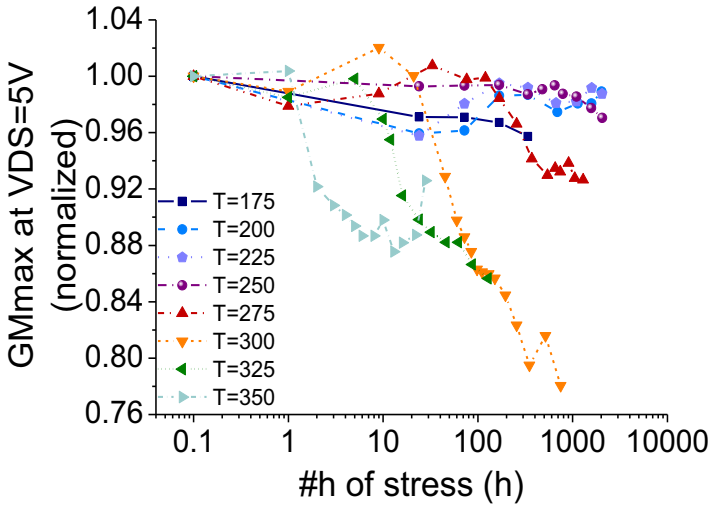


Figure 3.14: variation of the max g_m evaluated in saturation zone

The maximum transconductance value has been measured both in saturation (V_{DS}=5V) and in linear zone (V_{DS}=0.4V). If the maximum g_m in saturation zone is considered all the devices reported a strong decrease during the stress (Figure 3.14). A monotonic trend is reported at different ambient temperatures imposed, except for T_{AMB}=350°C. In this case, after a strong decrease shown until more than 10h, a slight increase is noticed until the end of the test. Similar

considerations can be done if the maximum transconductance is studied in linear zone Figure 3.15.

The transistor gate leakage current measured in ON condition (i.e. V_{GS}=0.4V) shows a behaviour consistent with the drain current measured in saturation zone. The transistor gate leakage current evaluated in OFF condition (i.e. V_{GS}=-1.2V) indicates a monotonic increase during the stress, in a consistent way with the GS diode gate current measured at V_{GS}=-1.2V, as it is states by

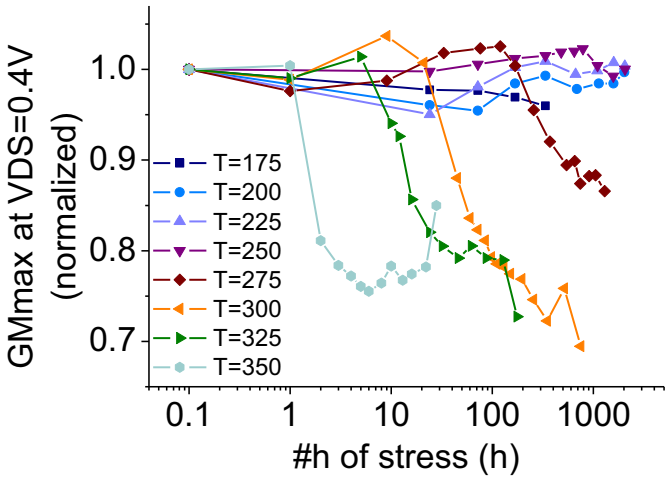
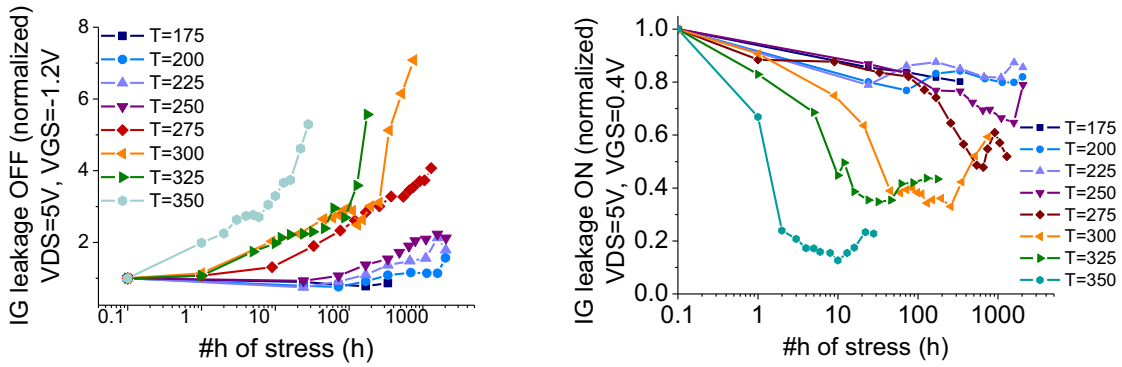


Figure 3.15: variation of the max g_m evaluated in linear zone



(a) (b)

Figure 3.16: variation of the transistor leakage current measured in (a) OFF and (b) ON state

From the analysis of the GS diode current when a forward bias is applied (i.e. V_{GS}=0.4V) it is possible to state a monotonic increase of the gate current (Figure 3.17). A consistent trend is noticed if GS diode current behaviour measured for different stress ambient temperatures applied is compared.

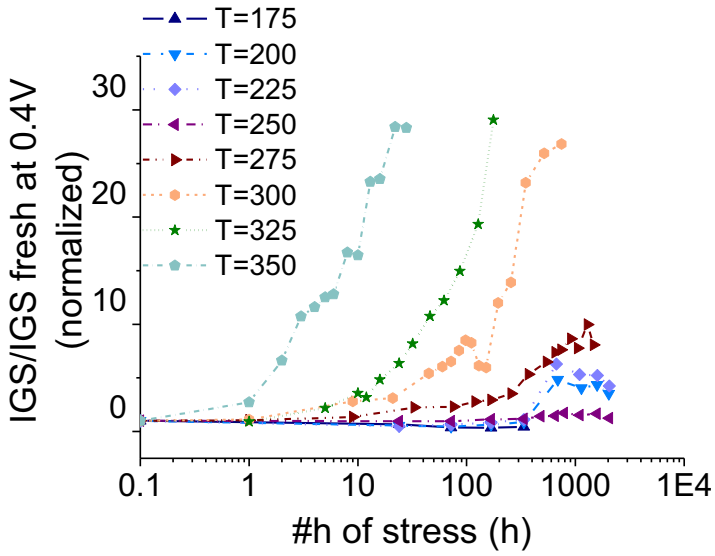


Figure 3.17: variation of the GS diode current when a VGS=0.4V is applied

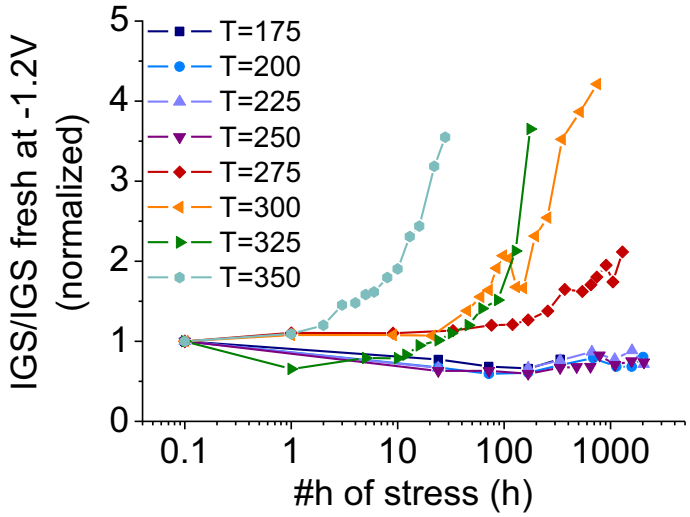


Figure 3.18: variation of the GS diode current when a VGS=-1.2V is applied

Pulsed analysis reveals that no significant variation is reported in the slump ratio evaluated during the stress in all the stress ambient temperatures applied. The variation follows a not monotonic trend; furthermore no significant correlation among different temperatures is reported. This aspect is confirmed in all the geometries analysed, thus excluding effects due to trapping phenomena aspects. The evaluation of the slump ratio variation is confirmed in Figure 3.19 which shows the average trend on devices characterized by a gate width of 0.2mm. In this case it has been decided to report the trend measured at V_{DS}=5V, V_{GS}=0.4V, thus at high dissipation condition in saturation zone, in order to choose a bias voltage (only at the drain terminal) near the operating point. Similar results have been reported when the slump ratio is considered in the knee voltage zone (V_{DS}=1V).

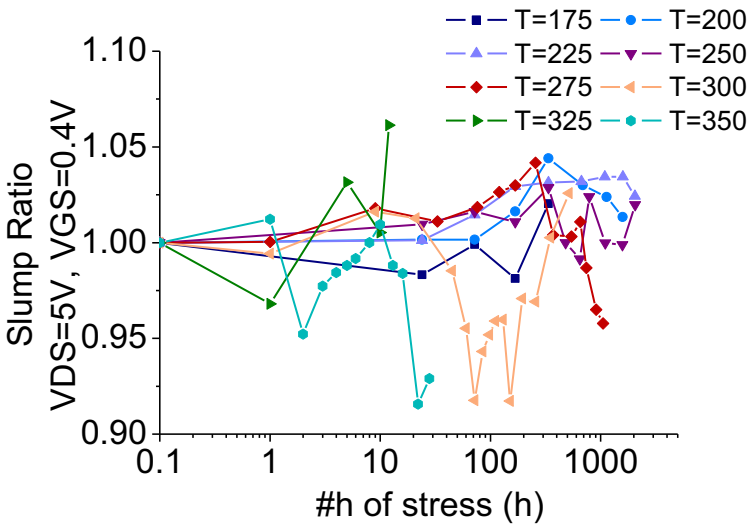


Figure 3.19: Slump ratio variation at VDS=5V, VGS=0.4V

3.3.3 Failure modes and activation energies

Figure 3.20 reports a detailed analysis of the drain current decrease on a representative device stressed at T_{AMB}=350°C. The OUT DC curve measured in a device before the stress, at the max I_{DSS} decrease and after the stress is shown. The saturated drain current strong decrease and recovery which face devices stressed at T_{AMB}=350°C is confirmed; moreover, as supported by the max g_m analysis, a meaningful decrease and recovery of the R_{ON} is stated.

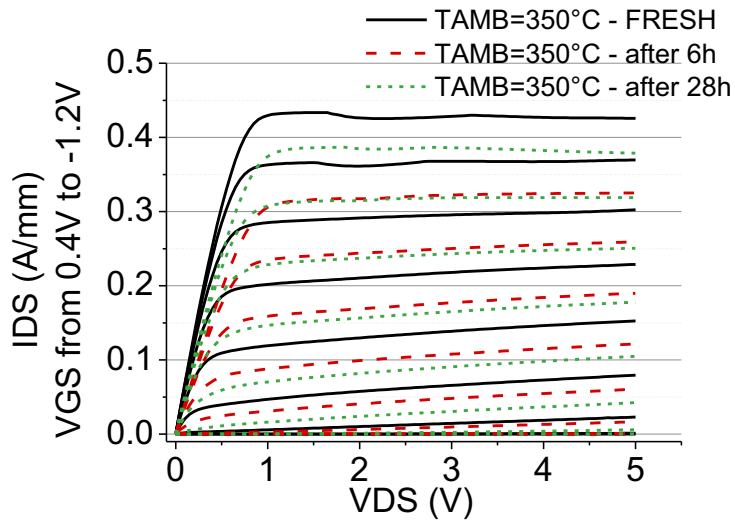


Figure 3.20: OUT DC characteristic of a device before, after 6h and 28h of stress at TAMB=350°C

The drain current trend suggests firstly the influence of the gate sinking phenomenon, supported by the g_m shift in the first step. Moreover, as indicated by Figure 3.21 the I_{DSS}

decrease can be due to the ohmic contact degradation. Figure 3.21 reports the detailed analysis of the g_m measured at a V_{DS}=5V carried out in the same step evaluated in Figure 3.20; the not monotonic trend of the g_m is noticed, confirming the R_{ON} evaluation.

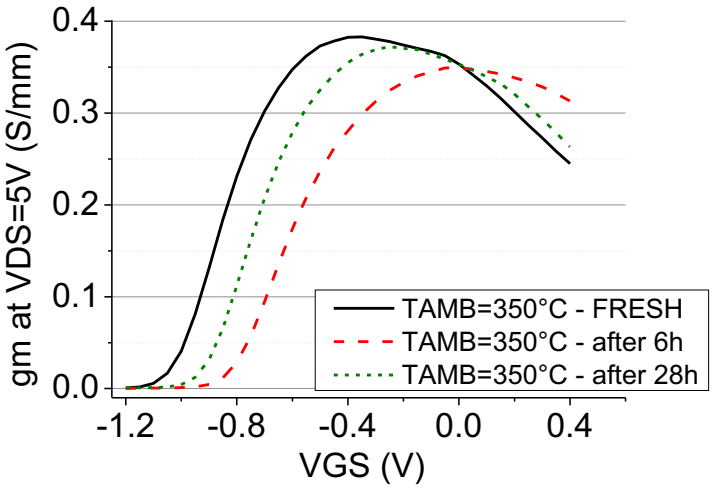


Figure 3.21: Transconductance in saturation zone of a device before, after 6h and 28h of stress at TAMB=350°C

Furthermore the not monotonic V_{TH} shift is shown, even if both gate sinking and ohmic contact degradation cannot justify the V_{TH} negative shift. Such behaviour can be defined by the monotonic trend confirmed in the GS diode current measured when a forward bias is applied Figure 3.17. In Figure 3.22 the I-V curve measured in a representative pHEMT before and after the stress and in correspondence of the maximum I_{DSS} decrease is reported.

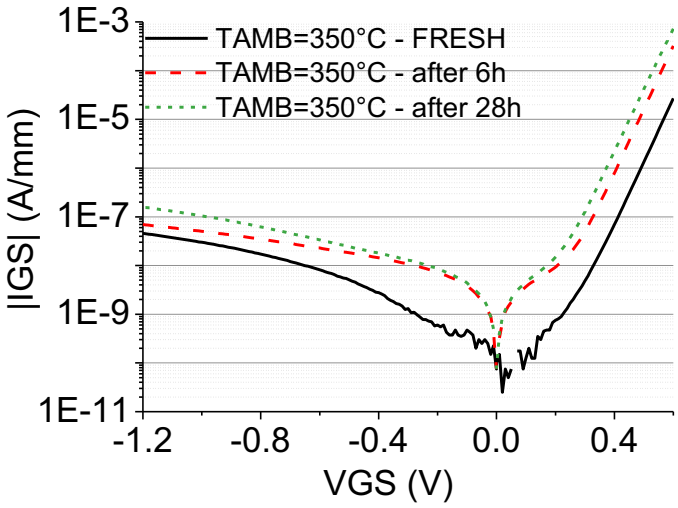


Figure 3.22: GS diode current measured before, after 6h and 28h of stress at TAMB=350°C

In order to find a correlation among the variation of the discussed parameters their activation energy has been measured and compared, considering the I_{DSS} and g_m decrease and diode current increase of, respectively, 10%, 5% and 300%. A activation energy of 2,14eV, 1.91eV and 1,98eV has been calculated, respectively (Figure 3.23).

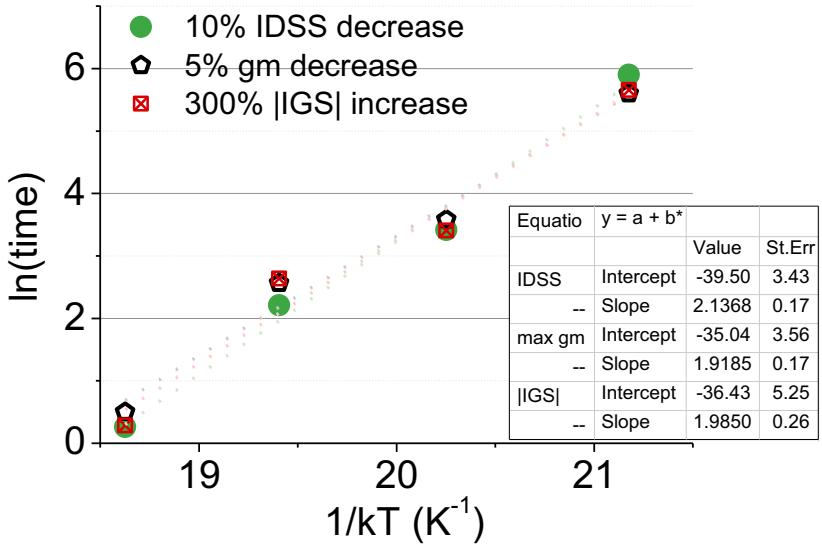


Figure 3.23: Activation Energy measured on 10% IDSS decrease, 5% g_m decrease, 300% |IGS| increase

3.3.4 Discussion about failure mechanisms

(i) Drain current decrease is firstly due to gate metal interdiffusion. Such phenomenon, deeply discussed in literature and known as "gate sinking", is supported by the threshold voltage positive shift. Moreover in the first step the threshold voltage positive shift is associated to a slight increase of the trasconductance value (Figure 3.24).

(ii) A second cause which determines I_{DSS} strong decrease is the degradation of the ohmic contacts. Such phenomenon is supported by the strong decrease of the maximum transconductance in devices stressed at higher temperature. The slight increase of the maximum transconductance shown in devices stressed at T_{AMB}=350°C is probably associated to a ohmic contacts annealing effect. This effect appears to be one of the reasons which lead to the drain current strong increase in pHEMTs tested at 350°C. However this mechanisms, as explained by Joh et al. [22] cannot clarify the threshold voltage negative shift.

In order to further investigate the ohmic contacts degradation end resistances have been measured. Figure 3.25 shows the end resistances R_D and R_S average value for a device characterized by W_G=8x50µm; consistent results have been noticed in devices characterized by different peripheries. Results are in agreement with the ones reported in Figure 3.14; it is

particularly possible to demonstrate that devices stressed at T_{AMB}=350°C are characterized by a max g_m value higher than the one found in devices tested at T_{AMB}=300°C or 325°C.

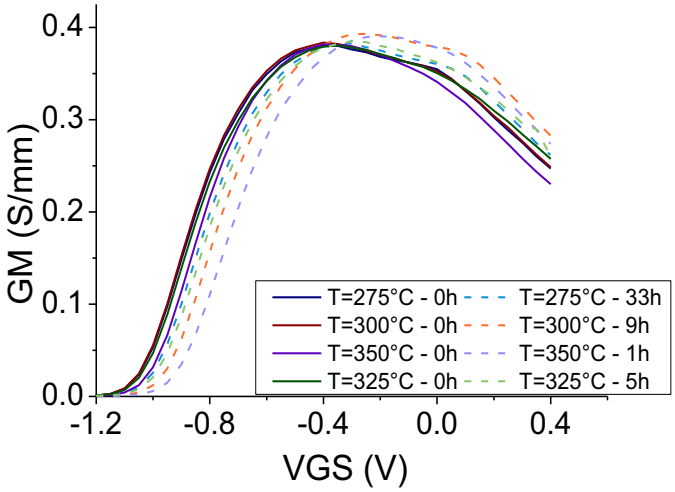


Figure 3.24: g_m max and v_{TH} variation at higher temperatures in the first step

(iii) The threshold voltage negative shift cannot be explained by de-trapping phenomena. Pulsed analysis revealed that trapping effects does not contribute to the I_{DSS} or V_{TH} variation. Moreover the drain current value measured faced no meaningful variation after a large amount of hours has passed.

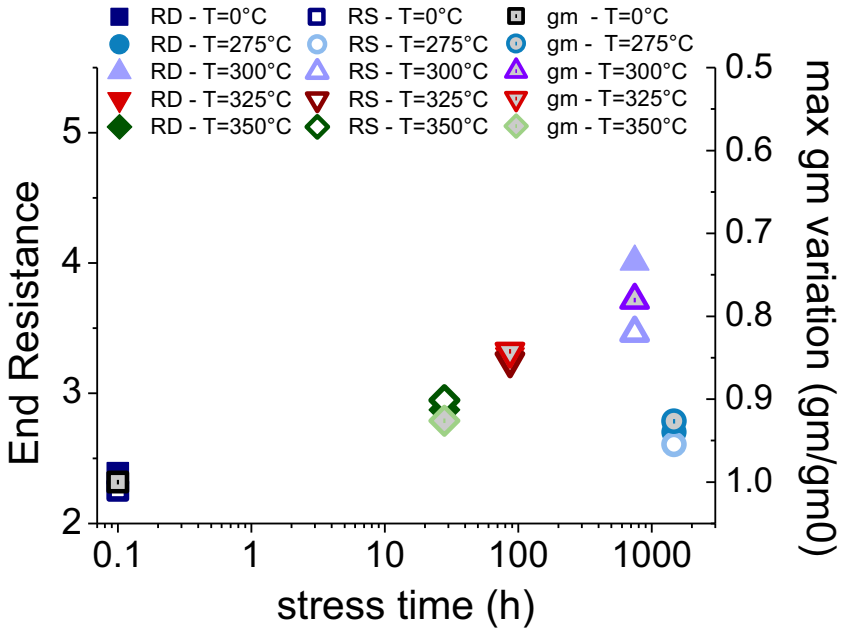


Figure 3.25: End resistance measurements and correspondence to transconductance peak variation

(iv) Considering the equation which defines the physical contributions to threshold voltage value, it is possible to make the hypothesis that the negative threshold voltage shift is due to a barrier height decrease. The barrier height decrease can be suggested by the monotonic and strong increase of the GS diode current measured when a forward bias is applied. Figure 3.26

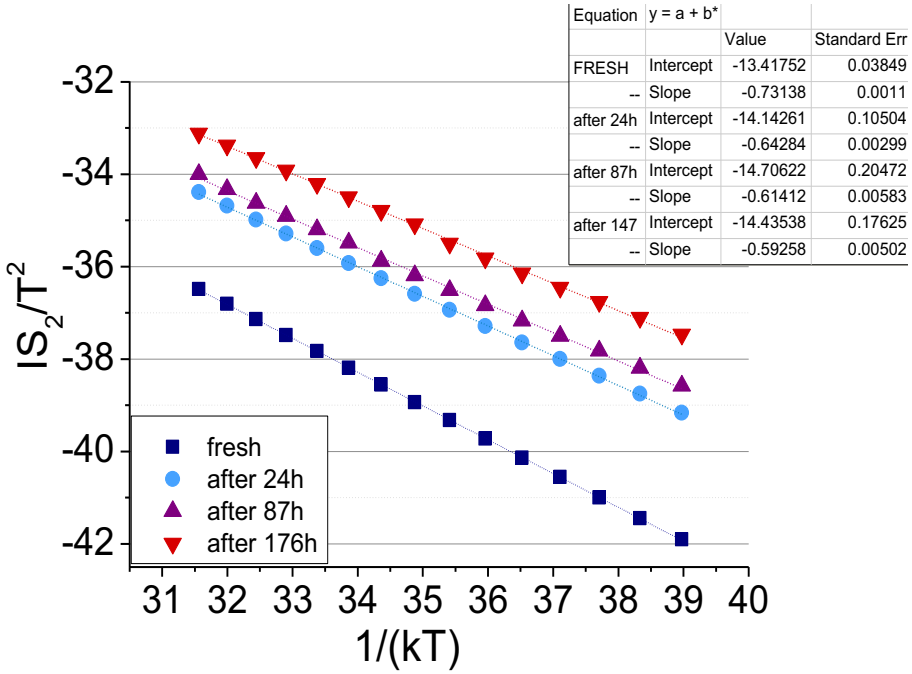


Figure 3.26:barrier height decrease on a device stressed at T_{AMB}=325°C

In order to better investigate the barrier height decrease it was decided to measure the barrier height value after each stress step. Barrier height has been calculated through diode I-V curve measured at several ambient temperatures imposed following the equations which state the relationship between Schottky diode gate current and temperature. The barrier height analysis revealed a monotonic decrease of the barrier height value in devices stressed at different temperatures, thus clarifying the presence of the threshold voltage negative shift. The barrier height analysis reported for a device stressed at T_{AMB}=325°C revealed a decrease in the barrier height from 0.73eV measured on a fresh device to 0.59eV on a devices stressed for 176h.

3.4 Channel temperature estimation

High Electron Mobility Transistors (HEMTs), based either on GaAs or GaN, are used for high power applications, and can reach high temperature levels during operation leading to significant effects on device performances and reliability. For an accurate thermal management, it is of fundamental importance to define methods capable of accurately estimating channel temperature under different operating conditions.

Over the last years, several techniques to evaluate junction temperature have been proposed in literature. For the estimation of channel temperature it is possible to apply electrical measurements. Thermal resistance (R_{TH})is calculated through the variation of a temperature sensitive parameter (TSP) measured as a function of both ambient temperature imposed and dissipated power and, thus, of the operating conditions. According to previous works reported in literature several parameters can be considered as TSP such as drain current measured in saturation region, as explained by [42], [43], on-state resistance (R_{ON})evaluated in the linear region, as shown in [43] or the forward voltage of GS diode curve biased at constant current [44]. For the channel temperature estimation it is preferable to employ pulsed measurements in order to avoid self-heating effects when the TSP variation as a function of the ambient temperature with no dissipated power must be considered.

A different approach to define thermal resistance and to evaluate temperature distribution employs optical analysis [45]. The main limit which affects optical measurements is the limited lateral resolution and the necessity of a dedicated set-up. Further issues are represented by the limited resolution given by the presence of metallization on the chip surface. The importance of optical methods is confirmed also by its use in multistage structures, such as MMIC power amplifiers, where significant interaction among stages can take place. Some of the optical methods previously explained in literature are: Raman micrography [46], spatially resolved photocurrent spectroscopy [47], infrared thermography [48], liquid crystal techniques which consists on the identification of “hot spots”, i.e. of regions where temperature reaches a local maximum.

The aim of this chapter is to provide for a detailed description of different techniques to estimate channel temperature of HEMTs and to present a critical comparison among them. The three methods compared within this work are: (i) the electrical DC technique proposed by McAlister et al. [43], hereafter called "DC method"; (ii) the electrical pulsed method presented by Joh et al. [42], hereafter called "pulsed technique"; (iii) the infrared thermocamera

evaluation. Results provide information on the advantages and drawbacks of these three methods, and detailed results on the thermal characteristics of GaAs pHEMTs.In order to confirm main advantages and limits of the methods the analysis has been extended to a four stage MMIC power amplifier. Furthermore cross thermal resistance due to interaction among different stages is evaluated.

3.4.1 Experimental details and results

All the measurements described within this paper are carried out on GaAs based multifinger pHEMTs with a gate length (L_G) of 0.25μm and seven different gate width (W_G) from 0.1mm to 0.96mm. Further information about devices has been provided in the previous paragraph.

DC Method

The experimental setup is composed by an Agilent 5263A parameter analyser, to measure the current-voltage (I-V) characteristics, and a Temptronik TP0315A-2 thermal chuck to impose a reliable and controlled chuck temperature. To verify the applied ambient temperature a Fluke thermometer has been used.

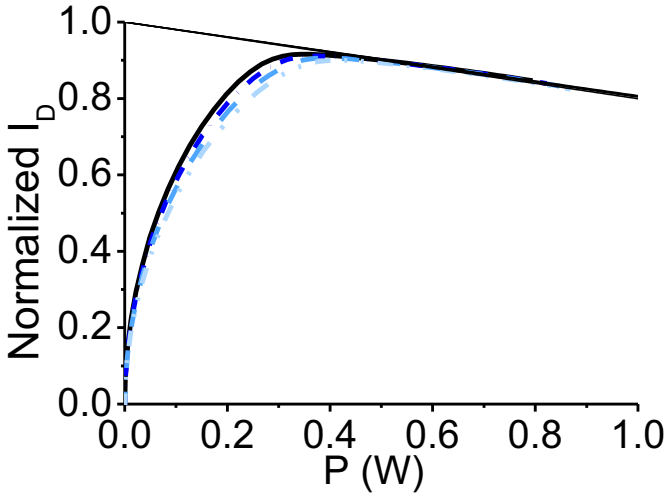


Figure 3.27: Normalized drain current as a function of added power for V_{GS} from 0.7V to 1V with 0.1V step

The DC method to estimate the channel temperature consists of two main steps: (i) measurement and (ii) calibration step. In the first case the variation of a TSP (in the case

explained the drain current in saturation zone) is measured as a function of the power dissipated. The relation between the drain current and the dissipated power is extrapolated from current voltage curves measured at different gate source voltage levels. Dissipated power is calculated as the sum of the product between current and voltage measured at the drain and gate terminal, although the second contribution can be considered in many cases as negligible. In the case proposed a V_{GS}, from 0.7 V to 1 V, is applied at a controlled ambient temperature of 25°C. From the linear regression of the I_D vs added power curve measured in the saturation region, the I_D value at a null added power is extrapolated. According to the method explanation provided by [43] such value can be defined as saturated drain current or I_{D0}. The I_D vs added power curve is then normalized for the corresponding I_{D0} for each V_{GS} value considered (Figure 3.27).

In the second step the TSP variation is studied as a function of the ambient temperature imposed. In the case presented the I_D vs added power curve is measured at V_{GS}=1V by applying chuck temperatures from 25°C to 175°C with 10°C step. In both the steps the same V_{DS} values have been used. The variation of the drain current as a function of ambient temperature imposed is shown in Figure 3.28. In order not to consider self-heating effects the I_{D0} value is considered.

From the variation of the TSP as a function of ambient temperature and dissipated power it is possible to define the relationship between estimated channel temperature and power, thus defining the thermal resistance value.

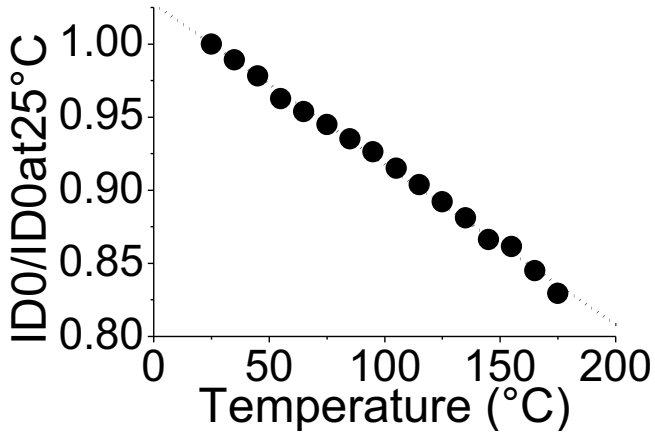


Figure 3.28: Normalized drain current at null added power as a function of temperature

The main drawback of the DC technique is the influence of device dimension on the measurement reliability. In devices with small periphery it is not possible to use this method since a not significant self-heating is reached leading to the impossibility of define a reliable I_{D0} value. In our case it was not possible to measure devices with gate width lower than 0.4mm. Furthermore it is of fundamental importance to have a linear decrease of the drain current as a function of drain voltage and, thus, dissipated power, due to the channel temperature reached.

Indeed the eventual presence of phenomena such as oscillations or kink effect strongly influence channel temperature estimation accuracy. In our case it was not possible to measure devices with a gate width higher than 0.9mm as a consequence of oscillations.

Pulsed Method

Pulsed technique employs a custom setup similar to the one used for pulsed measurements and described in the previous section. The setup is composed by two pulser to bias the gate and the drain terminal and an oscilloscope. Furthermore the temperature is controlled by a Temptronik thermal chuck and verified by a Fluke thermometer.

Consistently with the DC method, the technique can be divided in two main steps: (i) measurement step and (ii) calibration step. The TSP (temperature sensitive parameter) variation is studied as a function of dissipated power when a constant temperature is applied and as a function of chuck temperature when the device is biased with null power, respectively. In order to provide for an accurate comparison the bias point used to calculate the TSP variation in both the steps must be consistent. In our case it was considered the drain current value measured at high dissipation condition in saturation zone (V_{DS}=5.5V and V_{GS}=-0.2V).

In the measurement step the drain current vs voltage curve is defined by pulsing from different power dissipation levels. In order not to induce device degradation a maximum power dissipation of 2W/mm was imposed, on the basis also of device dimensions. A I_D vs P trend is defined by measuring the dissipated power for each baseline (Figure 3.29). During the calibration step the drain current is measured at for several ambient temperature levels from 25°C to 185°C with 10°C step in order to define a I_D vs T curve (Figure 3.29).

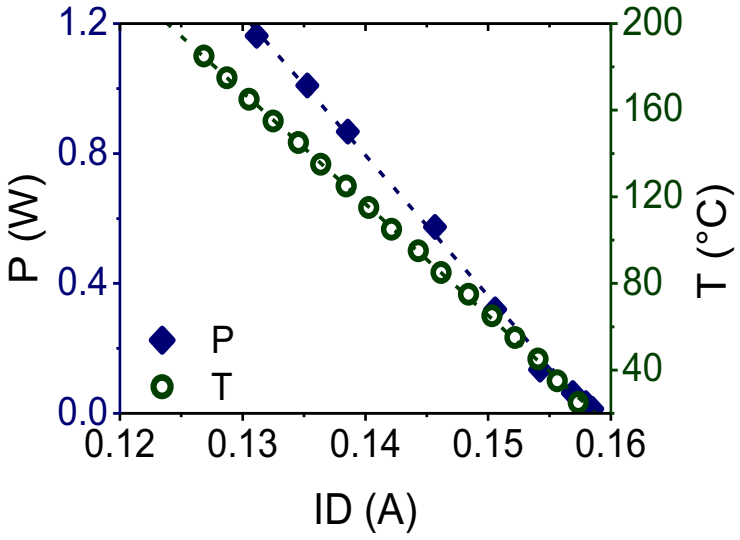


Figure 3.29: Trend of TSP variation as a function of ambient temperature and dissipated power

In both measurement and calibration step a pulse width of 2.5μm and a duty cycle of 0.5% was used. Pulse width was decided in order to avoid self-heating. Results on the dependence of drain current on temperature and power dissipation level allow one to extrapolate the relationship between channel temperature estimation and dissipated power, and thus to define the thermal resistance.

A drawback of the pulsed technique is given by parasitic or external capacitances and the consequent lowest limit of the pulse width. If the pulse width is lower than the time required to charge the parasitic or external capacitance the drain source voltage applied during the pulse width will not be constant and it will lead to a not reliable estimation due to the consequent dependence of the drain current width on time during the pulse. In the method proposed the time constant is defined either by parasitic resistances, either by a resistance included in the custom pulsed system between the drain terminal of the pHEMT and the pulser to measure the current.

Infrared thermal camera

This method employs an optical technique by means of a IR thermal camera to measure the channel temperature in the device. The pHEMT is biased with a power supply (in our case an Agilent 3631) while the channel temperature is evaluated with a FLIR SC325 infrared thermal camera, characterized by a IR resolution of 320x240 pixels and a detector pitch of 25μm. A further lens with magnification 2x has been used leading to a resolution of 50μm.

In the case proposed the device was biased with a constant drain source voltage value (V_{DS}=6V) for several different gate source voltages imposed (V_{GS} from 0.2V to 0.7V). For each power dissipation level imposed the correspondent temperature has been measured. In the case presented the considered temperature corresponds to the maximum value in the area considered.

The resolution provided by the IR camera and by the magnification lens limit the possibility of evaluating channel temperature in devices with small dimensions. In our case it was not possible to evaluate devices with gate width lower than 0.6mm due to the setup resolution. On the other hand devices with a high gate width reveal strong oscillations which impede the use of an optical method due to the impossibility of biasing the device in a reliable way.

A further drawback is given by the presence of metallization or air bridge. In our case, although the presence of air bridge and the consequent significant lack of accuracy, it was possible to measure the channel temperature

3.4.2 Experimental Results

It was possible to use DC method to estimate channel temperature only in three pHEMTs with different gate periphery from 0.4 mm to 0.9mm. Results demonstrate that the thermal resistance value increases as a function of gate width with a linear trend, as demonstrated by Figure 3.30.

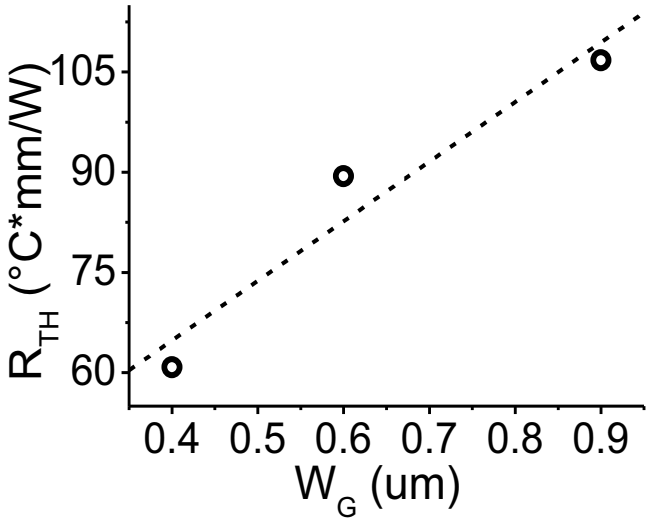


Figure 3.30: thermal resistance evaluation with DC method for devices with different gate peripheries

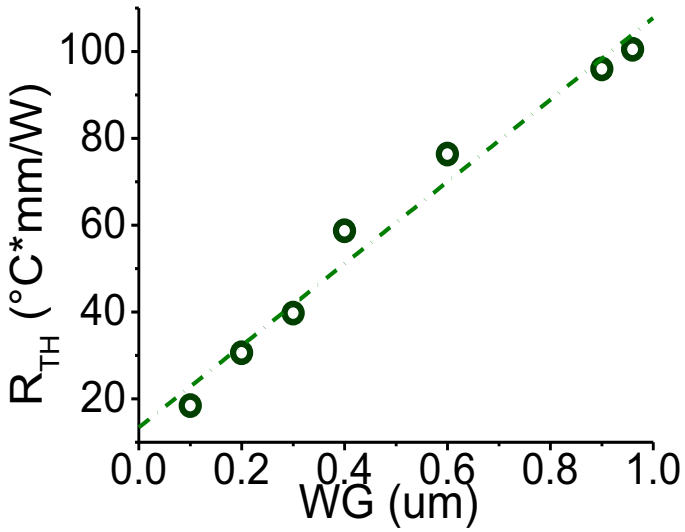


Figure 3.31: R_{TH} pulsed analysis measured for several peripheries

All the analysed pHEMTs revealed no significant parasitic or external capacitances. It was possible to use a pulse width value short enough not to influence the estimation with self-

heating effects but much higher than the time required to charge the parasitic capacitances. As a consequence it was possible to measure all the devices in the PCM. Eight devices with different geometries and gate width from 0.1mm to 0.96mm have been measured. Consistently with DC method results the thermal resistance curve as a function of gate width can be defined by a linear trend (Figure 3.31).

As a consequence of both oscillations and device dimensions it was possible to measure with optical method only pHEMTs with gate periphery of 0.6mm. Details are provided in the discussion about results.

3.4.3 Discussion about results

To study the reliability of the techniques proposed to estimate channel temperature a comparison of results obtained on the same device is proposed. The device is characterized by W_G=10x60µm, L_G=0.25µm and gate pitch of 20µm. A R_{TH} of, respectively, 149.0 °C/W for the DC method, 127.1°C/W for the pulsed method and 47.5°C/W for the optical method is reported in Figure 3.32, stating a consistency between DC and pulsed measurement.

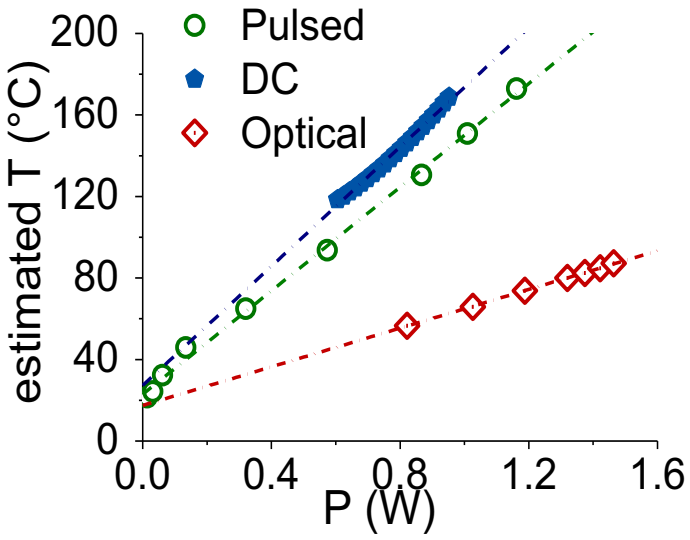


Figure 3.32: Comparison of RTH evaluation with several methods

From the comparison between DC and pulsed method it is possible to state that a quite higher thermal resistance value is measured in the first case. The intercept value of the curve (27.28°C), which describes the estimated temperature when no power is dissipated, is consistent with the ambient temperature applied during the measurement step.

DCmethod is influenced by the following inaccuracies: (i) The first cause for the slight overestimation is due to the not linear dependence of drain current in saturation zone on power and temperature. Furthermore inaccuracies are introduced by the not linear variation of TSP with power dissipated for small power dissipation levels, as it is suggested by I_D vs P during pulsed measurements (Figure 3.29). (ii) Inaccuracies are introduced by the estimation of the dissipated power. Indeed the gate contribution to dissipated power can be significant. In our case the dissipated power was calculated considering only the drain contribution, leading, in the worst case, to a inaccuracy of 1%. In many cases the gate contribution cannot be considered as negligible, especially as a consequence that, to achieve a significant self-heating, high gate source voltage and current values are considered. (iii) The presence of DC trapping can influence the drain current trend and, thus, the channel temperature estimation by leading to a not reliable trend to describe the variation of drain current as a function of ambient temperature imposed. (iv) The small range of dissipated power considered can influence the thermal resistance value. The analysis can vary on the basis of the range considered and does not provide reliable information about channel temperature estimation trend at low dissipated power levels.

Pulsed method slightly underestimates the results. The intercept value (22.89°C) is consistent with the ambient temperature applied during the measurement phase (Figure 3.32). (i) Pulse width is one of the main issues to obtain measurement reliability. The influence of self-heating during calibration step can lead to a different drain current variation as a function of ambient temperature imposed and, thus, to an underestimation of the channel temperature. For this analysis we chose a duty cycle of 0.5%: analysis with longer duty cycles provided significantly different results (for instance, with a duty cycle of 1 % we found an underestimation of 21 °C/W), thus indicating that a significant self-heating occurs also within the calibration phase.

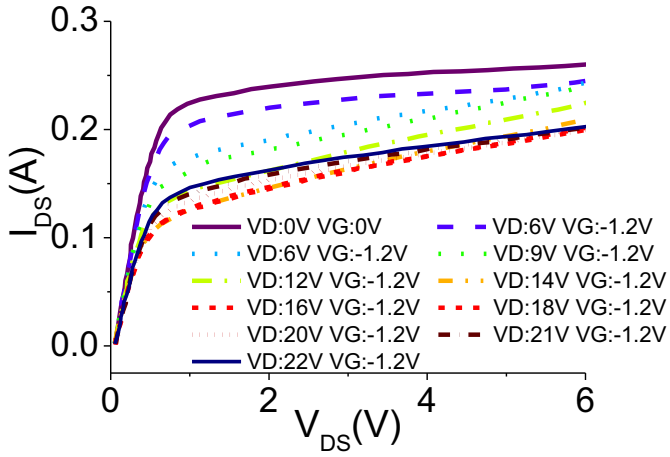


Figure 3.33: Analysis of trapping effects during pulsed evaluation: I_{DS} vs V_{DS}trend

(ii) Differently from DC technique pulsed measurements are much more influenced by trapping effects. These effects affect both the intercept value and the thermal resistance. It is important to choose for the comparison a bias point which does not strongly depend on traps and to impose, whether possible, power dissipation levels not highly affected by traps and degradation. Figure 3.33 shows the traps evaluation on the same device used for the thermal resistance analysis. A maximum current collapse of 18.4% is noticed when the device is biased with the same quiescent points and V_{DS} used for the R_{TH} evaluation; I_D-V_G analysis confirmed that the current collapse is due to a threshold voltage shift (Figure 3.34). Two R_{TH} values have been measured with the same measurement step, and a calibration step evaluated before and after the measurement step. A difference of 13°C/W in the thermal resistance and of 24°C in the intercept value (i.e. estimation of the ambient temperature imposed during the power map evaluation) has been noticed. (iii) Inaccuracies introduced by considering only the drain contribution in the power dissipation calculation can be considered as negligible. Indeed pulsed measurements are carried out at lower V_{GS} levels (V_{GS}=-0.2 V);

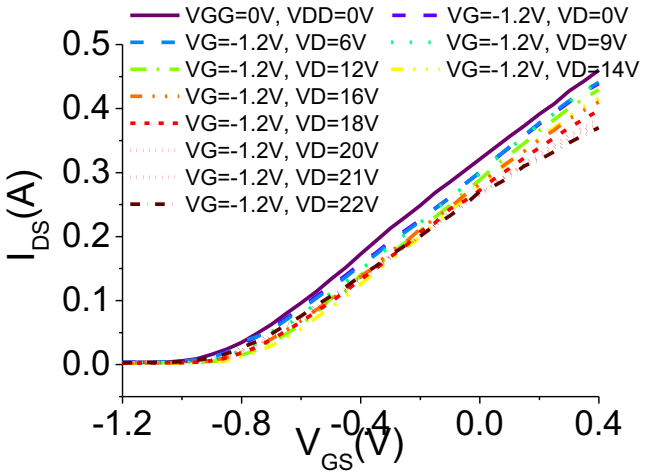


Figure 3.34: Analysis of trapping effects during pulsed evaluation: I_{DS} vs V_{GS}trend

Channel temperature estimated with IR thermal camera, as already shown by previous works reported in literature [46],[48], strongly underestimates thermal resistance results. The inaccuracy is mainly introduced by limited resolution, which is comparable with the device gate width. Furthermore the device small dimension and the presence of air bridge increases the lack of accuracy. Further imprecision in the channel temperature estimation is provided by a different emissivity and reflectivity coefficient which characterize the material on the surface, although a preliminary emissivity calculation has been done controlling and verifying the temperature with a thermal chuck and a thermometer.

3.4.4 Experimental Results on power amplifiers

In order to confirm the results obtained on pHEMTs it has been decided to further extend the analysis on a four stage MMIC power amplifier, evaluating the thermal resistance on each single stage. It was not possible to carry out pulsed measurements, as a consequence of the presence of external capacitors to prevent oscillations. For each stage chip capacitors of 100pF and SMD capacitors of, respectively, 100pF and 2µF have been used. In DC evaluation, during the measurement and calibration step the same parameters considered for pHEMTs analysis were used, except for the V_{GS}; a V_{GS} from 0.2 to 0.6V with 0.1V step was applied not to damage the device. For the same reason during IR measurements a V_{DS}=6V and a V_{GS} from -0.6 to 0V with 0.05V step was used. MMIC evaluation confirms that IR measurements underestimate channel temperature and that underestimation varies with device dimension (Figure 3.35).

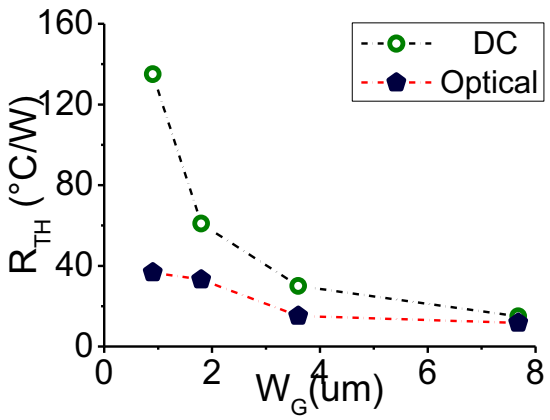


Figure 3.35: Comparison between R_{TH} of power amplifier measured with IR thermocamera and DC evaluation

In a multi-stage configuration, the temperature of one stage can be influenced by the power dissipated on the other stages. In order to evaluate the thermal interaction between the different stages, measurements were carried out with IR evaluation; it was not possible to adopt the DC method because the power amplifier cannot be heated with a temperature higher than 105°C. Each stage of the power amplifier was biased in two conditions: (i) only one stage was biased and all the other were kept in OFF condition, (ii) all the stages were biased with the same V_{GS} with no RF signal in order to consider the worst condition.

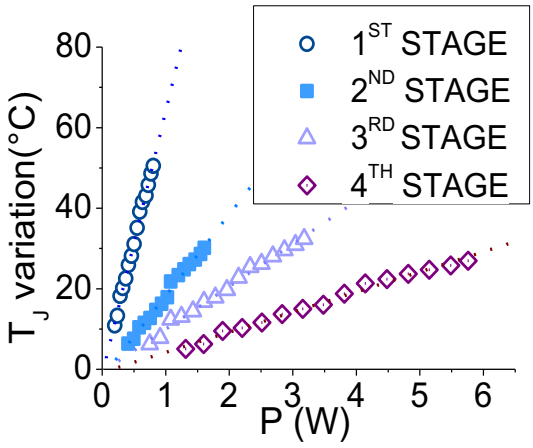


Figure 3.36: Temperature variation due to mutual influence between stages

From the difference of the junction temperature measured in both the conditions it was possible to calculate the cross thermal resistance value and to evaluate the influence of other stages in a four stage MMIC power amplifier. The analysis on different stages states that the influence of different stages depends on the periphery of the stage considered (Figure 3.36). The smallest stage, composed only by one pHEMT with 0.9mm gate width, is the most influenced stage, demonstrating a cross thermal resistance higher than 50°C/W (Figure 3.36).

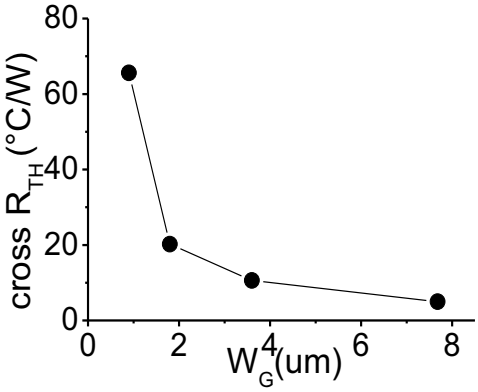


Figure 3.37: cross R_{TH} in a four stage MMIC power amplifier

3.5 HTOL TEST

The importance of defining a reliable thermal resistance value is essential to determine the device channel temperature at operating conditions and to establish a correct relationship between channel temperature reached by the device and dissipated power. On the basis of the results provided by the thermal resistance analysis a thermal stress with DC bias applied has been carried out. Four stages MMIC power amplifiers have been tested. Due to issues related to oscillations, ground connections and cross thermal resistance, it has been decided to stress only the first stage. DC measurements have been done on the first stage at every step of the stress, in order to monitor the DC main parameters.

During the test eleven boards have been stressed up to 2000 hours in four different conditions: (i) a high current condition (T_J=250°C, T_{AMB}=75°C); (ii) a low current condition, where a junction temperature T_J=225°C and an ambient temperature T_{AMB}=105°C are imposed; (iii) a medium high current condition, where a junction temperature T_J=225°C and a ambient temperature T_{AMB}=75°C are imposed; (iv) a medium low current condition, where a junction temperature T_J=250°C and a ambient temperature T_{AMB}=105°C are imposed.

Consistently with the low junction temperature imposed no significant degradation has been noticed in all the DC parameters measured in devices stressed. Some devices stressed show a significant degradation of the GS diode current, demonstrating in two cases also a failure in the inductance of the first stage. According to the negligible variation shown in drain current and threshold voltage the gate current degradation is probably due to the failure of external SMD capacitor with the high ambient temperature imposed.

3.5.1 Experimental details

Eleven four stage MMIC power amplifiers have been tested with HTOL test. The setup for the accelerated test is composed by a power supply to bias the device and thermal chambers to impose a constant ambient temperature.

At each step main parameters are monitored with DC analysis with a parameter analyser. Through DC characterization GS diode reverse and forward current, output I_DV_D and I_GV_D characteristic, I_DV_G and I_GV_G transcharacteristic and transconductance (g_mV_G) have been measured. Similarly to the long term thermal stress main parameters considered for the analysis are: (i) drain current measured in saturation zone, (ii) max g_m reported in linear and saturation

zone, (iii) transistor gate leakage current measured in OFF and ON state, (iv) diode current measured with reverse and forward bias applied, (v) threshold voltage (V_{TH}). As a consequence of external chip and SMD capacitors it was not possible to monitor devices with pulsed characterization.

Considering mutual influence among stages, preliminary issues related to power amplifiers mounted on boards and preliminary HTOL tests carried out at higher junction temperatures on all the stages, it has been decided to stress only the first stage of each board and to adopt a lower temperature, and thus a lower V_{GS} value in order to limit the degradation. It has been decided to stress only the first stage because it is the most sensitive due to (i) R_{TH} value measured on a single stage, (ii) considerations about mutual influence among stages. During the stress it has been decided to consider, for the first stage of all the boards tested, a thermal resistance value of 140°C/W. This value agrees with the thermal resistance measured with indirect electrical DC analysis and with correspondent simulations. During the stress the same V_{GS} value was used for all the boards stressed at the same nominal T_J and T_{AMB} value, resulting in negligible differences in the drain current value due to board and power amplifier variability, and, as a consequence, in a negligible variability in the junction temperature imposed. Finally, considering the not meaningful variation of the drain current value during the test (i.e. after 2000h), the V_{GS} value has been kept constant during the whole test. According to drain current decrease no significant inaccuracies have been introduced.

Devices have been tested up to 2000 hours in four different conditions: (i) a high current condition, where a junction temperature T_J=250°C and a ambient temperature T_{AMB}=75°C are imposed; in this case a drain current of approximately 0.205A is required and a correspondent V_G=-0.12V is imposed. (ii) a low current condition, where a junction temperature T_J=225°C and a ambient temperature T_{AMB}=105°C are imposed; a drain current of approximately 0.141A is measured and a correspondent V_G=-0.37V is imposed. (iii) a medium high current condition, where a junction temperature T_J=225°C and a ambient temperature T_{AMB}=75°C are imposed; In the third condition a drain current I_D=0.176A and a correspondent V_G=-0.24V are imposed. (iv) a medium low current condition, where a junction temperature T_J=250°C and a ambient temperature T_{AMB}=105°C are imposed. In the fourth condition a drain current I_D=0.171A and a correspondent V_G=-0.22V are imposed.

3.5.2 Experimental Results

According to the relatively low junction temperature reached during the test no significant variation has been reported in main DC parameters. An example of the analysis has been

reported for devices stressed in the first condition, thus in the high current condition. Similar results have been shown on devices tested with different conditions.

Many devices reported a strong degradation of the GS diode current, demonstrating a significant increase both when forward and reverse bias are applied. Consistent results have been noticed in the transistor gate leakage current. Figure 3.38 shows an example of diode current measured during the stress in a device tested in the first and second condition, respectively. According to the low variation of further parameters, such as drain current measured at high dissipation and operating condition or the threshold voltage, we can make the hypothesis that the gate variation is due to the external circuitry and not to the transistor.

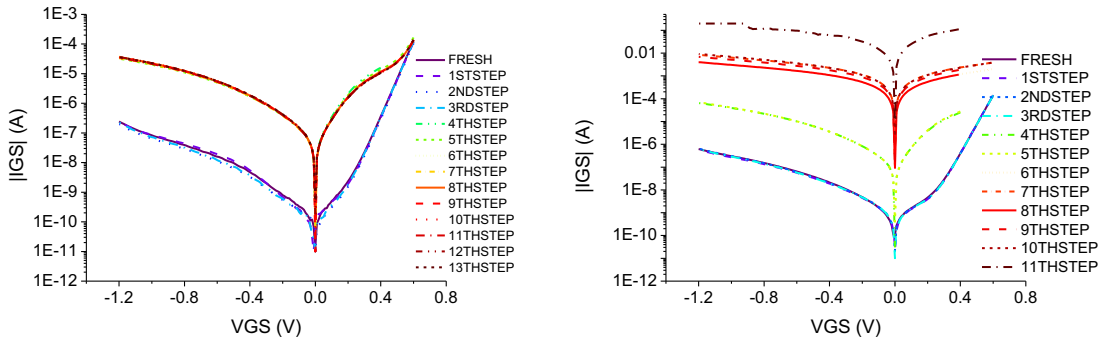


Figure 3.38: gs diode variation in a device stressed in the (a) first condition and in the (b) second condition

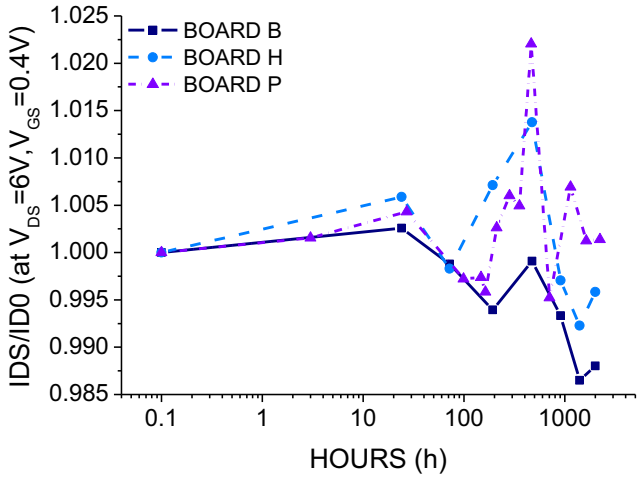


Figure 3.39; drain current variation measured at high dissipation condition – HTOL test 1st condition

No significant variation of the drain current measured in saturation zone at high dissipation condition is noticed (Figure 3.39). In all the conditions imposed a variation lower than 2% is

noticed. For each condition imposed no variability is noticed in different devices stress with the same DC bias.

On the contrary a significant variation is shown if the drain current is measured at operating point (Figure 3.40). This variation is not monotonic: after a strong increase reported in the first step a monotonic decrease is noticed up to 2000h of stress. A variation of 8%, 7%, 9%, 12% is noticed in the four conditions, respectively. Considering that a low drain current value is measured at operating point and that a maximum variation of 5mA is measured in the worst case, this variation can be considered as negligible. Consistent results are shown in the correspondent threshold voltage analysis; a variation lower than 25mV over V_{TH}=-0.9V is reported in the worst case (Figure 3.41).

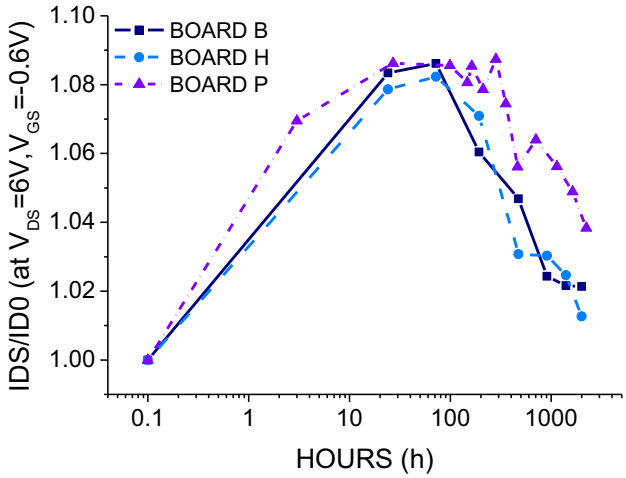


Figure 3.40: drain current variation measured at operating condition – HTOL test 1st condition

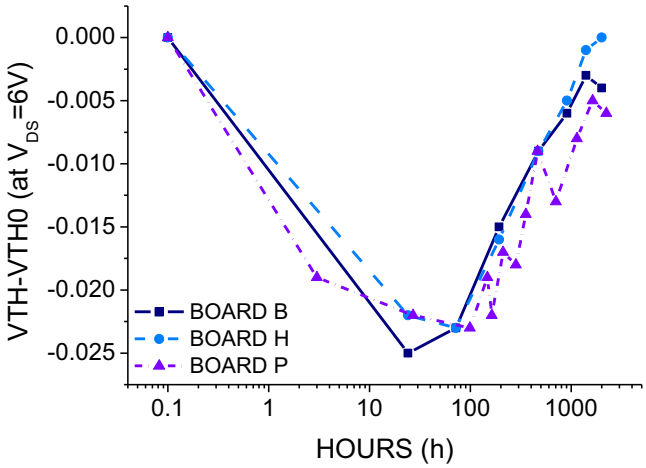


Figure 3.41:VTH variation – HTOL test 1st condition

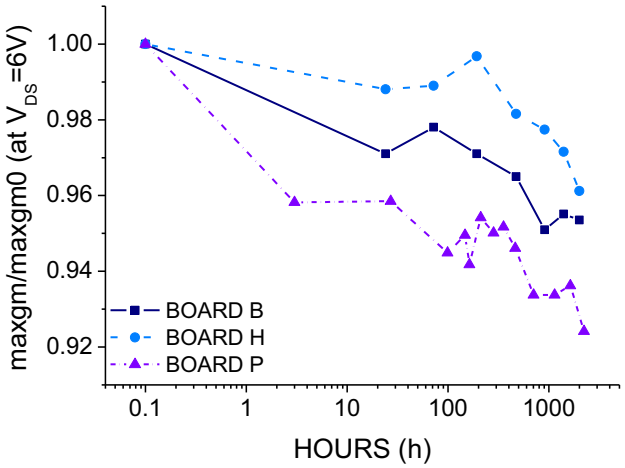


Figure 3.42: (a, (b) variation of max g_m in saturation zone - HTOL test 1st condition

Finally, through the transcharacteristic variation, the maximum trasconductance value has been calculated in the linear region (V_{DS}=0.4V) and in the saturation zone (V_{DS}=6V), demonstrating consistent results in both the conditions (Figure 3.42). In both the cases a strong variation is shown in the linear step, demonstrating a variation in the linear zone between 10% and 14% after 2000h of stress. The decrease in the saturation zone reaches a value between 2% and 6% after 2000h of stress. Since no variation is reported in the I_{DS} value it is possible that a contribution to the decrease of the maximum trasconductance value is due to an increase of parasitic series resistance, with a possible contribution of the external circuitry.

3.5.3 Discussion about results

Consistently with the results provided in the long term thermal storage stress no significant variation is noticed in the drain current measured in saturation zone when a junction temperature lower than 275°C is applied up 2000h. A not significant variation is measured also if threshold voltage is considered. If we compare the V_{TH} trend measured in a pure thermal storage and in a HTOL test we can notice consistent results (Figure 3.43, Figure 3.44). Furthermore we can make the hypothesis that the thermal resistance has been underestimated. This hypothesis is also supported by the difference between devices tested at the same junction temperature with different ambient temperature. We have not compared the max transconductance or the gate current variation, although significant degradation has been reported, since we can make the hypothesis that this variation is not due to the transistor but to the external circuitry.

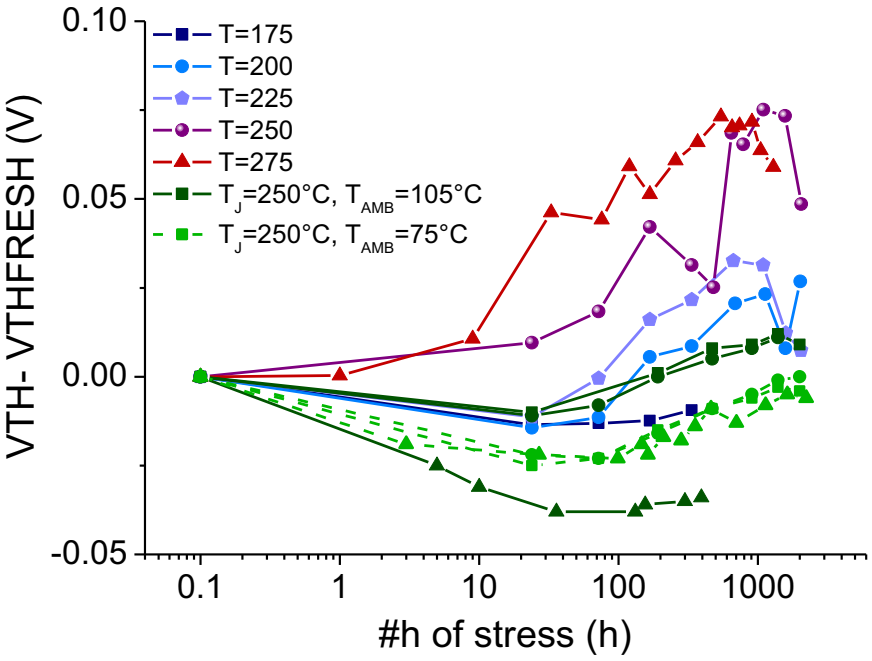


Figure 3.43: Comparison between VTH variation in pHEMTs tested with a pure thermal storage and MMIC power amplifier tested at Tj=250°C

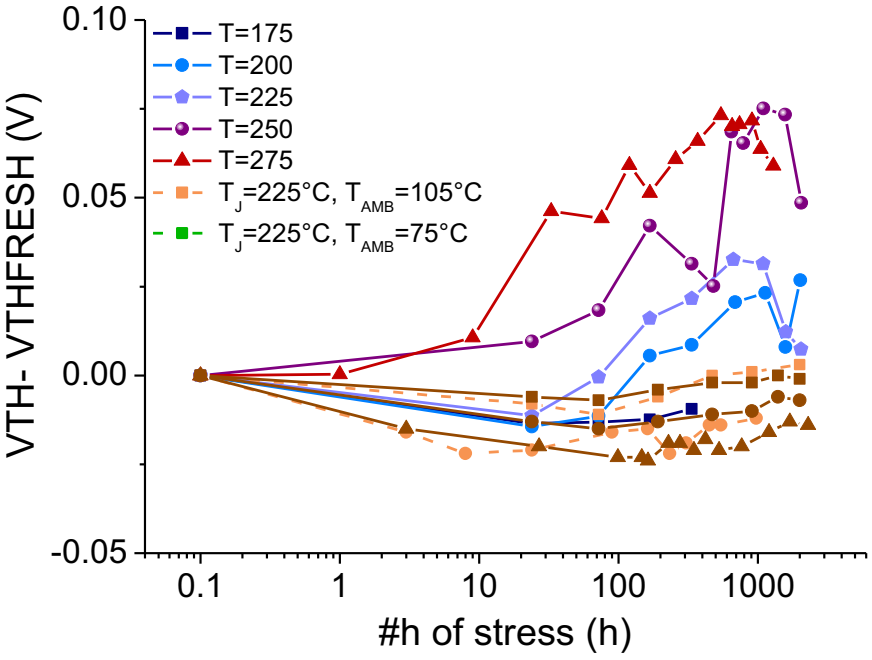


Figure 3.44: Comparison between VTH variation in pHEMTs tested with a pure thermal storage and MMIC power amplifier tested at Tj=225°C

Chapter 4:Electrostatic discharge effects

4.1 Fundamentals about ESD effects

In this chapter a short summary to describe fundamentals about ESD effects is proposed. In the first paragraph a preliminary description of main failure mechanisms and modes described in literature is provided [49], [50]. Degradation is mainly due to the high current and electric field consequent to the ESD phenomenon. Main effects are metal diffusion into the semiconductor, lateral material migration, contact spiking, melt filamentation and electromigration [49].

In the second paragraph methods to emulate ESD effects on devices are described [51]: (i) HBM, (ii) MM, (iii) TLP. HBM (Human Body Model) simulates a ESD phenomenon where a charged body transfers its electrostatic charge to a device. MM (Machine Model) was firstly introduced in Japan to study a different case than the HBM model. It simulates an electrostatic discharge from a charged machine, fixture or tool, thus leading to a more rapid and severe phenomenon. In this chapter we have decided to describe only measurements carried out on devices, not describing further important techniques such as charge device model or socket device model.

In the last paragraph a description of main ESD protection circuit is defined. Main structures used in a MMIC power amplifiers are: (i) Schottky diodes [52], [53], (ii) resonant circuit by means of inductors and capacitances [54]. The second structure is used especially in the input and output terminal of a RF device, while the first structure can be used in the gate terminals by using a chain of more diodes in series in an antiparallel configuration.

4.1.1 Failure modes and mechanisms due to ESD effects

Compound semiconductors are more sensitive than Si devices to ESD. Several properties lead to a worse behaviour [49]: (i) higher susceptibility to transient pulse stress, (ii) lower melting point (except for GaP), which, according to simulations, are about one order of magnitude lower than Silicon; (iii) lower thermal conductivity and specific heat; (iv) higher defect density which can lead to an easier development of burnout.

The flowing of large current densities, for instance when an electrostatic discharge takes place, induces high temperature and local high electric fields. Thus, depending on the time scale

and the power density, ESD can cause a localized damage or an extended melting of the structure affected. In compound semiconductor structures several mechanisms can occur, mainly due to the presence of metal layers required for Schottky and ohmic contact and epitaxially grown multi-layer structures required to generate a high electron mobility transistor. According to literature [49],[50] main mechanisms can be: (i) metal diffusion in the semiconductor, (ii) lateral material migration across the semiconductor surface between electrodes, which is mainly due to high electric field and which can lead to a consequent electrode short circuit bridge; (iii) contact spiking caused by focused current flow; (iv) melt filamentation due to current flow on a localized region; (v) degradation due to electromigration effects. A scheme to explain ESD degradation in MESFET is shown in Figure 4.1.

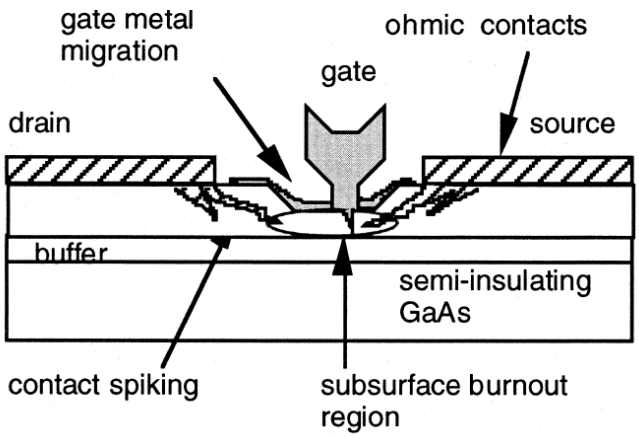


Figure 4.1: ESD degradation in MESFET [49]

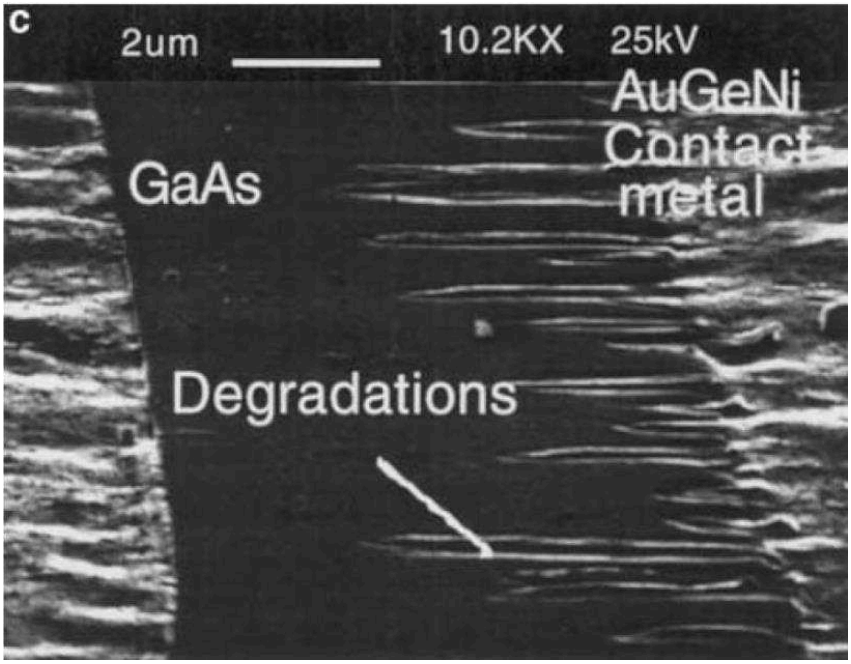


Figure 4.2: Gate blow off in a MESFET [49]

One of the main phenomena which occurs after ESD in GaAs FETs is the lateral material migration, which can cause short circuit with neighbouring metal and contacts, usually in the form of filaments (Figure 4.2, Figure 4.3). The focused current flow due to ESD phenomenon can induce a short circuit in the Schottky junction, thus generating metal semiconductor interdiffusion which can be described by metal contact spiking [49]. One of the main consequences is the creation of gate metallization melting leading to the presence of voids in the gate metal or to the removal of the entire gate (Figure 4.4). This phenomenon is usually called "gate blow off" [49],[50] (Figure 4.3).

Ohmic contacts, usually composed by AuGeNi, determine a degradation of devices like MESFETs or HEMTs after ESD phenomena. Although degradation is mainly due to material migration, two typologies of failure can be noticed. The first one consists of metal migration when the contact faces a high electric field with no significant dissipation of heat (Figure 4.5). A strong degradation occurs when, as a consequence of the large current generated, the sample is heated and a large amount of metal is transported. In the second case devices are usually characterized by a low resistance value. Contact material is determined after a molten metal bridge is generated due to the generation of a defined voltage. This phenomenon can lead to electronic charging by impact ionization or to the generation of thermal transient near the contact edges. A solution to the second typology can be provided by the use of refractory metals such as WSi in the contact or by the employ of a gate recess in order to reach a lower electric field between the contacts.

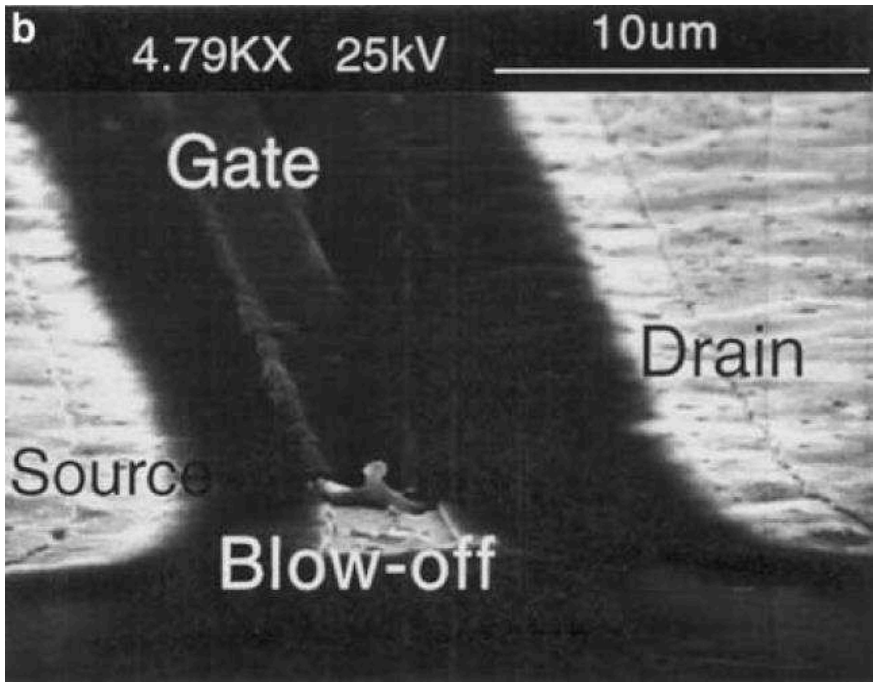


Figure 4.3: Ohmic contact degradation after ESD phenomenon [49]

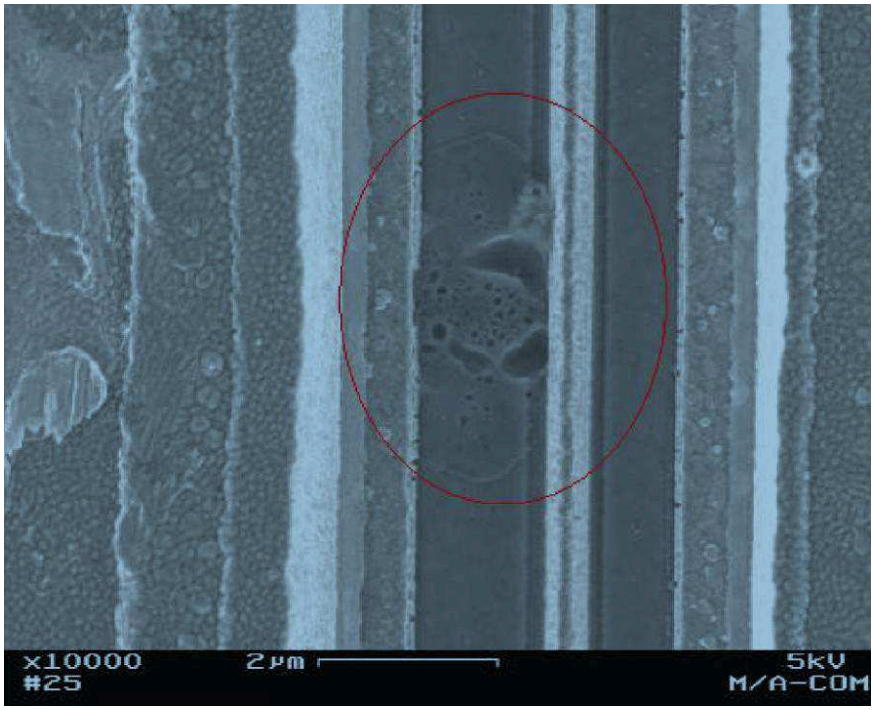


Figure 4.4: gate-source short circuit due to localized surface melting induced by ESD. [53]

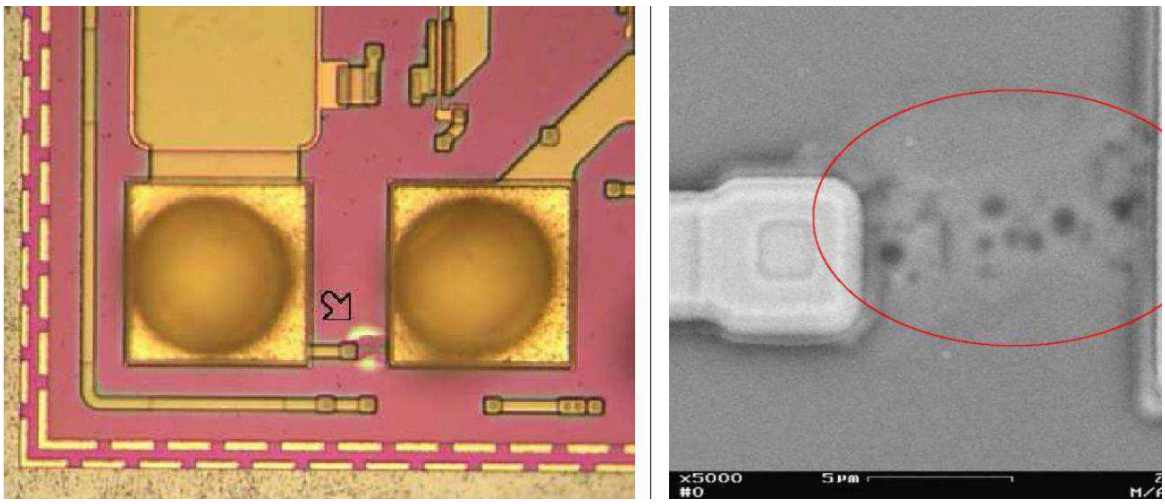


Figure 4.5: Surface damage between metal and contact due to ESD [53]

4.1.2 Methods to simulate ESD phenomena

HBM (Human Body Model)

The HBM (Human Body Model) test has been defined in the MILSTD 883x and widely studied in literature [51]. It is proposed to model a charged person approaching a device and transferring its charge to it. A schematic description of the situation is shown in Figure 4.6. The test structure is composed by a 1.5kΩ resistor and a 100pF capacitor (Figure 4.7a). When a

defined voltage is imposed, the capacitor is initially charged and then discharged, by means of a switch, to the device placed after the resistive load.

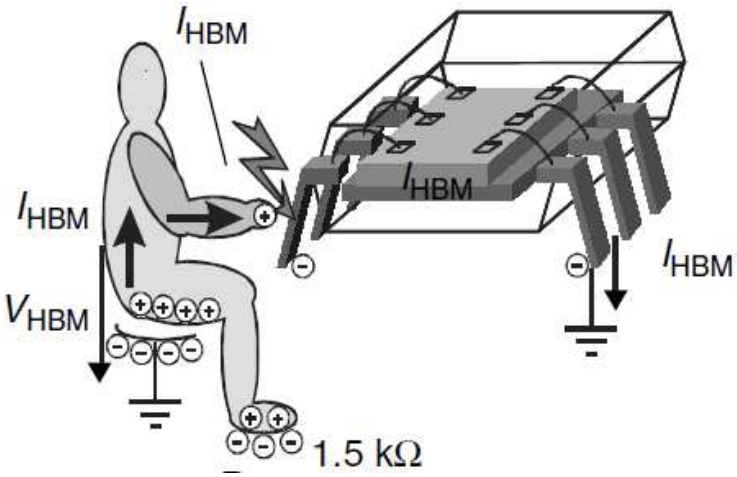
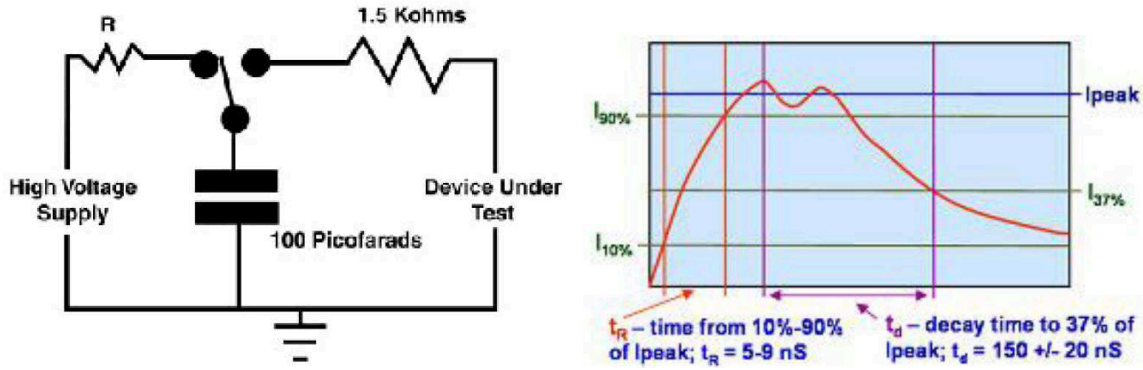


Figure 4.6: schematic of the human body model [51]



(a) (b)

Figure 4.7: (a) schematic test structure of a HBM model; (b) HBM corresponding current

In an ideal test the load inductance must be null. In a real test the parasitic inductance and the HBM resistance define the current rise time. According to definition provided by the standard the rise time (t_R)must be between 5ns and 9ns from 10% to 90% of the amplitude of the maximum current. Furthermore the time delay, which is the time required for the pulse to decay from 100% to 37% of the peak current must be 150±20 ns, as described in Figure 4.7b. The HBM pulse peak current at 400 V must be 0.27 +/- 10% A.

Main issues noticed in the HBM model are related to the presence of parasitic capacitances and resistances. An example is provided by Figure 4.8, where are studied the effects of the presence of parasitic capacitances due to, respectively, the parasitic stray capacitance of R_{HBM} and the interconnect and the parasitic capacitance of the test board, further parasitic issues can

be provided by the presence of DUT and a correspondent load resistance. In order to respect the rise and decay time provided by HBM standard it is important to accurately define a correspondent HBM inductance.

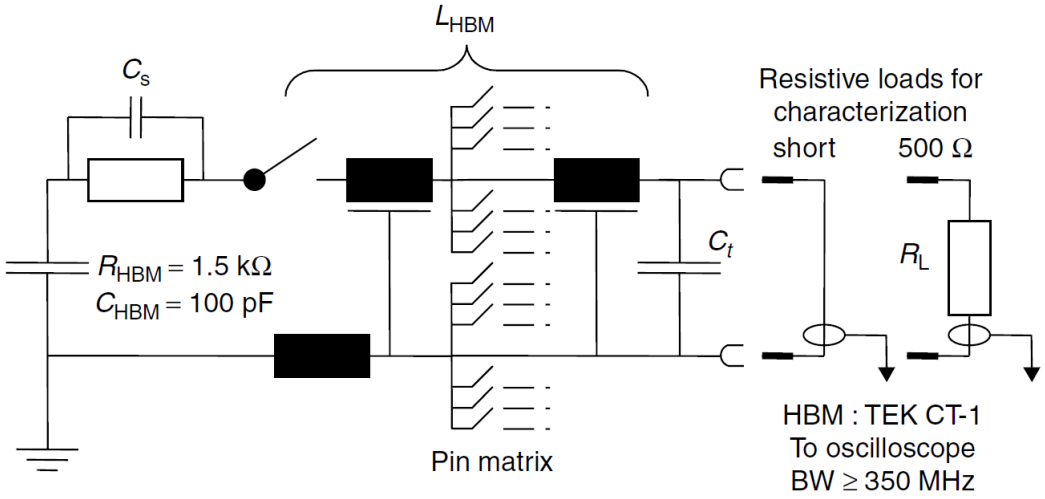


Figure 4.8: schematic of a HBM test structure with parasitic elements [51]

MM (Machine Model)

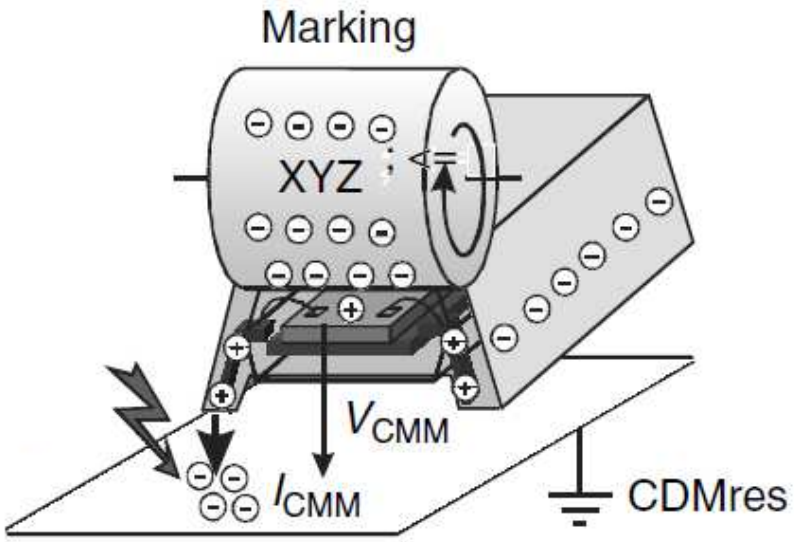


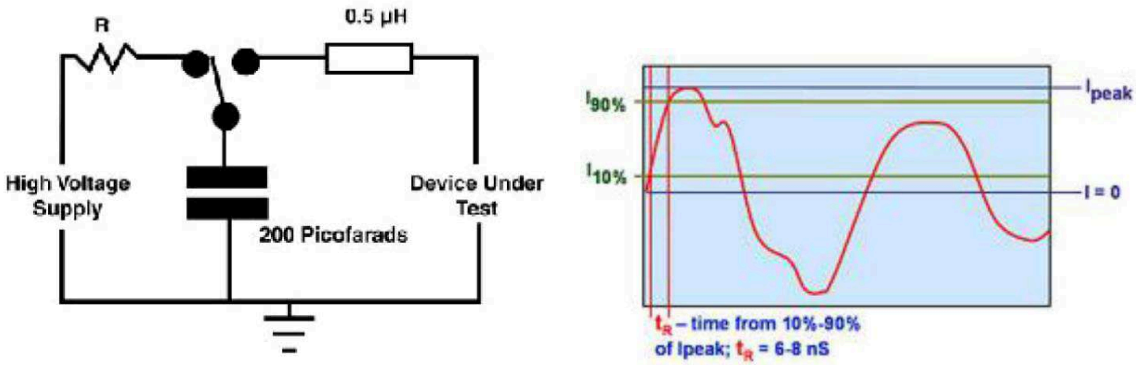
Figure 4.9: schematic of the machine model [51]

The MM (Machine Model) test has been developed in Japan in order to study a case similar to the HBM although more severe. It simulates an electrostatic discharge from a charged machine or tool. A schematic diagram to describe a situation is shown in Figure 4.9. The MM test circuit consists of a 200pF capacitor and a 500nH inductor (Figure 4.10a). The capacitor is charged at a defined voltage applied and then discharge through the inductor to the device. No

series resistance is used, even if in real test structures a parasitic resistance is reported. Thus, during the discharge, the dynamic impedance can be higher. MM shows similar failure mechanisms in the pn junction than the ones shown in HBM, although at lower pre-charge voltages.

During MM ESD testing, the MM test circuit must apply a sinusoidal signal (at 12 MHz), satisfying requirements imposed by standards and shown in Figure 4.10b. The rise time must be between 6 and 8 ns, while the MM peak current at 400 V must be 5.8 +/- 20% A. There is no correlation between HBM and MM thresholds. Depending on device tested the V_{MM} should be between 1/20 and 1/10 of the V_{HBM}.

Also in MM model a significant issue is provided by parasitic element, although with a stronger effect on discharge current than in HBM tests.



(a) (b)

Figure 4.10: (a) schematic test structure of a MM model; (b) MM current during test

TLP (Transmission Line Pulse)

Transmission line pulse has been widely used as a consequence of the possibility of simulating ESD phenomena with pulsed characterization. Indeed during the DC analysis the device can be affected by significant self-heating, thus leading to the conjunction of several different effects. A further advantage of TLP test is the availability of measuring several failure criteria, especially leakage current, before and after each measurement step.

The square pulse used to test the device is generated through the charge and discharge of the distributed capacitance of a transmission line (TL) [51]. Therefore the duration of the amplitude can be determined by using transmission lines with different properties (Figure 4.11). Pulse main properties also depends on the transmission line characteristics, such the impedance Z_0, according to its variation with material and geometry of the conductors and of the dielectric to isolate them.

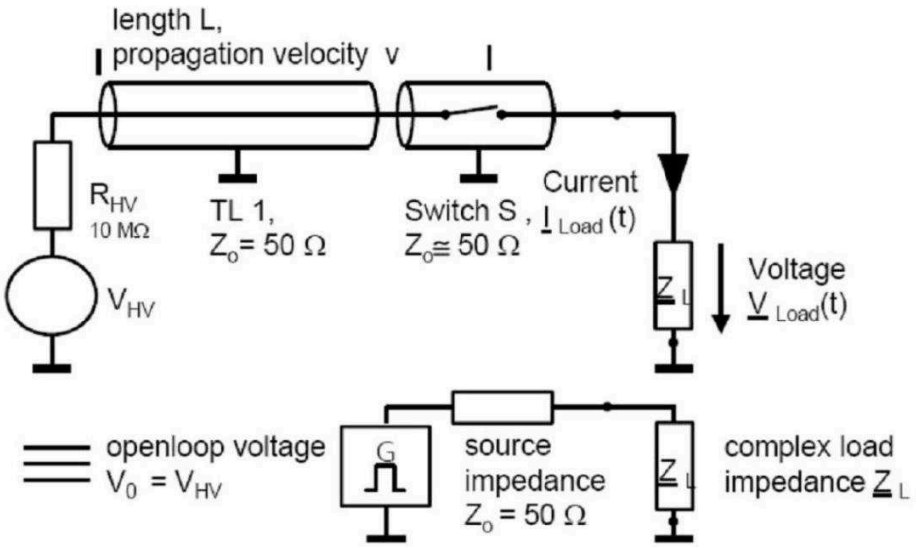


Figure 4.11: schematic of the TLP pulse generation circuit and the correspondent electrical model [51]

During the TLP testing the distributed capacitance of the transmission line is charged by a high voltage source through a high ohmic resistor. In this phase the coaxial switch is open. the square pulse is generated by the discharge of the transmission line into a resistive load or into a second transmission line. As a consequence the square pulse width can be calculated from the ratio between the length of the transmission line and the signal propagation velocity. According to calculations previously reported in literature [55] a 100ns wide pulse can be generated using a RG58 transmission line, characterized by a length of 10m, with a propagation velocity of 20cm/s. The amplitude of the pulse width is defined by the pre-charge voltage applied and by the source and load impedance as described in (4.1):

$$V_{pulse} = V_0 \cdot \frac{Z_L}{Z_L + Z_S} \qquad (4.1)$$

TLP method is characterized by two significant critical aspects: (i) relay switch properties; according to literature the most common solution to limit this issue is the use of a Reed relay surrounded by a metal sleeve or cylinder [51]. (ii) repeatability of the switching over full range, usually obtained through the establishment of a low series resistance by means of a metallic contact.

4.1.3 Design of ESD protection structures

The accurate design of an ESD protection structure is essential if MMIC devices operating at RF frequencies are considered. On one hand the main goal is to protect a MMIC structure through the design of a circuit implemented with the same technology used for the device in

order to improve the fabrication process. On the other hand it is important to employ a circuit which does not influence the device operation, especially when operating frequencies higher than 10 GHz are taken into account. Indeed a ESD protection circuit has to flow the most part of the current during an electrostatic discharge, thus avoiding the current flow in the RF circuitry, inducing no influence to the circuit during normal operation conditions. In order to flow the most part of the discharge current it is important to have a response time for the ESD circuit much lower than for the RF circuit and that, after the electrostatic discharge, normal operating conditions are reactivated after a short transient. According to the second requirement discussed above, the ESD protection circuit should not include any resistive elements, due to the consequent introduction of loss in the circuit. Furthermore the use of resistive components determine also the variation of further aspects such as introduction of noise, variation of matching condition in a RF device.

In order not to influence normal operating conditions a ESD structure should not introduce significant parasitic capacitances, especially in devices where the protection circuit is activated by the presence of switches, which mainly consist of diodes [52], [53]. As it will be discussed, in diodes protection structure the diode area significantly determines the ESD robustness; although a large area leads to a high ESD robustness, it enhances the impact of parasitic capacitances. If a RF structure is taken into account, it is of fundamental importance to remember that interconnection transmission lines added with the ESD circuit can lead to undesired effects such as parasitic capacitances generation, matching and reflection issues [54]. It is therefore essential to accurate design interconnections paying attention to corresponding length and dimension.

It is essential that the ESD circuit operates only during the discharge, especially when devices operating at the microwave frequencies for high power applications are considered. If, for instance, a switch has to flow the current to the GND terminal, the protection circuit can reflect the signal at the output of a different (previous) stage.

Diodes Protection Structure

In RF MMIC structures ESD protection circuits are often composed by Schottky diodes [52], [53]. The introduction of diodes in antiparallel configuration with the gate terminal does not influence RF performances but it leads to a significant protection to ESD phenomena. A solution commonly used consists of placing a bypass capacitor parallel to the gate source terminal, a series of diodes in anti-parallel configuration and one diode in parallel configuration. An example is shown in Figure 4.12. The number of diodes placed in anti-parallel configuration varies with the area and, thus, with the minimum ESD failure voltage required by standards and regulations.

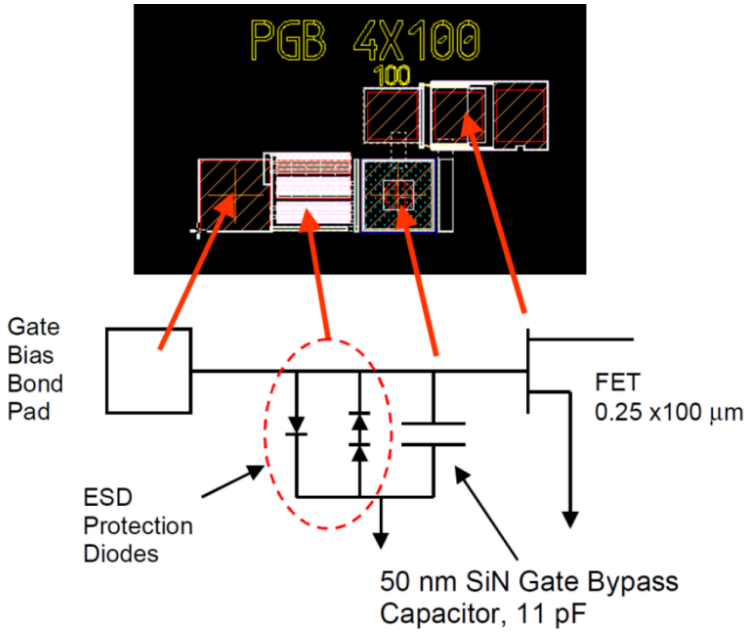


Figure 4.12: ESD diodes protection structure [52]

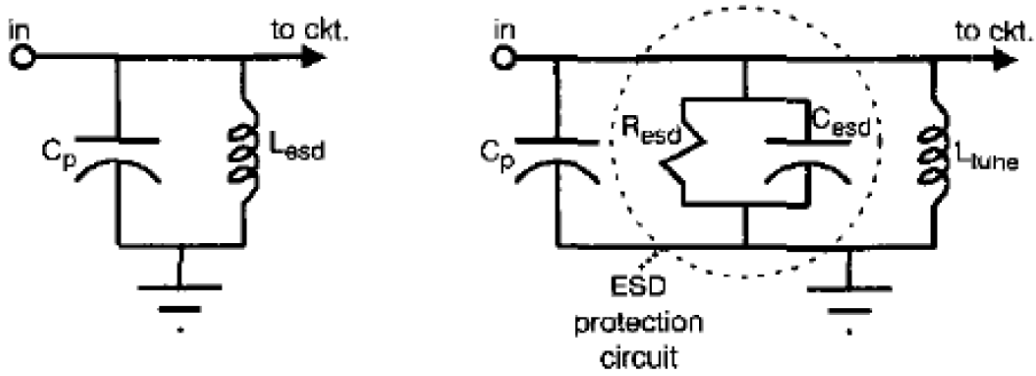
Schottky protection diodes define a direct path between a pad, which can receive a ESD, and GND. When a ESD occurs, since the voltage applied is higher than the diodes threshold voltage, diodes turn on and flow the current to the ground, thus avoiding the circuit degradation. Since diodes based on MESFET or Phemt structures are usually characterized by a low threshold voltage, typically of 0.6V, it is preferable to use a series of diodes in order they are turned on during the ESD phenomenon and not during normal operating conditions. Furthermore, in order to protect the device also from reverse breakdown diodes are usually placed in antiparallel configuration.

Experimental results discussed by Ersland et al. [53] demonstrate that HBM robustness varies with diodes dimension. According to [53] a breakdown voltage of 200V and 1200V has been measured for diodes gate periphery of 2x50µm and 2x400µm, respectively. Unfortunately, as a consequence of the influence of diodes dimension on parasitic capacitances, it is essential to define a diode dimension which leads both to a low parasitic capacitance and to a high ESD robustness.

Furthermore, according to the work proposed by Beall et al. [52], it is important to remember that FET devices are usually more sensitive to negative discharge, which, in the most part of the cases, represents the worst condition.

Resonant circuits

For high frequency applications it is possible to implement, at the RF pads, a ESD protection structure based on a resonant circuit [54]. This solution avoids the significant parasitic shunt capacitance, usually introduced by on-chip ESD protection structures, which affect RF performances at operating conditions. Furthermore it can be used also for high frequencies operation (i.e. higher than 2GHz), where the minimization of the high parasitic shunt capacitance is not possible. A circuit, shown in Figure 4.13a, was initially proposed by Leroux et al. [56]. The introduction of an inductance can compensate, at operating frequencies, the input parasitic capacitance and, during the electrostatic discharge, it can provide for a low impedance conductive path. However, although this approach determines a high HBM robustness, it does not offer a good solution when different ESD phenomenon, such as CDM (charged device model), occurs. A solution, proposed by Hyvonen et al. [54], is summarized in Figure 4.13b. This solution does not influence the normal operating conditions, as a consequence of the resonance established between inductor and capacitors and of the minimal influence provided by the resistance on RF performances. During the ESD event the structure can conduct high stress currents also under the high frequency which characterizes CDM stresses.



(a) (b)

Figure 4.13: LC resonator ESD protection circuit

4.2 Description of analysed devices

4.2.1 MMIC Power amplifier

The tested structure for ESD analysis is a MMIC power amplifier developed for high frequency applications such as point to point microwave systems. Further information about the structure have been given in chapter 3.2. The circuit diagram of the evaluated power amplifier is shown in Figure 4.14. It consists of four stages composed by a very reliable GaAs pHEMT MMIC foundry process. Each stage, except for the last one, is based on multi-finger pHEMT with a gate periphery of 0.9mm; in the last stage pHEMTs have a gate width of 0.96mm for a total dimension of 7.68mm.

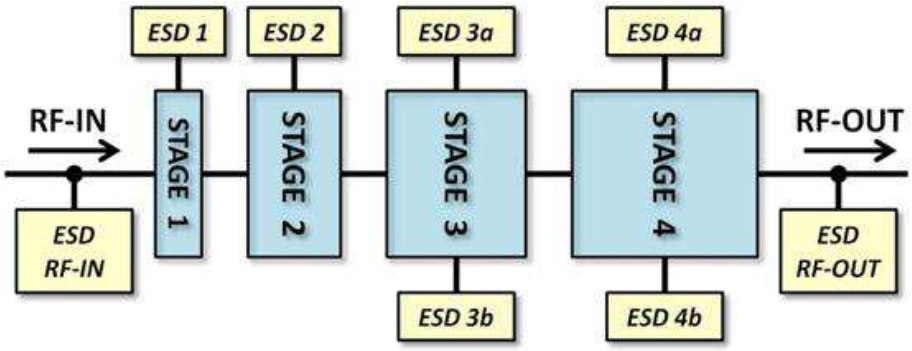


Figure 4.14: block diagram of the tested PA showing four stages and correspondent ESD protection structures.

Devices tested with the TLP were power amplifier on die, while devices tested with HBM and MM were packaged on a 5x5mm Quad Flat No Leads (QFN) package. The bonding diagram of the power amplifier into the QFN package is shown in Figure 4.15

Two typologies of ESD protection structures are noticed: (i) the RF input and output circuit and the drain terminals present a protection structure composed by ground path inductors and by pass capacitors in order to provide for a high ESD robustness without influencing the PA RF performances Figure 4.16a; (ii) all the gate terminals are protected through anti-parallel Schottky diodes. An example is shown in Figure 4.16b. The distribution of the currents between ESD protection circuit and the transistor gate terminal of the stage considered, in this case the first one, is shown in Figure 4.17.

The power amplifier design contains also a power detector compensated in temperature, able to give more than 30 dB of dynamic range. The correspondent circuit is characterized by a DET and REF (voltage reference) pad which can be influenced by ESD effects.

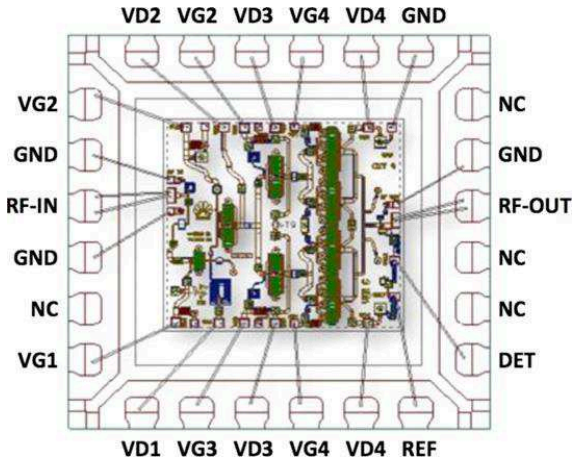


Figure 4.15: Bonding diagram of the tested PA into the 5 x 5 mm QFN package

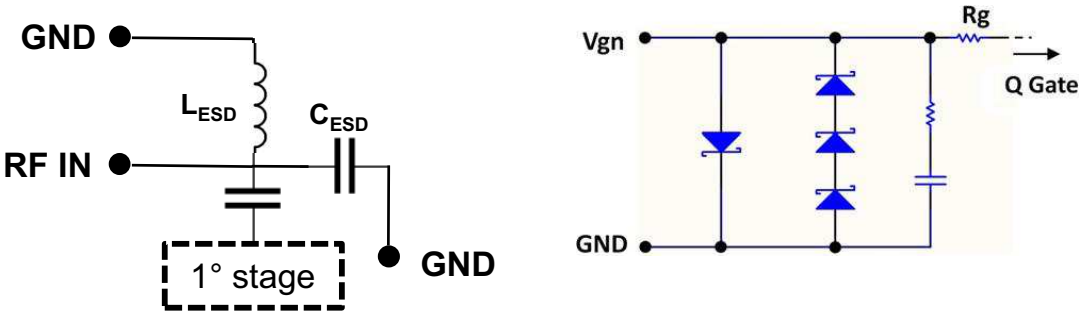


Figure 4.16: ESD protection circuit

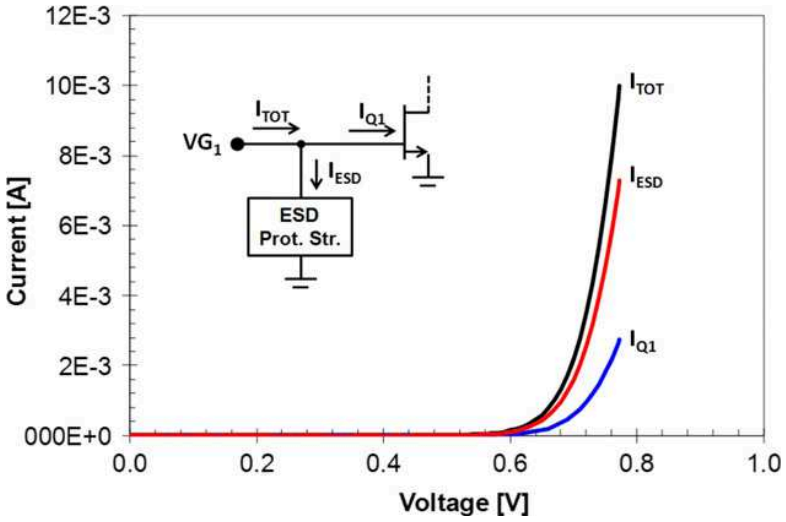


Figure 4.17: Distribution of the currents between the Gate ESD protection structure and the transistor Gate in the first stage

4.3 ESD analysis on a MMIC power amplifier

This chapter deals with the characterization of the ESD sensitivity of a MMIC power amplifier. RF input and output pads, gate terminals and drain terminals have been tested. Furthermore the sensitivity of the power detector has been measured. Three tests typologies have been carried out: (i) TLP test, (ii) standard HBM up to 2kV, (iii) standard MM up to 200V.

Analysis of power amplifiers ESD robustness states that: (i) no failure is shown in the RF pads vs GND up to an HBM with pre charging voltage of 2kV; failure of inductors between RF pad and GND has been measured with TLP analysis and confirmed by SEM analysis. (ii) the anti- parallel diodes to protect the gate terminal show a degradation after an HBM stress lower than 2kV, demonstrating consistent results in the TLP and MM analysis. The power detector reveals to be the most sensitive pad, showing a much lower HBM stress degradation voltage and demonstrating consistent results both with MM and TLP analysis.

4.3.1 Experimental details

Devices have been tested with three different models: (i) TLP, (ii) HBM, (iii) MM. Before TLP analysis a preliminary HBM-like test up to 4kV has been carried out. The test has been carried out with an Oryx Celestron-I HBM-like machine, placing the package in dead-bug position and contacting the pads with needles. Leakage and transconductance DC analysis was carried out after each step in order to monitor device condition and define an eventual degradation. Since results were consistent with the one reported in the HBM and MM tests, it has been decided not to provide for detailed results.

TLP was carried out with a custom setup previously described in [51], [55] which employs the principle of operation described in chapter 4.1.2. The TLP is a TDR-TLP (Time Domain Reflectometer Transmisson Line Pulse) characterized by a 100ns pulse width and a 1ns pulse rise time. Devices have been stressed both with positive and negative bias up to snapback identification at wafer level. After each stress device degradation was evaluated by means of a parameter analyser.

HBM and MM test have been carried out with industrial ESD qualification machine Oryx 11000-EX. HBM and MM stresses were carried out up to ±2 kV and ±200 V respectively, with a pre-charge voltage step of 250 and 25 V, respectively. At each step, for the same pre-charge voltage applied, stress with both a positive and a negative bias is applied. In order to identify a

possible failure of the device leakage current has been measured before and after each ESD stress (with 100mV applied). HBM and MM threshold voltage is defined as the stress voltage where a leakage current of 1µA is reached. After the stress, in order to further investigate device degradation characteristics, DC measurements have been carried out sweeping the drain voltage between ±100mV and keeping the transistor in off conditions in order not to cause a further degradation in the device.

4.3.2 Experimental results with TLP analysis

RF IN connections

The power amplifier is characterized by RF input and output terminals with a nominal operating frequency is in the Ku-band between 12.7GHz and 15.4GHz. These terminals are connected to the gate of transistor belonging to the first stage and the drain terminal of the transistors belonging to the last stage through bypass capacitors.

A 100ns TLP with 1ns rise time has been applied in order to test both the terminals. The test of the RF-IN vs GND circuit with a positive bias applied is shown in Figure 4.18. Stressed pin shows a linear trend up to 3A; a saturated I-V curve is then reported up to the failure point reached at about 7A with a correspondent voltage of 75V. An explanation to the curve trend is given both by the presence of inductors in the ESD protection structure, with an impedance value of 3.5Ω, which lead to a ohmic trend for lower current values and by the behaviour of metal lines under high current, which leads to the curve saturation.

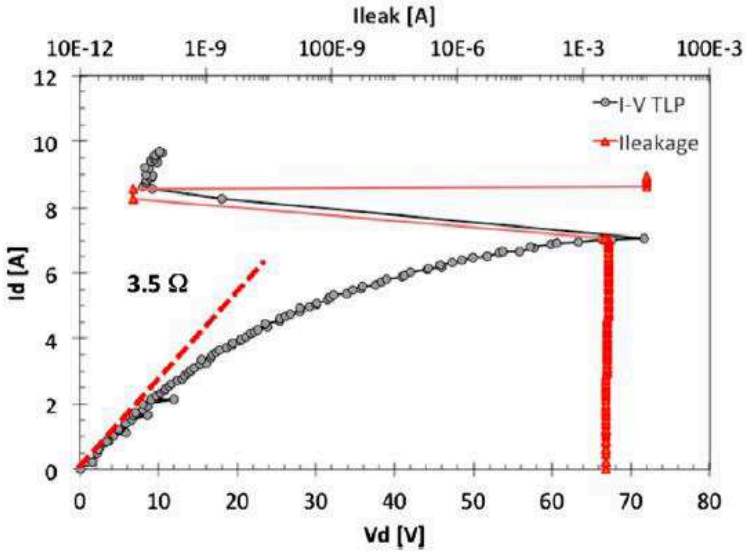
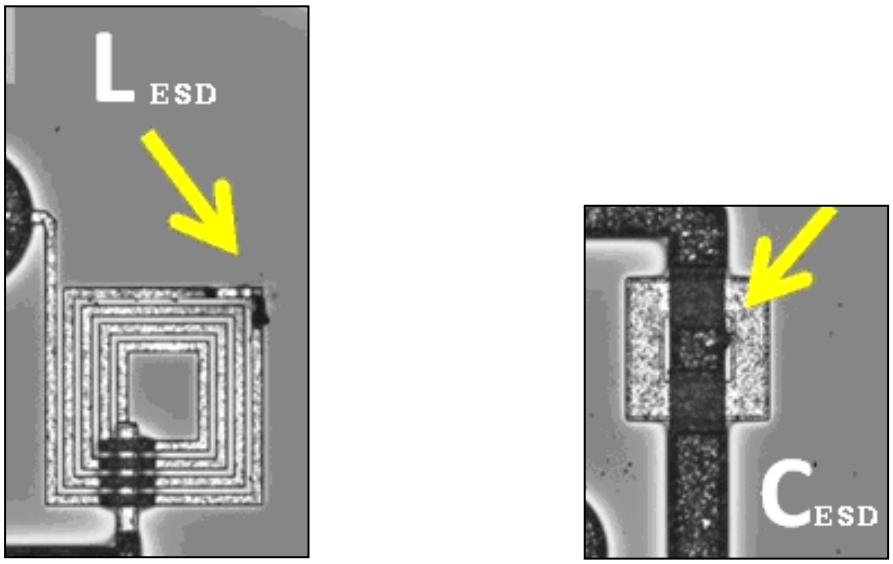


Figure 4.18: I–V TLP behaviour between RF-IN and GNDwith a positive bias applied (chip 1)

Optical inspection carried out after the TLP stress confirm that failure is due to an open circuit of the grounding inductor (Figure 4.19a). As it is possible to notice in Figure 4.19a the inductor is characterized by several burns consequent to the passage of a high current. Failure is further confirmed by the breakdown of the capacitor (Figure 4.19b) which leads to a lower impedance state as a consequence of the short circuit revealed after the failure point. A similar behaviour has been reported when a positive bias is applied during TLP test in a different device with similar characteristics (Figure 4.20, Figure 4.22)



(a) (b)

Figure 4.19: damages induced to LESD (open circuit) and CESD (short circuit) after TLP stress with positive bias at the RF INPUT (chip 1)

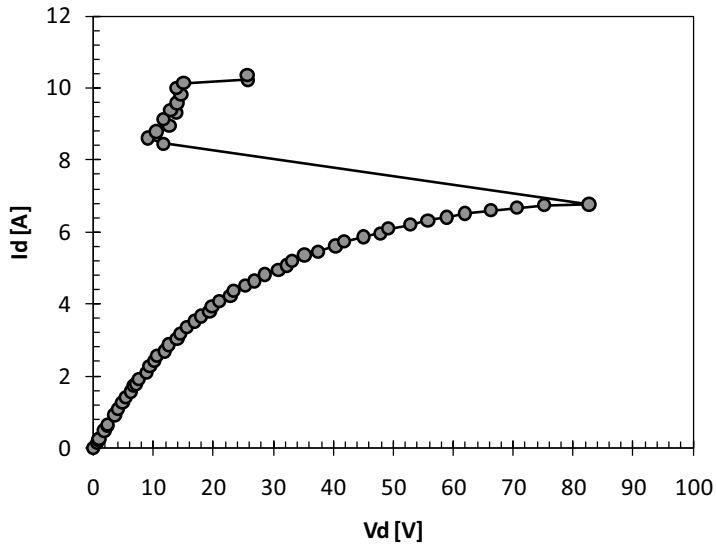


Figure 4.20: : I–V TLP behaviour between RF-IN and GNDwith a positive bias applied (chip 2)

The HBM like testing (carried out contacting the device in dead bug position with needles) showed no significant variation up to ±4 kV. This is confirmed by the electrical characteristics of the first stage of the PA where sub threshold current curves are overlapped (Figure 4.21)

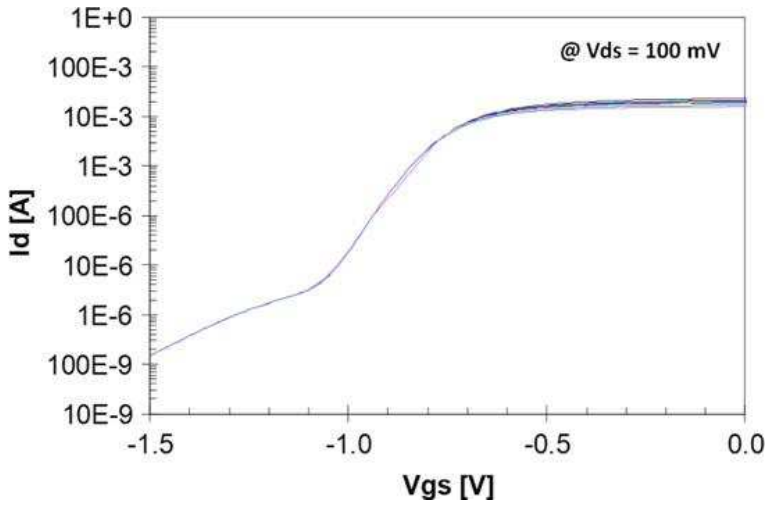
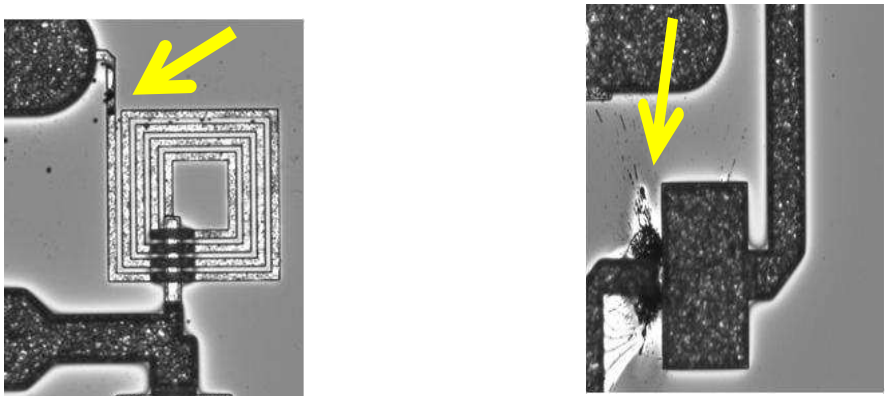


Figure 4.21: Id vs. Vgs curves of Q1 after ±4 kV HBM-like stresses applied to RF-IN vs.GND(VDS = 100 mV)



(a) (b)

Figure 4.22: damages induced to L_{ESD} (open circuit) and C_{ESD} (short circuit) after TLP stress with positive bias at the RF INPUT (chip 2)

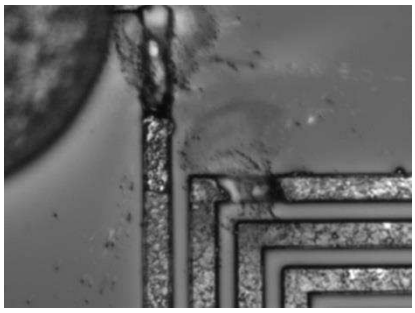


Figure 4.23:damages induced to LESD (open circuit) after TLP stress with negative bias at the RF INPUT

Concerning the negative TLP stress between GND and RF-IN, very similar results have been obtained. Indeed, as expected, also in this case the inductor L1 drained the ESD current to GND, up to a failure current level of 9 A (Figure 4.24). As it is possible to see from the evolution of leakage current (in red), the failure of the inductor (Figure 4.23) lead to an open-circuit condition. The short-circuit behaviour was then due to the damage of the capacitors vs. GND, as previously shown concerning the positive TLP stress.

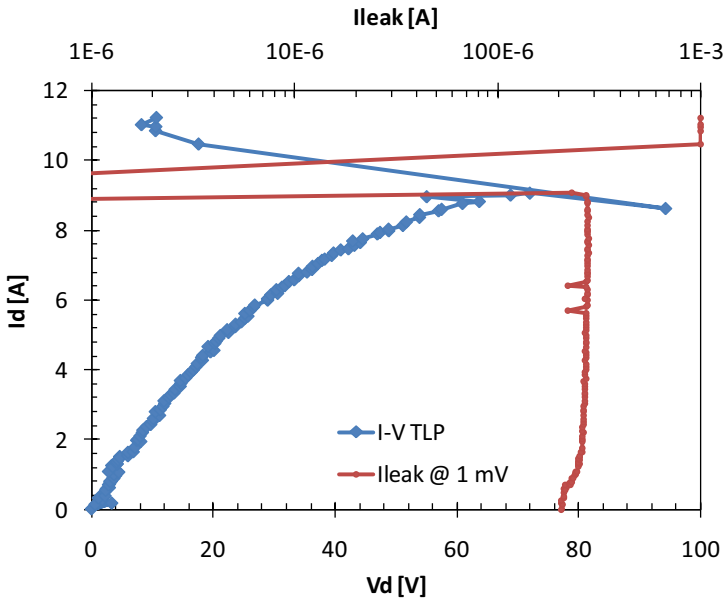


Figure 4.24: I–V TLP behaviour between RF-IN and GNDwith a negative bias applied

RF OUT connections

The ESD robustness of the RF OUT pin vs GND evaluated by means of TLP analysis is shown in Figure 4.25. A failure mechanism similar to the one discussed for RF IN pin is reported: the discharge flows through the two series inductors placed between the RF OUT and the GND pad.

In our case the series inductance has a correspondent impedance value of 2.0Ω. Similarly to RF IN pin behaviour the TLP I-V curve shows a linear behaviour up to about 4.5A leading to a slow saturation up to the failure point. When a current of 6.5A is reached at a voltage of 30V failure occurs, reporting an open circuit at the series inductors (Figure 4.26).

Consistently with TLP results and correlation between TLP and HBM tests, the HBM like testing (carried out contacting the device in dead bug position with needles) showed no significant variation up to ±4 kV. This is confirmed by the electrical characteristics of the last stage of the PA where sub threshold current curves are overlapped (Figure 4.27).

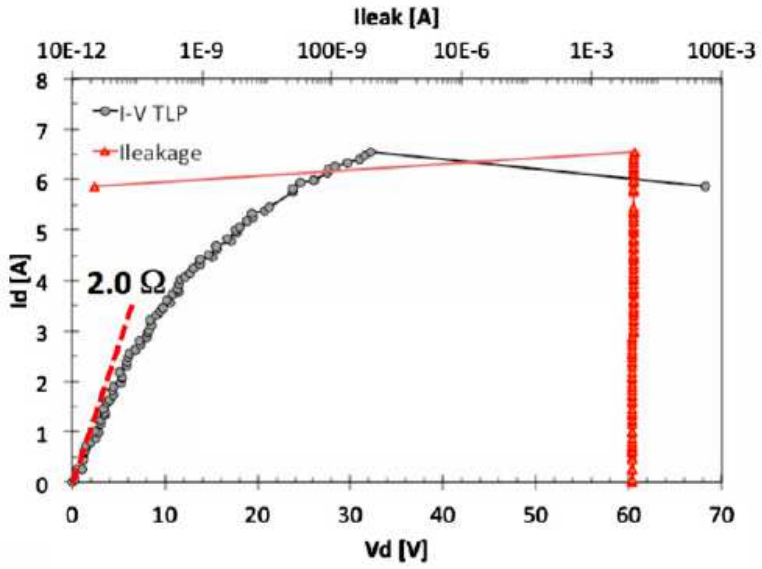


Figure 4.25: I–V TLP behaviour between RF-OUT and GNDwith a positive bias applied

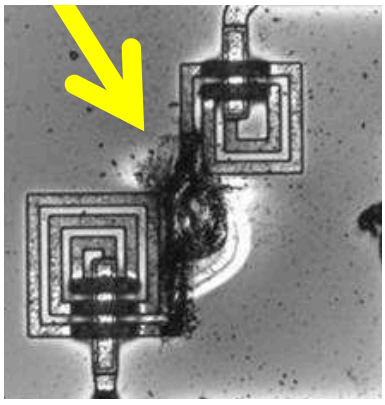


Figure 4.26: damages induced to LESD (open circuit) after TLP stress with positive bias at the RF OUTPUT

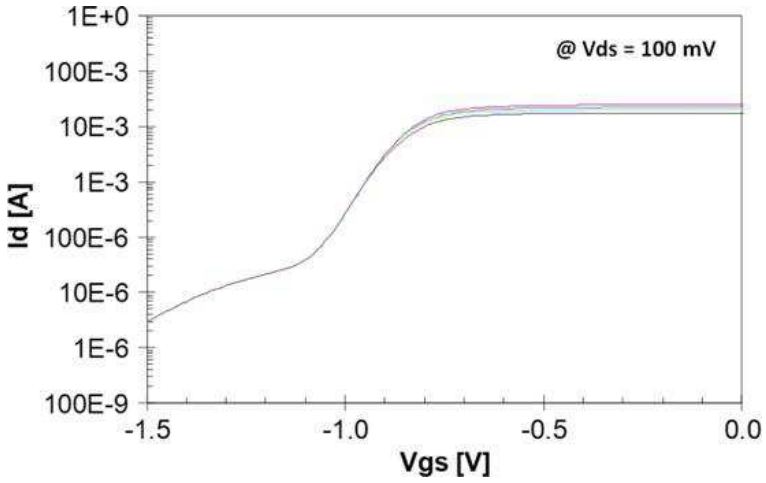


Figure 4.27: Id vs. Vgs curves of Q1 after ±4 kV HBM-like stresses applied to RF-IN vs. GND(VDS = 100 mV)

The hypothesis that the series inductances at the output mainly drains the ESD current is partially supported by the measurement of the coupled voltage during 100 ns TLP pulses after the capacitor placed in series between the RF out pad and the transistors of the fourth stage. The maximum value of the coupled signal measured in correspondence of the transistors of the last stage is 20 times lower than the voltage applied to the RF pad, thus demonstrating the impossibility of causing damages to the PA output stage when a high voltage is applied.

Consistent results have been noticed when a negative TLP stress is applied between RF OUT and GND. Also in this case the inductor drained the ESD current to GND, up to a failure current level of about 8.5A (Figure 4.28). The failure of the central part of the series inductors is shown in Figure 4.29.

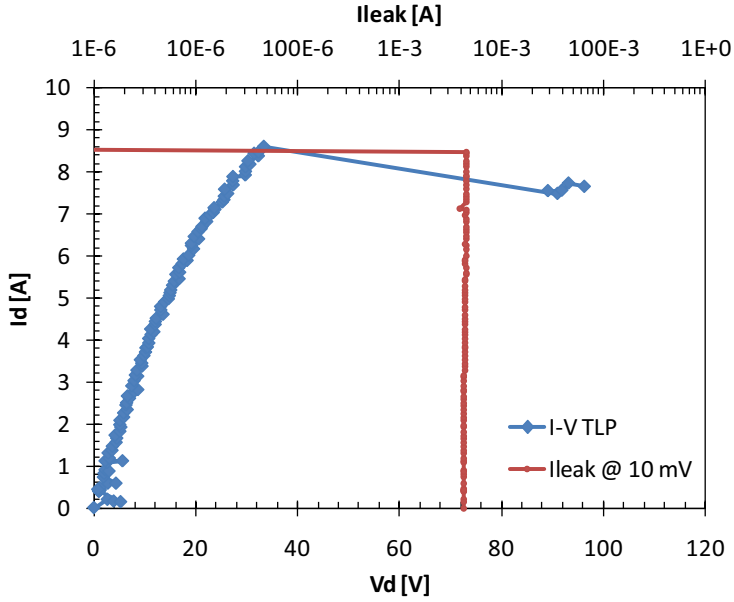


Figure 4.28: : I–V TLP behaviour between RF-OUT and GNDwith a negative bias applied

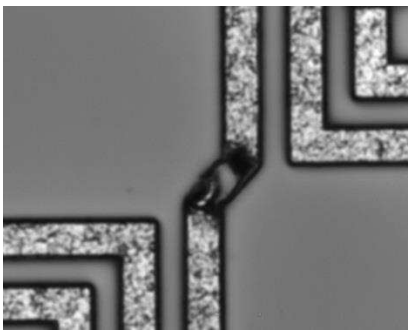


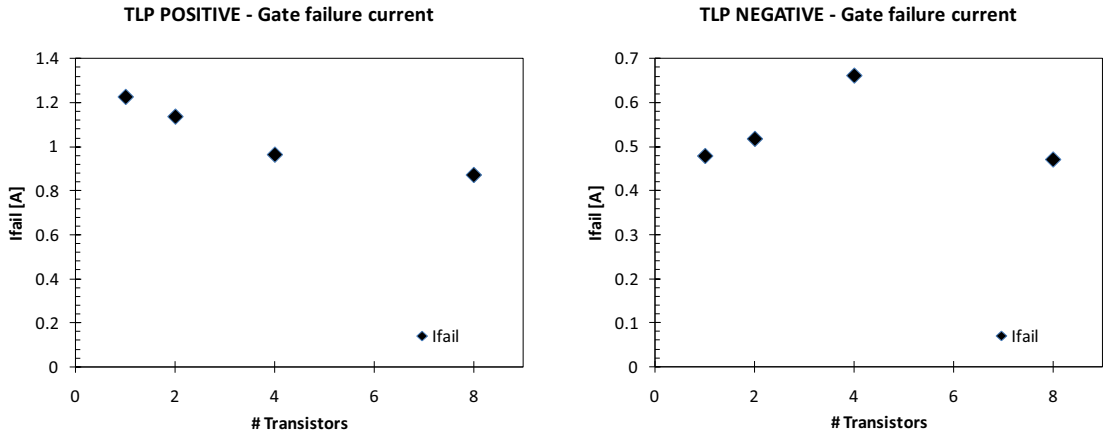
Figure 4.29: failure in the RF-OUT inductance after TLP test

GATE pads

The ESD robustness of gate pads has been studied by pulsing the V_G vs GND circuit with 100ns TLP pulses. After each pulse the device is monitored through the leakage current measurement at 500mV and -100mV, respectively. As explained in the device description the gate pads ESD protection structure is composed by anti- parallel Schottky diodes and bypass capacitors to GND.

Measurements state that, under positive TLP stress, the gate robustness decreases as a function of stage dimension, from a value of 1.2A in the first stage (composed by one pHEMT with gate width of 0.9mm) to a value of 0.9A in the last stage (composed by eight pHEMTs each one with gate periphery of 0.96mm). Results are shown in Figure 4.30. Consistent results have been measured with HBM and MM analysis and will be further explained.

A not monotonic trend is noticed in the gate failure current measured after a negative TLP stress has been applied. From the comparison between negative and positive TLP stress we can demonstrate that devices are much more sensitive during negative than positive pulses.



(a) (b)

Figure 4.30: gate failure current as a function of number of transistor when (a) positive and (b) negative TLP pulses are applied

Figure 4.31 and Figure 4.32 show the behaviour of the gate of the transistor of the first stage of the power amplifier. I-V curves have been measured with a positive and negative TLP pulse applied, respectively. Failure is reached at a value of 1.2A and less than 0.5A with the positive and negative bias applied at a voltage of, respectively, about 5 and 12V.

From the analysis of the distribution of gate current between the ESD protection circuit and the transistor of the first stage (Figure 4.17) it is possible to measure that the 70% of the current flowing to the gate terminal flows into the diode protection structure, while the remaining 30% in the transistor of the first stage.

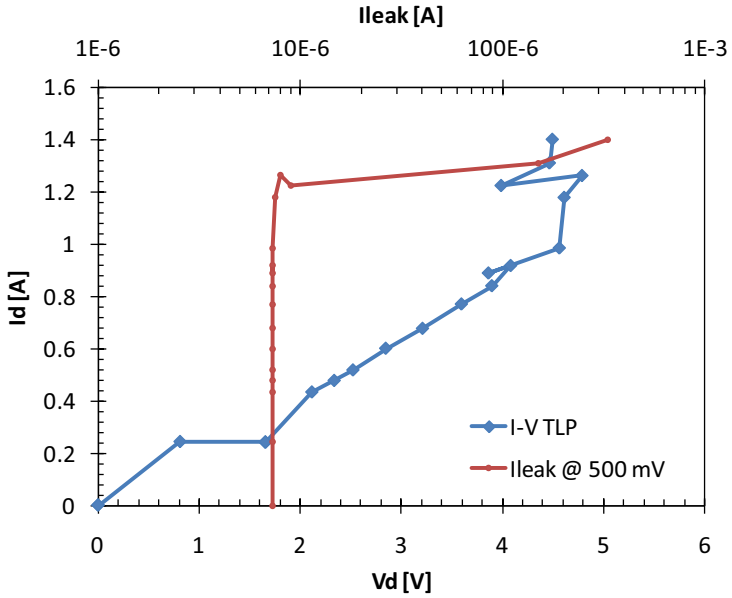


Figure 4.31: I–V TLP behaviour between VG1 and GND with a positive bias applied

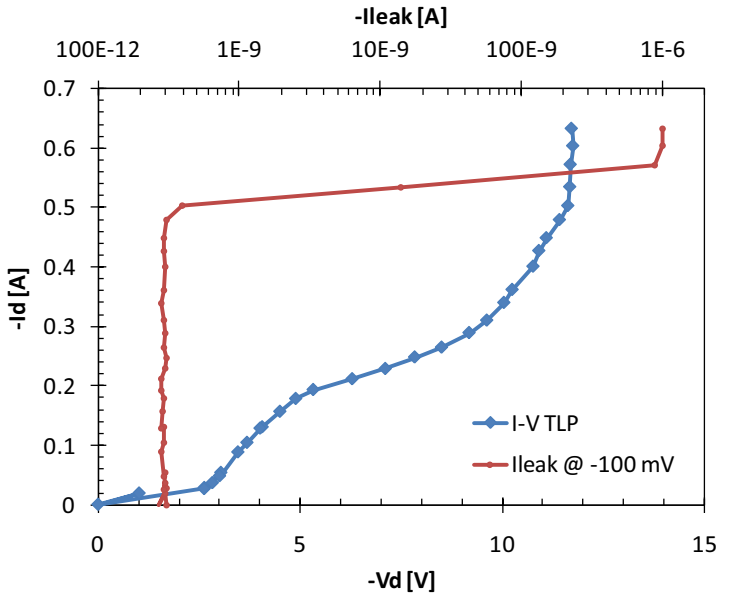


Figure 4.32: I–V TLP behaviour between VG1 and GND with a negative bias applied

We can therefore state that the failure of the gates connections is mainly due to the hard breakdown of the diodes used as ESD protection structure. The melting of the diodes fingers and their shortening is clearly visible in the SEM picture (Figure 4.33)

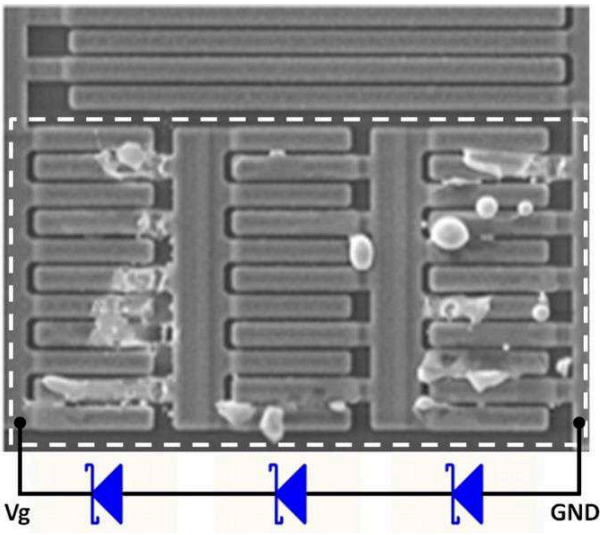


Figure 4.33: SEM picture of the damages induced by the negative TLP stress to thethree series Schottky diodes adopted to protect Gates connections

DRAIN pads

The ESD robustness of the Drain connections was tested applying positive and negative 100 ns TLP pulses to the drain pad vs. GND. All the drain pads have been evaluated.

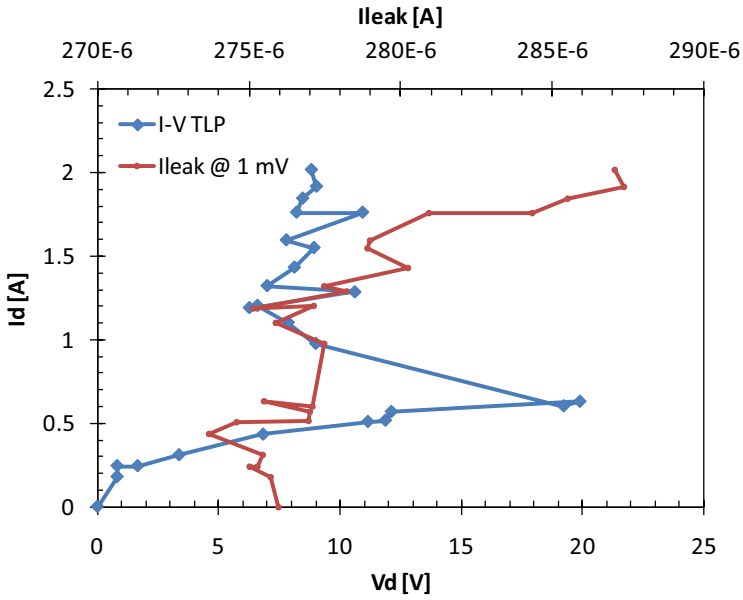


Figure 4.34: : I–V TLP behaviour between VD1 and GND with a positive bias applied

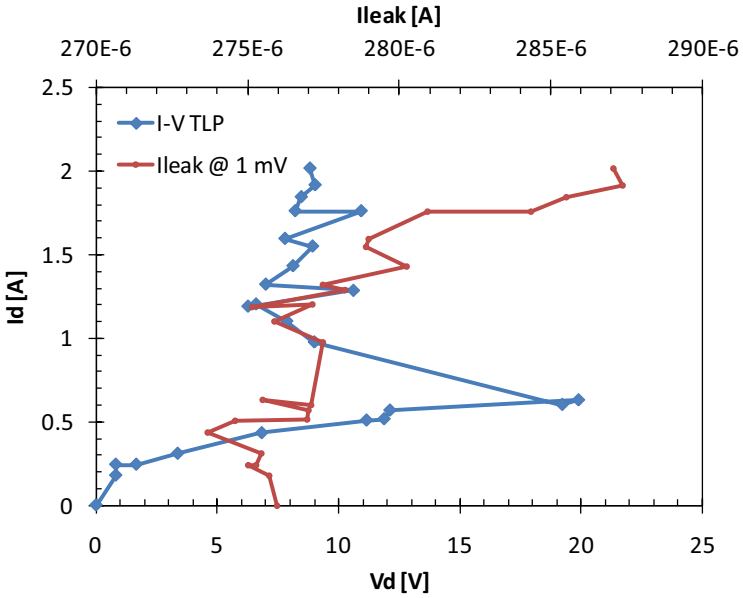


Figure 4.35: : I–V TLP behaviour between VD1 and GND with a negative bias applied

The ESD robustness of the Drain connections was tested applying positive and negative 100 ns TLP pulses to the drain pad vs. GND (the sensitivity to negative pulses was tested applying the pulses between GND and the respective pad). All the drain pads have been evaluated. The leakage current is measured at 1 mV. Differently to the Gate analysis previously shown, the leakage current did not offer a good indication of the device life state. An example has been reported in Figure 4.34 and Figure 4.35 for the first stage. Similar results have been shown in the further three stages.

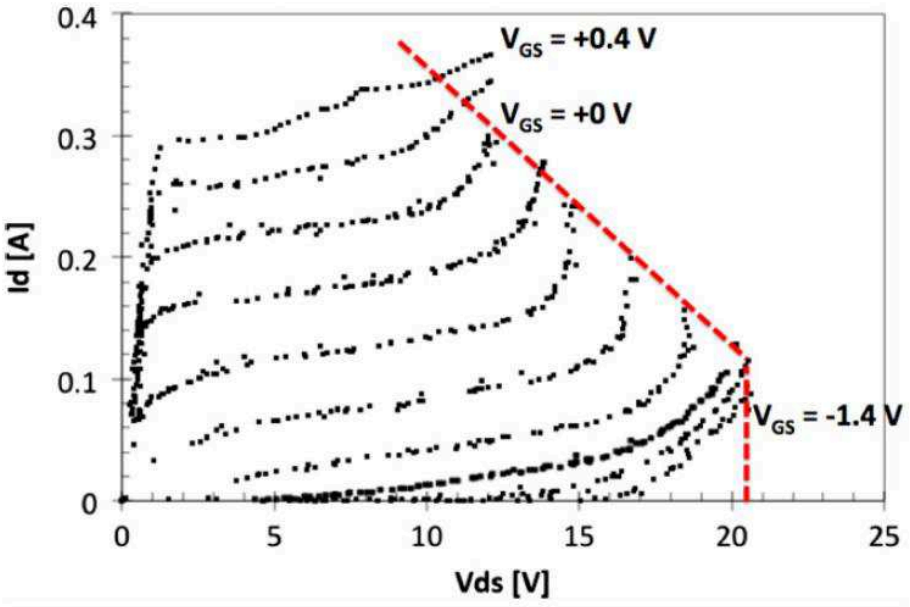


Figure 4.36: Safe operating area measured on a Phemt with TLP pulses for several VGS.

The S-like behaviour reported in Figure 4.36 has been previously studied in literature, both in GaAs HEMT and MESFET technology. Previous works reported in literature suggest that in a short channel transistor holes generated by impact ionization accumulate in the substrate and channel region between gate and source, leading to the generation of a parasitic bipolar transistor which enhances the injection of electrons from the source and the number of primary electrons flowing into the high electric field.

The S-shape is thus due to a conjunction of different phenomena: in pinch-off region breakdown phenomena cannot be described only by impact ionization but also by thermionic field emission. As a consequence, because of thermionic field-emission, electrons are injected from the gate to the drain-gate region of the insulator, which is characterized by a higher field. Furthermore, because of the higher insulator field the electrons enter the channel hot and, influenced by impact ionization, they flow through the drain. The current in off-state conditions has a low value and, lowest is the value, the highest must be the multiplication effects, which increase proportionally with drain source voltage and gate drain electric field.

In on-state conditions the breakdown is mainly determined by carrier multiplication due to channel electrons. Since the device is turned on, higher is V_{GS}, higher is the carrier multiplication; as a matter of fact the increase of drain current is determined at lower drain source voltage. Furthermore, as a consequence of impact ionization, at higher V_{GS} and with an higher electric field imposed a bigger number of holes can be extracted from the gate, leading to a higher gate current.

In ON state condition breakdown is also due to impact ionization, where holes generated can form the base of a parasitic bipolar transistor (PBT). The breakdown is due to the concomitance of the HEMT and the PBT behaviour, which causes, at high V_{DS} values, a positive feedback between the hole-electron pair which are generated and the increase of the number of primary electrons. As a consequence the breakdown voltage assumes a lower value.

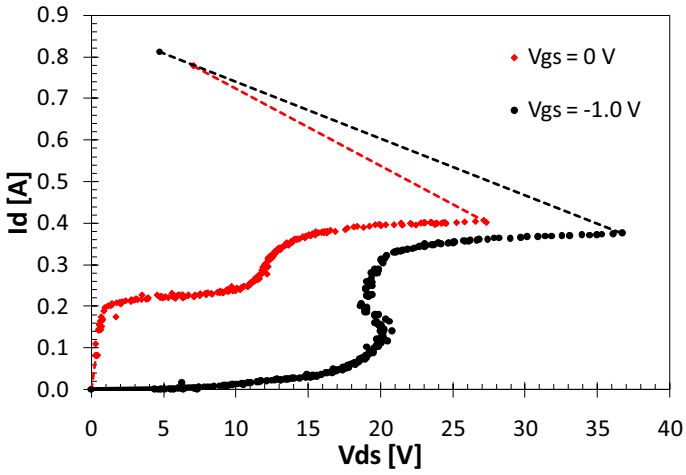


Figure 4.37: Breakdown measured on a Phemt with TLP pulses for several VGS.

To further investigate this phenomenon a detailed analysis has been carried out on a pHEMT developed with similar technology and characterized by a gate periphery of 0.6mm under both high dissipation (i.e. V_{GS}=0.2V) and closed channel condition (i.e. V_{GS}=-1V), confirming the S-shape trend (Figure 4.36). Moreover two devices have been stressed up to failure point (Figure 4.37) reached respectively at (27.1 V; 0.4 A) for V_{GS} = 0 V, and at (37.6 V; 0.37 A) for V_{GS} = -1.0 V.

Auxiliary Circuitry connections

The tested power amplifier is characterized by two simple circuits with the function of power detector: (i) a power detection circuit (DET pin) and a reference voltage (REF pin). In order to provide for a detailed analysis also the ESD robustness of the power detector was studied with positive and negative 100ns TLP pulses. These pads reveal to be the most sensitive in the power amplifier, demonstrating a TLP failure current between 0.1 and 0.15A in the worst case. In Figure 4.38 and Figure 4.39 the TLP positive and negative pulse applied between the DET and GND pad is shown. Due to the similarity of results measured in DET vs GND and REF vs GND pin only the first ones are reported. Consistently with analysis carried out on gate and RF pads the negative pulse induce an earlier failure, showing a failure at 0.1A and 0.3A when a negative and a positive pulses are applied, respectively.

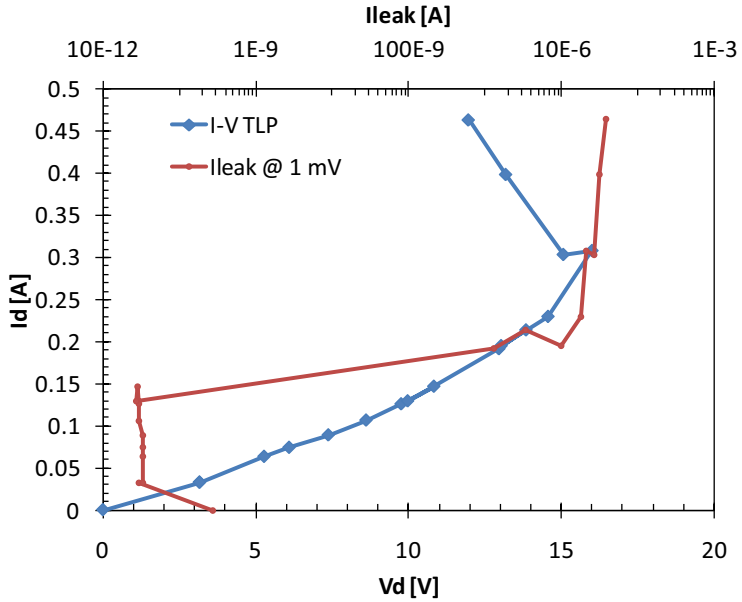


Figure 4.38: I–V TLP behaviour between DET and GND with a positive bias applied

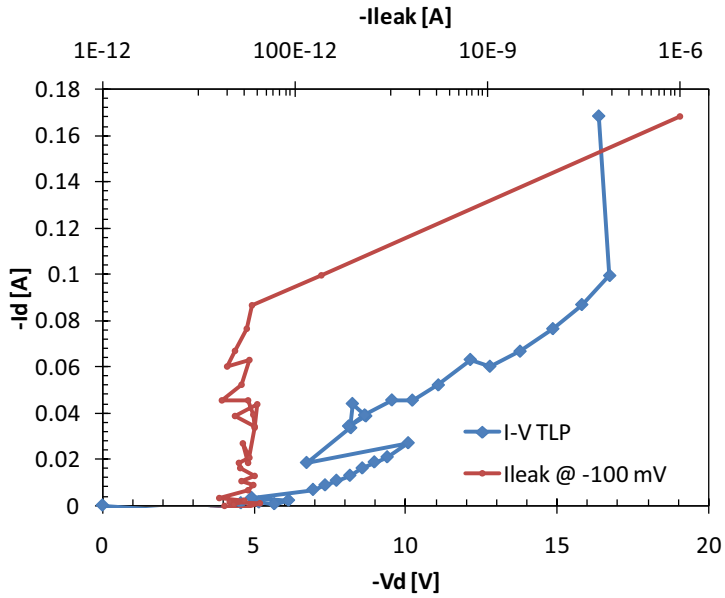
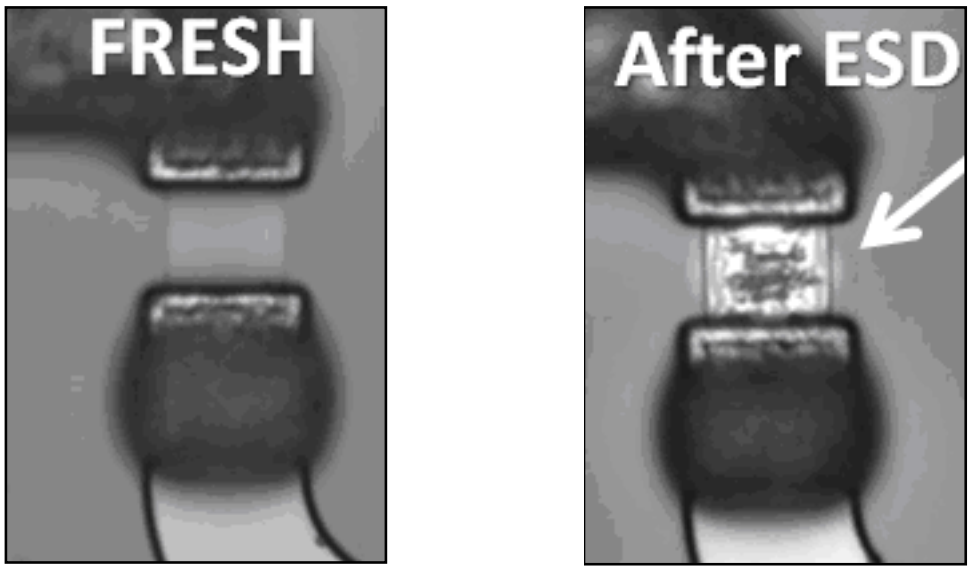


Figure 4.39: I–V TLP behaviour between DET and GND with a negative bias applied

The optical analysis revealed that, in both the cases, failure is due to the sudden breakdown of the integrated resistors. A comparison of resistors belonging to the DET circuit before and after the TLP analysis is reported Figure 4.40. Although improvements have be done by changing the resistance dimension, no significant variation in the ESD robustness has been noticed.



(a) (b)

Figure 4.40: resistance of the DET vs GND circuit (a) before and (b) after ESD stress

4.3.3 Robustness confirmation by means of HBM and MM tests

In order to further study the ESD robustness, analysis has been extended by studying ESD effects on power amplifiers by means of HBM and MM tests. All the pads have been tested , demonstrating consistent results with previous analysis carried out with TLP measurements. For the analysis of all the gate pads and detection circuit the relationship between TLP and HBM previously reported in literature, i.e. 1 A TLP ≈ 1.5 kV HBM.

At each step the device has been stressed with positive and negative bias. Furthermore, in order to monitor the device degradation after each step the pad leakage current has been measured at V=10mV. The failure point is defined as the voltage correspondent to a leakage current of 1μA in the gate pads and of 50μA in the detection circuit.

HBM test

Consistently with TLP analysis all the drain pads show no failure up to 2kV during HBM test. No significant variation is shown in leakage current monitored during the stress. Similar considerations can be done for the RF IN and the RF OUT circuit. On the basis of the failure point measured during TLP analysis HBM RF in and RF OUT should show a HBM robustness between 9.5kV and 10.5kV, much higher than the highest value imposed during HBM or HBM like stress.

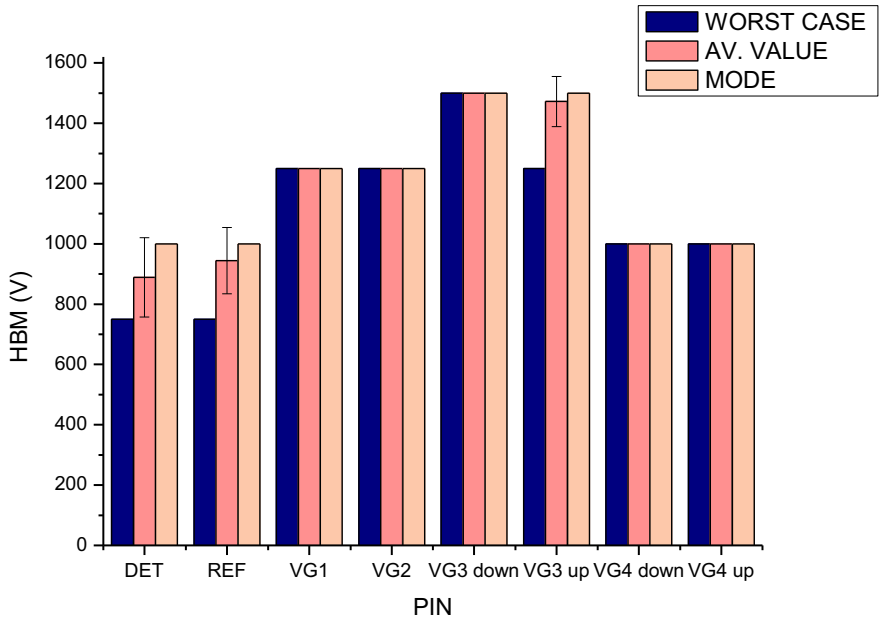
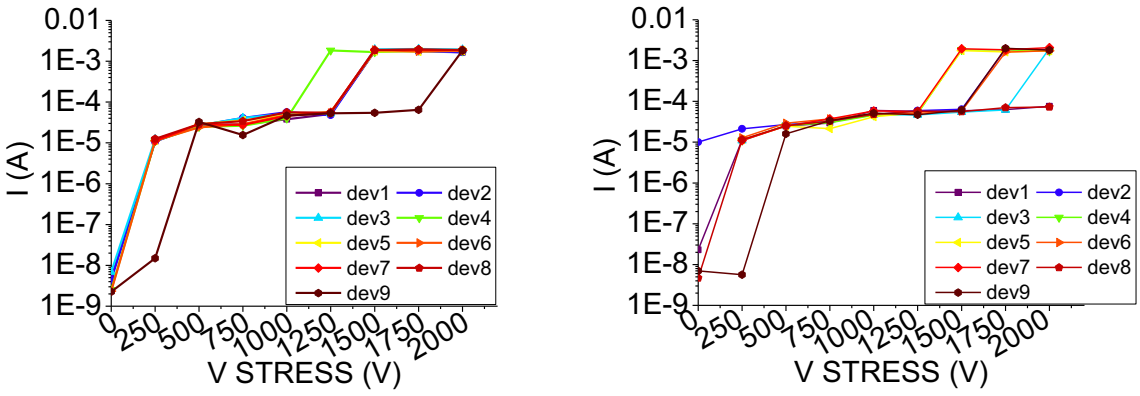


Figure 4.41: HBM robustness in gate pads and detection circuit evaluated as average value, mode and worst case

On the contrary all the V_G vs GND pads and pads corresponding to the detection circuit report a HBM robustness lower than 2kV. Several devices have been tested. Figure 4.41 reports the HBM robustness considered as the worst case measured, the average value and the mode. A HBM robustness between 1kV and 1.5kV is reported in all the V_G pads. Except for the V_G pad measured in the upper part of the third stage in one device, a significant reproducibility has been noticed in all the devices tested with a standard deviation lower than the step used (250V)

The V_G pads analysis carried out with negative TLP pulses demonstrates the first and the second stage report a similar robustness (about 0.5A). A higher robustness is shown in in the third stage (0.65A), while a TLP value of 0.45A is noticed in the fourth stage. The HBM robustness, evaluated as a function of number of transistors, has a similar trend than the TLP analysis. In both the first and the second stage an average HBM robustness of 1.25kV is noticed. In the third stage a higher robustness (1.5kV) is measured. In the last stage leakage current reaches a value of 1µA after a HBM voltage of 1kV is imposed. The relationship between TLP and HBM analysis is similar to the one reported in literature.

Consistently with TLP analysis the most sensitive pads are the DET vs GND and REF vs GND circuits. Furthermore, as demonstrated by the difference among the average value, the mode and the worst case, a not good reproducibility is reported (Figure 4.42). In the worst case a HBM robustness of 750V is measured if a leakage current of 50µA is considered. If a leakage current of 1µA is chosen the HBM robustness is in the most part of the cases lower than 250V both if the DET vs GND and the REF vs GND circuits are considered.



(a) (b)

Figure 4.42: leakage current measured in the (a) DET vs GND and in the (b) REF vs GND circuit during HBM test

MM test

Consistently with TLP analysis all the drain pads show no failure up to 200V during MM test. No significant variation is shown in leakage current monitored during the stress. Similar

considerations can be done for the RF IN and the RF OUT circuit. On the contrary all the V_G vs GND pads and pads corresponding to the detection circuit report a MM robustness lower than 200V. Several devices have been tested. Except for the DET vs GND circuit a low reproducibility has been noticed in the different devices tested. Figure 4.43 shows the worst, the average and the mode value for all the pad submitted to MM measurement. According to the difference noticed between the average and worst case in different devices, a difference in the voltage corresponding to the failure leakage current higher than the measurement step (25V) is shown in different devices considered.

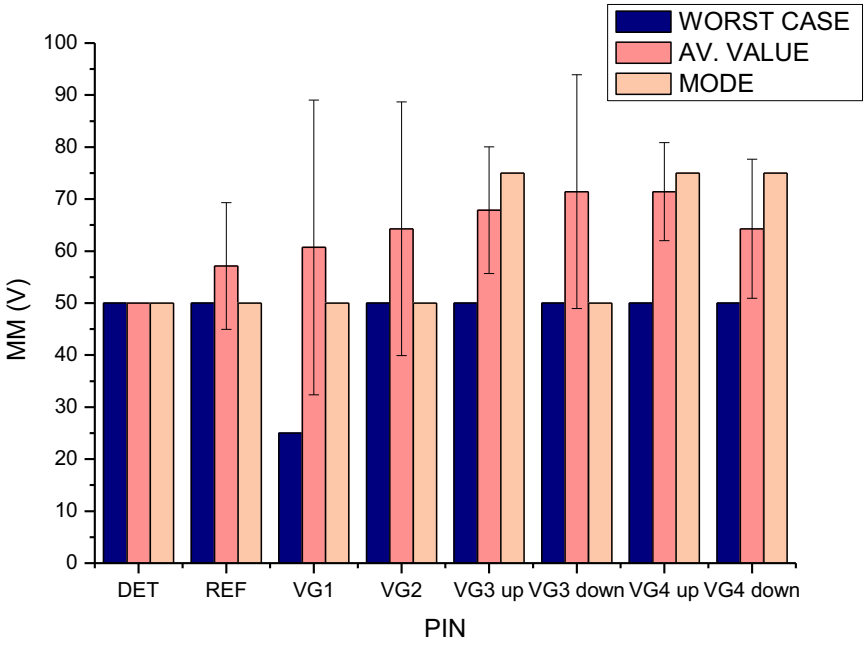


Figure 4.43: MM robustness in gate pads and detection circuit evaluated as average value, mode and worst case

In all the V_G pads an average MM robustness between 60V and 75V has been measured. However the MM robustness evaluated in the worst case is much lower. In the gate pads the worst case is represented by a robustness of 50V. Even if the detection circuit pads appear not to be the most sensitive pads we have to specify that a leakage current of 50μA has been chosen as failure point. If a value of 1μA is considered the robustness is in almost all the devices lower than 25V, both if REF vs GND and DET vs GND pads are studied.

Chapter 5:Trapping phenomena on AlGaN/GaN devices with Fe doped buffer layer

5.1 An Overview of traps in High Electron Mobility Transistors

The importance of trapping phenomena on High Electron Mobility Transistors relies on the effects induced on devices' performances, both in terms of DC and RF aspects. Recoverable degradation due to the presence of traps can be summarized in a decrease of the drain current due to the decrease of the maximum transconductance or to the threshold voltage positive shift. Furthermore traps severely limit the performances in devices which operate at high power and frequency, thus affecting the output power, the cut off frequency and determining an increase of noise even at low frequencies.

In AlGaAs/GaAs devices the effect was attributed to a carrier injection from the channel to the barrier layer with a consequent carrier trapping at low temperatures. The recovery of this phenomenon could happen through light excitation, higher temperature imposition and interchange of source and drain terminals [9].

In GaN technology traps effects are more important and lead to more severe effects as a consequence of the defective nature of the material. Moreover the polarization effects which characterize nitrides are higher than in further III-V materials. Although some devices are characterized by fast trapping in the order of few MHz, in the most part of the cases traps time constants are in a range between 1μs and hundreds of seconds.

Traps have been widely studied in literature by means of several methods, which mainly consist of dynamic transient analysis. Further methods have been reported in literature [1] and include: (i) luminescence investigation [57], (ii) photoionization spectroscopy [58], (iii) surface potential analysis [59] and (iv) deep level transient spectroscopy [60]. Trapping analysis usually provide three typologies of information: (i) thermal behaviour, (ii) energy characteristics and (iii) cross section. Several techniques widely explained in literature will be shown in detail in this chapter.

5.1.1 Trapping mechanisms

Trapping phenomena lead to anomalies in the output I-V characteristics, which can be caused by different aspects: channel carriers trapped in the barrier and in the buffer layer,

unpassivated surface states which can provoke a reduction of conducting charge, especially in the region between the gate and drain terminal.

Traps usually results from defects which depends on the crystal lattice and on the growth processes. An enhancement of trap effects are defined by the mismatch due to the hetero-interface. Finally traps can be caused by hot electron effects as a consequence of the high electric fields applied to the device.

According to literature [9] traps can be located in different parts of a AlGaN/GaN heterostructure: (i) interface between semiconductor and dielectric surface, (ii) barrier layer, (iii) buffer layer, (iv) interface between channel and barrier layer, (v) interface between substrate and semiconductor or nucleation layer, (vi) depletion zones of the series resistances. An example is provided by Figure 5.1.

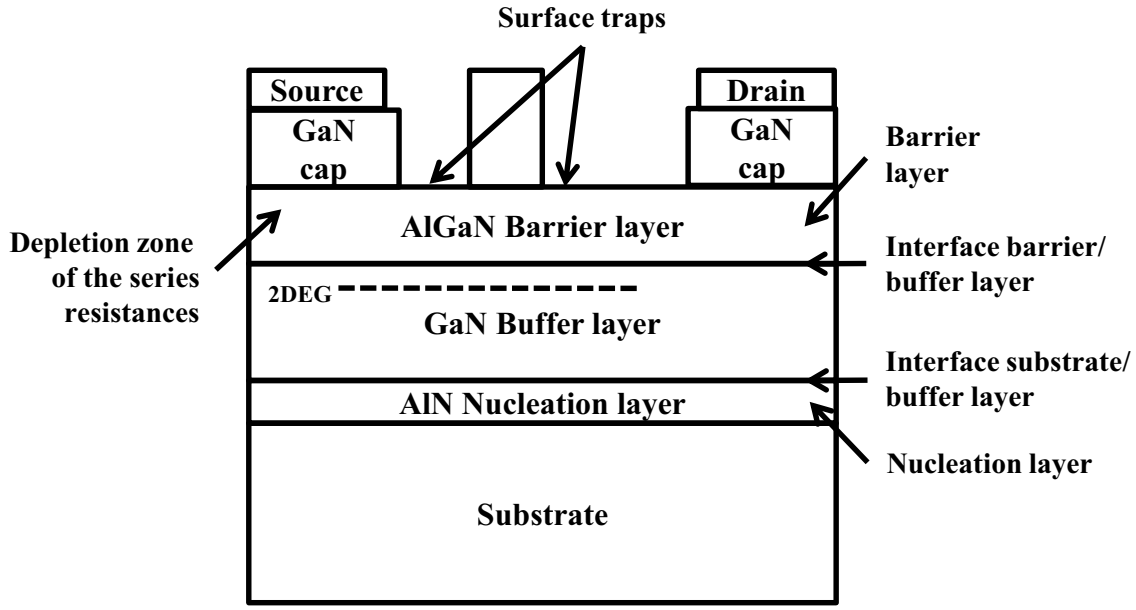


Figure 5.1: possible trap location on a AlGaN/GaN HEMT

One of the aspects which has been widely observed in the traps evaluation is the so called "gate lag". The physical mechanism seems to depend on the recharging of trapping centres when a different gate bias is applied. Studies proposed by several works reported [16], [60], [62] indicates that these trapping centres should be located in the surface and that can induce a strong variation especially when charge is trapped near the transistor channel. It has been associated to with ionized donor states located between gate and drain terminals near the AlGaN surface. Furthermore gate lag is usually defined by a stretched exponential trend in the range of seconds when the transient analysis is considered.

The effect of how traps pinch the channel between the gate and drain terminal is shown in Figure 5.2, where the DC and RF characteristics to demonstrate the RF current lag and mechanisms which define the degradation of RF performances.

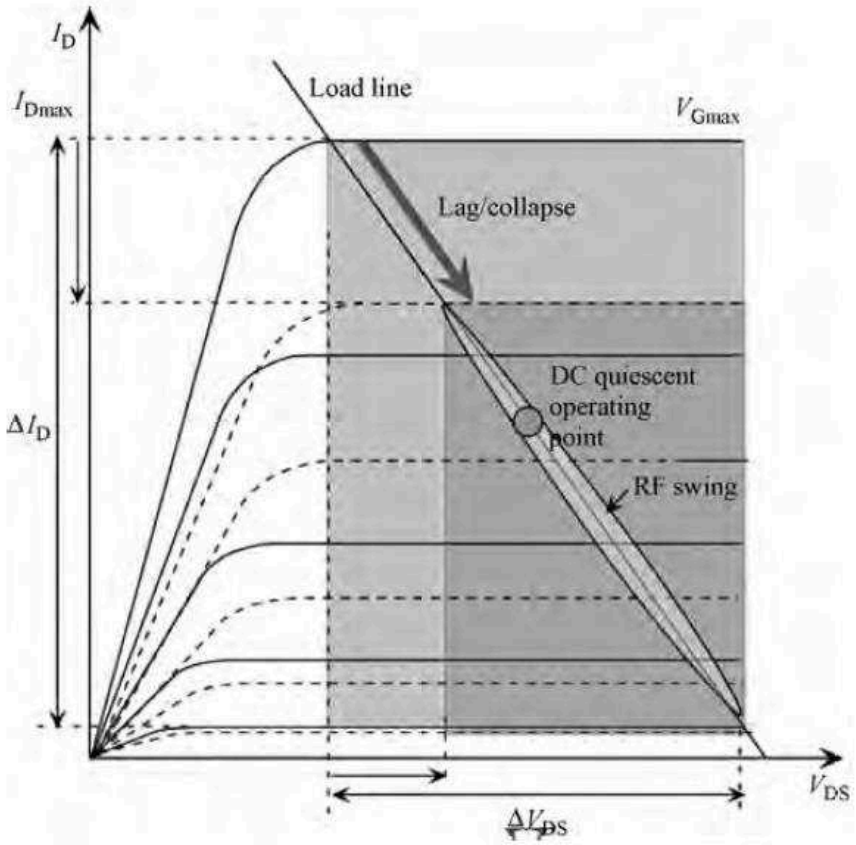


Figure 5.2: RF current lag superimposed to DC and RF characteristics [1]

Gate lag is not the only mechanism which determine current lag, as it can be defined by any negative charge between the channel and the surface. The carriers for barrier trapping, for instance, can be due to tunneling, which can be field assisted, from the gate to the semiconductor or from the channel as a consequence of high electric fields [1]. Finally traps in the buffer can cause kink phenomenon, even if previous works demonstrates than it can induce the so called current collapse and drain lag [63].

Anomalous effects caused by a buffer layer are determined by electrons in an n-channel trapped in the buffer layer which produce a region in the buffer layer characterized by a negative charge [1], [64]. It is usually determined by high drain voltages which induce carriers in the buffer layer where they are trapped by defect states [1]. A definition of this phenomenon has been described in detail by Klein et al. [64]: due to the high field the carriers, created by impact ionization or characterized by an energy high enough to be injected in regions outside the conducting channels, are trapped in defects which are usually located in the buffer layer near

the interface between the buffer and the channel. Recovery, and thus, emission of trapped electrons, can be determined by optical excitation. A schematic, proposed by Klein et al. [64], is shown in Figure 5.3.

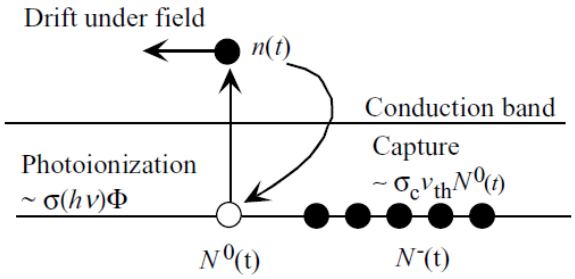


Figure 5.3: schematic of the carrier capture and photoionization of the buffer traps [1],[9]

The presence of traps in the buffer layer leads to the so called kink phenomenon [1]. Kink phenomenon is the drain current decrease measured with DC bias applied when high drain source voltages are applied. An example is shown in Figure 5.4a. Due to the high drain voltage and the consequent high electron field generated, electrons are injected into the buffer layer and get trapped. As a consequence a decrease of the drain current is noticed at first for increasing drain source voltages. Since charge trapped can be released as a consequence of both light and temperature for higher drain source voltage values current decrease can be recovered. Previous works reported in literature [65], [1], suggest that the presence of passivation with the consequent variation of surface states, does not influence the kink phenomenon, thus confirming that traps responsible for kink effect should be located in the buffer layer. A comparison is shown in Figure 5.4b

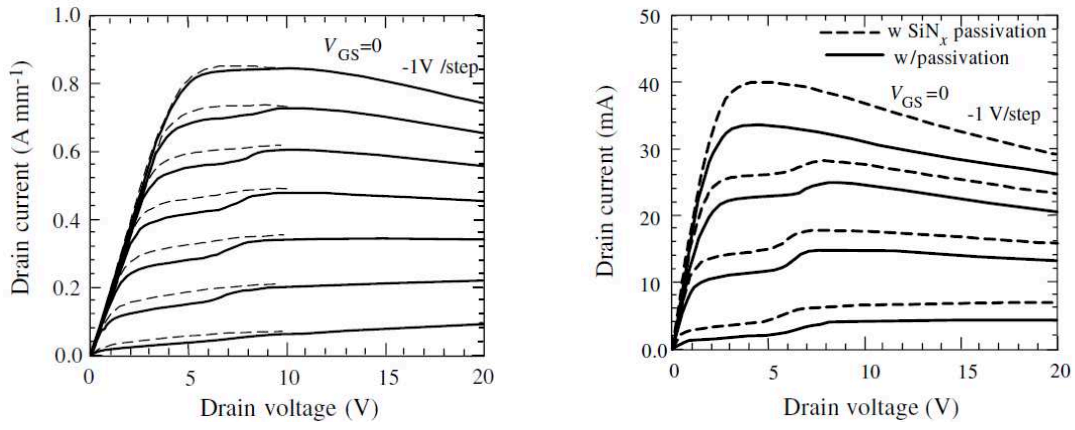


Figure 5.4: (a) kink effect; (b) evaluation of kink effect on a device with and without passivation [65]

Concerning barrier layer trapping an interesting definition is described by Mitrovanof and Manfra [66], with the consideration of localized trapping centres in the barrier layer near the gate and defining the trap level energy position with respect of the Fermi level on the basis of the bias applied to the gate. Figure 5.5 describes the energy diagram of the trapping centres, especially in AlGaN barrier layer, when the electric field is applied. Moreover trend in the absence of the electric field is also shown with dashed lines. The comparison of analysis with and without field demonstrates that the field lowers the barrier for emission [1]. Several different mechanisms can be noticed: (i) thermal ionization over the field-lowered barrier, also called Poole-Frenkel effect; (ii) phonon assisted and (iii) direct tunneling when the barrier width, defined by the distance x, is very low [1].

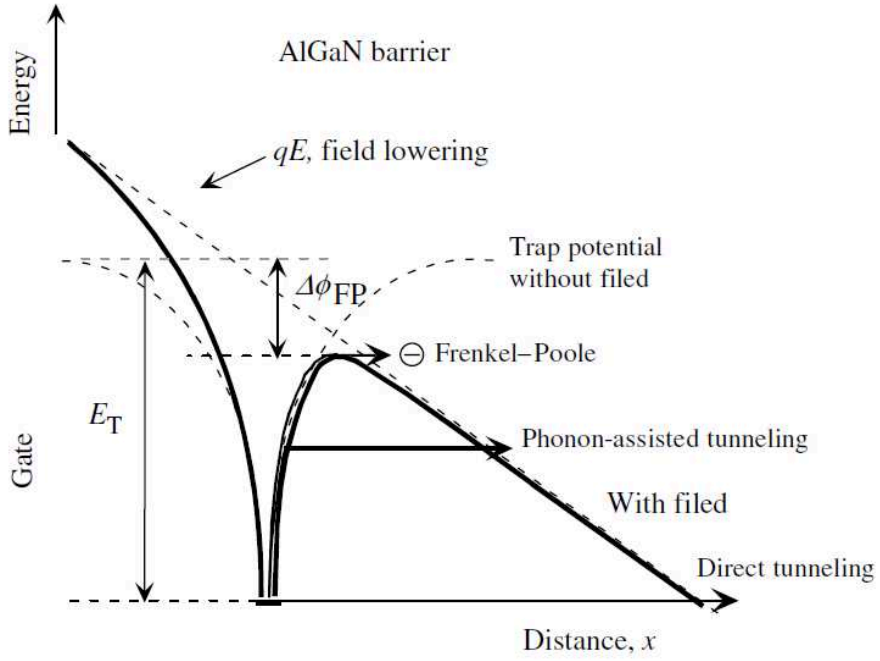


Figure 5.5: energy diagram of trapping center [1]

In the analysis of the correlation of current collapse as a function of surface charging, it is essential to highlight that current compression is strongly determined by surface states and the correspondent thermal distribution [1]. The presence of surface states and, thus, an increase of band bending determines channel depletion and, consequently, drain current decrease [1] (Figure 5.6). Drain current is correlated by the charge accumulation of traps located in the surface states or in the barrier layer, in both the cases placed at the edge of the gate terminal.

Drain current decrease due to surface states is higher in high frequency operating conditions [67]. When a device is switched at high frequency between gate bias points characterized by a strong difference, traps are not able to follow gate bias variation and cause a drain current variation. When the channel is defined (ON state condition) surface states are

donors levels positively charged to generate the 2DEG, while, in OFF state condition, electrons in the gate migrate to compensate the surface charges [68], [69]. As a consequence of traps high time constants, surface charges cannot assume the position previously achieved when the device is turned in ON state again. The presence of a negative charge which keeps the device partially in OFF condition limiting the drain current is therefore assumed. According to explanation described by Sabuktagin et al. [69], this condition can be ascribed to the presence of a "virtual gate" which limits the channel generation, thus determining a drain current decrease. A further explanation of the trapping mechanisms is provided in Figure 5.7.

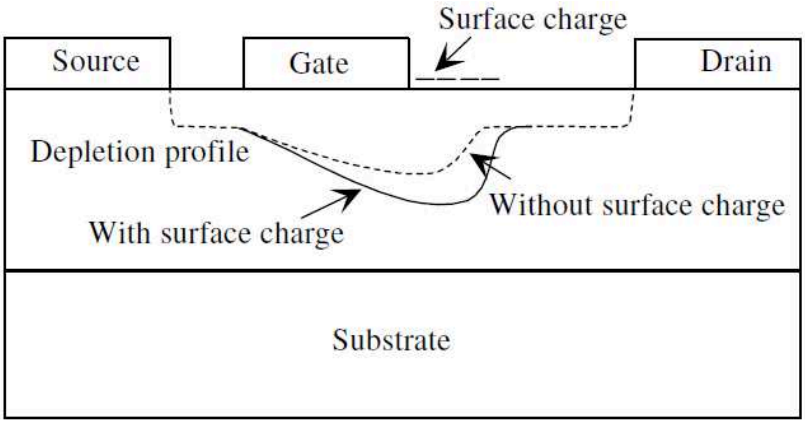


Figure 5.6: surface state effects on the depletion profile of a HEMT channel [1]

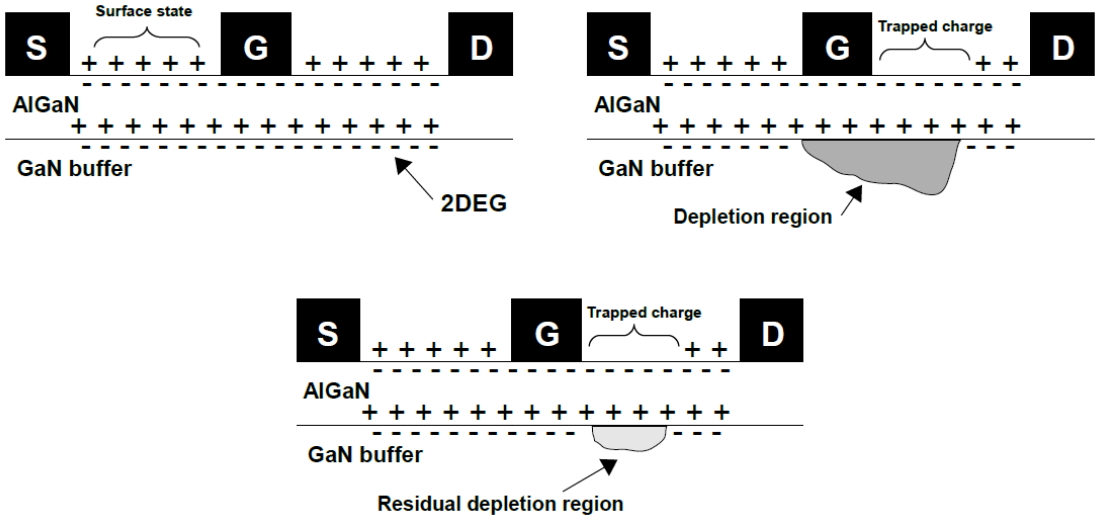


Figure 5.7: current compression mechanism

5.1.2 Design improvements to avoid trapping effects

Surface passivation

In literature several improvements and design issues concerning HEMT are reported. One of the most used solution to reduce charge trapped due to surface states is the deposition of a thin insulating layer, called passivation process, based on silicon nitride (SiN). A interface between the dielectric and the semiconductor is created, thus limiting surface charge defined by surface defects and leftover charge. SiN passivation is characterized by some issues such as the difficulty of generate a uniform layer deposition. The thin passivation is furthermore important since it protects the device from contaminants that may be present in the ambient environment.

Previous works reported in literature [65], [70], [71] establish that several improvements, both concerning DC and RF characteristics, are due to the presence of a passivation layer. If electrical properties are considered a contact resistance decrease of four order of magnitude has been demonstrated [72]. Furthermore an increase of the barrier height of almost 0.35eV has been measured [72].

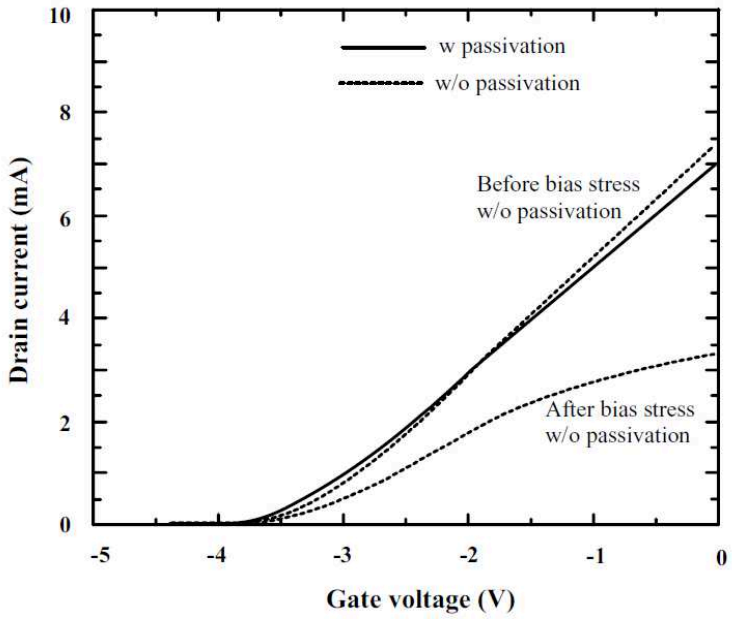


Figure 5.8: $I_D V_G$ measured in a device with and without passivation after drain stress at 10V [73]

The analysis of different materials used for passivation confirms that the silicon nitride is more effective than other materials, for instance SiO_2. The comparison between Si_3N_4 and SiO_2 proposed by Bernat et al [65]., demonstrates significant improvements, consequent to the high dielectric/semiconductor interface density in SiO_2: (i) higher carrier concentration at the interface, (ii) RF cut-off frequency and power performances, (iii) drain breakdown voltage.

Figure 5.8 shows a comparison between devices with and without passivation after drain stress by applying a drain voltage of 10V [73]. The device with no passivation layer exhibits a much higher drain current decrease after the stress

Field Plate

A second method to reduce dispersion issues consists of field plate structure. The field plate structure is a gate with a *T* or Γ shape which partially covers the gate drain region [13]. Therefore surface traps effects are limited as a consequence of a distribution of the electric field between the gate and the drain terminal, avoiding one of the main causes of the charge migration from the gate. With the use of a field plate the electric field peak at the edge of the gate terminal is distributed over the whole contact. The use of a field plate offers further advantages in applications which need high breakdown voltage, such as high voltage switching and high power amplifiers.

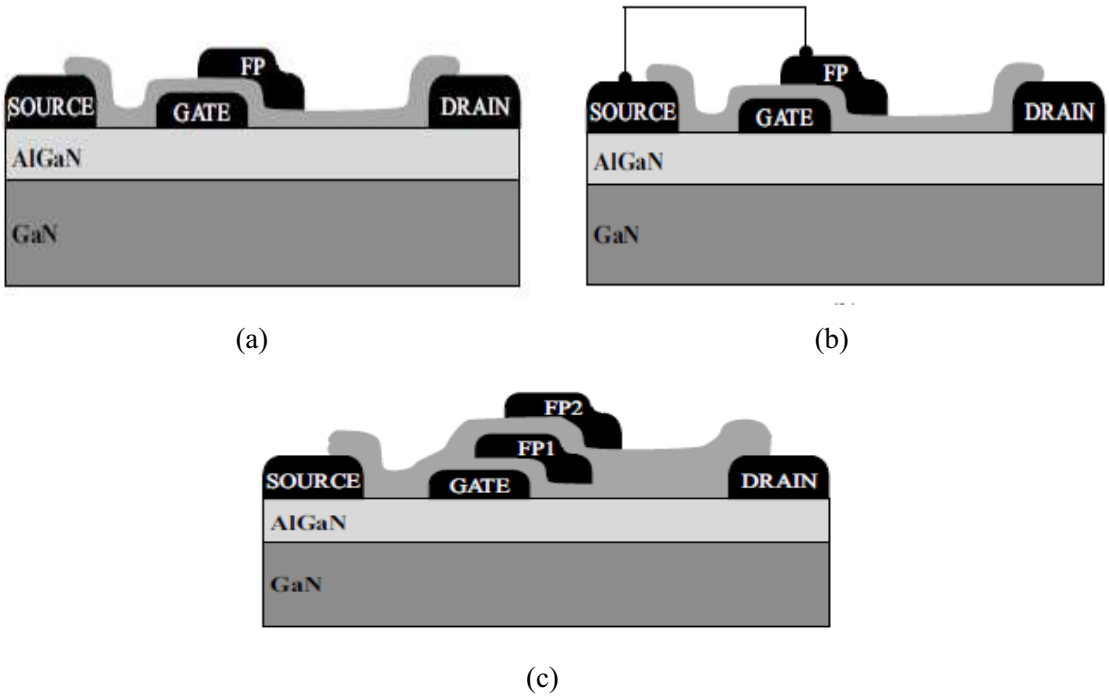


Figure 5.9: field plate schemes: (a) gate terminated field plate, (b) source terminated field plate, (c) multiple field plate structure [13]

Several methods to implement field plates are shown in Figure 5.9 [13]. The gate terminated field plate, which consists of an assisted extension of the gate toward the drain, offers a good solution, although an increase of the feedback capacitance between gate and drain is noticed. A further improvement is obtained connecting the field plate to the source, as reported in Figure 5.9b. Similarly, an increase of the drain source and gate source capacitance is

noticed, even if a reduction of the gate drain capacitance is shown. Several design schemes use both gate connected and source connected field plate to reach a trade-off between the enhancement of parasitic capacitances, thus obtaining improvements both in terms of breakdown voltage, trapping phenomena and device performances.

5.1.3 Methods to evaluate trapping phenomena

Several methods have been described in literature to evaluate trapping phenomena. Some of the techniques include luminescence investigation, photoionization spectroscopy, surface potential analysis, deep level transient spectroscopy (DLTS), pulsed and transient analysis, gate and drain lag. In this paragraph three different method are described: (i) pulsed measurements, also called double pulse; (ii) drain current transients; (iii) transconductance frequency dispersion ($g_m(f)$). The first two methods have been deeply used in the analysis while the last one will be explained since necessary to propose a comparison with drain current transients analysis.

Pulsed measurements

Pulsed measurements have already been summarized in 3.3.1. A more detailed analysis and description, also on the basis of the explanation provided in 5.5.1 about trapping phenomena and corresponding physical mechanisms, will be here presented.

Double pulse measurement is a pulsed analysis similar to DIVA (Dynamic IV Analyser) and based on a custom setup. The device is commonly biased with RF GSG tips inside a Karl Suss probe station. The setup is composed by two pulsers, in our case a HP8110A pulser at the gate terminal and a HP8114A pulser at the drain terminal. As it is possible to see in Figure 5.10 a HP8114A pulser is connected to the drain terminal through a R_{LOAD} impedance, while a HP8110 pulser is connected to the gate terminal; therefore a train of pulses is contemporaneously applied to the gate and to the drain terminal, while the source terminal is always ground connected. All the signals are acquired by an oscilloscope synchronized by using the gate source signal as trigger. As it is possible to notice in Figure 5.10 the transistor is connected in class A configuration. The output curve (both I_DV_G and I_DV_D) is defined by pulsing both the drain and the gate terminal from different power dissipation levels, also called baselines or quiescent bias point. The current which flows in the transistor is calculated as the current which flows to the R_{LOAD} impedance (Figure 5.11).

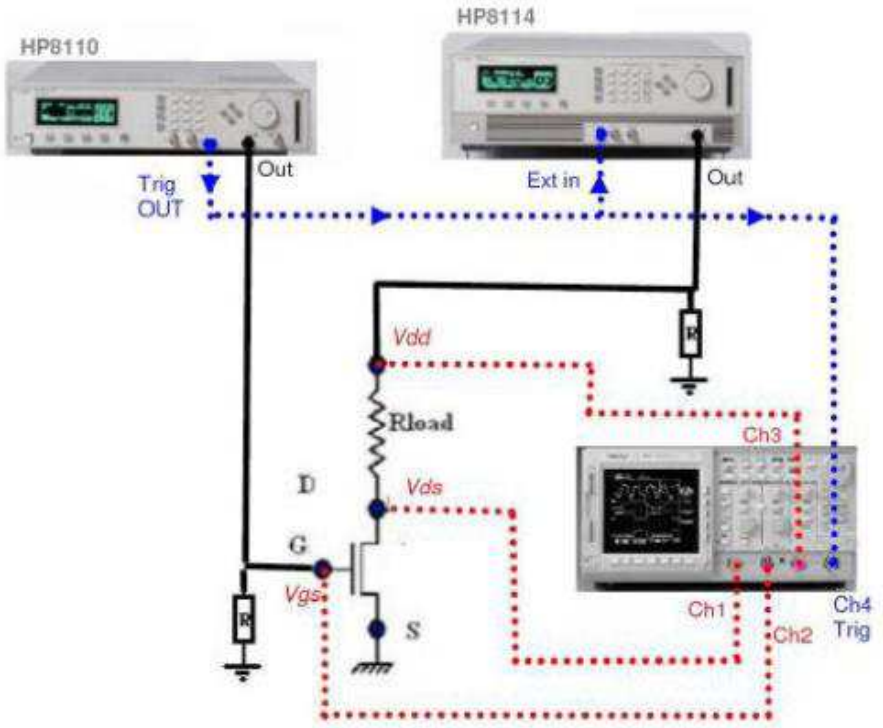


Figure 5.10: double pulse custom setup

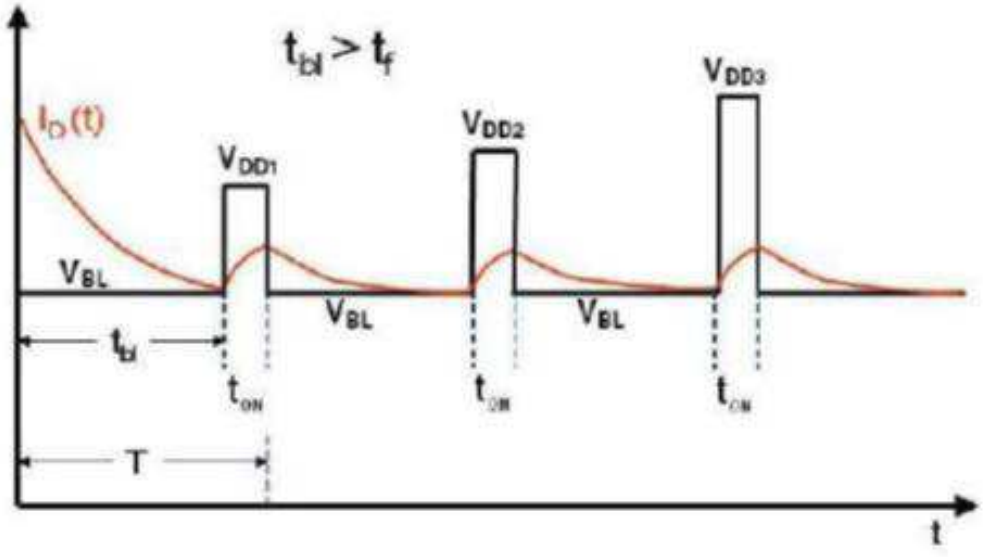


Figure 5.11: drain pulses applied during pulsed measurements and correspondent drain current

In order to study trapping phenomena several power dissipation levels are applied. The first baseline usually corresponds to a null power dissipation level, in order to understand the device behaviour when no trap influence is reported. Further quiescent bias points are applied in order to induce significant trap effects by the application of gate and drain bias which determine: (i) a higher leakage current and (ii) a higher drain gate voltage and, thus, a higher electric field.

The choice of an accurate pulse width and duty cycle is one essential aspect of pulsed measurements. Indeed pulse width must be short enough not to induce self-heating; on the other hand the current measured during the pulse must be constant at least in the portion of the pulse considered for the pulsed analysis. During pulsed analysis both a I_{DS} vs V_{DS} and a I_{DS} vs V_{GS} trend are usually defined. On the basis of the curves measured the following parameters are then calculated:

(i) Current Collapse (CC). The current collapse is defined as the ratio between the difference of the drain current measured at a defined V_{GS} and V_{DS} in two different quiescent bias points over the drain current in the first one. It is usually evaluated at the knee voltage in high dissipation condition, in order to consider the worst case.

$$Current\ Collapse\ (CC) = \frac{I_D^n - I_D^1}{I_D^1} \qquad (5.1)$$

(ii) slump ratio. Slump ratio (SR) is a parameter similar to the current collapse. It evaluates the relationship between drain current measured in two different quiescent bias points and it is calculated as the ratio between the drain current measured in two conditions

(iii) Threshold voltage dynamic shift. It is defined as the difference between the V_{TH} measured in different quiescent bias point

(iv) R_{ON} variation. It is calculated as the ratio of the on resistance measured in linear zone when two different quiescent bias points are applied

(v) max g_m variation. It is defined as the ratio between the peak of the transconductance evaluated when two different power dissipation levels are considered

Drain current transient

Drain current transient technique has been developed on the basis of the work of Joh et al. [74]. Drain current transient analysis is based on a custom setup, based on a power supply at the drain terminal, an amplitude waveform generator at the gate terminal and an oscilloscope to monitor the signals. The device, connected to the power supply with a load resistance, is biased with RF tips inside a Karl Suss probe station.

A similar setup, aimed at the achievement of much higher drain and gate bias during the measurements can be developed by means of two amplitude waveform generators connected with a 20x amplifiers and an oscilloscope. This second approach leads to some important advantageous aspects: (i) higher drain and gate voltages (up to 200V), (ii) the use of a single load resistance, since the drain source voltage is defined by the amplitude waveform generator.

In this paragraph, consistently to the measurements reported, only the first setup will be described in detail.

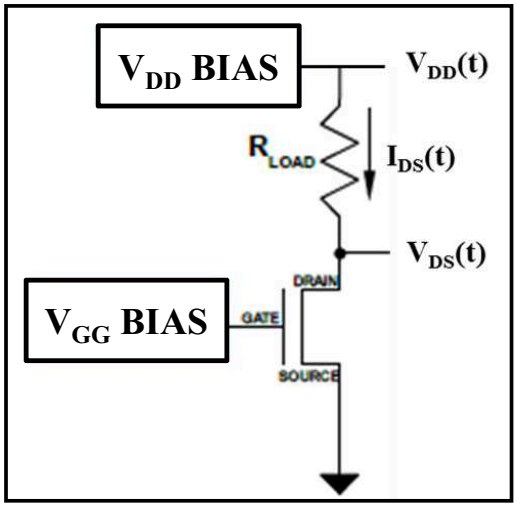


Figure 5.12: drain current transient setup (1st version)

During drain current transients the device is biased for a defined amount of time (usually 100s) in OFF state in a trapping condition. By switching the gate terminal from an OFF state to a ON state condition the device is then kept in a de-trapping condition. Sensitive parameter variation as a function of de-trapping time is measured through the load resistance; main parameter considered are usually the drain current in saturation region and the on resistance in linear zone. The load resistance value is chosen on the basis of the drain current which flows on the device in order to obtain the required drain source voltage value during both trapping and de-trapping phase. A schematic of the principle of operation and, thus, of the drain source voltage applied during OFF and ON state on the basis of the load resistance is shown in Figure 5.12 and in Figure 5.13.

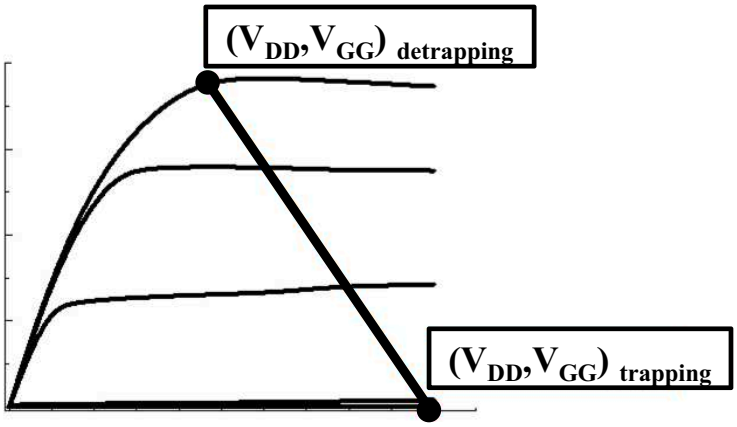


Figure 5.13: principle of operation of drain current transient setup

One of the main advantages of drain current transient technique is the high range of time included in the analysis. Differently from double pulse measurements reliable results can be measured between 1μs and hundreds of seconds. Furthermore drain current transients avoid the difficulty faced by DLTS measurements when devices with small dimension or characterized by a low capacitance value are considered. Finally, one of the important aspects is the possibility of integrating the drain current transient setup with further electrical measurements such as DC measurement used to monitor degradation or to apply a stress to the device.

The trapping and de-trapping transient data can be analysed with several techniques in order to define the time constant. A first method consists in fitting transients with a sum of pure exponentials following a least mean square fashion. This techniques follows the hypothesis that the several trapping processes which characterize the device behaviour are independent and decay with an exponential trend. The fitting function can be expressed by:

$$I_{DS} = I_{DS,\infty} - \sum_{i=1}^{n} A_i e^{-(t/\tau i)} \qquad (5.2)$$

A second method takes into account similar considerations. However, following the assumption that several processes do not follow a pure exponential, a further solution is provided by fitting the transient data with a sum of stretched exponentials. The following equation explains the fitting function:

$$I_{DS} = I_{DS,\infty} - \sum_{i=1}^{n} A_i e^{-(t/\tau i)^{\beta}} \qquad (5.3)$$

A final technique consists of the time constants determination in correspondence with the maximum variation of the transient data, which can be simply defined through the peak of the derivative function.

Drain current transient provides several important information: (i) traps thermal behaviour, which can lead to activation energy and cross section definition; (ii) evaluation of de-trapping characteristics on the basis of the gate and drain voltage applied during the trapping phase, thus explaining and making hypothesis about trapping phenomena and location; (iii) identification of line defects with filling time evaluation. Traps thermal behaviour can be evaluated by means of the data transient definition as a function of several ambient temperatures imposed. Through the determination of the time constants associated to each traps for every ambient temperature applied it is possible to define the Arrhenius plot, thus calculating the activation energy and the thermal cross section.

As discussed before for pulsed measurement, the imposition of a different gate and drain voltage during both trapping and de-trapping phase can lead to the evaluation of different trapping effects. Similarly to double pulse measurement, during the trapping phase it is possible to impose a bias at the gate and at the drain terminals which can lead to a higher gate leakage current or a higher electric field, thus enhancing the effect of different trapping phenomena and allowing to make hypothesis about both the trapping physical mechanism and the trap location.

Drain current transients can provide significant information about the nature of the defect which induce trapping mechanisms through filling time dependence analysis. This analysis basically consists of evaluating the data transient by varying only the trapping time and evaluating the variation of trap amplitude or time constants as a function of the trapping time (also called filling time). Cho et al. [75] explains, on the basis of simulation methods to describe charge in dislocations and point defects, that a significant dependence between the logarithmic trend of the amplitude variation as a function of filling time and line defects can be demonstrated. Indeed by changing the duration of the trap filling pulse used for transient measurements it is possible to understand if a deep level originates from point defects, or from linearly-arranged ones. Indeed, the occupancy of non-interacting point defects has an exponential dependence on the duration of the filling pulse, according to the (5.4)

$$N_T(t_p) = N_T + (n_T(0) - N_T)exp(c_n t_p) \qquad (5.4)$$

On the other hand, for linearly arranged defects the concentration of captured electrons depends logarithmically on the trap filling time, according to (5.5)

$$n_T(t_p) = c_n \tau N_T ln\left(\frac{t_p}{\tau}\right) \qquad (5.5)$$

Dynamic Transconductance Dispersion

Dynamic transconductance dispersion ($g_m(f)$) has been widely studied to characterize traps in MOS devices. A detailed description has been provided by Haddara et al. [76], where the transconductance frequency dispersion is demonstrated by considering a capacitance-resistance scheme to model the trap behaviour. A consistent measurement technique has been recently presented by Silvestri et al. [77], [78] to apply this technique also to AlGaN/GaN structures in quasi-equilibrium conditions. The measurement is usually carried out by biasing the drain terminal in the ohmic regime and keeping the gate terminal in the sub threshold region. The first condition is essential to analyse the whole channel region under the gate, while the second

condition is important not to taking into account the inversion layer capacitance. A constant drain voltage is applied while the gate terminal is biased with an AC voltage, with frequencies usually between 1Hz and 10kHz.

The technique is based on the assumption that a strong correlation exists between the inverse of the transconductance imaginary part and the trap conductance (G_p/ω), according to the following equation, where C_b is the barrier layer capacitance and I_d the drain current.

$$\frac{G_p}{\omega} = -qC_b I_d \frac{1}{kT} Im \frac{1}{g_m} \qquad (5.6)$$

One of the main advantages is that (i) this method limits inaccuracies induced by unwanted trapping phenomena, since only traps near the Fermi level are taken into account. Furthermore, (ii) on the basis of the transconductance variation with the gate voltage applied it is possible to make hypothesis on whether the evaluated region is in the buffer or barrier layer. Indeed the formula which describes the transconductance trend as a function of frequency explains how the variation of the time constant corresponding to the transconductance peak indicates that the states at the heterointerface are considered, as a consequence of the relationship between the time constant and the density of electrons in the channel (see (5.6)). Indeed any variation in the dc gate voltage induces a change in the electron density in the channel, varying the time constant. When the frequency of the peak is characterized by no variation with gate source voltage we can make the hypothesis that traps evaluated are probably in the buffer layer. Finally (iii) the application of a low drain current, due to the ohmic regime and sub threshold region condition, introduces negligible self-heating effects, thus avoiding inaccuracies in the Arrhenius plot due to a significant discrepancy between junction and ambient temperature. The cross section is measured on the basis of (5.7), where v_{th} is the thermal velocity and n_s the density of the electrons in the channel.

$$\tau = \frac{1}{v_{th}\sigma_t n_s} \qquad (5.7)$$

5.2 Overview of degradation phenomena in AlGaN/GaN devices

Although the HEMT technology obtained significant performances in RF and power applications, the reliability of HEMTs is severely affected by degradation mechanisms. Meneghesso et al.[79] have described in detail the phenomena which can limit device performances and reduce their reliability. These aspects can be divided in three main groups, according to their failure and accelerating mechanisms: (i) thermally activated, (ii) hot electrons, (iii) aspects related to GaN technology, especially AlGaN/GaN structures. A summary, which describes also the degradation location, is shown in Figure 5.14.

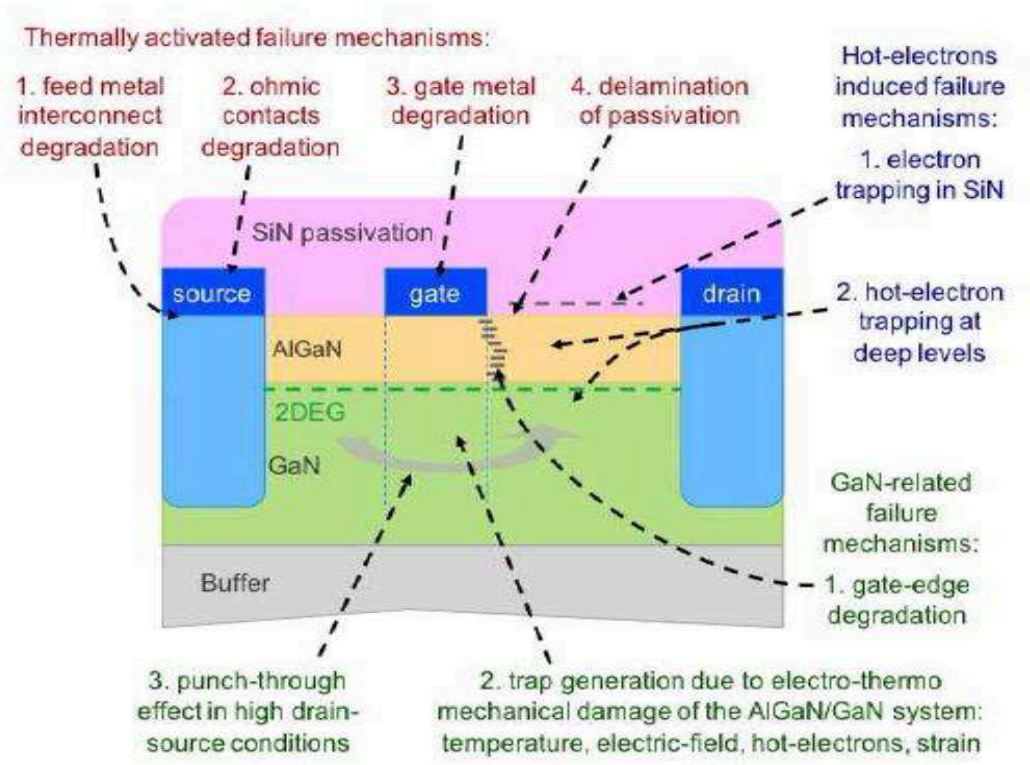


Figure 5.14: degradation mechanisms in a AlGaN/GaN structure [79]

The first aspect can induce effects which are mainly connected to Schottky and ohmic contacts. Furthermore, the degradation of metal interconnects and the delamination of passivation can be noticed. Electrical aspects can be summarized in: (i) trapping, which can be

noticed both in the SiN passivation layer and in deep levels; (ii) hot electrons, which can enhance the generation of lattice defects, especially when on state conditions are taken into account. Finally degradation related to the GaN technology must be considered. It can be described by (i) gate edge degradation due to the application of a negative bias at the gate terminal and (ii) the generation of traps which can be determined by electro-mechanical damage of the AlGaN/GaN system. This phenomenon is typically enhanced by the conjunction of several mechanisms during a stress condition: temperature, the imposition of a high electric field, presence of hot electrons and intrinsic strain due to GaN material. (iii) A high drain source condition imposed during the stress leads to the presence of punch-through, thus defining a significant passage of current even when OFF state condition is applied to the device. The drain and gate current measured in OFF state can be reduced by the introduction of iron or carbon doping in the buffer layer, thus creating an insulator layer which limits the punch-through effect.

If electrical degradation is considered, it is important to distinguish the device robustness when an OFF state or a ON state stress is applied. Indeed different degradation mechanisms are reported in the two conditions. When a reverse bias stress is imposed recoverable and permanent modification of electrical parameters is shown, mainly described by a permanent degradation of the gate current due to the generation of conductive paths for leakage gate current. When an on state stress is considered, electrical degradation is mainly described by the electric field generation between the gate and drain terminal and by effects related to the presence of hot electrons.

5.2.1 Off state stress

The reverse bias stress is evaluated by biasing the device in OFF state through the application of a negative voltage to the gate. A first kind of stress is called “reverse bias”; during the stress a negative voltage is applied to the gate while both the source and drain terminals are grounded if a symmetrical geometry is considered or just the drain terminal is grounded and the source is floating in the opposite case. Therefore the degradation is induced by the increasing leakage current and by the application of a higher electric field at the GS or GD diode. In the second kind of stress a high electric field is generated by biasing the device with a high drain gate voltage.

During an off state and on state stress the high electric field can be generated with a step stress or a constant voltage stress: in the first case an increasing voltage is applied for a defined amount of seconds, while in the second case the device is biased with a constant voltage up to degradation. Several studies have been reported in literature concerning the robustness of

AlGaN/GaN devices submitted to off state stress. A permanent degradation of the gate current due to the generation of conductive paths for leakage gate current has been demonstrated. According to previous works reported this mechanism is ascribed to inverse piezoelectric effects [80] or to a defect percolation effect [81], [82].

When the gate diode is biased in reverse bias condition an initial recoverable degradation is noticed, followed by a permanent gate diode damage. The effects during the stress can be divided into three main regions: (i) in the first region, during stress at moderate reverse gate bias, gate current shows an exponential and recoverable decrease, as a consequence of negative charge trapped under the gate. If further stress is applied a not recoverable damage is creating and mainly consists of defects randomly created due to defect generation and percolation process. Defects can be located in the barrier layer or at the hetero-interface, i.e. between the barrier and the buffer layer. Defects created lead to an increase of the noise superimposed to gate current, corresponding to the second region (ii) and to the generation of not recoverable leakage paths which determine a strong increase of the gate leakage current (iii). These degradation phenomena are noticed both if a step stress and a constant stress are imposed, as demonstrated by Figure 5.15.

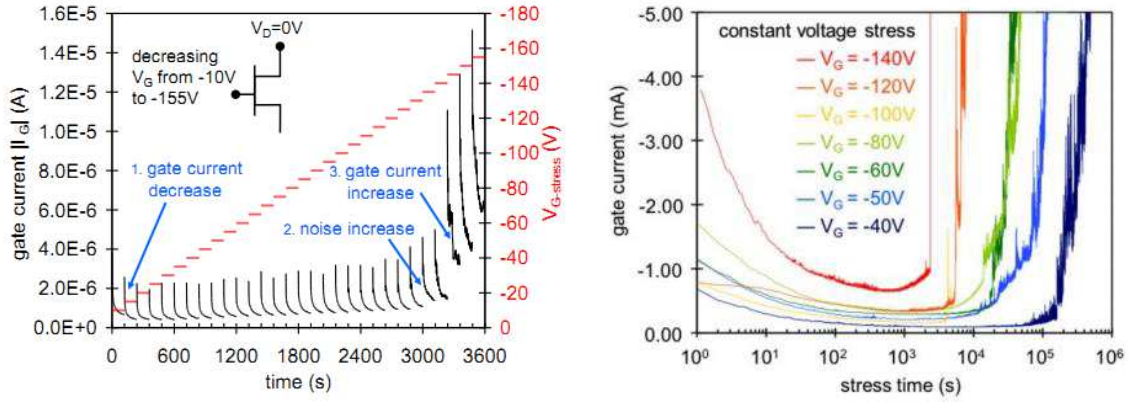


Figure 5.15: gate leakage current degradation during (i) step stress and (ii) constant voltage stress [79]

The increase of the gate leakage current is strongly correlated to the generation of “hot spots” detected with electro luminescence measurements which confirm the generation and increase of leakage conductive paths. Results reported in [79] confirm that a good correlation between the voltage stress imposed and the failure time is reported when a constant voltage stress is applied

5.2.2 On state stress

A device is submitted to a on state stress by biasing it with a gate voltage, corresponding to semi-on or high dissipation condition, and a high drain source voltage. In the case reported [79] devices have been stressed with several gate source voltages, in order to study its correlation with device degradation.

Devices submitted to on state stress reveal a strong decrease of a drain current mainly due to an increase of the on resistance measured in the linear region. Furthermore a decrease of the ratio between the electro luminescence and the drain current is noticed, thus suggesting a variation of the electric field generated with the gate drain voltage applied. From the variation of the electric field we can suppose that degradation is mainly induced by hot electrons. The application of a on state stress demonstrates a decrease of the electric field as a consequence of the trapping of negative charge in the access region between the gate and the drain terminal. The decrease of the on resistance measured in linear region confirms this phenomenon.

The correlation between electro luminescence and hot electrons let us make the hypothesis that hot electrons determine the degradation process. When a high drain source voltage is applied hot electrons are accelerated by the higher electric field generated and can be trapped in the device, especially in the hetero-interface, in the barrier layer or in the passivation layer.

The hypothesis is demonstrated by the not monotonic trend shown by the degradation effects as a function of different gate source voltage applied. The degradation dependence on gate source voltage is consistent with the bell shape reported by the electro luminescence measured as a function of gate source voltage, thus reflecting the hot electron behaviour, both in terms of amount and energy, with bias applied and its correlation with electro luminescence decrease as a function of stress bias applied. The hypothesis made is further demonstrated by the correlation established between the time to failure during the on state stress and the electro luminescence measured in a fresh device, which is directly proportional to hot electrons in the channel [79].

5.3 Description of analysed devices

5.3.1 AlGaN/GaN HEMTs with different Fe doped buffer layer

Analysed devices (named sample A-D) are AlGaN/GaN HEMTs with similar structure except for the Fe doping quantity in the buffer layer and buffer thickness, as described in a schematic cross section shown in Figure 5.16. Fe doping in the buffer layer, similarly to carbon doping, is usually introduced in order to reduce parasitic effects such as punch through phenomenon and, thus, to reduce drain and gate leakage current. The structure of the analysed AlGaN/GaN HEMT consists in a 20 nm $Al_{25}Ga_{75}N$ barrier layer with a 25% Al content. Fe doped devices are characterized by a 1.9 µm buffer layer thickness; a similar value (2.4 µm) is reported in devices with no buffer doped. Except for device A all the devices are characterized by an iron doped buffer, with increasing Fe doping from $1 \cdot 10^{17}$ in sample B to $4 \cdot 10^{17}$ in sample D. A 4H SiC and a 6H SiC substrate characterize device A and Fe doped devices, respectively. All the samples are covered with a SiN passivation layer to reduce surface trapping. An identical maskset is used for all the wafer tested. Devices dimensions are W_G=2x50 µm, L_G = 0.5 µm, L_{GS} = 1.25 µm, L_{GD} = 2.25 µm. Devices are not covered by field plate or air bridge.

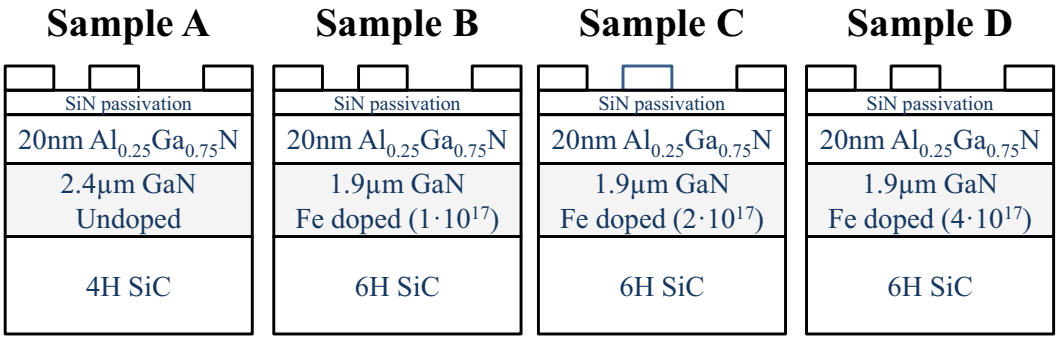


Figure 5.16: AlGaN/GaN HEMTs with different Fe doping quantity

DC Characterization

DC preliminary evaluation demonstrates that no significant variation is measured among devices with different characteristics. A good variability has been reported in devices belonging

to the same wafer. An example of DC characterization measured in samples belonging to different wafers is reported. Figure 5.17 shows the DC analysis on a sample A.

Devices belonging to sample A measured before the stress are characterized by a I_{DSS} of about 0.85A/mm and 0.65A/mm when measured at high dissipation condition at V_{GS}=1V and V_{GS}=0V, respectively. When measured in OFF state a I_{DLEAK} in the order of 0.1µA/mm and 1µA/mm is reported in linear and saturation zone, respectively. I_{GLEAK} measured in OFF and ON state shows consistent values with the GS diode. This last demonstrates a diode gate current of 0.1µA/mm when a reverse bias is applied (at V_{GS}=-6V). When a forward bias is applied (at V_{GS}=1V) a diode current of about 1µA/mm is measured. A transconductance peak higher of 0.35S/mm has been measured in saturation zone (V_{DS}=10V).

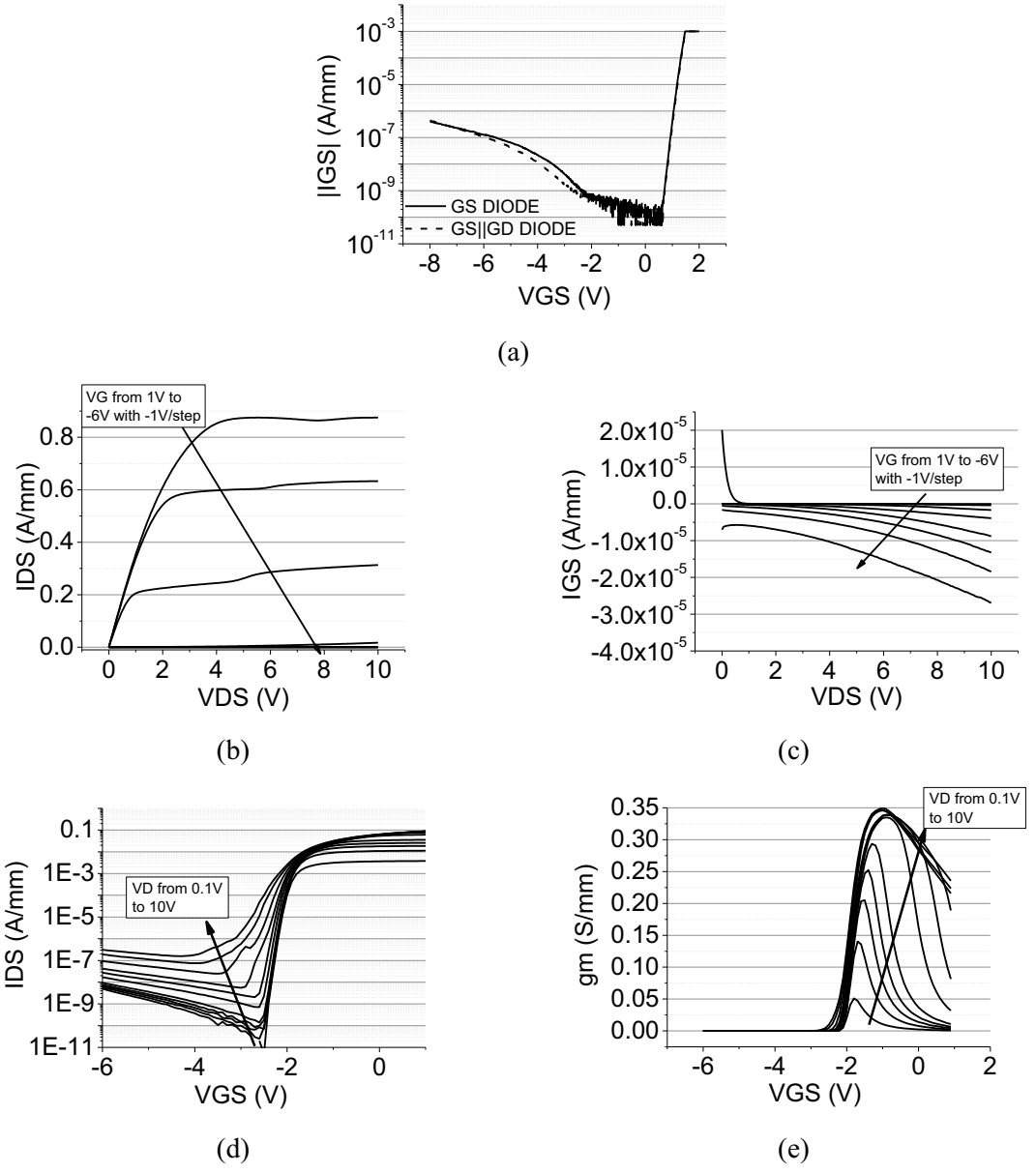


Figure 5.17: DC characterization in a AlGaN/GaN HEMT – sample A: (a) GS diode, (b) IDVD and (c) IGVD curve, (d) transcharacteristic, (e) transconductance

Devices belonging to sample D measured before the stress are characterized by a I_{DSS} of about 0.8A/mm and 0.6A/mm when measured at high dissipation condition at V_{GS}=1V and V_{GS}=0V, respectively. When measured in OFF state a I_{DLEAK} in the order of 1µA/mm and 10µA/mm is reported in linear and saturation zone, respectively. I_{GLEAK} measured in OFF and ON state shows consistent values with the GS diode. This last demonstrates a diode gate current lower than 10µA/mm when a reverse bias is applied (at V_{GS}=-6V). When a forward bias is applied (at V_{GS}=1V) a diode current of about 10µA/mm is measured. A transconductance peak higher than 0.3S/mm has been measured in saturation zone (V_{DS}=10V). Described data are reported in Figure 5.18.

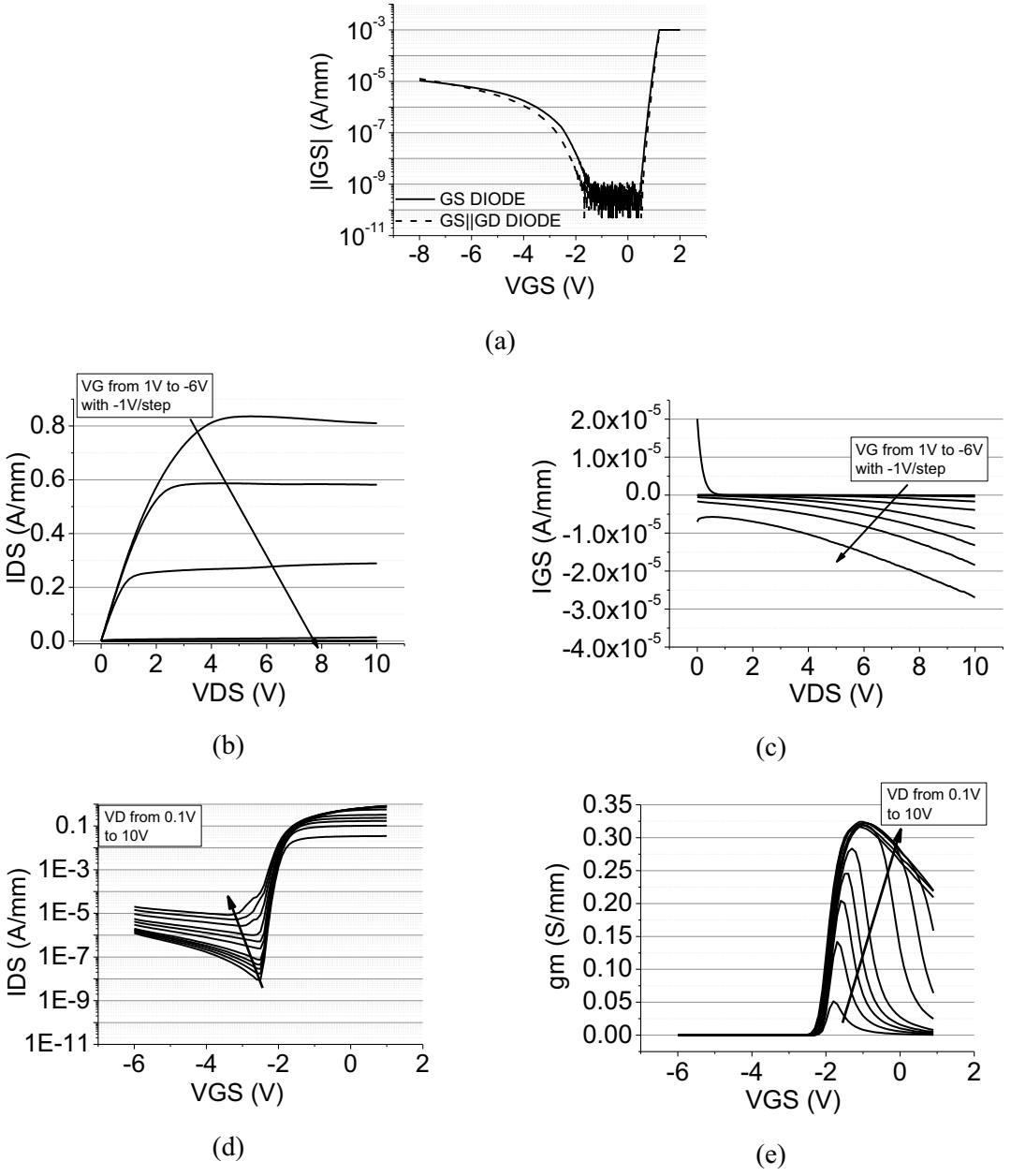


Figure 5.18: DC characterization in a AlGaN/GaN HEMT – sample D: (a) GS diode, (b) IDVD and (c) IGVD curve, (d) transcharacteristic, (e) transconductance

Similar results have been reported in samples B and C, characterized only by a lower iron quantity in the buffer layer. For completeness, details about DC curves measured are shown in Figure 5.19 and Figure 5.20.

The introduction of a different Fe doping quantity does not influence in a significant way the drain and gate current measured in OFF state.

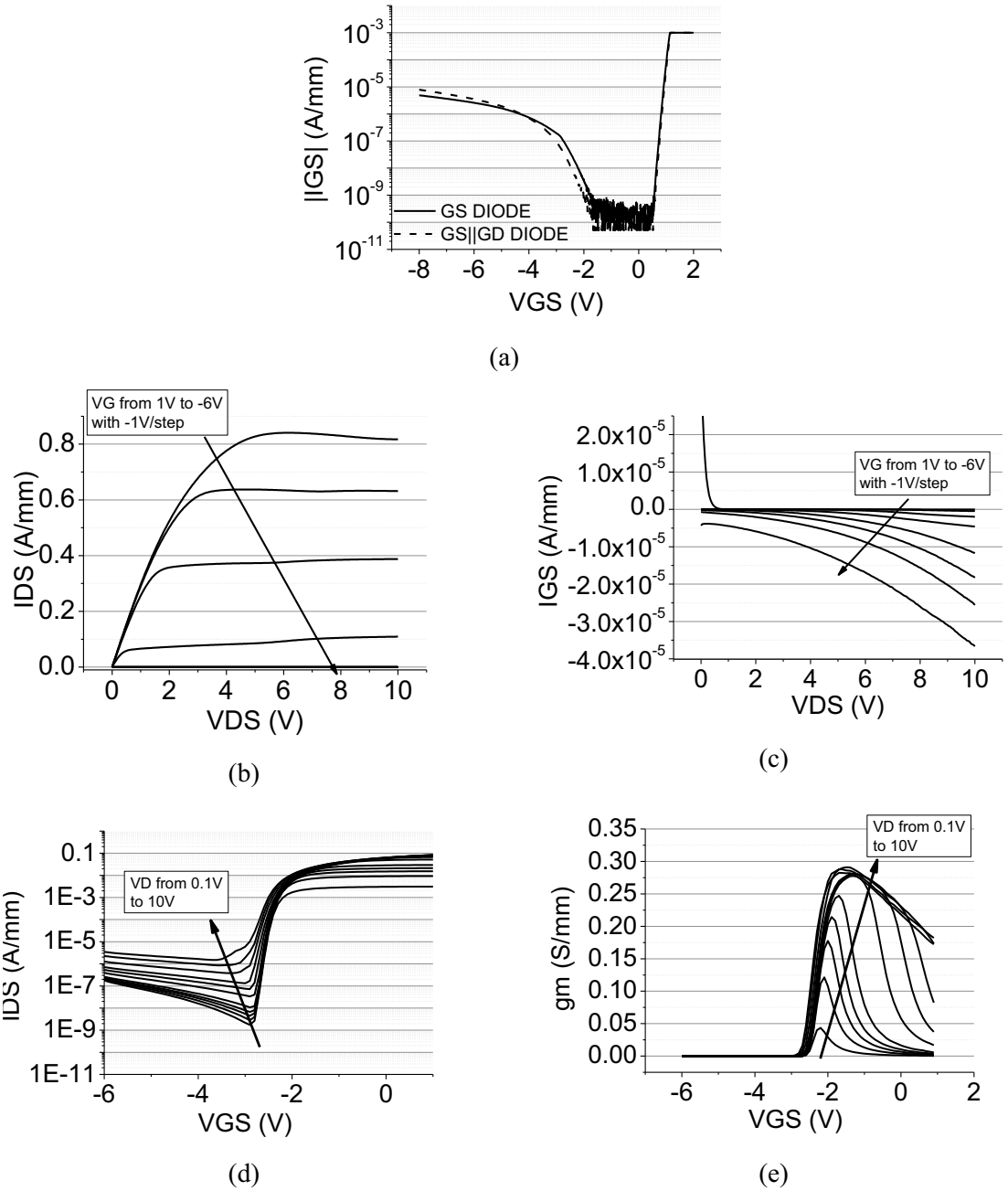


Figure 5.19: DC characterization in a AlGaN/GaN HEMT – sample B: (a) GS diode, (b) IDVD and (c) IGVD curve, (d) transcharacteristic, (e) transconductance

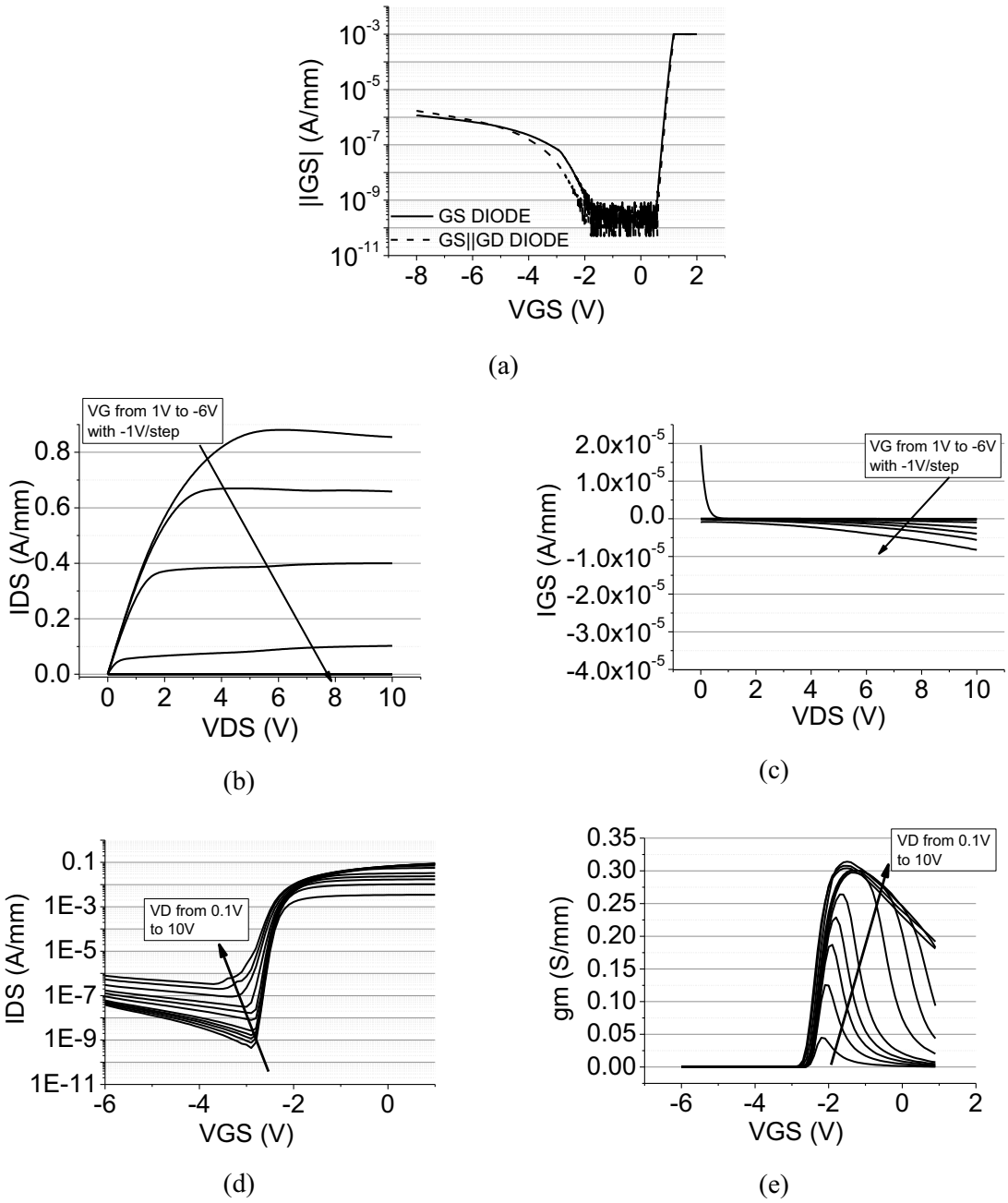


Figure 5.20: DC characterization in a AlGaN/GaN HEMT – sample C: (a) GS diode, (b) IDVD and (c) IGVD curve, (d) transcharacteristic, (e) transconductance

Fluorine effects

When a negative voltage is applied to all the devices a threshold voltage negative shift is reported. No further parameter faces degradation or variation, except for the drain current measured in ON state which is directly influenced by the threshold voltage trend. This threshold voltage negative shift saturates with time when a negative voltage is applied. Analysis carried out on devices developed with different process, i.e. with and with no etching, let us make the hypothesis that this effect is not due to device degradation but to fluorine presence in the device.

We can hypothesize that fluorine used for the etching during the process is trapped in the AlGaN barrier layer. Trapped fluorine can belong to two main typologies: (i) fluorine ions with interstitial position which represents a fixed negative charge (F_i^-); the consequence is a threshold voltage positive shift; (ii) fluorine is characterized by substitutional position within the nitrogen atoms inside the lattice crystal (F_N^{2+}); in this case the fluorine is a donor impurity and it can lead to a very slow trap. When a negative bias is applied to the gate, fluorine interstitial ions are "no more ionized" as a consequence of hot electrons due to leakage current. The fluorine ion, once has shown instability, is absorbed by the crystal lattice in correspondence of nitrogen vacancies, i.e. becoming F_N^{2+}, thus leading to a threshold voltage negative shift.

5.4 Trapping effects due to Fe doping in the buffer layer

In this chapter it is reported an extensive analysis of the impact of Fe doping quantity in the buffer layer on trapping behaviour. Iron atoms, similarly to carbon ones, are widely used in GaN HEMT technology to dope the buffer layer, thus providing significant buffer isolation, according to intrinsic n-type doping of GaN. This approach is essential to confine the carriers and provide for reduction of both buffer leakage current and punch-through components.

Trapping behaviour as a function of Fe doping quantity is studied by means of pulsed measurements and drain current transients. Analysis has been carried out on AlGaN/GaN devices with analogous barrier layer thickness and Al percentage but with different Fe doping in the buffer layer. Results are consistent with preliminary investigations reported in literature which associate that the use of Fe-doping leads to the presence of a trap level located 0.57-0.7 eV below the conduction band energy; previous results reported in literature concerning Fe doping effects consider a trap evaluation detected by $g_m(f)$ [77] or dynamic Ron measurements [83]. Trapping evaluation firstly demonstrates that the use of Fe-doping induces a measurable current collapse, which is related to the presence of a trap (T1) located in the buffer, according to the significant increase of current collapse with Fe-concentration in the buffer.

In the cases studied the activation energy of the trap detected is E_c-0.63 eV. We can hypothesize that this trap, which influences significantly the current collapse value, is not directly due to the iron doping. The trap is due to an intrinsic defect in the buffer layer characteristic of GaN, consistently with several works reported in literature which detect a similar trap even if with no buffer doped. However Trap concentration strongly depends on buffer doping quantity, according to results obtained. Drain current transient measurements carried out with several trapping phase time suggest that this trap behaves as a point defect clustering around dislocations

5.4.1 Experimental details

All the devices have been analysed both with pulsed analysis and drain current transients. Further information about measurement setup has been provided in 5.1.3.

Pulsed analysis has been evaluated by means of double pulse measurements. Four quiescent bias point are considered, from an initial condition characterized by V_{GSQ}= V_{DSQ} = 0 V, where no trapping effects are noticed, to a final state with V_{GSQ} = -6 V, V_{DSQ} = 20 V, to induce significant trapping mechanism without degrading the device. In all the four quiescent bias point both the I_DV_D and the I_DV_G curves are defined. I_DV_D is measured for V_{GS}=0V by sweeping the V_{DS} from 0 to 10V, while I_DV_G is evaluated for V_{DS}=0V by sweeping the V_{GS} from -5V to 0V. In both the cases a pulse width of 1 μs and a duty cycle of 1% are imposed in order not to induce significant self-heating or promote de-trapping effects. The measurement is taken between 840ns and 885ns after the pulse is applied. Current collapse is calculated at V_{DS}=3V, V_{GS}=0V in order to consider the drain current variation at high dissipation condition in the knee voltage zone, where the maximum degradation has been noticed. Dynamical V_{TH} is evaluated in a consistent V_{DS} bias point (i.e. V_{DS} = 3 V).

Current transients have been measured in a time range between 1 μs and 100 s. In order to carry out a consisted analysis with double pulse analysis the device is biased in OFF state during the trapping phase at V_{GSQ} = -6 V, V_{DSQ} = 20 V and in ON state during the de-trapping phase at V_{DS}=3V, V_{GS}=0V. In both the states the device is biased for 100s. Several ambient temperatures, from T=30°C to T=80°C have been imposed with the use of a thermal chuck in order to define traps activation energy and cross section. Ambient temperatures imposed have been chosen on the basis of traps time constants. Although stretched exponential and the peak of the derivative function provide for consistent results, in this chapter only the evaluation calculated through the analysis of the peak of the derivative function has been reported. Due to the drain current transient trend it was not possible to use the multi exponential function to extrapolate reliable data. Drain current transients have been carried out with the same time range and bias applied, by varying the filling time pulse, in order to investigate whether traps are due to point or line defects. Trap amplitude is studied with different trapping phase time from 10^{-5} to 10^{2}.

5.4.2 Experimental results

Pulsed analysis

Pulsed I_DV_D characterization indicates that the devices suffer from a significant current collapse. Although with different intensity, a similar trend is reported in all the samples considered; therefore only curves corresponding to sample D will be reported. Figure 5.21 shows that the current collapse is more evident in the saturation zone (V_{DS}>2 V), rather than in the linear regime.

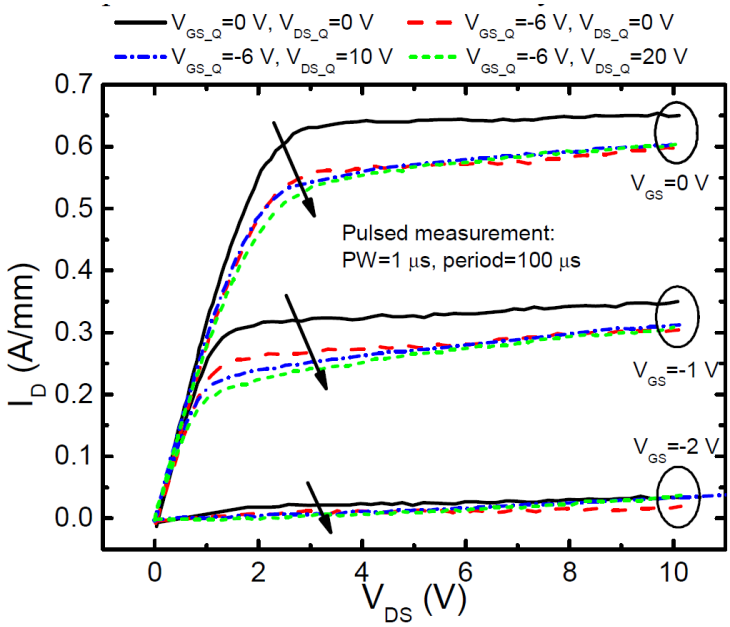


Figure 5.21: pulsed I_D-V_D characteristics measured starting from different quiescent bias points (V_{GSQ}, V_{DSQ}) on sample D

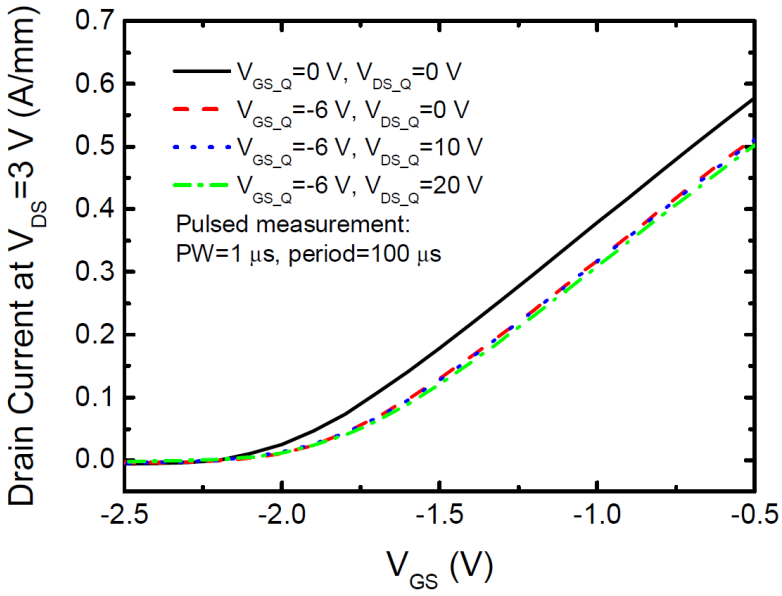


Figure 5.22: pulsed I_D-V_G characteristics measured starting from different quiescent bias points (V_{GSQ}, V_{DSQ}) on sample D

Furthermore, it is possible to notice that current collapse strongly depend on the quiescent bias point used for the pulsed measurements. The trend as a function of the bias applied during the quiescent bias point indicates that a strong current collapse is measured when a only a negative bias is applied to the gate, thus indicating that the current collapse strongly depends on the quiescent bias applied to the gate while drain voltage has a minor influence on current collapse. Therefore we can suppose that leakage current has a relevant impact on the recoverable decrease of drain current due to trapping effects. The lower difference in current

collapse measured between the second and the fourth quiescent bias point, thus increasing the gate drain voltage during the trapping phase and keeping constant the gate source voltage, suggests that the electric field variation induces an increase in the trapping phenomena, but not as the gate leakage current (Figure 5.23). This is confirmed by pulsed I_DV_G measurements reported in Figure 5.22, which indicate that current collapse is mainly due to a variation of the dynamical threshold voltage shift with no significant variation of the on resistance measured in liner region. This aspect indicates that trap levels filled by the quiescent bias point applied are mostly located under the gate of the devices rather than in the access region.

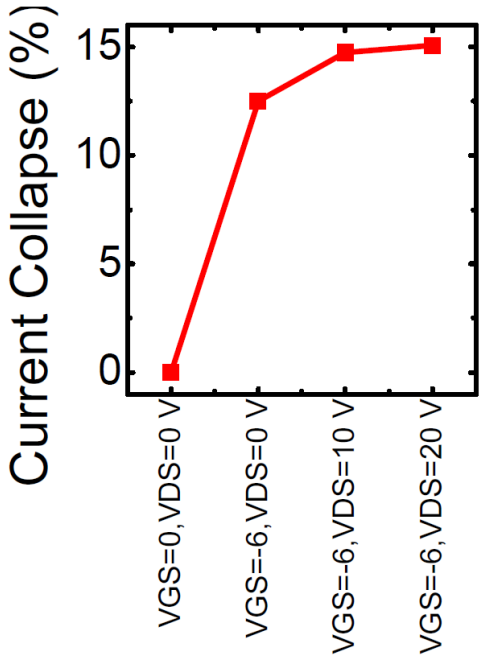


Figure 5.23: dependence of current collapse on the quiescent bias point used for the pulsed measurements

Drain current transient

The properties of the trap levels responsible for current collapse are investigated by Drain Current Transient (DCT) measurements. Figure 5.24 reports an example of drain current transient measured on sample D. The current transient measured at T=40°C in a fresh device reports the presence of two traps, labelled T1 and T2. They are characterized, respectively, by a time constant of 3.2ms and 0.25s. From the analysis of the peak of the drain current derivative curve, shown in Figure 5.25 as a function of ambient temperature imposed, it is possible to define the Arrhenius plot and calculate traps corresponding activation energy and cross section. Both traps are thermally activated with a corresponding t E_a=0.56eV and 0.74eV and a cross section of $4.23\text{x}10^{-15}$ and $4.14\text{x}10^{-14}$, respectively.

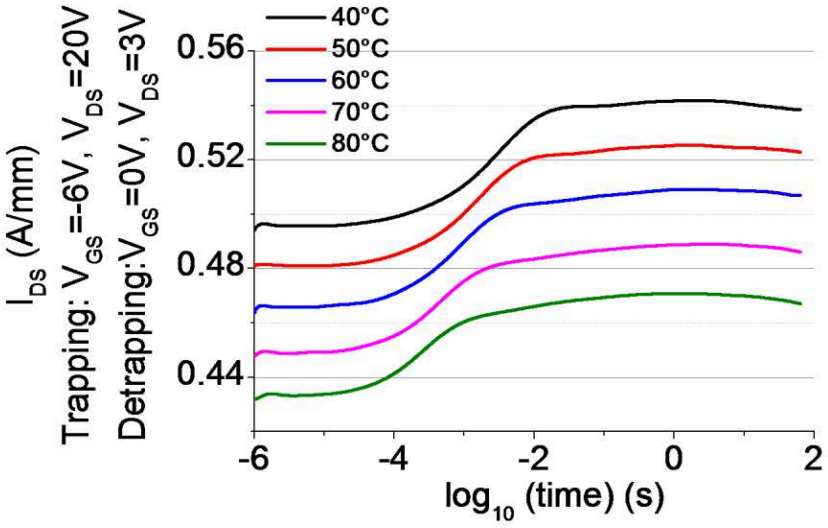


Figure 5.24: drain current transient measured on a fresh sample D with several ambient temperatures imposed from T=40°C to T=80°C

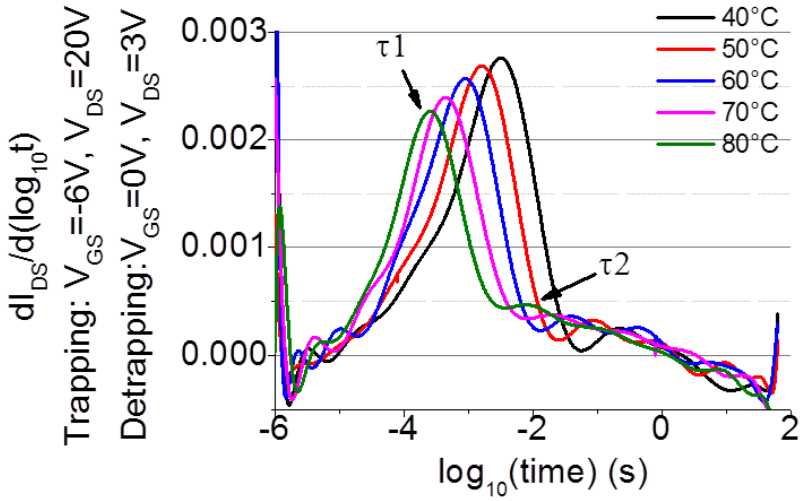


Figure 5.25: $\partial I_{DS}/\partial(\log_{10}t)$ measured in a fresh sample D with several ambient temperatures imposed from T=40°C to T=80°C

These values are evaluated with no temperature correction, thus supposing that no self-heating characterize the devices during the measurement. In truth, if an effective junction temperature is considered and corrected by adding to the ambient temperature the junction temperature measured through dissipation power and thermal resistance, an activation energy of $0{,}66 \pm 0{,}02eV$ and of $0{,}82 \pm 0{,}06eV$ characterize, respectively, trap 1 and trap 2 when a fresh sample D is considered (Figure 5.26).

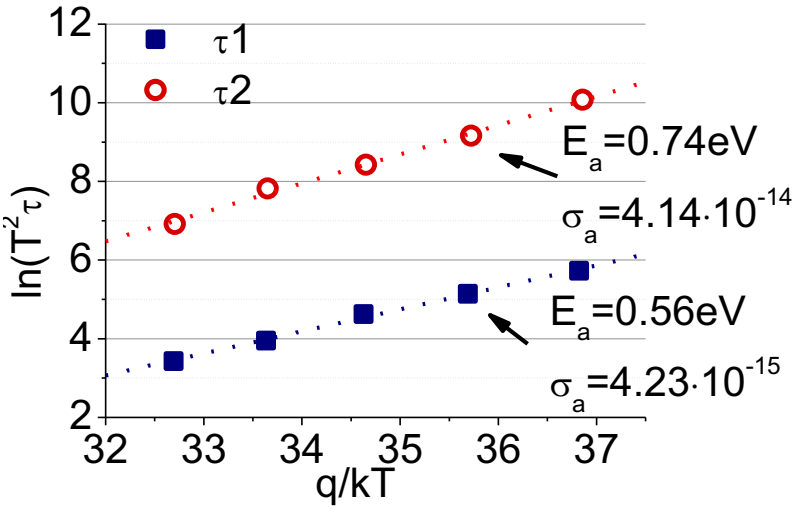


Figure 5.26: Activation energy and cross section of T1 and T2 measured on a fresh sample D

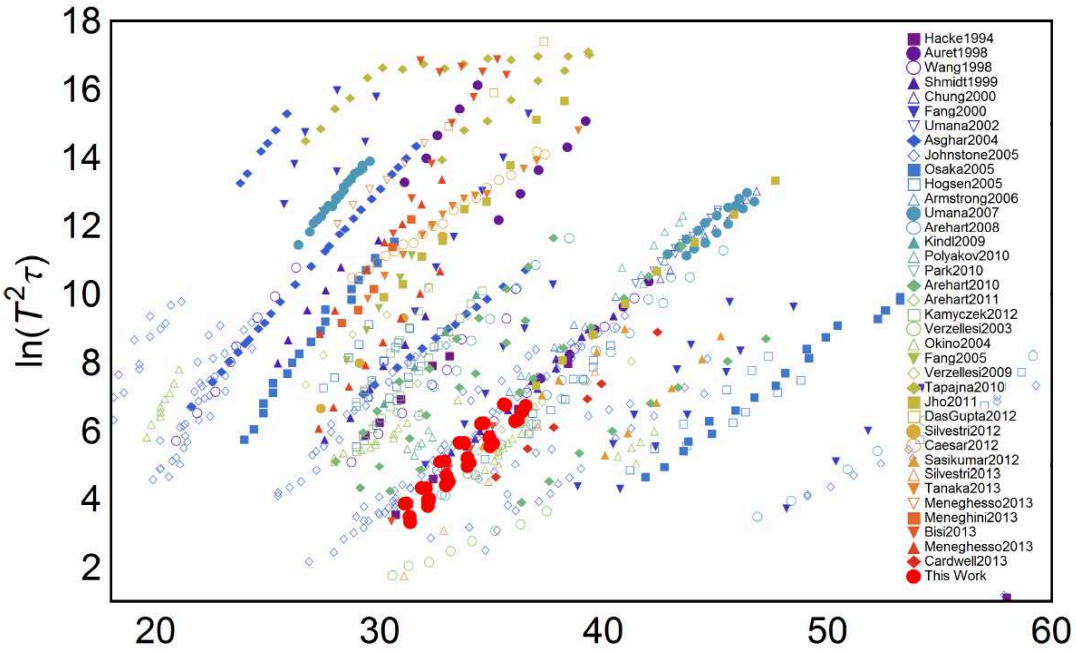


Figure 5.27: Comparison of traps activation energy with further works reported in literature

Prior work has been reported on traps characterized by a E_a of 0.56eV-0.58eV and cross sections in a range between $1\cdot10^{-15}$-$1\cdot10^{-16}$. Arehart et al. reported a detailed analysis [84], [85] of a thermally activated trap characterized by a E_a of 0.57eV and a σ_a of $6\cdot10^{-15}$ by means of constant drain current DLTS. On the basis of drain lag and CI_D-DLTS a speculation on the location of the trap in the drain acces region [84] and in AlGaN surface [85] is proposed, respectively. Furthermore, Sin et al. [86] studied with DLTS and HR-TEM techniques traps and defects in pre and post stressed AlGaN/GaN HEMT. Two traps, characterized by a E_a of 0.5eV and 0.7eV have been attributed to point defects in the AlGaN barrier layer [86]. However, from

the comparison of several devices characterized by a structure similar to the ones analysed except for a different GaN buffer layer thickness and different Fe-doping quantities, we can speculate that T1 should be probably located in the buffer layer. A significant correlation has been established with results proposed by [77], [83]. In these works a detailed analysis of traps behaviour in devices characterized by a Fe doped buffer layer has been proposed, both measuring the trapping behaviour with $g_m(f)$ and dynamic R_{ON} evaluation

Figure 5.28 reports the time-constant spectrum extrapolated from DCT measurements on the wafers with increasing Fe doping. Results demonstrate that current collapse is mostly due to the presence of a dominant trap level (labelled as T1 in the following); furthermore a second trap (labelled T2) characterizes all the devices. Trap T1 is supposed to be located in the buffer layer. Two main reasons suggest this hypothesis: (i) current collapse mostly originates from defects located under the gate, according to results extrapolated with pulsed measurements; (ii) the peak amplitude of T1 is directly related to the amount of Fe in the buffer.

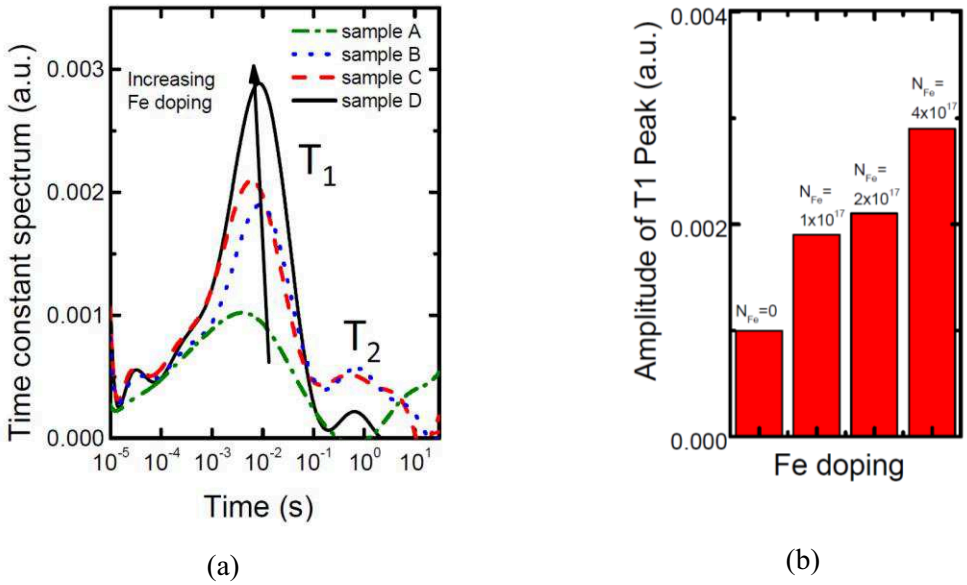


Figure 5.28: (a) time constant spectra extrapolated from DCT measurements on the wafers with increasing Fe doping; (b) dependence of the signal associated to trap T_1 on the iron concentration in the buffer

If the current collapse as a function of Fe quantity in the buffer layer is considered similar results are obtained. In this case we must take into account that the current collapse value is defined by both T1 and T2. Therefore, although T1 amplitude depends on Fe doping quantity, T2 is not necessarily located in the buffer layer and does not have a strong dependence on Fe doping. Indeed, as it is possible to notice in Figure 5.28a, the peak of T2 is higher in sample B and C than in sample A. Current collapse analysis shows that a similar current collapse value is noticed in Fe doped devices while a lower current collapse is noticed in devices with no Fe doping. Analysis for four representative devices is shown in Figure 5.29

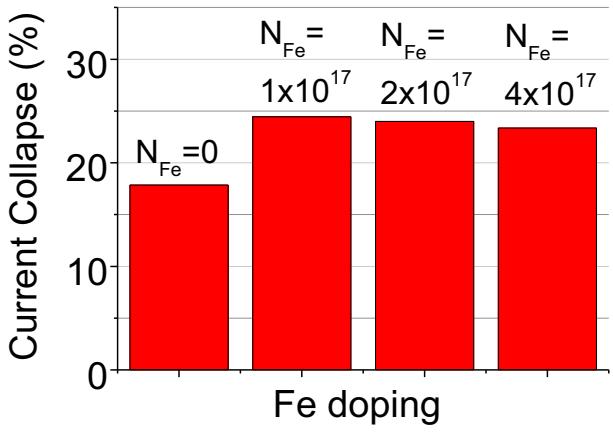


Figure 5.29: dependence of the current collapse measured at ambient temperature T=30°C on the iron concentration in the buffer

The activation energy corresponding to T1 does not vary in samples with Fe doping on the buffer layer, as demonstrated by Arrhenius plot in Figure 5.30. In all the cases measured trap T1 is thermally activated with an activation energy of 0.63 eV and $2.3 \cdot 10^{-14}$ cm^{-2}. In this case, differently from the activation energy reported in Figure 5.26, the Arrhenius plot has been corrected by considering also self-heating effects. On the contrary in devices with no Fe doping (sample A) T1 is thermally activated with a much lower activation energy (0.20 eV), thus confirming the possible location of T1 in the buffer layer.

Consistently with the assumption that T2 is not located in the buffer layer but probably in the barrier layer or at the hetero-interface, the activation energy does not change on the basis of the presence of iron doping in the buffer layer. In all the samples measured, except for sample D, an activation energy of 0.6-0.7eV is reported. Sample D is characterized by a slight higher activation energy (0.84eV). However, considering the Arrhenius plot reported in Figure 5.31 and evaluating the activation energy measured in all the samples with no temperature correction, we can make the hypothesis that there is no correlation between the iron doping in the buffer layer and the trap T2 activation energy. Indeed, if no temperature correction is considered, no significant difference is established through the comparison of the four different samples analysed.

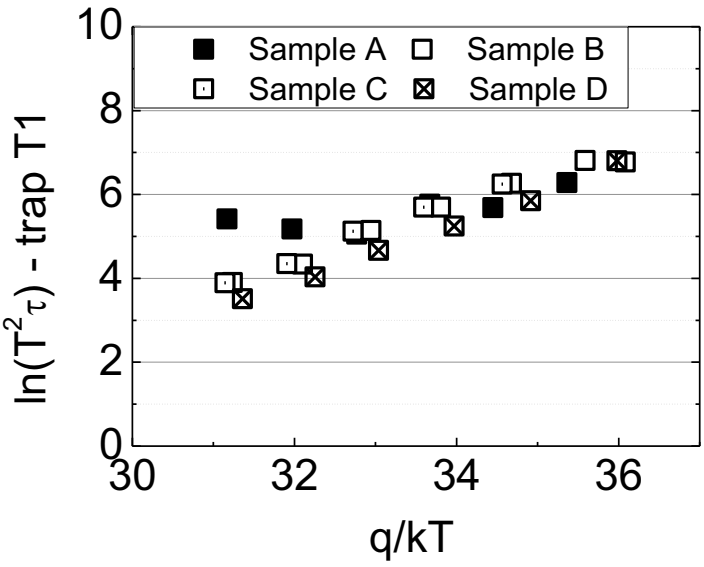


Figure 5.30: Comparison of the trap T1 activation energy (with temperature correction) measured in different samples

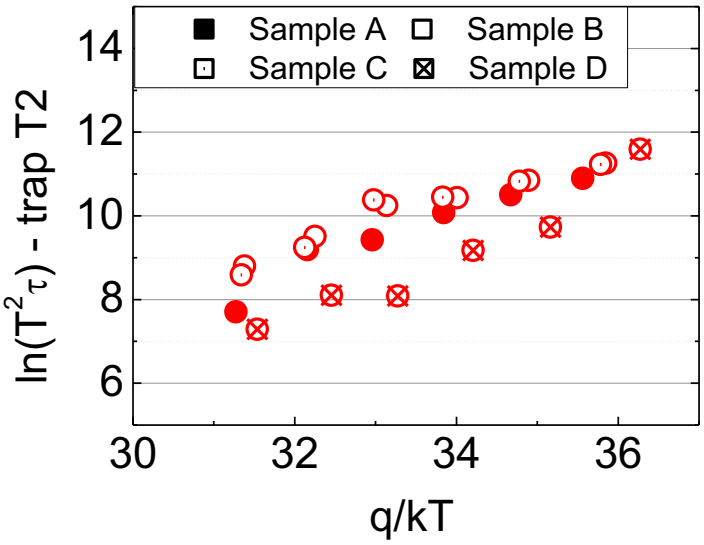


Figure 5.31: Comparison of the trap T2 activation energy (with temperature correction) measured in different samples

Filling pulse analysis

According to the explanation provided in 5.1.3, drain current transient evaluated with a different filling time, i.e. keeping the device in the trapping phase for a different amount of time without changing the de-trapping time imposed, can provide for significant information about trap nature. Investigation can be done on the basis of both the function which defines the

occupancy of non-interacting point defect with filling time and the function which describe the trend of the concentration of electrons in linearly arranged defects.

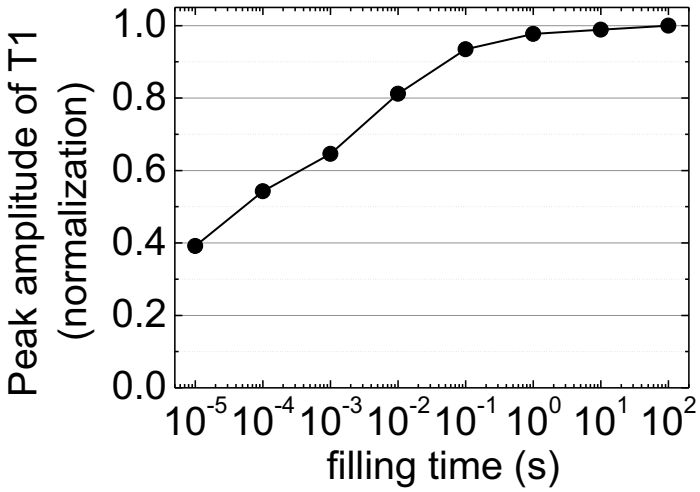


Figure 5.32: dependence of the amplitude of the signal of trap T_1 on the duration of the pulse used to fill the traps

The results measured on sample D and reported in Figure 5.32 demonstrate that the amplitude of the trap T1 increases with the trapping time following a logarithmic trend in a range between 10^{-5} and 10^{0}. This trend suggests that traps are related not linearly to point defects but to linearly arranged defects, such as point-defects clustering around dislocations. No variation of the time constant is shown (Figure 5.34). Similar considerations can be done if trap T2 is considered (Figure 5.34). the slight variation for lowest filling time when trap T2 is considered can be ascribed to a measurement inaccuracy. Indeed a minimum ratio between the time imposed during trapping and de-trapping time must be used due to an issue defined by the amplitude waveform generator. No variation of the rime constant is stated both if T1 and T2 is taken into account (Figure 5.33).

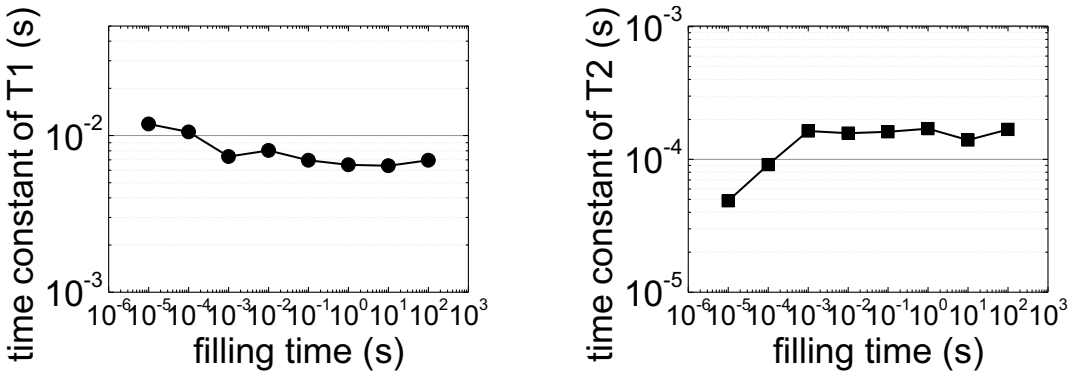


Figure 5.33: time constants corresponding to (i) trap T1 and (ii) trap T2

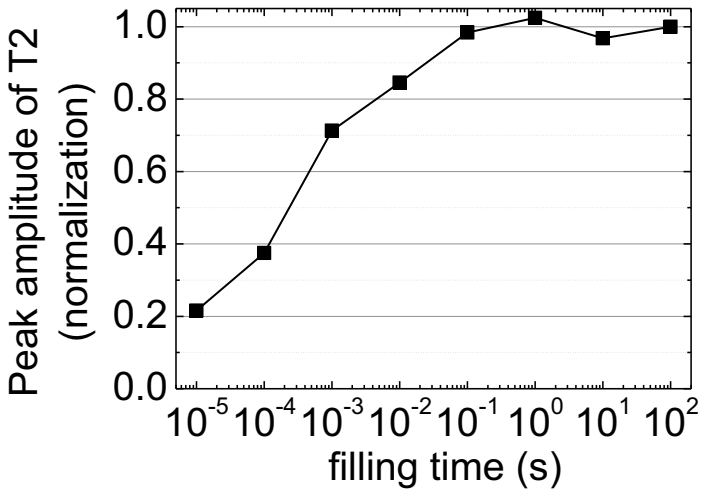


Figure 5.34: dependence of the amplitude of the signal of trap T_2 on the duration of the pulse used to fill the traps

5.5 The stress waltz: correlation between trapping effects and degradation phenomena

One of the most critical aspects which influences the reliability of GaN HEMTs is the so called current collapse, which has been largely explained in 5.1.3. Indeed, the worsening of both RF and power performances is mainly induced by trapping phenomena.

Recent studies reported in literature demonstrate that current collapse, and thus traps impact on device, can be strongly influenced by OFF state stress. Joh et al. [87] analyses the trend of current collapse and trap amplitude as a function of the stress, while Sasikumar et al. [88] compares the trapping behaviour of a device before and after a stress in semi-on conditions.

In this chapter the correlation between trapping effects and degradation phenomena induced by a reverse bias step stress is studied, thus defining the relationship between electrical parameters, such as diode and transistor gate leakage current, hot spots intensity revealed by emission microscopy and trapping behaviour, both in terms of quantitative and qualitative analysis measured with pulsed characterization and drain current transients, respectively.

Experimental data indicate that a device submitted to a reverse bias step stress, beyond a certain critical voltage which depends on the stress time during each step, shows an increase of leakage gate current which is strongly correlated with hot spots detected with electron microscopy. Beyond the so called critical voltage a strong correlation is shown also with the current collapse measured at high dissipation condition in the knee voltage zone. Consistent results are noticed in the increase of the amplitude of drain current transients, thus suggesting that no generation of new defective levels is reported but only the increase in the amplitude of current transients associated to pre-existing traps.

5.5.1 Measurement Details

A reverse bias step stress has been carried out by biasing the gate terminal for 120s with an increasing voltage at each step. Drain and source terminals are both grounded in order to stress both the GS and GD diodes; considering that L_{GD} and L_{GS} are different we must take into account that the test has been done on a not symmetrical device. The gate terminal is biased at an initial condition with V_G=-10V and increased with -5V step. The final condition imposed depends on the device degradation and robustness in order to reach device degradation avoiding

failure. In all the devices a maximum voltage between -80V and -90V has been applied to the gate terminal. Drain and gate current are measured during the stress in order to determine eventual degradation.

In order to define a correlation between different degradation phenomena at each step the device is fully characterized with: (i) DC measurement, (ii) pulsed characterization, (iii) drain current transients, (iv) light emission microscopy. Detailed information about pulsed analysis and drain current transients has been provided 5.1.3. The "stress waltz" is described in Figure 5.35

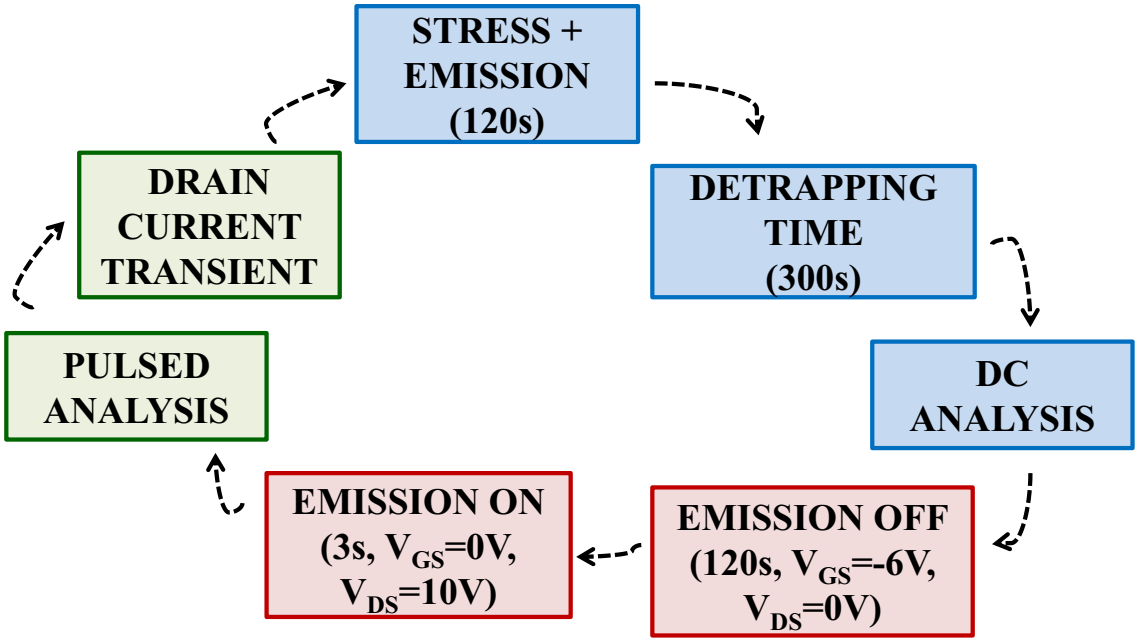


Figure 5.35: Reverse bias step stress measurement details

DC Characterization

Devices have been measured with a parameter analyser (Agilent 5263A) and biased with RF tips inside a Karl Suss probe station, in order to avoid oscillations. During the DC characterization the following curves have been evaluated: (i) GS and GS||GD diode current measured when forward and reverse bias are applied. It was not possible to measure GD diode as a consequence of the use of RF tips (ii) output I_DV_D and I_GV_D characteristic; (iii) I_DV_G and I_GV_G transcharacteristic; (iv) transconductance (g_mV_G).

Main parameters considered for the analysis are: (i) drain current measured in saturation zone (I_{DSS}) and knee voltage zone (respectively at V_{DS}=10V, V_{DS}=3V); drain current is considered both in high dissipation condition (V_{GS}=1V and V_{GS}=0V) and in OFF state (V_{GS}=-6V); (ii) max g_m reported in linear, knee voltage and saturation zone (V_{DS}=1V, V_{DS}=3V,

V_{DS}=10V respectively), (iii) transistor gate leakage current measured in OFF and ON state in saturation zone (V_{DS}= 10V and V_{GS}= -6V, V_{GS}=0V respectively), (iv) diode current measured with reverse and forward bias applied (V_{GS}= -6V, V_{GS}=1V respectively), (v) threshold voltage (V_{TH}), evaluated as the intercept with the x-axis of the curve tangent the I_DV_G curve measured in saturation zone.

Pulsed Characterization

Pulsed evaluation has been carried out with a custom setup, defining I_{DS} vs V_{DS} and I_{DS} vs V_{GS} curves by pulsing the drain (V_{DS}) and gate voltage (V_{GS}) from a quiescent bias point both at the gate and drain terminal (V_{GSQ} and V_{DSQ}), also called baseline or power dissipation level. Conditions similar to the ones imposed in preliminary measurements previously explained have been used. Therefore main conditions will be here only summarized: (i) four different power dissipation levels from a null power dissipation and trapping condition (V_{GSQ}=V_{DSQ}=0V) to a higher trapping quiescent bias point (V_{GSQ}=-6V, V_{DSQ}=20V), according to device degradation voltage; (ii) duty cycle of 1% with 1μs pulse width. Consistently with preliminary measurements current collapse is measured in the knee voltage zone at high dissipation condition while threshold voltage dynamical shift is considered in a consistent condition (i.e. V_{DS}=3V).

Emission microscopy

Light emission has been acquired with a high sensitivity silicon camera (IXON camera). During emission microscopy the device is biased both in OFF and ON state, respectively at V_{GS}=-10V, V_{DS}=0V and V_{GS}=0V, V_{DS}=10V. The emission is acquired for a different amount of time, in order not to reach camera saturation in a consistent way with current value during the conditions. An acquisition time of respectively 119s and 3s has been imposed. During the step stress the emission is acquired for 10s not to reach camera saturation.

Drain current transients

Drain current transients have been measured with a custom setup. Since the measurement setup has been already described in 5.1.3 main information will be just summarized. (i) Trapping and de-trapping phase have been imposed for 100s by biasing the device in OFF and ON condition, consistently with the last quiescent bias point imposed during pulsed measurements, where the highest current collapse was measured, and the bias condition to

evaluate current collapse. A bias corresponding to V_{GS}=0V,V_{DS}=3V and V_{GS}=-6V,V_{DS}=20V have been applied, respectively, during the de-trapping and trapping phase. (ii) drain current transient trend is evaluated in a range between 1µs and 100s. (iii) time constants are evaluated through the peak of the derivative function established through the drain current transient.(iv) to calculate activation energy several ambient temperatures have been imposed, from a minimum of 30°C to 80°C with 10°C step.

5.5.2 Analysis on device with Fe doped buffer layer

In this chapter a detailed analysis of a reverse bias step stress carried out on a sample D device, characterized by a Fe doped buffer layer, is reported. Preliminary measurements of the device measured have been explained in 5.3. A similar stress has been carried out on several devices with similar characteristics and structure. According to the strong reproducibility of results measured the analysis of only one sample is reported.

DC Characterization

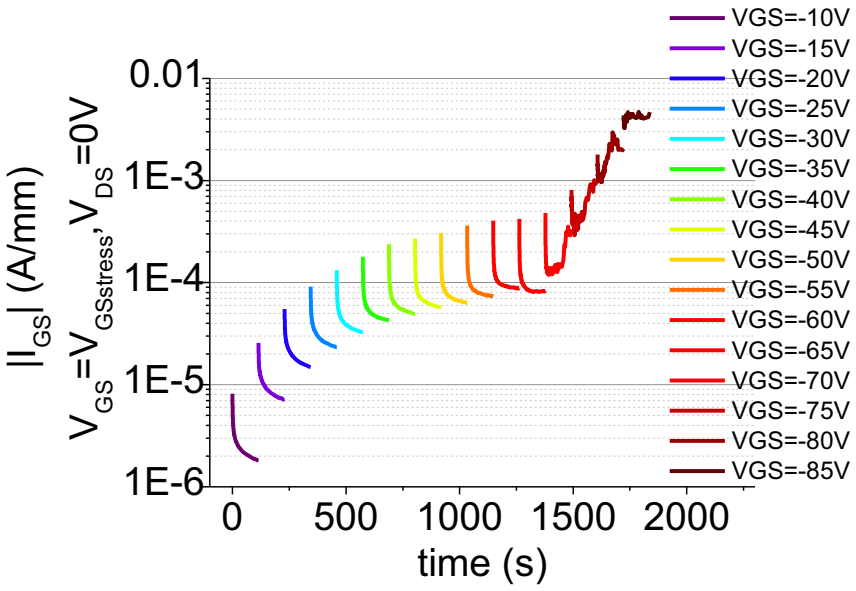


Figure 5.36: Transistor gate leakage current monitored during the execution of the step-stress experiment at V_{GS}=$V_{GSstress}$, V_{DS}=0V

The trend of the transistor DC gate current measured during the stress is shown in Figure 5.36, revealing that a not recoverable degradation occurs after a V_{GS}=-70V is imposed to the device. All the sample D tested show consistent results, with a variability in degradation of about ±10V. Hereafter the stress voltage corresponding to a not recoverable degradation will be called “critical voltage”; however it is important to highlight that this term is used improperly

since it strongly depends on the stress time imposed at each step and on the increasing voltage step.

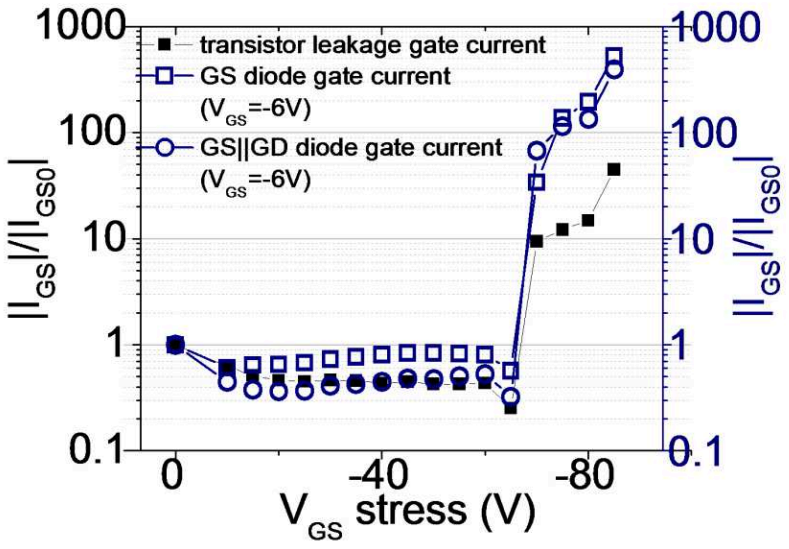


Figure 5.37: diode reverse current and transistor leakage gate current measured in OFF state during the stress

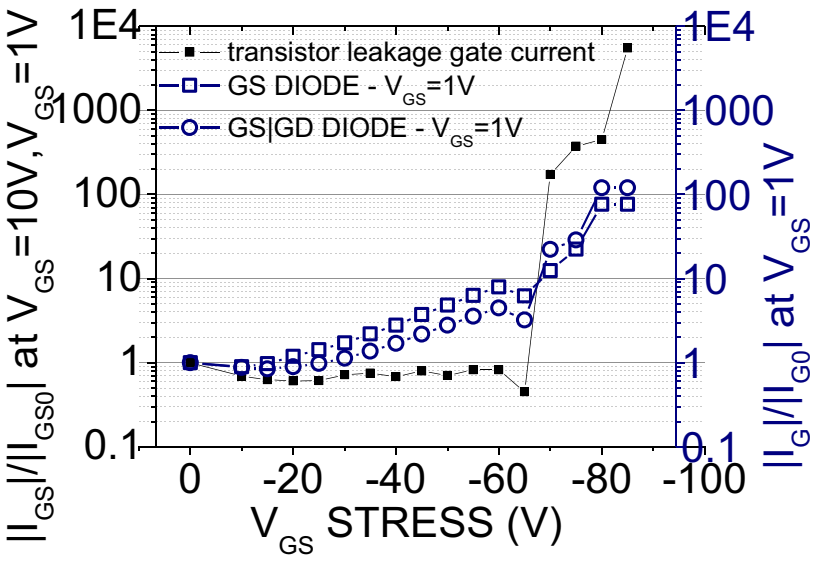


Figure 5.38: diode forward current and transistor leakage gate current measured in ON state during the stress

The not recoverable degradation is firstly described by the diode current measured both when reverse and forward bias is applied (Figure 5.37,Figure 5.38). An increase of more than two orders of magnitude is reported in the diodes reverse current. If a further stress is applied the diode reverse current shows an increase up to the end of the stress, reaching a variation of three orders of magnitude. The diode forward current reveals a degradation, showing an

increase of two orders of magnitude at the end of the stress. Differently from the diode reverse current, no sudden increase but a linear increase is noticed in the current measured when a forward bias is applied. Consistent results are noticed in the transistor gate leakage current. Leakage gate current measured in OFF state shows a variation of one order of magnitude after irreversible degradation, increased if a further stress is applied. A higher variation is shown in gate leakage current measured in ON condition; indeed a variation of two orders of magnitude is notice after the so called critical voltage. This variation increases up to four orders of magnitude if a further stress is imposed (Figure 5.40).

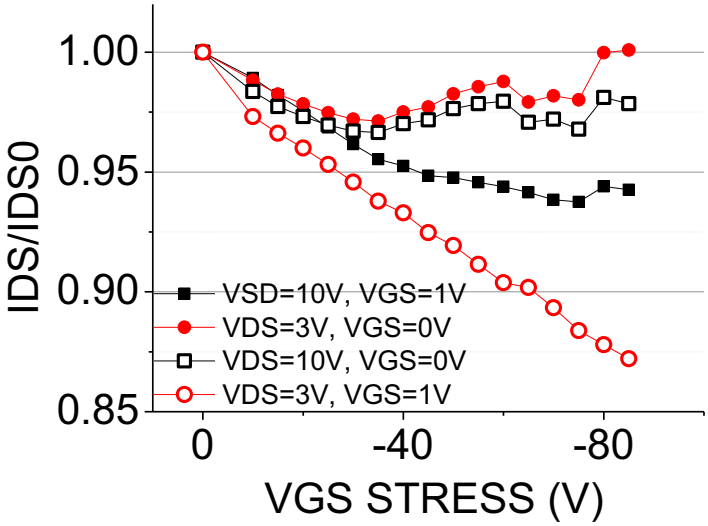


Figure 5.39: Drain current decrease monitored during the stress

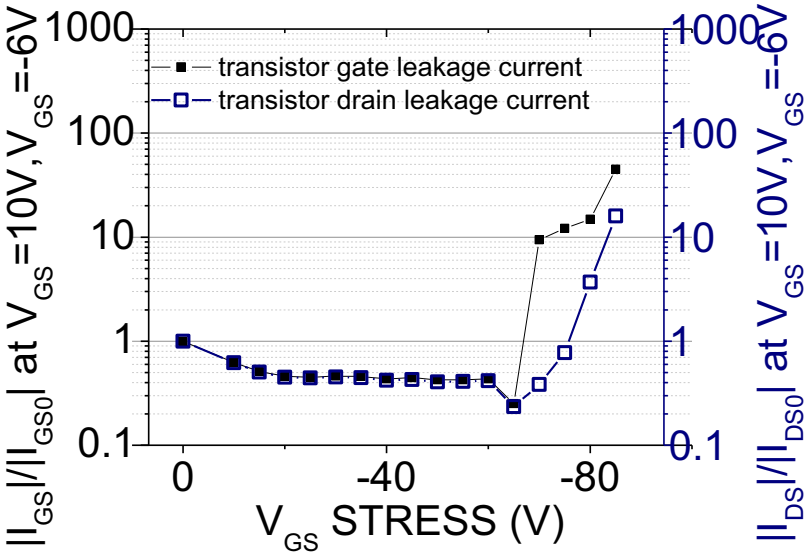


Figure 5.40: transistor leakage gate and drain current measured in OFF state during the stress

The drain current measured in saturation zone at high dissipation condition shows a decrease, both if considered at V_{GS}=0V or V_{GS}=1V. Analogous considerations can be done if the drain current is measured in knee voltage zone. When V_{GS}=1V is considered the decrease follows a monotonic trend; a decrease of less than 15% and of 5% is reached in knee voltage and saturation zones, respectively (Figure 5.39). When drain current is measured at V_{GS}=0V only a slight non monotonic variation is reported: after a decrease lower than 3% drain current keeps almost stable until the end of the stress. Consistently with the lower self-heating effects due to the lower dissipation condition no significant difference is established between the curve evaluated in knee voltage and saturation zone.

Transistor drain leakage current measured in OFF condition in the same condition used for gate leakage current shows a degradation after the critical voltage is applied. If a further stress is applied the variation continues increasing. Measurements carried out after a large amount of time demonstrate that the degradation is not recoverable. The trend is confirmed by the variation of the I_DV_G curve measured both in knee voltage and in saturation zone, at V_{DS}=3V and V_{DS}=10V respectively (Figure 5.41).

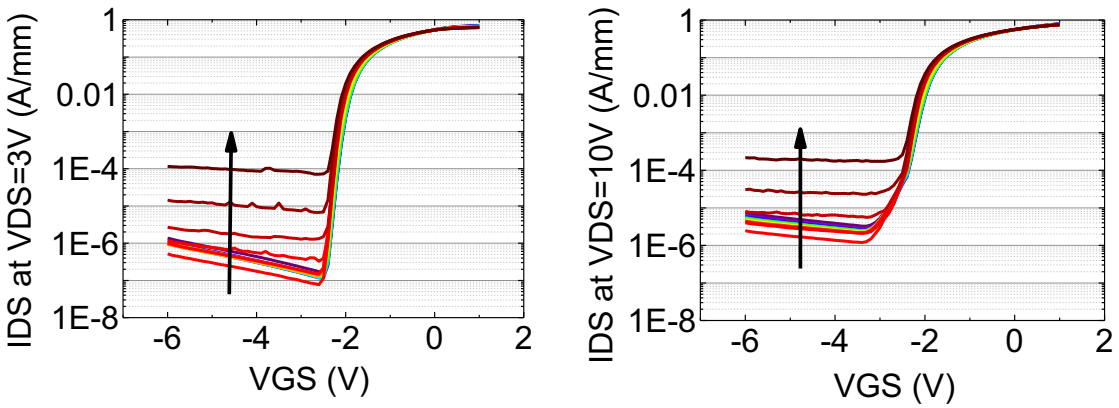


Figure 5.41: IDVG measured in the linear voltage (VDS=3V) and saturation region (VDS=10V)

Figure 5.41 states also that, during the stress, a not recoverable threshold voltage negative shift of almost 200mV is reported. Threshold voltage trend is explained in detail in Figure 5.42, both when knee voltage and saturation region are considered.

The analysis of the transconductance peak reports a monotonic decrease, independently from the region where it is considered. No significant difference is noticed if max g_m is evaluated in linear region (V_{DS}=1V), knee voltage (V_{DS}=3V) or saturation zone (V_{DS}=10V), as demonstrated by Figure 5.43. DC measurements carried out a large amount of time after the stress show that, differently from the transistor and diodes gate leakage current, drain current and max g_m decrease is partially due to degradation, partially to trapping during the OFF state

stress, despite a de-trapping time of 300s is waited between the end of the stress and DC characterization at each step.

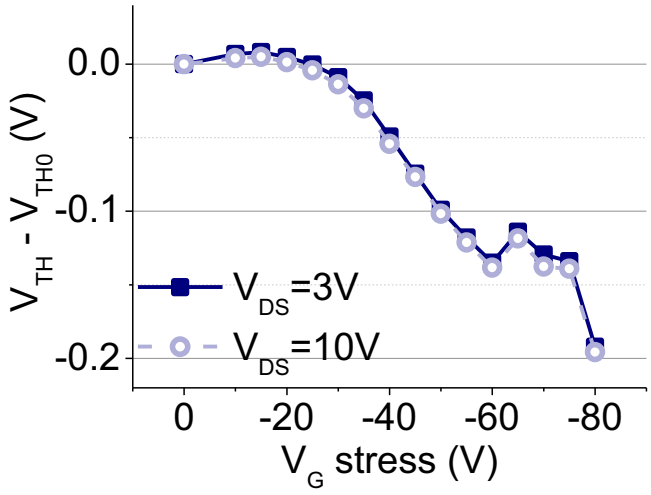


Figure 5.42: V_{TH} DC shift monitored during the stress

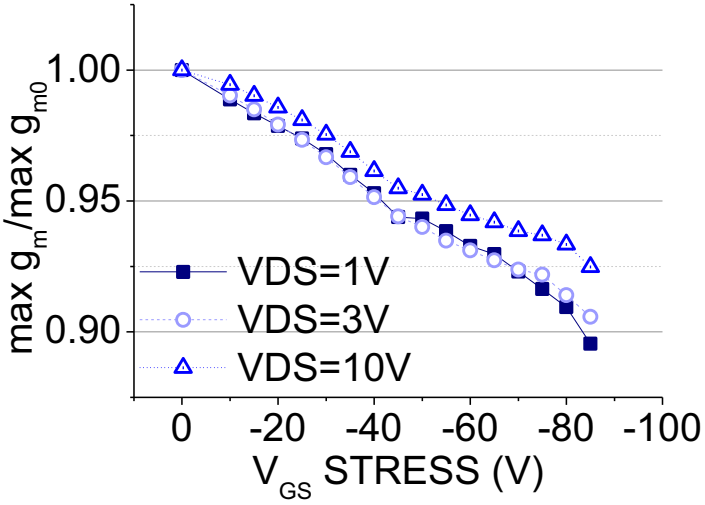


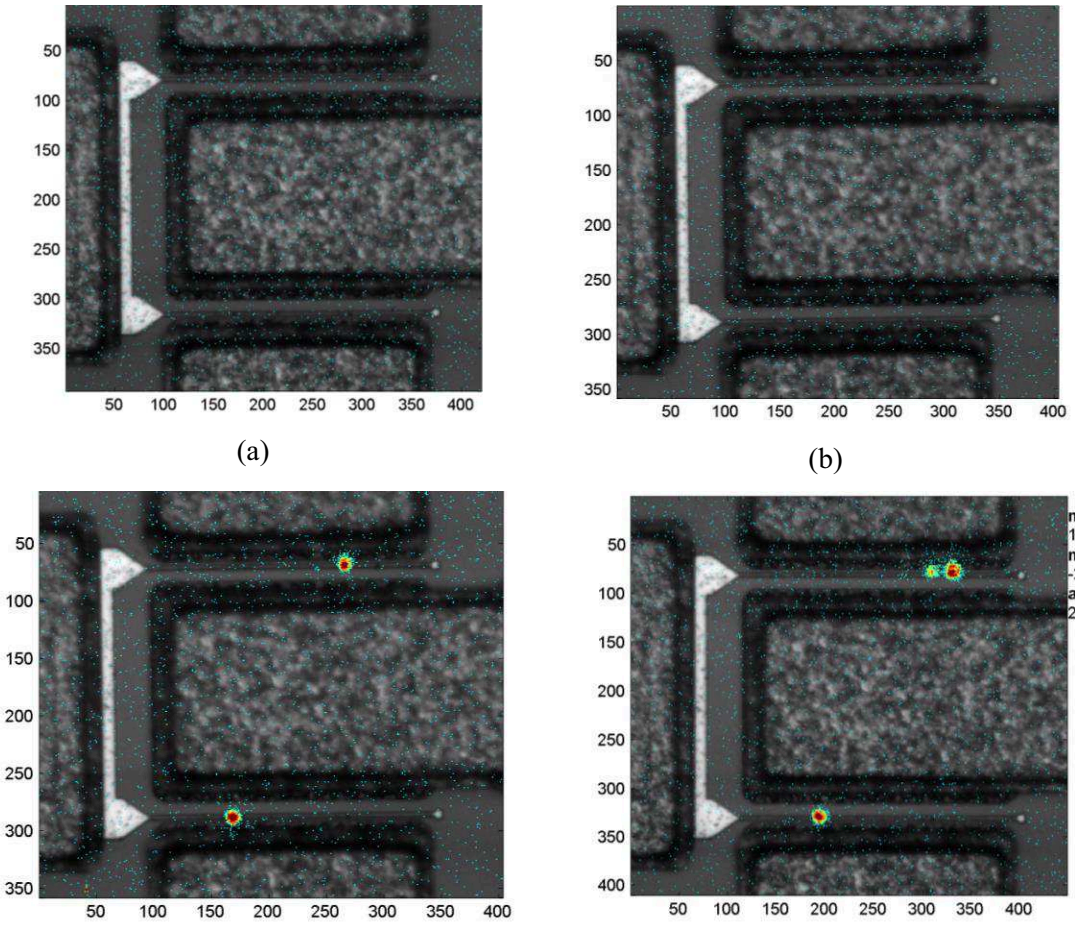
Figure 5.43: max g_m variation during the stress

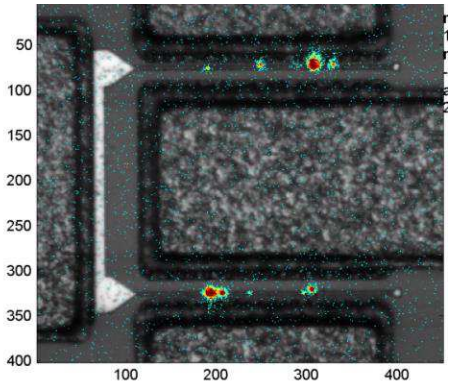
Emission Microscopy

Light emission has been measured in three different conditions: (i) during the stress and after each step in (ii) OFF or (iii) ON state conditions. Light emission measured during the stress (not here reported) is strongly correlated with the gate current measured during the stress. Unfortunately, as a consequence of the camera high resolution, saturation occurs for higher stress conditions, although a low emission time has been imposed during the stress.

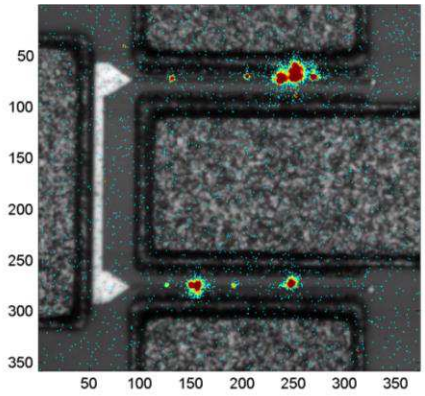
Emission measured in OFF state after each step shows that hot spots can be noticed only after V_{GS}=-70, in a consistent trend with the transistor gate current measured during OFF state emission (V_{GS}=-10V,V_{DS}=0V) and during DC analysis. Furthermore, if higher gate voltages are applied during the stress, an increasing of the hot spots intensity is reported, according to previous works reported in literature [89] and to electrical degradation mechanisms explained in 5.2. Figure 5.44 reports emission evaluated in OFF state in several steps: (i) fresh device, in order to show that no hot spot was shown before the stress, (ii) the step before not recoverable degradation; (iii) after not recoverable degradation, (iv) if further stress is applied after degradation; (v) at the last step of the stress.

Emission carried out at each step in ON condition is consistent with the variation of the drain current imposed. It is important to remember that the drain current decrease is partially due to trapping effects and partially to not recoverable degradation.





(e)



(f)

Figure 5.44: light emission carried out in OFF state after several steps: (a) before stress, (b) after V_{GS}=-65V, (c) after V_{GS}=-70V, (d) after V_{GS}=-75V, (e) after V_{GS}=-80V, (f) after V_{GS}=-85V

Pulsed analysis

To monitor trapping variation from a quantitative point of view current collapse has been evaluated during the stress. Degradation was found to induce an increase in the current collapse. The variation is more significant when high gate reverse voltages are applied to the gate. Furthermore, as it is possible to state in Figure 5.45, the variation is more prominent when a high gate drain voltage is applied.

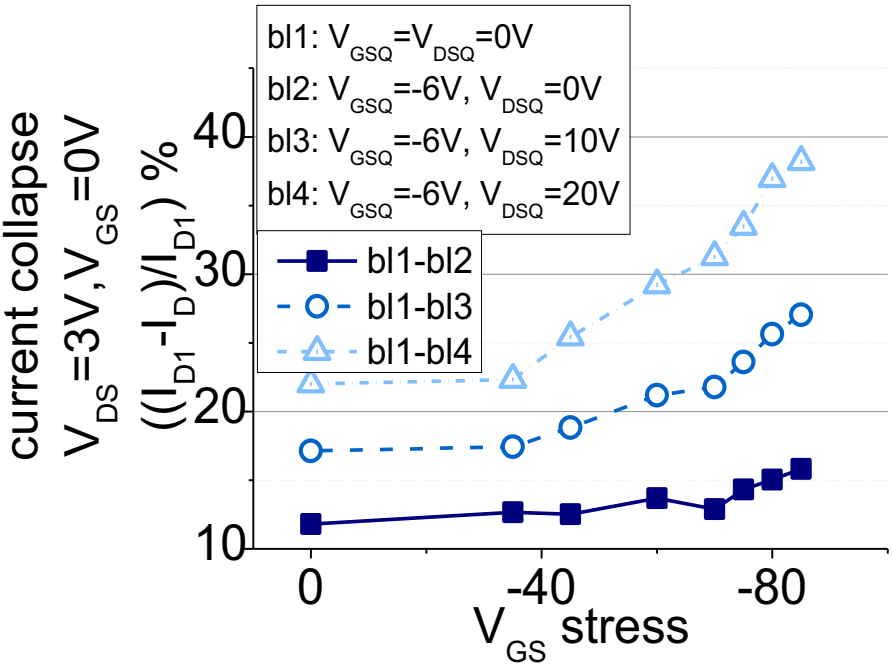


Figure 5.45: calculation of the current collapse monitored during the stress at several steps

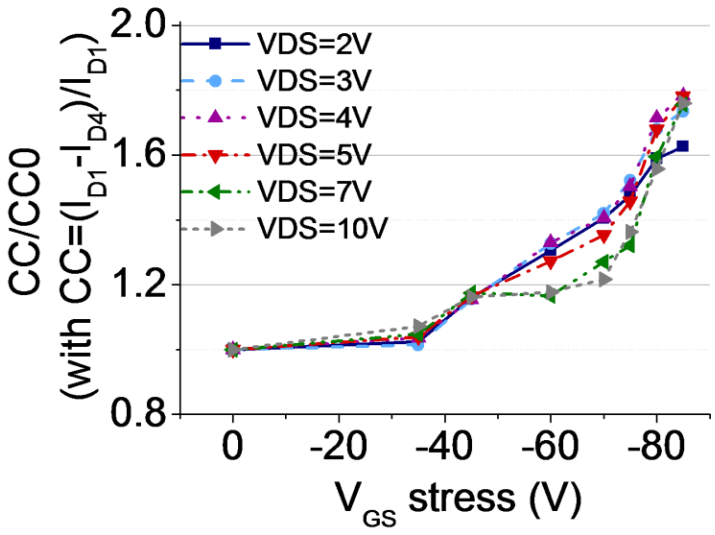


Figure 5.46: Current collapse evaluated during the stress at high dissipation conditions for several V_{DS} applied

When the first and the second quiescent bias point are considered, thus when drain voltage applied is null and only the trapping due to leakage current increase is considered, a slight variation from 12% to 15% is noticed during the stress. On the contrary, when the first and the fourth baseline are considered, the current collapse value duplicates by the end of the stress. A similar trend of trapping characteristics can be noticed if the current collapse is measured when a different V_{DS} is applied by pulsing from the same quiescent bias point (V_{DSQ}, V_{GSQ}). Figure 5.46 shows the current collapse evaluated during the stress between the fourth (V_{DSQ}=20V,V_{GSQ}=-6V) and the first baseline (V_{DSQ}=V_{GSQ}=0V) in high dissipation condition (i.e. V_{GS}=0V) for several V_{DS} applied.

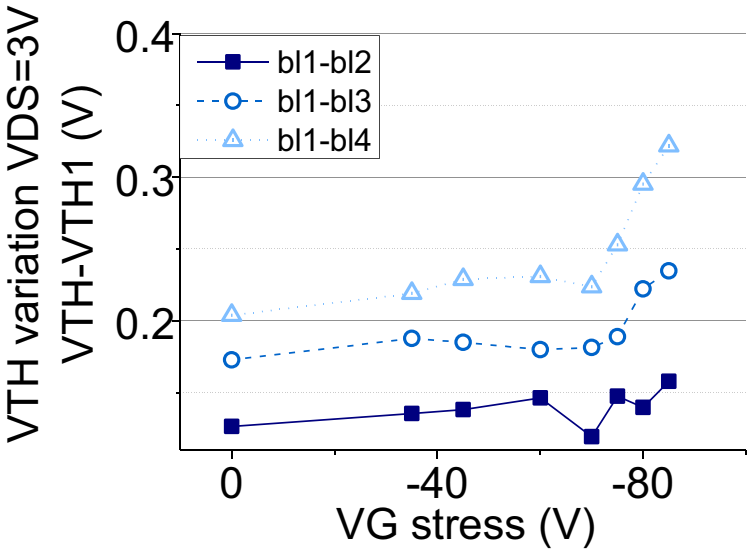


Figure 5.47: calculation of the VTH dynamical shift monitored during the stress at several steps

The analysis of the threshold voltage variation suggests that the current collapse increase is not mainly due to the threshold voltage dynamical shift, even if a significant dynamical shift is reported after degradation especially when a high drain gate voltage is imposed during the quiescent bias point (Figure 5.47).

Drain current transients

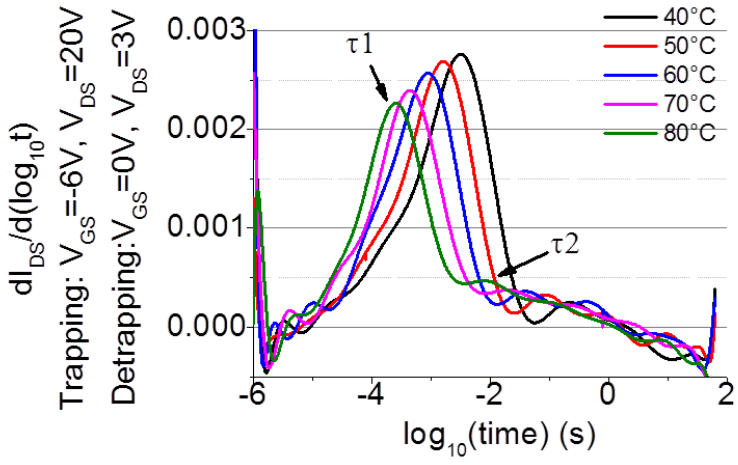


Figure 5.48: $\partial I_{DS}/\partial(\log_{10}t)$ variation during the stress – evaluation with ambient temperature T=40°C imposed

Transient analysis has been carried out before and after each step stress. However, in this case only the most significant curves are reported. It states that degradation does not induce generation of new defective levels but contributes to an increase of the signal associated two the pre-existing traps. Those traps have already been exhaustively described in the preliminary measurements 5.3. According to Figure 5.48, which shows the derivative function of the drain current transient it is possible to demonstrate that no new trap is detected.

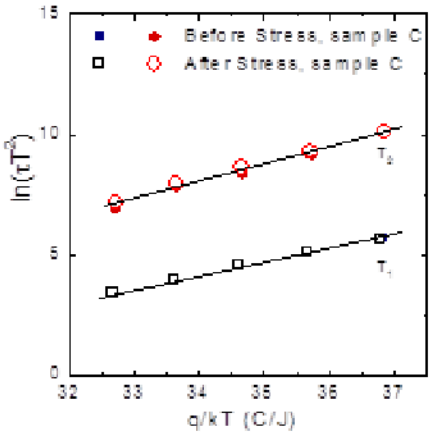


Figure 5.49: Arrhenius plot of the two trap levels of devices of series D (highest iron content) measured before and after stress.

Furthermore no change in the pre-existing traps time constant has been reported. the activation energy of the traps does not change after stress, both for T1 and T2 (±0.022eV and ±0.07eV, respectively). Detailed data are given in Figure 5.49.

T1 reveals an increase of 28%, varying from an initial amplitude of $2.76 \cdot 10^{-3}$ to a final one of $3.52 \cdot 10^{-3}$. T2 shows a variation of 173%, with an increase from $2.49 \cdot 10^{-4}$ to $6.80 \cdot 10^{-4}$. Traps amplitude variation is consistent with the increase of the current collapse (Figure 5.50). The variation of the drain current transient normalized to the value measured at t=100s is finally shown to confirm the results (Figure 5.51).

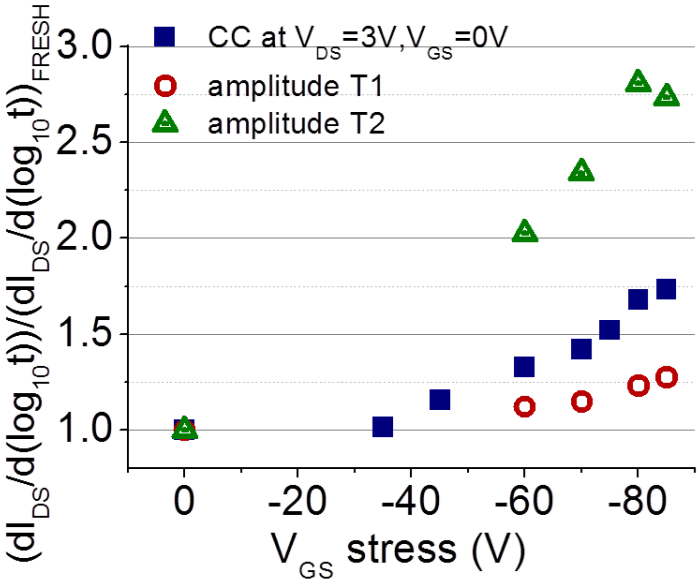


Figure 5.50: evaluation of traps T1 and T2 amplitude variation during the stress

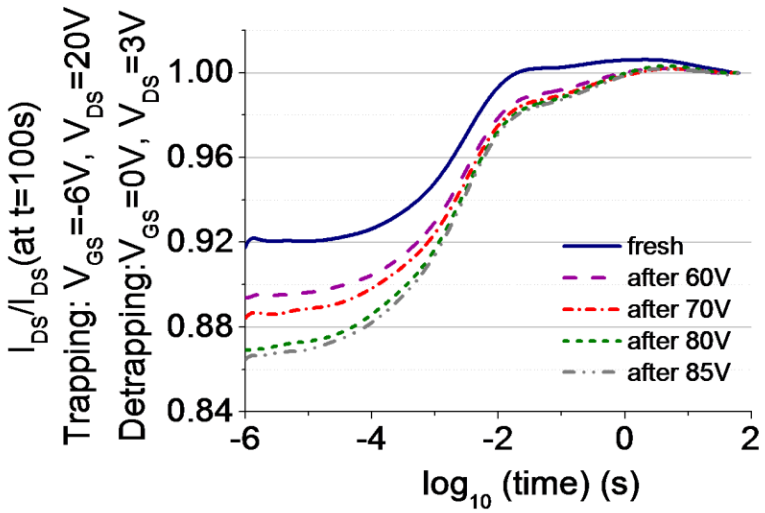


Figure 5.51: Drain current transient normalized to drain current measured at t=100s

Comparison of different degradation effects

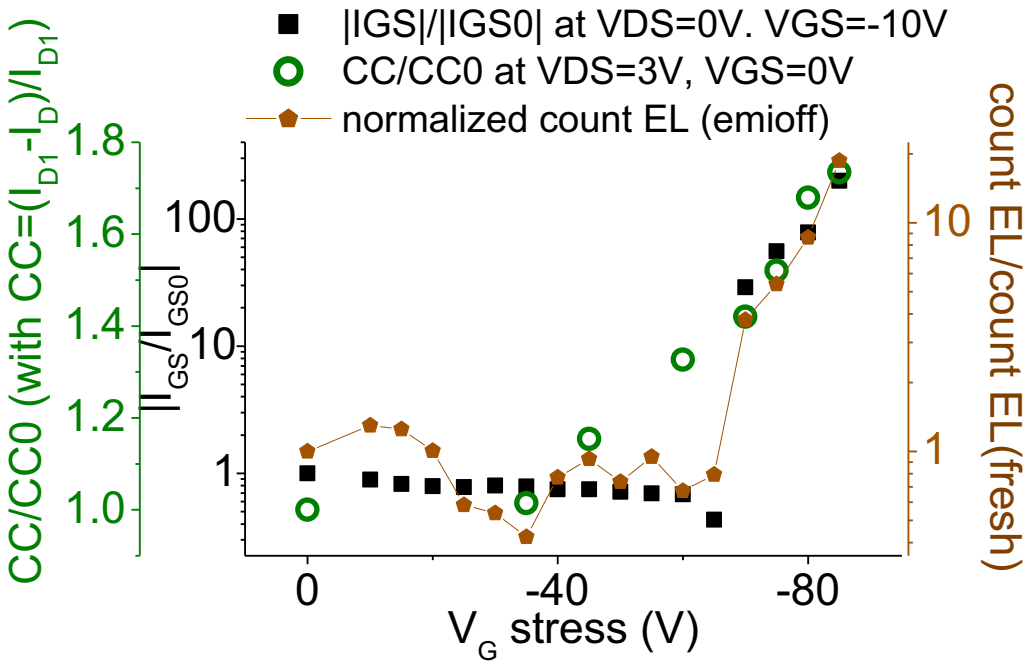


Figure 5.52: 3Y graph: comparison among DC, pulsed and light emission analysis

Figure 5.52 shows the correlation among several degradation effects measured through the analysis of different parameters: (i) count of the emission measured in OFF state monitored at each step of the stress; (ii) transistor leakage gate current measured during emission in OFF condition at V_{GS}=-10V, V_{DS}=0V; (iii) current collapse evaluated at V_{DS}=3V, V_{GS}=0V. All the compared characteristics are normalized to the fresh value. On the basis of Figure 5.52 it is firstly possible to demonstrate that a strong correlation is established between count reported during light emission and transistor gate leakage current. According to Figure 5.37 even if diode reverse current is considered a strong correlation among these parameters is established.

On the other hand dynamic measurements show a more complex behaviour, which can be divided into three main regions: (i) for lower gate source voltage applied during the stress (i.e. lower than V_{GS}=-45V in this ase) no variation of the current collapse is noticed; (ii) when higher gate source voltage is applied, even if no significant degradation is reported in both diodes and transistor leakage gate current, current collapse starts increasing; (iii) beyond not recoverable degradation the variation of the current collapse is strongly correlated with gate current, both when reverse diode current and transistor gate leakage current are taken into account.

This effect is more visible in Figure 5.53, where current collapse as a function of transistor leakage gate current is shown. The trap T1 amplitude variation is not considered, on the basis of

the strong relation established between pulsed and drain current transient demonstrated in Figure 5.50.

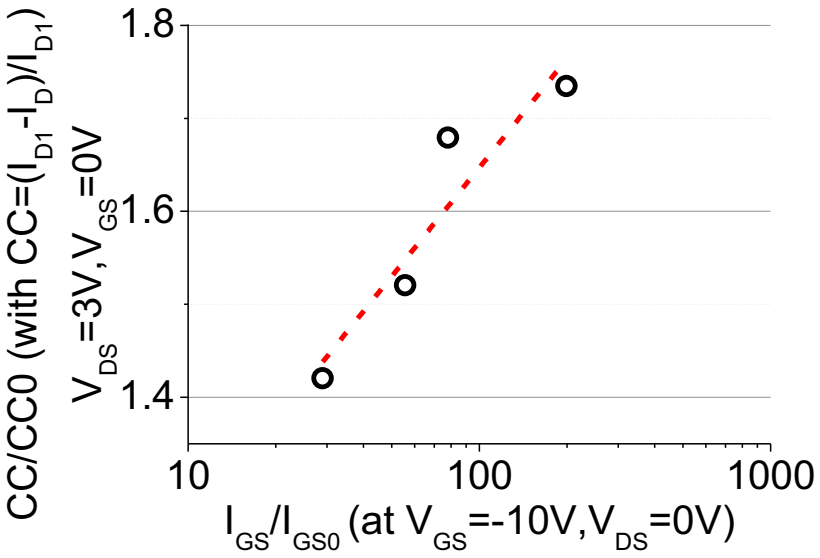


Figure 5.53: Correlation between current collapse and leakage gate current when a bias higher than the critical voltage is applied (dashed line is a guide to the eye)

5.5.3 Comparison in devices with different Fe doping quantities

In 5.5.2 we have reported preliminary measurements of all the samples considered (samples A, B, C, D), both in terms of DC characterization and trapping analysis. Furthermore a detailed analysis of a reverse bias step stress on a Fe doped device is proposed, widely focusing on the correlation between different degradation aspects: DC main parameters and trapping behaviour.

In this paragraph we present the comparison of the correlation among different degradation aspects measured in devices with different Fe doping in the buffer layer: (i) sample A with no Fe doped buffer layer, (ii) sample B with an intermediate Fe doping ($1x10^{17}$) and (iii) sample D with a high Fe doping quantity ($4x10^{17}$). Devices were all submitted to step stress, with an increasing (negative) gate voltage, drain and source terminals grounded. Representative results are reported for one device for each group. Several devices have been tested for each sample typology, stating that a good reproducibility is shown.

Figure 5.54 shows the diode gate current when reverse bias is applied (V_{GS}=-6V) monitored during the stress in all the samples. No correlation is shown between gate voltage at which occurs degradation and Fe doping quantity in the buffer layer. Difference noticed between devices with different Fe doping quantity is lower than the variability measured in devices with similar structure and doping. On the contrary devices with no iron doping are characterized by a much lower gate voltage applied at which not recoverable degradation occurs.

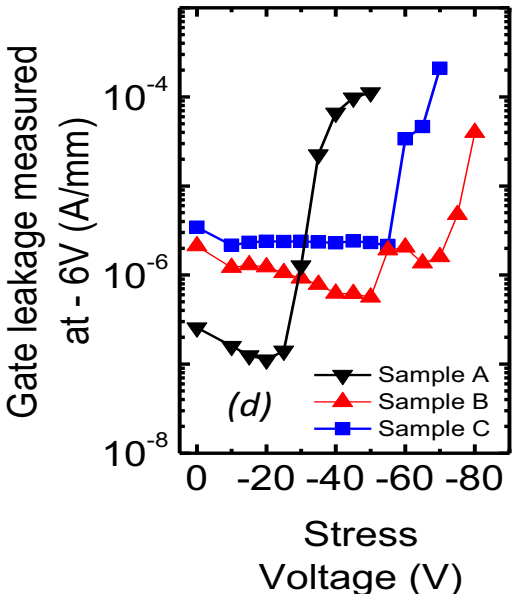


Figure 5.54: gate leakage current monitored during the stress for devices with different Fe doped buffer layer

The permanent degradation stated in all the device typologies is confirmed by Figure 5.55, where the GS diode I-V curve monitored at each step of the stress is shown for devices with different doping in the buffer layer. In the inset a representative light emission for sample B, measured after not recoverable degradation, is shown. The correlation between light emission count and gate current measured both in diodes and transistor leakage is confirmed for all the samples measured, independently from iron quantity in the buffer layer. This aspects confirms that the increase is due to the generation of defective paths identified through EL measurements.

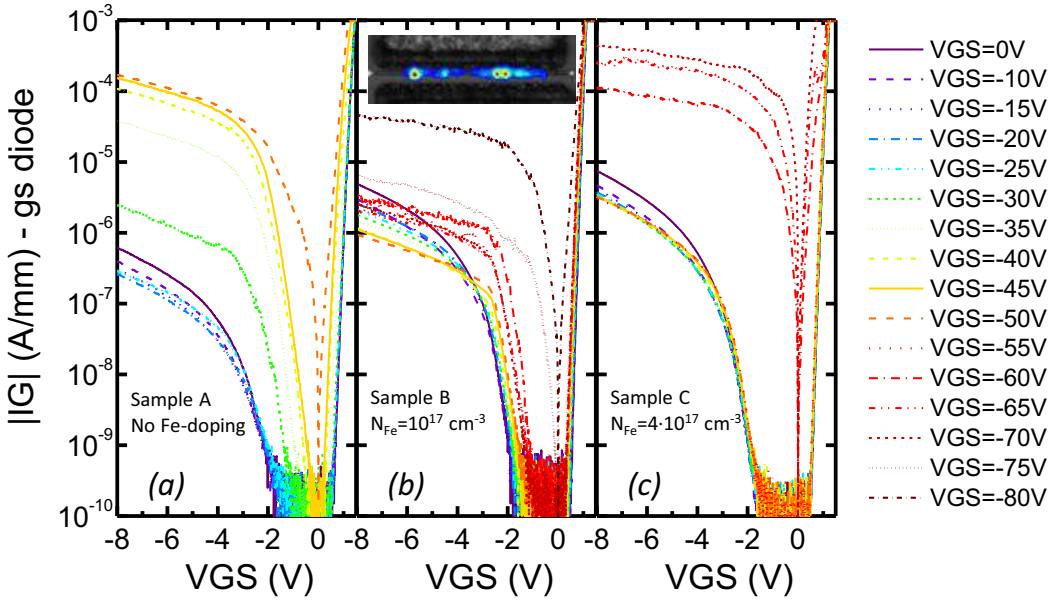


Figure 5.55: : variation of gate current before/after step-stress on three stressed devices (A, B and D)

Consistently with detailed analysis provided for a device with Fe doping in the buffer layer, stress induces an increase of current collapse. Devices with no iron doped buffer layer report an increase of current collapse several steps after degradation, while devices with Fe doped buffer layer exhibit a degradation of trapping conditions before the degradation.

EL microscopy indicates that the damage (increase in leakage current) takes place in correspondence of localized defective regions, with a size significantly smaller than gate width. The increase in current collapse detected after stress can be hardly explained by considering that stress induces the generation of defects only in such small-size regions. Furthermore it is important to remember that current collapse originates from both the traps T1 and T2. Therefore, although the amplitude T1 faces an increase, the increase of the current collapse is strongly affected also by the variation of the increase of the amplitude associated to trap T2. The trend of the current collapse variation during the stress is reported in Figure 5.56.

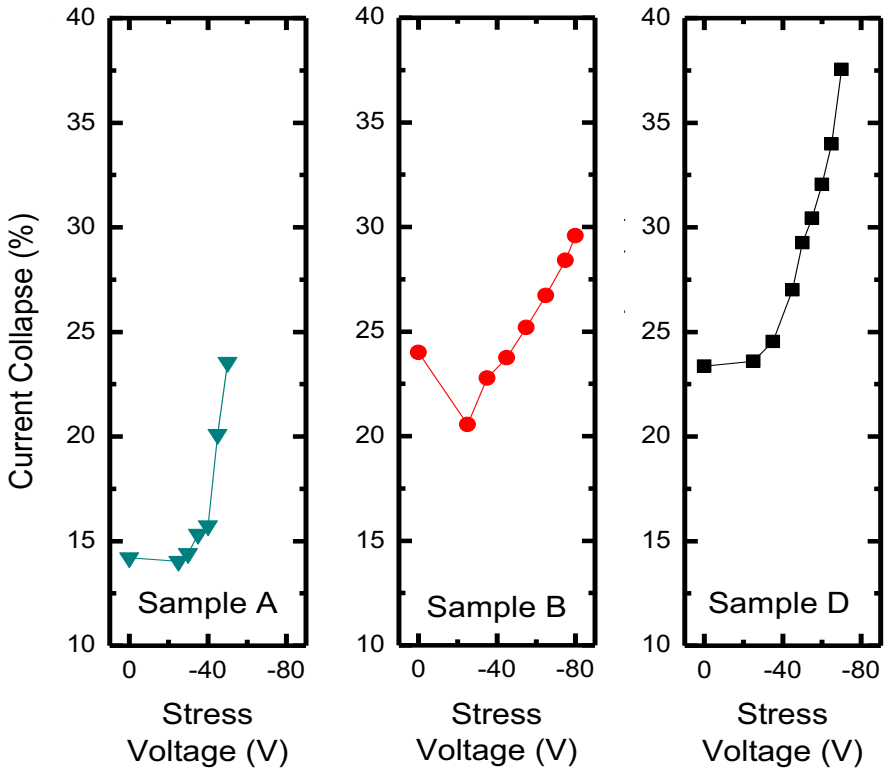


Figure 5.56: : variation in the current collapse measured during step-stress on the three series of samples. Data are plotted as a function of the stress voltage

Remarkably, drain current transient measurements carried out before/after stress indicate that, for all the analysed devices, the increase in current collapse is not correlated to the generation of new trap levels; indeed no new peak is found in drain current transients curves, thus confirming that in all the devices traps time constant does not change with the stress,

leading to no variation of the Arrhenius plot, both in terms of activation energy and cross section. The current collapse variation originates from the increase in the signal associated with the pre-existing trap levels T_1 (located in the buffer) and T_2 (located in the barrier).These changes (Figure 5.57) can be interpreted as follows.

The amplitude of the trap T_2 varies as a consequence of an increase in the concentration of a defect (T_2), which is supposed to be located in the AlGaN barrier layer. Defects corresponding to trap T_2 characterize the fresh device, as demonstrated by preliminary measurements and can be due to converse piezoelectric effect or high electric field applied. A different mechanism leads to the variation of the trap T_1 and it is not possible to describe variation of both the traps with analogous considerations. Indeed the location of trap T_1 in the buffer layer reduce the high influence of the electric field on trapping behaviour degradation and the probability of generating defects which, on the contrary, significantly characterizes the AlGaN barrier layer.

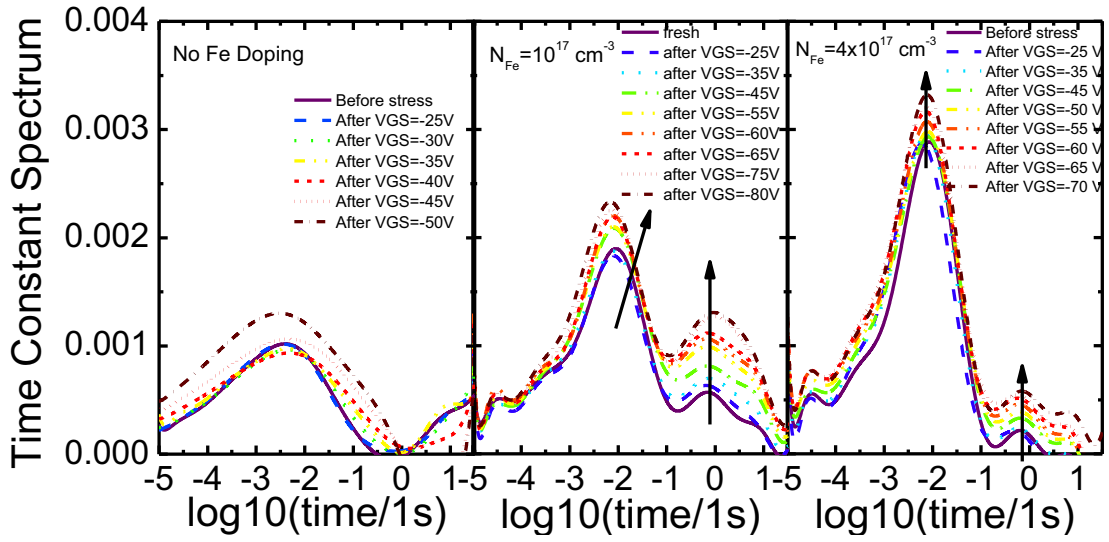


Figure 5.57: time constant spectrum extrapolated from drain current transient measurements carried out during the step stress of devices from wafer A, B, and C

The increase in the signal of T_1 can be explained by considering that, after stress, the generation of defect-related conductive paths between the gate and the channel significantly enhances the transfer of electrons towards trap states (T_1) located in the buffer; this enhances the current collapse related to T_1, even if the density of defects in the buffer does not change. Under this hypothesis, devices with no (or few) pre-existing defects in the buffer show a smaller increase in current after stress. The increase of the amplitude of signal corresponding to trap T_1 is further explained in Figure 5.58 as a function of the stress. In this case sample A has been stressed only up to V_{GS}=-50V. Further tests evaluated with a V_{GS} up to -80V, consistently with stress carried out in Fe doped samples, demonstrates an increase of both current collapse and signal amplitude associated to trap T1.

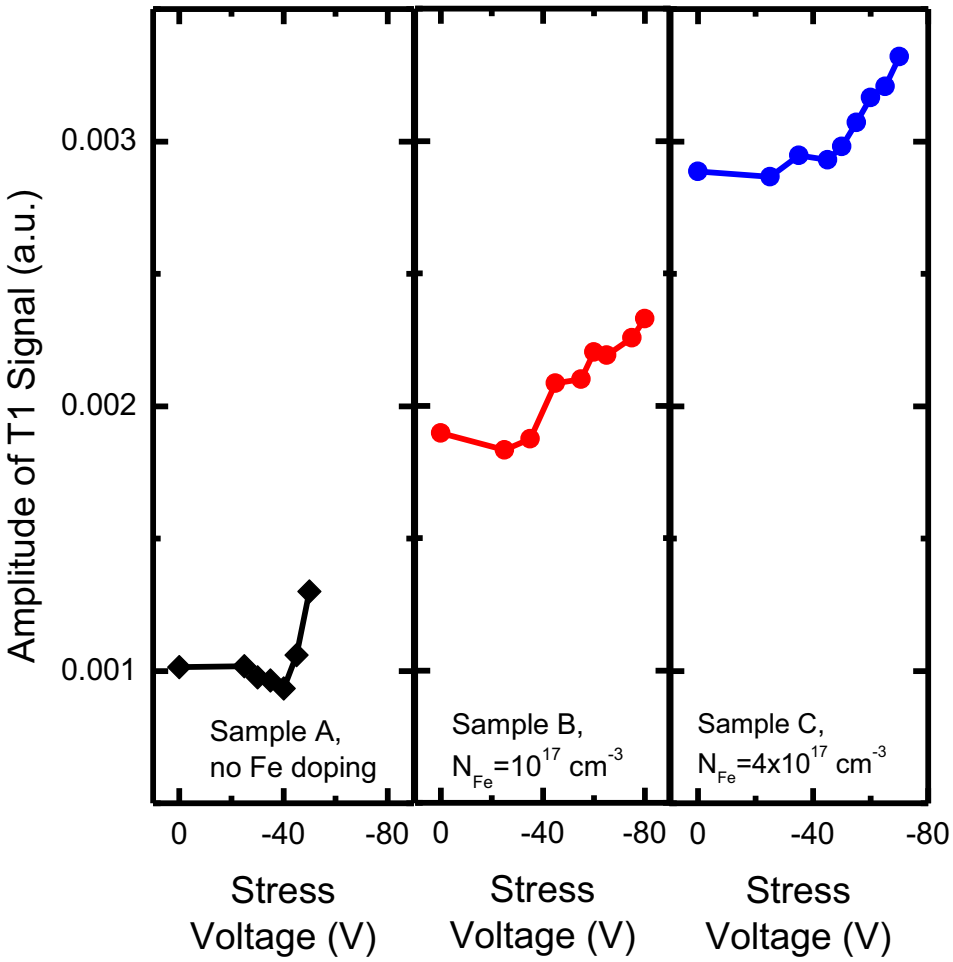


Figure 5.58: variation in the signal associated to trap T1 (maximum of the time constant spectra) measured during step-stress on the three series of samples. Data are plotted as a function of the stress voltage

Chapter 6:Improvements provided by the use of InAlN/GaN structures

6.1 Improvements provided by InAlN/GaN structures

The application of High Electron Mobility Transistors in application which require high power and frequency leads to the necessity of development new structures and geometries to improve device performances. Although significant performances are reported in literature about AlGaN/GaN HEMTs, InAlN/GaN structures represent an important alternative because of its properties which determine significant properties in terms of electrical parameters, analysis of the operation at high temperature, power performances [103], [104].

InAlN can achieve a lattice matched structure with GaN layer on the basis of In content in the barrier layer, thus increasing the device electrical stability, even at high temperatures. Furthermore, consistently with the deletion of the polarization effects a higher carrier density in the 2DEG is obtained for defined In content in the barrier layer, thus enhancing drain current and output power available.

Main disadvantages are due to the low intrinsic mobility of InAlN/GaN devices, which impede high drain current values. Furthermore significant difficulty in the device growth, both with OMPVE or MBE technique, has been reported.

6.1.1 Materials properties

InAlN is a ternary alloy that can be used to develop barrier layer in High Electron Mobility Transistors. This ternary alloy has been studied and used less than other materials, such as AlGaN, also because its growth is challenging as a consequence of diverse thermal stability, lattice constant and cohesive energy of AlN and InN [90].

First main advantage is the possibility of varying energy gap and lattice constants by changing the indium content in the allow ($In_xAl_{1-x}N$). This aspect allows the generation of a structure which can be defined lattice matched with GaN by imposing a In content of 17%, polarization matched with GaN by defining a In content of 32% or centro-symmetric polarization free barrier with In content of 43% [91]. Fig shows the energy gap and lattice constant variation as a function of Indium content. A energy gap of 5.4 eV corresponds to the lattice matched structure. A carrier density of 2.8 x 10^{13} cm^{-2} is measured [92].

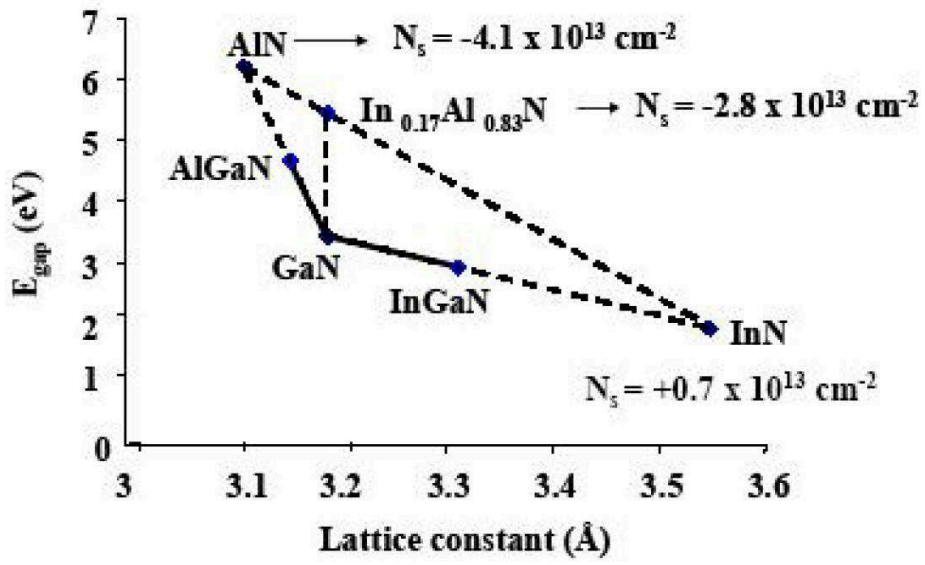


Figure 6.1: Energy gap and lattice constants in AlN, GaN and InN binary and ternary alloys [93]

According to previous works reported in literature [1] , it is possible to define the bandgap of InAlN alloys through the following empirical expression, where the term b is a bowing parameter.

$$E_g^{AlxInN} = xE_g^{AlN} + (1-x)E_g^{InN} - b_{AlInN}x(1-x) \qquad (6.1)$$

According to Figure 6.1 it is possible to determine a barrier (InAlN) and buffer (GaN) layer lattice matched by introducing a correct In quantity in the ternary alloy described. The absence of lattice mismatch leads to the deletion of mechanical stress and, thus, of piezoelectric polarization. On the other hand, consistently to the high Al content reported it is possible to achieve high spontaneous polarization constants, leading to a high carrier density concentration in the 2DEG which is usually higher than 2.8 x 10^{13} cm^{-2} [92]. The high carried density in the channel is proportional to the vicinity with AlN. Furthermore the Curie temperature which characterizes AlN (higher than 1000°C) determines a significant stability also from a thermal point of view.

One of the main disadvantages of the InAlN alloy is the very low carrier mobility in the 2DEG. As a consequence, despite the high carrier density, it is not possible to reach a current value which is high and not strongly dependent on gate length. In the first devices grown a mobility of almost 200-300cm^2/Vs was obtained. This aspect was mainly due to a roughness interface with a consequent scattering which limits the carriers in the obtaining a high velocity. An important solution to solve this problem is represented by the introduction of a thin AlN layer, determining a mobility higher than 1000cm^2/Vs [94], [95]. The mobility increase is strongly correlated with the AlN layer thickness. According to previous works reported in

literature [90] the peak of the mobility is reached for a AlN spacer thickness of 1nm (Figure 6.2). Although the use of AlN increases the carrier density with no strong decrease of the mobility, it is important to remember that, differently from InAlN alloy, it is not possible to easily obtain a lattice matched structure with GaN, thus inducing a mechanical strain variation with the consequent eventual determination of defects and piezoelectric polarization.

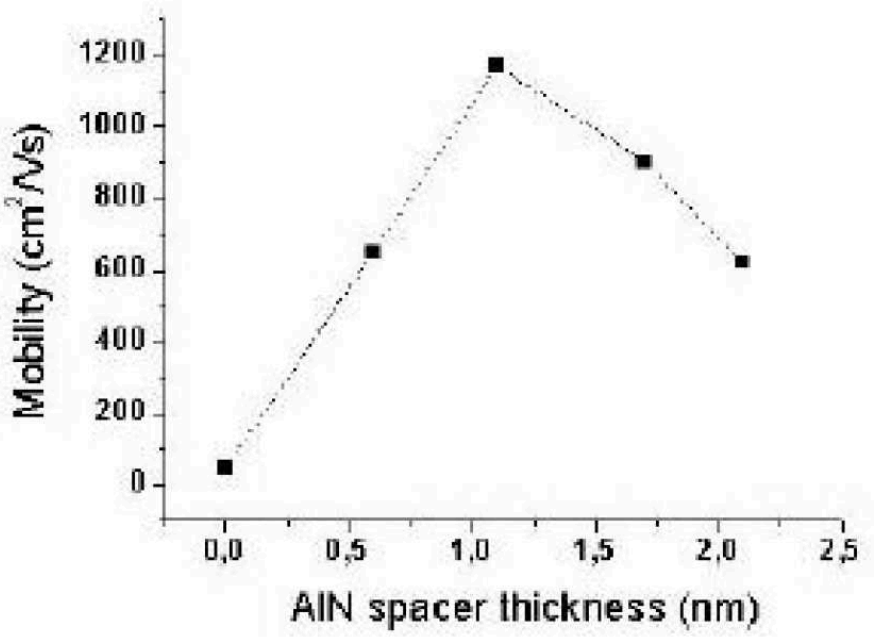


Figure 6.2: Mobility variation as a function of AlN spacer thickness [90]

A further aspect which contributes to InAlN better performances is represented by electronic surface properties, much dependent on device composition and preparation [96]. In FET structures characterized by a InAlN barrier layer an unpinned surface potential is obtained. As a consequence of the surface potential corresponding energetic level it is possible to reach much lower barrier layer thickness than AlGaN materials [95]. According to previous results studied it is possible to reach a barrier layer with 5nm without significantly compromise carrier density and electrical properties [97], [98], [99],[100]. Furthermore it is possible to achieve a lower device gate length and corresponding structural aspect ratio even obtaining good performances in terms of available frequency and short channel effects. The lowering of the barrier layer has important effects on device main electrical properties, which can mainly be summarized in a threshold voltage positive shift (Figure 6.3) [98] and change in the transconductance peak (Figure 6.4) [90].

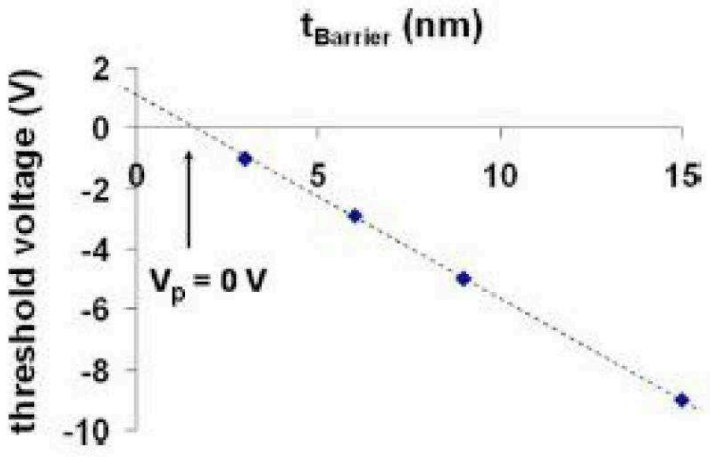


Figure 6.3: threshold voltage shift as a function of barrier thichness [98]

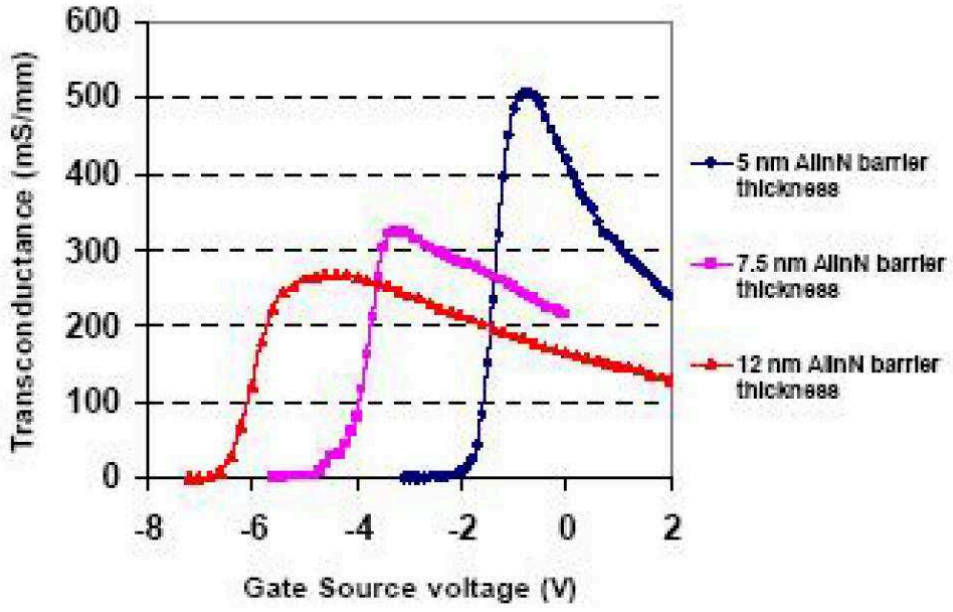


Figure 6.4: transconductance curve as a function of barrier layer thickness [90]

6.1.2 Electrical performances

InAlN material properties firstly determine high performances when drain current measured at high dissipation conditions is considered, as a consequence of the intrinsic high carrier density and of the high mobility reached by the use of an AlN spacer layer [94], [95]. Work of Kohn et al. [95] demonstrates that a InAlN/GaN structure characterized by a gate length of 0.15µm and gate width of 50µm can reach a drain current in saturation region of 2A/mm when measured at high dissipation conditions. High corresponding transconductance peak values are also demonstrated.

Drain current can be significantly influenced by the substrate used. Results concerning electrical parameters measured in a devices with (i) Si, (ii) SiC, (iii) sapphire substrate have been reported in Kohn et al. [95]. Highest performances are reached by SiC substrate with a value higher than 2A/mm, according to its thermal properties. Although the difference of 2DEG carrier density in the three substrates can be considered as negligible, drain current and power density are lower in Si and sapphire [100]. In all the conditions high frequency performances are reached [101,102].

Unfortunately InAlN/GaN HEMTs are often characterized by high gate leakage current values which limits the maximum voltages applicable. As a consequence Schottky contact is characterized by a significant passage of current, thus facing degradation when voltage levels of about 20-25V are imposed. Breakdown voltages are therefore influenced by this aspect. Although the barrier layer thickness can be lowered with no significant influence in the 2DEG carrier density performances, it causes higher gate leakage current, thus allowing the application of a lower voltage, Several works discuss how to avoid this issue; a solution consists of the introduction of an insulating layer to limit the gate leakage current [105], [106]. A further solution is the use of a field plate or T gate structure, which significantly enhances the breakdown voltage due to the gate leakage current improvement.

Consistently with pulsed measurement it is possible to state, on the basis also of works previous reported [107], that self-heating influences the drain current value in a significant way, even if improvements are provided by the use of a SiC substrate, according to its thermal properties. Concerning trapping behaviour similar considerations to the ones proposed for AlGaN/GaN devices can be taken into account. Similar solution are furthermore considered to improve performances.

InAlN structures demonstrates a high stability when a high temperature is imposed. One of the most important results are described by Medjdoub et al. [107]. It is shown that no degradation is noticed when the device is stressed at 1000°C. Results confirm the significant thermal stability due also to the lack of piezoelectric effect in lattice matched hetero-structures, neither when drain current is considered nor when metallurgical degradation at the gate contacts is evaluated. When temperatures higher than T=800°C are imposed different trapping effects influence the devices, due to the activation of traps which rely in the buffer, but no significant degradation is induced. [107]

6.2 Use of a different gate Schottky contact: improvements provided by a Mo/Au gate stack

Due to the significant problematic related to high leakage gate current in InAlN/GaN structures the choice of a proper Schottky gate contact is essential. The high leakage gate current can be ascribed to several phenomena, such as a (i) low barrier height due to the physical properties of gate stack material and InAlN barrier layer and the (ii) surface defects which strongly affect diodes characteristics.

The first issue can be overcome by using different materials, such as Ni or Pt which provide a quite high barrier layer. The impact of several metals used as gate schottky contact on AlGaN/GaN devices has been studied in detail in literature [109], [110], [111], [112]. Furthermore an interesting analysis of Schottky barrier properties of several various materials on n-GaN has been provided by Schmitz et al. [113]. The second issue can be overcome by using a MOS – like structure, so called MOSHEMT, or by a surface treatment by means of insulating materials. In this case it is possible to use thin layers of Al_2O_3, characterized by essential properties namely high energy gap, high breakdown field and significant thermal stability [105]; a further solution is provided by Kuzmik et al., which suggests the use of ZrO_2 or HfO_2.[115]

Some materials, like Molybdenum, are very important. First of all, as reported by Sozza et al. [108], it allows a high stability when stress is applied. Moreover, differently from Ni/Au, it allows the use of further techniques, such as sputtering, with the achievement of good performances in devices, both in terms of trapping phenomena and stability.

In this paragraph a comparison of InAlN/GaN HEMTs with analogous structure but different gate, respectively Mo/Au and Ni/Pt/Au, is studied. The effects of a different gate contact structure on DC and pulsed main characteristics are discussed. Despite no meaningful variation is noticed during DC analysis, pulsed evaluation demonstrates that the use of a Mo/Au gate contact leads to an improvement of trapping characteristics. By means of a three terminals step stress it is finally proved that Mo/Au does not significantly affect device stability.

6.2.1 Analysed devices

The analysed structures are InAlN/GaN HEMTs with a semi –insulating 4H SiC substrate, a 1.64µm GaN buffer layer, a 6.3nm $In_{0.19}Al_{0.81}N$ barrier layer with a 19,1% In content. Between the buffer and barrier layer a 1.5nm AlN interlayer is introduced to improve the device mobility. The whole structure is covered with a silicon nitride passivation layer. The ohmic contacts are composed by a Ti/Al/Ni/Au stack. Gate Schottky contact differs in the wafer. Half wafer is composed by a Mo/Au multi-layer structure, while the remaining half is made of a Ni/Pt/Au one. A schematic structure is shown in Figure 6.5.

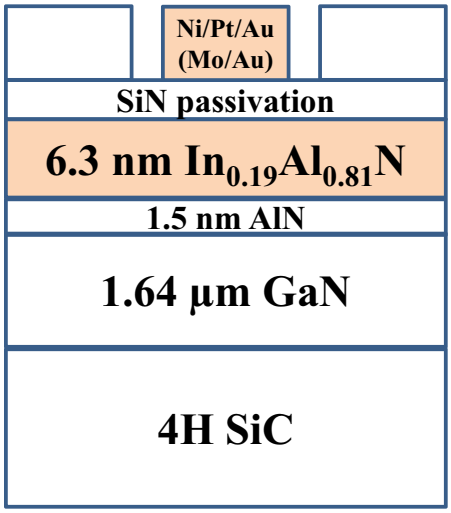


Figure 6.5: schematic cross section of the analysed devices

(a) (b)

Figure 6.6: representative figure of a (a) D1 and (b) D2 sample variation of Schottky contacts

The maskset offers several devices with different gate width and length, with a minimum gate length of 0.1µm. All the devices analysed in this chapter have a gate length of 0.25µm, since many devices with lower length revealed a high leakage drain current measured in OFF state. Two sets of devices have been analysed. Devices D1 are characterized by W_G=2x40µm, L_G=0.25µm, gate pitch 35µm, L_{GS}=0.5µm, L_{GD}=2µm. Devices D2 have a W_G=2x50,

L_G=0.25µm, gate pitch 35µm, L_{GS}=1µm, L_{GD}=2µm. All the devices are not covered by any field plate or air bridge. A representative image of devices D1 and D2 is then reported in Figure 6.6a and Figure 6.6b.

6.2.2 Measurement details

Several measurements have been carried out to state the improvements due to the use of a Mo/Au gate stack. Main evaluation is: (i) DC characterization, (ii) pulsed analysis, (iii) emission microscopy variation as a function of gate and drain bias imposed, (iv) OFF state three terminals stress.

DC Characterization

Devices have been measured with a parameter analyser (Agilent 5263A) and biased with RF tips inside a Karl Suss probe station, in order to avoid oscillations. During the DC characterization the following curves have been evaluated: (i) I-V of the GS diode and I-V of the GD||GS diode evaluated in linear and logarithmic scale; (ii) OUT DC characteristic of the transistor (i.e. I_{DS} vs V_{DS} and I_{GS} vs V_{DS}) measured for V_{GS} from higher to lower values and vice versa in order to study DC trapping; (iii) trans characteristic of the transistor (i.e. I_{DS} vs V_{GS} and I_{GS} vs V_{GS}) measured in linear, knee voltage and saturation zone; Sub threshold trend (i.e. log(I_{DS}) vs V_{GS}) measured in linear, knee voltage and saturation zone; transconductance (i.e. $\Delta I_{DS}/\Delta V_{GS}$ vs V_{GS}) measured in linear, knee voltage and saturation zone.

Main parameters considered for the analysis are: (i) drain current measured in saturation zone (I_{DSS}) considered both in high dissipation condition (V_{GS}=1V and V_{GS}=0V) and in OFF state (V_{GS}=-7V); the OFF state gate source voltage value is chosen on the basis of high drain leakage current; (ii) max g_m reported in saturation zone (V_{DS}=10V respectively), (iii) transistor gate leakage current measured in OFF and ON state in saturation zone (V_{DS}= 10V and V_{GS}= -6V, V_{GS}=0V and V_{GS}=1V respectively), (iv) diode current measured with reverse and forward bias applied (V_{GS}= -7V, V_{GS}=1V respectively), (v) threshold voltage (V_{TH}), evaluated as the V_{GS} corresponding to a drain current value of I_{DS}=I_{DSS}/100, I_{DS}=I_{DSS}/20, I_{DS}=I_{DSS}/2. Furthermore threshold voltage is also defined as the intercept with the x-axis of the curve tangent the I_DV_G.

Pulsed Characterization

Pulsed evaluation has been carried out with a custom setup, defining I_{DS} vs V_{DS} and I_{DS} vs V_{GS} curves by pulsing the drain (V_{DS}) and gate voltage (V_{GS}) from a quiescent bias. Details about measurement setup have been reported in 5.4.1. Three different power dissipation levels

from a null power dissipation and trapping condition (V_{GSQ}=V_{DSQ}=0V) to a higher trapping quiescent bias point (V_{GSQ}=-6V, V_{DSQ}=6V) are applied, according to device degradation voltage. A duty cycle of 1% with 1μs pulse width is considered; the measurement is taken in a range between 840-885ns after the pulse is applied. Two preliminary measurements have been carried out: in the first case four power dissipation levels have been applied leading to a (V_{GSQ}=-7V, V_{DSQ}=20V) while in the second case a maximum condition corresponding to (V_{GSQ}=-7V, V_{DSQ}=10V) is imposed. The degradation stated in both the structures during first condition and in the Ni/Pt/Au structure in the second one confirmed that it is not possible to apply high drain source and high gate source voltage in order not to degrade the device. Device degradation mainly consisted of: (i) threshold voltage positive shift; (ii) decrease of the drain current; (iii) slight variation of the leakage gate current measured in OFF and ON state.

Trapping is quantitatively defined by the variation of the drain current (current collapse) and by the shift of the threshold voltage (V_{TH} dynamical shift) measured when different baselines are imposed. The current collapse is defined as the ratio between the difference of the drain current measured at a defined V_{GS} and V_{DS} in two different baselines over the drain current value in the first of the two baselines. It is measured in knee voltage zone both at high dissipation (V_{GS}=0V) and semi-on conditions (V_{GS}=-1V) in order to analyse the worst case. The V_{TH} dynamical voltage is defined as the intercept of the curve tangent to the I_{DS} vs V_{GS} curve with x-axis in a consistent bias point (V_{DS}=3V).

Emission microscopy

Light emission has been acquired with a high sensitivity silicon camera (IXON camera). During emission microscopy the device is biased both in OFF and ON state, respectively at V_{GS}=-6V, V_{DS}=0V and V_{GS}=0V, V_{DS}=10V. The emission is acquired for a different amount of time, in order not to reach camera saturation in a consistent way with current value during the conditions. An acquisition time of respectively 119s and 3s has been imposed. During the step stress the emission is acquired for 10s not to reach camera saturation.

Furthermore, the emission as a function of different gate and drain bias applied is measured, in order to study the difference of the ratio between electro-luminescence and drain current in devices with a different gate stack.

Three terminals OFF state stress

During the OFF state three terminal step stress the sample has been biased in OFF condition for 120s, by applying a constant V_{GS} and V_{DS} value during each step. A V_{GS}=-6V has been applied, while V_{DS} is increased of 2V each step from V_{DS}=10V to V_{DS}=40V. Emission

microscopy measurements have been simultaneously acquired during the stress for 10s. After each step DC analysis has been carried out to monitor main DC parameters variation. Moreover light emission has been evaluated after each step by biasing the device in OFF (V_{GS}=-6V, V_{DS}=0V) and ON state (V_{DS}=10V, V_{GS}=0V) for 120s and 3s, respectively.

6.2.3 Device characterization

DC Characterization

DC analysis carried out with preliminary measurements states that no significant improvement is reached by devices with a Mo/Au gate stack if drain current or maximum transconductance measured in saturation zone is considered. All following figures have been measured on D2 devices, although consistent results have been noticed in D1 ones. The slight drain current value noticed in Mo/Au HEMTs is negligible if compared to device variability. An example of drain current and transconductance measured in devices D2 is shown in Figure 6.7a and Figure 6.7b, respectively. The output I_DV_D curve is measured from lower to higher gate source voltages applied, while the transconductance curve shown is measured in the knee voltage zone. Similar results are obtained if the output curve is measured from higher to lower gate source voltages and if the transconductance is evaluated for different drain source voltage values.

The I_DV_D output curve carried out from a lower to a upper gate source voltage and vice versa Figure 6.8 also states that no significant DC trapping and kink effect is noticed both in D1 and D2. Analogous results have been measured with Mo/Au and Ni/Pt/Au gate stack.

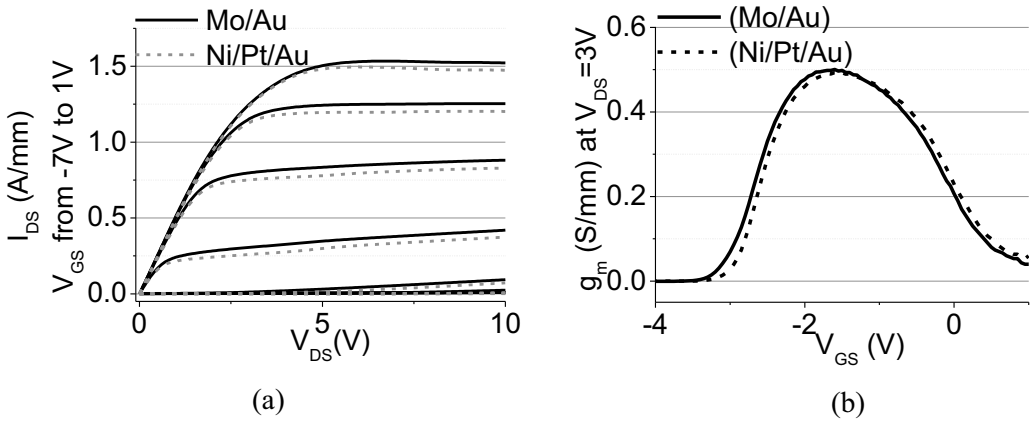


Figure 6.7: comparison between (a) output IDVD curve and (b) transconductance curve measured in devices with Mo/Au and Ni/Pt/Au gate stack.

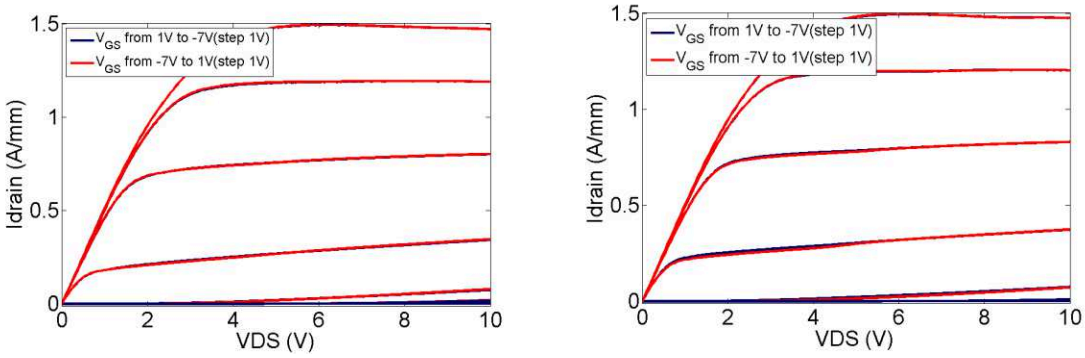


Figure 6.8: DC trapping evaluated in devices with (a) Mo/Au and(b) Ni/Pt/Au devices

The comparison of the transconductance measured in Mo/Au and Ni/Pt/Au devices during DC preliminary evaluation shows that no meaningful difference is reported in the max g_m, neither when linear nor when knee voltage region is considered. A low variation of the transconductance peak (about 5%) is measured in Mo/Au samples when saturation zone is studied.

Mo/Au devices seems to be characterized by significant improvements in terms of drain leakage current measured in OFF state , demonstrating a value about one order of magnitude lower Figure 6.9. However this difference can be considered not significant according to variability among different devices. Furthermore the employ of a different gate stack induces an average variation of 100mV in the threshold voltage (Figure 6.9). A good reproducibility of the V_{TH} value is stated in all the devices measured, both when D1 and D2 devices are considered. In Figure 6.9 the analysis has been carried out in knee voltage zone; consistent results have been noticed in saturation zone.

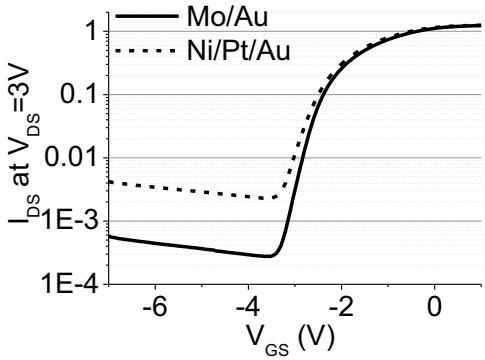
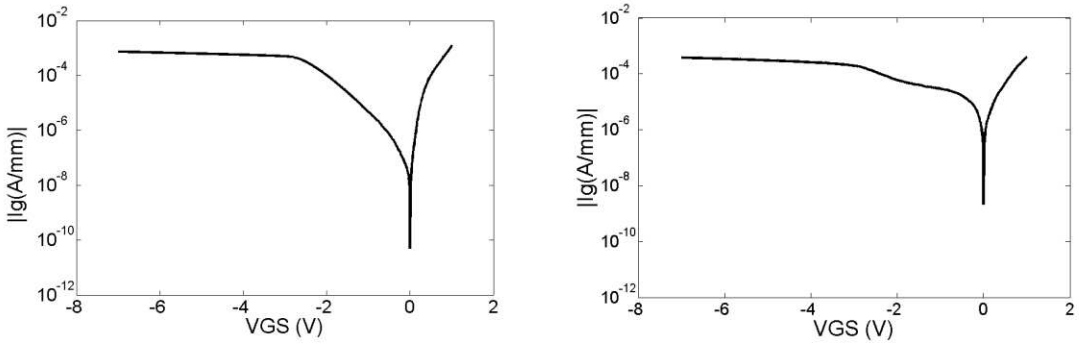


Figure 6.9: Comparison of I_{DS} vs V_{GS} in Mo/Au (solid curve) and Ni/Pt/Au (dashed curve) devices



(a) (b)

Figure 6.10: GS DIODE measured in a device with (a) Mo/Au and (b) Ni/Pt/Au gate stack

Gate leakage current demonstrates a high value, in the range between 10^{-4} and 10^{-3} A/mm, when the GS diode is considered. An example for Mo/Au and Ni/Pt/Au devices is reported in Figure 6.10. Consistent results have been noticed in the transistor leakage gate current measured both in OFF and ON state.

Pulsed analysis

Trapping behaviour as a function of different gate stack used has been investigated. Traps are defined only by pulsed measurements; it was not possible to evaluate drain current transients as a consequence of the low robustness, especially in Ni/Pt/Au devices. Furthermore the low current collapse value does not allow the detection of significant peaks in the derivative function corresponding to transient data.

Due to the low robustness stated in HEMTs with Ni/Pt/Au gate stack the highest trapping condition imposed is V_G=-6, V_D=6V, in order to avoid the influence of device degradation in pulse evaluation. Figure 6.11 and Figure 6.12 compares the behaviour of output I_DV_D curves in a representative Mo/Au and NI/Pt/Au device, demonstrating Mo/Au devices lower dispersion. A good reproducibility has been noticed in devices with similar structure, although characterized by different geometry such in the case of D1 and D2 devices.

Current collapse is evaluated in the knee voltage zone biasing the device in two condition: (i) high dissipation (i.e. V_{GS}=0V, V_{DS}=3V) and (ii) semi-on condition (i.e. V_{GS}=-1,V_{DS}=3V). In both the conditions considered the gate contact strongly influences trapping phenomena. Figure 6.13 shows the comparison between current collapse measured in semi-on condition in Mo/Au and Ni/Pt/Au devices. Although consistent results are demonstrated in high dissipation conditions, i.e. V_{GS}=0V, evaluation in semi-on condition shows a higher difference, consistently with the trap location as it will be explained, and a better reproducibility. An average current collapse value of 8% and 20% is measured in semi-on condition in Mo/Au and Ni/Pt/Au samples, respectively. Results for both D1 and D2 devices are shown.

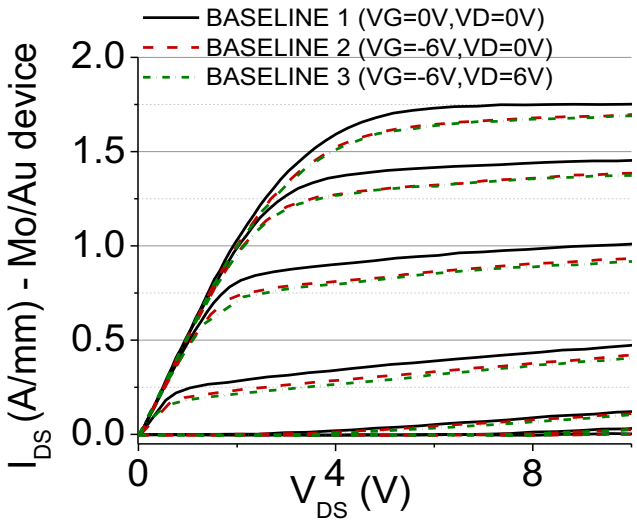


Figure 6.11: Pulsed I_{DS} vs V_{DS} measured on a Mo/Au device. V_{GS} from -7V to 1V with 1V/step

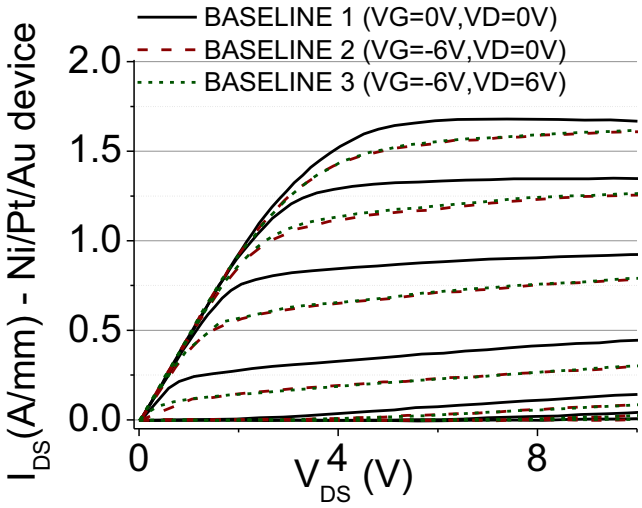


Figure 6.12: Pulsed I_{DS} vs V_{DS} measured on a Ni/Pt/Au device. V_{GS} from -7V to 1V with 1V/step

Figure 6.14 confirms that the current collapse is mainly due to the threshold voltage dynamical shift. An average V_{TH} shift of 290mV and 100mV is measured, respectively, on Ni/Pt/Au and Mo/Au devices when a consistent bias point is evaluated (V_{DS}=3V). A good reproducibility has been established in devices measured, although the slight difference in geometries considered. We can speculate that the improvement due to the use of a Mo/Au contact can be ascribed both to the use of a different gate stack, both to the different technological process. The difference verified in devices characterized by a different gate contact and the slight difference among main dynamical parameters variation during the second and third baseline suggests that traps may be located under the gate. This hypothesis is further suggested by the consistency between V_{TH} and I_{DS} variation during pused measurements.

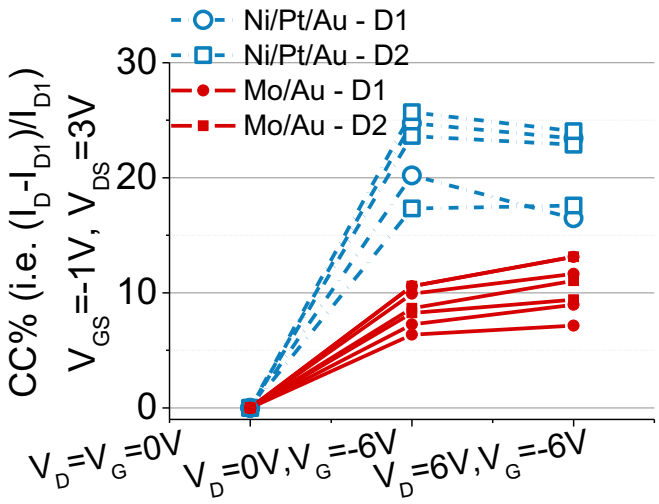


Figure 6.13: current collapse at V_{GS}=-1V, V_{DS}=3V

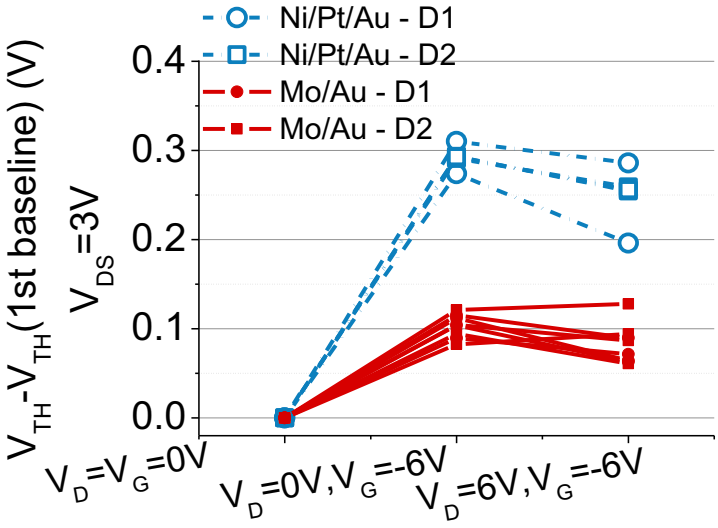


Figure 6.14: V_{TH} dynamical shift measured at V_{DS}=3V

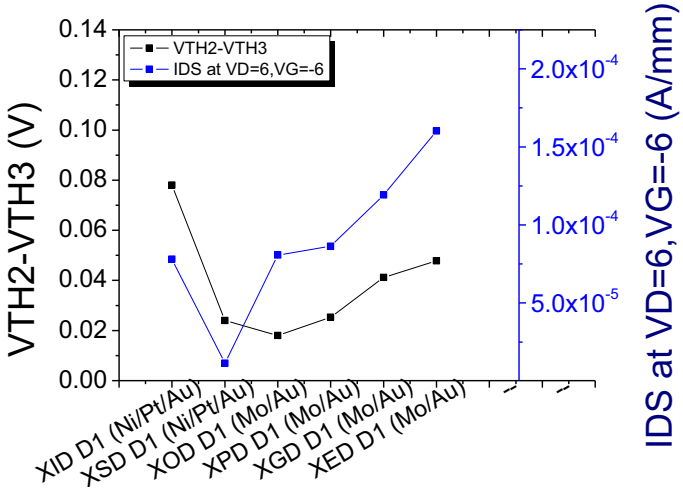


Figure 6.15: Correlation between threshold voltage dynamical shift during second and third quiescent bias point applied and transistor leakage drain current

In some devices current collapse is lower in the third quiescent bias point than in the second one. Consistent results are shown in the analysis of the threshold voltage shift, consistently with the assumption that traps are probably located under the gate and that the drain current variation is mainly determined by the threshold voltage dynamical shift. This can be due to the high drain current measured in OFF state, which is higher in the third condition than in the second. Indeed, a good correlation is established between threshold voltage variation in the second and third baseline and transistor leakage drain current (Figure 6.15).

Light emission microscopy

Light emission characterization is carried out during preliminary measurements in order to define the electro luminescence variation as a function of gate source voltage applied for several drain source voltages. Furthermore the ratio between EL value and drain current is determined in order to compare Mo/Au and Ni/Pt/Au performances.

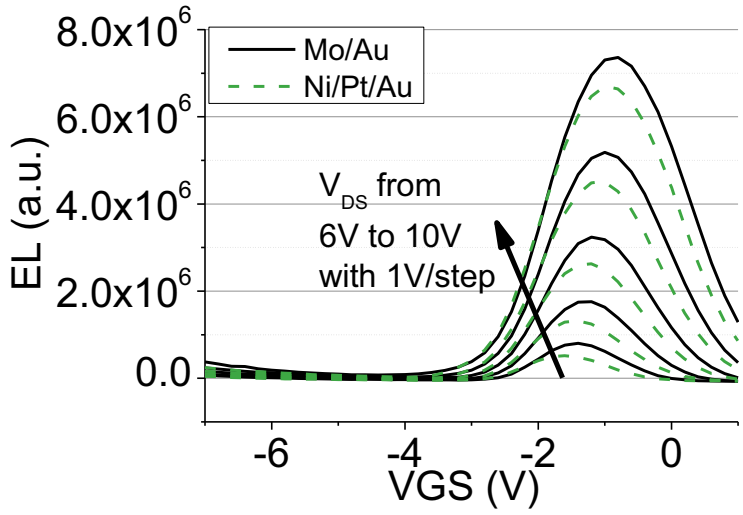


Figure 6.16: electro luminescence comparison in Mo/Au and Ni/Pt/Au devices

Drain current value and corresponding EL as a function of gate source voltage applied is shown for a representative device D1 with Mo/Au and Ni/Pt/Au gate stack (Figure 6.16). The EL describes the usual bell shape trend in both the cases, defining a higher value in Mo/Au devices. Similar results have been reported in the comparison of devices with different geometry, thus demonstrating in all the cases a higher electroluminesce in Mo/Au devices.

A different ratio between EL and ID is stated from the comparison between light emission analysis in Mo/Au and Ni/Pt/Au devices (Figure 6.17). Furthermore, if we compare the ratio of the maximum EL value over the corresponding drain current we can state that a slight higher

ratio value characterizes Mo/Au devices (Figure 6.18). A good reproducibility has been revealed by devices with different geometry.

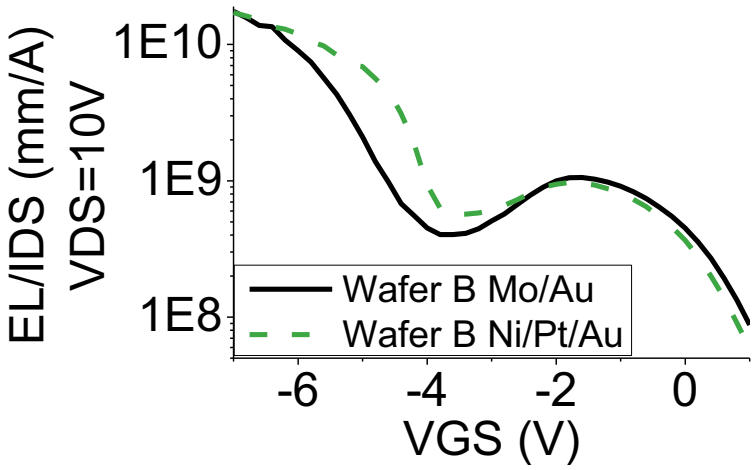


Figure 6.17: EL/ID trend in Mo/Au and Ni/Pt/Au devices measured at VDS=10V

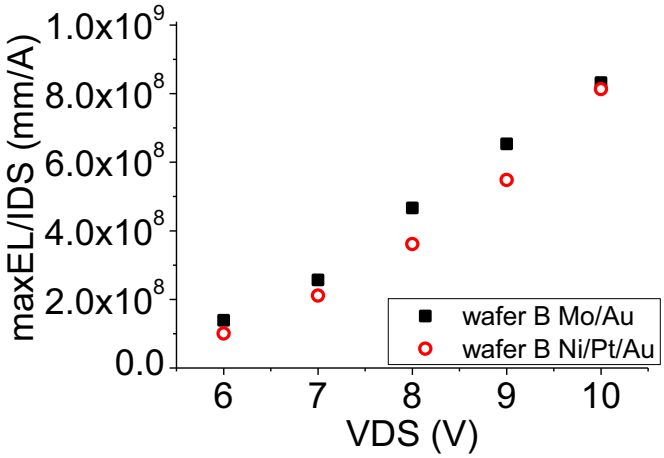


Figure 6.18: max EL/ID ratio or several VDS applied in Mo/Au and Ni/Pt/Au devices

6.2.4 Reliability analysis

Device robustness in terms of reliability analysis has been stated through an OFF state three terminal step stress. The device is kept in OFF condition for 120s each step by the imposition of a bias corresponding to V_{GS}=-6V. The source is kept grounded while a voltage increasing at each step is applied to the drain, from an initial condition V_{DS}=10V to a final one V_{DS}=40V. During step stress several parameters have been measured in order to monitor device degradation. A small number of samples (D1 and D2) has been measured; however similar results are noticed in devices characterized by the same gate stack.

Figure 6.19 shows an example of the current voltage characteristics measured in D2 devices before and after an OFF state step. DC analysis carried out during the stress demonstrates that the use of a Mo/Au gate stack does not influence the device stability, showing no significant improvement to reduce main DC parameters' degradation. A strong drain current degradation is reported in Mo/Au and Ni/Pt/Au devices, showing a higher drain current decrease in the knee voltage zone (about 35% at V_{DS}=3V,V_{GS}=0V) than in saturation region (about 20% at V_{DS}=10V,V_{GS}=0V). In both the cases an analogous drain current decrease has been noticed. Drain current variation is confirmed in Figure 6.20 which shows the drain current percentage variation. Drain current evaluated after more than 100h shows that the drain current degradation is not recoverable neither in Mo/Au nor in Ni/Pt/Au samples.

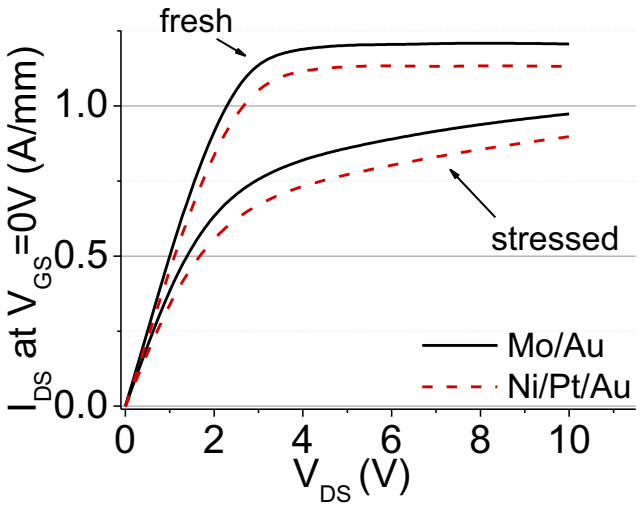


Figure 6.19: : Comparison of the I_{DS} vs V_{DS} curve on fresh and degraded devices after the last step of the stress (V_{DS}=40V, V_{GS}=-6V)

Drain current variation is firstly determined by the degradation of the transconductance peak. The analysis of the transconductance peak variation, evaluated in the knee voltage (V_{DS}=3V) and saturation zone (V_{DS}=10V), states that a significant decrease of 20%-25% and 10%-15% is reached after stress, respectively (Figure 6.21). The comparison between Mo/Au and Ni/Pt/Au samples demonstrates that Mo/Au gate stack does not affect device stability, leading to a degradation trend similar to Ni/Pt/Au.

Drain current variation is only partially determined by the threshold voltage monotonic positive shift consequent to the stress applied. A threshold voltage shift lower than 100-150mV is reported in both the cases analysed (Figure 6.22). A such low value cannot entirely justify the drain current decrease, which is significantly correlated with the transconductance trend. Although in the example reported in Figure 6.22one can hypothesize that Mo/Au reveals a lower shift, we must specify that such difference is lower than variability measured among devices with similar structure and gate stack.

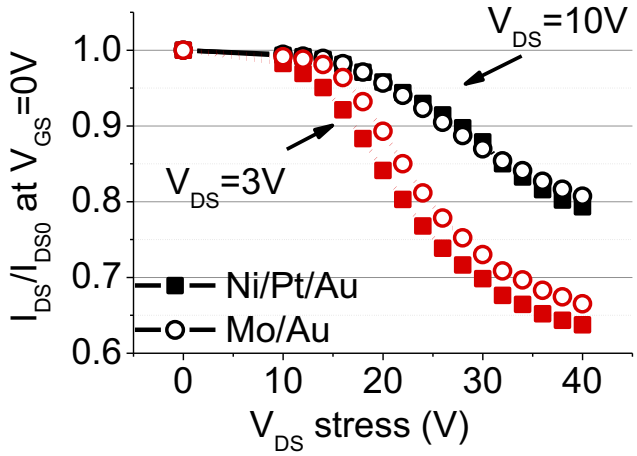


Figure 6.20: : I_{DSS} variation monitored during the stress

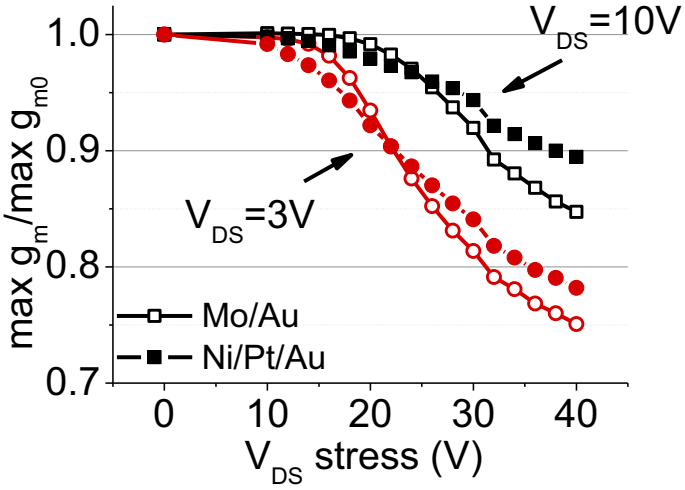


Figure 6.21: Max g_m variation monitored during the stress

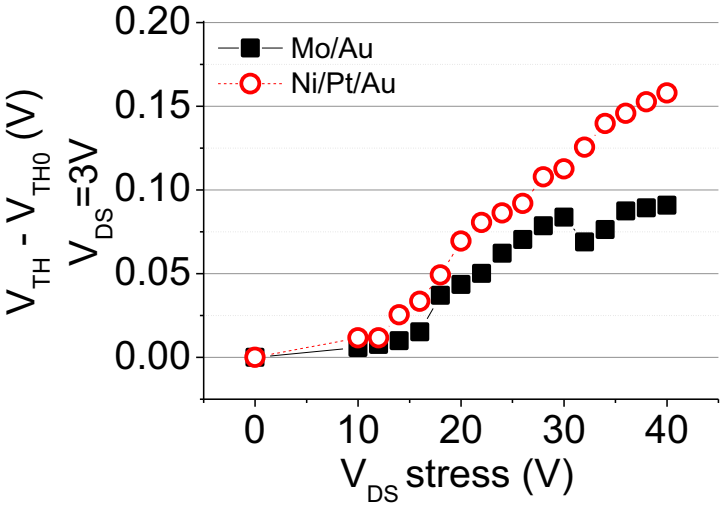


Figure 6.22: : V_{TH} variation monitored during the stress

According to the strong correlation between drain current and maximum transconductance peak we can speculate that the degradation is located in the access regions and mainly due to a degradation of the parasitic resistances.

The analysis of GS diode reverse current shows that no significant difference is reported whatever the gate material (Figure 6.23). On the contrary a quite higher difference is noticed between GS forward diode, showing a quite higher increase of the GS diode forward current when Ni/Pt/Au devices are stressed. The low diode current variation, lower than one order of magnitude, is probably justified by the high diode current measured in fresh device. Consistent results have been measured in transistor leakage gate current measured in OFF and ON state.

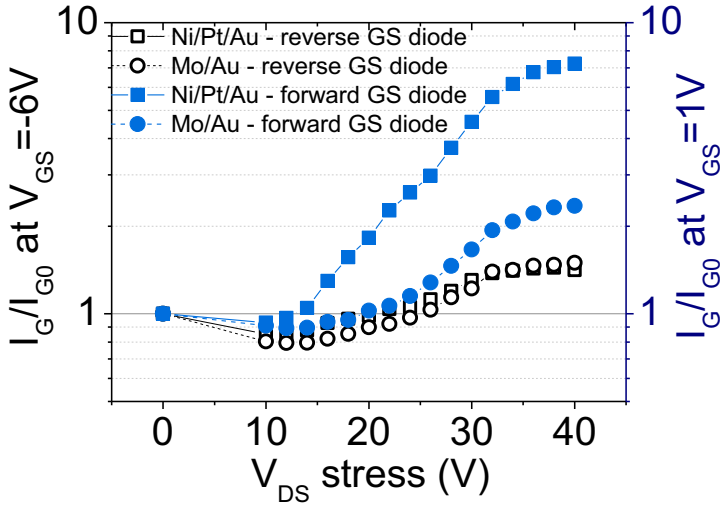
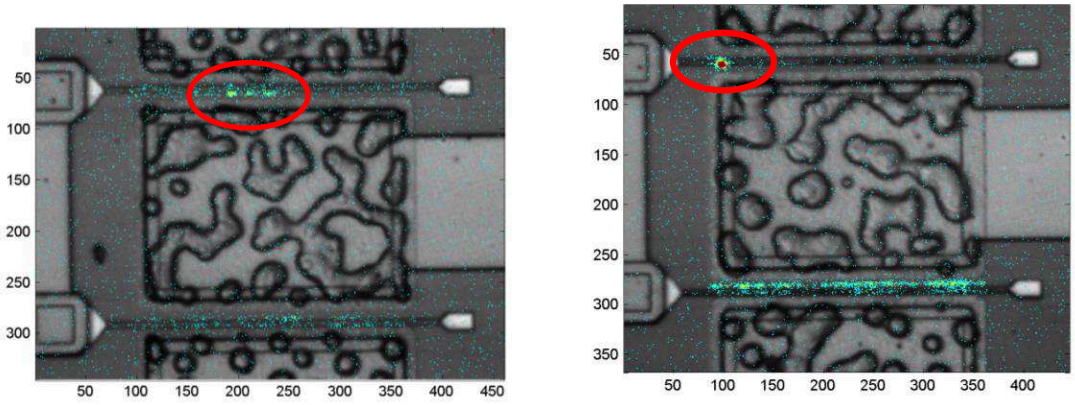


Figure 6.23: GS diode monitored during stress

Emission microscopy has been carried out during the stress and after each step biasing the device in ON and OFF state. The emission microscopy carried out during the OFF state test confirms the gate current behaviour. Furthermore it justifies high leakage gate current value measured in fresh device, revealing a hot spot also in the fresh device. This aspect is confirmed in many devices, both with Mo/Au and Ni/Pt/Au stack. An example is provided in Figure 6.24. No significant change in the hot spots is noticed in the comparison between a fresh device and device after stress, neither in Mo/Au nor in Ni/Pt/Au devices.

Emission microscopy evaluated in ON state is consistent with the drain current decrease monitored during the stress. No significant difference is established in devices with analogous geometry and structure but different gate contact.



(a) (b)

Figure 6.24: light emission measured in OFF state on a fresh device with Mo/Au and Ni/Pt/Au gate

6.3 Improvements provided by the introduction of recess at the ohmic contacts

In literature there are only a few works which describe techniques to improve the ohmic contacts performances in InAlN/GaN structures. One of the main goals is to obtain a structure with a low parasitic resistance. Ohmic contacts, similarly to AlGaN/GaN devices, usually employ a multilayer structure mainly composed by a Ti/Al/Ni/Au alloys generated through an annealing process with a temperature applied in the range between 850°C and 870°C. An interesting design is suggested by Yue et al. [115].

In this chapter it is proposed a solution to decrease parasitic resistances, thus improving device performances. Source and drain contacts are deposited after recess at the ohmic contacts. A comparison of main DC characteristics and trapping behaviour is proposed in structures with and with no recess at the ohmic contacts. The comparison is proposed for two different wafer, characterized by a similar but not analogous structure and different Carbon doping quantity to avoid parasitic leakage current.

DC analysis reveals that no significant improvement is obtained in gate leakage current, both when diodes and transistor are considered. On the contrary, a high variability is stated. A significant variation is noticed in I_{DSS} value, showing that a lower value corresponds to structures with recess at the ohmic contacts. This aspect is mainly due to the fact that a lower on resistance measured in linear zone is not obtained. Drain current behaviour is strongly correlated to transconductance peak trend.

Pulsed analysis states a high current collapse value with no significant correlation with device structure or presence of recess at the ohmic contacts. On the other hand drain current transient reveals important information. Two main traps, labelled T1 and T2, are detected in all the devices. Activation energy, differently from the cross section value, is not influenced by device structure. Consistent results have been measured with gm(f) analysis. On the basis of measurements we have done to define traps properties we can make the hypothesis that T1 is located in the buffer layer while T2 in the barrier layer. Furthermore, from the filling pulse analysis we can demonstrate that both the traps are due to line defects.

6.3.1 Analysed devices

Two structures have been analysed. The first, named wafer A, is an InAlN/GaN HEMT composed by a semi-insulating 4H SiC substrate, a 2.1 µm GaN buffer layer with low C doping, a 7.6 nm InAlN barrier layer with a 18.5% In content. The second, named wafer B, is an InAlN/GaN HEMT composed by a semi-insulating 4H SiC substrate, a 1.8 µm GaN buffer layer with high C doping, a 7.9 nm InAlN barrier layer with a 19.2% In content. In both the cases a 1.5nm AlN interlayer has been grown to enhance the mobility. Furthermore the structure is covered by a SiN passivation layer. The ohmic contacts are composed by a Ti/Al/Ni/Au/Ti/Pt alloy, while the gate schottky contact is composed by Ni/Pt/Au stack. In both wafer A and B half wafer is characterized by the definition of recess before the deposition of the ohmic contacts. A schematic structure is shown in Figure 6.25.

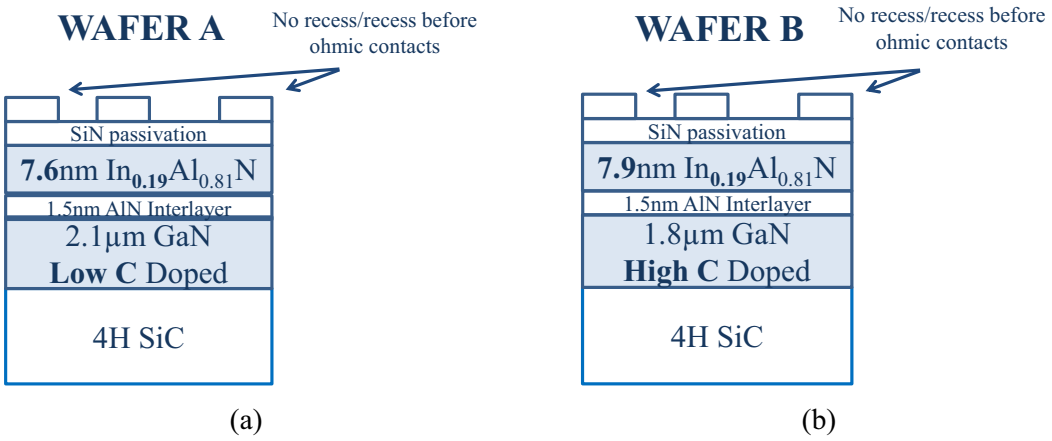


Figure 6.25: schematic structure of wafer (a) A and (b) B, both characterized by recess at the ohmic contacts in half wafer

Both the wafers have the same maskset. It offers three main groups of devices: (i) devices with W_G=2x50 µm and eight different L_G from 0.01µm to 1µm with L_{GD} and L_{GS} scaling with gate length; (ii) devices with W_G=2x380 µm and eight different L_G from 0.01µm to 1µm with L_{GD} and L_{GS} scaling with gate length; (iii) devices with W_G=2x53 µm, L_G=0.15µm, several L_{GS} and L_{GD} value in a range between 0.5 µm and 1.045 µm and between 1 µm and 2 µm, respectively. One set of devices has been analysed and here reported, namely D1. D1 is characterized by W_G=2x50 µm, L_G=0.7 µm, L_{GD}=3.63 µm and L_{GS}=1.67 µm. All the devices are not covered by air bridge. A representative image of analysed devices are shown in Figure 6.26.

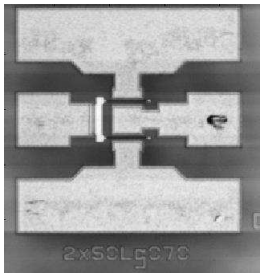


Figure 6.26: representative figure of a D1 sample variation of ohmic contacts

6.3.2 Measurement details

Devices have been characterized with several measurements, in order to clarify the improvements defined by the use of a recess at the ohmic contact and to analyse eventual differences, especially in the trapping behaviour, determined by the carbon doping, although the slight difference in the structure. Main analysis consists of: (i) DC characterization, (ii) pulsed analysis , (iii) drain current transients,

DC Characterization

Devices have been measured with a parameter analyser (Agilent 5260A) and biased with RF tips inside a Karl Suss probe station, in order to avoid oscillations. During the DC characterization the following curves have been evaluated: (i) I-V of the GS diode and I-V of the GD||GS diode evaluated in linear and logarithmic scale; (ii) OUT DC characteristic of the transistor (i.e. I_{DS} vs V_{DS} and I_{GS} vs V_{DS}) measured for V_{GS} from higher to lower values and vice versa in order to study DC trapping; (iii) trans characteristic of the transistor (i.e. I_{DS} vs V_{GS} and I_{GS} vs V_{GS}) measured in linear, knee voltage and saturation zone; (iv) Sub threshold trend (i.e. $\log(I_{DS})$ vs V_{GS}) measured in linear, knee voltage and saturation zone; (v) transconductance (i.e. $\Delta I_{DS}/\Delta V_{GS}$ vs V_{GS}) measured in linear, knee voltage and saturation zone.

Main parameters considered for the analysis are: (i) drain current measured in saturation zone (I_{DSS}) considered both in high dissipation condition (V_{GS}=1V and V_{GS}=0V) and in OFF state (V_{GS}=-6V); (ii) max g_m reported in linear, knee voltage and saturation zone (V_{DS}=1V, V_{DS}=4V, V_{DS}=10V respectively), (iii) transistor gate leakage current measured in OFF and ON state in saturation zone (V_{DS}= 10V and V_{GS}= -6V, V_{GS}=0V and V_{GS}=1V respectively), (iv) diode current measured with reverse and forward bias applied (V_{GS}= -6V, V_{GS}=1V respectively), (v) threshold voltage (V_{TH}) defined as the intercept with the x-axis of the curve tangent the $I_D V_G$.

Pulsed Characterization

Pulsed evaluation has been carried out with a custom setup, defining I_{DS} vs V_{DS} and I_{DS} vs V_{GS} curves by pulsing the drain (V_{DS}) and gate voltage (V_{GS}) from a quiescent bias. Details about measurement setup have been reported in 5.4.1. Three different power dissipation levels from a null trapping condition (V_{GSQ}=V_{DSQ}=0V) to a higher trapping quiescent bias point (V_{GSQ}=-6V, V_{DSQ}=10V) are applied, according to device degradation voltage. A duty cycle of 1% with 1μs pulse width is considered; the measurement is taken in a range between 840-885ns after the pulse is applied. Higher drain voltages imposed during quiescent bias point up to 20V lead not to any DC degradation but to variation of trapping characteristics.

Trapping is quantitatively defined by the variation of the drain current (current collapse), by the shift of the threshold voltage (V_{TH} dynamical shift) and by the on resistance variation measured when different baselines are imposed. The current collapse is measured in knee voltage zone (V_{DS}=4V) at high dissipation (V_{GS}=0V) conditions; V_{TH} dynamical shift is evaluated in a consistent point (V_{DS}=4V) while R_{ON} at V_{GS}=0V.

Drain current transients

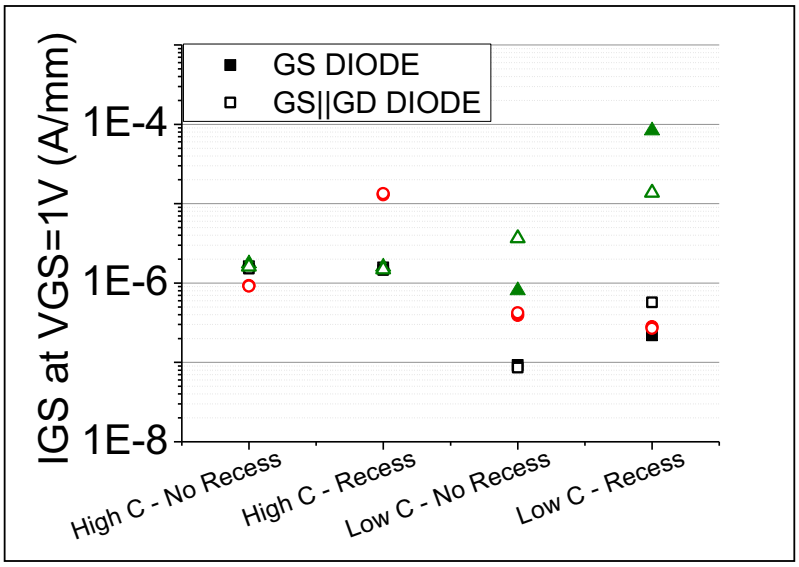
Drain current transients have been measured with a custom setup. Technical details have been provided in 5.4.1. Trapping and de-trapping phase have been imposed for 100s by biasing the device in OFF and ON condition, consistently with pulsed measurements. A bias corresponding to V_{GS}=0V,V_{DS}=4V and V_{GS}=-6V,V_{DS}=10V have been applied, respectively, during the de-trapping and trapping phase. Therefore drain current transient trend is evaluated in a range between 1μs and 100s. Time constants are evaluated through the peak of the derivative function established through the drain current transient; a further comparison with stretched exponential fit is shown. In order to calculate activation energy several ambient temperatures have been imposed, from a minimum of 120°C to 190°C with 10°C step. Drain current transient analysis has been confirmed by means of transconductance frequency dispersion measurements. Filling time analysis has been proposed in order to establish the nature of defects which induce the generation of traps.

6.3.3 DC characterization

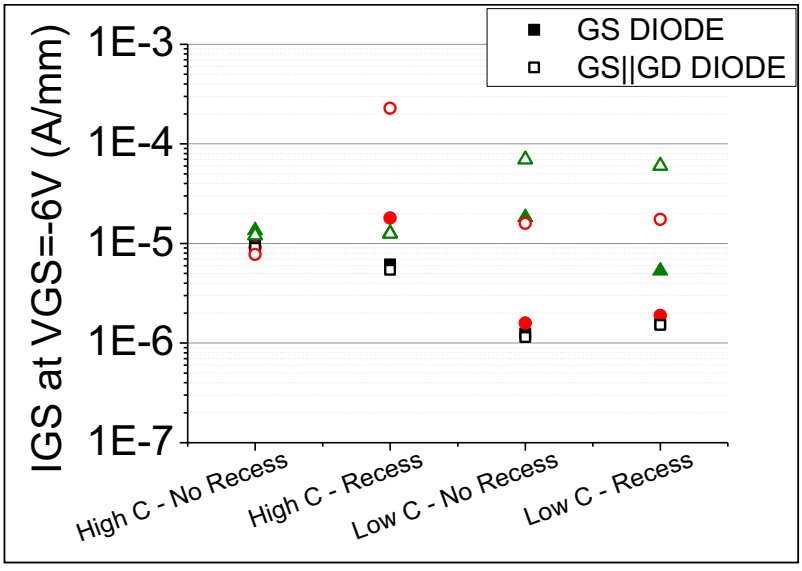
DC Characterization

DC analysis reported in this paragraph deals with evaluation of devices D1 belonging to wafer A and B. A strong reproducibility has been demonstrated in devices with different

geometry (not here reported). The analysis of diode gate current evaluated in the four conditions proposed, i.e. in different wafers and with eventual recess at the ohmic contacts, reveals the strong variability among devices with analogous structure. This aspect can be noticed both when a reverse or a forward bias is applied (Figure 6.27). Furthermore, no significant correlation with carbon doping or recess at the ohmic contacts is reported.



(a)



(b)

Figure 6.27: comparison of diode (a) forward and (b) reverse current in devices with different carbon doping and presence of recess at the ohmic contacts

An example of diodes measured in the four conditions is reported in Figure 6.28. In all the cases considered diode reverse and forward current reveals a quite low value in the order of magnitude of 1μA/mm and 10μA/mm when forward and reverse voltage is applied,

respectively. The evaluation of transistor gate leakage current measured in saturation zone in OFF and ON condition shows consistent results, demonstrating a value of 1μA/mm and 100μA/mm when measured at V_{GS}=0V and V_{GS}=-6V, respectively.

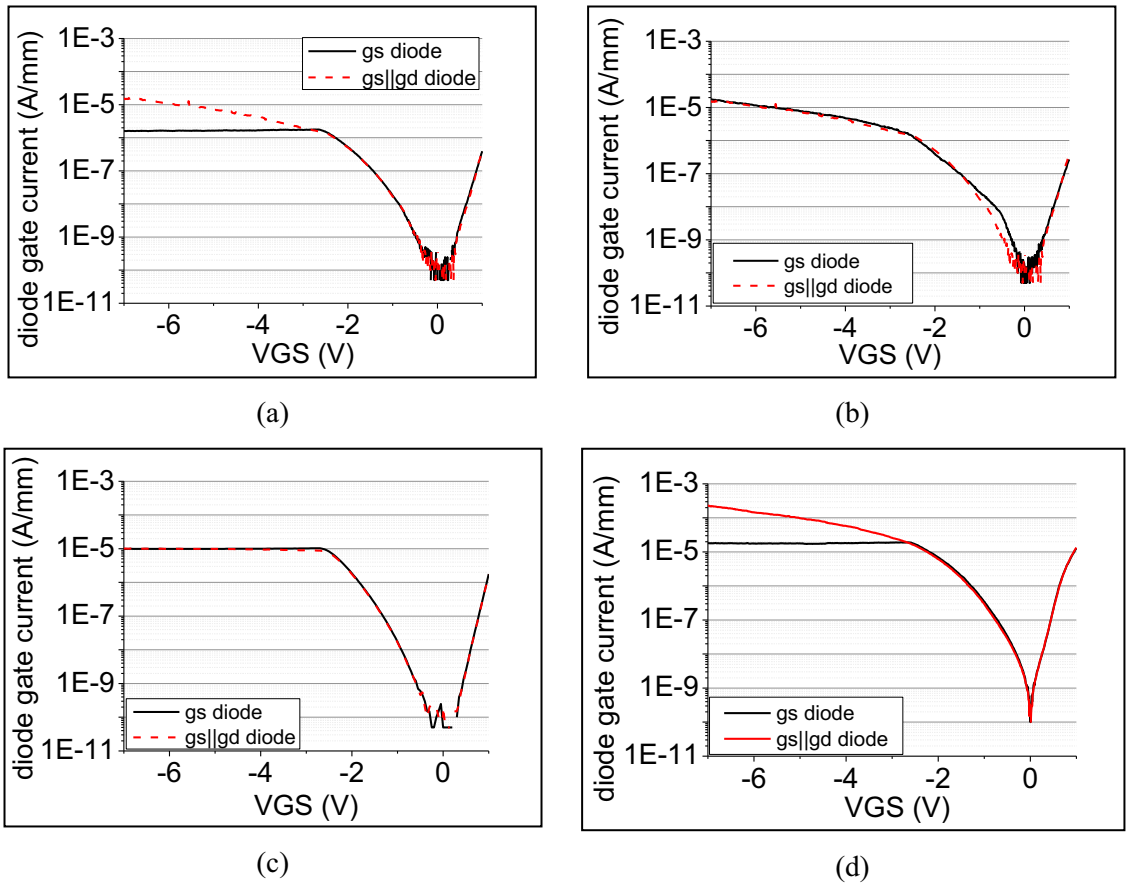


Figure 6.28: GS and GS||GD diode current for a representative device for the four conditions presented: (i) wafer A, no recess at the ohmic contacts, (ii) wafer A, recess at the ohmic contacts, (iii) wafer B, no recess at the ohmic contacts, (iv) wafer B, recess at the ohmic contacts

A significant correlation is noticed in drain current measured at high dissipation condition (Figure 6.29). Furthermore, except for devices with recess at the ohmic contacts belonging to wafer A, no strong variability is stated. Recess at the ohmic contacts leads to a lower drain current value both when wafer A and wafer B is considered. Furthermore a higher I_{DSS} is measured in wafer A; this aspect can be ascribed to the slight difference in barrier layer thickness and the high discrepancy in Indium content (i.e. 18.5% and 19.2%) in the two wafers.

Drain current variation as a function of wafer structure is mainly due to max g_m and R_{ON} variation (dashed line is a guide for the eye). This behaviour is better explained from the comparison of drain current vs voltage trend reported for four representative devices (Figure 6.31). Differently from the maximum transconductance evaluated in knee voltage and saturation zone, max g_m considered in linear zone does not change significantly with device structure. It is

important to highlight that, although a quite low difference is noticed, the recess at the ohmic contacts leads to a higher on resistance value measured in linear zone.

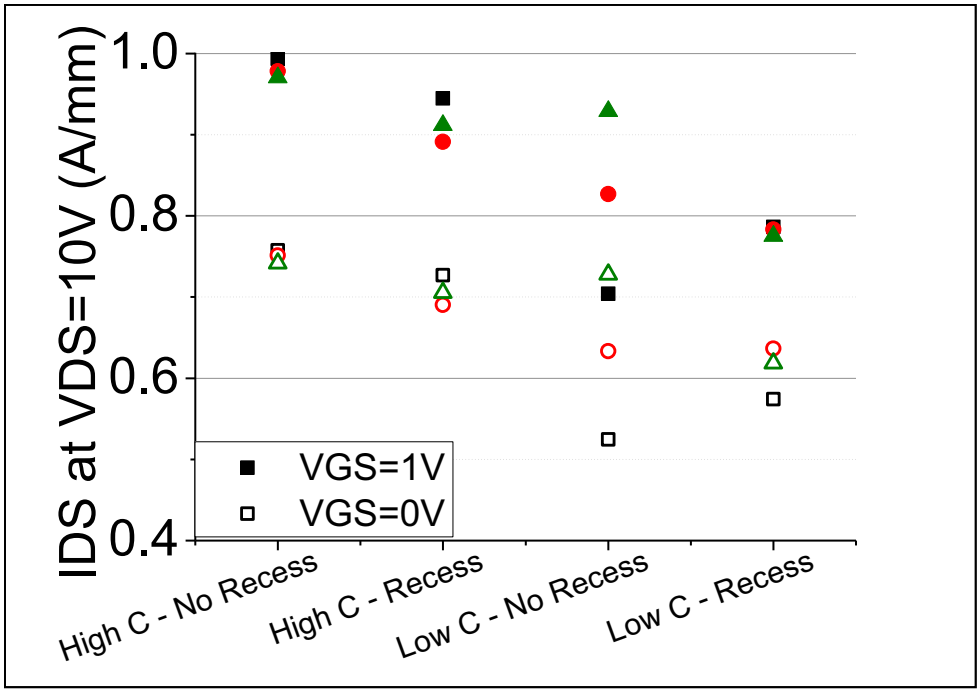
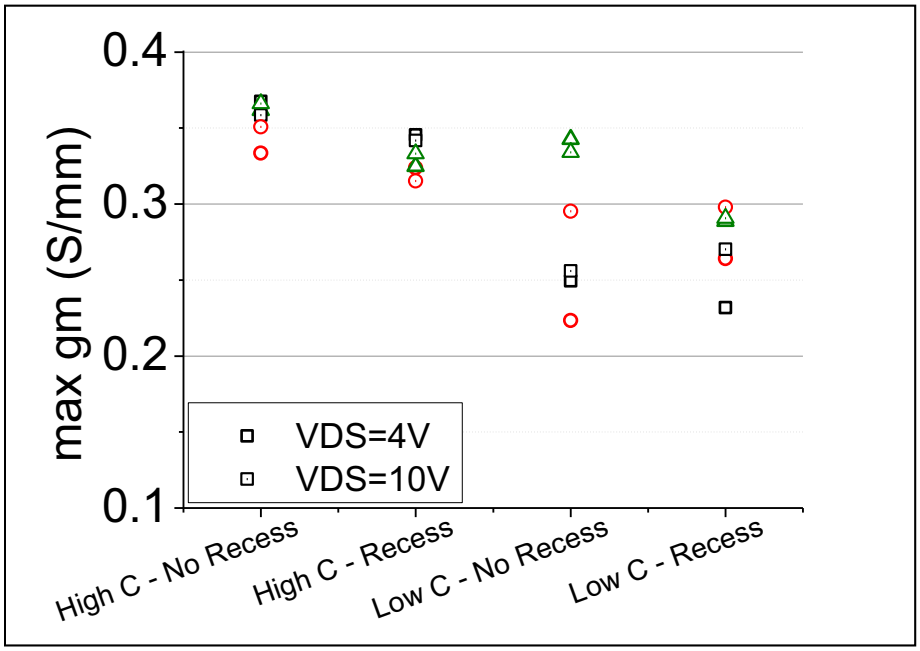
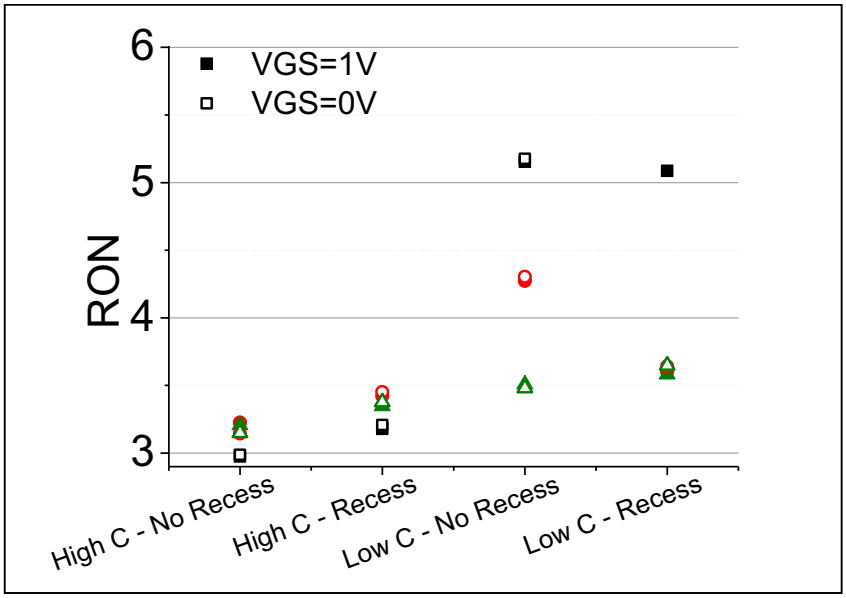


Figure 6.29: : comparison of IDSS in devices with different carbon doping and presence of recess at the ohmic contacts



(a)



(b)

Figure 6.30: comparison of (a) transconductance peak in knee voltage and saturation zone and (b) RON measured at high dissipation condition in the four conditions proposed

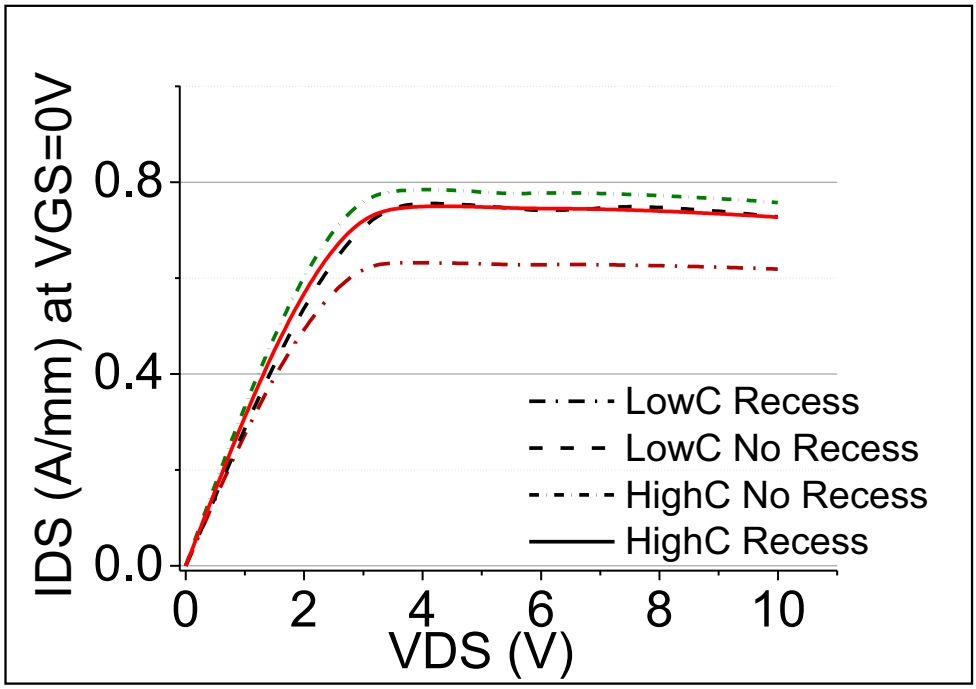
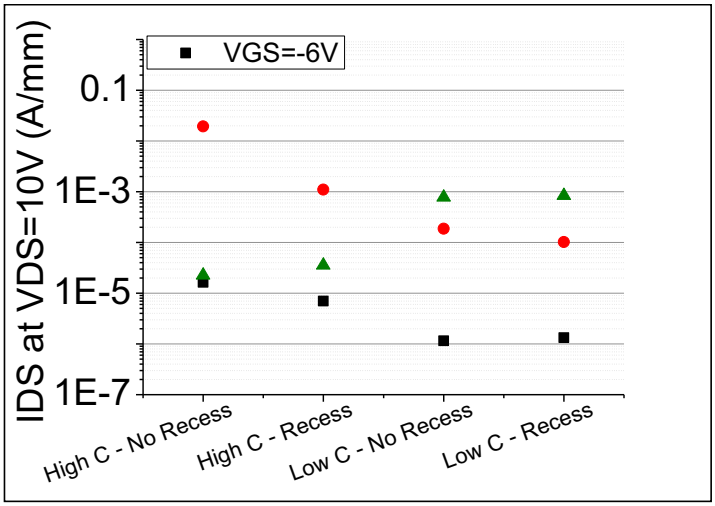
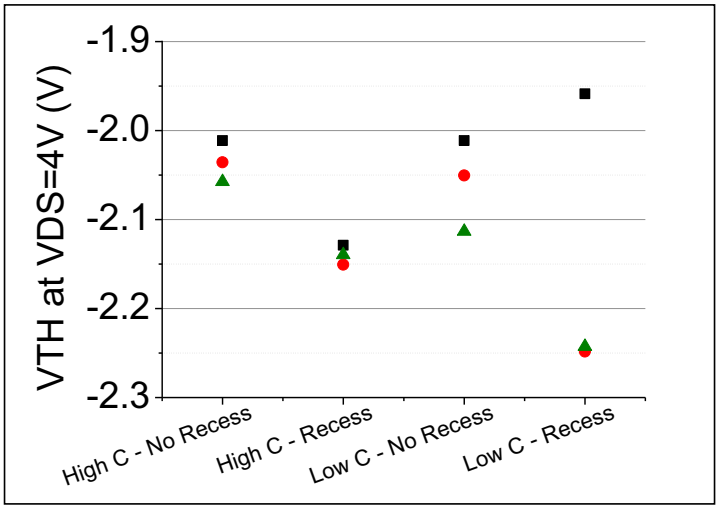


Figure 6.31: output IDVD curve describing a representative sample for the four conditions proposed

On the contrary no significant correlation between recess at the ohmic contact and threshold voltage shift is established (Figure 6.32). Similar considerations can be done for the transistor leakage drain current measured in OFF state. In this last case a strong variability is noticed in devices considered, although characterized by analogous structure. A detailed I_DV_G curve for four representative devices is shown in [Figure 6.33]



(a)



(b)

Figure 6.32: comparison of (a) leakage drain current and (b) threshold voltage in different conditions

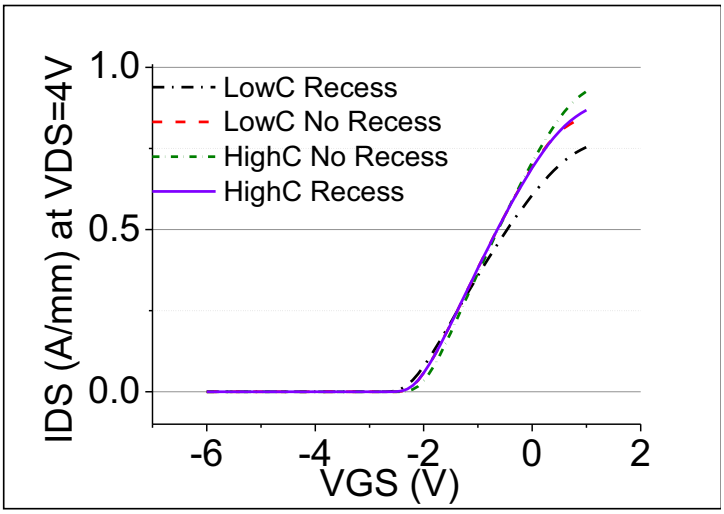
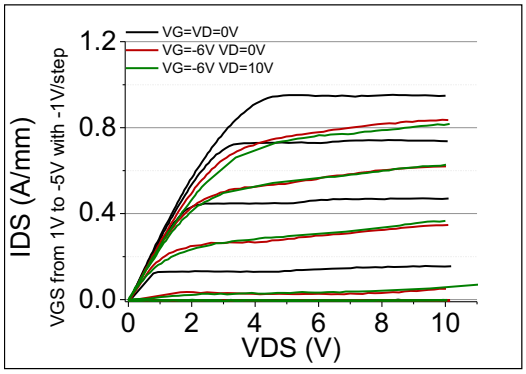


Figure 6.33: IDVG curve describing a representative sample for the four conditions proposed

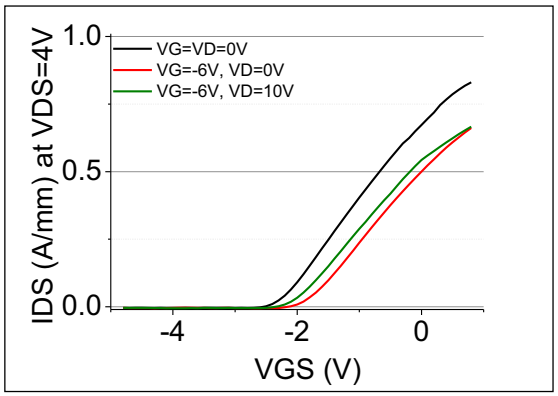
6.3.4 Trapping behaviour

Pulsed analysis

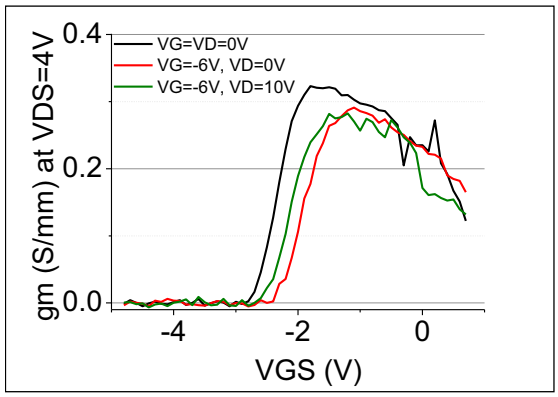
In Figure 6.34 an example of pulsed characterization is reported for a representative device D1 belonging to wafer B and characterized by recess at the ohmic contacts. Similar results have been reported in devices with different structure or with no recess at the ohmic contacts. From the I_DV_D curve it is possible to notice a drain current dispersion due to trapping effects; analysis of the I_DV_G and g_mV_G demonstrates that current collapse is partially due to threshold voltage dynamical shift and partially to a dynamical decrease of the maximum transconductance value. Furthermore a significant variation of the R_{ON} value is noticed.



(a)



(b)



(c)

Figure 6.34: pulsed analysis on a representative device D2 with recess at the ohmic contacts: (i) IDVD, (II) VTH, (iii) gm

From the comparison of the current collapse measured in devices with different structure and different ohmic contacts structure it is possible to determine the following statements: (i) no significant variation is noticed between the second and the third baseline, leading to the assumption that the imposition of a negative voltage to the gate terminal, even if with null drain voltage, determines a strong trapping condition. No significant variation in trapping effects is

introduced by the variation of drain voltage during quiescent bias point and, thus, by a further increase of the electric field generated between the gate and the drain terminal. (ii) all the devices reported a very high current collapse value, in many cases near 50%, as it is possible to state in Figure 6.35.

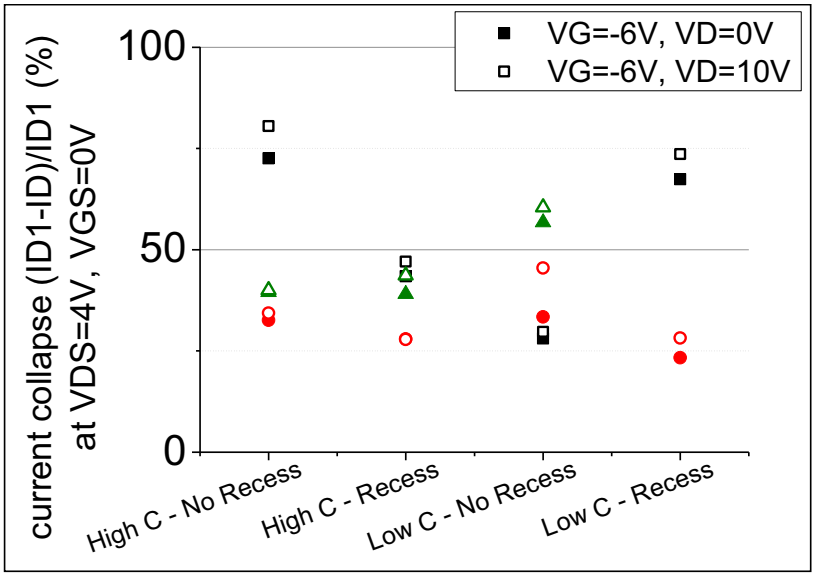
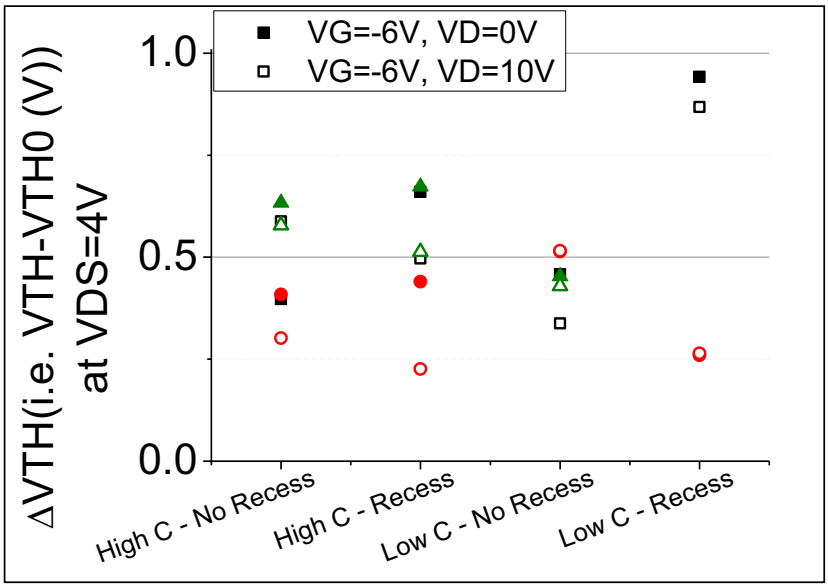
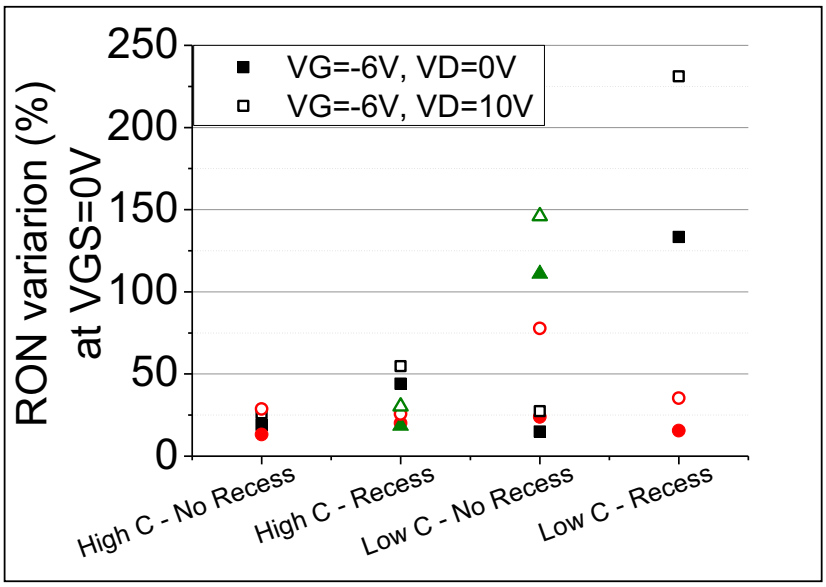


Figure 6.35: current collapse evaluated in different structures for different bias point applied during the quiescent bias point



(a)



(b)

Figure 6.36: (VTH dynamical shift and (b) RON variation evaluated in different structures for different bias point applied during the quiescent bias point

(iii) The drain current dispersion, consistently with $I_D V_G$ and $g_m V_G$ analysis, is consistent with the high V_{TH} dynamical shift and transconductance peak variation reported (Figure 6.36). (iv) Although devices are defined by an analogous structure, a strong variability is reported. On the contrary no correlation with wafer structure is shown. (i.e. buffer doping, barrier layer In content, or with eventual recess at the ohmic contacts).

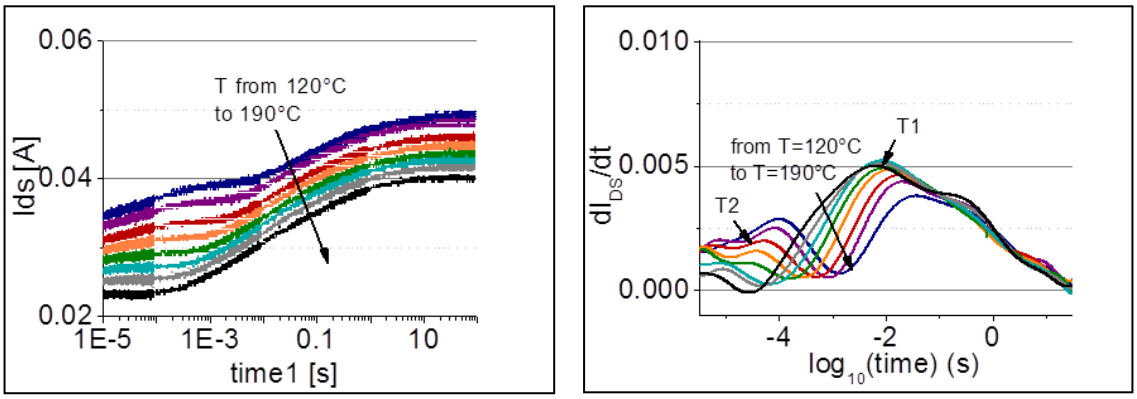
Drain current transients

Drain current transients revealed several differences among devices characterized by a different structure or recess at the ohmic contacts. Main results are: (i) a strong reproducibility in all the devices measured if characterized by the same structure; (ii) different time constants on the basis of structure considered; (iii) no variation of the activation energy but only of the cross section detected ; (iv) consistency with different measurements such as transconductance frequency dispersion; (v) two main thermally activated traps, labelled T1 and T2, are detected. A third trap, with much lower amplitude and in some cases with no thermal variation is detected. (vi) $g_m(f)$ measurements and works reported in literature let us make the hypothesis that T2 is located in the buffer layer, while T1 is probably located in the barrier layer. (vii) the analysis of transient data as a function of filling time revealed that trapping effects should be related to line defects.

In the following drain current transient and the corresponding derivative function to detect traps time constants are reported for one representative sample for each structure. Furthermore the corresponding Arrhenius plot is reported in order to demonstrate the correlation between

drain current transients evaluated with stretched exponential, with the peak of the derivative function and gm(f) analysis. Through the Arrhenius plot the activation energy is thus defined.

In Figure 6.37 drain current transient for a representative sample belonging to wafer A with no recess at the ohmic contacts is explained. Two traps are detected, with a time constant of almost 0.01s and 0.1ms respectively at T=120°C. Both traps are thermally activated. A third trap, corresponding to almost 0.1s is not thermally activated, although reported for all the temperatures measured.



(a) (b)

Figure 6.37: (a) drain current transient and (b) corresponding derivative function in a device of wafer A with no recess at the ohmic contacts

Figure 6.38 reports the corresponding Arrhenius plot. Time constants have been evaluated both with derivative and stretched exponential method, demonstrating no significant variation in the two techniques considered. Two main traps are detected; both traps are thermally activated with E_a=0.85 and 0.94eV respectively. One trap, revealed only by stretched exponential function and described by red squares, is an artefact introduced to obtain a better fitting with stretched exponential. When a lower order is used in the fit no significant variation in traps time constants is noticed.

$G_m(f)$ analysis detects only one trap, which shows a good correspondence with trap T2. From the comparison with further works reported in literature we can make the hypothesis that the trap labelled as T2 is probably located in the buffer layer. Unfortunately any wafer with no carbon doping has been evaluated, in order to accurately demonstrate the relationship between T2 and carbon. On the other hand, according to the description of the $g_m(f)$ provided in 5.4.1 and on the bias point imposed during measurements, $g_m(f)$ evaluation analyses a region corresponding to the buffer layer or far from the interface, on the basis of the justification provided by Silvestri et al. [77]. Therefore, considering that $g_m(f)$ detected only one trap corresponding to trap T2 we can speculate that it is located in the buffer layer.

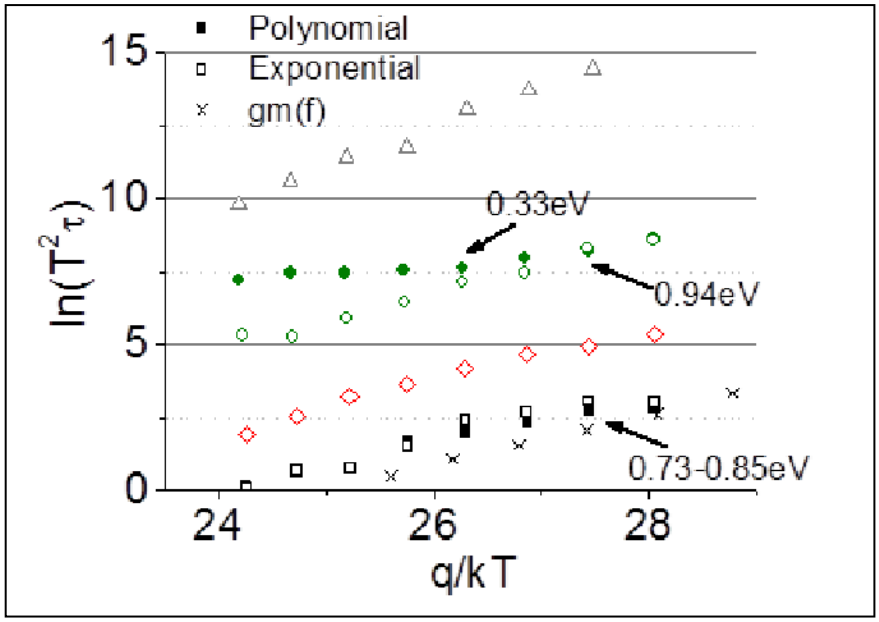
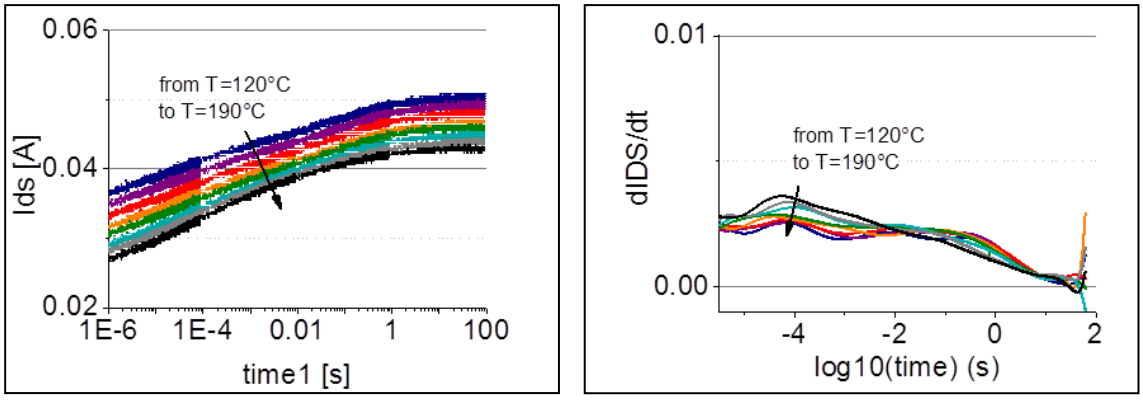


Figure 6.38: Arrhenius plot corresponding derivative function in a device of wafer A with no recess at the ohmic contacts

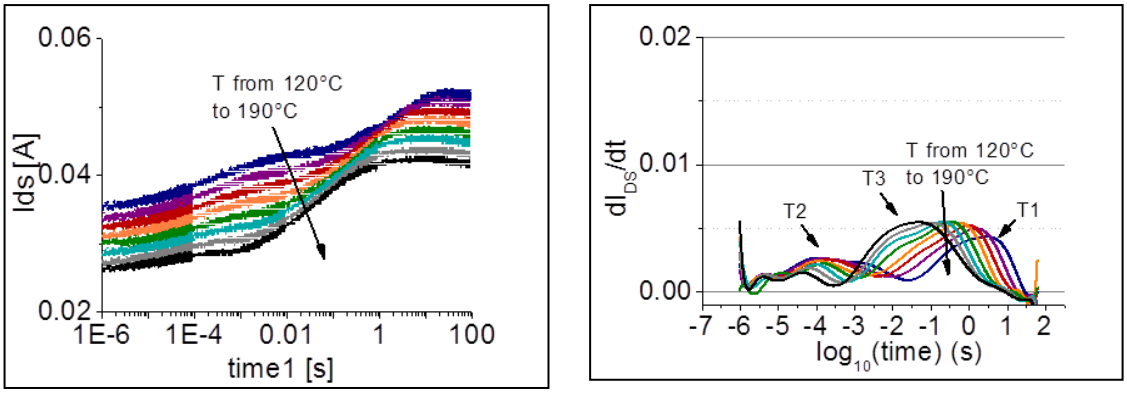


(a) (b)

Figure 6.39: (a) drain current transient and (b) corresponding derivative function in a device of wafer A with recess at the ohmic contacts

Devices belonging to wafer A and characterized by a recess at the ohmic contacts did show no relevant peak in the derivative function. It was not possible to measure traps time constant neither with drain current transients nor with $g_m(f)$ analysis. Figure 6.39 describes the drain current transient and derivative function of a representative device.

Figure 6.40 describes the drain current transient and derivative function of a representative device belonging to wafer B with recess at the ohmic contacts. Two traps are detected, with a time constant of almost 1s and 1ms respectively at T=120°C. A third trap, with lower amplitude intensity, is noticed at higher time constants.



(a) (b)

Figure 6.40: (a) drain current transient and (b) corresponding derivative function in a device of wafer B with recess at the ohmic contacts

All the three traps are thermally activated (Figure 6.41). The first and the second trap have an activation energy of, respectively, E_a=0.85 and 0.7eV. Concerning $g_m(f)$ analysis and correspondence between peak of the derivative function and stretched exponential analysis, considerations done for device belonging to wafer A with no recess at the ohmic contact can be taken into account.

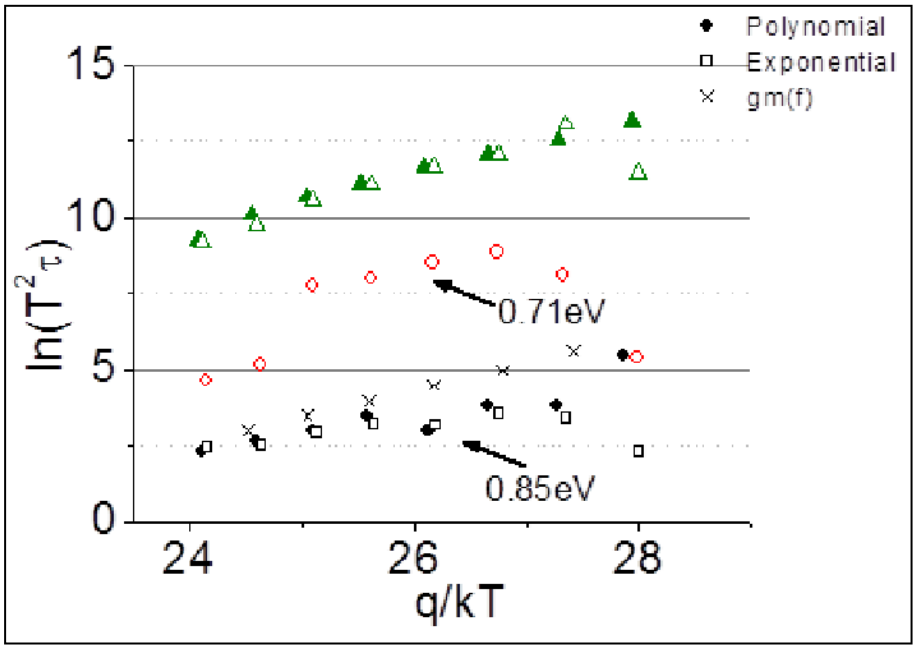
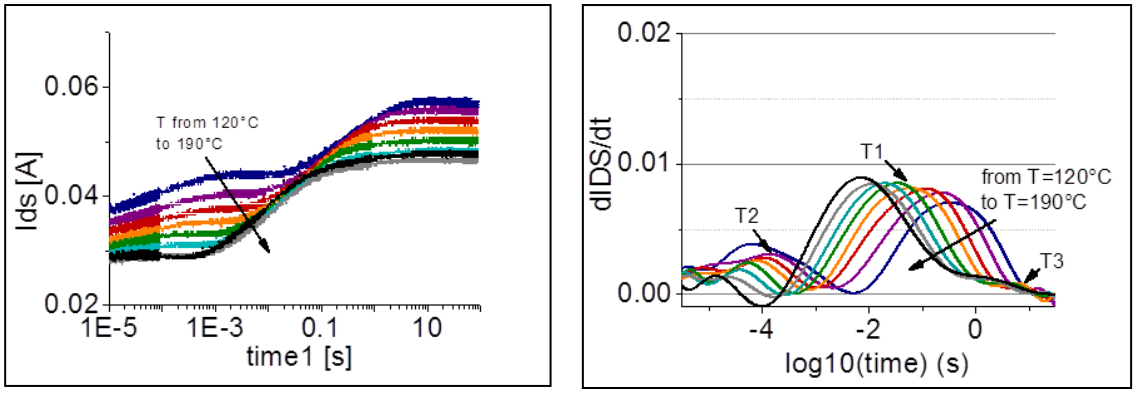


Figure 6.41: Arrhenius plot corresponding derivative function in a device of wafer B with recess at the ohmic contacts

Figure 6.42 describes the drain current transient and derivative function of a representative device belonging to wafer B with recess at the ohmic contacts. Two traps are detected, with a time constant of almost 0.3s and 0.2ms respectively at T=120°C. A third trap, with lower

amplitude intensity, is noticed at higher time constants. All the three traps are thermally activated.



(a) (b)

Figure 6.42: (a) drain current transient and (b) corresponding derivative function in a device of wafer B with recess at the ohmic contacts

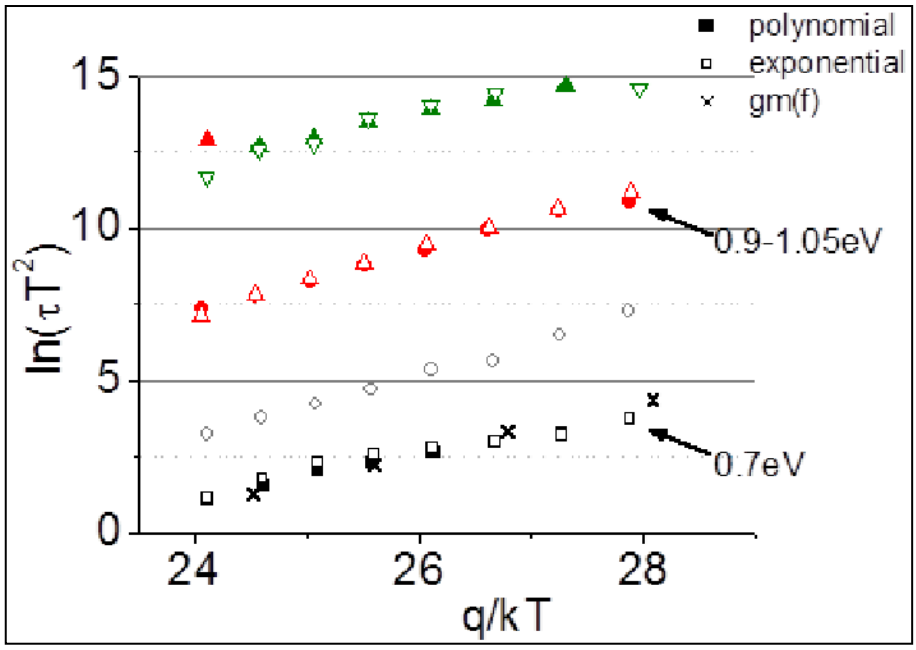


Figure 6.43: Arrhenius plot corresponding derivative function in a device of wafer B with recess at the ohmic contacts

The first and the second trap have an activation energy of, respectively, E_a=0.7 and 0.9-1.05eV. It is important to notice that, also in this case, a strong correlation between g_m(f) analysis and drain current transient is stated, thus indicating the possible location of trap T2 in the buffer layer (Figure 6.43).

As previously described in detail, a difference in the structure leads to a significant difference in the time constants, with a consistent variation of the corresponding cross section.

This difference is demonstrated in Figure 6.44 where the Arrhenius plot defined by $g_m(f)$ measurements and drain current transients is shown. Figure 6.43 also confirms that, although the variation in the time constant measured at T=120°C, no variation of the activation energy is measured. Figure 6.43 finally allows to demonstrate the strong correlation between $g_m(f)$ and drain current transients analysis and the strong reproducibility among devices with analogous structure. Each different symbol in Figure 6.43represents a different sample measured.

According to information provided in 5.4.1 concerning the relationship established between the amplitude of traps with different filling time and nature of defects, we can make the hypothesis that trap T2 is due to line defects. Indeed in all the structures analysed, except for device A with recess as the ohmic contacts, trap corresponding to trap T2 decreases with filling time following a logarithmic trend. In Figure 6.45.different symbols represent different samples belonging to wafer B with no recess at the ohmic contacts. Consistent results have been noticed in devices with different structure or recess at the ohmic contacts. No relevant variation in trap time constant is noticed.

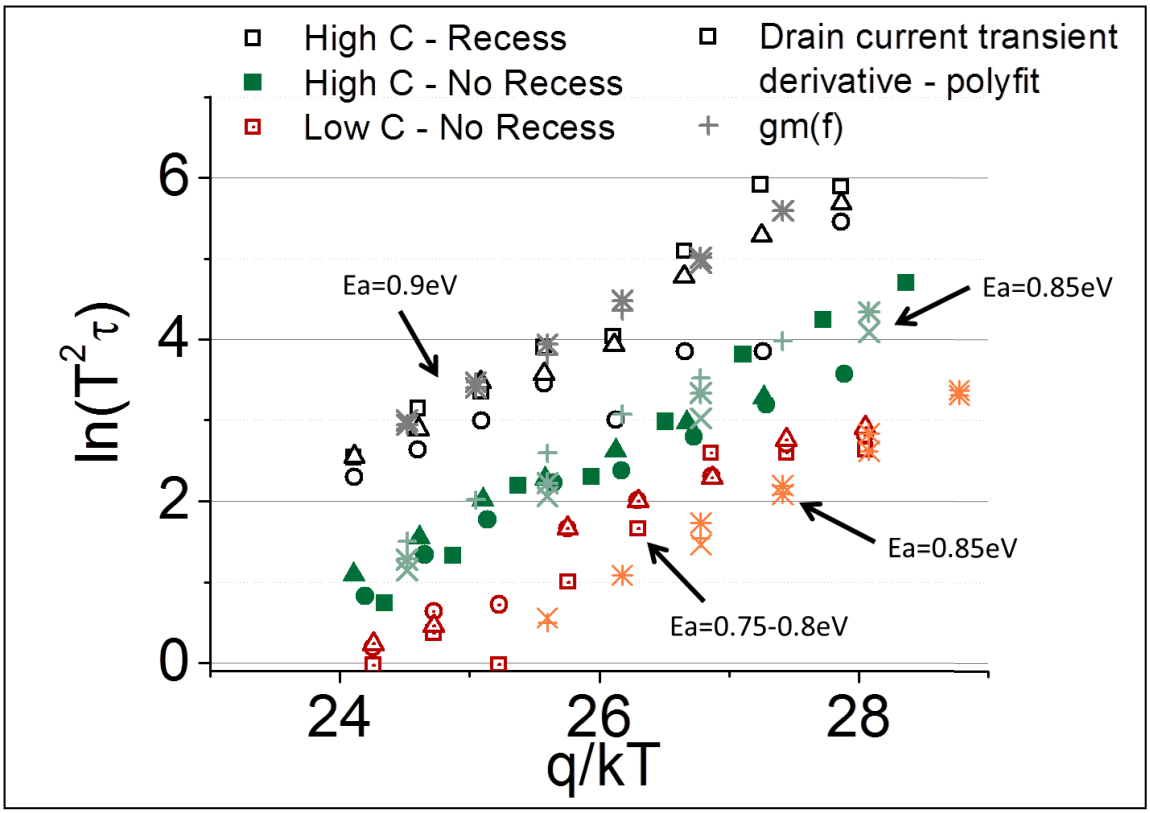
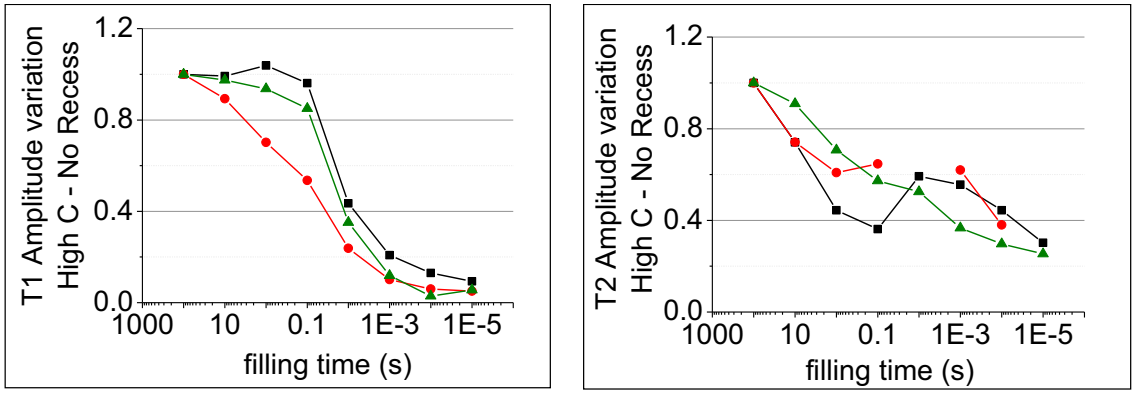


Figure 6.44: $g_m(f)$ and drain current transients evaluated for several devices with different structure



(a) (b)

Figure 6.45(a) trap T1 and (b) trap T2 variation as a function of filling time in a device of wafer B with no recess at the ohmic contacts

Conclusions

The main aim of the thesis is to evaluate reliability issues in several materials used for High Electron Mobility Transistors growth. Therefore the analysis focuses on the understanding and comparison of limits and performances due to the use of materials with different properties. Three typologies of discrete devices are mainly discussed: (i) gallium arsenide pseudomorphic HEMT; (ii) AlGaN/GaN HEMT with iron doping in the buffer layer; (iii) InAlN/GaN based structures with improvements at the Schottky and ohmic contacts. In order to further study in detail the behaviour of real commercial application the investigation on GaAs pHEMTs has been extended to GaAs MMIC four stages power amplifiers.

Four topics have been discussed and can mainly be summarized as follows: (i) Thermal degradation of GaAs devices; (ii) Electrostatic discharge on GaAs MMIC power amplifiers; (iii) Trapping phenomena on AlGaN/GaN HEMTs with Fe doping in the buffer layer and correlation with degradation effects during a reverse bias step stress; (iv) improvements provided by the use of an InAlN/GaN structure.

Thermal degradation of GaAs devices has been studied through a long term thermal stress on pHEMTs and long term HTOL where MMIC power amplifiers are stressed both with temperature and bias. The first analysis (i.e. long term thermal stress) states that degradation can be ascribed to three degradation mechanisms: (i) gate metal interdiffusion or gate sinking, demonstrated through the V_{TH} positive shift; (ii) ohmic contacts degradation, accompanied by the transconductance peak decrease and end resistances increase; (iii) degradation of the Schottky barrier height. The third mechanism, which prevails to the gate sinking after a defined amount of hours, leads to a not monotonic trend in drain current and V_{TH} degradation.

The second evaluation (i.e. long term HTOL test) shows that no significant effect is noticed if a junction temperature lower or equal to 250°C is reached. Furthermore, we can hypothesize that channel temperature has been underestimated on the basis of the comparison of V_{TH} degradation in the two tests.

The comparison among techniques compared to estimate a reliable channel temperature in pHEMTs demonstrates that DC and pulsed method show consistent results; on the other hand temperature is significantly underestimated with IR method. Analysis on the MMIC power amplifier confirms this statement; however it also explains that IR technique can estimate mutual interaction among stages in a simple way, demonstrating that mutual interaction decreases with device periphery.

Electrostatic discharge on GaAs MMIC power amplifiers states that auxiliary circuits are the most sensitive pads in the structure, with a HBM and MM degradation voltage of 250V and 25V, respectively, due to the failure of integrated resistances. Drain connection and RF circuitry show no degradation up to 2kV HBM and 200V MM. However TLP analysis reveals that degradation occurs in correspondence to a current of 6.5-7A, leading to an open circuit in the inductance of the resonant ESD protection circuit. Gate terminals show a robustness lower than 1kV and 50V in HBM and MM. Failure of the schottky diode protection structure is noticed.

Trapping phenomena analysis on AlGaN/GaN HEMTs with Fe doping in the buffer layer shows two main traps, T1 and T2, with an activation energy of 0.57eV and 0.74eV if self-heating effects are not considered, consistently with previous works reported in literature. Iron doping determines a measurable current collapse which is related to the presence of a trap (T1) located in the buffer layer, while no significant variation in the activation energy is noticed. The amplitude of trap T1 in devices with different structures suggests that the trap is due to an intrinsic defect in the buffer layer characteristic of GaN, although its concentration strongly depends on buffer doping quantity. The second trap T2 is probably located in the AlGaN. Current transients with different filling pulses applied suggest that trapping is due to line defects.

The electrical stress on devices with and with no Fe doping indicates that (i) a gate leakage current increase is noticed and it is correlated to light emission; (ii) beyond not recoverable degradation a significant correlation is established also with current collapse value; (iii) current collapse is due to an increase in the transient signal associated with the pre-existing trap levels, without the generation of new traps.

Correlation between degradation effects with different Fe doping buffer layer demonstrates that all the devices show a significant and not reversible increase in gate leakage current and in current collapse, even if correlation established in devices with and with no Fe doping follows different trends. Trap variation is not due to new traps levels. The hypothesis is that: change in the signal of T_2 may be due to an increase in the concentration of a defect (T_2), while the change of T1 is defined by generation of defect-related conductive paths between the gate and the channel.

Improvements due to the use of an InAlN/GaN structure are studied with two main analysis: (i) use of a different material for the Schottky gate contact (Mo/Au instead of Ni/Pt/Au); (ii) definition of a recess before the deposition of ohmic contacts to reduce parasitic resistances. In the first case, although no significant variation is noticed during DC analysis, pulsed evaluation demonstrates that the use of a Mo/Au gate contact leads to an improvement of trapping characteristics. Current collapse is mainly due to V_{TH} dynamical shift, thus we can suppose that traps are probably located under the gate. A Mo/Au gate stack improves trapping

conditions mainly due to the process used for contact deposition. By means of a three terminals step stress it is finally proved that Mo/Au does not significantly affect device stability.

The second analysis demonstrates that a significant variation is noticed in I_{DSS} DC value, with a lower value in structures with recess at the ohmic contacts. This demonstrates that a lower on resistance measured in linear region is not achieved by the presence of recess at the ohmic contacts. Pulsed analysis reveals a high current collapse value, not correlated to the structure, which is partially due to V_{TH} shift and partially to max g_m and R_{ON} variation. Drain current transient reveals two main traps, labelled T1 and T2. Device structure and recess influence both time constants and cross section, while no variation in the activation energy is measured. Previous works reported in literature and $g_m(f)$ analysis suggest that T1 is probably located in the barrier layer, while T2 in the buffer. Unfortunately there was no device with no carbon doping to state the influence of carbon doping on traps amplitude. Filling time measurements indicate that both the traps are mainly due to line defects.

List of Publications

Journals

Rossetto I, Meneghini M., Meneghesso G., Zanoni E., "*Reverse-bias stress of high electron mobility transistors: Correlation between leakage current, current collapse and trap characteristics*", Microelectronics Reliability special issue conference ESREF 2013, vol. 53 (2013), 1456-1460

Rossetto I., Rampazzo F., Silvestri R., Zanandrea A., Dua C., Delage S., Oualli M., Meneghini M., Zanoni E., Meneghesso G., "*Comparison of the performances of an InAlN/GaN HEMT with a Mo/Au gate or a Ni/Pt/Au gate*", Microelectronics Reliability special issue conference ESREF 2013, vol. 53 (2013), 1476-1480

Meneghesso G., Meneghini M., Stocco A., Bisi D., De Santi C., Rossetto I., Zanandrea A., Rampazzo F., Zanoni E., *"Degradation of AlGaN/GaN HEMT devices: Role of reverse-bias and hot electron stress",* Microelectronics Engineering, vol. 109 (2013), pp. 257-261

Meneghesso, G., Meneghini, M., Bisi, D., Rossetto, I., Cester, A., Mishra, U.K., Zanoni, E., "*Trapping phenomena in AlGaN/GaN HEMTs: A study based on pulsed and transient measurements*", Semiconductor Science and Technology, vol. 28 (2013) issue 7

Rossetto I., Meneghini M., Tomasi T., Yufeng D., Meneghesso M, Zanoni E., "*Indirect techniques for channel temperature estimation of HEMT microwave transistors: Comparison and limits*" , Microelectronics Reliability special issue conference ESREF 2012, vol. 52 (2012), p. 2093-2097

Tazzoli A., Rossetto I., Zanoni E., Yufeng D., Tomasi T., Meneghesso G., "*ESD sensitivity of a GaAs MMIC microwave power amplifier*", Microelectronics Reliability special issue conference ESREF 2011, vol. 51 (2011), pp.1602-1607

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