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CICLO XXVI

ANALYSIS OF DEFECTS AND PHYSICAL MECHANISMS THAT LIMIT THE ESD ROBUSTNESS OF LIGHT EMITTING DIODES

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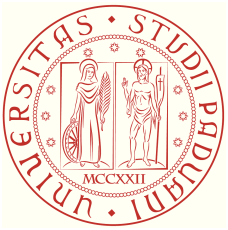

Scuola di Dottorato di Ricerca in Ingegneria dell'Informazione
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Analysis of defects and physical mechanisms that limit the ESD robustness of Light Emitting Diodes

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Contents

Abstract

This thesis reports the main results obtained from the Ph.D. research activity of the candidate. The activity was focused on the study of defects and physical mechanisms that limit the ESD robustness of Light Emitting Diodes (LEDs). In particular, most of the research activity was mainly focused on the analysis of GaN-based LEDs, which are the basis for the realization of blue and UV emitters, and white LEDs based on phosphor conversion.

After an initial overview on the most important theoretical concepts necessary for the understanding of physical results, four main sections can be identified in this thesis, concerning the presentation of research activity:

- First, we report an extensive analysis of the defect-related localized emission processes occurring in InGaN/GaN-based light-emitting diodes at low reverse and forward-bias conditions. The analysis is based on combined electrical characterization and spectrally and spatially resolved electroluminescence (EL) measurements. Results of this analysis show that: *(i)* under reverse bias, LEDs can emit a weak luminescence signal, which is directly proportional to the injected reverse current. Reverse-bias emission is localized in submicrometer-size spots; the intensity of the signal is strongly correlated to the threading dislocation (TD) density, thus suggesting that TDs are preferential paths for leakage current conduction. *(ii)* Under low forward-bias conditions, the intensity of the EL signal is not uniform over the device area. Spectrally resolved EL analysis of green LEDs identifies the presence of localized spots emitting in the yellow spectral region, whose origin is ascribed to localized tunneling occurring between the quantum wells and the barrier layers of the diodes, with subsequent defect-assisted radiative recombination.

- Afterwards, we propose an extensive study of the electroluminescence characteristics of InGaN-based LEDs with color-coded structure, i.e. with a triple quantum well structure in which each quantum well has a different indium content, in order to analyze the carrier distribution inside the quantum wells of the active region. The analysis is based on combined electroluminescence measurements and two-dimensional simulations, carried out at different current and temperature levels. Results indicate that: *(i)* the efficiency of each of

the quantum wells strongly depends on device operating conditions (current and temperature); *(ii)* at low current and temperature levels, only the quantum well closer to the *p*-side has a significant emission; *(iii)* emission from the other quantum wells is favored at high current levels. The role of carrier injection, hole mobility, carrier density and non-radiative recombination in determining the relative intensity of the quantum wells is also discussed.

- At this point, we propose the results obtained from the analysis of physical mechanisms that limit the ESD robustness of GaN-based LEDs. The analysis was carried out on several LED families with different ESD robustness. Each of analyzed sample family is characterized by two different parameters: the failure rate measured after the application of a single ESD pulse, named *First level failure F1*, and the failure rate measured after the application of a second ESD pulse, named *Second level failure F2*. After an initial electro-optical characterization, we have analyzed the LEDs by means of slow capacitance transient, deep level optical spectroscopy (DLOS) and deep level transient spectroscopy (DLTS) measurements. The experimental results show that: *(i)* the overall junction capacitance is strongly correlated to the *First level failure F1*, thus suggesting also a correlation between the maximum junction electric field and the *First level failure F1* of LEDs; *(ii)* the amplitude of capacitance transients, related to trapping phenomena, is strongly correlated to the *Relative failure* parameter, which is defined as the ratio *Second level failure F2/First level failure F1*. Thus, the presence of defects in the LED structures can influence the ESD robustness measured after the application of two consecutive ESD pulses; *(iii)* the correlation between trapping and *Relative failure* is confirmed by both DLOS and DLTS measurements.

- To conclude the study of physical mechanisms that limit the ESD robustness of Light Emitting Diodes (LEDs), we present an ESD characterization carried out on commercially available LEDs. In particular, we present an extensive analysis of the failure mechanisms of RGB (multichip) LEDs submitted to ESD testing: the tests have been carried out on several commercially available LEDs of four different suppliers. In order to better understand the failure mechanisms, we have submitted LEDs to ESD tests under reverse and forward bias condition separately, by means of a Transmission Line Pulser (TLP). The experimental results indicates that: *(i)* red LEDs (based on AlInGaP) have an higher ESD robustness with respect to green and blue samples (based on InGaN), both under reverse and under forward bias test; *(ii)* TLP negative pulses with a current smaller than the failure threshold can induce a decrease of the leakage current in GaN-based LEDs, due to a partial annihilation of defective paths responsible for reverse conduction; *(iii)*

typical failure mechanism of devices is represented by a catastrophic event, with short-circuiting of the junction. However, some of the analyzed red LEDs had shown "soft" failure, with gradual increase of the leakage current and corresponding decrease of the optical power, even without a catastrophic damage. Finally, also the temperature dependence of the ESD robustness of GaN-based devices has been studied.

Useful information on the research activity can be also found in the papers co-authored by the candidate and listed in the next section.

Sommario

La seguente tesi riporta i principali risultati ottenuti dall'attività di ricerca di Dottorato del candidato. L'attività è stata focalizzata sullo studio dei difetti e dei meccanismi fisici the limitano la robustezza alle scariche elettrostatiche (ESD) dei diodi emettitori di luce (LED). In particolare, la maggior parte dell'attività di ricerca è stata principalmente focalizzata sull'analisi dei LED basati su nitruro di gallio (GaN), che sono la base per la realizzazione di emettitori blu e UV e di LED bianchi basati sulla conversione dei fosfori.

Dopo una panoramica iniziale dei concetti teorici più importanti necessari per la comprensione dei risultati fisici, in questa tesi possono essere identificate quattro sezioni principali che riguardano la presentazione dell'attività di ricerca:

- In primo luogo riportiamo un'estesa analisi dei processi di emissione localizzati legati ai difetti, che si verificano nei diodi emettitori di luce basati sulla struttura InGaN/GaN. L'analisi è basata su una caratterizzazione elettrica combinata con misure di elettroluminescenza (EL) risolte spettralmente e spazialmente. I risultati di questa analisi mostrano che: *(i)* in condizioni di polarizzazione inversa i LED possono emettere un debole segnale di luminescenza, che è direttamente proporzionale alla corrente inversa iniettata. L'emissione in polarizzazione inversa è localizzata in spot di dimensione submicrometrica; l'intensità del segnale è fortemente correlata alla densità di *threading dislocation* (TD), suggerendo quindi che le *threading dislocation* sono percorsi preferenziali per la conduzione della corrente di *leakage*. *(ii)* In condizioni di bassa polarizzazione diretta, l'intensità del segnale EL non è uniforme sull'area del dispositivo. L'analisi EL risolta spettralmente dei LED verdi identifica la presenza di spot localizzati che emettono nella regione spettrale gialla, la cui origine è stata attribuita a *tunneling* localizzato che si verifica tra le buche quantiche e gli strati di barriera dei diodi, con successiva ricombinazione radiativa assistita da difetti.

- Successivamente proponiamo uno studio esteso delle caratteristiche di elettroluminescenca dei LED basati su InGaN con struttura *color-coded*, cioè una struttura a tripla buca quantica nella quale ciascuna buca quantica ha un

contenuto di indio differente, allo scopo di analizzare la distribuzione di portatori all'interno delle buche quantiche della regione attiva. L'analisi è basata su misure di elettroluminescenza combinate con simulazioni bidimensionali, eseguite a differenti livelli di corrente e temperatura. I risultati indicano che: *(i)* l'efficienza di ciascuna delle buche quantiche dipende fortemente dalle condizioni operative del dispositivo (corrente e temperatura); *(ii)* a bassi livelli di corrente e temperatura solo la buca quantica più vicina al lato p ha un'emissione significativa; *(iii)* l'emissione dalle altre buche quantiche è favorita ad elevati livelli di corrente. Sarà anche discusso il ruolo dell'iniezione dei portatori, della mobilità delle lacune, della densità di portatori e della ricombinazione non radiativa nel determianre l'intensità relativa delle buche quantiche.

- A questo punto proponiamo i risultati ottenuti dall'analisi dei meccanismi fisici che limitano la robustezza alle scariche elettrostatiche (ESD) dei LED basati su GaN. L'analisi è stata eseguita su numerose famiglie di LED con differenti robustezze ESD. Ciascuna delle famiglie di campioni analizzate è caratterizzata da due differenti parametri: il tasso di *failure* misurato dopo l'applicazione di un singolo impulso ESD, denominato *First level failure F1*, e il tasso di *failure* misurato dopo l'applicazione di un secondo impulso ESD, denominato *Secondo level failure F2*. Dopo un'iniziale caratterizzazione elettro-ottica, abbiamo analizzato i LED per mezzo di misure di transienti capacitivi lenti, *deep level optical spectroscopy* (DLOS) e *deep level transient spectroscopy* (DLTS). I risultati sperimentali mostrano che: *(i)* la capacità di giunzione complessiva è fortemente correlata al *First level failure F1*, suggerendo quindi anche una correlazione tra il massimo campo elettrico di giunzione e il *First level failure F1* dei LED; *(ii)* l'ampiezza dei transienti capacitivi, legata a fenomeni di intrappolamento, è fortemente correlata al parametro *Relative failure*, che è definito come il rapporto *Second level failure F2/First level failure F1*. Quindi la presenza di difetti nelle strutture LED può influenzare la robustezza ESD misurata dopo l'applicazione consecutiva di due impulsi ESD; *(iii)* la correlazione tra il *trapping* e il *Relative failure* è confermata sia dalle misure di DLOS, sia da quelle DLTS.

- Per concludere lo studio dei meccanismi fisici che limitano la robustezza ESD dei diodi emettitori di luce (LED), presentiamo una caratterizzazione ESD eseguita su dei LED disponibili commercialmente. In particolare presentiamo un'estesa analisi dei meccanismi di *failure* dei LED RGB (*multichip*) sottoposti a test ESD: i test sono stati eseguiti su numerosi LED disponibili commercialmente di quattro differenti produttori. Allo scopo di comprendere meglio i meccanismi di *failure*, abbiamo sottoposto i LED a test ESD in

condizioni di polarizzazione inversa e diretta separatamente, per mezzo di un *Transmission Line Pulser* (TLP). I risultati sperimentali indicano che: *(i)* i LED rossi (basati su AlInGaP) hanno una robustezza ESD più alta rispetto ai campioni verdi e blu (basati su InGaN), sia nei test in polarizzazione inversa, sia in quelli in polarizzazione diretta; *(ii)* impulsi TLP negativi con una corrente inferiore alla soglia di *failure* possono indurre una diminuzione della corrente di *leakage* nei LED basati su GaN, a causa di un parziale annientamento dei percorsi difettosi responsabili per la conduzione inversa; *(iii)* il tipico meccanismo di *failure* dei dispositivi è rappresentato da un evento catastrofico, con cortocircuitazione della giunzione. Tuttavia, alcuni dei LED rossi analizzati hanno mostrato *"soft" failure*, con graduale aumento della corrente di *leakage* ed una corrispondente diminuzione della potenza ottica, anche in assenza di un danno castastrofico. Infine, è stata studiata anche la dipendenza dalla temperatura della robustezza ESD dei dispositivi basati su GaN.

Utili informazioni sull'attività di ricerca possono essere trovate negli articoli in cui ha collaborato il candidato ed elencati nella successiva sezione.

List of Publications

International journal papers

- N. Trivellin, M. Meneghini, C. De Santi, S. Vaccari, G. Meneghesso, E. Zanoni, K. Orita, S. Takigawa, T. Tanaka, and D. Ueda, "Degradation of InGaN lasers: Role of non-radiative recombination and injection efficiency", *Microelectronics Reliability*, Vol. 51, Issues 9-11 pp. 1747-1751, September-November 2011.

- M. Meneghini, S. Vaccari, N. Trivellin, D. Zhu, C. Humphreys, R. Butendheich, C. Leirer, B. Hahn, G. Meneghesso, and E. Zanoni, "Analysis of defect-related localized emission processes in InGaN/GaN-based LEDs", *IEEE Transactions on Electron Devices*, Vol. 59, no. 5, pp. 1416-1422, May 2012.

- M. Meneghini, S. Vaccari, A. Garbujo, N. Trivellin, D. Zhu, C. J. Humphreys, M. Calciati, M. Goano, F. Bertazzi, G. Ghione, E. Bellotti, G. Meneghesso, and E. Zanoni, "Electroluminescence analysis and simulation of the effects of injection and temperature on carrier distribution in InGaN-based LEDs with color-coded quantum wells", *Japanese Journal of Applied Physics 52* (2013) 08JG09.

- S. Vaccari, M. Meneghini, A. Griffoni, D. Barbisan, M. Barbato, S. Carraro, M. La Grassa, G. Meneghesso, and E. Zanoni, "ESD characterization of multi-chip RGB LEDs", *Microelectronics Reliability*, Vol. 53, Issues 9-11 pp. 1510-1513, September-November 2013.

- C. De Santi, M. Meneghini, S. Carraro, S. Vaccari, N. Trivellin, S. Marconi, M. Marioli, G. Meneghesso, and E. Zanoni, "Variation in junction capacitance and doping activation associated with electrical stress of InGaN/GaN laser diodes", *Microelectronics Reliability*, Vol. 53, Issues 9-11 pp. 1534-1537, September-November 2013.

Papers on international conference proceedings

- S. Vaccari, M. Meneghini, D. Zhu, C. J. Humphreys, G. Meneghesso, and E. Zanoni, "Extensive electroluminescence analysis of InGaN-based Light-Emitting Diodes: temperature and current-dependent effects", *in Proceedings of 20th European Workshop on Heterostructure Technology, HETECH 2011*, $7 - 9^{th}$ November 2011, Lille, France.

- S. Vaccari, M. Meneghini, N. Trivellin, D. Zhu, C. Humphreys, R. Butendheich, C. Leirer, B. Hahn, G. Meneghesso, and E. Zanoni, "Extensive study of luminescence processes related to localized defects in InGaN-based Light Emitting Diodes", *in Proceedings of 36th Workshop on Compound Semiconductor Devices and Integrated Circuits, WOCSDICE 2012*, May $28 - 30^{th}$ 2012, Island of Porquerolles, France.

- S. Vaccari, M. Meneghini, D. Zhu, C. J. Humphreys, G. Meneghesso, and E. Zanoni, "Current and temperature dependence of electroluminescence in InGaN-based LEDs with multi-wavelength emission", *in Proceedings of 9th International Symposium on Semiconductor Light Emitting Devices 2012, ISSLED 2012*, July $22^{nd} - 27^{th}$ 2012, Berlin, Germany.

- N. Trivellin, M. Meneghini, S. Vaccari, B. Hahn, C. Leirer, G. Meneghesso, and E. Zanoni, "Electrical, spectral and thermal analysis of yellow luminescent dots in InGaN green LEDs", *in Proceedings of International Workshop on Nitride Semiconductors 2012, IWN 2012*, October $14 - 19^{th}$ 2012, Sapporo, Japan.

Papers accepted for publication on international journal

- M. Meneghini, S. Vaccari, M. Dal Lago, S. Marconi, A. Griffoni, A. Alfier, G. Verzellesi, G. Meneghesso, and E. Zanoni, "ESD degradation and robustness of RGB LEDs and modules: an investigation based on combined electrical and optical measurements", *accepted for publication on Microelectronics Reliability journal.*

Introduction

High-power light-emitting diodes (LEDs) are considered as excellent candidates for the realization of the next-generation light sources and for this reason, over the last decade many efforts have been done by several research groups and companies, in order to improve the performances of light-emitting diodes. In particular, great interest have been focused on gallium nitride-based LEDs, due to their several applications. In fact, blue LEDs are employed for the realization of white LED sources based on phosphor conversion. As a result, LEDs with luminous efficacy in excess of 100 lm/W have been recently demonstrated [1], thus clearing the way for a massive market penetration of solid-state light sources. On the other hand, green LEDs are expected to find large application in the display, automotive and projection fields [2] [3].

However, unlike other conventional III-V LEDs, gallium nitride based LEDs contain a large number of defects, such as threading dislocations (TDs) [4]. In order, to contribute to the improvement in LED technology, it is necessary to deeply understand the role of defects in limiting the electrical and optical performance of devices. Recently, preliminary reports have suggested that localized defects can be responsible for leakage current conduction and localized emission under reverse bias, and for spectral inhomogenities under forward-bias conditions [5] [6] [7] [8] [9]. However, despite the interesting results provided by these studies, no extensive analysis of the role of defects in influencing the emission properties of LEDs both under reverse and under forward bias condition can be found in literature up to now.

It has been demonstrated that defects can also limit the efficiency of LEDs in the low-current operating regime [10] and possibly also at high current densities [11] [12]. However, many other factors can limit the optical efficiency of LEDs, including: *(i)* carrier escape from quantum wells occurring at high current and temperature levels; *(ii)* efficiency droop, which is usually ascribed to Auger recombination [13] or carrier leakage effects [14]; and *(iv)* the fact that in a multiple quantum well structure, carriers are not uniformly distributed among the quantum wells and thus some of them does not contribute to the emission [15].

Despite the several applications of GaN-based LEDs, these devices particularly

suffer also by reliability issues, that limit their lifetime. In the last decade, several research groups have focused on the analysis of degradation mechanisms occurring in GaN-based LEDs, in order to better understand the failure mechanisms of these devices [16] [17] [18] [19]. In particular, the studies quoted above have shown that several factors lead to a gradual degradation of electrical and optical properties of nitride-based LEDs, including: *(i)* the increase in non-radiative recombination rate, due to constant current stress; *(ii)* the degradation of ohmic contacts occurring at high-temperature stress; and *(iii)* the degradation of optical properties of packages and phosphors in white LEDs for high temperature operation.

Another very critical reliability issue of LEDs is represented by Electrostatic Discharge (ESD) events: differently from the degradation mechanisms mentioned above, ESD can induce the catastrophic failure of devices. In the recent years, different solutions have been proposed in order to improve the ESD robustness of LEDs, including: employment of internal inverse-parallel protection diodes [20] [21] [22] [23] or CMOS protection circuits [24], realization of flip-chip structures with Metal-Oxide-Silicon submount [25] or insertion of a floating ring near the n-electrode [24], introduction of a n^--GaN layer [26] and finally the introduction of an Al film with an air gap on the bottom side of the sapphire substrate [27].

In this work we present an extensive analysis of defects and physical mechanisms that limit the ESD robustness of LEDs. In particular, most of work will be focused on gallium nitride-based light emitting diodes. Two main sections can be identified in this thesis concerning the analysis of experimental results: in the first part, we will analyze the influence of defects in the electrical and optical properties of GaN-based LEDs. Also the mechanisms that limit the carrier distribution inside the quantum wells of a multiple quantum well structure, thus limiting also the optical efficiency, will be studied. The aim of this work is to contribute to the understanding of the luminescence processes related to localized defects in GaN-based LEDs and also to the understanding of carrier injection and recombination processes occurring in a MQW structure, by presenting an analysis of the electroluminescence characteristics of color-coded LEDs measured at different current and temperature levels. On the other hand, in the second part of this work we will analyze the physical mechanisms that limit the ESD robustness of GaN-based LEDs: the purpose of this work is to understand the physical mechanisms responsible for the failure of devices, when submitted to ESD effects, and in particular the role of defects in determining the ESD robustness of LEDs. Thus, it is clear that the preliminary analysis of defects carried out in the first part of the work is fundamental, in order to obtain a better understanding of these failure mechanisms. Also an ESD characterization of RGB devices will be proposed, with the aim of obtaining a comparison between different LED technologies in terms of ESD robustness, in this particular case between AlGaInP-based red LEDs and GaN-based green and

blue LEDs.

After an initial overview on the theoretical concepts necessary to the understanding of experimental results, the main data obtained from the research activity will be presented. In particular, this thesis has been organized in different sections, as follow:

- *Chapter 1: Gallium Nitride.* In this section it will be presented a brief overview of the physical properties of gallium nitride, as it represents the basic material for the realization of white, blue and green LEDs. Also details on the doping and ohmic contacts realized on GaN will be provided.

- *Chapter 2: LED basics.* In this chapter an overview on the main electrical and optical properties of LEDs will be presented. Also the main LED structures will be briefly analyzed.

- *Chapter 3: Electrostatic Discharges on LEDs.* In this section will be provided an overview on electrostatic discharge events: in particular, the ESD generation mechanisms and ESD stress models will be discussed. Also the Transmission Line Pulse technique will be analyzed in detail, due to its importance in our work. Finally, the main works of ESD effects on LEDs that can be found in literature will be briefly recalled.

- *Chapter 4: Analysis of defect-related localized emission processes in GaN-based LEDs.* At this point, the results of defect analysis carried out on GaN-based LEDs will be presented. In particular, this section will be mainly focused on the emission processes related to defects and on their influence on the electrical and optical properties of LEDs.

- *Chapter 5: Analysis of injection processes and carrier distribution in MQW GaN-based LEDs with color-coded structure.* In this section, an extensive analysis of the electroluminescence characteristics of InGaN-based LEDs with color-coded structure will be presented. In particular, the study is based on combined EL measurements and simulations. Also the role of carrier injection and carrier distribution inside the quantum wells in determining the optical efficiency of devices will be discussed.

- *Chapter 6: Analysis of physical mechanisms that limit the ESD robustness of GaN-based LEDs.* At this point the results of analysis of physical mechanisms responsible for the ESD failure of GaN-based LEDs will be presented. In particular, the role of defects in determining the ESD robustness of devices will be deeply analyzed. This study have been carried out by means of slow capacitance transient, DLTS and DLOS measurements, as it will be shown.

- *Chapter 7: ESD characterization of RGB LEDs.* Finally, the results of an extensive ESD characterization carried out on several commercially available RGB devices will be presented. The ESD tests were carried out by means of the Transmission Line Pulse technique. Also optical characterization during stress tests have been carried out on some of the analyzed devices. To conclude, we will show also the results obtained from the analysis carried out on some commercially available LEDs, submitted to ESD stress test at different temperature levels.

Chapter 1

Gallium Nitride

The III-V nitrides represent excellent materials for the development of optoelectronic devices. In particular gallium nitride (GaN), aluminum nitride (AlN), indium nitride (InN) and boron nitride (BN) are the basic materials for this semiconductor class [28]; however boron nitride is still relatively immature as a semiconductor material [29]. The III-N material system covers a very broad range of wavelengths, from the infrared to the deep ultraviolet. In fact the combination of three basic materials cited above form a continuous alloy system (InGaN, InAlN and AlGaN) whose bandgaps range from 0.8 eV for InN and 3.4 eV for GaN to 6.2 eV for AlN at room temperature, as shown in Figure 1.1.

Gallium nitride is the fundamental material for this compound semiconductor class: its wide and direct energy bandgap makes it suitable in optoelectronic applications for the realization of blue and UV light emitting diodes. Gallium nitride is also characterized by good thermal stability and high thermal conductivity, compared to silicon and gallium arsenide, that allow a better heat dissipation in devices and thus the employment of this material in high-temperature and high power electronics. Moreover, due to the ability to form alloys, it is possible to produce LEDs and laser diodes with specific wavelength. Alloys are also fundamental to create heterojunctions with potential barriers inside the device structure.
All these features have made possible the realization of high power GaN-based LEDs that can be found in many applications: solid-state lighting, street lighting, traffic lights, projection fields, automotive. In fact, blue LEDs are employed for the realization of white LED sources based on phosphor conversion; on the other hand green LEDs are expected to find large application in the display and projection fields [2]. Also UV laser diodes have been demonstrated in the recent years, which are actually employed mainly in high-density optical systems and UV lithography. For this reason, before to recall the main electrical and optical characteristics of Light Emitting Diodes, it is necessary to review the main properties of gallium nitride and also the open issues related to this material, in order to better understand

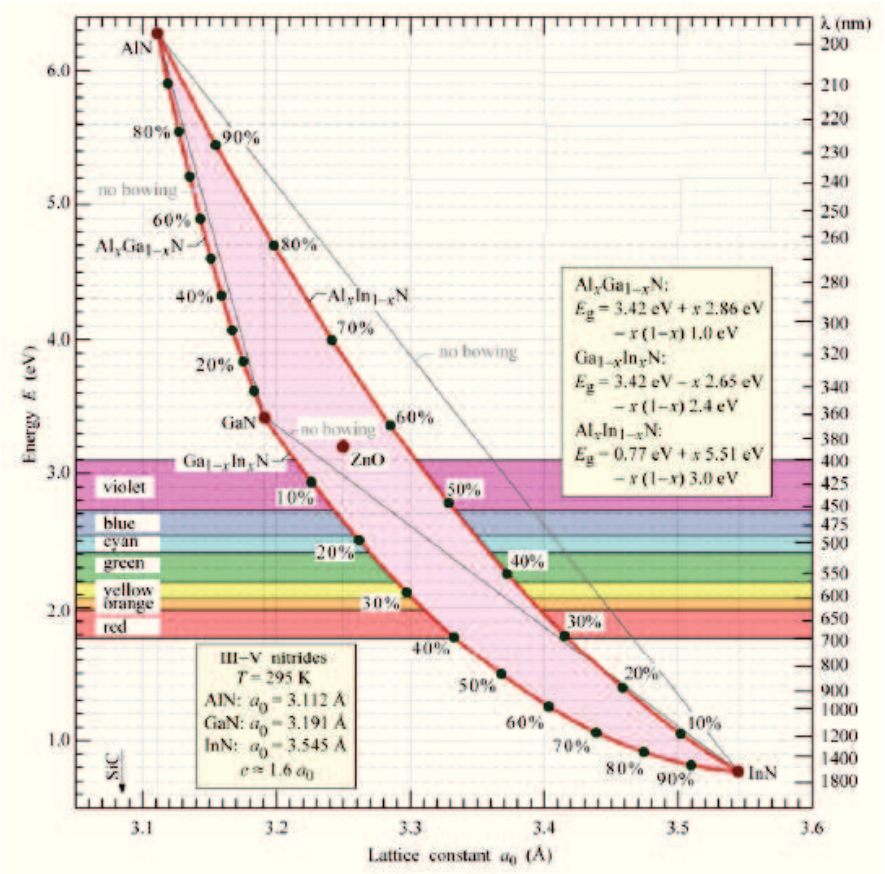

Figure 1.1: Bandgap energy vs lattice constant at room temperature for III-V nitride semicondutors.

the experimental results that will be presented in the following chapters.

In this chapter we will briefly review the main properties of gallium nitride, such as crystalline form, band structure and substrates for growth; after this, we will discuss the main problems related to the doping and the realization of ohmic contacts in GaN, and finally we will briefly discuss the typical defects that can be found in GaN, with particular focus to dislocations.

1.1 Crystalline forms and band structure

Gallium nitride is a direct bandgap semiconductor: this fundamental characteristic make it an attractive semiconductor for many optoelectronic applications (LEDs and laser diodes). Gallium Nitride and its alloys can crystallize in two different structures: **wurtzite** and **zincblende**, which schematic unit cells are shown in Figure 1.2. The III-V nitride semiconductors can be found also in the *rock salt* crystal structure, but it is of no importance to electronic devices so far [28].

The crystalline structure of gallium nitride can be provided by three lattice constants (a,b,c) and three angles (α,β,γ): this parameters are used to describe

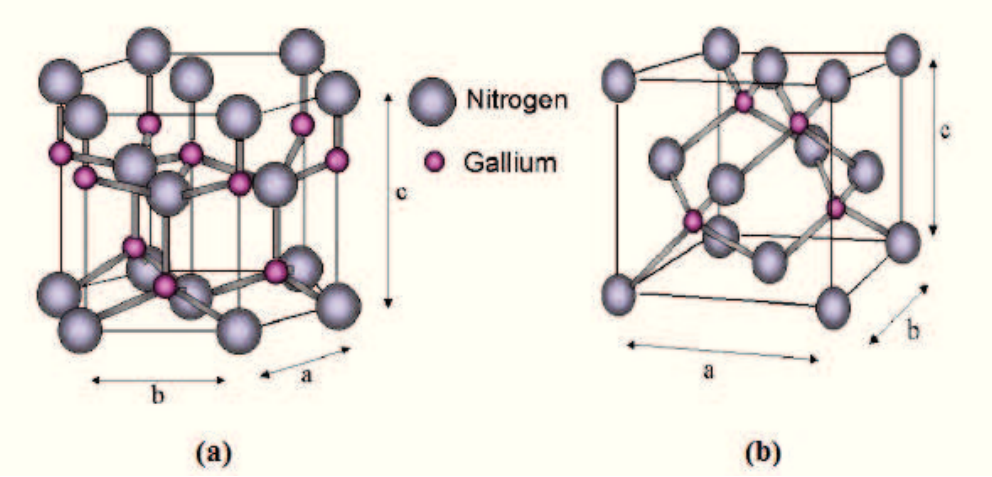

Figure 1.2: Schematic representation of (a) wurtzite and (b) zincblende unit cells for gallium nitride.

the distance and the reciprocal position of atoms in the unit cell of the crystal.

Wurtzite lattice has an hexagonal structure, with ($a = b \neq c$) and ($\alpha = \beta = 90°$, $\gamma = 120°$). The c-axis is orthogonal to the hexagonal plane. In particular, the lattice is a sequence of gallium and nitrogen atom surfaces which are placed along the c-axis, thus forming two hexagonal lattice structures compenetrated. The band structure of gallium nitride for the wurtzite case is shown in the E vs k diagram on the top of Figure 1.3: this band structure is similar to those of some direct-bandgap zincblende semiconductors, such as the GaAs for example, except for the fact that the degeneracy of the valence band is more pronounced in GaN with respect to GaAs, due to the strong electric field present in the crystal structure of GaN. However, the role of strain is less effective in GaN in deforming the valence band with respect to GaAs.

On the other hand, in zincblende lattice the nitrogen atoms are placed in a cubic structure and bonded to a tetrahedric structure composed by gallium atoms, thus forming two cubic lattice structures compenetrated. In particular zincblende structure has three identical lattice constants ($a = b = c$) and identical angles ($\alpha = \beta = \gamma = 90°$). The schematic band diagram of gallium nitride for the zincblende case is shown on the bottom of Figure 1.3.

Even though the two crystalline structures described above have some analogies from the crystallographic point of view, they are strongly different from the electrical and doping point of view. It is important to point out that electrical properties of a semiconductor are strongly dependent from the lattice constants of the crystal: for example, a smaller lattice structure implies a greater bandgap energy. There is also a relationship between temperature and bandgap, i.e. a higher temperature induce a widening of the crystal structure and thus a lower energy bandgap of the semiconductor.

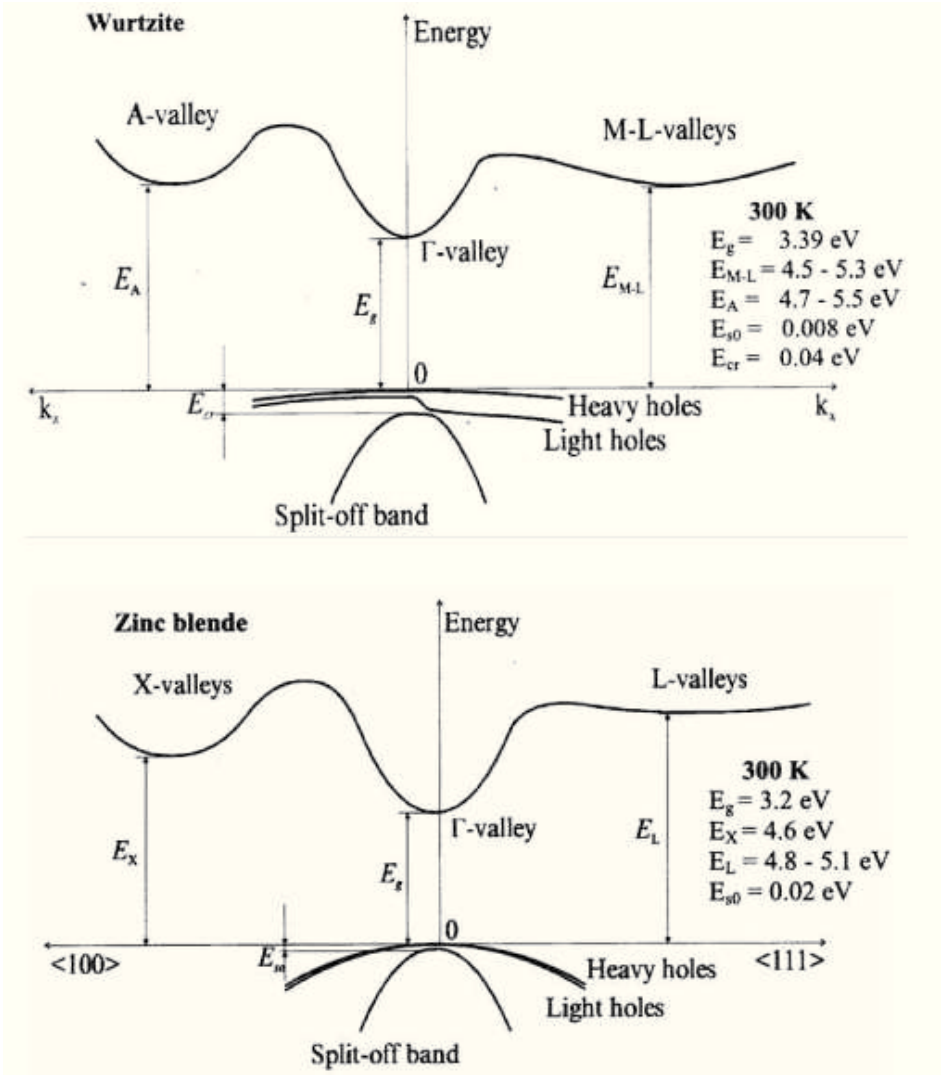

Figure 1.3: Gallium nitride band diagrams, both for the wurtzite and for the zincblende structures.

The gallium nitride is usually found in the wurtzite structure, differently from other widely used semiconductor materials, such as silicon and germanium, which have a diamond lattice, and other III-V semiconductors (for example GaAs e GaP), which have a zincblende structure.

The most important properties of gallium nitride, both for the wurtzite and for the zincblende structure, are reported in Table 1.1, where they are compared with other common semiconductors. As it can be noticed, the large bandgap of GaN implies a high electric breakdown field. The large bandgap energy of GaN allows also high temperature operation and provides improved radiation hardness. Another very important advantage of GaN is represented by the high thermal conductivity yet cited above, that allows the realization of high power devices.

Properties (300 K)	Symbol	Ge	Si	GaAs	GaP	GaN
Crystal structure	D = Diamond Z = Zincblende W = Wurtzite	D	D	Z	Z	W Z
Bandgap	D = Direct I = Indirect	I	I	D	I	D
Lattice constant	$a_0 = b_0$ [Å] c_0 [Å]	5.64	5.43	5.65	5.45	3.19 4.52 5.19 4.52
Bandgap energy	$E_g\,[eV]$	0.66	1.12	1.42	2.26	3.44 3.3
Intrinsic carriers concentration	$n_i\,[cm^{-3}]$	2×10^{13}	1×10^{10}	2×10^{16}	1.6×10^{10}	1.9×10^{10}
Electron mobility	$\mu_n\,[\frac{cm^2}{V \cdot s}]$	3900	1500	8500	110	1500
Hole mobility	$\mu_p\,[\frac{cm^2}{V \cdot s}]$	1900	450	400	75	30
Electron diffusion constant	$D_n\,[\frac{cm^2}{s}]$	101	39	220	2.9	39
Hole diffusion constant	$D_p\,[\frac{cm^2}{s}]$	49	12	10	2	0.75
Electron affinity	$\chi\,[V]$	4.0	4.05	4.07	-	4.1
Refractive index	n_{opt}	4.0	3.3	3.4	-	2.67 2.5
Breakdown field	$E_{break}\,[\times 10^5 \frac{V}{cm}]$	0.8	3	3.5	-	33
Dielectric constant	ε_r	-	11.9	12.5	-	9.5 -
Thermal conductivity	$k\,[\frac{W}{cm \cdot K}]$	0.606	1.412	0.455	0.97	1.5

Table 1.1: Comparison between the main physical properties of gallium nitride and some common semiconductor materials.

1.2 Polarization effects in III-N semiconductor materials

The most common epitaxial growth direction of III-V nitrides in the hexagonal wurtzite structure is the *c*-plane (i.e. normal to the [0001] basal plane), where the atoms are arranged in bilayers consisting of two closely spaced hexagonal layers, one with gallium atoms and the other with nitrogen atoms. In particular, gallium nitride grown on the *c*-plane have polarization charges located at each of the two surfaces of a layer, which can induce internal electric fields.

Spontaneous polarization fields, as well as strain-induced ***piezoelectric polarization fields*** can be found in gallium nitride: in the following of this section we will discuss separately these two polarization fields and their effects on the electrical and optical properties of semiconductors.

1.2.1 Spontaneous polarization

The covalent bond of gallium nitride is characterized by a stronger ionicity compared to other III-V covalent bonds: this is due to the lack of electrons occupying the outer orbitals of the nitrogen atom. In fact, the electrons of gallium atom involved in the metal-nitrogen covalent bond are strongly attracted by the Coulomb potential of the nitrogen atomic nucleus. The ionicity of this covalent bond, which correspond to a microscopic polarization, will result in a macroscopic polarization if the crystal has a lack of inversion symmetry, as in the case of gallium nitride both in the wurtzite and in the zincblende structure. This polarization effect is also called *spontaneous polarization*.

Gallium nitride layers can be grown either Ga-faced or N-faced, as shown in Figure 1.4. In the case of Ga-faced structure, the spontaneous polarization points toward the substrate, while for N-faced GaN, the polarization points toward the surface of the layer sequence. It is important to point out that both bulk and surface properties of GaN can depend significantly on whether the crystal is Ga-faced or N-faced.

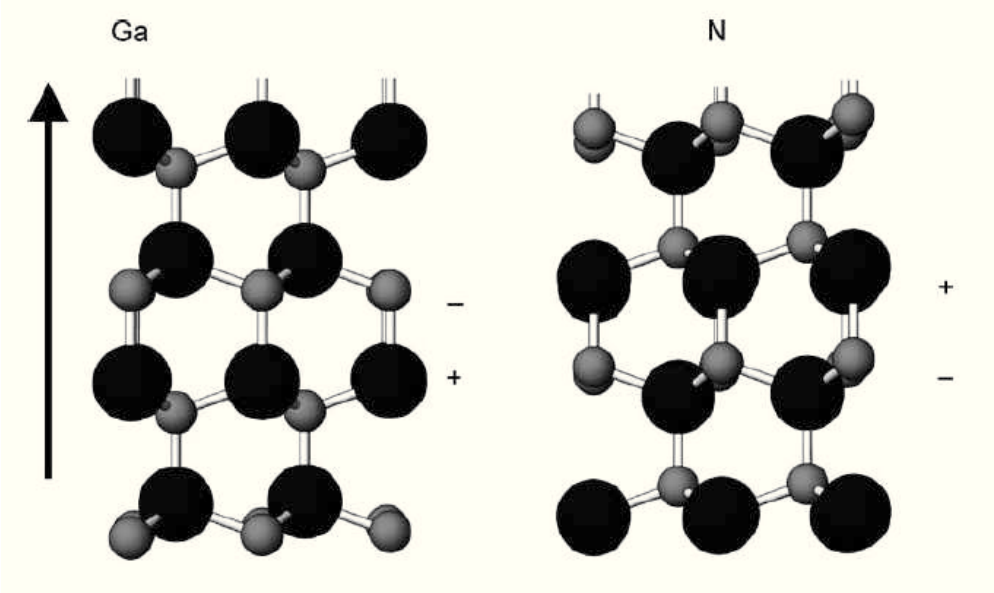

Figure 1.4: Crystal structure of wurtzite GaN for (left) Ga-face and (right) N-face growth.

Referring to the data reported in [30], a spontaneous polarization P_{SP} as high as $-0.029\ C \cdot cm^{-2}$ can be found in GaN, while in AlN and InN the spontaneous polarization is equal to -0.081 and $-0.032\ C \cdot cm^{-2}$ respectively. Note that for all materials the effective spontaneous polarization in negative and its magnitude increases from GaN to InN and to AlN.

1.2.2 Piezoelectric polarization

The *piezoelectric polarization* is based on strain to the III-nitride crystal and a displacement of the anion-sublattice to the cation-sublattice [28]. The strain in the epitaxial layer can be compressive or tensile. in the compressive-strain case, the epitaxial layer is laterally (i.e. in the plane of the wafer) compressed, while in the tensile-strain case the epitaxial layer is expanded along the lateral direction. The direction of piezoelectric polarization will depend on whether the crystal is Ga-faced or N-faced and if it is compressive-strained or tensile-strained. A summary of direction for spontaneous and piezoelectric polarization in different cases is reported in Figure 1.5.

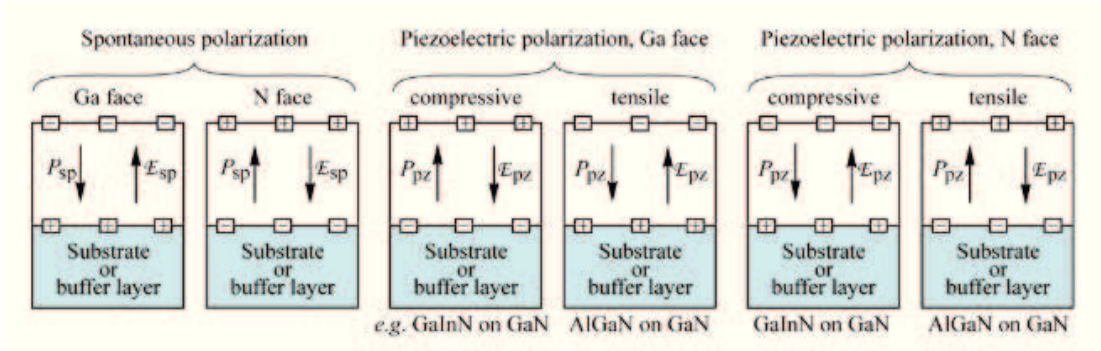

Figure 1.5: Direction of polarization field and electric field for spontaneous and piezoelectric polarization in Ga-faced and N-faced III-V nitrides.

Thus, in GaN-based material systems both a spontaneous polarization component and a piezoelectric polarization component will be present. The piezoelectric polarization P_{PZ} induced by strain along the c-axis in a strained layer of wurtzite-type III nitrides is equal to [31]:

$$P_{PZ} = 2 \cdot \frac{a - a_0}{a_0} \left(e_{31} - e_{33} \cdot \frac{C_{13}}{C_{33}} \right) \tag{1.1}$$

where e_{13} and e_{33} are the piezoelectric constants, C_{13} and C_{33} denote the elastic constants and finally a and a_0 are the lengths along the hexagonal edge, which are similarly modified.

If there is no external electric field applied to the semiconductor material, the total macroscopic polarization P can be expressed as the sum of spontaneous polarization P_{SP}, i.e. the polarization at zero strain, and the piezoelectric polarization P_{PZ}:

$$P = P_{SP} + P_{PZ} \tag{1.2}$$

For example, with reference to data reported in [32], the total polarization field inside a Ga-faced $Al_xGa_{1-x}N/GaN/Al_xGa_{1-x}N$ quantum well is equal to:

$$P = P_{SP} + P_{PZ} = (-0.029 + 0.0163x)\, C \cdot m^{-2} \tag{1.3}$$

which corresponds an electric field that can be expressed as:

$$E = \frac{P}{\epsilon_{GaN}\epsilon_0} = (3.6 \cdot 10^6 - 2.1 \cdot 10^6 x)\, V \cdot cm^{-1} \tag{1.4}$$

where ϵ_{GaN} and ϵ_0 represent the dielectric constants of gallium nitride and vacuum, respectively. The internal electric field of an $AlGaN/GaN$ heterostructure can be higher than 1 MV/cm. In [33] it has been estimated that an $In_{0.15}Ga_{0.85}N/GaN$ quantum well can have even an internal field as high as 2.1 MV/cm. In the next section will be shown as these important internal fields can influence the electrical and optical properties of III-V nitride materials.

1.2.3 Quantum-confined Stark effect

As a consequence of the strong electric field present inside a GaN-based heterostructure or quantum well, the bands in this region are strongly tilted and thus electrons and holes are separated on the opposite corners of the well, as shown in Figure 1.6. This phenomenon leads to the redshift of the transition energy between conduction and valence band. The redshift of electroluminescence with respect to the ideal potential well is also known as the ***Quantum-Confined Stark Effect***.

The Quantum-Confined Stark Effect results also in a reduction of the radiative recombination efficiency, since electrons and holes are not spatially overlapped inside the quantum well, thus reducing the recombination probability. This effect is particularly prominent for wide quantum wells, with a thickness greater than about 100 Å. In order to minimize this effect, it is necessary to keep very thin the quantum well layers: for this reason quantum well thickness of maximum 20-30 Å are tipically used [34]. Note in Figure 1.6 the effect of different layers thickness in the spatial overlapping of the wave function of electrons and holes respectively.

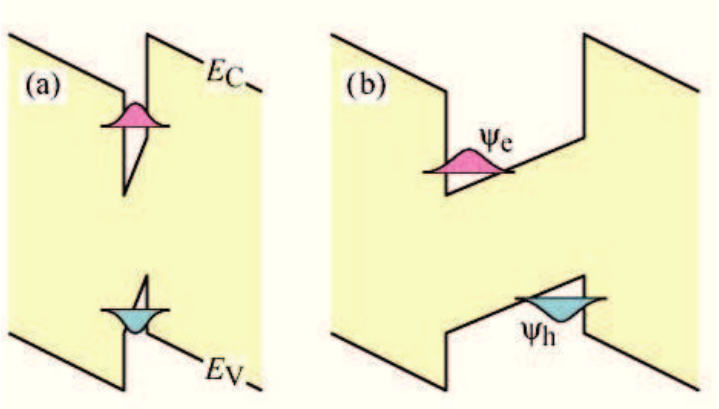

Figure 1.6: Schematic band diagram of (a) thin and (b) thick AlGaN/GaN heterostructure with internal polarization fields. Note that in this figure the substrate in on the right-hand side and the growth of III-nitrides is Ga-faced.

The polarization effects can be screened by a high free-carrier concentration inside the quantum well, which can be obtained either by high doping of the active region or by a high injection current. This screening effect results in a blue-shift of the emission as the injected current is increased, frequently found in InGaN-based LEDs. Alternatively, the screening of the internal field can be also obtained by applying a bias to the heterostructure: for example, Bunker *et al.* in [35] have shown that the compensation of the internal field of a single quantum well InGaN/GaN LED, resulting in a blueshift of the EL peak, can be obtained by applying a reverse bias to the LED. In particular, by increasing the reserve bias, it can be observed a cancellation of the piezoelectric field until flat-band conditions are reached; at this point a further increase in the reverse bias inverts the bands, inducing a redshift of the emission, as shown in Figure 1.7. This fact thus suggests that the direction of internal field is opposite to the applied reverse bias field.

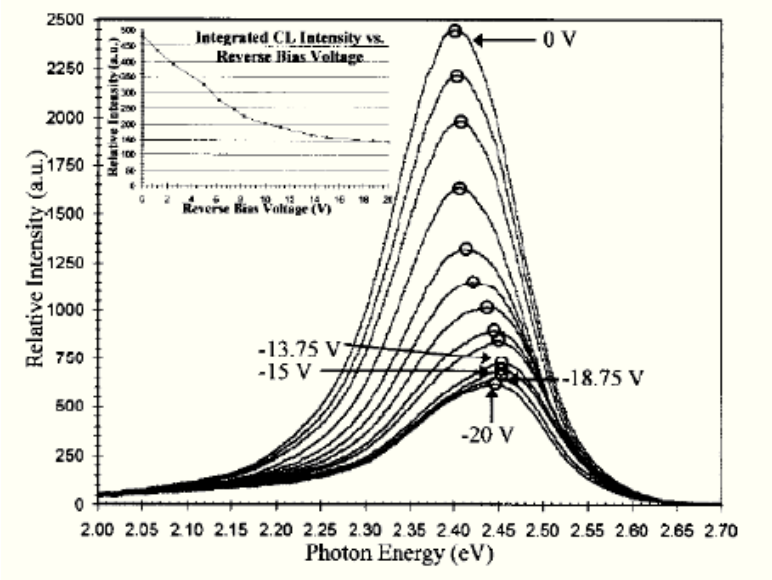

Figure 1.7: SEM-CL spectra of the InGaN MQW LED obtained at room temperature and at different reverse biases. The CL emission shows a peak blueshift of 52 meV until -15 V. For reverse biases higher than -15 V it begins to redshift. The circles indicate the peak position of the CL spectra [35].

Polarization effects in III-nitride semiconductors can also be used to reduce ohmic contact resistances in GaN-based devices. An example is represented by polarization-enhanced contacts to *p*-type GaN, where it is employed a thin, compressively strained InGaN cap layer deposited on the *p*-type GaN: the electric field in the cap layer is polarized in such a way that the tunneling probability of holes in increased [34].

1.3 Substrates for GaN growth

One of the major problems related to the gallium nitride is represented by the lack of a suitable substrate for its growth, which makes necessary the usage of *heteroepitaxy* technique. In reality, also *homoepitaxy* is today possible: however, neither conducting nor semi-insulating GaN substrates are so far available in sufficient diameter quality [36] [37]. Thus, in most cases gallium nitride is still produced by growth on a foreign substrate.
Usually the mismatch parameter between GaN and the foreign material is used as main criterion for the choice of the substrate. However, not only the lattice parameter is important for the choice of substrate material, but also other parameters need to be regarded, including the structure of crystal material, the treatment of a surface, the composition, the reactivity of the surface, as well as the chemical, thermodynamic and electrical properties of material. It is important to point out that the substrate determines also crystal orientation, polarity, polytype, surface morphology, elastic strains and concentration of gallium nitride defects.

The first attempts to grow gallium nitride were made by Johnson in 1930s [38], who synthesized GaN samples by the reaction of ammonia gas with metallic Ga at high temperatures, $900-1000\ ^{\circ}C$. Several efforts have been done in the subsequent decades, in order to grow good quality GaN crystals, but without significant results: the difficulties were mainly related to the hydrogen passivation and nitrogen vacancies, or other unknown defects, which made it difficult to obtain sufficient p doping. The first good quality GaN films were grown by Amano and Hiramatsu in the late 1980s and early 1990s [39] [40], who demonstrated that growth on sapphire substrates is facilitated by the insertion of an AlN buffer layer deposited at low temperature. In most cases gallium nitride is grown on sapphire and silicon carbide substrates, but in the recent years, many efforts have been done in order to obtain low dislocation density GaN films grown on gallium nitride substrate. Many research groups are also focusing on the growth of GaN films on silicon substrates. In this section we will briefly describe the main characteristics of the most important substrate materials usually employed for the GaN growth, highlighting the benefits and drawbacks deriving from each of them.

1.3.1 Sapphire (Al_2O_3)

The first good quality GaN films have been grown on sapphire substrate and today this material is still competitive for the realization of optoelectronic devices. The sapphire is widely used for several reasons, including its large availability, its hexagonal symmetry, which makes it compatible with wurtzite-GaN, its stability at the high temperature and pressure levels necessary for MOVPE and its low cost.

However, sapphire is characterized also by some drawbacks that limit the quality of devices. First, the lattice mismatch between sapphire and GaN, also shown in Figure 1.8, is close to 13 %, thus leading to a high density of dislocations in the grown materials ($10^{10}\,cm^{-2}$). In particular, such a great value of the defect density reduces the charge carriers mobility, the non-radiative lifetime and the thermal conductivity, all of which induce a degradation of device performances.

Second, the higher thermal expansion coefficient of sapphire with respect to that

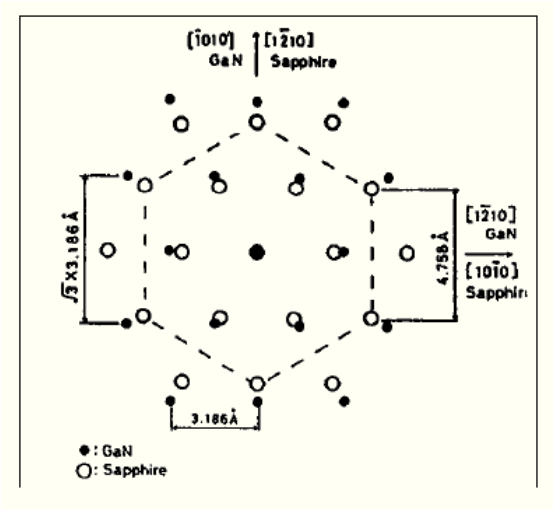

Figure 1.8: Schematic illustration of in-plane atomic arrangement in the case of (0001) GaN film grown on (0001) sapphire.

one of GaN induces biaxial compressive strain in the epitaxial layer during the cooling phase: this fact can lead to cracking in the grown crystal.

Third, the sapphire substrate is electrically insulating. Thus, all electrical contacts must be made in the front size of the device. A schematic illustration of a typical LED structure grown on sapphire substrate in shown in Figure 1.9(a). This fact results in a reduction of the area available for devices and in a higher complexity in the device fabrication. Moreover, in such a type of device the current flow is lateral, thus increasing the *current crowding* phenomenon, which is related to the high resistivity of GaN layers. The current crowding in particular induces also a decrease in the optical efficiency and a more prominent degradation of device due to the high current flowing near the n-type contact, as shown in Figure 1.10.

In order to improve the quality of GaN films on sapphire, it can be introduced an AlN buffer layer between the substrate and the GaN layer: this layer is first grown at low temperatures (usually about $500 - 550\ ^{\circ}C$ for MOCVD, $400\ ^{\circ}C$ for MBE [41]), which becomes amorphous. During the subsequent deposition of GaN, the high temperatures (usually about $1100\ ^{\circ}C$ for MOCVD, $700\ ^{\circ}C$ for MBE [41]), turn the AlN buffer in a crystalline form, thus forming a good base for the growth of high quality GaN films.

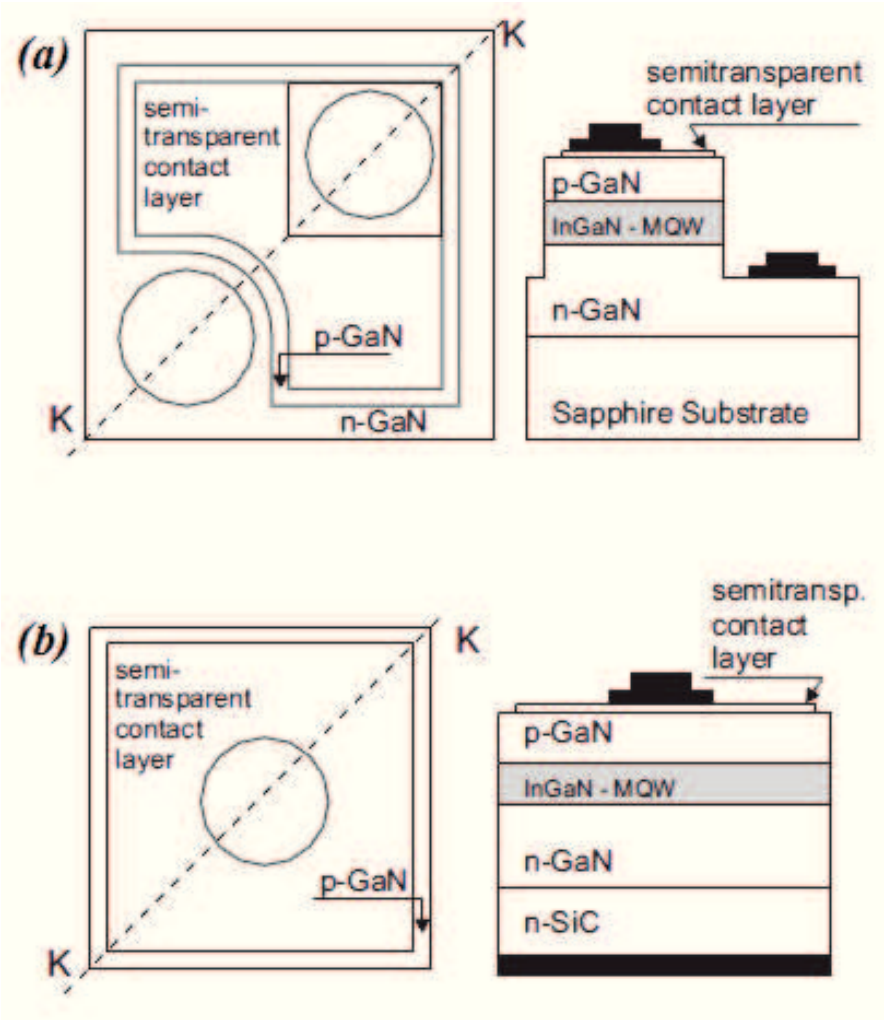

Figure 1.9: Schematic top view and cross section, along the k-k line, of a typical LED grown (a) on sapphire substrate and (b) on silicon carbide substrate.

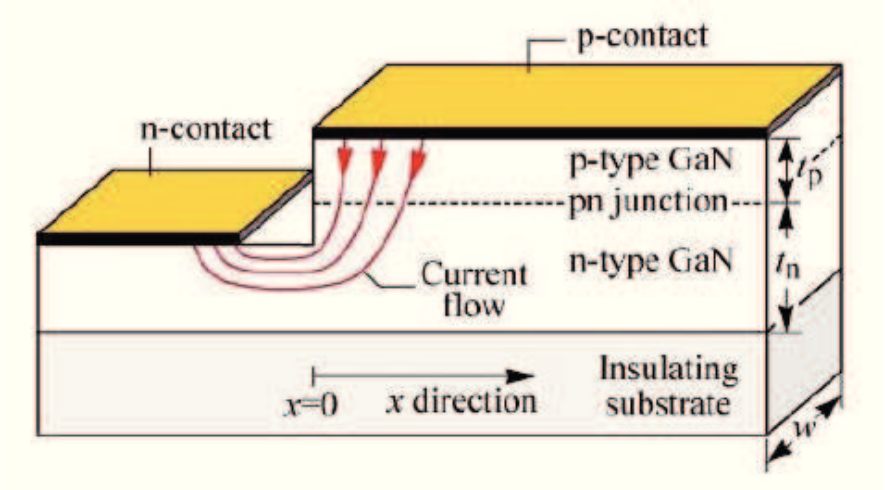

Figure 1.10: *Current crowding* phenomenon occurring on devices with lateral current flow.

1.3.2 Silicon Carbide (SiC)

Silicon Carbide has a number of advantages with respect to sapphire substrate for GaN growing. First, the lattice mismatch between SiC and GaN is only 3.4 % and with an AlN buffer layer it is further reduced [42]. Second, the silicon carbide substrate has an higher thermal conductivity with respect to sapphire. Third, it is possible to prepare electrically conductive SiC layers, thus enabling the realization of vertical structure devices, as shown in figure 1.9(b). In such a structure the electrical contacts can be mounted on the reverse side of structure: this fact reduces the complexity in the fabrication of devices, increase the emission area with respect to the sapphire case and reduces the current crowding effect, as the current flow is vertical and more uniform in this case.

There are both C-polar silicon carbide substrates, the so-called C-substrates, and Si-polar silicon carbide substrates, namely Si-substrates. In the first case, C atoms go into the substrate surface, whereas in the second case just Si atoms pass there. Nowadays, are preferable Si-substrates because the quality of GaN films is higher when they are grown on this substrate.

One of the major drawbacks of silicon carbide substrate is its high cost. Moreover, gallium nitride epitaxially grown on SiC shows some problems related to the poor wetting between these materials. These problems can be solved by using a low temperature AlN buffer layer [43], but this layer induces an increase in the resistance between the device and the substrate. Finally, the thermal expansion coefficient of SiC is less than that of AlN or GaN: due to this, the films are usually under biaxial tension at room temperature. This fact induces an increase of defect concentration, thus limiting the device reliability [44].

1.3.3 Silicon (Si)

Gallium nitride growth performed on silicon substrate represent a very attractive option for the realization of GaN-based devices for several reasons: first of all, silicon has excellent physical properties and it is available in large size wafer. Moreover silicon has a very low price and its crystal perfection is better than any other substrate material used to grow GaN films. Silicon has also good thermal stability under GaN epitaxial growth conditions and its surfaces can be prepared with good smooth finishes. In addition, there is a certain interest in the possibility of integrating optoelectronic GaN devices with electronic Si devices [45].

However, the quality of GaN films grown on silicon substrates is still very poor if compared to those grown on sapphire and silicon carbide substrates: this is due to the large lattice mismatch (17 %) and thermal expansion coefficient (56 %) between silicon and epitaxial gallium nitride and to the tendency of silicon to form

an amorphous silicon nitride layer Si_xN_y at the GaN/Si interface when exposed to reactive nitrogen sources. In order to avoid the formation of this amorphous nitride layer, buffer layers are usually deposited first on the silicon substrate, thus enhancing wetting and reducing the reactivity of the substrate. Furthermore, the buffer layers provide also a better lattice matching between the GaN film and the substrate. Finally, note that the thermal expansion coefficient of Si is more than two times lower as compared to that of GaN: this results in cracking of GaN layers during the cooling phase [46].

1.3.4 GaN substrates

In recent years, many efforts have been done in order to prepare high quality GaN films that can be subsequently used as homoepitaxial substrates for the GaN growth. GaN substrates are only recently available in n-conducting and semi-insulating form with diameters suitable for electronic device fabrication, i.e. of about 2-in [28]. This substrate in particular offers the best control over surface morphology, defect density and doping concentration. In fact, with homoepitaxial growth the defects, impurities and stress between different layers can be greatly reduced, thus leading to an increase in the device performances. Furthermore, the growth procedure can be strongly simplified because the process does not require additional steps, such as surface nitradation and low-temperature buffer layer growth. Note also that GaN substrates have high thermal and electrical conductivity, which makes devices grown on this substrate potentially more reliable.

Hydride vapor phase epitaxy (HVPE) represent the leading technique for growing bulk GaN materials [47] [48]: samples grown with this technique have low dislocation densities (about $2 \cdot 10^7\ cm^{-2}$). For all these reasons explained above, homoepitaxial GaN represents a very attractive perspective for the future development of high quality GaN-based devices.

1.3.5 AlN, ZnO and Diamond substrates

Nowadays also AlN substrates are under discussion for GaN growth: in particular this material is highly resistive and has a better thermal conductivity than GaN (actually its thermal conductivity is close to that of SiC). Furthermore AlN has a very low lattice mismatch. Free-standing AlN substrates with a thickness of 112 μm based on a Si(111) host substrate have recently been reported [49]. Note that AlN substrates may also enable more growth orientations and reduce the need of complex strain engineering. In Table 1.2 are summarized the basic properties of substrates for GaN growth that have been analyzed in this section.

Also wurtzitic zinc Oxide (ZnO) substrates are now available as large single

crystals: for the optoelectronic applications, it is attractive due to lattice mismatch with gallium nitride of only 2%.

Finally, also CVD diamond has been recently employed as substrate. Note that CVD diamond provides the highest thermal conductivity of any other substrate material. The devices are initially grown on Si substrate and then transferred to the CVD diamond via an atomic attachment process. The devices are found to be relatively dispersive and the beneficial impact of the improved heat removal cannot be clearly demonstrated [28].

Material	Lattice constant a [Å]	Mismatch to GaN (%)	Thermal conductivity ($Wm^{-1}K^{-1}$)	Thermal expansion coefficient ($10^{-6}\,K^{-1}$)	Isolation ($\Omega\,cm$)
GaN	3.189	0	130	5.59	$\geq 10^9$
6H SiC	3.08	3.4	490	4.2	$\geq 10^{11}$
6H s.i. SiC	3.08	3.4	370	4.2	$\geq 10^{11}$
Sapphire	$4.758/\sqrt{3}$	13	50	7.5	-
Silicon	5.4301	17	150	3.59	1-3 10^4
AlN	3.112	1	200	4.2	$\geq 10^{12}$

Table 1.2: Basic properties of some common substrate materials used for GaN growth.

1.4 GaN doping

The doping of gallium nitride is of fundamental importance, as in any semiconductor, in order to realize optoelectronics devices, such as LEDs and laser diodes. In this section we will review the properties of n and p-type dopants used for GaN and the main doping issues of III-nitride materials that have been encountered in the last years. III-N semiconductors are tipically doped with impurities such as Si, Ge, Se, O, Mg, Be and Zn. However, also unintentional impurities can be found in these semiconductor materials, including C, H, O and grown-in defects, such as vacancy and antisite point defects [28]: in particular the impurities induce a high unintentional n-type doping in gallium nitride: this factor, combined with the high material defectivity, due to the absence of an ideal substrate, have limited advances in GaN doping. Another factor has limited the development of high quality p-type GaN films: the most common acceptor dopant, i.e. Mg, can be easily compensated by hydrogen, thus strongly reducing the hole concentration obtainable from the doping process. All these factors will be discussed in more details in the following.

1.4.1 *n*-type doping

In blue LEDs, Silicon and Germanium are tipically used as n-type dopants for GaN films. However, as stated above, one of the major issues related to the control of n-type doping in GaN is represented by the high unintentional donor concentration present in gallium nitride. This problem was initially attributed to native defects [50], but more recent studies [51] [52] have ascribed this problem to the presence of nitrogen vacancies in the semiconductor. Further studies reported in [53] and [54] have suggested that the intrinsic n-type doping of gallium nitride is most likely due to the presence of unintentional impurities such as oxygen and silicon, which are calculated to be shallow donors with high solubility and thus they can react with semiconductor material, generating n-type conductivity.

Nowadays it is possible to grow high quality GaN films with a low intrinsic carrier concentration, thanks also the advances on MOCVD technique [51]: because there are fewer crystal defects or residual impurities, it has become possible to accurately control the n-type doping in gallium nitride.

Germanium is a shallow donor in GaN, which has an activation energy for ionization of 19 meV. This dopant is incorporated during growth by the reaction between GeH_4 and trimethilgallium and ammonia. By this way it is possible to obtain germanium concentration as high as $2 \cdot 10^{19}\, cm^{-3}$ [51].

On the other hand, silicon is a shallow donor with an activation energy similar to that of germanium and silicon doping is achieved by a similar reaction to that of germanium, using silane (SiH_4) as a precursor. It is important to point out that silicon easily fitting in on a Ga site, but it causes a large strain if it replaces a N atom or go on a interstitial site [54]: this is related to the fact that silicon has an atomic radius similar to gallium. For this reason, silicon is the most widely used donor dopant for GaN. It is preferred to germanium as n-type dopant also for the higher efficacy of the silicon incorporation process with respect to germanium.

1.4.2 *p*-type doping

Systematical research in the GaN system began in the 1960s. However, for a long time it was impossible to obtain high quality p-type GaN films and this fact has prevented the development of GaN-based LEDs and laser diodes. Different attempts of achieving p-type doping of GaN have been done using several acceptors elements, including lithium, sodium, potassium, beryllium, zinc, calcium and magnesium: the tests have demonstrated that magnesium is the best choice and for this reason in the last years many efforts have been done in order to realize stable Mg-doped GaN films [55].

The difficult in obtaining efficient p-type doping in GaN was partially due to

the high residual n-type background resulting from nitrogen vacancies or silicon or oxygen impurities. Another problem in p-type GaN is represented by the low doping activation, which is caused by two effects [34]: first, the chemical deactivation of acceptors by hydrogen atoms bonding to the acceptors. The role of hydrogen in p-type doping of gallium nitride will be discussed in more detail in the subsequent section. Second, the acceptors in gallium nitride have a high thermal activation energy, which is $\gg kT$ at room temperature (160-200 meV [44]): as a results, only a small percentage of acceptors are ionized at 300 K.

Amano *et al.* have demonstrated that acceptor dopants can be activated by means of Low-Energy Electron-Beam Irradiation (LEEBI) [56]: with this technique it is possible to break Mg-H bonds formed after growth of Mg-doped GaN layers and to obtain a hole concentration of $2 \cdot 10^{16}\, cm^{-3}$, which correspond a resistivity value in the order of 35 $\Omega \cdot cm$. A few years later, Nakamura *et al.* showed that acceptors can be activated also submitting the as-grown GaN layers to thermal annealing [51]. Typical thermal annealing conditions for MOCVD-grown p-type GaN are $675 - 725\ ^{\circ}C$ for 5 minutes in N_2 atmosphere; p-type $Al_{0.30}Ga_{0.70}N$ is annealed at higher temperatures, in the order of 850 $^{\circ}C$ for 1-2 minutes [34]. In Figure 1.11 it is shown the resistivity of Mg-doped GaN films as a function of annealing temperature: it can be observed that the resistivity is in the order of $10^6\, \Omega \cdot cm$ for low annealing temperatures, while it decreases to values as low as 2 $\Omega \cdot cm$ after treatment at 700 $^{\circ}C$. During thermal annealing, the relatively weak magnesium-hydrogen bond is broken and the hydrogen atoms are driven out of the epitaxial film. It is also believed that heating caused by LEEBI has a similar effect.

Youn *et al.* in [57] have demonstrated that there is an optimum annealing temperature, which results in the highest hole concentration, depending on the existing defects in Mg-doped GaN layers. In fact, they observed that for very high temperatures the hole concentration was decreased: this phenomenon was attributed to the generation of nitrogen vacancies compensating Mg at high annealing temperatures, but it is necessary to take into account also of the possibility of defects generation or other thermal effects.

Furthermore, other authors have shown that the activation process can be helped also by the presence of minority carriers [58]: in fact it was shown that the resistance of Mg-doped layer decreases under forward bias.

Another process that limits the performances of Mg-doped GaN layers is the self-compensation caused by the formation of $Mg_{Ga} - V_N$ deep donor, namely the nearest-neighbor association of Mg acceptor with nitrogen vacancy. The nitrogen vacancy, V_N, acts as a donor for GaN and thus, the V_N and Mg acceptors, which are oppositely charged, attract each other, tending to form $Mg_{Ga} - V_N$ [59] [60]. In order to limit this problem, it has been proposed to introduce nitrogen in the

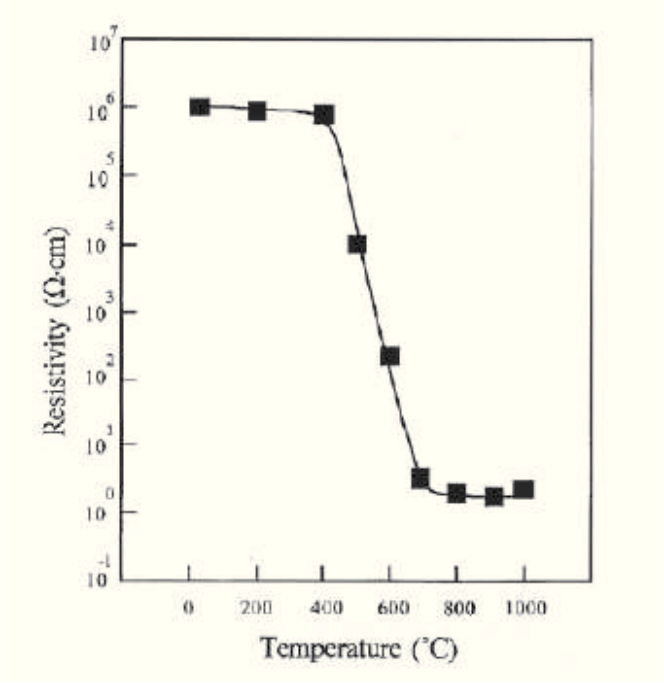

Figure 1.11: Resistivity of Mg-doped GaN layers as a function of annealing temperature in N_2 atmosphere.

growth chamber: by this way it is possible to fill the vacancies and to increase the hole concentration.

Finally, it is important to note that there is an upper limit for Mg incorporation as shallow acceptors, that is around $2 \cdot 10^{19}\, cm^{-3}$: further Mg-atoms forms deep donors, which are believed to be Mg-nitrogen vacancy complexes. Those deep donors compensate the Mg-acceptors resulting in the decrease of free holes and therefore the increase in the specific resistance. This effect can be observed also in the diagram reported in Figure 1.12.

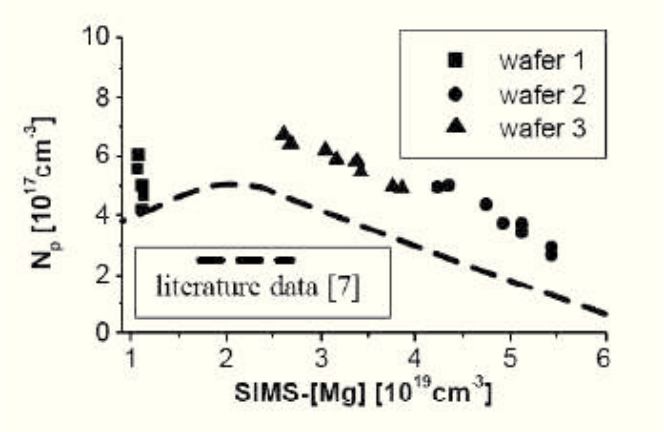

Figure 1.12: Hole cocnentration as a function of Mg concentration in Mg-doped GaN layer [61].

1.4.3 Role of hydrogen in gallium nitride

Hydrogen is contained in most of the reagents and liquids used in the growth, annealing and processing of semiconductors: for example H_2 is used as flow gas in MOCVD reaction. For this reason the hydrogen is the most present impurity in GaN layers. It is well known that molecular hydrogen, i.e. in the H_2 form, is chemical inactive, but on the other hand, atomic hydrogen, both in the H^0, H^+ and H^- form, diffuses rapidly even at low temperatures and it is very reactive with magnesium atoms. It can form neutral complexes with dopants, thus compensating the effect of dopants, as expressed by the following reactions:

$$D^+ + H^- = (DH)^0 \tag{1.5}$$

$$A^- + H^+ = (AH)^0 \tag{1.6}$$

where D^+ and A^- represent ionized donors and acceptors, respectively. These reactions can induces an increase in the resistivity of semiconductor. In particular it has also been demonstrated that hydrogen acts as a donor (H^+) in p-type GaN and as an acceptor (H^-) in n-type GaN, always counterating the prevailing conductivity.

The reaction between hydrogen and magnesium occurring in Mg-doped GaN layers is very critical: it can form neutral complexes, thus passivating the dopant. The chemical reactions involving hydrogen in Mg-doped GaN are the following:

$$H^+ + Mg^- \longrightarrow MgH \tag{1.7}$$

$$H^0 + Mg^0 \longrightarrow MgH \tag{1.8}$$

We have already seen in the previous section that the magnesium acceptor can be reactivated by post-growth annealing at high temperatures ($> 700\ ^\circ C$): with this method is also possible to remove the hydrogen from the p-type material. Other treatments that permit to reactivate the magnesium at lower temperatures, but without removing the hydrogen from the material, are LEEBI and minority carrier injection. We point out that the minority-carrier injection into the p-type region under forward bias leads ultimately to the formation of neutral interstitial H_2, that remains in the semiconductor material, according to the following reactions:

$$MgH \longrightarrow Mg^- + H^+ \text{ (Thermal dissociation)} \tag{1.9}$$

$$H^+ + e^- \longrightarrow H^0 \text{ (Hot electron capture)} \tag{1.10}$$

$$H^0 + e^- \longrightarrow H^- \text{ (Hot electron capture)} \tag{1.11}$$

$$H^- + H^+ = H_2 \tag{1.12}$$

where it is supposed that the breaking of the Mg-H bonds is due to the presence of hot electrons. Thermal electrons are not involved in this process because they recombine close to the junction and cannot reach higher depths. Thus, we can observe that H_2 molecules are not removed from the material. It is important to stress that this process is reversible, i.e. a subsequent annealing at temperature greater than 400 $^\circ C$ leads to a complete re-passivation of dopant through the following chemical reactions:

$$H_2 \longrightarrow H^+ + H^- \text{ (Thermal dissociation)} \tag{1.13}$$

$$H^- + h^+ \longrightarrow H^0 \text{ (Hole capture)} \tag{1.14}$$

$$Mg^- + H^+ \longrightarrow MgH \tag{1.15}$$

$$Mg^0 + H^0 \longrightarrow MgH \tag{1.16}$$

For the case of p-GaN, the hydrogen concentration is usually the same as the active Mg after growth. At 700 $^\circ C$, 20 minutes post-growth annealing in N_2 only reduces the hydrogen concentration by a factor of 2 or 3, but this is enough to have strong p-type conductivity.

1.5 Ohmic contacts on GaN

The formation of ohmic contacts on both n-type and p-type GaN layers is a fundamental component in the fabrication of optoelectronic devices. During the fabrication of ohmic contacts on GaN, four fundamental parameters have to be considered: annealing, surface treatment, doping concentration, and surface polarity. Annealing forms an intermediate compound at the interface or generates donor-type defects on the surface, which helps electron transport by tunneling. Surface treatment produces mechanical damage to the surface, which induces the donor-type defects. Doping concentration has a direct relationship with the Schottky barrier narrowing. Finally, also different polar surfaces result in different contact characteristics. In this section we will briefly discuss the most common materials and structures used for the realization of ohmic contacts on gallium nitride.

1.5.1 Ohmic contacts on n-GaN

For n-contacts on III-nitrides, intrinsic doping is the most important contender for reducing the contact resistance. We can define the Schottky barrier height of a contact on n-GaN as

$$q\phi_{SM} = q\left(\phi_M - \chi_S\right) \tag{1.17}$$

where ϕ_M represents the work function of the metal, while χ_S is the electron affinity of the semiconductor. The energy gap of n-GaN at room temperature E_G is equal

to 3.39 eV, and the electron affinity χ_S is 4.11 eV. However, the work function of most of the metals yields quite large Schottky barrier height ϕ_{SM}, so that carrier transport through the contact, due to pure thermionic emission, is rather difficult. In order to reduce the resistivity of ohmic contacts on n-GaN, the surface doping concentration is usually increased, with the aim to enhance tunneling injection.

Actually, the carrier flow in a ohmic contact is due both to tunneling and thermionic emission, in different proportions. A possible way to reduce the barrier height of contact is causing band-narrowing (BGN) of the conduction band. Consider a n-GaN layer with heavy doping, which creates an increasing number of new donor-type energy levels underneath the conduction band edge. Under these circumstances, the donors are so close together that donor levels degenerate merging together to create an impurity band: this fact thus induces a bandgap narrowing of the conduction band and this effect in particular is more prominent near the M/S interface. As a consequence, the barrier height ϕ_B is reduced, as shown in the band diagram of Figure 1.13. The new barrier height ϕ_{BE} becomes $\phi_{BE} = \phi_B - \Delta E_G$, where ϕ_B is the barrier height without BGN.

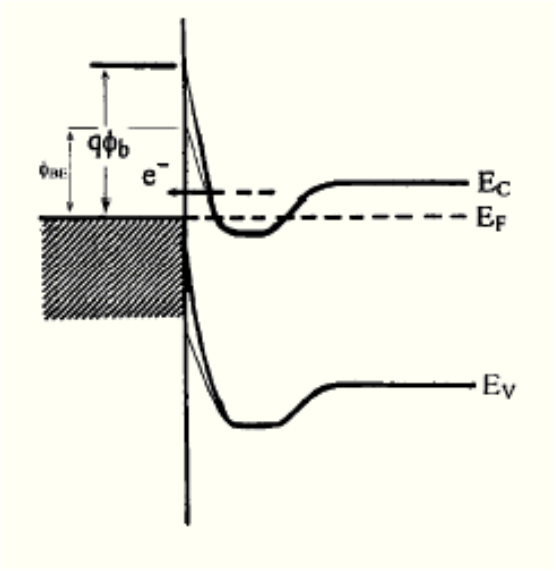

Figure 1.13: Schematic band diagram showing the reduction of barrier height at the interface M/S due to the bandgap narrowing. Note that ϕ_B is the height barrier without BGN, and ϕ_{BE} is the barrier height with BGN.

There are a number of design requirements that have been satisfied, in order to obtain low-resistivity contacts on n-GaN layers: among these, we can remember the alloyed contacts described in [62] and shown in Figure 1.14. These alloyed contacts should have a barrier layer, that must be metallic, located immediately close to the n-GaN layer, which acts as a barrier against the diffusion of the other metal layers toward n-GaN. The barrier layer should have a low work function and materials as TiN, TaN, ZrN, CoN are usually preferred to create this layer,

because they can be conveniently formed by the solid phase chemical reaction of the barrier layer metal (for example Ti, Ta, Zr, Co) with the N atoms of n-GaN. Moreover, the outdiffusion of N atoms from n-GaN to form these layers generates N vacancies, that are known to act as n-type dopant atoms, which can increase tunneling probability [59].
The contact should have also an overlayer metal, that acts as a sink for N atoms into the barrier layer metal enhancing solid phase chemical reaction between the nitrogen atoms and the metal atoms of the barrier layer. A good candidate for this role can be aluminum, as it does not create a large work function alloy, nor a thick wide bandgap material upon alloying.
Finally, one or more cap layers can be needed, in order to ensure the stability of system: in fact, it is important to take into account that the barrier layer metal and the overlayer metal may have high propensity for oxidation.

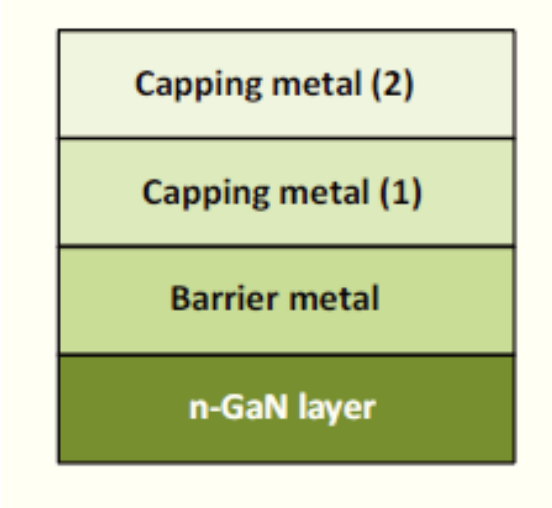

Figure 1.14: Schematic diagram showing an alloyed ohmic contact on n-GaN: the barrier layer, overlayers and cap layers ca be noticed in this typical structure.

Among the many contact metalization schemes that can be found in literature, Ti/Al-based contacts are the most widely used for ohmic contact formation to n-GaN and n-AlGaN, being the most common metal scheme Ti/Al/Ti/Au [63]. However, despite providing low contact resistances, Ti/Al-based ohmic contacts exhibit significant limitations, such as the formation of low-melting $AlAu_4$ phase, responsible for lateral flow during alloying at high temperatures [64]. In the recent years, many strategies for improving ohmic contacts have been proposed, including the employment of high melting point metals, such as Mo, V, W, WSi_x and Ir, acting as metal barrier, showing very promising results [65]: these metals confer more thermal stability and reproducibility then conventional ones.

1.5.2 Ohmic contacts on *p*-GaN

The difficulty of obtaining good quality ohmic contacts on *p*-GaN has represented one of the major factors that have limited the development of reliable and high efficient GaN-based optoelectronic devices. In the first experiments the specific contact resistance was very high: due to this fact, the metalization self-heating was strong, thus leading to metal migration through threading dislocations and eventual shorting of the junction. Several factors limit the specific contact resistance of ohmic contacts realized on *p*-GaN, including the following:

- The absence of a metal with a sufficiently high work function. In fact, it must be taken into account that the bandgap of GaN is 3.4 eV, the electron affinity is 4.1 eV, but metal work functions are tipically $\leq$ 5 eV. To better understand this fact, note the schematic band diagram of a *p*-type contact on GaN shown in Figure 1.15.
- The relatively low hole concentration in *p*-GaN.
- The tendency for the preferential loss of nitrogen from the GaN surface during processing: this can produce surface conversion to *n*-type conductivity.

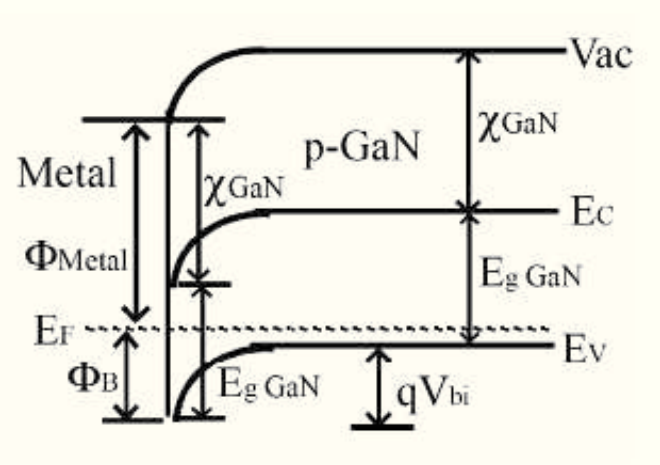

Figure 1.15: Schematic band diagram of a typical metal/*p*-type semiconductor junction.

High work function metals are tipically employed for the realization of ohmic contacts on *p*-GaN, such as Pd, Pt, Ni, or Cr, with an overlayer of Au. After the deposition, these metals are annealed at $400 - 750\ ^{\circ}C$, in order to increase the hole concentration of the surface through the depassivation of Mg-H complexes and formation of Ga vacancies through reaction with Au. Studies performed on these contacts have revealed that conduction processes are dominated by tunneling [61] and they also have a typical transmittance of around 60-75 % [66]. However, these

contacts have shown stability problems at high temperatures: in fact, degradation of Ni/Au contacts has been demonstrated, which can be ascribed to the formation of an islanded contact morphology, to the formation of reactions with the GaN resulting in a modification of the doping profile, and to the intermixing of Ni and Au, leading to the oxidation on the rough Ni surface and an increase of the series resistance [67].

A possible way to prevent excessive intermixing and contact morphology degradation is to use a high-melting-point diffusion barrier in the contact stack, but the transparency of such materials is low. However, an improvement in contact technology can be given by the use of Au-free structures: one of these is represented by thin oxides, such as Indium Tin Oxide (ITO). ITO films have some interesting properties, including: *(i)* high transparency in the visible spectrum (around 90 %), *(ii)* low electrical resistivity ($\ll 5 \cdot 10^{-4}\,\Omega cm$), and *(iii)* capability to provide high carrier concentration ($10^{20} - 10^{21}\,cm^{-3}$) and applicable mobility ($25 - 50\,cm^2/Vs$) [68]. However, optical properties of these contacts are limited by the high refractive index (2.1-2.5 at 405 nm of GaN-related materials and indium tin oxide), resulting in a reduced escape cone for the emitted light, so increasing considerably the total internal reflection phenomenon. In order to enhance the light extraction efficiency, several methods can be adopted, such as laser lift-off, GaN surface roughening, and contact layer patterning [69].

1.6 GaN alloys

Gallium nitride alloys are widely used in GaN-based optoelectronic devices, in order to realize heterostructure and quantum well structures, thus obtaining carrier confinement inside the active region, and to tune the desired wavelength emission, which is dependent on the material composition. More details about heterostructure and quantum well LEDs will be given in the next chapter. Ternary alloys of gallium nitride are usually obtained combining wurtzite polytypes of GaN, AlN, and InN, because they form a continuous alloy system whose direct bandgap ranges from ≈ 0.8 eV for InN to 6.1 eV for AlN. In particular, many properties of GaN alloy, such as the energy bandgap, effective masses of electrons and holes, and the dielectric constant, are dependent on the alloy composition.

The ternary AlGaN alloy has an energy bandgap greater than GaN and for this reason it is tipically used to form barrier layers inside the quantum wells, in order to obtain the carrier confinement in quantum well structures, or to realize the electron blocking barrier to limit the diffusion of electrons towards the p-type layer of GaN-based LEDs. AlN and GaN are reasonably lattice-matched (the lattice mismatch in only 3.9 %). Moreover, due to the wide band gap of AlN, only small

amounts of AlN are needed in the GaN lattice to provide sufficient carrier and optical field confinement in most of GaN-based optoelectronic devices. in general, the compositional dependence of the optical bandgap of AlGaN can be predicted by the following empirical expression:

$$E_g(Al_xGa_{1-x}N) = xE_g(AlN) + (1-x)E_g(GaN) - x(1-x)b \tag{1.18}$$

where $E_g(AlN)$ and $E_g(GaN)$ are the optical bandgap of AlN and GaN, respectively, and x and b are the AlN molar fraction and bowing parameter, respectively. In order to determine this relationship, precise characterization of both the bandgap and alloy composition is important. In particular, extensive studies have estimated a bowing parameter of $b = 1$ eV for the entire range of alloy composition. However it is important to consider that the validity of the characterization techniques used in determination of the optical properties of AlGaN alloys is deeply affected by the material crystalline quality and purity.

The InGaN ternary alloy has a energy bandgap smaller than GaN and thus it is mostly used to realize quantum wells in the active region of LEDs and lasers. In principle it is possible to obtain devices with emission wavelength comprised between violet, through blue and green, to red spectral region: however added complexity such as phase separation and other inhomogeneities due to the large disparity between Ga and In limits the indium incorporation in GaN to quite low values. Similarly to the case of AlGaN, the compositional dependence of the optical band gap of InGaN can be expressed as follow:

$$E_g(In_xGa_{1-x}N) = xE_g(InN) + (1-x)E_g(GaN) - x(1-x)b \tag{1.19}$$

where the bandgap of InN instead of that of AlN is used. Different values for bowing parameter have been estimated in different works: an earlier investigation of InGaN bowing parameter for alloys with small concentration of InN led to a bowing parameter of 1.0, which is in disagreement with 3.2 reported by Amano *et al.*. On the other hand, a bowing parameter of 2.5 eV was obtained from optical absorption measurements and a value of 4.4 eV was obtained from the position of emission peak. Finally, Nagatomo *et al.* noted that the $In_xGa_{1-x}N$ lattice constant varies linearly with the In mole fraction up to a least $x = 0.42$, but it violates the Vegard's law for $x > 0.42$: this fact can be caused by erroneous determination of the composition.

1.7 Crystallographic defects on GaN

Gallium nitride, as any other crystalline semiconductor, contains several crystallographic defects: these are generated during crystal growth, due for example to

the lattice mismatch between substrate and semiconductor material, or to the introduction of foreign atoms in the crystal structure present, for example, in the atmosphere of deposition chamber. Defects can strongly degrade electrical and optical properties of the semiconductor material: for example, in the previous section, we have already seen that nitrogen vacancies induce an unintentional n-type doping, which can make it difficult the realization of p-type doping on GaN. Furthermore, crystallographic defects can act also as non-radiative recombination centers, which strongly reduce the optical efficiency of devices. In particular, the concentration of defects can be very high in gallium nitride, due mainly to the high lattice mismatch between this semiconductor material and the typical substrates used for the growth, as we have already seen in the previous sections. For this reason, it is necessary to deeply understand the origins of defects in gallium nitride and as they can influence the electrical and optical properties of semiconductor. It can be identified three basic classes of crystallographic defects:

- ***point defects***, which are places where an atom is missing or irregularly placed in the lattice structure;
- ***linear defects***, also called *dislocations*, which are groups of atoms in irregular positions;
- ***planar defects***, which are interfaces between homogeneous regions of the material.

In this section we will briefly discuss each of these classes of defects in gallium nitride. These concepts are necessary for the understanding of the subsequent chapters.

1.7.1 Point defects

Point defects are defects that occur only at or around a single lattice point; they are not extended in space in any dimension. Point defects include self interstitial atoms, interstitial impurity atoms, substitutional impurity atoms, vacancies, Frenkel defects and antisite defects. A schematic illustration of these point defects (except for antisite defects) is reported in Figure 1.16.

A ***self-interstitial atom*** is an extra atom that has crowded its way into a interstitial void in the crystal structure. On the other hand, an ***interstitial impurity atom*** is a foreign atom that fit into the open space between the bulk atoms of the lattice structure. Interstitial impurity atoms are much smaller than the atoms in the bulk structure. An example of interstitial defect on gallium nitride is represented by hydrogen, that can passivate the magnesium dopant in p-type

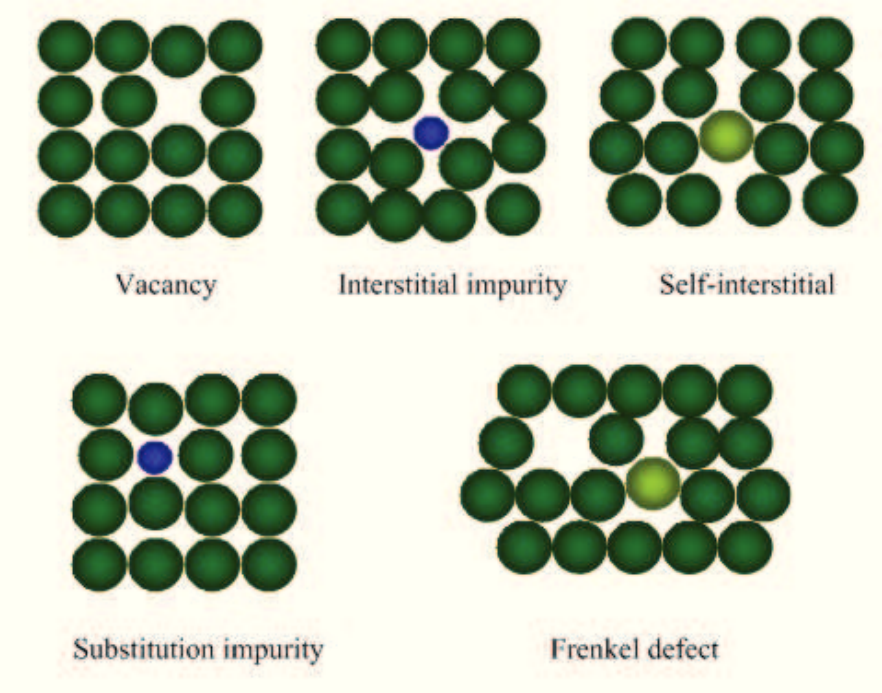

Figure 1.16: Schematic illustration of typical point defects in a crystal structure: a vacancy, interstitial impurity, self interstitial atom, substitution impurity and Frenkel defect can be observed.

layers, thus reducing the hole concentration. The role of hydrogen has been already discussed in section 1.4.3.

A ***substitutional impurity atom*** is an atom of a different type than the bulk atoms, which has replaced one of the bulk atoms in the lattice. The effects of this impurity on the surrounding crystal structure depend also by the dimension of the substitutional atom, but these atoms are usually close in size (within approximately 15 %) to the bulk atom. The most relevant substitutional impurity atoms in GaN are hydrogen, which effect has been described above, oxigen, which acts as a surface donor that causes unintentional n-type doping, and carbon, which acts as an acceptor dopant [70].

Vacancies are empty spaces where an atom should be, but is missing. They are common, especially at high temperatures when atoms change frequently and randomly their positions, leaving behind empty lattice sites. The stability of the surrounding crystal guarantees that the neighboring atoms will not simply collapse around the vacancy. An example of vacancies in gallium nitride is represented by nitrogen vacancies, which, as stated above, act as donors, thus inducing a unintentional n-type doping.

A nearby pair of a vacancy and and a interstitial is called a ***Frenkel defect***. This is caused when an ion moves into a interstitial site and creates a vacancy. Finally, ***antisite defects*** occur in a ordered alloy or compound when atoms of

different type exchange positions.

1.7.2 Linear defects

Linear defects, also called dislocations, are another type of defect in crystals. Dislocations are areas where the atoms are out of position in the crystal structure. Dislocations are generated and move when a stress is applied. There are two basic types of dislocations: the edge dislocation and the screw dislocation. However, mixed dislocations, combining aspects of both types, are also common.

Edge dislocations are caused by the termination of a plane of atoms in the middle of a crystal. In such a case, the adjacent planes are not straight, but instead bend around the edge of the terminating plane so that the crystal structure is perfectly ordered on either side. A schematic illustration of an edge dislocation in shown in Figure 1.17(a). On the other hand, a ***screw dislocation*** forms when one part of crystal lattice is shifted (through shear) relative to the other crystal part. It is called screw as atomic planes form a spiral surface around the dislocation line. Even if the screw dislocation is slightly more difficult to visualize, a schematic illustration of this type of defect is depicted in Figure 1.17(b).

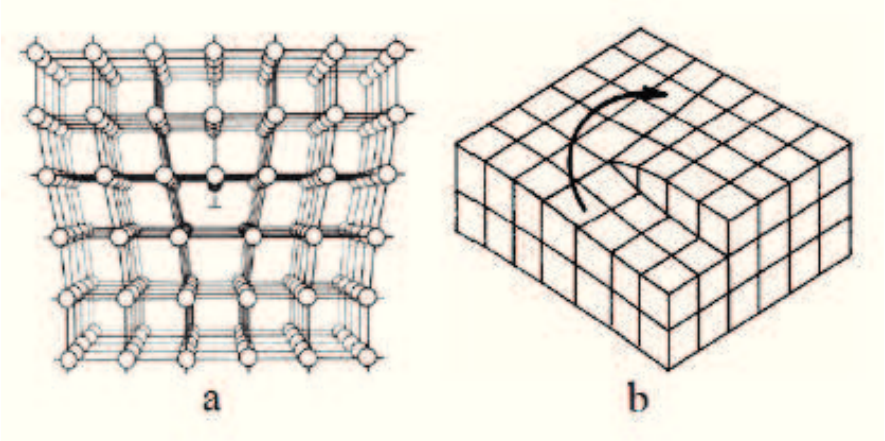

Figure 1.17: Schematic illustration of (a) edge dislocation and (b) screw dislocation in a crystal structure.

The presence of dislocations result in lattice strain (distortion). Dislocations can move if the atoms from one of the surrounding planes break their bonds and rebond with the atoms at the terminating edge. In gallium nitride dislocations form as a consequence of the lattice mismatch between GaN and the substrate used for growth. As a result, GaN epitaxial films have misfit dislocations (threading and edge dislocations), that are tipically on the order of $10^8 - 10^9\, cm^{-2}$ [34].

As an example, in Figure 1.18 are schematically shown the initial stages of GaN growth on a sapphire substrate: it can be observed that the initial layer,

also called the fault zone, which is grown at low temperatures (about 500 $°C$) and subsequently annealed, is highly dislocated. However, dislocations undergo self-annihilation during anneal, so that subsequent layer, indicated in the figure as semi-sound zone and sound zone, have much lower dislocation densities.

Generally, dislocation lines are electrically charged so that the region surrounding

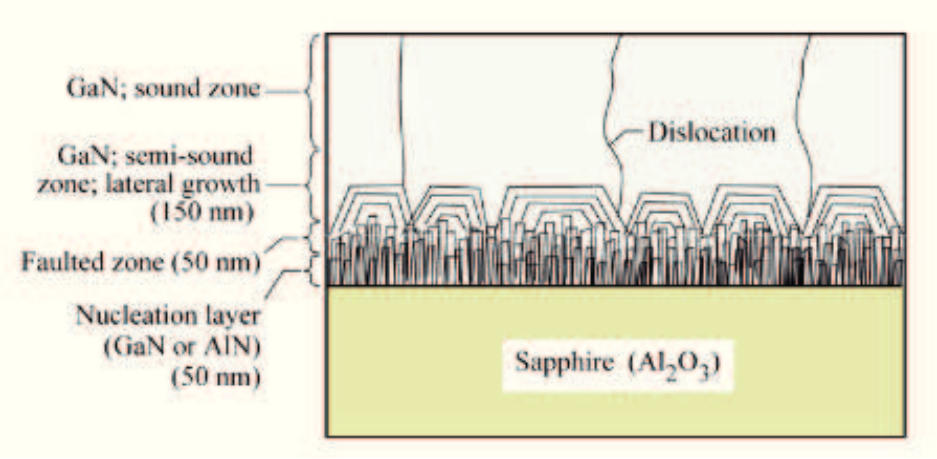

Figure 1.18: Dislocation structure of a GaN epitaxial layer grown with the nucleation layer on a sapphire substrate.

a dislocation line is either coulombically attractive or repulsive to a free carrier [34]. The nature of the coulombic interaction (attractive or repulsive) depends on the polarity of the dislocation line and the polarity of the carrier [34]. For example, in Figure 1.19 is shown the band diagram of a semiconductor with a negatively charged dislocation line, which is attractive for holes and repulsive for electrons.

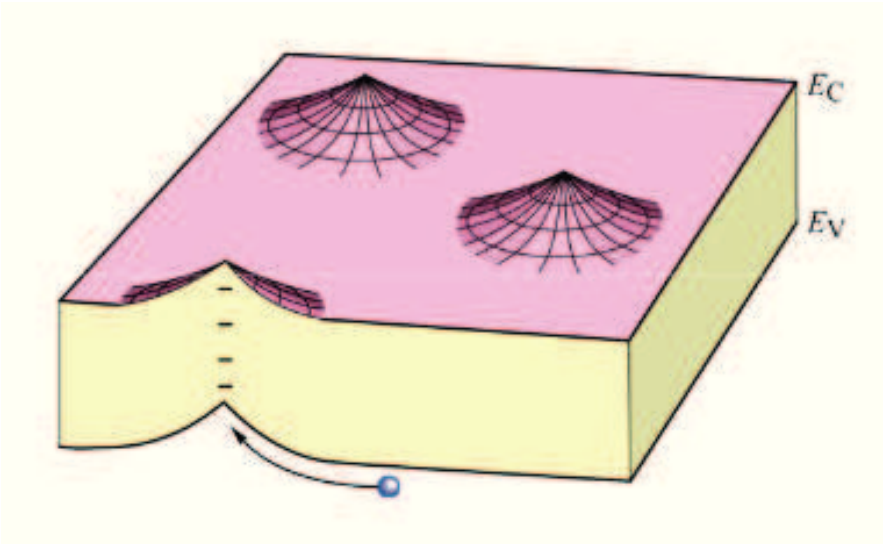

Figure 1.19: Band diagram of a semiconductor having negatively charged dislocation lines.

Dislocations act as non-radiative recombination centers: to understand this

fact, consider the temporal development of the carrier dynamics of a positively charged dislocation line shown in Figure 1.20. Initially electron are attracted by the potential of dislocation line, but holes are repelled. However, the continued collection of electrons will screen the dislocation potential. This phenomenon thus reduces the repulsive barrier of holes and as a result, electrons and holes will recombine non-radiatively via electron states of the dislocation line.

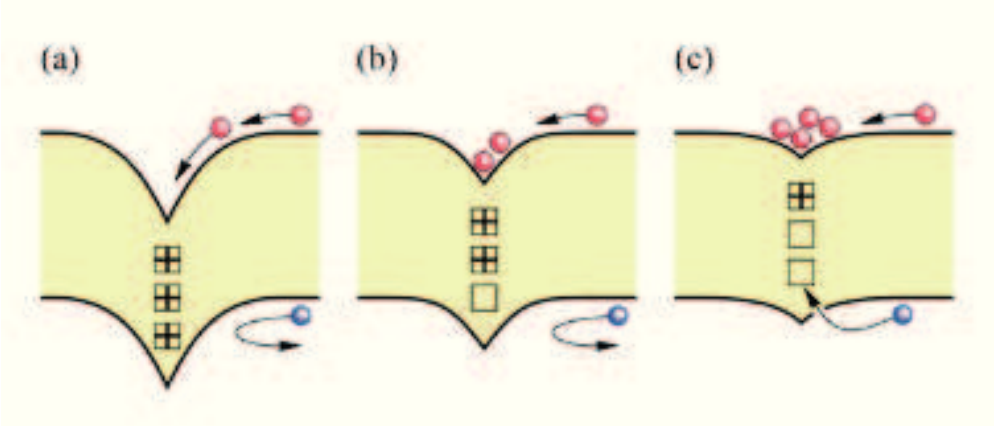

Figure 1.20: Non-radiative recombination process occuring in a positively charged dislocation line. Note that electronic states of the dislocation are located within the bandgap.

1.7.3 Planar defects

A planar defect is an imperfection in form of a plane between uniform parts of the material. The most important ***planar defect*** is a grain boundary. Grain boundaries occur where the crystallographic direction of the lattice abruptly changes: this usually occurs when two crystals begin growing separately and then meet. To better understand the origin of grain boundaries, we have to consider that solids generally consist of a number of crystallites or grains. Grains can range in size from nanometers to millimeters and their orientations are usually rotated with respect to neighboring grains. Where one grain stops and another begins is known as a grain boundary.

A disruption of the long-range stacking sequence can produce two other common types of crystal defects: *(i)* a ***stacking fault*** and *(ii)* a ***twin region***. A change in the stacking sequence over a few atomic spacings produces a stacking fault, whereas a change over many atomic spacings produces a twin region. A stacking fault is a one or two layer interruption in the stacking sequence of atom planes. A schematic illustration of a stacking fault is provided in Figure 1.21.

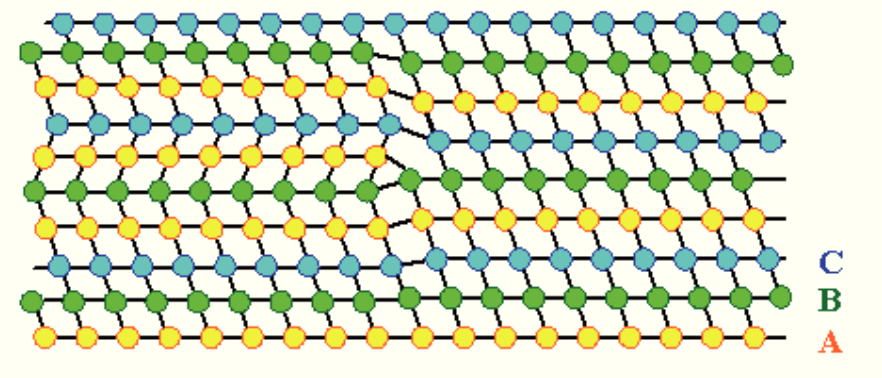

Figure 1.21: Schematic illustration of a stacking fault in a crystal structure.

1.7.4 Bulk defects

Even if bulk defects occur on a much bigger scale than the rest of crystal defects, it is important to give a brief description of this type of defect, also because they affect the movement of dislocations. The most common bulk defects are voids and precipitates. ***Voids*** are regions where there are a large number of atoms missing from the lattice: thus they can be thought as clusters of vacancies. On the other hand, ***precipitates*** occur when impurity atoms cluster together to form small regions of a different phase. The term phase refers to that region of space occupied by a physically homogeneous material.

Chapter 2

LED basics

The operation of Light Emitting Diodes (LEDs) is based on the spontaneous emission of photons from the active region of a *pn* junction. Consider the LED structure based on a *pn* homojunction shown in Figure 2.1: When the LED is operated under forward bias, electrons diffuse from the *n*-side to the *p*-side and holes diffuse from the *p*-side to the *n*-side, respectively. Under this condition there is a small region near the junction, where both the electron and hole concentration is high: as a consequence also the recombination probability is high in this region and thus electron-hole pairs can recombine radiatively, resulting in the emission of photons, whose energy is related to the bandgap of semiconductor material. This phenomenon is also known as ***electroluminescence***. However, electron-hole pairs can also recombine non-radiatively, resulting in this case in the emission of a phonon. In order to obtain LEDs with high luminous efficiency, it is important to maximize the radiative recombination and limit non-radiative recombination.

As it can be seen in the band diagram of Figure 2.1, when an electron recombines with an hole, it makes a transition from the conduction band to the valence band, emitting a photon with energy approximately equal to the energy gap of the semiconductor, that is:

$$h\nu \approx E_g \tag{2.1}$$

which corresponds the following emission wavelength in the vacuum:

$$\lambda = \frac{hc}{E_g} = \frac{1.24}{E_g(eV)} \quad [\mu m] \tag{2.2}$$

where h is the Planck constant and c the speed of light in the vacuum. Thus, the emission wavelength depends on the energy gap, that is a material property. In fact, in compound semiconductors, it is possible to determine the emission wavelength varying the composition of material, for example changing the relative indium composition in the InGaN ternary alloy.

Because the LED operation is based on spontaneous emission, photons are emitted with random phase and direction, i.e. the emitted light is incoherent, differently

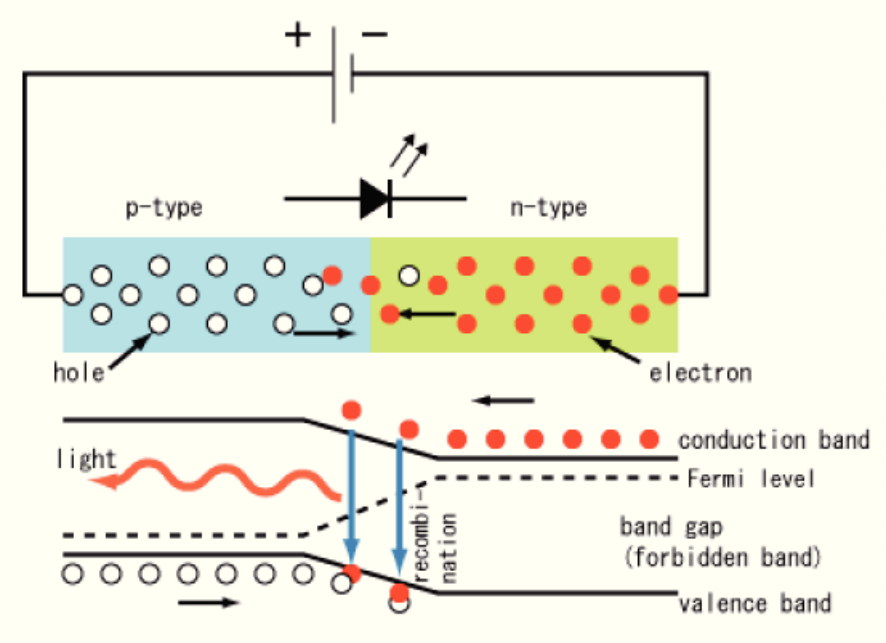

Figure 2.1: LED with *pn* homojunction under forward bias and its relative band diagram.

from laser diodes, where emitted light is coherent. This is the main difference between LED and laser operation.

In this chapter we will briefly review the basic concepts underlying the operation of LEDs. Initially we will deal with the recombination theory on semiconductors, analyzing both radiative and non-radiative recombination processes. After this, we will analyze the main LED structures, including homojunction, heterojunction, and quantum wells structure. Finally, we will conclude recalling the main electrical (current-voltage and capacitance-voltage characteristic) and optical properties (emission spectrum, optical efficiency and optical power-current characteristic). It is important to point out that the aim of this chapter is not to provide a complete treatment of light emitting diodes, but only the fundamental concepts necessary for the understanding of the experimental results presented in the subsequent chapters. Thus, it is assumed that the reader is already familiar with LEDs theory.

2.1 Recombination theory

In a semiconductor both *generation* and *recombination* processes can occur. In the first case, an electron is excited from the valence band to the conduction band, thus generating an electron-hole pair. The energy necessary for the excitation of electron from the valence to the conduction band can be provided by the absorption of a phonon or a photon with an energy at least equal to the energy gap of the semiconductor material. On the other hand, in a recombination process, an electron

initially present in the conduction band, recombines with an hole in the valence band, thus annihilating an electron-hole pair. In order to maintain the energy conservation, a phonon or photon with an energy approximately equal to the energy gap of material is emitted during process. The recombination process with emission of a photon is known as *radiative recombination*, while the recombination process with emission of a phonon is also called *non-radiative recombination*. In particular, the emission of phonons, which correspond to lattice vibrations, induce a heating of the material. A schematic illustration of radiative and non-radiative recombination processes occurring in a crystal is provided in Figure 2.2.

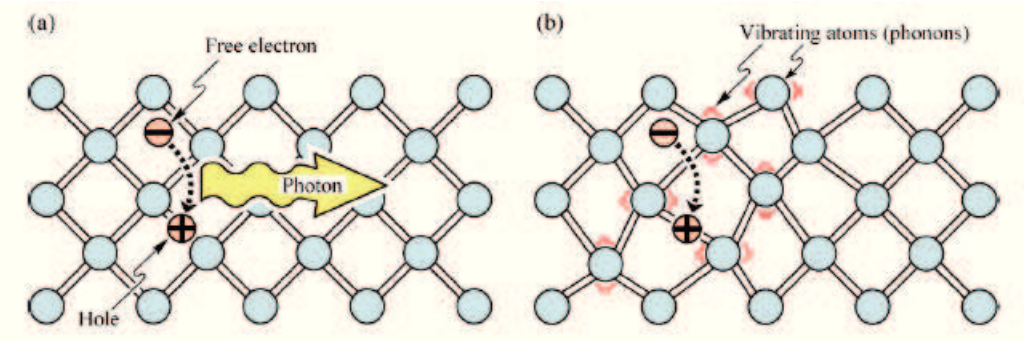

Figure 2.2: (a) Radiative recombination process with emission of a photon. (b) Non-radiative recombination process with emission of a phonon.

In this section the radiative and non-radiative recombination theory will be discussed separately: mathematical relationships will be also provided, in order to determine the lifetimes related to these processes. Finally, will be defined the internal quantum efficiency as a function of radiative and non-radiative lifetime.

2.1.1 Radiative recombination

Under thermal equilibrium condition, the electron and hole concentrations of both intrinsic and doped semiconductors, are related to each other by the law of mass action, i.e. $p_0 n_0 = n_i^2$, where p_0 and n_0 are the hole and electron concentration under equilibrium, respectively, and n_i represent the intrinsic carrier concentration, which depends on the temperature T of the semiconductor. Moreover, steady-state equilibrium condition, the generation rate G is equal to the recombination rate R, i.e. $R = G$.

Suppose that excess carriers are generated in the semiconductor material. Excess carriers can be generated either by absorption of light, and thus photons, or by an injection current. In this case, the semiconductor is no longer under thermal equilibrium conditions and also the law of mass action is no longer valid. The total carrier concentration both for electrons and holes can be expressed as follow:

$$n = n_0 + \Delta n \tag{2.3}$$

$$p = p_0 + \Delta p \tag{2.4}$$

where Δn and Δp are the excess carrier concentrations generated inside the semiconductor. Therefore, we can observe that the total carrier concentration can be expressed as the sum of equilibrium and excess carrier concentration. Suppose that at a certain instant t the generation process is interrupted: as a consequence, the initial thermal equilibrium condition in the semiconductor will be recovered by recombination of electron-hole pairs. Consider the recombination rate R, that represents the rate at which the carrier concentration decreases (R is usually measured in units of $cm^{-3}s^{-1}$): it will be proportional both to the available electrons in the conduction band and to the available holes in the valence band, i.e. it is proportional to the product of electron and hole concentrations. Therefore, the recombination rate R can be expressed by the following equation:

$$R = -\frac{dn}{dt} = -\frac{dp}{dt} = Bnp \tag{2.5}$$

where B is called the *bimolecular recombination coefficient* and the equation is known as the *bimolecular rate equation*. The coefficient B, expressed in units of cm^3s^{-1}, has typical values of $10^{-11} - 10^{-9}\, cm^3/s$ for direct-bandgap III-V semiconductors [34].

Now we are interested to analyze the recombination dynamics as a function of time, in a semiconductor submitted to photoexcitation. First, note that $\Delta n = \Delta p$, where Δn and Δp represent the steady-state excess carrier concentration, because electrons and holes are generated and annihilated in pairs. Using equations (2.3) and (2.4) in (2.5) it is obtained the following relation for the recombination rate:

$$R = B[n_0 + \Delta n(t)][p_0 + \Delta p(t)] = B[n_0 p_0 + \Delta n(t)(n_0 + p_0 + \Delta n(t))] \tag{2.6}$$

At this point we consider separately two different cases: low-level excitation and high-level excitation. In the case of ***low-level excitation***, the photogenerated carrier concentration is much smaller that the majority carrier concentration, i.e. $(\Delta n, \Delta p) \ll (n_0 + p_0)$. Using this condition, and the fact that $\Delta n = \Delta p$, as stated above, the equation (2.6) can be simplified as:

$$\begin{aligned} R &= Bn_i^2 + B(n_0 + p_0)\Delta n(t) \\ &= R_0 + R_{excess} \end{aligned} \tag{2.7}$$

Thus the recombination rate can be expressed as sum of the *equilibrium recombination rate* R_0 and the *excess recombination rate* R_{excess}.
The time dependence of the excess carrier concentration can be calculated from the following equation:

$$\frac{dn(t)}{dt} = G - R = (G_0 + G_{excess}) - (R_0 + R_{excess}) \tag{2.8}$$

Suppose that at the time $t = 0$ the photogeneration is interrupted, that correspond to the condition $G_{excess} = 0$. Furthermore, considering that the steady-state recombination and generation rates are equal, i.e. $R_0 = G_0$, the equation (2.8) can be simplified inserting relation (2.7), obtaining the differential equation:

$$\frac{d}{dt}\Delta n(t) = -B(n_0 + p_0)\Delta n(t) \tag{2.9}$$

which yields the following solution:

$$\Delta n(t) = \Delta n_0 e^{-\frac{t}{\tau}} \tag{2.10}$$

where $\Delta n_0 = \Delta n(t = 0)$. Thus an exponential dependence from the time is obtained for the excess carrier concentration. In particular, the carrier concentration decays exponentially with a characteristic time constant τ, that can be expressed as:

$$\tau = \frac{1}{B(n_0 + p_0)} \tag{2.11}$$

In the next section it will be shown that this time constant τ, also called the ***carrier lifetime***, strongly influences the internal quantum efficiency of semiconductor. The Figure 2.3 summarizes the time dependence of carrier concentrations under low-level excitation, occurring in a p-type semiconductor. The figure in particular shows that the excess carrier concentration is much smaller than the majority carrier concentration, but on the other hand it is much larger than the minority carrier concentration. Since $p_0 \gg n_0$ in a p-type semiconductor, in this case the carrier lifetime can be semplified with the relation $\tau = 1/(Bp_0) = 1/(BN_A)$, where N_A is the acceptor concentration. Similar considerations apply in the case of a n-type semiconductor.

On the other hand, in the condition of ***high-level excitation*** the excess carrier concentration is much larger than the equilibrium carrier concentration, i.e. $(\Delta n, \Delta p) \gg (n_0 + p_0)$. In this case the bimolecular rate equation (2.5) can be simplified as follow:

$$\frac{d}{dt}\Delta n(t) = -B\Delta n^2(t) \tag{2.12}$$

This differential equation yields the solution:

$$\Delta n(t) = \frac{1}{Bt + \frac{1}{\Delta n_0}} \tag{2.13}$$

where $\Delta n_0 = \Delta n(t = 0)$. Note that, differently from the low-level excitation case, this solution represent a non-exponential decay. If we define the time constant as the slope of the decay, we find the following time constant for the case of high-level excitation (thus, we can define a time constant even if it is a non-exponential decay):

$$\tau(t) = t + \frac{1}{B\Delta n_0} \tag{2.14}$$

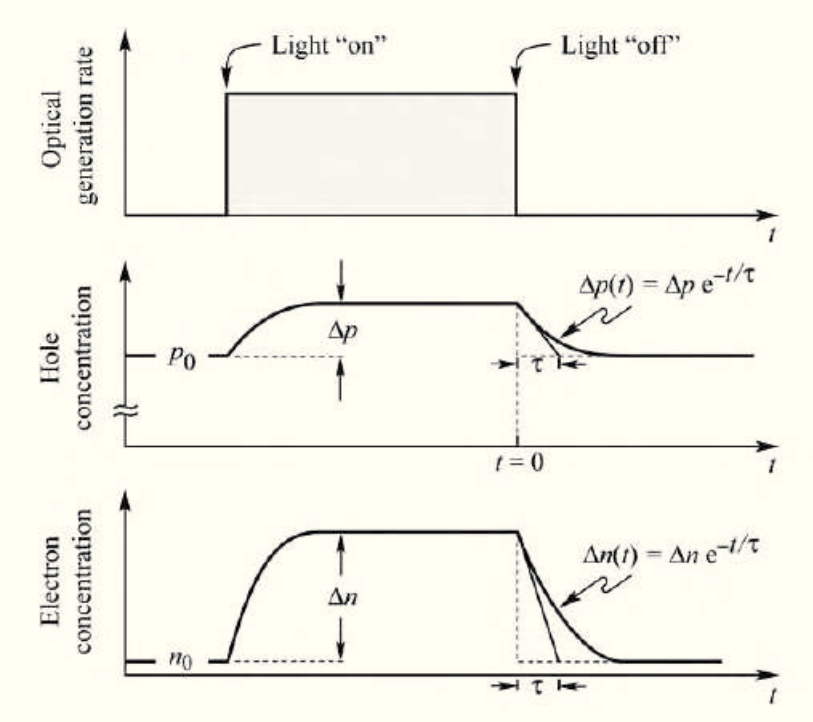

Figure 2.3: Electron and hole concentration as a function of time in a p-type semiconductor before, during and after an optical excitation process. The hypothesis of low-level excitation is assumed.

Note that the carrier lifetime τ depends on time, in contrast to the low-level excitation case, where it is time indipendent, as shown in the equation (2.11). In particular, the carrier lifetime for this case increases with time and for sufficiently long times, τ will approach the low-level excitation value. However, if a great excess carrier concentration is continuously generated, the carrier lifetime will remain constant and equal to the initial value $1/B\Delta n_0$, obtained for $t = 0$.

In this section we have referred to an electrically insulated semiconductor submitted to illumination. However, the same results both for low-level and high-level excitation can be applied to LEDs, where carriers in excess are injected in the active region of a pn junction under forward bias. Finally, it is also possible to determine an expression for the bimolecular recombination coefficient B by means of the Van Roosbroeck-Schockley model [34].

2.1.2 Non-radiative recombination

Non-radiative recombination results in the emission of phonons, which are lattice vibrations, thus inducing a heating of the semiconductor. Non-radiative recombination is obviously unwanted in optoelectronic devices and, in order to limit its contribution, it is important to deeply understand the physical mechanisms by which non-radiative recombination can occur. In this section three different types

of non radiative recombination will be discussed:

- recombination of free carriers via deep levels, also called Shockley-Hall-Read (SHR) recombination;
- surface recombination;
- Auger recombination.

The Shockley-Hall-Read and surface recombination are indirect recombination processes, which means that the recombination occurs via a deep level localized inside the bandgap of the material. On the other hand, Auger recombination is a direct recombination process, which involves three charged particles (two electrons and a hole, or two holes and an electron). In Figure 2.4 is reported a schematic illustration of a non-radiative recombination process via deep level, an Auger recombination and a radiative recombination process, respectively.

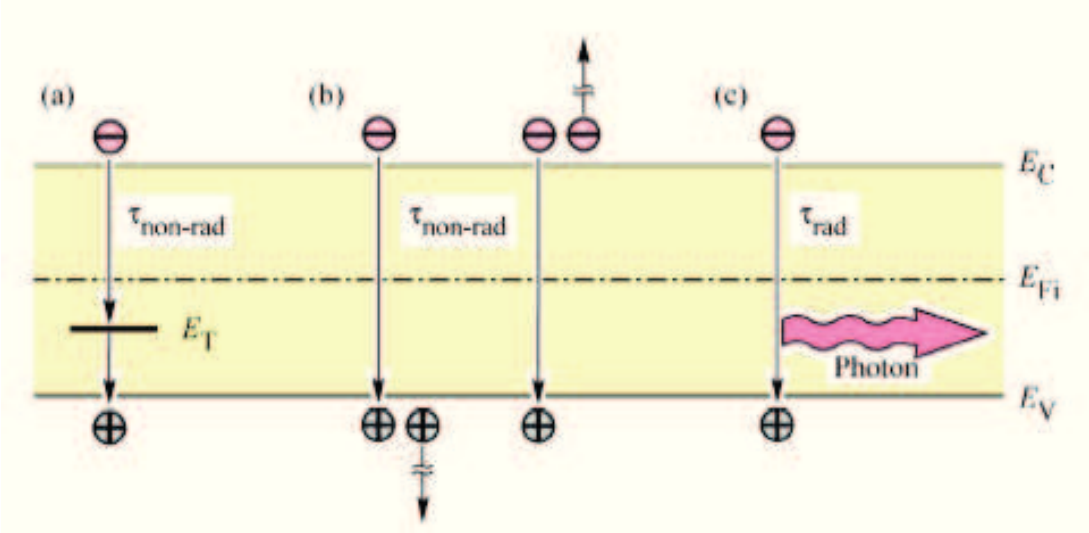

Figure 2.4: Band diagram of a generic semiconductor material, showing (a) non-radiative recombination process via deep level, (b) non-radiative Auger recombination and (c) a radiative recombination process.

Shockley-Hall-Read recombination

In section 1.7 we have seen that several defects can be present in a crystal structure: these defects include unwanted foreign atoms, native defects, dislocations, and any complexes of defects, foreign atoms, or dislocations. In compound semiconductors, such as gallium nitride, native defects include interstitials, vacancies, and antisite defects. Also the physical characteristics of these defects have been discussed in the previous chapter. Defects in a crystal structure are the most common cause for non-radiative recombination [34]. In fact, all such defects usually form one or

more energy levels within the forbidden gap of the semiconductor. Due to their position inside the energy gap, they are also called deep levels. Deep levels inside the bandgap act as efficient recombination centers, in particular if the energy level is close to the middle of the gap.

The recombination via deep levels is usually a non-radiative recombination process. However, radiative transitions via deep levels have been observed in some semiconductors materials. An example is represented by radiative recombination mediated by a deep level in n-doped GaP [34]. Another well-known example of radiative recombination assisted by the presence of defects is the radiative deep-level transition occurring in GaN and shown in Figure 2.5 [71]. Two different luminescence peaks can be observed in the figure: that one associated to the band-to-band transition at 365 nm, and a broad deep-level transition with emission centered near the yellow spectral range, at around 550 nm. It has been demonstrated that the yellow luminescence is due to Ga vacancies, a common point defect in n-type GaN. [72] [73] [74].

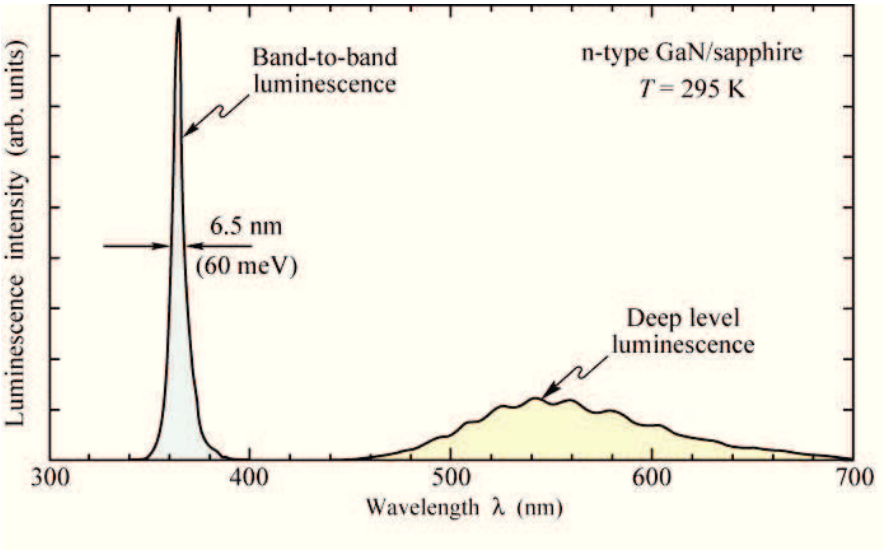

Figure 2.5: Photoluminescence spectrum of GaN, showing a band-to-band transition at 365 nm and an optically actived deep-level transition occurring at 550 nm. This measurements were performed at room temperature.

Four basic transitions are underlying to the non-radiative recombination via deep levels, which are also illustrated in Figure 2.6: electron capture or emission, and hole capture or emission. In the figure we suppose that the deep level is localized within the bandgap, at an energy level E_t.

The recombination of free carriers via deep levels was first analyzed by Shockley, Read, and Hall and for this reason it is also known as Shockley-Hall-Read (SHR) recombination. Generally, the non-radiative recombination rate through a deep

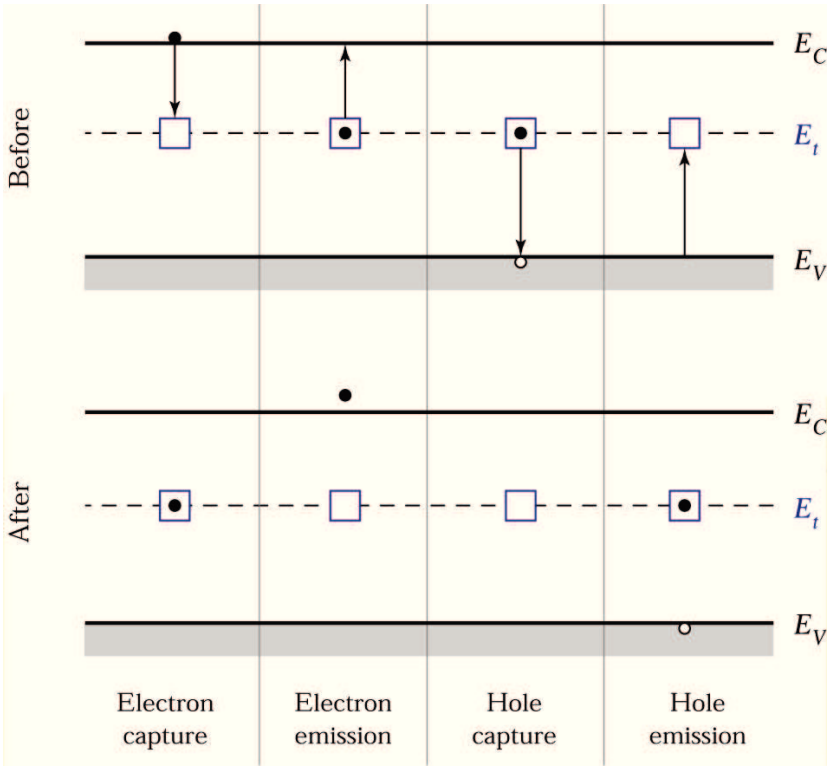

Figure 2.6: Capture and emission of carriers from a deep level localized inside the bandgap and localized at an energy level E_t.

level in a semiconductor at a temperature T can be expressed as:

$$R_{SHR} = \frac{v_{th}\sigma_n\sigma_p N_t(pn - n_i^2)}{\sigma_p[p + n_i e^{-\frac{E_t - E_i}{kT}}] + \sigma_n[n + n_i e^{\frac{E_t - E_i}{kT}}]} \tag{2.15}$$

where v_{th} is the thermal velocity of carriers, N_t is the trap level concentration, E_i represent the intrinsic Fermi level, E_t is the trap energy, n_i is the intrinsic carrier concentration, and σ_n and σ_p represent the electron and hole capture cross sections of the traps, respectively.
If electron and hole capture cross sections are identical, i.e. $\sigma_n = \sigma_p = \sigma_0$, the equation (2.15) can be simplified as follow:

$$R_{SHR} = v_{th}\sigma_0 N_t \frac{np - n_i^2}{p + n + 2n_i cosh(\frac{E_t - E_i}{kT})} \tag{2.16}$$

Inspection of equation (2.16) reveals two interesting results: first, the recombination rate is maximum when $E_t = E_i$, due to the fact that the hyperbolic cosine function is minimum at zero. This means that deep levels localized in the middle of the energy gap, i.e. with trap energy $E_t = E_i$, act as efficient recombination centers. Second, the recombination rate R_{SHR} enhances with increasing of the temperature. Thus, at high temperature operation non radiative-recombination is favored over radiative recombination.

In a n-type semiconductor ($n \gg p$) with low-level injection level, i.e. with $n \approx n_0$, the equation (2.16) can be simplified in the form:

$$R_{SHR} = v_{th}\sigma_p N_t(p - p_0) = \frac{p - p_0}{\tau_p} \tag{2.17}$$

where it has been defined the minority carrier lifetime (holes in this case) as:

$$\tau_p = \frac{1}{v_{th}\sigma_p N_t} \tag{2.18}$$

On the other hand, in the case of p-type semiconductor the recombination rate is:

$$R_{SHR} = v_{th}\sigma_n N_t(n - n_0) = \frac{n - n_0}{\tau_n} \tag{2.19}$$

with the following minority carrier lifetime (electrons in this case):

$$\tau_n = \frac{1}{v_{th}\sigma_n N_t} \tag{2.20}$$

Thus, under low-injection conditions, the non-radiative recombination rate R_{SHR} is proportional to the excess minority carrier concentration (electrons in a p-type semiconductor and holes in a n-type semiconductor) and to the inverse of their lifetime. For more details about the Shockley-Hall-Read recombination, see [75].

Surface recombination

Surfaces of a semiconductor material are a strong perturbation of the periodicity of the crystal lattice: due to this fact, substantial non-radiative recombination can occur at semiconductor surfaces. In fact, the presence of dangling bonds at the surfaces, as shown in Figure 2.7, introduce electronic states within the forbidden gap of the semiconductor, that act as non-radiative recombination centers. As a consequence, at surfaces a strong reduction of radiative efficiency is observed. Moreover, the increased non-radiative recombination at surfaces can induce a heating of semiconductor material in the surface area.

The recombination dynamics at surfaces is similar to Shockley-Hall-Read recombination, and thus the recombination rate at surfaces can be expressed in a similar form to that of equation (2.15) [76]. Assuming that the carrier concentration at surfaces is approximately equal to that in bulk material, the surface recombination rate $R_{surface}$ in a n-type semiconductor, where the low-injection condition is assumed, can be expressed with the following approximate equation:

$$R_{surface} = v_{th}\sigma_p N_{st}(p_s - p_0) \tag{2.21}$$

where $p_s - p_0$ represent the excess minority carrier concentration (holes in this case) in proximity of the surface, σ_p is the capture cross section and N_{st} is the

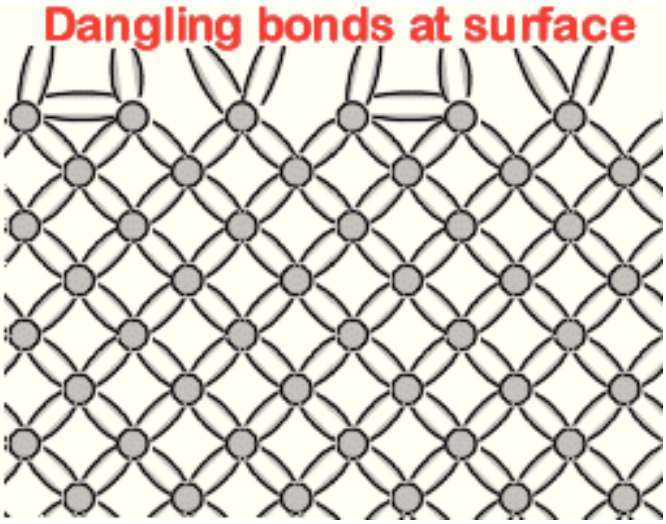

Figure 2.7: Dangling bond at the surface of a crystal structure.

surface density of recombination centers. Note that $R_{surface}$ is expressed in units of $cm^{-2}s^{-1}$, while R_{SHR} is expressed in units of $cm^{-3}s^{-1}$.

The dangling bonds may also rearrange themselves and form bonds between neighboring atoms in the same surface plane. They can also form bonds with foreign atoms present in the surrounding atmosphere. For this reasons, it is not easy to determine *a priori* the position of trap levels within the forbidden gap. In order to limit the non-radiative recombination of LEDs, it is important that the active region is far from surfaces: different solutions have been proposed in recent years, including passivation techniques to reduce the concentration of surface non-radiative recombination centers [75].

Auger recombination

Another important non-radiative recombination mechanism it the ***Auger recombination***. In this process, the energy becoming available through electron-hole recombination is dissipated by the excitation of a free electron high into the conduction band, or by a hole deeply excited into the valence band. The highly excited carriers will subsequently lose energy by multiple phonon emission until they are close to the band edge [34]. Note that, differently from Shockley-Hall-Read and surface recombination, this is a direct recombination process, because it does not need the presence of a deep level to occur. A schematic illustration of Auger recombination is provided in Figure 2.4 (b) and in more detail in Figure 2.8.

The Auger recombination rate can be expressed by two way, depending on the fact if the recombination energy is dissipated by the excitation of a electron or by the excitation of a hole. In the first case the Auger recombination rate is given by

$$R_{Auger} = C_n n^2 p \tag{2.22}$$

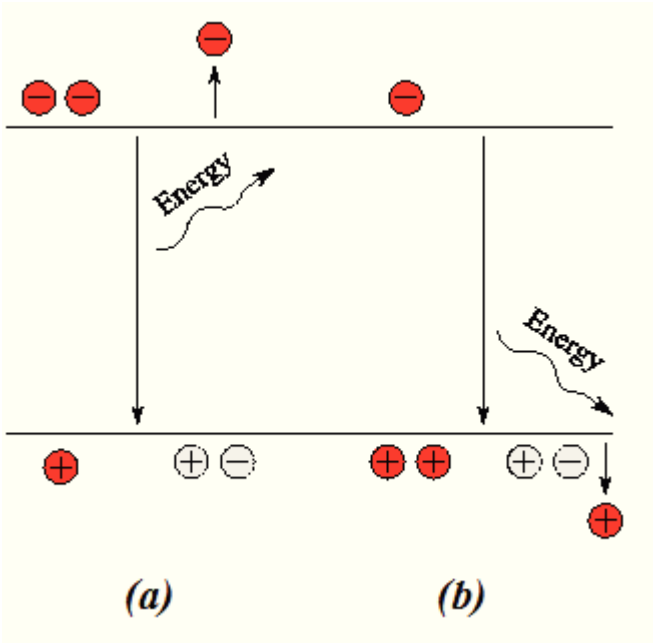

Figure 2.8: Auger recombination with the energy of recombination process dissipated (a) by the excitation of a free electron and (b) by the excitation of a hole.

while in the second case is given by:

$$R_{Auger} = C_p n p^2 \tag{2.23}$$

Note that the Auger recombination rate is proportional to the square of the carrier concentration (either p^2 or n^2), since two carriers of the same type are required for the recombination process. In the high-excitation limit, in which the non-equilibrium carriers have a higher concentration than equilibrium carriers, the Auger recombination rate reduces to:

$$R_{auger} = (C_p + C_n)n^3 = Cn^3 \tag{2.24}$$

where C is the ***Auger coefficient*** and it takes typical values of $10^{-28} - 10^{-29}\, cm^6/s$ for III-V semiconductors [77] [78].

Due to the cubic carrier concentration dependence expressed in the equation (2.24), the contribution of Auger recombination is relevant only at very high injection levels. Thus at lower carrier concentrations, the Auger recombination rate is very small and can be neglected for practical purposes.

2.1.3 Internal quantum efficiency

As we have already seen, in optoelectronic devices the non-radiative recombination processes are unwanted. In order to obtain high efficient devices it is important to limit the non-radiative recombination. However, even though non-radiative recombination can be reduced, it can never be totally eliminated. For example, the

Shockley-Hall-Read recombination cannot be reduced to zero, because even though the defect concentration can be drastically reduced by growth of high quality crystals, it is never zero. Also surface recombination can be reduced by separating the active region from any surfaces. However, even if the separation is large, a few carriers will still diffuse to the surface and recombine there. Finally, it has to be considered that the contribution of Auger recombination can never be totally avoided at high injection levels, also because it does not depends on the presence of defects.

The total probability of recombination can be expressed as a combination of radiative and non-radiative lifetime by the following relation:

$$\frac{1}{\tau} = \frac{1}{\tau_r} + \frac{1}{\tau_{nr}} \tag{2.25}$$

where τ_r is the radiative lifetime and τ_{nr} is the non-radiative lifetime.
In particular, the total non-radiative lifetime is related to the lifetime of the three non-radiative processes analyzed in this section, i.e. Shockley-Hall-Read, surface and Auger recombination:

$$\frac{1}{\tau_{nr}} = \frac{1}{\tau_{SHR}} + \frac{1}{\tau_{surface}} + \frac{1}{\tau_{Auger}} \tag{2.26}$$

At this point we can define the probability of radiative recombination, also called ***internal quantum efficiency*** η_{int}: it is given by the radiative probability over the total probability of recombination and it can be expressed as a function of radiative and non-radiative lifetimes as follow:

$$\eta_{int} = \frac{\tau_r^{-1}}{\tau_r^{-1} + \tau_{nr}^{-1}} \tag{2.27}$$

The internal quantum efficiency gives the ratio of the number of light quanta emitted inside the semiconductor to the number of charge quanta undergoing recombination. From the relation (2.27) it is clear that, in order to maximize the internal quantum efficiency of an optoelectronic device, it is necessary to increase the non-radiative lifetime and reduce the radiative lifetime.

In order to obtain optoelectronic devices with high internal efficiency, it is also important to employ direct band-gap semiconductor materials. To better understand this fact, in the remainder of this section the difference between direct and indirect bandgap semiconductor will be discussed.

It is well known that the energy-momentum $E-p$ diagram, or analogously the $E-k$ diagram, is parabolic for a free electron or hole. However, the $E-k$ diagram of a semiconductor material is much more complex and it is also dependent on the crystalline orientation. Moreover, electrons are localized near the minimum of conduction band, while holes are near the maximum of valence band: thus

recombination transitions usually occur between these two points in the $E-k$ diagram. If the minimal-energy state in the conduction band and the maximal-energy state in the valence band have the same crystal momentum, i.e. if the momentum of electrons and holes is the same in both the conduction band and the valence band, the material is called a *direct bandgap* semiconductor; otherwise it is an *indirect bandgap semiconductor*.

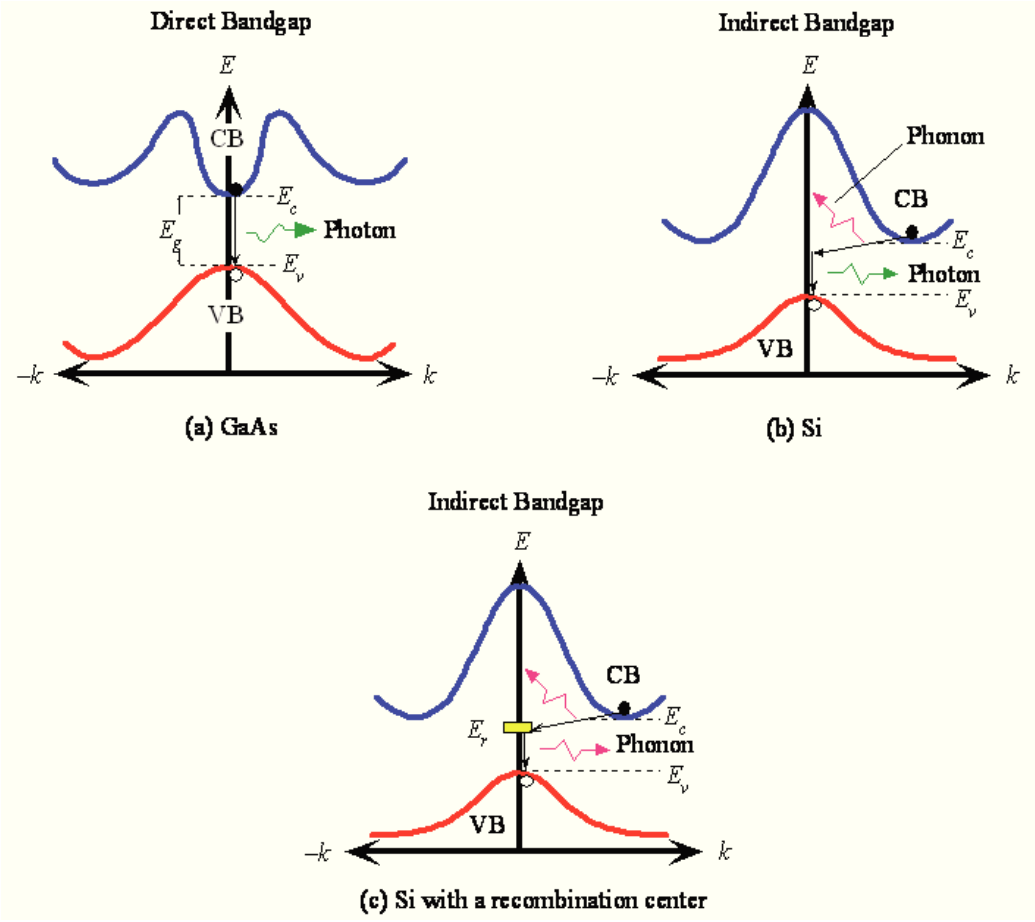

Figure 2.9: (a) Direct radiative recombination process occurring in GaAs, which is a direct bandgap semiconductor. (b) Indirect radiative recombination process occurring in silicon, which is an indirect bandgap semiconductor. (c) Non-radiative recombination process via deep-level occurring in silicon.

In ***direct bandgap*** semiconductors the recombination process with emission of a photon is a direct process that requires no assistance from lattice vibrations. The electron recombines with a hole, resulting in the emission of a photon, without a change in its k-vector inasmuch as the photon momentum is very small. This process correspond to a vertical transition on the $E-k$ diagram, as shown in Figure 2.9 (a) for the case of GaAs. Due to the fact that the minimum of conduction band and the maximum of valence band have the same k-vector, the probability of radiative recombination process is very high in a direct bandgap semiconductor

and for this reason they are preferred for the fabrication of optoelectronic devices, such as LEDs, lasers and photodetectors. Typical direct bandgap semiconductors are most of III-V compound semiconductors, such as gallium nitride (GaN) and gallium arsenide (GaAs), and its ternary and quaternary alloys, and II-VI binary compounds.

On the other hand, in ***indirect bandgap*** semiconductors the recombination process with emission of photons requires the simultaneous emission of lattice vibrations, i.e. phonons. When an electron in the conduction band recombines with a hole in the valence band, there is a change in its momentum in the crystal and this change in the momentum cannot be supplied by the momentum of the emitted photon, which is very small. Thus, the change in the electron momentum, required for the momentum conservation, must be provided by the emission of a phonon, as represented in Figure 2.9 (b) for the case of silicon. Since this radiative recombination process needs a third body, a lattice vibration, the probability of photon emission is not as high as in a direct bandgap semiconductor. For this reason, the probability of non-radiative recombination via deep levels, with phonon emission, is higher in indirect bandgap semiconductors, as shown for the case of silicon in Figure2.9 (c). Thus, it is clear that indirect bandgap semiconductors are not suitable for the realization of optoelectronic devices.

2.2 Typical LED structures

At the beginning of this chapter we have referred to a LED based on a *pn* homojunction structure. However, this is not the optimal solution, because the carrier concentration near the junction strongly depends on electron and hole diffusion constants, thus limiting the recombination probability. In this section more efficient LED structures will be analyzed. In particular, the following structures will be analyzed in more details:

1. first, the homojunction structure will be analyzed in more details, in order to better understand the origin of low efficiency related to this structure;
2. second, heterojunction structure will be presented, with particular focus to double heterostructure;
3. finally, quantum wells structures will be analyzed, showing the several advantages related to them.

2.2.1 Homojunction LEDs

The homojunction LED is the simplest LED structure, consisting of a *pn* junction realized with a single material. In such a structure, the carrier distribution de-

pends on the *diffusion constant* of the carriers. Under forward bias, electrons will diffuse from the n-side to the p-side, while holes will diffuse from the p-side to the n-side and eventually will recombine with majority carriers. The mean distance that a minority carrier diffuses before recombination is the *diffusion length*, which is equal to $L_n = \sqrt{D_n \tau_n}$ and $L_p = \sqrt{D_p \tau_p}$ for electrons and holes, respectively. We can see that the carrier distribution along the junction is proportional to the diffusion constant, and thus to the carrier mobility, and to their lifetime. In typical semiconductors, the diffusion length is in the order of a several micrometers. For example, the diffusion length of electrons in p-type GaAs is equal to $L_n \approx 15\mu m$, and thus the minority carriers are distributed over a region several micrometers thick [34]. Figure 2.10 shows the carrier distribution in a pn homojunction under zero bias and under forward bias, respectively. Note that minority carriers are distributed over a quite large distance under forward bias condition. Thus recombination occurs over a large region, with a strongly changing of minority carrier concentration.

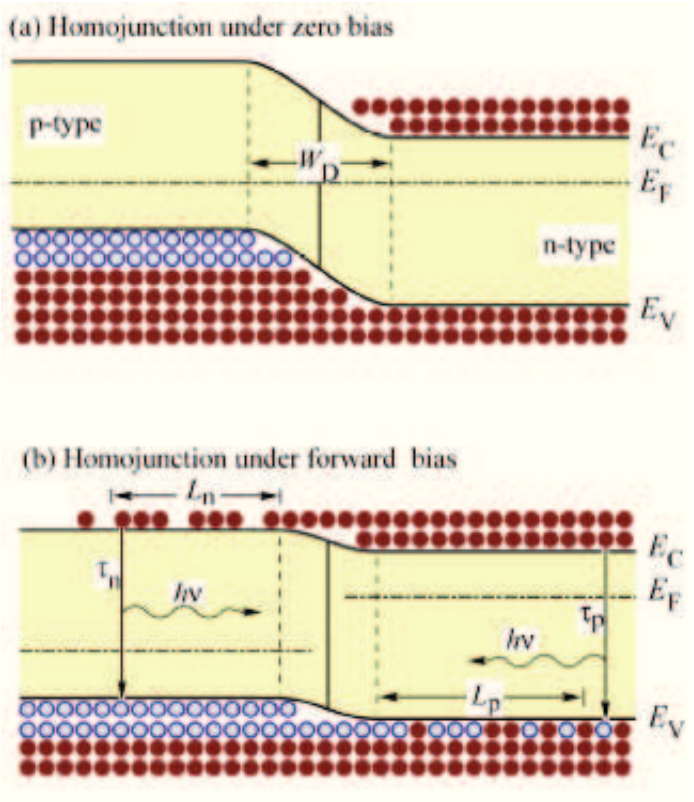

Figure 2.10: Carrier distribution in a pn homojunction under (a) zero bias and (b) forward bias.

The large recombination region in homojunctions is not beneficial for efficient recombination. This is due to the fact that the radiative recombination rate $R = Bnp$ is proportional both to electron and hole concentration and, as we have seen

above, these concentrations are quite low in this structure. For this reason, *pn* homojunction structure is not usually employed for the realization of LEDs.

2.2.2 Heterojunction LEDs

All high-intensity light-emitting diodes do not use the homojunction design but rather employ heterojunction structures, which have clear advantages over homojunction devices. Heterojunction devices employ two types of semiconductors, with different energy gap and other physical properties, such as the dielectric permettivity. As in homojunction LEDs, also in heterojunction LEDs materials with different conductivity (i.e. both n-type and p-type doped materials) are usually employed, even if interesting results can be obtained also employing materials with different energy gap and the same type of doping.

When a *pn* heterojunction is formed, electrons diffuse from the n-side to the p-side and holes diffuse from the p-side to the n-side, as in a *pn* homojunctions. However, as a consequence of the different energy gap and electronic affinity between different materials, the carrier diffusion creates discontinuities both in the conduction band (ΔE_c) and in the valence band (ΔE_v), as shown in Figure 2.11 for a generic heterojunction between two different semiconductors. In particular, from the Anderson's theory results $\Delta E_c = q(\chi_1 - \chi_2)$ and $\Delta E_v = \Delta E_g - \Delta E_c$.

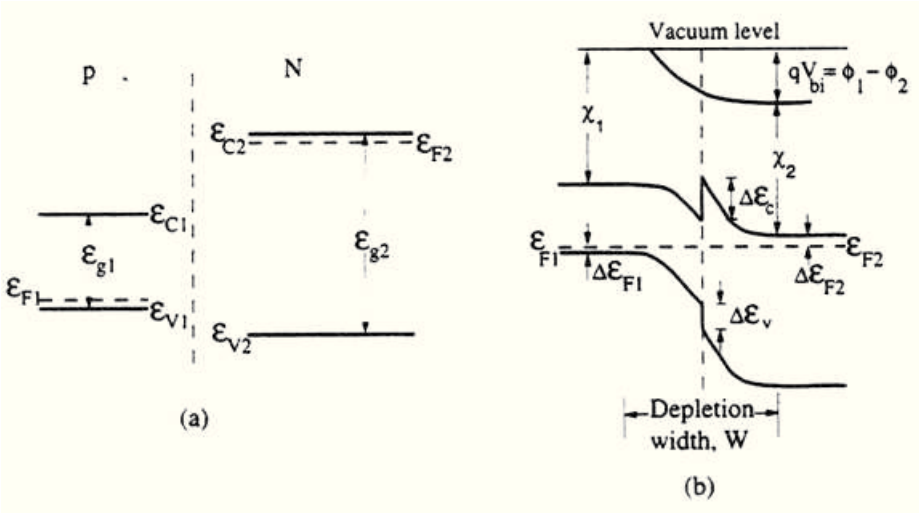

Figure 2.11: Band diagram (a) before and (b) after the formation of a heterojunction between two semiconductors with different energy gap. the band diagram on the right-hand is referred to the equilibrium condition under zero bias.

In order to understand how heterostructures can influence the carrier distribution in the proximity of junction, we consider the heterojunction of Figure 2.11 (b) when a forward bias is applied. An increase in the forward voltage reduces the electron barrier: the results of applied bias is shown in Figure 2.12: as it can be

noticed, the discontinuity ΔE_c in the conduction band does not slow the electron flow. On the other hand, even if also the barrier to hole flow is reduced, the discontinuity ΔE_v in the valence band does not change with increasing the forward voltage, thus strongly slowing the hole flow towards the n-side. As a result, a hole confinement was obtained in such a structure, thus increasing its concentration in proximity of the junction. As a consequence, the radiative recombination probability results increased with respect to the homojunction structure. However, from Figure 2.12 it is clear that it is not possible to obtain simultaneous confinement of both electron and holes in the same region. for this reason, even if a single heterojunction results in an improved radiative efficiency, it is not the best solution to obtain LEDs with high efficiencies.

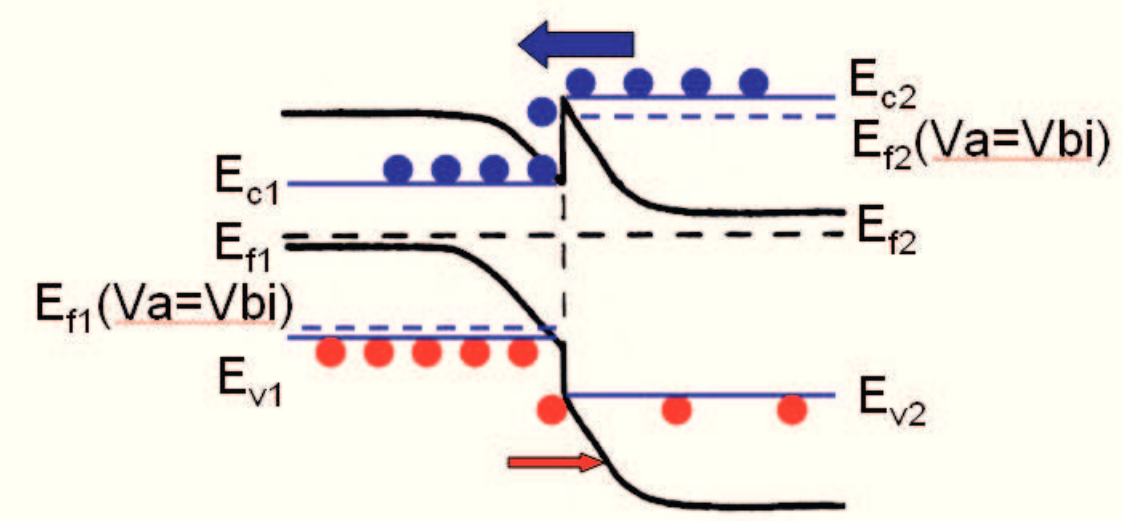

Figure 2.12: Carrier distribution in a *pn* heterojunction under forward bias condition.

A better solution that permits to obtain very high internal quantum efficiency is the double heterostructure (DH). It consists of two barriers, which are obtained interposing a small bandgap semiconductor, usually indicated as the active region, between two semiconductor layers having a greater energy gap with respect to the active region. The effect of heterojunctions on the carrier distribution is shown in Figure 2.13: as it can be noticed, carriers injected in the active region of the double heterostructure are confined to this zone by means of the barriers. As a result, the thickness of the region in which carriers recombine is given by the thickness of the active region, than rather the diffusion length. If the active region thickness is appropriately chosen, the radiative recombination rate can be strongly increased with respect to the homojunction structure, because the carriers in the active region of a double heterostructure have a much higher concentration than carriers in homojunctions. For example, the diffusion length of carriers may range

from 1 to 20 μm. On the other hand, the active region of a double heterostrucutre may range from 0.01 to 1 μm.

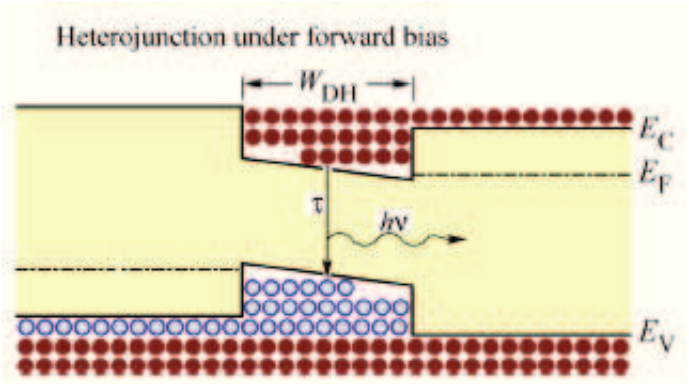

Figure 2.13: Carrier distribution in a double heterostructure (DH) under forward bias.

Double heterostructures can also be used to confine light to waveguide regions: this can be obtained thanks to the difference between the refractive index of active region and barrier layers. In particular, optical confinement is used for the realization of *edge-emitting* LEDs [34]. Moreover, due to the smaller energy gap of the active region with respect to the barrier layers, emitted photons from the active region will not be reabsorbed by barriers, thus further increasing the optical efficiency of devices.

However, hererostructures are characterized by also some drawbacks, that can limit the optical efficiency of devices, including:

- increased device resistance caused by the heterointerfaces;
- carrier loss in double heterostructures;
- carrier overflow in double heterostructures;
- lattice strain due to the lattice mismatch between different semiconductor materials.

In the following we will briefly analyze each of these drawbacks.

Resistance caused by heterointerfaces

One of the major drawbacks introduced by heterostructures is the resistance caused by heterointerfaces. In order to understand the origin of the resistance, we refer to Figure 2.14, which shows the band diagram of a heterostructure consisting of two semiconductors with different bandgap energy and it is assumed that both sides of the heterostructure are of n-type conductivity.

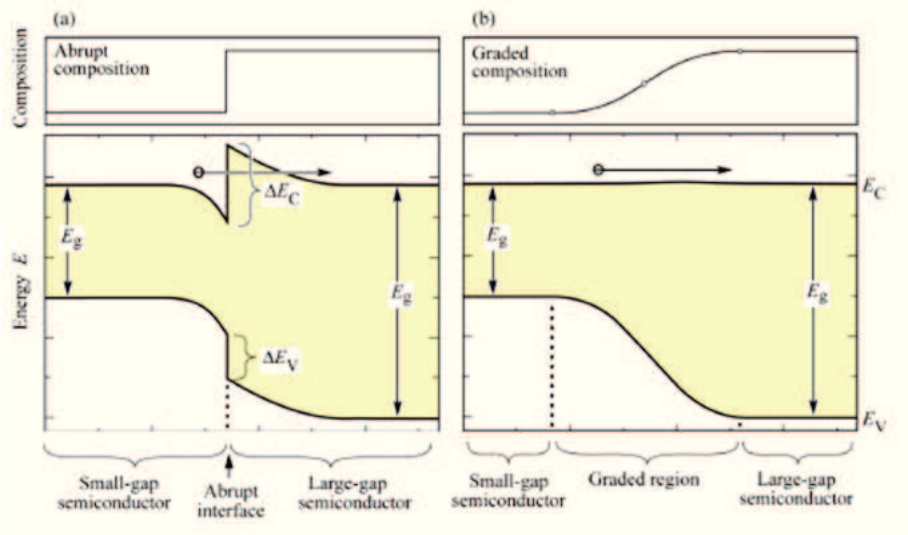

Figure 2.14: Band diagram of (a) an abrupt n-type-n-type heterojunction and (b) a graded heterojunction between two materials with different energy gap.

In such a structure, electrons in the large-bandgap material will diffuse over to the small-bandgap material. As a result, an electrostatic dipole forms, consisting of a positively charged depletion layer with ionized donors in the large-bandgap material, and a negatively charged electron accumulation layer in the small-bandgap material, thus inducing a band bending, as shown in Figure 2.14 (a). Note that a barrier to the electron flow is formed in the conduction band: thus, carriers transferring from one semiconductor to the other must overcome this barrier by either tunnelling or by thermal emission over the barrier. In any case, the barrier to electron flow constitutes a resistance at the heterointerface, which can have a strong deleterious effect on device performances. In fact, the thermal dissipation produced by this resistance leads to heating of the active region, thereby decreasing the radiative efficiency.

A possible solution to this problem is to eliminate heterostructure band discontinuities: this can be obtained by grading of the chemical composition of the semiconductor in the vicinity of the heterostructure, as shown in Figure 2.14 (b) [79]. In particular, it has been demonstrated that the resistance introduced by abrupt heterostructures can be completely eliminated by parabolic grading.

Carrier loss in double heterostructures

In this section we have seen that by means of carriers confinement in the active region of a double heterostructure, a high carrier concentration is attained, resulting in a high radiative efficiency. In an ideal structure all injected carriers are confined to the active region by the barrier layers.
The energy barriers at heterointerfaces, ΔE_c and ΔE_v, are typically of the order

of several hundreds of meV, i.e. much larger than kT. Free carriers in the active region are distributed according to the Fermi-Dirac distribution and, as a result, some carriers have a higher energy than the height of the confining barrier. Thus, some of the carriers will escape from the active region, as shown in Figure 2.15. This phenomenon will produce a leakage current and a reduction of the optical efficiency.

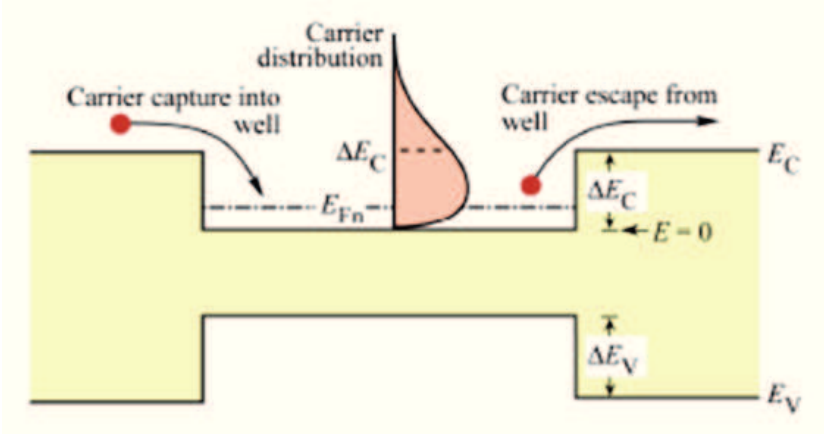

Figure 2.15: Carrier distribution in the active region of a double heterostructure, showing the carrier capture and escape.

The leakage current generated by carrier loss in double heterostructures depends on several factors, including the barrier heights ΔE_c and ΔE_v and the device temperature. Obviously, a reduction of barrier height induces an increase in the leakage current. Thus a high barrier height is required to minimize the leakage current. Also an increase of the temperature results in a increased leakage current, due to the higher thermal energy of carriers. In fact, the leakage current increases exponentially with temperature, thus strongly limiting the radiative efficiency. To reduce the temperature dependence of the emission, high barriers are required [34].

In order to reduce carrier leakage out of the active region, blocking layers are usually inserted. Such blocking layers are regions with a high bandgap energy located at confinement-active interface. In particular, the electron leakage current is larger than the hole leakage current, due to the usually larger diffusion constant of electrons compared to holes in III-V semiconductors. For this reason, *electron blocking layers* are used in many LED structures to reduce electron escape out of the active region.

An example of a InGaN-based LED structure with electron blocking layer is represented by the band diagram of Figure 2.16. The LED has a InGaN/GaN multi-quantum well active region [1] and AlGaN confinement layers. An AlGaN electron-blocking layer is included in the p-type confinement layer at the confine-

[1]This structure will be discussed in more detail in the next section

ment active interface. Figure 2.16 (a), which is referred to an undoped structure, shows that the AlGaN electron-blocking layer creates a barrier to current both for electrons as well as for holes. However, as shown in Figure 2.16 (b), in the doped structure the barrier in the valence band is screened by free carriers so that there is no barrier to the flow of holes in the p-type confinement layer. In particular, from the inset of Figure 2.16 (b) it can be observed that a potential spike and notch occur at the confinement-blocking layer interface. Hole must tunnel through the potential spike when propagating towards the active region. The valence band edge can be completely smoothed out by compositional grading at the confinement-blocking layer interface so that the electron blocking layer does not impede the hole flow at all [34].

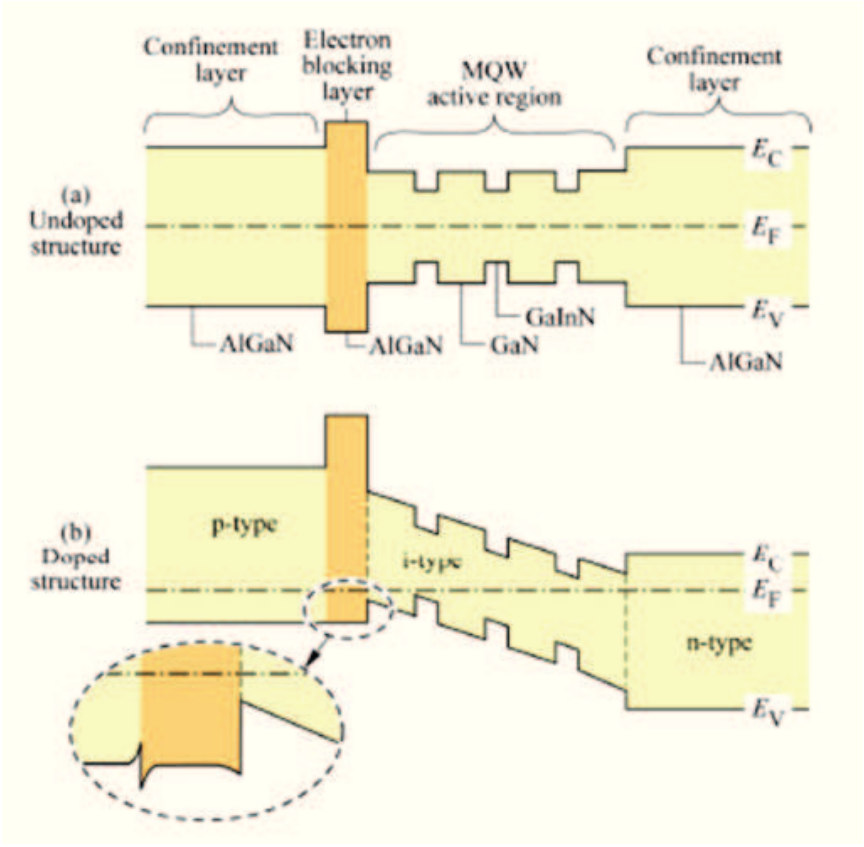

Figure 2.16: InGaN/GaN MQW LED structure with electron-blocking layer. (a) Band diagram without doping and (b) with doping.

Carrier overflow in double heterostructures

In a double heterostructure, as the injection current increases, the carrier concentration in the active region increases and consequently the Fermi level rises. For sufficiently high current densities, the Fermi energy will rise to the top of the barrier. At this point the active region is filled with carriers and a further increases

in the injection current will not result in a increase of the carrier concentration in the active region. This phenomenon is known as *carrier overflow*. As a result, the optical intensity saturates.

Generally, the problem of carrier overflow is more severe in structure with a small-active region volume. This, in turn strongly depends on the barrier heights ΔE_c and ΔE_v, and on the active region thickness. In order to limit this problem, heterostuctures with high barrier heights and high thickness need to be created. However, note that a high active region thickness can reduce the optical efficiency, due to the defects introduced by lattice strain at heterointerfaces. In fact, as the thickness of active region is increased, also the lattice strain increases. For this reason, multiple-quantum well (MQW) LED structures are usually preferred. As an example, in Figure 2.17 are shown the experimental results of an LED structure with one, four, six, and eight quantum wells [80]: as the number of quantum wells is increases, the current level at which saturation occurs increased, and the optical saturation intensity increases as well.

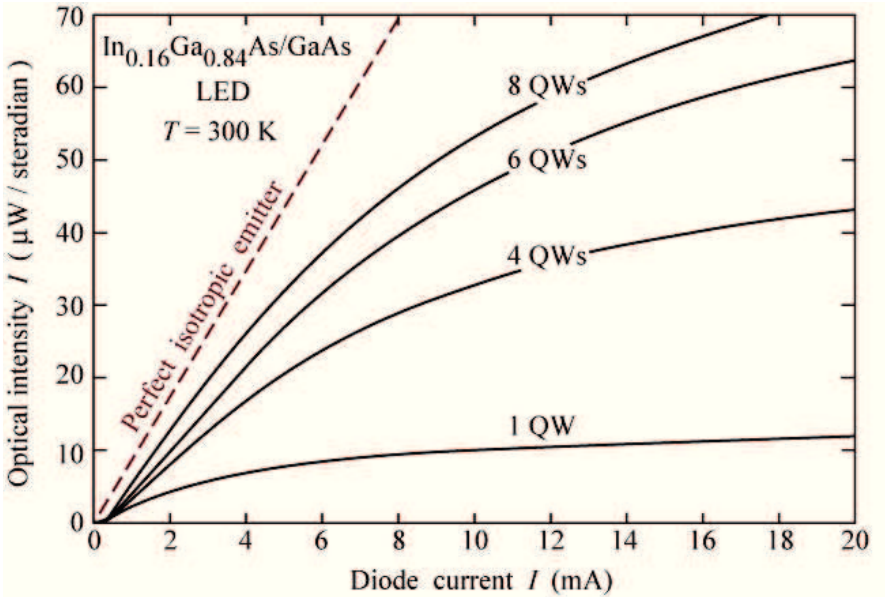

Figure 2.17: Optical intensity emitted by $In_{0.16}Ga_{0.84}As/GaAs$ LEDs with active region consisting of one, four, six and eight quantum wells, respectively [80]. Also the theoretical intensity of a perfect isotropic emitter is shown for comparison.

Lattice strain at heterointerfaces

Another problem related to heterostructures is represented by the lattice mismatch between different materials. The difference between lattice constants of the active region and the barrier layers induces *lattice strain* at heterointerfaces. In particular, lattice strain results in the formation of defects and dislocations in the crystal. The physical properties of defects in a crystalline structure were already discussed in

the section 1.7. An example is reported in Figure 2.18, that illustrates a crystal structure with lattice constant a_1 epitaxially grown on another crystal with lattice constant $a_0 > a_1$: dangling bonds can be observed at the heterointerface as a consequence of the lattice mismatch. As cited above, lattice strain negatively influences the optical efficiency of devices, due to the formation of defects and dislocations at heterointerfaces.

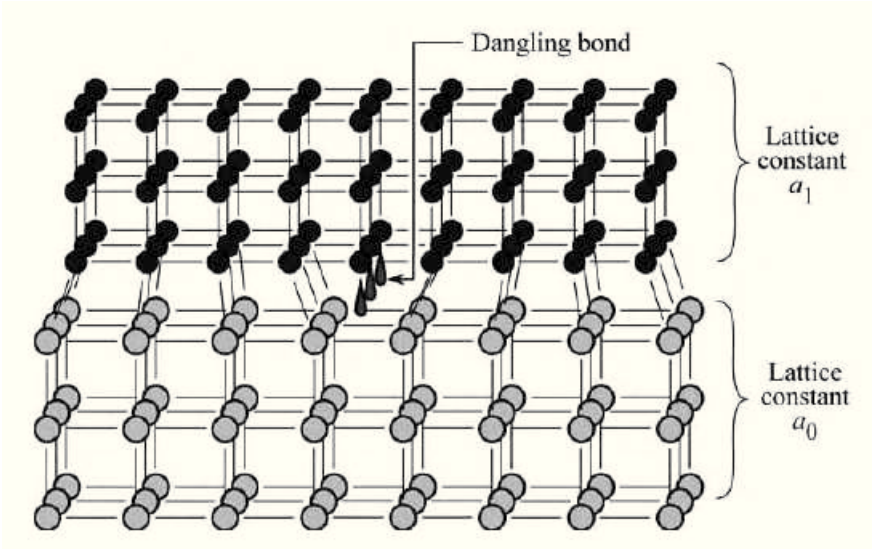

Figure 2.18: Schematic illustration of lattice strain between materials with different lattice constants in a crystal structure. Also dangling bonds can be observed as a consequence of lattice mismatch.

However, if the difference between the lattice constants of materials is small, it is possible to grow epitaxial layers with a small concentration of defects and dislocations. This is because the mismatched crystal grown on top of the semiconductor will initially be strained elastically and will assume the same in-plane lattice constant as the underlying substrate. Once the energy needed to strain the lattice exceeds the energy required to form misfit dislocations, the thin film relaxes to its equilibrium lattice constant by forming misfit dislocations. The layer thickness at which misfit dislocations are formed is called the *critical thickness* [34].

Finally, we have to consider that lattice strain induces also a piezoelectric field in the active region: as discussed in section 1.2.2, this field can induce a spatial separation between electrons and holes in the active region, resulting in a decrease of the optical efficiency. This effect is particularly prominent in heterostructures with high thickness of the active region. The problems related to piezoelectric field are reduced in quantum well structures, due to the small thickness of quantum wells.

2.2.3 Quantum well structures

A *quantum well structure* is a double heterostructure where the thickness of active region is very small, in the order of few nanometers. Thanks to the small active region thickness, very high carrier concentration ca be obtained in a quantum well LED, thus strongly increasing the radiative recombination rate.

Consider the single quantum well structure illustrated on the left side of Figure 2.19, where d_1 is the quantum well thickness. If the quantum well thickness is comparable to the De Broglie wavelength of electrons and holes, carriers are confined along the x-direction: as a consequence of this phenomenon, allowed energy states within the active region can no longer be considered continuous, but rather they become discrete. Thus, in such a structure, the active region acts as a potential well for carriers and for this reason it is called quantum well structure. The band diagram of a quantum well structure is shown in the center of Figure 2.19.

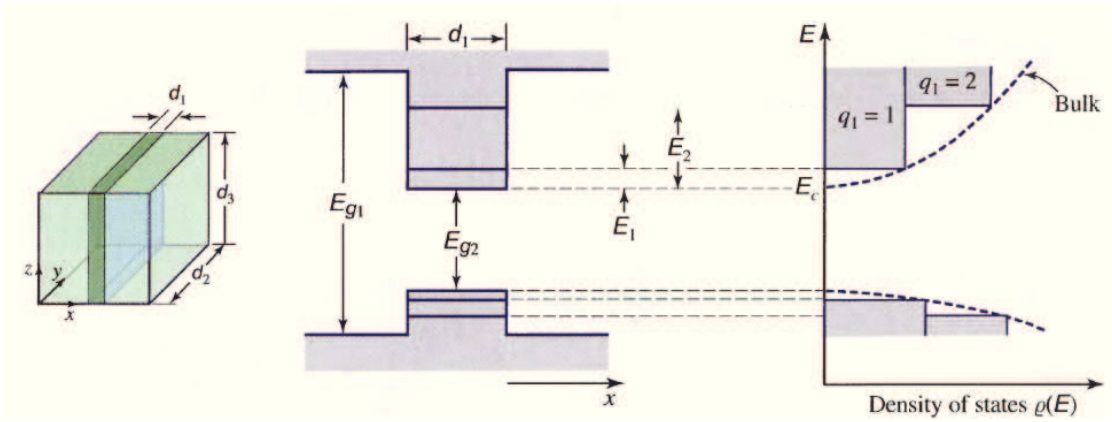

Figure 2.19: On the left side, tridimensional view of a single quantum well structure. On the center, band diagram of quantum well structure, showing the discrete energy states within the quantum well. On the right side, density of states in a quantum well structure.

Ideally, if the motion of carriers is permitted only along the x-direction, the recombination processes can occur only between discrete energy levels inside the quantum well. However, in practical cases, LED structure is tridimensional and thus, the quantum well has to be considered as a bidimensional layer: as a consequence, carriers are confined only along x-direction, but they can move freely along the other two directions. In this case, the energy-momentum relation for electrons can be expressed as follow [81]:

$$E = E_c + E_q + \frac{\hbar^2 k^2}{2m_c} \tag{2.28}$$

where E_c is conduction band edge, E_q is the difference between a discrete energy level inside the quantum well and the conduction band edge, m_c is the effective

mass of electron, and $k = (k_1,k_2)$ is the bidimensional wave vector relative to motion along y-z directions. Thus, from the relation (2.28), we can understand that recombination transitions do not exclusively occur between discrete energy levels. However, the quantum effect within the quantum well leads to a change in the density of energy states, as shown on the right side of Figure 2.28: in this case the density of energy states shows a piecewise constant trend, differently from the parabolic trend shown by a bulk semiconductor material. In particular, it is interesting to observe that the density of energy states is zero for energies lower than the fundamental level (i.e. the level with the lowest energy): this means that in a quantum well structure the lowest energy transition do not occur between the conduction and valence band edges, but rather between the fundamental discrete energy levels in the conduction and valence band of quantum well, respectively. This transition is illustrated in Figure 2.20.

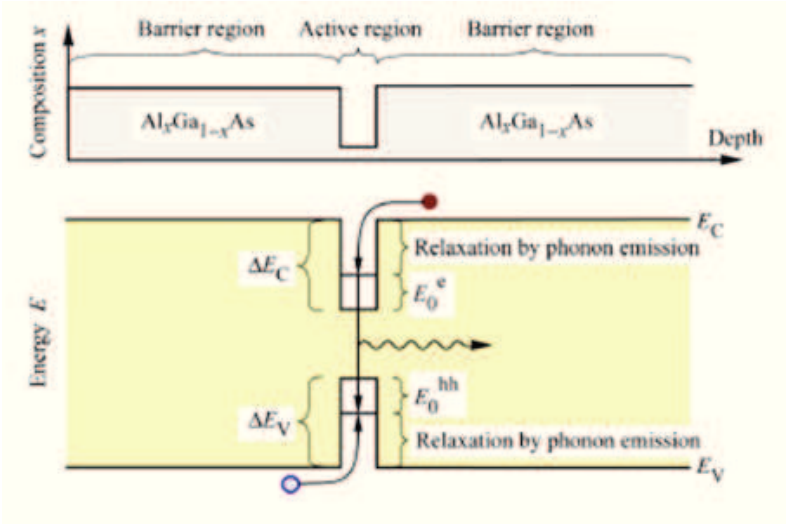

Figure 2.20: Material composition and band diagram of a quantum well structure. In particular, it is illustrated the radiative transition occurring between the fundamental energy levels in the conduction and valence band of quantum well.

Quantum well structures show some interesting advantages with respect to typical double heterostructures. First, the carrier concentration in a quantum well is higher than in a normal heterostructure, due to the reduced volume of active region: this determines an increase in the radiative recombination rate. Second, thanks to the small active region thickness, quantum well structures shows a smaller lattice strain and thus they can be grown with a small concentration of defects and dislocations. Finally, also the confinement effect due to piezoelectric fields is smaller in a quantum well structure with respect to a typical double heterostructure.

However, due to the reduced volume of the active region, the problem of carrier overflow occurring at high injection current is more severe in a quantum well structure with respect to a double heterostructure. To overcome this problem,

multiple-quantum well (MQW) structures are usually realized: by this way the active region volume is increased, without losing the advantages offered by quantum well structure. An example of AlGaAs/GaAs multiple-quantum well structure is illustrated in Figure 2.21.

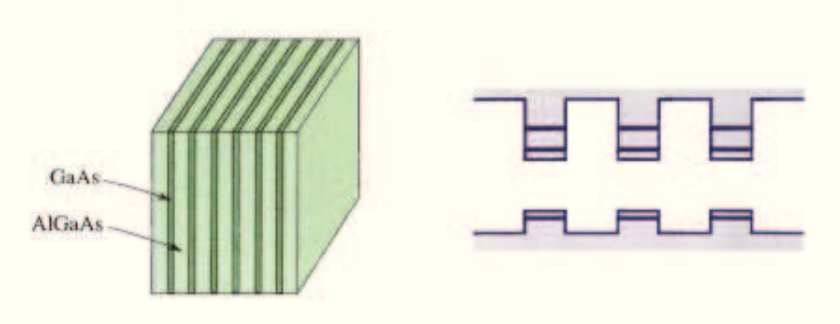

Figure 2.21: AlGaAs/GaAs multiple-quantum well (MQW) structure and relative band diagram. Because these materials are lattice matched in a large range of composition, they can be grown minimizing the lattice strain.

If the barrier layers thickness between the quantum wells of a MQW LED is very small, some of electrons can cross the barriers via tunneling effect: as a consequence, the discrete energy levels within the quantum wells degenerate into small bands. Finally, note that quantum well structures can be realized also by spatially varying the doping concentration of semiconductor, than rather the chemical composition: by this way, spatial charge layers, and thus potential barriers, are created in order to form quantum wells. [81].

2.3 Electrical properties of LEDs

Electrical properties of LEDs are described by the *current-voltage (I-V) characteristic* and by the *capacitance-voltage (C-V) characteristic*. In this section we will briefly review the main relations that describe the electrical properties of LEDs. However, for a more detailed and specific description of all the aspects concerning the electrical characteristics of the LEDs, reader can refer to [76] and [75].

2.3.1 Current-voltage (*I-V*) characteristic

From the electrical point of view, a light-emitting diode is equivalent to a *pn* junction diode and thus, the current-voltage (*I-V*) characteristic of an ideal LED is described by the well known *Shockley equation*:

$$I = I_s \left(e^{\frac{qV}{kT}} - 1 \right) \tag{2.29}$$

where I_s is the saturation current, which can expressed by the following relation:

$$I_s = A_{pn} q n_i^2 \left(\frac{1}{N_D} \sqrt{\frac{D_p}{\tau_p}} + \frac{1}{N_A} \sqrt{\frac{D_n}{\tau_n}} \right) \tag{2.30}$$

In the equation (2.30) A_{pn} represents the junction area, N_D and N_A are the donors and acceptors concentrations respectively, D_n and D_p are the diffusion constants for electrons and holes respectively, and finally τ_n and τ_p are the minority carrier lifetimes (electrons on the p-side and holes on the n-side respectively).
Figure 2.22 illustrates the I-V characteristic of an ideal pn junction in a linear and in a semilogarithmic scale, respectively. In particular, it can be noticed that under reverse bias condition the current saturates to I_s; on the other hand, under forward bias the current exponentially grows with increasing the applied voltage.

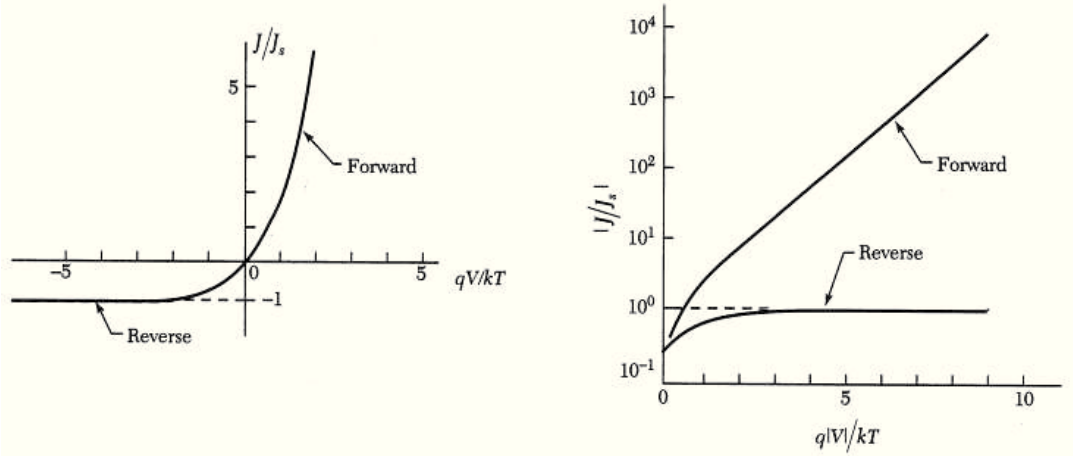

Figure 2.22: Current-voltage (I-V) characteristic of an ideal pn junction diode. The characteristic is shown in a linear scale on the left side, and in a semilogarithmic scale on the right side.

Under forward bias, for voltage levels much greater than the thermal voltage kT/q, the exponential term in the equation (2.29) dominates and thus the Shockley equation can be simplified with the approximate relation:

$$I \approx A_{pn} q \left(N_A \sqrt{\frac{D_p}{\tau_p}} + N_D \sqrt{\frac{D_n}{\tau_n}} \right) e^{\frac{q(V - V_D)}{kT}} \tag{2.31}$$

where V_D is *built-in* potential (also called the diffusion voltage) of the pn junction, which is given by:

$$V_D = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} \tag{2.32}$$

From the equation (2.31) it can be seen that the current of pn junction is very small, approximately equal to zero, for voltage levels lower than V_D, and it begins to exponentially grow for voltage levels greater than this value. The voltage level

at which the current starts to quickly grow is also called *threshold voltage* V_{th} and as we have just seen, it is approximately equal to the built-in potential V_D.

In the case of *pn* junction with high doping levels, the distance between Fermi level and conduction and valence band edges is very small: as a consequence, the built-in potential V_D is approximately equal to E_g/q. Thus, the threshold voltage is strongly related to the energy gap of the semiconductor material:

$$V_{th} \approx V_D \approx \frac{E_g}{q} \tag{2.33}$$

For this reason, the threshold voltage typically increases with decreasing of the optical emission wavelength. For example, red LEDs usually have a threshold voltage lower than that of blue LEDs. Figure 2.23 reports typical current-voltage characteristics of *pn* junctions realized with different semiconductor materials.

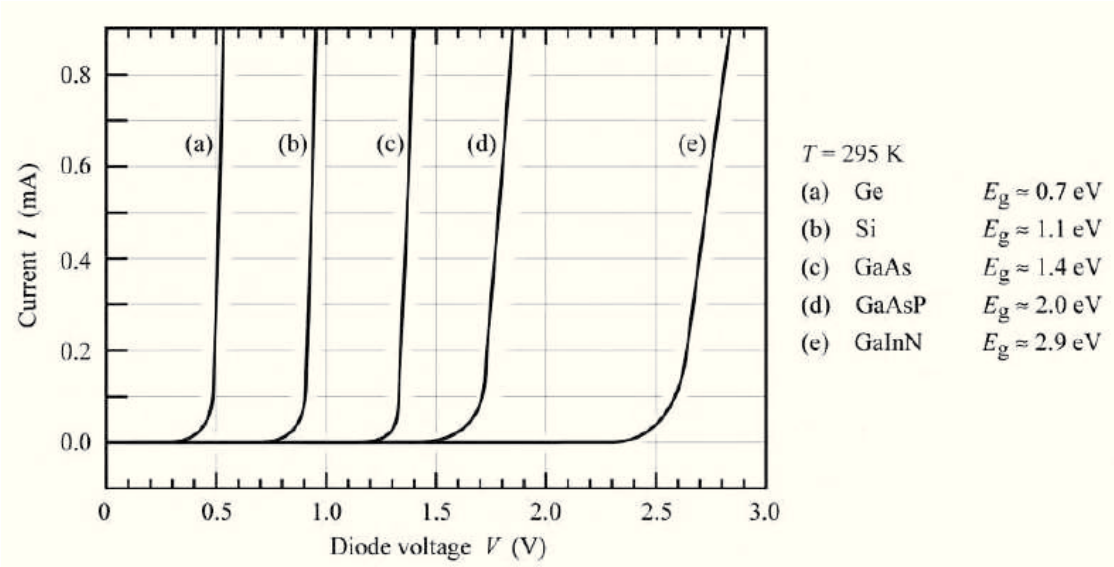

Figure 2.23: *I-V* characteristics of several *pn* junctions realized with different semiconductor materials. Note the increase in the threshold voltage with increasing of the energy gap.

For high reverse voltage levels, the breakdown phenomenon occurs in *pn* junction: this results in an abrupt increase of reverse current. Two different breakdown mechanisms can occur: the avalanche breakdown and the Zener breakdown. The voltage level at which this phenomenon starts can range from the order of tens of volts to hundreds of volts. In LEDs the breakdown voltage is usually quite low and this fact can represent a problem in some applications. For more details about the breakdown phenomenon occurring in diodes see [75].

2.3.2 Deviations from the ideal current-voltage characteristic

The current-voltage characteristic of a *pn* junction defined by the Shockley equation (2.29) has been obtained under the following ideality conditions:

1. negligible voltage drop across the contacts and neutral regions;
2. low-injection condition, i.e. the concentration of injected minority carriers is much smaller than that of majority carriers;
3. no recombination or generation processes occurs in the depletion layer.

In this section we will briefly analyze the non-ideality factors that can influence the electrical properties of LEDs and how they modify the current-voltage characteristic.

- **Generation and recombination processes in the depletion layer**: in practical diodes, there are trap levels in the depletion layer, which make generation and recombination events likely. Carrier generation and recombination causes an excess current for both forward and reverse bias.

  In the reverse-bias regime, the excess current is due to the generation of carriers in the depletion layer. On the other hand, under this operating regime, the recombination probability is very low because only a few carriers are injected in the active region. When a electron-hole pair is generated, due to the influence of the electric field present in the depletion layer, generated carriers are separated and drifted to the neutral regions. This results in the generation of a reverse current. If we suppose that generation processes occur via a deep level localized near the intrinsic Fermi level E_i, the generation current is given by:

  $$I_{gen} = A_{pn}\frac{qn_iW}{2\tau_0} \tag{2.34}$$

  where A_{pn} is the junction area, W is the depletion-layer thickness, and $\tau_0 = 1/N_t\sigma_0 v_{th}$ is the minority carriers lifetime defined in section 2.1.2 for the case of Shockley-Hall-Read recombination. At this point, the total reverse current of a *pn* junctions can be defined as follow:

  $$I_R = I_s + I_{gen} \tag{2.35}$$

  i.e. as the sum of saturation and generation current. Thus in practical diodes, the reverse current does not saturate to the saturation current value I_s, but rather it keeps increasing with reverse voltage due to the increasing depletion-layer width.

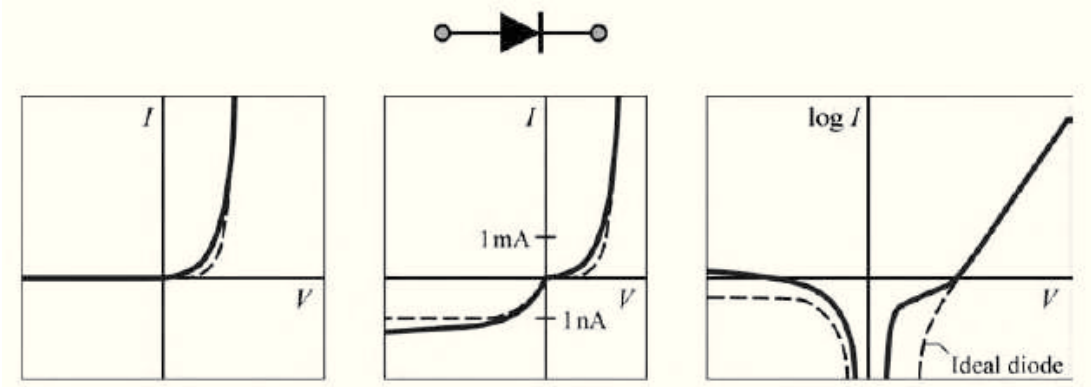

Figure 2.24: *I-V* characteristic of a *pn* junction, which includes the recombination and generation contributes. The characteristic is shown in the linear scale on the left side, with a particular of the curve near the origin on the center, and in semilogarithmic scale on the right side.

Under forward bias condition, the excess current is due to the recombination processes occurring in the depletion layer. The recombination current dominates only at low voltages. At higher voltages, the diffusion current dominates and thus the recombination current becomes negligible. Assuming that recombination transitions occur via a deep level lcoalized near the intrinsic Fermi level E_i, the recombination current is given by:

$$I_{rec} = A_{pn}\frac{qWn_i}{2\tau_0}e^{\frac{qV}{2kT}} \tag{2.36}$$

where A_{pn}, W e τ_0 are the junction area, depletion-layer thickness and minority carriers lifetime, respectively, as in the case of generation current.
The excess current under forward bias is also due to the surface recombination current, which is given by:

$$I_{sup} = A_{sup}Ce^{\frac{qV}{2kT}} \tag{2.37}$$

where A_{sup} is the external junction area and C is a generic constant that must be determined. Thus, the total forward current is given by the sum of diffusion contribution, and the two recombination currents defined in the equations (2.36) and (2.37), respetively:

$$I_F = I = I_s\left(e^{\frac{qV}{kT}-1}\right) + I_{rec} + I_{sup} \tag{2.38}$$

In typical silicon diodes, at low voltage levels, the recombination current in the depletion layer dominates, while in diodes based on III-V semiconductors, the dominant current at low voltage levels in due to the surface recombination [82]. In Figure 2.24 is shown the current-voltage characteristic of a *pn* junction, in both linear and semilogarithmic scale, when the recombination and generation contributes are taken into account.

- **Photocurrent**: if a photon is incident in the depletion layer of a *pn* junction, it can be absorbed, thus generating an electron-hole pair. The electrical field in the depletion layer separates the carriers and drifts them into the neutral regions. As a consequence, a photocurrent is generated, which is added to the reverse current. Alternatively, the generated electron-hole pairs can recombine, thus contributing to the excess recombination current under forward bias, at low voltage levels. In order to reduce the photocurrent contribution, measurements of *I-V* characteristic need to be carried out in the dark. In fact, photocurrent can negatively influence the measurements results. The effect of photocurrent on the current-voltage characteristic is reported in Figure 2.25.

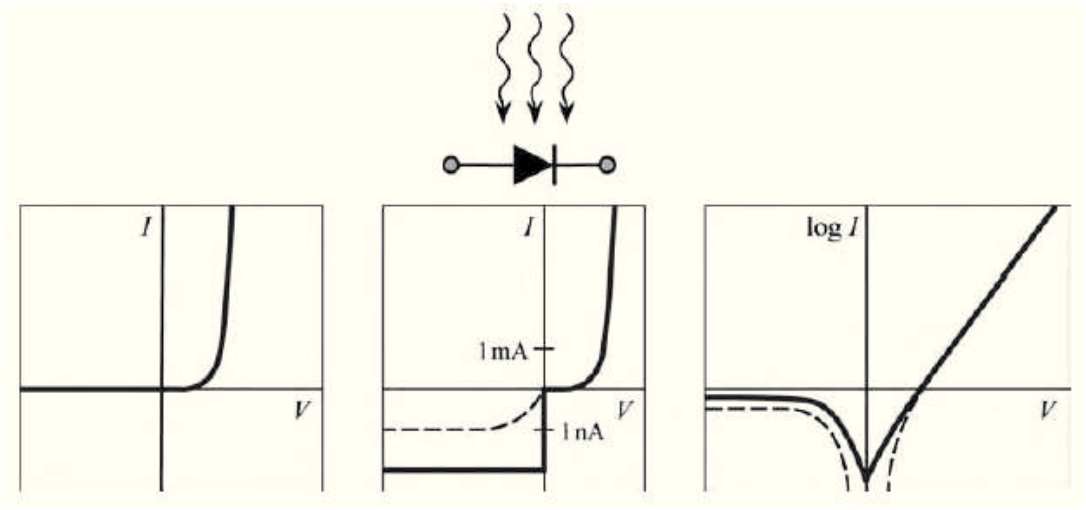

Figure 2.25: Current-voltage characteristic of a diode showing the photocurrent contribution. The characteristic is illustrated both on a linear and semi-logarithmic scale.

- **Series resistance and high-injection effects**: the resistance of contacts and neutral regions of a *pn* junction can be modeled with a resistance connected in series with an ideal diode. As a consequence, an additional voltage drops across it with increasing of current level. In particular, its contribution is negligible at low current levels, but it can be dominant at high currents. In fact, the *I-V* characteristic shows a deviation from the exponential behavior at high forward currents, as shown in Figure 2.26. Note that the series resistance has a linear and a logarithmic shape on the *I-V* characteristic when plotted on a linear and semi-logarithmic scale, respectively. Another contribution can modify the current-voltage characteristic at high current levels, that is the high-injection effects. This is due to the fact that in this operating regime the injected minority carrier concentration is comparable to majority

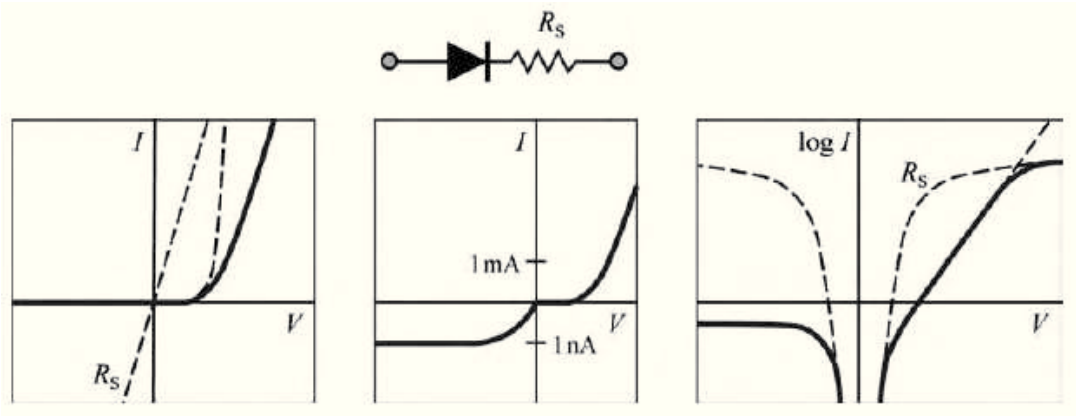

Figure 2.26: Current-voltage characteristic of a diode showing the contribution of a series resistance. The characteristic is reported both on a linear and semi-logarithmic scale.

carrier concentration and thus, the hypothesis used to derive the Shockley equation are no longer verified. Under these conditions, the current-voltage relation is given by:

$$I_{HI} \propto e^{\frac{qV}{2kT}} \tag{2.39}$$

Note the factor 2 present in the denominator of exponent [76]. As a consequence, also high-injection effects result in a decrease of the slope of characteristic with respect to the ideal case. However, at high current levels usually the dominant effect is given by the series resistance.

- **Parallel (shunt) resistance**: from an electrical point of view, defective regions and surface imperfections on a light-emitting diode can be modeled with a resistance connected in parallel with an ideal diode. This shunt resistance is usually very high, differently from the series resistance, which is usually quite low. The contribution of the parallel resistance is negligible at high current levels, because in this operating regime the current flowing across the junction dominates. On the other hand, the contribution of shunt resistance can be dominant at low forward voltage levels and under reverse bias. The parallel resistance effect on the *I-V* characteristic is reported in Figure 2.27: note that the forward "hump" seen on the semi-logarithmic plot has about the same level as the reverse current. This is a characteristic by which a shunt can be identified.

- **Parasitic diode with lower barrier height and smaller area than main diode**: surface states at the perimeter of the diode chip, or defective regions within the *pn* junction plane that have a lower barrier height than the main *pn* junction, can be sometimes modeled as parasitic diodes connected in parallel with the main diode. In particular such diodes display prema-

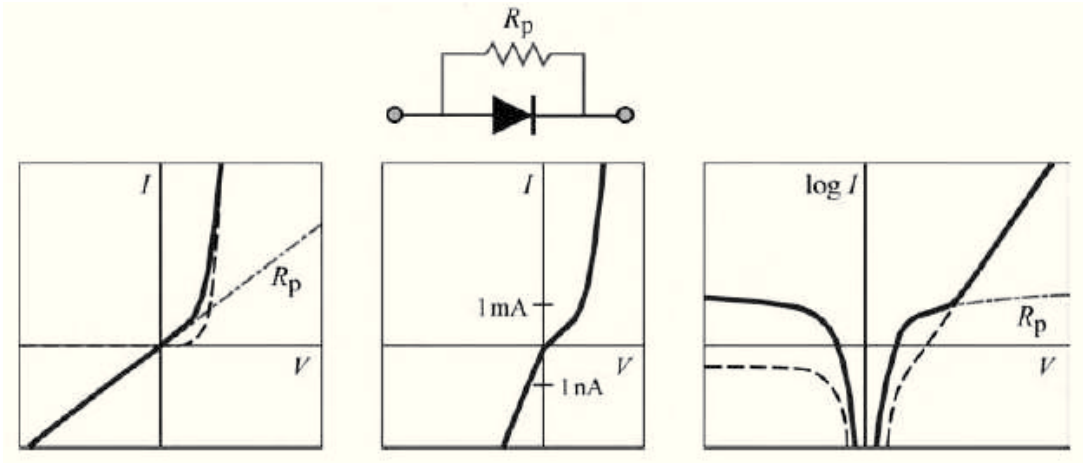

Figure 2.27: Current-voltage characteristic of a diode showing the contribution of a parallel resistance. The characteristic is reported both on a linear and semi-logarithmic scale.

ture turn-on, thus modifying the current-voltage characteristic, as shown in Figure 2.28. Note that the forward "hump" on the semi-logarithmic plot has much higher level than the reverse saturation current, which is not the case for diodes with a shunt [34].

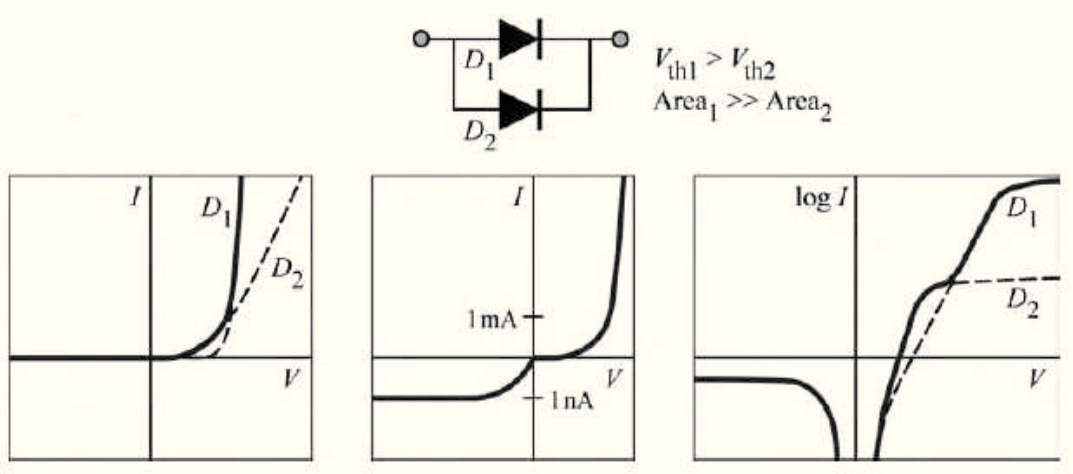

Figure 2.28: Current-voltage characteristic of a diode showing the contribution of a parasitic diode with lower barrier height and smaller area than main diode. The characteristic is reported both on a linear and semi-logarithmic scale.

Thus, the current-voltage characteristic, as given by the Shockley equation (2.29), needs to be modified in order to take into account parasitic resistances. Assuming a shunt resistance R_p (parallel to the ideal diode) and a series resistance R_s (in series with the ideal diode and the shunt), the I-V characteristic of a pn

junction diode is given by:

$$I - \frac{(V - IR_s)}{R_p} = I_s e^{\frac{q(V-IR_s)}{n_{id}kT}} \tag{2.40}$$

where n_{id} is the *ideality factor*: it is equal to 1 in the ideal case, while in practical diodes it is usually greater than 1. Under forward bias, $n_{id} = 2$ for low current levels, where the recombination contribute dominates. Then, $n_{id} = 1$ for medium current levels. Finally $n_{id} = 2$ for high-injection levels. However, n_{id} values greater than 2 can be found in several optoelectronic devices: for example, in InGaN/GaN based LEDs, n_{id} values as high as 7 can be found [34]. This phenomenon has been attributed to several factors:

- as suggested by Cao, Dmitriev and Eliseev, this behavior was attributed to the fact that in heterostructure-based devices conduction is based on significant tunneling components, that must be corrected using an appropriate parameter [83] [84] [85];
- Franssen observed that while in simple *pn* junctions recombination occurs in the neutral regions (Shockley model), in MQW structures radiative recombination takes place mostly in the middle of the depletion layer. This is expected to give rise to an increase of the ideality factor in the *I-V* characteristics [86];
- Shah considered that real diodes are formed by the series connection of more junctions, which contribute to the increase of the ideality factor of devices [87].

2.3.3 Temperature dependence of *I-V* characteristic

In this section, the temperature dependence of current-voltage characteristic will be analyzed. For the purpose, the study will be performed referring to a *pn* junction, but the results can be extended also to LED heterostructures. In particular, the temperature dependence of current-voltage characteristic under reverse bias and forward bias will be analyzed separately.

In the equation (2.35) we have seen that under reverse bias the current is given by the sum of saturation current I_s and generation current I_{gen}. Moreover, equations (2.30) and (2.34) show that both currents are proportional to the intrinsic carrier concentration n_i: in fact $I_s \propto n_i^2$, while $I_{gen} \propto n_i$. However, it is well known that the intrinsic carrier concentration increases with increasing of the temperature, as given by the following relation:

$$n_i = \sqrt{N_c N_v} e^{-\frac{E_g}{2kT}} \tag{2.41}$$

where N_c and N_v are the effective density of states at the conduction and valence band edges, respectively. It should be take into account also the temperature dependence of the energy gap E_g in the equation above, but it has been experimentally demonstrated that the term T in the denominator of exponent is dominant. Thus, an increase of the temperature results in an increase both of saturation current I_s and in the generation current I_{gen}. As a consequence, the reverse current increases with increasing of temperature.

In order to analyze the temperature dependence of current-voltage characteristic under forward bias, we calculate the temperature dependence of forward voltage across an ideal *pn* junction. To do this, we modify the Shockley equation (2.29) in the following form:

$$I = I_s^* \left(e^{\frac{qV - E_g}{kT}} - 1 \right) \tag{2.42}$$

where I_s^* is given by:

$$I_s^* = qA_{pn} \left(\frac{D_p N_c N_v}{L_p N_D} + \frac{D_n N_c N_v}{L_n N_A} \right) \tag{2.43}$$

Note that $L_n = \sqrt{D_n \tau_n}$ and $L_p = \sqrt{D_p \tau_p}$ are the diffusion lengths of electrons and holes respectively. The equation (2.42) has been derived from the Shockley equation using the temperature dependence of the intrinsic carrier concentration n_i reported in the relation (2.41). At this point, from the equation (2.42) we can derive an expression for the voltage V:

$$V(T) = \frac{kT}{q} \ln \frac{I}{I_s^*} + \frac{E_g(T)}{q} \tag{2.44}$$

The first term on the right hand is related to the temperature dependence of the Fermi level: with increasing of the temperature, the separation between quasi-Fermi levels E_{Fn} and E_{Fp} in the *n*-side and *p*-side decreases, because the Fermi energy shifts towards the middle of the gap. As a consequence, the forward voltage at a given current level decreases with increasing of the temperature. Note that even though this term is proportional to T, the temperature dependence of I_s^* is dominant.

On the other hand, the second term on the right hand of equation (2.44) is related to the temperature dependence of energy gap, which can be expressed by the following relation:

$$E_g(T) = E_g|_{T=0K} - \frac{\alpha T^2}{T + \beta} \tag{2.45}$$

where α and β are fitting parameters, frequently called the *Varshni parameters*. Thus, also this term decreases with increasing of the temperature at a given current level. In particular, it has been demonstrated that this term is usually dominant in the equation (2.44) [34].

Thus, the temperature dependence of the forward voltage results in a left shift of the *I-V* characteristic under forward bias, which correspond in a decrease of the threshold voltage. As an example, the temperature dependence of a GaAsP/GaAs LED is illustrated in Figure 2.29, which shows the *I-V* characteristic at 77 K and at room temperature. Inspection of the figure reveals that the threshold voltage as well as the series resistance of the diode increases as the diode is cooled [34].

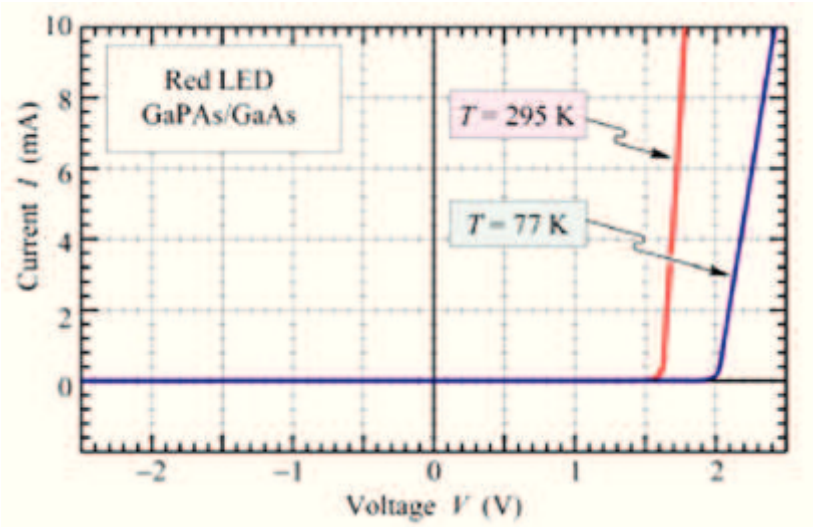

Figure 2.29: *I-V* characteristic of a GaAsP/GaAs red LED measured at 77 K and 295 K, respectively. The temperature dependence of the forward voltage can be observed from this figure.

2.3.4 Transport processes in light-emitting diodes

As we have seen in section 2.3.2, the equation (2.40) can be used effectively to describe the current-voltage behavior of optoelectronic devices, thanks to the presence of the ideality factor n_{id}. In fact, this parameter can be used to adjust the exponential dependence of current on voltage, in order to take into account that the carrier transport in practical devices involves other mechanisms with respect to the simple diffusion and recombination model provided by the Shockley equation.

In the recent years, a detailed description of the mechanisms ruling carrier transport in heterostructure LEDs has been provided by several literature works. Among these, we can remember the work of Hirsch *et al.*, which have described the temperature dependence of the *I-V* characteristic of multi-quantum well (MQW) LEDs [88]. Carrying out *I-V* characterization at different temperature levels (*I-V-T* measurements), they have identified different conduction mechanisms, which can be observed from the different regions of *I-V* characteristics illustrated in Figure 2.30.

As it can be observed in the figure, three different conduction domains have been

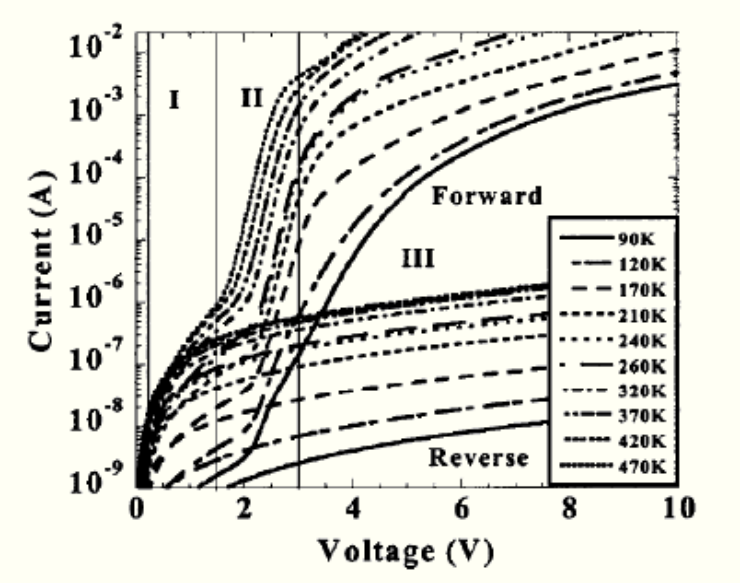

Figure 2.30: Typical *I-V* characteristics, as a function of temperature, of GaN-based LEDs under forward and reverse bias. It can be noticed the presence of three conduction domains, namely I, II and III.

identified by Hirsch *et al.*:

- For low forward and reverse bias (region I in Figure 2.30), carrier transport is dominated by a shunt resistance R_{sh}, and thus the current-voltage relation can be expressed as $I \approx V/R_{sh}$. In particular, this shunt resistance determines similar contributions both in forward and reverse bias. This shunt path has been attributed to hopping mechanism between next nearest neighbors electronic localized states (ELS) at low temperatures (less than 170 K) and to Poole-Frenkel mechanism, for T greater than the room temperature.

- For intermediate bias values (region II in Figure 2.30), carrier transport is dominated by tunneling processes at low temperature levels ($T \leq 250\,K$), while for higher temperatures the injection current is controlled by hole thermoionic emission from p-type GaN layer to the nearest quantum well.

- Finally, for high current values (region III in Figure 2.30), current is limited by the resistance of the neutral n-GaN and p-GaN access zones of the diode.

Furthermore, tunneling and Shockley conduction processes can be easily distinguished from *I-V* measurements carried out at different temperature levels [86]. In fact, if the Shockley conduction model dominates in a *pn* junction, the *I-V* characteristic can be described by the Shockley equation (2.29). On the other hand, if tunneling dominates conduction processes, the current-voltage behavior is well described by the following relation:

$$I = C_1 \left(e^{\frac{qV}{E_T}} - 1 \right) \tag{2.46}$$

where C_1 is a constant containing the built-in potential and the density of impurity traps, and E_T is an energy constant typical for tunneling processes. In a p^+/n step junction, this energy constant is given by:

$$E_T = \frac{4\hbar q\sqrt{N_D}}{\pi\sqrt{m^*\epsilon}} \tag{2.47}$$

where N_D is the donors concentration in the n-type material, ϵ is the dielectric constant of semiconductor material, and m^* is the effective mass of carriers.
Thus from the equations (2.29) and (2.46), we can see that the slope on a semi-logarithmic plot of the I-V characteristic shows a temperature-dependent behavior if the conduction is dominated by standard Shockley processes, whereas it is temperature-independent in the case of tunneling.

On the other hand, it has been observed that under reverse bias the leakage current is much higher than the classical saturation and generation current, given by the equation (2.34), which should be small in magnitude in wide band-gap materials and weakly voltage-dependent. In particular, Cao *et al.* have demonstrated that reverse dark current in LEDs was found to scale with *pn* junction area [83] [89] [90]. This suggests that the main mechanism is bulk leakage rather than surface leakage. They have also attributed this high reverse current to defect-assisted tunneling, or band-to-band tunneling. At low biases, field-dependent tunneling via defects located in the space-charge region could be a major contributor, while at high reverse voltages, the data are in good agreement with band-to-band tunneling as predicted by Zener tunneling model.
Furthermore, Li *et al.* have shown that the leakage current exhibits exponential dependence on the bias voltage, according to the relation $I = I_0 e^{qV/E_0}$ [91]. For low reverse bias, the main conduction process was attributed to leakage path through the surface states at the device mesa sidewalls, while for high reverse bias the probability of tunneling through defect states increases and this conduction process becomes dominant. In particular, Li showed that the preexponential factor I_0 is proportional to the square of the density of dislocations with a screw component, and that the energy parameter E_0 is related to the electrical activities of dislocations with a screw component, therefore attributing the entity of the leakage to the quality of the growth process.

2.3.5 Capacitance-voltage (C-V) characteristic

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To conclude the analysis of electrical properties of LEDs, in this section we will briefly review the capacitance-voltage (C-V) characteristic of a *pn* junction. It is very important to deeply understand the theory of capacitance related to a *pn* junction, because by means of C-V measurements, it is possible to evaluate the

distribution of charge in the proximity of the junction and to obtain information on the extension of the space charge region and band offsets and on the position of the heterointerfaces.

We start considering and abrupt *pn* junction, with acceptor and donor concentration equal to N_a and N_d in the two regions, respectively. It is well known that under reverse and low forward biases, a *pn* junction is equivalent to a capacitor associated to the space charge region (SCR), with plate separator distance equal to amplitude of SCR x_d and dielectric material equal to the semiconductor. Under forward bias, for voltage levels greater than the threshold voltage, the junction capacitance contribution disappear and the device capacitance is due to the diffusion capacitance, which is related to the modulation of minority carriers injected in the junction during LED operation. However, in the following we will not consider the contribution of diffusion capacitance, because in practical cases the C-V characteristic can be measured only for voltage levels lower than the threshold voltage. In fact, for high current levels, the *pn* junction no longer shows a capacitive behavior, but rather an inductive behavior. We recall that in an abrupt *pn* junction, the amplitude of the space charge region is given by the following relation:

$$x_d = x_n + x_p = \sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_a} + \frac{1}{N_d}\right)(V_D - V_a)} \tag{2.48}$$

where V_D is the built-in potential, while V_a is the external applied voltage, and x_n and x_p represent the amplitudes of SCR in the n-side and p-side, respectively. The fixed charge for unit of area in the SCR is expressed by:

$$Q = qN_d x_n = qN_a x_p \tag{2.49}$$

where N_d and N_a are the donors and acceptors concentrations, respectively. Note that the equality, shown in the equation above, comes from the charge neutrality principle. Since the charge Q varies with applied bias, we can define a low-signal capacitance for unit of area associated to the SCR, as:

$$C = \frac{dQ}{dV_a} = qN_d\frac{dx_n}{dV_a} = qN_a\frac{dx_p}{dV_a} \tag{2.50}$$

Using equations (2.48) and (2.50), we can express the junction capacitance for unit of area as a function of doping level and applied voltage, as follow:

$$C = \sqrt{\frac{q\epsilon}{2\left(\frac{1}{N_a} + \frac{1}{N_d}\right)(V_D - V_a)}} = \frac{\epsilon}{x_d} \tag{2.51}$$

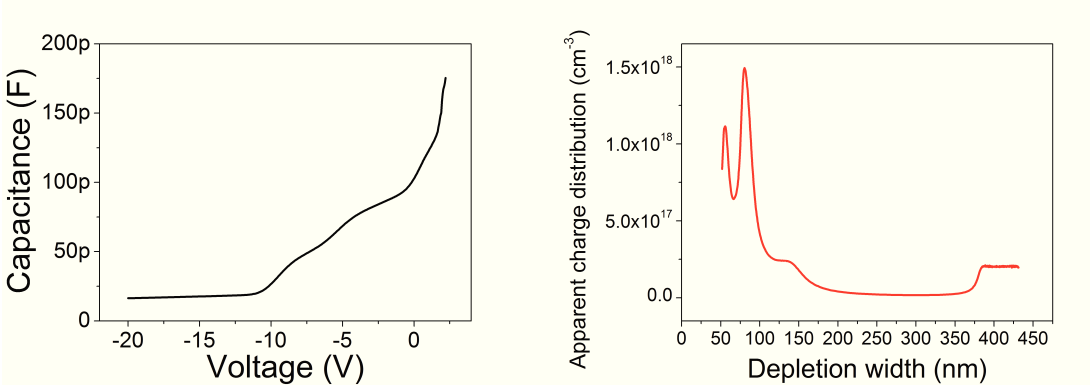
Therefore, from this expression we can understand that an increase of the applied voltage determines the narrowing of the SCR and the increase of the junction capacitance.

However, in practical diodes the doping concentrations N_d and N_a are not uniform in the n-side and p-side, respectively. This means that the C-V characteristic assumes a generic shape, depending on the charge distribution inside the junction. Consider a p^+n junction ($N_a \gg N_d$) with non-uniform doping distribution. In such a structure, the space charge region will extend mainly in the n-side, due to the heavy doping of p-type layer, i.e. $x_d \approx x_n$. Note that this assumption is usually verified in practical LEDs and thus, these results can be directly applied to practical cases. In this case, the concentration of charge at the boundary x_n of the SCR at the n-side can be expressed by the following relation:

$$N(x_n) = \frac{-2}{q\epsilon \left[\frac{d\left(\frac{1}{C^2}\right)}{dV_a}\right]} \tag{2.52}$$

This equation indicates that if the junction is asymmetric, the slope of the $1/C^2$ vs V curve is directly related to the concentration of charge at the border of the SCR. Thus, measuring the C-V characteristic of the device, and using the equation (2.52), it is possible to estimate the Apparent Charge Distribution (ACD) for one asymmetric diode. For more details about the C-V characteristic of pn junction, the reader can refer to [75].

However, in practical light-emitting diodes the presence of heterojunctions can strongly influence the behavior of the capacitance-voltage characteristics. The main difference with respect to simple pn junction is that in the case of heterostructure devices the bending of the conduction and valence band (due to a potential notch or to the presence of a quantum-well) can determine significant accumulation of free charge in specific regions of the devices. This free charge contributes to the capacitive behavior of the junction, as well as the fixed charge due to ionized dopant atoms. Thus, in principle it is not possible to describe a LED structure with a p^+n junction. However, it is very difficult to find an exact expression for the C-V characteristic of LEDs and for this reason in practical cases the equation (2.52) is still used to estimate the apparent charge distribution of LEDs, even though the result will represent only an approximation. Therefore, by means of capacitance-voltage characterization of an heterostructure-based device, it is possible to extrapolate information also on the position and characteristics of the charge accumulation regions. Furthermore, a C-V analysis can provide information on the band discontinuities at heterojunction interfaces. Figure 2.31 shows a typical C-V characteristic and the corresponding apparent charge distribution, obtained with the equation (2.52), for a typical MQW GaN-based LED.



(a) C-V characteristic. **(b)** Apparent charge distribution.

Figure 2.31: (a) Capacitance-voltage characteristic and (b) corresponding apparent charge distribution for a typical MQW GaN-based LED.

2.4 Optical properties of LEDs

To conclude the overview on light-emitting diodes, in this section we will analyze the optical properties of LEDs. Particular attention will be focused on the analysis of the emission spectrum and on the dependence of optical power on injected current in light-emitting diodes. However, also the radiation pattern and the light escape cone influence the optical properties of LEDs, but this features will not be analyzed in this section. For more details about optical characteristics of LEDs, the reader can refer to [34].

Before to analyze the emission spectrum and the optical power-current characteristic, we will briefly review the concepts related to the efficiency of a LED.
In an ideal LED, the active region emits one photon for every electron injected. Thus the ideal active region of a LED has a quantum efficiency of unity. However, in a practical LED the internal quantum efficiency is lower than the unity. The ***internal quantum efficiency***, that we have already introduced in the equation (2.27), can be defined as:

$$\begin{aligned} \eta_{int} &= \frac{\text{number of photons emitted from active region per second}}{\text{number of electrons injected into LED per second}} \\ &= \frac{P_{int}/h\nu}{I/q} \end{aligned} \tag{2.53}$$

where P_{int} is the optical power emitted by the active region and I is the injected current.

At this point, photons emitted by the active region should escape from the LED chip. In an ideal LED, all photons emitted by the active region will escape into the free space and such a LED has an extraction efficiency of unit. However, in practical LEDs not all the power emitted from the active region is emitted in the

free space and this can be due to several loss mechanisms. For example, light emitted by the active region can be reabsorbed in the substrate of the LED, or it may be incident on a metallic contact surface and be absorbed by the metal. Also the phenomenon of total internal reflection has to be considered as a possible loss mechanism. Thus, the light ***extraction efficiency*** can be defined as:

$$\begin{aligned} \eta_{extraction} &= \frac{\text{number of photons emitted into free space per second}}{\text{number of photons emitted from active region per second}} \\ &= \frac{P/h\nu}{P_{int}/h\nu} \end{aligned} \tag{2.54}$$

where P is the optical power emitted into free space.
In the case that the LED chip is not exposed to the air, but rather it is coated with a plastic lens or an epoxy encapsulant, the extraction efficiency can be expressed as the product of two terms: the extraction efficiency from LED chip η_{LEC} and the extraction efficiency from package η_{LEP}. Thus the total extraction efficiency in this case can be expressed as follow:

$$\eta_{extraction} = \eta_{LEC} \cdot \eta_{LEP} \tag{2.55}$$

In particular, in the case of white LEDs based on phosphors conversion, another factor has to be considered, that is the *phosphors conversion efficiency* η_{conv} [92].

To take into account the loss mechanisms related both to the generation of photons and to the extraction of photons from LED chip, the ***external quantum efficiency*** can be used, which is defined as follow:

$$\begin{aligned} \eta_{ext} &= \frac{\text{number of photons emitted into free space per second}}{\text{number of electrons injected into LED per second}} \\ &= \frac{P/h\nu}{I/q} = \eta_{int}\eta_{extraction} \end{aligned} \tag{2.56}$$

i.e. as the product of internal quantum efficiency and extraction efficiency.

To conclude, we can define the ***power efficiency***, also called *wallplug efficiency*, as:

$$\eta_{WPE} = \frac{P}{IV} \tag{2.57}$$

where P is the optical power emitted into free space, while the product IV is the electrical power provided to the LED. The power efficiency takes into account both for optical loss mechanisms and for electrical loss mechanisms. If we define the *electrical efficiency* η_{el} to take into account the electrical losses, the power efficiency defined in the equation (2.57) can also be expressed as follow:

$$\eta_{WPE} = \eta_{el} \cdot \eta_{ext} \tag{2.58}$$

2.4.1 Emission spectrum

In section 2.3 we have seen that the photons emitted from a LED have an energy approximately equal to the energy gap E_g. In an ideal LED, all emitted photons have the same energy and thus, the emission is monochromatic. However, this result has been obtained assuming verified two hypothesis:

1. the energy gap E_g of semiconductor material is much greater than the thermal energy kT/q;

2. we have supposed that all recombination transitions occur between the lower limit of conduction band and the upper limit of valence band.

In practical LEDs these hypothesis are not verified, because the carriers are distributed in the conduction and valence bands according to the Fermi-Dirac distribution and thus, recombination transitions can occur between different energy levels and not only between the edges of bands. As a consequence, photons with different energies can be emitted and the emission cannot be monochromatic. Thus, the emission spectrum of LEDs has a non-zero spectral width.

In order to calculate an expression for the emission spectrum of an LED, we start recalling the parabolic dispersion relations for electrons in the conduction band and holes in the valence band, respectively:

$$E = E_c + \frac{\hbar^2 k^2}{2m_e^*} \qquad \text{(per gli elettroni)} \tag{2.59}$$

$$E = E_v - \frac{\hbar^2 k^2}{2m_h^*} \qquad \text{(per le lacune)} \tag{2.60}$$

where m_e^* and m_h^* are the electron and hole effective masses, and E_c and E_v are the valence and conduction band edges, respectively.

In section 2.1.3 we have seen that, in order to obtain high values of radiative recombination efficiency, LEDs are usually realized with direct bandgap semiconductor materials, where the minimum of conduction band and the maximum of valence band in the $E - k$ diagram have the same momentum k. The dispersion relation of a generic direct bandgap semiconductor is shown in Figure 2.32. When an electron recombines with a hole, both energy and momentum conservation must be verified simultaneously. Because the momentum of emitted photons is usually much smaller than those of carriers, momentum conservation implies that transitions are vertical in the $E - k$ diagram, as shown in Figure 2.32. From this figure it is clear that not all emitted photons have the same energy and thus the emission is not monochromatic.

Using the dispersion relations of electrons and holes defined above and assuming that the distribution of carriers inside the bands can be approximated by the

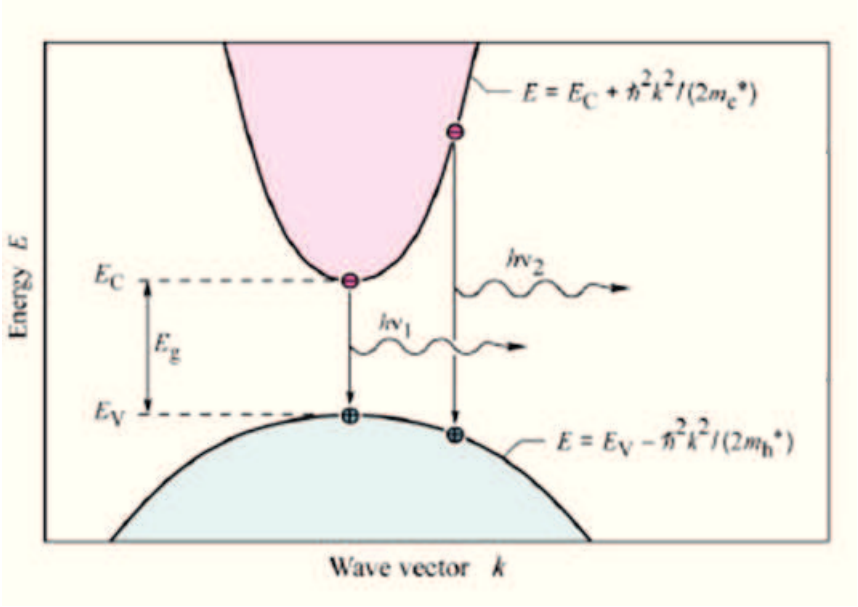


Figure 2.32: Parabolic electron and hole dispersion relations for a direct bandgap semiconductor, showing the vertical radiative recombination transitions.

Boltzmann distribution, it can be demonstrated that the *emission intensity* of LED can be expressed as a function of energy by the following relation:

$$I_t(E) \propto \sqrt{E - E_g} e^{-E/(kT)} \tag{2.61}$$

The lineshape of a LED is shown in Figure 2.33 as a function of energy: it can be noticed that for low energies, the intensity increases because the factor $\sqrt{E - E_g}$ in the equation (2.61) is dominant. On the other hand for high energies the intensity decreases because the term $\exp(-E/kt)$ becomes dominant. The maximum

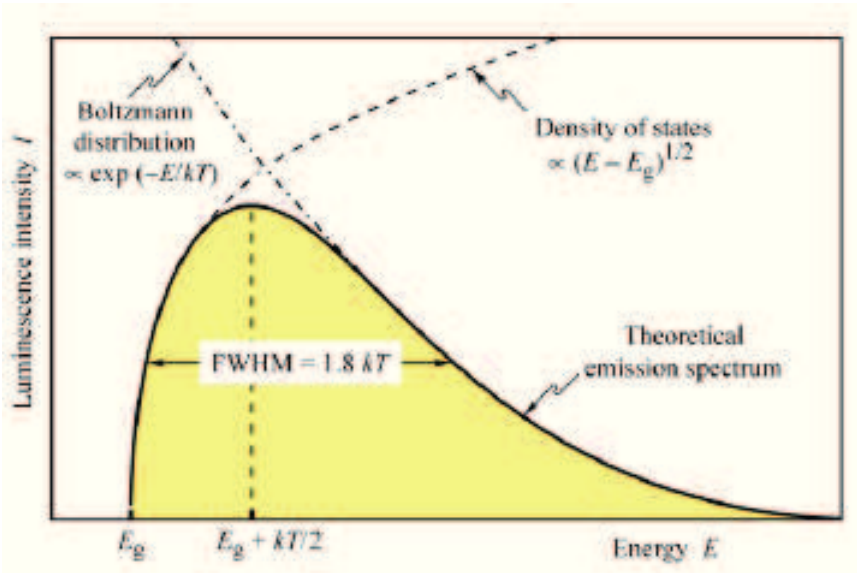


Figure 2.33: Theoretical emission spectrum of a LED as a function of energy.

emission intensity in the spectrum occurs at:

$$E = E_g + \frac{1}{2}kT \tag{2.62}$$

which corresponds the emission wavelength $\lambda = (hc)/E$.
The full-width at half-maximum (FWHM) of the emission is equal to:

$$\Delta E = 1.8kT \tag{2.63}$$

The FWHM can be expressed also in unit of wavelength as follow:

$$\Delta\lambda = \frac{1.8kT\lambda^2}{hc} \tag{2.64}$$

Note that the spectral width $\Delta\lambda$ is related to the emission wavelength λ by a quadratic law. Thus, the spectral width of a red LED will be grater than that of a blue LED, for example. However, the LED emission is usually narrower than the spectral width of a single color as perceived by the human eye. For this reason, LED emission is perceived by the human eye as monochromatic [34].

From the relation (2.62) we can see that varying the energy gap E_g, also the maximum emission wavelength changes. As a consequence, by appropriately choosing the semiconductor material, it is possible to determine the emission wavelength of LEDs. In the case of compound semiconductors, which are used for the realization of LEDs, it is possible to choose the emission wavelength also by changing the material composition of a ternary or quaternary alloy. As an example, Figure 2.34 shows the energy gap as a function of lattice constant for several compound semiconductors typically used in optoelectronic applications.

However, practical LEDs usually are characterized by an emission spectrum quite different from that reported in Figure 2.33: in ternary and quaternary compounds it is usually due to the *alloy broadening* effect, i.e. to the local variation in the material composition.

2.4.2 Temperature dependence of the emission spectrum

In this section the temperature dependence of emission spectrum of LEDs will be analyzed. In particular it will be analyzed the temperature dependence of both emission intensity peak and emission wavelength.

The emission intensity of LEDs decreases with increasing of the temperature. This is mainly due to the fact that at high temperature the non-radiative recombination rate increases with respect to the radiative recombination rate, as we have already seen in section 2.1.2: this obviously results in a decrease of the internal quantum efficiency. However, also other factors contribute to the reduction of emission intensity at high temperature levels: one of these, for example, is the increase

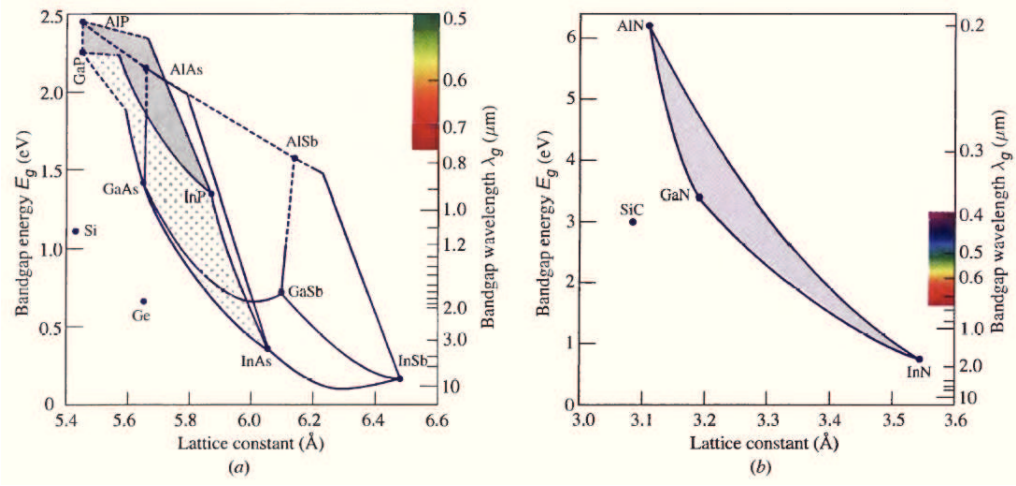


Figure 2.34: Energy gap and relative emission wavelength as a function of lattice constant for several III-V semiconductors. Solid lines are referred to direct bandgap ternary compounds, while dashed lines are referred to indirect bandgap ternary compounds. On the other hand, shaded areas are referred to quaternary compounds.

of carrier loss from quantum wells, due to the higher thermal energy of electrons and holes. Near room temperature, the temperature dependence of the LED emission intensity is frequently described by the phenomenological equation [34]:

$$I_t = I_t|_{300K} e^{-\frac{T-300}{T_1}} \tag{2.65}$$

where T_1 is the *characteristic temperature*. A high characteristic temperature, implying a weak temperature dependence, is desirable.

On the other hand, it has been experimentally observed that the emission wavelength increases with increasing of temperature: this results in a shift of the peak emission towards longer wavelengths. This phenomenon is due to the fact that with the increase of temperature the energy gap of semiconductor becomes smaller, as we have already seen in section 2.3.3: as a consequence, also the emission energy peak decreases, which corresponds to an increase in the emission wavelength. As an example, Figure 2.35 illustrates the emission spectra of an AlGaAs LED obtained at three different temperatures.

2.4.3 Optical power-current (L-I) characteristic

Another important optical property of LEDs is the optical power-current (L-I) characteristic, which reports the relation between the optical power L emitted by the device and the injected current I. In an ideal LED, the external quantum efficiency $\eta_{ext} = (P/h\nu)/(I/q)$ should be equal to unit, and thus the L-I characteristic should have the shape of a straight line. However, in practical LEDs this condition is not verified and the L-I characteristic shows different shapes, depending on the

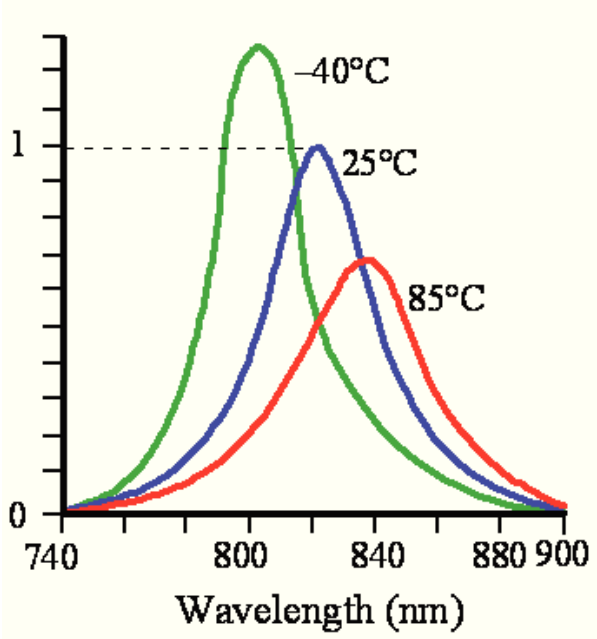


Figure 2.35: Emission spectra of an AlGaAs LED measured at three different temperatures. The values of intensity peak are normalized with respect to the intensity peak obtained at room temperature (25 $°C$). Note the reduction in the intensity peak and the shift of emission peak towards longer wavelengths with the increasing of temperature.

dominant recombination process in each region.

In order to obtain the optical power-current characteristic, we start writing the rate equation for LED under steady-state conditions [17]:

$$\frac{dn}{dt} = \frac{J}{qd} - (Bnp + AN_T n) = 0 \tag{2.66}$$

where J is the current density through the active region, d is the active layer thickness, q is the electron charge, Bnp is the radiative recombination rate and $AN_T n$ is the non-radiative recombination rate. In particular, B is the bimolecular recombination coefficient, while A is the non-radiative recombination coefficient adn N_T is the density of defects responsible for non-radiative recombination. Note that in the equation (2.66) any generation process has been neglected.

Under high injection conditions, which corresponds to medium-high injection current levels, the electron and hole concentrations injected in the active region are much higher than the steady-state concentrations, that is:

$$n \approx p \gg n_0, p_0 \tag{2.67}$$

where n_0 and p_0 are the steady-state electron and holes concentrations. Under this condition the equation (2.66) can be rewritten as:

$$Bn^2 + AN_T n - \frac{J}{qd} = 0 \tag{2.68}$$

In this operating regime, the radiative recombination represents the dominant process and thus it is verified the condition $Bn^2 \gg AN_T n$, due to the dependence on n^2 of BN^2 term. At this, point, observing that the optical power L is proportional to the radiative recombination rate Bn^2, one obtain:

$$L = Bn^2 \approx \frac{J}{qd} \tag{2.69}$$

i.e. the optical power is proportional to the injected current, resulting in a linear dependence for the L-I characteristic. Note that this condition is verified for medium-high current values.

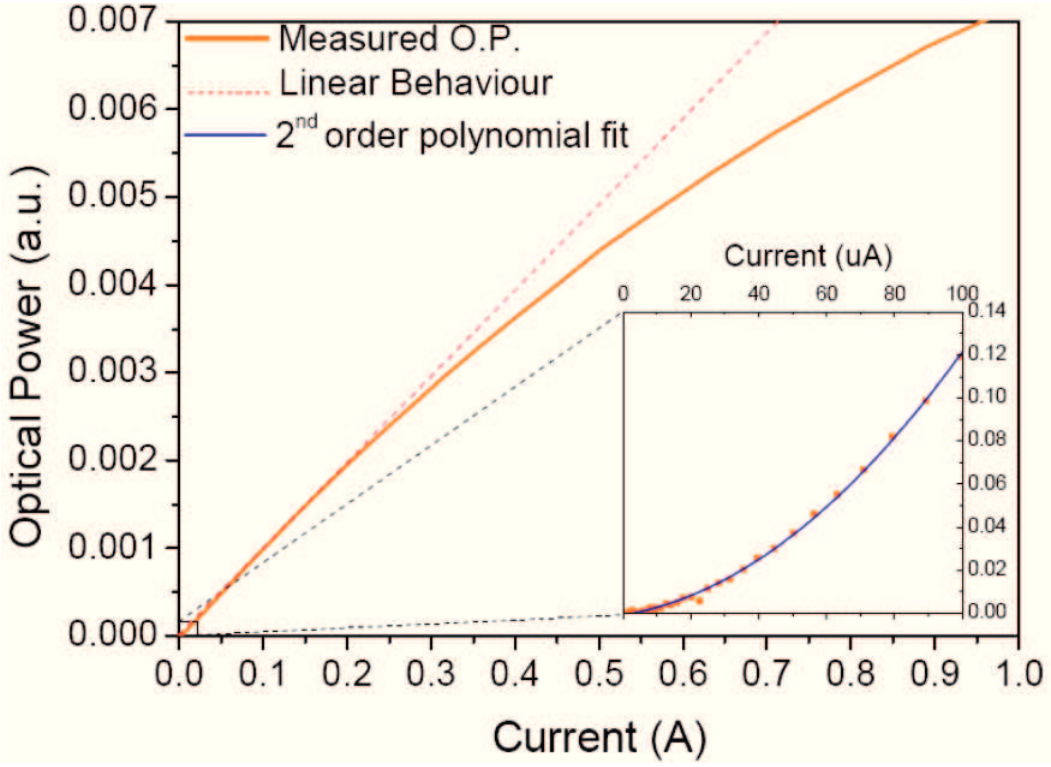


Figure 2.36: Typical optical power-current (L-I) characteristic of a LED reported on a linear-linear scale. The inset of figure shows in more detail the low current region.

On the other hand, under low-injection conditions, which corresponds low current levels, the injected carrier concentration is low and thus the dominant process becomes non-radiative recombination, due to dependence on n of non-radiative recombination rate. Under this conditions we obtain that $AN_T n \gg Bn^2$ and thus the equation (2.66) can be simplified as follow:

$$AN_T n = \frac{J}{qd} \tag{2.70}$$

Considering that also in this case the optical power is proportional to the Bn^2

factor, we obtain:

$$L = Bn^2 \approx \frac{B}{A^2}\left(\frac{J}{qdN_T}\right)^2 \tag{2.71}$$

i.e. for low current levels the optical power is proportional to the square of injected current, thus resulting in a quadratic dependence for the *L-I* characteristic.

At very high injection current levels, a further reduction in the slope of *L-I* characteristic can be observed, i.e. the optical power can be expressed as a function of the injected current by a sub-linear relation. This slope reduction can be attributed to several factors, including: *(i)* heating of the active region, which determines an increase of non-radiative recombination processes with respect to radiative recombination; *(ii)* carrier overflow in the quantum wells, occurring at high injection currents, and *(iii)* Auger recombination, which can be particularly severe in InGaN-based light-emitting diodes with high In content.

Thus summarizing, three different regions have been identified in the optical power-current (*L-I*) characteristic of a LED:

- at low current levels, where non-radiative recombination dominates, the *L-I* curve follows a quadratic law;
- at medium-high current levels, where radiative recombination dominates, the *L-I* curve follows a linear law;
- at very high current levels, the *L-I* curve follows a sub-linear law;

Figure 2.36 reports the optical power-current (*L-I*) characteristic for a typical LED.

Chapter 3

Electrostatic Discharges on LEDs

Electrostatic discharge events represent a critical problem for the reliability of electronic devices: in fact they can cause permanent damage that originates unexpected destruction of devices. It is estimated that the failure mechanism of 25 % of electronic devices is due electrostatic discharge phenomena. An ESD event can give rise to a current with very high intensity, which can reach values as high as tens of Amperes, and limited duration, comprised between tens and hundreds of nanoseconds. In particular, also LEDs are strongly sensitive to ESD events; typical damage induced by ESD events is a catastrophic failure, with short-circuiting of the junction: this usually results in an abrupt leakage increase and a decrease of optical power (note that in most of cases the LED does not emit light after failure). In the recent years, different solutions have been proposed by different research groups and companies, in order to provide adequate ESD protection to devices. For this reasons, it is fundamental to deeply understand the causes that originate electrostatic discharge events.

In this chapter we will discuss the ESD generation mechanisms and the effects of electrostatic discharges on optoelectronic devices. Also ESD stress models will be discussed, including the Human Body Model (HBM), the Charged Device Model (CDM) and the Machine Model (MM). Afterwards, also the Transmission Line Pulse (TLP) technique as alternative method to carry out ESD stress test will be discussed. Finally, typical device protection strategies and an overview on previous works on ESD effects on LEDs will be presented.

3.1 ESD generation mechanisms

In order to understand the origin of ESD phenomenon, consider two charged objects set at a distance d one from each other, as represented in Figure 3.1. Suppose that the two objects are conductive. If there is an accumulation of charge with opposite polarity on the two surfaces, as in the case of Figure 3.1, an electric field

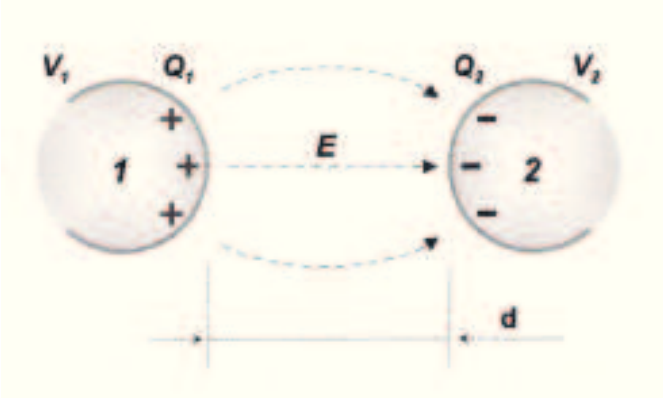


Figure 3.1: Two charged objects at a distance d from each other. Note that both objects are conductive.

E is formed in the surrounding space, which generates a force that acts on the atoms, free electrons and ions in the dielectric material between the two objects. In particular this field generates a current between the two objects that in most of the cases, if the intensity E is low, is negligible. Note that the intensity of field E depends on the quantity of charged stored on the two facing surfaces, on the distance d and on the characteristics of the two surfaces.

In the intensity of electric field E becomes higher, due for example to an increase of charge on the surfaces, or a reduction of distance d between them, the induced force can becomes strong enough to both break the bonds between electrons and nucleus in the atoms of dielectric material (air, for example) and free the electrons stored on the surface, thus increasing the current flowing between the two bodies. The increase of E can also lead to impact generation of electron-ion couples because of the increased kinetic energy of the free charged particles. The high current generated by this phenomenon is also known as avalanche discharge or *electrostatic discharge (ESD)*. During the ESD event, the dielectric loses its electrical insulator properties and becomes temporary conductive. The transition from isolation to conduction condition requires the breakdown of insulator or, if the breakdown condition is not fulfilled during the approach of the objects, the direct contact between the two objects. Finally, a low resistance plasma channel of ionized gas develops, and the formation of this resistive phase results in a visible and audible spark. As an example, the dielectric strength of air is about 30 kV/cm.

The amplitude, duration and waveform of electrostatic discharge are strongly influenced by several factors, including the time and current-dependent resistance of the plasma channel, the external resistance, the capacitance and the inductance of discharge circuit. An ESD can easily reach current values as high as some tens of Amperes and rise times less than 1 ns: in particular, this high current flowing can permanently damage electronic devices. During this phenomenon, the charge

redistribution causes the electric field to decrease rapidly. Note that, in order to maintain the electric arc, the voltage difference between the two objects must be higher than a minimum value of about 10 V and the discharge current must be higher than a minimum value too. When one of these two conditions is no longer met, charges automatically stop flowing.

On the other hand, in the case of "direct contact ESD" , i.e. when two charged objects get in touch before the conditions for arc generation are encountered, the formation of a real low-impedance conductive path between objects occurs, because charges can move directly from one object to the other. In this condition, which is often verified in practice, the generated current can reach higher values than in the case of arc generation. However rise times are usually shorter in this case.

At this point, it is interesting to analyze the physical mechanisms by means of two objects can be charged with opposite polarity. Four basic mechanisms that cause charge accumulation, thus generating electrostatic voltages, can be identified: triboelectric charging, ionic charging, direct charging and field-induced charging.

The ***triboelectric charging*** effect results from the mechanical contact and separation of two surfaces with different electron affinity. In particular, the object with the higher affinity acquires electrons and thus, after the separation, it will remain negatively charged with respect to the object with lower affinity. If the charges cannot immediately recombine, consecutive cases of contact and separation increase the amount of charges accumulated on the two surfaces, thus building up the electrostatic voltage. It is very important to notice that no friction or rubbing in necessary to generate and separate charge. Note also that a faster separation between objects reduces the chance of charges to recombine.
This charging process can be influenced by several factors, including humidity, temperature, contamination of surfaces, roughness and pressure of the surface contact. In particular, humidity increases the surface conductivity, thus increasing the recombination rate. In general, highly insulating hydrophobic materials, such as Teflon for example, are the most susceptible to charging and they can carry the charge for a very long time. Typical materials with different electron affinity, which can charged by triboelectric effect are listed in the Figure 3.2, from that ones with lower affinity on the top to that ones with higher affinity on the bottom of figure. In real-world situations, tribocharging occurs for example when walking on a carpet or rising from a chair. Triboelectric effect can also charge moving parts of machines as well as electronic devices. It also results from spray cleaning, for example, with pressurized high-resistive deionized water or from blasting with carbon dioxide pellets. Note that without proper grounding, for example, with wrist straps or controlled conductivity, tribocharging can generate electrostatic voltages as high as some tens of kV on persons. On the other hand, voltage levels reached by charged machines and electronic devices are usually lower. Corona discharges

or residual conductivity may also limit the voltage.

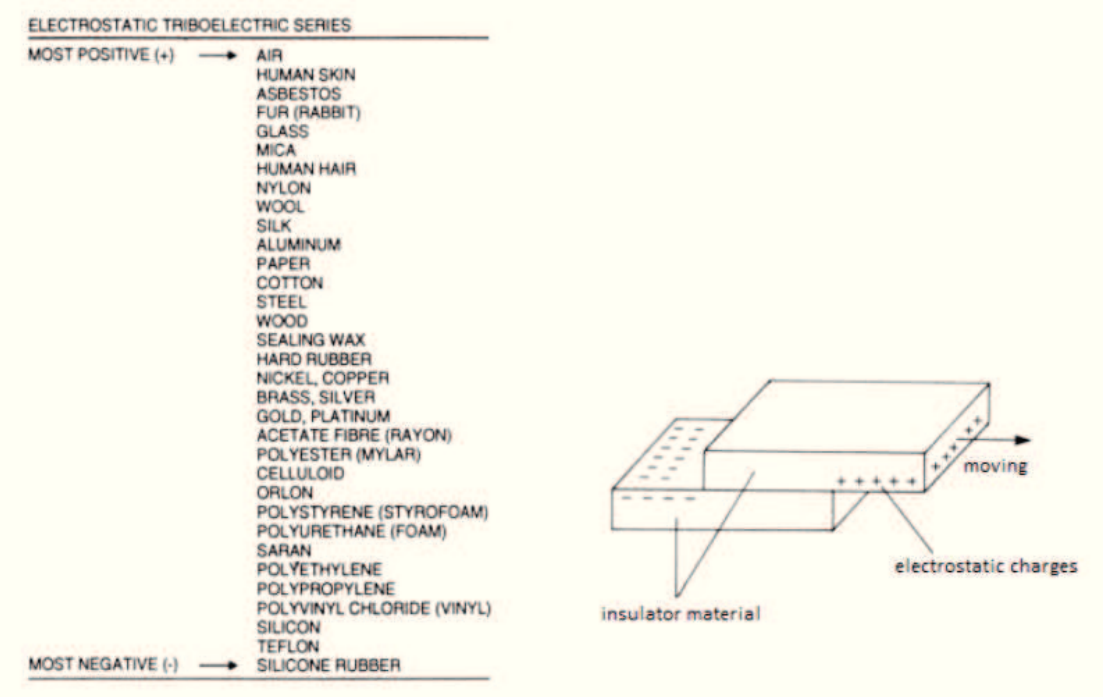


Figure 3.2: Electrostatic triboelectric series and illustration of typical tribocharging phenomenon.

Another charging mechanism is the ***ionic charging***, which is associated with the use of air ionizers. Note that air ionizers are fundamental for the neutralization of immobile charge on insulating surfaces. The ionic charging occurs only if the flow of ionized gas molecules is not properly balanced or adjusted to the charging properties of the individual manufacturing process step. The resulting voltage can be as high as some hundreds of volts. Note that this charging phenomenon, as well as triboelectric effect, are quite low processes.

Direct charging occurs when mobile charge is directly transferred from a charged object to another object by means of direct contact. This phenomenon may be associated with the insertion of a device into a test socket for example.

Finally, ***field-induced charging*** occurs when a neutral object is brought slowly into an external electrostatic field, or the electrostatic field increases. This external field induces the separation of mobile charge on the conductive parts of the object and, as soon as this still neutral body come in contact with another conductive object, at a different voltage, a very narrow and high current level pulse charges it. After this first stress, the object is charged and can consequently give rise to another electrostatic discharge involving other bodies. In particular, this process is closely related to direct charging process.

Among this mechanisms, tribocharging is the main cause for the generation of electrostatic field and consequently ESD events.

3.2 ESD stress models

In this section the ESD stress models typically used in electronic applications will be analyzed: the aim of this models is to describe the different types of ESD-phenomena occurring in an electronic environment. These models are also used by manufacturers and users of electronic devices to derive ESD test methods. In particular, three different ESD stress models will be described in this section:

- Human Body Model (HBM);
- Machine Model (MM);
- Charged Device Model (CDM).

There are also other stress models, including the SDM (Socket Discharge Model), the Contact Discharge Model, the Charged Board Model and the Cable Discharge Model, that is related to any cable connection. However, these models are not of interest for us, also because they give high reproducibility problems in practical cases. For this reason, these models will not be discussed in this section. Another particularly important ESD stress models is the TLP (Transmission Line Pulse), that will be discussed in more detail in the next section.

3.2.1 Human Body Model (HBM)

The ***Human Body Model (HBM)*** is used to describe and reproduce ESD events that occur when a charged person touches a grounded device, or gets near enough to the device to cause an electrostatic discharge. When the air breaks down between the finger and the electronic device, the capacitance of the person is discharged via the device into ground, thus generating a current pulse that can permanently damage the device. In particular, the human body model defines the current waveform for the discharge of a $100\,pF$ capacitor, which represents the body capacitance to the ground, through a $1.5\,k\Omega$ resistor, which represents the body resistance, and a $0\,\Omega$ load for different discharge voltages. Figure 3.3 shows a typical situation in which the usage of human body model is appropriate. The same figure illustrates also the equivalent circuit used for the human body model.

The ideal HBM model can be modeled with an equivalent RLC circuit and thus the discharge current ca be easily calculated from the solution of the second order differential equation:

$$\frac{d^2i(t)}{dt^2} + \frac{R}{L}\frac{di}{dt} + \frac{1}{LC}i = 0 \tag{3.1}$$

It can be demonstrated that in the HBM case the oscillation frequency $\omega = 1/\sqrt{LC}$ does not exceed the damping coefficient $\alpha = R/2L$, and thus the discharge is aperiodically damped. Thus, the parameters that characterize the current waveform are

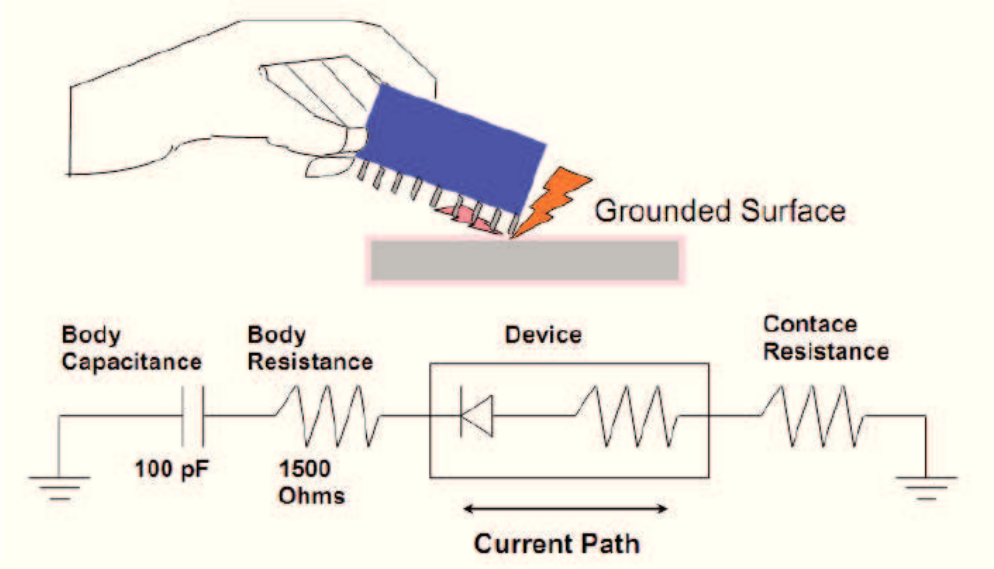


Figure 3.3: Practical situation in which a charged person touches a grounded integrated circuit and equivalent circuit for the Human Body Model (HBM).

C_{HBM}, that stores the charge, R_{HBM}, that limits the current, and L_{HBM}, which is the effective inductance of the discharge path in a real tester. This parameter, together with R_{HBM} determines also the rise time of the pulse. Note that the HBM model specifies the rise time of pulse as between $2\,ns$ and $10\,ns$ from 10 % to 90 % of the amplitude I_{MAX}, and it specifies also that the pulse amplitude has to decay to $1/e \cdot I_{MAX}$ within the $150\,ns$ that follow the rising time.
The solution of differential equation (3.1) for the case of HBM model is given by:

$$I_{HBM} = V_{HBM} C_{HBM} \frac{\omega_0^2}{\sqrt{a^2 - \omega_0^2}} e^{-\frac{R_{HBM}}{2L_{HBM}}} \sinh\left(\sqrt{a^2 - \omega_0^2}\right) t \tag{3.2}$$

where $a = R_{HBM}/2L_{HBM}$ and $\omega_0 = 1/\sqrt{L_{HBM}C_{HBM}}$, and $a > \omega_0$. The rise time can be estimated from this solution, obtaining:

$$t_{rise} = \frac{2L_{HBM}}{R_{HBM}} \tag{3.3}$$

In order to obtain a rise time of $10\,ns$, L_{HBM} is required to be about $7.5\,\mu H$. Thus, the HBM model represents a slow pulse, with typical rise times in the order of $10\,ns$, fall times of about $100 - 300\,ns$ and a high energy content. Finally, note that in a real HBM system additional parasitic elements are present, which may influence the discharge waveform.

3.2.2 Machine Model (MM)

The ***Machine Model (MM)*** is aimed to simulating abrupt discharge events which are caused by contact of devices with equipment and empty sockets (functional

test, burn-in, reliability testing, etc.). In particular, the discharge is generated externally to the device. This model was originally developed in Japan as a severe HBM and actually is widely used there.

The machine model is a low-impedance, high-current discharge, that oscillates if the load has a low value of impedance. The equivalent circuit is similar to the HBM circuit of Figure 3.3: the capacitance C_{MM} has a value of $200\,pF$, while R_{MM} is nominally $0\,\Omega$. For the inductance, an effective value of $0.75\,\mu H$ has been defined. Solving the differential equation (3.1), which is obviously applicable also to the machine model, we observe that the oscillation frequency $\omega = 1/\sqrt{LC}$ exceeds the damping coefficient $\alpha = R/2L$ in the machine model with low resistive loads: for this reason the discharge is an oscillation in this case. However, in a real ESD tester the resistance R_{MM} will be higher than 0 and thus the oscillation will be dumped. A typical situation that is well described by the machine model and the equivalent electrical circuit are reported in Figure 3.4, together with an example and the equivalent circuit of both human body model and charged device model. On the other hand, in Figure 3.5 is illustrated a comparison between the current waveforms of the three basic ESD stress models, i.e. HBM, MM and CDM, together with typical values of electrical components used in the equivalent circuits.

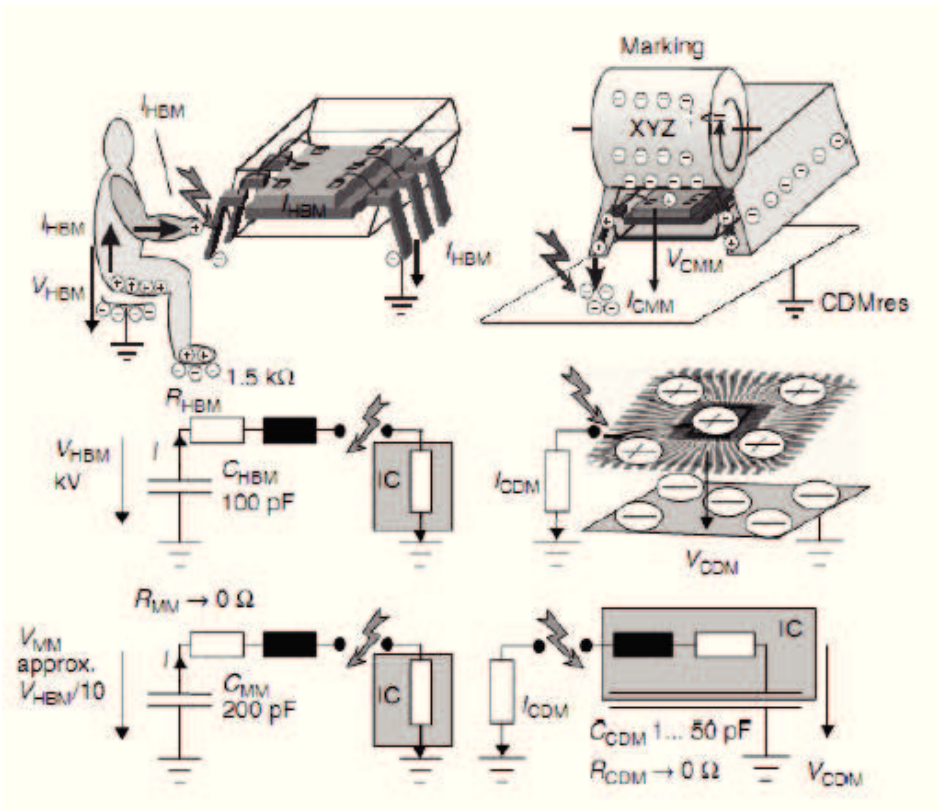


Figure 3.4: Practical situations in which the ESD stress models HBM, MM and CDM can be applied, and equivalent electrical circuits.

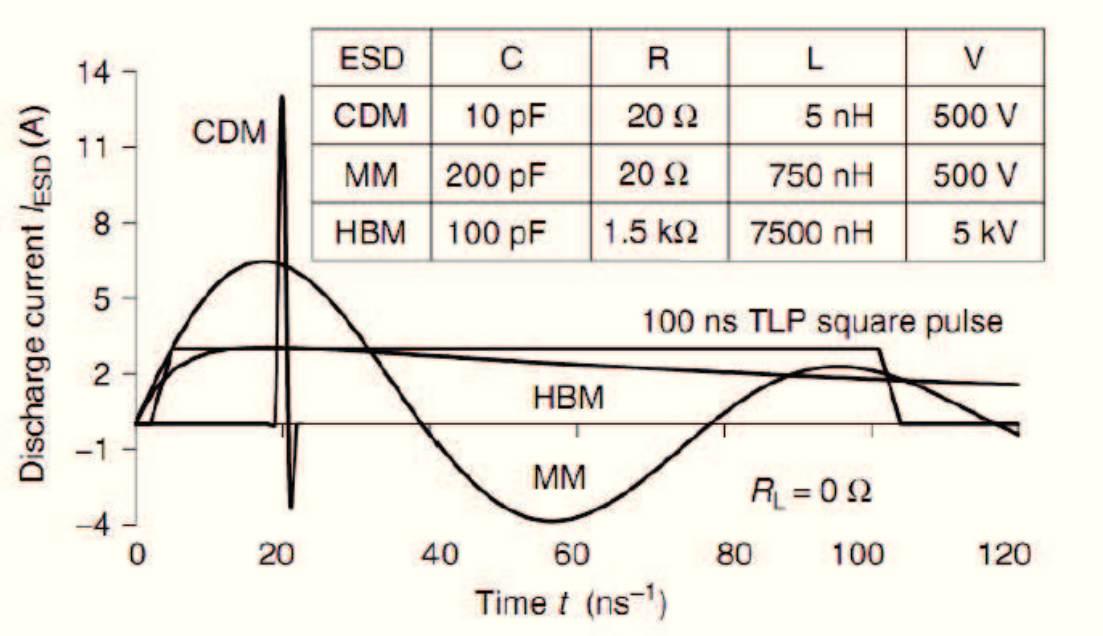


Figure 3.5: RLC discharge current waveforms of the three basic ESD stress models, HBM, MM and CDM in comparison with a TLP square pulse. Also typical values of electrical elements of RLC circuits are reported.

In comparison to the HBM, the machine model generates a very similar type of power-related failure in the *pn* junctions, but the pre-charge voltages at which they take place are lower. This happens because the pre-charge voltages in machine model correspond to higher current levels. For example, 200 V stress level in MM corresponds to a peak current of 3.5 A. The higher peak current occurring in MM with respect to HBM is also shown in Figure 3.5. From the same figure, it can be also seen that the MM is a fast pulse, compared to HBM, with a duration of a few tens of nanoseconds.

Finally, note that also in a MM-tester the parasitic elements have a very strong influence on the discharge current waveform, in particular through an integrated circuit with its dynamically changing impedance. The influence of parasitics on the MM waveform is even more significant in comparison with HBM.

3.2.3 Charged Device Model (CDM)

The ***Charged Device Model (CDM)*** simulates the ESD event occurring when an electrostatically charged device is abruptly discharged to a metallic ground. In particular, the discharge is generated internally to the device. The simulated event is most likely to occur in automated manufacturing lines which involves inadequate grounding or shielding for the IC devices. In particular, this type of phenomenon leads to two different models, a *charged device model (CDM)* and a *field-induced charged device model (FCDM)*, that differ in the charge-up method.

In both of them, in the worst case, the discharge is determined by the capacitance of the device, the inductance of the pin, and the resistance of the ionized channel, resulting in an extremely narrow pulse with a high peak current even for voltages around $1\,kV$.

The CDM pulse is characterized by a rise time less than $500\,ps$, a total duration of a few nanoseconds and with amplitudes of up to some tens of amperes. The typical current waveform of a CDM pulse is shown in Figure 3.5, in comparison with HBM, MM and TLP pulses. A typical situation in which CDM model can be applied and the equivalent discharge circuit are reported in Figure 3.4. Typical device damage that can be induced by CDM pulse is the oxide rupture due to the IR drops in the metal and poly lines of integrated circuits: this is due to the high peak current values that can reach CDM with respect to HBM and MM.

Also the charged device model is very sensitive to parasitic elements and for this reason the testers are very difficult to build. Moreover, unlike for the $1.5\,k\Omega$ current source characteristic of HBM with a nearly ideal or at least appropriate capacitor, resistor, and relay, the CDM-discharge circuit strongly depends on the device and on several environmental conditions. Another important thing to notice about this model is that different CDM testers exist, even though they will not be discussed in this thesis. Finally, unlike in HBM, in CDM the package determines the capacitance and contributes to the impedance of the discharge path. Therefore, the failure threshold depends directly on the package and any change of it or its material requires a new CDM qualification. This characteristic, together with the difficulty to build testers and the reproducibility problems shown in the previous sections, make it difficult to develop a unique standard and the CDM test method is actually still evolving.

To conclude this overview on three basic ESD stress models, it is important to point out that not all practical cases can be related to just one specific model. For example, the situation in which a charged person is putting a device onto a low resistive tabletop is something between the HBM and CDM model. The pulse that originates in this case can be considered as a combination of a fast high-current CDM pulse followed by an HBM discharge. Another interesting case is that one of a charged person discharging its capacitance via a metallic tool into a grounded object or an object with a large capacitance to ground: this situation results in a initial narrow peak rising in less than 1 ns that discharges the local capacitance of the tool, followed by a longer period in which the person is discharged. This case is also described by the so called System Level HBM, which is a more severe two-terminals stress model, typically employing a main capacitor of $150\,pF$ and a resistor of $330\,\Omega$.

Furthermore, it has to be considered that the three ESD stress models analyzed above describe a discharge through or into a device that is not powered. However,

in practical cases the electronic device can be connected to the power supply and in this cases the ESD effects may be worse. Thus, it is important to remember that these models do not describe every possible practical case; nevertheless, they are the ones currently employed in most of cases for the study of ESD phenomena and for the development and testing of experimental and commercial devices.

3.3 Transmission Line Pulse (TLP) technique

One of the major drawbacks represented by the ESD stress methods based on the three basic ESD stress models, i.e. HBM, MM and CDM, is that they usually yield only failure thresholds and do not provide a sufficiently detailed knowledge of the DUT (Device Under Test) behavior. Furthermore, DC characterization of electronic devices causes strong self-heating for higher currents and does not provide information on the transient behavior. For these reasons, pulsed characterization techniques are necessary in addition to the DC characterization: these techniques measure dynamic and the quasi-static device behavior. An important tool used to perform ESD testing and pulsed characterization on electronic devices is represented by the ***Transmission Line Pulse (TLP)*** technique. This system provides some interesting advantages over the classical ESD stress methods based on HBM, MM and CDM: first, it is characterized by a very good repeatability of the stress-tests both on the same and on different systems. Moreover, the TLP system permits also to acquire the waveforms of the voltage and current on the DUT during ESD events and give more complete and accurate results.

Because of these interesting characteristics and also to the fact that the TLP system is used in this thesis to carry out ESD characterization of LEDs, in this section we will provide a detailed description of TLP technique: after an initial general description of the system, different implementations will be also presented, including Current Source TLP, Time-Domain Reflectometer TLP, Time-Domain Transmission TLP and Time-Domain Transmission Reflectometer TLP.

3.3.1 Fundamentals of TLP technique

The TLP stress system can generate rectangular pulses of selectable duration and amplitude, by charging the distributed capacitance of a transmission line, that will be subsequently discharged on the DUT. With this system it is also possible to measure the evolution of leakage current after the application of each pulse and the quasi-static current-voltage characteristic. The quasi-static values of the voltage and the current on the DUT are obtained by averaging a certain region in the second half of the transient waveforms, at a time when most of the oscillations

caused by the parasitic capacitance and inductance of the TLP setup should have settled.

A schematic of the TLP pulse generation section is reported in Figure 3.6: a high-voltage source is used to charge the distributed capacitance of a transmission line TL1 via a high-ohmic resistor, while the coaxial switch S is open. After the switch closes, the transmission line TL1 discharges into a load with impedance Z_L (i.e. the DUT) or into a second transmission line TL2, thus producing a square pulse. The duration of the pulse is related to the line length L by the following relation:

$$t_{pulse} = \frac{L}{2v_p} \tag{3.4}$$

where v_p is the velocity of the signal that propagates from the witch to the high-ohmic end of this line and back to the switch. For example, with a transmission line 10 m long and a propagation velocity of 20 cm/ns, the system can generate a 100 ns wide pulse. The amplitude of the voltage pulse V is determined by the pre-charge voltage V_0 and the impedances of the source Z_S and the load Z_L as follow:

$$V = V_0 \frac{Z_L}{Z_L + Z_S} \tag{3.5}$$

Note that if a pulse travel along a transmission line, any discontinuity of the impedance $Z(x) = Z_0$ causes a partial reflection of the energy of the incident pulse. The reflection is of the same polarity as the incident pulse if the impedance difference $Z(x) - Z(x-1)$ is positive and of opposite polarity else.

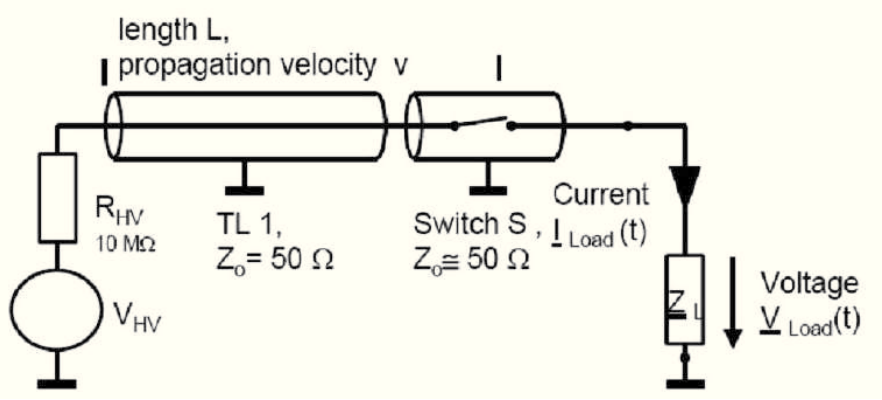


Figure 3.6: Schematic of the TLP pulse generation section.

Deviations from the ideal square shape of the pulse result from resistive and dielectric losses, that are frequency-dependent, and from variations in the impedance along the line through the whole system. For this reason, it is important to employ cables and components that are well matched, as short as necessary, and with low losses. Not that the relay switch is the most critical element of the TLP system.

Thus the necessary equipment for a TLP system is the controller, a high voltage generator, an oscilloscope and a source measuring unit for leakage measurement. The equipment is usually controlled by a software, that also extracts the actual current through the device $I_{DUT}(t)$ and the voltage across it $V_{DUT}(t)$. In the following we will briefly discuss the different implementations of a TLP system.

3.3.2 Current Source TLP

Figure 3.7 illustrates the schematic of a *Current Source TLP*, also referred as TLP500: it is mainly used to simulate HBM-stress by means of a 100 ns wide pulse. This system is characterized by the termination resistor and the source resistor, that forces the current through a low ohmic DUT. Voltage and current waveforms are measured independently by means of the oscilloscope, as close as possible to the DUT. Additional switches disconnect the DUT from the transmission line and connect it to the parameter analyzer for the leakage measurement. High parasitic elements at the DUT slow the achievable dV/dt. The matched termination eliminates multiple reflections between the open end of TL1 and the DUT. The oscilloscope and the probes determine the accuracy, which is nearly independent from the load impedance Z_{DUT}.

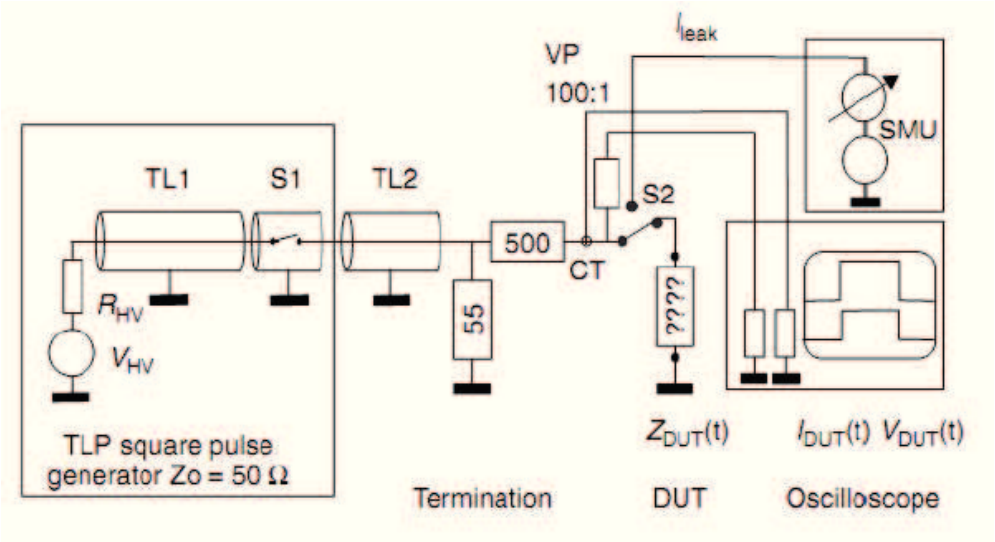


Figure 3.7: Schematic of a Current Source TLP.

3.3.3 Time-Domain Reflectometer TLP (TDR-TLP)

Figure 3.8 shows the schematic of a *Time-Domain Reflectometer TLP (TDR-TLP)*. This system, which is based on the high frequency propagation effects, has the advantage of maintaining the 50 Ω impedance from the generator to the device

with minimum parasitic elements and pulse distortion. The operation of TDR-TLP is based on the principle that if an incident square pulse reaches the DUT at the end of a transmission line, it is reflected depending on the impedance $Z_{DUT}(t)$ of the DUT relative to the impedance Z_0 of the transmission line, according to the following relation:

$$V_{reflected}(t) = \frac{Z_{DUT}\,(t - t_{delay}) - Z_0}{Z_{DUT}\,(t - t_{delay}) + Z_0} \cdot V_{incident}\,(t - t_{delay}) \tag{3.6}$$

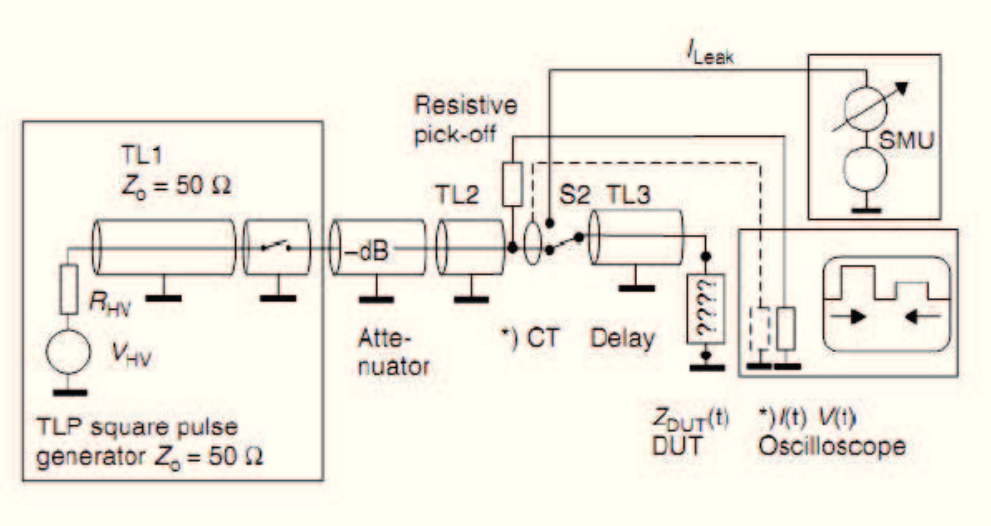


Figure 3.8: Schematic of a Time-Domain Reflectometer TLP (TDR-TLP).

The Time-Domain Reflectometer TLP can be implemented in two different ways, i.e. with or without a current transformer CT in the signal path. In the first case an oscilloscope with two channels is used to measure current and voltage reflected from the DUT independently, with the accuracy provided by the probes and the oscilloscope after a calibration of the attenuation factors of the system. In the other case, i.e. in a system without current transformer, for a known impedance Z_0, the current $I(t)$ can be calculated from the relation $I(t) = V_{incident}/Z_0$ for the incident pulse, and $I(t) = -V_{reflected}/Z_0$ for the reflected one.
Note that the transmission line TL3 shown in Figure 3.8 between the resistive pick-off and the DUT delays the reflected pulse with respect to the incident one. At this point, the voltage $V_{DUT}(t)$ and the current $I_{DUT}(t)$ at the DUT are given by:

$$V_{DUT}(t) = V_{incident}(t) + V_{reflected}\,(t - 2 \cdot t_{delay}) \tag{3.7}$$

$$I_{DUT}(t) = \frac{V_{incident}(t) + V_{reflected}\,(t - 2 \cdot t_{delay})}{Z_0} \tag{3.8}$$

An attenuator between the pulse generator and the DUT is recommended, in order to reduce multiple stress caused by multiple reflections that depend on the

DUT impedance. Finally, a coaxial relay in the delay line allows to disconnect the DUT from the stress line and connect it to a source measuring unit, in order to perform the leakage measurement.

3.3.4 Time-Domain Transmission TLP (TDT-TLP)

The *Time-Domain Transmission TLP (TDT-TLP)*, whose schematic is illustrated in Figure 3.9, avoids the uncertainties associated with the dispersion of the reflected pulse signal. First, a reference voltage pulse $V_{chg}(t)$ must be captured for every voltage step without the DUT in place. The voltage $V_{chg}(t)$ equals the measured voltage $V(t)$ times the attenuation factor a. After this step, the device is inserted in the fixture and the resulting pulses $V_{DUT}(t)$ are captured for the same pre-charge voltage levels.

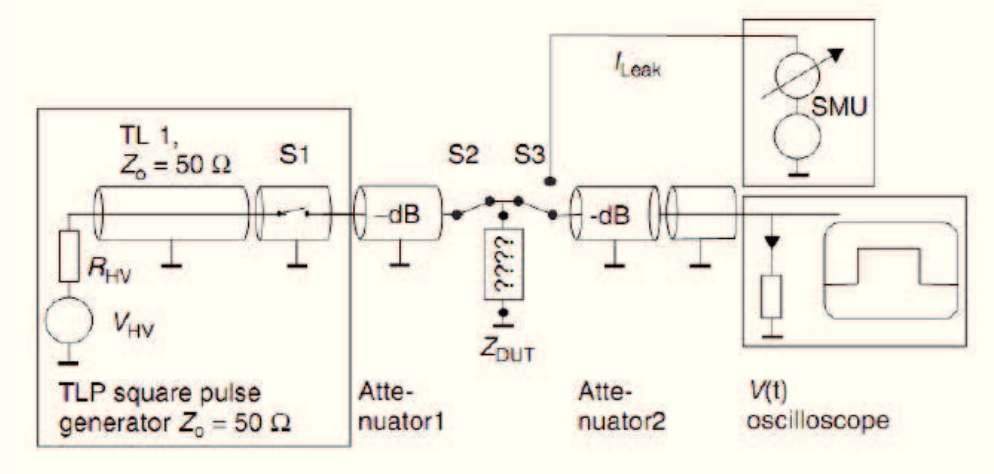


Figure 3.9: Schematic of a Time-Domain Transmission TLP (TDT-TLP).

Also in this case, an attenuator between the pulse source and the DUT is recommended, in order to reduce multiple reflections and stabilize the source impedance Z_0. For the first pulse of a series of decaying reflections, the current through the DUT can be calculated by means of the following equations:

$$Z_{DUT}(t) = \frac{V_{DUT}(t)}{V_{chg}(t) - V_{DUT}(t)} \cdot Z_0 \tag{3.9}$$

$$I_{DUT}(t) = \frac{V_{DUT}(t)}{Z_{DUT}(t)} \tag{3.10}$$

where $V_{DUT}(t)$ is the measured voltage across the DUT, attenuated to an amplitude safe for the oscilloscope.
Finally, note that two relays are necessary in order to isolate the DUT for leakage measurement between stress pulses.

3.3.5 Time-Domain Transmission Reflectometer TLP (TDTR-TLP)

To conclude the overview on different TLP implementations, in Figure 3.10 we report the schematic of a *Time-Domain Transmission Reflectometer TLP (TDTR-TLP)* or *Embedded DUT*: this system embeds the DUT between the center conductors of two transmission lines of equal length and requires a two-channel oscilloscope. The grounded outer conductors of the two lines are connected to each other. In particular, the length of the two lines must be equal, in order to align the transmitted and the reflected signal on the screen of oscilloscope. The length of the delay and termination line should exceed the length of the pulse generating TL1, in order to separate the reflected from the incident pulse at the pick-off.

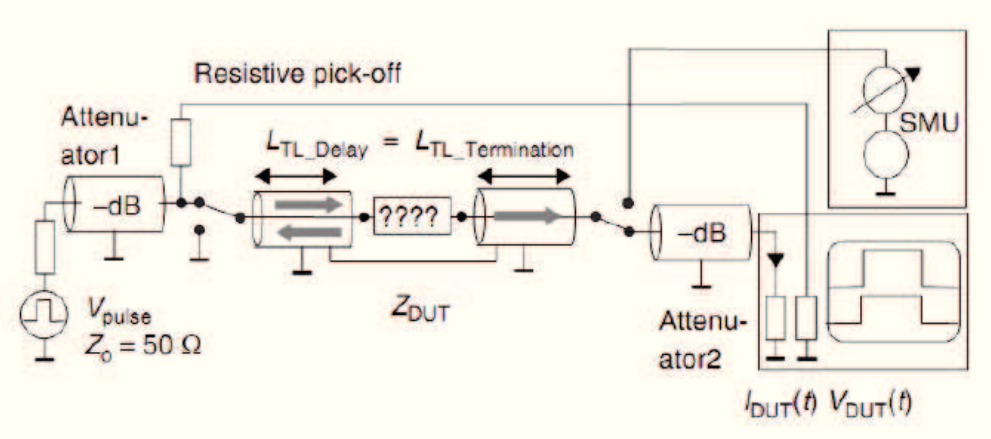


Figure 3.10: Schematic of a Time-Domain Transmission Reflectometer TLP (TDTR-TLP).

The voltage $V_{DUT}(t)$ can be calculated from the reflected pulse, considering the attenuation factor of the pick-off and the transmission lines, as follow:

$$V_{DUT}(t) = a \cdot 2 \cdot V_{reflected}(t) \tag{3.11}$$

On the other hand, the current $I_{DUT}(t)$ can be calculated from the transmitted voltage pulse at the 50 Ω input resistor of the oscilloscope, as follow:

$$I_{DUT}(t) = \frac{V(t)}{Z_0} \tag{3.12}$$

The usage of an attenuator between the pulse generator and the pick-off is recommended. Finally, additional coaxial relays may be necessary, in order to perform the leakage measurement.

3.4 ESD protection strategies on electronic devices

In the previous section we have seen that different phenomena can induce the generation of electrostatic discharges, and this events can permanently damage electronic devices. In particular, also ESD events with very low voltage levels, for example in the order of 100 V, that a person cannot even feel, can easily damage electronic components. Furthermore, it is important to point out that ESD events can give rise not only to catastrophic failures, detectable through inspection, but also to latent damages, that remain unnoticed until the device stops working. Note that latent damages are the most costly, because they cause to device to work for a while for customer applications, before giving unexpected and unexplained failures and consequently more returns, warranty costs and lower customer satisfaction. For these reasons, it is very important to protect electronic devices from ESD. In particular, two types of ESD protection strategies can be identified:

- passive protection strategies: these include ESD control methods, that are employed in the fabrication process and during usage where possible, in order to reduce the probability that an ESD occurs on device;

- active protection strategies: these include all possible protection structures that can be inserted within the single electronic device or into the global system.

In the following we will briefly analyze these two type of ESD protection strategies for electronic devices.

3.4.1 Passive protection strategies

The passive protection strategies to protect devices from ESDs consist in using some control methods to strongly reduce the probabilities of an ESD event occurs. This strategy is particularly effective at a manufacturing stage, where it is possible to modify the environment and the handling procedures.

Different techniques to reduce the risk of damage are employed both during the manufacturing process and in the testing phase, where human handling is commonly required. In general, to avoid ESDs, it is useful to employ static control materials. In fact it is strongly recommended to remove insulator materials from the workplace whenever possible, while dissipative materials are a strongly preferred choice. Furthermore, all conductors must be grounded and, to neutralize charged insulators that cannot be grounded, ionizers are employed. In fact ionizers flood area with ions, thus neutralizing charge. Also dissipative work surfaces and floor mats, that help to bleed off charges quickly and prevent charge accumu-

lation, must be grounded via ground cord to common point ground, as shown in Figure 3.11.

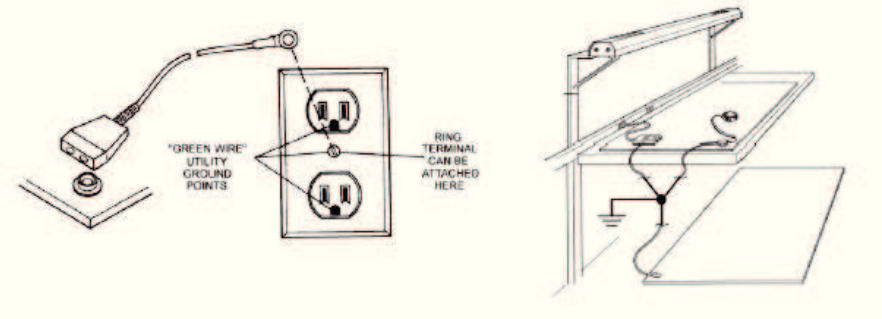


Figure 3.11: Example od ESD preventing policy: grounding of ESD floor materials through connection to common point ground.

Not only conductors, but also workers must be grounded to minimize damage risk. In order to obtain this, people must wear proper clothes, together with wrist straps and/or foot grounders. Examples of some of these solutions are illustrated in Figure 3.12.

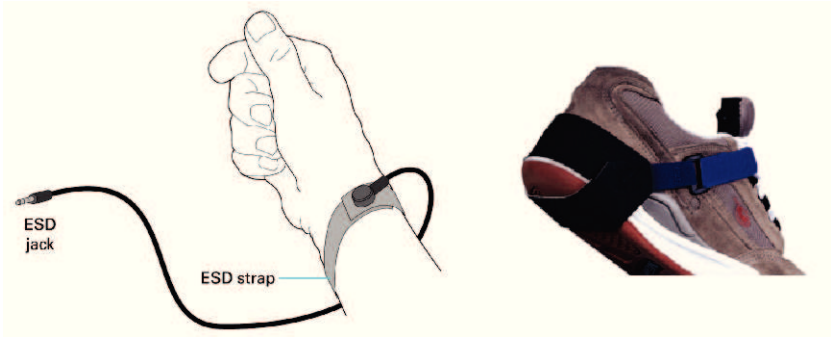


Figure 3.12: Examples of wrist strap and foot grounders typically used as ESD protection by workers.

Finally, it has to be considered that outside protected areas, the probability that an electrostatic discharge happens is higher: for this reason, it is necessary to shield ESD sensitive items through the usage of close metalized shielding bags or conductive boxes.

3.4.2 Active protection strategies

In the previous section we have analyzed some ESD protection strategies that can be used during manufacturing and testing processes. However, during normal operation these solutions are not feasible. Thus, it can be necessary to include some active protection structures within the device or global system.

An active ESD protection structure have to possess some fundamental characteristics, that is:

- it have to clamp the discharge voltage to shunt the stress current, that can be several Amperes for about 100/150 ns;
- the protection device must be very fast: its turn on time has to be lower than 1 ns, in order to be faster than the rise time of the discharge;
- it has to be robustness, to protect the device from numerous pulses;
- the protection circuit must not influence the normal device operation, for example introducing minimum series resistance and capacitance;
- it has to be cheap;
- it must occupy minimum area.

Figure 3.13 shows the schematic of an active ESD protection circuit connected to a CMOS inverter. There are several active ESD protection circuits, depending also on the type of device that has to be protected. However, in this thesis we will not present the different protection circuits for electronic devices, because this work is not aimed to study ESD protection devices. In the next section, when we will recall some previous works on ESD effects on LEDs that can be found in literature, we will briefly show some ESD protection strategies that have been developed specifically for light-emitting diodes.

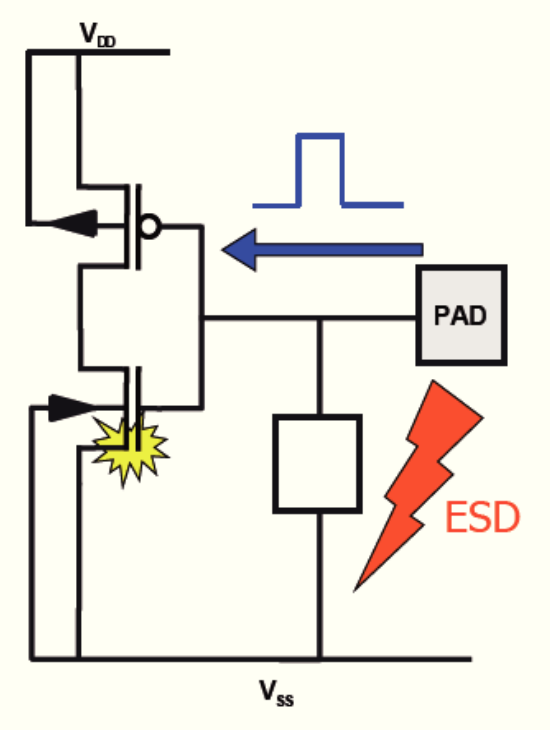


Figure 3.13: Active ESD protection circuit connected to a CMOS inverter.

3.5 Previous works on ESD effects on LEDs

In this chapter we have seen that electrostatic discharges represent a severe issue for the reliability of electronic devices. Also light-emitting diodes (LEDs) suffer particularly the effects of ESD events: these phenomena can induce the catastrophic failure of optoelectronic devices, usually resulting in a short-circuiting of the junction. As a consequence, the device shows an abrupt leakage increase and does not emit light after failure. However, also latent damages are sometimes observed in LEDs: in these cases, the LED can still emit light after the ESD event, before giving unexpected and unexplained failures. Thus, it is clear the importance of studying the effects of ESDs on light-emitting diodes. Wide-bandgap diodes, such as GaN-based diodes, are particularly sensitive to ESD events, due to inherently high values of the shunt parasitic resistor under reverse bias and the high breakdown voltages: for this reason, in the recent years most of research groups and companies have focused on the analysis of ESD effects on GaN-based LEDs.

But despite the importance of this topic, only few works can be found in literature up to now concerning the study of ESD effects on LEDs. On the other hand, many efforts have been done in the recent years by many research groups and companies, in order to increase the ESD robustness of light-emitting diodes. In this section, it will be provided a brief overview on previous works that can be found in literature, concerning the study of ESD effects on LEDs and the different solutions that have been proposed to improve the ESD robustness of optoelectronic devices.

Among the first papers on ESD effects on LEDs, we can identify the works of Meneghesso *et al.* in [93] and [94]. In these works, the authors report the results of ESD testing (HBM and TLP) carried out on commercially available GaN LEDs. In particular they highlight the difference in terms of ESD robustness between LEDs grown both on sapphire substrate and on silicon carbide substrate. The results have demonstrated that a non optimal design of layout leads to current crowding phenomena, thus determining premature failure. In particular, devices grown on SiC, adopting vertical current flow, and optimized layout and technology, achieved maximum ESD robustness in excess of 8 kV HBM, 5 A TLP. Also the role of resistive current paths in focusing the flow of charge and the voltage peaks under both DC and transient conditions is then considered, by means of simple considerations on a distributed network of elementary diodes and resistors representing the main electrical features of the LED structure. Other interesting results have been provided in [93]. In fact, it has been shown that in LEDs grown on sapphire, damages are usually localized along the border of the semitransparent metal, towards the n^+ contact, as shown in Figure 3.14. In particular, the damages observed after negative ESD stresses are much larger if compared with those under

positive ESD tests, due to the much higher power dissipated during negative stress. Furthermore, failure analysis carried out on the devices that presented premature fails under reverse stress, has revealed that the damages are no longer localized at the border of the semitransparent metal, but are randomly distributed along the surface of the LEDs.

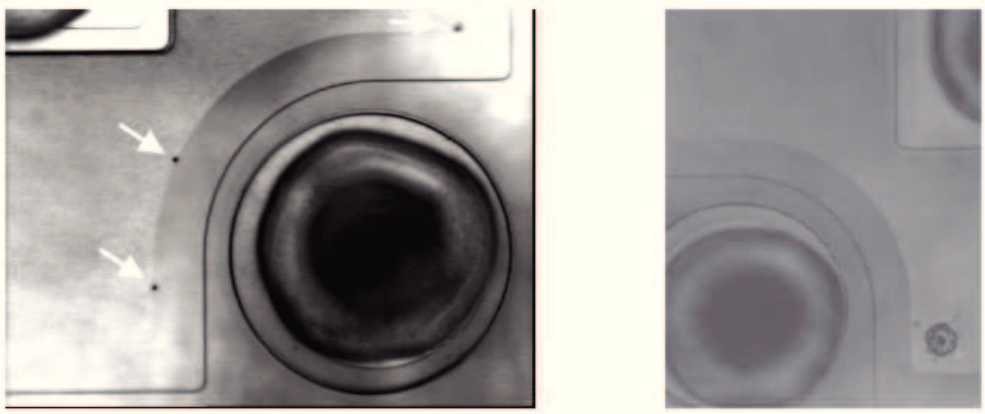


Figure 3.14: (Left) Optical micrograph of a LED failed after forward TLP test and (right) SEM micrograph of a device failed after reverse TLP test. The data are referred to LEDs analyzed in [93].

Another interesting work is that of Meneghini *et al.* reported in [95], which reports an extensive analysis of the degradation of InGaN-based LEDs submitted to electrostatic discharge events, by means of a TLP system. They observed that after ESD failure, LEDs behave as short circuits: ESD damage interests a localized region, as shown in Figure 3.15. In particular, they also noticed that in most of cases, damaged region is located in correspondence of one of the leakage paths identified by emission microscopy, thus suggesting that leakage paths responsible for leakage current conduction constitute weak points with respect to ESD events, since they allow an extremely high current to flow through a small-size path.

Results reported in [95] indicate also that even reverse TLP pulses with a current smaller than the failure threshold can modify the electrical characteristics of the LEDs, inducing a decrease in the leakage current: this effect, also shown in Figure 3.16, can be attributed to a partial annihilation of the leakage paths, due to the extremely high current densities injected through them.

Similar results to those reported in [95] have been obtained by Meneghini *et al.* also in [96]. In addition, in this work also a decrease in the reverse bias luminescence and the annihilation of some of the luminescent spots have been observed by EMMI measurements, thus confirming the hypothesis that ESD events with a current smaller than the failure threshold can annihilate some leakage paths.

Su *et al.* in [97] have analyzed GaN-based LEDs with *p*-cap layers grown at various temperatures. They have demonstrated that the ESD characteristics of

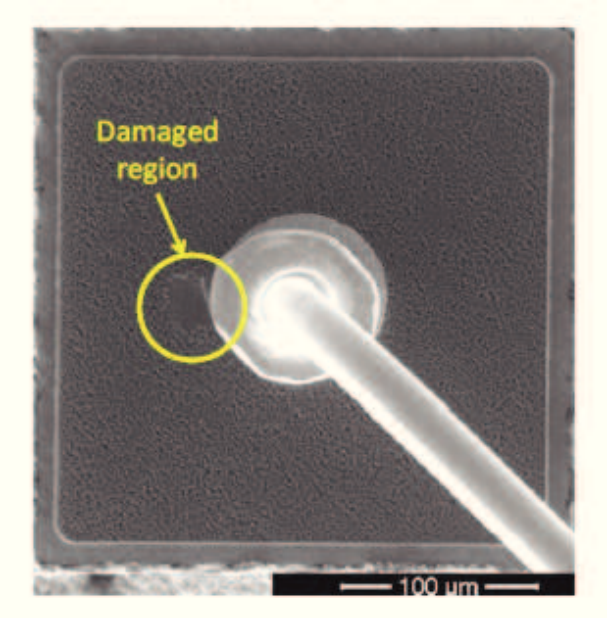


Figure 3.15: SEM image of a LED after ESD failure, showing the damaged region [95].

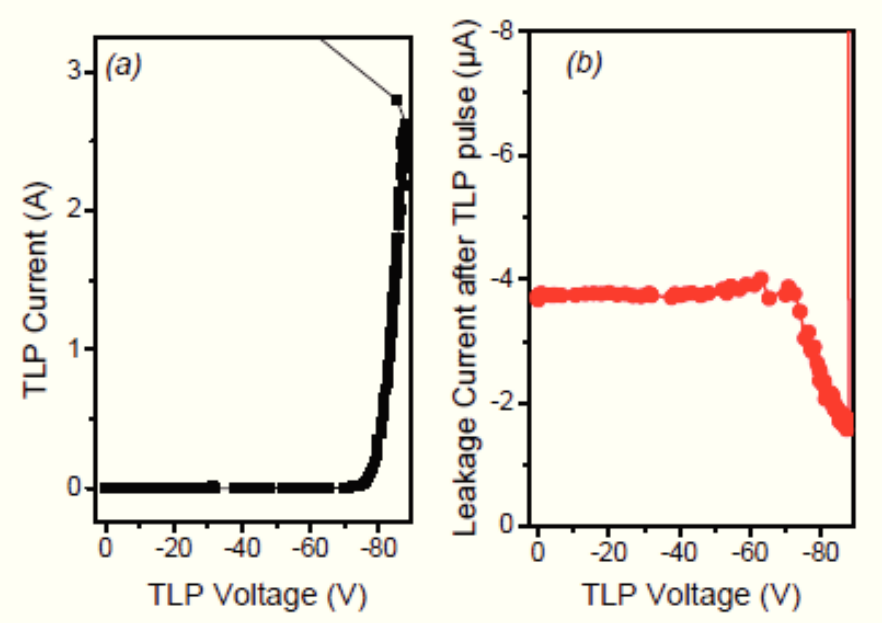


Figure 3.16: *(a) I-V* characteristic of one of the analyzed LEDs in [95], measured by the TLP system, and *(b)* leakage current evolution measured during TLP test, showing the decrase in the leakage current induced by reverse TLP pulses smaller than the failure threshold.

GaN-based LEDs could be significantly improved by raising the *p*-cap growth temperature from 900 °*C* to 1040 °*C*. In fact, LEDs with 900 °*C*-grown *p*-cap layer could only endure negative 1100 V electrostatic discharge (ESD) pulses, while LEDs with 1040 °*C*-grown *p*-cap layer could endure ESD pulses as high as negative 3500

V. Furthermore, from TEM micrograph it has been noticed that in p-GaN layer grown at 900 $°C$ there exist a large number of defects. In particular, as shown in Figure 3.17, these defects are V-shaped with a threading dislocation connected at the bottom, thus suggesting that ESD performances of LEDs were limited by the presence of V-defects.

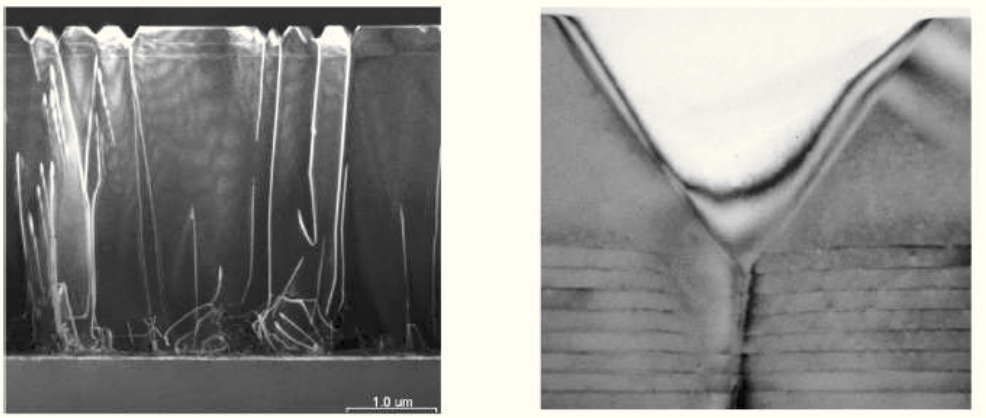


Figure 3.17: (a) TEM micrograph of a GaN-based LED with p-cap layer grown at 900 $°C$ and (b) enlarged image of the same sample, showing a V-defect [97].

In [98] Jang *et al.* have reported a study concerning GaN-based light-emitting diodes (LEDs) with p-type AlGaN electron blocking layers (EBLs) of different thicknesses, revealing that the LEDs could endure higher electrostatic discharge (ESD) levels as the thickness of the AlGaN EBL is increased. In particular, they attributed this improvement to the fact that a p-AlGaN EBL with higher thickness may partly fill the dislocation-related pits that occur on the surface of the InGaN-GaN multiple-quantum well (MQW) and that are due to the strain and the low-temperature-growth process. The results of this study show that the ESD endurance voltages could increase from 1500 to 6000 V when the thickness of the p-AlGaN EBL in the GaN LEDs is increased from 32.5 to 130 nm.

Tsai *et al.* in [99] have presented a study carried out on GaN-based LEDs with naturally textured surface grown by metal-organic chemical vapor deposition. In their experiment, a high-temperature-grown (HTG) p-GaN layer was inserted between the p-AlGaN electron-blocking layer and the LTG p-GaN contact layer, in order to suppress pit-related threading dislocations (TDs), that may intersect the underlying active layer. The results of this experiment show that GaN-based LEDs with the HTG p-GaN insertion layer can effectively endure negative electrostatic discharge voltage of up to 7000 V.

Finally, we can remember the interesting work of Jeon *et al.* reported in [100]. In this work the electrostatic discharge properties of InGaN-light emitting diodes were investigated in terms of the internal capacitance of the InGaN-LED, showing that LEDs with higher internal capacitance are typically more resistant to external

ESD impulses.

3.5.1 ESD protection strategies on LEDs

In the recent years several design solutions have been proposed, in order to increase the ESD robustness of light-emitting diodes, even though the knowledge of physical mechanisms that limit the ESD robustness of devices was quite poor. The research has been focused particularly on GaN-based LEDs, due to their large usage in a number of applications. In the following we will present an overview of the most interesting ESD protection strategies developed on light-emitting diodes.

The actually most used solution to protect LEDs from ESD events is the employment of a internal inverse-parallel protection diode, as shown in Figure 3.18: by means of this structure, a negative ESD-induced pulse current is expected to flow through the protection diode without damaging the major LED. Different implementations of this solution can be found in literature. In [20] an internal GaN *pn* junction diode was built, obtaining an increase in the ESD failure threshold under reverse bias from 300-400 to 2000 V.

Alternatively, Chang *et al.* in [25] have proposed GaN flip-chip power light-emitting diodes with metal-oxide-silicon submount. In particular, two different configurations have been proposed: a diode submount and a MOS submount connected to the flip-chip power LED in a reverse parallel way to achieve anti-ESD efficacy. In both cases an increased ESD robustness was observed.

On the other hand, in [21] have been employed GaN schottky diodes as protection devices: they were built internally inside the GaN green LEDs by using etching and redeposition techniques. Similar solutions have been proposed also in [22] and [23]. However, it is clear that these solutions can protect LEDs only from reverse discharges: this choice is related to the fact that the energy dissipated during reverse ESD events is much higher than the energy dissipated during forward ESD events, thus suggesting that reverse discharges are more damaging than forward discharges [34].

Other ESD protection circuits can consist of a series of Si diodes, one Si Zener diode, or two Si Zener diodes, as shown in Figure 3.19. Note that the last solution, which is a common solution in commercial devices, offers protection from both reverse and forward discharges [101] [102]. Using one or two Zener diodes, or placing several Si diodes in series, the threshold voltage of the ESD circuit increases to values beyond the turn-on voltage of the LED. Thus, under normal operating condition, the current flowing through the ESD circuit is negligible [34].

Another interesting solution to protect LEDs from ESD events was proposed by Chiang *et al.* in [26]. The authors have found that a thicker n^--GaN current spreading layer could spread the surge current in the lateral directions more

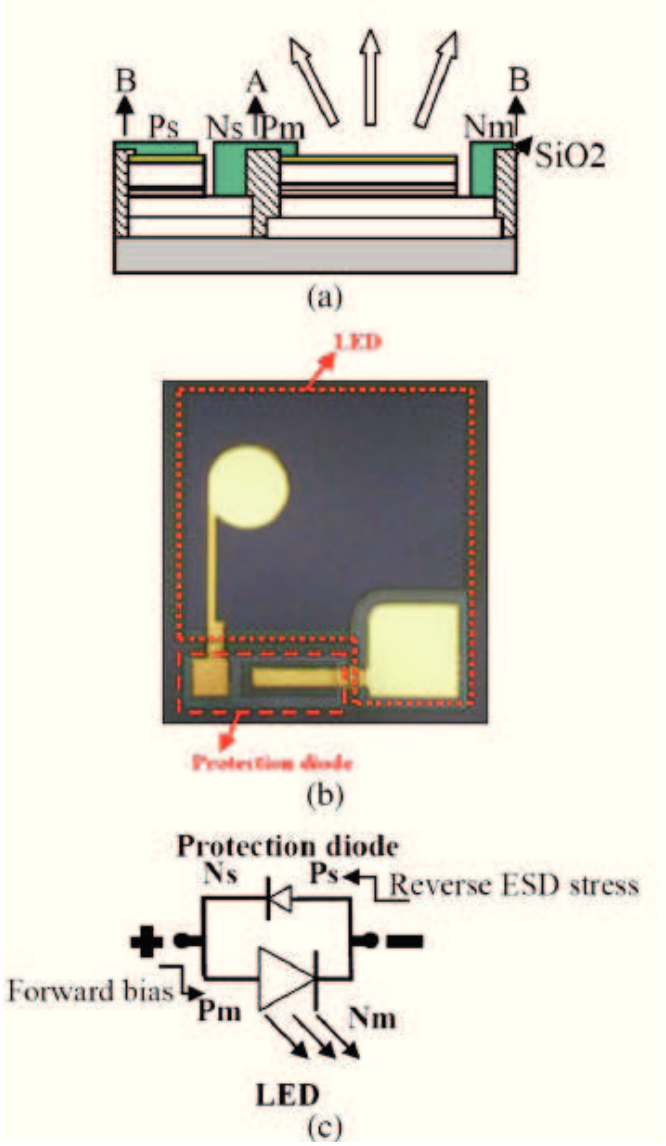


Figure 3.18: GaN-based LED grown on sapphire substrate, with an internal inverse-parallel protection diode [23].

effectively, thus improving the ESD characteristics of devices.

Also CMOS ESD protection circuits have been sometimes employed: an example is represented by [103]. An alternative solution was proposed by Hwang and Shim in [24], in which they have obtained an improvement of the electrostatic discharge voltage in an InGaN/GaN blue light emitting diode grown on sapphire substrate by inserting a floating metal ring near the n-electrode, as shown in Figure 3.20. In particular, they believe that the improvement in ESD voltage resulted from the reduction of the intensity of electric field peak in the pn junction near the metal electrodes, caused by the electrostatic induction phenomenon due to the floating metal.

To conclude, we can remember the interesting solution proposed by Park *et al.*

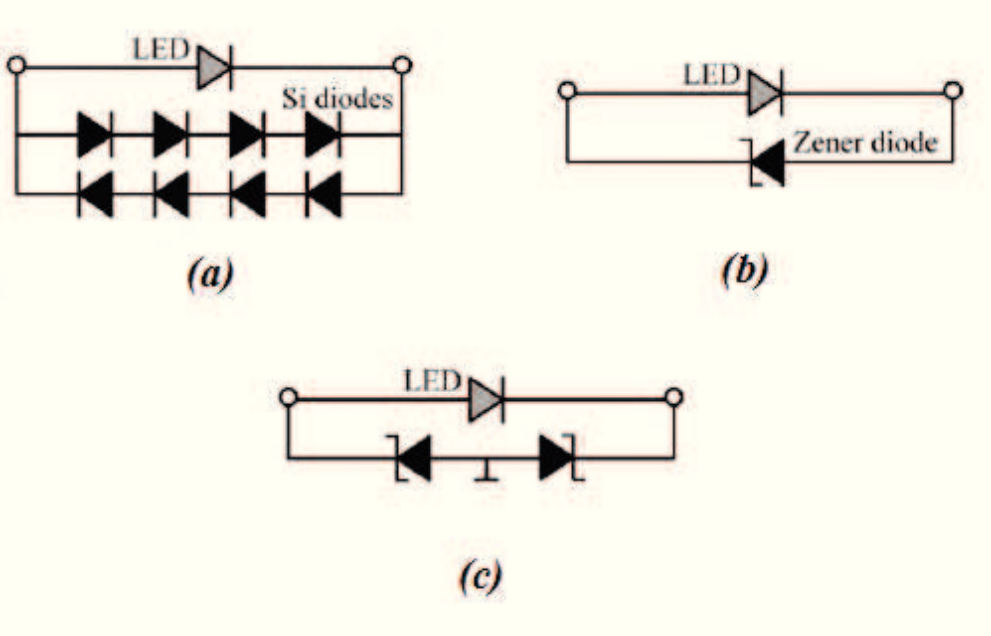


Figure 3.19: ESD protection circuits for LEDs, using (a) multiple Si diodes, (b) one Zener diode and (c) two Zener diodes.

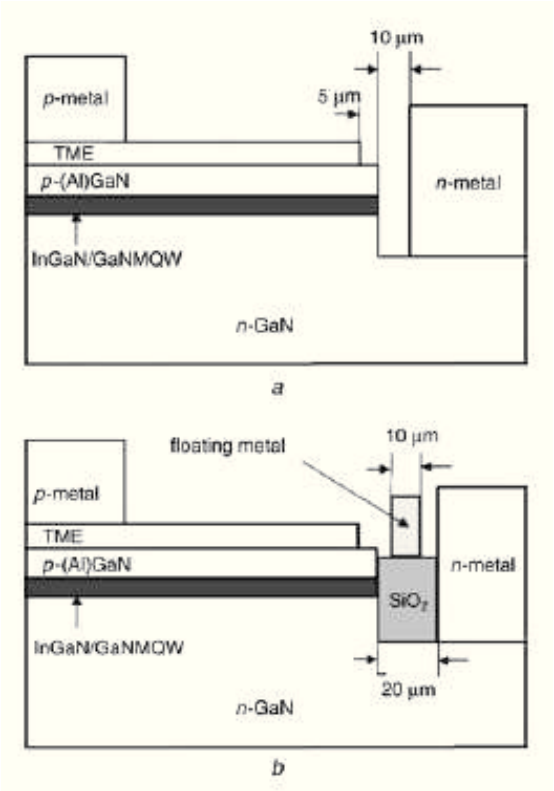


Figure 3.20: Cross sectional schematic views of a LED (a) without floating metal ring and (b) with a floating metal ring near the n-electrode [24].

in [27]. In this work, to improve the ESD robustness of GaN LEDs, an air gap was introduced as an ESD protection structure in an Al film on the bottom side of a

sapphire substrate, as illustrated in Figure 3.21. In particular, it has been shown that the negative-voltage ESD characteristic of GaN LEDs with an air gap was remarkably improved from -0.3 to -4 kV. The degradation of electroluminescent intensity of GaN LEDs, which was caused by ESD stress, was also suppressed by an air gap in GaN LEDs. An ESD-stress-induced current is believed to flow in an air gap to protect the multiquantum well of GaN LEDs.

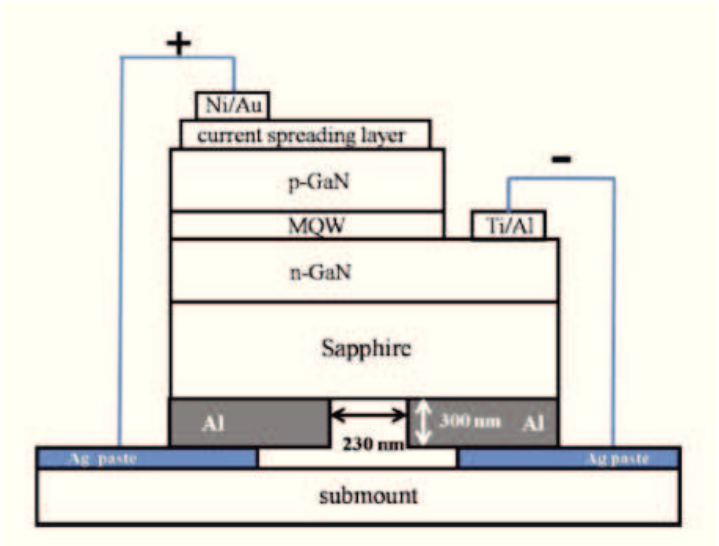


Figure 3.21: Cross sectional view of a LED structure with an air gap on the bottom side of the sapphire substrate [27].

Chapter 4

Analysis of defect-related localized emission processes in GaN-based LEDs

With this chapter we introduce the second part of this thesis, where the principal experimental results obtained from the research activity will be presented. In particular, in this chapter the effects of defects on electrical and optical properties of GaN-based LEDs will be analyzed: the study was focused on this class of devices, because, as it has been explained in chapter 1, gallium nitride and its alloys, such as InGaN, are characterized by a high defectiveness, mainly due to the lack of a ideal substrate for growth. This topic is of fundamental importance also to better understand the role of defects in limiting the reliability and the ESD robustness of LEDs, that will be discussed in the next chapters. As mentioned in the introduction of thesis, in the last years some preliminary reports have suggested that localized defects can be responsible for reverse leakage conduction and spectral inhomogenities under forward-bias conditions. However, no extensive analysis can be found in literature up to now, concerning the role of defects in influencing the optical properties of LEDs, both under reverse and under forward bias conditions.

The aim of this work is to achieve a better understanding of the luminescence processes related to localized defects in GaN-based LEDs. To obtain this, an extensive characterization of localized conduction and emission processes has been carried out. The analysis was based on combined electrical and optical measurements. In particular, optical characterization includes spatially and spectrally resolved electroluminescence (EL) and photoluminescence (PL) measurements. After an initial description of analyzed devices and experimental setups employed for this analysis, the results of emission processes observable under reverse bias, will be presented. Afterwards, the results obtained from analysis of defect-related emission processes occurring under low-forward bias conditions, will be presented. Finally,

a possible interpretation of defect-assisted radiative recombination processes occurring under low-forward bias condition is provided.

4.1 Analyzed LEDs and experimental details

The analysis was carried out on blue and green GaN-based LEDs with multiquantum well structure (MQW), grown by metal-organic chemical vapor deposition (MOCVD) on a sapphire substrate. The details of layered structure of devices is not known.

Blue LEDs have been provided by manufacturer as on-wafer chips. These samples are characterized by an emission wavelength of about 465 nm and an area of $120 \times 120\,\mu m^2$. In particular, blue LEDs with different threading dislocation densities (TDDs), of respectively $3 \cdot 10^8\ cm^{-2}$ and $8 \cdot 10^9\ cm^{-2}$, have been grown, in order to study the correlation between localized conduction and emission processes under reverse bias and structural defects. The dislocation density of this samples was determined by atomic force microscopy (AFM). In particular, before the growth of LED structures, GaN templates with high and low dislocation density respectively, have been grown as test samples. After that, the surface of these samples was treated using silane, in order to highlight pits, which are associated with the surface termination of dislocations. At this point, the pit density was counted, thus determining the dislocation density of each sample. Also several AFM images were taken to improve the statistical accuracy.
On the other hand, analyzed green LEDs have an emission wavelength of about 540 nm and an area of $290 \times 290\,\mu m^2$. Differently from blue LEDs, green chips were first removed from the sapphire substrate and then they were mounted on a metallic TO18 package using an epoxy glue. Note that with such a type of mounting, a vertical current flow can be obtained from these devices.

Both blue and green LEDs have been characterized by means of current-voltage (I-V) and spatially and spectrally resolved electroluminescence (EL) measurements. Furthermore, green LEDs were submitted also to photoluminescence (PL) measurements. Also electrical and optical characterization at different temperature levels have been carried out on analyzed samples: to do this, LEDs were placed on a thermally controlled stage in the dark, in order to adjust the sample temperature and to limit the influence of environmental light on experimental results.

Current-voltage (I-V) measurements were carried out by means of a HP4155 Semiconductor Parameter Analyzer. In particular, LEDs were placed in a test fixture directly connected to the instrument and the measurements were carried out in the dark, in order to limit the photogeneration induced by environmental light. The LEDs were measured both under reverse and under forward bias: in

particular, the forward current was limited to the value of 100 mA. Due to this relatively low current limit, it has been sufficient to employ a two-wire configuration for the connection between LED and the parameter analyzer.

The experimental setup for spatially and spectrally resolved electroluminescence (EL) measurements is based on an *Andor LUCA* cooled back-illuminated charge coupled device (CCD) camera, a monochromator, and a *Mitutoyo* optical microscope with long-working distance lenses. In particular, by means of the monochromator it is possible to acquire images relative to the emission at a specific wavelength. The system was calibrated in the 400 to 720 nm range using a halogen light source with known spectrum. The device under test is biased by means of a *SourceMeter Keithley 2536A*. Finally, by means of a GPIB connection between instruments and the PC, and a *Labview* program, the experimental procedure can be automatically performed. A schematic of EL experimental setup employed for this analysis is shown in Figure 4.1. Note that using this experimental setup, it

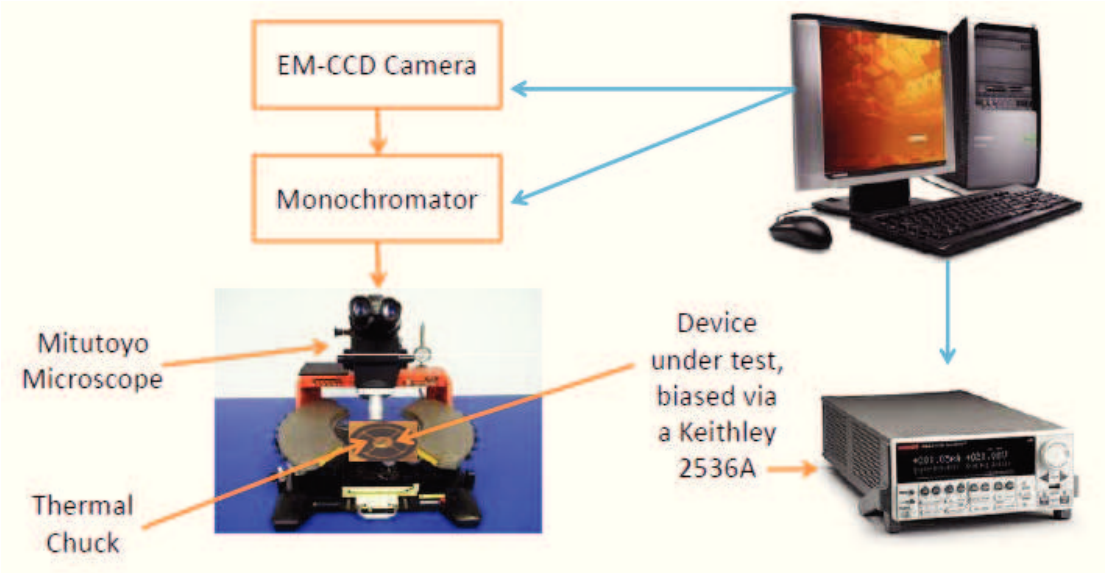


Figure 4.1: Schematic of experimental setup used to carry out electroluminescence (*EL*) measurements on analyzed devices.

is possible to measure the luminescence spectrum emitted from each point of the LED surface, thereby evaluating spectral variations over the device area. The spectral resolution of this system is 1 nm, while the spatial resolution depends on the optics used in the microscope. In particular, with a 50× lens, and the adopted collimating optics, a spatial resolution of approximately 1 μm is obtained.

Also spatially and spectrally resolved photoluminescence (*PL*) measurements were carried out by means of the same experimental setup used for EL characterization and represented in Figure 4.1, except for the fact that in this case a constant voltage level of 0 V is applied to the device under test, by means of the *SourceMeter Keithley 2536A*, and the photoexcitation of carriers within the LED structure is

obtained using a high-power LED emitting at 365 nm. In particular, light emitted from this LED was filtered by means of a bandpass filter with a bandwidth of 10 nm, which is centered at 365 nm. Finally, the excitation light was focused on the sample under test and the spatial uniformity of the beam was verified by optical microscopy.

4.2 Localized emission under reverse bias

The analysis of defect-related localized emission processes under reverse bias was carried out on blue LEDs with different threading dislocation densities (TDDs). The results of spatially and spectrally resolved electroluminescence measurements have shown that LEDs can emit a weak luminescence signal even under reverse bias conditions. Evidence of this phenomenon has been already observed in [104], where it has been attributed to the presence of structural defects, however without providing a direct indication of the role of dislocations in determining these emission processes. With this work, we study in more detail the correlation between EL signal under reverse bias and the presence of threading dislocations in the semiconductor material.

Also the relation between EL intensity and injected current under reverse bias

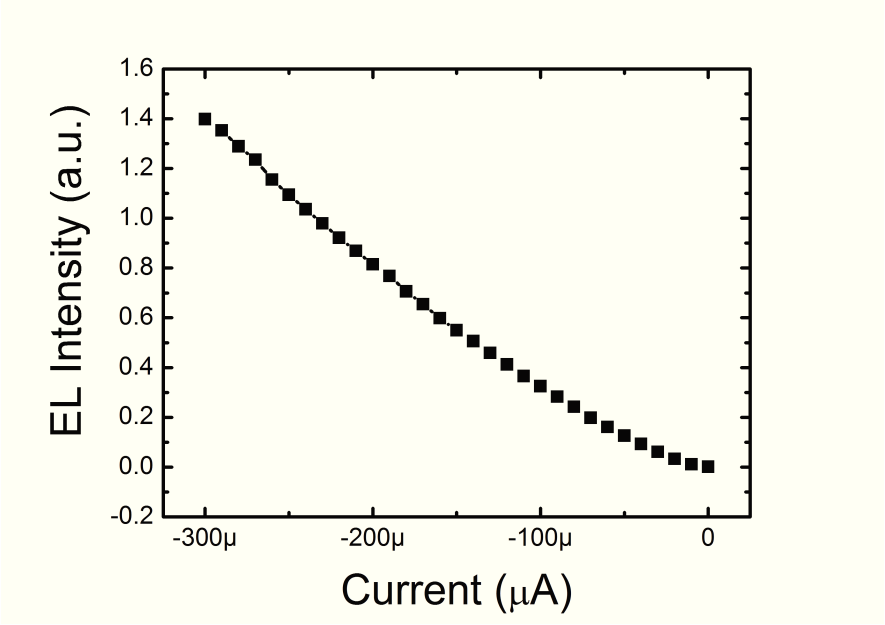


Figure 4.2: Relation between the intensity of EL signal under reverse bias and the injected reverse current for one of the analyzed LEDs.

has been studied and the result obtained from a representative sample is reported in Figure 4.2: as it can be observed, the intensity of reverse-bias luminescence is directly proportional to the injected reverse current, thus suggesting that lumines-

cence originates from the injection of carriers through preferential leakage paths. However, from the same figure it can be noticed that this proportionality is not verified at very low reverse current levels: this can be explained by the fact that surface conduction may become dominant with respect to the conduction through the junction in this operating regime. Note that the EL intensity has been obtained by integrating the EL spectra measured at each current level, by means of the experimental setup for electroluminescence measurements described above.

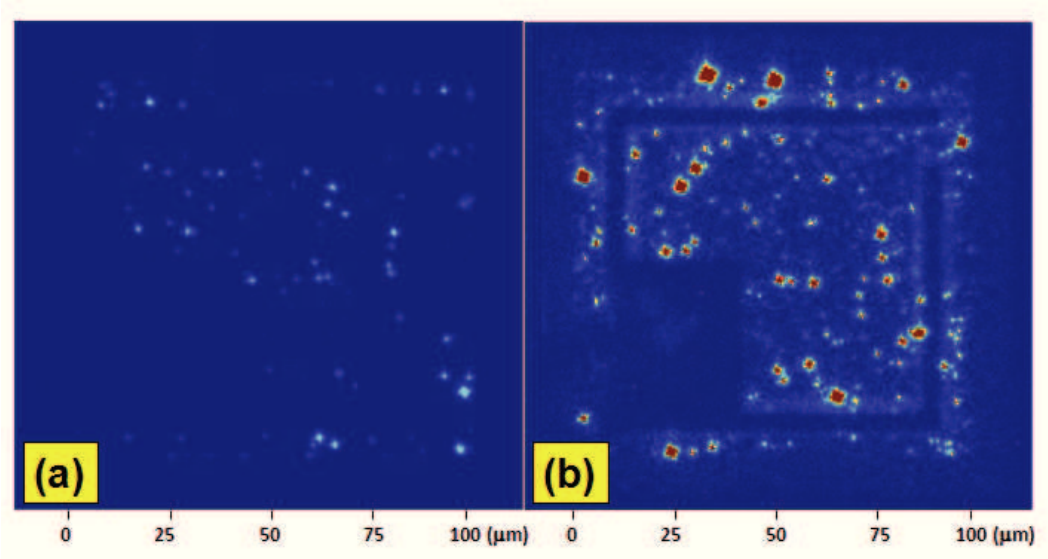


Figure 4.3: Spatially resolved EL image of a representative blue LED with a dislocation density of (a) $3 \cdot 10^8$ cm^{-2} and (b) $8 \cdot 10^9$ cm^{-2}, respectively. The emission were measured at -11 V. Note that the same integration time and false-color scale are used for both EL images.

A comparison between spatially resolved EL images, taken under reverse bias, of blue LEDs with low and high threading dislocation densities ($3 \cdot 10^8$ cm^{-2} and $8 \cdot 10^9$ cm^{-2}, respectively) is reported in Figures 4.3(a) and (b), respectively. These false-color images are referred to reverse-bias luminescence measured at -11 V. In particular, the measurements have been carried out with the same exposure time and the images are plotted with the same false-color scale, in order to obtain a consistent comparison. Some interesting results have been obtained from these figures: first, it can be noticed that reverse bias luminescence is localized in sumicrometer-size spots; in particular these luminescence spots identify the position of preferential leakage paths for injection of carriers under reverse bias. Second, the comparison between images indicates that the number and intensity of luminescence dots is strongly dependent on the threading dislocation density, thus suggesting that threading dislocations act as efficient paths for reverse current conduction and luminescence. This fact is further confirmed by the analysis of current-voltage (I-V) characteristics measured under reverse bias and shown in Figure 4.4, which

are referred to two samples with different threading dislocation density, previously submitted to EL characterization. As it is clear from the image, current has a power-law dependence on voltage, i.e. $I \propto V^k$, with $4 < k < 5$: this relation is typical for soft-breakdown conduction through structural defects [6] [105]. Furthermore, it can be noticed that the ratio between the two I-V curves of Figure 4.4 has the same order of magnitude as the ratio between the threading dislocation densities of analyzed devices, thus further confirming that threading dislocations are preferential paths for leakage current conduction under reverse bias.

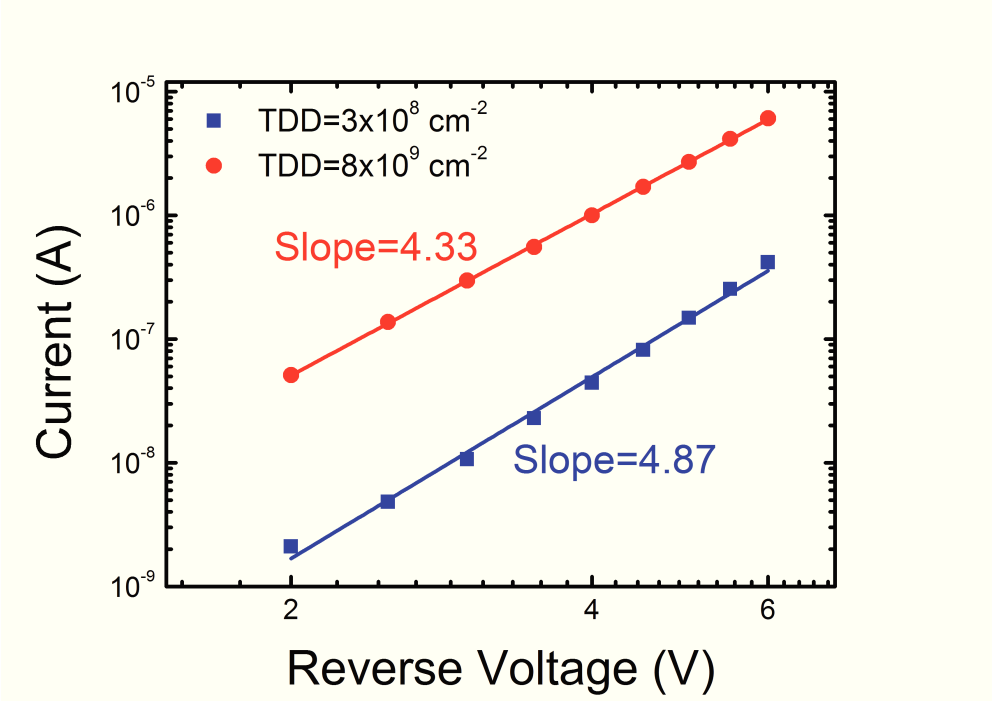


Figure 4.4: Current-voltage (I-V) characteristics, measured under reverse bias, of blue LEDs with different threading dislocation densities. Note that the curves are plotted on a log-log scale.

Thus, from the results reported above, it has been seen that light-emission measurements under reverse bias can be used to identify the position of preferential paths responsible for leakage current conduction. In particular, it has been also demonstrated that reverse current conduction occurs in proximity of threading dislocations. To conclude the study of emission processes occurring under reverse bias, also the EL spectra of LEDs have been analyzed. A comparison between the EL spectrum obtained under forward and reverse bias on a representative green LED is reported in Figure 4.5: the spectrally resolved EL measurements show that reverse bias emission has a broad visible spectrum centered at about 480 nm, thus indicating that light emission occurs in the quantum-well region, due to the recombination of carriers injected owing to the presence of structural defects. The higher spectral width under reverse bias with respect to that under forward bias, is

related to the fact that in this conditions recombination occurs through structural defects with different energy levels localized within the bandgap, thus resulting in the emission of photons with quite different energies. Furthermore, the emission peak is slightly blue-shifted with respect to the forward bias EL peak, due to the fact that the important piezoelectric fields, generated by the growth on c-plane of LEDs, can be significantly compensated at high reverse bias [106].

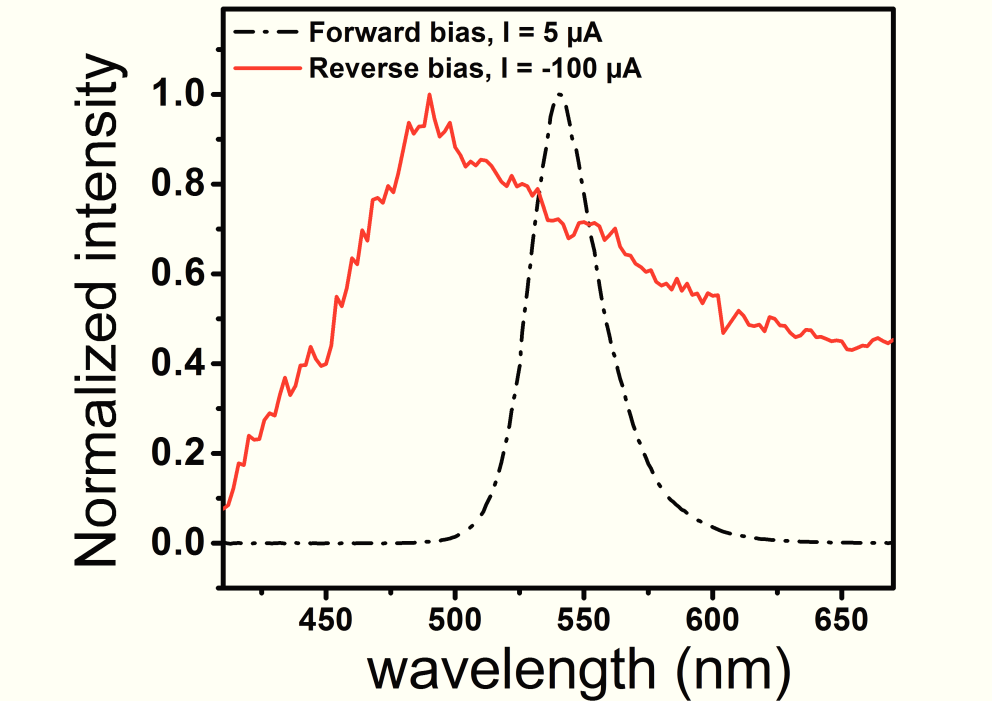


Figure 4.5: El spectra measured under forward and reverse bias conditions, on one of the analyzed green LEDs.

4.3 Localized emission under low forward bias

The analysis of defect-related localized emission processes occurring under low forward bias conditions, was performed on green LEDs. Spectrally and spatially resolved EL measurements carried out in this operating regime, have indicated that the distribution of luminescence on the LED surface can show significant fluctuations, both in terms of spectrum and intensity.

The analysis was first focused on EL characterization of devices. Figure 4.6(a) reports the false-color image of the EL emission of a representative green LED. In particular, the image was taken with the monochromator set to 540 nm and biasing the device with a current density level of 140 $\mu A/cm^2$, which corresponds a current of 120 nA for these LEDs, having an area of 290 $\times$ 290 μm^2: thus, the emission observable in the figure corresponds to the peak of luminescence with

the device biased in the low forward voltage region. As it can be noticed, the intensity of emission shows important fluctuations over the whole device area: the origin of this phenomenon will be discussed in the following, when also PL characterization will be presented. On the other hand, in Figure 4.6(b) is shown

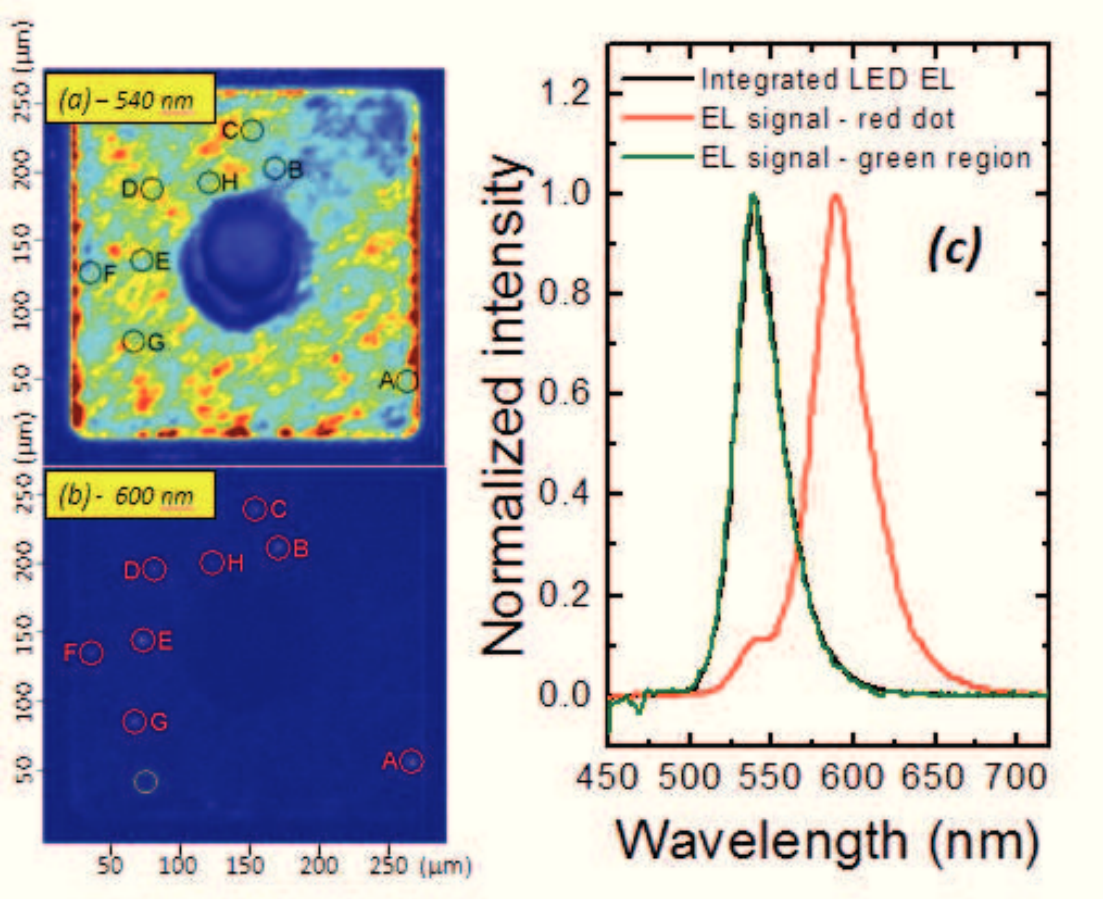


Figure 4.6: False-color emission images obtained from spatially resolved EL measurements carried out on one of the analyzed green LEDs. The images show the emission at (a) 540 nm and (b) 600 nm, respectively. (c) EL spectrum measured on the whole device area, in proximity of dot E [see (a)], and in a green-emitting region [denoted in (b) with the green circle], respectively.

a false-color image of the emission taken from the same device and at the same measuring current level, but in this case with the monochromator set at 600 nm: this image thus refers to the emission from LED in the yellow spectral region, under low forward bias conditions. It is interesting to observe that in this operating regime, the green LED shows localized yellow emitting dots with submicrometer size, that for clarity have been highlighted with circles and labeled with capital letters in Figure 4.6(b). Note that the density of these dots is low, compared with typical values for the threading dislocation density of GaN-based LEDs, and it can significantly vary from wafer to wafer, depending on fabrication processes: thus the origin of these dots in principle cannot be attributed to the presence of threading

dislocations, as it has been observed for reverse bias luminescence. Moreover, from the comparison between EL images of Figures 4.6(a) and (b), it can be noticed that yellow luminescent dots do not correspond to any particular feature recognizable in the green spectral region (note that the position of yellow dots have been indicated also in Figures 4.6(a), referred to the peak of device luminescence, with circles and capital letters).

To better understand the yellow luminescence process, also the EL spectra of these spots have been analyzed. The results of this analysis are reported in Figures 4.6(c), which shows the EL spectrum emitted by the whole LED surface, from dot "E" and from a green-emitting region, denoted with a green circle in Figure 4.6(b), respectively. In order to permit an efficient comparison, these spectra have been normalized to their maxima. From the figure, it can clearly noticed that the luminescence from dot "E" is significantly shifted with respect to the main device emission: in fact, this yellow spot shows an EL spectrum with a peak centered at about 600 nm, and only a small shoulder at 540 nm, i.e. in correspondence of the main LED emission peak. Note also that all other yellow emitting dots labeled in figure have a very similar luminescence spectrum, with the main emission centered at about 600 nm and a green shoulder. In particular, the relative intensity of yellow and green peaks varies for the different dots. On the other hand, the EL spectrum emitted from green-emitting region, denoted in Figure 4.6(b) with a green circle, has the same shape as the integrated device emission, centered at about 540 nm, indicating a good spectral uniformity of green luminescence.

In order to obtain more information on the nature of yellow luminescence observed on green LEDs, also photoluminescence (PL) characterization was carried out on these devices. The results of spatially resolved PL measurements are reported in Figure 4.7. In particular, Figure 4.7(a) shows a false-color image of the PL signal of a green LED taken with the monochromator set to 540 nm, while Figure 4.7(b) reports the distribution of PL signal from the same device, obtained with the monochromator set at 600 nm. In order to obtain a consistent comparison, similar excitation levels were used for both EL and PL measurements. Thus, the excitation level for PL measurements was tuned in order to let the integrated PL spectrum have the same peak level as that of the integrated EL spectrum measured at a current level of 120 nA (i.e. the current level used to obtain the EL images of Figure 4.6). As a result, an excitation power density of 50 mW/cm^2 was used in this case for PL measurements. Moreover, because the emission wavelength of excitation LED is 365 nm, as described in section 4.1, carriers are generated only within the quantum wells and not in the barrier layers.

As it can be noticed from the photoluminescence image of Figure 4.7(a), the PL signal taken at 540 nm, i.e. around the green emission peak, does not show

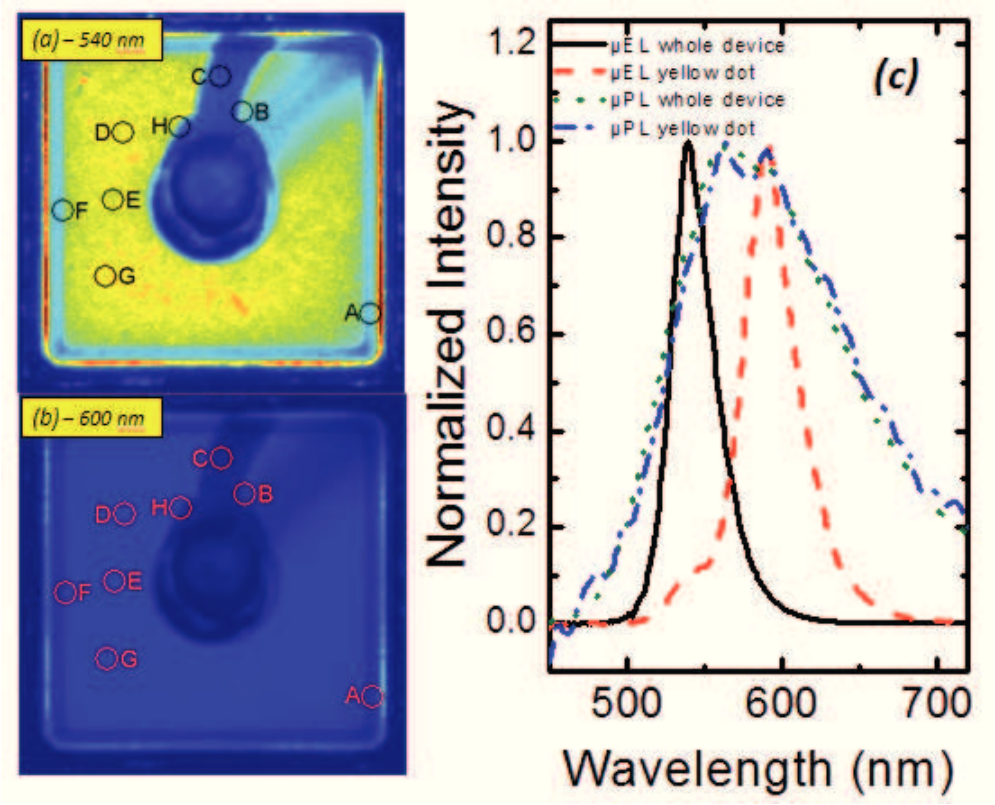


Figure 4.7: False-color emission images obtained from spatially resolved PL measurements carried out on one of the analyzed green LEDs. The images were taken at (a) 540 nm and (b) 600 nm, respectively. (c) EL and PL spectra measured on the whole device area and in proximity of yellow luminescent dot "E" [see (a)].

the strong intensity fluctuations observable in the corresponding EL image of Figure 4.6(a). This fact suggests that the intensity fluctuations detected from spatially resolved EL measurements in the green spectral region are not related to variations of the thickness or composition of the quantum well, but rather to locally lower acceptor concentration in *p*-GaN, as suggested in [107]. In particular, the lower acceptor concentration may determine local variations of the potential barrier for carrier injection or of the resistivity of semiconductor material at the *p*-side, thus locally varying the optical efficiency of LED. On the other hand, by optical excitation, carriers are independently generated from injection processes and therefore with a higher spatial uniformity: for this reason, intensity fluctuations are not visible in PL images.

After this, also the PL image recorded at 600 nm, i.e. in the yellow spectral region, and shown in Figure 4.7(b), has been analyzed. In particular, from the comparison between this image and the corresponding EL luminescence reported in Figure 4.6(b), it can be noticed that the PL signal does not show the presence of any yellow-emitting dot. To explain this fact, we have relied on the interpretation provided by [9], which suggests that yellow dotlike emission can originate from

tunneling-assisted radiative recombination: in this case, carriers are injected by tunneling from the quantum wells to the barrier or cladding layers, where they radiatively recombine through defects. Thus, according to this hypothesis, the results obtained from EL and PL measurements suggest that the yellow EL signal, occurring under low forward bias conditions, is generated only in correspondence of localized defective regions, where injection/tunneling of carriers towards deep states is favored. On the other hand, during PL measurements the generation rate is uniform on all device surface. Thus, for this reason, yellow luminescence dots are visible only in the EL signal and not in the PL signal. The absence of yellow luminescence in the PL signal is confirmed by also Figure 4.6(c), that reports a comparison between EL and PL spectra measured on the whole device area and in proximity of yellow dot "E": as it can be noticed, the PL spectrum of yellow spot has exactly the same shape as the integrated PL signal from the whole device surface. Note also that PL signal has a broad visible spectrum compared to EL spectrum. However, to verify this physical interpretation of the origin of yellow luminescence, it has been necessary to perform also electrical and EL measurements at different current and temperature levels. The results of this analysis will be presented in the following of this section.

4.3.1 Current and temperature dependence of yellow localized emission

The results of EL measurements carried out at different current levels on one of the analyzed green LEDs, are reported in Figure 4.8: in particular, the EL spectra shown in this image refer to the emission signal generated at dot "E" of Figure 4.6(b). As it can be observed, at very low current levels the EL spectrum of dot "E" is dominated by a yellow peak and has a green shoulder. However, with increasing current levels, the relative intensity of green shoulder with respect to the yellow peak significantly increases. In particular, it can be seen that for current levels higher than about 1-2 μA, the EL spectrum is dominated by green emission, and the yellow peak almost disappears.

To better understand the results obtained from EL measurements at different current levels, also the influence of the presence of yellow dots on electrical properties of devices has been analyzed. First of all, we can observe the comparison reported in Figure 4.9, between typical current-voltage (I-V) characteristics of a LED with a high density of yellow dots and one without yellow dots, respectively. As it can be noticed, the presence of yellow dots can significantly modify the low forward region of I-V curves of LEDs, by inducing an increase of current for voltage levels lower than about 2.2 V. On the other hand, for high voltage levels, greater than 2.2 V, which corresponds a current level greater than about 1 μA, the two

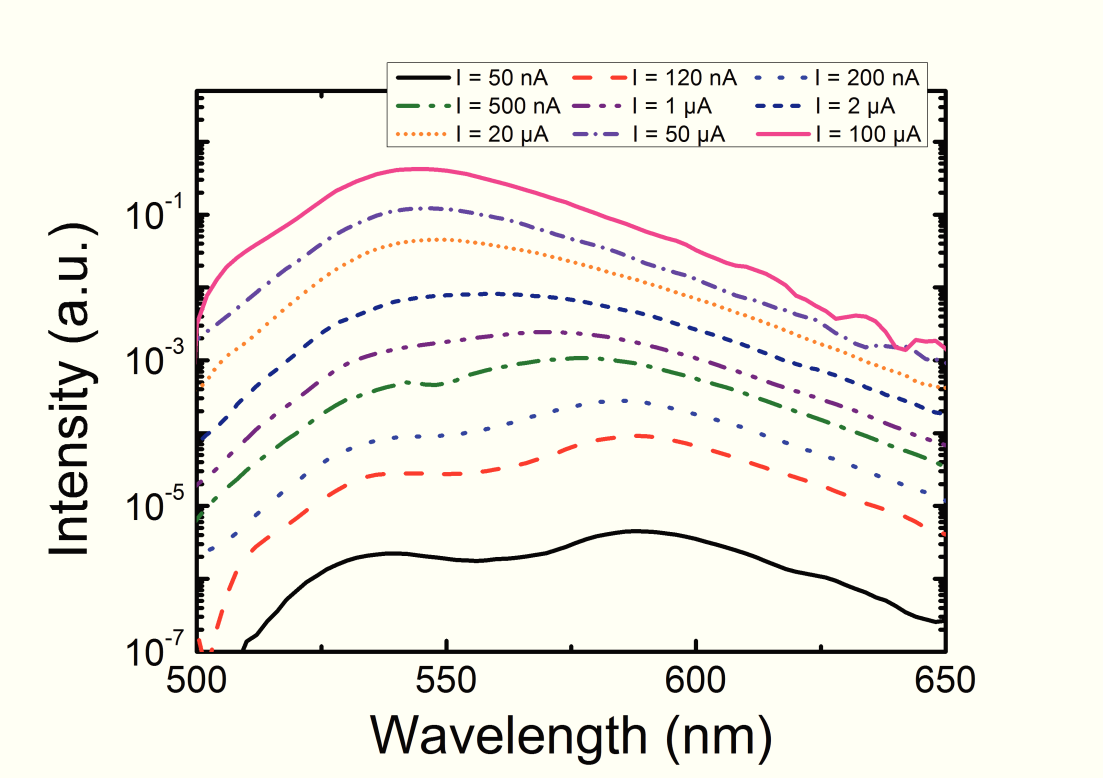


Figure 4.8: EL spectra of yellow-emitting dot "E" of Figure 4.6(b), measured at different current levels.

curves coincide, thus suggesting that in this region the dominant conduction process in the two LEDs is the same, and thus, it is not related to the presence of yellow dots.

Furthermore, current-voltage measurements carried out at different temperatures levels on a LED with a high density of yellow dots, indicate that under low forward bias the conduction is dominated by tunneling; in fact, from the *I-V* characteristics reported in Figure 4.10, it is clear that in the low-forward bias region, the slope of curves does not significantly vary with temperature, thus suggesting that current-voltage behavior can be well described by a relation of the type $I \propto e^{qV/E}$, i.e. the conduction is determined by a field-dependent process than rather by a thermally-activated one [89]. It has been mentioned in section 2.3.4 that such a type of relation describes a conduction process dominated by tunneling, where E is an energy parameter that reflects the tunneling transparency of the energetic barriers at the heterointerfaces. Thus, higher tunneling components, as in the case of devices with a high concentration of yellow dots, may correspond to a higher concentration of defects, since tunneling can be assisted by traps. On the other hand, for high voltage levels the slope of *I-V* curves in Figure 4.10 significantly changes, suggesting that the conduction starts to be dominated by carrier diffusion and recombination.

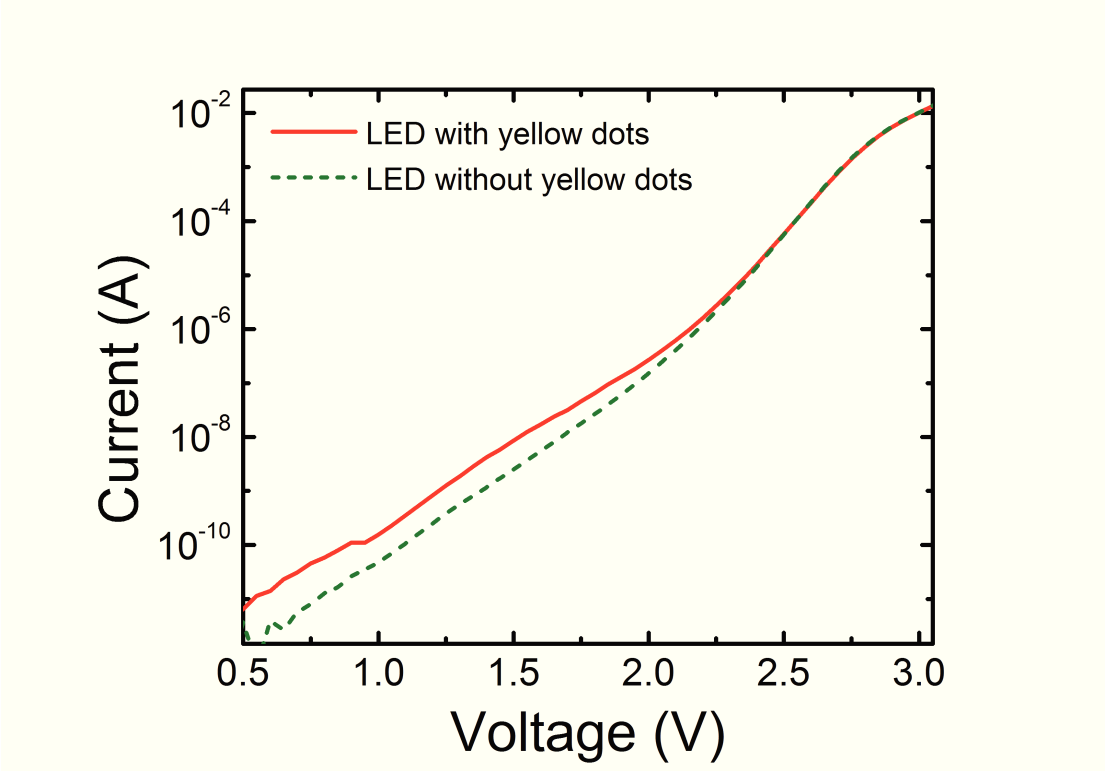


Figure 4.9: Comparison between current-voltage (I-V) characteristics of a green LED with a high density of yellow dots and one without yellow dots, respectively.

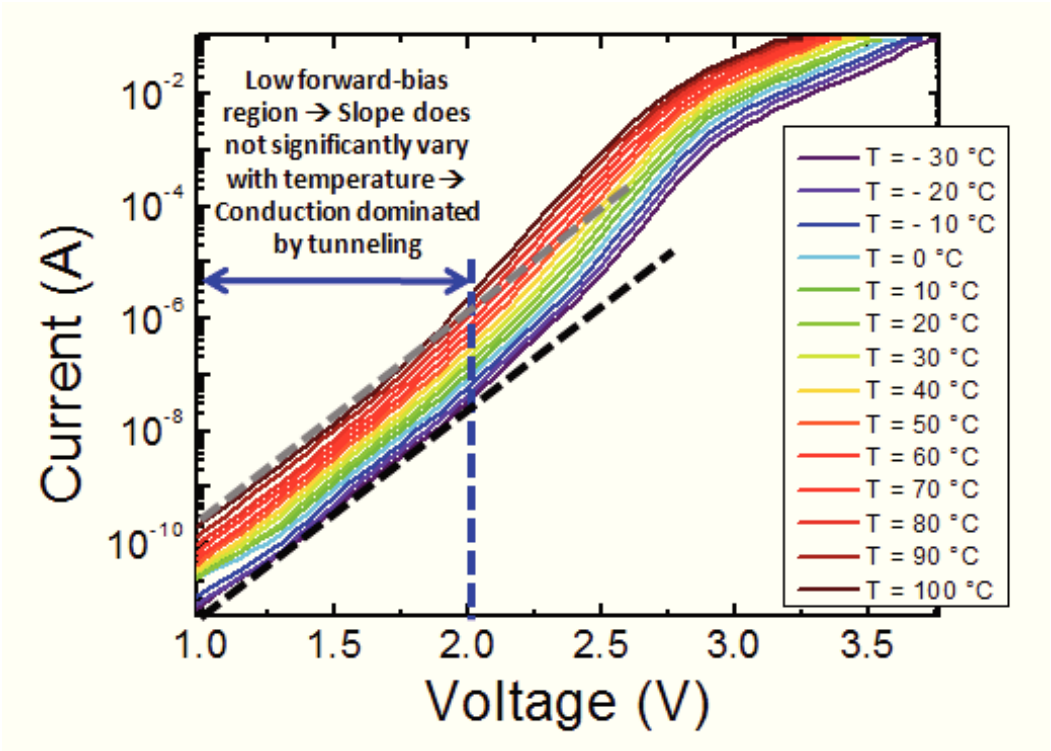


Figure 4.10: Current-voltage (I-V) characteristics measured at different temperature levels on one of the analyzed green LEDs with a high density of yellow-luminescent dots.

Also the temperature dependence of yellow emission from localized dots has been analyzed and the results are summarized in Figure 4.11. In particular, the EL spectra of dot "E" measured with an injection current of 120 nA and reported in Figure 4.11(a), show that with increasing of temperature, the localized yellow luminescence decreases more rapidly with respect to the green peak. Also the activation energies for the decay of the two luminescent peaks have been calculated, by means of the Arrhenius plot of the intensity variation of green and yellow luminescence shown in Figure 4.11(b): as it can be noticed, yellow luminescence decays with an activation energy of 0.64 eV, which is significantly higher than the 0.33 eV of green peak. Note that the stronger temperature dependence of yellow luminescence with respect to green emission, is due to the fact that yellow emission originates from a defect-related recombination process, activated by tunneling. In particular, with increasing of temperature, the yellow luminescence becomes weaker than the green emission, as reported in Figure 4.11(a), because at high temperature levels a large amount of carriers is injected in the quantum wells, and therefore, the band-to-band recombination is favored with respect to the yellow luminescence process, that occurs at low carrier density levels, due to the tunneling of carriers from the quantum wells to the barrier layers.

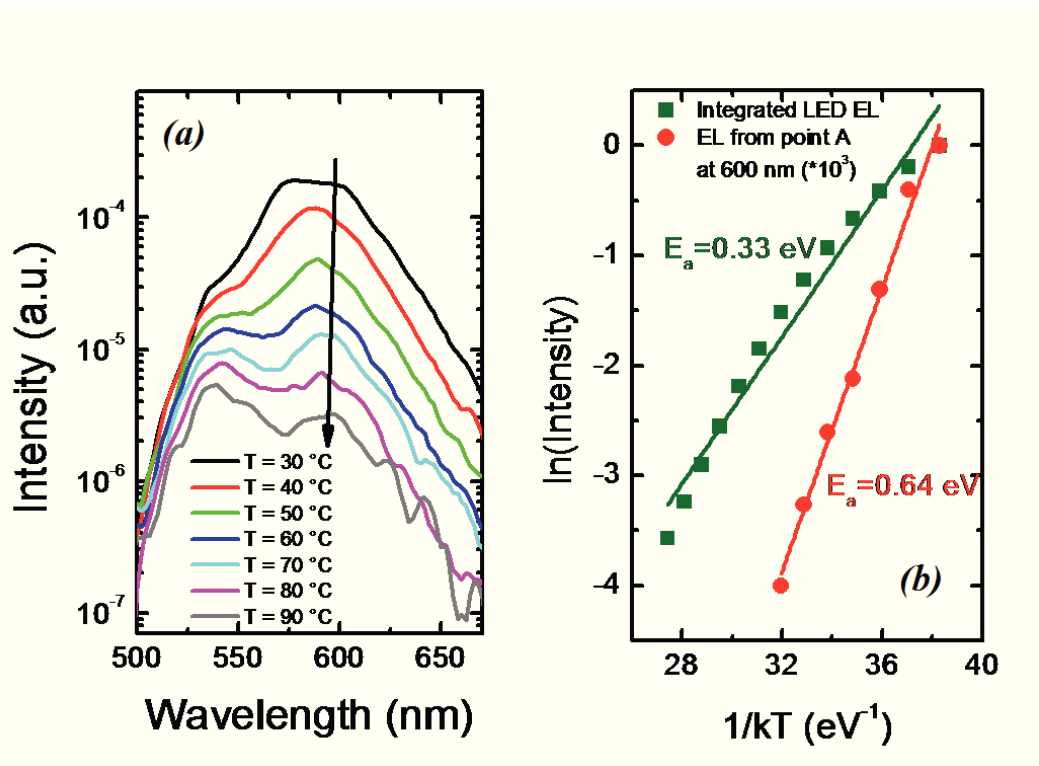


Figure 4.11: (a) EL spectra measured in proximity of dot "E" at different temperature levels and with an injection current of 120 nA. (b) Arrhenius plot of the intensity of green and yellow components of the emission from dot "E", taken from the plot in (a).

To conclude the analysis of defect-related localized emission processes under low forward bias, in the following of this section we propose a physical model that describes the recombination process responsible for yellow-dotlike luminescence in green LEDs.

4.3.2 Physical model for yellow localized emission

The results reported above suggest that yellow emission mainly occurs at low-forward bias conditions, where current conduction is dominated by tunneling, thus supporting the hypothesis that yellow luminescence is generated by tunneling processes occurring at localized regions, and possibly assisted by the presence of defects. A possible interpretation of these recombination processes is provided by the physical model proposed in Figure 4.12. In particular, this model is based on the fact that in the barrier layers there exists a deep acceptor level, which is typically present in intrinsic GaN layers and considered to be responsible for the yellow luminescence of GaN [108]. A schematic representation of recombination processes occurring for low and high voltage levels in the presence of these defects, are reported in the Figures 4.12(a) and (b), respectively.

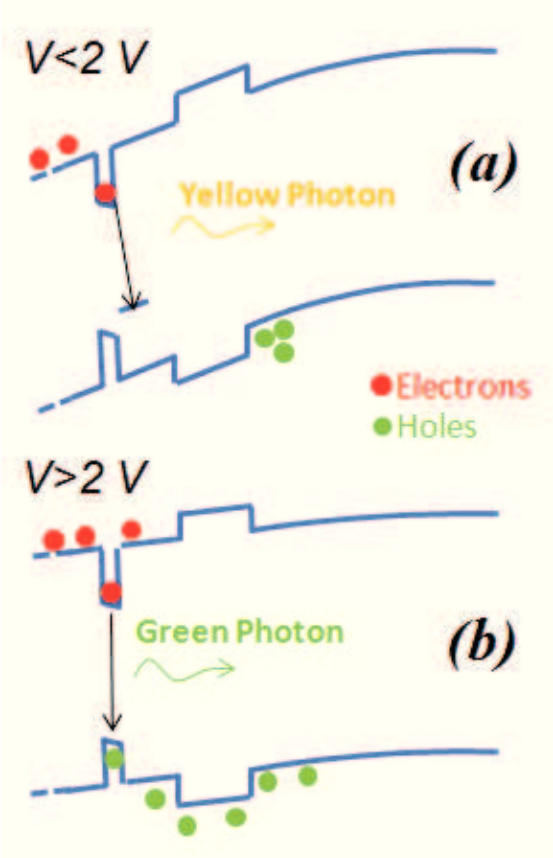


Figure 4.12: Schematic representation of recombination processes occurring in proximity of the yellow dots, for (a) low and (b) high voltage levels.

As shown in Figure 4.12(a), for low-forward voltage levels, only few holes can reach the quantum well region, due to the high potential barrier of the electron blocking layer (EBL). On the other hand, in this operating regime, electrons can be injected more esalily in the quantum wells. At this point, in proximity of a defective region, electrons may tunnel out of the quantum well and radiatively recombine to the deep acceptor level in the last quantum barrier, resulting in yellow emission centered at about 600 nm.

On the other hand, as represented in Figure 4.12(b), when the voltage level is increased above a given threshold, holes can overcome the potential barrier of the EBL, and thus they are injected in the quantum wells. Under these conditions, due to the high concentration of carriers inside the quantum wells, the dominant recombination mechanism becomes the band-to-band recombination in the quantum wells. For this reason, at high current levels EL analysis detects a green spectrum even from a yellow-emitting region.

Yellow luminescence occurs only in localized regions, with submicrometer size. These spots can correspond to the presence of structural defects, which may enhance the tunneling of carriers from the quantum well to the trap states responsible for yellow emission. At the beginning of this section, we have already said that yellow-dotlike emission cannot be associated to threading dislocations, because the density of these dots is significantly lower than the threading dislocation density of devices. Particular defective structures could easily form at the interface between the active layer and the p-type material, therefore playing a role in the measured yellow luminescence [9]. These defective structures include, for example, defects related to indium segregation, clusters of defects close to dislocations, and Mg-related defective structures.

Chapter 5

Analysis of injection processes and carrier distribution in MQW GaN-based LEDs with color-coded structure

In the previous chapter we have seen that localized defects can strongly influence the emission properties of GaN-based LEDs under reverse and low-forward bias conditions. Defect-related recombination results also in significant non-radiative components, thus reducing the efficiency of devices in the low operating regime and possibly at high current levels. However, it has been already mentioned in the introduction of this thesis that several other factors can limit the efficiency of LEDs, including the carrier escape from quantum wells, which is more prominent at high current and temperature levels, the efficiency droop, usually ascribed to Auger recombination, and the nonuniform distribution of carriers among the quantum wells of a multiple quantum well structure. In particular, this last phenomenon nowadays represents one of the most critical issues for the realization of high efficient multi-quantum well LEDs: for this reason, it is very important to analyze the carrier distribution and the injection processes in multiple quantum well structures and to deeply understand the physical mechanisms that limit the efficiency of such structures. To do this, in the last years, it was proposed to use GaN-based LEDs with color-coded structure: these device have a multi-quantum well structure, which is characterized by the fact that each quantum well has a different indium content, corresponding to a different emission wavelength. Thus, with such a type of structure, it is possible to analyze the emission from each quantum well by means of electroluminescence measurements.

Several works can be found in literature concerning the study of MQW-based LEDs with color-coded structure [15] [109] [110] [111]: in these studies, color-

coded devices have been used to study asymmetries in carrier distribution, i.e. to understand if in a MQW structure all the quantum wells emit light, to evaluate the relative contribution of each quantum well to the overall emission, and to analyze the injection and recombination processes within the LED structure. However, with a few exceptions, none of these works has attempted a combined experimental and simulation approach, to analyze color-coded structures. Different hypothesis on the origin of asymmetries in carrier distribution have been proposed in different works: in particular, both uneven hole distribution [15] [112], uneven electron distribution [113], and more balanced or complex profile have been suggested [109] [110]. With reference to the hypothesis of uneven hole distribution, the most quoted rationale related to this phenomenon is that holes are primarily injected into the quantum well closer to the p-side, and only a small fraction of them reaches the other quantum wells, mainly due to the poor hole mobility μ_p [114].

The aim of this work is to achieve a better understanding of the carrier injection and recombination processes occurring in multi-quantum well GaN-based LEDs. To obtain this, an extensive analysis based on combined electroluminescence measurements and simulations was carried out on color-coded LEDs. In particular, the EL analysis was performed at different current and temperature levels. The results of this analysis have been provided information on: *(i)* the role of current and temperature in changing the spectral characteristics, and thus the carrier distribution, of devices; *(ii)* the impact of the position of each quantum well on its contribution on device emission; *(iii)* the role of hole and electron mobilities, carrier density, and non-radiative recombination in determining the optical characteristics of devices.

In this chapter, after an initial description of analyzed devices and the experimental details adopted for this analysis, the results of electroluminescence characterization, carried out at different current and temperature levels, will be presented. Afterwards, also the results of simulations will be reported. Finally, results of EL analysis and simulations will be compared, in order to give a correct interpretation of phenomena that limit the optical efficiency of these devices.

5.1 Analyzed devices and experimental details

The analysis was carried out on multi-quantum well (MQW) InGaN-based LEDs with color-coded structure, having an area of $1.2 \times 10^{-3} cm^2$. The LEDs were grown on a sapphire substrate with a dislocation density of about $5 \times 10^9 \, cm^{-2}$, and were provided by manufacturer as on-wafer devices. A schematic of the layered structure of these devices is shown in Figure 5.1: as it can be seen from the figure, the LED structure comprises an active region with three quantum wells having a thickness of 2-3 nm, grown on the top of a Si-doped GaN layer. The particularity of this

structure is that each quantum well has a different indium content, corresponding to a different emission wavelength: with reference to Figure 5.1, QW1 (close to the p-side) has a 25 % In content, corresponding to green-yellowish emission centered at about 560 nm; QW2 (the intermediate one) has a 15 % In content, corresponding to blue emission, centered at about 460 nm; QW3 (close to the n-side) has a 5 % In content, corresponding to a violet emission, centered at about 400 nm. Finally, the LED structure includes a p-type region, which consists of a Mg-doped GaN cap layer, with a thickness of 130 nm and a doping level N_A equal to $3 \times 10^{19}\, cm^{-3}$. Note the absence of an electron blocking layer (EBL) in this structure: this choice is related to the fact that we want to analyze the injection processes and carrier distribution without the influence of this layer.

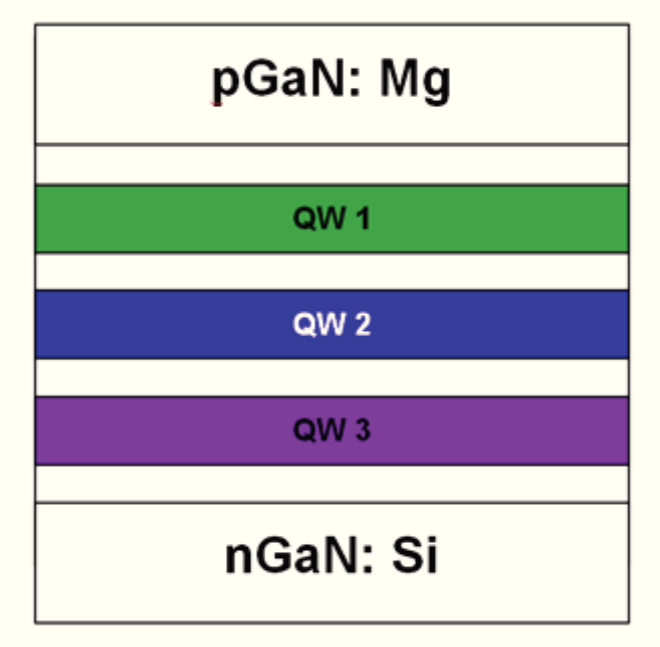


Figure 5.1: Schematic layered structure of analyzed LEDs with color-coded structure. The color of each quantum well suggests the corresponding wavelength emission.

The electroluminescence (EL) analysis on these devices was carried out at different current and temperature levels, by means of a *Instrument Systems CAS140CT* spectrometer and a *Mitutoyo* optical microscope with long-working distance lenses. The spectrometer was connected to the microscope by means of an optical fiber. The whole system, including the spectrometer, the optical fiber and the microscope, was calibrated with a halogen light source with known spectrum. The device under test is biased by means of a *SourceMeter Keithley 2536A*. Furthermore, to perform EL measurements at different temperature levels, devices were mounted on a thermally-controlled chuck: in particular, the measurement temperature was varied from 25 $°C$ to the maximum value of 250 $°C$.

Also simulations of these devices have been carried out by colleagues of *Politec-*

nico of Torino, in order to better understand the physical mechanisms that influence the optical efficiency of color-coded LEDs. All simulations were performed by means of the APSYS modeling software, which implements a two-dimensional (2D) drift-diffusion model coupled with several quantum corrections critical in III-nitrides optoelectronic devices. Full details about the material parameters adopted for the simulations may be found in [115] and [116].

5.2 Results of electroluminescence analysis

The results of EL analysis carried out at different current levels, on one of the analyzed LEDs with color-coded structure, are reported in Figures 5.2 and 5.3 for low and high current levels, respectively. In particular, by observing the EL spectra, it is possible to analyze the emission from each quantum well by measuring the EL intensity in proximity of the three fundamental wavelengths localized at about 560 nm, 460 nm and 400 nm, for QW1, QW2 and QW3, respectively (see the description of devices in the previous section).

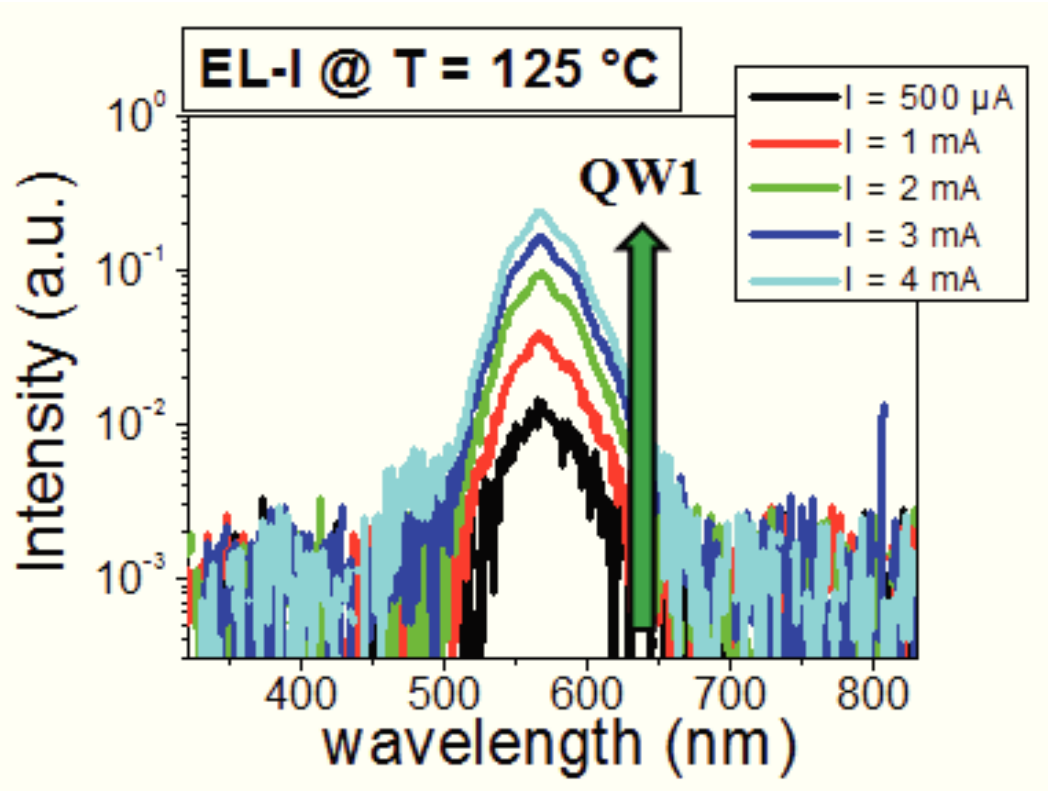


Figure 5.2: EL spectra measured at low current levels and at a temperature of 125 $°C$, on one of the analyzed samples.

EL spectra reported in Figure 5.2 indicate that for low measuring current levels, only QW1, which is the quantum well close to the p side, characterized by a green

emission centered at about 560 nm, contributes to device luminescence. On the other hand, no emission from QW2 and QW3 can be observed in this operating regime. On the contrary, with increasing current level, also QW2, characterized by blue emission centered at about 460 nm, starts to emit, as shown in Figure 5.3. However, also in this case no luminescence is detected from QW3, which is the one close to the n-side, with violet emission centered at about 400 nm, by means of the adopted measurement system.

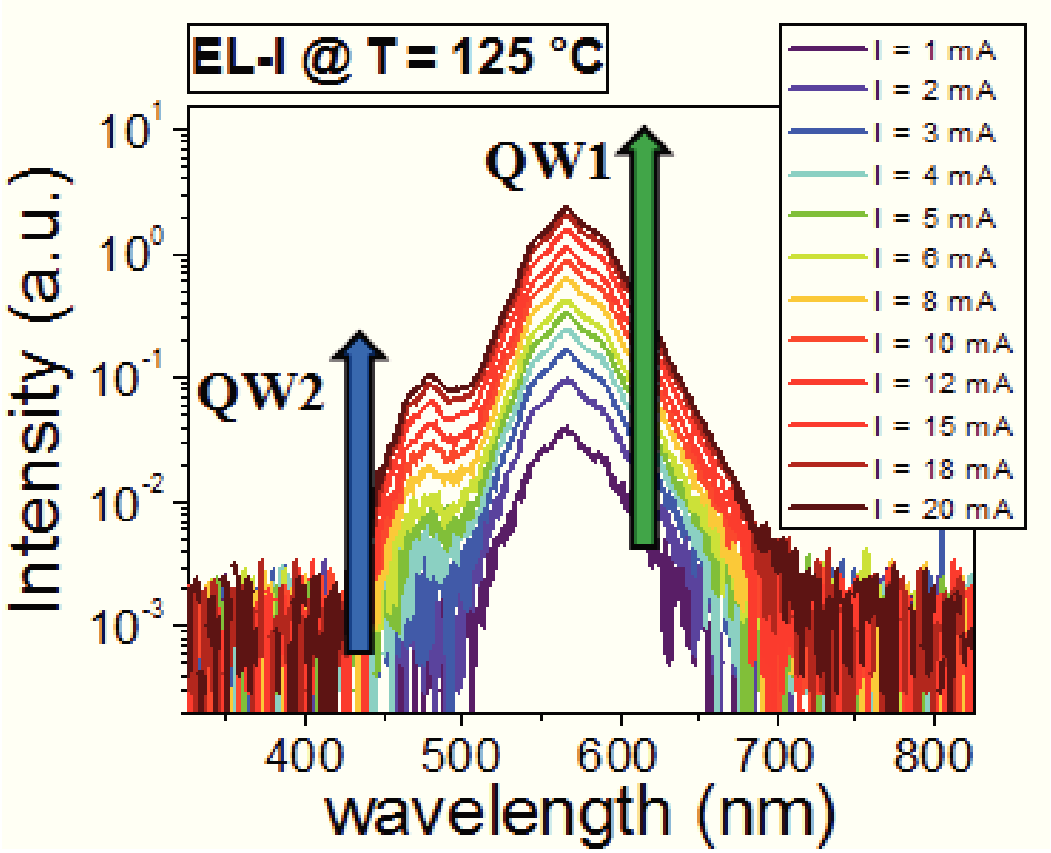


Figure 5.3: EL spectra measured at different current levels and at a temperature of 125 $°C$, on one of the analyzed samples.

With increasing current level, the intensity of both QW1 and QW2 significantly increases, as reported in the graphs of Figure 5.4, due to the increased amount of injected carriers. In particular, as it can be noticed from Figure 5.4(b), which reports the normalized EL intensity from QW1 and QW2 as a function of injected current (note that the intensities are normalized with respect to the values measured at 5 mA), the emission intensity of QW2 shows a stronger variation with respect to QW1. The superlinear behavior of QW2 shown in Figure 5.4(b), can be explained by the fact that the carrier density in QW2 shows a considerable increase with respect to QW1, with increasing of applied bias.

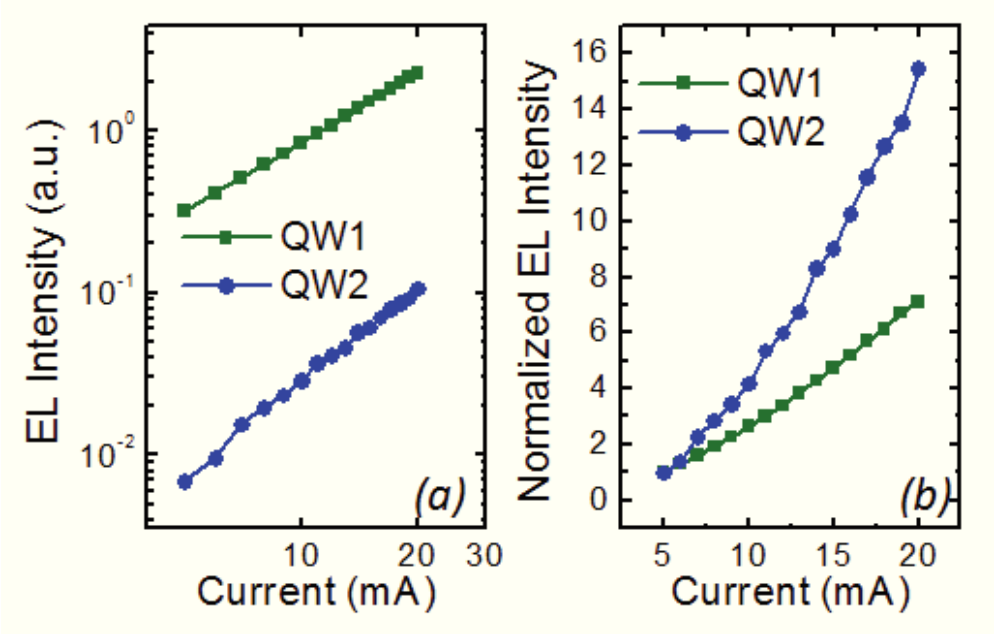


Figure 5.4: (a) EL intensity of the emission from QW1 and QW2 as a function of injected current. (b) Same data as in (a), normalized with respect to their value measured at 5 mA.

Thus, the results obtained from EL analysis carried out at different current levels seem to suggest that the emission from quantum wells in such a structure is limited by a poor hole injection from the p-side, possibly due to the low mobility of these carriers (typical hole mobility μ_p is around 10 $cm^2V^{-1}s^{-1}$, which is significantly lower than electron mobility $\mu_n \sim 100\, cm^2V^{-1}s^{-1}$). A possible interpretation of this hypothesis is provided in the schematic model of Figure 5.5: as a consequence of poor hole mobility or low carrier injection from the p-side, holes can reach the first quantum well close to the p-side and only few of them also the second one. However, no hole can reach the third quantum well. On the other hand, electrons can easily reach all the three quantum wells, thus resulting in a high emission from QW1 and only a slight emission from QW2, as we have obtained from experimental results.

Based on the results reported above, the EL measurements at different temperature levels were taken at an injection current of 20 mA, in order to analyze how the intensities of QW1 and QW2 vary with changing temperature. The EL spectra obtained from this characterization, which are reported in Figure 5.6, indicate that the intensities of both QW1 and QW2 show a strong decrease at high temperature levels: this phenomenon can be ascribed to an increase in the non-radiative recombination rate within the quantum wells, and/or to the fact that at high temperatures, carriers have a higher thermal energy, and therefore they can easily escape from the QWs. In a recent report it has been suggested that,

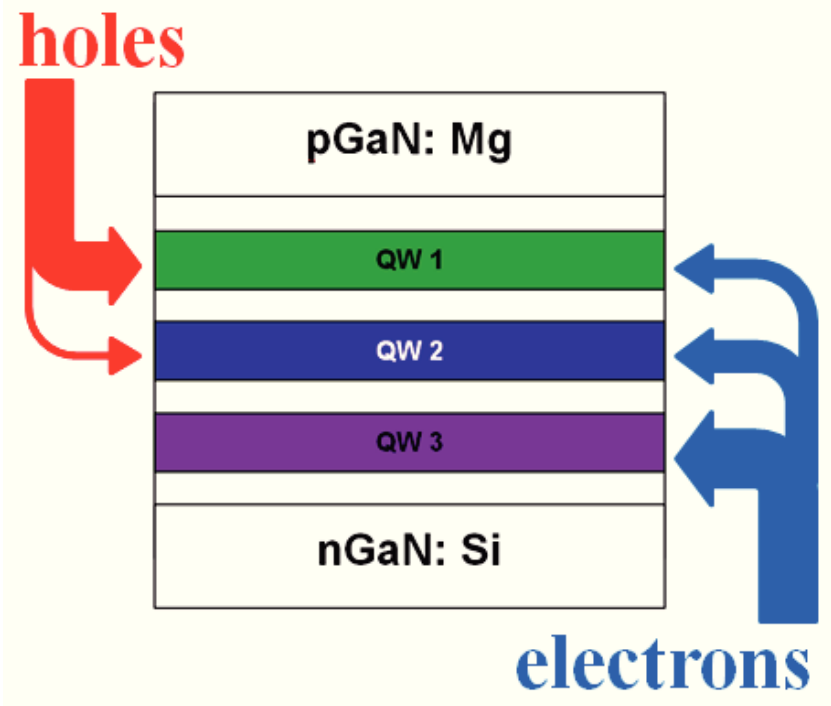


Figure 5.5: Schematic model of carrier injection on the active region of analyzed devices, based on the results of EL analysis carried out at different current levels.

in the green QW only, also Auger recombination could be significant, and that Auger coefficients increase linearly with temperature [117]. Another possible loss mechanism is the Auger-induced leakage, proposed in [118]: this process would approximately double the effects of Auger processes, since, in addition to removing an electron-hole pair, every Auger recombination event promotes a third carrier to energies well beyond the confining potential of the QWs. However, it is presently beyond the reach of the simulation model adopted within this work.

The strong decrease of EL intensity from both QW1 and QW2 is also shown in Figure 5.7. In particular, Figure 5.7(b), which reports the EL intensity of QW1 and QW2 as a function of temperature, normalized with respect to their values measured at 25 $°C$, shows that QW2 has a weaker temperature dependence with respect to QW1, i.e. the decrease in the intensity of QW2 is smaller than that of QW1, with increasing temperature. This phenomenon was initially attributed to a stronger activation of the acceptor dopant (Mg) occurring at high temperature levels, or to the fact that at high temperatures, holes have a higher thermal energy and thus, there is a increased probability that some of them can escape from QW1 and reach QW2.

However, considering the position and depth of the quantum wells, the following considerations can be done: *(i)* if the dominant mechanism responsible for the decrease of EL intensity from quantum wells was electron/hole escape due to the increased thermal energy of carriers at high temperature levels, this phenomenon

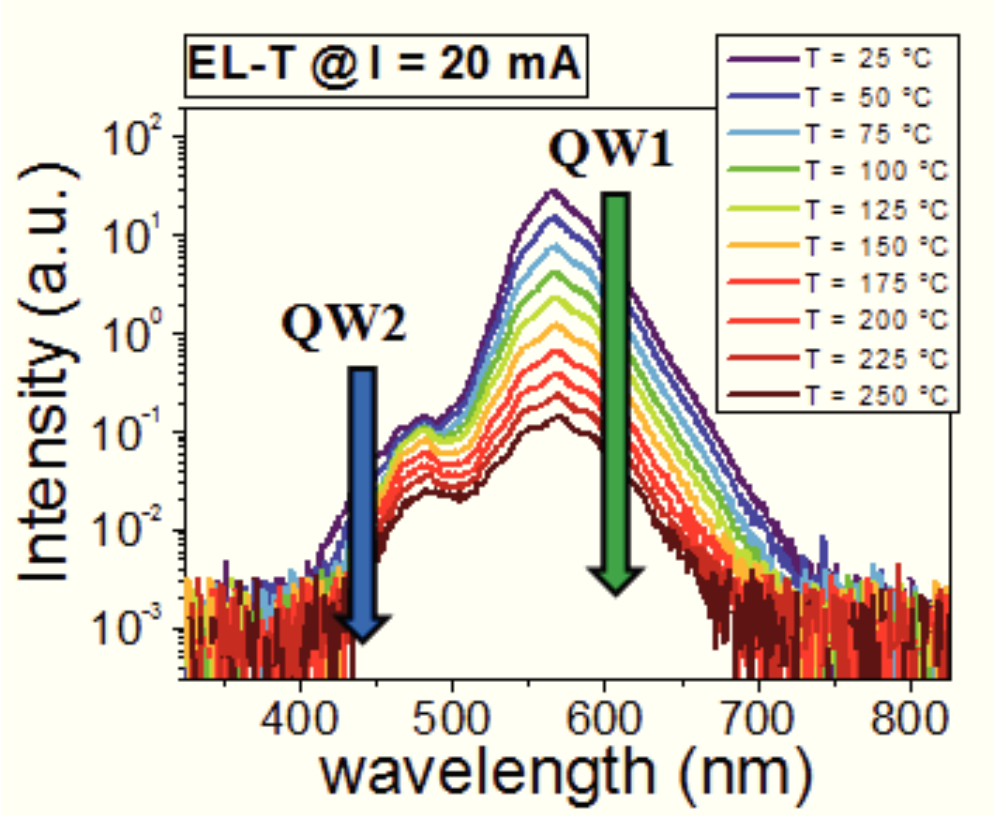


Figure 5.6: EL spectra measured at different temperature levels and at an injection current of 20 mA, on one of the analyzed samples.

should be more prominent in the blue quantum well (QW2), which is shallower, with respect to the green one (QW1), which is deeper. However, this is not the case, as it has been shown in Figure 5.7(b). *(ii)* On the other hand, the green quantum well (QW1) has a higher indium content, which should correspond to a higher defect density. For this reason, thermal quenching due to non-radiative recombination is more prominent in QW1 with respect to QW2, which has a lower indium content. *(iii)* If the mobility of holes is a real bottleneck for the efficiency of QW2, as quoted above, with increasing temperature level QW2 should show a stronger decrease with respect to QW1, since an increase in the temperature of devices would result in a decrease of hole mobility, and thus in a less amount of holes that can reach QW2. However, this is not the case, and thus the results of Figure 5.7 confirm that in reality hole mobility does not strongly influence the efficiency of quantum wells.

Thus, from the considerations above it is clear that more investigation on these LED structures is needed, in order to better understand the physical mechanisms that limit the emission from quantum wells: this has been obtained by means of two-dimensional simulations, carried out by colleagues of *Politecnico of Torino*, whose results will be presented and discussed in the next section.

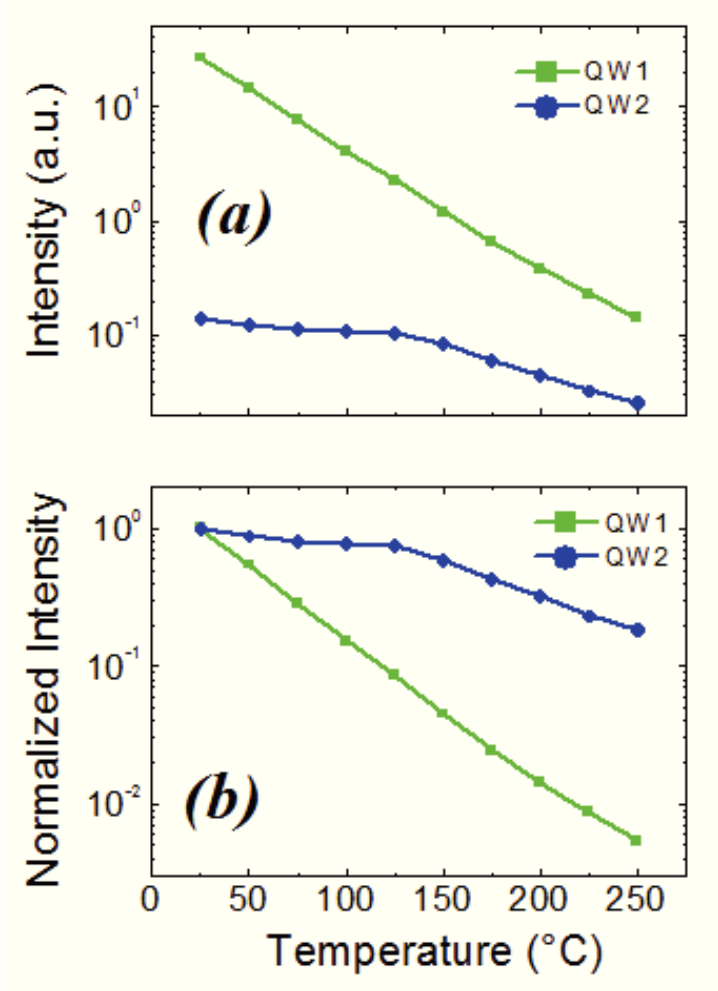


Figure 5.7: (a) Variation of the intensity of QW1 and QW2 with increasing temperature level. (b) Same data as in (a), but normalized with respect to their values measured at 25 $°C$.

5.3 Results of simulations

Two-dimensional simulations carried out by means of the APSYS modeling software on GaN-based LEDs with color-coded structure, have provided interesting results, which have contributed to the understanding of physical mechanisms that limit the optical efficiency of quantum wells.

Figure 5.8 reports the simulated band diagram, both at low and high current levels, and the simulated electron and hole densities within the quantum wells. The results of simulated band diagram reported in Figure 5.8(a), show that the fact that at low current levels (1 mA in the case of figure) only QW1 contributes to the whole emission of devices can be explained by observing that, when the device is biased with an injection current of 1 mA, the position of the quasi-Fermi level for electrons is significantly above the conduction band only in QW1. As a consequence, the electron densities in QW2 and QW3 are significantly lower

than that in QW1, thus reducing their recombination rate with respect the green quantum well. This fact is also confirmed by the simulated electron densities within the three quantum wells, shown in Figure 5.8(b). With increasing current level to 20 mA, from the same figure it can be noticed that the relative position between quasi-Fermi level for electrons and the conduction band significantly changes (note also the inset of Figure 5.8(a)), thus leading to an increase in the electron density in QW2. On the other hand, from Figure 5.8(a) it can be also observed that the position of quasi-Fermi level for holes with respect to the valence band, does not significantly change with increasing applied bias. This is also confirmed by Figure 5.8(c), which shows that the concentration of holes in the three quantum wells does not significantly vary with increasing bias from 1 mA to 20 mA. These simulations therefore suggest that the main factor limiting the efficiency of QW2 and QW3 at low current levels is the limited availability of electrons, than rather that of holes. In particular, the superlinear behavior of the emission from QW2 previously observed in Figure 5.4(b), can be attributed to the fact that the carrier density in QW2 strongly increases with respect to that of QW1, with increasing applied bias, as suggested by simulation results of Figure 5.8(b).

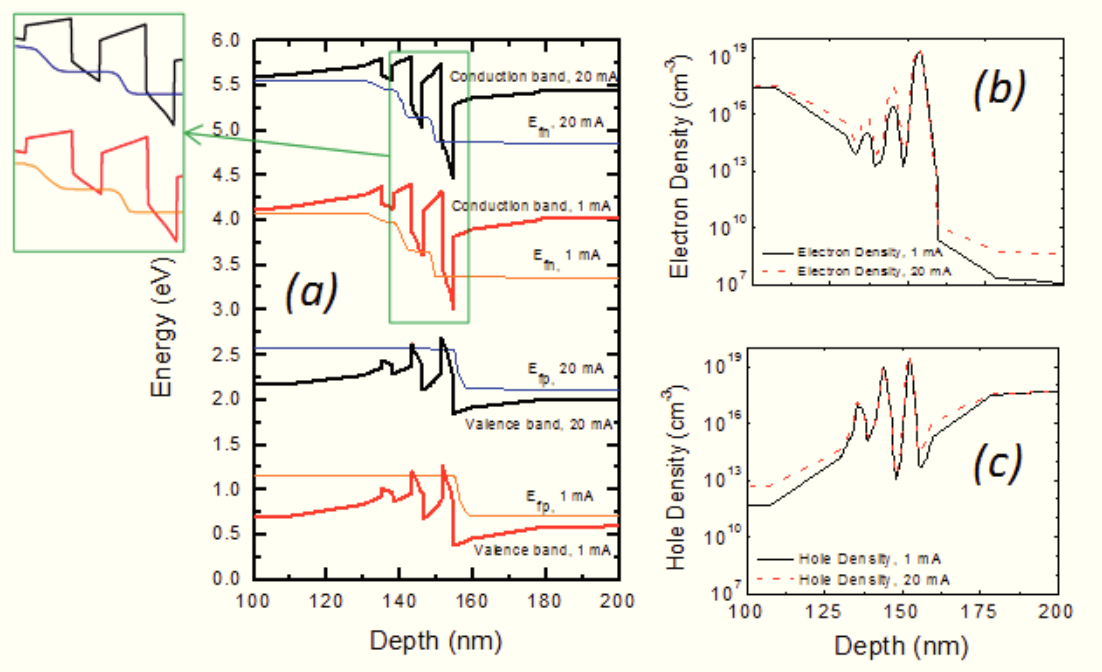


Figure 5.8: (a) Band diagram of the analyzed devices with color-coded structure, simulated at low (1 mA) and high (20 mA) current levels. (b) Corresponding simulated electron and (c) hole densities within the three quantum wells, at low and high current levels, respectively.

By observing again Figure 5.8(c), it can be noticed that in the structure under consideration, the hole density is nearly equal in the two topmost quantum wells.

In particular, this uniformity is almost insensitive to rather large variations of hole mobility. In fact, Figure 5.9 shows simulated electron and hole densities and EL spectra by considering various hole mobilities: no significant changes both in the carrier densities and in the emission are observed by varying hole mobility μ_p in a two-decade range. Thus, this result further supports the hypothesis that hole mobility does not represent a bottleneck for the efficiency of QW2.
The uniformity of hole density observed in Figure 5.8(c) is almost insensitive also to large variations of density and activation energy of acceptors in the p-type layer, spontaneous and piezoelectric polarization charge P at heterointerfaces, and band offset ratio $\Delta E_c/\Delta E_v$ at GaN/InGaN heterojunctions. In particular, the insensibility of hole density from variations of density of acceptors in the p-side, excludes also our previous hypothesis quoted above, that the weaker temperature dependence of QW2 with respect to QW1 could be attributed to a stronger activation of the acceptor dopant (Mg) occurring at high temperature levels.

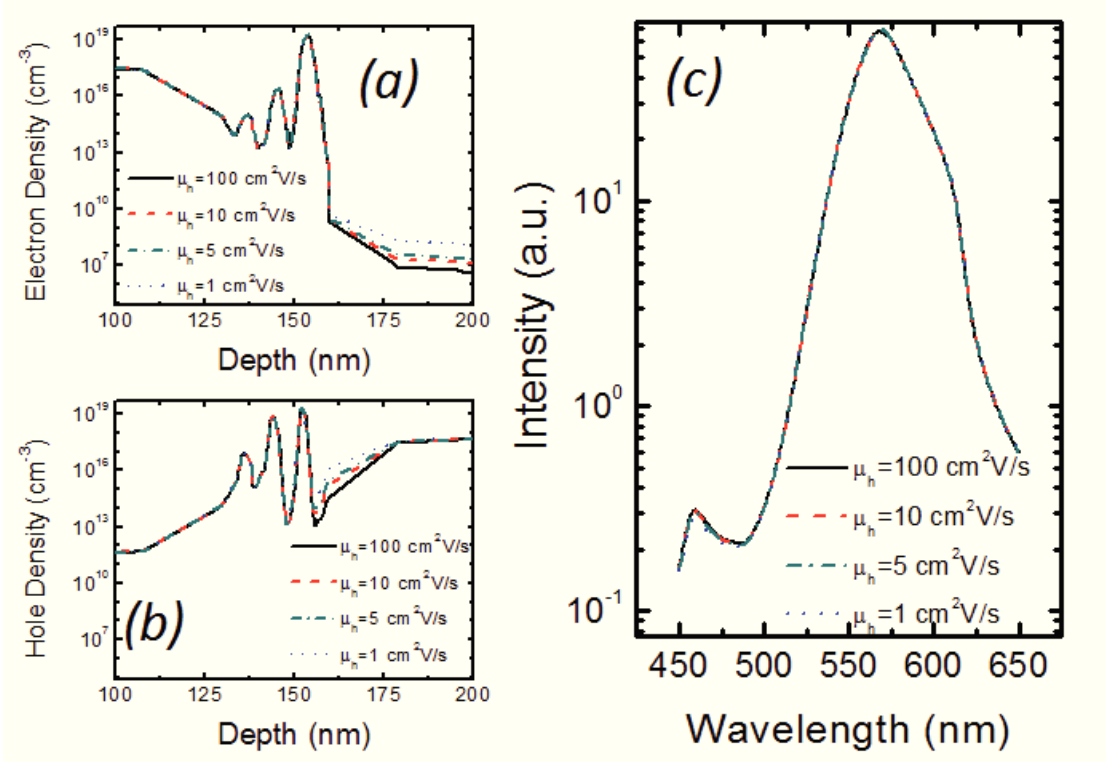


Figure 5.9: (a) Simulated electron and (b) hole densities at 1 mA, for different hole mobilities. (c) Simulated EL spectra by considering various hole mobilities.

On the other hand, from Figure 5.8(b) it can be noticed that the electron density has a strongly nonuniform profile, mainly because of the absence of an electron blocking layer in the analyzed structures. Furthermore, differently from the case of holes, the electron distribution among the quantum wells is heavily affected by temperature and injection level. In particular, with a reduction of the electron mo-

bility μ_n, for example due a higher temperature or larger ionized impurity and/or threading dislocation density, the corresponding electron concentration profile becomes less nonuniform, leading to a larger relative contribution of QW2 to the EL spectrum, as shown in Figures 5.10(a) and (b). A similar equalizing effect can be observed by slightly increasing the width of the barriers between quantum wells, as reported in Figure 5.10(c).

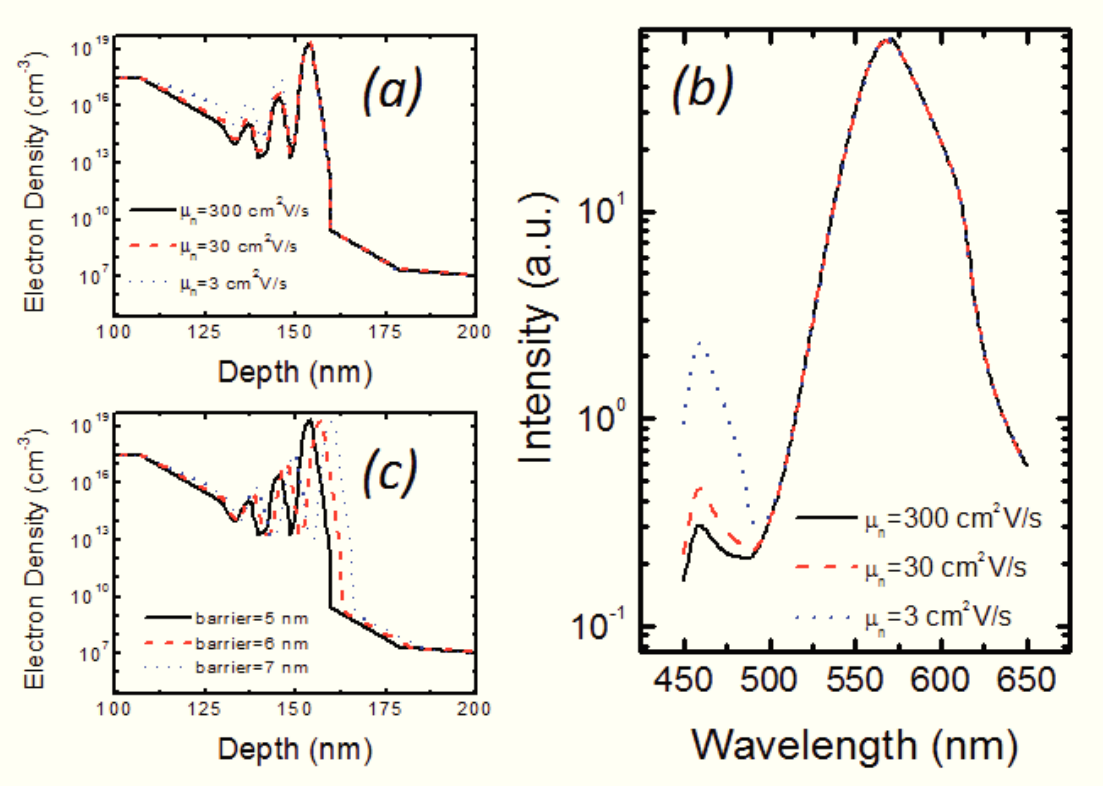


Figure 5.10: (a) Simulated electron densities at 1 mA, for different electron mobilities. (b) Simulated EL spectra by considering various electron mobilities. (c) Simulated electron densities at 1 mA for various thickness of the barriers between the quantum wells.

To conclude the analysis of injection processes and carrier distribution in multi-quantum well LEDs with color-coded structure, in the next section we will present some final considerations, which summarize the physical mechanisms that limit the efficiency of quantum wells.

5.4 Final considerations

The results of this extensive analysis based on combined electroluminescence measurements and simulations, have provided useful information on the physical mechanisms that limit the efficiency of quantum wells in the analyzed LED with color-coded structure. In particular, the following final considerations can be done:

- At low current levels, the poor efficiency of QW2 can be explained by the low density of electrons in this well. By increasing the bias level, the density of electrons in QW2 and QW3 significantly increases, as the quasi-Fermi level for electrons moves above the conduction band edge in QW2, thus determining a strong increase in the emission from this quantum well. On the other hand, results of simulations indicate that the hole injection is quite effective for both QW1 and QW2; moreover, the density of holes within the three quantum wells does not significantly vary with current level. These results thus suggest that the main factor limiting the efficiency of QW2 and QW3 at low current levels is the limited availability of electrons, than rather that of holes.

- From EL analysis, it has been seen that QW3 does not emit any measurable signal under conditions used in this work. The results of simulated band diagram suggest that this is due to the quite high distance between the quasi-Fermi levels and the band edges for both electrons and holes, in the whole analyzed current range. As a consequence of this fact, the concentrations of carriers in QW3 are considerably low compared to QW1 and QW2, and thus no violet light emission is detected. Also the hypothesis that the quite high distance between quasi-Fermi levels and the band edges is due to the absence of an electron blocking layer (EBL), has to be considered.

- Results of simulations have confirmed that, for the analyzed LED structures, hole mobility does not represent a real bottleneck for carrier injection and recombination. However, this consideration does not imply that hole mobility cannot play a critical role in determining the performance of MQW LEDs: its importance is determined by an interplay of several factors, most of them structural and amenable to optimization.

- The stronger thermal quenching of QW1 with respect to QW2, has been attributed to the higher defectiveness of the green QW compared to the blue one, which corresponds to higher non-radiative components, and therefore to a stronger sensitivity to thermal variations. Also Auger recombination and Auger-assisted leakage may contribute to the stronger decrease of EL intensity of QW1 compared to QW2 at high temperature levels, since they are expected to be significant only in the deepest quantum well.

Thus, the role of current, temperature, hole mobility, and carrier density in limiting the efficiency of InGaN-based LEDs with color-coded structure, have been discussed in this chapter. In particular, experimental results, supported by 2D simulations, provide information on the most important physical mechanisms that limit the radiative efficiency of LEDs at low and moderate current levels.

Chapter 6

Analysis of physical mechanisms that limit the ESD robustness of GaN-based LEDs

As we have seen in section 3.5, light emitting diodes are particularly sensitive to the effects of electrostatic discharge events, that can induce the catastrophic failure of devices. In particular, gallium nitride based LEDs suffer particularly from electrostatic discharges. In section 3.5 we have also seen that in the recent years several solutions have been proposed in order to increase the ESD robustness of LEDs. However, despite the different ESD protection strategies developed, the robustness of GaN-based LEDs is still quite low. For this reason, it is necessary to deeply understand the physical mechanisms that limit the ESD robustness of these devices, with the purpose to identify the mechanisms responsible for the ESD failure of LEDs, and thus contributing to the development of more reliable LEDs.

In this chapter we present an extensive study of physical mechanisms that limit the ESD robustness of GaN-based LEDs. The analysis was carried out on ten LED families, each characterized by a different value of ESD robustness. The aim of this work is to identify a possible correlation between the ESD failure rate of devices and their electrical and optical properties. Furthermore, after the complete characterization of influence of defects on electrical and optical properties of GaN-based LEDs carried out in chapter 4, also the role of defects in limiting the ESD robustness of devices will be analyzed in the following. After a brief description of analyzed devices, the results of an initial electro-optical characterization, based on current-voltage (I-V), capacitance-voltage (C-V), electroluminescence (EL) and optical power-current (L-I) measurements will be presented. Afterwards, the correlation between ESD robustness and the presence of defects will be analyzed, showing the data obtained from slow capacitance transient, deep level optical spectroscopy (DLOS) and deep level transient spectroscopy (DLTS)

measurements. To conclude, the main results will be summarized in a final section.

6.1 Description of analyzed LEDs

In this work 10 LED families have been analyzed: each of them is characterized by a different ESD robustness, whose details are provided below. The analyzed samples are GaN-based LEDs, emitting at about 465 nm, i.e. in the blue spectral range, with a multiple quantum well (MQW) structure. However, the layered structure of LEDs is not known. LEDs have an area of $290 \times 290\,\mu m^2$. The devices were grown by metal-organic chemical vapor deposition on a sapphire substrate; afterwards, the as-grown chips were removed from the sapphire substrate by means of the *laser-induced liftoff* technique, which is based on the application of high power laser pulses through the sapphire substrate, in order to thermally dissociate the interface and thus separate the two materials, as shown in Figure 6.1. Finally the LED dies were mounted on a metallic TO18 package using an epoxy glue. Note that by means of laser-induced liftoff technique, the LED contacts can be realized on the opposite side of the layered structure, thus enabling a vertical current flow. The surfaces of LEDs have been also smoothed, in order to allow a better observation of localized emission spots under reverse bias with high resolution, by means of an optical microscope.

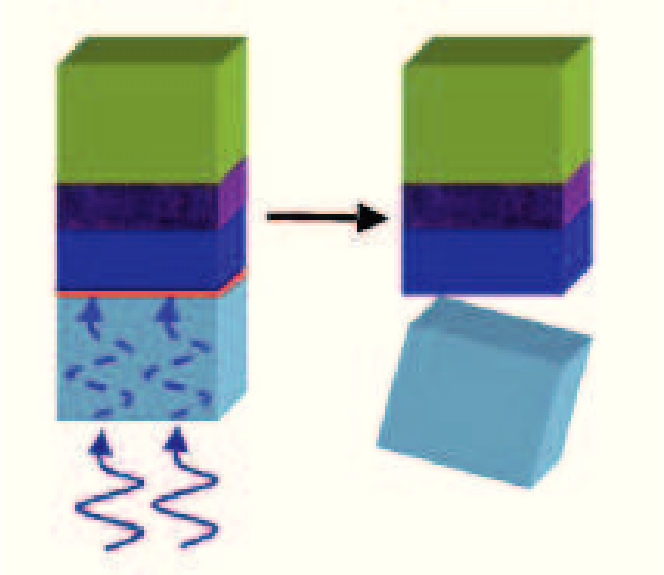


Figure 6.1: *Laser-induced liftoff* technique used for the removal of LED chip from sapphire substrate.

The LED families were called according to the name of wafers provided by the manufacturer. Thus, for simplicity, the analyzed LED series were named S20, S21, S22, etc., until S29, as indicated in the table 6.1. Before to start the charac-

terization, the LEDs were submitted to a ESD stress test under reverse bias by manufacturer, according to the HBM model. The ESD stress test is performed as follow:

1. A single reverse ESD pulse is applied to LEDs by means of a HBM system. Thus, the failure rate of each family in measured from the results of this test and it is called *First level failure F1.*

2. After that, the LEDs that have passed the first test are submitted to a second ESD test, which consists of the application of a second reverse ESD pulse according to the HBM model. The failure rate of LED series measured from this second test is called *Second level failure F2.*

3. Finally, the *Relative failure* can be calculated as the ratio *Second level failure F2/First level failure F1.*

Note that the second ESD pulse is applied after a short period from the application of the first ESD pulse. Thus, three parameters can be identified for each family from these ESD stress tests, that can be better defined as follow:

- ***First level failure*** (F1 %): it represents the failure rate of each LED family after the application of a single ESD pulse;

- ***Second level failure*** (F2 %): it represents the failure rate of each LED family after the application of a second ESD pulse;

- ***Relative failure*** (F2 %/F1 %): it is defined as the ratio *Second level failure/First level failure* and it represents the failure rate of each LED family after the application of a second ESD pulse, related to the quantity of devices that have failed after the first ESD pulse. Thus this parameter estimates the failure rate after the application of two consecutive pulses, taking into account the quantity of LEDs that effectively have been submitted to the second ESD stress test.

Thus, these three parameters define the ESD robustness of analyzed LEDs in two different conditions. The values of these parameters for the 10 LED series have been provided by the manufacturer and are reported in table 6.1. Note that it has not been provided the Second level failure value for the S23 family.

6.2 Preliminary characterization of LEDs

At the beginning of work, the 10 LED series with different ESD robustness have been submitted to a preliminary electrical and optical characterization. The aim of

LED family	First level failure F1	Second level failure F2	Relative failure F2/F1
	%	%	-
S20	4.28	11.02	2.575
S21	10.89	1.60	0.147
S22	0.55	0.54	0.982
S23	7.44	-	-
S24	1.15	1.86	1.617
S25	1.19	1.07	0.899
S26	13.17	12.88	0.978
S27	18.35	56.34	3.070
S28	6.32	9.20	1.457
S29	22.33	3.81	0.171

Table 6.1: Main parameters of analyzed LED families, that identify their ESD robustness.

this preliminary characterization is to identify any correlation between the parameters defined in the previous section, i.e. First level failure, Second level failure and Relative failure, and the electrical and optical properties of LEDs. This characterization is based on current-voltage (I-V), optical power-current (L-I), capacitance-voltage (C-V) and spatially resolved eletroluminescence (EL) measurements. In the following, the main results obtained from this characterization will be presented and discussed.

6.2.1 Current-voltage (I-V) measurements

The first characterization carried out on analyzed LEDs is the current-voltage (I-V) measurement. In particular, three LEDs from each family were measured. The choice to analyze only three samples for each LED series is related to the fact that LEDs from the same family have shown a quite good uniformity in the current-voltage characteristic and thus we believe that an analysis on this number of samples is sufficient for our purposes.

The current-voltage measurements were carried out by means of a HP4155 Semiconductor Parameter Analyzer, at room temperature. In particular, the LEDs were placed in a test fixture directly connected to the instrument and the measurements were carried out in the dark, in order to limit the photogeneration induced by environmental light. The LEDs were measured both under reverse and under forward bias: in particular, the reverse voltage was limited to the value of $-30\,V$, while the

forward current was limited to the value of 100 mA. Due to the relatively low current limit adopted under forward bias, it has been sufficient to employ a two-wire configuration for the connection between LED and the parameter analyzer.

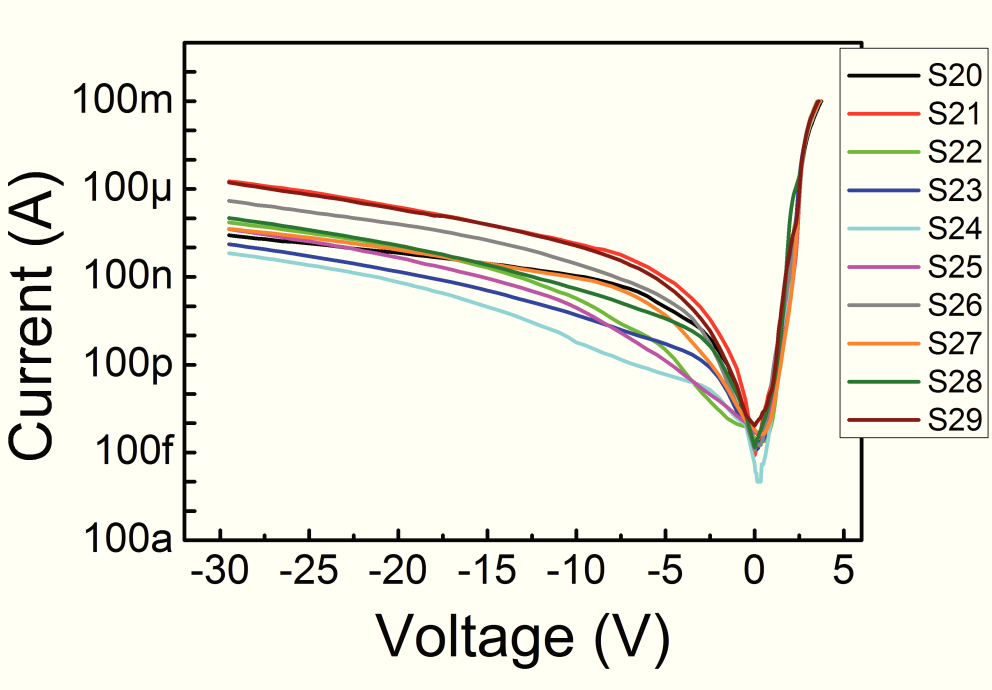


Figure 6.2: Current-voltage (I-V) characteristics of representative samples from analyzed LED families.

In Figure 6.2 it is illustrated the comparison between current-voltage curves of LEDs of the analyzed families. In particular, the characteristic of a representative sample from each LED family is reported in this plot. From the figure it can be noticed different values for the leakage current under reverse bias and also different values of the recombination current observable for low forward bias condition, indicating a different concentration of defects, dislocations and parasitic paths responsible for the leakage current conduction. Thus, this fact suggests that devices from different families differ in the layered structure or in the quality of grown layers, due for example to a different growth temperature.

At this point we have analyzed any correlation between the reverse leakage current, measured in this case at $-25\,V$, and the First level failure, Second level failure and Relative failure: we are looking for a relation between the ESD robustness described by these three parameters and the leakage current under reverse bias, because the LEDs were submitted to ESD stress test under reverse bias, as explained above, and thus the discharge current eventually flows through the preferential paths for leakage current conduction. The relations between leakage current for measured devices and the First level failure, the Second level failure and the Relative failure (that is Second level failure/First level failure) are reported

in the histograms of Figures 6.3, 6.4 and 6.5, respectively. In the histograms are reported also the corresponding values of First level failure, Second level failure and Relative failure for each LED family. Note that in Figure 6.3 the First level failure increases going towards the right side of histogram. Analogously, the Second level failure and the Relative failure increase going towards the right side of Figures 6.4 and 6.5, respectively. From these histograms, no particular correlation can be identified between the reverse-leakage current and the First level failure, the Second level failure and the Relative failure, thus suggesting that the ESD robustness of devices and the reverse-bias leakage are not correlated. This means that the presence of any defect and parasitic path responsible for the reverse conduction do not directly influence the ESD robustness of LEDs.

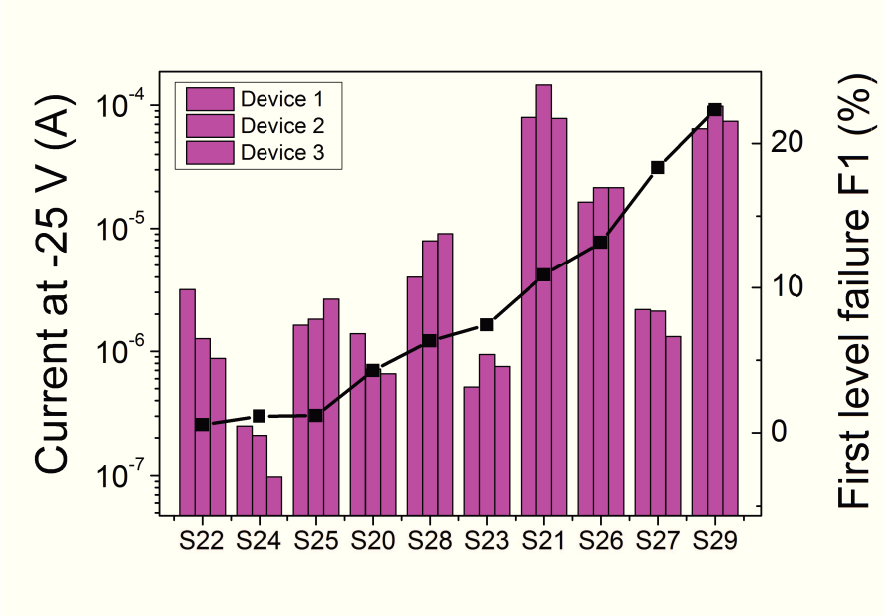


Figure 6.3: Hystogram showing the relation between First level failure and reverse leakage current measured at $-25\,V$ for the analyzed LED families.

6.2.2 Electroluminescence measurements under reverse bias

As a second step, analyzed LEDs were submitted to spatially resolved electroluminescence measurements under reverse bias. The choice of performing EL measurements under reverse bias is again related to the fact that defects responsible for emission processes occurring in this operating regime can be somehow correlated to the ESD robustness of LEDs. In fact, the high current injected during an ESD event can flow through these defects, thus determining a great localized heating in the junction and consequently the catastrophic failure of devices.

Also in this case three LEDs for each family were analyzed (in particular, they are the same submitted to current-voltage characterization). A single emission

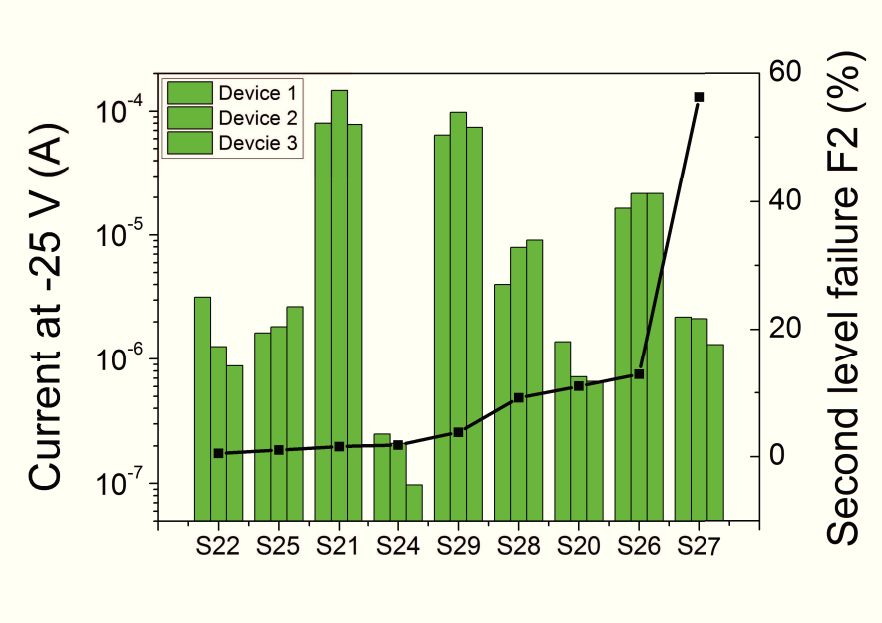


Figure 6.4: Hystogram showing the relation between Second level failure and reverse leakage current measured at $-25\,V$ for the analyzed LED families.

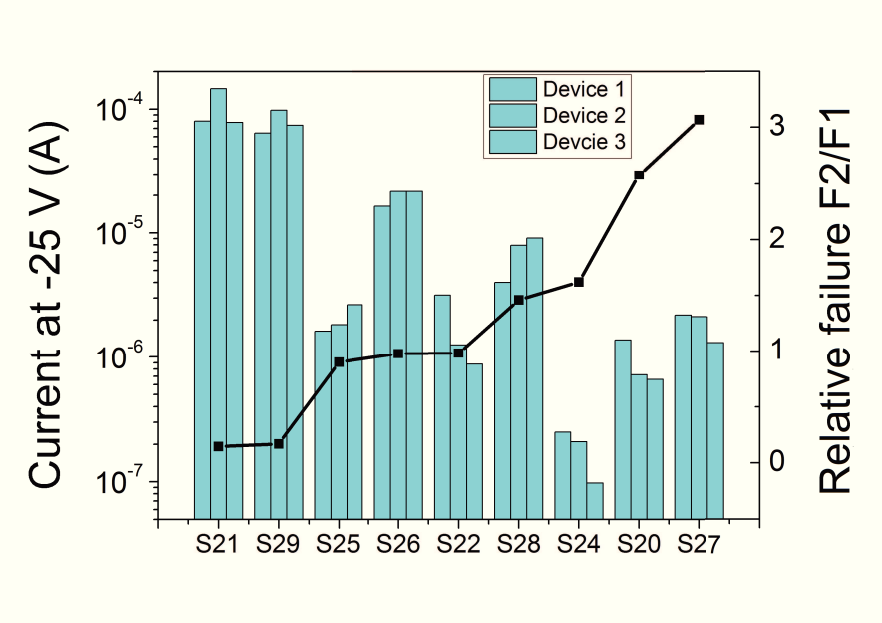


Figure 6.5: Hystogram showing the relation between Relative failure and reverse leakage current measured at $-25\,V$ for the analyzed LED families.

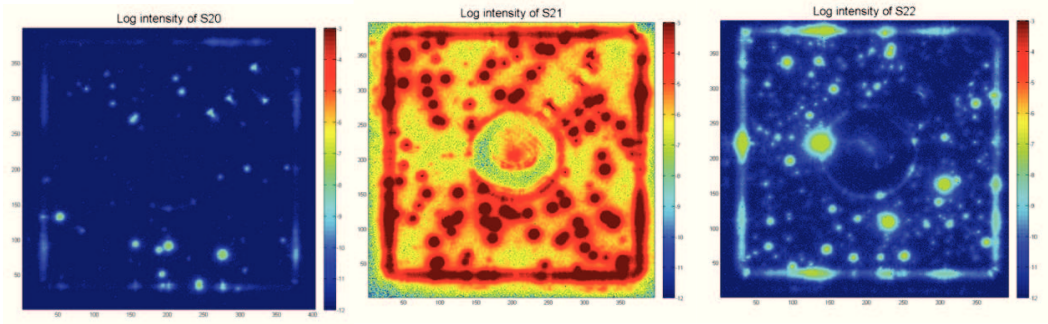
image was taken at $-30\,V$ for each LED, by means of a cooled back-illuminated charge coupled device camera *Andor LUCA* and a *Mitutoyo* optical microscope with long-working distance lenses. In particular, for our devices a 10x lens has been used. The reverse voltage on LEDs was applied by means of a *SourceMeter Keithley 2636A*. Note that the experimental setup is the same used for the *EL* characterization carried out in chapter 4, except for the fact that in this case the

monochromator is not employed, because we are interested to measure the whole emitted light from devices (i.e. at all emission wavelengths) under reverse bias, Thus, for more details the reader can refer to the experimental setup described in chapter 4.

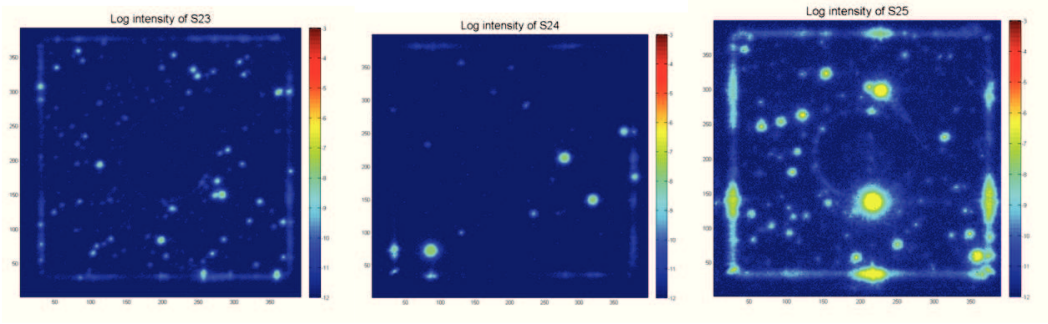
The false-color EL images taken at $-30\,V$ for a representative sample from each family are reported in Figure 6.6: several localized emitting spots can be observed in each LED. Note that all images are reported with the same intensity scale. It has been demonstrated in chapter 4 that localized spots identify the position of preferential paths responsible for the reverse-leakage conduction; in particular, the analysis carried out in chapter 4 has also revealed that the intensity and the number of luminescent dots are strongly dependent on the threading dislocation density, thus suggesting that threading dislocations act as efficient channels for reverse-bias conduction and luminescence. Based on these results, LED series showing a higher EL signal under reverse bias are thus characterized by the presence of a higher defect density, possibly threading dislocations. Note that in Figure 6.6 the intensity of images is shown in a logarithmic scale, due to the huge difference between the emission of different LED series: it is clear from the images, that some devices have a great emission under reverse bias, while others are characterized by a low luminescence signal.

In chapter 4 we have already seen that the intensity of reverse-bias luminescence is directly proportional to the injected reverse current. For this reason, we have analyzed the correlation between the EL signal measured at $-30\,V$ and the reverse leakage current measured at the same voltage level for the different LED families, obtaining the result shown in Figure 6.7: also in this case, a proportionality relation between EL signal and leakage current under reverse bias can be observed, even between LEDs of different families, which have different characteristics and structure, thus further confirming the results obtained in chapter 4.

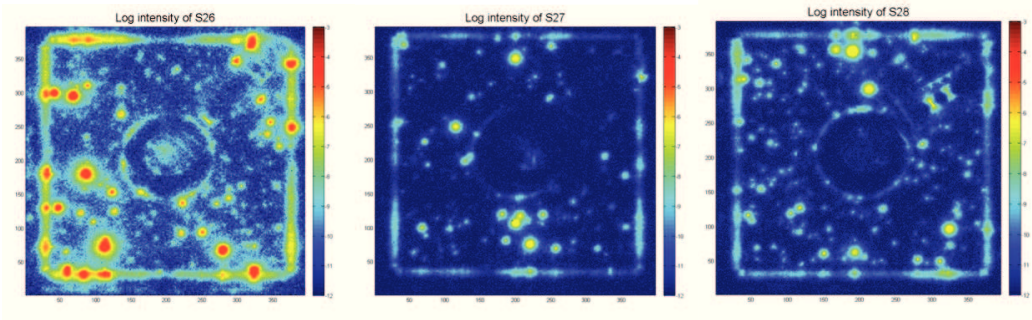
However, also in this case no correlation have been observed between the reverse luminescence and First level failure, Second level failure and Relative failure. This result can be easily understood considering this fact: the strong correlation between reverse EL signal and leakage current suggests that the defects and parasitic paths responsible for the reverse bias luminescence and reverse current-conduction are the same. In fact, as suggested in chapter 4, the luminescence originates from the injection of carriers through preferential leakage paths. On the other hand, in the previous section relative to the current-voltage characterization, we have seen that the presence of these leakage paths do not seem to be correlated to the ESD robustness of LEDs. As a consequence, also the luminescence generated by the injection of carriers trough these defective regions will not be related to the ESD robustness of analyzed devices.



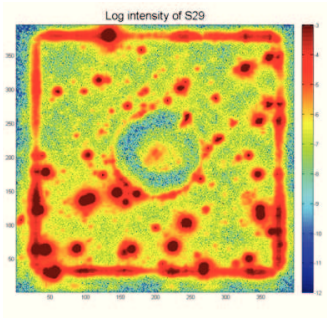
(a) S20 **(b)** S21 **(c)** S22



(d) S23 **(e)** S24 **(f)** S25



(g) S26 **(h)** S27 **(i)** S28



(j) S29

Figure 6.6: Spatially resolved false-color EL images of one of the analyzed LEDs for each family, measured at $-30\,V$. The intensity of EL images is reported in a logarithmic scale.

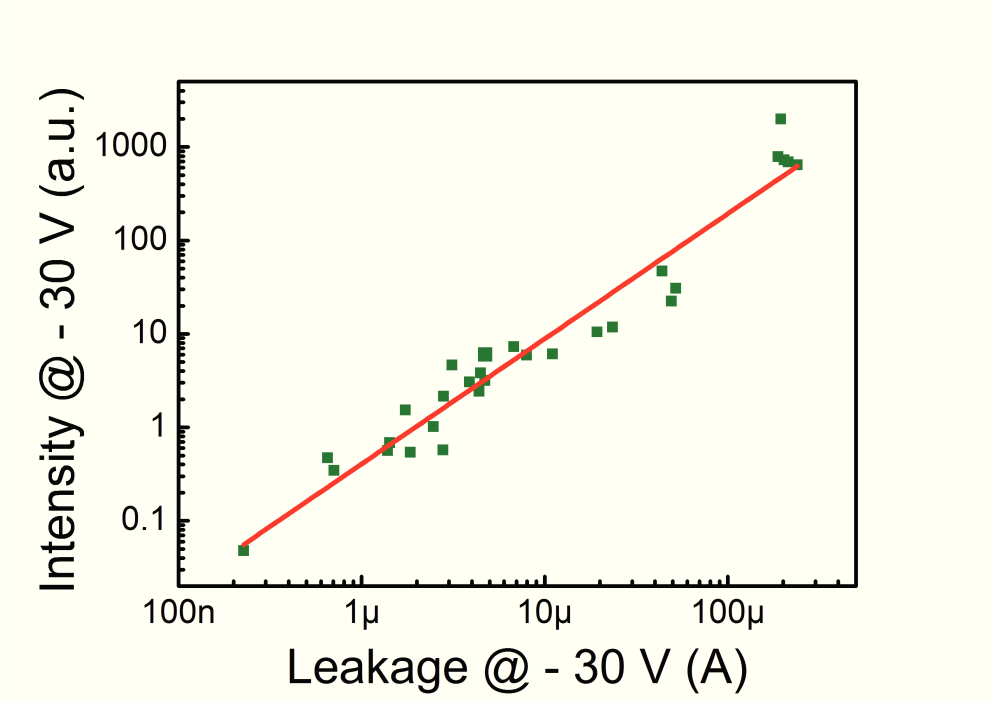


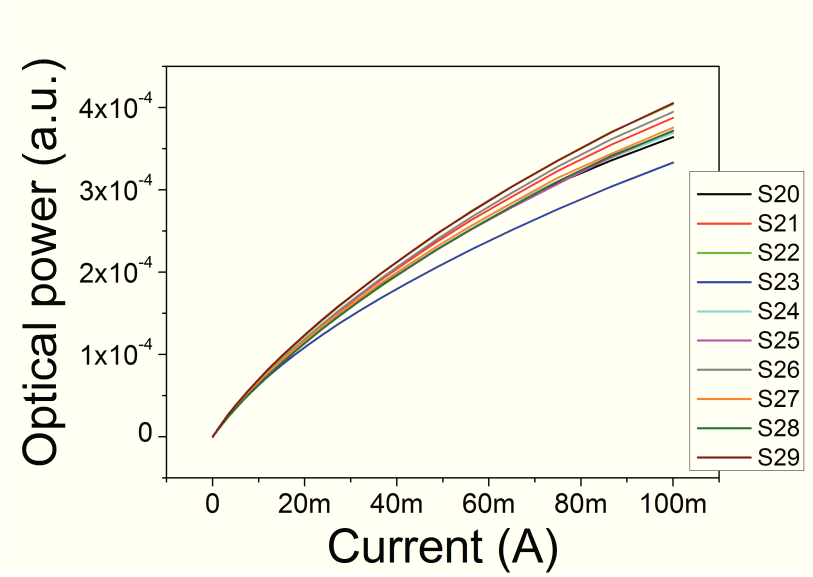
Figure 6.7: Intensity of EL signal measured at $-30\,V$ as a function of leakage current measured at the same voltage level, for different LEDs from the analyzed series. The data are represented in a log-log scale. Also the linear fit of data is reported in the figure.

6.2.3 Optical power-current (L-I) measurements

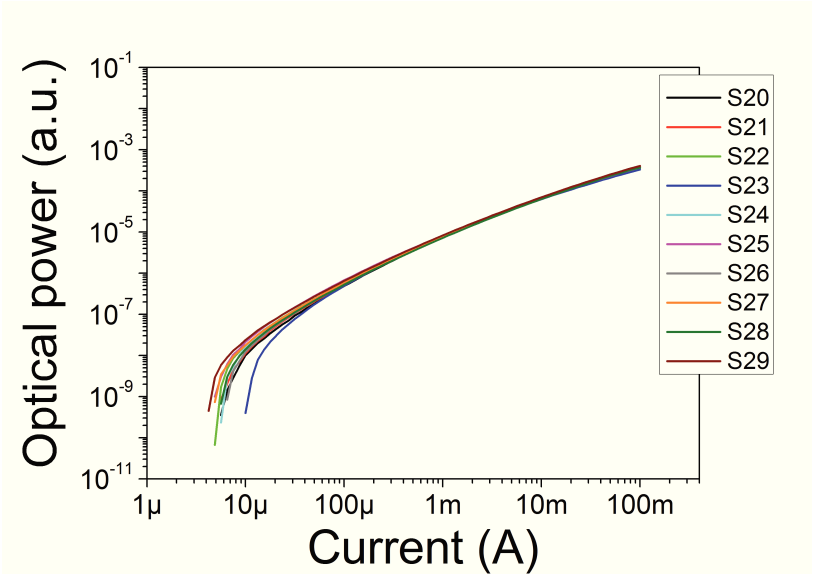
At this point, optical power-current (L-I) characterization was carried out on analyzed devices. In order to perform the measurements, the LED is biased at different current levels and the relative optical power is measured; in particular, a pulsed current is provided to the device, in order to limit the self-heating of the junction, which can strongly influence the measured optical power. The measurements were carried out by means of an integrating sphere and an *Optical Power Meter Newport 1830C*. The light emitted by the LED is collected by the integrating sphere and then it is incident on a photodiode. The photodiode is directly connected to the optical power meter, which provides a measure of the optical power emitted by LED. Note that the bias current was provided by means of a *SourceMeter Keithley 2636A*.

The results of L-I measurements for a representative sample from each LED family are reported in Figure 6.8 in a linear scale and in a log-log scale, respectively. Differences between optical power of LEDs from different families can be observed both in the low current region and in the high current region. The difference between curves in the low current region suggests a different value of the non-radiative recombination coefficient, and thus of the defect concentration between

different LED series. In fact, we can remember from section 2.4.3 that this region of *L-I* characteristic in dominated by non-radiative recombination processes. On the other hand, it is difficult to determine the physical mechanisms related to the different optical power emitted by devices at high current levels, without a knowledge of the LED structure. However, in principle, these differences can be attributed to a different extraction efficiency or a different multi-quantum well structure between LED series.



(a) *L-I* curves in a linear scale



(b) *L-I* curves in a log-log scale

Figure 6.8: Comparison between optical power-current (*L-I*) characteristics for a representative sample from each analyzed LED family. The curves are reported both in a linear and in a log-log scale.

First, we are interested to analyze the correlation between ESD robustness of LEDs and the optical power in the low current regime, because in this region of *L-I* characteristic the emission is dominated by the non-radiative recombination and thus it is influenced by the presence of defects. Our purpose is to analyze if defects that limit the optical power at low current levels can somehow influence the ESD robustness of devices. The results of this analysis are shown in Figure 6.9: the histograms report the optical power measured at an injection current of $20\,\mu A$ as a function of First level failure, Second level failure and Relative failure; in particular these three parameters increase going towards the right side of histograms. Note that no correlation can be identified between the optical power at low current levels and the First level failure, the Second level failure and the Relative failure. Thus as a result, defects responsible for non-radiative recombination under low forward bias condition do not seem to be correlated to the ESD robustness of LEDs.

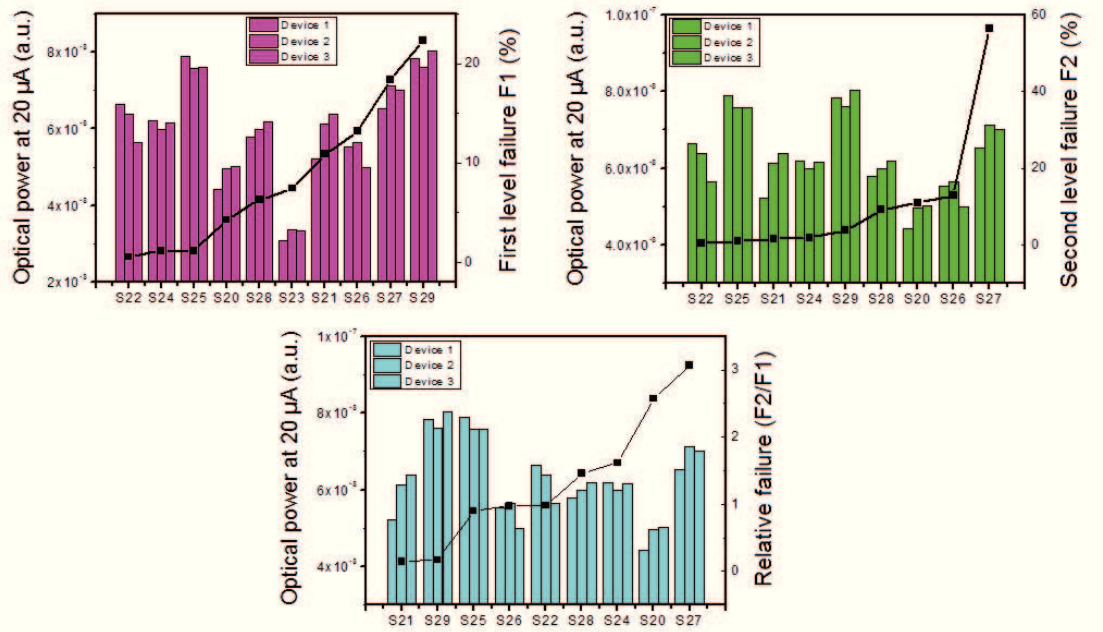


Figure 6.9: Optical power measured at an injection current of $20\,\mu A$ as a function of First level failure, Second level failure and Relative failure for LED families with different ESD robustness.

Also the correlation between ESD robustness and the optical power emitted at high current levels have been analyzed and the results are reported in the histograms of Figure 6.10, where the optical power measured at $100\,mA$ is shown as a function of First level failure, Second level failure and Relative failure. Note that also in this case no correlation can be found between the optical power under high forward bias condition and the First level failure or the Second level failure, or the Relative failure. Thus, the physical mechanisms that limit the optical power in the high current regime do not seem to be correlated to the ESD robustness of LED.

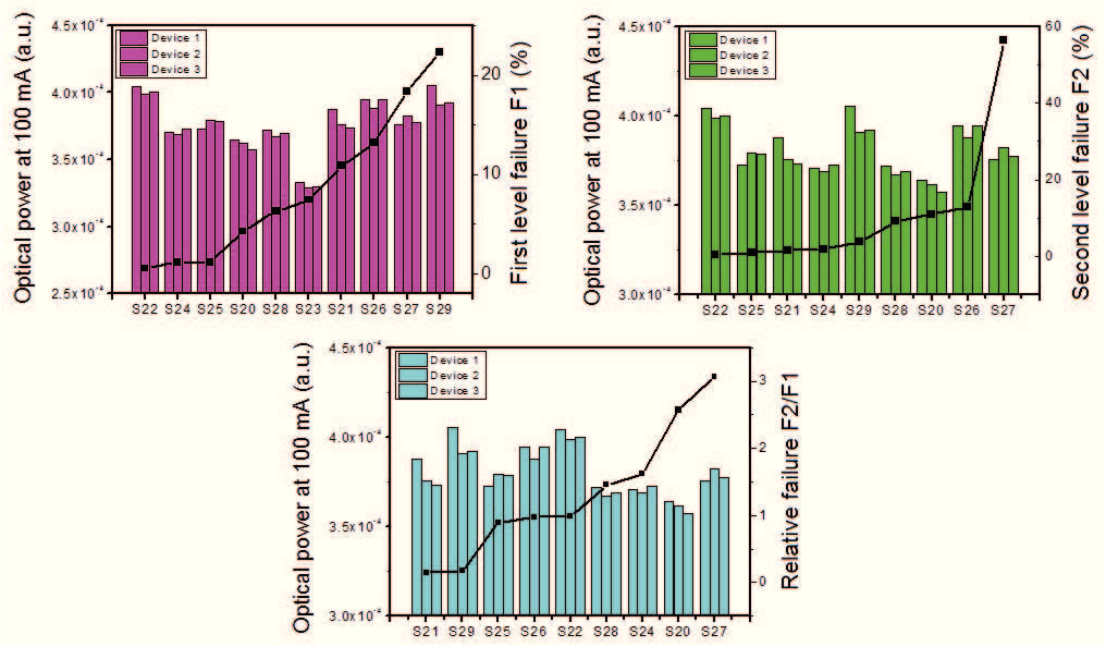


Figure 6.10: Optical power measured at an injection current of 100 mA as a function of First level failure, Second level failure and Relative failure for LED families with different ESD robustness.

6.2.4 Capacitance-voltage (C-V) measurements

Finally, to conclude this preliminary characterization, LEDs from different families were submitted to capacitance-voltage (C-V) characterization. The measurements were performed by means of a *Precision LCR Meter HP4248A*: this instrument permits to measure the impedance of devices and extrapolate the parameters of adopted model. In this case, we have used a C-G model, i.e. the LEDs were modeled by a capacitance, that represents the junction capacitance, and a parallel conductance, which represents the shunt resistance related to leakage paths. In particular, LEDs were placed in a test fixture directly connected to the instrument and the measurements were carried out in the dark, in order to limit the influence of light on the capacitance of devices. In fact, as it will be shown in the next sections, the capacitance of an LED can be strongly changed by lighting the surface of device. Note that the *LCR Meter* requires a 4-wire configuration to perform the measurement. Also the frequency of small signal can be changed between 100 Hz and 1 MHz. For our characterization, a frequency of 1 MHz for the small signal is typically used. The measurements were carried out under reverse bias and for low forward voltage levels, smaller than the threshold voltage.

The comparison between C-V measurements obtained with a frequency of 1 MHz for a representative sample from each family is shown in Figure 6.11. It is interesting to observe that some LED families show very similar C-V curves to each other: this is the case of families S21 and S29, or S22 and S25. Also

families S20 and S27 have similar C-V curves, as well as S23 and S24. On the other hand, families S26 and S28 have not similar characteristic to any other LED series. In particular, from the figure we can observe that all C-V curves shows a monotonic increasing trend. Furthermore, the steps of curves indicate the presence of a different charge accumulation or depletion regions.

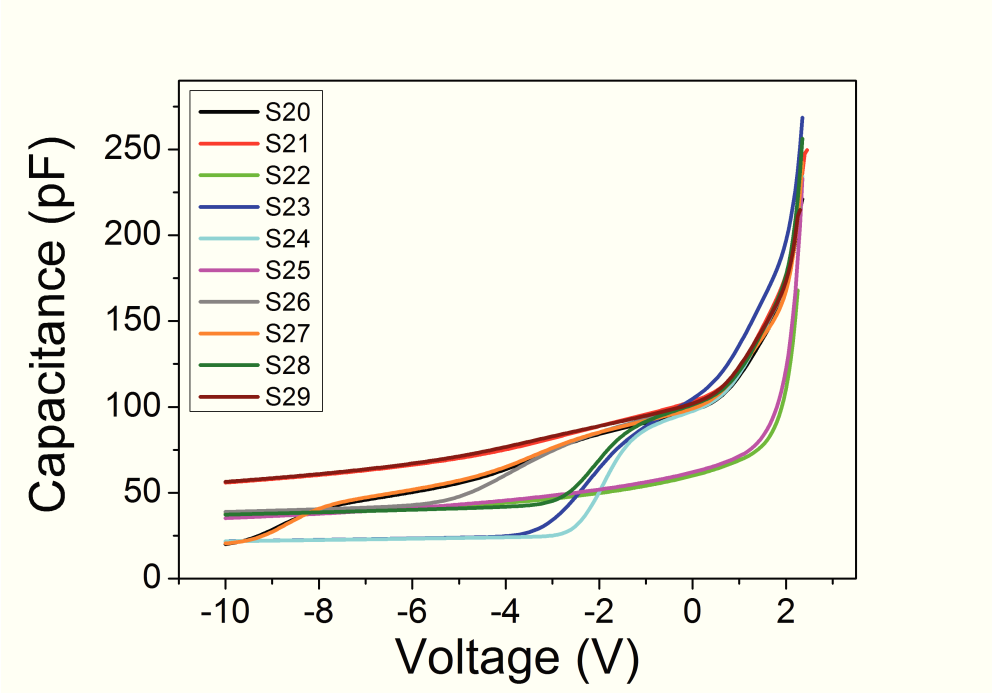


Figure 6.11: Comparison between C-V characteristics obtained at 1 MHz for a representative LED from each analyzed family.

In Figure 6.12 is shown the corresponding apparent charge distributions of analyzed LEDs, obtained from the C-V characteristics reported in Figure 6.11, by using the equation (2.52). Note that these apparent charge distributions were obtained assuming a p^+n junction structure for all LEDs. Obviously this is not verified in the reality and thus the values of charge and in particular of depletion width may not be exact. However, these curves permit us to obtain some approximate information about the layered structure of devices. In particular, from these apparent charge distributions we can obtain a consistent comparison between LED from different series. From the Figure 6.12 some interesting features can be observed:

1. LED families with similar C-V characteristics show also similar apparent charge distribution. This means that LEDs with similar C-V curves have also a similar layered structure. However, it can be demonstrated that LED families with similar structure do not necessarily show similar First level failure, Second level failure or Relative failure.

2. Most of LED families show a charge peak near the junction, which can be attributed to the presence of a quantum well: this fact suggests that LED families probably have a similar multiple quantum well structure as active region.

3. LED families show different layered structure far from the junction, with different position and doping level in the barrier layers.

However, note that the information provided by Figure 6.12 are not sufficient to determine any correlation between the ESD robustness and the structure of analyzed LEDs, such as presence of particular layers, of different growth temperature, or doping levels in different layers.

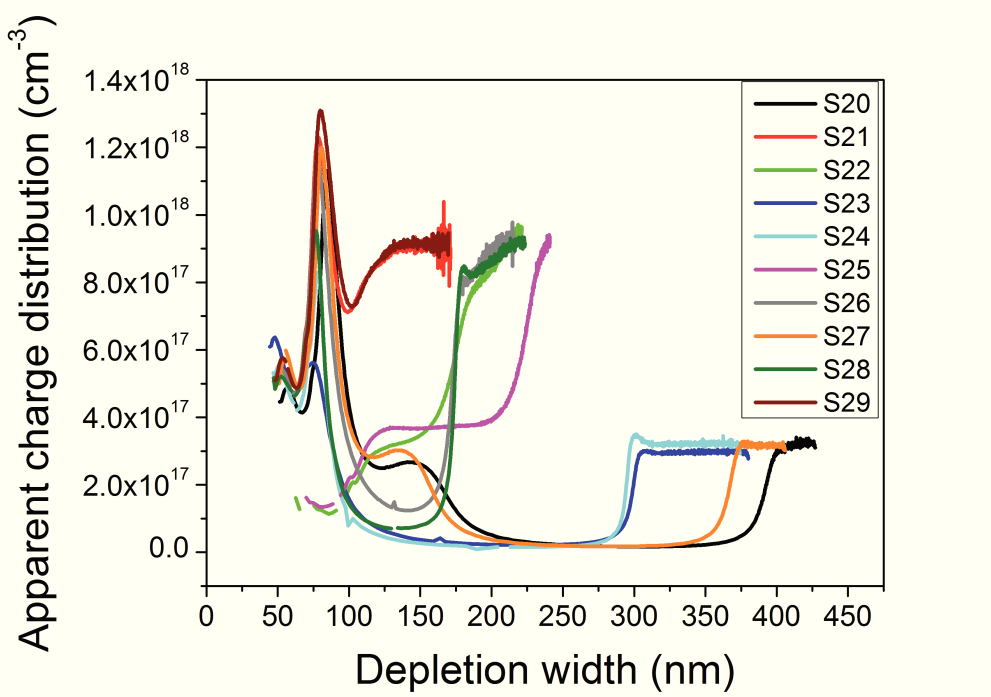


Figure 6.12: Comparison between apparent charge distributions obtained at 1 MHz for a representative LED from each analyzed family.

At this point, also in this case we have studied any correlation between the capacitance of LEDs and their ESD robustness. A very interesting result has been obtained from the analysis of C-V curves represented in Figure 6.13: light green curves are referred to families with high First level failure, while dark green curves are referred to LED series with low First level failure. Note that, as suggested in the inset of figure, devices with a higher capacitance show a lower ESD robustness; conversely, devices with a lower capacitance show a higher ESD robustness. This may be due to the fact that for the same intrinsic potential, a higher capacitance may imply a greater electric field.

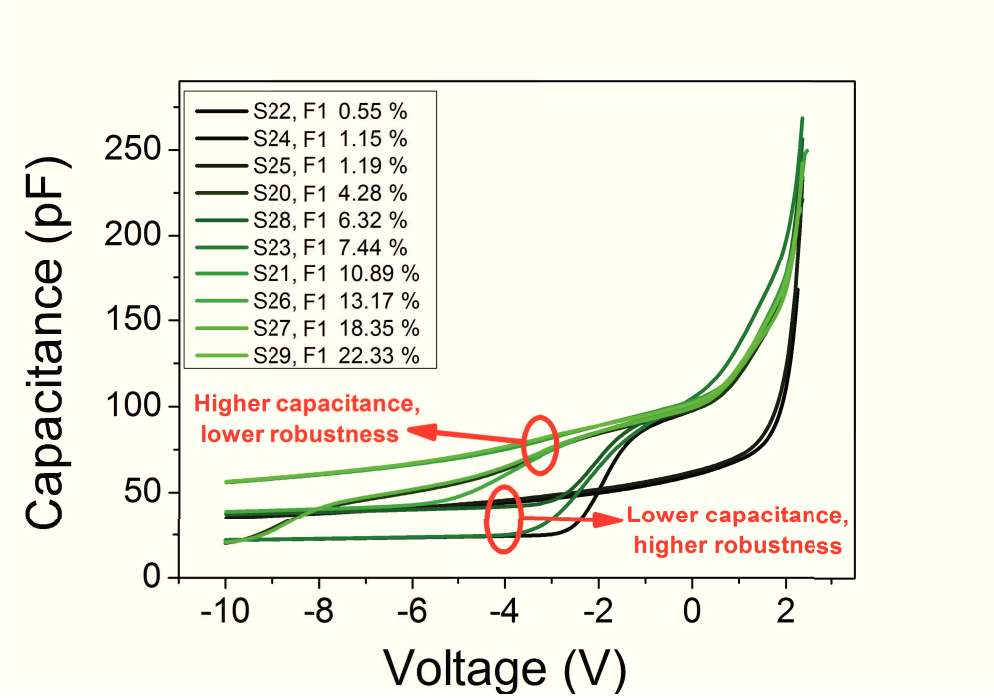


Figure 6.13: Comparison between C-V characteristics obtained at 1 MHz for a representative LED of each analyzed family. Light green curves are referred to devices with lower ESD robustness, while dark green curves are referred to LEDs with higher ESD robustness.

Based on the result obtained above, also the integral over the voltage of C-V curves has been calculated for each family. In particular, note that this integral represents the charge accumulated within the junction. The relation between C-V integral, and thus the total charge in the junction, and the First level failure is reported in the plot of Figure 6.14. It can be noticed a strong correlation between the total charge accumulated in the junction and the First level failure. A possible interpretation of this correlation is given by the fact that a higher junction capacitance, and thus a higher charge accumulated in the junction, induces the formation of a higher electric field, that can negatively influence the ESD robustness of LEDs. In particular, the maximum electric field can reach very high values when the LED is submitted to as ESD event under reverse bias, thus causing the catastrophic failure of device.

On the other hand, any particular correlation has been found between the total charge accumulated in the junction and the Second level failure or the Relative failure (i.e. Second level failure/First level failure), as shown in Figure 6.15. (Note that the Figure 6.15(a) seems to show a linear relation between charge Q and Second level failure, but the position of points S21 and S29 confirms that in reality this relation does not exist). Thus, a higher internal electric field seems to strongly influence the ESD robustness of LEDs when submitted to a first ESD event, but it

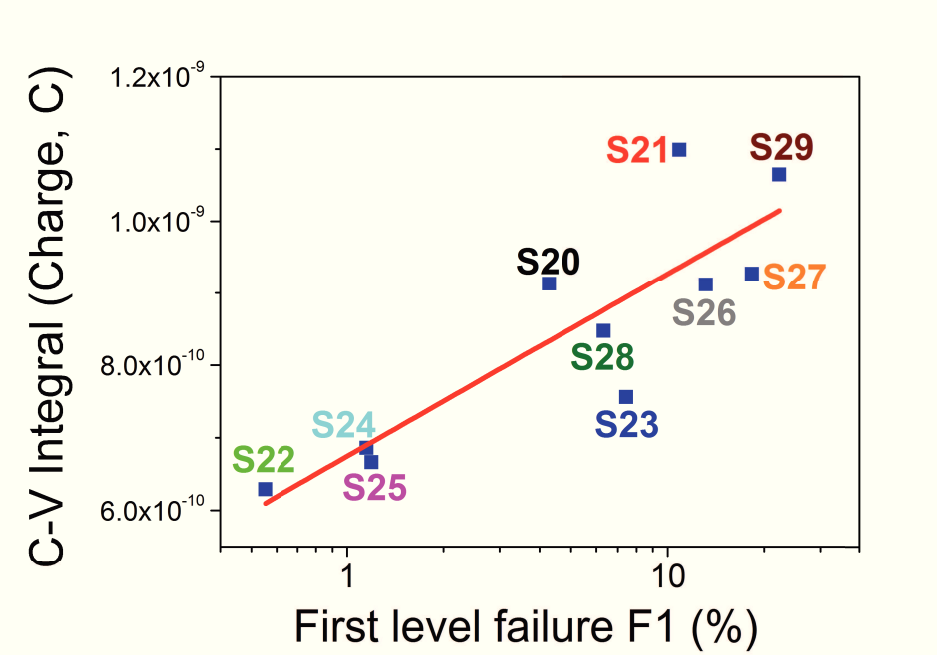


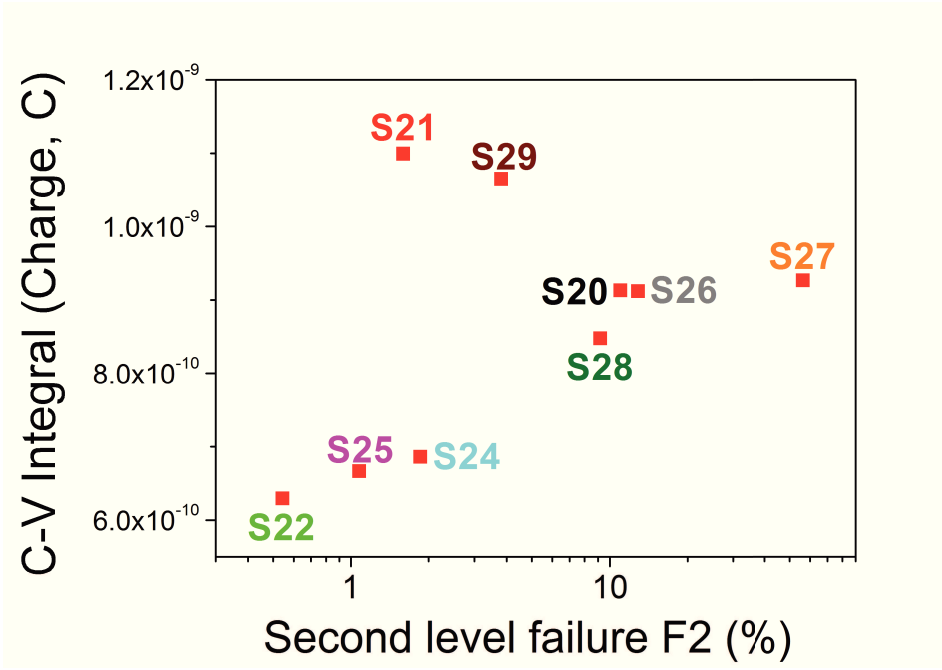
Figure 6.14: Relation between the total charge Q accumulated in the junction, obtained as integral of the C-V curve, and the First level failure of LEDs of different families.

does not seem to influence the ESD characteristics of devices when a second ESD pulse is applied after a short time.

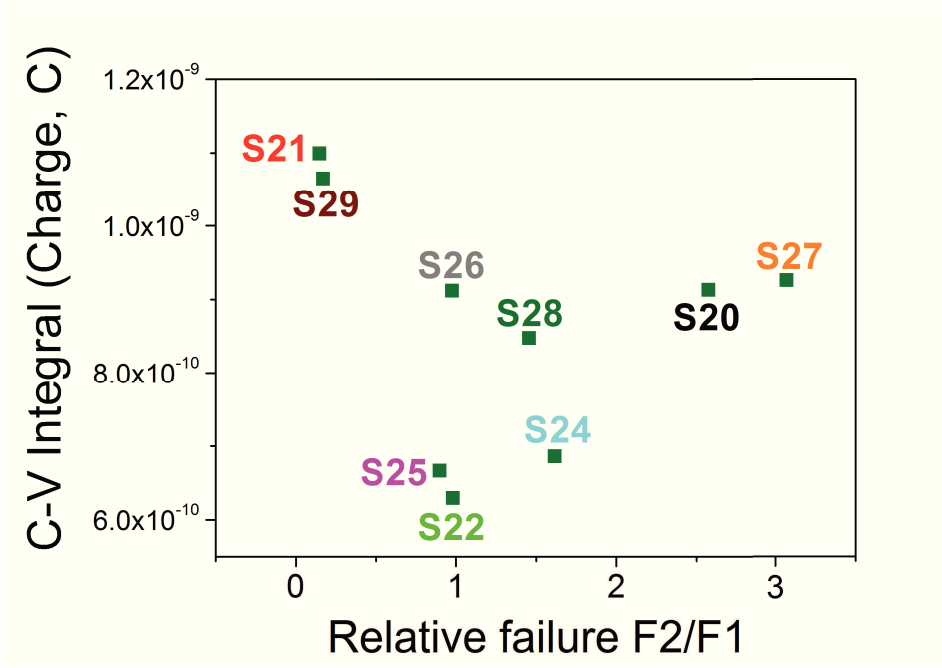
In order to study in more detail the physical mechanisms that limit the ESD robustness of LEDs when two consecutive ESD events are applied to devices, and thus the correlation with Second level failure and Relative failure, a different characterization method is needed. In the next sections we will present the results of an extensive characterization of defects present in analyzed LED structures, based on slow capacitance transient, deep level optical spectroscopy (DLOS) and deep level transient spectroscopy (DLTS) measurements.

6.3 Slow capacitance transient measurements

The preliminary electro-optical characterization has provided useful information only about the correlation between First level failure and the overall junction capacitance of LEDs. However, it is necessary to deeply understand the origin of Second level failure and/or Relative failure, i.e. the physical mechanisms that influence the ESD robustness when a second ESD pulse is applied after a short time from the first one. For this reason, an extensive analysis of deep levels present in the devices was carried out and the results will be reported in this and in the next sections. Note that the analysis is based on capacitance transient measurements, carried out by means of different techniques, because the junction capacitance of



(a) Relation with Second level failure



(b) Relation with Relative failure

Figure 6.15: Relation between the total charge Q accumulated in the junction, obtained as integral of the C-V curve, and (a) the Second level failure and (b) the Relative failure (i.e. Second level failure/First level failure) of LEDs of different families.

an LED is strongly influenced by trapping phenomena occurring via deep levels.

The first step of deep level characterization is to analyze the variation of junction capacitance when the device is submitted to a non-destructive ESD event: this

characterization is also called ***slow capacitance transient*** measurement. In the following of this section, the theory of this measurement and the experimental results obtained from analyzed LEDs will be presented.

6.3.1 Slow capacitance transient theory and experimental details

To perform a ***slow capacitance transient*** measurement, the junction capacitance of LED is continuously measured over the time and at a certain instant t a quasi-ESD pulse is applied under reverse bias to the device, i.e. a pulse with a duration greater than typical ESD events, in the order of a few ms, and amplitude much lower than that of a real ESD event, in the order of some tens of volts. This quasi-ESD pulse simulates an ESD event that reaches the device under reverse bias. The choice of generating such a type of pulse is related to the fact that with conventional ESD systems, such as a Transmission Line Pulser, it is not possible to control with high precision the amplitude of generated pulses. Thus, we have employed a conventional pulser, that can generate voltage pulses with lower amplitude. However, with a higher pulse duration, an energy with the same order of magnitude as a real ESD event can be transferred to the device, even if its amplitude is much lower. Also a constant reverse bias V_{rev} can be applied to the analyzed LED, in order to measure the variation of junction capacitance at different voltage levels, which corresponds to different depletion widths within the junction. Furthermore, due to the strong dependence of capacitance from temperature, the device is placed on a thermally controlled stage in the dark, in order to obtain a capacitance transient independent from temperature variations.

In our characterization, a *Boonton 7200 Capacitance Meter* have been used to measure the variation of junction capacitance: in particular, this instrument has a very high resolution, in the order of 1 fF and can measure the capacitance applying a small signal with a frequency of 1 MHz. This very high resolution can be obtained by means of the bridge configuration adopted in the capacitance meter: in such a type of connection the instrument measures the difference between the junction capacitance of LED and that of a reference capacitor (note that the reference capacitor is adjustable) and thus, it can measure this capacitance variations with very high precision and in a very small range.
A reverse bias of $V_{rev} = -10\,V$ was applied to the device by means of a *SourceMeter Keithley 2636A*. After several preliminary measurements, this voltage level has been identified as the optimum bias that maximizes the capacitance transient after the application of an ESD pulse. To better understand this fact, the reader can refer to Figure 6.16, that shows the apparent charge distributions of analyzed LED families as a function of reverse voltage: as it can be observed, a reverse bias of $-10\,V$

corresponds to a depletion layer edge localized far from the multiple quantum well region and near or inside the barrier layer in the n-type region. Considering that the capacitance transient is typically related to trapping phenomena, and thus to the presence of defects, this fact suggests that a high concentration of deep states is localized in this region of the junction for the analyzed LED families. Alternatively, this can be due to the fact that the high concentration of mobile charge present in proximity of quantum wells prevents the capacitance meter from measuring with precision the capacitance variations induced by trapping phenomena.

At a certain instant t, a pulse voltage V_{fill} under reverse bias with a duration of

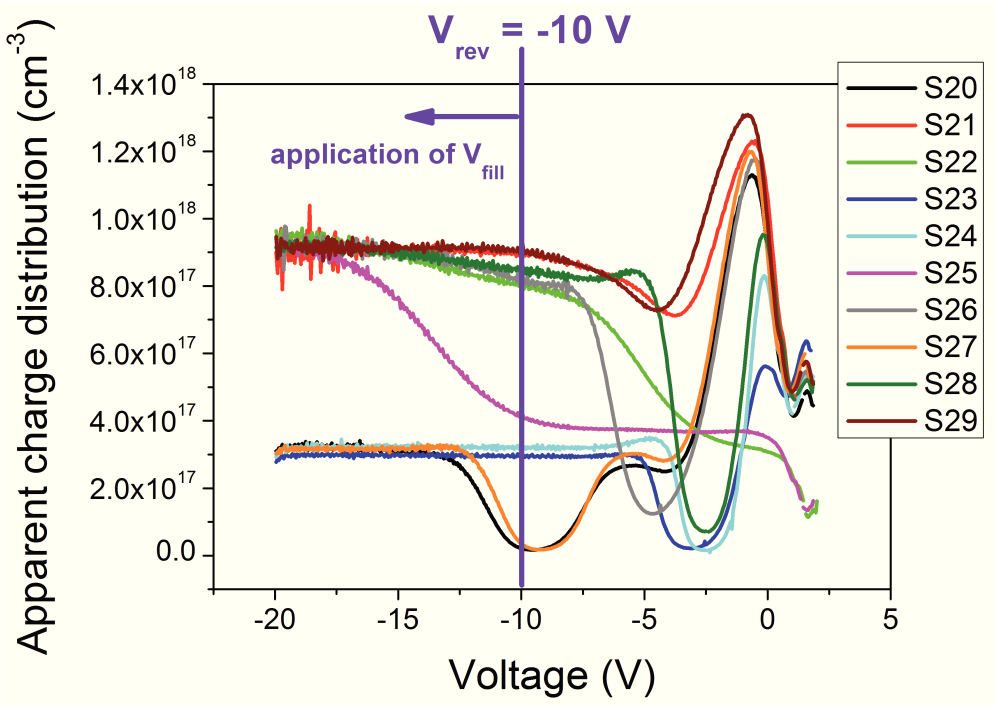


Figure 6.16: Comparison between apparent charge distributions as a function of applied voltage for a representative sample from each LED family. Note the depletion layer edge when a voltage of $V_{rev} = -10\,V$ is applied.

6 ms is applied to LED under test. Due to the different structure between LED families, several criteria can be chosen, in order to determine the voltage level of the pulse. For our analysis, the chosen criterion is to apply a voltage level V_{fill}, which corresponds to a reverse current during quasi-ESD event of $I_{fill} = -1\,mA$. This choice is related to the fact that the ESD failure threshold of a LED depends on the current level injected in the junction during ESD event, which can induce a great localized heating and eventually the catastrophic failure of device. Since each LED family is characterized by a different electrical characteristic, in order to obtain a pulse current of -1 mA, different voltage levels must be applied in each LED series. In particular, the pulse voltages applied to each family are reported in Table 6.2.

Also the quasi-ESD pulse is applied by means of the *SourceMeter Keithley 2636A*.

LED family	V_{fill} $(t = 6\,ms)$
S20	-100 V
S21	-40 V
S22	-62 V
S23	-90 V
S24	-100 V
S25	-72 V
S26	-53 V
S27	-100 V
S28	-57 V
S29	-40 V

Table 6.2: Voltage level V_{fill} applied during quasi-ESD pulse under reverse bias on each LED family, in order to obtain a pulse current of -1 mA.

In particular, the pulse is superimposed to the constant reverse bias V_{rev}, in order to obtain a correct result from measurement. A schematic of the evolution over the time of the applied voltage to the LED during the measurement is reported in Figure 6.17.

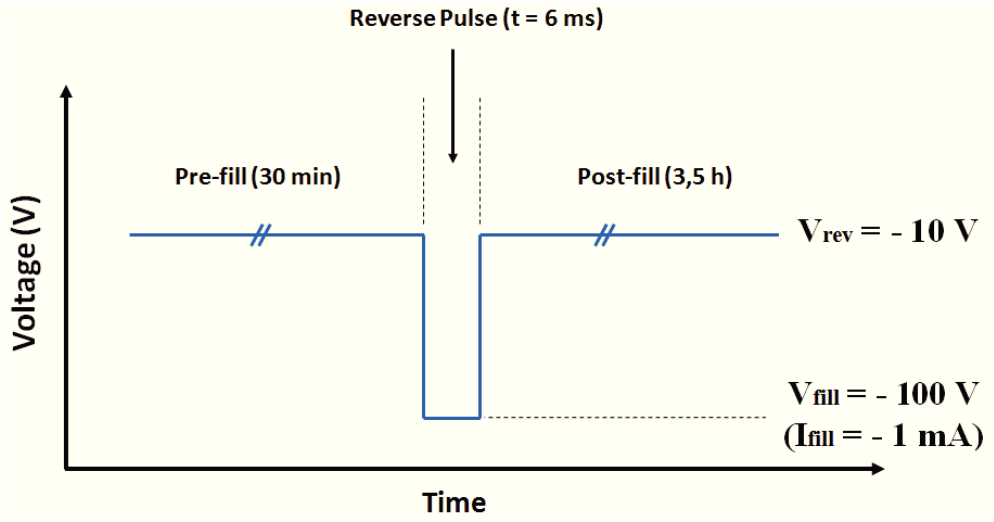


Figure 6.17: Evolution of LED applied voltage over the time, during the slow capacitance transient measurement.

When a quasi ESD-pulse is applied under reverse bias to a LED, a temporarily broadening of the depletion layer with respect to the steady-state condition, corresponding to the bias voltage V_{rev}, can be observed. Suppose now that one or more

deep levels are present within the energy gap in proximity of the depletion layer of the junction: when the reverse pulse is applied and the space charge region is broadened, the state of the traps will change. After the application of pulse, the depletion width will return to the initial value and the initial equilibrium condition in the semiconductor will be recovered. However, if the trap levels are located very deep within the energy gap, they cannot recover instantly the initial occupancy state: as a consequence, a variation in the junction capacitance will be temporarily observed. In particular, the capacitance will increase or decrease with respect to the initial value and this fact depends on several factors, including the type of semiconductor (n-type or p-type) and the type of trap, i.e. if it is a majority carriers trap or a minority carriers trap.

In our analysis we will refer to a p^+n junction, thus supposing that the space charge region will extend only in the n-side. As a consequence, we will refer only to n-type semiconductors to analyze the traps. However, our considerations can be easily extended to a p-type semiconductor. A typical slow capacitance transient obtained from analyzed LEDs is shown in Figure 6.18: as it can be observed, the pulse application have induced a positive capacitance transient, i.e. an increase in the junction capacitance (note that the pulse is applied at the time 0.5 h in the figure). In particular, a positive capacitance transient indicates the presence of a majority carrier trap (electrons in our case, with a n-type material), while a negative capacitance transient indicates a minority carrier trap (hole in our case). It is interesting to observe that the trap recovers the initial condition in a very long time, in the order of some hours: this fact suggests that the trap states are localized very deep inside the bandgap.

A possible interpretation of the trapping phenomenon occurring during and after the application of a quasi-ESD pulse is provided by the band diagrams of a p^+n junction shown in Figure 6.19, which are referred to different instants of slow capacitance transient measurement. With reference to the figure, that shows the n-side of the junction, E_D represents the energy of a donor level, E_T is the energy of a deep level localized within the gap and E_{Fn} is the quasi-Fermi level on the n-side. In particular, we suppose that far from the junction the trap level E_T is below the Fermi level. Moreover, we suppose that this trap is neutral when is occupied by electrons and positively charged when is empty. The evolution of band diagram can be explained as follow, referring to the same figure:

- Figure 6.19(a) represents the initial equilibrium condition: it can be observed that the donor and trap states localized above the Fermi level are empty (indicated as "+" in figure). The limit of depletion layer is localized at the edge of empty donors.

- Figure 6.19(b) shows the band diagram during the pulse application. As a

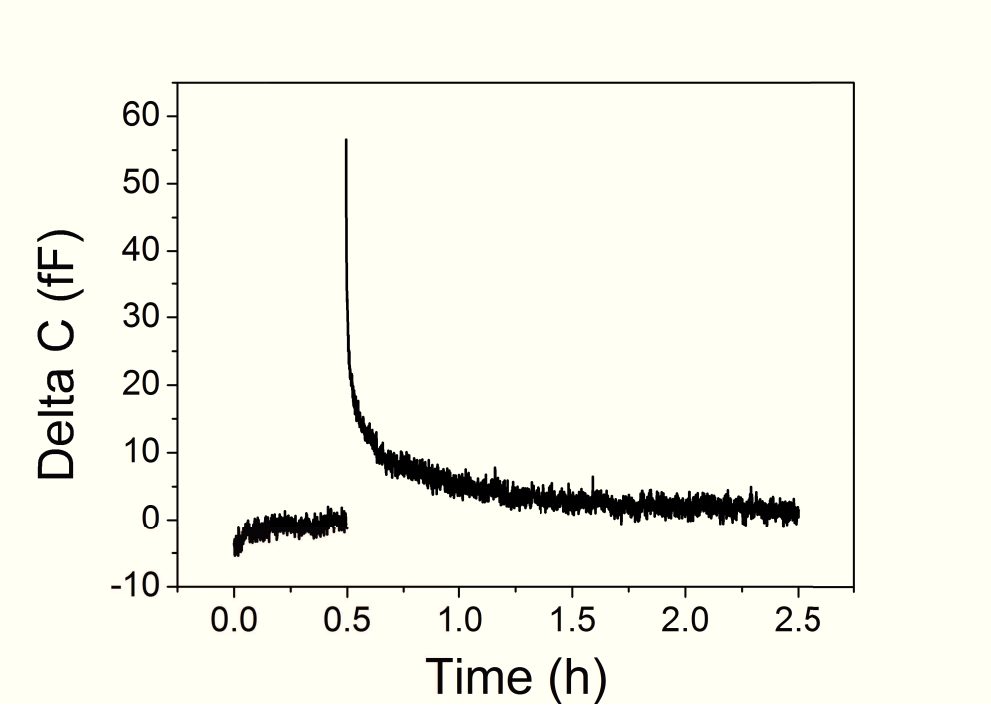


Figure 6.18: Typical capacitance transient generated after the application of a reverse quasi-ESD pulse in one of the analyzed LEDs.

consequence of applied bias, the band bending increases, with the result that more donors and trap states are empty of electrons.

- Figure 6.19(c) represents the condition after a short time from the pulse application, when the junction is recovering the initial condition. However, empty trap states are not able to instantly capture an electron, due to their deep position within the bandgap. As a consequence, in order to verify the charge neutrality principle, fewer donors are ionized (the charge on the p-side is equal to the initial value, because we suppose that the deep level is localized only in the n-side): this results in a narrowing of the space charge region and thus in a increase of the junction capacitance with respect to the initial value.

- Figure 6.19(d) shows the band diagram after a certain time from the pulse application. Because this is not the equilibrium condition, with the increasing of time the trap states will be able to capture electrons and correspondingly more donors will be ionized, in order to maintain the charge neutrality. As a consequence the depletion layer will extend and the capacitance will decrease towards the equilibrium value.

- Finally, after an enough long time, the initial condition will be completely recovered, as shown in Figure 6.19(e).

Note that in the previous considerations it has been assumed that the emission rate of electrons from trap states is much higher than the capture rate of electrons. Furthermore, this analysis can be easily extended to the case of a p-type semiconductor, or to a minority carrier trap.

From this presentation of slow capacitance transient measurement, it is clear that this experimental setup is in principle very similar to the DLTS setup[1], except for the fact that in this case V_{fill} is "more negative" with respect to V_{rev}, while in classical DLTS V_{fill} is usually "more positive" than V_{rev}, and the duration of measure is much longer than in typical DLTS. For this reason, we have called this measurement as *slow capacitance transient*. Furthermore, it is clear that this experimental setup is very useful to study the presence of impurity states localized very deep within the bandgap, which cannot be revealed with a classical DLTS system. In the following of this section we will present the results of slow capacitance transient analysis carried on LED families with different ESD robustness.

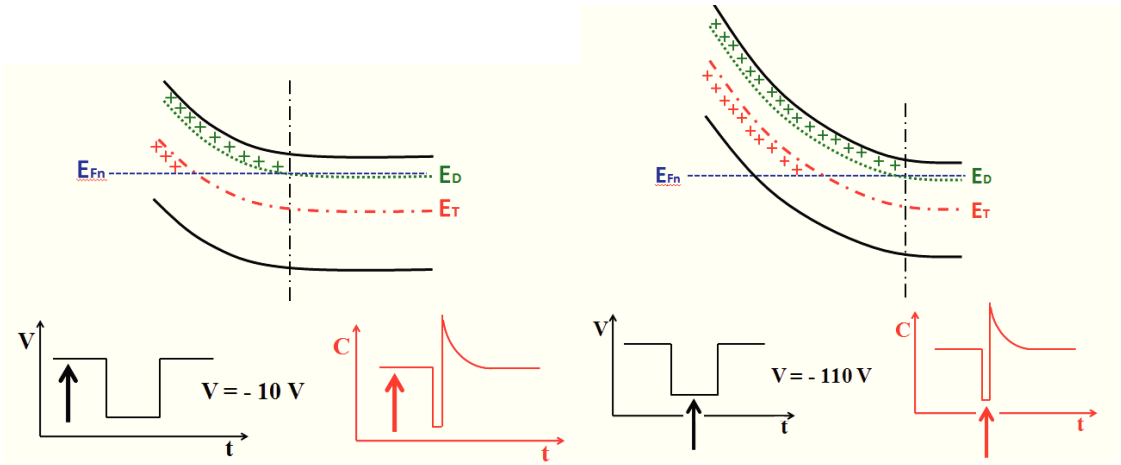
6.3.2 Results and discussion

The slow capacitance transient technique described above has been used to study the presence of deep levels inside the bandgap of LEDs with different ESD robustness, in order to identify any correlation between the presence of impurity states and First level failure, Second level failure and Relative failure. A comparison between the capacitance transients obtained from a representative LED for each family is reported in Figure 6.20, with the time axis both in a linear scale and in a logarithmic scale. Note that the comparison have been done between the *Delta C/C* quantity, instead of *Delta C* and only in this case the comparison between LED families can be considered consistent. This is due to the fact that each analyzed LED has a different background capacitance at the voltage V_{rev} and from the theory of DLTS, which is applicable in this case, it results that the trap density responsible for capacitance transients is proportional to the quantity Delta C/C, than rather Delta C. From the same figure it can be also noticed that capacitance transients do not follow an exponential trend: in fact, from a careful analysis, it can be demonstrated that more than one time constant is related to these transients.

At this point, the correlation between Delta C/C measured at the time $t = 0$ in Figure 6.20, which represents the amplitude of capacitance transients, and the ESD robustness has been analyzed. The results are reported in Figures 6.21 and 6.22 for the relation with First level failure, Second level failure and Relative failure, respectively.

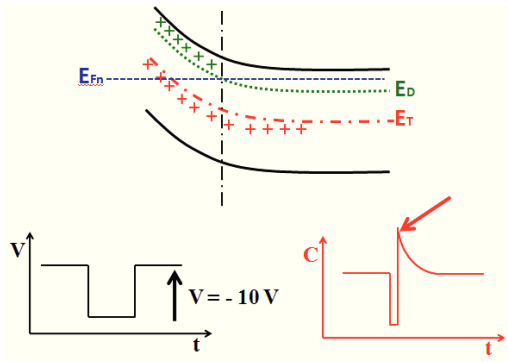
No correlation can be observed between the amplitude of capacitance transients and First level failure or Second level failure, as it can be noticed in Figure 6.21.

[1]The DLTS theory will be presented in the next sections

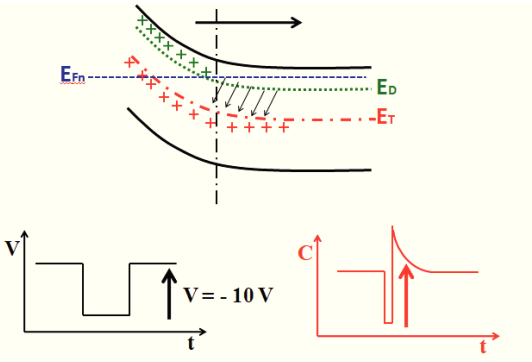


(a) Before pulse application.

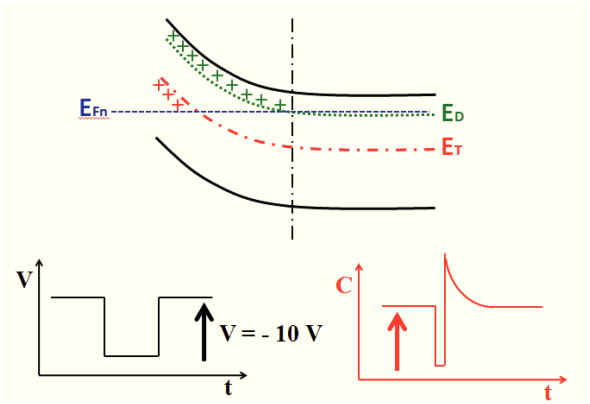
(b) During pulse application.



(c) At the end of pulse application.

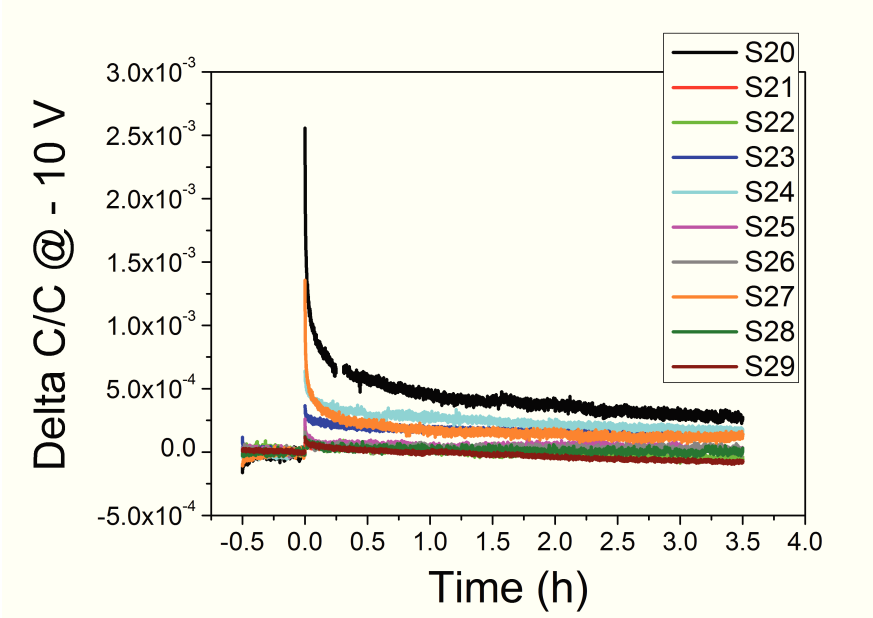


(d) The junction is recovering the initial condition.

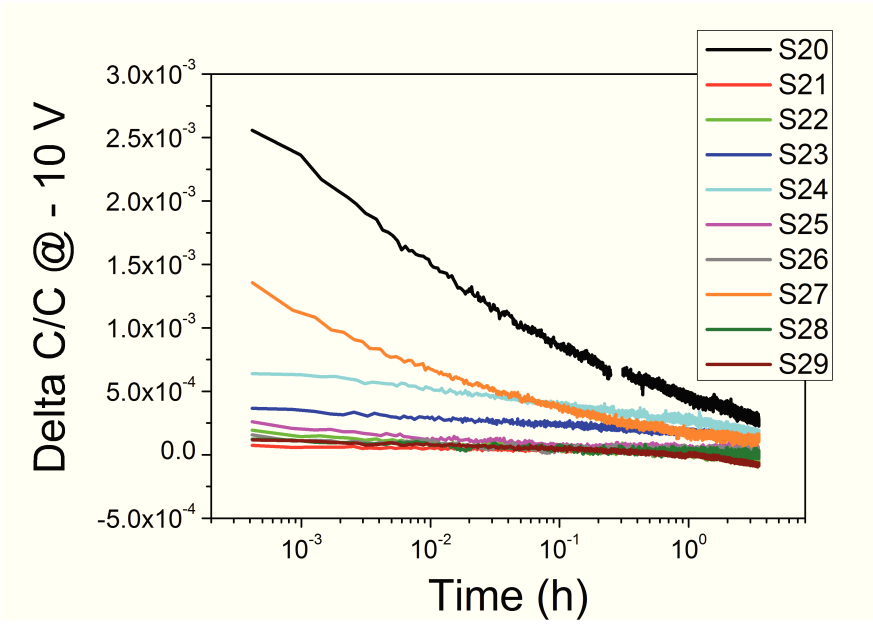


(e) The initial condition is completely recovered.

Figure 6.19: Evolution of band diagram during a slow capacitance transient measurement for a p^+n junction characterized by the presence of a majority carrier trap localized very deep within the bandgap. The figure shows only the band diagram of n-side.



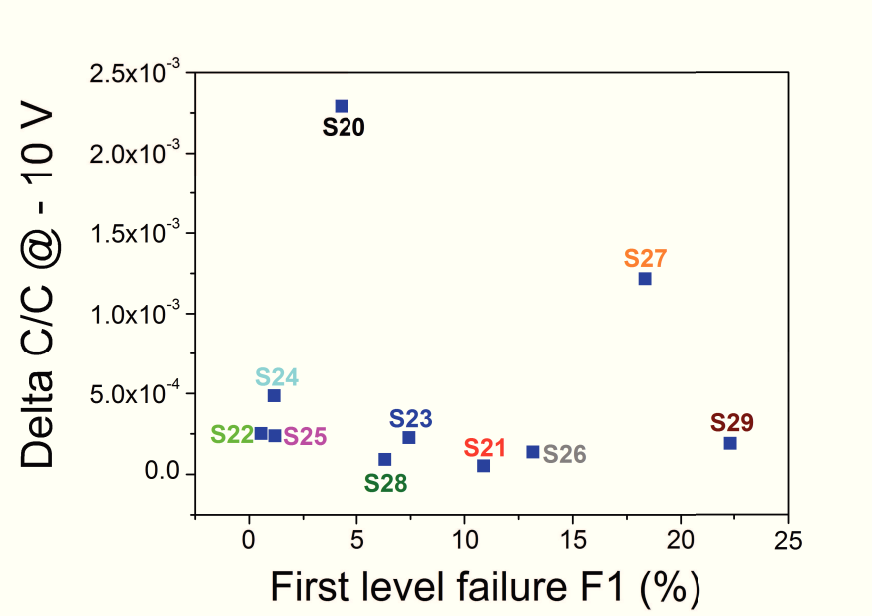
(a) Time axis in a linear scale.



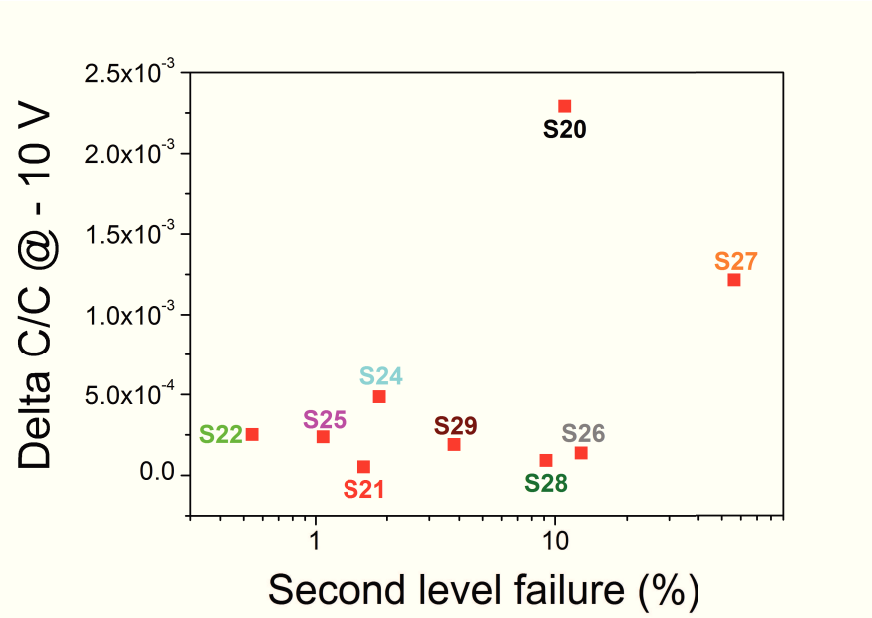
(b) Time axis in a logarithmic scale.

Figure 6.20: Comparison between slow capacitance transients measured for a representative sample from each LED family. These transients were measured with a $V_{rev} = -10\,V$. A pulse with a duration of 6 ms and amplitude V_{fill} equal to values reported in Table 6.2 has been applied during the measurements.

On the other hand, a strong correlation can be observed in Figure 6.22, as suggested also by the red line, between Delta C/C and the Relative failure. Thus, remembering that Delta C/C is proportional to trap density, the Relative failure, which represents the ESD robustness of LEDs when submitted to a second ESD pulse after a short time from the first one, is possibly related to the presence of



(a) Correlation with First level failure.



(b) Correlation with Second level failure.

Figure 6.21: Delta C/C as a function of First level failure and Second level failure for analyzed LED families with different ESD robustness.

donor traps. In fact, LED families with a higher trap density seem to show a higher ESD sensitivity when submitted to two consecutive ESD pulses. A possible interpretation of this phenomenon is the following: if we consider the reverse bias pulse applied during slow capacitance transient measurement as the first ESD pulse, we can see that the temporary change of trap states makes devices more susceptible to a new ESD event applied after a short time. This effect in particular is more

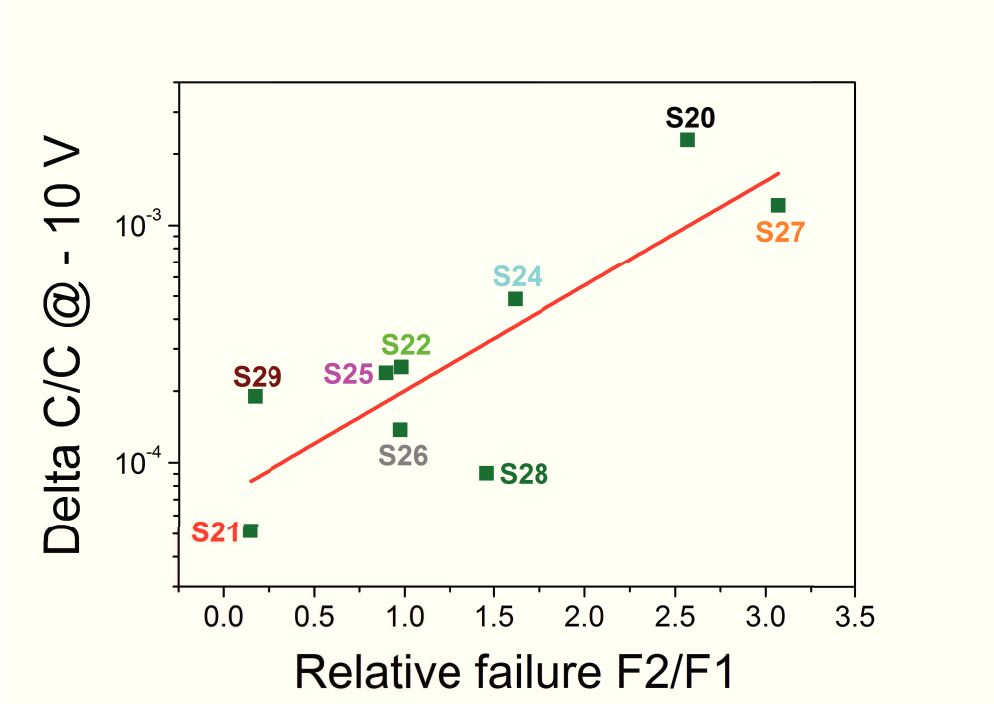


Figure 6.22: Delta C/C as a function of Relative failure for analyzed LED families with different ESD robustness.

prominent in LEDs with a higher trap density. Note also that the Relative failure is a more indicative parameter with respect to Second level failure for the failure rate after the application of a second ESD pulse, because it takes into account of the percentage of samples that effectively have passed the first ESD stress test and thus, that have been submitted to the second ESD stress test.

Also the effects of a positive pulse with respect to the bias level V_{rev} on capacitance transients have been analyzed. In order to do this, a voltage pulse with a duration of 10 ms and amplitude V_f "more positive" with respect to the bias level V_{rev} have been applied after a short time from the application of quasi-ESD reverse pulse[2]. A schematic of the voltage evolution during a slow capacitance transient with application of a forward pulse is shown in Figure 6.23. The bias level V_{rev} and the amplitude and duration of quasi-ESD pulse are the same used in the measurements presented above.

The slow capacitance transients obtained for several amplitudes of the forward pulse are reported in Figure 6.24: as it can be noticed, with a bias level $V_{rev} = -10\,V$, a forward pulse with an amplitude $V_f = -5\,V$ and duration 10 ms is sufficient to completely annihilate the capacitance transient, and thus the trapping effect, induced by reverse quasi-ESD pulse. This phenomenon can be explained considering that a "more positive" pulse with respect to the bias level V_{rev} induces

[2]Note that the amplitude of forward pulse V_f is not necessarily greater than zero

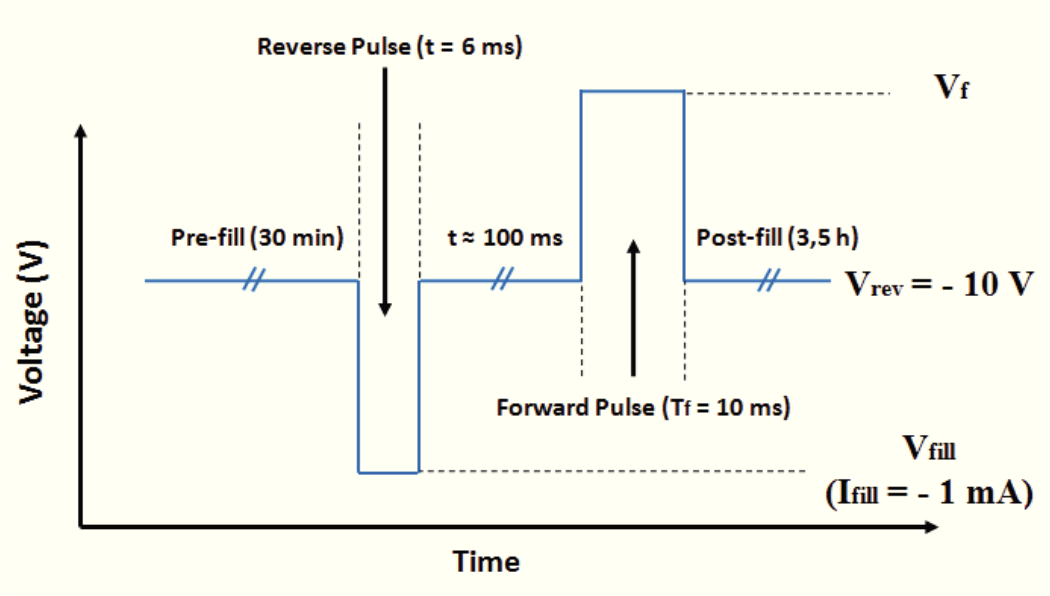


Figure 6.23: Evolution of applied voltage on LED over the time, during the slow capacitance transient measurement with application of a forward pulse.

a narrowing of space charge region: as a consequence, more free electrons are now available in the region of empty trap states, thus increasing the capture rate of deep levels. This results in a faster recovery of initial condition in the junction. Note also from the same figure, that a greater forward pulse can even induce a negative capacitance transient: this is due to the fact that in such a condition the contribution on junction capacitance of forward pulse is dominant with respect to that of the reverse pulse. In fact, as we will see in the section dedicated to DLTS measurements, a pulse amplitude V_f greater than the bias level V_{rev} induces a negative transient in the presence of a majority carrier trap, i.e. a trap for electrons in the n-side, as in our case.

The slow capacitance transient measurements have allowed us to identify the presence of deep levels within the bandgap of analyzed LEDs, which induce trapping phenomena. In particular, we have seen that these trapping phenomena are correlated to the ESD robustness of devices, by means of the Relative failure parameter. However, this technique does not provide any information about the activation energy of traps and thus of their position within the bandgap. For this reason, a further type of characterization is required, in order to determine the position of trap states in the gap. The classical DLTS technique cannot reveal these deep levels, because they are not thermally activated. In fact, maximum activation energy that can be revealed from a DLTS system is in the order of 1 eV, i.e. a deep level, for majority carriers for example, localized 1 eV below the conduction band edge. On the other hand, the deep levels responsible for slow capacitance transients have probably a higher activation energy than 1 eV, as suggested by the

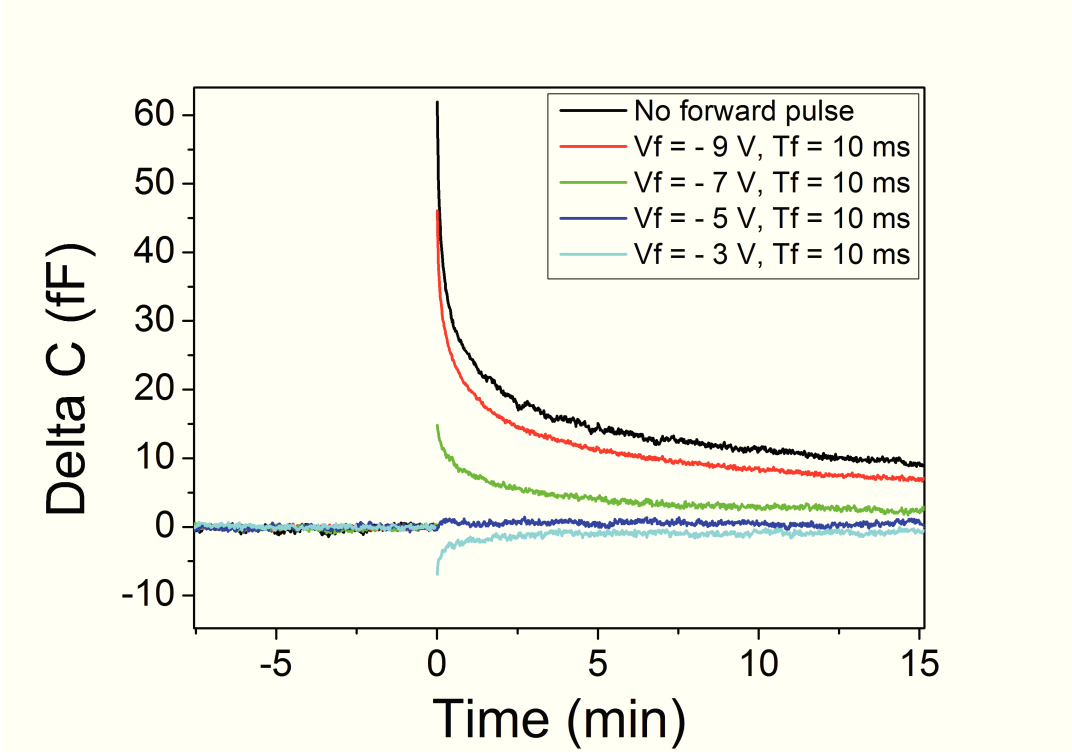


Figure 6.24: Slow capacitance transients obtained with different amplitudes of forward pulse, for a representative sample of analyzed LED families.

very slow transients generated by them. A possible way to estimate the activation energy and density of these trap states is represented by the Deep Level Optical Spectroscopy (DLOS) technique, which will be discussed in more detail in the next section.

6.4 *DLOS* measurements

Deep Level Optical Spectroscopy technique (also called *Optical DLTS*) is used to identify the presence of deep levels with a very high activation energy, and thus that cannot be revealed by means of classical DLTS technique, because they are not thermally activated. In particular, with DLOS measurements it is possible to extract the optical characteristics of a deep level, represented by the spectral dependence of the optical cross section $\sigma_o(h\nu)$, also called PCS, and by the Steady-State Photocapacitance (SSPC) characteristic [119]. In this section, first the DLOS theory and the experimental setup used for this measurement will be explained. Afterwards, the results of DLOS analysis carried out on LED series with different ESD robustness will be presented. In particular, also the correlation between deep levels responsible for slow capacitance transients and those detectable with DLOS technique, will be analyzed.

6.4.1 DLOS theory and experimental details

The experimental setup of Deep Level Optical Spectroscopy system is similar to that of slow capacitance transient measurements, except for the fact that in DLOS measurements the emission from a deep level is excited by a monochromatic light source, than rather a reverse quasi-ESD pulse. Thus, also in this case the capacitance is continuously measured over the time, by means of a *Boonton 7200 Capacitance Meter*, with a small signal frequency of 1 MHz, and together a bias level V_{rev} is applied across the LED by means of a *SourceMeter Keithley 2636A*, in order to investigate the variation of junction capacitance in proximity of different regions of active and barrier layers. At a certain instant t the LED surface is illuminated with a monochromatic light source: as a consequence, electrons or holes trapped in a deep level will be excited in the conduction or valence band by the absorption of photons and a variation in the junction capacitance will be observed. The capacitance will increase or decrease, depending on the type of trap; in particular a positive variation of the capacitance corresponds to the emission of majority carriers from the trap level, while a negative variation of capacitance corresponds to minority carrier emission from deep level. When the LED capacitance under illumination reaches the steady-state value, the light source is turned off: at this point the initial value of capacitance will be recovered over the time. A schematic of temporal evolution of the DLOS measurement is reported in Figure 6.25.

In our analysis a bias level V_{rev} of -10 V was applied to each analyzed LED, in

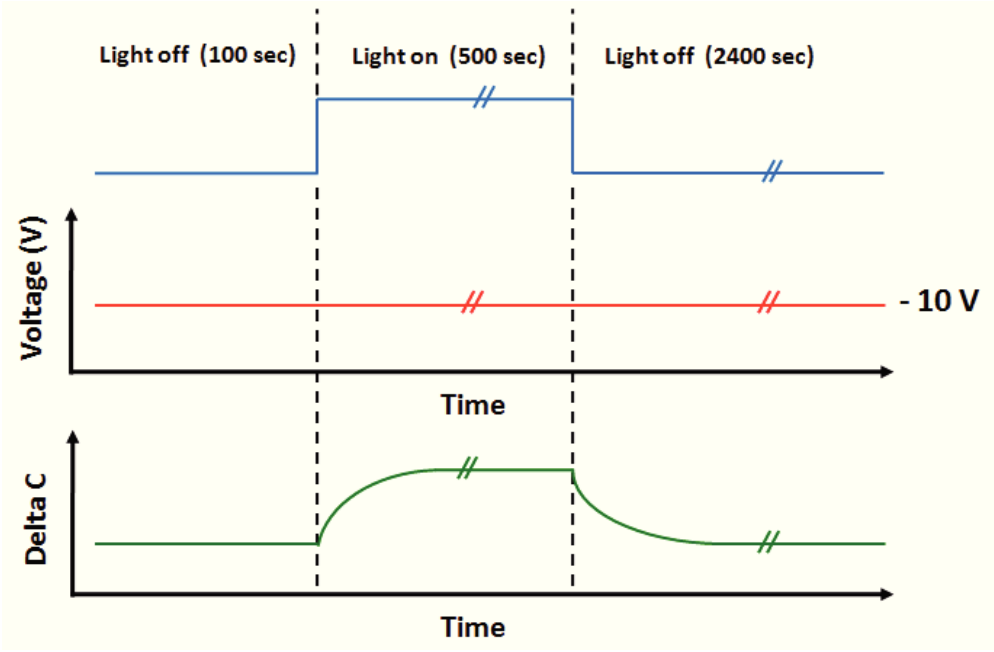


Figure 6.25: Schematic of temporal evolution of DLOS measurement.

order to give a consistent comparison with data obtained from slow capacitance

transient measurements. In the following we will refer to a p^+n junction with a majority carrier trap localized in the n-side (i.e. a trap for electrons). However, these concepts can be easily extended to a minority carrier trap or to a p-type semiconductor. A possible interpretation of trapping phenomena described above is provided by the band diagrams reported in Figure 6.26, which are referred to different instants of deep level optical spectroscopy measurement. With reference to the figure, that shows the n-side of the junction, E_D represents the energy of a donor level, E_T is the energy of a deep level localized within the bandgap and E_{Fn} is the quasi-Fermi level on the n-side. In particular, we suppose that far from the junction the trap level E_T is below the Fermi level. Moreover, we suppose that this trap is neutral when is occupied by electrons and positively charged when is empty. The evolution of band diagram can be explained as follow, referring to the same figure:

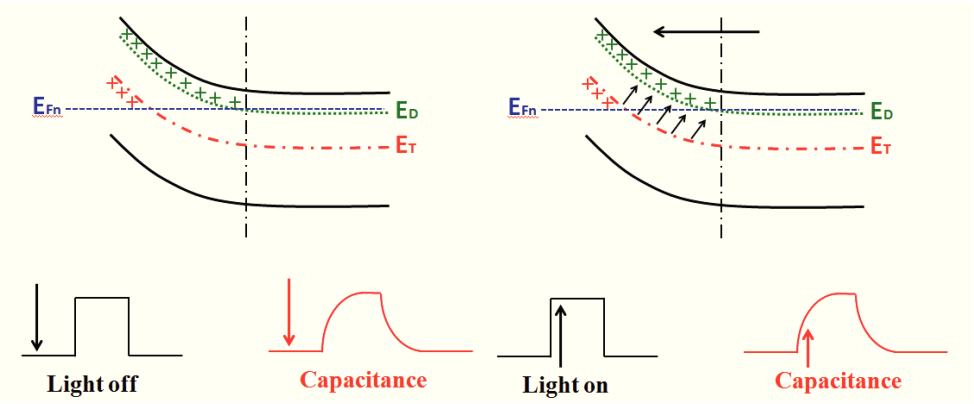
- Figure 6.26(a) represents the initial equilibrium condition: it can be observed that the donor and trap states localized above the Fermi level are empty (indicated as "+" in figure). The limit of depletion layer is localized at the edge of empty donors.

- Figure 6.26(b) shows the band diagram during the illumination. As a consequence of photexcitation, electrons trapped in the deep level E_T are excited in the donor level or in the conduction band by the absorption of photons.

- Figure 6.26(c) represents the steady-state condition under illumination. Due to photoexcitation, more trap states are empty. As a consequence, in order to verify the charge neutrality principle, fewer donors are ionized (the charge on the p-side is equal to the equilibrium value, because we suppose that the deep level is localized only in the n-side): this results in a narrowing of depletion layer and thus in a increase of the junction capacitance with respect to the initial value.

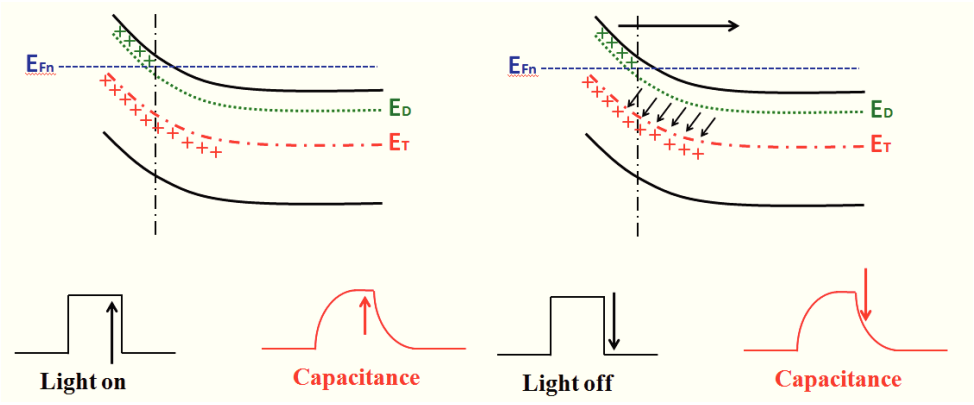
- Figure 6.26(d) refers to the band diagram after a short time by the turning off of the light. Because this is not the equilibrium condition, with the increasing of time the trap states will be able to capture electrons and correspondingly more donors will be ionized, in order to maintain the charge neutrality. As a consequence, the depletion layer will extend and the capacitance will decrease towards the equilibrium value. However, empty trap states are not able to instantly capture an electron, due to their deep position within the bandgap, and thus a certain time will be required to recover the initial condition.

- Finally, after an enough long time, the initial condition will be completely recovered, as shown in Figure 6.26(e).



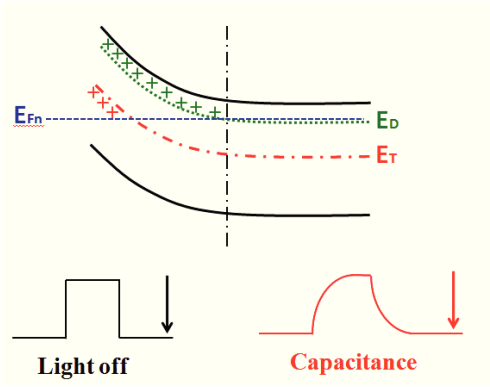
(a) Before turning on the light.

(b) The light has just been turned on.



(c) The capacitance under illumination has reached the steady-state value.

(d) The light has just been turned off.



(e) The initial condition is completely recovered.

Figure 6.26: Evolution of band diagram during a deep level optical spectroscopy (DLOS) measurement for a $p^{+}n$ junction characterized by the presence of a majority carrier trap localized very deep within the bandgap. The figure shows only the band diagram of n-side.

Note that in the previous considerations it has been assumed that the optical emission rate of electrons from trap states is much larger than the capture rate of electrons.

The monochromatic light is generated by means of a 50 W quartz-halogen lamp, which provides an illumination range spanning from the near-IR to visible, and a monochromator. Long pass optical filters on an automated filter wheel are used to cut out higher order modes that can excite further electrons from trap states, thus influencing the correct result of measurement. Finally, the light is focused on the sample by means of a lens. The light on sample is turned on and off by means of an automated mechanical shutter. Furthermore, also in this case the device is placed on a thermally controlled stage, in order to obtain a capacitance transient independent from temperature variations.

The DLOS procedure described above was performed at different wavelengths of incident light, in the range between 300 nm and 1000 nm, with a step of 10 nm. A typical DLOS transient, obtained from a representative sample, is reported in Figure 6.27. Note in particular the long times required in order both to reach the steady-state value under illumination and to recover the initial condition when the light is turned off: this suggests that the trap states responsible for the capacitance variation under illumination and detectable with the DLOS technique are very deep within the bandgap of semiconductor.

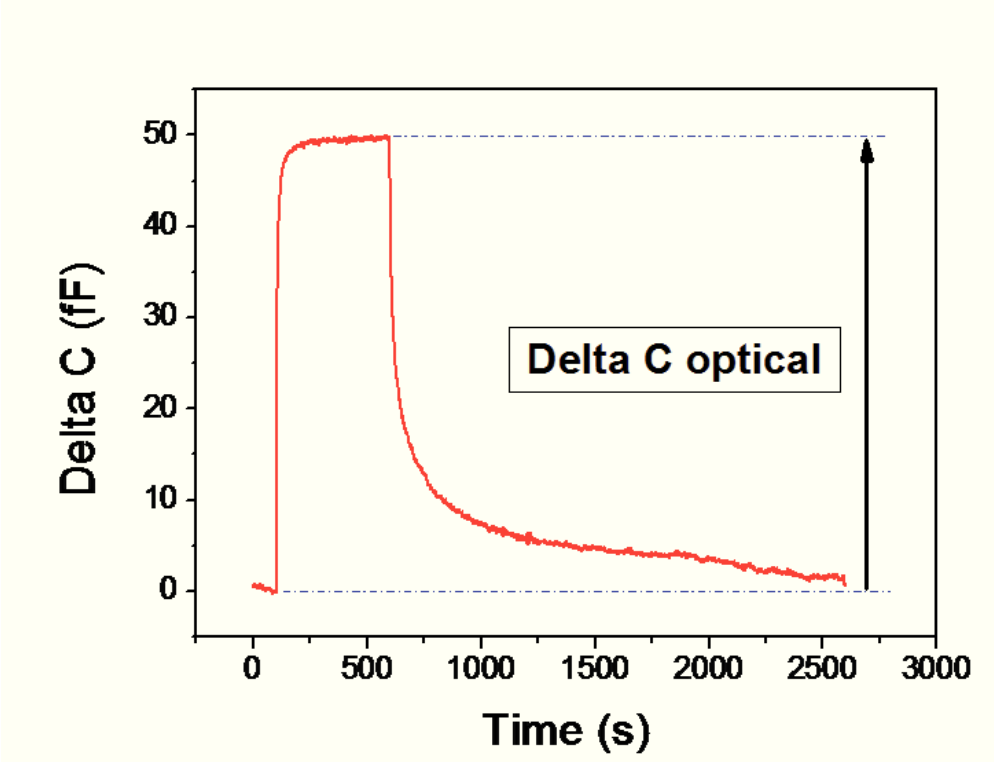


Figure 6.27: Typical DLOS transient obtained from a representative sample, at a specific wavelength of incident monochromatic light.

Deep level optical spectroscopy permits to extract the optical characteristics of a deep level. In particular two different types of analysis can be carried out on the optical transients, as that represented in Figure 6.27, obtained at different wavelengths, and thus at different energies of incident photons on LED surface: the first is the spectral dependence of Steady-State Photocapacitance (SSPC), which permits to identify the trap density N_t, while the second is the spectral dependence of optical cross-section (PCS), which provides information on the optical ionization energy E_o and the Franck-Condon energy d_{FC}. Note that the energy E_o is the minimum energy required for a photon to promote an electron or hole from a localized bandgap state to a delocalized state or a free carrier state upon absorption. On the other hand, the energy released in the form of multi-phonon excitation, as the local bonding configuration relaxes around a defect center immediately after a photoabsorption or photoemission event, is given by the Franck-Condon energy d_{FC}, which, to first order, is half of the Stokes shift[119].

The spectral dependence of *Steady-State Photocapacitance* provides an approximate overview of the deep level spectrum and enables us to determine the trap density N_t. In order to obtain the SSPC spectrum, the amplitude ΔC of optical transient under illumination of Figure 6.27 have to be measured for each wavelength. Thus the spectrum reports the amplitude ΔC, or alternatively $\Delta C/C$, as a function of photon energy $h\nu$. An example of SSPC spectrum for a representative sample is reported in Figure 6.28: with the increasing of energy, different changes in the slope of characteristic can be observed. Every change in the slope demarcates individual deep levels, because it corresponds to the onset of emission of carriers from the deep level. Note that these changes in the slope are not located in proximity of the optical ionization energy E_o, but rather they are located in proximity of the energy $h\nu = E_o - d_{FC}$: this is due to the phonon-assisted photoionization. Thus, from the SSPC spectrum it is not possible to determine the position of a deep level, given by the energy E_o, without the knowledge of the Franck-Condon energy d_{FC}. Moreover, the decrease in the amplitude of SSPC spectrum observable in Figure 6.28 for high photon energies is due to the absorption from the material of high energetic incident photons, before they can reach the active region of LED. The concentration of trap states N_t for a n-type semiconductor can be determined from the following relation:

$$\frac{\Delta C}{C} \cong \frac{N_t}{2N_d}\frac{\sigma_n}{\sigma_n + \sigma_p} \tag{6.1}$$

where $\Delta C/C$ can be obtained from the SSPC spectrum, N_d is the donor concentration, and σ_n and σ_p are the capture cross-sections for electrons and holes, respectively. This expression is evaluated for the value of $h\nu$ that yields the largest photocapacitance response. Furthermore, the application of this equation is limited to the case of $\Delta C \ll C$.

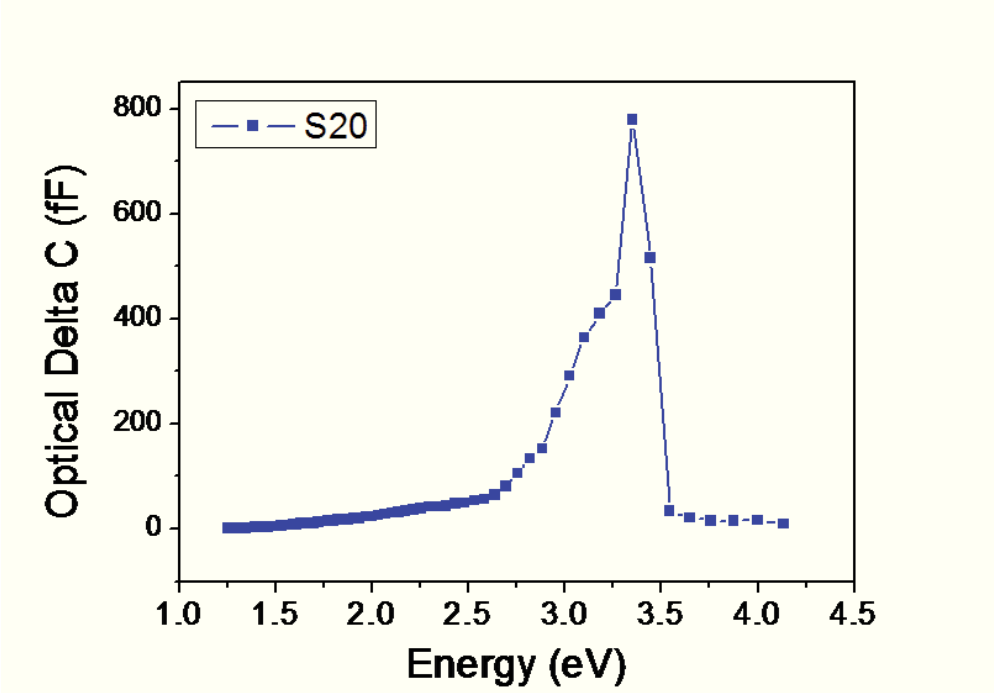


Figure 6.28: Steady-State Photocapacitance (SSPC) spectrum for a representative sample of family S20.

On the other hand, the parameters E_o and d_{FC} can be obtained by fitting the optical cross-section curve $\sigma_o(h\nu)$ to a theoretical expression. Thus, the analysis of spectral dependence of optical cross-section is necessary to extract the optical characteristics of deep levels. The photoionization (optical) cross-section (PCS), expressed in unit of cm^2, can be calculated by means of the following expression:

$$PCS(h\nu) = \frac{1}{\Phi(h\nu)\tau(h\nu)} \tag{6.2}$$

where $\Phi(h\nu)$ is the photon flux emitted by the quartz-halogen lamp, expressed as $number\ of\ photons/cm^2 \cdot sec$, and $\tau(h\nu)$ is the carrier lifetime of deep level. The photon flux can be easily measured by placing a calibrated photodetector at the output of monochromator, while in order to determine the value of $\tau(h\nu)$, the optical transients, such that of Figure 6.27, obtained at each wavelength have to be fitted at the beginning of illumination with the following first order exponential function [120]:

$$\Delta C(t) = \Delta C_0 \left(1 - e^{-t/\tau}\right) \tag{6.3}$$

Thus, the value of $\tau(h\nu)$ at each wavelength can be obtained as fitting parameter from the equation above. Note that this equation describes the photocapacitance change induced by a single deep level under optical excitation: for this reason only the first part of optical transient can be well fitted with this function. In fact, more than one deep level can contribute simultaneously to the capacitance variation

under illumination. Furthermore, several other factors can induce a deviation of the transient from the ideal shape.

A typical PCS characteristic for a representative sample of family S20, obtained from a DLOS measurement performed with a bias level of -10 V and light wavelengths comprised between 1000 nm and 300 nm, is shown in Figure 6.29. In particular, each transition in the PCS curve corresponds to the presence of a deep level, in this case to the emission of electrons from a donor level: the optical characteristics of deep level can be obtained by fitting the different regions of PCS curve with the *Passler* model proposed in [121], using E_o and d_{FC} as fitting parameters. The results of fitting carried out on this sample are reported in the same Figure 6.29: as it can be observed, two different trap levels have been identified, one with an optical ionization energy E_o of 2.191 eV, and a Franck-Condon factor d_{FC} of about 0.4 eV, and the other with an E_o of 3.35 eV and a d_{FC} of approximately 0.16 eV. Since the bandgap of wurtzite GaN is approximately equal to 3.44 eV, the level with an E_o of 3.35 eV probably corresponds to band-to-band transitions occurring in the bulk material with high energetic incident photons or to a shallow level localized near the valence band edge. Note also that very deep levels may strongly couple to the lattice and relax to a new atomic configuration upon carrier capture or emission. In this case, phonon-assisted photoionization from lattice-coupled deep levels results in a temperature dependent broadening of PCS characteristic, that manifests as absorption thresholds for $h\nu < E_o$. In such cases, the thresholds in the PCS and SSPC spectra are not necessarily equal to each other (even though they typically exhibit close agreement), and are less than E_o. In general, a larger d_{FC} will result in a broader PCS with a threshold at an energy less than E_o. [119]. Note that this is the case, for example, of trap with an E_o of 2.191 eV shown in Figure 6.29: as it can be observed, the threshold of this deep level is localized at about 2 eV.

In the following of this section the comparison of DLOS characterization, based on the analysis of both SSPC and PCS curves, carried out on LED families with different ESD robustness, will be presented. On the other hand, for more details on DLOS measurement and on analysis of deep levels carried out by means of this experimental setup, the reader can also refers to [122] and [123].

6.4.2 Results and discussion

Based on the results obtained in the previous section relatively to the slow capacitance transient measurements, we have analyzed the correlation between the DLOS signal of analyzed LEDs and their Relative failure. In particular, our analysis was initially focused on the comparison between a LED of family S20, which is characterized by a high Relative failure, and a sample of family S21, which is

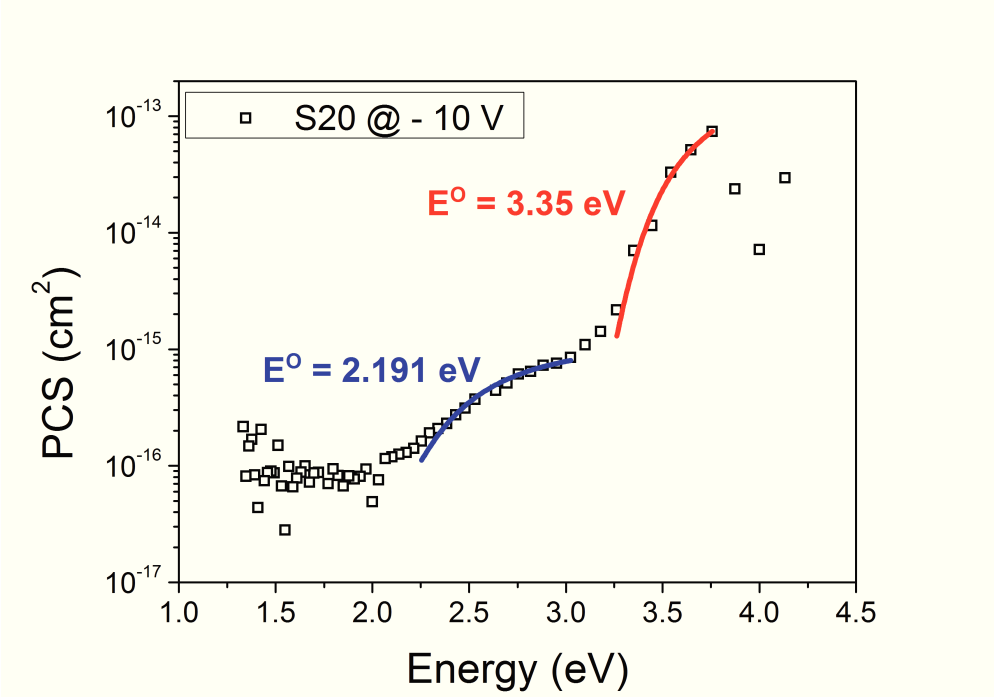
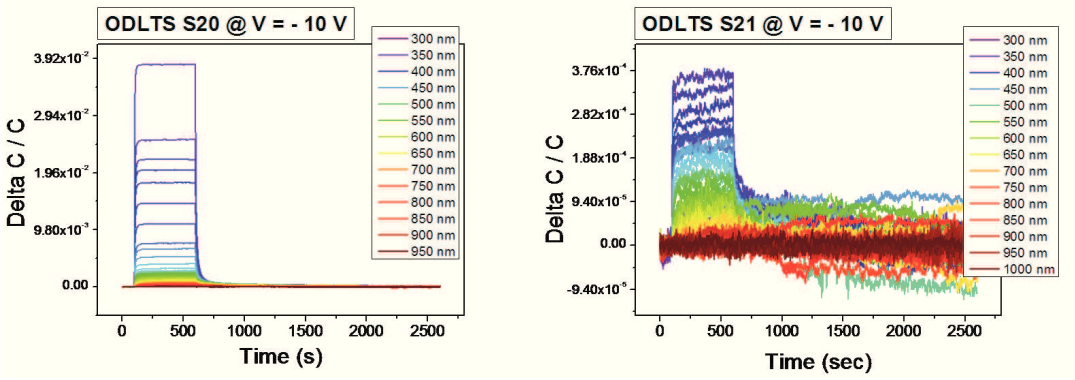


Figure 6.29: Spectral dependence of photoionization cross-section (PCS) of a representative sample of family S20 obtained from a DLOS measurement carried out at -10 V. Also the fitting curves, with corresponding optical ionization energy E_o of deep levels, are reported in this graph.

instead characterized by a low Relative failure. The optical transients obtained at -10 V and different illumination wavelengths for samples of families S20 and S21 are reported in Figure 6.30(a) and (b), respectively: note the huge difference between the amplitude of transients under illumination between the two devices. In particular, family S20, characterized by a higher Relative failure, shows a higher Delta C/C with respect to the family S21. Note also the different vertical scales used in Figure 6.30 and for this reason the transients of family S21 seem "noiser" with respect to those of family S20.

The comparison of PCS characteristics of two families, obtained from the analysis carried out on DLOS transients, is shown in Figure 6.31: as it can be observed, similar PCS curves, and also similar optical parameters for deep levels, have been obtained from this analysis. In particular, two deep levels have been identified in both samples: a deep level with E_o of about 2.2 eV and 2.4 eV for S20 and S21 family respectively, and same d_{FC} of about 0.4 eV; the second level has an E_o of about 3.35 eV and 3.24 eV for S20 and S21, respectively, with a d_{FC} equal to 0.16 eV for both samples. Note that the slight difference of E_o between the two devices is probably due to the limit of precision in determining this parameter from curve fitting. Furthermore, since the optical transients of Figure 6.30 show a positive capacitance variation with respect to the equilibrium value, these processes



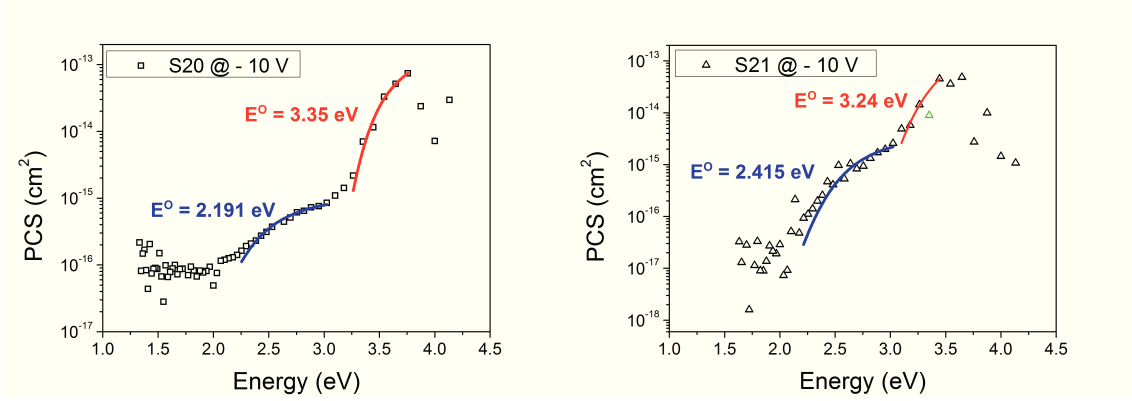
(a) High Relative failure. **(b)** Low Relative failure.

Figure 6.30: Comparison between optical transients obtained from DLOS measurements of a representative sample (a) from family S20, which is characterized by a high Relative failure, and (b) from family S21, which is characterized by a low Relative failure. Note the different vertical scale used in the two graphs, in order to permit an optimal observation of curves.

correspond to photoexcitation of electrons from the trap levels to the conduction band: as a consequence, the trap levels are localized at an energy $E_c - E_o$ within the bandgap of semiconductor. Deep levels localized at $E_c - 2.2\,eV$ $(E_c - 2.4\,eV)$ can be attributed to the presence of defects in this region of semiconductor. On the other hand, states localized at $E_c - 3.35\,eV$ $(E_c - 3.24\,eV)$ are probably due to band-to-band transitions or to a shallow donor level localized near the valence band edge. Thus, from the PCS analysis it is clear that analyzed LED families with different ESD robustness are characterized by similar energetic levels, even if the layered structure is quite different between LED families.

The SSPC analysis carried out on these two LED series have revealed quite similar characteristics, which are shown in Figure 6.32, thus confirming that similar energetic levels are involved in the trapping phenomena, as it has been seen from the PCS analysis. However, the amplitude of SSPC characteristics are different between analyzed samples. In particular, it can be noticed that the SSPC curve of family S20 has a higher amplitude with respect to that of family S21: this means that LEDs with a higher Relative failure are characterized by a higher defect density. In fact, we have seen that the amplitude of SSPC characteristic is proportional to the concentration of defects related to deep levels identified by means of PCS analysis. Thus, also in this case, a strong correlation between trap density and Relative failure of analyzed devices has been identified.

This hypothesis is further supported by histogram of Figure 6.33, which reports Delta C/C values obtained from DLOS measurements carried out at different energies of incident photons on some LED families with different Relative failure: as it



(a) High Relative failure. **(b)** Low Relative failure.

Figure 6.31: Comparison between PCS characteristics obtained from DLOS analysis of a representative sample (a) from family S20, which is characterized by a high Relative failure, and (b) from family S21, which is characterized by a low Relative failure. Also the values of optical ionization energy E_o of different deep levels are reported in the graphs.

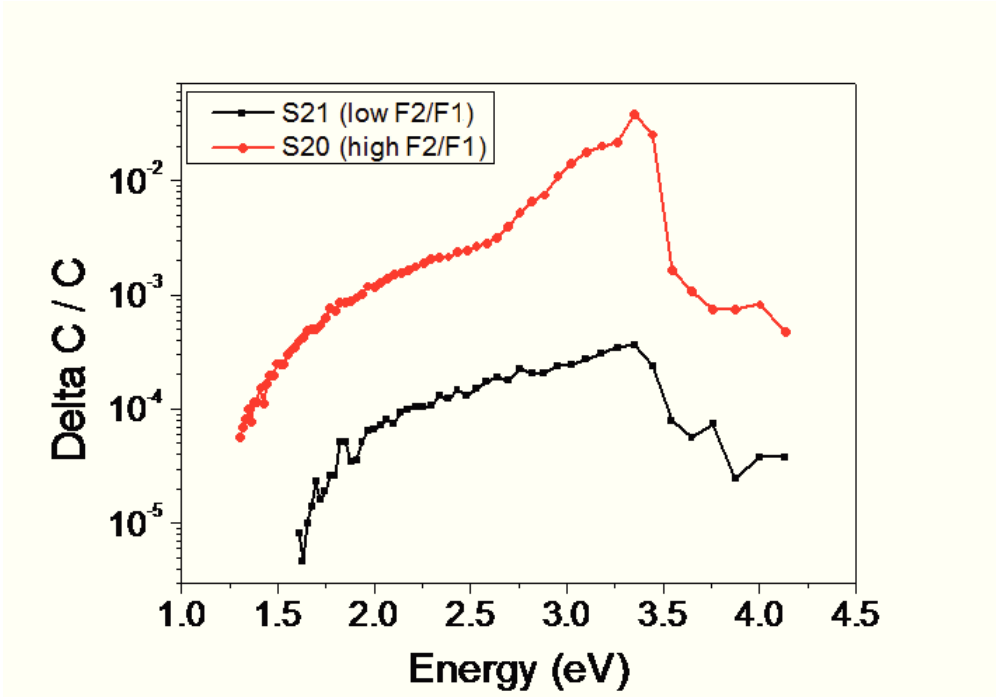


Figure 6.32: Comparison between SSPC characteristics of a representative LED of family S20, which has a high Relative failure, and one of family S21, which has a low Relative failure.

can be noticed, the amplitude of capacitance transients, and thus the concentration of defects related to deep levels, increases with increasing of the Relative failure.

To conclude this analysis, it is necessary to identify a correlation between the results obtained from DLOS measurements and slow capacitance transients pre-

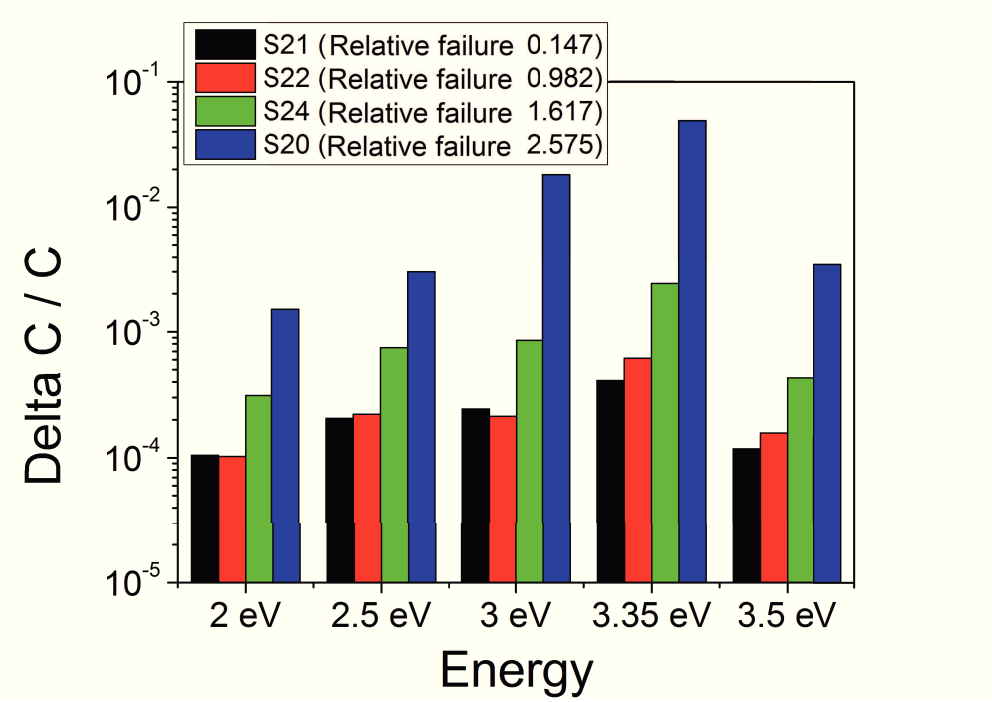


Figure 6.33: Histogram showing the amplitude of capacitance transients Delta C/C measured at different wavelengths on different LED families with increasing value of Relative failure.

sented in the previous section. In particular, the aim of this analysis is to identify the deep levels responsible for the capacitance transients when a reverse quasi-ESD pulse is applied to the LED. To obtain this, a new measurement was carried out, based on the combination of DLOS characterization with a slow capacitance transient measurement. A schematic of the evolution over the time of this measurement is reported in Figure 6.34: as it can be noticed, substantially it consists on the application of a reverse quasi-ESD pulse, superimposed to the bias level, while LED is under illumination. The capacitance variation is continuously acquired during the different phases of measurement. In order to correlate this procedure to the slow capacitance transient measurement, reverse quasi-ESD pulses with the same duration and amplitude as reported in Table 6.2 have been applied on different LED series.

The results of this analysis, obtained for a representative sample of family S20 at different wavelengths, are reported in Figure 6.35: as it can be observed, for incident light with a wavelength of 750 nm, the capacitance transient induced by reverse pulse is positive and its amplitude is only slightly reduced by the small optical transient. On the other hand, with an emitted light having 500 nm wavelength, the capacitance transient due to the reverse quasi-ESD pulse is completely suppressed: this means that the deep level responsible for slow capacitance transient analyzed in the previous section corresponds to an optical transition energy of

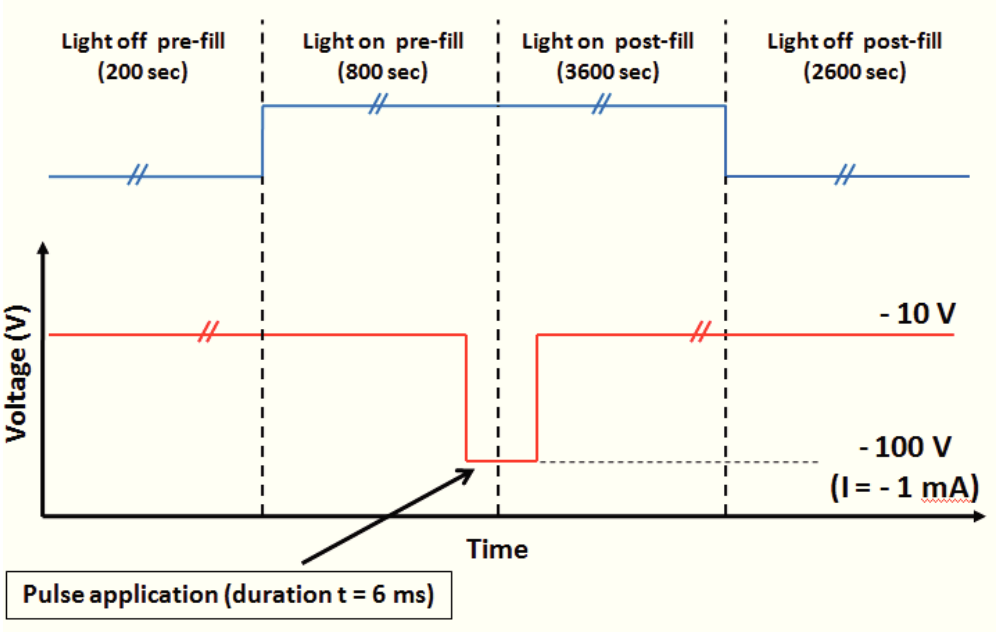


Figure 6.34: Schematic of temporal evolution of DLOS measurement with application of a reverse quasi-ESD pulse while the LED, in this case a representative sample of family S20, is under illumination.

about 2.48 eV. Based on the results obtained above from DLOS measurements, this energetic level can be identified with the deep level localized at about $E_c - 2.2\,eV$ for family S20. Moreover, from Figure 6.35 it can be also observed that for more energetic incident light, with a wavelength of 450 nm for example, the capacitance transient due to reverse pulse becomes negative: this fact also suggests that the shallow energy level localized at $E_c - 3.35\,eV$ cannot be responsible for the capacitance variation induced by an ESD pulse applied under reverse bias.

Thus, from DLOS analysis different deep levels have been identified: the positions of these trap states within the bandgap are very similar in all analyzed LED families. However, the concentration of defects related to these deep levels is quite different between LED series: in particular, it has been found that this concentration is strongly correlated to the Relative failure of LEDs. Furthermore, from the analysis of DLOS measurements carried out with the application of a reverse quasi-ESD pulse under illumination, it has been identified the deep level localized at about $E_c - 2.2\,eV$ as responsible for the trapping phenomena occurring during slow capacitance transient measurements and thus influencing the Relative failure, i.e. the ESD robustness of devices when two consecutive ESD pulses are applied on LEDs in a short time, under reverse bias. In the next section also deep levels detectable with the classical DLTS technique and their correlation with ESD robustness of LED series will be analyzed.

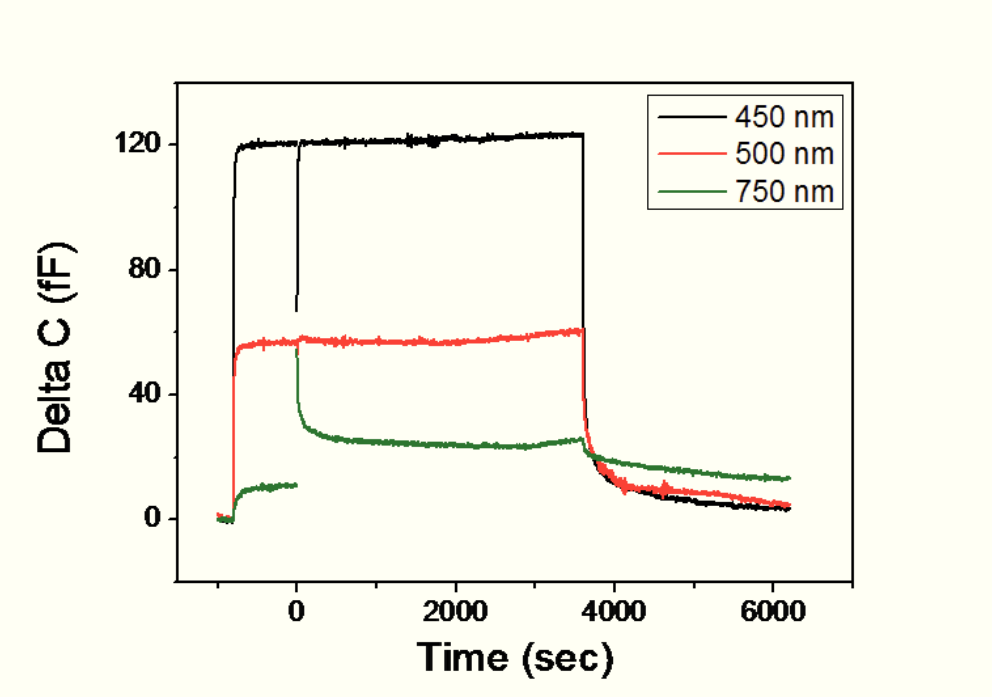


Figure 6.35: Capacitance transients obtained at different wavelengths from DLOS measurements with application of a reverse quasi-ESD pulse during the illumination phase, on a representative sample of family S20.

6.5 *DLTS* measurements

To conclude the analysis of deep levels present on LEDs with different ESD robustness, we have submitted the devices also to ***Deep Level Transient Spectroscopy (DLTS)*** characterization. As it has also been mentioned in the previous section, differently from the DLOS technique, DLTS analysis permits to identify deep levels with maximum thermal ionization energy E_{th} of about 1 eV, i.e. trap levels localized at maximum 1 eV below the conduction band edge or above the valence band edge. Note that in principle, deep levels detectable by DLTS setup can be also identified by means of DLOS technique. However, as we will see in the following of this section, other deep levels than those identified with DLOS analysis have been found for LED families with different ESD robustness. This is probably due to the low sensitivity of our DLOS system for incident photons with low energies, thus making it difficult to identify shallow levels. In fact, observing figure 6.29, it can be noticed that there is a quite high noise superimposed to the PCS characteristics for energies lower than 2 eV: this noise thus prevents from the determination of any deep level with optical ionization energy E_o lower than about 2 eV. In this section, first the DLTS theory and the experimental setup will be briefly explained. Afterwards, the experimental results obtained from analyzed LED families will be presented.

6.5.1 DLTS theory and experimental setup

The DLTS operation is very similar to that of slow capacitance transient measurement: in fact, also in this case the variation in junction capacitance induced by a temporary change in the polarization in measured. However, the following important differences exist between DLTS and DLOS or slow capacitance transient measurements:

- In DLTS measurements the voltage level V_{fill} of applied pulse is higher than the bias level V_{rev}. However, note that V_{fill} is not necessarily positive.
- The capacitance transients have typically a shorter duration, from some milliseconds to some seconds: this is due to the fact that trapping phenomena are faster for deep levels localized more close to the band edges, as those detectable by DLTS technique.
- In a DLTS measurement the capacitance transients are recorded at different temperatures of LED, than rather at different wavelengths on incident light, as in the case of DLOS technique.
- Differently from the techniques analyzed in previous sections, in DLTS measurement a negative capacitance transient corresponds to a majority carrier trap, while a positive capacitance transient corresponds to a minority carrier trap. Note that this result is valid both for n-type and for p-type semiconductors.

DLTS measurements were carried out by means of a *commercially available DLTS system SulaTech*, that comprises a high sensitive capacitance meter, a pulser and a cryostat. The LED was placed in a temperature-controlled stage in the dark, inside the cryostat, and thus it was connected to the DLTS system by means of a 2-wire connection. The capacitance is continuously measured over the time with the capacitance meter: this instrument, to measure the capacitance, applies a small signal with a frequency of 1 MHz. For our analysis we have applied to LED a bias level V_{rev} of -10 V, in order to obtain a consistent comparison with slow capacitance transient and DLOS characterization. At a certain instant t, a voltage pulse with a duration of 100 ms and amplitude V_{fill} of 0 V was applied. In particular, this value of V_{fill} has been chosen after some preliminary measurements carried out varying the pulse amplitude, in order to maximize the DLTS signal, thus suggesting that trap states are present also in the multi-quantum well region of analyzed LEDs. After the pulse application, the corresponding capacitance transient induced by trapping phenomena was recorded and analyzed by DLTS system. This process has been repeated at different temperature levels, in a wide range comprised between

83 K and 530 K, with a step of 1 K, in order to identify different thermally activated trap levels.

A possible interpretation of the trapping phenomena occurring during DLTS characterization is provided by the band diagrams of a p^+n junction shown in Figure 6.36, which are referred to different instants of DLTS measurement. With reference to the figure, that shows the n-side of the junction, E_D represents the energy of a donor level, E_T is the energy of a deep level localized within the bandgap and E_{Fn} is the quasi-Fermi level on the n-side. In particular, we suppose that far from the junction the trap level E_T is below the Fermi level. Moreover, we suppose that this trap is neutral when is occupied by electrons and positively charged when is empty. The evolution of band diagram can be explained as follow, referring to the same figure:

- Figure 6.36(a) represents the initial equilibrium condition: it can be observed that the donor and trap states localized above the Fermi level are empty (indicated as "+" in figure). The limit of depletion layer is localized at the edge of empty donors.

- Figure 6.36(b) shows the band diagram during the pulse application. As a consequence of applied bias, the band bending decreases, with the result that more donors and trap states are filled with electrons.

- Figure 6.36(c) represents the condition after a short time from the pulse application, when the junction is recovering the initial condition. However, trap states occupied by carriers are not able to instantly emit an electron, due to their deep position within the bandgap. As a consequence, in order to verify the charge neutrality principle, more donors are ionized (the charge on the p-side is equal to the initial value, because we suppose that the deep level is localized only in the n-side): this results in a broadening of the space charge region and thus in a decrease of the junction capacitance with respect to the initial value.

- Figure 6.36(d) shows the band diagram after a certain time from the pulse application. Because this is not the equilibrium condition, with the increasing of time the trap states will be able to emit electrons and correspondingly fewer donors will be ionized, in order to maintain the charge neutrality. As a consequence the depletion width will decrease and the capacitance will increase towards the equilibrium value.

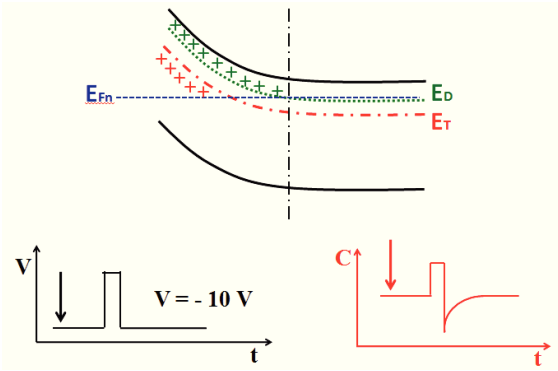
- Finally, after an enough long time, the initial condition will be completely recovered, as shown in Figure 6.36(e).

Note that in the previous considerations it has been assumed that the capture rate of electrons from trap states is much higher than the emission rate of electrons. Furthermore, this analysis can be easily extended to the case of a p-type semiconductor, or to a minority carrier trap.

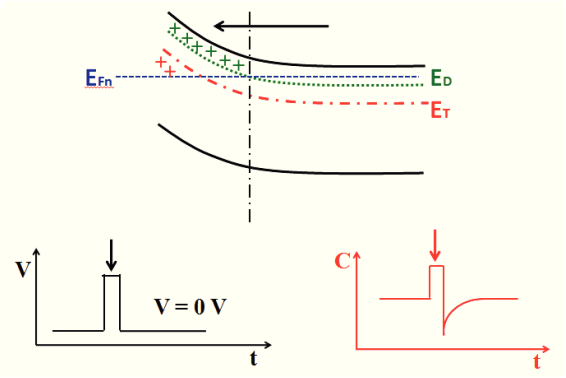
The capacitance transients obtained from a DLTS procedure are strongly dependent from the junction temperature: this means that each transient has a different time constant τ, in the hypothesis that the capacitance transients have an exponential trend. Thus, calculating this time constant at every temperature, a graph of time constant as a function of temperature can be obtained. Nowadays, the typically adopted DLTS analysis is that proposed by Lang in [124], which is based on the *rate window* concept, i.e. a system that is able to select capacitance transients with a specific time constant. In particular, this can be obtained by using a *dual-gated integrator (double boxcar)*: with this method, the amplitude of transients is measured in correspondence of two instants t_1 and t_2. The DLTS signal in given by the difference of these two values, i.e. $C(t_1) - C(t_2)$. As it can be observed from Figure 6.37, this difference is very small for high and low temperatures levels; on the other hand, when the time constant τ of capacitance transient is approximately equal to $t_2 - t_1$, the DLTS signal increases and reaches a maximum value in correspondence of a specific temperature. Thus, repeating this process at different temperature levels, we obtain a plot with the amplitude of DLTS signal as a function of temperature, which is usually called *DLTS spectrum*. In particular, the DLTS spectrum will be characterized by the presence of one o more peaks: each peak corresponds to the presence of a deep level inside the bandgap. From considerations above, it is clear that a negative peak will correspond to a majority carrier trap, while a positive peak will correspond to a minority carrier trap.

A DLTS system usually provides as result directly the DLTS spectrum, than rather the capacitance transients waveforms. In particular, the properties of trap states can be obtained from the analysis of DLTS spectrum, including the thermal ionization energy E_{th}, the capture cross-section σ and the trap density N_t. From considerations above it is also clear that by changing the rate window, acting on t_1 and/or t_2, also the shape of DLTS spectrum changes, in particular the position of peaks, and as we will see in the following, this is at the basis for the construction of the Arrhenius plot necessary for the determination of E_{th} and σ. Three different criteria can be chosen to change the rate window: *(i)* changing t_1, with t_2 constant; *(ii)* changing t_2, with t_1 constant; and *(iii)* changing both t_1 and t_2, by maintaining t_1/t_2 constant. Note that this last criterion is that adopted from our DLTS system: in particular, by choosing the t_1 value, the rate window is set to the value of $4.3 \cdot t_1$.

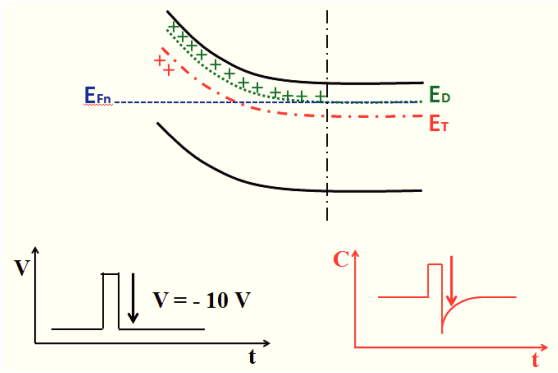
An example of DLTS spectrum obtained from one of analyzed LEDs of family S20 is shown in Figure 6.38: different curves are reported in this figure, each



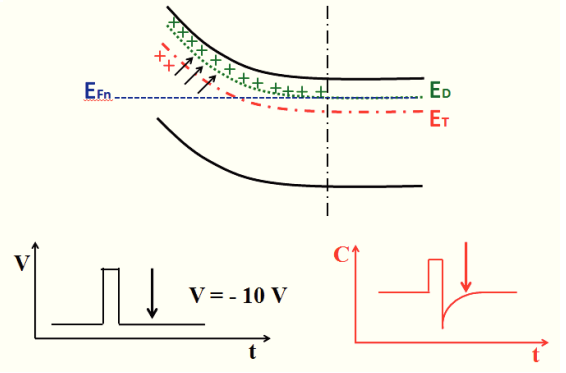
(a) Before pulse application.



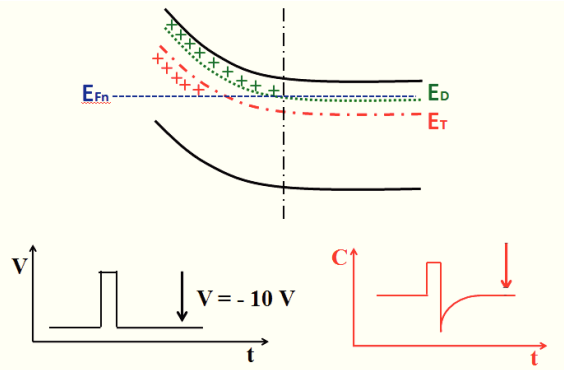
(b) During pulse application.



(c) At the end of pulse application.



(d) The junction is recovering the initial condition.



(e) The initial condition is completely recovered.

Figure 6.36: Evolution of band diagram during a DLTS measurement for a p^+n junction characterized by the presence of a majority carrier trap localized within the bandgap. The figure shows only the band diagram of n-side.

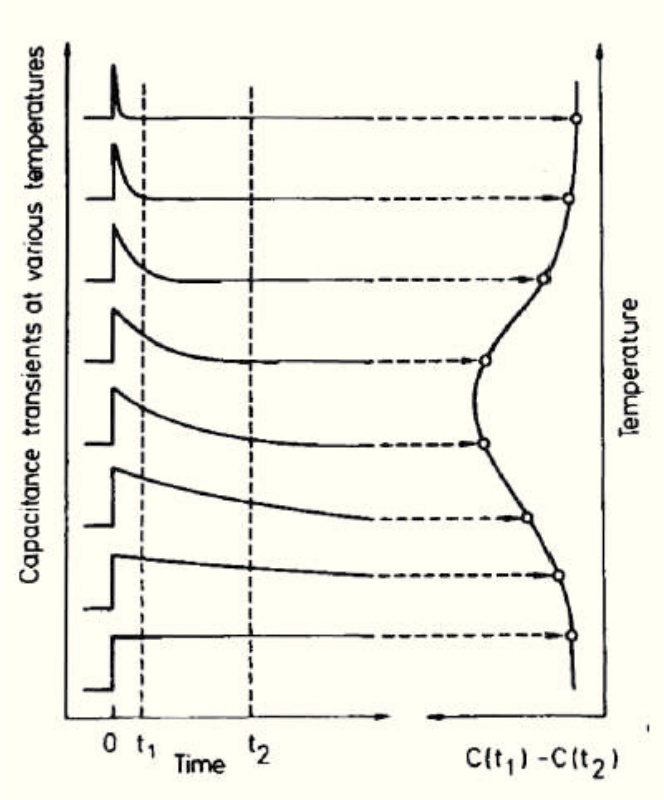


Figure 6.37: Implementation of *rate window* concept in the DLTS analysis, by means of a *double-boxcar integrator*.

corresponding to a different rate window, whose value of t_1 is reported in the legend. In particular, two negative peaks are clearly observable at about 300 K and 450 K: this peaks correspond to the presence of two majority carrier traps, that in the following we named e_1 and e_2. From the analysis of this DLTS spectrum, we can estimate the main parameters of traps.

The trap density is proportional to the peak amplitude in the DLTS spectrum. In particular, the trap concentration N_t is related to the peak amplitude of DLTS spectrum by the following relation:

$$N_t = 2\frac{\Delta C}{C}(N_D - N_A) \tag{6.4}$$

where ΔC is the amplitude of capacitance transient measured at the end of pulse application, C is the total capacitance of LED measured at V_{rev}, and $N_D - N_A$ is the net donor concentration on the n-side, referring to the example above of a p^+n junction, with a trap on the n-side. Thus, from the relation above it is clear that, in order to obtain the correct value of N_t, it is necessary to measure the amplitude of capacitance transients at $t_1 = 0$. However, in the following we will not calculate the exact values of N_t in the analyzed samples, because we do not know the real value of net donor concentration of LEDs. For this reason, we will focus only on the comparison of Delta C/C values.

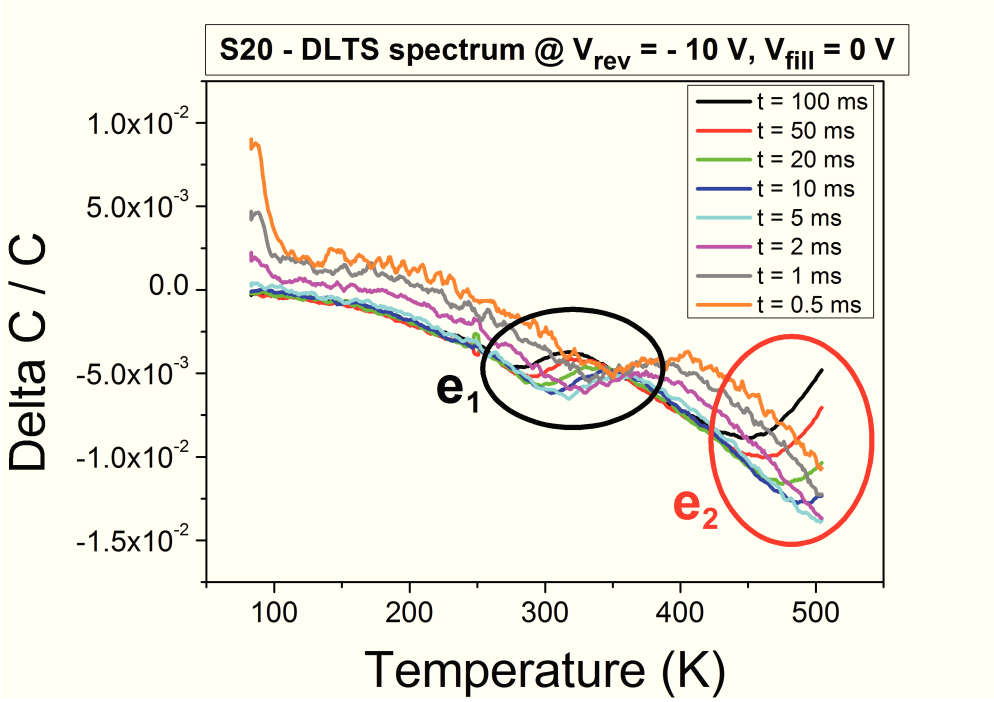


Figure 6.38: DLTS spectrum of a representative LED of family S20, obtained from a DLTS measurement carried out with $V_{rev} = -10\,V$, $V_{fill} = 0\,V$ and $t_{fill} = 100\,ms$.

On the other hand, in order to estimate the thermal ionization energy E_{th} and the capture cross-section σ, we need to extract the *Arrhenius plot* of the trap level. To obtain this, first the temperature T at which the peak of DLTS spectrum occurs for each rate window have to be determined. Afterwards, the emission rate corresponding to each curve of DLTS spectrum have to be calculated as $e_n = 1/4.3 \cdot t_1$ for our DLTS system. At this point the Arrhenius plot is simply obtained by plotting the relation $ln(T^2/e_n)$ vs q/kT, where k is the Boltzmann constant, with the different points previously determined by the analysis on DLTS spectrum. Finally, a linear fitting of Arrhenius plot provides the characteristics of trap level: in particular, the slope of straight line gives the E_{th} value, while the intercept is proportional to the capture cross-section σ. The corresponding Arrhenius plots with the linear fitting of trap levels identified in the DLTS spectrum of Figure 6.38 are reported in Figure 6.39: as it can be observed, trap levels e_1 and e_2 are localized at about $E_c - 0.6\,eV$ and $E_c - 1\,eV$, respectively. Note that these deep levels are localized closer to the conduction band with respect to impurity levels that have been idenfied by means of DLOS technique. The capture cross-sections have not been calculated in this case.

In the following of this section we will analyze the correlation between deep levels identified by means of DLTS analysis described above and the ESD robustness of LEDs. For more details about the DLTS theory and the analysis based on the rate window method, the reader can refer to [124].

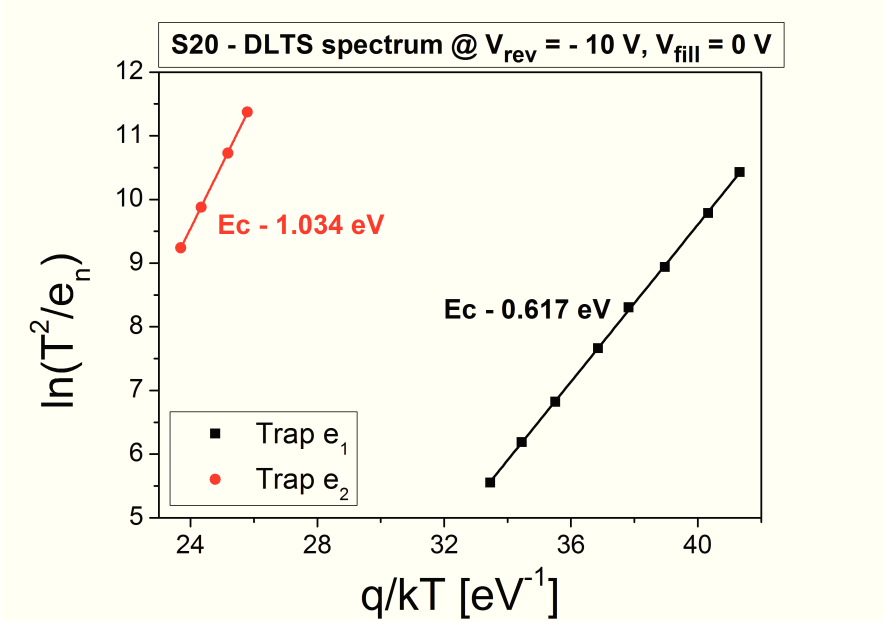


Figure 6.39: Arrhenius plots of traps e_1 and e_2 with relative linear fittings, obtained from the analysis of DLTS spectrum of Figure 6.38 for a representative LED of family S20.

6.5.2 Results and discussion

Each LED series with different ESD robustness has been submitted to DLTS characterization, following the experimental details provided above. A DLTS spectrum and the corresponding Arrhenius plots of identified traps have been obtained for each sample. In particular, all analyzed LEDs have shown similar DLTS spectra, characterized by the presence of two or three negative peaks, related to the presence of majority carrier traps, i.e. traps for electrons in our case. A comparison between DLTS spectra of different LED families, obtained with the same rate window, is reported in Figure 6.40: as it can be noticed, the main difference between DLTS spectra of different LED series is represented by the amplitude of DLTS peaks, than rather the position, which is similar in all analyzed devices. Note that the three deep levels have been named for simplicity e_1, e_2 and e_3 in the following, respectively. In particular, trap e_3 is detectable only in S21 and S29 families.

The comparison between Arrhenius plots of traps of each LED series is reported in Figure 6.41: as it can be observed, very similar activation energies have been obtained for traps e_1, e_2 and e_3 on different samples. The three traps are localized approximately at $E_c - 0.6eV$, $E_c - 1eV$ and $E_c - 0.2eV$ for e_1, e_2 and e_3, respectively. Also the positions of points in the Arrhenius plot of different devices are similar, thus suggesting that traps have also similar capture cross-section σ, even if it has not been directly calculated.

Based on these results, also in this case the correlation between the amplitude

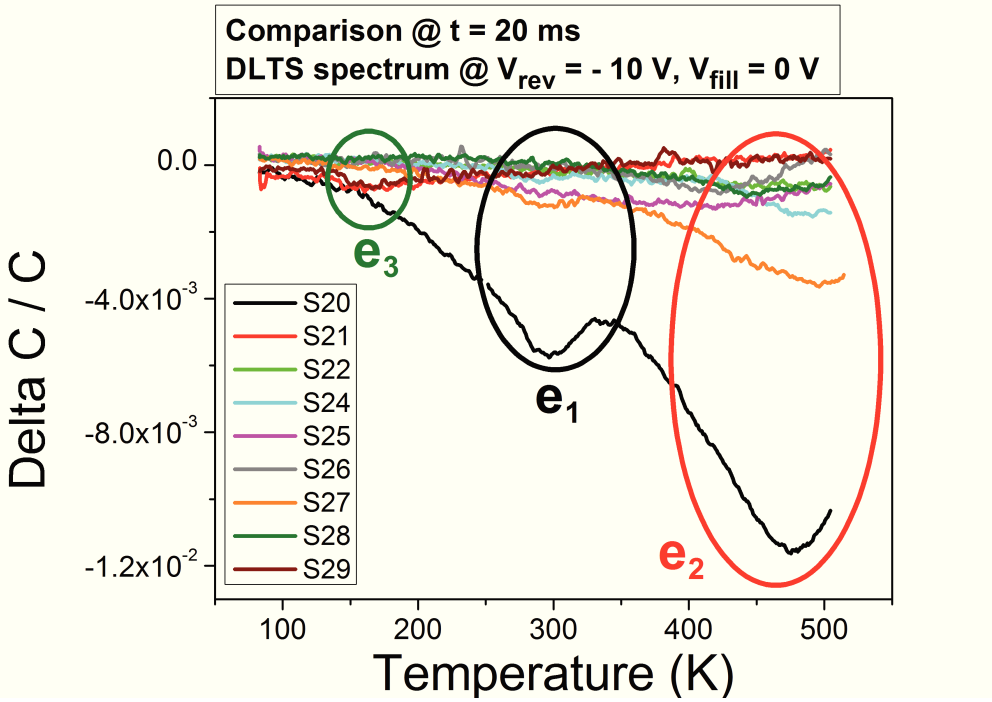


Figure 6.40: Comparison between DLTS spectra of a representative LED for each family. The DLTS curves are referred to a rate window with $t_1 = 20\,ms$.

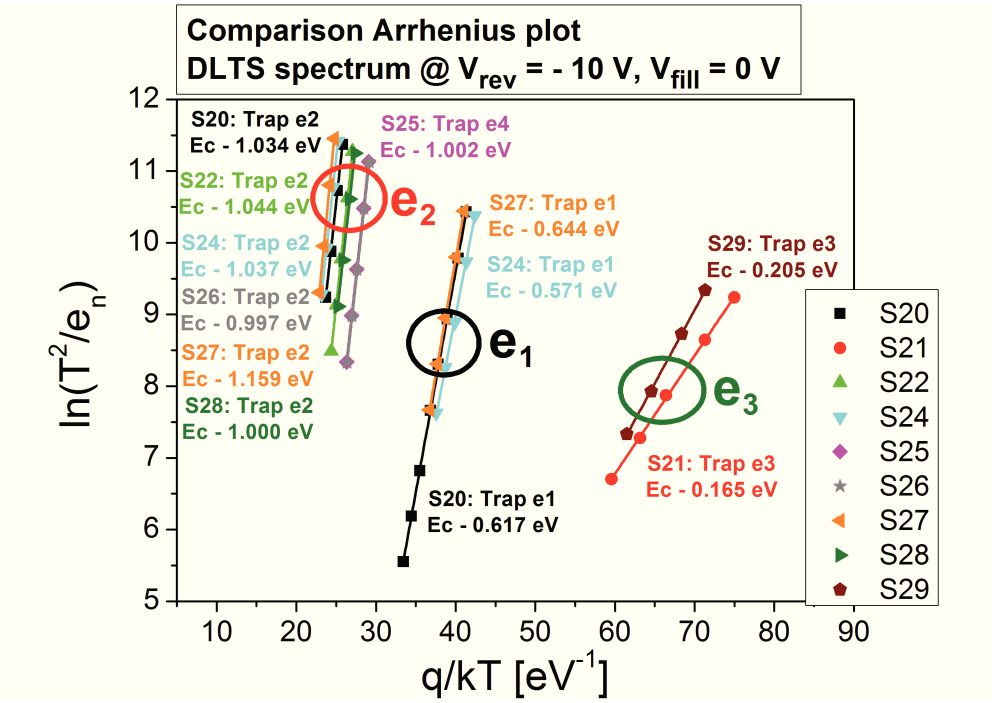


Figure 6.41: Comparison between Arrhenius plots of traps e_1, e_2 and e_3 for a representative LED from each family.

of DLTS signal in correspondence of peaks and the ESD robustness of devices, have been analyzed. In particular, this analysis has been focused only on traps $e1$ and e_2, because they are common to all LED families, and thus they are eventually

responsible for the First level failure, Second level failure or Relative failure. On the other hand, trap e_3 has been identified only in S21 and S29 families and for this reason it has been neglected for the study of correlation with ESD robustness.

The results of analysis of correlation between ESD robustness and DLTS peak amplitude are reported in Figures 6.42 and 6.43 for trap e_1 and e_2, respectively. From these figures, no correlation can be observed between the DLTS signal and

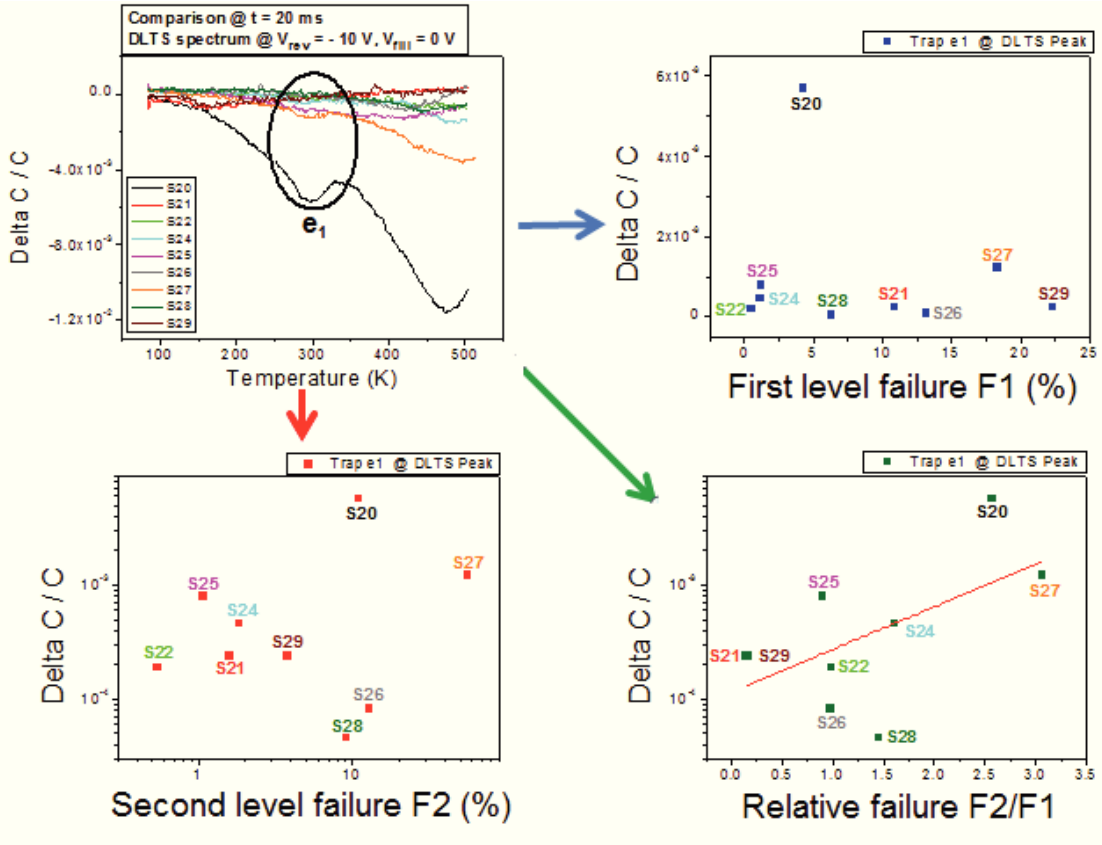


Figure 6.42: Correlation between DLTS peak amplitude, expressed as Delta C/C, of trap e_1 and First level failure, Second level failure and Relative failure. A correlation between peak amplitude and Relative failure (i.e. Second level failure/First level failure) can be observed.

First level failure and Second level failure, for both analyzed traps. On the other hand a strong correlation can be noticed between the DLTS signal and Relative failure (i.e. Second level failure/First level failure) in both traps. This correlation is suggested by also the red lines in the figures, obtained as linear fitting of points. In reality, Figure 6.42 shows that this correlation is quite weak in trap e_1: this fact can be attributed to the difficulty in measuring the DLTS peak amplitude of trap e_1 in some LED families, due to the limit of sensitivity of our DLTS system. In fact, in Figure 6.40 we can observe a rather high noise superimposed to the DLTS signal in most of curves.

As explained above, the amplitude of DLTS signal is proportional to the trap

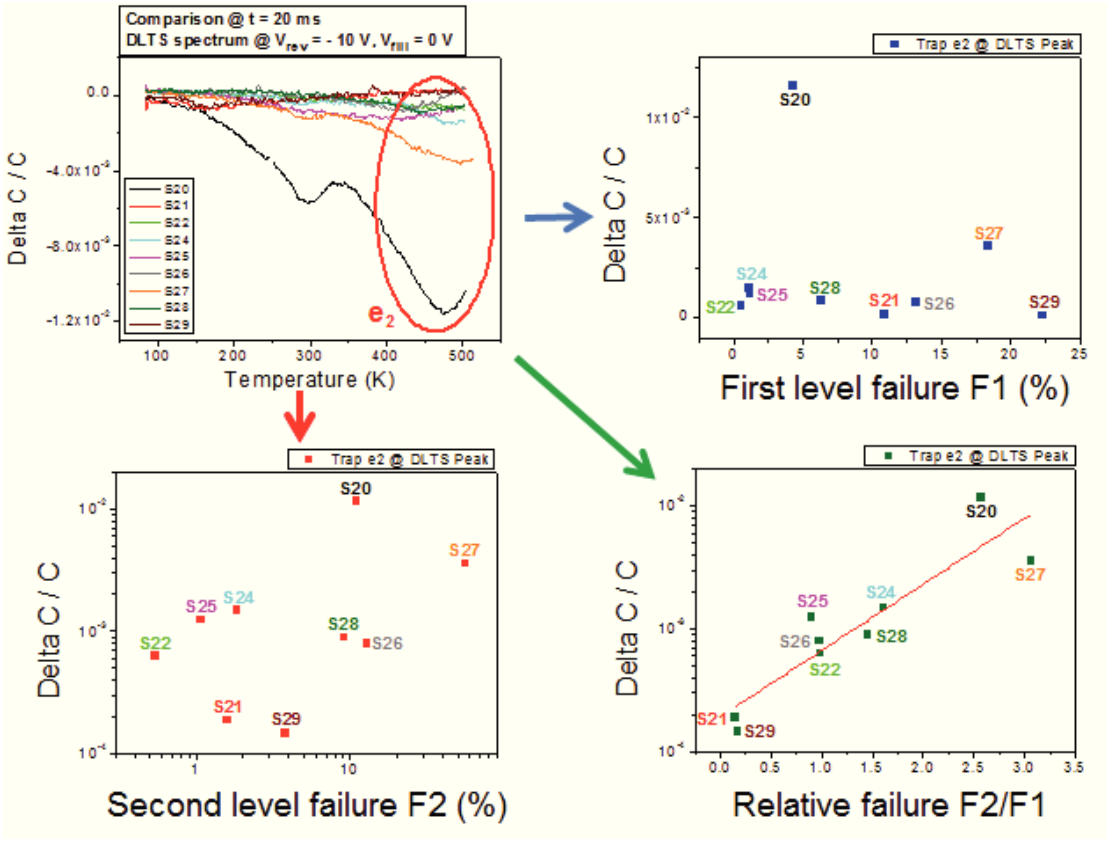


Figure 6.43: Correlation between DLTS peak amplitude, expressed as Delta C/C, of trap e_2 and First level failure, Second level failure and Relative failure. A correlation between peak amplitude and Relative failure (i.e. Second level failure/First level failure) can be observed.

concentration in the semiconductor. Thus, from these results it can be easily understood that also deep levels identified by DLTS characterization are responsible for the Relative failure, i.e. for the ESD robustness of LEDs when submitted to a second ESD pulse. In particular, devices with a higher trap density seem to have a lower ESD robustness. Thus also in this case, as it has been seen from DLOS analysis, the main difference between LED families is the presence of a different density of defects, that can influence the Relative failure of devices. However, all analyzed LEDs contain similar types of defects, as confirmed by the very similar deep levels identified by DLTS analysis.

6.6 Summary

An extensive study of physical mechanisms that limit the ESD robustness, expressed in terms of three parameters, i.e. First level failure, Second level failure and Relative failure, of GaN-based LEDs have been carried out in this chapter. In particular, our analysis was based on a general electro-optical characterization and

an extensive study of deep levels present in the semiconductor material, by means of slow capacitance transient, DLOS and DLTS measurements. Very interesting results and correlations between electrical and optical properties of devices and ESD robustness have been found from this study. In particular, the most important results obtained from the analysis can be summarized as follow:

- No correlation has been found between the ESD robustness of devices and their reverse leakage current, reverse bias luminescence and optical power under forward bias, respectively.

- A strong correlation between First level failure, which represents the ESD robustness of LEDs when submitted to a first ESD event under reverse bias, and the overall junction capacitance have been identified. In particular, this phenomenon has been attributed to the fact that a higher overall capacitance, which corresponds to a higher total charge accumulated in the junction, and thus to a higher electric field in the depletion layer, can negatively influence the ESD characteristics of devices during the application of a high reverse pulse.

- Different deep levels have been identified in analyzed LED families by means of both DLOS and DLTS technique. In particular, all analyzed LEDs have trap states with similar activation energies, but different concentrations. A strong correlation has been identified between the trap density of different LEDs and their Relative failure. This phenomenon can be explained by the fact that trapping phenomena related to these deep levels can influence the ESD robustness when devices are submitted to a second ESD event after a short time from the application of first ESD pulse. In particular, it has been shown that a higher trap density reduces the ESD robustness in such a condition.

- Trapping phenomena occurring during an ESD event have been observed by means of slow capacitance transient measurements. In particular, by combining DLOS and slow capacitance transient characterization, the deep level localized at $E_c - 2.2\ eV$ has been identified as main responsible for trapping phenomena occurring during the application of a reverse quasi-ESD pulse. In fact, by illuminating the LED surface with light having this energy, the capacitance transient induced by reverse pulse is completely suppressed.

Thus, this investigation has provided very important information about the physical mechanisms that limit the ESD robustness of GaN-based LEDs. In particular, these results are very important for the future development of LEDs with high ESD robustness.

Chapter 7

ESD characterization of RGB LEDs

In the previous chapter, the physical mechanisms that limit the ESD robustness of GaN-based LEDs have been extensively analyzed. To conclude our investigation of ESD effects on LEDs, in this final chapter we propose an extensive study of failure mechanisms occurring on LEDs, when they are submitted to ESD events. To obtain this, state-of-the-art LEDs were submitted to ESD stress test combined with an electrical and optical characterization, in order to determine the damages induced by ESD events, and thus to estimate the ESD robustness of devices, whose value is calculated on the basis of specified failure criteria.

In chapter 3 we have seen that electrostatic discharge (ESD) events represent one of the most critical problem for the failure of electronic devices, including also light-emitting diodes: in particular, ESD events usually induce the catastrophic failure of devices, and in some cases also latent damages, where the device can still emit light after the ESD event, before giving unexpected and unexplained failures. Note that ESD are present in the whole life of a LED, starting from device manufacturing, to the assembling, and to the final operating conditions. Thus, it is clear that this topic is of fundamental importance for the study of reliability of LEDs, and thus to realize devices with high ESD robustness. In chapter 3 it has been also seen that in the recent years many solutions have been proposed, in order to increase the ESD robustness of LEDs. However, despite the importance of this topic, and the different protection strategies developed by several research groups and companies, we have seen that only few works can be found in literature concerning the investigation of physical mechanisms that limit the ESD robustness of devices.

The aim of this work is to contribute to the understanding of physical mechanisms responsible for the degradation and catastrophic failure of LEDs submitted to ESD stress, highlighting the dependencies on device material. To do this, an ESD characterization, based on ESD stress test, was carried out on RGB LEDs fabricated by four leading manufacturers, in order to have and effective compari-

son between different device technologies and to ensure that the results obtained within this thesis are of general interest. In particular, by analyzing RGB devices, it can be described the effects of ESD events on two different technologies: AlInGaP-based red LEDs and GaN-based green and blue devices. Thus, with such an analysis we can understand how red, green and blue LEDs behave when they are submitted to ESD events, and identify possible differences between the three kinds of devices. In this chapter, after an initial description of analyzed RGB LEDs and the experimental setup used for this investigation, the results of ESD stress tests will be presented and discussed. In particular, the results of ESD stresses carried out under forward and reverse bias will be presented separately. Finally, also the results of ESD testing stress performed on LEDs at different temperature levels will be reported and discussed.

7.1 Analyzed RGB LEDs and experimental details

The analysis was carried out on commercially available RGB multichip LEDs from four different suppliers, referred in the following as Family 'A', 'B', 'C' and 'D'. Each RGB device includes an AlInGaP-based red LED, with an emission wavelength of about 635 nm, a GaN-based green chip, with emission centered at about 525 nm, and a GaN-based blue LED with an emission wavelength of about 465 nm. Each LED is characterized by different dimensions and also by a different contact structure. Images of one of the analyzed RGB LEDs for each family are reported in Figure 7.1, 7.2 and 7.3, for families 'B', 'C' and 'D', respectively[1]: note that each LED has a different area. Furthermore, green and blue LEDs of families 'B' and 'D' are not characterized by a vertical structure, because both contacts are made in the front size of device. Thus, also the effects of a different LED contact structure on the ESD robustness of devices will be analyzed in the following.

After a initial electro-optical characterization, a set of devices from each family with uniform characteristics was submitted to ESD testing, according to the TLP model. ESD events were simulated by means of a Transmission Line Pulser based on Time Domain Reflectometer (TLP-TDR) technique, as that described in section 3.3.3, which generates 100 ns pulses with increasing voltage and current amplitude at each next pulse. The rise and fall time of generated rectangular pulses is about 10 ns. A schematic of TLP system used for this study is shown in Figure 7.4: it includes a *Standford Research Systems PS350* high-voltage generator, a *Tektronix TDS680B* digital oscilloscope and a transmission line 10 m long. The voltage and current levels during pulse application were measured by

[1]Note that the images of LEDs of family 'A' are not reported, since it was not possible to acquire photos of these devices, due to presence of an epoxy encapsulant

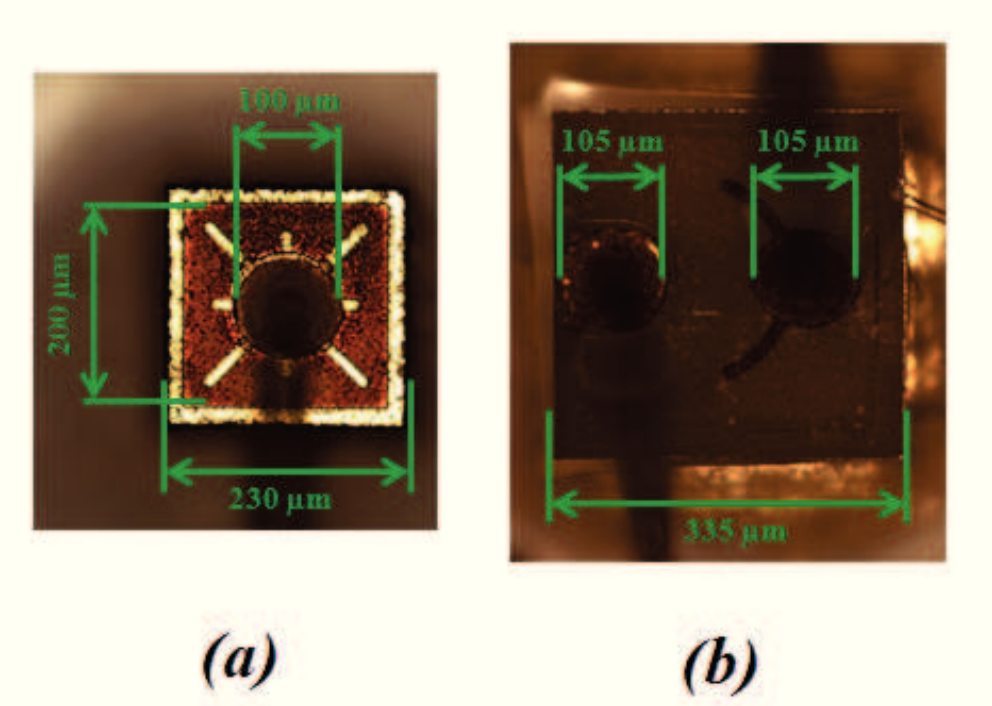


Figure 7.1: (a) Red and (b) green and blue LEDs of a representative RGB multi-chip sample of family 'B'. Also the dimensions of LED structures and contacts are indicated in figure.

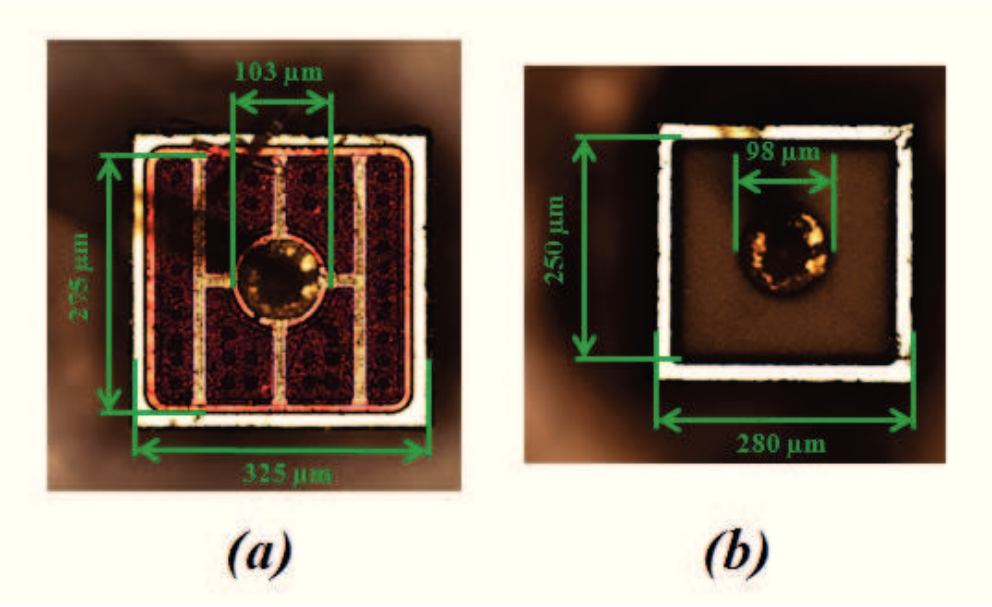


Figure 7.2: (a) Red and (b) green and blue LEDs of a representative RGB multi-chip sample of family 'C'. Also the dimensions of LED structures and contacts are indicated in figure.

means of a*Tektronix P6139A* voltage probe and a *Tektronix CT-2* current probe, respectively. Finally, a *HV H12-1A69 MEDER* switch was used to discharge the transmission line on the DUT (device under test). Also the series resistance of the

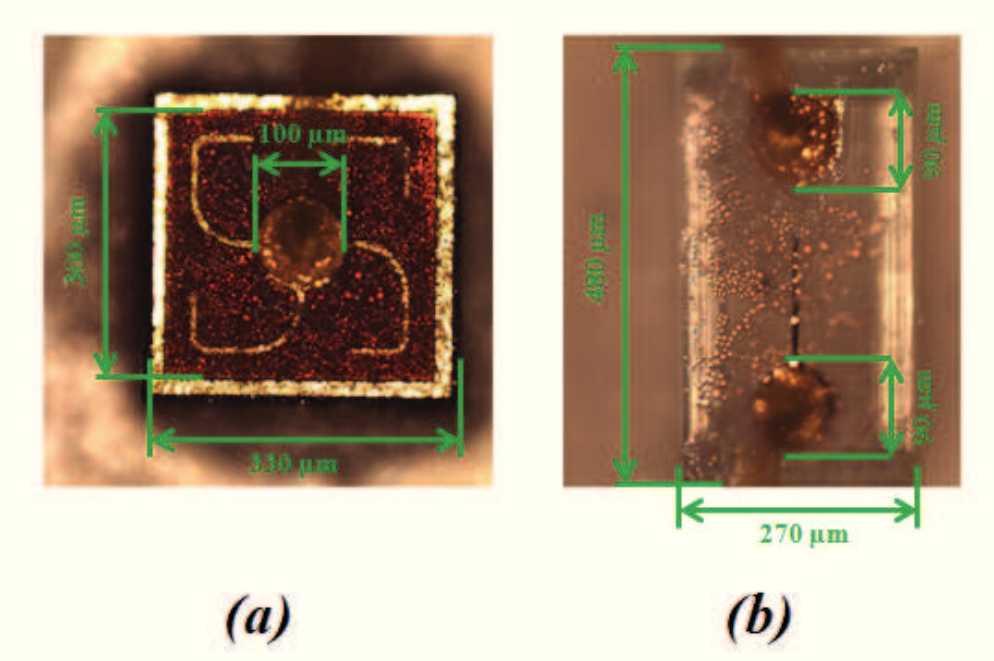


Figure 7.3: (a) Red and (b) green and blue LEDs of a representative RGB multi-chip sample of family 'D'. Also the dimensions of LED structures and contacts are indicated in figure.

setup, introduced by wires and connectors, was compensated by measuring a short circuit, in order to have quantitative results.

After each pulse the current-voltage (I-V) characteristic of the LEDs were measured by means of a *SourceMeter Keithley 2636A*, in order to evaluate the degradation induced by ESD events, such as possible modification of the leakage current and creation of shunt paths. Also the optical power-current (L-I) characteristic was measured after each pulse on some of the analyzed samples, by means of a *Optical Power Meter Newport 1830C* and an integrating sphere, in order to detect possible optical degradation even at stress levels below the failure one (note that the failure level has been defined as the ESD level that induces a total quenching of the EL signal or a catastrophic failure of the devices). For the tests, the devices were mounted on suitable printed circuit boards (PCBs), allowing for a reproducible positioning of the integrating sphere used for the measurement of the optical power.

In order to better understand the failure mechanisms, LEDs were submitted to ESD stress tests separately under reverse and forward bias conditions, i.e. a group of RGB devices were submitted to negative TLP pulses and another group to positive TLP pulses. The analysis was carried out on a statistically relevant number of samples ($>$ 20 RGB devices) for each family. The ESD stress tests consist on the application of TLP pulses with increasing voltage level, and the corresponding electrical, and eventually optical, characterization carried out after

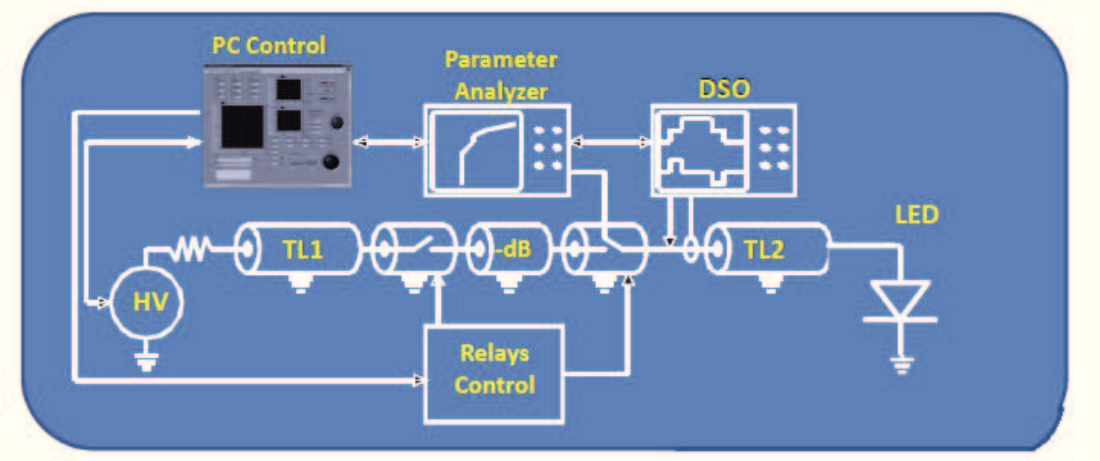


Figure 7.4: Schematic of TLP-TDR system used for the ESD characterization carried out on RGB multichip LEDs.

each pulse, until the failure level is reached (the failure criteria adopted for this analysis will be explained in the next section): a schematic of evolution of TLP test is shown in Figure 7.5. In the next section, the results of ESD tests carried out under reverse and forward bias separately, will be presented.

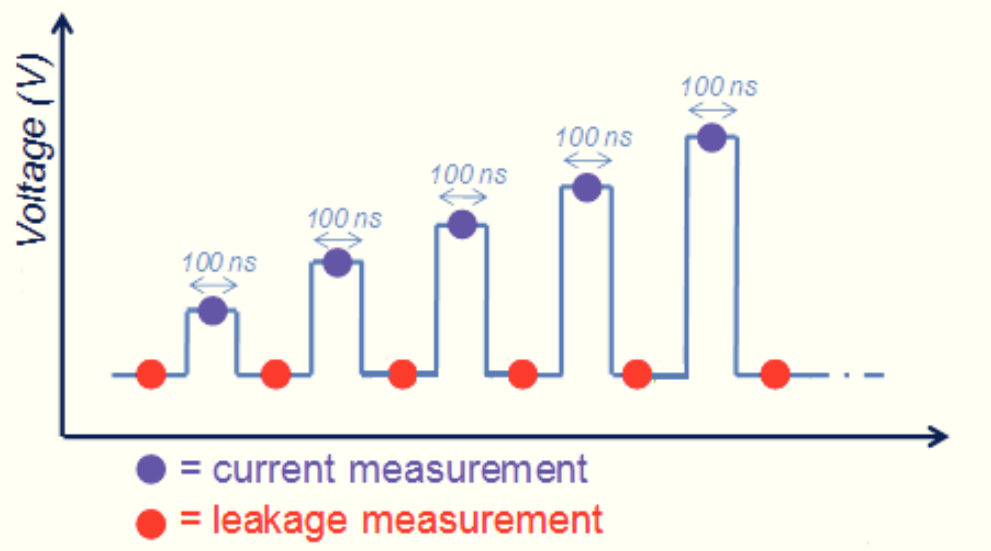


Figure 7.5: Schematic of evolution of TLP stress test carried out on analyzed RGB devices. Note that this schematic does not include the optical characterization performed on some of the tested samples.

7.2 Results of ESD tests on RGB multichip LEDs

In this section first the results of ESD tests carried out under forward bias on the analyzed RGB multichip LEDs will be presented and discussed. Afterwards,

the results of ESD tests for the reverse bias condition will be investigated. In particular, in the following we will present the results obtained on representative samples from the four different suppliers.

7.2.1 ESD tests under forward bias

Figure 7.6 reports the averaged TLP failure currents measured on the four analyzed LED families of RGB LEDs submitted to ESD tests under forward bias. The failure criterion chosen for this analysis corresponds to a forward leakage current of 10 μA measured at 1 V. From the histogram, it can be noticed that for all analyzed suppliers red LEDs have a higher ESD robustness with respect to green and blue LEDs. In particular, red LEDs of supplier 'A', 'B' and 'D' do not fail after a 37 A pulse, which is the maximum TLP current that can reach the TLP system used for this study. However, also red LEDs of family 'C' show a very high failure level compared to green and blue devices of the same RGB sample, in the order of 34 A. On the other hand, green and blue LEDs show a comparable ESD robustness in all analyzed families, except for devices of supplier 'C', probably due to their high variability in the failure current, as it can be noticed from the error bars shown in Figure 7.6.
The higher ESD sensitivity of green and blue LEDs with respect to red devices can be attributed to the high defectiveness of GaN, compared to AlInGaP. In particular, the low robustness of InGaN-based devices, such as green and blue LEDs, is consistent with results reported in [96], in which the ESD failure of these devices has been explained as due to the fact that they have high densities of structural defects; in fact, we can remember from chapter 4 that structural defects may act as preferential paths for current conduction.
In principle, the higher ESD robustness of red LEDs with respect to green and blue ones may be also attributed to the fact that AlInGaP-based LEDs usually have a vertical structure, while in GaN-based devices grown on sapphire substrate, both contacts are made in the front size of device. This results in a strong *current crowding* phenomenon, which can reduce the ESD robustness of GaN-based devices with such a contact structure. However, this is not the case for green and blue LEDs of family 'C', since they have a vertical structure as red LEDs, as shown in Figure 7.2, and thus in reality no correlation can be found between the ESD sensitivity of LEDs and their contact structure.

In Figures 7.7(a) and (b) are reported the typical current-voltage (I-V) characteristic and the leakage current evolution measured during positive TLP test on one of the analyzed RGB LEDs, in this case one from family 'C'. As it can be observed, both green and blue devices show a catastrophic failure, resulting in a short-circuiting of the junction (i.e. the device shows a ohmic-like behavior after

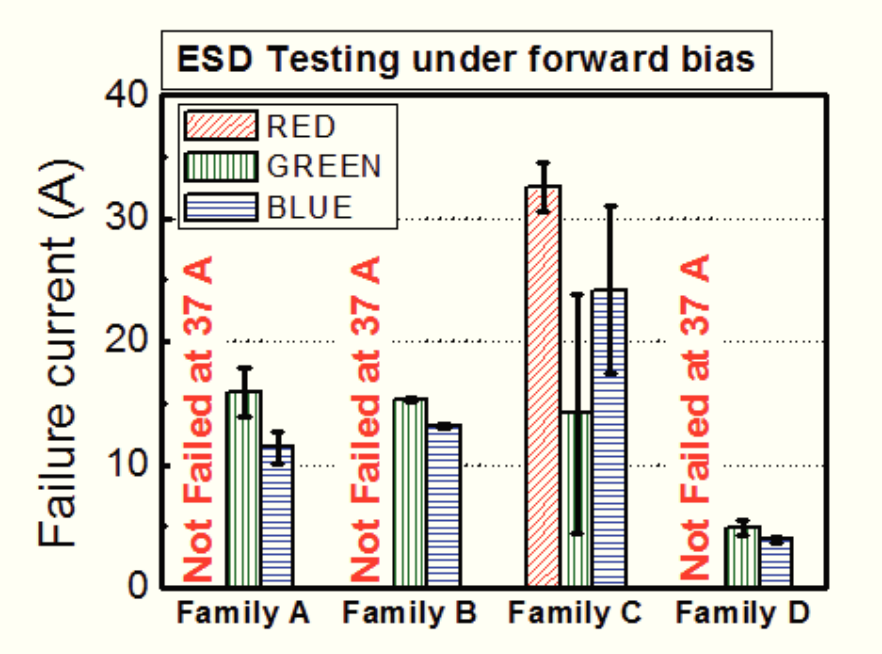


Figure 7.6: Averaged TLP failure currents for the red, green and blue LEDs of the four analyzed sample families. Results are referred to forward bias TLP tests.

the failure) and in an abrupt leakage increase. On the other hand, not failed red devices show only a slight increase in the leakage current at high TLP current levels. In particular, note in Figure 7.7(a) that red LED does not fail after a 37 A pulse, even if it reaches very high current and voltage levels compared to green and blue devices. Finally, it is important to point out that RGB devices of suppliers 'A', 'B' and 'D' have shown very similar characteristics to those reported in Figure 7.7 for family 'C' and thus, for this reason, they have not been reported in the following of this section.

7.2.2 ESD tests under reverse bias

As done in the previous section for TLP tests carried out under forward bias, in Figure 7.8 we report the averaged TLP failure currents measured on the four analyzed LED families of RGB LEDs submitted to ESD tests under reverse bias. The failure criterion chosen in this case corresponds to a reverse leakage current of 10 μA measured at $-5\ V$. Similarly to the forward bias condition, also in this case red LEDs exhibit the largest ESD robustness compared to green and blue devices. On the other hand, these latter have again comparable sensitivity, as it can be observed in the histogram of Figure 7.8. Also in this case the higher ESD robustness of red LEDs, with respect to green and blue devices, was attributed to the high defectiveness of GaN compared to AlInGaP, possibly related to the presence of a high density of dislocations in gallium nitride. In fact, as it has been discussed in

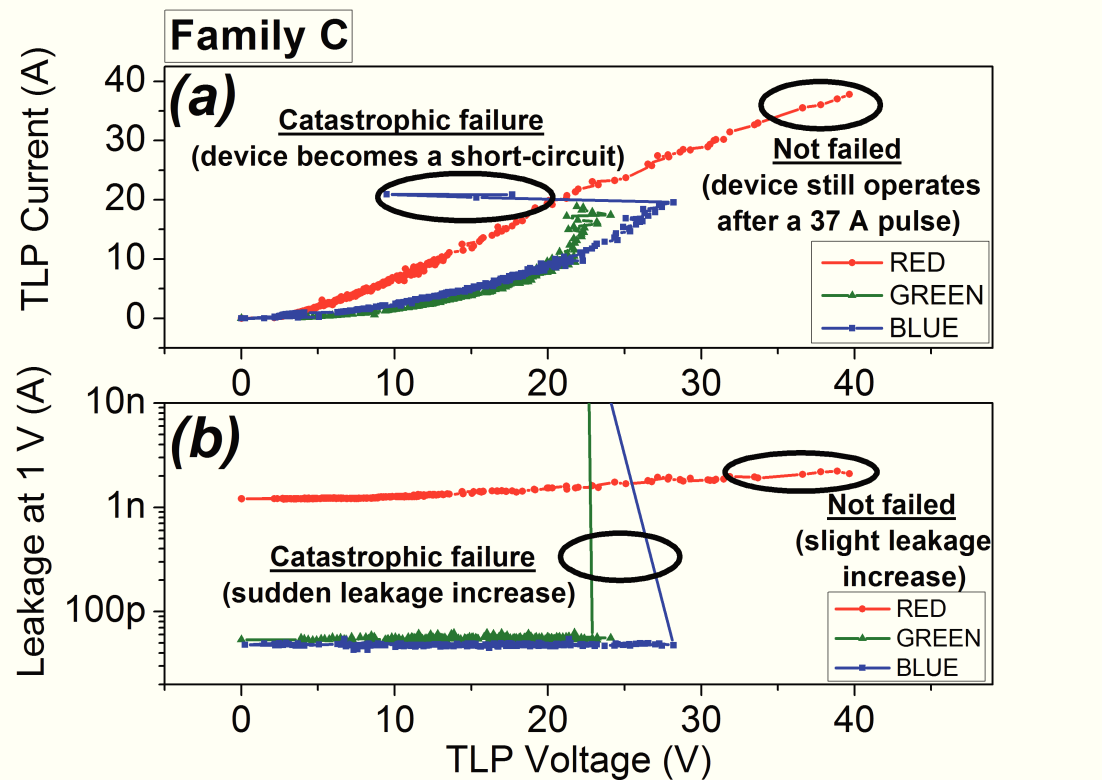


Figure 7.7: (a) Pulsed *I-V* characteristic (i.e. each point represents the current/voltage pair measured during one of the applied TLP pulses) and (b) leakage current evolution of a representative RGB sample of supplier 'C'. The device was submitted to forward bias TLP testing.

chapter 4, in GaN-based LEDs leakage current under reverse bias flows through defective paths related to the presence of dislocations. Thus, during an ESD event, the high discharge current can flow through these structural defects, determining a high localized heating and the premature failure of devices. In particular, the relation between threading dislocations and ESD sensitivity of GaN-based LEDs was already discussed in previous reports [97] [98]. Moreover, note that also in this case no correlation can be found between the ESD robustness of devices under reverse bias and the contact structure, since the conduction processes under reverse bias are not usually influenced by the contact layout of LEDs.

From the comparison between Figures 7.6 and 7.8 (note that the same vertical scale has been used in both histograms), it can be noticed that most of the investigated LEDs show a lower failure current under reverse bias with respect to the forward bias case. This result can be explained by the fact that during TLP tests carried out under forward bias, the voltage reached by the junction is significantly lower than that reached under reverse bias condition (see the comparison between quasi-static *I-V* curves reported in Figures 7.7 and 7.9, respectively). This results, for the same TLP current level, in a significantly lower dissipated power under

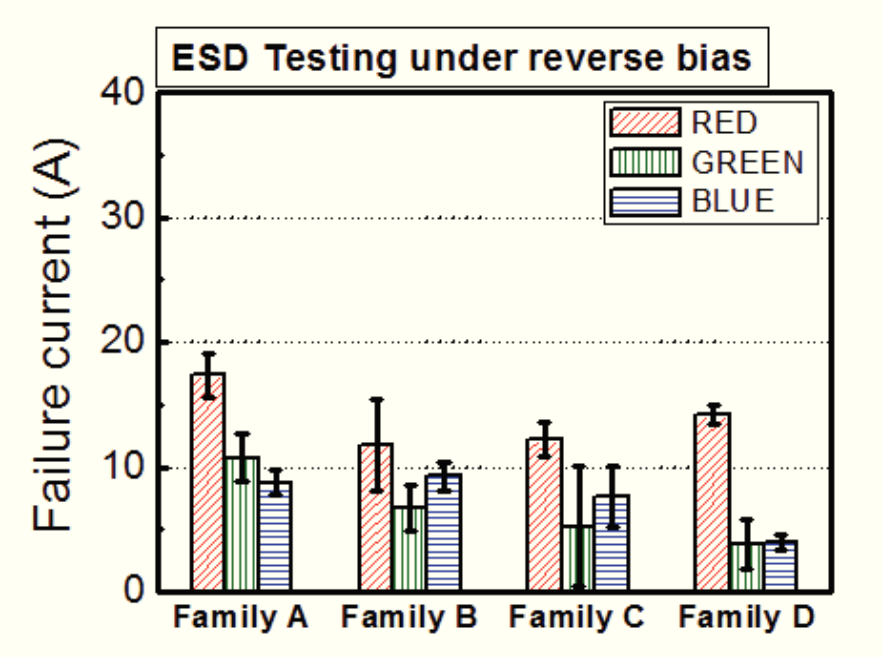


Figure 7.8: Averaged TLP failure currents for the red, green and blue LEDs of the four analyzed sample families. Results are referred to reverse bias TLP tests.

forward bias than under reverse bias condition, and thus the devices can reach higher current levels under positive TLP tests without reaching the thermal runway. Furthermore, under forward bias conditions the whole device area is supposed to contribute to current flow (apart from current crowding effects). On the other hand, under reverse bias the current flows only through localized leakage paths, as discussed in chapter 4, which can reach extremely high dissipated power, therefore being more prone to failure.

With a few exceptions, also under reverse bias ESD tests, green and blue LEDs have shown a catastrophic failure, with an abrupt leakage increase and short-circuiting of the junction, as shown in the I-V characteristic and leakage evolution of Figure 7.9, which is referred to one of the analyzed LEDs of family 'A'.

However, it is very interesting to observe from leakage current evolution shown in Figure 7.9, that non-destructive ESD events (i.e. ESD pulses with a voltage/current level lower than the failure threshold) can significantly modify the electrical characteristics of GaN-based devices under reverse bias, by determining a decrease of the leakage current. This phenomenon is highlighted also in Figure 7.10, which shows an enlargement of leakage evolution of Figure 7.9 in the region before failure. As suggested in [96], this phenomenon can be associated to the annihilation of some of the defective paths responsible for the reverse bias conduction, due to the high-current densities injected through them during TLP pulses. In particular, this fact is also confirmed by false-color emission images shown in Figure 7.11, which are referred to a green LED of supplier 'B' submit-

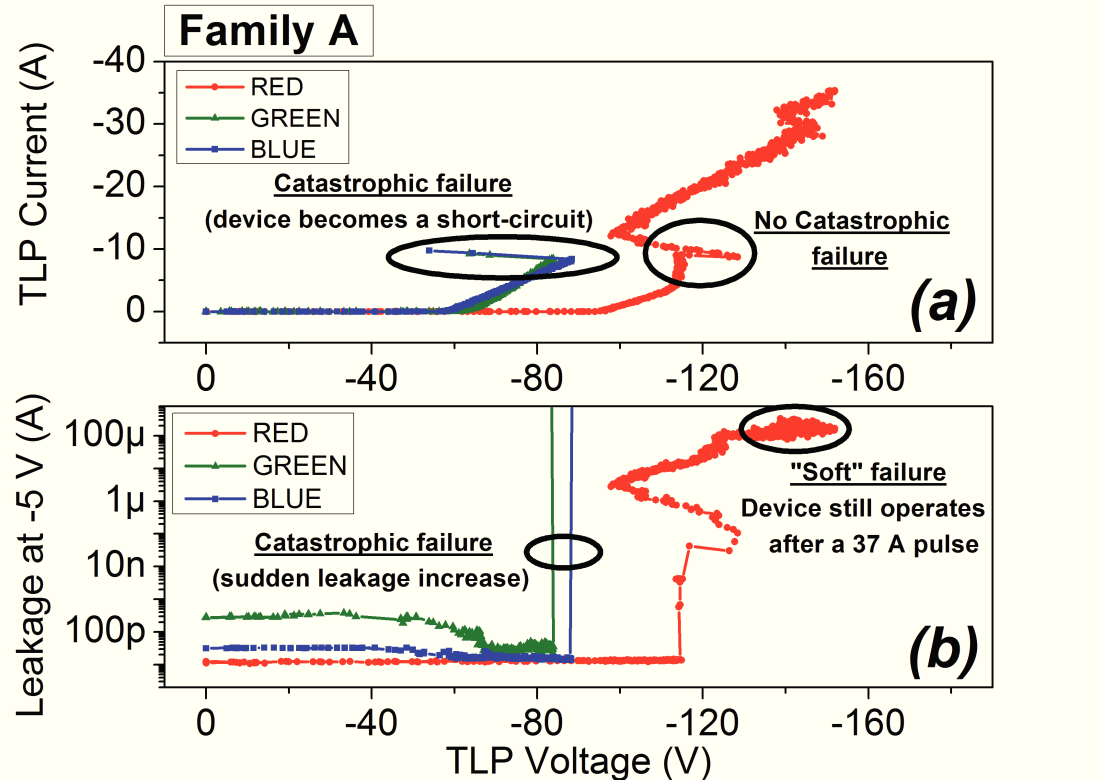


Figure 7.9: (a) Pulsed *I-V* characteristic (i.e. each point represents the current/voltage pair measured during one of the applied TLP pulses) and (b) leakage current evolution of a representative RGB sample of supplier 'A'. The device was submitted to reverse bias TLP testing.

ted to a non-destructive reverse ESD test: as it has been discussed in chapter 4, each localized luminescence spot can be identified as a preferential path for leakage current conduction, possibly related to the presence of structural defects, such as threading dislocations, and it can easily noticed from the comparison between Figures 4(b) and (c) that after non-catastrophic TLP test some of them disappear.

On the other hand, from Figures 7.9 and 7.10 it can be noticed that red LEDs of family 'A' show a completely different behavior. First of all, from Figure 7.10 we can observe that there is no particular variation in the leakage current of red LED before failure, probably due to the low defectiveness of AlInGaP with respect to GaN. Second, Figure 7.9 points out that red devices of supplier 'A' showed a "soft" failure, than rather a catastropic failure as green and blue LEDs, which consists in a gradual increase of the leakage current induced by negative pulses with a current higher than a given threshold, probably due to the generation of parasitic shunt paths. Note also from the *I-V* curve of Figure 7.9(a), that after this "soft" failure the LED shows a ohmic-like behavior. In order to better understand this particular failure mechanism and to analyze as it influences the optical properties of LEDs,

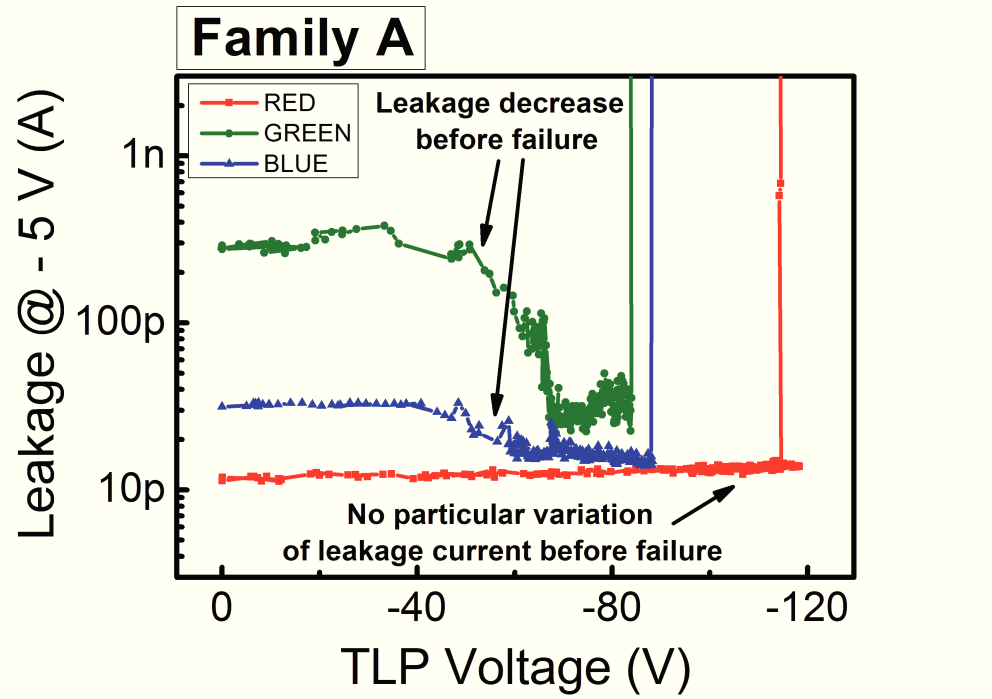


Figure 7.10: Enlargement of leakage evolution shown in Figure 7.9, which highlights the decrease of the leakage current occurring in GaN-based LEDs for negative pulses smaller than the failure threshold.

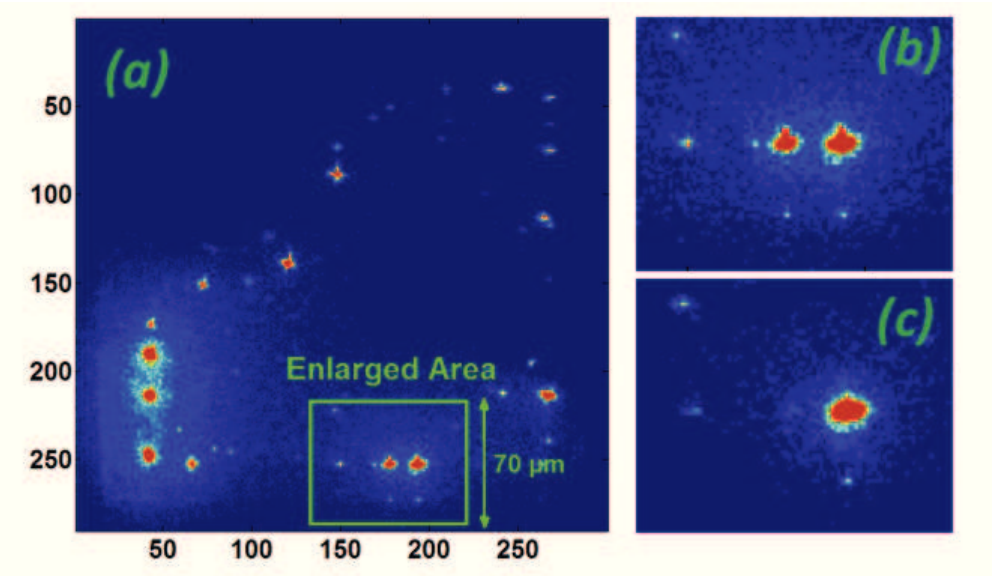


Figure 7.11: (a) False-color emission image taken at -45 V before ESD test on one of the analyzed green LEDs from supplier 'B'. (b) Enlarged image of the region highlighted in (a), and (c) same area as in (b), taken after non-destructive TLP test: note in this case that some of the luminescence spots have disappeared.

also optical power-current (L-I) characteristics were measured during ESD tests. The results of L-I measurements carried out on a representative red LED of family

'A' during negative TLP test are reported in Figure 7.12: as it can be observed, the optical power gradually decreases with increasing TLP current level above a given threshold. However, after the TLP test, the LED still emits light at high current levels and thus it can still operate after a 37 A pulse. Nevertheless, the long-term reliability of LED could be reduced.

In particular, the comparison between the evolution of leakage current and optical

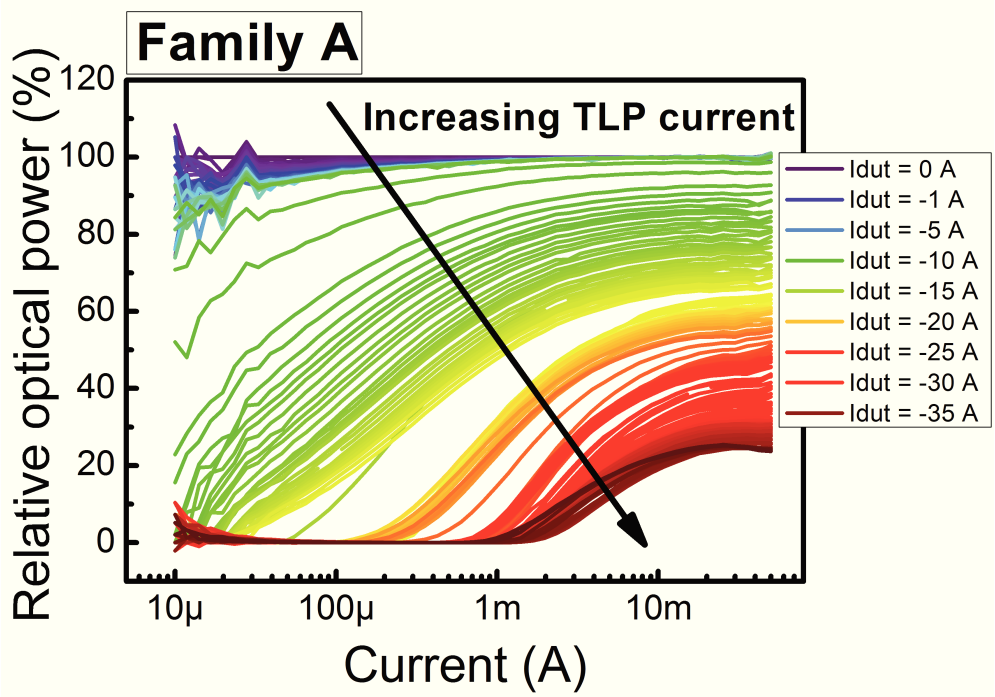


Figure 7.12: Relative optical power as a function of current, measured during TLP test on one of the analyzed red LEDs of supplier 'A'. Curves are normalized with respect to the optical power measured before the ESD test.

power during test, shown in Figure 7.13, reveals that the onset of electrical and optical degradation occurs at the same TLP current level: this "partial" degradation of red LEDs during ESD test can be explained by considering that non-destructive ESD events can induce the generation of shunt paths, which increase leakage current and decrease the optical efficiency at low measuring current levels.

However, it is important to point out that red LEDs of suppliers 'B' and 'C' have shown a catastrophic failure as GaN-based devices, than rather a "soft" failure as red LEDs of supplier 'A', resulting in a short-circuiting of the junction and in an abrupt leakage increase. Thus, the robustness of red LEDs is strongly dependent on material quality.

To conclude the investigation of failure mechanisms occurring on RGB devices under reverse bias, also the particular behavior shown by both red, green and blue LEDs of supplier 'D' has been analyzed. In figure 7.14 are reported the pulsed current-voltage (I-V) characteristics and the leakage current evolution measured

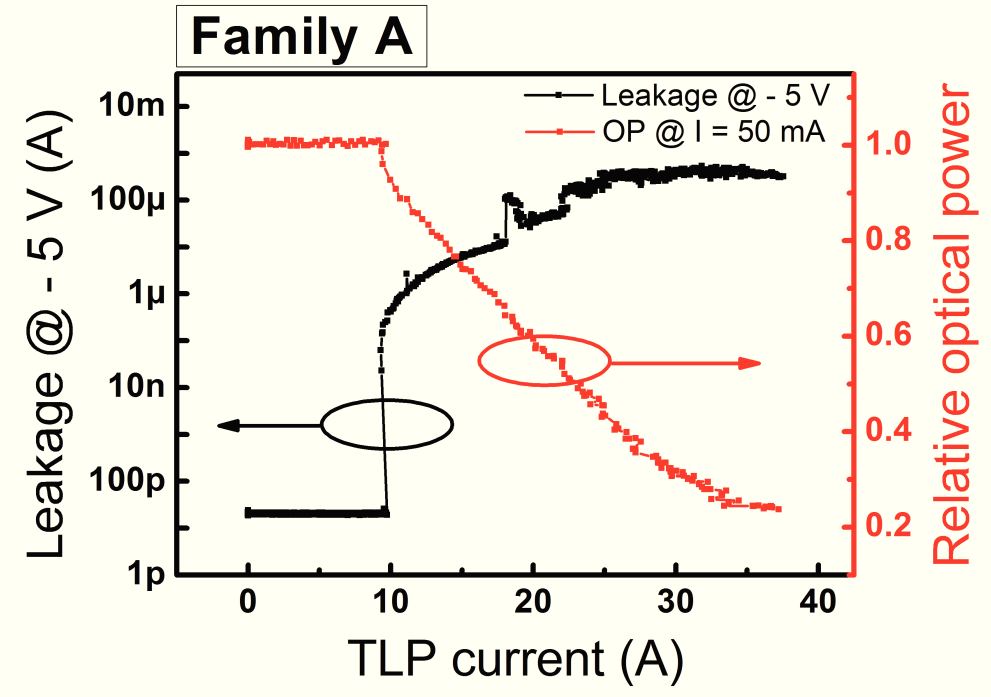


Figure 7.13: Leakage current measured at -5 V and optical power normalized with respect to the initial value, as a function of TLP current, for a representative red LED of supplier 'A', submitted to ESD test under reverse bias.

during ESD test on one of the analyzed RGB multichip LEDs of family 'D'. As it can be noticed from the figure, LEDs show two failures: an initial failure, labeled as 'F1', can be recognized as a sudden decrease in device impedance and in an abrupt leakage increase. However, after this initial failure the devices still emit light. Instead, the second failure corresponds to the condition in which LEDs do not longer emit light.

In order to better understand how these two failure mechanisms influence the electrical and optical properties of devices, also *I-V* and *L-I* measurements were carried out after the application of each pulse and the results are reported in Figure 7.15. In particular, the current-voltage characteristics measured before and after the critical steps of TLP test, shown in Figures 7.15(a), (c) and (e), confirm the result reported above and indicate that the first failure 'F1' results is the generation of a shunt parasitic leakage path. Remarkably, optical power-current characteristics measured before and after the critical steps of TLP test, shown in Figures 7.15(b), (d) and (f), indicate that the first failure 'F1' does not induce a catastrophic quenching of the EL signal emitted by the devices. In fact, even after the first failure, the LEDs still emit a significant EL signal: in particular, *L-I* curves measured after failure 'F1' appear rigidly shifted towards higher current levels with respect to that measured before failure. These results can be explained by considering that the first failure induces the generation of parasitic

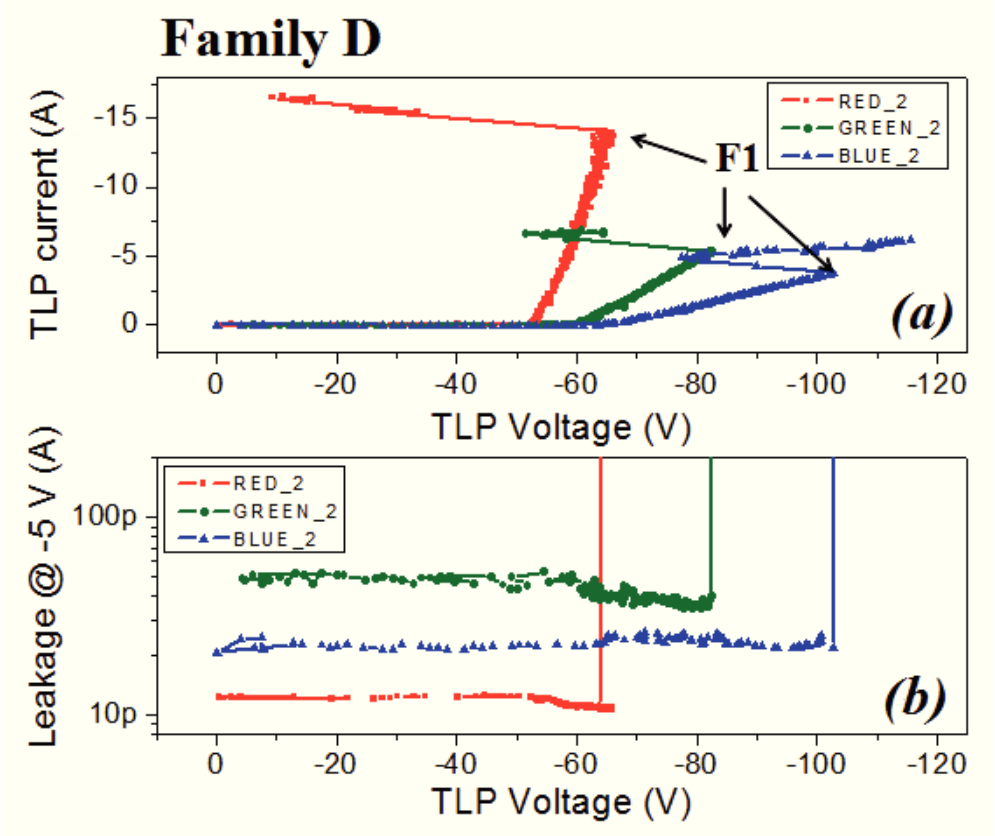


Figure 7.14: (a) Pulsed *I-V* characteristic (i.e. each point represents the current/voltage pair measured during one of the applied TLP pulses) and (b) leakage current evolution of a representative RGB sample of supplier 'D'. The device was submitted to reverse bias TLP testing. Note that the first failure is labeled as 'F1'.

shunt paths, as suggested above from *I-V* curves, which can effectively reduce the amount of carriers injected in the quantum well region, thus inducing a rightwards shift of optical power-current characteristics. Note also from Figure 7.14 that the devices can withstand several further TLP pulses with increasing amplitude, before reaching the complete quenching of electroluminescence signal. Thus, this RGB LEDs are characterized by a "critical" current level beyond which the shunt resistance of the devices starts decreasing, thus significantly affecting their electro-optical properties, without determining a complete shortening of the junction. This kind of failure, which is not always easily detected by the end user, since LED still emit light, can also lead to the instability of the electrical properties of LEDs. In fact, it is clearly visible in Figure 7.15(e) that some of the leakage paths generated by non-destructive ESD events can be partially annihilated by the flow of current, as it has been already seen above: note that the current-voltage curve measured immediately after the first failure 'F1' shows a sudden decrease when the device current becomes greater than about 3 mA, indicating a partial decrease in the parasitic leakage current induced by the measurement itself.

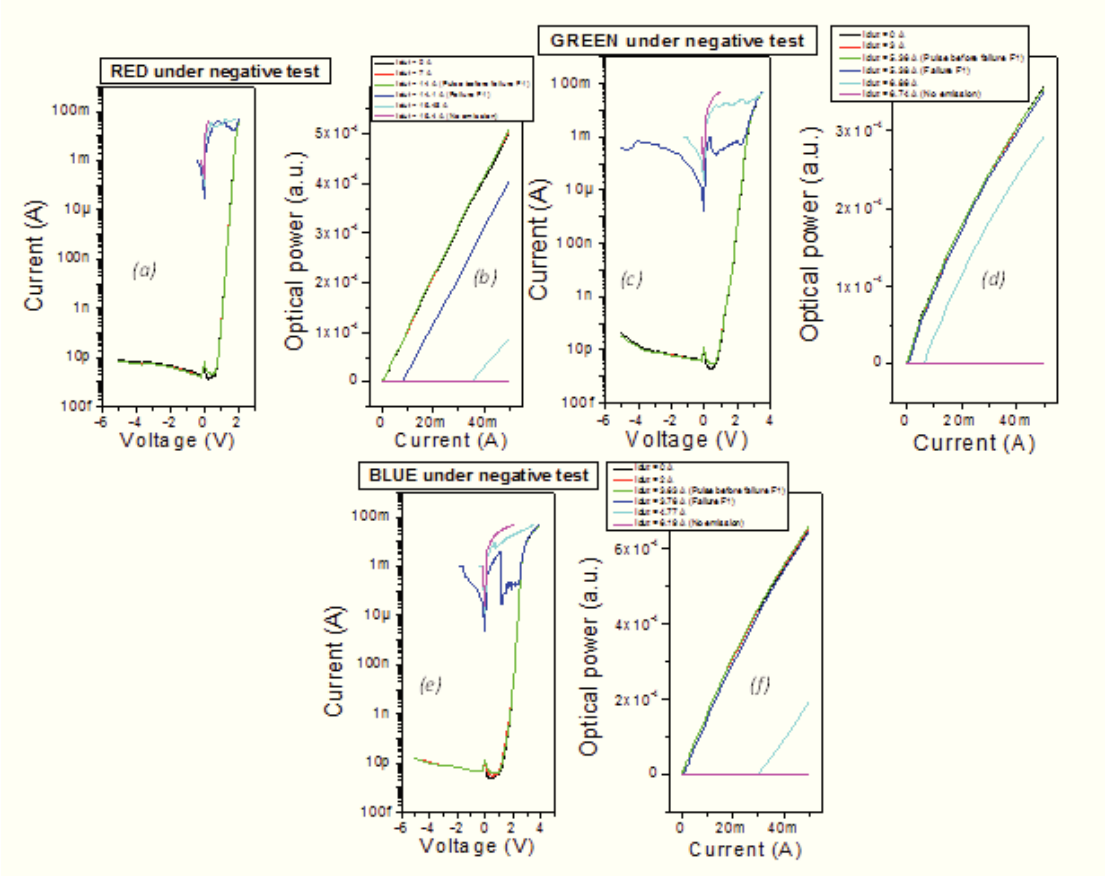


Figure 7.15: (a), (c), (e) Current-voltage characteristics measured during negative TLP test on a red, green and blue LED of family 'D', respectively. (b), (d), (f) Corresponding optical power-current characteristics measured during ESD test and referred to the same samples as in (a), (c) and (e).

To conclude, it is important to point out that the instability effect of electrical properties of LEDs discussed above can occur also during device operation, leading to fluctuation in the optical signal of the devices. As an example, in Figure 7.16 it is reported the variation of the optical power and the forward voltage of a representative blue LED of family 'D', both normalized with respect to their initial values measured before ESD test, which has been removed from the ESD testing setup immediately after it reached the first failure 'F1' and submitted to constant bias at 10 mA. As it can be observed, immediately after turn-on, the optical power and the voltage of the device show fluctuations. However, after some tens of seconds, the operating voltage and the optical power show a significant increase. In particular, this effect may be due to the fact that the exposure to forward bias leads to the partial annihilation of the shunt paths generated during ESD failure 'F1', thus partially recovering the initial performance of LED. Thus, we have seen that ESD events which do not lead to a permanent failure of the devices, can significantly affect the stability of a system based on LEDs.

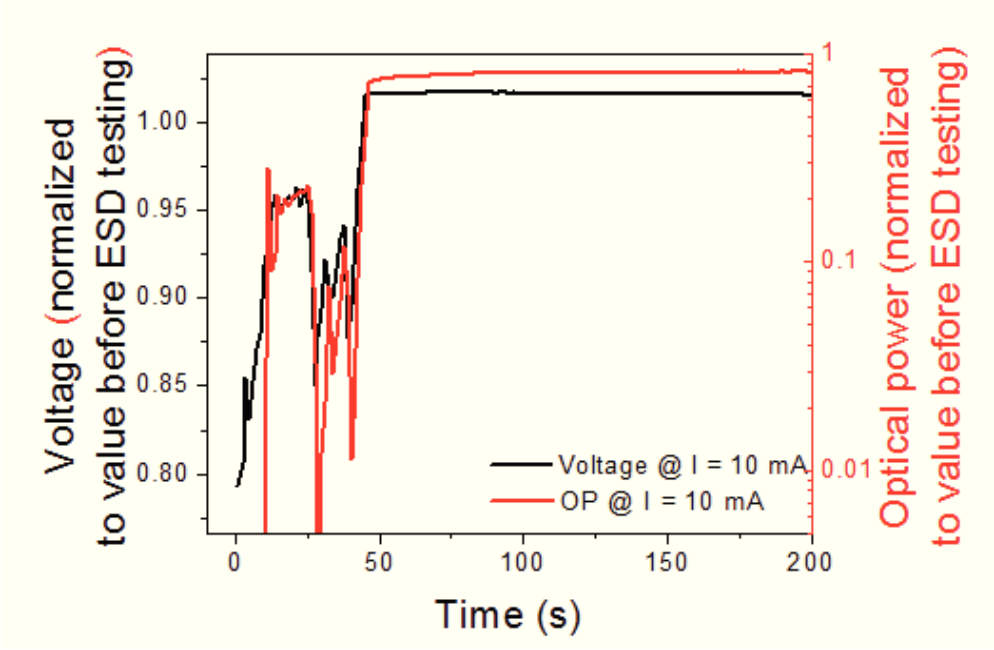


Figure 7.16: Variation of the forward voltage and the optical power measured at 10 mA on a blue LED of family 'D', that has been submitted to non-destructive ESD test under reverse bias, until the first failure 'F1'. After that, it has been removed from the TLP system and submitted to constant current operation. The device was biased at 10 mA, in order to observe the partial recovery of the electrical and optical characteristics. Note that the forward voltage and the optical power are normalized with respect to their values measured before the TLP test.

7.3 Temperature dependence of ESD robustness of LEDs

To conclude the analysis of ESD failure mechanisms of LEDs, in this section we propose the results of an ESD characterization performed on white LEDs at different temperature levels. The analysis was carried out on commercially available white LEDs based on phosphor conversion, and thus including a blue chip. The choice to perform this study on this kind of devices, than rather on RGB LEDs analyzed above, is related to the fact that these withe LEDs have shown a very good repeatability in terms of failure current with respect of all analyzed RGB devices. In fact, it is very important to carry out such a type of analysis on LEDs with a very low variability, since the possible variation of ESD robustness at different temperature levels may be very small.

The analysis was carried out at two different temperature levels, 25 $°C$ and 100 $°C$ respectively, in order to simulate two different junction temperatures (note that no constant bias is applied during test to samples). The first temperature obviously simulate operation at room temperature, while 100 $°C$ represent the

condition in which the LED is operating at high current levels, where the junction can reach very high temperature levels. The devices under test were placed on a temperature-controlled oven and the ESD tests were carried out by means of the same TLP system used for ESD characterization of RGB LEDs: thus, for more details about the Transmission Line Pulser, the reader can refer to section 7.1. After each pulse, a leakage measurement was carried out, in order to determine the degradation induced by ESD stress test. Also in this case LEDs were submitted to ESD tests separately under reverse and forward bias conditions, i.e. a group of devices were submitted to negative TLP pulses and another group to positive TLP pulses, in order to analyze the influence of temperature under different operating regimes. The analysis was carried out on a statistically relevant number of samples ($>$ 20 devices).

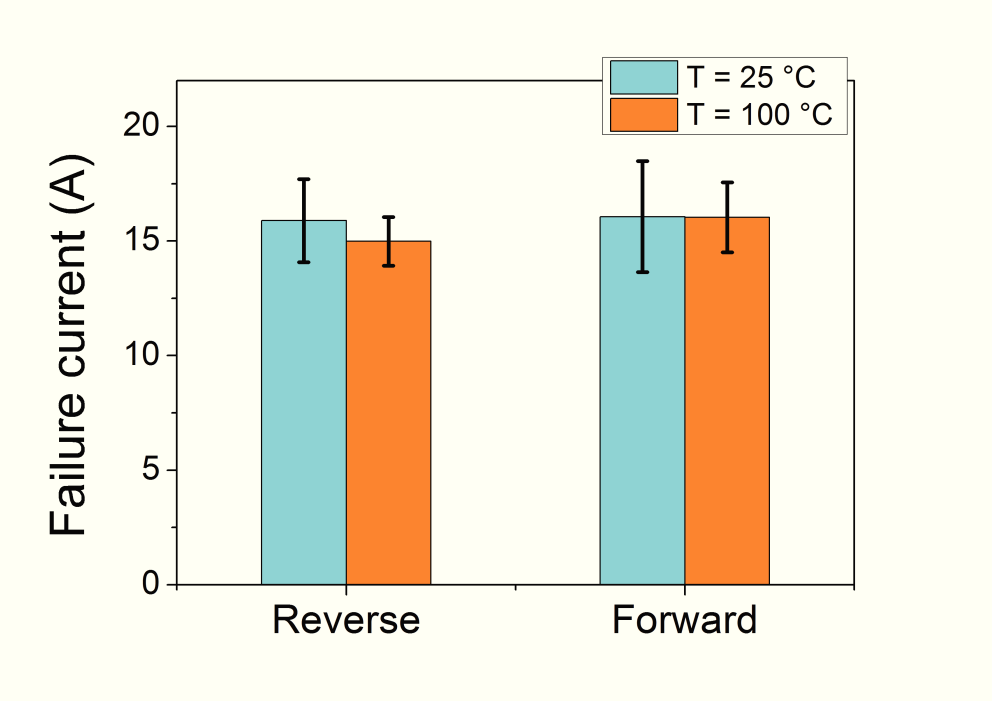


Figure 7.17: Comparison between averaged failure currents measured at low and high temperature levels, on white LEDs submitted to ESD characterization at different temperature levels. The results of ESD tests obtained both under reverse and under forward bias conditions are reported.

In principle, it can be supposed that at high temperature levels the ESD robustness of devices is reduced. In fact, during a destructive ESD event, high current densities are injected through localized regions of the junction, thus determining a high localized heating, that induces the short-circuiting of the junction. Thus, this temperature dependent phenomenon may be favored if the junction is working to a high temperature level. However, as reported in Figure 7.17, which shows the averaged failure currents obtained from this analysis both under reverse and under

forward bias, it can be observed that the operating temperature does not seem to influence the ESD robustness of analyzed LEDs. In fact, the averaged failure currents under forward bias are comparable, while under reverse bias only a slight decrease of the ESD robustness can be observed at 100 $°C$ compared to 25 $°C$. However, from the figure it can be noticed that this difference in the ESD failure level is smaller than the bar errors, and thus this variation in the ESD robustness under this operating regime is probably due to the uncertainty in determining the failure current, than rather to a influence of temperature.

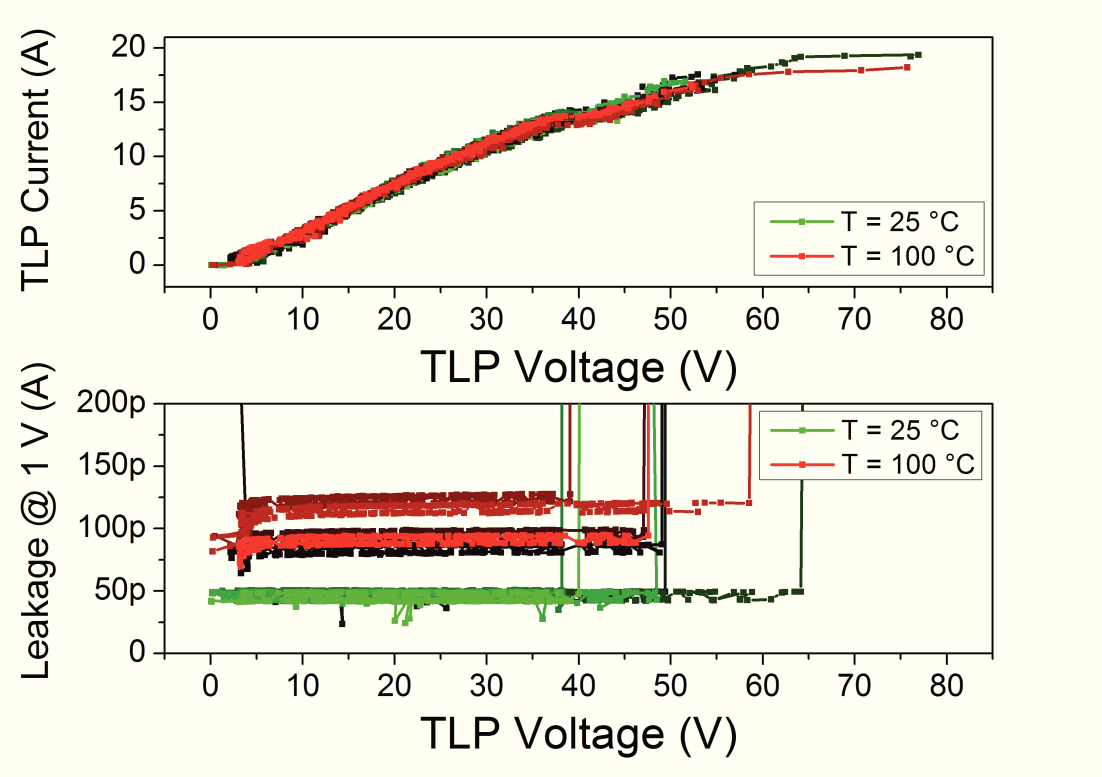


Figure 7.18: Comparison between (a) pulsed I-V characteristics (i.e. each point represents the current/voltage pair measured during one of the applied TLP pulses) and (b) leakage current evolutions of white LEDs submitted to positive TLP tests at 25 $°C$ (green curves) and 100 $°C$ (red curves), respectively.

Also the variations induced by temperature on the quasi-static I-V curves and the leakage evolution measured during TLP test, have been analyzed, and the results are reported in Figures 7.18 and 7.19, for the data obtained under forward and reverse bias, respectively. As it can be noticed, no particular variation can be observed between I-V curves obtained at low and high temperature levels during TLP tests, even though it is well known from chapter 2 that the current-voltage characteristic of a LED has a stronger dependence from temperature both under reverse and under forward bias conditions. This fact can be explained by considering that at high current/voltage levels reached during TLP pulses, the conduction

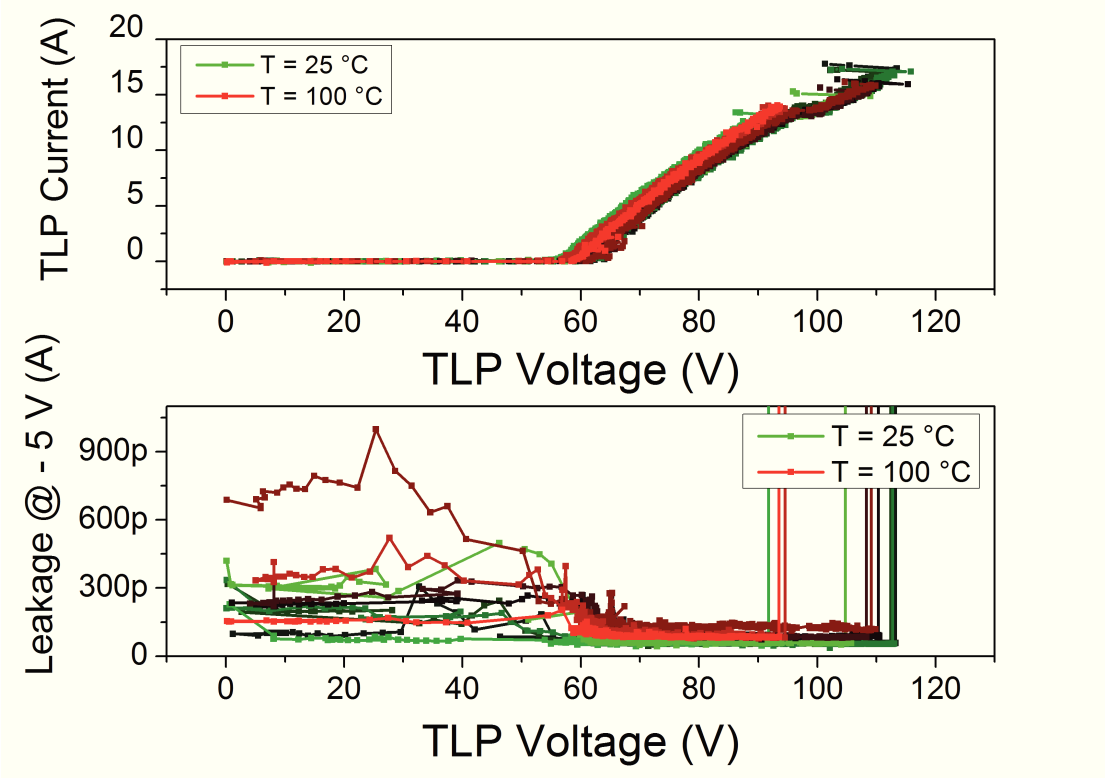


Figure 7.19: Comparison between (a) pulsed I-V characteristics (i.e. each point represents the current/voltage pair measured during one of the applied TLP pulses) and (b) leakage current evolutions of white LEDs submitted to negative TLP tests at 25 $°C$ (green curves) and 100 $°C$ (red curves), respectively.

through devices is dominated by other processes than those of an ideal LED, including breakdown under reverse bias, and effect of the series resistance or current crowding under forward bias (in fact, note the high series resistance of analyzed LEDs in Figure 7.18). Thus, the insensitivity of I-V curves from temperature can be due to the fact that the variations on current-voltage characteristics induced by the conduction processes mentioned above are not detectable in the range of temperatures $25 - 100\ °C$ with the adopted TLP system.
On the other hand, an increase of the leakage current before the ESD failure can be observed on devices submitted to TLP tests at 100 $°C$, both under reverse and under forward bias conditions. In particular, this increase of leakage current is related to the temperature dependence of the current-voltage (I-V) characteristic of LEDs for the low voltage levels at which the leakage measurement has been carried out. However, this increase of leakage current does not seem to influence the ESD robustness of devices both under reverse and under forward bias conditions.

Thus, this analysis has provided useful information on the temperature dependence of ESD robustness of LEDs. In particular, it has been seen that no correlation between temperature and ESD robustness of devices can be found in the analyzed

range $25 - 100\ ^{\circ}C$: this can be attributed to the fact that probably the temperature levels reached within localized regions of the junction during a destructive ESD events are much higher than those adopted for this analysis ($25 - 100\ ^{\circ}C$), thus suggesting that the influence of a high environmental temperature is minimal on the ESD sensitivity of LEDs. Note that, even though this investigation was carried out on commercially available white samples based on phosphor conversion, and thus including a blue chip, these results in general can be extended to all types of GaN-based LEDs.

Conclusions

Within this work, and extensive analysis of the defects and physical mechanisms that limit the ESD robustness of Light-Emitting Diodes has been presented. In particular, most of the research activity was focused on the study of GaN-based LEDs, due to their large employment in many applications, including solid-state lighting, display and projection fields, and to the severe reliability issued related to them. First, an analysis of emission processes related to the presence of defects, and of the carrier distribution and injection processes in multi-quantum well GaN-based LEDs have been presented. Afterwards, the activity was focused on the analysis of physical mechanisms that limit the ESD robustness of blue GaN-based LEDs and on the analysis of typical ESD failure mechanisms occurring on RGB multichip devices. In this final section, the most important and original results obtained from the Ph.D. reasearch activity of the candidate will be summarized.

In the first part of research activity, which results have been reported in chapter 4, we have presented a detailed characterization of localized emission processes occurring in GaN-based LEDs, both under reverse and under low forward bias conditions. In particular, original results obtained from this analysis indicate that:

- When LEDs are operated in the low operating regime, either under reverse or low forward bias conditions, they can show localized luminescent spots.

- Localized emission observed under reverse bias can be ascribed to the injection of carriers through localized defects, with subsequent radiative recombination. In particular, it has been seen that reverse bias luminescence is directly proportional to the injected reverse current and it is also strongly correlated to the threading dislocation density, thus suggesting that threading dislocations act as preferential paths for the injection of carriers in the active region of LEDs under reverse bias.

- Under low forward bias conditions, LEDs can show yellow localized emission, which occurs in proximity of submicrometer-size defects. EL analysis suggests that yellow luminescence originates from defect-related radiative recombination of electrons tunneling out to the barrier layers. In particular,

the origin of yellow luminescence was ascribed to the existence to a deep acceptor level, which is typically present in GaN barrier layers.

After that, the role of current, temperature, hole mobility, and carrier density in limiting the optical efficiency of InGaN-based LEDs with color-coded structure have been discussed in chapter 5. The analysis, based on combined electroluminescence measurements carried out at different current and temperature levels, and 2D simulations, has provided interesting results on the injection and recombination processes occurring in multi-quantum well LEDs. In particular, the most important results shows that:

- There is strong asymmetry in carrier distribution. In particular at low current levels only the quantum well closer to the p-side emits light; on the other hand, by increasing the applied bias also the second quantum well contributes to the emission, while the third quantum well, adjacent to the n-side, does not emit light at every operating condition. The poor efficiency of the second and third quantum well has been attributed to the low density of electrons in these wells, than rather to a poor hole injection. The strong asymmetry in the electron distribution between quantum wells may be also attributed to the absence of an EBL in these structures.

- Results of simulations have confirmed that hole mobility does not act as a bottleneck for carrier injection and recombination in such a type of structure. However, this fact does not necessarily imply that hole mobility cannot play a critical role in determining the performance of MQW LEDs.

- The stronger thermal quenching shown by the first quantum well, adjacent to the p-side and having the highest indium content, can be attributed to the higher non-radiative recombination occurring in the green quantum well with respect to the blue one, due to the higher density of non-radiative defects and to the higher contribution of Auger recombination, thus confirming that also defects can strongly influence the optical efficiency of quantum wells.

- The fact that no emission has been observed from the third quantum well, adjacent to the n-side, can be explained by considering that in the analyzed current and temperature ranges, the concentrations of both electrons and holes in this quantum well are considerably low, compared to those of two other quantum wells.

At this point, the research activity was focused on the study of physical mechanisms that limit the ESD robustness of GaN-based LEDs. The analysis, which has been presented in chapter 6, was particularly focused of the study of role of defects related to the presence of deep levels in influencing the ESD robustness of

devices. The most important results obtained from this investigation have shown that:

- A higher overall capacitance, which corresponds to a higher total charge accumulated in the junction, and thus to a higher electric field in the space charge region of devices, can negatively influence the ESD characteristics of LEDs under reverse bias. This was confirmed by the correlation identified between the First level failure, which represents the ESD robustness of LEDs when submitted to a first ESD event under reverse bias, and the overall junction capacitance.

- All analyzed LEDs have trap states with similar activation energies, but different concentrations. Also a strong correlation has been identified between trapping phenomena related to these deep levels and the ESD robustness when devices are submitted to a second ESD event after a short time from the application of first ESD pulse. In particular, a deep level localized at $E_c - 2.2\ eV$ has been identified as main responsible for trapping phenomena occurring during the application of a ESD event under reverse bias.

- On the other hand, no correlation has been observed between the ESD robustness of analyzed LEDs and their reverse leakage current, reverse bias luminescence and optical power under forward bias, respectively.

Finally, to conclude the analysis of physical mechanisms that limit the ESD robustness of LEDs, in chapter 7 it has been presented an extensive ESD characterization carried out on commercially available RGB devices, in order to achieve a better understanding of the failure mechanisms occurring on LEDs during an ESD event and to compare different technologies in terms of ESD sensitivity, i.e. AlInGaP-based red LEDs and GaN-based green and blue devices. Also the temperature dependence of ESD robustness of commercially available white LEDs, based on phosphor conversion, has been investigated. The main results obtained from this analysis can be summarized as follow:

- The higher ESD sensitivity of green and blue LEDs, with respect to red devices, can be attributed to the higher defectiveness of GaN compared to AlInGaP. On the other hand, any particular correlation has been identified from this analysis between the ESD robustness and the contact structure of devices. Moreover, LEDs are more sensitive to reverse-bias ESD testing, with respect to forward bias stress.

- GaN-based devices typically show a catastrophic failure with short-circuiting of the junction and an abrupt leakage increase. In particular, most of GaN-based devices, after failure, do not longer emit light.

- Most of red LEDs do not fail after positive TLP test. Note that the current limit of employed TLP system is 37 A.
- Some of the analyzed red LEDs have shown "soft" failure, which consists in a gradual worsening of the electrical and optical properties during test.
- TLP negative pulses with current level lower than the failure threshold can strongly influence the electrical properties of GaN-based devices, inducing a decrease in reverse-bias current and luminescence, due to the annihilation of some of the defective paths responsible for reverse current conduction.
- Non-catastrophic failure can also lead to the instability of electrical and optical properties of both red, green and blue LEDs.
- No correlation can be found between the ESD robustness of GaN-based LEDs and their operating temperature, in the analyzed range $(25 - 100\ ^{\circ}C)$.

Note that the results reported above have provided useful information on the role of defects in influencing the electrical and optical properties, and the ESD robustness of LEDs. In particular, these results are of fundamental importance for the future development of high efficient LEDs, characterized by also a high ESD robustness.

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Bibliography

[1] G. Kelly, "Understand color science to maximize success with LEDs," *Part 4 -LED Magazine*, February 2013.

[2] R. D. Dupuis and M. R. Krames, "History, development, and application of high brigthness visible light-emitting diodes," *J. Lightw. Technol.*, vol. 26, no. 9, pp. 1154–1171, May 2008.

[3] G. Meneghesso, M. Meneghini, and E. Zanoni, "Recent results on the degradation of white LEDs for lighting," *J. Phys. D. Appl. Phys.*, vol. 43, no. 35, p. 354007, September 2007.

[4] M. Meneghini, S. Vaccari, N. Trivellin, D. Zhu, C. Humphreys, R. Butendheich, C. Leirer, B. Hahn, G. Meneghesso, and E. Zanoni, "Analysis of defect-related localized emission processes in InGaN/GaN-based LEDs," *IEEE Transactions on Electron Devices*, vol. 59, no. 5, pp. 1416–1422, May 2012.

[5] M. Meneghini, N. Trivellin, M. Pavesi, M. Manfredi, U. Zehnder, B. Hahn, G. Meneghesso, and E. Zanoni, "Leakage current and reverse-bias luminescence in InGaN-based light-emitting diodes," *Applied Physics Letters*, vol. 95, no. 17, pp. 173 507–1–173 507–3, October 2009.

[6] X. A. Cao, S. F. LeBoeuf, K. H. Kim, P. M. Sandvik, E. B. Stokes, A. Ebong, D. Walker, J. Kretchmer, J. Y. Lin, and H. X. Jiang, "Investigation of radiative tunneling in GaN/InGaN single quantum well light-emitting diodes," *Solid State Electron.*, vol. 46, no. 12, pp. 2291–2294, December 2002.

[7] S. K. Zhang, W. B. Wang, A. M. Dabiran, A. Osinsky, A. M. Wowchak, B. Hertog, C. Plaut, P. P. Chow, S. Gundry, E. O. Troudt, and R. R. Alfano, "Avalanche breakdown and breakdown luminescence of AlGaN multiquantum wells," *Applied Physics Letters*, vol. 87, no. 26, pp. 262 113–1–262 113–3, December 2005.

[8] G. Onushkin, J. Lee, J. J. Yang, S. E. Park, M. H. Kim, and M. Koike, "Investigation of local tunneling phenomena in green InGaN-based LEDs," *Phys. Stat. Sol. (C)*, vol. 4, no. 7, pp. 2793–2796, June 2007.

[9] A. Mao, J. Cho, Q. Dai, E. F. Schubert, J. K. Son, and Y. Park, "Characteristics of dotlike green satellite emission in GaInN light emitting diodes," *Applied Physics Letters*, vol. 98, no. 2, pp. 023 503–1–023 503–3, January 2011.

[10] M. F. Schubert, S. Chhajed, J. K. Kim, E. F. Schubert, D. D. Koleske, M. H. Crawford, S. R. Lee, and A. J. Fischer, *Applied Physics Letters 91 (2007) 231114*.

[11] J. Hader, J. V. Moloney, and S. W. Koch, *Applied Physics Letters 96 (2010) 221106*.

[12] Hader and et al., *Applied Physics Letters*, vol. 99, p. 181127, 2011.

[13] A. Laubsch, M. Sabathil, J. Baur, M. Peter, and B. Hahn, "High-power and high-efficiency InGaN-based light emitters," *IEEE Transaction on Electron Devices*, vol. 57, no. 1, pp. 79–87, 2010.

[14] J. Piprek, "Efficiency droop in nitride-based light-emitting diodes," *Phys. Stat. Sol. (a) 207 (10)*, pp. 2217–2225, 2010.

[15] B. Galler, A. Laubsch, A. Wojcik, H. Lugauner, A. Gomez-Iglesias, M. Sabathil, and B. Hahn, *Phys. Stat. Sol. (c)*, vol. 8, no. 7-8, pp. 2372–2374, July 2011.

[16] M. Meneghini, L. Rigutti, L. R. Trevisanello, A. Cavallini, G. Meneghesso, and E. Zanoni, "A model for the thermal degradation of metal/(p-GaN) interface in GaN-based light emitting diodes," *Journal of Applied Physics*, vol. 103, p. 063703, 2008.

[17] M. Meneghini, L.-R. Trevisanello, G. Meneghesso, and E. Zanoni, "A review on the reliability of GaN-Based LEDs," *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 2, pp. 323–331, June 2008.

[18] M. Meneghini, A. Tazzoli, G. Mura, G. Meneghesso, and E. Zanoni, "A review on the physical mechanisms that limit the reliability of GaN-Based LEDs," *IEEE Transactions on Electron Devices*, vol. 57, no. 1, pp. 108–118, January 2010.

[19] M. Meneghini, U. Zehnder, B. Hahn, G. Meneghesso, and E. Zanoni, "Degradation of high-brightness green LEDs submitted to reverse electrical stress," *IEEE Electron Device Letters*, vol. 30, no. 10, pp. 1051–1053, Ocotber 2009.

[20] S. J. Chang, C. F. Shen, S. C. Shei, R. W. Chuang, C. S. Chang, W. S. Chen, T. K. Ko, and J. K. Sheu, "Highly reliable nitride-based LEDs with internal ESD protection diodes," *IEEE Transactions on Device and Materials Reliability*, vol. 6, no. 3, pp. 442–447, September 2006.

[21] S. J. Chang, C. H. Chen, Y. K. Su, J. K. Sheu, W. C. Lai, J. M. Tsai, C. H. Liu, and S. C. Chen, "Improved ESD protection by combining InGaN-GaN MQW LEDs with GaN schottky diodes," *IEEE Electron Device Letters*, vol. 24, no. 3, pp. 129–131, March 2003.

[22] S.-C. Shei, J.-K. Sheu, and C.-F. Shen, "Improved reliability and ESD characteristics of flip-chip GaN-based LEDs with internal inverse-parallel protection diodes," *IEEE Electron Device Letters*, vol. 28, no. 5, pp. 346–349, May 2007.

[23] Y. X. Sun, W. S. Chen, S. C. Hung, K. T. Lam, C. H. Liu, and S.-J. Chang, "GaN-based power flip-chip LEDs with an internal ESD protection diode on Cu sub-mount," *IEEE Transactions on Advanced Packaging*, vol. 33, no. 2, pp. 433–437, May 2010.

[24] S. Hwang and J. Shim, "Improved ESD voltage by inserting floating metal ring in GaN-based light emitting diodes," *Electronic Letters*, vol. 44, no. 9, April 2008.

[25] L.-B. Chang, K.-L. Chiang, H.-Y. Chang, M.-J. Jeng, C.-Y. Yen, C.-C. Lin, Y.-H. Chang, M.-J. Lai, Y.-L. Lee, and T.-W. Soong, "Electrostatic reliability characteristics of GaN flip-chip power light-emitting diodes with metal-oxide-silicon submount," *IEEE Transactions on Electron Devices*, vol. 57, no. 1, pp. 119–124, January 2010.

[26] T. H. Chiang, Y. Z. Chiou, S. J. Chang, C. K. Wang, T. K. Ko, T. K. Lin, C. J. Chiu, and S. P. Chang, "Improved optical and ESD characteristics for GaN-based LEDs with an n^--GaN layer," *IEEE Transactions on Devices and Materials Reliability*, vol. 11, no. 1, pp. 76–80, March 2011.

[27] T.-Y. Park, M.-S. Oh, and S.-J. Park, "Improvement of electrostatic discharge characteristics and optical properties of GaN-based light-emitting diodes," *IEEE Electron Device Letters*, vol. 30, no. 9, pp. 937–939, September 2009.

[28] R. Quay, *Gallium Nitride Electronics*. Springer Series in Materials Science, 2008.

[29] J. Edgar, "Properties of group III nitrides," *EMIS Data reviews series, ed. by J. Edgar (IEE INSPEC)*, no. 11, pp. 7–21, 1994.

[30] F. Bernardini, V. Fiorentini, and D. Vanderbilt, *Physics Review B 56, R10024*, 1997.

[31] O. Ambacher, B. Foutz, J. Smart, J. Shealy, N. Weimann, K. Chu, M. Murphy, A. Sierakowski, R. Dimitrov, A. Mitchell, and M. Stutzmann, *Journal of Applied Physics 87, 334*, 2000.

[32] O. Ambacher, "Growth and applications of group III nitrides," *Journal of Physics D: Applied Physics*, vol. 31, pp. 2653–2710, 1998.

[33] D. Jho, J. Yahng, E. Oh, and D. S. Kim, "Measurement of piezoelectric field and tunneling times in strongly biased AlGaN/GaN quantum wells," *Applied Physics Letters*, vol. 79, pp. 1130–1132, 2005.

[34] E. F. Schubert, *Light Emitting Diodes*, 2nd ed. Cambridge University Press, 2006.

[35] K. L. Bunker, R. Garcia, and P. E. Russella, "Scanning electron microscopy cathodoluminescence studies of piezoelectric fields in an AlGaN/GaN quantum well light emitting diode," *Applied Physics Letters*, vol. 86, pp. 082 108–1–082 108–3, 2005.

[36] K. Evans, *Compound Semiconductors*, vol. 10, 2004.

[37] J. Newey, *Compound Semiconductors*, vol. 8, 2002.

[38] W. C. Johnson and J. B. Parson, "Nitrogen compounds of gallium," *Journal Physics Chem.*, vol. 36, pp. 2588–2594, 1932.

[39] H. Hamano, N. Sawaki, I. Akasaki, and Y. Toyoda, "Metalorganic vapor phase epitaxial growth of a high quality GaN film using an AlN buffer layer," *Applied Physics Letters*, vol. 48, pp. 353–355, 1986.

[40] I. Akasaki and H. Hamano, "Crystal structure, mechanical properties and thermal properties of GaN," *IEEE International Electron Device Meeting*, vol. 96, p. 231, 1996.

[41] J. E. V. Nostrand, J. Solomon, A. Saxler, Q.-H. Xie, D. C. Reynolds, and D. C. Look, *Journal of Applied Physics*, vol. 87, no. 12, pp. 8766–8772, 2000.

[42] S. C. Jain, M. Willander, J. Narayan, and R. V. Overstraeteten, "III-nitrides: growth, characterization and properties," *Journal of Applied Physics*, vol. 87, no. 3, pp. 965–1006, 2000.

[43] E. Martinez-Guerrero and et al., "Structural properties of undoped and doped cubic GaN grown on SiC(001)," *Journal of Applied Physics*, vol. 91, no. 8, pp. 4983–4987, 2002.

[44] L. Liu and J. Edgar, "Substrates for gallium nitride epitaxy," *Materials Science and Engineering*, vol. R37, pp. 61–127, 2002.

[45] M. A. Sanchez-Garcia, F. B. Naranjo, J. L. Pau, A. Jimenez, E. Calleja, and E. M. Noz, "Utraviolet electroluminescence in GaN/AlGaN single-heterojunction light-emitting diodes grown on Si(111)," *Journal of Applied Physics*, vol. 87, no. 3, pp. 1569–1571, 2000.

[46] S. A. Kukushkin and et al., "Substrates for epitaxy of gallium nitride: new materials and techniques," 2007.

[47] X. Xu, R. P. Vaudo, C. Loria, A. Salant, G. R. Brandes, and J. Chaudhuri, "Growth and characterization of low defect GaN by hydride vapor phase epitaxy," *Journal of Crystal Growth*, vol. 246, no. 3-4, pp. 223–229, 2002.

[48] M. Hermann, D. Gogova, D. Siche, M. Schmidbauer, B. Monemar, M. Stutzmann, and M. Eickhoff, "Nearly stress free substrates for GaN homoepitaxy," *Journal of Crystal Growth*, vol. 293, no. 2, pp. 462–468, 2006.

[49] Y. Kumagai, T. Nagashima, and A. Koukito, *Japanese Journal of Applied Physics 46, L389*, 2007.

[50] H. P. Maruska and J. J. Tietjen, "The preparation and properties of vapor-deposited single crystal-line GaN," *Applied Physics Letters*, vol. 15, no. 10, pp. 327–329, 1969.

[51] S. Nakamura, S. Pearton, and G. Fasol, *The blue laser diode: the complete history*, 2nd ed. Springer, 2000.

[52] H. Morcoc, S. Strite, G. B. Gao, M. E. Lin, B. Sverdlov, and M. Burns, "Large-band-gap SiC, III-V nitride, and II-VI ZnSe-based semiconductor device technologies," *Journal of Applied Physics*, vol. 76, no. 3, pp. 1363–1398, 1994.

[53] C. G. V. de Walle, C. Stampfl, and J. Neugebauer, "Theory of doping and defects in III-V nitrides," *Journal of Crystal Growth*, vol. 505, 1998.

[54] C. G. V. de Walle and J. Neugebauer, "First-principles calculations for defects and impurities: applications to III-nitrides," *Journal of Applied Physics*, vol. 95, no. 8, pp. 3851–3879, 2004.

[55] J. Neugebauer and C. G. V. de Walle, "Chemical trends for acceptor impurities in GaN," *Journal of Applied Physics*, vol. 85, no. 5, pp. 3003–3005, 1999.

[56] H. Amano, M. Kito, K. Hiramatsu, and I. Akasaki, "p-type conduction in Mg-doped GaN treated with low energy electron beam irradiation (LEEBI)," *Japanese Journal of Applied Physics*, vol. 28, pp. L2112–L2114, 1989.

[57] D. H. Youn, M. Lachab, M. Hao, T. Sugahara, H. Takenaka, Y. Naoi, and S. Sakai, "Investigation on the p-type activation mechanism in Mg-doped GaN films grown by metalorganic chemical vapor deposition," *Japanese Journal of Applied Physics*, vol. 38, pp. 631–634, 1999.

[58] M. Miyachi, T. Tanaka, Y. Kimura, and H. Ota, "The activation of Mg in GaN by annealing with minority-carrier injection," *Applied Physics Letters*, vol. 72, no. 9, pp. 1101–1104, 1998.

[59] D. W. Jenkins and J. D. Dow, "Electronic structures and doping of InN, $In_xGa_{1-x}N$ and $In_xAl_{1-x}N$," *Physics Review B*, vol. 39, no. 5, pp. 3317–3329, 1989.

[60] S.-W. Kim, J.-M. Lee, C. Huh, N.-M. Park, H.-S. Kim, I.-H. Lee, and S.-J. Park, "Reactivation of Mg acceptor in Mg-doped GaN by nitrogen plasma treatment," *Applied Physics Letters*, vol. 76, no. 21, pp. 3079–3081, 2000.

[61] A. Weimar, A. Lell, G. Brudel, S. Bader, and V. Harle, "Investigation of low-resistance metal contacts on p-type GaN using the linear and circular transmission line method," *Physica Status Solidi A*, vol. 183, pp. 169–175, 2001.

[62] S. N. Mohammad, "Contact mechanisms and design principles for alloyed ohmic contacts to n-GaN," *Journal of Applied Physics*, vol. 95, no. 12, pp. 7940–7953, 2004.

[63] A. Motayed, R. Bathe, M. C. Wood, O. S. Diouf, R. D. Vispute, and S. N. Mohammad, "Electrical, thermal, and microstructural characteristics of Ti/Al/Ti/Au multilayer ohmic contacts to n-type GaN," *Journal of Applied Physics*, vol. 93, no. 2, pp. 1087–1094, 2003.

[64] M. W. Fay, G. Moldovan, P. D. Brown, I. Harrison, J. C. Birbeck, B. T. Hughes, M. J. Uren, and T. Martin, "Structural and electrical characterization of AuTiAlTi/AlGaN/GaN ohmic contacts," *Journal of Applied Physics*, vol. 92, no. 1, pp. 94–100, 2002.

[65] F. M. Mohammed, L. Wang, I. Adesisa, and E. Piner, "The role of barrier layer on ohmic performance of Ti/Al-based contact metallizations on AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 100, no. 2, p. 023708, 2006.

[66] Y. C. Lin and et al., "Nitride-based light emitting diodes with Ni/ITO p-type ohmic contacts," *Photonics Technology Letters, IEEE*, vol. 14, no. 12, pp. 1668–1670, 2002.

[67] L. Stafford, L. F. Voss, S. J. Pearton, H. T. Wang, and F. Ren, "Improved long-term thermal stability of InGaN/GaN multiple quantum well light-emitting diodes using TiB and Ir-based p-ohmic contacts," *Applied Physics Letters*, vol. 90, no. 24, p. 242103, 2007.

[68] R.-H. Horng, D.-S. Wuu, Y.-C. Lien, and W.-H. Lan, "Low-resistance and high-transparency Ni/indium tin oxide ohmic contacts to p-type gan," *Applied Physics Letters*, vol. 79, no. 18, pp. 2925–2927, 2001.

[69] R. Hong, S. Kim, D. Kim, T. Lee, J. Song, J. H. Cho, C. Sone, Y. Park, and T. Seong, "Enhancement of the light output of GaN-based ultraviolet light-emitting diodes by a one-dimensional nanopatterning process," *Applied Physics Letters*, vol. 88, no. 10, p. 103505, 2006.

[70] S. Pearton, J. C. Zolper, R. J. Shul, and F. Ren, "GaN: processing, defects, and devices," *Journal of Applied Physics*, vol. 86, no. 1, pp. 1–78, July 1999.

[71] W. Grieshaber, E. F. Schubert, I. D. Goepfert, R. F. J. Karlicek, M. J. Schurman, and C. Tran, "Competition between band gap and yellow luminescence in GaN and its relevance for optoelectronic devices," *Journal of Applied Physics 80, 4615*, 1996.

[72] J. Neugebauer and C. V. de Walle, "Gallium vacancies and the yellow luminescence in GaN," *Applied Physics Letters 69, 503*, 1996.

[73] E. F. Schubert, I. Goepfert, and J. M. Redwing, "Evidence of compensating centers as origin of yellow luminescence in GaN," *Applied Physics Letters 71, 3224*, 1997.

[74] K. Saarinen and et al., "Observation of the native Ga vacancies in GaN by positron annihilation," *Physics Review Letters 79, 3030*, 1997.

[75] R. S. Muller and T. I. K. with Mansun Chan, *Device Electronics for Integrated Circuits*, 3rd ed. Wiley, 2003.

[76] S. M. Sze, *Semiconductor Devices: Physics and Technology*, 2nd ed. John Wiley & Sons, Inc., 2001.

[77] R. Olshansky, C. B. Su, J. Manning, and W. Powazinik, "Measurement of radiative and non-radiative recombination rates in InGaAsP and AlGaAs light sources," *PIEEE Journal of Quantum Electronics QE-20 838*, 1984.

[78] G. P. Agrawal and N. K. Dutta, *Long wavelength semiconductor lasers.* John Wiley and Sons, New York, 1986.

[79] E. F. Schubert, L.-W. Tu, G. J. Zydzik, R. F. Kopf, A. Benvenuti, and M. R. Pinto, "Elimination of heterojunction band discontinuities by modulation doping," *Applied Physics Letters 60, 466*, 1992.

[80] N. Hunt, E. F. Schubert, D. L. Sivco, A. Y. Cho, and G. J. Zydzik, "Power and efficiency limits in single-mirror light-emitting diodes with enhanced intensity," *Electron. Lett. 28, 2169*, 1992.

[81] B. E. A. Saleh and M. C. Teich, *Fundamentals of Photonics*, 2nd ed. Wiley, 2007.

[82] M. Fukuda, *Optical Semiconductor Devices.* Wiley, 1999.

[83] X. A. Cao, J. M. Teetsov, M. P. Dévelyn, D. W. Merfeld, and C. H. Yan, "Electrical characteristics of AlGaN/GaN light-emitting diodes grown on GaN and sapphire substrates," *Applied Physics Letters*, vol. 85, pp. 7–9, 2004.

[84] V. Dmitriev, "GaN based p-n structures grown on SiC substrates," *MRS Internet J. Nitride Semicond. Res.*, vol. 1, pp. 29–33, 1996.

[85] P. G. Eliseev, P. Perlin, J. Furioli, P. Sartori, J. Mu, and M. Osinski, "Tunneling current and electroluminescence in AlGaN:Zn, Si/AlGaN/GaN blue light emitting diodes," *J. Electron. Mater.*, vol. 26, pp. 311–319, 1997.

[86] G. Franssen, E. Litwin-Staszewska, R. Piotrzkowski, T. Suski, and P. Perlin, "Optical and electrical properties of homoepitaxially grown multiquantum well AlGaN/GaN light emitting diodes," *Journal of Applied Physics*, vol. 94, no. 9, pp. 6122–6128, 2003.

[87] J. M. Shah, Y.-L. Li, T. Gessmann, and E. F. Schubert, "Experimental analysis and theoretical model for anomalously high ideality factors in AlGaN/GaN pn junction diodes," *Journal of Applied Physics*, vol. 94, pp. 2627–2630, August 2003.

[88] L. Hirsch and A. S. Barrière, "Electrical characterization of InGaN/GaN light emitting diodes by molecular beam epitaxy," *Journal of Applied Physics*, vol. 94, no. 8, pp. 5014–5020, 2003.

[89] X. A. Cao, E. B. Stokes, P. M. Sandvik, S. F. L. Boeuf, J. Kretchmer, and D. Walker, "Diffusion and tunneling currents in GaN/InGaN multiple quantum well light-emitting diodes," *IEEE Electron. Dev. Lett.*, vol. 23, pp. 535–537, 2002.

[90] X. A. Cao, J. A. Teetsov, F. Shahedipuor-Sandvik, and S. D. Arthur, "Microstructural origin of leakage current in GaN/AlGaN light-emitting diodes," *Journal of Crystal Growth*, vol. 264, pp. 172–177, 2004.

[91] D. S. Li, H. Chen, H. B. Yu, H. Q. Jia, Q. Huang, and J. M. Zhou, "Dependence of leakage current on dislocations in GaN-based light-emitting diodes," *Journal of Applied Physics*, vol. 96, pp. 1111–1114, 2004.

[92] A. Laubsch, M. Sabathil, J. Baur, M. Peter, and B. Hahn, "High power and high efficiency InGaN based light emitters," *IEEE Transactions on Electron Devices*, 2009.

[93] G. Meneghesso, A. Chini, A. Maschietto, E. Zanoni, P. Malberti, and M. Ciappa, "Electrostatic discharge and electrical overstress on GaN/InGaN light emitting diodes," *in Proceedings EOS/ESD Symposium*, pp. 247–252, 2001.

[94] G. Meneghesso, S. Possa, and M. Vanzi, "Investigation on ESD-stressed GaN/InGaN-on-sapphire blue LEDs," *Microelectronics Reliability 41*, pp. 1609–1614, 2001.

[95] M. Meneghini, A. Tazzoli, E. Ranzato, N. Trivellin, G. Meneghesso, and E. Zanoni, "A study of the failure of GaN-based LEDs submitted to reverse-bias stress and ESD events," *in Proceedings IRPS*, pp. 522–527, 2010.

[96] M. Meneghini, A. Tazzoli, R. Butendeich, B. Hahn, G. Meneghesso, and E. Zanoni, "Soft and hard failures in InGaN-Based LEDs submitted to electrostatic discharge testing," *IEEE Electron Device Letters*, vol. 31, no. 6, pp. 579–581, June 2010.

[97] Y. K. Su, S. J. Chang, S. C. Wei, S.-M. Chen, and W.-L. Li, "ESD engineering of nitride-based LEDs," *IEEE Transactions on Device and Material Reliability*, vol. 5, no. 2, pp. 277–281, June 2005.

[98] C.-H. Jang, J. K. Sheu, C. M. Tsai, S. C. Shei, W. C. Lai, and S. J. Chang, "Effect of the thickness of the p-AlGaN electron blocking layer on the improvement of ESD characteristics in GaN-Based LEDs," *IEEE Photonics Technology Letters*, vol. 20, no. 13, pp. 1142–1144, July 1 2008.

[99] C. M. Tsai, J. K. Sheu, P. T. Wang, W. C. Lai, S. C. Shei, S. J. Chang, C. H. Kuo, C. W. Kuo, and Y. K. Su, "High efficiency and improved ESD characteristics of GaN-Based LEDs with naturally textured surface grown by MOCVD," *IEEE Photonics Technology Letters*, vol. 18, no. 11, pp. 1213–1215, June 1 2006.

[100] S.-K. Jeon, J.-G. Lee, E.-H. Park, J. Jang, J.-G. Lim, S.-K. Kim, and J.-S. Park, "The effect of the internal capacitance of InGaN-light emitting diode on the electrostatic discharge properties," *Applied Physics Letters 94, 131106*, 2009.

[101] Lumileds, "Luxeon reliability," *Application Brief AB25, 11*, 2004.

[102] D. A. Steigerwald, J. C. Bhat, D. Collins, R. M. Fletcher, M. O. Holcomb, M. J. Ludowise, P. S. Martin, and S. L. Rudaz, "Illumination with solid state lighting technology," *IEEE J. Sel. Top. Quantum Electron. 8, 310*, 2002.

[103] J. J. Horng, Y. K. Su, S. J. Chang, W. S. Chen, and S. C. Shei, "GaN-based power LEDs with CMOS ESD protection circuits," *IEEE Transactions on Devices and Materials Reliability*, vol. 7, no. 2, pp. 340–346, June 2007.

[104] M. Meneghini, N. Trivellin, M. Pavesi, M. Manfredi, U. Zehnder, B. Hahn, G. Meneghesso, and E. Zanoni, "Leakage current and reverse-bias luminescence in InGaN-based light-emitting diodes," *Applied Physics Letters 95*, 2009.

[105] Z.-Q. Fang, D. C. Reynolds, and D. C. Look, "Changes in electrical characteristics associated with degradation of InGaN blue light-emitting diodes," *J. Electron. Mater.*, vol. 29, no. 4, pp. 448–451, April 2000.

[106] Y. D. Jho, J. S. Yahng, E. Oh, and D. S. Kim, "Field-dependent carrier decay dynamics in strained $In_xGa_{1-x}N/GaN$ quantum," *Phys. Rev. B*, vol. 66, no. 3, p. 035334, July 2002.

[107] G. A. Onushkin, S.-S. Hong, J.-H. Lee, J.-S. Park, J.-K. Son, M.-H. Kim, and Y. Park, "Local electroluminescence and time-resolved photoluminescence study of InGaN light-emitting diodes," *Appl. Phys. Lett.*, vol. 95, no. 10, pp. 101 904–1–101 904–3, September 2009.

[108] E. Calleja, F. J. Sanchez, D. Basak, M. A. Sanchez-Garcia, E. Munoz, I. Izpura, F. Calle, J. M. G. Tijero, J. L. Sanchez-Rojas, B. Beaumont, and P. Lorenzini, "Yellow luminescence and related deep states in undoped GaN," *Phys. Rev. B*, vol. 55, no. 7, pp. 4689–4694, 1997.

[109] M. Peter, A. Laubsch, W. Bergbauer, T. Meyer, M. Sabathil, J. Baur, and B. Hahn, *Phys. Status Solidi B*, vol. 206, p. 1125, 2009.

[110] R. Charash, P. P. Maaskant, L. Lewis, C. McAleese, M. J. Kappers, C. J. Humphreys, and B. Corbett, *Appl. Phys. Lett.*, vol. 95, p. 151103, 2009.

[111] C.-Y. Huang, Q. Yan, Y. Zhao, K. Fujito, D. Feezell, C. G. V. de Walle, J. S. Speck, S. P. DenBaars, and S. Nakamura, *Appl. Phys. Lett.*, vol. 99, p. 141114, 2011.

[112] A. David, M. J. Grundmann, J. F. Kaeding, N. F. Gardner, T. G. Mihopoulos, and M. R. Krames, *Appl. Phys. Lett.*, vol. 92, p. 053502, 2008.

[113] T.-S. Kim, B.-J. Ahn, Y. Dong, K.-N. Park, J.-G. Lee, Y. Moon, H.-K-Yuh, S.-C. Choi, J.-H. Lee, S.-K. Hong, and J.-H. Song, *Appl. Phys. Lett.*, vol. 100, p. 071910, 2012.

[114] I. V. Rozhansky and D. A. Zakheim, *Phys. Status Solidi A*, vol. 204, p. 227, 2007.

[115] S. Chiaria, E. Forno, M. Goano, and E. Bellotti, *IEEE Trans. Electron Devices*, vol. 57, p. 60, 2010.

[116] S. Chiaria, M. Goano, and E. Bellotti, *IEEE J. Quantum Electron.*, vol. 47, p. 661, 2011.

[117] F. Bertazzi, M. Goano, and E. Bellotti, *Appl. Phys. Lett.*, vol. 101, p. 011111, 2012.

[118] K. D. Chik and B. A. Richardson, *J. Appl. Phys.*, vol. 67, p. 2660, 1990.

[119] A. M. Armstrong, *Investigation of deep level defects in GaN:C, GaN:Mg and pseudomorphic AlGaN/GaN films*. The Ohio State University, 2006.

[120] S. K. Zhang, W. B. Wang, R. R. Alfano, A. Teke, L. He, S. Dogan, D. J. Johnstone, and H. Morkoc, "Photoionization study of deep centers in GaN/AlGaN multiple quantum wells," *J. Vac. Sci. Technol. B 28(3)*, May/June 2010.

[121] R. Passler, *Journal of Applied Physics 96, 715*, 2004.

[122] A. Armstrong, A. R. Arehart, and S. A. Ringel, "A method to determine deep level profiles in highly compensated, wide band gap semiconductors," *Journal of Applied Physics 97, 083529*, 2005.

[123] A. Armstrong, T. A. Henry, D. D. Koleske, M. H. Crawford, K. R. Westlake, and S. R. Lee, "Dependence of radiative efficiency and deep level defect incorporation on threading dislocation density for InGaN/GaN light emitting diodes," *Applied Physics Letters 101, 162102*, 2012.

[124] D. V. Lang, "Deep-level transient spectroscopy: a new method to characterize traps in semiconductors," *Journal of Applied Physics*, vol. 45, no. 7, 1974.