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# Characterization of Charge Trapping Phenomena in GaN-based HEMTs

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# Abstract

This dissertation reports on charge-trapping phenomena and related parasitic effects in AlGaN/GaN high electron mobility transistors. By means of static and pulsed I-V measurements and deep-level transient spectroscopy, the main charge-trapping mechanisms affecting the dynamic performance of GaN-based HEMTs devoted to microwave and power switching applications have been comprehensively characterized, identifying the nature and the localization of the deep-levels responsible for the electrically active trap-states.

A high-voltage measurement system capable for double-pulsed $I_D$-$V_D$, $I_D$-$V_G$ and drain-current transient spectroscopy has been successfully designed and implemented.

A characterization methodology, including the analysis of static I-V measurements, pulsed I-V measurements, and deep-level transient spectroscopy, has been developed to investigate the impact of voltage, current, and temperature on the parasitic effects of charge-trapping (threshold voltage instabilities, dynamic on-resistance increase, and transconductance reduction), and on trapping/detrapping kinetics. Experimental results gathered on transistor structures are supported by complementary capacitance deep-level transient spectroscopy (C-DLTS) performed on 2-terminal diode (FATFET) structures.

Two main case-studies have been investigated. Schottky-gated AlGaN/GaN HEMTs grown on silicon carbide substrate employing iron and/or carbon doped buffers devoted to microwave applications, and MIS-gated double-heterostructure AlGaN/GaN/AlGaN HEMTs grown on silicon substrate devoted to power switching applications. The devices under test have been exposed to the complete set of current-voltage regimes experienced during the real life operations, including off-state, semi-on-state, and on-state.

The main novel results are reported in the following:

- Identification of a charge-trapping mechanism promoted by hot-electrons. This mechanism is critical in semi-on-state, with the combination of relatively high electric-field and relatively high drain-source current.
- Identification of a positive temperature-dependent charge-trapping mechanism localized in the buffer-layer, potentially promoted by the vertical drain to substrate potential. This mechanism is critical in high drain-voltage off-state bias in high temperature operations.
- Identification of deep-levels and charge-trapping related to the presence of doping compensation agents (iron and carbon) within the GaN buffer layer.

- Identification of charge-trapping mechanism ascribed to the $SiN_X$ and/or $Al_2O_3$ insulating layers of MIS-gated HEMTs. This mechanism is promoted in the on-state with positive gate-voltage and positive gate leakage current.
- Identification of a potential charge-trapping mechanism ascribed to reverse gate leakage current in Schottky-gate HEMTs exposed to high-voltage off-state.
- The characterization of surface-traps in ungated and unpassivated devices by means of drain-current transient spectroscopy reveals a non-exponential and weakly thermally-activated detrapping behaviour.
- Preliminary synthesis of a degradation mechanism characterized by the generation of defect-states, the worsening of parasitic charge-trapping effects, and the degradation of rf performance of AlGaN/GaN HEMTs devoted to microwave operations. The evidence of this degradation mechanism is appreciable only by means of rf or pulsed I-V measurements: no apparent degradation is found by means of DC analysis.

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# 1 Introduction

Exploiting the physical properties of gallium nitride (GaN), aluminium nitride (AlN), indium nitride (InN) and related alloys (AlGaN, InGaN, InAlN, and InAlGaN), the solid-state electron devices based on III-nitrides semiconductor system will play a key role in the next generation power electronics.

Owing on the high bandgap (3.4 eV), the high breakdown electric field (3.3 MV/cm), and the high saturation velocity ($2.5 \times 10^7$ cm/s) of gallium nitride, GaN-based power amplifiers features several advantages with respect to those based on gallium arsenide (GaAs) and indium phosphide (InP): higher power density, increased bandwidth, increased efficiency, and higher operating temperature, key elements for the next-generation of *microwave* electronics devoted to wireless and satellite telecommunication systems, radars and military countermeasure systems.

In addition, since GaN can withstand higher electric field and higher temperatures than silicon, GaN-based devices can adopt highly scaled active-regions with lower on-resistance, and lower parasitic capacitance, leading to key advantages in the realm of *power switching* electronics for the development of smaller and more efficient energy conversion systems devoted to power-supply, automotive, and aerospace applications.

Thanks to the spontaneous and piezoelectric polarization charge at the AlGaN/GaN interface, and the onset of the two-dimensional high-mobility electron-gas (2DEG), the field-effect High Electron-Mobility Transistor (HEMT) is a viable architecture to implement GaN-based devices. Since the first, pioneering demonstration of a working AlGaN/GaN HEMT by Khan *et al.* in 1992, an impressive development of III-nitrides science and the technology has been promoted by worldwide distinguished universities, research institutes, and industries.

Nevertheless, in the progress towards the implementation of performant, reliable, and cost-effective high-power GaN-HEMTs, several physical and technological challenges still need to be faced and overcome. Among those, charge-trapping phenomena represent a key issue capable to degrade the static and the dynamic performance of these devices, promoting metastable threshold-voltage instabilities, transconductance droop, on-resistance increase, and the related well known current dispersion effects.

In the complex HEMT architectures, what causes charge-trapping phenomena is the combination of a sufficiently high density of deep-trap-states (also referred as deep-levels) and the presence of driving-forces promoting the capture of carriers. Deep-trap-

states can originate from native crystal defectiveness, impurities, by-products of doping processes, interfaces, electrical stress, and particles irradiation. Capture mechanisms can be exacerbated by suboptimal electric-field distribution, high hot-electron density, temperature, and parasitic leakage currents.

As a consequence, the accurate characterization of charge-trapping phenomena, the localization of the involved deep-trap states, and the identification of the related charge-trapping mechanisms represent key elements towards improved technological solutions, and dispersion-free device architectures.

The aim of this Doctoral dissertation is to discuss the methodology for a comprehensive characterization of charge-trapping phenomena, and to report on key results gathered in state-of-art GaN-based high electron mobility transistors.

Chapter 1 includes an insight on the main III-nitrides defect-states and on the Shockley-Read-Hall theory, preluded by an essay on the history of solid-state electronics reporting on the essential discoveries in the field, on the open challenges in the realm of GaN-based electronics.

In Chapter 2, we discuss two essential techniques employed for the analysis of charge-trapping phenomena, i.e., the double-pulse current-voltage measurements, and the deep-level transient spectroscopy, and we provide the guidelines for the implementation of a high-voltage pulsed measurement system.

In Chapter 3, we investigate the static and dynamic parasitic effects related to the GaN-buffer design in Schottky-gated AlGaN/GaN HEMTs grown on silicon carbide substrate and devoted to microwave applications, and we disclose an analysis of the relevant interplay between compensation strategy, pinch-off properties, and degradation mechanisms.

In Chapter 4, we present an extensive analysis of the main charge-trapping mechanisms in a MIS-gated double heterostructure AlGaN/GaN HEMT grown on silicon substrate and devoted to high power switching application, and we report on the role played by buffer-trapping, hot-electrons-related trapping, and MIS gate trapping.

Finally, in Chapter 5 we summarize novel experimental results gathered during this research program, discussing future perspective developments.

# 1.1 History of solid-state electron devices

The 20th century has been the theatre of one of the greatest scientific and technological revolution of human kind. With the establishment of quantum mechanics and quantum statistics, scientists grabbed the essence of the solid-state physics down to atomic scale, posing the basis for the technological development that fully exploited the properties of semiconductor materials towards the invention of solid-state electron devices. Kicked-off, and constantly trailed by the flourishing telecommunication industry, the development of new devices, new design paradigms, and new fabrication techniques, gave life to the modern electronics. The capabilities to acquire, transmit, elaborate, and store data at an unimaginable speed have been the backbone for the major scientific and social proceedings of our times. The capabilities to handle high power with outstanding efficiency is revolutionising the way we will transform the energy and the way we will impact on the planet. In the following, I will briefly report on the essential milestones which guided the evolution of solid-state devices from the early 20th century to date, and on the open challenges in the field of III-nitride electronics.

## 1.1.1 From cat's whiskers to P-N diodes

The first working solid-state devices in history were the cat's whisker detectors: patented in 1901 and 1906 by Bose and Pickard, they were employed in radio receivers to demodulate the AM radio signal until the birth of vacuum tubes in 1920s. During the World-War II, point-contact rectifiers had been the unique viable solution to realize microwave receivers for radar systems [1]. Based on crude, unstable point-contact between a springy piece of thin metal wire (so called cat's whisker) and a natural mineral lead sulfide crystal (galena) or silicon crystal, the cat's whisker detectors were the first devices that in fact implemented the rectifying metal-semiconductor junction. The "unilateral conduction" of metal-semiconductor junction, discovered by Braun in 1874, was successfully theorized thanks to the elements of modern solid-state physics by Schottky and Mott only in 1939 [2].

From the invention of cat's whiskers detectors, great progress was made in understanding the role played by impurities on the rectifying properties of point-contacts, the need for high-purity crystal refinement techniques, and the viable approaches to develop junction-based rectifiers. In 1940, Russel Ohl reported the onset of a parasitic energy barrier in a slab of silicon, likely ascribed to the parasitic segregation of impurities during metallurgic refinement. He accidentally discovered the P-N junction diode, the photovoltaic effect, and the role played by atoms from column III (e.g. boron and aluminium) and column V

(e.g. phosphorous and arsenic) in modifying the conductivity and the Fermi level of silicon and germanium [1].

### 1.1.2 The birth of the transistor

After the Second World War, the American electronics industry exploited the knowledge gained in the field of semiconductors devices. At the AT&T Bell Labs, William Shockley was designated head of a research group which goal was to develop a solid-state electronic device able not only to *rectify*, but also to *amplify* an electric signal, allowing to overcome the physical limits and the reliability issues of the vacuum tubes (triodes) and the electro-mechanical relays. According to preliminary studies, the adopted strategy was focused on the field-effect, which pioneering concepts had been patented in 1926, by Julius E. Lilienfeld from the University of Leipzig [3]. Several attempts were performed, both on silicon and on germanium. None of them succeeded: the problem was accurately believed to be related to the high density of surface interface-states that screened the gate electric-field, and inhibited the field-induced conductivity modulation. It was on December 1947 that John Bardeen and Walter Brattain, investigating viable solutions to the surface problem, fabricated what changed the history of electronics: the pnp germanium point-contact transistor, the first working solid-state amplifier device [4].

The working principle of point-contact transistors was not the quested field-effect, but the so-called *transistor-effect*, which fundamental action is actually played inside the body (and not at the surface) by the injection and the collection of minority carriers in two forward- and reverse-biased closely-spaced P-N junctions. Precisely and successfully theorized by W. Shockley in 1948, the transistor-effect enlighten the road for the physics-based design of the Bipolar Junction Transistor (BJT) [5]. The first BJT, labelled as “grown junction transistor”, was successfully implemented in 1950 [6], by means of the Czochralski growth technique, early developed in 1917. Nevertheless, a great issue undermined that solution: the relatively low operative frequency (around 10MHz), which arose by the minimum base width achievable by the doping process during Czochralski growth (at least 10 μm). It was by means of dopant-diffusion technique that, in 1954, transistors successfully implemented 1-μm-long diffused-base, achieving cut-off frequencies greater than 100 MHz [7]. Few years later, research works on chemical vapor deposition (CVD) allow the growth of thin layers of arbitrarily-doped single crystal silicon on silicon-substrate, leading to the further increase of operating frequency and breakdown voltage [8]. The introduction of the concept of epitaxy in the realm of solid-state electronics would be of ultimate importance for the incoming birth and development of III-V microwave devices.

Concerning the physical properties of viable semiconductor materials, silicon had a key intrinsic advantage over germanium: the higher band-gap. With $E_G$ = 1.1 eV, silicon-based transistors could sustain higher operating temperature with orders-of-magnitude lower leakage currents than germanium counterpart with $E_G$ = 0.67 eV. Despite a more difficult fabrication procedure, due to higher melting temperature (1415°C vs 937°C) and the higher chemical reactivity, the first silicon grown junction transistor was successfully implemented in 1954 by Teal at Texas Instruments [9]. The key process to obtain silicon crystals of purity comparable to the best obtained in germanium was the floating-zone refinement, presented in 1953 by H. C. Theurer [10].

It was only in 1960 that, investigating viable solutions to passivate the surface of silicon-based BJTs from the interaction with environmental humidity, M. M. Atalla and D. Kahng discovered that the presence of a layer of silicon oxide could effectively suppress the surface-states. As a by-product, the presence of the $SiO_2$ layer and the passivation of surface-states, finally allows to observe the field-effect, which was then able to penetrate within the bulk of silicon, modulating its conductivity [11]. Thanks to the outstanding natural properties of $Si/SiO_2$ interface, and the related advantages in manufacturing planar devices and monolithic architectures, the silicon-based MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) would soon became the hearth of integrated circuit[1], of the subsequent Very Large Scale Integration, and of the digital revolution of following decades.

Adhering to Moore's law, the birth and the evolution of microprocessors, microcontrollers, analog/digital converters, and volatile and non-volatile memories has revolutionized the humankind from the high-end scientific scopes, to the everyday social life.

### 1.1.3 III-arsenides electronics

Besides the aggressive scaling of transistor dimension and their application in highly integrated digital electronic systems, the field of solid-state electronics faced the emerging need for microwave (RF) devices. Firstly employed only in high-end scientific, military, and aerospace applications, the RF solid-state devices became eventually the backbone of the wireless communication systems, (e.g., satellite and cell phone) since 1980s. The demand for high operative frequencies (much greater than 1 GHz), high power gain, high stability, and low noise figure, driven physicists and electronics engineers towards an alternative, attractive semiconductor: the III-V gallium-arsenide compound—

[1] Invented in 1958 by Kilby at Texas Instruments and Noyce at Fairchild.

which features higher electron mobility (8500 vs 1500 $cm^2/Vs$) and higher overshoot electron velocity than silicon.

Thanks to direct band-gap, gallium-arsenide (GaAs) was originally employed in infrared Light Emitting Diodes (LEDs) since early 1960s. The first architecture able to effectively implement a GaAs transistor was eventually the Metal-Semiconductor Field-Effect Transistor (MESFET). Reported for the first time in 1966 by C. A. Mead [12], GaAs MESFET would be able to overtake silicon-based rf BJTs in terms of operative frequencies and noise figure: in 1980, the state-of-art Si BJT featured an $f_{max}$ of 35 GHz, whereas the GaAs MESFET counterpart exhibits a $f_{max}$ of 100 GHz [13].

In the late 1970s, the fabrication of MOSFET devices based on GaAs technology was extensively investigated. Unfortunately, any successful result was gathered. The main obstacle towards the realization of a GaAs MOSFETs was the overwhelming difficulties to growth the GaAs-oxide with sufficiently low interface state density. Again, as in the pioneering research works of the 1940s, unacceptably high interface-states density impeded and delayed for decades the effective implementation of a theorized field-effect device.

In the meanwhile, the concept of heterostructure and doping modulation was approached and investigated by R. Dingle and co-workers at the Bell Labs [14]. Relying on different energy-gap, but similar lattice-constant, gallium-arsenide (GaAs), aluminium-arsenide (AlAs), and their ternary alloys ($Al_xGa_{1-x}As$) can be effectively combined in the same (super)lattice structure, exploiting simultaneously the outstanding carrier confinement provided by the band-gap discontinuities, and the outstanding carrier-mobility ensured by the absence of coulomb-scattering in undoped layers. What made possible the research and the development of AlGaAs/GaAs heterostructures was the advent of the Molecular Beam Epitaxy (MBE). Presented in 1968 by J. R. Arthur Jr *et al.*, the MBE allows the growth of arbitrarily doped atomic monolayers, which allowed a control of epitaxial thickness and doping without precedent [15]. The bandgap engineering, the quantum carrier confinement, and possibility to design and implement two-dimensional high-mobility free-electron gas (2DEG) would soon became an extremely powerful tool in the hand of the device developers, permitting the realization of extremely high frequencies and low noise solid-state amplifiers.

It was in 1979, at the Fujitsu laboratories, that Takashi Mimura designed and realized the first working prototype of High Electron Mobility Transistor (HEMT) based on the AlGaAs/GaAs heterostructure [16]. The architecture of HEMT consisted of a few nm thick Si-doped $Al_XGa_{(1-X)}As$ barrier layer grown on top of an undoped GaAs buffer layer. The bi-dimensional high mobility electron gas (2DEG), formed at the AlGaAs/GaAs

interface, was effectively modulated by the field-effect provided by a Schottky gate contact. High electron mobility transistors, firstly employed as cryogenic Low-Noise Amplifiers (LNAs) in radio-astronomy applications, would soon became key devices both in scientific equipment, e.g. those devoted to microwave imaging, and in civil, mass-market wireless telecommunication systems, including satellite communication, cellular systems, cell-phones, and broad-band satellite television.

Since their invention, conventional GaAs-based HEMTs experienced key innovations that led to impressive improvements of their rf performances. In 1985, indium and related InGaAs and InAlAs alloys came into play. Featuring lower band-gap and even higher electron mobility than GaAs, InGaAs had been employed as channel layer in the novel double-heterostructure (AlGaAs/InGaAs/GaAs) *pseudomorphic*-HEMT [17]. The term pseudomorphic refers from the fact that InGaAs has different lattice constant than AlGaAs and GaAs, thus imposing severe constrains, including alloy compositions and critical thicknesses, on the design of the strained pHEMT heterostructure. It was with the introduction of very expensive indium-phosphide (InP) substrate with higher lattice-constant than GaAs (5.87 A vs 5.65 A) that pHEMTs could implement very aggressive alloy compositions (e.g., $In_{0.35}AlAs/In_{0.65}GaAs/In_{0.35}AlAs$), resulting in highly confined 2DEG, electron mobility of ~15000 $cm^2/Vs$, a sheet concentration of ~$4x10^{12}$ $cm^{-2}$, and outstanding maximum frequency of ~600 GHz [13]. In addition to the pHEMT, a compromise to obtain InP-free, low-cost devices, arose in the 1990s with the concept of *metamorphic*-HEMT, where a thick, relaxed InAlAs buffer layer was introduced to accommodate the lattice mismatch between the low-cost GaAs substrate and the InAlAs/InGaAs active region.

The constant increase of the operative frequencies is of course intimately related to the scaling of device geometry, including in particular the gate length and, for the sake of the aspect ratio, the barrier thickness. Key enabling technologies were the adoption of delta-doping [18], in which all the required dopant is concentrated in few monolayers at an engineered distance from the 2DEG within the (back)barrier, and the gate recess, employed to lower the barrier thickness. In Schottky-gate HEMTs, the physical limit of the gate-to-channel distance is 4 nm, and it was approached in the 2000s in devices with $L_G$ = 50 nm [19]. What impedes to further shrink the barrier thickness below ~4 nm is the exponential increase of the gate leakage current, which dramatically compromise the on/off current ratio. The solution would be the introduction of a thin layer of wide-bandgap material, such as an oxide, between the gate and the barrier. In 2003, around 30 years after the first, unsuccessful experiments on III-V MOSFETs, P. D. Ye *et al.* reported the growth of $Al_2O_3$ oxide layer on top of GaAs by means of *ex-situ* Atomic Layer Deposition (ALD) [20]. The acceptable interface-states density (~$10^{12}$ $cm^{-2}eV^{-1}$)

permitted the unpinning of the Fermi-Level and the proper field-effect channel modulation. Since then, the highly scalability of MOS architecture, joined with the outstanding electron mobility and injection velocity of InGaAs, make the III-V semiconductor a promising candidate not only for cutting-edge microwave applications, but also for replacing silicon in the non-planar ballistic channel n-logic transistors with $L_G < 14$ nm [21] [22].

With the given differences, the experience gathered since 1980 during the evolution of GaAs-based HEMTs would became of pivotal importance in the development of GaN-based electronics triggered almost 20 years later.

### 1.1.4 III-nitrides electronics

As happened for gallium arsenide, it was in the realm of the optoelectronics that researchers approached gallium nitride, thanks to its direct band-gap, in the late 1960s. Though light within infrared to green wavelengths could be generated with GaAs, GaAsP, and GaP:N, gallium nitride was a good candidate for covering the blue, violet and UV spectrum.

The synthesis of GaN, through the reaction of gallium and ammonia, was demonstrated for the first time by W. C. Johnson *et al.* in 1932 [23]. But it was only in 1969, that H. P. Maruska and J. J. Tietjen succeeded in the epitaxial deposition of an n-type GaN single crystal on sapphire substrate [24] by means of Halide Vapor Phase Epitaxy (HVPE) at a growth temperature of 950°C. Three years later, with the help of J. Pankove, Maruska realized the first blue and violet GaN-based MIS LED with the adoption of zinc and magnesium as colour centres [25]. But it was only in 1991, almost 20 years later, that Nakamura *et al.* developed the first p-n junction GaN LED thanks to the discovery of the hydrogen passivation of p-type magnesium dopant, and the subsequent introduction of a post-growth $N_2$ thermal annealing, necessary for the activation of the magnesium doping [26].

In the meanwhile, scientists and engineers developed alternative, more effective GaN growth techniques, adopting the MBE (in 1983), and the MOCVD (in 1986), which would play an essential role for the incoming evolution of GaN-based transistors. It was in 1992, that M. Asif Khan *et al.* observed for the first time the onset of a two-dimensional electron gas in low pressure MOCVD AlGaN/GaN heterojunction, paving the way for the subsequent successful implementation of the AlGaN/GaN high electron mobility transistor [27]. Precisely theorized by Bykhovski *et al.* in 1993, the formation of the 2DEG at the AlGaN/GaN interface is promoted by the presence of a net polarization

charge originating from both the spontaneous polar nature of III-nitrides, and the piezoelectric effect caused by strained AlGaN/GaN heterostructure [28].

Due to the physical advantages of the III-nitrides over silicon and GaAs semiconductors, including lower intrinsic carrier concentration, higher maximum breakdown field, higher electron saturation velocity, and higher thermal conductivity [29] [30], GaN-based HEMTs have represented excellent candidates for smaller, faster, and more efficient power amplifiers and power switches devoted not only to microwave (e.g., wireless infrastructure, base stations, military, aerospace, and satellite communication systems [31]), but also to power switching applications (e.g., power supply, automotive, and energy converters for both high-end and mass-market applications [32]).

#### 1.1.4.1 Substrates for GaN-based electronics

The development of mature, performant and reliable GaN HEMTs have faced several technological challenges; the first of those was represented by the substrate. Though the high-quality silicon, GaAs, and InP substrates can be fabricated at low cost with conventional melt growth methods, the growth of GaN substrate from melt is impracticable since it would require high temperature (~2225°C) and extremely high pressure (> $10^4$ atm) to avoid the decomposition of GaN at the melting point [33]. For this reason, the viable solution to fabricate GaN-based electronics was the adoption of metamorphic epitaxies on foreign substrates. The first GaN HEMT prototypes in the early 1990s were in fact grown on *sapphire* substrates ($\alpha$-$Al_2O_3$). Nevertheless, though highly available, chemically stable, and cost-effective, sapphire has a relatively high lattice mismatch with GaN (16%) which lead to relatively high epitaxial dislocation density ($10^{10}$ $cm^{-2}$), and a poor thermal conductivity (42 $Wm^{-1}K^{-1}$), which make it unsuitable for high temperature high power applications.

It was in 1997 that *silicon-carbide* (SiC), an alternative high-quality material, was successfully employed for the first time by S.C. Binari [34]. Despite the high cost (to date ~$3000 for a 4-inch wafer), due to outstanding thermal conductivity (~400 $Wm^{-1}K^{-1}$), relatively good lattice mismatch (3.5%), and typical epitaxial dislocation density of ~$10^8$ $cm^{-2}$, the semi-insulating SiC substrates still represent the optimal solution for the state-of-art GaN-based HEMT devoted to high-end power microwave electronics.

The compromise between cost, availability, and thermal conductivity is represented by *silicon*. Adopted for the first time in 2000 by S. Kaiser [35], silicon substrates feature outstanding availability, low cost, large diameters (up to 8 inch), excellent surface morphology, and relatively good thermal conductivity (148 $Wm^{-1}K^{-1}$). Silicon substrates represent the optimal solution for large-periphery power switching devices and for the

prospective integration of the GaN-electronics in the CMOS technology and related fabrication facilities [36]. The drawbacks of silicon are the narrow bandgap (1.1 eV), the relatively high GaN lattice mismatch (17%), the relatively high epitaxial dislocation density (~$10^9$ $cm^{-2}$), and the high GaN thermal expansion mismatch (54%) which are key challenges towards the realization of highly insulating buffer layers, essential for high-voltage operations.

Back to *free-standing GaN* substrates, it was in the late 1990s that alternative fabrication techniques have been explored. They include the Hydride Vapor Phase Epitaxy (HVPE), which allows to obtain GaN substrate after an high-rate growth on suitable foreign material (e.g., GaAs) and the subsequent delamination [37], or the *ammonothermal* growth, which is a solvothermal process that allows the solubilisation of polycrystalline GaN nutrient and their recrystallization on seed crystals in supercritical ammonia [38]. Though still highly expensive and small sized (2/3 inch), GaN substrates would be the key feature of the next generation of III-nitrides electronics and optoelectronics, enabling the possibility to develop polar, semi-polar and non-polar, low dislocation density (< $10^5$ $cm^{-2}$) homoepitaxial architectures, essential not only for highly efficient and reliable LEDs and LASERs, but also for vertical power transistors [39].

#### 1.1.4.2 Key technological achievements in GaN-based electronics

The epitaxial growth of high quality, crack-free III-Nitride layers with low dislocation density and smooth surface is hard to achieve because of the large lattice mismatch and large difference in thermal expansion coefficient with the foreign substrate. It was in 1983 and 1986 that Yoshida *et al.* [40] and Amano *et al.* [41] reported on the viable approach and the successful growth protocols that would allow the subsequent development of III-Nitride electronics not only on sapphire, but also in SiC and Si substrates: the introduction of a thin amorphous AlN buffer layer between the substrate and the single crystal GaN epitaxy.

Further improvements, especially in the case of GaN on silicon, were obtained with the introduction of AlN/GaN superlattice buffer structure [42]. In fact, even with the presence of AlN nucleation layer, the large lattice mismatch and the concerning difference in thermal expansion coefficient between GaN and silicon lead to parasitic tensile strain during the epitaxial growth, and during the cooling down of the sample. This leads to detrimental wafer bowing and to the formation of cracks when the thickness of the deposited layer exceeds a critical value, usually in the order of 1.4 μm to 3 μm [42]. It has been thanks to the introduction of a repeated sequence of few nm thick AlN and GaN layers that an additional compressive strain is created within the epitaxial structure [43],

counterbalancing the parasitic tensile strain caused by foreign substrate and increasing the critical thickness for crack-free GaN epitaxy. The adoption of Al/GaN superlattice buffer enabled the implementation of thicker GaN epitaxy, boosting the vertical breakdown of GaN-on-Si electron devices. A total GaN thickness of 9 μm and breakdown voltage of 1813 V has been recently reported by T. Egawa in [44].

What has been of great importance towards the improvement of electrical performance of GaN-based electronics is the control of parasitic unintentional doping of the (Al)GaN epilayers. Residual impurities originating from the growth environment and/or from the substrate, in fact, may lead to the spontaneous n-type doping and to the related undesired n-type conductivity of GaN epitaxy. This provide additional un-gated current paths, compromising the ideal subthreshold behavior, with the onset of buffer-related leakage current and early source-to-drain lateral breakdown. Viable solutions were found in the adoption of doping compensating agents: in the early 2000s, excellent results on the resistivity control in unintentionally doped GaN films were demonstrated both by means of iron [45] and carbon [46]. Further discussion on doping compensation, which is of great importance on charge-trapping phenomena, will be provided in section 1.2.1 and Chapter 3.

Besides doping compensation, other effective solutions to improve the carrier confinement in the GaN channel are the adoption of the AlGaN back-barrier layer, which provide electrostatic confinement due to higher bandgap, or the adoption of a thin InGaN layer between the GaN channel and the GaN buffer that, owing to the opposite piezoelectric polarization field in the InGaN layer, generates an additional potential barrier between the channel and the buffer [47].

Indium nitride and related alloys play a role not only for the buffer carrier confinement (InGaN back-barrier), but also for enhanced 2DEG density (InAlN and InAlGaN barrier). As successfully predicted by J. Kuzmik in 2001 [48], due to higher energy gap and higher spontaneous polarization charge, the lattice-matched heterostructure $In_{0.17}AlN/GaN$ features superior performance in terms of 2DEG and related drain current density with respect to conventional AlGaN/GaN architectures. The quaternary alloys InAlGaN are also the object of extensive research due to their better miscibility, hence higher growth quality growth than the ternary InAlN [49].

Furthermore, groundbreaking research in the realm of GaN-based microwave electronics is currently focused on the *N-polar* GaN epitaxy and N-polar GaN-based HEMTs [50]. In fact, due to the absence of inversion symmetry in wurtzite III-nitrides, the polarization charge of N-polar crystal is opposite to that of the Ga-polar crystals, causing the formation of 2DEG channels above instead of below the wide-bandgap barriers (e.g. AlGaN). It is

by exploiting this property that N-polar GaN HEMTs can be designed with the inverted double heterostructure GaN-channel/AlGaN-barrier/GaN-buffer. Since the GaN channel is directly exposed to the gate-contact and to the source- and drain-ohmic-contacts, these devices can attain extremely high gate-to-channel capacitance and extremely low ohmic contact resistance without compromising the 2DEG carrier concentration (determined by the barrier layer buried below the channel). Despite the high complexity of N-polar GaN epitaxial growth [51], N-polar HEMTs can achieve the aggressive scaling of the transistor dimensions, and the dramatic improvement of power gain and frequency performances towards W-band operations.

Finally, focusing the discussion on the high-power switching GaN-based electronics, the advent of affordable GaN bulk substrate and of highly performant MOS structures is enabling key elements for the development of novel and more efficient vertical devices. Reported in 2002 by Ben-Yaacov *et al.* [52], the AlGaN/GaN current aperture vertical electron transistor (CAVET) has been the first prototype of GaN-based vertical device. Though they are still in an explorative research phase, CAVETs enlighten the way towards the vertical topologies and novel design paradigms that could potentially exploit the full potential of the homoepitaxy on GaN bulk substrates.

#### 1.1.4.3 Gate technologies for GaN-based HEMTs

Playing a paramount role on device performances, the gate module has been and will be the key object of extensive research efforts. Exploiting the experience gathered on III-arsenides, the first employed gate technology has been the metal-semiconductor Schottky junction, implemented since the pioneering demonstration of the AlGaN/GaN HEMT in 1993.

Nevertheless, as already mentioned in the previous section, the intrinsic nature of Schottky junction have led to two pivotal limitations: the intrinsic onset of the forward-bias current, and the parasitic reverse-bias leakage current, which undermine not only the successful development of very high frequency highly scaled GaN-based amplifiers (which require very small gate-to-channel distance with sufficiently low leakage-current) but also the successful implementation of normally-off high-power GaN-based switches (which require positive threshold voltage, large positive gate-voltage swing, and high breakdown robustness).

It is the insulated-gate technology that, as happened for silicon-based and GaAs-based electronics, represents a viable solution to replace the Schottky-gate in field-effect transistors. The outstanding capabilities of modern deposition techniques, among those, the *ex-situ* atomic layer deposition (ALD), the plasma-enhanced ALD (PEALD), the

plasma enhanced chemical vapour deposition (PECVD), and the *in-situ* metalorganic chemical vapour deposition (MOCVD), and the outstanding spectrum of possible insulating materials, including not only the conventional $SiO_2$, $SiN_X$, $HfO_2$, $Al_2O_3$, but also the more explorative $Ga_2O_3$, $ZrO_2$, $TiO_2$, $Sc_2O_3$, MgO, $La_2O_3$, $Gd_2O_3$, ZnO, $Ta_2O_5$ and $Pr_2O_3$, define the extremely vast boundaries for the exciting quest towards the optimal MOS technology, with low-interface-states, low oxide-traps, high breakdown field, and good long-term reliability [53] [54] [55] [56] [57]. The successful development of performant and reliable MOS gates will pave the way not only towards the implementation of planar gate structures, but also recessed-gate and tri-gate structures [58], which are viable solutions to achieve positive threshold voltages and normally-off GaN-based devices.

Concluding the discussion on gate technologies, the possibility to adopt a p-type (Al)GaN layer in between the gate-metal and the AlGaN/GaN active region worth to be reported. Representing another interesting approach towards the implementation of normally-off devices, the p-AlGaN gate led to the conception of Gate Injection Transistors (GITs) reported for the first time by Uemoto *et al.* in 2007 [59].

The technological capabilities developed in the last decades generated outstanding opportunities for the design and the development of the next generation solid-state electronics. In this scenario, the scientific contribution provided by the exhaustive structural and electrical device characterization will play a key role towards the understanding the limits and the pitfalls of each technological solution, such as, the material defectiveness, the deep-levels and the charge-trapping phenomena.

## 1.2 Defect-states

Defect-states are the deviation in the crystalline structure from the perfect periodic arrangement of atoms in the ideal lattice. They play an essential role in solid-state electronics, since they can heavily affects the physical properties of employed semiconductors, partially or entirely compromising the performances of implemented devices. As reported in previous section, overwhelming parasitic interface-states have delayed of many years the demonstration of the first field-effect transistor (patented in 1925, demonstrated in 1952), and GaAs-based MOSFET (successfully demonstrated only in 2003). For these reasons, the analysis and the control of defect-states represent an essential part of the modern electronics.

Defect-states can be categorized in point-defects (vacancies, interstitials and antisites), extended defects (screw, edge, and mixed dislocations), foreign impurities, and interface-states. Their concentration is strictly influenced by the nature of involved elements and by the complex chemical and thermodynamic conditions existing during crystal growth; their impact on the device operations is related to their electrical properties and to their locations within the device structure. From the electrical point-of-view, their major effect is the introduction of allowed energy-levels within the forbidden energy-gap. Depending on their position within the gap, they can be categorized in *shallow-levels*, mainly responsible for parasitic doping effects, and *deep-levels*, mainly responsible for charge-trapping and/or non-radiative recombination effects (Figure 1-1). Approaching the discussion to III-Nitride semiconductor systems, a brief overview of typical defect-states in III-Nitrides crystals will be reported in the following. Then, the physics of charge (de)trapping mechanisms, based on the classic Shockley-Read-Hall theory (SRH) will be presented.

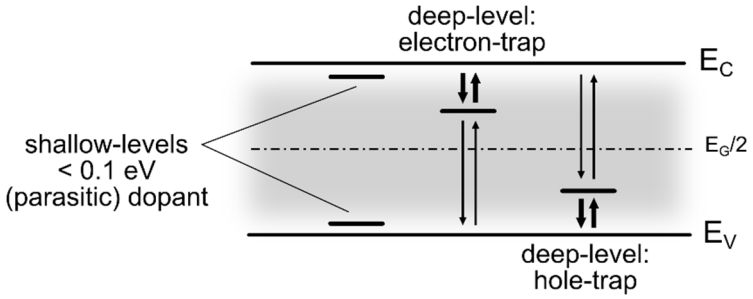



Figure 1-1 Depending on their position within the gap, defect-states and impurities can be categorized in *shallow-levels*, mainly responsible for parasitic doping effects, and *deep-levels*, mainly responsible for charge-trapping and/or non-radiative recombination effects. If deep-levels are localized in the upper-half of the energy-gap, they will experience higher probability to capture and emit electrons from and to the conduction-band, thus behaving as electron-traps. Complementarily, if they are localized in the lower-half of the energy-gap, they will more likely behave as hole-traps.

### 1.2.1 Defects and impurities in III-nitrides

The thermodynamics of defects-formation in GaN, AlN and related alloy (AlGaN) has been comprehensively investigated by means of first-principles calculations based on the state-of-art density-functional-analysis (DFT). In the following, I am reporting the essential results gathered from state-of-art literature, concerning the formation energies at the thermodynamic equilibrium, the charge-states, and the transition-levels of the main defects in III-Nitride semiconductors.

- Among the native point-defects, only **vacancies** ($V_{Ga}$ and $V_N$) have sufficiently low formation energies to play a dominant role during the growth of GaN crystals. Contrarily to GaAs systems, **antisites** ($N_{Ga}$ and $Ga_N$) and **interstitials** ($N_i$ and $Ga_i$) are highly improbable due to high formation energies (likely due to high mismatch in the covalent radii of Nitrogen and Gallium). Nevertheless, interstitials and substitutionals can be created during non-equilibrium conditions, e.g., electron irradiation or ion implantation [60].
- **Gallium vacancy** ($V_{Ga}$) has the lowest formation energy in n-type GaN, where it behave like triple acceptor. Its transition levels, comprised between $E_V + 0.25$ eV and $E_V + 1.1$ eV, are often indicted for the yellow luminescence [61]. Gallium vacancy is likely involved in complexes with hydrogen and nitrogen vacancy, with even lower formation energies [62]. Puzyrev *et al.* address the dehydrogenation of gallium vacancy as one of the causes of hot-electrons degradation mechanisms [63].
- Diverging predictions have been made on **nitrogen vacancy** ($V_N$). Van de Walle *et al.* reported that $V_N$ in GaN behaves as shallow-donors, and that it cannot be indicted as the major cause for unintentionally n-type doping since in n-type GaN they have relatively high formation energy [60]. On the other hand, Laalsonen *et al.* proposed that $V_N$ may introduce in GaN crystals two additional deep-levels at $E_C - 1.3$ eV and $E_C - 0.5$ eV, respectively [64].
- As predicted by Wright *et al.* [65] and Leung *et al.* [66], **dislocations**, including full core, open core, Ga vacancy and N vacancy core structures, feature a broad set of deep-levels within the forbidden energy gap, with a broad set of charge occupancy state. The Ga vacancy core structure, with the lowest formation energy in n-type GaN grown in N-rich environment, introduces five multiple deep-levels in the lower-half of the band-gap with occupancy state ranging from +2 to -3. The full core, most stable in p-type N-rich GaN, feature two deep-levels in the upper-half of the bandgap with (0/-1) and (-1/-2) transitions at EV+2.78 and EV+2.57 eV, respectively. The N-vacancy core structure, with lowest formation energy in Ga-rich conditions a part from n-type materials, introduces two deep-levels close

to mid-gap and one deep-level close to the conduction-band. Finally, the open core, more stable in n-type Ga-rich GaN, features 5 deep-levels distributed within the entire band-gap with occupancy state ranging from +2 to -3. Thanks to capture kinetics studies, the experimental evidence of electrically active deep-trap-states associated to dislocations have been reported by multiple research group [67] [68].

- **Silicon** in gallium substitutional ($Si_{Ga}$) behaves as shallow donor. It is energetically very stable (with the lowest formation energy among possible shallow donors), and it is usually employed as intentional n-type doping [60].
- **Oxygen** in nitrogen substitutional ($O_N$) behave as shallow donor, and it is believed to be one of the main causes of unintentially n-type doping. Furthermore, experimental evidence reveal that oxygen in GaN undergoes a DX transition (from shallow to deep-donor, featuring large lattice relaxation) when high hydrostatic pressures are applied or when $Al_XGa_{(1-X)}N$ alloys with $x > 0.3$ are present [69] [70].
- **Hydrogen**, which can be highly present in GaN grown by MOCVD and HVPE, is an amphoteric specie. In p-type GaN, it has low formation energy, it behave as (unintentional) donor (H+) compensating acceptors (see complexes with $V_{Ga}$ and $N_{Ga}$ [62], and Mg-H and C-H [71]), and it has relatively high diffusivity (0.7 eV). In n-type GaN, it behave as an acceptor (H-) with very low diffusivity. The transition (+/-) happens at $E_V + 2.4$ eV [72] [60].
- **Carbon** in GaN and AlN is amphoteric in nature. Depending on Fermi-level, carbon atoms can be incorporated either gallium or nitrogen substitutionals, featuring self-compensation properties. Carbon in gallium substitutional ($C_{Ga}$) behaves as shallow donor but has lower formation energy in p-type GaN. Conversely, carbon in nitrogen substitutional ($C_N$) behave as deep-acceptor but has lower formation energy in n-type GaN. Due to deep-acceptor behaviour and/or due to self-compensation properties, carbon doping is commonly employed to achieve highly insulating GaN. The (+/0) and (0/-) transition levels of $C_N$ are located at $E_V$+0.35 eV and $E_V$+0.9 eV, and are commonly indicted for Blue and Yelow Luminescence, respectively. $C_N$ in GaN exhibits AX-like behaviour. Among carbon interstitials ($C_i$), the split-interstitial configuration is the most probable, and it would introduce three deep-trap-states in the upper-part of the band-gap (towards the conduction-band). Nevertheless, at thermodynamic equilibrium, $C_i$ has sufficiently low formation energy only in p-type GaN grown under Ga-rich conditions. In Aluminium Nitride, $C_{Al}$ experience (+/0) and (0/-) transition levels at $E_C$-1.82 eV and $E_C$-1.68 eV, featuring DX-like configuration [73] [71].

- **Iron** is commonly adopted as compensating specie to achieve semi-insulating GaN. Comprehensive works on photoluminescence excitation spectroscopy (PLE) report that the acceptor-like (0/-) transition level of iron in GaN could be located at $E_V$+2.5 eV [74] or $E_C$-0.34 eV [75].
- **Fluorine** is extensive employed in GaN HEMT technology, both in the fabrication of the gate structure (e.g., as etching agent in plasma-enhanced anisotropic dry etching process) and in band-engineering required to achieve normally-off devices (as deep-acceptor implanted in the AlGaN barrier). According to first-principle calculation and experimental results, Fluorine can be incorporated either in negatively-charged interstitial position ($F_i^-$) or in positively-charged nitrogen substitutional position ($F_N^{2+}$) [76] [77]. The critical stability of crystallographic configuration of Fluorine atoms in (Al)GaN plays an essential role in the net fixed charge which strongly affects the threshold voltage of device.

Finally, focusing this discussion on the perspective implementation of MOS gate structure, I am reporting the essential results gathered from state-of-art literature, concerning the defect-states of silicon nitride ($Si_3N_4$) and aluminum oxide ($Al_2O_3$), two among the main dielectric materials employed as gate insulating layers so far.

- DFT calculation of **β-$Si_3N_4$** crystal structure have been reported by Vianello *et al.* in the framework of SiN-based nonvolatile memories (NVM) [78]. The hydrogen impurities in nitrogen substitutional position (1Si-H) and the silicon dangling bonds (Si dB) are the most thermodynamically stable in standard and Si-rich SiN, respectively. Both defects introduce a deep-trap-state around 1.2 eV below the conduction-band, essential to achieve the quested (in the case of solid-state memory) or parasitic (in the case of MIS-HEMTs) memory effect.
- Due to relatively high band-gap (6.5-9.0 eV), **$Al_2O_3$** is characterized by a broad set of deep-levels with a broad set of possible implications on electrical properties of MOS structures. Thanks to first-principles hybrid functional calculations, Choi *et al.* [79] [80] predicted that the aluminium vacancy ($V_{Al}$), featuring lowest formation energy in O-rich $Al_2O_3$, introduces three negatively charged acceptor-like states close to the valence-band. Similarly, aluminium interstitial ($Al_i$), more stable in p-type Al-rich materials, introduces two positively charged donor-like states close to the conduction band. $V_{Al}$ and $Al_i$ might be responsible respectively for negative and positive fixed charge at the $Al_2O_3$/(Al)GaN interface. On the other hand, aluminum dangling bonds (Al dB) and carbon impurities in aluminum position ($C_{Al}$) introduce deep-levels in the upper half of the energy gap, potentially aligned with the GaN conduction-band. These levels, which can exchange free

carriers with GaN conduction-band may be responsible for enhanced trap-assisted transport mechanisms, parasitic leakage current, and parasitic metastable charge-trapping phenomena.

### 1.2.2 Shockley-Read-Hall Theory

Theorized in 1952, the Shockley-Read-Hall theory describe the interactions between the free-carriers (electrons and holes) and the deep-levels within the forbidden energy-gap [81]. It is successfully employed to study the dynamics and the kinetics of charge-trapping and carrier generation/recombination mechanisms. In this theory, the occupancy-state of a defined deep-level and the interaction with the conduction- and valence-bands are regulated by the probability of capturing or emitting free-carriers. To grasp the completeness of this theory, and to appreciate its implication on a large variety of possible scenarios, I warmly recommend the reading of [81] [82] [83] [84].

In the following, to approach the discussion to charge-trapping and current collapse effects, we will focus on the representative case-study of electron-traps located in the upper half of the band gap, analyzing the electron capture- and emission probabilities, and deriving the kinetics of charge trapping and detrapping mechanisms. By mirroring the terminology, and employing the hole-related physical parameters, the following discussion can be fully adopted to analyze the hole-trap case.

The electron capture probability is defined as follow:

$$c_n = \sigma_n \langle v_n \rangle n \tag{1}$$

where $\sigma_n$, $\langle v_n \rangle$ and $n$ are the capture cross-section of the involved deep-level, the thermal velocity of electrons, and the free-electron concentration, respectively. By expressing $\sigma_n$ and $n$ in equation (1), we obtain:

$$c_n = \sigma_\infty Exp\left(-\frac{\Delta E_\sigma}{k\,T}\right) \langle v_n \rangle N_C Exp\left(-\frac{E_C - E_{F,n}}{k\,T}\right) \tag{2}$$

Where $\Delta E_\sigma$ is the activation energy of the capture cross-section, $N_C$ is the effective density of state in the conduction-band, $k$ is the Boltzmann constant in $eV \cdot K^{-1}$, $T$ is the temperature, and $(E_C - E_{F,n})$ is the relative position of the electrons quasi-Fermi level with respect to the conduction-band.

The electron thermal velocity $\langle v_n \rangle$ and the conduction-band effective density of state $N_C$ can be expressed as

$$\langle v_n \rangle = \left(\frac{3kT}{m^*}\right)^{1/2} \tag{3}$$

$$N_C = 2M_C\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2} \tag{4}$$

where $m^*$ is the electron effective-mass, $h$ is the Planck constant, and $M_C$ is the number of conduction band minima.

The occupancy ratio of a deep-level in thermal equilibrium responds to the Fermi-Dirac distribution

$$\frac{N_{Filled}}{N_{TOT}} = \frac{1}{1 + \frac{g_0}{g_1} exp\left(\frac{E_T - E_F}{kT}\right)} \tag{5}$$

Where $N_{TOT}$ is the total concentration of traps (expressed in $cm^{-3}$), $N_{Filled}$ is the concentration of filled traps, $g_0/g_1$ is the degeneracy ratio, and $E_T$ is the trap energy-level. Assuming negligible the hole-capture and hole-emission probabilities, the occupancy ratio can also be expressed by the balance of electron-capture and electron-emission probabilities:

$$\frac{N_{Filled}}{N_{TOT}} = \frac{c_n}{c_n + e_n} \tag{6}$$

By combining equations (5) and (6), the relationship between capture and emission of electrons results as follow:

$$\frac{e_n}{c_n} = \frac{g_0}{g_1} exp\left(\frac{E_T - E_F}{kT}\right) \tag{7}$$

which lead to the equation for the emission probability:

$$e_n = \sigma_n \langle v_n \rangle \frac{g_0}{g_1} N_C \, exp\left(-\frac{E_C - E_T}{kT}\right) \tag{8}$$

By rearranging equations (3) and (4) into equation (8), we obtain the classic form of the emission probability, used in deep-level transient spectroscopy to quantify the apparent activation energy $E_{na}$ and the apparent capture cross-section $\sigma_{na}$ of the observed deep-level:

$$e_n = \gamma T^2 \sigma_{na} \, exp\left(-\frac{E_{na}}{kT}\right) \tag{9}$$

where

$$\gamma = 2\sqrt{3} M_C (2\pi)^{3/2} k^2 m^* h^{-3} \tag{10}$$

In order to interpret the time-resolved drain-current transient spectroscopy (which methodology is extensively reported in Chapter 2), the kinetics of charge-trapping and detrapping mechanisms is discussed in the following.

Assuming an electron-trap $E_T$ with concentration $N_{TOT}$, the time-dependence of filled traps $N_{Filled}$ is governed by the following rate equation:

$$\frac{\partial N_{Filled}}{\partial t} = c_n(N_{TOT} - N_{Filled}) - e_n N_{Filled} \quad (11)$$

where $c_n(N_{TOT} - N_{Filled})$ is defined as capture-rate and $e_n N_{Filled}$ is defined as emission-rate.

Analyzing the case-study depicted in Figure 1-2, where at the equilibrium $E_F < E_T$:

1. At the thermodynamic equilibrium (Figure 1-2a), the capture-rate and the emission-rate are balanced, thus no net charge-trapping or detrapping mechanisms can be appreciated ($\partial N_{Filled}/\partial t = 0$). According to the occupancy ratio in equation (5), since $E_F < E_T$ , it is reasonable to assume that the majority of traps is empty ($N_{Filled}/N_{TOT} \approx 0$).
2. When the system is perturbed by increasing the quasi-Fermi level above the trap-level (Figure 1-2b), the capture probability becomes much higher than the emission probability ($c_n \gg e_n$), and the solution of equation (11) leads to the following exponential charge-trapping kinetics:

   $$N_{Filled}(t) = N_{TOT}\,[1 - e^{-c_n t}]$$

   where $c_n = 1/\tau_{cn}$.
3. Finally, assuming that all the majority of traps are filled ($N_{Filled}/N_{TOT} \approx 1$) and the external bias is removed (Figure 1-2c), the capture probability becomes much lower than the emission probability ($c_n \ll e_n$), and the solution of equation (11) leads to the following exponential charge detrapping kinetics:

   $$N_{Filled}(t) = N_{TOT}\, e^{-e_n t}$$

   where $e_n = 1/\tau_{en}$.

In order to better understand the implication of charge (de)trapping kinetics on the current-collapse phenomena and to interpret the deep-level transient spectroscopy results, the following essential observations can be drawn:

- *The capture probability depends intimately on the free carrier concentration*, which is expressed as $n = N_C\, Exp\big(-(E_C - E_{F,n})/kT\big)$. Being the quasi-Fermi

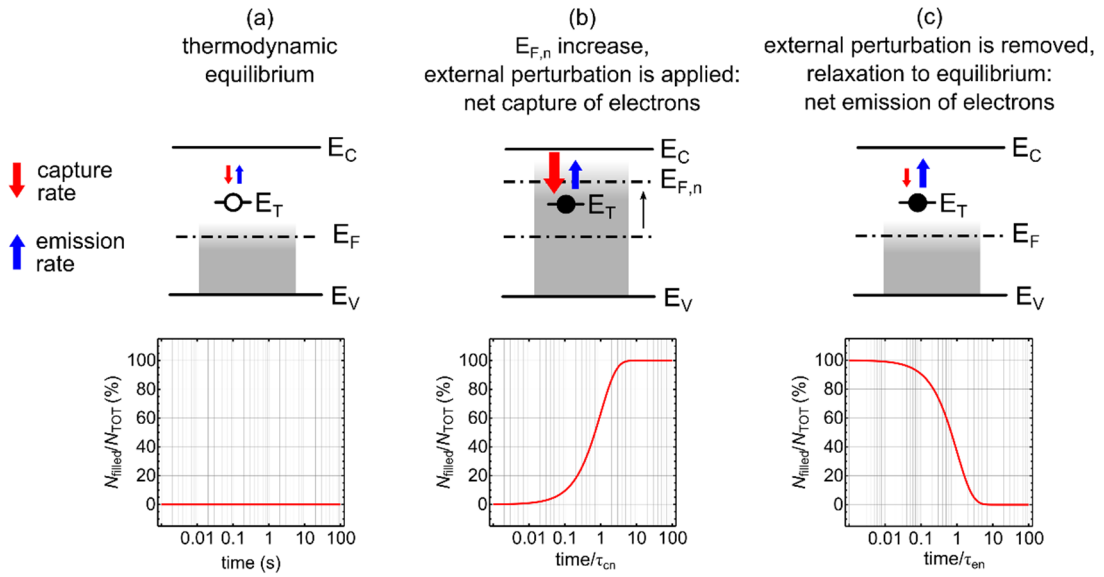



Figure 1-2 Schematic band-diagram and time evolution of trap-state occupancy under (a) arbitrary thermodynamic equilibrium, (b) bias-induced perturbation (filling or trapping phase), and (c) subsequent relaxation, detrapping phase.

level $E_{F,n}$ related to the applied bias, the capture probability is strongly bias-dependent. This is the key aspect for the charge (de)trapping and related current-collapse mechanisms. Under critical bias-conditions, some regions of the device can be expose to high electric field or to parasitic current injection. With respect to thermodynamic equilibrium, a bias-induced perturbation can lead to the increase (decrease) of the free-carrier concentration and the increase (decrease) of capture probability with respect to the emission probability promoting a net charge (de)trapping process.

- *The capture probability can be thermally activated*, i.e., increase exponentially with the temperature. The thermal activation of the capture probability can arise from *(i)* the thermal activation from the free-carrier concentration or *(ii)* the thermal activation of the capture cross-section. The former originates from the Fermi-Dirac distribution $Exp\left(-(E_C - E_{F,n})/kT\right)$: the higher is the temperature, the higher is free carrier concentration, the higher is capture probability. The latter, i.e., the activation energy of the capture cross-section, can be a feature of those defects which experience the "so-called" large lattice relaxation, i.e., in which the position, the bonding structure, and the electron configuration of the defect-state change with the charge-state of the center. In these cases, both the capture and the emission processes require the involvement of additional thermal energy (delivered by means of phonons) to accommodate the rearrangement of the defect coordinates [85].

- *The emission-probability is temperature activated* and, in low-field conditions, depends only on the trap energy level with respect to the conduction-band (in case of emission of electrons) or to the valence-band (in case of emission of holes). In this sense, it is by monitoring the charge de-trapping and the related emission probability that is possible to gather information on the deep-level signature in terms of apparent activation energy and apparent capture cross-section.
- Bias-dependent non-idealities affecting the extrapolation of the activation energy may be related to the Poole-Frenkel effect: in the case of donor-like traps, positively charged when empty, the energy barrier for the thermionic emission is lowered due to the applied electric-field and related band-bending. As a result, the emission-rate increase, leading to lower apparent activation energy [86].
- The Shockley-Read-Hall theory was originally developed to describe the interaction between free-carriers and deep-levels in the ideal-case of *bulk* materials, with no abrupt discontinuities in the space and energy domain. Nevertheless, with the advent of MOS devices and heterostructures, the capture and the emission of carriers may involve additional mechanisms: besides the conventional phonon-assisted (thermionic) capture and emission, trap-states may exchange free carriers via elastic, temperature-independent tunneling mechanisms. This is the common scenario of oxide traps in MOS gate structure, in which further analytical (or even numerical) modeling is required to grasp and predict the charge (de)trapping dynamics and related kinetics [84].

# 2 Characterization methodology

As will be reported in the next chapters, though GaN-based HEMTs represent good candidates for next generation microwave and power electronics [31] [87], their dynamic performance may be strongly affected by charge trapping phenomena [88], especially in relatively high-voltage operations.

One of the most evident effects of traps is the so-called current collapse, i.e. the dynamic decrease in drain current experienced by the device when operated with large gate-drain voltage swings [89]. This effect is strictly related to charge trapping at deep levels, which can be present in the as-grown material, related to the processing conditions [90], and/or induced by electrical stress.

The analysis of the current-collapse effects and the properties of the deep levels located in a HEMT structure is of fundamental importance for the following aspects: on one hand, it provides information on the dependence of the dynamic behaviour of the HEMTs on bias and temperature, which can be used for modelling the rf-characteristics of the devices; on the other hand, advanced techniques for defect characterization can be used for diagnostic purposes, i.e. for the identification of the nature of the deep levels generated as a consequence of electrical and thermal stress within the devices.

In this chapter, I will comprehensively discuss two essential measurement techniques employed for the analysis of charge-trapping phenomena: the double-pulse current-voltage (I-V) characterization (section 2.1), useful to quantify the effects of charge-trapping on the dynamic parameters of devices under test (in terms of threshold-voltage shift, transconductance degradation, and on-resistance increase), and the drain-current transient spectroscopy (DCTS, section 2.2), useful to identify the involved deep-trap-states.

In addition, I will briefly describe *(i)* the custom double-pulsed measurement system, designed and developed in order to obtain high-voltage drain-pulses up to 600 V (section 2.3); *(ii)* the on-the-fly pulsed measurement technique, which allow to investigate not only the detrapping, but also the trapping phase (section 2.4), *(iii)* a preliminary comparison between drain-current and capacitance deep-level transient spectroscopy performed on 3-terminal transistors and 2-terminal diodes, respectively (section 2.6), and *(iv)* the experimental evidence of surface-traps in unpassivated samples.

## 2.1 Double-Pulsed I-V measurements

A quick and reliable characterization of the current collapse can be obtained through the execution of pulsed drain-current vs drain- or gate-voltage ($I_D$-$V_D$ or $I_D$-$V_G$) measurements, which allow one to investigate the changes in drain current ($I_{DSS}$), on-resistance ($R_{ON}$) , transconductance ($g_m$) and threshold voltage ($V_{TH}$) induced by the capture of carriers at trap-states within the HEMT structure.

A schematic diagram of the double-pulse measurement is depicted in Figure 2-1. Both gate and drain contact are pulsed from a quiescent bias-point ($V_{G,Q}$;$V_{D,Q}$) to a measurement bias-point ($V_{G,Q}$;$V_{D,Q}$). During the measuring bias-point, the drain-current ($I_{DS}$) is acquired as the potential drop across a sense resistor (conventionally, in the order of 10-100 Ω). By tailoring the measuring bias-point, it is possible to sweep the whole $I_D$-$V_D$ and $I_D$-$V_G$ domain. By tailoring the quiescent bias-point, is it possible to inhibit or promote charge-trapping mechanisms. Typically, with the quiescent bias-point ($V_{G,Q}$;$V_{D,Q}$) = (0V;0V), we acquire the reference $I_D$-$V_D$ and $I_D$-$V_G$ characteristics, not affected by current-collapse. Then, with quiescent bias-points in high-field off-state ($V_{G,Q}$;$V_{D,Q}$) = ($V_{TH}$-2V;$V_{DD}$) or semi-on-state ($V_{G,Q}$;$V_{D,Q}$) = ($V_{TH}$+0.5V;$V_{DD}$), we promote the charge-trapping effects and monitor the related degradation of electrical performance. The pulse width, i.e., the measuring-bias period, is typically 1 µs (in this dissertation, referred either as $T_M$ or $T_{ON}$), whereas the pulse-period ranges typically from 100 µs to 1 ms (referred either as $T_Q$ or $T_{OFF}$).

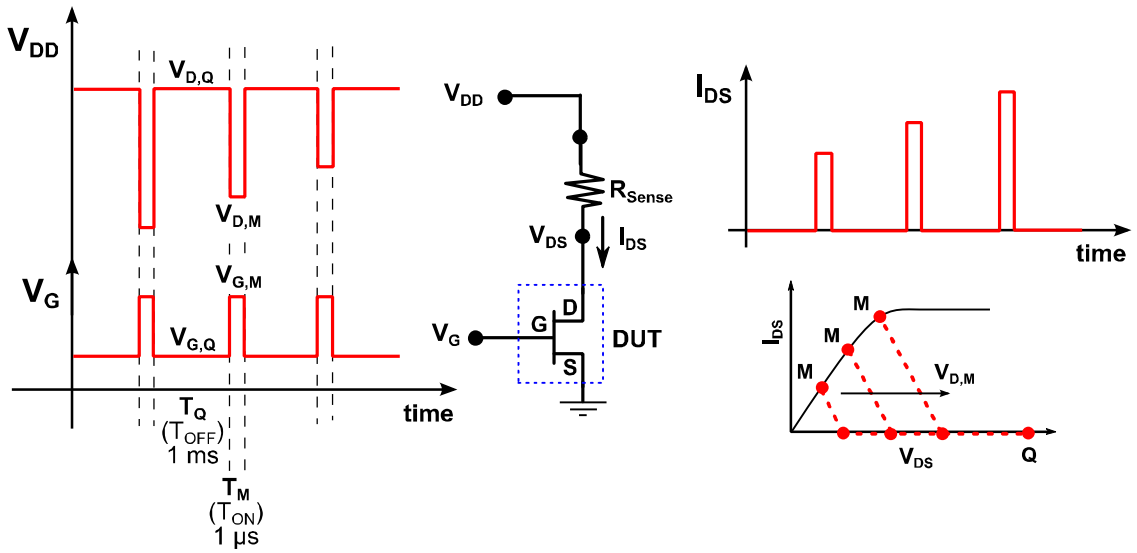



Figure 2-1 During double-pulse measurements, both gate and drain contact are pulsed from a quiescent-bias point ($V_{G,Q}$;$V_{D,Q}$) to a measurement bias point ($V_{G,Q}$;$V_{D,Q}$), and the drain-current ($I_{DS}$) is acquired as the potential drop across a sense resistor.

Representative double-pulsed $I_D$-$V_D$ and $I_D$-$V_G$ measurements performed on a test HEMT structure exposed to multiple off-state quiescent bias-points are reported in Figure 2-2. The monitored parameters which can be affected by charge-trapping effects include the saturation drain current ($I_{DSS}$), the on-resistance ($R_{ON}$), the threshold-voltage ($V_{TH}$), the transconductance peak ($g_{m,peak}$), and the transconductance droop ($g_{m,droop}$) evaluated at high gate-voltage ($V_{TH}$+3/4V).

By investigating how these parameters degrade when the device is exposed to off-state quiescent-bias allows a preliminary localization of defect-states within the complex HEMT structure. Meneghini *et al.* demonstrated that traps located in the region under the gate or in the access regions can be separately identified [90].

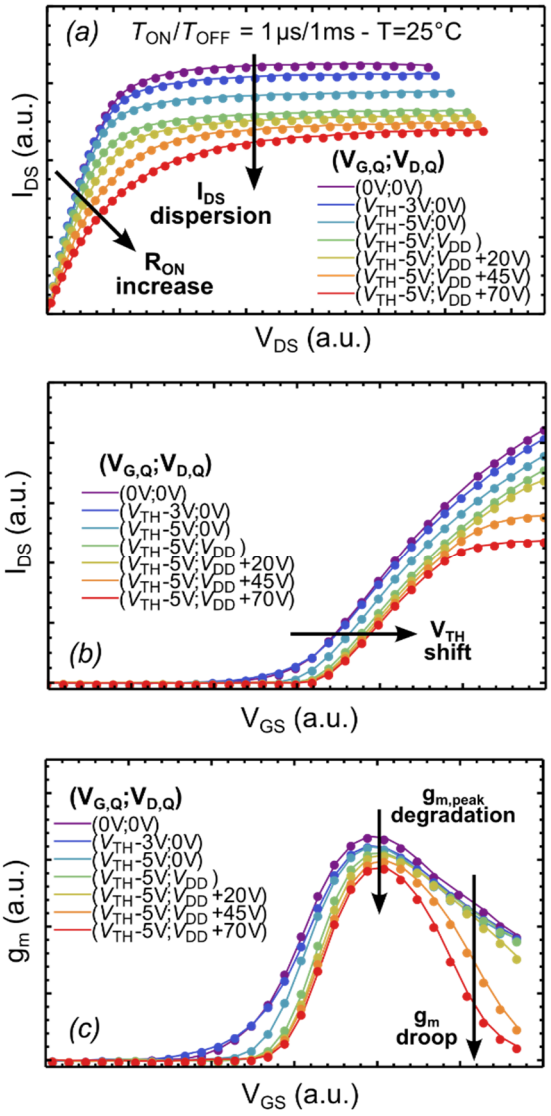



Figure 2-2 Double-pulsed *(a)* $I_D$-$V_D$ (b) $I_D$-$V_G$ , and *(c)* derived $g_m$-$V_G$ acquired on a test HEMT structure exposed to multiple off-state quiescent biases, with increasing drain-voltage.

Samples with large density of trapped charge located in the intrinsic device, i.e. in the region below the gate contact, exhibit predominantly a dynamic threshold-voltage shift ($\Delta V_{TH}$), as predicted in [91].

On the other hand, the presence of trapped-charge in the ungated source and drain access regions would increase the resistivity of the extrinsic device, promoting the dynamic decrease of the transconductance, with no significant modification of $V_{TH}$.

More in details, it is possible to discern whether the trapped charge is localized in the gate-source or in the gate-drain region by deconvolving two dominant effects on the transconductance curve: the $g_{m\text{-}peak}$ (degradation of the maximum value of the transconductance and the $g_{m\text{-}droop}$ (drop of the transconductance at high gate-voltage). By performing basics SPICE simulation of an intrinsic field-effect transistor with the inclusion of two distinct gate-source and gate-drain access resistances (modeled as lumped elements $R_S$ and $R_D$), we pointed out that an increase of $R_S$ (charge-trapping in the gate-source region) would mainly cause the degradation of the $g_{m\text{-}peak}$, whereas an increase of $R_D$ (charge-trapping in the gate-drain region) would mainly impact on the $g_{m\text{-}droop}$ at high gate-voltages. Results are depicted in Figure 2-3.

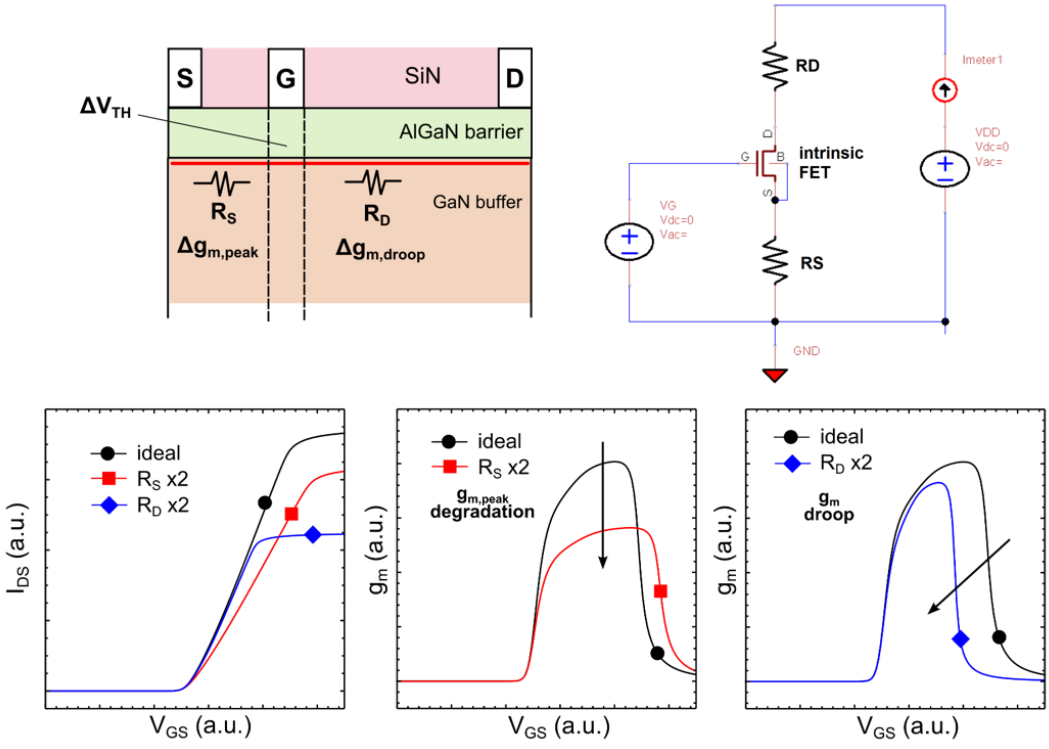



Figure 2-3 SPICE simulation of an intrinsic field-effect transistor with the inclusion of two distinct gate-source and gate-drain access resistances ($R_S$ and $R_D$). An increase of $R_S$ (charge-trapping in the gate-source region) would mainly cause the degradation of the $g_{m\text{-}peak}$, whereas an increase of $R_D$ (charge-trapping in the gate-drain region) would mainly impact on the $g_{m\text{-}droop}$.

In the following I am presenting three representative case-studies, to illustrate more in details the methodology reported so far.

The first case-study (case-study A) is represented by a Schottky-gated HEMT grown on a 3'' SiC substrate by means of metalorganic chemical vapour deposition (MOCVD) and devoted to microwave applications. The device structure consists of a 1.8µm GaN buffer layer, with a 22nm-thick AlGaN (18% Al) barrier. Gate-source spacing, gate-drain spacing, gate length and gate width are respectively 1µm, 3.5µm, 0.5µm and 100µm. The devices have a 1.3µm source-connected field-plate.

Figure 2-4 shows the $I_D$-$V_D$, $I_D$-$V_G$, and derived $g_m$-$V_G$ acquired exposing the device at different off-state quiescent bias points, up to $V_{D,Q}$ = 50 V. For the ($V_{GQ}$,$V_{DQ}$)=(-6V;50V) quiescent bias point, we measured a 40% decrease in $I_{DSS,}$ associated with a remarkable $V_{TH}$ positive shift (+700mV), slight $R_{ON}$ increase, and 20% $g_m$ peak reduction. Results indicate that, since the current collapse is mainly related to $V_{TH}$ positive shift, the deep levels which cause the majority of dynamic performance dispersion are located underneath the gate contact, into the (Al)GaN epitaxial layers. The slight $g_{m,peak}$ reduction may suggest minor trapping effects in the gate-source access region.

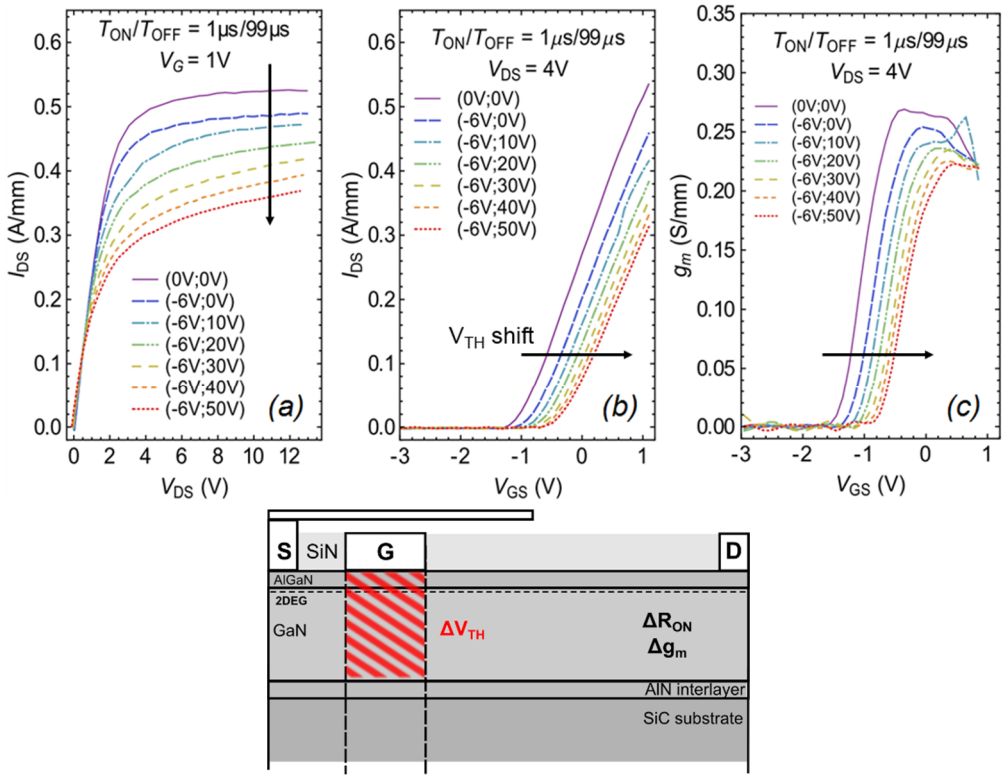



Figure 2-4 *(a)* $I_D$-$V_D$ (b) $I_D$-$V_G$ , and *(c)* $g_m$ (derived from $I_D$-$V_G$) pulsed characterization of case-study A: the dynamic current collapse is mainly caused by $V_{TH}$ positive shift, suggesting charge trapping within the epilayers in the intrinsic region below the gate contact. The employed pulse width/period ratio is 1µs/100µs.

The case-study B is represented by a preliminary HEMT structure designed for power switching application. The device structure is grown by means of MOCVD on a 4'' SiC wafer, and consists of a 1.8-µm-thick GaN buffer layer, with a 17-nm-thick AlGaN (22% Al) barrier. With respect to the first-case study, it features an up-scaled geometry in order to accommodate higher operating voltages: gate-source spacing, gate-drain spacing, and gate length are 2 µm, 20 µm, 2 µm, respectively. The devices have a 4 µm gate-connected field-plate.

Figure 2-5 shows the $I_D$-$V_D$, $I_D$-$V_G$, and derived $g_m$-$V_G$ acquired exposing the device at different off-state quiescent bias-points, up to $V_{D,Q}$ = 200 V. when subjected to high-drain-voltage quiescent bias-points, the device experiences a dramatic increase of the dynamic $R_{ON}$. From 0 V to 100 V, the dynamic on-resistance smoothly increases from 33.1 Ω·mm to 45.8 Ω·mm; from 100 V, it experiences a much steeper worsening, reaching 102 Ω·mm at $V_{D,Q}$ = 200 V. As can be noticed from $I_D$-$V_G$ and $g_m$-$V_G$ in Figure 2-5b and Figure 2-5c, the $R_{ON}$-increase is manifested in the droop of the transconductance, with no appreciable $V_{TH}$ shift. Conversely than in the previous case-study, these results indicate that, since the current collapse is mainly related to $R_{ON}$-increase and $g_m$-droop, the deep-levels and the charge-trapping mechanisms that cause the majority of dynamic

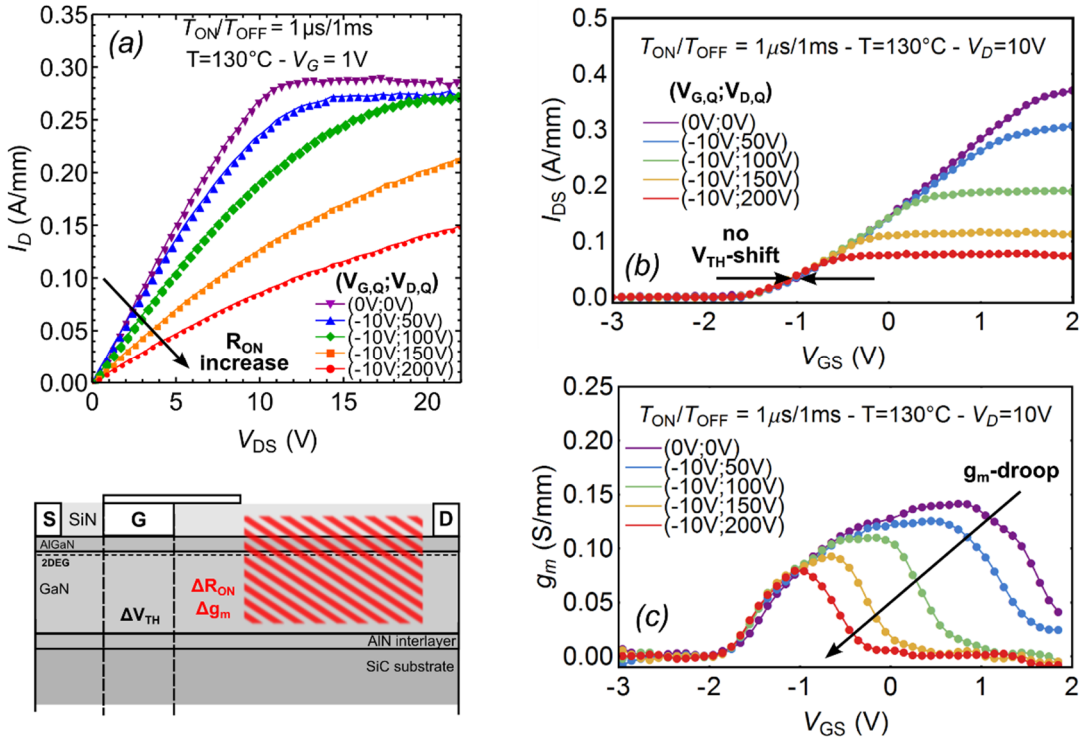



Figure 2-5 Double-pulsed *(a)* $I_D$-$V_D$ (b) $I_D$-$V_G$ , and *(c)* $g_m$-$V_G$ acquired on a preliminary power HEMT structure (case-study B) exposed to multiple off-state quiescent biases, with increasing drain-voltage up to 200 V. No $V_{TH}$-shift and remarkable $R_{ON}$-increase suggest that charge-trapping mechanisms are localized in the gate-drain access region.

performance dispersion are located within the gate-drain access region, potentially either in the SiN passivation or in the (Al)GaN epitaxial layers. Although Figure 2-5 shows the measurements acquired at 130°C, the reported $R_{ON}$ increase magnitude has been observed also at room temperature.

### 2.1.1 The role of the leakage current

The third case study (case-study C) is represented by the devices employed in the second case-study with the only addition of an 8-µm-long source-connected field-plate. This allow us to expose and characterize the behaviour of the sample up to 600 V. This case-study is important for two reasons: *(i)* it validates the double-pulsed measurement system up to 600 V, and *(ii)* provide interesting results on the potential correlation between the Schottky gate leakage-current and the parasitic charge-trapping effects.

What worth to be noticed is that when the device is biased with drain-voltages greater than 400 V, it experiences almost the total current collapse, i.e., the device behave as an open circuit also when it is supposed to act as a low resistive close circuit. This evidence proves the importance of high-voltage pulsed characterization for the effective development of power-oriented GaN-based HEMTs.

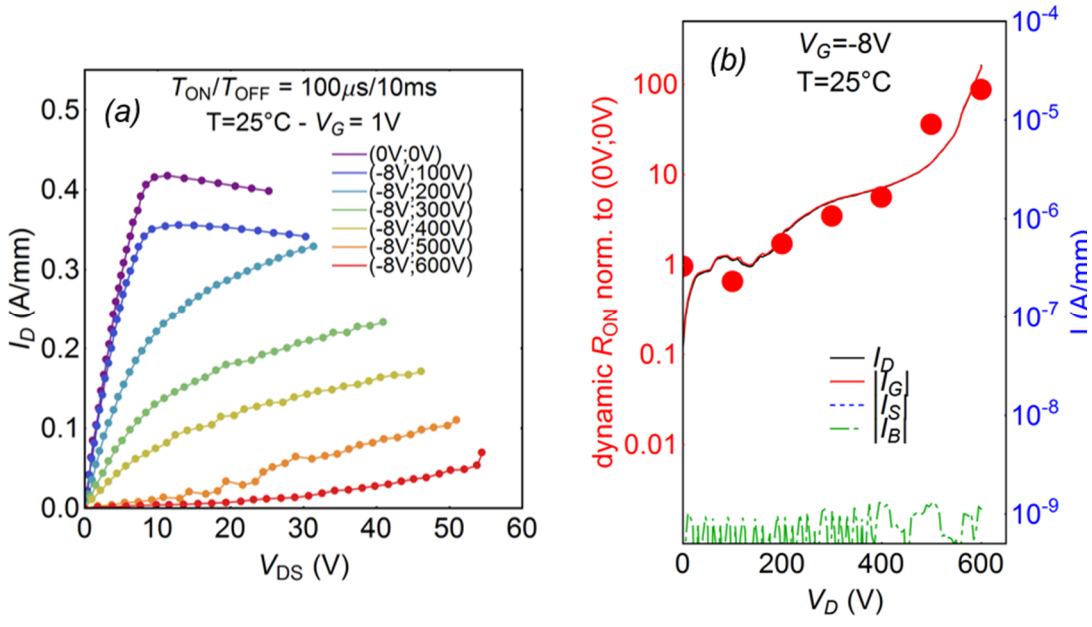



Figure 2-6 *(a)* double-pulsed $I_D$-$V_D$ acquired on a preliminary power HEMT structure (case-study C) exposed to multiple off-state quiescent biases, with increasing drain-voltage up to 600 V, *(b)* Superposition of the $R_{ON}$-increase and the leakage current promoted under high-voltage off-state. As can be noticed, an apparent correlation emerges between the $R_{ON}$-increase and the gate-leakage current, suggesting that the related charge-trapping mechanism may involve the injection of parasitic electrons from the gate metal into the epitaxial structure.

Besides the pulsed I-V characterization, an important step towards the comprehensive understanding of high-voltage charge-trapping issues is the investigation of any possible relation between charge-trapping and parasitic leakage-currents. To this aim, we have acquired (by means of a semiconductor parameter analyzer) the leakage-currents originating from the gate, source and substrate under high-voltage off-state regimes.

In this case-study, off-state leakage-currents originating from the source and the substrate contact are negligible throughout the $V_{DS}$ sweep from 0V to 600V (below the instrument resolution, 1nA/mm). Conversely, the reverse-biased gate-diode current experiences a remarkable increase from 60 nA/mm to 1μA/mm as the drain voltage is swept from 0V to 600V. Figure 2-6b illustrates the good correlation between the increase of the reverse gate-current and the increase of the dynamic $R_{ON}$. This would suggest that, in this case-study, the charge-trapping and the subsequent $R_{ON}$ increase could be likely promoted by the parasitic injection of electrons from the Schottky gate-contact into the deep-levels located within the epitaxial layers (and/or at the epitaxy/passivation interface) by means of transversal and/or longitudinal leakage-current paths [92] [93]. These experimental results shed light on the pivotal role played not only by the quality of the crystal growth but also by the possible origins of high-voltage leakage currents. Though the crystal and/or interface defectiveness determines the trap-states density, the parasitic leakage currents may represent the driving trapping-mechanism, by injecting parasitic carriers within the structure and providing additional charge available for being trapped. Further experimental evidence on the correlation between leakage current and charge-trapping mechanisms is reported in Chapter 4, section 4.4.

## 2.2 Drain Current Transient Spectroscopy

Thanks to the fact that it explores the whole output and transfer characteristics, pulsed $I_D$-$V_D$ and $I_D$-$V_G$ characterization is very effective for the investigation of current collapse; however, since its time acquisition window is fixed in the micro-seconds range, it does not provide information on the kinetics of involved charge (de)trapping mechanisms, and the subsequent identification of involved deep-levels. For this reason, deep-level transient spectroscopy, capable for the resolution and the identification of involved deep-trap states, is required. To this aim, several methods based on the analysis of a capacitance or current transients generated by the charging/discharging of defect-states have been proposed.

Capacitance-mode Deep-Level Transient Spectroscopy (C-DLTS) and Deep-Level Optical Spectroscopy (DLOS) have been widely employed to identify the deep levels: in most of the cases, the measurements are carried out on large area Schottky diodes, since can be difficultly applied to small periphery transistors due to their small gate capacitance. Unfortunately, the distribution of the electric field is significantly different in diodes and in actual transistors; therefore the results obtained by analyzing diodes provide information on the properties of the deep levels, but do not give a clear indication on where those levels are located in a HEMT structure, and on how they can influence the dynamic behaviour of the actual devices.

Contrarily, the effective description of the properties of the traps relevant for GaN-based transistors operation can be obtained by studying the time-resolved step-response of drain current induced by exposure to a trapping voltage, either through current-mode DLTS (I-

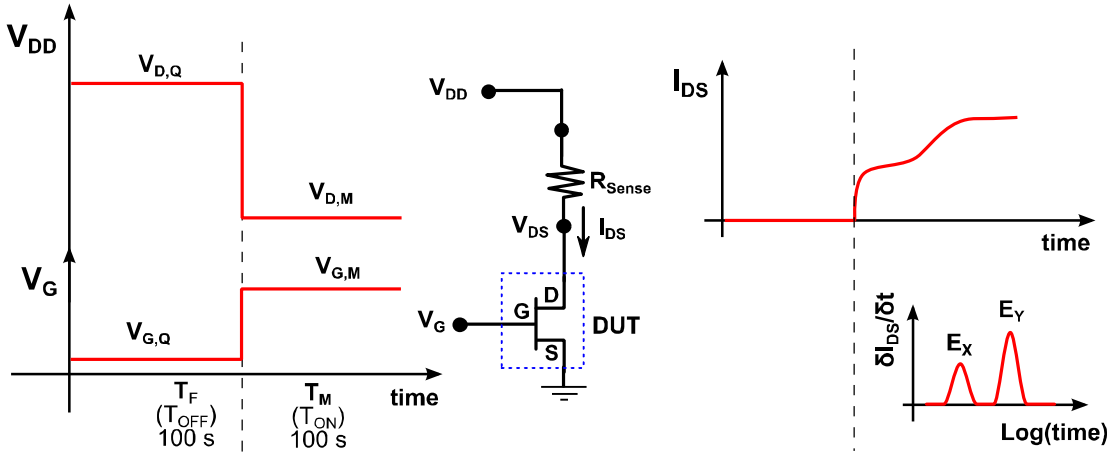



Figure 2-7 Device under test is subjected to a stress/trapping phase ($V_{G,F}$;$V_{DF}$, typically in the off-state or semi-on-state for a period of 100 s); then, it is biased in a low-field, low-power on-state ($V_{G,M}$;$V_{DM}$, typically in linear region, or right after the knee voltage) to permit the acquisition of the drain-current response and the analysis of the related time-constant spectrum.

DLTS) [88] [94] [95] or drain-current transient spectroscopy [96] [97] [98] [99] [100]: the latter method is faster, since it does not require to carry out a full temperature scan, but only to measure the current transients at some (5-10) temperature levels.

A schematic representation of drain current transient measurement is depicted in Figure 2-7. Firstly, the device under test is subjected to a trapping phase ($V_{G,F}$;$V_{D,F}$, typically in the off-state or semi-on-state, for a period of 100 s). Then, it is biased in a low-field, low-power on-state ($V_{G,M}$;$V_{D,M}$, typically in linear region, or in the saturation region close to the knee voltage) to permit the acquisition of the drain-current response and the analysis of the related time-constant spectrum.

Despite the relative simplicity of this technique, the choice of the parameters used for the measurements, and the method used for the analysis of the transients can strongly affect the results of the study. In the following, I will report few key guidelines concerning *(i)* the choice of the filling and the measuring bias-points, *(ii)* the modelling of the (non)exponential (de)trapping processing and the extrapolation of the related time-constant, *(iii)* the identification of the deep-level signatures (in terms of activation energy $E_A$ and capture cross-section $\sigma_c$) and their interpretation, and *(iv)* the study of the filling time-dependence. The following discussion is based on measurements performed on the case-study A, already characterized by means of pulsed $I_D$-$V_D$ and $I_D$-$V_G$ measurements in the previous section.

### 2.2.1 **Measuring bias-point**

The drain-current transients can be measured both in the linear [97] [101] [100] [99] and in the saturation region [96] [102]: the choice of the measuring point can significantly influence the results of the investigation, and – in some cases – hinder the observation of some trap levels.

Experimental data carried out by analysing the charge de-trapping transients either in the linear or in the saturation region (Figure 2-8) indicate that the choice of the bias point used for the measurement of the de-trapping transient can have a significant impact on the results: for the specific case-study, the transient recorded in linear region detected only a weak emission process (blue curve in Figure 2-8), while that recorded in saturation region (red curve in Figure 2-8) revealed remarkable current collapse, and the presence of two distinct current recovery processes, whose peaks in the derivative spectrum in logarithmic time scale (Figure 2-8b) have been labelled respectively “E2” and “$E_X$”. This result is very well correlated with that obtained with pulsed measurements (Figure 2-4), which indicate that current collapse is mainly caused by threshold voltage shift, hence manifesting itself predominantly in saturation region.

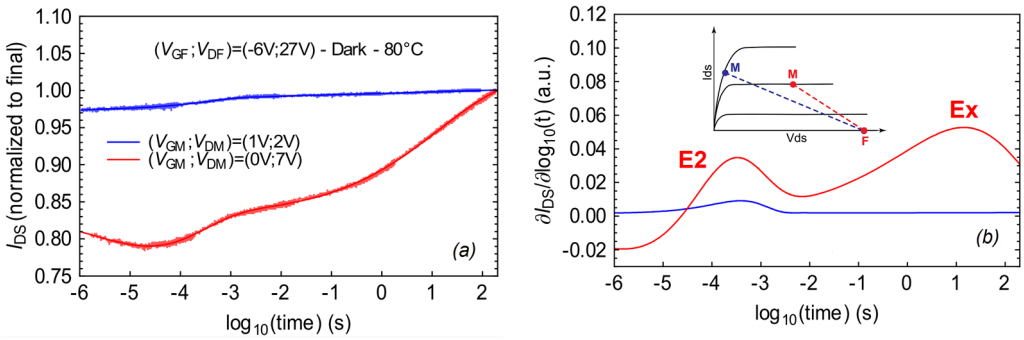



Figure 2-8 *(a)* Drain current transients performed in the linear and saturation regions, and *(b)* related differential signals: in good agreement with pulsed measurement, transients recorded in linear region detect only a weak emission process, while those recorded in saturation region reveal much higher current collapse and the presence of two emission processes labeled E2 and EX.

What worth to be learnt from this experiment is that to obtain meaningful and exhaustive deep-level spectroscopy, the measurement bias should lie in the current-voltage region in which the device under test suffers from the most prominent current-dispersion effects. As will be extensively reported in Chapter 4, to investigate the deep-levels responsible for charge-trapping mechanisms in devices suffering from $R_{ON}$-increase and negligible $V_{TH}$-shift, drain-current transient spectroscopy should be performed by acquiring the drain-current in the linear region rather than in the saturation region.

### 2.2.2 **Filling bias-point**

In the following, we demonstrate that through the use of proper trap filling voltages it is possible to achieve information on the location of the traps. This result was obtained by carrying out a set of transient measurements, starting from three different filling bias conditions: in the off-state ($V_{GF}$;$V_{DF}$)=(-6V;27V), with both high negative $V_{GS}$ and high positive $V_{DS}$, promoting both gate- and drain-dependent trapping; in the semi-on-state ($V_{GF}$;$V_{DF}$)=(-1V;27V), with high $V_{DS}$ level, promoting only the drain-dependent trapping mechanisms; and in the off-state ($V_{GF}$;$V_{DF}$)=(-6V;8V), with high negative $V_{GS}$ and low $V_{DS}$, in order to probe predominantly the gate-dependent trapping mechanisms.

The results of this comparison are summarized in Figure 2-9, and indicate the presence of several de-trapping transients: the amplitude of the transient labeled as "E2" is enhanced by filling pulses with high drain voltage, and experiences its maximum amplitude under semi-on trapping conditions ($V_{GF;}V_{DF}$)=(-1V;27V). On the contrary, the broad spectrum of transient "$E_X$" is constituted by two components: one drain-influenced (labeled E5), which is enhanced during semi-on condition, and one gate-influenced (labeled $E_{XG}$) which is enhanced during off-state trapping with moderate drain voltages and high negative gate bias ($V_{GF;}V_{DF}$)=(-6V,8V). Furthermore, during semi-on trapping condition an additional weak electron-capture or hole-emission process (labeled H1) is

detected. The results described in Figure 2-9 therefore indicate that by choosing proper filling voltages it is possible to distinguish between drain- and gate-dependent trapping processes.

The peaks E2 and E5 – whose amplitude is maximized by the combination of high drain voltage and relatively high drain current levels – can be ascribed to the trapping of negative charge in the buffer region, likely promoted by hot-electrons (see case *(1)* in Figure 2-10a). On the other hand, trap $E_{XG}$ is supposed to be located in the region under the gate, where charge trapping could be promoted by high reverse gate voltage and the subsequent high gate leakage current levels (see case *(2)* in Figure 2-10b).

The surface-related trapping phenomena, reported for completeness in Figure 2-10b (case 3), are unlikely to occur in this case-study since only slight dynamic degradation of the extrinsic parameters is detected. Thanks to unpassivated devices belonging to another experiment, we will present evidence of surface-related trapping in section 2.5.

The possible involvement of gate-leakage current originating from the Schottky gate contact have been reported in section 2.1.1, whereas further, striking evidence of hot-electrons-related trapping mechanisms will be described in Chapter 4, section 4.3.

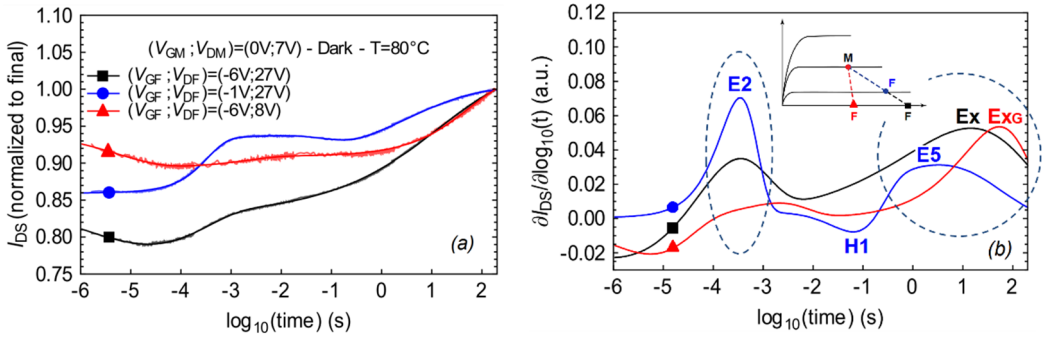



Figure 2-9 *(a)* Drain current transients recorded after different trapping conditions, and *(b)* related differential signals: E2 amplitude is enhanced by the combination of drain voltage and drain current experiencing his maximum after semi-on trapping condition, whereas broad EX spectrum is composed by one drain-influenced component (E5) and one gate-influenced component (EXG).

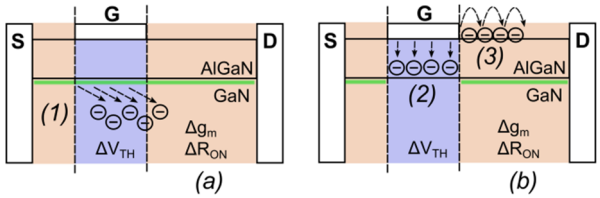



Figure 2-10 Possible trapping mechanisms and their influence on electrical parameters in (a) Semi-ON-state and (b) OFF-state bias operating points.

### 2.2.3 Extrapolation of charge (de)trapping time constants

Several methods can be used for the extrapolation of the time constants of the charge emission processes: the multi-exponential fitting [97] [103] [101], the analysis of the derivative of the current transients (the peak of the derivative is located in correspondence of the time constant of the emission process) [100] [99], and the stretched exponential fitting [96] have been adopted by various research groups. The choice of the method can modify the results of the investigation, since it can significantly change the shape and slope of the Arrhenius plot.

In our research activity, we implemented and compared three different methods for the evaluation of time constants: *(i)* the fitting of transient data by a polynomial function, and the subsequent extrapolation of time constants from the peaks of the $\partial I_{DS}/\partial \log(t)$ (derivative) curves [100], *(ii)* the fitting of the data by a function represented by the sum of 100 exponentials with fixed time constants and variable amplitude coefficients [97], and *(iii)* the fitting of the data by the stretched multi exponential function

$$I_{DS}(t) = I_{DS,final} - \sum_{i}^{N} A_i e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}}$$

where the fitting parameters $A_i$, $\tau_i$ and $\beta_i$ are respectively the amplitude, the typical time constant and the non-exponential stretching-factor of the $N$ detected charge emission ($A_i > 0$) or capture ($A_i < 0$) processes ($N$ typically ranges between 2 and 4 depending on the analysed samples). The comparative results of the different fitting algorithms are summarized in Figure 2-11. As can be noticed, the three methods provide different behaviors: in the ideal case of almost purely exponential transient (trap E2), the three methods return similar fitting parameters, hence leading to the same Arrhenius plot (see level E2 in Figure 2-12c); conversely, in the presence of stretched non-exponential

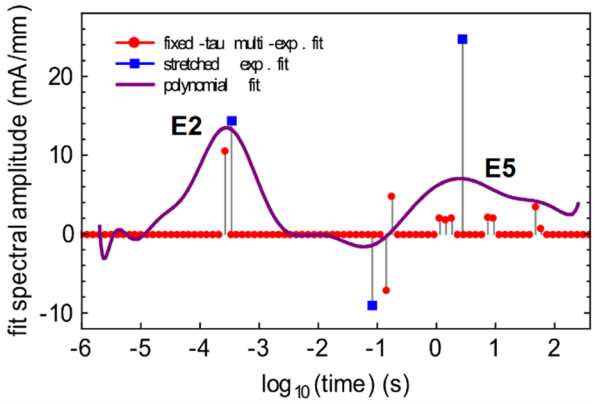



Figure 2-11 Comparison among the three data fitting algorithms: the sum of 100 exponentials with fixed time constants and variable amplitude coefficients; the sum of few stretched exponentials with variable time constants and amplitude coefficients, and a polynomial function with the subsequent extrapolation of time constants from the peaks of the $\partial I_{DS}/\partial \log(t)$.

processes (e.g., trap E5) the output of both polynomial and fixed-tau multi-exponentials fitting methods are affected by spectral dispersion, which manifest itself as the distortion of the differential current peak (for the polynomial fit case) or the splitting of spectral lines (for the multi-exp. fit). As a consequence, the time constants extrapolated by means of polynomial fitting and fixed-tau multi-exponential can significantly differ from those obtained through stretched exponential fitting: this difference may lead to a wrong extrapolation of the Arrhenius plots (level E5 in Figure 2-12c).

Previous literature reports ascribed the presence of strongly non-exponential transients to the following causes: *(i)* current transients originate from the superposition of different deep-levels emission processes [104]: as shown in Figure 2-9, $E_X$ is indeed composed by the namely E5 (drain-dependent) and $E_{XG}$ (gate-dependent) trap states; *(ii)* current transients are related to the presence of high density of defect states, as in the case of extended line defects, that lead to trapped electron delocalization and formation of mini-bands [105] [106]; *(iii)* current transients originate from the presence of defect states in alloy materials, such as $Al_XGa_{(1-X)}N$, which lead to deep-level splitting due to band discontinuity [107]; *(iv)* the charge emission parameters vary with the non-uniform distribution of the electric field within the complex HEMT structure [105]; and *(v)* trapping/de-trapping kinetics are not governed by thermal emission, but by other mechanisms, such as hopping or trap-assisted-tunnelling in the case of surface-traps [108] [109].

### 2.2.4 Identification of the deep-level signatures

For a better understanding of the properties of the deep levels responsible for current collapse, it is necessary to extrapolate the Arrhenius plots of the traps and their signature in terms of activation energies and capture cross-sections. These data are obtained by carrying out the current transient investigation at several temperature levels. The results of this investigation are summarized in Figure 2-12 and Figure 2-13: the signatures of E2, E5 and H1 (Figure 2-12) correspond to apparent activation energies and apparent capture-cross sections of 0.62 eV and $8.7 \times 10^{-15} cm^2$ for E2; 1.10 eV and $3.9 \times 10^{-12} cm^2$ for E5; and 0.91 eV and $3.3 \times 10^{-13} cm^2$ for H1. Conversely, $E_{XG}$ experiences very low thermal activation (<0.1 eV) and typical time constants in the order of 100s (Figure 2-13).

Neglecting the self-heating of the devices during the analysis of the current transients may lead to a wrong extrapolation of the Arrhenius plots. In order to avoid results

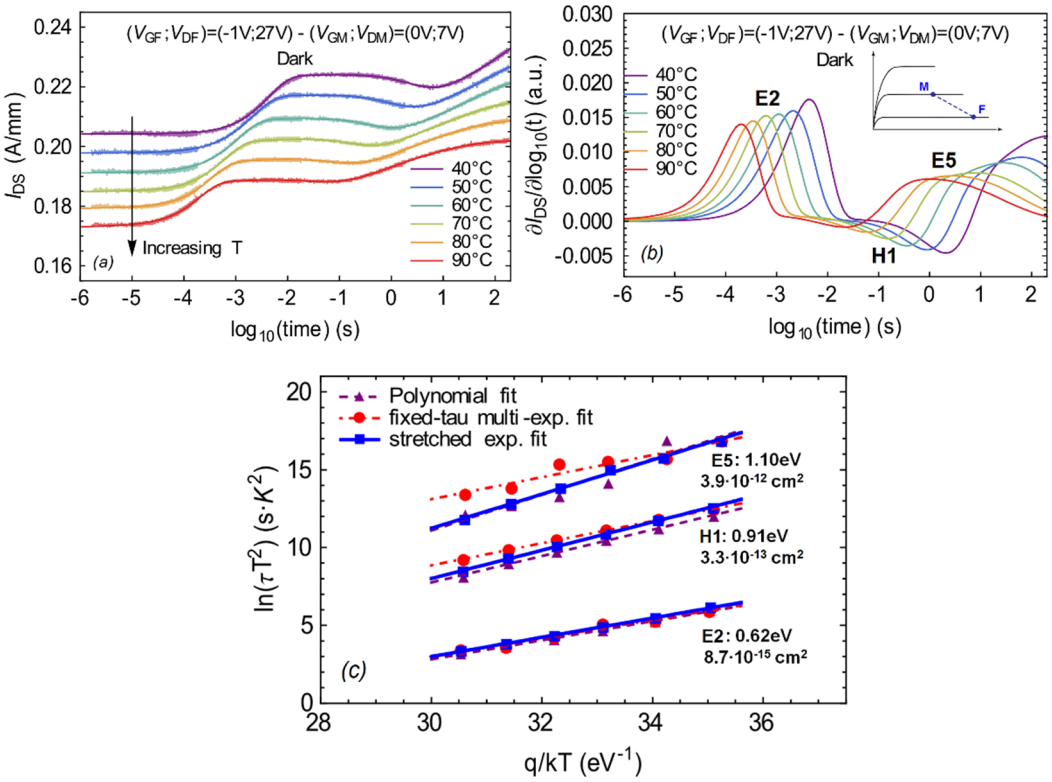



Figure 2-12 *(a)* Drain current transient acquired at multiple temperatures, and *(b)* related time-constant spectra. *(c)* Arrhenius plot with apparent activation energies ($E_A$) and capture cross-sections ($\sigma_c$) extrapolated by stretched exponential fit of E2- E5- and H1-related de-trapping processes. Comparison with other fitting methods is also reported.

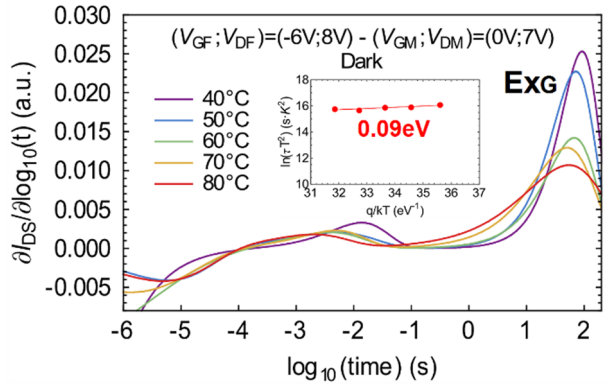



Figure 2-13 Thermal activation of $E_{XG}$ signal: very low activation energy and detrapping time constant in the order of 100s have been identified.

misinterpretation, the actual device temperature has been estimated taking into account the dissipated power during the measurement phase (around 1.5 W/mm) and the thermal resistance of the device (10 Kmm/W) measured by means of the pulsed-current method described by Joh *et al.* [110]. Further details on the importance of temperature correction are extensively reported by Chini *et al.* in [111].

### 2.2.5 **Filling-time dependence**

In the following, we demonstrate that it is possible to obtain more detailed information on the characteristics of the traps described above, by investigating the dependence of the signal related to traps E2, and E5 on the duration of the filling pulse used to promote the charge trapping.

For this investigation, trapping condition ($V_{GF}$ ;$V_{DF}$) = (-1V;27V) and temperature (80°C) were kept constant, whereas filling time has been varied from 100s down to 100µs. As can be observed in Figure 2-14, the amplitude of E5 displays a logarithmic dependence on the duration of the filling pulse.

Among the possible interpretations of this phenomenon, the corresponding trap level may be *tentatively* related to the presence of highly localized defect states, such as dislocations. As described in [112] [113] [67], the charging of either dislocation core sites, or hypothetical point defects and impurities segregated around the dislocations, would cause a constant reduction of the capture rate due to the formation of a Coulomb capture barrier with the increase of negative trapped charge. According to [67], the dependence of the charge filling time (before the saturation of the filled trap states) can be expressed as

$$n_T(t_F) = c_n \tau N_T \ln\left(1 + \frac{t_F}{\tau}\right)$$

where $c_n$, $N_T$ and $\tau$ represent respectively the capture probability, the defect states density and the characteristic time for the capture barrier build-up.

A more precise and reliable analysis of filling-time dependence can be obtained by means of on-the-fly pulsed measurement: its methodology is introduced in section 2.4, whereas some interesting results concerning the kinetics of charge-trapping mechanisms are reported in Chapter 4.

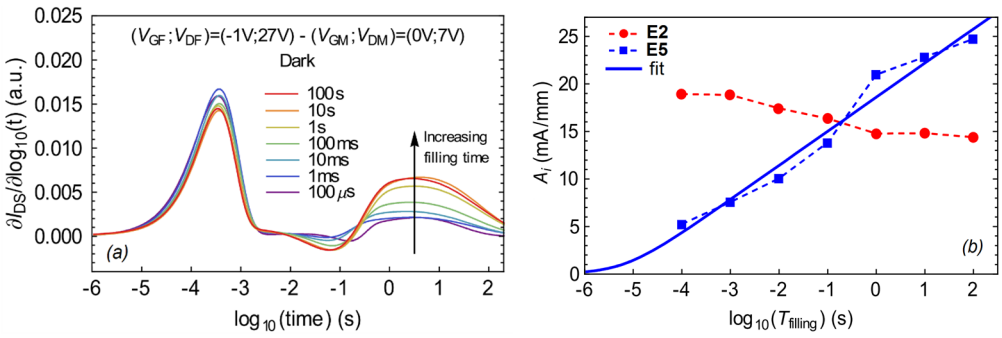



Figure 2-14 *(a)* E2 and E5 spectra and *(b)* their amplitudes recorded by adopting different filling times.

### 2.2.6 Identification of defects by a database of deep levels

The understanding of the physical origin of a trap is not straightforward, even though the activation energy and cross section of the corresponding deep level have been accurately extrapolated. To compare the results obtained within this work with previous literature reports, we have constructed a database of the deep levels presented over the last decades in more than 60 journal papers. In Figure 2-15 and Figure 2-16 we report the comparison between the signatures of the deep levels detected within this work and previous literature references.

As can be noticed, the signature of trap E2 ($E_A$=0.62eV; $\sigma_c$=8.7x10$^{-15}$cm$^2$) reveals good matching with the electron-trap E2/$E_C$-0.60eV which is broadly detected in several works regarding both n-type GaN Schottky-diode and HEMT structures [114] [97] [67] [115] [116] [117] [118] [119] [120] [121] [122] [123] [124] [125] [126] [127] [128]. This level has been generally ascribed to GaN defects, even though its origin is still controversial: Nitrogen anti-site native point defect [114] [117] and foreign impurities and dopants (C [122], Si [129], Mg-H complex [115], Fe [128]) have been also reported.

Level E5 ($E_A$=1.10eV; $\sigma_c$=3.9x10$^{-12}$cm$^2$) reveals similar signature of deep levels associated with GaN dislocations [116] [130] [131] [132], which would be consistent with the logarithmic filling time dependence reported in previous section.

Level H1 ($E_A$=0.91eV; $\sigma_c$=3.3x10$^{-13}$cm$^2$) displays similar signature with $V_{GA}$-related deep acceptor states reported in [120] [133] [134] [135] (in this case the 0.91 eV apparent activation energy represent the trap level energy from the valence band maximum). The level $E_V$ + 0.9 eV has been also reported more recently in [136] as possible charge-state transition of Carbon impurities in Nitrogen substitutional position ($C_N$).

Finally, the very low thermal activation and the very slow de-trapping typical time constant of the gate-influenced $E_{XG}$, are similar to trap signature detected and reported by Tapajna *et al.* [100], and could be supported by these explanations: *(i)* electron transport mechanism dominated by RC discharging processes, *(ii)* superficial shallow states filled and emptied by hopping conduction mechanisms, or *(iii)* deep-levels charge de-trapping by tunneling mechanisms. In other words, as we will show also in the next section, it may happens that drain-current transient spectroscopy acquired on complex HEMT structures features peculiar de-trapping processes not governed by the conventional thermionic-emission described by the SRH model, but other transport-limited mechanisms which required ad-hoc modelling.

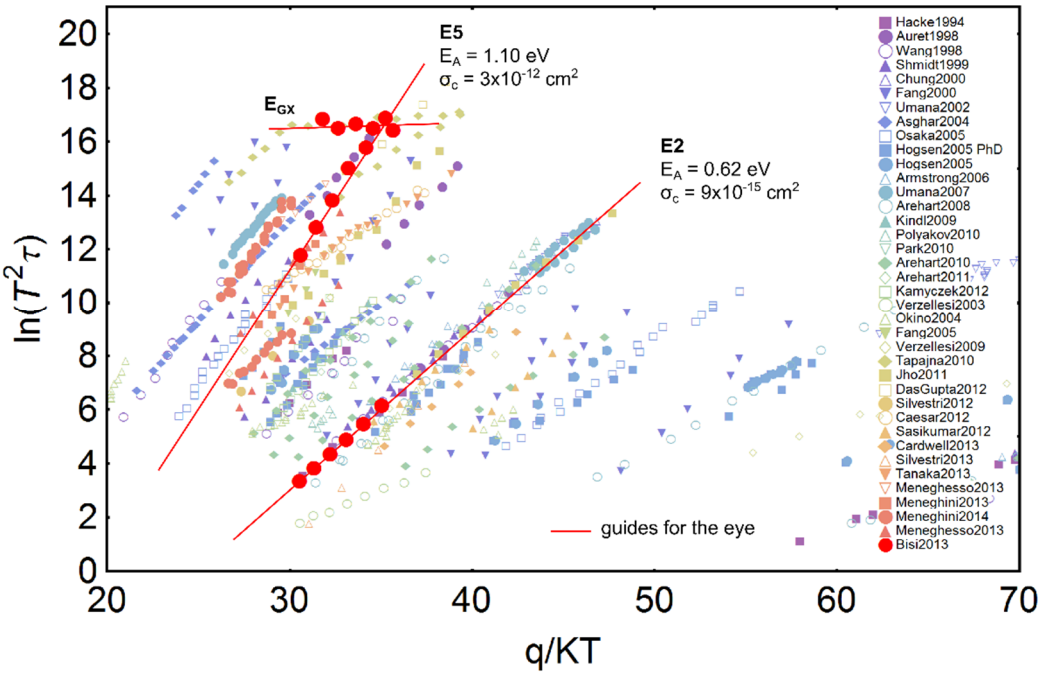



Figure 2-15 Superposition of deep-level signatures reported in the literature on GaN-based devices and those obtained in this work, tentatively ascribed to electron traps.

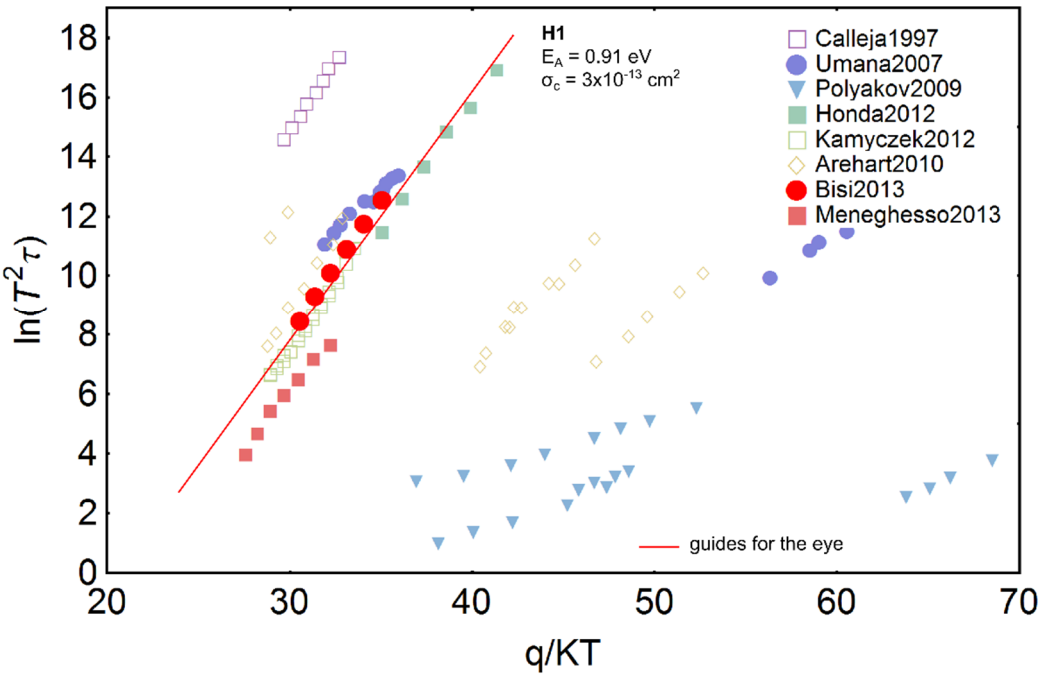



Figure 2-16 Superposition of deep-level signatures reported in the literature on GaN-based devices and those obtained in this work, tentatively ascribed to hole traps.

## 2.3 High-voltage pulsed measurement system

Since GaN-based HEMTs represent excellent candidates not only as power amplifiers in microwave systems, but also as power switches in high-voltage and high-power application, the characterization of charge-trapping phenomena at high-voltage regime play a key role for the development of GaN-based HEMTs technologies. Latent at low voltages, parasitic charge-trapping can be violently enhanced under critical high-voltage conditions, promoting the degradation of the dynamic parameters, e.g., the dynamic on-resistance ($R_{ON}$). For these reasons, the upgrading of the time-resolved characterization methodologies is of primary importance in order to properly identify the charge-trapping mechanisms and quantify their effects in high-voltage operational regimes. In the following, I will describe a high-voltage pulsed system designed and developed at the University of Padova during this doctoral research program.

The system, capable of both double-pulsed I-V characterization and drain current transient spectroscopy, is schematically depicted in Figure 2-17. It includes: (i) two low-power pulse generators; (ii) two high-speed power amplifiers, needed for the high-voltage pulses amplification; and (iii) a current-sensing resistor, a high-voltage differential probe, and a low-power signal acquisition module, devoted to the time-resolved acquisition of the drain-current and the related drain-voltage. The low-power functionalities, including the pulse generation and time-resolved signal acquisition, could be either implemented by stand-alone instrumentation, e.g., arbitrary waveform generators and oscilloscope, or embedded in a single low power, low-cost FPGA system. Similarly, stand-alone modules can implement the pulse amplification and the differential voltage-probing. High-voltage

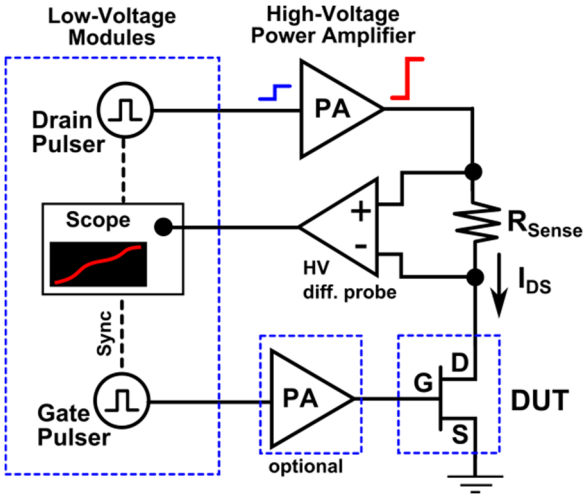



Figure 2-17. Schematic diagram of the proposed high-voltage double-pulsed sytem, including low-voltage pulse generators, high-speed power amplifiers, and high-voltage differential probe devoted to the current probing.

amplifiers, featuring output-voltage up to 1.4 kV and slew-rates greater than 370 V/µs, are already available on the market.

The three main advantages of the proposed setup are briefly summarized in the following. *First*, the time-resolved drain-current transient characterization inherits the advantages of the double-pulse system. Contrarily to the conventional fixed-$V_{DD}$ gate-lag technique, the proposed system allows to pulse not only the gate- but also the drain-voltage. As depicted in Figure 2-18, this allows the releasing of the load-line constrains between the trapping and the measuring phases. The possibility to adopt a very low resistive-load (which only purpose is the current-probing) strongly mitigates the detrimental measuring-bias variations caused by the dynamic (de)trapping processes experienced during the measurements. Figure 2-19 depicts the comparison of transient measurements stepping from $V_{DS}$ = 200 V to $V_{DS}$ = 12 V performed with the conventional gate-lag and the proposed double-pulse systems, which employ 20 kΩ and 100 Ω load-resistors, respectively. Due to the steeper load-line, the double-pulse system reveals more stable drain-voltage and more stable channel-temperature throughout the measurements, which are recommended conditions for reliable deep-levels identification.

*Second*, the consistency of the time-resolved data acquisition is assured throughout the time acquisition window. Thanks to the extremely wide bandwidth and memory-depth of the modern acquisition modules, no instrumentation swap is needed to cover the entire time span from 1µs to 100s, conversely to what proposed by Jin *et al.* in [137] where two different instruments are used to investigate the fast and slow time decades.

*Third*, the front-end stage of the low-power acquisition module in not directly connected to the drain terminal, therefore it is not strongly saturated during the high-voltage off-state biases. Thanks to high-voltage differential probing, the low-power acquisition module must neither bear the high drain-voltages responsible for the slow, detrimental front-end recovery transients, nor implement any additional clipping circuit.

Figure 2-20 depicts the $V_{DS}$, $V_{GS}$ and $I_D$ waveforms acquired during 200V off/on transition: in these conditions, the latency (defined as the delay between the beginning of the drain-pulse and the first valid $I_{DS}$ data) is 800 ns. The two spurious current peaks, detected in correspondence of the $V_{DS}$ pulse-edges, account for the (dis)charge of the coaxial cable parasitic capacitance: it has been experimentally proved that (i) their peak amplitude is proportional to the drain cable parasitic capacitance times $\partial V_{DS}/\partial t$, and (ii) the related parasitic current does not actually flow through the device under test, hence it does not affect its dynamic behavior.

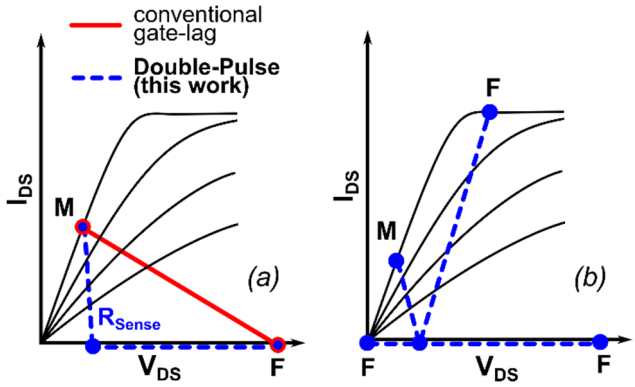



Figure 2-18. (a) Comparison between conventional fixed-$V_{DD}$ gate-lag technique and proposed double-pulsed technique. The latter allows the releasing of the load-line constrains, and the de-coupling of Filling/Measuring (F/M) bias-pairs. (b) Examples of filling and measuring bias-points which would require negative load-resistors, achievable only with the proposed double-pulsed technique.

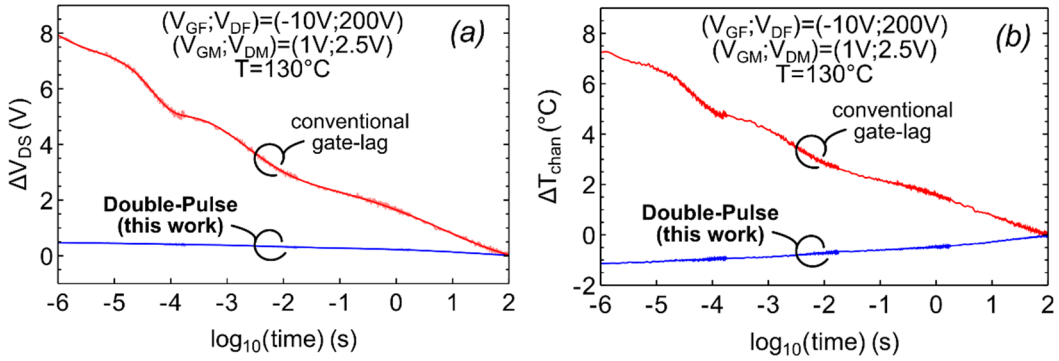



Figure 2-19. Drift of (a) drain-voltage, and (b) channel-temperature during the de-trapping transient acquired with conventional gate-lag and proposed double-pulsed techniques. The latter exhibits more stable values throughout the measurement.

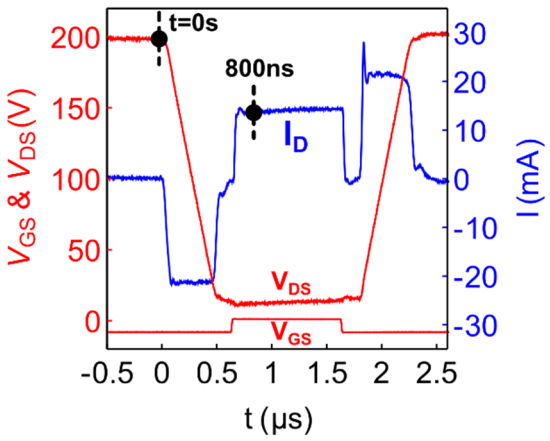



Figure 2-20. Typical $V_{DS}$, $V_{GS}$ and $I_D$ waveforms, acquired during off/on/off transition. $V_{DS}$ and $V_{GS}$ are stepped from 200V to 12V, and from -8V to 1V, respectively.

Concerning the specific case-study, the system developed at the University of Padova employs the following:

- two Agilent 33250A 80MHz arbitrary waveform generators,
- two FLC electronics A400 high-voltage linear amplifiers (with a slew-rate of 400V/µs),
- an Agilent N2791A 25MHz high-voltage differential probe,
- and a Tektronix TDS 654C 500MHz digital oscilloscope.

The maximum gate- and drain-voltages are imposed by the high-voltage amplifiers limits: the FLC A400 features a maximum output-voltage swing of ±200 V. In order to extend the limits up to 700 V, we employed a Trek PDZ700A high-voltage power amplifier.

Figure 2-21 shows the results of a brief calibration test of the system performed on a high-power 100 kΩ resistor (theoretically immune to charge-trapping and current dispersion effects) exposed to quiescent bias-point up to 600 V.

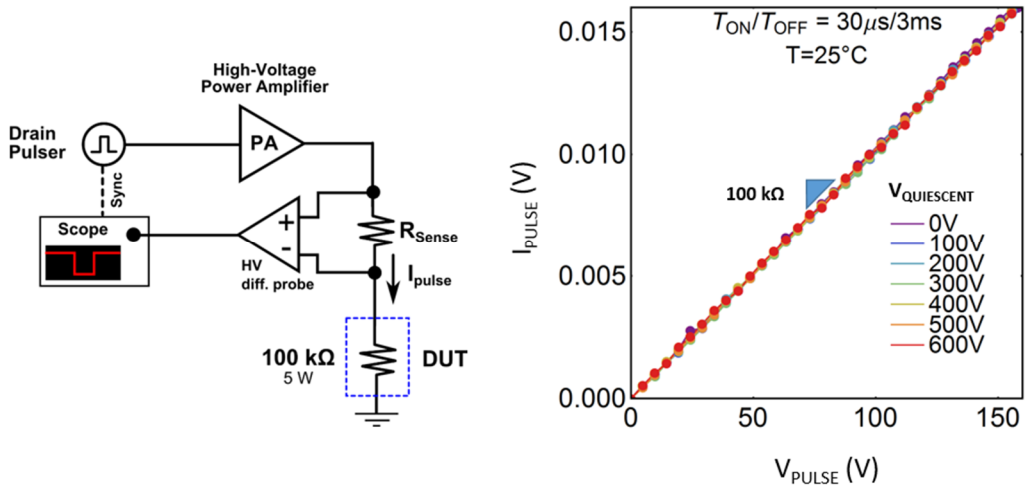



Figure 2-21. Calibration test performed on a high-power 100 kΩ resistor exposed to quiescent bias-point up to 600 V.

## 2.4 On-the-fly Pulsed Measurements

As reported in section 2.2.5, not only the investigation of the detrapping kinetics, but also the investigation of the trapping kinetics can provide useful information on charge-trapping mechanisms and involved defect-states. The charge-trapping kinetics, i.e., what is happening during the stress phase, can be *indirectly* assessed, by carrying out several drain-current transient measurements with different filling-time (as reported in section 2.2.5), or *directly* measured by means of *on-the-fly* pulsed measurements.

The concept "on-the-fly" was introduced in early 2000 to investigate positive- and negative-bias temperature instabilities (PBTI and NBTI) in $Si/SiO_2$ MOS technologies [138]. During the stress phase, the threshold-voltage was in fact assessed *on the fly* by performing quick gate and drain pulses around the stress voltage. This allowed to acquire the time-resolved evolution of threshold-voltage instability during the stress, avoiding parasitic recovery effects which can strongly affect the outcome of the analysis.

In order to comprehensively investigate the charge-trapping phenomena, we implemented an on-the-fly pulsed characterization protocol (Figure 2-22): during the filling-bias (also referred as stress phase), the device under test are repeatedly biased with short pulsed in the on-state, during which the instantaneous $I_D$ is acquired, and related instantaneous $R_{ON}$ or $V_{TH}$ are extrapolated. Then, the stress phase can be followed by a recovery phase, which purposes are the same of the drain-current transient technique: to acquire the recovery of drain current after the filling bias.

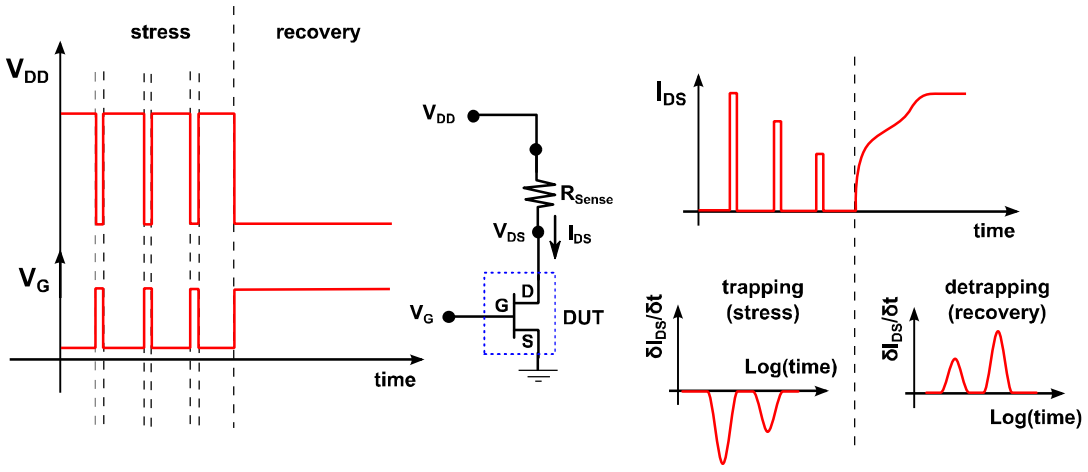



Figure 2-22. On-the-fly pulsed measurement: During the stress-bias, the device under test are repeatedly biased with short pulsed in the on-state, during which the instantaneous $I_D$ is acquired, and related instantaneous $R_{ON}$ or $V_{TH}$ are extrapolated. Then, the stress phase can be followed by a recovery phase, during which the drain current transient is recorded continuously, as in the drain-current transient spectroscopy.

Thanks to the adoption of the on-the-fly technique, we are able to monitor the charge-trapping kinetics (stress), and the charge-detrapping kinetics (recovery). The successful implementation of this technique is reported in Chapter 4.

## 2.5 On surface-related trapping

One of the groundbreaking achievements in the development of GaN-based electronics has been the introduction of the SiN passivation layer on top of the ungated access regions, to prevent surface-related current-collapse effects [89]. Governed by the net polarization charge across the AlGaN barrier, the 2DEG carrier density is dramatically influenced by the charge-state of the traps at the AlGaN surface [139]. When exposed to air, donor-like surface-states are able to capture electrons, neutralizing the net polarization charge and killing the 2DEG carrier concentration. Parasitic electrons can be injected from gate-metal during high-field off-state conditions. Properly understood by Vetury *et al.* [89], this phenomenon has historically referred as "virtual-gate". In the following, we report on the signature of surface-related trapping phenomena on pulsed I-V and drain-current transient spectroscopy.

Devices under test belong to a split experiment wafer fabricated at the University of California, Santa Barbara. The sample was grown by metal-organic chemical vapor deposition (MOCVD) on a silicon carbide substrate. The epitaxial structure consists of a 20 nm $Al_{0.36}Ga_{0.64}N$ barrier layer, a 0.7 nm AlN layer, a 10 nm GaN channel layer, a 1-μm-thick $Al_{0.04}Ga_{0.96}N$ back-barrier layer and a 300 nm $Al_{0.09}Ga_{0.91}N$ layer. Gate length is 1 μm, gate–drain and gate-source distances are equal to 2 μm, and 1 μm, respectively. The split-experiment consisted in having both not-passivated and passivated devices on the same wafer.

When exposed to off-state bias (pulsed measurements in Figure 2-23), not-passivated devices experience an appreciable reduction of the transconductance, and negligible $V_{TH}$-shift: this suggests charge-trapping phenomena in the access regions. Furthermore, since passivated devices feature almost absent dispersion effects (Figure 2-23a), we can confirm that the current-dispersion effects in not-passivated devices can be addressed to surface-related charge-trapping.

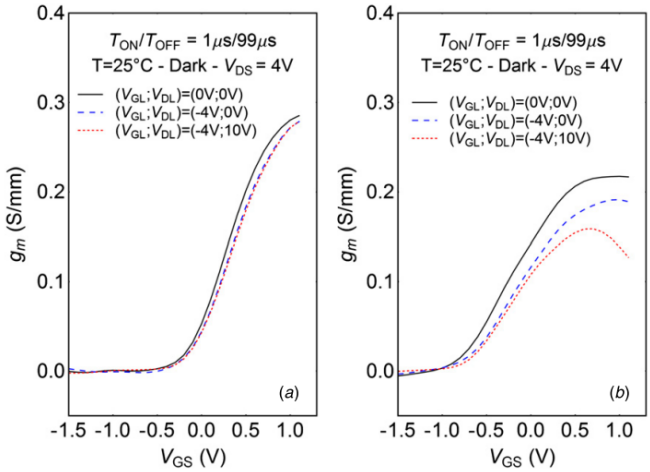



Figure 2-23 Pulsed $g_m$-$V_G$ acquired on *(a)* passivated and *(b)* not-passivated HEMTs. When exposed to off-state quiescent bias-point, not-passivated feature noticeable trasconductance degradation and no $V_{TH}$-shift.

Drain-current transient spectroscopy in Figure 2-24 discloses useful information on surface-traps signature. When the not-passivated HEMTs are switched on after 100 s at the filling bias ($V_{GQ}$;$V_{DQ}$) = (−4V;10V) the drain current features a significant recovery. This recovery is related to the emission of the carriers trapped at the surface of the devices, which determines a gradual reduction of the virtual gate effect responsible for the drain current decrease. The analysis of the de-trapping kinetics indicates that carrier emission is a slow process, with a dominant time constant around 100 ms and that the recovery of current can be fitted by a stretched exponential function with a stretch factor $\beta \approx 0.3$. Both results are consistent with a current-collapse mechanism related to the presence of surface traps [89]. In addition, temperature-dependent measurements indicated that the de-trapping of electrons from surface states is only weakly thermally activated, with an activation energy of 0.99 eV (see the Arrhenius plot in figure 4(b)). The slow de-trapping transients and the low activation energy indicate that thermal emission is not the main mechanism responsible for the release of the electrons trapped at surface states. The emission of the electrons trapped at the surface can be slowed down by other factors: once the device is switched on (after the filling pulse), the trapped electrons leave the surface, possibly via hopping towards the contacts, through the surface, or through trap states [109] [140] [141]. This mechanism may act as a bottleneck for the release of electrons trapped in the gate–drain access region during the de-trapping phase, i.e. when the gate–drain electric field is relatively low: as a consequence, the de-trapping kinetics can be long, and the time constants may have a relatively low temperature dependence.

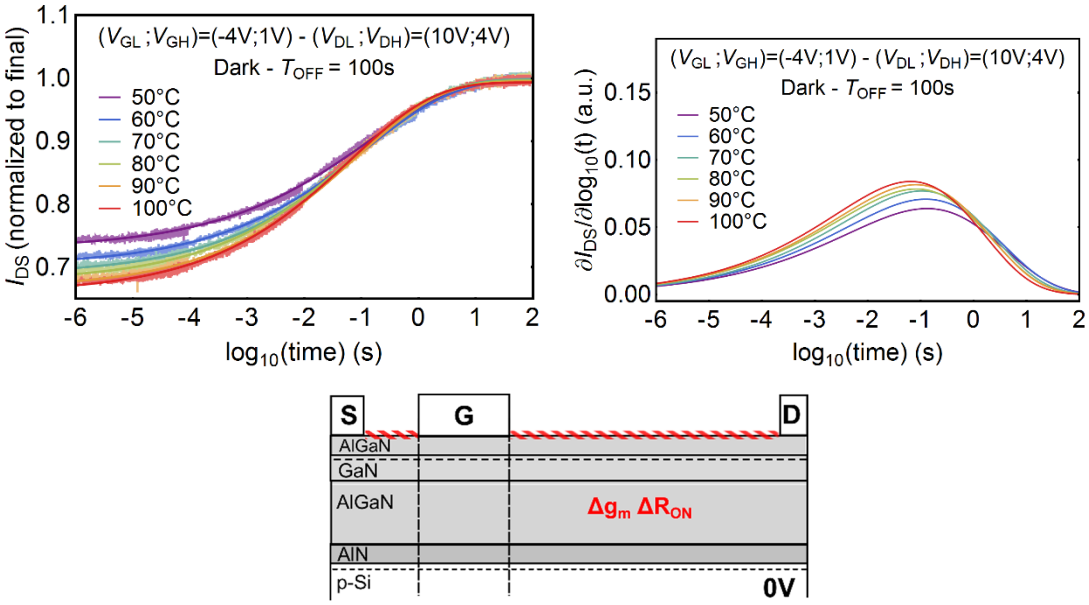



Figure 2-24 *(a)* Drain-current transient and (b) related spectroscopy acquired at multiple temperatures on a not-passivated HEMT. Highly stretched exponential behavior and very low thermal activation suggest that the dominant mechanism governing the detrapping of surface-states and the recovery of pristine electrical performance is not the SRH thermionic-emission but the transport mechanisms from the surface trap-state either towards the gate/drain contacts (by means of surface conduction) or towards the 2DEG (by means of trap-assisted transport mechanisms through the AlGaN barrier).

## 2.6 Capacitance DLTS

During this research program, capacitance deep-level transient spectroscopy (C-DLTS [142]) has also been preliminary investigated. This allowed us to point out agreements and discrepancies between the experimental results from two complementary deep-level spectroscopy techniques (drain-current transient spectroscopy, and capacitance DLTS). In fact, although they are both based on transient analysis, DCTS and C-DLTS rely on different measurement principles, potentially leading to distinct results. Though the DCTS probes the current transients in 3-terminal HEMTs subjected to large-signal swings (tens or even hundreds of Volts), the C-DLTS probes the capacitance transients in 2-terminal diodes subjected to small bias variation (hundreds of mV). For this reason, since different potential distributions, different depletion regions, and different leakage currents are involved, the comparison of the two techniques can reveal further, complementary information on the defect-states nature and location.

For a comprehensive understanding of capacitance DLTS technique, I warmly recommend the reading of [142] and consecutive literature. In this dissertation, I am limiting the description to the measurements parameters employed during our experiments, and a brief interpretation of gathered results.

Devices under test are two-terminal Schottky-gated AlGaN/GaN FATFET diodes packaged in TO-220 cases. C-DLTS measurements have been acquired by means of commercial DLTS system provided by SULA technologies. A box-car acquisition (t1 and t2) with 12 different sampling times (t1 is logarithmically spaced from 20 µs to 100 ms) and with a t2/t1 ratio of 11.5 has been employed. The filling pulse width has been set to 100 ms. The filling-voltage was set to 0 V; whereas the measuring voltage (i.e., the baseline of the pulse) was set close to the $V_{TH}$, where the C-V curve feature the maximum slope.

Figure 2-25 and Figure 2-26 depict the Capacitance-Voltage characteristics, the capacitance-DTLS spectra originating from different acquisition times, and the Arrhenius plot of the detected deep-levels signature, acquired over four different case-studies of AlGaN/GaN heterostructure, similar to those analysed in section 2.1 and 2.2.

A comparison between the deep-level signatures detected by means of drain-current transient spectroscopy and capacitance DLTS is reported in Figure 2-27. As can be noticed, good agreement is found between the signatures identified by the two techniques. The different deep-level have been tentatively categorized and labelled from E1 to E6,

consistently with those reported throughout the dissertation, and tentatively ascribed to electron traps.

Future research activities could be focused on the modelling of the capacitance-voltage profile of AlGaN/GaN heterostructures, understanding how to extract from C-DLTS a quantitative description of trap-state density and related spatial profile.

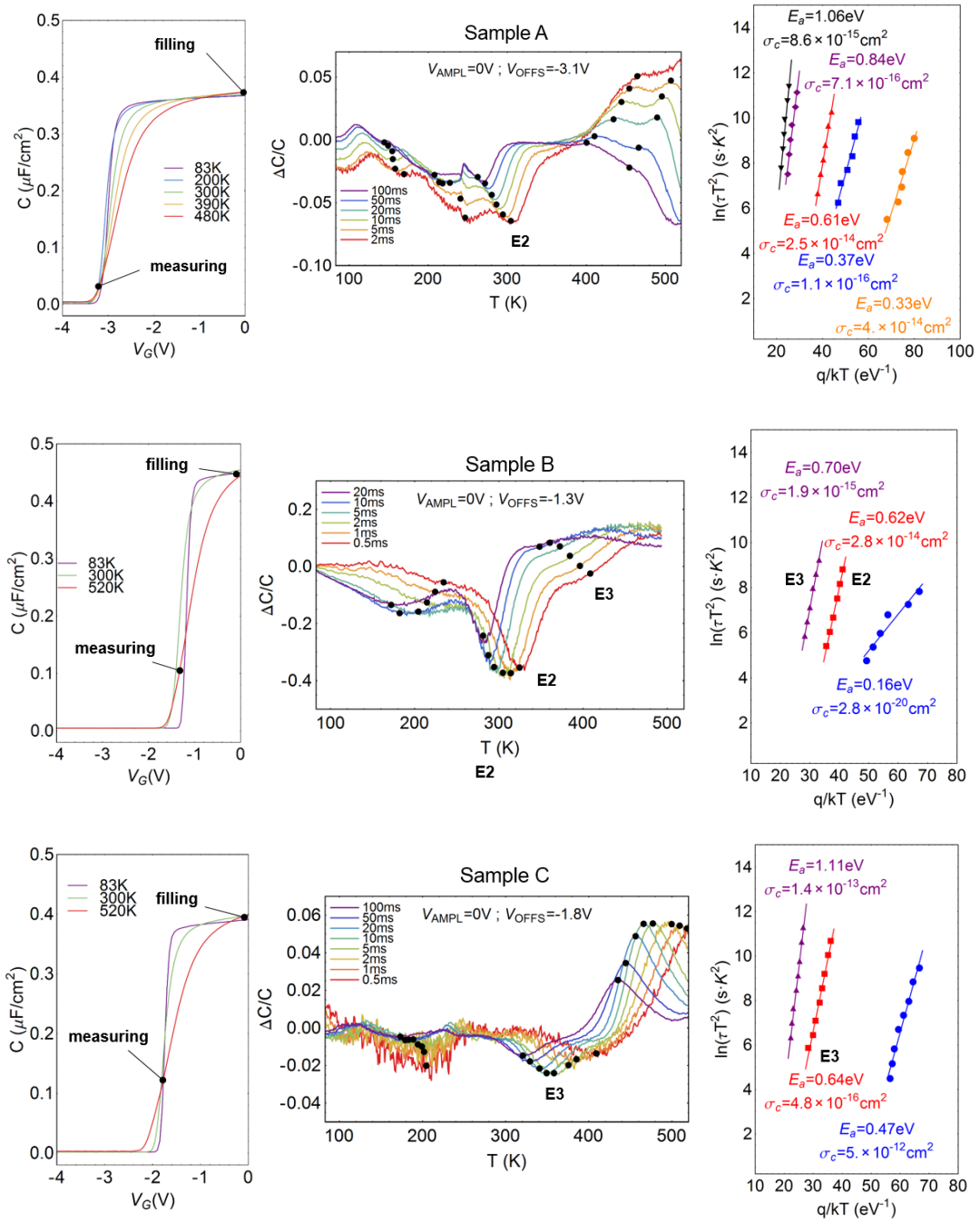



Figure 2-25 Capacitance-Voltage characteristics, the C-DTLS spectra originating from different acquisition times, and the Arrhenius plot of the detected deep-levels signature, acquired over four different case-studies of AlGaN/GaN heterostructure.

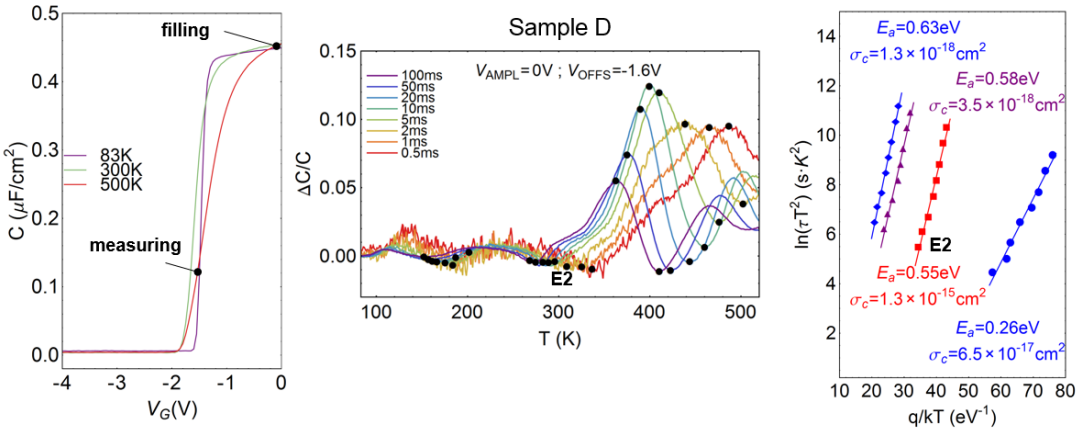



Figure 2-26 Capacitance-Voltage characteristics, the C-DTLS spectra originating from different acquisition times, and the Arrhenius plot of the detected deep-levels signature, acquired over four different case-studies of AlGaN/GaN heterostructure.

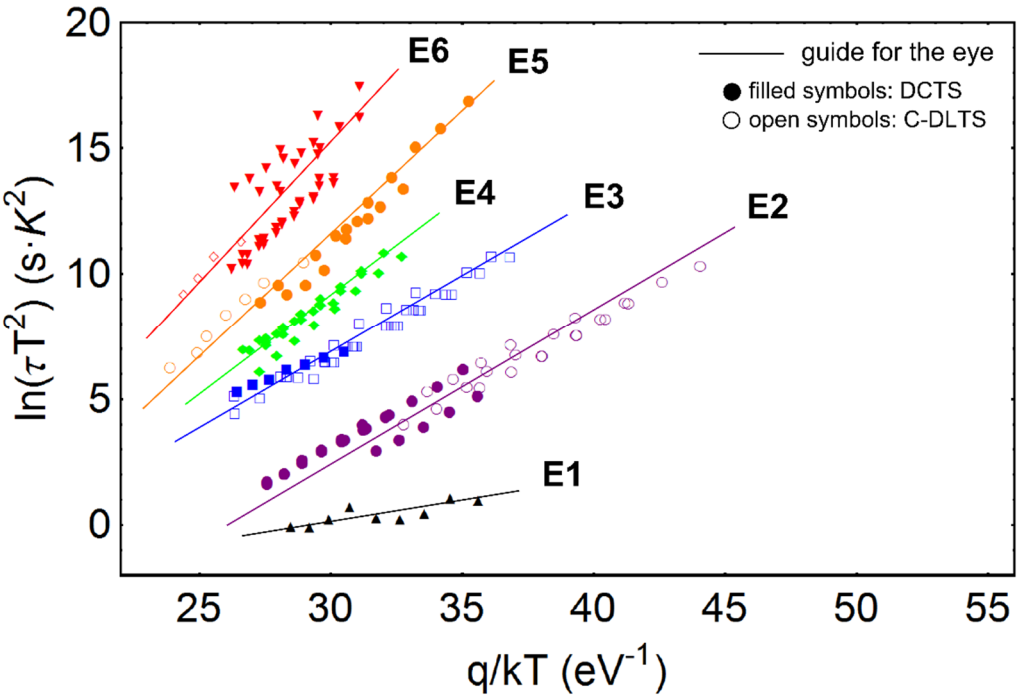



Figure 2-27 comparison between the deep-level signature detected by means of drain-current transient spectroscopy and capacitance DLTS.

# 2.7 Summary

In this chapter, effective techniques devoted to the characterization of current dispersion effects in high-electron mobility transistors have been discussed, including the detailed description of experimental setup, characterization methodologies, and data analysis. In brief:

- Double-pulsed $I_D$-$V_D$ and $I_D$-$V_G$ are effective measurements to quantify the effects of current collapse of GaN-based HEMTs exposed to critical bias conditions, either in the OFF-state and SEMI-ON-state.
- By monitoring the dynamic degradation of threshold-voltage, transconductance, and on-resistance, inferences on the localization charge-trapping mechanisms, and involved technological issues can be drawn.
- The shift of the threshold voltage ($\Delta V_{TH}$) suggests trapping in the intrinsic region of the device, below the gate contact.
- The degradation of the transconductance ($g_m$), strictly related to the degradation of the on-resistance ($R_{ON}$), suggests trapping in the extrinsic, access regions. More in details, a reduction of the $g_{m,peak}$ could be ascribed to trapping in the source-gate access region, whereas the worsening of the $g_{m,droop}$ could be ascribed to trapping in the gate-drain access region.
- More details on the involved deep-trap-levels and related charge (de)trapping mechanisms can be carrier out by means of drain-current transient spectroscopy.
- In order to gather a representative spectroscopy, the measuring bias point should be set in the current-voltage region where the device suffers from the more prominent current dispersion effects.
- By varying the filling bias point, we pointed out the existence of different gate- and drain-dependent charge-trapping mechanisms, which can be triggered in different current-voltage operative regimes. Related implications will be disclosed in Chapter 3 and Chapter 4.
- By performing drain-current transient spectroscopy at multiple temperatures, further inferences on trapping mechanisms involved deep-level can be drawn.
- We observed detrapping processes featuring thermally activated exponential kinetics, likely related to (Al)GaN bulk crystallographic defect-states: good agreement is found among the deep-level signatures (Arrhenius plot, apparent activation energy, and apparent capture cross-section) gathered by means of drain current transient spectroscopy, capacitance DLTS, and previous literature references.

- We also observed detrapping processes (e.g., related trap-states in ungated, and unpassivate AlGaN surface) with highly non-exponential kinetics and/or very low thermal activation energy. In these cases, the detrapping mechanisms is more likely governed by tunneling-, hopping- and/or trap-assisted transport mechanisms, and should be analyzed case by case.
- The investigation of the trapping kinetics by means of filling-time dependence or on-the-fly measurements leads to further information on involved defect-states and related trapping mechanisms. Further details will be disclosed in Chapter 4.
- Charge-trapping could be intimately related to parasitic leakage currents. Besides double-pulsed I-V and drain-current transient spectroscopy, we recommend the detailed monitoring of the leakage current originating from source, gate, and substrate terminals.

The application of the reported methodology is presented in the following chapters, in which we will present the effects of buffer compensation on static, dynamic and reliability performances (chapter 3), and the main mechanisms affecting the dynamic performances of MIS-HEMTs grown on silicon substrate devoted to switching application (chapter 4).

# 3 Impact of buffer doping compensation on the electrical behavior of AlGaN/GaN HEMTs

Among the key technological aspects of AlGaN/GaN HEMTs, the compensation of the unintentional n-type conductivity of the GaN buffer layers (e.g., by means of iron or carbon doping) is of essential importance for the optimization of the 2DEG carrier confinement, the substrate insulation, and the control of the short-channel effects.

Viable solutions involve the introduction of carbon and/or iron compensating species [45] [46], which compensate the unintentional donor species, render the GaN buffer layer semi-insulating, and improve the confinement of electrons in the 2DEG. Nevertheless, the presence of foreign impurities and the related growth conditions may give rise to enhanced crystallographic defect density, and enhanced parasitic charge-trapping phenomena.

Within this chapter, we comprehensively investigate the static and dynamic parasitic effects related to the GaN-buffer design, and we present an analysis of the relevant interplay between compensation strategy, pinch-off properties, and degradation mechanisms in Schottky-gated AlGaN/GaN HEMTs grown on silicon carbide substrate.

## 3.1 Devices under test and experimental details

Devices under test belong to fourteen wafers differing mainly for GaN buffer design. HEMTs were fabricated using the same process steps and layout, with a 0.5 μm Ni/Au gate; they adopt an AlGaN/GaN heterostructure with nominal 25% Al concentration and 23nm AlGaN thickness, with different buffer compensation, including either no doping (type I), $10^{17}$ $cm^{-3}$ C-doping (type II), $10^{17}$ $cm^{-3}$ Fe-doping (type III), or $10^{18}$ $cm^{-3}$ Fe and $10^{18}$ $cm^{-3}$ C co-doping (type IV).

The investigation methodologies include DC, double-pulsed, and Load-Pull characterizations, devoted to the evaluation of static- and dynamic- performances, and Drain-Current Transient Spectroscopy (DCTS), performed to identify the involved deep-trap-levels and related defect-states.

The DC analysis is performed with the semiconductor parameter analyzer Agilent E5260A. The characterization protocol includes the acquisition of the $I_G$-$V_G$, $I_D$-$V_D$ and $I_D$-$V_G$ curves, and the monitoring of the following parameters: saturation current ($I_{DSS}$), threshold voltage ($V_{TH}$), transconductance ($g_m$), reverse-biased gate-leakage current ($I_{G,LEAK}$), off-state source leakage-current ($I_{S,LEAK}$), subthreshold slope (SS), and Drain-Induced-Barrier-Lowering (DIBL). Thanks to static I-V characterization, the gate Schottky junction and related interface-states density (gate-diode I-V, subthreshold slope [143], and $I_{G,LEAK}$), and the insulating properties of the buffer layer (subthreshold region, DIBL and $I_{S,LEAK}$ [144] [145]) can be assessed.

Concerning the dynamic characterization techniques, the double-pulsed I-V analysis allows to investigate the charge-trapping phenomena affecting the electrical parameters, e.g., dynamic $I_{DSS}$ collapse, $R_{ON}$ increase, $V_{TH}$ shift, and $g_m$ droop. Pulsed $I_D$-$V_D$ output characteristic and $I_D$-$V_G$ transfer curve were obtained by pulsing both gate- and drain-terminal from defined quiescent bias points. Pulse width and pulse period are 1 μs and 100 μs, respectively. Pulsed measurements allows to investigate gate-lag and the drain-lag effects, i.e., how the variation of gate- and drain-voltage promote charge (de)trapping processes, affecting the dynamic performances of the devices.

The dominant deep levels involved in current dispersion phenomena have been identified thanks to drain-current transient spectroscopy. By investigating the carrier (de)trapping processes under different biases and temperatures, it is possible to identify not only the current dispersion mechanisms, but also the activation energies and capture cross-sections of the involved deep-levels. As a consequence, the location and the nature of the dominant defect-states responsible for the collapse of dynamic performances can be identified. The inferences on defect-states are supported by auxiliary structural analysis, including secondary ion mass spectrometry (SIMS) and X-ray Diffraction (XRD).

## 3.2 Static I-V analysis

The parasitic conductivity of GaN buffer strongly impact on the subthreshold behaviour of AlGaN/GaN HEMTs. Figure 3-1 shows the $I_G$-$V_G$ and $I_S$-$V_G$ characteristics acquired on four representative samples equipped with unintentionally doped (u.i.d.), $3x10^{17}$ $cm^{-3}$ C-doped, $2x10^{17}$ $cm^{-3}$ Fe-doped, and $10^{18}$ $cm^{-3}$ Fe- and $10^{18}$ $cm^{-3}$ C-doped buffer. Devices equipped with u.i.d. buffer feature remarkable source-to-drain leakage current and high DIBL coefficient, which are proofs of high parasitic buffer conductivity, poor carrier confinement, and poor pinch-off properties. Source-to-drain leakage-current and DIBL effects can be gradually mitigated by the adoption of acceptor-like carbon and iron doping which compensate the spontaneous n-type of u.i.d. buffer [45] [46]. Good subthreshold behaviour is achieved with doping concentration equal to or greater than $10^{18}$ $cm^{-3}$. In the following, the side effects of buffer doping on the dynamic performance of the devices are reported.

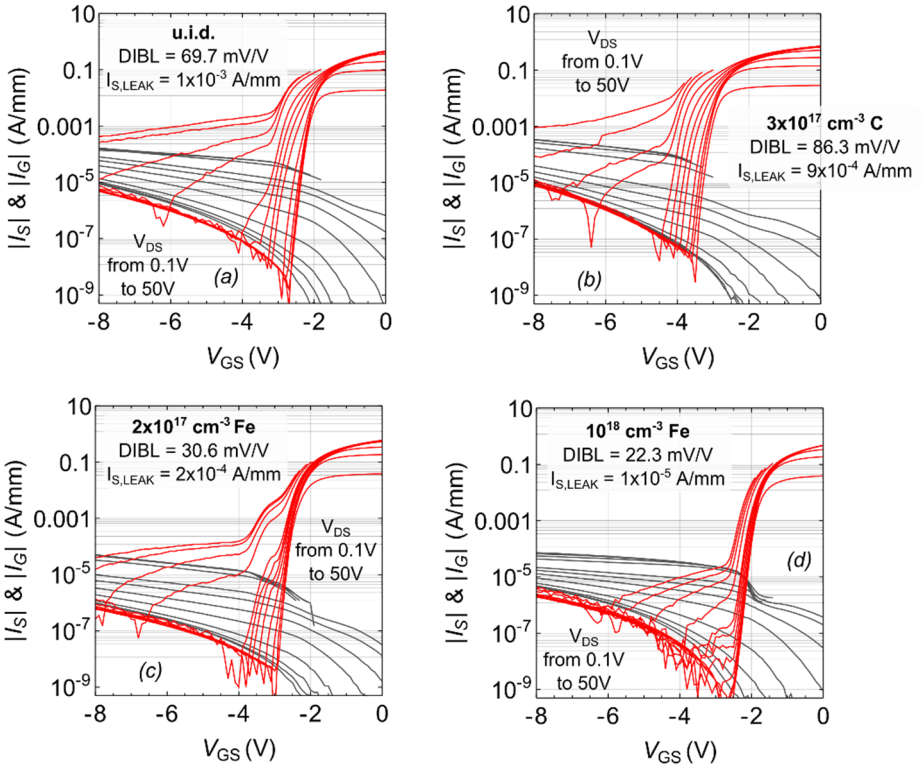



Figure 3-1 Static $I_G$-$V_G$ and $I_S$-$V_G$ characteristics of representative samples equipped with unintentionally doped (u.i.d.), $3x10^{17}$ $cm^{-3}$ C-doped, $2x10^{17}$ $cm^{-3}$ Fe-doped, and $10^{18}$ $cm^{-3}$ Fe- and $10^{18}$ $cm^{-3}$ C-doped buffer. $V_{DS}$ is stepped from 0.1V to 50V. Current compliance has been set at 0.1A/mm to avoid device degradation. Strong subthreshold issues (high source-to-drain leakage-current, and high DIBL effects) are detected in u.i.d. buffer, and are mitigated by the introduction of carbon and iron compensating species. Good subthreshold behaviour is achieved with doping concentration equal to or greater than $10^{18}$ $cm^{-3}$.

## 3.3 Pulsed I-V analysis and drain-current transient spectroscopy

To preliminarily investigate the impact of different buffer-compensation strategies on the dynamic performance of the devices under test, double pulsed $I_D$-$V_D$ measurements have been performed. Dynamic current dispersion has been evaluated in the quiescent bias point ($V_{GQ}$;$V_{DQ}$) = (-6 V;25V). Results reveal that wafers adopting iron- and/or carbon-doped buffer experience, on average, higher current dispersion than those adopting u.i.d. buffer.

In order to identify the roots of enhanced charge-trapping and related current dispersion effects, the devices under test have been submitted to drain current transient spectroscopy. Figure 3-3 depicts drain-current transients performed on representative devices equipped with u.i.d., $3x10^{17}$ $cm^{-3}$ C-doped, and $3x10^{18}$ $cm^{-3}$ Fe- $3x10^{18}$ $cm^{-3}$ C-doped buffer, subjected to 100s-long semi-on-state stress ($V_{GF}$;$V_{DF}$)=($V_{TH}$+0.5V;25V). Distinct electron de-trapping processes can be observed. The related emission rate have been extrapolated by means of stretched exponential fitting. By performing the measurements at different base-plate temperature, we characterized the thermal-activation of detrapping processes, gathering the activation-energy and the apparent capture cross-section of involved deep-levels. The detected deep-levels, labelled E2, E3, E4 and E5 can be mainly ascribed to III-nitride defects. Similar results have been reported in several research works on deep-level transient spectroscopy in (Al)GaN layers [114] [116] [146] [147].

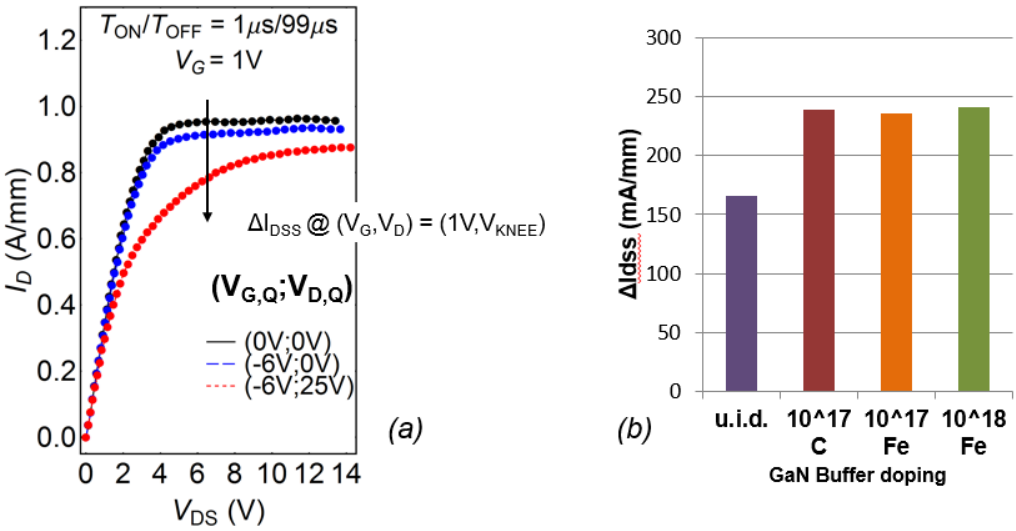
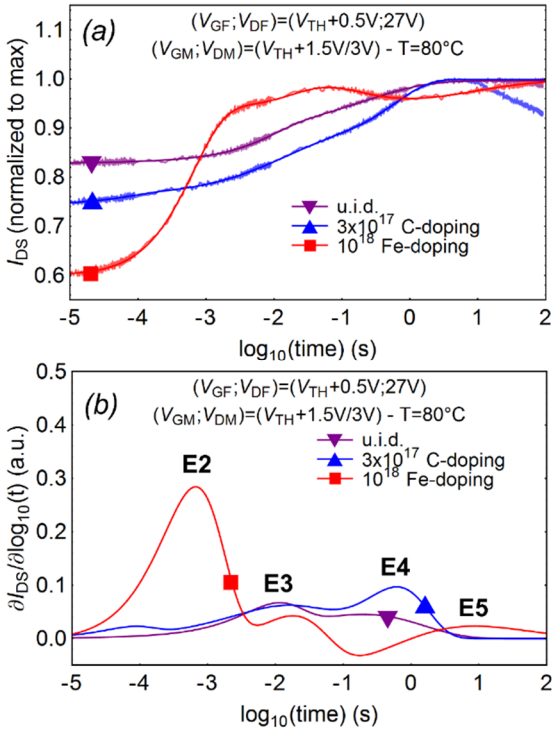
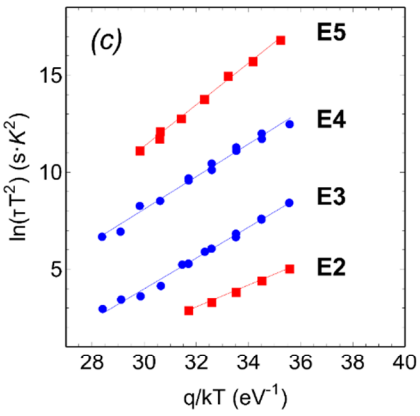



Figure 3-2 *(a)* Representative double-pulse ID-VD measurement, showing the collapse of drain-current when the devices under test are exposed to off-state. *(b)* Wafers adopting iron- and/or carbon-doped buffer experience, on average, higher current dispersion than those adopting u.i.d. buffer.




| Deep-level | E2 | E3 | E4 | E5 |
|---|---|---|---|---|
| **apparent $E_A$ (eV)** | 0.56 | 0.79 | 0.84 | 1.07 |
| **apparent $\sigma_\infty$ (cm²)** | $5x10^{-15}$ | $6x10^{-13}$ | $4x10^{-14}$ | $2x10^{-12}$ |
| apparent concentration in GaN buffer with | | | | |
| **u.i.d.** | / | low | low | / |
| **$3x10^{17}$ C** | / | low | **mid** | / |
| **$10^{18}$ Fe** | **high** | low | / | low |

Figure 3-3 *(a)* Recovery drain-current transients performed on representative devices equipped with u.i.d., $3x10^{17}$ $cm^{-3}$ C-doped, and $3x10^{18}$ $cm^{-3}$ Fe-doped buffer, subjected to 100s-long semi-on-state stress ($V_{GF}$;$V_{DF}$)=($V_{TH}$+0.5V;25V), and (b) related spectroscopy. (c) Thermal-activation of detected deep-levels.

# 3.4 On iron doping

Different research works reported that the iron-doping may be the cause for enhanced current-dispersion effects [148] [149] [128]. By means of secondary ion mass spectrometry, Chini *et al.* [148] claimed the correlation between the iron spatial distribution across SIMS profile and drain current transient amplitudes. Experimental results from [148] have been reproduced in Figure 3-4: though wafer A and wafer B got similar iron-concentration in the deep buffer region (≈$10^{18}$$cm^{-3}$ at 1 µm from 2DEG), they feature different concentration profiles within the channel region: as a result, wafer A exhibits higher iron concentration in the 2DEG proximity and it experiences higher current dispersion phenomena than wafer B.

Consistently with our results, enhanced dispersion-effects are ascribed to enhanced density of the deep-trap-level $E_C$-0.56 eV / $10^{-15}$ $cm^2$, labelled in this thesis as E2. Interestingly, we noted that the trap E2 could not be exclusively ascribed to iron: several scientific papers claim the presence of the E2 in GaN bulk layers and GaN-based devices

grown by means of different techniques, without the intentional introduction of foreign, dopant species [114] [150] [123]. Furthermore, from photoluminescence excitation works reported by Baur *et al.* [74] and Heitz *et al.* [75], the iron should introduce deep-acceptor-levels $E_V$+2.5eV and/or $E_V$+3eV in the GaN band-gap. For these reasons, it could be possible that the trap E2 ($E_C$-0.56eV), mainly detected in iron-doped wafers, would be

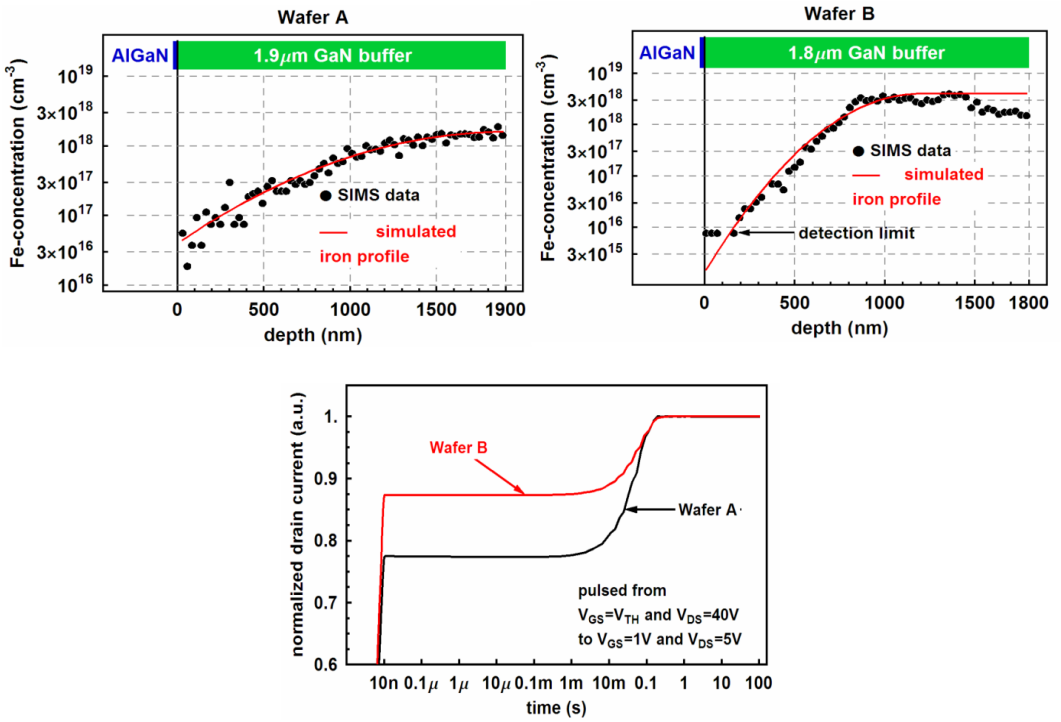
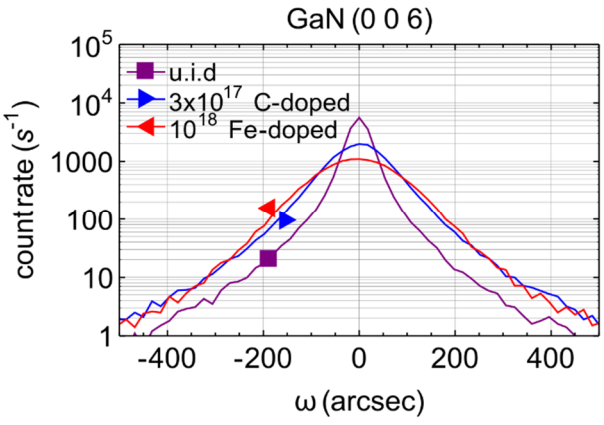



Figure 3-4 From Chini *et al.* [140]: SIMS profile and drain current transient amplitudes of two wafers (A and B) with similar iron-concentration (≈$10^{18}$cm$^{-3}$) in the deep buffer region (>1 µm from 2DEG), but different concentration profiles within the channel region. Higher iron doping in proximity of the 2DEG leads to higher current collapse addressed to E2 deep-levels.




| GaN buffer | (006) ω-scan FWHM (arcsec) |
|---|---|
| u.i.d. | 51 |
| 3x10$^{17}$ cm$^{-3}$ C-doped | 134 |
| 10$^{18}$ cm$^{-3}$ Fe-doped | 190 |

Figure 3-5 X-ray diffraction performed on u.i.d., 3x10$^{17}$ cm$^{-3}$ C-doped, and 3x10$^{18}$ cm$^{-3}$ Fe-doped wafers. The Ω-scan on the (006) GaN reflection, and related Full Width at Half Maximum (FWHM) suggest that doped wafers feature higher dislocation density, hence likely higher electrically active defect-states, than u.i.d. wafers.

not intimately related to the iron atoms themselves, but to native gallium nitride defects, which density increase can be promoted as *side effect* of the iron doping process.

These hypotheses are supported by structural analysis: X-ray diffraction have been performed on wafers equipped with u.i.d., $3x10^{17}$ $cm^{-3}$ C-doped, and $3x10^{18}$ $cm^{-3}$ Fe-doped buffer. Figure 3-5 depicts the Ω-scan, sensible to the dislocation density, on the (006) GaN reflection [151]. Interestingly, doped wafers feature higher Full Width at Half Maximum (FWHM) than u.i.d. wafer. This would suggest that the doping process, either due *(i)* to altered sub-optimal growth conditions, *(ii)* to the introduction of nucleation centres, or *(iii)* to the Fermi-Level effect on the dislocation formation energy, may leads to enhanced dislocation density, and possibly to enhanced electrically-active deep-trap-state density [65]. Rudzinski *et al.* [152] and Mei *et al.* [153] support these inferences by means of SEM, DIC, TEM, AFM and RHEED analyses, reporting enhanced concentration of threading dislocation in iron-doped GaN layers.

## 3.5 On carbon doping

Both donor-like and acceptor-like carbon-related deep-levels in GaN have been predicted. The numerical and experimental evidences for the acceptor level ($E_V$+0.9eV) have been proposed and reported by Lyons *et al.* [71] , Honda *et al.* [154], and by the undersigned and co-workers in [155]. A possible charge-trapping mechanism related to this level is presented in Chapter 4, section 4.2.

On the other hand, experimental evidences of carbon-induced donor-like deep-levels have been provided by Fang *et al.* [156] and Armstrong *et al.* [157]. In the research work presented in this chapter, the deep-level E4 ($E_C$-0.84eV/$4x10^{-14}$ $cm^2$) has been detected, featuring higher amplitude in devices equipped with carbon-doped buffers (see Figure 3-3). For this reason, it could be possible that also the adoption of a non-engineered, non-optimized carbon-based buffer-compensation may give rise to electrically-active deep-levels, and related current-dispersion effects.

Similarly to E2, also the level E4 has been widely observed in unintentionally doped GaN crystals, again suggesting the involvement of gallium-nitride native defects as side effect of carbon doping process. XRD analysis reported in Figure 3-5, reveal that C-doped wafer has higher FWHM than u.i.d. wafer. Higher FWHM in C-doped wafers have also been observed by Wickenden *et al.* [46] and Chen *et al.* [158].

## 3.6 Implication on RF reliability

Long-term reliability of GaN-based HEMT is a key aspect for the successful integration of the promising GaN-based electronics in high-power microwave applications. The characterization of the dominant degradation mechanisms and the identification of the related technological weaknesses play a pivotal role in the implementation of performant and reliable device architecture. During rf operation, GaN HEMT are submitted to the most stressful conditions, involving high current density, high electric fields and high channel temperature. Consequently, reliability evaluation should include rf accelerated testing as an essential part: rf operation can indeed induce failure modes and mechanisms which are not observed during DC or thermal storage tests [159].

In this section, we present an analysis of the relevant interplay between compensation strategy, pinch-off properties, and degradation mechanisms in rf-tested AlGaN/GaN HEMTs.

Before starting rf tests, devices were submitted to load-pull characterization in order to identify optimal matching conditions. Load matching point was chosen as a compromise between maximum output power and PAE. Fresh devices from each wafer were submitted to a 24 h CW rf test at 2.5 GHz with quiescent bias at ($V_{DS}$=30 V, $I_D$=30% $I_{DSS}$) and driven into a 6 dB compression point. Base-plate temperature was set to 40°C. For all tested devices, the estimated channel temperature was 100±20°C; no correlation was found between channel temperature and rf output power degradation. The characterization protocol performed prior to and after the stress tests includes static and pulsed $I_D$-$V_D$ and $I_D$-$V_G$ measurements and Drain Current Transient Spectroscopy (DCTS) [160].

Devices subjected to 24-hours rf test experienced a degradation on the rf output power ($\Delta P_{OUT}$) ranging from -0.05 dBm to -1.1 dBm. From static measurements performed prior to and after the stress, no worsening of the gate leakage current was detected, even in devices with $\Delta P_{OUT}$ = -1 dBm (Figure 3-6a). This suggests that the gate-edge degradation (e.g. caused by converse piezoelectric effects, time dependent breakdown, or electrochemical GaN oxidation [161]) is not the dominant degradation mechanism. Likewise, no correlation has been found between the degradation of rf performances and the variation of the dc parameters, as $I_D$, $g_m$ or $V_{TH}$.

Conversely, the main evidence of device degradation is a significant worsening of the current-collapse, suggesting the worsening of charge-trapping effects. Figure 3-6b shows the pulsed $I_D$-$V_D$ characteristics of a representative device with u.i.d buffer (type I) which experienced a $\Delta P_{OUT}$ of -1 dBm. Though no significant degradation is found in the

reference quiescent-bias point ($V_{G,Q};V_{D,Q}$) = (0V;0V), a remarkable drain-current degradation (-25% at $V_{DS}$ = 4 V) is found in the hot quiescent bias-point ($V_{G,Q};V_{D,Q}$) = ($V_{TH}$+0.5;25V). Figure 3-7 shows the correlation (with a Pearson's correlation coefficient $|r|$ of 0.77) between the increase of current-collapse and the decrease of rf output power among all tested wafers.

By investigating the causes of reported degradation, it has been noticed that the $\Delta P_{OUT}$ is more pronounced in those devices that feature worse pinch-off properties and enhanced short-cannel effects (Figure 3-8). Though featuring similar subthreshold-slope and gate leakage-current, devices grown on u.id. GaN buffer have higher DIBL (69.7 vs 22.3 mV/V) and higher $I_{D,LEAK}$ ($\approx 10^{-3}$ vs $\approx 10^{-5}$ A/mm), and experience higher $P_{OUT}$ degradation (-1.0 vs -0.2 dBm) than devices grown on $10^{18}$ cm$^{-3}$ Fe and C co-doped buffer. An intermediate behavior is shown by devices employing the other types of buffer, leading to a remarkable correlation ($|r|$ = 0.82) between the $\Delta P_{OUT}$ and the initial drain-source leakage (Figure 3-9).

These results provide an evidence on the correlation between hot-electron degradation mechanisms, already observed in GaN-based HEMTs [162] [163] [164], and parasitic

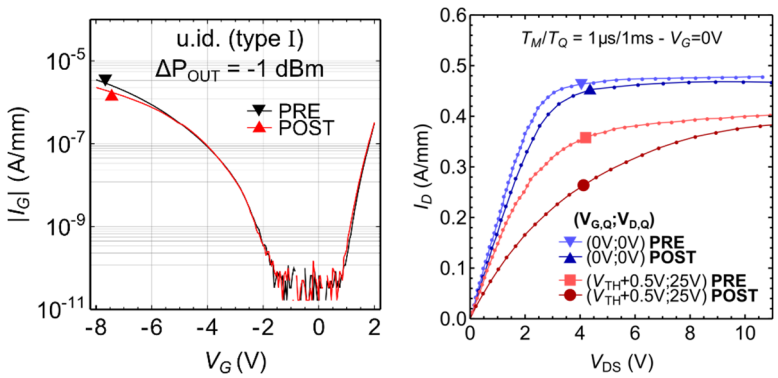



Figure 3-6 *(a)* $I_G$-$V_G$ characteristics and *(b)* pulsed $I_D$ vs $V_{DS}$ characteristics acquired prior to and after the stress of a representative u.i.d. sample experiencing a $\Delta P_{OUT}$ of -1 dBm. No gate-leakage increase and no significant $I_{DSS}$ variation are found. The worsening of the current-collapse is the only relevant evidence of device degradation induced by rf operations.

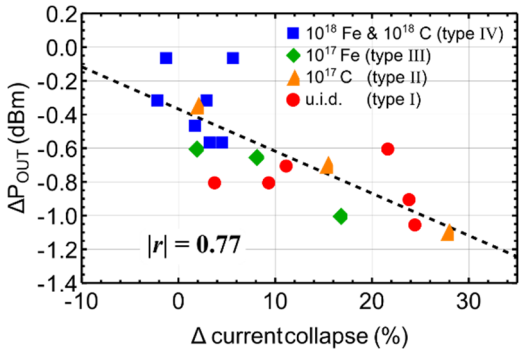
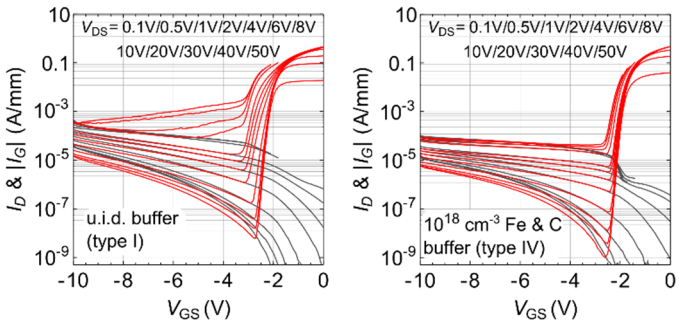



Figure 3-7 Good correlation is verified between $\Delta P_{OUT}$ and the worsening of current-collapse after rf test.

short-channel effects originating from the unintentional conductivity of GaN buffer layers. When devices are driven towards pinch-off, they cross regions of operation characterized by significant current densities and relatively high $V_{DS}$ and electric field magnitude. If parasitic buffer conductivity is present, source-to-drain subthreshold leakage is maintained beyond pinch-off. This could generate an high density of highly energetic carriers (hot-electrons) which can induce defects in the AlGaN and/or in the GaN layers through the direct damage of weak lattice bonds or the dehydrogenation of Ga vacancies or N antisites complexes [163] [62].

More in details, double-pulsed $I_D$ vs $V_{GS}$ characteristics (Figure 3-10 and Figure 3-11) show that the increase of current dispersion after rf testing is due to the generation of additional traps in the access region, as demonstrated by a remarkable dynamic




| | u.i.d. buffer | $10^{18}$ Fe & $10^{18}$ C Buffer |
|---|---|---|
| SS (mV/dec) | 91.2 | 89.2 |
| $\|I_{G,LEAK}\|$ (A/mm) | $6.4\times10^{-5}$ | $2.4\times10^{-5}$ |
| **DIBL (mV/V)** | **69.7** | **22.3** |
| **$I_{D,LEAK}$ (A/mm)** | **$1.2\times10^{-3}$** | **$3.6\times10^{-5}$** |
| **$\Delta P_{OUT}$ (dBm)** | **-1.05** | **-0.55** |

Figure 3-8 $I_D$ vs $V_{GS}$ and $I_G$ vs $V_{GS}$ characteristics measured at multiple $V_{DS}$ (from 0.1V to 50V) for *(a)* u.i.d. buffer and *(b)* $10^{18}$ cm$^{-3}$ Fe-doped buffer HEMTs. *(c)* Devices with u.i.d. GaN buffer feature higher DIBL, higher $I_{D,LEAK}$, and higher $\Delta P_{OUT}$.

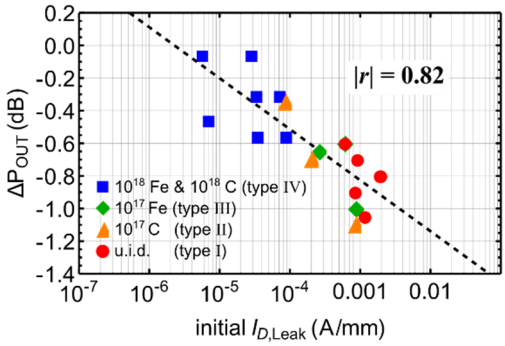



Figure 3-9 Good correlation was verified between initial subthreshold source-to-drain leakage current and rf output power degradation. $I_{D,Leak}$ is defined at ($V_{GS}$; $V_{DS}$)=($V_{TH}$-1V;40V).

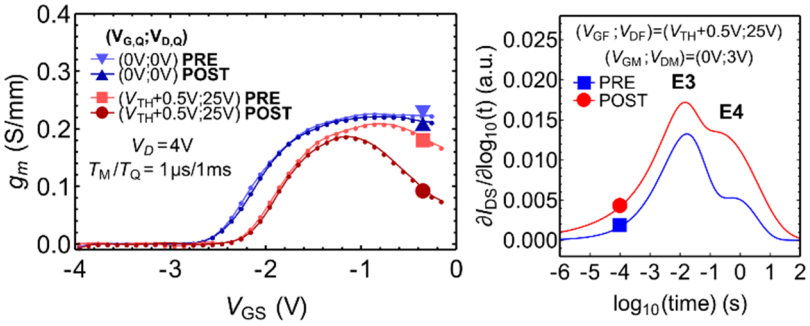



Figure 3-10. *(a)* pulsed $g_m$ vs $V_{GS}$ characteristics and *(b)* DCTS performed prior to and after the rf test on a representative sample experiencing a $\Delta P_{OUT}$ of -1 dBm (type I). Stress induces a remarkable (60%) $g_m$ droop in the hot quiescent bias-point ($V_{TH}$+0.5;25V), with the concentration increase of the pre-existing deep-levels E3 and E4.

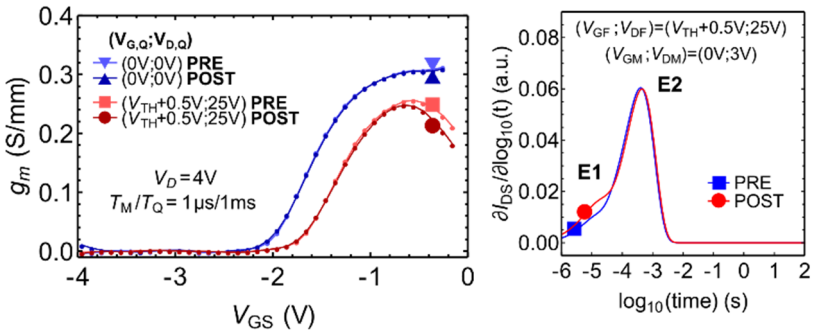



Figure 3-11. *(a)* pulsed $g_m$ vs $V_{GS}$ characteristics and *(b)* DCTS performed prior to and after the rf test on a representative sample experiencing a $\Delta P_{OUT}$ of -0.2 dBm (type IV). After the rf test, only 10% $g_m$ droop is found in the hot quiescent bias-point ($V_{TH}$+0.5;25V), with slight increase of pre-existing trap E1, and no relevant increase of trap E2.

transconductance droop (60%) accompanied by no $V_{TH}$ degradation. The worsening of current-collapse effects is caused by an increase of the concentration of the traps labelled E3 (with $E_A$ = 0.79 eV and $\sigma_c$ = 6x10$^{-13}$ cm$^2$) and E4 ($E_A$ = 0.84 eV; $\sigma_c$ = 4x10$^{-14}$ cm$^2$) detected in u.id. and 10$^{17}$ cm$^{-3}$ C-doped buffer devices, and already observed in GaN [116] [146] [165] or AlGaN [147] epitaxial layers. On the other hand, though devices with 10$^{18}$ cm$^{-3}$ Fe- and 10$^{18}$ cm$^{-3}$ C co-doping feature higher initial current dispersion (which is mainly caused by the iron-related E2 trap, $E_A$ = 0.56 eV; $\sigma_c$ = 5x10$^{-15}$ cm$^2$ [149] [166]), they experience negligible increase of trap density and improved rf reliability.

Concluding this subsection, it worth to be mentioned that we observed the increase of E4 density also in AlGaN/GaN HEMTs exposed to proton irradiation (further details are reported in [167]). This further experimental evidence corroborates the fact that the defect-state related to the trap E4 is potentially unstable and prone to be generated under electrons (as observed in this rf reliability campaign) or proton irradiation (as reported in [167]).

## 3.7 Summary

In this section, we have investigated the impact of buffer doping compensation in AlGaN/GaN HEMTs devoted to microwave applications. Devices employing buffer layer compensated via iron-doping experienced enhanced trapping effects, related to enhanced concentration of the deep-trap-level E2 (0.56 eV / $10^{-15}$ $cm^2$), whereas those compensated via carbon-doping lead to enhanced concentration of the deep-trap-level E4 (0.84 eV / $10^{-14}$ $cm^2$). It worth mentioning that the deep-levels E2 and E4 have been broadly observed in unintentionally doped gallium-nitride crystals, suggesting that the parasitic deep-trap-states may be ascribed not only to carbon and iron impurities, but also to GaN native defects. Their concentration may be enhanced by non-optimal thermodynamic growth conditions during the iron and the carbon incorporation.

Results from RF reliability campaign can be summarized as follows: *(i)* degradation consists of an increase of dynamic current collapse, with consequent degradation of rf performances; *(ii)* no DC degradation is observed, as the permanent degradation of rf power and current collapse is due to the increase of the density of pre-existing deep levels in the gate-drain access region; *(iii)* in particular, the worsening of current collapse effects is caused by an increase of the concentration of trap E3 (0.79 eV / $6x10^{-13}$ $cm^2$) and trap E4, detected in u.id. and $10^{17}$ $cm^{-3}$ C-doped buffer devices; finally *(iv)* a strong correlation has been found between the short-channel effects and subthreshold leakage current in untreated devices and the amount of rf power degradation under rf operation, thus suggesting an enhancement of hot electron effects during rf operation when the dynamic load line reaches deep pinch-off conditions and the devices with poor carrier confinement do not completely turn off. Since this mechanism is enhanced by short-channel effects and by poor carrier confinement, it strongly depends on GaN buffer compensation characteristics.

Finally, the reported methodology, including the monitoring of short-channel and current-collapse effects, can be adopted to provide effective screening parameters for early reliability assessment. In light of reported experimental evidence, we believe that the control of parasitic short-channel effects and parasitic defect-trap-state generation would play a fundamental role in determining the reliability of next-generation, highly scaled ($L_G$ < 0.5 μm) GaN-based high-electron mobility transistors.

# 4 Charge-trapping mechanisms in MIS-HEMTs grown on silicon substrate

Thanks to the physical properties of gallium nitride (GaN), aluminium nitride (AlN) and related alloys (AlGaN), GaN-based HEMTs are suitable not only as power amplifiers in for microwave applications, but also as power switches in energy conversion systems requiring high-voltage ($V_{DS} \geq 600$ V), high-power (> 100 W), high frequency (> 10 MHz), and high temperature ($T_{CH} > 300°C$) operations [168] [32] [169]. Nevertheless, deep-levels originating from threading dislocations, (un)intentional impurities, interfaces, and oxide-defects can degrade both the static and dynamic performance, promoting metastable charge-trapping effects, threshold-voltage instabilities, and ON-resistance increase. In this chapter we present an extensive analysis of the main charge-trapping mechanisms in a double heterostructure AlGaN/GaN MIS-HEMT grown on silicon substrate devoted to power switching applications. By means of static and dynamic measurements we report on *(i)* the physical origin of the charge-trapping mechanisms, *(ii)* the kinetics of the charge capture and emission processes, *(iii)* the nature of involved deep-levels, and *(iv)* the effects of charge-trapping on the dynamic performance of the device during high-voltage and high temperature operations. More specifically, three dominant trapping mechanisms have been identified and described: *(i)* the trapping at buffer defect-states promoted either by high temperature and/or high vertical drain-to-substrate potential, *(ii)* the injection of hot-electrons from the 2DEG into (Al)GaN channel traps promoted during SEMI-ON-state, and *(iii)* the trapping at interface-states or oxide-traps of the gate insulating stack, promoted by forward biased gate conditions.

## 4.1 Devices under test and experimental details

Devices under tests were grown on 150 mm p-type (111) silicon substrate, with a resistivity of 1-10 Ωcm. The epitaxial structure consists of 150 nm thick AlN interlayer, 2 μm thick AlGaN back-barrier composed by three layers with 70%, 40%, and 18% Al concentration respectively, a 150 nm unintentionally doped GaN channel layer, and a 10 nm $Al_{0.25}Ga_{0.75}N$ barrier layer capped by 10 nm in situ $Si_3N_4$. Gate processing includes a 15 nm thick $Al_2O_3$ layer deposited by atomic layer deposition (ALD) [170]. The cleaning procedures before the ALD step include a wet etch with HCl/H2O (1/1) at room temperature and a TMAH-based solution at 65°C. Gate structure features 1-μm-long gate-field-plate. For scientific reasons, these devices do not employ a source-connected field plate.

Charge-trapping effects were investigated by means of complementary pulsed and transient measurements. Double-pulse $I_D$-$V_D$ and $I_D$-$V_G$ characterization have been employed to identify the effects of charge-trapping on the dynamic parameters of the devices when exposed to distinct quiescent (stress) conditions [90]. On the other hand, Drain Current Transient Spectroscopy (DCTS) [160] and on-the-fly pulsed measurements were employed to identify the deep-levels (apparent activation energy and capture cross-section) responsible for charge trapping and detrapping mechanisms.

We investigate the charge-trapping mechanisms triggered during three, relevant operative conditions which cover the entire OFF/ON current-voltage swing. They include *(i)* the OFF-state, featuring high drain-voltage and high vertical field between the channel and the substrate, *(ii)* the SEMI-ON-state, characterized by the combination of high drain-voltage ($V_{DS} > V_{DS,KNEE}$), high longitudinal field, and relatively high source-to-drain current ($I_{DS}$ > 1 mA/mm), and *(iii)* the forward-biased gate condition, characterized by high gate-voltage ($V_G > 0V$).

## 4.2 Positive temperature-dependent buffer-trapping

When subjected to OFF-state bias, the devices under test experience an increase of the dynamic ON-resistance (Figure 1), and no evident threshold voltage shift (Figure 4a). This behaviour suggests the collapse of the 2DEG channel conductivity in the access regions [90]. Since the observed effect is completely recoverable, it can be ascribed to charge-trapping effects. Interestingly, the dynamic $R_{ON}$-increase is worsened if base-plate temperature is raised from 40°C (Figure 4-1a) to 160°C (Figure 4-1b). This positive temperature dependent $R_{ON}$-increase could represent a serious issue for GaN-based electronics, which are supposed to be operated in high-temperature conditions.

To further investigate the nature of this mechanism, time-resolved trapping/detrapping were acquired by means of *on-the-fly* (OTF) pulsed measurements [138]. During 1-ks-long stress-test, the device was repeatedly biased with short pulses in the linear region ($V_G$;$V_{DS}$)=(0V;0.5V) during which the instantaneous $I_{DS}$ is acquired, and the related instantaneous $R_{ON}$ was extrapolated. OTF pulse-width and pulse-period are 50 ms and 1 s, respectively: since involved trap-states feature slow de-trapping kinetics ranging from 1 s to 1 ks (depending on temperature, not shown here), the parasitic 50-ms-long OTF pulses produce no significant recovery effects. Since they have been acquired at different temperatures, the dynamic $R_{ON}$ values have been normalized to the DC values acquired prior to the stress at each temperature (60°C, 80°C, 100°C, 120°C and 140°C), in order to de-embed the temperature-dependent drop of the electron mobility.

Figure 4-2a and Figure 4-2b depict the time-resolved stress/recovery transients performed at multiple temperatures on a device with $L_{GD}$ = 10 µm subjected to an OFF-state stress at ($V_G$;$V_{DS}$;$V_B$)=(-8V;25V;0V). The $R_{ON}$ shows a gradual increase which magnitude ranges

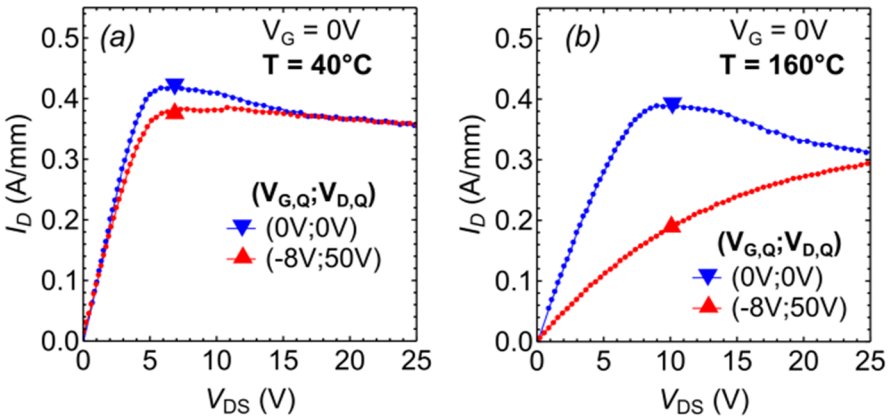



Figure 4-1 Pulsed $I_D$-$V_D$ characteristics acquired at (a) 40°C and (b) 160°C. When exposed to OFF-state quiescent bias ($V_{G,Q}$,$V_{D,Q}$)=(-8V;50V) devices under test experience a (recoverable) increase of the dynamic $R_{ON}$. This effect is strongly temperature-dependent, thus dramatically enhanced during high temperature operations.

from 40% to 80% of the initial value (depending on temperature). The observed process is completely reversible, hence can be fully ascribed to charge-trapping. Both stress and recovery kinetics rely on single exponential law, thus suggesting the involvement of bulk point-defects [68], and are accelerated by temperature. It can be noticed that both the rate (i.e., the inverse of the fitting exponential time constant) of the $R_{ON}$-increase, and the rate of the $R_{ON}$-recovery increases exponentially with temperature. This would explain why, for equivalent timings and voltages (as in the pulsed measurements in Figure 1), the device experiences remarkably higher current-collapse when exposed at higher temperature. $R_{ON}$-increase and $R_{ON}$-recovery have an activation energy of 0.90 eV and 0.95 eV, respectively.

In order to identify the observed charge (de)trapping mechanisms and to address the meaning of their activation energies, auxiliary back-gating measurements were performed. Relying on OFF-state stress only, in fact, the distinction between trapping in the superficial layers (hence ascribable to device processing issues), or trapping in the epitaxial layers (hence ascribable to crystal growth issues) is not straightforward [171]. An effective methodology to overcome this problem is to perform the stress also with *back-gating* biases, by applying a negative potential to the substrate terminal ($V_B$=-25V) and no potential difference between source, gate and drain terminals ($V_G$=$V_D$=$V_S$=0V). Under back-gating, in fact, surface-trapping is supposed to be negligible because no bias is applied between gate and drain terminals, and the formed 2DEG would screen the superficial layers from the field-effect induced by back-gating. In this sense, by means of back-gating stress only the charge-trapping mechanisms happening in the buffer region would be triggered.

Results (Figure 4-2c, and Figure 4-2d) reveal that, in the specific case-study, back-gating leads to the same stress/recovery transients, with the same exponential law, the same timings, and the same thermal activation (Figure 4-3) than those acquired during off-state stress, clearly indicating that *(i)* the observed charge-trapping process is unique, *(ii)* it is localized in the buffer region (Figure 3), *(iii)* it is the dominant mechanism affecting current dispersion during off-state regimes, and *(iv)* it is likely promoted by the vertical drain to substrate potential.

To investigate the implications of vertical charge-trapping mechanism on the design of the gate-drain access region, the $R_{ON}$-increase was characterized in devices featuring different $L_{GD}$. Results, depicted in Figure 4-4, reveal that the $R_{ON}$-increase is logarithmically dependent on $L_{GD}$. Conversely, no remarkable correlation can be found between the $L_{GD}$ and the capture-rate. Corroborating inferences of buffer-trapping induced by vertical electric field, these results suggest that the dominant mechanism

responsible for trapping does not occur in the proximity of the gate (or field-plate) edges, but in an extended area of the gate-drain access-region. Driven by vertical potential, the capture-rate would be independent from longitudinal field, thus independent from $L_{GD}$. On the other hand, the magnitude of the $R_{ON}$-increase relies on the ratio between the area exposed to the vertical field and the total source-to-drain extension, thus increases with $L_{GD}$ [172].

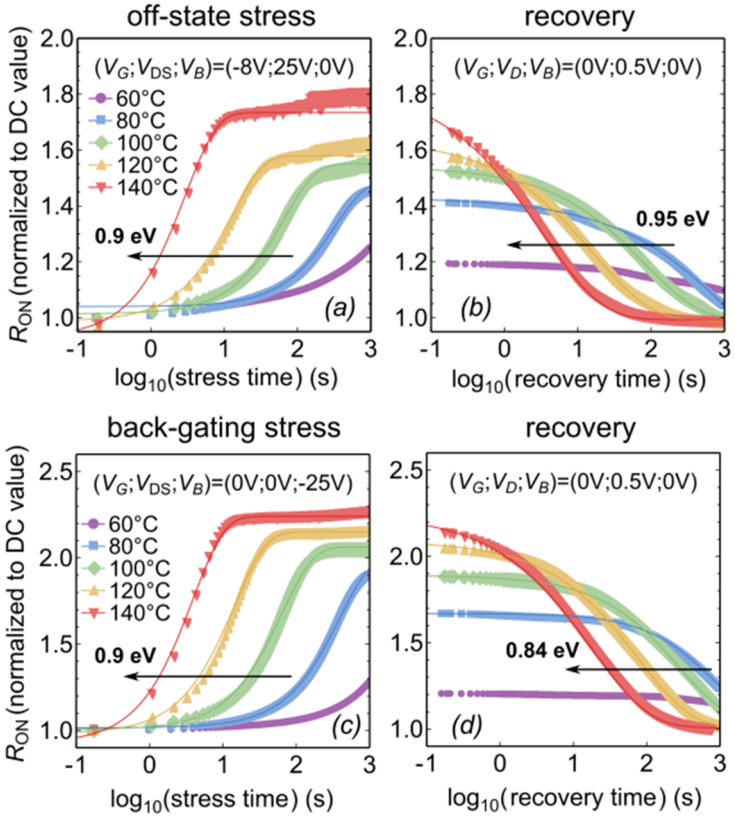



Figure 4-2 Stress and recovery transients performed in OFF-state and back-gating stress, suggesting a unique dominant trapping mechanism, localized in the buffer layers. The activation energies of the stress and recovery kinetics are 0.9 eV and 0.95 eV for the OFF-state stress, and 0.9 eV and 0.84 eV for the back-gating stress.

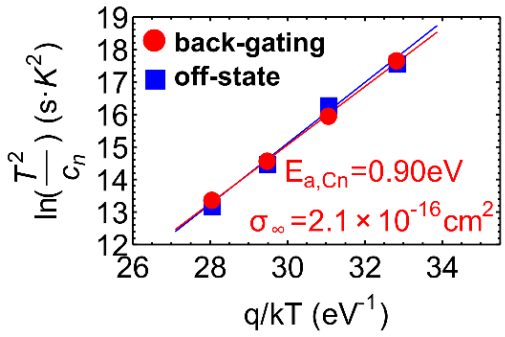



Figure 4-3 Arrhenius-plot showing the same activation energy of the $R_{ON}$-increase process, triggered either by OFF-state or back-gating stress.

As can be noticed from Figure 4-2, the magnitude of the $R_{ON}$-increase during back-gating is higher (up to 120% of DC value) than during OFF-state (up to 80%). This could be explained by the fact that during off-state stress, the high vertical electric-field between the formed 2DEG and the substrate is confined in the gate-drain access region, whereas during back-gating stress, it affects the entire source-to-drain extension.

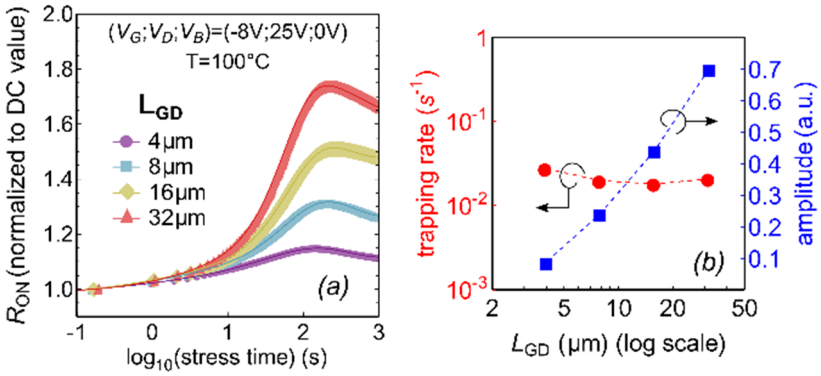



Figure 4-4 *(a)* OTF $R_{ON}$-increase in devices featuring different $L_{GD}$, and *(b)* dependence of the apparent trapping-rate and trapping-amplitude on $L_{GD}$.

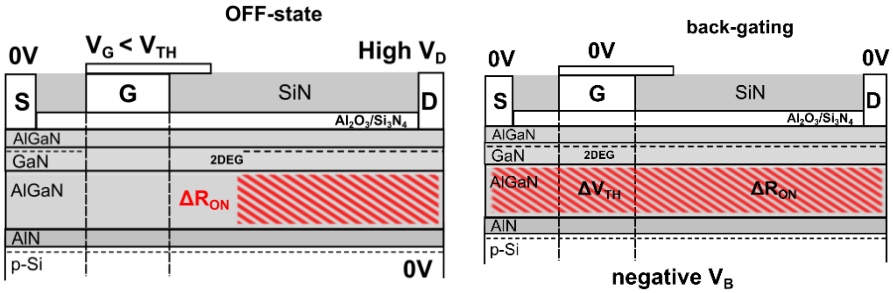



Figure 4-5 During off-state regimes, the dominant charge-trapping mechanism is promoted by vertical drain-to-substrate potential, is localized in the gate-drain access-region within the epitaxial buffer/backbarrier layers, and it causes a temperature- and field-dependent dynamic $R_{ON}$ increase.

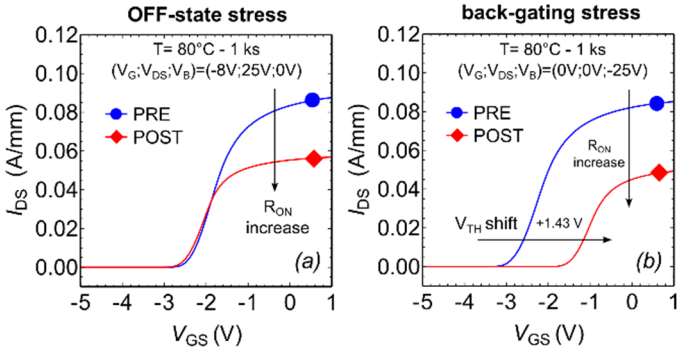



Figure 4-6 $I_D$-$V_G$ characteristics ($V_{DS}$ = 1 V) acquired prior to and after (a) off-state stress and (b) back-gating stress. When exposed to back-gating stress, the device experiences not only the dynamic $R_{ON}$ increase, but also a positive $V_{TH}$ shift of +1.43 V, proving that the buffer charge-trapping happens also within the intrinsic device region, below the gate contact.

Consistently, by performing $I_D$-$V_G$ measurement prior to and after 1-ks-long back-gating stress (Figure 4-6), it can be noticed that the device experienced not only the dynamic $R_{ON}$ increase, but also a positive $V_{TH}$ shift (+1.43 V); hence proving that the buffer charge-trapping promoted by back-gating bias happens also below the gate contact, within the intrinsic device region.

The underlying mechanism for the observed $R_{ON}$-increase can be explained by two different hypothesis: the first one (hypothesis A) considers the presence of electron traps in the buffer and the parasitic injection of electrons from the silicon substrate. In GaN-on-Si technologies, the possible existence of an inversion layer at p-Si/AlN interface [173], and the potentially high defectiveness of the III-nitrides transition- and buffer-layers can compromise the vertical insulation towards the substrate [174]. When the devices are submitted to high drain bias, electrons can be injected from the substrate to the buffer, through the highly defective AlN nucleation layer [174] [175], eventually being trapped in the gate-drain access region. An evidence supporting this scenario is the correlation between capture-rate and substrate leakage-current [176]. Under these assumptions, the activation energy of the $R_{ON}$-increase (0.90 eV) would be the activation energy of the electron-capture process, and would depend on the activation energy of the substrate leakage-current and on the activation-energy of the capture cross-section of the traps [177] [176], whereas the activation energy of the $R_{ON}$-recovery (0.95 eV) would be the activation energy for the electron-emission process, and would account for the thermal emission from the electron-trap-state to the conduction-band ($E_C$-$E_T$).

The second hypothesis (hypothesis B) considers the presence of hole-traps in the buffer. In this case the $R_{ON}$-increase, observed at high drain-voltage, could be explained by the depletion of the buffer, with the subsequent emission of the trapped holes and the net increase of fixed negative charge. In this case, according to the conventional SRH theory, the activation energy of the $R_{ON}$-increase (0.9 eV) would be the activation energy of the hole-emission process, and would account for the thermal emission from hole-trap-state to the valence-band, whereas the activation energy of the $R_{ON}$-recovery (0.95 eV) would be the activation energy of the hole-capture process, and would be governed by the concentration of free-hole, exponentially dependent to ($E_F$-$E_V$).

A likely scenario involving the hole-traps and the mechanisms proposed in the hypothesis B would be the presence of Carbon impurities either in the GaN channel or in the AlGaN buffer, which potentially introduce a deep-acceptor state with energy $E_V$+0.9 eV (hence behaving as hole-trap) as predicted by the first-principles calculations from Lyons *et al.* [71].

## 4.3 Hot-electrons trapping

The OFF/ON switching approach is a key aspect for the design of efficient power converters. Depending on the system specifications (switching loss, frequency, electromagnetic interference, cost, and complexity) either hard- or resonant soft-switching architectures can be designed and implemented. For a successful integration of novel GaN-based electronics, the implications of the OFF/ON switching must be meticulously investigated not only at the circuit level [178] but also at the device level [179]. In fact, during the OFF/ON transitions, the hard-switching load-line trajectories could potentially expose the transistor to critical current-voltage conditions, with the combination of very high voltage and relatively high current levels (Figure 4-13). This may lead to the parasitic generation of highly energetic electrons (hot-electrons) which can promote not only long-term

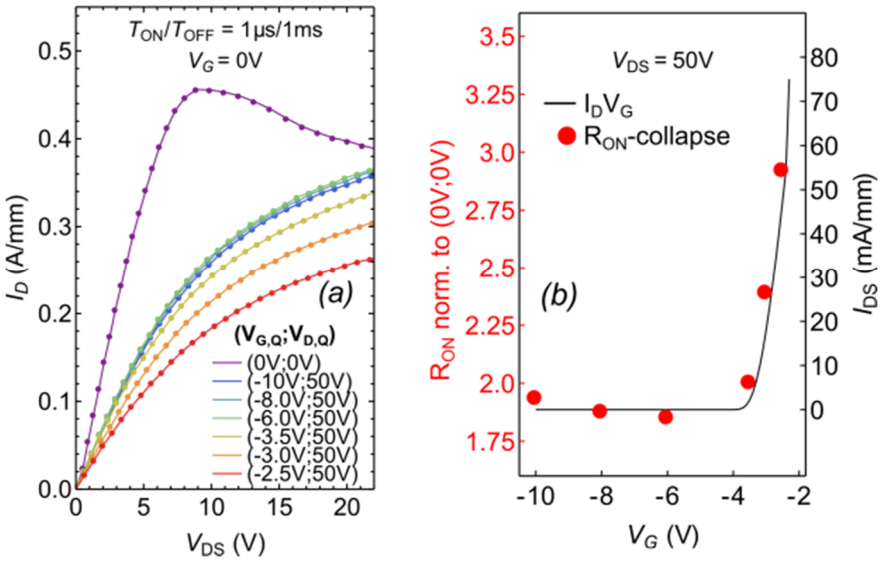



Figure 4-7 (a) Pulsed $I_D$-$V_D$ characteristics acquired with constant quiescent $V_{DS}$, and multiple quiescent $V_G$. Dynamic $R_{ON}$ increase worsen as $V_G > V_{TH}$. (b) Good correlation between $I_{DS}$ and dynamic $R_{ON}$ increase suggesting the influence of hot-electrons-related trapping mechanism.

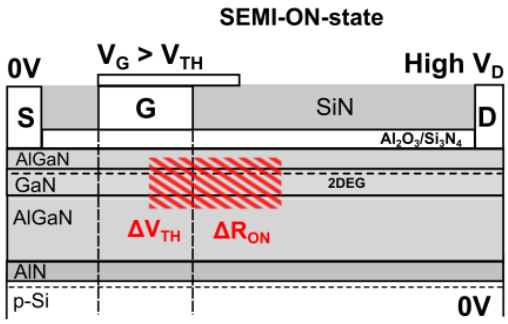



Figure 4-8 During SEMI-ON-state, with the combination of high drain voltage and relatively high drain current, hot-electrons can overcome the 2DEG confinement, being injected and trapped into epitaxial defect-state.

reliability issues [162] [163], but also the instantaneous drop of dynamic performance, caused by enhanced charge-trapping effects [180].

To investigate the influence of hot-electrons on the device performance, multiple pulsed $I_D$-$V_D$ and $I_D$-$V_G$ curves have been acquired by keeping the quiescent drain-voltage ($V_{D,Q}$ = 50 V) constant and by increasing step-by-step the quiescent gate-voltage, from the OFF-state ($V_G = V_{TH}$-6V) to the SEMI-ON-state ($V_{TH}$+2V). As can be noticed from data in Figure 4-7, in addition to the $R_{ON}$-increase promoted by high drain voltage in the OFF-state, a further worsening in the $R_{ON}$ is detected in the SEMI-ON-state, when $V_{G,Q} > V_{TH}$ ($I_{DS} > 1$ A/mm). Remarkably, the $R_{ON}$-increase triggered in the SEMI-ON-state is strongly correlated with drain current density. This suggests the existence of an additional charge-trapping mechanisms, promoted by the combination of high drain voltage *and* high source-to-drain current, hence likely related to hot-electrons.

By means of numerical simulation employing hydrodynamic transport models, Braga *et al.* demonstrated that even with moderated drain voltages (slightly higher than $V_{DS,SAT}$) an appreciable density of electrons (conventionally referred as hot-electrons) can gain

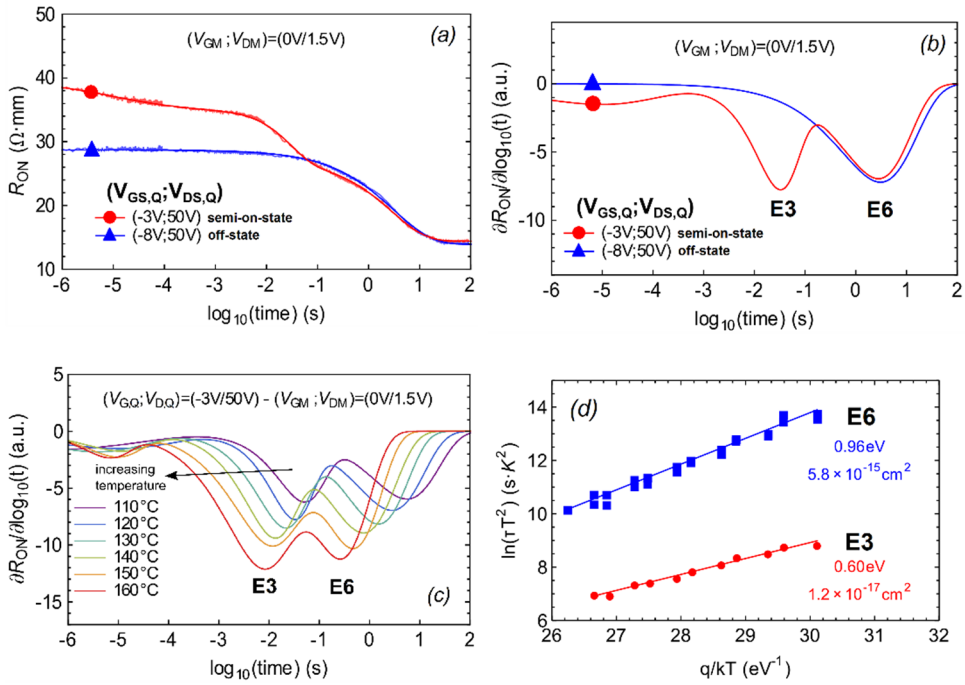



Figure 4-9 (a) Time-resolved $R_{ON}$-recovery transients, and (b) related derivative employed for deep-level spectroscopy acquired after 100s OFF-state and SEMI-ON-state tress. Coherently with pulsed measurements in Figure 4, an additional trap signal (labelled E3) appears after semi-on-stress, evidence of hot-electrons-related trapping mechanism. (c) and (d) thermal activation signatures of trap-state E3 and E6.

enough energy to overcome the 2DEG confinement, being consequently deflected into the epitaxial structure, and getting trapped at crystallographic defect-states [181].

Coherently with the proposed SEMI-ON charge-trapping mechanism, a 400 mV positive $V_{TH}$ shift has been observed in pulsed $I_D$-$V_G$ characteristics (not shown here), indicating that electrons, accelerated by the electric field in the proximity of the gate-edge, get trapped not only in the gate-drain access region, but also underneath the gate contact.

To ensure that the observed phenomenon is not caused only by self-heating effects, and to identify the trap-states responsible for hot-electrons-related charge-trapping mechanisms, drain-current transient spectroscopy has been performed by employing both OFF-state and SEMI-ON-state stress. Since we are focusing on the $R_{ON}$-increase and $R_{ON}$-recovery mechanisms, the drain-current transient have been acquired in the linear region and expressed as $R_{ON}$ transients.

From results, depicted in Figure 4-9a and Figure 4-9b, it can be noticed that besides the trap signal related to the buffer trapping (labelled E6), an additional trap signal (labelled E3) emerges when the device is biased in SEMI-ON-state, clearly indicating the presence of an additional trap mechanism. By performing DCTS at multiple temperatures (Figure 4-9c), the activation energy of the different detrapping processes have been extrapolated. The apparent activation energies and capture cross-sections of trap-state E3 and E6 are 0.60 eV and $1.2\text{x}10^{-17}$ $cm^2$, and 0.96 eV and $5.8\text{x}10^{-15}$ $cm^2$, respectively (Figure 4-9d). According to expectations, the activation energies of E6 detected by DCTS (0.96 eV) is similar to that obtained in OTF measurements (0.95 eV) reported in section 3.1.

Furthermore, it is worth mentioning that besides the parasitic effects on the dynamic performance, high hot-electrons densities may also lead to permanent degradation mechanisms [162] [163]. For this reason, we believe that with respect to the soft-switching, the hard-switching operations, featuring the simultaneous combination of high drain-voltage and high drain-current, may promote not only additional charge-trapping phenomena (as reported in this section) but also more prominent hot-electrons-related long-term degradation effects.

Hot-electrons related charge-trapping mechanisms have been recently reported by Wang *et al.* [182].

## 4.4 Trapping in the dielectric gate stack

The adoption of insulated-gate technology, with the introduction of thin dielectric layer(s) between the (Al)GaN epitaxy and the gate contact, allows a significant reduction of gate leakage current, and provide a viable solution towards the implementation of gate-recessed GaN-HEMT capable for normally-off operations [183]. To date, different dielectric materials, including $SiO_2$, $HfO_2$, $Si_3N_4$ and $Al_2O_3$, deposited on top of the III-nitride epitaxy by means of different techniques, including *ex-situ* atomic layer deposition (ALD), plasma-enhanced ALD (PEALD), plasma enhanced chemical vapour deposition (PECVD), and *in-situ* metalorganic chemical vapour deposition (MOCVD) have been tested and reported [54] [55] [56] [53] [57]. Nevertheless, due to the potential defectiveness of these wide-bandgap dielectrics [184] [79] and the related interfaces with the underlying epitaxy, charge-trapping at interface-, border-, and oxide-traps still remain of great concern for the prospective implementation of GaN-based MIS (or MOS) gate technologies.

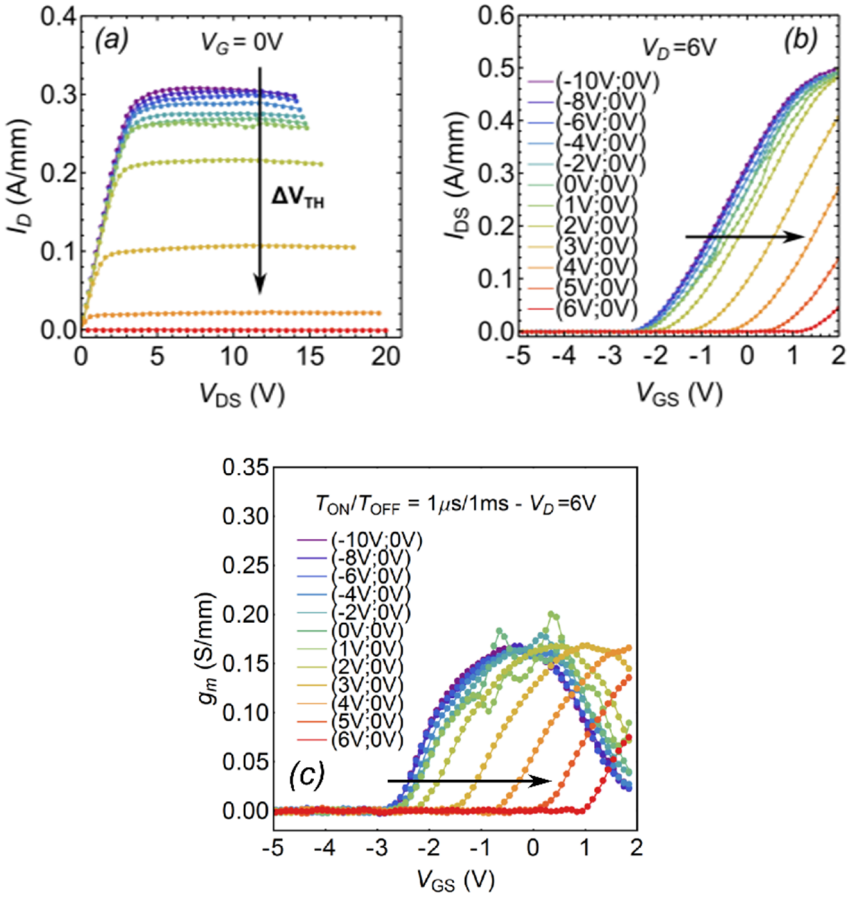



Figure 4-10 Double-pulsed *(a)* $I_D$-$V_D$, *(b)* $I_D$-$V_G$ , and *(c)* derived $g_m$-$V_G$ acquired at multiple quiescent gate-voltage. As $V_G > 0V$, positive $V_{TH}$ shift, and no $g_m$-peak degradation nor $g_m$-droop are observed. Charge trapping happens in the dielectric layers, underneath the gate-contact.

To investigate the effects of oxide traps on the dynamic parameter of the device, pulsed $I_D$-$V_D$ and $I_D$-$V_G$ characteristics have been acquired by keeping a quiescent $V_{DS}$ = 0V, (to avoid any contribution from trapping mechanisms in the epitaxial layers), and sweeping step-by-step the quiescent gate-voltage from deep pinch-off ($V_{TH}$-8V) to strong overdrive ($V_{TH}$+8V). As can be noticed from results (Figure 4-10), a remarkable positive $V_{TH}$ shift ($\Delta V_{TH}$) is triggered for $V_{G,Q} > 0$ V. $\Delta V_{TH}$ approaches +3.5 V in extremely high overdrive condition ($V_G = V_{TH}$+8V). Since no longitudinal driving force is applied, and no $R_{ON}$-increase is detected, the reported experiment suggests that charge trapping related to the positive overdrive happens in the gate dielectric layers, compromising the net charge density within the gate-to-channel stack and the threshold voltage [185]. As can be noticed from Figure 4-10c, the absence of both $g_m$-peak degradation and $g_m$-droop further confirms the absence of charge trapping in the access-regions.

Finally, as reported in Figure 4-11, an interesting correlation emerges between the onset of the positive $V_{TH}$ shift and the onset of the forward-bias gate current. Deserving further

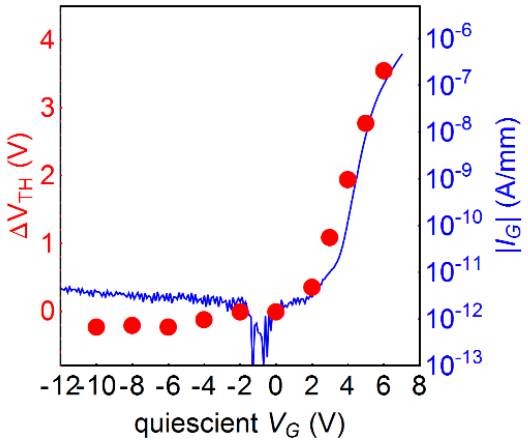



Figure 4-11 Superposition of gate current-voltage (I-V) characteristics, and threshold-voltage shift extracted from pulsed $I_D$-$V_G$ measurements. Strong correlation between $I_G$ and $\Delta V_{TH}$ suggests that the mechanism promoting the charge trapping in the dielectric stack would involve the injection of parasitic electrons from the 2DEG into the dielectric layers, where they can easily get trapped by oxide defect-states.

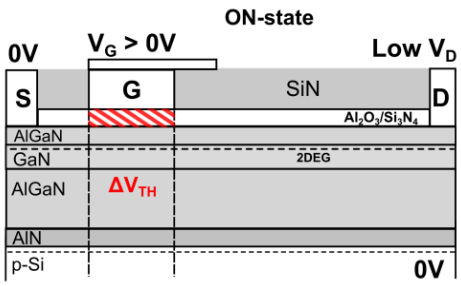



Figure 4-12 During ON-state regimes, with positively biased gate MIS-stack, electrons get trapped into the trap-states of the dielectrics layers (10-nm-thick of in-situ deposited $Si_3N_4$ and 15-nm-thick ALD $Al_2O_3$), leading to metastable $V_{TH}$ instabilities.

investigation, this behaviour may suggest that the mechanism promoting the charge trapping in the dielectric stack would involve the injection of parasitic electrons from the 2DEG into the dielectric layers, where they can easily trapped at bulk- and oxide-traps.

From dynamic threshold-voltage shift, a $D_{it}$ of ~$2x10^{12}$ $cm^{-2}eV^{-1}$ could be estimated. Nevertheless, it is likely that the charge trapping promoting the $V_{TH}$ shift during forward-bias stress may involve not only the interface-states, but also the oxide-states distributed within the dielectric thickness. In the latter case, an oxide-trap density of ~$5x10^{18}$ $cm^{-3}$ would be required. The distinction between interface- and oxide-traps is of great importance for the improvement of the MIS/MOS gate-insulated technologies, and could be achieved by the performance of combined C-V-f and photo-assisted C-V measurements on dedicated MOS test structures [186] [187] [188] [189].

By comparing the evidence of the different trapping mechanism on the dynamic performance of GaN-based MIS-HEMT investigated throughout this work, it is evident that the charge-trapping in the dielectric layers leads to the most severe parasitic effects. As can be noticed in Figure 7a, in fact, metastable $V_{TH}$ instabilities originating from strong gate overdrive ($V_{TH}$+8V) can promote the total current-collapse. In this sense, as historically happened for silicon-based CMOS technologies, the investigation of oxide traps, and the related parasitic transport and charge (de)trapping mechanisms will play a key role in the identification of the optimal dielectric material, and related optimal fabrication techniques [185] [187] [190] [191] [188].

## 4.5 Summary

In this chapter, we have reported on the three dominant trapping mechanisms affecting the dynamic performance in a double-heterostructure GaN-based MIS-HEMT grown on silicon substrate. In the OFF-state, with high drain voltage and pinched-off 2DEG, the unique, relevant mechanism is related to charge-trapping in the gate-drain access region the buffer layers caused by the vertical drain-to-substrate potential. This effect causes the dynamic increase of the ON-resistance, and is positively temperature-dependent, thus being of great concern for high-temperature operations. In the SEMI-ON-state, due to the presence of relatively high $V_{DS}$ and relatively high $I_{DS}$, an additional trapping mechanism emerges, involving the parasitic ejection of hot-electrons from the 2DEG, and their subsequent trapping at epitaxial defect-states. This mechanism affects both the ON-resistance and the $V_{TH}$, and is potentially able to degrade the device performance in hard-switching conditions. Finally, in the ON-state, characterized by low drain-voltage and positively-biased gate contact, trapping of electrons in the gate dielectric-layers results in strong metastable $V_{TH}$ instabilities. This mechanism is critical for applications with strong gate-overdrive. A visual summary of the gathered inferences is reported in Figure 10. The comprehensive understanding of charge-trapping mechanisms, and the awareness of related parasitic effects plays an essential role not only for the design of more effective device structures, but also for the engineering of more efficient circuital architecture, capable for optimized OFF/ON switching transition, which avoid to drive the transistor into critical biases invoking parasitic charge-trapping and the related dynamic performance degradation.

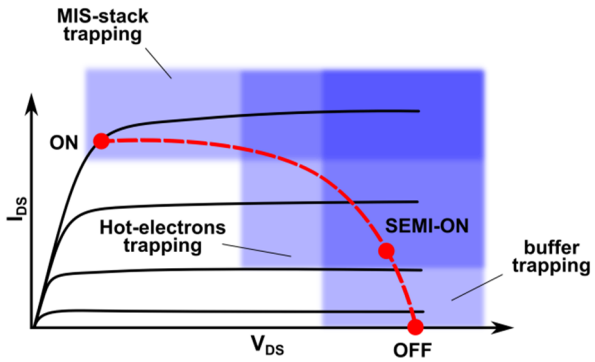



Figure 4-13 Schematic $I_D$-$V_D$ map with the hypothetical superposition of OFF/ON hard-switching transition and the critical biases invoking reported charge-trapping mechanisms. Hot-electrons-related charge-trapping and degradation mechanisms would play a critical role in hard-switching-based architectures.

# 5 Conclusions

In this dissertation, I have reported on charge-trapping phenomena and related parasitic effects in GaN-based HEMTs, discussing the motivation, the characterization methodology, and the main results gathered on state-of-art AlGaN/GaN HEMTs.

The proposed characterization methodology, which combine static and pulsed I-V measurements and drain-current transient spectroscopy, allows to quantify the effects of charge-trapping phenomena on the performance of electron devices under test, to identify the driving forces and the related mechanisms, and to identify the involved deep-trap states and their location within the complex HEMT structure.

During this research program, we have focused our attention on two different device architectures devoted to microwave applications (Chapter 3) and power switching applications (Chapter 4), and we have exposed the devices under test to the complete set of current-voltage regimes experienced during the real life operations: the off-state, featuring high electric-field and the rise of leakage currents, the-semi-on-state, featuring high hot-electrons density, and the on-state, featuring forward gate-current.

Summarizing the gathered results:

- A charge-trapping mechanism promoted by hot-electrons has been identified. This mechanism is critical in semi-on-state, with the combination of relatively high electric-field and relatively high 2DEG current.
- A positive temperature-dependent charge-trapping mechanism localized in the buffer-layer, potentially promoted by the vertical drain to substrate potential has been identified in double heterostructure MIS-HEMT grown on silicon substrate. This mechanism is distributed across the entire gate-drain access region and is critical in high drain-voltage off-state bias in high temperature operations.
- Identification of deep-levels and charge-trapping related to the presence of doping compensation agents (iron and carbon) within the GaN buffer layer.
- A charge-trapping mechanism ascribed to trap-state in the MIS dielectric stack have been identified in MIS-gated HEMTs. This mechanism is promoted in the on-state with positive gate-voltage and positive gate leakage current.
- Identification of a potential charge-trapping mechanism ascribed to reverse gate leakage current in Schottky-gate HEMTs exposed to high-voltage off-state.

- The signature of surface-traps in ungated and unpassivated devices has been characterized by means of drain-current transient spectroscopy. The drain current features a weakly thermally-activated stretched-exponential recovery process.
- A degradation mechanism characterized by the generation of defect-states, the worsening of parasitic charge-trapping effects, and the degradation of rf performance of AlGaN/GaN HEMTs devoted to microwave operations has been observed and documented. The evidence of this degradation mechanism is appreciable only by means of pulsed I-V measurements, whereas no apparent degradation is found by means of DC analysis.

Infographics, summarizing these results, are reported in Figure 5-1, Figure 5-2, and Table 5-1.

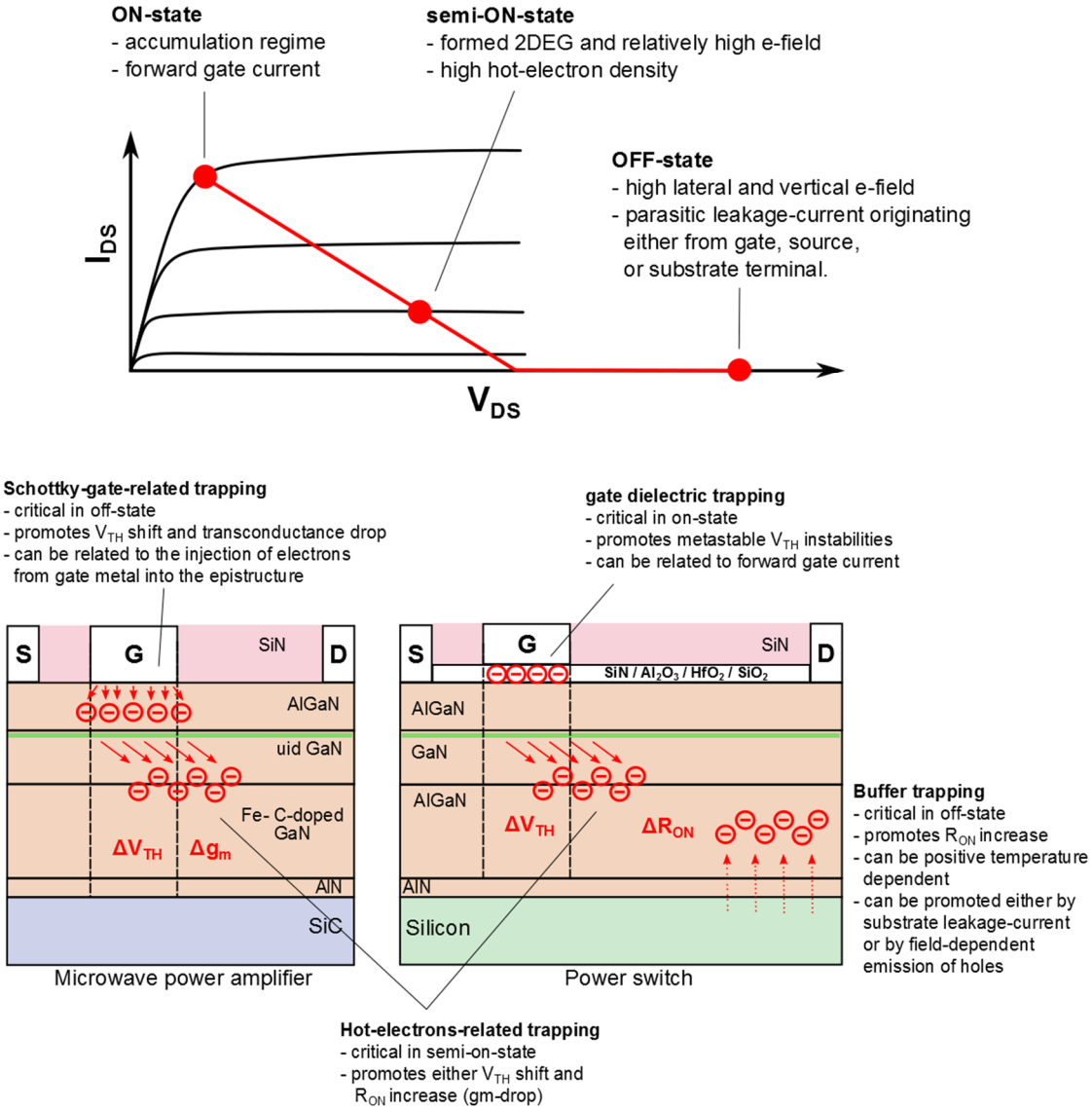



Figure 5-1 Set of investigated operating bias-points, and proposed charge trapping mechanisms.

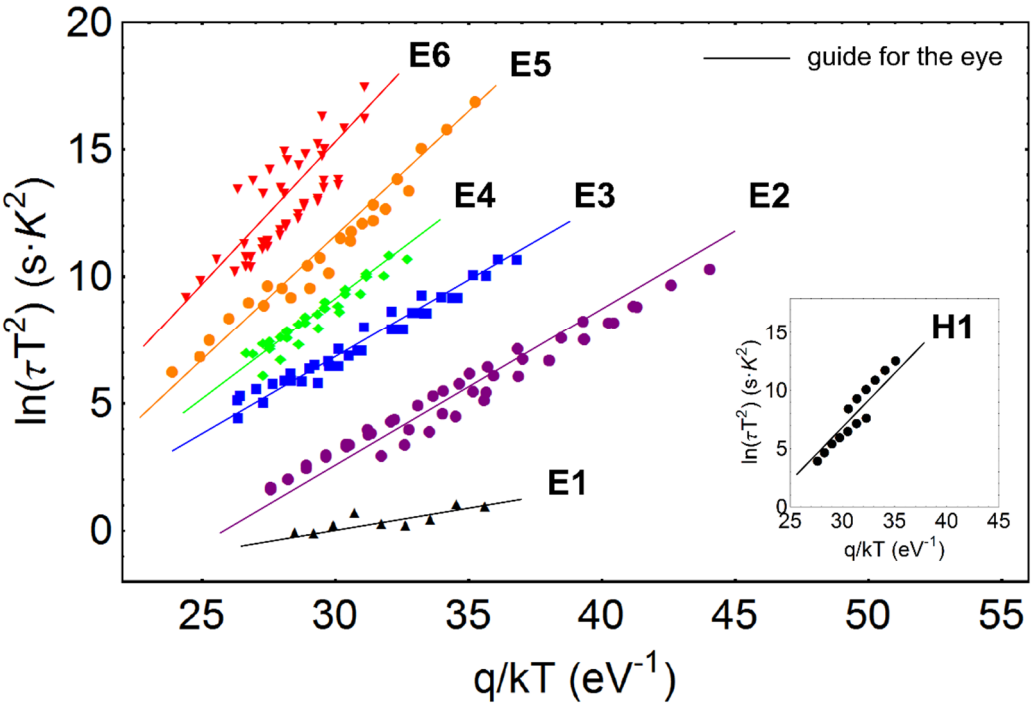



Figure 5-2 Arrhenius plot summarizing deep-level signatures ascribed to defect-state in AlGaN/GaN epitaxy detected in HEMTs under tests.

| | apparent $E_A$ (eV) | apparent $\sigma_c$ ($cm^2$) | comments |
|---|---|---|---|
| **E1** | 0.14 | 8e-20 | • Minor role in current-collapse |
| **E2** | 0.56<br>⋮<br>**0.62** | 5e-15<br>⋮<br>**9e-15** | • Enhanced concentration in iron doped samples.<br>• Most likely located in GaN buffer.<br>• Its filling is promoted during semi-on-state likely by hot-electrons. |
| **E3** | **0.52**<br>⋮<br>0.79 | **3e-17**<br>⋮<br>6e-13 | • Its concentration may increase when the devices are exposed to electrical stress.<br>• Its filling is promoted during semi-on-state likely by hot-electrons. |
| **E4** | **0.80**<br>⋮<br>0.85 | **4e-15**<br>⋮<br>4e-14 | • Enhanced concentration in carbon doped samples<br>• Its concentration increases when the devices are exposed to electrical stress or proton irradiation. |
| **E5** | **0.83**<br>⋮<br>1.10 | **1e-15**<br>⋮<br>4e-12 | • Feature logarithmic filling time dependence.<br>• Tentatively ascribed to extended defects. |
| **E6** | 0.83<br>⋮<br>**0.98** | 7e-18<br>⋮<br>**3e-15** | • Thermally activated trapping kinetics.<br>• Responsible for positive temperature-dependent current collapse, latent at ambient temperature. |
| **H1** | **0.91** | **3e-13** | • Enhanced concentration in carbon doped samples |

Table 5-1 Deep-level signatures ascribed to defect-state in AlGaN/GaN epitaxy detected in HEMTs under tests.

# Pubblications

**Journals**

**2015** **D. Bisi**, M. Meneghini, M. Van Hove, D. Marcon, S. Stoffels, T.-L. Wu, S. Decoutere, G. Meneghesso, E. Zanoni, "Trapping mechanisms in GaN-based MIS-HEMT grown on silicon substrate," *Phys. Status Solidi A*, DOI 10.1002/pssa.201431744.

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*of the Associazione Gruppo Italiano di Elettronica (GE 2013)*, Jun. 2013. **Best Paper Award**

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**2012** A. Chini, V. Di Lecce, F. Soci, **D. Bisi**, A. Stocco, M. Meneghini, A. Gasparotto, G. Meneghesso, E. Zanoni, "Experimental and Numerical Correlation between Current-Collapse and Fe-doping Profiles in GaN HEMTs" in *Proc. IEEE International Reliability Physics Symposium (IRPS 2012)*, April 2012, pp. CD.2.1 - CD.2.4.

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# Appendix A: Timeline of solid-state electronics history

| | | |
|---|---|---|
| 1833 | Empirical observation in silver sulphide of electrical conductivity with positive temperature coefficient, typical of semiconductor materials. | M. Faraday, England |
| 1874 | Discovery of **rectification effects** in lead sulphide crystals (galena) | F. Braun,<br>Würzburg University |
| 1901/<br>1906 | Patents of **cat's whiskers detectors** based on galena or silicon | J. C. Bose, Calcutta,<br>W. Pickard, AT&T |
| 1900s-<br>1930s | Establishment of quantum mechanics, quantum statistics, and modern solid-state physics | Planck, De Broglie, Brillouin, Heisenberg, Schrodinger, Einstein, Bloch, Fermi, Dirac |
| 1920s | Invention of the copper-oxide solid-state rectifier | |
| 1926 | Patent of a **field-effect** electron device | J. E. Lilienfeld |
| 1939 | Modern **theory of crystal rectifiers** | N. F. Mott, University of Bristol<br>W. Schottky, Germany |
| 1940 | Discovery of the silicon **PN junction** | R. Ohl, Bell Labs |
| 1947 | Discovery of the **germanium point-contact transistor** | J. Bardeen and W. Brattain,<br>Bell Labs |
| 1948 | Prediction of the **transistor effect**. Patent of the Bipolar Junction Transistor (**BJT**) | W. Schokley, Bell Labs |
| 1950 | First **grown** junction germanium transistor | W. Schokley, M. Sparks,<br>G. Teal, Bell Labs |
| 1952 | First **alloy** junction transistor | Saby |

| | | |
|---|---|---|
| 1952 | Junction Field-Effect Transistor (**JFET**) | W. Shokley, G. C. Dacey, I. M. Ross, Bell Labs |
| 1954 | First **diffused** junction germanium transistor. $f_t$ > 100MHz | Lee |
| 1954 | First **silicon-based** grown junction transistor | G. Teal, Texas Instruments |
| 1954 | Growth of **GaAs** single crystal by means of Vapor Phase Epitaxy (VPE) or Liquid Phase Epitaxy (LPE) | |
| 1957 | Conception of heterojunction bipolar transistor (**HBT**) and **heterostructures** design principles | H. Kroemer |
| 1958 | First **integrated circuits** | J. Kilby, Texas Instruments, R. Noyce, Fairchild |
| 1960 | **Epitaxial** diffused junction transistor | H. Theuerer, Bell Labs |
| 1960 | Silicon Metal-Oxide-Semiconductor Field-Effect Transistor (**MOSFET**) | M. M. Atalla, D. Kahng, Bell Labs |
| 1963 | Liquid Phase Epitaxy (**LPE**) | Nelson, RCA |
| 1966 | First **gallium-arsenide** Metal-Semiconductor Field-Effect Transistor (**MESFET**) | C. A. Mead, Caltech |
| 1968 | Metalorganic Chemical Vapour Deposition (**MOCVD**) | H. M. Manasevit, W. I. Simpson, Rockwell Corporation |
| 1968 | Molecular Beam Epitaxy (**MBE**) | J. R. Arthur Jr., Bell Labs |
| 1969 | First **GaN** epitaxy by means of Halide Vapor Phase Epitaxy (HVPE) | H. P. Maruska, RCA |
| 1974 | Observation of **quantum size effect** in AlGaAs/GaAs multiquantum wells | R. Dingle, Bell Labs |
| 1976 | Silicon-based Lateral Double-diffused power transistor (**LDMOS**) | J. D. Plummer, Stanford University |

| | | |
|---|---|---|
| 1978 | Discovery of doping modulation in **AlGaAs/GaAs heterostructures** | R. Dingle, Bell Labs |
| 1979 | Invention of the AlGaAs/GaAs High Electron-Mobility Transistor (**HEMT**) | T. Mimura, Fujitsu |
| 1982 | First experiments on III-V HBTs | |
| 1982 | Silicon-based Insulated-Gate Bipolar Transistor (**IGBT**) | B. J. Baliga, General Electric |
| 1982 | First **AlInAs/GaInAs** HEMT on **InP** substrate | K. Y. Chen, Bell Labs |
| 1983 | High quality GaN epitaxy using **AlN buffer** by MBE | S. Yoshida, Electrotechnical Laboratory |
| 1985 | AlGaAs/InGaAs **pseudomorphic**-HEMT | A. Ketterson, University of Illinois |
| 1986 | High quality GaN epitaxy using AlN buffer by MOCVD | H. Amano, Nagoya University |
| 1988 | InAlAs/InGaAs metamorphic-HEMT on GaAs substrate with relaxed InAlAs buffer | |
| 1989 | **p-type Mg-doped GaN** by means of Low-energy electron-beam irradiation (**LEEBI**) | H. Amano, Nagoya University |
| 1991 | p-type Mg-doped GaN using post growth $N_2$ thermal annealing | S. Nakamura, Nichia |
| 1992 | Observation of **2DEG in AlGaN/GaN** heterojuction | M. Asif Khan, Apa Optics Inc. |
| 1993 | First **AlGaN/GaN HEMT** on sapphire | M. Asif Khan, Apa Optics Inc. |
| 1997 | AlGaN/GaN HEMT grown on **SiC substrate** | S.C. Binari, Naval Res. Lab. |
| 2000 | AlGaN/GaN heterostructures on **silicon substrate** | S. Kaiser, Universität Regensburg |

| | | |
|---|---|---|
| 2000 | AlGaN/GaN HEMT grown on bulk **GaN substrate** | M. Asif Khan, University of South Carolina |
| 2000 | First **GaN MOSHEMT** with **PECVD $SiO_2$** | M. Asif Khan, University of South Carolina |
| 2000 | **N-polar GaN** films demonstrated by MBE and MOCVD | P. Guan, A. Zauner |
| 2002 | AlGaN/GaN Current Aperture **Vertical** Electron Transistors (**CAVET**) | I. Ben-Yaacov, UCSB |
| 2003 | First **GaAs MOSFET** with gate oxide grown by Atomic Layer Deposition (**ALD**) | P.D. Ye, Agere Systems |
| 2004<br>2005 | First experiments with **InAlN/GaN** and **InAlGaN/GaN** HEMTs | various |
| 2005 | First **GaN MOSHEMT** with **ALD $Al_2O_3$** as gate dielectric | P.D. Ye, Agere Systems |
| 2005 | ***In-situ*** MOCVD of **$Si_3N_4$** surface layer in AlGaN/GaN HEMTs | J. Derluyn, Imec |
| 2007 | Normally-off AlGaN/GaN Gate Injection Transistor (**GIT**) with p-AlGaN gate | Y. Uemoto, Panasonic |
| 2007 | **N-polar** GaN/AlGaN/GaN HEMTs | UCSB |

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