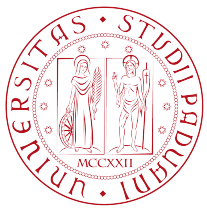

Head Office: Università degli Studi di Padova

Department of Information Engineering

Ph.D. COURSE IN: Information Engineering
CURRICULUM: I.C.T.
CYCLE XXXI

Hybrid DC-DC Converters Combining Charge Pump and Inductor Based Topologies: General Study and an Original Reconfigurable Topology Integrated Implementation

Thesis written with the financial contribution of Infineon Technologies Italia.

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Abstract

The need for reduced size DC-DC converters together with the importance of EMI regulations in the automotive environments is pushing towards DC-DC converters increased integration and magnetic element elimination or at least reduction. In this context this PhD work initially focused on the analysis of existing switched-capacitor converters solutions, providing an extensive analysis and comparison of the most common topologies proposed in literature, detailing the main advantages and drawbacks of the different solutions. After this initial stage, the research work focused on hybrid DC-DC converters combining charge-pump and inductor based topologies, with the goal of overcoming the switched-capacitor converters limitations while also guaranteeing reduced magnetic element requirements and/or switches voltage stress if compared to standard inductor based solutions. With this goal in mind some interesting topologies proposed in literature were analysed and used as a starting point to develop a number of novel solutions. Some of these solutions were also implemented and tested experimentally to demonstrate their feasibility and study their properties in a practical real-world scenario. A great deal of work was carried out in inventing and designing a topology combining reconfigurability with hybridization to yield buck-boost capability, wide conversion ratios and reduced magnetic element requirements. Starting from this novel solution, an integrated hybrid step-up DC-DC converter was implemented to demonstrate the topology hybrid modes operation. Overall this PhD work shows that hybrid converters are an interesting solution where full output voltage regulation or wide conversion ratios ranges are requested. These converters are also particularly interesting as a mean of obtaining high-gain topologies, that could be useful also in application fields different from automotive lighting.

This PhD work was sponsored by Infineon Technologies Italia.

Contents

Chapter 1

Introduction and Study Framework

In recent years LED devices have seen a steady rise in usage, not only in consumer but in industrial applications too. Also in the automotive environment, LEDs are becoming the preferred choice not only for high-end cars, but also for the less expensive ones. This widespread use, together with the continued push towards size reduction and the harsh requirements in term of efficiency and reliability in the automotive environment are fuelling the research of possible new DC-DC LED drivers solutions. Given this premise, this work first focused on the study of the state-of the art solutions for DC-DC converters for LED lighting applications in automotive environment.

1.0.1 Automotive LED Lighting Applications and State-of the Art Solutions

Automotive LED drivers cover a range of diverse specific applications, with different specifications (some examples are shown in table 1.1); anyway, the two major application areas are rear and front-lighting.
In the rear lighting case, where lower power is needed, the preferred solutions, thanks to their low cost, are still linear current regulators or even simple current-limiting resistors; the only exception is the case of OLED-based lamps, in which DC-DC converters are the preferred solution. Nevertheless, continuous push towards CO_2 emissions reduction is increasing the importance of efficiency even for the rear-lighting applications; therefore, a

	I_{LED} $[mA]$	$V_{LED\,max}$ $[V]$
Turn Indicator	140	30
Fog Lamp	500	10
Rear Light	100	30
High Beam	1500	20
Low Beam	1500	10
Daytime Running Light	350	60

Table 1.1: Examples of automotive LED lighting applications and approximate corresponding current and voltage levels.

strong interest in developing cost-effective low-power drivers with improved efficiency exists. In front-lighting applications instead, DC-DC converters are in most cases the preferred solution. Furthermore, it is important to notice that LED lamps are also used as a design feature, therefore load configuration flexibility and good dynamic performance is requested. One example of this is the use of animations in turn indicators, or the use of a LED-matrix based approach for high-beam lamps, allowing shadowing of incoming vehicles by dynamically turning ON and OFF the different single LEDs. These requirements, together with the wide battery functional voltage range (as it will be shown later), make buck-boost capability mandatory.

At the moment, there is not a single preferred choice for LED driving in automotive environment, but different solutions are used based on the requested output power together with EMC and cost/size considerations. One of the main solutions employed is the four-switches buck-boost (Fig.1.0.1). This solution allows to choose the optimum operating mode (buck, buck-boost or boost) depending on the requested conversion ratio, yielding efficiencies higher than 90% for an output power up to 100W.

Furthermore, the so-called "boost to battery" solution is also employed (Fig.1.0.2); this is simply a boost converter in which the load is connected in between the output and input node (the battery positive pole), implementing in practice a standard buck-boost converter. This solution is used for lower output power levels (typically up to 35W) and yields efficiencies in between 70 and 90%.

Another topology currently employed is the SEPIC converter (Fig.1.0.3). Even in this case the maximum target output power is about 35W; efficiencies

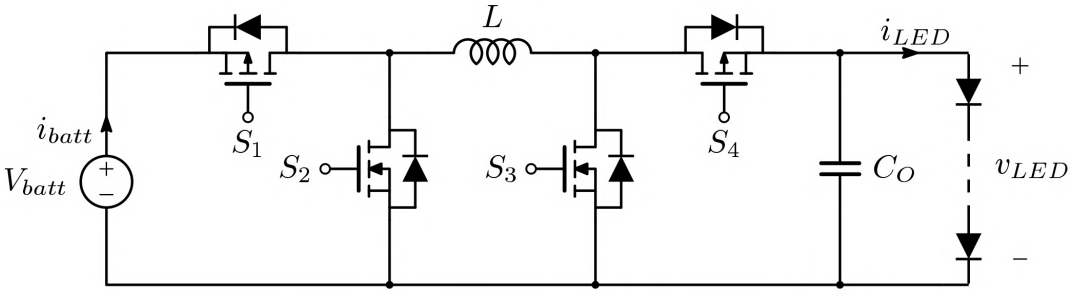


Figure 1.0.1: Automotive LED lighting state-of-the-art solutions: four-switches buck-boost.

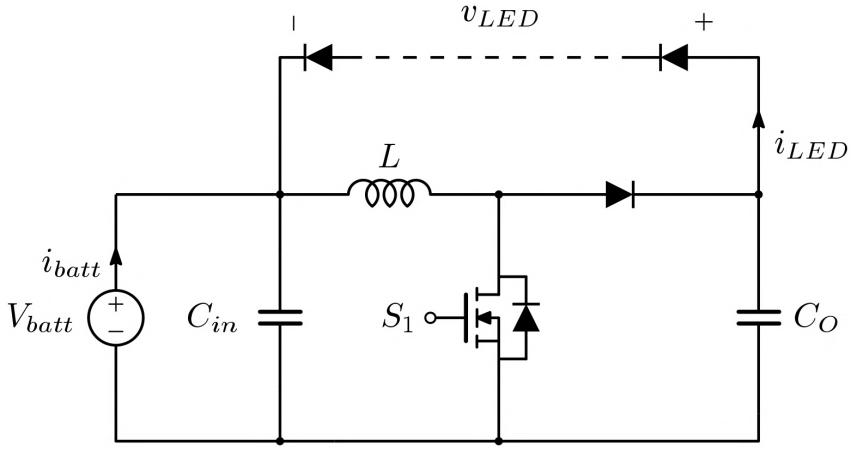


Figure 1.0.2: Automotive LED lighting state-of-the-art solutions: the so called "boost to battery".

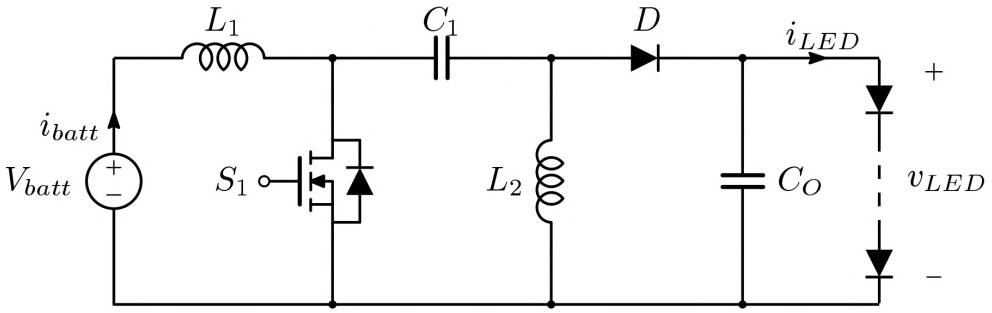


Figure 1.0.3: Automotive LED lighting state-of-the-art solutions: SEPIC converter.

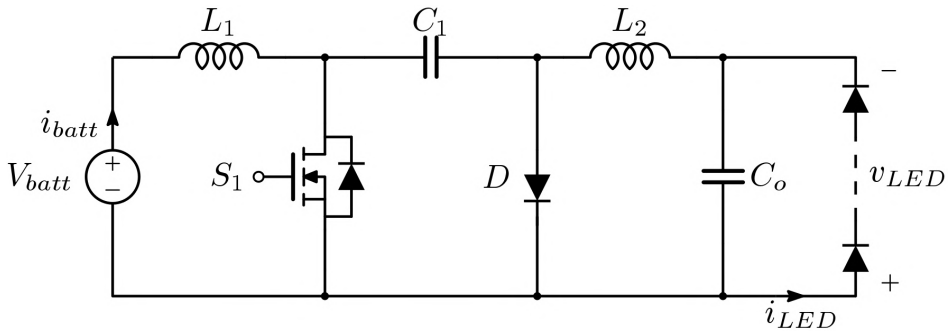


Figure 1.0.4: Automotive LED lighting state-of-the-art solutions: Čuk converter.

obtained using this converter are in the 70÷90% range.

Another topology currently employed is the Čuk converter (Fig.1.0.4). This topology has the advantage of good EMC properties, due to having one input and one output inductor; this characteristic, however, also gives a size drawback.

The most used solution anyway, is the so called "intermediate voltage" technique. This is simply the use of a battery-connected boost converter to generate a constant 60V voltage that is then used as an input for different standard buck converters that handle the various loads. This solution typically guarantees efficiencies around 90% and can provide an output power typically up to 65W.

1.0.2 Battery Voltage Specifications and Other Requirements

The automotive environment is characterized by extended functional ranges; based on AEC-Q100 for example, the temperature functional range goes from -40 to 125°C for grade 1 qualified devices and from -40 to 150°C for grade 0 qualified devices (the requested grade varies depending on the device function and position inside the vehicle). Harsh requirements are also in place with regards to reliability and electronics is also often required to provide some fault-protection functionality and diagnostics. In our case, while studying the automotive environment criticalities, special attention must be given to the battery voltage specifications. In 12V systems in fact, the battery functional range goes from 6 to 18V, meaning that the LED drivers must guarantee full functionality with input voltage variations in that range. Furthermore, the converter must protect the load in an even wider input voltage range; a number of over and undervoltage variations must in fact be considered, as reported in automotive standards for product validation. Some examples of these requirements are given by the standard LV124 for 12V systems.
One example is the so called "jump-start" test, simulating an external starting of the vehicle. According to the LV124 standard (defined by the major car manufacturers to complement the ISO-7637 ans ISO-16750 regulations), in this case the electronic device must withstand an increase of the battery voltage up to 27V for 300ms. Despite functionality preservation not being requested, the converter must still protect the load avoiding any failure, and it must also automatically recover functionality when the stress is over. The same battery overvoltage value is reached during the so-called "low-jump" test. The pulse duration is the same as in the previous case, even though the applied waveforms is different (since the scope of this work is not the study of specific industry-related standards, the two test waveforms are not reported here). This test simulates the dumping of an electric load that, in combination with a battery with reduced buffering capability, results in an energy-rich overvoltage pulse. Also in this case survivability and functionality recovery when the stress is over are requested. The so-called "cold-start" is instead an example of undervoltage test. In this case in fact, the battery voltage drops to 3V for about 18ms; after that it slowly increases back into the functional range. This test simulates the vehicle engine turn-ON. Even in this case survivability and functionality recovery when the stress is over is requested.

1.0.3 Resume

All these considerations, together with the ones regarding the automotive LED lighting loads, make the use of a buck-boost capable topology mandatory. Moreover, in order to satisfy all the different requirements regarding the battery voltage variations, a wide conversion ratios range is also requested. It must also be noted that, with the current push towards car connectivity improvement and the increased importance given to infotainment systems, a steady rise in the number of electronics devices embedded in cars must be expected in the near future. Therefore, reduction of size and weight of the electronics devices and supplies is a critical goal for the future of automotive too.
Due to this reason and under Infineon Technologies suggestion (Infineon Technologies was the industrial sponsor for this project), the research work took switched-capacitor converters as the starting point. These converters in fact, as it will be shown in the next chapter, are very integration-friendly due to their lack of magnetic elements, potentially allowing to move the system complexity from the circuit to the silicon level.

Chapter 2

Switched Capacitor Converters

Switched Capacitor Converters Properties

2.1 Switched Capacitor Converters Basic Characteristics

A switched capacitor converter (SCC) is a network of electronic switches and capacitors that operates off an input voltage and delivers power to a load. These converters are typically operated between two non-overlapping switching phases, that correspond to two different sub-topologies. In the following their main characteristics will be studied making some basic hypothesis and approximations:

- Steady-state operation
- Continuously varying state variables
- Output voltage peak to peak ripple much smaller than its DC value: $\frac{\Delta v_o}{V_o} \ll 1$

2.1.1 The 1:1 Cell

To better understand SCC properties, a very simple practical example can be considered. In Fig.2.1.1 a one to one switched capacitor converter is

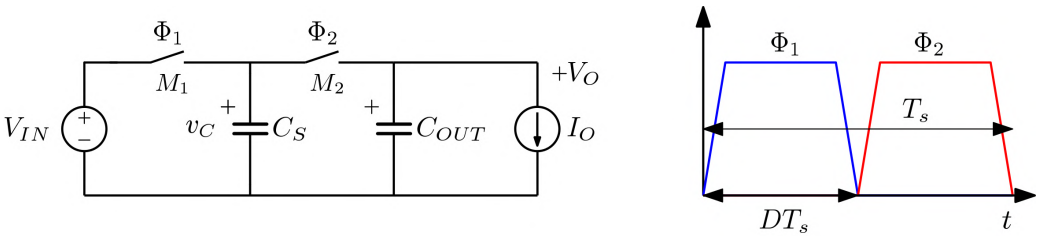


Figure 2.1.1: Basic one to one SCC and the corresponding switches ideal driving waveforms.

presented. This circuit has only one flying capacitor C_S and two switches. We will assume for simplicity that these two switches have the same on-resistance r_{sw}.

Let's name the two switching phases as Φ_1 and Φ_2 and define a duty cycle D as

$$D = \frac{T_{\Phi_1}}{T_s}$$

where T_{Φ_1} is the duration of Φ_1 and T_s is the switching period. In the switching phase Φ_1, M_1 is ON, while M_2 is open. It is then possible to write the following equation for the voltage v_C on C_S:

$$v_C(t) = v_C(0) + (V_{IN} - v_C(0))\left(1 - e^{-t/\tau}\right) \tag{2.1.1}$$

On the other hand, in the switching phase Φ_2, M_2 is conducting, while M_1 is open. The capacitor voltage then becomes

$$v(t) = v_C(DT_s) + (V_o - v_C(DT_s))\left(1 - e^{-(t-DT_s)/\tau}\right) \tag{2.1.2}$$

Combining equations (2.1.1) and (2.1.2) and exploiting the hypothesis made on the continuity and periodicity of v_C, expressed in the following equations

$$v_C\left(DT_s^-\right) = v_C\left(DT_s^+\right)$$

$$v_C(0) = v_C(T_s)$$

it is possible to obtain the following expressions

$$v_C(0) = \frac{V_o\left(1-e^{-\beta(1-D)}\right) + V_{IN}\left(1-e^{-\beta D}\right)e^{-\beta(1-D)}}{1-e^{-\beta}}$$

$$v_C(DT_s) = \frac{V_{IN}\left(1-e^{-\beta D}\right) + V_o\left(1-e^{-\beta(1-D)}\right)e^{-\beta D}}{1-e^{-\beta}}$$

where β

$$\beta \triangleq \frac{T_s}{\tau} = \frac{T_s}{R_{sw}C_s} \tag{2.1.3}$$

The knowledge of $v_C(0)$ and $v_C(DT_s)$ makes it possible to derive any other quantity of interest.

A parameter that is particularly interesting to evaluate, is the average current delivered to the load:

$$I_o = \frac{\Delta q_o}{T_s}$$

Δq_o represents the charge delivered by C_s during Φ_2 and can therefore be expressed as

$$\Delta q_o = C_s\left(v_C(DT_s) - v_C(0)\right)$$

Exploiting the previous equation and imposing $v_C(T_s) = v_c(0)$ it is then possible to find the following expression for I_o:

$$I_o = (V_{IN} - V_o)\, f_s C_s \frac{\left(1-e^{-\beta D}\right)\left(1-e^{-\beta(1-D)}\right)}{1-e^{-\beta}}$$

One important thing to notice, is that the average output current is proportional to $V_{IN} - V_o$. This makes it possible to express the voltage drop between the input and the output as a function of the average output current. It also possible to define an equivalent output resistance R_{eq}

$$R_{eq} \triangleq \frac{V_{IN} - V_o}{I_o} = \frac{1}{f_s C_s}\frac{1-e^{-\beta}}{\left(1-e^{-\beta D}\right)\left(1-e^{-\beta(1-D)}\right)} \tag{2.1.4}$$

The average power loss P_{loss} can now be considered

$$P_{loss} = P_{IN} - P_{OUT} = V_{IN} I_{IN} - I_o V_o$$

The average input current can be evaluated as

$$I_{IN} = \frac{\Delta q_{IN}}{T_s}$$

Steady-state operation yields $\Delta q_{IN} = \Delta q_o$, therefore $I_{IN} = I_o$. The average power loss is then given by

$$P_{loss} = (V_{IN} - V_o)\, I_o = R_{eq} I_o^2 \tag{2.1.5}$$

Analysing equation (2.1.5) it is possible to notice that the equivalent output resistance R_{eq} models the power dissipation in the circuit. This is actually true for all the switched capacitor converters.

2.1.2 Equivalent Output Resistance and Operational Regimes

In the previous section the analysis of a basic one to one SCC was carried out and an analytical expression for its output resistance was given. In equation (2.1.4) the output resistance R_{eq} is expressed as a function of the duty cycle and the parameter β, defined in (2.1.3). One aspect that is now interesting to understand, is how R_{eq} depends on β. This parameter expresses how fast the converter switches if compared to the charge and discharge time constant of the capacitor C_s. Let's consider the one to one cell again, exploiting the same hypothesis made in the previous section, it is now possible to estimate the limit value of R_{eq} when β tends to zero or infinite.

$$\lim_{\beta \to \infty} R_{eq} = \frac{1}{f_s C_s} \tag{2.1.6}$$

$$\lim_{\beta \to 0} R_{eq} = \frac{R_{sw}}{D} + \frac{R_{sw}}{1-D} = \frac{R_{sw}}{D\,(1-D)} \tag{2.1.7}$$

Since β expresses how fast the converter switches if compared to the charge and discharge time constant of the capacitor C_s, the conditions $\beta \to 0$ and $\beta \to \infty$ identify two different operating regimes:

1. an operating regime in which the switching period is much shorter than the charge and discharge time constant ($T_s \ll \tau$), named *fast switching limit*, or FSL

2. an operating regime in which the switching period is much longer than the charge and discharge time constant ($T_s \gg \tau$), named *slow switching limit*, or SSL

As a consequence, the two asymptotic limits for R_{eq} expressed in (2.1.6) and (2.1.7), can be identified as the equivalent output resistance *fast* and *slow switching limit*.

$$R_{FSL} \triangleq \lim_{\beta \to 0} R_{eq} = \frac{R_{sw}}{D\,(1-D)}$$

$$R_{SSL} \triangleq \lim_{\beta \to \infty} R_{eq} = \frac{1}{f_s C_s}$$

The two operational regimes named before will be now briefly considered singularly.

Fast Switching Limit

As previously said, this regime corresponds to a converter operating with a switching period much shorter than the flying capacitors charge and discharge time constants. In these conditions, the capacitors effectively act as voltage sources, and their voltage can be considered constant. The on-time of the switches is so short if compared to the capacitors charge and discharge times, that also the charge and discharge currents can be approximated as constant.

Since the capacitor voltages are approximately constant, the losses related to the capacitors charging and discharging become negligible and the equivalent output resistance is determined by the switches ON-resistances. This is a best-case scenario in terms of efficiency.

Slow Switching Limit

This regime corresponds to a converter operating with a switching period much longer than the flying capacitors charge and discharge time constants. In this operating condition the capacitors fully charge and discharge, currents

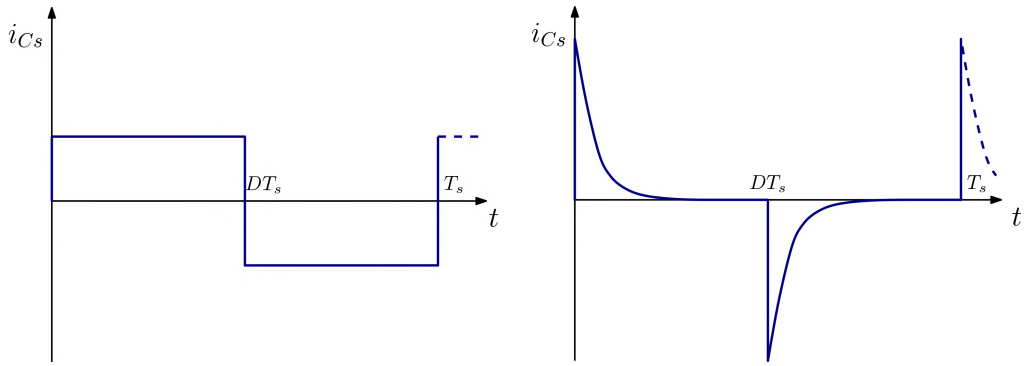


Figure 2.1.2: Examples of capacitor current waveforms in the FSL(left) and SSL (right) case.

waveforms are exponential and, for a desired average voltage value, the ripple is higher than in the FSL case.

Since the capacitors voltage can significantly vary during the switching period, power losses are dominated by the capacitors charge and discharge related dissipation, causing a drop in the efficiency.

An example of the current waveforms corresponding to the FSL and SSL conditions can be seen in Fig.2.1.2.

After studying the dependence of the equivalent output resistance on the parameter β, it is interesting to consider the relation between R_{eq} and the duty cycle.

In Fig.2.1.3 the equivalent output resistance normalized to the switches on-resistance R_{sw} as a function of D is shown (FSL case).

The first thing that it is possible to notice is that, for duty cycle values near to 0.5, the normalized equivalent output resistance value is almost constant, and starts to significantly increase for low and high values of D. In fact, when the duty cycle value becomes extremely high or low, $\frac{R_{eq}}{R_{sw}}$ asymptotically tends to an infinite value. This is important because, since the equivalent output resistance R_{eq} models the converter power losses, a high value of it means low efficiency. Fig. 2.1.3 shows, in fact, that the maximum efficiency corresponds to a fifty percent duty cycle value. This result makes sense, in fact, with constant average currents, very low or high duty cycle values mean that either the charge or discharge phase instantaneous current values, tend to become extremely high, thus dramatically increasing the losses.

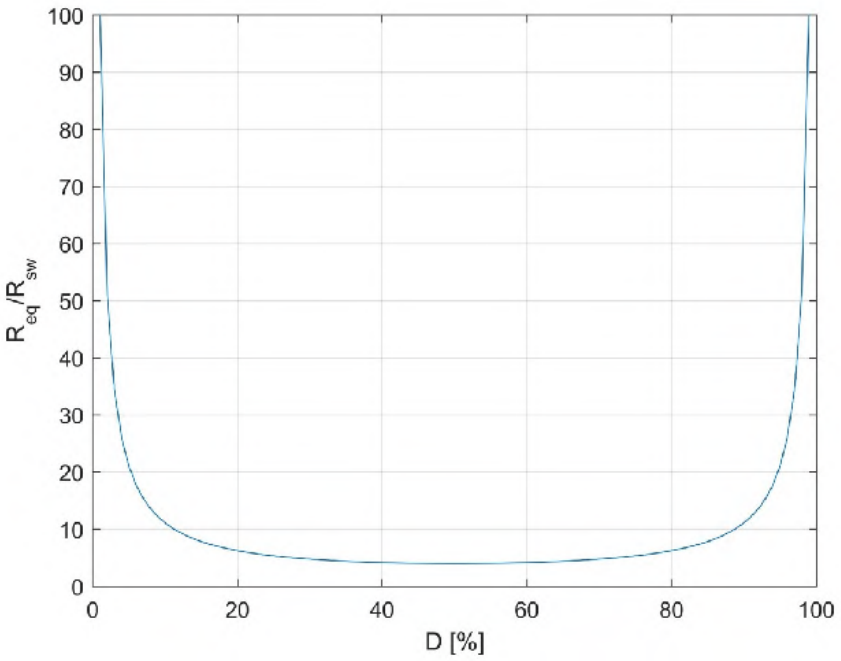


Figure 2.1.3: One to one SCC equivalent output resistance normalized to the switches on-resistance as a function of the duty cycle D (FSL case).

2.1.3 Equivalent Output Resistance Analysis Method

It was shown in the previous paragraphs that the equivalent output resistance of a switched capacitor converter models the power losses. There are different methods that allow to estimate it in a generic converter case. Example can be found in [1], while the most interesting method is described in [2] and [3]. Since the FSL operation is the best-case scenario for the efficiency, it is particularly interesting to estimate the *fast switching limit* equivalent output resistance. Since in this operational regime currents are supposed to be constant, this parameter can be simply evaluated by solving the Kirchhoff current equations and calculating the conduction losses on the switches. After this, it is possible to estimate the equivalent output resistance as

$$R_{FSL} = \frac{P_{loss}}{I_o^2}$$

where I_o^2 is the average output current and P_{loss} are the estimated switches conduction losses. This method will be used in the following to estimate the best case equivalent output resistance of the Dickson charge pump topology.

2.1.4 Conversion Ratio

One of the main characteristics of the switched capacitor converters is their fixed conversion ratio. In fact, the most common SCC topologies, in the step-up case, are characterized by a two phase operation: in one phase the load is being fed by the output capacitor, disconnected from the rest of the circuit; in the other phase the output capacitor is charged. It is then pretty straightforward to understand that the output voltage depends on how the flying capacitors are connected together during the output capacitor charging phase. In the step down case it is the input source that is alternatively connected or disconnected and the same reasoning applies.

Some techniques to regulate the output voltage are presented in literature, but they are usually based on changing the equivalent output resistance, for example by changing the duty cycle. When using this strategy, SCCs become somehow similar to linear regulators.

2.2 Multilevel Converters

Automotive applications typically require the converters to adapt to wide varying input and output voltages, therefore a single fixed conversion ratio is not a good choice. Combining multiple stages and implementing a reconfigurable topology allows to obtain a multi-level switched capacitor converter (a converter characterized by more than one possible conversion ratio). Starting from the most common SC converters their multilevel counterparts were derived. In the following the corresponding topologies will be shown and their characteristics in terms of resolution, switches voltage stress and number of components will be considered. The hypotheses made in this study were steady-state operation and the usage of a large output capacitor, so that the output voltage can be considered constant. Only step-up converters are presented here, anyway their step-down counterparts can be obtained by simply exchanging the input with the output.

2.2.1 Series-Parallel

This topology, shown in Fig. 2.2.1, is maybe the simplest one. As it is possible to see in Fig.2.2.2 and Fig.2.2.3, it is based on connecting a number of capacitors alternatively in parallel and in series with the input. Every flying capacitor is therefore charged to V_{IN} and if the converter has N cells, the output capacitor is charged to $N+1$ times the input voltage. The different conversion ratios can be selected by keeping the unnecessary cells inactive. In the example of Fig.2.2.1, to obtain a conversion ratio equal to N, C_1 will be always connected in parallel with the input.

To estimate the voltage stresses on the components, a generic cell of order k, with $1 \leq k \leq N$, was considered (Fig.2.2.4).

As it is possible to observe in Fig.2.2.5, it is straightforward to derive the voltage stress on S_2: $V_{OUT_k}$is in fact equal to V_{IN} for every k, therefore also for the voltage stress on v_{s_2} is equal to V_{IN} too.

Let's now consider the $k-th$ cell discharging phase; in this case $V_{OUT_{k-1}}$ is equal to kV_{IN}, we can therefore estimate the switches voltage stress as

$$v_{S_1} = V_{OUT_k} - V_{IN} = kV_{IN}$$

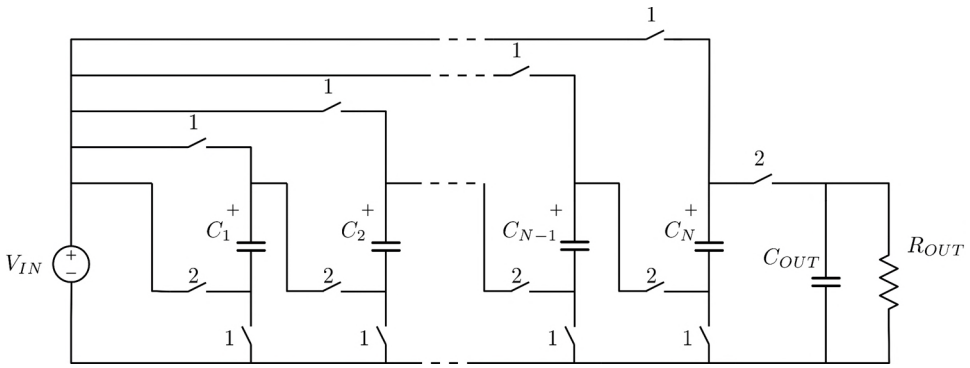


Figure 2.2.1: Series-parallel topology.

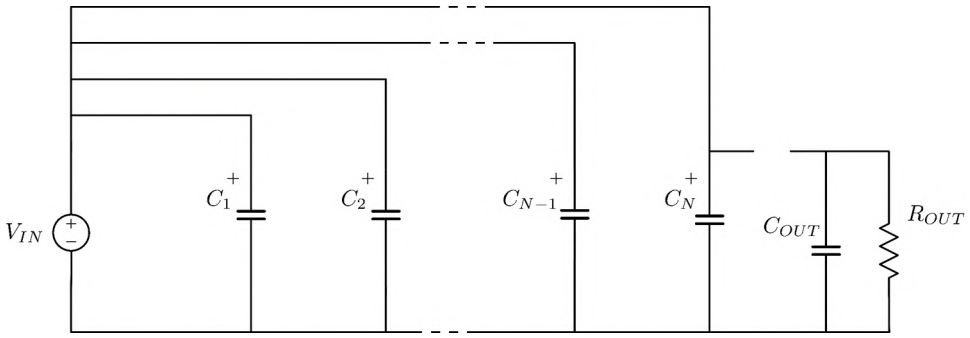


Figure 2.2.2: Series-parallel topology equivalent circuit in phase one.

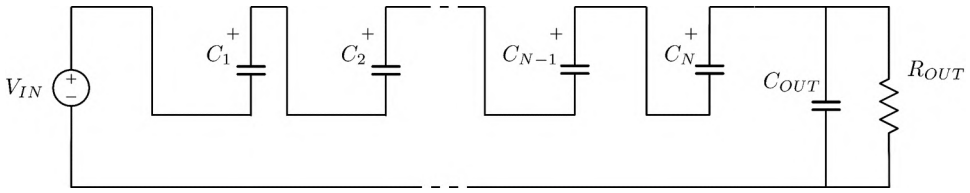


Figure 2.2.3: Series-parallel topology equivalent circuit in phase two.

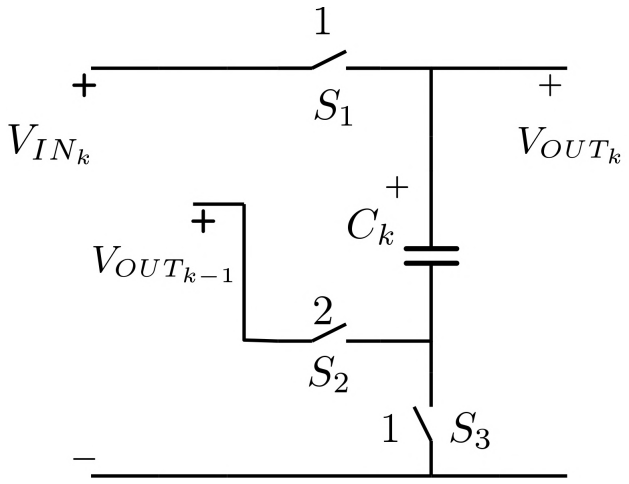


Figure 2.2.4: Generic series-parallel cell of order k.

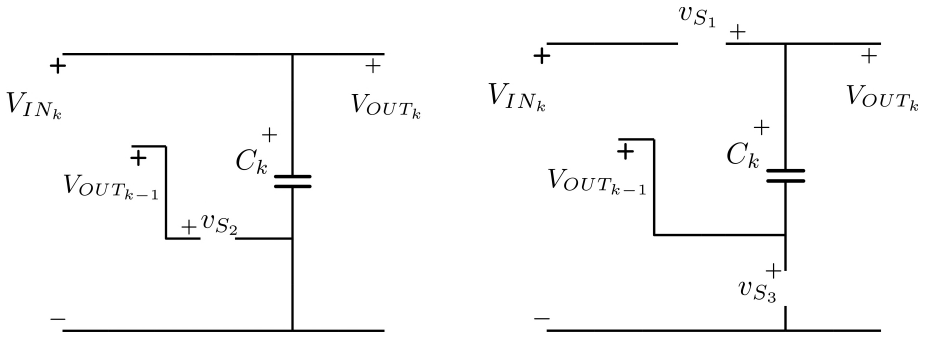


Figure 2.2.5: Generic series-parallel cell of order k equivalent circuit in the charging (left) and discharging (right) phase.

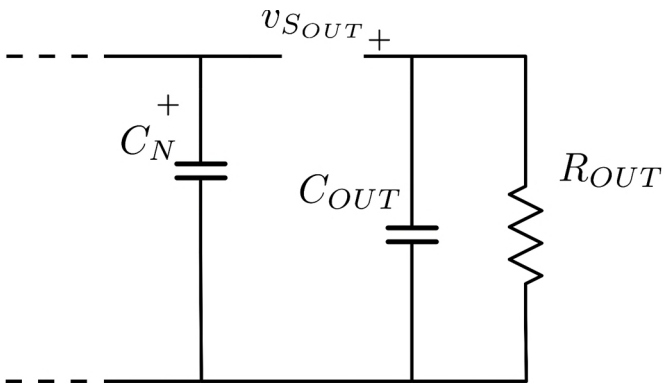


Figure 2.2.6: Series-parallel topology output switch voltage stress estimation.

$$v_{S_3} = V_{OUT_{k-1}} = kV_{IN}$$

Knowing the number of cells N of the converter, it is possible to estimate also the voltage stress on the output switch (Fig.2.2.6).

$$v_{S_{OUT}} = V_{OUT} - V_{IN} = NV_{IN}$$

Another important converter characteristic it is interesting to know is the number of switches needed to obtain a desired conversion ratio. Since every cell employs three switches and an extra output switch is also necessary, the total number of switches n_S amounts to $3 \cdot N + 1$, where N is the number of cells of the converter.

Knowing the relation between the number of cells and the conversion ratio, it is possible to express the estimated parameters as a function of the maximum requested conversion ratio M.

- Number of switches

$$3M - 2$$

- Number of flying capacitors

$$M - 1$$

- Maximum switch voltage stress

$$(M - 1)V_{IN}$$

i	0	1	2	3	4	5
F_i	1	1	2	3	5	8

Figure 2.2.7: Fibonacci series limited to the first six elements.

- Maximum flying capacitor voltage

$$V_{IN}$$

It is important to notice that, while the voltage applied on the flying capacitors is always equal to V_{IN}, the switches voltage stress depends on the maximum requested conversion ratio.

2.2.2 Fibonacci

This topology is called Fibonacci converter because it allows to obtain all the conversion ratios specified by the so called Fibonacci series; this is defined as the series in which the first two numbers are zero and one, and every other element is derived summing the previous two (in Fig.2.2.7 the first six numbers of the series can be seen). An N stages converter will implement a maximum conversion ratio equal to the $(N+1)-th$ number of the Fibonacci series. As in the series-parallel case, the different possible conversion ratios can be selected by keeping the unnecessary cells inactive (in parallel with the input voltage source or the output capacitor).

As it is possible to see in Fig.2.2.8, this topology is built cascading identical cells constituted of a capacitor and three switches. The most important thing to notice, respect to the modulation law shown in Fig.2.2.8, is that nearby cells work with alternate phases, so that when one cell's capacitor is being charged, the neighbouring two are being discharged.

To better understand how this converter works, a five time multiplier example can be considered (Fig.2.2.9). In phase one (Fig.2.2.10) C_1 is charged to V_{IN} while C_3 is charged by the series of C_1 and C_2. On the other hand, in phase two (Fig.2.2.11), C_2 is charged by the series of V_{IN} and C_1, while the output capacitor is charged by the series of C_2 and C_3. We can therefore write the following equations:

$$V_{C_1} = V_{IN}$$

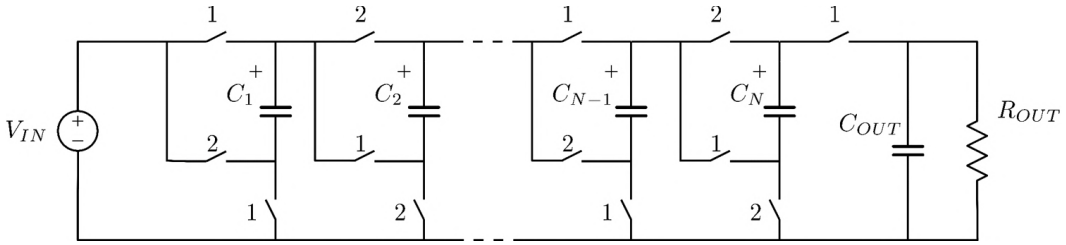


Figure 2.2.8: Fibonacci topology.

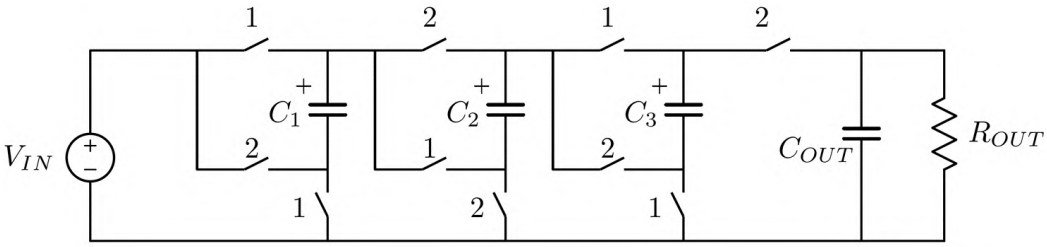


Figure 2.2.9: Fibonacci topology three stages example.

$$V_{C_2} = V_{IN} + V_{C_1} = 2V_{IN}$$

$$V_{C_3} = V_{C_2} + V_{C_1} = 3V_{IN}$$

$$V_{C_{OUT}} = V_{C_3} + V_{C_2} = 5V_{IN}$$

From this example, it is possible to see how every cell's capacitor is charged by the series of the capacitors of the two previous cells. The only exception is the first cell's capacitor, that is charged by V_{IN}.

To estimate the voltage stresses on the components, a generic cell of order k was considered. The charging phase can be considered first (Fig.2.2.12). Since we know that neighbouring cells work in the opposite phase, we are able to estimate the cell input voltage as

$$V_{IN_k} = V_{IN} F_k$$

where F_k is the $k-th$ number of the Fibonacci series. Therefore C_k is charged to

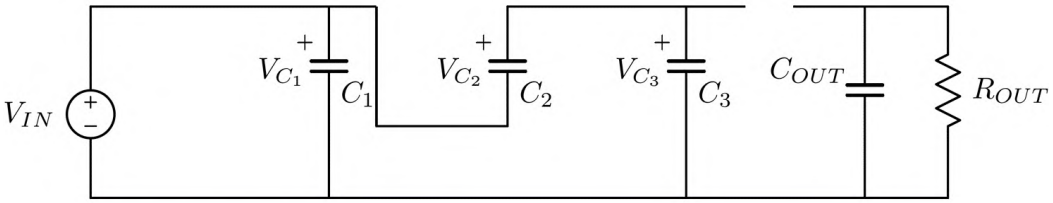


Figure 2.2.10: Fibonacci topology three stages example: phase 1.

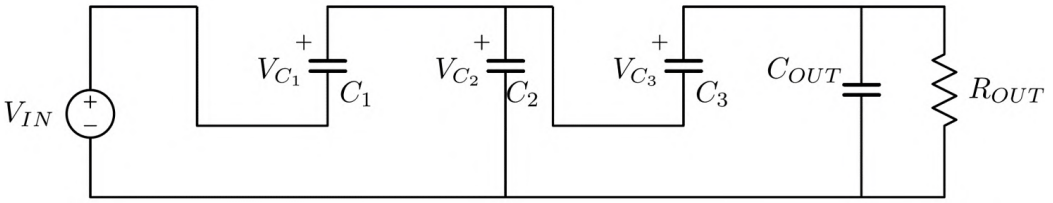


Figure 2.2.11: Fibonacci topology three stages example: phase 2.

$$V_{C_k} = V_{IN} F_k$$

and the voltage stress on S_2 is

$$v_{S_2} = V_{IN_k} = V_{IN} F_k$$

To estimate the voltage stress on S_1 and S_3 the discharge phase must be considered (Fig.2.2.12). In this case the neighbouring cells are in their charging phase, so that the $k-th$ cell input voltage can be estimated as

$$V_{IN_k} = V_{C_{k-1}} = V_{IN} F_{k-1}$$

Knowing the cell input voltage, the switches voltage stress can be estimated as

$$v_{S_1} = V_{C_k} = V_{IN} F_k$$

$$v_{S_3} = V_{IN_k} = V_{IN} F_{k-1}$$

Knowing the number of cells N of the converter, it is possible to estimate also the voltage stress on the output switch (Fig.2.2.6).

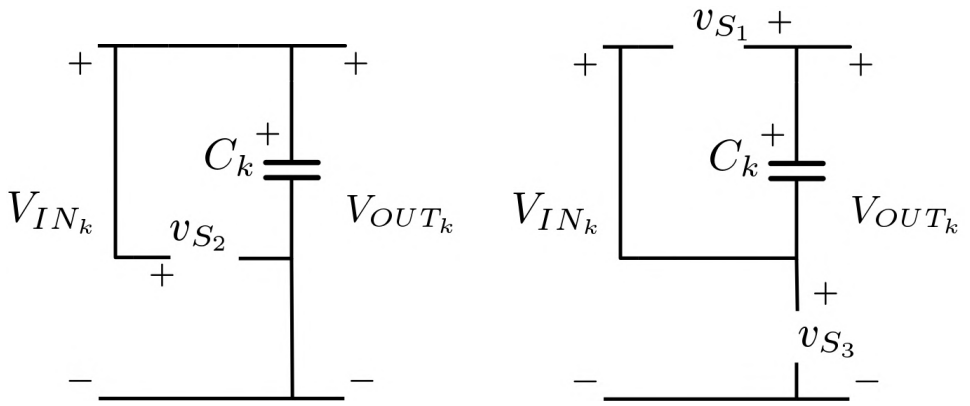


Figure 2.2.12: Generic Fibonacci topology cell of order k: charging (left) and discharging phase (right).

$$v_{S_{OUT}} = V_{OUT} - V_{C_N} = V_{IN} F_{N-1}$$

The Fibonacci converter characteristics can therefore be resumed as a function of the total number of cells N of the converter as follows:

- Number of switches
$$3N + 1$$
- Number of flying capacitors
$$N$$
- Maximum switch voltage stress
$$V_{IN} F_N$$
- Maximum flying capacitor voltage
$$V_{IN} F_N$$

It is important to notice that in this case, both the voltage applied to the flying capacitors and switches depends on the maximum requested conversion ratio.

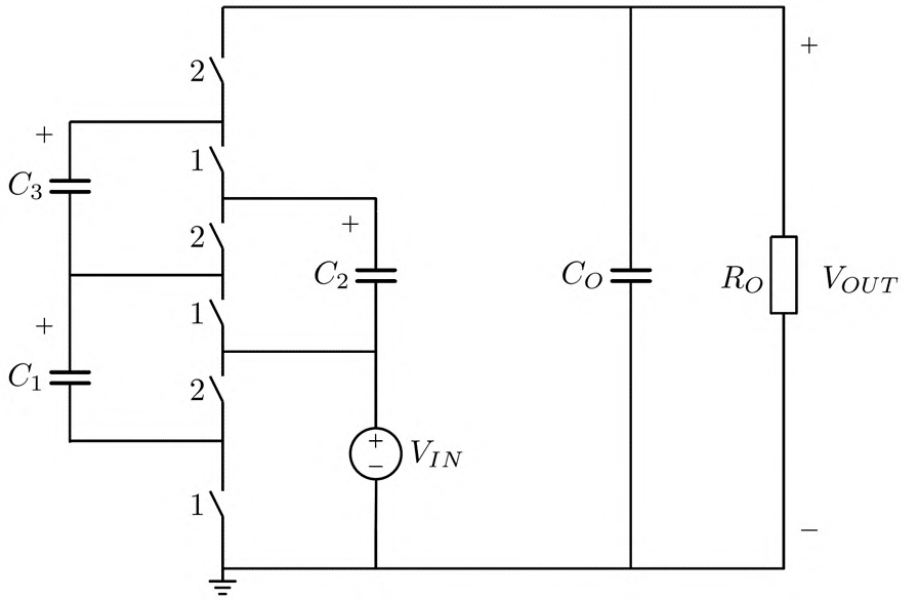


Figure 2.2.13: Standard ladder topology.

2.2.3 Multilevel Ladder

The basic ladder converter is characterized by the very interesting property of having a fixed voltage stress on all switches, equal to the input voltage. Unluckily this topology cannot be transformed into a multilevel converter simply by cascading multiple basic stages, therefore some variations had to be introduced developing the so called multilevel ladder topology.

To understand how this converter works, it is better to analyse its standard version first. For simplicity a three stage version can be considered (Fig.2.2.13). During the first operation phase (Fig. 2.2.14), C_1 is charged by V_{IN} and C_3 is charged by C_2. In the second phase (Fig.2.2.15), on the other hand, C_1 charges C_2 and C_O is charged by the series of V_{IN}, C_1 and C_3.

We can therefore write the following equations:

$$v_{C_1} = v_{C_2} = v_{C_3} = V_{IN}$$

$$V_{OUT} = V_{C_O} = V_{IN} + V_{C_1} + V_{C_3} = 3V_{IN}$$

All the flying capacitors are charged to the input voltage.

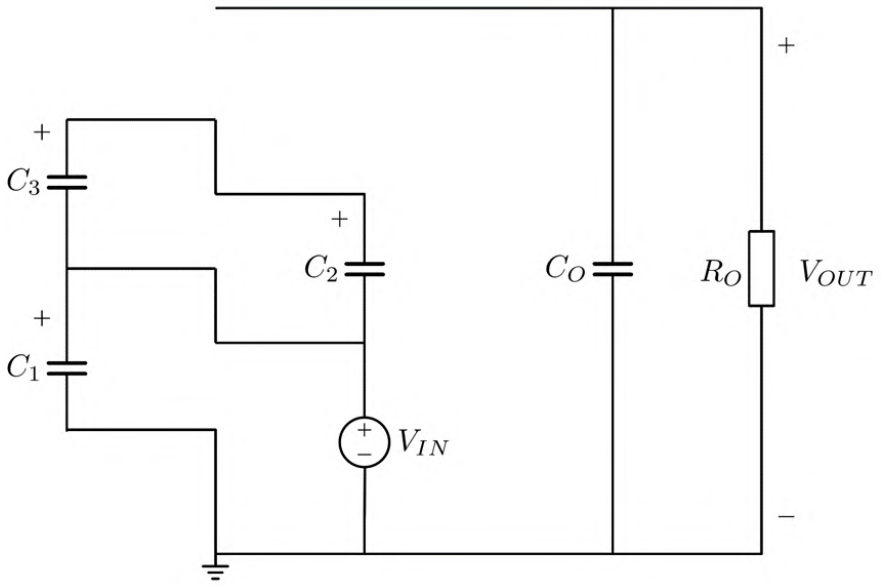


Figure 2.2.14: Three stage standard ladder equivalent circuits: phase one.

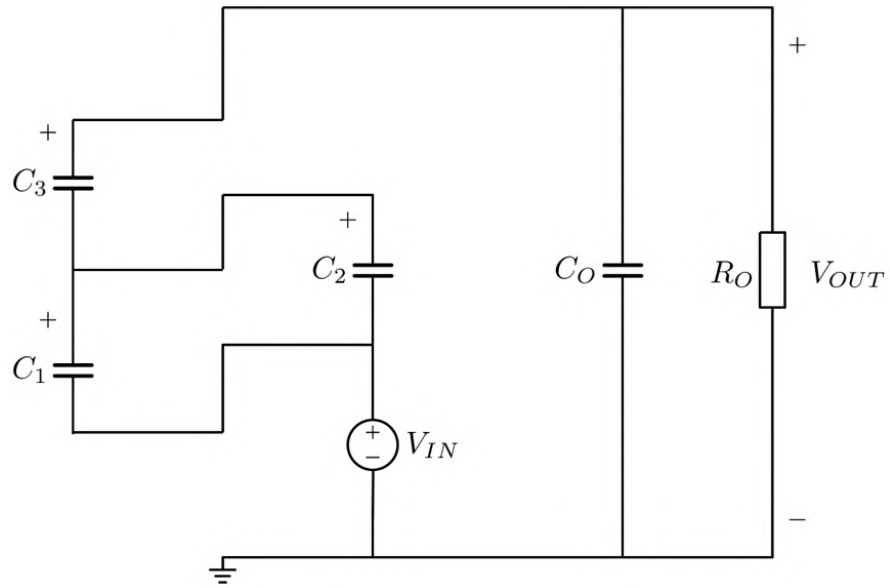


Figure 2.2.15: Three stage standard ladder equivalent circuit: phase two.

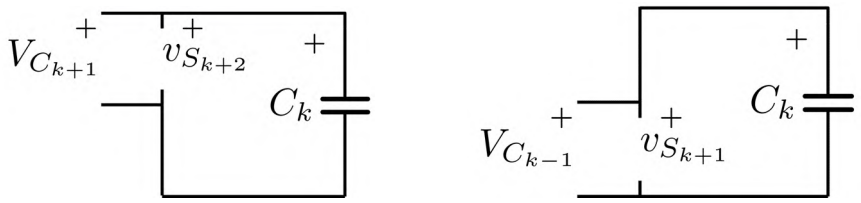


Figure 2.2.16: Standard ladder topology generic cell: equivalent circuit during the discharge (left) and charge phase (right).

This analysis can be generalized to an N flying capacitors converter case. Being the output capacitor always charged by the series of the odd flying capacitors, it is possible to derive the following expression for the output voltage:

$$M = \frac{V_{OUT}}{V_{IN}} = \frac{N+1}{2} + 1 = \frac{N+3}{2} \tag{2.2.1}$$

with N odd. In the even N case instead, the conversion ratio becomes

$$M = \frac{N+2}{2}$$

It is interesting to notice that, using N even flying capacitors, gives the same conversion ratio that can be obtained with $N-1$ elements, therefore it makes no sense.

The voltage stress on the switches must now be evaluated. The cell corresponding to a general $k-th$ flying capacitor is considered. The equivalent circuit in both the capacitor charge and discharge phase can be seen in Fig.2.2.16. Since every capacitor is charged to V_{IN}, it is straightforward to estimate the cell switches voltage stress:

$$v_{S_{k+1}} = V_{C_k} = V_{IN}$$

$$v_{S_{k+2}} = V_{C_k} = V_{IN}$$

The voltage stress on the switches is the same and equal to the input voltage.

As previously shown, the standard ladder converter is characterized by a single fixed conversion ratio. A simple way to transform this topology into

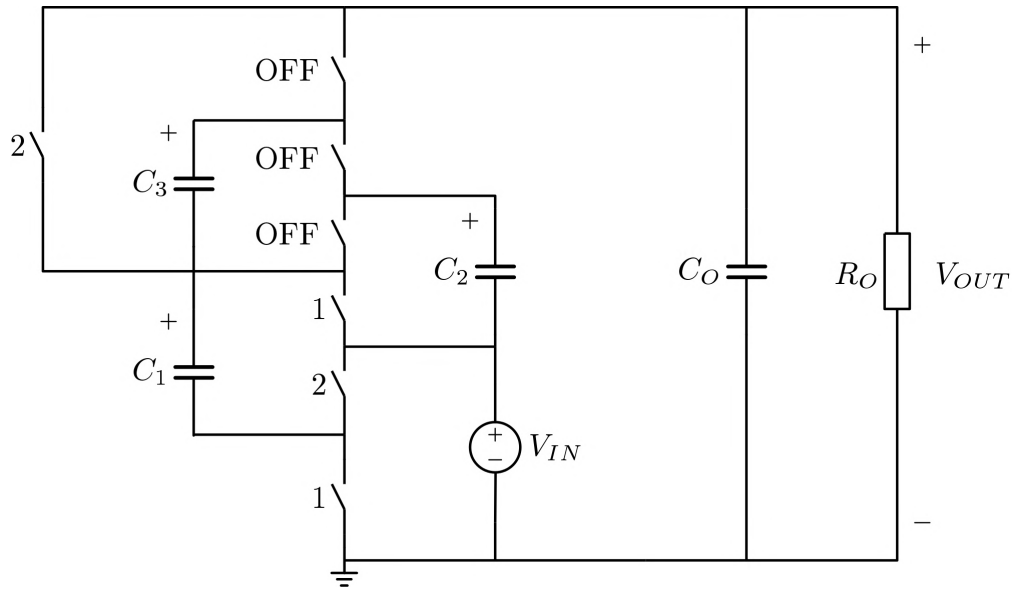


Figure 2.2.17: Example of the multilevel ladder topology. To allow for a lower conversion ratio than the one implemented by a standard ladder topology with three capacitors, some switches must be kept constantly OFF and an extra bypass switch must be added.

a multilevel one is adding some bypass switches. These switches allow to bypass part of the flying capacitors, reducing the equivalent number of them. Thus the conversion ratio is reduced too. The modified topology, named multilevel ladder converter, can implement all the integer conversion ratios comprised between two and $\frac{N+3}{2}$, and an example of this approach can be seen in Fig.2.2.17. In this specific case, the additional switch allows to bypass the capacitors C_2 and C_3, obtaining a conversion ratio equal to two.

The main advantage of the standard ladder converter is the low switches voltage stress. In the multilevel ladder case the voltage stress on the added devices must also be taken into account. Since every additional switch must connect the positive node of an odd flying capacitor with the output, it is possible to consider the generic case shown in Fig.2.2.18

The voltage stress on the bypass switch that connects the $k-th$ switch to the output can be estimated as follows:

$$v_{S_{kBP}} = V_{OUT} - v_x$$

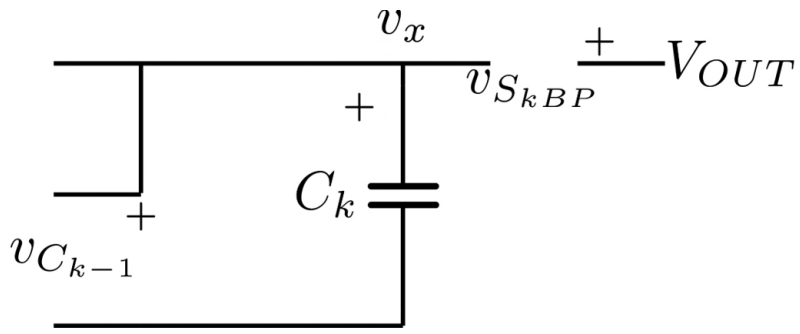


Figure 2.2.18: Multilevel ladder topology: $k-th$ cell bypass switch voltage stress estimation.

The voltage stress then varies depending on which flying capacitor is considered. To be able to compare this topology performance with the other ones, the worst case scenario is considered, this corresponds to the minimum $v_x$value, attained when considering $k = 1$. In that case the voltage stress on the bypass switch becomes

$$v_{S_{kBP}} = V_{OUT} - V_{C_1} = V_{OUT} - V_{IN} = (M-1)V_{IN} \tag{2.2.2}$$

Substituting eq.(2.2.1) in (2.2.2) we can express the voltage stress as a function of the converter number of cells

$$v_{S_{kBP}} = \left(\frac{N+3}{2} - 1\right) V_{IN} = \left(\frac{N+1}{2}\right) V_{IN}$$

The number of switches required for this converter must now be evaluated. For simplicity let's estimate the number of switches of a standard one flying capacitor converter first. In this case two switches for the cell are needed together with one extra input and one output device. If we think about expanding this structure, it is pretty clear that one new switch per extra cell is needed, therefore the number of switches n_S can be expressed as

$$n_S = 4 + (N-1) = 3 + N$$

In the multilevel ladder case an extra switch for every odd flying capacitor minus one will be needed. We can therefore write

$$n_S = 3 + N + \left(\frac{N+1}{2} - 1\right) = \frac{3N+5}{2}$$

The multilevel ladder characteristics, expressed as a function of the maximum attainable conversion ratio M, are summarized in the following:

- Number of switches
$$3M - 2$$
- Number of flying capacitors
$$2M - 3$$
- Maximum switch voltage stress
$$(M-1)V_{IN}$$
- Maximum flying capacitor voltage
$$V_{IN}$$

2.2.4 Dickson Charge Pump

This topology is one of the oldest SC converters and is probably the most used nowadays, both in literature and in the market. As it is possible to see in Fig.2.2.19 it is obtained cascading multiple basic cells, made of a flying capacitor and three switches, and adding an output capacitor and an additional switch.

To understand how this topology works, a four times multiplier example is studied (Fig.2.2.20). In phase one, Fig.2.2.21, the first flying capacitor (C_1) is charged to V_{IN}, while C_3 is charge by the series of the input voltage source and C_2. In this phase the load is being fed only by the output capacitor. In phase two instead (Fig.2.2.22), C_2 is charged by the series of C_1 and the input voltage source, while C_O is charged by the series of the input voltage source and C_3. We can then write the following equations for the capacitor voltages:

$$V_{C_1} = V_{IN}$$

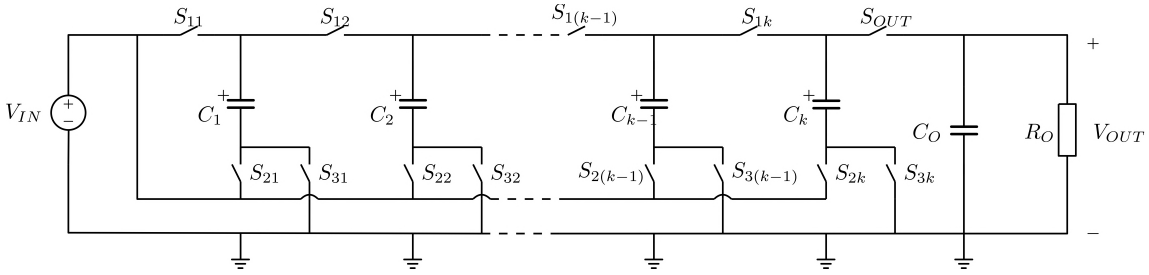


Figure 2.2.19: Generic Dickson charge pump converter.

$$V_{C_k} = V_{C_{k-1}} + V_{IN} \quad for\, k = 2, 3$$

$$V_{C_O} = V_{C_3} + V_{IN} = 4V_{IN}$$

As it is possible to understand from this specific example, in the Dickson charge pump topology every capacitor is charged to the input voltage plus the previous capacitor voltage, except the first one, that is charged to the input voltage. In general, we can therefore estimate the charging voltage of the $k-th$ flying capacitor as

$$V_{C_k} = kV_{IN} \tag{2.2.3}$$

Therefore a topology with N total flying capacitor implements a maximum conversion ratio equal to

$$M = (N+1)\, V_{IN}$$

To estimate the switches voltage stress a generic cell of order k is considered (Fig.2.2.23). To be able to compute the voltage stress it is important to remember that, in this topology, neighbouring cells work in the opposite phase, therefore, when one cell is in its capacitor charging phase, the neighbouring two are in the capacitor discharge one.

The $k-th$ cell charging phase is studied first (Fig.2.2.24). The switches S_{1k} and S_{3k} are ON and the voltage stress on S_{2k} is equal to

$$v_{S_{2k}} = V_{IN}$$

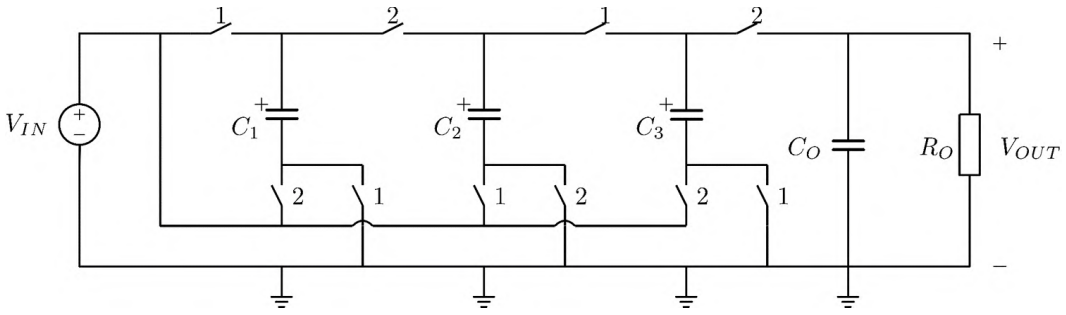


Figure 2.2.20: Dickson charge pump: four times multiplier example.

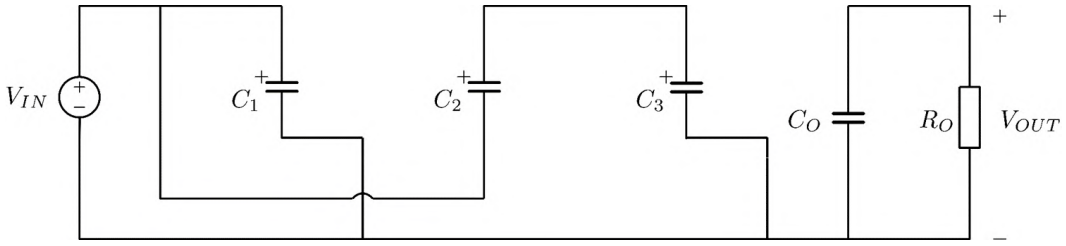


Figure 2.2.21: Dickson charge pump: four times multiplier example, phase one equivalent circuit.

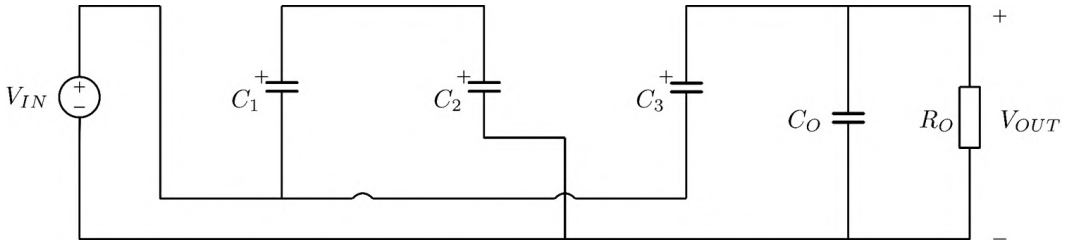


Figure 2.2.22: Dickson charge pump: four times multiplier example, phase two equivalent circuit.

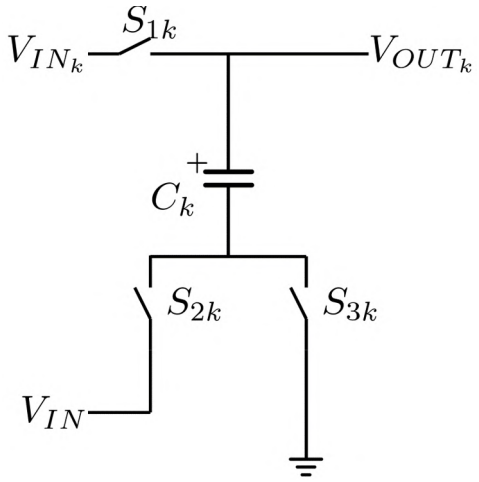


Figure 2.2.23: Generic Dickson charge pump cell.

In the discharging phase instead (also shown in Fig.2.2.24), S_{2k} is conducting, while the voltage stress on S_{1k} and S_{3k} is

$$v_{S_{1k}} = V_{IN} + V_{C_k} - V_{IN_k} \tag{2.2.4}$$

and

$$v_{S_{3k}} = V_{IN}$$

If $k > 1$ the cell input voltage during C_k discharging phase is given by eq.(2.2.5)

$$V_{IN_k} = V_{C_{k-1}} \tag{2.2.5}$$

Substituting eq.(2.2.3) in (2.2.5), equation (2.2.6) is derived.

$$V_{IN_k} = (k-1)\, V_{IN} \tag{2.2.6}$$

Using eq.(2.2.6) in (2.2.4) the voltage stress on S_{1k} can be finally estimated as

$$v_{S_{1k}} = 2V_{IN}$$

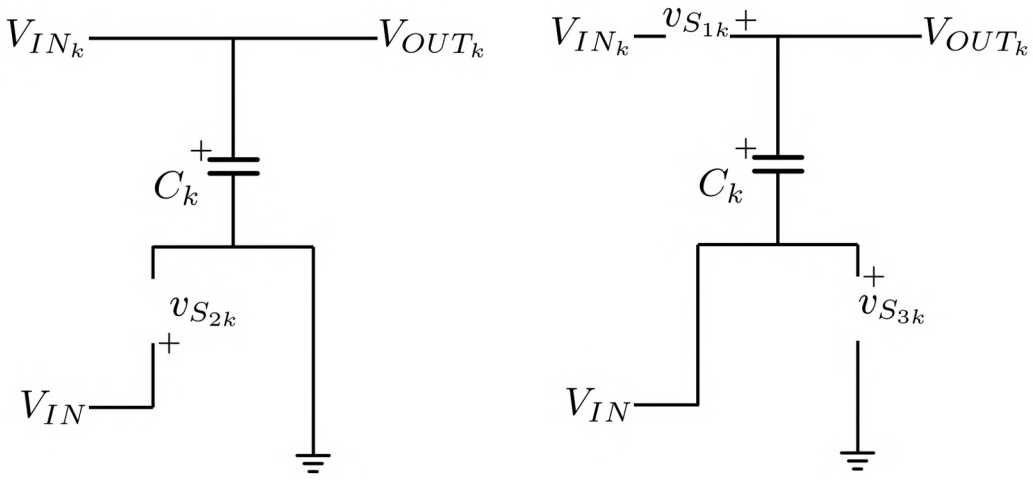


Figure 2.2.24: Generic Dickson charge pump equivalent circuit in the charging (left) and discharging (right) phase.

In the case of the first cell ($k = 1$) things are a bit different and equation (2.2.5) is not valid anymore. In this case the cell input voltage V_{IN_k} is in fact always equal to V_{IN}. The voltage stress on the switches is then described by the following equation:

$$v_{S_{11}} = v_{S_{21}} = v_{S_{31}} = V_{IN}$$

It is important to notice that, in this converter, the voltage stress on the switches is independent of the implemented conversion ratio.

As previously reported, this converter employs three switches and a flying capacitor for every cell, plus an extra switch that connects the last cell to the output. Given N total cells, the number of switches employed is

$$n_S = 3N + 1$$

The Dickson charge pump topology characteristics, expressed as a function of the maximum attainable conversion ratio M, are summarized in the following:

- Number of switches

$$3M - 2$$

- Number of flying capacitors

$$M - 1$$

- Maximum switch voltage stress

$$2V_{IN}$$

- Maximum flying capacitor voltage

$$(M - 1)\, V_{IN}$$

2.2.5 N Times Multiplier (nX Converter)

This topology is obtained cascading multiple basic cells made of two capacitors and four switches. The capacitors of every cell are charged to a voltage equal to V_{in} plus the charging voltage of the previous cell capacitor, it is therefore possible to write

$$V_{C_j} = V_{IN} + V_{C_{j-1}}$$

where V_{C_j} is the charging voltage of the capacitors of the $j - th$ cell.
In the case of an N cells topology the charging voltage of the capacitors of the highest order cell can then be expressed as

$$V_{C_N} = NV_{IN}$$

while the number of flying capacitors and switches employed is

$$n_c = 2N$$

and

$$n_s = 4N$$

A six times multiplier example of this topology can be seen in Fig.2.2.25. From this example it is possible to notice that this converter exploits interleaving to generate an output voltage equal to $2V_{C_N}$, where V_{C_N} is the

charging voltage of the capacitors of the highest order cell. The maximum attainable conversion ratio is therefore

$$M = 2V_{C_N} = 2NV_{IN}$$

It is also interesting to notice that, by using an interleaved structure, no extra output capacitor is needed.

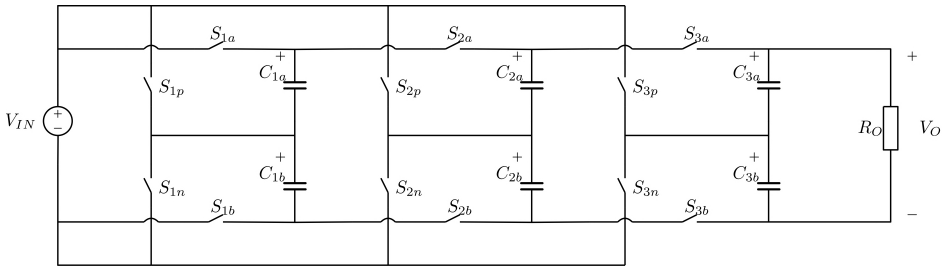


Figure 2.2.25: Six times multiplier nX converter.

To better understand how this converter works, the operation of the six times multiplier topology of Fig.2.2.25 is analysed in detail. The converter equivalent circuit in phase one can be seen in Fig.2.2.26. In this phase C_{1a}, C_{2b} and C_{3a} are charged, while the other capacitors are in their discharge phase. A clearer understanding of this can be obtained looking at figures 2.2.27, 2.2.28 and 2.2.29, where the different sub-circuits are highlighted.

It is important to notice that while C_{1a} is charged by V_{IN}, C_{2b} is charged by the series of the input voltage source and C_{1b}. Capacitor C_{3a} is instead charged by the series of V_{IN} and C_{2b}. It is then possible to write the following equations for the capacitor voltages:

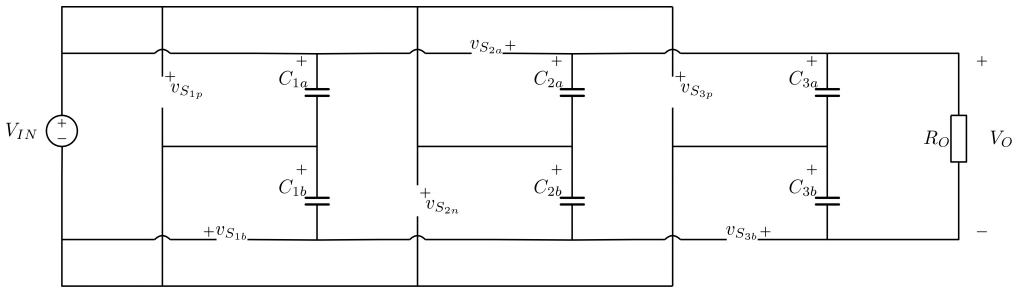


Figure 2.2.26: Six times multiplier nX converter phase one equivalent circuit.

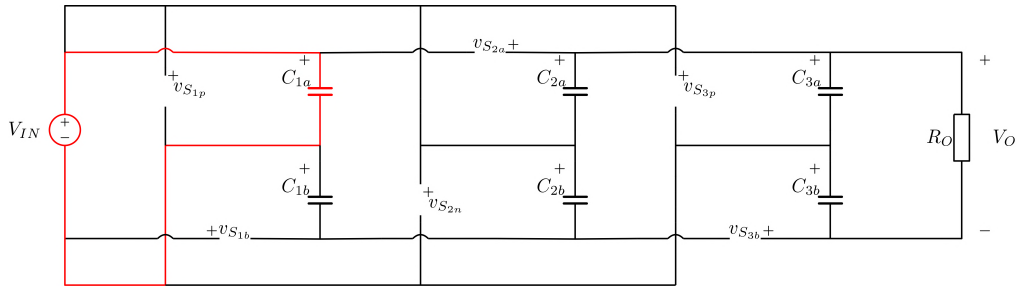


Figure 2.2.27: Six times multiplier nX converter phase one sub-circuits: C_{1a} charging circuit.

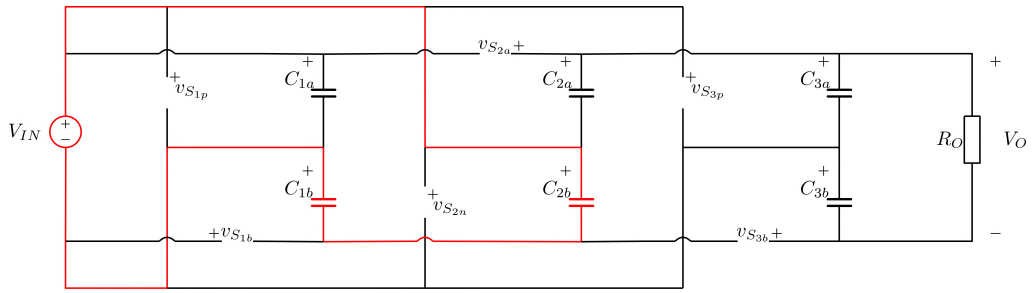


Figure 2.2.28: Six times multiplier nX converter phase one sub-circuits: C_{2b} charging circuit.

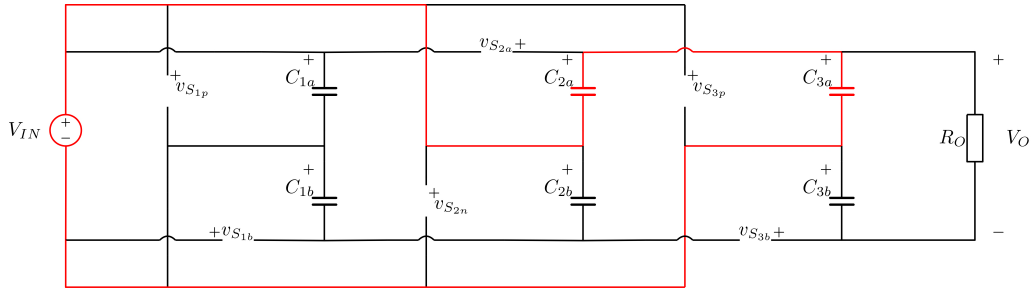


Figure 2.2.29: Six times multiplier nX converter phase one sub-circuits: C_{3a} charging circuit.

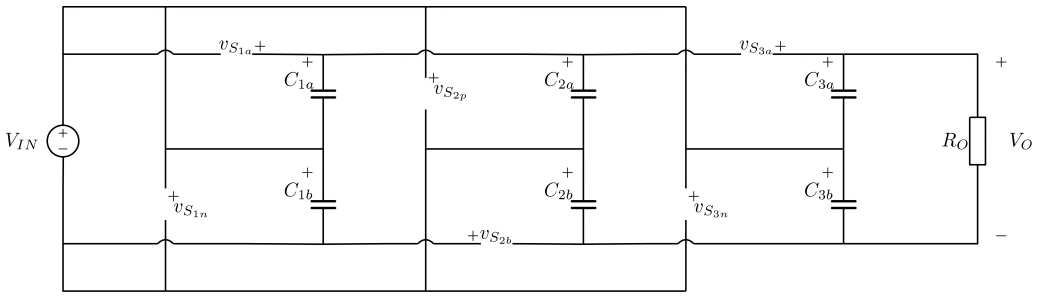


Figure 2.2.30: Six times multiplier nX converter phase two equivalent circuit.

$$v_{C_{1a}} = V_{IN}$$

$$v_{C_{2b}} = v_{C_{1b}} + V_{IN}$$

$$v_{C_{3a}} = v_{C_{2a}} + V_{IN}$$

Analogously, in phase two (Fig.2.2.30), C_{1b}, C_{2a} and C_{3b} are charged, while the other capacitors are in their discharge phase. Once again it is possible to highlight the different sub-circuits (Fig.2.2.31, 2.2.32 and 2.2.33) and the following equations for the capacitor voltages can be derived:

$$v_{C_{1b}} = V_{IN}$$

$$v_{C_{2a}} = v_{C_{1a}} + V_{IN}$$

$$v_{C_{3b}} = v_{C_{2b}} + V_{IN}$$

Combining the voltage equations obtained from the analysis, it is possible to estimate the capacitor charging voltages as

$$v_{C_{1a}} = v_{C_{1b}} = V_{IN}$$

$$v_{C_{2a}} = v_{C_{2b}} = 2V_{IN}$$

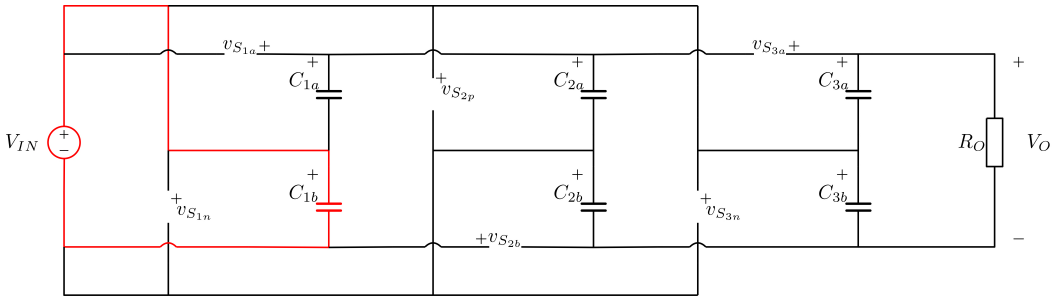


Figure 2.2.31: Six times multiplier nX converter phase two sub-circuits: C_{1b} charging circuit.

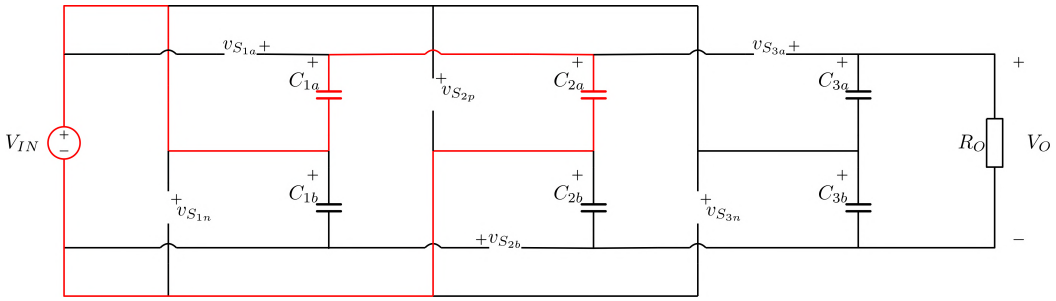


Figure 2.2.32: Six times multiplier nX converter phase two sub-circuits: C_{2a} charging circuit.

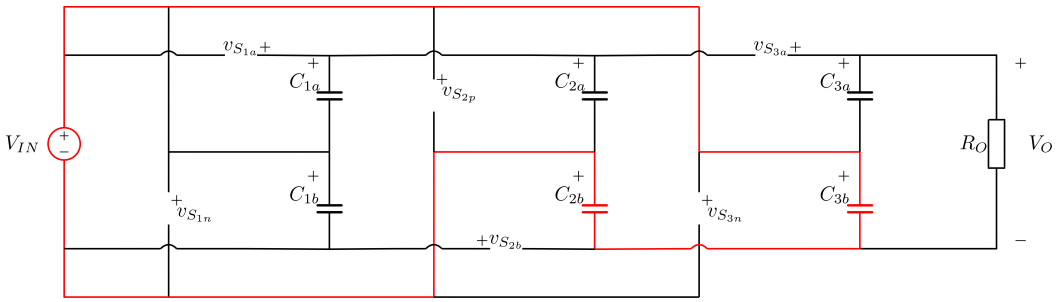


Figure 2.2.33: Six times multiplier nX converter phase two sub-circuits: C_{3b} charging circuit.

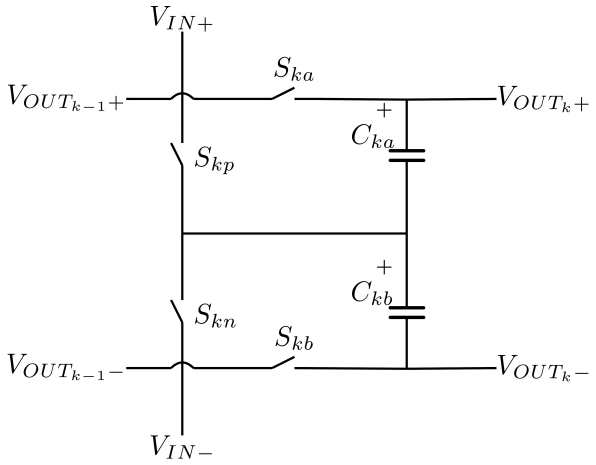


Figure 2.2.34: Generic nX converter $k-th$ cell.

$$v_{C_{3a}} = v_{C_{3b}} = 3V_{IN}$$

The output voltage is then

$$V_O = v_{C_{3a}} + v_{C_{3b}} = 6V_{IN}$$

This example shows us that, as said in the beginning of the section, every capacitor is charged to a voltage equal to V_{in} plus the charging voltage of the previous cell capacitors.

To estimate the switches voltage stress a generic cell of order k is considered (Fig.2.2.34), with $k > 1$. It is important to remember that, in this topology, neighbouring cells work in the opposite phase, and that V_{IN-} is the circuit voltage reference.

The cell equivalent circuits in the two operating phases are shown in Fig.2.2.35. In phase one capacitor C_{kb} is charged and the following expressions for the voltages can be derived:

$$V_{OUT_{k+}} = V_{IN_+} + v_{C_{ka}} = (k+1)\, V_{IN}$$

$$V_{OUT_{k-}} = V_{OUT_{k-1}-}$$

Phase two is C_{ka} charging phase and the voltages equations are:

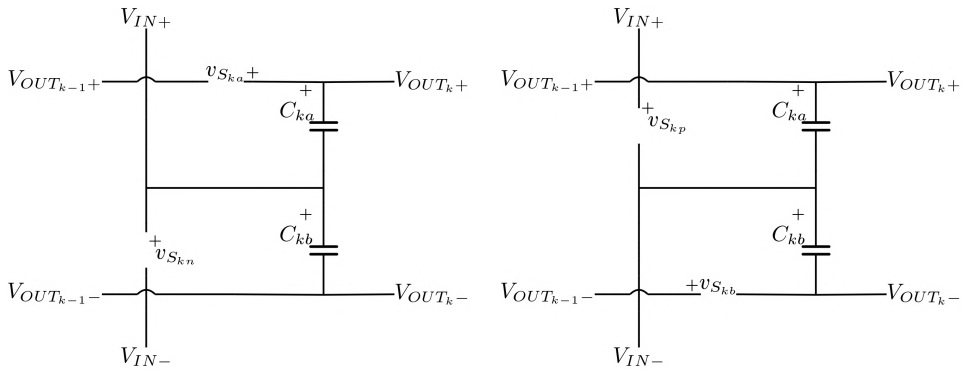


Figure 2.2.35: Generic nX converter $k-th$ cell equivalent circuit in phase one (left) and two (right).

$$V_{OUT_{k+}} = V_{IN-} + V_{C_{ka}} = kV_{IN}$$

$$V_{OUT_{k-}} = -v_{C_{kb}} = -kV_{IN}$$

After deriving the generic expressions for $V_{OUT_{k+}}$ and $V_{OUT_{k-}}$ in both operating phases, valid for every cell, the switches voltage stress can be estimated remembering that neighbouring cells work in the opposite phase and that V_{IN-} is the voltage reference. Considering once again the $k-th$ cell, phase one can be analysed first. The voltage stress on S_{ka} and S_{kn} can be estimated as

$$v_{S_{ka}} = V_{OUT_{k+}} - V_{OUT_{k-1+}} = (k+1)\,V_{IN} - (k-1)\,V_{IN} = 2V_{IN}$$

$$v_{S_{kn}} = V_{IN}$$

Considering phase two, the voltage stress on S_{kp} and S_{kb} can be calculated as

$$v_{S_{kp}} = V_{IN}$$

$$v_{S_{kb}} = V_{OUT_{k-1-}} - V_{OUT_{k-}} = -(k-1)\,V_{IN} + (k+1)\,V_{IN} = 2V_{IN}$$

In the $k = 1$ case, the equivalent circuit of the cell remains the same of the general situation (Fig.2.2.34 and 2.2.35), but the estimation of the input voltages $V_{OUT_{k-1+}}$ and $V_{OUT_{k-1-}}$ is straightforward. In fact, these two nodes coincide with V_{IN+} and V_{IN-} respectively. The switches voltage stress become then

$$v_{S_{1a}} = v_{S_{1n}} = v_{S_{1p}} = v_{S_{1b}} = V_{IN}$$

The characteristics of the nX converter can be expressed as a function of the maximum requested conversion ratio M:

- Number of switches
$$2M$$
- Number of flying capacitors
$$M$$
- Maximum switch voltage stress
$$2V_{IN}$$
- Maximum flying capacitor voltage
$$\frac{M}{2}V_{IN}$$

This topology is therefore characterized by a low and constant switches voltage stress, whose maximum value is equal to $2V_{IN}$, and a reduced output voltage resolution. In fact, due to its interleaved structure, the nX converter implements only even voltage conversion ratios. Voltage gains lower than the maximum one can be obtained simply keeping the unnecessary cells inactive (in parallel with the load or with the input).

2.2.6 Switched Capacitor Multilevel Converter Topologies Comparison

After studying the characteristics of the main multilevel switched capacitor converters it is possible to perform a comparison. The first goal is to understand which topology yields the highest conversion ratio for a given number

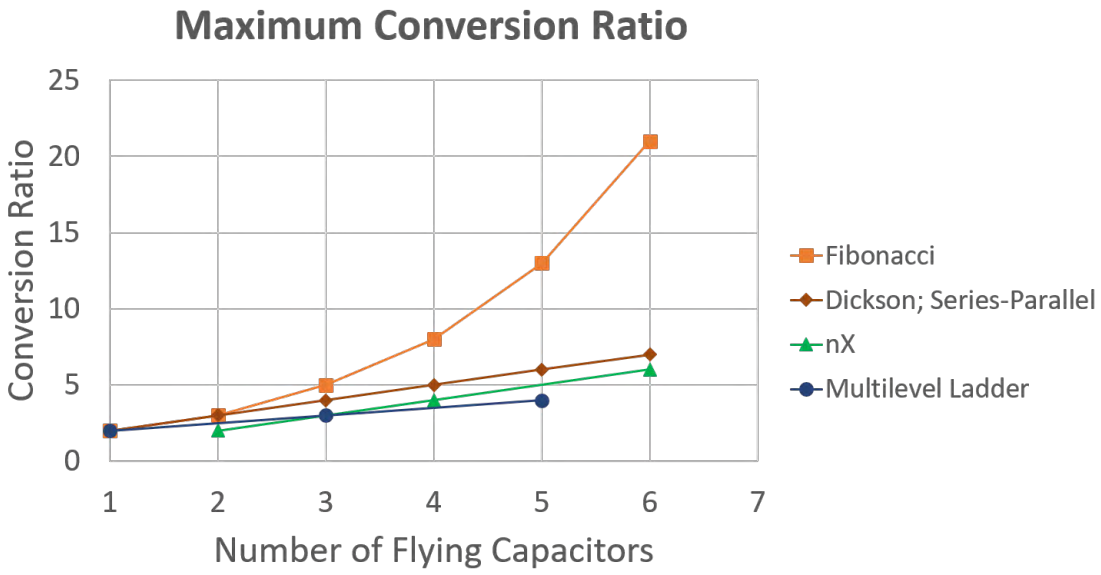


Figure 2.2.36: Maximum attainable conversion ratio for a given number of flying capacitors.

of flying capacitors. In Fig.2.2.36 the performances of the different converters are shown. The first thing that can be noticed is that the Fibonacci topology has clearly the highest gain, but the possible conversion ratios are limited to the numbers of the Fibonacci series, giving therefore a poor output voltage resolution. It is also interesting to notice that the multilevel ladder topology yields the lowest conversion ratio for a given number of capacitors, while the Dickson charge pump and the series-parallel converters have the same behaviour, with a voltage gain second only to the Fibonacci topology. The nX converter (the n times multiplier) gives a conversion ratio higher than the multilevel ladder only (if it is made of at least two cells).

After studying the maximum attainable conversion ratio, it is important to compare how the different converters characteristics depend on it (Table 2.2). First of all, it is interesting to analyse the number of switches needed to obtain a given conversion ratio M. As it is possible to see in Fig.2.2.37, the Dickson charge pump, multilevel ladder and series-parallel topologies all have the same performance. The nX and Fibonacci converter on the other hand, need less switches to obtain the same conversion ratio. The latter topology is thus the one that needs the least components to implement a converter

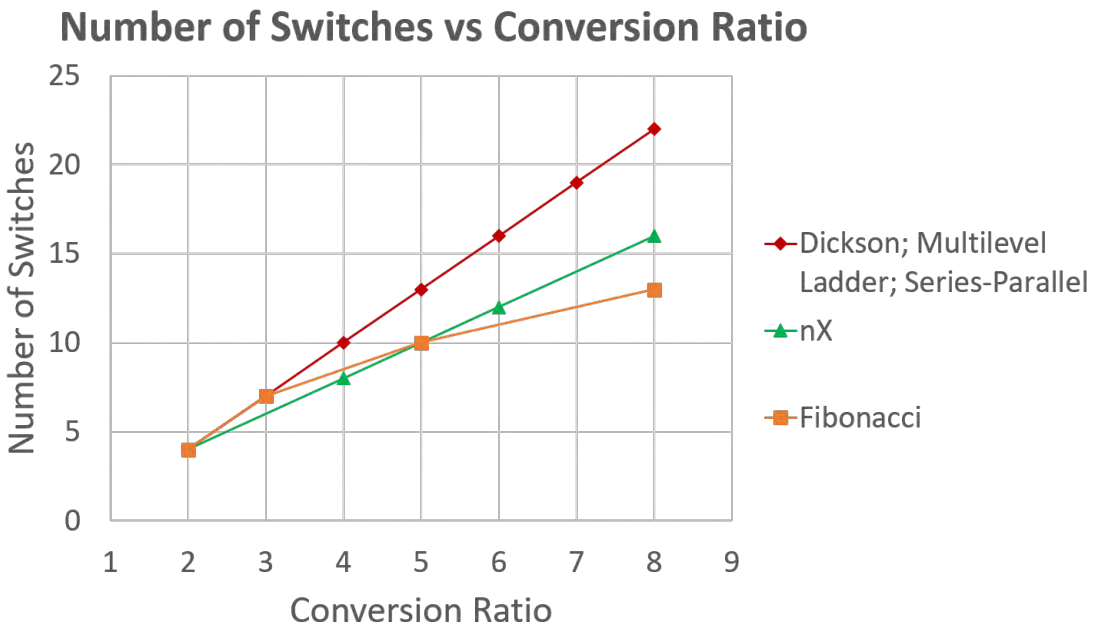


Figure 2.2.37: Number of switches needed to obtain a given maximum conversion ratio.

with a desired maximum conversion ratio.

All the analysed converters are anyway characterized by a high number of switches needed to obtain even moderate step up ratios, they are therefore more suitable for integrated applications.

After studying the number of switches required, the maximum voltage stress on the capacitors can be considered. In Fig.2.2.38 it is possible to observe how the multilevel ladder and series-parallel converters have the same voltage stress on every flying capacitor, equal to V_{IN}, while in all the other topologies the voltage stress increases with the requested conversion ratio. The Dickson charge pump is characterized by the highest stress, while the nX and Fibonacci topologies have intermediate behaviours.

Finally the switches voltage stress can be considered. Since, as previously said, switched capacitor converters are interesting mainly for integrated applications due to the high number of switches required and lack of inductor, this characteristic is more important than the capacitors voltage stress. Looking at Fig.2.2.39 it becomes instantly clear how the nX and Dickson charge

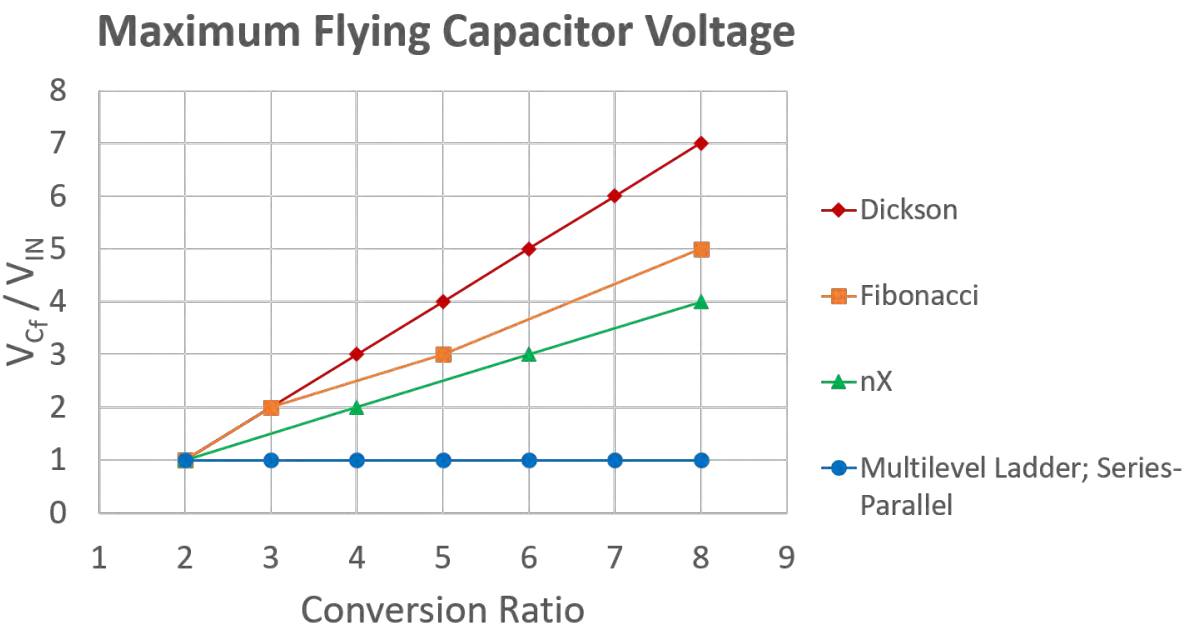


Figure 2.2.38: Maximum flying capacitors voltage stress for a given maximum conversion ratio.

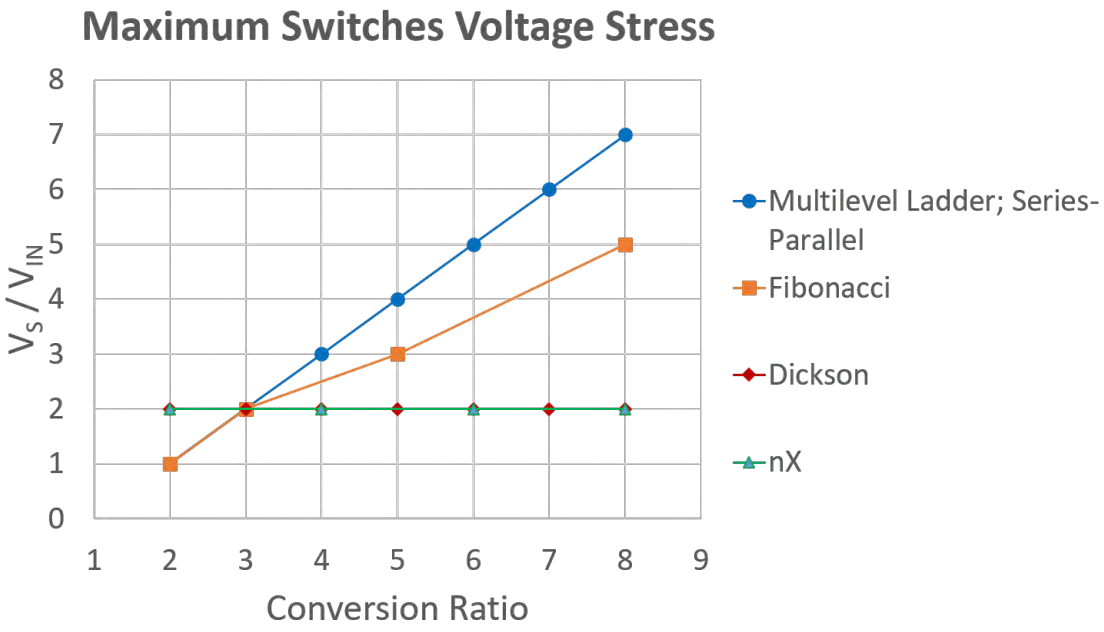


Figure 2.2.39: Switches voltage stress for a given maximum conversion ratio M.

pump topologies are the most interesting ones. In fact, these two converters are characterized by switches voltage stresses that do not depend on the implemented conversion ratio. On the other hand the multilevel ladder and the series-parallel have the worst performance, with a maximum switches voltage stress equal to $(M-1)\,V_{IN}$, while the Fibonacci converter has an intermediate behaviour, still dependent on the desired conversion ratio.

A deeper insight on the switches voltage stress can be gained observing table 2.1. This picture shows the maximum voltage stress and the number and values of the different voltage stress levels on the switches for every analysed topology. Once again it can be seen that the Dickson charge pump and nX converter have the best performance, while all the other topologies have a worse behaviour. In fact, the switches voltage stress depends on the requested conversion ratio and its maximum value increases with M.

An explicit comparison and resume of the converters characteristics can be seen in Table 2.2 and 2.3. In the first case the different parameters are expressed as a function of the maximum attainable conversion ratio M, in

	Series parallel	Fibonacci	nX Converter	Dickson	Multilevel Ladder
V_S max	$(M-1)V_{IN}$	$(M_{k-1})V_{IN}$	$2V_{IN}$	$2V_{IN}$	$(M-1)V_{IN}$
Number of voltage stress levels	M	$1+k^*$	2	2	M
Voltage Stress Levels	kV_{IN}; V_{IN}	F_k; F_{k-1}	V_{IN}; $2V_{IN}$	V_{IN}; $2V_{IN}$	V_{OUT}-kV_{IN}

Table 2.1: Switches voltage stress analysis.

	Series-parallel	Fibonacci	Multilevel Ladder	nX	Dickson
n_{C_f}	$M-1$	k^*	$2M-3$	M	$M-1$
n_S	$3M-2$	$3k^*+1$	$3M-2$	$2M$	$3M-2$
$\frac{V_{C_f}}{V_{IN}}$	1	F_k	1	$\frac{M}{2}$	$(M-1)$
$\frac{V_S}{V_{IN}}$	$(M-1)$	F_k	$(M-1)$	2	2

Table 2.2: Multilevel switched capacitor converters comparison: number of flying capacitors (n_{C_f}), number of switches (n_S), maximum normalized capacitor voltage ($\frac{V_{C_f}}{V_{IN}}$) and maximum normalized switches voltage stress ($\frac{V_S}{V_{IN}}$) as a function of the maximum conversion ratio implemented M; k^* is the index of M in the Fibonacci series.

the second they are expressed as a function of the number of employed flying capacitors k.

The former analysis remains valid if step down converters are considered. In this case the maximum conversion ratio M becomes the highest attainable step-down ratio.

After the analysis and comparisons carried out, some conclusions can be drawn:

- The Fibonacci topology guarantees the maximum conversion ratio for a given number of flying capacitors; it may be interesting where high conversion ratios are needed without much interest in the resolution

	Series-parallel	Fibonacci	Multilevel Ladder	nX	Dickson
n_S	$3k+1$	$3k+1$	$\frac{(3k+5)}{2}$	$2k$	$3k+1$
$\frac{V_{C_f}}{V_{IN}}$	1	F_k	1	$\frac{k}{2}$	k
$\frac{V_S}{V_{IN}}$	k	F_k	$\frac{(k+1)}{2}$	2	2
M_{MAX}	$k+1$	F_{k+1}	$\frac{(k+3)}{2}$	k	$k+1$

Table 2.3: Multilevel switched capacitor converters comparison: number of switches (n_S), maximum normalized capacitor voltage ($\frac{V_{C_f}}{V_{IN}}$) , maximum normalized switches voltage stress ($\frac{V_S}{V_{IN}}$) and maximum attainable conversion ratio (M_{MAX}) as a function of the number of employed flying capacitors k.

- The multilevel ladder topology yields the lowest conversion ratio for a given number of capacitors and loses the low voltage stress characteristic of its single-level version
- The nX converter has a low number of switches needed, intermediate performance in terms of the maximum attainable conversion ratio and low switches voltage stress; it may be interesting in cases where a lower resolution is not a problem
- The Dickson charge pump topology has intermediate properties and is interesting in multilevel applications because of its low constant switches voltage stress. It also has a better resolution than the nX converter.

2.2.7 Dickson Charge Pump FSL Equivalent Output Resistance Estimation

As it was shown in the previous section, the Dickson Charge Pump converter is the most interesting SC multilevel topology, due to its constant switches voltage stress and good resolution. It is therefore interesting to analyse its performance in terms of the best-case efficiency, estimating its FSL equivalent output resistance. To do so, the switches conduction losses must be analysed. Luckily, some hypothesis can be made to simplify the study: first of all, only steady-state operation is considered; second, as previously explained, in the FSL operational regime the capacitor currents can

be considered constant. The current flowing on a generic capacitor C_k in the converter operating phases A and B, having duration t_A and t_B respectively, will therefore have a constant value, that, in the following, will be indicated as $I_{C_{k(A)}}$ and $I_{C_{K(B)}}$ respectively. The two possible cases of a converter with an even and odd number of flying capacitors will be considered separately in the following.

Exploiting the previous hypotheses, defining a generic capacitor current as positive if it charges the capacitor itself, and remembering that in the Dickson charge pump topology neighbouring cells work in the opposite phase (meaning that when the generic capacitor C_k is charging, capacitors C_{k-1} and C_{k+1} are discharging), it is possible to write the following equation:

$$t_A I_{C_{k(A)}} + t_B I_{C_{k(B)}} = 0 \tag{2.2.7}$$

The previous expression provides then a relation between a given capacitor current value in the two operating phases, that is:

$$I_{C_{k(A)}} = -\frac{t_B}{t_A} I_{C_{k(B)}} \tag{2.2.8}$$

valid for every k comprised between 1 and the total number of flying capacitors N.

2.2.7.1 Even Number of Flying Capacitors Case

Let's consider the specific case of an even number N of flying capacitors, and define B as the output switch conduction phase and t_B as the output switch conduction time. It is then possible to identify B as every even capacitor discharging phase. B is in fact the last flying capacitor (C_N) discharging phase and, as previously explained, in this topology neighbouring cells work in opposite phases and this fact allows us to understand that even capacitors are all charging (and discharging) in the same phase. The same can be said of the odd capacitors, noting that if B is the even elements discharging phase, it is the odd elements charging one. It is then possible to derive the following expressions for every even k in between 2 and $N-2$:

$$I_{C_{k(A)}} = -I_{C_{k-1(A)}} \tag{2.2.9}$$

$$I_{C_{k(B)}} = -I_{C_{k+1(B)}} \tag{2.2.10}$$

Eq.(2.2.10), together with (2.2.8), can be used to obtain the following expression

$$-\frac{t_A}{t_B} I_{C_{k(A)}} = -I_{C_{k+1(B)}}$$

that, using (2.2.9), becomes

$$\frac{t_A}{t_B} I_{C_{k-1(A)}} = -I_{C_{k+1(B)}}$$

Once again exploiting the steady-state operation related equation (2.2.7), it is possible to finally write

$$I_{C_{k-1(B)}} = I_{C_{k+1(B)}} \tag{2.2.11}$$

Because of the FSL and steady-state operation hypotheses, it is therefore possible to write the following equation too

$$I_{C_{k-1(A)}} = I_{C_{k+1(A)}} \tag{2.2.12}$$

If an odd k is considered instead, it is possible to derive the following equations for k in between 1 and $N-1$:

$$I_{C_{k(A)}} = -I_{C_{k+1(A)}} \tag{2.2.13}$$

and

$$I_{C_{k(B)}} = -I_{C_{k-1(B)}} \tag{2.2.14}$$

Following the same procedure used in the even k case, expressions 2.2.11 and 2.2.12 can once again be obtained and are therefore valid for every k in between 1 and $N-1$.

It is also interesting to notice that, as shown in Fig.2.2.40, the current that flows on the output switch S_{OUT} is equal to the discharge current of the last $(N-th)$ flying capacitor. Assuming the convention shown in Fig.2.2.40 for the signs of the currents, under the assumptions made at the beginning of this section, it is then possible to write:

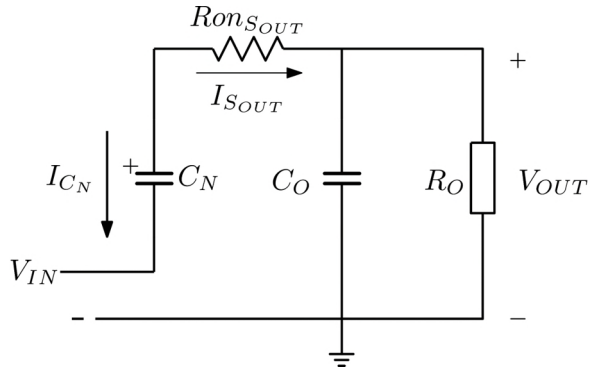


Figure 2.2.40: Output switch conduction phase.

$$I_{S_{OUT}} = -I_{C_{N(B)}} \tag{2.2.15}$$

Knowing eq.(2.2.15) and (2.2.11), it is possible to estimate the current in phase B for every flying capacitor as

$$I_{C_{k(B)}} = (-1)^{k+1} I_{S_{OUT}} \tag{2.2.16}$$

for k in between 1 and N. This finding allows to estimate I_{C_k} in phase A for every capacitor as:

$$I_{C_{k(A)}} = -\frac{t_B}{t_A} I_{C_{k(B)}} = -\frac{t_B}{t_A} (-1)^{k+1} I_{S_{OUT}} \tag{2.2.17}$$

After estimating every capacitor current value, it is possible to calculate the converter energy losses. To do so, the generic $k-th$ cell is considered (with $1 \leq k \leq N$). Fig.2.2.41 shows the cell charging phase, when the switches S_{1k} and S_{3k} are turned ON. In this case, defining the duration of the cell charging phase as t_{CH} to avoid a loss in generality, the energy can be expressed as

$$E_{CH} = \left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}} \right) I_{C_k}^2 t_{CH} \tag{2.2.18}$$

It is important to understand that t_{CH} can be either t_B or t_A depending on whether an odd or even cell is considered.

Analogously the discharging phase can be studied (Fig.2.2.42). In this case the conduction losses are given by

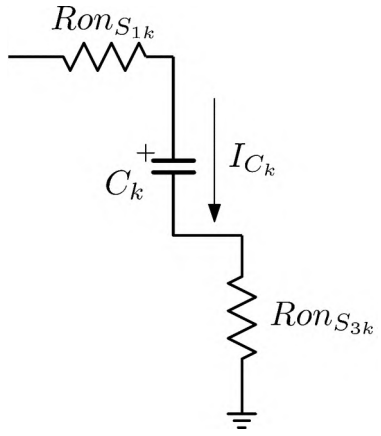


Figure 2.2.41: Generic $k-th$ cell charging phase.

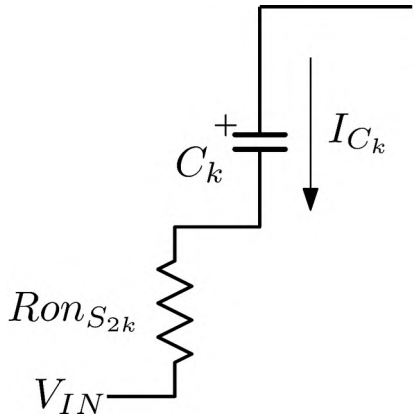


Figure 2.2.42: Generic $k-th$ cell discharging phase.

$$E_D = R_{on_{S_{2k}}} I_{C_k}^2 t_D \tag{2.2.19}$$

where t_D is the duration of the discharging phase, that once again can be t_B or t_A depending on whether an even or odd cell is considered.

The specific case of an even cell can now be studied. This cell capacitor is charging in phase A, therefore $t_{CH} = t_A$ and $t_D = t_B$. The energy loss equations become then

$$E_{CH} = \left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}}\right) I_{C_{k(A)}}^2 t_A$$

and

$$E_D = R_{on_{S_{2k}}} I^2_{C_{k(B)}} t_B$$

with k even and comprised between 2 and N.
Substituting (2.2.16) and (2.2.17) in the previous equations, we find

$$E_{CH} = \left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}} \right) I^2_{S_{OUT}} \frac{t_B^2}{t_A} \tag{2.2.20}$$

$$E_D = R_{on_{S_{2k}}} I^2_{S_{OUT}} t_B \tag{2.2.21}$$

In an analogous way, an odd cell can now be considered. Knowing $t_{CH} = t_B$ and $t_D = t_A$, eq.(2.2.18) and (2.2.19) become

$$E_{CH} = \left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}} \right) I^2_{S_{OUT}} t_B$$

$$E_D = R_{on_{S_{2k}}} I^2_{S_{OUT}} \frac{t_B^2}{t_A}$$

The energy loss on the output switch can be estimated considering Fig.2.2.40 and remembering that B was defined as the output switch conduction phase. The result is:

$$E_{S_{OUT}} = R_{on_{S_{OUT}}} I^2_{S_{OUT}} t_B \tag{2.2.22}$$

The energy loss equations previously derived have been expressed as a function of $I_{S_{OUT}}$, the current that flows on the output switch. Anyway this parameter can be expressed as a function of the load current. Looking at Fig.2.2.43 it is straightforward to derive the Kirchhoff current equations for the output node in both the converter operational phases:

$$Phase\, A: \quad i_{C_O} = -i_{LOAD}$$

$$Phase\, B: \quad I_{S_{OUT}} = i_{C_O} + i_{LOAD}$$

Remembering the FSL and steady-state operation hypotheses, assuming that C_O is large enough to keep the output voltage approximately constant,

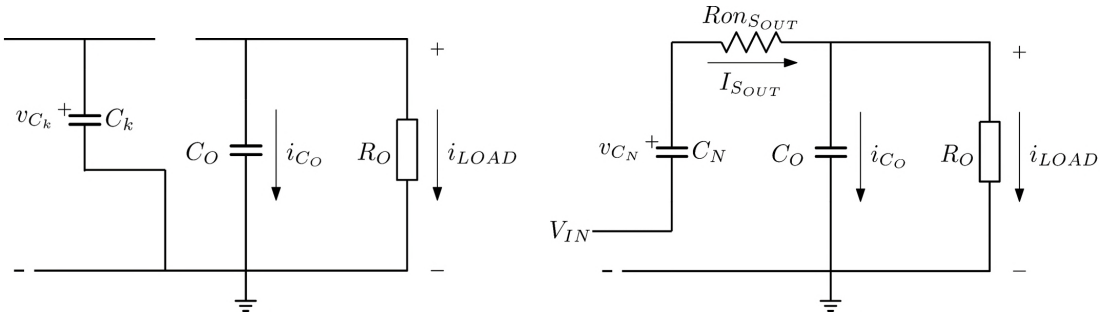


Figure 2.2.43: Output node KCL derivation: equivalent circuit in phase A (left) and B (right).

and calling I_{LOAD} the load current average value, it is possible to derive the following equation:

$$I_{S_{OUT}} = \frac{(t_A + t_B)}{t_B} I_{LOAD} \tag{2.2.23}$$

In fact, Since C_O was supposed to be large enough to keep the output voltage constant, also the load current is, giving the following equation:

$$i_{LOAD} = constant = \overline{i_{LOAD}} = I_{LOAD} \tag{2.2.24}$$

Due to the steady state hypothesis, C_O average current is zero, therefore $\overline{i_{S_{OUT}}} = I_{LOAD}$. Furthermore, due to the FSL operation, $i_{S_{OUT}(B)} = I_{S_{OUT}} = constant$, therefore $i_{S_{OUT}}$ average value can be easily estimated as

$$\overline{i_{S_{OUT}}} = \frac{t_B}{(t_A + t_B)} I_{S_{OUT}}$$

Exploiting this relation, and knowing $\overline{i_{S_{OUT}}} = I_{LOAD}$, eq.(2.2.23) is obtained. Defining $T_S = t_A + t_B$ the converter switching period, equation (2.2.23) becomes

$$I_{S_{OUT}} = \frac{T_S}{t_B} I_{LOAD} \tag{2.2.25}$$

To estimate the total energy losses, the different cells contributions must be summed, giving:

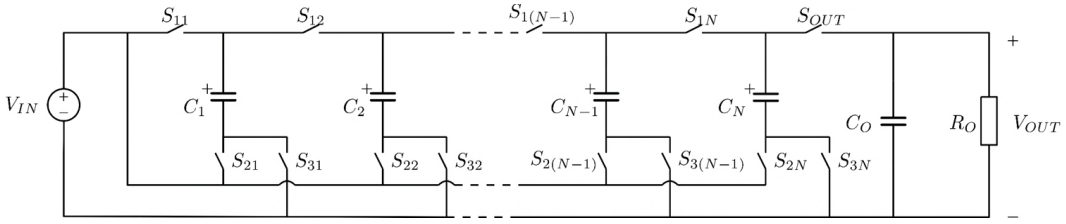


Figure 2.2.44: Generic N cells Dickson charge pump converter.

$$E_{LOST} = \left\{ \begin{array}{c} \sum_{k\ even} \left[\left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}} \right) I_{S_{OUT}}^2 \frac{t_B^2}{t_A} + R_{on_{S_{2k}}} I_{S_{OUT}}^2 t_B \right] + \\ \sum_{k\ odd} \left[\left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}} \right) I_{S_{OUT}}^2 t_B + R_{on_{S_{2k}}} I_{S_{OUT}}^2 \frac{t_B^2}{t_A} \right] + R_{on_{S_{OUT}}} I_{S_{OUT}}^2 t_B \end{array} \right\}$$

The previous equation can be written as

$$E_{LOST} = I_{S_{OUT}}^2 t_B^2 \left\{ \begin{array}{c} \sum_{k\ even} \left[\left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}} \right) \frac{1}{t_A} + R_{on_{S_{2k}}} \frac{1}{t_B} \right] + \\ \sum_{k\ odd} \left[\left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}} \right) \frac{1}{t_B} + R_{on_{S_{2k}}} \frac{1}{t_A} \right] + R_{on_{S_{OUT}}} \frac{1}{t_B} \end{array} \right\}$$

Eq. (2.2.25) gives $I_{S_{OUT}} t_B = T_S I_{LOAD}$. Using this information we finally get

$$E_{LOST} = i_{LOAD}^2 T_S^2 \left\{ \begin{array}{c} \sum_{k\ even} \left[\left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}} \right) \frac{1}{t_A} + R_{on_{S_{2k}}} \frac{1}{t_B} \right] + \\ \sum_{k\ odd} \left[\left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}} \right) \frac{1}{t_B} + R_{on_{S_{2k}}} \frac{1}{t_A} \right] + R_{on_{S_{OUT}}} \frac{1}{t_B} \end{array} \right\} \quad (2.2.26)$$

After evaluating the energy dissipated due to conduction losses, the equivalent output resistance can be estimated. Looking at the generic switched-capacitor converter equivalent model (Fig.2.2.45) it is in fact straightforward to derive the following expression:

$$E_{LOST} = \int_0^{T_S} R_{OUT} i_{LOAD}^2 dt \quad (2.2.27)$$

Knowing that

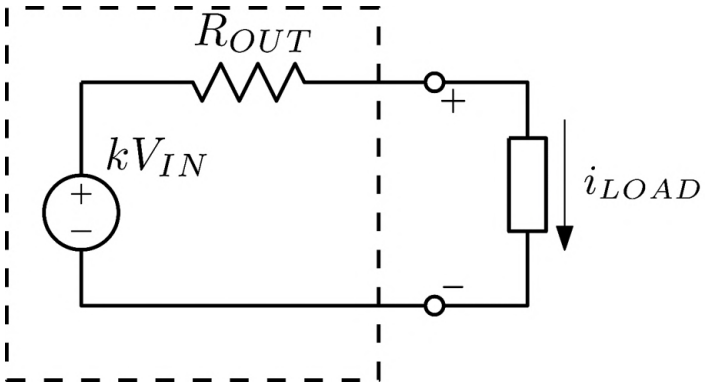


Figure 2.2.45: Generic switched capacitor converter equivalent model.

$$i_{LOAD} = constant = I_{LOAD}$$

eq.(2.2.27) becomes

$$E_{LOST} = \int_0^{T_S} R_{OUT} i_{LOAD}^2 dt = T_S R_{OUT} I_{LOAD}^2$$

The equivalent output resistance can therefore be estimated as

$$R_{OUT} = \frac{E_{LOST}}{T_S I_{LOAD}^2} \tag{2.2.28}$$

Substituting (2.2.26) in (2.2.28) the following expression for R_{OUT} is obtained:

$$R_{OUT} = T_S \left\{ \begin{array}{c} \sum_{k\ even} \left[\left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}} \right) \frac{1}{t_A} + R_{on_{S_{2k}}} \frac{1}{t_B} \right] + \\ \sum_{k\ odd} \left[\left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}} \right) \frac{1}{t_B} + R_{on_{S_{2k}}} \frac{1}{t_A} \right] + R_{on_{S_{OUT}}} \frac{1}{t_B} \end{array} \right\} \tag{2.2.29}$$

2.2.7.2 Odd Number of Flying Capacitors Case

Analogously to the previous case, defining B as the output switch conduction phase and being this switch turned ON during the last capacitor discharge

period, since neighbouring cells work in alternative, every flying capacitor C_k with k odd is discharging in phase B, while it is charging in phase A. For the same reason every C_k with k even is charging in phase B and discharging in phase A. It is then possible to derive the following expression for every odd k in between 3 and N

$$I_{C_{k(A)}} = -I_{C_{k-1(A)}} \tag{2.2.30}$$

and the following equation for every odd k in between 1 and $N-2$

$$I_{C_{k(B)}} = -I_{C_{k+1(B)}}$$

As seen in the even number of cells case, once again the FSL and steady-state operation hypotheses allow to calculate the capacitor currents in both phases, obtaining

$$I_{C_{k+1(A)}} = I_{C_{k-1(A)}}$$

with k odd and comprised between 3 and $N-2$. Combining the previous equation with (2.2.30), knowing that the discharge current of the last flying capacitor coincides with the output switch current, and exploiting once again the steady-state operation hypothesis, we get:

$$\mid I_{C_{k(B)}} \mid = I_{S_{OUT}}$$

$$\mid I_{C_{k(A)}} \mid = \frac{t_B}{t_A} \mid I_{C_{k(B)}} \mid = I_{S_{OUT}}$$

for every k in between 1 and N.

The energy losses in the generic $k-th$ cell, with $1 \leq k \leq N$, are still expressed by (2.2.18) and (2.2.19). In an odd cell case, being $t_{CH} = t_A$ and $t_D = t_B$, these equations become

$$E_{CH} = \left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}} \right) \frac{t_B^2}{t_A} I_{S_{OUT}}^2$$

$$E_D = R_{on_{S_{2k}}} I_{S_{OUT}}^2 t_B$$

In an even cell case instead

$$E_{CH} = \left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}}\right) I^2_{S_{OUT}} t_B$$

$$E_D = R_{on_{S_{2k}}} \frac{t_B^2}{t_A} I^2_{S_{OUT}}$$

The output switch conduction losses are still expressed by

$$E_{S_{OUT}} = R_{on_{S_{OUT}}} I^2_{S_{OUT}} t_B$$

Since the considerations made in the even total number of cells case about the relation between $I_{S_{OUT}}$ and the average load current I_{load} still apply, the total energy conduction losses are given by:

$$E_{LOST} = I^2_{LOAD} T_S^2 \left\{ \begin{array}{c} \sum_{k\ even} \left[\left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}}\right) \frac{1}{t_B} + R_{on_{S_{2k}}} \frac{1}{t_A}\right] + \\ \sum_{k\ odd} \left[\left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}}\right) \frac{1}{t_A} + R_{on_{S_{2k}}} \frac{1}{t_B}\right] + R_{on_{S_{OUT}}} \frac{1}{t_B} \end{array} \right\} \tag{2.2.31}$$

Also in this case the equivalent output resistance can be estimated as

$$R_{OUT} = \frac{E_{LOST}}{T_S I^2_{LOAD}} \tag{2.2.32}$$

Substituting (2.2.31) in (2.2.32) the following expression for R_{OUT} is thus obtained:

$$R_{OUT} = T_S \left\{ \begin{array}{c} \sum_{k\ even} \left[\left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}}\right) \frac{1}{t_B} + R_{on_{S_{2k}}} \frac{1}{t_A}\right] + \\ \sum_{k\ odd} \left[\left(R_{on_{S_{1k}}} + R_{on_{S_{3k}}}\right) \frac{1}{t_A} + R_{on_{S_{2k}}} \frac{1}{t_B}\right] + R_{on_{S_{OUT}}} \frac{1}{t_B} \end{array} \right\} \tag{2.2.33}$$

2.2.7.3 Notable Cases

Equations (2.2.29) and (2.2.33) allow to estimate the equivalent output resistance of a Dickson charge pump converter in any case, but they are not easy to interpret at a first glimpse. In order to get more information on the behaviour of the converter, some specific cases of interest are studied.

First of all it is important to recall that, as shown in the previous sections, switched capacitor converters have a fixed conversion ratio determined by the topology. Furthermore, when the duty cycle becomes too low or too high, the converter efficiency significantly drops. It is then pretty sensible to assume for a switched capacitor converter to be operated with a fixed fifty per cent duty cycle. In this case $t_A = t_B$, and the equivalent output resistance expressions become:

$$R_{OUT_{even}} = R_{OUT_{odd}} = 2 \left\{ \begin{array}{c} \sum_{k\,even} \left[R_{on_{S_{1k}}} + R_{on_{S_{3k}}} + R_{on_{S_{2k}}} \right] + \\ \sum_{k\,odd} \left[R_{on_{S_{1k}}} + R_{on_{S_{3k}}} + R_{on_{S_{2k}}} \right] + R_{on_{S_{OUT}}} \end{array} \right\}$$

Under the assumption $t_A = t_B$, the equivalent output resistance expression is the same both in the even and odd number of flying capacitors case.

Another important thing to remember is that the Dickson charge pump topology is characterized by fixed switches voltage stress. Referring to Fig.2.2.23, the voltage stress on the different switches can be resumed as:

- $v_{S_{1k}} = 2V_{IN}$ for $k > 1$
- $v_{S_{2k}} = v_{S_{3k}} = V_{IN}$ for every k
- $v_{S_{11}} = V_{IN}$

Knowing that the voltage stress on the output switch is $v_{S_{OUT}} = V_{IN}$, and calling R_{ON} the ON-resistance of a switch sized to withstand a voltage stress equal to V_{IN}, it is then sensible to hypothesize that the converter switches have the following on-resistances:

- $R_{on_{S_{1k}}} = 2R_{ON}$ for $k > 1$
- $R_{on_{S_{2k}}} = R_{ON}$ for every k
- $R_{S_{11}} = R_{ON}$
- $R_{on_{S_{OUT}}} = R_{ON}$

Under this assumption the equivalent output resistance becomes

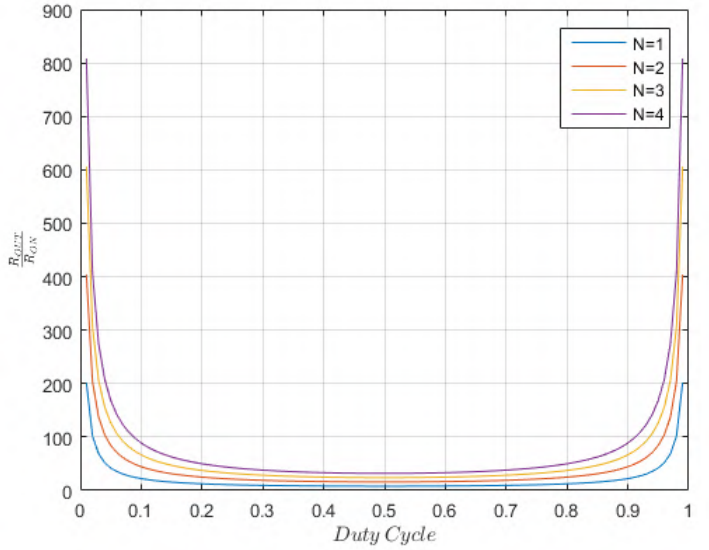


Figure 2.2.46: Dickson charge pump equivalent output resistance as a function of the duty cycle D for different total number of cells N.

$$R_{OUT_{even}} = R_{OUT_{odd}} = 2NR_{ON}\left(\frac{1}{t_A} + \frac{1}{t_B}\right)T_S$$

where N is the total number of cells (thus of flying capacitors) of the converter. It is interesting to notice that, also in this case, the expression that gives the equivalent output resistance is the same in both the even and odd number of flying capacitors case.

Defining the duty cycle as $D = \frac{t_B}{T_S}$ the previous equations can be written as

$$R_{OUT} = 2NR_{ON}\left(\frac{1}{(1-D)} + \frac{1}{D}\right) \tag{2.2.34}$$

The dependence of the Dickson charge pump equivalent output resistance on the duty cycle can now be studied. Fig.2.2.46 shows how R_{OUT} normalized to R_{ON} varies with D, for converters with different number of total cells N.

In the case the duty cycle is fixed to fifty per cent, equation (2.2.34) becomes

$$R_{OUT} = 8NR_{ON}$$

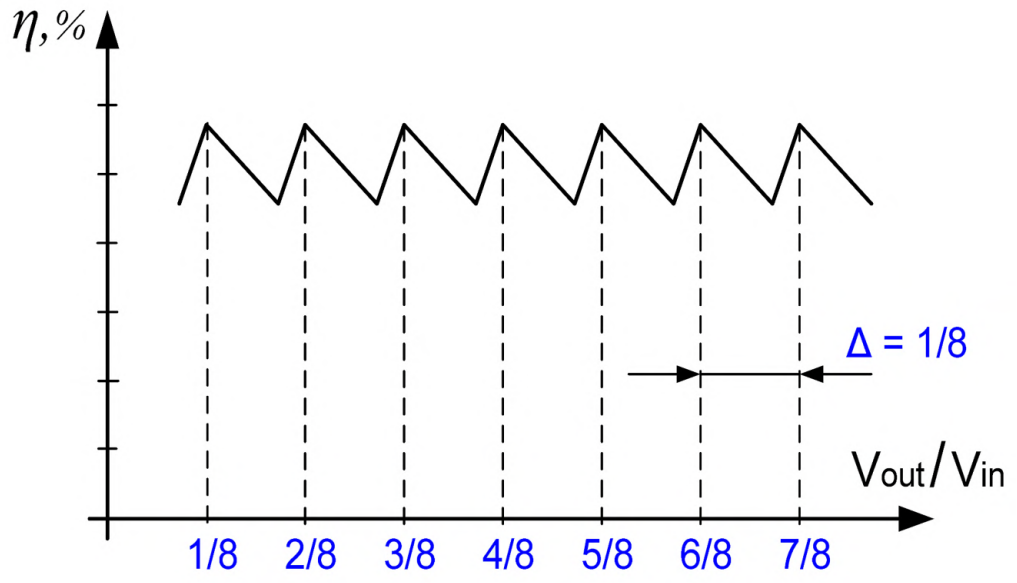


Figure 2.2.47: Example of a typical efficiency curve in a regulated multilevel SCC.

This is the best case equivalent output resistance under the previous assumptions. A simulation of the converter was performed using PLECS and the previous result was confirmed.

2.2.8 Notes on Multilevel SCCs and Output Voltage Regulation

The use of a multilevel SCC can be interesting not only to improve the attainable conversion ratios range, but also to improve the converter efficiency. As previously mentioned in fact, a switched capacitor converter efficiency is maximum when the requested conversion ratio coincides with the topology nominal one. The implementation of multiple possible conversion ratios is therefore an interesting way to reduce the requested regulation range. In fact, when adopting for example a duty cycle modulation technique in combination with a multilevel topology, the efficiency curve will typically look like the one shown in Fig.2.2.47. This picture shows the case of a step-down converter with seven possible conversion ratios and a resolution equal to $\frac{1}{8}V_{IN}$.

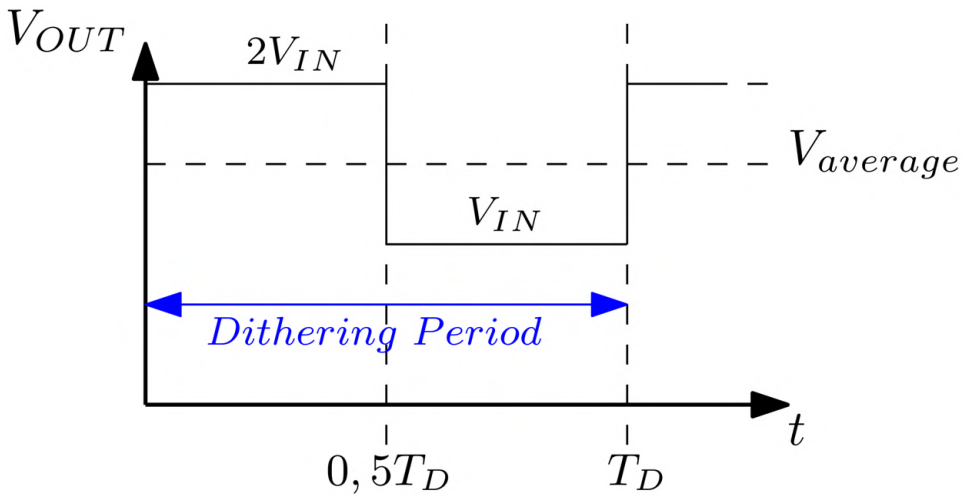


Figure 2.2.48: Example of output voltage regulation through the technique called *dithering*.

Another interesting technique that can be used to regulate the output voltage continuously when using a multilevel SCC, is the so called dithering. In this case the average output voltage is regulated by changing the conversion ratio between the values allowed by the topology. In Fig.2.2.48 an example of this technique is given. T_D is the so called dithering period, the desired conversion ratio is $M = 1.5$ and the closest ones implemented by the SCC are one and two. In this case, as shown in the picture, the converter operates with a conversion ratio equal to two for the first half of the dithering period, and to one in the second half. The average conversion ratio will therefore be equal to one and a half as requested. This technique has the advantage of allowing the converter to work in its theoretical maximum efficiency points, but the output voltage ripple will be equal to the converter resolution.

Chapter 3

Hybrid DC-DC Converters

Hybrid DC-DC Converters Review

Hybrid converters are circuits that mix the switched-capacitor/charge pump approach with "standard" inductor based topologies. The goal in doing this, is to exploit the higher energy density of capacitors to reduce the overall converter size and magnetic requirements in comparison with an equivalent standard inductor based topology. This is also a way of overcoming the switched capacitor converters main limitation while keeping an "integration friendly" approach.

Different approaches can be used to obtain a hybrid converter:

- Cascading and merging different topologies
- Parallel input serial output topologies
- Inserting charge pump sub-circuits inside standard topologies

It is important to notice that, as will be shown in chapter three, the charge pump and inductor actions can also be totally mixed in the converter operation, obtaining totally new converters.

In the following, some examples of the previous approaches that can be found in literature are shown to get a deeper understanding of the fundamental characteristics and principles that drive hybrid converters operation.

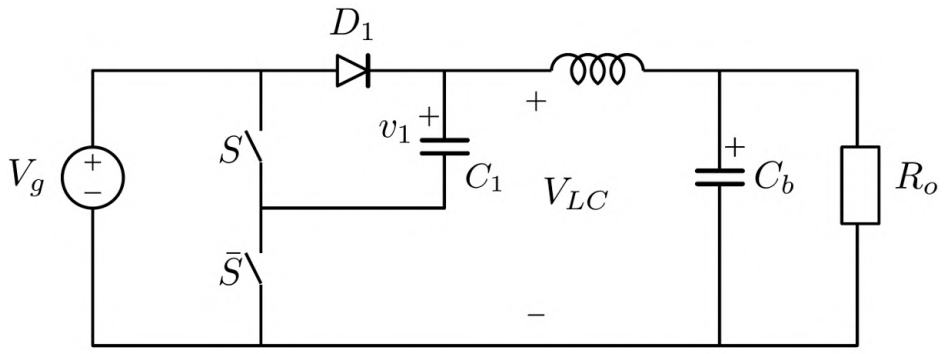


Figure 3.1.1: KY converter.

3.1 Cascading and Merging of Switched-Capacitor and Inductor Based Topologies

3.1.1 KY Converter

An example of the cascading/merging of a switched capacitor circuit with an inductor based one, is the so called "KY converter"[4]. This topology, shown in Fig.3.1.1, is obtained cascading a charge pump cell with a buck converter. It is important to notice that the buck stage switch and diodes are shared with the charge pump cell, so that the KY converter can be seen as a charge pump cell with an LC filter in series that averages the voltage at its input, just like in a buck converter. In this hybrid topology anyway, the filter input voltage varies between V_g and $2V_g$ (instead of changing between 0 and the input voltage); like in a buck converter anyway, it is the choice of the duty cycle that determines the conversion ratio, that in fact is given by the following equation:

$$M = 1 + D \tag{3.1.1}$$

To gain a better understanding on the matter, the operation of this converter is shown in detail. Phase $\overline{S}$ is considered first (Fig.3.1.2). In this phase diode D_1 is conducting and capacitor C_1 is charged to V_g, the same as the voltage V_{LC} applied to the output filter. In phase S instead (Fig.3.1.3), capacitor C_1 is connected in series with the input source, so that $V_{LC} = V_g + v_1 = 2V_g$. Drawing V_{LC} waveform, Fig.3.1.4, allows to straightforwardly estimate its

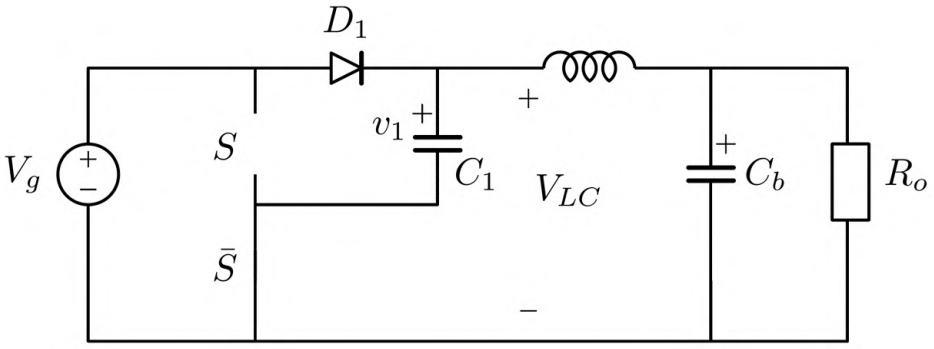


Figure 3.1.2: KY converter: phase A.

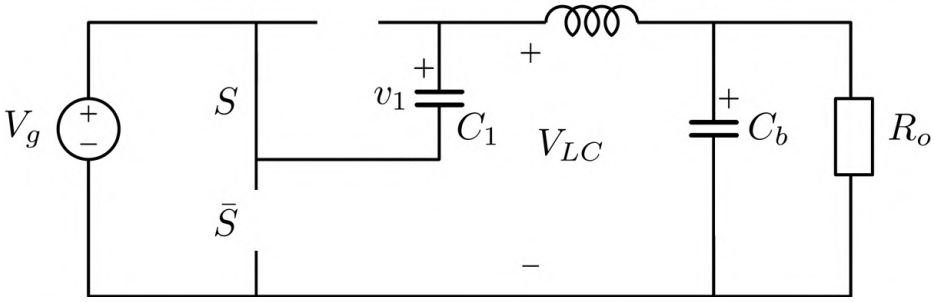


Figure 3.1.3: KY converter: phase B.

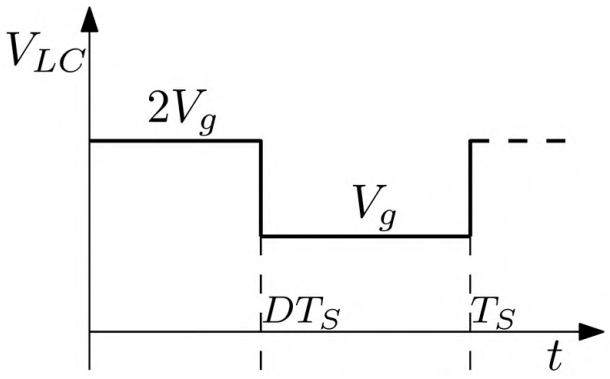


Figure 3.1.4: V_{LC} waveform.

average value, that corresponds to the converter output voltage.

$$V_o = \frac{2V_g DT_S + V_g (1-D) T_S}{T_S} = 2DV_g + (1-D) V_g = V_g (1+D)$$

We have therefore derived the expression for the conversion ratio presented in eq.(3.1.1).

It is now interesting to analyse the voltage stress on the devices. Considering the equivalent circuits in the two operating phases (Fig.3.1.2 and 3.1.3), it is possible to estimate the voltage stress as:

$$v_S = v_{\overline{S}} = V_g$$

$$v_{D_1} = v_1 = V_g$$

It is then interesting to notice that a step up converter was implemented, even if with a limited conversion ratio range, and that its switching devices voltage stress is reduced if compared with a standard equivalent boost; in the latter case, the voltage stress is in fact equal to the output voltage. Therefore in the hybrid topology the switching devices stress is reduced of a factor M (the conversion ratio). This characteristic is interesting not only because it allows to use smaller devices, but also because it reduces the switching losses, thus allowing to push the switching frequency higher, reducing the inductor size. Given the focus on the inductor size reduction, it is also interesting

to evaluate the inductor current ripple and average value under steady-state operation hypothesis. The inductor current ripple can be estimated as

$$\Delta i_L = \frac{(2V_g - V_{out})}{Lf_S} D = \frac{(2-M)(M-1)}{Lf_S} V_g$$

Calculating the derivative allows to estimate $M = 1.5$ as the value that maximizes the ripple, whose worst case value is then given by

$$\Delta i_{L-wc} = \frac{V_g}{4Lf_S}$$

On the other hand, in an equivalent boost converter case, the inductor current ripple is given by

$$\Delta i_{L\,boost} = \frac{V_g}{Lf_S} D = \frac{V_g}{Lf_S} \frac{(M-1)}{M}$$

Given that the KY converter maximum theoretical conversion ratio is equal to two, the worst case inductor current ripple is then

$$\Delta i_{L-boost\,wc} = \frac{V_g}{Lf_S} \frac{(M_{MAX}-1)}{M_{MAX}} = \frac{V_g}{2Lf_S}$$

The hybrid topology yields a reduction of the worst case inductor current ripple to (theoretically) half the value in an equivalent boost case. Nevertheless, it must be noted that in practice duty cycle limitations imposed by the charge-pump cell limit the maximum and minimum attainable conversion ratio. As the duty cycle approaches 0 or 100% in fact, the charge-pump cell efficiency dramatically decreases. M_{MAX} will then be lower than the theoretical value of two and as a consequence the worst-case equivalent boost inductor current ripple will also be lower, reducing the hybrid topology advantage The average inductor current is now considered. Under steady-state operation hypothesis the mean capacitor currents are zero. Looking at Fig.3.1.1 it is therefore easy to understand that, in the KY converter, the average inductor current is equal to the mean load current. In the boost case instead, the inductor average current is the mean input current. Making the hypothesis of an ideal lossless converter, the following relation between the average input and load currents I_{in} and I_{load} can be derived:

$$P_{in} = I_{in}V_g = P_{out} = V_{out}I_{load}$$

The previous equation can be used to derive the following

$$I_{in} = \frac{V_{out}}{V_g} I_{load}$$

Therefore

$$I_{in} = M I_{load}$$

Being the KY converter a step-up topology, the previous equation tells us that this hybrid circuit allows a reduction of the average inductor current of a factor equal to the conversion ratio.

Overall the KY converter allows to implement a step-up topology with a maximum voltage gain equal to two, with reduced maximum voltage stress, inductor current ripple and average value if compared to an equivalent standard boost topology, it is therefore a good example of how a hybrid approach can help improving these aspects while introducing a trade-off with the converter complexity.

3.1.2 Second Order KY Converter

The approach described in the previous section can be iterated using multiple stages in cascade. An example of this is given by the so called "second order KY converter", obtained cascading two switched capacitor cells and an LC filter.

Adding a second switched capacitor cell not only increases the possible voltage gain of the converter, but also allows different operating modes that can be selected varying the switches modulation law. The first possible operating mode is shown in Fig.3.1.5. In phase $\overline{S}$ (Fig.3.1.6) both the diodes D_1 and D_2 are conducting and the charge pump stages capacitors are charged to V_g. The output filter input voltage V_{LC} is therefore equal to the input voltage V_g. In phase S instead (Fig.3.1.7), the charge pump action takes place and capacitors C_1 and C_2 are connected in series, so that $V_{LC} = V_g + v_1 + v_2 = 3V_g$.

The converter output voltage is given by the average of V_{LC} over the switching period and, defining DT_S as the duration of phase $\overline{S}$, can be estimated as

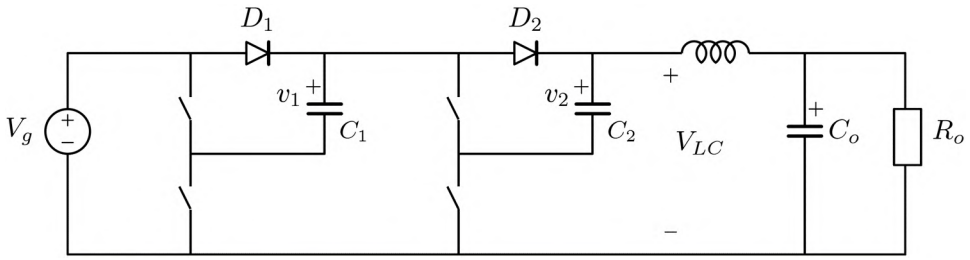


Figure 3.1.5: Second order KY converter: first possible operating mode.

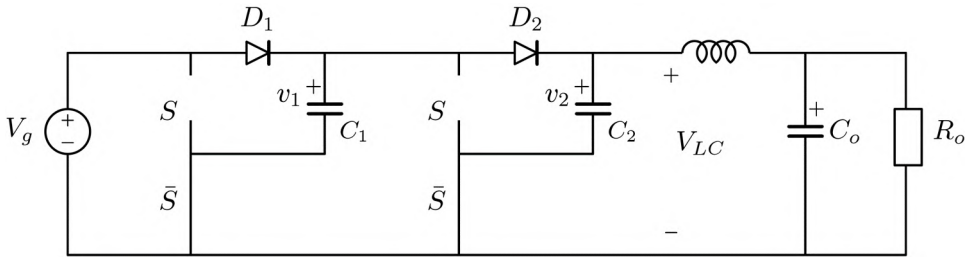


Figure 3.1.6: Second order KY converter: first possible operating mode, S phase equivalent circuit.

$$V_{out} = \overline{V_{LC}} = \frac{3V_g DT_S + V_g (1-D) T_S}{T_S} = (1+2D) V_g$$

The conversion ratio is then equal to

$$M = 1 + 2D$$

The switching devices voltage stress can now be estimated. Once again considering Fig.3.1.6 and 3.1.7, it is possible to write the following equations:

$$V_{\overline{s_1}} = V_g$$

$$V_{\overline{s_2}} = V_g + v_1 = 2V_g$$

$$v_{D_1} = v_{S_1} = v_1 = V_g$$

$$v_{D_2} = v_{S_2} = v_2 = V_g$$

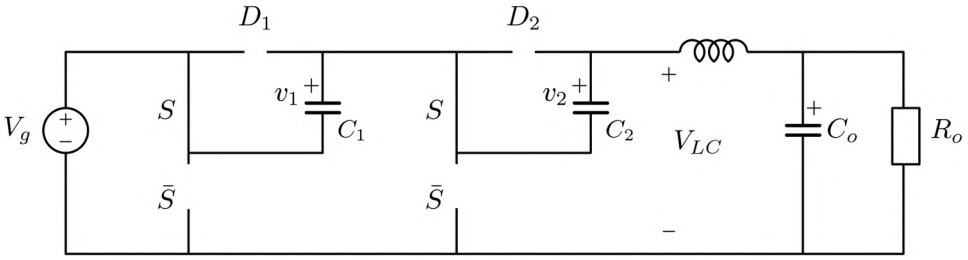


Figure 3.1.7: Second order KY converter: first possible operating mode $\overline{S}$ phase equivalent circuit.

The inductor current ripple can now be calculated, obtaining the following equation:

$$\Delta i_L = \frac{(3V_g - V_{out})\,D}{Lf_S} = \frac{V_g}{Lf_S}\frac{(3-M)\,(M-1)}{2}$$

Estimating the previous function derivative, it is possible to find the value of M corresponding to the worst case scenario, and that value is 2. In this case, the previous equation becomes

$$\Delta i_{L-worst\,case} = \frac{V_g}{2Lf_S}$$

In an equivalent boost case instead, since the maximum theoretical conversion ratio in this case is equal to three, the worst case inductor current ripple would be equal to

$$i_{L-boost\,wc} = \frac{V_g}{Lf_S}\frac{(M_{MAX}-1)}{M_{MAX}} = \frac{2}{3}\left(\frac{V_g}{Lf_S}\right) \tag{3.1.2}$$

Therefore, the hybrid topology grants a reduction of the worst-case inductor current ripple, even though it must be noticed that the considerations made in the standard KY converter case, regarding the duty cycle value and subsequent conversion ratio limitations, also apply in the second order converter case.

As seen in the first order KY converter analysis, also in the second order one case, under steady state operation hypothesis, the average inductor current equals the average load current. All the calculations made in the previous case remain then valid and the average inductor current, and consequently

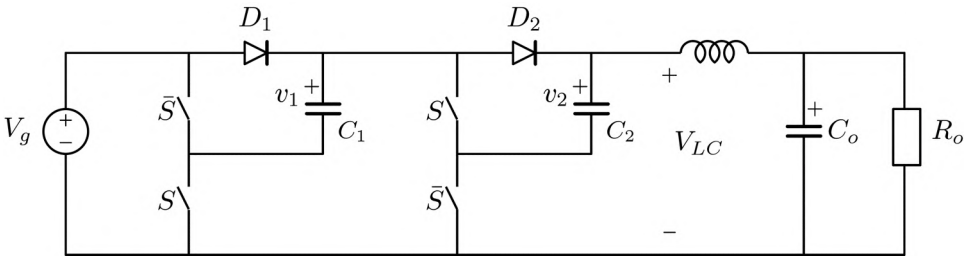


Figure 3.1.8: Second order KY converter: second possible operating mode.

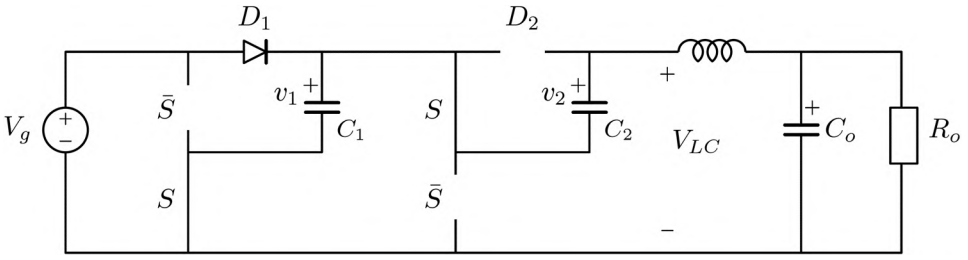


Figure 3.1.9: Second order KY converter: second possible operating mode S phase.

the magnetic element requirements, are therefore reduced with respect to an equivalent standard boost.

The second possible modulation law for the converter is shown in Fig.3.1.8. In this case the capacitors C_1 and C_2 charge to different voltages. Looking at Fig.3.1.9 it is in fact possible to notice that in phase S, C_1 is charged to V_g while C_2 is discharging. In this phase we can write the following equation for the output filter input voltage:

$$V_{LC} = V_g + v_2 \tag{3.1.3}$$

Analysing phase $\overline{S}$ equivalent circuit instead (Fig.3.1.10), it is possible to see how during this phase C_2 is charged by the series of V_g and C_1. It is then possible to estimate its charging voltage as

$$v_2 = V_g + v_1 = 2V_g \tag{3.1.4}$$

Substituting eq.(3.1.4) in (3.1.3) it is then possible to estimate V_{LC} during phase S, that is equal to $3V_g$.

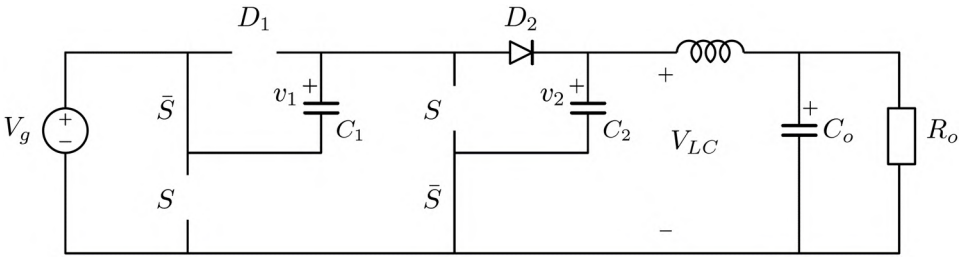


Figure 3.1.10: Second order KY converter: second possible operating mode $\overline{S}$ phase.

Knowing the values of V_{LC} in both of the operating phases, it is possible to determine the output voltage as V_{LC} average value.

$$V_{out} = \frac{3V_g DT_S + 2V_g (1-D) T_S}{T_S} = (2+D) V_g$$

The voltage conversion ratio is then equal to:

$$M = 2 + D$$

The switching devices voltage stress can now be evaluated. Once again considering Fig.3.1.9 and 3.1.10, it is possible to write the following equations:

$$v_{\overline{S_1}} = v_{\overline{S_2}} = v_{S_1} = V_g$$

$$v_{D_2} = v_{s_2} = v_2 = 2V_g$$

$$v_{D_1} = v_1 = V_g$$

The second order KY converter is therefore characterized by a step-up conversion ratio whose maximum value is three, while the maximum switching devices voltage stress is equal to $2V_g$, a lower value if compared to an equivalent boost converter, where the voltage stress is equal to the output voltage.

The inductor current ripple can now be analysed, obtaining the following equation:

$$\Delta i_L = \frac{(3V_g - V_{out}) D}{Lf_S} = \frac{V_g}{Lf_S} (3-M)(M-2)$$

Calculating the previous function derivative allows to estimate the value of M corresponding to the current ripple worst case, and that value is 2.5. It is then possible to estimate the worst case inductor current ripple, given by

$$\Delta i_{L-worst\,case} = \frac{V_g}{4Lf_S}$$

The same considerations regarding the average inductor current drawn in the first possible modulation law case apply here. Therefore, also in this case, the magnetic element requirements are reduced.

Overall the second order KY converter implements a step-up topology with a reduced average inductor current and switching devices voltage stress (in the worst case situation), it is therefore a nice example of how hybrid topologies can be used to meet these goals, even if these improvements introduce a trade-off with the circuit complexity and the number of components used.

3.2 Series-Parallel and Buck Cascaded Hybrid Converter

Another example of the approach used to derive the KY converter is shown in Fig.3.2.1. This topology, presented in [5], is obtained cascading a switched capacitor voltage divider stage and a buck converter. This solution however is not a simple cascade, but it also tries to mix the inductor and capacitor based approaches. In fact, as it can be seen in Fig.3.2.1, the switch identified as S_b acts both as the free-wheeling diode for the buck and as part of the step-down switched capacitor stage. A better understanding of how this topology works can be gained considering the converter equivalent circuits during the three different operating phases. Fig.3.2.2 shows the converter first operating phase. During this time the flying capacitors are charged to $\frac{1}{3}V_{in}$, while the buck stage is in its off-phase. In phase two instead (Fig.3.2.3), the buck is in its on-phase, and the series-parallel stage is delivering energy to its output. The flying capacitors are in in fact all connected in parallel with the buck stage input. In phase three finally (Fig.3.2.4), the buck stage is in free-wheeling mode and the inductor current is flowing on S_b body diode, while the flying capacitors are disconnected and neither charging or discharging.

To understand the advantage of this solution, the inductor current ripple is estimated:

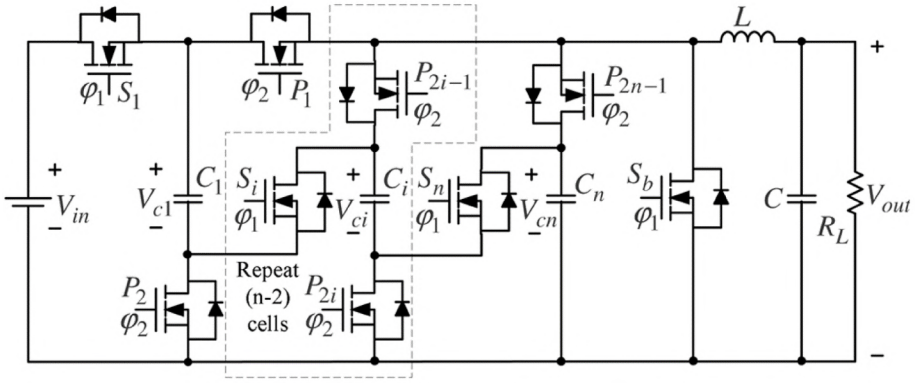


Figure 3.2.1: Hybrid cascaded converter.

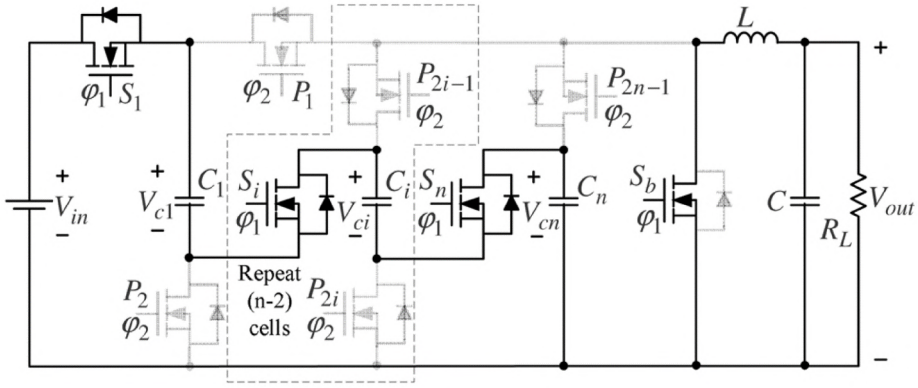


Figure 3.2.2: Hybrid cascaded converter: phase one equivalent circuit.

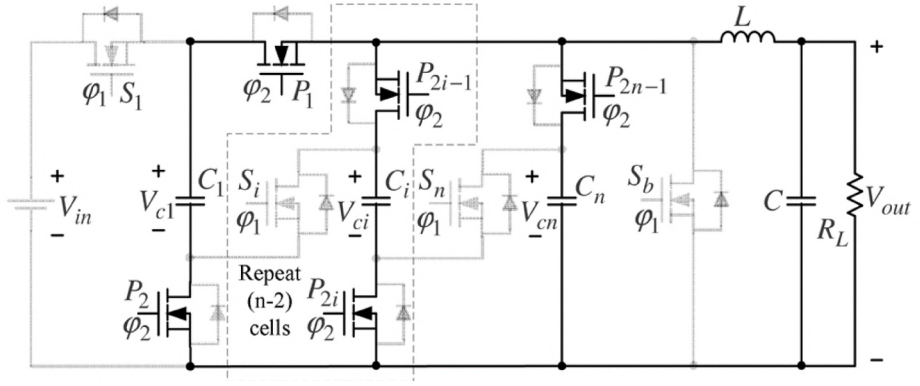


Figure 3.2.3: Hybrid cascaded converter: phase two equivalent circuit.

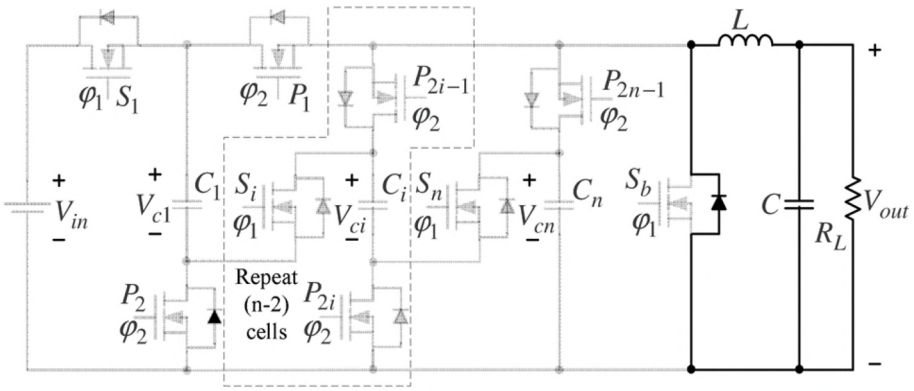


Figure 3.2.4: Hybrid cascaded converter: buck stage free-wheeling phase equivalent circuit.

$$\Delta i_L = \left(\frac{V_{in}}{3} - V_{out}\right)\frac{D}{Lf_S} = \frac{V_{out}}{Lf_S}\left(1 - \frac{V_{out}}{(V_{in}/3)}\right)$$

As it is possible to notice in the previous expression, being the term $(V_{in}/3)$ at the denominator side of the equation, the inductor current ripple is reduced by decreasing the buck stage input voltage. In a standard buck converter the inductor current ripple would in fact be

$$\Delta i_{L\,buck} = (V_{in} - V_{out})\frac{D}{Lf_S} = \frac{V_{out}}{Lf_S}\left(1 - \frac{V_{out}}{V_{in}}\right) = \frac{V_{out}}{Lf_S}(1 - M)$$

where M is the conversion ratio. Once again this equation clearly shows that increasing the implemented voltage conversion ratio (therefore reducing the buck stage input voltage) reduces the inductor current ripple. This solution is therefore interesting where a high step-down ratio is necessary.

Furthermore, it must be noticed that in this topology, the buck-stage duty cycle (that we called D in the previous calculations) does not coincide with the switched-capacitor cell duty cycle. An inductor free-wheeling phase, in which the switched-capacitor cell is inactive,is in fact introduced. This is very important because it allows to vary D while keeping the switched-capacitor cell in its optimum operating point. As a consequence, in this case, D can reach much higher values than, for example, in the KY converter case, expanding the converter's regulation capabilities.

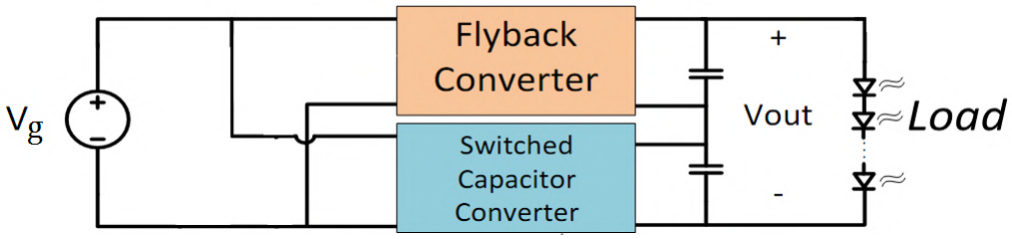


Figure 3.3.1: Hybrid parallel input serial output topology.

3.3 Parallel Input Serial Output Topology

This approach employs two distinct converters, one switched-capacitor and one inductor based, that are connected in parallel at their input, but whose output stages are in series. By doing this, it is possible to design the whole system to obtain a step-up topology in which the inductor based stage processes just a limited amount of the total output power; most of the requested step-up gain is in fact given by the switched capacitor stage, while the inductor based one performs just the fine tuning of the output voltage. This type of solution solves the switched capacitor converters output voltage regulation problems, while also reducing inductive element requirements with respect to a standard inductor based topology (as previously said most of the output voltage is in fact given by the switched-capacitor converter).

An example of this approach can be found in [6]. This topology, shown in Fig.3.3.2, is made of a step-up switched capacitor (a modified four times series-parallel multiplier) and a flyback converter. The use of an isolated topology allows to have a floating output that can be stacked onto the switched capacitor output stage.

Apart from the advantage of designing the inductor based converter sized for a lower power level, this solution has also the advantage of a reduced switches voltage stress. In an equivalent boost converter both switches are in fact exposed to MV_g, where M is the conversion ratio of the converter, while in an equivalent flyback instead, primary and secondary side switches are exposed to $V_g + nV_{out}$ and $\frac{V_g}{n} + V_{out}$ respectively, where n is the turns ratio of the flyback transformer. In the hybrid topology instead, the maximum voltage seen by any switch of the switched capacitor stage is $(M_{SC} - 1)\, V_{in}$, where M_{SC} is the conversion ratio of this sub-converter, and the voltage stress of the flyback is $V_g + n_{HSO} V_{fb}$ and $\frac{V_g}{n_{HSO}} + V_{fb}$, where n_{HSO} is the turns

ratio of the flyback transformer and V_{fb} is the output voltage of the flyback. The converter is designed such that $V_{SC} = M_{SC}V_g < V_{out}$, which makes the peak voltage stress of the switched capacitor converter inherently lower than an equivalent boost or flyback one. The voltage stress of the flyback is determined by n_{HSO}. To achieve lower peak voltage stress than the boost switches, the following condition must be met:

$$V_g + n_{HSO}V_{fb} < V_{out}$$

and this yields

$$n_{HSO} < \frac{(M-1)\,V_g}{V_{fb}}$$

Defining $M_{fb} = \frac{V_{fb}}{V_g}$, the previous equation becomes

$$n_{HSO} <= \frac{M-1}{M_{fb}} = \frac{M-1}{M - M_{SC}}$$

Using a parallel input serial output approach has also the advantage of allowing the output voltage ripple reduction by shifting the sub-circuits output voltage waveform phases. This solution can therefore be interesting when a step-up converter is needed.

Another interesting example that can be considered is shown in Fig.3.3.3. In this case, the concept of a step-up topology built combining a buck and a multilevel SCC is analysed, to make the possible advantages of this approach even clearer.

A comparison with an equivalent boost converter immediately shows the attainable improvements. As seen before in fact, using a buck instead of a boost converter allows to reduce the inductive part switches voltage stress of a factor equal to the conversion ratio M. It is also interesting to consider the inductor current ripple. As previously seen, in the buck case, the worst case inductor current ripple is equal to

$$\Delta i_{L-worst\,case} = \frac{V_g}{4Lf_S}$$

In a boost case instead, the same parameter was previously estimated to be

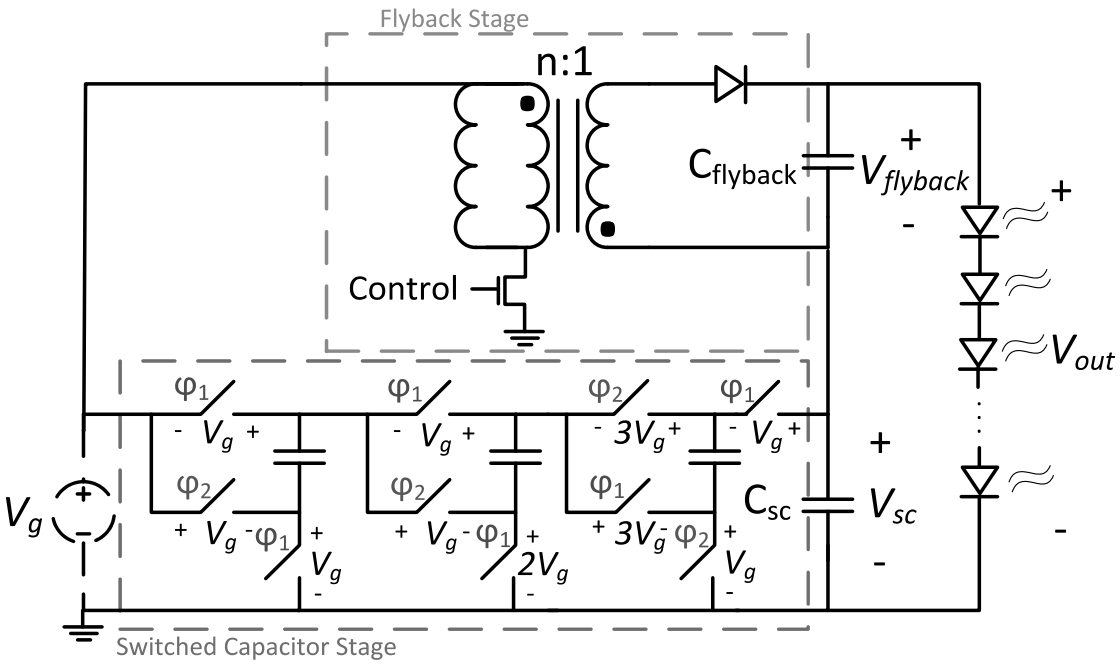


Figure 3.3.2: Hybrid parallel input serial output topology implementation.

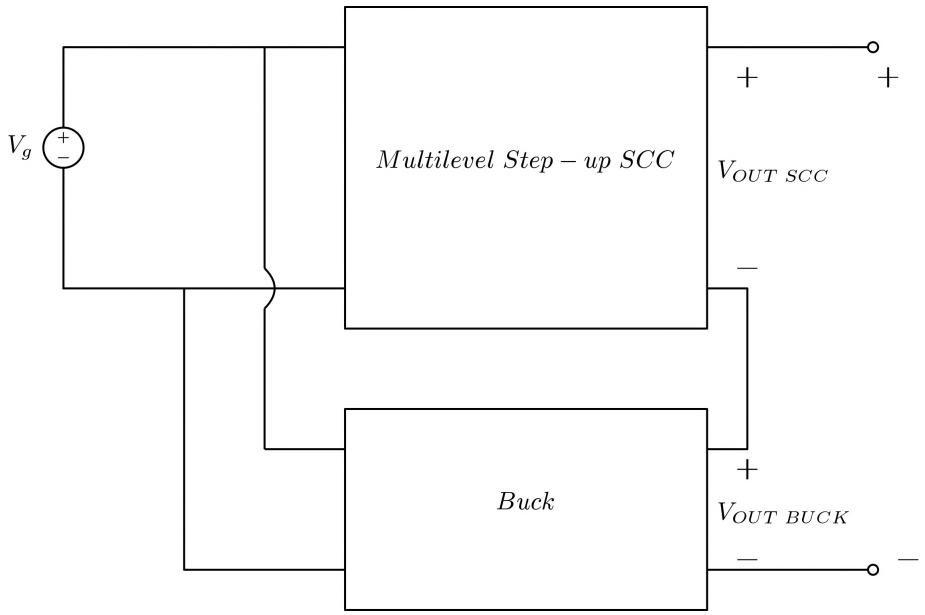


Figure 3.3.3: Possible hybrid parallel input serial output converter structure.

$$\Delta i_{L-worst\ case} = \frac{V_g}{Lf_S}\frac{(M_{max}-1)}{M_{max}}$$

where M_{max} is the maximum requested conversion ratio. Comparing the two previous expressions, it is possible to find that inductor current ripple in the hybrid topology case is lower than the same parameter in the equivalent boost for M_{max} higher than $\frac{4}{3}$. It is likely for a step-up application to request a higher maximum conversion ratio, therefore resulting in an increased inductor voltage ripple. It is then pretty clear that this type of hybrid topologies, can yield reduced inductive elements requirements, together with possibly reduced switch voltage stress; the latter is anyway dependent on the specific switched capacitor topology implemented. It is also very important to notice that the SCC converters shown in chapter one need to be modified in order to allow their output stages to be stacked on the buck one. In fact, the switched-capacitor converter stage must never connect the output nodes to the input, to avoid interfering with the buck stage operation. In particular, its negative output pin must never be connected to the input, otherwise a shorting of the buck stage occurs.

Chapter 4

Proposed Novel Hybrid DC-DC Topologies: Discrete Components Approach

As seen in the previous chapter, hybrid DC-DC converters can be an interesting choice to overcome the limitations of switched capacitor converters while reducing the magnetic element requirements.

4.1 Step-up Hybrid Buck

An example of how a charge pump and inductor based topology can be mixed together is shown in Fig.4.1.1. In this case the filtering action of the inductor and capacitor C_b is exploited to regulate the output voltage, by subtracting a controlled amount of voltage to the output capacitor charging voltage. To better understand this statement the converter operating phases are considered separately. As it is possible to see in Fig.4.1.2, during phase A switch $S_1$and diode D_o are turned OFF, while S_2 is ON. In this phase therefore, C_1 is charged to V_{in}, and $V_L = -v_b$, while the output capacitor C_o is providing energy to the load.

In phase B instead (Fig.4.1.3) S_2 is turned OFF, while S_1 and diode D_1 are ON. In this phase $V_L = V_{in} - v_b$, and C_O is charged by the series of V_{in} and C_1, it is therefore possible to write the following equation:

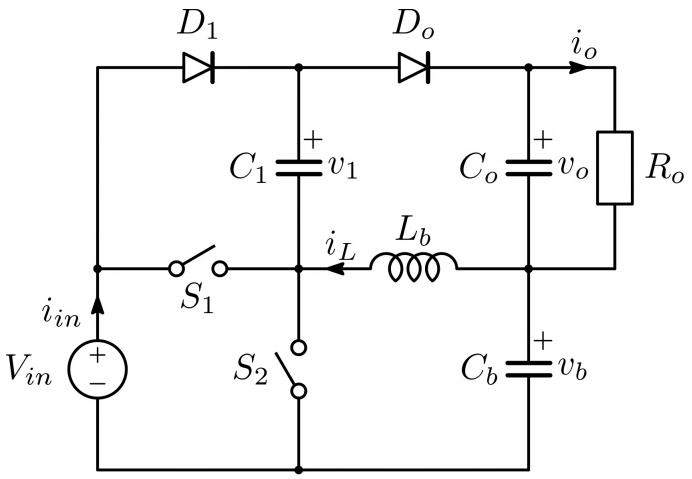


Figure 4.1.1: Step-up hybrid buck.

$$V_{in} + v_1 = v_o + v_b$$

that gives the following

$$v_o = 2V_{in} - v_b$$

The output capacitor is therefore charged to $2V_g$ minus a quantity v_b, that can then be used to regulate the output voltage. Since C_b is the output capacitor of a buck stage in fact, its voltage can be estimated as

$$v_b = DV_{in}$$

Therefore, it is possible to calculate the output voltage as

$$v_o = 2V_{in} - v_b = (2 - D)\, V_{in}$$

The converter conversion ratio is therefore

$$M = 2 - D$$

It is important to notice that this converter has a limited range of attainable conversion ratios. The theoretical minimum and maximum conversion ratio values are in fact 1 and 2.

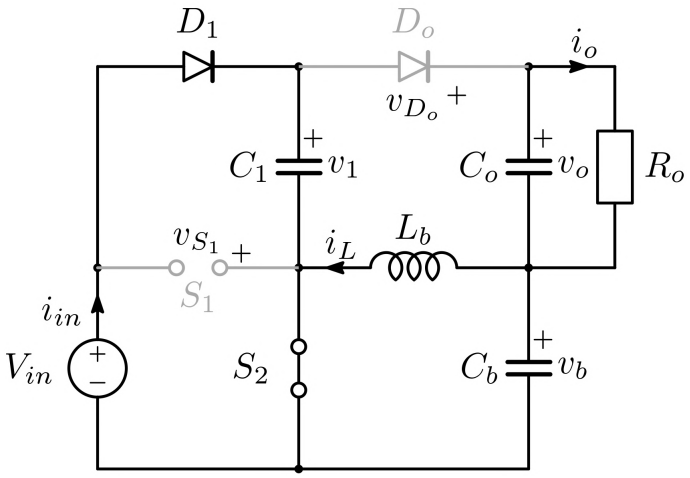


Figure 4.1.2: Step-up hybrid buck phase A equivalent circuit.

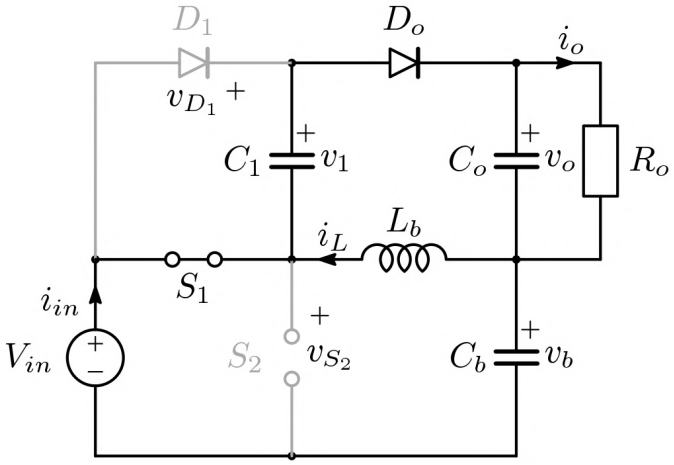


Figure 4.1.3: Step-up hybrid buck phase B equivalent circuit.

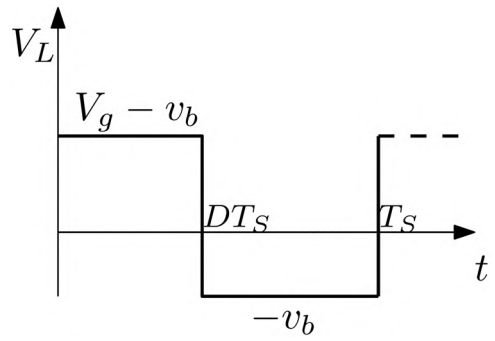


Figure 4.1.4: Step-up hybrid buck inductor voltage waveform.

After estimating the converter conversion ratio, it is possible to evaluate the switches and diodes voltage stress. Considering the converter ON-phase first (Fig.4.1.3), the voltage stress on diode D_o can be calculated as $v_{D_o} = v_b + v_o - V_{in} = V_{in}$, while $v_{S_2} = V_{in}$. On the other hand, observing the OFF-phase equivalent circuit, it is possible to estimate the voltage stress on S_1 and D_o, obtaining $v_{S_2} = V_{in}$ and $v_{D_1} = v_1 = V_{in}$.

It is now interesting to analyse the magnetic element requirements. Knowing the inductor voltage in both phases, the inductor current ripple can be estimated as

$$\Delta i_L = \frac{v_b\,(1-D)}{Lf_S} = \frac{V_{in}D\,(1-D)}{Lf_S} = \frac{V_{in}\,(2-M)\,(M-1)}{Lf_S} \tag{4.1.1}$$

In the worst case situation, corresponding to $D = 50\%$, the ripple becomes then

$$\Delta i_{L-worst\,case} = \frac{V_{in}}{4Lf_S} \tag{4.1.2}$$

The average inductor current can instead be estimated observing that, in steady state operation, the average current value of any capacitor is equal to zero. Applying the Kirchhoff current law at the node in common between L, C_b, C_o and R_o, it is then clear that the average inductor current is equal to the average load current

$$I_L = I_{load}$$

Comparing the previous results with a standard equivalent boost characteristics, it is possible to notice that the proposed hybrid topology has a lower average inductor current. Comparing it with the same parameter in the equivalent standard boost case in fact, we get

$$\frac{I_{L\,hybrid}}{I_{L\,boost}} = \frac{1}{M}$$

Performing the same comparison for the inductor current ripple, we get instead

$$\frac{\Delta i_{L\,hybrid}}{\Delta i_{L\,boost}} = (2 - M)\, M$$

This quantity is always lower than one for $1 \leq M \leq 2$ (Fig.4.1.6). The inductor current ripple is therefore reduced in the hybrid topology, as it is possible to see also looking at Fig.4.1.5.

Once again the hybrid converter succeeds in reducing the magnetic element requirements, while also decreasing the switching devices voltage stress. Anyway this topology has some very important drawbacks: a floating load and a very limited conversion ratio. Efficiency considerations on the charge pump part of the circuit in fact, make it difficult to vary the duty cycle in a broad range, limiting the actual range of attainable conversion ratios. Considering for example a duty cycle that can vary between 40 and 60%, the implemented conversion ratios range will go from $1,4$ to $1,6$.

4.2 Charge Pump Circuits Inserted Inside Standard Inductor Based Topologies

4.2.1 Step-up DC-DC Converters combining basic topologies with charge-pump

An interesting example of how new topologies can be derived inserting charge pump sub-circuits in standard inductor based converters, can be found in [7]. In this work a simple modification of basic Buck and Boost topologies so as to introduce a charge pump action that turns the overall structure into an equivalent step-up converter with reduced magnetic element requirements

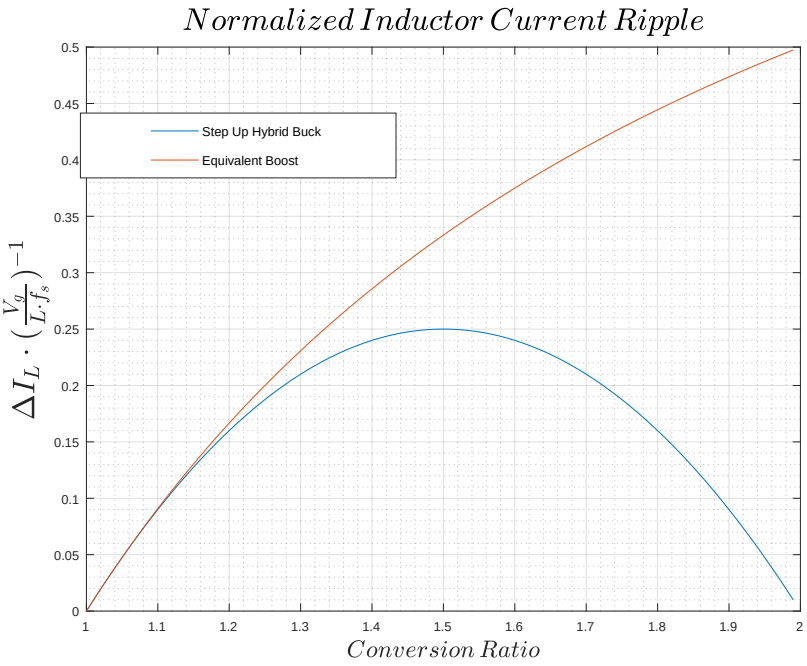


Figure 4.1.5: Normalized inductor current ripple: step up hybrid buck and equivalent standard boost converter.

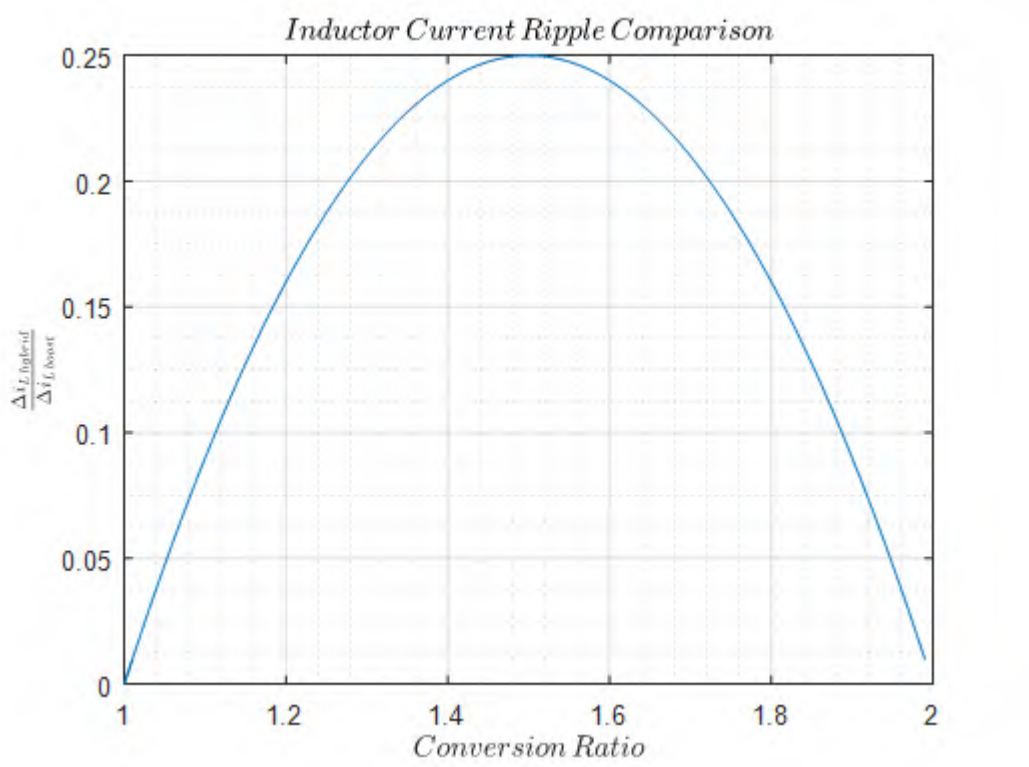


Figure 4.1.6: Step up hybrid buck inductor current ripple over the same quantity in an equivalent standard boost converter.

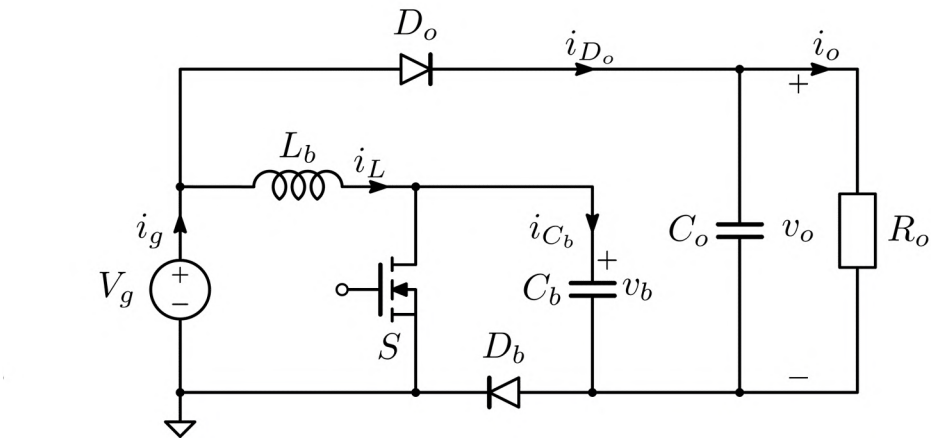


Figure 4.2.1: Boost derived hybrid topology.

compared to a standard Boost converter is described. Other advantages of the derived hybrid topologies are the reduced switch voltage stress and associated switching losses, at a price of possibly higher conduction losses and a floating load connection.

4.2.1.1 Boost Derived Topology

Starting from the basic Boost converter, the charge pump action can be introduced by adding an output diode and capacitor, and changing the position of the free-wheeling diode (Fig.4.2.1). Doing this, the charge pump action occurs in the switch ON-time. During the charge pump interval, the input source is delivering energy directly to the output through the charge pump action. This boost derived topology is actually a simplified version of one of the topologies presented in [8] (see Fig. 4c of the cited paper), where one of the charge pump sub-circuit is removed. Assuming continuous conduction mode (CCM) operation and unity efficiency, the ideal voltage gain of the topology results:

$$M = \frac{V_o}{V_g} = \frac{2 - D}{1 - D} \tag{4.2.1}$$

Thus this structure implements a step-up converter with a voltage gain higher than two.

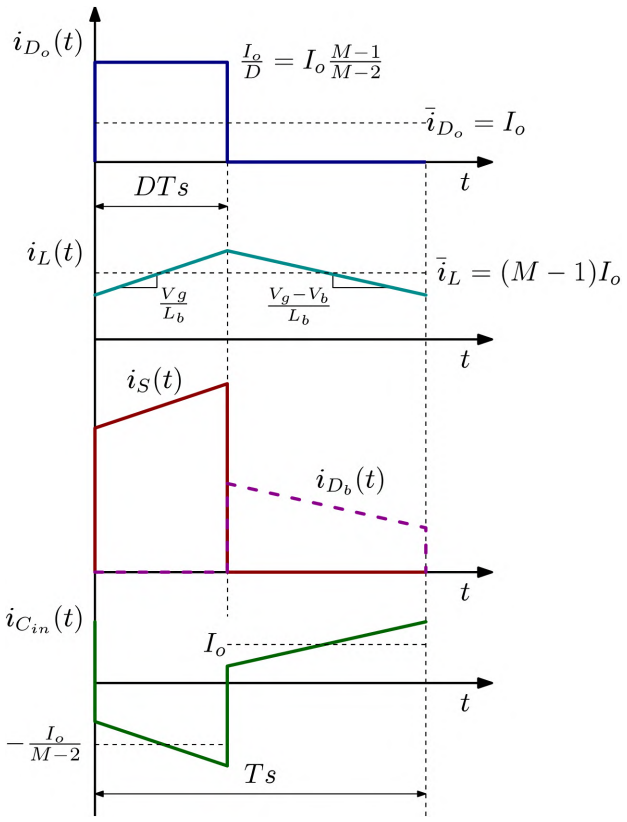


Figure 4.2.2: Boost derived topology theoretical waveforms.

The following analysis considers the scheme of Fig.4.2.1. Assuming the switching period is much lower than the charge pump time constant, the idealized instantaneous current waveforms are as shown in Fig.4.2.2, while the corresponding sub-topologies are reported in Fig.4.2.3. Note the use of a decoupling source impedance Z_g , here assumed purely inductive, so as the input capacitor average voltage is equal to V_g .

From these waveforms, and the unity efficiency assumption, the average inductor current results:

$$\bar{i_L} = (M-1)I_o \tag{4.2.2}$$

It is now interesting to compare the performance of the proposed topology with that of an equivalent Boost converter (a simple Boost converter operating at the same input and output voltages and power). From this perspective,

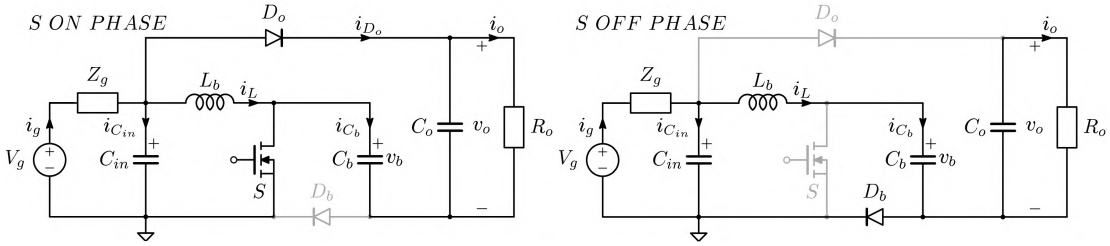


Figure 4.2.3: Boost derived topology equivalent circuits during the switch ON (left) and OFF time (right).

the normalized average inductor value from (4.2.2) is:

$$J_L = \frac{\bar{i_L}}{\bar{i}_L^{boost}} = \frac{M-1}{M}$$

Another interesting thing to notice is that, being $V_b < V_o$, the hybrid topology works at a lower duty cycle if compared to a standard boost converter. Thus, from (4.2.1), it is possible to estimate

$$\frac{D^{boost}}{D} = \frac{(M-1)^2}{M(M-2)} = f(M) > 1 \tag{4.2.3}$$

Consequently, for the same inductor current ripple, the needed inductance value in this hybrid topology is lower than in the standard Boost case. The ratio of the two inductance values is given by function $f(M)$, defined in (4.2.3). This fact, together with the lower average inductor current value, shows that this topology succeeds in reducing the overall magnetic energy and volume.

To understand this hybrid topology performance in terms of efficiency, the different loss sources must be analysed. To this purpose, the inductor current ripple is neglected for simplicity, so that $i_L(t) \approx I_L$.

Switch conduction losses

Calling r_S and $r_{boost}$the switch parasitic series resistances of the proposed topology and of the standard Boost, the normalized switch conduction losses can be calculated as follows:

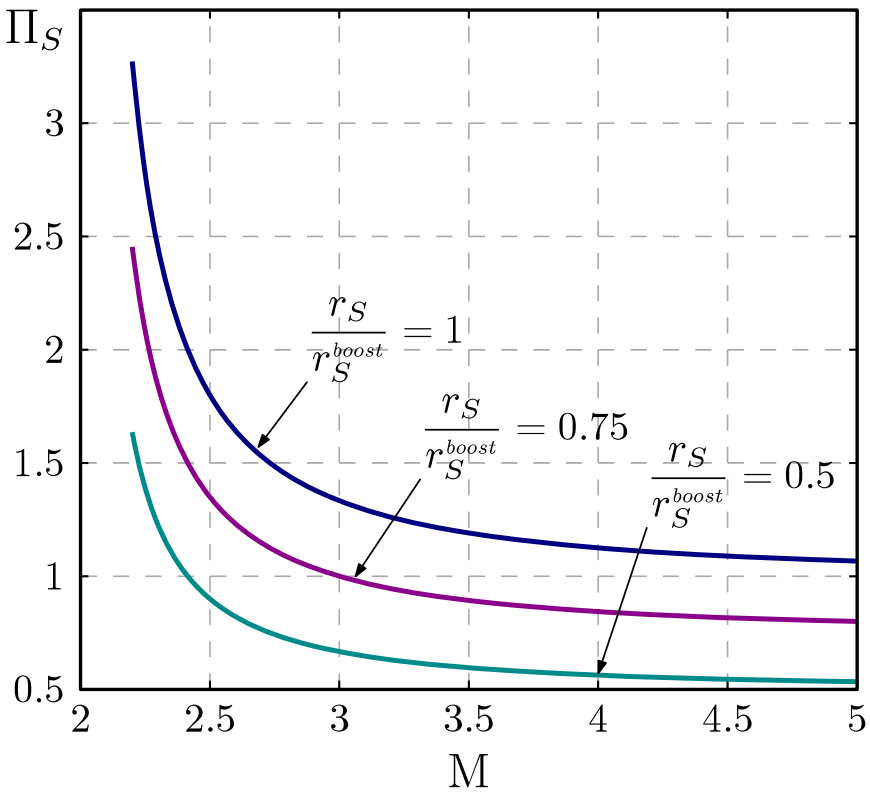


Figure 4.2.4: Boost derived topology normalized switch conduction losses ($\prod_S$) as a function of the conversion ratio M for different switches resistance values.

$$\frac{P_S}{P_S^{boost}} = \frac{r_S}{r_S^{boost}} \frac{(\frac{I_o}{D} + I_L)^2 D}{(M I_o)^2 D^{boost}} = \frac{r_S}{r_S^{boost}} f(M)$$

where (4.2.1) and (4.2.2) were used. Fig.4.2.4 plots the normalized switch conduction losses as a function of the voltage gain for three different values of switches resistance ratio. It is possible to notice that at a given voltage conversion ratio, the switch conduction losses of the proposed topology can be higher or lower of those of a standard Boost converter, depending on the relative value of the switch ON-resistance.

Switching losses

The normalized switch and diodes voltage stress, is given by:

$$U_{sw} = \frac{V_{sw}}{V_{sw}^{boost}} = \frac{1}{2-D} = \frac{M-1}{M}$$

Thus, assuming the same switching times, the normalized switching losses are:

$$\frac{P_{sw}}{P_{sw}^{boost}} = (\frac{M-1}{M})^2 < 1$$

Inductor conduction losses

Calling $r_L$and r_L^{boost} the inductor series resistances of the proposed topology and of the standard Boost, the normalized conduction losses are:

$$\frac{P_L}{P_L^{boost}} = \frac{r_L}{r_L^{boost}}(\frac{M-1}{M})^2 < 1$$

Diode conduction losses

In order to calculate the diode conduction losses, a simple series $V_{Do} - r_D$ model is used for a conducting diode. Let's calculate separately the two contributions of the cut-in voltage V_{D0} and of the parasitic resistance r_D. Note that, in the hybrid topology case, the contributions of both diodes D_o and D_b are summed. The normalized diode conduction losses can therefore be expressed as

$$\frac{V_{Do}}{V_{D_o}^{boost}}\left(\frac{I_o + (1-D)I_L}{I_o}\right) = 2\frac{V_{Do}}{V_{D_o}^{boost}} \tag{4.2.4}$$

where (4.2.1) and (4.2.2) were used and the same device was considered for the output diode D_o and the boost diode D_b. The contribution of the diode parasitic resistances is:

$$\frac{r_D}{r_D^{boost}} f(M) \tag{4.2.5}$$

As for the switch conduction losses, higher or lower diode conduction losses can be obtained, even if the factor two in the cut-in voltage related losses suggests that, despite the lower voltage rating devices of the proposed topology, an increase of these losses is, in most cases, to be expected.

Capacitor losses

Let's call r_{C_o}, $r_{C_{in}}$ and r_{C_b} the parasitic resistances of output, input and boost output capacitors, respectively (see Fig.4.2.3). The associated power dissipation, compared with the power loss of the output capacitor of a standard boost converter (neglecting the inductor current ripple implies a loss free Boost input capacitor), is given by the following expression:

$$\frac{r_{C_o} + r_{C_{in}} + (M-1)^2 r_{C_b}}{(M-1)(M-2) r_C^{boost}}$$

In the hybrid case, higher capacitor losses have to be expected.

In summary, while the reduced magnetic element requirements are granted, the overall conversion efficiency can be higher or lower compared with a simple Boost converter, depending on the relative weight of conduction and switching losses.

4.2.1.2 Buck Derived Topology

Starting from the basic Buck converter, the charge pump action can be introduced by adding an output diode and capacitor, and changing the position of the filter inductor as shown in Fig.4.2.5. Doing this, the charge pump action occurs during the main switch off time. During the charge pump interval, the input source is delivering energy directly to the output through the charge pump action.

Assuming continuous conduction mode (CCM) operation and unity efficiency, the ideal voltage gain results:

$$M = \frac{V_O}{V_g} = 1 + D \tag{4.2.6}$$

Thus the modified structure implements a step-up converter with gain comprised between one and two. It is important to notice that, in this topology, a synchronous Buck cell must be used.

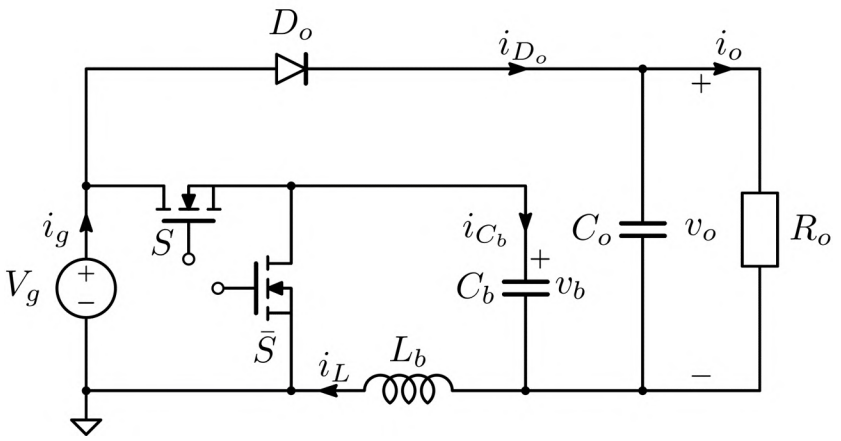


Figure 4.2.5: Buck derived hybrid topology.

The analysis carried out in the boost derived topology case, can be performed also for the buck-derived one. The main converter waveforms are shown in Fig.4.2.6, under the same simplifying hypothesis of CCM operation and a switching period much lower than the charge pump time constant. The corresponding sub-topologies are reported in Fig.4.2.7; also in this case a decoupling source impedance Z_g, assumed purely inductive, is considered.

Once again comparing the hybrid topology with a standard boost converter, the normalized average inductor current is given by:

$$J_L = \frac{\overline{i_L}}{\overline{i_L^{boost}}} = \frac{1}{M} < 1$$

Moreover, comparing the inductance values for the same inductor current ripple, we have:

$$\frac{L}{L_{boost}} = M(2 - M) = 1 - D^2 < 1$$

where (4.2.6) has been used.

It is then clear that also the Buck-derived boost topology succeeds in reducing the overall inductor volume.

As done in the previous case, it is now important to analyse the different loss contributions, to estimate the converter efficiency when compared to a

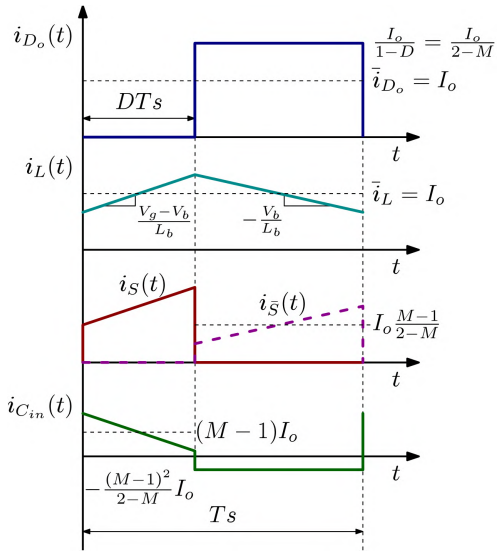


Figure 4.2.6: Buck derived topology theoretical waveforms.

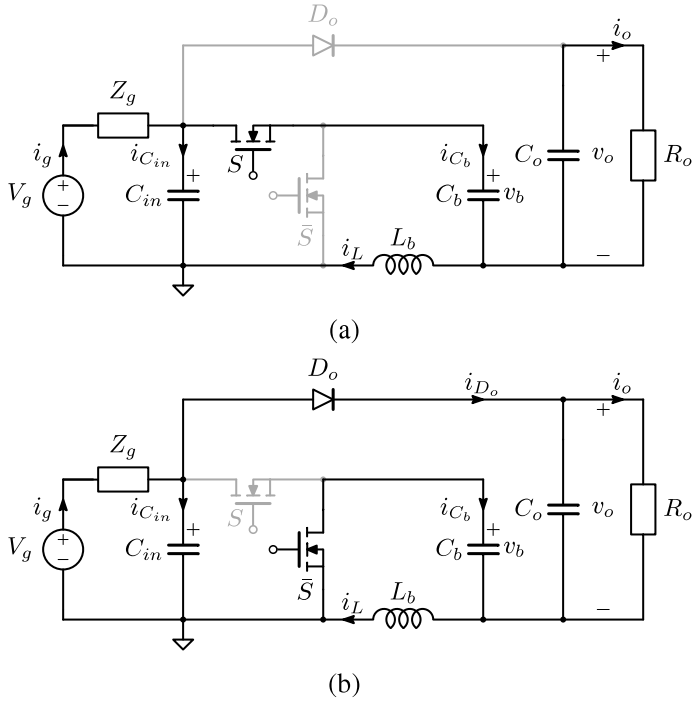


Figure 4.2.7: Buck derived topology equivalent circuits during the switch ON (a) and OFF (b) phase.

standard boost converter. Once again the inductor current ripple is neglected for simplicity.

Switches Conduction Losses

Considering the same on resistance for both switches S and $\overline{S}$, their overall normalized conduction losses are:

$$\frac{P_S}{P_S^{boost}} = \frac{r_S}{r_S^{boost}} \frac{1}{M(2-M)} \tag{4.2.7}$$

Similarly to the previous topology, the switches conduction losses of the proposed topology can be higher or lower of those of a standard Boost converter, depending on the relative value of the switches on resistance. It must be noticed that equation 4.2.7 was derived considering a standard asynchronous boost converter, while the proposed hybrid topology employs a synchronous buck stage.

Switching Losses

The normalized switch and diodes voltage stress, is given by:

$$U_{sw} = \frac{V_{sw}}{V_{sw}^{boost}} = \frac{1}{M}$$

Thus, assuming the same switching times, the normalized switching losses are:

$$\frac{P_{sw}}{P_{sw}^{boost}} = \frac{1}{M^2} < 1$$

Inductor Conduction Losses

Calling r_L and r_L^{boost} the inductor series resistances of the proposed topology and of the standard Boost, the normalized conduction losses are:

$$\frac{P_L}{P_L^{boost}} = \frac{r_L}{r_L^{boost}} \frac{1}{M^2} < 1$$

Diode conduction losses

The output diode D_o carries the same average current of the corresponding diode in the standard boost topology. Thus, the loss contribution of the cut-in voltage V_{Do} is simply proportional to this voltage, while the contribution of the diode parasitic resistance is:

$$\frac{r_D}{r_D^{boost}} \frac{1}{M(2-M)}$$

Comparing this result with (4.2.7), the same considerations done for the switch conduction losses apply.

Capacitor losses

The parasitic resistances of output, input and boost output capacitors can be defined as r_{C_o}, $r_{C_{in}}$ and r_{C_b} respectively. The associated power dissipation, compared with the power loss of the output capacitor of a standard boost converter (neglecting the inductor current ripple implies a loss free Boost input capacitor), is given by the following expression:

$$\frac{r_{Co} + r_{C_b} + (M-1)^2 r_{C_{in}}}{(2-M) r_C^{boost}}$$

In this case, higher capacitor losses have to be expected.

4.2.1.3 Experimental Verification

In order to verify the theoretical and simulation results, a prototype of the boost derived topology was built, using the specifications and passive components reported in Fig.4.2.8.

The silicon devices are: switch Infineon IPD90N06S4-07, boost diode 50WQ10FN, output diode STPS5L60.

The main converter waveforms, taken at nominal output voltage and power, and at an input voltage of $13.8\,V$, are shown in Fig.4.2.9. This figure reveals an important deviation from the theoretical analysis, given by the resonant behaviour of the output diode current i_{D_o} . In fact, in this discrete implementation, the parasitic inductance of the current path during the switch

TABLE I
CONVERTER SPECIFICATIONS

Parameter	Symbol	Value	
Minimum input voltage	$V_{g_{min}}$	12	V
Maximum input voltage	$V_{g_{max}}$	20	V
Output voltage	V_o	60	V
Output power	P_o	60	W
Switching frequency	f_{sw}	300	kHz

TABLE II
CONVERTER PARAMETERS

Parameter	Symbol	Value	
Input capacitor	C_{in}	$10 + 470$	μF
Boost capacitor	C_b	10	μF
Output capacitor	C_o	10	μF
Inductor	L_b	21	μH

Figure 4.2.8: Boost derived topology prototype specifications.

on time resonates with the series connected boost, input and output capacitances, thus changing the current waveform through the output diode (the current probe alone, used to measure the diode current, contributes to the overall parasitic inductance for few tens of nH). Without such parasitic inductance, the small device parasitic resistances, together with the low capacitor values, would have made the charge pump circuit to operate in the slow switching regime, in contrast with the hypothesis made for the theoretical analysis. Such operating mode would imply higher conduction losses.

To prove the above statement, a $PLECS^{®}$ simulation of the circuit of Fig.4.2.3 was performed with and without a parasitic inductance $L_p = 40nH$ in series with the output diode. All capacitors have an estimated ESR of 20 mΩ , while the inductance series resistance is 10 mΩ . The switch R_{DSon} is 8 mΩ and the diode model parameters are $r_D = 20m\Omega$, $V_{Do} = 0.4V$. The simulation results are reported in Fig.4.2.10, clearly demonstrating the effect of such parasitic inductance in shaping the output diode current.

A standard Boost prototype was built as well using the following components: switch IRFR540ZPbF, diode 50WQ10FN, output capacitor C_o=10F, and the same input inductor of 21 μH, for simplicity. The efficiency comparison is reported in Fig.4.2.11: these are practically the same, with just a slight

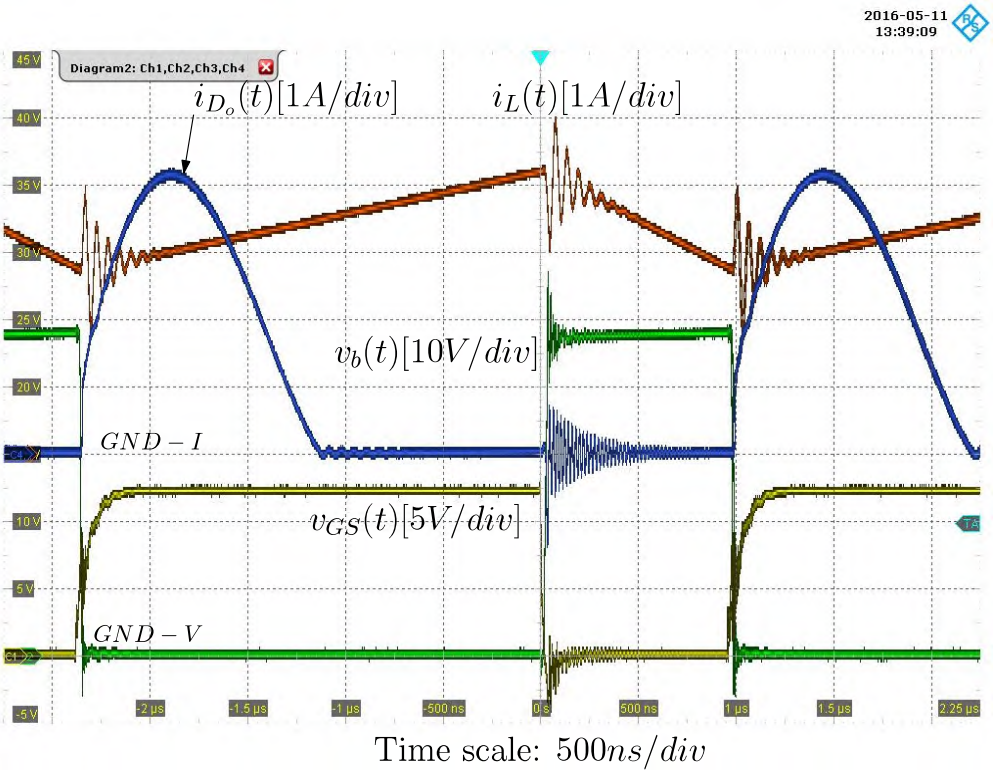


Figure 4.2.9: Boost derived topology prototype experimental waveforms: $GND - I$ indicates the reference level for the current waveforms, while $GND - V$ indicates the reference level for the voltage ones.

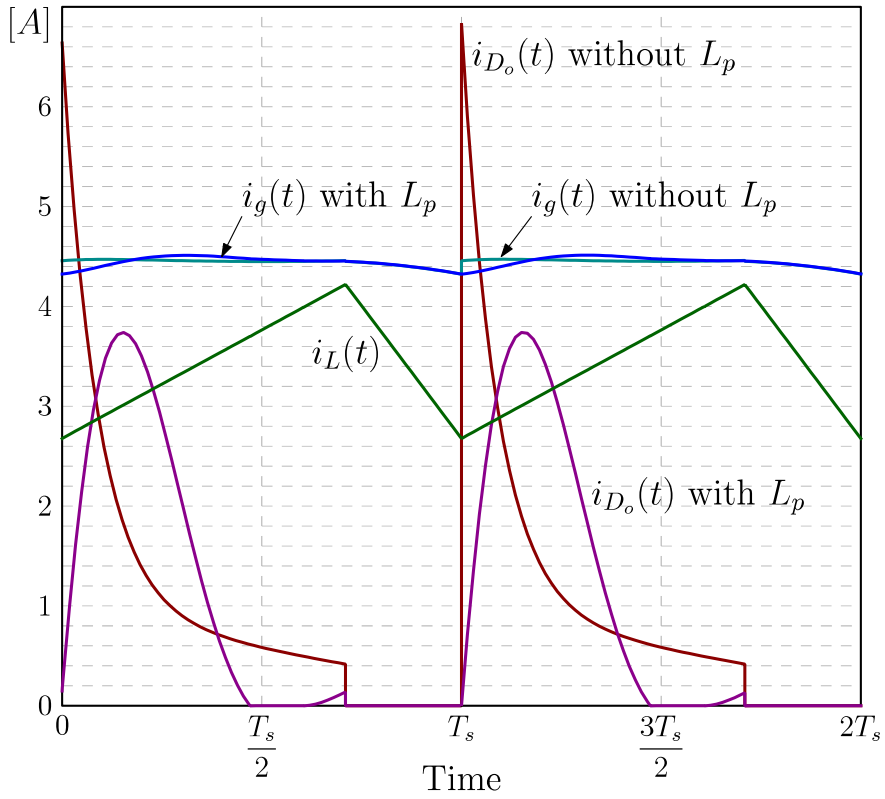


Figure 4.2.10: *PLECS*®simulation of the boost derived topology with and without a parasitic inductance in series with the output diode.

improvement at lower input voltages. Anyway, it must be remembered that the MOSFET used for the standard Boost prototype is rated at 35 A, with $R_{DSon} = 28.5$ mΩ, while the one used for the charge pump topology is rated at 90 A, with $R_{DSon} = 6.9$ mΩ.

4.2.1.4 High Gain Topology

Hybrid converters can be an interesting choice not only to reduce the size of converters, but also to increase the maximum attainable conversion ratio. In particular, the approach of merging a charge pump with an inductor based topology can be used to derive also isolated topologies. In the case of the Buck and Boost derived hybrid topologies previously described, following the same approach found in many papers, a coupled winding can be added to

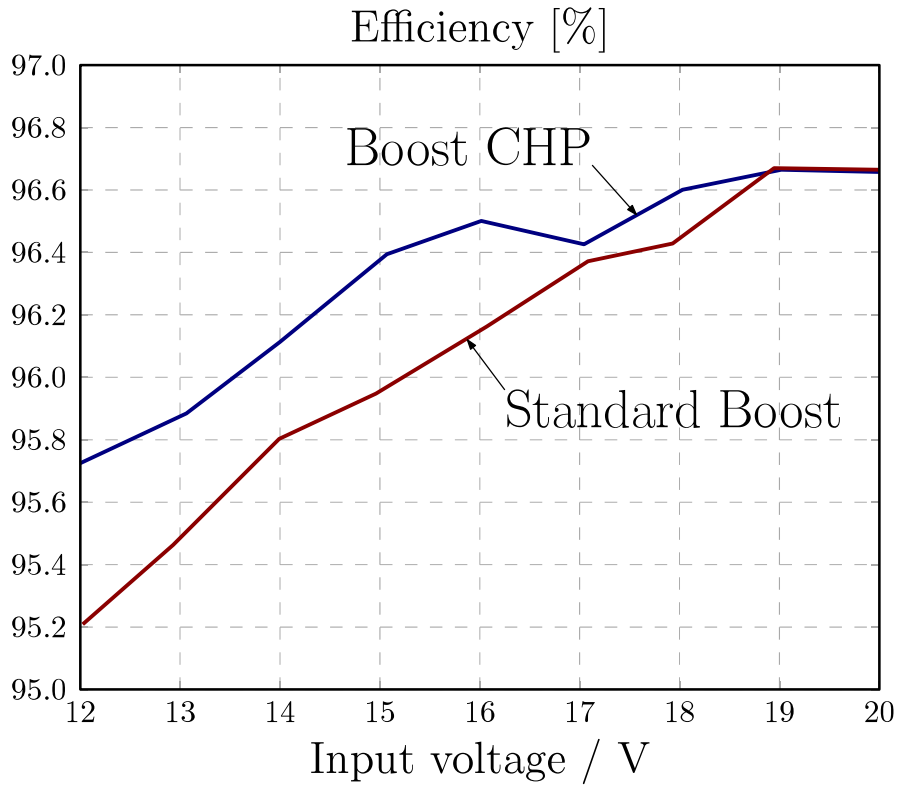


Figure 4.2.11: Experimental prototypes efficiency comparison.

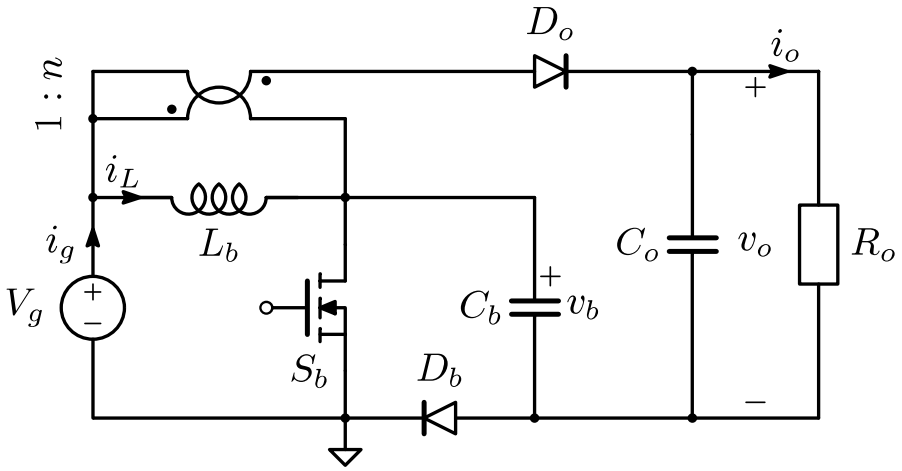


Figure 4.2.12: Boost derived high gain topology.

the main inductor and connected in series with the output diode (Fig.4.2.12 and 4.2.13).

Calling $n = \frac{N_s}{N_p}$ the coupled winding turns ratio, the ideal voltage gain of these converters is given by the following equations.

High gain Buck-derived topology:

$$M = \frac{V_o}{V_g} = \frac{V_g + (1+n)V_b}{V_g} = 1 + (1+n)D$$

High gain Boost-derived topology:

$$M = \frac{V_o}{V_g} = \frac{(1+n)V_g + V_b}{V_g} = \frac{n+2-(n+1)D}{1-D}$$

The topology modification for the Buck-derived structure is especially advantageous because it allows a much wider voltage gain variation, compared to the original solution. Moreover, the coupled winding allows to eliminate the need for a floating load connection, still guaranteeing a high gain, as shown in Fig.4.2.14. In this case the voltage gain reduces to $M = 1 + nD$. Finally,

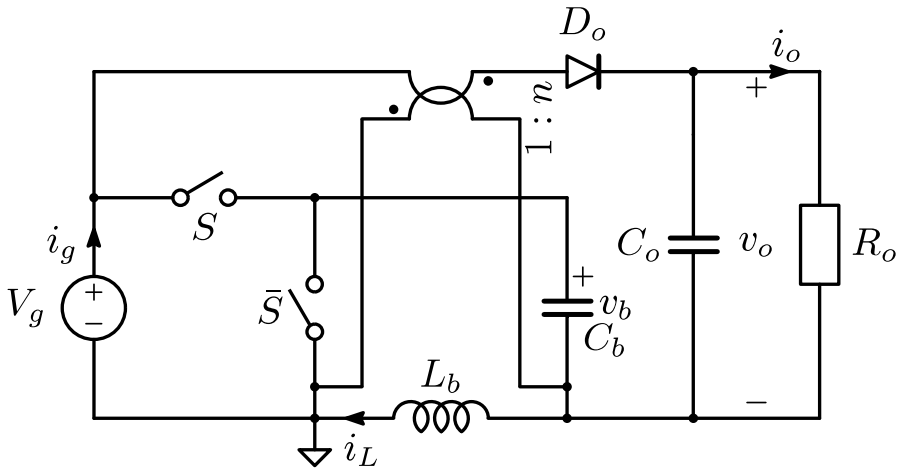


Figure 4.2.13: buck derived high gain topology.

all these coupled winding arrangements exploit the unavoidable transformer leakage inductance to achieve a resonant energy transfer similar to what has been obtained with the original Boost derived implementation using discrete components.

4.2.1.5 Boost Derived High Gain Topology

The circuit scheme of the boost derived high gain topology can be seen in Fig.4.2.15. An additional capacitor C_1 and diode D_1 are used so as to increase the boost action and to avoid any ringing across the output diode D_o at its turn off. Without the presence of a clamping element in fact, at D_o turn-OFF the diode's junction capacitance would resonate with the parasitic inductance and secondary winding leakage inductance that are in series with the diode, generating a voltage ringing that can cause reliability problems. The presence of D_1 instead, guarantees that D_o anode voltage is clamped, while also giving a flowing path for i_{D_o} as it tends to go negative. The sub-circuit inside the dashed rectangle represents the coupled inductor model, accounting for the magnetizing inductance L_μ and both primary and

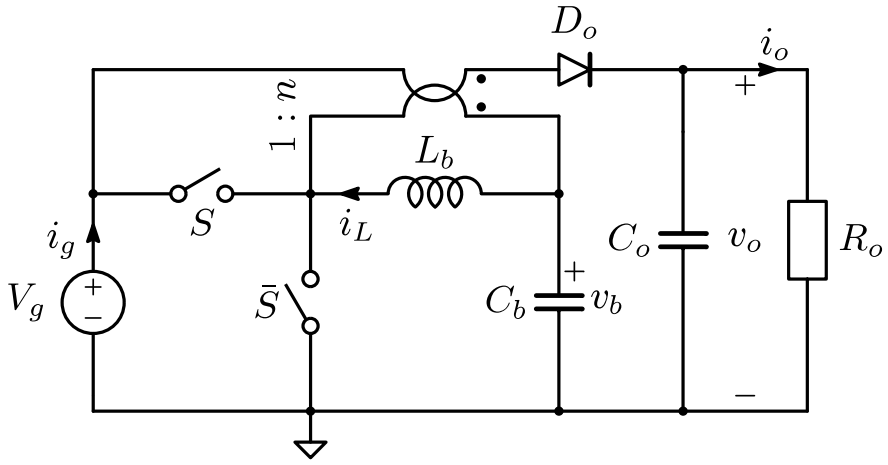


Figure 4.2.14: Buck derived high gain topology variation.

secondary leakage inductances L_p and L_s.

Similarly to what was observed in the discrete component implementation of the Boost-derived charge pump converter previously described, the transformer leakage inductance allows a resonant energy transfer during the output diode conduction interval. Thus, assuming the diode current $i_{D_o}(t)$ always completes a half resonant period during its conduction interval, the converter main waveforms are shown in Fig.4.2.16, and the corresponding sub-topologies are reported in Fig.4.2.17.

%endfigure

Note the two possible operating modes (denoted Mode 1 and Mode 2 in Fig.4.2.16) that, with the parameters used in both simulation and experimental measurements, appear at nominal conditions and with minimum and maximum input voltages, respectively. A qualitative description of the converter operation is given in the following.

Interval $t_0 \leq t \leq t_1$: see Fig.4.2.17(a). This phase starts at instant t_0 when the switch is turned on under zero current condition. The current in diode D_1, given by $i_{D_1}(t) = i_{L_S}(t)$, decreases rapidly to zero thanks to the positive

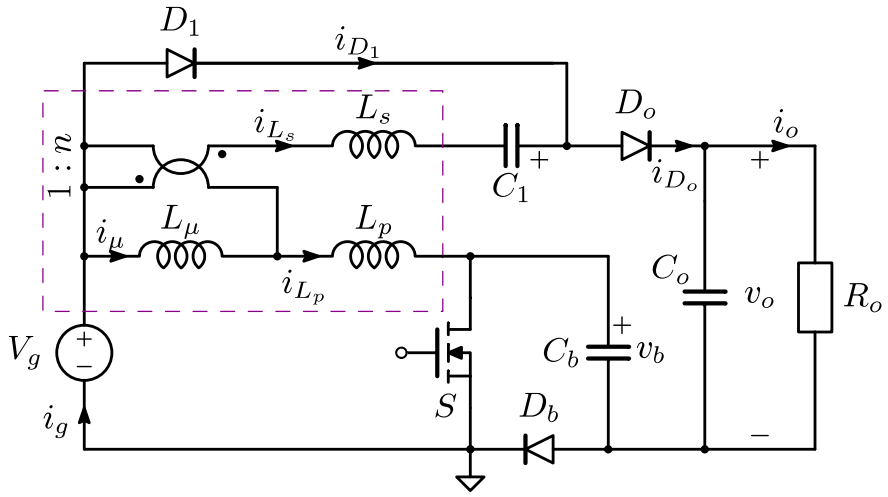


Figure 4.2.15: Boost derived high gain topology with transformer parasitics included.

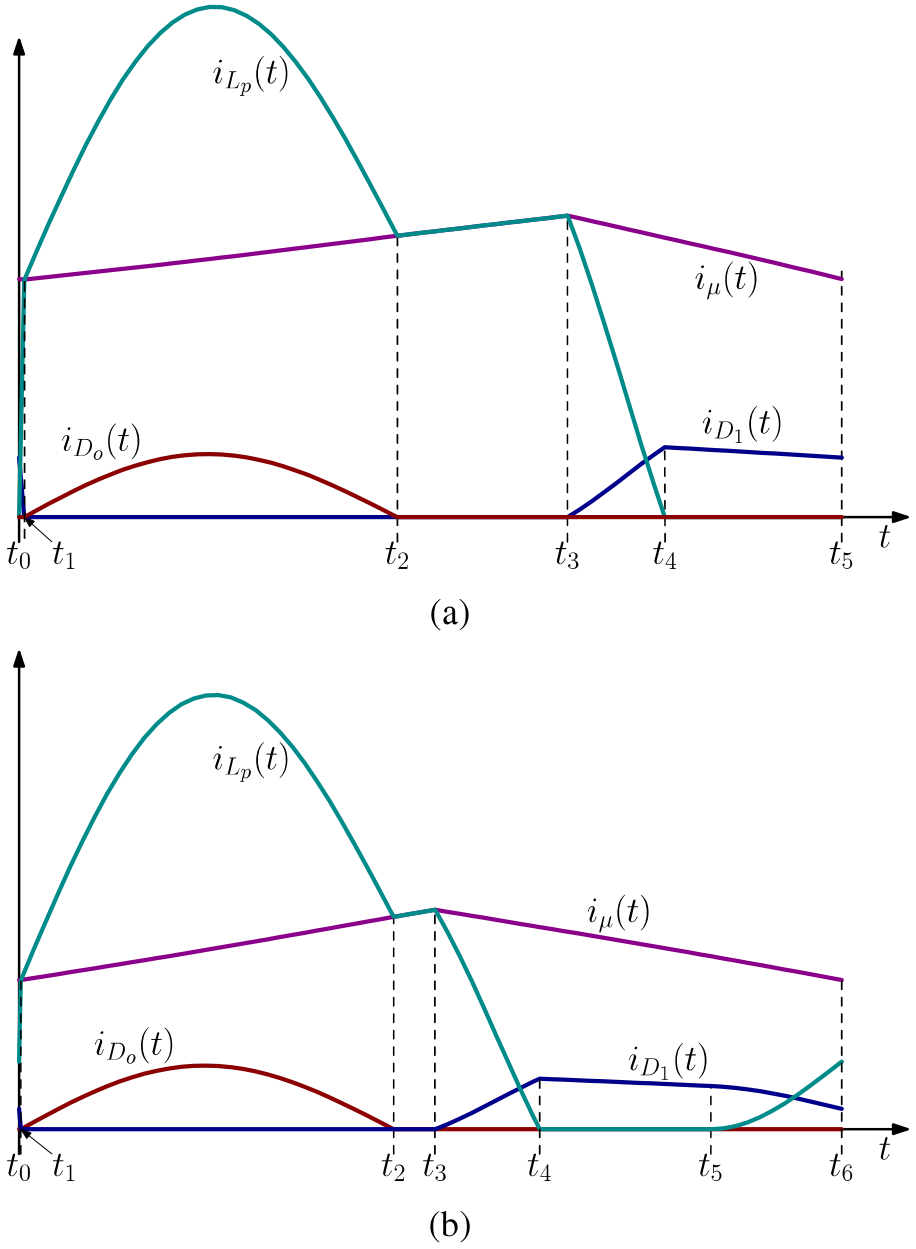


Figure 4.2.16: High gain boost derived converter main theoretical waveforms:(a) $Mode\,1$; (b) $Mode\,2$..

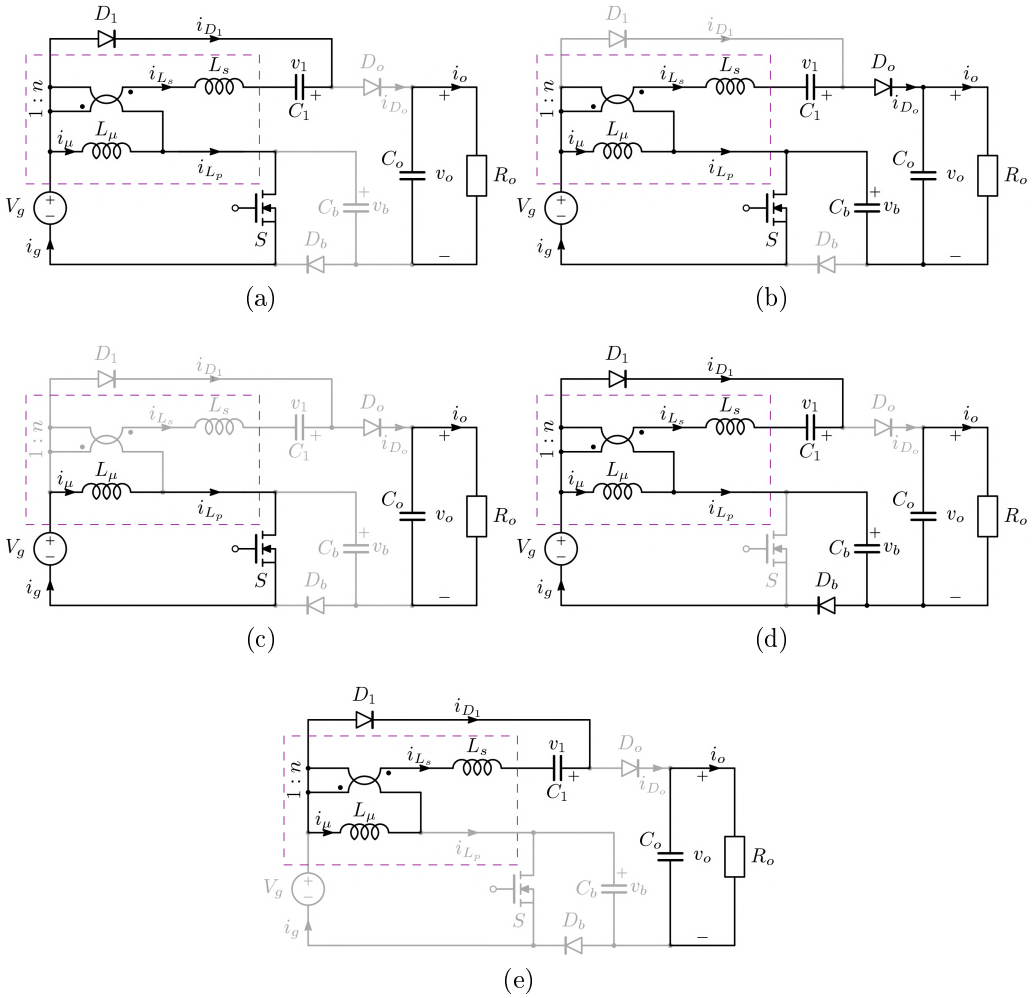


Figure 4.2.17: High gain boost derived converter sub-topologies.

voltage applied to the secondary leakage inductance. This sub-interval is very short and almost invisible in Fig.4.2.16.

$Interval t_1 \leq t \leq t_2$: see Fig.4.2.17(b). When D_1 turns off, diode D_o becomes forward polarized, and the energy transfer to the output begins through a resonance between L_S and the series connection of C_1 and C_b. According to the hypothesis made, a half cycle resonance is completed before the end of the switch on time.

$Interval\, t_2 \leq t \leq t_3$: see Fig.4.2.17(c). During the remaining part of the switch on time, the transformer primary inductance $L_\mu + L_p$ is charged by the input voltage, until the switch is turned off at instant t_3.

$Interval\, t_3 \leq t \leq t_4$: see Fig.4.2.17(d). At the switch turn off instant, diodes D_b and D_1 turn on and the primary current i_{L_p} decreases toward zero in a resonant manner, involving L_s, L_p, L_μ, C_1 and C_b . When it reaches zero at instant t_4 diode D_b turns off.

$Interval\, t_4 \leq t \leq t_5$: see Fig. 4.2.17(e). This sub-topology remains active until the end of the switching period under Mode 1 operation. However, since during this interval capacitor C_1 is charged, it may happen that diode D_b becomes forward polarized (Mode 2), giving rise to the same sub-topology of Fig.4.2.17(d), as shown in the interval $t_5 \leq t \leq t_6$ of Fig.4.2.16(b).

In order to validate the simulation results and theoretical analysis, a prototype was built according to the specification listed in the image of Fig.4.2.18, where the design parameters are reported too. The employed MOSFET and diodes are: $S = AUIRFD4310Z$, $D_b = 20CWT10FN$, and $D_o = D_1 = IDD03SG60$.

The main converter waveforms, taken at nominal conditions for $V_g = 25V$, and for $V_g = 35V$, can be seen in Fig.4.2.19(a) and Fig.4.2.19(b), respectively. Note the good agreement with the theoretical waveforms of Fig.4.2.16 (current $i_{L_s}(t) = i_{D_o}(t) - i_{D_1}(t)$). The maximum switch voltage stress is roughly 90 V, considering the small high frequency ringing at its turn off. The converter efficiency as a function of input voltage, taken at nominal output voltage and power, is reported in Fig.4.2.20: these values are aligned with other high step-up converter topologies designed for the same specifications that is possible to find in literature.

TABLE III
HIGH-GAIN CONVERTER SPECIFICATIONS

Parameter	**Symbol**	**Value**	
Minimum input voltage	$V_{g_{min}}$	25	V
Maximum input voltage	$V_{g_{max}}$	35	V
Output voltage	V_o	400	V
Output power	P_o	300	W
Switching frequency	f_{sw}	300	kHz

TABLE IV
HIGH-GAIN CONVERTER PARAMETERS

Parameter	**Symbol**	**Value**	
Input capacitor	C_{in}	$2.2 + 10$	μF
Boost capacitor	C_b	$0.1 + 1$	μF
Output capacitor	C_o	1	μF
Voltage doubler capacitor	C_1	0.1	μF
Magnetizing inductance	L_μ	21	μH
Primary leakage inductance	L_p	1	μH
Secondary leakage inductance	L_s	0.1	μH
Transformer turns ratio	n	4	

Figure 4.2.18: High gain boost derived prototype specifications and design parameters.

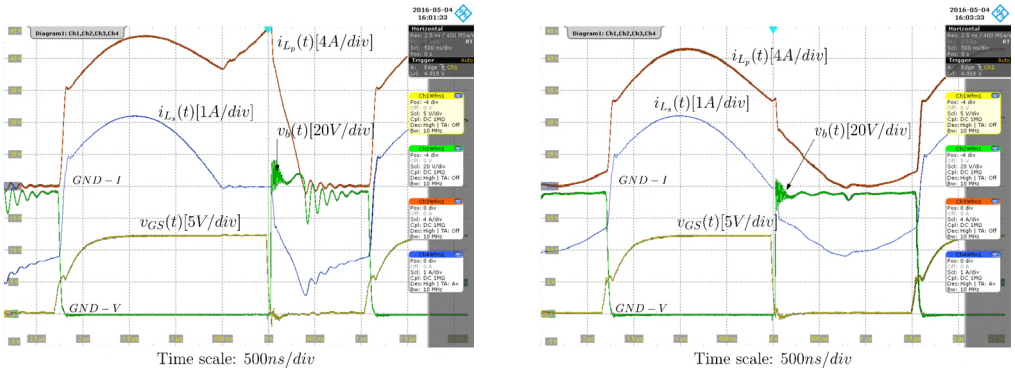


Figure 4.2.19: High gain boost derived topology experimental waveforms for $V_g = 25V$ (left) and $V_g = 35V$ (right).

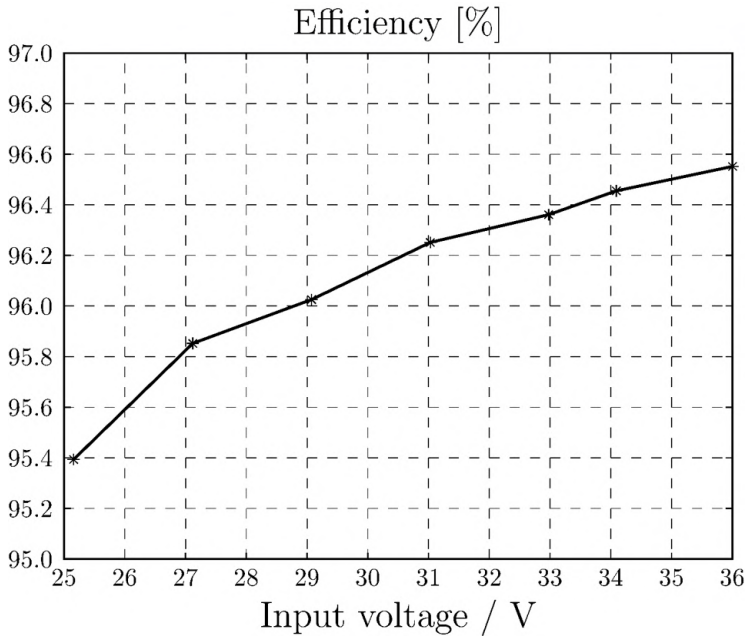


Figure 4.2.20: High gain boost derived topology experimental efficiency.

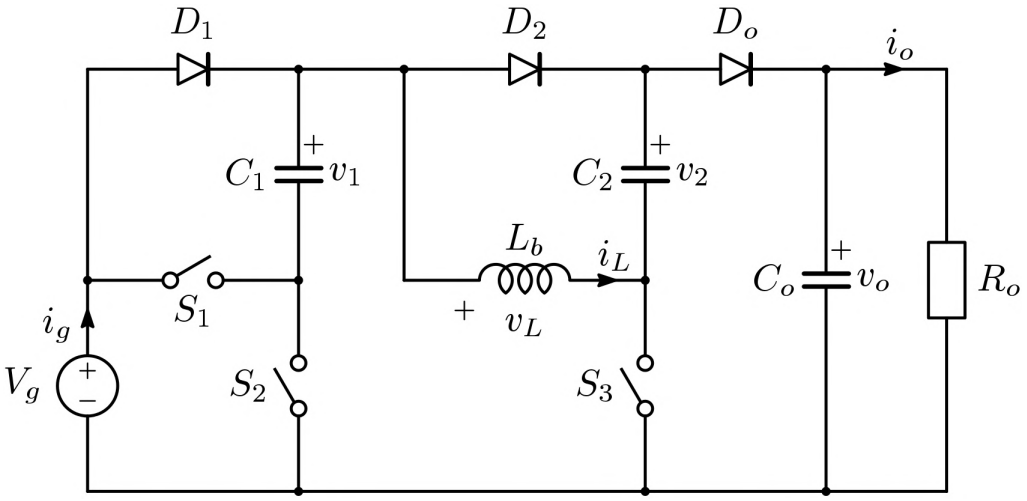


Figure 4.3.1: The new step-up hybrid topology with an expanded range of attainable conversion ratios.

4.3 Reconfigurable Step-up Hybrid Topology

Following the same path that allowed to derive the hybrid step-up buck, it is possible to obtain a new step-up topology with an expanded range of attainable conversion ratios. In this new converter (Fig.4.3.1), two possible switches modulation laws can be implemented, also helping expand the range of attainable conversion ratios.

4.3.1 First Possible Switches Modulation Law: CHP1

In this case, during the converter ON-phase, switches S_1 and S_3 are turned ON, while S_2 is OFF. The converter equivalent circuit is shown in Fig.4.3.2 and, as it is possible to see in the picture, capacitor C_2 is charged by the series of V_g and C_1, while the inductor voltage is equal to $V_g + v_1$. The output diode D_o is OFF, therefore the energy is delivered to the load by the output capacitor C_o.

During the OFF-phase instead (Fig.4.3.3), switch S_2 is ON, while S_1 and S_3 are OFF. C_1 is charged to V_g, and this allows us to estimate the charging voltage of C_2 as $2V_g$. Knowing v_2, the inductor voltage can be estimated as $3V_g - v_o$.

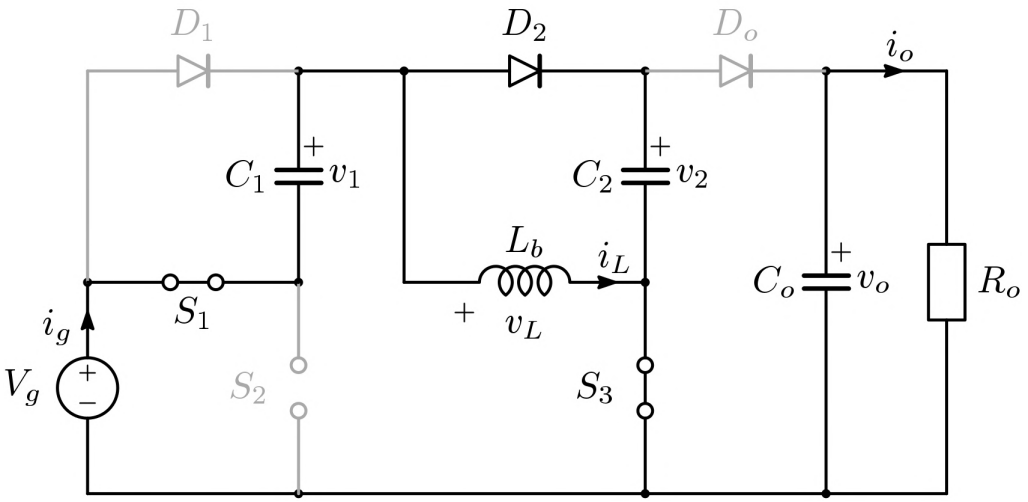


Figure 4.3.2: New step-up hybrid topology first possible modulation law: ON-phase equivalent circuit.

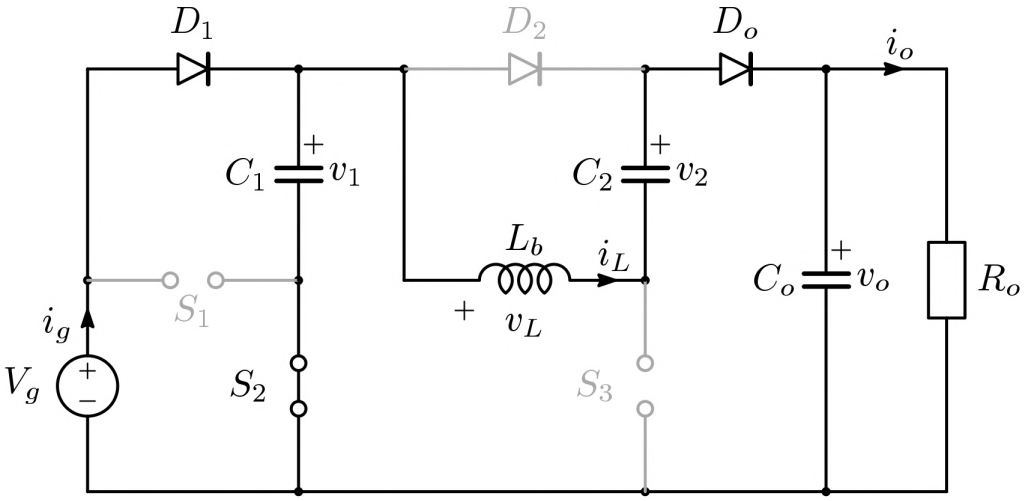


Figure 4.3.3: New step-up hybrid topology first possible modulation law: OFF-phase equivalent circuit.

Identifying DT_s as the duration of the converter ON-phase, and knowing the inductor voltage in each phase, the steady-state operation hypothesis allows us to derive the converter conversion ratio, that is

$$M = \frac{v_o}{V_g} = \frac{3 - D}{1 - D}$$

It is now interesting to estimate the switches and diodes voltage stress (Fig.4.3.4 and 4.3.5). Observing the ON-phase equivalent circuit, it is possible to immediately estimate the voltage stress on S_2, D_1 and D_o as

$$v_{s_2} = V_g$$

$$v_{D_1} = v_1 = V_g$$

$$v_{D_o} = v_o - v_2 = (M - 2)\, V_g$$

Studying the OFF-phase equivalent circuit instead, allows us to estimate S_1, S_2 and D_2 voltage stress. It is in fact possible to observe that

$$v_{S_1} = V_g$$

$$v_{S_3} = v_o - v_2 = (M - 2)\, V_g$$

$$v_{D_2} = v_2 - v_L = (M - 1)\, V_g$$

4.3.2 Second Possible Switches Modulation Law: CHP2

In this case, during the converter ON-phase (Fig.4.3.6), switches S_2 and S_3 are ON, while S_1 is OFF. Both the capacitors are therefore charged to V_g, that is also the inductor voltage. In the OFF-phase instead (Fig.4.3.7), the switch S_1 is ON, and the capacitors are connected in series to charge C_o. The inductor voltage is equal to $3V_g - v_o$.

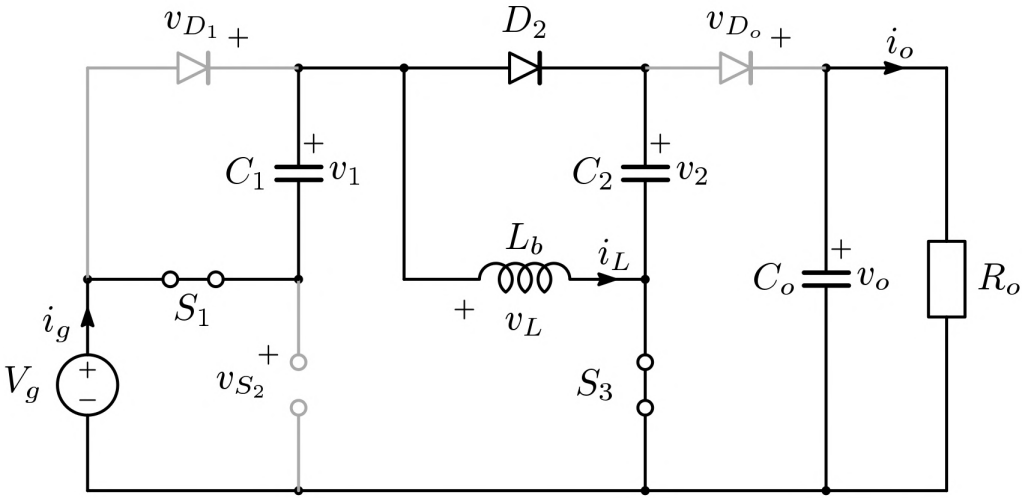


Figure 4.3.4: New step-up hybrid topology first possible modulation law voltage stress estimation: ON-phase equivalent circuit.

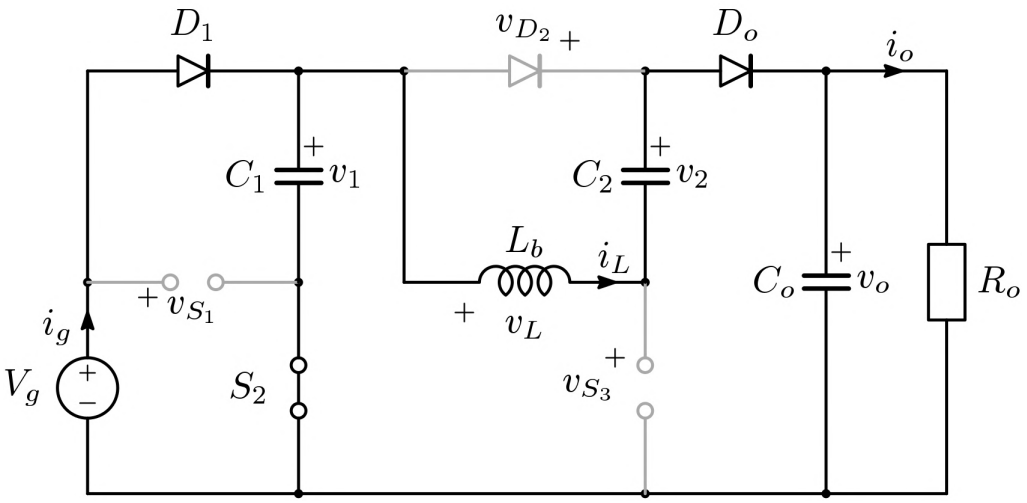


Figure 4.3.5: New step-up hybrid topology first possible modulation law voltage stress estimation: OFF-phase equivalent circuit.

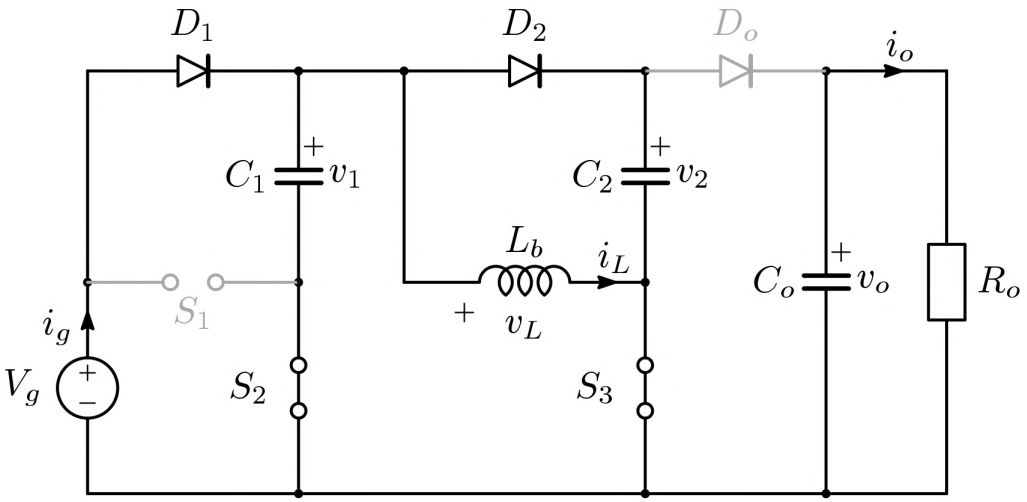


Figure 4.3.6: New step-up hybrid topology second possible modulation law: ON-phase equivalent circuit.

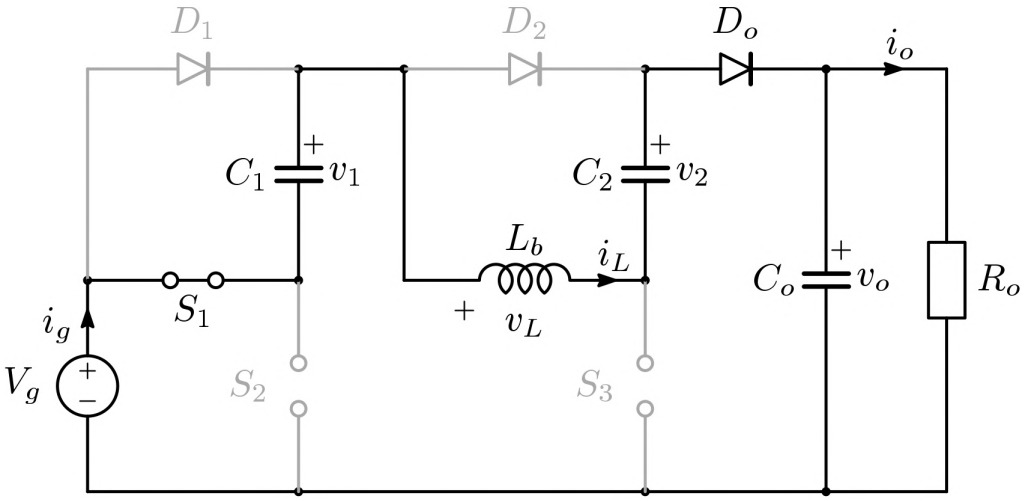


Figure 4.3.7: New step-up hybrid topology second possible modulation law: OFF-phase equivalent circuit.

Identifying DT_s as the duration of the converter ON-phase, and knowing the inductor voltage in each phase, the steady-state operation hypothesis allows us to derive the converter conversion ratio, that is

$$M = \frac{v_o}{V_g} = \frac{3 - 2D}{1 - D}$$

After deriving the conversion ratio, it is interesting to estimate the switches and diodes voltage stress. Looking at Fig.4.3.6, it is possible to calculate the voltage stress on S_1 and D_o, given by

$$v_{S_1} = V_g$$

and

$$v_{D_o} = v_o - V_g = (M - 1)\, V_g$$

Considering the OFF-phase equivalent circuit instead (Fig.4.3.7), it is possible to complete the voltage stress analysis, observing that

$$v_{S_2} = V_g$$

$$v_{D_1} = v_1 = V_g$$

$$v_{S_3} = v_o - v_2 = (M - 1)\, V_g$$

$$v_{D_2} = v_2 - v_L = (M - 2)\, V_g$$

4.3.3 Magnetic Element Requirements

It is now interesting to estimate the inductor current average value and ripple. Let's start from the latter. Knowing the voltage v_L in each phase, it is pretty straightforward to calculate

$$\Delta i_{LCHP1} = \frac{2V_g}{Lf_s} D = \frac{2V_g}{Lf_s} \left(\frac{M - 3}{M - 1} \right)$$

$$\Delta i_{L\,CHP2} = \frac{V_g}{L f_s} D = \frac{V_g}{L f_s} \left(\frac{M-3}{M-2} \right)$$

The average inductor current can instead be evaluated noting that, under steady-state operation hypothesis, every capacitor average current is equal to zero. Therefore, looking at the topology schematic (Fig.4.3.1), it is possible to write the following equations, valid in both operating modes:

$$\overline{i_{D_2}} = \overline{i_{D_o}} = \overline{i_o} = I_o$$

$$I_L = \overline{i_{D_1}} - \overline{i_{D_2}} = \overline{i_{D_1}} - I_o$$

To be able to express I_L as a function of I_o, we need to estimate $\overline{i_{D_1}}$, whose value varies depending on which modulation law is considered.

In the first modulation case (see Fig.4.3.2 and 4.3.3), it can be noticed that

$$i_{D_1} = \begin{cases} i_L + i_{D_2} & ON - phase \\ 0 & OFF - phase \end{cases}$$

We can therefore estimate D_1 average current value as $\overline{i_{D_1}} = \frac{1}{T_s} \int_0^{DT_s} (i_L + i_{D_2})\, dt$. From this equation we get

$$\overline{i_{D_1}} = \frac{1}{T_s} \left(\int_0^{DT_s} i_L dt + \int_0^{DT_s} i_{D_2} dt \right) = \frac{1}{T_s} \int_0^{DT_s} i_L dt + \overline{i_{D_2}} = D I_L + I_o$$

After estimating $\overline{i_{D_1}}$, and knowing that $D = \frac{M-3}{M-1}$, it is finally possible to calculate the average inductor current as a function of the conversion ratio M, obtaining

$$I_L = \frac{(M-1)}{2} I_o$$

In the second modulation case (see Fig.4.3.6 and 4.3.7), it must be remembered that

$$i_{S_1} = \begin{cases} 0 & ON - phase \\ i_L & OFF - phase \end{cases}$$

Its average value is then

$$\overline{i_{S_1}} = (1 - D)\, I_L = \frac{1}{(M-2)} I_L$$

Knowing that $\overline{i_{D_1}}$ is given by the average input current (that is MI_o) minus $\overline{i_{S_1}}$, its value can be estimated as

$$\overline{i_{D_1}} = MI_o - \frac{1}{(M-2)} I_L$$

Recalling that $I_L = \overline{i_{D_1}} - I_o$, we can then write

$$I_L = MI_o - \frac{1}{(M-2)} I_L - I_o$$

The previous equation allows us to estimate the average inductor current in the CHP2 modulation case as

$$I_L = (M-2)\, I_o$$

The average inductor current in the hybrid step-up converter is then given by

$$I_{LCHP1} = \frac{(M-1)}{2} I_o$$

$$I_{LCHP2} = (M-2)\, I_o$$

where $CHP1$ and $CHP2$ denote the first and second possible modulation law cases. It is possible to notice that in both cases the average inductor current is reduced in comparison with an equivalent standard boost case, where $I_L = MI_o$. The inductor current ripple instead, can be higher than in a standard boost converter when employing $CHP1$ modulation law. Resuming the converter characteristics, it is also interesting to notice that, even though the number of components needed in the hybrid topology is much higher than that of a standard boost, the voltage stress on them is in most of the cases greatly reduced. Even the maximum voltage stress value is reduced, being equal to $(M-1)\, V_g$ instead of MV_g.

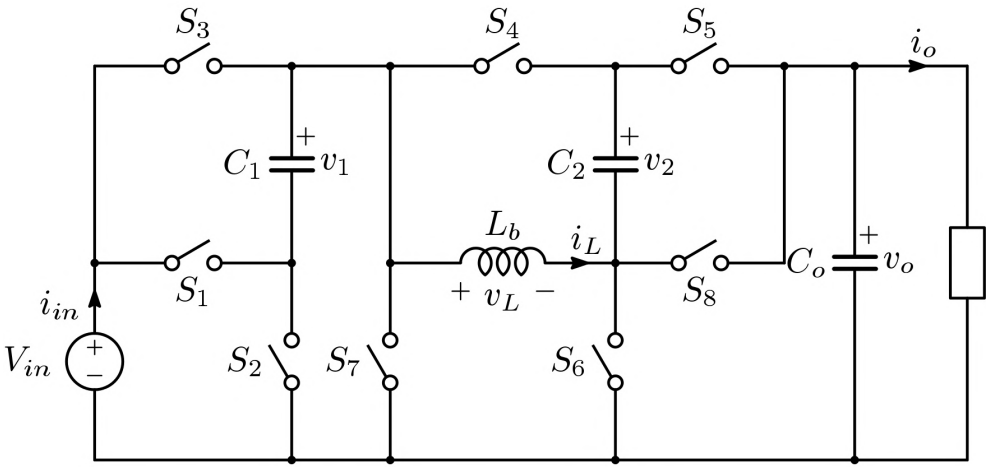


Figure 4.4.1: Reconfigurable buck-boost hybrid topology.

4.4 Reconfigurable Buck-boost Hybrid Topology

The hybrid topology introduced in the previous section has the advantage of a reduced average inductor current, but due to its step-up only nature it is not fit for the targeted automotive application. Since reconfigurability (that is changing the switches modulation law to implement different conversion ratios) was already exploited to obtain advantages over a standard topology, it can be further used to obtain step-down capability too. This goal is met inserting two additional switches in the previous step-up hybrid converter, the resulting topology can be seen in Fig.4.4.1. The extra-switches, employed to obtain the step-down capability, are S_7 and S_8.

This topology allows eight different operating modes, depending on which switches are kept ON and OFF respectively, and on the modulation law. In particular a four switches buck-boost can be implemented and as a consequence the three basic inductive converters, buck, boost and buck-boost operation can be emulated. KY operation can also be implemented. Furthermore, the topology allows four additional hybrid operation modes, two of which are the ones implemented by previously shown reconfigurable step-up hybrid topology, the so called CHP1 and CHP2 operating modes.

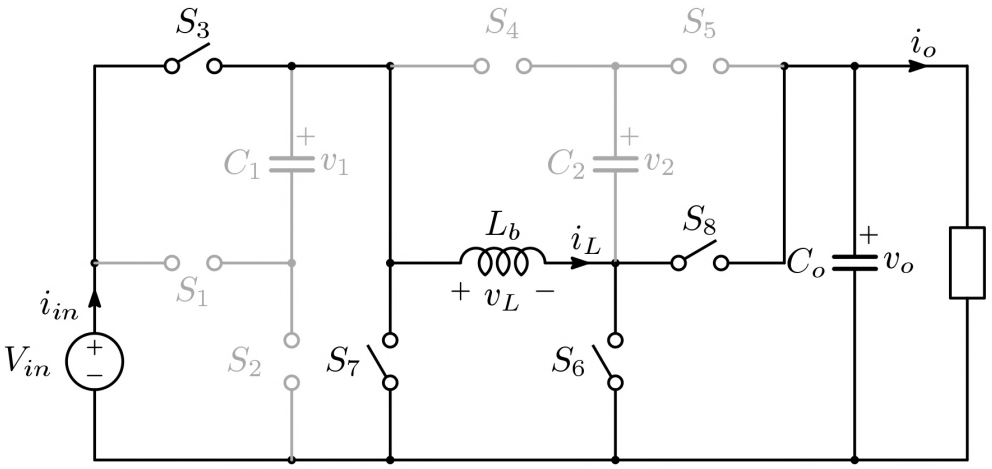


Figure 4.4.2: Reconfigurable buck-boost hybrid topology: four switches buck-boost converter emulation.

4.4.1 Operating Modes

In the following the different operation modes will be shown in detail, highlighting the converter equivalent circuit in each operating phase.

4.4.1.1 Basic Inductive Converters Emulation

As previously mentioned, the converter can be configured in such a way to implement a four switches buck-boost. This is obtained by keeping switches S_1, S_2, S_4 and S_5 constantly off, while modulating the other four. The resulting equivalent circuit in shown in Fig.4.4.2. It is straightforward to understand how, by changing the switches modulation law, this operating mode allows the standard buck and boost converter emulation. In the first case it is sufficient to keep S_6 constantly OFF, S_8 constantly ON and modulate S_3 and S_7. In the second case, S_2 and S_3 are kept constantly ON (C_1 is always in parallel with the input), S_7 is constantly off, while S_6 and S_8 are modulated.

4.4.1.2 KY Mode

The reconfigurable buck boost hybrid topology not only implements the standard inductor based topologies previously presented, but also offers five different hybrid operating modes. In particular it also implements the previously

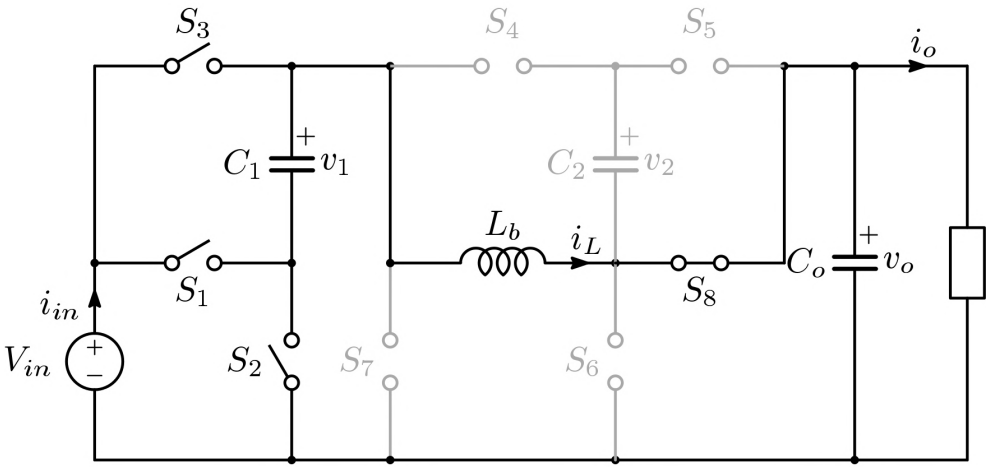


Figure 4.4.3: Reconfigurable buck-boost hybrid topology: KY converter emulation.

presented KY converter. The equivalent topology implementing this operating mode is shown in Fig.4.4.3; switches S_4, S_5, S_6 and S_7 are kept inactive, S_8 is always ON, while S_1, S_2 and S_3 are modulated (Fig.4.4.3). Since the analysis of this operating mode was already performed in 4.4.1.2, it won't be shown again here.

4.4.1.3 CHP1 and CHP2 Mode

As previously said, the reconfigurable buck-boost hybrid topology was derived from the reconfigurable hybrid step-up topology by adding switches S_7 and S_8. Therefore, if these two are constantly OFF, while all the others are modulated, what we get is the hybrid step-up converter. As a consequence, operating modes CHP1 and CHP2 can be implemented (Fig.4.4.4). In this case the converter operation and characteristics remain unchanged if compared to what shown in sections 4.3.1 and 4.3.2 and therefore will not be reported here.

4.4.1.4 CHP3 Mode

In CHP3 operating mode (Fig.4.4.5), switches S_4, S_5 and S_7 are inactive, while all the others are modulated. During the ON-phase (Fig.4.4.6), switches

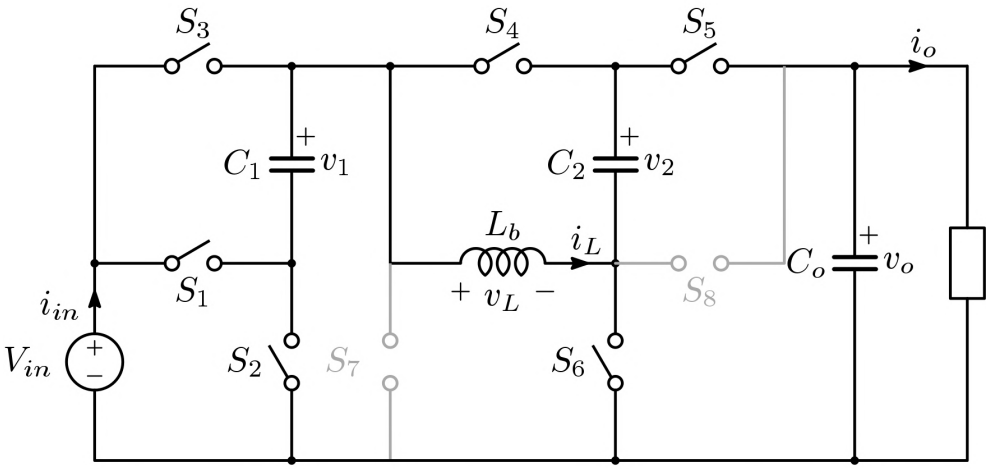


Figure 4.4.4: Reconfigurable buck-boost hybrid converter: hybrid step-up topology emulation.

S_1 and S_6 are ON, so that C_1in connected in series with V_{in} and $v_L = V_{in}+v_1$, while the output capacitor C_o is providing energy to the load.

During the OFF-phase instead (Fig.4.4.7), capacitor C_1 is charged to V_{in} and the inductor voltage is $v_L = V_{in} - v_o$.

Knowing the inductor voltage in both operating phases and exploiting the steady-state operation hypothesis, it is possible to write

$$2DV_{in} = (v_o - V_{in})(1 - D)$$

The previous equation can be used to estimate the conversion ratio, that is

$$M = \frac{v_o}{V_{in}} = \frac{1 + D}{1 - D}$$

4.4.1.5 CHP4 Mode

In CHP4 operating mode (Fig.4.4.8), switches S_4, S_5 and S_7 are inactive, while all the others are modulated. During the ON-phase (Fig.4.4.9), switches S_2, S_3 and S_6 are ON and C_1 is charged to V_{in}, that is also the voltage applied to the inductor.

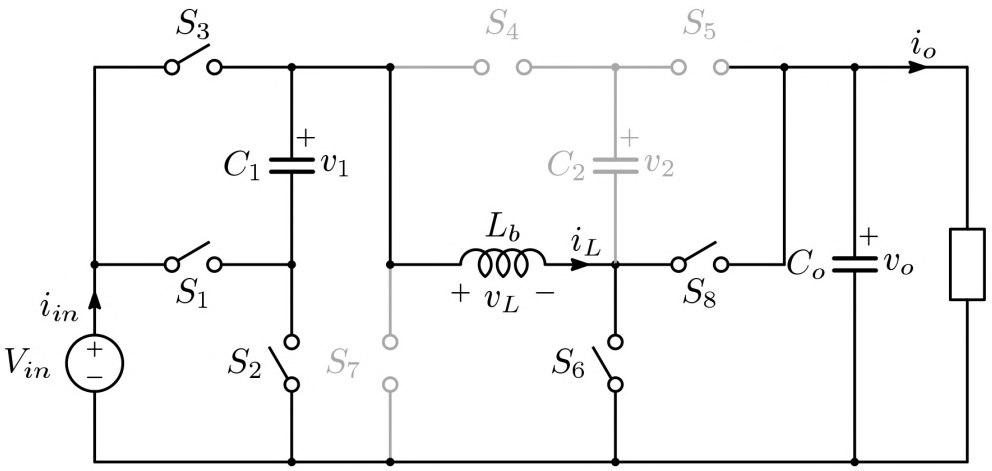


Figure 4.4.5: CHP3 hybrid operating mode.

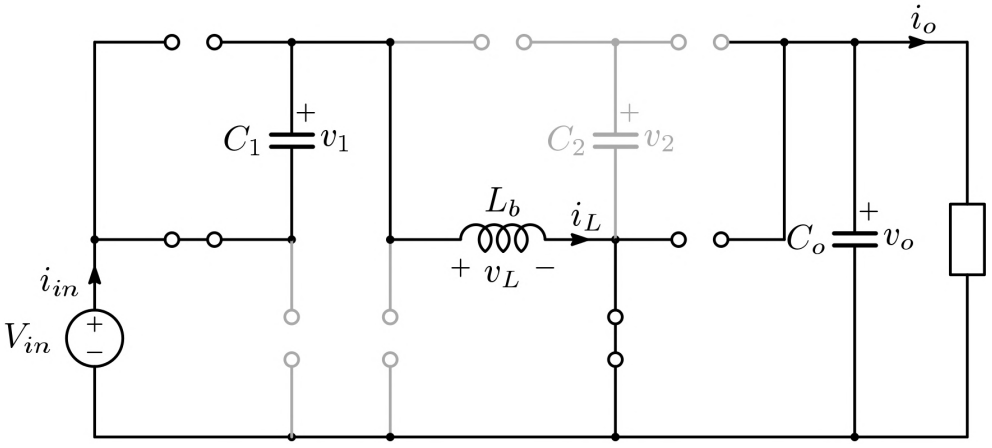


Figure 4.4.6: CHP3 mode: ON-phase equivalent circuit.

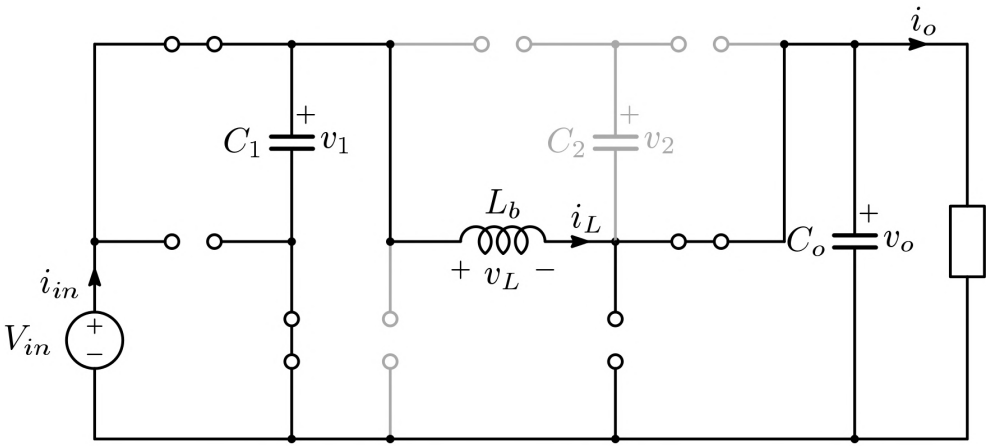


Figure 4.4.7: CHP3 mode: OFF-phase equivalent circuit.

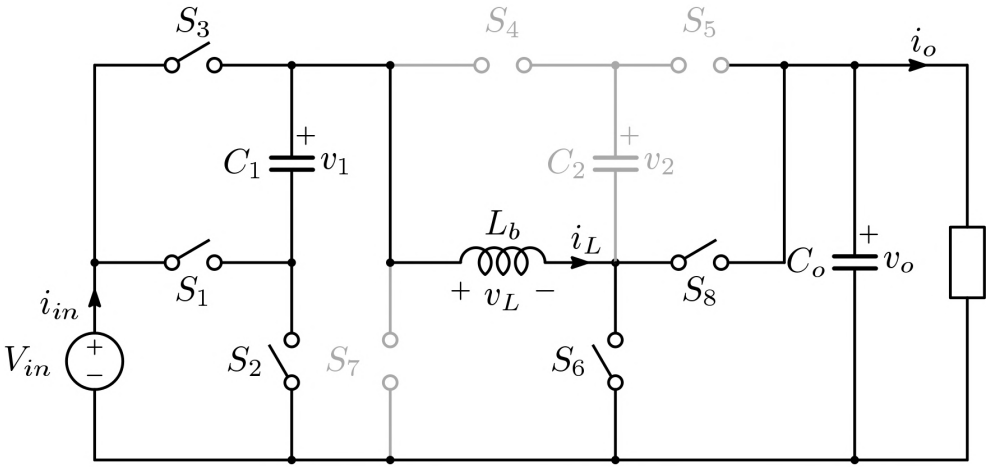


Figure 4.4.8: CHP4 hybrid operating mode.

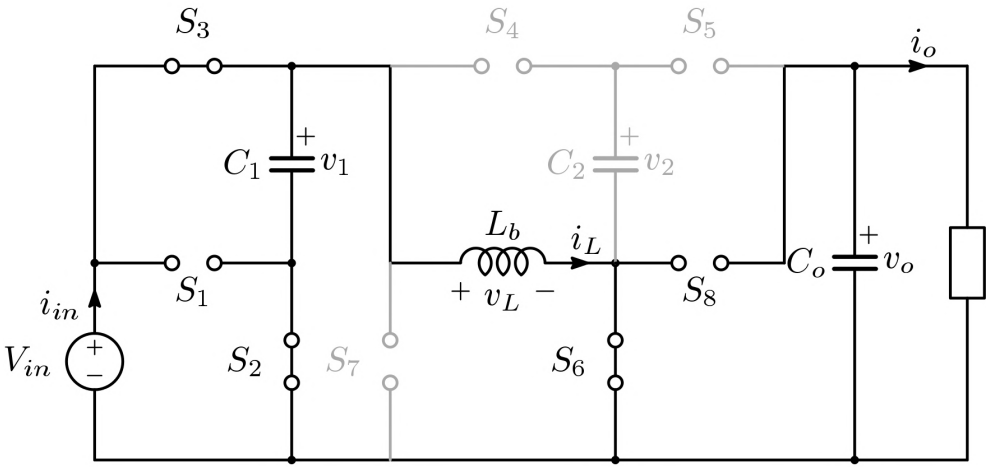


Figure 4.4.9: CHP4 mode: ON-phase equivalent circuit.

During the OFF-phase instead, capacitor C_1 is connected in series with V_{in} and $v_L = 2V_{in} - v_o$.
Knowing the inductor voltage in both operating phases, and exploiting the steady-state operation hypothesis, we can write the following equation

$$DV_{in} = (v_o - 2V_{in})(1 - D)$$

It is then possible to estimate the voltage conversion ratio as

$$M = \frac{v_o}{V_{in}} = \frac{2 - D}{1 - D}$$

4.4.2 Magnetic Element Requirements Analysis

As previously reported, one of the key goals in designing a hybrid converter is the magnetic elements requirements reduction if compared to a standard inductor based topology. It is therefore important to estimate these requirements in our newly developed topology. Since the requirements in the buck, boost and buck boost case are well known, and the KY converter together together with the CHP1 and CHP2 operating modes have already been studied, in this section only the analysis carried out on the hybrid modes CHP3 and CHP4 is shown.

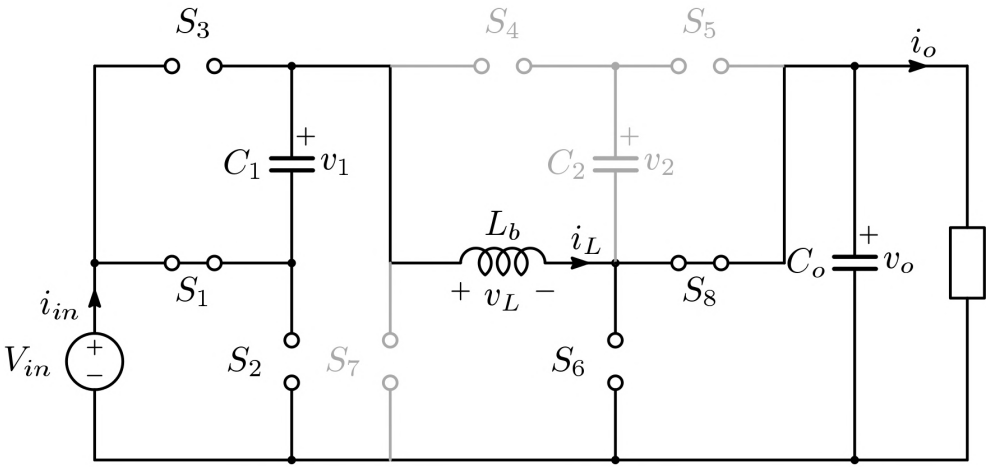


Figure 4.4.10: CHP4 mode: OFF-phase equivalent circuit.

4.4.2.1 Average Inductor Current Estimation

CHP3 Mode To calculate the average inductor current when the converter is operating in CHP3 mode, the equivalent circuit must be considered. As it is possible to see looking at Fig.4.4.6 and 4.4.7, it is possible to write the following equation regarding the average load current I_o

$$\overline{i_{S_8}} = I_o + \overline{i_{C_o}}$$

Under steady-state operation hypothesis, any capacitor average current is zero, therefore $\overline{i_{S_8}} = I_o$.
We also know that

$$i_{S_8} = \begin{cases} 0 & ON - phase \\ i_L & OFF - phase \end{cases}$$

we can therefore write the following equation

$$\overline{i_{S_8}} = (1 - D)\, I_L \tag{4.4.1}$$

Knowing that the conversion ratio for CHP3 mode is

$$M = \frac{1 + D}{1 - D}$$

it is possible to estimate the duty cycle as a function of M, obtaining

$$D = \frac{M-1}{M+1}$$

Finally, substituting the previous in (4.4.1), we get

$$I_L = \left(\frac{M+1}{2}\right) I_o$$

CHP4 Mode Since the output stage is the same in CHP4 and CHP3 mode, the considerations made in the previous section are still valid. Therefore, it is still possible to write

$$I_o = (1-D)\, I_L$$

Knowing that the conversion ratio for CHP4 mode is

$$M = \frac{2-D}{1-D}$$

it is possible to estimate the duty cycle as a function of M, obtaining

$$D = \frac{M-2}{M-1}$$

Finally we get

$$I_L = (M-1)\, I_o$$

Average Inductor Current Comparison After estimating the average inductor current value for every operating mode, a comparison with an equivalent buck-boost topology can be performed.

Fig.4.4.11 shows this comparison in the case of a maximum requested conversion ratio equal to ten. The hybrid modes duty cycle variation was limited in between 40 and 60%, except for CHP1, that is used to provide the higher conversion ratios up to the maximum value of ten. Even though this is just an example, it is possible to notice how the hybrid topology allows a strong

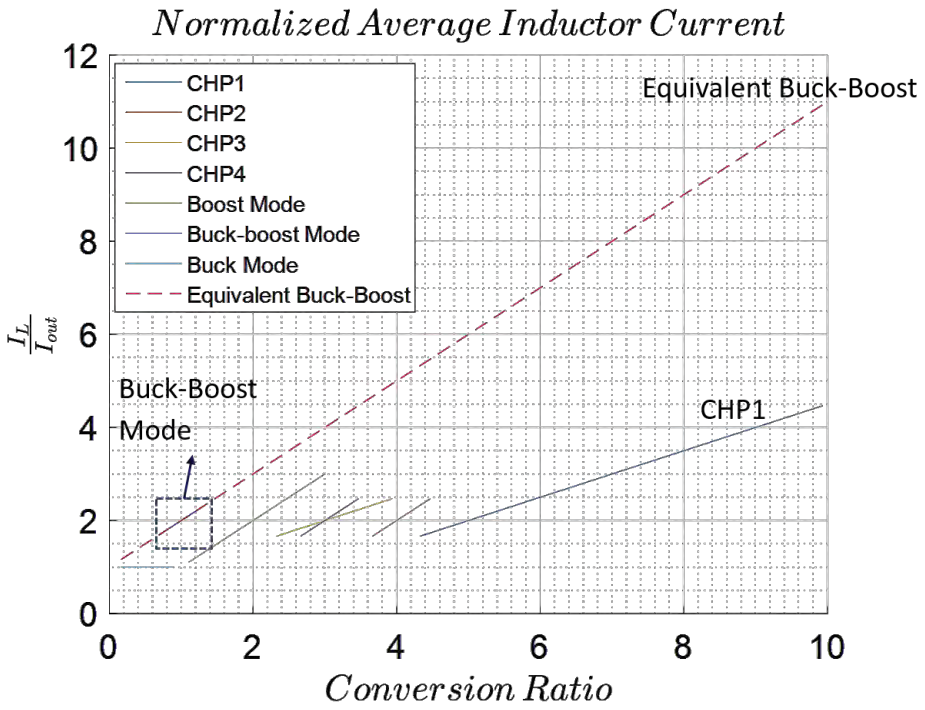


Figure 4.4.11: Normalized average inductor current comparison.

reduction in the average inductor current if compared to an equivalent buck-boost capable of handling the same requested conversion ratio range. It is also important to notice how reconfigurability can be exploited to maximize the average inductor current reduction by changing the operating mode based on the requested conversion ratio.

4.4.2.2 Inductor Current Ripple

The inductor current ripple can be easily estimated observing the inductor voltage. Since, as seen in the average inductor current estimation case, all but CHP3 and CHP4 operating modes have been previously analysed, in the following just the results concerning CHP3 and CHP4 modes will be shown.

CHP3 Mode In this case the inductor current voltage is given by the following equation

$$\Delta i_{LCHP3} = \frac{2V_{in}}{Lf_s} D$$

Knowing the relation between the duty cycle and the conversion ratio, it is easy to estimate

$$\Delta i_{LCHP3} = \frac{2V_{in}}{Lf_s} \left(\frac{M-1}{M+1} \right)$$

CHP4 Mode In this case the inductor current ripple is given by the following equation

$$\Delta i_{LCHP4} = \frac{V_{in}}{Lf_s} D$$

Knowing the relation between the duty cycle and the conversion ratio, it is easy to estimate

$$\Delta i_{LCHP4} = \frac{V_{in}}{Lf_s} \left(\frac{M-2}{M-1} \right)$$

Inductor Current Ripple Comparison To compare the inductor current ripple in the various converter operating modes with an equivalent buck-boost topology, a normalization current I_n is defined

$$I_n = \frac{V_{in}}{Lf_S}$$

Fig.4.4.12 shows this comparison under the same conditions considered for the average inductor current comparison: a maximum requested conversion ratio equal to ten and hybrid modes duty cycle variation limited in between 40 and 60%, except for CHP1, used to provide the higher conversion ratios up to ten.

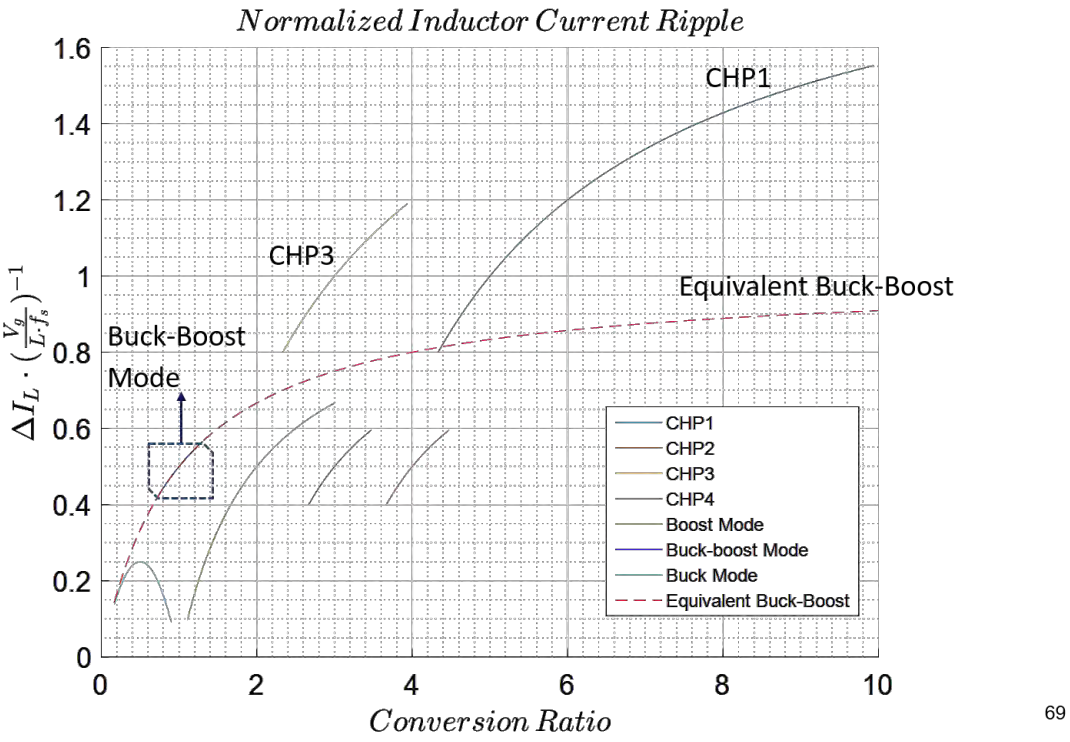


Figure 4.4.12: Normalized inductor current ripple comparison. In this graph $V_g = V_{in}$.

4.4.3 Voltage Stress

After studying the converter operation and the magnetic element requirements, it is interesting to estimate the switching devices voltage stress. This parameter is particularly interesting in integrated applications, where it is in fact related to the technology that can be used to implement the circuit. Before showing the calculation results, some considerations can be made. First of all, it is interesting to notice that, as shown in the operating modes description, the voltage of the circuit node corresponding to C_1 positive terminal can only be equal to 0, V_{in} or $2V_{in}$. As a consequence, since C_1 can only be either discharged or charged to V_{in}, it is straightforward to understand that, in the case of S_1, S_2 and S_3 the voltage stress can only be equal to V_{in}, while in S_7 case it can only be V_{in} or $2V_{in}$. In the other switches case instead, things are not so straightforward. For example, in S_6 case, the worst-case voltage stress depends on the maximum conversion ratio implemented by each hybrid mode; the same is true for S_5 and S_4, while S_8's is clearly the maximum output voltage. It must also be noticed that, due to its limited regulation capabilities, KY mode would be probably seldom used in practice. The corresponding voltage stress is reported only to give a complete converter analysis.

The switches voltage stress in nominal conditions for every operating mode is shown in table 4.1. The worst-case evaluations are instead resumed in table 4.2. As previously mentioned, it is important to notice that the worst-case voltage stress values strongly depend on the chosen operating sequence; in fact, changing the maximum and minimum conversion ratios implemented by a given operating mode, the worst-case voltage stress of some switches can change, as it is possible to see in S_4, S_5 and S_6 case. Therefore, it is immediately clear that a more accurate worst-case voltage stress estimation should be performed again after studying the transition characteristics and developing a proper control technique.
Despite the previous considerations, some interesting observations based on the performed voltage stress evaluation can be made. For example, it is interesting to notice how, for some switches, the voltage stress can be both positive and negative.
One example of this is S_2; despite the nominal values worst-case evaluations showing that the negative polarity voltage stress is zero, it must in fact be noticed that the switch voltage stress in buck mode is equal to $-v_1$ (capacitor C_1 charging voltage). Despite being v_1 equal to zero in steady-state,

Operating mode		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Buck	ϕ_{ON}	0	V_{in}	–	$V_{in} - v_o$	0	v_o	V_{in}	–
	ϕ_{OFF}	V_{in}	0	V_{in}	$-v_o$	0	v_o	–	–
Buck-Boost	ϕ_{ON}	0	V_{in}	–	V_{in}	$-v_o$	–	V_{in}	$-v_o$
	ϕ_{OFF}	V_{in}	0	V_{in}	$-v_o$	0	v_o	–	–
Boost	ϕ_{ON}	V_{in}	–	–	V_{in}	$-v_o$	–	V_{in}	$-v_o$
	ϕ_{OFF}	V_{in}	–	–	$V_{in} - v_o$	0	v_o	V_{in}	–
KY	ϕ_{ON}	–	V_{in}	$-V_{in}$	$2V_{in} - v_o$	0	v_o	$2V_{in}$	–
	ϕ_{OFF}	V_{in}	–	–	$V_{in} - v_o$	0	v_o	V_{in}	–
CHP4	ϕ_{ON}	V_{in}	–	–	V_{in}	$-v_o$	–	V_{in}	$-v_o$
	ϕ_{OFF}	–	V_{in}	$-V_{in}$	$2V_{in} - v_o$	0	v_o	$2V_{in}$	–
CHP3	ϕ_{ON}	–	V_{in}	$-V_{in}$	$2V_{in}$	$-v_o$	–	$2V_{in}$	$-v_o$
	ϕ_{OFF}	V_{in}	–	–	$V_{in} - v_o$	0	v_o	V_{in}	–
CHP2	ϕ_{ON}	V_{in}	–	–	–	$V_{in} - v_o$	–	V_{in}	$-v_o$
	ϕ_{OFF}	–	V_{in}	$-V_{in}$	$2V_{in} - v_o$	–	$v_o - V_{in}$	$2V_{in}$	$-V_{in}$
CHP1	ϕ_{ON}	–	V_{in}	$-V_{in}$	–	$2V_{in} - v_o$	–	$2V_{in}$	$-v_o$
	ϕ_{OFF}	V_{in}	–	–	$V_{in} - v_o$	–	$v_o - 2V_{in}$	V_{in}	$-2V_{in}$

Table 4.1: Nominal switches voltage stress for every operating mode.

	Positive Stress Polarity	Negative Stress Polarity
S_1	$V_{in\,M}$	–
S_2	$V_{in\,M}$	0^*
S_3	$V_{in\,M}$	$-V_{in\,M}$
S_4	$2V_{in\,M}$	$min\left\{(2V_{in} - v_o)_{CHP4}\,,\,(V_{in} - v_o)_{CHP3}\,,\,(2V_{in} - v_o)_{CHP2}\,,\,(V_{in} - v_o)_{CHP1}\right\}$
S_5	0^{**}	$min\left\{v_{oCHP3}\,,\,v_{oCHP4}\,,\,(2V_{in} - v_o)_{CHP2}\,,\,(V_{in} - v_o)_{CHP1}\right\}$
S_6	$max\left\{v_{oCHP4}\,,\,v_{oCHP3}\,,\,(v_o - V_{in})_{CHP2}\,,\,(v_o - 2V_{in})_{CHP1}\right\}$	–
S_7	$2V_{in}$	–
S_8	–	v_{oM}

Table 4.2: Worst-case switches voltage stress. Subscripts m and M identify a parameter minimum and maximum value respectively.
*: in buck operation S_2 voltage stress is $-v_1$, where v_1 is capacitor C_1 charging voltage. Such voltage is only equal to zero under steady-state operation hypothesis.
**: it must be noticed that in every operating mode in which S_8 is not always OFF, S_5 voltage stress is equal to $+v_2$, that is C_2 charging voltage. In those mode such voltage is only equal to zero under steady-state operation hypothesis.

this may not be always the case, especially if operating mode transitions are taken into account. However, it must be noticed that, in case the device were implemented using a single MOSFET, a negative voltage would turn the body diode ON. Furthermore, a proper control technique (that is necessary to handle the transitions) could for example guarantee a total discharging of C_1 before transitioning to the buck mode, exploiting the inductor current to draw charge from the aforementioned capacitor. In a similar way, despite the results showing voltage stress of both polarities, S_4 could also be implemented using a single MOS or even a diode, without causing any problem to the converter operation. In the case a positive voltage stress were applied, the device body diode would turn ON, charging C_2, but this would not cause any problem to the converter operation.

Similarly to what has been said in S_2 case, the voltage stress can assume both positive and negative values in the case of S_3 too. Unlike in S_2 and S_4 cases anyway, this time the converter can not function properly if a single MOS implementation is used. To understand this, it is possible to take a look at the buck mode OFF-phase equivalent circuit shown in Fig.4.4.13. As it is possible to see, if S_3 were implemented using a single MOS blocking negative voltages, during the buck mode OFF-phase a short-circuit between the input source and ground would occur. If S_3 were implemented using a positive voltage blocking single MOS instead, problems would arise in every hybrid mode. During the first cell charge-pump phase in fact, in which C_1 is connected in series with the input source, the aforementioned capacitor would be short-circuited, as shown in Fig.4.4.14 in the case of CHP1 mode. Therefore, S_3 should be implemented using a back-to-back MOSFET or, if available, body diode-less devices.
Another example in which the device voltage stress can be both positive and negative in case of non steady-state operation is S_5. In all the operating modes in which S_8 is not always OFF in fact, S_5 voltage stress is equal to $+v_2$, where v_2 is C_2 charging voltage. Despite having $v_2 = 0$ in steady-state condition, it is not possible to guarantee that such condition is always met. Moreover, similarly to S_3 case, using a single MOS for the switch implementation would impede the proper operation of some of the converter operating modes. Looking at Fig.4.4.15 in fact, it is possible to see that, for example, in CHP1 mode the use of a single positive voltage blocking MOS would cause C_2 to be charged by the output instead of the series of V_{in} and C_1, disrupting

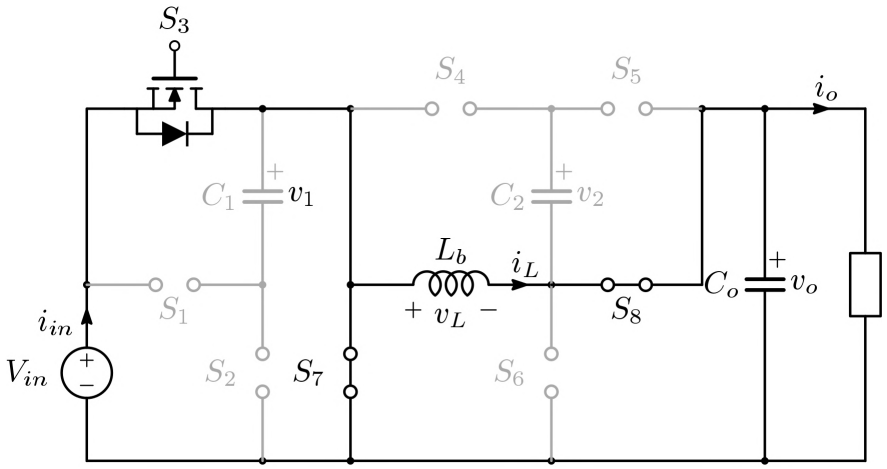


Figure 4.4.13: Buck mode OFF-phase equivalent circuit in the case S_3 is implemented using a single negative voltage blocking MOS device.

the intended converter operation. The minimum theoretical CHP1 conversion ratio is in fact equal to three, therefore we always have $v_o > 2V_{in}$. If a single negative voltage blocking MOS would instead be used, buck-boost operation could not take place. Looking at Fig.4.4.16 in fact, it is possible to see that, during the ON-phase, in the case $v_o < V_{in}$, S_5 body diode would be forward polarized, charging the output capacitor to V_{in}.
All the previous considerations were confirmed right through PLECS® simulation and an example of the possible resulting topology implementation is shown in Fig.4.4.17. Switches S_4, S_7 and S_8 could be implemented using simple diodes while switches S_1, S_2 and S_6 require a single MOS. On the other hand, to avoid to hamper the converter functionality, S_3 and S_5 should be implemented using back-to-back MOSFETs or, if available, body diode-less devices.
Overall, it must be noticed that this paragraph constitutes a preliminary study of this newly proposed topology. The development of a proper control technique is for now beyond the scope of the work, but will need to be studied in the future. The transitions between different operating modes will need to be studied extensively, to understand the converter behaviour in depth and proper control techniques to handle these transitions will need to be studied too. At that time, a proper re-examination of the switches voltage stress will need to be performed.

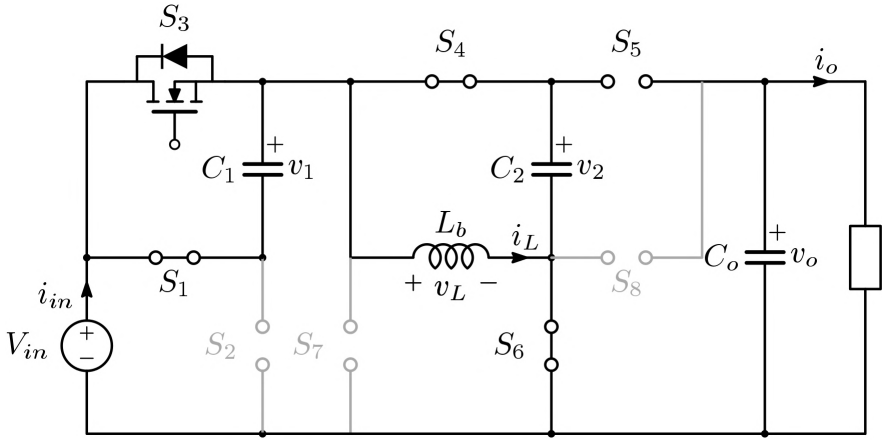


Figure 4.4.14: CHP1 mode ON-phase equivalent circuit in the case S_3 is implemented using a single positive voltage blocking MOS device.

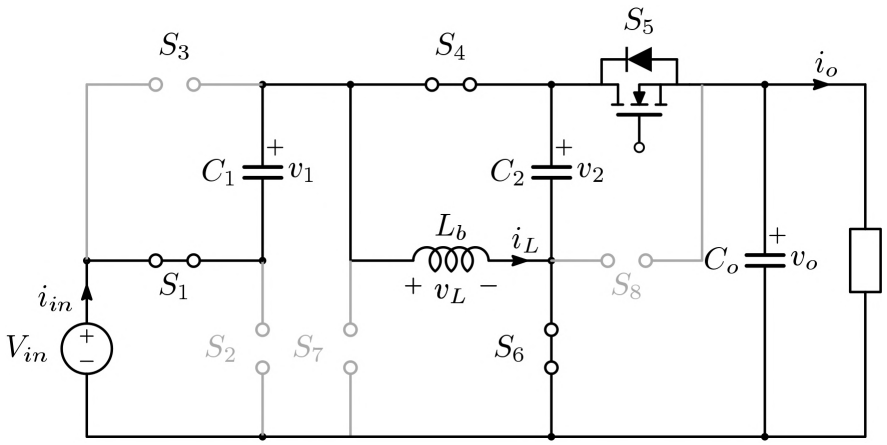


Figure 4.4.15: CHP1 mode OFF-phase equivalent circuit in the case S_5 is implemented using a single positive voltage blocking MOS device.

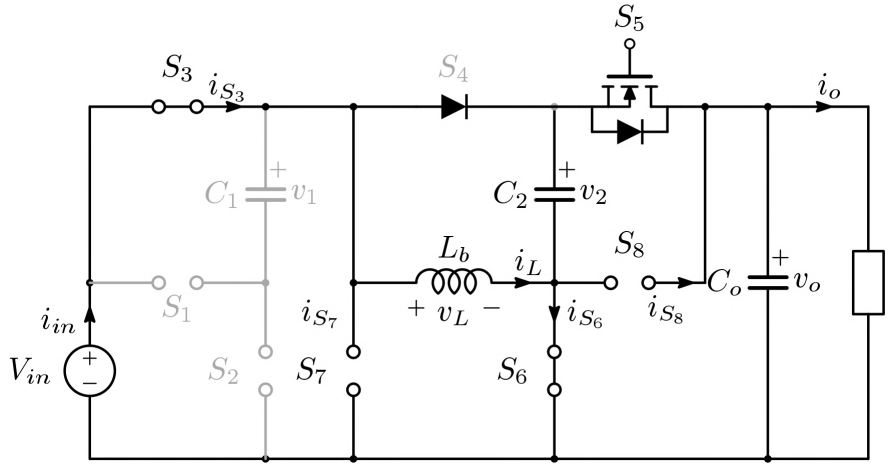


Figure 4.4.16: Buck-boost mode ON-phase equivalent circuit in the case S_5 is implemented using a single negative voltage blocking MOS device.

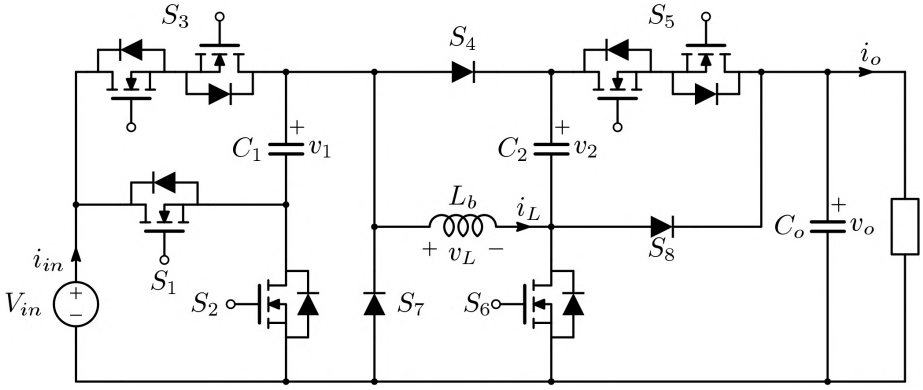


Figure 4.4.17: Possible reconfigurable hybrid buck-boost topology implementation in the case of transitions possible only between adjacent operating modes.

4.5 Reconfigurable Buck-boost Capable Hybrid Topology Simplified Implementation

After studying the properties of the reconfigurable buck-boost capable topology presented in the previous chapter, a simplified version of this converter was designed and implemented as a proof of concept. This prototype (Fig.4.5.1) is a step-up only topology implementing hybrid modes CHP4, CHP2 and CHP1. Mode CHP3 was discarded due to its lack of advantages in comparison with the other hybrid modes; in fact it does not expand the range of possible achievable conversion ratios when the standard boost mode is also implemented, while also being characterized by a higher inductor current ripple than modes CHP2 and CHP4. It should be noted that this simplified prototype is incidentally coincident with a synchronous implementation of the reconfigurable step-up hybrid topology proposed in section 4.3.

The scope of this prototype is testing the hybrid operating modes and verify their feasibility in practice. The proposed simplified prototype application specifications are listed in table 4.3 and mimic a real case automotive lighting application. Two different possible switching frequencies can be selected, 300kHz or 1.8MHz.

With the goal of maximizing the magnetic element requirements reduction, an operating mode sequence was chosen where mode CHP4 is used to yield a maximum conversion ratio of 4.5, while CHP2 maximum conversion ratio is limited to 6.5. The highest conversion ratios are implemented using mode CHP1. Table 4.4 summarizes the chosen operating sequence, while also highlighting the maximum theoretical average inductor current. M_{min} and M_{max} are the minimum and maximum voltage conversion ratio for a given operating mode. $M_{max\,limit}$ is the maximum voltage gain possible in a given operating mode without exceeding the maximum average inductor current specification, corresponding to the average inductor current at $M = 10$ using CHP1 mode. $I_{L\,max}$ is the maximum theoretical average inductor current for a given operating mode and a 70mA load current.

4.5.1 Simplified Prototype Operating Modes

In the simplified prototype implementation operating modes CHP1 and CHP2 remain unchanged if compared to the complete buck-boost capable topology.

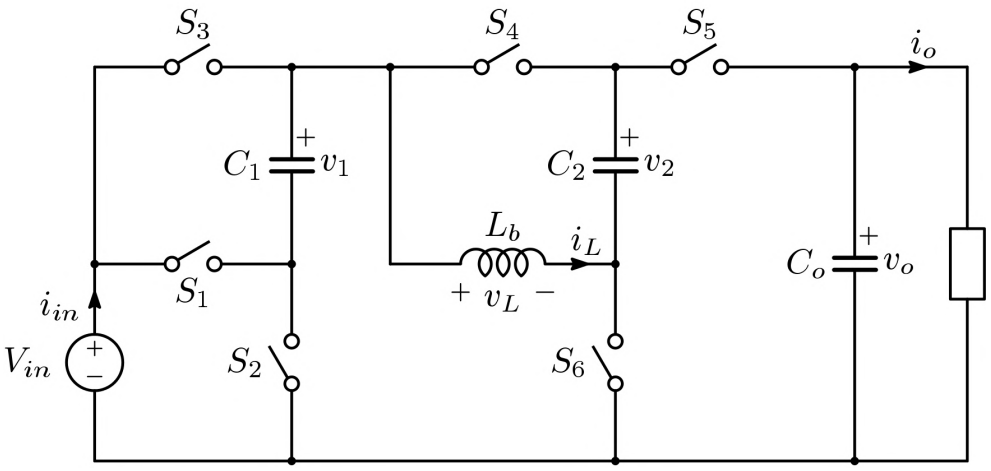


Figure 4.5.1: Simplified reconfigurable topology schematic.

Parameter	Value	Unit
Input Voltage (V_{in})	6 to 18	V
Output Voltage (V_o)	45 to 60	V
Nominal Load current (I_o)	70	mA

Table 4.3: Simplified integrated converter prototype specifications.

	CHP4	CHP2	CHP1
M_{min}	2.5	4	6
M_{max}	4.5	6.5	10
$M_{max\,limit}$	5.5	6.5	\
$I_{L\,max}\,[A]$	0.245	0.315	0.315

Table 4.4: Integrated prototype selected operating sequence. M_{min} and M_{max} are the minimum and maximum voltage conversion ratio for a given operating mode. $I_{L\,max}$ is the maximum theoretical average inductor current for a given operating mode and a 70mA load current.

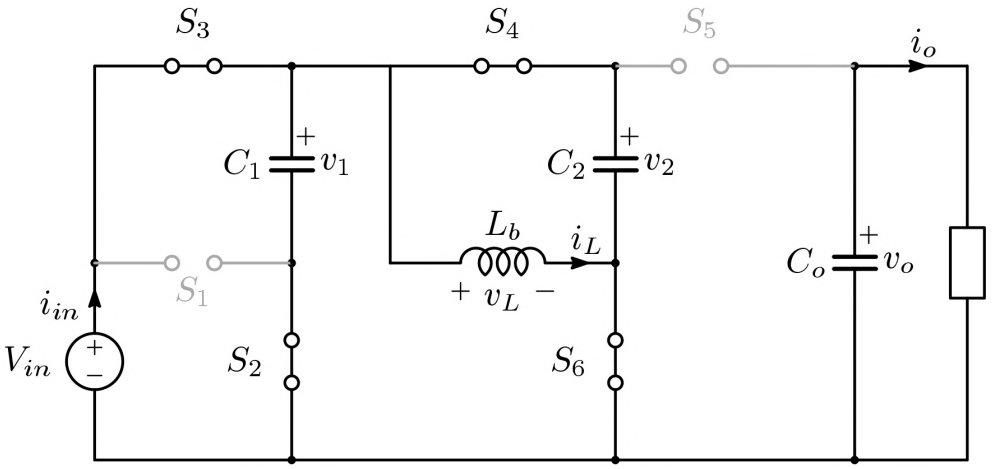


Figure 4.5.2: CHP4 Mode ON-Phase equivalent circuit in the simplified prototype implementation.

Mode CHP4 is instead implemented in a slightly different way than previously shown in subsection 4.4.1.5. In fact, as it is possible to see observing CHP4 mode equivalent circuits during the ON and OFF phases (fig.4.5.2 and 4.5.3 respectively), in the simplified implementation only C_2 cell is switched in CHP4 mode, while C_1 is always kept in parallel with the input source.

Observing the ON-Phase equivalent circuit it is possible to notice that in this phase both the capacitors C_1 and C_2 are in parallel with the input source, thus charging to V_{in}. At the same time the inductor is also being charged with $v_L = V_{in}$. During the OFF-Phase instead, the inductor and C_2 are connected in series with the input source and energy is delivered to the output. In this case $v_L = 2V_{in} - v_o$. Knowing v_L in both operating phases and under steady-state operation hypothesis, the conversion ratio can be estimated as

$$M = \frac{V_o}{V_{in}} = \frac{2 - D}{1 - D}$$

The expression of the conversion ratio as a function of the duty cycle remains unchanged if compared to the buck-boost capable topology.

Exploiting the steady state operation hypothesis, under which average capacitor currents are equal to zero, it is possible to write

$$I_L = I_{S_3} - I_{S_4}$$

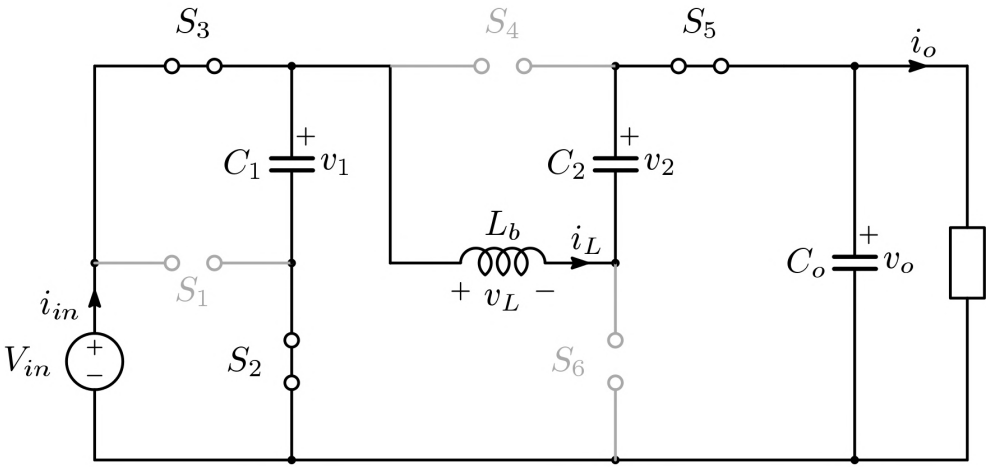


Figure 4.5.3: CHP4 Mode OFF-Phase equivalent circuit in the simplified prototype implementation.

Knowing that steady-state operation hypothesis allows to write $I_{S_4} = I_{S_5} = I_o$ and $I_{S_3} = I_{in}$ the previous equation becomes

$$I_L = I_{in} - I_o$$

Under unitary efficiency hypothesis it is then possible to write

$$I_L = (M-1)\, I_o$$

where M is the voltage conversion ratio. Once again CHP4 characteristics are unchanged with respect to the complete topology.

Finally, observing Fig.4.5.2, it is possible to estimate the inductor current ripple as

$$\Delta i_{L\,CHP4} = \frac{V_{in}}{L f_s} D$$

Knowing the conversion ratio as a function of the duty cycle it is possible to derive the inverse function, obtaining the duty cycle as a function of the conversion ratio:

$$D = \frac{M-2}{M-1}$$

.

Substituting this result in the inductor current ripple expression it is possible to obtain

$$\Delta i_{L\,CHP4} = \frac{V_{in}}{L f_s}\left(\frac{M-2}{M-1}\right)$$

once again equal to the complete buck-boost capable topology case.

4.5.2 IC Prototype Design

Fig.4.5.4 shows the actual topology implementation. Switches S_1, S_3, S_4 and S_5 were implemented using P-MOSes and this was done to reduce the IC pin count in S_1 case (eliminating the need for a bootstrap capacitor pin), and to simplify the drivers design in the floating switches case. The switches S_2 and S_6, that are referred to ground, were instead implemented using NMOS devices. The maximum switches voltage stress in this simplified prototype is V_{in} in S_1, S_2 and S_3 case, while it is $v_o\left(1-\frac{1}{M_{max}}\right)$, where M_{max} is the highest between the maximum conversion ratios implemented by CHP2 and CHP4, for S_4, S_5 and S_6. Since the employed 130nm BCD technology offers 20, 40 and 60V devices, the input voltage varies in between 6 and 18V and the maximum output voltage is equal to 60V, the input devices (S_1,S_2 and S_3) were implemented using 20V MOSfets, while the output ones (S_4,S_5 and S_6) were implemented with 60V devices. It must be noticed that the higher input voltage values correspond to lower conversion ratios; it is then straightforward to understand that CHP4 mode will be used to handle those input voltage values. Since the first cell is not switching in this operating mode, no voltage spike-related reliability problems exist in using 20V devices. However, that would be not true if modes CHP2 and CHP1 would be used in the same conditions. In that case, the input switches S_1,S_2 and S_3 should be implemented using 40V devices.

The area budget for the power stage switches was chosen to be approximately 2.5mm^2, as a result of both layout and performance considerations; the switches were then sized making the hypothesis of dominating conduction losses to allow for output current maximization. To do so, after estimating the switches RMS currents under the hypothesis of FSL operation, the total conduction losses as a function of the switches areas in CHP1 mode at the

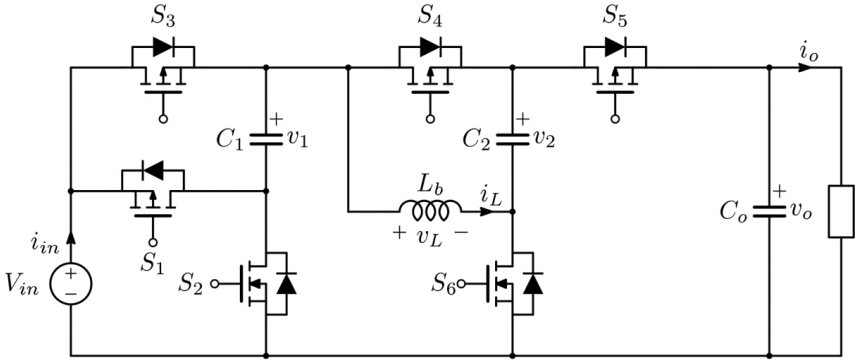


Figure 4.5.4: Simplified reconfigurable prototype implementation.

maximum requested conversion ratio were estimated. The Lagrange multipliers method was then employed to estimate the switches areas that, given the aforementioned total area budget, optimize the conduction losses. The resulting switches areas are shown in table 4.5. To better accommodate the different components at the layout level, most of the switches were implemented using multiple devices in parallel; as it is possible to see in fact, S_1, S_2, S_5 and S_6 were implemented with two devices in parallel, while S_3 was implemented using three devices in parallel. The aforementioned operating point was chosen as the converter optimization point because it is the one corresponding to the highest output power; furthermore, it also corresponds to the highest duty cycle employed by any of the operating modes, subsequently corresponding also to the lowest conduction times for some of the switches, potentially yielding the highest conduction losses.

After sizing the MOSfets, the converter 1.8MHz operation in correspondence of each operating mode maximum and minimum duty-cycle values was simulated using $PLECS^{®}$ for values of the flying capacitors varying in the range from the tens of nano to the tens of micro Farads; the converter efficiency was estimated for every capacitance value. By doing this, the flying capacitance values guaranteeing FSL operation were identified, resulting in $C_1 = C_2 = 10\mu F$ (some margin to account for components tolerance was considered). In fact, the aforementioned $PLECS^{®}$ simulation considered only conduction losses, since the switches models include only the $R_{ds\,ON}$; as a consequence, the simulated efficiency peak corresponds to the fast-switching limit operation.

Switch	Number of Devices in Parallel	Area [mm^2]	Estimated R_{ON} at 25°C [Ω]
S_1	2	0.5327	0.138
S_2	2	0.4873	0.037
S_3	3	0.5998	0.112
S_4	1	0.2043	1.807
S_5	2	0.3825	0.874
S_6	2	0.3793	0.131

Table 4.5: IC prototype power-stage: switches area, implementation and nominal resistance.

After sizing the flying capacitors, a proper inductance value was chosen. Once again, to do so, CHP1 operation at 1.8MHz and maximum conversion ratio was considered. Also in this case a simulation-based design technique was employed, due to the limited time available to validate the IC design before the tape-out deadline and the wide range of possible operating conditions. In particular Cadence Virtuoso® simulation using the sized power MOSfets models but ideal passives and driving was performed at different possible inductance values and the corresponding efficiency was estimated. The inductance value optimizing the converter efficiency was then chosen, yielding $L = 3\mu H$. Since a commercially available inductor was used, the nominal inductance value was chosen to be $3.3\mu H$. The design was carried out following the principle of block reuse, both to speed-up the process in the presence of strict deadlines and to avoid possible reliability problems. The IC block diagram can be seen in Fig.4.5.5. The designed blocks include a pMOS driver, an nMOS driver, a half-bridge driver and a mode selection logic.

The block called "mode selection logic" allows the selection of the converter operating mode through two state bits, generated outside the IC. The block basic cell can be observed in Fig.4.5.6. As it is possible to see, a cascade of multiplexers selects the proper driving signal to be fed to the specific MOS driver. Each of the four inputs of the two multiplexers controlled by bit b_0 is in fact connected either to the PWM signal corresponding to the converter ON-Phase, to its complementary signal (with dead-time), to the high logic level or to ground, depending on which is the proper driving signal in the given operating mode. Each couple of control bits b_0 and b_1 values identifies

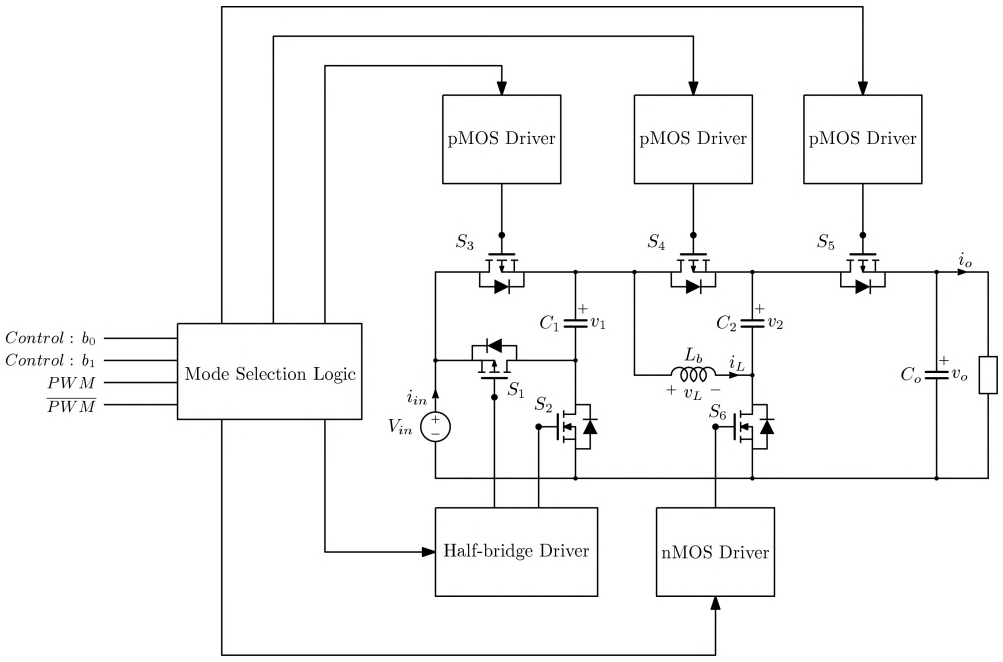


Figure 4.5.5: IC prototype schematic.

a specific operating mode.

Table 4.6 shows the correspondence between the control bits and the different operating modes; having two control bits yields four different possible configurations: three are used for the converter hybrid modes and one for an extra operating mode in which S_3, S_4 and S_5 are constantly OFF, while S_1 and S_2 are driven by PWM and its complementary signal respectively. Three multiplexers are needed for every MOS, thus the mode selection logic block is implemented using eighteen total multiplexers.

	b_1	b_0
CHP1	1	1
CHP2	1	0
CHP4	0	1
EXTRA MODE	0	0

Table 4.6: Mode selection logic: configuration bits and operating modes.

It must be noted that the PWM signal for the driving of the switches and its complementary with a dead-time are generated outside the IC. This choice was made to allow more freedom in terms of maximum/minimum dead-time and operating frequency selection.

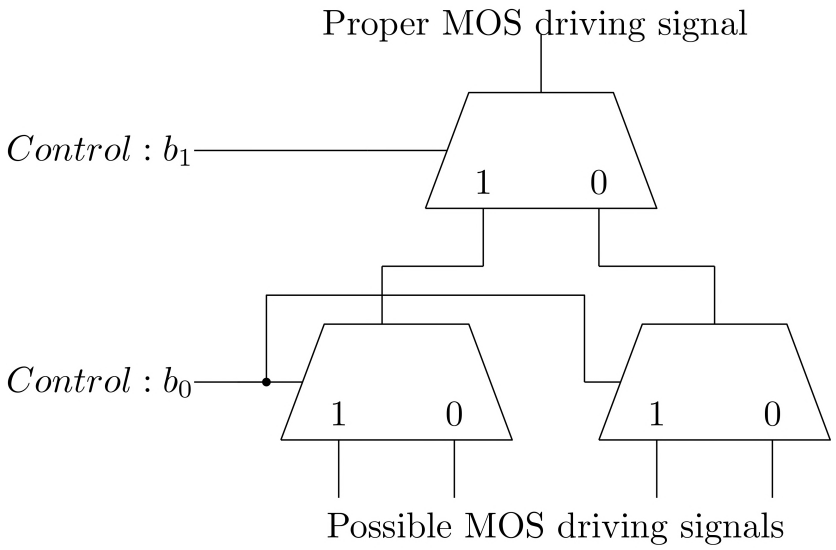


Figure 4.5.6: Operating mode selection logic basic cell.

The pMOS driver general structure is shown in Fig.4.5.7. As it is possible to see this block is constituted of a voltage regulator, a MOS gate-driving stage and a level shifter to shift the driving signal fed by the mode selection logic to the proper level. The level shifter schematic is shown in Fig.4.5.8. To understand how this block works, the circuit behaviour in the case of transition of the *Input* signal from low to high is explained. When the *Input* signal is low, M_1 is OFF, while $\overline{v_{out}}$ is high ($\overline{v_{out}} = V_{source}$) and v_{out} is low ($v_{out} = V_{SSH}$). The voltages $\overline{v_{out}}$ and v_{out} are fixed by the two inverters $logic1$ and $logic2$ that act as a data storing unit. Analysing the level-shifter right branch, it is possible to see that, since v_{out} is low and equal to V_{SSH} M6 is OFF. As a consequence, being $\overline{Input}$ high, M2 is ON with no current flowing on it and its v_{ds} is zero and that causes M4 to be also ON with v_{ds} equal to zero. Therefore, M6 v_{ds} is equal to V_{SSH}, showing the reason why this device must be a high voltage one. Analysing the left branch instead, it is possible to notice that, since $\overline{v_{out}}$ is high and equal to V_{source}, the PMOS M5 is ON (it must be remembered that $V_{SSH} \approx V_{source} - 2.5$, while M1 is OFF, causing M3 to be OFF as well. In this case, it is important to notice that M3 gate is fixed at 2.5V; this is meant to limit M1 drain voltage maximum value to $2.5 - V_{th\,M3}$, causing M3 (that is a high-voltage device) to withstand most of

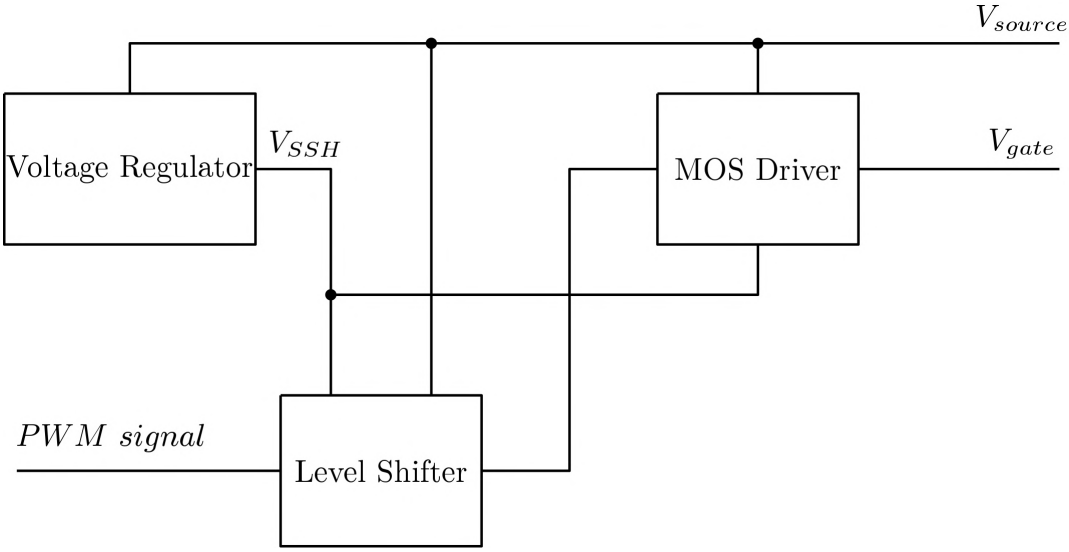


Figure 4.5.7: PMOS driver simplified structure.

the voltage stress, that since M5 is ON with no current flowing on it is equal to V_{source}, protecting in such a way the low-voltage device M1.

When the *Input* signal rises, M_2 turns OFF, while M_1 turns ON and $\overline{v_{out}}$ starts to decrease. At first, during this transition phase, $\overline{v_{out}}$ is also connected to V_{source} through *Logic*2, so that its decrease is slow; it is only when $\overline{v_{out}}$ drops below *Logic*1 low-voltage threshold that v_{out} can complete its transition from the high to the low voltage level. At that moment in fact, *Logic*1 output, that is also *Logic*2 input, becomes high and $\overline{v_{out}}$ transition can complete, yielding $\overline{v_{out}} = V_{SSH}$. Since the circuit is symmetric, it is straightforward to understand that the block behaviour is the same when the *Input* signal changes from high to low. In this case what has been just said can be applied to the circuit right branch. It must be noticed that M_1 and M_2 are low voltage MOSFETs, while M_3 and M_4 are high-voltage ones.

The voltage regulator schematic is shown in Fig.4.5.9. A current reference is fed to the block and used to generate the proper voltage rail for the MOS gate-driving block. It is important to notice that, due to M8 device structure, a capacitance in between ground and V_{SSH} is introduced. This is important because, in some of the pMOS cases, the source voltage of the device is moving fast, due to the inductor current free-wheeling and the switched-capacitor cells behaviour. This capacitance to ground could slow V_{SSH} movement when

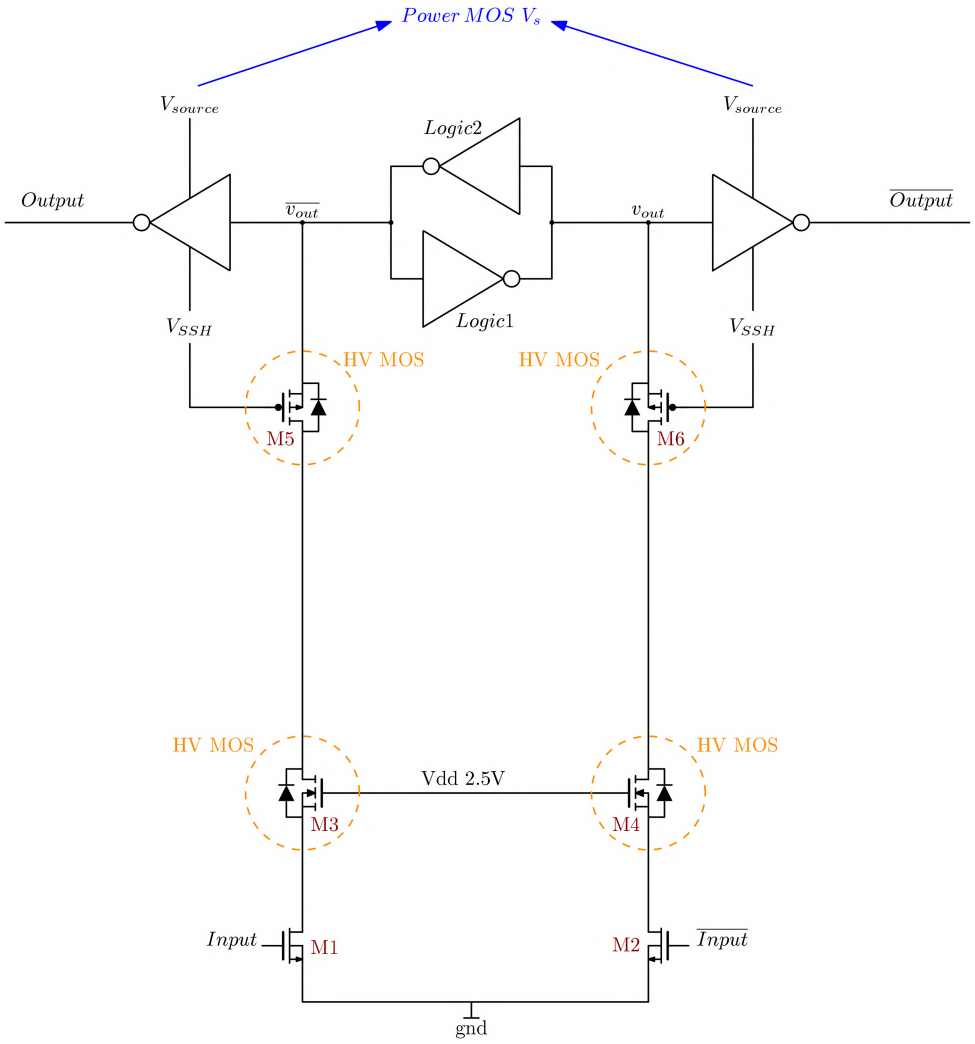


Figure 4.5.8: PMOS driver level shifter schematic. The signal marked as *input* can be PWM or its complementary signal, depending on the specific MOS driven and on the operating mode selected.

the MOS source voltage is changing rapidly, giving rise to reliability problems and unwanted effects.

To avoid this problem, in the case of S_3 and S_4 a slightly modified schematic is used. As shown in Fig.4.5.10, M8 is no longer connected to ground; "V_{ref}" is in fact connected to the negative plate of the capacitor whose positive plate is connected to the pMOS source. This solution is shown in Fig.4.5.11.

The aforementioned figure also allows to understand the function of the left part of the circuit (the current mirror implemented by transistors M3, M5 and M7). As can be noticed in the schematic, transistors M4 is a high-voltage device and as a consequence, as previously mentioned in M8 case, it introduces a capacitance to ground. Due to this, when V_{source} increases rapidly, the voltage gradient generates a current i_{C4} that charges the aforementioned capacitance. If the left side mirror (M3, M5 and M7) did not exist, this charging current i_{C4} would make i_y higher than the intended value i_x (we would in fact have $i_y = i_x + I_{C4}$), causing an increase in the generated rail too. To understand how the current-balancing circuit in the left works, it must be notice that M3 is a high voltage device too, and as such it introduces a parasitic capacitance towards ground too. As a consequence, also in this case, a rapid increase in V_{source} will cause the generation of a charge current i_{C3}. It is now important to notice that, since M3 is sized as M4, their capacitances towards ground will be approximately equal, yielding $i_{C3} \approx i_{C4}$. By using the current mirror M5-M7 then, i_{C3} is mirrored into i_C that, also being approximately equal to i_{C4} balances its contribution, yielding $i_x \approx i_y$. As a consequence, the generated voltage rail V_{rail} is approximately constant.

Fig.4.5.12 shows the gate-driving circuit schematic. The level-shifted PWM signal (together with its complementary) drives the two inverter chains, whose higher and lower supply voltages are the MOS source voltage and V_{SSH}, that is generated by the voltage regulator previously shown. To better understand how this block works, the equivalent circuit during the MOS turn-ON phase is shown. Initially (Fig.4.5.13) the power pMOS gate capacitance is discharged to ground. When V_{gate} has become approximately equal to $V_{SSH} - V_{th}$, M_3 turns OFF, and the power device turn-ON is completed by the floating inverters chain through M_4 (Fig.4.5.14). This structure is used to sink most of the current to ground instead of the voltage regulator. This is meant to avoid rail fluctuations (the regulator is open-loop) and improve the driver performance by decreasing the MOS turn-ON time.

The nMOS driver schematic is shown in Fig.4.5.15. As it is possible to

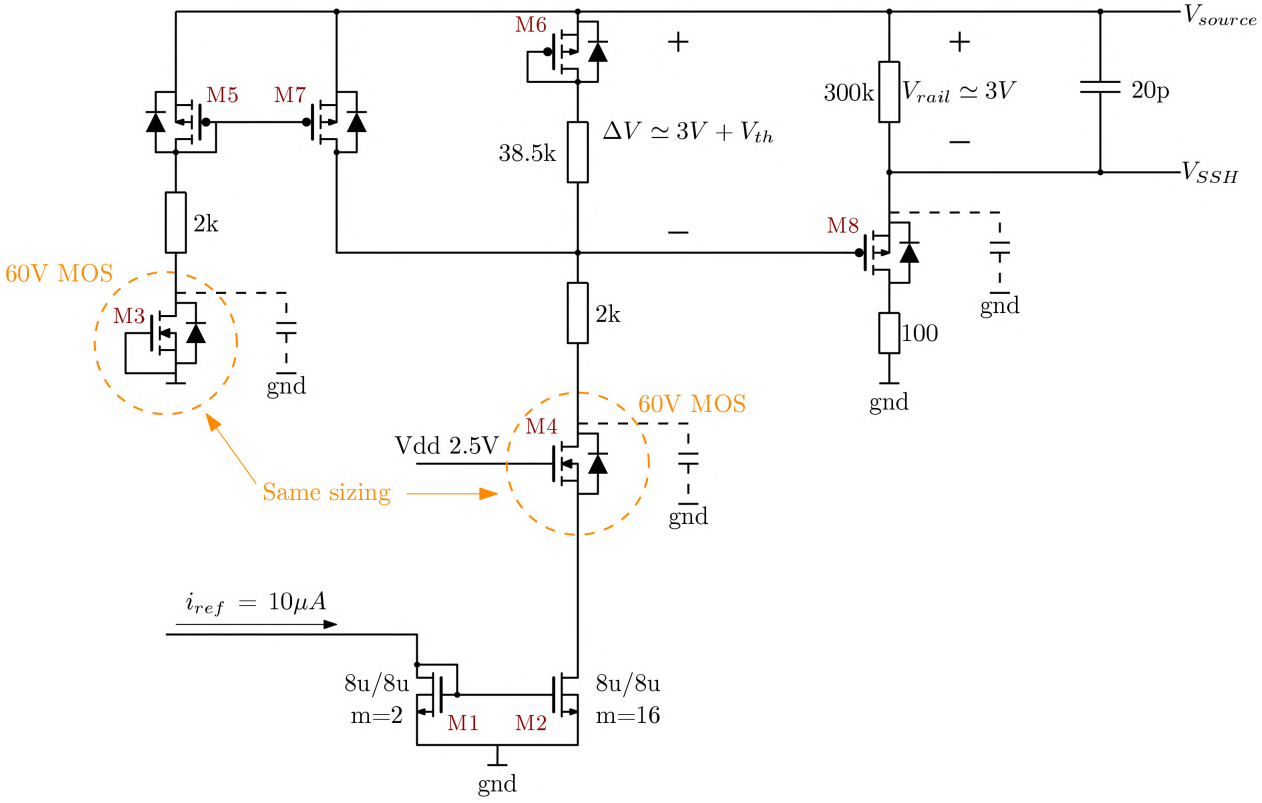


Figure 4.5.9: PMOS driver: standard voltage regulator structure.

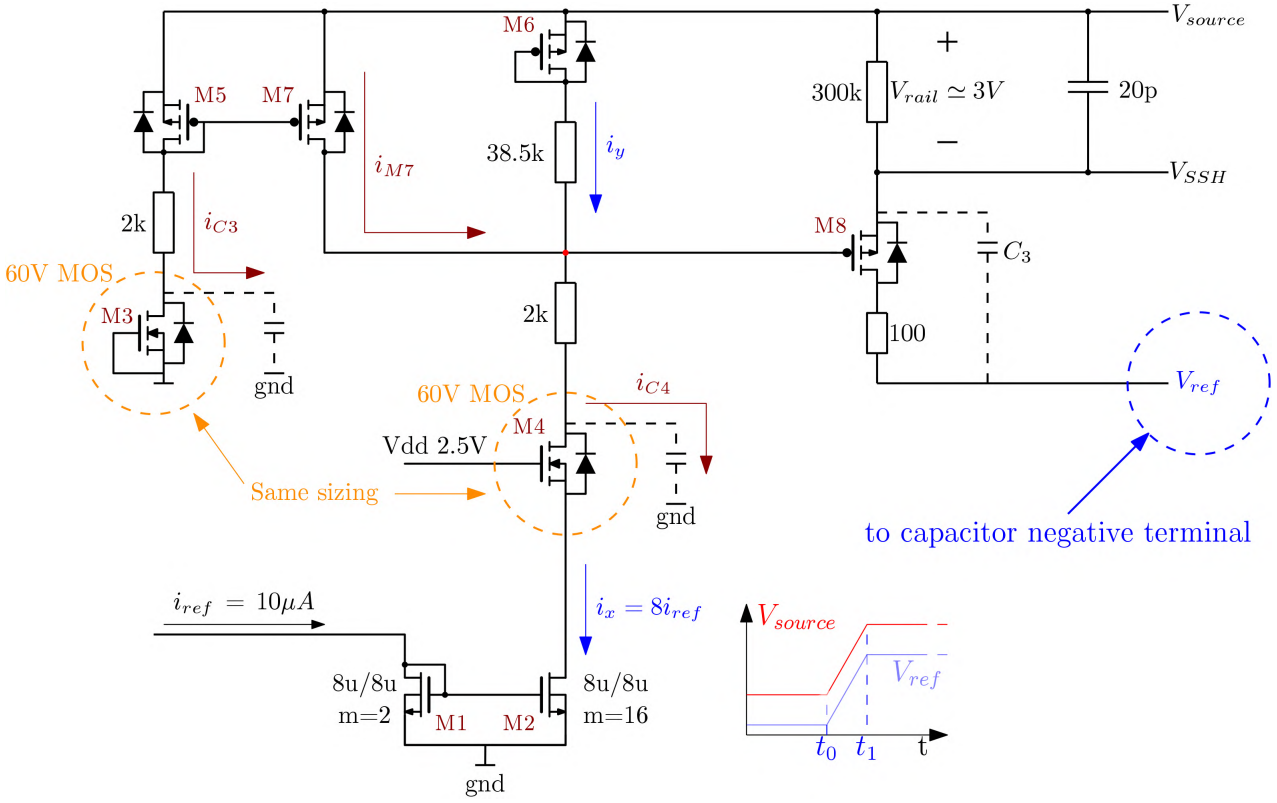


Figure 4.5.10: PMOS driver: "floating reference" voltage regulator structure.

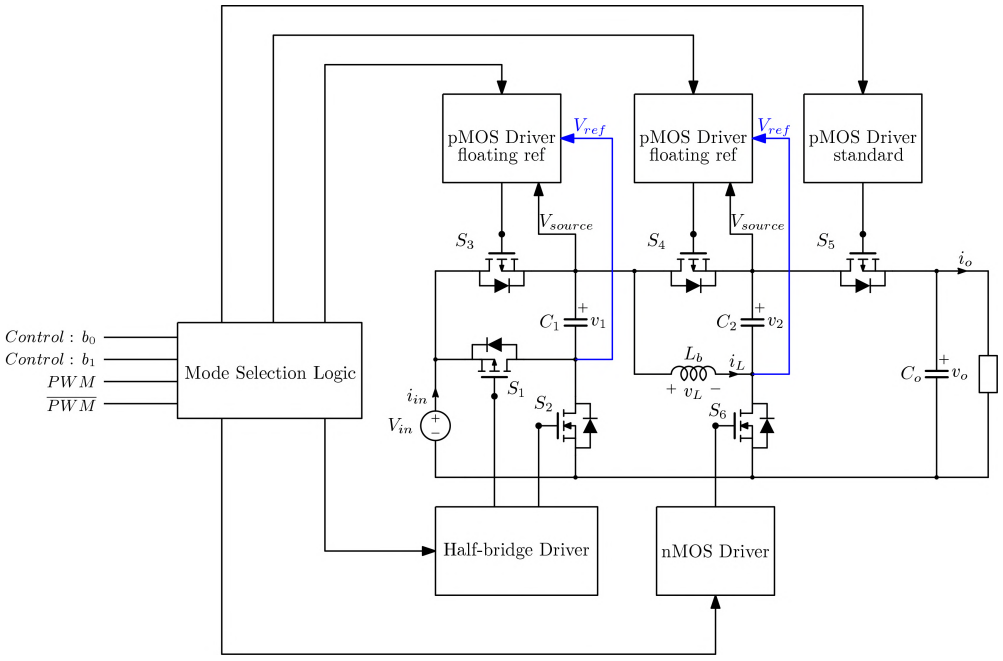


Figure 4.5.11: Integrated prototype schematic with modified pMOS driver reference for S_3 and S_4.

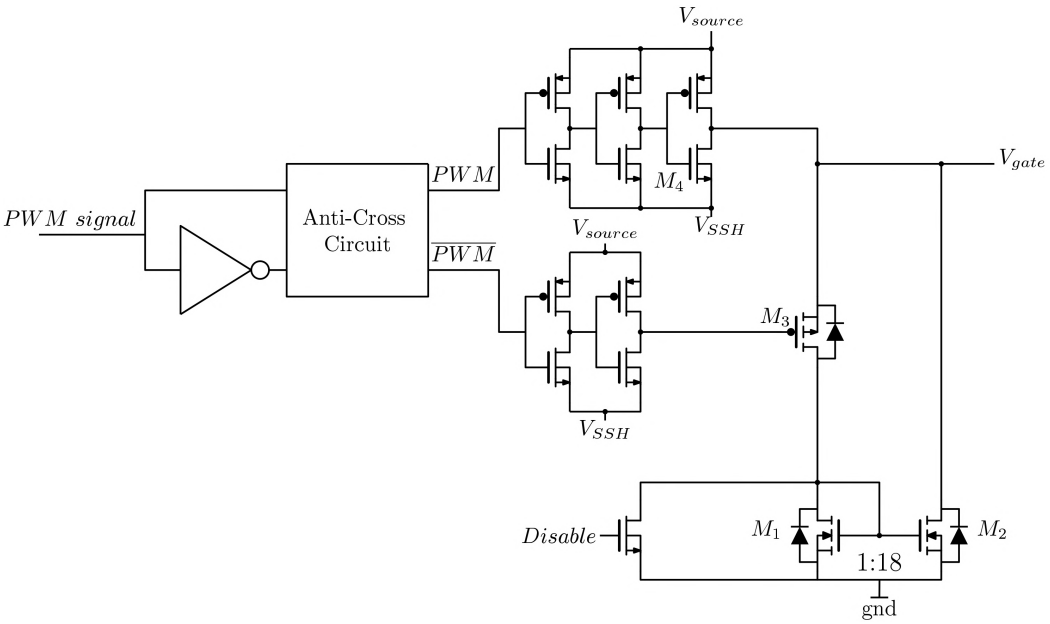


Figure 4.5.12: PMOS driver gate driving circuit schematic.

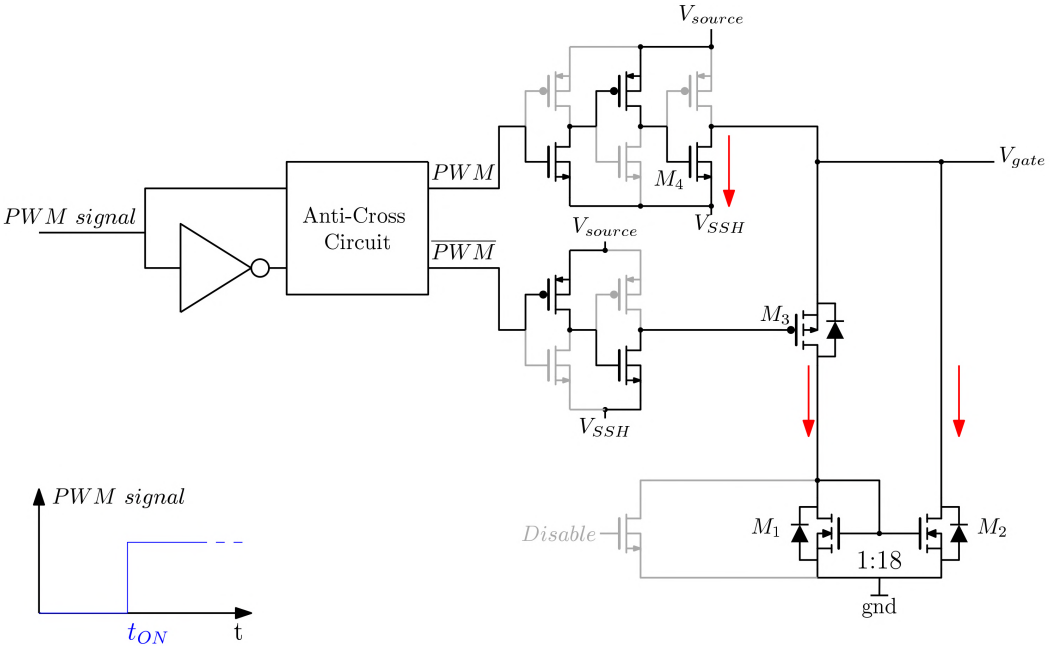


Figure 4.5.13: PMOS driver gate driving circuit: equivalent circuit during the initial stage of the MOS turn-ON phase.

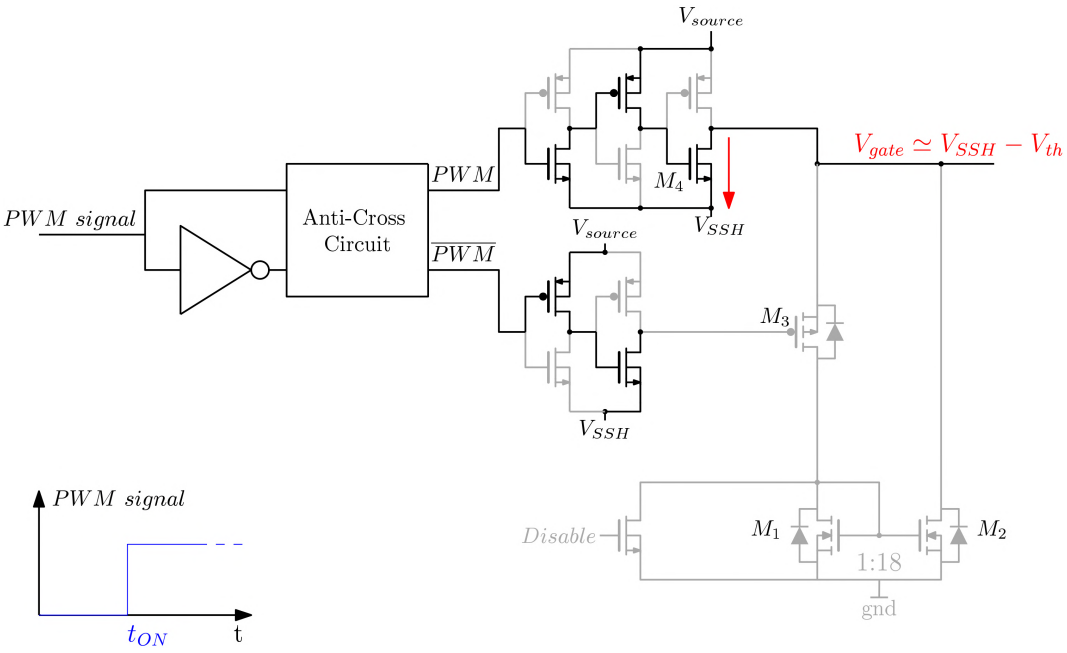


Figure 4.5.14: PMOS driver gate driving circuit: equivalent circuit during the final stage of the MOS turn-ON phase.

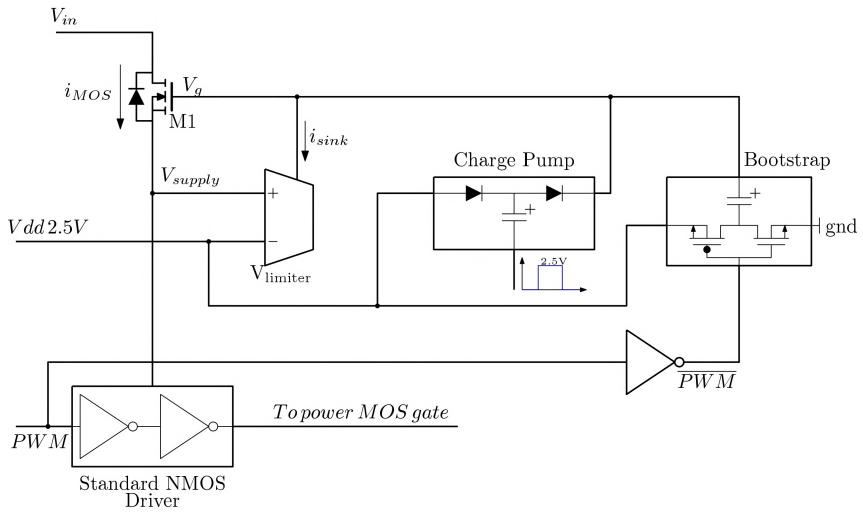


Figure 4.5.15: NMOS driver generic structure.

see, this block is characterized by using a linear voltage regulator to generate the 2.5V supply (V_{supply}) for the standard gate-driving inverters chain (here named "standard NMOS driver"). A single stage diode-capacitor charge pump is employed to generate M_1 gate voltage (V_g) from the 2.5V source. Looking at the circuit, it is possible to notice that the voltage V_{supply} is equal to $V_g - V_{gs\,M1}$; when minimum current is drawn by the driver, we have then $V_{supply} \approx V_g - V_{th}$. When the power nMOS must be turned ON and the PWM signal gets high anyway, a bootstrap circuit boosting V_g is needed to compensate for the driver supply current-related increase in $V_{gs\,M1}$. It must be noticed in fact, that, since M_1 works in the saturation region, $i_{MOS} = k\left(\frac{W}{L}\right)(V_{gs\,M1} - V_{th})^2$; the voltage V_{supply} is therefore dependent on i_{MOS}. As a consequence, assuming a constant V_g, when i_{MOS} increases $V_{gs\,M1}$ must increase too. Without a boost in V_g, the supply voltage $V_{supply} = V_g - V_{gs\,M1}$ would decrease below the requested value. It must be noted that this is an open-loop system specifically designed for a fixed operating point. The only feedback-based voltage regulation is eventually performed by a voltage limiter that senses V_{supply}, compares it with the 2.5V supply and, if the former is higher than the latter, draws a 1μA current from V_g node to first limit the voltage increase and then decrease V_g, until V_{supply} reaches 2.5V.

Finally the half-bridge driver structure is shown in Fig.4.5.16. As it is possible

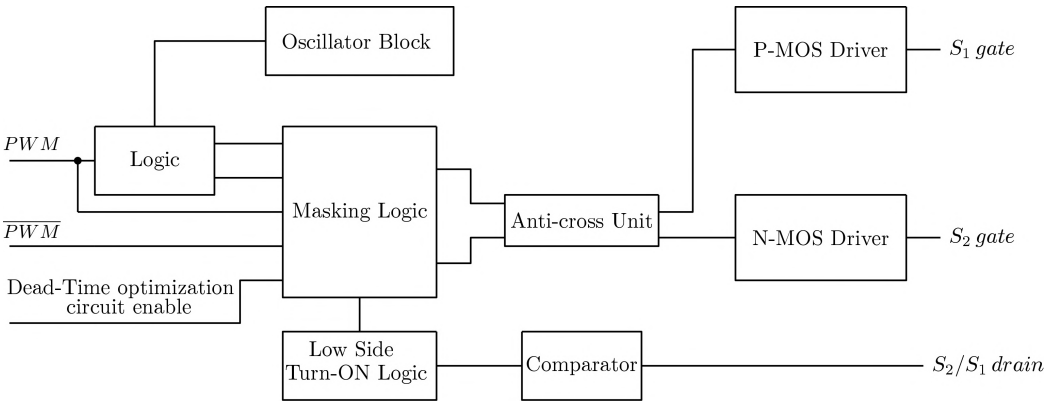


Figure 4.5.16: IC half-bridge driver simplified schematic.

to see, the half-bridge driver is made of two MOS drivers, an anti-cross unit to prevent cross-conduction in between the driving signals, an oscillator, three logic blocks and a comparator. The comparator, together with the block called "Low Side Turn-ON Logic", provides the half-bridge driver with a dead-time duration optimization capability. The comparator in fact senses S_2 drain voltage and sets the nMOS driver input PWM signal high when the MOS drain voltage has decreased enough. On the other side the "Low Side Turn-ON Logic" guarantees that S_2 driver input signal is set to its high value after a certain time, configurable from the outside, even if the drain voltage of S_2 is still high. This block (Fig.4.5.17) is important to guarantee the converter functionality even in possible unforeseen operation scenarios.

The masking logic allows to enable or disable the dead-time optimization feature setting the enable signal to the proper value, while the "Logic" block handles some enable signals together with the S_2 driving signal generation in case the dead-time optimization feature is activated. The oscillator provides the clock needed for the nMOS driver charge pump and is used to generate some enable signals inside the logic blocks. The p and nMOS drivers are equal to the ones shown in the previous subsections.

4.5.3 Experimental Results

Two different PCB prototypes were built, one to evaluate the proposed converter performance at $f_{sw} = 1.8\,MHz$, the other to test the operation at $f_{sw} = 300\,kHz$. Both prototype characteristics are shown in Table 4.7. It

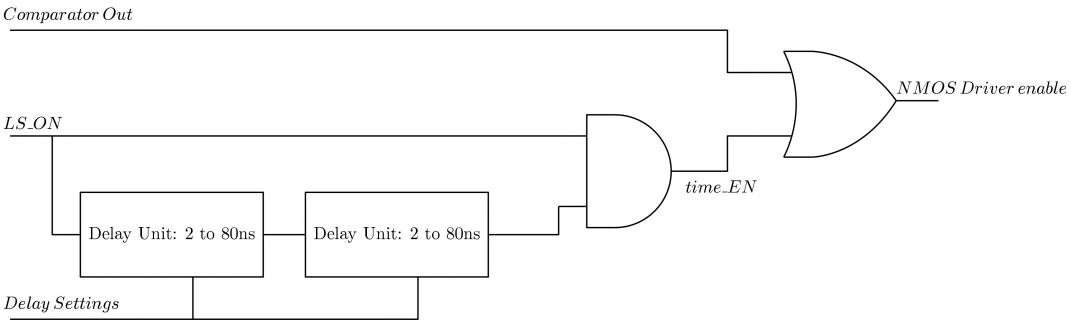


Figure 4.5.17: "Low Side Turn-ON Logic" block schematic. LS_ON is the complementary signal generated by the "Logic" block from the converter PWM driving signal. If the output of the comparator block does not become high after a given time, externally configurable in between 4 and 160ns, tim_EN forces the nMOS driver enable high, turning S_2 ON.

Operating frequency (f_{sw})	$300kHz$	$1.8MHz$
Nominal Load current (I_o)	$70mA$	$70mA$
Flying capacitance ($C_1 = C_2 = C_f$)	$60\mu F$	$10\mu F$
Inductance (L)	$18\mu H$	$3.3\mu H$

Table 4.7: IC test PCBs specifications: 1.8MHz and 300kHz case comparison.

should be noted that the products $f_{sw} \cdot C_f$ and $f_{sw} \cdot L$ are approximately equal (in the limit of the inductance and capacitance values available), this is meant to guarantee the same FSL operation and inductor current ripple, allowing a comparison of the converter performance at the higher and lower switching frequencies possible in an automotive environment. In both cases the traces thickness was chosen to be 70 µm.

Both PCBs are characterized by an on-board PWM driver that generates the converter PWM driving signal and a complementary one with dead-time adjustable using a potentiometer. Both the PWM driver and the IC references generation unit can be connected either to the converter input or to an extra auxiliary source, allowing to test the converter even in the case of extremely low input voltages. In case of need, the 2.5 and 1.5V references can be supplied by external generators too.

The converter operating mode can be configured using two slide-switches, but can also be set by two eternal signals fed to the inputs of a couple of

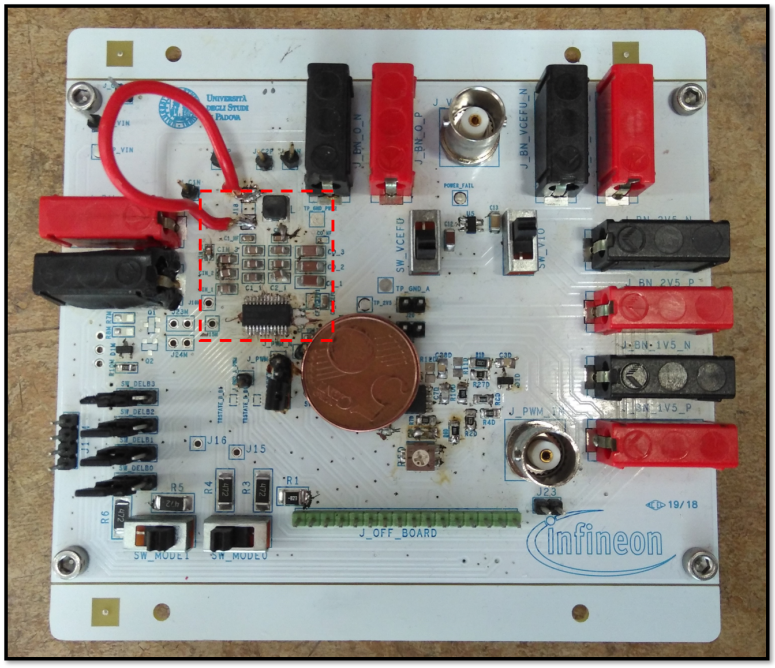


Figure 4.5.18: Picture of the 1.8MHz test board with a 5 Euro cents coin for dimensions comparison. The converter power stage is highlighted in red.

three-state buffers. The dead-time optimization block can be enabled or disabled via jumper configuration. When the half-bridge dead-time optimization block is enabled, four on-board jumpers allow to set the maximum dead-time duration. A temperature-sensing circuit is also present on the PCB and it works by forcing a current into two diodes integrated in the IC. A sixteen pins connector is inserted for potential connection to an external digital device, allowing PWM and operating mode selection signals off board generation, together with I/O buffers powering. A picture of the PCBs can be seen in Fig.4.5.18 and 4.5.19.

All three possible operating modes were characterized at $V_{in} = 6$ and $12V$. Since CHP4 mode is the one providing the lower conversion ratios, it was characterized also at $V_{in} = 18V$, while CHP2 and CHP4 were not.

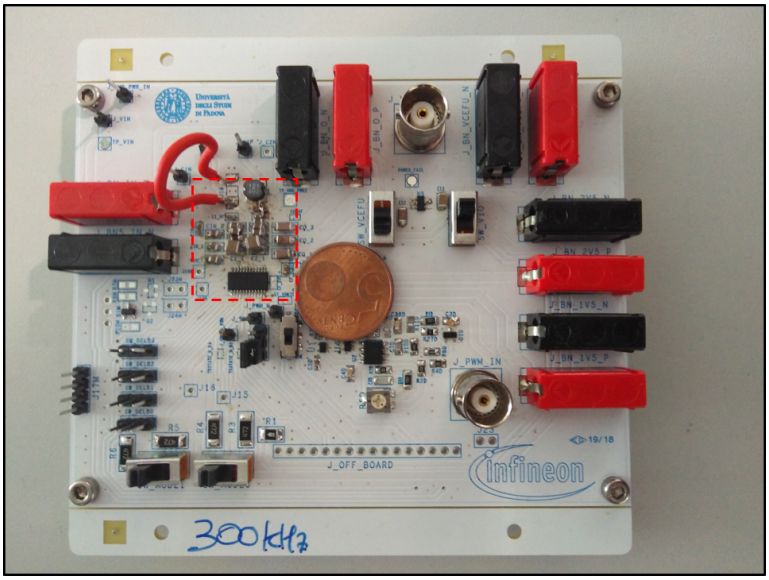


Figure 4.5.19: Picture of the 300kHz test board with a 5 Euro cents coin for dimensions comparison. The converter power stage is highlighted in red.

Experimental Results at 1.8MHz

Fig.4.5.20 shows the measured efficiency in the case of $V_{in} = 6V$ and load current equal to $70mA$. As it is possible to see, the converter operation at 1.8MHz does not yield the requested conversion ratios. As the conversion ratio increases in fact, the efficiency keeps dropping until a catastrophic decrease at higher conversion ratios occur, making the converter operation untenable.

Fig.4.5.21 shows instead the efficiency at the same switching frequency and load current but $V_{in} = 12V$. In this case, since the maximum requested conversion ratio is lower and equal to 5, the converter can yield all the requested conversion ratios. CHP4 is once again the operating mode with the highest efficiency.

The same measures were repeated with a current load equal to 100mA. The results obtained with V_{in}=6V are shown in Fig.4.5.22. As it is possible to notice, results are similar to the I_o=70mA case. Even here in fact, the converter performance is characterized by a sudden and catastrophic drop in efficiency at the higher conversion ratios. Anyway, it must be noticed that, in CHP2 and CHP1 case, at the lower conversion ratios, the increase in load

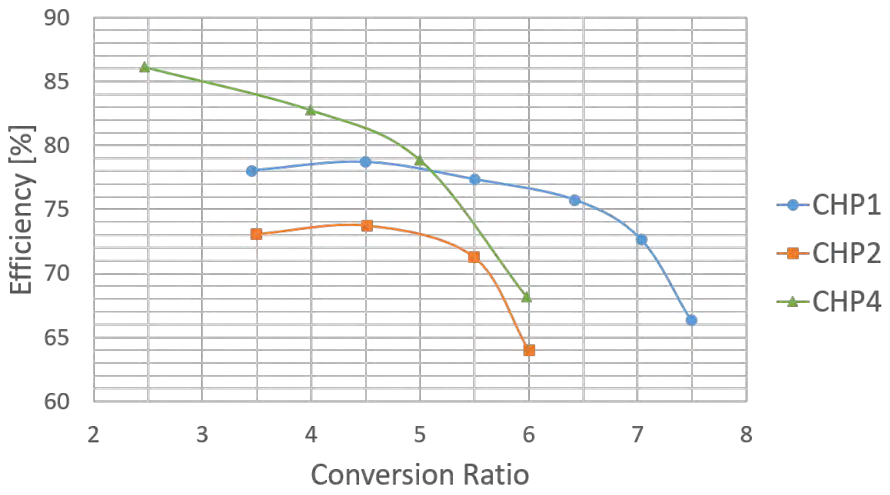


Figure 4.5.20: IC prototype efficiency at 1.8MHz with $V_{in} = 6V$ and $I_o = 70mA$.

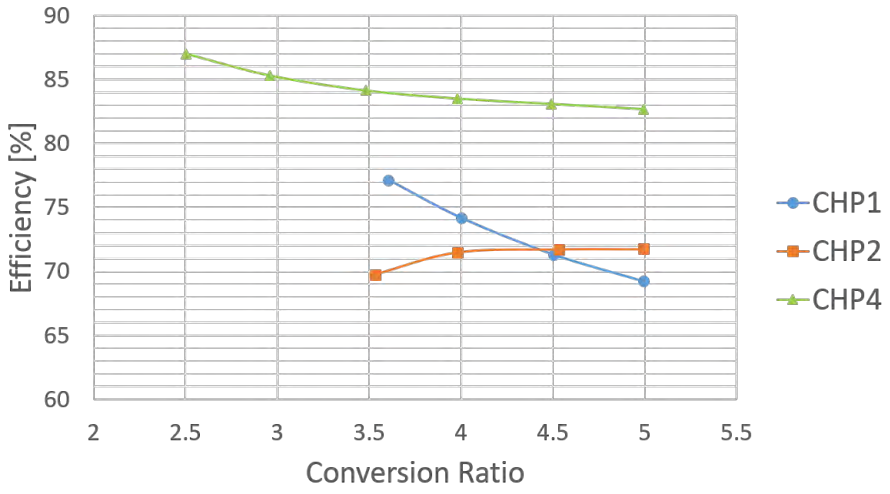


Figure 4.5.21: IC prototype efficiency at 1.8MHz with $V_{in} = 12V$ and $I_o = 70mA$.

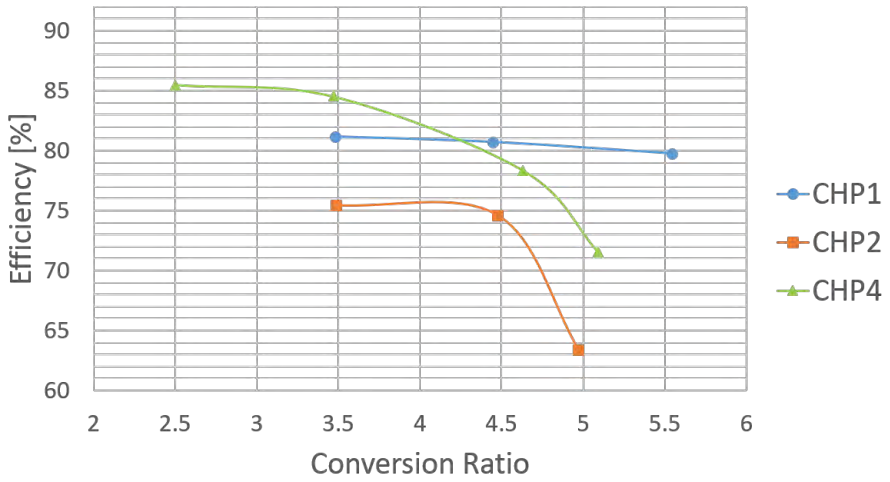


Figure 4.5.22: IC prototype efficiency at 1.8MHz switching frequency with $V_{in} = 6V$ and $I_o = 100mA$.

current produces an increase in efficiency too; this is probably due to the fact that the weight of conduction losses is increasing, pushing the converter operation closer to the conditions for which it was optimized. Anyway, it must also be noticed that in the 100mA load current case the efficiency drop occurs at lower conversion ratios if compared to the 70mA one.
Fig.4.5.23 shows instead the efficiency at 1.8MHz switching frequency, V_{in}=12V and I_o=100mA. Even in this case the efficiency is generally improved if compared to the I_o=70mA case.

Finally, figure 4.5.24 shows CHP4 mode efficiency with $V_{in} = 18V$ for the two cases of I_o equal to 70 and 100mA. Once again the increase in output current has improved the converter efficiency.

Experimental Results at 300kHz

Fig.4.5.25 shows the measured efficiency at $V_{in} = 12V$ and $I_o = 70mA$ for the three possible operating modes; once the conversion ratios were not limited at the ones shown in Table 4.4 to give a complete view of the different operating modes performances. It must be in fact be remembered that, as shown in table 4.4, CHP4 mode could be used up to a gain of 5.5 without

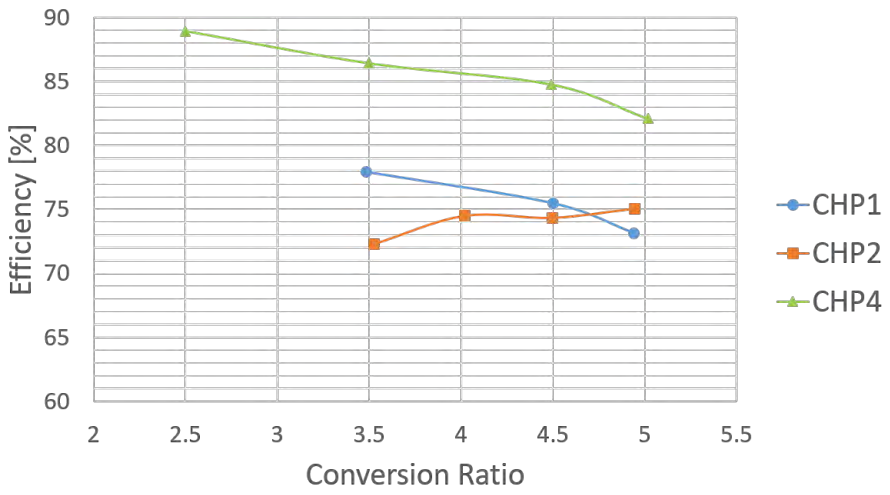


Figure 4.5.23: IC prototype efficiency at 1.8MHz switching frequency with $V_{in} = 12V$ and $I_o = 100mA$.

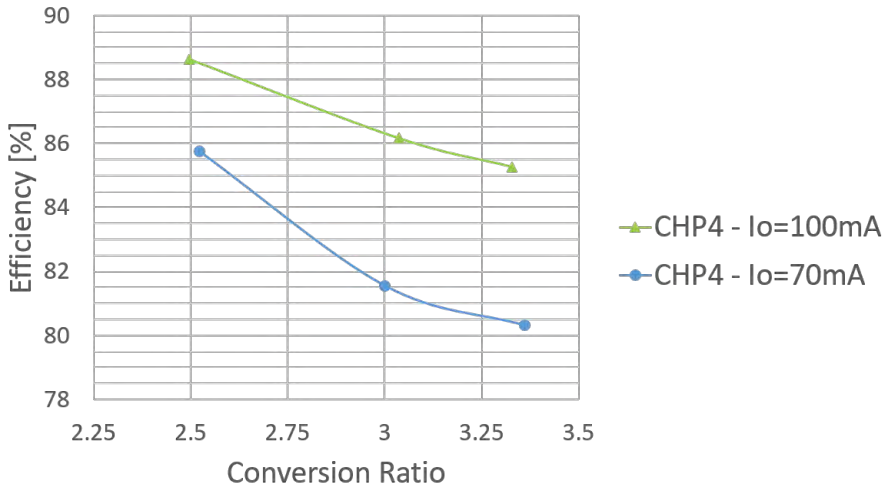


Figure 4.5.24: IC prototype efficiency at 1.8MHz with $V_{in} = 18V$: only CHP4 mode was characterized.

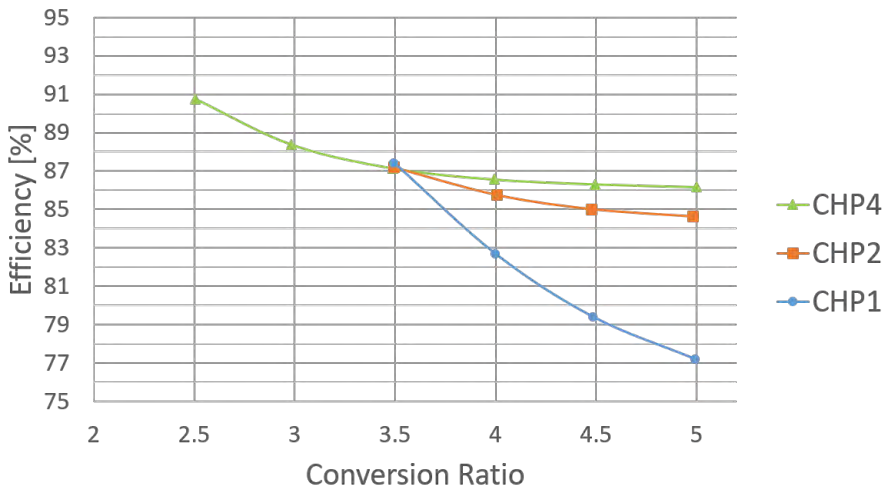


Figure 4.5.25: IC prototype efficiency at 300kHz with $V_{in} = 12V$ and $I_o = 70mA$.

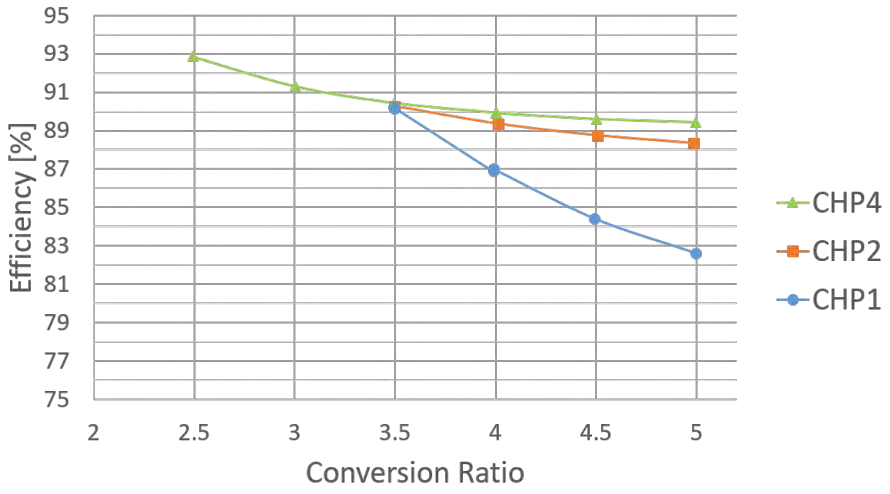


Figure 4.5.26: IC prototype efficiency at 300kHz with $V_{in} = 12V$ and $I_o = 100mA$.

any penalty in terms of theoretical maximum average inductor current.
Looking at Fig.4.5.25, it is possible to see the best efficiencies are obtained using mode CHP4; in fact, it must be remembered that in CHP4 mode only one of the switched-capacitor cells is being switched, as opposed to CHP1 and CHP2, in which both cells are switching. Peak efficiency is over 90%. CHP2 shows a little worse performance, while CHP1 is characterized by the lowest efficiency, with a minimum value of about 77% in correspondence of the maximum voltage conversion ratio, that in this case is equal to 5; it corresponds in fact to an output voltage equal to $60V$, that is the technology limit. If the output current is increased to 100mA, the efficiencies of Fig.4.5.26 are obtained. As it is possible to notice, the increase in the output current produces an increase in the efficiency too; the same considerations made in the 1.8MHz switching frequency case apply here. Peak efficiency is almost 93%. Fig.4.5.27 and 4.5.28 show the prototype efficiency at 300kHz with $V_{in} = 6V$ in the case of an output current equal to $70mA$ and $100mA$ respectively. Also in this case, CHP4 mode yields the highest efficiency, with a peak of about 92% in the $I_o = 100mA$ case. Lowest efficiency is about 77%, obtained in CHP1 mode at the maximum voltage conversion ratio, equal to 10. It is important to notice that, in contrast to what observed at 1.8MHz, in the 300kHz switching frequency case the converter not only is fully functional, but successfully yields all the requested conversion ratios.

Finally, figure 4.5.29 shows CHP4 mode efficiency with $V_{in} = 18V$ in the two cases of a load current equal to 70 and 100mA respectively.

In observing the previous efficiency result anyway, it is important to remember that this IC is a first-time design and its purpose was not to fully optimize the topology performance, but to demonstrate its feasibility in practice and provide knowledge on the criticalities and characteristics of hybrid converters implemented through integrated solutions. A redesign of the converter based on the results obtained by this work should yield improved performance. An example of this is given by the PWM generation circuit; in the implemented prototype in fact, the PWM generator allow to adjust the dead-time duration to optimize the performance, but the resulting dead-time is always symmetric. Considering Fig.4.5.30 as an example, observing $v_{C_{2n}}$ waveform, it is instead immediately clear how the resonant transitions taking place during the passage from the OFF to the ON phase of the converter takes much longer to complete if compared to the resonant transitions during the other dead-time phase. It is then straightforward to understand how the efficiency

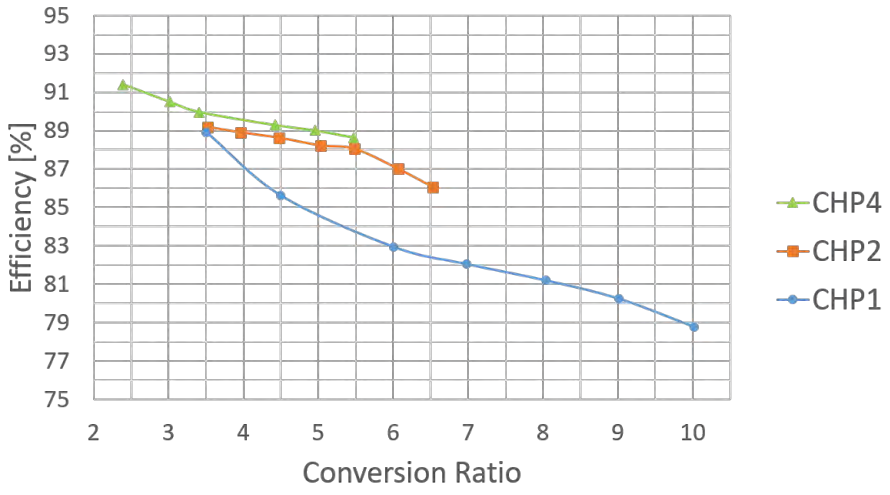


Figure 4.5.27: IC prototype efficiency at 300kHz with $V_{in} = 6V$ and $I_o = 70mA$.

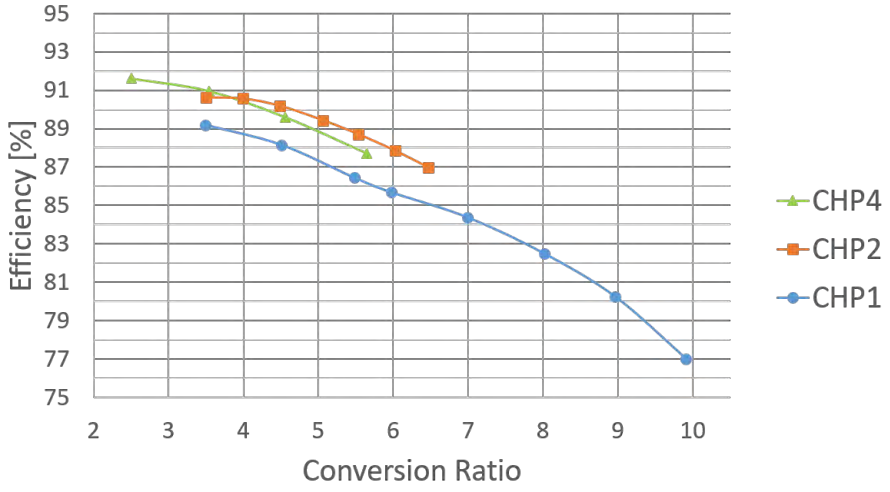


Figure 4.5.28: IC prototype efficiency at 300kHz with $V_{in} = 6V$ and $I_o = 100mA$.

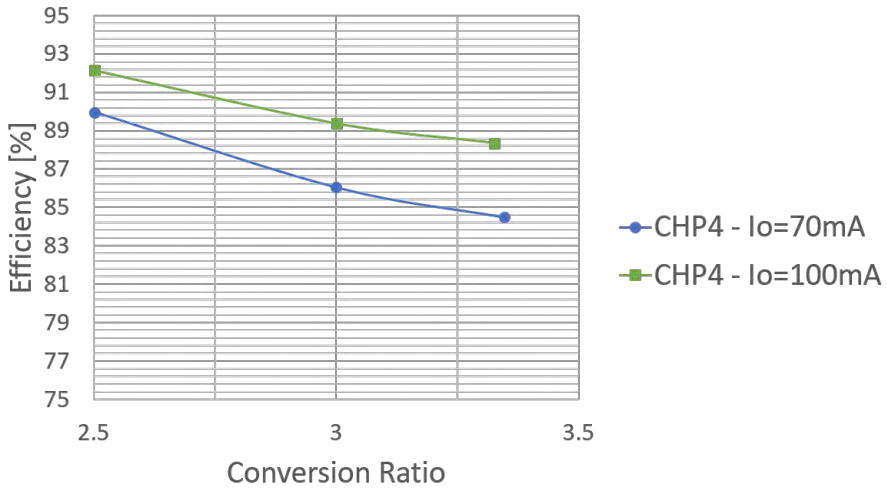


Figure 4.5.29: IC prototype efficiency at 300kHz with $V_{in} = 18V$: only CHP4 mode was characterized.

could be improved by using asymmetric dead-time durations. In the previous case in particular, the optimum converter operation in terms of efficiency would be reached reducing the duration of the dead-time corresponding to the transition from the converter ON to the OFF phase. It is also important to notice that, despite the corresponding data not being reported in the text, in some cases (especially in CHP1 mode at 300kHz) the inductor current ripple was much bigger than actually needed to obtain soft-switching, possibly yielding further margins for the converter efficiency improvement. A proper redesign should then take this into account too.

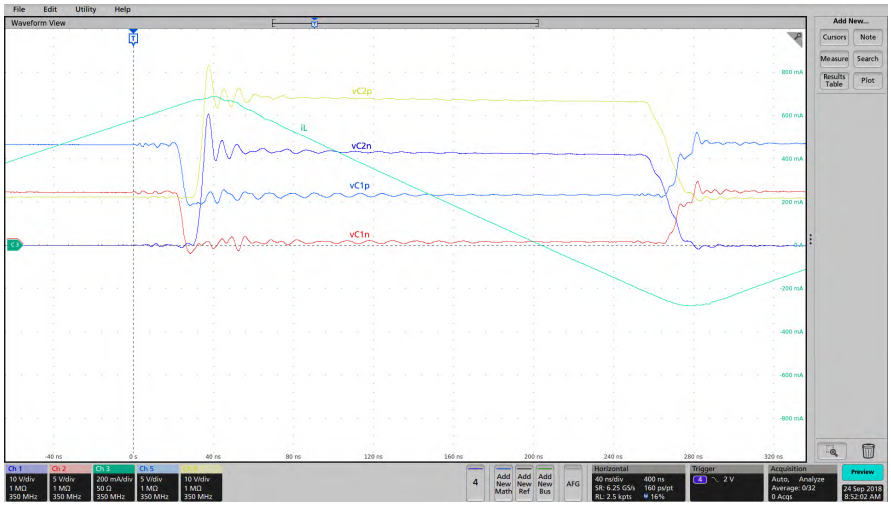


Figure 4.5.30: CHP1 Operating Mode: operation at $V_{in} = 6V$, $f_{sw} = 1.8\,MHz$, $I_o = 70\,mA$ and $v_o \approx 33V$. The waveforms $vC2p$ and $vC2n$ correspond to C_2 positive and negative plate voltage respectively. Waveforms $vC1p$ and $vC1n$ are instead C_1 positive and negative plate voltage. Waveform iL is the measured inductor current. Time scale is 40ns/div; vC1p and vC1n waveforms vertical scale is 5V/div, while vC2p and vC2n's is 10V/div; the inductor current waveform vertical scale is 200mA/div.

Experimental Efficiency Analysis

After reporting the experimental data regarding the prototype efficiency, it is interesting to compare them with the simulation results, to try to understand what are the main power loss causes. To do so, a comparison between the experimental and Cadence Virtuoso®-based simulation results, obtained considering the power-stage devices models, but ideal driving and passives, is carried out, starting from the case of a 1.8MHz switching frequency. Fig.4.5.31 shows the efficiency curves in CHP1 mode case: the light blue curve on top is the simulated converter efficiency as a function of the duty cycle, while the experimental data are reported in orange. As it is possible to see, a big difference between the simulation and experimental results exists, it is then interesting to perform and estimation of the different power loss causes to understand what is the main limitation to the converter performance. To do so, the driving losses must be estimated too, but due to the integrated-circuit nature of the prototype, a direct measure of the different power dissipation contributions is not possible (MOS drivers are integrated and not accessible from the outside). As a consequence, the driving losses estimation was performed simulating the complete driver circuits in the different operating points shown in Fig.4.5.31. The resulting losses were then added to the power dissipation data results obtained in the simulation with ideal drivers, yielding the efficiency curve shown in yellow in Fig.4.5.31. It is interesting to notice that, by adding the simulation-estimated driving losses, a drop of more than 10% in efficiency occurs.
However, a noticeable difference between the simulation predicted efficiency and the experimental results still exists. As a second step then, the estimation of inductor losses was also performed; it must in fact be remembered that quasi-square wave operation was chosen, yielding a high ripple to average ratio for i_L, possibly generating high losses in the magnetic core. To estimate the inductor dissipation, the employed magnetic device was mounted on the prototype PCB without any other component, and a DC current was imposed onto it. The resulting voltage drop was measured together with the inductor temperature at different DC current values, obtaining an approximated dissipated power-ΔT relationship. The estimated power-temperature relation allowed to approximately calculate the inductor losses in the different operating points by measuring the inductor temperature using a thermal camera while characterizing the converter efficiency. The obtained values were then added to the previously obtained results including power stage and

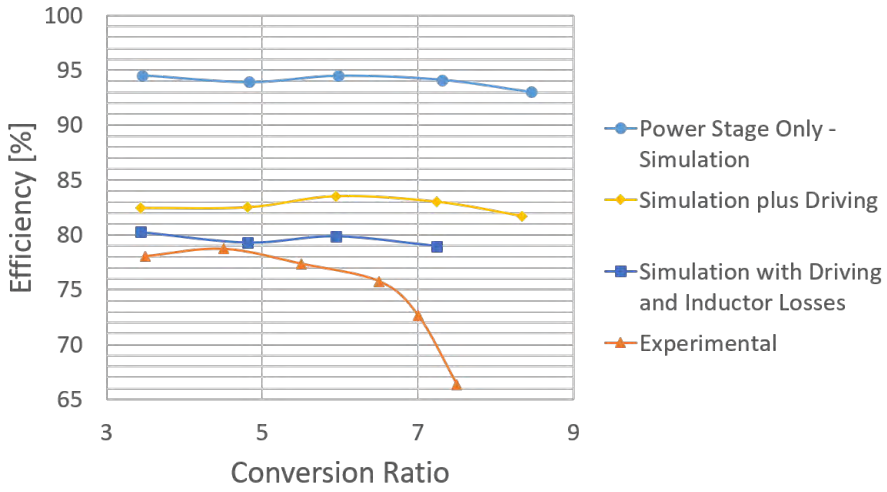


Figure 4.5.31: Converter CHP1 mode simulation and experimental efficiency comparison at $f_s = 1.8MHz$.

driving-related losses, yielding the dark blue efficiency curve in Fig.4.5.31. As it is possible to see, the simulated/calculated curve is now much closer to the experimental data at lower conversion ratios, but a significant difference still exists at higher ones. In that regard, it must be noticed that Cadence Virtuoso® simulation does not account for the devices heating; simulations are in fact performed at a fixed chosen temperature (in the graph case 27°C). Anyway, a number simulations performed at higher temperatures considering the converter power stage with an ideal driving do not show a big influence of temperature on the converter efficiency. As a consequence, a verified hypothesis for this drop in efficiency at higher conversion ratios could not be found.

If the same procedure is applied in CHP2 case, Fig.4.5.32 is obtained. Also in this case a huge difference between the experimental (in orange) and ideal driving simulation (light blue) data exist. Applying the same procedure followed in CHP1 case, and adding the estimated driving losses contributions to the ideal driving simulation, the yellow efficiency curve is obtained. In this case the driving losses contribute for about a 10% drop in efficiency. Adding also the estimated inductor losses yields the blue curve. These attained data still show some difference with the experimental ones, but its

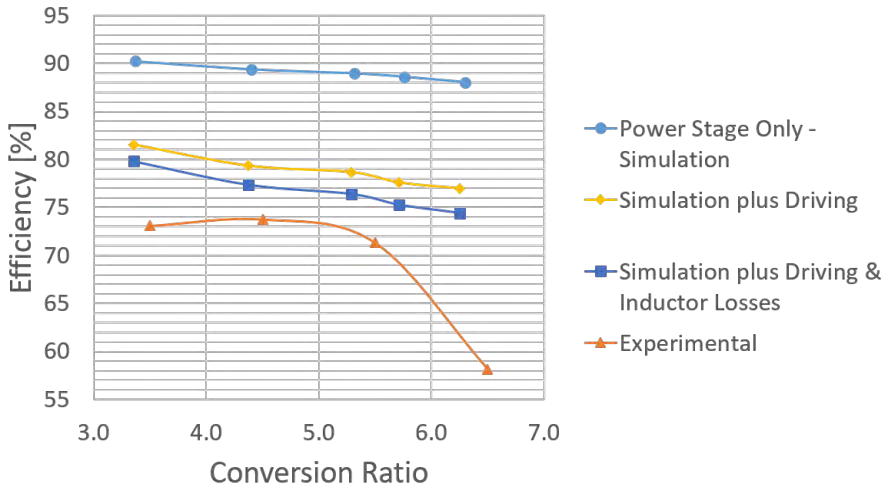


Figure 4.5.32: Converter CHP2 mode simulation and experimental efficiency comparison at $f_s = 1.8MHz$.

magnitude is much reduced at the lower conversion ratios. However, it must be noticed that once again a higher difference with the experimental data exists at higher conversion ratios.

Finally, considering CHP4 mode, Fig.4.5.33 is obtained. Also in this case, the power stage efficiency with ideal driving simulation is considered first (light blue) and compared with the experimental data (orange). Once again a consistent difference in between these two curves exists. Following the same procedure used in CHP1 and CHP2 case, the driving and inductor losses contributions can be added, obtaining the yellow and blue curves. At lower conversion ratios these two contributions seem to account for most of the difference in between simulation and experimental results, with driving losses in particular being the major contribution. Anyway, even if the magnitude of the phenomenon is lower, even in CHP4 case the difference between the blue curve and experimental data increases at higher conversion ratios.

The same comparisons and estimations can be made in the 300kHz switching frequency case. If CHP1 mode is considered, Fig-4.5.34 is obtained; once again the simulation data is reported in light blue, while the experimental data is in orange. Driving and inductor losses can be estimated following the

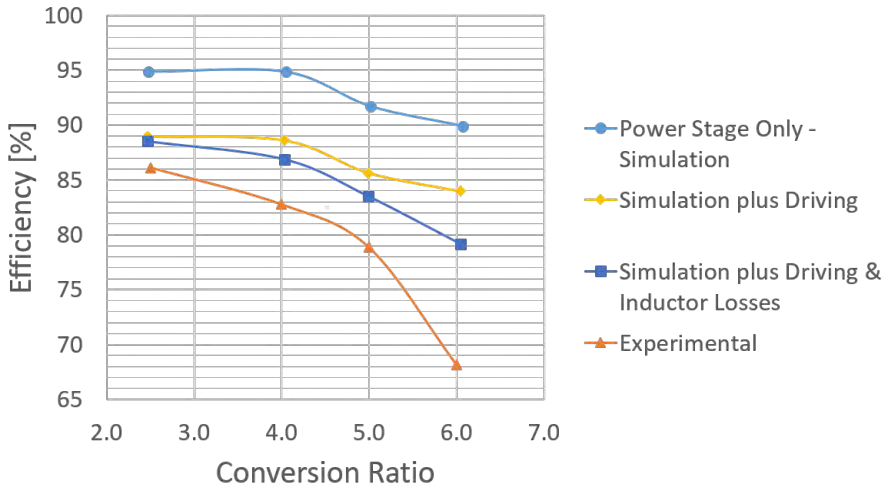


Figure 4.5.33: Converter CHP4 mode simulation and experimental efficiency comparison at $f_s = 1.8MHz$.

same procedure used in the 1.8MHz case and, adding these contributions to the power-stage only simulation data, the yellow (only driving losses added) and blue (driving plus inductor losses added) curves can be obtained. It is interesting to notice that, in this case, the magnetic element losses seem to have a higher impact than the driving ones. This makes sense considering the lower switching frequency, but it must also be noticed that the employed inductor belongs to a different product family if compared to the 1.8MHz case and this could be the cause of a worse performance in terms of power dissipation. It must also be noticed that, at the minimum conversion ratio, the simulated/calculated efficiency is lower than the experimental one, suggesting that one of the aforementioned contributions may have been overestimated.

If CHP2 is considered instead, Fig.4.5.34 is obtained. The same considerations made in CHP1 case apply here; in fact, as it is possible to see, the driving losses weight is greatly reduced if compared to the 1.8MHz case, while the inductor power dissipation causes most of the drop. The efficiency data estimated adding both inductor and driving losses to the ideal-driving power stage simulation results (the blue curve) are in this case very close to the experimental ones.

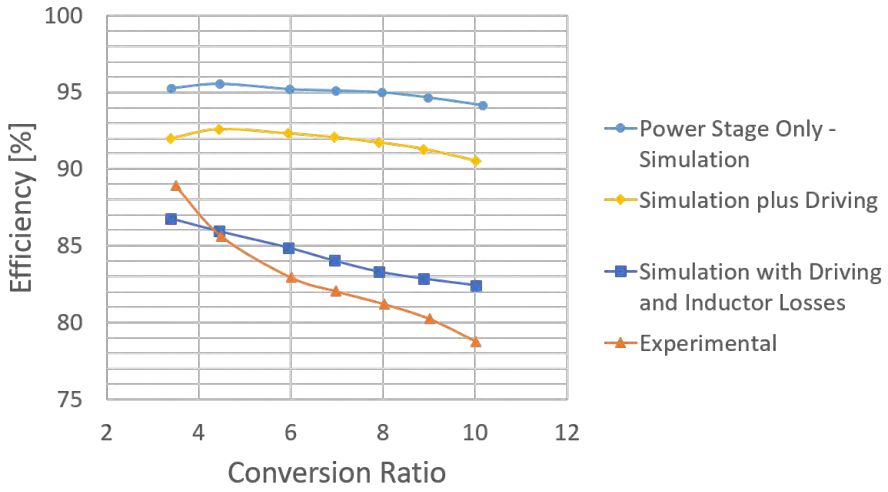


Figure 4.5.34: Converter CHP1 mode simulation and experimental efficiency comparison at $f_s = 300kHz$.

Finally, CHP4 is considered in Fig.4.5.36. As it is possible to see, the same considerations made in the other two 300kHz operating modes case apply here. Driving losses weight is strongly reduced if compared to the 1.8MHz switching frequency case, while the inductor dissipation importance is increased. Data obtained adding the estimated driving and inductor losses to the original ideal-driving simulation are compatible with the experimental ones, considering that a certain degree of approximation in the estimations performed exists.

Overall, the performed analysis suggests that, in the 1.8MHz switching frequency case, driving losses have a huge impact on the converter performance, helping to explain the gap in efficiency between this and the 300kHz operation case. However, even though driving and inductor losses make up for most of the gap between simulation and experimental data, a gap still exists, especially at higher gains. Part of this gap can be for sure related to a self-heating related effect, however some other loss mechanism still unaccounted for exists.
In the 300kHz case instead, driving losses are much reduced and their contribution, together with the inductor losses' one, seems to reasonably explain

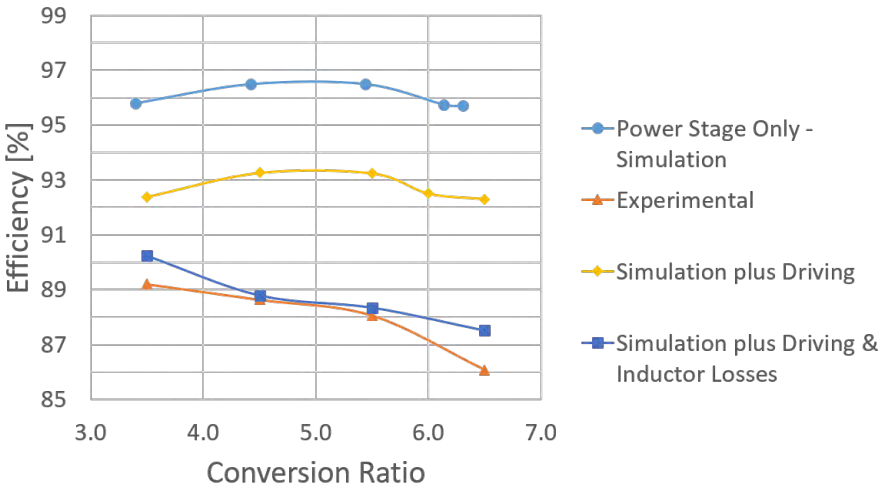


Figure 4.5.35: Converter CHP2 mode simulation and experimental efficiency comparison at $f_s = 300kHz$.

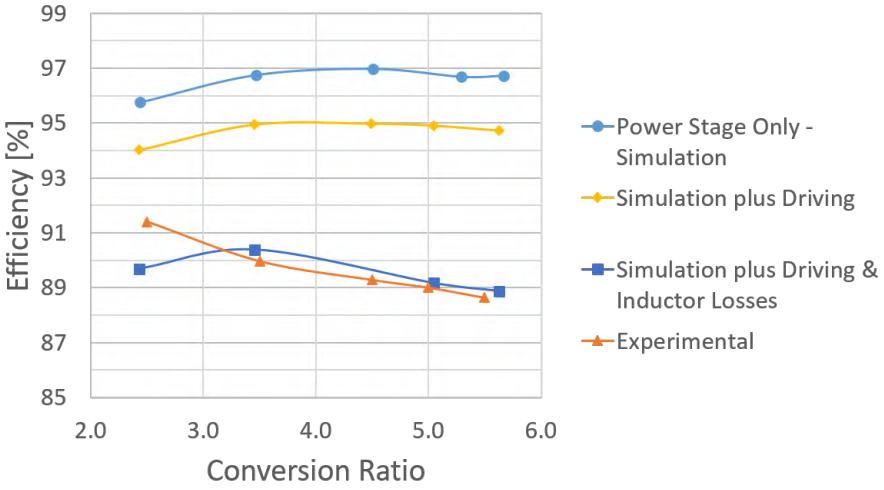


Figure 4.5.36: Converter CHP4 mode simulation and experimental efficiency comparison at $f_s = 300kHz$.

the gap between power-stage simulation and experimental results. In this case, it is also interesting to notice the increased weight of inductor-related losses, suggesting that, by choosing a more suitable inductor, the prototype performance could be improved.

4.5.4 Dead-Time Transitions Analysis

It was mentioned at the beginning of section 4.5.2 that the converter power--stage was designed under the hypothesis of dominating conduction losses. However, experimental results suggest that this is not the case for the real--case scenario of this target application. To optimize the performance it is then important to understand what happens during the dead-time in between the converter ON and OFF-phases, studying the voltage transitions at the different nodes, to be able to understand how it is possible to achieve soft-switching.

CHP1 Mode Dead-Time Transitions

The transition from the ON to the OFF phase is considered first. It is important to remember that, in the ON-phase, the inductor is charged, therefore, at the beginning of the aforementioned transition i_L is always positive. The converter equivalent circuit in this phase is shown in Fig.4.5.38. It is important to notice that, since during the converter ON-phase S_1, S_4 and S_6 were conducting, while S_2, S_3 and S_5 were OFF (see Fig.4.5.37), at the beginning of the dead-time we have $v_{S_2} = v_{S_3} = V_{in}$ and $v_{S_5} = v_o - 2V_{in}$; v_{S_1},v_{S_4} and v_{S_6} are instead all equal to zero.

When all the switches are turned OFF at the beginning of the transition phase, i_L keeps flowing and distributes between i_x, i_y i_z, i_u, i_v and i_w (that are all positive with the directions reported in the picture), drawing charge from S_2 and S_3 drain-source capacitance, while charging S_1, S_4 and S_6 C_{ds} and discharging S_5's. As a consequence v_{S_2} decreases and v_{S_1} increases in a resonant way, until $v_{S_1} = V_{in}$ and $v_{S_2} = 0$. At that point the body diodes of S_2 and S_3 can turn ON, allowing i_L to flow onto them, yielding zero-voltage turn-ON for both S_2 and S_3. The same process takes place in S_6, S_4 and S_5 case, with v_{S_6} and v_{S_4} that increase and v_{S_5} decreases in a resonant way, until S_5 body diode is no longer reverse-biased and can turn ON. Fig.4.5.39 shows the experimental waveforms associated with this transition taken at

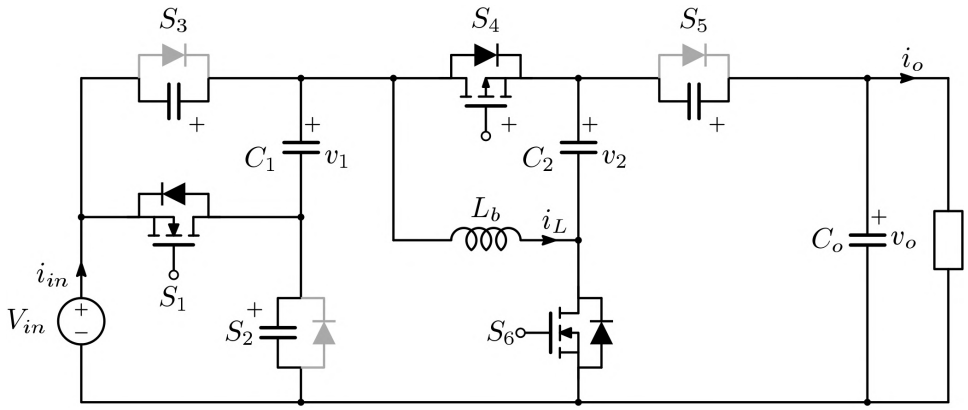


Figure 4.5.37: CHP1 mode ON-phase equivalent circuit.

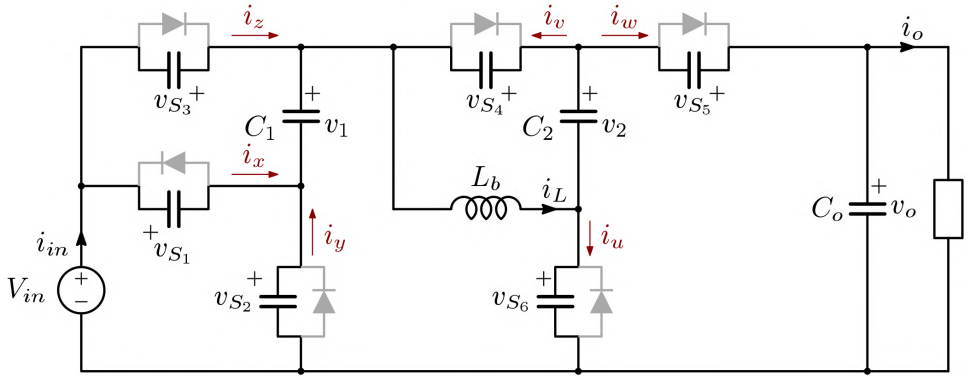


Figure 4.5.38: Converter equivalent circuit and inductor current contributions during the transition from CHP1 mode ON to the OFF-phase.

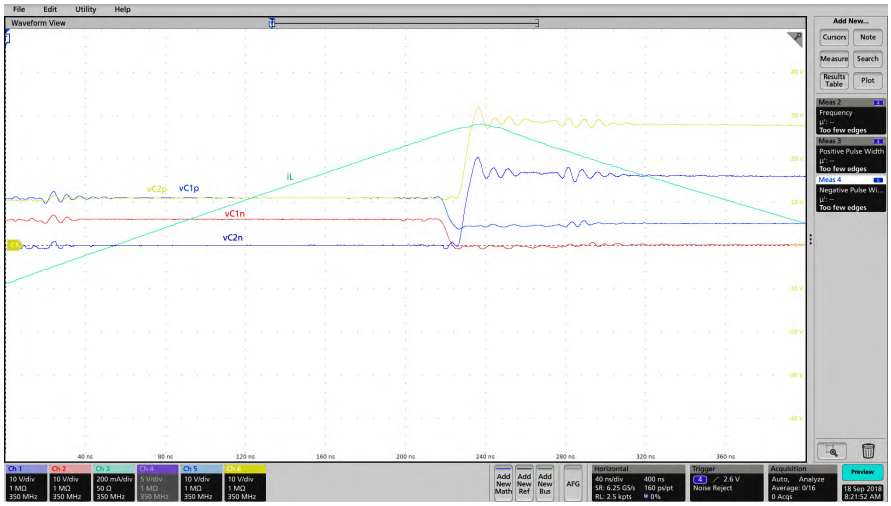


Figure 4.5.39: CHP1 operating mode transition from the ON to the OFF--phase: experimental waveforms at 1.8MHz switching frequency, $V_{in} = 6V$, $I_o = 70mA$ and $v_o \approx 27.3V$. The waveforms $vC2p$ and $vC2n$ correspond to C_2 positive and negative plate voltage respectively. Waveforms $vC1p$ and $vC1n$ are instead C_1 positive and negative plate voltage. Waveform i_L is the measured inductor current. Time and voltage scales are 40ns and 10V per division respectively; the inductor current waveform vertical scale is instead 200mA/div.

$f_s = 1.8MHz$, $V_{in} = 6V$, $I_o = 70mA$ and $v_o \approx 27.3V$. Waveforms $vC1p$, $vC1n$, $vC2p$ and $vC2n$ correspond to C_1 and C_2 positive (p) and negative (n) plates voltage respectively. Waveform iL is the measured inductor current. It is possible to appreciate the resonant transitions characterizing the nodes movements.

The transition from the OFF to the ON-phase can instead take place in two different ways. It must in fact be noticed that, in the OFF-phase, the inductor is being discharged, therefore its current is decreasing. As a consequence, depending on the sign of the inductor current value at the end of the converter OFF-phase, two different situations can take place. Fig.4.5.41 shows the converter equivalent circuit during the transition from the OFF to the ON-phase in the case the inductor current minimum value is positive. It is important to notice that, since during the OFF-phase S_2, S_3 and S_5

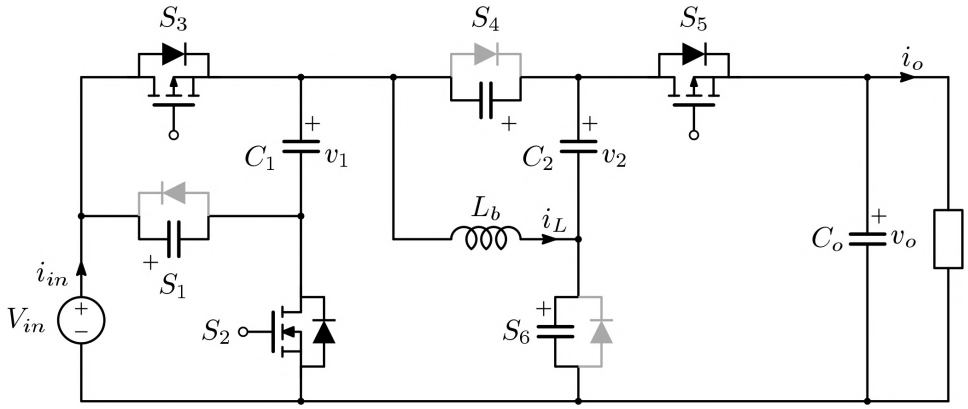


Figure 4.5.40: CHP1 mode OFF-phase equivalent circuit.

were conducing, v_{S_2}, v_{S_3} and v_{S_5} are all equal to zero at the start of this transition phase. Therefore, when the switches are all turned OFF, the body diodes of S_2, S_3 and S_5 can turn-ON, allowing the inductor current to flow onto them. In this scenario there is no resonant charge/discharge, and the drain-source capacitances of S_1, S_4 and S_6 remain all charged, giving a hard transition when the corresponding switches are turned-ON. Fig.4.5.42 shows the converter main waveforms in such condition; as it is possible to notice, no resonant transition occurs. A slight decrease in $vC1n$ and $vC1p$ occurs at the beginning of the dead-time; in particular, as it is possible to notice, $vC1n$ becomes slightly negative and this can be explained by the turn-ON of S_1 body diode. The waveforms $vC2p$ and $vC2n$ show instead a slight increase, associated with S_5 body diode turn-ON.

In the case the minimum inductor current is negative instead, the converter is once again characterized by resonant transitions. As it is possible to observe in Fig.4.5.43 in fact, the negative inductor current splits in different paths, generating the different currents i_x, i_y, i_z, i_u, i_v and i_w that are all positive with the direction depicted in the figure. Remembering that at the beginning of the transition phase $v_{S_2} = v_{S_3} = v_{S_5} = 0$, while the other C_{ds} are all charged in the polarities shown in Fig.4.5.43, it is straightforward to understand that i_L charges S_3 and S_2 drain-source capacitance while discharging S_1's (it charges it with negative polarity). In a similar way, the negative i_L draws charge from S_6 and S_4 C_{ds}, while charging S_5's and making then v_{S_5} increase, while v_{S_6} and v_{S_4} decrease. Therefore, if the dead-time duration is long enough to allow the resonant charge/discharge process to complete,

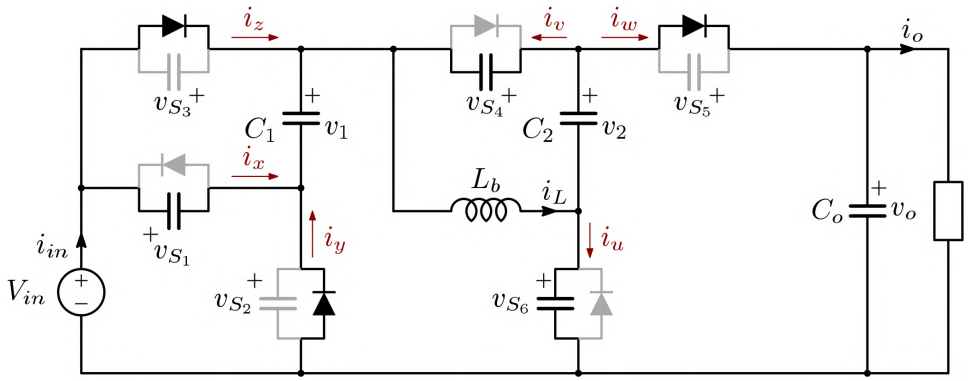


Figure 4.5.41: Converter equivalent circuit and inductor current contributions during the transition from CHP1 mode OFF to the ON-phase in the case of a positive minimum inductor current.

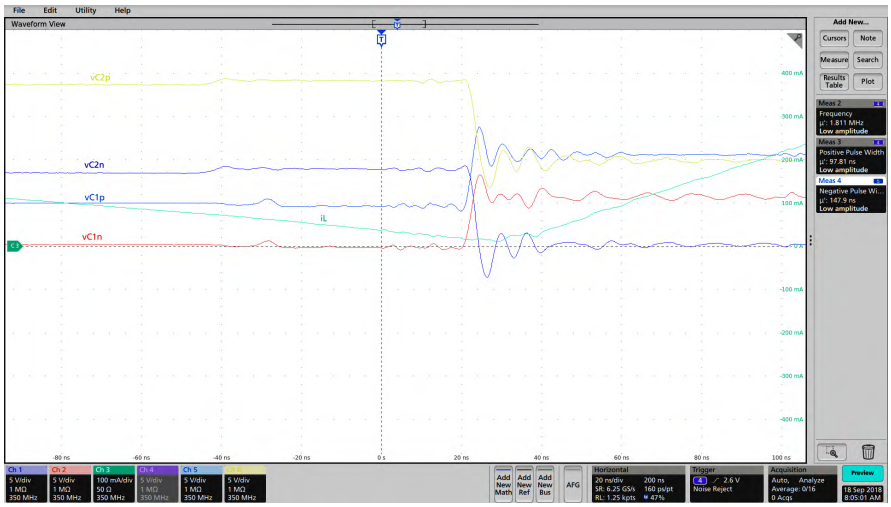


Figure 4.5.42: CHP1 operating mode transition from the OFF to the ON--phase: experimental waveforms at 1.8MHz switching frequency, $V_{in} = 6V$, $I_o = 135mA$ and $v_o \approx 18.6V$. The waveforms $vC2p$ and $vC2n$ correspond to C_2 positive and negative plate voltage respectively. Waveforms vC1p and vC1n are instead C_1 positive and negative plate voltage. As it is possible to see, in this case the inductor current i_L is always positive. Time and voltage scales are 20ns and 5V per division respectively; the inductor current waveform vertical scale is instead 100mA/div.

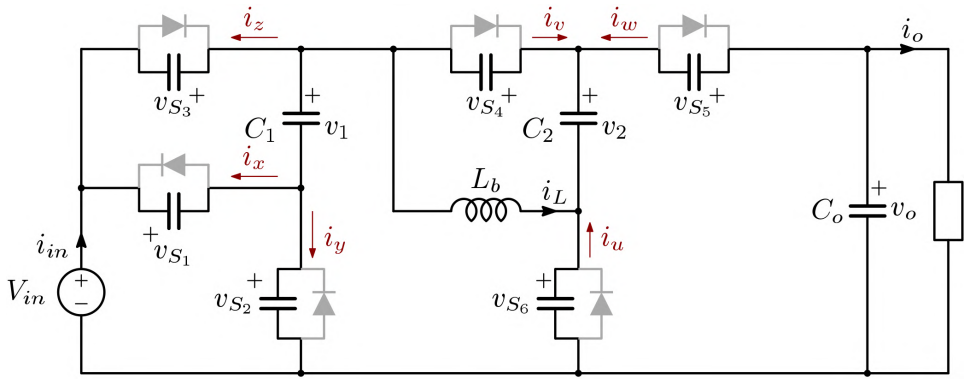


Figure 4.5.43: Converter equivalent circuit and inductor current contributions during the transition from CHP1 mode OFF to the ON-phase in the case of a negative minimum inductor current.

zero-voltage turn-ON is obtained for S_6, S_4 and S_1. Sizing the converter to work in the so-called quasi-square-wave operation would therefore be beneficial, allowing switching losses reduction though soft-switching transitions. Fig.4.5.44 shows he main converter waveforms during the transition from the OFF to the ON phase, in the case of a negative inductor current at the end of the OFF-phase; it is possible to appreciate the resonant transitions of the converter nodes voltages.

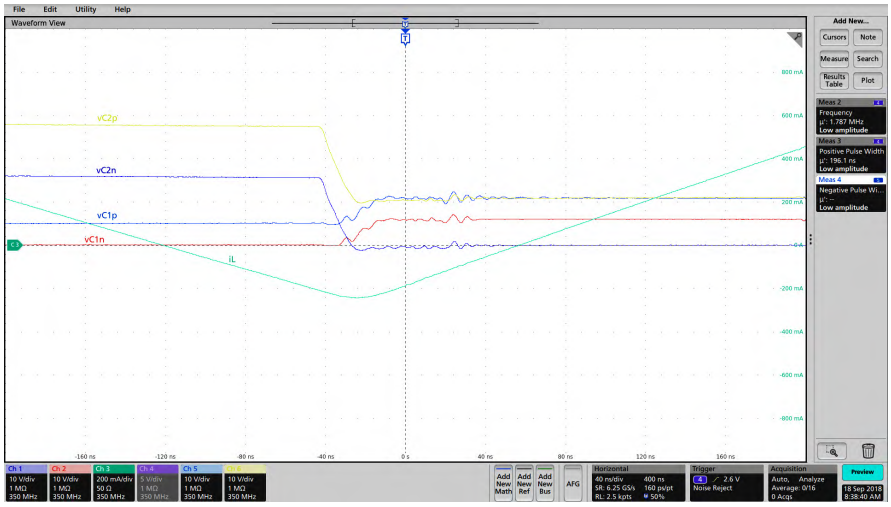


Figure 4.5.44: CHP1 operating mode transition from the OFF to the ON--phase: experimental waveforms at 1.8MHz switching frequency, $V_{in} = 6V$, $I_o = 70mA$ and $v_o \approx 27.3V$. The waveforms $vC2p$ and $vC2n$ correspond to C_2 positive and negative plate voltage respectively. Waveforms $vC1p$ and $vC1n$ are instead C_1 positive and negative plate voltage. Time and voltage scales are 40ns and 10V per division respectively; the inductor current waveform vertical scale is instead 200mA/div.

CHP2 Mode Dead-Time Transitions

CHP2 operating mode case is now considered. Once again, the transition from the ON to the OFF phase is considered first. As in CHP1 mode, also in this case the inductor is charged during the ON-phase, therefore, at the beginning of the transition from the ON to the OFF-phase, i_L is always positive. The converter equivalent circuit in this phase is shown in Fig.4.5.46. It is important to notice that, since during the converter ON-phase S_2, S_3, S_4 and S_6 were conducing, while S_1 and S_5 were OFF (CHP2 ON-phase equivalent circuit can be seen in Fig.4.5.45), at the beginning of the transition we have $v_{S_1} = V_{in}$ and $v_{S_5} = v_o - V_{in}$, while v_{S_2},v_{S_3}, v_{S_4} and v_{S_6} are instead all equal to zero. Because of this, when all the switches are turned OFF, considering the first cell, the inductor current can split into two contributions and force S_2 and S_3 body diodes into conduction. As a consequence, S_1 C_{ds} does not discharge and v_{S_1} remains high until the switch is turned ON, giving a hard turn-ON. Considering the second charge pump cell instead, since at the beginning of the transition phase v_{S_5} is equal to $v_o - V_{in}$, S_5 body diode is reverse biased and cannot turn-ON. As a consequence, i_L splits into three paths, generating the currents i_u, i_v and i_w that are all positive with the direction shown in Fig.4.5.46. It is then straightforward to see that, as a consequence, S_5 drain-source capacitance is discharged while S_4 and S_6's are charged. Therefore, resonant charge transfers take place until v_{S_5} decreases to zero and the inductor current can flow onto S_5 body diode, giving a soft turn-ON of switch S_5. As it is possible to see in Fig.4.5.47, showing the main converter waveforms ($vC1p$, $vC1n$, $vC2p$ and $vC2n$ are respectively C_1 and C_2 positive (p) and negative (n) plate voltage) during the considered transitions, experimental results confirm the performed analysis. It is in particular possible to appreciate $vC2p$ and $vC2n$ resonant transitions as opposed to $vC1p$ and $vC1n$ hard ones.

If the transition from the OFF to the ON-phase is considered, since in the OFF phase the inductor is discharged and its current decreases, two different situations can occur, depending on whether the inductor current at the end of the OFF-phase is positive or negative. Analysing the transitions however, it must be also remembered that, in CHP2 OFF-phase S_1 and S_5 are ON, while all the other switches are OFF (see Fig.4.5.48); if the minimum inductor current is positive then, considering the first charge-pump cell, S_2 and S_3 body diodes are reverse-biased and cannot turn ON. As a consequence,

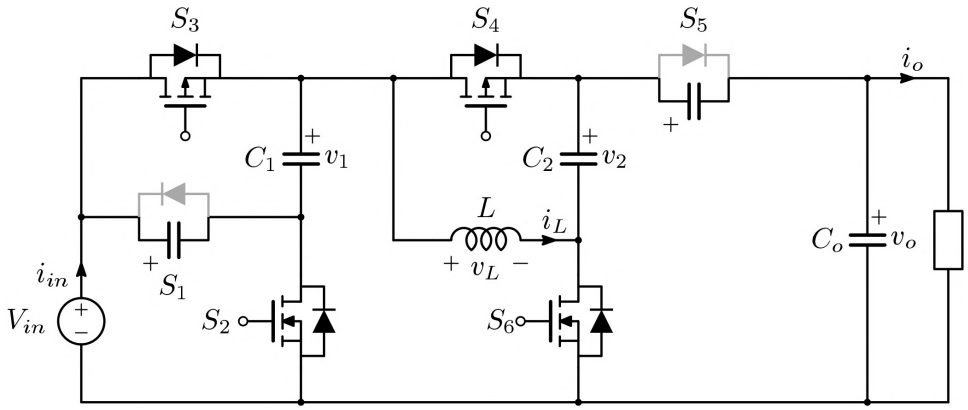


Figure 4.5.45: CHP2 mode ON-phase equivalent circuit.

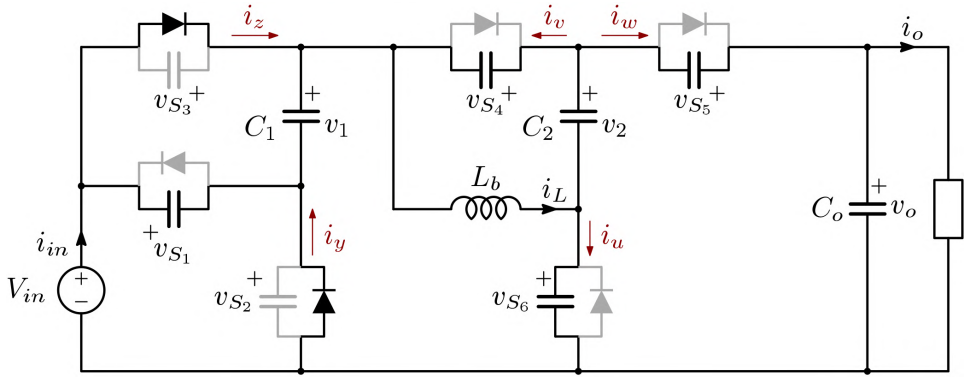


Figure 4.5.46: Converter equivalent circuit and inductor current contributions during the transition from CHP2 mode ON to the OFF-phase.

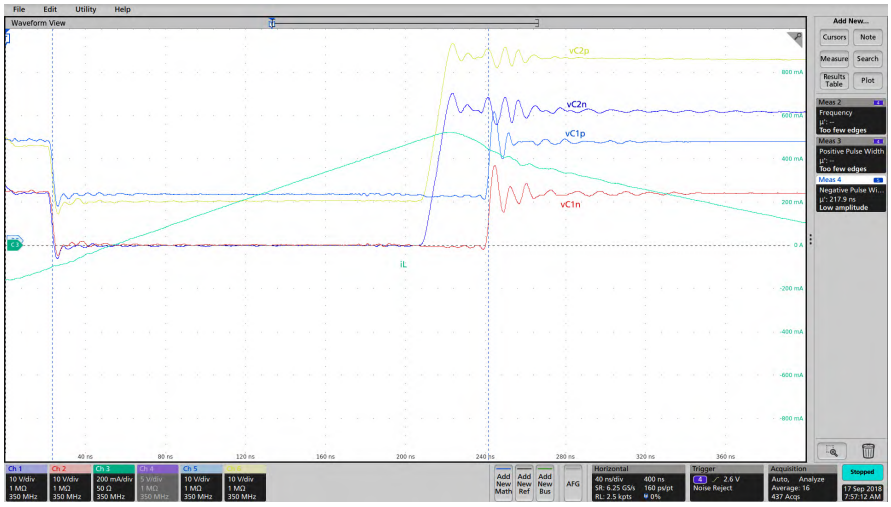


Figure 4.5.47: CHP2 operating mode transition from the ON to the OFF--phase: experimental waveforms at 1.8MHz switching frequency, $V_{in} = 12V$, $I_o = 70mA$ and $v_o \approx 42V$. The waveforms $vC2p$ and $vC2n$ correspond to C_2 positive and negative plate voltage respectively. Waveforms $vC1p$ and $vC1n$ are instead C_1 positive and negative plate voltage. Time and voltage scales are 40ns and 10V per division respectively; the inductor current waveform vertical scale is instead 200mA/div.

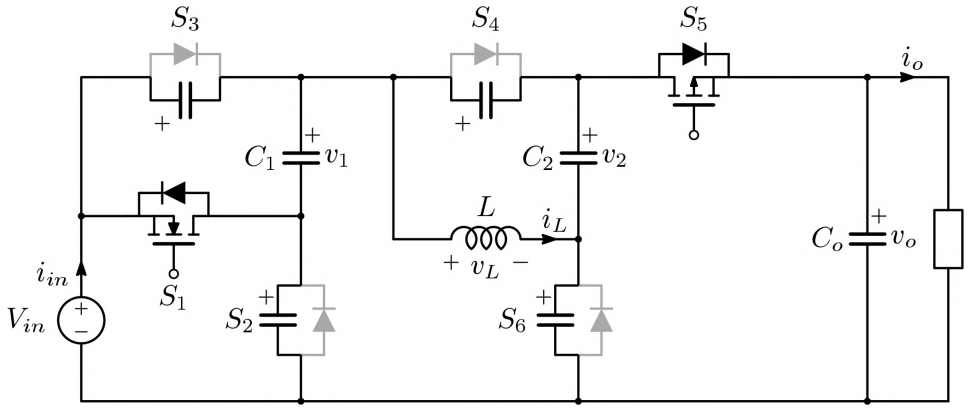


Figure 4.5.48: CHP2 mode OFF-phase equivalent circuit.

i_L splits into three paths, generating the currents i_x, i_y and i_z that are all positive with the convention used in Fig.4.5.49. Therefore, a resonant charge transfer occurs, with v_{S_2} and v_{S_3} decreasing while v_{S_1} increases until the body diodes of S_2 and S_3 can turn ON, allowing the inductor current to flow onto them. If the dead-time is long enough then, soft-switching is achieved for S_2 and S_3. Considering the second cell instead, since S_5 body diode is not reverse-biased, i_L can flow onto it. As a consequence, S_4 and S_5 C_{ds} are not discharged until the corresponding switches are turned ON, not achieving soft-switching for these devices. An example of the transition from the OFF to the ON-phase in the case of a positive minimum inductor current can be observed in Fig.4.5.50. It is possible to appreciate $vC1p$ and $vC1n$ resonant transitions, even though the dead-time duration is not long enough to obtain soft-switching and the ON-phase begins before $vC1n$ has fully decreased.

If the minimum inductor current is negative instead, the transitions taking place during the considered dead-time differ. As shown in Fig.4.5.51 in fact, considering the first charge-pump cell, the inductor current can directly flow onto S_1 body diode. Therefore, since v_{S_2} and v_{S_3} do not decrease until S_2 and S_3 are turned ON, these switches are characterized by a hard turn-ON. Considering the second cell instead, a resonant charge transfer process takes place, discharging both S_5 and S_6 drain-source capacitance. However, it must be noticed that, since i_L flows onto S_1 body diode, C_1 is now connected in series with the input. As a consequence, S_4 drain voltage is fixed and equal to $V_{in}+v_D+v_1$. S_6 drain-source voltage v_{S_6} is then given by $V_{in}+v_d+v_1-v_{S_4}-v_2$.

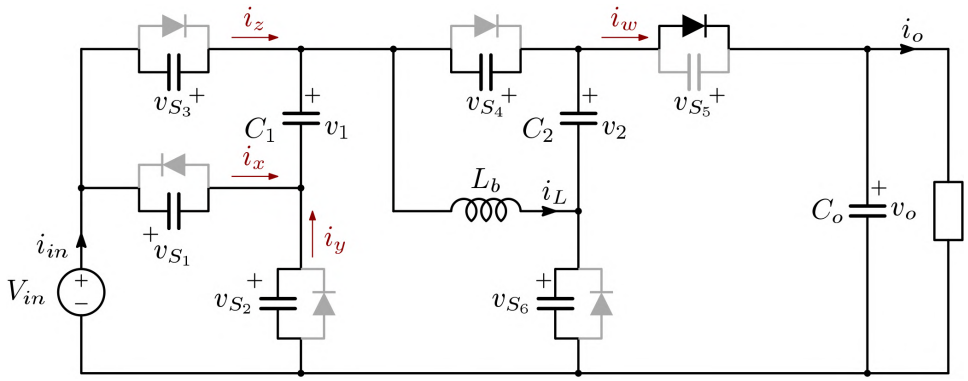


Figure 4.5.49: Converter equivalent circuit and inductor current contributions during the transition from CHP2 mode OFF to the ON-phase in the case of a positive minimum inductor current.

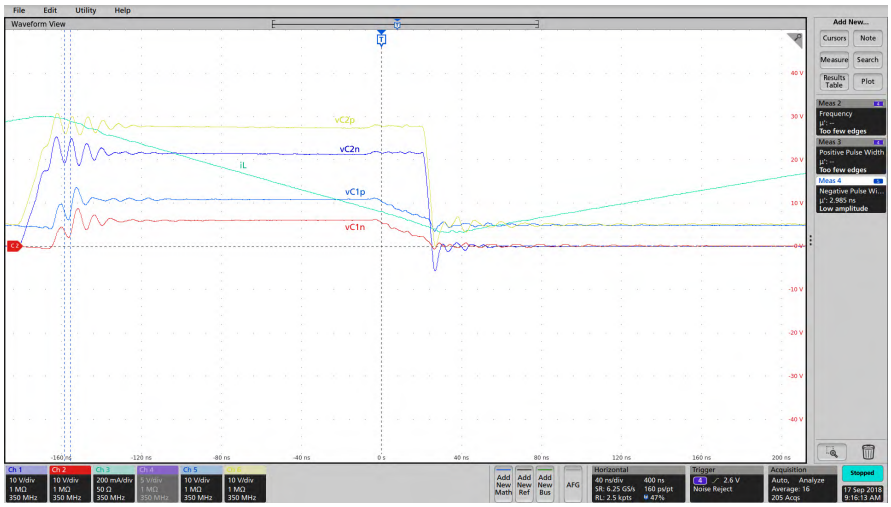


Figure 4.5.50: CHP2 operating mode transition from the OFF to the ON--phase: experimental waveforms at 1.8MHz switching frequency, $V_{in} = 6V$, $I_o = 100mA$ and $v_o \approx 26V$. The waveforms $vC2p$ and $vC2n$ correspond to C_2 positive and negative plate voltage respectively. Waveforms $vC1p$ and $vC1n$ are instead C_1 positive and negative plate voltage. As it is possible to see, in this case the inductor current i_L is always positive. Time and voltage scales are 40ns and 10V per division respectively; the inductor current waveform vertical scale is instead 200mA/div.

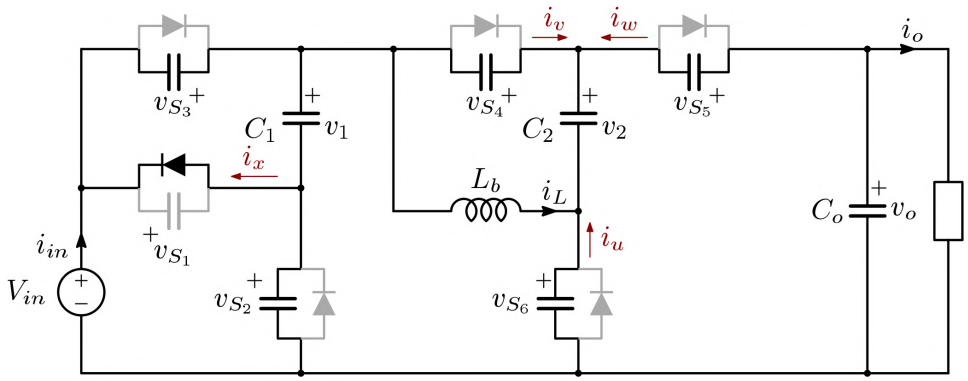


Figure 4.5.51: Converter equivalent circuit and inductor current contributions during the transition from CHP2 mode OFF to the ON-phase in the case of a negative minimum inductor current.

It must also be noticed that, at the beginning of this transition phase, v_{S_6} is equal to $v_o - V_{in}$ while v_{S_4} is instead equal to $v_o - 2V_{in}$. Therefore, since v_{S_4} is lower than v_{S_6}, S_4 C_{ds} discharges first, yielding $v_{S_6} = V_{in} + v_d + v_1 - v_2 \approx V_{in} + v_d$. This clamping effect does not allow S_6 C_{ds} to discharge completely, ultimately yielding a hard turn-ON for the device. Experimental results confirm the analysis, as shown in Fig.4.5.52. Waveforms $vC2p$ and $vC2n$ are C_2 positive and negative plate voltage respectively, while $vC1p$ is C_1 positive plate voltage. As it is possible to notice, a resonant decrease of both $vC2p$ and $vC2n$ occurs at first (corresponding to v_{S_6} decrease); however, when $vC2p$ becomes approximately equal to $vC1p$, S_4 body diode can turn ON and vS_6 (that corresponds to $vC2n$) is clamped.

As a result of this analysis, it is important to notice that, in CHP2 case, achieving soft-switching for the devices of both charge-pump cells at the same time is not possible. Furthermore, even when quasi-square wave operation is employed, soft turn-ON for S_6 cannot be achieved, due to a clamping effect caused by the inductor current flowing on S_1 body diode together with S_4 and S_6 different voltage stress levels. These characteristics figure to be an important limitation, that may suggest to avoid the use of CHP2 mode, transitioning directly from CHP4 to CHP1.

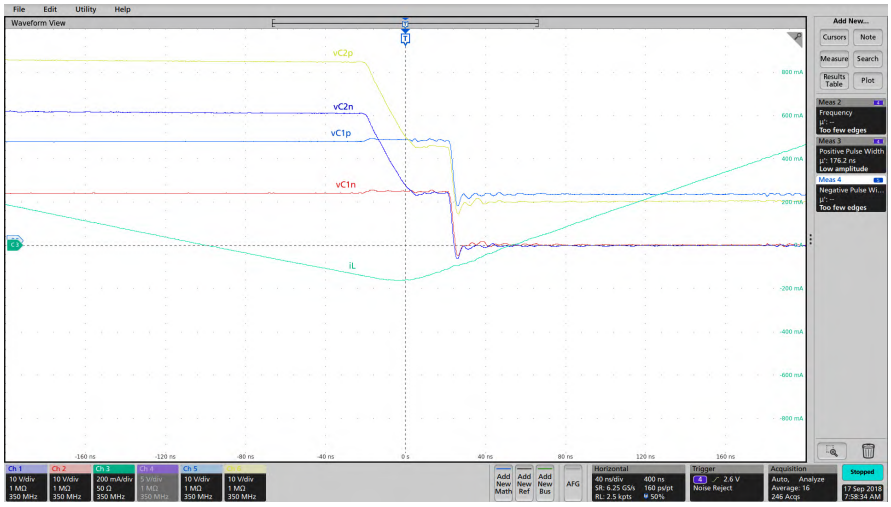


Figure 4.5.52: CHP2 operating mode transition from the OFF to the ON--phase: experimental waveforms at 1.8MHz switching frequency, $V_{in} = 12V$, $I_o = 70mA$ and $v_o \approx 42V$. The waveforms $vC2p$ and $vC2n$ correspond to C_2 positive and negative plate voltage respectively. Waveforms $vC1p$ and $vC1n$ are instead C_1 positive and negative plate voltage. Time and voltage scales are 40ns and 10V per division respectively; the inductor current waveform vertical scale is instead 200mA/div.

CHP4 Mode Dead-Time Transitions

Finally, CHP4 operating mode is analysed In this case, the first flying capacitor is constantly in parallel with the input source, therefore the analysis regards only the second charge-pump cell, where the same considerations made in CHP1 case apply. In the case of the transition between the ON and the OFF-phase in fact, the inductor current is always positive but, since S_5 was OFF, at the beginning of the transition its body diode is reverse-biased (CHP4 mode ON-phase equivalent circuit is shown in Fig.4.5.53). As a consequence, i_L splits into different paths, generating the currents i_u, i_v and i_w that are all positive with the convention used in Fig.4.5.54. As a consequence, a resonant charge/discharge process takes place, with i_v and i_u charging S_4 and S_6 drain-source capacitances while i_w discharges S_5's, until the body diode of S_5 is no longer reverse-biased and the inductor current can flow onto it, yielding zero-voltage turn-ON for S_5 at the beginning of the OFF-phase. Fig.4.5.55 shows the experimental waveforms corresponding to this transition, taken at $f_s = 1.8MHz$, $V_{in} = 12V$ and $I_o = 70mA$; it is possible to appreciate how the inductor current i_L slope changes its sign only after the resonant transitions are over, meaning that S_5 body diode is finally ON, yielding $v_L = v_o - 2V_{in} < 0$.

As mentioned in CHP2 and CHP1 case, also CHP4 mode transition from the converter OFF to the ON-state can occur in two different ways, depending on whether the inductor current at the end of the OFF-phase is positive or negative. If i_L is positive, when S_5 is turned OFF the inductor current directly transfers onto S_5 body diode and no resonant transition occurs. The corresponding equivalent circuit in shown in Fig.4.5.57. As a consequence,

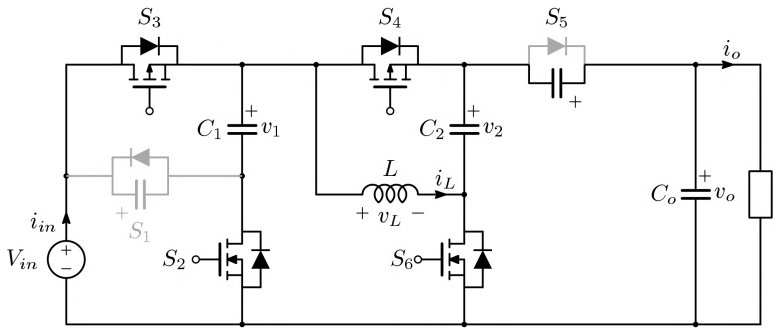


Figure 4.5.53: CHP4 mode ON-phase equivalent circuit.

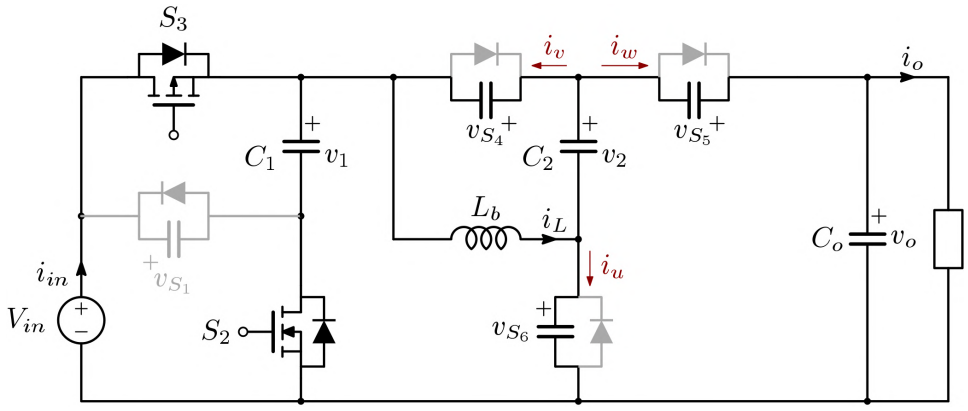


Figure 4.5.54: Converter equivalent circuit and inductor current contributions during the transition from CHP4 mode ON to the OFF-phase.

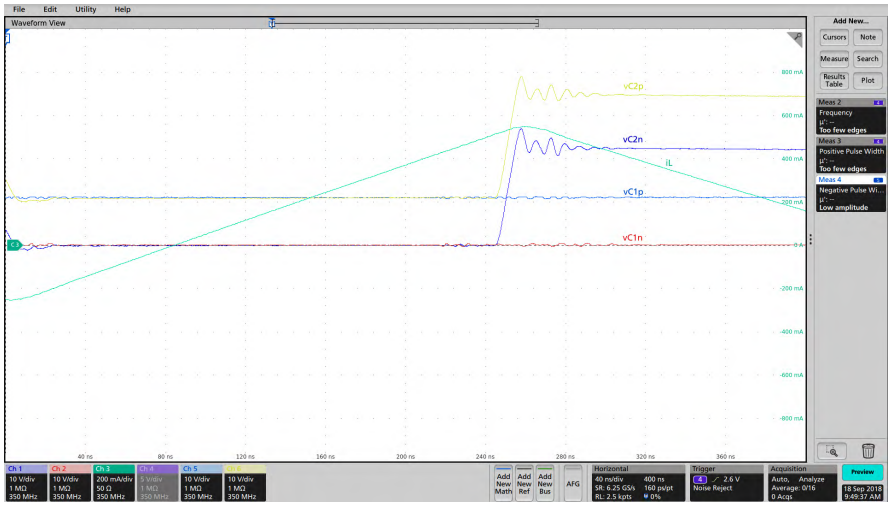


Figure 4.5.55: CHP4 operating mode transition from the ON to the OFF--phase: experimental waveforms at 1.8MHz switching frequency, $V_{in} = 12V$, $I_o = 70mA$ and $v_o \approx 33.6V$. The waveforms $vC2p$ and $vC2n$ correspond to C_2 positive and negative plate voltage respectively. Waveforms $vC1p$ and $vC1n$ are instead C_1 positive and negative plate voltage. Waveform i_L is the measured inductor current. Time and voltage scales are 40ns and 10V per division respectively; the inductor current waveform vertical scale is instead 200mA/div.

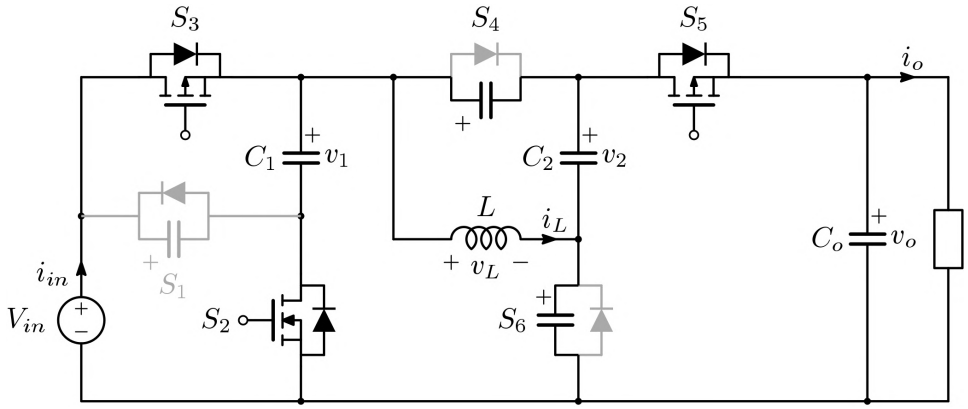


Figure 4.5.56: CHP4 mode OFF-phase equivalent circuit.

the turn-ON of S_4 and S_6 at the beginning of the converter ON-phase is hard. Fig.4.5.58 shows the converter experimental waveforms in this case; as it is possible to see, the end of the converter OFF-phase is associated with a slight increase in $vC2p$ and $vC2n$, associated with S_5 body diode turn-ON.

If i_L at the end of the OFF-phase is negative instead, the inductor current cannot flow onto S_5 body diode and it splits into different paths, generating the currents i_u, i_v and i_w. Since these currents are all positive with the directions considered in Fig.4.5.59, a resonant charge/discharge phase occurs in which charge is drawn from S_4 and S_6 source-drain capacitances, while S_5's is charged. If the dead-time duration is long enough, this process ends when the body diodes of S_4 and S_6 are no longer reverse-biased and the inductor current can flow onto S_6, yielding zero-voltage turn-ON at the beginning of the converter ON-phase. Therefore, as seen in CHP1 case, also in CHP4 mode sizing the converter to work in the so-called quasi-square-wave operation would therefore be beneficial, allowing switching losses reduction though soft--switching transitions. The aforementioned considerations are confirmed by the experimental observations, as shown in Fig.4.5.60. As it is possible to see in fact, in this case $vC2p$ and $vC2n$ transitions are resonant (the curves slope is in fact much lower if compared to Fig.4.5.58 case) and it can be noticed that $vC2n$ becomes slightly negative before the beginning of the ON-phase, marked by the change of slope in the inductor current iL.

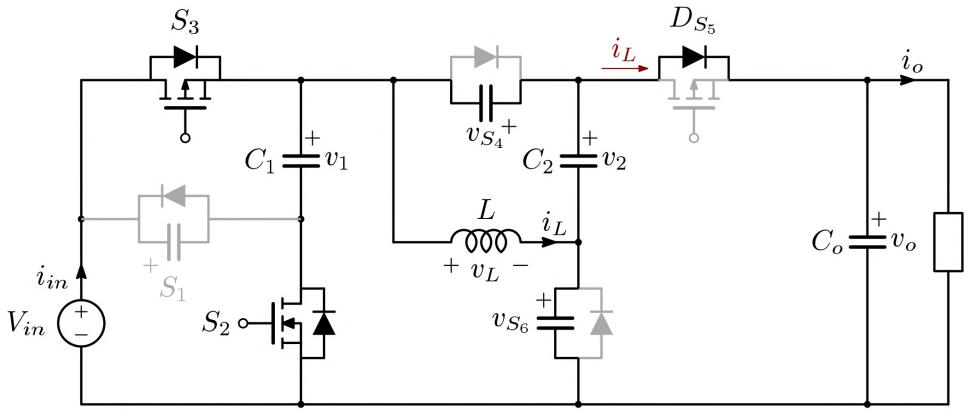


Figure 4.5.57: Converter equivalent circuit and inductor current contributions during the transition from CHP4 mode OFF to the ON-phase in the case of a positive minimum inductor current.

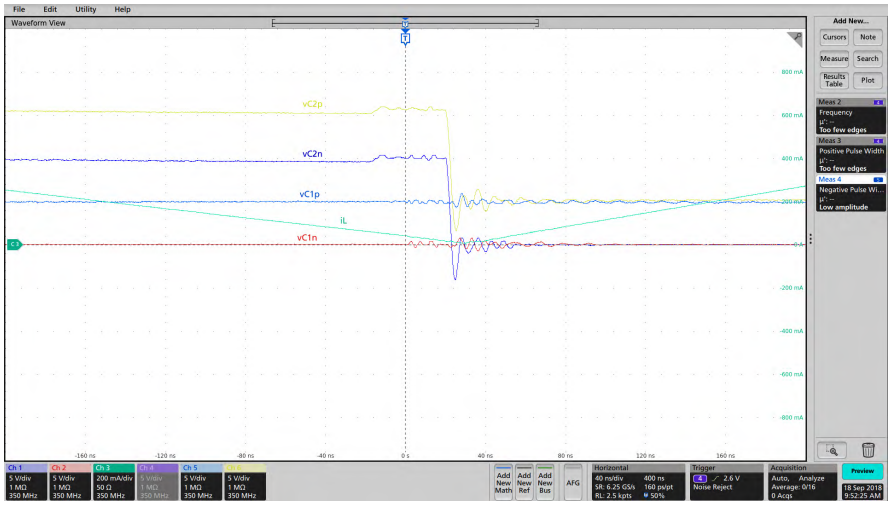


Figure 4.5.58: CHP4 operating mode transition from the OFF to the ON--phase: experimental waveforms at 1.8MHz switching frequency, $V_{in} = 6V$, $I_o = 100mA$ and $v_o \approx 15V$. The waveforms $vC2p$ and $vC2n$ correspond to C_2 positive and negative plate voltage respectively. Waveforms $vC1p$ and $vC1n$ are instead C_1 positive and negative plate voltage. Waveform i_L is the measured inductor current. Time and voltage scales are 40ns and 5V per division respectively; the inductor current waveform vertical scale is instead 200mA/div.

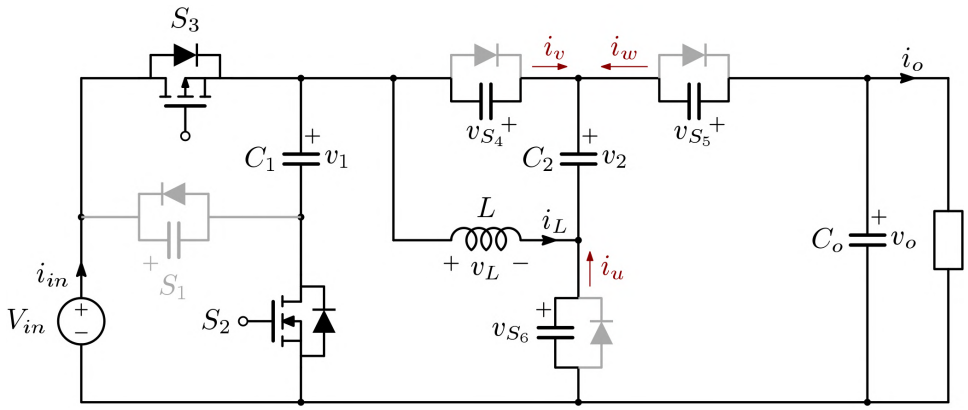


Figure 4.5.59: Converter equivalent circuit and inductor current contributions during the transition from CHP4 mode OFF to the ON-phase in the case of a negative minimum inductor current.

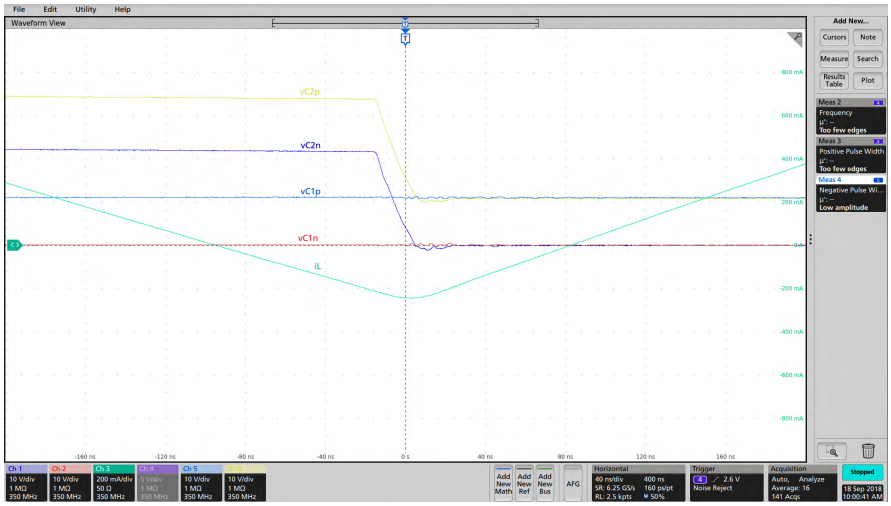


Figure 4.5.60: CHP4 operating mode transition from the OFF to the ON--phase: experimental waveforms at 1.8MHz switching frequency, $V_{in} = 12V$, $I_o = 70mA$ and $v_o \approx 33.6V$. The waveforms $vC2p$ and $vC2n$ correspond to C_2 positive and negative plate voltage respectively. Waveforms $vC1p$ and $vC1n$ are instead C_1 positive and negative plate voltage. Waveform i_L is the measured inductor current. Time and voltage scales are 40ns and 10V per division respectively; the inductor current waveform vertical scale is instead 200mA/div.

4.5.5 Resume and Final Considerations

The previously proposed buck-boost capable reconfigurable hybrid topology offers some interesting properties and was a first attempt at building a hybrid converter with a specific industrial application target. Anyway, implementing a buck-boost capable topology using charge-pump cells is for some aspects highly challenging; it would for example require using back to back MOSFETs to block voltages in both polarities. This solution, together with the switches implementation and driving problems, would also pose some design challenges regarding the inductor current free-wheeling during dead-time. Due to these considerations a simplified version of the topology was implemented as a more general proof of concept and possibly a solution for boost-only applications. Two different PCB prototypes were built to allow testing at $f_{sw} = 1.8\,MHz$ and $300\,kHz$. Experimental characterization was carried out at constant output current over the whole specified conversion ratios range without the use of a heat sink. Keeping in mind that the designed prototype was meant to be a proof of concept, the experimental results show that the converter real-world implementation is possible even though its design is not optimized.

To optimize the converter performance, a redesign should be performed, which could not be completed due to the imposed project deadlines. Strong attention should be put in the optimization of the power stage design, sizing the devices to optimize both the conduction and switching losses. An optimized design of the converter should also include a bootstrap capacitor allowing to implement S_1 as an N-MOS, together with a PWM driver capable of generating asymmetric dead-times. Further study should also consider implementing $S_3\,S_4$ and S_5 as N-MOSes too, even though that would require solving the problem of generating a V_g equal to $V_s + 2.5V$, that would be for example higher than V_{in} in S_3 case.

Is is also important to notice that, in real-world applications, it may be interesting to consider the implementation of mode CHP4 alone. This is in fact the operating mode that shows the higher efficiencies and requests the lower number of components, while still yielding a reduced average inductor current if compared to a standard boost converter.

4.6 Non-isolated High Step-up DC-DC Converter with Minimum Switch Voltage Stress

The need for high step-up DC-DC converters to be used as interfaces between low-voltage, high-current renewable energy sources, like fuel cells and photovoltaic modules, and a common high voltage DC bus in distributed generation systems, has boosted the research efforts toward solutions capable of overcoming the limitations of the conventional Boost topology. The high voltage gain can be achieved exploring different approaches, like using charge pump circuits, voltage multiplier cells, magnetic coupling, voltage lift, etc. A quite vast overview of the different techniques can be found in [9] – [14].

Most of the topologies presented in literature are based on the basic Boost cell, like in [15] – [17], meaning that the switch voltage stress, even if lower than the output voltage, always remains higher than the input voltage, and dependent on the switch duty-cycle. Moreover, being the main magnetic element in series with the input voltage, its average current value is the load current multiplied by the voltage gain (under the assumption of unity conversion efficiency).

On the other hand, switched-capacitor (SC) topologies may allow to reduce the switch voltage stress to the minimum value corresponding to the input voltage, like in the topologies proposed in [18], and [19]. The conversion efficiency of SC converters depends on the relative value of capacitor charging/discharging time constant τ_c compared with the switching period T_s. The best efficiency is obtained when $\tau_c \gg T_s$, so as the charging/discharging currents are almost constant in any phase. However, this favourable situation is not likely to occur in discrete SC converter implementations, where the low R_{DSon} of the switches, together with the relative low switching frequency compared with integrated solutions, will require unpractical capacitance values to satisfy the above inequality. In these situations, good efficiencies can still be obtained even in discrete implementations for high power levels, by shaping the charge/discharge currents through inductors (both parasitic elements and/or intentionally added), like in [18], and [20] – [22].

Despite their attractiveness in terms of modularity and possible integration due to the lack of magnetic elements, a very high voltage gain requires a large number of active devices, with relative driving circuitry. For this reason, SC circuits have been combined with coupled inductors to enhance their

step-up capability as well as to make the overall voltage conversion ratio easily controllable through the converter duty-cycle ([23]−[31]). The topology proposed in this paper is based on the work [32] and can be though as derived from the basic voltage-doubler switched-capacitor cell shown in Fig. 4.6.1a by adding a buck stage and a coupled inductor. The result is a step-up converter featuring: minimum switch voltage stress set by the input voltage; reduced inductor average current value, compared with a Boost converter with the same voltage gain; zero-voltage switching in the whole load range; soft diode turn off; leakage inductance exploitation; straightforward design. Drawbacks are a pulsed input current and a limited gain variation compared to Boost-based topologies. However, the achievable gain variation is enough to make the proposed topology useful for interfacing single photovoltaic panels with a high DC link voltage in micro-inverter applications.

In section 4.6.1, the derivation of the proposed converter is outlined, while section 4.6.2 describes in detail its operation. Section 4.6.3 derives useful equations to estimate component current and voltage stresses, and section 4.6.4 reports a simple, non iterative design procedure to calculate all the component values.

Experimental results, taken on a 44 V to 400 V, 300 W prototype, are included in section 4.6.5 showing the performance of the proposed high step-up topology.

4.6.1 Topology derivation

Starting from the basic voltage-doubler switched-capacitor cell shown in Fig. 4.6.1a, the first step toward the proposed high step-up topology, is shown in Fig. 4.6.1b. In order to charge C_1 to a voltage dependent on the switch S_1 duty-cycle D, an $L_b - C_b$ filter is added in parallel to S_2, thus forming an equivalent Buck cell, and a secondary winding is coupled to the filter inductor, with turns ratio n, and put in series with D_1. In this way, an equivalent voltage source, represented by the transformer secondary winding, is added in the C_1 charging path during S_2 ON interval. This voltage is a function of the converter duty-cycle, being related to the Buck capacitor voltage v_b. Assuming a unity efficiency and neglecting the transformer leakage inductance, the capacitor average voltages are $V_b = DV_g$ and $V_1 = (1 + nD)V_g$.

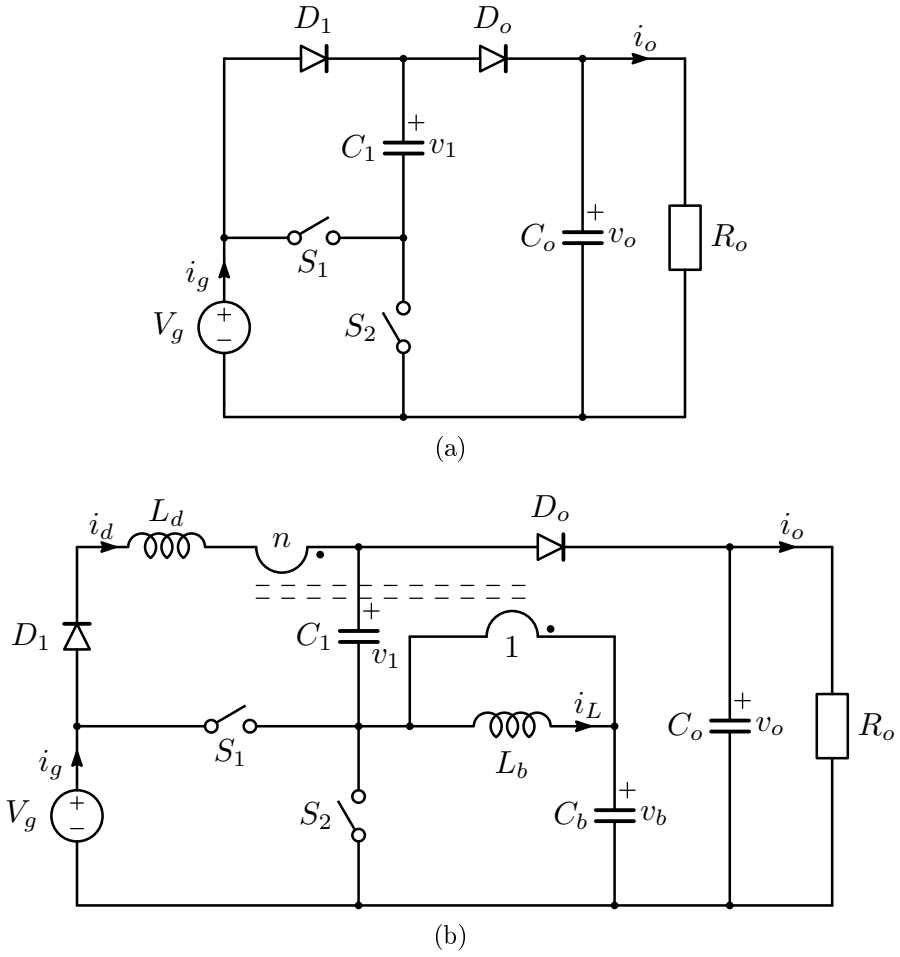


Figure 4.6.1: Topology derivation: (a) basic voltage-doubler switched-capacitor cell; (b) modified topology for higher voltage gains.

Consequently, the ideal voltage gain results:

$$M = \frac{V_o}{V_g} = \frac{V_g + V_1}{V_g} = 2 + nD. \tag{4.6.1}$$

Moreover, the *charge balance* condition at steady-state for the capacitors yields $\bar{i}_{Do} = \bar{i}_d = I_o$, and $\bar{i}_L = nI_o$.

In the circuit shown in Fig. 4.6.1b, the coupled windings introduce a non negligible leakage inductance L_d that helps to shape the C_1 charging current during the S_2 conduction interval. However, in the output capacitor charging phase (S_1 conduction interval), only component and layout parasitic inductors in the current path are present: the associated small value is not enough to limit the current peak during this phase, unless huge capacitance values are used. Even more problematic is the high frequency resonance that starts, at the D_1 turn-off instant, between the diode junction capacitance and the coupled inductor leakage inductance L_d, that causes a severe voltage stress and EMI generation.

For these reasons, the topology is modified as shown in Fig. 4.6.2, adding one more capacitor-diode branch $C_2 - D_2$. In this way, the secondary winding is in series with both charging and discharging current paths, as it will be clarified in the following section, and all diode voltages are clamped, thus eliminating the parasitic oscillations. Assuming that the conduction intervals of diodes D_o and $D_{1,2}$ are always lower than the corresponding switch conduction intervals of S_1 and S_2 respectively, the converter main waveforms in a switching period appear as shown in Fig. 4.6.3. The voltage gain, under the above assumptions, results from the charge pump actions according to which capacitors C_1 and C_2 are charged to $V_1 = (1 + nD)V_g$ and $V_2 = nDV_g$, respectively, during the S_2 conduction interval, while C_o is charged to $V_o = V_1 + V_2 + V_g + n(1-D)V_g$, during the S_1 conduction interval. Accordingly, the voltage gain results:

$$M = \frac{V_o}{V_g} = 2 + n(1 + D). \tag{4.6.2}$$

This expression reveals the previously mentioned topology limitation in terms of voltage gain variation capability, compared with Boost-based structures. Moreover, considering the constraints imposed by the desired converter operation according to Fig. 4.6.3, the duty-cycle variation is limited. This aspect is further clarified in Section 4.6.4.

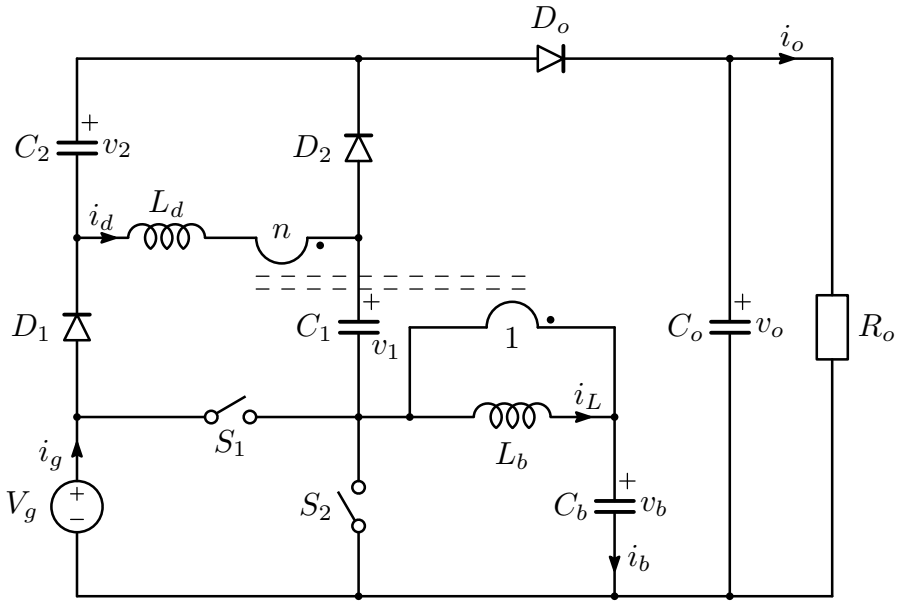


Figure 4.6.2: Proposed high step-up topology derived from Fig. 4.6.1b.

Once again, the *charge balance* condition at steady-state for the capacitors yields $\bar{i}_{Do} = \bar{i}_{D1} = \bar{i}_{D2} = \bar{i}_d = I_o$, and $\bar{i}_L = I_L = nI_o$. Thus, compared with an equivalent gain Boost converter, the average value of the coupled inductor magnetizing current is reduced by a factor $n/M \ll 1$.

4.6.2 Converter operation

In order to simplify the analysis let's neglect the magnetizing current ripple assuming $i_L(t) \approx I_L = nI_o$. The output voltage is also considered constant, i.e. $v_o(t) \approx V_o$. The converter operation is divided into four sub-intervals, described in Fig. 4.6.4.

– *Interval* $0 \leq t \leq t_1$ (see Fig. 4.6.4a). When the switch S_1 is turned on, a resonant tank is formed involving C_1, C_2, C_b, and L_d, with initial conditions $i_d(0) = 0$, $v_1(0) = V_{1p}$, $v_2(0) = V_{2p}$, $v_b(0) = V_{bv}$ (see Fig. 4.6.3). The simplified scheme is reported in Fig. 4.6.5, with the following parameters: $C_A = C_1C_2/(C_1 + C_2)$, $C_B = C_b/n^2$, $v_A(0) = v_B(0) = 0$, and $V_k = V_o - (n +$

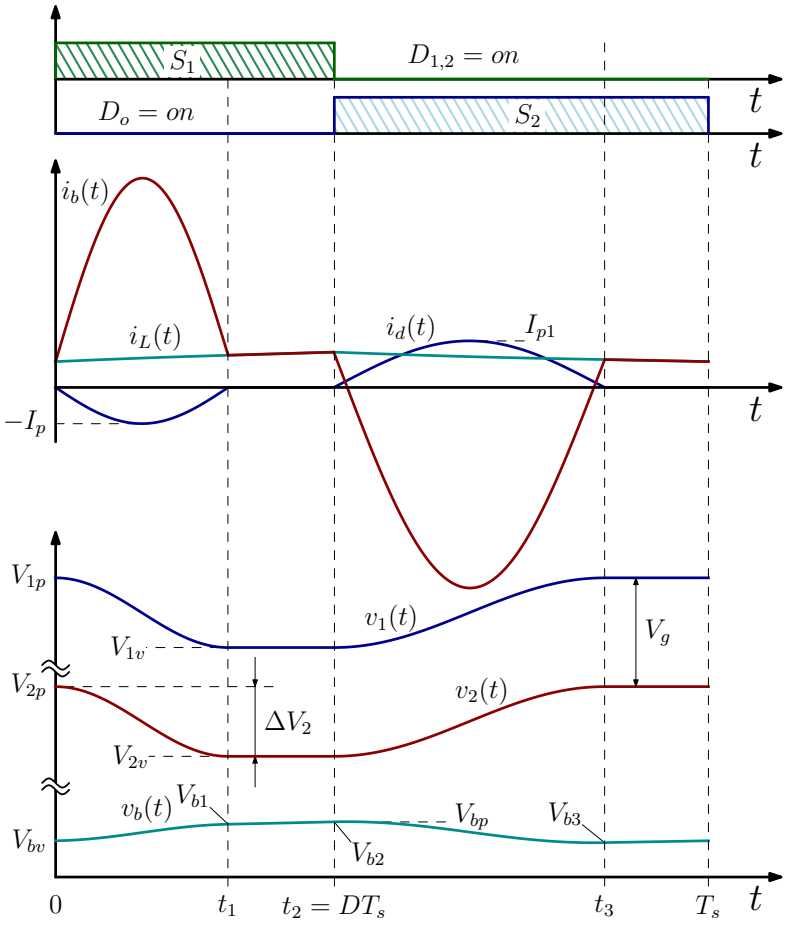


Figure 4.6.3: Main waveforms in a switching period.

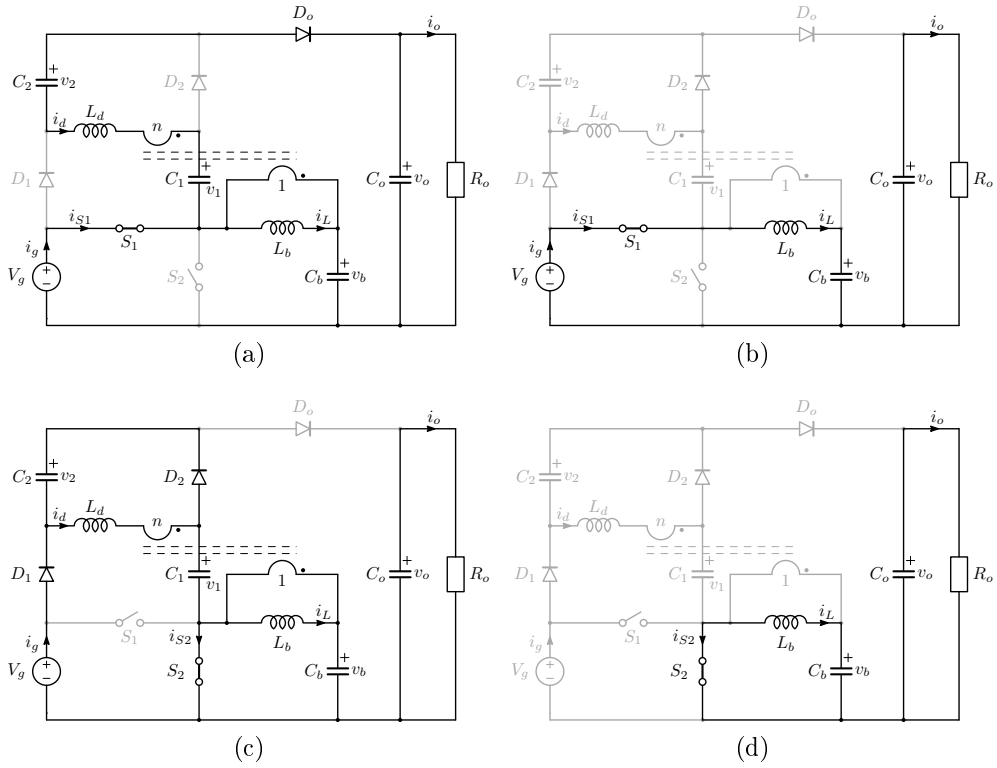


Figure 4.6.4: Sub-topologies in a switching period: (a) interval $0 \leq t \leq t_1$; (b) interval $t_1 \leq t \leq t_2 = DT_s$; (c) interval $t_2 \leq t \leq t_3$; (d) interval $t_3 \leq t \leq T_s$.

$1) V_g + nV_{bv} - V_{1p} - V_{2p}$. The resonant current and voltages are:

$$i_d(t) = \frac{V_k}{Z_r}\sin(\omega_r t) + \frac{n^2 C_r}{C_b} I_o \left(1 - \cos(\omega_r t)\right), \tag{4.6.3}$$

$$\begin{aligned} v_{1,2}(t) = {} & V_{1,2p} + \frac{C_r}{C_{1,2}} V_k \left(1 - \cos(\omega_r t)\right) + \\ & - \frac{n^2 C_r^2}{C_b C_{1,2}} Z_r I_o \sin(\omega_r t) + \frac{n^2 C_r}{C_b C_{1,2}} I_o t, \end{aligned} \tag{4.6.4}$$

$$\begin{aligned} v_b(t) = {} & V_{bv} - \frac{nC_r}{C_b} V_k \left(1 - \cos(\omega_r t)\right) + \\ & + \frac{n^3 C_r^2}{C_b^2} Z_r I_o \sin(\omega_r t) - \frac{nI_o}{C_b}\left(\frac{n^2 C_r}{C_b} - 1\right) t, \end{aligned} \tag{4.6.5}$$

where

$$C_r = \frac{1}{\dfrac{1}{C_1} + \dfrac{1}{C_2} + \dfrac{n^2}{C_b}}, \quad \omega_r = \frac{1}{\sqrt{L_d C_r}}, \quad Z_r = \sqrt{\frac{L_d}{C_r}}. \tag{4.6.6}$$

This phase ends at instant t_1 as soon as the resonant current $i_d(t)$ reaches zero, i.e. from (4.6.3):

$$t_1 = \frac{2}{\omega_r} \tan^{-1}\left(-\frac{V_k}{I_o}\frac{\omega_r C_b}{n^2}\right) \approx \frac{\pi}{\omega_r}. \tag{4.6.7}$$

In fact, as it will be clear later on, the *sine* term in (4.6.3) is dominant, thus making the interval duration practically equal to half the resonance frequency. Using such approximation, the resonant current peak value (I_p in Fig. 4.6.3) is approximated as:

$$I_p \approx -i_d\left(\frac{T_r}{4}\right) = -\frac{V_k}{Z_r} - \frac{n^2 C_r}{C_b} I_o. \tag{4.6.8}$$

Thus, approximately after half the resonant cycle, diode D_o turns off, and only the Buck stage remains operating, as shown in Fig. 4.6.4b.

– *Interval* $t_1 \le t \le t_2 = DT_s$ (see Fig. 4.6.4b). In the remaining part of the main switch on time, neglecting the magnetizing current ripple, the capacitor C_b continues to be charged almost linearly according to

$$v_b(t) = V_{b1} + \frac{nI_o}{C_b}(t - t_1), \tag{4.6.9}$$

where V_{b1} is the value reached at the end of the previous sub-interval, i.e. (4.6.5) calculated at $t = t_1$ (see Fig. 4.6.3). At the end of this sub-interval the voltage across C_b is $V_{b2} = V_{b1} + (nI_o/C_b)(t_2 - t_1)$.

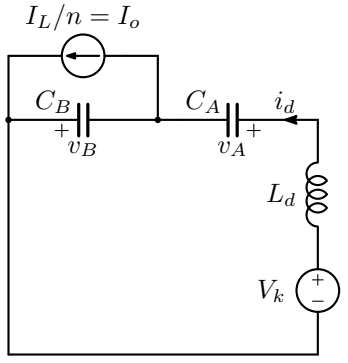


Figure 4.6.5: Simplified resonant circuit during intervals [0, t_1] and [t_2, t_3].

– *Interval* $DT_s \le t \le t_3$ (see Fig. 4.6.4c). In this interval S_2, D_1 and D_2 are conducting, thus recharging C_1 and C_2

in a resonant manner. The simplified circuit is the same as in Fig. 4.6.5, with different expressions for $C_A = C_1 + C_2$ and $V_{k1} = -V_{2v} + nV_{b2}$, while $C_B = C_b/n^2$ remains the same (now voltage V_k was renamed as V_{k1} to avoid confusion with the previous resonance phase). The resonant current and voltages are:

$$\begin{aligned} i_d(t) &= \frac{V_{k1}}{Z_{r1}} \sin(\omega_{r1}(t-t_2)) \\ &\quad + \frac{n^2 C_{r1}}{C_b} I_o \left(1 - \cos(\omega_{r1}(t-t_2))\right), \end{aligned} \tag{4.6.10}$$

$$\begin{aligned} v_{1,2}(t) &= V_{1,2v} + \frac{C_{r1}}{C_1 + C_2} V_{k1} \left(1 - \cos(\omega_{r1}(t-t_2))\right) + \\ &\quad - \frac{n^2 C_{r1}^2}{C_b(C_1 + C_2)} Z_{r1} I_o \sin(\omega_{r1}(t-t_2)) \\ &\quad + \frac{n^2 C_{r1}}{C_b(C_1 + C_2)} I_o (t - t_2), \end{aligned} \tag{4.6.11}$$

$$\begin{aligned} v_b(t) &= V_{b2} - \frac{nC_{r1}}{C_b} V_{k1} \left(1 - \cos(\omega_{r1}(t-t_2))\right) + \\ &\quad + \frac{n^3 C_{r1}^2}{C_b^2} Z_{r1} I_o \sin(\omega_{r1}(t-t_2)) \\ &\quad - \frac{nI_o}{C_b} \left(\frac{n^2 C_{r1}}{C_b} - 1\right) (t - t_2), \end{aligned} \tag{4.6.12}$$

where

$$C_{r1} = \frac{1}{\dfrac{1}{C_1 + C_2} + \dfrac{n^2}{C_b}}, \quad \omega_{r1} = \frac{1}{\sqrt{L_d C_{r1}}}, \quad Z_{r1} = \sqrt{\frac{L_d}{C_{r1}}}. \tag{4.6.13}$$

The turn off of diodes D_1 and D_2 at instant t_3 when the resonant current $i_d(t)$ goes to zero, concludes this phase. From (4.6.10), the interval duration is calculated as:

$$t_3 - t_2 = \frac{2}{\omega_{r1}} \left(\pi - \tan^{-1}\left(\frac{V_{k1}}{I_o} \frac{\omega_{r1} C_b}{n^2}\right)\right) \approx \frac{\pi}{\omega_{r1}}. \tag{4.6.14}$$

Once again, the *sine* term in (4.6.10) is dominant, and using this approximation, the resonant current peak value (I_{p1} in Fig. 4.6.3) simplifies as:

$$I_{p1} \approx i_d \left(t_2 + \frac{T_{r1}}{4}\right) = \frac{V_{k1}}{Z_{r1}} + \frac{n^2 C_{r1}}{C_b} I_o. \tag{4.6.15}$$

– *Interval* $t_3 \leq t \leq T_s$ (see Fig. 4.6.4d). In the last fraction of the switching period, the free-wheeling phase of the Buck sub-section continues, and capacitor C_b discharges according to the following relation

$$v_b(t) = V_{b3} - \frac{nI_o}{C_b}(t - t_3), \tag{4.6.16}$$

being V_{b3} the voltage at the end of the previous sub-interval (see Fig. 4.6.3).

4.6.3 Components current and voltage stress

In this section, the device voltage and current stresses are determined under the assumption of a negligible magnetizing current ripple. In order to estimate the current RMS values in different components, the following approximation of the resonant current was considered:

$$i_d(t) \approx \begin{cases} -I_p \sin(\omega_r t) & \text{for } 0 \leq t \leq t_1 \approx \dfrac{\pi}{\omega_r} \\ I_{p1} \sin(\omega_{r1}(t - t_2)) & \text{for } t_2 \leq t \leq t_3 \approx t_2 + \dfrac{\pi}{\omega_{r1}} \\ 0 & \text{otherwise} \end{cases} \tag{4.6.17}$$

– *Diode* D_o. This diode carries the resonant current $i_{Do}(t) = -i_d(t)$ during interval $[0, t_1]$. Consequently, its peak value is given by (4.6.8). Here, V_k can be estimated by observing that, for the capacitor *charge balance*, $\bar{i}_{Do} = I_o$. Thus, from (4.6.3), we have:

$$I_o = -\frac{1}{T_s}\int_0^{t_1} i_d(t)dt \quad \Rightarrow \quad V_k = -Z_r I_o \pi \left(\frac{T_s}{T_r} + \frac{n^2 C_r}{2C_b}\right). \tag{4.6.18}$$

As far as the diode voltage stress is concerned, from Fig. 4.6.4c we get:

$$V_{Do} = V_o - V_{1v} \approx V_o - \left(V_1 - \frac{\Delta V_1}{2}\right), \tag{4.6.19}$$

where the capacitor voltage variation ΔV_1 is calculated considering that the charge the capacitors C_1 and C_2 deliver to the output in a switching period is equal to the load current integrated over the switching period, i.e.:

$$\Delta V_{1,2} = \frac{I_o T_s}{C_{1,2}}. \tag{4.6.20}$$

Considering the approximation (4.6.17), the diode current RMS value is given by:

$$I_{Do_{\mathrm{RMS}}} = \frac{I_p}{2}\sqrt{\frac{T_r}{T_s}}. \tag{4.6.21}$$

– *Diodes* $D_{1,2}$. These devices conduct during interval $[t_2, t_3]$, where current $i_d(t)$ is shared between C_1 and C_2, i.e. $i_{D1,2}(t) = i_d(t)C_{1,2}/(C_1 + C_2)$. The diode current peak value in the charging phase is equal to $I_{p1}C_{1,2}/(C_1 + C_2)$. Once again, from the condition $\bar{i}_d = I_o$, an expression for V_{k1} in the interval $[t_2, t_3]$ is found:

$$V_{k1} = Z_{r1}I_o\pi\left(\frac{T_s}{T_{r1}} - \frac{n^2C_{r1}}{2C_b}\right). \tag{4.6.22}$$

The maximum diode voltage stress can be inferred from Fig. 4.6.4a, and results $V_{D1,2} = V_o - V_g - V_{2,1v} \approx V_o - V_g - \left(V_{2,1} - \dfrac{\Delta V_{2,1}}{2}\right)$. Considering the approximation (4.6.17), the diode current RMS value is given by:

$$I_{D1,2_{\mathrm{RMS}}} = \frac{I_{p1}}{2}\frac{C_{1,2}}{C_1 + C_2}\sqrt{\frac{T_{r1}}{T_s}}. \tag{4.6.23}$$

– *Switch* S_1. The current flowing into the main switch S_1, during interval $[0, t_2 = DT_s]$, from Fig. 4.6.4a, is $i_{S1}(t) = i_L(t) - (1+n)i_d(t) = i_{Cb}(t) - i_d(t)$. Thus, its peak value is given by $I_{S1_{pk}} = nI_o + (1+n)I_p$. The switch voltage stress is clearly given by the input voltage, while the switch RMS current value results:

$$I_{S1_{\mathrm{RMS}}} = I_o\sqrt{\frac{I_p}{I_o}\frac{n+1}{\omega_r T_s}\left(4n + (n+1)\frac{\pi}{2}\frac{I_p}{I_o}\right) + n^2 D}. \tag{4.6.24}$$

– *Switch* S_2. The instantaneous switch current, in the interval $[t_2 = DT_s, T_s]$, is given by $i_{S2}(t) = i_{C1}(t) - i_{Cb}(t) = -i_L(t) + (C_1/(C_1 + C_2) + n)i_d(t)$. Consequently, its peak value is calculated as $I_{S2_{pk}} = -nI_o + (C_1/(C_1 + C_2) + n)I_{p1}$. Like S_1, the voltage stress is given by the input voltage. Its RMS current value is calculated as:

$$I_{S2_{\mathrm{RMS}}} = I_o\sqrt{\frac{I_{p1}}{I_o}\frac{n+\xi}{\omega_{r1}T_s}\left(-4n + (n+\xi)\frac{\pi}{2}\frac{I_{p1}}{I_o}\right) + n^2(1-D)}, \tag{4.6.25}$$

where $\xi = C_1/(C_1 + C_2)$.

– *Capacitors* $C_{1,2}$. The RMS current value through C_1 and C_2 is totally determined by the resonant current. Considering the approximation (4.6.17), we obtain:

$$I_{C1,2_{\mathrm{RMS}}} = \sqrt{\frac{I_p^2}{2}\frac{T_r}{2T_s} + \frac{I_{p1}^2}{2}\frac{T_{r1}}{2T_s}\left(\frac{C_{1,2}}{C_1 + C_2}\right)^2}. \tag{4.6.26}$$

The maximum capacitor voltage is $V_{C1,2} \approx V_{1,2} + \Delta V_{1,2}/2$.

– *Capacitor* C_b. The current through capacitor C_b is $i_{Cb}(t) = i_L(t) - n i_d(t)$. Considering (4.6.17), we get:

$$I_{Cb_{\mathrm{RMS}}} = nI_o\sqrt{\frac{I_{p1}}{I_o}\frac{1}{\omega_{r1}T_s}\left(-4 + \frac{I_{p1}}{I_o}\frac{\pi}{2}\right) + \frac{I_p}{I_o}\frac{1}{\omega_r T_s}\left(4 + \frac{I_p}{I_o}\frac{\pi}{2}\right) + 1}. \tag{4.6.27}$$

The average voltage across the capacitor C_b is simply equal to $V_{Cb} = DV_g$.

– *Coupled inductor*. The coupled inductor primary winding carries the same current as C_b, while the secondary current RMS value is:

$$I_{d_{\mathrm{RMS}}} = \sqrt{\frac{I_p^2}{2}\frac{T_r}{2T_s} + \frac{I_{p1}^2}{2}\frac{T_{r1}}{2T_s}}. \tag{4.6.28}$$

4.6.4 Design constraints

In this section, guidelines for the selection of the main converter components are given. The considered specifications are listed in Table 4.8. In the following, we consider $C_1 = C_2 = C_x$.

– *Turns ratio n*. The main idea under the choice of the coupled inductor turns ratio is to guarantee the converter operation as described in the previous section, i.e. $t_1 < DT_s$, and $t_3 - t_2 < (1-D)T_s$. Considering the approximations (4.6.7) and (4.6.14), and taking into account the input voltage variation, we can write:

$$\frac{\pi}{\omega_r} \leq D_{\min} T_s \tag{4.6.29}$$

$$\frac{\pi}{\omega_{r1}} \leq (1 - D_{\max})\, T_s \tag{4.6.30}$$

Table 4.8: Converter specifications

Parameter	**Symbol**	**Value**	
Minimum input voltage	$V_{g_{min}}$	40	V
Nominal input voltage	$V_{g_{nom}}$	44	V
Maximum input voltage	$V_{g_{max}}$	48	V
Nominal output voltage	V_o	400	V
Nominal output power	P_o	300	W
Switching frequency	f_s	200	kHz

Considering the equal sign in (4.6.29) and (4.6.30) as boundary conditions, and taking the ratio we get:

$$\frac{1+\lambda}{1+4\lambda} = \left(\frac{D_{\min}}{1-D_{\max}}\right)^2, \tag{4.6.31}$$

where $\lambda = C_b/(2n^2C_x)$. Deriving parameter λ from the above equation, we get:

$$\lambda = \frac{1-\left(\dfrac{D_{\min}}{1-D_{\max}}\right)^2}{4\left(\dfrac{D_{\min}}{1-D_{\max}}\right)^2 - 1}, \tag{4.6.32}$$

Being λ positive, from (4.6.31) and (4.6.32) the condition $(1-D_{\max})/2 < D_{\min} < 1-D_{\max}$ must be satisfied. Thus, using (4.6.2), the following constraint is found:

$$n_{min} = \frac{M_{min}+M_{max}-4}{3} < n < n_{max} = \frac{2M_{min}+M_{max}-6}{4}. \tag{4.6.33}$$

The above relation reveals the mentioned limitation in terms of allowed input voltage range, since applying the condition $n_{min} \leq n_{max}$ yields the following constraint:

$$M_{max} \leq 2\left(M_{min}-1\right). \tag{4.6.34}$$

The selected value for n, from expression (4.6.33), is:

$$n = \frac{n_{min}+n_{max}}{2} = \frac{10M_{min}+7M_{max}-34}{24}. \tag{4.6.35}$$

– *Magnetizing inductance* L_b. Even if the above analysis considers a negligible Buck inductor current ripple, the latter has a modest effect on the converter voltage gain. On the other hand, a high inductor current ripple may have a beneficial effect in terms of inductor size and reduction of switching losses, especially if a *quasi-square-wave* operation is achieved (i.e. the current i_L is negative at the end of S_2 conduction interval). In this case, zero-voltage turn on of both switches is achieved, provided that the current value at the commutation instants is enough to completely charge/discharge the switching node capacitance. Please note that this soft-switching condition is independent of the resonant current i_d, since the latter is always zero at the commutation instants. By imposing this constraint and assuming a piece-wise linear current ripple, the following limit value is found:

$$L_{b_{max}} = \frac{V_o - (2+n)V_{g_{max}}}{2n^2 I_o f_s}. \tag{4.6.36}$$

A suitable margin should be considered in choosing an inductance value lower than the limit (4.6.36), considering that the voltage ripple on v_b may not be so negligible, a fact that would make the hypothesis of a piece-wise linear inductor current not well verified.

– *Leakage inductance* L_d. Instead of imposing a value for the coupled inductor leakage inductance, the value measured on the implemented transformer is used. This approach avoids the complexity of building a transformer with a precise value of the total leakage inductance. Clearly, this approach is allowed by the many degrees of freedom the topology has, as the two resonance frequencies ω_r and ω_{r1} are functions of five parameters, namely L_d, C_1, C_2, C_b, and n (see (4.6.6) and (4.6.13)). In any case, no particular winding arrangements are necessary, considering that a standard winding configuration with primary layers on top of the secondary layers, generates a leakage inductance in the range of few percent ($2 \div 10\%$) of the magnetizing one (referred to the same winding).

– *Capacitors* C_b *and* $C_x = C_1 = C_2$. From (4.6.32), parameter λ is calculated, and from (4.6.29) we get:

$$C_b = n^2 \frac{1+4\lambda}{L_d} \left(\frac{D_{min}}{\pi f_s} \right)^2. \tag{4.6.37}$$

Then, from λ definition, $C_1 = C_2 = C_b/(2n^2\lambda)$.

Table 4.9: Converter parameters

Parameter	**Symbol**	**Value**	
Primary turns number	N_p	3	
Secondary turns number	N_s	15	
Magnetizing inductance	L_b	3.7	µH
Secondary leakage inductance	L_d	4.3	µH
Flying capacitors	$C_1 = C_2$	100	nF
Buck capacitor	C_b	6×0.68	µF
Output capacitor	C_o	1	µF
Input capacitor	C_{in}	3×2.2	µF

Table 4.10: Calculated voltage and current stress at nominal operating point

Parameter	$\mathbf{D_o}$	$\mathbf{D_1}$	$\mathbf{D_2}$	$\mathbf{S_1}$	$\mathbf{S_2}$	$\mathbf{C_1}$	$\mathbf{C_2}$	$\mathbf{C_b}$	$\mathbf{C_{in}}$
I_{peak} [A]	4.72	4.72	4.72	32	21	4.72	4.72	27.3	32
I_{RMS} [A]	1.68	0.98	0.98	11.9	8.9	1.95	1.95	13	12
V_{stress} [V]	281	281	237	44	44	155	111	18.5	44

4.6.5 Prototype design and experimental results

In order to verify the above theoretical analysis and the performance of the proposed high step-up topology, a prototype was designed and built according to the specifications listed in Table 4.8. The active devices are: $S_1 = S_2 =$ IPB010N06N (60 V, 180 A) from Infineon®, $D_1 = D_2 =$ IDD03SG60C from Infineon®, $D_o =$ C3D03060E from Cree®. The SiC diodes have been used just for their immediate availability in the lab, even if their voltage rating is much higher than needed.

From (4.6.33), being $8.33 \leq M \leq 10$, the transformer turns ratio n should be selected in the range $4.78 \div 5.17$; thus, $n = 5$ was chosen. The maximum magnetizing inductance value to guarantee *quasi-square-wave* operation from (4.6.36) is 8.5 µH, and the selected value was much lower in order to have enough negative current at S_2 turn off to charge the parasitic capacitance of the switching node up to the input voltage before S_1 is turned on. The value measured at primary side on the wounded RM10 core was $L_b = 3.74$ µH. The total secondary leakage inductance is $L_d = 4.3$ µH. Once this value

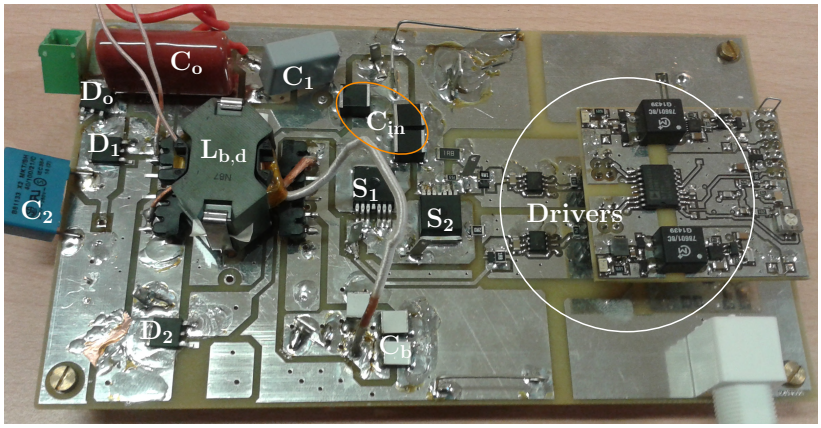


Figure 4.6.6: Photo of the prototype showing the main components.

is referred to the primary side, it gives a leakage-to-magnetizing inductance ratio of 4.65%. The primary winding layer consists of three turns of Litz wire (400 strands of 71 µm diameter) positioned on top of a two-layers secondary winding, made by 15 turns of Litz wire (200 strands of 50µm diameter). Like any inductor carrying a non-zero average current, also the coupled inductor used in this topology needs a suitable air-gap that, in the used RM10 core has a thickness of 150 µm, in both central and lateral legs. From (4.6.32), parameter λ is equal to 0.714; consequently, from (4.6.37), C_b should be 4 µF. Considering the high RMS current flowing in this capacitance that, based on (4.6.27) was estimated equal to 13 A, six 0.68 µF film capacitors were connected in parallel. Finally, from λ definition, $C_{1,2}$ should be 114 nF, and the standard 100 nF value was used. The input capacitor is $C_{in} = 3 \times 2.2$ µF, while the output one is $C_o = 1$ µF. All converter parameter values are listed in Table 4.9. With the selected component values, the calculated current and voltage stress at the nominal operating point, using the expressions developed in section 4.6.3, are listed in Table 4.10. The photo of the implemented prototype is reported in Fig. 4.6.6 and it shows the main active and passive components.

The converter main waveforms at two different input voltage values and for nominal output voltage and power are reported in Fig. 4.6.7. Please note that, despite the currents in the switches are not directly measured, the relative information can be easily gathered from the displayed waveforms since $i_{S1}(t) = i_{Cb}(t) - i_{C1}(t)$, during interval $[0, t_2 = DT_s]$, while $i_{S2}(t) =$

$i_{C1}(t) - i_{Cb}(t)$, during interval $[t_2 = DT_s, T_s]$. Looking at these experimental waveforms we can highlight two main aspects. The first one has to do with the delay between the S_1 turn-off instant and the instant C_1 starts to be charged: this is due to the different charging current paths the resonant current $i_d(t)$ divides in, one involving C_1, D_1, S_2, and C_{in}, and the other involving just C_2, and D_2. It happens that, when S_2 turns on, D_1 and D_2 turn on at different instants (D_2 first), so that, at the beginning, the resonance involves just C_2, and only when D_1 turns on, also C_1 comes into play. This phenomenon is better appreciated looking at the measures shown in Fig. 4.6.8, taken at nominal conditions, that reports the flying capacitor voltages $v_{C1}(t)$ and $v_{C2}(t)$: in this operating point, the delay is about 380 ns.

The second consideration is that at the minimum input voltage the condition $T_{r1}/2 < (1 - D_{max})T_s$ is not met, as revealed by the current waveforms in Fig. 4.6.7a taken at $V_g = 42\,\mathrm{V}$. This is caused by four main factors: the aforementioned double resonance, that affects the $t_3 - t_2$ interval, the high magnetizing current ripple that affects the overall voltage gain, the non unity converter efficiency, and the input voltage ripple ($\Delta V_g = 2.8\,\mathrm{V}$) both calling for a higher duty-cycle value compared with the theoretical one. Being the design done considering boundary equations, it cannot cope with any deviation from the theoretical analysis. Nonetheless, violating the condition (4.6.30), does not cause any harm to the converter operation, being the diode current rate of change always limited by the transformer leakage inductance L_d. This remains true also for low duty-cycle values where condition (4.6.29) might not be satisfied. In this case, another topological state appears with a higher rate of change of current $i_d(t)$, as can be seen from the measure taken at $V_g = 52\,\mathrm{V}$ ($P_o = 160\,\mathrm{W}$) reported in Fig. 4.6.10.

The S_2 gate-to-source and drain-to-source voltages shown in Fig. 4.6.7 demonstrate that the ZVS condition at turn on is always satisfied for S_2, and almost satisfied for S_1. In any case, the switching node voltage appears clean and ringing free. At reduced output power, the converter enters deeply into *quasi-square-wave* operation, thus guaranteeing ZVS commutations even at light load. This is demonstrated by the measure shown in Fig. 4.6.11 that was taken at 40 W of output power ($V_g = 44\,\mathrm{V}$, $V_o = 400\,\mathrm{V}$). The comparison between some calculated quantities and the corresponding measured values is shown in Table 4.11: despite the rough approximations used in the analysis the matching is quite good, the main discrepancy caused by the higher

duty-cycle value of the experimental setup (see comments above). Note that the peak current value in the switches is over-estimated for S_1 and under-estimated for S_2. This is due to the constant magnetizing current i_L assumed in the analysis, opposed to the designed high current ripple ($\Delta i_{L_{pk-pk}} > 2\bar{i}_L$) for *quasi-square-wave* operation.

The comparison between measured and theoretical duty-cycle as a function of the voltage conversion ratio at nominal output voltage and power, is shown in Fig. 4.6.9. As we can see, the measured behaviour follows the theoretical expectation from (4.6.2), except for a translation to higher values due to the circuit losses. The last point corresponding to the minimum input voltage (maximum voltage gain) tends to deviate from the linear behaviour predicted by (4.6.2) because of the different operating condition mentioned above (i.e. $T_{r1}/2 > (1 - D_{max})T_s$).

The conversion efficiency (power stage only) was calculated measuring input and output powers using digital multimeters (Keysight 34461A), for input/output voltages and output current, while the input current was read directly on the DC power supply Chroma 62050P-100-100. The overall relative error on the efficiency calculation is lower than 0.5%, the main contribution coming from the input current measurement (0.1% of reading plus 0.1% of range). The measured efficiency at different input voltage values and for two different power levels is shown in Fig. 4.6.12: values above 95% are achieved at nominal power except at the lower part of the input voltage range ($V_g = 42\,\mathrm{V}$). Here, the slight efficiency reduction is caused by the different operating condition mentioned above according to which $T_{r1}/2 > (1 - D_{max})T_s$, that is causing an increase of S_1 turn-on losses, as revealed by the $v_{DS2}(t)$ waveform in Fig. 4.6.7a. At lower output current values, the efficiency remains above 90% down approximately to one tenth of the nominal power, as revealed by the measurement reported in Fig. 4.6.13 for two different input voltage values ($V_g = 44\,\mathrm{V}$ and $V_g = 48\,\mathrm{V}$). The relative losses distribution between the different components was calculated based on the stress analysis reported in Section 4.6.3 at the nominal operating point, and the result is shown in Fig. 4.6.14. The total power loss was estimated as $P_{Loss}^{Estimated} = 10\,\mathrm{W}$, lower than the measured one $P_{Loss}^{Measured} = 15.8\,\mathrm{W}$. As we can see, turn-off switching losses have been considered too, even if the commutation time intervals are very difficult to predict. This is because the switching node transition is affected by the huge MOSFET's output capacitance (roughly $3.4\,\mathrm{nF}$ each), that acts as a loss-less snubber, especially at the S_2 turn off,

Table 4.11: Comparison between theoretical expectations and experimental results at the nominal operating point

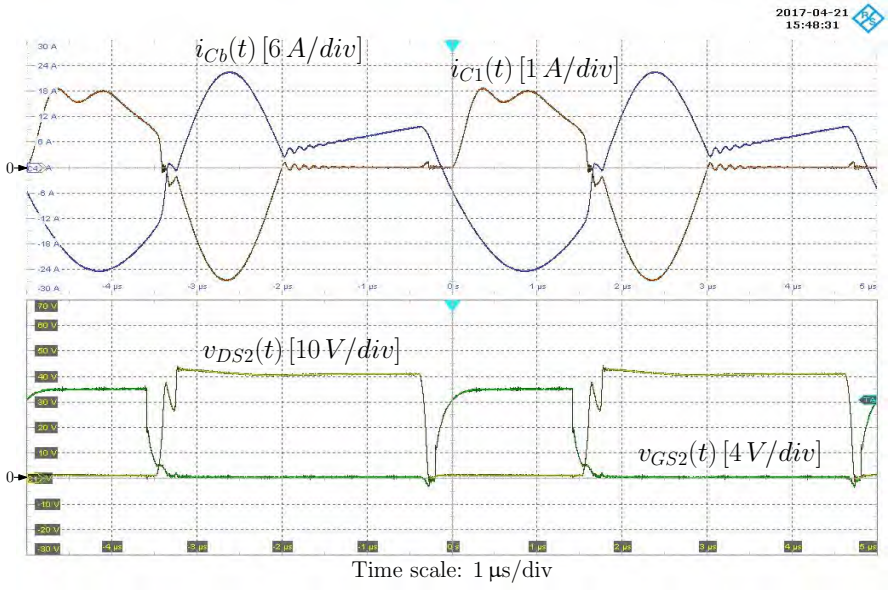
	D	$\mathbf{V_{1v}}$ [V]	$\mathbf{V_{1p}}$ [V]	$\mathbf{V_{2v}}$ [V]	$\mathbf{V_{2p}}$ [V]	$\mathbf{I_p}$ [A]	$\mathbf{I_{p1}}$ [A]	$\mathbf{I_{S1_p}}$ [A]	$\mathbf{I_{S2_p}}$ [A]
Theory	0.42	117	155	73	111	4.72	4.45	32	21
Measure	0.5	126	165	77	121	5.2	4.69	29	24

where the switched current is quite low ($\approx -2.5\,\mathrm{A}$ from Fig. 4.6.8). However, the forecasted total S_1 losses of $1.37\,\mathrm{W}$ are not unrealistic, since the temperature measured on the device package in the same operating point was $83°C$ without forced air circulation (ambient temperature $T_A \approx 20°C$). With a thermal resistance from junction to ambient of the TO263-7 package ranging between $40\,K/W$ with $6\,cm^2$ of cooling area and $62\,K/W$ with minimal footprint, it means a dissipated power in the range $1 \div 1.6\,\mathrm{W}$. Turn-on switching losses have been neglected for both switches, thanks to the *quasi-square-wave* operation imposed by a proper selection of the magnetizing inductance L_b, even if this condition is not completely met for S_1, as can be inferred from the rising edge of voltage $v_{DS2}(t)$ in Fig. 4.6.7b. However, the small switched current and residual voltage ($\approx 10\,\mathrm{V}$), give a negligible contribution to the overall losses. The core loss was estimated based on the manufacturer data of the used N87 ferrite material. The high RMS current value flowing in the devices, which is the price to pay for having the minimum switch voltage stress, makes the control of any parasitic resistance in the current path crucial in order to limit the conduction losses. This is the reason why the input and the buck stage capacitances were implemented by connecting in parallel more lower value capacitors, as revealed in table II. For the same reasons, the SiC diodes used in the experimental prototype are not the best choice for this circuit, where they are naturally turned off by the resonant current i_d. Looking at their voltage stress (see table III), lower voltage rating and, consequently, lower voltage drop Si devices could be used for a better overall efficiency.

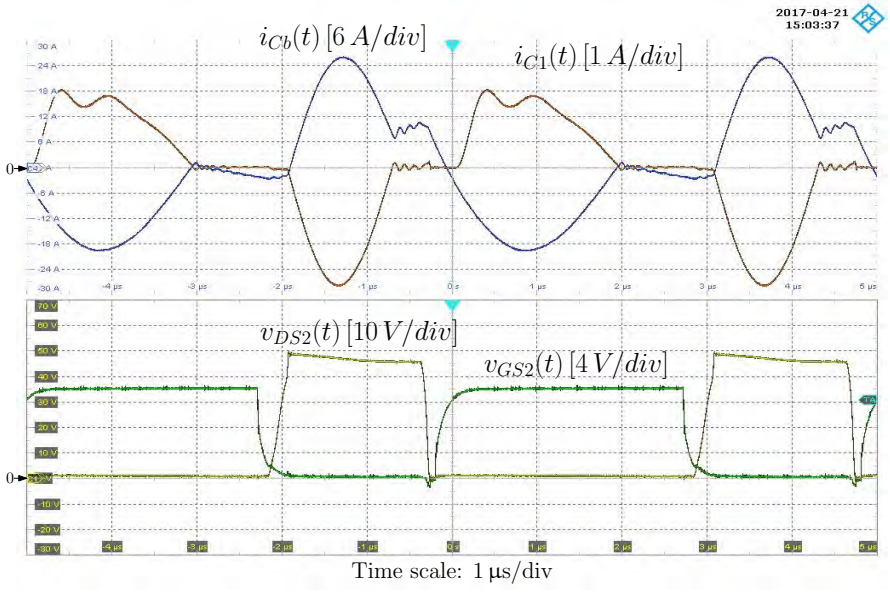
4.6.6 Conclusions

This Ph.D. dissertation presented a high step-up topology featuring minimum switch voltage stress as well as reduced magnetic energy, compared with an equivalent gain conventional Boost converter. The conversion process explores both a magnetic coupling and a charge pump mechanism to efficiently transfer energy to the output. The leakage inductance of the coupled inductors is explored to shape the capacitor charging/discharging current so as to achieve soft diode commutations.

A detailed design procedure was described to easily calculate the needed passive component values. The *quasi-square-wave* operation allows ZVS turn on of all switches. Experimental results taken on a 300 W prototype confirmed the theoretical analysis and expectations.



(a)



(b)

Figure 4.6.7: Measured converter main waveforms at nominal output voltage and power: (a) $V_g = 42\,\mathrm{V}$; (b) $V_g = 48\,\mathrm{V}$.

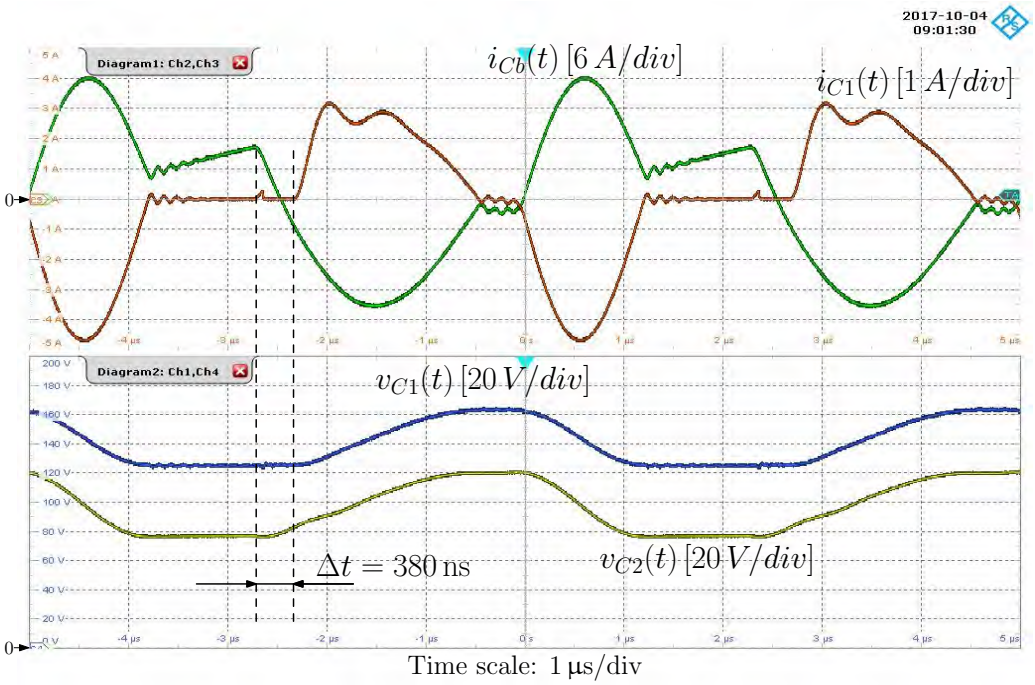


Figure 4.6.8: Measured converter main waveforms at nominal condition showing the delay between the S_1 turn-off instant and the instant C_1 starts to be charged.

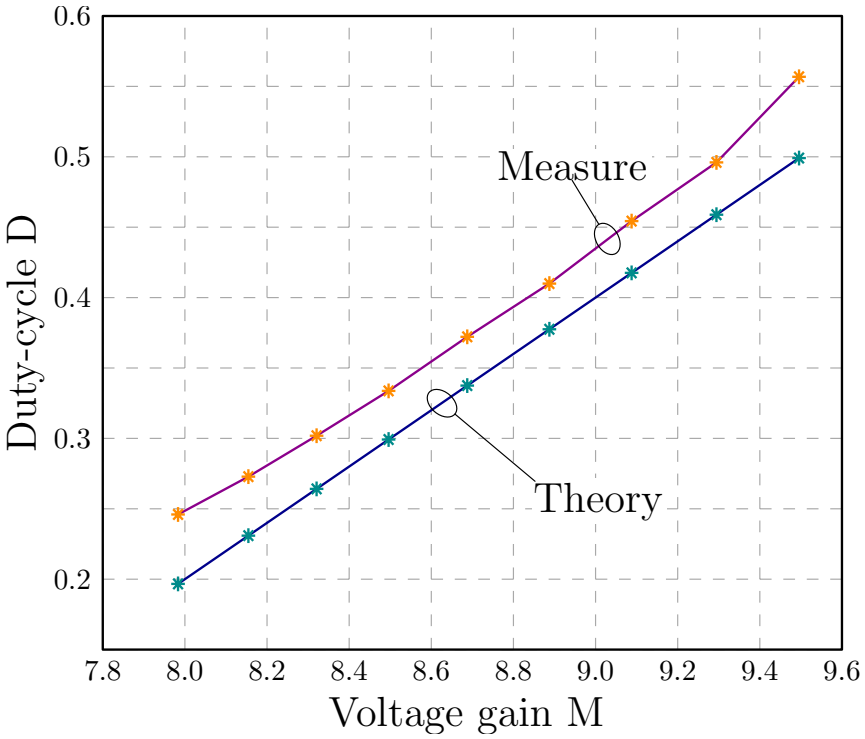


Figure 4.6.9: Comparison between measured and theoretical duty-cycle as a function of the voltage conversion ratio (nominal output voltage and power).

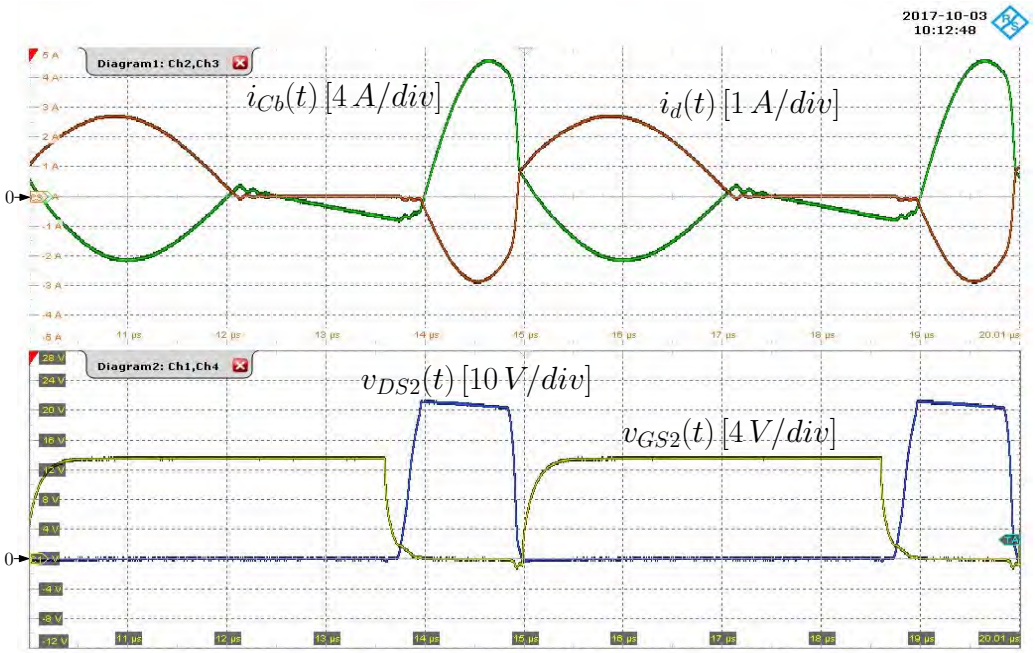


Figure 4.6.10: Measured converter main waveforms at $V_g = 52\,\mathrm{V}$ and nominal output voltage and 160 W of output power.

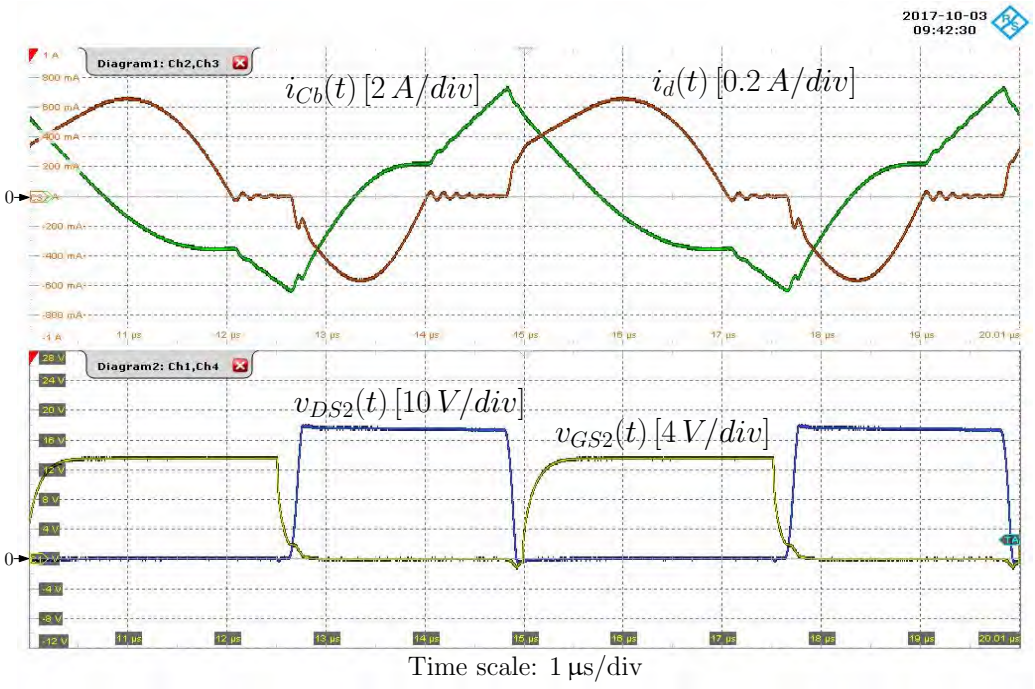


Figure 4.6.11: Measured converter main waveforms at nominal input and output voltages and 40 W of output power.

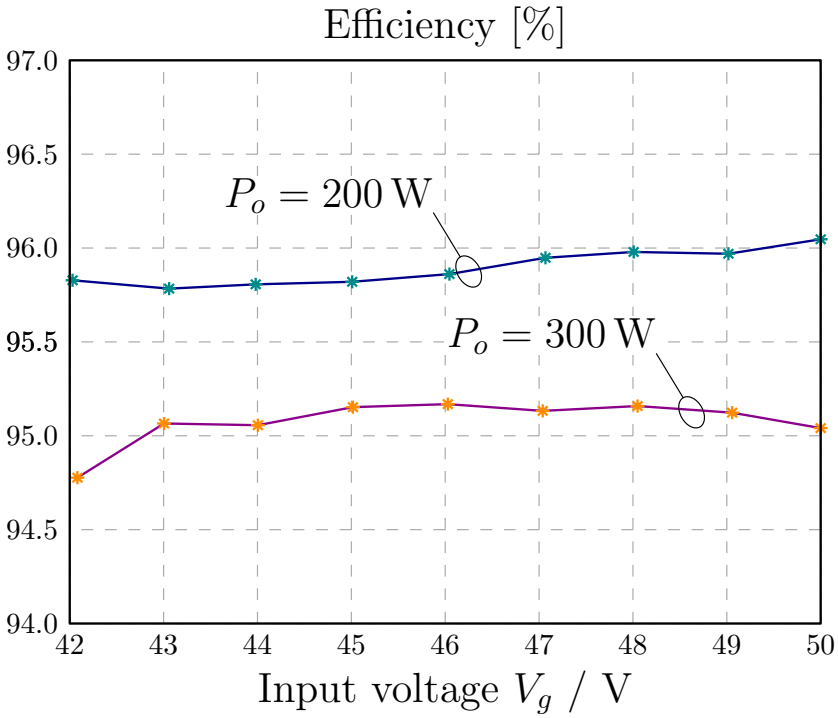


Figure 4.6.12: Conversion efficiency as a function of input voltage for two different output power levels.

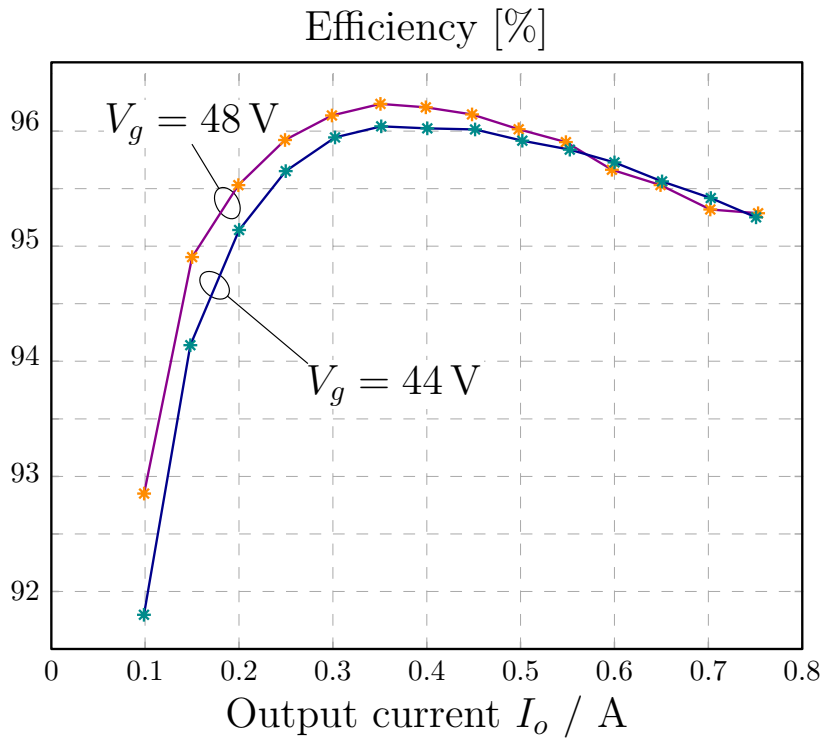


Figure 4.6.13: Conversion efficiency as a function of the output current for two different input voltage values.

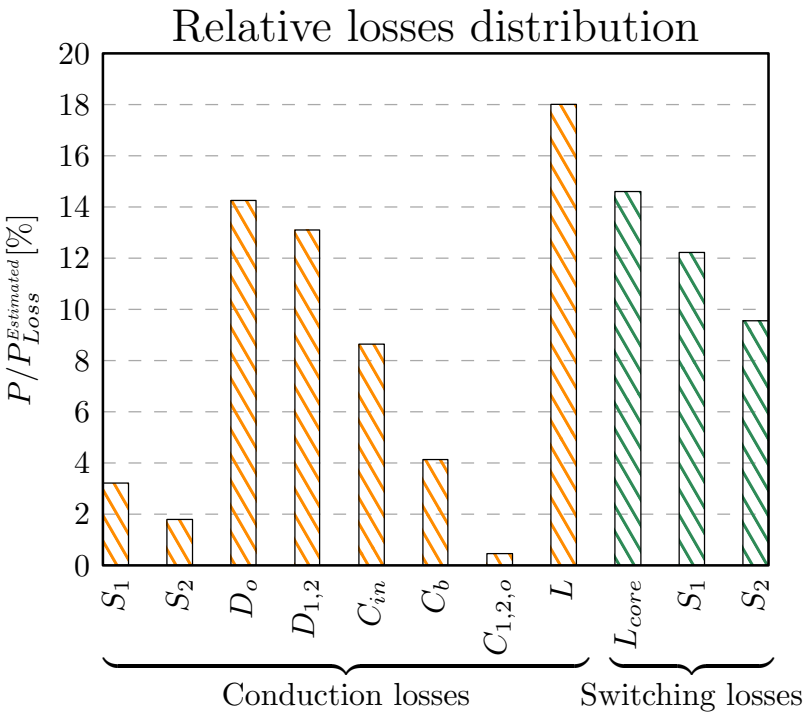


Figure 4.6.14: Calculated relative losses distribution among the main components (estimated overall losses at nominal condition $P_{Loss}^{Estimated} \approx 10\,\mathrm{W}$). Notation $D_{1,2}$ means the sum of D_1 and D_2 conduction losses, while $C_{1,2,o}$ means the sum of C_1, C_2 and C_o conduction losses.

4.7 Reconfigurable Three Switches Hybrid Step-Down Converter

While most of the effort of this PhD thesis has been focused on step-up topologies, hybrid topologies can be an interesting choice for step-down applications too, allowing a reduction of the average inductor current and lower conversion ratios at the same duty-cycle if compared to a standard buck converter. In this section a step-down converter combining hybridization with reconfigurability is presented (Fig.4.7.1). This topology employs three switches and one switched-capacitor cell to obtain four different possible operating modes, including a step-down implementation of the KY converter [4] and the standard buck operation. The desired operating mode can be chosen simply by changing the switches modulation law.

4.7.1 Operating Modes and Characteristics

4.7.1.1 Mode 1

In the so called "Mode 1" operation, the switches operation is synchronous, in fact they are all conducting during the converter ON-phase. The resulting equivalent circuit during this topological phase is shown in Fig.4.7.2.

As it is possible to see, in this phase capacitor C_f is charged to v_o while the inductor is also charged and its voltage v_L is equal to $V_{in} - v_o$. Observing the equivalent circuit it is straightforward to estimate the diodes voltage stress, that is equal to V_{in} in the case of D_1, while it is v_o in D_2 case.

In the OFF-phase instead (Fig.4.7.3), the switches are turned OFF and the inductor current flows onto the diodes.

In this phase the inductor is discharged and, neglecting the diodes voltage drop, its voltage is equal to $-v_o - v_1 = -2v_o$. The switches voltage stress is equal to V_{in} for S_1, while it is v_o for both S_2 and S_3. Knowing the inductor voltage in both phases, under the hypothesis of steady-state operation and (as previously mentioned) neglecting the diodes voltage drop, the conversion ratio can be estimated as

$$M = \frac{V_o}{V_{in}} = \frac{D}{2 - D}$$

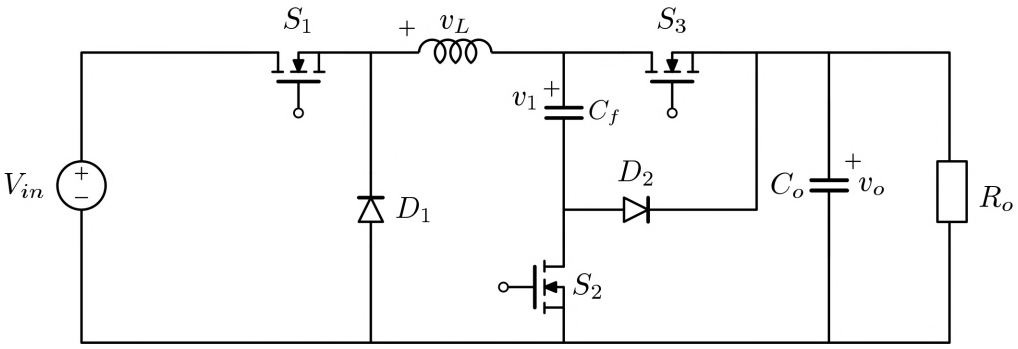


Figure 4.7.1: Reconfigurable three switches hybrid step-down converter schematic.

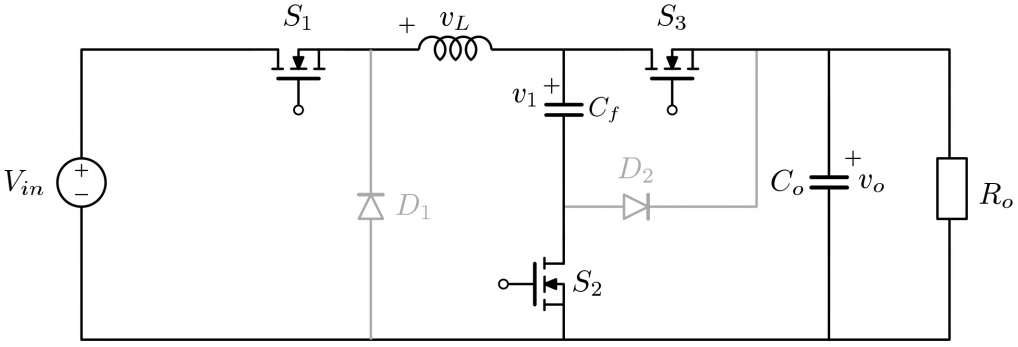


Figure 4.7.2: Reconfigurable three switches hybrid step-down converter: Mode 1 ON-Phase equivalent circuit.

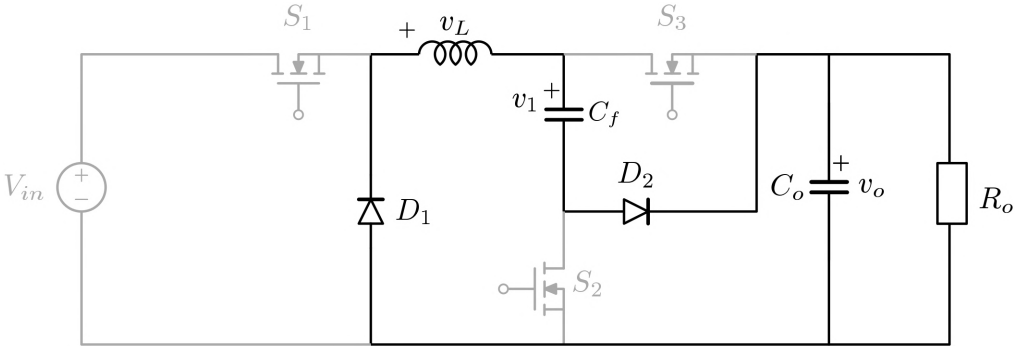


Figure 4.7.3: Reconfigurable three switches hybrid step-down converter: Mode 1 OFF-Phase equivalent circuit.

Observing Fig.4.7.2 and 4.7.3 we can also estimate the average inductor current. The average input current can be in fact written as $I_{in} = I_{S_1}$, but knowing that i_{s_1} is equal to i_L during the ON-Phase and zero during the OFF-Phase, the average current that flows on S_1 can be estimated as

$$I_{S_1} = DI_L$$

Deriving the expression of the duty cycle D as a function of the conversion ratio and substituting it in the previous equation yields

$$I_{in} = I_{S_1} = \left(\frac{2M}{1+M}\right) I_L$$

Under unity efficiency hypothesis we can write the previous equation as

$$MI_o = \left(\frac{2M}{1+M}\right) I_L$$

thus obtaining the average inductor current as a function of the average load current:

$$I_L = \left(\frac{M+1}{2}\right) I_o$$

Knowing the inductor voltage v_L in both topological states we can also estimate the inductor current ripple. We can in fact write

$$\Delta i_L = \frac{D\left(V_{in} - v_o\right)}{Lf_s}$$

Once again writing the duty cycle as a function of the conversion ratio we can derive the following equation:

$$\Delta i_L = 2M \left(\frac{1-M}{1+M}\right) \frac{V_{in}}{Lf_s}$$

4.7.1.2 Mode 2

In the so called "Mode 2" operating mode S_2 and S_3 are OFF during the ON-Phase, thus forcing the inductor current to flow onto D_2, while S_1 is

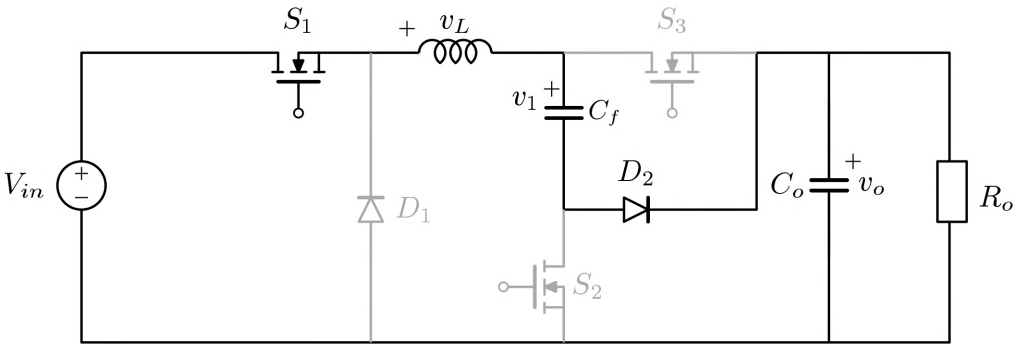


Figure 4.7.4: Reconfigurable three switches hybrid step-down converter: Mode 2 ON-Phase equivalent circuit.

turned ON. Observing the converter equivalent circuit in this phase, shown in Fig.4.7.4., it is possible to estimate the inductor voltage v_L, that is equal to $V_{in} - v_1 - v_o$. Therefore, since as it will be shown later, $v_1 = v_o$, we find that v_L is equal to $V_{in} - 2v_o$. The switching devices voltage stress is then equal to v_o in S_2 and S_3 case (neglecting the diode voltage drop), while it is V_{in} in D_1 case.

The OFF-phase equivalent circuit is shown in Fig.4.7.5. During this phase S_1 is turned OFF and the inductor current flows onto D_1. Switches S_2 and S_3 are turned ON and the capacitor C_f is connected in parallel with the output, thus giving $v_1 = v_o$ as previously mentioned. The inductor is discharged and its voltage v_L is equal to $-v_o$. The switching devices voltage stress, neglecting the diode voltage drop, is equal to V_{in} in S_1 case, while it is v_o for D_2.

Knowing the inductor voltage in both topological states, under steady-state operation hypothesis and neglecting the diodes voltage drop, it is possible to estimate the conversion ratio as

$$M = \frac{V_o}{V_{in}} = \frac{D}{1+D}$$

Observing the topology schematic we can also estimate the average inductor current. As previously observed, the average input current can be in fact written as $I_{in} = I_{S_1}$, but knowing that $i_{s_1} = i_L$ during the ON-Phase and zero during the OFF-Phase, the average current that flows on S_1 can be

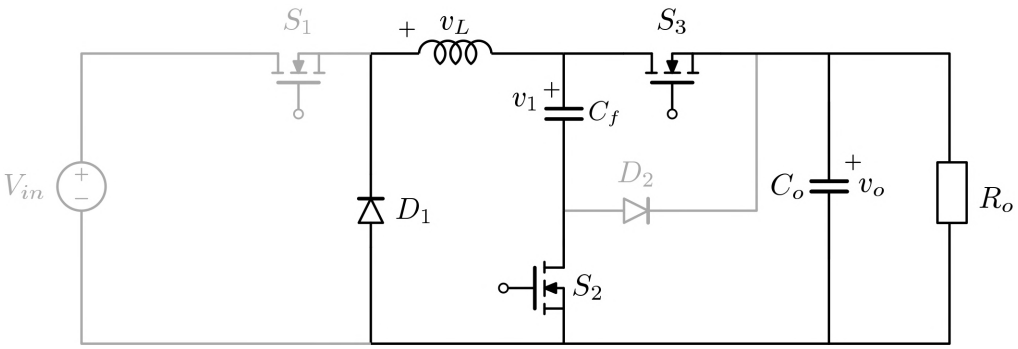


Figure 4.7.5: Reconfigurable three switches hybrid step-down converter: Mode 2 OFF-Phase equivalent circuit.

estimated as

$$I_{S_1} = DI_L$$

Deriving the expression of the duty cycle D as a function of the conversion ratio and substituting it in the previous equation yields

$$I_{in} = I_{S_1} = \left(\frac{M}{1-M}\right) I_L$$

Under unity efficiency hypothesis we can write the previous equation as

$$MI_o = \left(\frac{M}{1-M}\right) I_L$$

thus obtaining the average inductor current as a function of the average load current:

$$I_{L=} (1-M)\, I_o$$

Observing Fig.4.7.5 it is also possible to estimate the inductor current ripple. It is in fact possible to write

$$\Delta i_L = \frac{D\,(V_{in} - 2v_o)}{Lf_s}$$

Once again writing the duty cycle as a function of the conversion ratio we can derive the inductor current ripple expression as a function of the conversion ratio M and the input voltage V_{in}, obtaining the following equation:

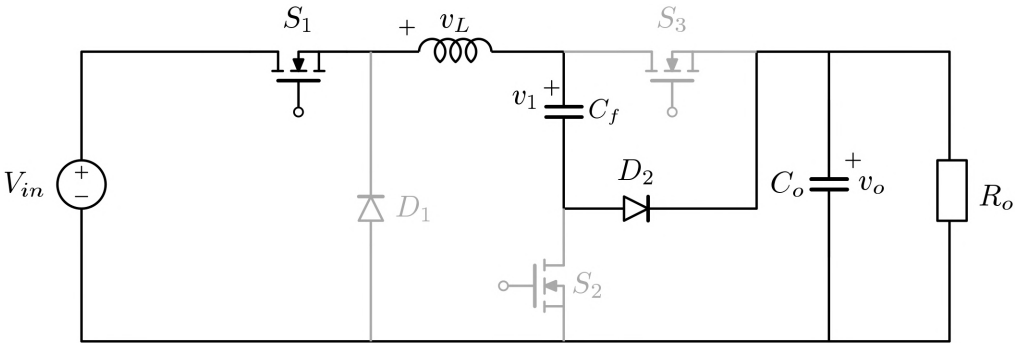


Figure 4.7.6: Reconfigurable three switches hybrid step-down converter: step-down KY operation ON-Phase equivalent circuit.

$$\Delta i_L = M\left(\frac{1-2M}{1-M}\right)\frac{V_{in}}{Lf_s}$$

4.7.1.3 Step-Down KY Operation

In the third possible hybrid operating mode the topology implements a step-down version of the KY converter [4]. In this operating mode switch S_1 is constantly ON, D_1 is constantly OFF, while the switches S_2 and S_3 are synchronous, both conducting in the OFF-Phase.

The ON-phase equivalent circuit is shown in Fig.4.7.6. As previously said switches S_2 and S_3 are OFF thus forcing the inductor current to flow on D_2; the inductor voltage v_L in this phase is equal to $V_{in} - v_o - v_1$. Knowing that, as it will be shown later, $v_1 = v_o$, we can then estimate $v_L = V_{in} - 2v_o$. The switching devices voltage stress is V_{in} in the case of D_1, while (neglecting the diodes voltage drop) it is v_o in S_2 and S_3 case.

The OFF-phase equivalent circuit is instead shown in Fig.4.7.7. In this phase the inductor is charged and its voltage v_L is equal to $V_{in} - v_o$. Since in this phase switches S_2 and S_3 are turned ON, the flying capacitor C_f is connected in parallel with the output capacitor C_o, thus giving $v_1 = v_o$ as previously mentioned. The diodes voltage stress can be estimated as V_{in} in D_1 case, while it is v_o in D_2 case.

Knowing the inductor voltage in both operating phases, under steady-state operation hypothesis and neglecting the diodes voltage drop, the conversion ratio can be estimated as:

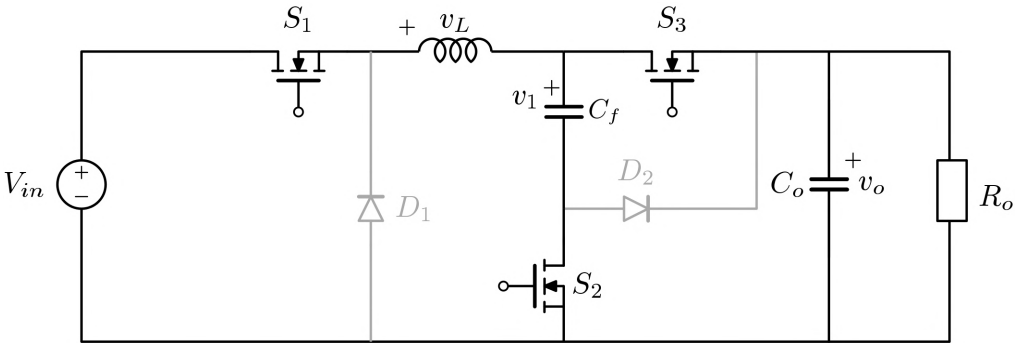


Figure 4.7.7: Reconfigurable three switches hybrid step-down converter: step-down KY operation OFF-Phase equivalent circuit.

$$M = \frac{V_o}{V_{in}} = \frac{1}{2 - D}$$

Observing the converter equivalent circuits in this operating mode it is also possible to estimate the inductor current average value and ripple. Since $S_1$is always ON, it is in fact possible to write

$$I_L = I_{in}$$

being I_{in} the average input current. Under unity efficiency hypothesis it is then straightforward to derive

$$I_L = MI_o$$

Looking at Fig.4.7.7 we can instead write for the inductor current ripple the following equation

$$\Delta i_L = \frac{(1 - D)\,(V_{in} - v_o)}{Lf_s}$$

Writing the duty cycle as a function of the conversion ratio, it is possible to derive the inductor current ripple expression as a function of the conversion ratio M and the input voltage V_{in}, obtaining the following equation:

$$\Delta i_L = \frac{(2M - 1)\,(1 - M)}{M} \frac{V_{in}}{Lf_s}$$

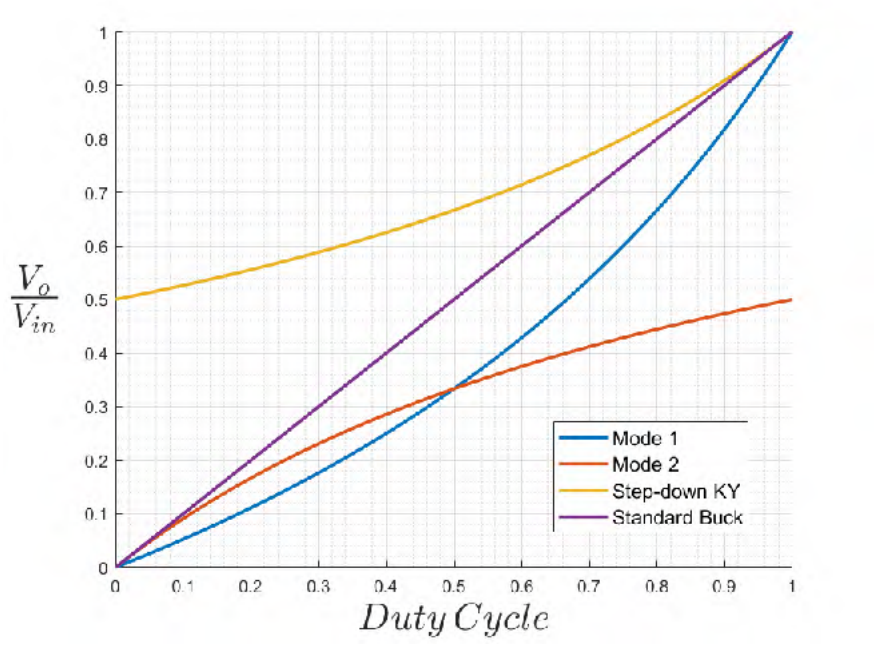


Figure 4.7.8: Reconfigurable three switches hybrid step-down converter attainable conversion ratios as a function of the duty cycle.

4.7.2 Characteristics Resume

A complete view of the attainable conversion ratios as a function of the duty cycle is shown in Fig.4.7.8. As it is possible to see, operating mode 1 yields all the conversion ratios in between 0 and 1, while mode 2 is limited to a maximum of 0.5 and the step-down KY has a minimum conversion ratio of 0.5. It is also important to notice how, with the same duty cycle value, mode 2 and especially mode 1 yield a lower conversion ratio if compared to the standard buck operation. Nevertheless, it must be noticed that, by using a charge-pump cell, it is likely that extremely high or low duty cycle values would cause a significant drop in efficiency, limiting in practice the range of attainable conversion ratios.

Figures 4.7.9 and 4.7.10 show the inductor current average value and ripple in comparison with an equivalent standard buck converter. As it is possible to see, the hybrid topology allows a reduction of both the average inductor current and inductor current ripple in all operating regimes except Mode

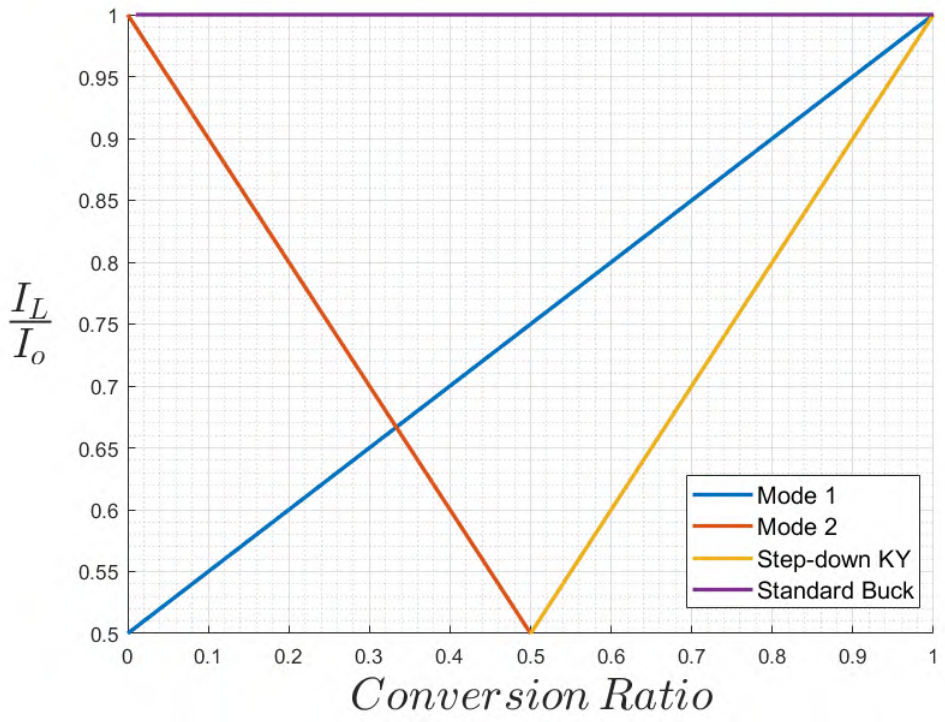


Figure 4.7.9: Reconfigurable three switches hybrid step-down converter average inductor current normalized to the average load current. Comparison with an equivalent standard buck case.

1, that is characterized by a higher inductor current ripple. Nevertheless it must be noted that this characteristic may potentially not be a major problem; it could be in fact exploited to obtain quasi-square wave operation in a synchronous implementation of the proposed topology, targeting for example applications requesting very low output voltage values.

4.7.3 Conclusions

The proposed topology shows some interesting characteristics. Reconfigurability allows a complete set of step-down conversion ratios and the use of a hybrid converter approach allows for the reduction of the average inductor current in comparison with a standard buck converter. The reasonable

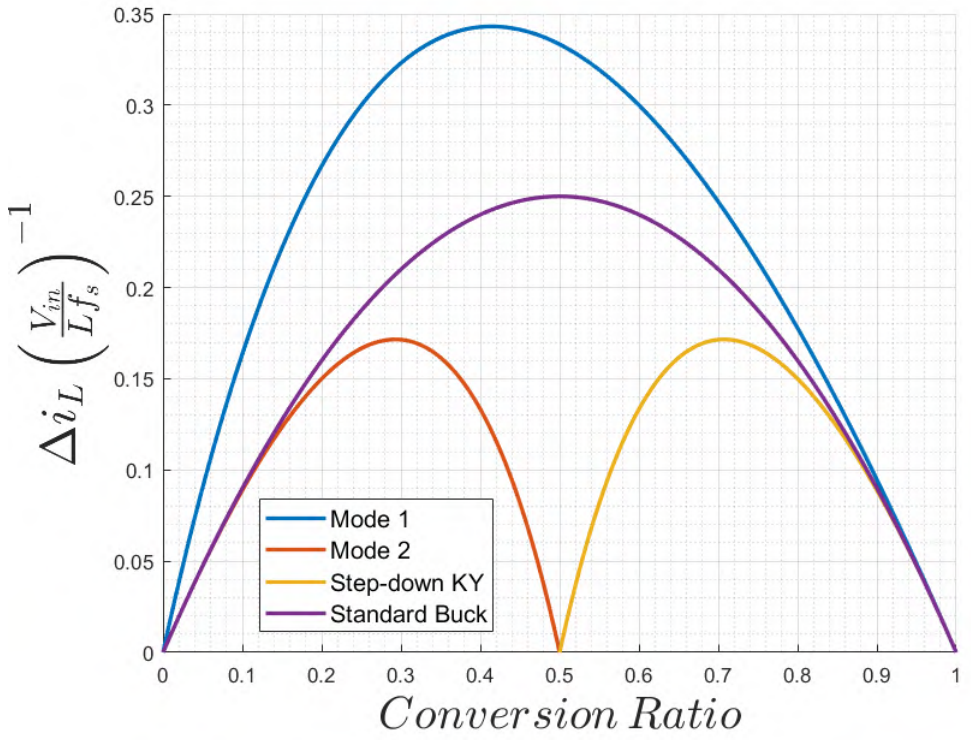


Figure 4.7.10: Reconfigurable three switches hybrid step-down converter normalized inductor current ripple. Comparison with an equivalent standard buck case.

	Hybrid Mode 1	Hybrid Mode 2	Step-down KY	Standard Buck
$\frac{I_L}{I_o}$	$\frac{(M+1)}{2}$	$(1-M)$	M	1
$\Delta i_L \left(\frac{V_{in}}{Lf_s}\right)^{-1}$	$\frac{M(1-M)}{(1+M)}$	$\frac{M(1-2M)}{1-M}$	$\frac{(1-M)(2M-1)}{M}$	$M(1-M)$

Table 4.12: Reconfigurable three switches hybrid step-down converter magnetic element requirements as a function of the conversion ratio resume.

component count and the presence of only one high-voltage switch make this topology interesting also for a discrete components implementation, but it must be noted that, in the case of a low output voltage application, D_2 should be replaced by a MOSFET to avoid a dramatic loss of efficiency. A totally synchronous implementation of the converter would instead help mitigate the drawback of Mode 1 having a higher inductor current ripple if compared to a standard buck. In both cases it should be noticed that only the two input switching devices are rated for a high voltage (V_{in}), while all the others are rated for the output voltage, that is potentially very low.

Chapter 5

Conclusions and Resume

Switched capacitor DC-DC converters are interesting for integrated applications due to their lack of a magnetic element but have the big disadvantage of fixed conversion ratios, allowing a continuous output voltage regulation only through increased power dissipation. A way of lowering the regulation related power dissipation would be to adopt multilevel switched capacitor converters and possibly use the so called dithering. Different multilevel switched capacitor converters were studied, but they all have some specific drawbacks, either in terms of voltage stress on the switches, output voltage resolution, number of requested components or difficulty of designing proper drivers.

The multilevel switched-capacitor topology that shows the most interesting properties is the Dickson charge pump circuit. This topology has a fixed maximum switches voltage stress, independent of the requested conversion ratio, three switches per cell, but its step-up version still allows to generate just integer conversion ratios. To obtain fractional output voltage resolution a cascade approach would be needed, highly increasing the converter complexity.

Hybrid converters mix switched-capacitor topologies with inductor based ones. These converters effectively allow to reduce the inductor size (and therefore the converter size itself) either by decreasing the average inductor current, the inductor voltage per second product or the switches voltage stress when compared to a standard equivalent topology. They also succeed in overcoming the main switched-capacitor converters limit, allowing a continuous regulation of the output voltage.

Different hybrid topologies found in literature were analysed, highlighting

their advantages when compared to a standard equivalent boost. Using these as a starting point different novel hybrid converters were proposed, each with specific advantages. In particular, combining the hybrid and reconfigurable converter approaches, a new topology capable of generating all the conversion ratios requested for a typical automotive LED lighting application was proposed. This converter allows standard inductive buck, boost and buck-boost operation, together with other five hybrid operating modes. These different operating regimes are obtained re-configuring the topology depending on the requested conversion ratio. By using eight switches this converter can therefore guarantee regulation with an input voltage varying between eight and eighteen Volts and an output voltage varying between three and sixty Volts, together with a reduced average inductor current if compared to an equivalent standard topology. The proposed solution hybrid operating modes were tested experimentally, through the implementation of an integrated simplified boost-only converter using discrete passive components but integrated switches, drivers and logic. The experimental tests show that, without employing appropriate cooling strategies, the prototype cannot operate at 1,8MHz at the higher conversion ratios. The efficiency starts in fact to decrease dramatically, with a positive feedback mechanism that makes the dissipated power increase even more, possibly until the failure of the IC. When the frequency is instead limited to 300 kHz (corresponding to the maximum value possible in the lower frequency automotive window) while the products $f_{sw}{\cdot}L$ and $f_{sw}{\cdot}C_f$ are kept constant (where L and C_f are the inductance and flying capacitance values respectively), the prototype shows a much higher efficiency and successfully yields the requested voltage conversion ratios. This, together with the observations made in the previous chapter, show that the proposed topology could potentially be interesting for real-world industrial applications; optimizing the converter design following the observations made in this thesis should in fact yield much improved performances.

5.0.1 Future Work

This thesis work allowed to study the characteristics of switched-capacitor converters and especially of hybrid converters. Different topologies were proposed and implemented. The knowledge gained and the results obtained constitute a strong foundation on which future work can be based. Some of

the topologies proposed but not implemented could be further studied and experimentally verified; multiphase switched-capacitor converters could be studied; other novel integrated hybrid topologies could be derived, for example adding other cells to the proposed reconfigurable buck-boost topology to further reduce the magnetic element requirements. Regarding the latter, some work remains to be done too. The converter dynamic properties should be studied, developing a proper average model. Furthermore, since it is such a vital feature of the proposed reconfigurable topology, a special focus should be put on investigating the converter behaviour during transitions between different operating modes. A proper controlling technique should also be studied and tested, in order to develop e complete architecture. Finally, a converter design optimization should be performed, taking into account the switching and driving losses too.

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