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Open issues in GaN-based HEMTs: performances, parasitics and reliability

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Abstract

Gallium nitride based high electron mobility transistors ($HEMTs$) are excellent candidates for high frequency and power applications. Due to high breakdown field, mobility, saturation velocity and thermal conductivity of GaN-based materials, $HEMTs$ may operate at voltage and temperature ranges far beyond conventional semiconductor as Si, $GaAs$ or InP; they also have a Baliga figure of merit many times higher and a lower resistance and hence reduced switching times and losses leading to improved efficiency. Still, they are affected by (i) parasitics phenomena and (ii) reliability issues: defects and dislocations may induce high leakage currents, kink effect and soft breakdown, while, in the reliability field, hot electrons, high electric fields and power are still under investigation.

In the first part of this work parasitics have been investigated. In particular, great interest has been devoted to trapping phenomena, which mainly influence the on-resistance (R_{ON}); transient and pulsed measurements help to extrapolate useful information as location in the epilayer structure, activation energy and cross section of the traps responsible of the R_{ON} collapse; we also studied leakage phenomena, proving that both the phenomena can be significantly reduced with the introduction of a $AlGaN$ back-barrier layer which, thanks to the additional band offset that prevents electrons from traveling and being trapped deep into the buffer. Finally, kink effect has been characterized; main results show it becomes almost negligible when a capping layer is grown over the AlGaN barrier and a semi-insulating substrate is used.

An extensive analysis of the electrical and optical properties of HEMTs biased in a non-destructive breakdown regime is the main topic of the second part. HEMTs can reach a sustainable breakdown condition with a V_G lower than the pinch-off voltage. Phenomena are mainly activated by two mechanisms, depending on the gate voltage

applied: when V_G is close to the pinch-off, space charge injection of electrons occurs and a parasitic path between source and drain is formed; if a more negative voltage is applied, breakdown occurs due to electrons injection through the gate. Tests reveal that HEMTs can emit a weak electroluminescence (EL) signal: this is localized at the edge of the gate when a low current is flowing; it shifts to drain edge and the intensity reaches its maximum at higher I_D when breakdown conditions are met. Moreover, the breakdown has a non-monotonic dependence from the temperature; this result confirms that two different mechanisms jointly interact at high voltage levels, one dominating on the other depending on the biasing condition. Single-heterostructure (SH) has a soft breakdown due to a poor ability to confine electrons into the channel and the consequent punch-through, independently from the gate to drain distance (L_{GD}). Many approaches have been successfully tested in order to improve the breakdown voltage (BV): GaN buffer doped with C or Fe, application of double-heterostructure (DH) epitaxy and devices with an $AlGaN$ back-barrier grown on a doped buffer. These solution efficiently increase the BV, which also becomes dependent from L_{GD} distance with a slope that ranges from $30\,V/\mu$m to $50\,V/\mu$m.
The third part deals with reliability issues. Results of accelerated life tests show that in SH devices a quick degradation of the electrical properties is visible in off-state even at low drain voltage biasing condition: the punch-through leakage path increases defects formation, causing a strong device degradation even in short life tests. DH devices present improved reliability due likely to (i) lower leakage currents (ii) less *sub-surface DIBL* (iii) higher breakdown values.
The last section is devoted to the NPI Project. The purpose of the third placement has been the analysis of the performances and of the reliability behavior of $GH25$ technology. DC measurements show that technology process is quite mature: low off-state and leakage currents, good output current and very few devices with non-standard behavior. Still, the devices suffer from kink effect as confirmed by pulsed measurements; moreover, pulsed characterization enlightens a consistent trapping phenomena, the current collapse being $\approx 30\%$, mainly related to traps under the gate into the buffer. Maximum gain available MAG analysis from RF tests reveals the source terminated field plate ($STFP$) to positively increases the gain, thanks to an extended depletion region that reduces current lag due surface effects. The application of the field plate

brings an additional capacitance, affecting the cross-over frequency which shifts from $\approx 25\,GHz$ to $\approx 20\,GHz$.

Current controlled breakdown measurements enlightened how, when a high V_D is applied, a parasitic paths between source and drain is formed due to sub-surface DIBL (punch-through). The critical voltage which the phenomena take place at depends from many factors: (i) the longer the gate drain distance is, the less the punch-through is likely to occur (ii) it shifts toward lower voltages when increasing V_G due to the reduction of the depletion region under the gate (iii) $STFP$ seems to have no meaningful effects.

These results seems to be related with those obtained from off-state step stress, where a fast degradation of the gate takes place for V_D higher than $70\,V$ until sub-surface DIBL occurs; when a parasitic source-drain channel is formed, the degradation rate reduces significantly because most of the current is sustained by the source. The only relevant visible change is the increase in off-state and leakage currents and parameters. A comparison with breakdown test results suggests that the cause may be the same described for current controlled breakdown.

Life tests have been carried out selecting three different biasing conditions (i) with high current and low field (I_D = 660mA/mm, V_D = $10V$), (ii) high field and low current (I_D = 5mA/mm, V_D = 60V), and (iii) class A bias point (I_D = 400mA/mm, V_D = 30V) at 423K to assess the reliability along the load line. Class A results show a fast degradation of the output current and a steep increase of on-resistance within 100 hours; similar results are visible when the sample is biased at high current and low voltage, even if at a much lower degree. When the device is biased at high voltage and low currents, only a small decrease of output characteristic is reported; on the other hand, both off-state and leakage currents significantly increase. The Class A condition is the worst working condition. The degradation can be caused (i) by high power and visible only when both high voltage and high current are applied (ii) by high temperature to which both the power dissipation and the high temperature jointly contribute. Additional tests at room temperature could help to understand the failure mechanisms.

Sommario

Gli *High Electron Mobility Transistor* ($HEMTs$) sono eccellenti candidati per applicazioni ad alta frequenza e di potenza. Grazie all'alta tensione di breakdown, alle elevate mobilità, velocità di saturazione, e conducibilità termica dei materiali basati su nitruro di gallio, gli $HEMTs$ possono operare ad elevate tensioni e a temperature di gran lunga superiori a quelle dei semiconduttori convenzionali, quali silicio Si, arsenuro di gallio $GaAs$ o fosfuro d'indio InP; denotano inoltre una Baliga's figure of merit di diversi ordini superiore e una minore resistenza con la conseguenza di ridotti tempi di transizione e perdite parassite molto inferiori che consentono una maggior efficienza. Tuttavia sono affetti da (i) fenomeni parassiti transitori che causano instabilità e (ii) problematiche legate all'affidabilità: impurità, difetti e dislocazioni possono indurre elevate correnti di perdita, effetto kink e basse tensioni di rottura mentre, per quanto concerne l'affidabilità, gli effetti degenerativi correlati a elettroni ad alta energia (chiamati anche *hot electrons*), o dipendenti dagli elevati campi elettrici a cui i dispositivi vengono sottoposti o dalla potenza sono ancora oggetto di studio al fine di identificare i meccanismi e le leggi di degradazione.
La prima parte di questo lavoro è stata dedicata all'analisi dei fenomeni parassiti. In particolare la maggior attenzione è stata dedicata ai fenomeni di trapping, che tendono ad influenzare soprattutto la R_{ON}; l'uso di tecniche quali lo studio dei transienti e le misure impulsate si rivelano molto utili per raccogliere informazioni come la distribuzione spaziale all'interno della struttura dei dispositivi, l'energia di attivazione e la sezione di cattura responsabili del collasso della resistenza in on-state; anche le correnti di perdita sono state oggetto di studio che ha provato come l'uso di strutture alternative con per esempio, l'introduzione di uno *back-barrier layer* in $AlGaN$, grazie alla presenza di un band-gap aggiuntivo all'interfaccia con il *GaN channel layer* che

impedisce agli elettroni di spostarsi in profindità nel *buffer layer* e di rimanere intrappolati o muoversi verso regioni a potenziale differente, cosentono di ridurre in modo significativo le correnti di perdita. Infine, è stata portata avanti una caratterizzazione delle proprietà del *kink*: i risultati evidenziano come l'uso di un substrato altamente resistivo e la deposizione di un capping layer in GaN sopra la barriera di AlGaN rendano l'effetto trascurabile. Una dettagliata analisi delle proprietà elettriche ed ottiche di dispositivi $HEMTs$ polarizzati in condizioni di breakdown sostenibile costituisce l'argomento principale della seconda parte. Gli $HEMTs$ possono essere polarizzati in condizioni di breakdown non distruttivo se la tensione di gate V_G è inferiore alla tensione di pinch-off. Il fenomeno viene attivato nella maggior parte dei casi considerati da due meccanismi, a seconda della tensione applicata al contatto di gate. Quando la tensione V_G è vicina alla condizione di pinch-off, ha luogo l'iniezione di portatori nella regione di carica spaziale e si ha la formazione di un canale conduttivo parassita che consente il flusso di corrente tra source e drain; se la tensione al gate viene ridotta, la formazione del canale è meno probabile, e il breakdown avviene a causa dell'iniezione di carica attraverso il gate. I tests mostrano inoltre che in condizioni di breakdown gli $HEMT$ possono emettere un debole segnale di elettroluminescenza: quest'ultimo è localizzato lungo il bordo del gate quando la corrente che fluisce è molto bassa; ma si sposta verso il bordo del drain e il segnale diventa più intenso quando la I_D raggiunge le condizioni di breakdown sostenibile. Inoltre, il breakdown mostra un comportamento non monotonico in funzione della temperatura, il che conferma la coesistenza di due differenti meccanismi che interagiscono alle alte tensioni, l'uno dominando sull'altro o viceversa a seconda delle condizioni di polarizzazione. Ls singola eterostruttura è soggetta a breakdown già a basse tensioni ($35\,V$) a causa della scarsa capacità di confinare gli elettroni all'interno del canale, indipendentemente dalla distanza gate-drain. Molte soluzioni alternative sono state testate con successo nel tentativo di migliorare il breakdown: dispositivi con buffer GaN drogato con ferro Fe o carbonio C, l'applicazione di doppie eterostrutture e infine strutture con una back-barrier $AlGaN$ cresciuta su buffer GaN drogato. Queste soluzioni si sono rivelate efficienti nel migliorare il breakdown, che è risultato dipendere anche dalla distanza gate-drain.

La terza ed ultima parte è dedicata all'affidabiltà dei dispositivi. I risultati dei tests di vita accelerata mostrano che nei dispositivi a singola eterostruttura si riscontra una

rapida degradazione delle caratteristiche elettriche in off-state anche in condizioni di basse tensioni: il punch-through causa la formazione di difetti aggiuntivi che ne minano l'affidabilità. Al contrario, i dispositivi in doppia eterostruttura mostrano una migliore affidabilità grazie a (i) correnti di perdita molto inferiori (ii) ridotta probailità di punch-through, che ha solitamente luogo ad alte tensioni (iii) tensioni di breakdown molto più elevate.

Nell'ultima sezione si è dato spazio al progetto NPI in collaborazione con l'ESA, con lo studio delle caratteristiche dei $GH25$. La caratterizzazione DC ha mostrato una tecnologia matura, anche se ancora soggetta a fenomeni di instabilità come il kink e il current collapse ($\approx 30\,\%$). L'uso di field plates ha efficacemente migliorato il MAG al costo di una ridotta frequenza di cross-over, e nei test per il breakdown si è rivelato trascurabile. I dati ottenuti nei test in off-state hanno mostrato una ridotta degradazione delle caratteristiche elettriche, fino al raggiungimento di una tensione critica che, confrontata con i risultati del breakdown, suggerisce che la possibile causa di rottura sia ancora il punch-through.

I life test condotti a $150\,°C$ hanno purtroppo evidenziato come il punto di lavoro in classe A presenti una assai rapida e significativa degradazione dei dispositivi. Due possibili cause sono state considerate: la degradazione può essere dovuta a (i) elevata potenza (ii) elevata temperatura del dispositivo a cui contribuisce la condizione di polarizzazione. Ulteriori test a temperatura ambiente potrebbero essere d'aiuto nell'identificare il meccanismo coinvolto.

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Chapter 1

Materials and Devices properties

1.1 Gallium nitride properties

Despite the fact that GaN has been studied far more extensively than the other group III-nitrides, further investigations are still needed to approach the level of understanding of technologically important materials such as Si and $GaAs$. GaN growth often suffers from large background n-type carrier concentrations because of native defects and, possibly, impurities. The lack of commercially available native substrates exacerbates the situation. These, together with the difficulties in obtaining p-type doping, and the arcane fabrication processes caused the early bottlenecks stymieing progress. Information available in the literature on many of the physical properties of GaN is in some cases still in the process of evolution, and naturally controversial. This is in part a consequence of measurements being made on samples of widely varying quality.

The burgeoning interest in nitrides has led to substantial improvements in the crystal growth and processing technologies, thus overcoming many difficulties encountered earlier. Consequently, a number of laboratories consistently obtained high quality GaN with room-temperature background electron concentrations as low as $5 \cdot 10^{16}\, cm^3$. The successful development of approaches leading to p-type GaN has led to the demonstration of excellent p-n junction LEDs in the UV, violet, blue, green, and even yellow bands of the visible spectrum with brightness suitable for outdoor displays, CW lasers, and UV detectors, including the ones for the solar blind region. Moreover, power

modulation doped field effect transistors (MODFETs) also generically referred to as heterojunction field effect transistors (HFETs) have been developed. What follows reports on the state of knowledge regarding the physical properties of GaN.

Table 1.1: *Properties of gallium nitride in the two phases, wurzite and zinc blende.*

Properties	Symbol	unit	wurzite	zincoblenda
Latice constant	$a = b$	Å	3.189	4.52
	c	Å	5.185	4.52
Coefficient of thermal expansion	$\Delta a/a$	K^{-1}	5.59×10^{-6}	...
	$\Delta c/c$	K^{-1}	3.17×10^{-6}	...
Band-gap	E_g	eV	3.39	3.44
Band gap temperature coefficient	dE_g/dT	eV/K	-6.0×10^{-4}	...
Band gap pressure coefficient	dE_g/dP	$eV/kbar$	4.2×10^{-3}	...
Intrinsic carrier concentration	n_i	cm^{-3}	1.9×10^{10}	
Electron mobility	μ_n	cm^2/Vs	1500	
Thermal diffusion constant	D_n	cm^2/s	39	
Electronic affinity	χ	V	4.1	
Refraction index	n		2.33	2.5
Breakdown field	ϵ_1	V/cm	33×10^5	
Thermal conductivity	κ	$W/(cmk)$	1.3	
Dielectric constants	ϵ_0		8.9	...
	ϵ_∞		5.35	...
Phonon modes	A_1TO	cm^{-1}	560	...
	E_1TO	cm^{-1}	144	...
	E_2	cm^{-1}	144	...
	A_1LO	cm^{-1}	560	...
	E_1LO	cm^{-1}	144	...

1.1.1 Chemical properties of the *GaN*

Since 1932, when *Johnson et al.* [1] synthesized GaN for the first time, GaN has been well known as an exceedingly stable compound exhibiting significant hardness. Its chemical stability at elevated temperatures together with its hardness that has made it an attractive material for protective coatings. Moreover, its wide energy bandgap has made it also an excellent candidate for device operation at high temperatures and caustic environments.

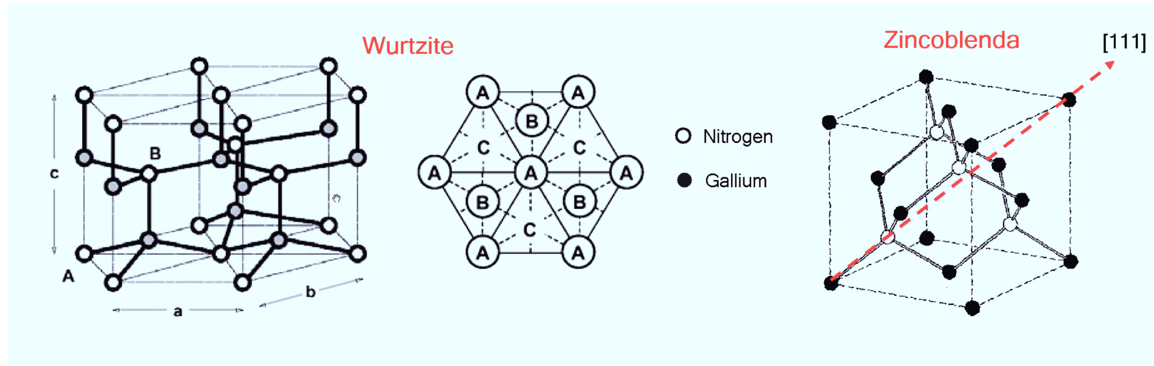


Figure 1.1: *Chemical structure of the two phases, wurzite e zinc blende, typical of the GaN.*

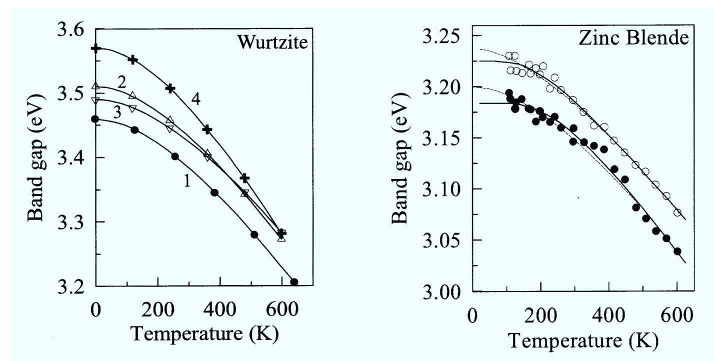


Figure 1.2: *Gallium nitride E_g dependency from temperature.*

Apart from its hardness, *GaN* has got more and more attention from researchers due excellent semiconducting features. The excellent thermal stability of gallium nitrides grants the use of high-temperature processing; however, its chemical stability represents a technological issue. Conventional wet etching techniques have not been as successful for *GaN* device fabrication. *Maruska et Tietjen* [2] reported that this binary compound is insoluble in H_2O, acids, or bases at room temperature, but show solubility in hot alkali solutions at very slow rates. *GaN* reacts with *NaOH*, causing the formation of a thin *GaOH* layer on the surface which prohibits wet etching of the nitride itself (*Pankove* [3]): To circumvent this difficulty, an electrolytic etching technique has been developed. Low-quality *GaN* has been etched at reasonably high rates in *NaOH* [4], H_2SO_4 [5], and H_3PO_4 [6], extremely useful for identifying defects and estimating their densities; on the other side, they are not as useful for the fabrication of devices [7].
Well-established chemical etching processes do help for the device technology development. Various dry etching processes reviewed by *Mohammad et al.* [8] and *Pearton et al.* [9] are promising possibilities, but also have several disadvantages, including

the generation of ion-induced damage and difficulty in obtaining smooth etched side-walls. There have been many efforts involving assisted wet etching techniques. Photoenhanced electrochemical (*PEC*) wet etching has been demonstrated and offers the advantage of low surface damage and low equipment cost [10].

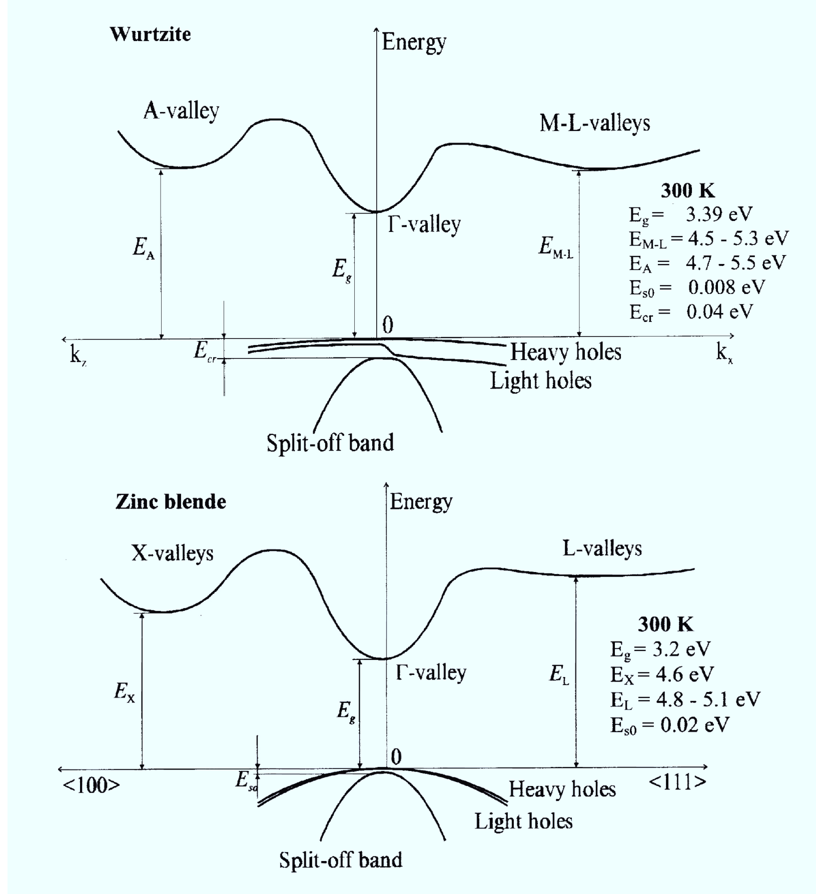


Figure 1.3: *Babd structure of wurzite and zinc blende.*

1.1.2 Structural properties of the *GaN*

Gallium nitride can be found in two different phases: wurzite and zinc blende; the latter is usually unstable and it is prone to change its phase to the former. Wurzite structure of *GaN* has lattice onstants $a = 3.189\,\mathring{A}$ and $c = 5.185\,\mathring{A}$ as first reported by *Maruska and Tietjen* [2], given a mean coefficient of thermal expansion of $\Delta a/a = \Delta b/b = 5.59 \cdot 10^{-6}\,K^{-1}$ over the temperature range $300 - 900\,K$; as far as c is concerned, values $\Delta c/c$ have been approximated to $3.17 \cdot 10^{-6}\,k^{-1}$ and $7.75 \cdot 10^{-6}\,k^{-1}$ for temperature ranges $300 - 700\,K$ and $700 - 900\,K$ respectively.

These parameters are subject to variation depending on many factors: growth condition, impurities concentrations and film stoichiometry. Lattice constants are reported to grow larger when the gallium nitride is grown at higher rates, probably because of increased interstitial defects, or in case of Zn heavy doping [11] or Mg [12], which seem to be prone to occupy lattice sites of the much smaller nitrogen stoms and thus causing lattice expansion.

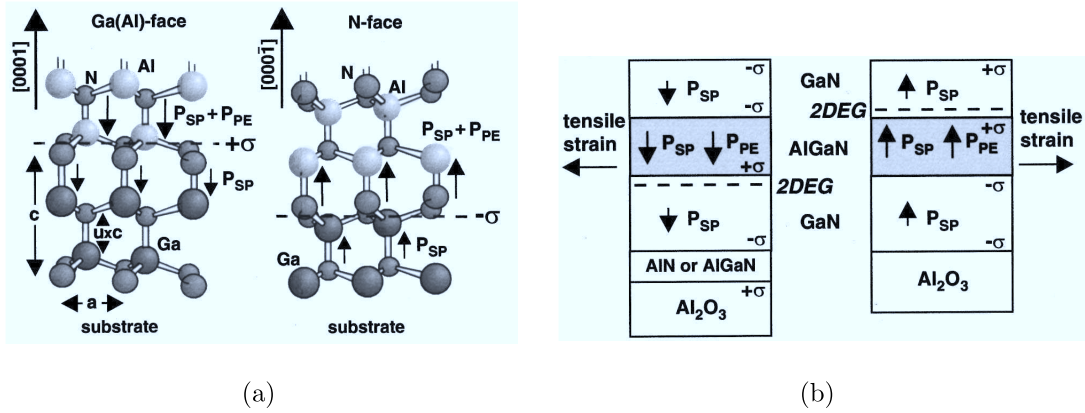
1.1.3 Electrical properties of *GaN*

Gallium nitride has been reported in all the cases to be unintentionally n-type doped, in most cases with electron concentration in the order of $10^{16}\,cm^{-3}$; due to impossibility to detect in sufficient quantity any impurity into the GaN, this spontaneous polarization has been associated with native defects widely thought to be nitrogens vacancies. Hence, development of reliable p-type doping layers has been for a long time a challenge to researcher, resulting in heavily compensated, highly resistive films. Room-temperature and liquid nitrogen temperature mobilities of $\mu_n \approx 600\,cm^2/Vs$ and $\mu_n \approx 1500\,cm^2/Vs$ at a carrier concentration of $n = 4 \cdot 10^{16}\,cm^{-3}$ and $n = 8 \cdot 10^{16}\,cm^{-3}$ has been measured. In the $300 - 900\,K$, the mobility tend to vary with T^{-2}, and at $900\,K$, a mobility of $\mu_n \approx 25\,cm^2/Vs$ has been measured.

1.1.4 Optical properties of the *GaN*

GaN is primarily of interest for its potential as blue and UV emitter. The gallium nitride direct energy band gap has been accurately measured by *Maruska and Tietjen* [2] and has been found equal to $3.39\,eV$; many authors studied its dependency from temperature, estimating a temperature coefficient of $dE_g/dT = -6 \cdot 10^{-4}\,eV/K$ in the linear above $180\,°C$ (*Pankove et al.* [13]); *Matsumoto et Aoki* [14] found it to be $dE_g/dT = -3.5 \cdot 10^{-4}\,eV/K$ in the range $30 - 150\,K$ and confirmed the value found by Pankove when temperature range is $150\,K - 300\,K$. *Monemar* [15] determined the fundamental band gap to be $3.503 \mp 0.005\,eV$ at $1.6\,K$ and fit the temperature dependence of the band gap to the empirical relation

$$E_g = 3.503 + \frac{5.08 \cdot 10^{-4}\,T^2}{T - 996}\,eV \tag{1.1}$$



(a) (b)

Figure 1.4: *(a) Crystal structure, polarization induced bound sheet charge, piezoelectric and spontaneous polarization, of pseudomorphic AlN/GaN heterostructures with Ga Al!-face or N-face polarity. (b) Spontaneous polarization, piezoelectric polarization bound interface charges, and 2DEGs in pseudomorphic GaN/AlGaN/GaN heterostructures with Ga-face or N-face polarity. In Ga-face heterostructures the 2DEG is located close to the lower AlGaN/GaN interface, in N-face heterostructures close to the upper GaN/AlGaN interface. GaN/AlGaN/GaN[16].*

The phonon modes have received considerable attention, and four main modes have been identified in heavily doped GaN needles. The A_1 and E_1, both of them transverse optical TO, have been observed at $533\,cm^{-1}$ and $559\,cm^{-1}$ respectively; E_2 modes at $144\,cm^{-1}$ and $569\,cm^{-1}$. There have been several measurements of the optical constants on GaN. The refraction index have been measured: $n(3.38\,eV) = 2.67$ and $n(1.0\,eV) = 2.33$; dielectric constant is $\epsilon_0 = 8.9$, but at high frequency $\epsilon_\infty = 3.35$ while electron affinity has been estimated to vary in the range $4.1\,eV \geq \chi \geq 2.1\,eV$.

1.2 The heterostructure AlGaN/GaN

An heterostructure is formed when a semiconductor material is grown with epitaxial techniques on the top of another semiconductor material. When the *AlGaN* is grown on the top of the *GaN* layer, the *AlGaN* layer adopts in its growing process the lattice constant of the neighboring semiconductor. In order to accommodate the mismatch between the lattice constants, the thin *AlGaN* epitaxial layer becomes internally strained. This internal accommodation works only if the thickness of the strained *AlGaN* layer is below a specific limit; above this limit the mismatch is accommodated by the formation of dislocations and defects at the interface.

In the absence of an external electric field, the total polarization P of GaN or $AlGaN$ layers is the sum of the spontaneous polarization P_{SP} and the strain-induced or piezoelectric polarization P_{PE} . The spontaneous polarization for GaN and AlN is negative: in the layers grown in the (0001) direction, P_{SP} is opposite to the growth direction and increases in magnitude with the Al mole fraction in the $Al_xGa_{1-x}N$ alloy. Piezoelectric polarization arises due to strain at the $AlGaN/GaN$ interface related to the difference in lattice constants between these two materials, $\approx 2.4\,\%$ difference between AlN and GaN at $300\,K$. This piezoelectric field points from the cation-terminated face to the anion-terminated face and is equal to

$$P_{PE}(x) = 2 \cdot \frac{a(x) - a(0)}{a(0)} \left[e_{31}(x) - e_{33}(x) \frac{C_{13}(x)}{C_{33}(x)} \right] \tag{1.2}$$

where $a(x)$ and $a(0)$ are the lattice constants of $Al_xGa_{1-x}N$ and GaN, respectively, e_{31} and e_{33} are piezoelectric constants, and C_{13} and C_{33} are elastic constants. The important fact is increasing the Al content in the strained $AlGaN$ barrier leads to an increase in both piezoelectric and spontaneous polarization. Associated with the abrupt changes of the polarization field at the $AlGaN/GaN$ interface is a polarization-induced charge density:

$$\sigma = P(AlGaN) - P(GaN) = P_{SP}(AlGaN) + P_{PE}(AlGaN) - P_{SP}(GaN) \tag{1.3}$$

If the surfaces of the grown $AlGaN/GaN$ structures are $Ga(Al)$-terminated, the positive polarization-induced charge will be located at the $AlGaN/GaN$ heterointerface, while negative charge will be sitting at the top of the $AlGaN$ barrier. The positive charge tends to be compensated by electrons that form a two-dimensional electron gas at the $AlGaN/GaN$ interface. The negative polarization-induced charge at the top of the AlGaN layer has to be reduced then by some positive surface charges. Free electrons tend to compensate the positive polarization induced sheet charge which is bound at the lower $AlGaN/GaN$ interface for Ga-face or in case of N-face $GaN/AlGaN/GaN$ $HEMT$ structures, at the upper $GaN/AlGaN$ interface. The value of the total polarization induced sheet charge is the same in heterostructures of different polarities for a given Al concentration and strain of the barrier. For undoped Ga-face $AlGaN/GaN$ or $GaN/AlGaN/GaN$ HEMT structures, the sheet electron concentration $n_S(x)$ can

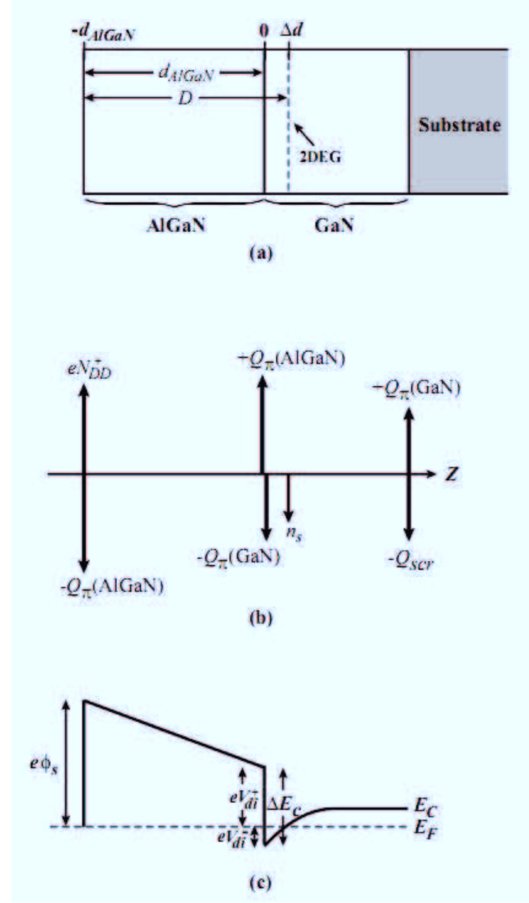


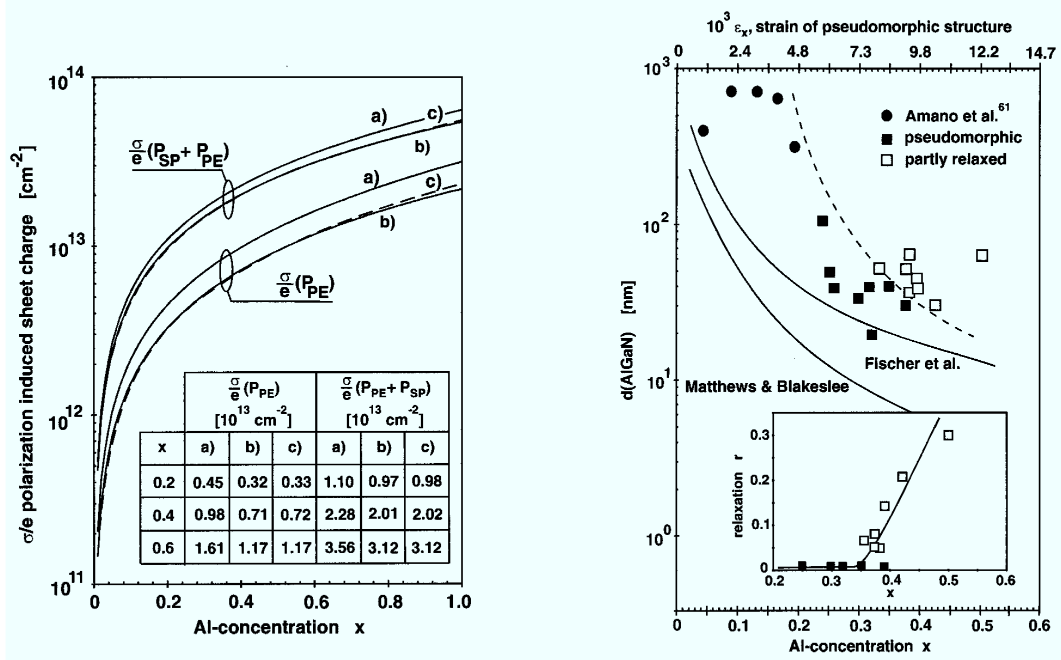
Figure 1.5: *(a) Typical AlGaN/GaN heterostructure used in Ga-face HEMT technology, along with (b) the charge distribution and (c) the band diagram of the structure [17].*

be calculated by using the total bound sheet charge $\sigma(x)$:

$$n_s(x) = \frac{\sigma(x)}{e} \frac{\epsilon_0 \epsilon(x)}{d_{AlGaN} e^2} [e\phi_b(x) + E_F(x) - \Delta E_C(x)] \tag{1.4}$$

$\epsilon(x)$ is the relative dielectric constant of $Al_xGa_{1-x}N$, d_{GaN} and d_{AlGaN} are the thicknesses of the barrier and the cap layer, $e[\phi_b(x)]$ e $e[\phi_b^{eff}(x)]$ are the effective Schottky barriers of the gate contact on top of $AlGaN$, $E_F(x)$ is the Fermi level with respect to the GaN conduction-band-edge energy, and ΔE_C is the conduction band offset at the $AlGaN/GaN$ interface where a 2DEG forms; For undoped $HEMT$ structures and assuming that the background concentration of free carriers can be neglected ($N_d \leq 10^{16}\, cm^{-3}$), it is found that the value of the sheet carrier concentration is dominated by the total polarization induced sheet charge which can be controlled by the alloy composition of the barrier. The band gap of $Al_xGa_{1-x}N$ is measured to be

$$E_g(x) = xE_g(AlN) + (1 - x)E_g(GaN) - 1.0x(1 - x) \tag{1.5}$$



	σ/e (PPE) [10^13 cm^-2]			σ/e (PPE+ PSP) [10^13 cm^-2]		
x	a)	b)	c)	a)	b)	c)
0.2	0.45	0.32	0.33	1.10	0.97	0.98
0.4	0.98	0.71	0.72	2.28	2.01	2.02
0.6	1.61	1.17	1.17	3.56	3.12	3.12

Figure 1.6: *(a) Bound piezoelectric $\sigma/e(P_{PE})$ and total polarization $\sigma/e(P_{SP} + P_{PE})$ induced sheet charge versus alloy composition. The insert enables a comparison for alloy compositions of $x = 0.2$, 0.4, and 0.6 (b) Critical thickness of AlGaN grown on relaxed GaN calculated vs Al concentration x (lower horizontal scale), or strain of pseudomorphic grown heterostructures ϵ_x (upper scale). The insert shows the degree of relaxation r(x) measured by HRXRD vs alloy compositions for AlGaN barriers with a thickness of about 300 Å [16].*

The questions that remain open include what determines the Fermi-level position at the non-metallized surfaces of the $AlGaN/GaN$ structures and what is the origin of the 2DEG electrons in the nominally undoped samples. A possible explanation is based on the existence of the surface donor-like states. These states might be the source of both the 2DEG electrons and the positive charges compensating the negative polarization-induced charge at the top of the $AlGaN$ layer. Assuming these donor-like surface states are located quite deep in the $AlGaN$ band gap, they will all be occupied at small values of barrier layer thickness d_{AlGaN}. No 2DEG will be formed and the field in the top layer will be determined by the polarization-induced charges. As the width of the $AlGaN$ layer increases, the Fermi level at the surface slides down approaching the deep donor level. Once the Fermi level reaches the surface states they start emptying. A two-dimensional electron gas can then be formed at the $AlGaN/GaN$ interface and the field in the $AlGaN$ barrier will be reduced. As the thickness of $AlGaN$ layer is increased further, the 2DEG density will tend to saturate approaching the value of the

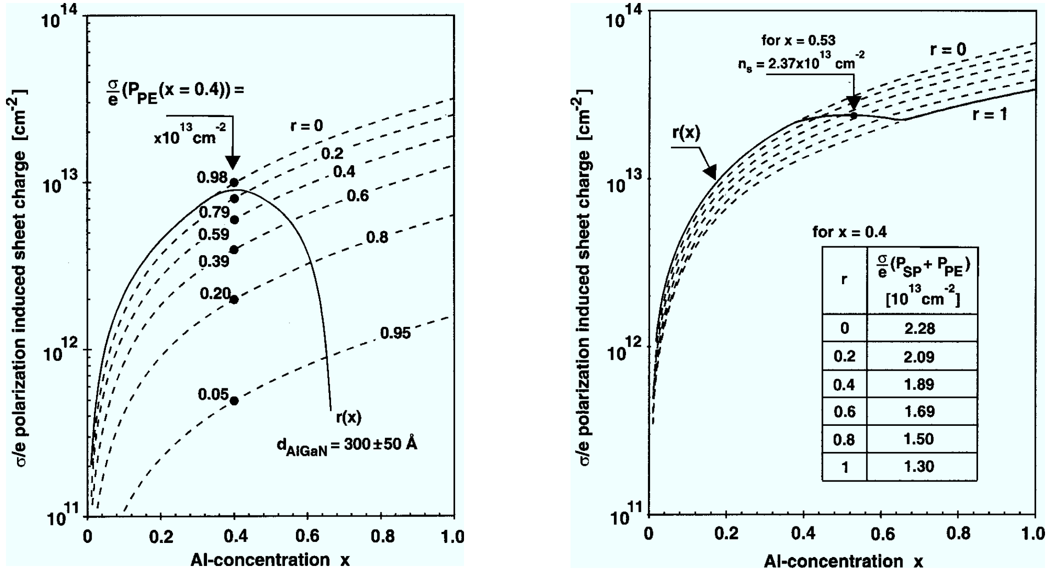


Figure 1.7: *Graphs show, on the left, calculated $\sigma/e(P_{PE})$ for pseudomorphically grown AlGaN/GaN heterostructures r=0, and barriers with different degrees of relaxation r=0.2, 0.4,..., vs Al concentration of the top layer (dashed lines). On the right, $\sigma/e(P_{SP}+P_{PE})$ vs Al concentration of the top layer (dashed lines). The solid line represents $\sigma/e(P_{SP}+P_{PE})$ for AlGaN barriers with a thickness of about 300 Å by talking into account the measured degrees of relaxation r(x). The inset shows the calculated sheet charges for different degrees of relaxation of an $Al_{0.4}Ga_{0.6}N/GaN$ heterostructure.[16].*

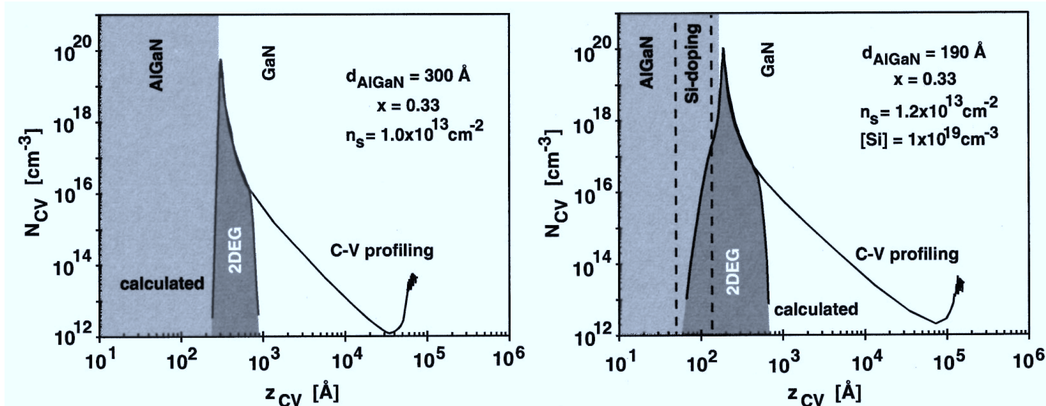


Figure 1.8: *Measured and calculated sheet carrier distributions of 2DEGs located close to the interface of pseudomorphically grown Ga-face $Al_{0.33}Ga_{0.67}N/GaN$ HEMTs. A sheet carrier concentration of $1 \cdot 10^{13}\, cm^{-2}$ was determined by C–V profiling for an undoped barrier with a thickness of 300 Å. For a 190 Å thick doped barrier with a silicon concentration of $1 \cdot 10^{19}\, cm^{-3}$ over a depth of 100 Å (spacer layer 30 Å), a sheet carrier concentration of $1.2 \cdot 10^{13}\, cm{-}2$ was observed at room temperature. [16].*

polarization-induced charge, assuming the thickness of the *AlGaN* barrier does not reach the critical thickness at which relaxation of the ternary alloy occurs.

1.3 Substates

GaN growth is done starting from substrate of different material, due to the lack of a mature technology able to growth *GaN* substrates. This forced choice has some drawbacks, due to the differences in the materials properties used. Most used materials are sapphire (Al_2O_3), silicon carbide (SiC) and silicon (Si). Only in the last few years new processes (HVPE-hydride vapor phase epitaxy and high-pressure growth) have been developed and allow the realization of thick *GaN* layer that can be used without the carrier substrate; still, these processes lack the maturity to become useful in commercial areas.
Sapphire is the most used, due to low cost, good thermal stability and large substrate

Table 1.2: *Properties of the different substrates used for GaN epitaxy.*

Property	Unit	Al_2O_3	6H-SiC	Si
Simmetry		hexagonal	hexagonal	cubic
Lattice constant a	$\AA$	4.765	3.08	5.431
Lattice constant c	$\AA$	12.982	15.117	-
Thermal conductivity	$W/(cm\,K)$	0.25	3.8	1.56
Lattice mismatch with *GaN*	%	15	3.1	17

are available thanks to maturity of the technology; the main disadvantage is a poor thermal conductivity, hence inducing self-heating the device in high power biasing condition, making the sapphire inappropriate for applications in high power fields. Also, gallium nitride and sapphire have a $\approx 15\,\%$ lattice mismatch, thus introducing an elevated concentration of defects in the buffer layer.
Another material used is the silicon carbide. The material show a low lattice mismatch with the *GaN* ($3.5\,\%$). On the other side, SiC substrates have high costs; moreover, it is difficult to control resistivity and they also suffer from high dislocation density.
A possible solution is the use of silicon substrates. Lattice mismatch with *GaN* is

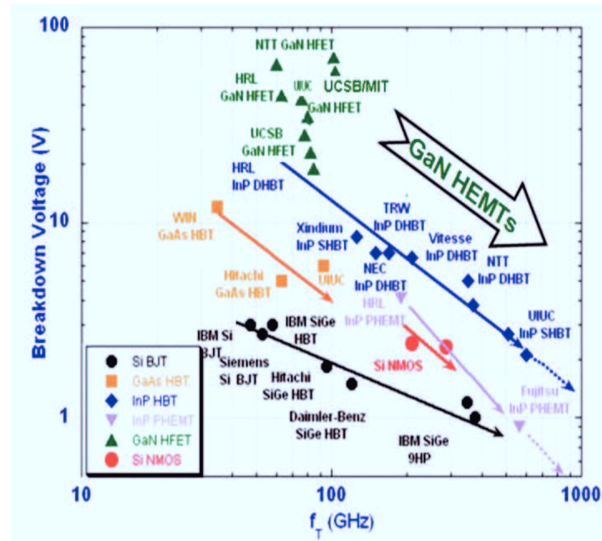


Figure 1.9: *Breakdown voltage vs. cut-off frequency of the actual semiconductor technologies [18].*

higher than the other two, but it is very cheap and growth processes are well know; Furthermore, it is available in high quality and large diameter wafers. Finally this allows to integrate in the same wafer both Si-based and GaN-based devices.

1.4 Power switching devices

The capability of the gallium nitride to withstand very large critical electric fields makes GaN-based $HEMTs$ extremely attractive for any power switching application, where electronic devices switch from a off-state, with very low (leakage) currents and high voltages to an on-state condition where high current levels flow through the device biased at low voltages and vice-versa. In this operating condition, an ideal device should have no power dissipation in both states, that means zero currents in off-state, and negligible voltage in on-state, but also during transitions between the two states. For a real device these requirements translate into very low leakage current when turned off in low power bias point, almost infinite subthreshold slope, and low on-resistance with a low knee voltage, in order to minimize the voltage drop once the device turns on; from the time response point of view, it is essential the rise-time is optimized in order to grant the widest range of frequencies, and thus of applications too.

Here comes in handy the extremely high breakdown voltages the GaN can sustain, together with the possibility to drive very high current with a minimal voltage drop

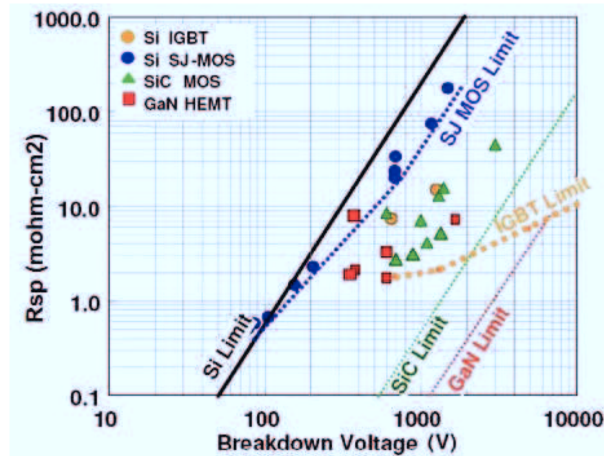


Figure 1.10: *Specific ON-state resistance vs. breakdown voltage for typical high-power switching technologies based on different semiconductors; theoretical data (line) and experimental results (dots) [19].*

and the small parasitic capacitance inside a $HEMT$ that grants fast switching times and high frequencies (Fig. 1.9 and 1.10). The main disadvantage is that the GaN technology is usually depletion-mode, and devices grown show a negative threshold. Hence, the channel is formed at zero-bias condition, and it requires the application of a negative voltage to turn off the device and grant safety.

In order to overcome this difficulties, multiple solution have been tested with positive results. *Uemoto et al.* [20] have presented a normally-off GaN transistor with a breakdown voltage of $800\,V$ and $2.6\,\Omega m \cdot cm^2$ R_{ON}; *Huang et al.* [21] a $MOS - GaN$ switch integrating a n-channel lateral $GaN\ MOSFET$ with a $770\,V$ blocking voltage Schottky diode. Moreover, *Niiyama et al.* [22] have presented a $+3\,V$ threshold-voltage $GaN\ MOSFET$, with a breakdown voltage higher than $1550\,V$ and *Kanamura et al.* [23] have shown a triple cap layer with recessed-gate structure, e-mode, $MIS{-}HEMT$, with $+3\,V$ of threshold voltage and $320\,V$ of off-state breakdown.

1.5 Trapping effects

The growth techniques which are far from being able to deposit impurity-free material; the different materials and their properties that cause strain and dislocation that propagates into each layer; the complex epilayer composition with the consequent interfaces, doping; the process that alter the surfaces with etching, masks, metal depo-

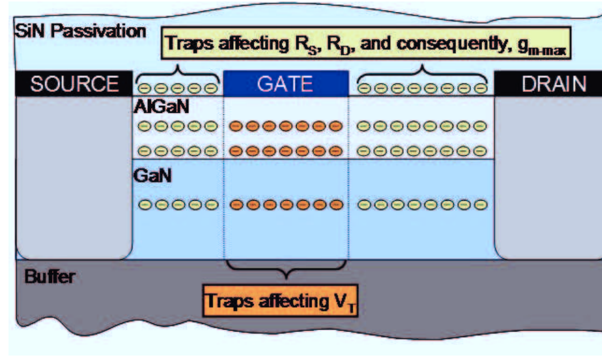


Figure 1.11: *Different possible traps position inside the AlGaN/GaN HEMT layer structure and parameters affected.*

sition are the main causes for the presence of material defects, which creates unwanted available energy-states.
This energy-states can act as traps for both electrons or holes, depending on their nature. They can be located deep into the buffer, in the *AlGaN* barrier layers, at the surface of the devices, or in the interfaces between all these layers. Depending on their position, they cause different effects and may affect DC performances, causing variation on the threshold, or the dynamic transconductance. They may even alter *RF* behavior (Fig. 1.13). In the recent years, their characterization has attracted attention from several research groups, in the attempt to identify their nature and properties and to find a possible solution to their side-effects, that can strongly influence the working condition of the devices. Above all, two main phenomena are often encountered, but are still under analysis due to their complex nature: kink effect and current collapse.

1.5.1 Kink effect

The kink effects is a (very) slow trapping phenomena that induces a reduction in the measured currents at low drain voltages. it is possible to define a critical voltage V_{kink} as the maximum voltage below which the drain current reduction is visible for a fixed V_{GS}; below it the current reduces due to trapping, above this voltage I_D quickly recover, and is no longer visible. Varying V_G, it is possible to trace a locus of V_{kink}, see Fig. 1.12, that divide the output region into two areas. This phenomenon seems to be related to electrons interaction with two different deep levels. At V_{DS} below V_{kink}, electrons are captured by a deep acceptor state and the threshold shifts towards

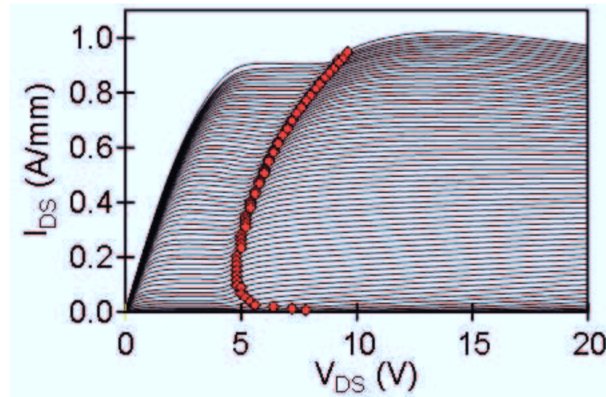


Figure 1.12: *Output characteristics of a kink-affected device. Red diamonds correspond to the maximum of the output conductance (V_{Kink}) [24].*

positive voltages; when the drain voltage applied is higher than V_{kink}, a field-assisted de-trapping phenomena takes place, and the current is restored to its normal levels. The non monotonic dependence of the drain kink voltage at different V_G indicates a possible impact-ionization de-trapping mechanism caused by channel hot electrons [25], feasible at this voltage level.

Kink effects manifest itself in many different ways: it may appear after repeated measures, or in some biasing condition only; sometimes trapping occurs when the device is not biased, and reduces, or disappear, after few measurements. It is well know its dependance from dwell time in the biasing condition, and from light, which may help de-trapping if using a light of proper wavelength.

1.5.2 Current collapse

Current collapse, also known as current compression or $DC - to - RF$ dispersion, is a parasitic effect that reduces the RF output power at high frequency: it causes a reduction of the dynamic saturation current compared to the DC current, an increase of the access resistances, mainly on the drain side, and hence a reduction of the dynamic transconductance, which reduces the RF gain and the output RF power, Fig. 1.13.

The increase of the drain access resistance, the shift of the knee voltage, and the reduction of the saturation current, cause a significant reduction of the maximum available RF power. Furthermore, the effect increases the high-frequency distortion

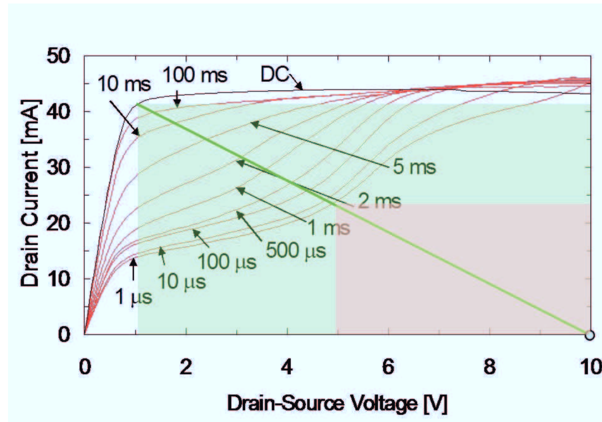


Figure 1.13: *Schematic representation of the current-collapsed output characteris- tics measured decreasing the integration time.*

and reduces the efficiency:

$$P_{OUT} = \Delta V \cdot \Delta I = (BV - V_{knee}) \cdot I_{DSAT} \tag{1.6}$$

current collapse is correlated with the accumulation of negative charge on the surface traps. Electrons coming from the gate, due to the high electric-field located at the drain edge of the gate, can fill the donor states located on the surface close to the gate terminal. When this happens, the negative charge of the channel electrons are no longer balanced and part of the channel will be depleted.

The extension of the depletion region acts as negative biased virtual gate [26] that depletes part of the channel. The current is no longer controlled only by the standard gate by the applied gate-bias, but also by the virtual-one, which depends on the amount of charge trapped on the surface states. The virtual gate acts with a delay depending on the de-trapping response of the surface traps which are usually slower than the desired working frequency. Unfortunately, no direct control is given over the virtual gate and the device will work with a maximum current depending on the slowest phenomena between the RF-sweep and the trapping/detrapping transients of surface traps, and not at the maximum DC performances. In pulsed operation, it will be affected by the trapping condition induced by the bias-point, and by the de-trapping transient reached after the on-state pulse [27].

1.6 Breakdown

The most unique feature of power semiconductor devices is their ability to withstand high voltages. While in transistors designed for microprocessors and semiconductor memories, the pressure to reduce their size to integrate more devices on a monolithic chip has resulted in a reduction in their operating voltage, the desire to control larger power levels in motor drive and power distribution systems has encouraged the development of power devices with larger breakdown voltages.

1.6.1 Definition

Devices used in power application usually switch between an open channel condition with high flow of current into the channel and a state where the gate is turned off, with almost negligible current and high voltage, the biasing condition depending on the device electrical characteristics and the load-line applied; in order to have better performances as, for example, optimal swing and extremely low leakage, the gate voltage applied is usually set lower than the device pinch-off potential V_{po}, while the drain is usually set at a high voltage.
This biasing condition requires the device gate to have strong blocking capability in order to withstand the high potential which is cause of degradation thus increasing a sub-threshold leakage currents. Leakage will increase both with voltage applied to the drain and with time, reducing the efficiency of the switching, and usually it should be at least three orders of magnitude than the device maximal output current I_{max}. Thus, referring also to literature [28][29], it is possible to define a common reference $I_{Leakmax} \approx 1\ mA/mm$ as maximum leakage current that may vary depending upon technology and composition of the devices under test. In case of higher current levels when high drain voltages are applied, destructive processes may take place, causing the degradation of electrical properties and eventually catastrophic damages to the device. The breakdown voltage BV is typically defined as the terminal voltage where a sharp increase in current occurs on the output $I - V$ characteristic; the definition given is generic because the terminal and currents considered depends upon the measurement configuration used.
A distinction is usually made between horizontal or lateral breakdown and vertical

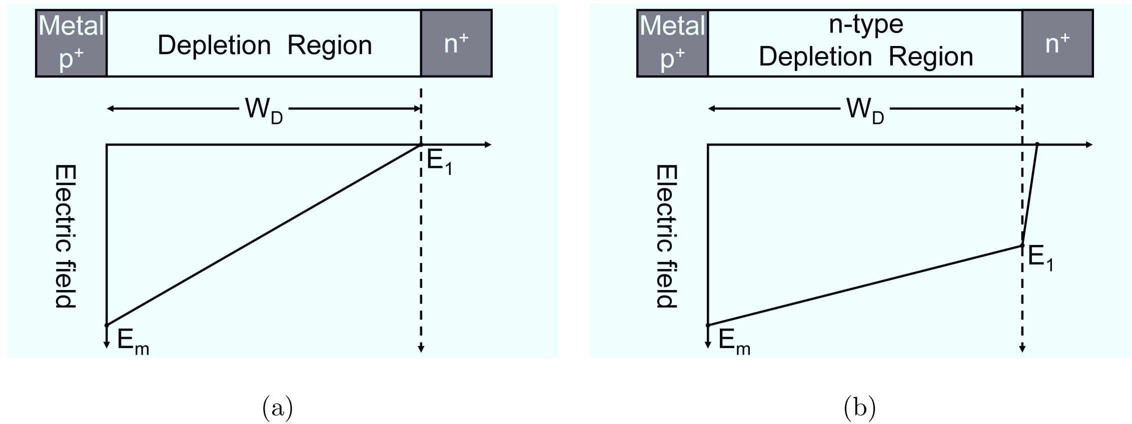
one. The former is a measure of the robustness of the horizontally designed device that involves currents flowing laterally between gate, source and drain contacts; the latter is instead defined for vertically designed devices or to study existence of current flowing from top layers through buffer and substrate in horizontally designed devices. When this phenomenon becomes relevant, the substrate bias becomes an essential element in the breakdown analysis.

1.6.2 Theoretical BV and R_{ON} calculations

In a semiconductor, the ability to support high voltages without the onset of significant current flow is limited by the avalanche breakdown. This phenomenon depends on the electric field distribution within the structure: high electric fields can be created within the interior of power devices as well as at their edges. In order to meet the breakdown voltage requirements for the application while minimizing the on-state voltage drop and hence reduce power dissipation, an optimization of power devices design must be performed [30].

Theoretical critical field and breakdown voltage

Power devices are designed to support high voltages within a depletion layer formed across either a *p-n* junction, a metal-semiconductor (Schottky barrier) contact, or a metal-oxide-semiconductor (MOS) interface. Any mobile carrier entering the depletion layer either due to the space-charge generation phenomenon or by diffusion from adjacent quasi-neutral regions, is swept out by the electric field generated by the applied voltage. As the applied voltage is increased, the electric field in the depletion region increases, resulting in acceleration of the mobile carriers to higher velocities. With further increase in the electric field, the mobile carriers gain sufficient kinetic energy, so that their interaction with the lattice atoms produces the excitation of electrons from the valence band into the conduction band. The generation of electron-hole pairs due to energy acquired from the electric field in the semiconductor is referred to as the *impact ionization*. Since these electron-hole pairs also undergo acceleration by the electric field in the depletion region, they significantly contribute to the generation of further pairs of electrons and holes. Hence, impact ionization is a multiplicative phe-



(a) (b)

Figure 1.14: *Distribution of the electric field (a) in an abrupt parallel-plane Schottky or p^+-n^+ junction (b) in a punch-through Schottky or p-i-n junction [30].*

nomenon, which produces a cascade of mobile carriers being transported through the depletion region leading to a significant current flow through it. Since the device can not sustain the application of higher voltages due to a sudden increase in the current, it is considered to undergo avalanche breakdown. Thus, maximum operating voltage for power devices is limited by the avalanche phenomenon.

The onset of the avalanche breakdown condition can be analyzed starting from the hypothesis that the voltage is supported across only one side of the structure. This holds true for an abrupt Schottky or *p*-*n* junction with a very high doping concentration on one side when compared with the other side. The analysis of a one-dimensional abrupt junction can be used to understand the design of the drift region within power devices. The case of a *p*-*n* or metal-*n* junction is illustrated in Fig. 1.14(a) where the p^+ side is assumed to be very highly doped, so that the electric field supported within it can be neglected. When this junction is reverse biased by the application of a positive bias to the *n*-region, a depletion region is formed in the *n*-region together with the generation of a strong electric field within it that supports the voltage.

Hence, considering abrupt parallel-plane junctions, the analytical solution for avalanche breakdown voltage as a function of the doping concentration N_D in the *n*-region for GaN can be expressed as [31]

$$BV_{pp} = 2.87 \times 10^{15} N_D^{-\frac{3}{4}} \tag{1.7}$$

to which is associated a maximum electric field at the junction usually defined as the critical electric field for breakdown E_C; in case of wurzite GaN [31]

$$E_C = 3.4 \times 10^4 N_D^{\frac{1}{8}} \tag{1.8}$$

In the case of some power devices, the on-resistance of the drift region is greatly reduced by the large concentration of minority carriers injected; consequently, it is preferable to use a thinner depletion region with a reduced doping concentration to support the voltage; this is called the *punch-through design*. The electric field for the punch-through design, shown in Fig 1.14(b), takes a trapezoidal shape and varies more gradually through the drift region due to its lower doping concentration and then very rapidly with distance within the n^+ end region due to its very high doping concentration. The electric field at the interface between the drift region and the n^+ end region is given by

$$E_1 = E_m - \frac{qN_D}{\varepsilon_S} W_P \tag{1.9}$$

where E_m is the maximum electric field at the junction, N_D is the doping concentration in the n-type drift region, and W_P is the width of the n-type drift region. The voltage supported is given by

$$V_{PT} = \Big(\frac{E_m + E_1}{2}\Big) W_P \tag{1.10}$$

where the small voltage supported within the n^+ end region has been neglected. The punch-through diode undergoes avalanche breakdown when the E_m becomes equal to E_C. Using this condition in eq. 1.10 together with the field distribution in eq. 1.9, the breakdown voltage for the punch-through diode is given by

$$BV_{PT} = E_c W_P - \frac{qN_D}{2\varepsilon_S} W_P^2 \tag{1.11}$$

The breakdown voltages calculated using this relationship are shown in Fig. 1.15 for GaN punch-through diodes with various thicknesses for the drift region. In performing these calculations, the change in the critical electric field with doping concentration was taken into account. For any doping concentration for the drift region, the breakdown voltage for the punch-through diode is reduced due to the truncation of the electric field at the n^+ end region; it becomes smaller as the thickness of the drift region is reduced. This reduced drift region thickness is beneficial not only for reducing the on-state voltage drop but also for reducing the stored charge and consequently the reverse recovery power loss [30].

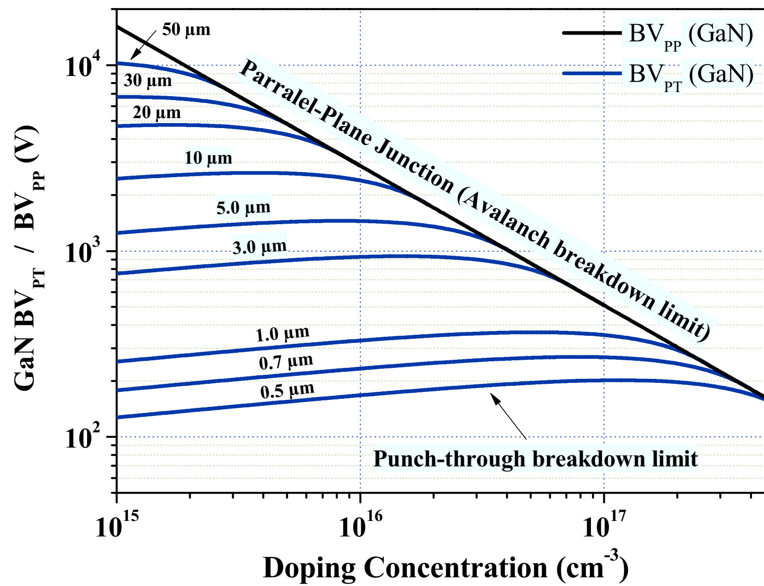


Figure 1.15: *Breakdown voltages for the P-i-N diodes with punch-through design [32].*

Theoretical limits of power devices

The semiconductor devices discussed above contain a drift region designed to support the blocking voltage. The properties (doping concentration and thickness) of the ideal drift region can be analyzed by assuming an abrupt junction profile with high doping concentration on one side and a low uniform doping concentration on the other side, while neglecting any junction curvature effects by assuming a parallel-plane configuration. The resistance of the ideal drift region can then be related to the basic properties of the semiconductor material.

The solution of Poisson's equations leads to a triangular electric field distribution

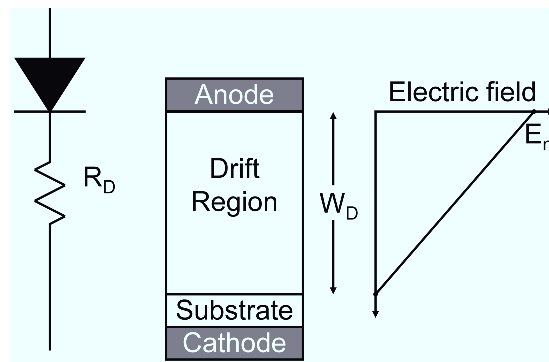


Figure 1.16: *Structure, electric field distribution and schematic of an ideal drift region [30].*

within a uniformly doped drift region with the slope of the field profile being deter-

mined by the doping concentration. The drift region can withstand an electric field lower than the critical electric field E_C. Hence the peak of the electric field E_m has to be less or equal than E_C, which, together with the doping concentration, determines the maximum depletion width W_D. The resistance of an ideal drift region of area A can be calculated using the equation [30]:

$$R \cdot A = \int_0^{W_D} \rho(x)dx = \int_0^{W_D} \frac{dx}{q\mu_n N_D(x)} \tag{1.12}$$

where μ_n is the low-field mobility, N_D is the doping concentration of the drift region and W_D is the drift region thickness. In case the region is uniformly doped, N_D is no longer dependent on the position and integrating the latter equation yields to

$$R_{ON,sp} = \frac{W_D}{q\mu_n N_D} \tag{1.13}$$

The depletion width W_D is

$$W_D = \frac{2BV}{E_C} \tag{1.14}$$

where BV is the desired breakdown voltage. The doping concentration in the drift region required to obtain this BV is given by:

$$N_D = \frac{\varepsilon_S E_C^2}{2qBV} \tag{1.15}$$

hence, the specific on-resistance is easily obtained as a function of the BV

$$R_{ONideal} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3} = \frac{4BV^2}{Baliga's\,FoM} \tag{1.16}$$

The denominator of this equation is commonly referred to as *Baliga's figure of merit for power devices*. It is an indicator of the impact of the semiconductor material properties on the resistance of the drift region. The cubic dependence of the on-resistance on the critical electric field for breakdown favors wide band-gap semiconductors such as silicon carbide and gallium nitride. Some approximations are usually applied to estimate the on-resistence [33]:

$$\begin{aligned} E_C &\propto N_D^y \\ \mu_n &\propto N_D^{-x} \\ R_{ON,sp} &\propto BV^\alpha \end{aligned} \tag{1.17}$$

where α is defined as

$$\alpha = \frac{2 - x - y}{1 - 2y} \tag{1.18}$$

which gives, for gallium nitride [31], the following approximation

$$R^{GaN}_{ON,sp} = 2.4 \times 10^{-12} BV^{2.5} \tag{1.19}$$

Using the same approximations for $6H - SiC$ [31] and $4H - SiC$ [30] it yields

$$R^{6H-SiC}_{ON,sp} = 1.45 \times 10^{-11} BV^{2.6} \tag{1.20}$$

$$R^{4H-SiC}_{ON,sp} = 2.97 \times 10^{-12} BV^{2.5} \tag{1.21}$$

respectively. In the same way, for Si [30]

$$R^{Si}_{ON,sp} = 5.93 \times 10^{-9} BV^{2.5} \tag{1.22}$$

1.6.3 Measurements techniques

Many different criteria and measurement techniques have been used in extracting values. The breakdown voltage BV can hence be defined either visually from the shape of the breakdown characteristic [34][35][36][37][38], or a given current criteria as for example when the point-by-point percent increase in the reference parameter becomes greater than a predefined value [29] or as the voltage at which the current flowing exceeds the $I_{Leakmax}$ set for the device under test [34][39][40][41][42][43][44]. Literature blossoms with many definitions depending on the measurement technique used. When a two terminals T_1, T_2 test is considered, the BV is defined as $BV_{T_1 T_2}$ and the most relevant parameter is the current flowing among the two terminals, taking into account possible parasitic paths causing additional leakage phenomena. Many authors measured gate-source BV_{GS} [34][39][36][40], configuring the drain floating and the source grounded; others the gate-drain BV_{DG} [34][39][40][42] breakdown voltage after setting source floating and drain grounded. Another way is to ground both source and drain, obtaining a voltage that is approximately the smaller between BV_{GS} and BV_{DG} [34][35][40][45].

In a three terminal test (four terminal when the substrate is considered), the most important parameter is the BV_{DS}, or its analogous BV_{DG}. The current flowing can either come from the gate current (G), the source (Ch) or the substrate (Sub), depending on

which terminal mostly contributes to the breakdown [29].
In case of a three terminal measurement an additional degree of freedom is given by the possibility to study breakdown in off- (when the device is turned off) or on-state (when the voltage applied to the gate is higher than V_{po}).

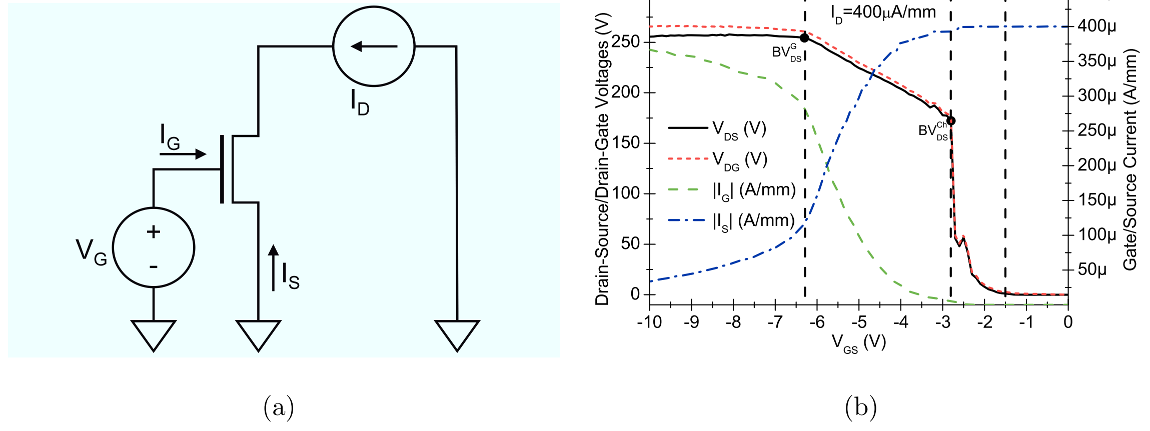
Off-state breakdown

For many applications, the off-state drain-source breakdown voltage BV_{DS} is an important parameter, that can be properly defined as the drain voltage of the turned off device with respect to the grounded source, where a sharp increase in I_D takes place on the output characteristics. Different mechanisms can jointly contribute to the breakdown, depending on environmental and technological factors as temperature, voltage and composition. It is thus impossible to have a precisely defined value for BV_{DS}, in particular due to two main reason:

- The difficulty in defining the pinch-off voltage of a device. This requires to define a unique standard to identify it and V_{po} to have a low spread. In the first case, a few methodologies are used that vary on measurement and extraction technique. On the other side, threshold voltage is technology dependent, thus being different from one to the other.

- The dependence of the breakdown voltage and V_{GS} [34], correlated to the mechanisms contributing which may activate and dominate under different biasing conditions, each one imprinting a different behavior to the phenomenon.

A breakdown measurement can be carried out performing a sweep in V_D, with gate voltage held constant and source/substrate grounded, monitoring the currents during the sweep; to avoid destruction of the devices, a compliance is set (usually $\approx 1mA/mm$) on all the currents. Unfortunately any voltage controlled technique is not reliable due to the slow activation of compliance, in this way significantly increasing the possibility of a catastrophic degradation of the device under test in most cases. For this reason a different approach has been used, sweeping the drain current instead; this avoid current runaway and destruction of the device if the range is properly selected.
A reliable technique was developed by *Bahl et al.* [28]. To characterize the breakdown, a fixed predefined current is injected into the drain, and the gate-source voltage is



(a) (b)

Figure 1.17: *(a) Schematic of the Bahl's Drain-Current Injection technique (b) example of measurements on a single-heterostructure epilayer structure.*

ramped down from a strong forward bias to below threshold, and V_{DS}, V_{DG} and I_G are monitored. The *Drain-Current Injection technique*, whose schematic is shown in Fig. 1.17(a), traces their loci versus V_G at fixed I_D on the $I - V$ plane. BV_{DS} and BV_{DG} are defined for

$$I_D = -I_G \tag{1.23}$$

that implies $I_S = 0$. It is also possible to unambiguously measure BV^G_{DS} as the maximum V_{DS} attained, irrespective of the gate voltage. Additionally, in some cases it is possible to identify the onset of the channel breakdown BV^{Ch}_{DS}. No mathematical expression can be used in this case, but it can be defined as the voltage at which a sudden decrease of the slope on V_{GS}, V_{DS} characteristics occurs, provided BV^{Ch}_{DS} greater than BV^G_{DS}. At this point it is possible to enlighten different regions Fig. 1.17(b):

1. Linear region. The device is conducting and consequently V_{DS} is very low.

2. Saturation region. V_{DS} increases rapidly; the slope is determined by the finite on-resistance of the device; the lower limit of this region is BV^{Ch}_{DS}, whether it can be identified, or BV^G_{DS} otherwise.

3. Channel breakdown region. This region is not always visible, due to the impossibility to identify a proper BV^{Ch}_{DS} in some cases; it is usually defined as the V_{GS} range from BV^{Ch}_{DS} to BV^G_{DS}. In this region, the source feeds the I_D and a channel breakdown occurs; the gate current contribution is almost negligible. As V_{GS} is

lowered, the current contribution coming from the source weakens, V_{DS} gradually increases up to its maximum until the channel is closed and from this point on the breakdown is almost completely sustained by the gate.

4. Drain-gate breakdown region. When a further decrease of V_{GS} is considered, the drain-gate voltage is no longer dependent upon the V_{GS}, while the current coming out from the drain is supplied by the gate itself; the V_{DS} decreases together with the slope of the $I - V$ characteristic.

Transitions among adjacent regions are not neat and clean, as it is possible to observe looking at the $I - V$ characteristics, but leakage mechanisms act altogether, each one with a contribution that may be significant or negligible depending on the voltage range considered.
Bahl's technique has some crucial advantages compared to others:

1. It is current controlled, and reduces the risk of device burnout due to current runaway.
2. Avoids repetitive scans, which is especially useful in unstable devices.
3. It may help to resolve or distinguish from different mechanisms that causes the breakdown.

On-state breakdown

Besides off-state breakdown, another interesting figure of merit is the on-state the breakdown, thought of as a significant upturn in the current or a rise in the output conductance. *Somerville et al.* [46] gives an insight into the techniques and issues related to the BV in on-state; moreover, studying the $GaAs$ based materials and devices, he tries to give a proper definition and develops a *Gate-Current Injection technique.* In gallium arsenide devices, carrier multiplication started by channel electrons is often considered the main responsible for the breakdown. Starting from this hypothesis, a fraction of the impact ionization generated holes move to the gate, thus increasing I_G and creating the typical bell shape. The gate current is usually some orders of magnitude lower than the drain one; thus, it is more sensitive to impact ionization effects, and can predict more accurately any sudden increase in the parameters monitored.

On-state breakdown should also converge to off-state one as the device is turned off. During the measurement I_G is set constant at an optimal value I_{Goff} where the OFF-state BV_{DS} has been previously measured, I_D is increased from I_G to a predefined value (usually 20% to 40% of I_{Dmax}), thus plotting a locus of V_D versus I_D. The on-state BV_{DS} so defined is consistent for many reasons:

1. It is consistent with BV definition given in off-state, provided the sweep starts from $I_D = I_G$.
2. A rise in the gate current means a rise in I_D. Hence, an increase in output conductance follows, and its locus is defined too.
3. The technique allows investigation of the physics lying behind.
4. It give a reasonable prediction of the device burnout.

Additional single spot measurements confirm the result of this technique to be safe and reproducible.

On-state BV_{DS} is also a useful tool to predict burnout in $GaAs$ devices. In the off-state I_G is almost purely tunneling and TFE dependent; as the drain current increases, impact ionization starts to generate holes which move to the gate. But I_G is set constant, so V_{DG} must drop. Burnout takes place at almost the same I_G, regardless of I_D so long as the device is fully on. Thus, it can be associated with the total multiplication current, efficiently monitored observing gate current characteristic. The selection criteria may depend on the technology used and on the epitaxial design of the device under test. Unfortunately, this technique cannot be applied to the GaN. In gallium nitride technology, impact-ionization is negligible; tunneling mechanisms usually dominate the gate current, which cannot be used to monitor hot electron phenomena. In order to overcome this issue, electroluminescence measurements have been used; in GaN it is due to intraband transitions of highly energetic carriers, thus it can be used as an alternative method to study hot carrier behavior under different biasing condition.

1.6.4 Mechanisms leading to breakdown

Many different mechanisms can lead to breakdown. By increasing the voltage difference at the drain terminal, the whole potential difference will increase, in this way

increasing the electric field in the device. Hence, carriers will be subject to higher electrical forces, and would drift to lower potential regions moving through intermediate potential levels until they reach the drain; the path these carriers chose to follow defines different breakdown mechanisms. The more the epilayer structure of the devices is complex, the more the probability of potential breakdown mechanisms have to be considered. The paths can be generated laterally and located into a semiconductor layer, in an insulator layer, in an interface between layers, in the ambient or even between different devices if the device insulation used, Mesa or implantation, has not properly been performed during fabrication process; or it can be vertical through the substrate, especially in n-type substrates.

Impact ionization mechanism

In off-state, leakage current is dominated by many phenomena, including tunneling, TFE and hopping; hence, off-state BV_{DS} strongly depends on them. When dealing with Si or $GaAs$ [47] technology, as the device is turned on, electrons flow through the high-field gate-drain region, where they undergo impact ionization, with a consequent production of hole-electron pairs, increasing the overall carriers; in particular, a hole fraction escape to the gate, thus increasing I_G. In semi-on biasing condition, all the phenomena jointly contributes to the gate current. When the device is finally fully on, the latter dominates, and the on-state BV_{DS} becomes quite vertical due to the exponential dependence of the impact ionization on field.
For a given biasing condition, the gate current is determined by electrons flow through the gate due to off-state phenomena and by the fraction of holes generated by impact ionization that are collected by the gate itself

$$I_G = I_{TFE} + I_{ii} \tag{1.24}$$

while off-state phenomena mainly depend on extrinsic carrier concentration, gate Schottky barrier height and biasing condition. In order to avoid extremely complex calculations that will require a detailed knowledge of the field in the channel and of the ionization rate, it is possible to use an expression experimentally verified in literature [48]

$$I_{ii} = AI_D exp\Big(\frac{-B}{V_{DG} - V_T}\Big) \tag{1.25}$$

where A is a scaling constant that depends on device design, while B has to be determined by sidegate measurements. Carrier multiplication depends linearly on the carrier flux, I_D, and has an exponential dependence on the field in the drain-gate region. The model considered properly fit both the initial drop in on-state BV_{DS} when in semi-on condition and the typical vertical behavior in fully on-state. Moreover, it gives an exact prediction of the initial rise and subsequent saturation of impact ionization that is seen in the sidegate measurements. Finally, it is a useful mean to foresee burnout, helping to identify a critical current above which constant impact ionization corresponds to constant gate current.

Increasing n_s results in much more vertical on-state BV_{DS} loci. In devices with higher n_s, off-state BV_{DS} is low, and so it is the field in the channel and the transition from off-state phenomena into impact ionization is slower, causing a slight degradation of the on-state BV_{DS}. So, decrease in n_s means off-state BV_{DS} improves, and so does the contribution of impact ionization on on-state BV_{DS} as well.

Examination of allowable load-lines makes it clear that the shape of on-state BV_{DS} is crucial to power limit for the different designs. In high n_s devices, the locus intersects the load-line close to the off-state, and the device is limited almost exclusively by gate thermionic field emission; engineering the SBH would help to improve power performances. In case n_s is low, the intersection is far from the off-state, and impact ionization dominates: other approaches, such as composite channel or reduced indium concentration should be used.

Somerville reports interesting results. $GaAs$-based devices show a negative trend for off-state BV_{DS} while increasing the temperature and a positive one for on-state BV_{DS}; on the other hand, BV_{DS} drops both in off- and on-state with the temperature when testing InP-based devices.

Given these results, while in InP the main mechanism seems to be tunneling/thermionic field emission, in $InGaAs$ in on-state, taking into consideration its positive dependence with the temperature, impact ionization has a major role. Analysis of the I_G/I_D ratio versus $1/(V_{DG} - |V_T|)$ reveals that, at lower values, a typical impact ionization behavior can be observed, with a strong dependence from I_D. At higher value, where I_D is lower, the ratio is almost constant, suggesting that an I_D independent phenomena is dominating, as tunneling/TFE [47].

Bulk threshold leakage breakdown mechanism

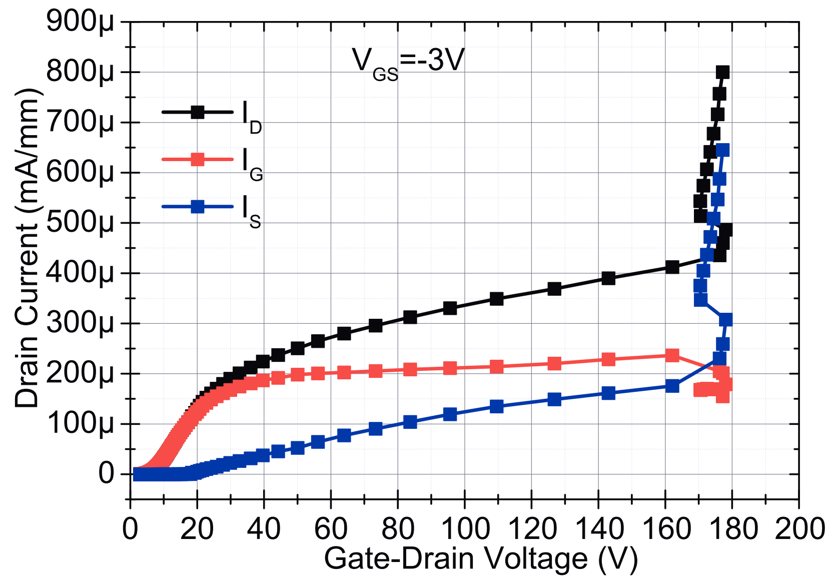


Figure 1.18: *Punch-through on a single-heterostructure HEMT. I_S (blue line) suddenly increases, due to the formation of a parasitic path along the channel.*

When a three-terminal breakdown variable current injection measurement is considered, under particular circumstances, the $I - V$ output characteristic shows a sudden increase of I_D, not followed by I_G, which eventually stays some order of magnitude lower than the drain current (see Fig. 1.18); additional two-terminal gate-drain measurements show no sudden increase of the leakage current, hence indicating that the gate does not leak, and it could not feed any possible current surge as seen in the three-terminal measurement. In the same way, when a fixed current value is forced to the drain while reducing the gate voltage from on-state to off-state, the drain voltage rapidly increase to maintain the current level imposed, but the gate one remains almost constant or decreases.

Most often, in GaN, monitoring the current coming from the source reveals that the sudden increase seen is sustained by the source, and a parasitic path is created between the two terminals through the buffer layer underneath the depletion region; thanks to the high electric field due to the high V_{DS} applied, carriers acquire high levels of energy which in some cases, depending on the epitaxial structure and on the thickness of the depletion region and on the biasing condition at the gate, can move deep into the bulk and travel to the drain. This effect is well known in literature as space charge injection

into the GaN buffer layer [49], carrier spill-over [50], or buffer layer punch-through effect [51][52].

Schottky drain reverse bias tunneling leakage breakdown mechanism

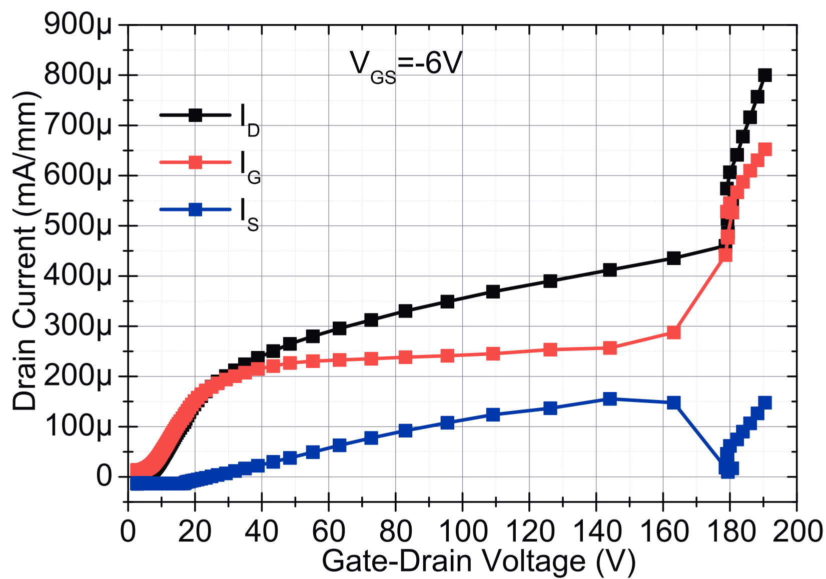


Figure 1.19: *Tunneling on a single-heterostructure HEMT. When the breakdown takes place, I_G (red line) increases, approximately following I_D due to tunneling leakage phenomena.*

As reported by many authors [53][54], tunneling leakage currents flowing through the Schottky gate in reverse biasing conditions is influenced by many factors; most important are temperature, vertical electrical field at the gate edge and the strain of the top-barrier layer. Two mechanisms dominate: tunneling from metal into the semiconductor, which the more the reverse biasing condition is severe the more it increases; the second is associated with the presence of dislocations that generate leakage current paths, often consistent with hopping phenomena or trap assisted tunneling. Fig. 1.19 show a breakdown measurement where the breakdown takes place due to tunneling phenomena through the Schottky gate contact in reverse biasing condition. When the drain current increases, the main contribution comes from the gate; at $V_{DS} \approx 180V$, a sudden surge in I_D occurs, followed by I_G.

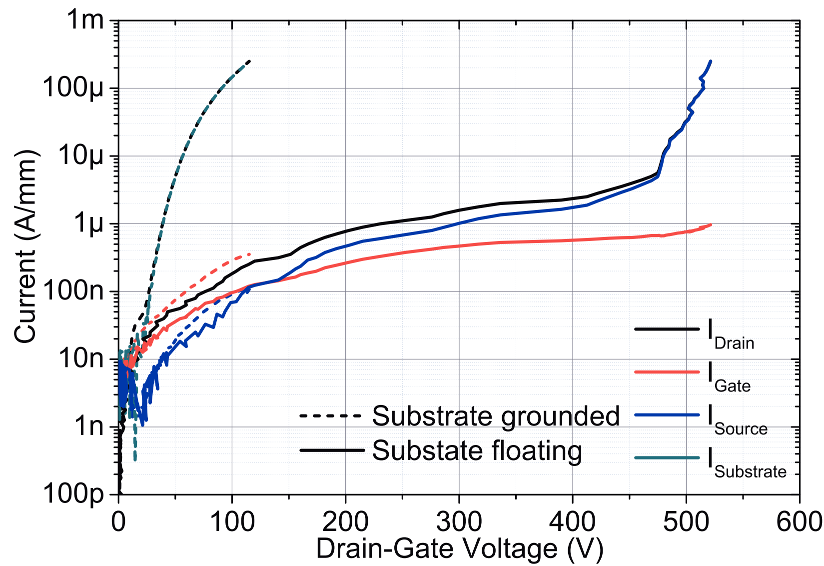


Figure 1.20: *Breakdown measured with substrate left floating(solid line) and biased to ground (dashed line) on a $L_{GD} = 15\,\mu m$ device. In the first case, the BV increase over $500\,V$. In the second it is $\approx 150\,V$; in this case the contribution to the (drain) leakage current comes from the substytate. Similar results have been found on the different epilayer designs considered.*

Substrate leakage breakdown mechanism

As previously seen, leakage phenomena are not only horizontal, but in many cases a meaningful path exists from one terminal through the substrate. This leaking path becomes extremely important when the substrate is grounded or biased. The amount of the leakage strongly depends on the ability of the substrate to isolate upper layers from the bottom; this can be improved, for example, with an optimization of the epilayer structure and the presence of additional doping into the buffer and/or the substrate itself. Fig. 1.20 shows brealdown measurements carried out on a single device with substrate floating and grounded. On the other side, when the substrate is left floating, due to a self-biasing effect, it can reach a voltage apt to create a parasitic path between source and drain [55], decreasing the BV.

Inter-device insulation leakage breakdown mechanism

Another cause of leakage is the current flowing between neighboring devices. For this reason, inter-device (Mesa)-insulation is used to hinder carrier flow to other devices; moreover, it also provides insulation at off-state conditions between source and drain ohmic contact of the device itself. Otherwise, lack of insulation can cause carriers to

find additional leaking path increasing sub-threshold leakage currents. The insulation ability strongly depends on the Mesa type insulation. Mesa recess with the use of Cl_2/BCl_3 reactive ion etching creates conductive states created at the edge of the active area used as a path to carriers in high voltage biasing conditions; also, the gate Schottky metal contact crosses the 2DEG carriers reach zone, creating gate leakage. Another technique can be used and consist in $^{14}N^{+}$ multi-energy implantation. Here it is essential the dose of the implantation: if the implantation dose is too small, it may not be effective leaving the strain of the $AlGaN$ top-barrier layer and remains of carriers reach volumes in the 2DEG; excessive implantation can cause damages, creating new conductive defects in the GaN buffer [32].

Other sources of sub-threshold leakage breakdown mechanisms

Besides the major sub-threshold leakage mechanisms, there exist additional paths that are less probable to be involved. The path between gate and drain contacts through the $AlGaN - SiN$ passivation interface and/or interfaces between silicon nitride passivation with different N concentrations are may be candidate to leakage phenomena. A common catastrophic breakdown can take place at high voltages through arcing into the air usually involving neighboring contacts of the device. Every layer added to the structure can contribute to create additional leaking path hence increasing the chances of breakdown.

1.7 Reliability Issues

Thanks to the outstanding properties of gallium nitride, the continuos development of technology has given proof of the excellent performances of GaN-based $HEMTs$ in a wide range of application, from RF to high-power switching applications. Despite the large effort spent in recent years, with a substantial increase of published papers concerning device's robustness, a gap concerning reliability aspects has still to be filled.

This gap finds its origin in part due to the continuous evolution of the technology which, even if it has greatly improved, is still far from maturity, partly due to the lack of knowledge concerning failure modes and mechanisms. A common approach to

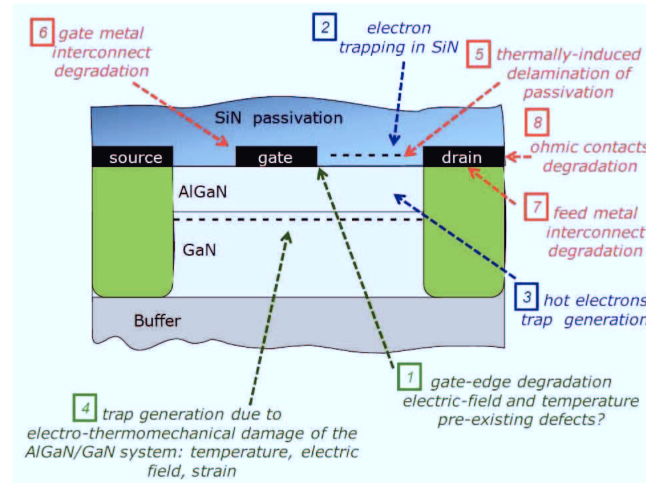


Figure 1.21: *Failure mechanisms recently identified on GaN HEMTs. In red, thermally-activated mechanisms; in blue, mechanisms related to the presence of hot electrons, which are common to all high-voltage FET; in green, mechanisms which are peculiar to GaN devices, due to the polar and piezoelectric nature of this semiconductor material [56].*

study reliability for standard semiconductor technologies is to use a three-temperature accelerated life-tests to extract the life-time of a device: devices are biased on the real operative point and, using the temperature as degradation accelerating factor, it is possible to build a diagram that provides the estimation of the life-time of a device at the real temperature and bias operation using failure times extracted.

In fact, GaN shows different degradation modes (Fig. 1.21) and has no clearly defined degradation accelerating factors or degradation laws; hence, these techniques cannot be considered reliable. Indeed, many authors do not report thermally activated failure mechanisms or negative temperature correlated failure mechanisms. Moreover, infant mortality still plague GaN technology, clearly indicating it is not still mature.

From the literature, temperature has been identified as an accelerating factor for passivation stability and for contacts degradation with metal diffusion on the semiconductor or inter-mixing of the metal layers that respectively cause variation of the Schottky barrier and of the ohmic contact; hot-electrons have been associated to trapping effects on the surface or within the semiconductor layers. Besides these effects, already encountered in other technologies, GaN materials, even due to the polar nature of the device structure, have been correlated with new degradation effects, the gate-edge degradation and bulk-trap generations.

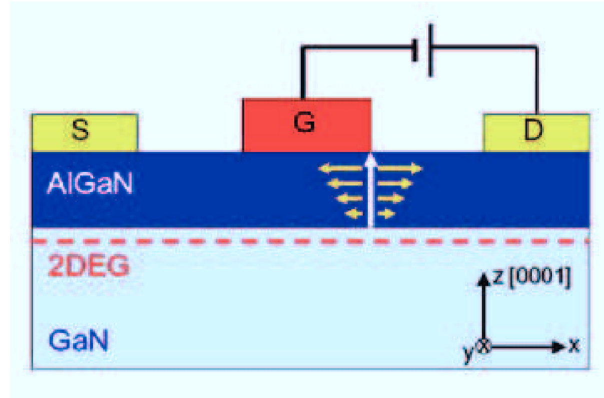


Figure 1.22: *Illustration of GaN HEMT under reverse bias between gate and drain. Mechanical tensile stress (yellow) is induced by the vertical electric field (white) through inverse piezoelectric effect. [57].*

1.7.1 Gate related degradation phenomena

When operative, GaN High Electron mobility transistor are subject to high voltages, and the electrical field can reach values of several MV/cm, with a severe condition especially at the drain-edge of the gate contact, see Fig. 1.22. The presence of defects closely located to it may favor electron migration from the metal to the $AlGaN$ barrier layer due to trap assisted tunneling. Reverse biasing the gate and progressively reducing the gate voltage, it has been reported that an abrupt increase of the leakage current takes place after a critical voltage that depends upon the technology. Before this critical point, no degradation occurs; beyond it the gate current show a non-recoverable current increase of a few order of magnitude, an increase of dispersion and sometimes an increase of the ohmic contacts parasitic resistance and a decrease of the saturation current I_{DSS} [58]. This phenomena have been widely studied in literature [59][60]. Many authors reported a correlation between increase of current collapse effects and increase in leakage currents, that suggests formation of traps in the $AlGaN$ barrier close to the gate edges, where the field has its peak. *Joh et al.* [59] explain it using the concept of converse piezoelectric effect. The model takes into consideration the piezoelectric nature of GaN and $AlGaN$ materials and the extremely high vertical electric field within the barrier layer in the normal $HEMT$ application. Indeed, the latter is subjected to significant in-plane tensile stress (with stored elastic energy) due to the polarization contributions, both spontaneous and piezoelectric, even without bias.

When a reverse bias is applied, the vertical component of the electric field at the gate-edge sharply increases, thus enhancing the tensile strain and the stored elastic energy, particularly at the edge of the gate where the field reaches its maximum value. Once a certain critical level of stored elastic energy or strain is reached, crystallographic defects can be produced in the *AlGaN* especially at the points where the sum of the intrinsic and the applied field is maximum. These defects can then promote the injection of electrons from the gate into the AlGaN barrier layer, through a trap-assisted tunneling mechanism, inducing parasitic paths for the leakage current increase. Consequently, defects can degrade the electrical characteristics of the transistors by affecting transport properties or by inducing trapping effects. Shen demonstrated that relaxation, although only partial, of the *AlGaN* barrier causes degradation of both 2DEG mobility and carrier concentration. Once injected, electrons traveling through the the *AlGaN* barrier acquire extremely high energy levels, which they relax when entering or traveling into the channel due to intra-band transition that generates electroluminescence signal that can be captured with an electroluminescence microscope. Thus, each jump visible in the current characteristics, caused by carrier injection, can be correlated with formation, or increase, of hots spots, usually associated with weak points correlated to existing of generated defects. This gave birth to various failure analysis techniques, in particular Transmission Electron Microscopy analysis (TEM), to try to confirm the failure mechanism with a clear signature of the material defect creation. In fact, using TEM, it is possible to identify crack and pits [61][62] in between gate and *AlGaN* barrier layer, usually located in the the drain side of the gate contact, whose formation is enhanced by time and temperature.

1.7.2 Hot electron induced degradation

The high-voltage breakdown and the high current capabilities can allow device operation with the simultaneous presence of very high power levels. In this condition electrons are accelerated by the high electric-field can reach energies much higher than the equilibrium value. These hot electrons can overcome energy barriers, dissipate energy colliding with the crystal lattice and hence create defects or dangling bonds which may act as deep levels or traps. Hence, hot electron can cause degradation processes

and trapping phenomena within the passivation or GaN layers. The interaction with the $AlGaN$ layer can indeed enhance the crystal defect propagation and increase the vertical leakage but so far there is no clear evidence. In $GaN-HEMT$ technology, the impact-ionization is negligible and the gate current, usually dominated by tunneling injection mechanisms, cannot be used as a hot-electron indicator.

An alternative method for hot electron evaluation comes from the electroluminescence measurements (EL). EL is usually due to intra-band transitions of highly energetic electrons. In GaN devices, this is not due to band-to-band recombination, but typically associated with hot-electrons accelerated by the high longitudinal electric-field in the channel, which scatter with charged centers releasing the energy in the form of photons [63, 64]. At low V_{GS} below the pinch-off voltage, the drain-to-gate voltage is maximum inducing the maximum electric-field; but, due to the absence of electrons in the channel, the emission intensity is zero. Increasing the gate voltage, the carriers start flowing and are simultaneously accelerated by the high electric-field in the gate-drain region, thus increasing the light emission in particular at the drain-edge of the gate, where electric-field reaches its peak. But at the same time, the increase of the gate voltage causes the decrease of the drain-to-gate voltage and consequently of the electric field. When the carrier increase can no longer balance the electric field reduction, EL intensity decreases. Increasing the drain voltage, the EL keeps the same bell-shaped behaviour, but it increases its intensity with a near-exponential trend, and it slightly shifts the V_{GS} corresponding to the EL-peak, depending on the different trade-off between electron concentration and electric field intensity at higher drain voltages. Therefore, the electro-luminescence measurements at different gate voltages gives an efficient method for the hot-electrons evaluation.

In the recent years, hot-electron degradation has been proposed as the dominant failure mechanism on $GaN-HEMTs$ just in few works. *Coffie et al.* [65] have presented a RF-power degradation with a negative activation energy, typical of hot-electron induced degradation. *Meneghesso et al.* [66] have shown bigger performance reduction on semi-on state stress with respect to on-state (higher temperature) and off-state (higher electric field) stress, followed by a remarkable slow-trapping phenomena especially at the highest current tests.

Chapter 2

Devices description

During this work, many different epilayer designs have been tested. The analysis has involved both depletion-mode and enhancement mode wafers.
The normally-on wafers here considered have no doping; some of them have n-type SiC substrate, others have been grown on semi-insulating SiC and have an additional $5 \cdot 10^{18}\, cm^{-3}$ Si-doped capping layer. Epilayer designs include single-heterostructures and double-heterostructures. All the informations relative to their structure are reported in Table 2.1. The only exception consists in a different single-heterostructure wafer, hereafter labelled $SH : BV$, whose epilayer design cannot be given; devices from this wafer have been used for some tests on the breakdown, and it will be stated in the breakdown results chapter.
As far as normally-off devices are concerned, available wafers include single heterostructures with different buffer dopings (carbon or iron) or with no doping at all, double-heterostructures and an improved heterostructure using an $AlGaN$ back-barrier grown over a carbon doped buffer. Other differences include the availability of a capping layer, doping with a rare gas into the substrate and the application of a $p - GaN$ gate. Table 2.2 summarizes the characteristics of the normally-off wafers epilayer structure.

Table 2.1: *Epilayer structure of normally-on wafers.*

Wafer ID	Substrate	Nucleation	Buffer	Back-barrier	Channel	Barrier	Cap	Gate
SH-A	SiC	AlN	GaN	-	-	$AlGaN$	-	-
	n-typ	$360\,nm$	$2400\,nm$	-	-	$30\,nm$ 23%	-	-
SH-B	SiC	AlN	GaN	-	-	$AlGaN$	-	-
	n-type	$360\,nm$	$1750\,nm$	-	-	$30\,nm$ 25%	-	-
SH-C	SiC	AlN	GaN	-	-	$AlGaN$	GaN	-
	semi-ins.	$50\,nm$	$1550\,nm$	-	-	$17\,nm$ 25%	$5\,nm$, $5 \cdot 10^{18}$	-
DH-D	SiC	AlN	-	$AlGaN$	GaN	$AlGaN$	-	-
	n-type	$360\,nm$	-	$1840\,nm$, 5% Al	$15\,nm$	$30\,nm$, 23 % Al	-	-
DH-E	SiC	AlN	-	$AlGaN$	GaN	$AlGaN$	GaN	-
	semi-ins.	$350\,nm$	-	$1600\,nm$, 5 % Al	$35\,nm$	$18\,nm$ 25% Al	$5\,nm$, $5 \cdot 10^{18}$	-

Table 2.2: *Epilayer structure of normally-off wafers.*

Wafer ID	Substrate	Nucleation	Buffer	Back-barrier	Channel	Barrier	Cap	Gate
SH:C	SiC	AlN, $300\,nm$	$GaN:C$, $3100\,nm$, $2\cdot 10^{18}$	-	GaN	$AlGaN$	$3\,nm$	-
	n-type				$100\,nm$	$13\,nm$, 23% Al	$5\cdot 10^{18}$	-
DH:C	SiC	AlN, $100\,nm$	$GaN:C$, $3150\,nm$, $2\cdot 10^{18}$	$AlGaN$	GaN	$AlGaN$	-	$p-GaN$
	n-type	UID GaN, $1\,\mu m$		$500\,nm$, 5% Al	$35\,nm$	$14\,nm$, $23\,\%$ Al	-	$100\,nm$
DH	SiC	AlN, $100\,nm$	-	$AlGaN$	GaN	$AlGaN$		$p-GaN$
	n-type			$3560\,nm$, $5\,\%$ Al	$35\,nm$	$14\,nm$ 24% Al		$103\,nm$
DH+Ar	SiC	AlN, $300\,nm$	-	$AlGaN$	GaN	$AlGaN$	-	$p-GaN$
	n-type			$3560\,nm$, 5% Al	$35\,nm$	$14\,nm$, $24\,\%$ Al	-	$103\,nm$
	Ar^+ impl.		-	-	-			-
SH:Fe	SiC	AlN, $80\,nm$	UID GaN, $200\,nm$			$AlGaN$		$p-GaN$
	n-type		$GaN:FE$, $2070\,nm$, $2\cdot 10^{18}$			$14\,nm$ 23% Al		$102\,nm$
			UID GaN, $1\,\mu m$					-
SH:Fe+Ar	SiC	AlN, $80\,nm$	UID GaN, $200\,nm$			$AlGaN$		$p-GaN$
	n-type		$GaN:FE$, $2070\,nm$, $2\cdot 10^{18}$			$14\,nm$ 23% Al		$102\,nm$
	Ar^+ impl.		UID GaN, $1\,\mu m$	-	-			-

Chapter 3

Parasitics

Even if it has proved excellent performances, *GaN* technology still suffers from current collapse due to trapping effects at the surface or/and in the buffer. This instability causes the increase of the R_{DSon}, which can be defined as the ratio V_{DS}/I_{DS} in linear region, in dynamic mode during the switching on.
Unfortunately, in this way the R_{DSon} contributes to losses in the real application, and it consequently must be reduced in order to improve the efficiency in the switching mode power supply. Thanks to the high voltage and high current dynamic R_{DSon} set-up developed, it is possible to perform such measurements giving a direct feedback to the epitaxy and to the technology development team.

3.1 Performances

3.1.1 Normally-on devices

A basic characterization has been carried out on the normally-on devices. All

Table 3.1: *Parameters extracted from normally-on measurements.*

Parameter		SH-A	SH-B	SH-C	DH-D	DH-E
I_{Dmax}	A/mm	720	750	680	430	570
V_{po}	V	$-2.6\,V$	$-2.5\,V$	$-1.5\,V$	$-1.7\,V$	$-0.8\,V$

devices from *SH* wafers show comparable maximum output currents (see Fig. 3.1

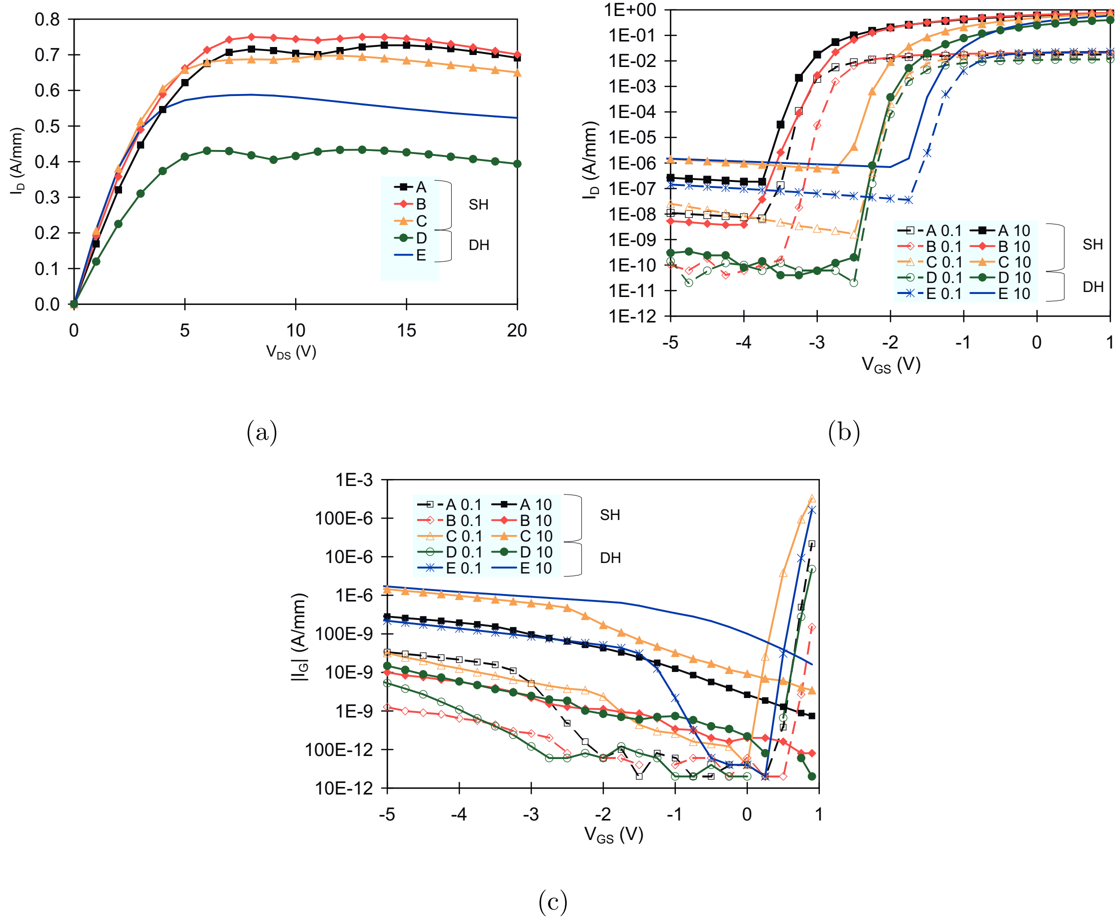
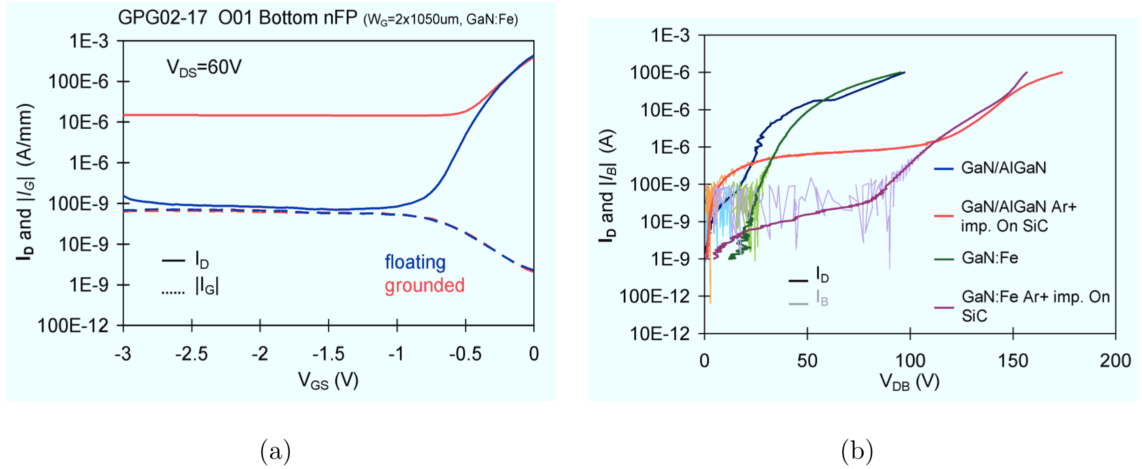


Figure 3.1: *DC characterization of normally-on devices: (a) output comparison of* $L_{GD} = 6\,\mu m$ *devices at* $V_{GS} = 1\,V$ *(b)* I_D*–*V_G *and (c)* I_G*–*V_G *comparison of* $L_{GD} = 6\,\mu m$ *devices* $V_{DS} = 0.1\,V$ *(dashed line) and* $10\,V$ *(continuos line).*

and Table 3.1). While wafer $SH-A$ and $SH-C$ report similar values both in on- and off-state conditions, $HEMTs$ from $SH-B$ have gate leakage currents 2 order of magnitude lower; V_{po} is -2.6 V and -2.5 V for $SH-A$ and $SH-B$, -1.5 V in devices from wafer $SH-C$. In DH $HEMTs$ maximum output currents are substantially lower than SH; gate leakage currents are $10^{-11}\,A/mm$ and $10^{-8}\,A/mm$ for the former, $10^{-9}\,A/mm$ and $10^{-6}\,A/mm$ in the latter in on- and off-state respectively. Threshold voltage is $-1.7\,V$ for wafer $DH-D$, $-0.8\,V$ for $DH-E$. $DH-D$ devices, grown over n-type SiC substrate and without capping, show some interesting effects, see Fig. 3.1(b) and Fig. 3.1(c). The first is very low sub-threshold currents, which are ≈ 3 order of magnitude lower than other devices at $V_{DS} = 10\,V$; moreover, threshold voltage is less sensitive to V_{DS} changes, that means also minor Drain Induced Barrier Lowering ($DIBL$) effect, hence improved robustness of devices blocking capabilities. Finally,



(a) (b)

Figure 3.2: *Leakage currents for DH and SH:Fe, implanted and not, epilayer strucutures.*

the double-heterostructure reduces n_s, causing a shift of V_{po} towards positive voltages. The application of the capping layer causes an additional positive V_{po} shift.

3.1.2 Normally-off devices

DC characterization carried out on normally-off wafers report interesting results. Carbon doped devices show good performance, but with the drawback of high leakage currents. Among the other wafers, *SH:Fe* wafers have higher I_{DS} and R_{ON} but lower V_{po} than *DH* wafers. Substrate implantation, performed using rare gas Ar^+ to avoid introducing unintentional n/p-type doping, has negligible effects on *DC* characteristics and parameters in *SH:Fe* wafer. *AlGaN/GaN/AlGaN* devices report different behaviors whether they have been implanted or not: implanted devices have lower I_{DS} and higher V_{po}. Moreover, non-implanted *GaN:Fe* and *AlGaN/GaN/AlGaN* have the same order of sub-threshold current; such a similarity is visible for implanted devices too. A small difference is present between non-implanted and implanted wafers. Ion-implanted wafers report an additional reduced peak in the transconductance at lower voltages than the main one. Further investigations are necessary to fully understand the nature of this peak.

As can be seen on Fig. 3.2(a), an increase of drain leakage in off-state (I_{Doff}) in $I_D - V_G$ curves on grounded *SiC* substrate devices; on n-type substrate devices, an additional conductive vertical path connect the top layers to the *SiC*, and hence current can flows through the substrate; the phenomenon is more pronounced (approximately one order

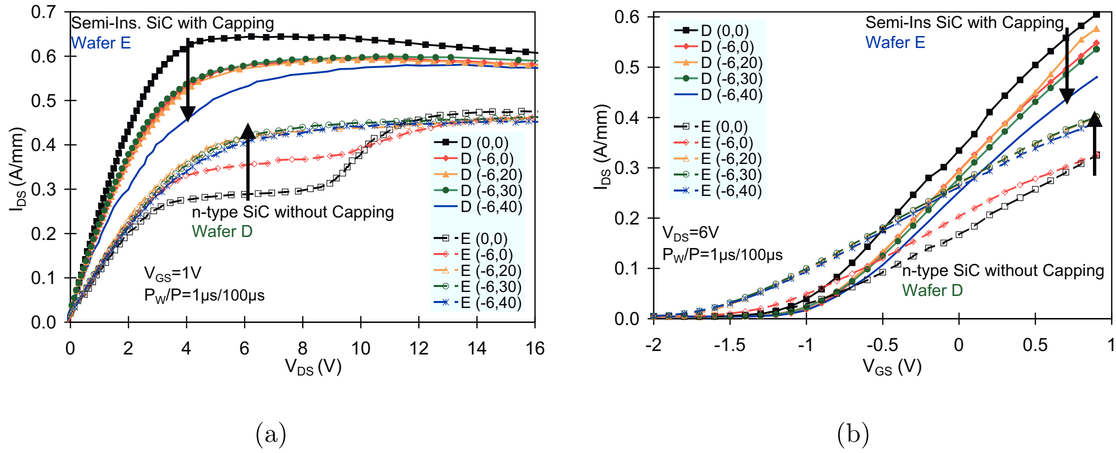


Figure 3.3: *Comparison of dinamic measurements results between n-type SiC substrate devices (dashed line) and those with semi-insulating substrate and capping layer (solid line). Test carried out report the results do not depend on the presence of an AlGaN back barrier.*

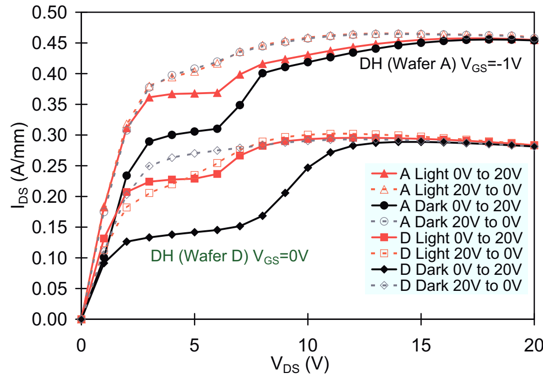


Figure 3.4: *Comparison of DC measurements results between SH (dashed line) and* 15 nm *channel DH (solid line). Both the epilayer structure have n-type SiC substrate and no capping.*

of magnitude) on *SH:Fe* than the *DH*. In both cases, the Ar^+-implantation effectively suppress the substrate current. Fig. 3.2(b) shows the leakage flowing through SiC substrate carried out in the different epilayers structures. Clearly Ar^+-implantation significantly improve the vertical leakage current; this technique introduces new traps due to displacement damage of the impinging ions. These traps capture electrons flowing through the substrate consequently reducing the overall vertical current.

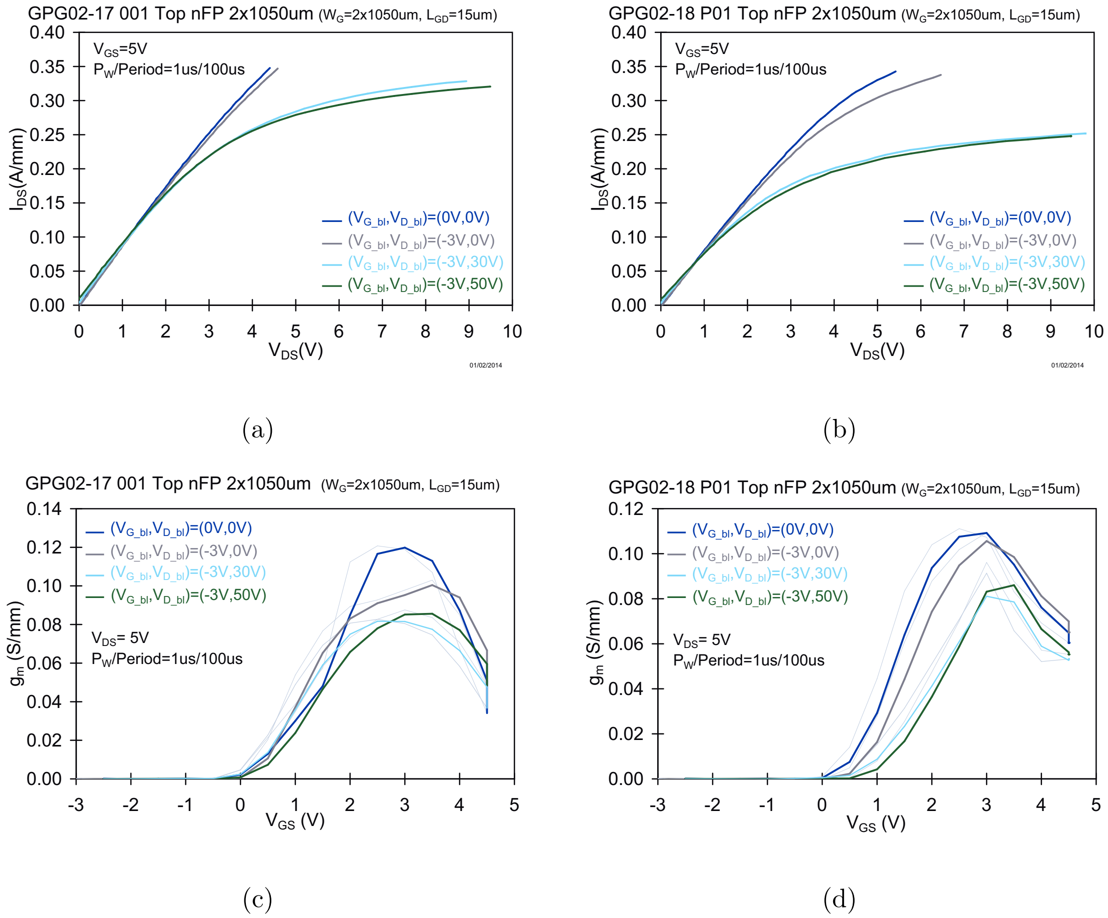
3.2 Trapping and instability

3.2.1 Normally-on devices

Pulsed measurements were carried out by using a custom DIVA-like system. Results have enlightened on two different behaviors. Current collapse in most of the wafers is lower than 15 %. Devices grown over n-type SiC, which are also uncapped, show a pronounced kink phenomena that disappear by increasing the bias drain voltage in off-state condition V_{Dqbp} (Fig. 3.3(a)). Those with semi-insulating SiC substrate do not have such kink effecting pulsed condition. Kink is attributed to electron trapping in the buffer under the gate, since it is due to a threshold voltage shift only (see dashed lines in Fig. 3.3). In these devices, at high V_{DSqbs}, field assisted detrapping phenomena occur hence removing trapped electrons and consequently the kink effect. Hence charge trapping in the buffer layer is removed, and no kink can be observed.
To better understand kink phenomena, measurements sweeping V_{DS} from $0\,V$ towards higher voltages light improves I_D due to photo-assisted detrapping (Fig. 3.4); during sweep from high-to-low voltages no relevant kink is present, thanks to the previous high field assisted detrapping during the low-to-high V_{DS} sweep. The n-type SiC is more prone to kink effect that can hence be attributed to the substrate.

3.2.2 Normally-off devices

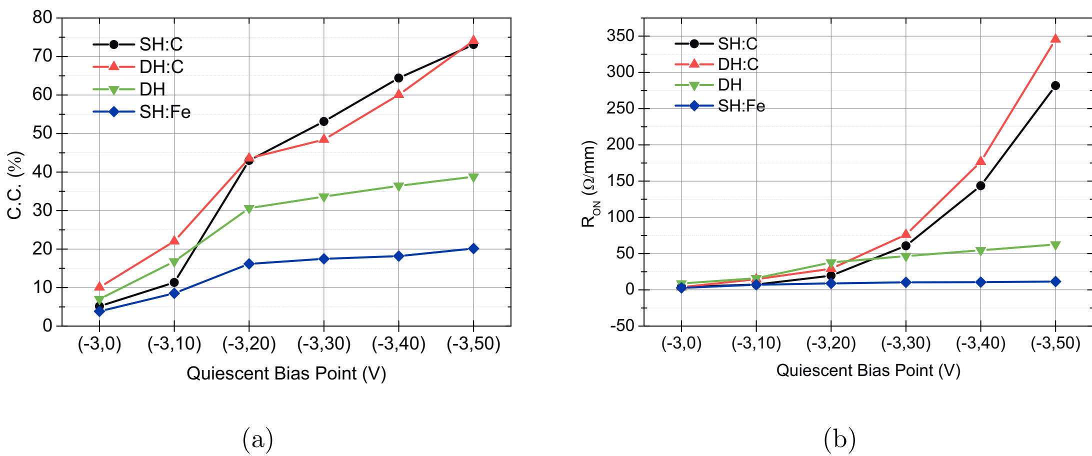
In normally-off devices, Ar^+-implantation on SiC seems to cause a consistent threshold shift in both *AlGaN/GaN/AlGaN* Double Heterostructures and Single Heterostructure with Iron compensation wafer (Fig. 3.5); this suggests increased traps population into the buffer layer under the gate; no differences are visible in the reduction of the transconductance peak, suggesting no alteration of the trapping in the access regions.
In C-doped wafers, peak reduction and R_{ON} increase are caused respectively by trapping in the access regions and into the buffer under the gate. Current collapse and R_{DSon} grow and transconductance drops steeply while increasing the V_D of the quiescent bias point as reported in Fig. 3.6, suggesting that Carbon-doped devices greatly suffer from trapping effect with respect to *DH* undoped or *SH:Fe* doped ones.



(a) (b)

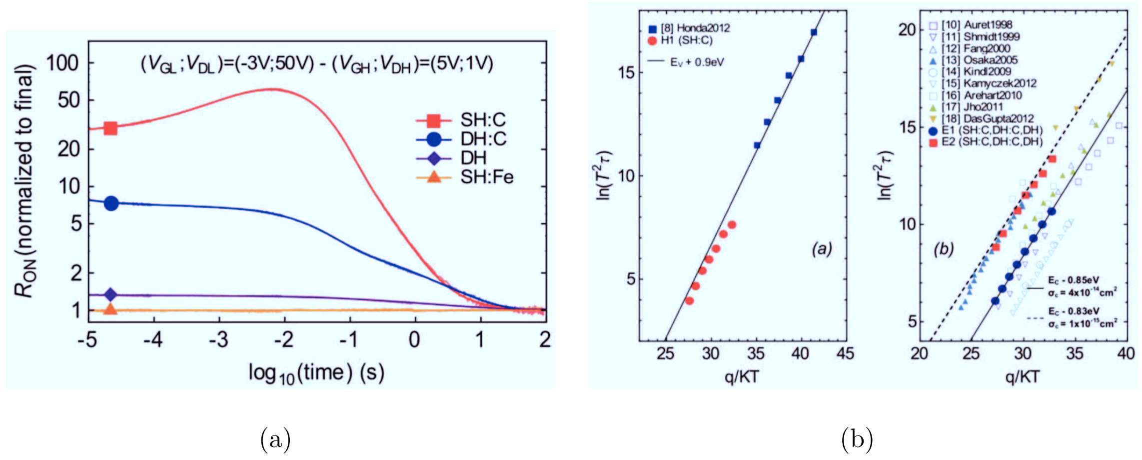
(c) (d)

Figure 3.5: *Pulsed measurement carried out on SH:Fe with n-type SiC (left) and Ar^+ ion-implanted SiC (right).*



(a) (b)

Figure 3.6: *Comparison of the current collapse and on-resistance varying the quiescent bias point.*



(a) (b)

Figure 3.7: *(a) R_{DSon} transients performed on SH:C, DH:C, DH, SH:Fe and (b) activation energy associated to H_1 (detected only in the SH:C devices), E_1 and E_2 (detected in the SH:C, DH:C and DH devices).*

The comparison between the normalized R_{DSon}-transient, see Fig. 3.7, performed on one representative device for a subset of the available wafers, show interesting results. *DH:C* samples display a much lower initial dynamic R_{DSon} collapse, suggesting that the introduction the *AlGaN* back-barrier is beneficial for the suppression of the dynamic R_{DSon} collapse. A further improvement is obtained through the use of double heterostructure devices without any Carbon doping. An almost complete suppression of the R_{DSon} collapse was obtained by using the single-heterostructure devices with iron-buffer compensation.

R_{DSon} transient has been measured at different temperature in order to extract the traps activation energy. The results of the current transients for the $SH:C$, $DH:C$, and DH samples, reveal the presence of three distinct processes, here referred as H_1 (detected only in the *SH:C* devices), E_1 and E_2 (detected in the *SH:C*, *DH:C* and *DH* devices), which are thermally activated.

The deep-level H_1, modeled as a deep-acceptor state and located at ($E_V + 0.84\,eV$, $\sigma = 3 \times 10^{-13}\,cm^2$) within the band-gap, could be ascribed to the deep-acceptor states intentionally introduced by the Carbon-doping. E_1 ($E_C - 0.85\,eV$, $\sigma = 4 \times 10^{-14}\,cm^2$) and E_2 ($E_C - 0.83\,eV$, $\sigma = 10^{-15}\,cm^2$) (detected in the *SH:C*, *DH:C* and *DH* samples), which compete with H_1 by inducing a decrease in dynamic R_{ON}, reveal similar signature with both *GaN* and *AlGaN*-related defect-states. Although the *DH:C* samples have a Carbon-doped buffer, samples do not display the signature of the Carbon-related

H_1 trap. This result suggest that $AlGaN$ back-barrier placed between the GaN channel and the Carbon-doped GaN buffer effectively reduces the possibility of trapping carriers at Carbon-related impurities.

Chapter 4

Breakdown

4.1 Dependency of the breakdown BV on the gate voltage

Off-state breakdown measurements have been carried out on $SH : BV$ wafer by means of a semiconductor parameter analyzer: logarithmic drain current sweeps have been executed at several gate voltage level, starting from a low V_{GS} biasing condition up to a gate voltage close to pinch-off. Currents contributions coming from gate, drain and source have been separately evaluated, in the attempt of achieving a detailed description of the breakdown process.
Results of current-controlled $I_D - V_D$ measurements indicate that devices can operate in a sustainable breakdown condition. Breakdown is reached when the drain current approaches a critical level. Above this level, the slope of the $I_D - V_D$ curve shows a rapid increase, and the voltage is usually almost pinned at BV_{DS}. For low gate voltage levels, in the whole analyzed voltage range, drain and gate currents are almost equal; no meaningful contribution to the breakdown process comes from the source. In this condition, when the gate is at high negative bias, the channel region is almost completely depleted and no significant current can flow between source and drain.

For low gate voltage levels, in the whole analyzed voltage range, drain current is almost equal to gate current, while source current gives no significant contribution to the breakdown process; when the gate is at high negative bias, the channel region is depleted and carriers flow between source and drain is negligible. Based on previous

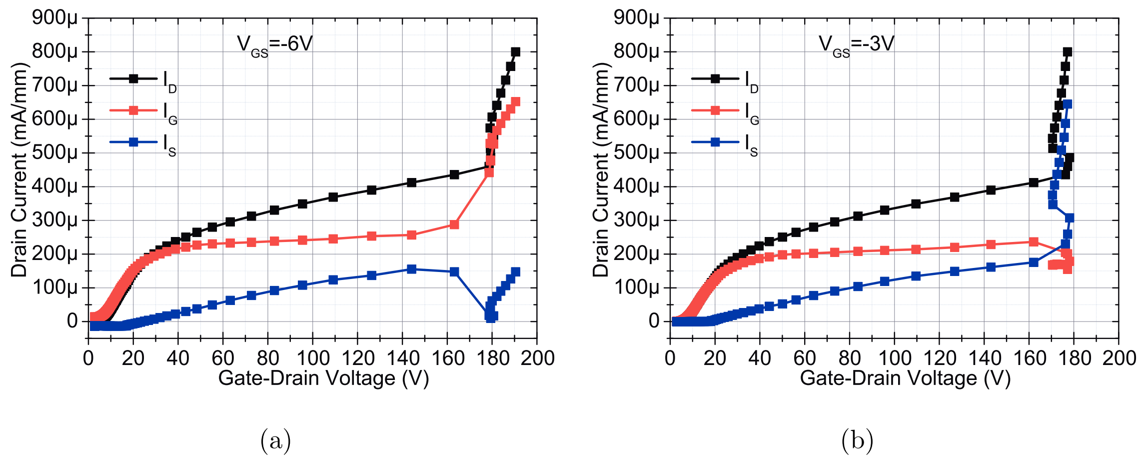


Figure 4.1: *Measurements carried out on AlGaN/GaN HEMTs with an n-type silicon carbide substrate. The devices have a gate-source distance of* $0.8\,\mu m$*, a gate-drain distance of* $4\,\mu m$*, a gate length of* $0.5\,\mu m$*, and a gate width of* $100\,\mu m$*. The pinch-off voltage of the analyzed devices is* $-2.6\,V$*.* I_D *critical level is* $\approx 455\,mA/mm$*, while the* $BV_{DS} \approx 180\,V$ *at* $V_{GS} = -6\,V$*.*

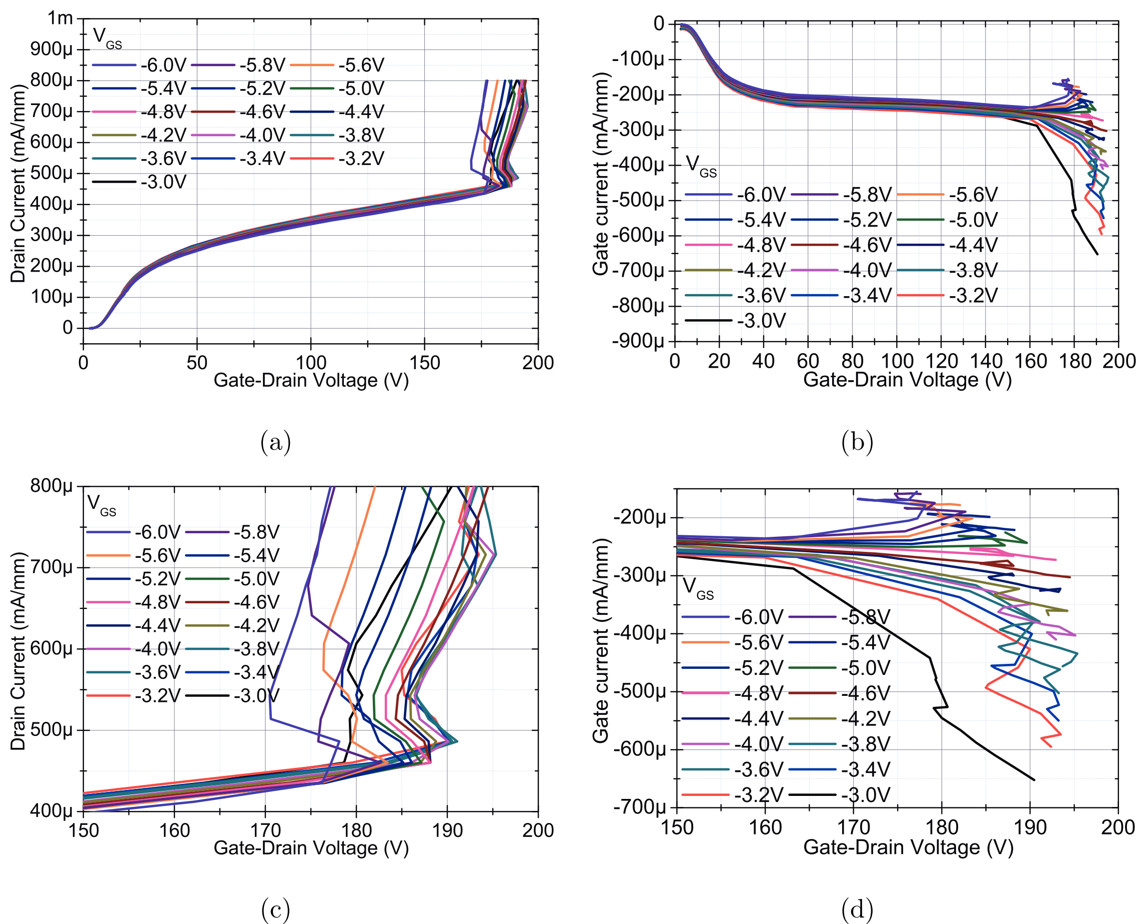
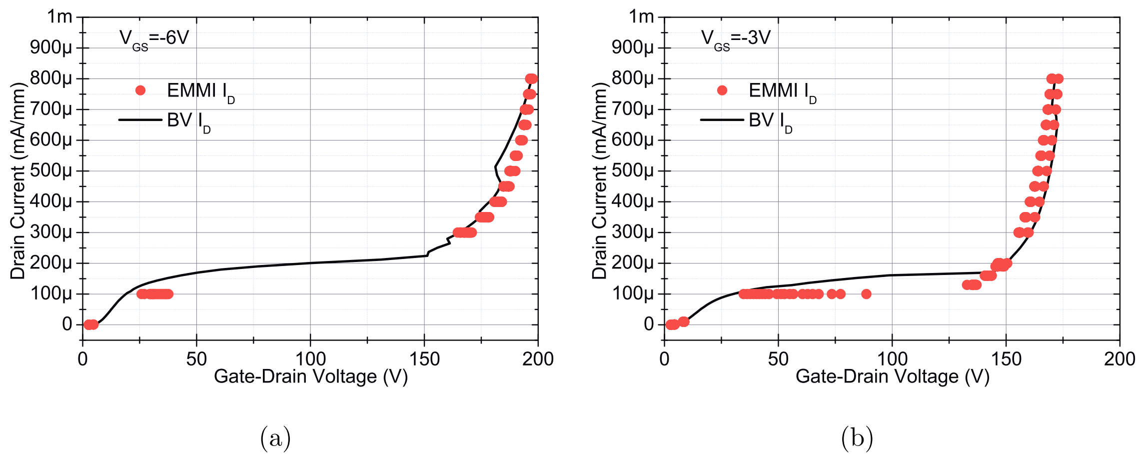


Figure 4.2: *Evolution of* BV_{DS} *current characteristics (a)* I_D *(b)* I_G *and (c) (d) their behavior in BV range, while increasing* V_{GS} *from* $-6\,V$ *to* $-3\,V$*, step* $0.4\,V$*.*

literature reports, the following two theories can be used to explain the fact that breakdown (drain) current is almost completely sustained by gate current: (i) when V_{GS} is significantly lower than the pinch-off voltage, gate-drain leakage dominates the drain current flowing. Several leakage conduction mechanisms, such as thermionic emission [54], tunneling-induced current [54], or surface hopping [53], altogether contribute to the overall leakage current. Beyond a critical drain voltage level, breakdown may occur due to a hopping mechanism [53], in this way causing a steep increase in I_D. (ii) at high drain voltage levels, impact ionization may occur due to the injection of electrons from the gate (gate-injection [54]) and it may eventually, when V_{DS} get close to BV_{DS}, cause a significant increase in breakdown current. On the other hand, results indicate that, for gate voltage levels close to the pinch-off, breakdown current almost completely comes from the source, and a negligible contribution is feed from gate. This behavior can be explained by considering that with increasing gate voltages, the depth of the space charge region is significantly reduced. Hence, a parasitic path between source and drain may become possible, due to the space-charge injection (or punch-through) of electrons in the GaN layer.

4.2 Electroluminescence measurements



(a) (b)

Figure 4.3: *$V_{GS} = -6\,V$ and $-3\,V$ EMMI measurements carried out on AlGaN/GaN HEMTs with an n-type silicon carbide substrate. The devices have a gate-source distance of $0.8\,\mu m$, a gate-drain distance of $4\,\mu m$, a gate length of $0.5\,\mu m$, and a gate width of $100\,\mu m$. The I_D current during EMMI tests shows a V_{DS} shift to higher voltages due to breakdown walkout.*

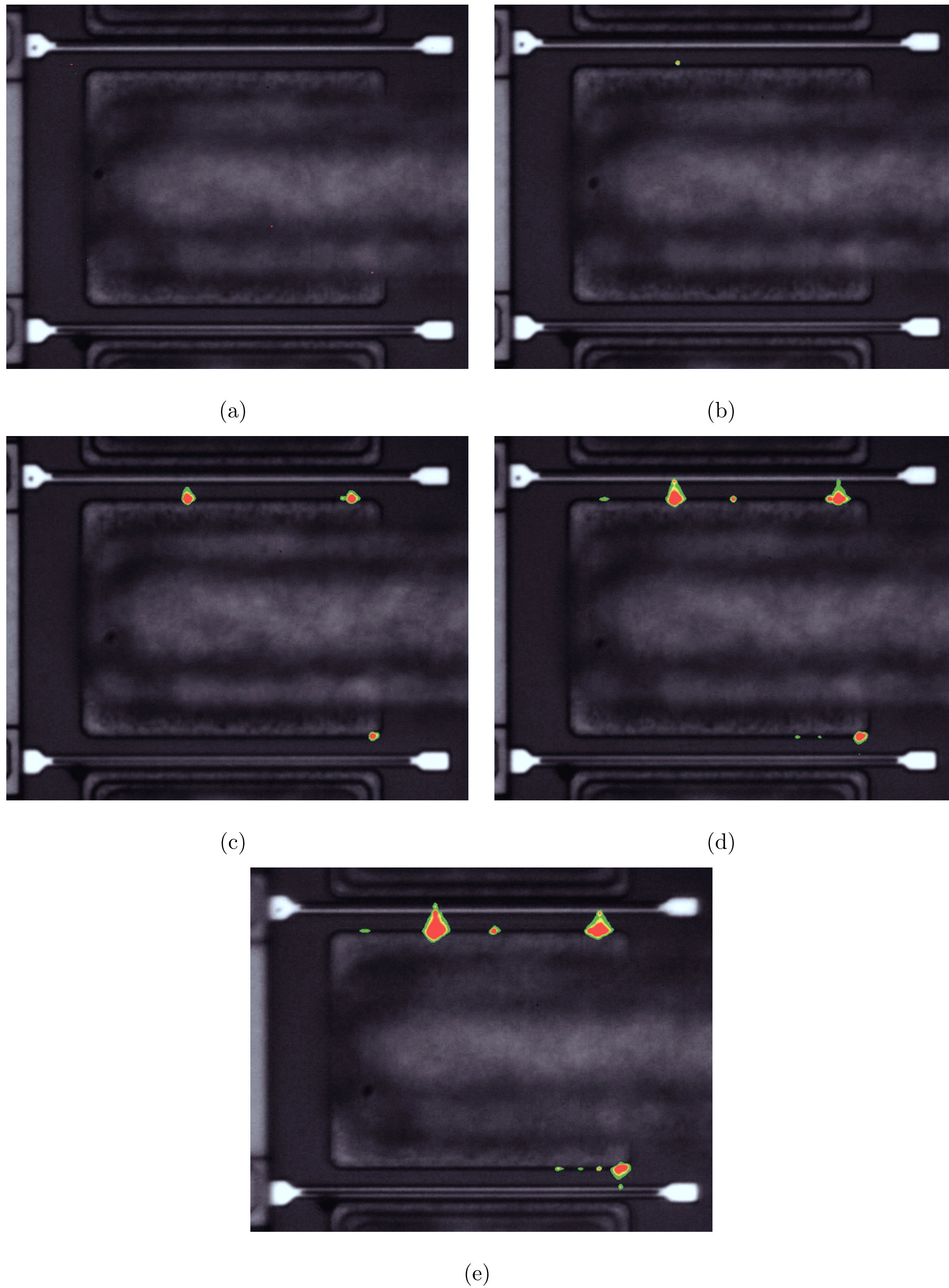


Figure 4.4: *EMMI Images show the main hot spots at $V_{GS} = -3\,V$ (a) $I_D = 0.1\,\mu m$ (b) $I_D = 130\,\mu m$ (c) $I_D = 300\,\mu m$ (d) $I_D = 550\,\mu m$ (e) $I_D = 800\,\mu m$.*

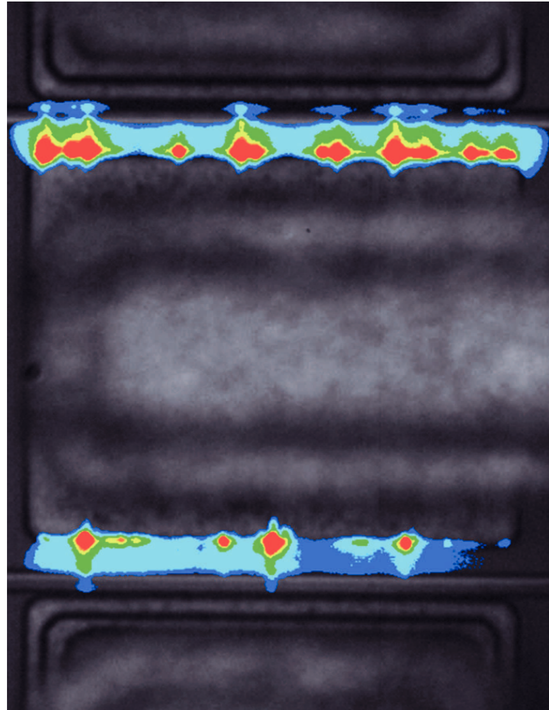
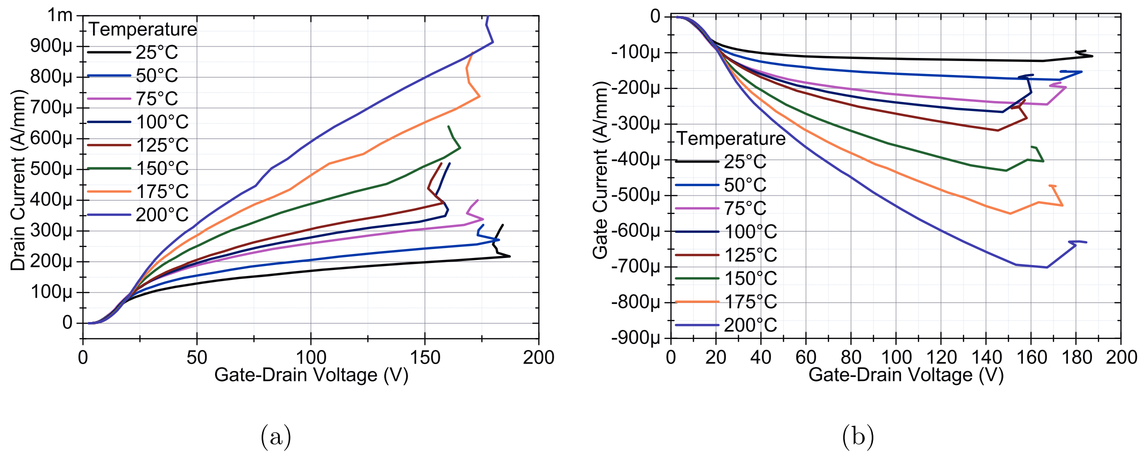


Figure 4.5: *False color EMMI image showing the spatial distribution of emission, from blu (low intensity) to red (high emission intensity).*

Electroluminescence investigation has been carried out to gain further insight into the physical origin of the breakdown phenomena: the emission pattern of the devices was measured both at $V_{GS} = -3$ and $-6\,V$. Results (Fig. 4.3 and Fig. 4.4) indicate that when the $HEMTs$ are biased in sustainable breakdown conditions, a significant light emission is detected along the width of the gate. Comparing the results at the same biasing condition, emission patterns measured at the two gate voltage levels, $V_{GS} = -3\,V$ and $V_{GS} = -6\,V$, are quite similar, despite the origin of breakdown current is different.

This result suggests that, independently of the origin of breakdown current, the highly accelerated electrons (either coming from the gate if $V_{GS} = -6\,V$, or from the source if $V_{GS} = -3\,V$) injected towards the drain may release their excess energy (in proximity of the drain) by emitting visible light. It is worth noticing that emission originates from several hot spots distributed all along the width of the gate: these spots represent preferential breakdown sites, and possibly correspond to weak areas originated by defects formation during layer deposition and/or processing.



(a) (b)

Figure 4.6: *Temperature measurements carried out ranging from* $25^{\circ}\,C$ *to* $200^{\circ}\,C$ *on AlGaN/GaN HEMTs with a silicon carbide substrate. The devices have a gate-source distance of* $0.8\,\mu m$*, a gate-drain distance of* $4\,\mu m$*, a gate length of* $0.5\,\mu m$*, and a gate width of* $100\,\mu m$*. Two different BV trends are visible: a low temperature one and a high temperature one those temperature coefficient is negative and positive respectively.*

4.3 Effects of temperature on the BV

To achieve a better understanding of the origin of breakdown, $I_D - V_D$ characterization in current-controlled mode at several temperature levels has been carried out. Results obtained with $V_{GS} = -6\,V$ are summarized in Fig. 4.6: similar results were obtained also at $V_{GS} = -3\,V$. With increasing temperature, a significant increase in the leakage current components was detected (see Fig. 4.6(b), for voltages smaller than 150 V). Remarkably, despite the strong increase in gate leakage current, breakdown can be detected in the whole analyzed temperature range, as a sudden increase in drain current. It is clear from measurements results in Fig. 4.6 that the breakdown voltage has a non-monotonic dependence on temperature: with increasing temperature up to $100\,^{\circ}C$, BV decreases from $\approx 170\,V$ to $\approx 155\,V$, thus showing a negative temperature coefficient. On the other hand, a further increasing of the operating temperature causes BV increases to 186V; at higher temperature range, a positive temperature coefficient has been found (see Fig. 4.7(b)).

The non-monotonic behavior seen so far can find a possible explanation in the co-existence of two different mechanisms. Increasing temperature between 30 and $100\,^{\circ}C$, significantly increases gate-drain leakage current components, and this determines a decrease in the breakdown voltage; these results and explanation are coherent to what ob-

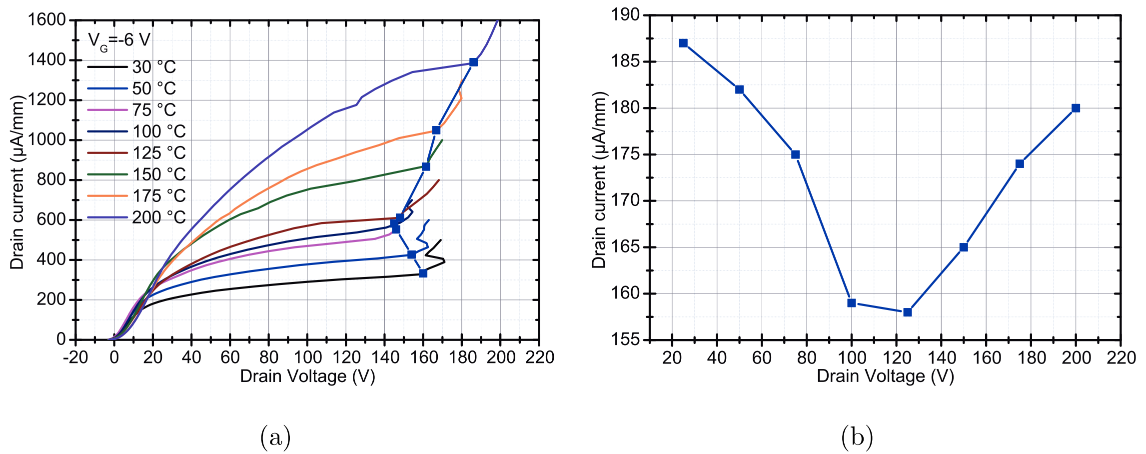


Figure 4.7: *Temperature measurements carried out ranging from 25° C to 200° C on AlGaN/GaN HEMTs with a SiC substrate. Two different BV trends are visible: a low temperature one and a high temperature one those temperature coefficient is negative and positive respectively.*

served in [53]. Concerning the increase in breakdown voltage detected for $T > 100\,°C$, the following considerations can be made: previous reports suggested that breakdown current may partly originate from impact ionization. Under this assumption, the increase in temperature causes a decrease of the impact ionization rate because of the increased lattice vibrations; hence breakdown would be more difficult and this would result in a positive temperature coefficient in the high temperature region.

A contribution of impact ionization to the total breakdown current can not be ruled out, considering the very high electric fields applied to the devices in sustainable breakdown conditions. However, experimental results suggest that, at high temperature levels, breakdown current originates from a different mechanism, i.e., an increased drain-source leakage. This can be understood by analyzing Fig. 4.8: consistently with what described in Fig. 4.2, results in Fig. 4.8 indicate that in the temperature range between 30 and $100\,°C$, the contribution of source-drain current is negligible, compared to gate-drain current components. On the other hand, for temperatures greater than $100\,°C$ (and high drain voltages) source-drain leakage starts contributing to the breakdown current (see the curves measured at $200\,°C$ in Fig. 4.8). The positive temperature coefficient of breakdown voltage in the high temperature region ($T > 100\,°C$) can be possibly explained by considering that with increasing temperatures, the conduction of electrons through the buffer can be limited by the increased phonon scattering, which results in a reduction of electron mobility. Due to such mobility reduction, source-

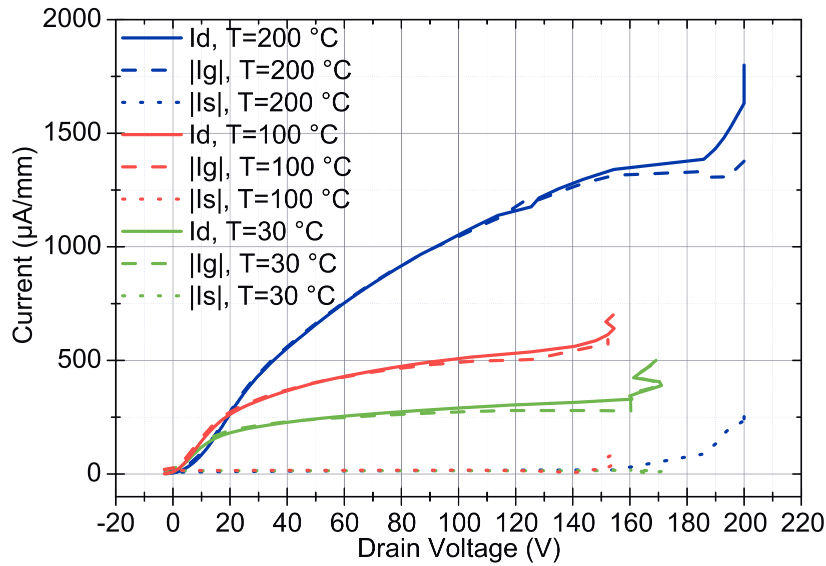


Figure 4.8: *Temperature measurements carried out at different temperature. Drain, gate and source current are visible.*

drain current contribution to the breakdown current weakens, and BV consequently improves.

4.4 Influence of double-heterostructure and doping

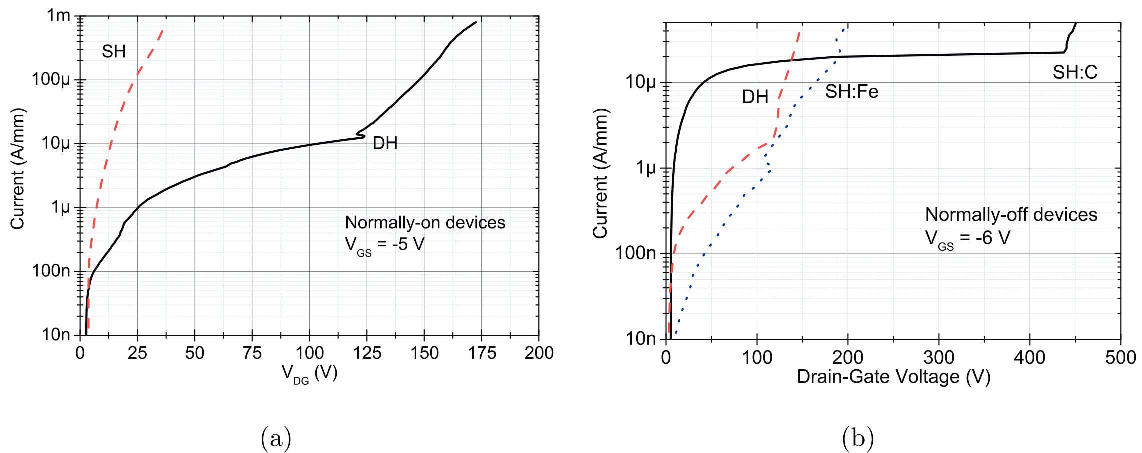


Figure 4.9: *Comparison at $L_{GD} = 3\,\mu m$. (a) normally-on SH and DH devices; BV measured at $800\mu A/mm$ (b) normally-off SH:C, SH:Fe, DH; BV measured at $50\mu A/mm$.*

Fig. 4.9 show a comparison among normally-on $SH - A$ and $DH - D$ wafers for $L_{GD} = 3\,\mu m$. Results show a meaningful improvement on BV when an additional $AlGaN$ back-barrier layer is used with respect to the standard GaN, regardless of the

geometrical parameters of the devices under test. For the conventional GaN buffer layer the channel volume under the gate is totally depleted by the gate induced field; while increasing the drain-gate voltage, if the electric field is high enough, the electrons can acquire a high energy level and easily bypass this field and travel through the buffer layer to the lower potential regions. In DH-$HEMTs$ the presence of the $AlGaN$ back-barrier layer causes the formation of an energy barrier towards the buffer layer and hence prevents the majority of the carriers from spilling over into the $AlGaN$, thus leaving the channel layer. This reduces the sub-threshold drain-leakage current and postpones the punch-through of the buffer layer. The height of the energy barrier at the channel/back-barrier interface can be engineered setting the Al concentration during growth process as can be seen in [29].
Analogous measurements have been carried out for normally-off $SH : C$, $SH : Fe$ and DH devices; results are reported in Fig. 4.9; comparison among wafers show that doping is more efficient than the DH structure in improving the breakdown. In wafers with a doped buffer a different phenomena is taking place. The deposition of a doped GaN buffer layer introduces traps and defects in the lattice structure. In off-state biasing condition these doping-induced traps contribute in capturing carriers flowing to the drain: this reduces the overall current, and, moreover, an additional barrier is created, thus further reducing the leakage phenomena. The effect of these additional traps may improve with increasing the bias at the drain, while their de-charging time constant may be long enough to guarantee a stable barrier against undesired charge flow. In particular carbon doping seems to be extremely effective as a shield [67][55].

4.5 Scaling with gate-drain length

An analysis of gate-drain length variation on the breakdown voltage has been carried out on normally-on $SH - A$ $DH - D$ devices (Fig. 4.10), considering both single- and double-heterostructure. Devices with a single-heterostructure have a lower breakdown voltage. For SH devices, BV_{DS} was found not to improve with increasing gate-drain length; the small variations reported are related to process variability and are independent from the parameter considered. On the other hand, double-heterostructure devices showed a much higher BV_{DS} value, increasing with gate-drain distance: $\approx 40\,V/\mu m$.

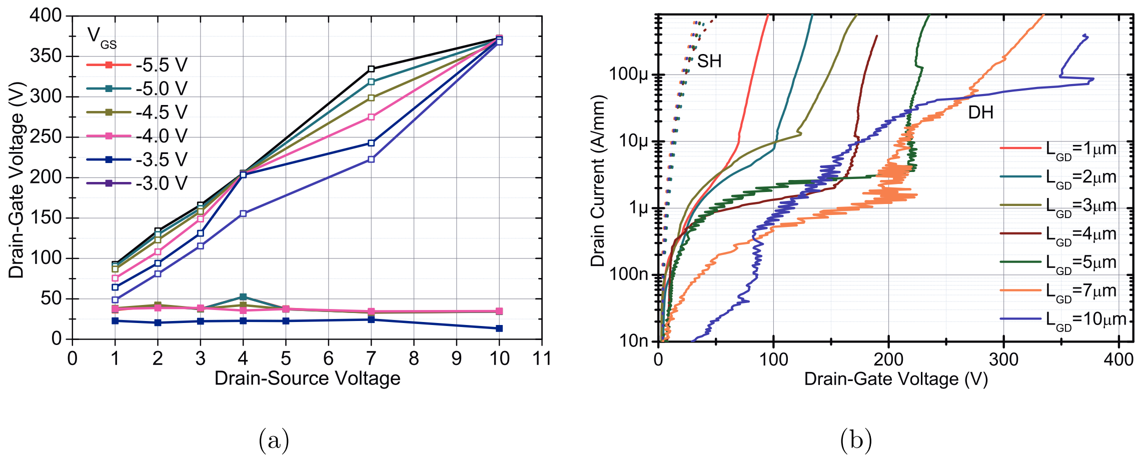


Figure 4.10: *Measurements carried out on normally-on SH and 15 nm channel DH HEMT devices with a n-type SiC substrate. The devices have a L_{GS} of 1 µm, a L_{GD} between 1 and 10 µm, a L_G of 0.5 µm, and a W_G of 2×125 µm. The pinch-off voltage of the analyzed devices is -2.6 V and -1.7 V for SH and DH devices respectively.*

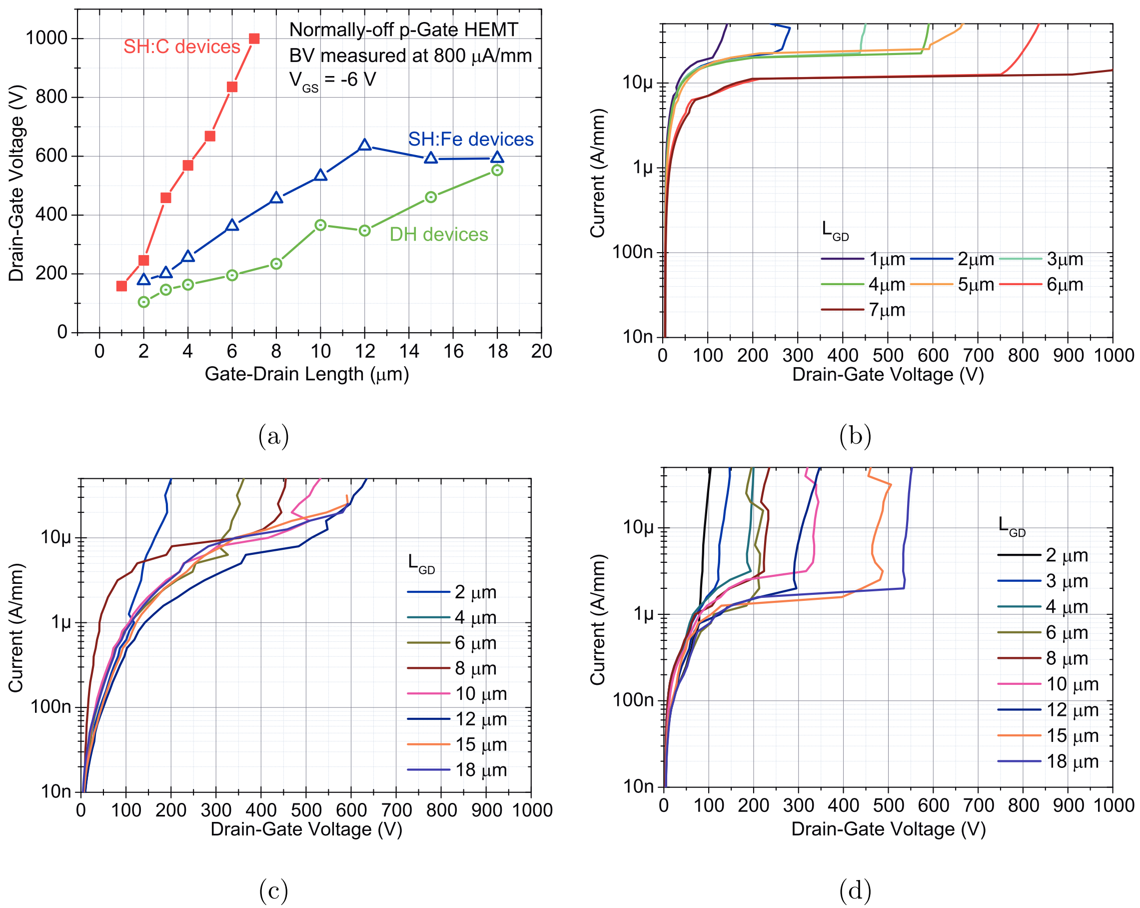


Figure 4.11: *Measurements carried out on normally-off SH:C, SH:Fe and and 35 nm channel DH HEMT devices ($L_G = 1$ µm, $L_{GS} = 1$ µm, $L_{GD} = 1$ to 18 µm and $W_G = 2 \times 125$ µm) with a n-type SiC substrate.*

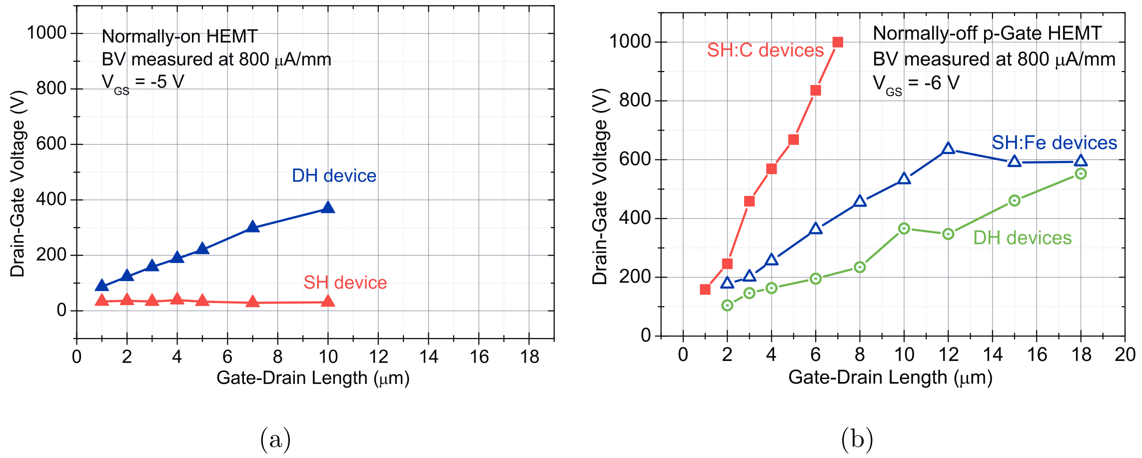


Figure 4.12: *Scaling with L_{GD} of breakdown on (a) normally-on (BV measured at $800\,\mu A/mm$) and (b) normally-off (BV measured at $50\,\mu A/mm$) devices.*

This is consistent with the results reported in [68]; the increase here reported is common to all gate bias conditions considered, with a profile almost linear within the range of gate-drain distance here considered.

Similar measurements have been carried out on normally-off devices, once again in the subset of $SH : C$, $SH : Fe$ and DH (Fig. 4.11). Both single-heterotructure reports better results than double-heterostructure; in Fe- doped devices, the BV improves over $600\,V$ and eventually saturates at for gate-drain distances greater than $12\,\mu m$. Results on $SH : C$ wafer report the best results: optimal V/L_{GD} slope, and at $7\,\mu m$ the breakdown is already beyond $1000\,V$, the capability of the instrumentation used. DH has reduced improvement with scaling and saturates at higher gate-drain distance; the maximum BV_{DS} range between $550\,V$ and $600\,V$.

An explanation of the two very different behavior can be given as follows. In case of an undoped single-heterostructure, the electron bypass is mainly dependent of buffer material properties; the influence of geometrical device variations such as gate-to-drain distance is then negligible, which results in the observed non-scaling with L_{GD}. In the case of double-heterostructure $HEMTs$, a high potential barrier in the GaN channel/$AlGaN$ back-barrier layers interface generated by the band-gap difference and the accumulated negative polarization charge shifts punch-through at much higher voltages. For short gate-drain length, the influence of V_{DS} on the buffer layer potential barrier is strong, thus giving a strong scaling between L_{GD} and V_{DS}. As the V_{DS} increases the buffer layer interface potential barrier reduces and eventually allows elec-

trons to flow into the buffer layer resulting in punch-through. For large L_{GD}, the impact of a varying V_{DS} on the potential situation at the gate area is smaller. The potential barrier is rather dominated by the gate potential. The scaling between L_{GD} and V_{DS} is then much weaker than in the case of short L_{GD} and eventually saturates for sufficient long gate-drain distances. This saturation is confirmed experimentally [68]. Tests carried out on *p-gate* devices confirms the good results obtained DH epi-layer designs, but the traps induced by lattice disorder due to doping into the buffer work as a better barrier to reduce phenomena that cause the breakdown. While in *DH*, once the energy barrier is overcome, the electrons can freely move along the whole channel length, traps are almost uniformly distributed into the whole channel length, thus electrons can be captured at any point in the channel, with the result of a much better isolation on the *GaN* doped region, may the doping be *C* or *Fe* [55].

4.6 Effects of different *SiC* substrates

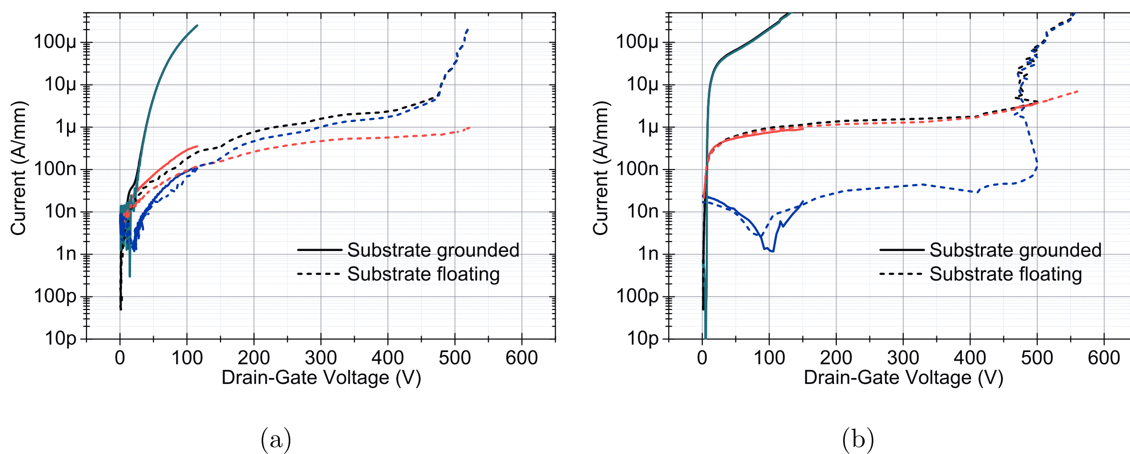


Figure 4.13: *Measurements carried out on normally-off HEMT devices grown over a n-type SiC substrate: (a)* 35 *nm channel DH (b) SH:Fe devices.*

Additional tests have been performed to study the effect of substrate biasing, see Fig. 4.13. A subset of normally-off devices ($SH : Fe$ and DH with and without with a semi-insulating Ar^+ ion-implanted substrate and $SH : C$) have been measured with substrate grounded and with substrate left floating. Considering the data collected, it can be easily understood that, with grounded substrate, the BV, in $SH : Fe$ and DH designs, strongly decreases to value ranging between $150\,V$ and $250\,V$ depending

on the epilayer structure considered; moreover, the main contribuition to breakdown current comes from the substrate; this indicates the formation of a vertical parasitic path as the n-type SiC substrate has a poor isolation capability. It is worth noticing that a difference is visible between the first measurement carried out and any other subsequent measurement in devices with substrate grounded; a reduction of the BV, that seems to be permanent, occurs in almost all the samples tested, indicating a possible degradation of the substrate itself, with a further reduction of the already poor isolation capability. Only in $SH:C$ devices that show no meaningful difference and no breakdown takes place in the whole voltage range analysed (up to $1000\,V$).
Tests on wafers with a semi-insulating Ar^+ ion implanted substrate show a significant improvement of the BV: the implantation causes dislocation damage introducing lattice disorder into the upmost region of the lattice. The use of a rare gas grant that no n-/p-type unintentional doping that could cause the formation of additional leakage paths. Implantation in this case did not degrades electrical properties of the device except for a small increase in R_{ON} [55], and positively works against the vertical current due to improved electrons trapping.

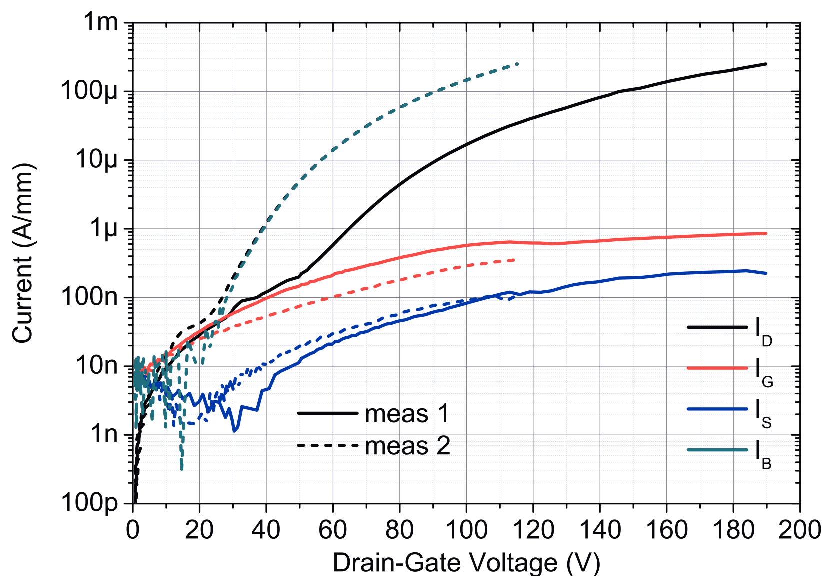


Figure 4.14: *Repeated BV measurements on a devces. A negative shift of the BV is visible.*

Chapter 5

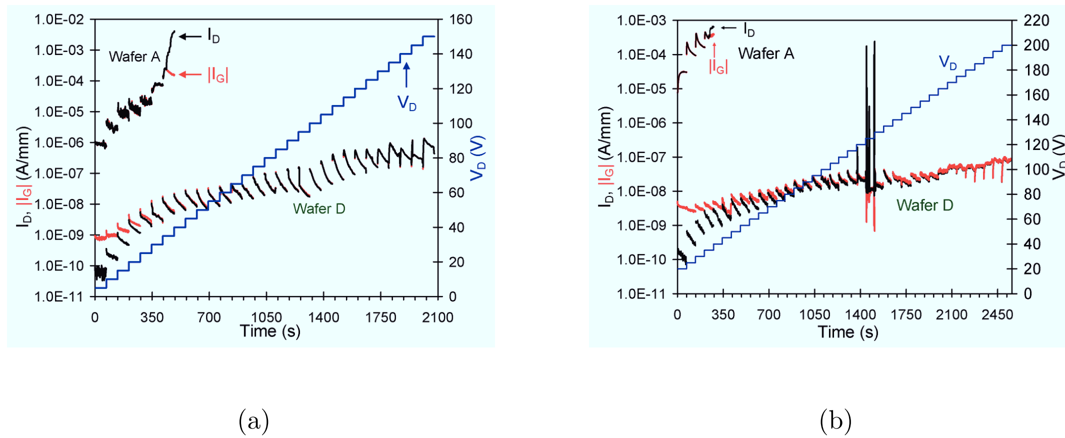
Reliability

5.1 Off-state step stress

The recent development of $GaN - HEMT$ technology has highlighted the very good material properties and the excellent device performances that make the GaN an excellent candidate for both RF and high-power switching applications.
Several groups have devoted to create devices with long-lasting electrical characteristics that could satisfy market requests of reliable applications in both areas. Despite the continuos attempts, this target is far from being achieved, mainly due to the continuos evolution of GaN technology from one side, and the limited knowledge so far acquired in failure mechanisms associated with gallium nitride.

5.1.1 Normally-on devices

The reliability of $SH - A$ and $DH - D$ devices has been preliminarily evaluated by means of off-state step-stress. With a constant gate voltage of $V_G = -5\,V$, which has been set in order to bias the device under test in an off condition far from V_{po}. In *SH-A* devices V_D was increased from $5\,V$ to $200\,V$, with steps of $5\,V$ steps, while in *DH-D* devices, V_D was increased from $20\,V$ to $200\,V$, with steps of $5\,V$ steps. Each stage of the step-stress experiment had a duration of $70\,s$. Electroluminescence images have been taken during each step with an exposure time of $60\,s$. Devices with $L_{GD} = 3\,\mu m$ and $6\,\mu m$ have been tested, see Fig. 5.1(a) and Fig. 5.1(b) respectively.
Results indicate that single-heterostructure samples suffer from a much lower robust-



(a) (b)

Figure 5.1: *Comparison between normally-on SH and DH epilayer design of I_D and I_G currents during off-state voltage step stress (a) $L_{GD} = 3\,\mu m$ (b) $L_{GD} = 6\,\mu m$. SH devices show the same failure voltage, regardless of the gate-drain distance. Failure voltage in DH samples instead show a very good scaling with L_{GD}, with a slope $\approx 50\,V/\mu m$.*

ness, since they start showing severe degradation at a drain voltage of $35\,V$; also, they do not show any improvement with increasing the gate-drain distance, since both $L_{GD} = 3\,\mu m$ and $L_{GD} = 6\,\mu m$ degrade at $35\,V$ (Fig. 5.1). Degradation is represented by a large increase of the drain current, which is not correlated to an analogous variation in gate current. Hence, it follows that the total amount of leakage current after degradation is bypassing the gate region in this way indicating buffer leakage effects, see Fig. 5.2. Moreover, the comparison between pre- and post-stress DC measurements indicates that stress induced an increase of leakage currents.

Analysis of the electroluminescence images shows that no measurable electroluminescence signal has been detected on the devices before the execution of the stress experiments, but during step stress it enlightens the formation of bright hot spots in correspondence with abrupt changes in drain currents as reported in Fig. 5.3. The presence or appearance of these hot spots indicates the existence of weak points in the device, due usually to formation of defective areas during device fabrication; there regions are more sensitive to biasing condition, and more prone to degradation. The longer the dwell time and the more severe the biasing condition are, the faster their degradation is, with consequent formation of additional leakage paths that induce sudden increase in leakage currents, easily spotted in the I_D and I_G characteristics with the afore mentioned abrupt changes, or jumps.

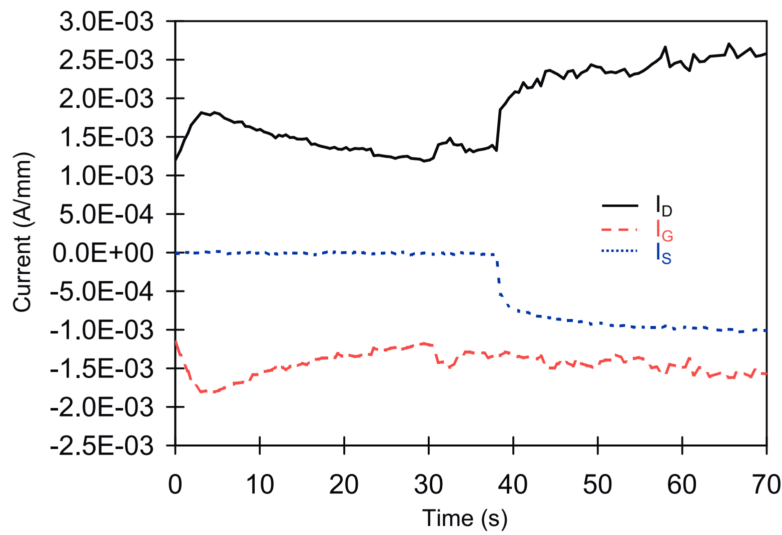
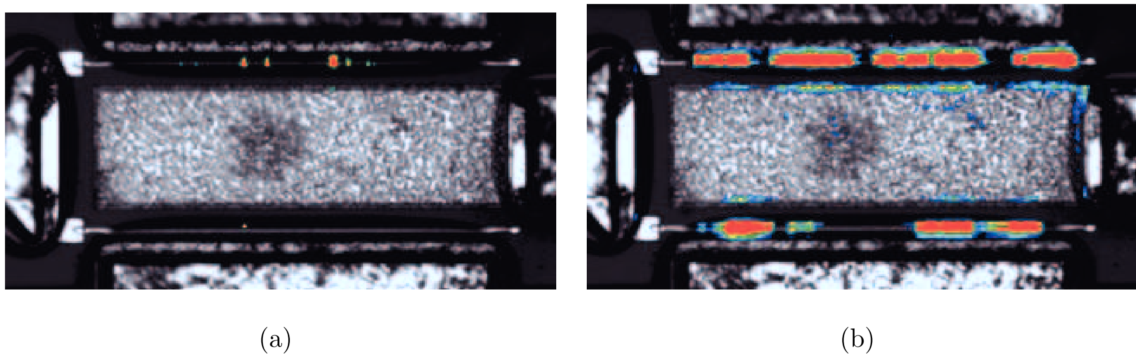


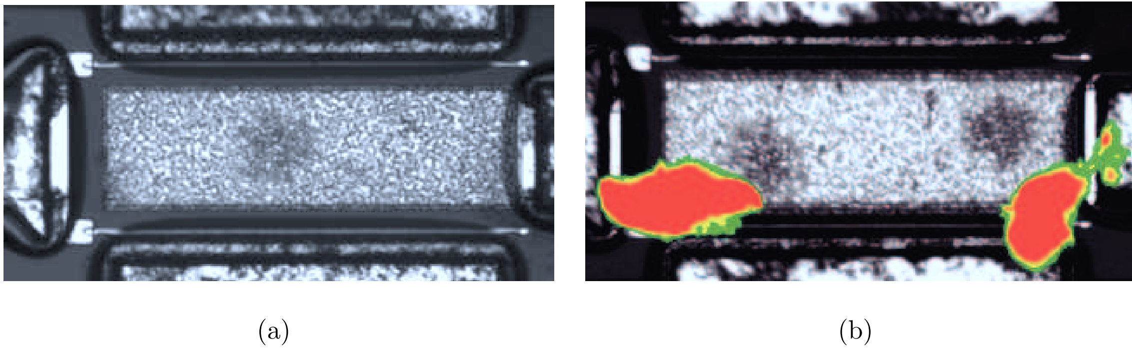
Figure 5.2: *Currents characteristics during the* $35\,V$ *step on a normally-on SH sample. After* $\approx 40\,s$ *the source current increases due to the formation of a parasitic path between source and drain.*

Remarkably, Fig. 5.4 show that no degradation was observed in DH devices, either by DC characterization or EL investigation, up to $150\,V$ (for $L_{GD} = 3\,\mu m$) or up to $200\,V$ for $L_{GD} = 6\,\mu m$. ($200\,V$ was the limit of our instrumentation). DH $L_{GD} = 3\,\mu m$ sample was destroyed by a catastrophic degradation occurring at $155\,V$, corresponding to the unstressed device breakdown limit of about $50\,V/\mu m$. In this case, the presence of the back-barrier has many beneficial effects. The reduction of the unintentional carrier concentration reduces the leakage current and power losses in off-state. Moreover, the additional barrier improves electrons confinement into the channel, thus postponing



(a) (b)

Figure 5.3: *Electroluminescence images for a standard device from SH wafer with* $L_{GD} = 3\,\mu m$*; first hot spots are visible when the drain is biased at* $25\,V$ *(a) and the device reaches a critical condition at* $35\,V$ *(c).*



(a) (b)

Figure 5.4: *Electroluminescence images for a standard double-heterostructure device with* $L_{GD} = 3\,\mu m$*; EMMI do not show any hot spot at* $150\,V$ *(a). Only when the drain voltage is set to* $155\,V$ *(b) a sudden catastrophic degradation takes place, destroying the device.*

the punch-through to much higher voltages and improving reliability. EL measurement does not show any hot spot; this suggests that no additional leakage path is formed during the test, not even at $200\,V$.

5.1.2 Normally-off devices

Off-state voltage step-stresses have been carried out on normally-off DH, DH with Ar^+ ion-implanted SiC substrate, $SH : Fe$ and $SH : Fe$ with Ar^+ ion-implanted SiC substrate in order to compare the devices behavior with substrate floating and grounded. Step-stress tests up to $V_{DS} = 200\,V$ have been performed on floating and on grounded substrate condition. These step-stress tests used the following setup: constant gate voltage ($V_G = -3\,V$) and drain voltage from $10\,V$ up to device failure (or failure criteria $I_{DStress} = 1\,mA/mm$), with $10\,V/2$ minutes long step (source grounded). During stress the emission-microscopy images have been performed. After each step, a complete DC characterization and off-state $EMMI$ have been carried out.
Substrate biasing condition is a crucial point to assess the failure voltage. Indeed on tests with substrate grounded no DC degradation appears but $I_{DStress}$ reaches current failure criteria ($1\,mA/mm$). Wafers with n-type substrate (DH and $SH : Fe$) show a sudden increase of the drain current since the $30\,V$ step, regardless of their epilayer structure, while the gate current does not follow the same trend, as reported in Fig. 5.5; the same test carried out with substrate floating show no sudden I_D increase (Fig. 5.6). This indicates that in n-type substrate wafers, a parasitic path is formed between

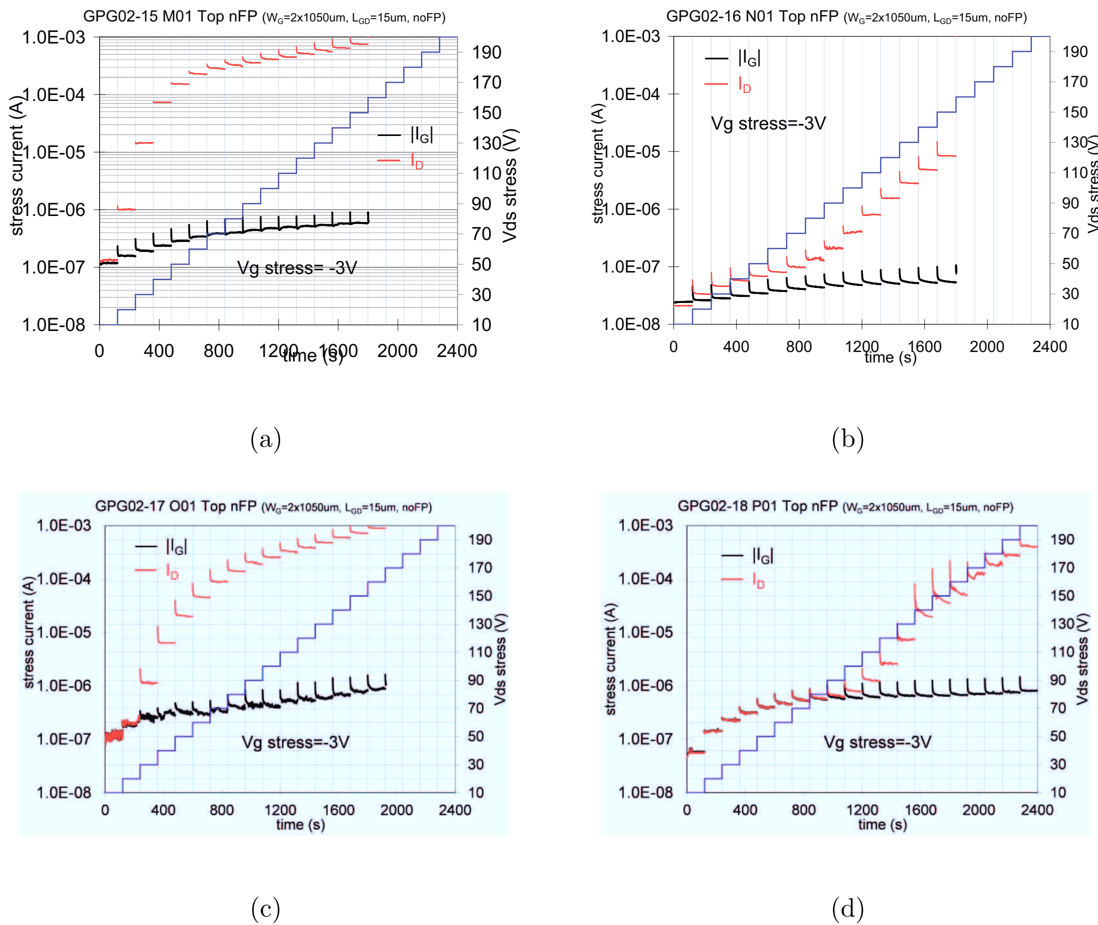
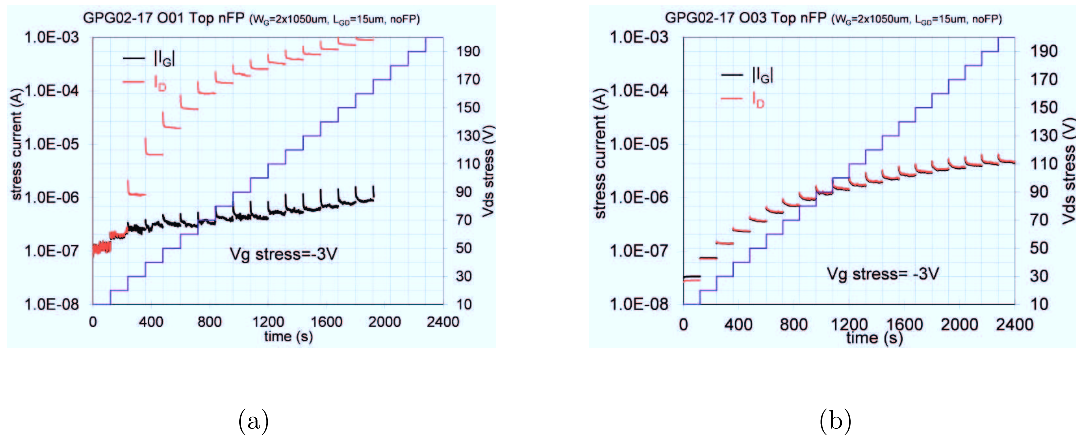


Figure 5.5: *Drain and gate currents evolution during off-state voltage step stress with grounded substrate (a) DH (b) DH with Ar^{+} ion-implanted SiC substrate (c) $SH:Fe$ (d) $SH:Fe$ with Ar^{+} ion-implanted SiC substrate. The comparison between devices with n-type SiC (on the left) and those with Ar^{+} ion-implanted SiC substrate (on the right) show the improvement obtained using a semi-insulating substrate.*

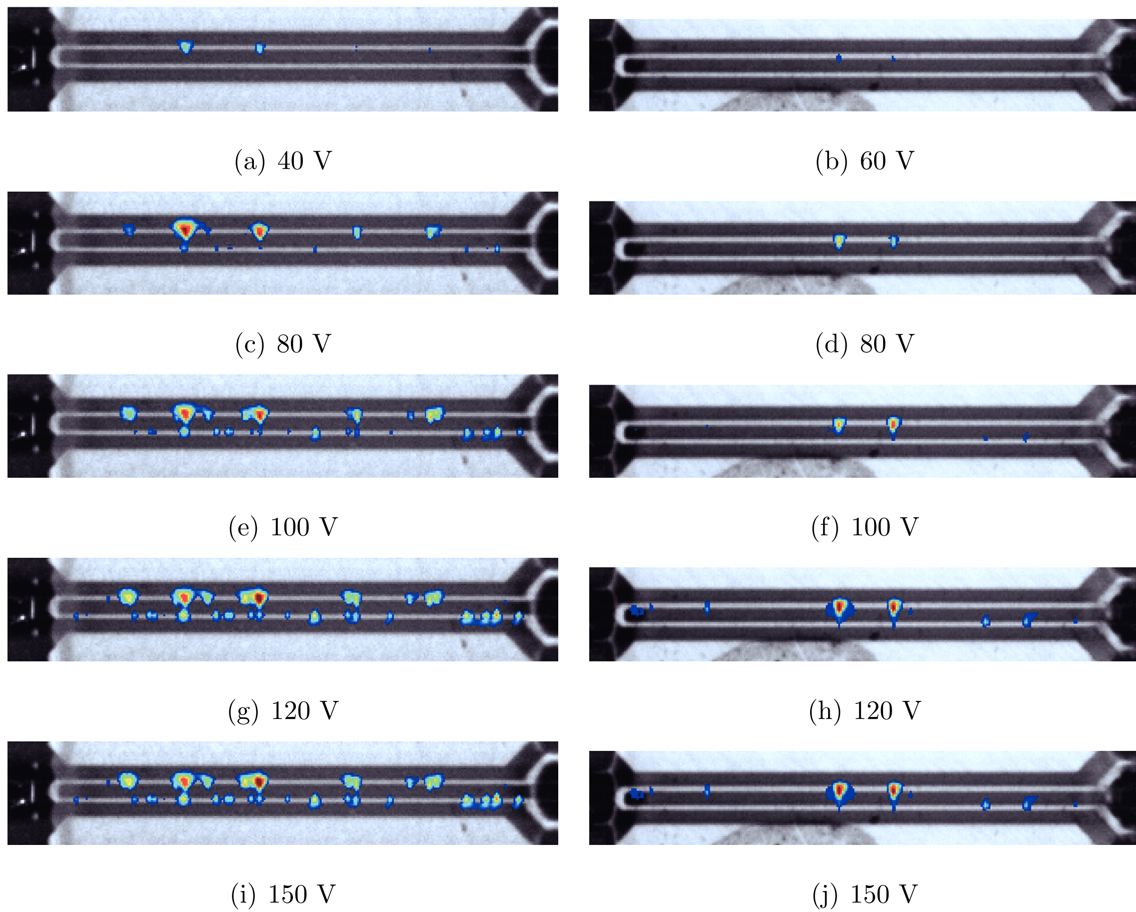
drain and substrate, and a vertical breakdown takes place with formation of $EMMI$ hot spots growing after each step both in size and number with V_D, as reported in Fig. 5.7.

Fig. 5.5 also reports the results for DH and $SH:Fe$ both with Ar^{+} ion-implanted SiC substrate. Data indicate that the use of a semi-insulating substrate positively reduces the vertical leakage current. Use of the SI substrate improves the failure voltage for $SH:Fe$ epilayer design, and confirms the n-type substrate as the weakest point in the heterostructure. Unfortunately, this does not hold when DH design is considered, because no improvement in the failure voltage is visible even if the I_D is positively reduced. This suggests that the DH weak point may not be the substrate only, which



(a) (b)

Figure 5.6: *Drain and gate currents evolution during off-state voltage step stress with substrate (a) grounded and (b) floating on* $SH : Fe$ *wafer. Similar results have been reported for the other wafers.*



(a) 40 V (b) 60 V

(c) 80 V (d) 80 V

(e) 100 V (f) 100 V

(g) 120 V (h) 120 V

(i) 150 V (j) 150 V

Figure 5.7: *Results of spatially-resolved EL measurements carried out under off-state conditions with substrate grounded, for increasing drain voltages.* $V_{GS} = -3V$. *Left: DH, Right SH:Fe.*

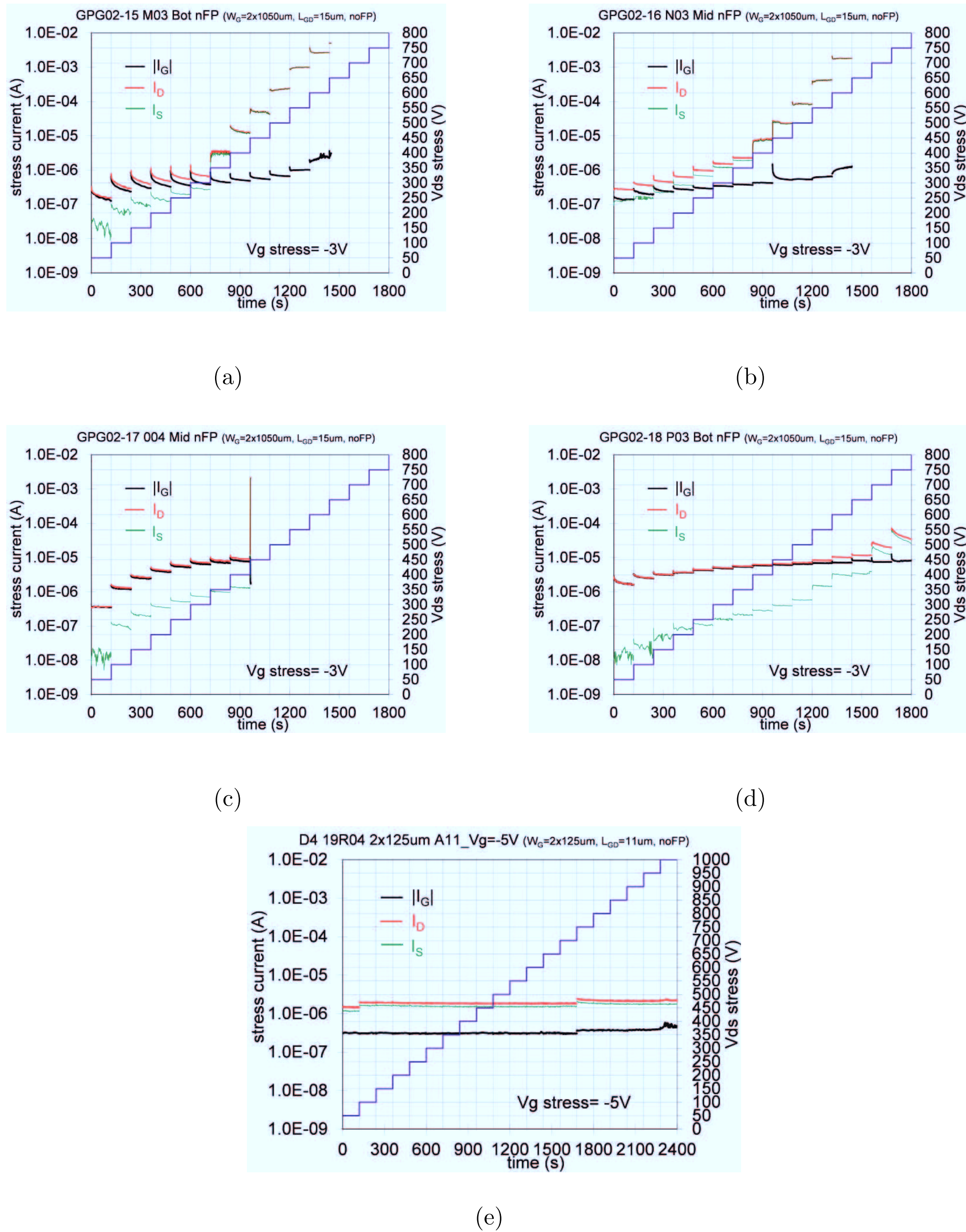
has already proved to improve the reliability for $SH : Fe$, but the back-barrier should be considered as a possible element of weakness too.

Step-stress tests up to $V_{DS} = 1000\,V$ have been performed only on floating substrate condition using the following setup: constant gate voltage ($V_G = -3V$) and drain voltage from $50\,V$ up to device failure (or failure criteria $I_{DStress} = 1\,A/mm$), with $50\,V/2$ minutes long step (source grounded). During stress the emission-microscopy images have been performed; after each step, a complete DC characterization and few off-state emission-microscopy images have been performed. These tests have been carried out on DH, DH with Ar^+ ion-implanted SiC substrate, $SH : Fe$ and $SH : Fe$ with Ar^+ ion-implanted SiC substrate and $SH : C$. Devices without field plate (nFP) and with first field plate gate connected and second field plate floating ($2FP$) have been used.

Step-stress tests with substrate floating show very high failure voltages, see Fig. 5.9, without meaningful degradation of electrical properties during tests before catastrophic degradation. Values obtained strongly depend on the epilayer structures of the device under test.

Tests on DH with n-type and with Ar^+ ion-implanted SiC substrate show the failure voltage takes place again at the same voltage, thus showing the cause of the failure is not related to possible charge flow through the floating self-biasing substrate, but to other mechanisms. Punch-through phenomena is present in DH devices since low drain voltage steps, where the drain-source parasitic path is formed at $150\,V$-$200\,V$, but it is usually undetected or reported at V_D close to the failure voltage in tests involving $SH : Fe$ wafers and reported in only one case in $SH : C$ devices, see Fig. 5.8. Punch-through may be likely the cause of the failure for DH devices, whose performances are not enhanced by the Ar^+-implantation on SiC; in this case no catastrophic degradation takes place, and no degradation of the electrical properties of device is visible.

Different results can be seen considering the $SH : Fe$ epilayer structure. Devices with n-type substrate have a failure voltage of $400\,V$ while their counterpart grown over a semi-insulating substrate can withstand up to $800\,V$. A possible explanation may be the propagation of defects and dislocations from the highly resistive substrate to the upper layers, that work against current flow by trapping electrons close to the channel. The best results are obtained with Carbon doping on SH: tests carried out show that



(a) (b) (c) (d) (e)

Figure 5.8: *Drain and gate currents evolution during off-state voltage step stress with grounded substrate (a) DH (b) DH with Ar^+ ion-implanted SiC substrate (c) SH : Fe (d) SH : Fe with Ar^+ ion-implanted SiC substrate (e) SH : C. The comparison between devices with n-type SiC ((a) and (c), on the left) and those with Ar^+ ion-implanted SiC substrate ((b) and (d) on the right) show the improvement obtained using a semi-insulating substrate.*

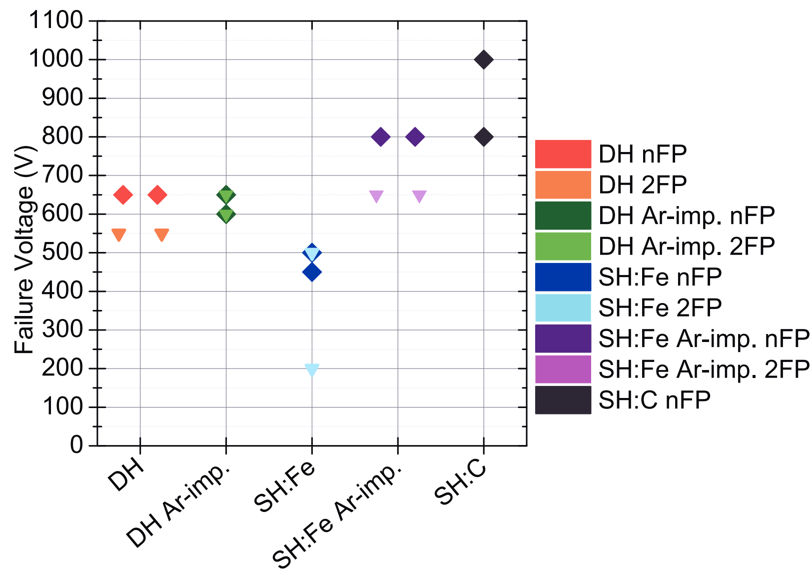


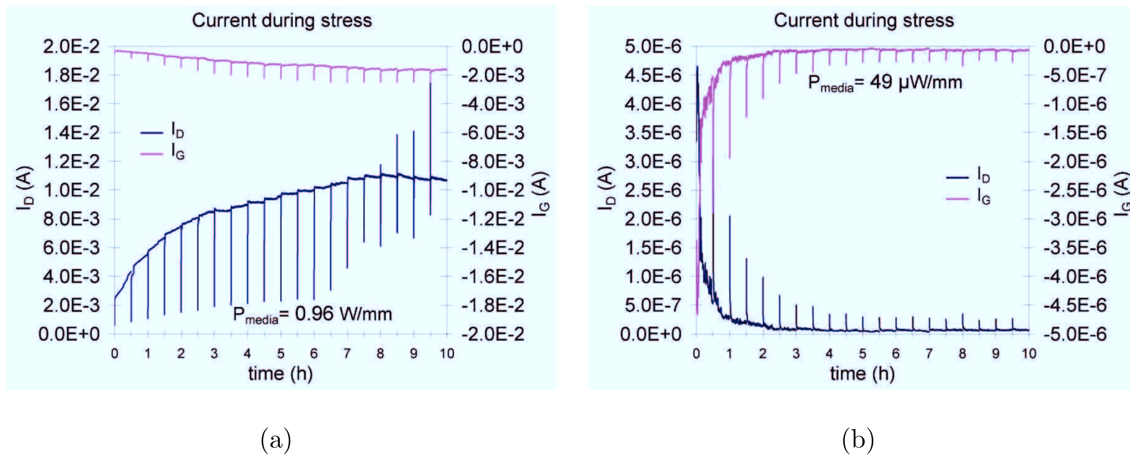
Figure 5.9: *Comparison of the failure voltage extrapolated by tests results. The best results is given by SH:C epilayer design.*

this epilayer design can withstand up to $1000\,V$.

2FP design gives no improvement or worse results than *nFP* devices. This may be due to a non optimum field-plate design. Additional tests may help to identify the reason of this inefficiency.

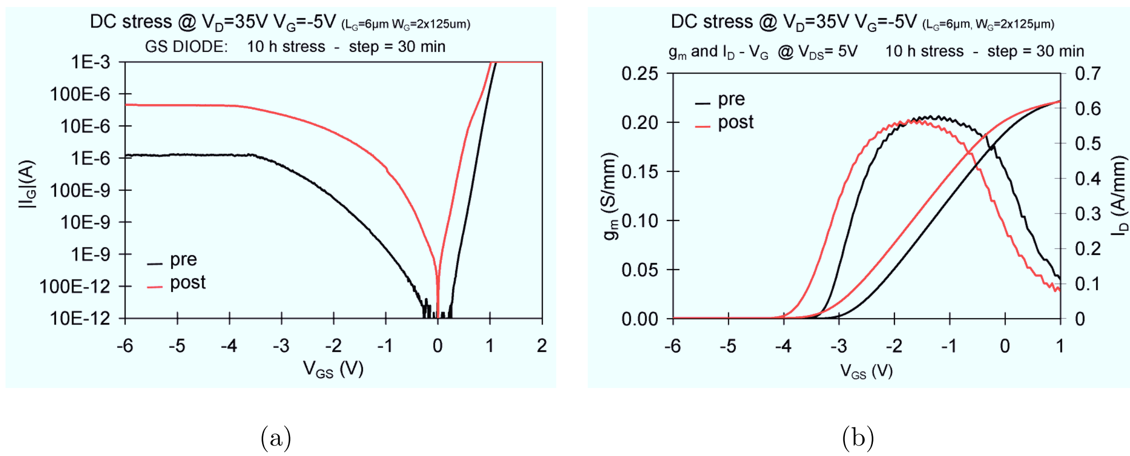
5.2 DC Life test

Normally-on $SH - A$ and $DH - D$ devices have been tested to assess reliability. A 10 h stress at fixed $V_G = -5\,V$, $V_D = 35\,V$ has been carried out on devices with $L_{GD} = 6\,\mu m$. *SH* devices present an evident degradation consisting in an increase of gate leakage current (in absolute value) together with an increase of the drain current. Comparison of pre- and post-electroluminescence measurements confirms increase in number and size of hot spots, correlated to leakage paths formation (see Fig. 5.12). *SH* shows pinch-off voltage shift towards negative values and leakage current increase, see Fig. 5.11, that explain the observed increase in the drain current. This mechanism was found to be permanent, as demonstrated by repeating the measurements after a one month rest period. Results therefore suggest that stress induced a permanent degradation of the Schottky barrier, with subsequent increase in the leakage current in off-state and the shift of pinch-off voltage.



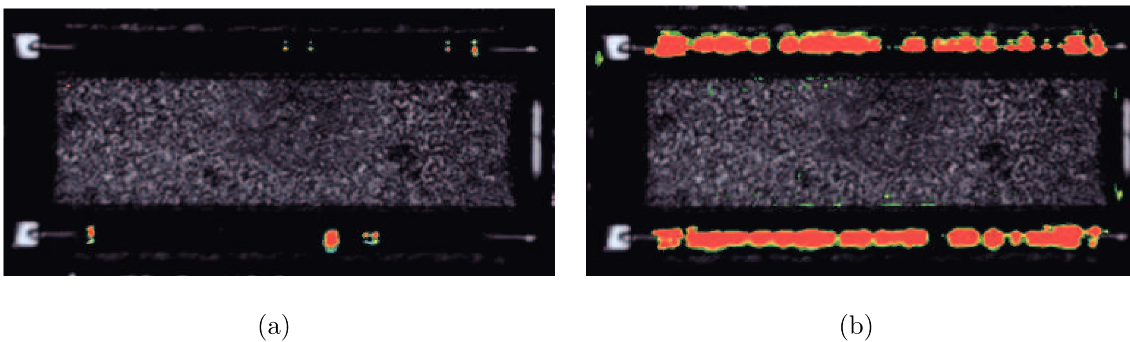
(a) (b)

Figure 5.10: *Currents during DC short life test carried out on a $L_{GD} = 6\,\mu m$ device: (a) SH-A device (b) DH-D.*



(a) (b)

Figure 5.11: *Pre- and post-stress characteristics of a SH-A device (a) gate-source I_G and (a) g_m.*



(a) (b)

Figure 5.12: *Spatially resolved EMMI measurements carried out during life test on normally-on SH at (a) $5\,V$ (b) $35\,V$.*

Double-heterostructure *HEMTs*, biased at the same condition, show only a negligible degradation. To further test the *DH* devices, a life test at $V_G = -5\,V$, $V_D = 200\,V$ has been carried out. Even at this condition, the devices face minimal degradation, confirmed also by *EL* measurements where no formation of hot spot was visible. It is worth noticing that *DH* devices did not show any variation in pinch-off voltage, even for the $V_G = -5\,V$, $V_D = 200\,V$ biasing condition. In this case, the current levels during each step of the stress remained extremely low ($\approx 10^{-8}$ to $10^{-7}\,A/mm$) and the decrease of currents during the first few hours of the life test suggests the presence of trapping (Fig. 5.10). Double heterostructure devices present a significantly better performances than the *SH* ones, likely for the following reasons (i) they have very low leakage currents (ii) due to the back-barrier, subsurface DIBL is postponed to much higher voltages, thus improving the failure voltage and the reliability of the devices. The *DH* devices analyzed within this paper still suffer from some issues: (i) relatively low output current (ii) kink phenomena. The low output current can be improved adding, for example, a thin *AlN* layer. The kink seems to be related to the trapping in the substrate. The use of a semi-insulating *SiC* substrate could reduce these phenomena.

Chapter 6

ESA NPI Project

6.1 Measurement Plan Description

6.1.1 Basic Characterization

In this section it will be described a the preliminary characterization carried out on GH25 samples provided by UMS, specifying most relevant parameters, measurement setting conditions and devices tested.

DC characterization

Table 6.1: *Parameters extracted from $I_D - V_G$ measurement at $V_D = 10\,V$.*

Parameter	Unit	Biasing Conditions	Notes
$I_{DS@V_D=10V}$	A/mm	$V_{DS} = 10\,V$, $V_{GS} = 0\,V$	Drain current at $V_{GS} = 0\,V$
$I_{Dmax@V_D=10V}$	A/mm	$V_{DS} = 10\,V$, $V_{GS} = 1\,V$	Drain current at $V_{GS} = 1\,V$
$I_{Doff@V_D=10V}$	A/mm	$V_{DS} = 10\,V$, $V_{GS} = -7\,V$	Drain current at $V_{GS} = -7\,V$
$I_{Gleak@V_D=10V}$	A/mm	$V_{DS} = 10\,V$, $V_{GS} = -7\,V$	Gate current at $V_{GS} = -7\,V$
$V_{p-1\%Idss@V_D=10V}$	V	$V_{DS} = 10\,V$, $I_D = 1\%$ of I_{DSS}	
$g_{m_0@V_D=10V}$	mS/mm	$V_{DS} = 10\,V$, $V_{GS} = 0\,V$	
$g_{m_{max}@V_D=10V}$	mS/mm	$V_{DS} = 10\,V$	g_m peak measured
$I_{DSg_{m_{max}}@V_D=10V}$	mA/mm	$V_{DS} = 10\,V$, $g_m = g_{m_{max}10V}$	Current at g_m peak
$V_{GSg_{m_{max}}@V_D=10V}$	V	$I_{DS} = I_{DSg_{m_{max}}10V}$	Voltage at g_m peak

Preliminary DC characterizations at room temperature has been performed to de-

fine variability of parameters in the *GH25 M3* technology, identify malfunctioning devices and presence of any possible issue (kink, leakage, pinch-off for example). The characterization of different transistors gives an idea of the DC performances and capabilities, together with a preliminary analysis of the variability of the parameters extracted from measurements. From the $I_D - V_G$ at $V_D = 10V$ the following parameters can be extracted (6.1) The same is done for $I_D - V_G$ at $V_D = 15\,V$:

Table 6.2: *Parameters extracted from $I_D - V_G$ measurement at $V_D = 15\,V$.*

Parameter	Unit	Biasing Conditions	Notes
$I_{DS@V_D=15V}$	A/mm	$V_{DS} = 15\,V$, $V_{GS} = 0\,V$	Drain current at $V_{GS} = 0\,V$
$I_{Dmax@V_D=15V}$	A/mm	$V_{DS} = 15\,V$, $V_{GS} = 1\,V$	Drain current at $V_{GS} = 1\,V$
$I_{Doff@V_D=15V}$	A/mm	$V_{DS} = 15\,V$, $V_{GS} = -7\,V$	Drain current at $V_{GS} = -7\,V$
$I_{Gleak@V_D=15V}$	A/mm	$V_{DS} = 15\,V$, $V_{GS} = -7\,V$	Gate current at $V_{GS} = -7\,V$
$V_{p-1\%Idss@V_D=15V}$	V	$V_{DS} = 15\,V$, $I_D = 1\%$ of I_{DSS}	
$g_{m_0@V_D=15V}$	mS/mm	$V_{DS} = 15\,V$, $V_{GS} = 0\,V$	
$g_{m_{max}@V_D=15V}$	mS/mm	$V_{DS} = 15\,V$	g_m peak measured
$I_{DSg_{m_{max}}@V_D=15V}$	mA/mm	$V_{DS} = 15\,V$, $g_m = g_{m_{max}15V}$	Current at g_m peak
$V_{GSg_{m_{max}}@V_D=15V}$	V	$I_{DS} = I_{DSg_{m_{max}}15V}$	Voltage at g_m peak

A search is used to find the pinch-off voltage at $V_{DS} = 10\,V, 15\,V$.

Table 6.3: *Biasing condition for pinch-off voltage extraction.*

Parameter	Unit	Biasing Conditions	Notes
$V_{po@Vd=10V}$	V	$V_{DS} = 10\,V$, $I_{DS} = 1\,mA/mm$	Drain current at $V_{GS} = 0\,V$
$V_{po@Vd=15V}$	V	$V_{DS} = 15\,V$, $I_{DS} = 1\,mA/mm$	Drain current at $V_{GS} = 0\,V$

It is possible to extract R_{ON}:

Table 6.4: *Biasing condition for on-resistence extraction.*

R_{ON}	$ohm * mm$	$V_D = 0.5\,V$, $V_G = 0\,V$, $V_S = 0\,V$

Leakage currents at $30\,V$ are also collected

Table 6.5: *Biasing condition applied to high voltage (30 V) leakage measurements.*

$I_{D@V_D=30\,V}$	A/mm	$V_{DS} = 30\,V$, $V_{GS} = -7\,V$
$I_{G@V_D=30\,V}$	A/mm	$V_{DS} = 30\,V$, $V_{GS} = -7\,V$

To calculate drain and source end-resistance, a fixed current of $1\,mA$ is applied to the gate; in turn, source and drain are set to $0\,V$, while the remaining terminal is set to null current. In this way, the voltage at X (under the gate in the channel) is the same as the last terminal, where no current

$$V_X = V_G - R_G \cdot I_G \tag{6.1}$$

but the drain current flowing is set to zero

$$I_D = 0 \tag{6.2}$$

thus $V_X = V_D$ and the end-resistance on the source side is:

$$R_S = \frac{V_X}{I_G} = \frac{V_D}{I_G} \tag{6.3}$$

Similar calculations give an estimation of R_D. Measured values and extrapolated parameters are reported:

Table 6.6: *End-resistance measured parameters and their biasing condition.*

Parameter	Unit	Biasing Conditions	Notes
R_D V_D	V	$V_D = 0\,V$, $I_G = 1\,mA/mm$, $I_S = 0\,mA/mm$	Drain voltage
R_D V_S	V	$V_D = 0\,V$, $I_G = 1\,mA/mm$, $I_S = 0\,mA/mm$	Source Volage
R_D V_D	V	$I_D = 0\,mA/mm$, $I_G = 1\,mA/mm$, $V_S = 0\,mA/mm$	Drain voltage
R_D V_S	V	$I_D = 0\,mA/mm$, $I_G = 1\,mA/mm$, $V_S = 0\,mA/mm$	Source Volage
R_D	Ohm*mm		Extracted from data
R_S	Ohm*mm		Extracted from data
$R_D + R_S$	Ohm*mm		Extracted from data

From gate and drain diode measurements some useful information are available. The first is the ideality parameter N of the diodes. Second, the series resistance R_S. Third,

Table 6.7: *Gate-souce and gate-drain diodes parameters.*

Parameter	Unit	Biasing Conditions	Notes
Gate-Source Diode N	Unitless		Extracted from data
Gate-Source Diode R_S	Ohm*mm		Extracted from data
Gate-Source Diode I_S	A/mm		Extracted from data
Gate-Drain Diode N	Unitless		Extracted from data
Gate-Drain Diode R_S	Ohm*mm		Extracted from data
Gate-Drain Diode I_S	A/mm		Extracted from data
I_{GS_7V}	A/mm	$V_{GS} = -7V$	
I_{GD_7V}	A/mm	$V_{DS} = -7V$	

the current flowing I_S and finally the leakage currents at $V_G = -7\,V$.

Devices to test: *DCXA, DCXB, DCXC, DCXD*

Number of tests: *all of available samples*

Measurements and condition: *full DC characterization*

S-parameters characterization

Table 6.8: *RF parameter: maximum available gain (MAG), cut-off frequency f_τ and S-parameters.*

Parameter	Unit	Conditions
MAG_2	dB	f=2GHz
MAG_{10}	dB	f=10GHz
MAG_{18}	dB	f=18GHz
f_τ	Hz	Extrapolated on the $-20\,dB$ region
S_{11}	$\|\|, ^\circ$	$f = 200\,MHz$ to $40\,GHz$
S_{12}	$\|\|, ^\circ$	$f = 200\,MHz$ to $40\,GHz$
S_{21}	$\|\|, ^\circ$	$f = 200\,MHz$ to $40\,GHz$
S_{22}	$\|\|, ^\circ$	$f = 200\,MHz$ to $40\,GHz$

In order to characterize *RF* devices, a characterization to study the behavior of most common RF parameters; first of all, S-parameters, a mathematical construct

that quantifies how RF energy propagates through a multi-port network, at different load points while changing the frequency of the system. Together with them, also the maximum available gain (MAG) at different frequencies. All the tests will be carried at the bias condition $V_D = 30\,V, I_D = 250\,mA/mm$ (which is equal to $I_{DS} = 21.5\,mA$ for the $86\,\mu m$ gate width devices examined).
Devices to test: *RFXA, RFXB, RFXC, RFXD*
Number of tests: *all of available samples*
Measurements and condition: *full RF characterization*

Pulsed characterization

Pulsed $I - V$ characterization is extremely useful to have information about trapping. The application of pulsed bias reduces self-heating of the devices thanks to a low duty cycle and gives useful information about trapping effects, which are brought out when relevant quiescent bias point (V_{GSq}, V_{DSq}) are applied. The current collapse $CC/$ slump ratio SR parameters are defined as:

$$CC(V_{DSq}) = 1 - \frac{I_{DSAT}(V_{GSq}, V_{DSq})}{I_{DSAT}(0,0)} = 1 - SR(V_{DSq}) \tag{6.4}$$

I_{DSAT} is defined as the current measured at a fixed V_{DS} (usually equal to knee voltage) and $V_{GS} = 0\,V$. In our tests the CC/SR are usually calculated at $V_{DS} = 10\,V$; the device suffers from kink effect hence $I_D - V_G$ measurements are carried out also at $V_{DS} = 15\,V$, thus slump ratio is evaluated both in approximately pre- and post-kink condition. The current collapse is also evaluated by the measurement of transconductance profile $g_m - V_{GS}$. This measurement helps to better discriminate where traps are located. Even if usually not a destructive measurement, it is carried out only in a subset of the devices available.

Devices to test: *RFXA, RFXB, RFXC, RFXD*
Number of tests: *4-6 per kind and per each milestone*
Measurement: *full pulsed characterization*

Table 6.9: *Time and biasing condition applied for double pulsed measurements.*

Parameter	Conditions
pulse period T	$100\,\mu s$
pulse width T_{ON}	$1\,\mu s$
Duty Cycle δ	$1\,\%$
Quiescent Bias Point (V_{GSq}, V_{DSq})	$(0\,V, 0\,V)$ $(-7\,V, 0\,V)$ $(-7\,V, 30\,V)$

6.1.2 Breakdown tests

This test is useful to study characterization of the breakdown, and can give a significant insight of physics behind it (gate leakage mechanisms, punch-through phenomena, hopping, impact ionization). The punch-through can be strongly suspected when considering the possible shift of threshold voltage in the $I_D - V_G$ measurements while increasing the V_{DS} applied [29][69]. The more the ΔV_{po}, the more the probability the phenomena to occur and the lower the V_{DS} which it becomes relevant.
This test can be carried out sweeping drain voltage or current and monitoring all other parameters. Anyway, due to the slow activation of protection system at reaching the compliance limit, if this test is voltage controlled it is usually destructive. For this reason, it is preferable if the test is current controlled. Preliminary DC characterizations were carried out at room temperature; sweep on drain current up to $0.9\,mA/mm$ compliance. This test helps identifying the critical voltage to breakdown of the devices; it also can help studying the effects of field plate application and the dependence of the breakdown from L_{GD} and other parameters.

Table 6.10: *Parameter monitored during breakdown measurements*

Parameter	Unit	Conditions
V_D	V	$I_D = [90\,nA, 900\,\mu A]$, $V_{GS} = [-7\,V, -4\,V]$,
I_G	A/mm	$I_D = [90\,nA, 900\,\mu A]$, $V_{GS} = [-7\,V, -4\,V]$,
I_S	A/mm	$I_D = [90\,nA, 900\,\mu A]$, $V_{GS} = [-7\,V, -4\,V]$,

Devices to test: *DCXA, DCXB, DCXC, DCXD*

Number of tests: *4 per kind*

Measurement: *preliminary full DC characterization followed by I_D controlled breakdown; post test full DC characterization*

6.1.3 Reliability

In this section it will be described all reliability tests performed on $GH25$ samples provided by UMS.

Off-state step stress test

In this test, V_D is increased from $20\,V$ up to failure criteria or to the limit of the instrumentation used in a three terminals configuration at fixed V_G and source to ground. Only off-state bias condition, where the device is in pinch-off condition ($V_G = V_P - 3\,V$ for example) thus enhancing both trapping effects and leakage phenomena, has been tested. No electroluminescence has been performed during this tests.

Devices to test: *DCXA, DCXB, DCXC, DCXD*

Number of tests: *4 per kind*

Measurement: Preliminary full DC characterization, DC step stress V_D from $20\,V$ up to failure criteria, $10\,V/1$ hour step. Relaxation time 10 minutes.

Load line life stress test

3 working point in the load line as defined for *GH25* devices (from the knee point at $V_G = 1\,V$ to $I_D = 0\,V$, $V_D = 60\,V$) have been chosen to study the evolution of the devices (1) under high voltage and reduced currents, (2) at high voltage and currents and (3) low voltage but high currents. For all of these points a test has been carried out for a variable dwell time at fixed bias condition at a temperature $T_{Test} = 423K$.

Devices to test: *DCXD*

Number of tests: *1 per bias point and per temperature*

1 samples $I_{DS} = 660\,mA/mm$, $V_{DS} = 10\,V$, $T_{Test} = 423K$

1 samples $I_{DS} = 400\,mA/mm$, $V_{DS} = 30\,V$, $T_{Test} = 423K$

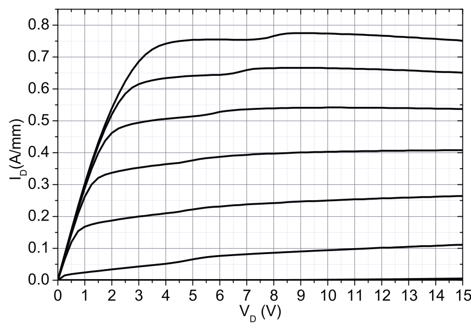
1 samples $I_{DS} = 5\,mA/mm$, $V_{DS} = 60\,V$, $T_{Test} = 423K$

6.2 Results and Analysis

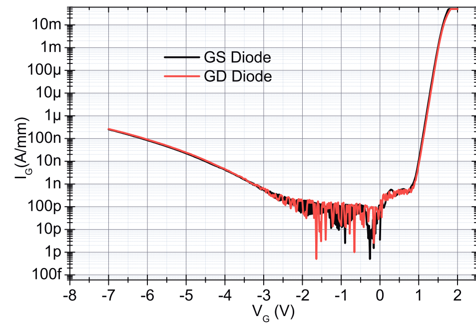
6.2.1 Basic Characterization

DC characterization

All *DCXA*, *DCXB*, *DCXC*, *DCXD* devices available in *GH25 GREAT2* milestone *M3* batch have been measured to evaluate DC performances and capabilities, together with a preliminary analysis of the variability of the parameters extracted from measurements. All main curves are here reported for each device type, followed by the comparison of the most important *DC* parameters (Fig. 6.1-Fig. 6.8). The technologic process has reached a mature state, and the *DC* characterization reveals small differences between devices of the same kind. Only some devices from few bare dies (*Q24* most of all) show large variation from the standard profile, mainly for their position in the wafer, which is suspected to be closest to wafer edges. The comparison between the different device types reveal that the source terminated field plate has little or no effect in the *DC* behaviour of the various devices, as can be seen comparing both curves and DC parameters extracted. Almost all the devices suffer from kink effect; the V_{Kink}, depending on geometrical properties of the devices, gate voltage applied and also due to variability of parameters among devices of the same technologic manufacturing process, ranges between $6\,V$ and $10\,V$.



(a)



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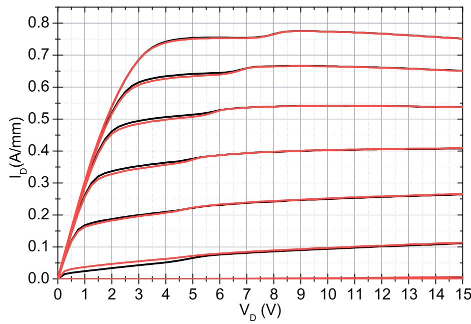

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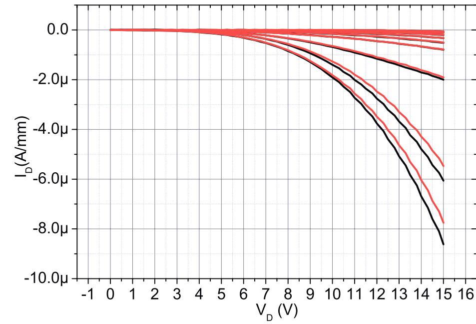

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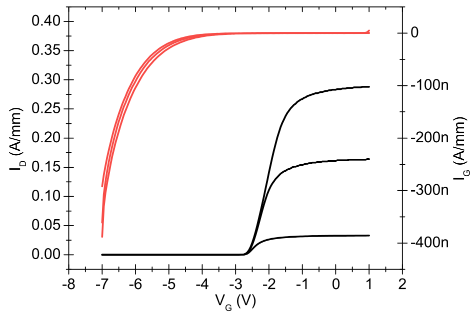

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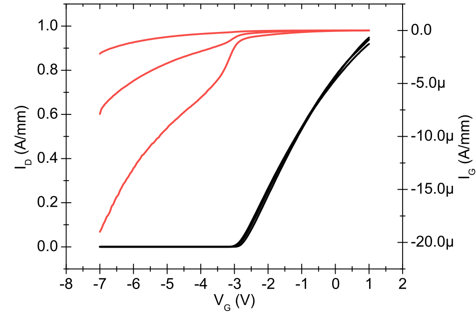

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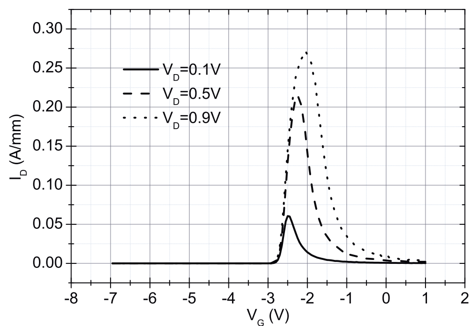

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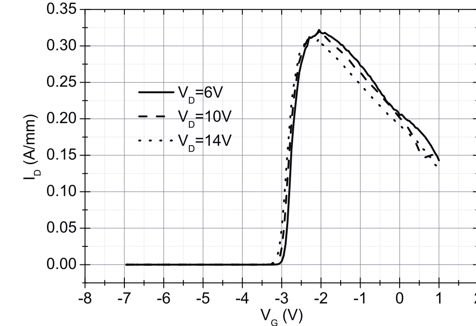
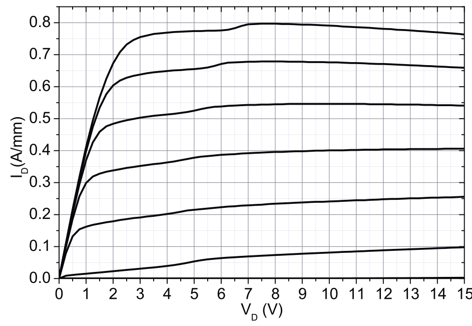
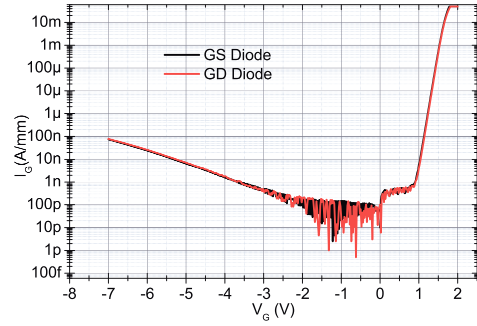


(h)

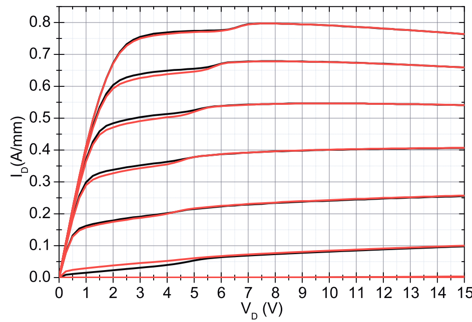
Figure 6.1: *Standard DCXA device: (a) $I_{DS} - V_{DS}$ at $V_{GS} = [-4\,V, 0\,V]$, $0.5\,V$ step; (b) GS and GD diodes $I - V$; up to bottom and bottom to up (c) $I_{DS} - V_{DS}$ (d) $I_{GS} - V_{DS}$; $I_{DS} - V_{GS}$ (e) at $V_{DS} = [0.1\,V, 0.9\,V]$, $0.4\,V$ step and (f) $V_{DS} = [6\,V, 14\,V]$, $4\,V$ step; $g_m - V_{GS}$ (g) at $V_{DS} = [0.1\,V, 0.9\,V]$, $0.4\,V$ step and (h) $V_{DS} = [6\,V, 14\,V]$, $4\,V$ step.*



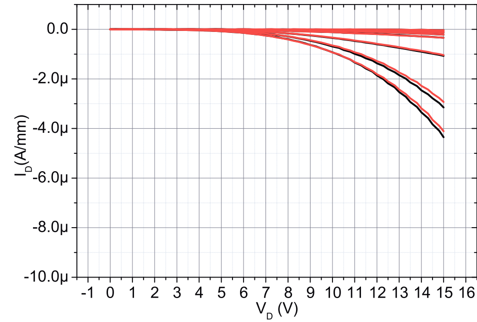
(a)



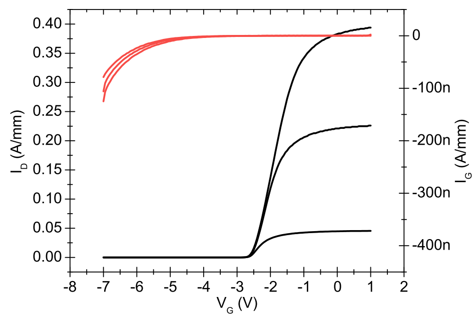
(b) GS and GD diodes $I - V$



(c) up to bottom and bottom to up $I_{DS} - V_{DS}$



(d) up to bottom and bottom to up $I_{GS} - V_{DS}$



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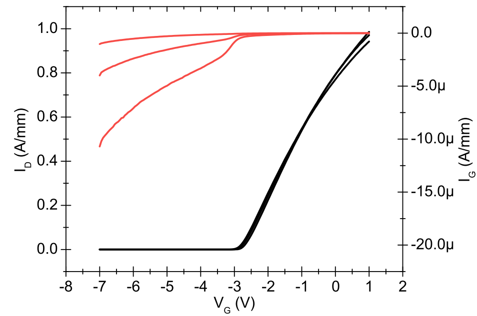

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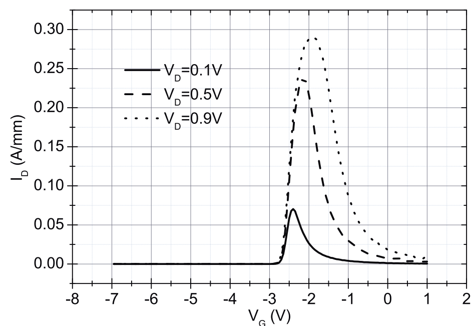

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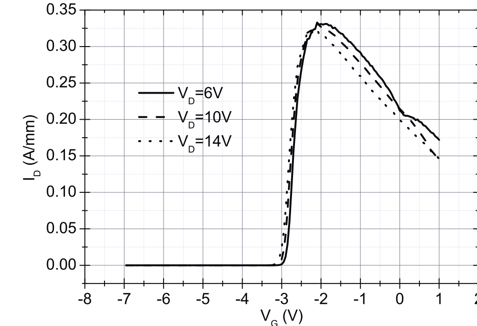

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Figure 6.2: *Standard DCXB device: (a)* $I_{DS} - V_{DS}$ *at* $V_{GS} = [-4\,V, 0\,V]$, $0.5\,V$ *step; (b) GS and GD diodes* $I - V$*; up to bottom and bottom to up (c)* $I_{DS} - V_{DS}$ *(d)* $I_{GS} - V_{DS}$; $I_{DS} - V_{GS}$ *(e) at* $V_{DS} = [0.1\,V, 0.9\,V]$, $0.4\,V$ *step and (f)* $V_{DS} = [6\,V, 14\,V]$, $4\,V$ *step;* $g_m - V_{GS}$ *(g) at* $V_{DS} = [0.1\,V, 0.9\,V]$, $0.4\,V$ *step and (h)* $V_{DS} = [6\,V, 14\,V]$, $4\,V$ *step.*

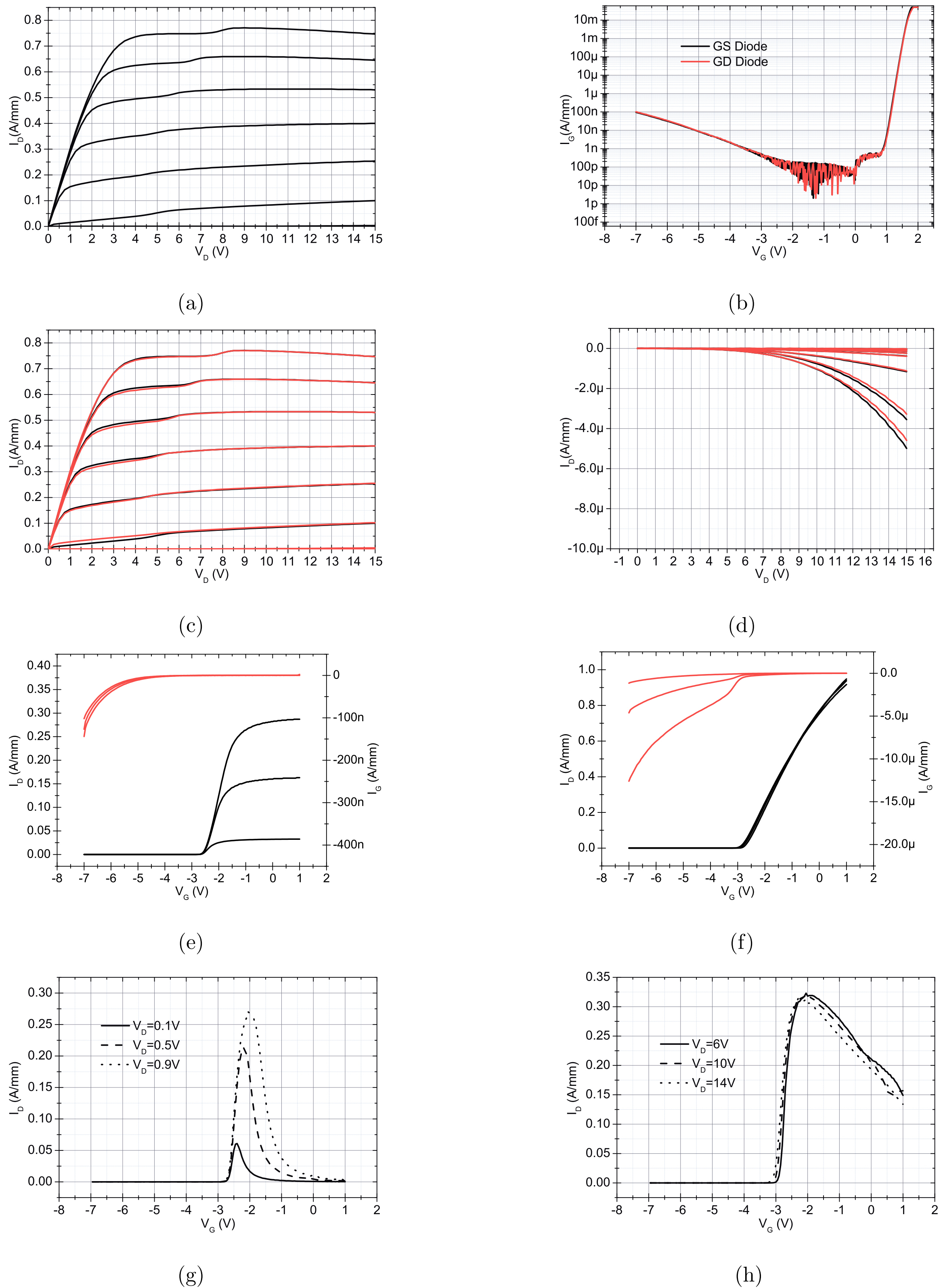


Figure 6.3: *Standard DCXC device: (a)* $I_{DS} - V_{DS}$ *at* $V_{GS} = [-4\,V, 0\,V]$*,* $0.5\,V$ *step; (b) GS and GD diodes* $I - V$*; up to bottom and bottom to up (c)* $I_{DS} - V_{DS}$ *(d)* $I_{GS} - V_{DS}$*;* $I_{DS} - V_{GS}$ *(e) at* $V_{DS} = [0.1\,V, 0.9\,V]$*,* $0.4\,V$ *step and (f)* $V_{DS} = [6\,V, 14\,V]$*,* $4\,V$ *step;* $g_m - V_{GS}$ *(g) at* $V_{DS} = [0.1\,V, 0.9\,V]$*,* $0.4\,V$ *step and (h)* $V_{DS} = [6\,V, 14\,V]$*,* $4\,V$ *step.*

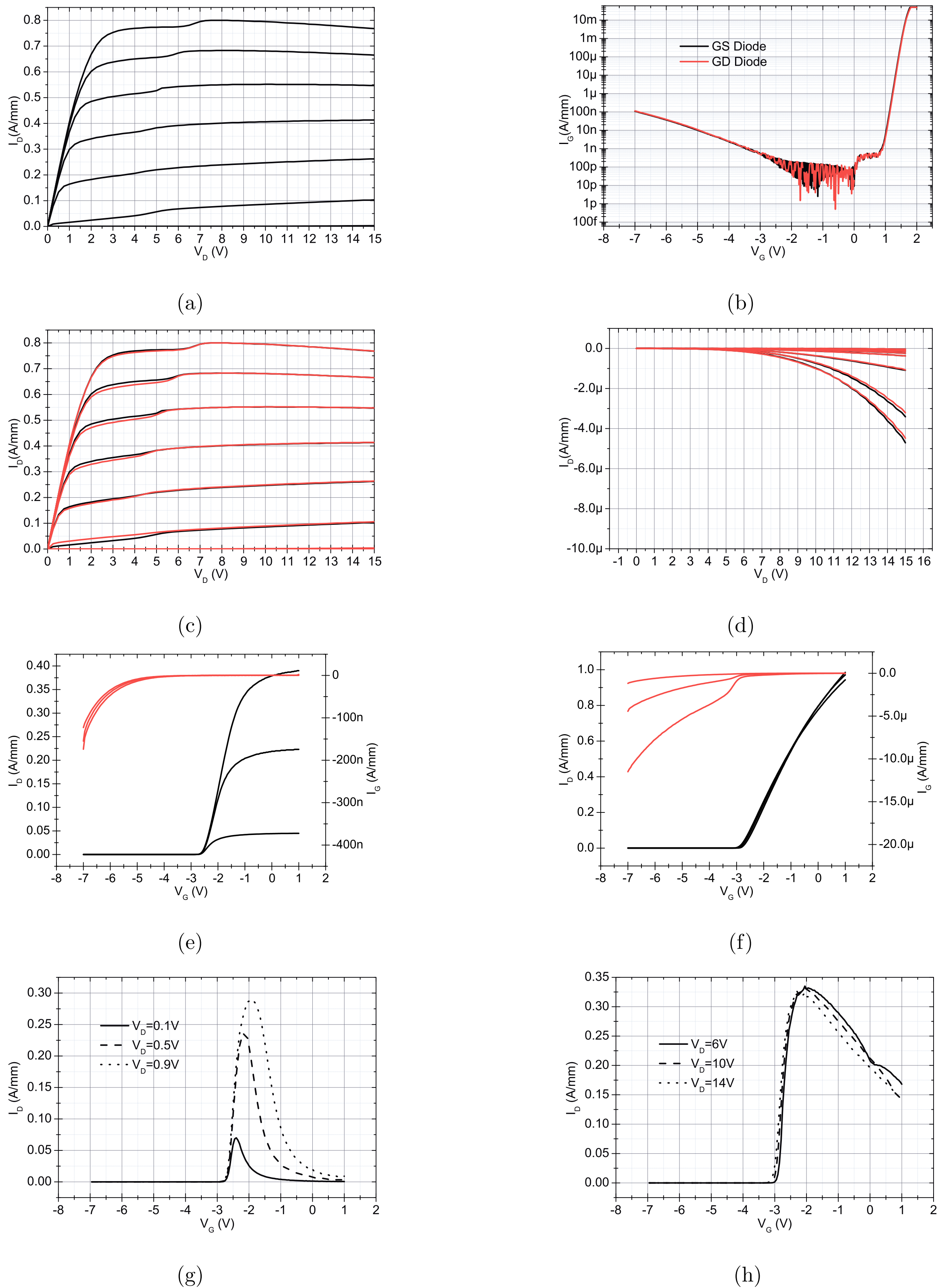


Figure 6.4: *Standard DCXD device: (a) $I_{DS} - V_{DS}$ at $V_{GS} = [-4\,V, 0\,V]$, $0.5\,V$ step; (b) GS and GD diodes $I - V$; up to bottom and bottom to up (c) $I_{DS} - V_{DS}$ (d) $I_{GS} - V_{DS}$; $I_{DS} - V_{GS}$ (e) at $V_{DS} = [0.1\,V, 0.9\,V]$, $0.4\,V$ step and (f) $V_{DS} = [6\,V, 14\,V]$, $4\,V$ step; $g_m - V_{GS}$ (g) at $V_{DS} = [0.1\,V, 0.9\,V]$, $0.4\,V$ step and (h) $V_{DS} = [6\,V, 14\,V]$, $4\,V$ step.*

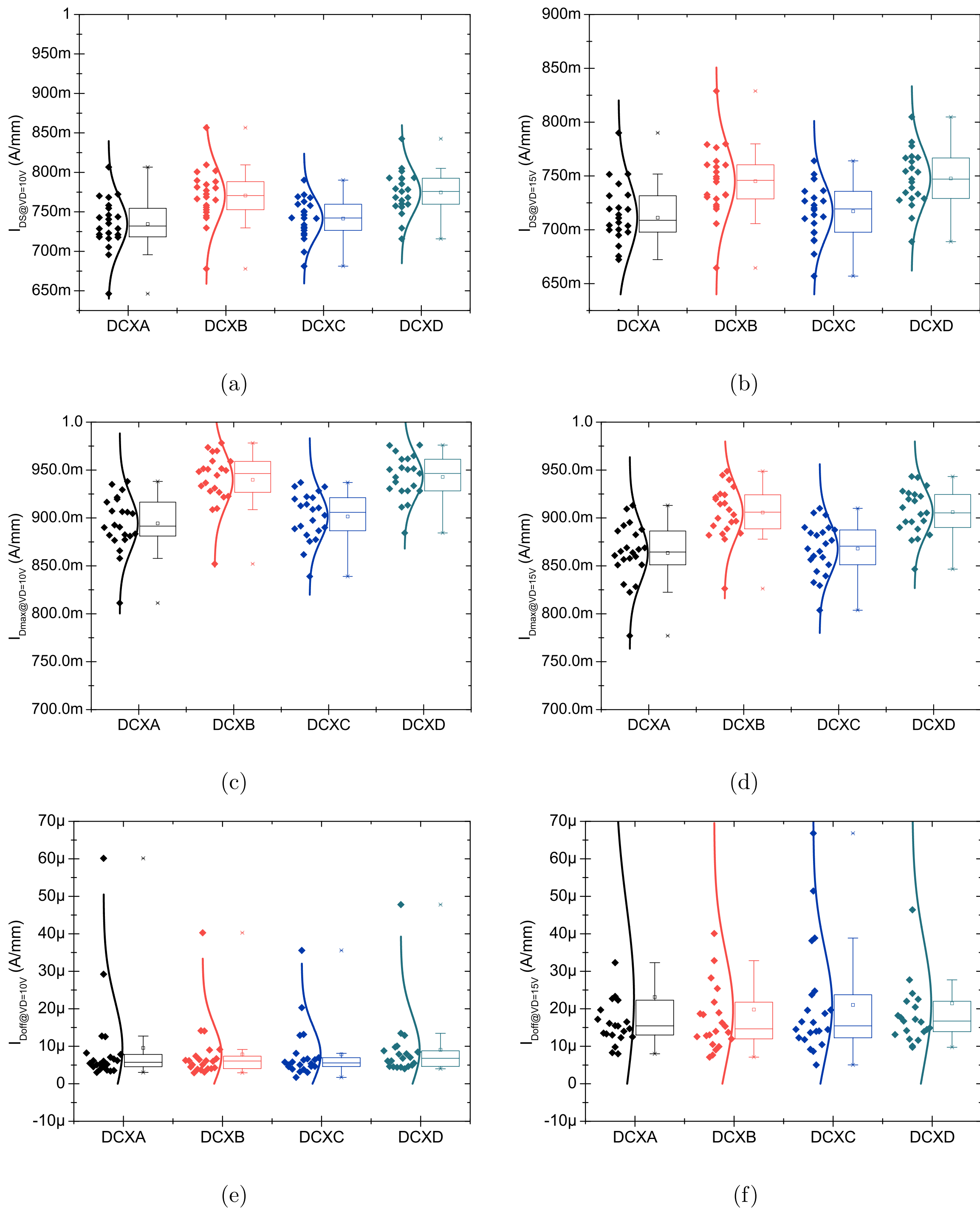


Figure 6.5: *Spread measured in I_{DS} (a) at $V_{DS} = 10\,V$, $V_{GS} = 0\,V$ and (b) at $V_{DS} = 15\,V$, $V_{GS} = 0\,V$. Spread in $I_{DS_{max}}$ measured (c) at $V_{DS} = 10\,V$, $V_{GS} = 0\,V$ and (d) at $V_{DS} = 15\,V$, $V_{GS} = 0\,V$. Spread in $I_{D_{off}}$ measured (e) at $V_{DS} = 10\,V$, $V_{GS} = -7\,V$ (f) at $V_{DS} = 15\,V$, $V_{GS} = -7\,V$.*

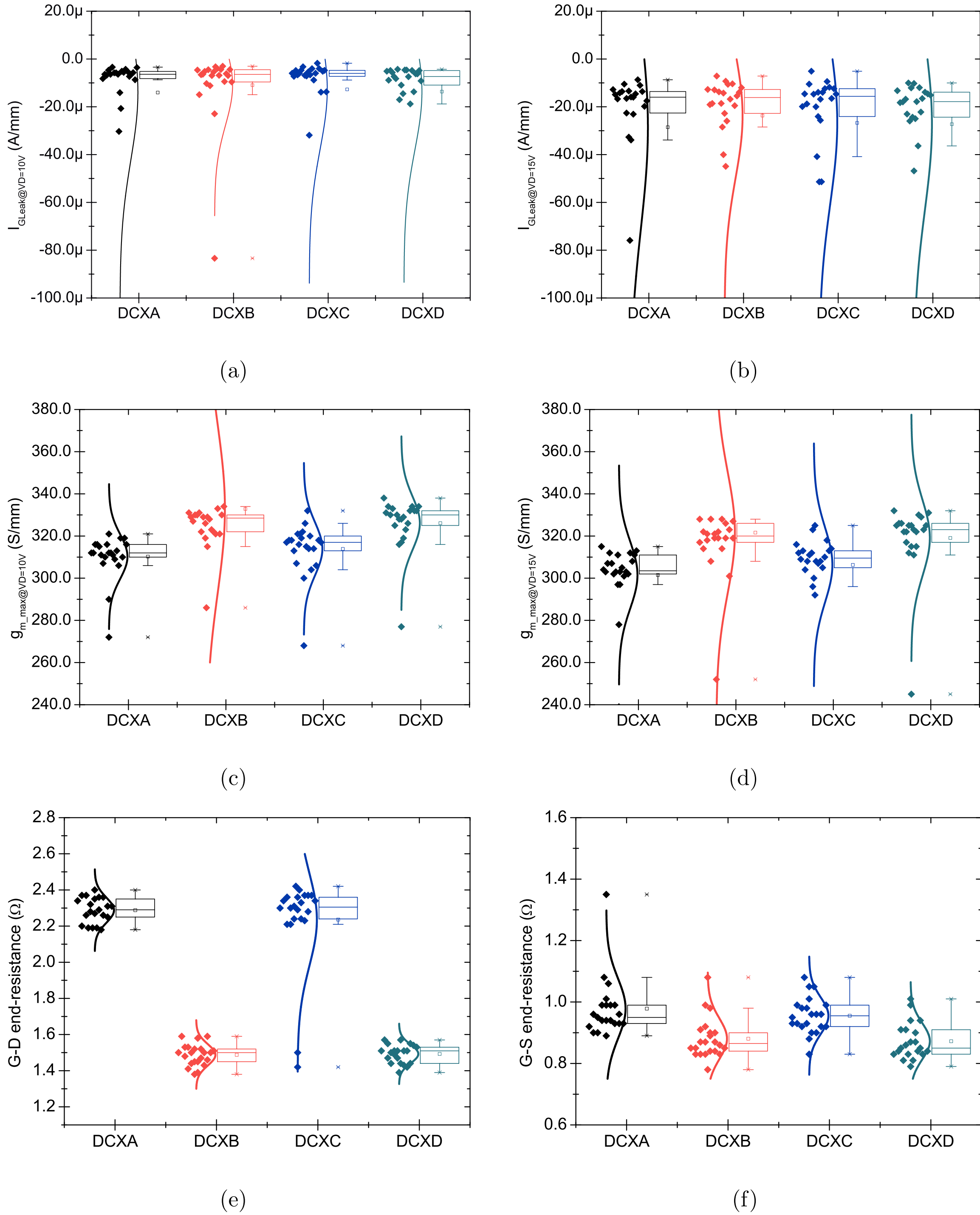


Figure 6.6: *Spread measured in $I_{G_{Leak}}$ (a) at $V_{DS} = 10\,V$, $V_{GS} = -7\,V$ and (b) at $V_{DS} = 15\,V$, $V_{GS} = -7\,V$. Spread in $g_{m_{max}}$ measured (c) at $V_{DS} = 10\,V$, $V_{GS} = 0\,V$ and (d) at $V_{DS} = 15\,V$, $V_{GS} = 0\,V$. Spread (e) in $R_{D_{end}}$ measured at $V_D = 0\,V$, $I_G = 1\,mA/mm$ and $I_S = 0\,mA/mm$ (f) in $R_{S_{end}}$ measured at $I_D = 0\,mA/mm$ and $I_G = 1\,mA/mm$ and $V_S = 0\,V$.*

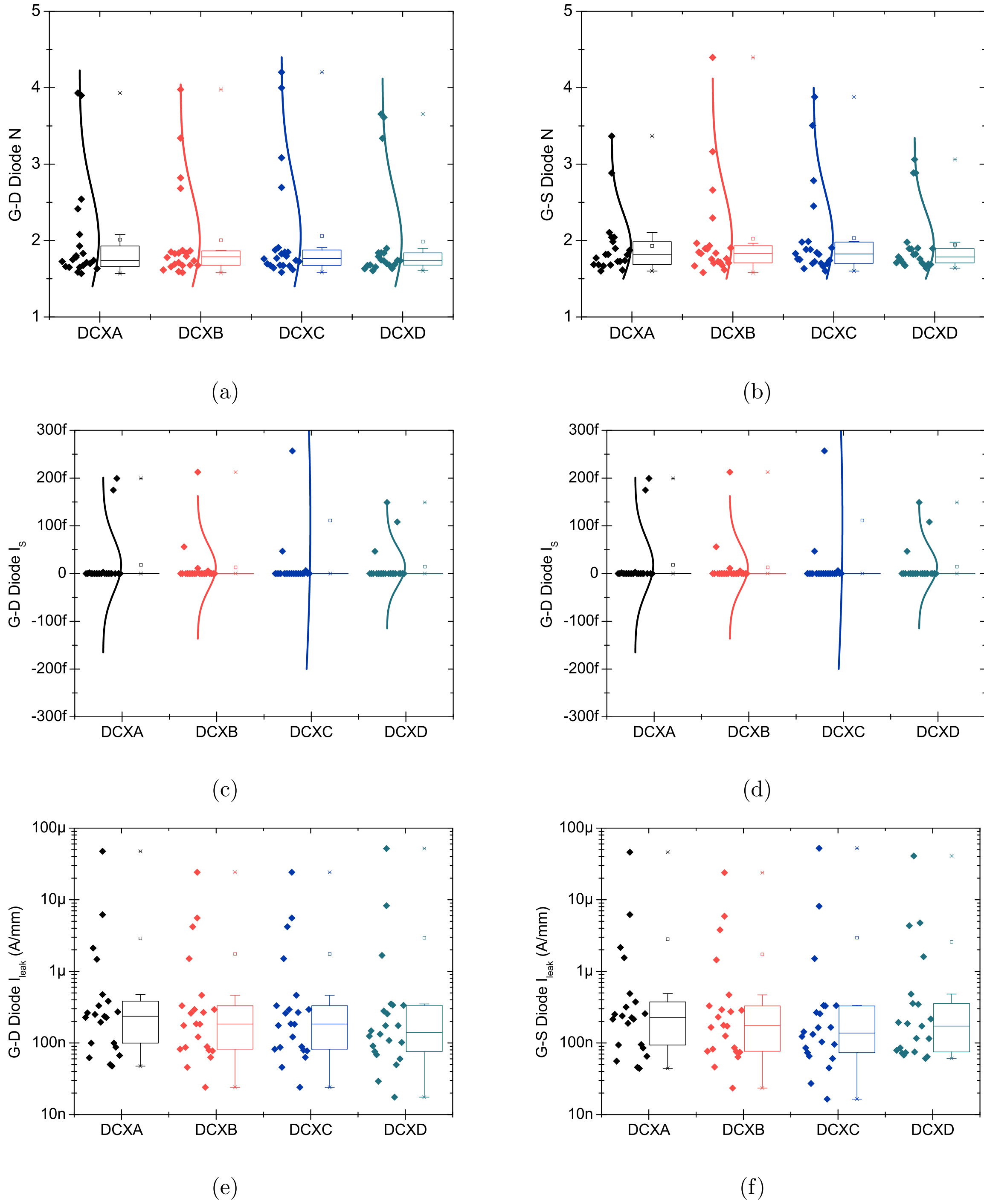


Figure 6.7: *Spread measured in gate-drain diode (a) ideality factor N (c) I_S (e) leakage current at $I_{GS} = -7\,V$ and in gate-source diode (a) ideality factor N (c) I_S (e) in leakage current at $I_{GS} = -7\,V$.*

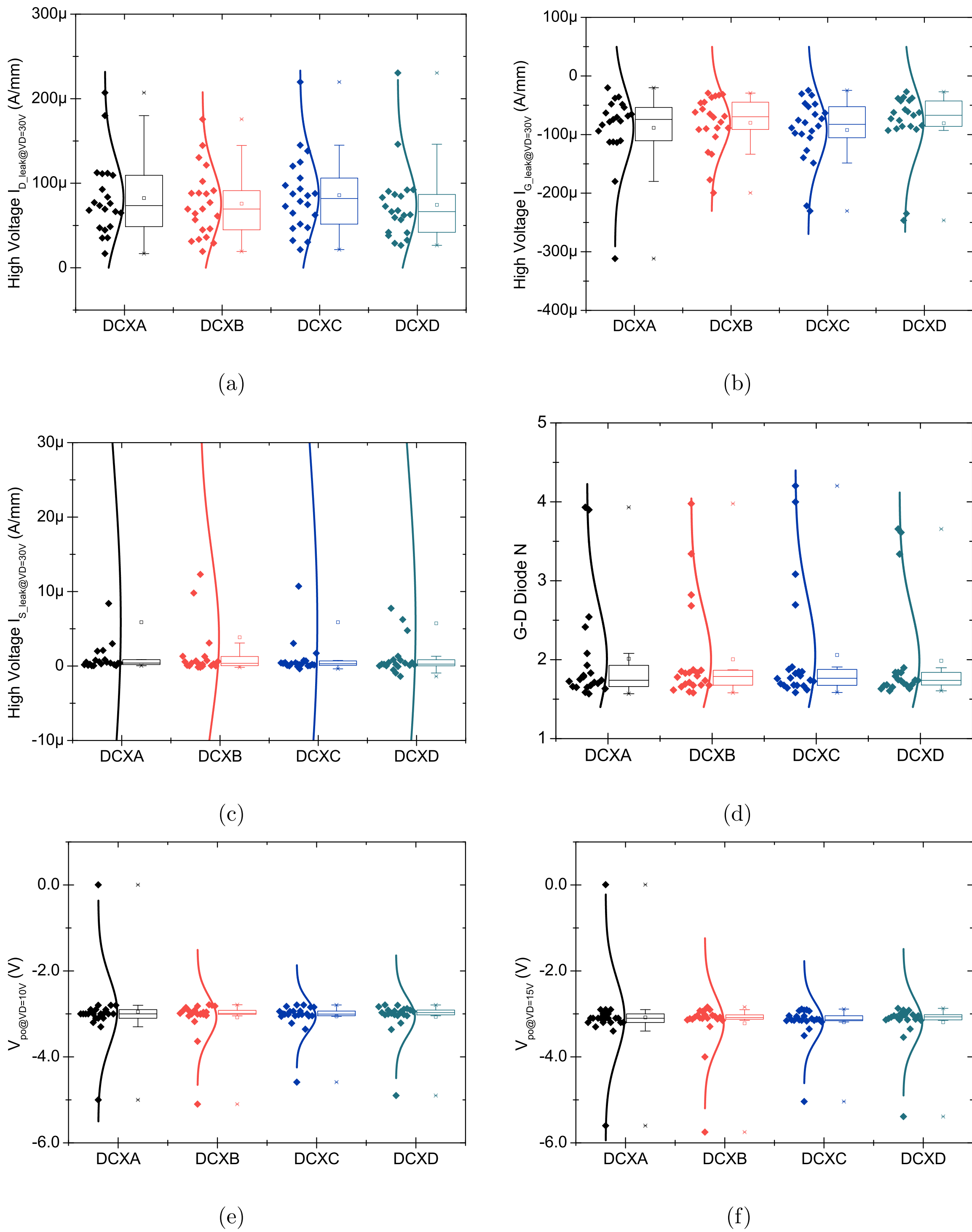


Figure 6.8: *Spread measured (a) in $I_{D_{Leak}}$ at $V_{DS} = 30\,V$, $V_{GS} = -7\,V$ (b) in $I_{G_{Leak}}$ at $V_{DS} = 30\,V$, $V_{GS} = -7\,V$ (c) in $I_{S_{Leak}}$ at $V_{DS} = 30\,V$, $V_{GS} = -7\,V$. Spread (e) in R_{ON} and in V_{po} measured (e) at $V_{DS} = 10\,V$, $I_{DS} = 1\,mA/mm$ (f) at $V_{DS} = 15\,V$, $I_{DS} = 1\,mA/mm$.*

S-parameters characterization

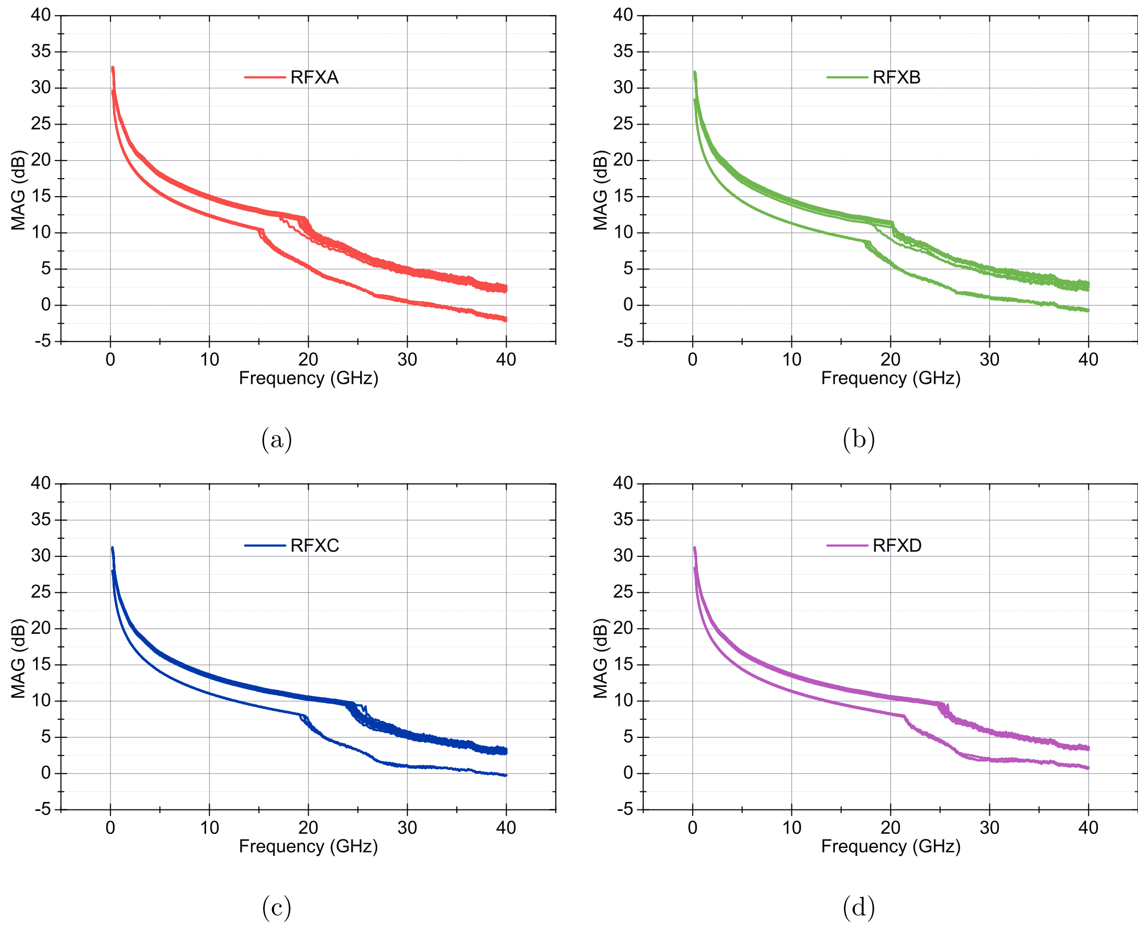


Figure 6.9: *RF MAG measured for (a) RFXA (b) RFXB (c) RFXC (d) RFXD devices.*

In order to characterize RF devices, a characterization to study the behaviour of most common RF parameters was performed; first of all, S-parameters at different load points while changing the frequency of the system. Together with them, also the maximum gain available (MAG) at different frequencies.

All devices available have been tested. Few of them show non-standard behaviour, with lower MAG values and crossover frequencies (Fig. 6.9-Fig. 6.10). Gain behaviour reveals to have a weak dependence from geometries of the devices and only a small $f_{Cross-over}$ shift is visible. It shows substantial difference when field plate is considered: the STFP increases the overall MAG, but the crossover between MAG and MAG occurs at lower $f_{Cross-over}$ (Fig. 6.10); STFP devices have a $f_{Cross-over} \approx 20\,GHz$. Devices without STFP have a lower gain, but in this case the crossover takes place at $f_{Cross-over} \approx 25\,GHz$, which is substantially higher than the previous case. Within

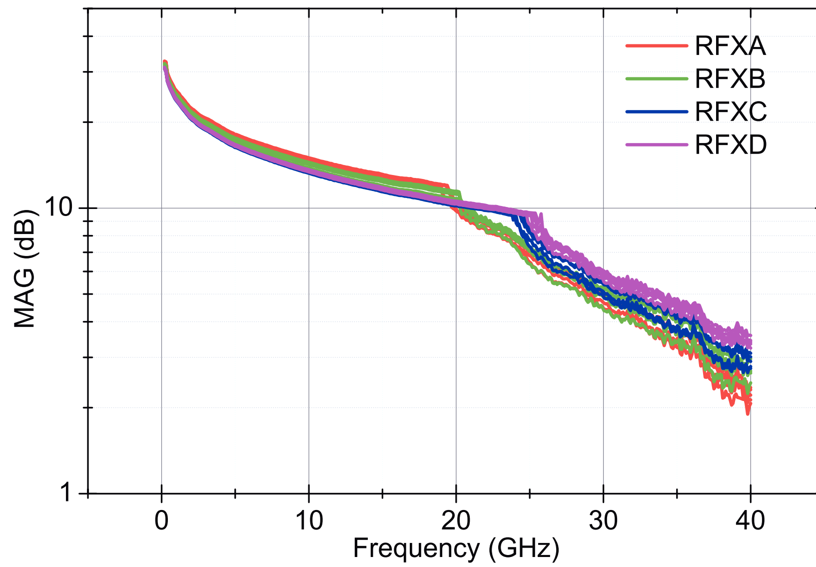


Figure 6.10: *Comparison of the results obtained for all RF devices.*

the frequency window, i.e. from $20\,GHz$ to $25\,GHz$, STFP devices behave worse than their counterpart without field plate, suggesting that a careful analysis of frequency range of application should be necessary when designing a new system. At frequencies higher than $25\,GHz$ the gap between reduces but does not disappear completely. The field plate thus results in a trade-off between crossover frequency and MAG.

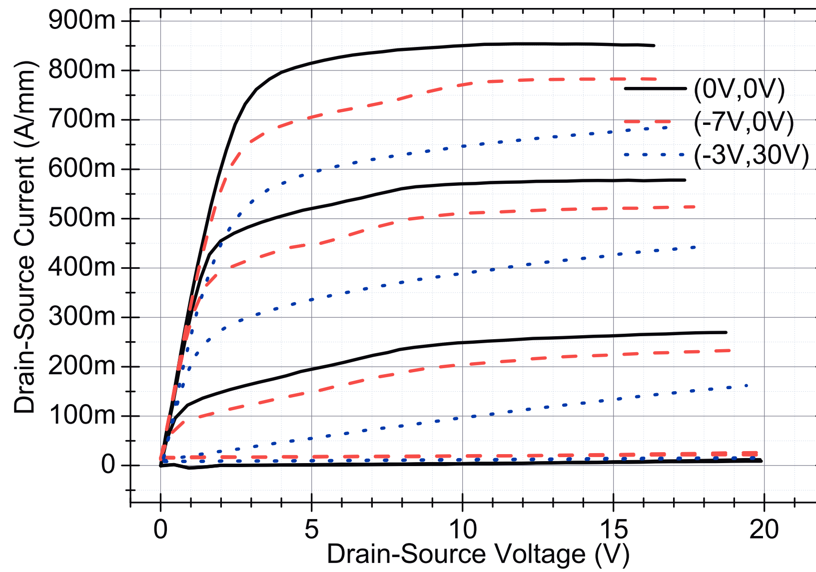
Pulsed characterization

Double pulsed characterization has been carried out on 4 samples per device type. The quiescent bias point applied are $(0\,V, 0\,V)$ (solid line), $(-7\,V, 0\,V)$ (dashed line), $(-7\,V, 30\,V)$ (dotted line), to assess trapping phenomena and current collapse. All the samples show current collapse: the ΔI_{DS} range is approximately from $120\,mA/mm$ to $180\,mA/mm$ and the slump ratio is reported in Table 6.11. A reduced kink effect can be seen especially when the $(-7\,V, 0\,V)$ quiescent bias point is applied. For the evaluation of the slump ratio, the $I_D - V_G$ characteristics at $V_D = 4\,V$, close to the knee voltage where this effect is most meaningful and kink is visible, and at $V_D = 15\,V$ are considered (Table 6.11). All the samples also have a pinch-off shift ΔV_{po} towards less negative voltages; most of the samples measured show a negligible reduction of the transconductance peak. This can be explained with traps mainly located under the gate into the buffer layer, and negligible trapping in the access regions. The results for representative samples, one for each gate-drain distance, are here reported; devices with STFP show no meaningful differences.

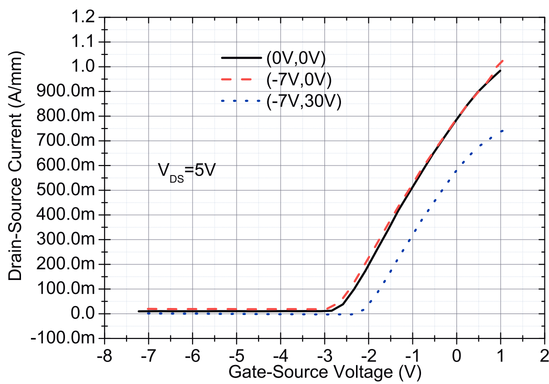
Table 6.11: *Average S.R. at $V_D = 4\,V$ and $V_D = 15\,V$*

Device	Average Slump Ratio	
	$V_D = 4\,V$	$V_D = 15\,V$
RFXA	0.67	0.80
RFXB	0.76	0.85
RFXC	0.66	0.80
RFXD	0.72	0.80

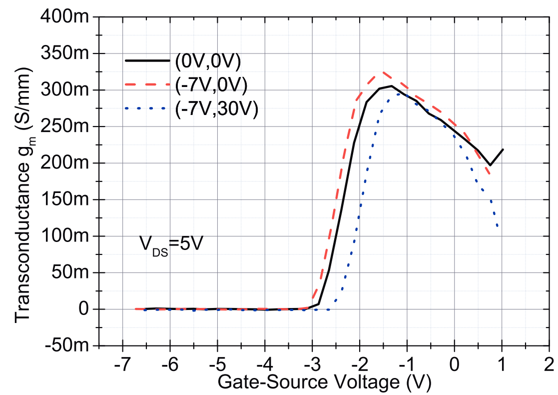
DCXA ($W_G = 1 \times 100\,\mu m$, $L_{GD} = 3.5\,\mu m$, $L_{GS} = L_{FP} = 1\,\mu m$, $L_\Gamma = 0.3\,\mu m$, Γ *Gate, STFP)*



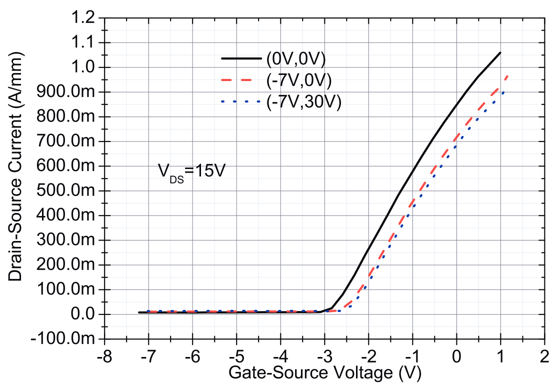
(a)



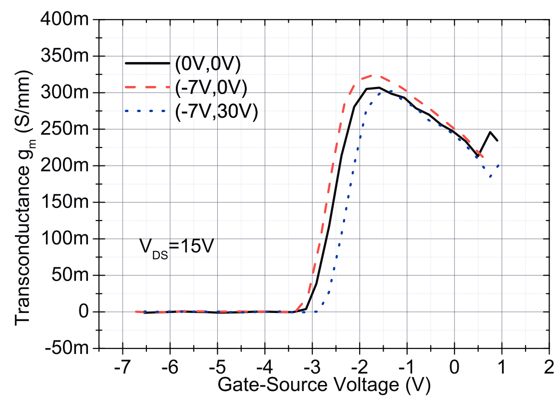
(b)



(c)



(d)



(e)

Figure 6.11: *Pulsed measurements carried out on a standard RFXA device: (a)* $I_D - V_{DS}$*; (b)* $I_D - V_{GS}$ *and (c)* $g_m - V_{GS}$ *at* $V_{DS} = 5V$*; (d)* $I_D - V_{GS}$ *and (e)* $g_m - V_{GS}$ *at* $V_{DS} = 15V$*.*

DCXB ($W_G = 100\,\mu m$, $L_{GD} = 1.7\,\mu m$, $L_{GS} = 0.8\,\mu m$, $L_\Gamma = 0.3\,\mu m$, $L_{FP} = 1\,\mu m$, Γ Gate, STFP)

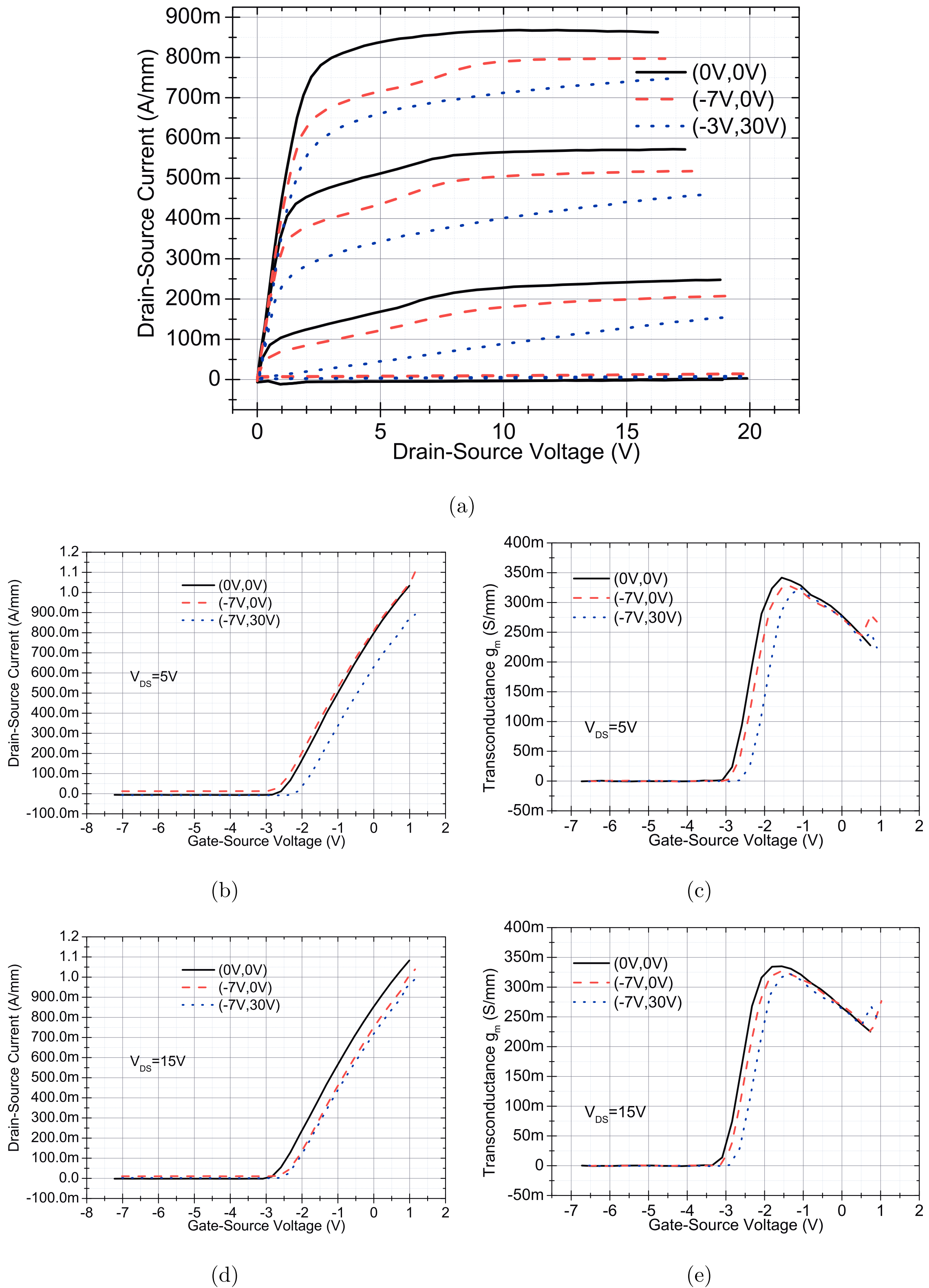
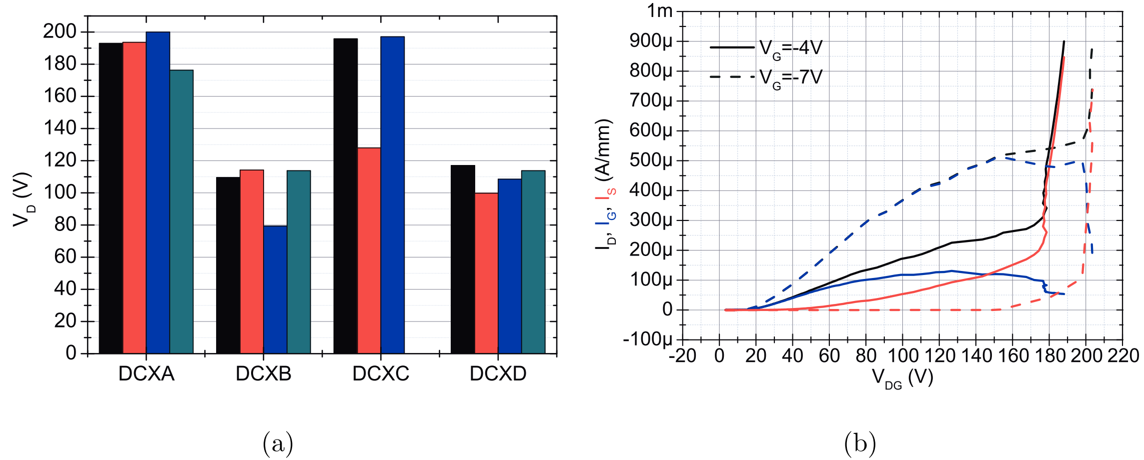


Figure 6.12: *Pulsed measurements carried out on a standard RFXB device: (a) $I_D - V_{GS}$ and (b) $g_m - V_{GS}$ at $V_{DS} = 5V$; (c) $I_D - V_{GS}$ and (d) $g_m - V_{GS}$ at $V_{DS} = 15V$.*

6.2.2 Breakdown tests

This test was carried out sweeping drain current up to $0.9\,A/mm$, increasing V_G from $-7\,V$ to $-4\,V$ at $0.25\,V$ steps, V_S to ground and monitoring the other parameters (V_D, I_G, I_S). The breakdown voltage is taken at $I_D = 0.9\,A/mm$. Some interesting



(a) (b)

Figure 6.13: *(a) BV_{DG} for all devices measured taken at $V_{GS} = -6\,V$. Devices from the same bare die and grouped with other devices with the same geometry. (b) Example of I_D, I_G, I_S for curves at $V_{GS} = -7\,V$ and $V_{GS} = -4\,V$. In this case the sample shown is form bare die AI40, device DCXA.*

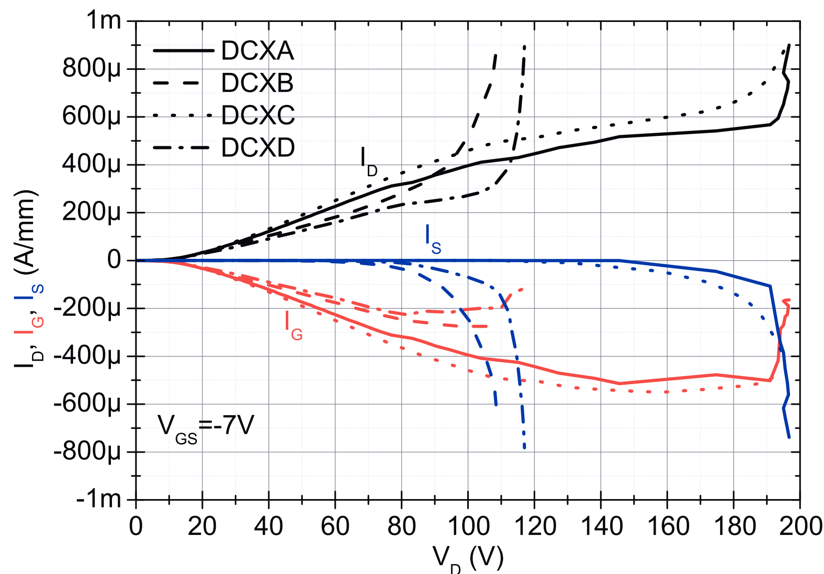


Figure 6.14: *V_{DG}, I_G, I_S measured at $V_{GS} = -7\,V$ for all the 4 device types (Bare die AI 40). I_D (continuous line), I_G (dotted line) and I_S (dashed line) are plotted as function of V_{DG}.*

results can be observed. When a low drain current flows in the devices, the only relevant contribution comes from the gate, where various parasitic phenomena contribute to

carriers flow. At some point, the current reaches a value such that I_D increases, no longer followed by I_G, and I_S steeply grows due to a parasitic channel between source and drain. A sub-surface DIBL can be the cause of the formation of the channel itself. The current level at which it occurs is V_G dependent; increasing the voltage applied to the gate, it decreases due a reduction of the depletion region: the carrier population increases and a conductive path between source and drain is the more likely to form the more the V_G is closer to pinch-off (Figure 6.13). V_G applied and geometry have a high influence on this phenomena; negligible effects seem to be related to availability of field plate (Figure 6.13(a) and Figure 6.14). The main results of this test are here reported. All the curves here reported refer to bare die AI 40.

DCXA ($W_G = 1 \times 100\,\mu m$, $L_{GD} = 3.5\,\mu m$, $L_{GS} = L_{FP} = 1\,\mu m$, $L_\Gamma = 0.3\,\mu m$, Γ *Gate, STFP*)

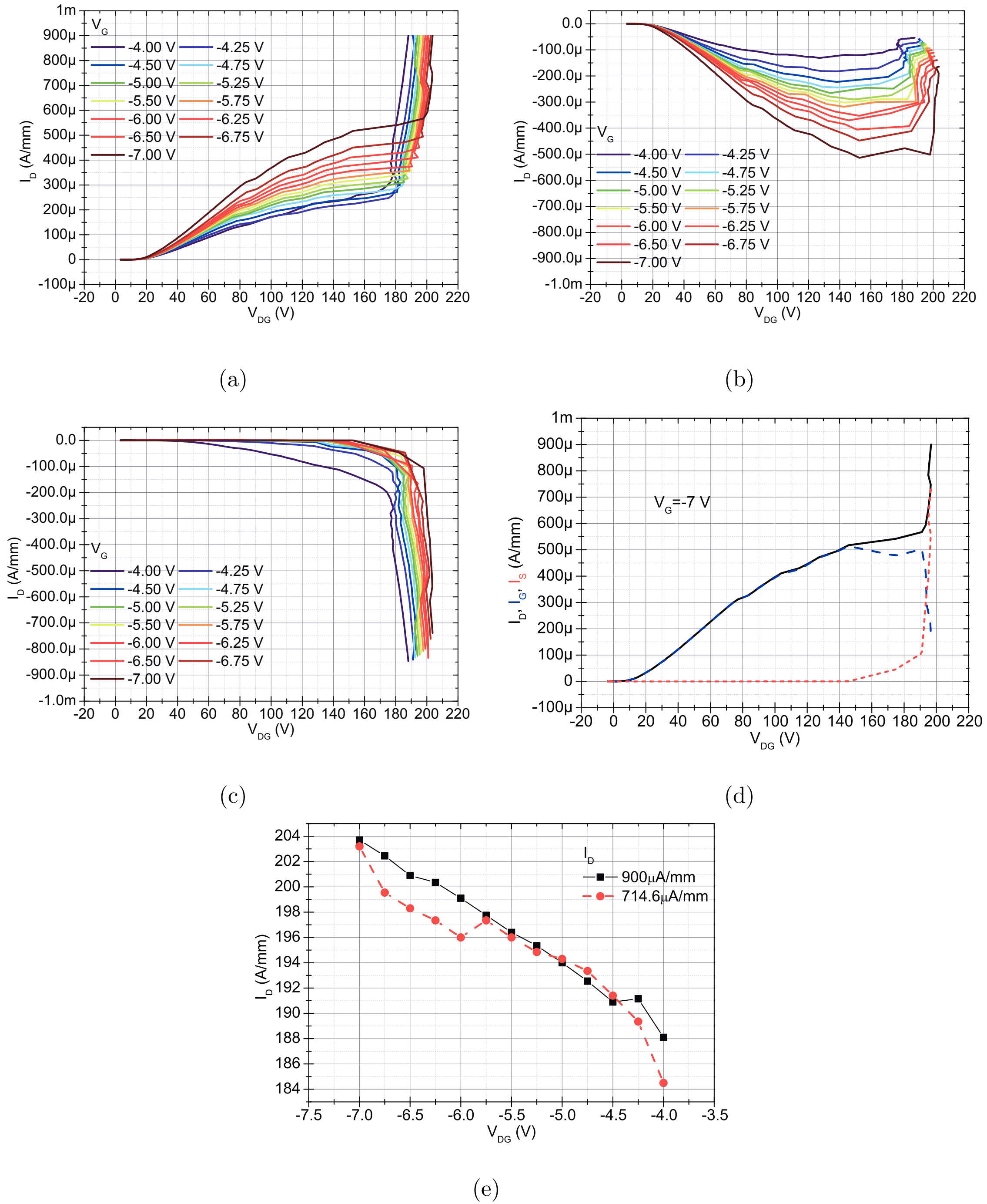


Figure 6.15: *BV measured on DCXA devices: (a)* $I_D - V_{DG}$ *(b)* $I_G - V_{DG}$ *(c)* $I_S - V_{DG}$ *at* $V_{GS} = [-7\,V, -4\,V]$*; (d)* V_D*,* I_G*,* I_S *measured at* $V_G = -7\,V$ *(e)* $V_{DG} - V_G$ *at different* I_D*.*

DCXB ($W_G = 100\,\mu m$, $L_{GD} = 1.7\,\mu m$, $L_{GS} = 0.8\,\mu m$, $L_\Gamma = 0.3\,\mu m$, $L_{FP} = 1\,\mu m$, Γ *Gate, STFP*)

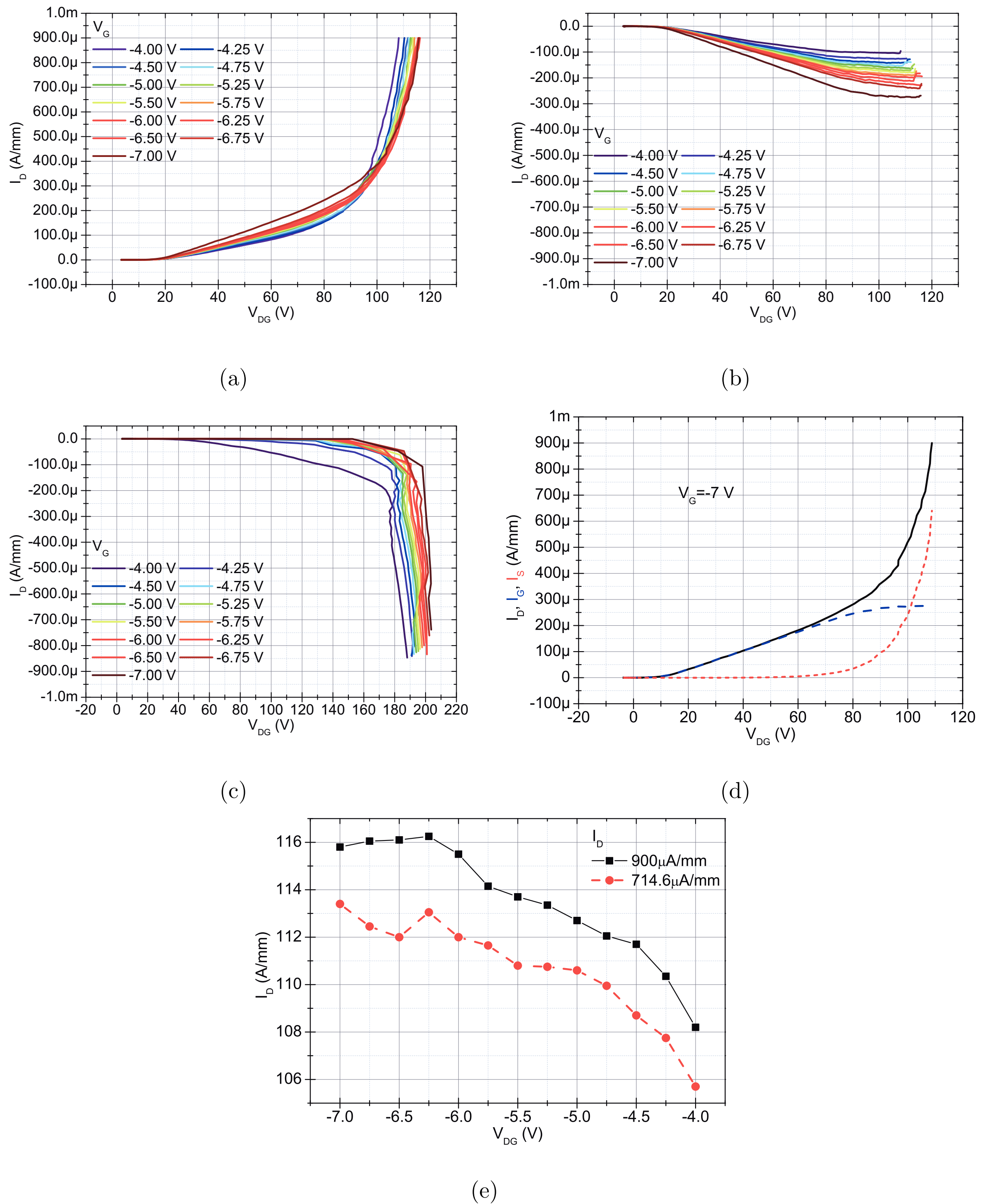


Figure 6.16: *BV measured on DCXB devices: (a)* $I_D - V_{DG}$ *(b)* $I_G - V_{DG}$ *(c)* $I_S - V_{DG}$ *at* $V_{GS} = [-7\,V, -4\,V]$*; (d)* V_D*,* I_G*,* I_S *measured at* $V_G = -7\,V$ *(e)* $V_{DG} - V_G$ *at different* I_D*.*

DCXC ($W_G = 1 \times 100\,\mu m$, $L_{GD} = 3.5\,\mu m$, $L_{GS} = 1\,\mu m$, $L_\Gamma = 0.3\,\mu m$, Γ *Gate*)

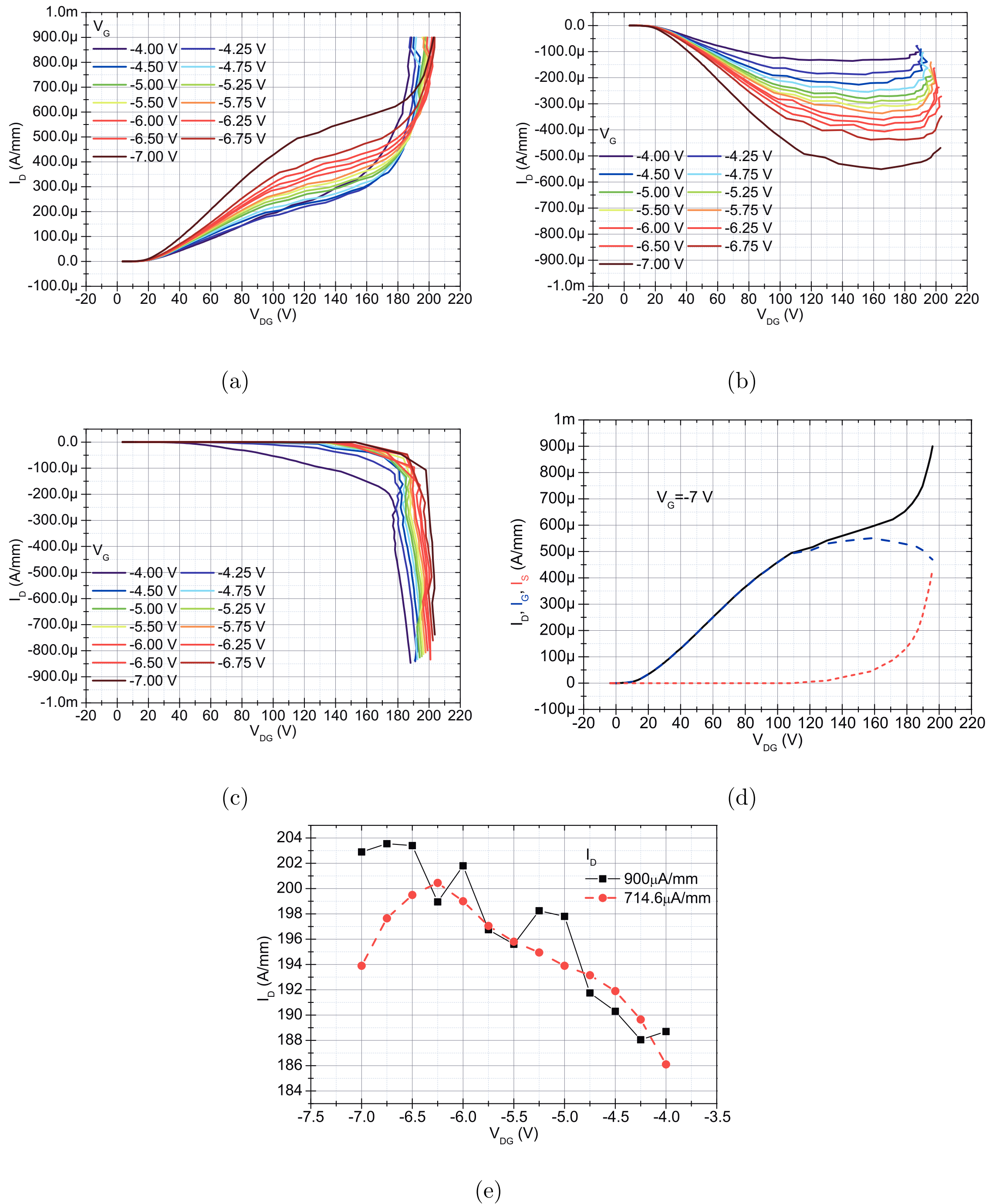


Figure 6.17: *BV measured on DCXC devices: (a)* $I_D - V_{DG}$ *(b)* $I_G - V_{DG}$ *(c)* $I_S - V_{DG}$ *at* $V_{GS} = [-7\,V, -4\,V]$*; (d)* V_D*,* I_G*,* I_S *measured at* $V_G = -7\,V$ *(e)* $V_{DG} - V_G$ *at different* I_D*.*

DCXC ($W_G = 1 \times 100\,\mu m$, $L_{GD} = 1.7\,\mu m$, $L_{GS} = 0.8\,\mu m$, $L_\Gamma = 0.3\,\mu m$, Γ *Gate)*

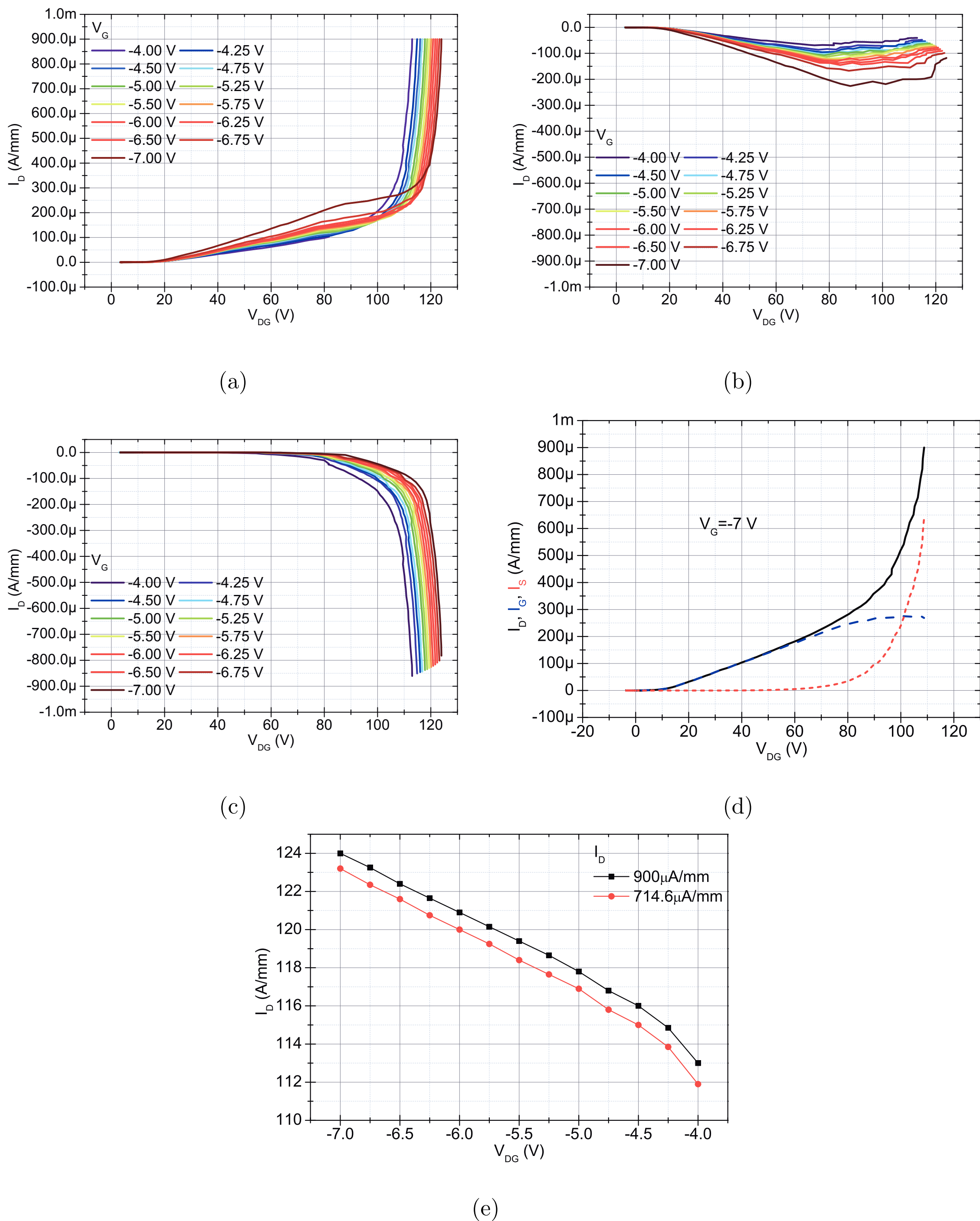


Figure 6.18: *BV measured on DCXD devices: (a)* $I_D - V_{DG}$ *(b)* $I_G - V_{DG}$ *(c)* $I_S - V_{DG}$ *at* $V_{GS} = [-7\,V, -4\,V]$*; (d)* V_D*,* I_G*,* I_S *measured at* $V_G = -7\,V$ *(e)* $V_{DG} - V_G$ *at different* I_D*.*

6.2.3 Reliability

Off-state step-stress

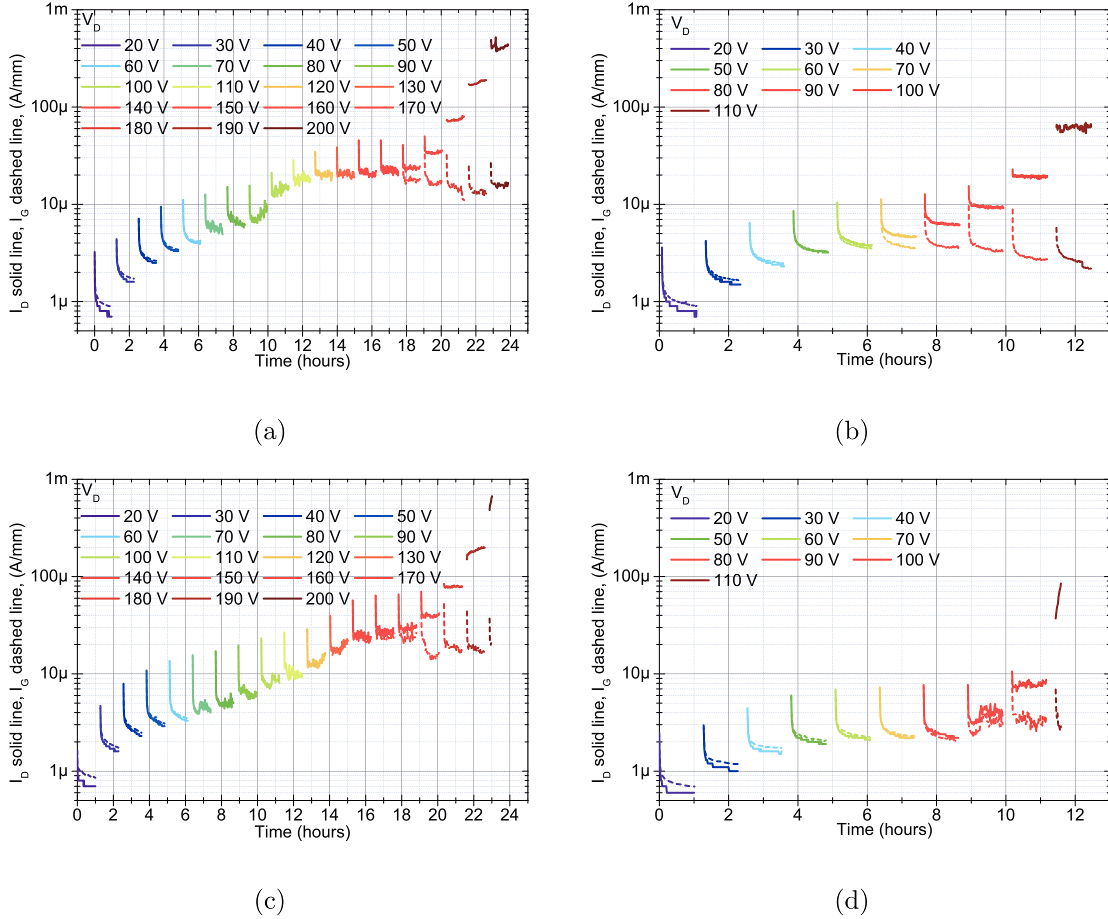


Figure 6.19: *Evolution of the drain and gate currents during the test: (a) DCXA (b) DCXB (c) DCXC (d) DCXD.*

To understand the reliability behaviour on the *GaN* devices designed for the space applications, step-stress tests in deep off-state condition in a three terminal configuration have been carried out. In this test the device is in deep off-state: $V_S = 0\,V$, $V_G = -7\,V \ll V_{po}$ and V_D is increased at $10\,V$ step from $20\,V$ up to failure criteria or to the limit of the instrumentation used. No electroluminescence has been performed during this tests. All the four different devices have been tested, 4 devices per kind to confirm repeatability of the results; before the beginning of the test and after every step a *DC* characterization is performed, and the results include the evolution of all the main curves and parameters. In addition, real-time current during each step are reported. Some interesting observations can be done regarding the results. First, *GH25*

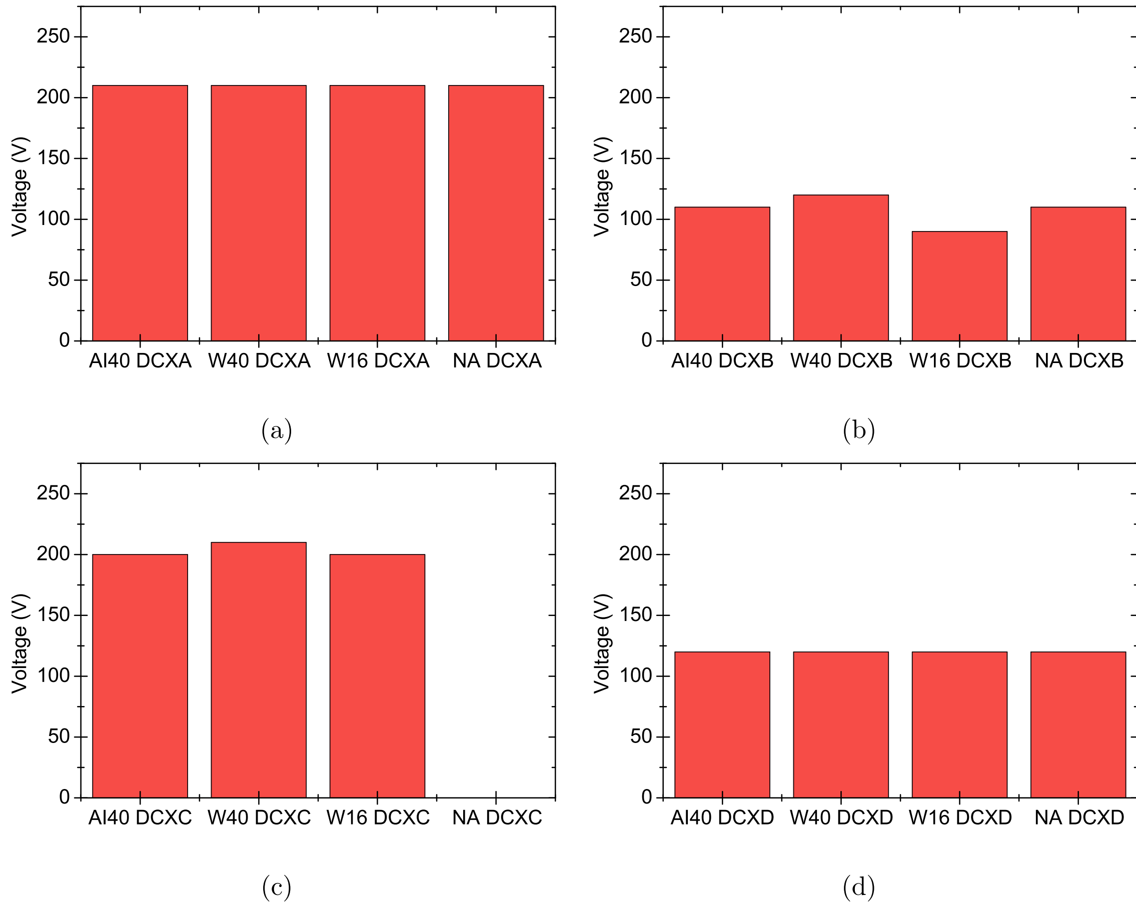


Figure 6.20: *Failure voltages measured in (a) DCXA (b) DCXB (c) DCXC (d) DCXD.*

devices show very good breakdown values, similar to those reported for GH50. Moreover, the results have good repeatability: only small variation are visible comparing the sample of a type. BV_{DS} are reported in Table 6.12. Evolution of the characteristics through the test reveals only negligible alteration of $I_D - V_D$ and transconductance g_m. Increases of the off-state and leakage currents are instead visible in diodes, $I_D - V_G$ and HV measurements (Fig. 6.22 and Fig. 6.23); Results obtained on devices with and without field plate enlighten no meaningful diffetences. The cause of failure is unlikely to be related to gate contact degradation, due to the small variation during the stress

Table 6.12: *Breakdown voltage measured sorted by device type*

Device	Failure voltage	Notes	Device	Failure voltage	Notes
DCXA	210 for all samples	Γ Gate, STFP	DCXB	110, 120, 110, 100	Γ Gate, STFP
DCXC	200, 210, 200	Γ Gate	DCXD	120 for all samples	Γ Gate

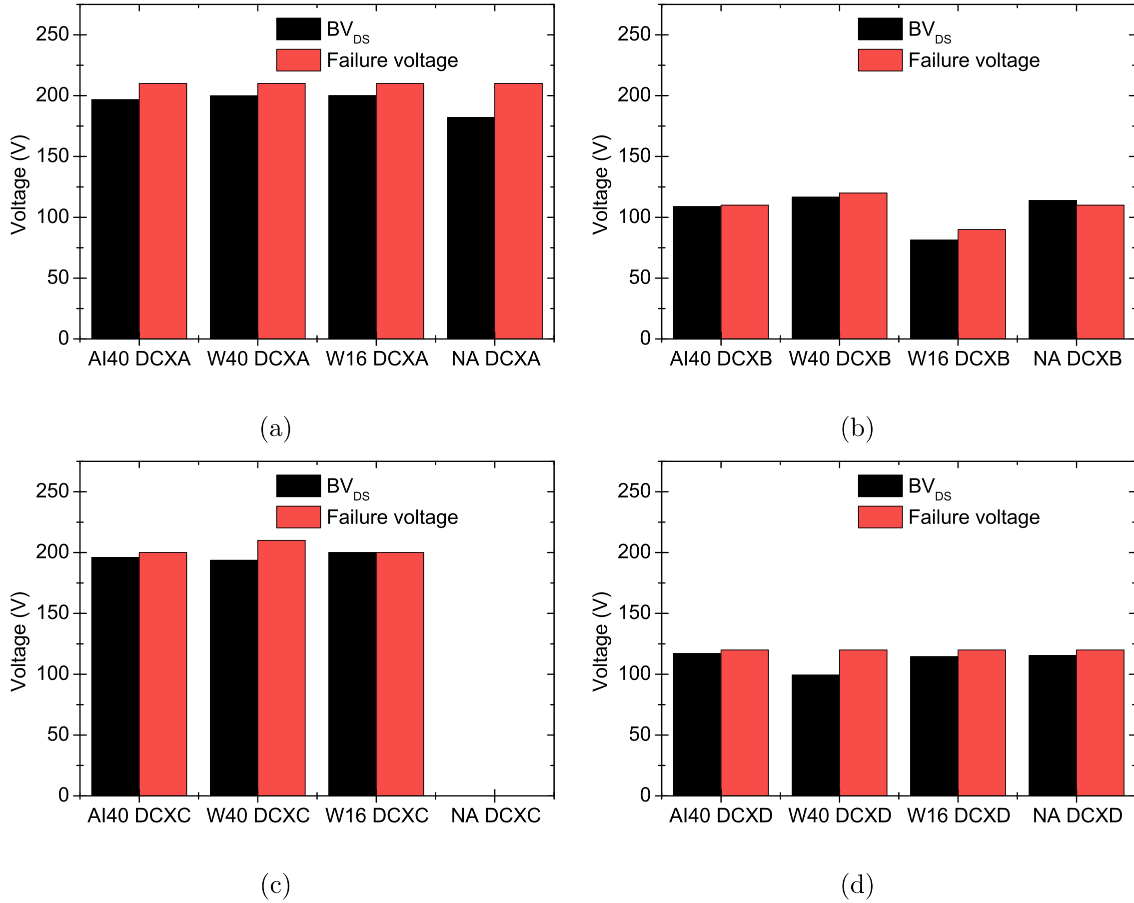


Figure 6.21: *Comparison between BV_{DS} and FV (a) DCXA (b) DCXB (c) DCXC (d) DCXD.*

on the diode electrical characteristic. Comparing the I_D, I_G, I_S characteristics of the breakdown voltage with the evolution of the parameters in the off-state step stress in devices with longer L_{GD}, the range of voltages can be subdivided into 3 region. A first one that goes up to $\approx 70\,V$: degradation in off-state step stress is almost absent and some parameters can also slightly improve (see $I_D - V_G$ measurements and parameters); in breakdown measurement all current are still very small. The second region, from $\approx 70\,V$ to $\approx 150\,V$: in both tests the current increases and is almost completely sustained by the gate which shows a fast degradation. Last, above $\approx 150\,V$ when the punch-through takes place as confirmed by I_S sudden increase, a region where most of the current comes by the source and the degradation in off state is slower-than in the previous region.

The results of this test are compared with those obtained with the breakdown test (Fig. 6.21). The difference between the voltage measured can be in part explained by the different setup of the two measurements and in the longer dwell time at low voltages in

case of off-state step stress, that, due to some sort of breakdown walkout, contributes in improving the critical voltage. The comparison reveals that it is highly probable that the cause of the catastrophic degradation is related to the same phenomena that causes the strong increase of I_D in the first test.

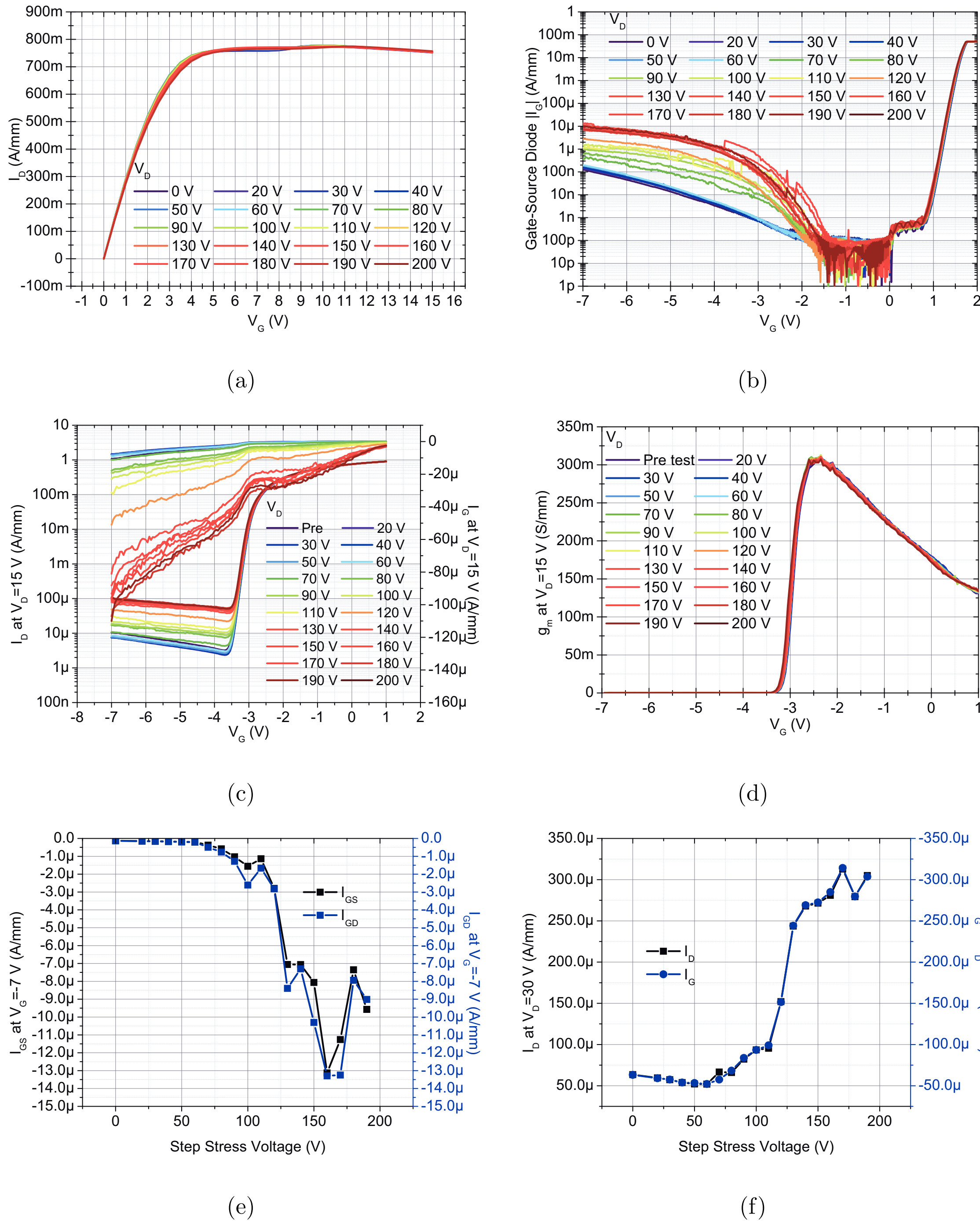


Figure 6.22: *Evolution of the electrical characteristics during the off-state step stress in a standard $L_{GD} = 3.4\,\mu m$ device with field plate; devices without field plate show similar results. (a) drain current I_D (b) gate-source diode (c) $I_d - V_G$ (d) g_m (e) gate-source leakage (f) HV leakage.*

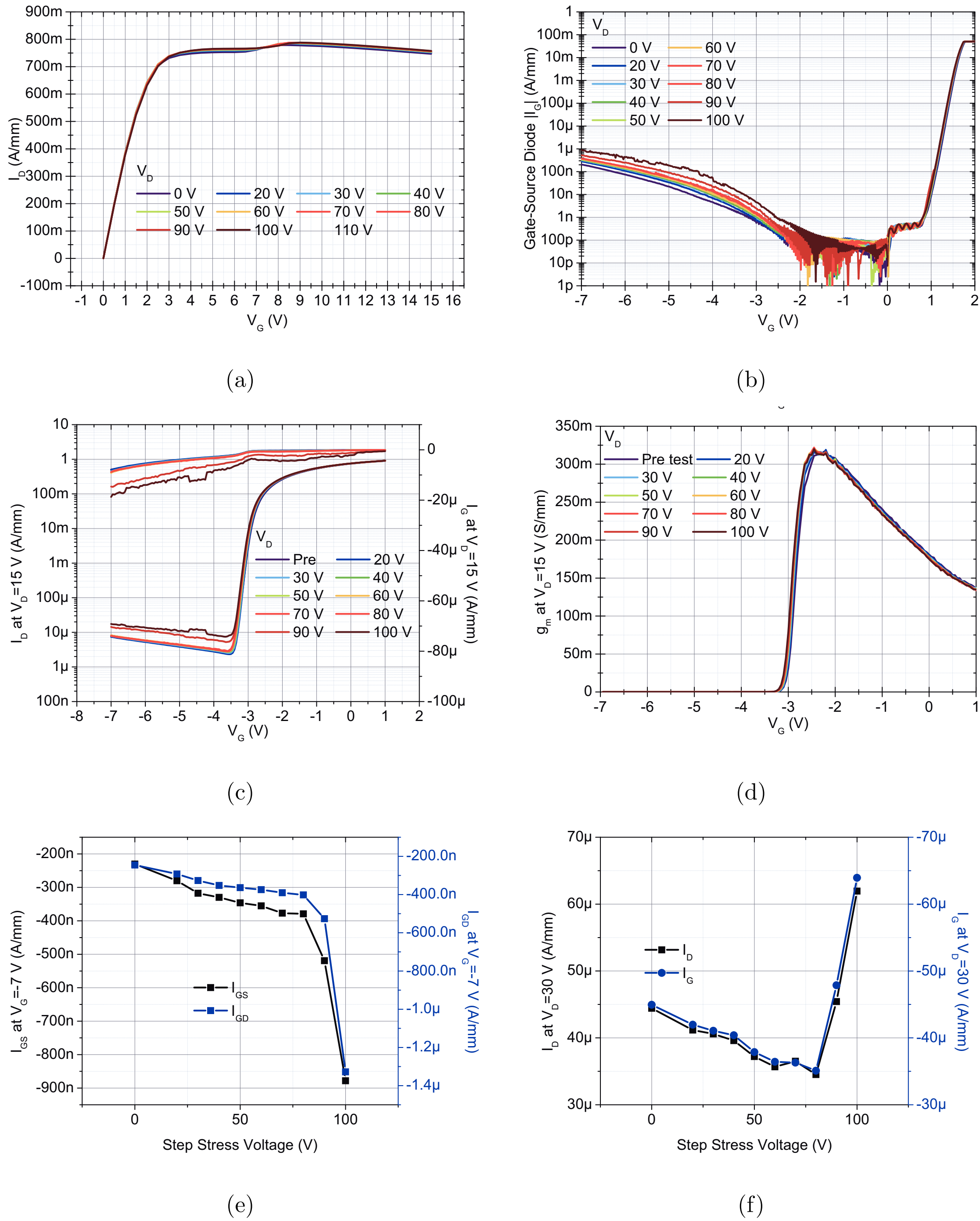


Figure 6.23: *Evolution of the electrical characteristics during the off-state step stress in a standard $L_{GD} = 3.4\,\mu m$ device with field plate; devices without field plate show similar results. (a) drain current I_D (b) gate-source diode (c) $I_d - V_G$ (d) g_m (e) gate-source leakage (f) HV leakage.*

Load line life test

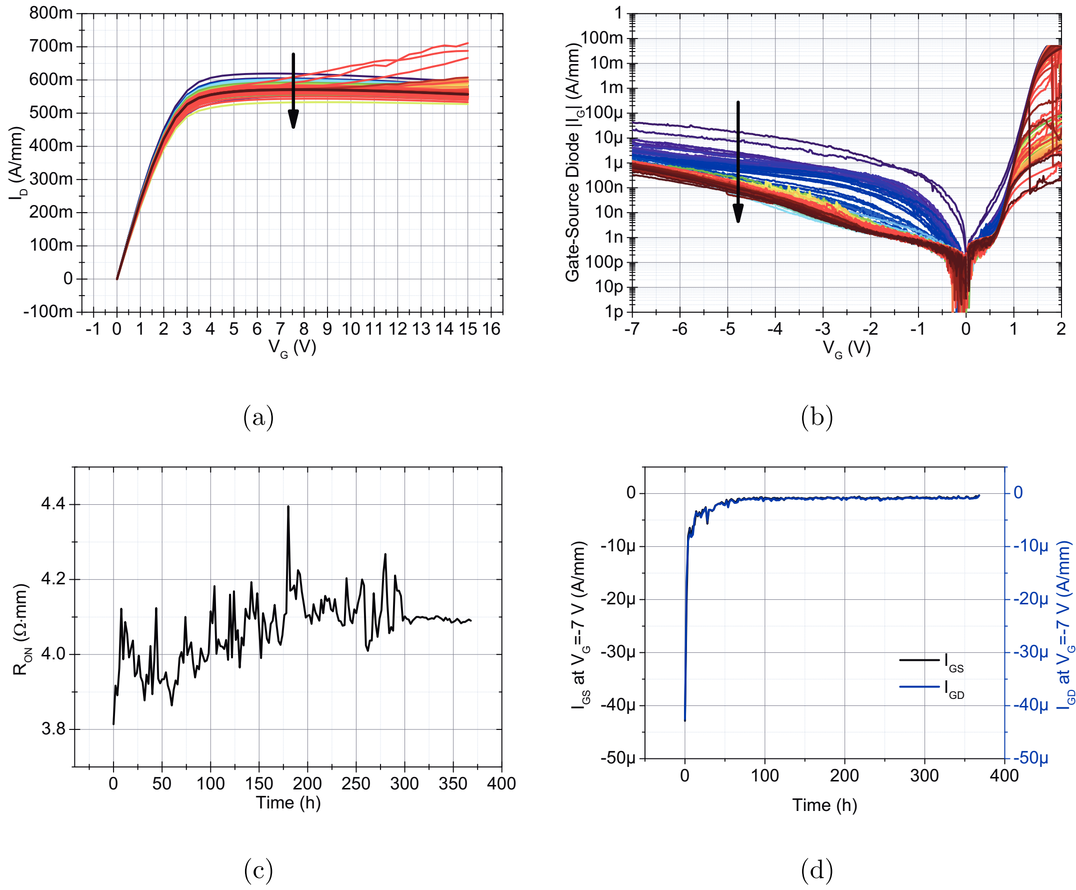


Figure 6.24: *Life test $I_{DS} = 660\,mA/mm$, $V_{DS} = 10\,V$, $T_{Test} = 423\,K$.*

3 working point in the load line as defined for *GH25* devices (from the knee point at $V_G = 1\,V$ to $I_D = 0\,A$, $V_D = 60\,V$) have been chosen to study the evolution of the devices (1) under high voltage and reduced currents, (2) at high voltage and currents and (3) low voltage but high currents. For all of these points a test has been carried out for a variable dwell time at fixed bias condition at a temperature $T_{Test} = 423\,K$. Device chosen for this test was the DCXD ($W_G = 1 \times 100$, $L_{GD} = 1.7\,\mu m$, $L_{GS} = 0.8\,\mu m$, $L_\Gamma = 0.3\,\mu m$, Γ Gate)

- 1 samples $I_{DS} = 660\,mA/mm$, $V_{DS} = 10\,V$, $T_{Test} = 423\,K$
- 1 samples $I_{DS} = 400\,mA/mm$, $V_{DS} = 30\,V$, $T_{Test} = 423\,K$
- 1 samples $I_{DS} = 5\,mA/mm$, $V_{DS} = 60\,V$, $T_{Test} = 423\,K$

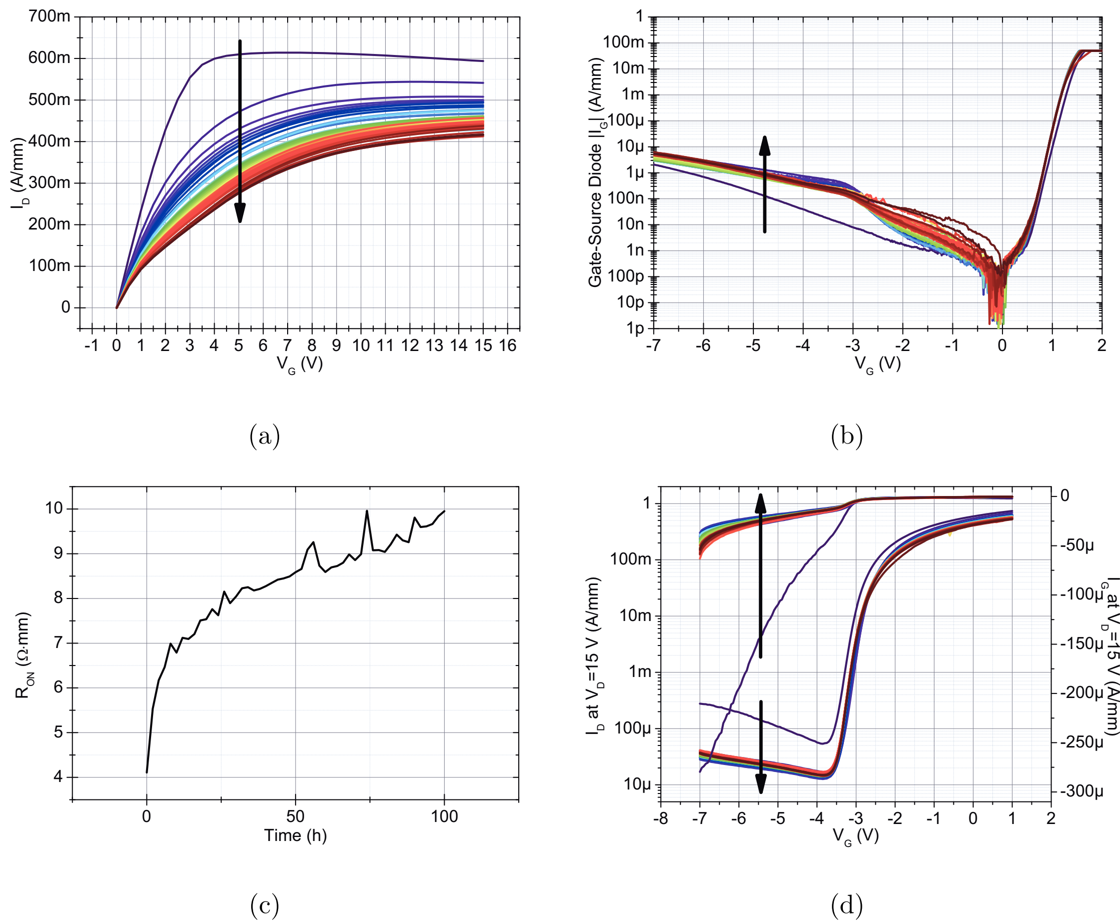


Figure 6.25: *Life test* $I_{DS} = 400\,mA/mm$, $V_{DS} = 30\,V$, $T_{Test} = 423\,K$.

Under high current and low voltage biasing condition (Fig. 6.24), sample shows a reduction of off-state and leakage currents together with the drain current. The pinch-off voltage V_{po} shifts towards less negative voltages, while the on-resistance increases. After $\approx$ 50 hours, the device seems to reach a stable condition, as confirmed both by curves and evolution of parameters monitored. The device was tested for 368 hours.
The sample in Class A (Fig. 6.25) was biased for only 100 hours. Small changes are visible in the diodes and $I_D - V_G$ characteristics; most interesting changes regards the strong decrease of the output current in $I_D - V_G$ together with steep increase of the on-resistance: their evolution seems to be strictly connected and occurs only in this bias point. No other parameter follow the same trend.
In the last biasing condition, results similar to those seen for the off-state step stress are reported (Fig. 6.26): increase of off-state leakage, negligible variation of the drain current, pinch-off shift towards less negative gate voltages; also, the on-resistance is

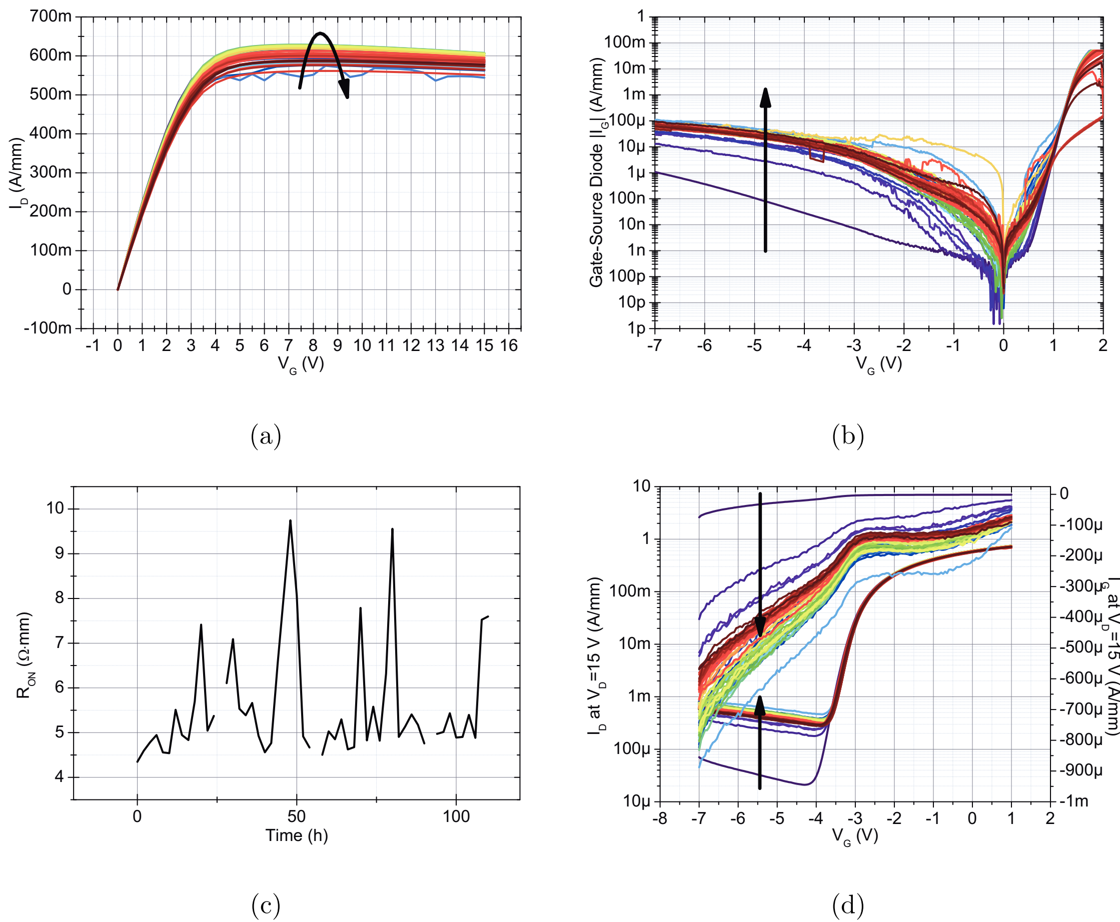


Figure 6.26: *Life test* $I_{DS} = 5\,mA/mm$, $V_{DS} = 60\,V$, $T_{Test} = 423\,K$.

almost stable after the first few steps. This indicates a degradation of the Schottky barrier height, due to formation of traps during the stress, while the access regions seem not to be significantly affected.

From the test carried out, it is clear that Class A results show a fast degradation of the output current and a steep increase of on-resistance within 100 hours; similar results are visible when the sample is biased at high current and low voltage, even if at a much lower degree. When the device is biased at high voltage and low currents, only a small decrease of output characteristic is reported; on the other hand both off-state and leakage currents significantly increase.

The Class A condition is the worst working condition. Two possible hypothesis can be proposed: The degradation can be caused (i) by high power and visible only when high voltage and high current are applied (ii) by high temperature to which both the power dissipation and the high temperature jointly contribute. Additional tests at

room temperature could help to understand the failure mechanisms.

Conclusions

In this work, a systematic study was carried out dealing with many different aspects of the GaN technology. Instability, breakdown and reliability have been under investigation to identify an optimal heterostructure design that could grant the exploit of all the excellent properties of the GaN-based devices minimizing it side effects.
Great attention has been devoted to the breakdown phenomena. The main intent has been understanding the physics behind the phenomenon, and the factors that influence it. The analysis reveal that breakdown is mainly related to two phenomena that jointly contribute to it: gate leakage current contributions (TFE, tunneling, hopping), and punch-through, that is the formation of a parasitic path between source and drain, that can be easily spotted monitoring the source current. The former takes place when the device is biased in a deep off-state condition and the depletion region is wide; on the other hand, the more this region becomes thinner, the more is the probability that the latter may occur.
The breakdown behavior with temperature show two different temperature coefficient: a negative one with a reduction of the BV and a positive one above $100\,°C$. The non-monotonic behavior can find a possible explanation in the co-existence of two different mechanisms. Increasing temperature between $30\,°C$ and $100\,°C$, significantly increases gate-drain leakage current components, and hence decreases the breakdown voltage. As far as the increase in breakdown voltage detected for $T > 100\,°C$ is concerned, previous reports suggested that breakdown current may partly originate from impact ionization. Under this assumption, the increase in temperature causes a decrease of the impact ionization rate because of the increased lattice vibrations; hence breakdown would be more difficult and this would result in a positive temperature coefficient in the high temperature region.

It as also been confirmed the importance of electroluminescence measurements as a means to study evolution of the breakdown. Electroluminescence investigation suggests that, independently of the origin of breakdown current, the highly accelerated electrons (either coming from the gate, or from the source injected towards the drain may release their excess energy (in proximity of the drain) by emitting visible light. It is worth noticing that emission originates from several hot spots distributed all along the width of the gate: these spots represent preferential breakdown sites, and possibly correspond to weak areas originated by defects formation during layer deposition and/or processing.

A comparison between the different SH design has proven itself to suffer from many issues as the many tests confirmed. The SH devices suffer from kink and trapping, but in particular, the worst result are the soft breakdown, which is mainly caused by the poor capability in confining electrons into the channel layer, allowing thus charge spill-over, or punch-through. For the same reason, the single-heterostructure achieved poor results in reliability tests, where the device show a poor failure voltage and a fast degradation of the electrical properties.

Double-heterostructure wafers show improved performances. The introduction of the back-barrier significantly improved the ability to confine electrons in the GaN channel region thanks to the additional band-gap at the channel/back-barrier interface. This effect strongly depend on the Al concentration in the back-barrier and in the channel thickness; unfortunately, they are accompanied by DH epilayer design reduces the maximum current and causes a positive shift of the V_{po}. The lower leakage current and improved electron confinement has proven essential to have a better breakdown; the back-barrier postpone punch-through, enabling DH design both to improve BV up to $600\,V$ and to scale with L_{GD}. Moreover, DH show a much better reliability.

Even if a very good blocking capability has been achieved in this way, it is still far from the threshold of $1000\,V$. This results could be granted by using a doped GaN buffer. In this case, an analysis has been performed considering both carbon and iron. The use of Fe as dopant has shown interesting result. Iron doped devices have good electrical properties, and, compared to the other wafer, have a low R_{ON} collapse. They also achieved a better breakdown slope with respect to DH ones, but, in our tests, the breakdown measured saturates at $\approx 600\,V$ when $L_{GD} = 12\,\mu m$; this technology reaches

the same BV at a smaller gate-drain distance, but does not improve the maximum BV. Moreover, in reliability tests, $SH : Fe$ devices show a lower failure voltage than DH or $SH : C$.

The epilayer design using carbon positively overcome the $600\,V$ barrier, and reaches the limit of $1000\,V$ at $L_{GD} = 7\,\mu m$, with the best slope ($\approx 130\,V/\mu m$). Outstanding results have been obtained in the reliability tests: devices could reach the $1000\,V$ without significant degradation. On the other side, these devices show extremely high current collapse phenomena and an increase in R_{ON} up to $\approx 350\,\%$. In this case, the use of carbon as a dopant seems to be deleterious for the on-resistance stability

Breakdown tests involved also the analysis of the different biasing condition applied at the substrate. Tests carried out enlighten that, if the substrate is grounded, the devices suffer from vertical current, that causes a soft breakdown. This could be a significant problem if the device is used in application were it is usually biased.

Data confirmed that both the double-heterostructure and the iron-doped single heterostructure reaches breakdown condition at $\approx 170\,V$, with no meaningful difference between the two different epilayer designs.

The problem cannot be ascribed to the conductive n-type substrate; the use of a semi-insulating substrate has prove itself useful for the $SH : Fe$ wafer, improving above $200\,V$ the vertical breakdown, but the double-heterostructure show no improvement, suggesting that a different solution, for example an higher band-gap at the channel/back-barrier interface, should be used also.

The use of field plates, single or multiple gives contrasting results. Only gate field plated devices could withstand few hundred $\mu A/mm$, improving the breakdown. All the other solutions not only were ineffective, but reduced the BV. Similar results are visible in reliability tests, were $2FP$ have been tested. The devices have, at best, the same failure voltage as nFP devices, but most devices show a lower one. The use of field plates seems to be still not completely mature in the devices tested so far.

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