UNIVERSITÀ DEGLI STUDI DI PADOVA

Facoltà di Ingegneria

Dottorato di ricerca in
Scienza e Tecnologia dell'Informazione

Tesi di Dottorato

RELIABILITY AND PARYLENE ENCAPSULATION OF ORGANIC DEVICES

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CICLO XXIII

***Cutter**: You settled on a name yet?*
***Robert Angier**: Yes I have. The Great Danton.*
***Cutter**: Bit old-fashioned, isn't it?*
***Robert Angier**: No. It's sophisticated.*

from Christopher Nolan's "The Prestige", 2006

A Roberto, Lucia, e Luna ...

Abstract

Organic semiconductors are at the basis of a relatively new research field, called Organic Electronics. The study of the photo-conductive, electrical and optoelectronic properties of organic materials, the charge and exciton transport as well as the thin film growth has led to the development of *organic* transistors, LEDs and solar cells. More complex organic designs, like flexible electronic circuits, photovoltaic panels and Radio Frequency IDentification (RFID) tags are under development, while OLEDs modules are nowadays one of the most promising technologies for display and lighting application and their break-in the mainstream electronic markets is forthcoming.
In this context the stability over time of the organic semiconductor, the use of a proper encapsulation, and a sufficient lifetime of the encapsulated organic devices become essential in order to achieve the success of this technology. Moreover, the investigation of the physical phenomena behind the degradation of the performance of the basic organic devices is both a scientific challenge and an appealing quest for the research community.

During the last three years I mainly focused my studies on two kind of organic devices, namely Organic Light-Emitting Diodes (OLEDs) and Organic Thin-Film Transistors (OTFTs).
More precisely I have worked in two domains: the first part of my work concerns the study of the reliability and thermal properties of OLEDs, mostly based on Alq3 Electron Transport Layer (ETL), and NPD Hole Transport Layer (HTL). These studies have been carried out by investigating the variation of the electrical, optical and thermal characteristics of the devices, during reliability stress tests. Within this work we have tested OLEDs with different inner structure (sort and thickness of the organic layers as well as of the contacts), different size and shapes of the active area. Both temperature and current have been singularly used as stress accelerating factors. The carrying out of reliability tests at different stress current values has allowed to extrapolate degradation laws, and consequently to calculate lifetime laws. Our studies on phosphorescent OLEDs stressed at different current levels, show an increase of the operating voltage univocally correlated with the number of carriers injected in the devices during the stress.
Electro-luminescence degradation mechanisms in small-molecules based OLEDs have been investigated. In particular, we focused on intrinsic degradation phenomena that determine the decrease of the optical power during standard operation. The results of this analysis provide information on the physical processes responsible for OLEDs degradation, suggesting a strong correlation between the reduction in the luminance intensity of the devices and the occurrence of defects

and positive trapped charge at the Alq3/NPD interface.
Moreover, we studied the uneven decrease of the optical power along the active area of OLEDs subjected to electrical stress tests. This phenomenon has been correlated to the self-heating and surface temperature profile of the devices. A current crowding phenomenon has been hypothesized in order to explain the light emission, as well as the surface temperature distribution.
An extensive study has been applied to the thermal properties of the anode layer of the OLEDs, by comparing devices built with different Transparent Conductive Oxides (TCO). Particularly, the performance and reliability of OLEDs with Indium-Tin Oxide (ITO) and Indium-Zinc Oxide (IZO) anode contact layer have been investigated. The devices have been compared in terms of efficiency, thermal resistance and reliability. The results of this study have shown that OLEDs with IZO anodes guarantee performance comparable with OLEDs with ITO anodes, and proved a better heat dissipation as well as longer lifetime.

The last part of my work is related to the technological development of both bottom and top contact OTFTs, and to the study of their stability. By working in collaboration with the European microelectronic research centre *IMEC*, we have manufactured innovative photo-lithographic patterned top contact OTFTs. By using a wet etching process, we have realized top contact OTFTs with 10μm channel length, obtaining mobilities greater than $0.5cm^2/(Vs)$. Moreover, we have developed an innovative process flow that allows the patterning of Silver source-drain contacts on the top of the organic semiconductor, by using plasma dry etching. The process flow has been proved on silicon, as well as on foil substrate. Finally, we have investigated the reliability of standard Pentacene-based organic transistors and the encapsulation of these devices by using a poly(p-xylylene) polymer (Parylene C).

List of Publications:

A. Pinato, M. Meneghini, A. Tazzoli, A. Cester, N. Wrachien, E. Zanoni, G. Meneghesso, B. D'Andrade, J. Esler, S. Xia, J. Brown. "Indium Zinc Oxide as an alternative to Indium Tin Oxide in OLEDs Technology". HeTech'08, 17^{th} European Workshop on heterostructure Technology, 2008

A. Pinato, M. Meneghini, A. Cester , N. Wrachien, A. Tazzoli, E. Zanoni, G. Meneghesso, B. D'Andrade, J. Esler, S. Xia, J. Brown "Improved Reliability Of Organic Light-Emitting Diodes With Indium-Zinc-Oxide Anode Contact", 2009 IEEE International Reliability Physics Symposium, Montreal, Canada, April 26-30, 2009

A. Pinato, A. Cester, M. Meneghini, N. Wrachien, A. Tazzoli, S. Xia, V. Adamovich, M. S. Weaver, J. J. Brown, E. Zanoni, G. Meneghesso. "Impact of trapped charge and interface defects on the degradation of the optical and electrical characteristics in NPD/Alq_3 OLEDs", IEEE Transactions on Electron Devices, Vol. 57, N^o. 1, January 2010

N. Wrachien, A. Cester, **A. Pinato**, M. Meneghini, A. Tazzoli, G. Meneghesso,J. Kovacb, J. Jakabovicb, D. Donovalb, "Charge Trapping in Organic Thin Film Transistors", HeTech'08, 17^{th} European Workshop on heterostructure Technology, 2008

N. Wrachien, A. Cester, **A. Pinato**, M. Meneghini, G. Meneghesso, A. Tazzoli, J. Kovac, J. Jakabovic, D. Donoval, "Threshold Voltage Instability In Organic Tft With SiO_2 And SiO_2/Parylene-Stack Dielectrics", 2009 IEEE International Reliability Physics Symposium, Montreal, Canada, April 26-30, 2009

N. Wrachien, A. Cester, **A. Pinato**, M. Meneghini, A. Tazzoli, G. Meneghesso J. Kovac, J. Jakabovic, D. Donoval, "Organic TFT with SiO_2-Parylene Gate Dielectric Stack and Optimized Pentacene Growth Temperature", 39^{th} European Solid-State device research Conference, ESSDERC 2009, Athen 14 - 18 September 2009

N. Wrachien, A. Cester, N. Bellaio, **A. Pinato**, M. Meneghini, A. Tazzoli, G. Meneghesso, K. Myny, S. Smout, J. Genoe, "Light, Bias, and Temperature Effects on Organic TFTs", 2010 IEEE International Reliability Physics Symposium, Anaheim, USA, April 26-30, 2010

Sommario

I semiconduttori organici sono alla base di un relativamente nuovo campo di ricerca, chiamato Elettronica Organica. Lo studio delle proprietá elettriche, foto-conduttive e optoelettroniche dei materiali organici, il trasporto di carica e di eccitoni, e lo studio della crescita di film sottili, ha permesso lo sviluppo di transistors, LED e celle solari basati su semiconduttori organici. Design più complessi, quali circuiti elettronici e pannelli fotovoltaici flessibili, RFID (Radio Frequency IDentification) tag sono al momento in via di sviluppo, mentre i display OLED sono considerati una delle tecnologie più promettenti per quanto riguarda i display e l'illuminazione, ed è prevista come imminente la loro diffusione nel mercato elettronico mondiale.
In questo contesto la stabilità nel tempo del semiconduttore, l'utilizzo di un incapsulamento adeguato e un sufficiente tempo di vita del dispositivo incapsulato, diventano essenziali al fine di ottenere il successo di questa tecnologia. Inoltre lo studio dei fenomeni fisici alla base del degrado delle performance dei dispositivi basati su semiconcuttore organico, rappresenta per la comunità scientifica sia una sfida, sia un'affascinante ricerca.

Nel corso degli ultimi tre anni mi sono occupato principalmente dello studio di due tipi di dispositivi organici: LED a semiconduttore organico (OLED) e transistor a semiconduttore organico (OTFT). In particolare ho lavorato in due diversi ambiti: la prima parte del mio lavoro riguarda lo studio dell'affidabilità e delle proprietà termiche di OLED, basati sull'electron transport layer (ETL) Alq3 e sull'hole transport layer (HTL) NPD. Questi studi sono stati realizzati monitorando la variazione delle caratteristiche elettriche, ottiche e termiche dei dispositivi durante test di stress accelerato. All'interno di questo lavoro abbiamo testato OLED con differente struttura interna (tipo e spessori sia degli strati organici che dei contatti), con differente dimensione e forma dell'area attiva. Entrambe temperatura e corrente sono state singolarmente utilizzate come fattori acceleranti. La realizzazione di stress di affidabilità utilizzando differenti valori di corrente di stress, ha permesso di estrapolare leggi di degrado, e conseguentemente di calcolare il tempo di vita dei dispositivi. I nostri studi su OLED fosforescenti sottoposti a stress elettrico, con differenti valori di corrente di stress, hanno mostrato un aumento della tensione operativa dei dispositivi univocamente correlato con il numero di portatori iniettato nei dispositivi durante lo stress.
Sono stati investigati meccanismi di degrado dell'elettroluminescenza di OLED basati su oligomeri. In particolare ci siamo concentrati sui fenomeni di degrado intrinseco che provocano una diminuzione della potenza ottica durante il funzionamento standard. I risultati di questa analisi forniscono informazioni sui processi

fisici responsabili del degrado degli OLED, e indicano una significativa correlazione tra la diminuzione dell'intensità luminosa dei dispositivi e la presenza di difetti e carica positiva intrappolata all'interfaccia tra Alq_3 e NPD. Inoltre abbiamo investigato la disuniforme diminuzione di potenza ottica lungo l'area attiva di OLED sottoposti a test di stress elettrico. Questo fenomeno è stato correlato all'auto-riscaldamento e al profilo superficiale di temperatura dei dispositivi. Si è ipotizzata la presenza di un effetto di current crowding al fine di spiegare la presenza delle due disuniformi distribuzioni, ottica e termica.
Uno studio approfondito è stato realizzato sulle proprietà termiche dello strato di anodo degli OLED, confrontando dispositivi realizzati con diversi ossidi trasparenti conduttivi (TCO). In particolare si sono investigate le prestazioni e l'affidabilità di OLED con ossido di Stagno-Indio (ITO) e ossido di Zinco-Indio (IZO) come contatto di anodo. I dispositivi sono stati confrontati in termini di efficienza, resistenza termica e affidabilità. I risultati di questo studio hanno dimostrato che gli OLED realizzati con anodi di IZO hanno performance confrontabili con dispositivi con anodi di ITO, e mostrano una migliore dissipazione termica e maggiore tempo di vita.

La seconda parte del mio lavoro è legata allo sviluppo tecnologico di OTFT di tipo bottom e top contact, e allo studio della loro affidabilità.
Collaborando con il centro europeo di ricerca di microelettronica *IMEC*, abbiamo prodotto innovativi top contact OTFT realizzati con fotolitografia. Utilizzando un processo di wet etching, abbiamo realizzato dispositivi di tipo top contact con lunghezza di canale di 10μm, ottenendo mobilitá maggiori di $0.5\text{cm}^2/\text{Vs}$. Inoltre abbiamo sviluppato un innovativo processo che permette il patterning fotolitografico di contatti d'Argento sopra il semiconduttore organico, utilizzando dry etching mediante plasma. Tale processo di patterning stato dimostrato sia su substrato di silicio che di pellicola. Infine abbiamo investigato l'affidabilità di transistor organici basati sul Pentacene, e l'incapsulamento di questi dispositivi con il polimero Parylene C.

Contents

List of Figures

Nomenclature

Chemicals

$a-Si$ Amorphous Silicon, page 5

Ag Silver, page 59

Al Aluminum, page 49

$Alq3$ tris(8-hydroxyquinoline)aluminium, page 4

Ar Argon, page 67

Au Gold, page 55

$C_{22}H_{14}$ Pentacene, page 10

$C60$ Buckminsterfullerene, page 8

CF_4 Carbon Tetrafluoride, page 67

Cr Chromium, page 59

Cu Copper, page 59

$CuPc$ Copper Phthalocyanine, page 4

DIW Deionized Water, page 56

GaN Gallium Nitride, page 85

HFEs Hydrofluoroethers, page 60

IPA Isopropanol, page 56

SiO_2 Silicon Dioxide, page 55

ITO Indium Tin Oxide, page 44

IZO Indium Zinc Oxide, page 44

LiF Lithium Fluoride, page 49

$MoOx$ Molibdenum Oxide, page 69

NMP N-Methyl-2-pyrrolidone, page 81

NPD N,N´-Di-[(1-naphthyl)-N,N´-diphenyl]-1, 1´-biphenyl)-4, 4´-diamine, page 21

O_2 Oxygen, page 67

O_3 Ozone, page 89

OTS Octadecyl Trichloro Silane, page 89

$P\alpha MS$ poly(alpha-methyl styrene), page 89

Pd Palladium, page 57

PEN Polyethylene naphthalate, page 72

PES Polyethersulfone, page 57

PGMEA 2-[1-methoxy]propyl acetate, page 80

PVP Poly-vinyl-pyrrolidone, page 72

Si Silicon, page 5

ZnO Zinc Oxide, page 48

ZnS Zinc Sulfide, page 69

Other Symbols

ε_0 Vacuum dielectric constant, page 9

ε_{ins} Relative dielectric constant, page 9

C_{ins} Capacitance per unit area, page 9

I_{ds} Drain-source current, page 9

LEP Light Emission profile, page 24

R_{th} Junction Thermal Resistance, page 43

T_j Junction Temperature, page 43

$\text{TTF}_{70\%}$ 70% time to failure , page 53

V_{ds} Drain-source voltage, page 78

V_{gs} Gate-source voltage, page 78

Acronyms

AFM Atomic Force Microscopy, page 49

AMdisplay Active Matrix display, page 6

BL Blocking Layer, page 49

CCD Charge-Coupled Device, page 17

CVD Chemical Vapour Deposition, page 55

EML EMissive Layer, page 49

ETL Electron Transport Layer, page 4

FOLED Flexible Organic Light Emitting Diode, page 75

HIL Hole Injection Layer, page 4

HIL Hole Injection Layer, page 49

HTL Hole Transport Layer, page 4

IC Integrated Circuit, page 5

MOSFET Metal Oxide Field Effect Transistor, page 9

OMBD Organic Molecular Beam Deposition, page 5

OTFTs Organic Thin Film Transistors, page 5

OVPD Organic Vapour Phase Deposition, page 2

PhOLED Phosphorescent Organic Light Emitting Diode, page 13

RF Radio Frequency, page 67

RFID Radio Frequency IDentification, page 6

RMS Roughness Measurement System, page 49

SAM Self Assembled Monolayer, page 89

TCO Transparent Conductive Oxide, page 49

TFT Thin Film Transistor, page 5

UV Ultra Violet, page 61

VDP Vapour Deposition Polymerisation, page 77

Chapter 1

General Introduction

In 1976 the Alan MacDiarmid sowed the seed of a revolutionary technology by proving the first conducting *polymer* [1]. Thanks to this discovery, he was invested with the Nobel prize for chemistry. Years later, when the first organic transistor was built, the applied physics tried to investigate the utility of these materials for a wide range of applications. The research field concerning the study of devices based on conductive polymers took the name of *Organic*[1] *Electronics*.

In this first chapter it is provided a small introduction to organic electronics and to the organic devices that are more relevant within this work, i.e. OLEDs and OTFTs.

1.1 Organic Electronics

Although crystalline silicon (Si) has been the dominating technology in the semiconductor industry over the last decades, semiconducting thin film technologies are better suited to realize some specific applications. Processing in crystalline Si technology always has to start from the high quality crystalline Si wafer, which limits the size of the application and the versatility. Semiconducting thin films on the other hand, can be deposited on such a arbitrary substrate of arbitrary size, enabling applications such as large area displays or solar cells covering complete windowpanes. Organic semiconductor technology is one of the available thin film technologies with the additional advantage that the low deposition temperatures allow the use of flexible substrates.

Since semi-conduction in organic crystals and polymers films has been proved (between the 1950s and 1970s [2, 3]), organic conjugated macromolecules and polymers have generated a large scientific interest. These materials combine the

[1]The name "organic" is an historical name,dating back to 19^{th} century, when it was believed that organic compounds could only be synthesised in living organisms through *vis vitalis*. Namely an organic compound is every member of a large class of chemical compounds whose molecules contain carbon, with exception of carbides, carbonates, carbon oxides and gases containing carbon. The dividing line between organic and inorganic is contended and historically arbitrary; generally speaking, however, organic compounds are defined as those compounds which have carbon-hydrogen bonds.

ability to conduct electronic charge, typical of semiconductors and metals, with specific plastic properties like reduced cost and mechanical flexibility. Moreover, organic materials offer several processing advantages over conventional semiconducting materials, including a reduced thermal budget and the possibility to process on the top of inexpensive substrates, such as polymers and glass. The perspective of low cost device fabrication on large, flexible substrates is clearly not achievable by using the standard inorganic semiconductor processing technology. Instead, manufacturing electronic devices on large substrates will most likely be based in printing-based techniques (e.g. screen printing, micro contact printing, ink jet printing, etc.), stamping, or low vacuum deposition methods, such as organic vapour phase deposition (OVPD). The lower processing costs entail lower cost for the finalized device. An important market for devices with massively low cost per unit could be the health one. Due to the safety requirements, single-use devices are highly desirable, without forgetting the bio-compatibility of the most of these polymers, which clearly makes them useful for specific bio-sensing applications.

Moreover, organic materials are characterized by a huge variation in structure and properties, and this adaptability is one of the principal reason for studying their application to electrical engineering problems. These remarkable materials still represent an enormous range of challenging in synthesis, and structure for chemists, such as the wide choice of their molecular structure and the possibility to incorporate side-chains or grains with specific behaviour into the bulk material or on the surface, enabling the production of films with specific physical and chemical properties [4]. Foe example many molecules and polymers have pronounced optical qualities that can be adjusted by modifications of chemical structure. Electrical properties such as conductivity are also dependent on molecular design. Thanks to this flexible, and/or optically transparent polymers and oligomers could open new scenes to electronic devices in the next future. Totally new and innovative applications can be realized by achieving sufficient device performance at considerably reduced cost. Organic solar cells is for instance one of the promising research field of organic electronics [5]. Solar cells have been investigated for a long period of time, using several inorganic materials. Although organic solar cells most likely will never be able to compete with inorganic solar cells in terms of efficiency, they actually have a few advantages compared to their inorganic counterparts. They can be produced more cheaply, such that the price per unit energy generated by the cell may turn out to be lower than that of inorganic solar cells. Then, the absorption coefficient of organic semiconductors is much larger than that of inorganic semiconductors. Moreover, organic solar cells can be reproduced on flexible substrates, which allows for the integration of solar cells on textiles. Other *organic* fields of research are related to: Organic Light emitting Diodes (OLEDs, see section 1.2), organic thin film transistors (OTFTs, see section 1.3), organic lasers, organic sensors and other innovative devices. More complex organic designs, like flexible electronic circuits, photovoltaic panels and Radio Frequency IDentification (RFID) tags are under development, while OLEDs are going to conquer the lighting and the display worldwide market.

1.2 OLEDs

Research in the optoelectronic properties of organic material has already been going on for nearly 100 years, starting with the publication of the discover of photo-conductivity in organic crystals in 1906 [6]. The first actual OLED, based on anthracene, was fabricated in 1963 (even still with extremely high operating voltage). Nevertheless, for a real breakthrough we have to wait till 1987, with the work by Tang and Van Slyke about the performance of green emitting thin film OLEDs based on the small organic molecule tris(8-hydroxy quinoline) (Alq3) [7]. In 1990, Bradley described the first polymer OLED, based on poly(p-phenylene vinylene) (PPV) [8]. It showed that was possible to spin coat a precursor polymer onto the transparent conducting indium-tin-oxide (ITO) anode substrate, thermally converting the precursor to PPV, and finally evaporating a thin Aluminium cathode layer on the PPV. Since then, the competition between small-molecule OLEDs and solution processed OLEDs continues in parallel. Improvements , also in terms of reliability, have been terrific: from devices with a lifetime in air of less than 1 minute, to green OLEDs capable to operate continuously for over 20 thousands hours at a brightness of 100 cd/m^2 [9]. Moreover, these devices can count on several potential advantages:

- Relative easy and low cost fabrication
- Opportunity to be solution processed, or evaporated on any kind of substrate
- Wide viewing angle
- Great brightness

In the last years, several multinational companies (i.e Sony, Samsung) have started to show previously passive, and subsequently active matrix displays based on OLEDs. Small OLED-based displays are already commercially available, usually in mobile applications, such as in cell phones, mp3-players, etc. Moreover, OLEDs are suitable for flexible displays not only because they have a thin, solid-state and flexible structure, but also because their wide viewing angle allows them to be viewed even when they are flexed. Other advantages of OLEDs are their wide colour gamut and quick response times, enabling full-colour smooth moving images even on flexible films. OLED technology is a promising candidate for the front plane of a high-quality flexible display and its performance can be enhanced when the OLED is driven in active-matrix (AM) operation. In 2005 Samsung presented a 40-inch OLED TV display, demonstrating the proof of principle for a large OLED display. Recently, Organic Light-Emitting Diodes have demonstrated efficiencies as high as 102 lm/W, demonstrating a path for future adoption of OLEDs as light sources [10]. Therefore, another market segment in which OLEDs could come into play, is ambient lighting. OLEDs provide a technology for large area diffuse light sources, while leaving the freedom to design panels in any kind of shape [11]. Whereas OLED displays consist of an array of small red, blue and green pixels, OLED lighting applications require an

homogeneous, pleasant white light, i.e. a required colour rendering index of at least 80. In addition, lighting requires high brightnesses (roughly 1000 cd/m^2, as compared to 100 cd/m^2 for display applications), and OLED lighting panels need to be highly efficient. The luminous efficacy should be preferably larger than 50 lm/W. Therefore, it is clear that OLED lighting imposes different and more demanding requirements than OLED displays. One of the most critical part is nowadays the emitter used for the blue part of the spectrum, especially in terms of operational lifetime.

In the next paragraph we report the state of art of intrinsic degradation in Alq3-based OLEDs. An extensive study of this relevant topic is then reported in chapter 3.1.

1.2.1 Intrinsic degradation on Alq3-based OLEDs

Since the report on the first efficient OLED by Tang and Van Slyke in 1987 [7], tris(8-hydroxyquinoline)aluminium (Alq3) has been one of the most widely adopted emitter material in OLED technology. Alq3 can be used for the realization of devices emitting in the green-red spectral region. The degradation of OLEDs during operation time can be strongly determined by the worsening of the properties of Alq3 layer. In fact, Alq3-based OLEDs can be affected by several failure mechanisms, such as the formation of dark spots [12, 13], catastrophic failures [14], and long-term intrinsic degradation that is responsible for the OLED brightness decrease over time, without any visible deterioration of the active area. Over the last decade, the first two issues have been overcome, by both using improved sealing techniques and depositing organic materials with high purity degree. On the other hand, intrinsic degradation still remains an open issue, which is worth of investigation, even though several hypotheses on the origins of this kind of degradation have been already proposed. For a long time the morphological instability of the Hole Transport Layer (HTL) has been depicted as one of the main mechanism responsible for OLED degradation [15, 16]. This resulted into the research of hole transport materials with high glass transition temperatures (T_G) [17, 18]. These studies led to the synthesis of several important OLED materials. Although it has been demonstrated that the use of HTLs with high T_G increases the device robustness to high temperature environments, it does not impact its operational stability, especially at room temperature [19, 20]. Furthermore, OLED stability has been chased by different methods, such as the introduction of a Copper Phthalocyanine (CuPc) buffer layer between the ITO and the Hole Injection Layer (HIL), and the doping of the HTL. Nevertheless, the argued reasons behind the success of these technological solutions were often incomplete and sometimes contradictory. In particular, the key issue concerned the localization of the degradation processes, in the HTL or in the Electron Transport Layer (ETL). A turning point was set by Aziz that observed that in Alq3 significant photo-luminescence decrease is observed during holes injection, while the photo-luminescence stays almost constant during electrons injection [21]. These results, therefore, provided strong evidence that injection of holes into the Alq3 layers can be responsible for the optical degradation of OLEDs. The enhanced stability of OLEDs developed inserting a mixed layer at the HTL-Alq3 interface,

confirmed this hypothesis, suggesting that OLEDs degradation mainly takes place at or close to that interface. Furthermore, the long-term luminance decrease has been related to the instability of the Alq3 cationic species [22] and to the accumulation of positive charge at the emitting OLED interface [23, 24]. The instability of the cationic species induces the creation of by-products that have been related to a decrease in device electro luminescence. Moreover, it has been shown that these by-products play different roles as charge traps, electron-holes recombination centres and fluorescence quenchers. However, holes injection into the Alq3 layer still appears to be one of the main factors responsible for OLED optical degradation. This hypothesis is confirmed by the fact that cyclic voltammetry on Alq3 in solutions showed the irreversibility of the Alq3 oxidation process [25].

1.3 OTFTs

For more than two decades now, organic thin-film transistors (OTFTs) based on conjugated polymers, oligomers, or other molecules have been studied as a possible alternative to more traditional, mainstream thin-film transistors (TFTs) technology, based on inorganic materials. Traditional crystalline Silicon (Si) field-effect transistors are the leader technology in semiconductor industry. Nevertheless, there are application where crystalline Si is not the best option. Crystalline wafer limits the substrate size and the versatility, being a rigid base. On the contrary thin-film semiconductors do not come in wafers, but they can be deposited on arbitrary sized substrates. Although Crystalline Si performance and cost per transistor cannot be achieved by thin-film based devices, by using this technology unique products can be manufactured. The most established thin film technology is Amorphous Si (a-Si). Another emerging thin-film technology is the one related to metal oxide semiconductors. These materials showed high mobilities (up to 100 $cm^2/(Vs)$, versus 1 $cm^2/(Vs)$ for a-Si), low temperature deposition (availability of flexible substrates) and optical transparency.

Organic semiconductor technology is clearly another competitor of thin-film technologies. Integrated circuits (ICs) fabricated using organic TFTs (OTFTs), offer the potential of enabling low-cost processing, flexible, adequately performing logic circuits (an example of microprocessor on foil is reported in fig. 1.1). As mentioned before, organic semiconductors can be processed at low temperatures, allowing deposition on different kind of substrates (Silicon, glass, polymers, textiles). An organic semiconductor layer can be grown virtually on any kind of surface if properly treated. No epitaxial growth on a crystalline substrate is required. A wide range of deposition methods can be used (OMBD, CVD, etc). Moreover, OTFTs may be solution-processed, allowing the fabrication of large-area devices. Nowadays the mobility of OTFTs and of a:Si TFTs are comparable. Nevertheless, it is foreseen that OTFTs should be patterned by printing, potentially lowering down considerably the price of this technology compared to the a:Si one [26]. Therefore, Organic thin-film transistors have been recognized as a breakthrough technology for next generation electronics due to their unique advantages, such as light-weight, flexibility, and low-cost fabrication [27, 28]. Recently it has been proved that also a:Si TFTs can be processed at around 100℃ on a flexible sub-

strate, with good off-current and mobility, and great environmental stability [29]. However, low temperature processed a:Si are affected by low bias stability due to the huge amount of unsaturated bonds that can act as traps. On the contrary organic semiconductors do not show any unsaturated bonds.

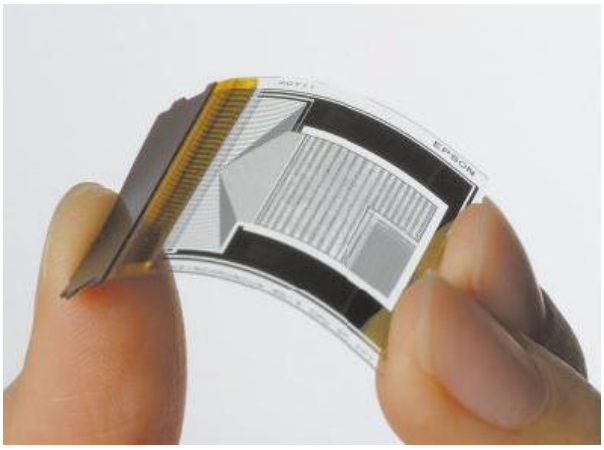


Figure 1.1: The industry's first flexible 8-bit asynchronous microprocessor by Epson.

To manufacture an organic TFT, the organic semiconductor and the other materials required (gate electrode, gate dielectric, source and drain contacts) are deposited as thin layers on the surface of an electrically insulating substrate, such as glass or plastic foil. The total thickness of the device can be less than 100 nm. Several methods exist for the deposition and patterning of the individual layers of the TFT. Gate electrodes and source and drain contacts are often prepared using inorganic metals. Non-noble metals, e.g aluminium or chromium, are suitable for the gate electrodes while noble metals, most notably gold, are a popular choice for the source and drain contacts, since they tend to provide better contact performance than other metals. The gate dielectric material must be compatible with the substrate used, and the thickness is a compromise between the desire to work at low voltage levels, and the need of a low leakage current.

Organic transistors are potentially useful for applications that require electronic functionality with low or medium complexity distributed over large areas on unconventional substrates, i.e. applications in which the use of silicon devices and circuits is technically or economically not feasible. Potential applications include postage stamps [30, 31], radio frequency identification (RFID) tags [32], "smart" cards [4, 33, 34]. OTFTs can be processed on plastic films (like PEN or Parylene) achieving field-effect mobility higher than 0.1 cm^2/Vs and a current on/off ratio greater than 10^5. This means that they can be used in an Active-Matrix (AM) display allowing the production of thin, flexible displays [35, 36, 37]. The entry of these products in the worldwide market is imminent (see in Fig. 1.2 and 1.3, some *Sony* prototypes of flexible AM-OLED display). Strategies for increasing the performance of organic TFTs include further improvements in the carrier mobility of the organic semiconductor by synthesizing new materials, improving purification and enhancing the molecular order in the semiconductor layer [38], and scaling of the organic transistor dimensions.

Figure 1.2: Sony full-color top-emission QQVGA AM-OLED display.

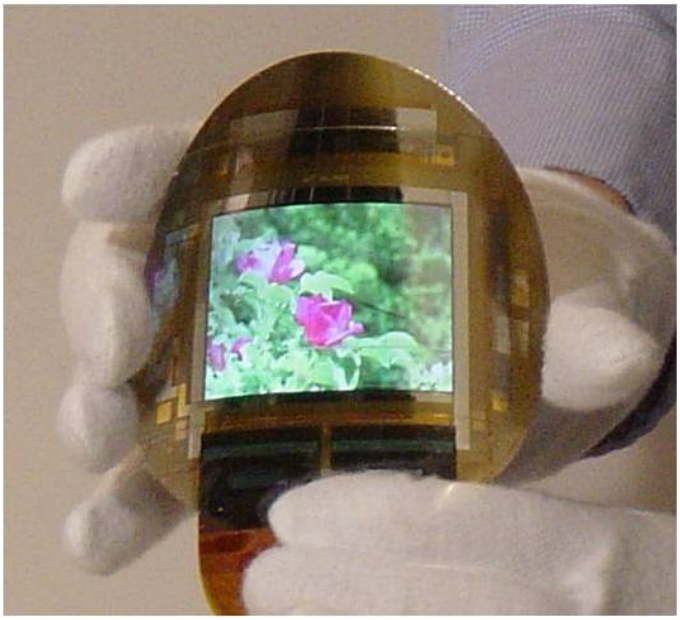


Figure 1.3: Sony OTFT-OLED display operating with bending condition.

1.3.1 A bit of history

The first organic TFT with the small molecule Pentacene as organic semiconductor, was first reported in 1992 [39]. In 1995, an OTFT was fabricated by using the n-type semiconductor *Buckminsterfullerene* (C60), resulting in an electron field-effect mobility of almost 0.1 $cm^2/(\mathrm{Vs})$ [40]. In the same year, the Philips group published the worldwide first results of an organic integrated circuits [41]. For the first time, OTFTs were sufficiently good performing to construct logic gates that displayed voltage amplification. Moreover the fabrication of a ring oscillator demonstrated that these logic gates could switch subsequent gates and perform logic operations. This breakthrough delineated the start of a new era in the field of organic electronics, as it became clear that OTFTs might provide a useful technology for certain applications, accepting a relatively low performance, but at the same time requiring low cost. Since 1992 we have observed a constant increase in mobility, which was achieved either by improving the processes used for the fabrication of the transistors and by synthesizing new organic materials. In 1999, Pentacene OTFT were fabricated with a field-effect mobility in excess of $2cm^2/(\mathrm{Vs})$ [42]. In terms of mobility, OTFTs became more performing than amorphous silicon TFTs. In order to obtain these high mobility values, the morphology of the Pentacene film was optimized by applying surface treatments. Thanks to the efforts of many research groups working in the field of organic electronics, the OTFT performance steadily increased. In 2003, the 3M research group showed that a Pentacene OTFT mobility in excess of $5cm^2/\mathrm{Vs}$ could be systematically fabricated [32]. Even so, the success of OTFTs is still not guaranteed. Potential obstacles are yield, lifetime, and insufficiently fast progress in low-cost production technologies (printing and solution processed OTFTs). In addition, other thin film technologies like Silicon, polysilicon, chalcogenide, Zinc Oxide (ZnO), and carbon nanotubes have progressed concerning the mobility as well as low deposition temperatures.

1.3.2 Basic Operation

Traditional Si transistors operate by exploiting the inversion of the channel. By increasing the gate-source voltage the channel is depleted and consequently a layer of minority carriers is formed. In this regime the transistor is on and applying a voltage between drain and source it is possible to have a current flow. On the contrary, if we increase the gate-source voltage in the other direction we get the creation of an accumulation layer with majority carriers, and applying a voltage between drain and source we have no current flow due to the double reverse biased pn junctions. Instead an organic transistor usually operates in accumulation. By increasing in the proper way the gate-source voltage, we get the creation of an accumulation layer that allows the flow of holes (in a p-OTFT) between the electrodes, if subjected to a voltage bias. If the gate voltage is increased in the other direction, the organic semiconductor gets depleted and can create an inversion layer. Nevertheless the flowing current is limited because most of organic semiconductors transports only one kind of carrier. In order to limit the parasitic currents , the thickness of the semiconductor is usually kept

small (30 to 50nm). Despite that, OTFTs can be modelled by using the inorganic typical transistor equations [43]. Two curves are usually measured to characterize a field-effect transistor: the transfer characteristics and the output characteristics.

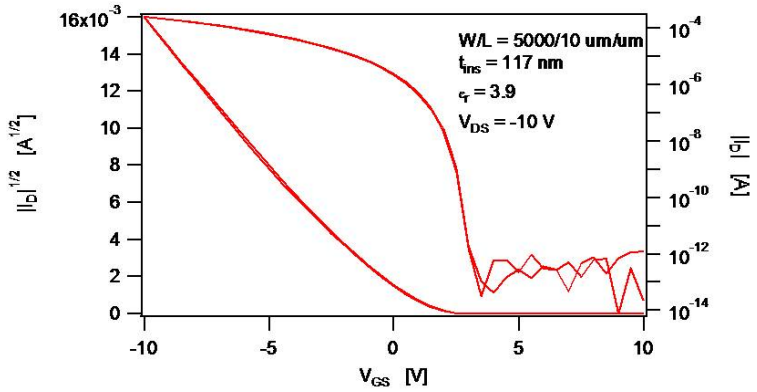


Figure 1.4: OTFT transfer characteristic in the linear regime.

In order to measure the transfer characteristic, the drain-source voltage is kept constant, while we have a variation of the gate-source voltage. Depending on the drain-source voltage, the transistor is operating in the linear or in the saturation regime. Fig. 1.4 shows the transfer characteristics of a p-type organic transistor, measured in the saturation regime.

Assuming the conventional gradual channel approximation, the current I_{ds} measured between drain and source in the saturation and linear regime can be described as following:

$$I_{ds} = -\frac{W}{2L}\mu C_{ins}(V_{gs} - V_t)^2, \qquad |V_{ds}| > |V_{gs} - V_t| \qquad (1.3.1)$$

$$I_{ds} = -\frac{W}{L}\mu C_{ins}(V_{gs} - V_t - \frac{V_{ds}}{2})V_{ds}, \qquad |V_{ds}| < |V_{gs} - V_t| \qquad (1.3.2)$$

where W is the channel width, L the channel length, μ the mobility, C_{ins} is the capacitance of the gate dielectric per unit area

$$C_{ins} = \frac{\varepsilon_0 \varepsilon_{ins}}{t_{ins}} \qquad (1.3.3)$$

where ε_0 is the vacuum dielectric constant, ε_{ins} is the relative dielectric constant, and t_{ins} is the thickness of the dielectric. Finally, V_t is the threshold voltage. For silicon MOSFETs, the threshold voltage V_t is defined as the minimum gate-source voltage required to induce strong inversion. As over mentioned, organic TFTs do not operate in inversion mode, so actually it should not be possible to define a threshold voltage. Nevertheless, the threshold voltage concept is useful for organic TFTs, since it represents the minimum gate-source voltage required to obtain appreciable drain current, and because it marks the transition between the different regions of operation.

Equations 1.3.1, 1.3.2 clearly state that is possible to extrapolate the mobility

of the OTFT from the I_{ds} vs. V_{gs} characteristic. In particular it follows that the mobility μ is proportional to I_{ds} in linear regime and to its square root $I_{ds}^{1/2}$ in saturation regime. The two mobilities can slightly differ, we have decide to work with the one calculated in saturation regime because it is less affected by parasitic currents. Two other parameters are usually consider to evaluate the performance of an organic transistor: one is the onset voltage V_{on}, defined as the gate-source voltage at which I_d increases abruptly (see figure: 1.4), and the inverse of the sub-threshold slope S^{-1}, that is the voltage step needed to gain one decade in current at V_{on}. The sub-threshold slope depends on the gate dielectric capacitance and on the trap states at the interface [44].

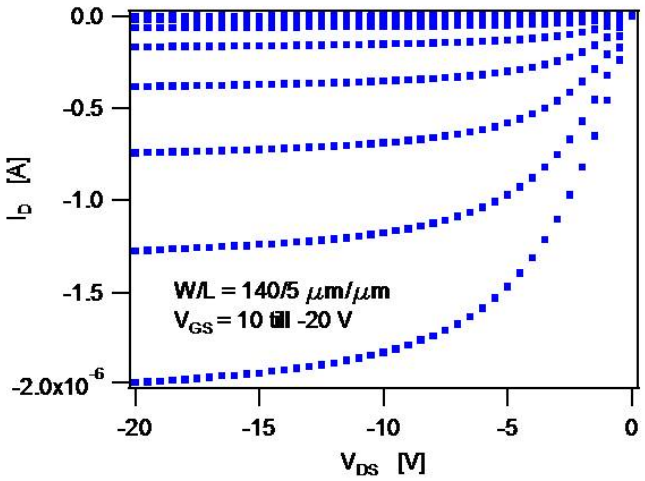


Figure 1.5: OTFT output characteristic.

An output characteristic is obtained by measuring the current I_{ds} varying the drain-source voltage for different gate voltage levels (see Fig. 1.5). Here we can distinguish two regimes, the linear one, where I_{ds} is linearly proportional to V_{ds}, and the saturation one, where I_{ds} should be almost independent of V_{ds}.

1.3.3 Pentacene

All the OTFTs that we have manufactured within this work, used *Pentacene* as organic semiconductor. For this reason we have considered appropriate to dedicate a subsection to this organic material.

Although a substantial number of small-molecule semiconductors have emerged, Pentacene consistently provides the largest carrier mobilities, due to its favorable crystal structure. This organic material is constituted by five linearly-fused benzene rings ($C_{22}H_{14}$) and it has the appearance of a dark-blue powder (its structure is shown in figure 1.6). Being a small molecule, Pentacene can be deposited by evaporation in ultrahigh-vacuum (around 10^{-8} torr in our system) with a technique called Organic Molecular Beam Deposition (OMBD). The Pentacene is heated in a Knudsen cell until it sublimates (usually around 200℃). The molecules evaporate inside a chamber where the sample is usually anchored upside down (see App. C for more details). The growth of the Pentacene layer is

highly influenced by the temperature of the cell and of the substrate. Pentacene can also be deposited using an OVPD system. In this case the molecules of the material are transported by a carrier gas at low vacuum.

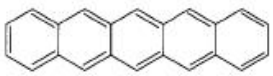


Figure 1.6: Structure of a molecule of Pentacene ($C_{22}H_{14}$).

In the following I will provide some details about the Pentacene growth relying on Stijn Verlaak's PhD thesis about the growth of small-molecule organic semiconductors [45, 46]. During the semiconductor deposition from a gas phase, Pentacene molecules hit the substrate and start to accumulate at the surface. When several molecules aggregate, a *nucleus* is formed. This nucleation process can be modelled thermodynamically. Simulations reveal that due to the increasing number of aggregated molecules, the nuclei start to growth determining the start of the Pentacene thin-film growth. Depending on the growth condition, two-dimensional or three-dimensional nuclei can be formed. These two different growths are, electronically speaking, very different. Three-dimensional nuclei form ill-connected, isolated grains while two-dimensional growth, on the contrary, leads to the formation of a continuous film. The growth on one regime, or the other one, is determined by the deposition rate and the substrate temperature. Obviously, also the kind of substrate plays a role on the morphology of the film. Chemically treating the substrate, i.e with self-assembled monolayers, it is possible to tune the surface energy of the substrate (for more details see App. B). Prior to the real deposition, vacuum sublimation and/or absorption chromatography are used to purify Pentacene. The grade of purity of the material has a tremendous impact on the mobility of the finalized devices. As previously mentioned, with this organic semiconductor it is possible to obtain OTFTs with mobilities up to 5 cm^2/Vs [47]. One of the drawbacks of using this material, it is the fact that it quickly degrades in presence of oxygen and light. An unstable transistor can be characterized by a shift of the transfer curves towards more positive or negative voltages. This voltage shift can be influenced by an extended applied bias, illumination or other environmental conditions. For this reason, all the organic devices, manufactured using Pentacene as a semiconductor, need an effective encapsulation (a specific study about this topic is provided in chapter 6).

Chapter 2

OLEDs optical investigation

For studying optoelectronic devices it is interesting not only to investigate the amount of light generated by the device, but also the distribution of this emitted light along the active area. Such a study can give many information about the device, like the current distribution, heat distribution, presence of defects, hot spots, etc. Often during the ageing, the device modifies its light emission distribution, and the investigation of this variation can help in understanding the physical mechanisms behind the degradation of the optical and electrical characteristics. The light emission distribution of an OLED along its active area, can be measured by using an emission microscope[1]. In this chapter we present two optical studies that we have carried out on phosphorescent OLEDs, and on solution-processed OLEDs.

2.1 PHOLED size and shape impact on light emission

In the following we present an optical analysis that we have carried out on phosphorescent OLEDs (PhOLEDs), with different size and shape. In particular, we measured devices with $5mm^2$, $1mm^2$, and $0.01mm^2$ active area with square and circular shape. All the different devices have been biased with equal current density in order to correctly compare their light emission profiles, i.e. the distribution of the light emission intensity all along the active area. We have arbitrary decided to bias the devices at two different current density levels: $1mA/cm^2$ and $40mA/cm^2$. In this study we have used an Hamamatsu emission microscope, and its parameters have been set in order to maximize the CCD acquisition range. We have used microscopic lenses with different magnifications and the light emission profiles have been normalized to their maximum.

The Light Emission Profiles (LEP) have been analysed by using false colours

[1] An emission microscope is a microscope furnished with a CCD camera that *counts* the photons emitted by the focused device, providing a number that is proportional to the light emitted. By keeping unchanged the measurement positions and parameters, it is possible to follow the optical degradation of a device over time.

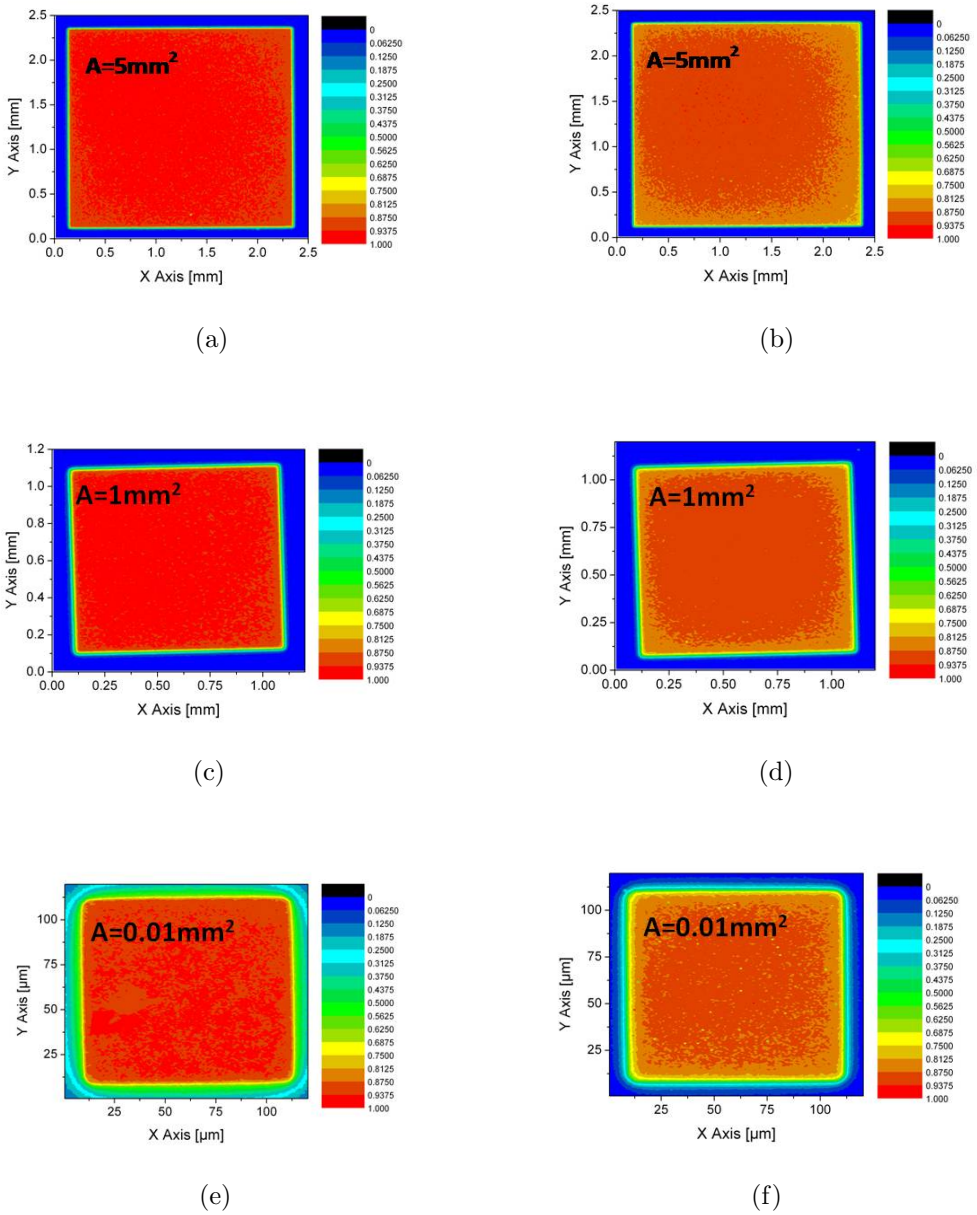


Figure 2.1: Light emission profiles of squared PhOLEDs with different size, measured at 1mA/cm² and 40mA/cm²: (a) square 5mm² at 1mA/cm², (b) square 5mm² at 40mA/cm², (c) square 1mm² at 1mA/cm², (d) square 1mm² at 40mA/cm², (e) square 0.01mm² at 1mA/cm², (f) square 0.01mm² at 40mA/cm²

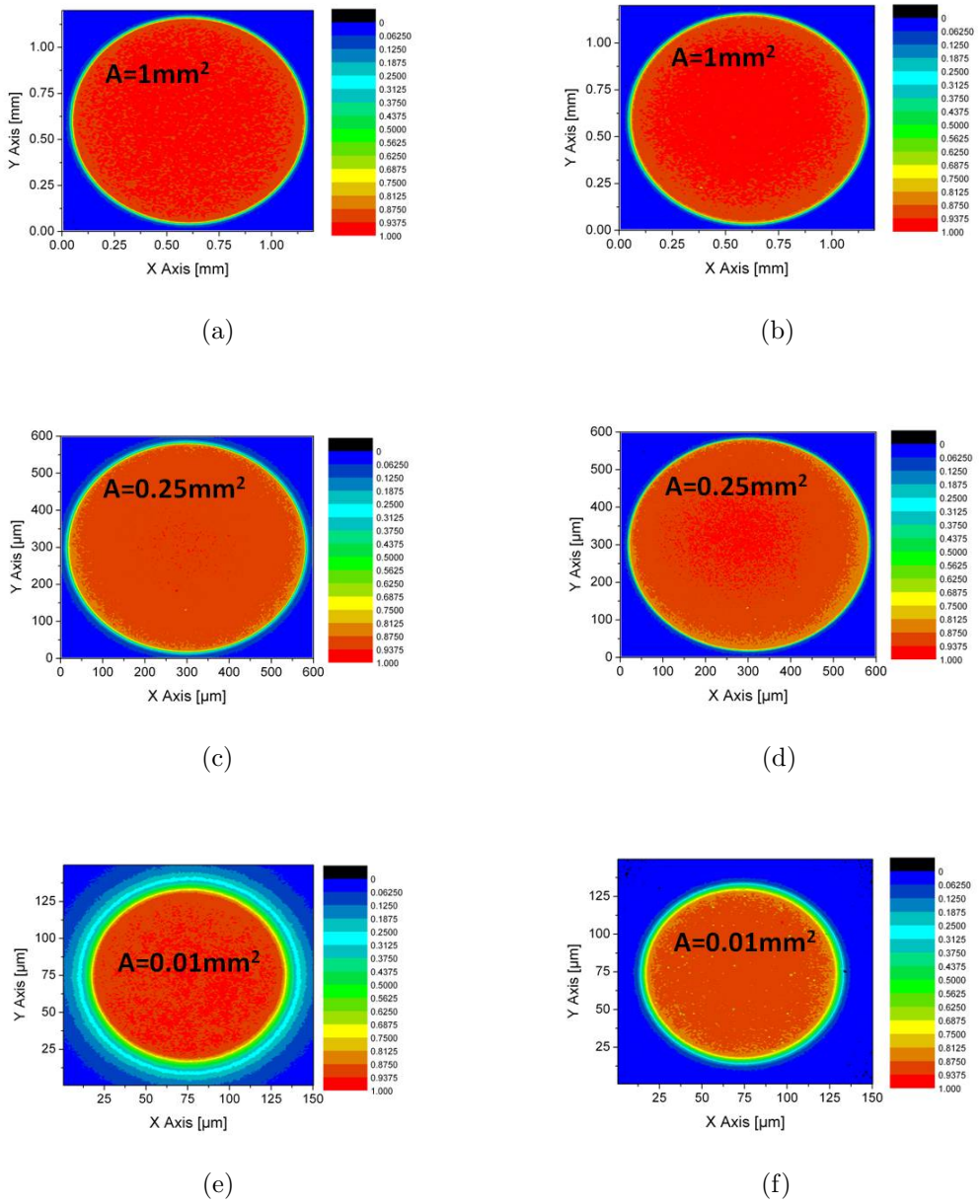


Figure 2.2: Light emission profiles of circular PhOLEDs with different size, measured at 1mA/cm² and 40mA/cm²: (a) circular 1mm² at 1mA/cm², (b) circular 1mm² at 40mA/cm², (c) circular 0.25mm² at 1mA/cm², (d) circular 0.25mm² at 40mA/cm², (e) circular 0.01mm² at 1mA/cm², (f) circular 0.01mm² at 40mA/cm²

maps, normalized to the maximum intensity along the active area. As clearly shown in the LEPs shown in Fig. 2.1 and Fig. 2.2, light emission is quite concentrated in the centre of the active areas. The phenomenon is more pronounced at high current density (40mA/cm^2). The effect seems to be independent of the size of the device area, being present both in the small, medium and large area devices. Reducing the area, it is not possible to obtain a fully uniform emission pattern. As previously mentioned the light is concentrated more in the centre of the device, therefore at the corners of the squared structures we can observe a lower intensity of the light emitted (see Fig. 2.1). Nevertheless, even observing the circular devices reported in Fig. 2.2, we notice a border effect that is probably related to a crowding current effect. Such an effect will be further investigated in chapter 4 where it will be related with the surface thermal distribution of the devices. Finally, we have tried to compare the integrated optical power of a square device with a circular one on equal area, in order to understand if a structure could be more efficient than the other one in terms of total optical power. The experiment has been repeated at different bias current levels. The results are reported in Fig. 2.3, that shows that there is no significant difference in the total light emitted by the two different devices.

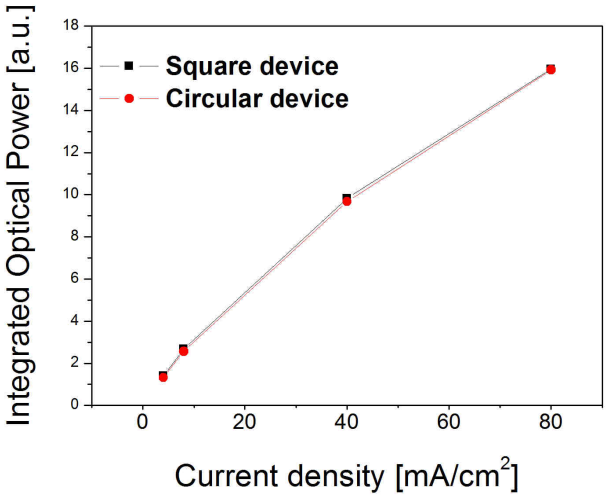


Figure 2.3: Integrated optical power of a circular and a square device of equal area (1mm^2), measured at different current density levels.

2.2 Light emission distribution of solution processed OLEDs

In the following, we report an investigation on the optical properties of solution processed OLEDs. We have performed emission profile and spectral measurements for analysing the optical uniformity of the devices. As in the study presented in the previous section, the emission profiles have been measured by using an *Hamamatsu Phemos* emission microscope. The devices have been biased by

means of a Keithley current source. The $2mm^2$ devices have biased with a current of $60\mu A$. The emission profiles reported in the figures below have been normalized to their maximum, in order to better describe the range of light intensity variation at devices surface. Measured emission profiles are shown in the following figures (Fig. 2.4 and Fig. 2.5) for a set of 7 devices.

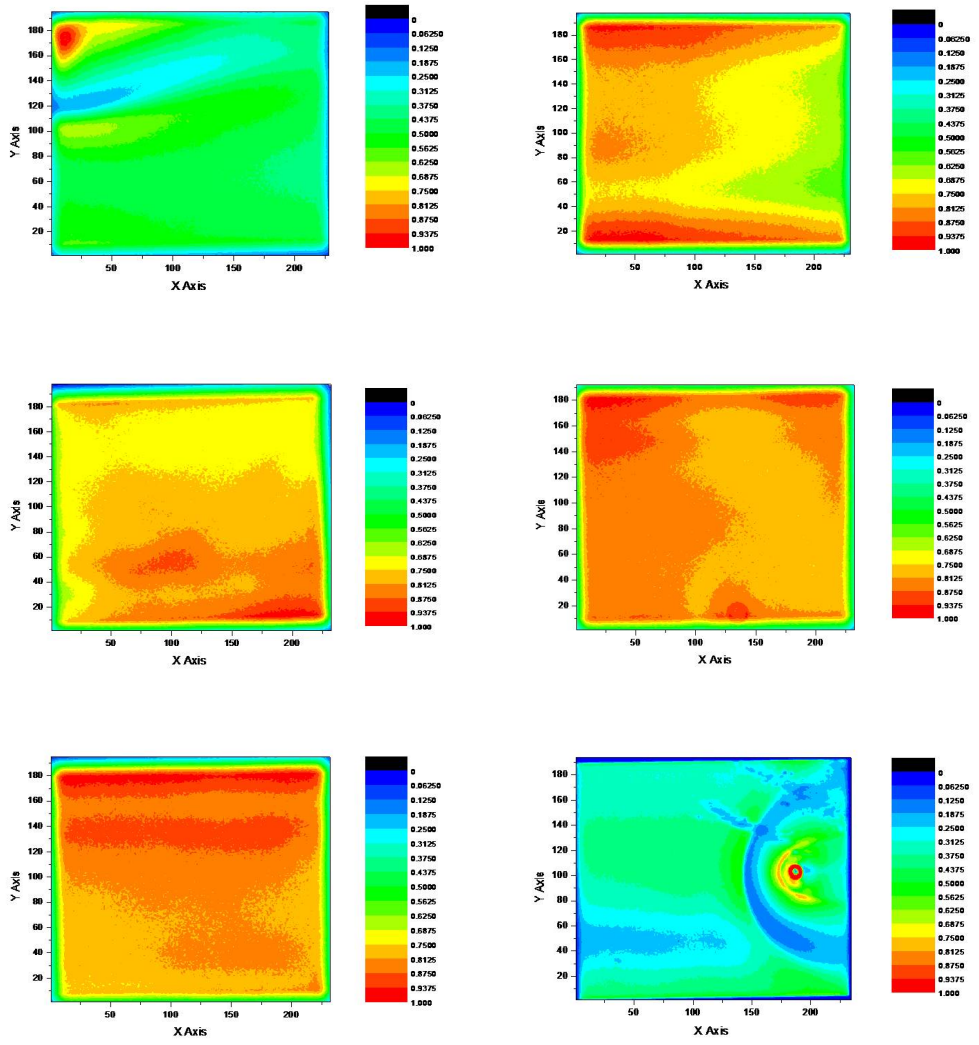
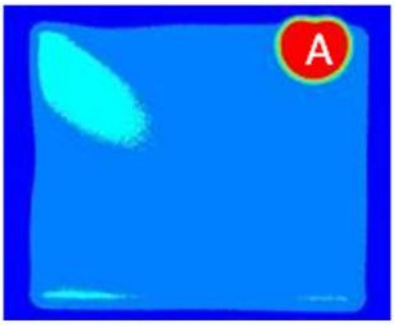


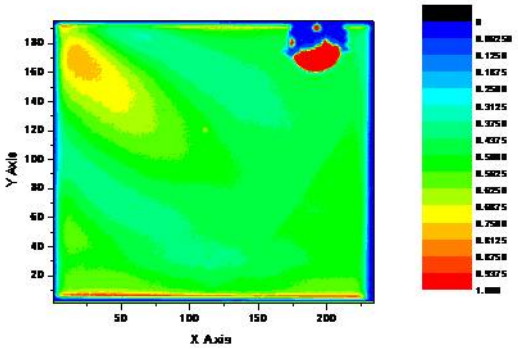
Figure 2.4: Light emission profiles of solution processed OLEDs biased at 1mA.

For devices reported in Fig. 2.5 the bias current level has been adjusted in order not to saturate the CCD[2] of the microscope. This device showed a non-uniform emission pattern, with a spot-like emission behaviour (region A in Fig. 2.5(a)). After the electro-optical characterization we have noticed that the emission pattern in region A has changed (see Fig. 2.5(b)). This effect has been attributed to the presence of some material, accumulated between the anode and the coating that seems the result of a combustion process (shown by using a stereoscopic microscope in Fig. 2.6).

[2]CCD stands for Charge-Coupled Device.



(a)



(b)

Figure 2.5: Light emission distribution measured before (a) and after (b) electro-optical characterization.

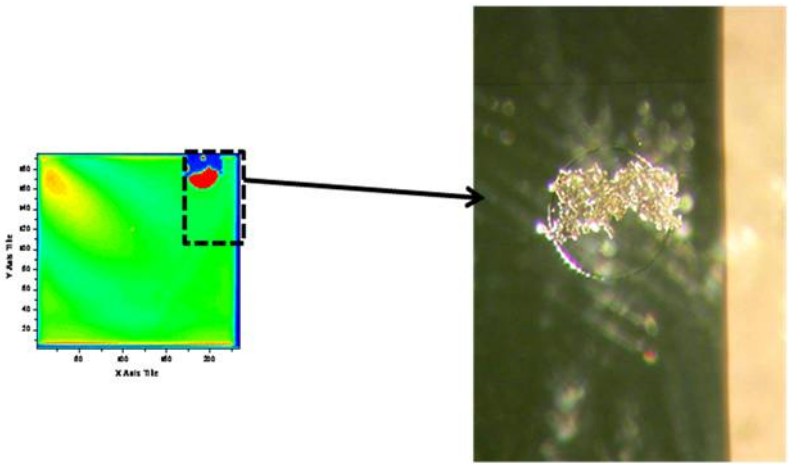


Figure 2.6: Stereoscopic microscope picture of impurities formed upon device.

Using an *Ocean Optics USB 4000* spectrometer we have measured the emission spectra of this solution processed OLEDs. The light emission has been normalized to the peak value in order to allow the comparison of the spectra shape of the different devices. We did not detect any dependence of the spectral shape on the injected current level (see Fig. 2.7). For this reason, we have arbitrary compared the behaviour of the different OLEDs carrying out spectra measurements at 1mA (see Fig. 2.8). All the devices showed nearly the same spectral shape. In particular, not even the spectrum of device with uneven light emission distribution, previously shown in Fig. 2.5, has shown any significant difference from other devices.

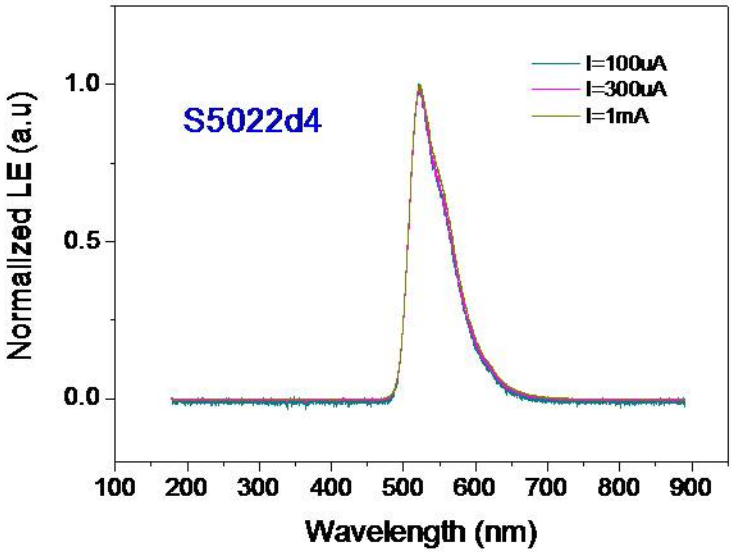


Figure 2.7: OLED Emission spectrum at different current levels.

In order to further investigate possible relation between luminescence unevenness and spectrum emission, we have measured local emission spectra by integrating our spectrometer with a microscope. In this way we were able to obtain small focused portion of the active area. The emission spectra collected in 9 different regions are reported in Fig. 2.9 and 2.10. We have normalized the light emission spectra to their peak values in order to detect possible variations of spectral shape among the nine zones of the active area. Nevertheless, no significant variation has been detected between the different regions.

Therefore, the solution processed OLEDs that we have tested showed uneven emission distribution all along the active area, especially if compared with the evaporated OLEDs showed in the previous section. This fact suggests that the unevenness of the emission profile does not correspond to modification in the spectral characteristics, but it is correlated only to differences in current/emission distribution, reasonably related to technological defects.

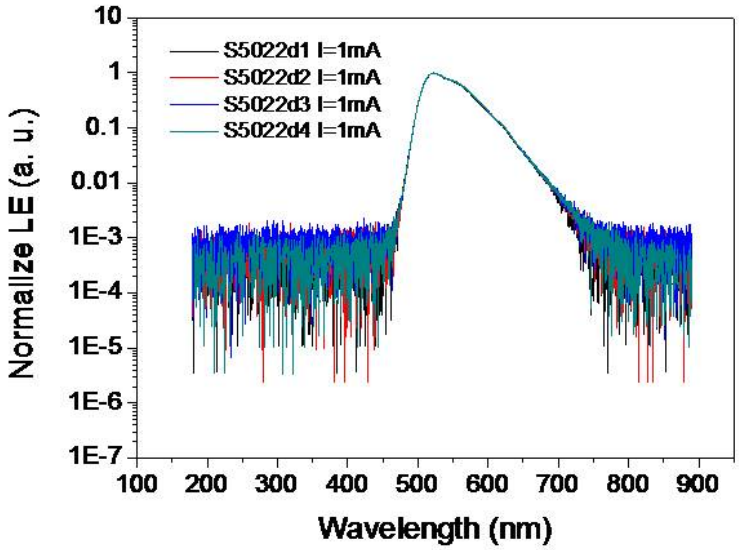


Figure 2.8: OLED emission spectra of different devices.

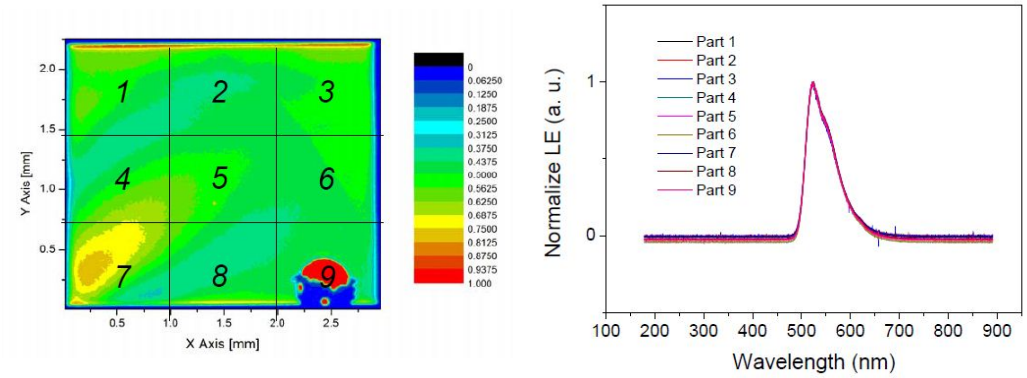


Figure 2.9: Emission spectra measured in 9 different parts of the active area.

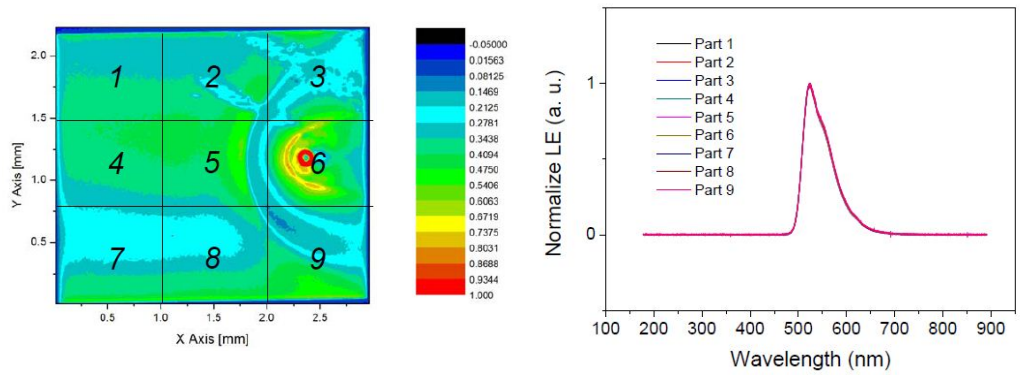


Figure 2.10: Emission spectra measured in 9 different parts of the active area.

Chapter 3

Reliability stress tests on Alq3/NPD OLEDs

In this chapter, first we present a study about the investigation of the reliability of small molecules OLEDs, with simplified structures, consisting of NPD as hole transport layer, and Alq3 as electron transport layer. The results of this analysis provide information on the physical processes responsible for OLED degradation. Secondly, we focused on a reliability study that we have performed on phosphorescent OLEDs stressed at different current levels. The variation of the electrical and optical characteristics of these devices have been monitored in order to study the degradation effects, and extrapolate a time to failure law.

3.1 Optical and electrical degradation of NPD/Alq3 OLEDs

As previous mentioned, OLEDs have attracted much attention for their large potential in flat panel display application. In this context lifetime of OLEDs is a critical parameter in order to fulfil market standards. OLEDs luminance reduction over time has been deeply investigated [48, 49, 50, 51] and driving strategies and new materials have been developed in order to solve this criticality in OLEDs spread [52, 53, 54]. In the following we present our study on the electro-luminescence degradation mechanism in NPD/Alq3 based (a resume of the state of the art of this relevant topic has been reported in chapter 1.2.1). Moreover, we focused on intrinsic degradation phenomena that determine the decrease in the optical power of OLEDs during standard operation. The study was carried out on simplified OLED structures, by means of combined optical and electrical characterization techniques. Our investigations were carried out on simplified undoped OLED structures, because such devices allow an easy interpretation of the impedance measurements. The approach we followed here, favours simplicity in studying the degradation mechanisms of the organic materials interface, over exactness in determining the real device lifetime, which is not our primary goal. In fact, the degradation kinetic highlights a quite fast degradation (with a strong

reduction after 1000-hour stress), which is not unexpected, but it is due to the simple OLEDs structure.

In this work we have tested OLEDs with NPD as HTL and Alq3 as ETL and as Emitting Layer (EML). The device structure is reported in Fig. 3.1. The analysis was performed on devices with different thicknesses for the HTL and ETL layers (as summarized in Fig. 3.2), with the aim of understanding whether the thickness of the different layers could influence the OLED reliability. Samples were prepared on commercial Glass-ITO substrates, which consisted of a 20nm SiO_2 barrier layer between the soda lime glass and 120nm thick ITO. All organic layers were deposited under high-vacuum conditions (1x10^{-7} Torr) and the devices were transferred directly from vacuum into an inert environment glove-box, where they were encapsulated using a UV-curable epoxy, and a glass lid with a moisture getter. A 10nm thick HIL is deposited between the HTL and the ITO, in order to improve the hole injection rate from the anode during the forward bias condition. The cathode consisted of Aluminum deposited on Lithium Fluoride and the active areas were defined by an insulating grid. The OLED emission profiles were assumed to be Lambertian, and the luminance was measured with a Si-photodiode mounted on an integrating optical sphere.

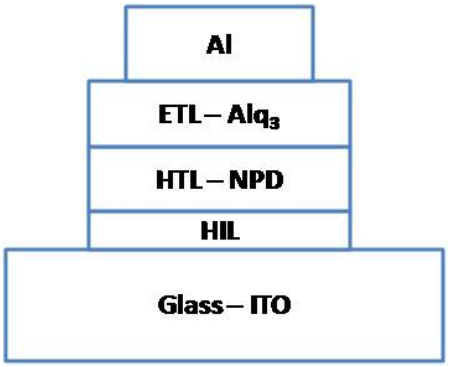


Figure 3.1: Cross section of the device structure employed in this study.

Anode	HIL	HTL	ETL	Cathode
120nm	10nm	NPD [100nm]	Alq3 [60nm]	Al [100nm]
120nm	10nm	NPD [60nm]	Alq3 [60nm]	Al [100nm]
120nm	10nm	NPD [40nm]	Alq3 [60nm]	Al [100nm]
120nm	10nm	NPD [60nm]	Alq3 [100nm]	Al [100nm]
120nm	10nm	NPD [60nm]	Alq3 [80nm]	Al [100nm]
120nm	10nm	NPD [60nm]	Alq3 [40nm]	Al [100nm]

Figure 3.2: Table with the layers thicknesses of OLEDs studied within this work.

The devices were fully electrically and optically characterized. In particular, we periodically carried out Current density vs Voltage (J-V), Capacitance vs Voltage (C-V), and Luminance vs. Current density (L-J) measurements during

ageing time. We also used an *Hamamatsu Phemos* light emission microscope to measure the luminance profile all over the device active area. The devices subjected to this characterization and reliability study have an active area of $2mm^2$.

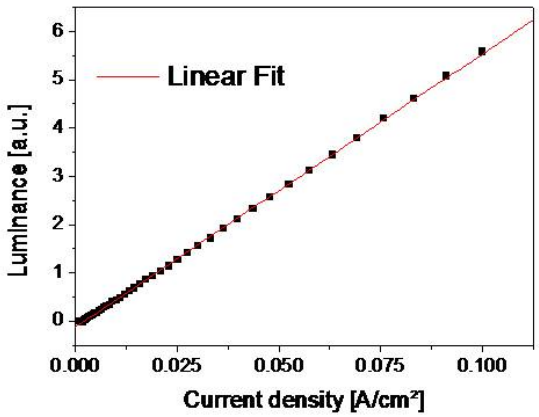


Figure 3.3: Luminance of OLED plotted as a function of bias current density.

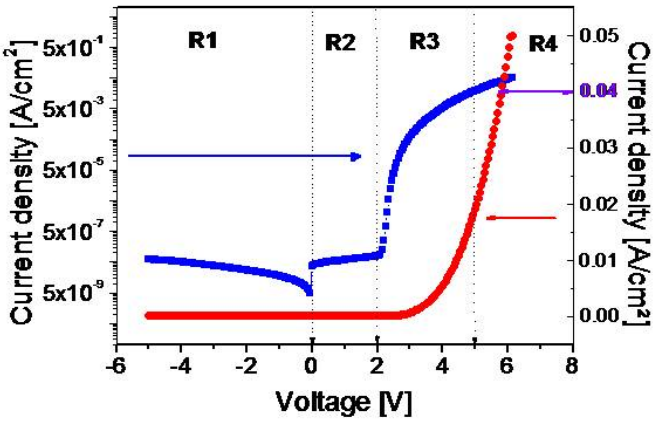


Figure 3.4: OLED Current density (log scale in the left, linear scale in the right) vs. voltage.

Fig. 3.3 shows the luminance as a function of the current density (L-J) for a typical OLED with the structure above described. The curve shows quite a linear relation between optical power and the injected current density. Fig. 3.4 shows the J-V typical curve taken on a device with 100nm Alq3 and 60nm NPD layers, plotted in semi-logarithmic scale. In order to simplify the following discussion, we arbitrary distinguish four regions on the basis of current dependence on applied voltage (V*):

Region 1: The reverse bias region V*< $0V$

Region 2: The low-forward bias regions V*> 0V and V*< $2V$

Region 3: The exponential forward region (namely, 2 <V*< $5V$), where the current exponentially increases with voltage

Region 4: The linear forward region (namely V*> $5V$), where the current linearly increases with the anode voltage

The horizontal marker in Fig. 3.4 defines the operative current of our OLEDs, i.e. 40mA/cm^2. In the following, we will arbitrarily refer to V_{ON} as the anode voltage needed to achieve such current density level. All the devices were stressed at a constant current density of 120mA/cm^2, i.e. three times larger than the nominal current density. We chose such a current in order to achieve a reasonable acceleration of the life tests, avoiding the formation of parasitic leakage paths across the organic films, and the consequent device breakdown. During the electrical stress the devices were kept at room temperature. The accelerated electrical stress was periodically interrupted in order to perform the characterization of the devices (L-I, J-V, and C-V).

After the initial characterization, we have selected a number of samples with average performances for the subsequent ageing tests. In Fig. 3.5 we plot the L-J curves taken in an OLED before stress (fresh) and during stress at different stress times. A good linear relation exists between the luminance and the current density both before and after stress at a current of 120mA/cm^2, but the slope monotonically decreases as the stress time increases, indicating a reduction of the OLED efficiency. It is worth noticing that the percentage of optical power degradation is independent of the measuring current level. After a 1000-hours stress, the luminance of the device reduces down to 55% of its initial value. In such accelerated working conditions, the test structures considered within this work have shown an extrapolated 50% time to failure of about 1270 hours. No catastrophic failures or formation of dark spots have been detected, which indicates the exclusion of external factors (such as the interaction with particles, moisture, and oxygen) in the optical degradation mechanisms. A quantitative description of the reduction in device efficiency is given in Fig. 3.6, where we plotted the optical power degradation as a function of the stress time, for all the analysed devices. Noticeably, all the devices listed in the table of Fig. 3.2, showed similar degradation kinetics suggesting that the degradation rate is nearly independent on the NPD and Alq3 layer thicknesses. For this reason, in the following we discuss only the data obtained on the samples with a 100nm NPD layer and 60nm Alq3 layer, representative for all the sets of analysed OLEDs. As shown in Fig. 3.6, the optical power decreased down to the 55% of its initial value after 1000 hours of stress at 120mA/cm^2. The entity of luminance degradation was found to be independent of the measuring current level.

The analysis of the light emission profiles (LEP), measured by using a PHEMOS Emission Microscope, provides further information on the degradation process. Fig. 3.7(a) reports a false colour maps of the light emission profile of a fresh device, driven at the nominal current density of 40mA/cm^2. The emission scale has been normalized to the maximum detected on the scanned area. Before stress, the emission intensity is slightly concentrated at the centre of the device area. In fact the edges have a 10% lower luminance compared to the centre of

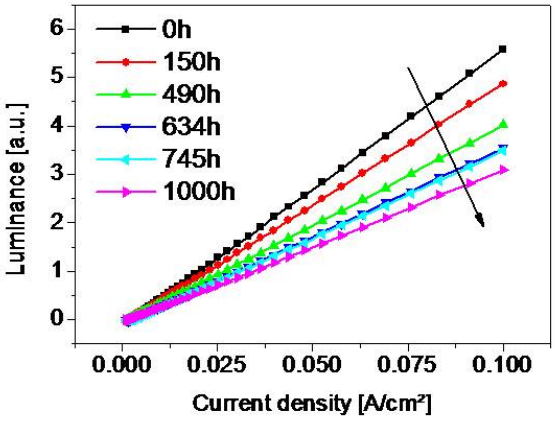


Figure 3.5: Normalized Luminance of OLED under stress, plotted as a function of current density at different stress times (accelerated electrical stress at 120mA/cm).

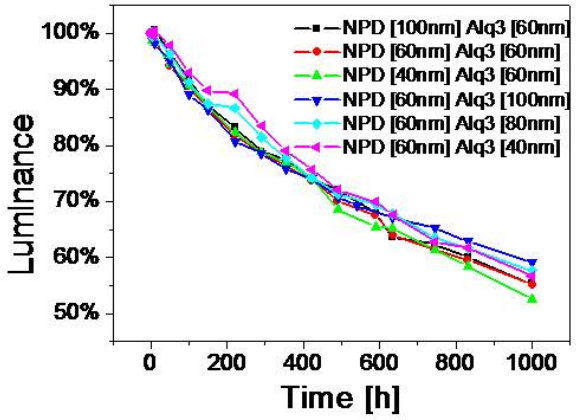
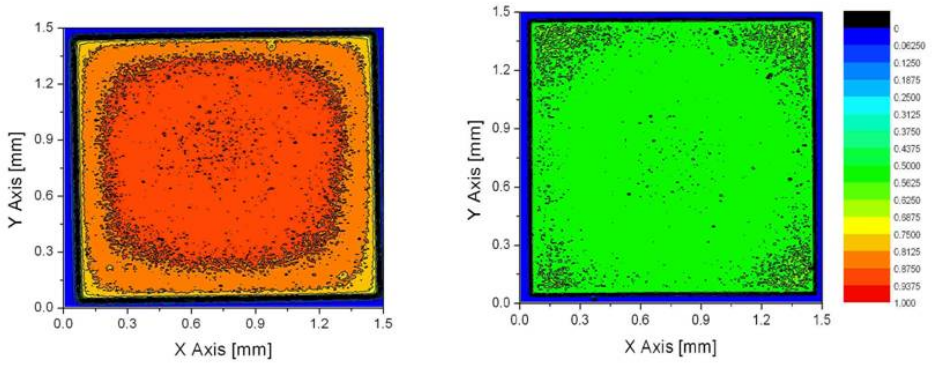


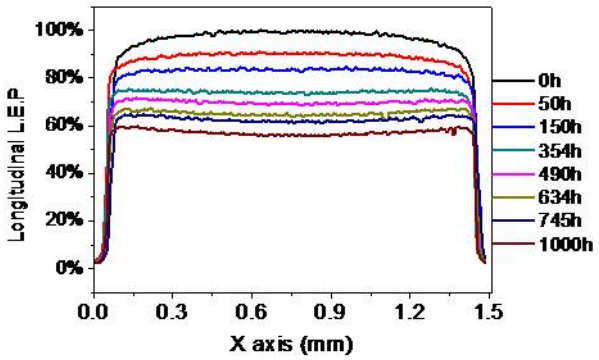
Figure 3.6: Optical degradation kinetics of OLEDs with different structural parameters, monitored at 100 mA/cm. Electrical aging has been carried out at 120mA/cm.

the active area. This result suggests that the devices show some current and emission crowding that should be correlated with a stronger self-heating near the centre of the emitting area. This hypothesis is in agreement with what discussed in chapter 2.1 and with the OLED thermal behaviour that will be described in chapter 4.2. Fig.3.7(b) shows how the spatial distribution of the emitted light is modified after the accelerated electrical stress of the device: the measurements have been normalized as in Fig. 3.7(a), so that they provide a direct indication of the intensity decrease at each point on device area. We can notice an emission decrease along the entire active area of about 45%, and this is in agreement with the luminance decrease shown in Fig. 3.6. In order to achieve more quantitative information on the degradation of the light emission profiles, we have analysed the intensity profiles on the median lines of the devices (longitudinal intensity profiles), reported in Fig. 3.7(c). During stress time the emission intensity becomes lower, but more uniformly distributed on device active area. Noticeably,

the intensity decrease is more pronounced in the centre of the OLED area, with respect to the border region. This idea is consistent with the fact that the current density is higher at the centre of the devices and therefore can explain the stronger degradation.



(a) (b)



(c)

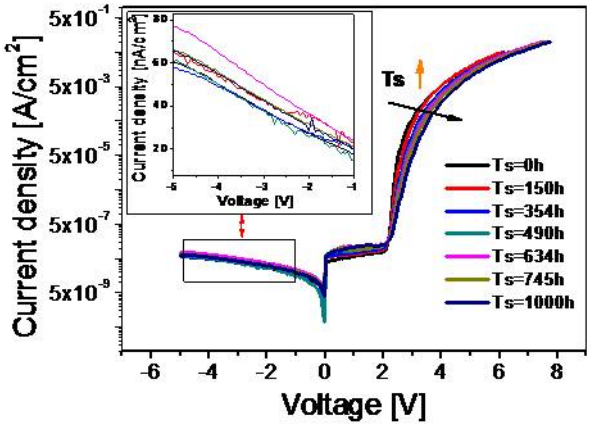
Figure 3.7: Light Emission profile of an OLED biased at 40mA/cm^2 before (a) and after (b) 1000h of stress at 120mA/cm^2. c) Longitudinal light emission profile of an OLED biased at 40mA/cm^2, measured during the accelerated electrical stress at 120mA/cm^2 for different stress time.

The J-V characteristics of the OLEDs are shown in Figs. 3.8(a) and 3.8(b) in semi-logarithmic and linear current scale, respectively. The J-V characteristics of Fig. 3.8(a), in the reverse bias region (down to -5V), represents an almost linear dependence (shown in the inset in Fig. 3.8(a)). The linear relation between current and voltage suggests that this current is due to different contributions, such as the drift of the intrinsic carriers [55], the surface conduction at device borders, and the parasitic current contribution of our equipment. The leakage current increases during stress if a weak forward bias is applied (Region 2 in Fig. 3.8(a)). Applying a positive voltage, we observe that the rapid increase in the current starts at a voltage of about 2V, which corresponds to the estimated work function difference between the ITO and the Al-LiF. This value is in agreement

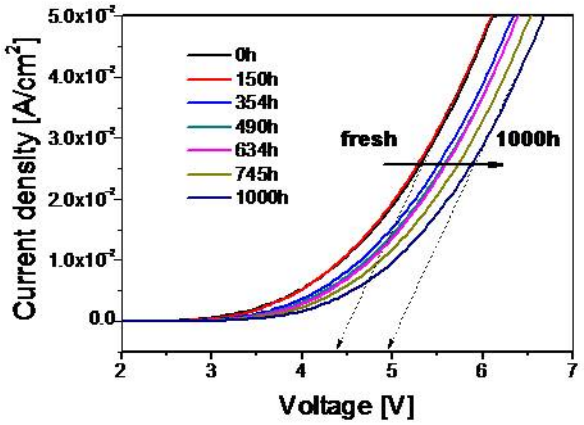
with those reported in literature [56]. If we consider the current above 2V, i.e. in the Region 3, we observe a progressive decrease in the slope in the semi-logarithmic scale during stress time (Fig.3.8(a)). This change suggests the build up of a negative trapped charge at the interface. This trapped charge tends to reduce the electric field across the ETL, but at the same time it tends to increase the electric field across the HTL. In order to explain the J-V slope decrease during stress, we must assume that the quantity of negative charge rises as the gate voltage increases. This occurs if defects are pushed below the quasi-Fermi level, capturing one electron, as the anode voltage is increased. In the linear forward region, the behaviour of the OLED is mainly influenced by the series resistance of the device, resulting in a linear relation between voltage and current for high bias conditions. Interestingly, the slope of the J-V characteristics in this region does not strongly change during stress, suggesting that the series resistances of the ETL and HTL layers remain nearly constant during the ageing. Moreover, stress induces a significant rigid shift of the linear J-V curves towards higher voltage levels (Region 4 in Fig. 3.8(b)), corresponding to an increase in the operating voltage (V_{ON}) of the devices. In Fig. 3.8(c) we show the increase in the OLED operating voltage V_{ON}. This result supports the idea that the degradation of the electrical characteristics is dominated by an intrinsic degradation at the interface between NPD and Alq3. The inter facial degradation mechanism is also supported by the fact that different thicknesses of NPD and Alq3 do not affect the OLEDs lifetime.

In order to achieve a more comprehensive picture of the degradation process, during stress we have carried out capacitance vs voltage (C-V) measurements at two different frequencies, namely 300Hz and 10kHz. C-V measurements have been carried out by using a HP 4284A precision LCR meter in a 4 cables configuration. The system has been calibrated before the measurements, in order to avoid the influence of the cables in the impedance measurement. A sinusoidal ac signal of 50mV amplitude has been superimposed to the dc bias. The evolution of the C-V curves during stress is shown in Fig. 3.9(a) and Fig. 3.9(b), respectively. Remarkably, during the electrical stress, the C-V curves shift rightward and the transition region of the C-V curves is progressively more stretched as the stress time increases. We quantify the shift of the C-V by measuring the position of the inflex point as conventionally done in literature [23, 56]. The results are summarized in Fig. 3.9(c) as a function of the stress time, and they highlight a linear relation between the C-V shift and the stress time. Furthermore, we repeated the C-V measurement for the 1000-hours stressed device after a 3-month storage (see Fig. 3.9(a)). The results show that negligible variation occurred, suggesting that most of the charge trapping derives from irreversible phenomena. Finally in Fig. 3.10, by performing a double sweep C-V, we show that a very small hysteresis (as large as 50mV in fresh device and 100mV after 1000-hour stress) appears in the devices under test.

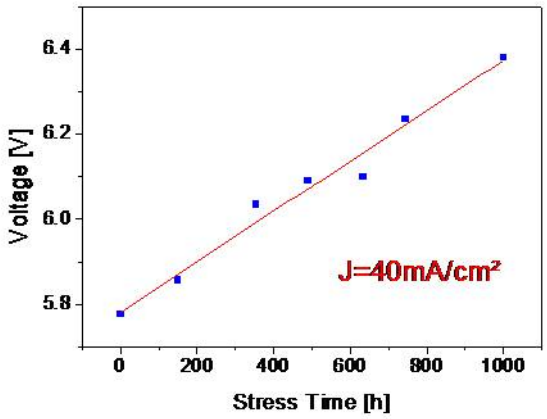
Electrical aging of OLEDs generates defects near the HTL/ETL interface, which are likely responsible for the luminance decrease during electrical stress. In order to ascertain the nature of the NPD/Alq3 interface defects, we performed and analyzed the evolution of the C-V curves during the accelerated electrical stress. At this purpose, we have adopted the model described by Kondakov [23].



(a)

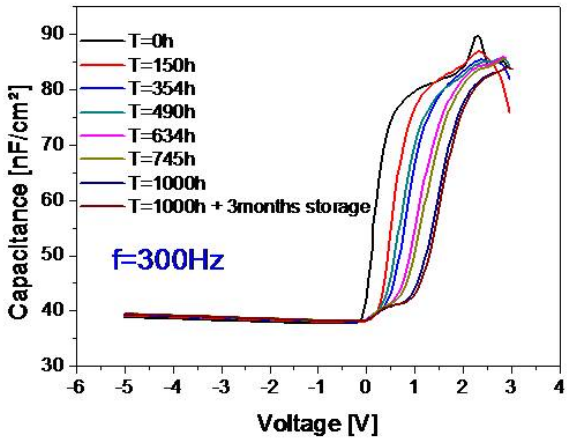


(b)

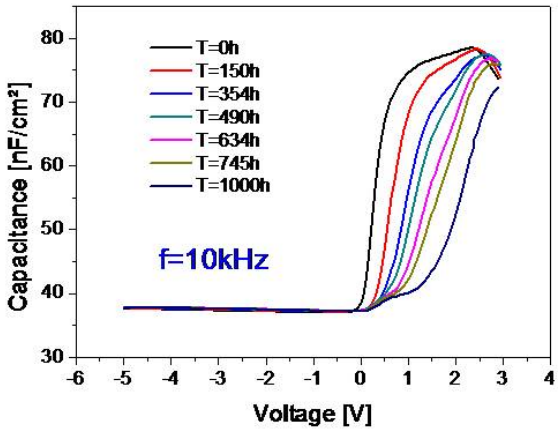


(c)

Figure 3.8: (a) Current density (log scale) vs voltage, measured at different stress time (T_s). (b) Current density (log scale) vs voltage variation during constant current stress at 120mA/cm^2. (c) Evolution of V_{ON} during constant current stress, and its linear fitting.



(a)



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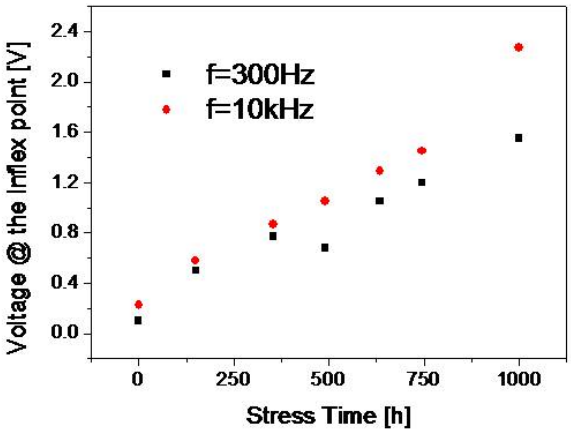


(c)

Figure 3.9: Capacitance vs. voltage at different stress levels, measured at a frequency of 300Hz (a) and 10kHz (b). (c) Voltage at the inflex point as a function of the stress time.

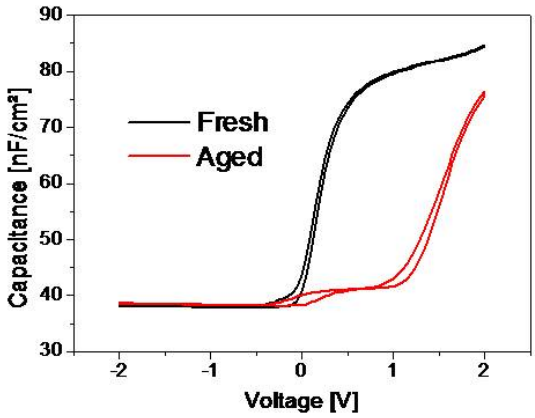


Figure 3.10: Capacitance vs. voltage, measured at a frequency of 300Hz, before and after the stress. As shown the hysteresis is negligible in the fresh device as well as after 1000 hours of stress.

First of all, we have to consider the band model of the OLED qualitatively depicted in Fig. 3.11. The cathode work function (in our case LiF-Al) is close to the LUMO level of the Alq3, allowing for a good electron injection in the ETL. Still the employment of a HIL guarantees a good hole injection in the HTL. In first approximation, ITO does not allow injection of minority electrons during reverse bias, the same is for aluminum respect to holes. Kondakovs model also assumes that the interface between HTL and ETL blocks holes in the HTL and electrons in the ETL. In reverse voltage condition there are no carriers inside the device, and two equal amounts of charges with opposite polarities are stored in the cathode and in the anode. The total capacitance measured in this region is given by the series of the three dielectrics (HIL, HTL and ETL). If then we move from 0V to positively bias voltage values (Figs. 3.11 (b) and (c)), the capacitance increases due to the onset of the hole injection from the anode. Since the hole injection is more efficient than electron injection, a higher electric field is generated across the ETL than across the HTL. This difference in electric field is maintained by a net positive charge at the HTL/ETL interface. Under high hole injection conditions, the capacitance of the HIL and HTL is screened, and the resulting capacitance is equal to that of the Alq3 layer. In our devices, the capacitance transition occurs almost at 0V (see Fig. 3.9(a)), which is not the same voltage at which the conduction starts (approximately 2V in Fig. 3.9(a)). This is because the C-V transition is correlated to the formation of a mobile hole charge sheet at the Alq3/NPD interface, due to the different carrier injection efficiency from the cathode and the anode. Instead, the OLED current is determined at a larger degree by the electron injection rather than hole injection. We can tentatively explain what occurs during the constant current stress with the aid of Fig. 3.11 (d) and (f). It has been reported in literature that accelerated electrical stress produces positive charge at the Alq3/NPD interface [24]. This charge is likely responsible for the rightward shift of the C-V curves in Fig 3.9(c). In fact, the positive charge trapping decreases the electric field across the NPD layer, and it opposes to the hole injection from the anode. This is schematically depicted in Fig. 3.11 (d), where the dashed lines represents the band structure before stress

and the solid line are the bands after stress. Hence, a higher voltage is needed to produce the same electric field across the NPD layer, and the consequent capacitance transition. The evolution of the J-V curves in Fig. 3.8(a) is apparently in contrast to this interpretation. In fact, because the OLED current is determined at a larger degree by the electron injection, we should expect a leftward shift of the J-V curves, due to the increase of the electric field across the ETL. This is not observed either at low positive voltage (around 2V), where the current is only marginally modified by the stress, or at higher electric field, where V_{ON} behaves even oppositely (see Fig. 3.8(c)). We have already discussed that the increase in V_{ON} cannot be only ascribed to an increase in the series resistance, because OLED with different thicknesses, feature quantitatively the same behavior during stress. In fact, if some appreciable change of the series resistance occurred, we would expect to observe a much larger increase of V_{ON} in those devices with greater layer thicknesses, which has not been observed. The J-V behavior can be tentatively explained by assuming that the constant current stress produces both a fixed interface trapped charge and a number of neutral interface states, as schematically depicted in Fig. 3.11 (d). These states may come from the oxidation of the Alq3, as previously reported [22], and they should act as electron interface traps, which captured an electron as soon as its energy level moves below the Fermi level. As soon as the voltage increases, more and more defects are pushed below the quasi-Fermi level at the NPD/Alq3 interface; if we assume that, each time a defect goes below the Fermi level, it captures an electron or, equivalently, it releases a hole, the increase in the anode voltage, translates in a progressive increase in the net negative charge, which compensates the initial positive fixed charge. This is confirmed by Kondakov et al. [57], who shows the formation of weakly emission deep electron traps in the vicinity of the interface between the hole and electron transport layers.

Following this interpretation, at moderately low voltage, i.e. when only the hole injection should be appreciable, the contribution of the positive charge is dominating because the majority of the defects are empty, being located above the Fermi level. Therefore the C-V curves are expected to shift rightward, due to the reduction of the hole injection rate at the anode interface. On the other hand, electron injection should be easier thanks to the positive charge (see Fig. 3.11 (e)). In principle this should increase the OLED current in that voltage range. Unfortunately, in that voltage range the OLED current is dominated by parasitic leakages and transient trapping/detrapping contributions. If we consider the current above 2V, the contribution of the neutral defects becomes comparable to that of positive charge. In fact, for voltage around 2V, there is a moderate shift of the J-V curve. When the bias voltage exceeds 2V the contribution of the neutral defects become dominant (Fig. 3.11 (f)) and the rightward shift of the J-V curves becomes larger and larger as the anode voltage increases. As soon as the electric field across the ETL is high enough, an appreciable electron conduction begins, the device enters the linear region, the band bending of the NPD becomes negligible (see for instance [58]), and the quasi-Fermi level at the Alq3/NPD interface is pinned to that of the NPD layer. In this way, the interface trapped charge reaches its maximum value and the J-V curves remain parallel to each other. The fact that V_{ON} increases during stress, suggests that the contribution of the electron interface traps is dominant at high electric field (Fig. 3.11 (f)), with respect to

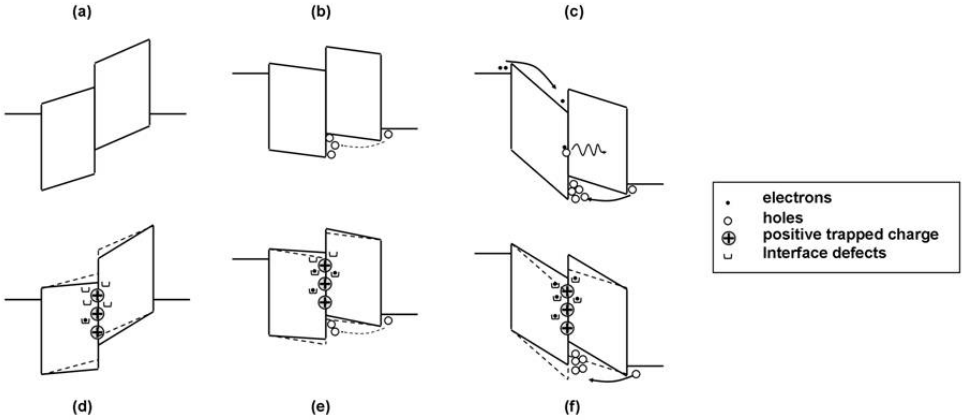


Figure 3.11: Qualitative and simplified band diagram model of the OLED structure considered in this work (not to scale). (a), (b), and (c) refer to the qualitative band positions of a fresh OLED. For sake of simplicity we neglected any charge trapped in the fresh device before stress, and we omitted the hole injection layer between ITO and NPD. (d), (e), and (f) represent the modification of the band structure induced by the stress. The dashed lines represent the band structure before stress, and the solid line represents the band structure after stress. The position of the trapped charges and the neutral defects is only qualitative and it must be considered concentrated very close to the organic film interfaces.

the positive fixed trapped charge. A rough estimation of the fixed trapped charge can be done by using the method proposed in [59]. Fig. 3.12 summarizes the evolution of the trapped charge from the C-V shift. A good linear relation appears as a function of the stress time.

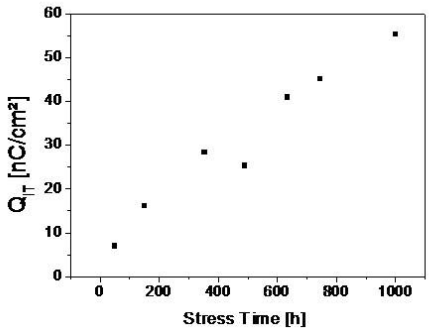


Figure 3.12: Interface charge as a function of stress time, estimated with the method proposed in [59].

3.2 Phosphorescent OLEDs submitted to accelerated stress

In this section we report a reliability study that we have performed on phosphorescent OLEDs (PhOLEDs) with NPD as HTL and Alq3 as ETL. The emission layer was Alq3 doped with Iridium-based guest. We tested devices with 2mm^2 area. For our study we have considered four devices that have been subjected to a preliminary electrical and optical characterization. Then we have carried out ageing stress using current as accelerating factor. The OLEDs have been stressed using four different current density values (40, 80, 120 and 160mA/cm^2). The degradation of the electrical and optical characteristics has been monitored during stress. In particular, the optical degradation kinetic has been analysed in order to extrapolate the Time To Failure dependence on the operating current density. The optical measurements have been realized both with a Si-photo diode, as well as with a light emission microscope. The electrical characteristics of the OLEDs have been measured by using an HP 4155A Parameter Analyser. All measurements were performed at room temperature and devices were protected from environment illumination during the measurements. After the initial electrical and optical characterization we have periodically measured the devices, in order to follow the electrical and optical degradation kinetics.

The electrical characteristics of the fresh OLEDs were reproducible and overlap each other, as shown in Fig. 3.13. The semi-log plot in Fig. 3.13 shows the current density as a function of bias voltage (J-V) for the four devices before the electrical stress. Before submitting the devices to the accelerated stress, we have verified that they had a similar electrical behaviour, as well as a similar optical behaviour. This is reported in Fig.3.14 where we have plotted the optical power as a function of current density, and effectively the optical curves of the devices before stress are almost superimposed.

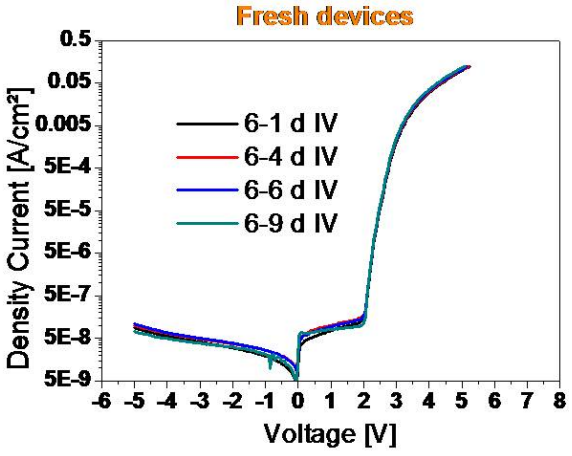


Figure 3.13: Current density vs Voltage, plotted in a semi-log scale for fresh devices.

In Fig. 3.15 it is reported the J-V curves for different stress times for each device. It is possible to notice that there is no significant increase of the reverse bias

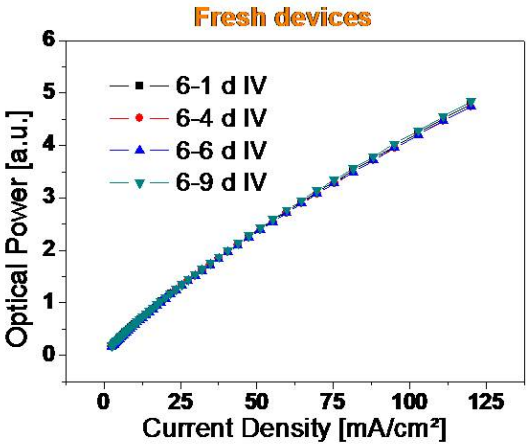


Figure 3.14: Optical power plotted as a function of current density for fresh devices.

current during stress. On the contrary, remarkable modifications of the curves occur after the turn on voltage, with the operating voltage that increases during the ageing. This increase is qualitatively shown in Fig. 3.16 for the reference current density of 40mA/cm^2.

The operative voltage increases more for higher stress currents. The faster degradation kinetics may come from two contributions: the larger number of injected carrier, which increases by increasing the stress current density; and the higher electric field across the organic films, which depends on the voltage drops across the overall stacked layers. The higher the electric field, the higher is the energy a carrier may achieve while moving across the organic semiconductor. In inorganic semiconductor device, it has generally been observed that the degradation rate increases as the average carrier energy increases. In order to separate these two contributions, we plotted in Fig. 3.17 the evolution of the operating voltage as a function of the cumulative injected charge during stress, namely (T_{stress} * J_{stress}). In this case the 4 curves are very close to each others, and only a moderate dependence on the stress current density is observed. This means that the electrical degradation rate is only marginally affected by the current density level during stress, and then, by the electric field across the organic layers.

Predictably, the degradation of the optical characteristics features the same trend than the electrical characteristics with higher optical degradation rate for higher stress current densities. In particular, looking at the device subjected to the highest stress level (stress current density of 160mA/cm^2), we can observe a loss of the 80% of the initial optical power after 290h of stress (as reported in Fig. 3.18). Moreover, as shown by the almost horizontal curves of Fig. 3.19 (which shows the optical power, measured at different stress times, normalized to the fresh condition), the degradation rate is independent of the bias current density.

During the stress, we have also monitored the change of the light emission profile of the devices. We have measured the same spatial degradation reported in the previous section. In Fig. 3.20 we have showed the initial emission profile

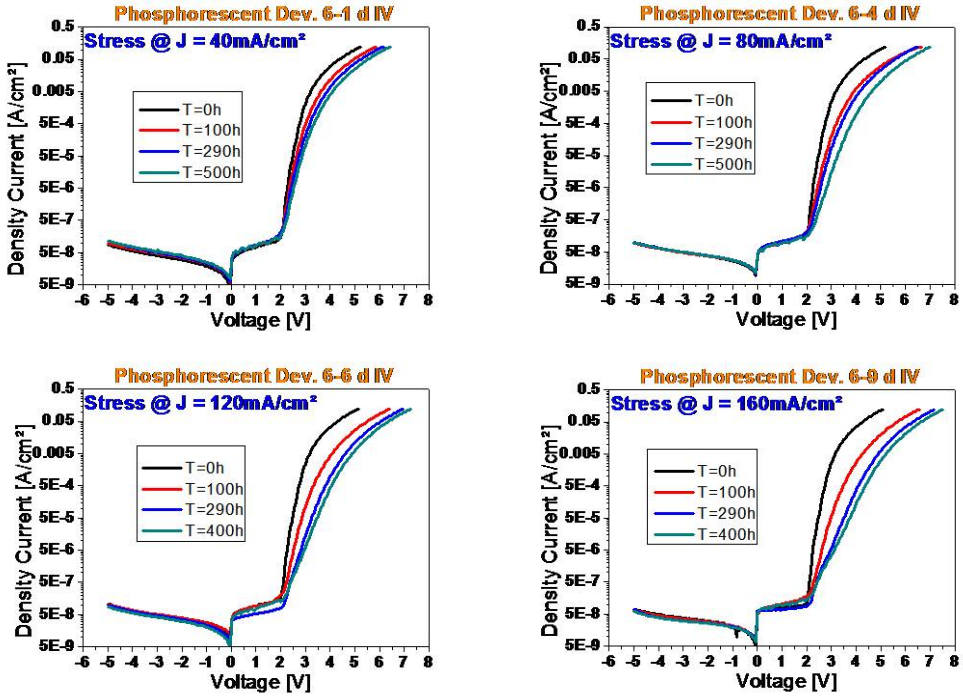


Figure 3.15: Current density vs voltage curves, plotted in a semi-log scale for the devices aged at different stress current levels.

condition, and the modified profile after 400 hours of stressed at 160mA/cm^2. The measurements have been performed biasing the device at 1mA/cm^2 and 40mA/cm^2. We have observed the typical higher degradation in the centre of the device. In particular, we have focused our attention on the evolution of the optical emission in a longitudinal line. The plot in Fig. 3.21 shows that, starting from an initial condition of almost uniform emission along the centre of the active area, after 400h of stress we reach an uneven condition where the emission at the edges is significant higher than the emission in the centre of the device (as highlighted in Fig. 3.22). This behaviour has been observed in all the devices subjected to stress, even if it is more evident when the device has lost more than 50% of its initial luminance.

In Fig. 3.23 we have reported the luminance degradation kinetics for all the devices subjected to accelerated stress, plotting their optical power in a semi-log scale as a function of stress time, and normalizing to each initial optical power. As over mentioned, the electrical degradation was solely dependent on the number of carriers injected in the OLED (see Fig. 3.17). Instead if we plot the optical degradation kinetics as a function of the cumulative injected charge $T_{stress} * J_{stress}$ (see Fig. 3.24), we can observe that the optical degradation rate remains higher for devices stressed at higher current densities. This means that the optical degradation is not dependent only by the injected charge. We can suppose that the optical degradation is affected also by the temperature reached by the device during the stress, and by the electric field across the device.

The optical degradation kinetics reported in Fig. 3.23 allows for the extrapolation of a Time To Failure law (TTF). If we consider the 70% Time To Failure

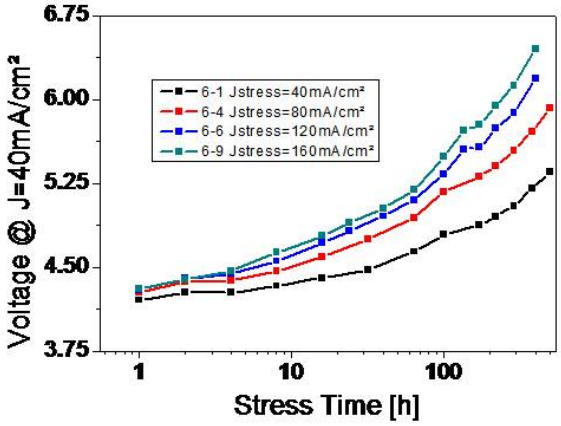


Figure 3.16: Voltage rise during stress time for the 4 devices under stress. The voltage has been measured at a current density of 40mA/cm².

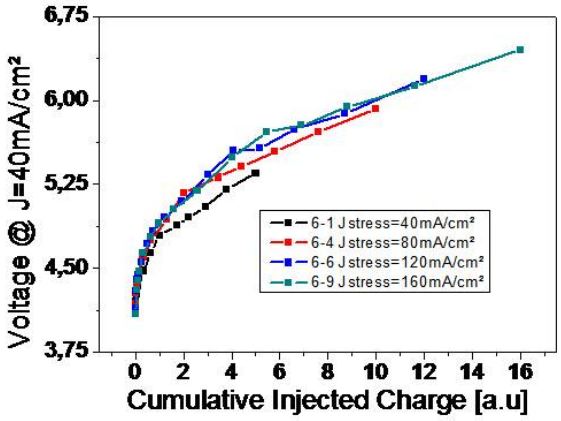


Figure 3.17: Voltage rise during stress time for the 4 devices, plotted as a function of injected carriers.

($TTF_{70\%}$) for all the four devices (orange arrows in Fig. 3.23), and we plot these values as a function of stress current density (shown in Fig. 3.25), we can calculate a TTF law. By plotting the $TTF_{70\%}$ as a function of stress current density in a log-log scale, we obtain a linear relationship that can be fitted (as reported in Fig. 3.20(d)). So we can hypothesize the following relation between $TTF_{70\%}$ and the bias current density J:

$$\log_{10}(TTF_{70\%}) = -1.56 \log_{10}(J) + 5.07 \tag{3.2.1}$$

$$TTF_{70\%} = 10^{(\log_{10}(J^{-1.56})+5.07)} = 117490 * J^{-1.56} \tag{3.2.2}$$

Using this equation it is possible to foresees the $TTF_{70\%}$ for any bias condition. For example if we consider a bias condition of $2mA/cm^2$ and $5mA/cm^2$ (values closer to the working point of these devices in real applications), we can obtain

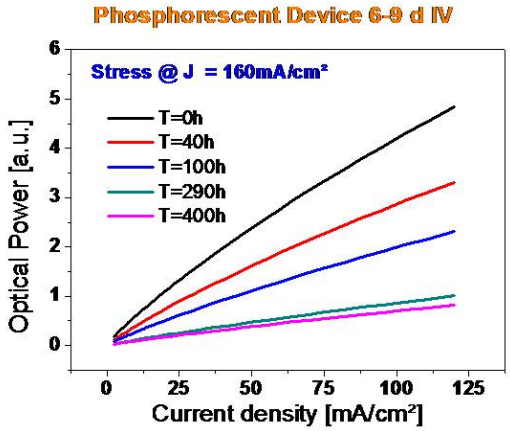


Figure 3.18: Optical Power plotted as a function of current density at different stress times for device stressed at 160mA/cm^2.

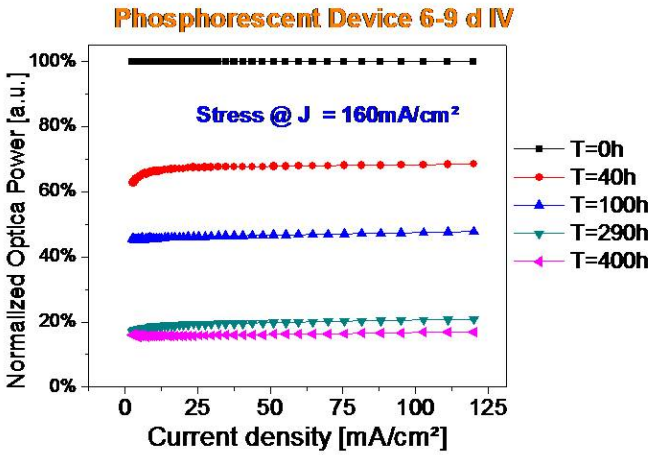


Figure 3.19: Normalized Optical Power plotted as a function of current density, at different stress times for device stressed at 160mA/cm^2.

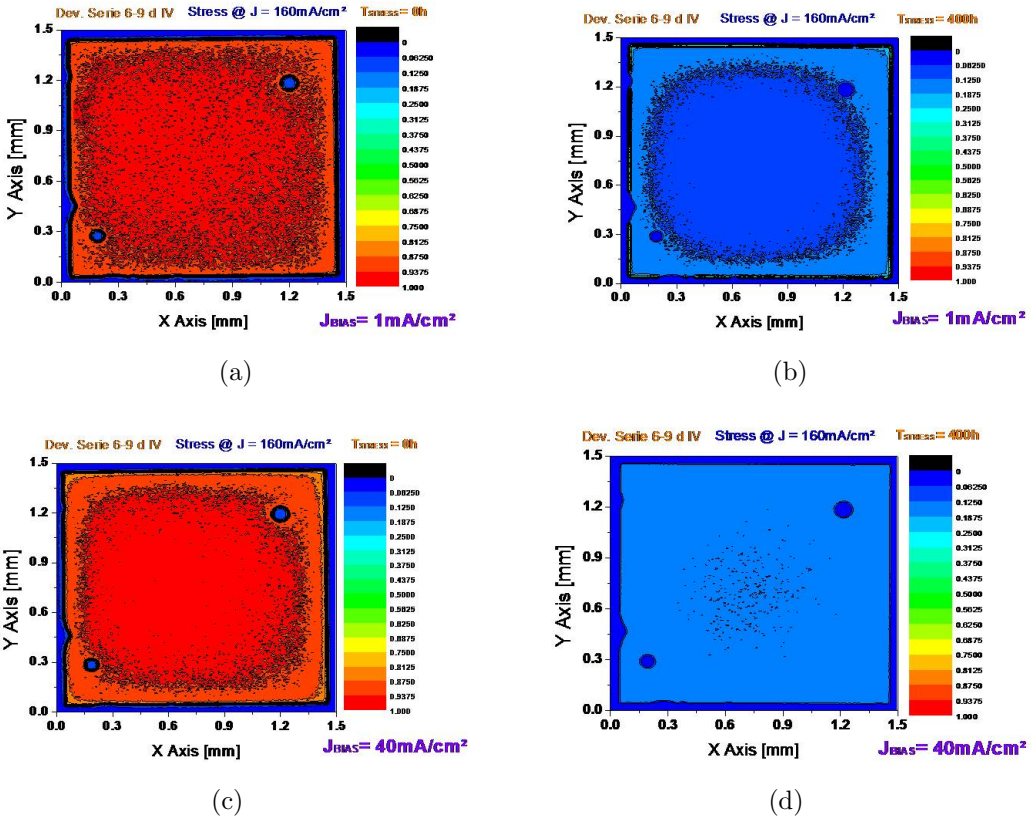


Figure 3.20: Light Emission Profiles of device stressed at a current density of 160mA/cm^2: (a) fresh, measured at 1mA/cm^2; b after 400 hours of stress, measured at 1mA/cm^2; (c) fresh, measured at 40mA/cm^2; d after 400 hours of stress, measured at 40mA/cm^2; .

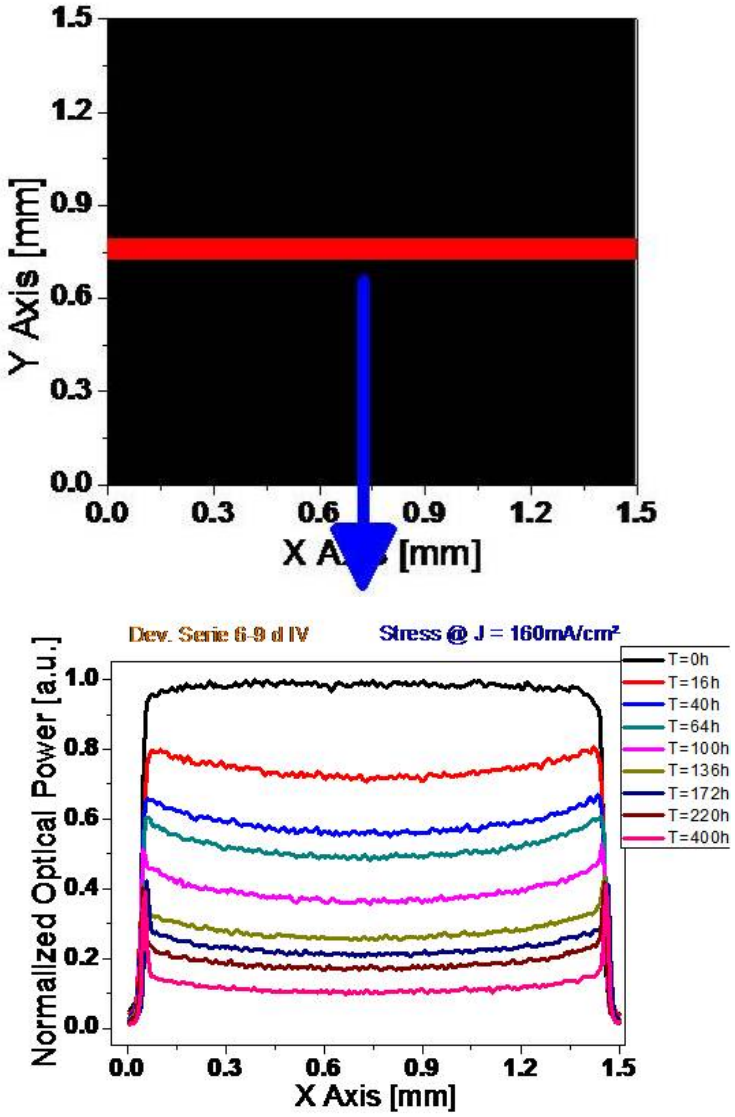


Figure 3.21: Longitudinal Light Emission Profile for device stressed at $160mA/cm^2$, measured at $40mA/cm^2$ at different stress times.

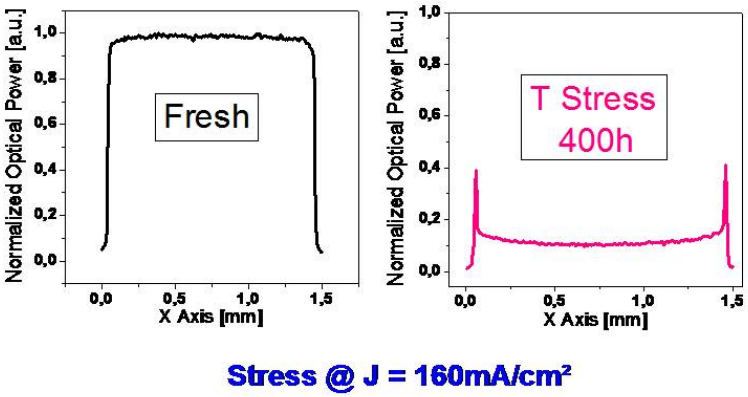


Figure 3.22: Longitudinal Light Emission Profile of a device biased at 1mA/cm^2, fresh and after 400 hours of accelerated stress at 160mA/cm^2.

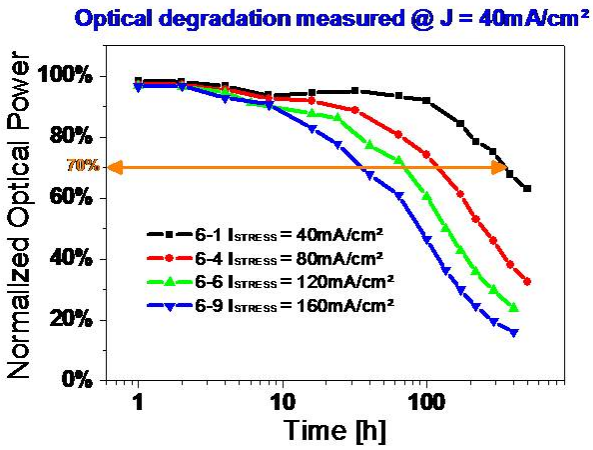


Figure 3.23: Optical power degradation kinetics for four devices, stressed using 4 different current levels. Orange line refers to 30% luminance decrease.

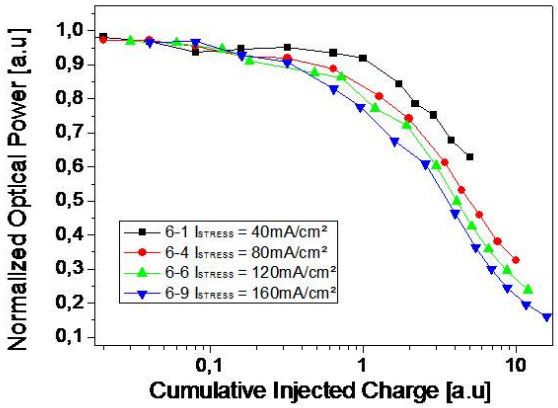


Figure 3.24: Optical power degradation kinetics for four devices, stressed using 4 different current levels and plotted as a function of cumulative injected charge.

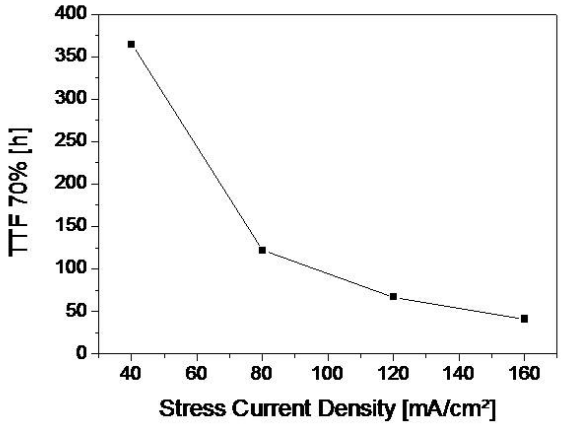


Figure 3.25: 70% Time To Failure (that corresponds to a 30% luminance decrease) plotted as a function of stress current density.

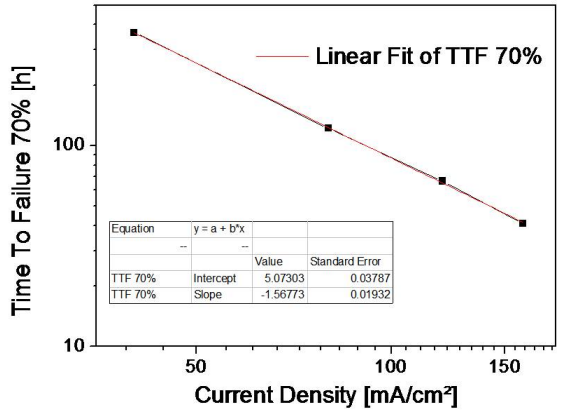


Figure 3.26: 70% Time To Failure as a function of current density, plotted in a log-log scale. Red line indicates the linear fitting of the curve, while in the table are reported the values of the fitting.

a $TTF_{70\%}$ of about respectively 40 and 10 thousand hours.

$TTF_{70\%}(J = 2mA/cm^2) = 39847hours$

$TTF_{70\%}(J = 5mA/cm^2) = 9541hours$

Our studies on phosphorescent OLEDs stressed at different current levels, show an increase of the operating voltage univocally correlated with the number of carriers injected in the devices during the stress. Moreover, studying the optical kinetics, we have observed a higher optical loss in the centre of the active area This stress effect will be further discuss in the next chapter. We have shown that is possible to extrapolate a Time To Failure law by analysing the optical degradation kinetics.

Chapter 4

Thermal study on Alq3/NPD OLEDs

This chapter is dedicated to the thermal study of organic light emitting diodes. In section 4.1 it is reported the description of a method for the evaluation of an important thermal parameter, i.e the *junction thermal resistance*. This method has been applied to standard Alq3/NPD, as well as to phosphorescent devices with different anode materials (see section 4.3). Moreover, we continue our study on the uneven light emission profiles reported in chapter 2, by studying the surface temperature distribution in section 4.2.

4.1 Evaluation of the junction thermal resistance

As previously mentioned in chapter 1, all the organic semiconductor materials need to be processed at low temperature (or at least much lower than their glass transition temperature). This limitation occurs also during the working of the finalized organic device, whose use is allowed only in a specific temperature range, in order no to decrease the expected life of the device. The determination of these thresholds is not straightforward, and it is strictly related to the operating conditions of the device. It is definitely important to be able to estimate the working temperature of a device in specific operating conditions and its capacity to exchange heat with the environment. The knowledge of these parameters can allow safe operation of the finalized device, but moreover it can help at a former level by influencing the choice of the materials, the design, and the kind and shape of encapsulation. Ultimately, the estimation of the thermal parameters, during and after the development phase, is essential in order to improve the performance and the lifetime of the finalized device.

A standard parameter that is considered for the thermal study of optoelectronic devices is the junction thermal resistance (R_{th}). This parameter gives informations about the operative temperature of the device. Knowing the R_{th} and the power dissipated by the device, it is possible to calculate the junction temperature (T_j) of the device. As over mentioned, the operative temperature of the device is usually related to its lifetime and to the optical and electrical

degradation mechanisms. In section 4.3 we will show a study where we compare the R_{th} of OLEDs built on different kind of substrates, namely ITO (Indium Tin Oxide) on glass, IZO (Indium Zinc Oxide) on glass. Finally, the thermal resistance can also be monitored during a reliability accelerated test, and the study of its variation can contribute in understanding the degradation mechanism that is taking place inside the device.

In order to evaluate the junction temperature (T_j) in OLEDs devices, we have used a method that monitors the change in the operation voltage of the device, allowing the extrapolation of the R_{th} (a detailed description of this technique is given in App. A). This method has been already adopted in other field of opto-electronics, for instance in the measurement of junction temperature in GaN-based laser diodes [60] and GaN-based light-emitting diodes [61, 62]. We have tested devices with NPD as HTL, and Alq3 as ETL. Voltage measurements have been carried out at different current densities (between 4 and 100 mA/cm^2) and temperature levels (between 55 and 75℃). All the voltage measurements have been carried out by using short current pulses (300μs), in order to avoid devices self heating (in these conditions we can assume that the junction temperature corresponds to the controlled oven temperature). Fig. 4.1 shows that for each measuring current level the relation between the corresponding voltage and temperature is roughly linear. Subsequently, the chamber temperature has been fixed at 55℃, and the devices have been biased for a fixed period of 60 seconds at each of the measuring current levels used before. The voltage variation across the OLED has been monitored, in order to obtain the thermal transient of the device (as shown in Fig. 4.2). The asymptotic voltage value at each current level, can be used to extrapolate the junction temperature (see App. A). Junction temperature versus current density and versus electrical power are reported in Fig. 4.3.

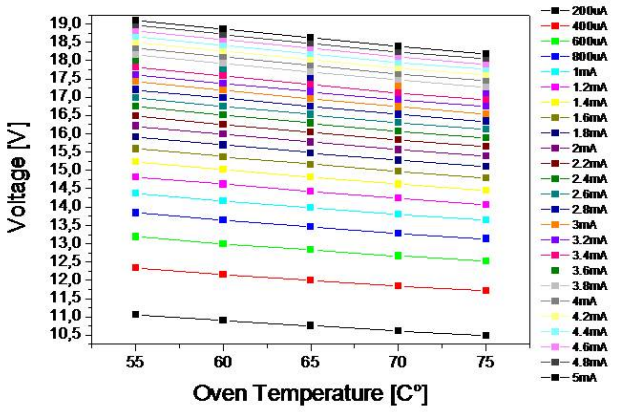


Figure 4.1: Voltage drop across the OLED, measured at different currents and oven (junction) temperatures.

In particular, from the linear fitting of this last graph (see Fig. 4.3(b)) we can extrapolate two important parameters, the intercept and the slope:

- The intercept is around 55℃, and this proves the reliability of our measurements being the oven temperature with switched-off device exactly at the

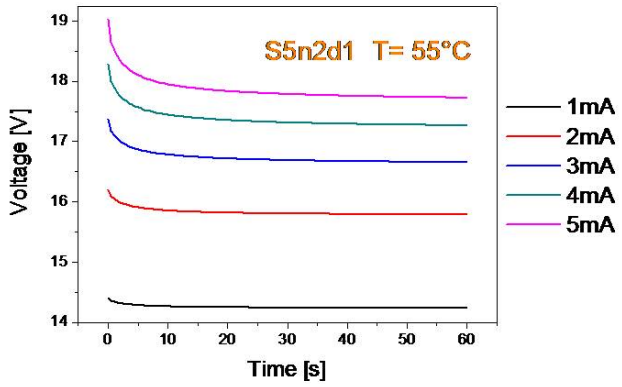


Figure 4.2: Voltage thermal transients, measured at different bias current densities.

same temperature.

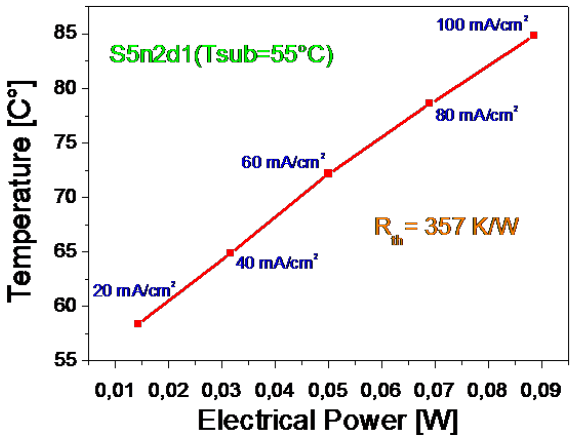
- The slope is the junction-to-ambient thermal resistance, that indicates the dissipation capability of the device.

It is worth noticing that the extrapolated thermal resistance slightly underestimates the actual value, due to the fact that the calibration measurements represented in Fig. 4.1 have been carried out assuming the junction temperature to be exactly equal to the temperature set in the thermal chamber, but a slight self heating can take place even during the short current pulses used for the characterization. The analysis repeated on a larger set of devices, has resulted in a junction thermal resistance between 300 and 500K/W for this kind of OLEDs.

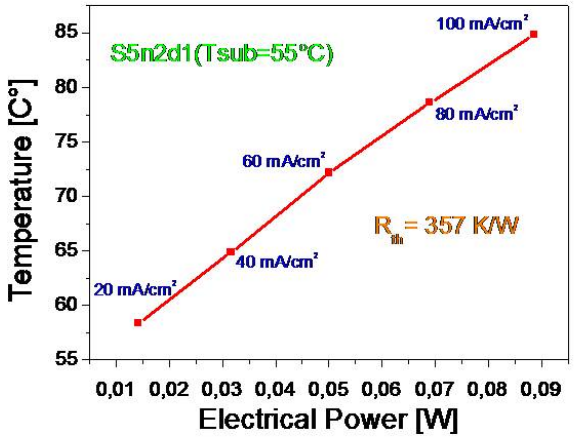
4.2 OLEDs surface thermal analysis

In this section we present the study of Alq3-NPD OLEDs with an active area of 5mm^2, subjected to thermal investigation by using an infra-red camera. In particular we have measured the surface temperature of these devices by using a *ThermoVision A20-M IR* camera. This camera tool has a spatial resolution of about 50μm and a temperature resolution of $\pm$2°C. The setup has been calibrated by calculating the emissivity coefficient, the entire procedure is automatically completed by the IR camera software.

First we had tried to measure the temperature surface profile at environment temperature, but the glass substrate naturally reflected the infrared emission of the circuitry of the camera beside the Focal Plane Array, introducing artefacts in the image. To avoid this reflection and others environment interferences, we have put the sample inside a thermal chamber at a temperature of 55°C, leaving accessible the light emission side of the device. Then, after reaching the thermal equilibrium, we have mapped the surface temperature profile at the desired current level.

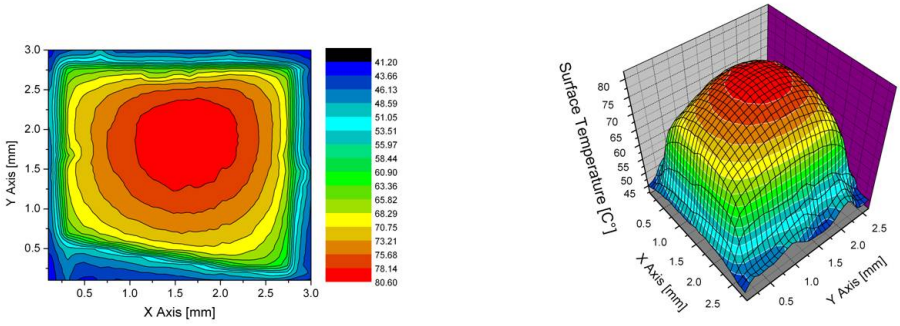


(a)



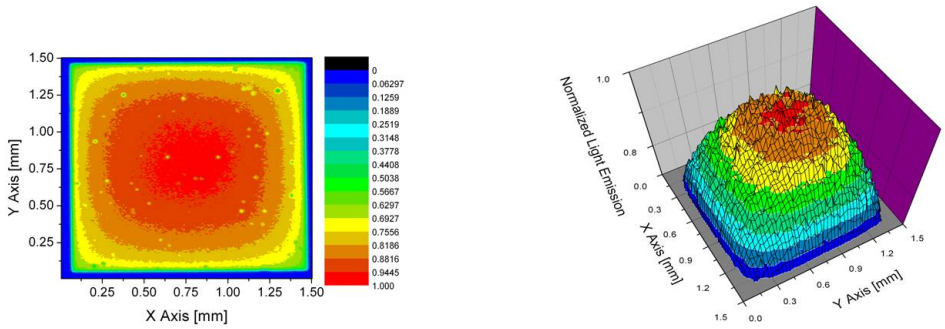
(b)

Figure 4.3: (a) Junction temperature vs current density. (b) Junction temperature vs electrical power.



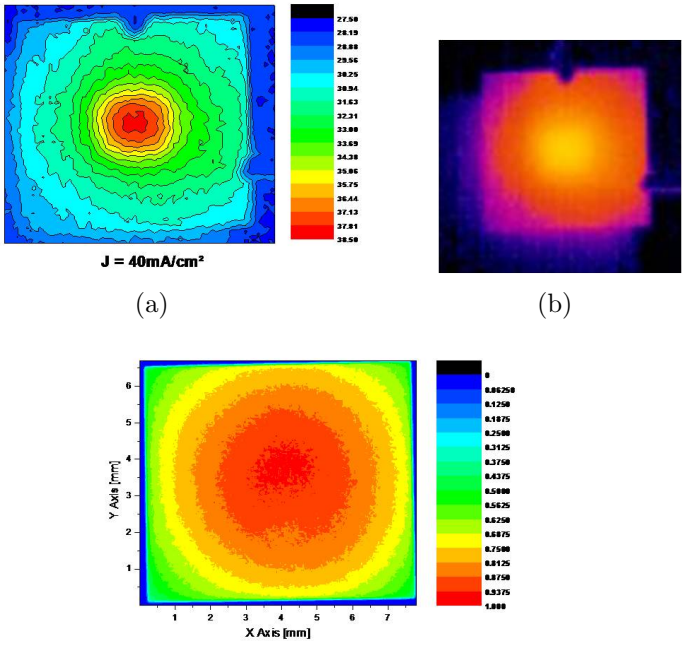
(a) (b)

Figure 4.4: Planar (a) and 3-D surface temperature profile of a 5mm² OLED, biased at 5mA.



(a) (b)

Figure 4.5: Planar (a) and 3-D light emission profile of a 5mm^2 OLED, biased at 5mA.



(a) (b)

(c)

Figure 4.6: (a) Thermal surface profile of a 0.5cm^2 OLED, biased at a current density of 40mA/cm^2. (b) Picture of heating distribution, obtained by using an IR thermal camera. (c) Light emission distribution above the active area.

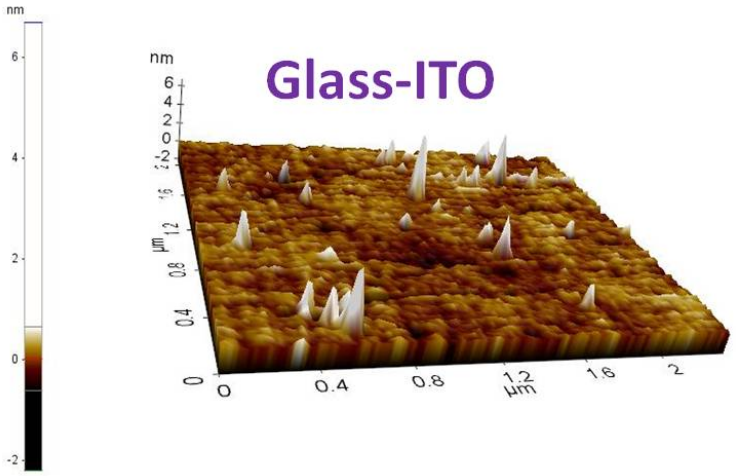
A surface thermal map is reported in Fig. 4.4 for a device biased at 5mA. We can observe that the self heating is more pronounced in the centre of the active area, and that it assumes a radial descendent trend. This is in agreement with the optical behaviour of this kind of devices, and we presume that it could be strongly related to current spatial distribution. In fact, analysing the light emission profile of the sample, at the same bias conditions (reported in Fig. 4.5), it is possible to notice the higher emission in the centre of the active area, already reported in chapter 2. The analysis has been repeated on a large area OLED ($0.5cm^2$), biased at $40mA/cm^2$ (data reported in Fig. 4.6). A reasonable explanation behind the two observations can be the following: biasing the device, the centre of the OLED becomes warmer due to a more difficult heat draining of the centre of the OLED compared with the border area. This means that raising the bias current, the effect should increase, and this is in agreement with what shown in chapter 2. An increase of the temperature determines a localized increase of the current density, thus generating a larger photon emission at the centre of the device. Moreover, the increasing of the flow current in the centre of the device raises the temperature of that portion of the active area, creating a positive feedback that is limited by the exchange of heat with the environment.

4.3 Thermal study on OLEDs with different anode materials

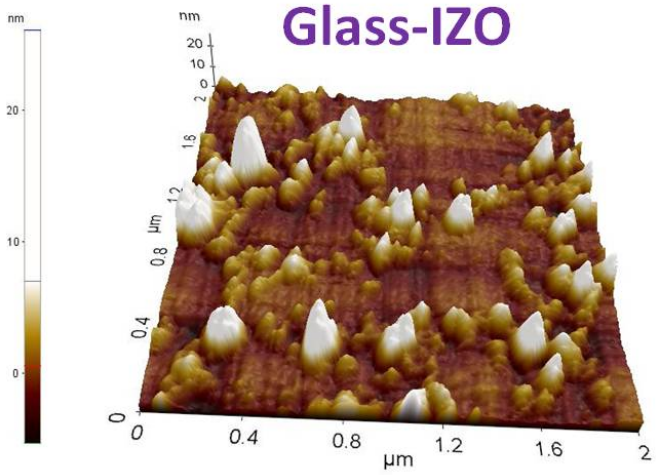
The performance of OLEDs are strongly influenced by the properties of the anode layer, that must have low resistance, high transparency, good chemical stability and exceptional surface smoothness. The most widely adopted anode material is ITO [63]: however, the use of this material presents a set of critical issues, including the release of oxygen and indium into the organic layers, chemical instabilities in a reduced ambient [64], and the need of high temperatures (up to 250℃) for the optimization of the electrical and optical properties of ITO anodes. ZnO-doped In_2O_3 (IZO) has been proposed as a viable alternative to ITO, because of its high work function and transparency [64, 65], high etching rate [66], low-temperature processing and good conductivity [64, 66, 67]. Recently, studies on the use of IZO for the realization of OLEDs has been reported, as well as on the comparison of the performance of devices with ITO and IZO anode [64, 68]. Nevertheless, no detailed analysis of the influence of an IZO anode layer on the reliability of the OLEDs has been presented up to now. In the following we show a comparison of the performance and reliability of Organic Light-Emitting Diodes with Indium-Tin Oxide and Indium Zinc Oxide anode contact layer. In collaboration with the American company *Universal Display Corporation* (UDC) we have performed a study comparing devices with different anodes material in terms of efficiency, thermal resistance and reliability.

The analysis has been carried out on two sets of $0.1mm^2$ OLEDs. One set of samples was prepared on commercial glass/ITO substrates, which consisted of a 20nm SiO_2 barrier layer between the soda lime glass and a 80nm thick ITO layer. The second set of devices was developed on glass/IZO plates, obtained by

etching off the ITO from commercial Glass/ITO substrates and then by sputter coating 80nm of IZO onto the substrates. The OLED contained a hole injection layer (HIL), a phosphorescent doped emissive layer (EML), a blocking layer (BL), and an electron transport layer (ETL). The cathode consisted of Aluminum (Al) deposited on Lithium Fluoride (LiF), and the active areas were defined by an insulating grid. All the devices have the same inner structure and they differ only for the anode layer material. An Atomic Force Microscopy (AFM) has been used in order to check the smoothness and uniformity of the two Transparent Conductive Oxides (TCO) . AFM image analysis of glass substrates coated with ITO and IZO lines (see Fig. 4.7) show a quite smooth surface profile with an RMS value below one nanometer for both substrates.



(a)



(b)

Figure 4.7: (a) AFM image of a commercial glass-ITO substrate (b) AFM image of a glass-substrate coated with IZO.

All organic layers were deposited under high-vacuum conditions (1x10^{-7} Torr) and devices were transferred directly from vacuum into an inert environment glove-box, where they were encapsulated using a UV-curable epoxy, and a glass lid with a moisture getter. The OLED emission profiles were assumed to be Lam-

bertian, and luminance normal to the substrate was measured with a SpectraScan PR705.

Before submitting the devices to the accelerated electrical stress, the electrical and optical characteristics of the samples on ITO and IZO substrate have been compared by means of current density-voltage (J-V) and luminance vs current density (L-J) measurements. A method for the evaluation of the thermal resistance of the samples has been developed on the basis of the technique proposed by Xi et al. [69]. The thermal resistances of the devices with different anode materials have been compared by means of this method (summarized in App. A). Finally, a set of devices with average characteristics has been selected for the ageing tests: OLEDs with ITO and IZO layer have been submitted to ageing tests at constant current density. The stress current levels were selected in order to obtain an initial luminance of 2000cd/m^2, and they corresponded to 73.1mA/cm^2 and 75.6mA/cm^2 for the devices with ITO and IZO anode respectively. During stress, we have continuously monitored the optical power and the forward voltage of the devices, in order to achieve a good description of the degradation kinetics. The devices have been physically realized in the company *UDC* and have been subsequently characterized in our labs in Padova. Results of this analysis are reported in the following.

First of all the different devices have been optically compared. Fig. 4.8 shows the luminance expressed in candles per square meters (cd/m^2) of a device with ITO anode and one with IZO anode layer. The emission intensity of the two different samples has been found comparable.

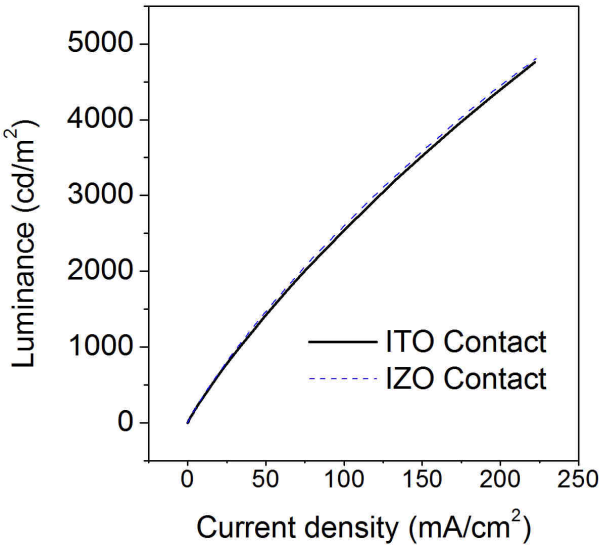


Figure 4.8: Luminance vs current density (LJ) characteristic of devices with ITO and IZO anode and equal inner structure.

Subsequently, the devices have been electrically characterized. As shown from the current-density vs voltage graph of Fig. 4.9, the use of an IZO contact improves the electrical properties of the OLED structure, allowing a slight reduction of the operating voltage of about 0.4V. In fact, at nominal current density of

40mA/cm^2, the voltage drop on the OLED with ITO contact is 11.31V, while it decreases to 10.91V for the device with IZO anode.

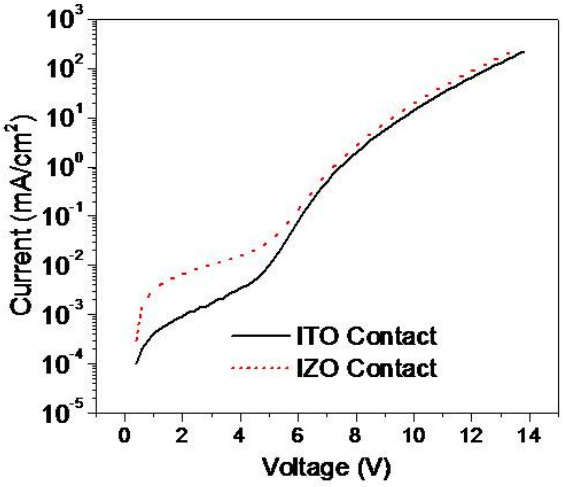


Figure 4.9: Current density vs Voltage (J-V) characteristics of devices with ITO (solid line) and IZO anode (dashed line) an a semi-log scale.

After the electrical and optical characterization we have performed a thermal analysis. The evaluation of the thermal resistance of the samples has been carried out by using the method proposed by Xi et al. in [69], and explained in section 4.1 and App. A. This method consists of two phases, a calibration phase and a thermal resistance evaluation phase. During the calibration phase, we have placed the devices in a thermal chamber, and evaluated the dependence of the forward voltage on junction temperature (in the range between 35 and 65°C) for different measuring current levels. The measurements have been carried out by means of short current pulses, so that no significant self-heating was introduced. Under these conditions the junction temperature (T_j) corresponded to the chamber temperature, allowing the mapping of the forward voltage as a function of the junction temperature at a given current level (I_M). For each I_M, the junction voltage was found to have a linear dependence on temperature, as shown by the $V(I_M;T_C)$ curves reported in Fig. 4.10.

After this initial calibration phase, we have fixed the temperature in the oven at 35°C, driven the OLEDs at each of the measuring current levels I_M used in the calibration phase, and we have evaluated the voltage reached by the devices at the end of the self-heating transients (see Fig. 4.11). From these voltage values it is possible to evaluate the junction temperature at the different driving current levels, and therefore to evaluate the thermal resistance of the devices [69]. From this analysis we have found that the devices with IZO contact have a significantly lower thermal resistance (R_{th}= 5.7K/mW), compared to the OLEDs with ITO anode (R_{th}= 10.3K/mW). Detailed results for the set of analysed devices are reported in Fig. 4.12. Subsequently, we have decided to investigate the reliability of the different devices. In Fig. 4.13 we compare the typical optical degradation of devices with ITO and IZO as anode contact. Both the sets of devices showed an initial recovery phase where, in the first 10 hours of electrical stress, the optical power increased of about 5% with respect to the initial value. After this phase we

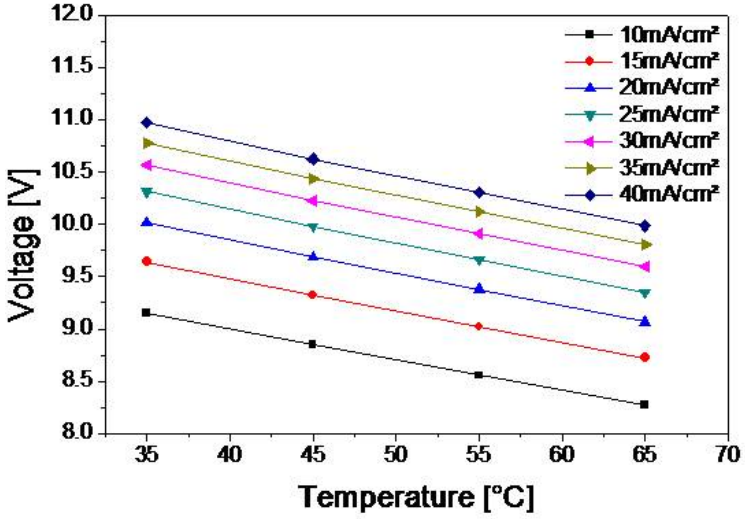


Figure 4.10: Voltage as function of oven temperature, for a device biased at different current density levels.

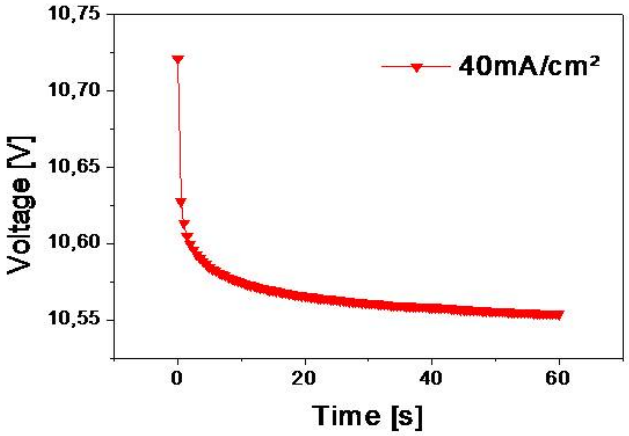


Figure 4.11: Voltage transient of a device biased at a current density of $40mA/cm^2$.

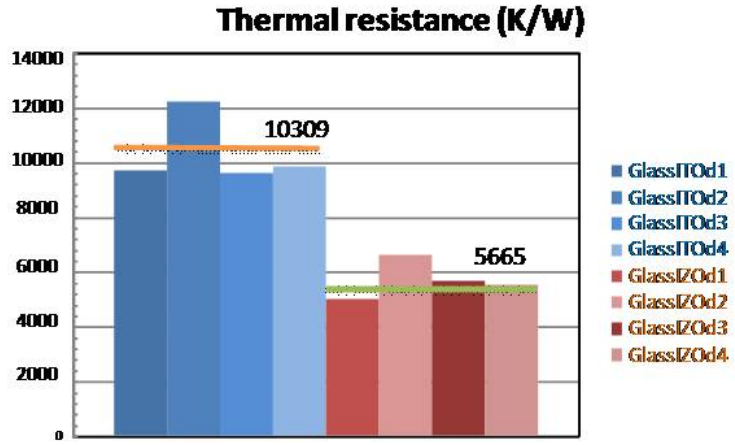


Figure 4.12: Thermal resistance evaluated for devices with ITO anode and with IZO anode (two sets of four devices). The devices with ITO and IZO anode show respectively an average thermal resistance of 10.3 K/mW and 5.7 K/mW.

found a different degradation behaviour for the two sets of devices. In particular OLEDs with ITO as anode contact showed a faster optical degradation compared to the devices with IZO contact: the 70% time to failure ($TTF_{70\%}$, i.e. time necessary for a 30% decrease of the optical power) was 140h and 200h, for the OLEDs with ITO and IZO anode contact respectively.

This results indicate that the use of an IZO contact can guarantee a significant improvement of the reliability of the devices, even under the accelerated stress conditions used within this work. Finally, in Fig. 4.14 we report the trend of the voltage drop on the devices during the stress phase. OLEDs with ITO as anode, has a higher forward voltage compared to the devices with IZO anode. In particular for both devices during the stress we have a rise of the operating voltage: 29% of increase for both devices when they reach the 60% of their initial luminance.

Therefore, we have demonstrated that Indium Zinc Oxide could be a good candidate to substitute Indium Tin Oxide in OLEDs technology. In particular the results of this study indicates that:

- The use of an IZO anode ensure optical efficiency comparable to the use of ITO contacts.
- Devices with IZO contact have a significantly lower thermal resistance, compared to the ones with ITO anode, therefore they are subjected to a lower self heating during standard operation conditions.
- Accelerated stress tests show that the OLEDs with IZO anode shows longer lifetime compared to devices with ITO anode.

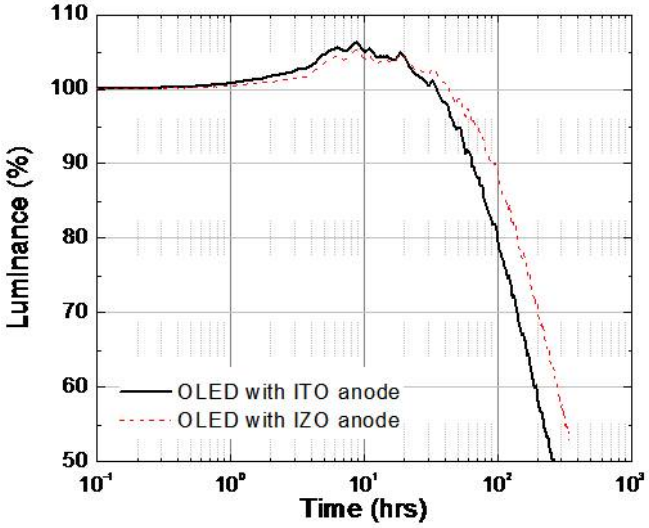


Figure 4.13: Luminance degradation curves measured during stress for OLEDs with ITO (solid line) and IZO anode (dashed line).

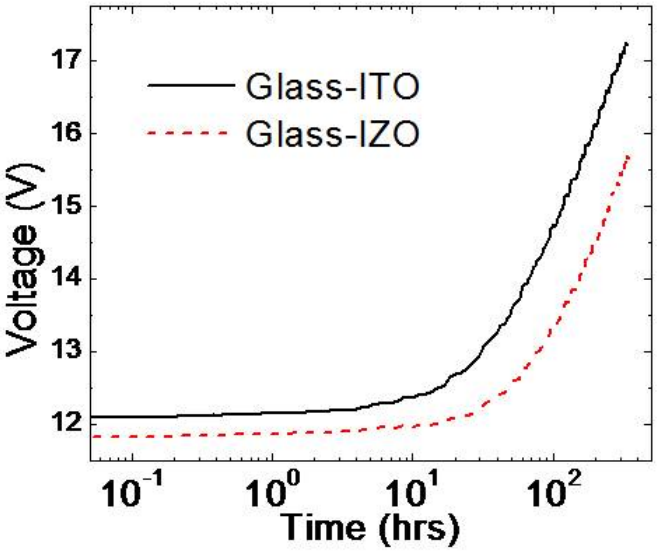


Figure 4.14: Forward voltage increase, measured during accelerated electrical stress for OLEDs with ITO and IZO anode.

Chapter 5

OTFTs technology development

In the previous chapters we have reported characterization and reliability studies on OLEDs, while from this chapter on we deal with OTFTs processing and development. In particular, we focused on the development of silver top contact OTFTs, realized by photo lithography, by using both wet and dry etching processes.

5.1 OTFTs processing

Organic thin-film transistors can be fabricated in a number of way, depending on the aim of the experiment or the field of application of the final device. Figure 5.1 shows some of the possible configurations. These structures are obtained by exchanging the positions of the fundamental elements (source and drain, gate, dielectric and the organic semiconductor) that constitutes the device. Each configuration clearly imply a specific flow of processing. In the case of a *Bottom-Contact configuration* the source and the drain are covered by the organic semiconductor (as in the *Top-Gate configuration*). Instead, in the case of a *Top-Contact configuration* the organic semiconductor is put upon the dielectric, and the contacts are built upon the semiconductor (see fig. 5.1).

Top Contact OTFTs can be processed on a highly doped n++ Si wafer that acts both as a substrate and as a gate electrode. On the top of the n++ Si it is present a thin layer of silicon dioxide (SiO_2), that plays the role of dielectric of the final transistor. SiO_2 can be thermally grown on Si wafer or deposited by sputtering or chemical vapour deposition (CVD) on other substrates. At the backside of the sample, a thin layer of evaporated Aluminium usually ensures a better ohmic contact between the gate and the chuck probe during the measurements. The contact pads are usually realized in Gold (Au) that, due to its work function, ensures great holes injection. The research community is putting effort on replacing this expensive metal with other materials.

In the following sections I will show our results on this specific research field. For processing OTFTs we can mainly distinguish 2 ways : with or without photolithography. By using *shadow mask* it is possible to define the semiconductor

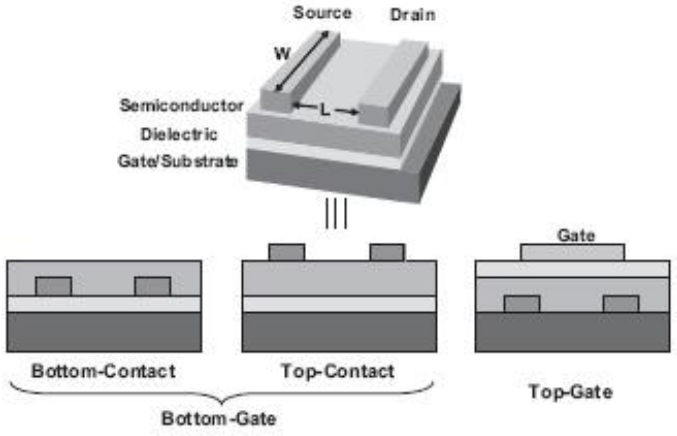


Figure 5.1: Different structures of organic thin-film transistors.

and the contact pads area directly during their evaporation. This technique prevents the need of the expensive and time-consuming photolithographic steps. Unfortunately, the main and decisive drawback of this technique is that it does not allow to define channel lengths lower than $30\mu m$. Also the rough alignment of the masks, during different processing steps, limits the use of this technique for developing complex structures and circuits. The other way of processing OTFTs adopts photolithography. Photolithographic steps can be used for patterning the metal contacts, the dielectric, the semiconductor and to open the vias. The lithographic processing allows the scaling down of the channel length till few micrometers and the alignment of different photolithographic steps can be done with submicron accuracy. The patterning of the semiconductor is essential in order to lower leakage current and therefore to improve the I_{ON}/I_{OFF} current rate [11]. The OTFTs developed within this work contain a Pentacene layer deposited by OMBD. The deposition takes place in ultra high vacuum conditions at a rate of about 0.25 Å/s and keeping the substrate at a temperature of about 68℃. Further details about this deposition technique, and about the specific tool used in this work are provided in App. C.

In the following I will provide some details about the processing techniques that have been used during this work. Initially the Si-SiO_2 substrates are subjected to a standard cleaning that consists in an ultrasonic bath of few minutes, dipping in Acetone at a temperature of about 60℃ for 1 minute and dipping in isopropanol (IPA). The cleaning is completed by a fast oxygen plasma treatment. Before the deposition of the organic semiconductor, a specific surface treatment protocol has been applied (details in App. B), in order to allow a good growth of the Pentacene upon the dielectric and/or upon the metal pads, and achieve high level mobility. The thickness of the semiconductor has been chosen quite thin (between 30 and 50nm) in order to reduce the parasitic current. For the photolithographic steps we have used chromium masks manufactured by the British company *Photronics (UK) LTD*. The masks have been designed in order to pattern interdigitate structures with different W/L (width/length) ratio. After lift off and etching processes, the samples were rinsed in deionized water (DIW). At the end of the processing flow, the devices have been electrically measured by

a probe station in nitrogen atmosphere.

5.2 Photolitographic top contact OTFTs

Processing of thin films of small molecule organic semiconductors is more problematic compared to their inorganic counterpart. The electrical properties of these films are sensitive to chemical effects during the fabrication, such as exposure to organic solvents, resists and developers, plasma treatments, therefore many conventional processes cannot be directly used. Such limited processibility constrains also the use of specific device geometries. As it will be shown in section 6.1, standard OTFT for prototype applications uses an inverted device structure with a gate electrode, a dielectric, and two bottom source-drain contacts deposited and patterned before the pentacene layer evaporation. This structure implies a high contact resistance [70]. In addition, with the bottom contact device structure, the metal of the contacts must be resistant to oxidation and other chemical effects before the thermal evaporation of pentacene. This limits the choice of metal to high work function, stable materials like Au and Palladium (Pd). Therefore huge effort has been put by the research community in trying to develop a top contact processing flow for organic transistor. A variety of exotic methods for depositing or attaching top contacts on organic thin films have been reported. Examples include silicon membrane masking, shadow masking, lift off with re-entrant profiles, and ink-jet printing. These processing are often complicated, limited in resolution, or with degraded performance [71, 72]. Recently, this topic gained in importance due to the development of active-matrix flexible OLED displays. Top-emission OLED driven by OTFTs has been reported by SONY in 2007 [73]. As shown in the cross-section of Fig. 5.2, Sony used a top contact OTFT, where the organic semiconductor was patterned by using an integrated shadow mask[1]. With this solution a wide selection of flexible substrates can be taken in account for a top-emission structure. Sony proved its OLED display both on glass and PES film.

More recently, Sony has showed an upgraded full-color flexible top-emission AM-OLED display driven by organic TFT backplane [75] (pictures have been reported in Fig. 1.2 and Fig. 1.3). Moreover, what it is highly inherent to the present work, it is that the Sony researchers were able to manufacture an OLED active matrix by using a lift-off free and shadow mask free process (not even the integrated one used in the previous work dated 2007). They used a low-cost copper electrode for the source drain contacts (see Fig. 5.3). Understandably, no details were provided by Sony about the actual processing. One goal of the present work was to study an innovative processing flow for *photolitographically* patterning top contact OTFTs without the use of Au for the source-drain contacts (see structure in Fig. 5.7).

[1] An integrated shadow mask is typically a patterning that is realized upon a substrate. In a lift-off process a pattern is realized with a resist, a material is deposited upon the pattern and finally the resist is removed with some solvents, leaving behind the patterning of the material that was deposited above. In the case of the use of an integrated shadow mask the process is similar, but the resist is not washed away, but it physically remains inside the device [74].

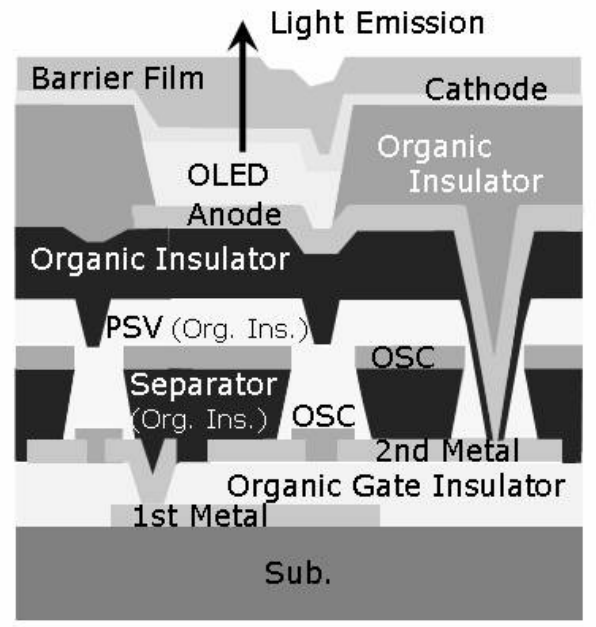


Figure 5.2: Cross-section of flexible SONY *OLED display. Note the patterning of the organic semiconductor by using an integrated shadow mask 1 (source: SID 09 [75]).*

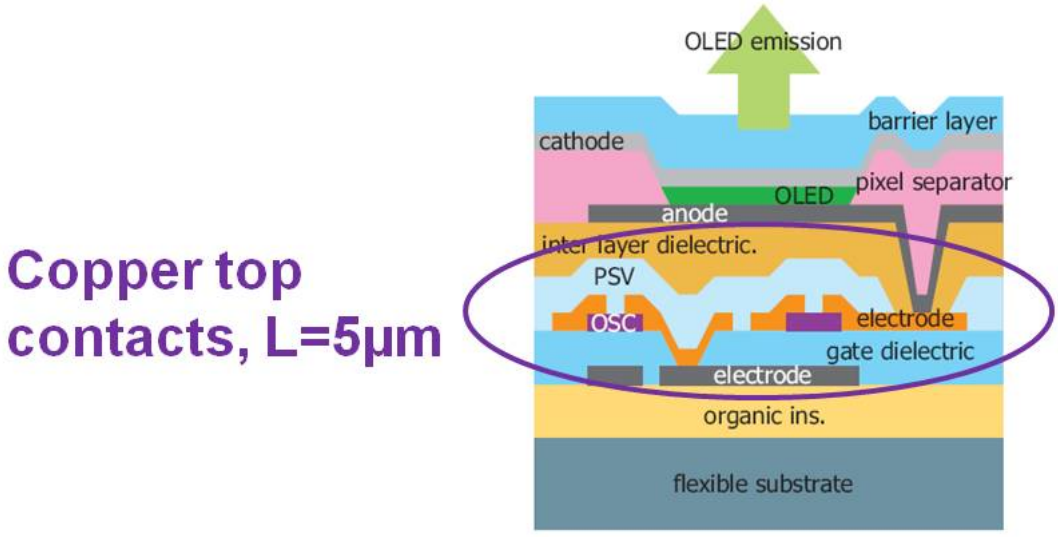


Figure 5.3: Cross-section of flexible SONY *OLED display. Note the patterning of copper contacts on the top of the organic semiconductor (source: SID 07 [73]).*

First of all we want to point out which were the main challenges of this research work. In literature it is reported how difficult is to use other metals in place of gold for contact pads in bottom contact OTFTs. Nevertheless, the use of a top contact structure should somehow ease this issue thanks to the strong vertical electric field that is created between the contact pads and the semiconductor and the gate in a vertical structure. This vertical field strongly enhances the injection of carriers. Therefore we can state that the substitution of the gold for the contacts, is strictly related to the development of a top contact structure. This has been proved by some preliminary tests where we have realized top contact OTFTs with different metals like, Chromium (Cr), Copper (Cu), and Silver (Ag) evaporated by using shadow masks. A shadow mask is a metal mask that is screwed upon the sample before the evaporation of the metal, in order to get the deposition only in specific areas. In this way it is possible to have a rough direct definition of the contact pads. The mobility curves of these samples are reported in Fig. 5.4, 5.5 and 5.6. The graphs show maximum mobilities between 0.2 and 0.4 $cm^2/(Vs)$. These curves showed that it is possible to realize top contact OTFTs with good mobility without using Au. Similar tests have also been realized by using Aluminium and Titan Tungsten.

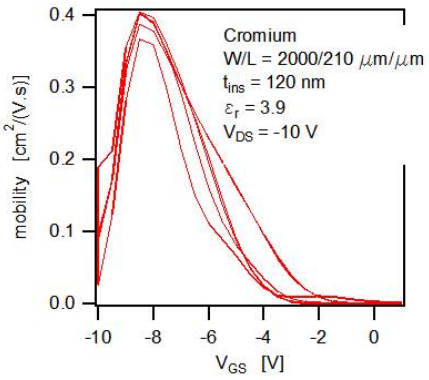


Figure 5.4: Mobility curves of OTFTs with Chromium contacts evaporated through shadow masks.

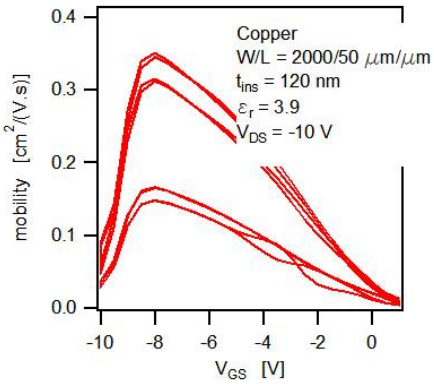


Figure 5.5: Mobility curves of OTFTs with Copper contacts evaporated through shadow masks.

These results where in agreement with what reported in literature, that is the possibility to manufacture top contact OTFTs with different kind of metal

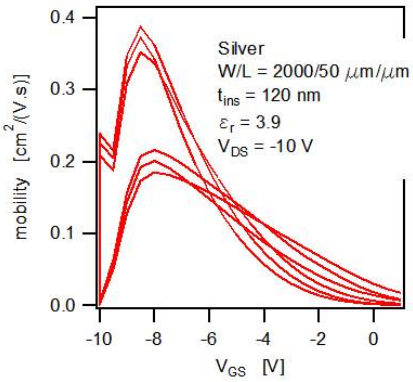


Figure 5.6: Mobility curves of OTFTs with Silver contacts evaporated through shadow masks.

evaporated though a shadow mask [76, 77]. Unfortunately, the use of a shadow mask does not allow to realize devices with a channel length lower than 30μm. The realization of complex organic circuits, even with the use of interdigitate structures, implies the use of OTFTs with a maximum channel length of 5-10μm. Such a low resolution is achievable only by using photolithographic techniques, and this is what this work aimed for.

Two were the main challenges of this work:

1. The first was to find proper photolitho products that do not damage the organic semiconductor below during processing. It is known that exposure of the semiconductor to a traditional solvent-based photoresist or developer would lead to a severe degradation of the semiconductor [78]. A further proof of the impossibility to use standard photolitho techniques upon Pentacene will be given in section 6.3.

2. The second one was to develop a feasible processing flow to concretely realize the top contacts OTFTs, by using a lift-off or an etching process.

An etching patterning is generally preferred because it gives a better spatial uniformity on the characteristics of the final devices. At the same time, as it will explained below, the realization of a dry etching on top of an organic semiconductor can severely damage it.

The first challenge has been partially solved by using innovative products developed by the *Orthogonal INC* (to this day several patents are pending on these new solvents). This company is developing innovative Hydrofluoroethers (HFEs) products that behave as orthogonal solvents for non-fluorinated organic materials. Here the adjective orthogonal means that there is not chemical reaction between fluorinated solvents and the not fluorinated materials. These products showed to work optimally and reproducibly for patterning organic semiconductors (in agreement with what reported by the inventors in [79, 80, 81]). Unfortunately, the critical step in our processing was the patterning of the metal on the top of the semiconductor. This required to try out different recipes with different parameters (spinning time, baking time and temperature, exposure, post baking

time and temperature, developing time) before finding a working solution. Moreover, the parameters showed to be dependent on the kind of metal that should be patterned. Specific details about the various tunable parameters of the spin coater are given in App. D, while informations about the mask aligner tool used within this work are reported in App. E. A specific filter has been used to adapt the ultraviolet (UV) light of the MA6 lamp to the exposure specifications of the orthogonal resist.

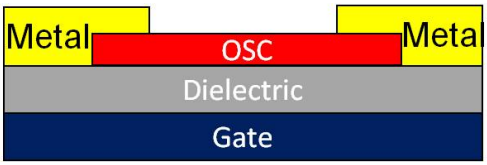


Figure 5.7: Top contact OTFT structure.

Referring to Fig. 5.7, in all our tests we have used standard Si-SiO_2 substrates. After a surface treatment with SAM monolayers we have evaporated 30nm of Pentacene. Afterwards a 50nm metal layer was evaporated upon the Pentacene. The main issue was to pattern this metal layer by using a lift-off, a wet etching or a dry etching process in order to obtain an OTFTs with the structure shown in Fig 5.7. Of course we were linked to the use of the orthogonal products in order not to damage the organic semiconductor. Many attempts have been performed by using Chromium, as well as Copper and Silver. No significant results have been obtained by using Chromium and Copper. The best results have been obtained by using Silver in place of Gold. Nevertheless, we want to point out that the lift off of the Silver did not worked due to the difficulties to pattern the Silver leaving no residuals upon the Pentacene. We will show how this issue has been overcome in section 5.4.

In the following I will explain in details the processing related to the development of Silver top contacts OTFTs, patterned by wet and dry etching.

5.3 OTFT with wet etched Silver Top Contact

As over mentioned, after several attempts with different metals and patterning techniques we were able to define a processing flow for patterning photolithographic top contact OTFTs. The main processing steps are reported in Fig. 5.8. As shown in Fig. 5.8(a) our processing start from standard Si-SiO_2 samples. Firstly we have evaporated 30nm of Pentacene by OMBD (see App. C). Subsequently the semiconductor layer has been patterned by using the orthogonal resist, developer and stripper. As mentioned in the previous section, such a photolitho step does not degrade the organic semiconductor. In Fig. 5.8 we have omitted photolitho steps for the organic semiconductor because they can be considered a standard process. All photolitho steps have been carried out in the yellow area of a clean room. The mask alignment and the exposure step have been realized by using an MA6 tool (for more details see App. D and App. E).

After the patterning of the Pentacene we have evaporated a 50nm layer of

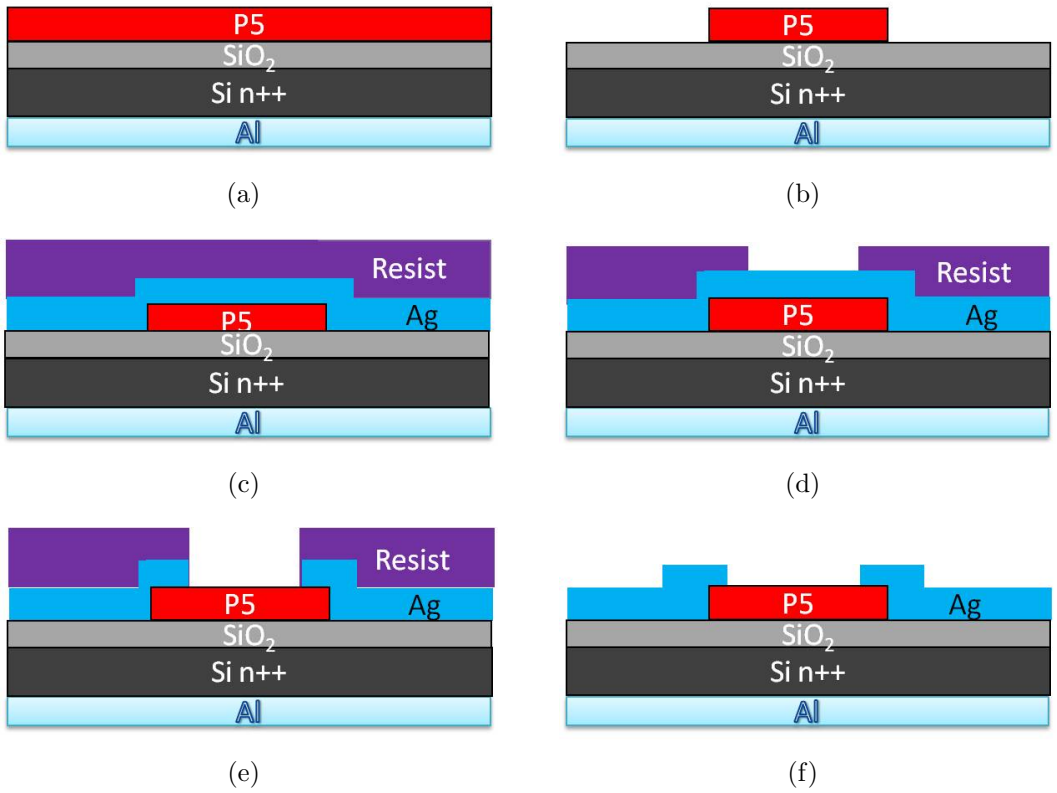


Figure 5.8: Wet etched Silver top contact flow: (a) Si-SiO_2 substrate after the evaporation of 30nm of Pentacene, (b) after the patterning of the Pentacene with the orthogonal resist, (c) a 50nm layer of Silver is evaporated and a 700nm layer of orthogonal resist is spin coated upon the substrate, (d) the orthogonal resist is adequately patterned, (e) the silver is wet etched by using a chromium etchant solution, (f) the resist is removed by using the proper stripper.

Silver upon the substrate, and then spin coated a 700nm layer of orthogonal resist as shown in Fig. 5.8(c), with the aim of realizing an etching process. Afterwards, by using a proper mask, we have patterned the resist. Here we had some optical problems in the developing of the resist. With standard photolitho products the correct developing of the resist after the exposure, and eventually, post-exposure bake phase, is verified under the microscope. The operation is done by checking if the channels are *open*, that is verifying if the developer had enough time to remove the resist also in the thinnest areas. This was not possible by using the special orthogonal resist for patterning the silver. Fig. 5.9 show one of our test structure after the development of the orthogonal resist. As you can notice, the $5\mu m$ line looks open, but a further investigations with a Dektat tool revealed that the development was not completed. This optical problem was the cause of many failed experiments before the definition of the correct development time.

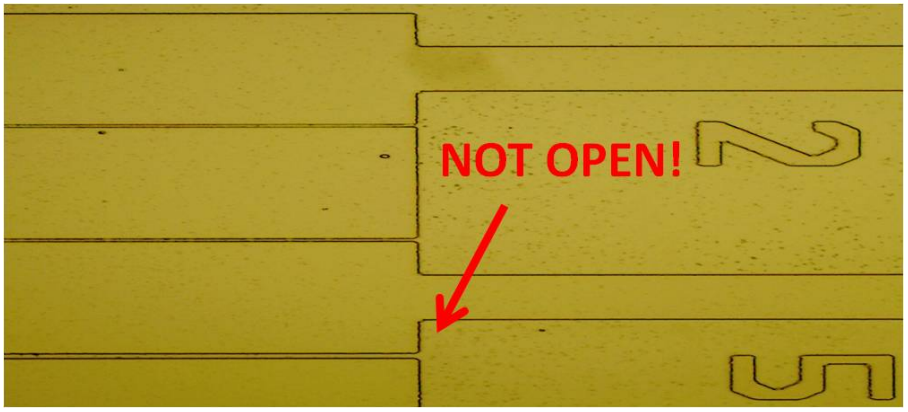


Figure 5.9: Test structure with incomplete development after exposure and post-exposure bake. The 5µm channel looks open but actually it is not.

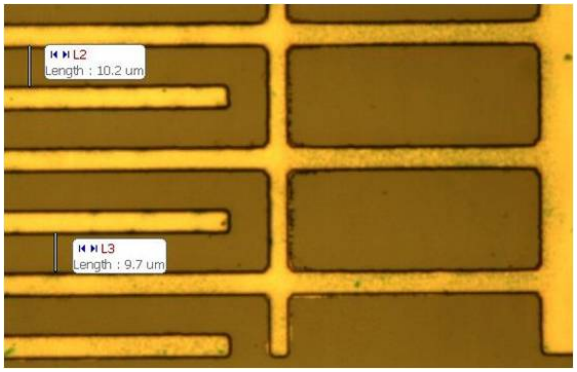
Subsequently, we had to face the most critical step, the wet etching of the silver (reported in Fig. 5.8(e)). The silver has been chemically attacked by using a chromium etchant solution.

We used two techniques to perform the etching:

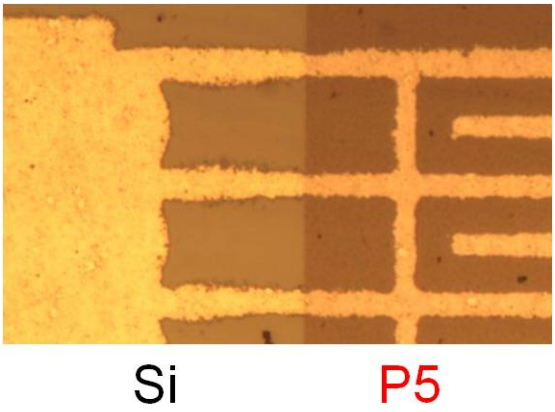
1. The first technique consists in the simple immersion of the sample in a becker filled with the etchant solution diluited with water. Several solution concentrations and different immersion times have been tried in order to get the best recipe. An accurate etching was necessary in order to etch completely the 50 nm of silver without harming the Pentacene semiconductor below, that was clearly sensible to contact with an acid etchant solution.

2. The second etching technique consists in the use of an automatic etcher. This tool consist of a teflon chamber, whereby the sample is place upon a programmable rotating plate. Different pipes reach the chamber. This pipes can pour water and etchant solution inside the chamber, as well as flushing the rotating sample with nitrogen. By tuning the rotation speed and time, flushing speed and time, it is possible to define the right parameters for the etching. Moreover with this tool it is possible to control the etching time with one tenth second accuracy.

Both techniques have been successfully used. In particular great patterning of the silver has been obtained by working with Si dummy samples (see Fig. 5.10(a)). It is common to singularly investigate the various steps of a long processing, in order to save time and resources. This is why at the beginning we have tried to develop our processing by patterning the orthogonal resist directly on Si dummy samples. Unfortunately when we moved to the structure reported in Fig. 5.8, we noticed the undesired effect reported in Fig. 5.10(b).



(a)

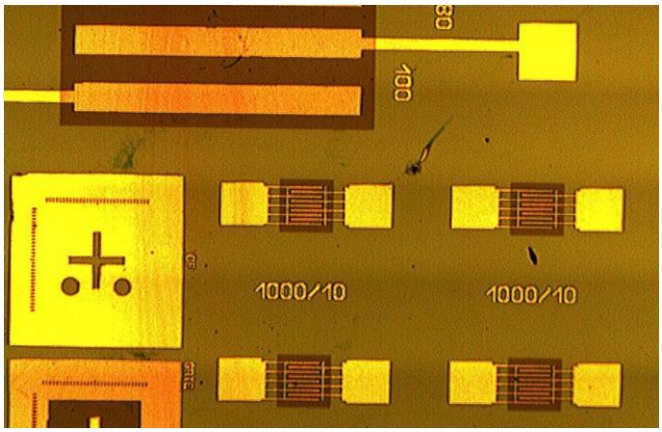


(b)

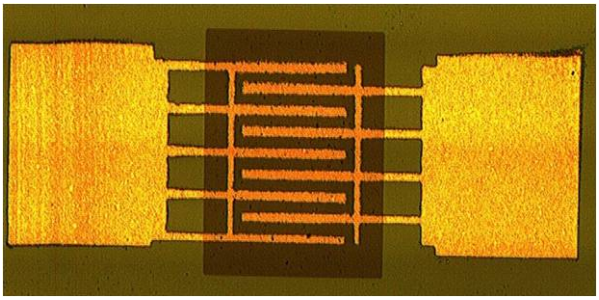
Figure 5.10: (a) Silver patterned on Silicon dummy sample. (b) In the left side the patterned silver is upon Si-SiO_2, on the right side it is upon Pentacene. The patterned silver upon the organic semiconductor looks more etched.

The patterned silver looked more or less etched depending on the fact that it was upon the SiO_2 or upon the Pentacene. Clearly the etching rate should be independent of that, and related only to the procedure of etching. We explained this phenomenon by assuming that when the etching solution reaches the substrate below the silver, there is an *under-etching* effect that is more prominent if the substrate is an organic material. Therefore, moving to the complete real structure, the etching step was even more critical, and the use of the automatic etcher became essential. This is why the best results, in terms of mobility, have been obtained by using the automatic etcher tool, mainly due to the lower time of contact between the Pentacene and the etchant solution required by this technique after the etching of the silver. The last necessary step of this processing is related to the stripping of the resist. Both stripping and development of the

orthogonal resist have been performed by using a spin coater in dynamic distribution dispense conditions (for further details see App. D). The structures obtained by using the steps previously described are shown in Fig. 5.11.



(a)



(b)

Figure 5.11: (a) Top contact OTFTs where the silver has been patterned by wet etching. (b) Zoom of a 5000µm/10µm photolitho patterned top contact OTFT.

OTFTs with 10μm channel length result well defined. Structures with thinner channels resulted over etched. Attempts to reduce even more the etching time resulted in an incomplete etching of the silver layer. Nevertheless, the 10μm channel length OTFTs showed great performance. Fig. 5.12 and Fig. 5.13 report the output and the transfer characteristics of one of the processed OTFT. The output characteristic shows that is possible to control the I_{ds} current through the gate terminal, obtaining a FET behaviour. The extrapolated parameters reported in the transfer characteristic of Fig. 5.13 are excellent. The devices showed a mobility higher than $0.5cm^2/(Vs)$, a threshold voltage around -3V, a onset voltage not far from 0V and a sub-threshold slope of about -0.5V/decade. Some of these devices have been subjected to bias stress. Applying to the device a gate-source voltage of +12, -12V, in order to get an effective +1,-1MV/cm stress electric field at the gate, and measuring the threshold voltage shift at logarithmic time intervals, we have obtained the graph reported in Fig. 5.14. We notice, for both positive and negative stress, a threshold voltage shift below 2V after 10 thousands seconds. These data are consistent with bias stability observed in literature for gold bottom contact Pentacene OTFTs.

So far we have showed that is possible to manufacture silver top contact OTFTs with great performance. This is done by patterning the source-drain

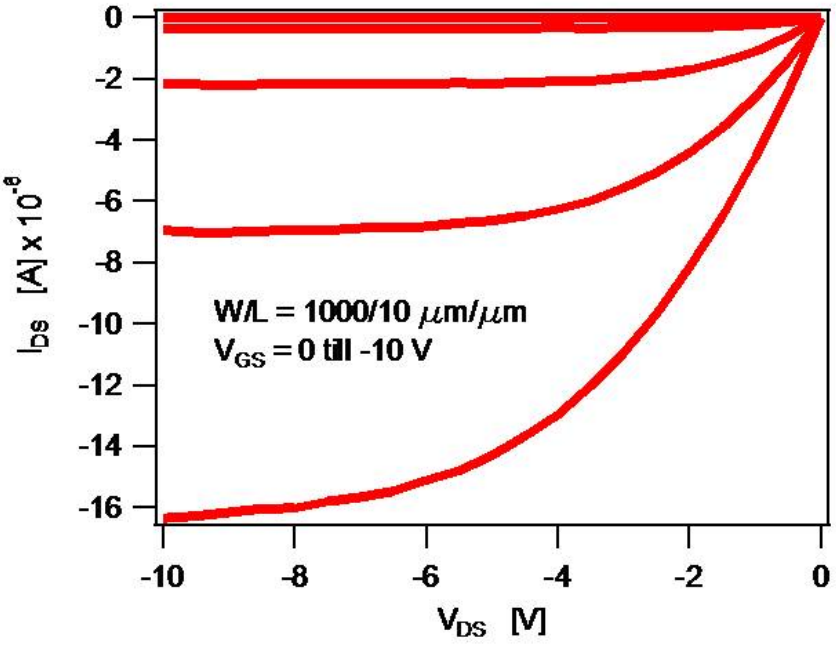


Figure 5.12: Output characteristic of a Silver top contact OTFT patterned by wet etching.

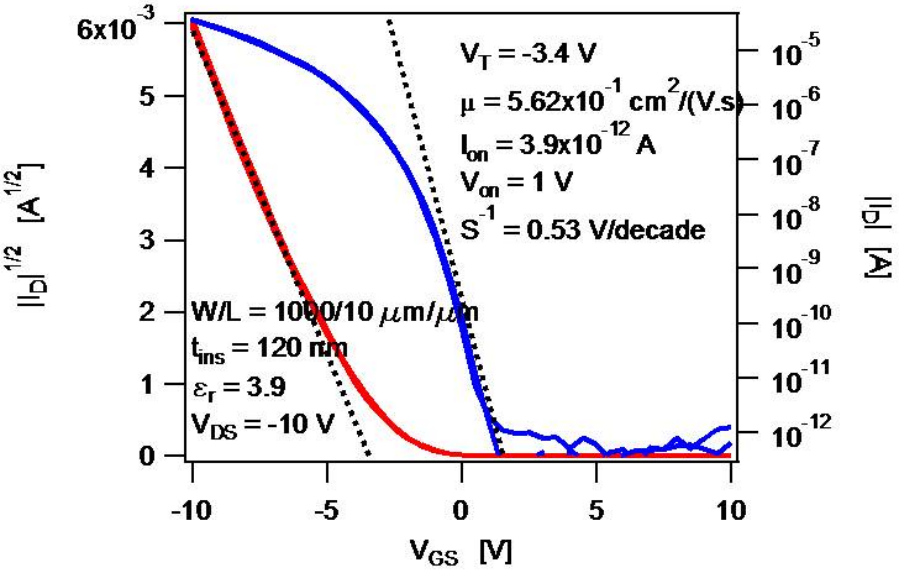


Figure 5.13: Transfer characteristic of a Silver top contact OTFT patterned by wet etching.

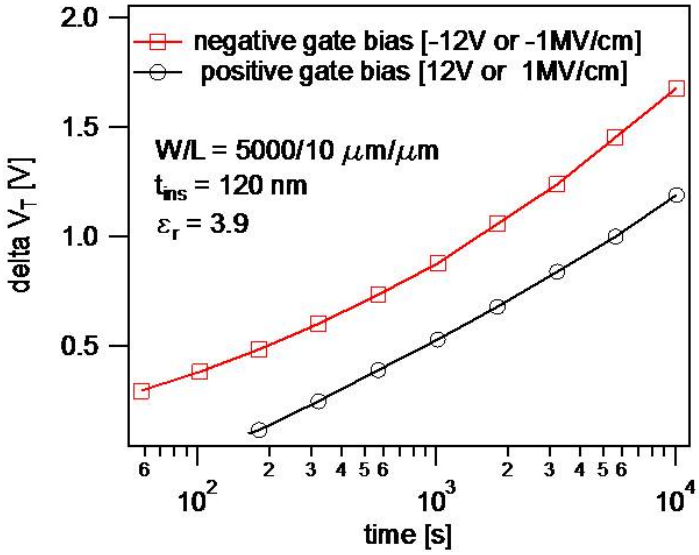


Figure 5.14: Bias stress on a Silver top contact OTFT patterned by wet etching.

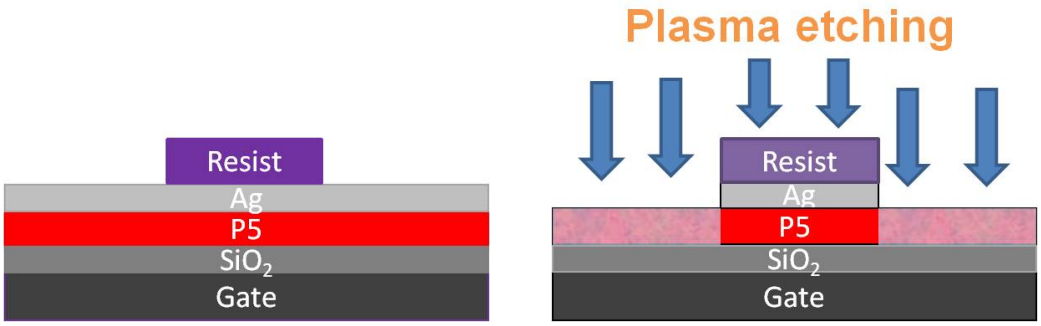
contacts by using a wet etching process with a chromium etchant solution. Unfortunately, as previous mentioned such a technique gives poor uniformity on the yield of the finalized sample. This is why we have also investigated a process flow for realizing OTFTs with Silver contacts, patterned by dry etching. This will be the main topic of the next section.

5.4 OTFT with dry etched Silver Top Contact

As over mentioned, the patterning of the contacts of an OTFT by using a dry etching process is highly favourable compared to the use of a wet etching or lift-off process. The main reason is related to the uniformity and accuracy that a dry etching ensures. We refer to dry etching as a plasma etching with the use of mixed ionized gases like Oxygen (O_2), Argon (Ar), and Carbon Tetrafluoride (CF_4). The radio frequency (RF) power and the flow of the various gases need to be tuned in order to get the correct recipe for the dry etching of the different materials. In our studies we have used specific parameters in order to etch a silver layer[2].

Unfortunately, the simple patterning of the silver upon the Pentacene layer, by using the orthogonal resist was not sufficient for obtaining working transistors. As shown in Fig. 5.15(b), if we try to etch away the silver upon the Pentacene, we have strong unwanted degradation of the semiconductor. One could argue that this problem was present also in the flow processing related to wet etched silver top contacts, presented in the last section. This is definitely true, and there this issue has been partially overcome by finely tuning the wet etching parameters in order to try to stop the etching just after the erosion of the 50nm silver layer. This was not feasible in a dry etching process. The point is that plasma has a specific

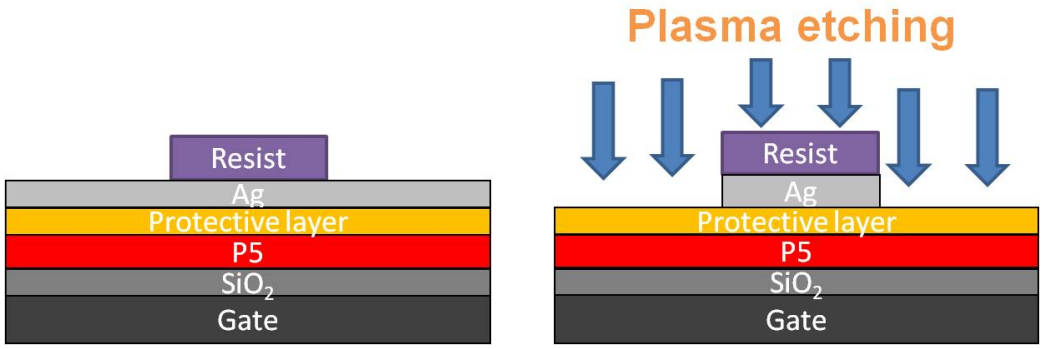
[2]We have used 60sccm Ar gas, 20sccm O_2 gas, and 60sccm CF_4 gas. The tool has been set at 150W RF power, and it has worked at a pressure of 0.03mbar.



(a) (b)

Figure 5.15: (a) Top contact flow where the resist ha been patterned upon the metal layer. (b) The plasma dry etching of the metal harms the Pentacene layer.

etching rate of the silver, but the etching rate toward the Pentacene is several times higher. Therefore, when the plasma reaches the Pentacene surface, after having etched the 50nm of silver, it quickly damages or destroys the Pentacene layer, and no calibration of the etching time is feasible. In order to overcome this issue we thought to modify the processing flow by inserting a *protective layer* between the Pentacene and the Ag. The main function of this extra layer was to protect the organic semiconductor during the plasma etching (as shown in Fig. 5.16).



(a) (b)

Figure 5.16: (a) Top contact flow where a protective layer has been deposited before the metal evaporation. (b) The plasma dry etching of the metal could be stopped by the protective layer, without harming the Pentacene layer.

The protective layer should guarantee several functions:

- It should be deposited upon the Pentacene without damaging the organic semiconductor, therefore with a low temperature deposition process.
- It should ensure good hole injection in the Pentacene from the Silver, that is should act as a HIL.
- It should ensure great vertical conductivity, and minimal lateral conductivity in order not to create leakage current paths.

- It should protect the Pentacene during the dry etching of the silver.
- It should not be damaged by the dry etching of the silver upon it.
- Eventually, it could also be patterned with a process that does not damage the Pentacene below.

We have strongly looked for a good candidate as protective layer, and finally we have tested two materials: Zinc Sulfide (ZnS), and Molibdenum Oxide (MoOx). These materials have been chosen for be tested because their work function indicate the possibility to inject holes in the Pentacene, and at the same time they have already been used in literature as HILs [82, 83, 84]. In particular we have experimented different thicknesses of MoOx, from 2 up to 10nm. Unfortunately, no significant results have been obtained from these studies. In particular, ZnS showed not to inject enough efficiently, so it was not possible to observe any transistor behaviour. Instead transistors built with MoOx partially worked. This oxide works as protective layer during the plasma dry etching. But its lateral conductivity was too high, and this implied a huge leakage current in reverse bias conditions. The consequence is an awful I_{on}/I_{off} rate, with just few orders of magnitude of difference between the on an the off state of the organic transistor.

Nevertheless the MoOx proved that the idea of protecting the Pentacene during the dry etching was correct. And this was the beginning of a complete reformulation of the problem flow that has ended in the successful and innovative process represented in Fig. 5.17 [3]. Thanks to this processing flow we were able to obtain dry etched top contact OTFTs, both on Silicon and foil substrate with good mobility and uniformity. This processing flow is mainly based on two ideas: the first one is to use the orthogonal resist itself as protective layer, the second one is to simulate a lift-off process, with the real aim of performing an etching one. In the following all the steps will be explained in details. As shown in Fig. 5.17(a), the first step is the patterning of the orthogonal photo resist onto the Pentacene. Afterwards the 50nm silver layer is evaporated upon the patterned resist (see Fig. 5.17(b)). This steps are usually done with the aim of performing a lift-off process, but this is not the case. Now another layer of orthogonal resist is spin coated upon the silver, and patterned by using the mirror mask of the one previously used for patterning the first resist layer (see Fig. 5.17(c) and Fig. 5.17(d)). In practice, first we have used the dark field version of the source-drain mask, and after we have used the light field version. In this way we have opened a via to the silver that is not in contact with the Pentacene, but just upon the orthogonal resist. As shown in Fig. 5.17(e) at this step it was possible to perform the dry etching by using the plasma tool (a DSE etcher tool). We want to point out that during the etching the plasma removes all the silver upon the orthogonal resist, and that the etching it is stopped by the thick layer of resist without being capable of harming the organic semiconductor below. Finally, as shown in Fig. 5.17(f), the orthogonal resist is stripped all along the sample leaving below the patterned silver contacts.

[3] For sake of simplicity in the structures of fig. 5.17 it has not been shown that the Pentacene is also patterned.

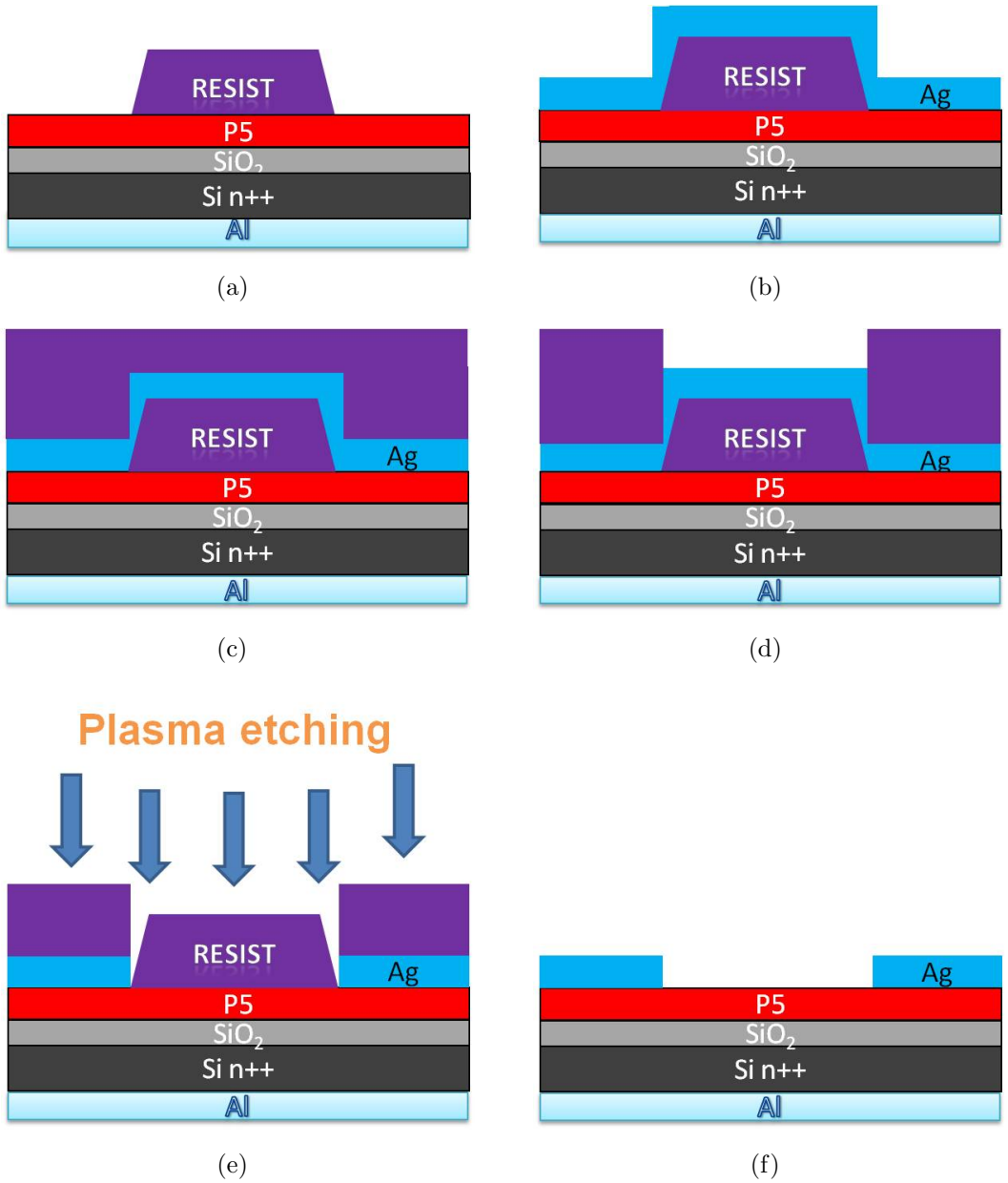
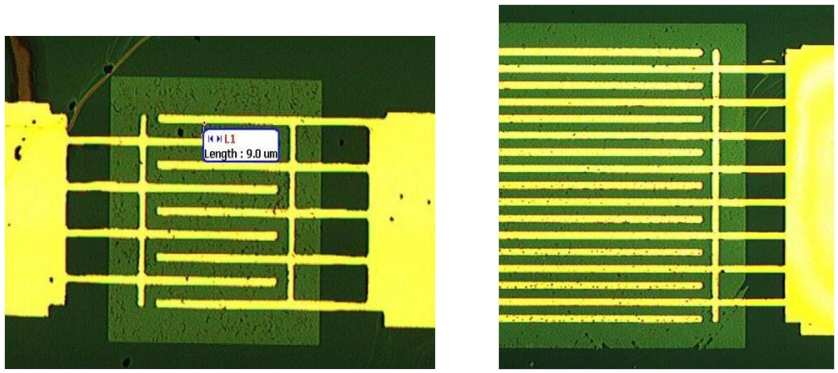


Figure 5.17: Dry etched Silver top contact flow: (a) here the orthogonal photo resist is patterned upon the 30nm Pentacene layer (like usually done in a lift-off process); (b) the 50nm Ag layer is deposited upon the patterned resist; (c) and (d) a further orthogonal resist layer is put upon the Ag layer and patterned with a mask that is the mirror of the one previously used in step (a)*; (e) the sample is subjected to dry etching, only the exposed silver is etched by the plasma, and at the same time after the removal of the silver the plasma is stopped by the thick resist layer; (f) the orthogonal resist is finally removed leaving below the patterned silver upon the undamaged Pentacene.*

By using this processing flow we were able to obtain well patterned devices, as the ones shown in Fig. 5.18.



(a) (b)

Figure 5.18: Dry etched Silver top contact OTFTs with (a) 10μm and (b) 5μm channel lengths.

The transfer characteristic of a 10μm channel length OTFT patterned by using this processing flow is reported in Fig. 5.19 and it shows good mobility (around 0.3cm^2/Vs), a threshold voltage of -1.3V and a sub threshold slope of 0.7V/decade.

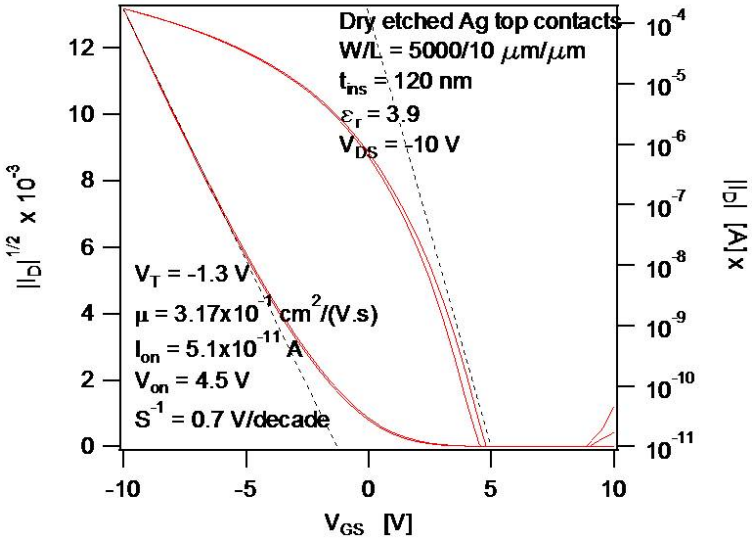
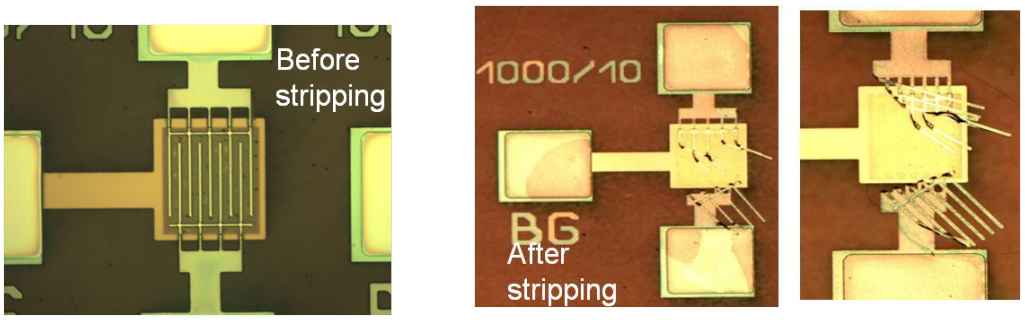


Figure 5.19: Transfer characteristic of a dry etched top contact OTFT with a 10μm channel length, in saturation conditions.

If we compare this processing flow with the one related to the wet etched silver contacts, presented in the previous section, we can observe that an extra photolitho step is required. In detail, in the processing flow presented in sec. 5.3 we count two necessary photolitho steps, one for patterning the Pentacene, and one for patterning the orthogonal resist upon the silver. In the processing flow presented in this section for silver top contact OTFTs obtained with dry etching, there is a photolitho step for patterning the Pentacene (see footnote 3), another one for patterning the resist upon the Pentacene, and a last one for patterning

the resist upon the silver, therefore 3 steps in total. Such a extra step can represent a significant increase of cost of the whole flow, especially looking at the industrialization of processing. Nevertheless, the exciting results obtained by using this technique, i.e. great uniformity and the possibility to scale the processing down to few micrometers of channel length, could largely justify the higher cost of this technological solution.

Moreover, we have tried to export the processing flow to a Polyethylene naphthalate (PEN) foil substrate, with an OTFT structure with 200nm of the polymer Poly-vinyl-pyrrolidone (PVP)) as a dielectric (clearly in a flexible structure it is not possible to use SiO_2 as a dielectric). All the processing worked correctly up to the stripping phase. As shown in Fig. 5.20(a), the sample looked optically perfect before the stripping, but afterwards the fingers have lost adherence to the substrate (see Fig. 5.20(b)). This problem is now under investigation but we strongly believe that should not be difficult to improve the adhesion between the silver and the Pentacene below (as shown in Fig. 5.20(b) the metal has a good adhesion upon the dielectric, and the problem is localized upon the organic semiconductor).



(a) (b)

Figure 5.20: Bad patterning of top contact OTFT on foil: (a) Before the stripping phase the devices look optically perfect; (b) After the stripping phase the interdigitated fingers have lost adhesion with the Pentacene below.

Nevertheless, it was possible to measure some basic OTFTs structures usually used for extrapolating the contact resistance. In Fig. 5.21 it is reported the transfer characteristic of one of this device with 100μm channel length. The device shows a mobility of 0.15 $cm^2/(Vs)$, an onset voltage of 2.5V, a threshold voltage of -2.2V and a subthreshold slope of 0.73V/decade. The values of these standard parameters are similar to those reported in literature for bottom contact OTFTs on foil.

The data, presented so far, testify that is possible to manufacture top contact OTFTs with silver source-drain contacts by using an etching process, both on Silicon and foil substrate.

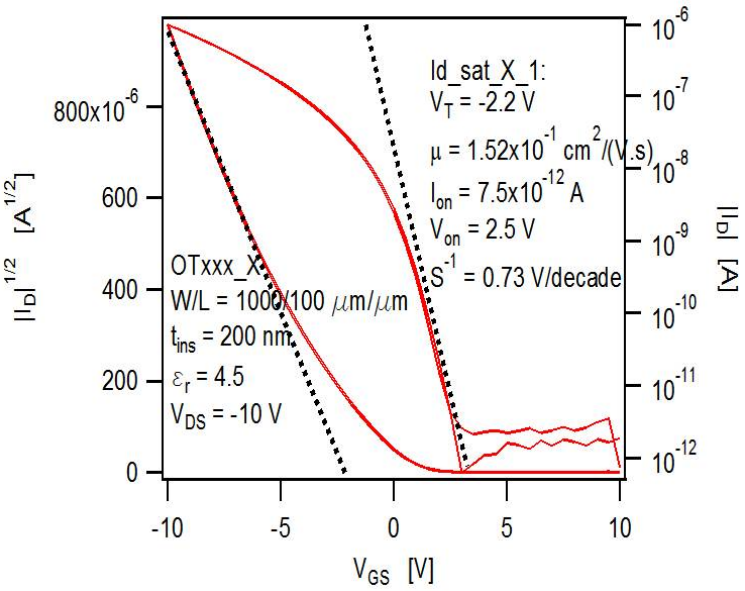


Figure 5.21: Transfer characteristic of a dry etched top contact OTFT on PEN foil with a 200nm PVP dielectric and a 100µm channel length. The curve has been measured in saturation conditions.

Chapter 6

Parylene encapsulation of Organic TFTs

In this chapter it is discussed the use of Parylene as encapsulation material for bottom contact OTFTs. Moreover, a specific study on encapsulated OTFTs is reported in section 6.3.

6.1 OTFT encapsulation

As explained in section 1.3, OTFTs and generally organic devices, need a proper encapsulation in order not to be subjected to a fast degradation. OTFTs transfer characteristics show large hysteresis when the devices are measured directly in air. The origin of these electrical instabilities has to be related to absorption of oxygen and/or water in the organic semiconductor film and charge trapping in the semiconductor or at the dielectric/semiconductor interface. A good encapsulation should protect the organic semiconductor from interactions with gas and moisture, light and other adverse environmental conditions [85, 86]. While transparent passivation layers are indispensable in organic electroluminescence devices (like the glass used for the OLEDs studied in the previous chapters), instead many applications of organic FETs require mechanical flexibility. Several solutions has been proposed in literature for encapsulating organic devices. One of the most promising it is the use of a single or multiples layers of the polymer Parylene [87, 88]. Other research groups tried to combine a Parylene layer with different oxide layers [89, 90]. Parylene film is a transparent, chemically stable polymer with low permeation rate of oxygen and water vapor. It has been considered a good candidate to be used as a barrier layer for FOLED (Flexible OLED) [91], due to its excellent homogeneous and conformal coverage, with no formation of pinholes and micro-cracks. In section 6.3 I will show some data that confirm the goodness of the choice of such a encapsulation also for OTFTs. As shown in Fig. 6.1 our test have been carried out on standard bottom contacts OTFTs. The devices have a 200nm SiO_2 dielectric and the gold contact pads are realized by lift off. Finally a 30nm Pentacene layer is evaporated by using an OMBD (see App. C for more details). In this case the semiconductor layer is not

patterned. Before the measurement, by using the needle of the probe station, a cut is done around the device under measurement in order to lower the leakage currents. Afterwards the device can be measured directly in a metal glove-box, avoiding contact to air.

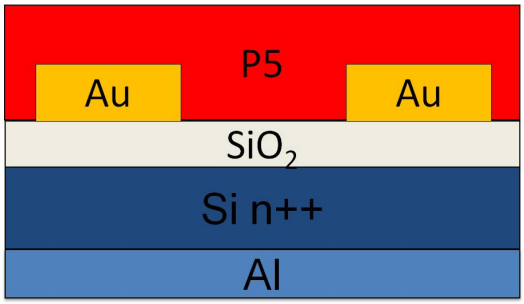


Figure 6.1: Standard bottom contacts OTFTs with gold contact pads, used for testing Parylene encapsulation.

In our experiments we have used a Parylene system with a load chamber integrated inside a glove-box (see App. F). The sample, after the first measurements, is put inside the Parylene system load chamber and it is coated with a variable thickness of Parylene-C. Our Parylene coating system ensures an accuracy of few tens of nanometres on the final encapsulation layer. Advantage of Parylene coating is that it is performed at environmental temperature and in vacuum conditions. As our measurements proved (see section 6.3), no degradation acts during the encapsulation phase. More details on Parylene material and coating can be found on App. F. One big advantage of encapsulating OTFTs, even at a research level, it is that after encapsulation the OTFTs can be subjected to an annealing phase in a vacuum oven at a temperature of 140℃, without any degradation or crystallization of the semiconductor, either a break of the device. If the OTFT is not encapsulated, such annealing is not possible because the high oven temperature changes the semiconductor crystal structure from the thin-film phase to the bulk phase, causing a drop in the mobility of the OTFT [92]. If we repeat the electrical measurements after such annealing phase, we usually observe an improvement of the characteristics of the devices, with the onset and threshold voltage that shift closer to 0V. This behaviour should be related to the release of gases and moisture during the annealing phase that can last up to 24 hours, but it needs to be optimized relating to the kind of substrate and organic semiconductor. Clearly, annealing phase has to be performed at lower temperature if a flexible substrate is used. In our studies we have used the polymer Parylene-C for encapsulation, however Yasuda et al. reported also the use of this polymer as a gate dielectric, with great FET performance [93]. Another variant of Parylene that can be successfully used as dielectric, as shown in literature [94], is Parylene-SR, developed by the Japanese company *DSK Da Isankase Iko. LTD.* In the next session I will provide some informations about the use of Parylene for encapsulation.

6.2 Parylene-C as encapsulation coating

For encapsulating our test bottom structures devices we have decided to use the polymer Para-xylylene C, alias Parylene-C. This is an inert, hydrophobic, bio-compatible coating material used in a wide variety of industries.

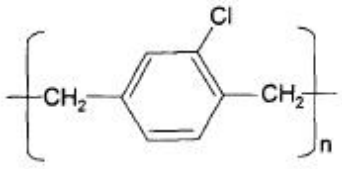


Figure 6.2: Structure of Parylene-C.

Parylene-C exhibits static and dynamic coefficients of friction in the range of 0.25 to 0.33 and this allows the use of this material as a dielectric and/or encapsulant in flexible OTFTs (in such devices the use of SiO_2 is not possible). The chemical structure of Paralyne-C is shown in figure 6.2. The room-temperature vapour deposition of Parylene results in a pinhole-free, relatively smooth and uniform film. Its excellent electrical and mechanical properties in electronic applications have been already partially demonstrated [95]. Parylene-C offers an excellent combination of electrical and physical properties, including very low permeability to moisture and corrosive gases. The Parylene coating gives a continuous transparent and conformal film. Para-xylylene film is applied to substrates in an evacuated deposition chamber by a process known as vapour deposition polymerization (VDP). This involves the spontaneous desublimation of a vapour that has been formed by heating a dry, powdered raw material known as dimer (shown in fig. 6.3). This vapour converts, at room temperature in low vacuum conditions, to an inert polymer film on substrate surfaces in a dry, non-solvent and catalyst-free process.

Figure 6.3: A box of Parylene-C.

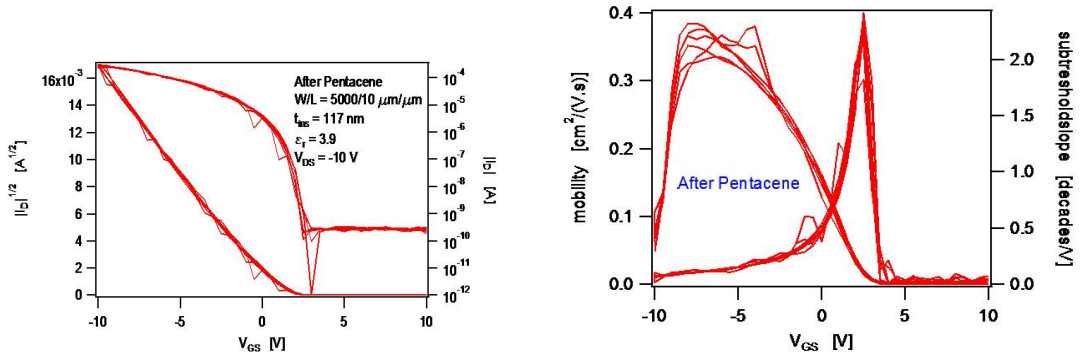
In our processing Parylene has been deposited at a pressure of few millibar. The powder has been first vaporized at 135℃ and then cracked into monomer

units at 690℃ in the pyrolysis part of the tool. Subsequently, the stable monomer then enters the deposition chamber polymerizes onto the substrate. As the coating is formed at room temperature, stresses related to differential thermal expansion are avoided. As mentioned before, film thickness is strictly determined by the amount of dimer used. The Parylene deposition system that has been used in this study is integrated in a nitrogen filled glow-box, allowing the loading of the devices that need to be coated, without any exposure to moisture or humidity. The resulting coating film is able to resist against chemical attack from organic solvents, inorganic reagents and acids [96].

6.3 Stability test on encapsulated OTFTs

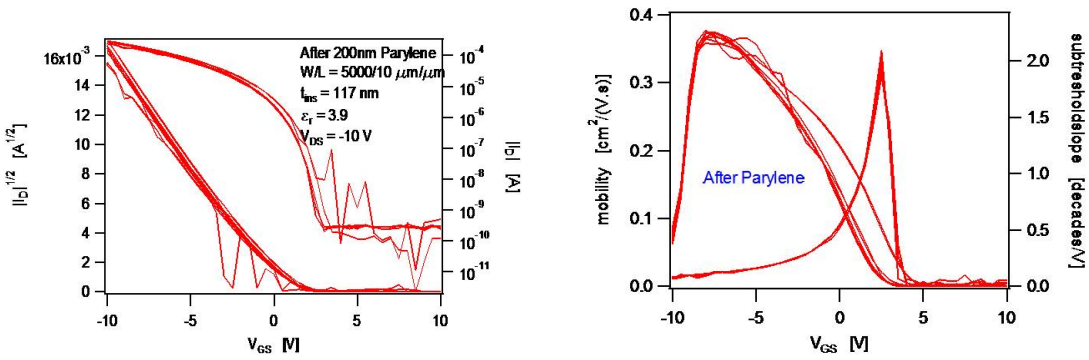
The aim of this study was to verified the goodness of the use of the polymer Parylene as encapsulant for organic devices. Partial results have been already published in literature, where the use of a Parylene passivation layer showed not to affect FET device performance [97]. Moreover, we were also interested in understanding if a thin layer of Parylene-C could be a good barrier against solvents and basic solutions. Within the European project *Flame*, we have collaborated in the development of a flexible OLED display with integrated OTFTs active matrix. Such a complex project implies more than 10 photo lithographic steps, and multiples technological challenges need to be overcome. Within this project, we studied if it was possible to process a photolitho step upon a Parylene layer. As mentioned before we have tested standard bottom contact OTFTs, on Si-SiO_2 samples, with gold contacts pads and with a final semiconductor Pentacene layer of 30nm (see fig. 6.1). A rough patterning of the semiconductor was done directly by using the probe needle in order not to lower the leakage currents and improve the I_{ON}/I_{OFF} current ratio. A photolithographic patterning of the semiconductor should have been possible by using a water soluble resist and by performing an O_2 plasma etching. Nevertheless we preferred to opt for manual patterning in order not to expose the samples to air and moisture after the Pentacene evaporation.

In these experiments we have worked with 1.5cm·1.5cm samples. All the samples have been diced from a quarter of a 6-inch wafer processed until the patterning of the gold contact structures. This way of working ensures a huge reduction of processing time and a good uniformity of the samples. Before Pentacene evaporation the diced samples have been subjected to surface treatment (see App. B). Our photolitho masks are designed in order to obtain diced samples with more than 50 OTFTs with interdigitate source-drain structure at different channel lengths (from 2 to 10μm). For simplicity we have decided to work with OTFTs with a relative width of 5000 and a channel length of 10μm. Fig. 6.4 shows the data about the first sample measured after the 30nm Pentacene evaporation. In the left we have reported the transfer curve, measured in saturation conditions ($V_{ds} = -10V$), while in the right we have the extracted mobility and the subthreshold slope as a function of the V_{gs} voltage. The graphs show OTFTs with total good electrical characteristics with maximum mobility between 0.3 and 0.4 $cm^2/(Vs)$, and a threshold voltage of few volts.



(a) (b)

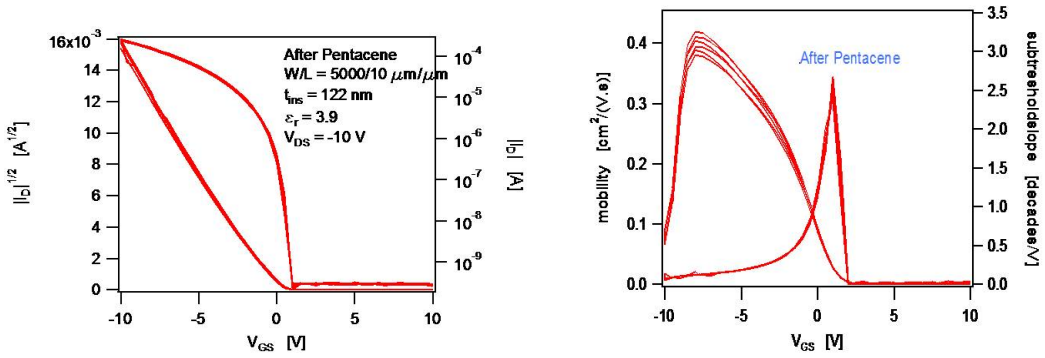
Figure 6.4: (a) Transfer curves after Pentacene evaporation. (b) Mobility and subthreshold slope curves after Pentacene evaporation.



(a) (b)

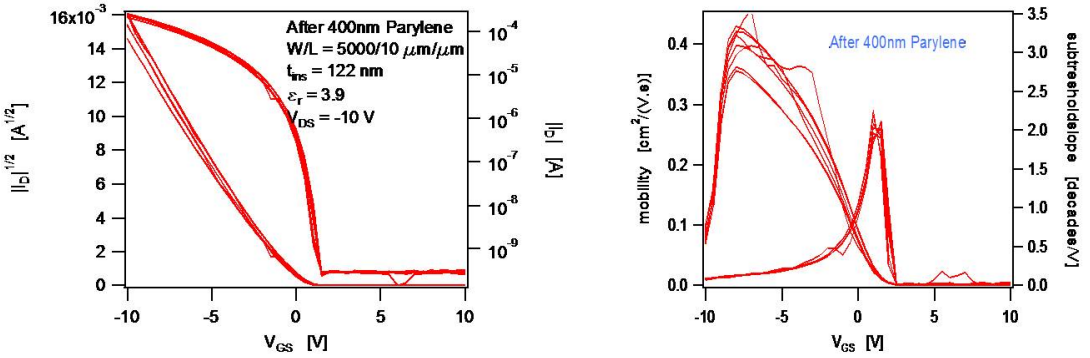
Figure 6.5: (a) Transfer curves and (b) mobility and subthreshold slope curves after coating with 200nm of Parylene-C.

After the first measurements, this sample has been coated with 200nm of Parylene-C, and the selected transistor have been remeasured. The Parylene has not been patterned because the layer was thin enough for allowing the penetration through it by using the probe needle. The curves reported in Fig. 6.5, show that no significant variations incurred. The experiment has been repeated by considering a new OTFTs sample (measurements after Pentacene evaporation in Fig. 6.6) coated with 400nm of Parylene-C. Fig. 6.7 again shows that no degradation or modification of the OTFTs characteristics takes place during the processing of coating with this polymer.



(a) (b)

Figure 6.6: (a) Transfer curves and (b) mobility and subthreshold slope curves before Parylene coating.



(a) (b)

Figure 6.7: (a) Transfer curve and (b) mobility and subthreshold slope curves of OTFTs coated with 400nm Parylene.

The measurements has been repeated after exposure to air for different times, without revealing any kind of degradation that is usually immediate if the sample is exposed to air with no Parylene encapsulation. These results are in agreement with what shown in literature [92]. As over mentioned we were interested in testing the permeability of this polymer against solvents and basic solutions. For achieving this goal we have performed a rough test by dipping OTFTs samples coated with 400nm of Parylene-C in 3 different test liquids for 60s. Afterwards the samples have been dried with nitrogen gas and remeasured. The test liquids that we have chosen are: the solvent PGMEA (2-[1-methoxy]propyl acetate), the

solvent NMP (N-Methyl-2-pyrrolidone), and the developer OPD5262. Reference samples have been also used to monitor the influence of air exposure during the experiments.

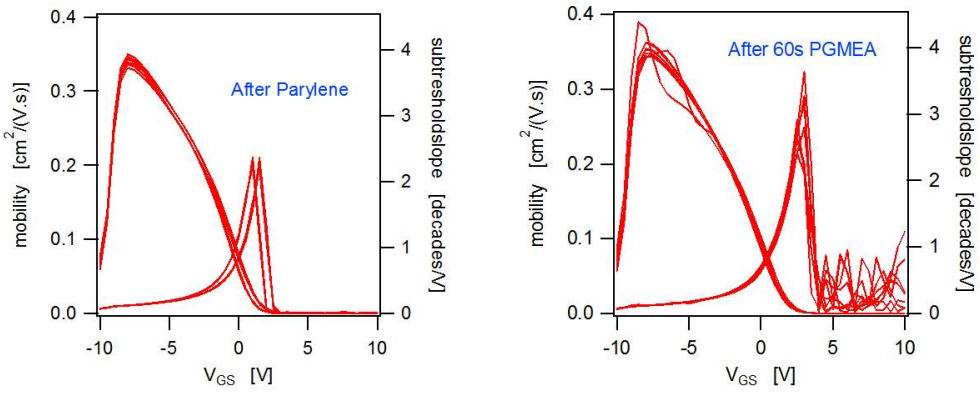


Figure 6.8: Mobility and subthreshold slope curves of OTFTs encapsulated with 400nm of Parylene-C, before (a) and after(b) immersion for 60s in PGMEA

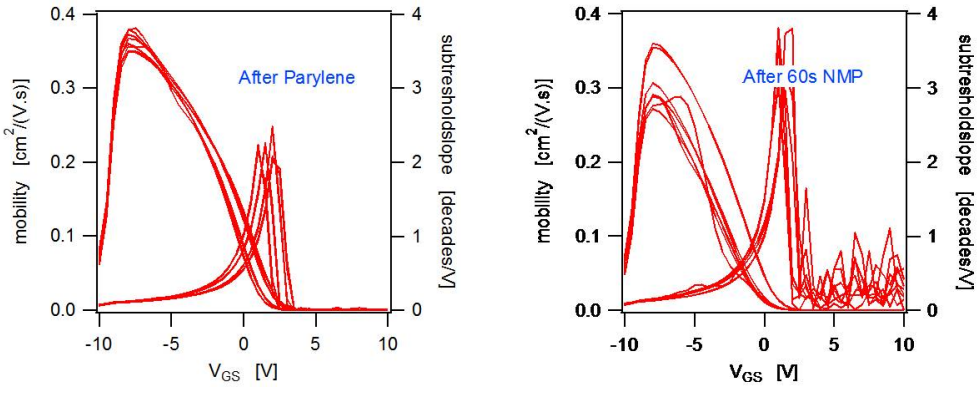


Figure 6.9: Mobility and subthreshold slope curves of OTFTs encapsulated with 400nm of Parylene-C, before (a) and after(b) immersion for 60s in NMP

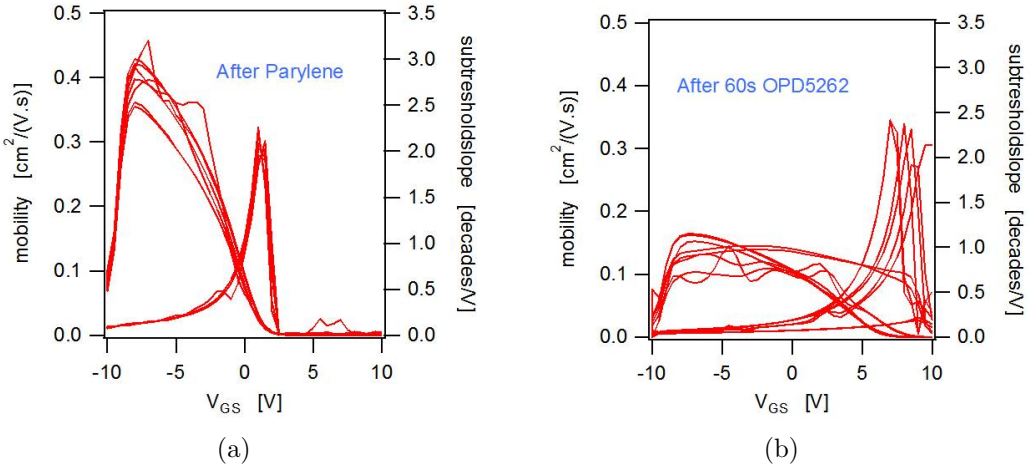


Figure 6.10: Mobility and subthreshold slope curves of OTFTs encapsulated with 400nm of Parylene-C, before (a) and after(b) immersion for 60s in the developer OPD5262

In Fig. 6.8, 6.9, 6.10 we compare the mobilities and subthreshold slopes of the OTFTs subjected to the experiments, before and after the immersion for 1 minute in the three liquids, PGMEA, NMP and OPD5262. For immersion in PGMEA we have no significant variations of the curves, proving a good permeability of the material to this solvent. For the sample dipped in NMP we have a variation of the curves with a mobility decrease in some of the measured devices of about 20%. Finally, in the case of the immersion of the sample in OPD6252, fig. 6.10 indicates a strong degradation of the devices, with a more of 50% decrease of the mobility and a general shift of the threshold voltage of several volts. Moreover we have observed that if we tried to anneal the degraded sample at 140℃ for 20 hours we have an opposite shift of the curves that roughly come back to the previous point, but no recovery of the mobilities. These results demonstrate that the coating with Parylene-C does not negatively affect the performance of the OTFTs. Moreover, such coating is able to protect the devices from contact to air and moisture. A preliminary study has shown that even a thin layer of this material (400nm) seems to act as a discrete barrier for solvents but not for the developer OPD5262. This fact partially limits the possibility to perform further photolitho steps upon the Parylene layer. At the same time we have to notice that in our experiments we have subjected the samples to extreme conditions, and that processing wisdoms can be developed in order to reduce the impact of this developer in a photolitho step.

Chapter 7

Conclusions

By performing an optical analysis on Alq3-based OLEDs, we have observed uneven light emission distribution. In particular we have analysed the light emission profiles that showed an higher light intensity in the centre of the active area (as reported in chapter 2). The change of the light emission distribution has been monitored during accelerated electrical stress. These data have been completed with the results of a thermal analysis on temperature surface distribution upon the active area. Thermal IR images revealed that surface temperature along the active area has its maximum on the centre, and it decreases moving toward the edges. As shown in chapter 4.2, the optical and thermal behaviour of these devices are strictly correlated. The two phenomena have been explained by assuming that: the first effect is the creation of the radial thermal distribution, due to a worse capacity of dissipating heat in the centre of the active area, compared to the edges; subsequently the temperature difference creates an uneven current distribution that is greater where the resistivity of the material is lower, i.e. the warmer centre of the device; the thickening of the current increases the local temperature, producing a positive feedback limited only by the exchange of heat with the environment. Such uneven uniformity of the light emission causes an uneven optical degradation during working operation.

In chapter 3 we have presented a work about the investigation of the reliability of small molecules OLEDs, with simplified structures, consisting of NPD as hole transport layer, Alq3 as electron transport layer, and an hole injection layer between NPD and ITO electrode. The results of this study can be summarized in the following:

- The optical power emitted by the OLEDs showed a remarkable decrease during constant current stress, showing a 50% TTF of about 1270 hours with neither catastrophic breakdown nor the formation of dark spots.

- From the emission microscopy images, taken before and after stress, we have observed a much stronger degradation of the luminescence in the center of the device, with respect to the corners/borders. These results are compatible with a significant current and emission crowding that may determine also a stronger self-heating near the centre of the device area.

- The changes of the electrical characteristics are correlated with the optical degradation. The nature of this degradation has been studied by a combined analysis of the J-V and C-V curve evolution during stress.
- The device degradation mechanisms can be tentatively explained by assuming that the constant current stress produces both a fixed interface (positive) trapped charge and a number of neutral interface states, likely correlated with the oxidation of the Alq3.
- A rough estimation of the fixed trapped charge shows a good linear relation between the stress time and the amount of this trapped charge.

Our studies on phosphorescent OLEDs stressed at different current levels, show an increase of the operating voltage univocally correlated with the number of carriers injected in the devices during the stress. Also in this typology of devices we have detect the current crowding phenomenon over mentioned, even if less prominent. A time to failure law have been calculated for these devices.

As reported in section 4.3, we have studied the use of IZO in place of ITO as anode layer in OLEDs. Our results indicate that the use of IZO anodes guarantees OLED performance comparable with commercial ITO anodes, and allows an improved heat dissipation and devices reliability. We have correlated this improvement in the OLED reliability with the thermal properties of the device rather than with the ITO and IZO morphological properties. OLEDs with IZO as anode contact show a lower thermal resistance, and this positively affects the optical stability of the devices.

The second part of my work is related to the technological development of both bottom and top contact OTFTs. By working in collaboration with the European microelectronic research centre *IMEC*, we have manufactured innovative photo-lithographic patterned top contact OTFTs. By using a wet etching process, we have realized top contact OTFTs with 10μm channel length, obtaining mobilities greater than $0.5cm^2/(Vs)$. Moreover, we have developed an innovative process flow that allows the patterning of Silver source-drain contacts on the top of the organic semiconductor, by using plasma dry etching. The process flow has been proved on silicon, as well as on foil substrate.

Appendix A

Evaluation of the thermal resistance

A parameter that is usually considered for optoelectronic devices thermal study is the junction thermal resistance (R_{th}). This parameter gives informations about the operative temperature of the device and its capacity to exchange heat. Knowing the R_{th} and the power dissipated by the device, it is possible to calculate the junction temperature (T_j) of the device. The operative temperature of the device is usually strictly related to its lifetime and also to the optical and electrical degradation mechanisms. The thermal resistance can be a good reference parameter for comparing devices with different materials or structures, providing precious indications for technology design and developing. Knowing the working junction temperature of an OLED, it is possible to plan an experiment where the devices are subjected only to thermal stress, at that specific temperature. In this way it is possible to investigate separately the influence of temperature and current density on the degradation kinetics. Moreover, if a device is stress at a certain current, knowing the R_{th} we know the temperature reached by the device during the electrical stress. Typically, electrical stress test are performed in conditions that are highly worse than standard condition. This is done in order to induce an accelerate degradation, and allow the study of the lifetime of the device in a reasonable time. If this done at different accelerated stress conditions, then it is possible to estimate the real lifetime of the device. Therefore, for studying OLEDs degradation a current that is many times the nominal current is typically used. Unfortunately, this implies that the temperature reached by the junction of the device can be much higher than the one reached in standard bias conditions. This temperature stress can introduce new degradation mechanism that are not actually related with the normal working of the device. Knowing in advance the value of this temperature is therefore essential for studying the degradation and the failure mechanisms of the device.

In the following we will explain a method for evaluating the junction thermal resistance. This method refers to calculation of thermal junction resistance of inorganic Gallium Nitride (GaN) LEDs, otherwise we have verified the possibility of applying this method also to OLEDs. The method consists in two phases: a *calibration phase* and a *temperature evaluation phase*.

Calibration phase

During this first phase, it is measured the relation between the voltage drop across the device at a certain current bias condition and the junction temperature. This is realized by putting the device under test in a thermal chamber at a certain temperature T*. Then the voltage drop across the OLED is measured by applying a short current pulse. The shortness of this pulse allows for avoiding self-heating of the device. In this condition we can assume that the temperature of the thermal chamber is the junction temperature. It is therefore possible to plot the voltage drop as a function of the junction temperature by repeating the measurement for different T*. This relation can be usually fitted by a linear or exponential function. For sake of simplicity lets assume to have a linear relation (similar simple calculations can be done in the case of an exponential dependency):

$$V_f = A + BT_J \tag{A.0.1}$$

where V_f is the voltage drop across the device, T_J is the oven temperature and A and B are fitting parameters.

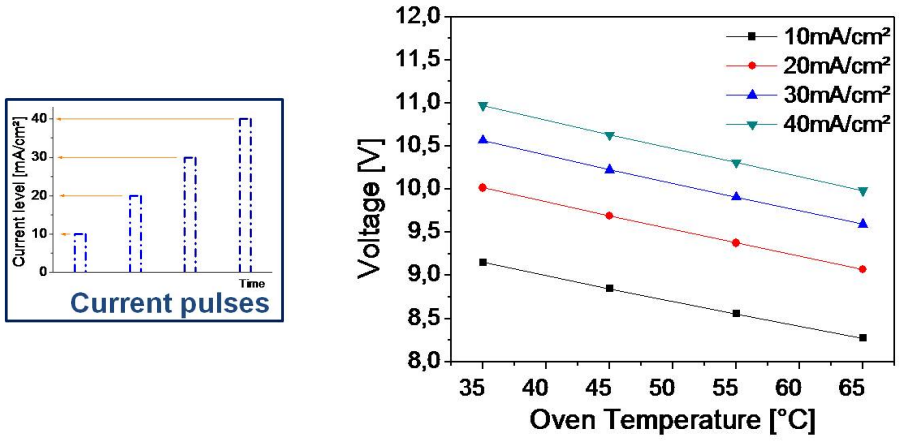


Figure A.1: Voltage mapping for estimating junction thermal resistance.

Temperature evaluation phase

After the first phase, the device is kept at a fixed temperature T_O and it is biased at a constant current density J_{BIAS} measuring the voltage transient. When the device reaches a stable electrical condition, it is possible to use that voltage value for obtaining the junction temperature. The voltage reached by the OLED is substituted in equation A.0.1 and the equation is solved respect to T_J, revealing the junction temperature reached by the device. By subtracting T_O to this value we can determine the temperature increase ($\triangle T$) and dividing for the power dissipated (P_{diss}) we can finally extract the thermal resistance value R_{th}:

$$R_{th} = \frac{\triangle T}{P_{diss}} \tag{A.0.2}$$

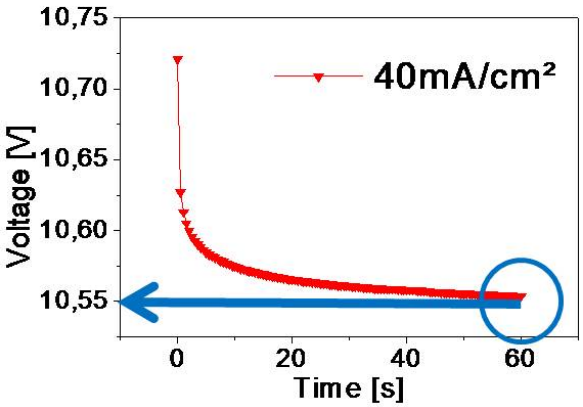


Figure A.2: Voltage transient used for extrapolating the junction thermal resistance.

Appendix B

Surface Treatment

This appendix gives an overview of the use of a surface treatment before the evaporation of the Pentacene (see App. C). In order to optimize the growth of the organic semiconductor, it is possible to change the surface energy of the interface, and so to control the interaction of the first semiconductor monolayer with the substrate. Moreover such a surface treatment can passivate dangling bonds and traps and therefore improve mobility, threshold and onset voltage of the final transistor [98].

The first step is a cleaning step where the sample is treated with acetone, isopropanol alcohol. The cleaning step is completed with a UV-O_3 treatment of about 15 minutes. This extensive cleaning removes most of the organic contaminants that may still be present at the surface. At this point the samples can be dipped in a 1-dodecanethiol solution (structural formula shown in figure B.1) for about half an hour. In this way we have the creation of a SAM (Self Assembled Monolayer) upon the gold . SAMs have a head which selectively attaches to a surface and a tail that finally establishes the surface properties of the interface covered with the SAM. Immediately, after the thiol treatment, the sample is transferred inside a vacuum oven that has been specifically designed with a inner metal chamber. The samples remain inside this chamber for about 1 hour together with few drops (30μl) of OTS (Octadecyl Trichloro Silane, structural formula shown in figure B.1) at a temperature of 60℃. In the chamber there is a saturated atmosphere that allows the creation of a silane SAM upon the SiO_2. Now the treated surface of the sample allows a good growth of the organic semiconductor.

Another technique that has been used for surface treatment it is the coating with a polymer layer. As reported in literature [99, 100], we have used a thin spin coated layer of $P\alpha MS$ (poly alpha-methyl styrene, structural formula shown in Fig. B.2). This surface treatment can be used in place of the silane treatment.

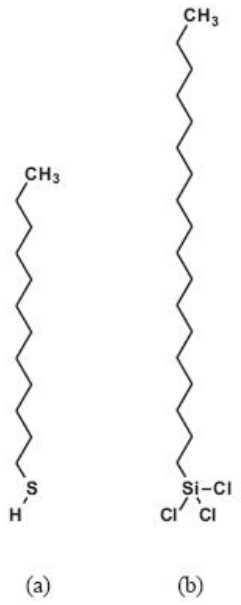


Figure B.1: The structural formula of (a) 1-dodecanethiol and (b) octadecyl trichlorosilane (OTS).

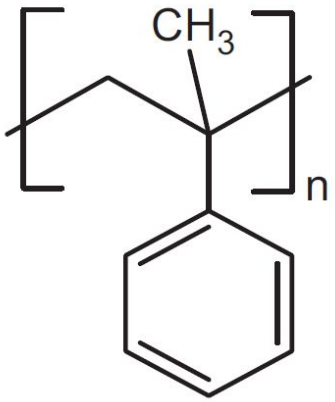


Figure B.2: PαMS structural formula.

Appendix C

Organic Molecular Beam Deposition

OMBD is a technique to deposit organic small molecules. The deposition takes place in a chamber in ultra high vacuum conditions (pressure lower than $10^{-}8$ torr). Such a high vacuum lowers the probability to have reaction between the organic semiconductor and gases or moisture that are present inside the evaporation chamber. The material is loaded in a crucible of a Knudsen cell and heated up. The beam of the sublimated material is directed towards the substrate where the deposition is desired. The vacuum decreases the temperature needed to reach the sublimation point of the organic semiconductor and increases the mean free path of the evaporated material. The resulting mean free path is thousand times greater than the crucible-substrate distance, an this ensures that there is negligible deflection of the evaporated beam. The goodness of the growth of the organic semiconductor layer is influenced by the substrate temperature and by the deposition rate that can be usually tuned by varying the temperature of the crucible of the Knudsen cell (typical values are few tenths of Angstroms per second). A surface treatment of the substrate by using self-assembling monolayers can be also necessary (for details see App. B). The deposition rate is measured by a water-cooled calibrated quartz crystal contained inside the chamber. Typical values that have been used are 0.25 Å/s for the deposition rate and 68℃ for the substrate temperature.

The evaporation tool used to process the samples studied in this work contains several Knudsen Cell in order to give the opportunity to evaporate different metals and organic materials. It is connected to a nitrogen-filled glove-box where the samples can be stored and measured. Moreover, a Parylene coater is integrated inside the glove-box allowing (in the case of bottom contact OTFTs), the direct encapsulation of the devices just after the evaporation of the organic semiconductor, and avoiding exposure to the gases and moisture present in the air.

In the following I will list the basic step for performing a Pentacene evaporation in a OMBD system:

1. Loading of the sample from the N_2 metal glove box into the load lock.

2. Pumping down of the load lock to a pressure lower than 10^{-7} torr.

3. Transportation of the sample inside the evaporation chamber by using a metal arm. The complete transfer process is performed in ultra-high vacuum conditions and the flux path from the Knudsen cell to the sample is interrupted by a shutter.

4. The temperature of the Pentacene cell is increased until a deposition rate of 0.25 Å/s is reached and the substrate holder is usually heat up to 68℃.

5. When a stable molecular flux is obtained, the shutter is opened.

6. The shutter is closed when the desired thickness of material is deposited upon the sample. The thickness is calculated by using the data gathered by the quartz crystal.

7. The sample is unload into the load lock by using the metal arm.

8. The pressure of the load lock is raised up to 1 atm.

9. The sample is unload in to the N_2 metal glove box.

Although OMBD is a well-suited technology for depositing small molecule organic semiconductors at a research level, it cannot be the best choice from the point of view of large scale, industrial processing facilities due to the necessity of expensive and not versatile ultra-high equipment. Another method exists to deposit Pentacene films in low vacuum or even atmospheric conditions, the Organic Vapour Phase Deposition (OVPD).

Appendix D

Spin Coating Process Description

Spin coating has been used for several decades for the application of thin films. The complete process consists of a dispense stage in which a fluid is deposited onto the substrate surface by using a pipette, an acceleration stage that spreads the liquid removing the exceeding part of it, a high speed spin stage to thin the fluid, and a drying stage to eliminate excess solvents from the resulting film (usually performed by using an hot plate or an oven). The time and rotation speed determines final coating thickness.

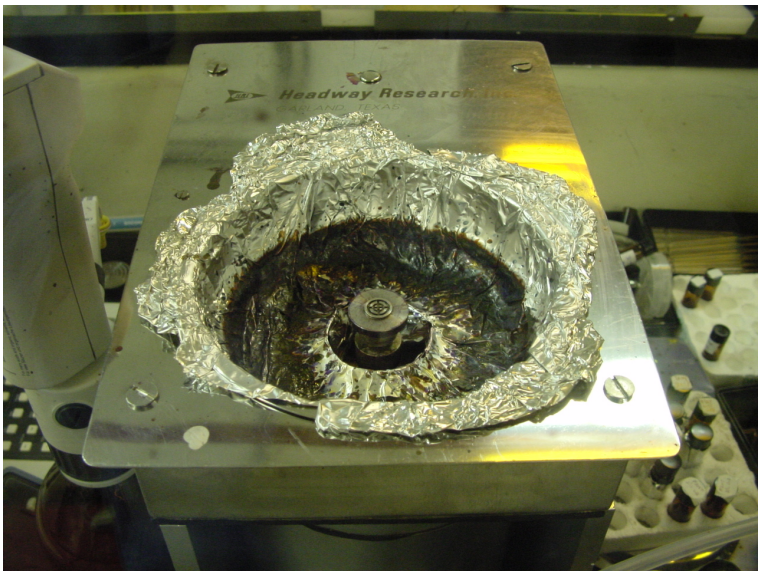


Figure D.1: The Spin Coater with interchangeable support.

D.1 Spin Coating Stages.

As over mentioned, in the *first stage* the deposition of the coating fluid onto the substrate is done by using a pipette that pours the coating solution out. Usually this dispense stage provides a substantial excess of coating solution, compared to the amount that will ultimately be required in the final coating thickness,

resulting in a big quantity of wasted liquid. The coating liquid has to not to contain bubbles that may degrade the spin coating.

In the *second stage* the substrate is accelerated up to its final, desired, rotational speed. This stage is usually characterized by fluid expulsion from the wafer surface by the rotational chuck. Owing to the initial height of fluid on the wafer surface, spiral vortices may briefly be present.

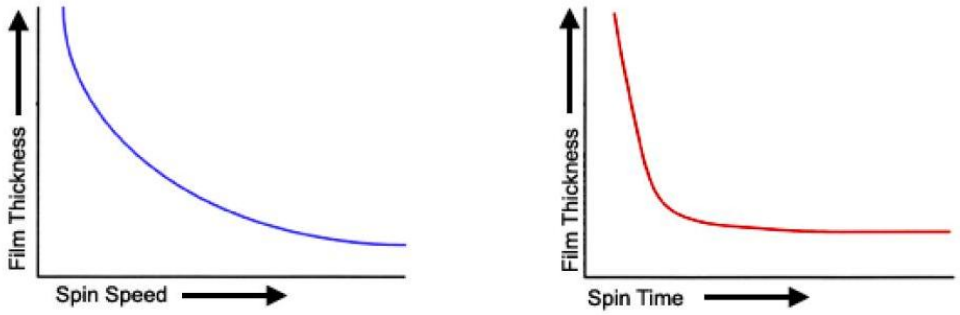


Figure D.2: Typical Film Thickness vs Spin Speed and Film Thickness vs Spin Time characteristics.

The *third stage* is when the substrate is spinning at a constant rate and fluid viscous forces dominate fluid thinning behaviour. The time of the spinning depends on the wanted thickness, as you can see in Figure D.2. This stage is characterized by gradual fluid thinning. Edge effects are often present because the fluid flows uniformly outwards, but when it finds the edges it creates droplets that flung out. Thus, depending on the surface tension, viscosity, rotation rate there may be a difference in thickness around the edge of the coated sample.

The *fourth stage* is when the substrate is spinning at a constant rate and solvent evaporation dominates the coating thinning behaviour. As the prior stage advances, the fluid thickness reaches a point where the viscosity effects yield only rather minor net fluid flow. During this stage the coating reaches its final thickness.

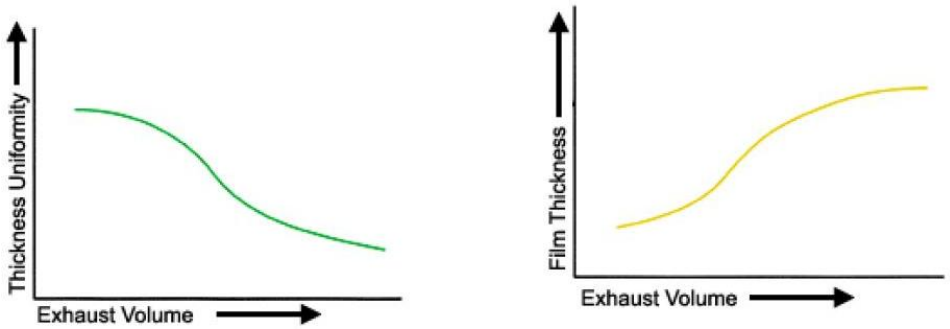


Figure D.3: Typical Thickness Uniformity vs Exhaust Volume and Film Thickness vs Exhaust Volume characteristics.

D.2 Static Distribution, Dynamic Distribution

Two common methods of dispense are Static Distribution and Dynamic Distribution. Static distribution is simply the depositing of a small puddle of fluid on or near the centre of the substrate. This quantity can vary depending on the viscosity of the fluid and the size of the substrate to be coated. Higher viscosity and/or larger substrates typically require a larger puddle to ensure full coverage of the substrate during the high speed spin step. Dynamic dispense is the process of dispensing while the substrate is turning at low speed. A speed of about 500 rpm is commonly used during this step of the process. This serves to spread the fluid over the substrate and can result in less waste of material since it is usually not necessary to deposit as much to wet the entire surface of the substrate. This is a particularly advantageous method when the fluid or substrate itself has poor wetting abilities and can eliminate voids that may otherwise form.

After the dispense step it is common to accelerate to a relatively high speed to thin the fluid to near its final desired thickness. Typical spin speeds for this step range from 1500-6000 rpm, again depending on the properties of the fluid as well as the substrate. This step can take from 10 seconds to several minutes. The combination of spin speed and time selected for this step will generally define the final film thickness. In general, higher spin speeds and longer spin times create thinner films. The spin coating process involves a large number of variables that tend to cancel and average out during the spin process so it is best to allow sufficient time for this to occur.

D.3 Spin Speed

Spin speed is one of the most important factors in spin coating. The speed of the substrate (rpm) affects the degree of radial (centrifugal) force applied to the liquid resin as well as the velocity and characteristic turbulence of the air immediately above it. In particular, the high speed spin stage generally defines the final film thickness. Relatively minor variations of ± 50 rpm at this stage can cause a resulting thickness change of 10%.

Film thickness is largely a balance between the force applied to shear the fluid resin towards the edge of the substrate and the drying rate which affects the viscosity of the liquid. As the liquid dries, the viscosity increases until the radial force of the spin process can no longer appreciably move the liquid over the surface. At this point, the film thickness will not decrease significantly increasing the spin time.

D.4 Acceleration

The acceleration of the substrate towards the final spin speed can also affect the coated film properties. Since the liquid begins to dry during the first part of the

spin cycle, it is important to accurately control acceleration. In some processes, 50% of the solvents in the resin will be lost to evaporation in the first few seconds of the process.

Acceleration also plays a large role in the coat properties of patterned substrates. In many cases the substrate will retain topographical features from previous processes; it is therefore important to uniformly coat the liquid over and through these features. While the spin process in general provides a radial (outward) force to the liquid, it is the acceleration that provides a twisting force. This twisting aids in the dispersal of the liquid around topography that might otherwise shadow portions of the substrate from the fluid.

D.5 Fume Exhaust

The drying rate of the fluid during the spin process is defined by the nature of the fluid itself (volatility of the solvent systems used) as well as by the air surrounding the substrate during the spin process. It is well known that such factors as air temperature and humidity play a large role in determining coated film properties. It is also very important that the airflow and associated turbulence above the substrate itself be minimized, or at least held constant, during the spin process.

The slower rate of drying offers the advantage of increased film thickness uniformity across the substrates. The fluid dries out as it moves toward the edge of the substrate during the spin process. This can lead to radial thickness non-uniformities since the fluid viscosity changes with distance from the centre of the substrate. By slowing the rate of drying, it is possible for the viscosity to remain more constant across the substrate.

Drying rate and hence final film thickness is also affected by centre ambient humidity. Variations of only a few percent relative humidity can result in large changes in film thickness. By spinning in a closed bowl the vapours of the solvents in the resin itself are retained in the bowl environment and tend to overshadow the affects of minor humidity variations.

Appendix E

MA6 mask aligner

The SUSS MA6 Mask Aligner allows the usual top-side alignment and the less common bottom-side alignment for accurate backside processes. For our processing we used top-side alignment. The system provides a dual video microscope. The user is able to set the gap between the resit and the mask, the time of the exposure, the kind of exposure (hard contact, soft contact, flood exposure, exposure with cycles, etc). For our samples we used a hard contact exposure; after the wafer has moved into contact, the vacuum underneath the wafer is switched off and nitrogen is purged under the wafer. So a closer contact between wafer and mask is guaranteed, even with large wafers.
The system can work with samples of different sizes (3,5 and 6 inch), indeed that is for the masks (7″x7″, 5″x5″, 4″x4″). The MA6 tool is capable of printing resist thicknesses from less than 0.1 μm to a few hundred micron and a resolution of less than 0.1μm.

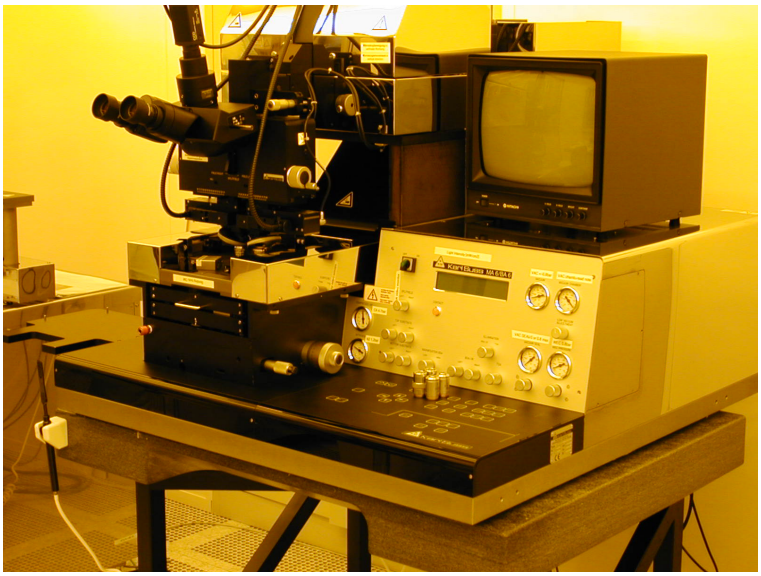


Figure E.1: Mask Aligner MA6.

Appendix F

Parylene Deposition System

Parylene, or poly-p-xylylene, is an organic polymer. Several varieties of Parylene exist, including Parylene-N, Parylene-C, Parylene-D, Parylene-SR. Parylene is merely considered a coating material but it can be also used as dielectric. Parylene-N and Parylene-SR provide particularly high dielectric strength and a dielectric constant that is independent of frequency. The dielectric constant determines the capacitance: a higher dielectric constant results in higher capacitance and higher electric field at the surface of the dielectric. Type N deposits at the rate of approximately 0.75μm per hour. Type C is less conformal than N, but deposits at a much higher rate, of about 5μm per hour. For the processes concerning this work I have used Parylene-C.

Some desirable properties of the polymer Parylene (poly-para-xylylene) are:

- Biocompatibility
- Truly conformal material (pin-hole free at 25 nm thickness)
- Thin film dielectric
- Excellent moisture/chemical barrier properties
- High mechanical strength

In this appendix I will give some detail about the deposition processing (coating) of this polymer. A good adhesion of Parylene to a wide variety of substrates can be achieved by treating the surface of the samples with a dilute solution of an organic silane prior to Parylene coating, that turns the treated surfaces to be hydrophobic. The Parylene deposition process consists of three basic steps, all done in the presence of vacuum: sublimation, pyrolysis, polymerization. Sublimation consists of heating solid Parylene dimer (di-para-xylylene) until it sublimates into the gaseous state. In our system that has been done at a temperature of 135℃. Pyrolysis consists of heating and cleaving of the gaseous Parylene dimer into a monomer (para-xylylene). In our system that has been done at a temperature of 690℃. Subsequentely, during the polymerization, the gas enters in the load chamber and polymerize onto the substrate at room temperature, forming a

transparent film. The pressure gradient across the three zones drives the parylene deposition process. The coating grows as a conformal film (poly-para-xylylene) on all exposed substrate surfaces, edges and in crevices. The thickness of the coating depends on the amount of dimer placed in the load material chamber and on the temperature of sublimation.

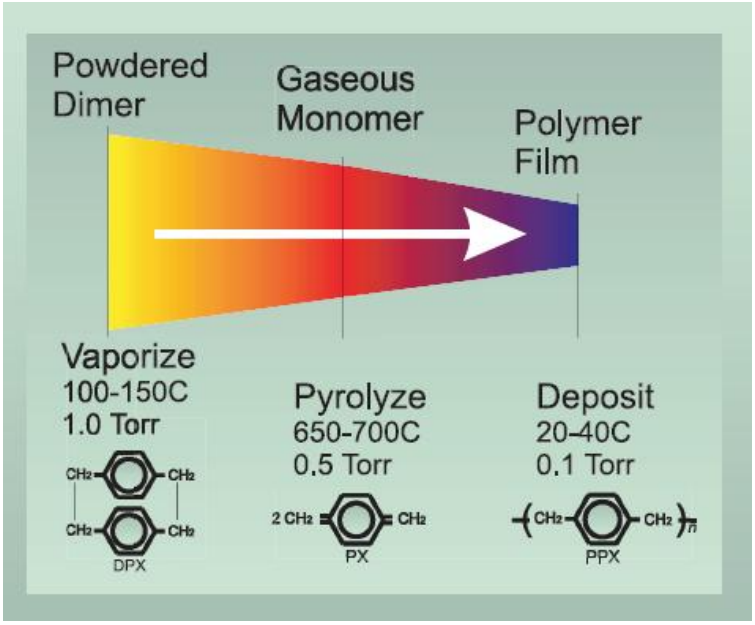


Figure F.1: Parylene Deposition Process.

The Parylene system that we have used consist of tubes and chambers that enable the Parylene deposition process to occur. The five main components of the system are:

- Vaporizer - This heats the Parylene dimer until it sublimates (vaporizes).
- Pyrolysis Furnace - This further heats and cleaves the gaseous Parylene dimer into monomer form.
- Deposition Chamber - This is the chamber where the Parylene is deposited as a polymer onto the substrate. In our system it is integrated in a nitrogen-filled glove box, allowing the loading and unloading of the samples without exposure to air.
- Cold Trap - This is a cryogenic device that uses liquid nitrogen to cool a steel cylinder. The chilled cylinder then condenses Parylene process by-products and prevents any contamination or break of the vacuum pump.
- Vacuum Pump - This maintains vacuum to the system.

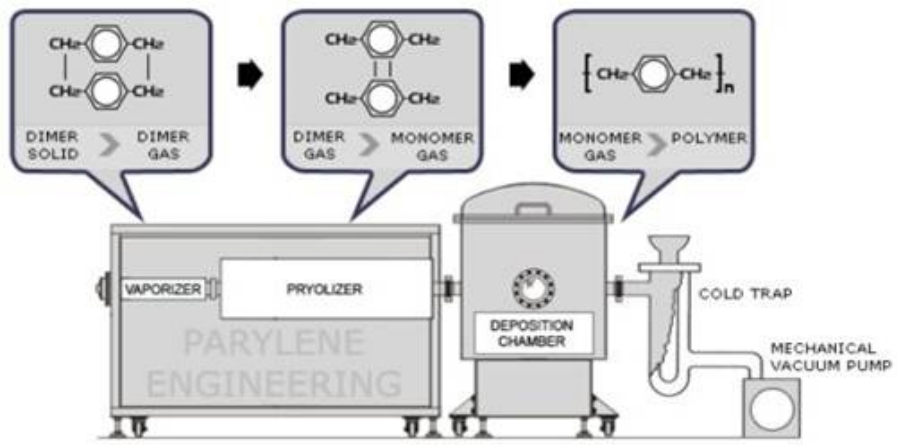


Figure F.2: Parylene coating system (Source: http://typexycoating.com).

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