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Ciclo XX

ANALYSIS AND DESIGN OF A NOTCH FILTER FOR THE REJECTION OF INTERFERENCE IN UWB SYSTEMS AND ITS APPLICATION TO A 0.13-μm CMOS RECEIVER FRONT-END

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Abstract

This work reports the analysis and the design of a 0.13-μm CMOS fourth-order notch filter for the rejection of the 5–6 GHz interference in UWB front-ends. The filter is integrated into an analog front-end for Mode #1 UWB systems, i.e. operating in the 3.1–4.8 GHz frequency range. A thorough analysis based on a simplified model of the filter is carried out. An algorithm for the automatic tuning and calibration of the filter is also discussed and demonstrated. Two versions of the circuit are designed and fabricated: the first comprises a low-noise amplifier (LNA) and the filter, the second expands it to a complete front-end. In the latter version the filter was also redesigned. The filter provides more than 35 dB of attenuation and has a tuning range of 900 MHz, adding less than 30% power consumption to the LNA. The out-of-band IIP3 takes a 9-dB advantage from the filter and the compression of the gain due to the out-of-band blocker is reduced by at least 6 dB in the complete front-end.

Sommario

In questo lavoro sono riportate l'analisi e la progettazione di un filtro notch del quarto ordine per la reiezione dell'interferenza tra 5 e 6 GHz nei front-end per applicazioni UWB. Il filtro, realizzato in tecnologia CMOS da 0.13 μm, è stato integrato in un front-end analogico per sistemi UWB di tipo Mode #1, cioè funzionanti nella gamma di frequenze tra 3.1 e 4.8 GHz. Viene condotta una dettagliata analisi teorica del filtro, basata su un modello semplificato dello stesso, ed è altresì discusso e dimostrato un algoritmo per la sintonizzazione e calibrazione automatiche del filtro. Sono progettate due versioni del filtro: la prima comprende un amplificatore a basso rumore (LNA) ed il filtro, mentre la seconda espande la prima ad ottenere un front-end completo. Il filtro nella seconda versione subisce una leggera revisione. Il filtro fornisce più di 35 dB di attenuazione ed ha un intervallo di sintonizzazione di 900 MHz, aggiungendo meno del 30% al consumo di potenza del LNA. L'intermodulazione del terzo ordine IIP3 migliora di 9 dB grazie al filtro e la compressione del guadagno causata dall'interferenza fuori banda è ridotta di almeno 6 dB nel front-end completo.

Introduction

The release of the spectrum spanning from 3.1 to 10.6 GHz by the Federal Communications Committee (FCC) in 2002 [1] has started a vast effort to exploit the potentials of such a wide range of available frequencies and set off the development of Ultra-Wideband (UWB) systems. In particular, UWB systems are seen as a viable way to support short-range communications with data-rates up to 480 Mb/s using a multi-band OFDM signaling format [2]. With an average spectral density limit of -41.3 dBm/MHz, UWB systems are particularly subject to narrowband interference [3]–[8]. High power interferers such as wireless LANs (WLANs) in the 5-6 GHz spectrum may exceed the received UWB signal power by more than 60 dB, causing desensitization of the receive chain [7], [8]. These signals are also referred to as "blockers", because in their presence the desired signal may be no more detected by the receiver and are thus "blocked". The mentioned WLAN signals are particularly hard to deal with, because they are the closest to the UWB band and because another portion of the spectrum is available for UWB at higher frequency, so that a low pass filter is not applicable in a full-band system. Obtaining a high wide-band attenuation in the 5–6 GHz range without degrading the gain involves the use of many large passives with a high quality factor. With a reduced number of components, filtering can be achieved at the price of a decrease in the in-band gain because of the intrinsically low-sloped roll-off of these filters [5], [6]. In addition, the parasitic resistances associated to the passive components prevent a high attenuation, and an active compensation can improve it only at a single frequency [9]. A base-band filtering may also be performed [8], [10], but this does not address the problem of the saturation and gain desensitization of the receiver.

In this thesis, an interference rejection scheme based on a tunable narrowband notch filter, which can achieve a high attenuation with a reduced number of

passive components, is studied and realized. The basic idea is that, in the presence of many blockers, the largest one is mostly responsible for the deterioration of the linearity performance. Consequently, that one is the interferer that needs to be suppressed [11]. Moreover, as the notch filter operates on a small frequency range, it can take full advantage of a one-frequency compensation circuit and obtain a high attenuation at the notch frequency. In this way, employing a reduced number of components and causing a small degradation in the in-band gain, the notch filter shows a good trade-off between provided attenuation and power consumption. The major drawback of the narrow-band filtering is that it needs tuning, therefore a strategy for the automatic tuning and calibration of the filter is also proposed and demonstrated.

This work is developed in a two-step fashion using a standard 0.13-μm CMOS technology provided by Infineon Technologies AG. A first design was intended to study the behavior and the performance of the notch filter itself, and comprised a low-noise amplifier (LNA) and the filter [12]. A second design was made for the sake of verifying the impact of the filter on an entire front-end and demonstrating the tuning and calibration algorithm [13].

Chapter 1 of the thesis gives some basics on Radio-Frequency receivers and Ultra-Wideband systems. A high-level description of the architecture of a RF receiver will be given, focusing on the issues of input and noise matching. After introducing Ultra-Wideband systems, the design techniques will be extended to suite broad-band applications. Finally, the problem of the interference will be introduced.

RF building-blocks designs make large use of inductors to achieve high frequencies of operation. Chapter 2 gives an insight into the design of integrated inductors and their modeling. Three electromagnetic simulators will be briefly described and compared: ASITIC (developed at the Berkeley Wireless Research Center), ADS Momentum and Sonnet. In this work, six inductive structures were used, and each of them will be described in this chapter, along with the results from the EM simulations.

Chapter 3 is the core of this work. In this chapter the notch filter will be analyzed in depth and the type of network and the values of the components will be chosen so as to optimize the power consumption. An algorithm for the frequency tuning and current calibration will be studied and, on this basis, specifications

for additional circuits will be derived.

In Chapter 4, the design of the building blocks will be discussed. The LNA features a transformer-based input network, which will be described in detail. The design of the LNA and of the notch filter will be illustrated in both versions of the design, along with a brief discussion on the mixer (employed only in the second design). Then, a few words will be said on a digital system that controls the notch frequency and the bias current (basically, a serial-to-parallel converter) and the results from the simulations will be shown.

The results from the measurements are reported in Chapter 5. After a short discussion upon the measurement setup, the results of the small-signal tests will be shown and the linearity of the circuits will be assessed. Finally, some comments will be made on validating the proposed tuning and calibration algorithm.

Introduzione

La concessione dello spettro di frequenze da 3.1 a 10.6 GHz da parte del Federal Communications Committee (FCC) nel 2002 ha dato il via ad un notevole sforzo per sfruttare le potenzialità di una così ampia gamma di frequenze disponibili ed ha lanciato lo sviluppo di sistemi Ultra-Wideband (UWB). In particolare, i sistemi UWB sono visti come una strada praticabile per consentire comunicazioni a corto raggio con velocità di trasmissione fino a 480 Mb/s utilizzando una modulazione OFDM [2]. Avendo un limite di appena -41.3 dBm/MHz sulla densità spettrale media, però, i sistemi UWB sono particolarmente soggetti ad interferenze provenienti da sistemi a banda stretta [3]–[8]. Segnali interferenti di elevata potenza, come le reti wireless locali (WLAN) nello spettro tra 5 e 6 GHz, possono eccedere la potenza del segnale UWB ricevuto di più di 60 dB, causando una desensitizzazione della catena di ricezione [7], [8]. Questi segnali interferenti sono detti anche "blockers", poiché in loro presenza il segnale desiderato potrebbe non essere più rilevato dal ricevitore, risultando di conseguenza "bloccato". I segnali WLAN summenzionati sono particolarmente ardui da gestire perché sono i più vicini alla banda UWB e perché a frequenze più alte esistono altre frequenze disponibili per l'UWB, rendendo impraticabile la soluzione di un filtraggio passa-basso in un sistema che utilizzi l'intera banda. Ottenere un'elevata attenuazione a larga banda nello spettro fra 5 e 6 GHz senza degradare il guadagno in banda significa dover utilizzare molti componenti passivi con un alto fattore di qualità. Con un numero di componenti ridotto, il filtraggio può essere ottenuto al prezzo di una diminuzione del guadagno in banda a causa della pendenza intrinsecamente bassa del roll-off di questi filtri [5], [6]. In più, le resistenze parassite dei componenti passivi ne limitano l'attenuazione e una compensazione attiva la può migliorare solamente ad un'unica frequenza [9]. In alternativa, si potrebbe pensare di applicare un filtro in banda base [8], [10], ma

ciò non risolverebbe il problema della saturazione e della desensitizzazione del guadagno del ricevitore.

In questa tesi viene studiato e realizzato uno schema di reiezione dell'interferenza basato su un filtro notch a banda stretta sintonizzabile, il quale può raggiungere un'elevata attenuazione con un numero ridotto di componenti passivi. L'idea di base è che, in presenza di molti blocker, il più intenso è anche il maggior responsabile del deterioramento delle prestazioni di linearità. Di conseguenza, quello sarà l'interferente che deve essere soppresso [11]. Inoltre, siccome il filtro notch opera su una gamma ristretta di frequenze, può sfruttare appieno un circuito di compensazione a singola frequenza ed ottenere un'alta attenuazione alla frequenza del notch. In questo modo, impiegando un basso numero di componenti e causando solo un piccolo degrado nel guadagno in banda, il filtro notch appare un buon compromesso tra l'attenuazione fornita e la potenza consumata. La principale controindicazione del filtro a banda stretta è che ha bisogno di essere sintonizzato, quindi viene proposta e dimostrata anche una strategia per la sintonizzazione e la calibrazione automatiche.

Questo lavoro è stato sviluppato in due passi successivi utilizzando una tecnologia CMOS standard da 0.13 μm fornita da Infineon Technologies AG. Un primo design era inteso a studiare il comportamento e le prestazioni del filtro notch in sè, comprendendo un LNA ed il filtro [12]. Un secondo design è stato realizzato con lo scopo di verificare l'impatto del filtro su un intero front-end e di dimostrare l'algoritmo per la calibrazione e sintonizzazione automatiche [13].

Il Capitolo 1 della tesi fornisce alcune nozioni di base sui ricevitori a radiofrequenza (RF) e sui sistemi UWB. Verrà fornita una descrizione ad alto livello dell'architettura di un ricevitore RF, concentrandosi sulle problematiche dell'adattamento d'impedenza all'ingresso e sull'ottimizzazione del rumore. Dopo aver introdotto i sistemi UWB, le tecniche di design verranno estese alle applicazioni a banda larga. Infine verrà introdotto il problema dell'interferenza.

I blocchi circuitali utilizzati nei circuiti RF fanno largo uso di induttori per arrivare ad elevate frequenze di lavoro. Il Capitolo 2 fornisce un approfondimento sulla progettazione degli induttori integrati e sulla loro modellizzazione. Verranno brevemente descritti e confrontati tre simulatori elettromagnetici (EM): ASITIC (sviluppato al Berkeley Wireless Research Center), ADS Momentum e Sonnet. In questo lavoro sono state utilizzate sei strutture induttive, ciascuna delle quali

sarà descritta in questo capitolo insieme con i risultati delle simulazioni elettromagnetiche.

Il Capitolo 3 è il cuore di questo lavoro. In questo capitolo il filtro notch sarà analizzato in dettaglio e verranno scelti il tipo di rete da utilizzare ed i valori dei componenti che ottimizzano il consumo di potenza. Saranno studiati un algoritmo per la sintonizzazione in frequenza e la calibrazione in corrente e su queste basi verranno anche derivate delle specifiche per dei circuiti addizionali.

Nel Capitolo 4 si discuterà del design dei singoli blocchi circuitali. L'amplificatore a basso rumore prevede una rete d'ingresso basata su un trasformatore che sarà descritta in dettaglio. La progettazione del LNA e del filtro notch saranno illustrate per entrambe le versioni del circuito, assieme ad una breve discussione sul mixer (utilizzato solo nella seconda versione). Dopodiché verranno date alcune informazioni su un sistema digitale che controlla la frequenza del notch e la corrente di polarizzazione (si tratta, fondamentalmente, di un convertitore seriale-parallelo) e verranno mostrati i risultati delle simulazioni.

I risultati di misura sono riportati nel Capitolo 5. Dopo una breve discussione sul set-up della strumentazione, saranno mostrati i risultati dei test al piccolo segnale e verranno valutate le prestazioni in termini di linearità. Infine, verranno proposti alcuni commenti sulla validità dell'algoritmo di sintonizzazione e calibrazione che è stato proposto.

Chapter 1

UWB Radio-Frequency Receivers

Starting from galena radios of the early 20^{th} century, and coming up to the present days, the basic principles of radio-frequency (RF) receivers underwent very little changes, being basically made of a tuned filter and a demodulator. What is changed during these long years is the architecture of the receivers, which evolved in order to cope with the various problems that appeared during the development of the wireless communication technology.

1.1 Basic architectures of RF receivers

The two basic architectures are the homodyne and the heterodyne receivers, the former being a sort of a degenerated version of the latter.

Fig. 1.1 shows the basic scheme of a heterodyne receiver. First of all, the RF received signal is filtered and amplified, then, by means of a mixer, it is downconverted to an intermediate frequency (IF) and filtered again before being eventually demodulated to base-band. The first applications of radio transceivers were the transmission of audio signals, whose band goes from 20 Hz to 20 kHz. So, on the basis of this origin, the value of IF lets us make a distinction between heterodyne receivers: if IF is lower than 20 kHz, we have the actual heterodyne, while if IF is higher than 20 kHz, we call it super-heterodyne.

The homodyne receiver, whose block diagram is shown in Fig. 1.2, may be considered a degenerated case of heterodyne in which IF = 0 Hz. In this case, a single downconversion step is needed, and the signal is converted directly to

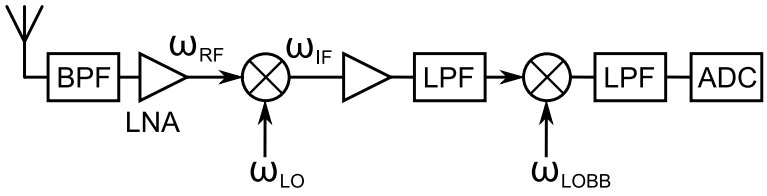


Figure 1.1: *Basic block diagram of a heterodyne receiver front-end.*

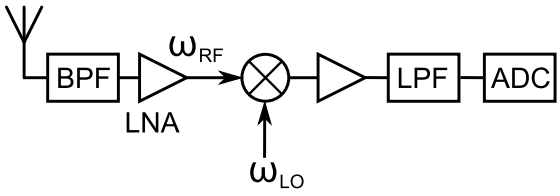


Figure 1.2: *Basic block diagram of a homodyne receiver front-end.*

base-band frequencies (for this reason, the homodyne receiver is also referred to as "direct conversion").

In heterodyne receivers [14], the received RF signal with center frequency ω_{RF} is mixed with a tone at frequency ω_{LO} generated by a local oscillator. The resulting signal will be equally split into two different bands, with center frequencies $\omega_{\mathrm{IF}} = \omega_{\mathrm{RF}} - \omega_{\mathrm{LO}}$ and $\omega_{\mathrm{HF}} = 2\omega_{\mathrm{RF}} - \omega_{\mathrm{LO}}$. Assuming that we are able to easy filter the ω_{HF} component, our signal will now be centered around ω_{IF}. However, ω_{RF} will not be the only frequency to be converted to ω_{IF}. The mixer performs the multiplication of the two signals $s_{\mathrm{RF}}(t) = A_{\mathrm{RF}} \cos \omega_{\mathrm{RF}} t$ and $s_{\mathrm{LO}}(t) = A_{\mathrm{LO}} \cos \omega_{\mathrm{LO}} t$. The low-pass filtered result of this operation is proportional to $\cos(\omega_{\mathrm{RF}} - \omega_{\mathrm{LO}})t$, which is not different from $\cos(\omega_{\mathrm{LO}} - \omega_{\mathrm{RF}})t$. This means that the signal at $\omega_{\mathrm{IM}} = 2\omega_{\mathrm{LO}} - \omega_{\mathrm{RF}} = \omega_{\mathrm{LO}} + \omega_{\mathrm{IF}}$, called "image signal", will also be converted to ω_{IF}. Fig. 1.3 illustrates this process. The problem of the image is not to be underestimated, as this signal can have a power much higher than that of the wanted signal. A straightforward way to get rid of the image signal is to use an image-rejection filter before the mixing stage. However, this poses some issues on the choice of ω_{IF}. The problem of filtering the image would suggest the choice of a large ω_{IF}, so that a bandpass filter can provide for a high attenuation at the frequency ω_{IM}.

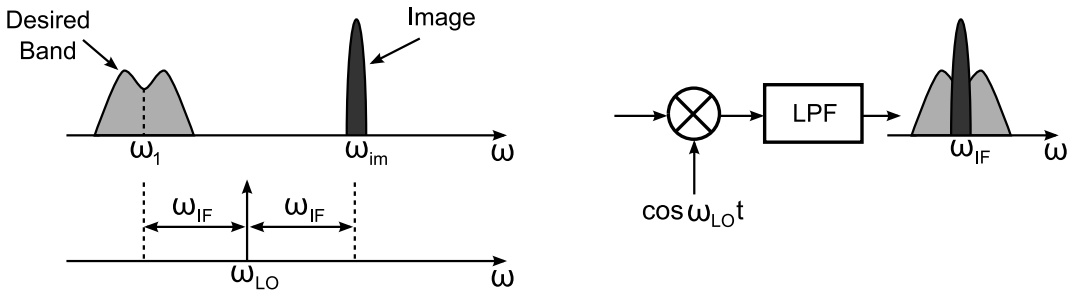


Figure 1.3: *The problem of the image signal in heterodyne receivers.*

However, after the downconversion, a channel select filter is needed and if ω_{IF} is high this filter may not be selective enough, as Fig. 1.4(a) shows, because it would need a very high quality factor Q (defined as the ratio of the center frequency to the bandwidth of the filter). On the other hand, a low ω_{IF} would allow for a bandpass filter with lower Q, but at the same time it would prevent a high attenuation at ω_{IM} (Fig. 1.4(b)). Therefore, a careful selection of IF is needed to cope with the image signal. A trade-off between selectivity at IF and image attenuation at RF is the dual-IF topology sketched in Fig. 1.5, where the concept of heterodyne receiver is applied to multiple downconversion steps. After each conversion step, a partial channel selection is performed, thus relaxing the quality

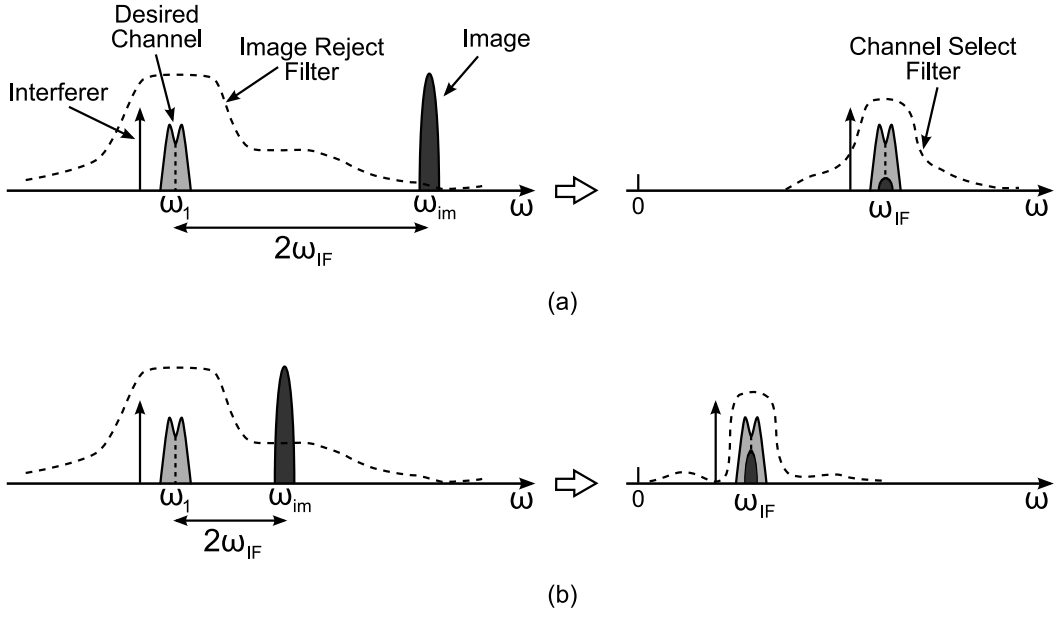


Figure 1.4: *Image rejection by selecting IF. (a) High IF. (b) Low IF.*

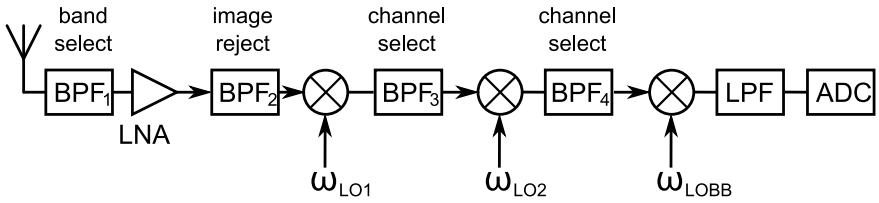


Figure 1.5: *Dual IF architecture for the rejection of the image signal.*

factor requirements. Another way to handle the image signal is at architectural level, using two quadrature conversion paths and exploiting the phase relationships between the two paths to cancel the image signal. Figs. 1.6 and 1.7 show two famous image-reject receivers: the Hartley receiver and the Weaver receiver. In the Hartley receiver of Fig. 1.6, the 90° shift changes the polarity of the image signal, so that the image components have opposite polarities at nodes B and C, while the desired signal components have the same polarity. Therefore, if we sum the total signals at B and C, the image is cancelled. The Weaver architecture in Fig. 1.7, instead, performs basically the same operation using a second quadrature mixing operation instead of a single 90° phase shift stage. The detailed analysis of the operation of these architectures and the issues they raise go beyond the scope of this work, and can be found in [14].

Homodyne receivers are immune from the image problem as, being $\omega_{\mathrm{IF}} = 0$, the image coincides with the signal itself. Moreover, the channel selection filter and the subsequent downconversion stages are replaced by low-pass filters and baseband amplifiers, which are more easily integrated on the same chip. The direct conversion scheme, however, has many issues that in many cases prevent its use. Here we will mention two of them. First of all, the multiplication of the RF signal and the LO signal produces a DC component as $\omega_{\mathrm{RF}} = \omega_{\mathrm{LO}}$. The same happens when the LO and RF signals are not perfectly isolated from each other, thus causing the signal (LO or RF) to be mixed with itself (this phenomenon is called "self-mixing"). The DC offset is dangerous in that it may cause, in the better case, a modification in the biasing conditions of the circuit and, if directly amplified, the saturation of the front-end. This effect can be mitigated with the use of AC coupling between the building blocks. In heterodyne receivers, the problem of the offset is less important, as the IF is far from DC. In this case, the self-mixing may arise only because of the leakage, but the offset is band-

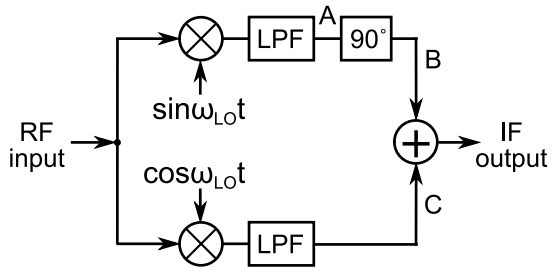


Figure 1.6: *Basic block diagram of a Hartley receiver architecture for the rejection of the image signal.*

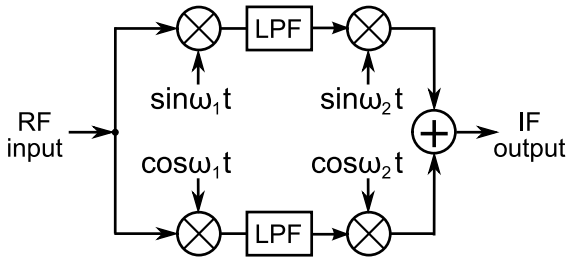


Figure 1.7: *Basic block diagram of a Weaver receiver architecture for the rejection of the image signal.*

pass filtered at IF level. The second problem of homodyne receivers is related to the flicker noise of the active devices. Especially in CMOS implementations of these receivers, the flicker noise may kill the received signal, as most systems are narrow-band, with a channel bandwidth of a few megahertz or even kilohertz, and the corner frequency of the $1/f$ noise is usually around 1 MHz. In broad-band systems, the flicker noise is limited to a very small part of the spectrum, so this problem is less critical, as the flicker noise provides negligible contribution to the average noise figure.

1.2 Input and noise matching techniques

As seen in the previous Section, a band-pass filter is needed immediately after the antenna to attenuate out-of-band interference. Due to linearity and power consumption constraints, these filters are usually passive ones, so they need to be properly terminated. The subsequent stage is the low-noise amplifier (LNA), so its input impedance must provide the right termination to the antenna filter. The LNA must then feature an input resistance that matches the resistance of the antenna (usually 50 Ω). Several techniques can be used to provide a real impedance at the LNA input [9]. A straightforward way is to simply add a 50-Ω shunt resistor at the input terminals of a common-source amplifier, as sketched in Fig. 1.8(a). The shunt resistor, though, adds thermal noise directly at the input of the amplifier and realizes a resistive partitioner that attenuates the input signal by a factor of 2. The combination of these two effects produces unacceptably high noise figures. To circumvent the signal attenuation due to the resistive partitioner, the shunt-series amplifier of Fig. 1.8(b) can be used. The voltage gain of this amplifier is

$$A_V = -\frac{R_L}{R_E}\frac{R_F - R_E}{R_F + R_L} \tag{1.1}$$

where

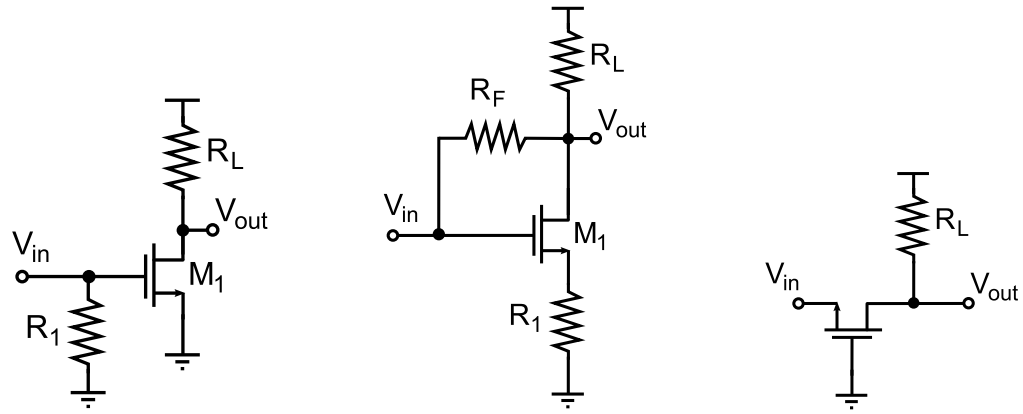
$$R_E = \frac{1}{g_m} + R_1. \tag{1.2}$$

The input resistance is then

$$R_{\text{in}} = \frac{R_F}{1 - A_V} = \frac{R_E(R_F + R_L)}{R_E + R_L}. \tag{1.3}$$

However, the feedback resistance continues to inject noise into the input terminal, and the noise figure remains high, although significantly lower than what results from the previous approach. Fig. 1.8(c) shows how the resistive noise can be avoided by using a common-gate stage, whose input resistance (looking into the source terminal) is equal to $1/g_m$.

All three of the described topologies, though, suffer from a degradation of the noise performance due to the presence of noisy resistances in the signal path (considering the channel resistance of the common-gate stage). A topology that



(a) (b) (c)

Figure 1.8: *Input matching techniques. (a) Resistive termination at the input. (b) Shunt-series feedback. (c) Common-gate input stage*

can provide a real impedance at the input without adding additional noise is the inductively degenerated common-source amplifier of Fig. 1.9(a). In this case, the input impedance can be derived from the equivalent schematic of Fig. 1.9(b):

$$Z_{\text{in}} = sL_S + \frac{1}{sC_{\text{gs}}} + \frac{g_m}{C_{\text{gs}}}L_S \approx sL_S + \frac{1}{sC_{\text{gs}}} + \omega_T L_S. \tag{1.4}$$

At the frequency $\omega = 1/\sqrt{L_S C_{\text{gs}}}$, Z_{in} is real and the input matching can be granted without loss in the noise performance, as a purely reactive component (such as an inductance) is noiseless. Moreover, this approach can be used to obtain simultaneous input and noise matching [15], because in this case the input impedance that allows for input matching is the same as the optimum impedance that allows for the minimum noise figure (that is, the noise figure of the driver transistor alone).

To better understand this result, we will now briefly recall the noise behavior of MOSFETs and the classical noise matching technique and the compare it to the simultaneous input and noise matching technique as done in [15].

The channel thermal noise of a MOS transistor is modeled as an additional current generator between the drain and the source of the transistor. The power spectral density of this current is

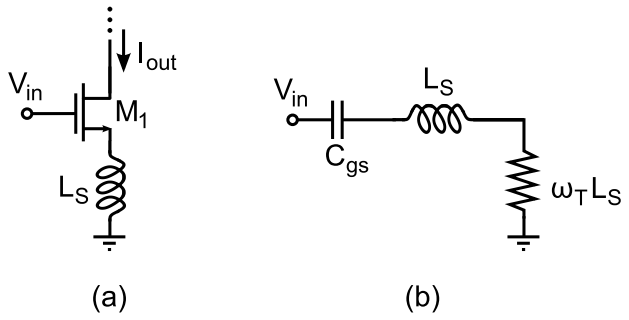


Figure 1.9: *Inductively degenerated common-source amplifier. (a) Schematic. (b) Equivalent schematic for input impedance calculation.*

$$S_{\mathrm{i_{nd}}}(\omega) = 4kT\gamma g_{d0} \tag{1.5}$$

where k is the Boltzmann constant, T is the absolute temperature and g_{d0} is the drain–source conductance when $V_{DS} = 0$. γ is an excess noise parameter that depends on the technology and on the bias conditions. It has a value of unity at $V_{DS} = 0$ and of 0.67 in saturation mode with long-channel devices, and can be more than 2 in short-channel ones. Due to the fluctuating potential of the channel caused by the channel thermal noise, the noise itself capacitively couples into the gate terminal, originating induced gate noise, whose power spectral density is

$$S_{\mathrm{i_{ng}}}(\omega) = 4kT\delta g_g \tag{1.6}$$

where

$$g_g = \frac{\omega^2 C_{\mathrm{gs}}^2}{5g_{d0}}. \tag{1.7}$$

$\delta \approx 1.33$–4 is another excess noise parameter and C_{gs} is the gate–source parasitic capacitance. Because of its dependence on ω^2, the induced gate noise is sometimes referred to as "blue noise", as its power increases at higher frequencies. Fig. 1.10 shows the small-signal model of the noisy transistor. The two described noise currents are correlated with each other, with a correlation coefficient

$$c = \frac{S_{\mathrm{i_{ng}i_{nd}}}(\omega)}{\sqrt{S_{\mathrm{i_{ng}}}(\omega) S_{\mathrm{i_{nd}}}(\omega)}} \tag{1.8}$$

For MOS devices, $c \approx j0.395$, which is a purely imaginary value, thus reflecting the capacitive coupling between the two noise sources. The minimum noise figure of a cascode amplifier (Fig. 1.11) is then

$$F_{\min}(\omega) = 1 + \frac{2}{\sqrt{5}} \frac{\omega}{\omega_T} \sqrt{\gamma\delta(1 - |c|^2)} \tag{1.9}$$

with $\omega_T = g_m/C_{\text{gs}}$.

In order for the amplifier to have the minimum noise figure, it must see a source admittance

$$Y_S = \frac{1}{Z_S} = Y_{\text{opt}}^{\text{o}}(\omega) = \alpha\omega C_{\text{gs}} \sqrt{\frac{\delta}{5\gamma}(1 - |c|^2)} - j\omega C_{\text{gs}} \left(1 + \alpha|c| \sqrt{\frac{\delta}{5\gamma}}\right) \tag{1.10}$$

where $\alpha = g_m/g_{d0}$ accounts for short channel effects. Therefore, with a proper input matching network, the original source impedance Z_S' can be transformed into $1/Y_{\text{opt}}^{\text{o}}$ to obtain noise matching. However, the input admittance of the

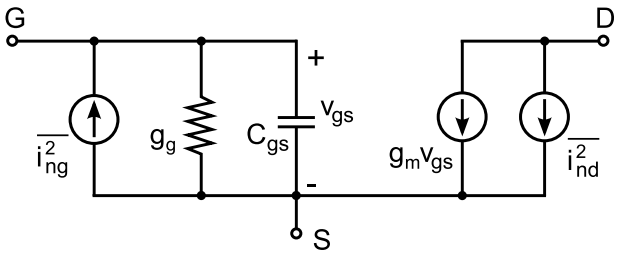


Figure 1.10: *Small-signal model of a MOS transistor including noise sources.*

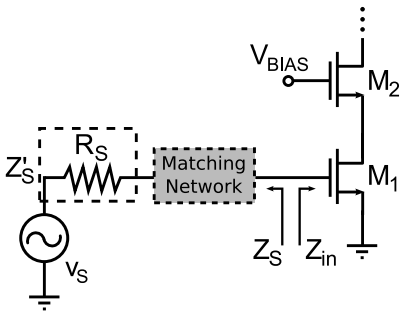


Figure 1.11: *Simple cascode amplifier.*

amplifier is $Y_{\text{in}} = 1/Z_{\text{in}} = j\omega C_{\text{gs}}$. To obtain input matching, the input impedance should be the complex conjugate of the source impedance ($Z^{\text{o}}_{\text{opt}} = Z^{*}_{\text{in}}$), but from (1.10) we can see that in this case it is not possible.

With the inductively degenerated cascode topology, instead, the optimum noise-matching impedance becomes

$$Z_{\text{opt}}(\omega) = \frac{1}{Y^{\text{o}}_{\text{opt}}(\omega)} - j\omega L_S = Re\left[\frac{1}{Y^{\text{o}}_{\text{opt}}}\right] - m\frac{1}{j\omega C_{\text{gs}}} - j\omega L_S. \tag{1.11}$$

while the minimum noise figure is not changed. Keeping in mind that the condition for simultaneous input and noise matching is $Z_{\text{opt}} = Z^{*}_{\text{in}}$, (1.4) and (1.11) show that, as long as m is reasonably close to unity, the inductive degeneration helps reaching both matching conditions at the same time without any impact in the minimum noise figure.

1.3 Ultra-Wideband systems

The Federal Communication Commission (FCC) released the spectrum for Ultra-Wideband (UWB) systems in 2002, allocating the frequencies from 3168 MHz to 10560 MHz for wide-band applications with an in-door spectral density limit of -41.3 dBm/MHz [1]. Two industry consortia have proposed two different ways of exploiting the potential of this new technology. The first proposal suggests the use of this spectrum for impulse-radio applications (based on the transmission of very short pulses that occupy the entire available spectrum). The second proposal, supported by the Wi-Media Alliance, concerns the application of UWB for short-range and high data-rate communications [2], [16]. According to this

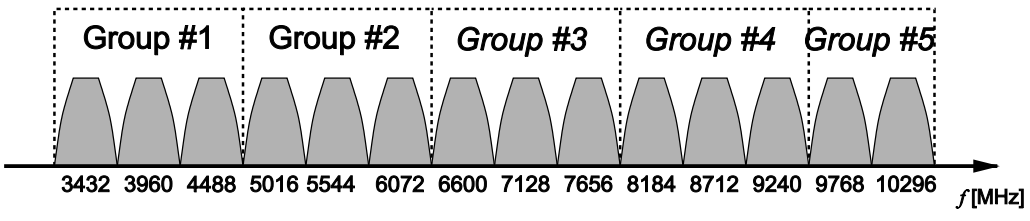


Figure 1.12: *Spectrum partitioning in UWB systems.*

proposal, the huge UWB frequency range is divided into fourteen, 528-MHz wide, sub-bands so that the transceiver can process signals with smaller bandwidth. Therefore, the center frequency of the N$^{\text{th}}$ sub-band, in megahertz, is given by

$$f_N = 2904 + 528{\times}N. \tag{1.12}$$

As Fig. 1.12 shows, the various UWB sub-bands are grouped into four groups made of three sub-bands each, plus a fifth group made of only two bands. The use of a sixth one, including sub-bands #9 to #11, was also proposed to allow for world-wide inter-operability, as the spectrum from 6 to 9 GHz was the only world-available one. The possibility to use this group, though, is presently being revisited, because the Electronic Communications Committee (ECC) has decided to reduce the upper edge of the UWB band from 9 GHz to 8.5 GHz, thus excluding sub-band #11 from operation in Europe [17]. The proposed transmission scheme makes use of frequency hopping between multiple sub-bands in the same band group to interleave OFDM symbols, providing robustness against multi-path fading and interference.

The wide bandwidth of UWB signals poses several challenges on the design of the receivers, and in particular on the LNA, which will have to feature input match and low noise figure over the entire bandwidth, as well as a flat gain and good linearity.

1.4 Broad-band input and noise matching

The input matching techniques discussed in Sect. 1.2 found their application in narrow-band systems. However, those concepts can be extended to a wide-band fashion.

The solution that uses the shunt gate resistor is intrinsically wide-band, but we already saw that it has very poor noise performance. The amplifier with shunt-series feedback can also be suitable for wide-band applications, but achieving a low NF at high frequency poses serious constraints on the size of the input transistor of the amplifier. If we call C_{in} the total input capacitance of the amplifier and we assume the matching condition $R_F = (1 + A)R_S$ (where R_F is the feedback resistor, R_S is the source resistance and A is the voltage gain of the amplifier), the input impedance is $Z_{\text{in}}(s) = R_S/(1 + sR_SC_{\text{in}})$ [18]. This means that in order

to achieve a good matching at high frequencies we must have a small C_{in}, and this cannot always be possible. Distributed amplifiers can address this issue, but at the price of a power consumption increased by a factor higher than five. Wide-band input matching and good noise performance can be obtained by expanding the inductively degenerated common source amplifier by embedding the input network into a multi-section reactive network to provide impedance matching over a wider band [18], [19]. A conventional LC ladder network [20] can be used for the purpose.

In wide-band systems, the noise analysis can be performed following the guidelines of the narrow-band analysis, and then optimization can be performed on the average noise figure, calculated over the in-band frequencies. The detailed analysis can be found in [18]. Here is reported the resulting (non-averaged) NF:

$$F(\omega) \approx 1 + \frac{P(\omega)}{g_m R_S} \frac{\gamma}{\alpha} \tag{1.13}$$

where

$$P(\omega) = \frac{p^2\alpha^2\chi^2(1-|c|^2)}{1+2|c|p\alpha\chi+p^2\alpha^2\chi^2} + \omega^2 C_t^2 R_S^2 (1+2|c|p\alpha\chi+p^2\alpha^2\chi^2),$$

$$p = \frac{C_{\text{gs}}}{C_t}, \qquad \chi = \sqrt{\frac{\delta}{5\gamma}} \qquad \text{and} \qquad C_t = C_{\text{gs}} + C_P.$$

C_P is a capacitance that may be added between the gate and source terminals of the transistors to give flexibility to the design and achieve noise and input matching under power constraints [15]. Once averaged against the frequency, the design variables are the drain bias current I_D and the transistor width. The optimization of the NF can therefore be performed on these two parameters.

1.5 Interference in UWB systems

The huge frequency range covered by UWB systems makes them particularly subject to interference, coming from other transmission standards whose frequencies of operation lie inside the UWB spectrum. The power of these blockers can be more than 60 dB higher than the wanted UWB signal and can desensitize the receiver gain and saturate the analog front-end [7], [8]. Moreover, their second- and third-order intermodulation products can fall in-band and add up to the signal.

The major sources of interference are the following:

• GSM	0.9 GHz and 1.9 GHz
• Bluetooth / IEEE 802.11b/g	2.4–2.5 GHz
• WiMAX [7], [8], [21]	2.5–2.9 GHz
	3.4–3.6 GHz
	5.2–5.9 GHz
• IEEE 802.11a / Wi-Fi	4.9–5.8 GHz

In particular, the most critical blockers are the ones coming from the various wireless LANs from 5 to 6 GHz, corresponding to UWB band group #2, and from the emerging WiMAX, which uses two bands in the 3–6 GHz range. Fig 1.13 shows the spectra of these blockers against the UWB spectrum. The presence of a large number of blockers in the 5–6 GHz band is the reason why the band group #2 will not be used in UWB systems.

Table 1.1 summarizes several significant out-of-band blockers that produce in-band intermodulation products (0.9-GHz GSM is supposed to be sufficiently attenuated by the antenna filter, and so it is excluded from the table). For simplicity, only intermodulation between different standards is considered. We can see that there is plenty of blockers that can produce in-band intermodulation products.

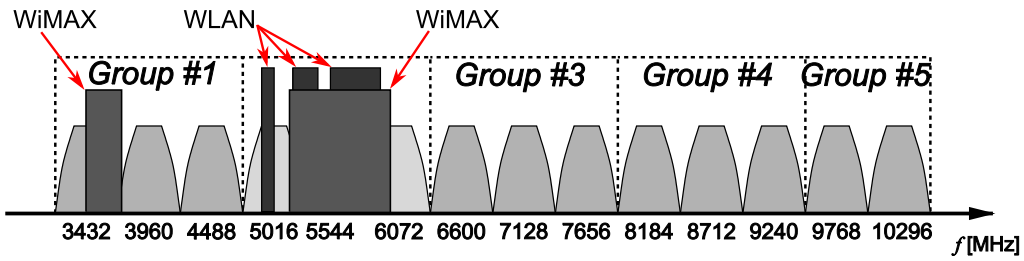


Figure 1.13: *Blockers inside the spectrum of UWB systems.*

Table 1.1: *Intermodulation products of out-of-band blockers in UWB spectrum*

f_1 [GHz]	f_2 [GHz]	IM order	f_{IM} [GHz]	f_1 [GHz]	f_2 [GHz]	IM order	f_{IM} [GHz]
1.9	2.4	2	4.3	2.4	5.2	3	8
1.9	2.4	3	3.9	2.4	5.8	2	3.4
1.9	2.5	2	4.4				8.2
1.9	2.5	3	4.1	2.4	5.8	3	9.2
1.9	2.9	2	4.8	2.9	4.9	2	7.8
1.9	2.9	3	3.9	2.9	4.9	3	6.9
1.9	4.9	2	6.8	2.9	5.2	2	8.1
1.9	4.9	3	7.9	2.9	5.2	3	7.5
1.9	5.2	2	7.1	2.9	5.8	2	8.7
1.9	5.2	3	8.5	2.9	5.8	3	8.7
1.9	5.8	2	3.9	4.9	5.2	2	10.1
			7.7	4.9	5.2	3	4.6
1.9	5.8	3	9.7	4.9	5.8	3	4
2.4	2.9	3	3.4				6.7
2.4	4.9	2	7.3	5.2	5.8	3	4.6
2.4	4.9	3	7.4				6.4
2.4	5.2	2	7.6				

Chapter 2

Integrated Inductors and Transformers

Integrated inductors are often used to design RF integrated circuits such as mixers, oscillators and amplifiers because they occupy less area and ensure a smaller power dissipation compared to the off-chip solution. However, the resistivity of metal strips and substrate causes a considerable reduction of the quality of the inductors. Moreover, the maximum operating frequency is limited by the self-resonance f_R, whose value depends on the parasitic capacitances.

2.1 Physical design parameters

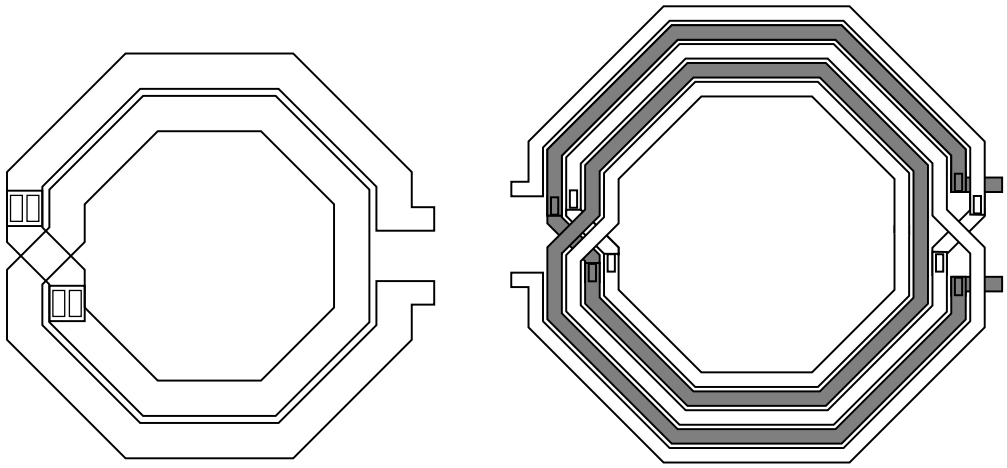
The most widely used on-chip inductor is the planar spiral, shown in Fig. 2.1(a) in an octagonal-shaped symmetrical implementation. The advantage of a higher-sided shape is that there are less current-crowding effects, and so the spiral is nearer to the ideal behavior. However, with respect to a square spiral with the same radius, a high-sided shape occupies less area, thus reducing the inductance.

The design parameters of this kind of structures are:

- external radius R;
- number of windings N;
- width of metal traces W;
- separation between traces D.

By coupling two inductors and interleaving the windings, it is also possible to create planar transformers as shown in Fig. 2.1(b).

The inductance of an arbitrary spiral inductor is a function of all the listed parameters and of the geometry of the spiral.



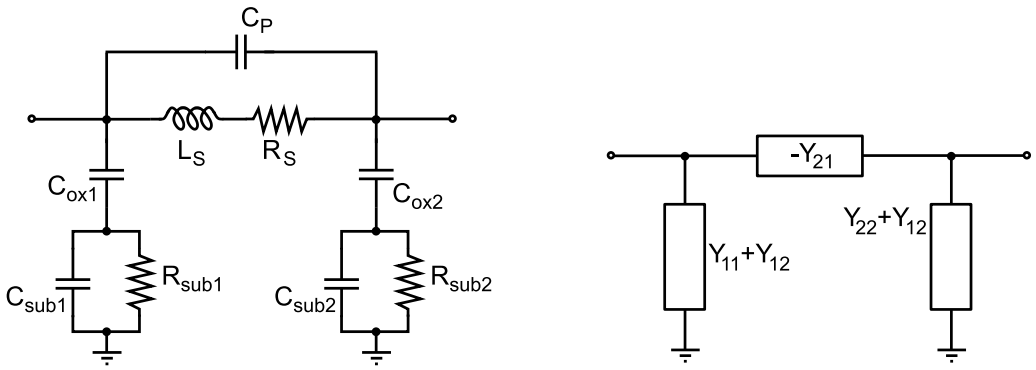
(a) (b)

Figure 2.1: *Basic layout of planar integrated inductive structures. (a) Planar spiral inductor. (b) Planar spiral transformer.*

2.2 Modeling

The most used model for spiral inductors is the π-model of Fig. 2.2(a), where L_S is the inductance, R_S is the resistance of the metal trace, and C_P is the edge-to-edge capacitance between the coils. C_{ox1} and C_{ox2} are the oxide capacitances between the metal line and the substrate seen at each terminal. $C_{\text{sub1,2}}$ and $R_{\text{sub1,2}}$ are the substrate capacitances and resistances, respectively.

Inductors are generally simulated with electro-magnetic (EM) simulators, which can compute the scattering (S-) parameters of the structure [20]. From the S-parameters of the EM-simulated inductor, we can calculate the admittance (Y-) parameters, from which the general PI network of Fig. 2.2(b) can be derived.



(a) (b)

Figure 2.2: *PI model of a two-port integrated inductor. (a) PI model with lumped components. (b) General purpose PI model with Y-parameters.*

At a low frequency, C_P can be considered as an open circuit, so we can compute L_S and R_S as

$$L_S = \frac{\mathcal{I}m\left(-1/Y_{21}\right)}{2\pi f} \tag{2.1}$$

$$R_S = \mathcal{R}e\left(-\frac{1}{Y_{21}}\right). \tag{2.2}$$

If the inductor is symmetrical, we can also assume that $Y_{11} = Y_{22}$. In this way, we have $C_{\text{ox1}} = C_{\text{ox2}}$, $C_{\text{sub1}} = C_{\text{sub2}}$ and $R_{\text{sub1}} = R_{\text{sub2}}$. Now, we can compute the impedance (Z-) parameters. At low frequencies, we can assume that C_P and C_{sub} are open circuits, L_S is a short circuit and R_S is negligible with respect to R_{sub}. Under this assumptions, Z_{11} becomes as sketched in Fig. 2.3 and C_{ox} and R_{sub} can be computed:

$$C_{\text{ox}} = -\frac{1}{2}\frac{1}{2\pi f\mathcal{I}m\left(Z_{11}\right)} \tag{2.3}$$

$$R_{\text{sub}} = 2\mathcal{R}e\left(Z_{11}\right). \tag{2.4}$$

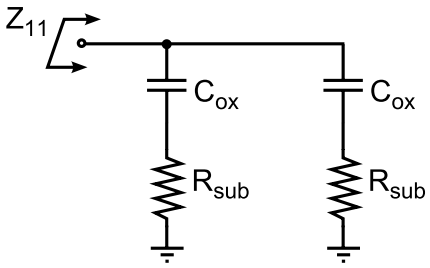


Figure 2.3: *Calculation of Z_{11} in the low-frequency approximation.*

Otherwise, if the inductor is not symmetrical, the two shunt branches of the π-model are not equal, and (2.3) and (2.4) must be splitted into:

$$C_{\text{ox1}} = -\frac{1}{2\pi f \mathcal{I}m\left(Z_{P1}\right)} \tag{2.5}$$

$$C_{\text{ox2}} = -\frac{1}{2\pi f \mathcal{I}m\left(Z_{P2}\right)} \tag{2.6}$$

$$R_{\text{sub1}} = \mathcal{R}e\left(Z_{P1}\right) \tag{2.7}$$

$$R_{\text{sub2}} = \mathcal{R}e\left(Z_{P2}\right) \tag{2.8}$$

where $Z_{P1} = 1/(Y_{11} + Y_{12})$ and $Z_{P2} = 1/(Y_{22} + Y_{12})$ as in Fig. 2.2(b).

The remaining components of the network determine the frequency behavior of the inductor, and can be estimated by fitting the circuit to the data of the EM simulation.

2.3 EM simulations

There are several EM simulators that can be used to simulate inductive structures. EM simulators accept as input the layout of a component (be it an inductor, or a capacitor, or even a transistor) and numerically solve the EM Green equations, given the physical parameters of the materials (metal stripes and dielectrics between metals). During this thesis three of them were used, each with its own advantages and disadvantages.

2.3.1 ASITIC

ASITIC is a free tool developed at the University of California, Berkeley [22]. This tool can be used to design spiral inductors and transformers, but symmetrical structures (such as the ones used in this work) are not allowed. ASITIC was therefore used to get a first-order estimation of the physical parameters needed to provide a certain amount of inductance and of the parasitic resistance of the structure.

2.3.2 ADS Momentum

ADS Momentum is a commercial EM simulator able to calculate the EM behavior of an arbitrary structure. Because of its higher versatility, it can give more accurate results than ASITIC, and was used to simulate the employed structures. The output of the EM simulation is the set of S-parameters. The file into which the data is saved is then made available for circuit simulations with Spectre. For the EM data to be reliable, the structure must be simulated up to frequencies higher than the self-resonant frequency. During the small-signal analysis, the S-parameters are converted into Z- or Y- parameters, so the EM structure is treated as a conventional n-port device. In order to perform transient simulation, though, the S-parameter data must be fitted to a rational function, so as to be anti-transformed and a time-domain solution can be found. This may not always be possible and can cause convergence problems.

2.3.3 Sonnet

Sonnet is another commercial tool for EM simulations and it works exactly in the same way as Momentum does. It can simulate an arbitrary structure, given the parameters of the materials, storing the calculated S-parameters into a file readable by Spectre. The main difference between this tool and Momentum is that Sonnet has a more accurate way to compute the lateral capacitance between two metal stripes on the same metal level, so that the self-resonant frequency in general is lower than the ones calculated by Momentum and closer to the real one. However, for some reason, the output data is not easily fitted to a rational function, causing the order of the polynomials to rise up to more than 40 for

complex structures such as the transformers, besides the fact that convergence is not always achieved. This causes Spectre simulations to run very slowly, often taking ours to complete. In addition, both Sonnet and Momentum fail to correctly calculate the Green functions for low frequencies, so the minimum frequency for safe simulations is around 100 MHz. Both of them, however, can be told to perform a DC simulation (without which rational fitting would not be reliable).

2.4 Implemented inductors

In this work, several inductors were designed and simulated with both ADS Momentum and Sonnet. All of the inductors are symmetrical structures with octagonal shape and a center tap and were simulated as 3-port structures. Two transformers were designed, as well, one of which (Sect. 2.4.5) is used as two differentially-driven coupled inductors. Both of them have octagonal shape. In the following, a summary of the simulation results is given, and the main parameters, such as the inductance, the equivalent series resistance, the quality factor and self-resonance frequency are shown. As a symmetrical inductor may be considered as a particular transformer with one terminal of the primary winding shorted with a terminal of the secondary, the coupling factor k is also extracted for each structure.

The equivalent inductance and resistance are computed as dictated in (2.1) and (2.2), respectively. The inductors will be driven in a differential mode, therefore the differential quality factor will be extracted using the T-model in Fig. 2.4, which is more suitable in this case.

With this model, we define a differential impedance $Z_D = Z_{11} + Z_{22} - 2Z_{21}$, from which we can derive the values

$$L_{\mathrm{d}} = \frac{\mathcal{I}m\,(Z_D)}{2\pi f}, \qquad R_{\mathrm{d}} = \mathcal{R}e\,(Z_D) \qquad \text{and} \qquad Q_{\mathrm{d}} = \frac{\mathcal{I}m\,(Z_D)}{\mathcal{R}e\,(Z_D)}. \tag{2.9}$$

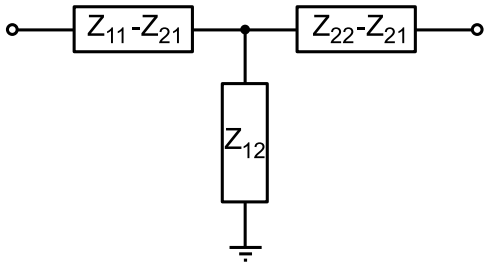
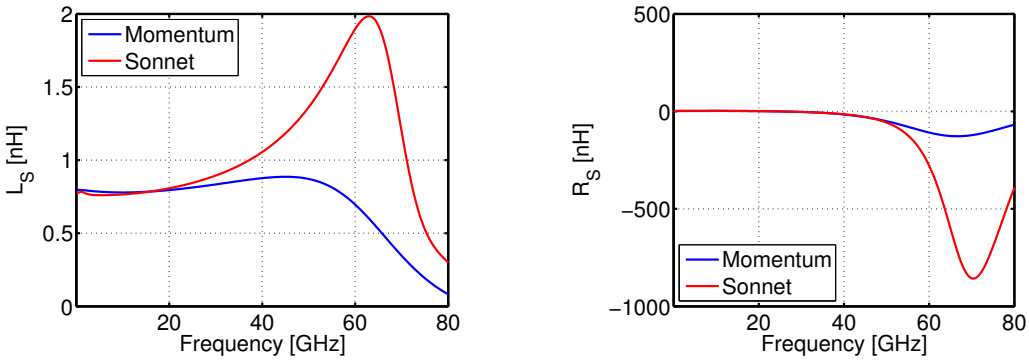


Figure 2.4: *T-model of a 2-port system.*

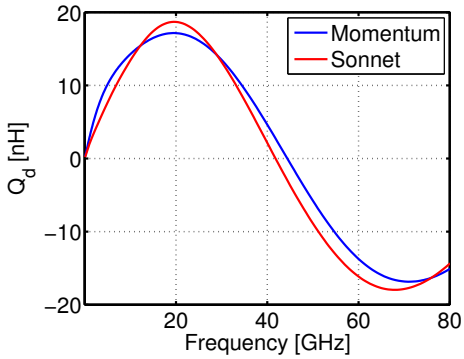
2.4.1 0.8-nH differential coil

The desired inductance of this structure is small, so it was realized with a quite wide metal strip to reduce the parasitic resistance. As this coil will be used to inductively degenerate the LNA drivers, a small parasitic resistance helps keeping the noise low. Fig. 2.5 shows the simulated behavior of this inductor. Both Sonnet and Momentum give a low-frequency inductance value $L_S = 0.78$ nH (Fig. 2.5(a)) and the parasitic resistance simulated by Momentum is $R_S = 1.8\ \Omega$ (Sonnet computes it as $R_S = 2.5\ \Omega$, cf. Fig. 2.5(b)). The resistance seems to be mainly due to the resistance of the vias. As plotted in Fig. 2.5(c), the maximum quality factor is $Q = 17$ in Momentum simulations and $Q = 19$ in Sonnet ones. From Fig. 2.5(a) we can also see that the self-resonance frequency is above 80 GHz.



(a) (b)

Figure 2.5: *Significant parameters of the 0.8-nH inductor. ADS Momentum and Sonnet simulations. (a) Equivalent differential inductance. (b) Equivalent differential resistance.*



(c)

Figure 2.5: *Significant parameters of the 0.8-nH inductor. ADS Momentum and Sonnet simulations. (c) Differential quality factor.*

2.4.2 1.6-nH differential coil

The results of EM simulations on this coil are shown in Fig. 2.6. The low-frequency value of the inductance is $L_S = 1.6$ nH (Fig. 2.6(a)) and the low-frequency resistance is $R_S = 3\ \Omega$ in Momentum simulation, while Sonnet computes it as $R_S = 4\ \Omega$ (Fig. 2.6(b)). In this case, the self-resonance frequencies calculated by the two simulators are very close to each other. Their values are $f_{\mathrm{SR}} = 24.4$ GHz (Momentum) and $f_{\mathrm{SR}} = 24.6$ GHz (Sonnet). The coupling factor between the two half coils is $k = 0.58$ according to Momentum and $k = 0.72$ according to Sonnet. Fig. 2.6(c) shows that the maximum quality factor is $Q \approx 12$ in both simulations. As this coil will be used in the notch filter, it is useful to consider the quality factor at 5 GHz, where the filter is going to operate. The value is $Q_{5\mathrm{GHz}} = 10.8$, as computed by Momentum. Sonnet gives the similar result $Q_{5\mathrm{GHz}} = 9.5$.

2.4.3 2.8-nH differential coil

The EM-simulated inductance, resistance and quality factor of this coil are shown in Fig. 2.7. The low-frequency value of the inductance is $L_S = 2.7$ nH (Fig. 2.7(a)) and the equivalent low-frequency resistance is $R_S = 5.5\ \Omega$ in Momentum simulations, while in Sonnet ones it is $R_S = 6.5\ \Omega$ (Fig. 2.7(b)). Now, the self-resonance

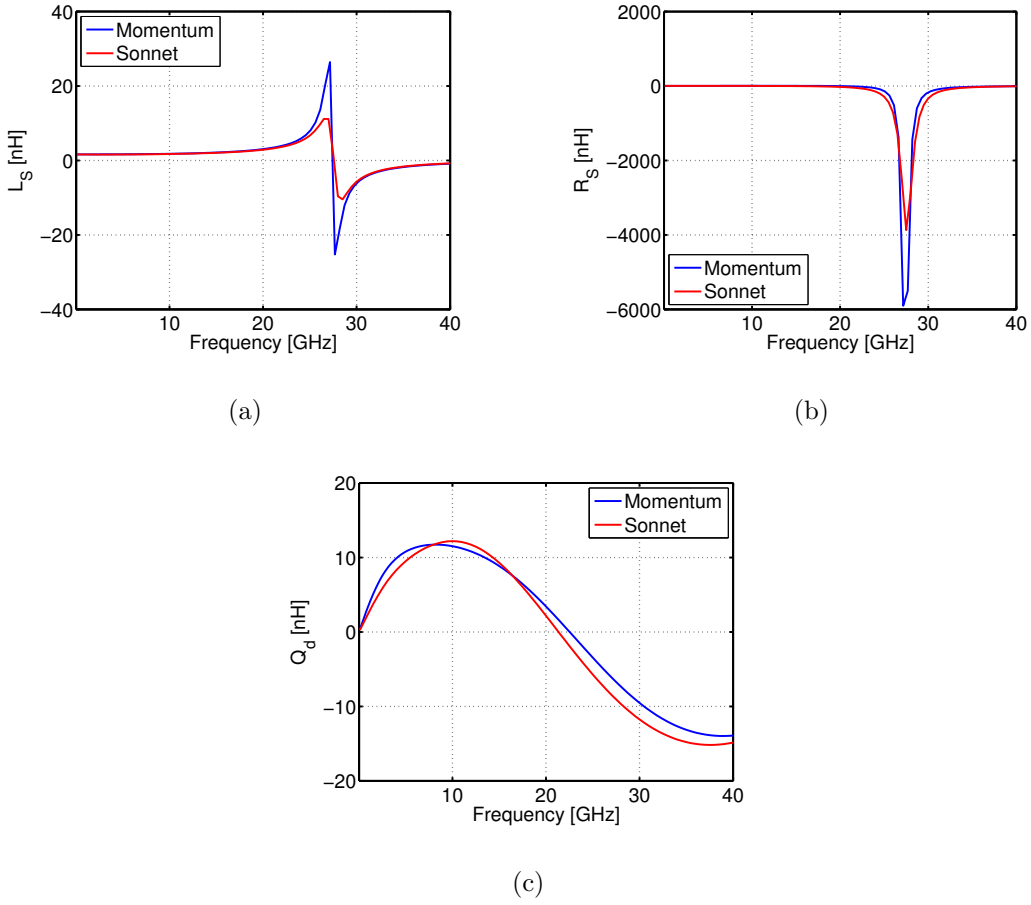


Figure 2.6: *Significant parameters of the 1.6-nH inductor. ADS Momentum and Sonnet simulations. (a) Equivalent differential inductance. (b) Equivalent differential resistance. (c) Differential quality factor.*

computed by Sonnet ($f_{\mathrm{SR}} = 19$ GHz) is lower than the Momentum-calculated one ($f_{\mathrm{SR}} = 20.4$ GHz). The coupling factor between the two half coils is $k = 0.66$ as computed by both simulators. The quality factor is shown in Fig. 2.7(c). Its peak value is $Q = 12.3$ in the case of Momentum data and $Q = 10.8$ in the case of Sonnet data. Again, as this coil will be used in the notch filter, we concern about the values at 5 GHz, that are $Q_{5\mathrm{GHz}} = 11.4$ and $Q_{5\mathrm{GHz}} = 9.7$ according to Momentum and Sonnet, respectively.

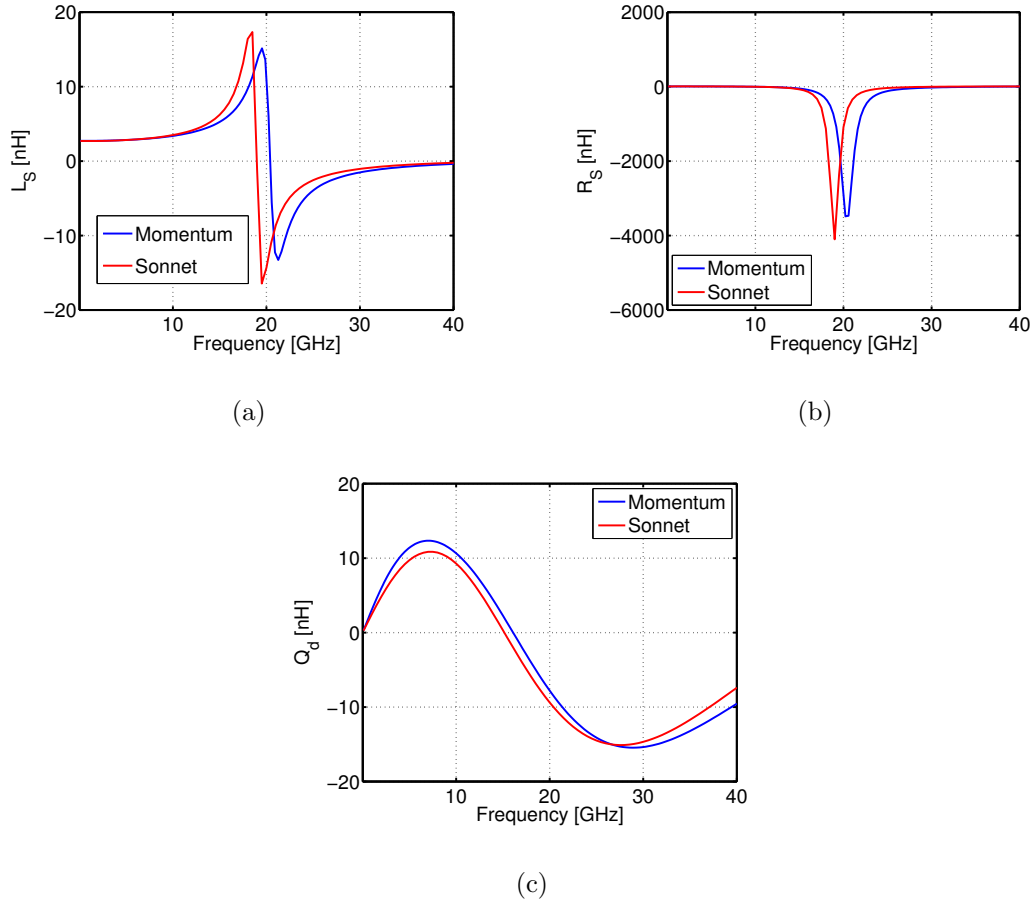


Figure 2.7: *Significant parameters of the 2.8-nH inductor. ADS Momentum and Sonnet simulations. (a) Equivalent differential inductance. (b) Equivalent differential resistance. (c) Differential quality factor.*

2.4.4 3.8-nH differential coil

Fig. 2.8 shows the EM-simulated equivalent differential inductances, resistances and quality factors. The low-frequency inductance is $L_S = 3.7$ nH and the low-frequency series resistance is $R_S = 7\,\Omega$ in Momentum simulations and $R_S = 8\,\Omega$ in Sonnet simulations. The self resonance frequency is $f_{\mathrm{SR}} = 15$ GHz (Momentum) and $f_{\mathrm{SR}} = 13.7$ GHz (Sonnet). From Fig. 2.8(c) we see that the maximum quality factor is $Q = 11$ in Momentum simulations and $Q = 9.5$ in Sonnet ones.

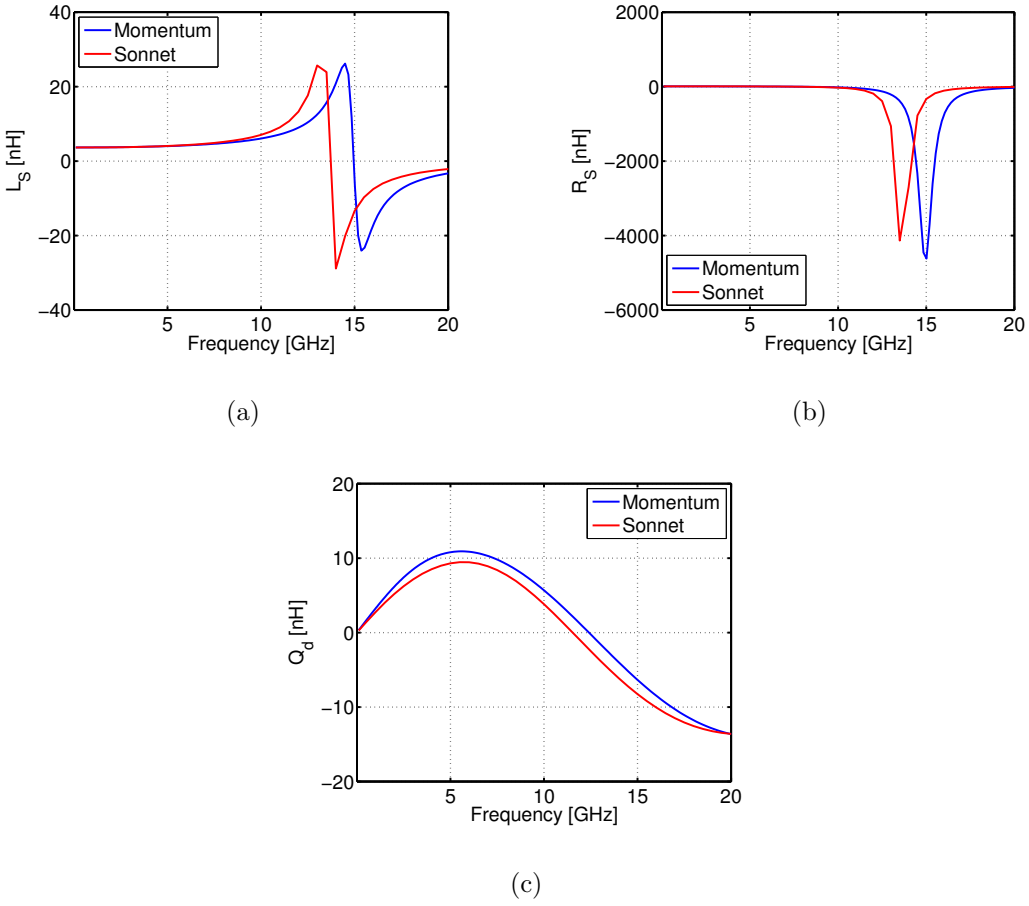


Figure 2.8: *Significant parameters of the 3.8-nH inductor. ADS Momentum and Sonnet simulations. (a) Equivalent differential inductance. (b) Equivalent differential resistance. (c) Differential quality factor.*

This structure was also integrated stand-alone for measurement purposes. In this case, one of the terminals was grounded and a single-port measurement was performed, therefore obtaining a single-ended inductance. So, a comparison is now given between the single-ended parameters obtained from the simulations and the ones obtained from the measurements. The equivalent single-ended inductance, resistance and quality factors are thus given by

$$L_S = \frac{\mathcal{I}m\,(1/Y_{11})}{2\pi f} \tag{2.10}$$

$$R_S = \mathcal{R}e\,(1/Y_{11}) \tag{2.11}$$

$$Q = \frac{\mathcal{I}m\,(1/Y_{11})}{\mathcal{R}e\,(1/Y_{11})}. \tag{2.12}$$

Fig. 2.9(a) shows the inductance extracted from EM simulations and 1-port measurement results.

The low-frequency inductance is 3.7 nH, equal to the differential one, as expected, in all of the three cases. The three values of the self-resonance frequency f_{SR} are 10.7, 10.1 and 9.19 GHz for the Momentum simulation, the Sonnet simulation and the measurement results, respectively. The values are clearly different from the differential ones because of the different way in which these values are computed.

Fig. 2.9(b), instead, shows the equivalent series resistance obtained in the same conditions. Again, the low-frequency values are equal to the differential ones. The measured low-frequency values follow the Momentum ones. Fig. 2.9(c) shows the simulated and measured single-ended quality factors of the inductor, which are different from the differential ones for the same reasons as the f_{SR}'s are. Finally, the maximum quality factor in the three cases (Momentum, Sonnet, measured, respectively) is 7.1, 6.1 and 6.

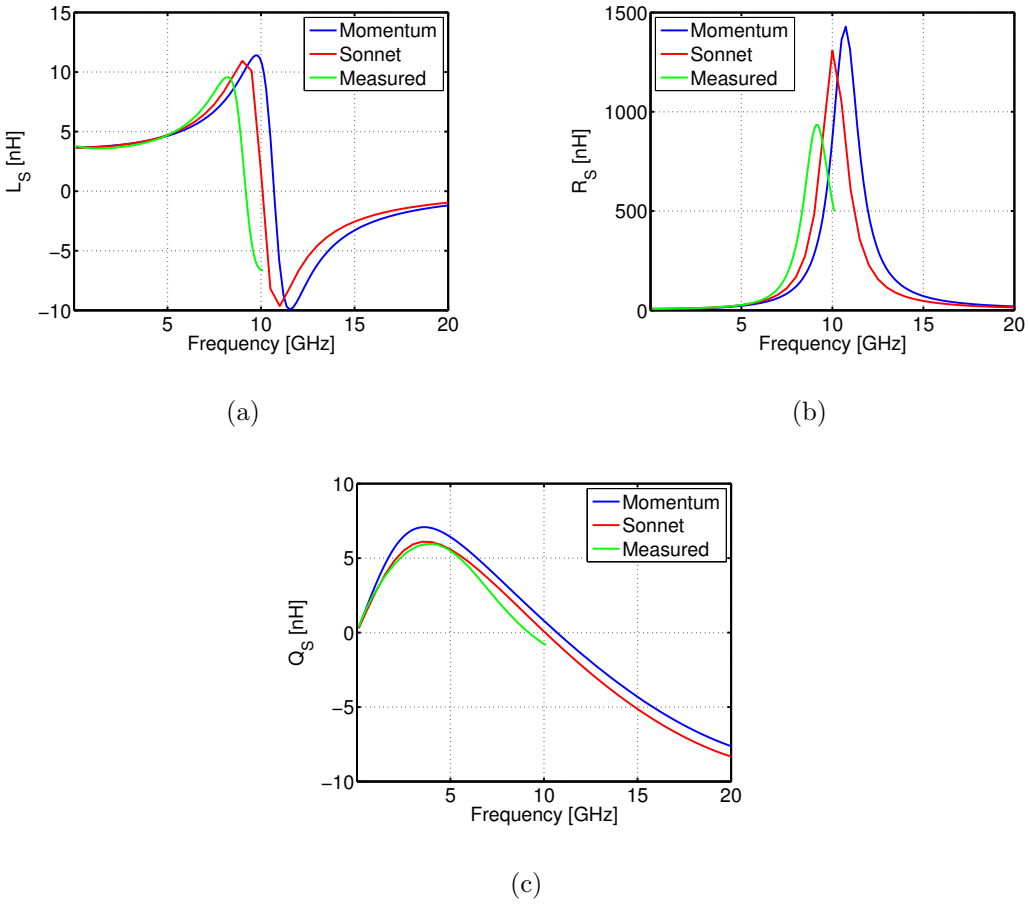


Figure 2.9: *Significant parameters of the 3.8-nH inductor in the 1-port configuration. ADS Momentum simulation, Sonnet simulation and measurement results. (a) Equivalent single-ended inductance. (b) Equivalent single-ended resistance. (c) Single-ended quality factor.*

2.4.5 4.4-nH 1:1 transformer

This structure is a 1:1 transformer and is used in differential mode as two mutually coupled inductors [23]. In this way, the effective inductance in differential mode is raised by a factor equal to the coupling factor k: $L_{S_{\text{eff}}} = (1+k)L_S$.

A first set of simulations is obtained by letting one of the coils be floating and simulating the other one as a two-port system, as shown in Fig. 2.10(a). This lets us compute the significant values of a single inductor, with no mutual coupling. This procedure leads to the one-coil plots in Fig. 2.11. The significant values are reported in Table 2.1.

A second set of simulations was performed as illustrated in Fig. 2.10(b) to extract the same values when the two coils are driven in a differential mode. This configuration brings the structure to resemble a symmetrical coil like the ones discussed above. Fig. 2.12 shows the usual plots obtained with this new configuration. The significant values obtained in this way are reported in Table 2.1, too. The effective low-frequency differential inductance is 8.9 nH, that is $L_{S\text{s}} = 2 \times (1+k)L_S$ because we are considering two coupled coils, while L_S refers to a single-coil inductance. Therefore, the coupling coefficient is $k = 0.72$.

This structure was integrated stand-alone for measurement purposes. The measurements were performed on-wafer on a probe-station in the configuration depicted in Fig. 2.10(c), where the mutual inductor is treated as a proper 1:1 transformer. To provide fair comparison with the measurements, a third set of simulations were run in this kind of configuration. The results of both simulations

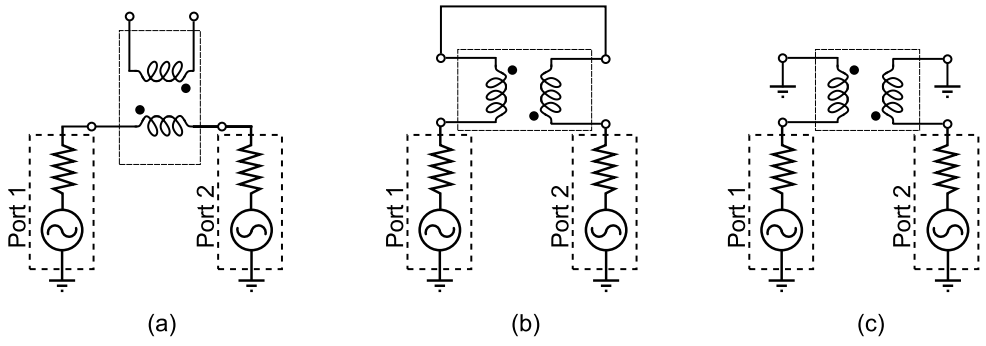


Figure 2.10: *Configurations for the simulation of the 4.4-nH coupled inductor. (a) One-coil configuration. (b) Differentially-driven configuration. (c) Transformer-like configuration*

and measurements are reported in Fig. 2.13 and are obtained using the T-model in Fig. 2.4 with the following expressions:

$$L_S = \frac{\mathcal{I}m\left(Z_{11}\right)}{2\pi f} \tag{2.13}$$

$$R_S = \mathcal{R}e\left(Z_{11}\right) \tag{2.14}$$

$$Q_S = \frac{\mathcal{I}m\left(Z_{11}\right)}{\mathcal{R}e\left(Z_{11}\right)}. \tag{2.15}$$

The reported plots refer to the primary winding only, as we assume that the plots for the secondary are the same as the ones for the primary, being the structure symmetrical. Table 2.1 reports these results, as well. The measurement data suffer from the effect of the parasitic capacitance provided by the pads. This capacitance have been partly, but not entirely, de-embedded. The self-resonance frequency is above 10 GHz, which is the maximum measured frequency, therefore the real datum for f_{SR} cannot be extracted.

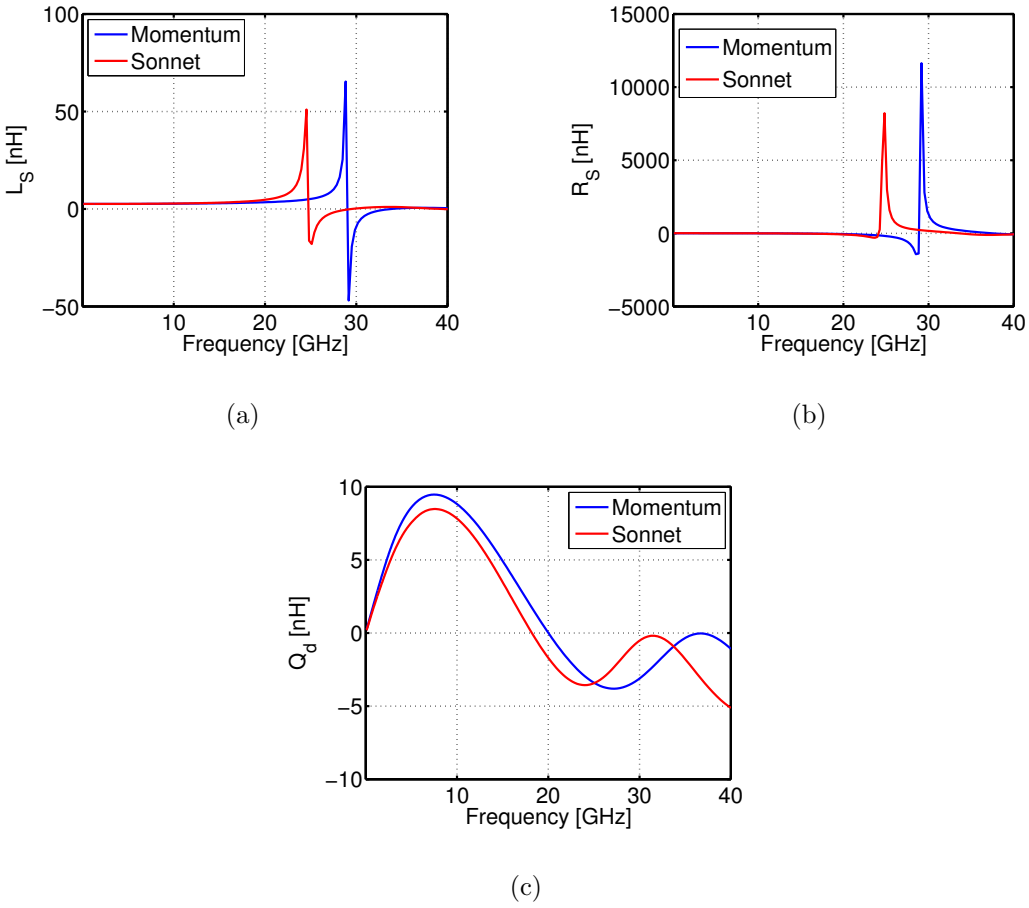


Figure 2.11: *Significant parameters of the 4.4-nH mutual inductor in the one-coil configuration. ADS Momentum and Sonnet simulations. (a) Equivalent one-coil inductance. (b) Equivalent one-coil resistance. (c) One-coil quality factor.*

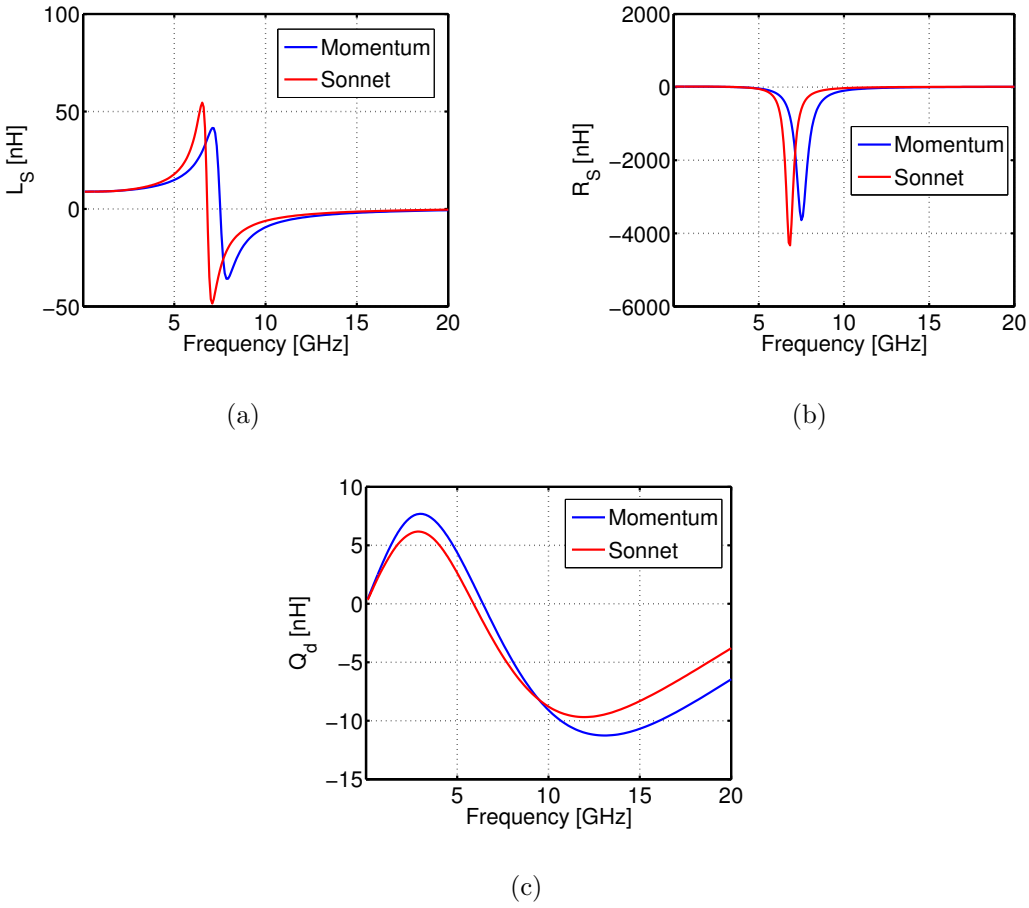


Figure 2.12: *Significant parameters of the 4.4-nH mutual inductor in the differentially-driven configuration. ADS Momentum and Sonnet simulations. (a) Equivalent differential inductance. (b) Equivalent differential resistance. (c) Differential quality factor.*

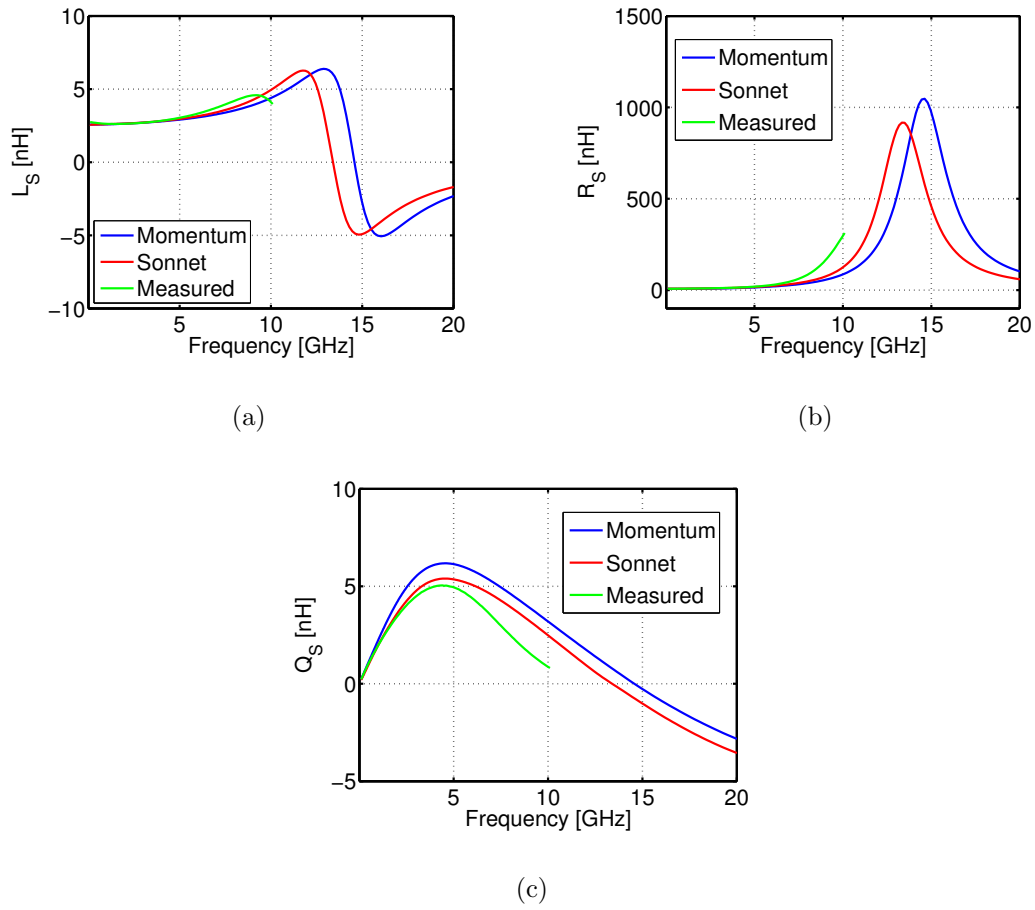


Figure 2.13: *Significant parameters of the 4.4-nH mutual inductor in the transformer-like configuration. ADS Momentum and Sonnet simulations. (a) Equivalent single-ended inductance. (b) Equivalent single-ended resistance. (c) Single-ended quality factor.*

Table 2.1: *Summary of the significant parameters of the 4.4-nH mutual inductor in the three considered configurations.*

(a) One-coil configuration					
	L_S [nH]	R_S [Ω]	f_{SR} [GHz]	Q_{peak}	Q_{5GHz}
Momentum	2.58	7	29	9.5	8.6
Sonnet	2.58	8	24.8	8.5	7.6
(b) Differentially-driven configuration					
	$L_{S\mathrm{d}}$ [nH]	$R_{S\mathrm{d}}$ [Ω]	f_{SRd} [GHz]	$Q_{\mathrm{peak(d)}}$	$Q_{\mathrm{5GHz(d)}}$
Momentum	8.9	14	7.52	7.7	4.4
Sonnet	8.9	16	6.81	6.2	2.6
(c) Transformer-like configuration					
	$L_{S\mathrm{x}}$ [nH]	$R_{S\mathrm{x}}$ [Ω]	f_{SRx} [GHz]	$Q_{\mathrm{peak(x)}}$	$Q_{\mathrm{5GHz(x)}}$
Momentum	2.58	7	14.6	6.2	6.1
Sonnet	2.58	8	13.4	5.4	5.4
Measured	2.75	7.5	–	5	5

2.4.6 1:$(1/\sqrt{2})$ transformer

This structure is used in the input network of the LNA to achieve input and noise matching as will be explained in Sect. 4.2.1. We want the transformer to provide an impedance transformation of a factor of 1/2, therefore in the case of an ideal transformer, we would need a winding ratio $n = 1/\sqrt{2}$. However, as we already saw in the foregoing discussion, the two windings are never perfectly coupled, and have a coupling factor $|k| < 1$. The relationships that hold between the electric parameters are:

$$\begin{cases} V_1 = s\mathrm{L}_1 I_1 + s\mathrm{M} I_2 = Z_{11} I_1 + Z_{12} I_2 \\ V_2 = s\mathrm{M} I_1 + s\mathrm{L}_2 I_2 = Z_{21} I_1 + Z_{22} I_2 \end{cases} \tag{2.16}$$

$$n = \sqrt{\frac{L_1}{L_2}} = \sqrt{\frac{\mathcal{I}m(Z_{11})}{\mathcal{I}m(Z_{22})}} \tag{2.17}$$

$$k = \frac{M}{\sqrt{L_1 L_2}} = \frac{\mathcal{I}m(Z_{21})}{\sqrt{\mathcal{I}m(Z_{11})\mathcal{I}m(Z_{22})}}, \tag{2.18}$$

where L_1 and L_2 are the self-inductances of the primary and secondary winding, respectively, and M is the mutual inductance between the two. V_1, I_1, V_2 and I_2 are the voltages and currents as in Fig. 2.14. The non-perfect coupling results in a different transformation ratio n'. If we model the transformer as illustrated in Fig. 2.15, the effective transformation ratio results in [24]

$$n' = \frac{L_1}{M} = \frac{n}{k}. \tag{2.19}$$

The structure was integrated stand-alone and measured on-wafer in the configuration illustrated in Fig. 2.14. The simulation were run considering the transformer as a 5-port device, with a center tap on the secondary winding that acted as the fifth terminal. The center tap is used in the LNA to provide biasing to the circuit. However, here are shown simulations run in the configuration of Fig. 2.14 in order to provide a comparison with the measurement results.

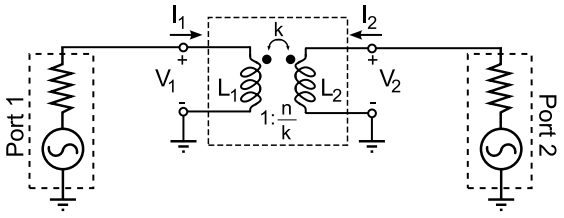


Figure 2.14: *Simulation and measurement setup of the transformer.*

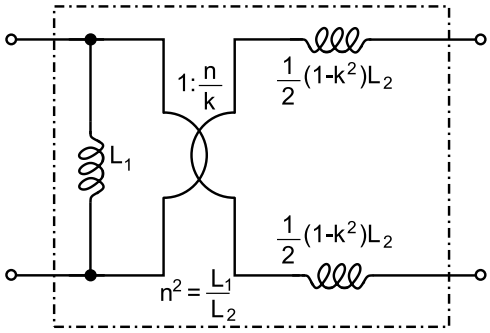
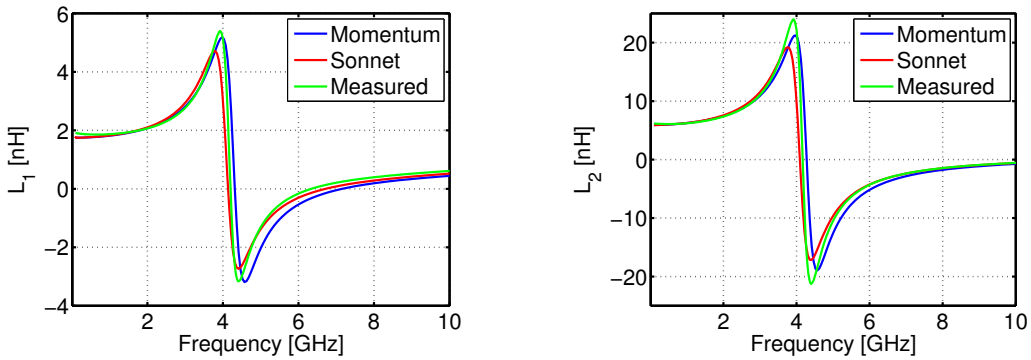


Figure 2.15: *Circuit model of a transformer with non-perfect coupling.*

Figs. 2.16–2.19 show the discussed parameters as extracted from Momentum and Sonnet simulations and from the measurements. The quality factors Q_1 and Q_2 are derived using

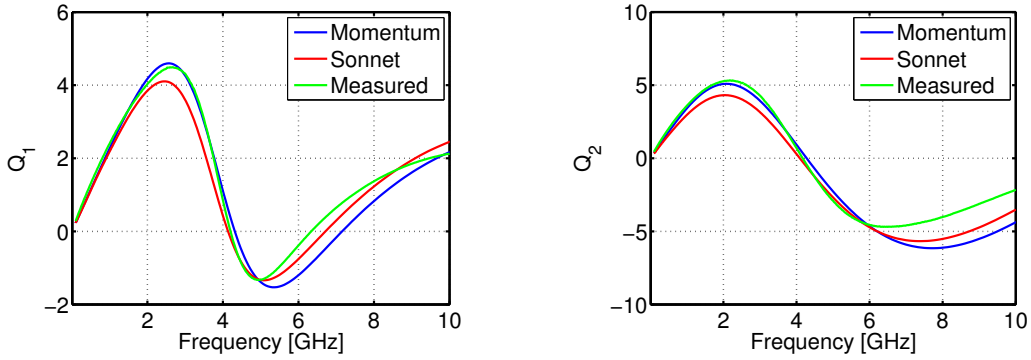
$$Q_1 = \frac{\mathcal{I}m(Z_{11})}{\mathcal{I}m(Z_{11})} \qquad \text{and} \qquad Q_2 = \frac{\mathcal{I}m(Z_{22})}{\mathcal{I}m(Z_{22})}.$$

Table 2.3 summarizes the simulated and measured values of L_1, L_2, n, k and n/k, as well as the maximum single-ended quality factors $Q_{1-\mathrm{pk}}$ and $Q_{2-\mathrm{pk}}$ of both windings. The self-resonance frequencies f_{SR1} and f_{SR2} are also reported.



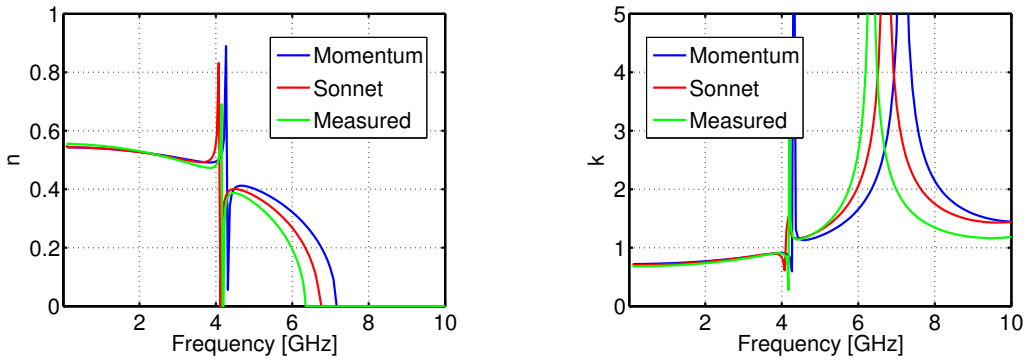
(a) (b)

Figure 2.16: *Self-inductances of the 1:(1/$\sqrt{2}$) transformer. (a) Primary coil. (b) Secondary coil.*



(a) (b)

Figure 2.17: *Single-ended quality factors of the 1:(1/$\sqrt{2}$) transformer. (a) Primary coil. (b) Secondary coil.*



(a) (b)

Figure 2.18: *Winding ratio and coupling factor. (a) Winding ratio. (b) Coupling factor.*

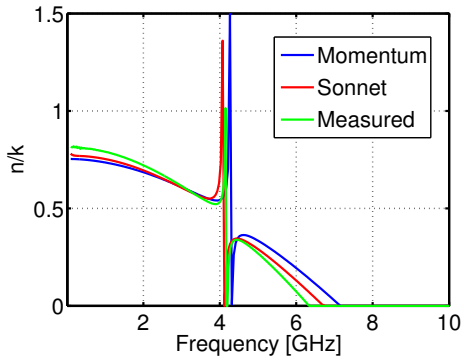


Figure 2.19: *Effective transformation ratio n' of the 1:$(1/\sqrt{2})$ transformer.*

Table 2.3: *Summary of the significant parameters of the 1:(1/$\sqrt{2}$) transformer.*

Single-ended parameters						
	L_1 [nH]	L_2 [nH]	$Q_{1-\mathrm{pk}}$	$Q_{2-\mathrm{pk}}$	f_{SR1} [GHz]	f_{SR2} [GHz]
Momentum	1.75	5.9	4.6	5.1	4.31	4.28
Sonnet	1.75	5.9	4.1	4.3	4.14	4.09
Measured	1.85	6.1	4.5	5.3	4.2	4.17

Coupling parameters			
	n	k	$n' = n/k$
Momentum	0.54	0.72	0.75
Sonnet	0.54	0.7	0.77
Measured	0.55	0.68	0.81

Chapter 3

Analysis of the Notch Filter

The operation of the notch filter is inspired by the image-rejection filter reported in [25] and is based on the series resonance of a reactive network. It works in current mode, as at the (series) resonance frequency f_N, the current is steered away from the signal path, so that a notch appears in the transfer function of the LNA. Fig. 3.1 shows how this goal can be accomplished. The schematic shows a part of a cascode amplifier (M_1, M_3 and L_S), at which the impedance Z_N, representing the notch filter, is attached. At f_N, $Z_N = 0$, so the current is steered from the load to ground.

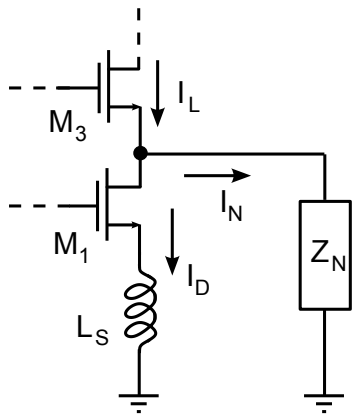


Figure 3.1: *Conceptual schematic of the notch filter.*

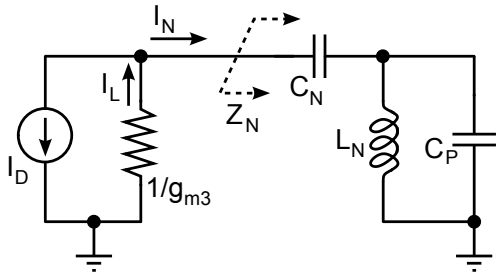
3.1 Choice of the topology

A design approach that makes use of a simple LC network with a single inductor, as done in [25], leads to the equivalent circuit sketched in Fig. 3.2(a). I_D is the drain current of the driver transistor of the amplifier (M_1 in Fig. 3.1), while g_{m3} is the transconductance of the cascode transistor M_3. The load resistance, as seen at the source of M_3, is then $1/g_{m3}$. The capacitance C_P is the parasitics contribution. The transfer function G_F of this simplified model is

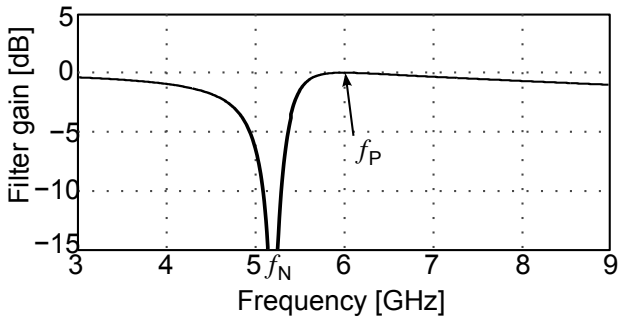
$$G_F = \frac{I_L}{I_D} = \frac{g_{m3} Z_N}{1 + g_{m3} Z_N}. \tag{3.1}$$

The equivalent impedance Z_N, as indicated in Fig. 3.2(a), is

$$Z_N = \frac{1 + s^2 L_N (C_N + C_P)}{s C_N (1 + s^2 C_P L_N)}. \tag{3.2}$$



(a)



(b)

Figure 3.2: *Single-inductor notch filter. (a) Ideal schematic. (b) Transfer function.*

With respect to a series LC circuit, it features an additional parallel resonance at a frequency f_P slightly higher than the notch frequency f_N. The expressions of these two frequencies are:

$$f_P = \frac{1}{2\pi\sqrt{C_P L_N}} \tag{3.3}$$

$$f_N = \frac{1}{2\pi\sqrt{L_N(C_N + C_P)}}. \tag{3.4}$$

Eq. (3.5) gives the expression of G_F, which is plotted in Fig. 3.2(b).

$$G_F = \frac{1 + s^2 L_N(C_N + C_P)}{1 - s\frac{C_N}{g_{\mathrm{m3}}} + s^2 L_N(C_N + C_P) - s^3\frac{C_N C_P L_N}{g_{\mathrm{m3}}}}. \tag{3.5}$$

The pole caused by the additional parallel resonance falls out-of-band and causes a peak on the gain at that frequency. As $f_P > f_N$, this makes the roll-off of the notch steeper on its upper side rather than on the lower side. This is usually good in narrow-band systems, where f_P can be designed to be at the frequency of the wanted signal, while the notch can be put at the frequency of the image signal. However, the spectrum of Mode #1 UWB systems, for which this front-end is designed (i. e. 3–5 GHz), lies on frequencies lower than f_N, so a steeper roll-off on the lower side of the notch would be preferred so as to avoid degradation the in-band gain near the notch frequency.

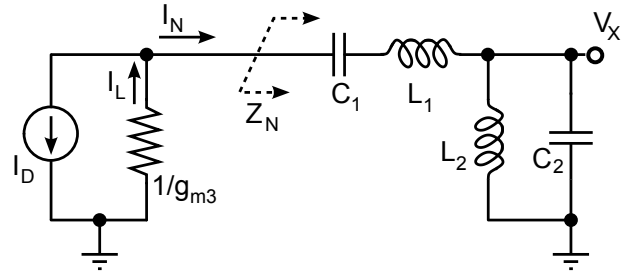
This can be achieved with the double-inductor topology of Fig. 3.3(a). As Fig. 3.3(b) shows, this network features two series resonances, at frequencies f_1 and f_2, and a parallel resonance at f_P, which now falls in-band. The analytical expressions of Z_N, f_1 and f_2, as well as the expression of I_L/I_D, are reported in equations (3.6)–(3.9). f_P has the same expression as (3.3), with C_P and L_N replaced by C_2 and L_2, respectively.

$$Z_N = \frac{1 + s^2(C_1L_1 + C_1L_2 + C_2L_2) + s^4C_1C_2L_1L_2}{sC_1(1 + s^2C_2L_2)} \tag{3.6}$$

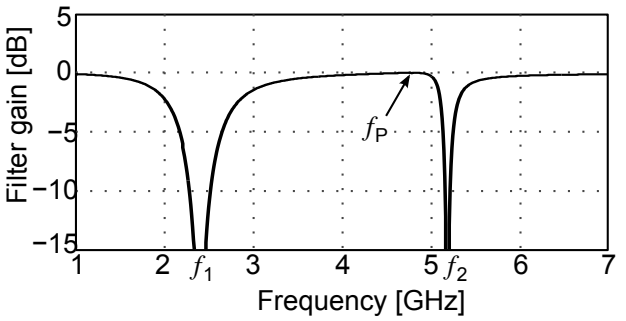
$$f_{1,2} = \frac{1}{2\pi}\sqrt{\frac{C_1L_1 + C_1L_2 + C_2L_2 \pm \sqrt{\Delta_{LC}}}{2C_1C_2L_1L_2}} \tag{3.7}$$

$$\Delta_{LC} = C_1^2L_1^2 + C_1^2L_2^2 + C_2^2L_2^2 + 2C_1^2L_1L_2 + 2C_1C_2L_2^2 - 2C_1C_2L_1L_2 \tag{3.8}$$

$$G_F = \frac{I_L}{I_D} = \frac{1 + s^2(C_1L_1 + C_1L_2 + C_2L_2) + s^4C_1C_2L_1L_2}{1 - s\frac{C_1}{g_{m3}} + s^2(C_1L_1 + C_1L_2 + C_2L_2) - s^3\frac{C_1C_2L_2}{g_{m3}} + s^4C_1C_2L_1L_2}. \tag{3.9}$$



(a)



(b)

Figure 3.3: *Double-inductor notch filter. (a) Ideal schematic. (b) Transfer function.*

We choose to set by design f_1 to the 2.4 GHz ISM band, while f_2 is made tunable around 5.2 GHz, to take care of the IEEE 802.11a blockers. f_P is placed near 4.8 GHz, so that it can be effective in keeping the roll-off steep on the lower side of the notch at f_2. Doing so, the network with two inductors offers a better performance for this kind of application at the price of a higher area consumption, allowing for a smaller degradation of the in-band gain compared to the single-inductor topology.

To better understand how the single components are involved in determining f_1 and f_2, we can perform a simplified analysis, considering the case in which $L_1 \gg L_2$. In this case, Eqs. (3.6) and (3.7) can be written as:

$$Z_N = \frac{[1 + sC_1(L_1 + L_2)]\,[1 + sC_2(L_1 \parallel L_2)]}{sC_1(1 + s^2 C_2 L_2)} \tag{3.10}$$

$$f_1 = \frac{1}{2\pi C_1(L_1 + L_2)} \tag{3.11}$$

$$f_2 = \frac{1}{2\pi C_2(L_1 \parallel L_2)}. \tag{3.12}$$

We can see that f_1 is controlled by C_1 and L_1, while f_2 depends mostly on C_2 and L_2. We will see in the next Sect. that we need $L_1 \approx 3L_2$, so this approximation does not hold in this specific case. However it gives a glimpse of how the notch frequencies behave with respect to the values of the components.

3.2 Choice of the components

In order to compensate for the resistive losses of the passive components of the filter, an active network is needed. We assume that the losses related to the inductors are dominant on those given by the capacitors. Then, they can be approximated by a resistance in series with each inductor (as seen in Sect. 2.2), while the compensation circuit can be modeled as the equivalent negative resistance synthesized by the active network. Fig. 3.4(a) shows the equivalent circuit, where R_1 and R_2 are the parasitic resistances of L_1 and L_2, respectively, while R_N is the synthesized negative resistance. The transfer function of this circuit is plotted in Fig. 3.4(b). As R_N can fully compensate for the losses only at a single frequency [9], its value is set to be mostly effective at the higher notch frequency.

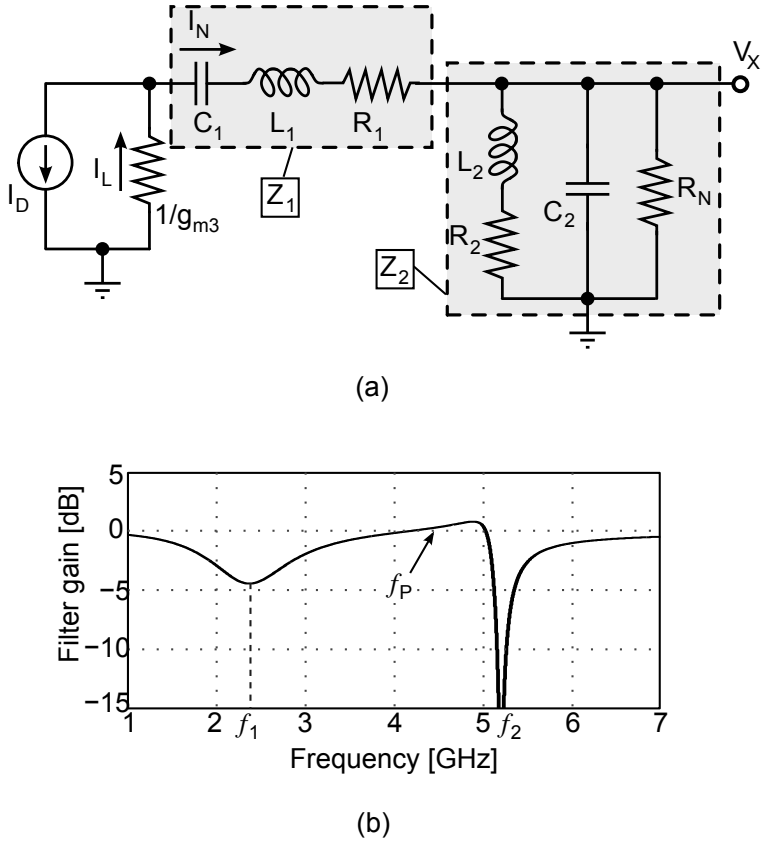


Figure 3.4: *Double-inductor notch filter with losses and active compensation. (a) Ideal schematic. (b) Transfer function.*

Moreover, it should be noted that if R_N is set to compensate the lower notch, the higher one becomes overcompensated, causing instability.

R_N will be synthesized by an active circuit, whose power consumption grows as the losses become higher. As the losses themselves depend on the values of the passive components, the reactive network must be optimized for low power consumption. The following analysis will explain how the optimization can be achieved.

We have four unknowns (the four reactive components) and two boundary conditions (the two notch angular frequencies $\omega_1 = 2\pi f_1$ and $\omega_2 = 2\pi f_2$). Thus, we have two degrees of freedom. The choice of the first degree of freedom falls upon the (angular) frequency of the in-band parallel resonance $\omega_P = 1/\sqrt{C_2 L_2}$ as it is easily related to the values of the components and it is a very significant parameter, because it is responsible for the steepness of the roll-off. The other

degree of freedom is chosen, somewhat arbitrarily, as L_1. In this way, the values of C_1, C_2 and L_2 can be expressed as functions of $f_P = \omega_P/2\pi$ and L_1, on the basis of the ideal network of Fig. 3.3(a), as follows:

$$C_1 = \frac{\omega_P^2}{L_1\omega_1^2\omega_2^2} \tag{3.13}$$

$$C_2 = \frac{1}{L_1(\omega_1^2 + \omega_2^2 - \omega_P^2 - \frac{\omega_1^2\omega_2^2}{\omega_P^2})} \tag{3.14}$$

$$L_2 = \frac{L_1(\omega_1^2 + \omega_2^2 - \omega_P^2 - \frac{\omega_1^2\omega_2^2}{\omega_P^2})}{\omega_P^2}. \tag{3.15}$$

Figs. 3.6(a)–(c) show contour plots of such values obtained with MatLab.

A first-order estimation of the required inductance values leads to $L_1 \approx 4$ nH and $L_2 \approx 1$ nH. The quality factors $Q = 2\pi f L/R$ of both inductors for $f = f_2$ have been extracted by means of EM simulations and are $Q_1 = 5$ and $Q_2 = 7$. [1] We consider them constant for inductance values similar to the estimated ones. This gives a rough relationship between the inductors and their own parasitic resistances. After introducing the parasitic resistances, the value of conductance $G_N = 1/R_N$ that cancels the losses at f_2 can also be computed in function of f_P and L_1. From Fig. 3.4, we write the expressions of Z_1 and $Y_2 = 1/Z_2$:

$$Z_1 = \frac{1}{sC_1} + sL_1 + R_1 \tag{3.16}$$

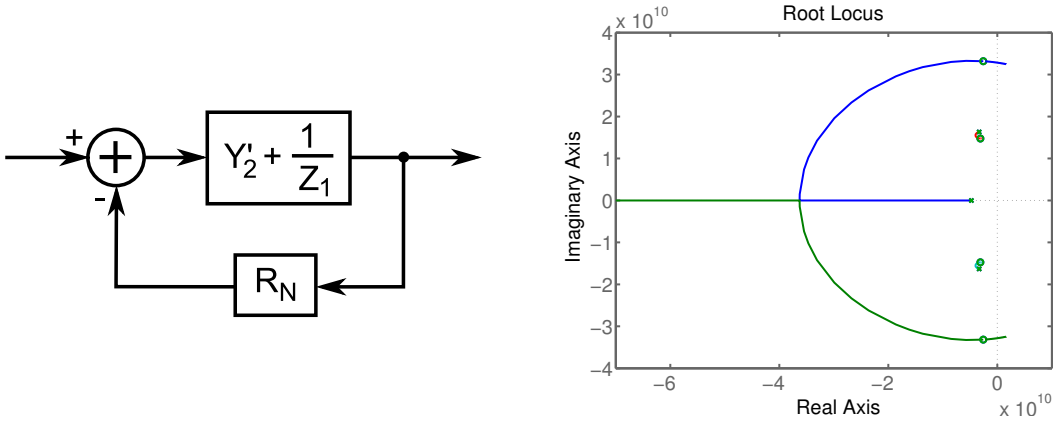
$$Y_2 = sC_2 + \frac{1}{sL_2 + 1/R_2} + G_N = Y_2' + G_N. \tag{3.17}$$

The condition that ensures an ideal notch, i. e., a notch with infinite depth, is $Z_N = Z_1 + 1/Y_2 = 0$. $\mathcal{I}m(Z_N) = 0$ derives from the lossless circuit, while $\mathcal{R}e(Z_N) = 0$ means that the losses are compensated (as seen before, this can happen only at a single frequency). The condition $Z_N = 0$ can be rearranged as

$$Y_2' + \frac{1}{Z_1} = \frac{1}{R_N}, \tag{3.18}$$

which is the expression of he root locus of $Y_{\mathrm{RL}} = Y_2' + 1/Z_1$, as Fig. 3.5(a) shows.

[1] The quality factors shown in Sect. 2.4 refer to the final implementations of the inductors and not to this first-order estimate



(a) (b)

Figure 3.5: *Calculation of R_N with the root-locus technique. (a) Block diagram. (b) MatLab plot of the root locus.*

The root locus tells us the position on the complex plane of the closed-loop poles p_{CL} of the system in Fig. 3.5(a), which are, in turn, the zeroes of Z_N, as a function of R_N. Now, in order for the notch to have the maximum depth, the zeroes of Z_N must be purely imaginary (so that the absolute value of Z_N drops to zero). Fig. 3.5(b) shows a MatLab plot of an example of the root locus for positive values of R_N, with a little extension into negative values to show the crossing of the imaginary axis by the locus plot. The two long blue and green lines represent the poles of Y_{RL} (i.e., the zeroes of Z_N) at f_2, while the two shorter lines (in red and light blue, barely visible) are the poles at f_1.

In conclusion, the values of R_N that maximize the depth of the notch are the ones that satisfy

$$\mathcal{R}e(p_{\mathrm{CL}}(R_N)) = 0. \tag{3.19}$$

The resulting $G_N(f_P, L_1) = 1/R_N$, obtained with the help of MatLab, is given in Fig. 3.6(d). A higher absolute value of G_N indicates a higher power consumption. In this way we were able to find a relationship that binds each given set of components to the power needed to compensate its losses (in terms of G_N). Then, we can choose the values of the passive components that need a lower power consumption.

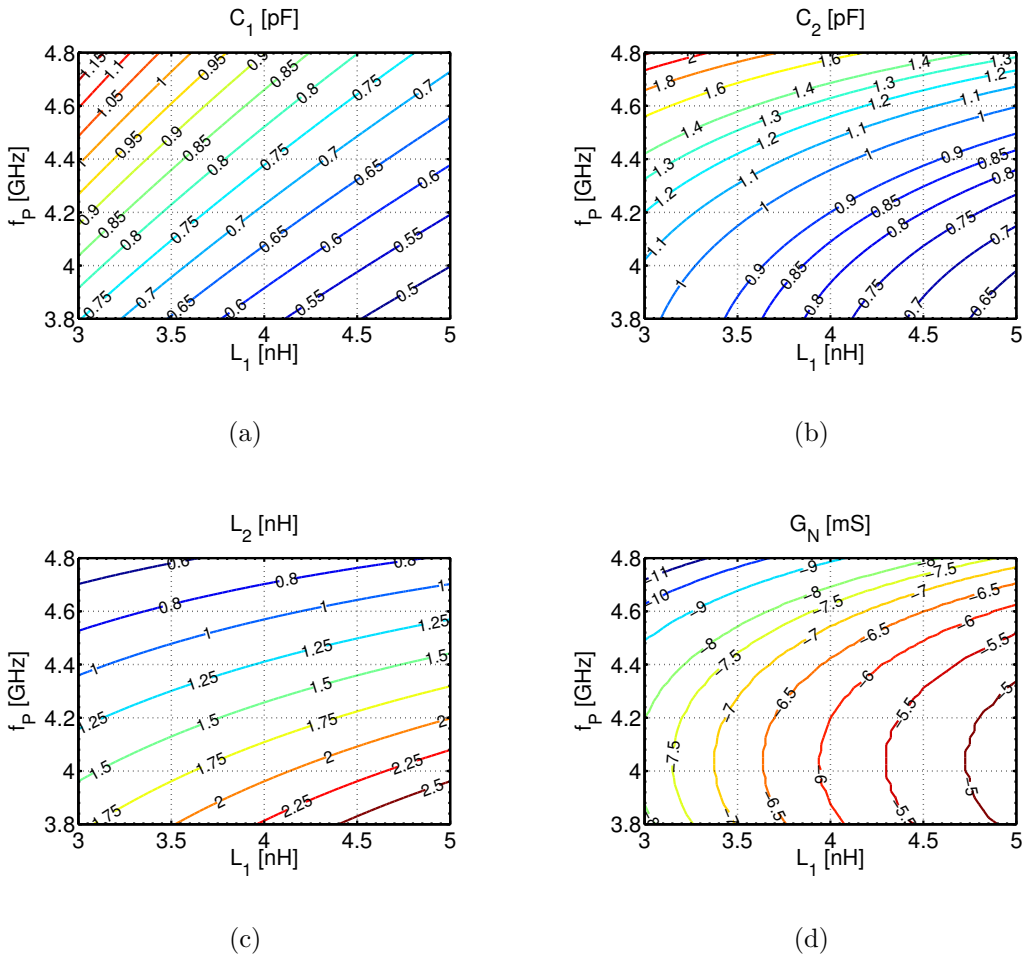


Figure 3.6: *Values of passive components vs. f_P and L_1. (a) C_1 [pF]. (b) C_2 [pF]. (c) L_2 [nH]. (d) G_N [mS].*

Although the main target of this analysis is to optimize the network for minimum power consumption, we also have to pay attention to other constraints. First of all, the area consumption: the bigger the values of the passives, the larger the area they occupy. This would lead to choose the capacitances on the lower right corner in Figs. 3.6(a) and 3.6(b), where the power consumption (Fig. 3.6(d)) is minimum, as well. At the same time, though, that choice maximizes both L_1 and L_2 (Fig. 3.6(c)). L_2 is minimum on the very opposite corner. Furthermore, f_P must be close to the upper edge of the band (i. e. 4.8 GHz) to keep the roll-off of the filter steep. On the other side, if f_P is too close to the upper limit, the notch will become too narrow, and it will be difficult to tune. A reasonable trade-off is near the upper right corner. The design choice is $L_1 = 4.5$ nH and $f_P = 4.5$ GHz.

The complete list of the calculated values is reported in Table 3.1.

Table 3.1: *Values of the filter components.*

C_1 [pF]	C_2 [pF]	L_1 [nH]	L_2 [nH]	f_P [GHz]	G_N [mS]
0.7	1.0	4.5	1.25	4.5	-6.1

3.3 Frequency tuning and current calibration

In the foregoing analysis we assumed that the notch filter was tuned at a fixed frequency. The blocker, though, is not at a single frequency, but may show up in a range that goes from 4.9 to 5.8 GHz (considering IEEE 802.11a interferers). As the notch filter is a narrow-band system, it will not be able to provide for a high attenuation in the entire Wi-Fi band at the same time. Therefore, a frequency tuning scheme must be implemented. To do this, we make the capacitors variable. Fig. 3.7 shows the dependence of the notch frequency f_2 on the values of the capacitors. For each (C_1, C_2) pair, f_2 is calculated on the basis of the circuit of Fig. 3.4(a), with the values of G_N that maximize the depth of the notch (which are plotted in Fig. 3.8). f_2 is more sensitive to variations on C_2 rather than on C_1: a variation of $\pm 20\%$ of C_2 leads to a tuning range more than 1-GHz wide, while a $\pm 20\%$ variation in C_1 makes f_2 change in a range of about 100 MHz. As a consequence, C_2 is selected as the variable capacitance. This result agrees with

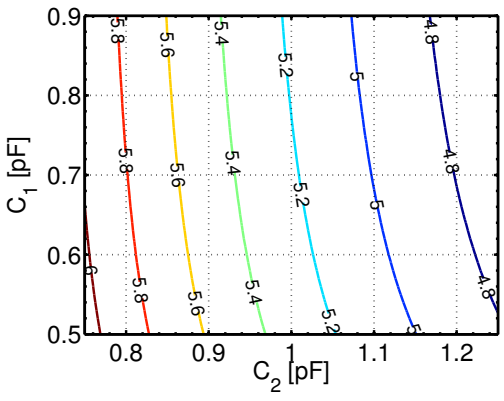


Figure 3.7: *Notch frequency f_2 [GHz] vs. variation of capacitors.*

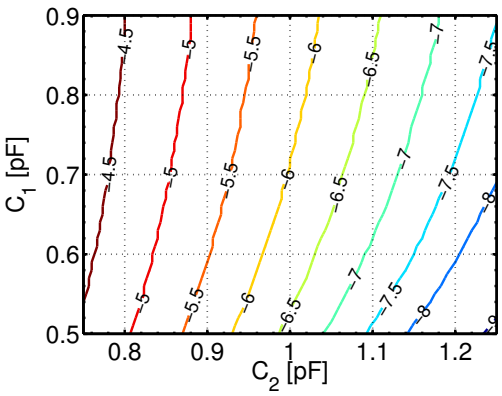


Figure 3.8: *Negative conductance G_N [mS] needed for loss compensation vs. variation of capacitors.*

the simplified analysis given at the end of Sect. 3.1, according to which f_2 is more sensitive on C_2 rather than on C_1. The range of variation of C_2 must be doubled if we take into account the process spreads, which can cause a further $\pm 20\%$ variation in C_2 and C_1. Inductors, on the other hand, are very large structures, and the uncertainties on their behavior due to process spreads may be neglected with respect to the ones coming from the capacitors. As mentioned above, the target of our filter is the Wi-Fi signal in the band from 5 to 6 GHz. In particular, we focus on the lower US band, made of two contiguous, 100-MHz wide, subbands from 5.15 to 5.35 GHz. These bands are the closest to the Mode #1 UWB band, and are the most difficult to deal with. So, we decide to tune the filter in the 5.15–5.35 GHz frequency range, and design it considering the variations on C_1 and C_2 as due to process spreads.

At the input of the receiver chain, many blockers may appear, and we aim at mitigating the one with the highest power. However, the interferer must be sensed in some way, so that we can tune the notch on top of it. To do so, we refer to Fig. 3.4(a) and observe that the transfer function

$$\Psi_A = \frac{V_X}{I_D} = -\frac{s^2 \frac{C_1 L_2}{g_{m3}}}{1 - s\frac{C_1}{g_{m3}} + s^2(C_1 L_1 + C_1 L_2 + C_2 L_2) - s^3 \frac{C_1 C_2 L_2}{g_{m3}} + s^4 C_1 C_2 L_1 L_2} \tag{3.20}$$

is bandpass. By comparing (3.20) and (3.9) we can also notice that Ψ_A is complementary to G_F if C_1/g_{m3} is small enough, as the poles of Ψ_A get close to the

zeroes of G_F. Even in the presence of lossy components and active compensation, this relationship does not change in a significant way, as depicted in Fig. 3.9.

In this way, we can change the value of C_2 to shift the frequency of the notch over the designed frequency range and measure the corresponding signal power at node V_X. The filter will be tuned to the frequency at which the detected signal strength is maximum. The power of the signal can be measured with a received signal strength indicator (RSSI), which is commonly present in any RF transceiver.

If C_2 is implemented with a varactor, the notch frequency can be moved continuously in frequency, and, in principle, one can always detect the strongest interferer. If C_2 is made of a capacitor array, instead, the search for the blocker is performed in discrete steps. This raises the important issue of determining the width of the frequency step. As we mentioned above, the focus is on the two lower US sub-bands of 802.11a, whose channel bandwidth is 20 MHz. The network derived from the foregoing circuit analysis produces a notch that can attenuate at least 10 dB over a bandwidth of 100 MHz. The notch is then wide enough to adequately attenuate an entire channel. Without loss of accuracy for this analysis, we consider a box approximation of the notch, in which the attenuation is 10 dB over a 100 MHz bandwidth and zero elsewhere, so that each tuning of the filter is represented by a different box. If the 20-MHz blocker is not fully included into a certain box (because it falls at its edge), then we

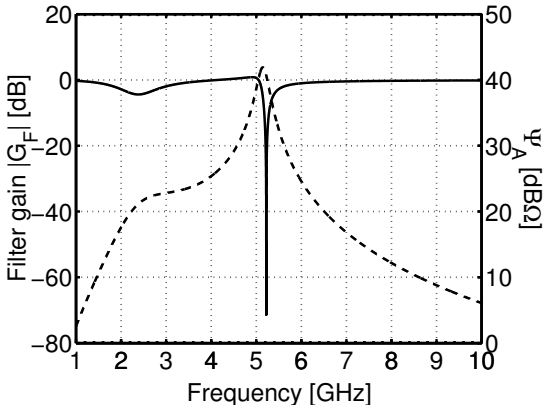


Figure 3.9: *Transfer function $\Psi_A = V_X/I_D$ (dashed line, right axis) and notch filter transfer function (solid line, left axis).*

want it to fall entirely into the adjacent one. To do so, the two adjacent boxes must overlap by at least the width of the blocker. If not, there will always be a worst case in which the blocker will not be completely included in either box. Therefore, the frequency step must be 80 MHz or less, which corresponds to a C_2 unit capacitance of about 40 fF (see Fig. 3.7). In this way, an attenuation of at least 10 dB will be granted over each 20-MHz channel.

A variation on C_2, though, causes a spread not only on the notch frequency f_2, but on G_N, as well, as Fig. 3.8 points out. A fluctuation of $\pm 20\%$ on C_2 produces a spread on G_N of about $\pm 30\%$. This means that, for each tuning of the filter, a different bias current is needed for the active circuit to maximize the notch depth. Therefore, a current calibration is needed, as well. In order to perform this task, we consider the filter as made of the series of the two impedances Z_1 and Z_2, with the negative resistance included within Z_2 (cf. Fig. 3.4(a)). Then, we reconfigure the filter into an oscillator, as Fig. 3.10 illustrates. The filter has its deepest notch when the zeroes of the equivalent impedance $Z_N = Z_1 + Z_2$ are on the imaginary axis of the complex plane. In the same way, the oscillator obtained from the reconfigured circuit starts up when the zeroes of the equivalent admittance $Y'_N = 1/Z_1 + 1/Z_2$ lie on the imaginary axis. If we write $Z_1(s) = n_1(s)/d_1(s)$ and $Z_2(s) = n_2(s)/d_2(s)$, we have:

$$Z_N(s) = \frac{d_2(s)n_1(s) + d_1(s)n_2(s)}{d_1(s)d_2(s)} \tag{3.21}$$

$$Y'_N(s) = \frac{d_1(s)n_2(s) + d_2(s)n_1(s)}{n_1(s)n_2(s)} \tag{3.22}$$

and we can see that they have the same zeroes. This holds in general, regardless

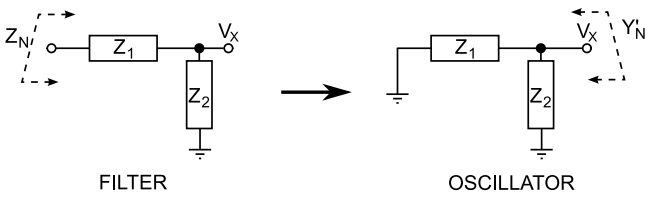


Figure 3.10: *Reconfiguration of the notch filter into an oscillator for calibration.*

of what Z_1 and Z_2 are actually made of. This means that the condition that maximizes the depth of the notch is the same that starts the oscillation in the reconfigured circuit. So, we can reconfigure the filter into an oscillator and then increase its bias current until we detect the oscillation. The detection can be performed with the same RSSI we use for the frequency tuning, so we can grant the stability of the notch filter, as unwanted oscillations can be detected. If we control the bias current and the value of C_2 with a digital word, the calibration loop can be closed in the digital domain.

3.4 Specifications for auxiliary circuits

Apart from the frequency tuning step, a second issue arises from the use of a discrete tuning: the RSSI must have a certain minimum resolution in order to detect the difference between the power sensed at two adjacent steps and decide which is the highest. To perform this kind of analysis, let us call f_{S0} and $f_{S1} = f_{S0} + 80$ MHz two adjacent notch frequency steps and let us consider a blocker whose center frequency f_B lies in between them as in Fig. 3.11. The input blocker has a bandwidth B and is considered as provided by the current source I_D. Its power, referred to a 1-Ω resistance, is then $P_B = |I_D|^2 \cdot 1\Omega$. Let us also call P_0 the power at the node V_X when the filter is tuned to f_{S0} and P_1 the power at V_X when the filter is tuned to f_{S1}. Both P_0 and P_1 are referred to a 1-Ω resistance, too, and depend on P_B, B and on $f_B - f_{S0}$. The power transfer

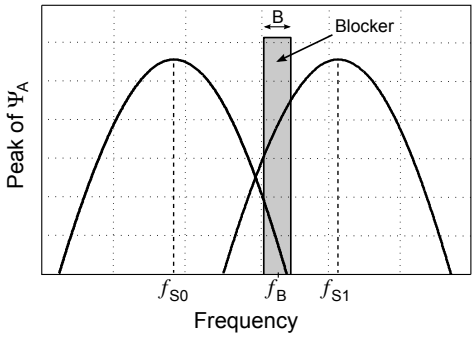


Figure 3.11: *Peaks of two adjacent positions of the sensing function Ψ_A (qualitative plot). $f_{S1} - f_{S0} = 80$ MHz.*

function from the input to the node V_X is then $|\Psi_A/1\Omega|^2$. We consider then the figure of merit P_A as the ratio of $P_0 - P_1$ to the maximum output power that can appear at V_X. The expression of P_A is given in (3.23), where $|\Psi_A/1\Omega|_{\max}$ is the peak value of $|\Psi_A/1\Omega|$.

$$P_A = \frac{P_0 - P_1}{|\Psi_A/1\Omega|^2_{\max} P_B} \tag{3.23}$$

Fig. 3.12 shows a contour plot of the function P_A: on the x axis there is $\Delta f_B = f_B - (f_{S1}+f_{S0})/2$, while on the y axis there is the bandwidth of the blocker. The most critical frequency is the one at which P_A is the same whether the filter is tuned to f_{S0} or to f_{S1}. To derive a specification on the minimum resolution of the RSSI, consider now Fig. 3.13, which plots the difference $\Delta G_F = |G_{F1}|_{dB} - |G_{F0}|_{dB}$, where $|G_{F1}|$ is the gain of the filter when it is tuned to f_{S1} and $|G_{F0}|$ is the gain of the filter when it is tuned to f_{S0}. On the left hand of the plot, the blocker undergoes a higher attenuation if the filter is tuned to f_{S0}. Vice versa, on the right hand of the plot the attenuation is higher if we tune the filter to f_{S1}. We consider ΔG_F negligible if $|\Delta G_F| \leq 3$ dB (shaded stripe in Fig. 3.13). This means that if -2.6 MHz $\leq \Delta f_B \leq 11.4$ MHz, we do not mind whether the filter is tuned to f_{S0} or to f_{S1}, because the attenuation is almost the same. So, in order to tune the filter to the strongest blocker with a tolerance of 3 dB on the attenuation, we must be able to detect it with a frequency tolerance of $|\Delta f_B| \leq 2.6$ MHz, which

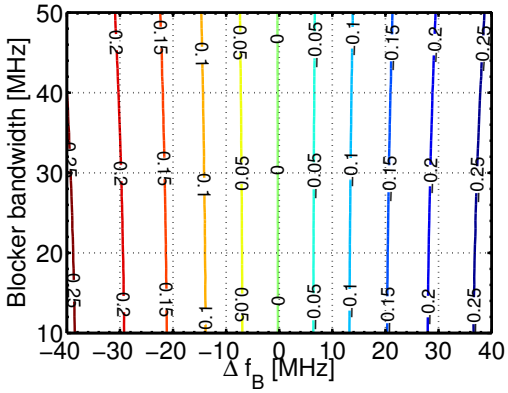


Figure 3.12: *Difference between the power sensed by Ψ_A when tuned to two adjacent steps. The difference is relative to the maximum output power that can appear at V_X.*

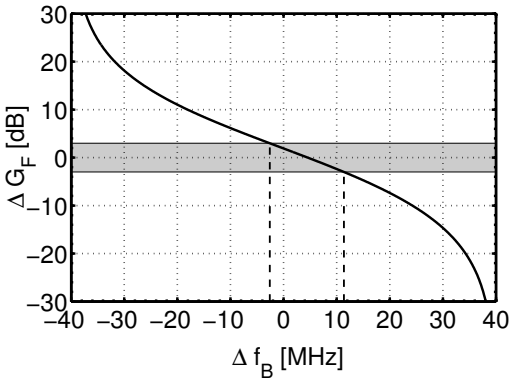


Figure 3.13: *Difference in the gain of the notch filter between two neighbor positions.*

corresponds to $P_A = \pm 17.4 \times 10^{-3}$ in Fig. 3.12 for $B = 20$ MHz. Therefore, if we want the RSSI to detect the highest amount of power with a tolerance of 3 dB, it must have a minimum resolution of 1.74%, that is 6 bits. It is interesting to note that this strategy does not care whether the power actually comes from the strongest blocker or from several weaker ones. What matters (and is sensed) is the total amount of filtered power.

It must be also noted that the value of 6 bits just derived refers to a full-scale signal, and the dynamic range of the RSSI must be added to this value. Let us call $P_X = |\Psi_A/1\Omega|^2_{\max} P_B$ the maximum power that may appear at V_X with an input power P_B (i.e., the denominator of (3.23)). Let us also call P_{RSSI} the maximum signal power processable by the RSSI and $P_{\mathrm{X,max}} = |\Psi_A/1\Omega|^2_{\max} P_{\mathrm{B,max}}$ the maximum power that may appear at its input, with the obvious meaning of $P_{\mathrm{B,max}}$. The foregoing analysis is carried on in the case that $P_{\mathrm{RSSI}} = P_X$. However, if we assume $P_{\mathrm{RSSI}} = P_{\mathrm{X,max}}$ and $P_X < P_{\mathrm{RSSI}}$, the difference $P_0 - P_1$ may fall below the resolution of the RSSI even though $|\Delta G_F| > 3$ dB, possibly causing a failure in determining the highest blocker. Therefore, the resolution must be increased by a sufficient number of bits, i.e. the dynamic range of the RSSI. An example will help clarify this point. Let us suppose that $P_{\mathrm{RSSI}} = P_{\mathrm{X,max}} = 0$ dBm. This means that the resolution of the 6-bit RSSI is -18 dBm. Consider then a blocker with bandwidth B = 20 MHz and Δf_B = -20 MHz such that $P_X = P_{\mathrm{X,max}} = 0$ dBm. From Fig. 3.13 we see $\Delta G_F = 11$ dB, while from Fig. 3.12 we have $P_A = 0.14$. This means that $P_0 - P_1$ = -8.54 dBm, which is well above the resolution of the

RSSI. However, if the blocker has, e.g., a power such that P_X = -12 dBm, then ΔG_F remains as before (i.e. 11 dB), but now $P_0 - P_1$ = -20.54 dBm, below the resolution of the RSSI. In the latter case, the RSSI will not be able to decide between the two positions even though $\Delta G_F > 3$ dB. Therefore the resolution of the RSSI must be increased by a number of bits that takes into account the dynamic range of the RSSI itself.

A further consideration must be made upon the speed of the tuning cycle. In a scenario where the UWB system coexists with a single 802.11a network, we can assume that the WLAN operates on a single, 20-MHz wide, channel. In this situation, the filter will have to be tuned only once. If the WLAN channel of operation changes, or another network appears, the quality of the UWB signal (which can be measured at system level) will be degraded, and a tuning cycle will be triggered. The speed of the tuning cycle will depend on the speed of the digital circuit that implements the algorithm, but its realization goes beyond the scope of this work. However, we can make a supposition based on the format of the WLAN transmission frame [26]. The frame, in addition to the coded data, contains a preamble, basically used for receiver synchronization, and a "SIGNAL" OFDM symbol, which provides the receiver with some information on the transmission rate and the length of the frame. The duration of the preamble is 16 μs and the duration of the "SIGNAL" symbol is 4 μs. Assuming that the preliminary information (preamble + "SIGNAL") is a small part of the transmitted frame, it is reasonable to expect the tuning of the filter to set up in the preamble + "SIGNAL" time. So the target set up time of the tuning algorithm is 20 μs. As regards the calibration routine, instead, we do not care much about its speed, as it is supposed to be performed *una tantum* at start up.

3.5 Conclusions

In summary, a thorough analysis of the notch filter has been carried out and the values of its components has been chosen so as to provide a good trade-off between area and power consumption. Assuming that C_2 and the bias current of the filter are controlled by digital words, an algorithm for current calibration and frequency tuning has been analyzed and proposed, too. It acts as follows: at start-up, for each value of C_2 we reconfigure the filter into an oscillator and

detect the current that makes it oscillate. Then, the corresponding digital words pair is stored into a memory register and recalled when necessary. This performs the current calibration. During normal operation, the frequency tuning can be triggered: by acting on C_2, the passband of the sensing function Ψ_A is shifted along the tuning range and is tuned to the frequency at which the maximum power is detected at node V_X. Because of temperature drift, the calibration may deteriorate, but a new calibration cycle may be triggered when required.

Chapter 4

Design of the Building Blocks

We already saw in Chapter 1 that in wideband systems the architecture of choice is the homodyne, or direct-conversion, receiver because of the lack of the image problem and because in this case the flicker noise is not an issue. Therefore, as UWB sub-bands have a bandwidth of 528 MHz, the direct-conversion receiver is chosen in this work, as well. A comprehensive block diagram of the receiver is given in Fig. 4.1: a differential topology is employed because of its higher immunity to common mode disturbances. The circuit is intended for the operation in the first three sub-bands of the UWB spectrum (cf. Sect. 1.3), that is from 3.1 to 4.8 GHz, also called Mode #1.

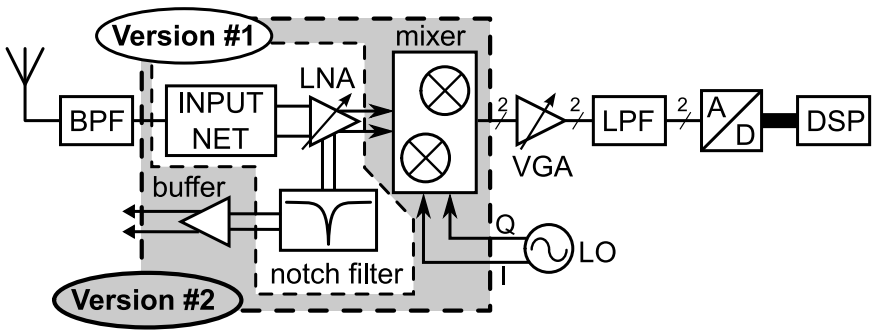


Figure 4.1: *Block diagram of the wide-band receiver.*

4.1 General considerations

As we already mentioned, this work has been developed in a two-step fashion in order to highlight and verify different facets of the design. Therefore, two versions of the front-end were implemented. The first version comprises a low noise amplifier with a transformer-based input-matching network, the notch filter and a buffer to drive the pad capacitances at the output [12]. These blocks are inside the white dash-box in Fig. 4.1. The second version expands the previous one to make up a front-end by adding a couple of double-balanced mixers at the output of the LNA and an additional buffer in order to have access to the auxiliary node of the notch filter for measurement purposes [13]. The two mixers are needed to recover both the I and Q channels from the OFDM signal. However, only one of these channels is output. Nonetheless, we decided to insert both mixers in the circuit in order to provide the LNA with a load as much close to the real one as possible. In this second version, the LNA has also a 3-step variable gain feature to improve the receiver performance. The blocks inside the shaded dash-box in Fig. 4.1 are included in this version only.

In both versions, the output buffer is matched to the 50-Ω impedance of the measurement instrument.

4.2 Low-noise amplifier

In both versions, the LNA is based on a cascode stage with an inductive source degeneration, which can provide a simultaneous input and noise matching, as seen in Chapter 1. The LNA also features an input network based on a transformer, extending what reported in [27] to a wide-band fashion in order to obtain a wide-band input and noise matching.

4.2.1 Transformer-based input network

The input network is designed as a two-section ladder network. By embedding a transformer, we can exploit the flux leakage to implement the two gate inductances while the shunt inductance is given by the self-inductance of the primary coil. This behavior was already mentioned in Sect. 2.4.6 and is shown in Fig. 4.2.

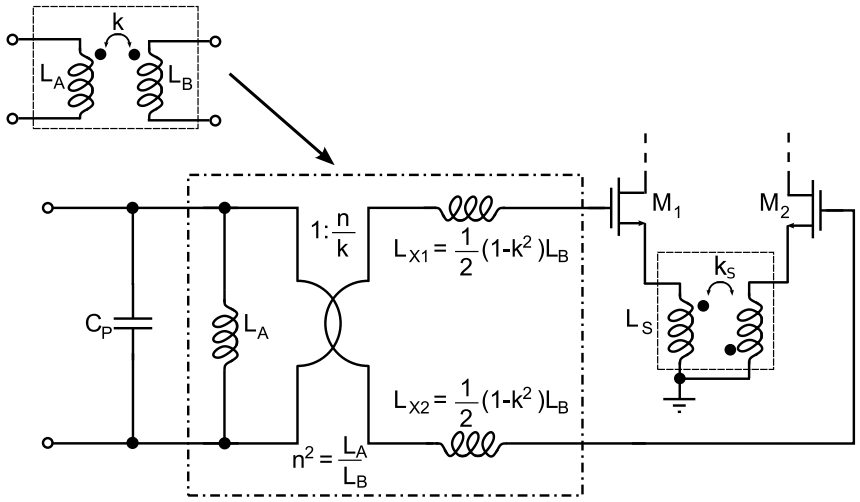


Figure 4.2: *Transformer-based input network.*

L_A and L_B are the self-inductances of the primary and secondary windings, respectively, while k is the coupling factor between the two coils. The equivalent inductances L_{X1} and L_{X2} appear because of the flux leakage and are related to L_B and k by the following:

$$L_{X1,2} = \frac{1}{2}(1 - k^2)L_B. \tag{4.1}$$

In this way, L_{X1} and L_{X2} can be used as series gate inductances. Thus, the transformer serves as three coils with only a single structure, saving a lot of area. Moreover, the impedance transformation associated to the operation of the transformer can be exploited to improve the noise performance, as the noise figure (NF) is inversely proportional to the source resistance [18]. Finally, the transformer can be used as a balun, so that, by simply connecting one of the terminals of the primary coil to ground, we can also perform the needed conversion from the single-ended antenna to the differential circuit.

The capacitance C_P in Fig. 4.2 includes both the parasitic capacitances of the transformer and the ones coming from pad and ESD protections. In Table 2.3 of Sect. 2.4.6 we can see that the self-resonance frequency of the transformer is about 4 GHz, so the structure operates above the self-resonance. However, the transformer is not needed to be wide-band (with respect to the bandwidth of the LNA), just because the parasitic capacitances of the primary coil are embedded into the input network. In this way, the explicit capacitance used is $C_1 \approx 0.4$ pF.

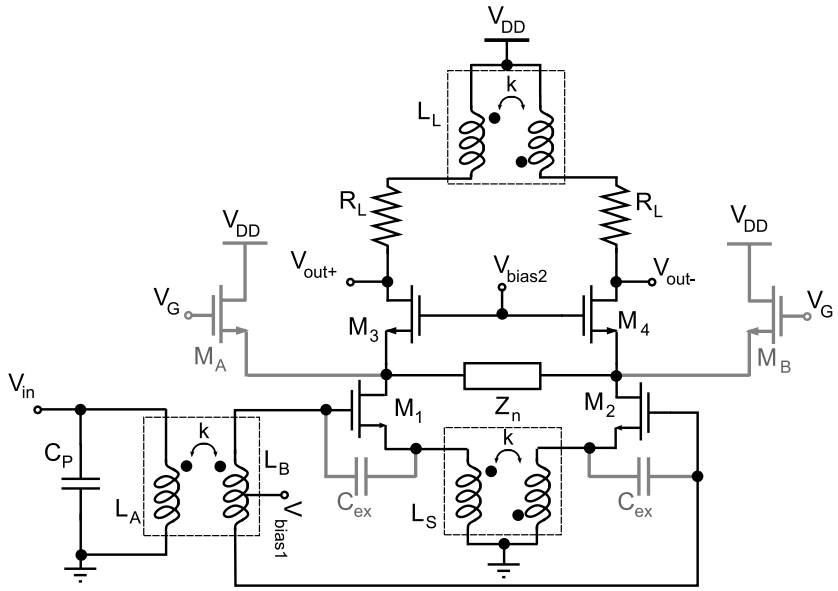


Figure 4.3: *Schematic of the LNA. Transistors M_A and M_B and capacitors C_{ex}, in gray lines, are included in the second version only.*

In the second version of the circuit, a different layout for the transistors was used. This caused a variation in the parasitic capacitances and resulted in a degraded input match. In order to return the S_{11} to reasonable values, explicit capacitors $C_{\mathrm{ex}} = 250$ fF (in gray in Fig. 4.3) were added between the gates and the sources of the drivers and C_P was set to 200 fF. However, by doing this while keeping the same input network, the noise performance becomes sub-optimal. Because of these additional capacitances, we expect a 0.2-dB degradation of the average NF in the third band.

4.2.2 First version

The complete schematic of the LNA is shown in Fig. 4.3. The sizes of M_1 and M_2 are 300μm/0.12μm, while the cascode transistors M_3 and M_4 are 150μm/0.12μm. The bandwidth is extended by means of a shunt-peaking load. Introducing an inductor in series with the load resistance adds a zero to the frequency responce of the amplifier that compensates the decrease of the gain due to the parasitic capacitor at the output node. Because of the differential nature of the circuit, all

the employed coils have a symmetrical structure. It is interesting to note that the entire wide-band differential LNA needs only three coils, just like narrow-band ones do. The differential values of L_S and L_L are 0.8 nH and 3.7 nH, respectively, as mentioned in Sect. 2.4. The shunt-peaking resistance is $R_L = 50\ \Omega$. Biasing is provided to the drivers by setting their gate voltages V_{bias1} through the center tap of the secondary winding of the transformer. The bias current is 8.3 mA per branch. Finally, the impedance Z_N in Fig. 4.3 represents the notch filter.

4.2.3 Second version

The second version of the LNA is based on the first, with a few modifications. The two transistors M_A and M_B in gray in Fig. 4.3 appear only in this version, for instance. They have the same size as M_3 and M_4 and their role is to perform the 3-step variation of the LNA gain by means of the current steering technique connecting their gates to ground, V_{bias2} or V_{DD}. When their gates are connected to ground, they are turned off, and the amplifier is in its *high-gain mode* (HG). When the gates are connected to V_{bias2}, instead, as they have the same size and bias as M_3 and M_4, they steal about half of the bias current from the cascode transistors and cause a reduction of the gain of about 6 dB, taking the amplifier to a *low-gain mode* (LG). Finally, if the gates of M_A and M_B are connected to V_{DD}, the maximum amount of current is driven away from the load and the amplifier works as an attenuator (*attenuation mode*, AG). The three operation modes are set externally by a couple of bits (B_{VG1} and B_{AM}) that control a set of switches that connect the gates of M_A and M_B to the proper voltage. Capacitors C_{ex} appear only in the second version, too, and their role has been discussed above. The sizes of the other components remain unchanged with respect to the first version.

4.3 Notch filter

The notch filter was thoroughly analyzed in Chapter 3. Here we will discuss some implementation details. The filter has a differential structure too, and the use of the double-inductor topology takes the inductors count to four. Therefore, a strategy to reduce the area consumption is mandatory. The schematic of the

filter in the first version is sketched in Fig. 4.4. In order to reduce the area consumption, a symmetrical coil has been employed as the shunt inductor L_2. The two series inductors L_1, instead, have been made of a highly symmetrical structure made of two identical tightly coupled coils that exploit the magnetic coupling to achieve a higher effective inductance [23]. The employed structure is shown in the inset of Fig. 4.4 and was described in Sect. 2.4.5.

4.3.1 First version

As shown in Fig. 4.4, the shunt capacitance C_2 is made of a fixed capacitor C_2' and a varactor, which is controlled by the external voltage V_{tune} and grants the frequency tuning of the circuit. The differential value of L_2 is 1.65 nH. The two coils in L_1 have a self-inductance of 2.58 nH each and a coupling factor $k = 0.73$. So, the effective inductance in differential mode is $L_{1,\text{eff}} = (1 + k)L_1 = 4.46$ nH. C_2 varies from 1.22 pF to 1.66 pF and $C_1 = 0.6$ pF. The negative resistance is synthesized by the cross-coupled CMOS pair M_5–M_6. The resistance seen into the drain of the CMOS pair is $R = -1/g_m$, the negative sign arising from the positive

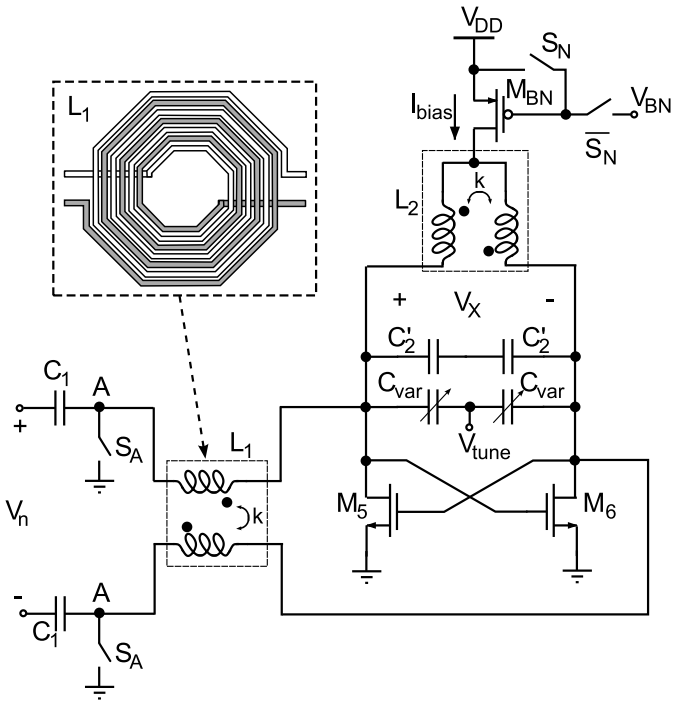


Figure 4.4: *Schematic of the notch filter in Version #1.*

feedback of the cross-coupled configuration. These two transistors have a size of 19.5μm/0.12μm and are biased with a variable current controlled externally by a 3-bit digital word in steps of 400 μA. In fact, as seen in Chapter 3, the bias current needed to maximize the depth of the notch depends on the frequency at which the filter is tuned. The bias circuit also features a set of switches (summarized as S_N and $\overline{S_N}$ in Fig. 4.4) that allow to switch the filter off. Another pair of switches (S_A) connect the node A in Fig. 4.4 to ground to avoid spur resonances when the filter is turned off. Therefore, in order to switch off the filer, both S_N ad S_A are to be closed. The presence of S_A sets the order in which C_1 and L_1 must be placed in the circuit. If the inductor is directly connected to the LNA, when the filter is turned off there will be a DC path from the cascode node to ground, thus obliterating the gain of the LNA itself. Finally, the tuning range is designed to be around the 5.2 GHz Wi-Fi band. However, due to a small design mistake, the actual designed tuning range goes from 4.65 GHz to 5.35 GHz.

4.3.2 Second version

In Version #2, the filter has been slightly redesigned, as shown in Fig. 4.5. The varactor has been replaced with an array of capacitors controlled by an external 4-bit digital word $B_{\mathrm{C3}} \dots B_{\mathrm{C0}}$ to allow for the tuning and calibration loop to be closed in the digital domain. The switches S_A now connect A to V_{DD}. In parallel with them there are a couple of capacitors C_R, which are a replica of C_4, controlled by the series switches S_R for reconfiguration purposes. The position of the bias current generator has also been changed. Initially, a reconfiguration scheme that did not involve C_R was studied, and the oscillator was made of L_1, L_2 and C_2 only, using the switch S_A for the reconfiguration. However, with the schematic of Fig. 4.4, in the reconfiguration mode the bias current would close through L_1 and S_A, thus bypassing M_5 and M_6 and preventing the compensation of the losses. Connecting S_A to V_{DD} without changing the position of M_{BN} would force the drain node of the cross-coupled pair to V_{DD} when S_A is closed, thus preventing the filter to be switched off. If, instead, we leave S_A connected to ground and move M_{BN} as in Fig. 4.5 there would be a direct DC path from V_{DD} to ground when S_A is closed. Therefore, the solution was to move both. With the introduction of the actual reconfiguration system, these changes would not

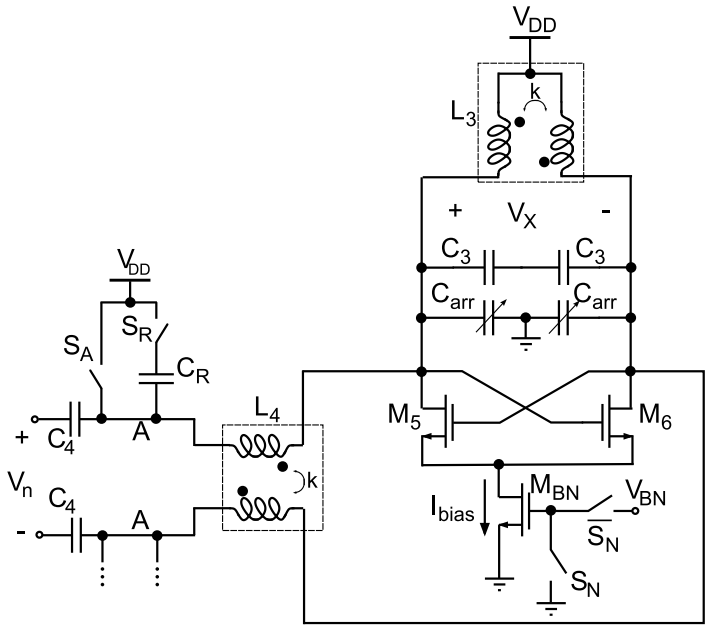


Figure 4.5: *Schematic of the notch filter in Version #2. The circuitry needed for the reconfiguration is shown on a single branch for clarity.*

be needed anymore because S_A is never closed when the bias current is on, and the reconfiguration is obtained by means of S_R, which is DC-isolated from the rest of the circuit thanks to C_R. However, we decided to keep the modifications. Because of the parasitics of the switches, C_1 has been modified to 0.33 pF. When the filter is reconfigured into an oscillator, the LNA is turned off (thus leaving one terminal of C_1 connected to a high impedance, so that it does not interfere with the operation of the oscillator) and S_R is closed. The designed tuning range is extended, going from 4.8 to 6 GHz. This led to new values of L_2 and C_2: $L_2 = 2.72$ nH (differential value) and C_2 is made variable from 0.28 pF to 1.18 pF, excluding the parasitics. The bias current is controlled by means of an external digital word, in steps of 100 μA. The voltage V_X is output by means of a buffer so that the transfer function Ψ_A described in Chapter 3 could be measured, thus making possible the verification of the calibration and tuning algorithm.

4.3.3 Biasing circuit

The current generator summarized by M_{BN} in both versions is actually a cascode current mirror. Fig. 4.6 shows the schematic of the biasing circuit of the first version. A 3-bit digital word ($B_{\mathrm{N2}}B_{\mathrm{N1}}B_{\mathrm{N0}}$) changes the current in steps of 400 μA, from 0.9 mA to 3.7 mA. The mirror transistors are scaled in powers of 2, so that the number of branches is $\log_2$ the number of variation steps. A logic network combines the three bits with a fourth one (B_{en}) that switches off the biasing circuit by connecting to V_{DD} the gates of the mirror transistors and opening the connection with the mirrored branch. The voltage V_{biasN} is nominally set to 1.3 V, and it can be trimmered externally to provide fine tuning of the current between one step and the other, and possibly to increase the maximum current up to 5 mA, by setting it to 1.65 V (which is the maximum allowable supply voltage). The size of the unit pMOS transistor is $12\mu\mathrm{m}/0.2\mu\mathrm{m}$. The size of the three nMOS transistors is $15\mu\mathrm{m}/0.2\mu\mathrm{m}$.

The biasing circuit of the second version is the dual of the one just described, with the addition of four more branches (taking the number of bits to seven) to take into account non-estimated losses in the circuit and to avoid the trimmered control on V_{biasN}. The current step is now 100 μA and the size of the unit transistor (nMOS this time) is $6.5\mu\mathrm{m}/0.18\mu\mathrm{m}$. The transistors of the main bias branch have a size of 5:1, while the digitally controlled branches are scaled in powers of 2 from 1:1 to 64:1, thus providing a current variable from 0.5 mA to 13.3 mA. The position of the switches and the combinatorial logic are slightly different, but the modifications are trivial. The schematic of this circuit is omitted because it is very crowded and it gives no further information than Fig 4.6.

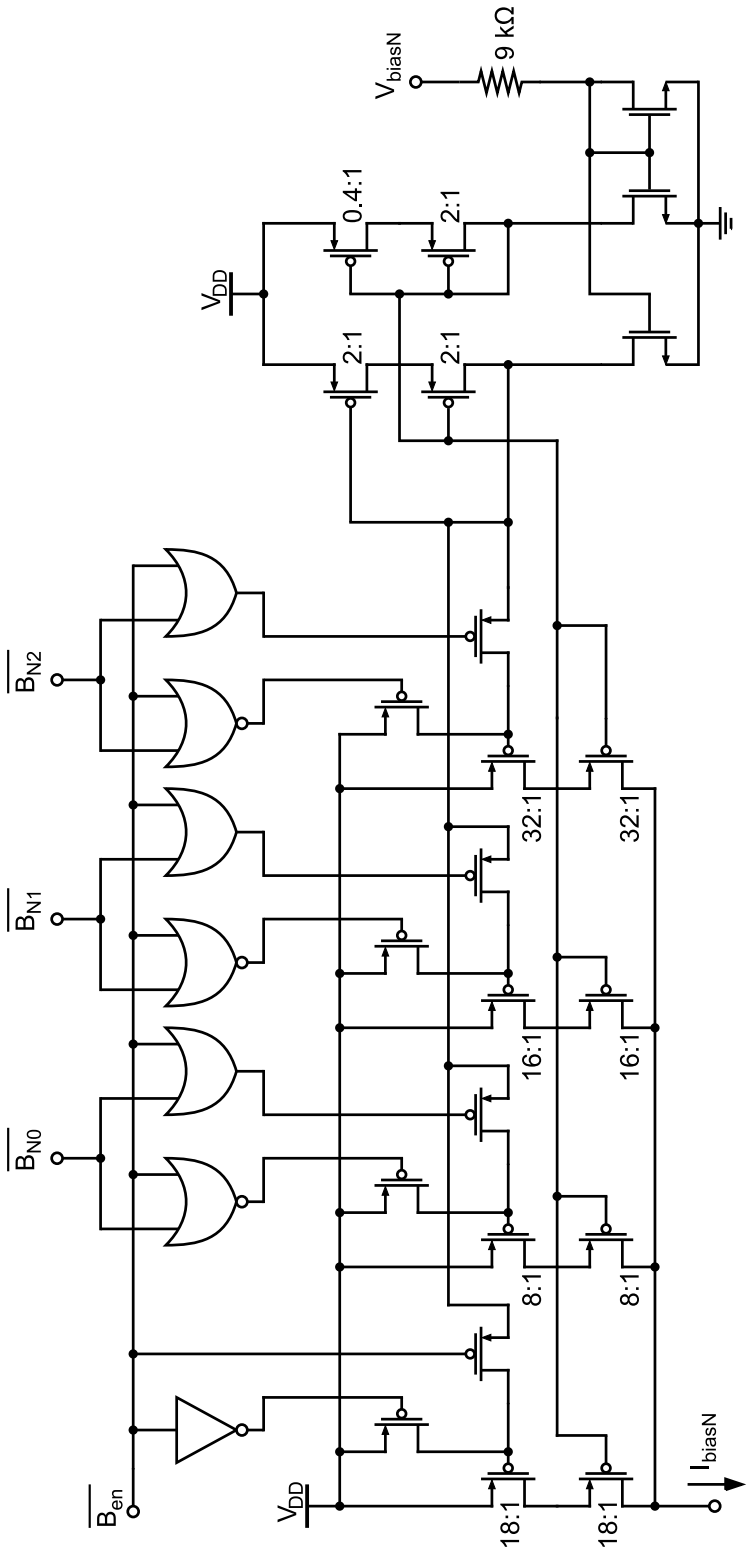


Figure 4.6: *Schematic of the biasing circuit of the notch filter in the first version.*

4.4 Mixer

The mixer, included only in the second version of the circuit, was designed inside Infineon by R. Salerno. It uses a conventional double-balanced structure, based on the Gilbert cell, with the addition of a current injection system to reduce the flicker noise of the switches. A first order RC output network helps filtering out of band interferers [13]. The schematic is shown in Fig. 4.7. The biasing circuit is Infineon's IP, and may not be shown here. The bias current is 1.6 mA.

At the input of the mixer, originally, a switchable capacitive divider was supposed to be present in order to provide further 3 dB of attenuation when activated. However, this feature was removed at last minute, but the input bit B_{VG2} that controlled the divider still figures among the inputs, although it is dummy.

The output of the mixer is fed to an output buffer for measurement purposes.

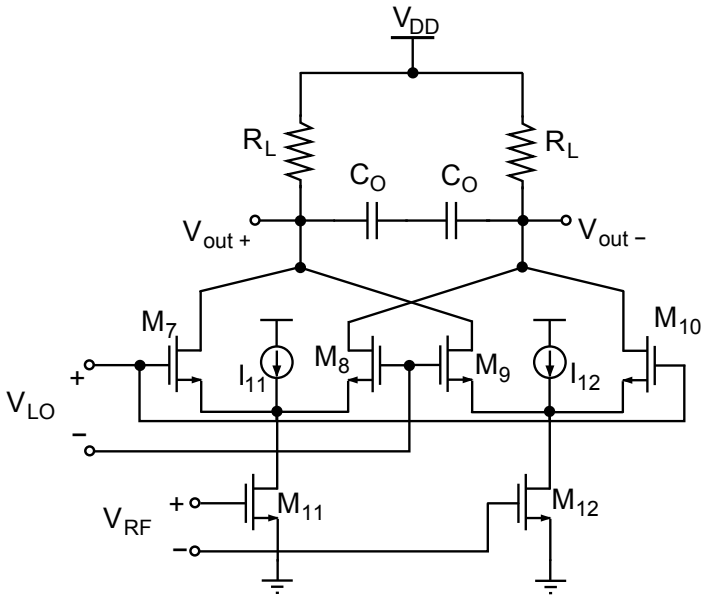


Figure 4.7: *Schematic of the employed mixer. Biasing not shown.*

4.5 Digital control

Version #2 of the chip has many control bits that must be fed to the circuit:

- Four bits that control the frequency tuning ($B_{C3} \dots B_{C0}$)
- Seven bits that control the bias current of the notch filter ($B_{N6} \dots B_{N0}$)
- Three bits that control the gain of the LNA (B_{VG1}, B_{VG2} (dummy), B_{AM})
- One bit that switches off the LNA (B_{LNAoff})
- One bit that enables the notch filter (B_{en})
- One bit that toggles the oscillator mode of the filter (B_{osc})

Some of these bits are in conflict with each other, so they are processed by a simple combinatorial network to resolve the conflicts. They are illustrated in Tables 4.1 and 4.2. The total number of control bits is then 17. To avoid an excessive crowding of the input lines, the control bit are given to the circuit in a serial fashion by using a full-custom serial interface provided by Infineon, which has only four input bits and can handle an arbitrary number of output bits.

Table 4.1: *Effect of the bits B_{AM} and B_{VG1} on the status of the circuit.*

B_{AM}	B_{VG1}	LNA status	Filter status
0	0	*HG mode*	*Not affected*
0	1	*LG mode*	*Not affected*
1	0	*AG mode*	*Not affected*
1	1	*AG mode*	*Not affected*

Table 4.2: *Effect of the bits B_{en} and B_{osc} on the status of the circuit.*

B_{en}	B_{osc}	LNA status	Filter status
0	0	*ON*	*Switched off. S_A closed, S_R closed, $\overline{S_N}$ open.*
0	1	*ON*	*Switched off. S_A closed, S_R closed, $\overline{S_N}$ open.*
1	0	*ON*	*Switched on. S_A open, S_R open, $\overline{S_N}$ closed.*
1	1	*OFF*	*Oscillator mode. S_A open, S_R closed, $\overline{S_N}$ closed.*

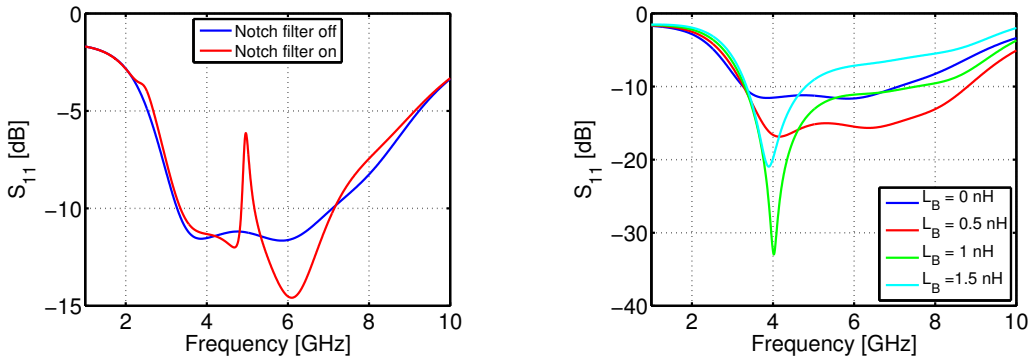
4.6 Simulation results

The circuits were designed within the Cadence Design Framework environment and simulated using Spectre and SpectreRF. The inductors were inserted into the circuits using a component, *n-port*, that can read an external input data file, such as the ones coming from the EM simulations. Unfortunately, post-layout simulations could not be run because of some bug in the tool configuration we could not figure out.

4.6.1 First Version

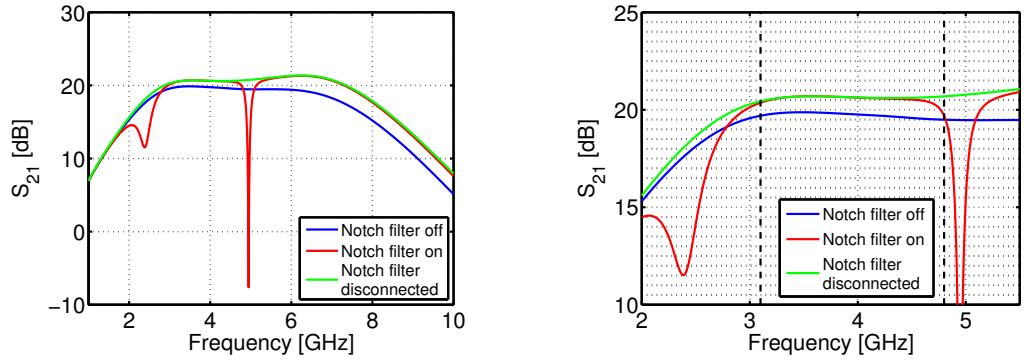
The simulations were run including a 100-fF input capacitance to account for the pad parasitics and no bondwire inductance. The input match is shown in Fig. 4.8. Fig. 4.8(a) shows the S_{11} of the LNA both with the notch filter off and on. We have S_{11} < -10 dB in the band from 3.3 to 7.1 GHz. The presence of the notch filter does not significantly affect the return loss. The effect of the bondwire inductance on the input match is shown in Fig. 4.8(b). The input network is robust against the presence of a bondwire inductance up to 1 nH. Actually, a small inductance (which will be surely present) helps the input match.

The frequency response (S_{21}) of the filter is plotted in Fig. 4.9. In Fig. 4.9(a) we can see that the maximum gain of the LNA is 19.9 dB and becomes 20.7 dB when the filter is turned on. The frequency response of the LNA without the



(a) (b)

Figure 4.8: *Input match simulation. (a) Effect of the notch filter. (b) Effect of the bondwire inductance.*



(a) (b)

Figure 4.9: *Simulated S_{21} of the LNA when the filter is tuned off and on. The case in which the notch is physically disconnected from the LNA is also shown. (a) Full-scale. (b) Horizontal zoom on the frequencies of interest.*

notch filter is also plotted. It can be noted that the latter curve follows the curve of the turned-on filter. The turned-off curve, instead, shows a degradation of the gain of about 1 dB. This happens because, when the filter is turned off, it does not magically disappear, but it has always some load effect on the LNA. When the filter is on, though, the load effect is part of the operation of the filter and is included in the effect of the filter network, being partly resonated. A zoom on the x axis around the frequency of interest is provided in Fig. 4.9(b) to show the roll off on the edges of the UWB Mode #1 band. The tuning range of the filter can be appreciated in Fig. 4.10, and it goes from 4.65 GHz to 5.25 GHz. From the same figure we see that the secondary notch at 2.4 GHz (which provide 9.2 dB of attenuation) is not affected by the tuning of the main one. Table 4.3 summarizes the current consumption and the input settings for the three curves. These simulations do not take into account the attenuation provided by the output buffer.

The simulated noise figure is reported in Fig. 4.11. The minimum noise figure is 3.4 dB when the filter is turned off, while turning the filter on lowers it to 3.1 dB. As the circuit is a wide-band system, we are more concerned on the average noise figure (NF_{AVG}) of each sub-band rather than on the spot NF. The values of NF_{AVG} for each sub-band is summarized in Table 4.4.

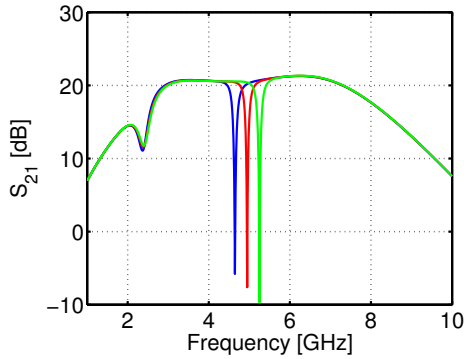


Figure 4.10: *Notch filter tuning range (Version #1).* $f_{MIN} = 4.65$ *GHz,* $f_{MAX} = 5.35$ *GHz.*

Table 4.3: *Current consumption and tuning range of the notch filter.*

$B_{N2}B_{N1}B_{N0}$	V_{biasN}	I_{biasN}	V_{tune}	f_N
000	1.3 V	3.67 mA	1.5 V	4.65 GHz
101	1.3 V	1.69 mA	0.84 V	4.95 GHz
110	1.13 V	1.09 mA	0.6 V	5.35 GHz

The transformer in the input network, because of its non-ideal behavior, causes some insertion loss. In order to evaluate this effect, an ideal matching network similar to the LNA input network was designed including the lumped model of the transformer shown in Fig. 4.2. Then, the ideal transformer model was replaced by the EM-simulated structure while keeping the rest of the network unchanged, as Fig. 4.12 illustrates, and a comparison was made between the gains of the two networks. Fig. 4.13(a) shows the return loss, which is not much affected by the

Table 4.4: *Average noise figure* NF_{AVG} *of each of the three sub-bands of UWB Mode #1.*

Filter status	Band #1	Band #2	Band #3
OFF	3.44 dB	3.56 dB	3.90 dB
ON	3.15 dB	3.23 dB	3.62 dB

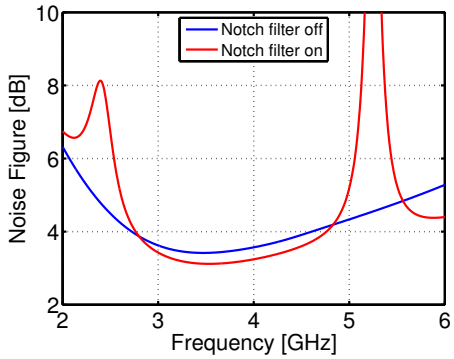


Figure 4.11: *Simulated noise figure of the LNA.*

replacement. Instead, Fig. 4.13(b) shows that the insertion of the real structure in the place of the ideal model causes a degradation of the gain, that is the insertion loss. In the frequency range of interest, the insertion loss of the transformer is about a couple of dB.

Finally, a couple of words on the output buffer. It is just made of two separate single-ended source-followers matched to an output resistance of 50 Ω, thus giving

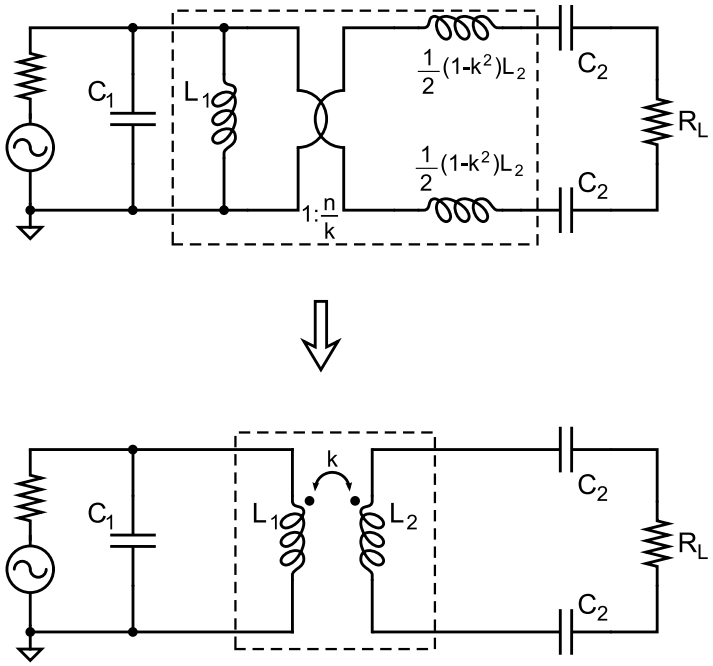
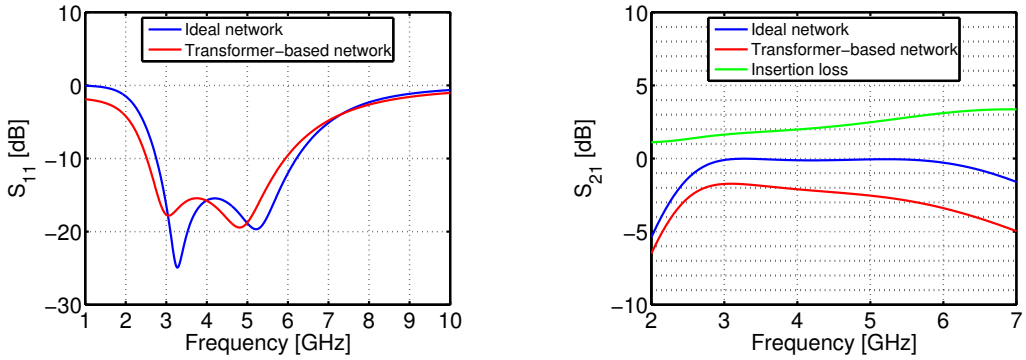


Figure 4.12: *Network used to estimate the insertion loss of the transformer.*



(a) (b)

Figure 4.13: *Estimation of the transformer insertion loss. (a) Input match (S_{11}). (b) Gain (S_{21}).*

6 dB of attenuation. Because of the AC coupling between the LNA and the buffer, a capacitive divider exists at the input of the buffer, so some further attenuation affects the signal. Fig. 4.14 shows the frequency response of the buffer. Its attenuation is about 7.5 dB, including the cap divider contribution, therefore this value must be subtracted from the previously simulated LNA gain to have the actual output. Linearity simulations could not be run because of convergence problems in the periodic steady-state simulations.

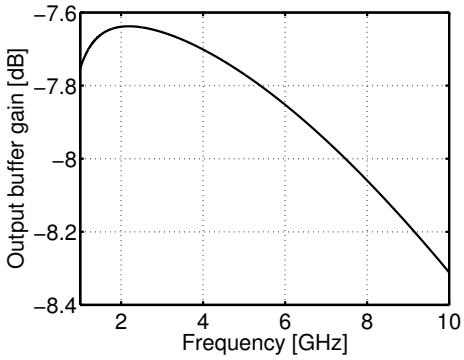
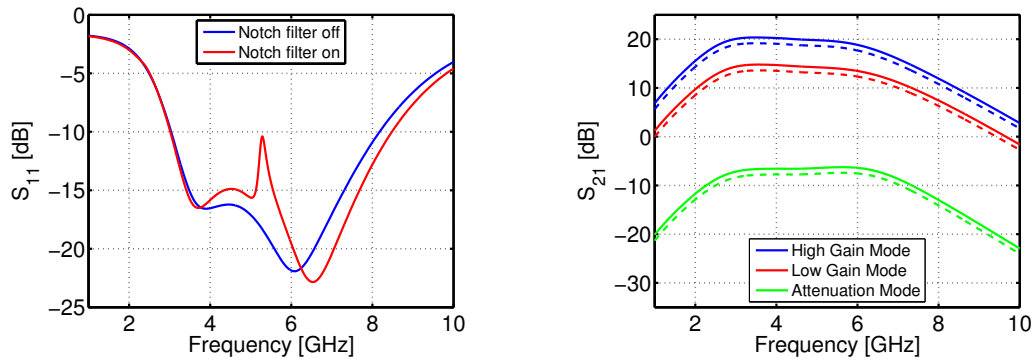


Figure 4.14: *Frequency response of the output buffer.*

4.6.2 Second Version

Again, a 100-fF capacitance emulating the pad capacitance is added to the input network. The effect of the bondwire has been already assessed, so Fig. 4.15(a) shows only the S_{11} of the front-end with the filter turned off and on. Fig. 4.15(b), instead, shows the S_{21} of the LNA in the three gain settings. In the simulation, the LNA is loaded by two mixers, one for each of the I and Q channels of a OFDM signal, as it would be in a real product. The LNA and the mixers are AC coupled, therefore a capacitive divider exists at the input of the mixers, that causes some attenuation, as happened with the output buffer in the first version. The S_{21} of the LNA after the cap divider is shown in Fig. 4.15(b) in dashed lines. The maximum gain before the cap divider is 20.4 dB and 14.8 dB in the HG and LG modes, respectively. In AG mode, the attenuation is about 6.5 dB. The cap divider attenuates the signal by about 1.2 dB.

In this version, one-tone linearity simulations (periodic steady-state simulations) were mandatory in order to simulate the conversion gain of the mixer. Therefore, just for this kind of simulations, the symmetrical inductors were replaced by lumped models whose behavior was somewhat similar to the EM-simulated ones, although not very accurate. The simulations are then not very



(a) (b)

Figure 4.15: *Simulation of the S-parameters of the LNA in Version #2. (a) Input match with notch filter off and on. (b) Frequency response in the three gain settings. Filter switched off. Solid line: measured at the output of the LNA; dashed line: measured at the input of the mixer.*

reliable, but were run to verify the functionality of the system and are reported in Fig. 4.16. In this way, 1-dB compression point simulation could also be run, resulting in a 1-dB CP of -27 dBm, -26.5 dBm and -26 dBm for UWB sub-bands #1, #2 and #3, respectively.

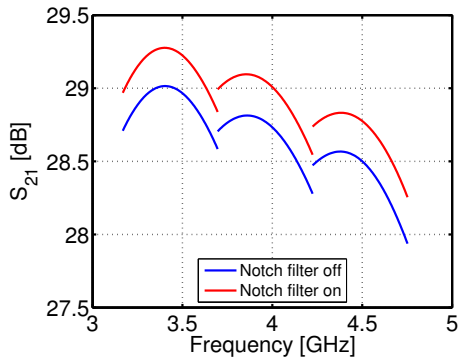


Figure 4.16: *Conversion gain of the front-end in the HG mode with the filter turned off and on.*

When the notch filter is turned on, its auxiliary output can be measured. The result of the simulation is given in Fig. 4.17. The result includes the contribution of the RF buffer used to output the auxiliary node. Table 4.5 shows the simulated tuning range of the filter along with the current consumption in three significant cases (filter tuned to f_{MIN}, f_{MAX} and 5.2 GHz).

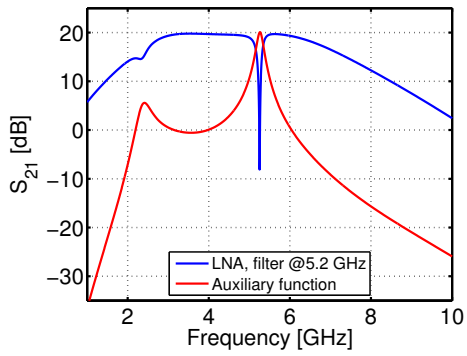


Figure 4.17: *Frequency response of the LNA in HG mode (filter turned on and tuned to 5.2 GHz) and frequency response of the auxiliary node.*

Table 4.5: *Current consumption and tuning range of the notch filter.*

$B_{\mathrm{N6}} \ldots B_{\mathrm{N0}}$	V_{biasN}	I_{biasN}	$B_{\mathrm{C3}} \ldots B_{\mathrm{C0}}$	f_N
0010010	0.5 V	2.33 mA	1111	4.78 GHz
0001000	0.5 V	1.32 mA	1000	5.21 GHz
0000010	0.5 V	0.71 mA	0000	6.04 GHz

The noise figure of the LNA (loaded by the mixers) is reported in Fig. 4.18 in the HG and LG gain settings. As regards the noise figure of the front-end, we must consider the double-sideband NF, rather than the single-sideband, for the receiver is of the direct conversion kind. For some reason, however, the simulation of the noise figure of the entire front-end (pnoise analysis) is not reliable, as it results lower than the noise figure of the LNA. Therefore, it is not reported here. The average noise figure of the LNA is not reported, either, as it cannot be measured, so it makes no sense to compute it. In any case, we can notice the degradation at high frequency due to the rearrangement of the input network (cf. Sect. 4.2.3). The NF in LG mode is obviously higher because of the lower gain, but this is not an issue, because if we need the LG mode, it means that we have a strong input signal, which will not be affected by the noise in a significant way.

Fig. 4.19 shows the frequency response of the two buffers used in the circuit. In Fig. 4.19(a) is plotted the voltage gain of the base-band buffer used at the

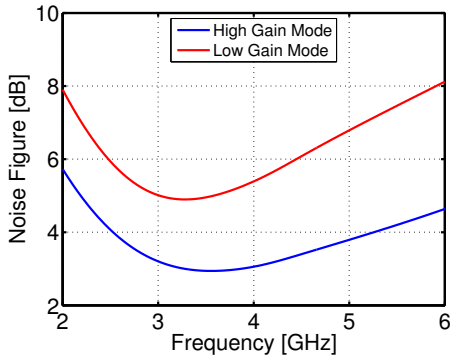
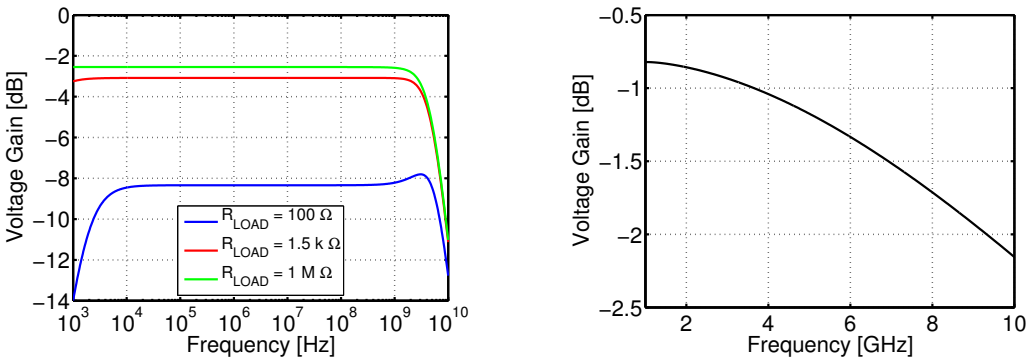


Figure 4.18: *Simulated noise figure of the LNA in the HG and LG modes (filter turned off).*

output of the mixer. Its output is matched to a 50-Ω load and it has a DC gain of -2.5 dB. The passband behavior is due to the AC coupling at the output of the buffer. Therefore, when loaded by a high impedance, the buffer can be assumed to have a gain of -2.5 dB in the band of interest (0–1 GHz). Fig. 4.19(b), instead, shows the voltage gain of the RF buffer used to output the auxiliary node of the notch filter. The attenuation provided by the buffer is about 1 dB at the frequencies of interest (3–5 GHz).



(a) (b)

Figure 4.19: *Voltage gain of the two buffers used in Version #2. (a) Output buffer loaded by three different resistances. (b) RF buffer for the auxiliary output of the filter*

Chapter 5

Measurements Results

The measurements were performed partly at Infineon labs in Villach, Austria, and partly in the Microelectronic Measurements Lab at the Department of Information Engineering, University of Padova. In particular, all the noise measurements were made at Infineon's. On the contrary of what has been done in the previous chapter, where the simulations were reported separately for each version of the circuit, here it is preferred to present them in a combined fashion so as to highlight the differences in the two circuits and to infer some important considerations about the effect of the notch filter on the entire front-end.

5.1 Fabrication and assemblage

The prototypes of the chips were fabricated in a 0.13 μm digital CMOS process, with a 1.5 V supply voltage. Including the pads, the area occupied by the two dies is 1.6 mm^2 (Version #1) and 2.25 mm^2 (Version #2). Both of them were assembled in a chip-on-board fashion for measurement purposes. The power consumption of the first version is 32.5 mW. The notch filter consumes about 7.5 mW when tuned to 5.2 GHz, while the LNA consumes 25 mW. The power consumption of the second version is 30 mW, excluding the notch filter, which draws a power variable from 1.35 to 5.55 mW.

Microphotographs of the chips are reported in Fig. 5.1.

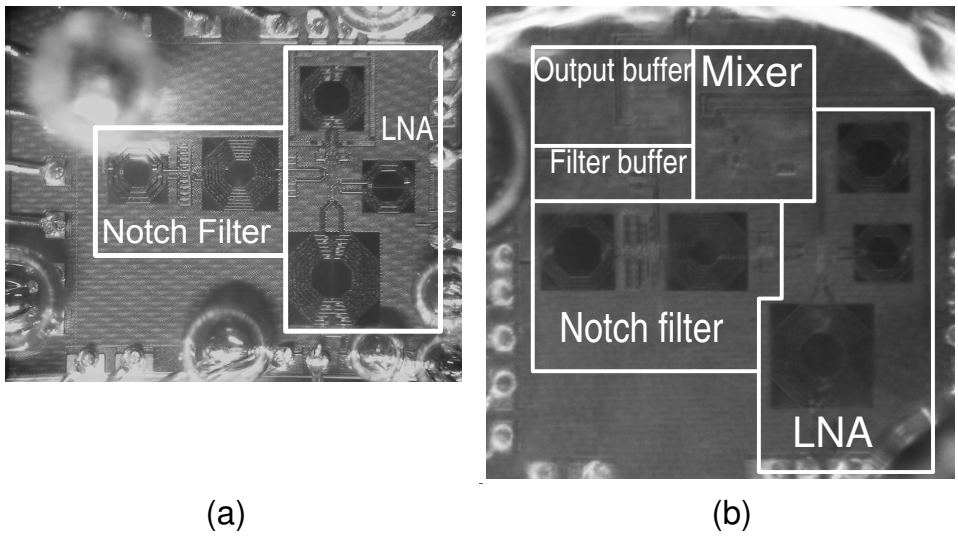


Figure 5.1: *Microphotograph of the die. (a) Version #1. (b) Version #2.*

5.2 Measurement setup

The S-parameters of the first version were measured at Infineon labs in Villach with a 4-port network analyzer featuring an automatic computation of the balanced combination of two separate ports. This means that we used three ports of the network analyzer, one for the input signal (which is single-ended) and two for the output (one for each of the two terminals of the differential output). In this way we could get the differential output directly from the instrument. Two-tone tests were carried out using two signal generators. Their outputs, summed with each other with a passive power combiner, whose attenuation has been de-embedded at measurement time, and using a spectrum analyzer to measure the output. The chip needed four DC voltage sources, which were provided by two double-output DC power supplies. Measurements of the second version were a bit trickier, as a mixer was involved. The conversion gain could be measured at the Photonics Lab at the Department of Information Engineering of the University of Padova with another 4-port network analyzer, which had an additional internal oscillator to provide mixer measurement functionality. Unfortunately, it could not compute the balanced output while in mixer mode, so we had to use an external differentail amplifier (whose gain was afterwards de-embedded). As the

external buffer had a high input impedance, the on-chip output buffer was not affected by the matched load and showed 2.5 dB of attenuation over the whole bandwidth (instead of 8.5 dB). The local oscillator signal, as said, was provided by the network analyzer itself. However, as the on-chip LO input is differential, a hybrid coupler was used to perform the conversion. The DC voltages were given by an *ad hoc* DC board. This board contained several current regolators to provide the bias voltages. A trimmer assured the control over the output voltage. A voltage regulator supplied the V_{DD} voltage. The digital inputs were generated by a digital pattern generator. Its output voltage swing, though, was designed for TTL levels, much higher than the 1.5 V needed to drive the circuit. This issue was solved in a simple way, by using resistive partitioners to take the voltage to the desired value, and shielded flat cables to avoid cross-talk between the outputs of the pattern generator. This approach slowed down a lot the rise- and fall-times of the digital signals, however this did not seem to disturb the circuit. Finally, the noise mesurements were performed at Infineon labs with a spectrum analyzer featuring a particular plug-in for noise measurements.

5.3 Small-signal and noise tests

The return loss of the two chips is shown in Fig. 5.2. The blue line is the S_{11} of Version #1 when the notch filter is off, while the red one is the S_{11} of the same version when the filter is turned on. The rearrangement in the layout of the LNA in the second version and the introduction of the additional capacitors C_{ex} led to a different S_{11} (green line), as the simulations suggested. The different capacitive coupling between drain and gate of M_1 and M_2 helps isolating the input from the notch filter, so the S_{11} of the front-end when the filter is turned on cannot be distinguished from the S_{11} when the filter is off. This effect does not seem to appear on simulation results. However, it must be noticed that also in the first version the coupling of the filter to the input appears much reduced in the measurement data with respect to simulations. Therefore, recalling that no post-layout simulations could be run, the effect appearing in the measured S_{11} of the second version is not surprising.

In both cases, S_{11} < -10 dB in the band of interest, and the notch filter does not have much influence on the input reflection. This validates the use of

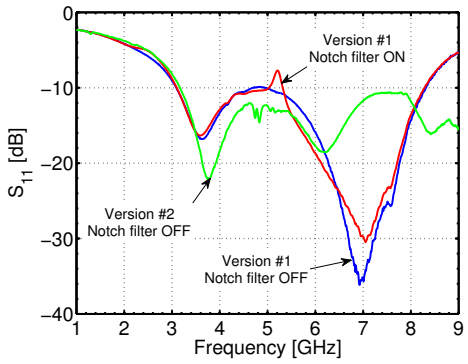
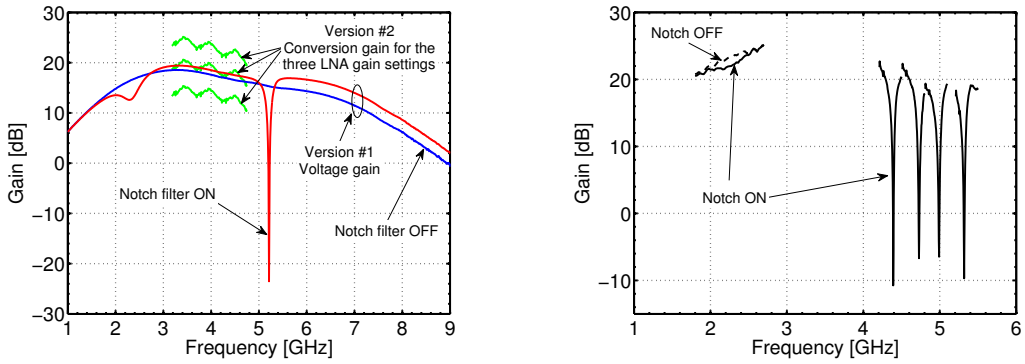


Figure 5.2: *Measured S_{11} of the two versions of the circuit.*

the transformer in the wide-band input-matching network. The entire 2-section input network occupies an area of 0.14 mm^2, as compared to the 0.21 mm^2 occupied by the analogous one reported in [28], made of separate inductors, with no degradation in the input match performance.

The gains of the two circuits are sketched in Fig. 5.3(a). The maximum gain of the LNA alone (blue line) is 18.5 dB, which becomes 19.4 when the notch filter is turned on (red line). The green lines show the conversion gain of the complete front-end in the three sub-bands and for the three gain configuration of the LNA. The on-chip buffer of the first version was de-embedded from the gain measurements, as we could measure a similar one and add up its attenuation to the measured LNA gain. As described above, the buffer in the second version was loaded with a high impedance, so that its contribution is that of the DC attenuation. As this could not be directly measured, we used the simulation datum to de-embed it from the gain results. The noise measurements in both versions, however, do take into account the contribution of the buffers. The maximum gain in HG mode is 25 dB (sub-band #1), which is 4 dB lower than simulation results. The bandwidth of the LNA is clearly smaller than simulated, this effect being probably due to parasitic capacitances at the output of the LNA. The excess capacitance at the output is provided by the wiring of the circuit and might have been estimated only by means of post-layout simulations. The LG and AG modes do not seem to behave as expected, too. LG mode lowers the gain by 4 dB, which is still acceptable as compared to the expected 6 dB. However, the LNA in AG mode does not attenuate the signal, but provides just 10 dB less gain than HG mode. For some reason, the two current-steering transistors do



(a) (b)

Figure 5.3: *Measured voltage gain and performance of the notch filter. (a) Voltage gain of the LNA in Version #1 and conversion gain of the front-end in Version #2. (b) Performance of the notch filter in Version #2.*

not seem to steer a proper amount of current. In addition, the mixer (whose bias current is not manually controllable) draws twice the expected DC current, so we cannot exactly tell what is its contribution to the conversion gain. The notch filter, though, is functional, and its maximum attenuation is as high as 44 dB at f_2 in the first version. The secondary notch, at 2.4 GHz, gives an attenuation of 6 dB. The measured tuning range of the main notch frequency goes from 4.7 to 5.4 GHz. The performance of the notch filter in Version #2 is assessed in Fig. 5.3(b). The filter frequency response is shown for four settings of the digital control word $B_{C3} \ldots B_{C0}$. The attenuation provided by the main notch is 36 dB, while the secondary notch is less effective than the one in the first version, as its attenuation is only 3 dB. The frequency of the main notch can be tuned from 4.4 to 5.3 GHz. These values of tuning range are shifted towards lower frequencies by about 1 GHz with respect to the design because of underestimated parasitic capacitances, mainly coming from the heavy wiring of the capacitor array. The same happened to the secondary notch, as its center frequency is 2.2 GHz, as opposed to the designed 2.4 GHz.

A summary of noise measurements is given in Table 5.1. In the first version the minimum average NF is as low as 3.6 dB in the first sub-band. When the filter is turned on, the NF undergoes a degradation of 0.1 dB, 0.2 dB and 0.6 dB

Table 5.1: *Average noise figure measurements.*

circuit version	notch filter status	NF_{AVG} [dB]		
		Band #1	Band #2	Band #3
LNA alone	OFF	3.6	3.8	4.4
	ON	3.7	4.0	5.0
Complete front-end	OFF	5.1	5.4	6.2
	ON	5.1	5.4	6.2

in sub-bands #1, #2 and #3 respectively. It must be reminded that the input network integrates a balun, so an external one, which would add at least 1 dB to the NF, is not needed. Moreover, an external filter dedicated to the rejection of the interference in the 5–6 GHz frequency range would degrade the in-band gain, thus further increasing the NF. The presence of the mixer in the second version introduces an increase of about 1.5 dB in the average noise figure. As predicted in Sect. 4.2.1, in the third band the noise increment is slightly higher with respect to the other two bands because of the rearrangement in the LNA layout and of the addition of C_{ex}. In this version, the presence of the filter does not have any significant influence on the NF. This is mainly due to the fact that, for the same tuning, the filter in the second version consumes about 70% less current than the one in Version #1 and therefore injects much less current noise into the LNA.

5.4 Linearity tests

Several linearity tests were performed on both chips, and the results are collected in Tables 5.2–5.4. Table 5.2 shows the results of the gain compression tests. The 1-dB compression point (1dB-CP)[1] of the LNA (Version #1) is about -9 dBm, while the front-end's one is -30 dBm, a couple of dB less than the simulation results. As the maximum gain of the LNA in the first version is 19.4 dB, we can roughly estimate the mixer 1dB-CP in the following way. With an input

[1] 1dB-CP is the power of the in-band input signal that causes a reduction of 1 dB of the amplifier gain.

signal power of -30 dBm and a 1dB-CP of -9 dBm, the LNA is supposed to be operating in the linear region. Therefore, the compression is entirely due to the mixer, at whose input there will be a signal amplified by the 20-dB gain of the LNA, that is -10 dBm. As a consequence, we can say that the input power that causes a compression of 1 dB in the conversion gain of the mixer is approximately -10 dBm. The 1dB-CP of the front-end was measured also in the low gain modes (LG and AG). The improvement in the 1dB-CP is compatible with the decrease in the gain of the LNA. Table 5.2 also reports the cross-band 1 dB compression point (xCP)[2] [12] for Version #1 and for Version #2 in the three gain modes, both with the notch filter off and turned on (and tuned on top of the blocker at 5.2 GHz). While the improvement due to the filter is of only a couple of dB in the first version, we can see that the notch filter is more effective in the second one, where the improvement given by the filter is as much as 7 dB in band #3. Again, in the low gain modes, the improvements in this factor of merit are compatible with the reduction of the gain of the LNA. The linearity of the LNA itself, on the other hand, being limited by the operation of the driver transistors, is not influenced by the variation in the gain. When the LNA of the complete front-end is in the low gain modes, we notice that the xCP performance of the front-end tends to converge to the xCP of the LNA alone. This means that the linearity of the front-end is mostly limited by the linearity of the mixer, and demonstrates the benefits of the notch filter to the overall system.

In-band and out-of-band two-tone tests are reported in Tables 5.3 and 5.4, respectively. The two-tone tests have been performed with the second version in HG mode. In Table 5.3 are reported the in-band IIP3 and the in-band IIP2, the latter obtained measuring the output tone appearing at the frequency that is the difference between the two test tones [29]. In Table 5.4, for each version, 'OFF' and 'ON' refer to the filter status. The underlined tone is the one that gets filtered. The presence of the filter gives an improvement of 4 dB in the IIP3 of the LNA and as much as 10 dB in the IIP3 of the front-end.

[2]xCP is the power of the out-of-band blocker that causes a reduction of 1 dB of the in-band gain.

Table 5.2: *In-band 1-dB compression point and cross-band 1-dB compression point.*

(⋆) Refers to Version #1. (‡) Refers to Version #2

Sub-band number	1dB-CP [dBm]			xCP (⋆) [dBm]	xCP (‡) (HG) [dBm]		xCP (‡) (LG) [dBm]		xCP (‡) (AG) [dBm]	
	(⋆)	(‡) (HG)	(‡) (LG)	(‡) (AG)	OFF	ON	OFF	ON	OFF	ON
#1	-9	-30	-24	-18	-12	-10	-24.5	-18.5	-20	-15	-14	-10
#2	-8.7	-29	-24	-19	-12	-10	-25.5	-19	-21	-16	-15	-11
#3	-9.4	-28	-23	-20	-12	-10	-27	-20	-23	-17	-17	-12

Table 5.3: *In-band two-tone tests.*

Sub-band number	Version #1		Version #2 (HG)	
	IIP2 [dBm]	IIP3 [dBm]	IIP2 [dBm]	IIP3 [dBm]
#1	14.6	-2.5	7.8	-20.2
#2	14.1	1.8	2.3	-19.5
#3	14.2	-1.6	-1	-18.3

Table 5.4: *Out-of-band two-tone tests.*

Blocker [GHz]		IM order	IIP – V. #1 [dBm]		IIP – V. #2 (HG) [dBm]	
#1	#2		OFF	ON	OFF	ON
4.9	5.2	3	–	–	-13.2	-4.7
5.2	5.8	3	0.4	4.6	-11.4	-1.6
1.9	5.2	2	–	–	15.1	20.4
2.3	5.8	2	35.6	36	13.8	14.6
1.9	2.3	2	25.9	28.2	4.8	6.2

Fig. 5.4 shows the large signal behavior of the notch filter in Version #2. We plot the maximum attenuation of the notch filter (tuned to 5.2 GHz) as a function of the power of the blocker. The attenuation is higher than 15 dB for blocker powers up to -16 dBm. The data obtained with the bias current set to I_N and I_O are compared, being I_N the current that maximizes the notch depth and I_O the one that starts the oscillation in the reconfigured circuit. The curve relative to I_O has a sub-optimal behavior for smaller blocker powers, but the two curves tend to converge for increasing powers. The xCP measurement in band #3 is also shown. Even at high levels of blocker power the attenuation is actually given by the filter, and not due to the compression of the in-band gain.

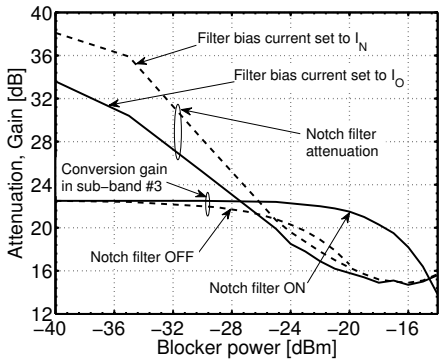


Figure 5.4: *Large signal behavior of the notch filter and xCP test.*

5.5 Tuning and calibration algorithm

The functionality of the calibration and tuning algorithm was investigated by measuring the auxiliary output in the second version of the chip. The transfer function V_X/V_{in} is shown in Fig. 5.5 for some settings of $B_{C3} \ldots B_{C0}$. Settings 0000 and 1111 are included. The function is clearly bandpass. The inset shows the value of V_X/V_{in} when a blocker at 5.2 GHz is applied at the input. The peak is about 7 dB higher than the neighbor points, thus corroborating the analysis of Chap. 3, and confirming that the tuning strategy given there can be successfully put in practice.

The algorithm for the current calibration of the notch filter is assessed in Fig. 5.6. The currents I_N and I_O are plotted for each combination of $B_{C3} \ldots B_{C0}$. I_N is plotted in solid line with squares, while I_O is plotted in dashed line and circles. The two currents are very close to each other, upholding the illustrated calibration process. All the measurement results shown for the second version of the circuit were obtained with the filter biased to the current given by the calibration process.

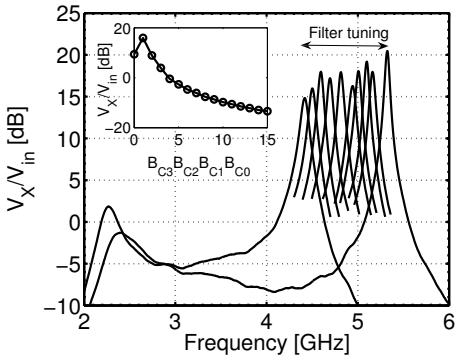


Figure 5.5: *Measured transfer function V_X/V_{in} for some tunings (including edge ones). Inset: Value of V_X/V_{in} for each setting of $B_{C3} \ldots B_{C0}$ with blocker at 5.2 GHz.*

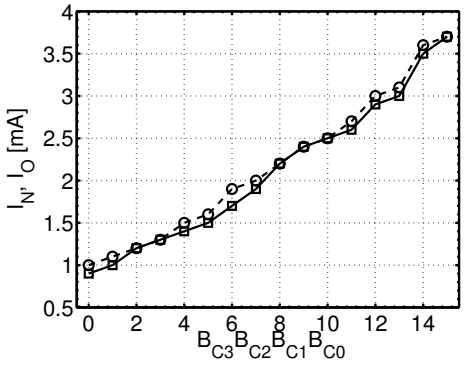


Figure 5.6: *Measured I_N (□) and I_O (○) for each setting of $B_{C3} \ldots B_{C0}$.*

Conclusions

In this thesis the results of the research activity carried out during the Ph. D. course were illustrated. A notch filter for the rejection of the WLAN interference in UWB systems was designed and integrated into a receiver analog front-end. The circuit was integrated in a standard 0.13-μm CMOS technology provided by Infineon Technologies AG. The front-end features an input network based on a transformer that provides for input matching and single-ended to differential conversion, as well as noise optimization. A thourough analysis of the filter was carried out that established a guide-line to the choice of the network and of the components values so as to optimize the power and area consumption. To verify the effectiveness of the filter, two versions of the system were implemented. The first version comprised a stand-alone LNA with the notch filter, and allowed for a study of the behavior of the filter itself. The second version included also a mixer and was designed to demonstrate the effect of the notch filter on the overall front-end and the feasibility of the algorithm for automatic tuning and calibration. In this work original results were achieved regarding the optimization of the notch filter, its applicability to an analog front-end and the feasibility of the self-tuning system. The achieved results led to the publication of two papers in conference proceedings [12], [13]. The filter can provide for more than 40 dB of attenuation, but the benefits on the performance of the LNA are limited by the fact that the linearity of the LNA is mostly related to the driver transistors. On the other hand, the filter showed its potential when included into a complete front-end: the linearity of the front-end is limited by the performance of the mixer, and turning the notch filter on improves the xCP of the system by 7 dB and IIP3 by as much as 10 dB. The reconfiguration concept for the calibration was demonstrated, as well as the effectiveness of the tuning algorithm.

Conclusioni

In questa tesi sono stati illustrati i risultati dell'attività di ricerca svolta durante il corso di dottorato. Un filtro notch per la soppressione dell'interferenza WLAN nei sistemi UWB è stato disegnato ed integrato in un front-end analogico per un ricevitore. Il circuito è stato realizzato in tecnologia CMOS da 0.13 μm di Infineon Technologies AG. Il front-end ha una rete d'ingresso basata su un trasformatore che fornisce adattamento d'impedenza all'ingresso, la conversione da single-ended a differenziale ed un'ottimizzazione delle prestazioni di rumore. È stata inoltre svolta un'approfondita analisi del filtro per stabilire delle linee guida per la scelta del tipo di rete e per la scelta dei valori dei componenti allo scopo di ottimizzare il consumo di potenza e di area. Per verificare l'efficacia del filtro, sono state realizzate due versioni del sistema. La prima versione includeva solamente un LNA con il filtro notch ed ha permesso di studiare il comportamento del filtro in sè. La seconda versione includeva in più un mixer ed era stata disegnata per dimostrare l'effetto del filtro sull'intero front-end e la fattibilità dell'algoritmo per la sintonizzazione e la calibrazione automatica dello stesso. In questo lavoro sono stati raggiunti risultati originali sull'ottimizzazione del filtro notch, la sua applicabilità ad un front-end analogico e la fattibilità del sistema di sintonizzazione. I risultati raggiunti hanno portato alla pubblicazione di due articoli su atti di conferenze [12], [13]. Il filtro può fornire più di 40 dB di attenuazione, ma i benefici sulle prestazioni del LNA sono limitate dal fatto che la linearità del LNA è legata soprattutto ai transistor che fanno da driver del circuito. D'altra parte, il filtro ha mostrato le sue potenzialità quando è stato incluso in un front-end completo: la linearità del front-end è limitata dalle prestazioni del mixer, e l'accensione del filtro migliore il xCP del sistema di 7 dB e l'IIP3 di ben 10 dB. L'idea della calibrazione tramite riconfigurazione in oscillatore è stata altresì dimostrata, così come l'efficacia dell'algoritmo di sintonizzazione.

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Gasperin and Stefano Dal Toso. In this list, the most important is missing. I cannot find better words to say about Andrea Maniero than what he has said about me: “an ideal companion for the last two years, one of the best people to share my desk with”.

Of course, I cannot finish this section without an heartfelt thank you to my parents because they always let me take my choices, regardless of the difficulties, and my brother too. Finally, wish to thank all my (not many) friends for all the good time spent during the years and the fun I had.

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Bibliography

[1] (2002) Revision of part 15 of the commission's rules regarding ultrawideband transmission systems. Federal Communication Commission. [Online]. Available: http://www.fcc.gov/Document_Indexes/Engineering_Technology/2002_index_OET_Order.html

[2] (2005) Standard ECMA-368: High rate ultra wideband PHY and MAC standard. Ecma International – European association for standardizing information and communication systems. [Online]. Available: http://www.ecma-international.org/publications/standards/Ecma-368.htm

[3] J. R. Bergervoet, K. S. Harish, S. Lee, D. M. W. Leenaerts, R. van de Beek, G. van der Weide, and R. Roovers, "A WiMedia-compliant UWB transceiver in 65nm CMOS," in *IEEE ISSCC Digest of Technical Papers*, San Francisco, CA, Feb 2007, pp. 112–113.

[4] C. Sandner, S. Derksen, D. Draxelmayr, S. Ek, V. Filimon, G. Leach, S. Marsili, D. Matveev, K. L. R. Mertens, F. Michl, H. Paule, M. Punzenberger, C. Reindl, R. Salerno, M. Tiebout, A. Wiesbauer, I. Winter, and Z. Zhang, "A WiMedia/MBOA-compliant CMOS RF transceiver for UWB," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2787–2794, 2006.

[5] A. P. Chandrakasan and F. S. Lee, "A BiCMOS ultra-wideband 3.1–10.6-GHz front-end," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1784–1791, 2006.

[6] G. Cusmai, M. Brandolini, P. Rossi, and F. Svelto, "A 0.18-μm CMOS selective receiver front-end for UWB applications," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1764–1771, 2006.

[7] S. Lo, I. Sever, S.-P. Ma, P. Jang, A. Zou, C. Arnott, K. Ghatak, A. Schwartz, L. Huynh, V. T. Phan, and T. Nguyen, "A dual-antenna phased-array UWB transceiver in 0.18-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2776–2786, 2006.

[8] R. Roovers, D. M. W. Leenaerts, J. Bergervoet, K. S. Harish, R. C. H. van de Beek, G. van der Weide, H. Waite, Y. Zhang, S. Aggarwal, and C. Razzell, "An interference-robust receiver for ultra-wideband radio in SiGe BiCMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2563–2572, 2005.

[9] T. H. Lee, *The Design of CMOS Radio-Freqency Integrated Circuits*, 1st ed. Cambridge University Press, 1998.

[10] T. W. Fischer, B. Kelleci, K. Shi, A. İ. Karşılayan, and E. Serpedin, "An analog approach to suppressing in-band narrow-band interference in UWB receivers," *IEEE Transactions on Circuits and Systems–I: Regular Papers*, vol. 54, no. 5, pp. 941–950, 2007.

[11] A. Bevilacqua, A. Maniero, A. Gerosa, and A. Neviani, "An integrated solution for suppressing WLAN signals in UWB receivers," *IEEE Transactions on Circuits and Systems–I: Regular Papers*, vol. 54, no. 8, pp. 1617–1625, 2007.

[12] A. Bevilacqua, A. Vallese, C. Sandner, M. Tiebout, A. Gerosa, and A. Neviani, "A 0.13μm CMOS LNA with integrated balun and notch filter for 3-to-5 GHz UWB receivers," in *IEEE ISSCC Digest of Technical Papers*, San Francisco, CA, Feb 2007, pp. 420–421.

[13] A. Vallese, A. Bevilacqua, C. Sandner, M. Tiebout, A. Gerosa, and A. Neviani, "An analog front-end with integrated notch filter for 3-5 GHz UWB receivers in 0.13 μm CMOS," in *Proceedings of the IEEE European Solid-State Circuits Conference*, München, Germany, Sept 2007, pp. 139–142.

[14] B. Razavi, *RF microelectronics*, 1st ed. Prentice Hall, 1998.

[15] T.-K. Nguyen, C.-H. Kim, G.-J. Ihm, M.-S. Yand, and S.-G. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 05, pp. 1433–1442, 2004.

[16] (2005) High rate - ultra wide band (UWB) background. Ecma International – European association for standardizing information and communication systems. [Online]. Available: http://www.ecma-international.org/activities/Communications/tg20_UWB_Background.pdf

[17] (2006, amended 2007) UWB technology in bands below 10.6 GHz. Electronic Communications Committee. [Online]. Available: http://www.ero.dk/documentation/docs/doc98/official/pdf/ECCDEC0604.PDF

[18] A. Bevilacqua and A. M. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1–10.6-GHz wireless receivers," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2259–2268, 2004.

[19] A. Ismail and A. A. Abidi, "A 3–10-GHz low-noise amplifier with wideband LC-ladder matching network," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2269–2277, 2004.

[20] G. L. Matthaei, L. Young, and E. M. T. Jones, *Microwave Filters, Impedance–Matching Networks, and Coupling Structures*, 1st ed. McGraw–Hill Book Company, 1964.

[21] A. Amer, E. Hegazi, and H. Ragai, "A low-power wideband CMOS LNA for WiMAX," *IEEE Transactions on Circuits and Systems–II: Express briefs*, vol. 54, no. 1, pp. 4–8, 2007.

[22] A. M. Niknejad and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF ICs," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1470–1481, 1998.

[23] J. J. Zhou and D. J. Allstot, "Monolithic transformers and their application in a differential CMOS RF low-noise amplifier," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 2020–2027, 1998.

[24] M. Guarnieri and G. Malesani, *Elementi di elettrotecnica. Reti elettriche.*, 1st ed. Edizioni Libreria Progetto, 1998.

[25] T. H. Lee, H. Samavati, and H. R. Rategh, "5-GHz CMOS wireless LANs," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 268–280, 2002.

[26] (1999, reaff. 2003) IEEE std 802.11a-1999(R2003). IEEE-SA Standards Board. [Online]. Available: http://standards.ieee.org/getieee802/download/802.11a-1999.pdf

[27] I. Bhatti, R. Roufoogaran, and J. Castaneda, "A fully integrated transformer-based front-end architecture for wireless transceivers," in *IEEE ISSCC Digest of Technical Papers*, San Francisco, CA, Feb 2005, pp. 106–107.

[28] A. Bevilacqua, C. Sandner, A. Gerosa, and A. Neviani, "A fully integrated differential CMOS LNA for 3-5-GHz ultrawideband wireless receivers," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 3, pp. 134–136, 2006.

[29] D. Manstretta, M. Brandolini, and F. Svelto, "Second-order intermodulation mechanisms in cmos downconverters," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 03, pp. 394–486, 2003.