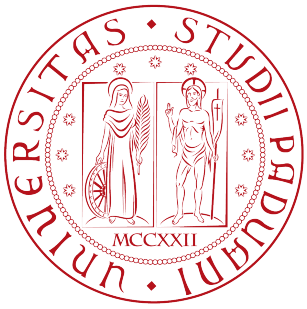

Università degli studi di Padova
Dipartimento di Ingegneria dell'Informazione

Analysis and Design of a Wide-Bandwidth Low Power Sigma-Delta ADC in CMOS Technology

Tesi di: Alberto CELIN

Scuola di Dottorato in Ingegneria dell'Informazione
Indirizzo in Scienza e Tecnologia dell'Informazione
Ciclo XXIX

Supervisore
Chiar.mo Prof. Andrea Gerosa

Direttore della Scuola
Chiar.mo Prof. Matteo Bertocco

Coordinatore di Indirizzo
Chiar.mo Prof. Carlo Ferrari

I can't change the direction of the wind,
but i can adjust my sails to always reach my destination.

— Jimmy Dean

To my mother and to my father.

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I thank whatever gods may be
For my unconquerable soul.
I am the master of my fate
I am the captain of my soul.

— Nelson Mandela

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Sommario

L'evoluzione delle tecnologie CMOS ha portato a molte sfide per i designer di circuiti analogici. La riduzione delle dimensioni dei transistor ha un grande impatto sul design del circuito analogico, in quanto ne degrada in modo considerevole le performance. Ad esempio, la ridotta tensione di alimentazione e la degradazione delle caratteristiche dei dispositivi sono problemi inevitabili per i designer di dispositivi CMOS. In quanto interfaccia tra i circuiti analogici e quelli digitali, il convertitore Analogico Digitale (ADC) si sta muovendo verso tecnologie CMOS ultra-scalate al fine di godere dei vantaggi che lo scaling tecnologico porta sulla circuiteria digitale. Questo pone una crescente difficoltà nel design degli ADC.
I convertitori Sigma-Delta ($\Sigma\Delta$) sono dei promettenti candidati per la conversione analogico-digitale (A/D). La ragione di ciò è duplice. Da un lato, a differenza degli altri convertitori che necessitano di elementi molto performanti per ottenere risoluzioni elevate, i convertitori $\Sigma\Delta$ mostrano una elevata robustezza alle imperfezioni dei blocchi che li compongono. Questo è ottenuto grazie ad un esteso utilizzo di cricuiteria digitale, che nelle tecnologie CMOS scalate risulta preferibile grazie al suo basso consumo di potenza e all'elevata densità. D'altra parte, anche il numero di applicazioni industriali è cresciuto. Infatti, a cominciare dalle prime applicazioni in campo audio, possiamo trovare convertitori $\Sigma\Delta$ in una gran varietà di interfacce A/D, come strumentazioni biomediche fino al campo delle comunicazioni.
Nonostante l'architettura $\Sigma\Delta$ sia un soggetto ormai maturo, ci sono tutt'ora diverse questioni irrisolte. A causa della presenza di un elemento fortemente non lineare, il quantizzatore, all'interno del loop di feedback, l'analisi esatta della modulazione $\Sigma\Delta$ risulta complicata. In questa tesi, un approccio a livello circuitale e a livello di sistema viene presentato per il design di un convertitore ADC a bassa potenza e a bassa tensione di alimentazione in tecnologia nanometrica CMOS. Nella prima parte di questo lavoro, viene introdotta una particolare topologia $\Sigma\Delta$ adatta al design di convertitori in tecnologia nanometrica. La caratteristica piú importante di questa topologia è la funzione di trasferimento tra ingresso e uscita unitaria. Viene presentata un'analisi dettagliata, portando alla scelta ottimizata di parametri di sistema. Viene inoltre presentata una nuova circuiteria digitale per estendere l'uso del modulatore $\Sigma\Delta$ a bande più elevate.
La seconda parte di questa tesi è dedicata al design circuitale. Il principale raggiungimento di questo lavoro è un modulatore $\Sigma\Delta$ in tecnologia 65nm con un range dinamico di 94dB. Il consumo di potenza è 407μW in un banda di 500kHz con una tensione di alimentazione di 1.2V. Questo design dimostra che la topologia $\Sigma\Delta$ feedforward è una scelta eccellente per il design di ADC a bassa potenza, elevata banda ed elevata risoluzione in tecnologie nanometriche CMOS.

Abstract

The evolution of the CMOS technology brings many challenges to analog designers. The scaling-down of the transistor feature size has a big impact on analog circuit design, because it considerably degrades the performance of an analog circuit. For instance, the reduced supply voltage and the degraded device characteristics are inevitable problems for CMOS designers. As an interface between the analog circuit and the digital circuit, the Analog-to-Digital Converter (ADC) is moving into scaled nanometer CMOS technologies due to the advantages for the digital circuit. This put increasingly difficult demands on the design ADCs.
Sigma-Delta ($\Sigma\Delta$) ADCs are promising candidates for the Analog-To-Digital (A/D) conversion. The reason for that is twofold. One the one hand, unlike the other converters that need accurate building blocks to obtain high resolution, $\Sigma\Delta$ converters show low sensitivity to the imperfections of their building blocks. This is achieved thanks to the extensive use of digital circuitry, which is preferred in CMOS technologies due to their low power and high density characteristics. On the other hand, the number of applications with industrial interest has also grown. In fact, starting from the earliest in the audio band, we can find $\Sigma\Delta$ converters in a large variety of A/D interfaces, ranging from instrumentation to communications.
Despite the fact that $\Sigma\Delta$ is a mature subject, there are still many unanswered questions. Due to the incorporation of a highly non-linear element (the quantizer) in the feedback loop, the exact analysis of $\Sigma\Delta$ modulation is a very challenging task. In this thesis the circuit level approach and the system level approach are presented for low-power, low-voltage $\Sigma\Delta$ ADC design in nanometer CMOS technologies. In the first part of this work, a full-feedforward $\Sigma\Delta$ topology suitable for the $\Sigma\Delta$ ADC design in nanometer CMOS technologies is introduced. The most important feature of this topology is that the signal transfer function is unity, which is fairly indipendent of the building block characteristics. A detailed analysis is presented in this text, leading to optimized system-level parameters. Also a new digital circuitry is presented in order to extend the usage of $\Sigma\Delta$ modulators at higher signal bandwidths.
The second part of the thesis is dedicated to the circuital design. The main achievement is a 65nm CMOS $\Sigma\Delta$ modulator with 94dB Dynamic Range (DR). The power dissipation is 407μW in a 500kHz signal bandwidth under a 1.2V power supply voltage. This design proves that the feedforward $\Sigma\Delta$ topology is an excellent topology for low-power, high bandwidth and high resolution $\Sigma\Delta$ ADC designs in nanometer CMOS technologies.

Contents

Acknowledgements **vii**

Abstract **xi**

List of Figures **xvii**

List of Tables **xxiii**

1 Introduction **1**
1.1 Motivations 1
1.2 System Overview 3
1.3 System Challenges 5
1.4 Conclusions and Thesis Outline 8

2 Sigma-Delta Overview **11**
2.1 Introduction 11
2.2 Fundamental of Sigma Delta Modulation 11
2.2.1 Oversampling 12
2.2.2 Noise Shaping 15
2.2.3 Topology of ΣΔ ADCs 16
2.2.4 Definition of Performance Metrics for a ΣΔ ADC 18
2.2.5 Higher Order ΣΔ ADC 19
2.2.6 Digital Filter 20
2.3 Non-idealities in Discrete Time ΣΔ Modulators 21
2.3.1 Effect of Finite Amplifier DC-gain 23
2.3.2 Integrator Settling Error 25
2.3.3 Effect of Finite Amplifier GBW 28
2.3.4 Effect of Finite Amplifier SR 30
2.3.5 Effect of Circuit Noise 30
2.3.6 Effect of Clock Jitter 32
2.4 Continuous Time ΣΔ Modulators 33
2.5 Conclusion 34

3 System Analysis **35**
3.1 Introduction to Feed-Forward Topology 35
3.2 FF and FB ΣΔ - Comparison 38
3.2.1 Single Loop 38
3.2.2 Lower Distortion 39

3.2.3 Amplifier Requirements . . . 40
3.2.4 Multi-bit Quantization . . . 43
3.3 Dynamic Element Matching . . . 44
3.3.1 Butterfly Randomization . . . 46
3.3.2 Individual Level Averaging (ILA) . . . 47
3.3.3 Data Weighted Averaging (DWA) . . . 49
3.3.4 DWA Second-Order (DWA2) . . . 53
3.3.5 Randomized DWA (RnDWA) . . . 56
3.3.6 Partitioned DWA (PDWA) . . . 57
3.3.7 Bi-Directional DWA (BiDWA) . . . 58
3.4 System-Level Design . . . 60
3.4.1 Power Consumption Minimization . . . 61
3.4.2 Quantizer Power Consumption . . . 62
3.4.3 Amplifier Power Consumption . . . 62
3.4.4 Proposed DWA (NewDWA) . . . 65
3.4.5 Analog Adder . . . 69
3.4.6 OTAs Requirements . . . 70
3.5 Conclusion . . . 73

4 Design and Simulation **75**
4.1 First Integrator . . . 75
4.1.1 Switches . . . 75
4.1.2 Amplifier . . . 79
4.1.3 Biasing and CMFB . . . 81
4.2 Second Integrator . . . 84
4.2.1 Amplifier . . . 84
4.3 Analog Adder . . . 86
4.3.1 Amplifier . . . 88
4.4 Comparator . . . 93
4.4.1 Background . . . 93
4.4.2 Dynamic Comparator . . . 95
4.4.3 Proposed Comparator . . . 97
4.4.4 Reference Voltage Generation . . . 103
4.5 Digital Circuitry . . . 105
4.5.1 DWA . . . 105
4.5.2 Logarithmic Shifter . . . 105
4.5.3 Binary Encoder . . . 105
4.5.4 Full Adder . . . 107
4.5.5 Timing Requirements . . . 109
4.5.6 BiDWA . . . 112
4.5.7 NewDWA . . . 114
4.6 Conclusion . . . 116

5 Measurement Setup **119**
5.1 Background . . . 119
5.2 Fixed-Frequency Solution . . . 120
5.3 Variable-Frequency Solution . . . 122

6 Conclusion **127**

A Error estimation in DEM **131**
A.1 Worst-Case DAC Mismatch Effect 131
A.2 SNR Butterfly Algorithm 132
A.3 SNR General DEM 133
A.4 SNR DWA 135

List of Publication **137**

Bibliography **139**

List of Figures

1.1 Evolution of technology nodes in semiconductor manufacturing processes. 2
1.2 Supply voltages used for scientifically reported CMOS ADCs over time (black points). Data points (blue diamonds), representing the evolution of low-voltage state-of-the-art, have been highlighted. Trend line fit to 1985-2007 data. 3
1.3 General blocks of a ΣΔ ADC. 4
1.4 On the left a two-level DAC with the output values versus its two possible input values. On the right a multi-level DAC. 5
1.5 Threshold and supply voltages versus technology node 6
1.6 Transistor intrinsic gain versus CMOS minimum channel length . . 7
1.7 Output signal swings in different output stages 7

2.1 General block diagram of an A/D converter. A Nyquist-rate ADC is assumed. 12
2.2 Antialiasing filter for (a) Nyquist-rate ADCs and (b) oversampling ADCs. 13
2.3 Illustration of the quantization process for a multi-bit quantizer. In (a) the I/O characteristic of the quantizer is depicted, while in (b) the multi-bit quantization error is shown. 13
2.4 Quantization noise for (a) Nyquist-rate ADCs and (b) oversampling ADCs. 14
2.5 Quantization noise shaping: (a) conceptual block diagram and (b) effect on the in-band noise of an oversampling noise-shaping ADC. 15
2.6 Main blocks of a DT ΣΔ modulator. 16
2.7 ΣΔ modulator: (a) block diagram and (b) ideal linearized model. . 17
2.8 Illustration of a typical output spectrum of a ΣΔ modulator and its main characteristics. 18
2.9 Illustration of the performance metrics of a ΣΔ modulator on a typical SNR-SNDR curve. 19
2.10 Root locus in Z-plane for a second-order modulator and a third-order modulator. 20
2.11 Output spectrum of the quantizer and its filtered version after the decimation filter. 21
2.12 Fully-differential implementation of a first-order DT ΣΔ modulator. 22
2.13 Main non-idealities affecting the performance of SC ΣΔ modulators. 22
2.14 SC integrator with N input paths and finite amplifier gain A_V . . . 23

2.15 Simulation results for the influence of limited DC-gain amplifier on the in-band noise of SC ΣΔ modulators. 24
2.16 Multi-input path SC integrator followed by a loading multi-input path SC integrator. 26
2.17 Amplifier single-pole model. 26
2.18 Simulation results for the influence of amplifier GBW on the in-band noise of SC ΣΔ modulators. 29
2.19 Simulation results for the influence of amplifier SR on the output spectrum of SC ΣΔ modulators. 30
2.20 Equivalent circuit model for integration, with noise sources due to switches and due to the amplifier. 31
2.21 General block diagram of a continuous-time ΣΔ ADC. A low pass modulator is assumed. 33

3.1 ΣΔ topologies: (a) the traditional FB topology; (b) the FF reduced distortion topology. 36
3.2 Second-order FF ΣΔ modulator. 37
3.3 Output swing of integrators in a second-order FF ΣΔ with a 5 bit internal quantizer. 38
3.4 Second-order FB ΣΔ modulator. 38
3.5 Loading SC Integrator for ΣΔ modulators: (a) Integrator Load for a FB ΣΔ, (b) Integrator Load for a FF ΣΔ. 39
3.6 Behavioral simulation of the otuput SNDR: (a) in FB topology; (b) in FF topology. Thermal noise is included in this simulation. . . . 40
3.7 SNR as a function of the gain of the first integrator in a FF topology with a 4 bit embedded quantizer and a FB topology with a single bit embedded quantizer. Dashed line represents the ideal case. . . 42
3.8 SNR as a function of the bias current I_{bias} of the first integrator in a FF topology with a 4 bit embedded quantizer and a FB topology with a single bit embedded quantizer. Dashed line represents the ideal case. 42
3.9 Topology of a typical multi-bit quantizer embedded in a ΣΔ modulator. 44
3.10 No DEM: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations. 45
3.11 Topology of a typical multi-bit feedback DAC in a ΣΔ modulator with DEM algorithm. 45
3.12 Randomization of the selection of unity elements with a butterfly randomizer with three bit control. 46
3.13 Butterfly DEM: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations. 47
3.14 SNR as a function of the OSR and of the mismatch among unit elements when Butterfly randomization is applied. The solid line represents the simulated results, while the dashed line represents the mathematical modeling. 48

3.15 Operation principle of the (a) rotation approach and of the (b) addition approach of ILA. The shaded boxex indicate which unit elements contribute positive for a 3 bit DAC employing ILA. . . . 48
3.16 ILA DEM: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in the rotation approach, and for low OSR case (c) and high OSR case (d) in the addition approach. A second-order FF modulator is considered. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations. 49
3.17 Operation principle of the rotation of DWA. The shaded boxex indicate which unit elements contribute positive for a 3 bit DAC employing DWA. 50
3.18 DWA: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations. 51
3.19 SNR as a function of the OSR and of the mismatch among unit elements when DWA is applied. The solid line represents the simulated results, while the dashed line represents the mathematical modeling. 52
3.20 Updating rule for a second-order DWA. The input sequence $1-6$ is considered respectively in (a) and (b). 53
3.21 DWA2: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations. 54
3.22 Comparison between common DEM algorithms in terms of SNDR as a function of the OSR. 54
3.23 Comparison between DWA and DWA2 in presence of thermal noise. Several sizes of sampling capacitors are considered. 55
3.24 Operation principle of the rotation of RnDWA. The shaded boxex indicate which unit elements contribute positive for a 3 bit DAC employing RnDWA. 56
3.25 RnDWA: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations. 56
3.26 Operation principle of the rotation of PDWA. The shaded boxex indicate which unit elements contribute positive for a three-bit DAC employing PDWA. 57
3.27 PDWA: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations. 57
3.28 Operation principle of the rotation of BiDWA. The shaded boxex indicate which unit elements contribute positive for a 3 bit DAC employing BiDWA. 58
3.29 BiDWA: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations. 58
3.30 The topology of the $\Sigma\Delta$ modulator used for this design. 61
3.31 The power consumption in the $\Sigma\Delta$ modulator with respect to the number of bits of the internal quantizer. 63

3.32 SNR as a function of the gain of the first integrator in a FF topology with a 4 bit embedded quantizer and with a 5 bit embedded quantizer. Dashed line represents the ideal case. 64
3.33 SNR as a function of the bias current I_{bias} of the first integrator in a FF topology with a 4 bit embedded quantizer and with a 5 bit embedded quantizer. Dashed line represents the ideal case. 64
3.34 Operation principle of the rotation of (a) BiDWA and (b) NewDWA. The shaded boxex indicate which unit elements contribute positive for a 3 bit DAC. 65
3.35 NewDWA: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations. 67
3.36 SFDR of BiDWA and NewDWA for a FF $\Sigma\Delta$ second-order modulator as a function of the OSR. A $\sigma_w = 2\%$ is considered for this simulation. 68
3.37 Output spectra of a FF $\Sigma\Delta$ second-order modulator with a 5 bit internal quantizer when DWA is applied and when NewDWA is applied. 68
3.38 Analog Adder implementation: (a) Summing using Charge Sharing, (b) Summing using an Active Adder 69
3.39 The $\Sigma\Delta$ modulator circuit used for this design. 71
3.40 Output spectrum of second-order FF $\Sigma\Delta$ modulator: (a) not performing adder amplifier compared with an ideal adder; (b) performing adder amplifier compared with and ideal adder. 72
3.41 Dynamic Range of the proposed design. 73

4.1 Implementation of the First Integrator with the embedded multi-bit DAC. 76
4.2 Inverse of the switch on-resistance as a function of the signal voltage for (a) an nMOS switch, (b) a CMOS switch with high supply voltage and (c) a CMOS switch with low supply voltage. 77
4.3 Implementation of bootstrap circuit and switching device. 78
4.4 Simulation of the bootstrap circuit. 79
4.5 Telescopic OTA. 80
4.6 Bode diagram of the transfer function of the Telescopic OTA realizing the first integrator. 81
4.7 Simulation of the the transfer function of the Telescopic OTA realizing the first integrator in all the process corners (Nominal, FF, FS, SF, SS). 81
4.8 Montecarlo simulation of the transfer function of the Telescopic OTA realizing the first integrator. 82
4.9 Biasing of the Telescopic OTA. 82
4.10 Switched Capacitor CMFB. 83
4.11 Implementation of the Second Integrator. 84
4.12 Bode diagram of the transfer function of the Telescopic OTA realizing the second integrator. 85
4.13 Simulation of the the transfer function of the Telescopic OTA realizing the second integrator in all the process corners (Nominal, FF, FS, SF, SS). 86

4.14 Montecarlo simulation of the transfer function of the Telescopic OTA realizing the second integrator. 86
4.15 Implementation of the analog adder. 87
4.16 OTA topology used for the analog adder. 88
4.17 Parasitic capacitance and internal pole in the proposed OTA. . . . 89
4.18 Bode diagram of the transfer function of the OTA realizing the analog adder. 91
4.19 Simulation of the the transfer function of the OTA realizing the analog adder in all the process corners (Nominal, FF, FS, SF, SS). 91
4.20 Montecarlo simulation of the transfer function of OTA realizing the analog adder. 92
4.21 Simulation of the loop gain of the OTA realizing the analog adder. 92
4.22 Biasing of the OTA realizing the analog adder. 93
4.23 Comparator with pre-amplifier topology. 94
4.24 Effect of kickback noise. 95
4.25 Resistive divider dynamic comparator. 96
4.26 Differential pair comparator. 97
4.27 Proposed dynamic comparator. 98
4.28 Positive output of the proposed dynamic comparator in function of the size of the switches M_5 and M_6. 98
4.29 Positive output of the proposed dynamic comparator. 99
4.30 Output of the Set-Reset Latch after the comparator. 100
4.31 Montecarlo simulation of the output transient response of the comparator. 101
4.32 Histogram of the offset of the comparator. 101
4.33 Input/Output Characteristic of the 5 bit embedded quantizer. . . . 102
4.34 Montecarlo simulation of the input/output characteristic of the 5 bit embedded quantizer. 102
4.35 Voltage reference glitch caused by kickback noise. 103
4.36 Reference voltage generation for the 5 bit internal quantizer. . . . 104
4.37 Reduced voltage reference glitch caused by kickback noise with the capacitor solution. 104
4.38 An optimized implementation of the first-order DWA algorithm. . . 105
4.39 Three-stage multiplexer based logarithmic shifter. 106
4.40 An example of the basic operation of a three-stage logarithmic shifter. 106
4.41 Three bits MUX based encoder. 107
4.42 An example of the basic operation of a MUX based encoder. 107
4.43 Single cell 5 bit full adder. 108
4.44 An example of the basic operation of the single-cell full adder. . . . 108
4.45 First-order FF $\Sigma\Delta$ modulator with input feedforward and its timing diagram. 109
4.46 Physical implementation of the circuit used to generate the two non-overlapping phases. 110
4.47 Transient simulation of the 11th bit of signals *Therm-Code* and *Shuff-Code* and of the 2nd bit of signals *Enc-Code*, *ptr*, and *next-ptr*; the time axis is divided in two sets, in order to zoom around the rising and the falling edge of phase Φ_2, respectively. 111

4.48 Transient simulation of the delay introduced by DWA when the logarithmic shifter is implemented with pass transistor or transmission gate logic. . . . 112
4.49 Implementation of the BiDWA algorithm. . . . 113
4.50 Feedback delay introduced by DWA and BiDWA algorithm. . . . 113
4.51 Implementation of the NewDWA algorithm. . . . 114
4.52 Critical path for a single bit line of the (a) NewDWA algorithm and of the (b) BiDWA algorithm. . . . 115
4.53 Feedback delay introduced by NewDWA and BiDWA algorithm. . . . 115
4.54 Validation of the behavioral model with a transistor-level simulation. 116
4.55 Time response of the $\Sigma\Delta$ output filtered by the CIC filter. . . . 117
4.56 Pie chart of the power consumption of the proposed design. . . . 117

5.1 Spectrum of the sine-wave generated by a common laboratory instrument as the HP33250A. . . . 120
5.2 Spectrum of the wave generated by a crystal quartz oscillator. . . . 121
5.3 Low-pass filtering of the crystal quartz oscillation. . . . 121
5.4 Spectrum of the filtered wave produced by the crystal quartz oscillator. . . . 122
5.5 Basic Wien-bridge oscillator circuit. . . . 123
5.6 (a) Classical Wien-Bridge network and (b) rearranged Wien network. 124
5.7 Low distortion oscillator based on the Wien-Bridge topology. . . . 124
5.8 Ultra low distortion oscillator used for the ADC test. . . . 125
5.9 Output noise of the proposed oscillator versus the oscillation frequency. . . . 126
5.10 Output spectrum of the low distortion oscillator used for the ADC test. . . . 126

6.1 Layout of the proposed design of the $\Sigma\Delta$ modulator. . . . 127
6.2 Photo of the die. . . . 128
6.3 Measured output spectrum of the proposed design. . . . 129

List of Tables

3.1 Comparison between Single-Stage OTAs and the Miller OTA. . . . 41
3.2 Comparison of the main DEM algorithms at OSR = 16 in terms of SNR and SFDR. . . . 59
3.3 Comparison of the main DEM algorithms at OSR = 8192 in terms of SNR and SFDR. . . . 60
3.4 Sizing of the capacitors of the proposed design. . . . 70
3.5 Minimum specifications of the analog blocks of the modulator. . . 72
3.6 System-Level parameters of the proposed design. . . . 73

4.1 Characteristics of the Telescopic Cascode topology. . . . 80
4.2 Effect of parameters variation in CMFB network. . . . 84
4.3 Characteristics of the proposed OTA topology. . . . 90
4.4 Comparison of DWA, BiDWA and the proposed algorithm in terms of time delay, power consumption and area. . . . 116

Chapter 1

Introduction

1.1 Motivations

Silicon integrated circuit technology, including transistors and other electronic components, are dependent on micro and nanoelectronic technologies. Regarding to the cost of transistor fabrication and high-volume production, integrated circuits are highly demanded in various applications in human activities such as telecommunication, medical, education and others.
Though our world has an analog nature, nowadays information is very often stored, transferred and processed digitally. The advantage is obvious: digital signals are much more immune to noise than their analog counterparts. Noise and distortion will accumulate during the transfer or copy of an analog signal, while a digital signal can be losslessly copied or transferred as long as the noise and distortion are lower than the threshold which changes the digital value. Moreover signal processing circuits can be implemented more easily, accurately and economically in digital domain thanks to the fast and continuous development of CMOS process.
Driven by the speed demand of digital circuits, the CMOS technology is continuously scaling-down. It is worth mentioning that shrinking the size of MOSFETs not only increases the performance speed, by decreasing the parasitic capacitors of the devices and the interconnections, but also decreases the energy consumption of the device. In the last years, due to well-developed techniques in deposition, pattering and characterization, the size of electronic components has been decreasing from above 100nm to about 20nm today. There is a significant improvement in node technology in last decades as the 10μm technology node reached the 22nm in 2011, as shown in Figure 1.1.
It is apparent in Figure 1.1 that the evolution of technology nodes follows the well known Moore's law [1], which states that the number of component for integrated circuits doubles every year. Although there is enough motivation for shrinking the size of the transistors, as the higher integration of the devices, some issues should be addressed before reaching the limit. Obviously a limiting factor is the economical issues since the cost of fabrication for integrated circuits increases strongly by reducing the size of the components. However, from the designer point of view, the major problem is that the reduction of the size of transistors has led at the same time also to the reduction of the supply voltage. Moreover, portable electronics

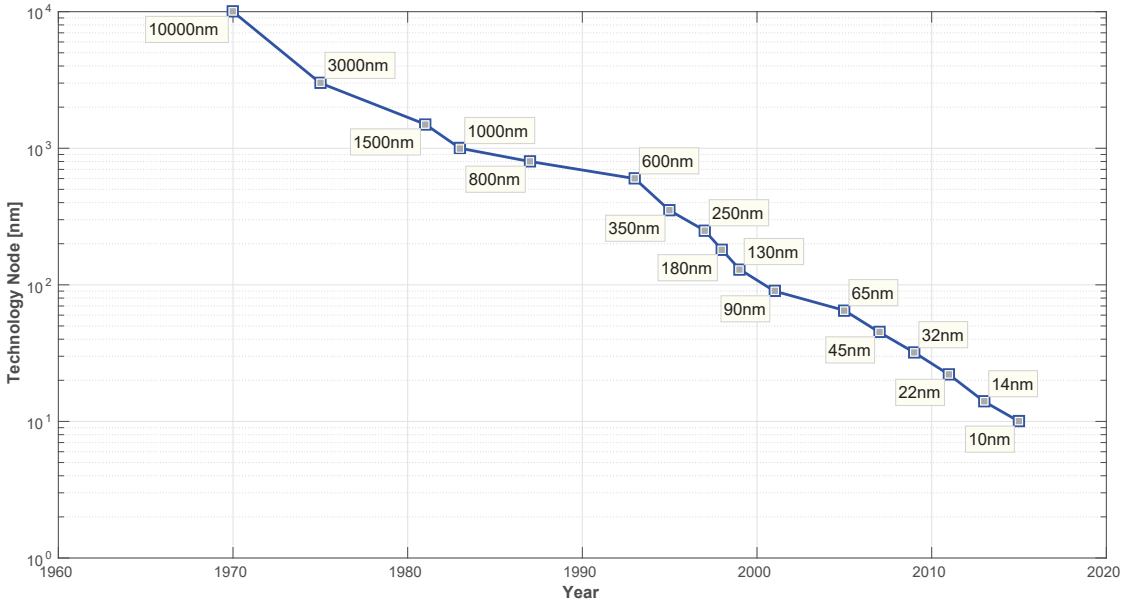


Figure 1.1: Evolution of technology nodes in semiconductor manufacturing processes.

with low-voltage operation and, therefore, long life battery find big markets. All these factors have made the low-voltage circuit design a hot topic recently.
However, the low supply voltage constraint makes the analog design challenging due to the reduced signal swing. On the other hand, the scaling-down of the CMOS technology results into the degradation of the device characteristics, making the analog Integrated Circuit (IC) design in nanometer CMOS technologies more challenging. As previously mentioned, the digital circuitry is a crucial point in the majority of applications. In order to transform the analog information into digital information an Analog-to-Digital Converter (ADC) is used. Being an interface between the analog world to the digital circuit, the ADC is implemented with the same technology as the digital circuit. As a result, the reduction of the power supply voltage of the ADC is inevitable.
Figure 1.2 shows the voltage supplies reported for CMOS Analog-to-Digital (A/D) converters reported in scientific publications [2,3]. Observing the hystorical trend of Figure 1.2, fitting to the state-of-the-art data from 1985–2007, yields that the lowest reported V_{DD} was scaled by $\sim$2$\times$ every five years during this period. It is also evident from the number of papers published in the last years the increasing attention for sub-1V supply voltage [4], in line with the increasingly stringent requirements of the industry with regard to low-power applications. The reduction of the supply voltage, combined with the reduction of the parasitic capacitance, brings to a reduction of the power consumption of the circuit. For a CMOS logic gate, e.g. an inverter, the static and dynamic power consumption can be expressed as:

$$P_{static} = V_{DD} \cdot I \tag{1.1}$$

$$P_{dynamic} = C_L \cdot V_{DD}^2 \cdot f. \tag{1.2}$$

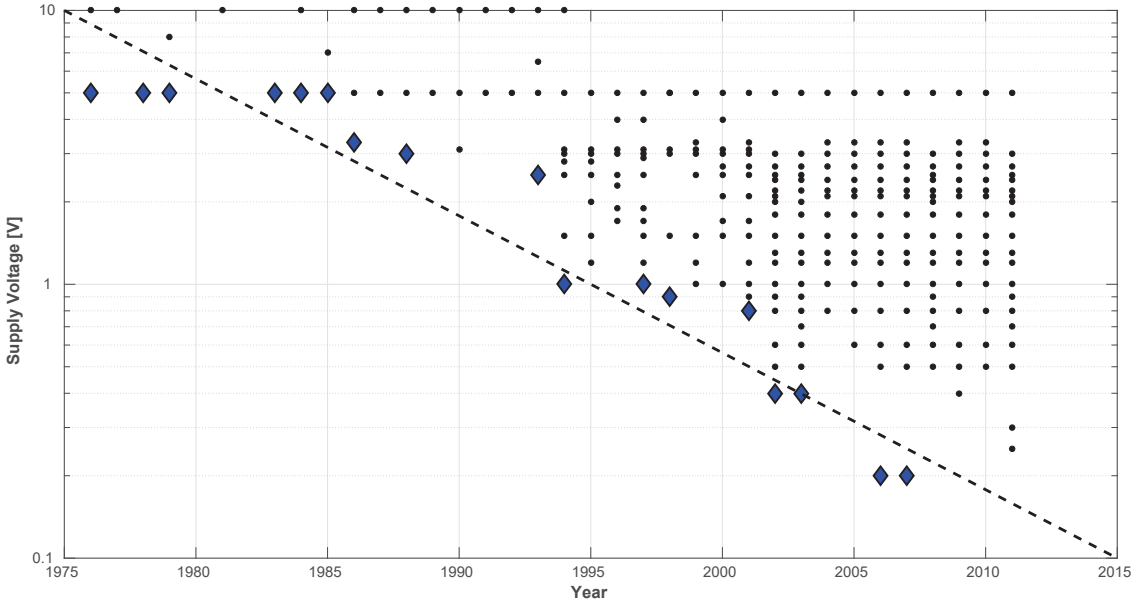


Figure 1.2: Supply voltages used for scientifically reported CMOS ADCs over time (black points). Data points (blue diamonds), representing the evolution of low-voltage state-of-the-art, have been highlighted. Trend line fit to 1985-2007 data.

In these equations V_{DD} plays a fundamental role in the reduction of the overall power consumption. However this reduction in the power consumption has drawbacks. In fact the decrease of the supply voltage obviously results into a performance degradation of the ADC. Generally speaking, to maintain the same dynamic range in a system, the noise floor should be lowered while the signal swing is reduced. Moreover the distortion problem tends to be more severe with the reduction of the supply voltage reduction [5].

1.2 System Overview

Among different ADCs, the Sigma-Delta ($\Sigma\Delta$) ADC is most suitable for high-resolution applications due to its high linearity feature. Compared to other kinds of ADCs, $\Sigma\Delta$ modulators cover the widest conversion region of the resolution-versus-bandwidth plane, being the most efficient solution to digitize very diverse types of signals in an increasing number of application scenarios, which span from high-resolution low-bandwidth data conversion (like digital audio, sensor interfaces, and instrumentation) to ultra-low power biomedical systems and medium-resolution broadband wireless communications. This versatility, together with their robustness and their simplicity in many practical situations, has motivated that more and more engineers today consider $\Sigma\Delta$ as a first choice for their research projects and their industrial products. The first idea underlying the operation of $\Sigma\Delta$ modulators was patented by Cutler in 1960 [6], although its application to the construction of data converters was first reported in the published literature by Inose in 1962 [7].

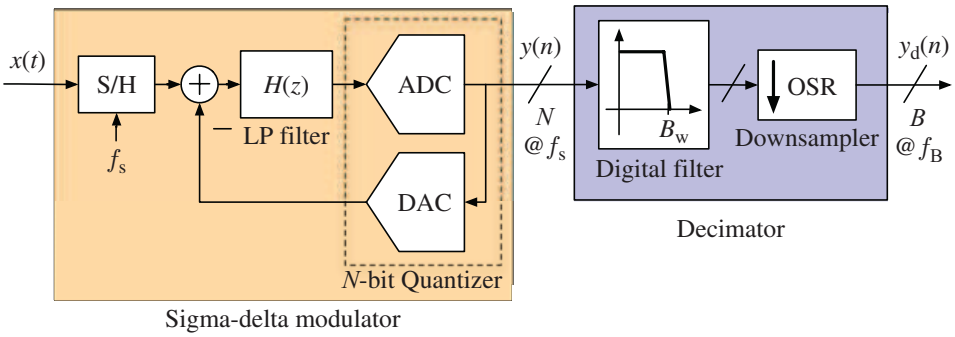


Figure 1.3: General blocks of a ΣΔ ADC.

The general architecture of a ΣΔ modulator is reported in Figure 1.3. The fundamental principle behind ΣΔ modulators is based on the combination of two signal processing techniques, namely oversampling and quantization noise shaping. The former consists of taking the signal samples at a higher rate than the one dictated by the Nyquist sampling theorem. These samples are commonly quantized with a large error by using a low-resolution quantizer. The resulting oversampled quantization error is filtered in the modulator feedback loop, so that its frequency spectrum is shaped in such a way that a large portion of its power is pushed out of the signal band, where it is removed by a digital filter. The outcome of the combined action of oversampling and noise shaping allows ΣΔ modulators to achieve a high precision digitization by using a low-resolution coarse quantizer. Therefore, unlike other kinds of ADC architectures that require high-precision analog circuits, ΣΔ modulators trade the accuracy of their analog circuitry by the speed of digital signal processing, thus achieving a higher degree of insensitivity to circuit error mechanisms and potentially benefiting from CMOS technology evolution towards the nanometer scale.
However, in order to increase the resolution of the ΣΔ modulator, the designers generally increase the oversampling value. Therefore the ΣΔ modulators were generally relegated to low-bandwidth applications [8]. In order to extend the usage of ΣΔ modulation into the wide-band applications the designers start to think to other solutions. One possibility is to increase the sampling frequency, which however is not recommended since it limits the settling of the amplifiers, how it will be more clear in Chapter 2. Moreover, as reported in Equation (1.2), increasing the sampling frequency brings to an increase of the dynamic power consumption. Another solution is to increase the noise-shaping power by increasing the number of integration stages. The main concern of this solution is the stability problem, and therefore the order of ΣΔ modulators is generally small.
The most interesting solution is to increase the resolution of the internal quantizer. Using an N bit quantizer instead of 1 bit quantizer can reduce the quantization error by a factor of 2^N, thus increase the resolution by $6.02N$dB. This resolution increase is not related to the oversampling ratio. Moreover, since the multi-bit quantizer gives a more accurate prediction of the current input than a 1 bit quantizer does, the input to the integrators is smaller. In fact, as apparent from Figure 1.3, the output of the quantizer is fed-back to the input of the Low Pass (LP) filter, namely

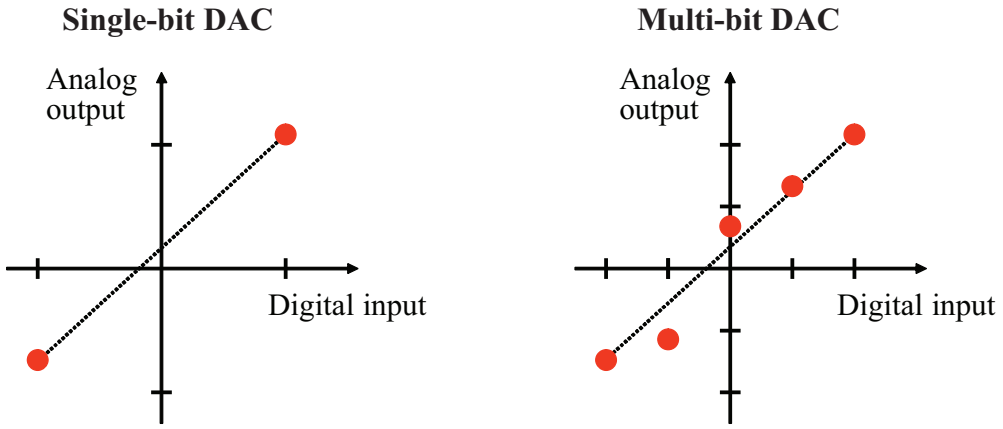


Figure 1.4: On the left a two-level DAC with the output values versus its two possible input values. On the right a multi-level DAC.

the integrator. As a result the integrator has lower possibility to saturate and the stability is improved. Furthermore this helps in the context of low-voltage applications since it reduces the swing values needed for the amplifier to work in its linear region.

1.3 System Challenges

For a multi-bit Sigma Delta modulator the biggest problem that has to be solved is the multi-bit Digital-to-Analog converter (DAC) non-linearity, which is not noise-shaped. This is evident in Figure 1.4. The $\Sigma\Delta$ ADC is often only 1 bit, taking the advantage that a 1 bit DAC is inherently linear since it has only two output levels. Adding even only one level to the DAC breaks the intrinsic linearity of the two-levels DAC, since three points are not always connected by a straight line [9]. In order to solve the non-linearity problem of a single-stage multi-bit modulator, one method is to use digital corrections as Dynamic Element Matching (DEM) circuits. A DEM circuit can randomize or noise-shape the DAC non-linearity. This method does not need calibration, but the DEM is not free of limitations. In fact the DEM algorithm needs a digital circuitry that can ruin the stability of the overall modulator. Moreover, as it will be demonstrated in this thesis and in particular in Chapter 3, the DEM algorithm suffers of a non-linear behavior when the oversampling ratio (OSR) is low.
Despite the already mentioned advantages of the multi-bit architecture regarding the low-voltage supply range applications, the design in this field is not free from issues. In fact, the decreasing feature size of the modern CMOS process gives rise to the scaling of the threshold voltage (V_{TH}), but not in proportion to the reduction of the supply voltage, as shown in Figure 1.5. This figure shows also that for deeper technology (from 45nm), the V_{TH} inverts the decreasing trend of the last steps in order to reduce leakage current and short channel effects. The

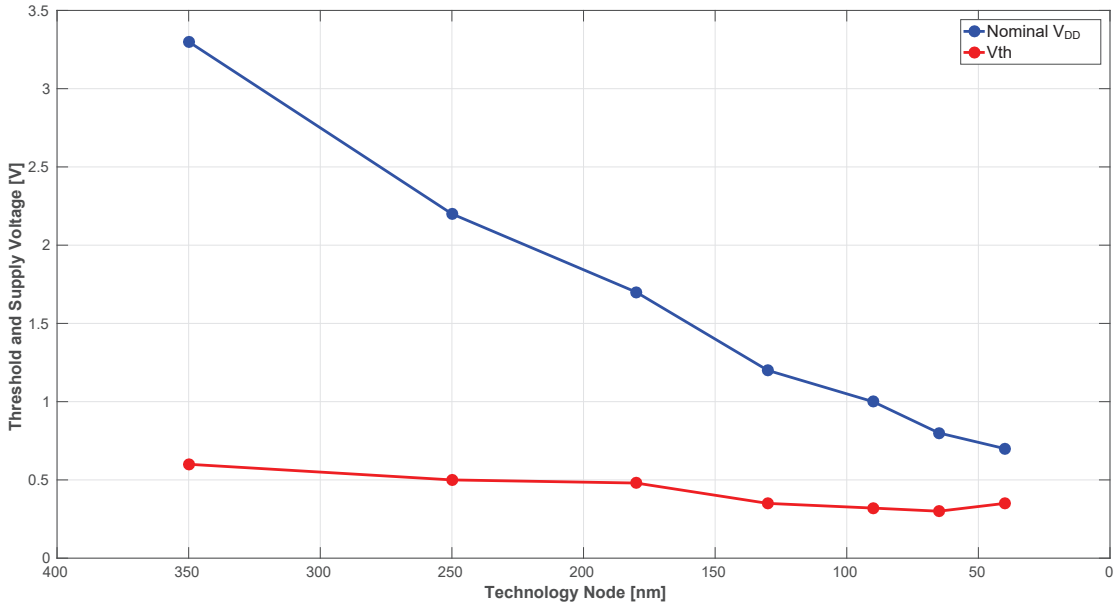


Figure 1.5: Threshold and supply voltages versus technology node

fact that the downsizing of V_{TH} is decelerated implies that the overdrive voltage ($V_{OV} = V_{DD} - V_{TH}$) is reduced, and therefore the design of analog blocks becomes even more difficult [10]. Since the technology scaling implies the reduction of the overdrive voltage V_{OV}, an increase of the transconductance g_m of the transistor is obtained. In fact, the transconductance of the transistor in strong inversion and subthreshold region is given by the following expression:

$$g_m = \frac{2I_D}{V_{OV}}, \tag{1.3}$$

therefore reducing the overdrive voltage leads to an increase of the transconductance of the transistor. However, this does not ensure a higher DC-gain of the MOS. In fact, the intrinsic gain of a MOS transistor is defined as:

$$A_0 = \frac{g_m}{g_{ds}} = g_m r_0, \tag{1.4}$$

where $g_{ds} = 1/r_0$ is the output conductance of the active MOS transistor. The intrinsic gain is actually the maximum gain that a transistor can reach. It is the amplification ability of a MOS transistor. Even though MOS transistor transconductance tends to be larger when the scaling down increases, as expressed in Equation (1.3), the output resistance r_0 drop is so high that the transistor intrinsic gain decreases. In fact, due to short-channel effects related with CMOS shrinking, the output conductance is increased strongly. This fact is clearly shown in Figure 1.6. The result shown in Figure 1.6 implies a big problem for the design of operational amplifiers. In fact, the reduction of the intrinsic gain of the transistor results in a reduction of the DC-gain of the amplifier. In particular the finite opamp gain in $\Sigma\Delta$ modulator can produce the well known effect of dead zones. In fact, for certain

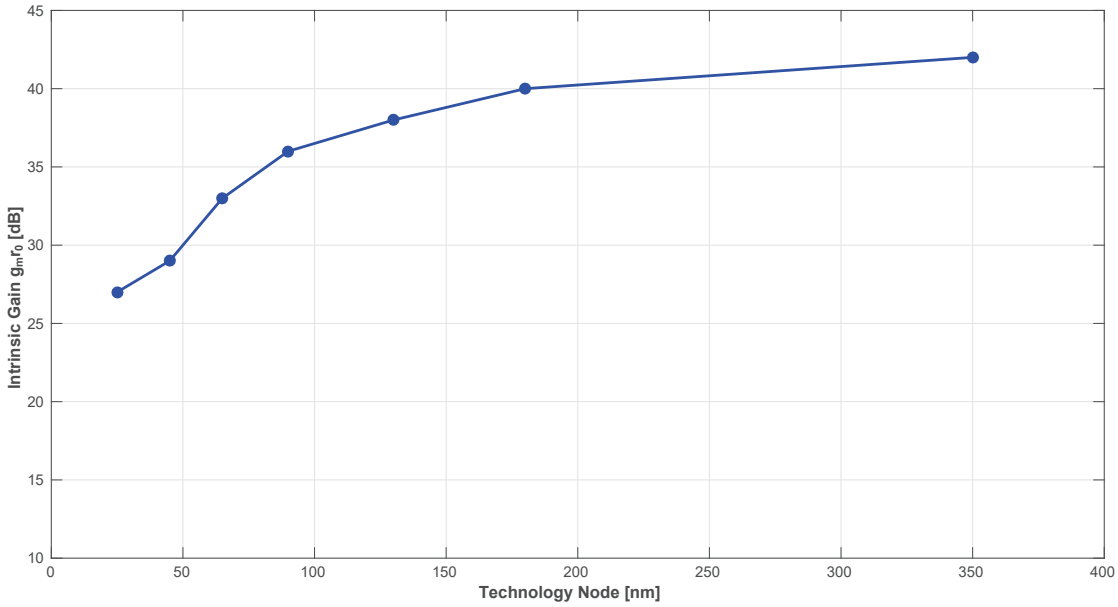


Figure 1.6: Transistor intrinsic gain versus CMOS minimum channel length

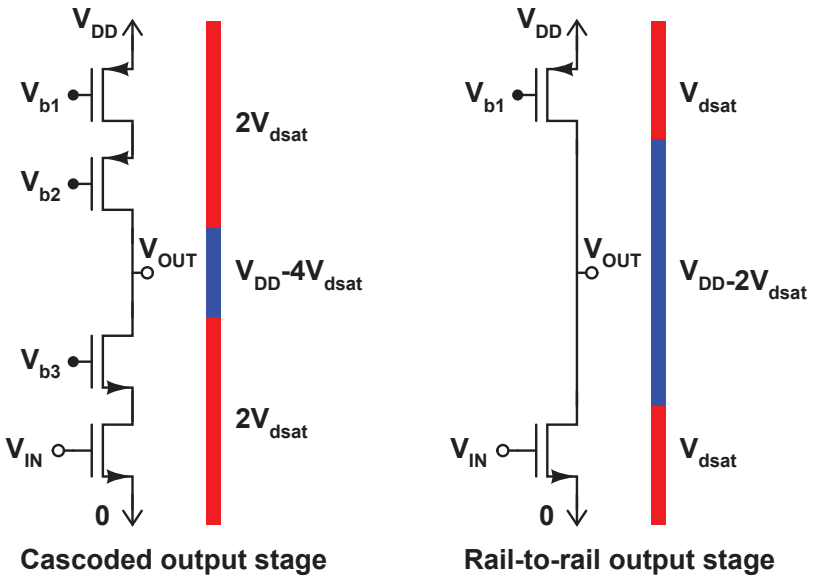


Figure 1.7: Output signal swings in different output stages

input signals, the input may not be properly encoded by the ΣΔ modulator. That is, there is a range of input for which the modulator may produce the same average output value. This range is known as a dead zone. This effect is strongly related to limit cycles in that the output is an endlessly repeating bitstream. As it will become more clear in the following Chapters, a low DC-gain of the amplifier leads therefore to a significant issue in ΣΔ modulator designs.

Solution as transistor cascoding can be applied in order to increase the gain.

However, insufficient voltage headroom makes stacking of transistors no longer efficient. In Figure 1.7 two output stages and corresponding signal swings are shown: a cascoded output stage on the left and a rail-to-rail output stage on the right. For proper operation the transistors have to be in saturation, which requires the drain-source voltage to be at least equal to the saturation voltage V_{dsat}, which depends on the current level and technology line width. In typical opamp designs the values are some hundreds of millivolts. In practice, in addition to the V_{dsat}, some extra voltage margin has to be reserved to achieve robustness against inaccurate biasing and to get a decent output impedance. The reduction in signal swing in the cascode stage is twice that in the rail-to-rail stage. It is obvious that as the supply voltage gets lower the margin eats an increasing portion of signal range. Therefore, at lower power supply voltages, a multistage amplifier is preferable to achieve high DC-gain. In fact, the multistage amplifier ensures a rail-to-rail output. However, these amplifiers require large compensation capacitor for stability, consume more current, require multifeedback loop for controlling common-mode voltage of the intermediate node and are noisier than a single stage cascode amplifier.
A possible solution to increase the gain is to force the MOS to operate in the sub-threshold region ($V_{GS} < V_{TH}$). In fact, as indicated in Equation (1.3), decreasing the overdrive voltage brings to a greater transconductance. In this region the MOS presents some useful advantages, such as, minimum overdrive, small gate capacitance and large gain. On the contrary, the device has low speed. Moreover, it is worth to notice that the mismatch of a transistor with a normal distribution with mean μ and standard deviation σ, defined as

$$\sigma_{V_{TH}} = \frac{A_{V_{TH}}}{\sqrt{WL}} \tag{1.5}$$

where $A_{V_{TH}}$ is a technology constant, is greater in a sub-threshold biased transistor, since the term $A_{V_{TH}}$ is three times higher than the value in saturation [11], leading to a mismatch and consequently input offset, which requires a compensation scheme to be removed. Therefore having MOS in subthreshold region is usually not recommended. Furthermore, it is worth to notice that generally the models of the subthreshold region used in the software for transistor design are not well defined and generally their behavior in the real world is different from their behavior in simulations.

1.4 Conclusions and Thesis Outline

The considerations made so far indicate different problems in the design of ADC in scaled CMOS technologies. On the one hand nanometric technologies generally lead to reductions in power consumption, on the other make more difficult to design ADCs. Moreover the industries demand for wide-band applications has brought the designers to consider the multi-bit quantizer world. However $\Sigma\Delta$ modulators hide several challenges with the multi-bit quantizer approach.
This work is devoted to the design of wide-bandwidth and low power $\Sigma\Delta$ ADC in 65nm technology.
The outline of the presented work is as follows.

Chapter 2 gives a brief introduction of some important features of the $\Sigma\Delta$ ADC. The basics concepts of oversampling and noise shaping are introduced. The structure of discrete-time (DT) $\Sigma\Delta$ will be analyzed in detail.
Chapter 3 illustrates the system analysis of the proposed modulator. The topology used for this design is described, comparing it with the standard topology. Also a strategy in the choice of the main system parameters is presented. A *MATLAB/Simulink* model including the main non-linearities is described. An in-depth description of the characteristics of the DEM algorithms in the literature is presented, describing also an innovative algorithm that unifies efficiency with simple hardware implementation.
Chapter 4 moves further down from the system-level description given in previous chapters to the circuit and physical level. The circuital implementation takes into account the considerations at system level, as in a standard top-down design strategy. Some innovative design solutions are also presented in this Chapter. In this Chapter also the *Cadence Spectre* simulations are presented. All the blocks of the modulator are simulated with the foundry models. The *Simulink* model is validated, in this Chapter, by the circuital simulations.
Chapter 5 presents some solutions in the measurement setup for a high resolution ADC. Two different possibilities in order to generate high resolution sine wave to test the modulator are described.
Chapter 6 summarizes some conclusions.

Chapter 2

Sigma-Delta Overview

2.1 Introduction

The ADC is a fundamental building block in modern electronic systems. As a bridge between the analog to digital world, the ADC functions as a translator from an analog quantity to a digital code. There are many types of ADCs and each of them has its own advantages and shortages. Among them the $\Sigma\Delta$ ADC features high resolution without requirement of high-precision devices, making it a popular choice of high resolution ADCs in cheap CMOS technologies.
This Chapter presents the principle of the ADC firstly. Then the $\Sigma\Delta$ ADC is introduced and it is explained how oversampling and noise shaping are used in ADCs to improve the resolution of the ADC. Starting with the principle of oversampling technique, the concept of noise shaping is introduced, as a more powerful mean of moving the quantization noise power out of the signal band. Then the suppression of the quantization noise with the digital filtering is explained.
The second part of this Chapter analyzes the main non-ideal mechanisms affecting the performance of $\Sigma\Delta$ modulators. Although it is commonly accepted that $\Sigma\Delta$ ADCs are less sensitive to non-idealities in the analog circuitry than other conversion techniques, their impact will be larger the more demanding the ADC specifications. Therefore, the influence of these errors on the modulator performance must be carefully considered during early design phases. The effect of the non-idealities are explained in this Chapter. System-level considerations, behavioral models, and closed-form expressions are obtained for the influence of each non-ideality. From them, estimable guidelines for the design of $\Sigma\Delta$ modulators can be extracted. Some details about the differences between Discrete-Time (DT) $\Sigma\Delta$ and Continuous-Time (CT) $\Sigma\Delta$ are explained. Also some circuital levels considerations are given.

2.2 Fundamental of Sigma Delta Modulation

In order to properly interface the analog world (composed of continuous-time, continuous-amplitude signals) with the digital world (composed of discrete-time, discrete-amplitude signals), ADCs require some additional signal processing building blocks. Figure 2.1 illustrates the general block diagram of an ADC intended for the conversion of low-pass (LP) signals. First, the bandwidth of the input signal

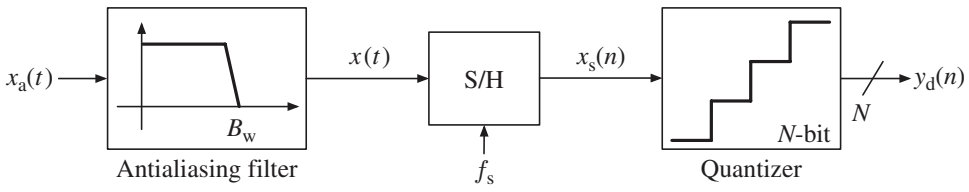


Figure 2.1: General block diagram of an A/D converter. A Nyquist-rate ADC is assumed.

$x_a(t)$ must be limited to half of the sampling rate (Nyquist theorem). Otherwise, undesired higher frequency components will alias into the band of interest, and combine with the desired signal. Therefore a properly named anti-alias filter (AAF) must precede any sampling operation. Also the input signal $x(t)$ must be blocked for sufficient time, so that its amplitude can be determined. For that reason, the ADC is also often preceded by a sample-and-hold (S/H) block.
Finally, the values of $x_s(n)$ are quantized using N bits, so that each continuous-valued input sample is mapped into the closer discrete-valued level out of the 2^N that cover the input range, yielding the converter digital output $y_d(n)$.

2.2.1 Oversampling

The sampling process performs the continuous-to-discrete transformation of the input signal in time. According to the Nyquist theorem, to prevent information loss, $x(t)$ must be sampled at a minimum rate of $f_N = 2B_w$, often referred to as the Nyquist frequency. On the basis of this criterion, the ADCs, in which the analog input signal is sampled at the minimum rate $f_s = f_N$, are called Nyquist-rate ADCs. Conversely, $\Sigma\Delta$ modulators are called oversampling ADCs, in which $f_s > f_N$. How much faster than required the input signal is sampled is expressed in terms of OSR, defined as

$$\text{OSR} = \frac{f_s}{2B_w}. \tag{2.1}$$

Whether oversampling is used or not in an ADC has a noticeable influence on the requirements of its AAF. In fact in Nyquist-rate ADCs, where the input signal bandwidth B_w coincides with $f_s/2$, aliasing will occur if there are frequency components above $f_s/2$. Therefore high-order analog AAFs are thus required to implement sharp transition bands capable of removing out-of-band components with no significant attenuation of the signal band, as shown in Figure 2.2(a).
Conversely, in oversampling ADCs, the replicas of the input signal spectrum are farther apart than in Nyquist-rate ADCs. As illustrated in Figure 2.2(b) the order required for the AAF is greatly relaxed since f_s is much greater than the signal bandwidth.
Furthermore the strategy of oversampling reduces also the quantization noise. In fact, while performing the continuous-to-discrete transformation of the input signal, inevitably a quantization error is introduced [12-14]. Figure 2.3(a) depicts the I/O characteristic of a quantizer. Continuous input amplitudes are discretized into

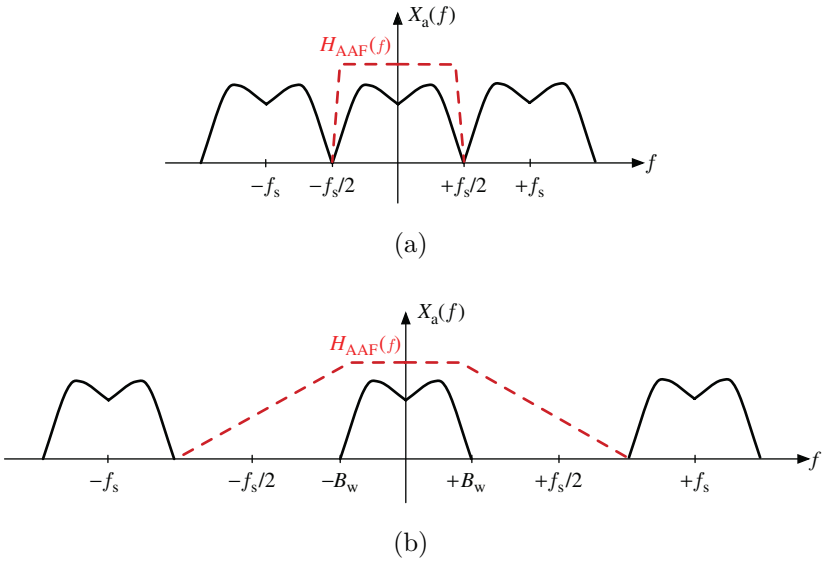


Figure 2.2: Antialiasing filter for (a) Nyquist-rate ADCs and (b) oversampling ADCs.

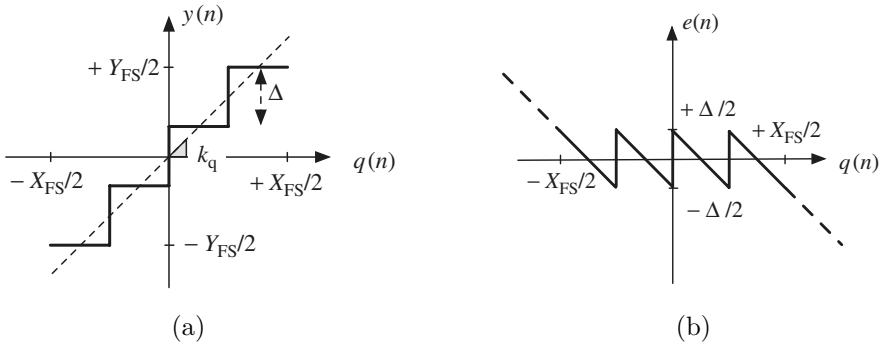


Figure 2.3: Illustration of the quantization process for a multi-bit quantizer. In (a) the I/O characteristic of the quantizer is depicted, while in (b) the multi-bit quantization error is shown.

discrete output values. Assuming an uniform quantizer, as the one in Figure 2.3(a), the separation between adjacent output levels is defined as the quantization step:

$$\Delta = \frac{Y_{FS}}{2^N - 1} \tag{2.2}$$

where Y_{FS} stands for the full-scale output range. Also in Figure 2.3(a) the gain of the quantizer k_q is shown. This gain can be defined as the ratio between the mean square value of the quantizer output and that of its input. As shown in Figure 2.3(b), the quantizer operation generates a rounding error that is a non-linear function of the input, namely the quantization error. Assuming that the output error $e(n)$ is completely unconrrelated with the quantizer input $q(n)$, we can see the quantization error as a random process with a uniform probability distribution in the range $[-\Delta/2, +\Delta/2]$. Note that this assumption is not strictly valid, but it is commonly accepted in the ADC design [15]. However, the larger the number

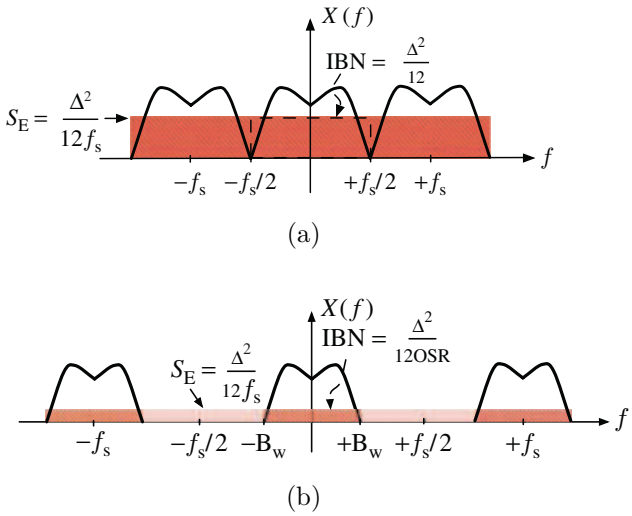


Figure 2.4: Quantization noise for (a) Nyquist-rate ADCs and (b) oversampling ADCs.

bits in the quantizer, the better is the approximation. This assumption is known as the additive white noise approximation of the quantization error, allowing to linearize the non-linear quantizer with the equation $y(n) = k_q q(n) + e(n)$. The power associated to the quantization error can be computed as

$$\bar{e}^2 = \sigma_e^2 = \int_{-\infty}^{+\infty} e^2 \mathrm{PDF}(e)\mathrm{d}e = \int_{-\Delta/2}^{+\Delta/2} e^2 \mathrm{d}e = \frac{\Delta^2}{12} \tag{2.3}$$

where PDF is the probability density function which, for the assumption of uniform white noise made before, is equal to one. Therefore the power spectral density (PSD) of the quantization error in the range $[-\Delta/2, +\Delta/2]$ is

$$S_E = \frac{\bar{e}^2}{f_s} = \frac{\Delta^2}{12 f_s}. \tag{2.4}$$

For a full-scale sine wave ($X_{FS}/2 = Y_{FS}/2$) the maximum Signal-to-Quantization Noise ratio (SQNR) is given by

$$\mathrm{SQNR} = \frac{P_{sig}}{P_{qnoise}} = \frac{(Y_{FS}/2)^2/2}{\Delta^2/12} \approx \frac{(Y_{FS}/2)^2/2}{(Y_{FS}/2^N)^2/12} = \frac{3}{2}2^{2N} \tag{2.5}$$

where P_{sig} is the signal power and P_{qnoise} is the power of the quantization noise. Expressed in dB, this becomes Equation (2.6), which is widely used to assess the performance of data converters

$$\mathrm{SQNR}\ [\mathrm{dB}] = 6.02N + 1.76. \tag{2.6}$$

For a Nyquist ADC all the quantization noise power falls inside the signal band and passes to the ADC output as a part of the input signal itself, as illustrated in Figure 2.4(a). Conversely, if an oversampled signal is quantized, because $f_s > 2B_w$, only a fraction of the total quantization noise power lies within the signal band, as illustrated in Figure 2.4(b). We define the in-band noise power (IBN) as the noise inside the signal bandwidth. Since the ADC is oversampled the IBN is given by

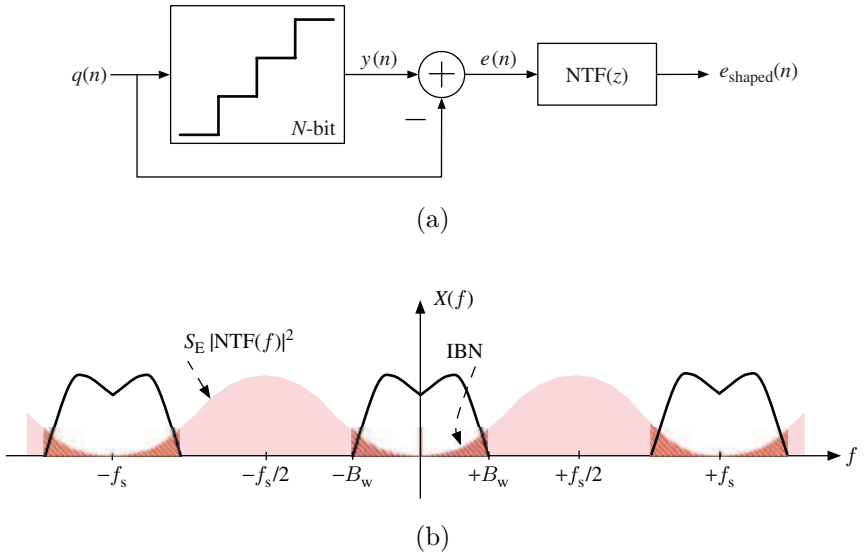


Figure 2.5: Quantization noise shaping: (a) conceptual block diagram and (b) effect on the in-band noise of an oversampling noise-shaping ADC.

$$\text{IBN} = \int_{-B_w}^{+B_w} S_E(f)\mathrm{d}f = \int_{-B_w}^{+B_w} \frac{\Delta^2}{12 f_s}\mathrm{d}f = \frac{\Delta^2}{12 \cdot \text{OSR}} \tag{2.7}$$

where Equation (2.1) and Equation (2.4) are used in the last step. As apparent from Equation (2.7) the larger is the OSR, the smaller is the IBN. We can evaluate the SQNR also in the case of oversampled converters. Using the same principle of Equation (2.5) the SQNR of an ideal oversampled ADC is obtained in dB as

$$\text{SQNR [dB]} = 6.02N + 1.76 + 10\log(\text{OSR}). \tag{2.8}$$

2.2.2 Noise Shaping

As previously stated, the oversampling can be used to trade speed for resolution. However speed is a limited resource and at a rate of 3dB/octave, as can be easily derived from Equation (2.8), plain oversampling provides only moderates improvements. It will be shown below that there are better ways to use oversampling. In Figure 2.4 the quantization noise had a flat power spectral density. A more efficient way to use oversampling is to shape the spectral density such that most of the quantization noise power is outside the desired signal band.
This is illustrated in Figure 2.5(a), where the quantization noise is conceptually obtained by subtracting the quantizer input signal $q(n)$ from its output $y(n)$ and then passes through a filter transfer function, usually called the Noise Transfer Function (NTF).
For quantizers working on LP signals, the NTF is of high-pass type and can be easily obtained from a differentiator filter, with a Z-domain transfer function given by

$$\text{NTF}(z) = (1 - z^{-1})^L \tag{2.9}$$

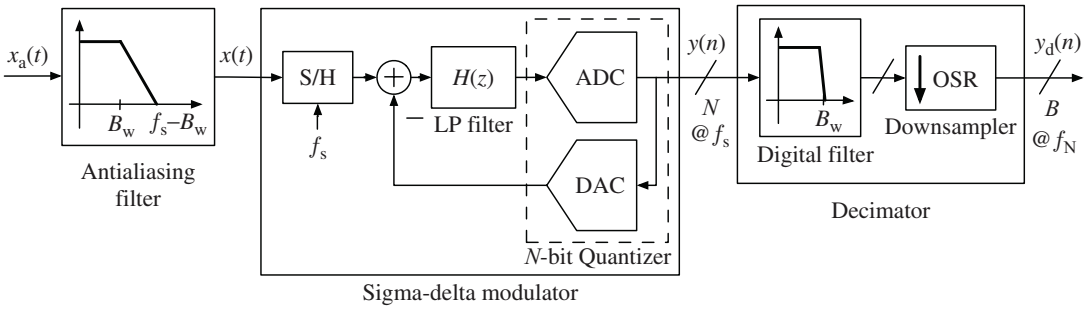


Figure 2.6: Main blocks of a DT ΣΔ modulator.

where L stands for the filter order. To calculate the SQNR it is first necessary to find the squared magnitudes of this transfer function, obtained for $z = e^{j\omega} = e^{j2\pi f/f_s}$. Therefore, Equation (2.9) can be approximated for low frequencies as

$$|\mathrm{NTF}(z)|^L = |1 - e^{-j2\pi f/f_s}|^L = \left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^L \approx \left(\frac{2\pi f}{f_s}\right)^L \tag{2.10}$$

so that the power due to shaped quantization noise that lies within the signal band (Figure 2.5(b)) yields

$$\mathrm{IBN} = \int_{-B_w}^{+B_w} S_E(f)|\mathrm{NTF}(f)|^2 \mathrm{d}f \approx \frac{\Delta^2}{12}\frac{\pi^{2L}}{(2L+1)\mathrm{OSR}^{(2L+1)}}. \tag{2.11}$$

Repeating the operations made in Equation (2.5), by simply substituting the power of the quantization noise with the IBN evaluated in Equation (2.11) a new SQNR is obtained

$$\mathrm{SQNR\ [dB]} = 6.02N + 1.76 + 10\log\left(\frac{2L+1}{\pi^{2L}}\right) + (2L+1)10\log(\mathrm{OSR}). \tag{2.12}$$

This expression shows two important results: for a first-order modulator, namely $L = 1$, SQNR improves with OSR at a rate of 9dB/octave. As expected, by shaping the quantization error, a higher effective resolution can be obtained. However it is worth to notice that the total noise power at the output (for full bandwidth) is higher than that of a Nyquist rate converter. Thus for very small oversampling ratio the performance becomes worse than for unshaped oversampled converters [15]. Thus there is a lower limit in the OSR, below which ΣΔ converters do not provide any benefits.

2.2.3 Topology of ΣΔ ADCs

Figure 2.6 illustrates the basic block diagram of a ΣΔ ADC [16] intended for the conversion of LP signals, which consists of the following:

- **Antialiasing filter**, which band limits the analog input signal to avoid aliasing during its subsequent sampling. As already discussed the principle of oversampling relaxes the requirements of AAF.

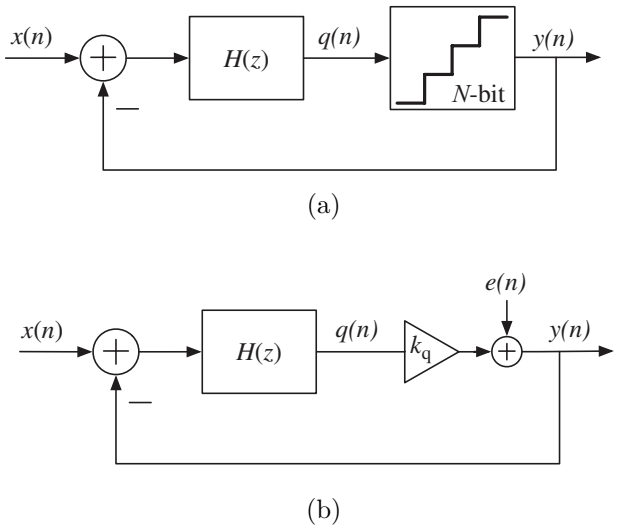


Figure 2.7: ΣΔ modulator: (a) block diagram and (b) ideal linearized model.

- **Sigma Delta modulator**, in which the oversampling and quantization of the band-limited analog signal take place. The quantization noise of the embedded N-bit quantizer is shaped in the frequency domain by placing an appropriate loop filter $H(z)$ before it and closing a negative feedback loop around them. In this Chapter the 1-bit quantizer case is considered.
- **Decimation filter**, in which a high-selectivity digital filter sharply removes the out-of-band spectral content of ΣΔ modulator output and thus most of the shaped quantization noise. The decimator also reduces the data from f_s down to the Nyquist frequency, while increasing the word length from N to B bits to preserve resolution.

Using the linearized model for the quantizer and assuming and ideal D/A converter, the linearized model of the modulator depicted in Figure 2.7(a) is shown in Figure 2.7(b).
The linear model contains two inputs: the input signal $x(n)$ and the quantization error $e(n)$. The output can be represented in the Z-domain as

$$Y(z) = H_x(z)X(z) + H_e(z)E(z) \tag{2.13}$$

where $X(z)$ and $E(z)$ are respectively the Z-transform of the input and of the quantization error. The signal and noise transfer functions can be respectively calculated as

$$H_x(z) = \frac{H(z)k_q}{1 + H(z)k_q} \tag{2.14}$$

$$H_e(z) = \frac{1}{1 + H(z)k_q}. \tag{2.15}$$

Equations (2.14) and (2.15) are respectively called Signal Transfer Function (STF) and the already defined NTF.

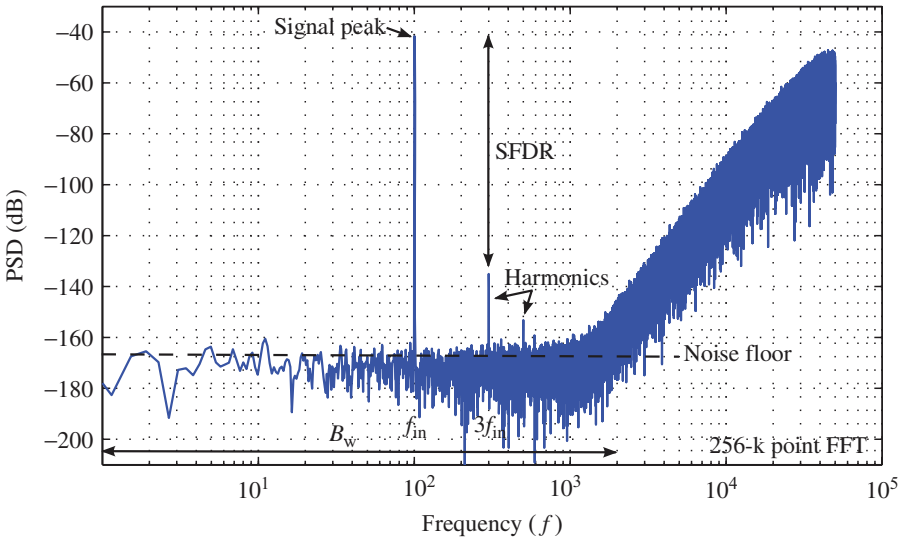


Figure 2.8: Illustration of a typical output spectrum of a ΣΔ modulator and its main characteristics.

From these relations, the operation of the ΣΔ converter becomes obvious. The loop-filter is designed to have a large gain inside the signal band and a small gain outside the band. Note that, if the loop filter is designed such that $|H(f)| \gg 1$ within the signal band then $|STF(f)| \approx 1$ and $|NTF(f)| \ll 1$; that is, the quantization noise is ideally canceled while the input signal is perfectly transferred to the output.
As an example, a first-order low-pass ΣΔ converter is considered where the loop-filter $H(z)$ consists of an integrator,

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.16}$$

that, in combination with an embedded quantizer with $k_q = 1$, leads to a ΣΔ modulator whose output is given by

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z). \tag{2.17}$$

2.2.4 Definition of Performance Metrics for a ΣΔ ADC

Contrary to Nyquist-rate ADCs, whose performance is mainly characterized by static performance metrics, that is, monotonicity, gain and offset errors, differential non-linearity (DNL) and integral non-linearity (INL), ΣΔ ADCs characteristics are typically measured using dynamic performance metrics, which are obtained from the frequency-domain representation of the output sequence.
Figure 2.8 illustrates an exemplary spectrum of a ΣΔ modulator output when a sinusoidal signal with frequency f_{in} is applied. This figure shows the Spurious-Free-Dynamic Range (SFDR) that is the ratio of the signal power to the strongest spectral tone.
Noise power metrics are derived from the ΣΔ output spectra by integration over the signal bandwidth B_w. Some other important specifications are discussed here.

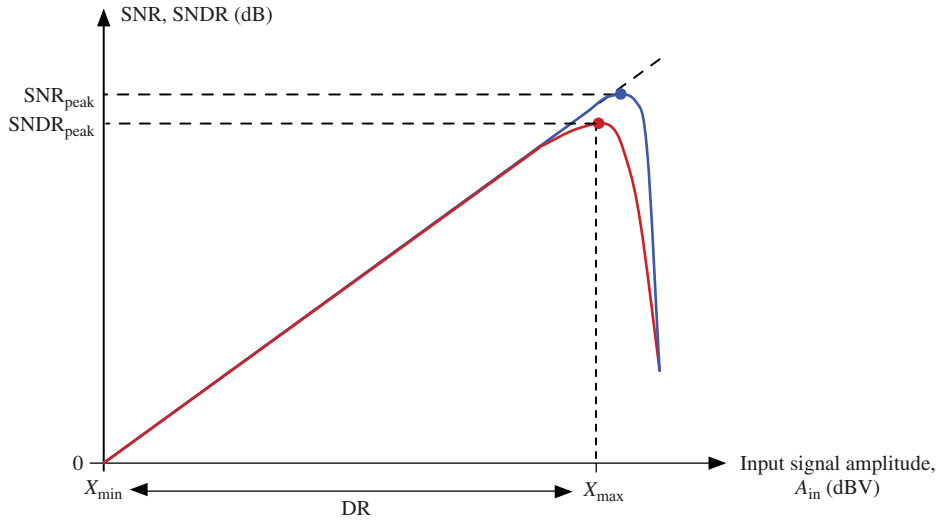


Figure 2.9: Illustration of the performance metrics of a ΣΔ modulator on a typical SNR-SNDR curve.

- Signal to Noise Ratio (SNR), which is the ratio of the input signal power to the noise power measured at the output of the converter. Unlike the already defined SQNR the noise here should include not only the quantization noise but also all the circuit noise.
- Signal to Noise and Distortion Ratio (SNDR), which is the ratio of the input signal power to the power of distortion components and noise measured at the output of the converter. As illustrated in Figure 2.9, accounting for the harmonics at the modulator output, makes a typical SNDR curve to deviate from the SNR curve only for large input amplitudes. In fact for large input the distortion becomes noticeable.
- Dynamic Range (DR), which is defined as the difference between the input amplitude that corresponds to the SNDR$_{\text{peak}}$, namely X_{max}, and the amplitude for which SNDR = 0dB, namely X_{min}.
- Effective Number of Bits (ENOB), which is the number of bits of the modulator and it strictly connected to the DR by the Equation (2.18)

$$\text{ENOB [bit]} = \frac{\text{DR [dB]} - 1.76}{6.02}. \tag{2.18}$$

2.2.5 Higher Order ΣΔ ADC

The output of an ideal LP Lth-order ΣΔ modulator in the Z-domain can be considered to be

$$Y(z) = z^{-L}X(z) + (1 - z^{-1})^{L}E(z). \tag{2.19}$$

As apparent from Equation (2.12) increasing the order L of the modulator improves the increment of SQNR when the OSR is doubled. In fact, with $L = 1$ the SQNR

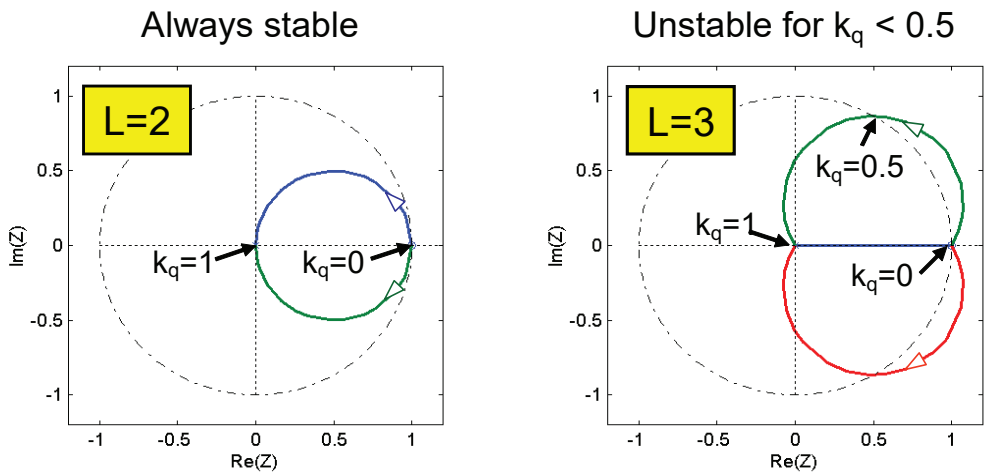


Figure 2.10: Root locus in Z-plane for a second-order modulator and a third-order modulator.

improves with OSR at a rate of 9dB/octave, with $L = 2$ at a rate of 15dB/octave and with $L = 3$ at a rate of 21dB/octave. In general the SQNR will improve with the OSR at a rate of $(6L + 3)$dB/octave.
However, increasing the order of the modulator presents some side-effects. These issues are related to the quantizer gain, previously defined as k_q. For first and second-order modulator loops, variations in the gain of the quantizer do not cause problems, other than a temporary reduction of performance. However, for higher-order modulators, there are forbidden values of k_q. If reached, they will cause the modulator to become unstable.
The Figure 2.10 shows the z-plane root-locus representation of the NTF's poles and zeros.
For both the second-order and third-order noise transfer functions, the zeros are located at DC, namely $z = 1$. For normal operation the gain of the quantizer is equal to 1, $k_q = 1$, in which case both NTFs have their poles at $z = 0$. As the quantizer gain k_q changes between 1 and 0, the poles of the second-order NTF remain always inside the unit circle, satisfying the condition for stability. However, for the third-order NTF, the poles fall outside the circle for part of the root locus, causing the instability of the overall modulator.

2.2.6 Digital Filter

In order to remove the quantization noise outside the bandwidth a Digital Filtering action is needed. The decimation filter takes the 1 bit modulator output as its input and filters the out-of-band quantization noise and decreases the sampling frequency to a value closer to twice the highest frequency of interest. The most common used decimator for $\Sigma\Delta$ modulators is based on a sinc filter, which can be efficiently realized as a Cascaded Integrator and Comb (CIC) filter [17]. The transfer function of the CIC filter is

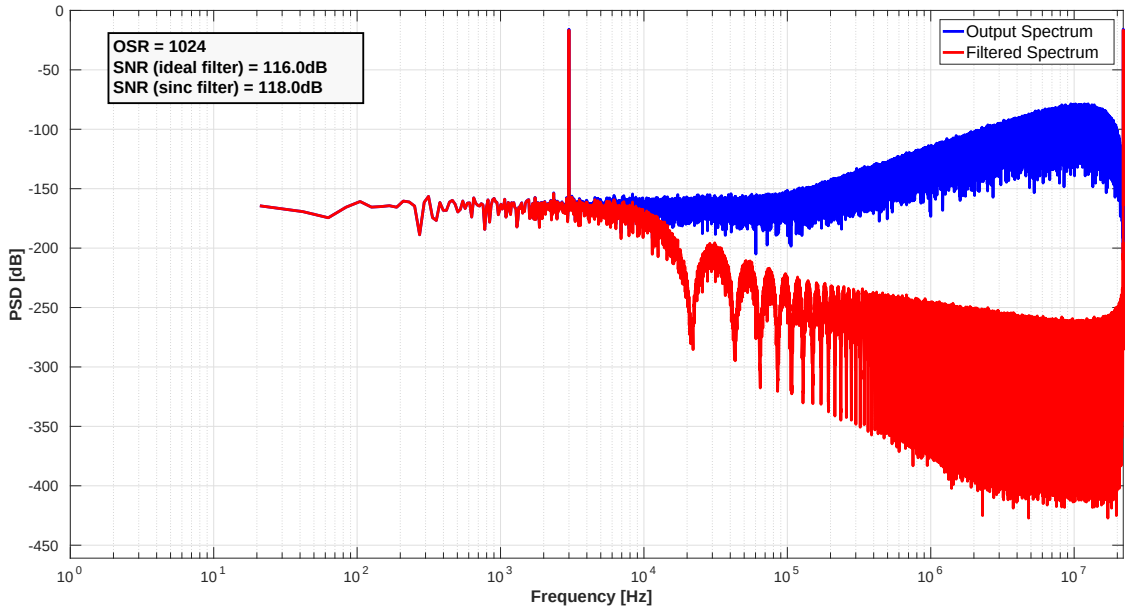


Figure 2.11: Output spectrum of the quantizer and its filtered version after the decimation filter.

$$H_{\mathrm{CIC}}(z) = \left(\frac{1}{\mathrm{OSR}} \cdot \frac{1 - z^{-\mathrm{OSR}}}{1 - z^{-1}}\right)^{M} = \left(\frac{1}{OSR} \sum_{x=0}^{\mathrm{OSR}-1} z^{-x}\right)^{M} \tag{2.20}$$

where M is the sinc filter order. For ΣΔ converters it is generally recommended to choose the order of the sinc filter M equal to the modulator order L plus one [18-19]. One possible drawback of the CIC filter is the in-band attenuation, which usually requires proper compensation in some applications. The effect of a CIC filter on the output spectrum of the ΣΔ is depicted in Figure 2.11. The effectiveness of the CIC filter in removing the shaped quantization noise is apparent. Furthermore the CIC filter is attenuating some noise at the edge of the conversion bandwidth, which in this case does not give a disadvantage, since the frequency input signal is significantly lower than the Bandwidth, but indeed gives a 2dB gain in terms of SNR with respect to an ideal step filter.

2.3 Non-idealities in Discrete Time ΣΔ Modulators

Figure 2.12 shows the circuital implementation of a first-order DT ΣΔ modulator with a single bit quantizer.
The integrator is realized with a classical switched-capacitor (SC) integrator, implementing the the transfer function of Equation (2.16). The single bit quantizer is realized with a simple comparator, which gives as output V_{ref-} or V_{ref+}, namely 0 or V_{DD}. There are a number of circuit non-idealities and non-linearities that degrade the performance of the analog modulator blocks. The way in which these

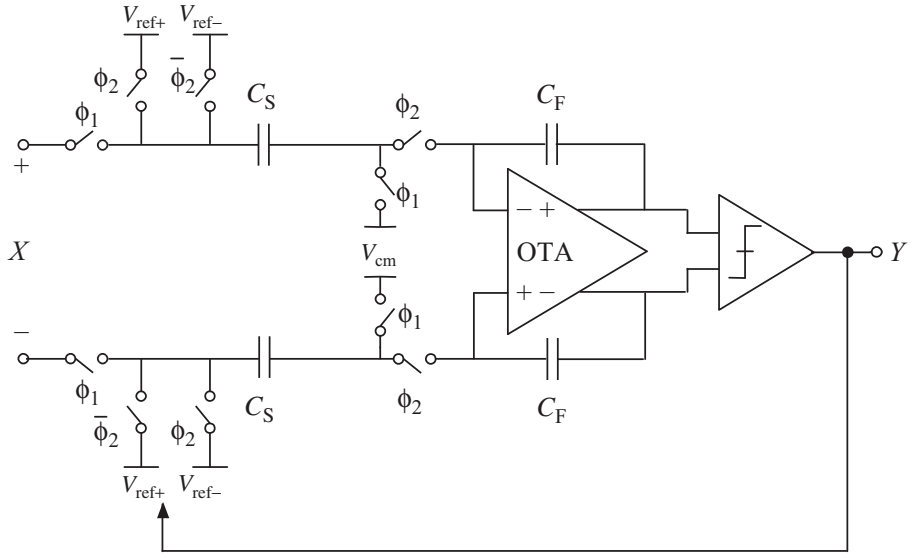


Figure 2.12: Fully-differential implementation of a first-order DT ΣΔ modulator.

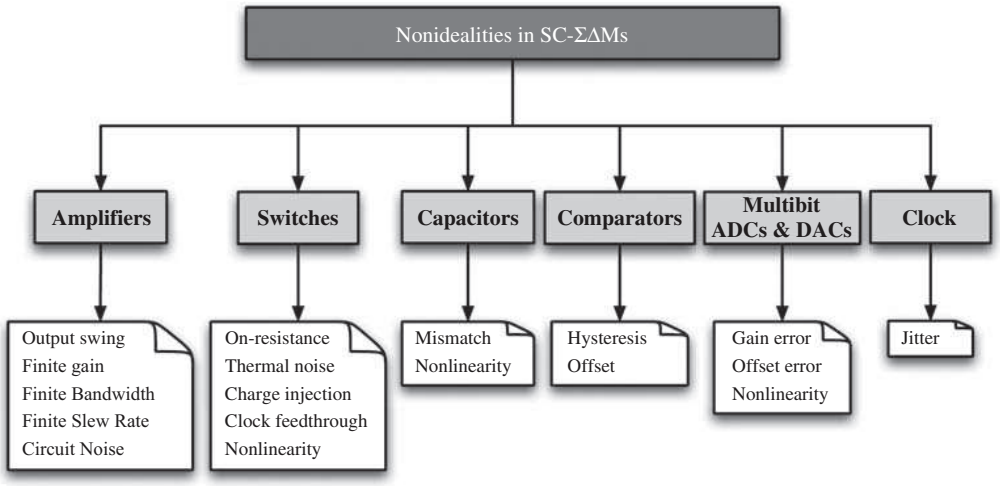


Figure 2.13: Main non-idealities affecting the performance of SC ΣΔ modulators.

non-idealities affect the performance of ΣΔ modulators depends on many different factors.
In the case of SC implementation, the main non-ideal effects can be grouped as illustrated in Figure 2.13.
The influence of non-idealities on the performance of the ΣΔ modulators strongly depends on the location of the corresponding noise source in the modulator [20-21]. According to these criteria, the above errors can be classified into two main families:

- **Errors that modify the modulator NTF** such as the finite amplifier gain and gain-bandwidth product and capacitor mismatch.
- **Errors that can be modeled as additive noise at the modulator input** and, hence, are not in-band attenuated by the noise shaping. Among

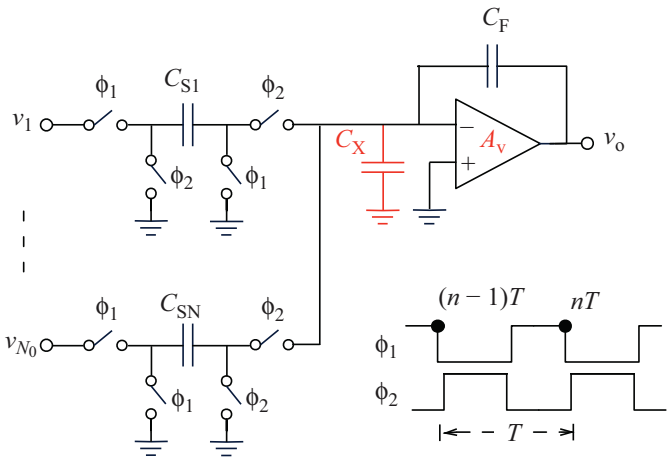


Figure 2.14: SC integrator with N input paths and finite amplifier gain A_V

other, some errors belonging to this family are clock jitter, circuit noise, and distortion caused by circuit non-linearities

The issues generated by the non-idealities of Figure 2.13 are described below. However, some non-idealities such as the effects of the mismatch between the capacitors, the non-linearity of the switches and the multi-bit ADC errors will be explained in Chapter 3 and in Chapter 4.

2.3.1 Effect of Finite Amplifier DC-gain

As already stated, the ideal transfer function of the integrator is given by

$$H_{ITF}(z) = \frac{z^{-1}}{1 - z^{-1}}. \tag{2.21}$$

If the finite amplifier gain A_v and the parasitic capacitor C_x at the amplifier summing node is accounted for in the charge transfer of an SC integrator, as shown in Figure 2.14, its difference equation can be written as [21]:

$$\begin{aligned} v_o(nT) = & \frac{1 + \left(1 + \frac{C_x}{C_F}\right)\frac{1}{A_V}}{1 + \left(1 + \frac{C_x}{C_F} + \sum_{i=1}^{N}\frac{C_{Si}}{C_F}\right)\frac{1}{A_V}} v_o[(n-1)T] + \\ & + \frac{\sum_{i=1}^{N}\frac{C_{Si}}{C_F} v_i[(n-1)T]}{1 + \left(1 + \frac{C_x}{C_F} + \sum_{i=1}^{N}\frac{C_{Si}}{C_F}\right)\frac{1}{A_V}}. \end{aligned} \tag{2.22}$$

Transforming Equation (2.22) to the Z-domain it is possible to obtain the filter transfer function including the limited gain effect ($H_{LG}(z)$)

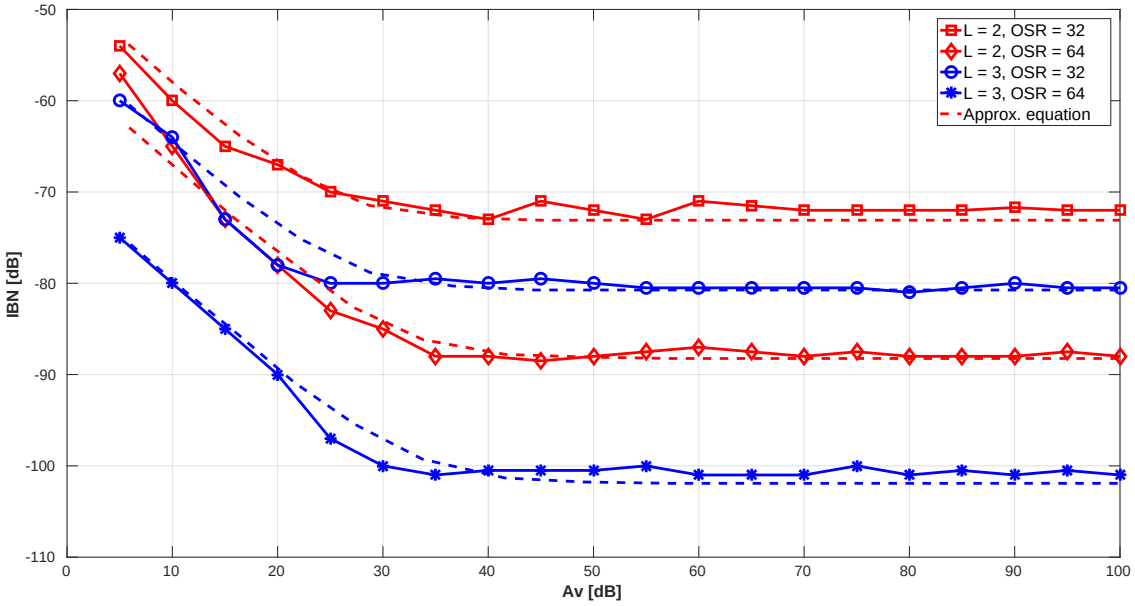


Figure 2.15: Simulation results for the influence of limited DC-gain amplifier on the in-band noise of SC ΣΔ modulators.

$$H_{LG}(z) = \frac{1}{1+\left(1+\frac{C_x}{C_F}+\sum_{i=1}^{N}\frac{C_{Si}}{C_F}\right)\frac{1}{A_V}} \cdot \frac{z^{-1}}{1-z^{-1}\left[\frac{1+\left(1+\frac{C_x}{C_F}\right)\frac{1}{A_V}}{1+\left(1+\frac{C_x}{C_F}+\sum_{i=1}^{N}\frac{C_{Si}}{C_F}\right)\frac{1}{A_V}}\right]}. \tag{2.23}$$

Therefore, if compared with the ideal case $H_{ITF}(z)$, amplifier finite gain introduces a gain error in the transfer function ad a shift of its pole from its ideal position ad DC ($z = 1$). Neglecting the gain error, which is actually negligible in a ΣΔ modulator thanks to the feedback loop, Equation (2.23) can be re-written as

$$H_{LG}(z) \approx \frac{z^{-1}}{1-z^{-1}\left(1-\frac{1}{A_V}\sum_{i=1}^{N}\frac{C_{Si}}{C_F}\right)}. \tag{2.24}$$

The result is known as lossy integration since only a part of the integrator output in the previous period is added to the new input [21]. Including the transfer function of Equation (2.24) yields:

$$\mathrm{STF}(z,\mu) = \frac{1}{1+\mu} \approx 1-\mu \tag{2.25}$$

$$\mathrm{NTF}(z,\mu) = \frac{1-z^{-1}+\mu z^{-1}}{1+\mu} = (1-\mu)(1-z^{-1})+\mu z^{-1} \tag{2.26}$$

with $\mu = \frac{1}{A_V}\sum_{i=1}^{N}\frac{C_{Si}}{C_F}$. So, on the one hand, a small error in the modulator gain is produced and, additionally, a change in the quantization noise shaping function

due to a displacement of the zero from its nominal position in DC. Note that, if $\mu = 0$, namely $A_V \to \infty$, Equations (2.25) and (2.26) are reduced to the ideal case. The increase in the quantization noise power can be calculated as

$$\text{IBN} = \frac{\Delta^2}{12}\left(\frac{\mu^2}{\text{OSR}} + \frac{\pi^2}{3\text{OSR}^3}\right). \tag{2.27}$$

Equation (2.27) has a term proportional to the squared leakage factor μ, and inversely proportional to OSR, which, for high oversampling ratio or small amplifier DC-gain, can dominate the total noise power. A generic expression can be obtained for the in-band quantization noise power, valid for an arbitrary-order single-loop modulator.

$$\text{IBN}_{LG} = \frac{\Delta^2}{12}\left[\frac{\mu^2\pi^{2L-2}L}{(2L-1)\text{OSR}^{2L-1}} + \frac{\pi^{2L}}{(2L+1)\text{OSR}^{2L+1}}\right]. \tag{2.28}$$

The number of extra error terms, namely those that depend on μ, grows with the modulator order. Nevertheless, for usual values of the oversampling ratio and amplifiers DC-gain, the dominant error for a Lth-order modulator is inversely proportional to OSR^{2L-1}. Note that the DC gain of the amplifiers should be in the range of the oversampling ratio ($\mu \propto 1/A_v = 1/\text{OSR}$) in order to keep the terms of Equation (2.28) proportional to the $(2L+1)$-th power of OSR and retain the ideal noise shaping. Figure 2.15 shows the effect of the finite DC gain of amplifiers on a ΣΔ modulator. The in-band noise is plotted also according with Equation (2.28). Note that the simulated results are in good accordance with the closed-form expression of Equation (2.28).

2.3.2 Integrator Settling Error

Speed limitations in SC integrators due to the limited dynamic response of amplifiers cause errors in the charge transfer [22]. The impact of the resulting error in the integrator output voltage settling error on the modulator performance will be higher, the higher the sampling frequency. This is one of the reason why increasing the sampling frequency in a ΣΔ modulator is not recommended. Let consider the circuit of Figure 2.16 with a SC integrator consisting in N input branches and another SC integrator acting as a load. The amplifier is modeled with the equivalent circuit of Figure 2.17.
The equivalent capacitive load at the amplifier output node is given by

$$\begin{aligned} C_{eq,\Phi_1} &= C_x + \left(C_L + \sum_{i=1}^{N} C_{Si}\right)\left(1 + \frac{C_x}{C_F}\right) \\ C_{eq,\Phi_2} &= C_x + \sum_{i=1}^{N} C_{Si} + C_L\frac{1}{\beta}, \end{aligned} \tag{2.29}$$

where β is the feedback factor and it is given by

$$\beta = \frac{C_F}{C_F + \sum_{i=1}^{N} C_{Si} + C_x}. \tag{2.30}$$

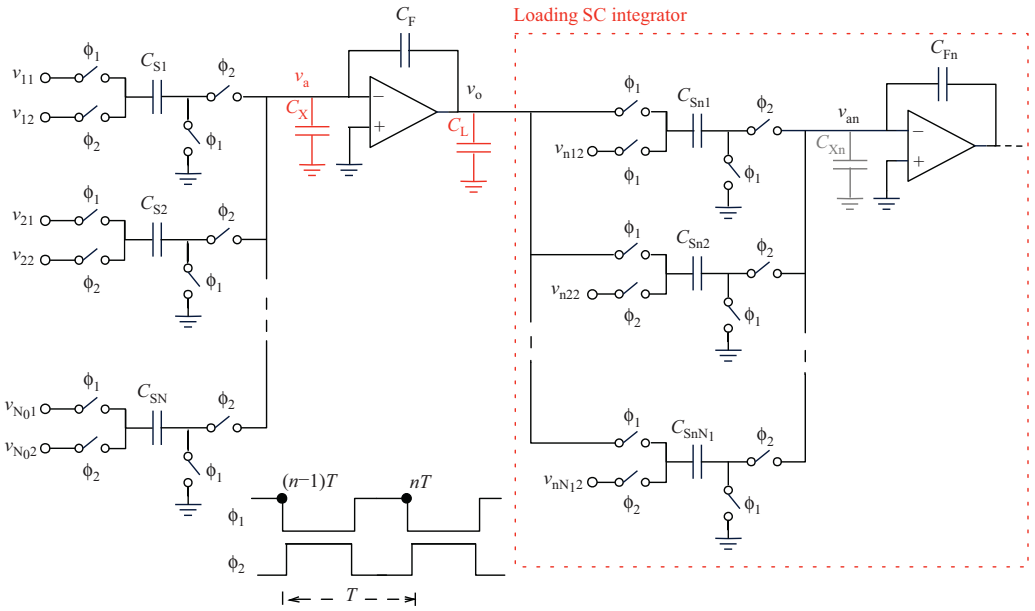


Figure 2.16: Multi-input path SC integrator followed by a loading multi-input path SC integrator.

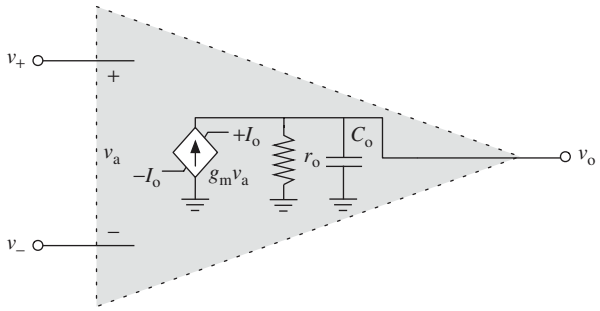


Figure 2.17: Amplifier single-pole model.

The settling mode is analyzed during a complete clock cycle, namely during the sampling (Φ_1) and integration phase (Φ_2), considering the different possibilities for the amplifier dynamic operation, linearly or in slew, and keeping track of the voltage at both the integrator output v_o and the amplifier summation node v_a. Therefore, the error in the integrator output voltage at the end of one sampling-integration process can be accurately obtained.

Let $v_a[(n-1/2)T]$ and $v_o[(n-1/2)T]$ be the respective amplifier input and output voltages at the end of an integration phase, which will serve as initial conditions to derive of the integrator evolution during a complete clock cycle. The voltage at the amplifier summation node at the end of the next sampling phase, at $t = nT$ can be

accurately obtained as

$$v_a(nT) = \begin{cases} v_{a0,\Phi_1} \mathrm{e}^{\frac{-g_m}{C_{eq,\Phi_1}}\frac{T}{2}}, & \text{if } |v_{a0,\Phi_1}| \leq \frac{I_0}{g_m} \\ \frac{I_0}{g_m}\mathrm{sgn}(v_{a0,\Phi_1})\mathrm{e}^{\frac{-g_m}{C_{eq,\Phi_1}}(\frac{T}{2}-t_{0,\Phi_1})}, & \text{if } |v_{a0,\Phi_1}| > \frac{I_0}{g_m}, t_{0,\Phi_1} \leq \frac{T}{2} \\ v_{a0,\Phi_1} - \frac{I_0}{C_{eq,\Phi_1}}\mathrm{sgn}(v_{a0,\Phi_1})\frac{T}{2}, & \text{if } |v_{a0,\Phi_1}| > \frac{I_0}{g_m}, t_{0,\Phi_1} > \frac{T}{2} \end{cases} \tag{2.31}$$

where I_0 is the maximum output current, to account for the limited Slew Rate (SR), t_{0,Φ_1} is the duration of the SR-limited integrator settling (relative to $T/2$) given by

$$t_{0,\Phi_1} = \frac{C_{eq,\Phi_1}}{g_m}\left(\frac{g_m|v_{a0,\Phi_1}|}{I_0} - 1\right), \tag{2.32}$$

where $\mathrm{sgn}(\cdot)$ is the sign function and v_{a0,Φ_1} represents the value of v_a at the beginning of the sampling phase, which can be computed as

$$v_{a0,\Phi_1} = v_a[(n-1/2)T] - \sum_{i=1}^{N}\frac{C_{Si}}{C_{eq,\Phi_1}}\{v_o[(n-1/2)T] - v_{C_{Si}}[(n-1/2)T]\} \tag{2.33}$$

where $v_{C_{Si}}$ is the voltage across capacitor C_{Si}.
The integrator output voltage at the end of sampling phase can be obtained as

$$v_o(nT) = v_o[(n-1/2)T] + \left(1 + \frac{C_x}{C_F}\right)\{v_a(nT) - v_a[(n-1/2)T]\} \tag{2.34}$$

as opposed to the ideal situation in which $v_0(nT) = v_o[(n-1/2)T]$.
Note from Equations (2.31) and (2.34) that, for the integrator model in Figure 2.16, the amplifier gain-bandwidth product (GBW) and output SR during sampling are obtained as:

$$\begin{aligned} \mathrm{GBW}_{\Phi_1}\ [\mathrm{rad/s}] &= \frac{g_m}{C_{eq,\Phi_1}}, \\ \mathrm{SR}_{\Phi_1}\ [\mathrm{V/s}] &= \frac{I_0}{\beta C_{eq,\Phi_1}}. \end{aligned} \tag{2.35}$$

During the integration phase, the incomplete settling model is evaluated proceeding in a similar way done for the sampling phase. Thus, at the end of the subsequent integration phase, that is at $t = (n+1/2)T$, the value of v_a is given by

$$v_a[(n+1/2)T] = \begin{cases} v_{a0,\Phi_2} \mathrm{e}^{\frac{-g_m}{C_{eq,\Phi_2}}\frac{T}{2}}, & \text{if } |v_{a0,\Phi_2}| \leq \frac{I_0}{g_m} \\ \frac{I_0}{g_m}\mathrm{sgn}(v_{a0,\Phi_2})\mathrm{e}^{\frac{-g_m}{C_{eq,\Phi_2}}(\frac{T}{2}-t_{0,\Phi_2})}, & \text{if } |v_{a0,\Phi_2}| > \frac{I_0}{g_m}, t_{0,\Phi_2} \leq \frac{T}{2} \\ v_{a0,\Phi_2} - \frac{I_0}{C_{eq,\Phi_2}}\mathrm{sgn}(v_{a0,\Phi_2})\frac{T}{2}, & \text{if } |v_{a0,\Phi_2}| > \frac{I_0}{g_m}, t_{0,\Phi_2} > \frac{T}{2} \end{cases} \tag{2.36}$$

where t_{0,Φ_2} is the duration of the SR-limited integrator settling (relative to $T/2$) given by

$$t_{0,\Phi_2} = \frac{C_{eq,\Phi_2}}{g_m}\left(\frac{g_m|v_{a0,\Phi_2}|}{I_0} - 1\right), \tag{2.37}$$

and v_{a0,Φ_2} represents the value of v_a at the beginning of the integration phase. The latter can be computed as

$$\begin{aligned} v_{a0,\Phi_2} = \frac{1}{C_{eq,\Phi_2}}\left(1 + \frac{C_L}{C_F}\right)\sum_{i=1}^{N} C_{Si}\{v_{i2}(nT) - v_{i1}[(n-1/2)T]\} + \\ + \frac{C^\star}{C_{eq,\Phi_2}} v_a(nT) \end{aligned} \tag{2.38}$$

where v_{i1}, v_{i2} are the voltages connected to the input of the ith SC branch during Φ_1, Φ_2, respectively, and $C^\star$ represents

$$C^\star = C_x + C_L\left(1 + \frac{C_x}{C_F}\right). \tag{2.39}$$

The integrator output voltage at the end of the integration phase can be obtained as

$$\begin{aligned} v_o[(n+1/2)T] = v_o(nT) + \sum_{i=1}^{N}\frac{C_{Si}}{C_F}\{v_{i1}[(n-1/2)T] - v_{i2}(nT)\} - \\ - \left(1 + \frac{C_x}{C_F}\right) v_a(nT) + \frac{1}{\beta} v_a[(n+1/2)T] \end{aligned} \tag{2.40}$$

as opposed to the ideal integration process with no dynamic limitations, in which the last two terms in Equation (2.40) are zero.
The amplifier GBW and output SR during this phase can be obtained similarly as for the sampling phase to be

$$\begin{aligned} \mathrm{GBW}_{\Phi_2}\ [\mathrm{rad/s}] &= \frac{g_m}{C_{eq,\Phi_2}}, \\ \mathrm{SR}_{\Phi_2}\ [\mathrm{V/s}] &= \frac{I_0}{\beta C_{eq,\Phi_1}}. \end{aligned} \tag{2.41}$$

2.3.3 Effect of Finite Amplifier GBW

The model for the transient response of SC integrators described can be easily incorporated into behavioral simulations for SC $\Sigma\Delta$ modulators to accurately quantify the influence of settling errors on the modulator performance. Besides this behavioral model, it is often useful to work with closed-form expressions which can help to gain insight of the influence of settling parameters on different modulator topologies. For this purpose, a linear transient response will be assumed for SC integrators now, in order to exclude the effect of SR.
The finite difference equation of an SC integrator can be obtained from Equations (2.31), (2.34), (2.36), (2.40)

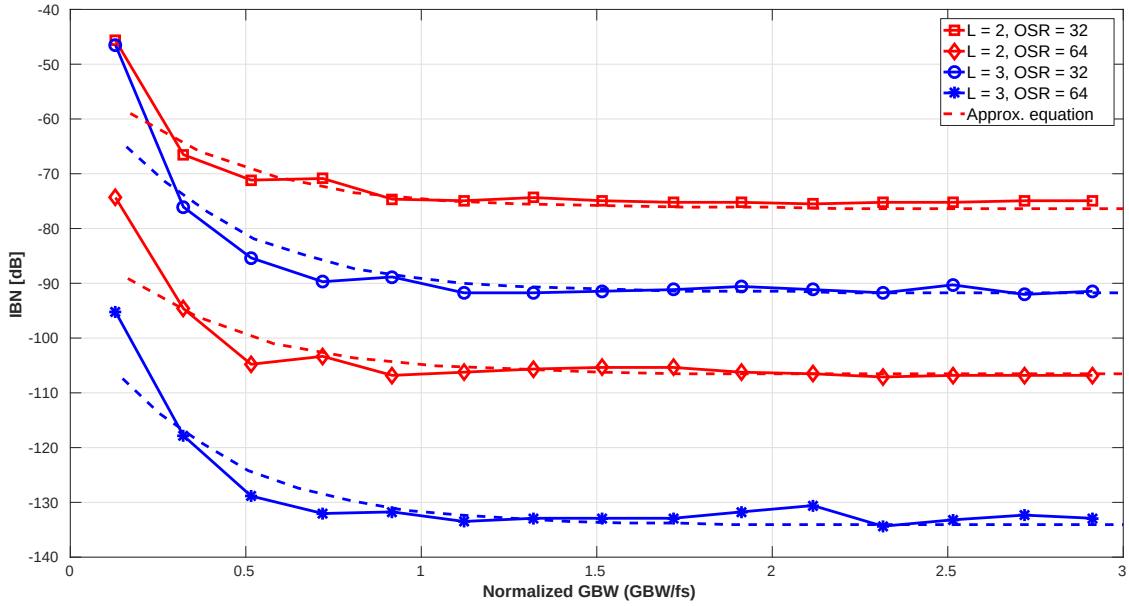


Figure 2.18: Simulation results for the influence of amplifier GBW on the in-band noise of SC ΣΔ modulators.

$$v_o[(n+1/2)T] \approx v_o[(n-1)T] + \frac{C_S}{C_F}(1-\epsilon_{ST})\{v_1[(n-1)T] - v_2[(n-1/2)T]\} \quad (2.42)$$

where only one input branch is considered for simplicity. The settling error associated with the linearly limited response is represented by ϵ_{ST}, which thus contain terms in $\mathrm{e}^{-\mathrm{GBW}_{\Phi_1}T/2}$ and in $\mathrm{e}^{-\mathrm{GBW}_{\Phi_2}T/2}$. If settling errors associated with integration dominate on the overall defective settling over those originated during sampling, the linear settling can be simply reduced to

$$\epsilon_{ST} \approx \mathrm{e}^{-\mathrm{GBW}_{\Phi_2}T/2}. \quad (2.43)$$

Transforming Equation (2.43) to the Z-domain, the integrator output results in

$$v_o(z) \approx \frac{C_S}{C_F}(1-\epsilon_{ST})\frac{z^{-1}v_1(z) - z^{-1/2}v_2(z)}{1-z^{-1}} \quad (2.44)$$

so that, under the assumptions made earlier, settling error translates into a gain error in the ideal filter transfer function $H_{ITF}(z)$, whose effect on the IBN can be computed as in the finite-gain amplifier case as

$$\mathrm{IBN} \approx \frac{\Delta^2}{12}\frac{\pi^{2L}}{(2L+1)\mathrm{OSR}^{2L+1}}\prod_{i=1}^{L}(1+\epsilon_{ST})^2 \quad (2.45)$$

Figure 2.18 illustrates the effect of the finite GBW on single-loop SC. As also apparent from Figure 2.18 the mathematical modeling proposed in Equation (2.45) follows well the simulated results.

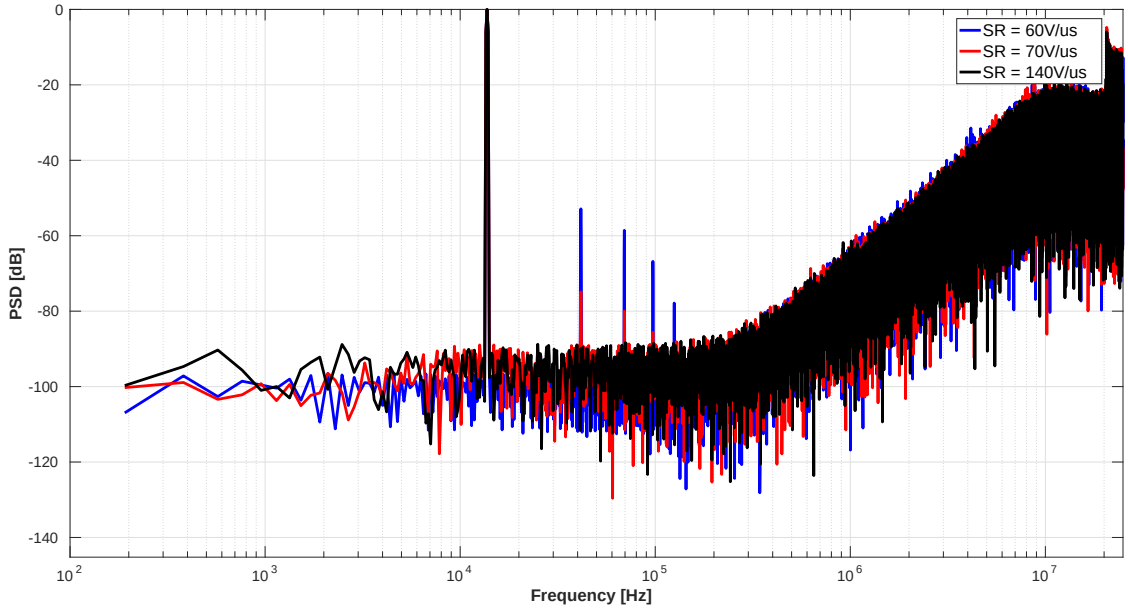


Figure 2.19: Simulation results for the influence of amplifier SR on the output spectrum of SC ΣΔ modulators.

2.3.4 Effect of Finite Amplifier SR

Contrary to errors arising from finite amplifier GBW, finite amplifier SR caused by limited output current I_0 capability has a purely non-linear effect on the performance of ΣΔ modulators, generating distortion and an increase in the noise floor.
For the case of a general SC ΣΔ modulators, SR-limited integrator dynamics basically translate into distortion. Figure 2.19 illustrates the impact of amplifier SR on a single bit second-order ΣΔ modulator operating with an oversampling ratio of 64. It is worth to notice that SR-limited integrator dynamic is a non-linear signal-dependent phenomenon whose occurrence frequency during the modulator operation is directly determined by the signal level at the integrators inputs. Therefore, the way to reduce SR requirements on a SC ΣΔ modulator is to exploit the multi-bit internal quantization, as it will be explained in Chapter 3.

2.3.5 Effect of Circuit Noise

Electronic noise generated in transistors and resistors is present in any circuit implementation and imposes an ultimate limit to the resolution of ADCs.
As previously stated, the influence of nonidealities on the IBN of ΣΔ modulators is mainly determined by the location of the corresponding noise source in the modulator. With respect to circuit noise, all SC integrators in a ΣΔ modulator add noise in the modulator pass-band, but the role of the front-end integrator is indeed dominant. In fact, when referred to the modulator input, noise power contributed by the remaining integrators is divided by the gain of preceding integrators within the modulator pass-band, so their influence strongly diminishes while moving from front-end to back-end integrators. However, no shaping takes place at the modulator

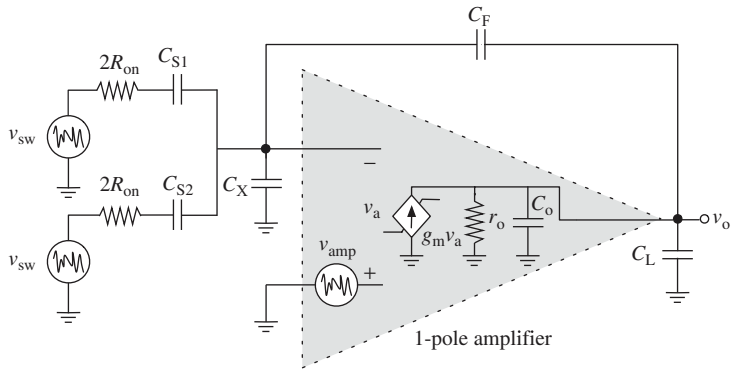


Figure 2.20: Equivalent circuit model for integration, with noise sources due to switches and due to the amplifier.

input and first integrator, therefore the design of this block is generally critical.
In a SC integrator the main elements that generate noise are the switches and the amplifier. A model of the SC integrator that highlights the noise sources is depicted in Figure 2.20. The noise generated by the switch is generated by the finite conductive resistance R_{on}. In Figure 2.20 the noise source of the switches is modeled as a source voltage v_{sw} in series with the resistors. The PSD of each of these noise sources in a single-sided frequency representation is thus $S_{sw} = 4kT \cdot 2R_{on}$ where k is the Boltzmann's constant and T is the absolute temperature. Each of the noise sources generates a sample-and-held noise component in the corresponding capacitor voltage given by the well-known kT/C expression [23-25]

$$S_{sw,C_{Si}}(f) \approx \frac{2kT}{C_{Si} f_s} \mathrm{sinc}^2(\pi f / f_s). \tag{2.46}$$

On the other hand, a single-pole model is assumed in Figure 2.20 for the amplifier and its equivalent input noise is modeled by v_{amp} at the positive input terminal. The amplifier noise is basically determined by a broadband thermal component and a narrow-band flicker component, so that

$$S_{amp}(f) \approx S_{amp,th}(f) + S_{amp,1/f}(f) \approx S_{amp,th}\left(1 + \frac{f_{cr}}{f}\right) \tag{2.47}$$

where $S_{amp,th}(f)$ represents the amplifier thermal noise PSD referred to its input and f_{cr} represents the amplifier corner frequency, namely the cross frequency between the $1/f$ noise and the white noise.
Adding up the former circuit noise components in the SC integrator, the total input referred noise PSD yields

$$S_{noise,in}(f) \approx \frac{8kT}{C_{S1} f_s}\left(1 + \frac{C_{S2}}{C_{S1}}\right) + S_{amp,th}\left(\frac{\mathrm{GBW}_{\Phi_2}}{2f_s} + \frac{f_{cr}}{f}\right)\left(1 + \frac{C_{S2}}{C_{S1}}\right)^2. \tag{2.48}$$

The input-referred IBN of an SC ΣΔ modulator due to circuit noise can be easily obtained by integrating the former expression over the input signal bandwidth, so that

$$\begin{aligned}\mathrm{IBN}_{noise} = &\frac{4kT}{C_{S1}\mathrm{OSR}}\left(1+\frac{C_{S2}}{C_{S1}}\right) + \\ &+ S_{amp,th}\left[\frac{GBW_{\Phi_2}}{4\mathrm{OSR}} + f_{cr}\ln\left(\frac{B_w}{f_0}\right)\right]\left(1+\frac{C_{S2}}{C_{S1}}\right)^2,\end{aligned} \tag{2.49}$$

in which the $1/f$ noise component has been integrated from a frequency $f_0 > 0$ to exclude DC due to its logarithmic nature. Therefore some practical issues can be deducted:

- For a given OSR, to reduce the contribution of the switches thermal noise the size of the sampling capacitors at the modulator input must be increased, which however results in larger speed requirements for the amplifier and thus in larger power consumption.
- For a given OSR, in order to reduce the contribution of the amplifier thermal noise, its GBW must be reduced as much as the integrator settling requirements allow.
- To reduce the flicker contribution the amplifier corner frequency must be kept low. This can be obtained by increasing the size of the input differential pair. Otherwise techniques as chopper are often used to reduce the $1/f$ component [26].

2.3.6 Effect of Clock Jitter

Discrete-time $\Sigma\Delta$ modulators are affected in practice by timing uncertainties6 in the clock phase that control the SC operation. However, they exhibit larger tolerance to clock jitter than Nyquist converters, because jitter sensitivity is reduced by the modulator OSR [27]. The effect of clock jitter in SC-$\Sigma\Delta$ modulators is mainly limited to a sampling uncertainty of the modulator input signal. Timing uncertainties during the integration phase only cause an extra error to be added to the integrator settling and their influence can be neglected in practice, whereas the contributions of other integrators than the front-end one will be reduced by noise shaping.
Sampling time uncertainty causes a non-uniform sampling of the modulator input signal that results in an increase of the in-band error power [27].
Under the assumption of white jitter, the power of this modulated error distributes uniformly, so that only a fraction is located within the pass-band. The in-band noise due to clock jitter can thus be easily obtained as

$$\mathrm{IBN_j} = \int_{-B_w}^{B_w} \frac{A_{in}^2}{2}\frac{(2\pi f_{in}\sigma_j)^2}{f_s}\mathrm{d}f = \frac{A_{in}^2}{2}\frac{(2\pi f_{in}\sigma_j)^2}{\mathrm{OSR}} \tag{2.50}$$

where σ_j represents the standard deviation of the timing uncertainty. Taking into account that $A_{in} \leq \Delta/2$ and $f_{in} \leq f_s/(2\mathrm{OSR})$, an upper bound can be calculated for Equation (2.50)

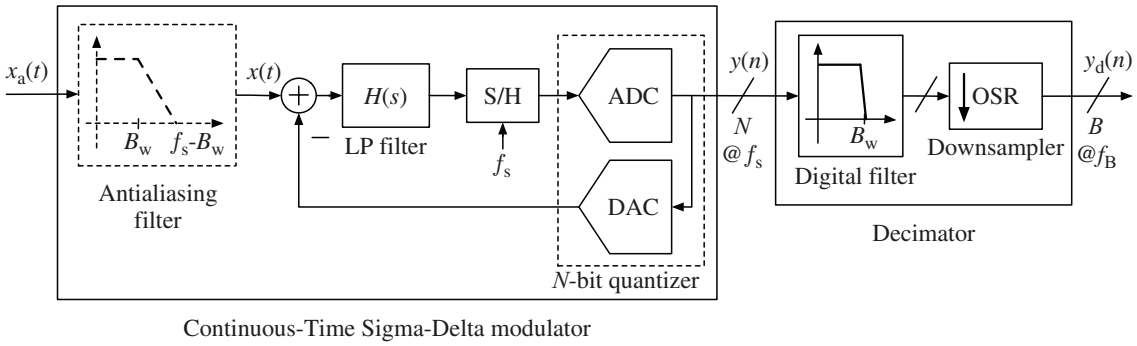


Figure 2.21: General block diagram of a continuous-time ΣΔ ADC. A low pass modulator is assumed.

$$\mathrm{IBN_j} \leq \frac{\Delta^2}{8}\frac{(\pi f_s \sigma_j)^2}{\mathrm{OSR}^3} \tag{2.51}$$

showing that the sensitivity of SC ΣΔ modulators to clock jitter is reduced by OSR^{-3}.

2.4 Continuous Time ΣΔ Modulators

The majority of ΣΔ modulators reported up to recent years were implemented using DT circuit techniques, mostly based on SC circuits. However, the increasing demand for even faster ADCs in broadband communication system has raised the interest in CT ΣΔ modulators over the past years, as they are able to operate at higher sampling rates with lower power consumption than their DT counterparts [20,28].

Figure 2.21 illustrates the general block diagram of a CT ΣΔ modulator for the case of LP input signals.

Looking at the differences between the DT and CT implementations, the most significant one is related to the location of the sampling operation, which moves from the modulator input in DT ΣΔ modulators to the point before the quantizer in CT ΣΔ modulators. The loop filter can thus be realized using CT circuit techniques, but, given that the modulator output is a DT signal and the modulator input is a CT signal, a discrete-to-continuous time transformation is required. The CT ΣΔ modulator presents some pros compared to the DT implementation:

- Errors associated to the sampling process have less impact on the modulator performance [29]. As the sampling operation takes place before the quantizer, the resulting errors attenuate in a similar way as the quantization error does.
- There is no settling error associated to the loop filter circuitry.
- They are not affected by kT/C noise as SC ΣΔ modulators do.

Despite the advantages could lead to consider a better solution the CT ΣΔ modulators, SC implementations have several advantages:

- Intrinsically lower parameter variations, as most circuit parameters are defined by capacitor ratios, instead of absolute parameter values as in the case of CT $\Sigma\Delta$ modulators.

- The DT $\Sigma\Delta$ is less affected by timing uncertainties [30]. Even though, in CT $\Sigma\Delta$ modulators, sampling time uncertainties occur at the quantizer input, where the jitter-induced error is strongly suppressed by the noise shaping, errors resulting from timing uncertainties in the DAC feedback signal add directly to the modulator input with no suppression, hence being the dominant jitter effect and limiting the overall modulator performance. It can be easily demonstrated that the jitter noise for a CT $\Sigma\Delta$ modulator is reduced by only OSR^{-1}.

- For the DT ADC, the STF for the analog portion is generally flat and dominated by the magnitude response of the decimation filter. The STF is not flat for a CT ADC. This is especially detrimental because it limits the useful input signal range for the ADC. In communications applications, with large out-of-band interferers, it can cause the ADC to become unstable. For these applications, it may be necessary to filter the interferers or sacrifice some of the ADC's dynamic range.

2.5 Conclusion

As described in this Chapter, $\Sigma\Delta$ modulators represents an interesting choice for high-resolution ADC. In order to achieve high-resolution the designers usually increase the oversampling ratio, with the result of decreasing the signal bandwidth, or they increase the modulator order, with the significant drawback on the stability issue of the modulator.
Therefore the $\Sigma\Delta$ is actually an ADC relegated in the low bandwidth application. Moreover, despite the $\Sigma\Delta$ is considered a topology with high robustness to the circuital non-idealities, when the modulator has to achieve high performance, some non-idealities can ruin the dynamic range of the modulator reducing consequently the resolution.
In the following Chapter a way to extend the modulator usage into high-bandwidth application is explained. Furthermore, as it will be explained, this method guarantees a higher robustness to the modulator non-idealities.

Chapter 3

System Analysis

The analysis of the non-ideal effects described in Chapter 2 allows deriving precise equivalent circuits and models for the different ΣΔ building blocks. This Chapter focuses its attention on a ΣΔ topology, namely the Feed-Forward (FF), which exploits a feed-forward loop in order to increase the linearity of the overall modulator [31]. Such topology is well-known in the literature of ΣΔ modulators, however some details are not well explained and, furthermore, some advantages of this particular topology are not always exploited.
A brief introduction to the ΣΔ FF topology is given and a comparison with the standard, or Feed-Back (FB) topology, is shown. Moreover a description of the main techniques to avoid the non-linearity of a multi-level DAC is given.
In the second part of this Chapter the System-Level Analysis of the design presented in this thesis is described. In order to evaluate all the system parameters, a strategy for the minimization of the overall power consumption is given.

3.1 Introduction to Feed-Forward Topology

With the continuing advancement of technology, oversampled data conversion is becoming attractive for use in wide-band applications. However, at very low oversampling ratio required for such applications, these ADCs are increasingly sensitive to circuit imperfections, and require high-quality analogue components. For instance, as described previously, the effects of limited DC-gain and finite bandwidth are less attenuated with a low OSR. Moreover, the advancement in technology scaling has brought several problems in the design of high-quality analogue components due to the low supply voltage.
Figure 3.1(a) shows the traditional topology described in the previous Chapter. Since the transfer function of the filter is the classical integrator

$$H(z) = \frac{z^{-1}}{1 - z^{-1}}, \tag{3.1}$$

it is easy to shown that the STF is just a delay of a single clock cycle. Therefore, the input signal of the integrator $X_1(z)$ is given by

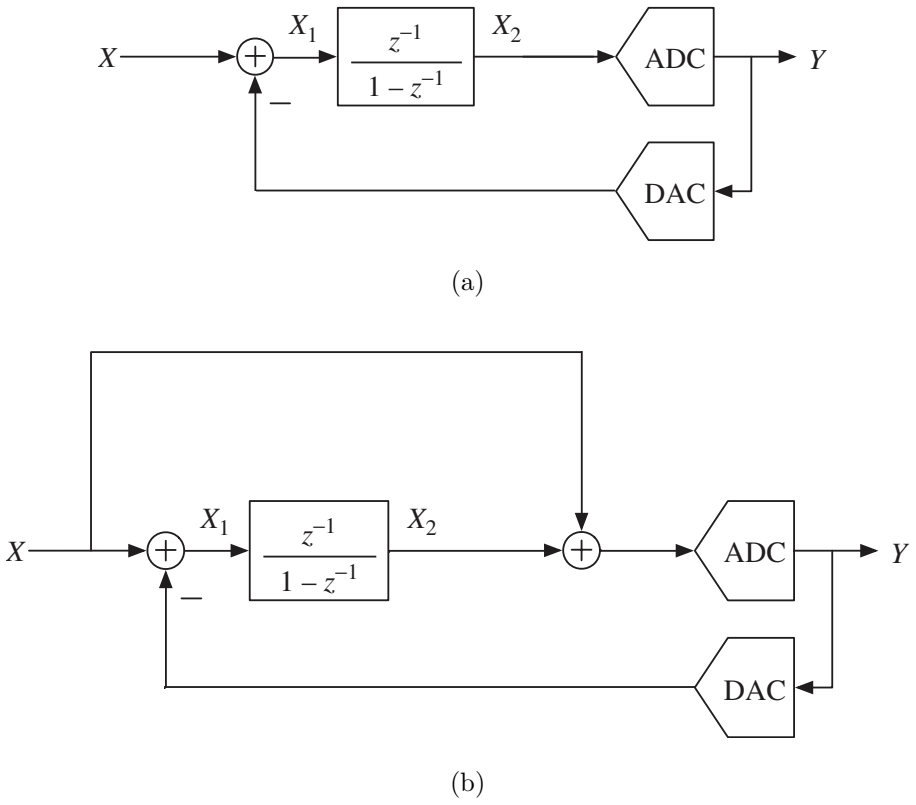


Figure 3.1: ΣΔ topologies: (a) the traditional FB topology; (b) the FF reduced distortion topology.

$$X_1(z) = X(z) - (\mathrm{STF}(z)X(z) + E(z)\mathrm{NTF}(z)) = X(z)(1-z^{-1}) - \frac{V_{FS}}{2^N - 1}(1-z^{-1}), \tag{3.2}$$

where $E(z)$ is the quantization noise. Therefore, increasing the number of bits N of the internal quantizer decreases the input $E(z)$ of the integrator. However, the delay introduced by the STF causes X_1 to contain a high-pass filtered version of the input signal X, which is restored to its full amplitude by the integrator. As already stated in the previous Chapter, because of non-linear effect of the amplifier, harmonic components of the input signal are created at the output of the modulator. As already stated these effects can be mitigated by increasing the OSR, however this solution is impractical in wide-band applications.
This non-linearity problem can be solved by canceling the delay in the STF between X and Y. This is achieved by the topology of Figure 3.1(b). In this case the STF is

$$\mathrm{STF}(z) = \frac{Y}{X} = 1. \tag{3.3}$$

It is easy to demonstrate that the noise transfer function is unaffected, but the integrators will now process quantization noise only. In fact Equation (3.2) is changed into

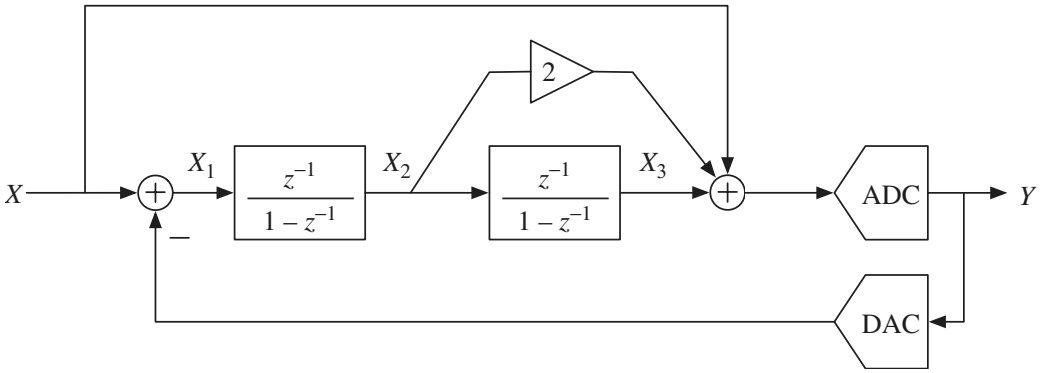


Figure 3.2: Second-order FF ΣΔ modulator.

$$X_1(z) = X(z) - (\mathrm{STF}(z)X(z) + E(z)\mathrm{NTF}(z)) = -\frac{V_{FS}}{2^N - 1}(1 - z^{-1}), \tag{3.4}$$

therefore the integrator is processing the quantization noise only.
The described concept can be extended to noise shaping of any order.
For istance in Figure 3.2 a second-order FF ΣΔ modulator is depicted. The main transfer functions of this modulator are

$$\begin{aligned} &\mathrm{STF(z)} = 1, \\ &\mathrm{NTF(z)} = (1 - z^{-1})^2. \end{aligned} \tag{3.5}$$

The removal of the input signal component reduces the swing at the internal nodes which relaxes the headroom requirements. In fact, as described in Chapter 1.3, one of the main challenges in scaled nanometric technology is the reduced supply voltage which implies also a reduction in the available output headroom voltage.
In Figure 3.3 the output swing voltage of the first and of the second integrator is shown.
The output of the two integrators is given by

$$\begin{aligned} X_2(z) &= X_1(z)\left(\frac{z^{-1}}{1 - z^{-1}}\right) = -E(z)z^{-1}(1 - z^{-1}) = -\frac{V_{FS}}{2^N - 1}z^{-1}(1 - z^{-1}), \\ X_3(z) &= X_1(z)\left(\frac{z^{-1}}{1 - z^{-1}}\right)^2 = -E(z)z^{-2} = -\frac{V_{FS}}{2^N - 1}z^{-2}. \end{aligned} \tag{3.6}$$

Equation (3.6) shows that both the integrators do not process the input, but only the quantization noise. In fact the output swing of the integrators is not related to the input voltage, but to the quantization noise, and, therefore, to the number of bits of the internal quantizer N. It is significant to notice that if a single bit quantizer is used the advantage of the reduced input swing is not exploited [32]. In fact, the signal processed by the integrators is still not related to the modulator input, however the output swing is given by the full scale voltage V_{FS}. This does not reduce the headroom voltage, therefore the unitary STF does not ensure itself the high linearity.

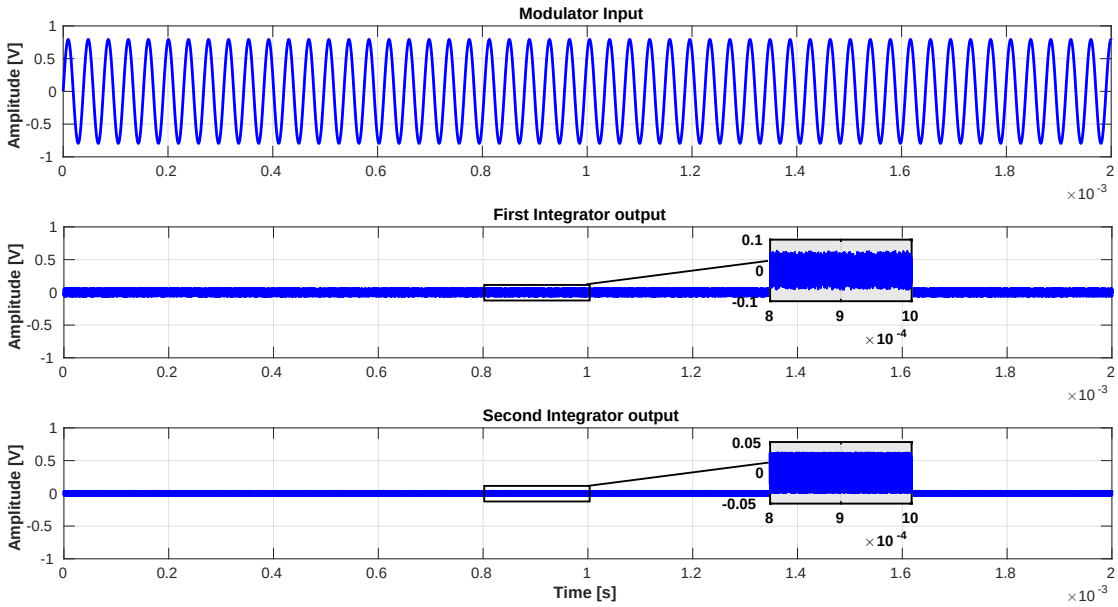


Figure 3.3: Output swing of integrators in a second-order FF ΣΔ with a 5 bit internal quantizer.

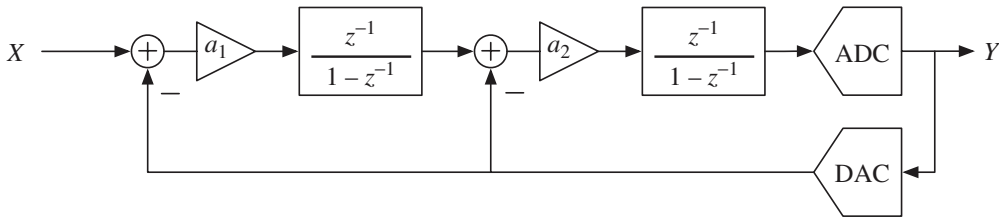


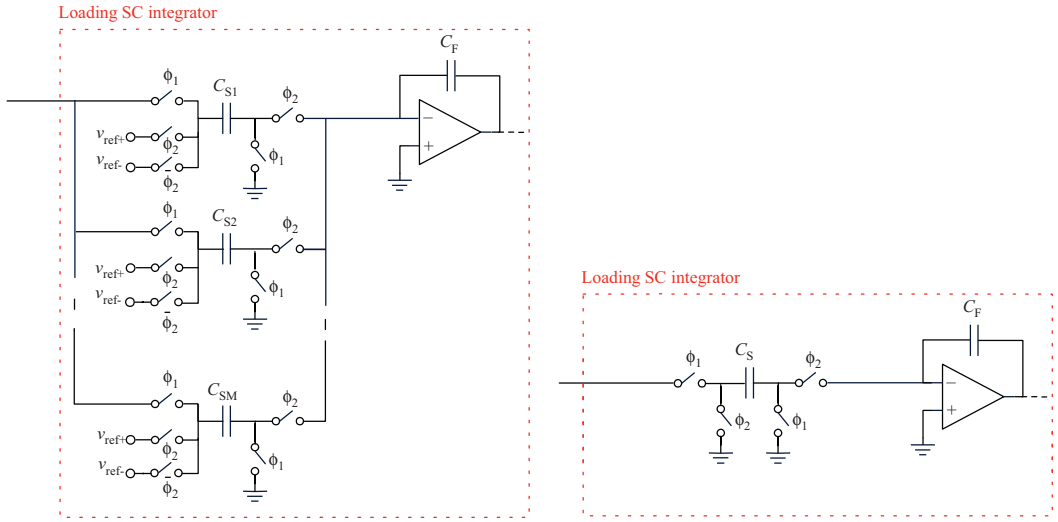
Figure 3.4: Second-order FB ΣΔ modulator.

3.2 FF and FB ΣΔ - Comparison

In order to highlight the advantages of the FF ΣΔ topology, some differences with the standard topology are drawn below. In Figure 3.4 a second-order traditional ΣΔ is depicted.

3.2.1 Single Loop

The first noticeable difference with the modulator of Figure 3.2 is the single feedback loop. In fact, regardless of the modulator order, the FF topology has a single feedback loop, while the number of loops in a FB ΣΔ is equal to the modulator order L. This not only increases the area occupied by the modulator, but furthermore increases the power consumption of the first integrator. In fact, since the capacitor size of the second integrator is not critical in terms of thermal noise, usually a small capacitor is used in order to decrease the capacitor load of the first integrator. However, in a multi feed-back loop, the feedback loop into



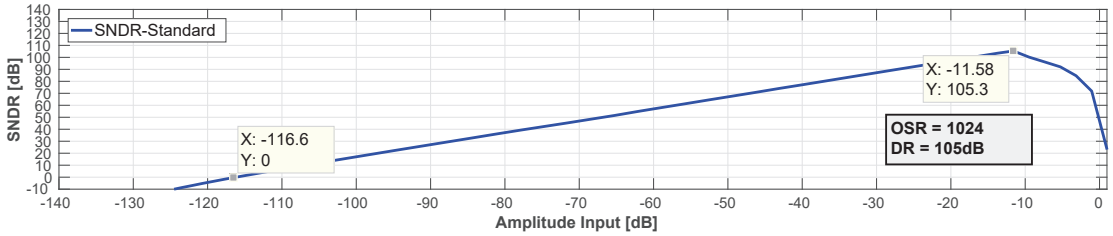
(a) (b)

Figure 3.5: Loading SC Integrator for ΣΔ modulators: (a) Integrator Load for a FB ΣΔ, (b) Integrator Load for a FF ΣΔ.

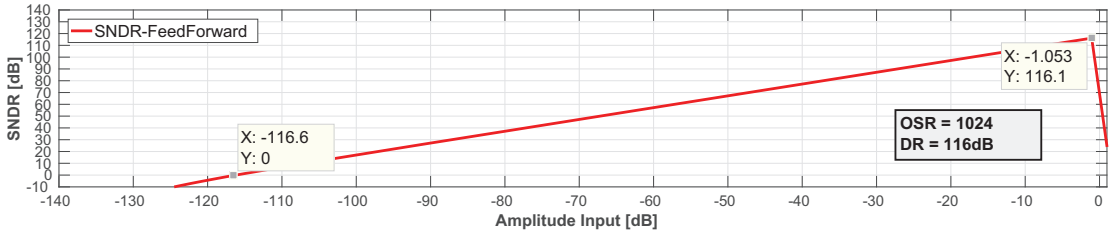
the second integrator implies to realize the DAC embedded not only in the first integrator, but also in the second integrator. In Figure 3.5(a) the second integrator for a standard ΣΔ topology is depicted. In general, for a N multi-bit quantizer, a $M = 2^N$ paths integrator has to be designed. Since the coefficient transfer function is realized by the ratio of the capacitors $\sum_{i=1}^{M} C_{Si}/C_F$, where C_{Si} are the sampling capacitors of the M paths and C_F is the feedback capacitor, the size of the total sampling capacitor $C_S = \sum_{i=1}^{M} C_{Si}$ is limited by the factory minimum size. In fact, defining C_{min} as the minimum size of the capacitor guaranteed by the factory rules, the minimum size of the sampling capacitor must be $M \cdot C_{min}$. Conversely, as shown in Figure 3.5(b), there is no need in the FF topology of splitting up the sampling capacitor, therefore it is possible to use a much smaller capacitor.

3.2.2 Lower Distortion

As shown in Equations (3.4) and (3.6) in the FF topology the integrators do not process the input signal, but only the quantization noise. Combined with a multi-bit quantizer this property can greatly reduce the output swing of the integrators, avoiding the distortion due to headroom saturation. In fact, when a full-swing signal is applied as input of the modulator, since the signal processed by the integrators is not related to the input, the SNDR does not degrade. Conversely, in the FB topology, when a large input is applied, the harmonics at the output of the integrators become noticeable and the SNDR starts to deviate from the SNR curve. This fact is appreciable in Figure 3.7.
Figure 3.7 reports the simulated SNDR as a function of the input signal amplitude (normalized to the ADC full-scale voltage) for both architectures. It is worth to stress out that these simulations include the thermal noise, that in fact is the dominant noise source in the conversion bandwidth. Therefore the two architectures



(a)



(b)

Figure 3.6: Behavioral simulation of the otuput SNDR: (a) in FB topology; (b) in FF topology. Thermal noise is included in this simulation.

exhibit the same noise floor, although the forward architecture actually has a much lower quantization noise level, being a multi-bit modulator. As a consequence, the SNDR graphs for low input level are very similar. Observing the estimated SNDR at high input level, it is apparent that in the FB architecture the amplifier distortion and limited swing make the SNDR gradually fall down and in fact the peak SNDR is achieved at an input level of -11dB. Conversely in the forward architecture these impairments are absent and the SNDR can increase with the input level approaching almost the full-scale voltage. This translates into the forward architecture having a 11dB larger DR [33]. Since the DR is generally higher in the FF topology, in order to reach the same resolution with a FB topology it is necessary to increase the OSR. This explains why this topology becomes famous for wide-band applications.

3.2.3 Amplifier Requirements

Besides the higher linearity, we can appreciate how much the forward architecture is outperforming the feedback one, only estimating the required performance of the amplifiers. The required output swing for the forward architecture is obviously greatly reduced, as already explained. The combination of a forward architecture with a multi-bit quantizer allows to use single-stage amplifiers, instead of multi-stage rail-to-rail amplifiers. This obviously translates into a much lower power consumption, since there is no need of additional load capacitors to stabilize the amplifier. In Table 3.1 a comparison between the most common Operational Transconductance Amplifier (OTA) topologies is presented. The multi-stage OTA is an attractive solution, since it joins a high output swing with high gain. However the output capacitor is higher if related to other OTA topologies, since a Miller capacitor C_M is needed in order to stabilize the amplifier. Since in FF architecture the voltage swing is not a real issue, low power amplifier OTAs can be used. One

	Single-Stage OTA		Multi-Stage OTA
Topology	Telescopic OTA	Folded Cascode	Miller OTA
out swing	$V_{DD} - 5V_{dsat} - v_{in,cm}$	$V_{DD} - 4V_{dsat}$	$V_{DD} - 2V_{dsat}$
out capacitor	C_o	C_o	$C_o + C_M$
gain	medium	medium	high
power consumption	low	low	medium

Table 3.1: Comparison between Single-Stage OTAs and the Miller OTA.

could point out that the DC-gain of single-stage OTA is not comparable with the multi-stage one. However this is not a problem in the FF architecture. Since the ADC input signal is no longer processed by the integrators a less demanding amplifier in term of DC-gain can be used. As already discussed in Chapter 2.3.1, the effect of limited DC-gain is to increase the in-band quantization noise power. This is generated by the fact that a fraction of the previous sample out of the integrator is added to the sample input. The integrator leakage is given by

$$v_o(nT) - \alpha v_i[(n-1)T] = \frac{1 + \left(1 + \frac{C_x}{C_F}\right)\frac{1}{A_v}}{1 + \left(1 + \frac{C_x}{C_F} + \sum_{i=1}^{N}\frac{C_{Si}}{C_F}\right)\frac{1}{A_v}} v_o[(n-1)T], \tag{3.7}$$

where α is the gain error defined in Equation (2.23). However, since $v_o[(n-1)T]$ is the amplified version of the small voltage at the inverting input of the amplifier, namely $v_a[(n-1)T]$, the integrator leakage is negligible.
In Figure 3.7 the SNR is plotted as a function of the DC-gain A_v of the first integrator. After the crossing point between the solid line, which represents the limited DC-gain amplifier, and the dashed line, which represents the ideal SNR, the effect of the limited DC-gain amplifier becomes neglectable. It is apparent from Figure 3.7 that the gain needed for the FF architecture to achieve the ideal SNR is much lower than the gain in the FB topology. Therefore, not only the output swing of the amplifier is greatly reduced, but also a significant reduction in the required gain is obtained. This gives the possibility to use the single-stage OTA of Table 3.1, even though their DC-gain is not high, especially when compared with multi-stage OTA.
Furthermore, the swing reduction also implies a significant reduction in the minimum slew-rate. In fact, the slot time t_0 in which the amplifier is in slewing is given by

$$t_0 = \frac{A_v\beta}{1 + A_v\beta}\frac{V_{in}}{\mathrm{SR}}. \tag{3.8}$$

Equation (3.8) implies that if the input signal V_{in} is small, also the slewing-time t_0 is reduced. This fact is even more clear by looking at the source of the SR issue. In fact an amplifier shows a linear settling, instead of an exponential settling, if

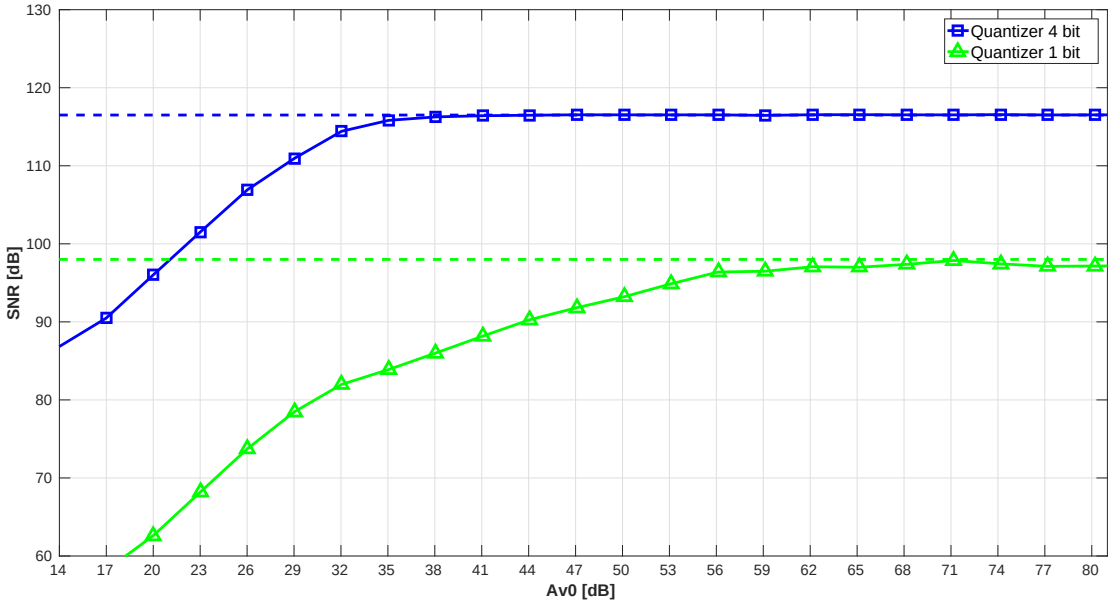


Figure 3.7: SNR as a function of the gain of the first integrator in a FF topology with a 4 bit embedded quantizer and a FB topology with a single bit embedded quantizer. Dashed line represents the ideal case.

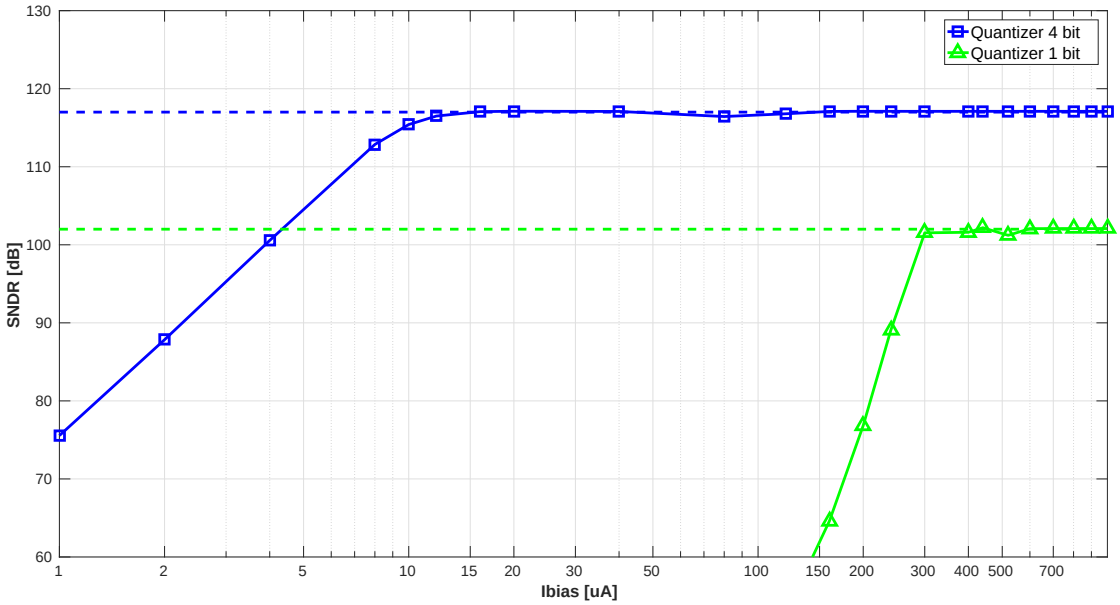


Figure 3.8: SNR as a function of the bias current I_{bias} of the first integrator in a FF topology with a 4 bit embedded quantizer and a FB topology with a single bit embedded quantizer. Dashed line represents the ideal case.

the differential input is completely unbalanced, which happens when $V_{in} > \sqrt{2}V_{ov}$. Therefore, if a small input differential voltage V_{in} is applied, the differential couple is never unbalanced. Since the ADC input signal is no longer processed by the

integrators, a less accurate settling is tolerated, and hence a less demanding amplifier of bandwidth can be used.
It is possible to reconduct the amplifier GBW and output SR to the bias current I_{bias}

$$\begin{aligned} \text{GBW [Hz]} &= \frac{g_m}{2\pi C_{eq}} = \frac{g_m}{2\pi C_{eq}} \frac{I_{bias}}{I_{bias}} = \frac{I_{bias}}{4\pi C_{eq}} \cdot \frac{g_m}{I_D}, \\ \text{SR [V/s]} &= \frac{I_{bias}}{\beta C_{eq}}, \end{aligned} \tag{3.9}$$

where $I_D = I_{bias}/2$ and g_m/I_D is a technology parameter. Therefore a similar graph as the one for DC-gain of Figure 3.7 can be plotted. In Figure 3.8 the effect of limited SR and GBW becomes negligible when the solid line reaches the dashed line, which represents the ideal case. It is apparent that the crossing point is reached for lower values of I_{bias} in the FF topology, which implies a lower power consumption, but furthermore implies lower GBW and lower SR, since they are both proportional to I_{bias}.

3.2.4 Multi-bit Quantization

The several benefits described previously, guaranteed by the combination of the unitary STF and the multi-bit embedded quantizer, lead to an optimized design in terms of power consumption, high linearity and high bandwidth. However multi-bit quantizers also have an important drawback that may counter the former advantages. In fact, contrary to 1 bit quantizers, which are intrinsically linear because only two levels are used for quantization, multi-bit quantizers exhibit in practice some non-linearities in their transfer characteristic, mostly due to device mismatching, which significantly influence the ΣΔ modulator performance.
When a multi-bit quantizer is used, also a multi-level DAC in the feedback loop is needed. Errors related to the multi-level DAC are injected in the feedback path, and, therefore, they directly add to the ΣΔ modulator input signal and pass to the ΣΔ modulator output as part of the input signal itself. Consequently, the linearity of a multi-bit ΣΔ modulator will be no better than that of the multi-bit embedded DAC, and the latter must be designed to achieve the linearity target for the whole ΣΔ ADC, what may be challenging under the influence of component mismatching. Figure 3.9 illustrates the architecture that is typically used for the multi-bit quantizer. The N bit ADC consists of a bank of $M = 2^N - 1$ comparators that digitizes the loop filter output into thermometer code, which will be subsequently coded into binary. The DAC employs M unit elements, namely capacitors in SC implementation, to reconstruct the analog feedback signal using 2^N levels. The i-th analog output level is generated by activating i unit elements and adding their outputs. DAC errors are caused by the mismatching between its unit elements, which makes the DAC output levels deviate from their nominal values. Assuming that the actual value of each unit element follows a Gaussian distribution, the worst-case relative error in the DAC output y_{DAC} can be estimated

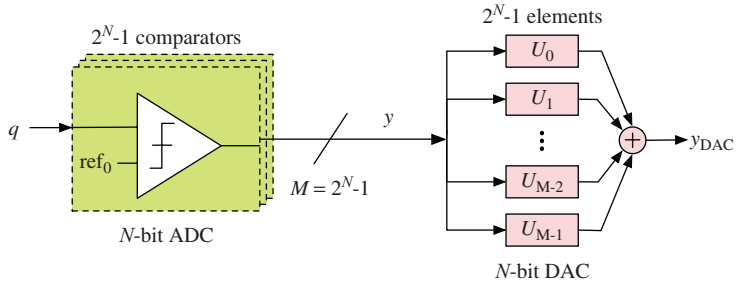


Figure 3.9: Topology of a typical multi-bit quantizer embedded in a ΣΔ modulator.

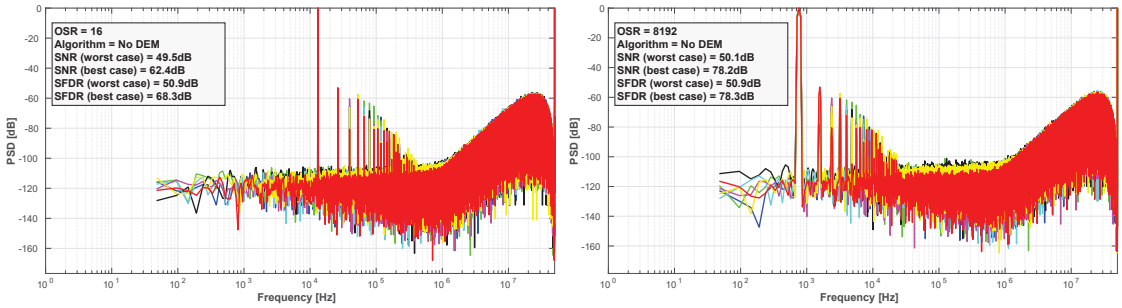
from the derivative of the variance of the mismatch between the unit elements as

$$\sigma\left(\frac{\Delta y_{DAC}}{y_{DAC}}\right) = \frac{1}{2\sqrt{2^N}} \cdot \sigma\left(\frac{\Delta U}{U}\right), \tag{3.10}$$

where $\sigma\left(\Delta U/U\right)$ stands for the relative error in the value of the unit element. Equation will be analytically demonstrated in Appendix A.1. Obviously, the DAC accuracy increases with the number of unit elements, as stated by the weak law of large numbers. In fact, for a large numbers of identically distributed random variables, it can be demonstrated that the probability that the nominal value differs from the mean value of an arbitrary positive ϵ tends to zero. However, for a ΣΔ with a 4 bit embedded quantizer in order to achieve a 16 bit linearity a matching better than 0.01% is needed. Device matching achieved in present-day CMOS processes is nevertheless in the range of 0.1% (10 bits). This means that achieving linearities better than 12 or 13 bits in multi-bit ΣΔ modulator by means of relying only on standard device matching usually leads to prohibitive area occupation.
A direct method to improve the standard device matching is laser trimming, which can sometimes be done at the foundry, but at the expense of additional fabrication and measurement steps and increased cost. Calibration and correction schemes have also been proposed, either in analog or digital domain, but they are often expensive to implement.
Among the different alternatives that have been developed through the years for achieving high-linear multi-bit ΣΔ, the DEM technique prevail because of the modest component matching required.

3.3 Dynamic Element Matching

In Figure 3.10 the effect of a non-linear DAC is shown. As previously discussed, mismatches among the unit elements cause DAC non-linearities that generate harmonic distortion in ΣΔ modulator. This distortion does not take advantage of any noise shaping, since it is generated in the feedback loop.
For a multi-bit DAC as the one of Figure 3.9, there is an univocal correspondence between the thermometric code input y and the respective error of the DAC output y_{DAC}, because the same unit elements are always used for generating a given DAC output level. The operation principle of DEM consists in breaking this direct



(a) (b)

Figure 3.10: No DEM: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations.

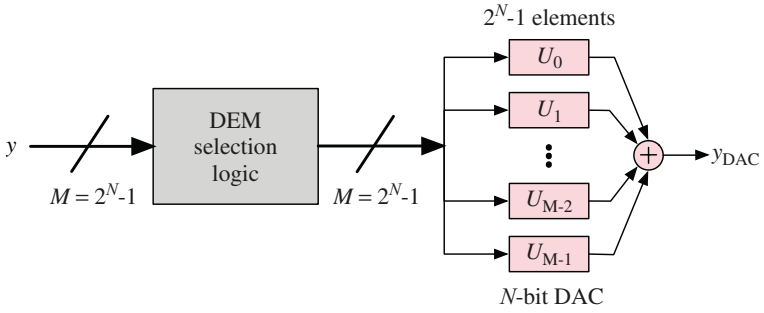


Figure 3.11: Topology of a typical multi-bit feedback DAC in a $\Sigma\Delta$ modulator with DEM algorithm.

correspondence by varying over time the set of elements that are employed for generating a given DAC level, thus transforming its fixed error into a time-varying one [34,35]. To that purpose, as conceptually shown in Figure 3.11, a digital block is incorporated, which controls the selection of unit elements at each clock cycle according to an algorithm that tries to null the average error in each DAC level over time.

To realize a noise shaping DEM, there are many choices with their own trade-offs between performance and complexity. For any DEM algorithm it can be estimated the Signal to Mismatch Noise Ratio (SMNR)

$$\text{SMNR [dB]} = 10 \cdot \log \left(\frac{2^N}{2\sigma_w^2 (1 - 2^{-N})^2 \int_{-\pi/\text{OSR}}^{\pi/\text{OSR}} |H_{DEM}(\omega)|^2 \text{d}\omega} \right) \tag{3.11}$$

where H_{DEM} is the mismatch spectral shaping function of the DEM algorithm and σ_w is the mismatch between unit elements, as it will be demonstrated in Appendix A.3.

The general goal of DEM is to modify the distortion terms, hence signal-dependent

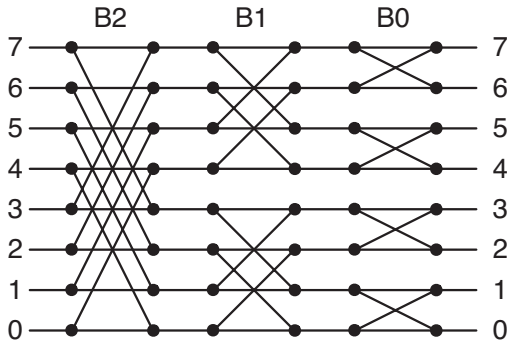
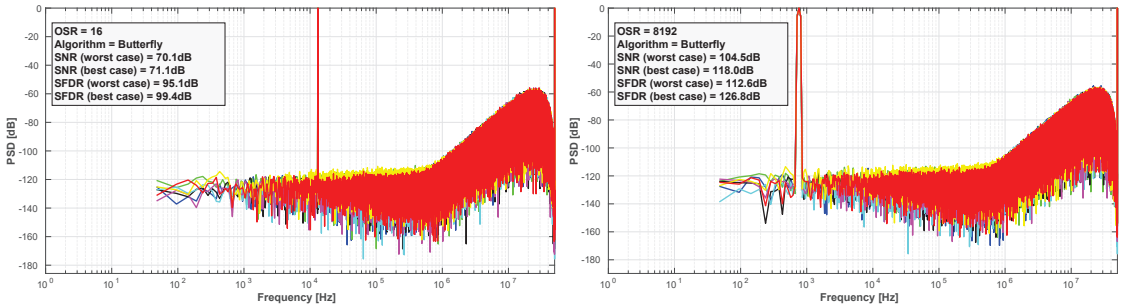


Figure 3.12: Randomization of the selection of unity elements with a butterfly randomizer with three bit control.

errors, to become signal-independent. Therefore, by using DEM, the idea is to reduce the SFDR.

3.3.1 Butterfly Randomization

A first approach to use DEM in a $\Sigma\Delta$ was introduced by Carley in [36] and by Leung [37]. The element selection logic performs a randomization.
The selection of the unity element is defined by the randomizer that receives the thermometric code out of 2^N input lines and generates a scrambled set of 2^N controls.
Notice that the number of possible scrambled outputs is $(2^N)!$ which is a very large number even for a relatively small number of levels. Such a large number of connections is difficult to code but also all these connections are not strictly necessary for obtaining a random result. What is actually necessary is avoiding frequent repetitions of the same or similar code which would produce tones and not noise-like spectra.
It is typically enough to randomize the elements with a subset of possible connection. A very effective solution is shown in Figure 3.12 known as the butterfly randomization, consisting of a series of butterfly switches coupling inputs to outputs. This kind of randomizer cannot generate all the possible connections, however the use of $\log_2(2^N)$ butterfly stages, as done by the scheme of Figure 3.12, ensures that any input can be connected to any output. The control of the butterfly switches can be done using $\log_2(2^N)$ bits. More simply the control can be done by successive divisions by 2 of the clock.
Figure 3.13 shows the simulation results for a second-order $\Sigma\Delta$ FF converter when randomization is used for the selection of the DAC elements. As a result of the randomization a white-noise floor for low frequencies is shown. For high frequencies the second-order noise shaping is still present. Since no harmonic distortion components are visible, the SNDR is significantly better if compared to the simulations of Figure 3.10.
It can be demonstrated that the SNR determined by just the mismatch error and



(a) (b)

Figure 3.13: Butterfly DEM: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations.

an OSR oversampling results

$$\mathrm{SNR} = \frac{3 \cdot 2^N \cdot \mathrm{OSR}}{\sigma_w^2}. \tag{3.12}$$

The mathematical demonstration of Equation (3.12) is described in Appendix A.2. This equation has been also validated by Montecarlo simulations. In Figure 3.14 the simulated SNR is compared with the mathematical modeling of Equation (3.12). It is apparent that the benefit given by the butterfly randomization is just 3dB per octave, as it happens for a plain oversampling architecture. Instead, for $\Sigma\Delta$ converters it would be profitable to have, in addition to the quantization noise shaping, a shaping of the mismatch error.

3.3.2 Individual Level Averaging (ILA)

The individual level averaging (ILA) approach aims to excercising each unity element with equal probability for each digital input code [37,38]. The algorithm uses a register of indexes, one index $I_k(i)$ for each possible input code k. The elements that are used when code k is applied are $I_k(i), I_k(i)+1..., I_k(i)+k-1$, where i represents the time index. When the index exceeds the number of elements, then the selection wraps around and the first element is used.
The result is that successive occurrences of the same code leads to the use of all the unity elements of the array. As mentioned, this method requires using indexes, as shown in Figure 3.15, for remembering the used set of elements for converting a given code so a different set is used at the next occurrence of the input code. In this way, after a few conversions of the same input, all the elements of the DAC are employed, and the mismatch is averaged out.
There are two methods for selecting elements: the rotation approach and the addition approach. The rotation approach, shown in Figure 3.15(a), increases the index of the code k, I_k, by one each time the code k occurs. The addition method increases by k the index I_k modulo 2^N all the times an input whose value is k occurs.
In order to better understand the algorithm in Figure 3.15 an input sequence

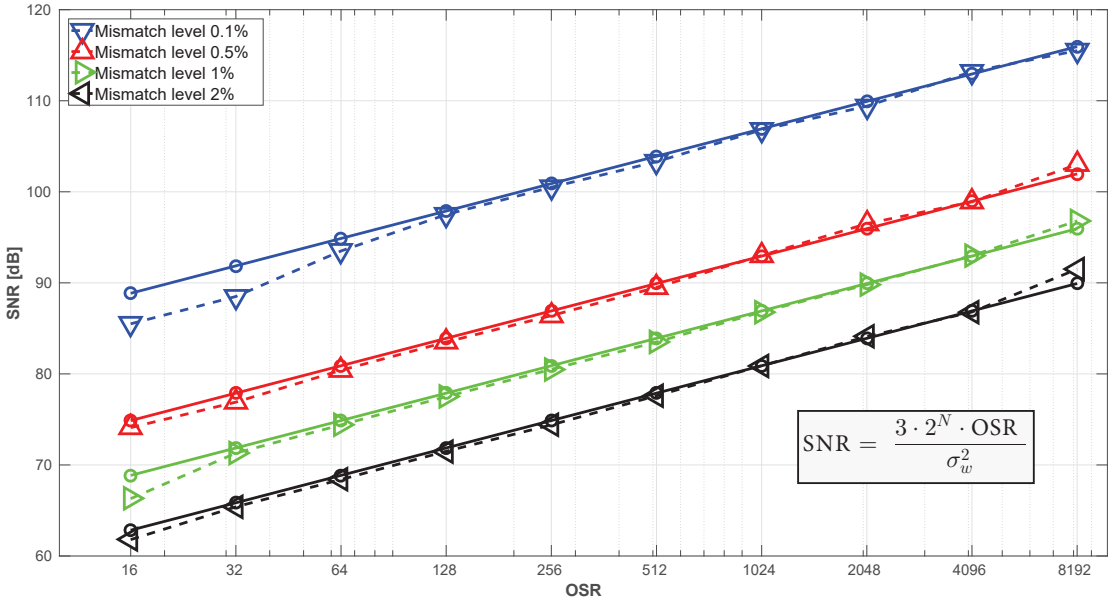


Figure 3.14: SNR as a function of the OSR and of the mismatch among unit elements when Butterfly randomization is applied. The solid line represents the simulated results, while the dashed line represents the mathematical modeling.

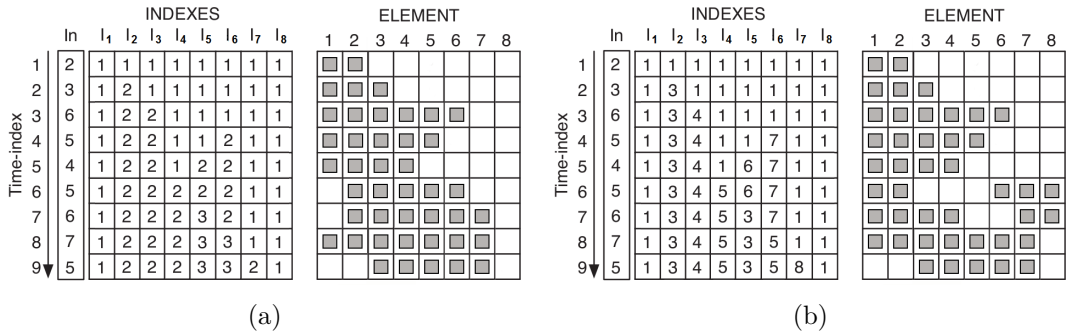


Figure 3.15: Operation principle of the (a) rotation approach and of the (b) addition approach of ILA. The shaded boxex indicate which unit elements contribute positive for a 3 bit DAC employing ILA.

example made by [2 3 6 5 4 5 6 7 5] is considered. Initially all the indexes are equal to 1. Then, when the input is equal to 5, the index I_5 is updated to 2 in the rotation approach, while it is updated to 6 in the addition approach. The next time the input is 5, the selected unit elements start from the element 2 in the rotation approach, while from the element 6 in the addition approach.
Figure 3.16 shows the effect of both the ILA approaches in a second-order FF modulator. For low frequencies, a first-order shaping of the DAC-error can be observed. Due to this noise shaping, the DAC-error is smaller than for Butterfly algorithm at low frequencies. Therefore, the performance will be significantly better

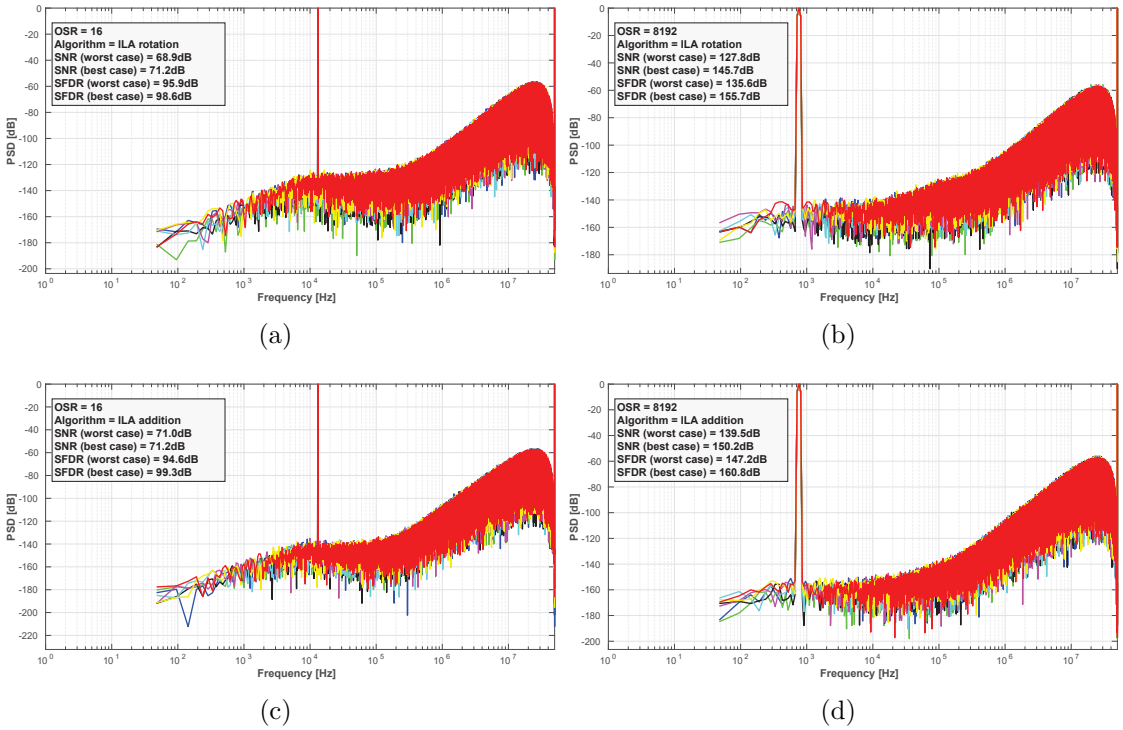


Figure 3.16: ILA DEM: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in the rotation approach, and for low OSR case (c) and high OSR case (d) in the addition approach. A second-order FF modulator is considered. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations.

for large oversampling ratios. It is worth to notice that this shaping is not present for higher frequencies.

3.3.3 Data Weighted Averaging (DWA)

Data weighted averaging (DWA) was introduced in [39] and resembles ILA quite closely, but it is less complex. Instead of using a separate register for each possible input code, DWA uses only one register which is common to all input codes.
The advantage of DWA methos is that the rotation cycle is fast thanks to the update of the only index every clock period [40]. The update logic of DWA is shown in Figure 3.17. For each phase the index is increased by the value of the input. The register always points to the first unused unit element. DWA rotates through all the elements such that all the elements are used at the maximum possible rate and each element is used the same number of times. This ensures that the errors introduced by DAC quickly average to zero.
It is relatively easy to show that DWA method determines a first-order shaping of the mismatch error [41]. With the aim to demonstrate the first-order shaping of the distortion generated by the mismatch among the capacitors, U_{mean} is defined as the mean between the unit elements of the DAC, namely

$$U_{mean} = \frac{1}{2^N} \sum_{i=1}^{2^N} U_i. \tag{3.13}$$

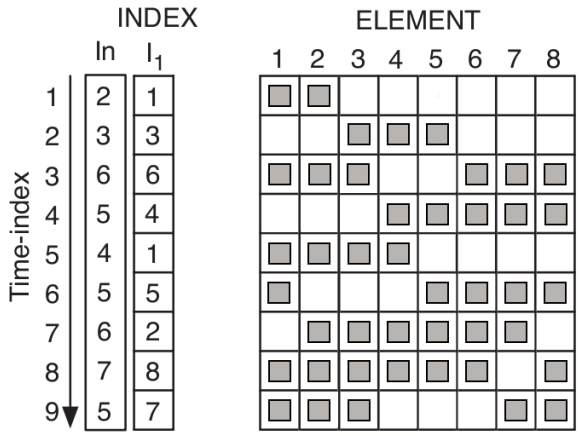


Figure 3.17: Operation principle of the rotation of DWA. The shaded boxex indicate which unit elements contribute positive for a 3 bit DAC employing DWA.

Let $y(k)$ the input of the DWA, $y_{DAC}(k)$ the output of the DWA and $I(k)$ the index of DWA at time k. Under the hypothesis that $I(k-1) < I(k) - 1$, the output of the DWA for a general input $y(k)$ can be written as follows:

$$\begin{aligned} y_{DAC}(k) &= \sum_{i=I(k-1)}^{I(k)-1} U_i = \sum_{i=I(k-1)}^{I(k)-1} (U_{mean} + \delta U_i) \\ &= U_{mean} \cdot y(k) + \sum_{i=I(k-1)}^{I(k)-1} \delta U_i \\ &= U_{mean} \cdot y(k) + \epsilon(k). \end{aligned} \tag{3.14}$$

Equation (3.14) can be easily translated into

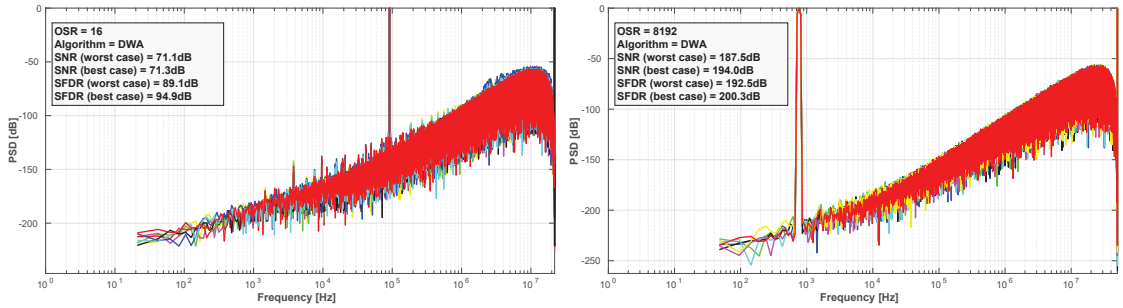
$$\begin{aligned} \epsilon(k) &= \sum_{i=I(k-1)}^{I(k)-1} U_i - y(k) \cdot U_{mean} \\ &= \sum_{i=I(k-1)}^{I(k)-1} U_i - [I(k) - 1 - I(k-1) + 1]\, U_{mean} \\ &= \sum_{i=1}^{I(k)-1} U_i - [I(k) - 1] U_{mean} - \sum_{i=1}^{I(k-1)-1} U_i + [I(k-1) - 1] U_{mean} \end{aligned} \tag{3.15}$$

where $\epsilon(k)$ is the mismatch contribution.
Defining the Integral Mismatch function $IM(I(k))$ as the sum between the differences of the actual unit elements with the mean among all the elements, namely

$$IM(I(k)) = \sum_{i=1}^{I(k)} (U_i - U_{mean}) = \sum_{i=1}^{I(k)} U_i - I(k) \cdot U_{mean} \tag{3.16}$$

it is possible to modify Equation (3.15) as

$$\epsilon(k) = IM(I(k)) - IM(I(k-1)) \tag{3.17}$$



(a) (b)

Figure 3.18: DWA: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations.

which is, in the Z-domain

$$E(Z) = (1 - z^{-1})IM(I) = H(z) \cdot IM(I), \tag{3.18}$$

showing that, as already stated, the mismatch among the unit elements is shaped by a first-order noise shaping function. It is worth to notice that the Integral mismatch function has actually the same definition of the INL, but applied to the mismatch between the unit elements.
The SNR that can be obtained with DWA is given by

$$\text{SNR} = \frac{3 \cdot 2^N \cdot \text{OSR}^3}{4\pi^2 \sigma_w^2 \cdot (1 - 2^{-N})^2} \tag{3.19}$$

as it will be demonstrated analytically in Appendix A.4. It is interesting to notice from Equation (3.19) that increasing the number of bits of the internal quantizer leads to a higher SNR. This is motivated by the fact that the effect of the mismatch between the unit elements is reduced when the number of bits is increased, as apparent also from Equation (3.2.4).
Figure 3.18 shows simulation with DWA. The graphs clearly show that DWA performs significantly better than the previously discussed DEM techniques, and it is proven also by simulations that DWA provides first-order shaping of the DAC error. However, Figure 3.18(a) shows that the DAC error contains harmonic distortion components and tones. This problem is very well known in the literature and it is generated by the cyclic nature of selection of DAC units in the DWA algorithm. This logic may generate tones in the modulator output spectrum that may be folded back into the signal band. Supposing a constant input value of the DAC Y_{DAC}, it is easy to see that DWA ends a complete rotation in $2^N/[\text{gcd}(Y_{DAC}, 2^N)]$, where $\text{gcd}(Y_{DAC}, 2^N)$ is the greatest common divisor between the input and the number of elements. As a result we have a period sequence in the mismatch error

$$\left\{ \sum_{i=1}^{Y_{DAC}} \epsilon_i \quad ; \sum_{i=Y_{DAC}+1}^{2 \cdot Y_{DAC}} \epsilon_i \quad \ldots \sum_{i=2^N - Y_{DAC}+1}^{2^N} \epsilon_i \quad \ldots \right\}. \tag{3.20}$$

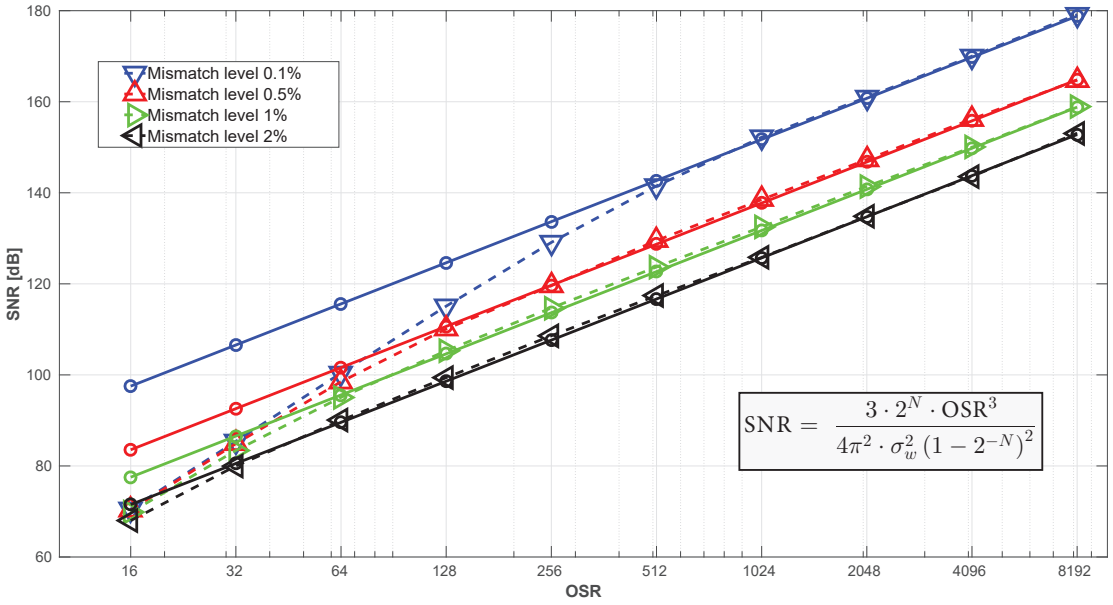
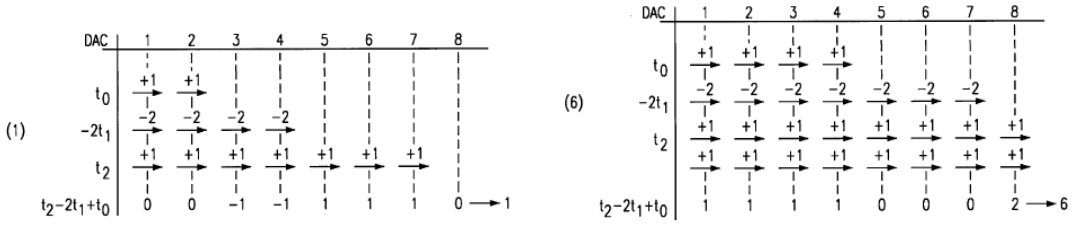


Figure 3.19: SNR as a function of the OSR and of the mismatch among unit elements when DWA is applied. The solid line represents the simulated results, while the dashed line represents the mathematical modeling.

From Equation (3.20) it results that the position of the tone is given by $f_{tone} = [\gcd(Y_{DAC}, 2^N)]/2^N \cdot f_s \cdot n$ with $n = 1, 2, 3....$ Imposing that the inter-modulation between tones generated by DWA and harmonics of the input signal falls outside the signal bandwidth we obtain:

$$\frac{f_s}{2^N} - \frac{f_s \cdot n}{2 \cdot \mathrm{OSR}} > \frac{f_s}{2 \cdot \mathrm{OSR}} \longrightarrow \mathrm{OSR} > \frac{2^N \cdot (n+1)}{2}. \tag{3.21}$$

Equation (3.21) points out that greater is the value of N, greater is the value of OSR needed to avoid the distortion generated by DWA. Moreover, by increasing N to big values, it can become necessary to use a segmented feedback path as in [42], with a significant drawback of a more complex hardware implementation. The fact that at low OSR the efficiency of DWA starts to degrade with respect to the nominal situation, namely the one that satisfies Equation (3.21), it is even more clear in Figure 3.19, where the dashed line represents the SNDR calculated from the simulated spectrum that includes the distortion term due to the harmonics generated by the algorithm, while the solid line represents the SNR of Equation (3.19). It is clear that the mathematical modeling is not adequate for low OSR value. In fact, in this situation, the power of the spurious tones due to the algorithm cyclicity is the dominant term limiting the SNDR. Conversely, the SNR calculated in Equation (3.19) only accounts for the noise floor the input signal harmonics were translated into by means of the DEM algorithm.
Several ways to overcome these degradations have been proposed. They are discussed next.



(a) (b)

Figure 3.20: Updating rule for a second-order DWA. The input sequence $1-6$ is considered respectively in (a) and (b).

3.3.4 DWA Second-Order (DWA2)

By changing the update rule is possible to obtain an arbitrary noise shaping. In Equation (3.18) it has been stated that the Z-transform mismatch error can be expressed as a function of a general transfer function $H(z)$ and the Integral Mismatch

$$E(z) = H(z) \cdot IM(I(z)). \tag{3.22}$$

For example, a second-order low-pass DEM technique can be found in [43,44]. For $H(z) = (1 - z^{-1})^2$ we obtain by the inverse Z-transform

$$\epsilon(k) = IM(I(k)) - 2 \cdot IM(I(k-1)) + IM(I(k-2)). \tag{3.23}$$

This behavior can be obtained in three steps:

1. Define three thermometric vectors t_0, t_1, t_2. Each vector has an index, respectively $I(k-2)$, $I(k-1)$ and $I(k)$, which represent the number of "ones" in the vector.

2. Values of $I(k-2)$ and $I(k-1)$ are well known from the previous cycle. The $I(k)$ index can be found rearranging the Equation (3.23) as

$$I(k) = y(k) + 2 \cdot I(k-1) - I(k-2), \tag{3.24}$$

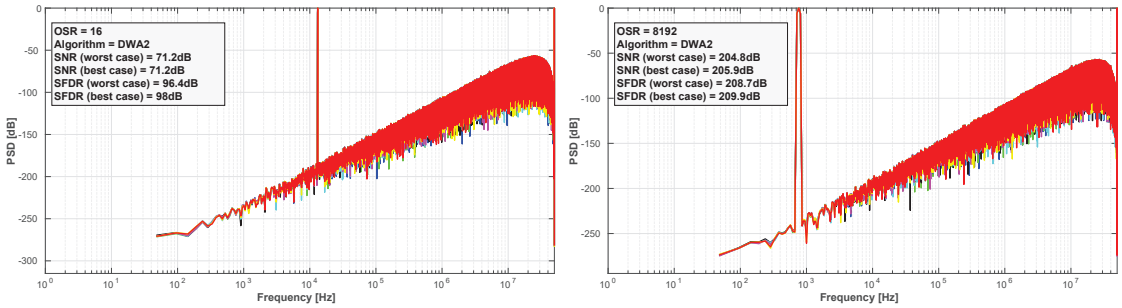
   where $y(k)$ is the output value of the modulator.

3. The DAC unit element control vector will be

$$CTRL = t_2 - 2 \cdot t_1 + t0 \tag{3.25}$$

   In the next cycle $I(k-2)_{new} = I(k-1)$ and $I(k-1)_{new} = I(k)$.

In Figure 3.20 an example of conversion in a second-order DWA is depicted. The first step is shown in Figure 3.20(a) with a conversion of $y(k) = 1$. Assuming an initial $I(k-2) = 2$ (t_0) and $I(k-1) = 4$ (t_1) Equation (3.24) yields $I(k) = 7$ (t_2). In Figure 3.20(a) t_0 is defined assigning to the first two elements the value $+1$, $-2t_1$ is defined assigning to the first four elements the value -2, which implies



(a) (b)

Figure 3.21: DWA2: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations.

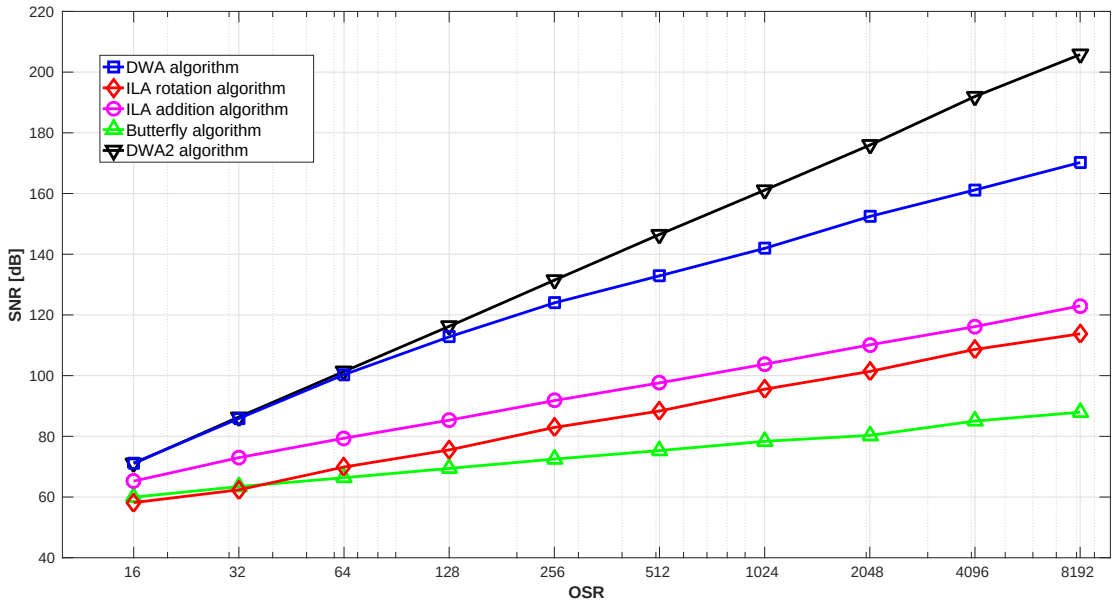


Figure 3.22: Comparison between common DEM algorithms in terms of SNDR as a function of the OSR.

a total value -8 and similarly it is defined the vector t_2. The sum of the tree vectors gives the thermometric code that controls the unit elements of the DAC. The thermometric code is realized assigning at each element the sum of the values in the column. For instance the first value is given by the sum of $+1$,-2 and $+1$ which is 0. In the following step $I(k-1)_{new} = I(k) = 7$ and $I(k)_{new} = 4$. In the following step a conversion of $y(k) = 6$ is considered and shown in Figure 3.20(b). From Equation (3.24) yields $I(k) = 16$. In the following step $I(k-1)_{new} = I(k) = 16$ and $I(k)_{new} = 7$.

In Figure 3.21 the efficiency of the second-order DWA is depicted. It is apparent that the DWA2 does not contain any harmonics for low OSR. Besides that, DWA2 offers better performance even at high OSR.

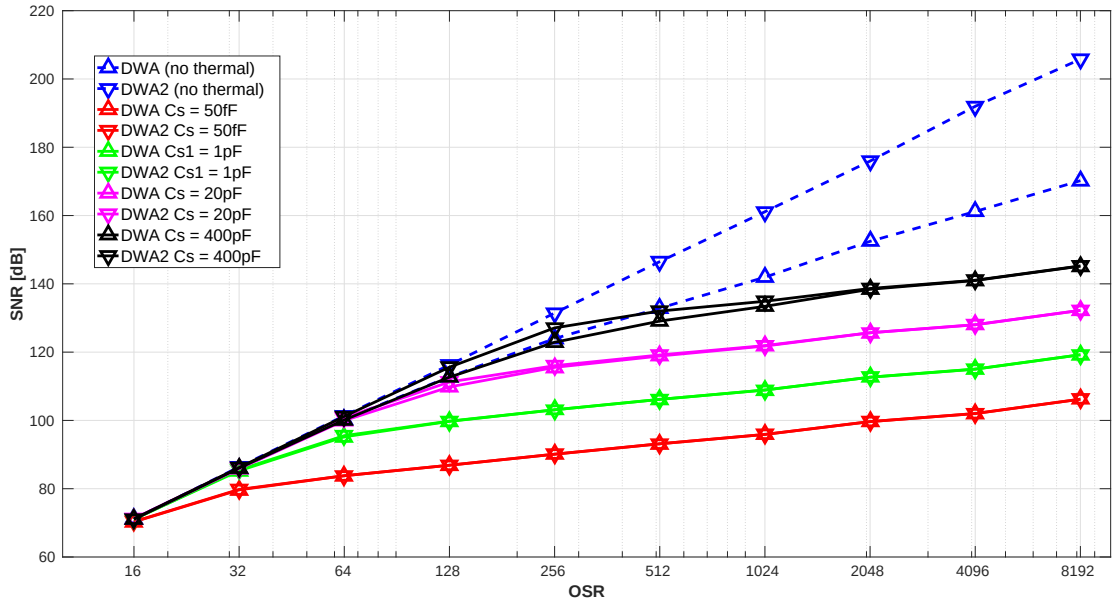


Figure 3.23: Comparison between DWA and DWA2 in presence of thermal noise. Several sizes of sampling capacitors are considered.

This is even more clear in Figure 3.22. In fact the SNDR guaranteed by the second-order DWA is always greater than the SNDR of the other algorithms. This SNDR is extremely close to the curve of an ideal $\Sigma\Delta$ converter. For low OSR the SNDR of DWA2 is similar to the one of DWA, since at low OSR the first-order shaping and the second-order shaping are similar. However, the SFDR of DWA2 is significantly better than the one of DWA.
Although the second-order DWA offers better performance with respect to the first-order one, it is worth to take into consideration two important points in order to select the most appropriate DEM algorithm. First of all, the DEM performance has to be evaluated in the context of the whole ADC: as explained in Chapter 2 in the conversion band the thermal noise floor will largely dominate the shaped quantization noise, as well as the noise resulting from the DEM averaging. Therefore the thermal noise will actually hide the second-order performance gain. This is clear in Figure 3.23. Only when the size of the sampling capacitor reaches values such that the thermal noise level is lower than the quantization noise of DWA, but greater of quantization noise of DWA2, there is an advantage in using the second-order DWA. However, such values are impossible to be realized in an integrated circuit, for instance 400pF. Furthermore, the SNR of DWA2 is greater than the SNR of DWA only for a small set of OSR values. Otherwise, the SNR of the two algorithms coincides.
The second important point to consider is the hardware implementation, as it will be discussed in Chapter 4.

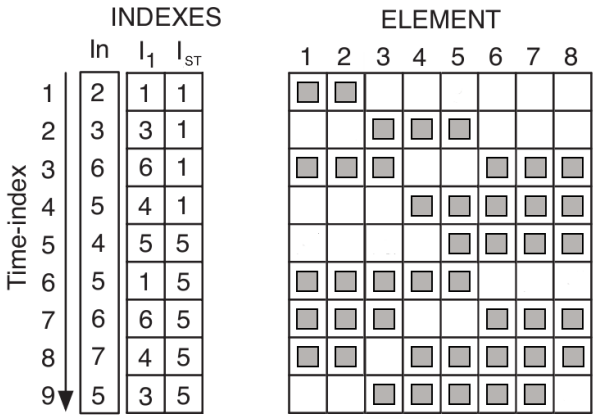
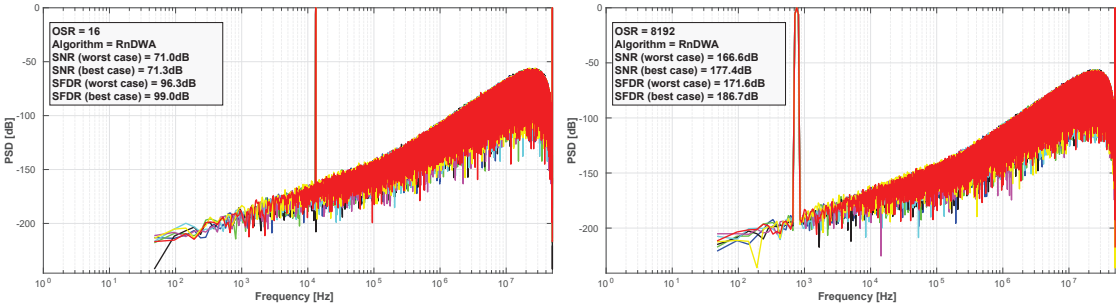


Figure 3.24: Operation principle of the rotation of RnDWA. The shaded boxex indicate which unit elements contribute positive for a 3 bit DAC employing RnDWA.



(a) (b)

Figure 3.25: RnDWA: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations.

3.3.5 Randomized DWA (RnDWA)

Another possibility in order to avoid the in-band distortion for low OSR is described in [45] with Randomized Data Weighted Averaging (RnDWA). The distortion will be masked by the white noise introduced by randomization. This is accompanied with some increase in in-band noise and lower SNR. The main idea of this algorithm is that no unit element should be re-selected before all others have been selected. This algorithm adds randomization to the cyclic process of DWA.
In Figure 3.24 it is described RnDWA in a 8 elements DAC: when DWA ends a complete rotation a random new start point is selected, in this example $I = 5$ and the pointer I_1 is increased to this location (without choosing the units in between). The new starting index I_{ST} is updated to the new value given by randomization. We continue selecting units until we reach this same start point again. Montecarlo simulations of RnDWA are presented in Figure 3.25 and, as apparent, the tones generated by DWA are masked by increasing of the noise floor. The noise shaping behavior is preserved.

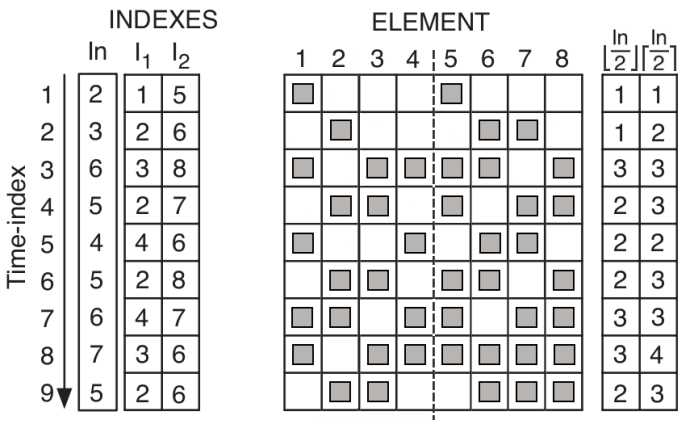
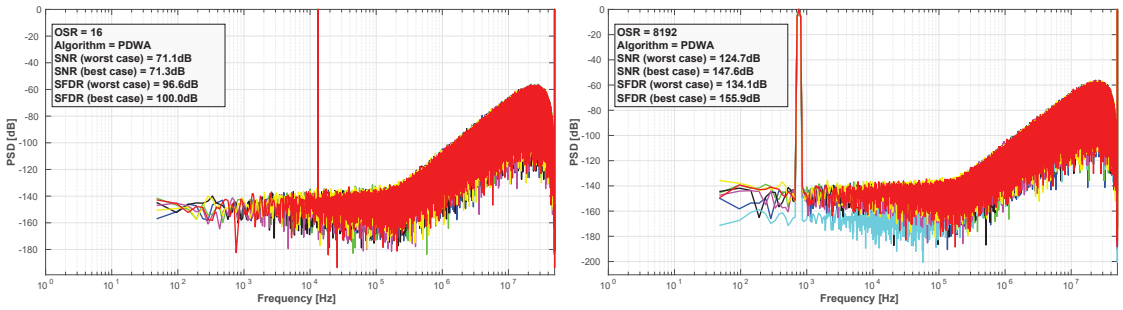


Figure 3.26: Operation principle of the rotation of PDWA. The shaded boxex indicate which unit elements contribute positive for a three-bit DAC employing PDWA.



(a) (b)

Figure 3.27: PDWA: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations.

3.3.6 Partitioned DWA (PDWA)

Partitioned Data Weighted Averaging (PDWA) is another approach to avoid the tones generated in DWA [46]. The principle of this algorithm is related with Equation (3.21): if the number of elements is reduced, also the least value of OSR, such that the inter-modulation between tones generated by DWA and harmonics of the input signal will not fall in the signal bandwidth, is reduced. The DAC is divided in two parts which both use DWA. The input of DAC is divided in two parts. The quotient, or in other words the floor value of the input divided by two, is the input to the first part, while the sum of the quotient and the remainder, the ceiling value of the input divided by two, is the input of the second part. In Figure 3.26 the indexes I_1 and I_2 are updated like in standard DWA but with half elements. In contrast to DWA the DAC error is no longer first-order noise-shaped and so it performs significantly worse than the previous algorithm, as depicted in Figure 3.27.

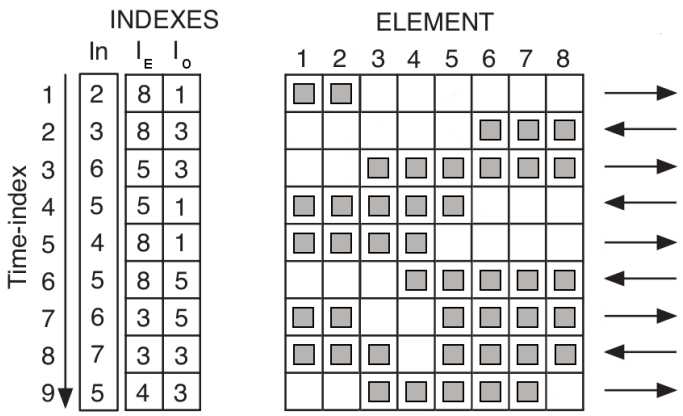
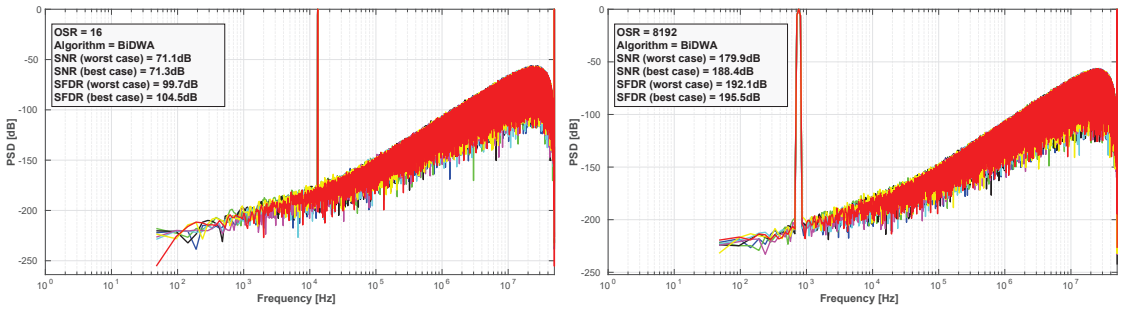


Figure 3.28: Operation principle of the rotation of BiDWA. The shaded boxex indicate which unit elements contribute positive for a 3 bit DAC employing BiDWA.



(a) (b)

Figure 3.29: BiDWA: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations.

3.3.7 Bi-Directional DWA (BiDWA)

Instead of adding randomization we can break the cyclic nature of DWA in a deterministic way. Bi-Directional Data Weighted Averaging (BiDWA) is proposed in [47]. A practical example of BiDWA is described in Figure 3.28. Two pointers, I_E for the even phases of the clock and I_O for the odd phases of the clock, are used. While during the odd clock cycles the elements are selected like in standard DWA, during the even clock cycles the selection logic is reversed in the other direction. The pointer logic update is described in (3.26) distinguishing the even, I_E, from the odd phases, I_O:

$$\begin{cases} I_O(k+1) = (I_O(k-1) + y(k-1)) \bmod 2^N \\ I_E(k+2) = (I_E(k) - y(k)) \bmod 2^N. \end{cases} \tag{3.26}$$

	SNR (min)	SNR (max)	SFDR (min)	SFDR (max)
Butterfly	70.1	71.1	95.1	99.4
ILA (rotation)	68.9	71.2	95.9	98.6
ILA (addition)	71.0	71.2	94.6	99.3
DWA	71.1	71.3	89.1	94.9
DWA2	71.2	71.2	96.4	98
RnDWA	71.0	71.3	96.3	99
PDWA	71.1	71.3	96.6	100
BiDWA	**71.1**	**71.3**	**99.7**	**104.5**

Table 3.2: Comparison of the main DEM algorithms at OSR = 16 in terms of SNR and SFDR.

It can be analytically demonstrated that also BiDWA takes advantage of a first-order noise shaping behavior, that is

$$H(z) = (1 - z^{-2}). \tag{3.27}$$

Equation (3.27) at low frequencies can be reconducted with the Taylor series to the first order noise shaping. However, the two indexes break the cyclic behavior of DWA, reducing therefore the spurious tones in the signal bandwidth. Simulations of Figure 3.29 proves that the BiDWA preserves the first-order noise shaping.
Table 3.2 proves that BiDWA is the best algorithm to be used in low OSR applications. This is motivated by the fact that the nature of the BiDWA relies on a deterministic approach, instead of a randomized selection as in the RnDWA. This implies that BiDWA is a more robust modified version of DWA than the other solutions. However, intuitively, the hardware implementation of BiDWA is more complex than the DWA implementation, since the logic should be able to shift in two directions. Furthermore two indexes are needed in BiDWA, instead of a single index as in DWA. This difference in terms of hardware implementation hides another important figure of merit for the DEM algorithm, which is the time delay introduced by DEM. The influence of time delay in a FF $\Sigma\Delta$ modulator will be explained in Chapter 4, when the circuital implementation of the modulator presented in this thesis will be described. Since the interest of this work is on wide-band $\Sigma\Delta$ modulator, the behavior of DEM algorithms at low OSR takes a great importance. However, when moving to high OSR, it has been observed that the second-order DWA is out-performing the other algorithms, as apparent in Table 3.3. It is worth to notice in Table 3.3 that again the BiDWA approach shows a small variance in the SFDR distribution if compared with the other algorithms. Also in this case, as already stated in Chapter 3.3.4, the circuital implementation is the most important drawback.
All the algorithms described until now solves the DAC non-linearity in a digital

	SNR (min)	SNR (max)	SFDR (min)	SFDR (max)
Butterfly	104.5	118.0	112.6	126.8
ILA (rotation)	127.8	145.7	135.6	155.7
ILA (addition)	139.5	150.2	147.2	160.8
DWA	187.5	194.0	192.5	200.3
DWA2	**204.8**	**205.9**	**208.7**	**209.9**
RnDWA	166.6	177.4	171.6	186.7
PDWA	124.7	147.6	134.1	155.9
BiDWA	179.8	188.4	192.1	195.5

Table 3.3: Comparison of the main DEM algorithms at OSR = 8192 in terms of SNR and SFDR.

way, which is preferable for the designers since it takes advantages of the fast scaled CMOS technology, make it possible to exploit the multi-bit quantization in a FF $\Sigma\Delta$ modulator. In the following part the system-level description of the design of this thesis will be presented.

3.4 System-Level Design

In Figure 3.30 the topology used for this design is shown. The supply voltage for this design is $V_{DD} = 1.2$V in a 65nm CMOS technology. As apparent from Figure 3.30 a modulator order $L = 2$ is chosen. This is due to stability problems, since, as already explained in Chapter 2.2.5, the second-order modulator is inherently stable, while a greater order would lead to instability for high input voltage. Moreover, since a multi-bit quantizer is used, increasing L will not give us advantages [48]. This is due to the fact that the noise floor is given by thermal noise and, thanks to the multi-bit quantizer, the thermal noise is several decibels higher than the quantization noise. For this reason having third-order shaping will not increase in a sensible way the resolution of the modulator. If a third-order modulator $L = 3$ is chosen, the same resolution is achieved, but with a higher complexity, higher power consumption and stability's problems.
With the aid of a behavioral simulator developed in *MATLAB/Simulink* that accounts for the main circuit non-idealities, namely finite gain and bandwidth and slew-rate of the amplifiers, thermal noise from the switches and the amplifiers, clock jitter and the mismatch between the sampling capacitors, a second-order modulator has been designed using the architecture of Figure 3.30.

The sampling frequency is $f_s = 50$MHz with an OSR = 50. This choice was made in order to realize a relatively wide-band $\Sigma\Delta$ modulator, namely

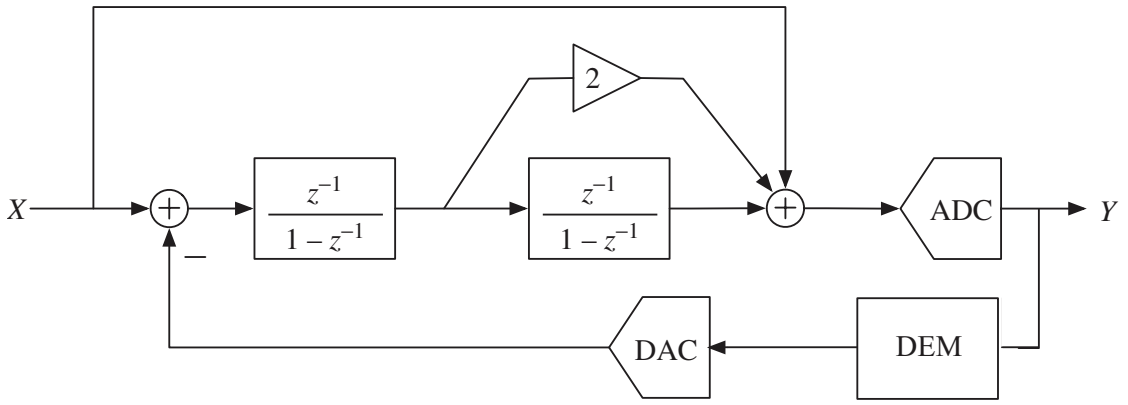


Figure 3.30: The topology of the ΣΔ modulator used for this design.

$$B_w = \frac{f_s}{2\text{OSR}} = 500\text{kHz}, \tag{3.28}$$

which is a large conversion bandwidth for a ΣΔ topology. In fact, usually, the ΣΔ ADCs signal bandwidth is not greater than 100kHz [49].
The OSR is a key modulator parameter. In fact, the fraction of the switches thermal noise falling into the conversion bandwidth is given by

$$P_{thermal} \propto \frac{kT}{C_s \cdot \text{OSR}} \tag{3.29}$$

where C_S is the value of the capacitor in the integrator input branch. In a properly designed ΣΔ converter the thermal noise is the dominant noise source. With OSR = 50, considering the need to keep the size of the capacitor C_S small enough to keep low the power consumption, but in order to meet a DR of at least 90dB with a 1.2V supply voltage, a sampling capacitor $C_S = 600\text{fF}$ is chosen.
In order to completely characterize the overall modulator, the number of bits of the internal quantizer must be chosen. In the following a strategy with the aim of a power consumption minimization is described in order to choose the number of bits of the embedded quantizer.

3.4.1 Power Consumption Minimization

The most important components used in the ΣΔ ADC are comparators and amplifiers [50]. The impact of these components in terms of power consumption will now be discussed.
In particular a minimum in the total power consumption can be found with respect to N, the number of bit of internal quantizer. In fact, increasing the number of bits N leads to a smaller input swing of the integrators, which implies a reduction of the specifications of the amplifiers as DC-gain, SR and GBW. However increasing N leads to an increment of the power consumption of the internal quantizer.

3.4.2 Quantizer Power Consumption

Defining P_C the power consumed by a single comparator in the quantizer it is possible to evaluate the power of the overall quantizer (P_Q) as

$$P_Q = P_C \cdot \left(2^N - 1\right). \tag{3.30}$$

The speed of the comparator is controlled by its time constant $\tau_c = C_{LC}/g_m$, where C_{LC} is the load capacitor of the comparator and g_m is the transconductance of the comparator.
Since the comparator must be able to detect a voltage of $V_{fs}/2^N$ in a decision time T_d then

$$\frac{V_{fs}}{2^N} \cdot e^{(T_d/\tau_c)} = V_{fs}. \tag{3.31}$$

Assuming $T_d = 1/2f_s$ (where f_s is the oversampling frequency) it is possible to evaluate the minimum g_m and, therefore, the minimum supply current I_C, recalling that $I_C = g_m V_{eff}$ with V_{eff} essentially a technology's parameter.
After some calculation the P_C is characterized as

$$P_C = V_{fs} \cdot [2N \cdot \ln(2) \cdot f_s C_{LC} V_{eff}]. \tag{3.32}$$

According to (3.30) and (3.32)

$$P_Q = V_{fs} \cdot [2N \cdot \ln(2) \cdot f_s C_{LC} V_{eff}] \cdot \left(2^N - 1\right). \tag{3.33}$$

3.4.3 Amplifier Power Consumption

Thanks to Noise-Shaping and also to a smaller input amplitude, the power consumption of the amplifiers is mainly determined by the first amplifier in the cascade of SC integrators which realize the loop of the modulator. For this reason in the following analysis the power consumption of the other amplifiers is neglected. Furthermore the gain of the OTA is assumed to be adequate to neglect the gain errors with a single stage OTA, otherwise an additional supply current should be required to ensure a good phase margin (PM) in a two stage OTA with Miller capacitor. The power dissipation of the amplifier can be expressed by estimating the supply current under the constraint of the SC integrator settling $T_{ex} + T_{ls} = T_s$, where T_{ex} is the exponential settling time, T_{ls} is the time of linear evolution due slew-rate and T_s is the total available time. Considering the time constant of the amplifier $\tau_a = C_{LA}/(g_m\beta)$, where β is the feedback factor of the OTA, as defined in Equation (2.30) and for this design is $\beta = 0.43$, ϵ_D is the dynamic error of the OTA integrator, C_{LA} is the total load capacitor of the amplifier and g_m is the transconductance of the OTA we obtain

$$T_s = \frac{g_m r_0 \beta}{1 + g_m r_0 \beta} \cdot \frac{V_{in}}{\mathrm{SR}} - \tau_a \left[1 + \ln(\epsilon_D)\right]. \tag{3.34}$$

By substituting $T_s = 1/2f_s$, $\mathrm{SR} = I_A/C_{LA}$ into Equation (3.34) and recalling that the input of the amplifier in the feed-forward topology is given by the quantization

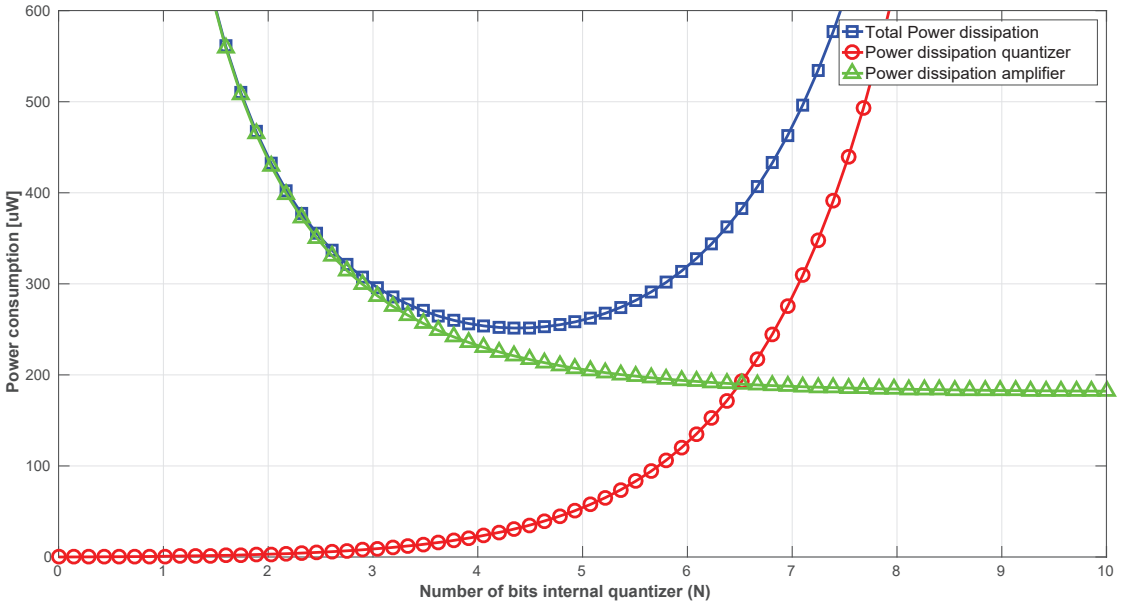


Figure 3.31: The power consumption in the ΣΔ modulator with respect to the number of bits of the internal quantizer.

error $\Delta = V_{fs}/(2^N - 1)$ and solving for I_A, the power dissipation can be expressed, using $P_A = I_A V_{DD} = I_A V_{fs}$, as

$$P_A = 2f_s \cdot V_{fs} \left[\frac{V_{fs}}{2^N - 1} \cdot C_{LA} - \frac{2V_{eff} \cdot C_{LA}}{\beta} \left(1 + \ln(\epsilon_D)\right) \right]. \tag{3.35}$$

The analysis made on the power consumption in this Chapter implies some results: V_{eff} is a very important parameter and it favors deep-submicrometer MOS process. In fact scaled technologies bring lower V_{eff} as well as inherently smaller minimum capacitors, which also helps in lower power dissipation. Furthermore both Equations (3.32) and (3.35) are function of the number of bits of the internal quantizer N. Using the parameters estimated with the behavioral simulations in *MATLAB* the total power consumption with respect to N has been plotted in Figure 3.31.
Figure 3.31 highlights the existence of a minimum in the total power consumption and suggests an optimal value for N. With the parameters of the design proposed in this thesis, an optimal value for the number of bits of internal quantizer has been found between $N = 4$ and $N = 5$. After further analysis the solution with a 5 bit embedded quantizer has been chosen. This choice is motivated by the need to simplify the design of the first integrator in terms of the minimum specifications to make negligible the effects of non-idealities.
It is apparent in Figure 3.32 that with a $N = 5$ embedded quantizer a lower gain of the first integrator is needed, with respect to the 4 bit case. Furthermore, as depicted in Figure 3.33, the bias current needed to neglect SR and GBW non-ideal effects is clearly reduced in the 5 bit case.
However it should be taken into account that the number of bits of internal quantizer can lead into difficulties in the digital algorithm needed to remove the non-linearity

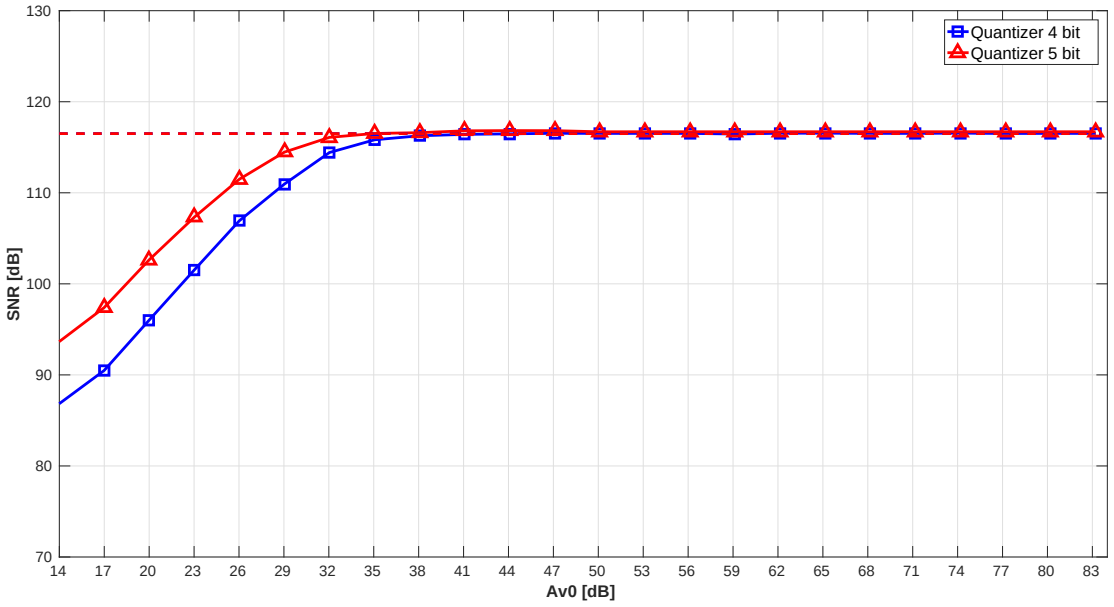


Figure 3.32: SNR as a function of the gain of the first integrator in a FF topology with a 4 bit embedded quantizer and with a 5 bit embedded quantizer. Dashed line represents the ideal case.

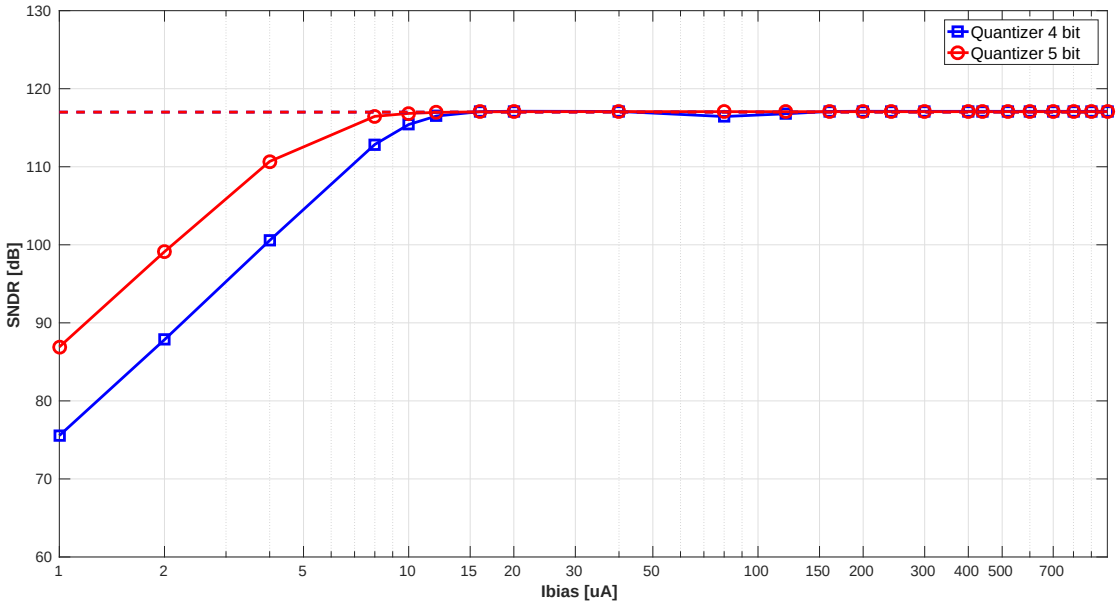


Figure 3.33: SNR as a function of the bias current I_{bias} of the first integrator in a FF topology with a 4 bit embedded quantizer and with a 5 bit embedded quantizer. Dashed line represents the ideal case.

of the DAC. In fact, as already described previously with Equation (3.21), increasing the number of bits of internal quantizer, leads to a higher minimum value of OSR in order to avoid the tonal behavior of DWA. In the following section a new DEM

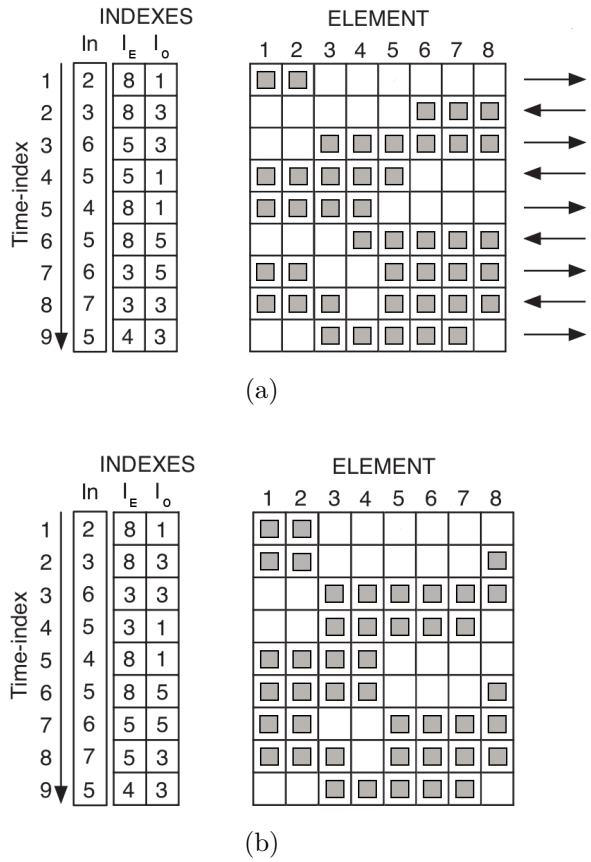


Figure 3.34: Operation principle of the rotation of (a) BiDWA and (b) NewDWA. The shaded boxex indicate which unit elements contribute positive for a 3 bit DAC.

algorithm that solves the DWA harmonic issue is presented, with the efficiency of BiDWA but with an easier hardware implementation.

3.4.4 Proposed DWA (NewDWA)

As previously stated, in Table 3.2, the BiDWA is one of the most promising algorithm in terms of mismatch canceling.
The use of BiDWA is however limited because its hardware implementation is not efficient in terms of power and area consumption and may often result too slow, as it will be highlighted in Chapter 4.
The proposed algorithm is obtained with the aim of obtaining the same transfer function of the classical BiDWA, that can be expressed as

$$H_{BiDWA}(z) = (1 - z^{-2}). \tag{3.36}$$

In Figure 3.34(a) the selection scheme of BiDWA is recalled. Considering the odd phases, under the hypotesis that $I(k-2) < I(k) - 1$, the output of the BiDWA for a general input $y(k)$ can be written as follows:

$$\begin{aligned} y_{DAC}(k) &= \sum_{i=I(k-2)}^{I(k)-1} U_i = \sum_{i=I(k-2)}^{I(k)-1} (U_{mean} + \delta U_i) \\ &= U_{mean} \cdot y(k) + \sum_{i=I(k-2)}^{I(k)-1} \delta U_i \\ &= U_{mean} \cdot y(k) + \epsilon(k). \end{aligned} \tag{3.37}$$

Equation (3.37) can be easily translated into

$$\begin{aligned} \epsilon(k) &= \sum_{i=I(k-2)}^{I(k)-1} U_i - y(k) \cdot U_{mean} \\ &= \sum_{i=I(k-2)}^{I(k)-1} U_i - [I(k) - 1 - I(k-2) + 1]\, U_{mean} \\ &= \sum_{i=1}^{I(k)-1} U_i - [I(k) - 1] U_{mean} - \sum_{i=1}^{I(k-2)-1} U_i + [I(k-2) - 1] U_{mean}. \end{aligned} \tag{3.38}$$

Therefore, as in DWA, using the definition of Integral Mismatch function $IM(I(k))$ of Equation (3.16) it is possible to modify Equation (3.38) as

$$\epsilon(k) = IM(I(k)) - IM(I(k-2)) \tag{3.39}$$

which is, in the Z-domain

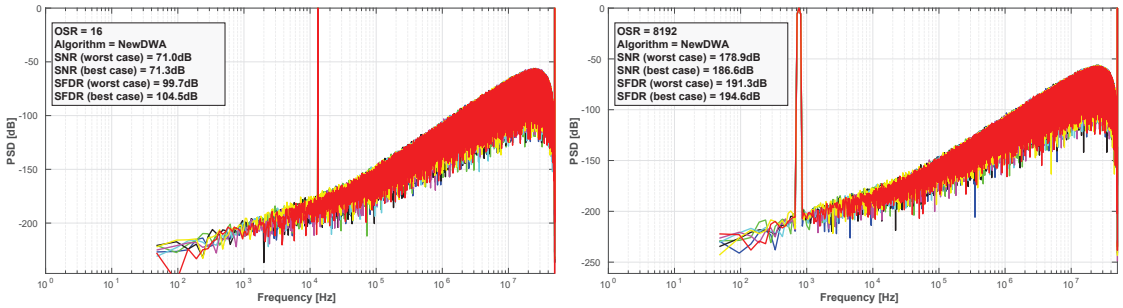
$$E(z) = (1 - z^{-2}) IM(I). \tag{3.40}$$

Let's now consider the even phases, in which the direction rotation is reversed. Under the hypotesis that $I(k+1) < I(k-1) - 1$, the output of the BiDWA $y_{DAC}(k+1)$ for a general input $y(k+1)$ can be written as follows:

$$\begin{aligned} y_{DAC}(k+1) &= \sum_{i=I(k+1)}^{I(k-1)-1} U_i = \sum_{i=I(k+1)}^{I(k-1)-1} (U_{mean} + \delta U_i) \\ &= U_{mean} \cdot y(k+1) + \sum_{i=I(k+1)}^{I(k-1)-1} \delta U_i \\ &= U_{mean} \cdot y(k+1) + \epsilon(k+1). \end{aligned} \tag{3.41}$$

Equation (3.41) can be modified with a variable substitution, namely $k + 1 = t$, which yields

$$\begin{aligned} y_{DAC}(t) &= \sum_{i=I(t)}^{I(t-2)-1} U_i = \sum_{i=I(t)}^{I(t-2)-1} (U_{mean} + \delta U_i) = \\ &= U_{mean} \cdot y(t) + \sum_{i=I(t)}^{I(t-2)-1} \delta U_i = \\ &= U_{mean} \cdot y(t) + \epsilon(t). \end{aligned} \tag{3.42}$$



(a) (b)

Figure 3.35: NewDWA: Montecarlo simulation for (a) low OSR case and for (b) high OSR case in a second-order FF modulator. A mismatch of $\sigma_w = 0.1\%$ is considered for these simulations.

Equation (3.42) can be easily translated into

$$\begin{aligned}\epsilon(t) &= \sum_{i=I(t)}^{I(t-2)-1} U_i - y(t)\cdot U_{mean} \\ &= \sum_{i=I(t)}^{I(t-2)-1} U_i - [I(t-2)-1-I(t)+1]\,U_{mean} \\ &= \sum_{i=1}^{I(t-2)-1} U_i - [I(t-2)-1]U_{mean} - \sum_{i=1}^{I(t)-1} U_i + [I(t)-1]U_{mean}.\end{aligned} \tag{3.43}$$

Therefore, using the definition of Integral Mismatch function $IM(I(k))$ of Equation (3.16) it is possible to modify Equation (3.43) as

$$\epsilon(t) = IM(I(t-2)) - IM(I(t)) \tag{3.44}$$

which is, in the Z-domain

$$E(z) = (z^{-2}-1)IM(I) = -(1-z^{-2})IM(I). \tag{3.45}$$

Equation (3.45) proves that the rotation in the opposite direction does not change the absolute value of the transfer function, therefore it does not change the power of shaping the mismatch error, as apparent in Equation (3.11). This implies that the change of rotation does not give any real advantage. In fact the only real necessary condition in order to obtain the transfer function $(1-z^{-1})^2$ is to have concordant direction of rotation between phase k and phase $k+2$, for all k.
In Figure 3.34(b) an example of evolution during time of the two pointers and the corresponding set of the selected elements in the DAC is reported. Two indexes, I_E and I_O, are stored in two separate registers. In the even phases the rotation is controlled by the actual value I_E, which is updated for the next even phase with the actual input value, while I_O remains unchanged. In the odd phases the rotation is controlled by the actual value of I_O, which is updated for the next odd phase with the actual input value, while I_E remains unchanged.

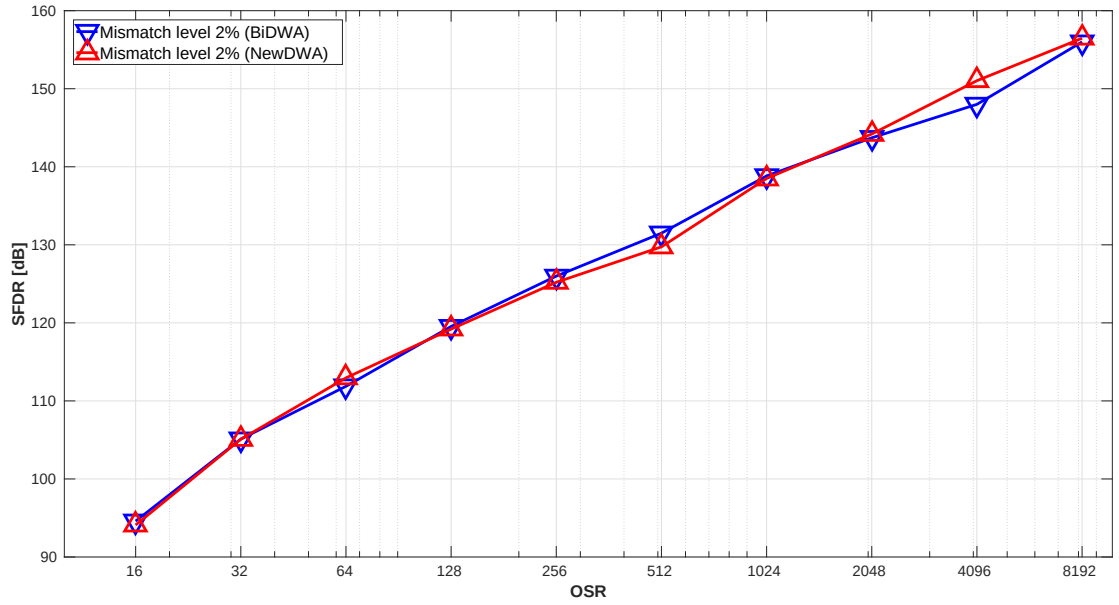


Figure 3.36: SFDR of BiDWA and NewDWA for a FF $\Sigma\Delta$ second-order modulator as a function of the OSR. A $\sigma_w = 2\%$ is considered for this simulation.

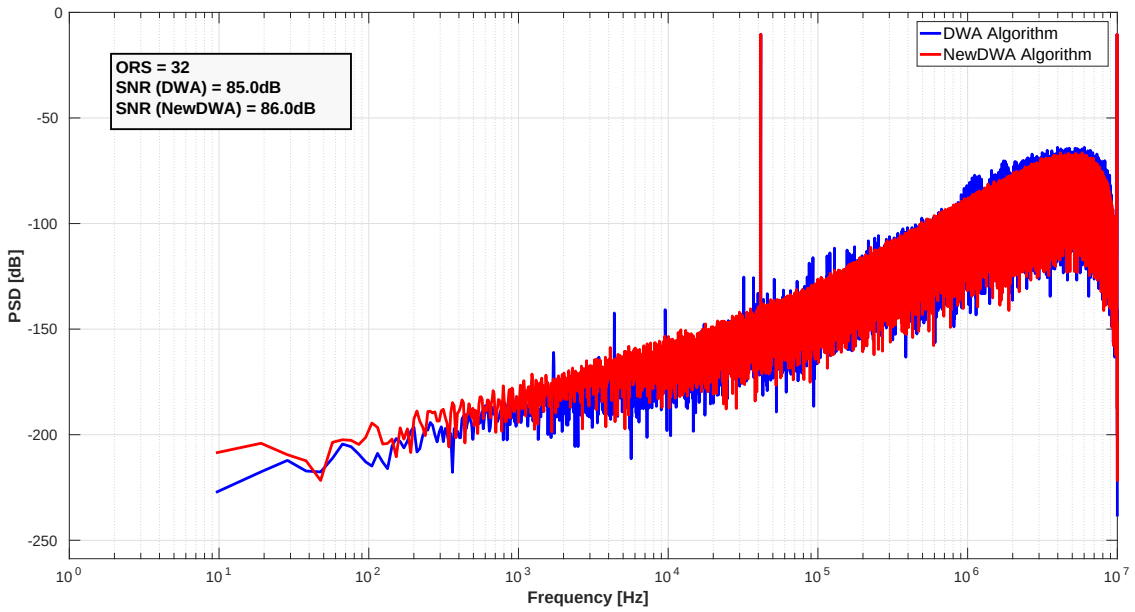


Figure 3.37: Output spectra of a FF $\Sigma\Delta$ second-order modulator with a 5 bit internal quantizer when DWA is applied and when NewDWA is applied.

Intuitively, the implementation of the DEM as expressed in Figure 3.34 can be realized in a simpler way with respect to the original BiDWA, because the rotation in two opposite directions is no more required. However, the NewDWA still requires to use two pointers to be used alternatively. As it will be clear in Chapter 4, this is

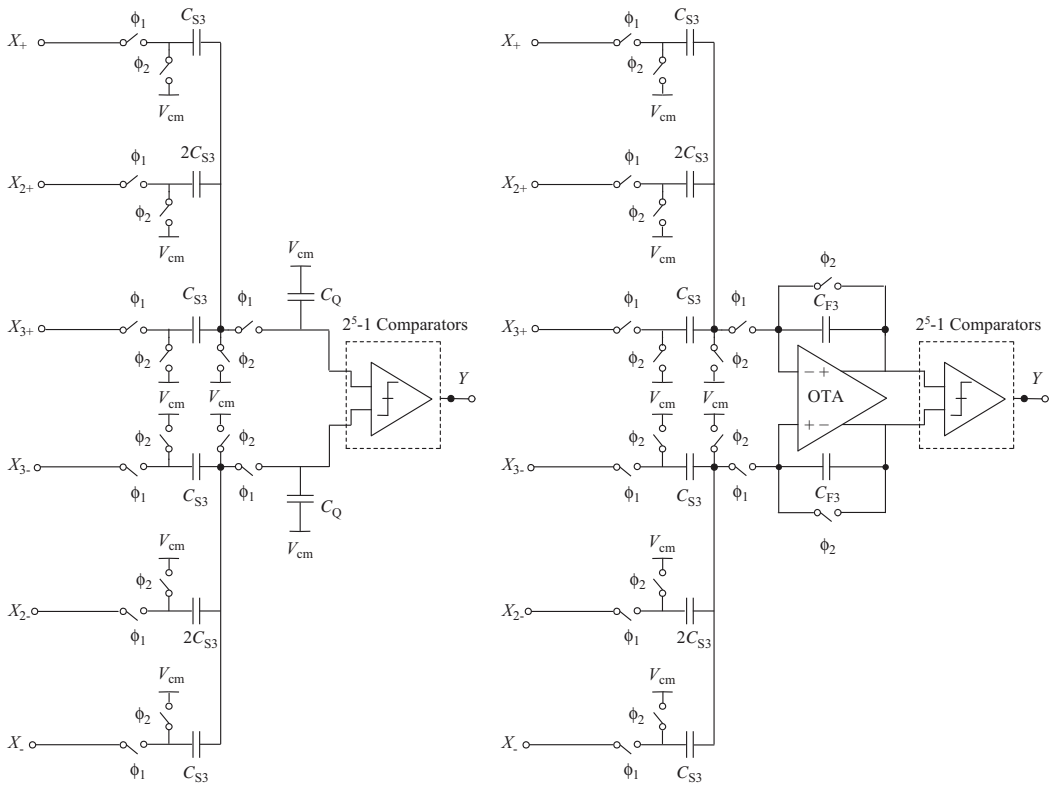


Figure 3.38: Analog Adder implementation: (a) Summing using Charge Sharing, (b) Summing using an Active Adder

not a real problem.
In Figure 3.35 the Montecarlo simulations of the NewDWA with a 5 bit internal quantizer are shown. It is apparent, from a comparison with the simulations of BiDWA, as the one depicted in Figure 3.29, that the efficiency of the two algorithms is the same. This fact was to be expected considering that the two algorithms share the same mismatch transfer function. This is even more clear by looking at the result of Figure 3.39. In fact it is apparent that the SFDR for these two algorithms is the same, regardless of the OSR, proving again the same efficiency of the two algorithms.
The efficiency of NewDWA in terms of removing the tonal behavior of DWA is shown in Figure 3.37.

3.4.5 Analog Adder

The architecture of Figure 3.30, besides the integrator and the comparator, has the need of an element able to sum all the input branches input signals before the quantizer, namely the input signal and the output of the two integrators. Conventionally there are two ways to implement the required summing function [51].
The first possibility is to generate the sum signal using charge sharing. This

	C_{S1_i}	C_{F1}	C_{S2}	C_{F2}	C_{S3}	C_{F3}
Capacitor Size	20fF	600fF	100fF	100fF	50fF	50fF

Table 3.4: Sizing of the capacitors of the proposed design.

approach is shown in Figure 3.38(a). Although this approach does not increase the overall power consumption, it has several drawbacks. First, the comparator input signal is attenuated, which makes it more vulnerable to the comparator offset voltages. In fact the input of the quantizer is given by

$$X_q = \frac{X + 2X_2 + X_3 - V_{ref}}{3}. \tag{3.46}$$

Since three input signals are summed, the input signal of the quantizer is attenuated by 3×. In order to maintain the quantizer monotonicity the comparator must make the correct decision for a $\Delta/2$ input signal in the presence of a comparator offset voltage:

$$\frac{\frac{\Delta}{2}}{3} - V_{os} \geq 0 \implies V_{os} \leq \frac{\Delta}{6}. \tag{3.47}$$

From Equation (3.47) it is determined that for a 5 bit quantizer with a supply voltage of 1.2V in deep-sub-micron CMOS, the comparator offset voltage must be less than 6mV. This stringent offset requirement necessitates the use of offset cancellation techniques with an attendant power penalty. Moreover, with this solution, the first and the second integrator, during their integration phase, have to drive the input capacitor of the 31 quantizers. This substantial load capacitance requires the use of relatively large power consumption in the first integrator stage. The second possibility is to use a switched-capacitor amplifier to sum the three signals, as in Figure 3.38(b). This adds power consumption and design complexity to the ADC. Moreover, since this amplifier has to process the input signal X, a rail-to-rail output stage has to been designed.
Both the solutions were assessed and it was observed that the solution with the analog adder requires a total power consumption lower than the solution based on charge sharing. In fact, the charge sharing solution increases the power consumption of the first integrator and of the comparator. Furthermore, the solution based on charge sharing is not reliable since the charge-sharing effect is not a phenomenon easy to control, on the contrary it is usually an undesirable signal integrity phenomenon. Moreover, has it will be shown in the followings, the requirements of the adder amplifier does not require to design a two-stage Miller OTA, therefore an efficient solution in terms of power-consumption can be chosen.

3.4.6 OTAs Requirements

In Figure 3.39 the circuit used for this design is depicted. The capacitors have been sized in order to achieve the −94dB floor noise requirements. The size of the capacitors is given in Table 3.4.

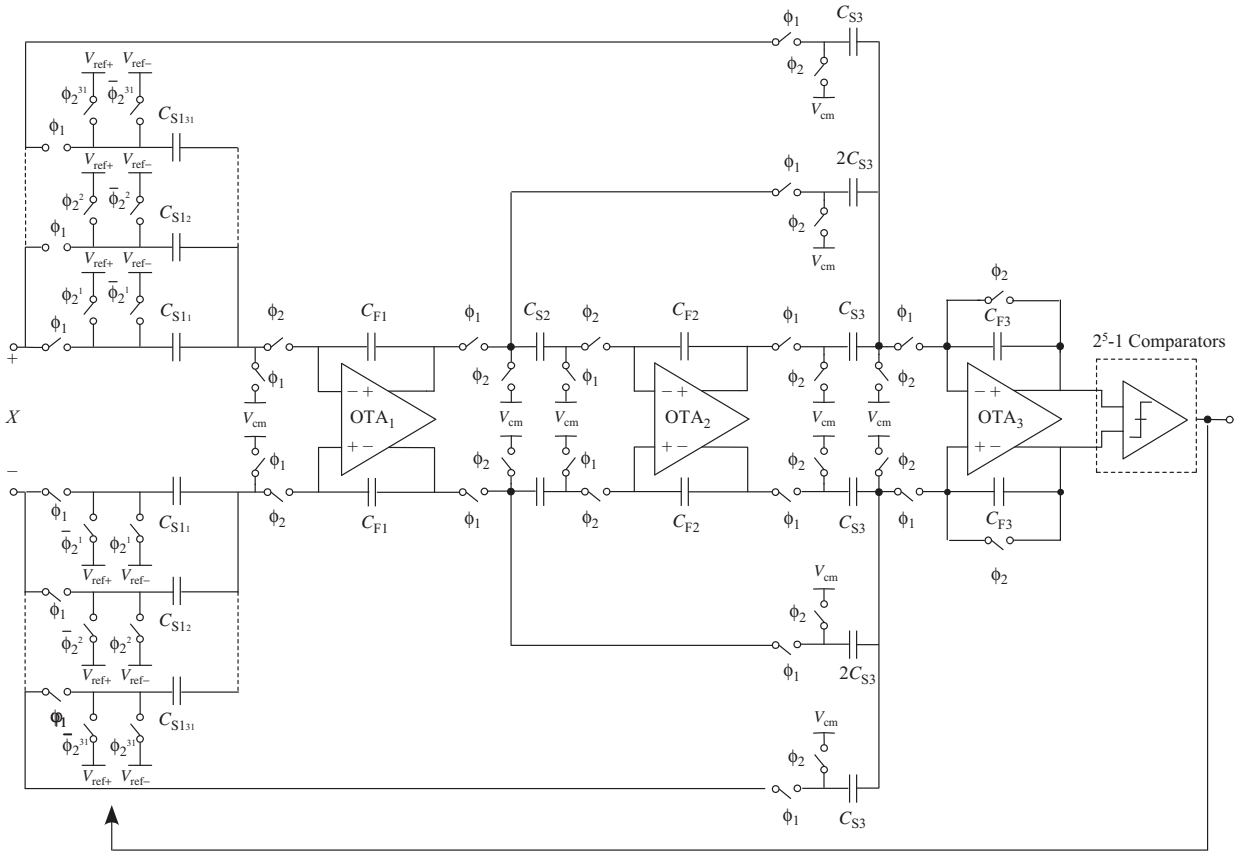


Figure 3.39: The ΣΔ modulator circuit used for this design.

The sampling capacitor of the first integrator has been splitted into 31 capacitors C_{S1_i}, with $i = 1, 2, ...31$, which can be connected separately to either V_{ref+} or V_{ref-}. This allows the implementation of the multi-bit feedback without additional capacitances, thereby avoiding additional kT/C noise and capacitive loading of the integrator. Notice that the power consumption remains the same as for a single bit implementation with a sampling capacitor $\sum_{i=1}^{31} C_{S1_i} = C_S$ and also the die size is comparable. Although this topology imposes tough requirements on the reference buffers, this implementation is preferred due to the good power and settling characteristics. Moreover, since the use of each unit capacitor can be directly controlled, this implementation is very well suited for dynamic element matching techniques.

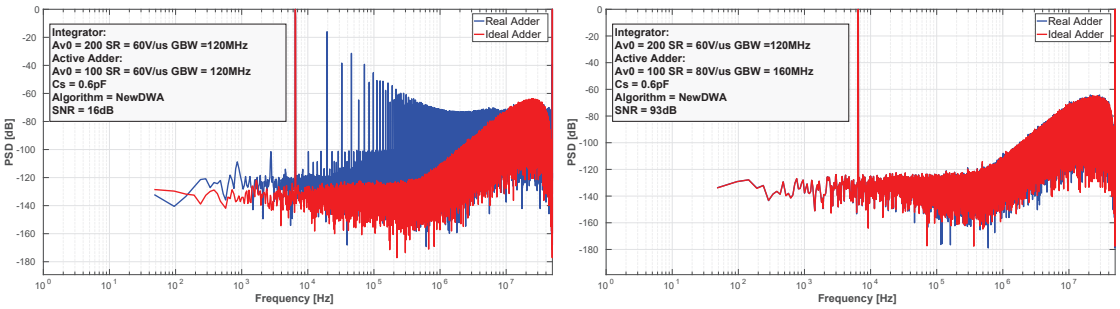
The size of the capacitors has been minimized in order to have a low power consumption. The size of the capacitor of the first integrator has been chosen in order to meet the noise requirements, while the other capacitors can be chosen of smaller size, since the effect of the second integrator and of the analog adder on the thermal noise floor is reduced by respectively a first-order and a second-order noise-shaping.

The specifications of the three OTAs, namely the two integrators and the analog adder, have been summarized in Table 3.5.

It is worth to notice that the specifications of the amplifier which realizes the

	First Integrator	Second Integrator	Adder
A_v	46dB	40dB	38dB
Output swing	$V_{fs}/20$	$V_{fs}/40$	V_{fs}
GBW	120MHz	90MHz	160MHz
SR	60V/μs	40V/μs	80V/μs

Table 3.5: Minimum specifications of the analog blocks of the modulator.



(a) (b)

Figure 3.40: Output spectrum of second-order FF $\Sigma\Delta$ modulator: (a) not performing adder amplifier compared with an ideal adder; (b) performing adder amplifier compared with and ideal adder.

analog adder are more stringent than the specifications of the first integrator. In particular, the output of the analog adder is equal to the full-scale voltage V_{fs}. This is motivated by the fact that one of the input branch of the adder processes the input of the modulator. Therefore also the specifications in terms of GBW and SR are more stringent. Although this block has more severe requirements, it takes advantage of a second-order noise shaping, since it sees the same transfer function of the quantization noise. Thanks to the effect of second-order noise shaping the non-linearities of the analog adder are reduced.
In Figure 3.40(a) the effect of a not performing real amplifier is shown. The effect is an increase in the in-band noise with the addition of several harmonics that degrade the SNDR. In fact, even though the adder amplifier takes advantage of second-order noise shaping, it must be sufficiently fast to be able to follow the changes of the input signal. When the specifications of Table 3.5 are achieved in the output spectrum, as in Figure 3.40(b), the harmonics are no longer present. Also the noise floor is not increased, unlike Figure 3.40(a), and the output spectrum is comparable with the ideal adder case.

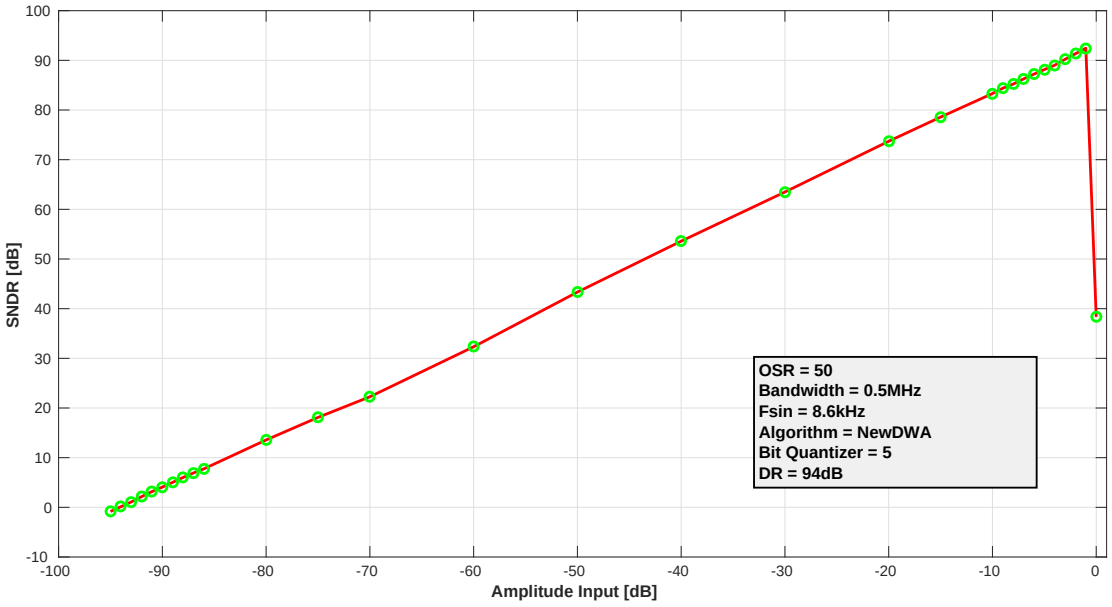


Figure 3.41: Dynamic Range of the proposed design.

f_s	50MHz
OSR	50
Bandwidth	500kHz
Modulator Order	2
Bit Quantizer	5
DR	94dB

Table 3.6: System-Level parameters of the proposed design.

3.5 Conclusion

In Figure 3.41 the SNDR in function of the input amplitude of the modulator is shown. A Dynamic Range of 94dB is obtained with a sine wave input signal with a frequency such that all the main harmonics fall inside the signal bandwidth, namely $f_{sin} = 8.6$kHz. In fact, with a signal bandwidth of 500kHz, all the main harmonic components of f_{sin} fall inside the band, and thus the robustness of the FF topology against the harmonic distortion is proved. As apparent from Figure 3.41 the maximum SNDR is reached for an input value very close to the full scale input signal, which is one of the main features of the FF topology. The minimum SNDR is given by the thermal noise floor. It is worth to notice that in this simulation the mismatch between the capacitors of the DAC is included, but it is shaped by the DEM algorithm described in this Chapter. Thanks to the NewDWA approach the SNDR is not reduced by the harmonic distortion produced by the common DWA algorithm, and thus a higher linearity is obtained. It is worth to notice

that, including all the non-linear effects as the limited DC-gain of the amplifier and the mismatch among the unit elements of the DAC, the SQNR is close to 100dB, therefore doubling the value of the sampling capacitor does not give any real advantage in the dynamic of the modulator, instead it would double the power consumption of the overall ADC. In Table 3.6 the system-level parameters of the modulator are summarized. In the following Chapter the transistor-level design of the overall modulator will be described, with the aim of validating the behavioral model explained in this Chapter.

Chapter 4

Design and Simulation

In this Chapter the design of the $\Sigma\Delta$ modulator is described. After the system analysis the transistor level is studied, as in a classical top-down design strategy. The behavioral model described in Chapter 3 will be validated through simulations using the CMOS 65nm foundry model. All the simulations have been performed with *Cadence* and *Virtuoso Spectre Simulator*.

4.1 First Integrator

Figure 4.1 shows the implementation of the First Integrator. The DAC has been embedded into the first integrator. The sampling capacitor has been split up into 31 capacitors such that $\sum_{i=1}^{31} C_{S1i} = C_{F1}$. During the phase Φ_1 the input V_{in} is sampled into the 31 sampling capacitors. The bottom plate of the sampling capacitors is connected to the common mode voltage. It must be ensured that the output of the quantizer becomes available before the start of the integration phase Φ_2. In fact, when the integration phase starts, the thermometric code of the quantizer must be stable in order to detect which switches are connected to V_{ref-} and which ones to V_{ref+}. During this phase the charge is moved into the feedback capacitor C_{F1}.

4.1.1 Switches

The switches have been implemented using transistor MOS. An ideal switch has infinite resistance when it is open and zero resistance when it is closed. At high supply voltages (5V and higher), a MOS transistor is a good enough approximation of that. If R_{ON} is the on-resistance of a single switch the finite on-resistance of the switches translates into a gain error in the ideal transfer function of the integrator. Moreover the finite resistance can cause problems when the supply voltage is scaled down.
The on-resistance of a MOS switch can be written as

$$R_{ON} = \frac{L}{W\mu C_{ox}(V_{GS} - V_T)}. \tag{4.1}$$

Equation (4.1) is valid when $V_{GS} \geq V_T$, with smaller gate-source voltages the resistance is infinite. In general, the value R_{ON} can be reduced by increasing

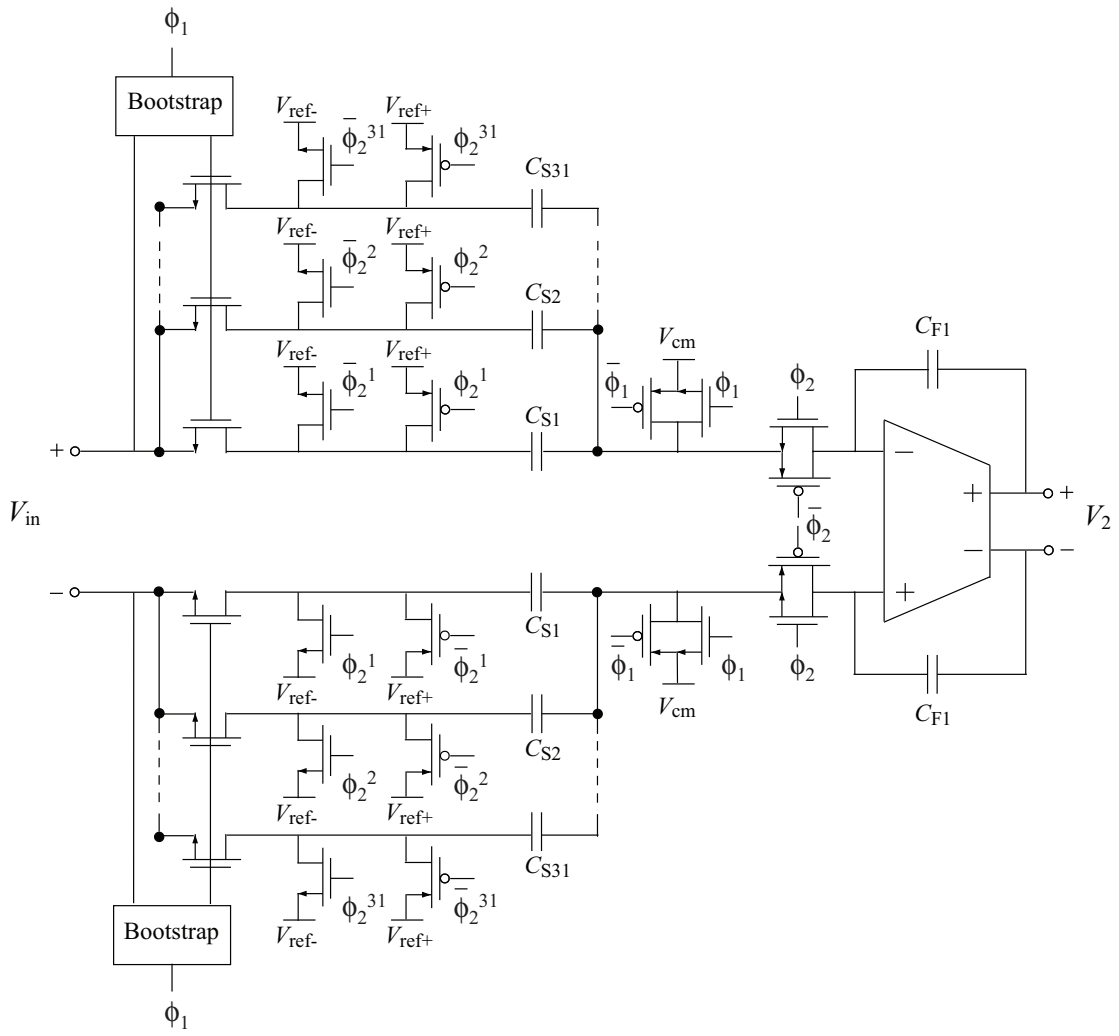
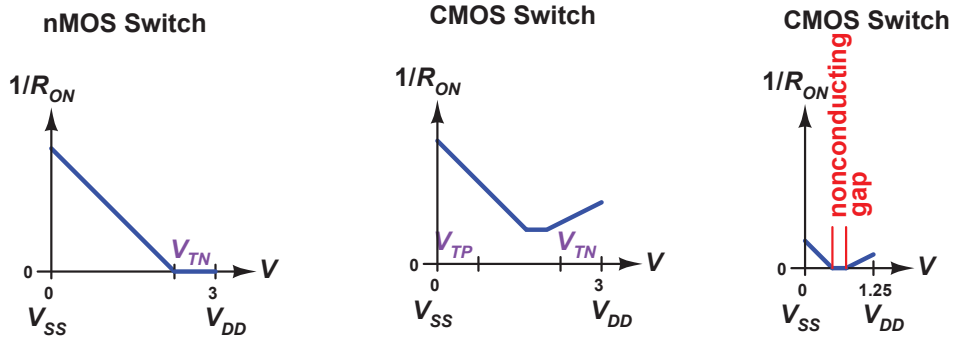


Figure 4.1: Implementation of the First Integrator with the embedded multi-bit DAC.

the aspect ratio (W/L) of the transistors in the CMOS switch, as apparent from Equation (4.1). However, this increases the transistors area, and consequently their associated drain/source capacitances, with the subsequent penalty in the transient response and integrators dynamics degradation. Therefore, there is a trade-off between the maximum value of R_{ON} that can be tolerated and the drain/source parasitic capacitances associated with the CMOS switch that are in turn on conditioned by the value of capacitors used in the SC branches. Furthermore, there is another problem connected to the MOS switches implementation. In fact, a single-transistor switch cannot conduct over the whole rail-to-rail signal range, since, for example, an nMOS switch, whose gate is tied to V_{DD}, cuts off when the signal level is raised within a threshold voltage of V_{DD}. This is illustrated in Figure 4.2(a), where the inverse of the on-resistance is plotted against the signal level. The whole range can be covered by putting an nMOS and a pMOS in parallel to form a CMOS switch or a transmission gate (Figure 4.2(b)). Switches in SC $\Sigma\Delta$ modulators are usually implemented as CMOS transmission gates, so that, at least, either the nMOS or the pMOS transistors are on for a given voltage level to be



(a) (b) (c)

Figure 4.2: Inverse of the switch on-resistance as a function of the signal voltage for (a) an nMOS switch, (b) a CMOS switch with high supply voltage and (c) a CMOS switch with low supply voltage.

transmitted. The resistance in the triode region of the nMOS and pMOS can be approximated to

$$\begin{aligned} R_{ON,N} &= \frac{L_N}{W_N \mu C_{ox}(V_{DD} - V_{TN} - V_{in})}, \\ R_{ON,P} &= \frac{L_P}{W_P \mu C_{ox}(V_{in} - |V_{TP}|)}. \end{aligned} \tag{4.2}$$

The on-resistance of the CMOS transmission gate is thus obtained as $R_{ON} = R_{ON,P}||R_{ON,N}$, warranting a rail-to-rail operation of the switch as long as $V_{DD} > V_{TN} + |V_{TP}|$. In Figure 4.2(b) the supply voltage is much larger than the sum of the two threshold voltages. Therefore, in this case, it is relatively easy to achieve a large conductance from rail to rail for V_{in}. However, when V_{DD} is less than the sum of the two threshold voltages, as in Figure 4.2(c) there is a large range of V_{in} for which the switch will not conduct. In the feed-forward circuit the majority of transistor sees a small signal swing, thanks to the unitary STF. For instance, as depicted in Figure 4.1, the transistors with one of their terminals connected to the reference voltages V_{ref-} and V_{ref+}, namely 0 and V_{DD} are realized respectively with a simple nMOS or a pMOS. This is explained by the fact that the nMOS conducts well the digital 0, while the pMOS conducts well the digital 1. The transistors with one of their terminal connected to the common mode V_{cm} are realized with a transmission gate, since the drain-source voltage is independent from the input signal. In this case the drain-source voltage does not change much over the clock periods. However, the transistors connected to the input signal V_{in} must be realized with a different strategy, since a rail-to-rail input signal is applied at the source of the transistor and the drain is not connected to a constant voltage. Combined with a low-supply voltage this implies the condition depicted in Figure 4.2(c).
In order to solve the problem of this non-conducting gap a bootstrap voltage solution has been chosen [52]. The schematic of the actual bootstrap circuit is depicted in Figure 4.3. It operates on a single phase clock Φ that turns the switch M_0 on and

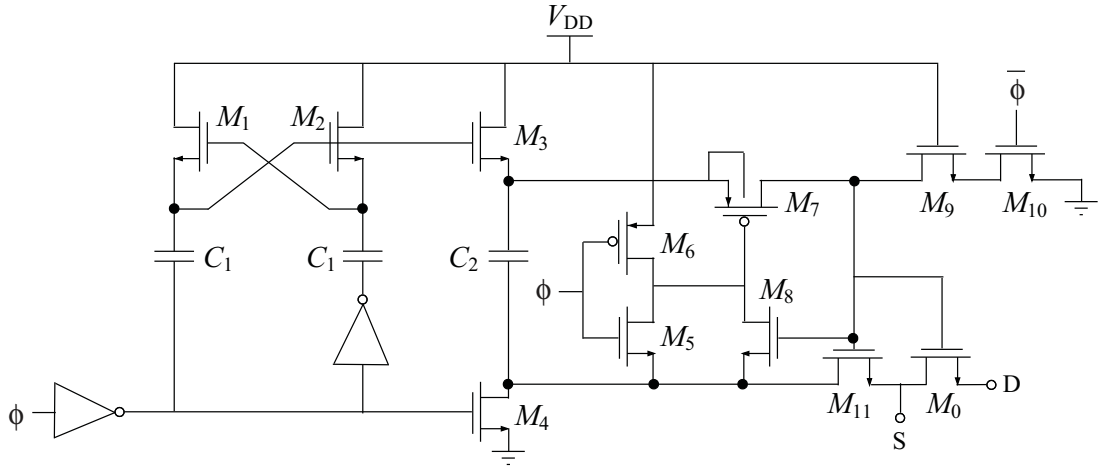


Figure 4.3: Implementation of bootstrap circuit and switching device.

off. During the off phase, Φ is low. Devices M_9 and M_{10} discharge the gate of M_0 to ground. At the same time, V_{DD} is applied across capacitor C_2 by M_3 and M_4. This capacitor will act as a battery across the gate and the source during the on phase. M_7 and M_{11} isolate the switch from C_2 while it is charging.
When Φ goes high, M_5 pulls down the gate of M_7, allowing charge from the battery capacitor C_2 to flow onto the gate of M_0. This turns on both M_{11} and M_0. M_{11} enables the gate to track the input voltage S shifted by V_{DD}, keeping the gate-source voltage constant regardless of the input signal. For example, if the source S is at V_{DD}, then the gate of M_0 is at $2V_{DD}$, however, $V_{GS} = V_{DD}$. Because the body (nwell) of M_7 is tied to its the source, latch-up is suppressed. In Figure 4.1 this circuit is represented by the Bootstrap block. Two devices in Figure 4.3 are not functionally necessary but improve the circuit reliability. Device M_9 reduces the V_{DS} and V_{GD} experienced by device M_{10} when $\Phi = 0$. The channel length of M_9 can be increased to further improve its punch-trough voltage. Device M_8 ensures that $V_{GS,7}$ does not exceed V_{DD}. Figure 4.4 shows a simulation of the bootstrap circuit with $V_{DD} = 1.2$V. When the clock is high, the gate voltage of the switch is greater than the analog input signal by a fixed difference V_{DD}. This ensures the switch is operated in a manner consistent with the reliability constraints. Therefore rail-to-rail signals can be used without a degradation for the switch linearity.
The design of the bootstrap circuit of Figure 4.3 follows these rules: the capacitor value is a trade-off between the area considerations and the ability to charge the load to the desired voltage level. In particular C_2 must be sufficiently large to supply charge to the gate of the switching device in addition to all parasitic capacitances in the charging path; M_3 and M_4 are large in order to quickly charge C_2 during the phase $\Phi = 0$; C_1 is large enough so that the boosted voltage at the gate of M_3 and M_1 is sufficient to turn M_3 and M_1 on; M_7 and M_{11} aspect ratio is large in order to decrease the rise time of the boosted clock.
In all the switches, in order to reduce charge injection effects and clock feed-through,

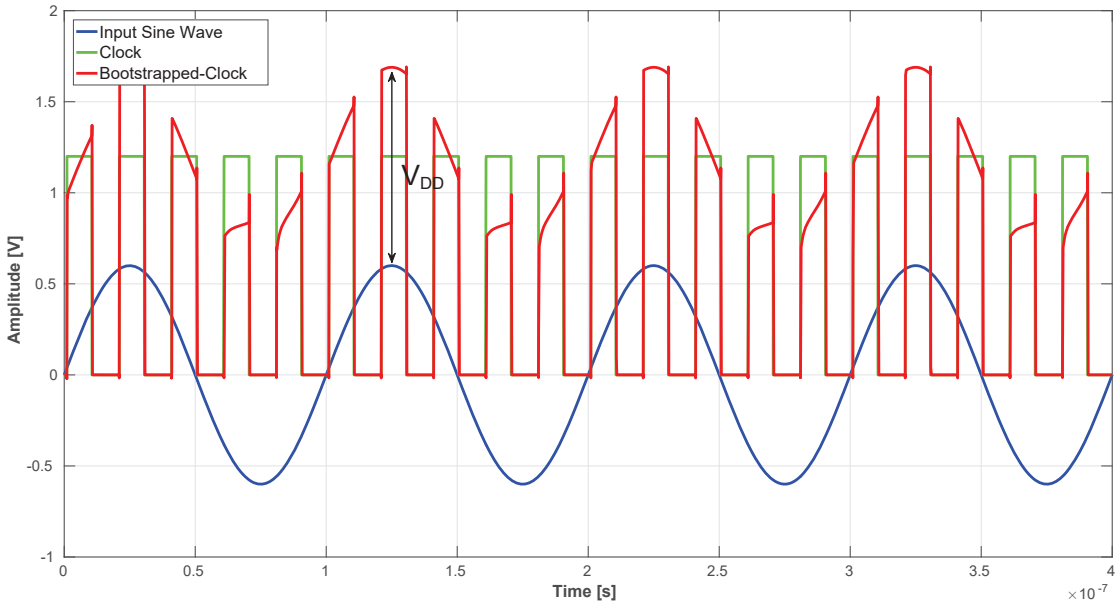


Figure 4.4: Simulation of the bootstrap circuit.

bottom plate sampling strategy is used. With bottom plate sampling the switches connected to the common mode voltages, or to the reference voltages, are opened slightly earlier compared to the switches connected to the input. In this way there is no charge injection on the sampling capacitor.

4.1.2 Amplifier

The amplifier is realized in order to achieve the specifications of Table 3.5, namely DC-gain $A_v = 46$dB, GBW = 120MHz and SR = 60V/μs. Since the output swing is small, a cascode output stage can be used [53]. Between the Folded cascode and the Telescopic cascode, the second topology is chosen. In fact, even though the telescopic topology offers a lower output swing, which for this design is not a real issue, the folded cascode is noisier.
The telescopic OTA shown in Figure 4.5 combines a small power consumption with a high GBW. The basic characteristics of a Telescopic OTA are summarized in Table 4.1, where the evaluated noise is the equivalent noise reported to the input of the amplifier.
It is worth to notice that the transistors M_9, M_{10} and M_{11} are part of the biasing circuitry. In fact the transistor M_9 copies the current of M_8 in order to generate the correct bias for M_3 and M_4 through the transistors M_{10} and M_{11}. The current that is flowing into this branch is a scaled copy of the current of the actual amplifier stage, in order to minimize the overall power consumption. Since the SR is given by SR $= I_{bias}/C_L$ where I_{bias} is the total current and C_L is loading capacitor of the OTA, including the output parasitic capacitor of the OTA, it is possible to find the biasing current needed for the OTA. The first integrator load is given not only by the sampling capacitor of the second integrator, but also by the sampling capacitor

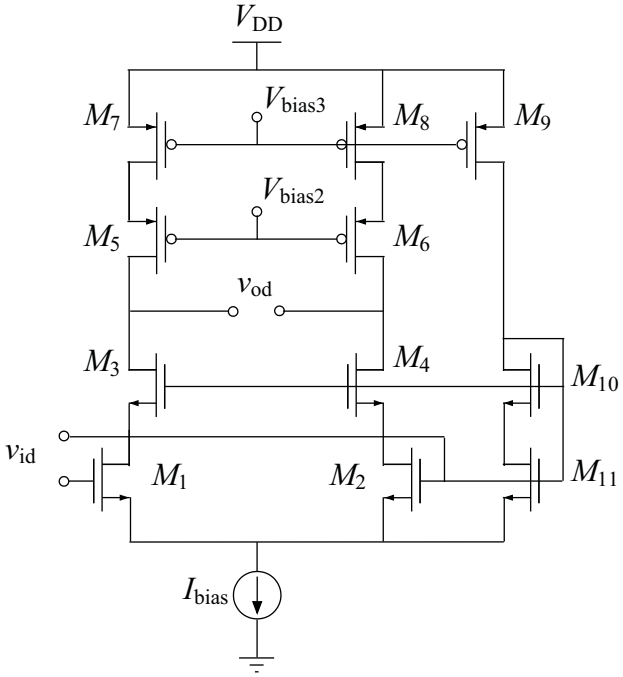


Figure 4.5: Telescopic OTA.

A_v	R_{out}	BW	GBW	Noise
$g_{m1}R_{out}$	$\frac{1}{2}r_{01}g_{m2}r_{02}$	$\frac{1}{2\pi R_{out}C_L}$	$\frac{g_{m1}}{2\pi C_L}$	$2\left[v_{n1}^2 + (\frac{g_{m7}}{g_{m1}})^2 v_{n7}^2\right]$

Table 4.1: Characteristics of the Telescopic Cascode topology.

of the adder since there is one path bringing the output of the first integrator into the analog adder, therefore

$$C_L = C_o + C_{S2} + 2C_{S3} + C_{F1}(1-\beta) \tag{4.3}$$

where C_o is the output parasitic capacitor of the OTA, C_{S2} is the sampling capacitor of the second integrator, C_{S3} is the sampling capacitor of the adder and $C_{F1}(1-\beta)$ is the feedback capacitor reported at the output for the Miller effect [54]. With $I_{bias} = 150\mu$A the simulated transfer function of the Telescopic OTA is reported in Figure 4.6.

As apparent from Figure 4.6 the GBW and the DC-gain satisfy with a good margin the specifications found by the behavioral model. Moreover also process corner and Montecarlo simulations have been performed in order to ensure the reliability of the amplifier. The process corner simulations are performed in all the five possible process corners, namely the nominal corner, the fast-fast (FF) corner, the slow-slow (SS) corner, the fast-slow (FS) corner and the slow-fast (SF) corner. The process corner simulation is depicted in Figure 4.7, while the Montecarlo simulation is shown in Figure 4.8. As apparent from both the figures the minimum specifications are always achieved. The simulated power consumption of the amplifier is $P = 180\mu$W.

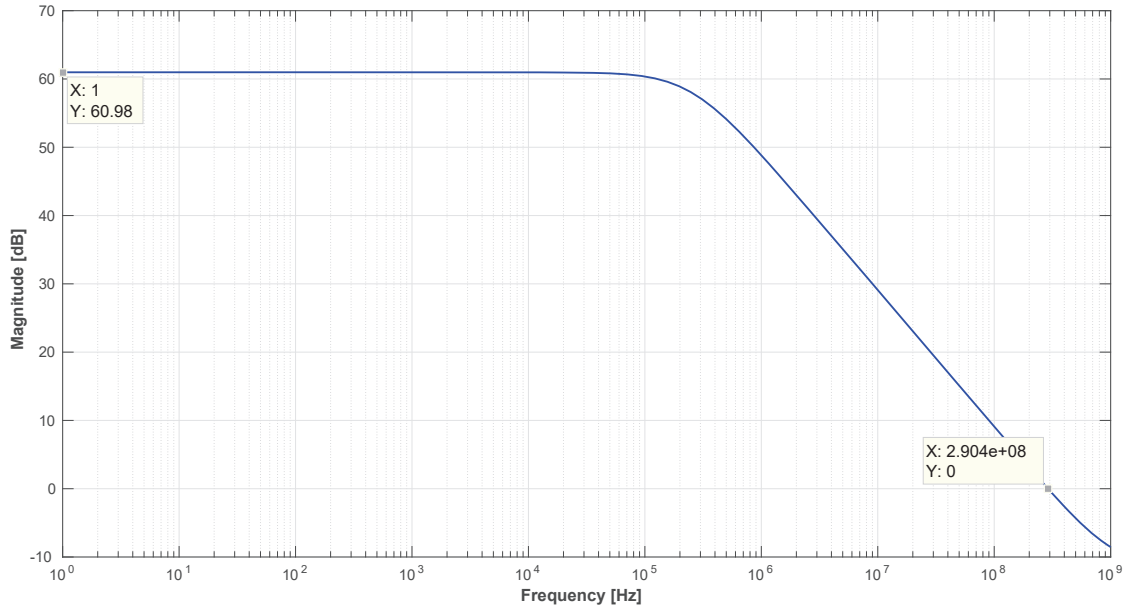


Figure 4.6: Bode diagram of the transfer function of the Telescopic OTA realizing the first integrator.

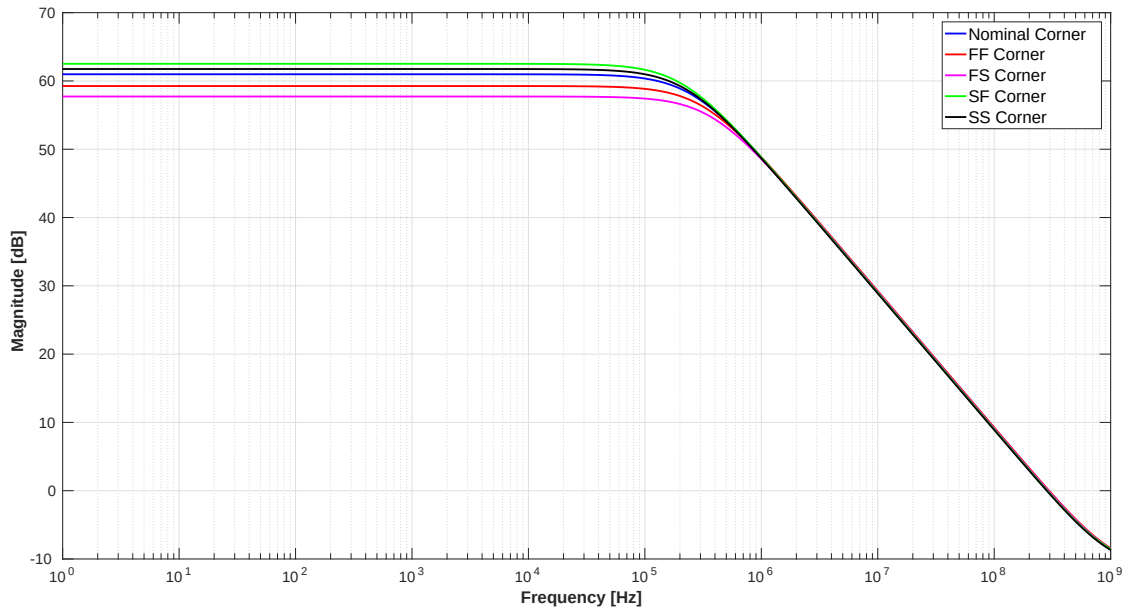


Figure 4.7: Simulation of the the transfer function of the Telescopic OTA realizing the first integrator in all the process corners (Nominal, FF, FS, SF, SS).

4.1.3 Biasing and CMFB

The biasing of the Telescopic OTA is shown in Figure 4.9. A high-swing cascode current mirror topology is used. This current mirror generates the biasing for the pMOS transistors, namely the transistors acting as a load, of the Telescopic OTA.

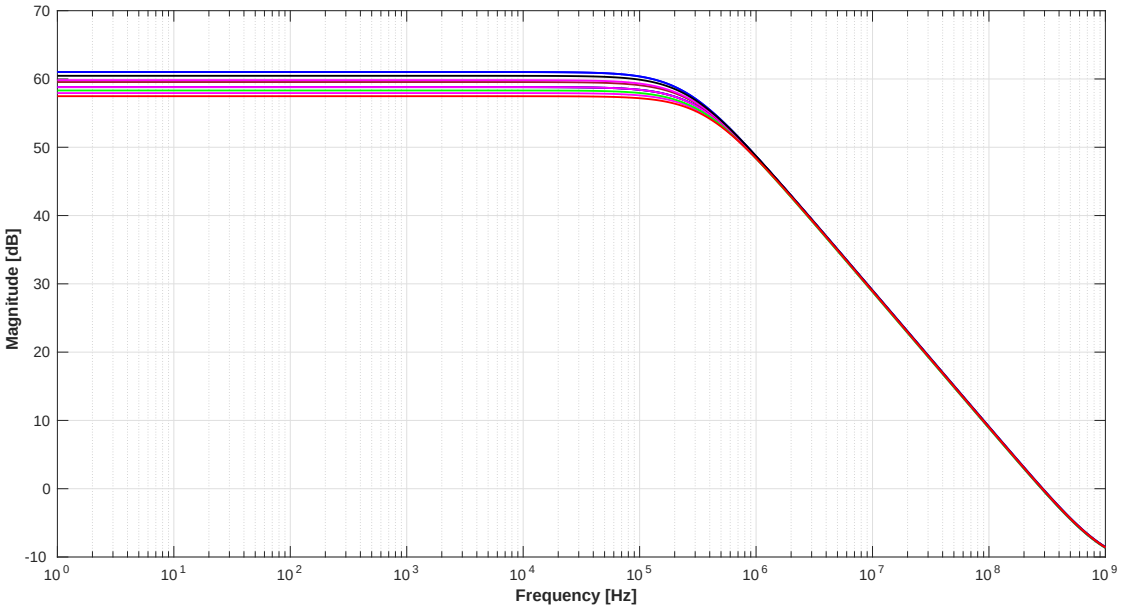


Figure 4.8: Montecarlo simulation of the transfer function of the Telescopic OTA realizing the first integrator.

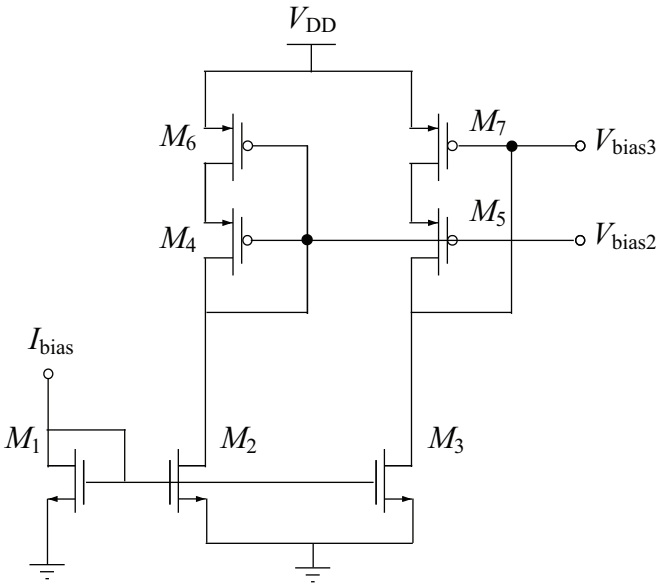


Figure 4.9: Biasing of the Telescopic OTA.

The current consumption of this stage has been minimized in order to minimize the overall power consumption.
Since the overall design is based on a fully differential implementation, a circuit to control the output common mode of the amplifier is necessary. A common mode feedback loop (CMFB) [55] has been implemented with switched capacitors as depicted in Figure 4.11.

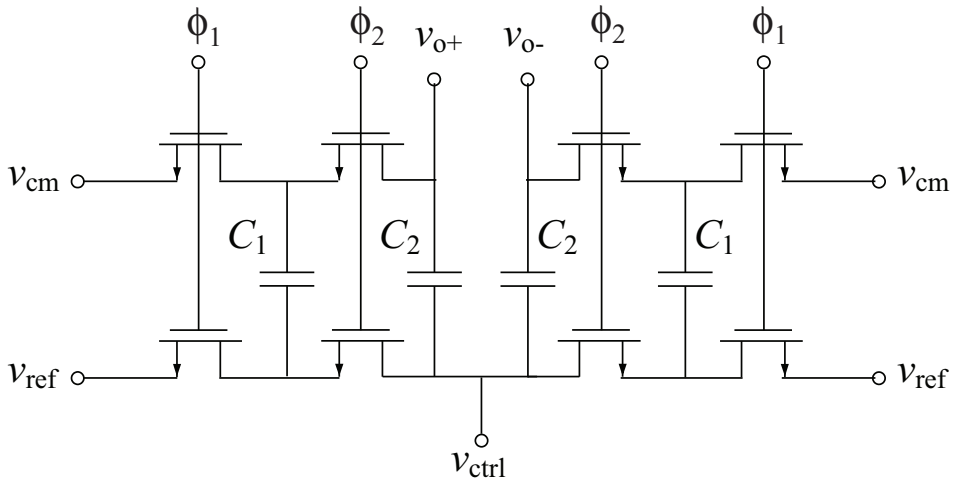


Figure 4.10: Switched Capacitor CMFB.

The control voltage v_{ctrl} is applied into the gate of a transistor in parallel to the transistor generating the bias current of the OTA. The reference voltage v_{ref} is generated by transistor connected as a diode. Practical considerations need to be taken into account when designing fully differential OTAs that use SC-CMFB. The most critical parameters for a good design are the open loop CMFB gain A_{cm} and the bandwidth BW. A_{cm} needs to be as high as possible for better accuracy when V_{cm} reaches the steady state. On the other hand, the CMFB BW should be as large as the differential mode BW in order to track fast CM variations. The challenge is to obtain the highest CMFB gain while having the required BW and still maintain the OTA required specifications.

When designing the SC-CMFB network the parameters under control in the circuit are the sizes of the capacitor and the size of the switching transistors. The capacitance ratio C_1/C_2 has an effect over the v_{cm} settling time. For high values of C_1/C_2 the DC CM voltage settles faster after start-up. This suggests that C_2 should be as small as possible and C_1 as large as possible. However, having a slow start-up for the DC CM output voltage is not a real problem in a $\Sigma\Delta$ modulator. Nevertheless it is recommended to keep C_2 small as possible since a small C_2 implies that also the BW of the OTA increases, due to the fact that C_2 is part of the OTA loading capacitor. It is worth to notice that C_1 can not be too large because it would require larger switches to keep the CMFB network RC constant low. The use of larger switches increases the charge injection error and requires more chip area. Furthermore, by increasing the size of the switches also the size of the parasitic capacitors is increased. Table 4.2 summarizes how changing the parameters A_{cm}, BW_{cm}, C_1, C_2 and W_{switch} improves the OTA and CMFB performance. In this design $C_1 = 80\text{fF}$ and $C_2 = 20\text{fF}$.

Effect	A_{cm}	BW$_{cm}$	C_1	C_2	W_{switch}
DC V_{cm} Settling time ↓	-	↑	↑	↓	↑
V_{cm} accuracy ↑	↑	-	↑	-	↓
OTA BW ↓	-	↑	-	↓	-
Charge injection error ↓	-	-	↓	-	↓

Table 4.2: Effect of parameters variation in CMFB network.

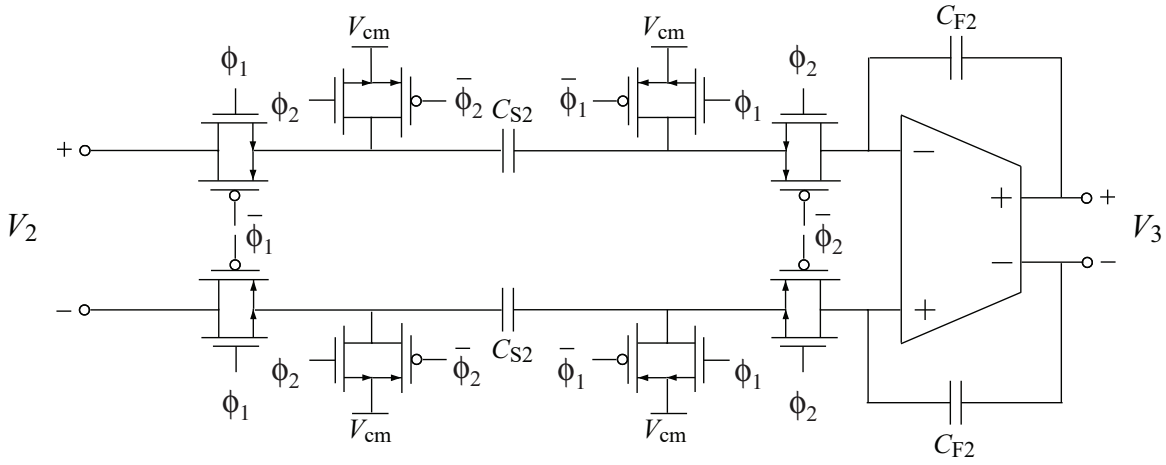


Figure 4.11: Implementation of the Second Integrator.

4.2 Second Integrator

The implementation of the second integrator is shown in Figure 4.11. As already discussed, one of the advantages of the FF topology is that there is only one feedback loop, therefore there is no need of embedding a DAC also in this integrator. All the switches are realized with a transmission gate logic. There is no need of bootstrapping switches since the voltage swing in the nodes of this stage is independent of the input signal, but it is related only to the quantization noise.

4.2.1 Amplifier

The amplifier is realized in order to achieve the specifications of Table 3.5, namely DC-gain $A_v = 40$dB, GBW = 90MHz and SR = 40V/μs. Since the output swing is small, a cascode output stage can be used. As for the first integrator, a telescopic cascode topology is used (as the one in Figure 4.5).
Since the SR is given by SR $= I_{bias}/C_L$ where I_{bias} is the total current and C_L is loading capacitor of the OTA, it is possible to find the biasing current needed for the OTA. The second integrator load is given by only the adder, therefore

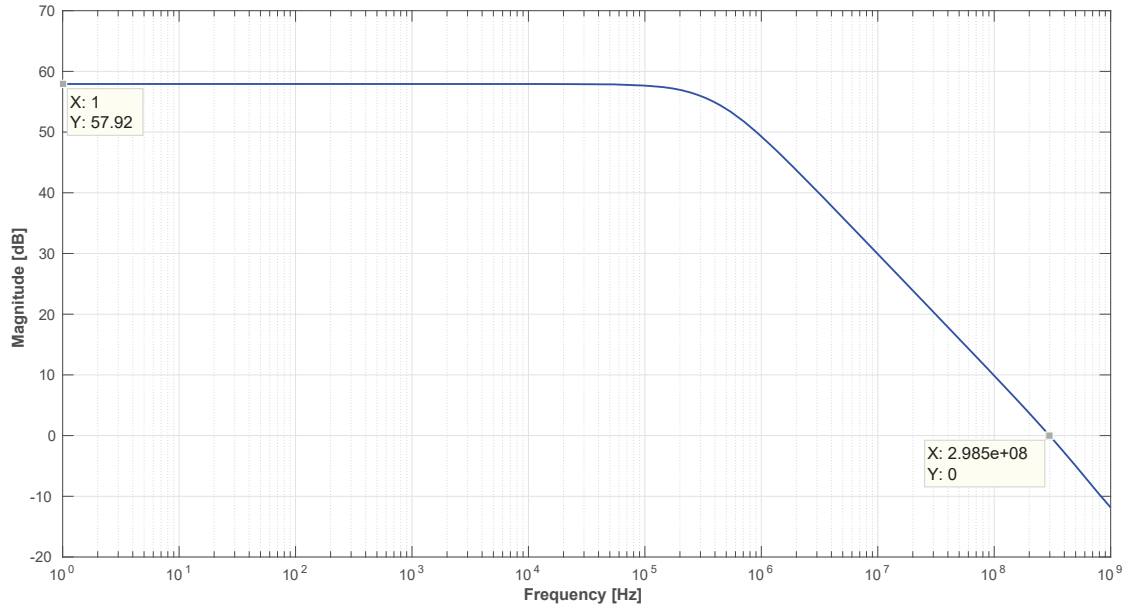


Figure 4.12: Bode diagram of the transfer function of the Telescopic OTA realizing the second integrator.

$$C_L = C_o + C_{S3} + C_{F2}(1 - \beta), \tag{4.4}$$

where C_o is the output parasitic capacitor of the OTA, C_{S3} is the sampling capacitor of the adder and $C_{F2}(1-\beta)$ is the feedback capacitor reported at the output for the Miller effect. Since the thermal noise is dominated by the first stage, the size of these capacitors is reduced. The combination of a reduced specification in terms of SR and GBW, with a reduced load capacitor, expressed in Equation (4.4), yields $I_{bias} = 15\mu$A. The simulated transfer function of the Telescopic OTA is reported in Figure 4.12.
As apparent from Figure 4.12 the GBW and the DC-gain satisfy with a good margin the specifications found by the behavioral model. Moreover also process corner and Montecarlo simulations have been performed in order to ensure the reliability of the amplifier. The process corner simulation is depicted in Figure 4.13, while the Montecarlo simulation is shown in Figure 4.14. As apparent from both the figures the minimum specifications are always achieved. The same biasing circuit of the first integrator OTA has been used in order to generate the correct biasing of the pMOS load transistors. The simulated power consumption of the amplifier is $P = 20\mu$W.

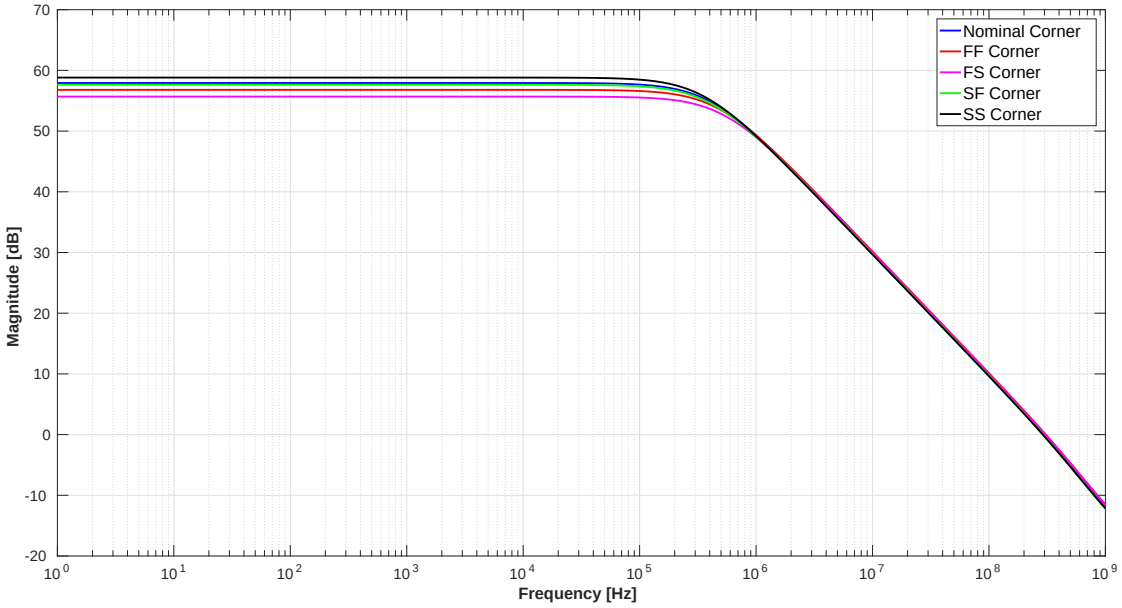


Figure 4.13: Simulation of the the transfer function of the Telescopic OTA realizing the second integrator in all the process corners (Nominal, FF, FS, SF, SS).

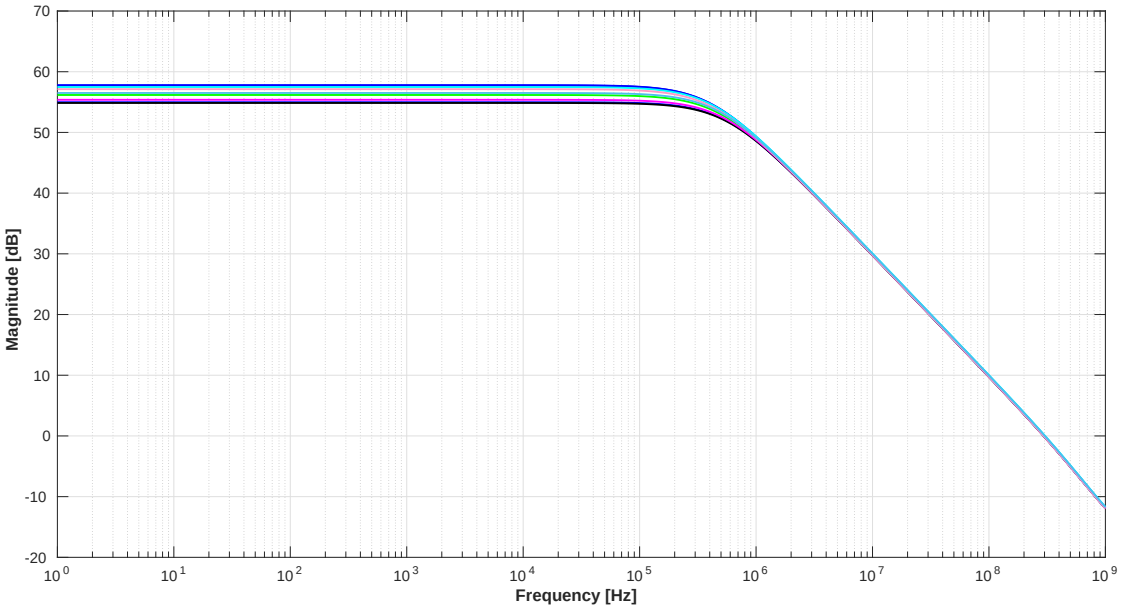


Figure 4.14: Montecarlo simulation of the transfer function of the Telescopic OTA realizing the second integrator.

4.3 Analog Adder

The implementation of the analog adder is shown in Figure 4.15. The majority of the switches of this stage is realized with a transmission gate. The only exception is represented by switches with one of their terminals connected to the input signal.

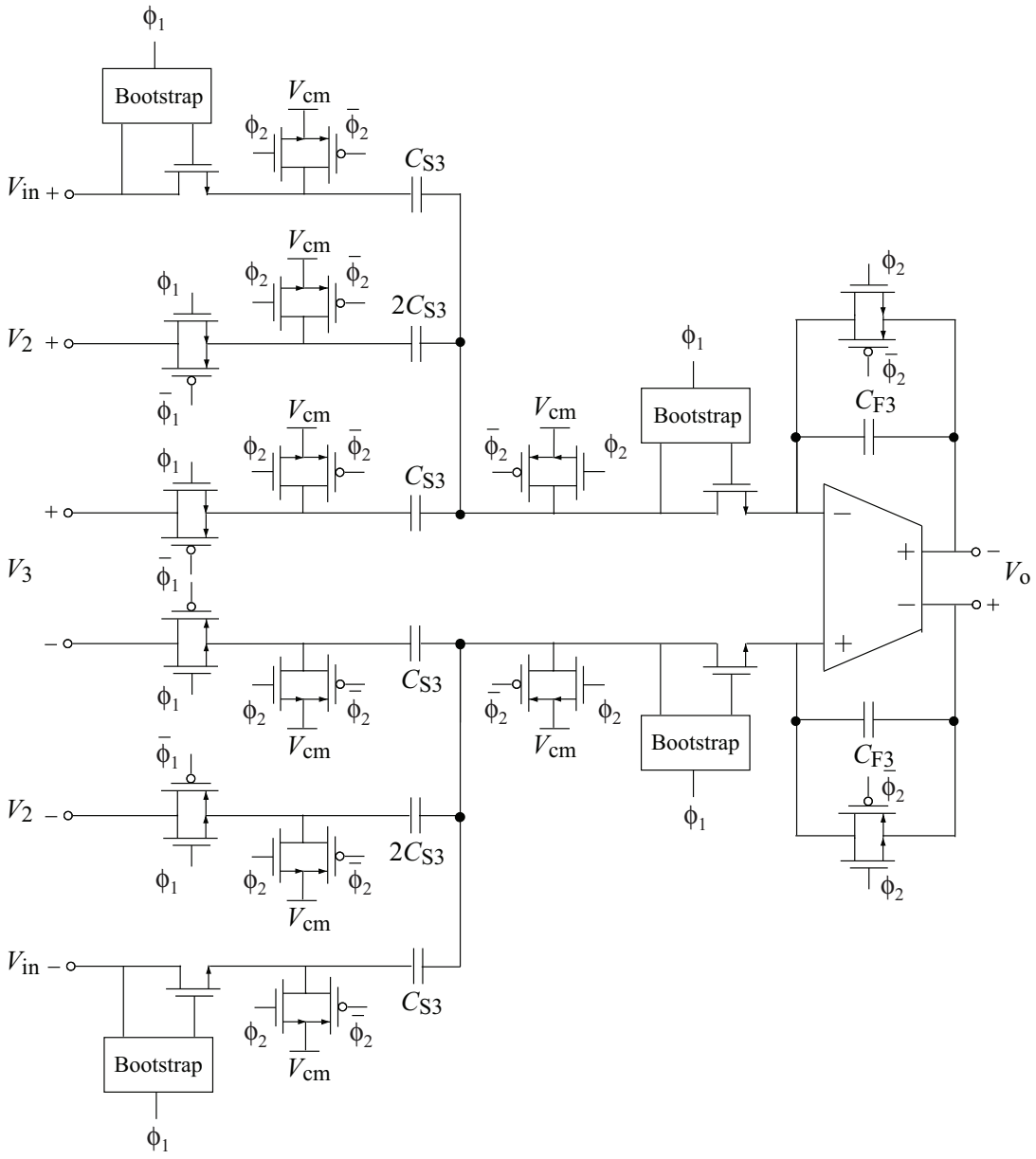


Figure 4.15: Implementation of the analog adder.

In fact these switches, that are located on the feed-forward branch, have a full signal swing and, therefore, are realized as bootstrapped switches. The implementation of a SC adder is similar to an integrator. During the phase Φ_1 the charge is move into the sampling capacitors and into the feedback capacitor C_{F3}. During this phase the output voltage V_o is given by

$$V_o = -\left[-\left(\frac{C_{S3}}{C_{F2}}V_{in} + \frac{2C_{S3}}{C_{F2}}V_2 + \frac{C_{S3}}{C_{F2}}V_3\right)\right]. \tag{4.5}$$

It is worth to notice that Equation (4.5) is the result of an inverting summing amplifier circuit, which motivates the minus sign inside the square brackets. However, since at the output of the analog adder the signs are swapped, in Equation (4.5)

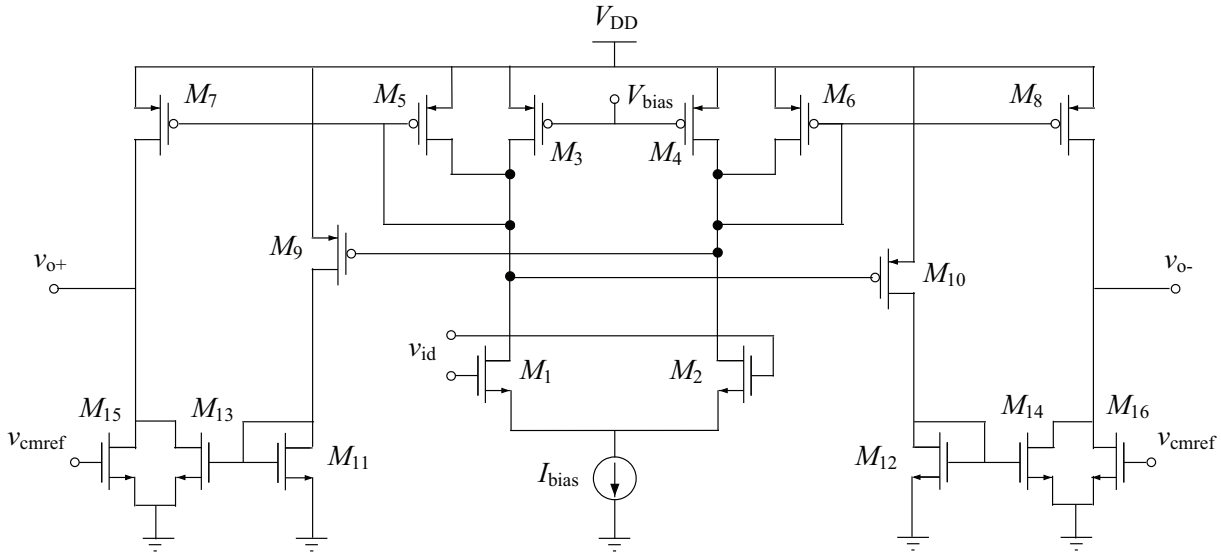


Figure 4.16: OTA topology used for the analog adder.

there is another negative contribution. In this way the input-output transfer function is mainly positive. During the Φ_2 phase the charge in the capacitors is setted to zero, making the capacitors available for a new summation in the next Φ_1 phase.

4.3.1 Amplifier

The amplifier is realized in order to achieve the specifications of Table 3.5, namely DC-gain $A_v = 38$dB, GBW = 160MHz and SR = 80V/μs. The problem of this stage is that the the output swing is rail-to-rail, since one of the branches of the adder process the input signal, therefore a cascode output stage cannot be used otherwise distortion due to headroom saturation will appear at the output of the adder. The specification on the DC-gain makes it impossible to use a single-stage rail-to-rail amplifier in a 65nm technology. Therefore, in order to achieve the gain of $A_v = 38$dB, a two stage amplifier must be used. However, the multi-stage amplifier, which spends power on driving the compensation capacitances, is not competitive compared with the single-stage amplifier in terms of power efficiency. In order to avoid a Miller OTA, which would lead to a Miller compensation capacitor and therefore to a large power consumption, a new amplifier topology has been studied. The topology of the amplifier is shown in Figure 4.16. Transistors M_3 and M_4 act as two current sources placed in parallel with the diode-connected transistors, M_5 and M_6, and shunt part of the current from these transistors. Assuming that

$$\frac{(W/L)_7}{(W/L)_5} = \frac{(W/L)_{13}}{(W/L)_{11}} = B \qquad \frac{(W/L)_3}{(W/L)_5} = \frac{k}{1-k} \tag{4.6}$$

the output current that is flowing into M_7 is given by

$$I_{D7} = \frac{B(1-k)I_{bias}}{2} = B(1-k)I_{D1}. \tag{4.7}$$

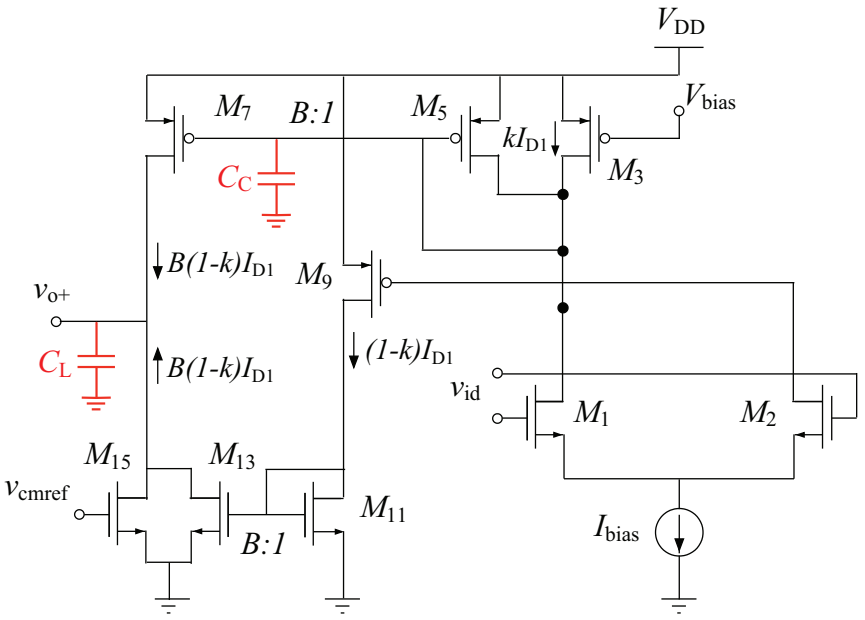


Figure 4.17: Parasitic capacitance and internal pole in the proposed OTA.

The gain of the OTA is given by

$$A_v = \frac{g_{m1}}{g_{m5}} g_{m7} r_{07} = g_{m1} B \; r_{07} = \frac{2I_{D1}}{(V_{GS1} - V_T)} \frac{B}{\lambda_7 I_{D7}} \tag{4.8}$$

where λ is the channel length modulation coefficient. The gain of the OTA can be expressed substituting Equation (4.7) into Equation (4.8) yielding

$$A_v = \frac{1}{1-k} \frac{2}{(V_{GS1} - V_T)\lambda_7}. \tag{4.9}$$

From Equation (4.9) it can be seen that the OTA gain is enhanced $1/(1-k)$ times. As apparent, the gain enhancement can be adjusted by changing the k factor. Practically, the gain enhancement is restricted by several factors.
The main concern is the frequency response. Using this technique will result in an increased impedance of the internal node, namely the impedance on the gate of M_5. The non-dominant pole frequency will be pulled down and the phase will be reduced too. Shown in Figure 4.17, the total parasitic capacitance associated to the gate of M_5 is represented by C_C while the total capacitor associated to the output, including the parasitic capacitor, is represented by C_L.
The non dominant pole is given by

$$P_{nd} = \frac{g_{m5}}{2\pi C_C} = \frac{2I_{D5}}{2\pi C_C (V_{GS5} - V_T)} = \frac{2(1-k)I_{D1}}{2\pi C_C (V_{GS5} - V_T)}. \tag{4.10}$$

As apparent from Equation (4.10) increasing the capacitor C_C will lead to a smaller non-dominant pole, which can lead to instability. The GBW of the OTA can be expressed as

A_v	R_{out}	BW	GBW	Noise
$g_{m1}B\ R_{out}$	r_{07}	$\frac{1}{2\pi R_{out}C_L}$	$\frac{B\ g_{m1}}{2\pi C_L}$	$2v_{n1}^2\left[\frac{1}{g_{m1}}+\frac{g_{m3}}{g_{m1}^2}\left(1+\frac{1}{B}\right)+\frac{g_{m13}}{B^2g_{m1}^2}\right]$

Table 4.3: Characteristics of the proposed OTA topology.

$$\text{GBW}=\frac{B\ g_{m1}}{2\pi C_L}=\frac{2B\ I_{D1}}{2\pi C_L(V_{GS1}-V_T)}. \tag{4.11}$$

To maintain a reasonably safe phase margin, the non-dominate pole has to be placed at least more than 3 times of the GBW. Assuming that the overdrive voltages of the transistors are the same, then the following criteria can be drown:

$$k\leq 1-3B\frac{C_C}{C_L}. \tag{4.12}$$

Equation (4.12) implies that a maximum gain enhancement can be achieved, without affecting the linearity of the OTA. The smaller C_C/C_L ratio, the more gain enhancement can be achieved. The larger the capacitance load is, the higher gain can be reached. However having a large capacitance load leads to a small bandwidth of the modulator, therefore is not advisable to increase the load capacitor of the OTA. Finally the SR of this topology is given by

$$\text{SR}=\frac{2B(1-k)I_{bias}}{C_L}. \tag{4.13}$$

Summarizing the results, the OTA depicted in Figure 4.16 achieves quite high DC-gain by increasing the factor k. Moreover a quite large GBW can be obtained by increasing the factor B. However there is a trade-off between the choice of the parameters B and k and the stability of the modulator. In fact if B is too large, from Equation (4.12), the maximum factor k in order to stabilize the amplifier is small and therefore a small gain enhancement $1/(1-k)$ is achieved. On the other hand, choosing a large value for k in order to achieve a large gain enhancement, will lead to a reduction of B and therefore a reduction of the GBW. The characteristics of this OTA are summarized in Table 4.3

An interesting feature of this topology is the high GBW and high SR. This fact is important because the adder must achieve more stringent specifications with respect to the integrator. Furthermore the loading capacitor of the OTA is mainly given by the input capacitors of the the 31 comparators, which is actually a large capacitor. With $I_{bias}=70\mu$A the simulated transfer function of the proposed OTA is reported in Figure 4.6.

As apparent from Figure 4.18 the GBW and the DC-gain satisfy with a good margin the specifications found by the behavioral model. Moreover also process corner and Montecarlo simulations have been performed in order to ensure the reliability of the amplifier. The process corner simulation is depicted in Figure 4.19, while the Montecarlo simulation is shown in Figure 4.20. As apparent from both the figures the minimum specifications are always achieved.

Also the loop gain of the OTA has been simulated, as shown in Figure 4.21. As

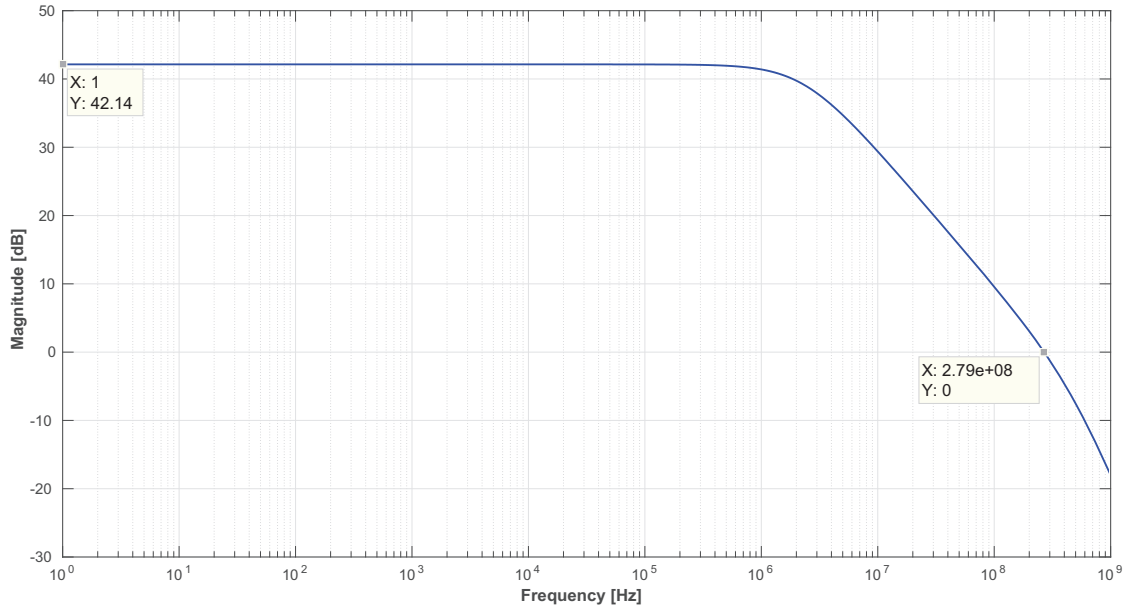


Figure 4.18: Bode diagram of the transfer function of the OTA realizing the analog adder.

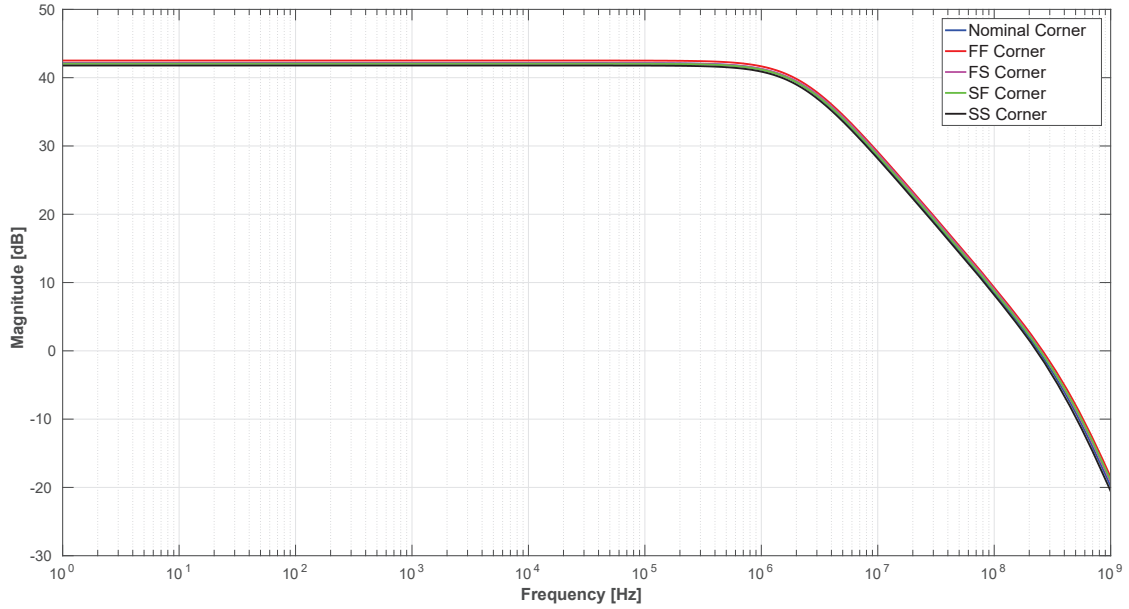


Figure 4.19: Simulation of the the transfer function of the OTA realizing the analog adder in all the process corners (Nominal, FF, FS, SF, SS).

apparent from Figure 4.21 the phase margin (PM) of the amplifier is $PM = 78°$, which ensures a good stability for the amplifier. The simulated power consumption of the amplifier is $P = 100\mu$W.
The biasing of the OTA of Figure 4.16 is depicted in Figure 4.22. The CMFB

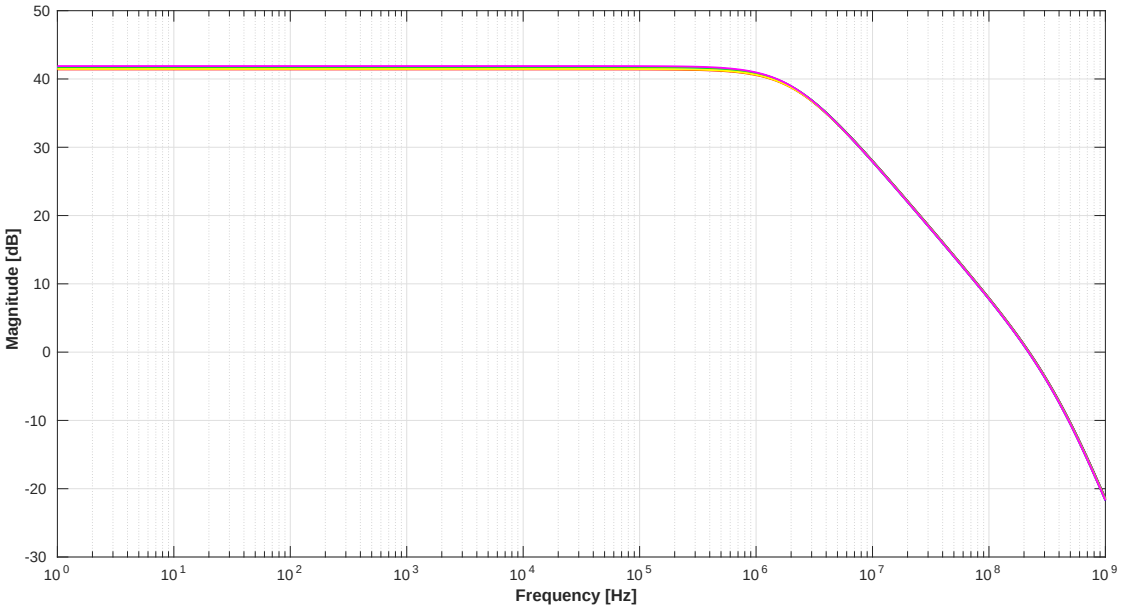


Figure 4.20: Montecarlo simulation of the transfer function of OTA realizing the analog adder.

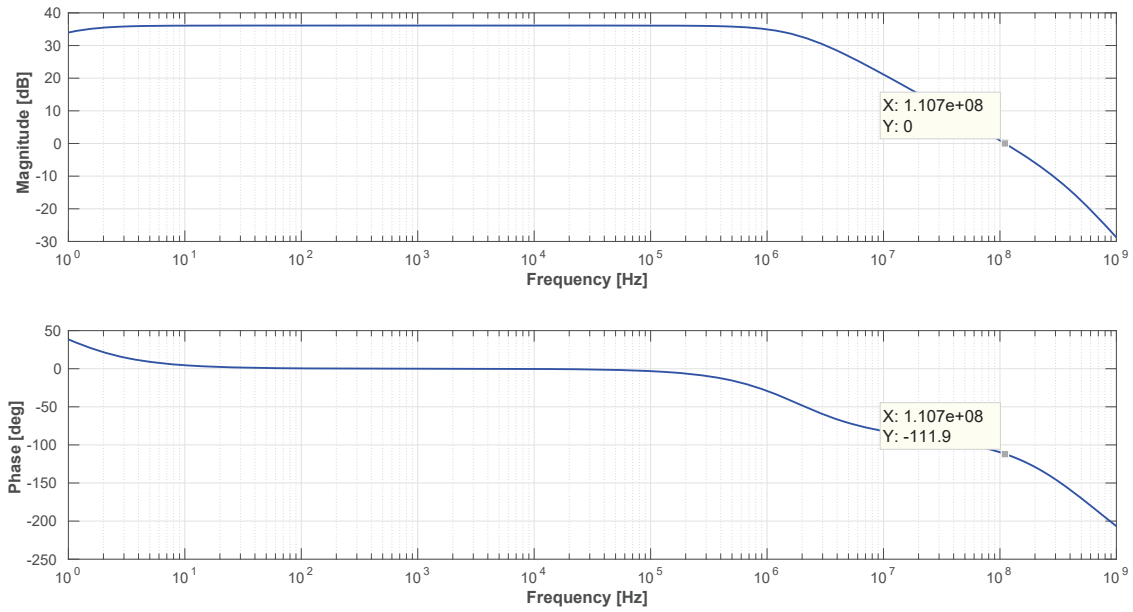


Figure 4.21: Simulation of the loop gain of the OTA realizing the analog adder.

circuit has been realized as in the Telescopic OTA with the difference that the control voltage v_{cmref} is placed in the output branch of the OTA.

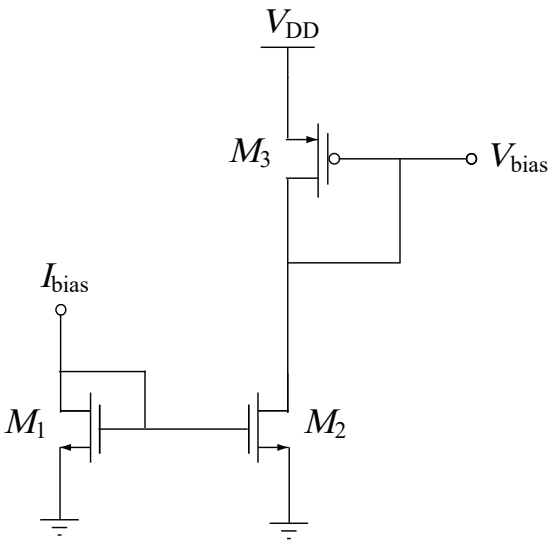


Figure 4.22: Biasing of the OTA realizing the analog adder.

4.4 Comparator

4.4.1 Background

The comparator is a circuit that compares an analog signal with another analog signal, or reference, and yields as output a binary signal based on the comparison. The idea is to amplify the input signal in order to saturate the output of the comparator to V_{DD} or 0, depending on the sign of the input difference. In order to have a correct behavior, the minimum difference between the input signal and the reference that the comparator must be able to solve is equal to the less significant bit [56].
Architecture of modern high speed comparator essentially consists of a pre-amplifier stage and a latch stage. The pre-amplifier stage amplifies the input signal to improve the comparator sensitivity and it also isolates the input of the comparator from switching noise coming from the positive feedback stage [57]. The second stage is a latch stage which is used to determine the larger input signal and thus need to have high gain. Usually, in order to achieve high gain and fast response, a positive feedback is used.
In Figure 4.23 a classical comparator with pre-amplifier is shown [58]. The pre-amplifier amplifies the difference between the differential input voltage $(v_{i+} - v_{i-})$ and the differential reference voltage $(v_{rp} - v_{rn})$, according to:

$$\begin{aligned} v_{o-} &= A\left[((v_{rp} - v_{i+}) - (v_{rn} - v_{i-})\right] \\ v_{o+} &= A\left[((v_{rn} - v_{i-}) - (v_{rp} - v_{i+})\right] \end{aligned} \tag{4.14}$$

where A is the DC-gain. It is worth to notice that the nMOS differential pair is loaded with pMOS diodes and pMOS cross-coupled latch, namely transistors M_5,

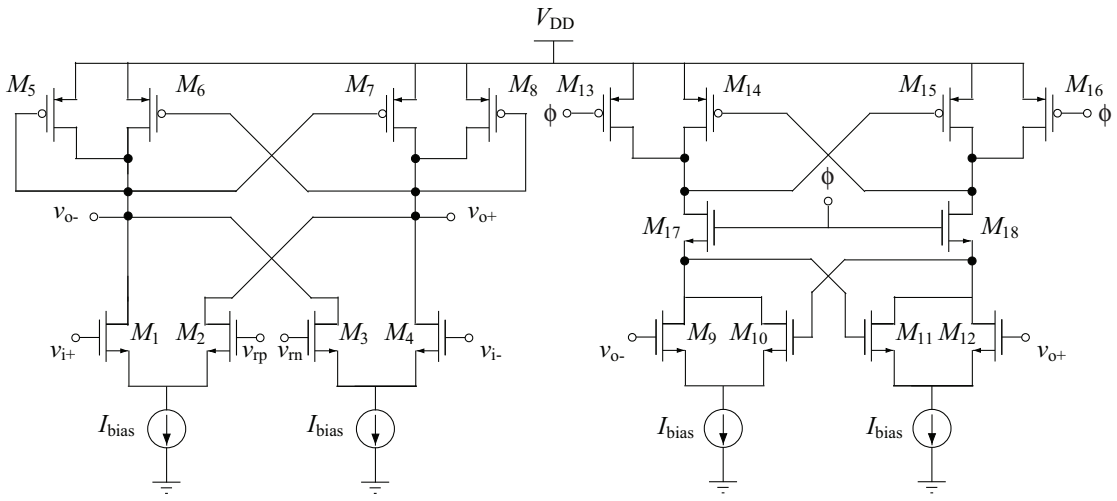


Figure 4.23: Comparator with pre-amplifier topology.

M_6, M_7 and M_8. This ensures high gain and there is no need of CMFB to control the output common mode. The DC-gain of the amplifier is given by

$$A = -g_{m1}\left[\frac{1}{g_{m5}}||\left(-\frac{1}{g_{m6}}\right)||r_{01}||r_{05}||r_{06}\right] \approx -\frac{g_{m1}r_{01}}{3}. \tag{4.15}$$

The pre-amplifier output difference $(v_{o+} - v_{o-})$ is then passed to the latch, which, on the positive edge of the clock, determines the digital output signals, depending on its input. The pre-amplifier is the most commonly uses solution placed in front of the comparator for two main advantages.
The first reason is the reduction of the input-referred offset. In fact, due to mismatch between input transistors, the circuit exhibits a DC offset of different values. This value of DC offsets depends on the mismatch of input and output voltages. The offset can limit the performance of comparator and can make the system non-linear. The total input-referred comparator offset is given by

$$V_{os}^2 = V_{os,1;2;3;4}^2 + \frac{V_{os,9;12}}{A^2}. \tag{4.16}$$

As apparent from Equation (4.16), the input-referred latch offset is divided by the gain of the pre-amplifier. This also motivates why it is important to have a large gain in the pre-amplifier, as the one of Equation (4.15). In fact the gain of the pre-amplifier reduces the offset of the second stage. However it should be noticed that the offset of the pre-amplifier is not reduced, therefore the size of the transistor $M_1 - M_4$, namely the differential pair of the pre-amplifier, must be chosen correctly in order to limit its offset.
The second reason is the reduction of the kickback noise effect. In order to show the effect of the kickback noise a common structure of a latched comparator is shown in Figure 4.24 for the sake of clarity. During the regeneration process the latched comparator uses the two cross-coupled inverters implementing a positive feedback mechanism to scale the digital level. The large voltage variations on the

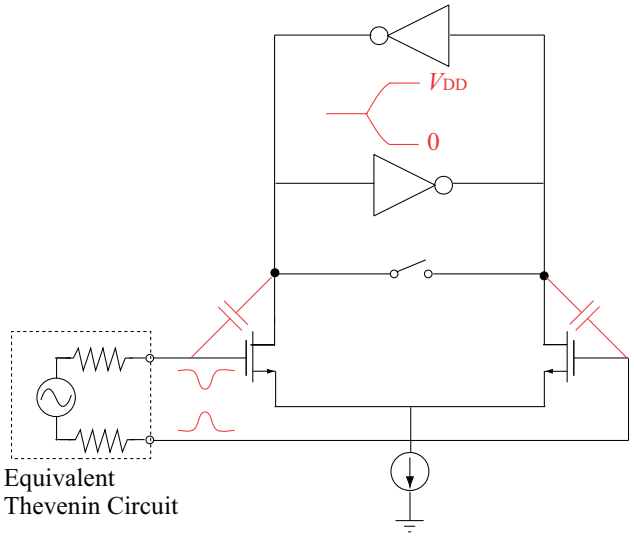


Figure 4.24: Effect of kickback noise.

regeneration nodes are coupled, through the parasitic capacitances of the transistors, to the inputs. Since the circuit preceding does not have zero output impedance, the input voltage is disturbed, which may degrade the accuracy of the converter. Since the pre-amplifier isolates the latch from the input voltage, the kickback noise effect is reduced.
Besides the advantages that the solution including the pre-amplifier stage ensures, the main problem of this kind of solution is the increase in the power consumption.

4.4.2 Dynamic Comparator

Conventionally, to decrease the offset voltage, a pre-amplifier has been utilized prior to the regenerative latch stage, which is able to amplify a small input signal to a large output signal to achieve a low latch offset voltage and a low kickback noise. Nevertheless, a pre-amplifier based comparator performance is affected from large static power dissipation. Therefore, a dynamic latch comparator without pre-amplifier is very much enviable for high speed and low power applications.
The comparator shown in Figure 4.25 is called a resistive divider comparator, and it is proposed in [59]. The main advantage of this design is the zero DC power dissipation and built-in circuitry to adjust the threshold voltage as in Equation (4.17)

$$v_{i+} - v_{i-} = \frac{\mu_n C_{ox} W_1/L_1}{\mu_n C_{ox} W_3/L_3}(v_{rp} - v_{rn}). \tag{4.17}$$

In Figure 4.25, to adjust the threshold voltage, transistors $M_1 - M_4$ are utilized as the adjustment circuitry. In order to adjust the threshold voltage is necessary to change the size ratio between the two differential pairs. On the other hand, latch circuit is composed with the transistors $M_5 - M_{12}$. When $\Phi = 0$, transistors M_9 and M_{12} are in conducting mode, M_7 and M_8 go to cut off region. As a result both

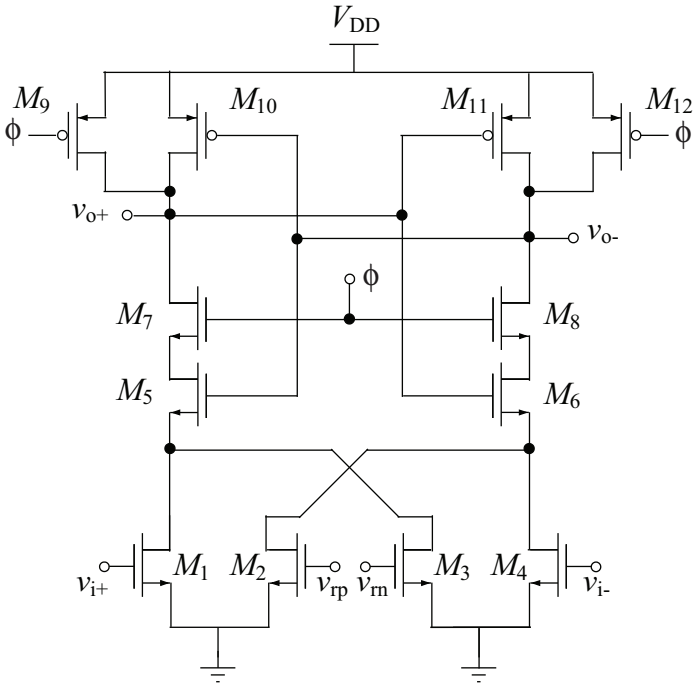


Figure 4.25: Resistive divider dynamic comparator.

the differential outputs become V_{DD} and there is no current passes between the supply voltage and ground. Concurrently, M_{10} and M_{11} are in cut off region while M_5 and M_6 are in conducting mode. On the other hand, when $\Phi = V_{DD}$ both the transistor M_7 and M_8 turns on but keeps M_5 and M_6 transistors in saturation region as both of these transistors gates still hold the value V_{DD}, since V_{DD} is the output during the previous phase, namely the reset phase. The inputs of the left and right branches formed by $M_1 - M_4$ determines whether the output holds the value V_{DD} or 0V. Since $M_1 - M_4$ are in deep linear region, while M_5 and M_6 are in the saturation region, the input-referred offset is sensitive to the device mismatch of $M_1 - M_4$ and especially $M_5 - M_6$. The offset can reach hundreds of millivolts, which is unbearable in a multi-bit quantizer.

Another fully differential dynamic comparator is depicted in Figure 4.26 [60]. The comparator consists of two cross coupled differential pairs with inverter latch at the top. All of the differential pairs and current source transistors are in the saturation region at the regeneration time, which makes the offset insensitive to device mismatch. The trip point of the comparator depends on the imbalance between the differential pairs and the switch controlled current sources. However, several drawbacks compromise its application. If there are any non-idealities or mismatches present, the two inverter tail currents will not be same and will result in large offset for the comparator. The second problem is related to the inputs of the differential pairs. A large difference between the two inputs to a differential pair will result in the turning off one of the differential pair transistor and all the tail current will be drawn into the other transistor. Hence, the comparator will be only

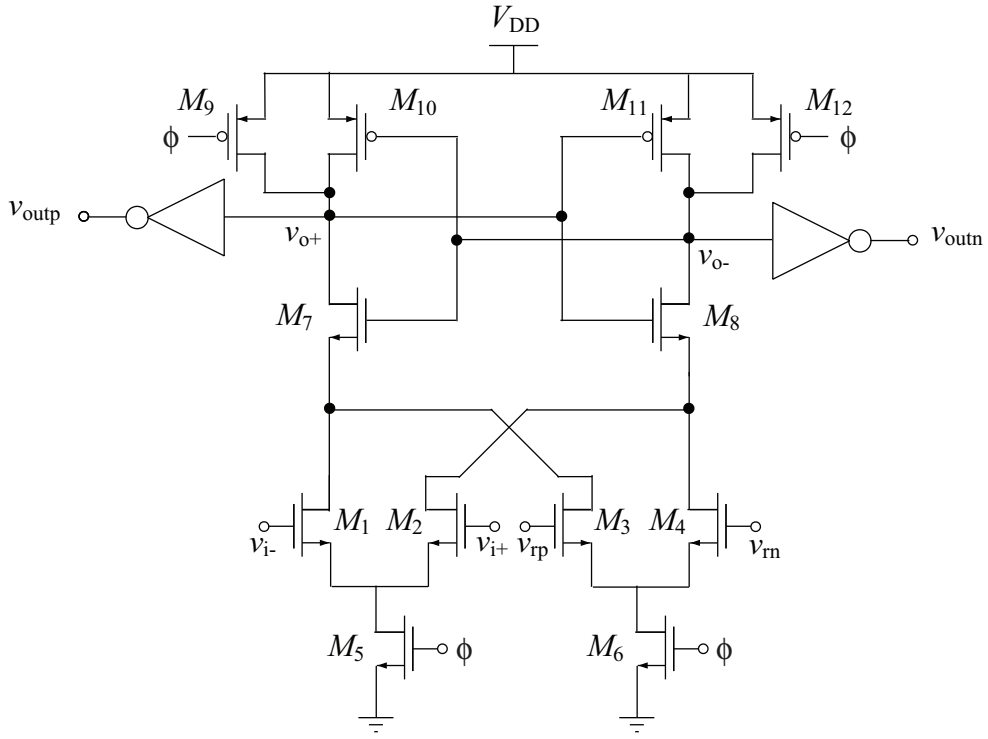


Figure 4.26: Differential pair comparator.

comparing v_{i+} with v_{rp} (or v_{i-} with v_{rn}) rather than a comparison of differential v_i with differential v_r.

4.4.3 Proposed Comparator

To overcome the drawbacks of the two dynamic comparators mentioned above and to exploit their advantages, some improvements are introduced to make the proposed comparator not only insensitive to device mismatch but also capable of operating at lower supply voltage and larger input swing. The proposed comparator is shown in Figure 4.27.

One key point in designing this comparator is the aspect ratio of the switches M_5 and M_6 which should be designed large enough in order to make the delay introduced by the comparator as small as possible. In fact, by increasing the size of the current source transistors, the time constant connected to the charging of the output capacitor will be smaller, and, therefore, a faster switching activity between the two supply voltages takes place. The effect of increasing the size of transistors M_5 and M_6 on the comparator output of Figure 4.27 is shown in Figure 4.28.

The operation of the comparator is as follows. When the comparator is in the reset phase, namely $\Phi = 0$, M_5 and M_6 are in cut-off region. There is no static current from V_{DD} to ground, as in the resistive divider dynamic comparator. During this phase M_9 and M_{12} are in conducting mode. The nodes v_{o+} and v_{o-} are pulled up to V_{DD}, therefore the output voltage v_{outp} and v_{outn} is pulled down to 0.

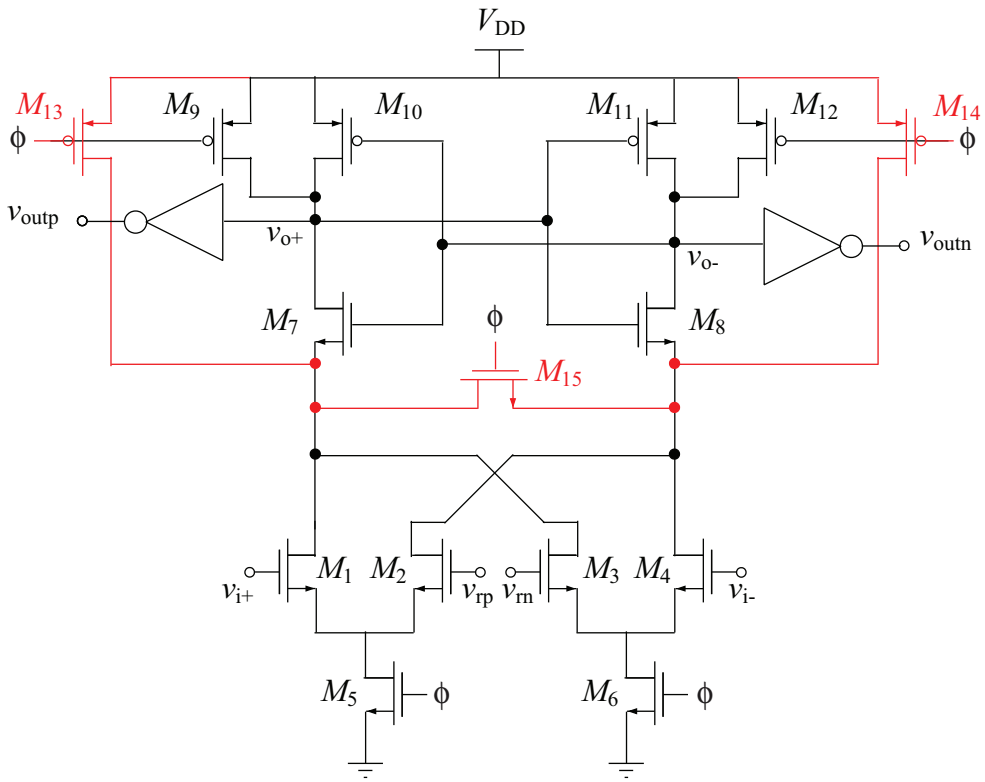


Figure 4.27: Proposed dynamic comparator.

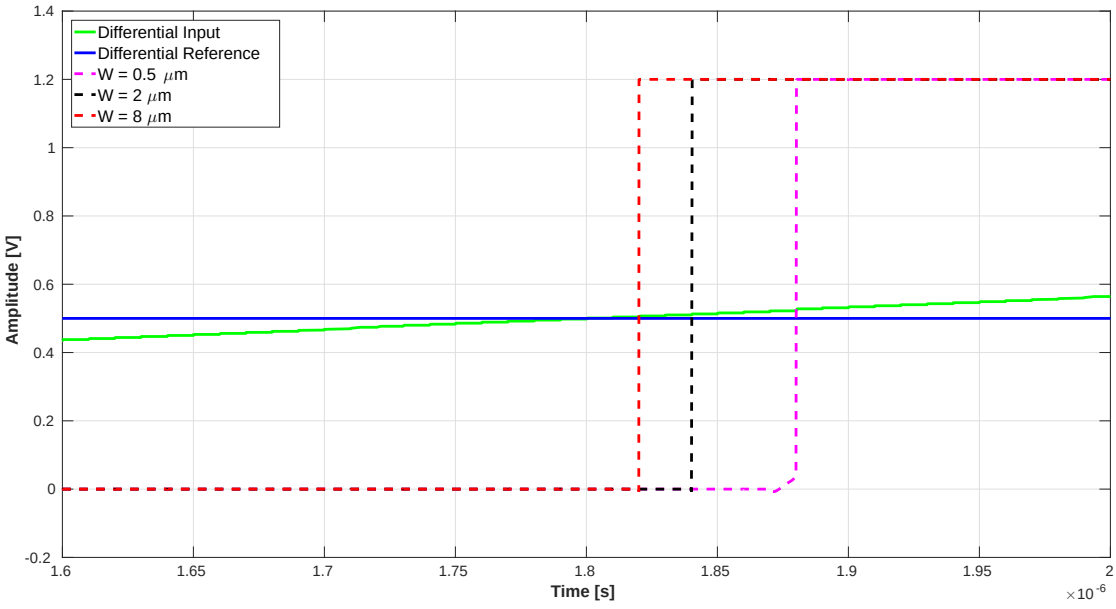


Figure 4.28: Positive output of the proposed dynamic comparator in function of the size of the switches M_5 and M_6.

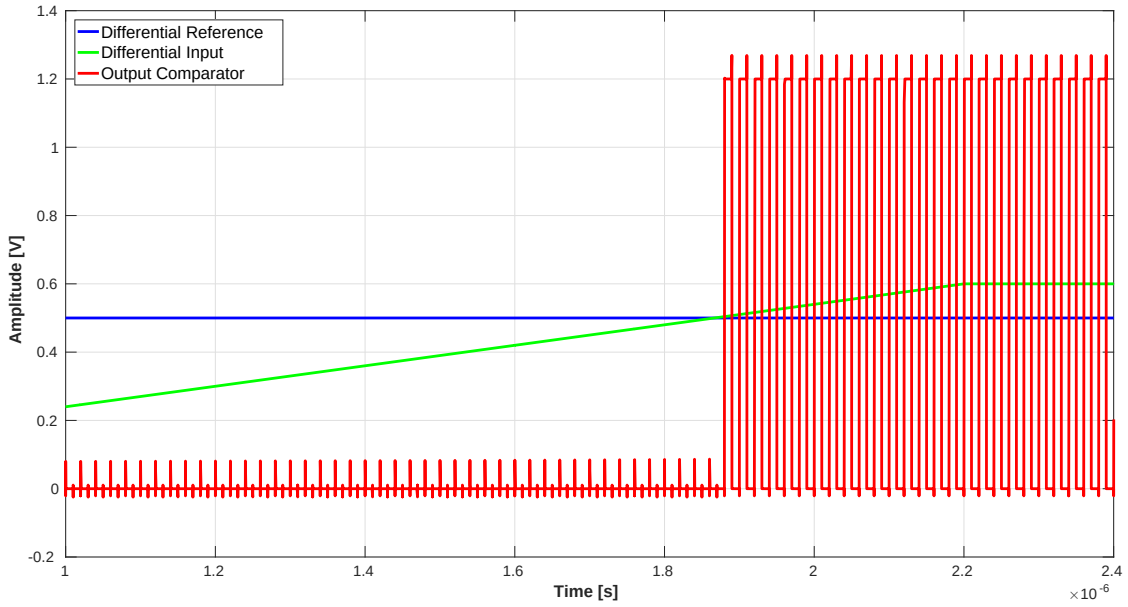


Figure 4.29: Positive output of the proposed dynamic comparator.

Once Φ goes high, the sources of the differential pairs are pulled down by switches M_5 and M_6, while the drain of the differential pairs are still close to V_{DD} because of no transient current from V_{DD} to ground at the start of the regeneration phase. Therefore transistors $M_1 - M_4$ are in the saturation region at this moment. In the meantime, the comparator begins to compare the input voltage and reference voltage. As in the resistive divider comparator the ratio of the sizes of the input transistors determines the trip point, as in Equation (4.17). However, in this case, unlike the resistive divider case, the input transistors are operating in the saturation region. Few modifications have been made to this structure if compared to the differential dynamic comparator. The most important modification is related to the input signals. As pointed out in the typical differential pair comparator, one of the input transistors will be turned off if there is a large input differential and will result in the comparison of two signals rather than comparison of two differential signals. To address this problem v_{i+} and v_{rp} (and v_{i-} and v_{rn}) are combined in one differential pair. Transistors M_{13} and M_{14} are included to reduce the effect of the mismatch of M_7 and M_8 on the input-referred offset. In fact at the end of the reset phase the sources of M_7 and M_8 are connected to V_{DD}. Since also v_{o-} and v_{o+} are pulled up to V_{DD}, transistors M_7 and M_8 are in the linear region. Therefore their mismatch becomes much less important. It is worth to notice that, during the reset phase, the sources of M_7 and M_8 are shorted for the purpose of eliminating the effect of last comparing result to the next decision, namely the recovery-time issue.
The functional performance of the proposed dynamic comparator is shown in Figure 4.29.
As apparent from Figure 4.29 when the differential reference is greater than the differential input the positive output is 0, regardless of the clock phase. When the differential input becomes greater than the differential reference the output is 0

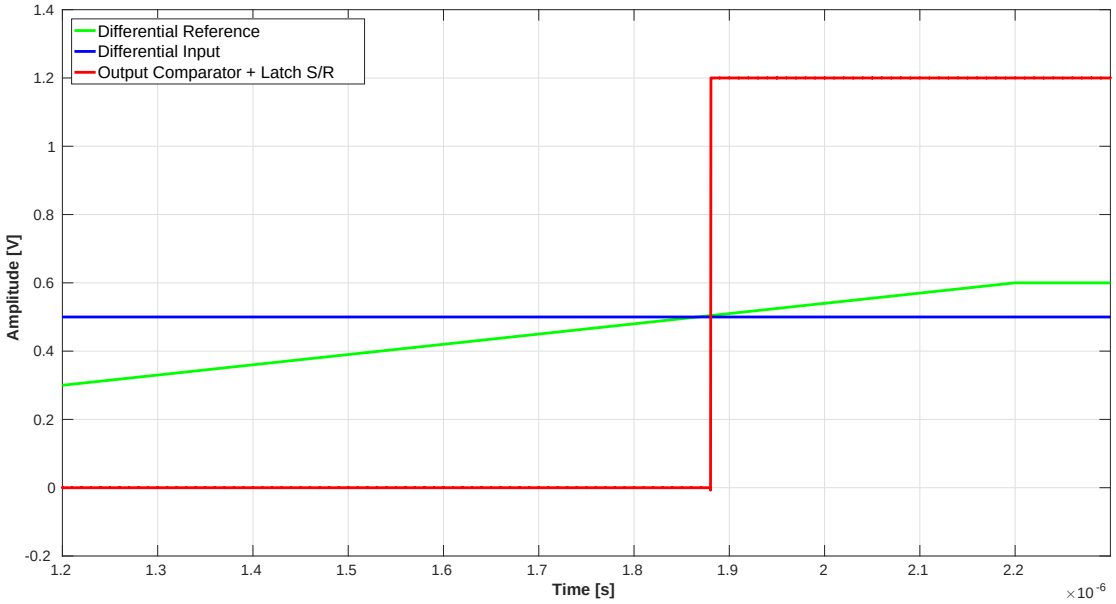


Figure 4.30: Output of the Set-Reset Latch after the comparator.

during the reset phase, while during the regeneration phase is equal to V_{DD}.
In order to generate the thermometric code, a Set-Reset Latch has been used to hold the correct output value for the entire clock cycle. The effect of the Set-Reset Latch is shown in Figure 4.30.
In order to evaluate the comparator offset and hysteresis a slow ramp-waveform input signal is applied to the comparator, with a Montecarlo approach. The simulation is depicted in Figure 4.31.
From Figure 4.31 it is possible to evaluate the offset and the hysteresis of the comparator.

$$v_{os} = \frac{v_{i1} + v_{i2}}{2} - v_{th} = \frac{0.5411 + 0.4768}{2} - 0.5 = 0.009\text{V}$$
$$v_h = \frac{v_{i1} - v_{i2}}{2} = \frac{0.5411 - 0.4768}{2} = 0.03\text{V} \tag{4.18}$$

The offset of the comparator has been evaluated also with an histogram, as shown in Figure 4.32.
As apparent from Figure 4.31 and Figure 4.32 this topology effectively ensures a very low offset.
The simulation regarding the overall quantizer is depicted in Figure 4.33. As for the offset evaluation, this simulation is performed with a slow ramp-waveform input signal. As apparent, the differential non-linearity coincides with DNL = 0 LSB, which ensures a monotonic transfer function with no missing codes. The simulated INL for the quantizer is INL = 0 LSB. Even looking at the Montecarlo simulation, as in Figure 4.34, the DNL is low enough to ensure the monotonicity of the quantizer. Since it would be impossible to perform a Montecarlo simulation of

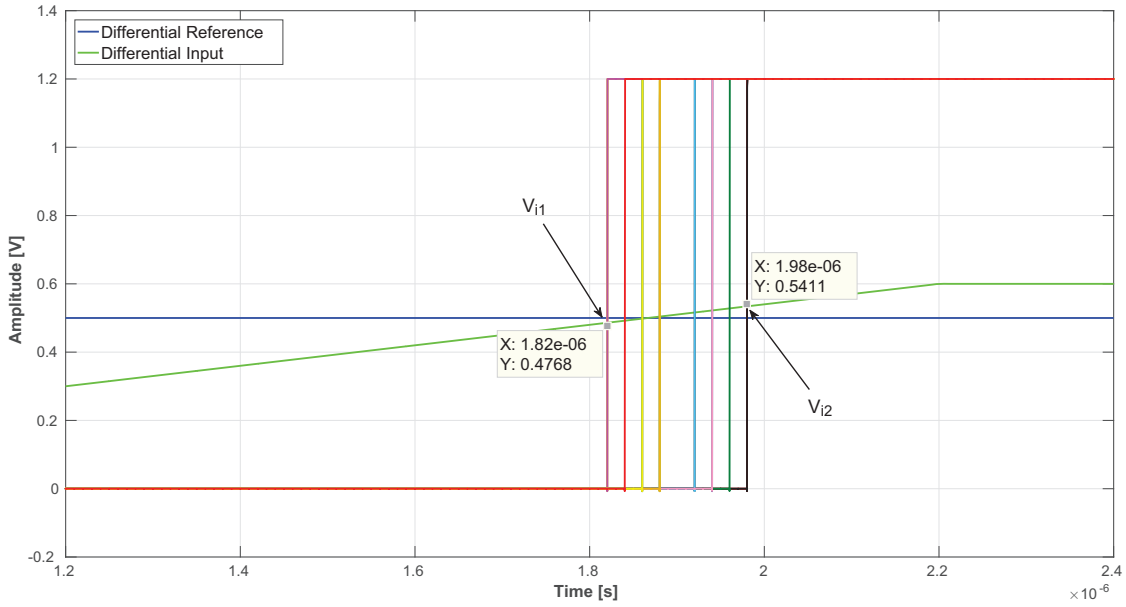


Figure 4.31: Montecarlo simulation of the output transient response of the comparator.

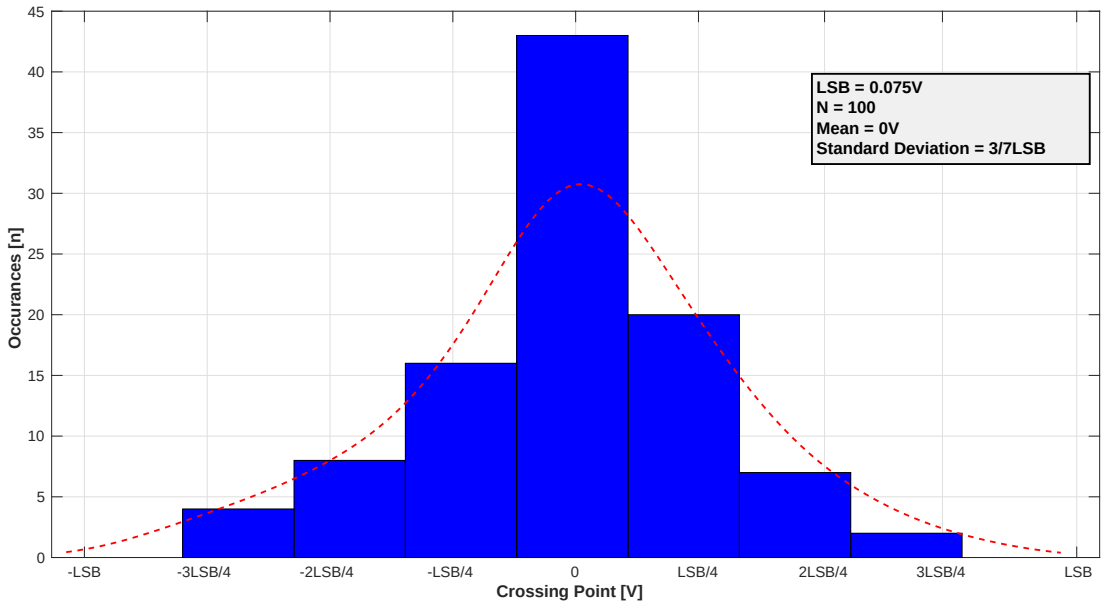


Figure 4.32: Histogram of the offset of the comparator.

the overall $\Sigma\Delta$ modulator, the non-linearity of the 5 bit flash quantizer has been integrated into the *MATLAB* model, with the aim of evaluating the effects of this non-linearity on the output SNDR. These effects do not degrade the performance of the overall modulator, as expected since this element takes advantage of the second-order noise shaping and therefore its performances are relaxed.

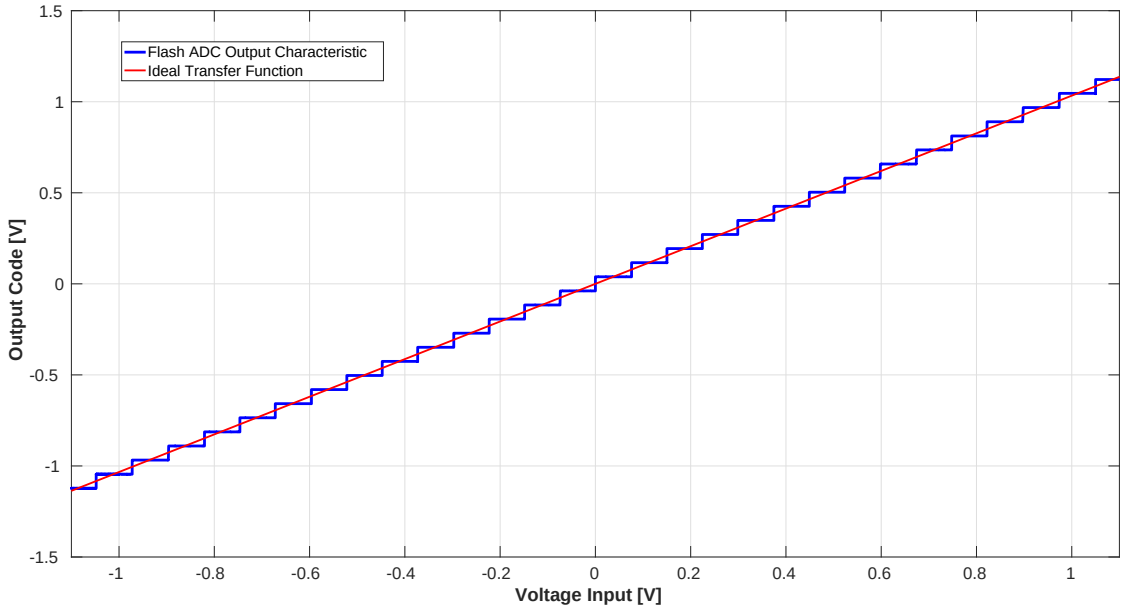


Figure 4.33: Input/Output Characteristic of the 5 bit embedded quantizer.

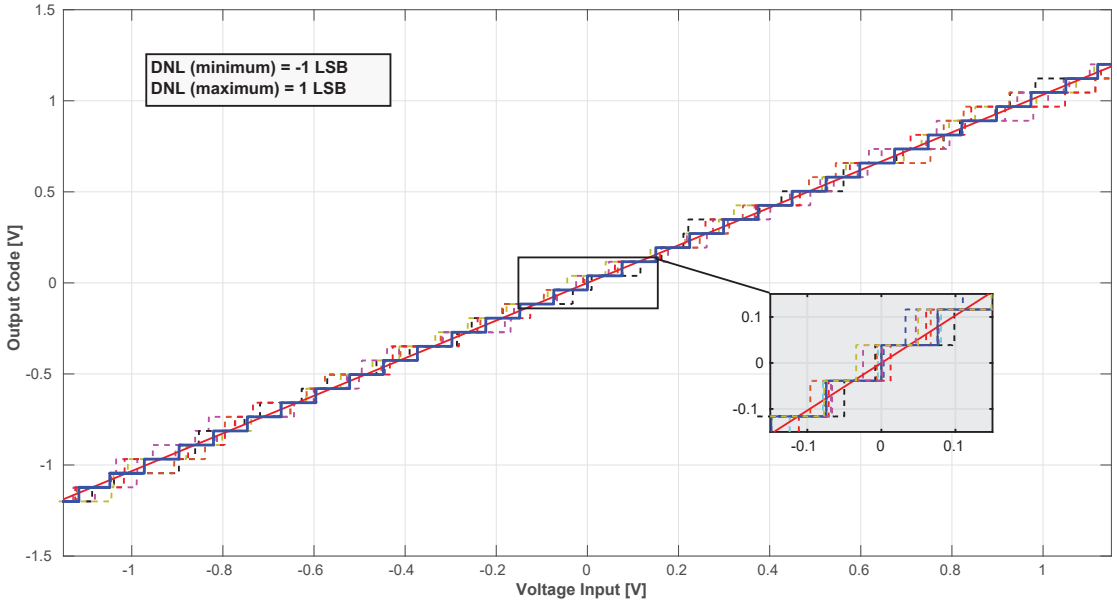


Figure 4.34: Montecarlo simulation of the input/output characteristic of the 5 bit embedded quantizer.

Also the overall power consumption has been simulated and the power consumption of the overall quantizer is $P = 72\mu$W.

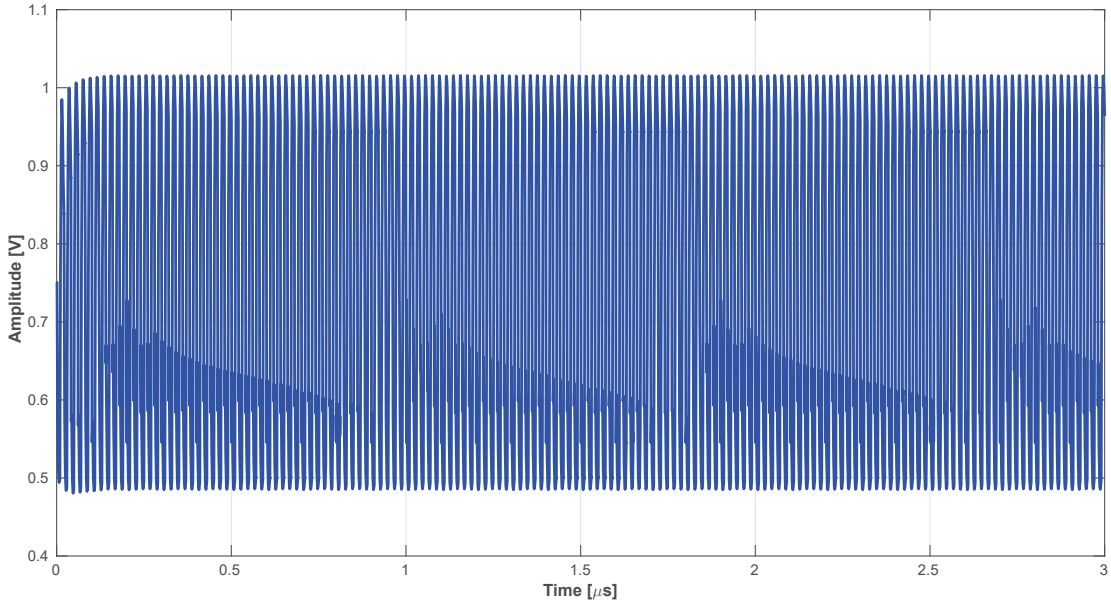


Figure 4.35: Voltage reference glitch caused by kickback noise.

4.4.4 Reference Voltage Generation

Besides the offset, the major problem of a general dynamic comparator is the already mentioned kickback noise effect. Without a pre-amplifier that isolates the switching activity of the latch from the input voltage, the comparator works wrong because of the input reference glitch. The effect of the kickback noise on the reference voltage is shown in Figure 4.35.
As apparent from Figure 4.35 the reference voltage has a large variation with respect to its nominal value, namely for this simulation case $V_{ref} = 0.75$V. Furthermore, this voltage variation exceeds the LSB, which for a 5 bit internal quantizer with a reference voltage of 1.2V is only 75mV. This implies that the comparator output gives an incorrect digital value and, therefore, the overall system makes a mistake much larger than the LSB.
A way to solve this problem is by paralleling a small capacitor with the differential pair. Hence, the glitch caused by the kickback noise effect is reduces effectively. Therefore, the generation of the reference voltages for the flash ADC includes, beside the classical resistive ladder, 31 capacitors for each reference voltage. The reference voltage generation is shown in Figure 4.36. In order to reduce the current consumption of the resistive ladder a high resistor, namely $R = 31k\Omega$ is used. Therefore a current consumption on the resistive ladder of 1.2μA is obtained. The capacitor size has been chosen in order to reduce the kickback noise leading to $C = 180$fF. As apparent from Figure 4.37, the proposed solution to reduce the kickback noise is effective, since a sensible reduction of the voltage variation over the reference voltage is obtained. As shown in Figure 4.37 the disturbance on the reference voltage is reduced to only 3mV.

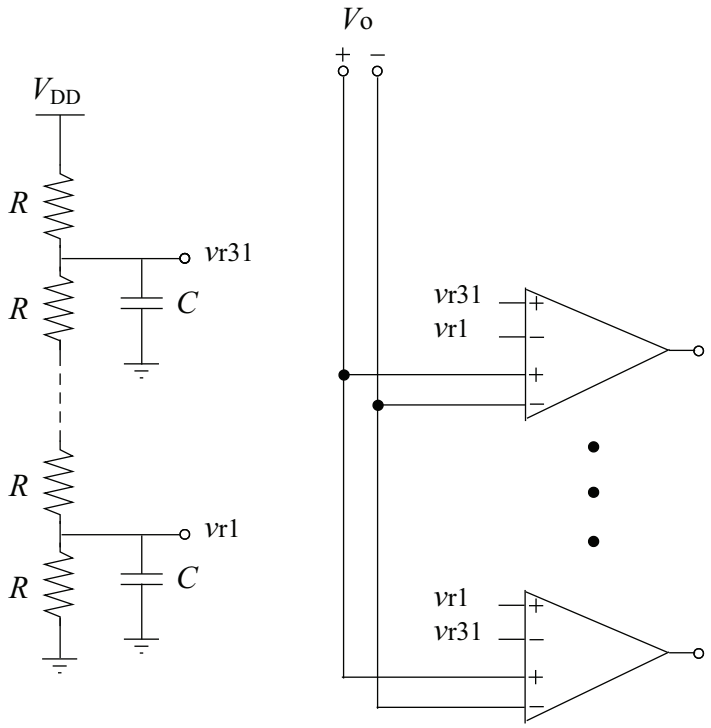


Figure 4.36: Reference voltage generation for the 5 bit internal quantizer.

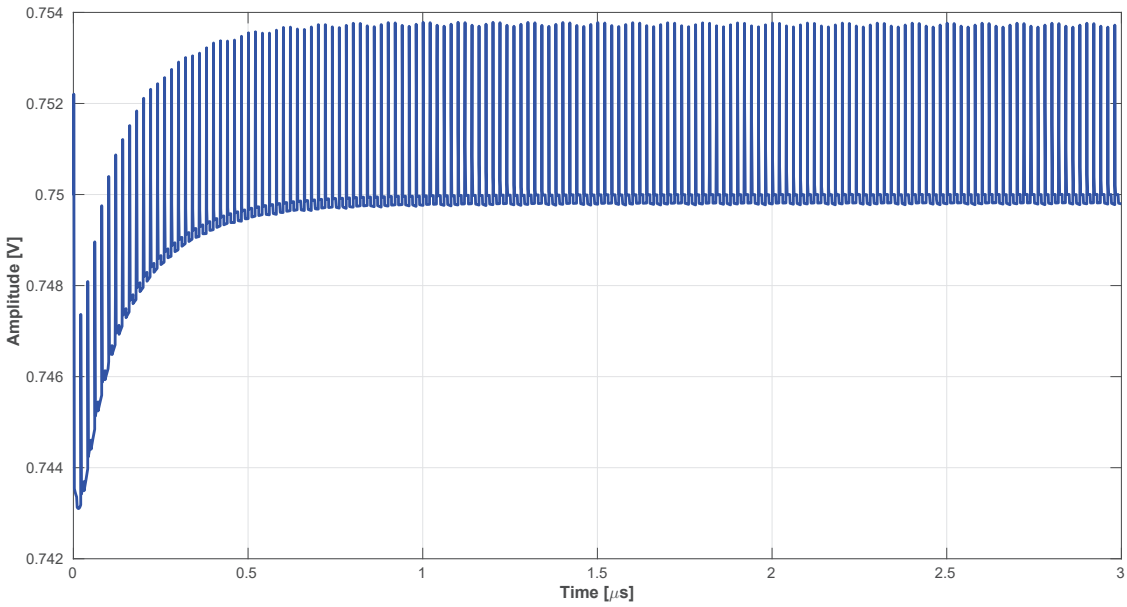


Figure 4.37: Reduced voltage reference glitch caused by kickback noise with the capacitor solution.

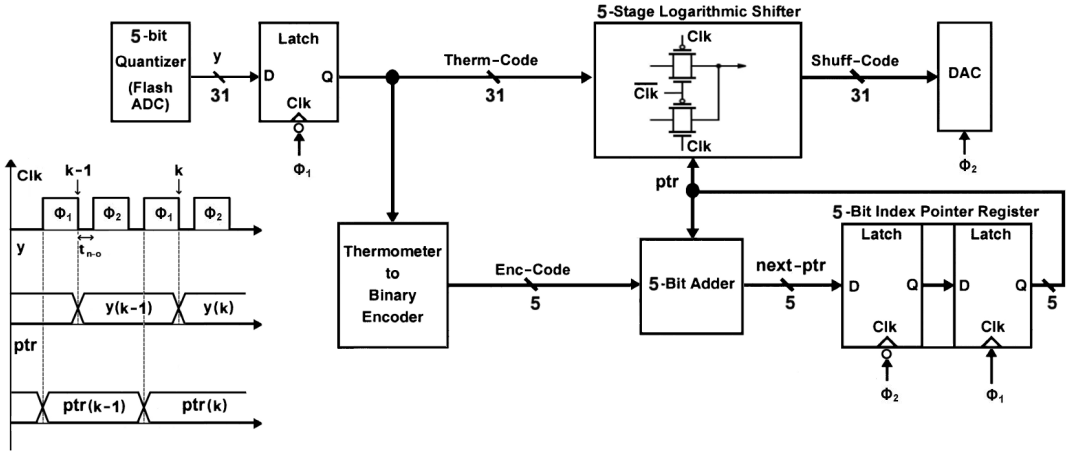


Figure 4.38: An optimized implementation of the first-order DWA algorithm.

4.5 Digital Circuitry

4.5.1 DWA

As already discussed in Chapter 3, the DWA algorithm is one of the most used DEM algorithm thanks to its simplicity. In Figure 4.38 an optimized physical implementation for the first-order DWA is proposed. The 31 bits of the thermometer code generated by the $\Sigma\Delta$ flash ADC, *Therm-Code*, can be permutated by means of a simple logarithmic shifter [61], using the proper value of the pointer.

4.5.2 Logarithmic Shifter

The implementation of the logarithmic shifter is shown in Figure 4.39. For the sake of clarity a three bits logarithmic shifter is depicted, while in the design a 5 bit shifter is actually used. Depending on the value of the pointer, *ptr*, the input thermometer code is shuffled, so that the shuffled code is shifted of $(ptr)_{10}$, where $(ptr)_{10}$ is the decimal representation of the code *ptr* [61]. An example of the operation of the barrel shifter is shown in Figure 4.40, where the thermometer code is shifted of $(101)_{10} = 5$ positions. As it will become more clear below, this block is a key element for the hardware implementation of the DWA and it must be ensured that the time delay introduced by the logarithmic shifter is minimized.

4.5.3 Binary Encoder

The pointer value is converted from a thermometer code into a binary one with an encoder [62]. The implementation of the Binary encoder is depicted in Figure 4.41. For the sake of clarity a three bits encoder is depicted, while in the design a 5 bit encoder is used. The encoder implementation is based on multiplexers (MUX). The main idea behind this design of the proposed MUX based encoder is to group the results of smaller length MUX-based encoders to form a larger encoder for thermometer to binary conversion. Consider the example of Figure 4.42. The

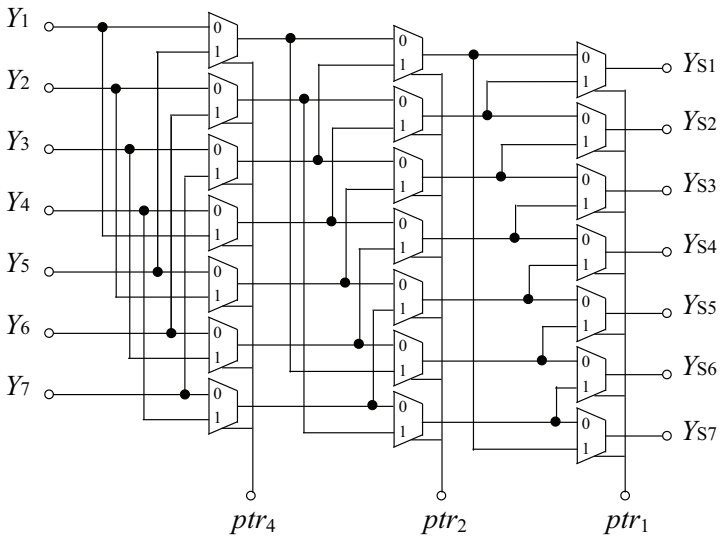


Figure 4.39: Three-stage multiplexer based logarithmic shifter.

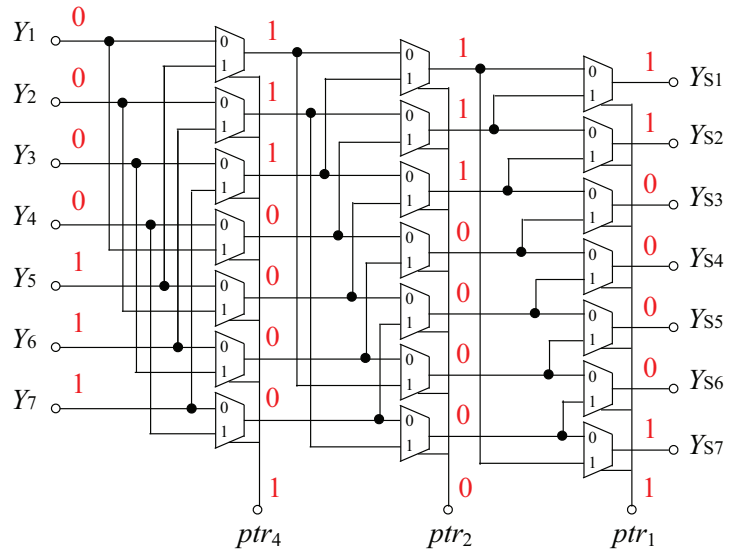


Figure 4.40: An example of the basic operation of a three-stage logarithmic shifter.

thermometer code is given by 0000111. Since the Y_4 signal is 0 all the bits to the left side of Y_4, namely $Y_{1,2,3}$, are 0, therefore the MSB of the binary code is equal to 0. The LSB bits Y_{LSB} and Y_{LSB+1} are now defined by the number of 1 present in the right side of Y_4, which is equal to three. This now represents the LSB bits of the final binary code. Since the basic operation of the proposed MUX based decoder needs a bubble correction circuit for correcting the bubble errors, an array of OR logic ports is used in order to correct a possible single bubble error.

Among the existing thermometer-to-binary encoders the proposed design offers the smallest power consumption and the smallest area [62].

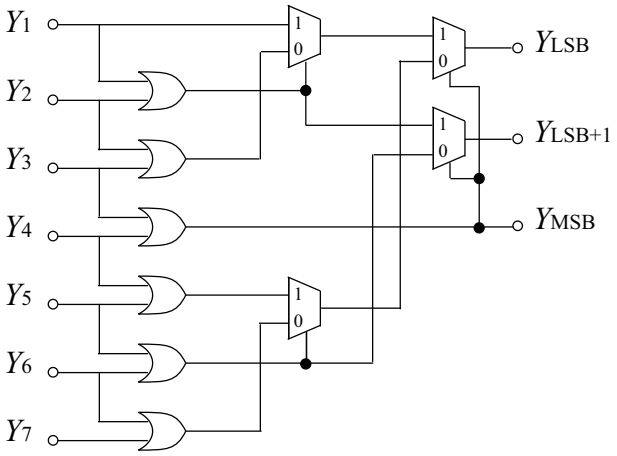


Figure 4.41: Three bits MUX based encoder.

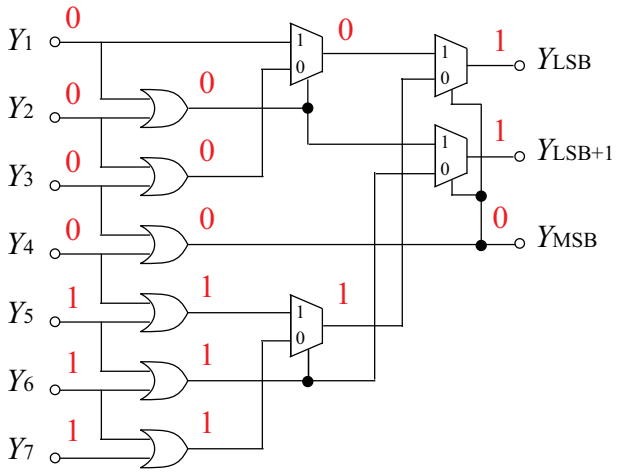


Figure 4.42: An example of the basic operation of a MUX based encoder.

4.5.4 Full Adder

In order to update the pointer value a 5 bit adder must be used [63,64]. In the DWA algorithm the pointer value is updated according to Equation (4.19)

$$ptr(k) = (ptr(k-1) + y(k-1)) \bmod 2^N. \tag{4.19}$$

The design of the adder is depicted in Figure 4.43. It has 16 transistors and it is based on the 4-transistor implementations of the XOR and NXOR functions presented in [63].
It is easy to verify that the nodes X, Y, Z implement the following functions

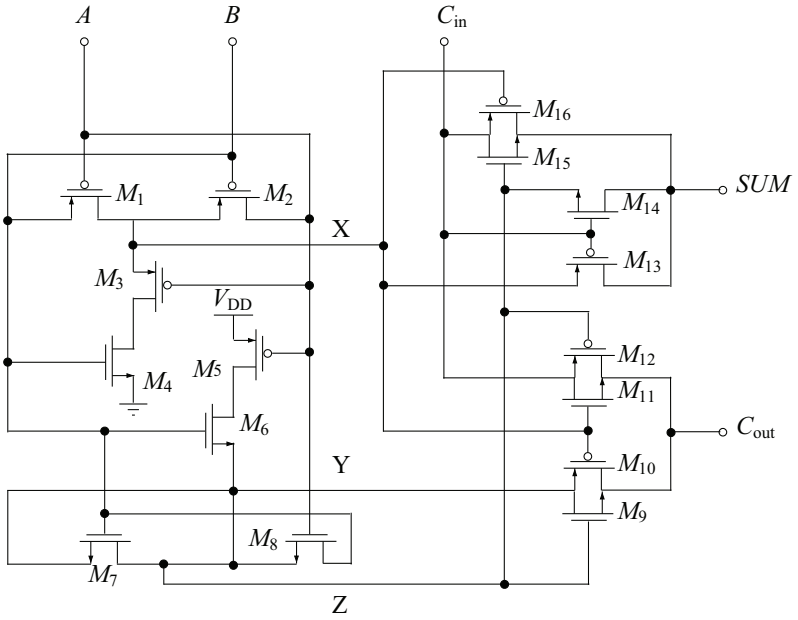


Figure 4.43: Single cell 5 bit full adder.

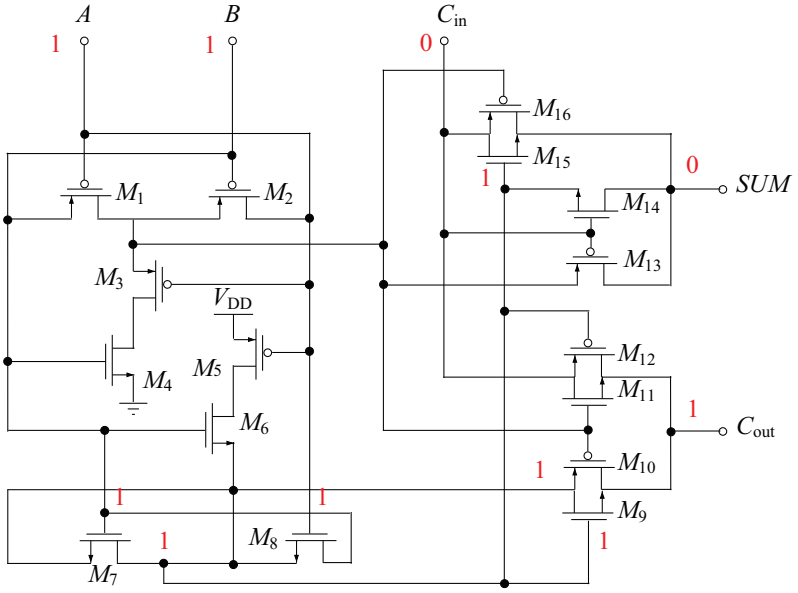


Figure 4.44: An example of the basic operation of the single-cell full adder.

$$\begin{aligned} \mathrm{X} &= \mathrm{A}\ \mathit{XOR}\ \mathrm{B} \\ \mathrm{Y} &= \bar{\mathrm{A}}\ \mathit{XOR}\ \mathrm{B} \\ \mathrm{Z} &= \mathrm{X}\ \mathit{XOR}\ \mathrm{C_{in}} \end{aligned} \tag{4.20}$$

From Equation (4.20) it yields

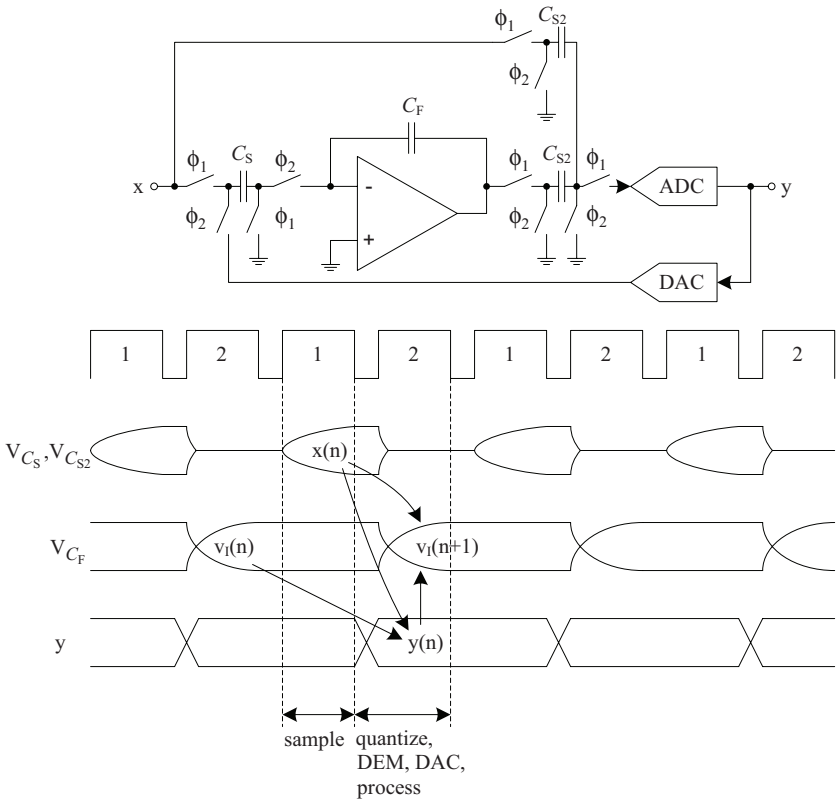


Figure 4.45: First-order FF ΣΔ modulator with input feedforward and its timing diagram.

$$\begin{aligned} \text{SUM} &= (\text{A } \mathit{XOR} \text{ B}) \mathit{ XOR } \text{ C}_{\text{in}} \\ \text{C}_{\text{out}} &= \text{A} \cdot \text{B} + \text{C}_{\text{in}} \cdot (\text{A } \mathit{XOR} \text{ B}) \end{aligned} \tag{4.21}$$

which is actually the 1 bit full-adder functionality. An example of how this full adder works is depicted in Figure 4.44.

4.5.5 Timing Requirements

One of the challenges in the implementation of the ΣΔ architecture is the timing of the feedback loop path [65]. Considering the architecture of the design proposed in this thesis, it must be ensured that the output of the quantizer becomes available before the start of the integration phase of the first amplifier, as already mentioned. This constraint is due to the need of having a delay-free signal transfer function and, as a result, a removal of the input signal component which allows to use more efficient opamp architectures. This problem becomes worse with the use of DEM algorithms [66]. To understand this timing limitation the implementation of a first-order FF modulator and its timing diagram is depicted in Figure 4.45.
The quantizer output thermometer code y becomes available at the end of clock phase Φ_1, being Φ_1 and Φ_2 the two non-overlapping clocks of the switched-capacitor integrators included in the ΣΔ modulator. The shuffled version of this code drives

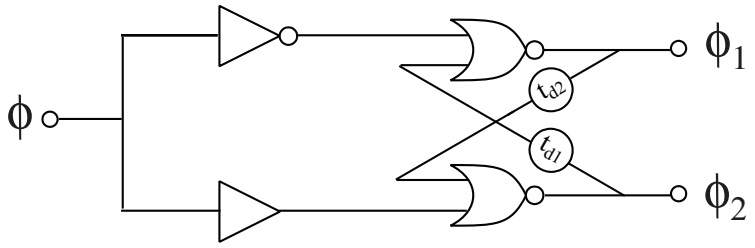


Figure 4.46: Physical implementation of the circuit used to generate the two non-overlapping phases.

the modulator DAC and must be stable at the beginning of Φ_2, when the integration phase of the first amplifier starts. Therefore the permutation of $y(k)$ bits must be performed within the non-overlapping time of the clock phases, t_{n-o}. In the literature several solutions to avoid this timing delay issue are proposed, however they are often based on a modification of the analog part that involves a substantial increase of the power consumption [67,68].
Given that the timing issue in the cancellation logic may be critical, the selection of the most adequate DEM algorithm must also consider the hardware implementation, with particular emphasis on the time requested for the permutation of the thermometer code bits [69].
As highlighted in the timing diagram of Figure 4.38 the propagation through the shifter starts at the end of phase Φ_1 and must be completed within the rising edge of phase Φ_2, when the DAC must provide a stable signal to the modulator. The shifter propagation time corresponds in the worst case to the delay of the cascade of five transmission gates.
Assuming that the two non-overlapping clock phases are generated with the circuit reported in Figure 4.46, the non-overlapping period, t_{n-o}, is equal to the propagation time through the two delay chains t_{d1} and t_{d2}. When such delay chains are realized cascading few CMOS inverters it is easily obtained that the propagation delay through the five transmission gates of the shifter is slightly lower than t_{n-o}.
When a new value of *Therm-Code(k)*, or equivalently $y(k)$ as depicted in the time diagram of Figure 4.38, is generated on the falling edge of Φ_1 it also triggers an update of the pointer *ptr*. Such a new value of *ptr* is actually used for the permutation of the next value of the input code *Therm-Code(k+1)*, therefore all the hardware blocks in the lower part of Figure 4.38 have a much relaxed time constraint. In particular, in the proposed realization, the 5 bit adder must provide a stable signal to the following master-slave register at the falling edge of Φ_2: hence a time span as long as half the clock period is available. This proves that in the case of the DWA algorithm, the time criticality is limited to some simple digital blocks and hence it can be easily managed [70].
Conversely, for instance, a second-order DWA suffers of a more complex hardware implementation: in fact this algorithm requires that some unit elements contribute multiple times in one clock cycle. This implies that the clock period is divided into sub-periods and in each of these sub-periods, a specific unit element can have either

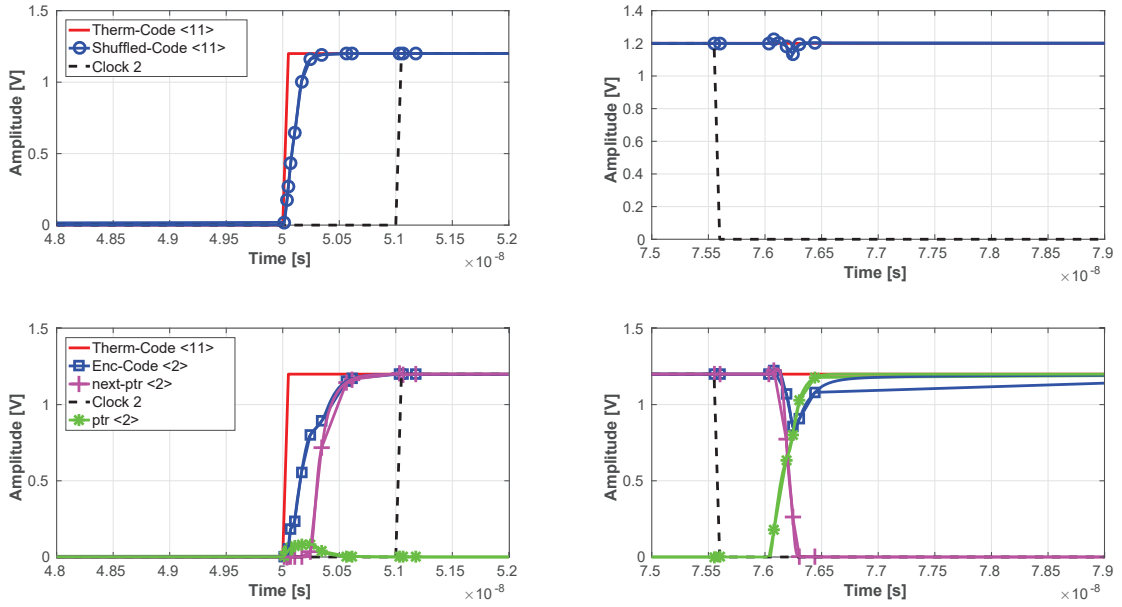


Figure 4.47: Transient simulation of the 11th bit of signals *Therm-Code* and *Shuff-Code* and of the 2nd bit of signals *Enc-Code*, *ptr*, and *next-ptr*; the time axis is divided in two sets, in order to zoom around the rising and the falling edge of phase Φ_2, respectively.

a positive, negative or zero contribution. This strategy degrades the maximum clock speed of the converter and in particular it becomes almost impossible to satisfy that all the necessary operations are performed within the t_{n-o} period. This fact motivates why the second-order DWA, despite being the most performing solution among all the DEM algorithms, is not commonly used in the literature.
The 5 bit adder and the thermometric encoder, being outside the critical path, can be designed with the target of area and power consumption saving, as previously explained.
Some transistor-level simulation results using the foundry models are presented in Figure 4.47. At time 50ns an update of *Therm-Code* occurs due to the high-low commutation of phase Φ_1. As shown, the signal *Shuff-Code* converges to its new value well before the next rising edge of Φ_2, as required by the critical timing schedule. Then it remains constant until a new value of *Therm-Code* will arrive. Signals *Enc-Code*, *ptr*, and *next-ptr* are also plotted in the lower part of Figure 4.47. Signals *Enc-Code*, and *next-ptr* are updated as a consequence of the *Therm-Code* variation with no timing issues at all, since *ptr* will be sampled by the index pointer register at the falling edge of Φ_2, which occurs in the right side graphs of Figure 4.47. After this latter event, the new value of *ptr* is available (after the rising edge of Φ_1). The same bit permutation has been simulated with a multiplexer in the barrel shifter realized with a nMOS pass transistor logic, followed by a level restorer in order to restore the high logical level. However, with this kind of solution, the delay time is increased in the signal path as apparent in Figure 4.48.

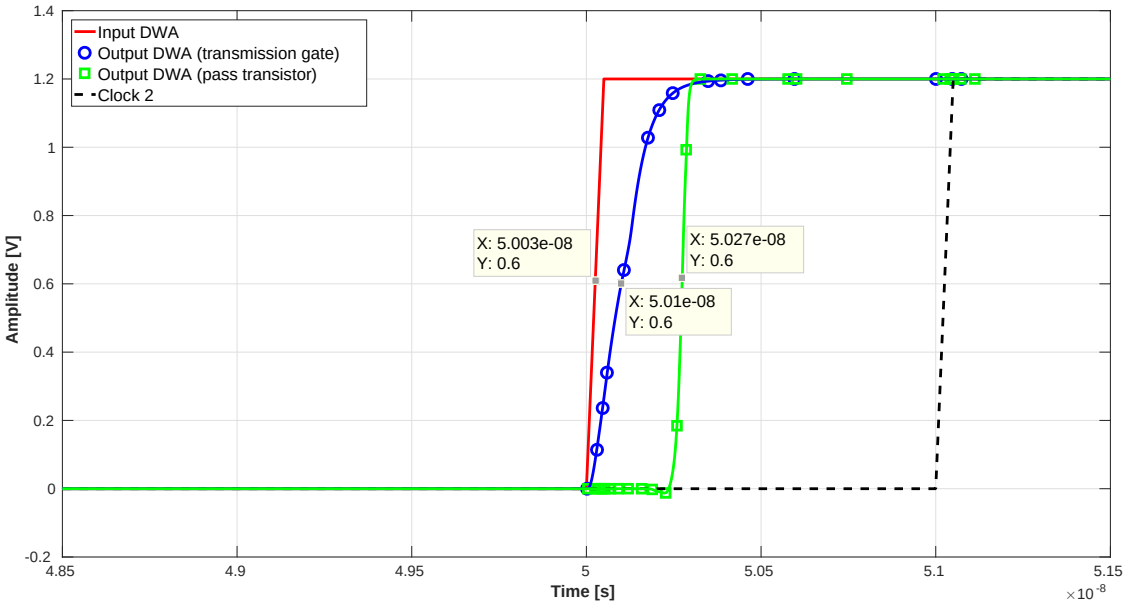


Figure 4.48: Transient simulation of the delay introduced by DWA when the logarithmic shifter is implemented with pass transistor or transmission gate logic.

4.5.6 BiDWA

As already discussed, the main drawback of DWA is the presence of spurious tones in the signal bandwidth for low OSR. The most efficient solution to solve the harmonic behavior of DWA is the BiDWA. The critical point of BiDWA is, however, its hardware implementation. In fact the need to implement the two pointers requires to double the hardware with respect to DWA, allowing the barrel-shifter to shift in two directions. Beyond the power and area increase due to the larger number of logic gates, the circuit of Figure 4.49 can easily become critical in terms of timing.
Considering the critical signal path from the quantizer output, y, to the DAC input, it is worth to observe that, with respect to the circuit solution of Figure 4.38, the extrinsic load of the first latch has been doubled and a multiplexer at the end of the signal path has been added. This results in a significant increase of the propagation delay that, as stated earlier, must be lower than the non-overlapping period of the clock phases Φ_1 and Φ_2. In Figure 4.50 simulations at the transistor level are performed order to compare the delay in the signal path for the BiDWA and the DWA algorithms.
It is apparent that the delay introduced by the BiDWA algorithm is larger than the DWA solution.
This fact is justified by two elements. Firstly, the additive multiplexer increases the time propagation. The effect of this additive multiplexer becomes even more evident when a large number of bits N is used. In fact the time propagation through a sequence of N transmission gates is given by

$$t_p = 0.69 \cdot C \cdot R_{eq} \frac{N(N+1)}{2}, \tag{4.22}$$

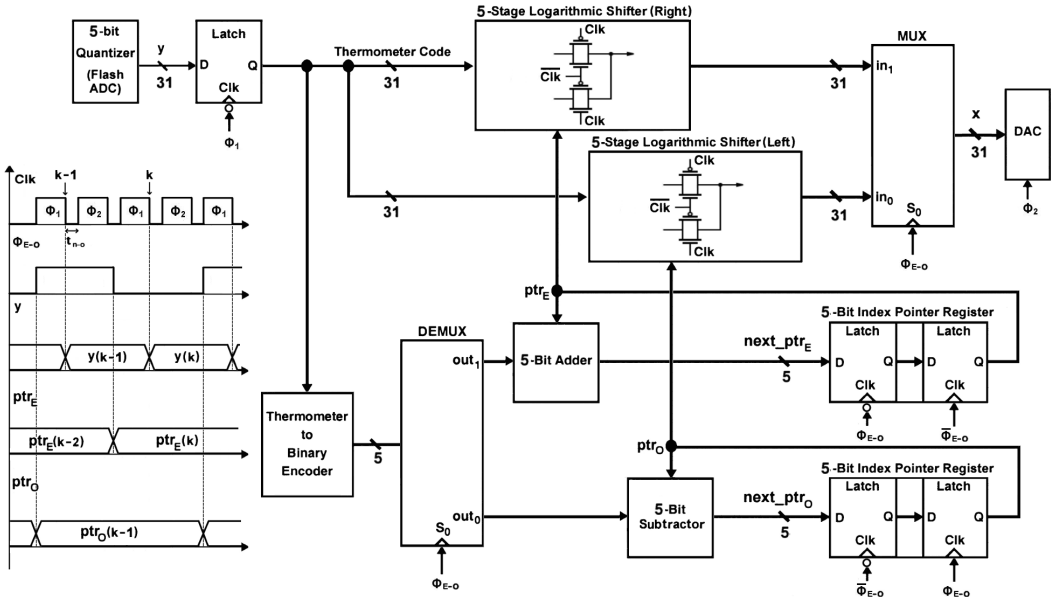


Figure 4.49: Implementation of the BiDWA algorithm.

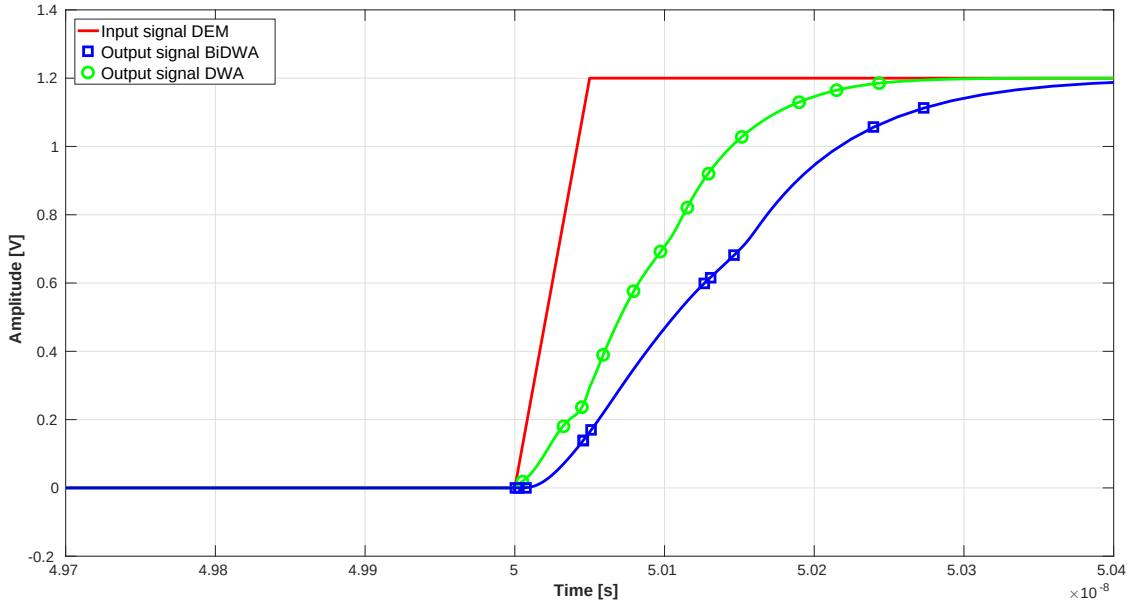


Figure 4.50: Feedback delay introduced by DWA and BiDWA algorithm.

which shows that there is a quadratic dependence between the propagation time and the number N of elements in the barrel shifter. Secondly the load seen by the 5 bit quantizer increases in the BiDWA. One may argue that the load seen by the 5 bit quantizer can be reduced with a demultiplexer before the two barrel shifters. However this solution has been investigated and leads to a further increase of the delay in the signal path.
This problem in the time delay, combined with the area and power consumption, has in fact made the BiDWA a rarely used algorithm in the literature.

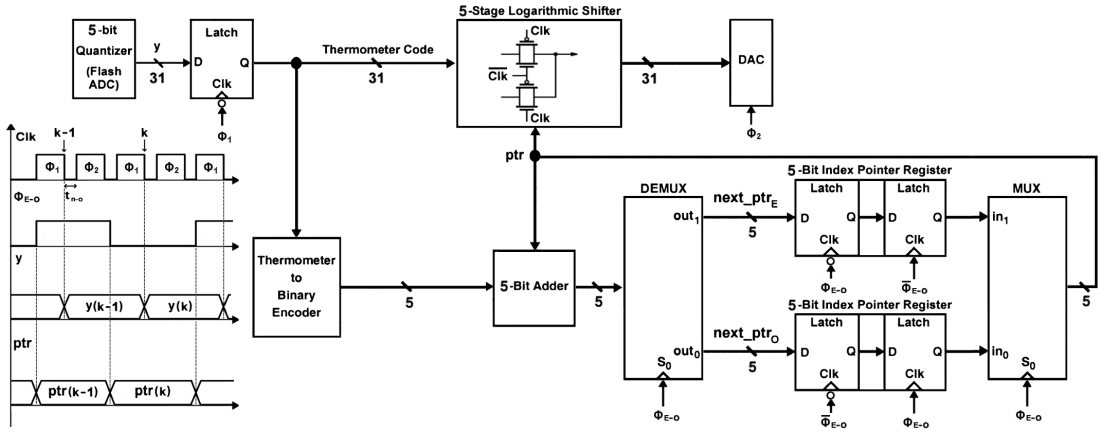
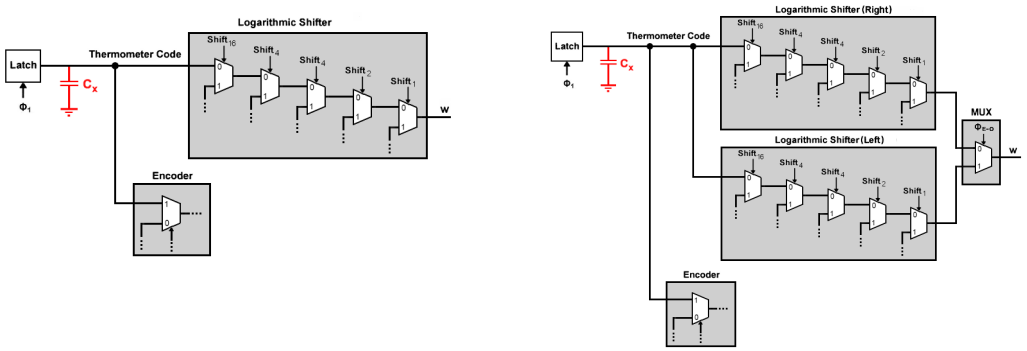


Figure 4.51: Implementation of the NewDWA algorithm.

4.5.7 NewDWA

As explained in Chapter 3.3.4 the NewDWA has the same efficiency of the BiDWA and, therefore, can be considered as a good solution for the low OSR applications. It was also already shown how intuitively the proposed algorithm has an easier hardware implementation in comparison with the BiDWA algorithm. The details of the hardware implementation of the NewDWA are given below and the time delay introduced by this algorithm is compared with the one of DWA and BiDWA.
The implementation of the proposed algorithm is shown in Figure 4.51.
The scrambling operation is performed with the classical logarithmic shifter. The 5 bit adder sums *ptr* with the encoded thermometric code. During Φ_{E-O} the output of the adder passes through the out_1 path of the demultiplexer as the next ptr_E. The pointer is stored in the master stage of the 5 bit index pointer register of the even pointer path, while the output of the slave latch is locked, ensuring a stable pointer *ptr* to the logarithmic shifter. It should be noted that in this phase the master stage of the register of the odd pointer is disabled, therefore the odd pointer is not modified during this phase. During $\bar{\Phi}_{E-O}$ the slave stage of the register of the even pointer is enabled and captures the signal stored in the master stage. This ensures that $next\text{-}ptr_E$ is stable and available unchanged for the next Φ_{E-O} phase, when the multiplexer selects the path in_1. The behavior of the odd path is similar. In this case it is needed to ensure a stable pointer during $\bar{\Phi}_{E-O}$, therefore the phases of the master-slave registers of the odd pointer path are reversed. The afore mentioned timing criticality still involves the logarithmic shifter only.
For the sake of clarity the critical path of NewDWA and BiDWA have been depicted respectively in Figure 4.52(a) and in Figure 4.52(b).
It is clear that the critical path of the BiDWA algorithm includes an additional multiplexer, which selects the correct scrambled thermometric code depending on the Φ_{E-O} phase. Moreover the capacitive load C_x seen by the latch in the BiDWA solution is greater than the capacitive load seen by the latch in this modified version, due to the presence of the other logarithmic shifter. Therefore the usage of BiDWA not only consists of a mere duplication in a parallel path, but it also affects the critical path. It is worth to notice that the implementation of the NewDWA is actually very similar to the basic DWA, with the only difference of the pointer



(a) (b)

Figure 4.52: Critical path for a single bit line of the (a) NewDWA algorithm and of the (b) BiDWA algorithm.

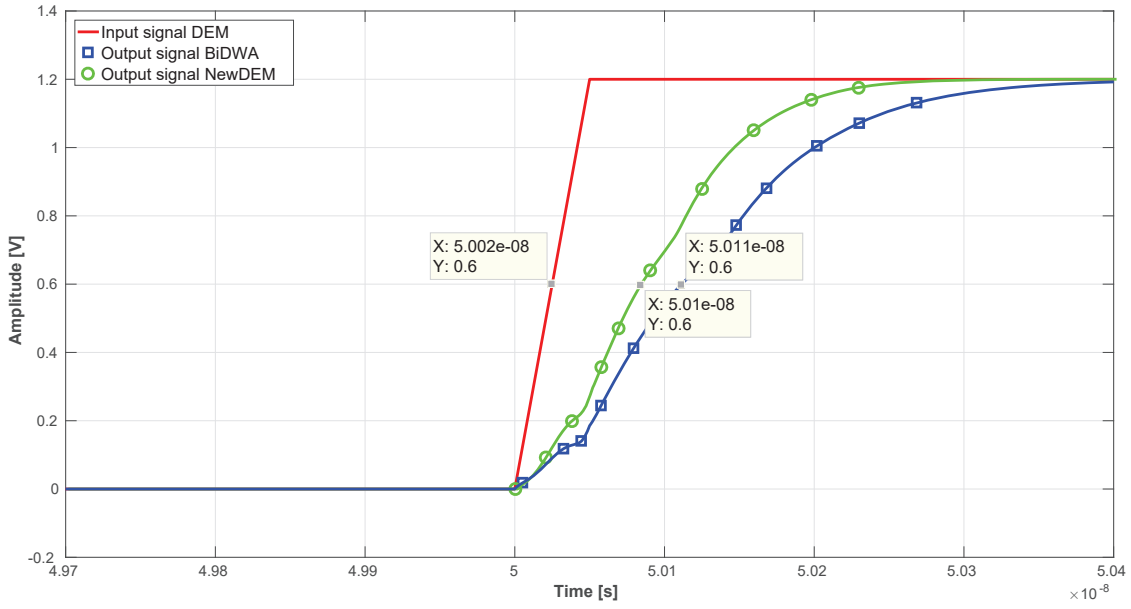


Figure 4.53: Feedback delay introduced by NewDWA and BiDWA algorithm.

register. As a consequence the hardware complexity of the proposed algorithm is very similar to the one of a standard DWA and, more importantly, the gates in the critical path are almost identical, leading to a similar capacitive load. Conversely in the case of a BiDWA all the updating logic must be doubled, because the update rule of the two pointers is different. Furthermore, the number of gates and the parasitic loads in the critical path increase, exacerbating the timing criticality.
Figure 4.53 reports the worst case propagation delay through the critical signal path for the circuit of Figure 4.51 and of a standard BiDWA. Using a BiDWA would imply an increase of 23% in the propagation delay through the critical path. Similar considerations can be drawn with respect to power and area consumption, as summarized in Table 4.4. The proposed design includes the possibility to change the algorithm between the DWA and the NewDWA with a digital input code. This

	DWA	BiDWA	NewDWA
Time Delay (ps)	74	96	75
Power Consumption (μW)	0.15	0.24	0.18
Area (normalized to DWA area)	1	2.12	1.25

Table 4.4: Comparison of DWA, BiDWA and the proposed algorithm in terms of time delay, power consumption and area.

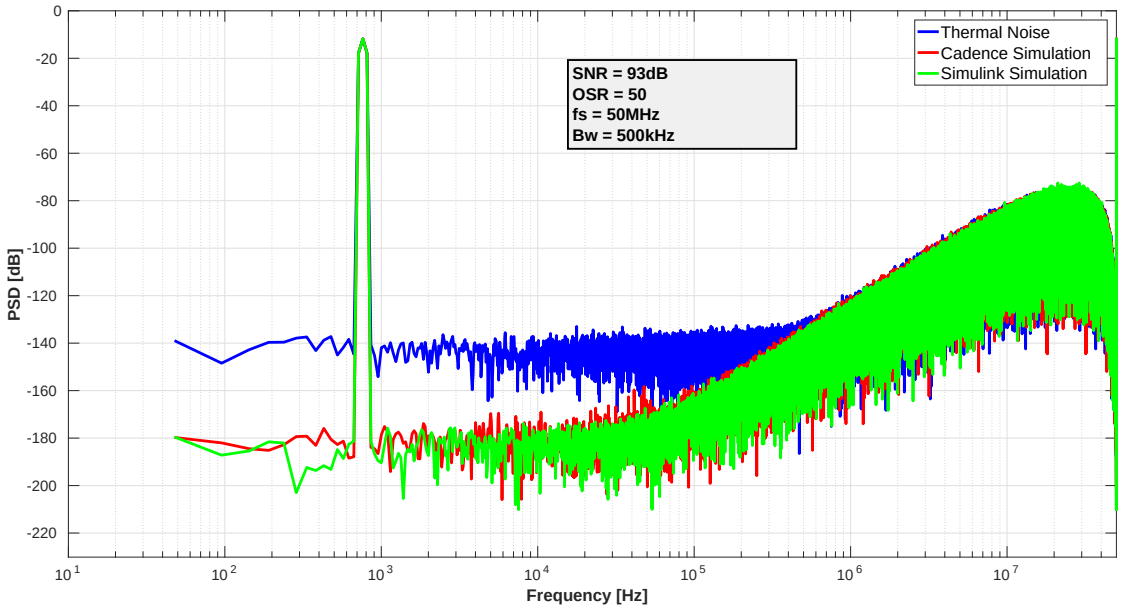


Figure 4.54: Validation of the behavioral model with a transistor-level simulation.

gives the possibility of having a performing $\Sigma\Delta$ modulator also for high OSR values. Moreover the possibility of disabling the DEM completely is included.

4.6 Conclusion

The overall design has been implemented in a 65nm technology with a 1.2V power supply. A transient simulation has been performed in order to validate the behavioral model and the result is depicted in Figure 4.54. As apparent the behavioral model follows well the transistor simulation. Also in Figure 4.54 a behavioral simulation including the thermal noise is reported.
In Figure 4.55 the time evolution of the 5 bit output signal when a CIC filter is applied is depicted. This simulation has been performed in *Cadence* assuming an ideal CIC filter. As shown in Figure 4.55, assuming a constant input as input of the modulator, the filtered output signal is enclosed between $\pm$LSB/2, where LSB is the least significant bit value relative to the 94dB dynamic range, coherently with

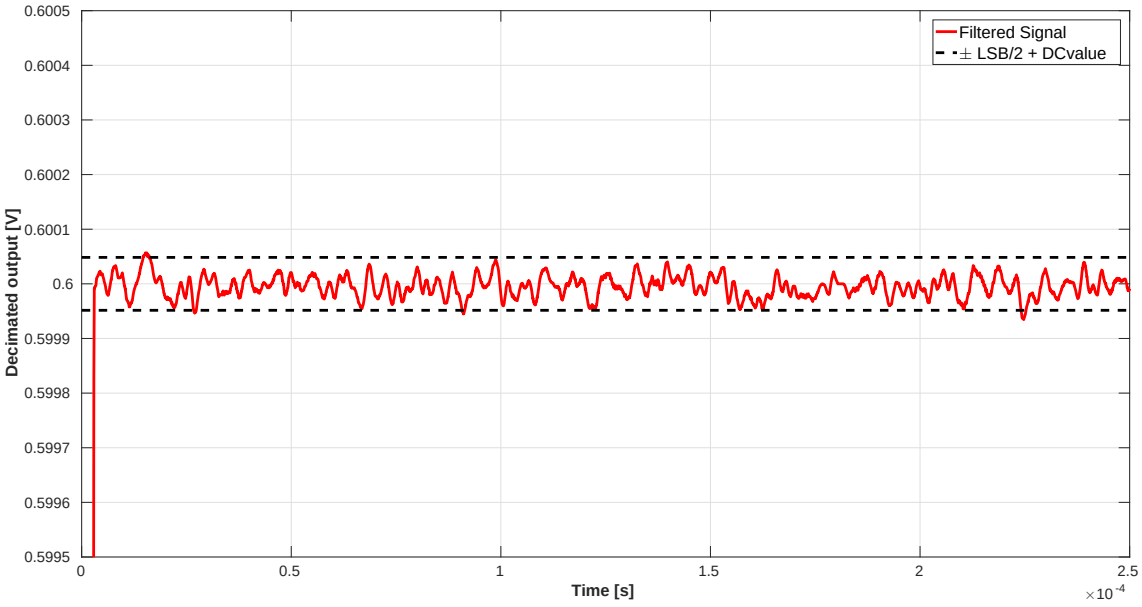


Figure 4.55: Time response of the ΣΔ output filtered by the CIC filter.

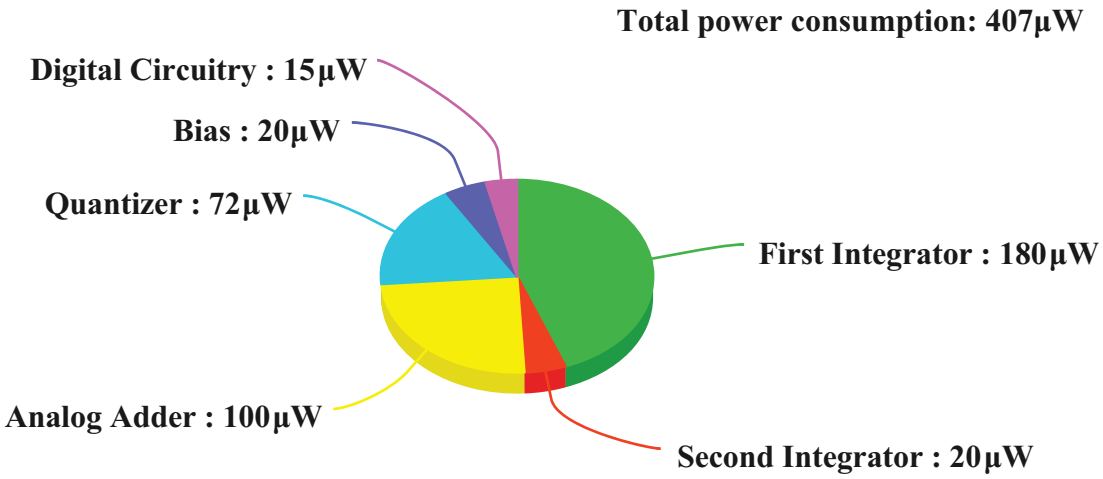


Figure 4.56: Pie chart of the power consumption of the proposed design.

the result obtained in the behavioral model.
In Figure 4.56 a pie chart of the power consumption of the system is depicted. The overall power consumption is $P = 407\mu$W. Considering the Figure of Merit (FOM) defined by Walden which is defined as

$$\text{FOM [J/conv]} = \frac{P}{2^{ENOB} \cdot 2B_w} \tag{4.23}$$

for this design a FOM = 8.7fJ/conversion is estimated.

Chapter 5

Measurement Setup

In this Chapter the measurement setup of a $\Sigma\Delta$ modulator is described. Besides a computer-based ADC-output to read the converter's output and to perform the Fourier transform on the modulator output, the main element of an ADC measurement setup is the input generator. The major problem with high resolution ADC is that the measurement setup requires a sine-wave generator with a very low residual distortion. The purity of the sine-wave must be higher than the resolution of the ADC, otherwise it will be impossible to verify the effective performance in terms of ENOB of the ADC. In this Chapter low-distortion and low-noise oscillator designs are described in order to verify the performance of the proposed design and in order to provide a general strategy for the testing of high-resolution ADC.

5.1 Background

The system's oscillator is the most difficult to design part of the measurement setup. Linearity testing of ADCs can be very challenging because it requires a signal generator substantially more linear than the ADC under test. The oscillator must have transcendentally low levels of impurity to meaningfully test 16 bit ADCs. Commercially available wave generators offer many functions, but the cost is high and furthermore the linearity and the noise floor are not sufficient to test the performance of the ADC.
Figure 5.1 shows the spectrum of a sine-wave generated by the arbitrary waveform generator HP33250A. This kind of generator can generate several types of waveforms, but with a limited linearity. In fact, as apparent from Figure 5.1, the noise generated by the instrument is too high and, therefore, a limited dynamic of DR = 60dB can be measured. The spectrum of Figure 5.1 has been measured with a Spectrum Analyzer Agilent E4407B with a Resolution BandWidth RBW = 10Hz. Also the Total Harmonic Distortion (THD), defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency, has been measured yielding THD = -59dB.
The major problems of this generator are the noise floor and the linearity.
Firstly the high noise floor at the input is reported at the output of the modulator without any noise-shaping and, therefore, it becomes the dominant noise source of the modulator. It is worth to notice that this solution includes also a high

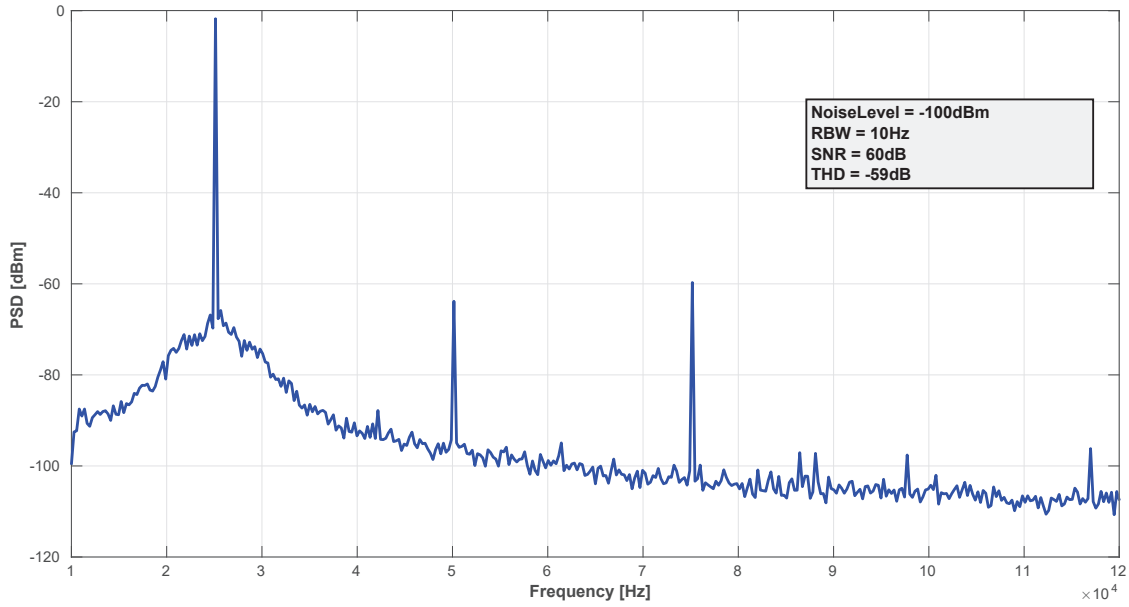


Figure 5.1: Spectrum of the sine-wave generated by a common laboratory instrument as the HP33250A.

phase noise. The phase noise is the frequency domain representation of random fluctuations in the phase of the waveform. The effect of the phase noise on the spectrum is to spread the power of the signal to adjacent frequencies, resulting in noise side-bands.
Secondly the distortion at the input is reported at the output, and then feed-back at the input inter-modulating with the harmonics at the input yielding other harmonics.
In the following two possible solutions to create a pure sine-wave are described.

5.2 Fixed-Frequency Solution

A first possible solution is to low-pass filtering the signal generated by the input. Since the signal generated by the signal generator of Figure 5.1 has a high noise floor also for low frequencies and it is moreover characterized by a significant phase noise, a high selectivity band-pass filter should be used. The design of this kind of filter can be challenging, therefore an alternative solution must be chosen.
A solution with lower noise and lower phase noise is represented by a crystal quartz oscillator. A crystal oscillator is a basic element used to create an electrical signal with a precise frequency. Quartz crystals are manufactured for frequencies from a few tens of kilohertz to hundreds of megahertz, however in this case design, for a signal bandwidth of 500kHz, a crystal oscillator with a fixed frequency of 32.768kHz is used.
In Figure 5.2 the spectrum of the signal generated by the crystal quartz is depicted. As apparent the noise floor is reduced, while the distortion is increased. This is motivated by the fact that the crystal quartz generates a square-wave and, therefore,

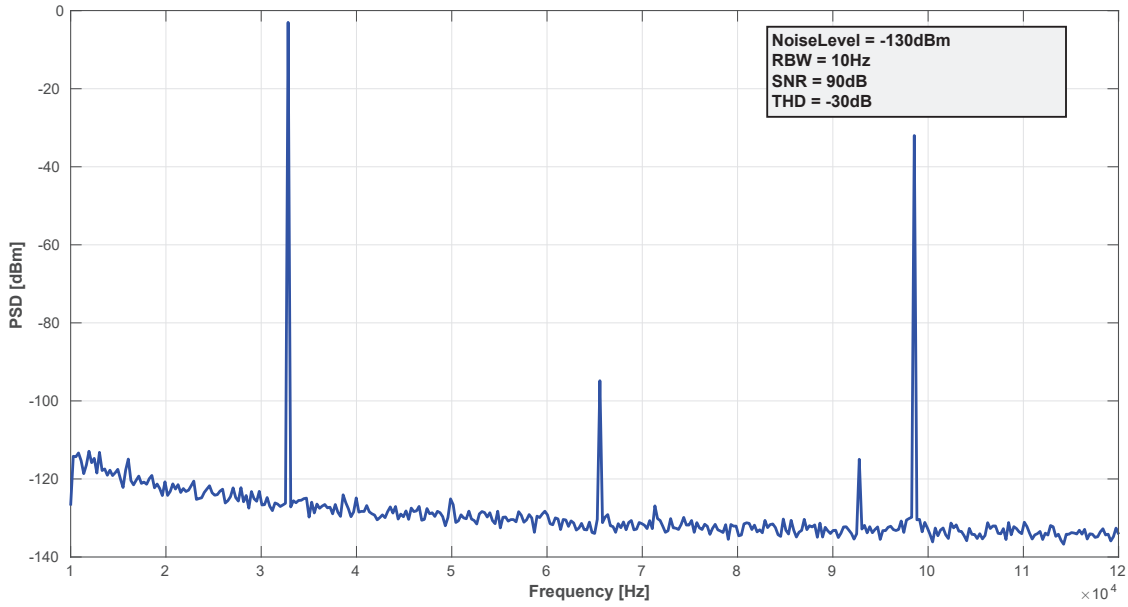


Figure 5.2: Spectrum of the wave generated by a crystal quartz oscillator.

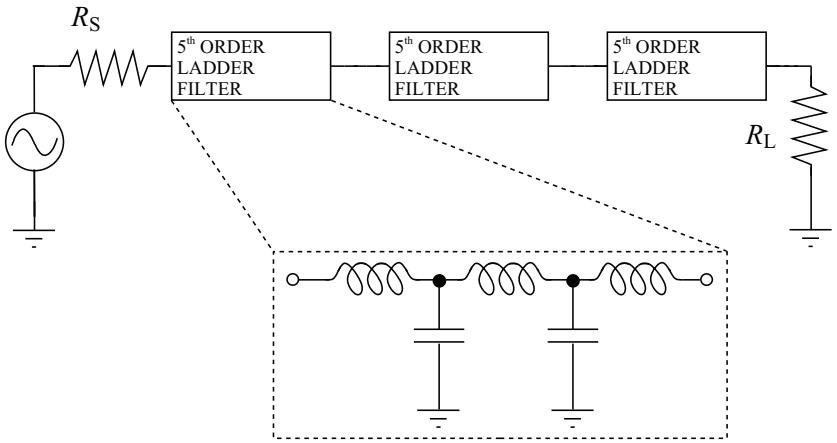


Figure 5.3: Low-pass filtering of the crystal quartz oscillation.

there is a high distortion.
In order to reduce the distortion produced by the crystal quartz a system as the one depicted in Figure 5.3 is used.
Three 5th-order ladder filters are used in order to clean the signal efficiently. The ladder filter has been designed taking as bandwidth frequency the oscillation frequency of the crystal quartz oscillator. In order to get maximally flat pass-band a Butterworth filter has been designed.
One of the characteristics of the ladder filter is the high insensibility to the variation of the parameters. This is an important feature since the discrete components are usually defined with a tolerance of ±20%, and, as a consequence, the signal

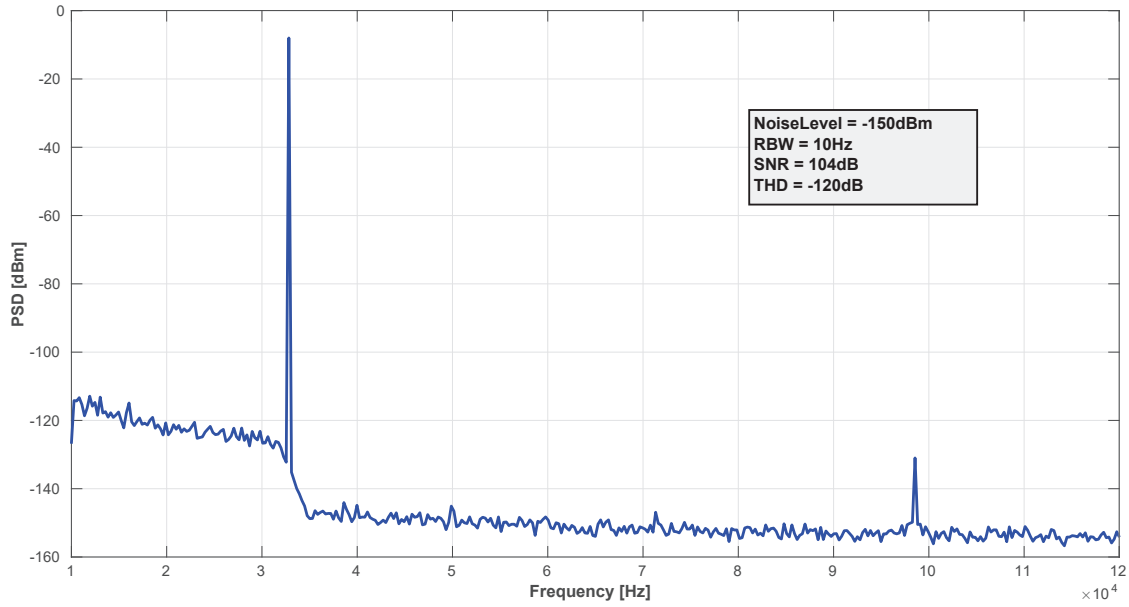


Figure 5.4: Spectrum of the filtered wave produced by the crystal quartz oscillator.

bandwidth may change with the variation of the values of inductors and capacitors. The effect of the low pass filtering of the 15th-order ladder filter on the square-wave produced by the crystal quartz oscillator is depicted in Figure 5.4.
From Figure 5.4 it is apparent the profile of the low pass filtering near the sine-wave peak. The noise floor for high frequencies is given by the noise of the spectrum analyzer, therefore a higher SNR is actually obtained. This solution provides a sufficient SNR for the design proposed in this thesis, however with this kind of solution only a single frequency can be tested, namely $f_{in} = 32.768$kHz. In the following a variable-frequency solution is described.

5.3 Variable-Frequency Solution

Among the variable-frequency sine-wave oscillators the Wien-Bridge network remains the most popular since the basic circuit can be very simple in form.
The basic circuit for an oscillator of this form, using a single operational amplifier as the gain block, is shown in Figure 5.5.
The loop gain of the basic Wien network is given by

$$T = \left(\frac{sCR}{1 + s3RC + s^2R^2C^2} - \frac{R_2}{R_1 + R_2} \right). \tag{5.1}$$

The Barkhausen condition, namely when the loop gain $|T| = 1$, is satisfied for an oscillation frequency f

$$f = \frac{1}{2\pi RC}. \tag{5.2}$$

The condition to start the oscillation is given by

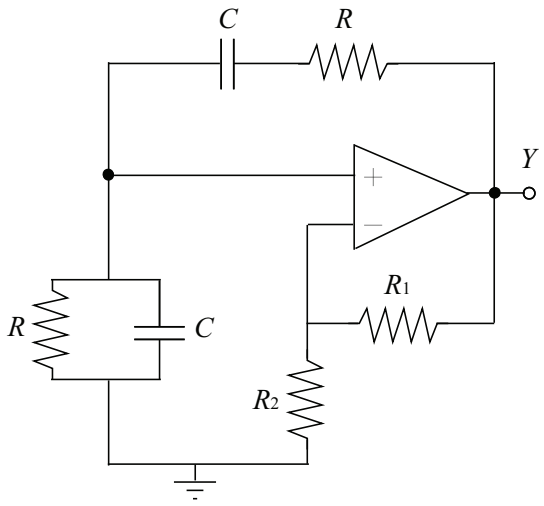


Figure 5.5: Basic Wien-bridge oscillator circuit.

$$|T| > 1 \implies R_2 > 2R_1. \tag{5.3}$$

With a loop gain greater than one, the oscillator will start. The conventional oscillator circuit is designed so that it will start oscillating and then, when the amplitude reaches a certain value, the loop gain will be stabilized to the unitary value. The amplitude control, commonly known as Amplitude Gain Control (AGC), is a closed-loop feedback regulating circuit, with the purpose of restoring the condition $|T| = 1$ when a certain amplitude is reached. The AGC network can be realized in several ways, such as diodes, thermistors, field effect transistors or photocells. Depending on the type of AGC network used, different distortions are applied and, therefore, the linearity of the oscillator strongly depends on the type of AGC network used.

However, in the form shown in Figure 5.5, a significant problem exists in that the transmission of a normal Wien network, at the operating frequency given by Equation (5.2), is only 1/3, which means that an inconveniently large proportion of the output signal voltage appears at the input of the amplifier, and will lead to non-linearities.

However, it is not implicit, in the use of a Wien network as the frequency-control method, that the configuration shown in Figure 5.5, in which the output of the network is taken to the non-inverting input of the amplifier and the amplitude controlling negative-feedback signal is taken to the other, is the only circuit configuration which can be employed.

In Figure 5.6(a) the classical Wien-Bridge network is shown. In this classical solution the signal at the inverting input of the amplifier is attenuated of only 1/3. If, instead of the network of Figure 5.6(a) being connected between a signal source E_x and the 0V line, it was connected between two signal sources E_x and $-E_y$, where these are sinusoidal and identical in frequency and the negative sign implies phase opposition, as shown in Figure 5.6(b), then a small, in-phase signal would exist at the point X, at the frequency of maximum transmission f, if E_x is slightly

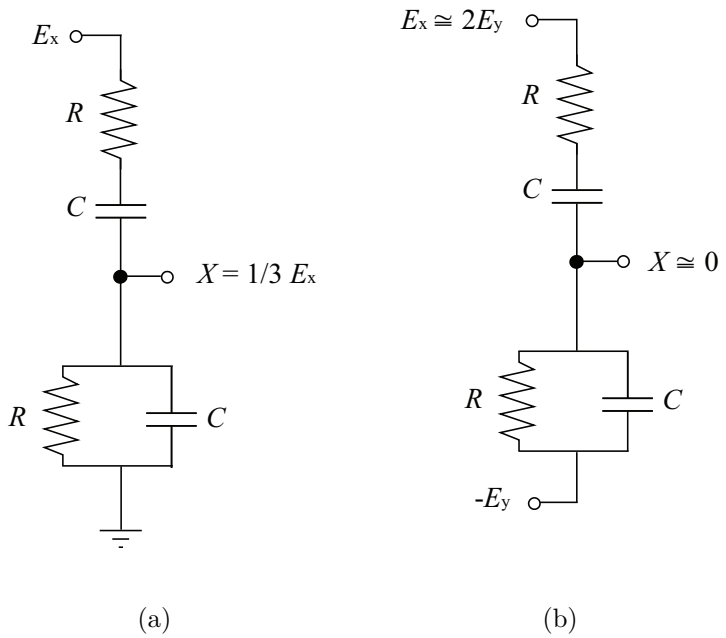


Figure 5.6: (a) Classical Wien-Bridge network and (b) rearranged Wien network.

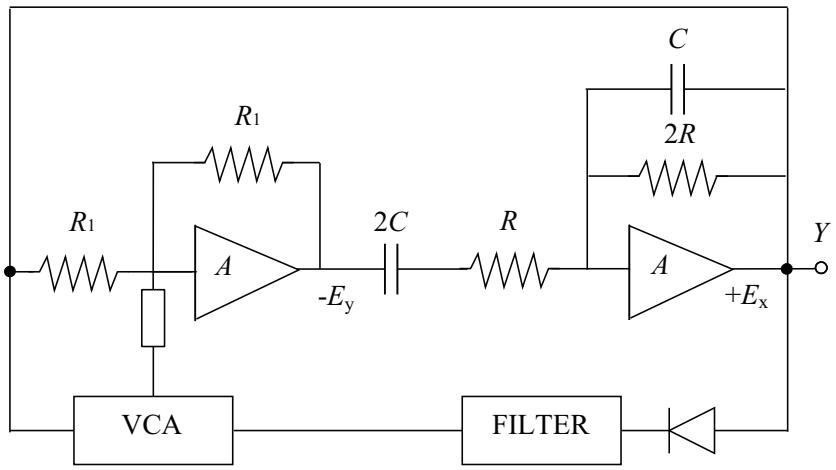


Figure 5.7: Low distortion oscillator based on the Wien-Bridge topology.

greater than $-2E_y$.
In order to generate the $-E_y$ signal an amplifier acting as an inverter can be used, as the one in Figure 5.7.
Instead of using equal values for R and C the Wien-Bridge of Figure 5.7 uses $2R$, C, R and $2C$ in order to avoid the inverting amplifier with a gain of -2. The amplitude stabilization is reached with the feedback network shown in Figure 5.7 consisting in a Filter and in a Voltage Controlled Amplifier (VCA).
The complete oscillator circuit is shown in Figure 5.8. $IC1$ and $IC2$ are low noise,

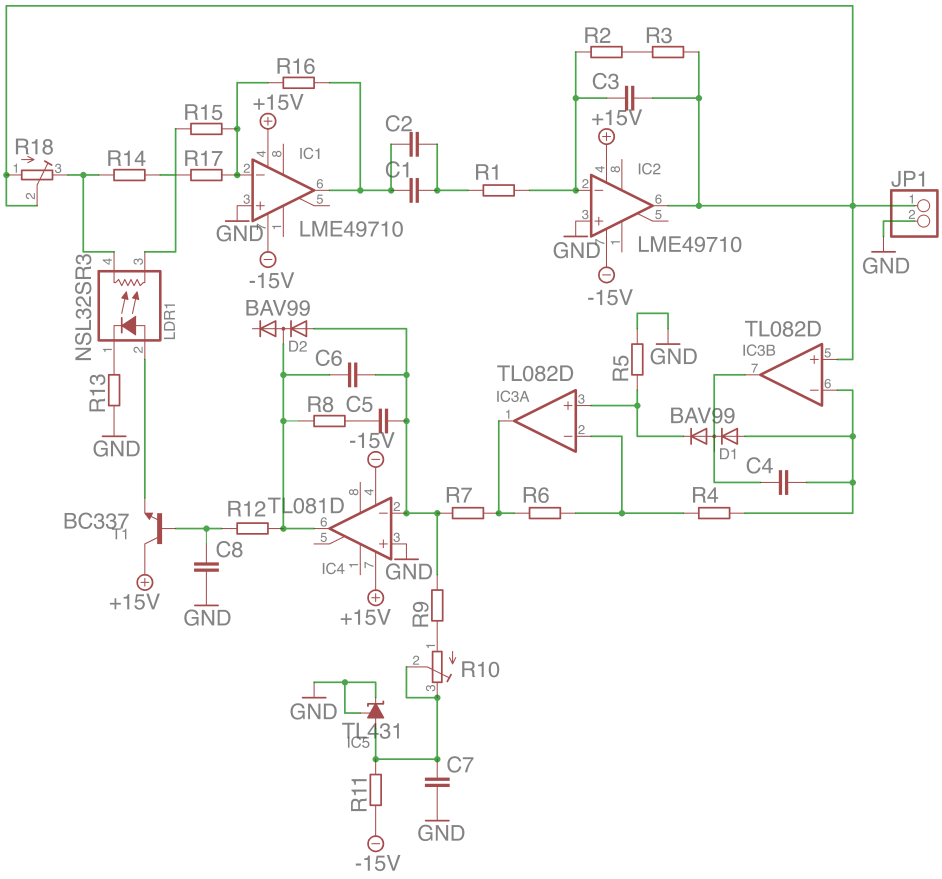


Figure 5.8: Ultra low distortion oscillator used for the ADC test.

high linearity LME49710 amplifiers. These amplifiers have non-linearity below 0.1ppm with a relative large bandwidth. $IC1$ acts as an inverter with gain -1. $IC2$, in conjunction with R_1, R_2, R_3, C_1, C_2, C_3 forms a band-pass filter that sets the oscillator's resonant frequency. Therefore, the frequency of the oscillation can be tuned by changing the values of these resistors and capacitors. The GBW of the selected amplifier ensures a good linearity and low noise performances over the bandwidth of interest, namely $0 - 500$kHz. For higher frequencies the distortion of the LME49710 increases and, therefore, other type of integrated circuits should be chosen. The simulated output referred noise is reported in Figure 5.9. As apparent the output noise is low enough to ensure a good SNR for all the frequencies inside the signal bandwidth.

For the amplitude stabilization, the oscillator's AGC circuit consists of a full-wave rectifier with high input impedance ($IC3A$, $IC3B$), integrator $IC4$ and an opto-coupler. The optocoupler has been chosen in order to avoid a high non-linearity in the AGC circuit.

The performances of this low distortion oscillator has been validated over the bandwidth of interest and a spectrum example is reported in Figure 5.10.

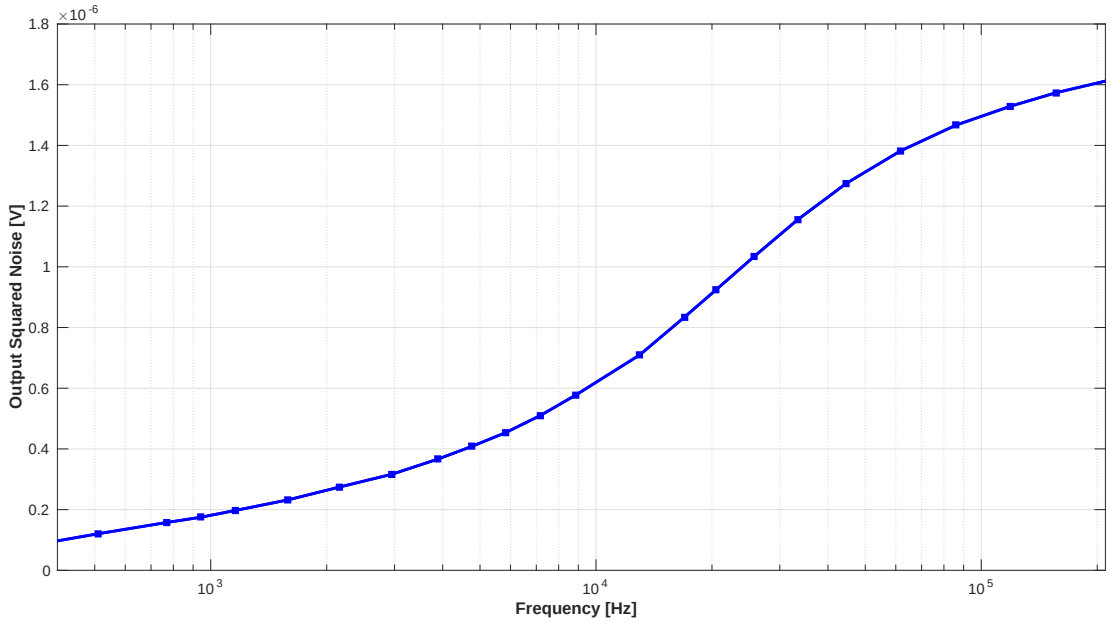


Figure 5.9: Output noise of the proposed oscillator versus the oscillation frequency.

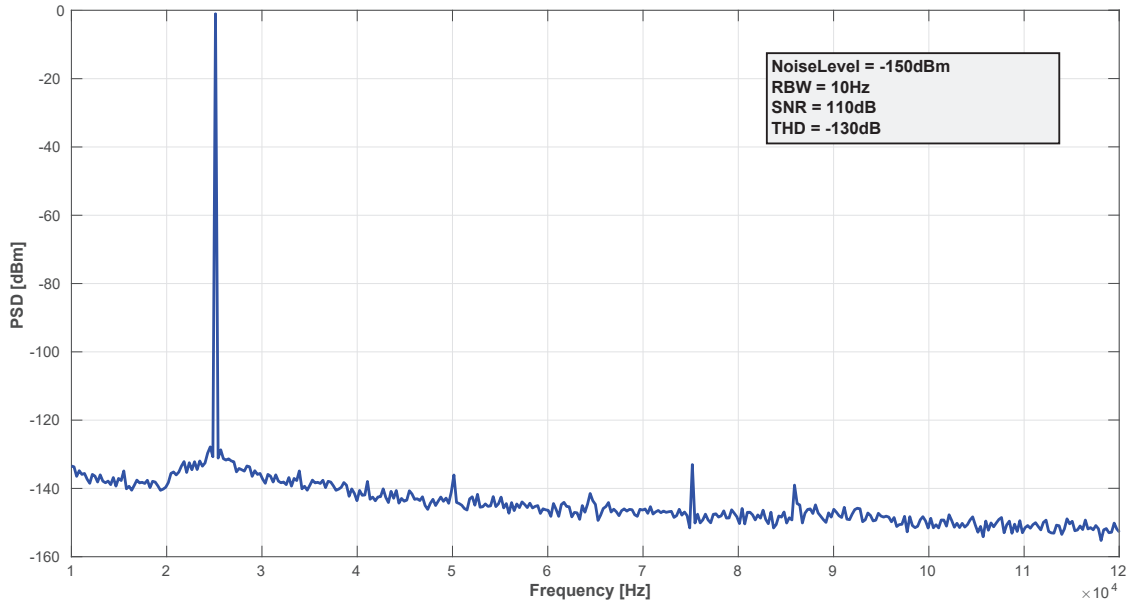


Figure 5.10: Output spectrum of the low distortion oscillator used for the ADC test.

Chapter 6

Conclusion

The chip has been fully designed in 65nm technology. The layout of the chip is depicted in Figure 6.1. The top view of the circuit includes all the main blocks of the modulator described in Chapter 4.

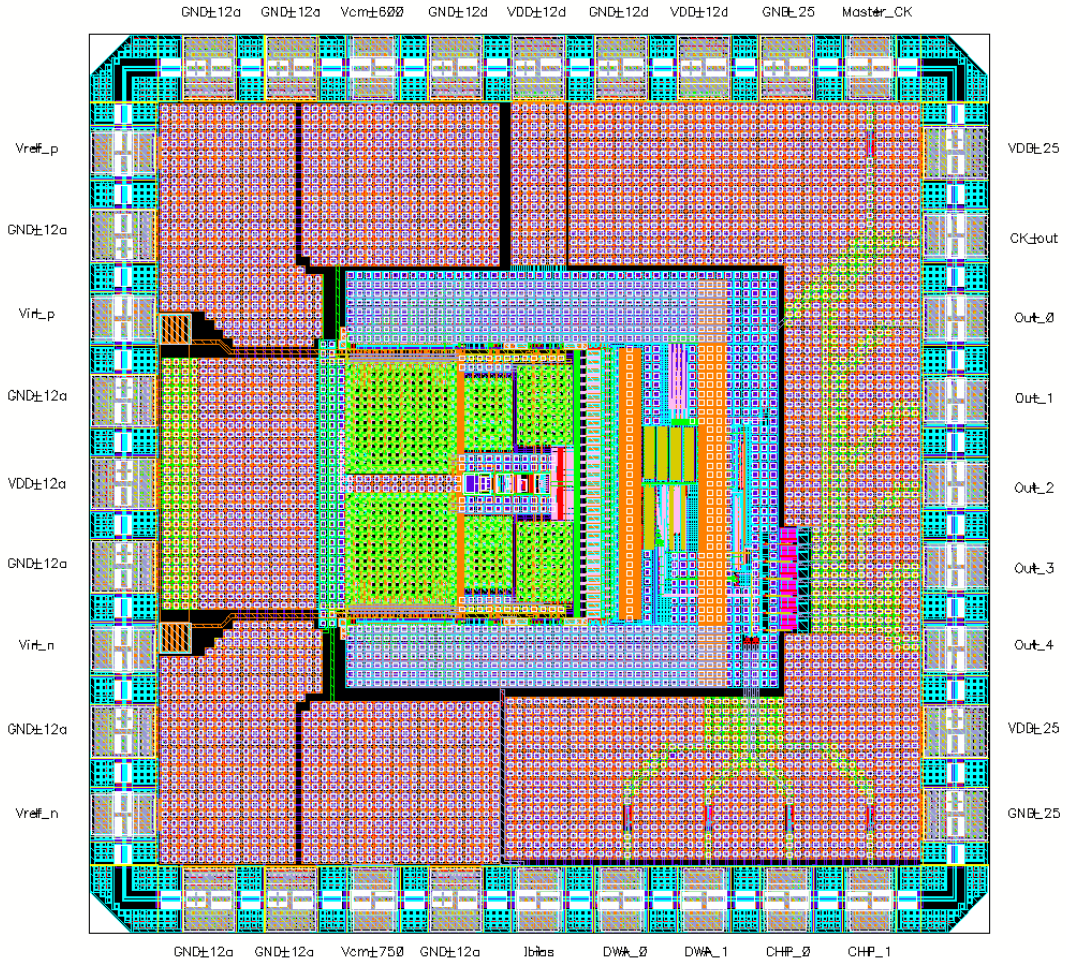


Figure 6.1: Layout of the proposed design of the ΣΔ modulator.

Input-to-Output buffers are designed in order to take the five output digital signals from the core of the chip to the pad ring. Also the clock is taken out from the core

of the chip in order to synchronize the digital output stream without an external clock. Output-to-Input buffers are also designed in order to take several signals, namely the master clock and some digital programming signals, from the pad ring to the core of the chip. These buffers have a different power supply with respect to the power supply of the core of the chip. The supply voltage of the buffers is $V_{DD} = 2.5\text{V}$.
Decoupling capacitors are placed between the pad ring and the core of the chip in order to stabilize the constant signal like the references of the DAC, the common modes and the supply voltages coming from outside of the chip. The size of these capacitors is in the order of hundreds of pF. Furthermore, in order to achieve good quality voltage references, additional by-pass capacitors are added outside of the chip on the printed circuit board (PCB). The size of the core of the chip is $400\mu\text{m}\times400\mu\text{m}$, while the size of the overall chip including the by-pass capacitors and the pad ring is $1\text{mm}\times1\text{mm}$. An additive PCB has been designed in order to generate the pure sine-wave signal, as explained in Chapter 5.
The photo of the die is depicted in Figure 6.2

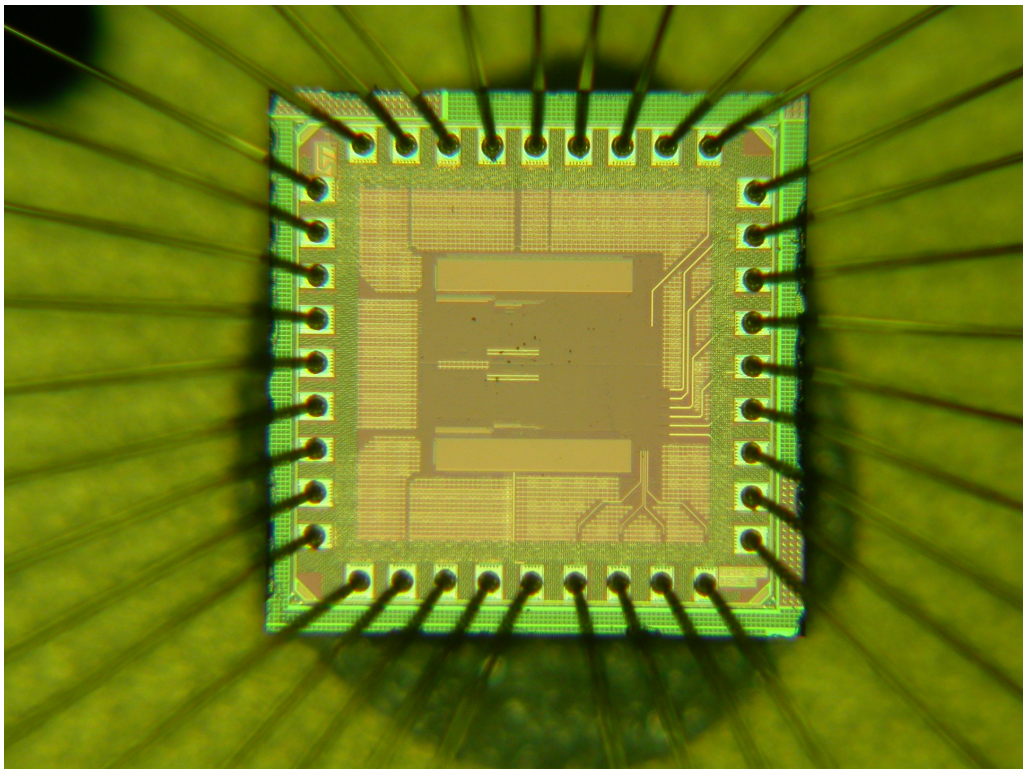


Figure 6.2: Photo of the die.

The chip has been firstly measured with the waveform generator HP33250A yielding the result depicted in Figure 6.3.
The floor noise and the several harmonics existing in this measured output spectrum are motivated by the spectrum of the signal generated by the arbitrary waveform generator, proving that the modulator is actually measuring the linearity of the arbitrary waveform generator. However, due to ESD (electrostatic discharge) the diode protections of the pad of the chip have been damaged and it has not been possible to perform other measurements on the same version of the chip. Other

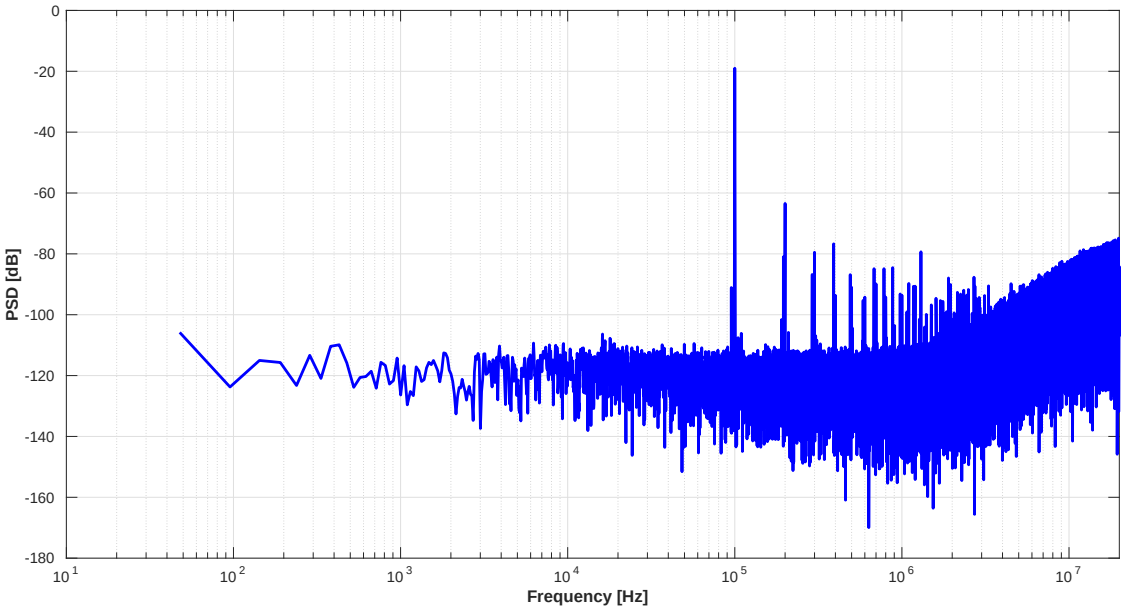


Figure 6.3: Measured output spectrum of the proposed design.

version of the same chip coming from the same fabrication run has been measured, but with unsuccessful results. This event has been motivated as a process related issue. This hypotesis has been validated also with Montecarlo simulations on *Cadence*. In fact some issues have been found in the comparator and in particular the Montecarlo simulations have showed that, for some instances, the output of the 31 comparators was 0 or V_{DD}, regardless of the sign of the input. This was motivated by the fact that the dynamic comparator of this design, depicted in Figure 4.27, was in its first version realized with a single transistor bias, and not two separate biases M_5 and M_6 as in the new version of the design, with all the sources of the nMOS $M_1 - M_4$ shorted. Even with a little unbalance of the matching properties between the transistor of the differential pairs the output generated was uncorrect. However, as shown in the simulation of Figure 4.31, this problem has been solved The new chip should have a maximum SNDR value at -3dBfs and a minimum SNDR value at -97dBfs which yields a dynamic range of 94dB.
The following step in the validation of the work presented in this thesis is to wait the silicon coming from the foundry and then measuring the new version of the chip. However this step takes generally a lot of time and it was not possible to measure the new version of the chip before the ending of the PhD activity. However the simulation results, both at transistor level and system level, in addition with the strict mathematical modeling used for the all the main blocks of the design are encouraging for a validation of the design even with the silicon measurements.

Appendix A

Error estimation in DEM

A.1 Worst-Case DAC Mismatch Effect

In this section the effect of the mismatch between the unit elements on the output voltage of the DAC is evaluated. Assuming that all the elements values are drawn from an identical Gaussian probability distribution having a mean U and a standard deviation of ΔU, the standard deviation of the output voltage for a digital code word K can be expressed as

$$\Delta y_{DAC} = (\Delta U)\sqrt{K}. \tag{A.1}$$

For an N bit internal DAC, there will be $M = 2^N$ individual unit elements and the full scale output will be $M \cdot U$. The standard deviation of the output voltage can be expressed as a fraction of the full-scale voltage:

$$\frac{\Delta y_{DAC}}{y_{DAC}} = \frac{(\Delta U)\sqrt{K}}{U \cdot M}. \tag{A.2}$$

The greatest error comes for the largest value of K, which is M. Assuming that the zero output and the full-scale output $M \cdot U$ define the line from which the error at each output code will be measured, the deviation from this line is given by

$$\Delta y_{DAC}(K) = \left(\sum_{i=1}^{K} U_i\right) - \left(-\frac{K}{M}\sum_{i=1}^{M} U_i\right), \tag{A.3}$$

which can be expressed also as

$$\Delta y_{DAC}(K) = \frac{M-K}{M}\left(\sum_{i=1}^{K} U_i\right) - \left(-\frac{K}{M}\sum_{i=K+1}^{M} U_i\right). \tag{A.4}$$

Recalling that Equation (3.10) has to be demonstrated, the standard deviation of the normalized output, that is $\sigma(\Delta y_{DAC}/y_{DAC})$, can be expressed by dividing the terms on the right of the equation for the nominal value of the full scale voltage $U \cdot M$, while the term on the left is divided by y_{DAC}, as defined in Equation (A.2):

$$\frac{\Delta y_{DAC}(K)}{y_{DAC}(M)} = \frac{M-K}{M^2}\left(\sum_{i=1}^{K} \frac{\Delta U_i}{U}\right) - \left(-\frac{K}{M^2}\sum_{i=K+1}^{M} \frac{\Delta U_i}{U}\right). \tag{A.5}$$

Under the assumption that all of the element values are independent samples of a normal probability density, the variance of the output voltage, as a fraction of the nominal full-scale output voltage, is given by

$$\sigma^2\left[\frac{\Delta y_{DAC}(K)}{y_{DAC}(M)}\right] = \left(\frac{M-K}{M^2}\right)^2 \cdot K \cdot \sigma^2\left[\frac{\Delta U}{U}\right] + \left(\frac{K}{M^2}\right)^2 (M-K) \cdot \sigma^2\left[\frac{\Delta U}{U}\right]. \quad \text{(A.6)}$$

This expression can be simplified to get the gain between the standard deviation of the element fractional mismatch and the standard deviation of the internal DAC's output as a fraction of nominal full scale:

$$\sigma\left[\frac{\Delta y_{DAC}(K)}{y_{DAC}(M)}\right] = \sqrt{\frac{1}{M}\frac{K}{M}\frac{M-K}{M}}\sigma\left[\frac{\Delta U}{U}\right]. \quad \text{(A.7)}$$

It is worth to notice that the variance of the output voltage is a parabolic function of the digital input code. It goes to zero at both zero output and full-scale output, since it chosen the straight line between those two points as reference for measuring errors. The maximum of Equation (A.7) is reached when $K = M/2$. Therefore by substituting $K = M/2$ in Equation (A.7) it yields

$$\sigma\left(\frac{\Delta y_{DAC}}{y_{DAC}}\right) = \frac{1}{2\sqrt{2^N}} \cdot \sigma\left(\frac{\Delta U}{U}\right) \quad \text{(A.8)}$$

what was to be demonstrated.

A.2 SNR Butterfly Algorithm

In this section the resolution for the randomization Butterfly algorithm is evaluated. Let U_i the unit elements of the DAC and $y(k)$ the input of the Butterfly Algorithm. As already defined in Equation (3.15) the mismatch contribution is given by

$$\epsilon(k) = \sum_{i=1}^{y(k)} U_i - y(k) \cdot U_{mean}. \quad \text{(A.9)}$$

To simplify the evaluation of the noise contribution of the randomization, it's assumed that:

- All the combination of selected unit elements have the same probability.
- The unit elements U_i are random variables with expectation $\mathrm{E}(U_i) = 1$ and variance σ_w^2.
- The unit elements U_i and U_j are independent variables for $i \neq j$.

As all the cells have the same probability density function, the variance of the mismatch is independent on the selected unit elements. Therefore the variance can be found as

$$
\begin{aligned}
E(\epsilon^2) &= E\left[\left(\sum_{i=1}^{y(k)} U_i - y(k)\cdot U_{mean}\right)^2\right] = \\
&= E\left[\left(\sum_{i=1}^{y(k)} U_i - \frac{y(k)}{2^N}\sum_{i=1}^{2^N} U_i\right)^2\right] = \\
&= \left(y - \frac{y^2}{2^N}\right) U_{mean}^2 \sigma_w^2.
\end{aligned}
\tag{A.10}
$$

where, in the last step of Equation (A.10) it has been exploited that the general unit element U_i can be written as $U_i = U_{mean} + \delta U_i$ where δU_i is a random variable with variance $U_{mean}\sigma_w^2$. This formula shows that the power of the mismatch error with the Butterfly algorithm is modulated by the value of the input code y. This noise power cancels at the extremities of the range, for $y = 0$, as no element is selected, and for $y = 2^N$, as all the elements are selected. The noise power is maximum in the middle of the range, for $y = 2^{N-1}$. The power of the noise can be found by integration for all possible input y as

$$
P_{noise} = \int_{y=0}^{y=2^N} \left(y - \frac{y^2}{2^N}\right) U_{mean}^2 \sigma_w^2 \mathrm{d}y = \frac{U_{mean}^2 \cdot 2^N \cdot \sigma_w^2}{6}. \tag{A.11}
$$

The peak-to-peak output is given by $2^N \cdot U_{mean}$ therefore the signal power is given by $P_{sig} = 2^{2N} \cdot U_{mean}^2/2$. Assuming that the mismatch error is white between 0 and $f_s/2$ it yields

$$
SNR = \frac{3 \cdot 2^N \cdot OSR}{\sigma_w^2}. \tag{A.12}
$$

A.3 SNR General DEM

In this section it will be demonstrated that for a general DEM the SMNR can be estimated as

$$
\text{SMNR [dB]} = 10 \cdot \log\left(\frac{2^N}{2\sigma_w^2(1-2^{-N})^2 \int_{-\pi/\text{OSR}}^{\pi/\text{OSR}} |H_{DEM}(\omega)|^2 \mathrm{d}\omega}\right). \tag{A.13}
$$

For a general $\Sigma\Delta$ with $\text{NTF}(z) = (1 - z^{-1})^L$ it has already been shown that the in-band quantization noise is given by

$$
\text{IBN} = \int_{-B_W}^{+B_W} S_E(f)|\text{NTF}(f)|^2 \mathrm{d}f \approx \frac{\Delta^2}{12}\frac{\pi^{2L}}{(2L+1)\text{OSR}^{(2L+1)}}. \tag{A.14}
$$

However, for a general user-defined NTF the in-band quantization noise can be written as

$$\text{IBN} = \int_{-B_W}^{+B_W} S_E(f)|\text{NTF}(f)|^2 \text{d}f = \frac{f_s}{2\pi} \int_{-\frac{\pi}{\text{OSR}}}^{+\frac{\pi}{\text{OSR}}} \frac{\Delta^2}{12 f_s} |\text{NTF}(\omega)|^2 \text{d}\omega \tag{A.15}$$

where the angular frequency is $\omega = 2\pi f / f_s$. The power of the sinusoidal input is given by

$$P_{sig} = \frac{(Y_{FS}/2)^2}{2} = \frac{Y_{FS}^2}{8} = \frac{\Delta^2 \cdot (2^N)^2}{8}. \tag{A.16}$$

Therefore it is possible to estimate the SNR from Equations (A.15) and (A.16):

$$\text{SNR [dB]} = 10 \cdot \log \left(\frac{2^{2N}}{\frac{1}{3\pi} \int\limits_{-\pi/\text{OSR}}^{\pi/\text{OSR}} |\text{NTF}(\omega)|^2 \text{d}\omega} \right). \tag{A.17}$$

Let's now consider the DEM and the SMNR for a general DEM algorithm. We will demonstrate that an equivalent equation as Equation (A.17) can be obtained by studying the DEM algorithms. In Chapter 3.3.3, Equation (3.18) the Z-transform of a general mismatch error has been defined as

$$E(z) = H_{DEM}(z) IM(I), \tag{A.18}$$

where H_{DEM} is the mismatch-shaping transfer function of the general DEM algorithm and $IM(I)$ is the Integral Mismatch function of the index I. To derive the output spectrum analytically would require exact knowledge of the PSD of the index I. It is not trivial to find the general PSD pointer function.
Recalling the result of Equation (3.16) the Integral Mismatch function is defined as

$$IM(I(k)) = \sum_{i=1}^{I(k)} U_i - I(k) U_{mean} = \sum_{i=1}^{I(k)} U_i - \frac{1}{2^N} \sum_{i=1}^{2^N} I(k) \cdot U_i. \tag{A.19}$$

However the index $I(k)$ can be written using the very well known arithmetic series $\sum_{k=1}^{n} k = k(k+1)/2$ as

$$I(k) = \frac{1}{2^N} \sum_{i=1}^{2^N} \left(I(k) + \frac{2^N + 1}{2} - i \right) \tag{A.20}$$

which yields

$$IM(I(k)) = \sum_{i=1}^{I(k)} U_i - I(k) U_{mean} = \sum_{i=1}^{I(k)} U_i + \frac{1}{2^N} \sum_{i=1}^{2^N} \left(i - \frac{2^N + 1}{2} - I(k) \right) U_i. \tag{A.21}$$

Assuming two different indexes, I_1 and I_2, it is possible to compute the self-correlation function of the mismatch noise. The self-correlation will be used to

evaluate the noise power. After some calculation and using the result obtained in Equation (A.21) it turns out that

$$E\left[IM(I_1)\cdot IM(I_2)\right]=\frac{\sigma_w^2}{2^N}\left\{\frac{2^{3N}-2^N}{12}-\frac{2^N}{2}\left(I_2-I_1\right)\cdot\left[2^N-\left(I_2-I_1\right)\right]\right\}. \quad \text{(A.22)}$$

This expression will be used in order to compute the self-correlation of the mismatch noise, which is given by

$$\Psi(p)=E[IM(I_k)\cdot IM(I_{k+p})]. \quad \text{(A.23)}$$

Assuming that all the input values of the input code have the same probability and considering a worst-case scenario it is easy from Equation (A.22) to obtain

$$\Psi(p)=\frac{\sigma_w^2(1-1/2^N)^2\cdot 2^N}{12}. \quad \text{(A.24)}$$

As stated by the Wiener-Khinchin theorem the self-correlation function of a wide-stationary random process has a spectral decomposition given by the power spectrum of that process. In other words, assuming $S(f)$ as the power spectral density of the integral mismatch function and $\Psi(p)$ the self-correlation function of the mismatch noise for the Wiener-Khinchin it holds that

$$S(f)=\sum_{p=-\infty}^{\infty}\Psi(p)\mathrm{e}^{-j(2\pi f)p}. \quad \text{(A.25)}$$

Therefore the Wiener-Khinchin theorem can be used to find the mismatch error's PSD. From Equation (A.24) using the equivalence given in Equation (A.25) it yields:

$$S_\epsilon=\frac{\Delta^2\sigma_w^2(1-1/2^N)^2\cdot 2^N}{4}. \quad \text{(A.26)}$$

Therefore, using the signal power estimated in Equation (A.16) and the noise power estimated in Equation (A.26) the estimated SNR for a general DEM with mismatch transfer function $H_{DEM}(z)$ is

$$\text{SMNR [dB]}=10\cdot\log\left(\frac{2^N}{2\sigma_w^2(1-2^{-N})^2\int\limits_{-\pi/\text{OSR}}^{\pi/\text{OSR}}|H_{DEM}(\omega)|^2\mathrm{d}\omega}\right), \quad \text{(A.27)}$$

what was to be demonstrated.

A.4 SNR DWA

It is relatively easy to otbatin the SNR of the DWA, knowing that the Equation (A.27) is valid for a general DEM algorithm. In order to obtain the SNR of the

DWA algorithm the result demonstrated on the previous Section of Equation (A.19) is used. For the DWA case the $H_{DEM} = (1 - z^{-1})$ is the already demonstrated first-order high-pass transfer function. Therefore

$$\int_{-\pi/\mathrm{OSR}}^{\pi/\mathrm{OSR}} |H_{DEM}(\omega)|^2 \mathrm{d}\omega = \frac{2\pi^2}{3\mathrm{OSR}^3}. \tag{A.28}$$

By substituting the result of Equation (A.28) into Equation (A.27) it yields

$$\mathrm{SNR} = \frac{3 \cdot 2^N \cdot \mathrm{OSR}^3}{4\pi^2 \sigma_w^2 \cdot (1 - 2^{-N})^2}. \tag{A.29}$$

which is the result obtained in Chapter 3.3.3.

List of Publication

1. A. Celin and A. Gerosa, "Optimal DWA design in scaled CMOS technologies for mismatch cancellation in multibit $\Sigma\Delta$ ADCs" , *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1454-1457, May 2015

2. A. Celin and A. Gerosa, "A reduced hardware complexity data-weighted averaging algorithm with no tonal behavior", *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 702-705, May 2016

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