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Advanced Non-Volatile Memories: Reliability and Ionizing Radiation Effects

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Contents

Summary

In few years conventional Floating Gate Flash memories will be replaced with other devices able to guarantee a further scaling in dimension and better performances.

In fact, in the last years the size of Floating Gate Flash memory cells has been constantly reduced in order to obtain high-density and low-cost products. Still, Flash memories have now to face the problems deriving from such continuous scaling and it is not clear if/how they could be scaled below the 45nm technology node.

In this scenario, semiconductor companies are exploring different solutions to overcome the Flash memories scaling limits and new non-volatile memory devices have been proposed. Some of them could be seen as natural evolutions of conventional Floating Gate Flash memories, like Nanocrystal Memories and SONOS. At the same time, completely new technologies are also investigated, like ferroelectric memory (FeRAM), magnetoresistive memory (MRAM) or Phase Change Memory (PCM).

Today, it is not clear which solution will be the winning one.

The aim of this thesis is to study some advanced non-volatile memories from the point of view of the reliability. In particular, we focus our attention to the ionizing radiation effects on these devices.

The thesis is organized as follows:

- *Chapter 1* is an introduction about the scaling issues of Floating Gate Flash memories and about the new concepts for non-volatile data storage.

- *Chapter 2* is an overview about the radiation environments, the importance of radiation effects for electronic devices and about the basic mechanisms of interaction between ionizing particles and electronic devices. In the second part of this chapter the effects of ionizing radiation on oxides and on conventional Floating Gate Flash memories are also briefly described.

- The first part of the *Chapter 3* focuses on the ionizing radiation effects on Nanocrystal Memories. In the second part, we study a peculiar electrical characteristic of Nanocrystal Memories by using TCAD simulations.

- *Chapter 4* deals with the ionizing radiation effects on Phase Change Memories.

- In C*hapter 5* we study the radiation effects on capacitors with an Oxide-Nitride-Oxide (ONO) stack as dielectric.

Chapter 1

Introduction

In the last decade the impressive growth of the portable systems market (palmtop, mobile PC, mp3 audio player, digital camera and so on) has attracted the interest of the semiconductor industry on non-volatile memory (NVM) technologies for both code and mass storage applications. Since the demand for mobility applications is the main driver behind NVM technologies and components, ever higher capacity and system performance, lower power consumption, smaller form factor and lower system costs are thus required. The current NVM mainstream is based on the Floating Gate Flash technology, which has a nearly 100% market share [Bez04].

1. Floating Gate Flash Memories

A floating gate cell is similar to a common MOSFET with one major modification, that is a polysilicon layer called Floating Gate (FG) surrounded by insulator and located between the Gate (called Control Gate - CG) and the channel [Cap99, Bez03]. Varying the amount of charge trapped into the FG, we can change the threshold voltage of the MOSFET and in this way it is possible to memorize the information.

Fig. 1 shows a schematic cross section of a FG cell. The FG is completely surrounded by the insulator, preventing the charge loss. Today, the thickness of the SiO_2 layer that separates the FG and the channel is in the order of 8-10 nm. This layer is called Tunnel oxide, as it allows the passage of electrons by Fowler-Nordheim tunneling. The interpoly dielectric is the insulator layer separating the FG from the control gate, and it is formed by a stack of oxide-nitride-oxide ($SiO_2/Si_3N_4/SiO_2$), commonly referred as ONO. The ONO stack prevents any possible leakage current from the FG.

Fig. 2 reports some TEM cross section of FG cells where are visible the thin tunnel oxide layer of the ONO stack. In actual devices, the FG features hundreds of nm in thickness and the gate covers it even on the lateral sides in order to obtain a high capacitive coupling between FG and CG.

Electrons (or holes) can be injected into the FG though two different conduction mechanisms that is Fowler-Nordheim (FN) tunneling and Channel Hot Electron (CHE) injection [Cap99]. Conversely, only the FN tunneling is used to remove the electrons from the FG.

Once the electrons (or holes) are trapped into the FG, they remain trapped in this layer being the FG surrounded by insulator. As long as the charge remains in the FG, the memory cell preserves the stored information. Conventionally, FG Flash memories are expected to retain the

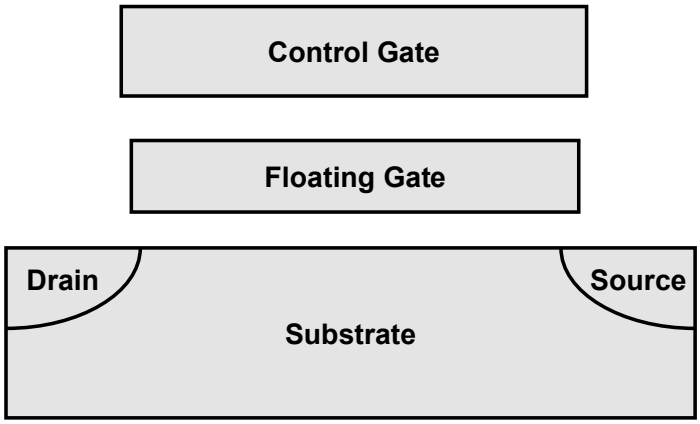


Fig. 1 Schematic cross-section of a Floating Gate Flash memory cell.

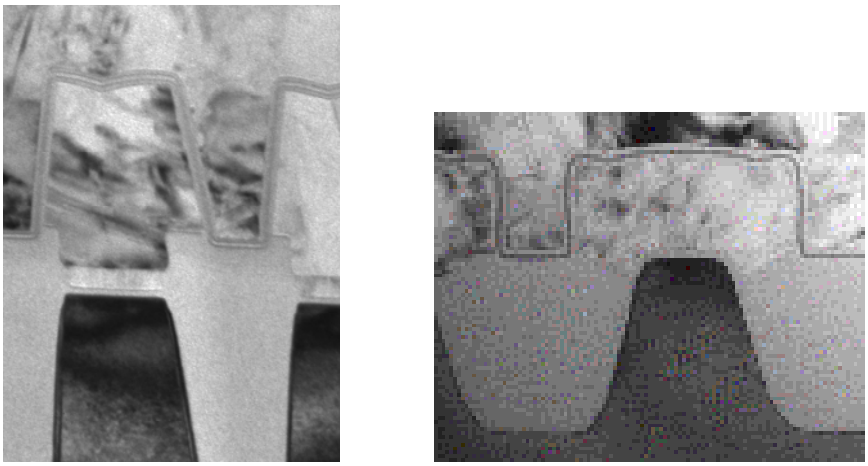


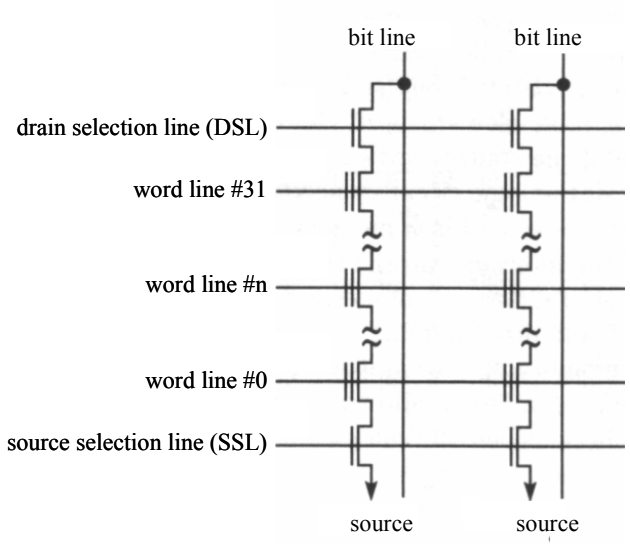
Fig. 2 TEM picture of Floating Gate Flash memory cells.

stored information for 10 years at least. For this reason one of the most important issues for the FG flash memory cells fabrication is the quality of the tunnel oxide and of the control dielectric.

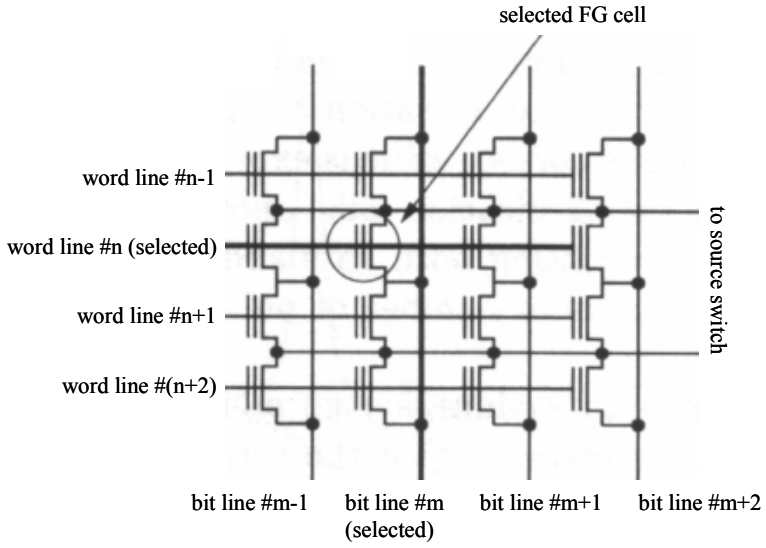
Two different array configurations are used in FG Flash memory chips: NOR or NAND. The NOR configuration (Fig. 3) features a high reliability and a fast random access; still it is very expensive in term of power and area. Conversely, the NAND configuration features a fast sequential access and it is more area and power efficient.

2. Floating Gate Flash Cells Scaling

In the ITRS Roadmap 2007 [Itr07] are clearly evidenced which are the most important issues to overcame in order to scale the Floating Gate Flash cells below the 45nm technology node. Looking at Fig. 4 [Itr07], we see that in few years both NAND and NOR technologies will face problems due to the scaling. In particular, for FG NAND Flash the most important issue to overcome will be represented by the interpoly dielectric. Today, an oxide/nitride/oxide (ONO) stack is used as interpoly dielectric in FG cells. This stack guarantee a long retention time especially thanks to the nitride layer that act as trapping layer preventing the formation of leakage currents. In the technology nodes below 35 nm, the ONO stack will be not enough to



(A) NAND



(B) NOR

Fig. 3 NAND (A)and NOR (B) array configuration.

guarantee the required cell retention capability and it should be replaced with a layer or a stack of high-K materials. With high-K materials it will be possible to have a relatively thick interpoly dielectric layer thus meeting the requirements in term of retention of the cell; at the same time, high-K materials will allow a high capacitive coupling between CG and FG. Still, as reported in the table of Fig. 4, no known solutions exist for the interpoly dielectric below the 32nm technology node.

Concerning the NOR technology, the situation is even worse. In this case the major issue is represented by the tunnel dielectric thickness that today is around 9 nm. In fact, a further reduction of the tunnel thickness will result in an unacceptable reduction of the FG cell retention characteristics and for this reason there are not known solutions for the NOR FG cells scaling below the 45nm technology node.

NAND Flash									
NAND Flash technology – F (nm) [1]	51	45	40	36	32	28	25	22	20
Number of word lines in one NAND string [2]	32	32	64	64	64	64	64	64	64
Cell type (FG, CT, 3D, etc.) [3]	FG	FG	FG	FG/CT	CT	CT	CT-3D	CT-3D	CT-3D
3D NAND number of memory layers	1	1	1	1	1	1	2	2	2
A. Floating Gate NAND Flash									
Cell size – area factor a in multiples of F^2 SLC/MLC [4]	4.0/2.0	4.0/2.0	4.0/1.3	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0	4.0/1.0
Tunnel oxide thickness (nm) [5]	6-7	6-7	6-7	6-7	6-7	6-7	6-7	6-7	6-7
Interpoly dielectric material [6]	ONO	ONO	ONO	ONO	ONO	High-κ	High-κ	High-κ	High-κ
Interpoly dielectric thickness (nm)	10-13	10-13	10-13	10-13	10-13	9-10	9-10	9-10	9-10
Gate coupling ratio (GCR) [7]	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7
Control gate material [8]	n-Poly	n-Poly	n-Poly	n-Poly	n-Poly	Poly/metal	Poly/metal	Poly/metal	Metal
Highest W/E voltage (V) [9]	17-19	17-19	15-17	15-17	15-17	15-17	15-17	15-17	15-17
Endurance (erase/write cycles) [10]	1.E+05	1.E+05	1.E+05	1.E+05	1.E+05	1.E+05	1.E+05	1.E+05	1.E+05
Nonvolatile data retention (years) [11]	10-20	10-20	10-20	10-20	10-20	10-20	10-20	10-20	10-20
Maximum number of bits per cell (MLC) [12]	2	2	3	4	4	4	4	4	4

(A)

A. Floating gate NOR Flash									
Cell size—area factor a in multiples of F^2 [22], [23], [24], [25]	9-11	9-11	9-11	9-11	9-11	9-11	9-11	9-11	9-11
Gate length L_g physical (nm) [26]	130	120	100	90	80	70	64	56	50
Tunnel oxide thickness (nm) [27]	8–9	8–9	8–9	8	8	8	8	7 - 8	7 - 8
Interpoly dielectric material [28]	ONO	ONO	ONO	ONO	ONO	ONO	High-κ	High-κ	High-κ
Interpoly dielectric thickness EOT (nm)	13-15	13-15	13-15	13-15	13-15	13-15	8-10	8-10	8-10
Gate coupling ratio [29]	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7	0.6–0.7
Highest W/E voltage (V) [30]	7-9	7-9	7-9	7-9	7-9	7-9	6-8	6-8	6-8
I_{read} (μA) [31]	25-34	23-31	21-27	20-26	19-25	17-22	15-20	14-19	13-18
Endurance (erase/write cycles) [32]	1.00E+05	1.00E+05	1.00E+05	1.00E+06	1.00E+06	1.00E+06	1.00E+06	1.00E+06	1.00E+06
Nonvolatile data retention (years) [33]	10–20	10–20	10–20	10–20	10–20	10–20	20	20	20
Maximum number of bits per cell (MLC) [34]	2	2	2	2	2	2	2	2	2
Array architecture (with cell contact (CC) or virtual ground (VG))[35]	CC	CC	CC	CC	CC	CC	CC/VG	CC/VG	CC/VG

(B)

Fig. 4 Scaling issues for NAND (A) and NOR (B) Flash [Itr07].

3. Non-Volatile Memories: New Solutions

Considering these concerns about the FG Flash scaling, most semiconductor companies are exploring new solutions for non-volatile data storing. There are two distinct ways to overcome the Flash memory scaling limits [Bez04].

One possible solution is represented by memories based on charge trapping, such as *Nanocrystal Memories* and *SONOS memories* [Des04, Des03, Sha04]. These devices have a structure similar to conventional FG Flash cells; however in these devices the charge is not stored in a monolithic FG, but into a layer of nanocrystals or of nitride. Being the charge trapped into discrete traps, the tunnel oxide thickness (and than the cell dimensions) of these devices can be reduced without a drastic reduction of the retention capability. In fact, in conventional FG Flash cells, a conductive spot due to oxide defects in the tunnel oxide may cause the lost of all the charge stored in the FG. On the contrary, in such new devices a single

conductive spot may discharge only a small part of the charge trapped near the spot location, while most of the charge would be preserved, resulting in a negligible variation of the cell threshold voltage.

One of the most important advantages of memories based on charge trapping is that they have a structure similar to conventional FG Flash cells. They use only common and well-known materials and the fabrication process is fully compatible with the standard CMOS technology. Moreover, it is relatively easy to memorize two or more bits per cell in such devices, being possible to inject the charge only near the source or the drain.

The other way to offer non-volatile memories with better performances and scalability, is to use new materials and alternative memory concepts such as FeRAM, MRAM or PCM.

FeRAM [Kim03] is the only alternative NVM that has been commercialized so far, even if several challenging technology problems, mainly related to new materials and new manufacturing technologies, are still limiting their diffusion.

The *MRAM* [Sla02] technology relies on the adoption of a tunnel junction coupled to magnetoresitive materials that exhibit changes in the electric resistance when a magnetic field is applied. However, their development has faced many challenges that impact the manufacturability of high-density devices.

The *PCM* technology [Pir03, Pir04, Bez06] is one of the best candidates to cover different NVM application fields, matching both the high density as well as the high performance specifications. PCM exploits thermally reversible phase transitions of chalcogenide alloys (e.g., $Ge_2Sb_2Te_5$). The basic cell structure is composed by one transistor and one resistor (1T/1R) that can be programmed through the current induced Joule heating, and can be read by sensing the resistance change between the amorphous and the polycrystalline phase. Despite this technology dates back to the ‘70 s, its application for NVM has known renewed efforts in these years, showing the capabilities to reach the maturity for manufacturability. To date, a common constrain to miniaturize an NVM cell beyond the 32 nm node is constituted by the selector transistor scaling. To address this issue, several zero-transistor cells have been so far proposed, as the 0T/1R threshold switching PCM cell (TF-RRAM) [Che03]. Although several concerns still exist on the performance, feasibility, and manufacturability, the cross-point NVM based on a zero-transistor cell is considered as the ideal solution to continue to follow Moore’s law, combining great interests for the research challenges and for the industrial potentialities.

Chapter 2

Radiation Effects Overview

Every electronic device is subjected to radiation. Even the PC you use in your office or in your house is subjected to a flux of ionizing particles that pass through its electronic components and that may cause a bit-flip or a soft error.

In the last years, the radiation effects on electronic devices have become a major concern for manufacturing companies, as demonstrated by the words of Intel's senior scientist Eric Hannah [Bbc08]: “What happens is if a cosmic ray causes a collision inside the silicon chip, that releases lots of charged particles. All our logic is based on charge, so it gets interference. The risk from cosmic rays may not be thought of as a big problem on a single computer with a single chip, as there is the potential for error only perhaps every several years. But on a supercomputer with 10,000 chips, there was the potential for 10 or 20 faults a week. And the risk of cosmic ray interference will only increase as chips get smaller. This is because circuits will require less charge per switch to operate. Since the amount of charge from cosmic rays will remain the same, there will be a "bigger disturb". And this is potentially a problem not just for PCs and supercomputers, but anything with computer-operated parts - for example cars.”

“You could be going down the autobahn at 200 miles an hour and suddenly discover your anti-lock braking system doesn't work because it had a cosmic ray event,” Mr Hannah said. “It's strange, but this is the reality we're moving into as we get smaller and smaller circuits.”

This chapter is organized as follow. The fist section is an overview on the radiation environments. In the second section we review the radiation effects on electronic devices, focusing on the single event effects and on the total ionizing dose effects. The last two paragraphs summarize the ionizing radiation effects on oxides and on FG Flash memories.

1. Radiation Environments

Nearly every chip is hit by some sort of radiation. Not even a circuit protected by several meters of concrete can be safe, since alpha particles can originate inside the chip due to radioactive contaminants.

In the following we will briefly describe the most important radiation environments, such as space, the atmospheric environment, the high energy physics environment and the nuclear power plant environment. The end of this paragraph is dedicated to another source of radiation: the alpha-emitter contaminants.

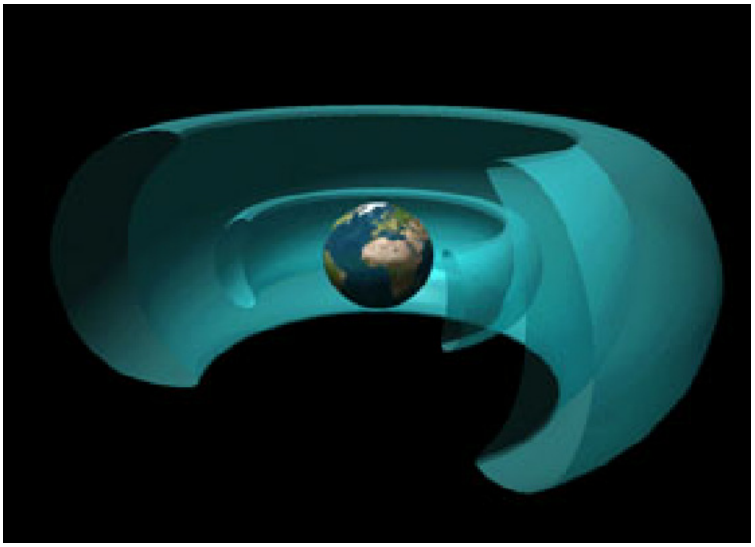


Fig. 1 Diagram of Earth's Van Allen radiation belts [Maz02].

1.1 Space radiation environment

1.1.1 Trapped Particles

Charged particles that come into contact with the Earth's magnetic field can become trapped in the near-Earth environment [Dod99]. These particles include electrons, protons, and heavy ions. The trapped particle belts (Van Allen belts, Fig. 1) consist of two regions of trapped particles: an inner and an outer belt, separated by a region of reduced particle flux (the so-called "slot" region). Although the origin of trapped particles in the near-Earth environment is not completely understood, sources include the solar wind and transient solar events, cosmic ray particles from interplanetary space, and reaction products from cosmic ray collisions with the Earth's atmosphere.

Protons

Regardless of origin, energetic protons do exist in the near-Earth environment and are one of the most prominent sources of damage on electronic devices. They range in energy from tens of keV to hundreds of MeV, with fluxes as high as 10^5 protons/cm^2/sec for protons with energy > 30 MeV [Bar97]. Protons with these energies are easily able to penetrate shielding and impinge on electronics within spacecraft [Lum04].

Probably the most important region for protons is the South Atlantic Anomaly (SAA), a region off the east coast of South America with greatly increased proton flux at altitudes less than 1000-2000 km. The SAA exists because of the difference between the Earth's geographic spin axis and its magnetic axis, which causes a localized region of lower magnetic field off the Argentine coast [Bar97, Dye98]. During passes through the SAA, the flux of energetic (>30 MeV) protons can be more than 10^4 times as intense than at equivalent altitudes over other regions of the Earth. The SAA is illustrated in Fig. 2, which shows flux contours for protons with energy > 30 MeV as a function of latitude and longitude at altitudes of 500 km (Fig. 2 a),

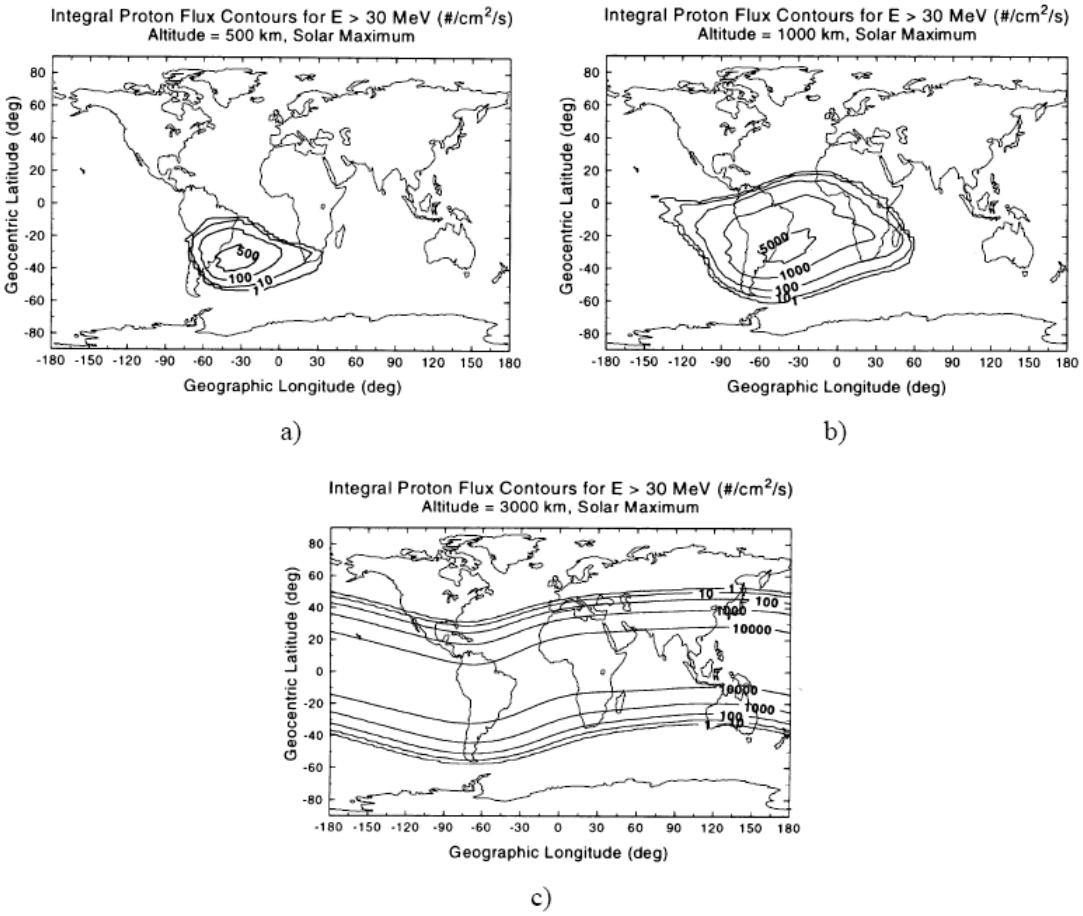


Fig. 2 Integral proton flux contours as a function of latitude and longitude [Dod99].

1000 km (Fig. 2 b), and 3000 km (Fig. 2 c). At low altitudes, the SAA is highly localized, and as altitude increases, the SAA becomes less distinct until at 3000 km (Fig. 2 c) the normal Van Allen belt structure re-emerges.

Heavy Ions

The Van Allen belts are predominantly composed of trapped electrons and protons, but it is now well accepted that heavy ions are also trapped by the Earth's magnetic field [Bar03]. The origin of these particles is thought to be anomalous cosmic rays, which are neutral interstellar particles that drift into the solar system, become ionized by the solar wind and accelerated to 10's of MeV/nucleon, and are subsequently trapped by the magnetosphere [Bar97]. Several kind of heavy ions have been measured, such as He, C, N, O, and Ne. The peak in trapped heavy ion fluxes is at altitudes just above the inner proton belt. Because the trapped heavy ions have relatively low energies (10's of MeV/nucleon), these particles may not penetrate through spacecraft shielding and therefore are not expected to be a major concern for electronic devices.

1.1.2 Transient Particles

Solar Event Protons and Heavy Ions

The activity level of the Sun is never constant, but follows a cyclical variation of active years followed by quiet years [Lum04]. The period of recent solar cycles has varied between 9 and 13 years, with an average of about 11 years. Solar cycle activity is frequently gauged by the observed number of sunspots, but many solar processes show the same variation. This includes the incidence of energetic solar events, with maximum numbers of solar flares occurring during active years. Solar events still occur during solar quiet times, but they occur less frequently.

Solar events can be broadly characterized as being either gradual or impulsive [Bar97]. The gradual events produce a raised particle flux that decays slowly over several hours or even days. These events are proton-rich and can produce high-energy (> 30 MeV) proton fluences higher than 10^9 protons/cm^2 accumulated over a few days. Gradual events are responsible for the majority of large proton fluence events, and occur at a frequency of about 10 per year during solar maximum conditions. Impulsive events are by definition of much shorter duration (hours at most), and are marked by increased fluences of heavy ions and low energy electrons. Impulsive events produce heavy ion fluences that can be orders of magnitude above the galactic cosmic ray background. These heavy ions have energies ranging from tens of MeV/nucleon to hundreds of GeV/nucleon, but at the upper end of this range the flux falls below the galactic cosmic ray background.

Galactic Cosmic Rays

Solar event particles are true transient particles in the sense that elevated fluxes of particles are observed only for a short time following an event. In contrast, galactic cosmic rays (GCR) form a background component of radiation that shows a slow cyclical variation with solar activity [Dod99, Sex92, Bar03]. GCR are composed of very highly energetic protons and heavy ions that come from outside the solar system. These particles must fight against the solar wind to enter the solar system and are therefore at their maximum intensity at solar minimum and drop off a factor of 2 to 10 at solar maximum. The particle composition of GCR is shown in Fig. 3. Protons comprise about 83% of the GCR flux, He nuclei (alpha particles) account for 13%, 3% are electrons, and the remaining 1% are heavier nuclei. Even though they are not very abundant, heavy ions are very important because they deposit the most energy per unit pathlength. Because they are so energetic (tens of MeV/nucleon to hundreds of GeV/nucleon), they do not become trapped and are not significantly attenuated by spacecraft shielding. GCR that hit the atmosphere form a cascade of secondary particles, as discussed in the next section.

1.2 The Atmospheric Radiation Environment

The atmospheric radiation environment comes about as a result of the space radiation environment impinging on Earth's atmosphere. As very highly energetic cosmic rays enter the upper atmosphere they interact with oxygen and nitrogen in the atmosphere and produce a cosmic ray shower of daughter products. The primary galactic cosmic rays are so energetic that

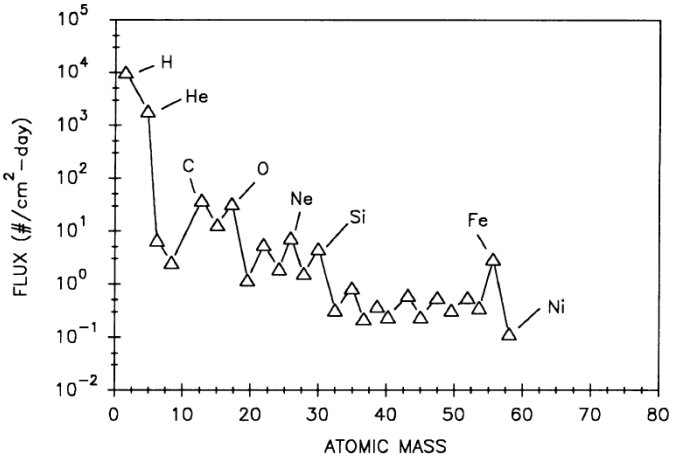


Fig. 3 Particle composition of galactic cosmic rays [Dod99].

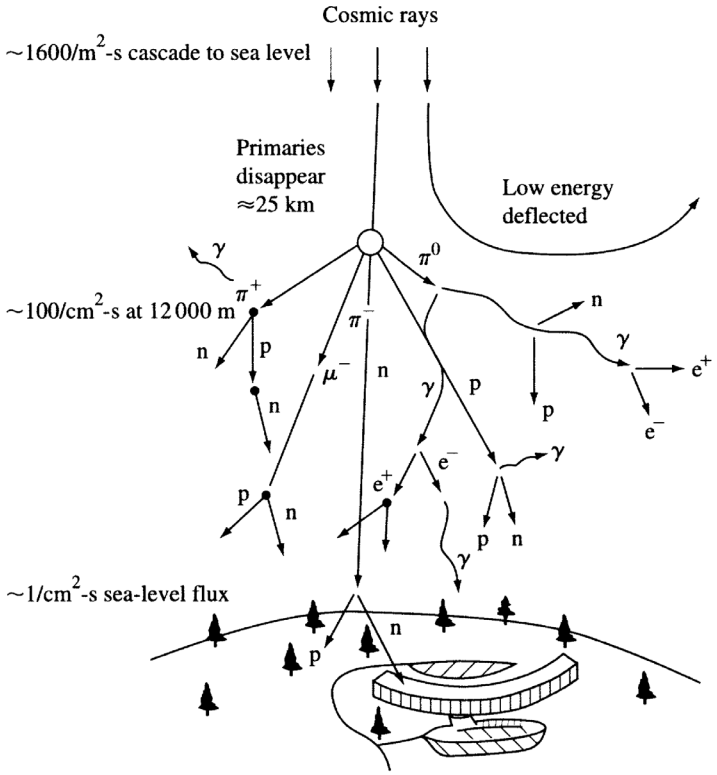


Fig. 4 Particle shower produced by cosmic rays [Dod99].

some of the daughter products can reach all the way through the atmosphere to ground level, equivalent to passing through more than 13 feet of concrete. A diagram of a cosmic ray shower is shown in Fig. 4 [Dod99]. The daughter products primarily responsible for causing soft errors in high-altitude and terrestrial electronics are neutrons and protons. The fluxes of neutrons and protons have similar characteristics with respect to energy and altitude variation, with both populations extending to energies greater than 1 GeV. Both neutrons and protons show a maximum flux at an altitude of 17-18 km, with the sea-level flux being several hundred times

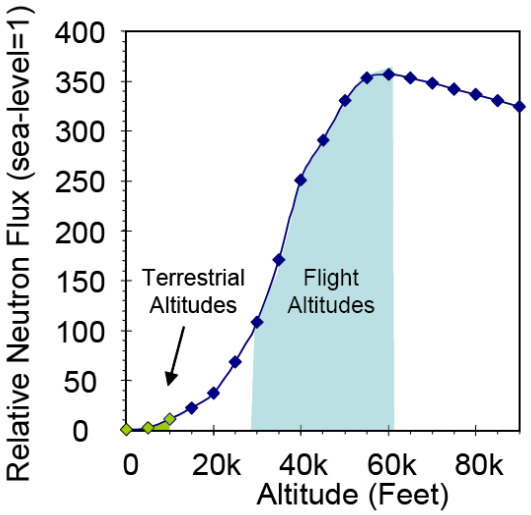


Fig. 5 Neutron flux variation with altitude [Bau05].

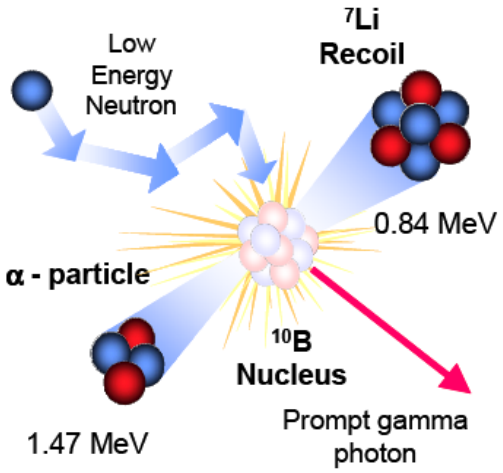


Fig. 6 Upon capturing a neutron the B nucleus becomes unstable and breaks apart, emitting two ionizing particles: a 1.47 MeV alpha particle and a 0.84 MeV lithium recoil [Bau05].

lower than at aircraft altitudes. A plot of the altitude variation of the neutron flux is shown in Fig. 5 [Bau05]. The neutron flux also varies as a function of latitude: the neutron flux is highest at the poles, because the primary galactic cosmic rays can penetrate furthest into the atmosphere there.

The neutron shower from cosmic rays hits atmosphere with a wide spectrum of energies, but they rapidly lose energy. Most atoms do not readily absorb neutrons, so the end of the cosmic shower is a flux of neutrons at their lowest energy. These are called *thermal neutrons*, and have about the same velocity as room-temperature atoms (~2000 m/s) [Bau05]. The thermal neutrons survive up to several seconds since few natural atoms interact with them. Thermal neutrons are a major concern for electronic devices as they may interact with Boron that is extensively used as a p-type dopant in silicon. Boron is composed of two isotopes, $_{11}B$ (80.1%) and $_{10}B$ (19.9%).

$_{10}B$ is unstable when exposed to neutrons and breaks into ionizing fragments shortly after absorbing a neutron as illustrated in Fig. 6 ($_{11}B$ also reacts with neutrons; however, its reaction cross-section is nearly a million times smaller, and its reaction products, gamma rays, are much less damaging). The thermal neutron capture cross-section of $_{10}B$ is extremely high in comparison to most other isotopes present in semiconductor materials - by 3 to 7 orders of magnitude [Bau05]. Unlike most isotopes that emit gamma photons after absorbing a neutron, the $_{10}B$ nucleus breaks apart with an accompanying release of energy in the form of an excited $_{7}Li$ recoil nucleus and an alpha particle (a prompt gamma photon is also emitted from the lithium recoil soon after fission occurs). The alpha and the lithium recoil are both capable of inducing soft errors in electronic devices.

1.3 High Energy Physics and Nuclear Power Plants

High energy physics experiments require the read-out electronics to work under extremely harsh conditions. As an example, it has been estimated that the read-out electronics used in the upgrade of the CERN Large Hadron Collider (LHC) would be subjected to Total Ionizing Dose (TID) close to hundreds of Mrad, with particle fluence up to 10^{16} hadrons/cm^2 after only 5 years of operation [Gon07].

Nuclear power plants are another harsh environment from the standpoint of radiation.

1.4 Alpha particles

Radioactive contamination is not rare. Luckily, almost all of this radiation is unimportant. Still, there is one type of radioactive contamination that can produce errors in an IC, that is trace of materials that emit alpha particles (a He nucleus). For example, the first evidence of sea-level soft errors on 16 Kb DRAMs was given by May and Woods (1979). The source of the radiation was traced to alpha particle emission from contaminates in ceramic packing produced in a factory on the Green River, Colorado, which was downstream from an old uranium mine [Zie04].

The prime source of alpha particles is from heavy elements such as thorium or uranium, and even the smallest trace contamination of some elements can cause serious problems. The contaminants maybe present into the package or into the solder materials. Unfortunately, these contaminants cannot be eliminated without incurring in extremely high costs.

2. Radiation effects on IC

Depending on the radiation environment in which the chips are immersed, ionizing radiation can produce different effects. Concerning CMOS circuits, there are two broad categories of radiation effects: *Single Event Effects* (SEE), which are due to a single strike of a particle with high ionizing power; and *Total Ionizing Dose* (TID) effects, which are due to the progressive build-up of defects caused by the passage of many particles with low ionizing power, such as electrons or protons.

2.1 Single Event Effects

2.1.1 Basic Mechanisms of Single Event Effects

All non-destructive single-event effects are caused by the same fundamental mechanism: collection of charge at a sensitive region of a microcircuit following the passage of an energetic particle through the device.

By definition, as ionizing radiation passes through a target material electrons and holes are released along the path of ionizing particles. There are two primary methods by which carriers are released: direct ionization by the incident particle and ionization by secondary particles created by nuclear reactions between the incident particle and the target material. Direct ionization can cause soft errors if the incident particle (such as a heavy ion) is ionizing enough to free a very high density of carriers. For lighter particles (e.g., protons), direct ionization may produce an insufficient amount of charge to cause upset directly and soft errors may instead be due to ionization produced by secondary particles.

Direct Ionization

An energetic particle passing through a semiconductor material frees charged carriers along its path as it loses energy. When all of its energy is lost, the particle comes to rest in the semiconductor, having traveled a total path length referred to as the particle's *range*. The terms *Linear Energy Transfer* (LET) or *dE/dx* is used to describe the energy loss per unit path length of a particle as it passes through a material. LET has the units of $MeV \times mg^{-1} \times cm^2$, because the energy loss per unit path length (in MeV/cm) is normalized by the density of the target material (in mg/cm^3). We can easily relate the LET of a particle to its charge deposition per unit path length, because for a given material it takes a certain amount of energy to release an electron-hole pair. For example, in silicon one electron/hole pair is produced for every 3.6 eV of energy lost, and silicon has a density of 2328 mg/cm^3. Using these values it is easy to show that an LET of 97 $MeV \times mg^{-1} \times cm^2$ corresponds to a charge deposition of 1 pC/μm. A curve of particular interest for understanding the interaction of a given energetic particle with matter is the LET of the particle versus depth as it travels through the target material. Fig. 7 shows such a curve for a 210-MeV chlorine ion traveling through silicon. This figure shows the basic characteristics of ion-induced charge deposition as a function of depth. A peak in the charge deposition occurs as the particle nears its range, and then a precipitous drop in deposition as the particle reaches its range and comes to rest. The peak in charge deposition is referred to as the *Bragg peak*, and in general occurs as the particle reaches an energy near 1 MeV/nucleon [Pet97].

Whether or not the charge deposited through direct ionization is sufficient to cause an upset of course depends on the individual device and circuit that has been struck as well as the strike location and trajectory. Direct ionization is the primary charge deposition mechanism for upsets caused by heavy ions. Lighter particles such as protons do not usually produce enough charge by direct ionization to cause upsets in memory circuits, but recent research has suggested that as devices become ever more susceptible, upsets due to direct ionization by protons may occur.

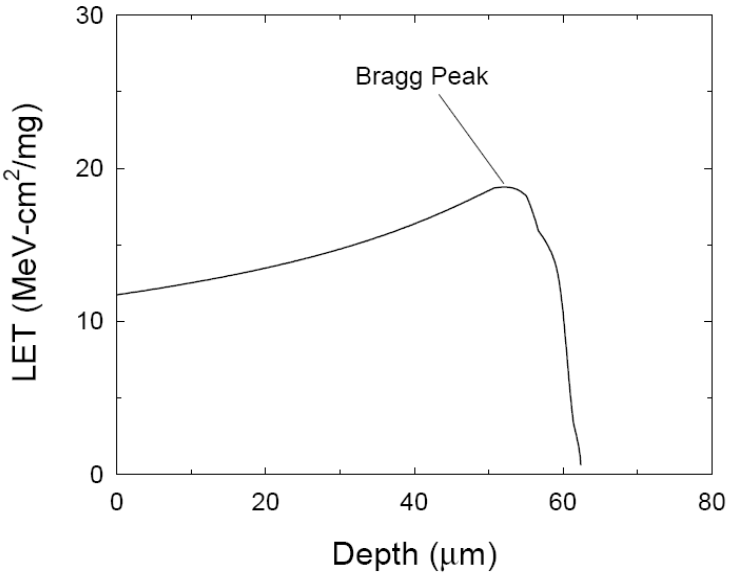


Fig. 7 Linear energy transfer (LET) vs. depth curve for 210-MeV chlorine ions in silicon [Dod99].

Nuclear Reaction Effects

As mentioned above, direct ionization by light particles usually does not produce a high enough charge density to cause upsets. Unfortunately, this does not mean that we can ignore these lighter particles. Protons and neutrons can both produce significant upset rates due to indirect mechanisms [Dod99]. As a high-energy proton or neutron enters the semiconductor lattice it may undergo an inelastic collision with a target nucleus. This may result in the emission of alpha (α) or gamma (γ) particles and the recoil of a daughter nucleus (e.g., Si emits α-particle and a recoiling Mg nucleus), or a spallation reaction, in which the target nucleus is broken into two fragments (e.g., Si breaks into C and O ions), each of which can recoil. Any of these reaction products can now deposit energy along their paths by direct ionization. Because these particles are much heavier than the original proton or neutron, they can deposit higher charge densities as they travel and therefore may be capable of causing a soft error. These inelastic collision products typically have fairly low energies and do not travel far from the particle impact site.

Once a nuclear reaction has occurred, the charge deposition is not greatly different in character from a directly ionizing heavy ion strike. Therefore, once deposited, it is subject to the same fields and concentration gradients and is collected in a similar manner.

2.1.2 Single Event Effects - Classification

A particle passing through a semiconductor can give rise to several different effects, depending on the type and bias conditions of the struck device, on the position of the ion hit and on the features of the impinging particles. The most important are [Dod99]:

Single Event Upset (SEU) also known as *soft error*, because it results in a loss of information and not in permanent damage to the affected circuit (hard error). When a particle strikes a

memory cell, it may cause a flip in the stored value, what was memorized as a '0' may become a '1' and viceversa.

Single Event Latch-up (SEL) occurs when the impinging particle activates parasitic BJT structures, causing high currents to be drawn from the power supply. A power-cycle is needed to restore proper operation, even though permanent damage may occur to the device during the high-current condition.

Single Event Functional Interruption (SEFI) occurs when a state machine controlling a device, such as a Flash memory or an FPGA, is upset by a heavy ion, causing a stop in the device operation.

Single Event Gate Rupture (SEGR) occurs when a particle with a high ionizing power impinges on a device biased over a critical voltage causing the rupture of the gate oxide, i.e., the formation of a conductive path which effectively shorts the anode and the cathode.

2.2 Total Ionizing Dose

Total ionizing dose effects are related to the progressive build-up of radiation-induced trapped charge and defects inside the exposed devices, caused by low-LET particles.

For MOS device degradation, the primary concern is electron-hole pair generation in oxides. Some fraction of the electrons and holes become trapped in the oxide and they may cause the release hydrogen and induce interface traps at the Si/SiO_2 interface.

2.2.1 Ionization Effects

High-energy electrons (secondary electrons generated by photon interactions or electrons present in the environment) and protons can ionize atoms, generating electron-hole pairs [Mcl87]. As long as the energies of the electrons and holes generated are higher than the minimum energy required to create an electron-hole pair, they can in turn generate additional electron-hole pairs. In this manner, a single, high-energy incident photon, electron, or proton can create thousands of electron-hole pairs. The minimum energy required for creating an electron-hole pair, E_p, in silicon, silicon/dioxide and GaAs is given in Table I [Sch02]. Also given in Table I are the densities for the three materials and the initial charge pair density per rad deposited in the material, g_0. The latter quantity is obtained from the product of the material density and the deposited energy per rad divided by E_p. A rad (radiation absorbed dose) is a unit used to quantify the total absorbed ionizing dose in a material. It is a measure of the amount of energy deposited in a material and is equal to 100 ergs of energy deposited per gram of material (1 rad = 100 erg/g = 6.24×10^{13} eV/g). The energy deposited in a device must be specified for the material of interest. Thus, for a MOS transistor, total dose is measured in units of rad(SiO_2) or rad(Si).

2.2.2 Basic Mechanisms of Total Ionizing Dose Effects

When an MOS transistor is exposed to high-energy ionizing irradiation, electron-hole pairs are created uniformly throughout the oxide. Electron-hole pair generation in the oxide leads to almost all total dose effects. The generated carriers induce the build-up of charge, which can lead to device degradation. The mechanisms by which device degradation occurs are depicted in Fig. 8 [Sch02]. Fig. 4 is a plot of an MOS band diagram for a p-substrate capacitor with a

Material	E_p (eV)	Density (g/cm^3)	Pair density generated per rad, g_0 ($pairs/cm^3$)
GaAs	~4.8	5.32	~7 x 10^{13}
Silicon	3.6	2.328	4 x 10^{13}
Silicon Dioxide	17	2.2	8.1x10^{12}

Table 1 Minimum energy for creating electron-hole pairs, density, and pair density generated per rad for GaAs, silicon, and silicon dioxide [Sch02].

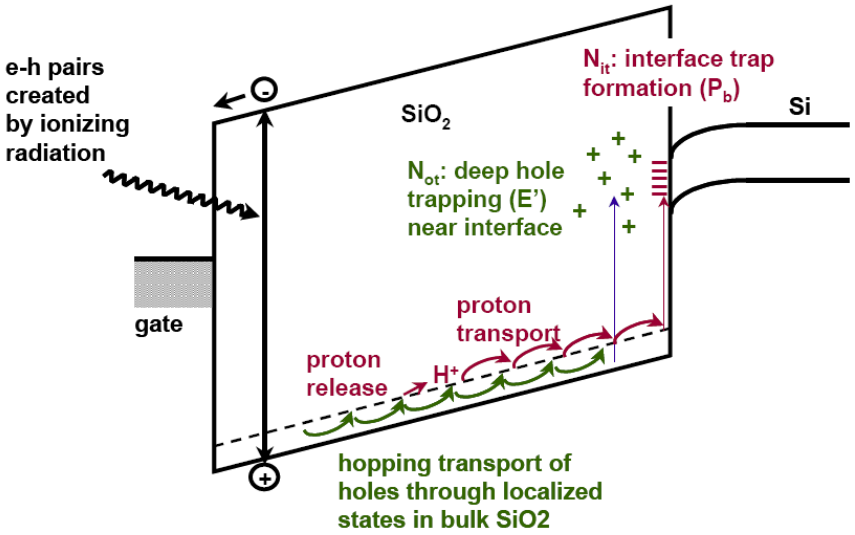


Fig. 8 Band diagram of an MOS capacitor with a positive gate bias. Illustrated are the main processes for radiation-induced charge generation [Sch02].

positive applied gate bias. Immediately after electron-hole pairs are created, most of the electrons will rapidly drift (within picoseconds) toward the gate and holes will drift toward the Si/SiO_2 interface. However, even before the electrons leave the oxide, some of the electrons will recombine with holes. The fraction of electron-hole pairs that escape recombination is called the electron-hole yield. Those holes which escape "initial" recombination will transport through the oxide toward the Si/SiO_2 interface by hopping through localized states in the oxide. As the holes approach the interface, some fraction of the holes will be trapped, forming a positive oxide-trap charge. Hydrogen ions (protons) are likely released as holes "hop" through the oxide or as they are trapped near the Si/SiO_2 interface. The hydrogen ions can drift to the Si/SiO_2 where they may react to form interface traps. At threshold, interface traps are predominantly positively charged for p-channel transistors and negatively charged for n-channel transistors.

In addition to oxide-trapped charge and interface-trap charge buildup in gate oxides, charge buildup will also occur in other oxides including field oxides and silicon-on-insulator (SOI) buried oxides [Bar05]. The radiation-induced charge buildup in gate, field, and SOI buried oxides can cause device degradation and circuit failure. Positive charge trapping in the gate oxide can invert the channel interface causing leakage current to flow in the OFF state condition (V_{GS} = 0 V). This will result in an increase in the static power supply current of an IC and may also cause IC failure. In a similar fashion, positive charge buildup in field and SOI buried

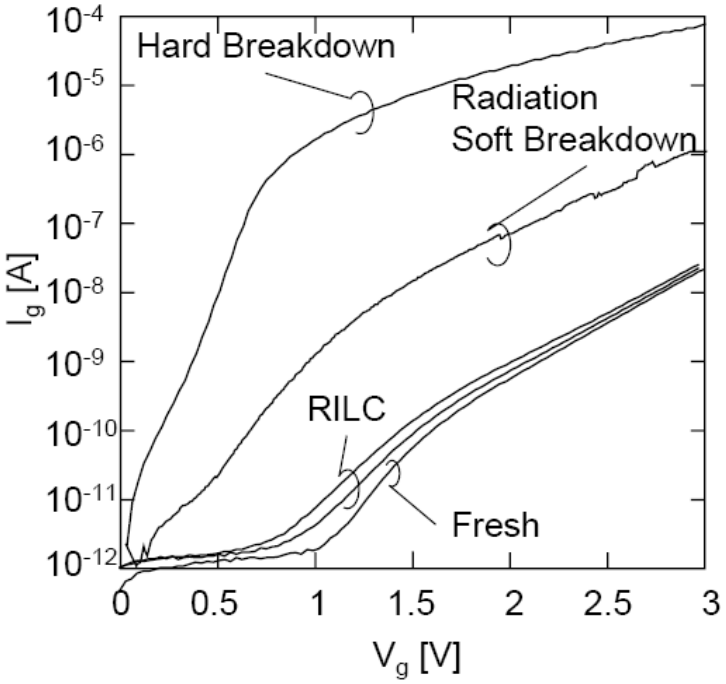


Fig. 9 Gate Current vs. Gate Voltage (Ig-Vg) measured before and after irradiation on a 3-nm oxide. The two curves referring to RILC have been measured after irradiation with $5.8 \cdot 10^{10}$ and $1.5 \cdot 10^{11}$ Si ion/cm^2. The RSB has been obtained after irradiation with 10^7 I ions/cm^2 [Ces01].

oxides can cause large increases in IC static power supply leakage current (caused by parasitic leakage paths in the transistor). In fact, for advanced ICs with very thin gate oxides, radiation-induced charge buildup in field oxides and SOI buried oxides normally dominates the radiation-induced degradation of ICs. Large concentrations of interface-trap charge can decrease the mobility of carriers and increase the threshold voltage of n-channel transistors [Bar05]. These effects will tend to decrease the drive of transistors, degrading timing parameters of an IC.

2.3 Radiation Effects on Oxides

The gate oxide thinning enhances the device radiation tolerance to charge trapping problems due to TID effects. In fact, being the electron tunneling distance around 3 nm in SiO_2, when the oxide thickness reaches 6 nm or less the radiation induced oxide positive charge is easily recombined or neutralized by electrons tunneling from the gate and/or Si substrate. This oxide thickness was approximately reached at the CMOS technological node of 0.25 μm. Following the CMOS technological evolution the gate oxide thickness is now below 2 nm, becoming almost immune to gate oxide charge trapping problems due to the gate oxide transparency to electrons. Still, this last characteristic has become the weak point from a reliability viewpoint [Pac03].

Ionizing radiation (as well as electrical stresses) can in fact produce defects acting not as trapping centers but as the agents of leakage paths across the gate oxide driving an excess gate current. Gate leakage adversely affects the overall circuit power consumption, which has been

often taken as the key parameter for reliability predictions. Fig. 9 resumes the different leakage currents that may be measured on a thin oxide after irradiation. The characteristics of the leakage currents depend on the oxide thickness and on the ionizing particle LET.

High LET particles may cause a huge increase of the capacitor current (Hard Breakdown). This phenomenon is known as *Single Event Gate Rupture* (SEGR) and it has been observed on relatively thick oxides irradiated under high oxide fields with high LET particles [Fle00, Sex98, Tit98].

Radiation Induced Leakage Current (RILC) was reported for oxides in the range 4-10 nm [Cec98, Cec00, Lar99]. On the contrary to SEGR, RILC is only a modest increase of the leakage current across the oxide (Fig. 9) and may be a severe limits for non-volatile memories. When the oxide thickness is scaled well below 4 nm, as in the contemporary CMOS technologies, the leakage current due to the direct tunneling of electrons across the oxide trapezoidal barrier is very large even in unstressed devices and RILC may be negligible.

Finally, *Radiation induced Soft Breakdown* (RSB) has been observed in 3 and 4nm oxides only after irradiation with high LET ions [Cec99, Cec99b, Cec00, Cec00b], and consists in a large increase of the oxide leakage current, which is however smaller than in Hard Breakdown regime.

2.3.1 Radiation Induced Leakage Current

The current density – oxide field characteristics (J_g-E_{ox}) of a 6-nm oxide are shown in Fig. 10 [Cec99], before and after a high dose irradiation with 8 MeV electrons produced by a pulsed LINAC accelerator. The main effect of irradiation is represented by the increase of the low-field gate current, observed between E_{ox}=3 MV/cm and E_{ox}=6 MV/cm, due to RILC. The oxide trapped charge in the stressed capacitors is negligible, as deduced from the overlap of the high-field characteristics of irradiated and unirradiated devices, corresponding to the FN tunneling regime.

RILC is attributed to the electrons passing through the oxide by Trap Assisted Tunneling (TAT) [Cec98, Cec00b, Lar99]. RILC features many similarities with Stress Induced Leakage Current (SILC), the main difference being the origin of the oxide traps: the ionizing particles for RILC, the electric stress for SILC. As SILC, RILC is attributed to inelastic TAT: when bias is applied to the gate, electrons can tunnel into the oxide trap where they loose part of their energy and then they reach the anode through another tunnel process (Fig. 11) [Cec98].

An analytical model of RILC has been developed for ultra-thin oxides submitted to ionizing radiation, based on the analytical solution of the Schrödinger equation for a simplified oxide band structure [Lar99]. Here RILC occurs through a two-step process: first, an electron tunnels into the oxide defect from the cathode conduction band edge. Then, the electron tunnels out the trap after having lost approximately 1.5 eV, in agreement with previous findings for SILC. Simulation results have shown that the most effective traps promoting RILC conduction are located close to the middle of the oxide and are energetically placed 1.3 eV below the oxide conduction band.

A leakage current that may be classified as RILC has been reported also in 10 nm thick oxide after heavy ion irradiation, as illustrated in Fig. 12 [Can01]. Before irradiation the FN injection is established at $|Vg| > 7$ V. After irradiation with I ions an excess leakage current appears between 5 V and 9 V, before and inside the FN regime. No current enhancement is observed after irradiation with Si ions. The excess current, measured in both negative and positive gate

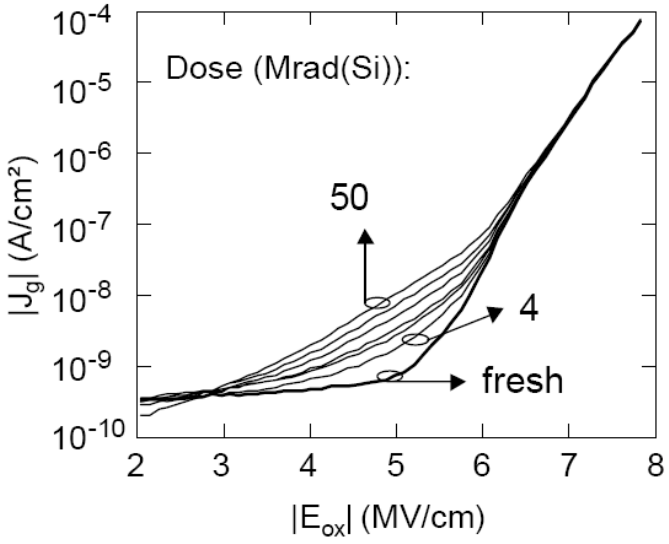


Fig. 10 Negative Jg-Eox curves measured before (fresh) and after irradiation for various doses ranging from 4 to 50 Mrad(Si) [Cec99].

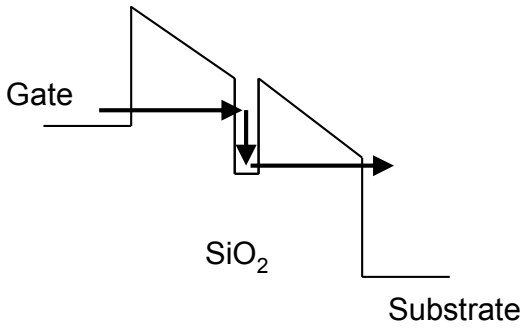


Fig. 11 Schematic representation of inelastic TAT through a MOS capacitor.

voltage sweeps, has been attributed to Multi-Trap Assisted Tunneling (M-TAT), as electrons should tunnel across the oxide through two or more traps. While conventional RILC and SILC may be modeled by inelastic Single-Trap Assisted Tunneling (S-TAT) [Lar99], in 10-nm oxides the tunneling probability to/from a trap 5 nm far from the interfaces is so low, that S-TAT could not support any measurable DC current. Noticeably, DC SILC has never been observed in 10-nm devices after electrical stresses [DeS00] (the main component of SILC after electrical stresses for tox≥10 nm is a transient current, caused by charging/discharging of stress generated traps near the oxide interfaces [Reu97]). This means that a critical trap density is needed for M-TAT, which can only be produced by ions with high LET, as low LET Si ions (see Fig. 12) are unable to produce the excess leakage. Only dense ion tracks can produce locally a high defect density, enabling M-TAT. Moreover, only high ion doses may generate M-TAT in 10-nm oxides: in fact, only for very high oxide defect densities the probability of having some traps aligned along a conductive path is high enough to produce a measurable leakage current.

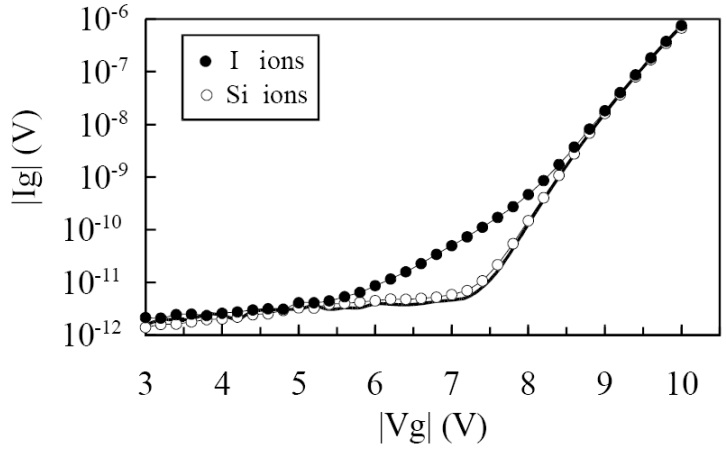


Fig. 12 I_g-V_g curve maeasured on a 10nm thick capacitor after 20 Mrad(Si) iodine (close circles) and silicon (open circles) irradiation. The solid line is the as-received negative I_g-V_g curve [Can01].

2.3.2 Radiation induced Soft Breakdown

The relative increase of the gate current due to RILC is much reduced in oxide thinner than 3-4 nm, due to the increased tunneling current even in a fresh device. A large impact on the gate current is measured instead when a Soft Breakdown (SB) event occurs [Cec99, Cec99b, Con01, Mal01, Mir00, Sex98]. RSB was detected as a sudden, large increase of the gate current, much larger than in case of RILC (see Fig. 9), but still smaller than in case of Hard Breakdown. The electrical characteristics of RSB are similar to those ones associated to the SB produced by electrical stresses [Cec00] and can be modeled following the empirical relation proposed for electrically induced SB [Mir99]:

$$I_{RSB} = a \cdot V^b$$

In contrast with RILC, which is associated to a tunneling process across a single trap, RSB conduction is activated when one or more regions with high defect density are produced in the oxide layer.

RSB is characterized by Telegraph Noise. Fig. 13 shows the gate current measured in a 3-nm oxide after irradiation with 257 MeV I ions, at Vg = -2.7V. The RSB current approximately behaves as a multi-level Random Telegraph Noise (RTN). Such fluctuations correspond to the activation/deactivation of conductive paths (inside the radiation induced weak spots) across the oxide, occurring after irradiation [Ces01]. By focusing on a small portion of the gate current response a “small” RTN appears superimposed on the main “large” fluctuations (see inset of Fig. 13).

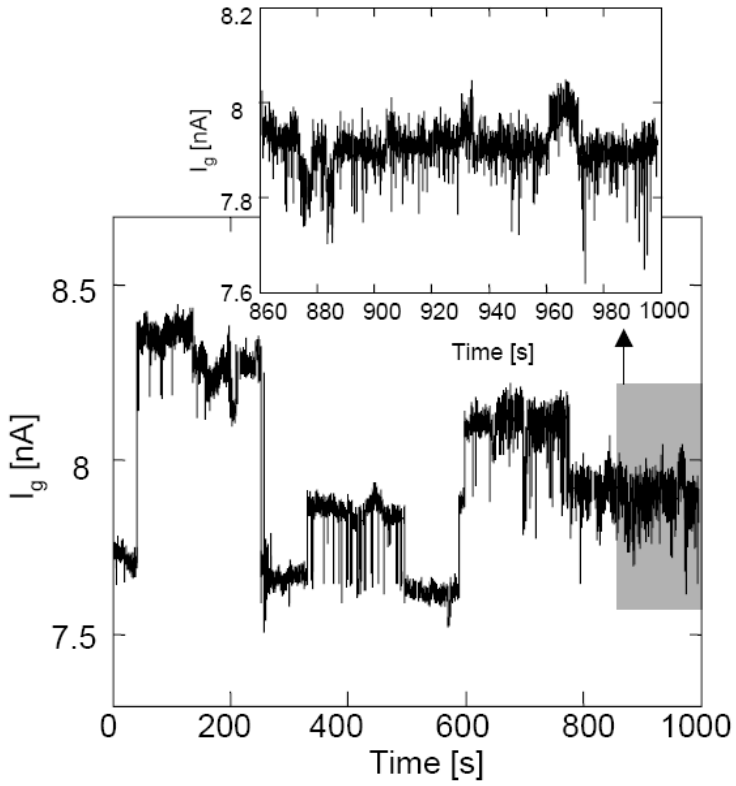


Fig. 13 Gate current measured at Vg=-2.7 V as a function of measurement time in a 3-nm oxide after $7 \cdot 10^6$ I ions/cm^2 [Ces01].

2.4 Radiation Effects on Floating Gate Flash Memories

2.4.1 Total Ionizing Dose Effects

The first model available for charge loss from FG was developed in 1989 for an EEPROM technology by Snyder *et al.* [Sny89]. According to this model, the charge loss from the FG is due to three contributions (see Fig. 14). Electrons and holes are generated in the oxides surrounding the FG. Electrons surviving recombination are quickly swept away, while holes will begin to slowly move toward the FG (through the tunnel oxide) because of the electric field produced by the charge stored into the FG. Part of them will be injected in the FG [contribution (1) in Fig. 14], while the remaining will be trapped in the oxide [contribution (2) in Fig. 14]. The contribution (3) in Fig. 14 is the photoemission of electrons stored in FG, where they gain enough energy from the impinging radiation to jump over the energy barrier of the oxide. This model proved good enough to describe experimental data.

Even if this model is still valid, it has some limits coming from the fact that it was developed for a technology of the late 1980s, having major differences with a modern one. For example, the FGs size was in the micrometer range (versus 0.13 nm or less of the modern technology); the tunnel and interpoly oxide thicknesses were 40 nm (versus 6–10 nm of the modern

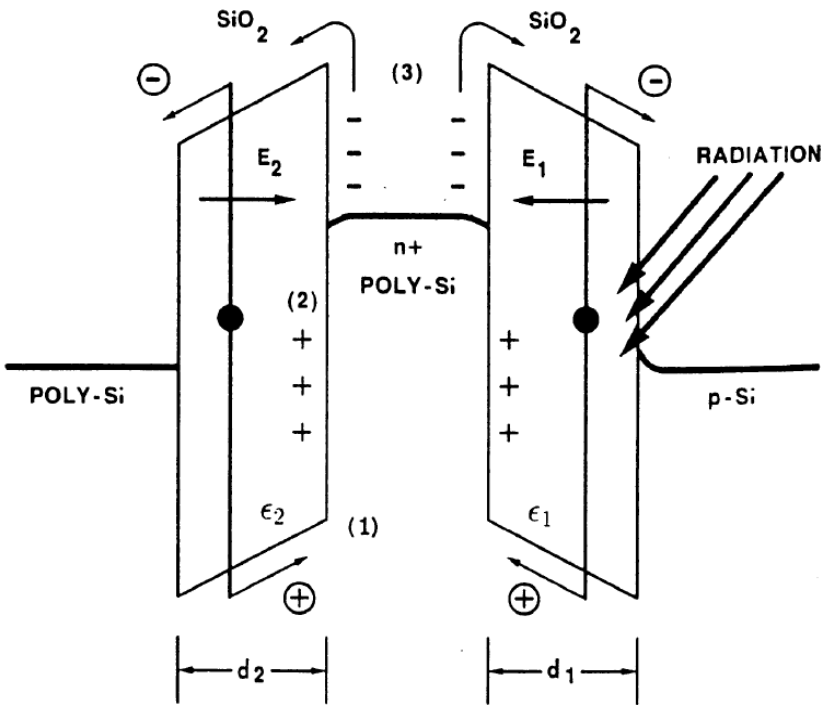


Fig. 14 Main contributions to threshold voltage degradation in an FG cell during TID experiments, according to [Sny89].

technology) and 47 nm (versus 16 nm) respectively; the interpoly oxide was a simple SiO^2 layer (now it is an ONO stack) [Cel04].

However, results obtained on a modern Philips technology after irradiation with γ-rays tends to confirm this model in its general ideas [Cel04, Cel04c, Wan04], as can be seen in Fig. 15. In agreement with Snyder's model, for the "0" ("1") state the result of irradiation is the reduction (increase) of FG, moving toward the "intrinsic" (that is, of the FG transistor with no charge stored in the FG).

2.4.2 Single Event Effects

The impact of a heavy ion has two main effects on a FG cell.

First, the ion causes the loss of part (or even all) the charge stored in the FG [Cel04d, Cel06c, Cel02]. When the ion passes through the FG cell, it produces a 4 nm wide cylinder of electron/hole pairs that fast recombine. The percentage of pairs that recombine depends on the electric field into the insulator and on the ion LET. The percentage of surviving holes and electrons strongly decreases when increasing the ion Linear Energy Transfer (LET) coefficient, i.e., the density of the electron-hole track: in denser tracks recombination is by far more efficient [Cel04d]. Still, before the recombination, this electron/hole pairs cylinder produced by the impinging ion act as conductive path causing a prompt discharge of the FG. Fig. 16 shows the cell distributions measured before and after irradiation with I and Ni ions. Note that the threshold voltage of the hit cells has noticeably reduced after irradiation, indicating a partial discharge of the FG.

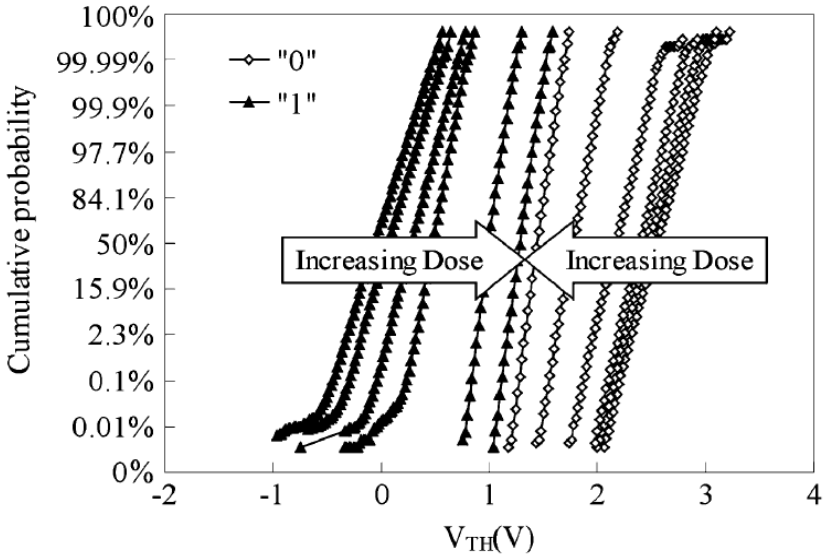


Fig. 15 Distribution of threshold voltages for Philips devices during irradiation with Co60-rays [Cel04b].

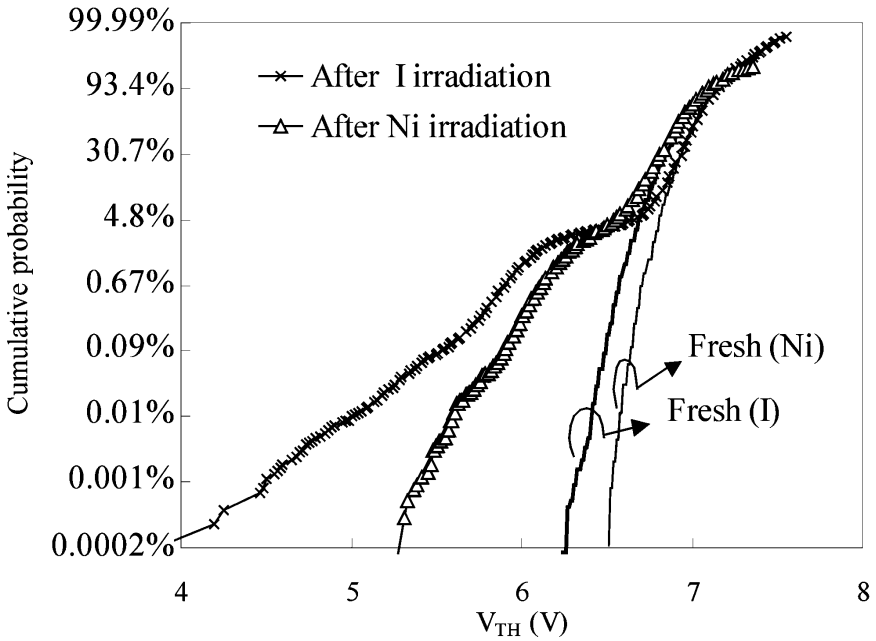


Fig. 16 Cumulative probability plot of threshold voltages of a Flash cell array before and after irradiation with 210 Iodine and Nickel ions [Cel05].

The second effect a heavy ion produces on a FG cell is the formation of defects along the ion track [Cel05, Cel06b]. Such defects cause tiny leakage currents similar to RILC. The electrons exploit these defects to pass from the FG to the substrate by M-TAT conduction thought the Tunnel oxide and this eventually results in a drastic reduction of the cell retention capability [Lar04]. As an example, Fig. 17 shows the cell distribution of a chip irradiated with I ions, measured after a re-programming operation following the irradiation, and then 1.5h, 48h and 164h after the re-programming. Some of the cells clearly feature a large threshold voltage reduction due to the charge loss from the FG caused by the ion induced defects into the tunnel oxide.

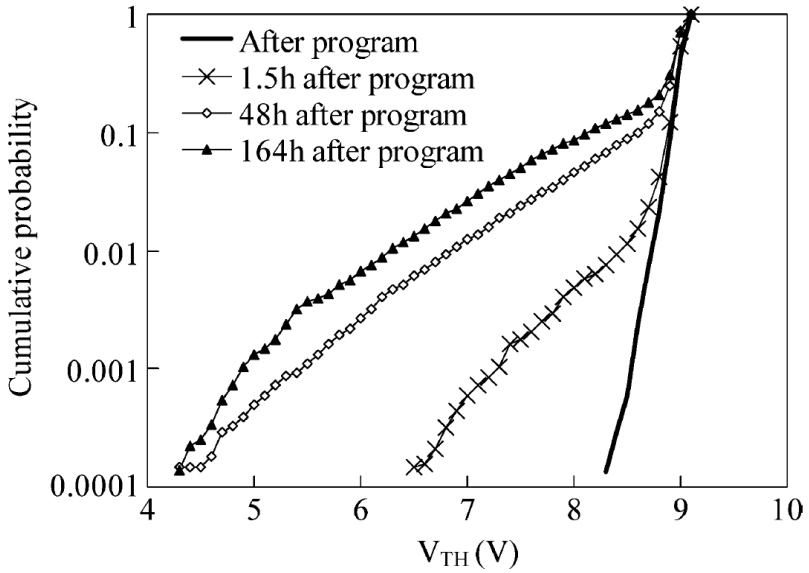


Fig. 17 Cumulative distribution of V for cells a Flash cell array hit by iodine ions, after being re-programmed [Cel05].

Chapter 3

Nanocrystal Memories

1. Introduction

Nanocrystal memories (NCM) [Des99, Ger04, Des04] represent the natural evolution of flash memories and present some important advantages with respect to other emerging technological approaches, such as ferroelectric or phase change materials, which require a more complex fabrication process and the use of uncommon materials. Instead, NCM fabrication is relatively simple and employs the materials commonly used in a typical CMOS process, adding very few steps.

The cross section of a nanocrystal cell is shown in Fig. 1. It resembles the conventional FG Flash cell in structure, but the continuous polysilicon FG is replaced by a layer of discrete and isolated Si nanodots, as illustrated in Fig. 2 reporting two TEM pictures of the nanocrystal layer.

Having replaced the floating gate with a nanocrystal layer, NCM present a better resistance than standard FG memories against SILC disturbance. In fact, in NCM only a small number of nanocrystals (NC) should be discharged by a single weak spot due to preexisting and/or stress induced defects inside the tunnel oxide. This permits the preservation of the charge in most of the discrete storage nodes and the improvement of the retention characteristic. Therefore, additional advantages are obtained with this structure, such as the better scalability of the tunnel oxide thickness and the consequent lowering of programming/erasing voltages [Des03]. NCM cells also feature reduction of the drain induced turn-on effect [Com06] thanks to the limited coupling between drain and nanocrystals. Moreover, with this structure it is easily possible to store two bits in a single cell [Cor03], injecting charge only in the nanocrystals close to the drain or to the source, thus increasing the data density that could be stored in a chip.

This chapter is organized as follows. The first part deals with the results of the radiation experiments on NCM: Paragraph 1 investigates Total Ionizing Dose effects while Paragraph 2 is dedicated to Single Event Effects.

In the second part, we study peculiar electrical properties of NCM cells by using TCAD simulations.

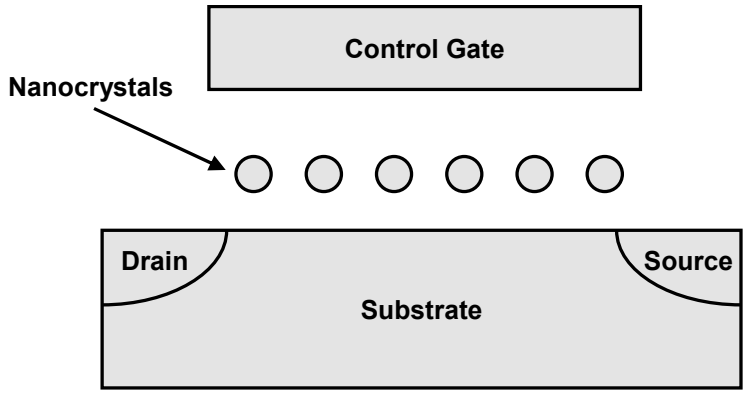


Fig. 1 Schematic cross-section of a generic nanocrystal memory cell.

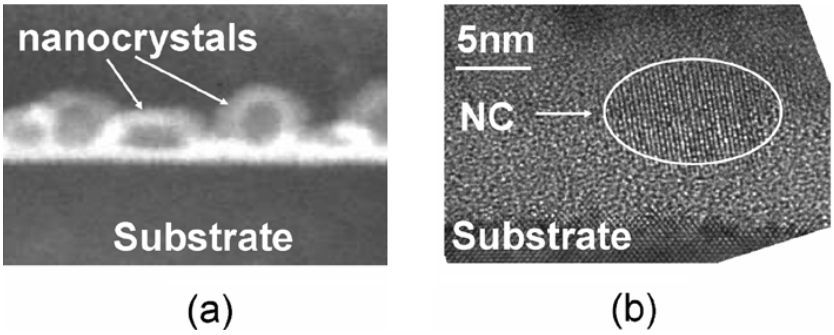


Fig. 2 TEM cross-sections of the nanocrystal layer.

2. Nanocrystal Memory Cells

NCM have been provided by STMicroelectronics (Catania, Italy). They feature a channel length of 0.3 μm and a channel width of 0.2 μm; the tunnel oxide is 5 nm thick and the control gate oxide consists of an ONO stack with an equivalent oxide thickness (EOT) of 12 nm (Fig. 3). In detail, the physical thickness of the bottom oxide in the ONO stack is 4.5 nm; the nitride layer is 6 nm; and the top oxide is 5 nm. Each of these three layers was produced by chemical vapor deposition (CVD). The silicon nanocrystal layer was deposited by low pressure CVD (LPCVD) in the Si nucleation regime using SiH_4 as a precursor [Amm02], using standard semiconductor equipment. A post deposition annealing was carried out in order to crystallize the Si islands. A nanocrystal density of $5 \cdot 10^{11} cm^{-2}$ was determined by TEM measurements, with an average nanocrystal diameter of 6 nm. Each cell contains about 300 nanocrystals. We measured both single cells and CAST (Cell Array Stress Test) [Cap97], that are arrays of 256k cells connected in parallel, with common terminals. Through the CAST structure, we can measure the average cell behavior, and we are also able to detect the presence of a few defective tail cells. In particular, with this structure we can recognize the presence of few cells with a V_T lower than the mean CAST V_T, because in this case we would see a bump in the I_{DS}-V_{GS} CAST characteristic, due to the anticipated turn-on of these anomalous cells. However, we are not able to detect the presence of few cells with V_T higher than the mean CAST V_T; in fact, when most of the cells in the array are conducting, the I_{DS} of the CAST saturates and we cannot see the variation due to few high V_T cells.

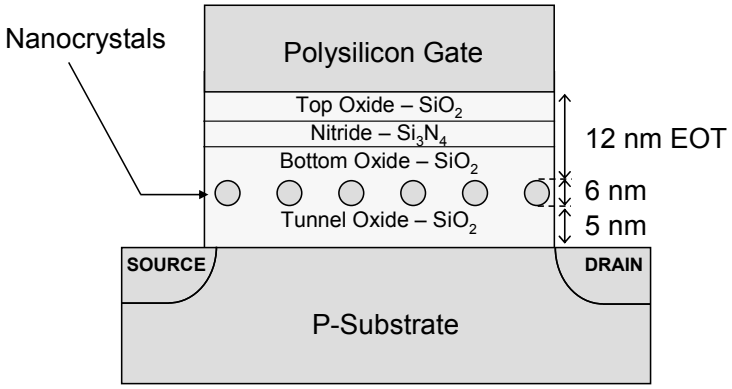


Fig. 3 Schematic cross-section of a nanocrystal memory cell.

The programming (P) and erasing (E) operations were performed through Fowler-Nordheim (FN) injection, by applying a gate voltage of +15 and -15 V for 2 ms, with the other terminals grounded. Single cells can be programmed also through CHE. Still, it is impossible to program CAST through CHE due to the external series resistance of these structures. For this reasons we chose to use FN injection for both single cells and CAST, in order to compare easily the data.

Due to the reduction of the tunnel oxide thickness, the voltages used for the FN programming/erasing operations are slightly lower than that used in the current Flash technology, in which the total potential difference between control gate and substrate is higher than 15 V during FN P/E operations. Noticeably, a further reduction of the programming voltages can be achieved programming through CHE.

While a "programmed" cell stores a net negative charge in the nanocrystal layer, producing a high threshold voltage, an "erased" cell stores a net positive charge corresponding to a low V_T. We have estimated that after programming each nanocrystal stores about 3-4 electrons.

Fig. 4 shows the I_{DS}-V_{GS} characteristic of a CAST in the programmed and erased state. The exponential behavior typical of the MOSFET subthreshold conduction appears for 1 V < V_{GS} < 2.5 V in the P and -1 V < V_{GS} < 0.8 V in the E state, respectively. The drain current is clamped at about 3 mA by the external CAST series resistance. The programming window (i.e., the difference between programmed and erased threshold voltage) is about 2 V. The threshold voltage was extrapolated from the I_{DS}-V_{GS} curves in the sub-threshold region at a fixed current of 10 μA in CAST and of 10 nA in single cells.

3. Irradiation Effects on Nanocrystal Memories

3.1 Total Ionizing Dose Effects

3.1.1 Irradiation experiments

Irradiation was performed at the 2.5 MV AN2000 Van de Graaff accelerator [Boc96] at the INFN Legnaro National Laboratories, Italy. We have irradiated samples with 2 MeV protons (LET = 0.11 MeV·mg^{-1}·cm^2) at the wafer level.

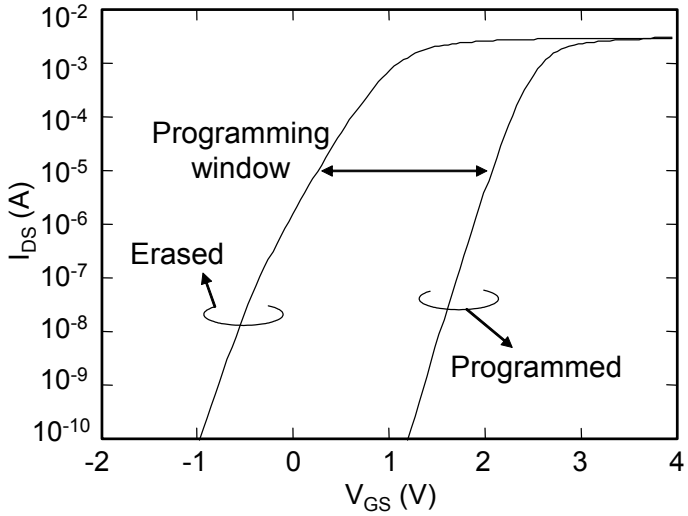


Fig. 4 I_{DS}-V_{GS} characteristic of a CAST in the programmed and in the erased state.

TABLE I IRRADIATION DOSES AND FLUENCES USED IN PROTON IRRADIATION EXPERIMENTS

Fluence (p/cm^2)	Dose (SiO_2)	Ion hits/cell
$5.7 \cdot 10^{10}$	100 krad	34
$5.7 \cdot 10^{11}$	1 Mrad	340
$5.7 \cdot 10^{12}$	10 Mrad	3 400
$5.7 \cdot 10^{13}$	100 Mrad	34 000
$5.7 \cdot 10^{14}$	1 000 Mrad	340 000

Irradiation was performed with fluences ranging from $5.7 \cdot 10^{10}$ to $5.7 \cdot 10^{14}$ protons/cm^2, that correspond to 100 krad(SiO_2) and 1 Grad(SiO_2), respectively. It has been estimated that 34 and 340000 protons hit the gate area of each cell at the lowest and at the top fluence, respectively. Table I reports the details of the irradiation data. During the irradiation experiments the device terminals were kept floating. Being the memory cells in high impedance state for most of their operating life, to keep floating the device terminals during irradiation is a good approximation of the typical operating condition [Old05]. One half of the total number of cells and CAST used in the irradiation experiment were in the programmed state and one half in the erased state during the irradiation. Measurements were performed 24 hours after irradiation.

3.1.2 Charge lost during irradiation

Figs. 5 A and B show the I_{DS}-V_{GS} characteristics of a CAST and of a single cell, respectively, taken before and after irradiation with $5.7 \cdot 10^{12}$ protons/cm^2 (10 Mrad (SiO_2)). Devices irradiated in the erased state show only negligible variations with respect to programmed devices and are not shown for clarity in the figure that is relative to CAST and single cell in the P state during the irradiation. The I_{DS}-V_{GS} curves change appreciably after irradiation (see curves (1) and (3)). This variation is due to the decrease of the net negative charge stored in the nanocrystals, as summarized in Fig. 6 for the CAST V_T measured immediately after irradiation. The programming window progressively decreases at increasing fluence, similar to the behavior of

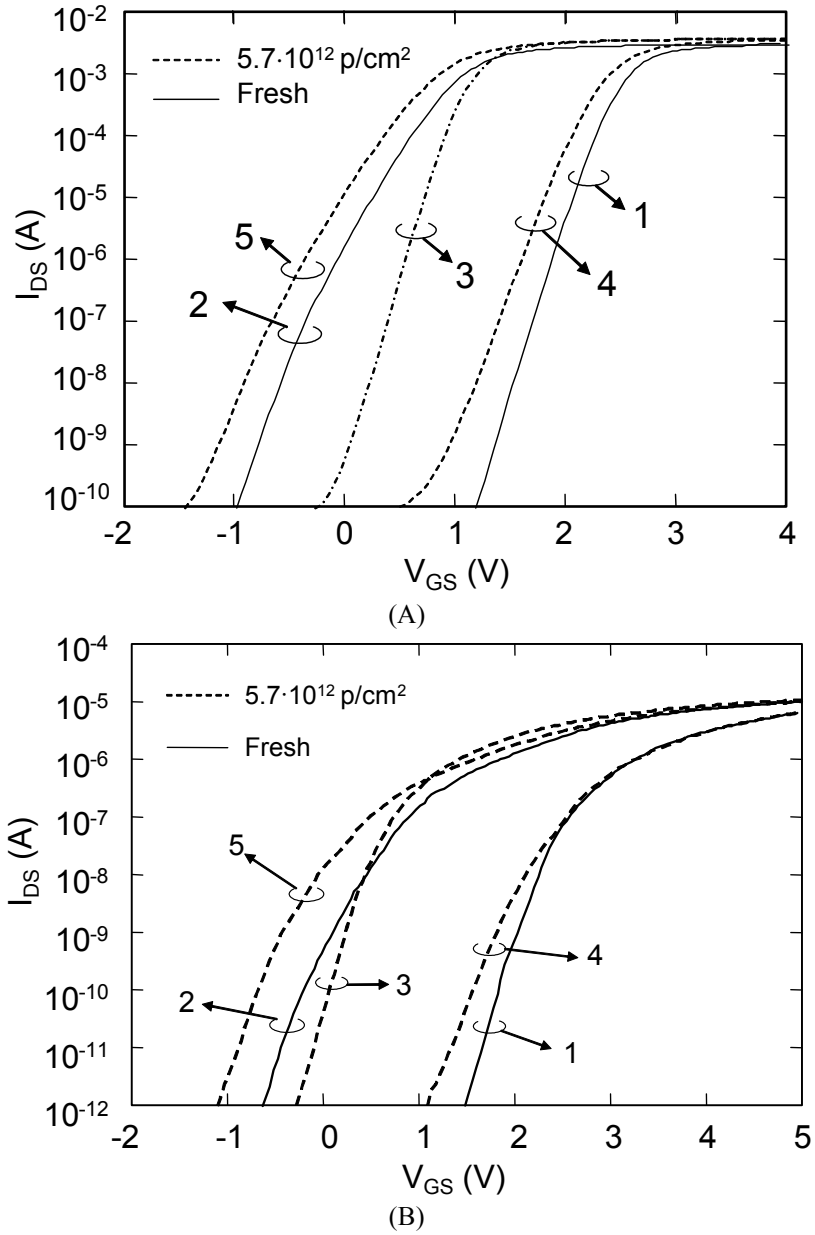


Fig. 5 I_{DS}-V_{GS} characteristics of a CAST, (a), and cell, (b), before and after proton irradiation. Curves (1) and (2) were taken with the devices in the programmed and the erased state, respectively, before the irradiation. Curve (3) were taken immediately after the irradiation with a fluence of $5 \cdot 10^{12}$ protons/cm^2. Curves (4) and (5) were taken after a programming and erasing operation, respectively, performed after the irradiation. CAST and cell showed here were irradiated in the programmed state.

irradiated FG Flash memories [Cel04]. After 10 Mrad(SiO_2), the charge stored in nanocrystals is completely lost. After 1 Mrad, NCM cells have lost only half of their stored charge.

Due to irradiation the NCM V_T moves toward its intrinsic value, corresponding to zero net charge in the nanocrystals. Both electrons and holes produced by the 2 MeV protons in the oxides surrounding the nanocrystals are subjected to the electric field produced by the charge stored in the nanocrystal layer. When nanocrystals are negatively (positively) charged, holes (electrons) produced by the ionizing particles are attracted toward the nanocrystals and they may recombine with the stored charge, while electrons (holes) drift far away from nanocrystals.

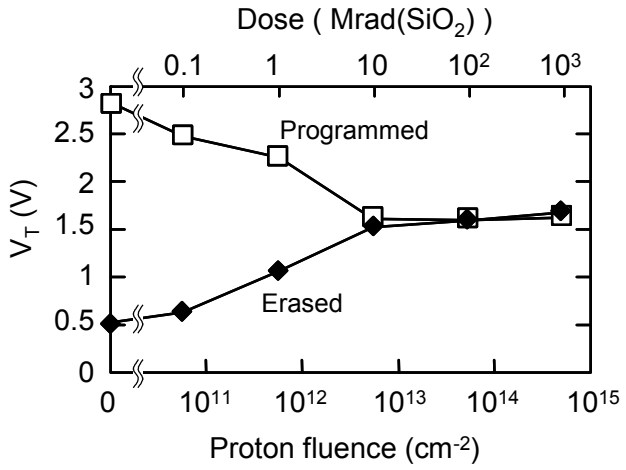


Fig. 6 Threshold voltage measured immediately after irradiation as function of proton fluence in both programmed and erased CAST.

The charge generated by the ionizing radiation in the nitride layer should not have any important role in the nanocrystal neutralization process, as the charge yield is almost zero in the nitride [Cel04, Cel04c]. Also, electrons and holes generated in the top oxide over the nitride layer may hardly contribute to the neutralization of the charge stored in the nanocrystal layer, being easily trapped at the nitride interface. The reduction of the tunnel oxide thickness with respect to FG Flash memories (5 nm vs. 8-10 nm in Flash) results also in a smaller quantity of charge produced by radiation in the oxide that can neutralize the stored charge.

Photoemission current, i.e., electrons that gain enough energy from the radiation to escape from nanocrystals, may contribute as well to the net charge loss from nanocrystals [Cel04]. Cellere, et al., [Cel04c] have shown that flash memory cells with smaller FG area loose a smaller quantity of charge during irradiation, due to the reduction of the photoemission contribution. From this point of view, our devices are less sensitive to the photoemission than floating gate memories, because the area covered by nanocrystals is only 15% of the total gate area.

3.1.3 NCM MOSFET electrical characteristics

Curves (4) and (5) in Fig. 5A represent the I_{DS}-V_{GS} characteristics of the NCM CAST after P and E operations following irradiation, respectively. Both curves shift by -260 mV with respect to the pre-irradiation ones, with negligible variations of the programming window. The single cell shows a similar behavior (Fig. 5B). In Fig. 7, the average threshold voltage shift of the P and E states for five CAST is plotted as a function of proton fluence. The negative V_T shift increases with the proton fluence, with negligible differences between the V_T measured in the P and E states. This shift is due to positive charge trapping, usual in thick oxides [Sch02]. Identifying the net charge location in our devices is however not straightforward. The positive charge cannot be trapped in the thin tunnel oxide, where it can be easily neutralized by electrons tunneling through the thin dielectric layer (5 nm). Positive charge should not be trapped in the nitride layer, which is more prone to electron trapping and more conductive for holes [Deg96]. Hence, this positive charge should be trapped at the nitride/oxide interface [Hol02] or within the oxide layer over the nanocrystals, far enough from the channel interface and from nanocrystals

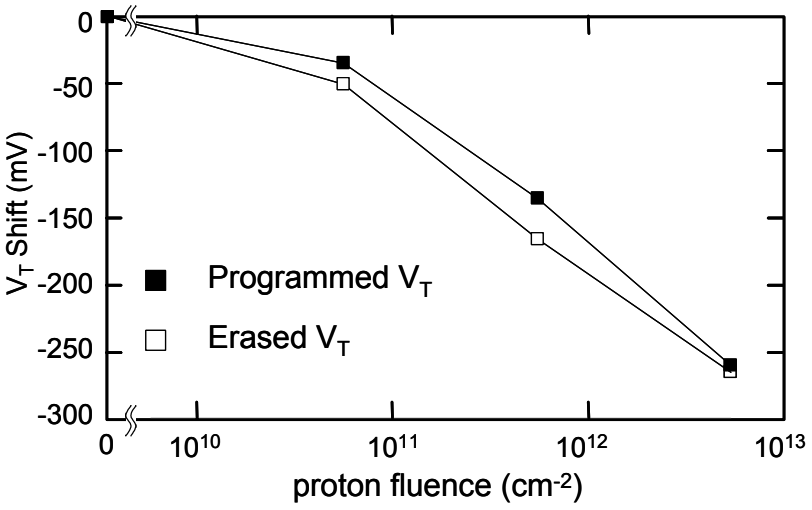


Fig. 7 Threshold voltage variation between fresh and irradiated devices as a function of the fluence. The irradiated devices were programmed or erased before the measurements.

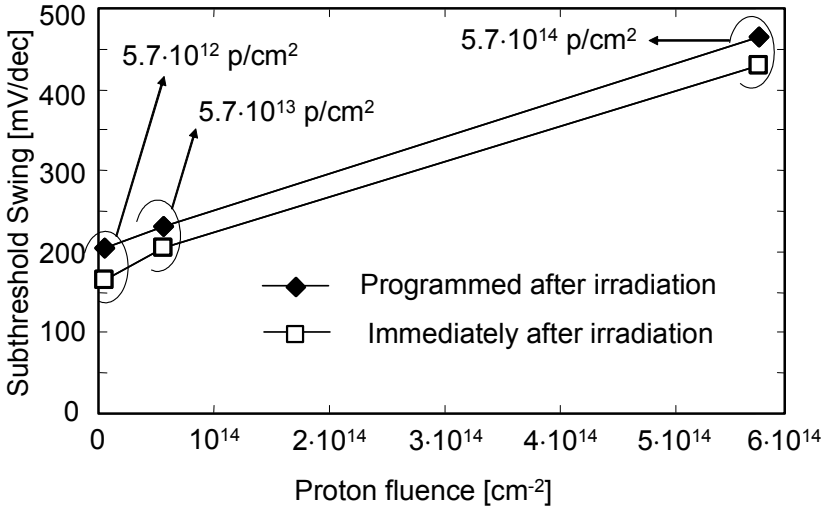
to make electron tunneling unlikely. From the V_T shift of 150 mV that observed in devices irradiated at the fluence of $5.7 \cdot 10^{11}$ protons/cm^2, we calculated that the density of the positive trapped charge is between $1.6 \cdot 10^{11}$ (100 h per cell) and $6.5 \cdot 10^{11}$ holes/cm^2 (390 h per cell), depending on the position of the charge in the oxide.

It is really hard to make a rigorous calculation of the radiation induced charge surviving prompt recombination. On one side, in fact, the discrete nanodots produce a non-uniform electric field in the SiO_2; on the other side, the charge stored in nanocrystals progressively neutralizes, resulting in a gradual variation of the electric field and then of the fraction of the radiation generated charge in SiO_2 that survive prompt recombination. Still, we have estimated that in the case of irradiation with 1 Mrad(SiO_2) about 600-700 e/h pairs per cell generated by radiation survive the prompt recombination. This value is higher than the positive trapped charge (100-390 h per cell): the difference can be explained taking into account the overestimation in the calculation of the number of e/h pairs produced by radiation, due to the neutralization of the charge stored in nanocrystals, and the possible escape from the oxide of some holes produced by radiation.

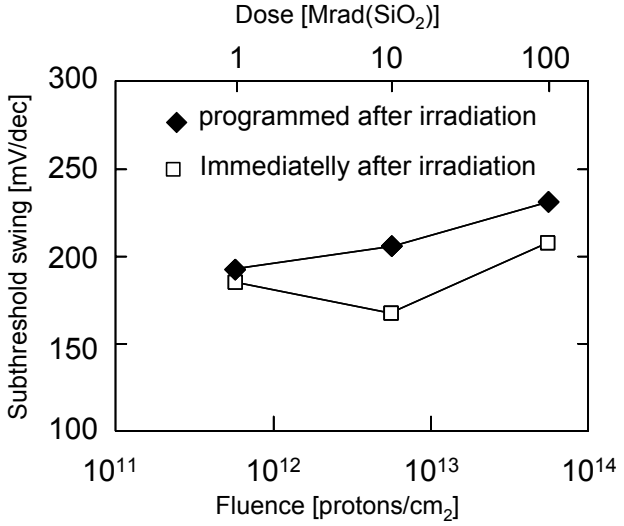
Quite surprisingly, the radiation induced V_T shifts remain constant even after several P and E steps following irradiation, arising some intriguing questions. In fact, if the V_T shift would be due only to a fixed positive trapped charge, this charge should be easily neutralized by electrons injected during subsequent P/E operations [Can01], in contrast with the observed results.

3.1.4 Subthreshold slope

Back to Fig. 5, it is worth to note the peculiar behavior of the subthreshold regions of the I_{DS}-V_{GS} curves. The subthreshold swing of unirradiated CAST is 182 mV/dec in the P state (curve (1)). The subthreshold swing measured immediately after irradiation (curve (3)) is comparable to the swing of the device in the P state before irradiation (curve (1)), and it is much smaller than in the P (curve (4)) or E (curve (5)) state of irradiated devices. This difference is clarified in Figs. 8 A and B, reporting the subthreshold slope of irradiated devices before and after the re-programming operation. In particular, Fig. 8 A shows the subthreshold slope of



(A)



(B)

Fig. 8 Subthreshold swing of the I_{DS}-V_{GS} characteristics measured in CAST immediately after irradiation and after a programming operation following the irradiation as a function of the fluence (high fluences in (a), low fluences in (b)).

devices irradiated at fluences ranging from $5.7 \cdot 10^{12}$ to $5.7 \cdot 10^{14}$ protons/cm^2. For clarity, Fig 8 B separately shows the subthreshold swing of the devices irradiated at low fluences from $5.7 \cdot 10^{11}$ to $5.7 \cdot 10^{13}$ protons/cm^2. The swing of re-programmed devices linearly increases with the proton fluence, due to accumulation of Si/oxide interface defects (N_{it}) produced by irradiation.

It is worth to note that for high doses (Fig. 8 A) there is an almost constant difference of about 30 mV/dec in the swing of the I_{DS}-V_{GS} characteristic measured immediately after irradiation and after a reprogramming operation. In contrast, in devices irradiated at 1 Mrad(SiO_2) we see only a small difference in the subthreshold swing, as reported in Fig. 8 B. This effect is a peculiar aspect of irradiated NCM, never observed in FG cells.

Interface defects at the Si/oxide give the same contribution to the subthreshold swing in the I_{DS}-V_{GS} measurements taken immediately after the irradiation and after the re-programming operation. In fact, at a fixed drain subthreshold current, the band bending at the silicon/oxide

interface should be the same independently on the charge state of the nanocrystals. Consequently, also the interface state occupancy should be independent on the nanocrystal charge state. So, the different swing of the re-programmed curve should be independent from these defects and it must be related to other factors.

These data can be explained considering the discrete nature of silicon nanodots. When nanocrystals are positively or negatively charged, the MOSFET conductive channel potential is not uniform, because it is influenced by the charge stored in nanocrystals. In contrast with FG memories, where the presence of a high doped polysilicon floating gate assures the channel potential uniformity, in NCM each electron stored in a nanodot influences only the electrostatic potential of the neighboring channel region. This fact results in a non-uniform channel potential: when enhancing the gate voltage, the substrate inversion occurs first in those regions far from negative charged nanocrystals, as will be discussed later in this chapter. The conduction through the channel of the cell is then not uniform, and takes place only in a small part of the gate area. Only when the gate voltage is high enough, the inversion layer is formed everywhere under the gate, and electrons flow trough the gate area. The result of this fact is that the transistor exhibits a slow "turn-on" with increased subthreshold swing. When nanocrystals are neutral, the potential in the channel is more uniform then in the P or E state, because it is not influenced by the nanocrystal stored charge, and electrons start to flow underneath the entire gate area, resulting in a faster "turn-on" of the transistor and then in a low subthreshold slope. Hence, slow and fast turn-on are connected to the charge state of nanocrystals.

From Fig. 6, we see that after a high dose irradiation (higher than 10 Mrad(SiO_2)), any charge previously stored in nanocrystals has been completely neutralized. Hence, the irradiated cells show a fast turn-on. After a P or E operation, nanocrystals are charged again producing a slow turn-on, thus explaining the constant difference of 30 mV/decade observed in the subthreshold swing before and after a P operation (Fig. 8 A) in irradiated devices.

After low dose irradiation (such as 1 Mrad(SiO2)), the charge stored in nanocrystals is only partially neutralized and then we measure only a slight difference in the subthreshold swing before and after a P operation (Fig. 8 B).

3.1.5 Data retention

To study data retention capabilities of irradiated devices some experiments have been performed leaving the devices unbiased at room temperature for long times and periodically measuring them. The NCM cells were one half in the P and one half in the E state. Fig. 9 shows the V_T variation after 8-day storage as a function of proton fluence. The programmed threshold voltage drops by 100 mV in fresh devices and in devices irradiated at the low fluences (up to $5.7 \cdot 10^{11}$ protons/cm^2), while it approaches -460 mV after the largest fluence ($5.7 \cdot 10^{14}$ protons/cm^2). Smaller variations are observed for the E state, ranging from 30 mV in unirradiated devices to 260 mV in devices irradiated with the highest fluence. Fig. 10 shows the V_T time variations.

The E V_T shows smaller variations with respect to the P V_T also over a long time (i.e. 50 days), as illustrated in Fig. 10. This demonstrates that the most critical state for retention is the programmed one, where electrons stored in the nanocrystals can tunnel out toward the substrate across the 3.1 eV high oxide potential barrier. For converse, in the erased state the positive NC charge can be neutralized in two ways: i) the stored holes may tunnel out toward the substrate; ii) the electrons from the silicon conduction band may tunnel into the nanocrystal recombining

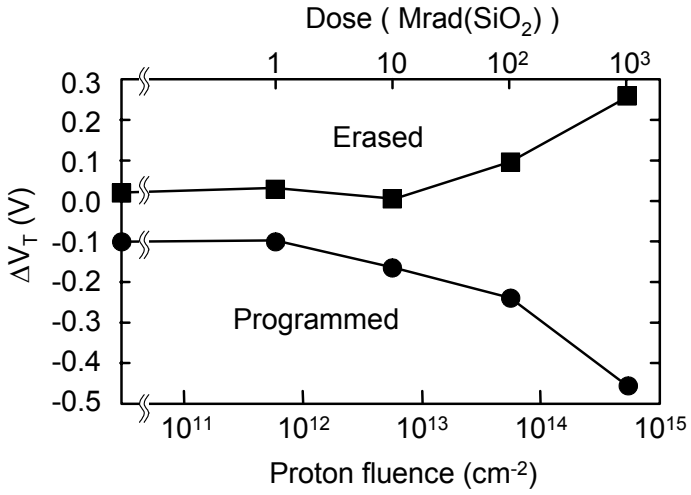


Fig. 9 Programmed and erased threshold voltage variation of CAST after 8 day device storage with all terminals floating as a function of the proton fluence.

the holes. Both these contributions are much lower than in the programmed cell. In the first case, the hole barrier height is 4.8 eV, much larger than the electron barrier in the conduction band. In the second case, at $V_{GS} = 0$, the substrate is depleted and the electron population is very low, hence there are very few electrons which may tunnel into the nanocrystals.

Devices irradiated with $5.7 \cdot 10^{11}$ protons/cm^2 and the unirradiated devices show very similar V_T variations, even after 50 days. In Fig. 11 we have fitted the measured P V_T time variation to extrapolate the V_T variation after 10 years, i.e., one of the most important requirement for nonvolatile memories. The experimental data empirically fit the relation:

$$\Delta V_{th}(T) = A(\phi) \cdot T^{0.2} \qquad (1)$$

where T is the time, ϕ is the proton fluence, and $A(\phi)$ is a fitting parameters dependent on the fluence. From our extrapolation, the unirradiated devices and devices irradiated with fluences up to $5.7 \cdot 10^{11}$ protons/cm^2 are expected to feature a V_T variation of about 300 mV after 10 years. Device irradiated with $5.7 \cdot 10^{13}$ protons/cm^2 should exhibit a variation of 800 mV and devices irradiated with $5.7 \cdot 10^{14}$ protons/cm^2 should loose all the stored charge before 10 years.

Hence, proton irradiation can significantly affect the data retention property of NCM only for fluences exceeding $5.7 \cdot 10^{11}$ protons/cm^2. In fact, an oxide defect may discharge through RILC only one or few nearest-neighboring NC's. Most of the storage nodes may be discharged only when the oxide trap density becomes comparable with NC density, i.e., at high fluences. Noticeably, we estimated that the number of protons passed in the tunnel oxide underneath the area covered by nanocrystals is about 50 for a fluence of $5.7 \cdot 10^{11}$ protons/cm^2, i.e., only 16% of nanocrystals are hit by a proton, and about 500 for a fluence of $5.7 \cdot 10^{12}$ protons/cm^2, i.e., every nanocrystal is hit by 1.6 protons on average. Hence, considering that only when the fluence is $5.7 \cdot 10^{12}$ protons/cm^2 or higher there is a degradation of the NCM retention capability, only when the impinging protons produce defects within the tunnel oxide underneath most of the nanocrystals in the cell the retention time of the cell is reduced.

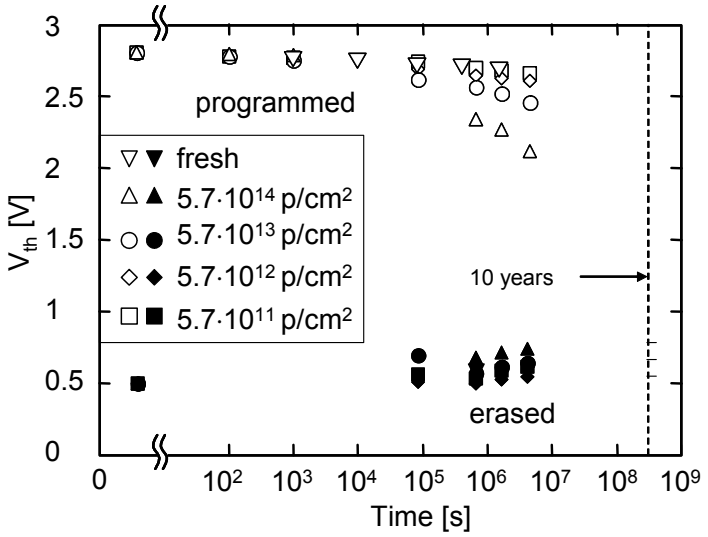


Fig. 10 Threshold voltage of both unirradiated and irradiated CASTs during long time data retention experiment. Closed symbols represent the erased thresholds and open symbols represent programmed thresholds.

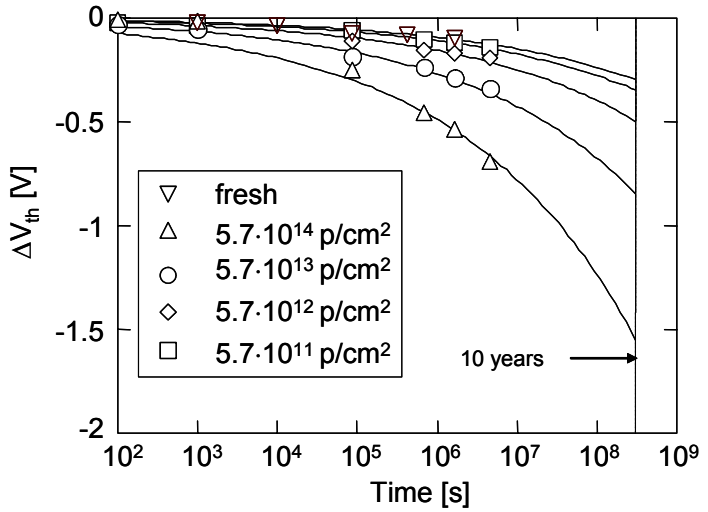


Fig. 11 Threshold voltage variation of programmed CAST as a function of the time. The lines represent the empirical fit by Eq. (1).

The V_T variations observed in the unirradiated devices may be attributed to the direct tunneling of electrons from nanocrystals to the substrate through the tunnel oxide barrier, or to a trap assisted tunneling across preexisting traps/interface defects (i.e., deriving from the fabrication process). Nevertheless, we can reasonably assume that in a 5 nm oxide the trap assisted tunneling across process-induced traps is negligible [Nic99].

The lateral tunneling [Com04], i.e., the tunneling of electrons from a nanocrystal at high potential to another one at lower potential, cannot significantly contribute to the degradation of the data retention capability of this NCM device. The lateral tunnel effect can be a real issue in NCM: when nanodots can exchange electrons, a single leaky spot in the tunnel oxide may discharge a large part of them. Generally the lateral tunneling is observed in devices fabricated with processes such as low energy silicon implantation, which has poor control of the NC size

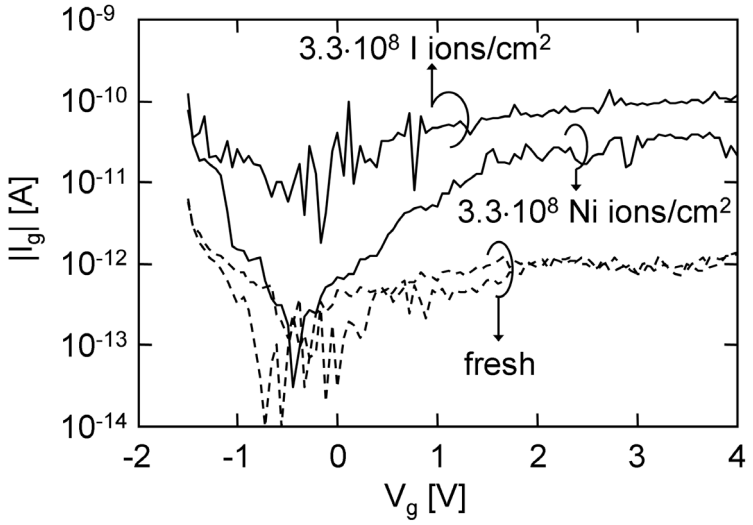


Fig. 12 Gate leakage current measured before and after I and Ni irradiation with an ion fluence of $3.3 \cdot 10^8$ ions/cm^2 in two CAST.

and distribution. Still, in our devices, which are processed by LPCVD, the NC density has a value such that the mean distance between two nanodots is higher than the tunnel oxide thickness, so that the tunneling probability of one electron between two adjacent NCs is much lower than the tunneling probability from a nanocrystal to the substrate.

3.2 Single Event Effects

3.2.1 Irradiation Experiments

All irradiations were performed at the SIRAD facility of the Tandem Van Der Graaf accelerator at the INFN Legnaro National Laboratories, Italy [Wys01]. The samples were irradiated with I ions (301 MeV, LET = 64 MeV·cm^2·mg^{-1}) and Ni ions (182 MeV, LET = 31.3 MeV·cm^2·mg^{-1}) at wafer level. The device terminals were left floating during irradiation. For each ion we used three fluences: $0.83 \cdot 10^8$ ions/cm^2, $1.7 \cdot 10^8$ ions/cm^2, and $3.3 \cdot 10^8$ ions/cm^2, corresponding to hit cells percentage (assuming a single ion hit on a cell) of 5%, 10% and 20%, respectively, in the CAST. We irradiated 12 CAST for each ion type and fluence value. The maximum ion fluence has been chosen in order to keep small enough the percentage of double hits on the same cell. We calculated that the double hit probability is 0.12%, 0.45%, 1.6% for an ion fluence of $0.83 \cdot 10^8$ ions/cm^2, $1.7 \cdot 10^8$ ions/cm^2, and $3.3 \cdot 10^8$ ions/cm^2, respectively.

3.2.2 CAST Irradiation with I and Ni ions

Despite the large gate dielectric thickness, after irradiation an increase of the oxide leakage current has been measured, as shown in Fig 12 for two CAST arrays irradiated with $3.3 \cdot 10^8$ I ions/cm^2 and $3.3 \cdot 10^8$ Ni ions/cm^2, respectively. At $V_g = 4$ V the gate current increases from 1 pA (fresh) to 100 pA (30 pA) after I (Ni) ion irradiation. As expected, the gate current increase is larger after I ions irradiation, due to the larger LET coefficient. The large gate current enhancement derives from the formation of one or more conductive paths across the gate

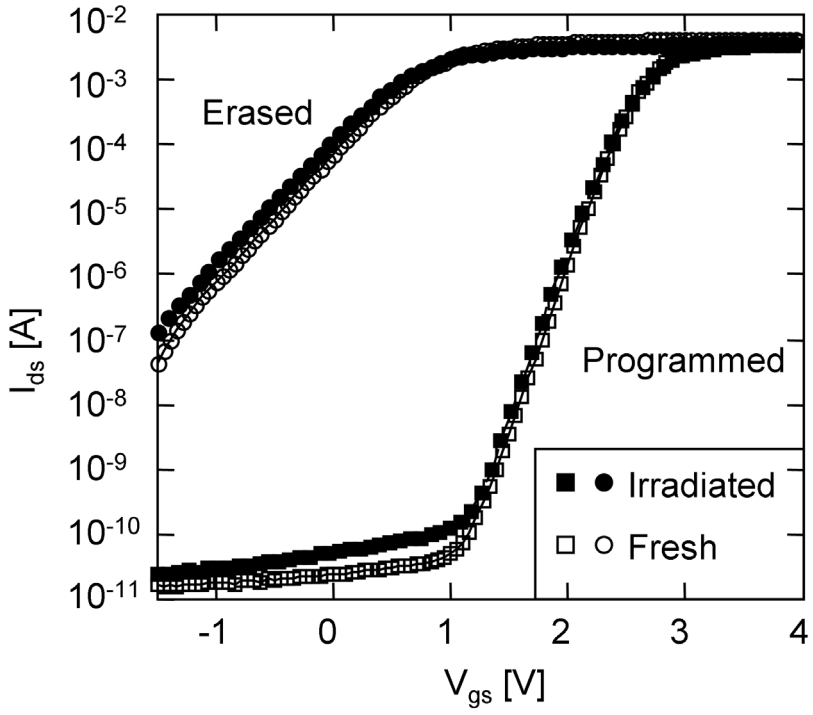


Fig. 13 I_{ds}-V_{gs} curves measured before and after irradiation with $3.3 \cdot 10^8$ I ions/cm^2.

dielectric, due to the ion hit. Moreover, we observed the large leakage current increase only in some irradiated CAST. In particular, we measured this current increase in 25% of irradiated samples with the highest fluence (50000 ion hits), while only 5% of the CAST irradiated at lower fluence (25000 and 12500 ion hits) exhibited an appreciable gate current increase. This indicates that this conduction does not uniformly affect the whole gate area, but it is localized in one or few leaky spots that have a limited probability of being activated by the impinging ions.

The drain current in subthreshold region is shown in Fig. 13 for both P and E states before and immediately after irradiation. Noticeably, irradiation induces negligible changes in the CAST drain current, without affecting the subthreshold slope as well. This is in agreement with previous measurements on FG memory cells [Cel02] that showed no degradation of the cell transistor electrical characteristics after a single heavy ion hit.

When considering irradiation of non-volatile memory cells there are two main degradation mechanisms involved; the former coming from the immediate charge loss, due to a single ion strike [Cel04d], and the latter deriving from a reduction of the long-term data retention, due to the generation of tiny oxide leakage currents [Lar03].

Concerning the first mechanism, data shown in Fig. 13 indicate that no noticeable charge loss occurred in the CAST cells due to heavy ion irradiation, which consequently appears not to be a problem for this technology. Coming to the second problem, moving from a floating gate MOSFET typical of contemporary Flash memories, with a relatively thick tunnel oxide (8-10nm), to the novel nanocrystal technology, with thinner gate oxide (4-5 nm), the leakage current could become an even bigger issue, in principle. In fact, the radiation induced oxide leakage current quickly increases with reducing oxide thickness below 6 nm [Sca97], being it either Radiation Induced Leakage Current (RILC) [Cec98, Lar99], Radiation Soft Breakdown

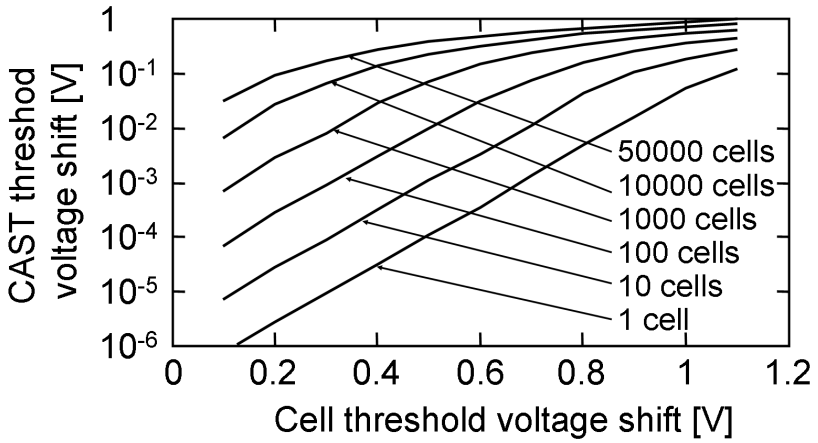
(RSB) [Cec00, Con01, Mas01], accelerated breakdown or wear-out [Ces01, Ces02, Cho02, Ces03b, Ces04].

In our devices we have reported of a 100 pA steady state leakage current after I ion irradiation (see Fig. 12). Due to the large thickness of the overall insulator between the control gate and the Si substrate (12 nm + 5 nm thick = 17 nm), this conduction can not be attributed to single trap assisted tunneling producing RILC [Lar99] which is observed in much thinner oxides (<5-6 nm) [Ces00]. Yet, previous studies [Can01] evidenced that heavy ion irradiation produces measurable DC leakage current even in 10 nm thick oxides. The origin of this leakage current is related to a multi-trap-assisted conduction through a defect cluster generated along the ion track. In our NCM devices, this conduction mechanism is seldom observed; it could be promoted, or even activated, when the ion hits the gate oxide in close proximity of a cluster of 2-3 neighboring nanocrystals, interacting with the ion-generated defects to enhance the path conductance. The generation probability of such paths is very low, around 10^{-5}–10^{-6} spot/ion, in agreement with previous studies on thin gate oxide submitted to heavy ion irradiation [Ces01, Ces02, Cho02, Ces03]. Remarkably, the weak spots responsible for the large gate current increase could be associated to the defects generated along overlapping ion tracks.

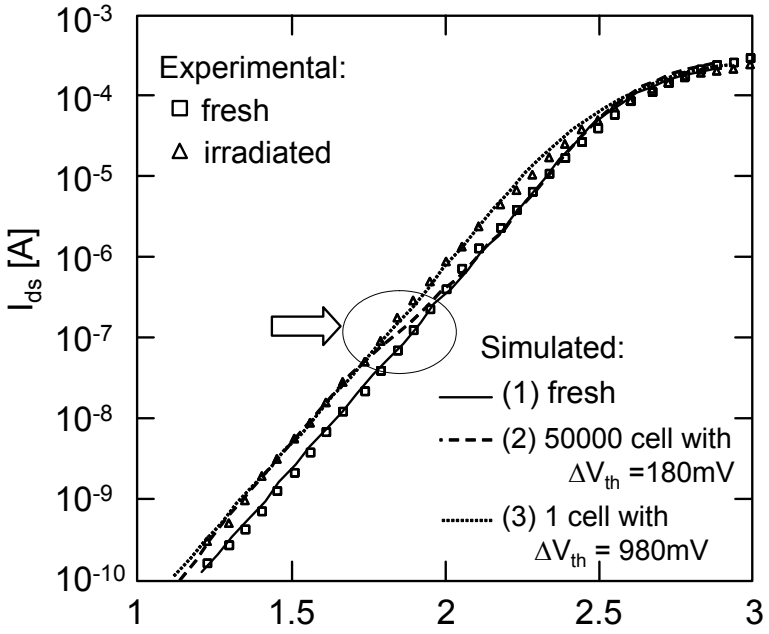
The floating gate capacitance of a memory cell is in the range of 1 fF: a 100 pA leakage current should completely discharge it in few tens of μs. For converse, in Fig. 13 we do observe no substantial differences between irradiated and fresh devices indicating that no critical charge loss occurred in the irradiated CAST cells.

The improved robustness of NCM to heavy ion irradiation derives from the discrete storage effect, limiting the transient effect of a single ion and the impact of the radiation induced leakage currents expected across the thin tunnel oxide, such as RILC and RSB. In fact, if nanocrystals are regularly arranged over the channel area and their spacing is sufficiently large (equal to or larger than the tunnel oxide thickness), an oxide trap or a cluster of defect, generated by the impinging ions and located under a storage node, should discharge only one or few nanocrystals in close proximity of the cluster of traps. Similarly, the transient conductive path due to the electron/hole pair generated during irradiation can only discharge those NCs located close enough to the ion track, with negligible impact on the threshold voltage. This confirms that the transient conductive path generated by the passing ion is limited to few nanometers in radius [Cel04d]. We remind that each cell contains approximately 300 nanocrystals, so that few discharged neighboring nanocrystals cannot produce any low-V_T path from source to drain, hence leaving practically unchanged the I_{ds}-V_{gs} curve of the ion-hit cell.

It is worth to remark that it is not easy to find a relation between the charge loss and the threshold voltage of a nanocrystal memory cell. In fact, whereas in a conventional Flash cell the charge in the floating gate is always uniformly distributed, in case of a nanocrystal cell, the charges are stored in discrete locations. When some nanocrystals have lost part of the stored electrons, the remaining stored charges do not rearrange themselves. This gives rise to a local variation of the charge density over the nanocrystal layer, consequently producing a local variation of the potential at the silicon/oxide interface. Hence the channel starts forming earlier in those regions where the nanocrystals have lost some of their electrons. This means that the effective threshold voltage shift of a nanocrystal cell is not only a function of the total charge lost, but it is also function of the position of the defective nanocrystals, i.e., those ones that have lost their charges.



(A)



(B)

Fig. 14 a) Simulated relation between the CAST threshold voltage shift and cell threshold voltage shift. Different curves refer to different number of shifting cell. b) Comparison between simulated and experimental I_{ds}-V_{gs} curves in subthreshold region in the programmed CAST.

For sake of simplicity, we have performed simulations caring of only the actual threshold voltage shift of the cell and not consider either the actual position of the defective nanocrystals, or the charge lost by the defective nanocrystal. Fig. 14a shows the relation between the CAST V_t shift and the damaged cell V_t shift. The different curves refer to different numbers of cells having lost charge. For instance, the 50 mV shift of Fig. 13 might be produced either by a 120 mV shift of 50000 cells, or by a 630 mV shift of 100 cells, or a 980 mV shift of a single cell. If the shift were produced by a single defective cell we should observe a kink in the CAST subthreshold current of Fig. 13, like that highlighted in Fig. 14b. For converse, we experimentally observed that the CAST drain current features a rigid leftward shift, which is a signature of a small charge loss in almost all the cells hit by an ion, producing a threshold voltage shift as large as 0.18 V per cell.

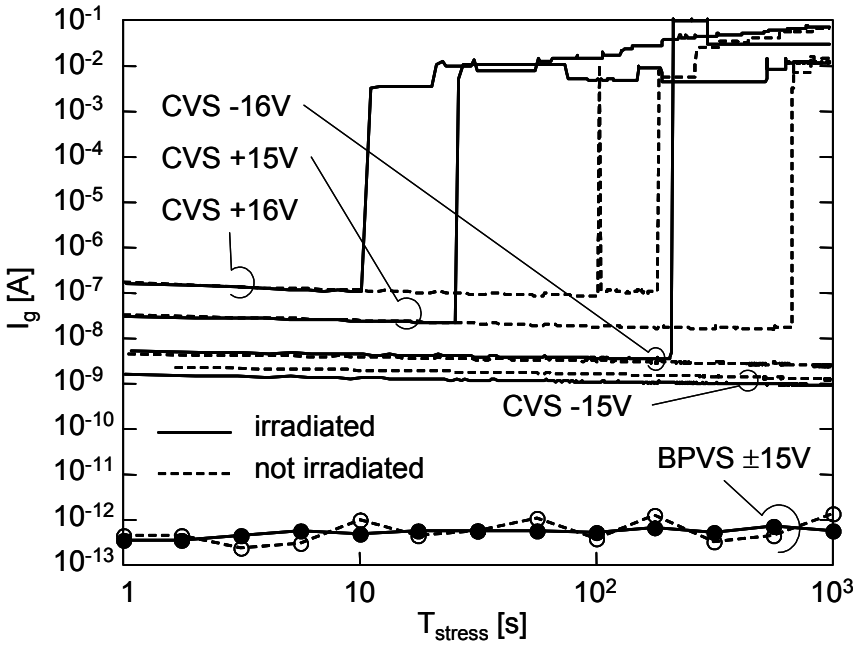


Fig. 15 Gate current during electrical stresses performed on irradiated and not irradiated devices. Different V_g polarities and modes (CVS and BPVS) are compared. For BPVS we show the I_g value read from I_g-V_g curves at V_g=4V.

3.2.3 Electrical Stresses and Irradiation

In order to assess if any latent damage is present in the tunnel or control oxide even in those samples which do not exhibit any gate leakage current after irradiation, we submitted to accelerated electrical stress both irradiated (with I ions) and not irradiated CAST, using different electrical stress techniques:

a) Constant Voltage Stress (CVS) with |Vg| = 15 V to 18 V.
b) Bipolar Pulsed Voltage Stress (BPVS) by applying square pulses to the gate between -Vg and +Vg (Vg=15 V or 16 V) and pulse frequency from 10 Hz to 100 kHz.

All stresses were carried out with grounded source, drain and substrate. Figs. 15-17 summarize the effects of electrical stresses on some fresh and irradiated devices by using the two stress methods listed above. The gate current during electrical stress is plotted in Fig. 15, showing the accelerated breakdown of irradiated oxide, at least when CVS is applied. The P/E state V_T evolution is shown in Fig. 16 for CVS and in Fig. 17 during CVS and BPVS. In both figures, irradiated and fresh devices are shown. Comparing Figs. 16 and 17 we observe no or negligible V_T variation during negative CVS, while for both fresh and irradiated devices we observe a positive shift of the threshold voltages during positive CVS. In addition, BPVS produces also the progressive thinning of the programming window. Before the breakdown irradiated and fresh devices show the same behavior during stress.

It is worth to note that negative CVS produces very small effects in terms of V_T variation, at least before breakdown. Instead, negative charge trapping is seen after the positive CVS, probably at the Si/SiO_2 interface and/or in the nitride layer [Mur03], which is prone to electron

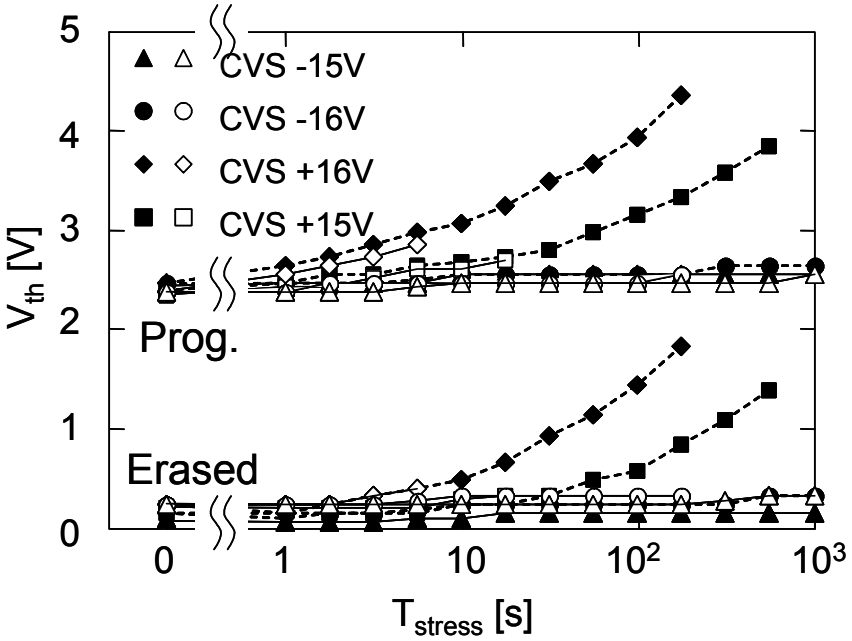


Fig. 16 Evolution of the P/E V_t during CVS with different Vg values and polarity performed on irradiated (open symbols) and not irradiated (close symbols) samples.

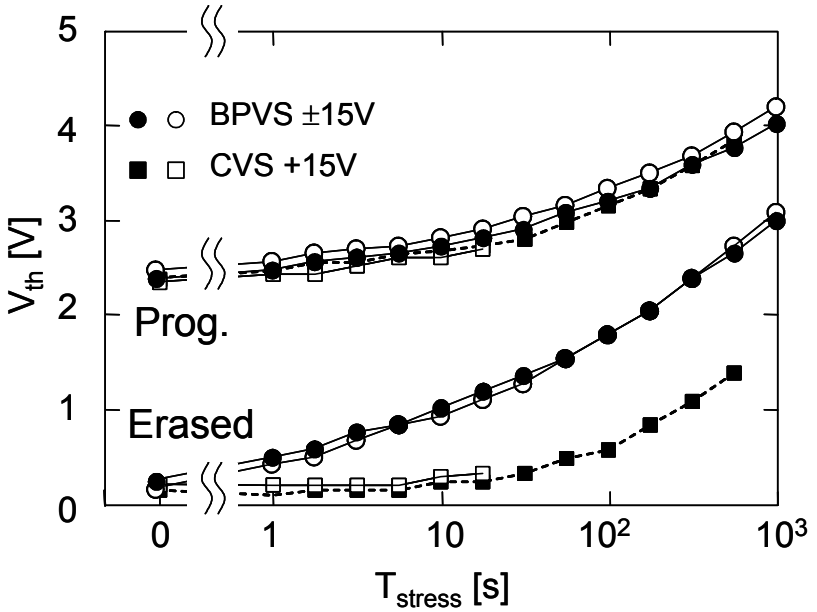


Fig. 17 Evolution of the P/E V_t during positive CVS and BPVS performed on irradiated (open symbols) and not irradiated (close symbols) samples.

trapping. The different degradation mechanisms may be ascribed to the different electron energy during injection. If the negatively charged defects were generated in the ONO layer, than more defects are generated with positive CVS, i.e., electron injection toward the gate. In this case electrons can gain much more energy than during negative CVS, when electrons are injected from the top oxide layer. Similarly, interface states can be generated by holes/hydrogen ions injected from the gate during positive CVS. It is worth to remark that negligible changes are observed between irradiated and not irradiated CAST.

A second observation comes from Fig. 17 about the difference among CVS and BPVS. Positive CVS produce a large V_T increase, without shrinking the programming window. This can be easily ascribed to the negative charge trapped in the ONO layer, as in conventional Flash cell [Mur03]. Conversely, during BPVS the programming window is strongly decreased, being the erased V_T increased during BPVS much more than the programmed V_T (see Fig. 17). Remarkably, this two stress conditions are quite different: during CVS the electric field is larger in the ONO layer, due to the charge of NC that are negatively charged with Vg > 0 V and positively charged with Vg < 0 V. During BPVS, NC are continuously charged and discharged. At each high-low transition, V_G is pulled high, while NCs are still positively charged. This reduces the average ONO electrical field, but it increases the average tunnel oxide electric field. In this condition the tunnel oxide should be more degraded than ONO.

Incidentally, from data reported in [Amm04] we estimated that program and erase time should be around 1 ms or less, with a P/E voltage of ±15 V. This means that at the pulse beginning the gate voltage mainly drops across the tunnel oxide, while at the pulse end the voltage drops across the ONO layer. Hence, we can argue that the thinning of the threshold window is ascribed to the enhanced degradation of the tunnel oxide, coming from interface state generation at NCs or Si/SiO_2 interface.

Even though immediately after heavy ion irradiation no appreciable modification of V_T appears, the acceleration of TTDB (Time To Dielectric Breakdown) indicates the presence of some defective regions, corresponding to the ion hits. These regions have negligible effects on NC-MOSFET characteristics, but they may act as seeds of further degradation, when applying the high field electrical stress. Incidentally, irradiated devices lifetime reduction is seen after CVS, i.e., when ONO is subjected to the higher oxide field. On the contrary irradiation is unable to produce accelerated breakdown during BPVS, at least in time intervals as long as those used in this work. This peculiar behavior seems to confirm the idea that the major effects of heavy ion irradiation are in the ONO layers rather than in the tunnel oxide and, therefore, the accelerated breakdown observed after heavy ion irradiation should start from the ONO layer and later it propagates toward tunnel oxide.

3.2.4 Data retention

In order to assess the impact of the measured gate leakage currents (see Fig. 12), some retention experiments have been performed on P CAST. After programming, all the irradiated and fresh devices were stored with all terminals floating and the I_{ds}-V_{gs} curves were periodically measured over a 20 days period. The corresponding V_T values are plotted in Fig. 18. V_T keeps monotonically decreasing, by –25 mV/time decade on fresh devices and –40 mV/time decade on irradiated ones. The dependence on ion source and fluence is very small. Being the experimental data affected by uncertainty, it is not possible to identify a clear and consolidate trend.

Fig. 19 shows the I_{ds}-V_{gs} curves of irradiated CAST taken immediately, 9 days and 20 days after programming. The subthreshold slope does not change during this charge retention experiment. This means that no cells among the array has lost a critical amount of stored charge, i.e., large enough to produce a threshold voltage shift in the cell, much larger than the average shift of the whole CAST, which is in the 100 mV range.

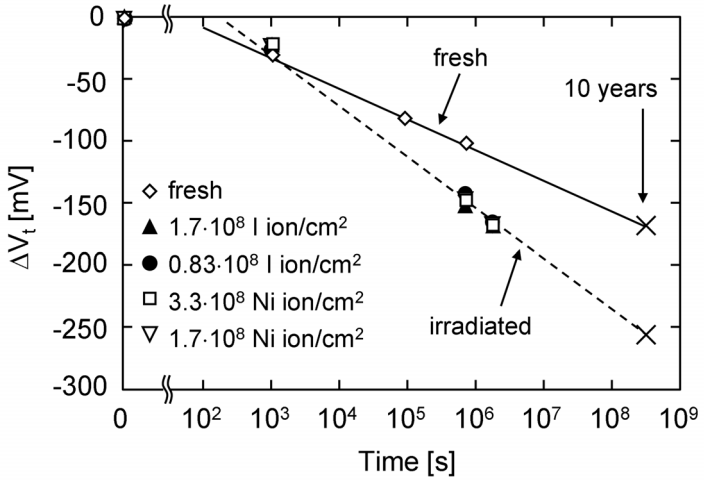


Fig. 18 Retention characteristics of fresh and irradiated CAST in the programmed state.

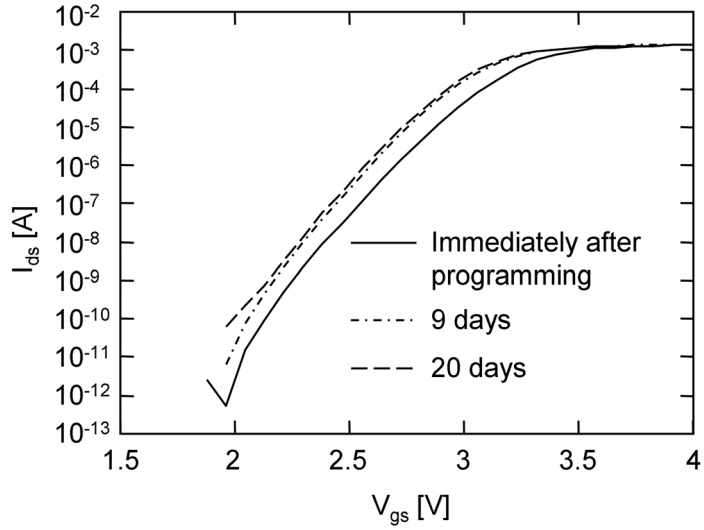


Fig. 19 I_{ds}-V_{gs} curves in subthreshold region measured immediately after programming, 9 days after programming and 20 days after programming in a CAST irradiated with $3.3 \cdot 10^8$ ions/cm^2

The threshold voltage shift of Fig. 18 is due to the charge lost from nanocrystals, due to the fresh tunneling current and/or the gate excess current due to the weak spots generated by irradiation (see Fig. 12). In a fresh device the threshold voltage decreases with -25 mV/time decade, starting from the value read at namely 1000 s. This means that in time as long as 10 years ($3 \cdot 10^8$ s) the threshold voltage should shift by –140 mV (corresponding to 0.5 electrons lost for each nanocrystal on average).

Irradiated devices loose charge from nanocrystals at a faster rate (–40 mV/dec); comparing irradiated devices to each other we cannot identify any clear trend as a function on ion type or ion fluence. This fact is only apparent and it is one of the main experimental limits of the CAST structure. We must take into account that the threshold voltage has been estimated by the shift of the drain current measured in subthreshold region, at a fixed current. In the programmed state, the threshold voltage shift is dominated by the first cells turning-on. This means that in an

irradiated CAST the weaker cells are the major responsible for the threshold voltage shift. We can argue that these cells might be the most damaged, e.g., those ones receiving a double ion hit or those cells, which experience the largest increase of the gate leakage (see Fig. 12). Random fluctuations on threshold voltage occurring even between two consecutive measurements of the same CAST or the same single cell (as large as 2-3 mV) add to the small variation observed, making even more difficult to extrapolate the actual trend.

Nonetheless, it is worth to remark again that the I_{ds}-V_{gs} curves of Fig. 19, taken immediately after programming, after 9 days, and after 20 days keep parallel to each other in the subthreshold region, showing only a rigid shift toward negative voltages, due to the discharge of some nanocrystals. Again the rigid shift of the CAST characteristics is a clear signature that the majority of the hit cells are shifting leftward. From the simulation we calculated that if the number of damaged cells is in the order of 50000, the actual threshold voltage variation of each cell should be 350 mV. The absence of the kink in the CAST characteristics, confirms that no cell has lost all its charge.

In principle if an ion hit affects one nanocrystal at most, we do not expect to observe any appreciable change in the retention time characteristics, against the experimental evidence. Hence, it must be present some other damage mechanism that can affect also those regions of the cell, which are not directly hit. In fact, a single ion generates a dense electron/hole track with small radius. Holes surviving recombination diffuse and eventually generate oxide defects in a much wider region. In a previous work [Ces04] the size of this Physically Damaged Region (PDR), was reported to range from 0.2 μm to 1 μm, i.e., as large as (or larger than) the single cell size. At this point some considerations are worth about the discharge rate of the nanocrystals mediated by defects in the tunnel oxide. If one defect is generated below a nanocrystal in the middle of the tunnel oxide (namely at 2.5 nm from both interfaces), we may expect a fast NC discharge (occurring in seconds or less). Instead, if a trap is generated near the NC interface or in between two NC's, it behaves as border trap [Fle92] being 4-5 nm far from the substrate/oxide interface. Such trap may quickly capture electrons from the nanocrystals only if they lie close to them. However, they always exchange electrons with the substrate over times as long as several hours [Old96]. If we were dealing with a floating gate cell, each trap generated by irradiation in the middle of the tunnel oxide should contribute to discharge the monolithic floating gate, regardless its position over the gate area. For converse, in a NCM cell, the overall nanocrystal area is only 15% of the total gate area and only a small percentage of the traps generated by the impinging ion should be close enough to a nanocrystal, to be effective in discharging its stored charge. This qualitatively explains why the discharge rate of the irradiated devices is less than twice that of the fresh cells.

4. Peculiar Characteristic of NCM cells

4.1 Experimental and Devices

For this study, cells with different size have been analyzed, with W raging from 0.16 μm to 0.24 μm and L raging from 0.24 μm to 0.34 μm, with the same structure reported in Fig. 3.

For comparison, also FG Flash memory cells with almost the same structure reported in Fig. 3 have been analyzed. The Flash cells have a FG instead of the nanocrystal layer and they have a thicker tunnel oxide (~10 nm). Still, the other technological parameters (dimensions, doping profile, etc.) are identical.

For both NCM cells and FG Flash cells, the Programming (P) and the Erasing (E) operations were carried out by Fowler-Nordheim (FN) injection, applying a bias $V_G = +V_{G\text{-}PROG}$ and $V_G = -V_{G\text{-}PROG}$, respectively, to the gate for 2 ms with all the other terminals grounded, where $V_{G\text{-}PROG}$ is the programming voltage and it is equal to 15 V, where not differently specified. During the P operation, electrons of the channel are injected into the NCs (or FG) and the V_T of the cell increases; during the E operation, holes are trapped into NCs and the cell V_T decreases. We use FN injection instead of Channel Hot Electron Injection for the programming because in this way all the NCs are uniformly charged.

4.2 Experimental Results

Fig. 20 A and B show the I_D-V_G characteristics of a NCM cell (W = 0.16 μm, L = 0.3 μm) after a P and an E operation in linear and logarithmic scale, respectively. We applied a constant bias V_D = 50 mV to the drain during the measurement. As depicted in Fig. 20, the cell V_T was simply extrapolated as the V_G at which a fixed I_D current is measured. We extrapolated the cell V_T in the linear region considering a threshold drain current $I_{D\text{-}LIN}$ = 10 μA (Fig. 20 A) and in the subthreshold region considering $I_{D\text{-}SUBTh} = 10^{-10}$ A (Fig. 20 B). The Programming Window (PW), i.e., the difference between the P and E V_T, is 1.27 V if extrapolated in the linear region (*Linear PW,* Fig. 20 A). Surprisingly, the PW extrapolated in the subthreshold region (*Subthreshold PW*, Fig. 20 B) is 1.68 V, and the difference between the Subthreshold PW and Linear PW (simply *the Difference* in the following) is 0.41 V.

For clarity, in Fig. 21 we show the same I_D-V_G characteristics of Fig. 20, but with the E I_D-V_G curve shifted by 1.27 V, i.e., the value of the Linear PW. The E curve perfectly overlaps the P curve for $I_D \geq 10$ μA (Fig. 21 A). For lower current values, the two curves do not overlap and the distance between them progressively increases. Observing the same plot in logarithmic scale (Fig. 21 B), we note that the P and E curves are almost parallel in subthreshold region, and the P curve is always on the right of the E curve.

FG Flash memory cells do not show the same behavior of NCM cells. We reported in Fig. 22 A and B the P and E I_D-V_G characteristics of a FG Flash cell (W = 0.16 μm, L = 0.3 μm), in linear and in logarithmic scale, respectively (V_D = 50 mV). As depicted in the figure, the FG Flash Memory cell features the same PW (2.42 V) in linear and in subthreshold region and the Difference is hence 0 V, as expected. If we shift the E I_D-V_G curve by 2.42 V, i.e., the value of the PW, the E curve perfectly overlaps the P curve in both linear and subthreshold region (not

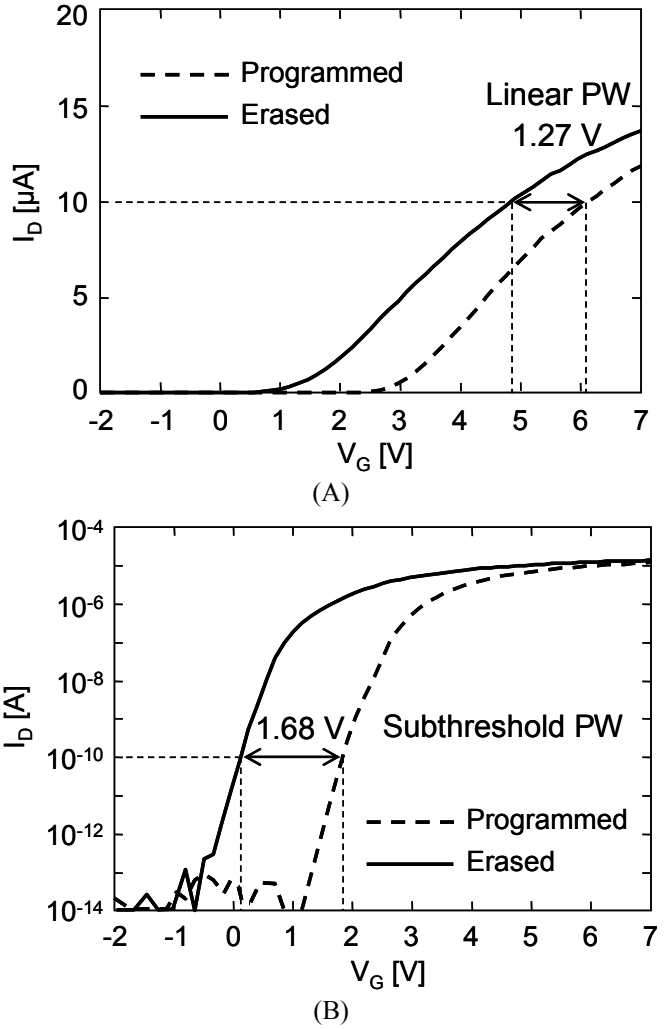


Fig. 20 I_D-V_G characteristics of a NCM cell after a programming operation (dotted line) and after an erasing operation (solid line), in linear scale (A) and in logarithmic scale (B).

shown here for brevity). This result indicates that the Difference observed in the NCM cells is a peculiar characteristic of this kind of memories.

PW and Difference do not assume the same values in all the NCM cells. In the plot of Fig. 23 we reporte the Difference as a function of the Subthreshold PW measured on 25 different NCM cells. The PWs of the cells range from –0.2 V to 1.7 V. This is due to the variation of the NCs number in the cells. In fact, cells with no/few NCs feature a small or even null PW, while cells with a large number of NCs feature larger PWs. In the plot of Fig. 23 some cells show small negative PWs: this fact is not due to a measurement error but it is due to the motion of the charge trapped into the ONO control dielectric [Gas07].

The line reported in Fig. 23 represents the minimum square linear interpolation of the experimental points. It is clear that the Difference is almost 0 for cells with small PWs (i.e., cells with no/few NCs) while it is larger in cells with large PWs. Yet, there is a large spread of the points in the region corresponding to large PWs (>1 V), where the Difference assumes values raging from 0 to 0.75 V. In particular, in Fig. 23 we evidenced four cells (indicated by the numbers) that feature a similar PW (between 1.22 V and 1.35 V) but very different

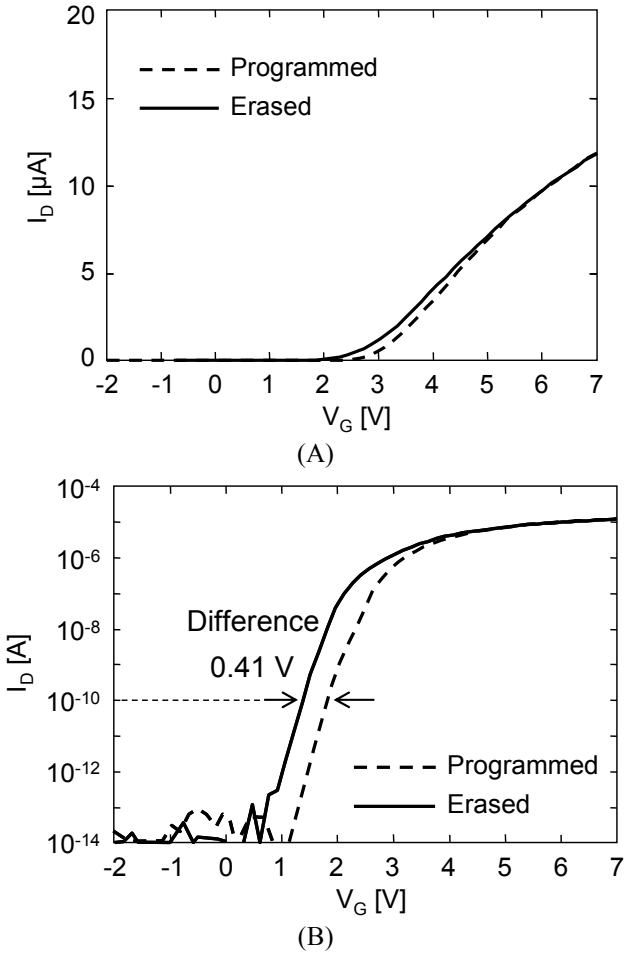


Fig. 21 I_D-V_G characteristics of a NCM cell after a programming operation (dotted line) and after an erasing operation (solid line), in linear scale (A) and in logarithmic scale (B). The Erased ID-VG is shifted by 1.27V in both the plots.

Difference values (between 0 V and 0.7 V). This result suggests that the Difference is not related only to the NCs number (and then to the PW), but also to other factors.

Fig. 24 shows the Subthreshold PW, the Linear PW and the Difference of a NCM cell (W=0.24 μm and L=0.34 μm) as a function of the $V_{G\text{-}PROG}$ used for the P and E operations. We varied $V_{G\text{-}PROG}$ between 11 V and 16 V. We chose this range of values because P/E operations are unable to modify the NCs charge for $V_{G\text{-}PROG} < 11$ V. On the other hand, P/E operations performed with $V_{G\text{-}PROG} > 16$ V stress the cell with a consequent degradation of its electrical characteristics.

By increasing $V_{G\text{-}PROG}$ the number of electrons (holes) injected into the NCs during the P (E) operation increases and this fact results in the enhancement of both Linear and Subthreshold PW. The subthreshold PW is larger than the linear PW for all the $V_{G\text{-}PROG}$ values. The Subthreshold PW ranges from 0.09 V to 1.32 V while the Linear PW ranges from 0.06 V to 0.92 V. The Difference shows the same behavior and it increases with $V_{G\text{-}PROG}$, assuming values between 0.03 V and 0.4 V. In Fig. 24 we report the linear interpolations of the experimental points corresponding to the Subthreshold PW, the Linear PW and the Difference. The linear interpolations match very well the experimental points. It is worth to note that the Difference is between 24% and 30% of the Subthreshold PW for all the $V_{G\text{-}PROG}$ values (in the following, we

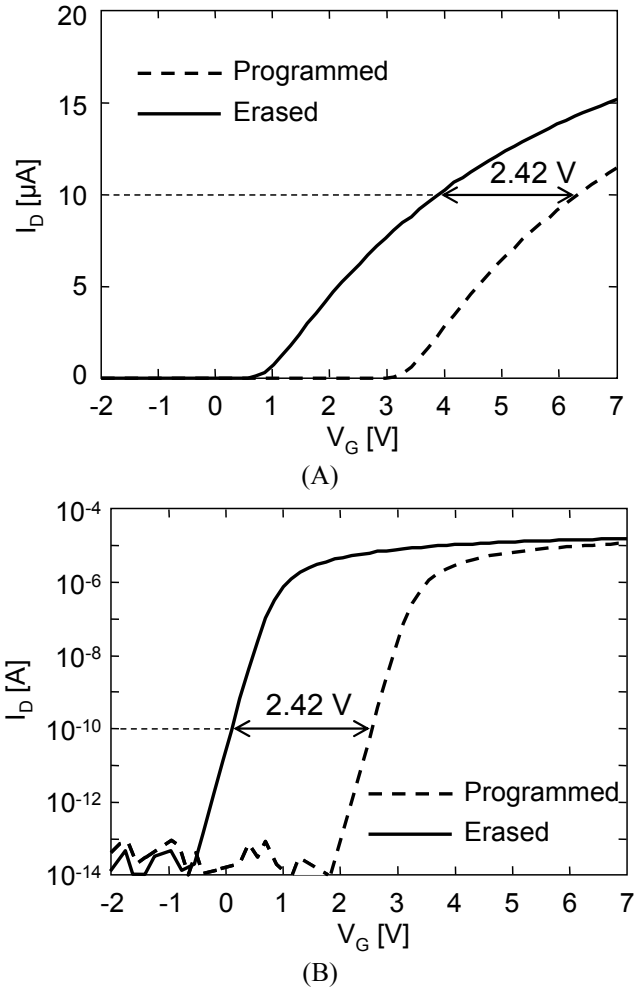


Fig. 22 I_D-V_G characteristics of a floating gate Flash memory cell after a programming operation (dotted line) and after an erasing operation (solid line), in linear scale (A) and in logarithmic scale (B).

will call *Percent Difference* the percent value of the Difference respect to the Subthreshold PW). Hence, the Percent Difference of the cell is almost independent of $V_{G\text{-}PROG}$ and then of the amount of charge stored into the NCs. Yet, the Percent Difference is strongly connected to the cell structure. In fact, resuming Fig. 23, we see that cells with almost the same Subthreshold PW feature very different Difference values, and then the Percent Differences of these cells are clearly different.

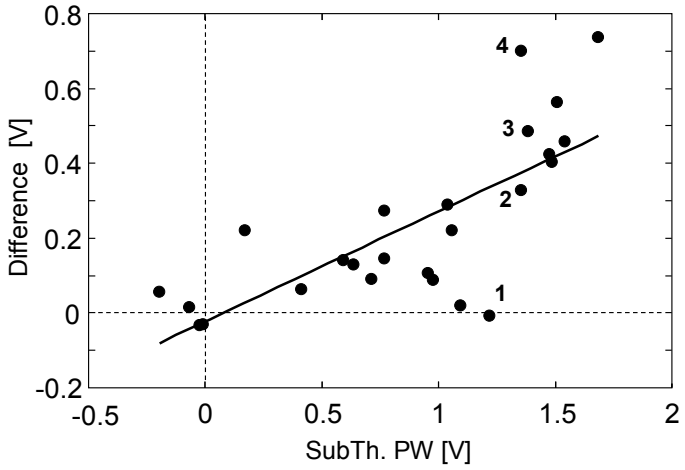


Fig. 23 Difference as a function of the Programming window measured on 25 different NCM cells. (The line is the linear fit of the experimental points).

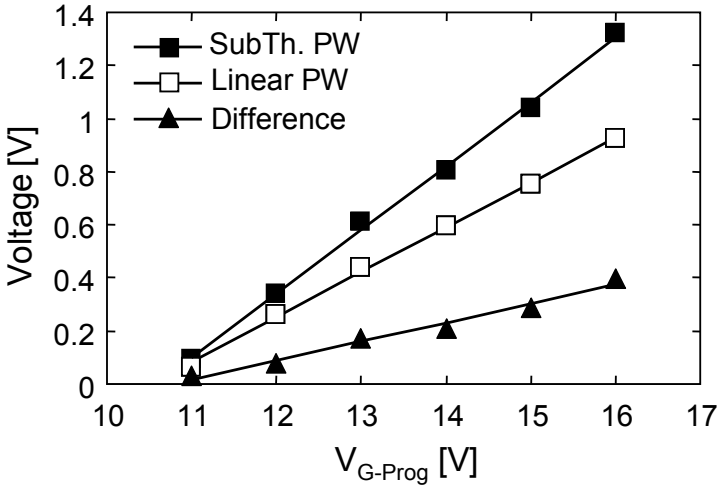


Fig. 24 Subthreshold Programming window, linear programming window and Difference as a function of the voltage used for the P/E operations in a NCM cell. (The lines represent the linear fits of the experimental points)

4.3 TCAD Simulations

4.3.1 Difference as a function of the amount of charge

We investigated the cause of the Difference observed in NCM cells by performing 2-D TCAD simulations using Taurus MEDICI by Synopsys. In Fig. 25 we show the structure of a simulated cell with nine NCs. The NCs have been modeled as square of high-doped Polysilicon with width = 5 nm and height = 5 nm and they are 30 nm apart. The tunnel oxide is 5 nm think and the control dielectric is an ONO stack with a physical thickness of 15 nm (5 nm bottom SiO_2, 5 nm Si_3N_4, 5 nm top SiO_2). The Source and Drain diffusions are identified by the white lines in Fig. 25. The channel length is 300 nm.

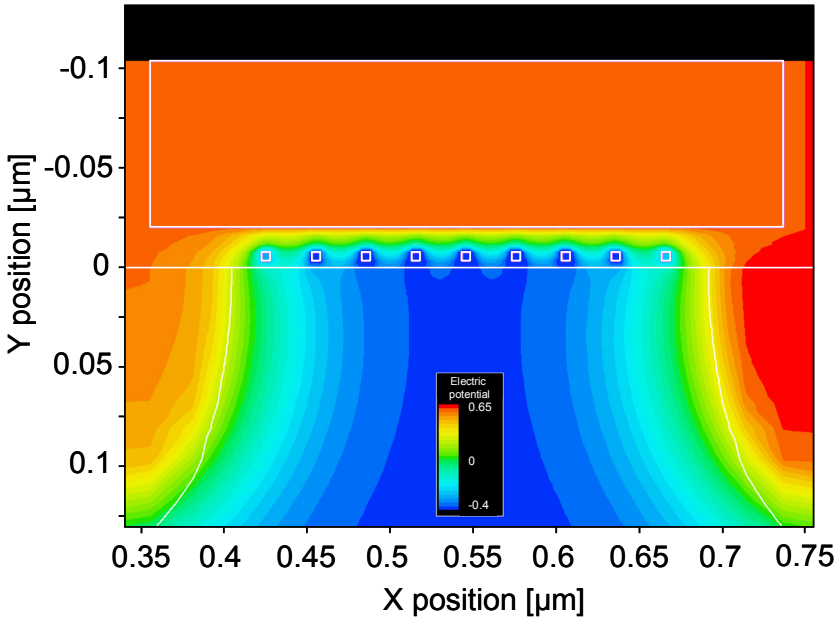


Fig. 25 Structure of a simulated NCM cell with 9 nanocrystals. The color represents the potential.

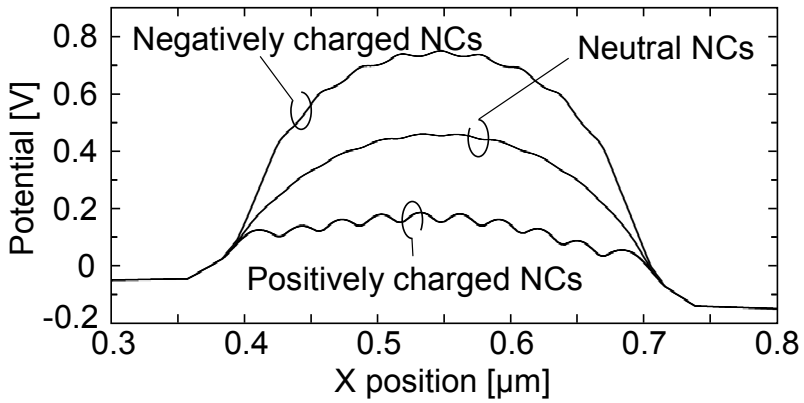
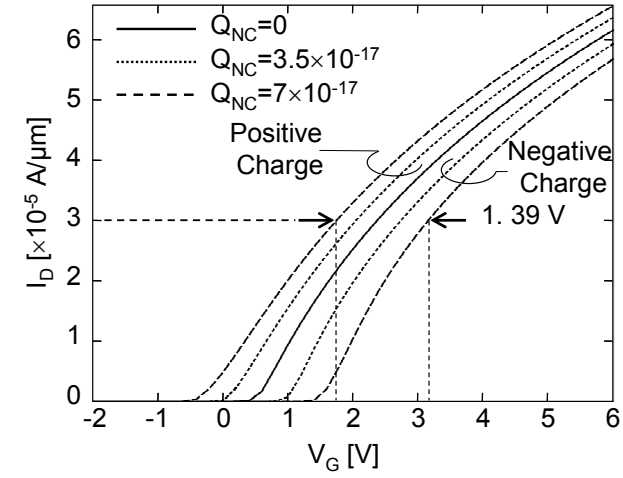


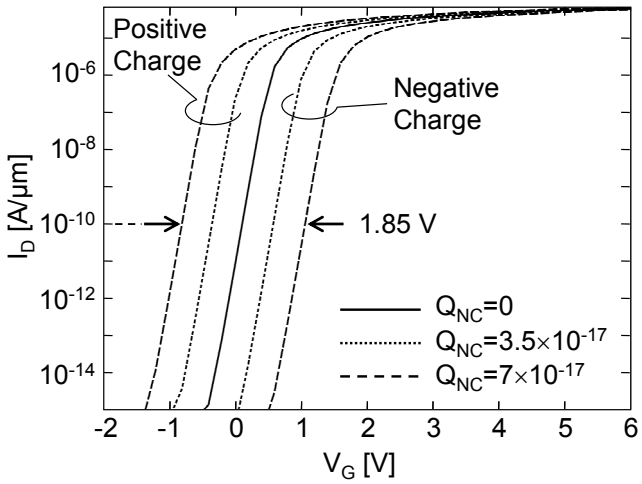
Fig. 26 Channel conduction band potential calculated with different amount of charge into the nanocrystals (V_G=0 V).

In Fig. 25 we represented also the electric potential calculated applying $V_G=V_S=V_{Bulk}=0$ V and V_D = 0.1 V and considering a fixed charge density $Q_{NC} \approx 3.5\times10^{-17}$ C/µm into each of the nine nanocrystals. We chose this charge value to simulate the effect of a single electron into each of the NCs. In fact, approximating the NCs as a cube with dimensions 5 nm×5 nm×5 nm in 3-D, the charge of a NC is $Q_{NC}\times0.005 \approx 1.7\times10^{-19}$ C, almost corresponding to the charge of a single electron.

Fig. 26 shows the conduction band potential measured in the channel 1 nm under the tunnel oxide with V_G=0 V for three different charge states of the NCs: neutral (Q_{NC} = 0 C/µm), negatively charged ($Q_{NC} \approx -3.5\times10^{-17}$ C/µm) and positively charged ($Q_{NC} \approx +3.5\times10^{-17}$ C/µm, corresponding to one hole into each NC). The conduction band potential is clearly influenced by the charge stored into the NCs. In particular, the potential increases when NCs store negative charge. Hence, the potential barrier that electrons of the Source have to pass to reach the Drain



(A)



(B)

Fig. 27 Simulated ID-VG characteristics of a NCM cell with 9 nanocrystals in linear (A) and logarithmic scale (B). The different lines correspond to different amount of charge into the nanocrystals.

is higher than in the case of neutral NCs. Conversely, when NCs store positive charge the potential barrier is reduced.

In Fig. 26 we observe that NCs produce also a localized variation on the potential profile. In fact, besides modifying the mean height of the potential barrier, the NCs charge has a local effect that produces an "undulate" potential profile. Considering for instance the potential profile calculated with NCs positively charged, we note nine drops of the potential in correspondence of the nine NCs. The same is true when NCs are negatively charged, but in this case the potential increases in correspondence of each NC, as expected.

Figs. 27 A and B show the simulated I_D-V_G characteristics of a cell with 9 NCs, in linear and logarithmic scale, respectively, with V_D = 0.1 V. The solid line represents the I_D-V_G characteristic with Q_{NC} = 0 C/μm (called neutral I_D-V_G). To simulate the I_D-V_G characteristic of the cell in the P and in the E state, we put a charge Q_{NC} = -Q_{PROG} and Q_{NC} = +Q_{PROG}, respectively, into each NC. In all the simulations, we consider the same amount of charge into each NCs to simulate the real case; in fact, the FN programming assures that all the NCs store about the same amount of charge. The four dotted curves of Fig. 27 represent the P and E I_D-V_G

characteristics obtained considering two values of Q_{PROG}: $Q_{PROG} = 3.5\times10^{-17}$ C/μm and $Q_{PROG} = 7\times10^{-17}$ C/μm. The P curves (i.e., negative Q_{NC}) are on the right of the neutral I_D-V_G, and the E curves are on the left of the neutral I_D-V_G, as expected. Moreover, the distance from an I_D-V_G and the neutral I_D-V_G increases enhancing Q_{PROG}.

As in the case of the experimental characteristics (Fig. 20), we define the Linear PW and the Subthreshold PW as the PW extrapolated at the fixed drain current $I_{D\text{-}LIN} = 3\times10^{-5}$ and $I_{D\text{-}SUBTh} = 10^{-10}$ A/μm, respectively. Noticeably, Considering the P and E I_D-V_G characteristics obtained with $Q_{PROG} = 7\times10^{-17}$ C/μm, the Linear PW is 1.39 V and the Subthreshold PW is 1.85 V, with a consequent Difference of 0.46 V. Hence, the Difference appears also in the simulations. This result excludes that the cause of the Difference could be the charging/discharging of interface traps, or the motion of charge inside the oxide or similar effects. In fact, we do not consider all these effects in the simulation and hence they cannot account for the Difference.

Moreover, the Difference is observed in the 2-D simulations and then the Difference is not connected to the 3-D structure of the NCM cells. It is important to underline this fact because some authors evidenced that the conduction in a NCM cell is not uniform [Iel04b, Com03, Gus07]. In fact, when NCs store negative charge the channel inversion close to the NCs is inhibited; vice-versa, the inversion layer is formed at lower V_G close to the NCs when they store positive charge. As a consequence the channel is not uniform and the electrons percolate from Source to Drain only through the inverted regions. Following this model, the conduction is strongly connected to the 3-D structure of the NCM cell. Yet, we observe the Difference in 2-D simulated cells where the percolation is not present. Hence, the cause of the Difference is not related to the percolation of electrons or to other effects due to the 3-D structure of the cell.

Other authors reported different values of the PW in subthreshold and in linear region in NCM [Mol04, Fio05]. Yet, they analyzed NCM cells built with Silicon-On-Insulator technology, with ultra low channel W (between 30 and 80 nm) and with NCs placed also on the lateral side of the channel [Mol04]. They attributed the observed difference to the effect of these NCs on the lateral side of the channel. As a consequence, when the channel width increases the difference tends to disappear. In our case, the Difference is clearly due to other causes because we used cells with no NCs on the channel lateral sides.

Fig. 28 shows the Subthreshold PW, the Linear PW and the Difference of the simulated cell of Fig. 25 as a function of Q_{PROG}. The Linear and the Subthreshold PW linearly increase with Q_{PROG}. The Difference shows the same behavior as a function of Q_{PROG}. Moreover, the Percent Difference assumes values between 26.5% and 23.5% for each charge value. There is a clear correlation between Fig. 28 and Fig. 24. In Fig. 24, we show the PWs and the Difference measured in a real cell as a function of $V_{G\text{-}PROG}$. Increasing $V_{G\text{-}PROG}$, the charge stored by the NCs, i.e., Q_{PROG}, is enhanced. Hence, both the plots of Fig. 24 and 28 shows the PWs and the Difference as a function of the charge stored into the NCs, in a real device (Fig. 24) and in a simulated device (Fig. 28). Comparing the two plots, it is clear as the simulated and in the real cell feature the same behavior.

4.3.2 Influence of the Nanocrystals width

To understand the cause of the observed Difference simulations have been performed varying the width of the NCs. We used the same cell structure described before (Fig. 25) with a fixed number of NCs (9) uniformly spaced in the oxide above the channel. The distance between the centers of two adjacent NCs is 30 nm. We kept constant the NCs height (5 nm) and

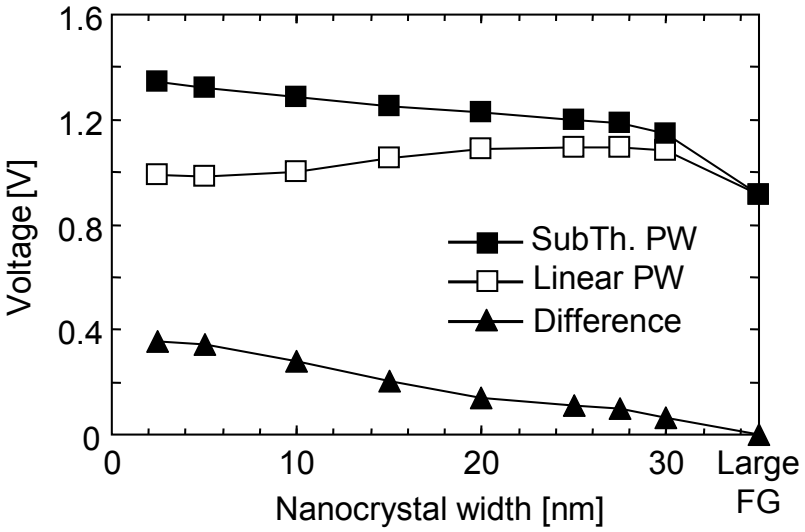


Fig. 29 Subthreshold PW, linear PW and Difference as a function of the nanocrystal width of a simulated NCM cell.

we varied the NCs width from 2.5 nm to 30 nm, maintaining the position of the NCs centers fixed. For each width value, we measured the Linear PW, the Subthreshold PW and the Difference for a fixed amount of charge stored into each NC. We set $Q_{NC} = -Q_{PROG}$ and $Q_{NC} = +Q_{PROG}$ with $Q_{PROG} = 5\times10^{-17}$ C/μm to simulate the cells in the programmed and erased state, respectively. The results are reported in Fig. 29 that shows the Linear PW, the Subthreshold PW and the Difference as a function of the NCs width. When the NCs width is 30 nm, the NCs are connected and we obtain a sort of Floating Gate. Yet, in this case, there are two channel regions between Drain and FG and between FG and Source that are not "covered" by the FG (the length of these regions is 15 nm). Hence, we decided to perform another simulation enlarging the FG by 20 nm in both directions: in this way the FG covers also a part of the Source and Drain diffusions, as in a real FG Flash Memory cell (indicated as "Large FG" in the plot of Fig. 29). In this case, we simulated the device with a fixed charge equal to $\pm9\times Q_{PROG}$ ($\pm4.5\times10^{-16}$ C/μm) inside the FG to simulate the P and E characteristic, in order to maintain almost the same charge amount, having replaced 9 NCs with a FG.

In Fig. 29 we observe that the Subthreshold PW is larger than the Linear PW for all the NCs width values. Yet, the Subthreshold PW reduces enhancing the NCs width; from the other hand, the Linear PW enhances as the NCs width increases. The abrupt reduction of both Linear and Subthreshold PW that is observed in the case of the Large FG is due to the reduction of the charge density in the oxide above the channel. In fact, as just explained, in this case we enhanced the FG length in order to cover part of the Drain and Source diffusion. However, we kept constant the amount of charge and hence the charge density is reduced, and then the PWs.

The Difference reduces as the NCs width enhances and the Difference is almost null when the NCs width is 30 nm (i.e., in the case of the FG). The Difference is null in the case of a large FG that covers the entire channel.

This result clearly indicates that the cause of the Difference observed in the real and in the simulated devices is the localization of the charge into specific regions above the channel (i.e.,

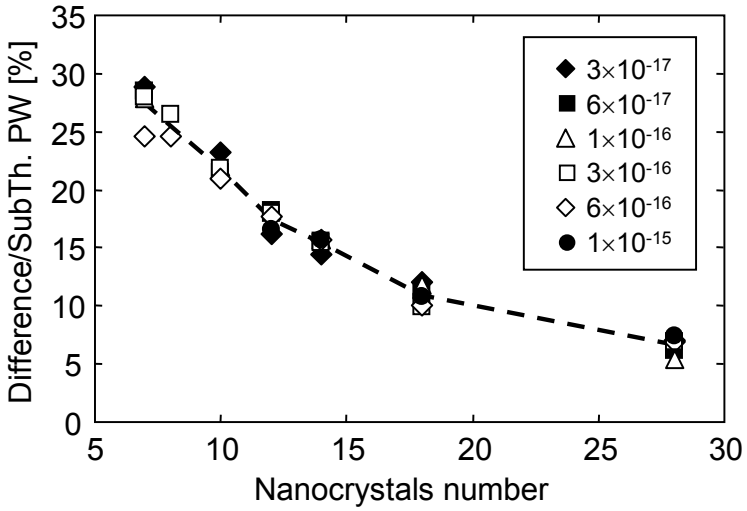


Fig. 30 Percent Difference as a function of the nanocrystals number of a simulated NCM cell. Different symbols represents different amount of charge into the nanocrystals.

the NCs). Instead when the charge is localized uniformly along all the channel length (i.e., in the case of the FG) the Difference is 0.

4.3.3 Influence of the Nanocrystals number

We investigated the correlation between the NCs density and the Difference performing 2-D simulations and varying the NCs number of the cells from 7 to 28. The NCs were uniformly spaced above the channel and we kept constant their dimensions (height = 5 nm, width = 5 nm). For each configuration we simulated the P and E I_D-V_G characteristic considering a fixed charge $-Q_{PROG}$ and $+Q_{PROG}$, respectively, into each NC. We performed simulations with different values of Q_{PROG}, raging from 3×10^{-17} to 1×10^{-15} C/μm.

Fig. 30 shows the Percent Difference as a function of the NCs number. The different symbols correspond to different Q_{PROG} values, as indicated in the legend. For clarity, we inserted in the plot the line that connects the medium values of the points obtained for different Q_{PROG} values.

First, it is important to note that the Percent Difference decreases enhancing the NCs number. This result is in agreement with the results showed in Fig. 29. In fact, the (Percent) Difference decreases when the charge is uniformly distributed along the channel. With a small number of NCs in the cell, the charge (and hence the potential in the channel) is not "uniform" and the Difference assumes large values. With a large NCs number, the charge (and the channel potential) is more uniform and the Difference is low. Finally, in the case of a FG, the charge is perfectly uniform over the channel and the (Percent) Difference is null. Hence the Percent Difference is strongly dependent on the structure of the cell (in particular, on the NCs number).

Observing Fig. 30 we note also that the Percent Difference is almost constant for different Q_{PROG} values. The points obtained simulating cells with a large NCs number with different Q_{PROG} are almost overlapped and we observe only a small spread in the points corresponding to a low NCs number. This result agrees with experimental data of Fig. 24, where we observe that the Percent Difference is almost constant varying $V_{G\text{-}PROG}$.

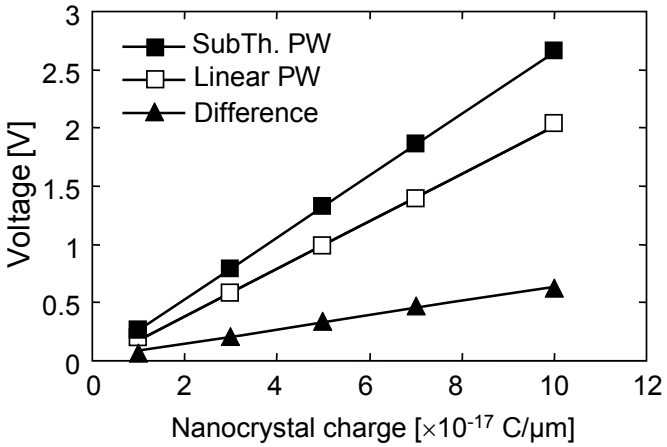


Fig. 28 Subthreshold PW, linear PW and Difference as a function of the nanocrystal charge of a simulated NCM cell (the lines represent the linear fits of the data).

4.3.4 Influence of the Nanocrystals position

Fig. 23 shows that there are cells with almost the same PW that feature very different Difference values and there are cells with a large PW (>1 V) that feature a null Difference (see cell 1 in Fig. 23). These results indicate that the Difference is influenced not only by the NCs number.

To understand if the NCs position could influence the Difference, we performed simulations considering a NCM cell with 4 NCs 30 nm apart, and placed in the oxide above the central part of the channel, near the Source diffusion and near the Drain diffusion. For each of the three configurations we simulated the I_D-V_G curve (V_D = 0.1 V) and we measured the PW and the Difference, for different Q_{PROG} values. The results are reported in Fig. 31 A and B, where we show the Linear PW and the Percent Difference, respectively as a function of Q_{PROG}.

In each one of the three configurations, the Linear PW linearly increases with Q_{PROG}. The largest PW is obtained when NCs are placed above the central region of the channel and a lower Linear PW when NCs are near the Source or the Drain diffusion (Fig. 31 A). The Percent Difference is strongly influenced by the NCs position (Fig. 31 B). The highest Percent Difference (between 40 and 50%) is obtained when NCs are in the central part of the channel. When NCs are near the Source diffusion the Percent Difference is between 17% and 22%. Finally, the lowest Percent Difference (between -2 and 12%) is obtained when NCs are near the Drain diffusion.

We can explain this result considering the potential profile of the channel for different NCs charge state (Fig. 26). The potential is higher in the central part of the channel and for this reason we obtained a larger PW and a larger Percent Difference when NCs are placed in the central part of the channel, where they have a strong influence on the channel potential profile. Conversely, when NCs are placed near the Drain or the Source diffusion they exert a lower effect on the channel potential profile with a consequent reduced PW and Percent Difference.

The Percent Difference is lower when NCs are near the Drain respect when they are localized near Source. This fact could be the influence of the Drain potential on the NCs. The

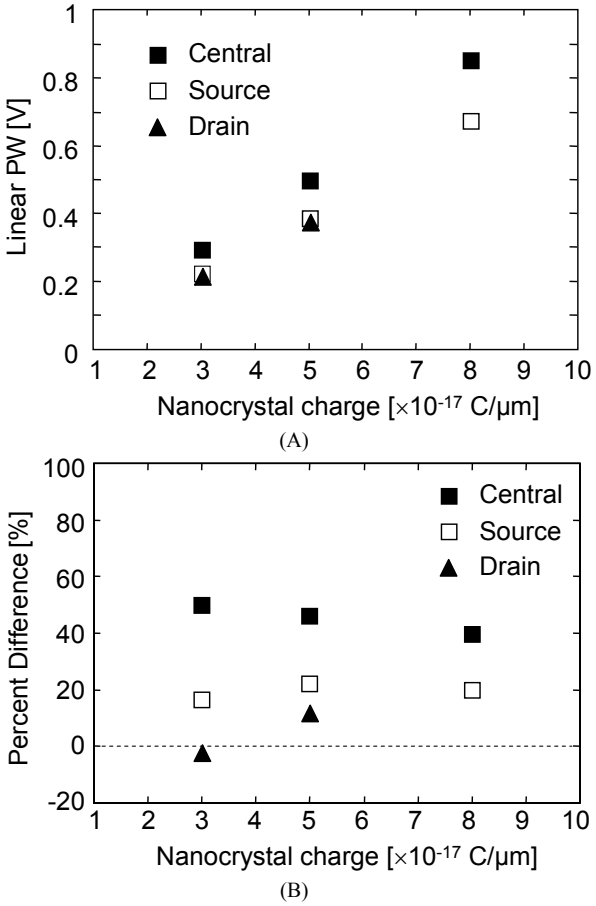


Fig. 31 Linear PW (a) and Percent Difference (B) of a simulated NCM cell with four nanocrystals, as a function of the Nanocrystals charge. Different symbols refer to different nanocrystals locations (in the central region of the channel, near source or near drain).

drain potential reduces the NCs potential limiting their effect on the channel potential with a consequent reduction of the Percent Difference.

Chapter 4

Phase Change Memories

1. Introduction

Phase Change Memories (PCM) [Pir03] seem to be one of the most promising candidates to replace FG Flash memories. PCM employ a chalcogenide material, such as the $Ge_2Sb_2Te_5$ alloy (GST), to store the information. GST can reversibly change its microstructural phase between amorphous and polycrystalline when properly heated and cooled. In the amorphous phase, GST features a high resistance while the polycrystalline state is characterized by a low resistance value. Hence, by measuring the GST resistance it is possible to recover the stored information. Several works demonstrate that PCM feature high cycling capability, good retention characteristics and large scaling potential [Pir03, Bez06, Pir04].

Since in PCM data are represented by a structural phase rather than by an electrical charge, these devices are supposed to be tolerant to ionizing radiation effects. Few works [Ber00, Mai00, Mai04] have addressed radiation effects on PCM. In [Mai00], the authors investigated both Total Ionizing Dose (TID) effects and Single Event Effects on a 64kbit PCM array integrated with radiation-hardened CMOS technology. Their results indicate a high resistance of PCM against ionizing radiation and they evidence in the CMOS circuitry the most sensitive part of these devices. Nevertheless, they used rad-hard CMOS technology and no work has investigated radiation effects on PCM integrated with non rad-hard technology.

2. Experimental Devices

4Mbit PCM test-chips produced by STMicroelectronics (Agrate, Italy) have been used for the radiation experiments [Bed04, Bed04b, Bed05]. Fig. 1 shows the schematic of the basic storage element, composed by the heater and the GST. The GST ($Ge_2Sb_2Te_5$) is heated by Joule effect forcing a current flow through it [Pel04]. To switch the structural phase state of the material from amorphous into crystalline (SET operation) the GST is heated at a temperature between 200°C and 500°C [Iel05, Lac04, Bed05b]. This range of temperatures is not enough to melt GST, and the alloy tends to become polycrystalline (SET state). In this state GST is characterized by a low resistance. To switch from the crystalline to the amorphous state (RESET operation), GST must be heated at a temperature higher than the melting point (around 600°C). If the current is abruptly removed, GST is quenched in a high-disordered amorphous state (i.e. high resistance). The length of the SET and RESET operations is in the order of one hundred nanoseconds.

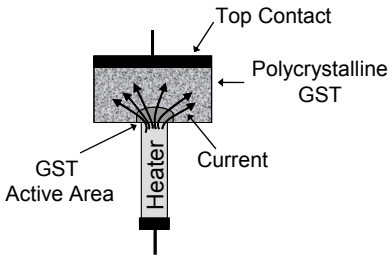


Fig. 1 Schematic representation of the PCM storage element.

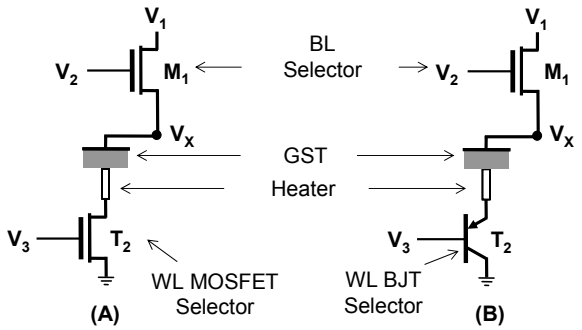


Fig. 2 Schematic of PCM cells with MOSFET WL-selector (A) and with BJT WL-selector (B).

It is worth to underline that only a small portion of the GST is involved in the phase change. As depicted in Fig. 1, when the current flows through the storage element, the current density needed to heat GST above the melting temperature is reached only in the region near the heater contact (called active area) and then only this part of GST changes its phase, whereas the remaining GST is always in the polycrystalline state [Itr04, Iel04]. The interface between GST and heater has an area of ~2000 nm^2.

To read the stored information, the current that flows through the GST is measured. The circuit used for the reading operation is schematically represented in Fig. 2 [Bed04, Bed05]: M_1 is the bit-line (BL) selector nMOS and M_2 is the word-line (WL) selector. Chips with different WL selectors, that is, MOSFET and BJT (Fig. 2A and 2B) have been used. The size of chips with BJT selectors (BJT-chips) is 8 Mbit, while those with MOSFET selectors (MOS-chips) are 4 Mbit. During the reading operation in a MOS-chip, V_1 and V_3 are high (>3 V) and V_2 is set at 0.9 V, assuring that the current flowing through a RESET cell is enough to be sensed by the external circuitry. Moreover, with $V_2 = 0.9$ V the maximum current flowing through a SET cell is about 100 μA. This current is sensibly lower than the current needed to change the GST phase, at least in the time range of the reading operation. Hence, the reading operations do not modify the state of the cell.

Fig. 3 shows the organization of the cell array in the test-chip. Each BL is connected to 2048 GST elements and each WL is connected to the gate of 2048 WL-selector MOSFETs (BJT-chips have a similar organization). The chips were realized using 0.18 μm CMOS technology with Shallow Trench Isolation (STI). The oxide thickness of the MOSFETs of Fig. 2 is 7 nm and the minimum length of the transistors is 0.36 μm. A micrograph of the experimental MOS-chip is reported in Fig. 4. In this picture the large rectangular area is occupied by the cell array. The physical dimension of the cell array is 2.4×4.4 mm^2. The area outside the cell array is

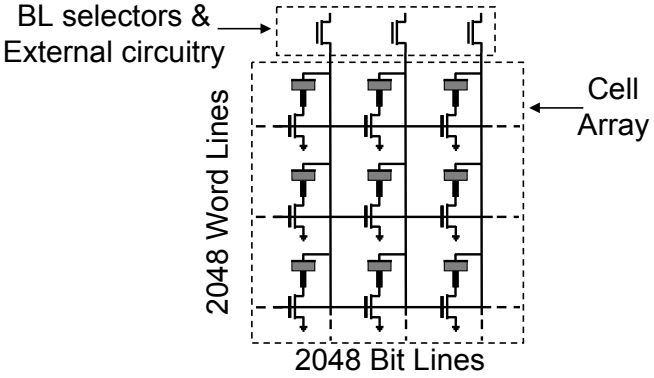


Fig. 3 Schematic representation of the cell array of a chip with MOSFET selector.

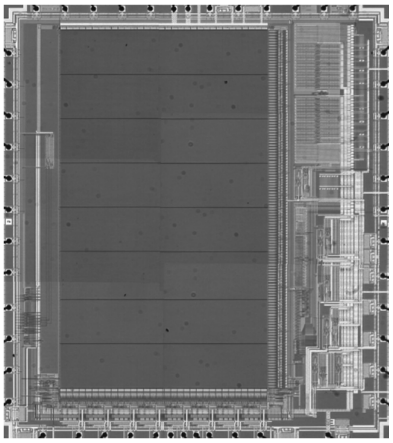


Fig. 4 Microphotograph of a PCM chip.

occupied by the BL-selector MOSFETs, the column/row decoders and the external circuitry. The sensing circuitry used for the measurements is outside the test-chip.

Fig. 5 shows the cell distribution of a fresh MOS chip as a function of the current measured in the cells. The cells were programmed one half in the RESET state and one half in the SET state. The RESET distribution (i.e., low current) is between 0 and 1.8 μA while the SET distribution (i.e., high current) features values in a larger range (between 38 and 80 μA) and for this reason the SET distribution height is lower than that of the RESET distribution in the log-log plot of Fig. 5. Different test-chips show modest differences in the distributions due to process variations.

The behavior of the SET and RESET cells after the programming operation is noticeably different. In fact, GST in the crystalline state is stable and the resistance of the SET cells is constant with time.

On the other hand, the amorphous GST is not stable. The resistance of the amorphous GST increases with time. This is a peculiar characteristic of PCM [Pir04b]. The rate of the GST resistance increase is not constant and it decreases with time after the RESET operation. Noticeably, the resistance variation is neutralized by a RESET operation and it starts again after each RESET.

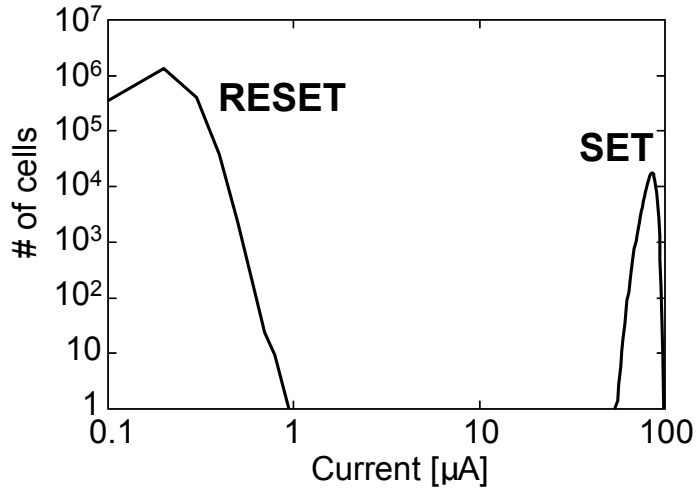


Fig. 5 RESET and SET distribution of a fresh device.

TABLE I
MEASURING SETUP USED FOR THE IRRADIATION EXPERIMENT

Step	Operation
1	Programming
2	1 month device storing
3	Reading
4	Irradiation step
5	1st Reading
6	Inverse programming of ½ of the
7	2nd Reading
8	Inverse programming of ½ of the
9	3rd Reading
10	Repeat step 4 to higher dose

3. Electron Irradiation Effects

3.1 Irradiation Experiments

We irradiated MOS-chips with an 8-MeV pulsed electron beam (2 μs pulse length, 25 Hz pulse repetition rate) at the LINAC Irradiation Facility (ISOF-CNR, Bologna, Italy). We irradiated each of a total of four test-chips to the increasing doses of 1, 3, 10 and 30 Mrad(SiO_2) with a dose rate of 13 krad(SiO_2)/s. The duration of the irradiation experiment was two hours.

The measuring setup used for the irradiation experiment is schematically described in Tab. 1. Before the irradiation we programmed the cells of the four test-chips one half in the SET state and one half in the RESET state (Step 1) with a checkerboard pattern. This programming operation was performed one month before the irradiation (Step 2). In this way, the RESET distribution drift due to the instability of the amorphous GST has only a negligible impact on the measurements performed during the experiments. In fact the resistance variation rate

reduces with the time elapsed from the RESET operation and, after one month, distributions measured within some hours (i.e., more than the duration of the irradiation experiment) show no differences.

Few minutes before the irradiation we read the test-chips (Step 3). After each irradiation step we read the cells (Step 5). Then we "inversely" programmed one half of the cells (Step 6) in each of the four devices and we read the test-chips again (Step 7). In the "inverse" programming step cells in the RESET state have been programmed in the SET state and vice-versa, in order to investigate if the radiation could compromise the SET/RESET operations. Afterward we inversely programmed (Step 8) and read (Step 9) again the test-chips. It is important to underline that each inverse programming operation performed during the irradiation experiment was applied on the same subset of cells. Hence one half of the cells were only read and never programmed during the whole irradiation experiment. In the following we will refer to these cells simply as "read cells" (i.e., those cells not programmed at Step 6 and 8) while we will call "programmed" the other cells (i.e., those cells programmed at Step 6 and 8).

3.2 Experimental results

Fig. 6 shows the RESET (a) and the SET (b) distributions of the read cells of a chip measured before irradiation and after each irradiation step; in Fig. 7 we report the average current (I_{AVE}) of the RESET and SET distributions as a function of the total dose. The I_{AVE} of the RESET distribution (RESET-I_{AVE}) increases constantly as a function of the dose and the maximum shift is 1.7 μA after 30 Mrad(SiO_2) (Fig. 7(a)).

The SET distribution shows a different behavior (Fig. 7(b)). In fact, the SET-I_{AVE} increases at low irradiation dose. At 3 Mrad(SiO_2) the SET-I_{AVE} shows a turn-over and starts decreasing. The maximum SET-I_{AVE} shift is 2.5 μA, measured after 3 Mrad(SiO_2).

The functionally of the SET and the RESET operations is not compromised by the irradiation. Fig. 8 shows the RESET (a) and SET (b) distribution of the programmed cells measured before irradiation and after each irradiation step. In Fig. 9 we report the corresponding I_{AVE} as a function of the dose. The distributions reported in Fig. 6 and in Fig. 8 were measured on the same test-chip during Step 9 with reference to Tab. 1. Comparing Fig. 6 and 7 with Fig. 8 and 9, we note that programmed and read cells show a similar behavior as a function of the dose. In fact, also the RESET-I_{AVE} of programmed cells constantly increases with dose (Fig. 9(a)) and the programmed cell SET-I_{AVE} shows a turn-over (Fig. 9(b)), as the read cell SET-I_{AVE}. In the programmed cells, the maximum shift of the RESET-I_{AVE} is 2.4 μA and that of the SET-I_{AVE} is 3 μA.

In Fig. 10 we compare the RESET (a) and the SET (b) distributions of read and reprogrammed cells measured after 1 Mrad(SiO_2). These distributions were read at Step 9 with reference to Tab. 1. The programmed RESET distribution (Fig. 10(a)) clearly features higher values respect to the read cell distribution and the difference between their I_{AVE} is 0.5 μA. On the other hand, the read and programmed SET distributions (Fig. 10(b)) shows only negligible variations. In Fig. 11 we report the differences between the programmed and the read cell RESET-I_{AVE} (ΔI_{AVE}-RESET) and SET-I_{AVE} (ΔI_{AVE}-SET) as a function of the dose. ΔI_{AVE}-SET is 0.4 μA before irradiation and it features a maximum value of 2.3 μA that corresponds to a 3.5% variation respect to the SET-I_{AVE}. These values of ΔI_{AVE}-SET are compatible with the variations of the distributions measured after a programming operation in fresh devices. In fact, we do not

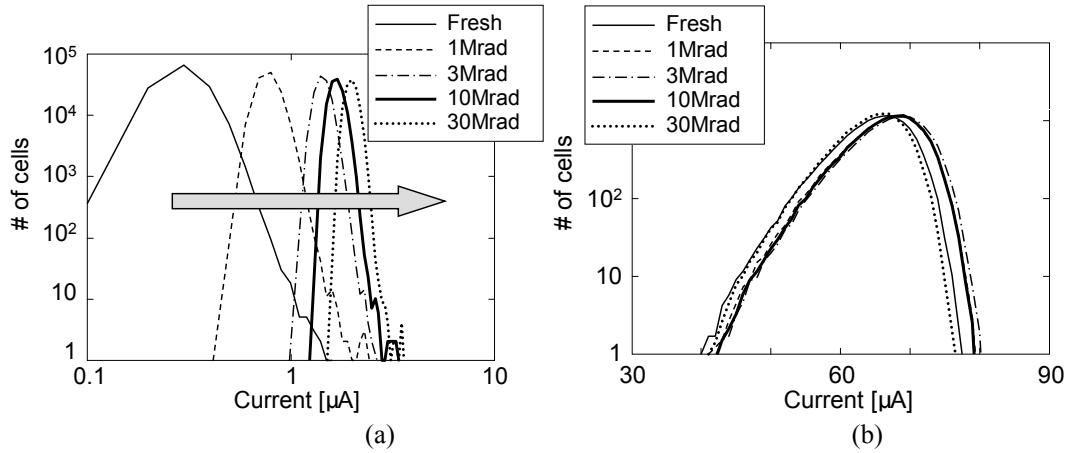


Fig. 6 RESET (a) and SET (b) read cell distributions measured before irradiation and after each irradiation step.

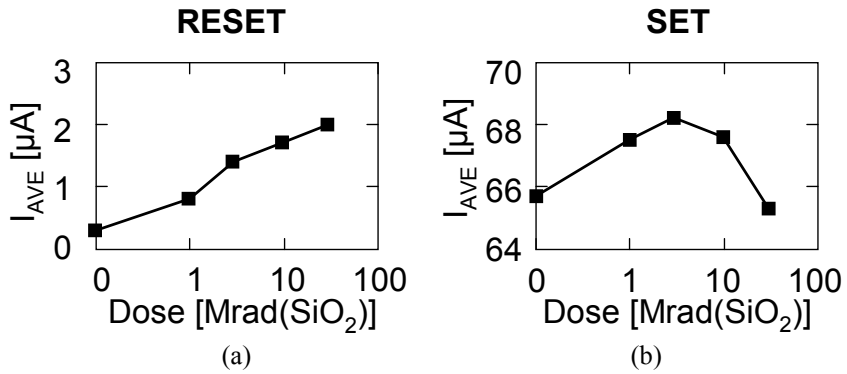


Fig. 7 Average current of the RESET (a) and SET (b) read cell distributions as a function of the dose.

use a "controlled" algorithm for the SET operation, i.e., we do not measure the resistance of each cell after the SET operation, reprogramming it if necessary, in order to obtain the same resistance value after each programming. Hence the distribution measured after a SET operation does not perfectly match the previous one. For the same reason, ΔI_{AVE}-SET is not null even before the irradiation experiment.

The programmed cell RESET-I_{AVE} is higher than the read cell RESET-I_{AVE} for each irradiation dose and ΔI_{AVE}-RESET ranges between 0.5 and 0.7 μA (Fig. 11(a)). These values are noticeably higher than the read cell RESET-I_{AVE}, corresponding to variations of 62.5% and 35%, respectively.

These large variations do not depend on the irradiation. In fact, they are due to the increase of the amorphous GST resistance with time. The read cell distribution was measured one month after the RESET operation while the programmed cell distribution only few minutes after the RESET operation. Hence, it is clear that the cell distribution measured immediately after the RESET operation is noticeably higher than that measured after longer times and this explains the differences observed in Fig. 10(a).

Fig. 12 shows the RESET (a) and SET (b) programmed cell distributions measured 10 minutes, 2 hours, 1 day and 1 month after irradiation to 30 Mrad(SiO_2), by storing the devices floating at room temperature. The corresponding I_{AVE} are reported in Fig. 13. Both the SET and RESET distributions shift toward current values lower than those measured immediately after

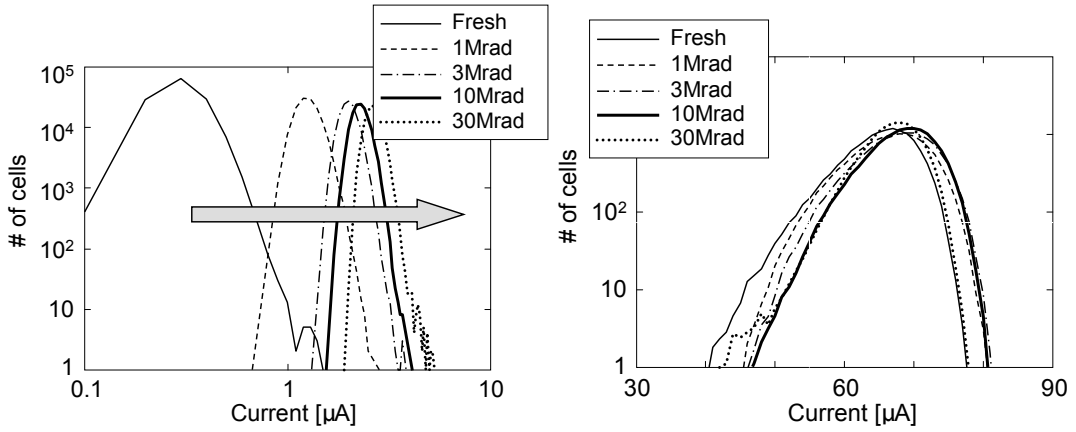


Fig. 8 RESET (a) and SET (b) programmed cell distributions measured before irradiation and after each irradiation step.

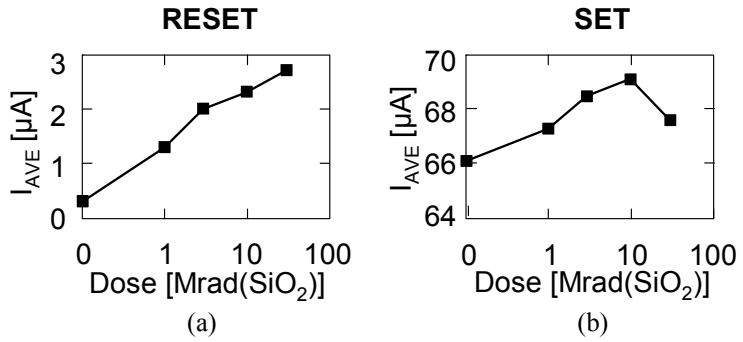


Fig. 9 Average current of the RESET (a) and SET (b) programmed cell distributions as a function of the dose.

irradiation. The SET-I_{AVE} variation is 6.2 μA and that of the RESET-I_{AVE} is 2 μA. Noticeably, after one month the SET distribution is shifted at current values lower than the fresh one while the RESET distribution is still slightly higher than the fresh one. The read cell distributions show the same behavior during the post irradiation annealing.

3.3 Discussion of the experimental results

3.3.1 SET distribution modifications

As reported in [Sch02, Pac03, Man02], TID produces important modifications of the electrical characteristics of 0.18 μm technology n-channel MOSFETs with thin gate oxide. First, TID commonly produced a reduction of the V_{th} due to the accumulation of positive charge in the gate oxide. The V_{th} reduction is lower than few hundreds mV due to the small thickness of the gate oxide [Man02, Fac05]. Increasing the dose, the V_{th} enhances due to the increase of interface defects that overwhelm the effect of the positive charge trapping [Fac05]. Gate-oxide charge trapping and interface defects build up affect the electrical behavior of the MOSFET in the "ON" state, i.e., when $|V_{GS}|$ and $|V_{DS}| > 0$ V. The MOSFET behavior in the OFF state (i.e., when $V_{GS} = 0$ V) is noticeably affected also by positive charge trapping in STI. This positive charge forms a parasitic transistor that drives an OFF-state current and prevents the MOSFETs

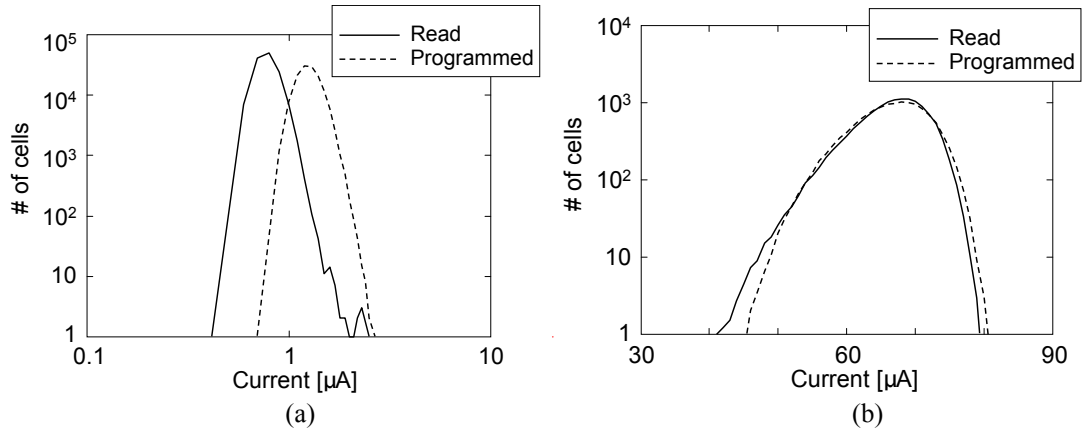


Fig. 10 RESET (a) and SET (b) distributions measured after 1Mrad(SiO_2) irradiation dose. The solid lines represents the distributions of read cells and the dotted lines the distributions of programmed cells.

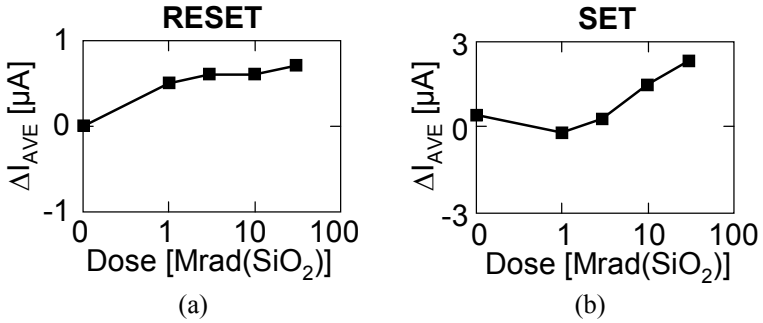


Fig. 11 Difference between the programmed cells and the read cells average currents (ΔI_{AVE}) measured after each irradiation step.

to be completely turned off [Sha98]. The OFF-state current can assume even considerable values in the order of hundreds of nA [Man02, Fac05, Sha98, Tur04].

The shift observed in the SET distribution after irradiation can be ascribed to the modifications of the MOSFETs electrical characteristics. In particular, the read cell SET distribution increases for doses lower than 10 Mrad(SiO_2) (Fig. 7(b)). This radiation-induced shift toward higher current values mostly comes from positive charge trapping in the gate oxide of the BL-selector MOSFETs.

With reference to the circuit of Fig. 2(a), during the reading operation V_1 and V_3 are high and V_2 is set at 0.9 V. The GST resistance of a SET cell is in the order of 10 kΩ. During the reading operation the BL-selection MOSFET operates in the saturation region and its threshold voltage is 350 mV [Bed04]. With our measuring set-up, we can choose the value of V_2. Fig. 14(a) shows the distributions of a subset of SET cells measured in a fresh device. The different distributions were measured setting $V_2 = 0.9 + \Delta V_2$, with ΔV_2 = -22.5, 0, +22.5, +45 mV. Fig. 14(b) shows the I_{AVE} of the distributions as a function of ΔV_2. Increasing ΔV_2 (i.e., V_2), the distribution moves toward higher current values and the relation between ΔV_2 and I_{AVE} is almost linear in the values range considered in this experiment. The results of Fig. 12 indicate that the measured cell current is proportional to the GST resistance and to V_x:

$$I_{CELL} \cong V_X / R_{GST} \qquad (1)$$

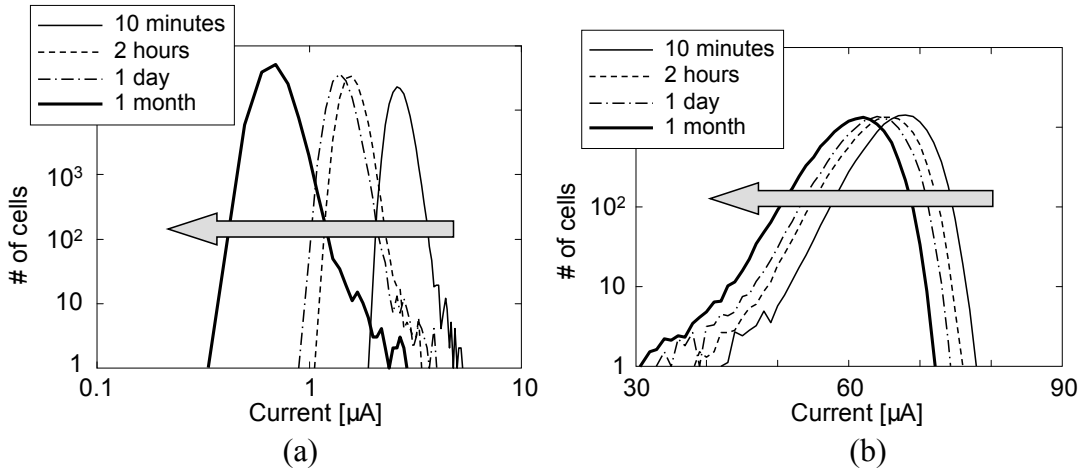


Fig. 12 RESET (a) and SET (b) programmed cell distributions measured 1 minute, 2 hour, 1 day and 1 month after the irradiation.

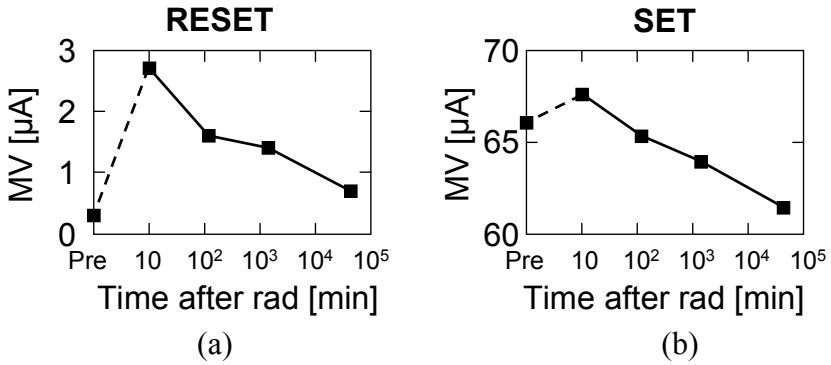


Fig. 13 Average current of the RESET (a) and SET (b) programmed cell distributions as a function of the time after the irradiation

and the node X voltage depends on the M1 threshold voltage (V_{thM1}), being [Bed04]:

$$V_X \cong V_2 - V_{thM1}. \quad (2)$$

Hence, the current flowing trough the GST depends on V_{thM1}. Radiation produces positive charge trapping in M_1 gate oxide. The consequent V_{thM1} reduction results in an enhancement of V_X and then in an enhancement of the current measured during the reading operation.

Incidentally, positive charge trapping in the gate oxide of M_2 has no effects on the measured current. In fact, the voltage applied to the M_2 gate is so high (~3.5 V) that even a large variation of V_{thM2} should have a negligible effects on the current driven by M_2 and hence on the read current.

From equation (2) it is clear that the V_2 enhancement and the V_{thM1} reduction produce the same effect on V_X (and hence on the read current). The variation observed after 3 Mrad(SiO_2) in the SET-I_{AVE} of is 2.5 μA (Fig. 7). From Fig. 14(b), we can estimate that this 2.5 μA variation corresponds to a V_{thM1} reduction of 20 mV. This value agrees with the V_{th} variation due to charge trapping after high radiation doses in 7 nm gate oxide [Man02].

Increasing the dose, the SET-I_{AVE} shows a turn-over and starts decreasing (Fig. 7(b)).

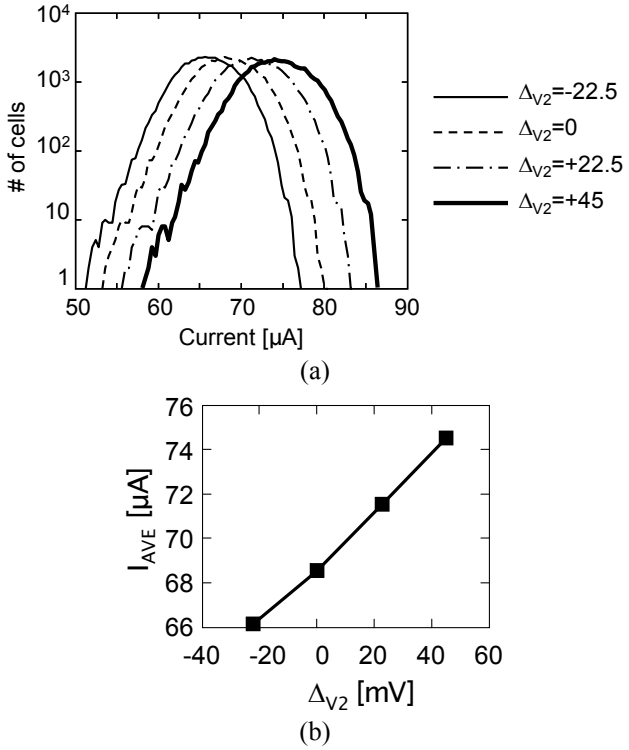


Fig. 14 (a): SET distributions measured in a fresh device with different values of V_2 (V_2 = 0.9V + Δ_{V2}). (b): Average current of the distributions as a function of Δ_{V2}.

The enhancement of the interface defects number (N_{it}) in the MOSFETs in series to the GST element (M_1 and M_2 in Fig. 2(a)) produces the observed SET-I_{AVE} reduction. In fact, the N_{it} increase results in an enhancement of the MOSFETs' V_{th} [Sch02, Pac03]. Equation (2) indicates that a V_{thM1} enhancement results in the reduction of the measured current, in agreement with our experimental results.

Secondly, the N_{it} increase causes also a reduction of the MOSFETs' mobility with a consequent reduction of the current driven by M_1 and M_2 (and then of the cell current).

Hence, the SET distribution variation is mostly attributed to the combined effect of the positive charge trapping in M_1 (causing the current enhancement) and the enhancement of interface defects in M_1 and M_2 (causing the current reduction). Noticeably, the turn-over is observed after 3 Mrad(SiO_2) in agreement with data reported in [Fac05].

Consider now the programmed SET cells. These cells were inversely programmed two times after each irradiation step: during the first programming (Step 6 in Tab. 1), they change from the SET to the RESET state. In the second programming (Step 8 in Tab. 1), they pass from the RESET to the SET state. On the contrary, the read SET cells were never reprogrammed.

Comparing the distribution of read and of programmed cells (Fig. 10(b)) we observe only marginal differences after irradiation. This result indicates that irradiation does not produce appreciable variations of the GST characteristics in the active area. In fact, during the first programming the cells change from the SET to the RESET state and the active area of the GST is melted. Hence, any defects produced by radiation should be annealed and the possible radiation induced modifications of the GST active area should be disappeared in the programmed cell distribution. On the contrary, these possible modifications should affect the

read cell distribution. Being the difference between the programmed and the read cell distribution negligible, we can state that the characteristics of the GST active area are not appreciably modified by radiation.

The programmed and the read cell SET distribution shows the same behavior as a function of the doses (Fig. 7(b) and Fig. 9(b)). This result confirms that the SET distribution behavior during irradiation is mostly ascribable to the degradation of the MOSFETs electrical characteristics. In fact, while any possible defect produced by radiation in the GST active area is neutralized during the programming, the gate oxide trapped charge and N_{it} are not affected by this operation. Since read and programmed cells show the same behavior with dose, the variation of the cells is dominated by the gate oxide trapped charge and by N_{it}.

During the post-irradiation room temperature annealing (Fig. 12(b) and 13(b)), the SET distribution drifts toward lower current values. This variation may be attributed to the neutralization of positive charge trapped into MOSFETs gate oxide [Sch02]. From Fig. 14(b), we estimated that the 6.2 μA variation observed after the annealing corresponds to a 45 mV V_{thM1} increase.

After 1 month, the SET-I_{AVE} is lower than before irradiation. In fact, after the neutralization of the positive trapped charge, the effect of the interfaces defects prevails resulting in the measured current reduction.

3.3.2 RESET distribution

In a RESET cell, the GST resistance is in the order of 1 MΩ and the measured current is in the order of 1 μA. This current is mainly limited by the GST resistance. Considering Fig. 7(a), the I_{AVE} of the RESET distribution is 0.3 μA before irradiation; after 30 Mrad(SiO_2) the I_{AVE} is 2 μA, corresponding to 666% of the pre-rad value. Such a difference cannot be explained only by positive charge trapping in the gate oxide. In fact, the V_{thM1} reduction should be more than 1 V in order to account for the measured RESET-I_{AVE} variation. Such a large V_{thM1} variation is not compatible with the V_{th} variation produced by radiation in MOSFETs with 7 nm thick oxide [Man02].

We can explain the RESET-I_{AVE} behavior considering the leakage currents that affect the WL-selector MOSFETs (M_2). The leakage that affects M_2 of the read cell has negligible effects on the measured current. In fact, during the reading operation we apply a high gate voltage to M_2 and the current is limited only by the GST resistance. Yet, the leakage currents of all the 2047 not-selected MOSFETs connected at the bit-line result in an enhancement of the measured current. The RESET-I_{AVE} enhancement is 1.7 μA after 30 Mrad(SiO_2). Being this variation due to 2047 WL-selector MOSFETs, the leakage current of a single MOSFETs is in the order of 1 nA.

The not-selected MOSFETs are in the off state during the reading operation. This off-state leakage can be ascribed to positive charge trapping in the STI of MOSFETs [Fac05, Sha98, Tur04].

After irradiation, the RESET distributions drift toward lower current values (Fig. 12(a)). This variation may be only in part attributed to the neutralization of positive charge trapped into M_1 gate oxide, as in the case of the SET distribution. Other facts are responsible for the measured drift. First, the instability of the amorphous GST results in the reduction of the RESET-I_{AVE}. Second, the reduction of the leakage currents contributes to the RESET-I_{AVE} variation. The leakage reduction could be due to the neutralization of the charge trapped in the shallow trench

TABLE II
DETAILS OF THE PROTON IRRADIATION

Chip	Chip type	Dose	Area	Fluence	Protons per GST
1-BJT	8Mbit - BJT	3, 10, 30	total chip area	1.7×10^{12}	17, 57, 170
2-BJT	8Mbit - BJT	3, 10, 30	total chip area	5.7×10^{12}	17, 57, 170
3-BJT	8Mbit - BJT	3, 10, 30	total chip area	1.7×10^{13}	17, 57, 170
4-MOS	4Mbit - MOSFET	1	total chip area	5.7×10^{11}	6
5-MOS	4Mbit - MOSFET	3	total chip area	1.7×10^{12}	17
6-MOS	4Mbit - MOSFET	10	total chip area	5.7×10^{12}	57
7-MOS	4Mbit - MOSFET	3	part of the array	1.7×10^{12}	17
8-MOS	4Mbit - MOSFET	10	part of the array	5.7×10^{12}	57
9-MOS	4Mbit - MOSFET	30	part of the array	1.7×10^{13}	170

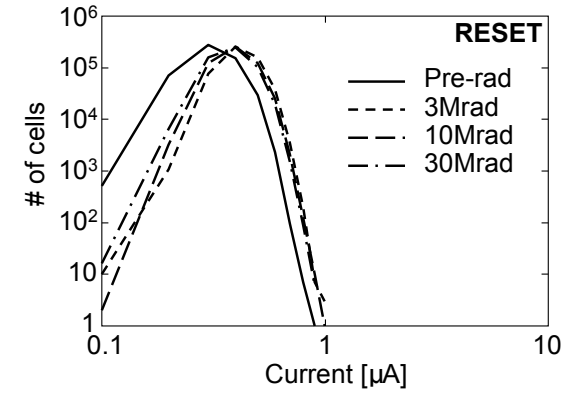
insulation oxide that causes the OFF-state current. The positive charge produces an electric field at the STI edges that attracts electrons. These electrons can neutralize the trapped charge. Moreover, TID produces also interface defects at the STI edges. Yet, while the positive charge build-up is fast, the interface defects formation is a slower process [Sch02]. Hence, the leakage reduction can be attributed in part to the positive charge neutralization and in part to the enhancement of interface defects with time after the irradiation.

4. Proton irradiation effects

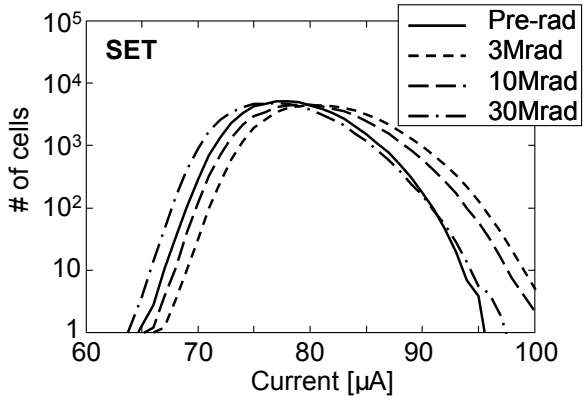
4.1 Irradiation Experiments

We irradiated PCM chips with 2-MeV protons and with 50-MeV Cu ions. The cells of all chips were programmed with one half in the RESET state and with one half in the SET state with a checkerboard pattern before irradiation.

Proton irradiations were performed using the μ-beam line at the AN2000 irradiation facility at the INFN-Laboratori Nazionali di Legnaro (Italy). The details of the proton irradiations are given in Table 1. We irradiated a total of 3 BJT-chips and 6 MOS-chips. Each BJT-chip was irradiated to increasing doses of 3, 10, and 30 Mrad(SiO_2) (chip 1,2,3-BJT in Table 1) and three MOS-chips were irradiated to doses of 1, 3 and 10 Mrad(SiO_2) (chip 4,5,6-MOS). The entire chip area of chips 1-6 was uniformly irradiated. Furthermore, in three other MOS-chips (7,8,9-MOS) only a part of the cell array was irradiated by using a beam spot of 1×2.3 mm^2 at doses of 3, 10, and 30 Mrad(SiO_2). Based on the size of the cell array of 2.4×4.4 mm^2, we estimate that 21% of the total array cells were exposed to irradiation, corresponding to ~910K cells. The external circuitry of chips 7, 8 and 9-MOS was not irradiated. All of the chips were irradiated at a dose rate of 10 krad(SiO_2)/s. The proton fluence and the nominal number of protons that passed through the GST active area of each cell are also given in Table 2.



(A)



(B)

Fig. 15 RESET (A) and SET (B) distributions measured before irradiation and after 3, 10 and 30 Mrad(SiO_2) proton irradiation in a chip with BJT selectors (irradiation performed on the entire chip area).

4.2 Prompt Irradiation Effects

4.2.1 Experimental results

Fig. 15 shows the RESET and the SET distributions of chip 1-BJT measured before and after proton irradiation to 3, 10 and 30 Mrad(SiO_2). The SET distribution shifts by +2.6 μA after 3 Mrad(SiO_2) and then it shows a turnover and starts decreasing. The RESET distribution shifts by +0.1 μA after 3 Mrad and it remains almost constant for higher doses.

Fig. 16 shows the RESET and the SET distributions of chip 6-MOS taken before and after proton irradiation to 10 Mrad(SiO_2). The RESET and the SET distributions shift by +7.7 μA and by +11.5 μA, respectively, after irradiation. These shifts are noticeably larger than those observed in BJT-chips at the same dose (Fig. 15).

Fig. 17 shows the distributions of chip 9-MOS measured before and after proton irradiation to 30 Mrad(SiO_2) over a fraction of the cell array. The SET distribution shows a slight shift toward higher current. Noticeably, a clear second peak appears in the RESET distribution after irradiation, shifted by +5.2 μA with respect to the main distribution. For clarity, we report in Fig. 18 the distribution of $\Delta I_{POST-PRE}$ (i.e., the difference between the cells current values measured after and before irradiation) of chip 9-MOS, showing that both the RESET and SET

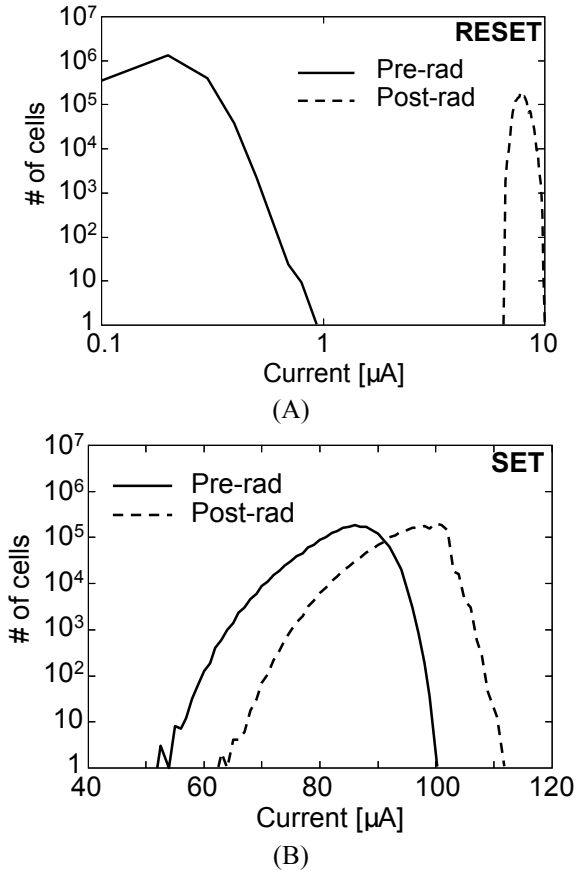


Fig. 16 RESET (A) and SET (B) distributions measured before and after 10 Mrad(SiO_2) proton irradiation in a chip with MOSFET selectors (irradiation performed on the entire chip area).

$\Delta I_{POST-PRE}$ distributions feature a second peak, at +5 and +4 μA, respectively. This second peak corresponds to the subset of cells whose current substantially increased (>1 μA) after irradiation. We calculated that the number of cells with a current shift larger than 1 μA is almost the same for RESET and SET, being 756k cells in both cases. Hence, 1.5 M cells feature a $\Delta I_{POST-PRE} > 1$ μA: noticeably, this value is larger than the number of irradiated cells (~910k)!

In Fig. 19 we show a color map of $\Delta I_{POST-PRE}$ for chip 9-MOS 2048×2048 cell array (both SET and RESET cells). In Fig. 19 we highlighted two regions of the array: Region A corresponds to the irradiated area; Region B contains all the cells featuring $\Delta I_{POST-PRE}>1$ μA. Regions A and B extend between the 420th BL and the 1140th BL along the X axis. Region A (i.e., the irradiated region) spans between the 430th and the 1530th WL while Region B includes all the WLs. Hence, not only the cells hit by the beam feature $\Delta I_{POST-PRE}>1$ μA but all the cells connected to a BL hit by protons.

4.2.2 Discussion

The SET distribution of 1-BJT (Fig. 15(b)) shifts by +2.6 μA after proton irradiation to 3 Mrad(SiO_2). This shift is due to proton induced positive charge trapping in the gate oxide of the BL selector MOSFETs (M_1 in Fig. 2(b)), with a consequent reduction in threshold voltage (V_{th}) [Sch02, Pac03, Man03, Fac05]. This results in the enhancement of the measured current, as

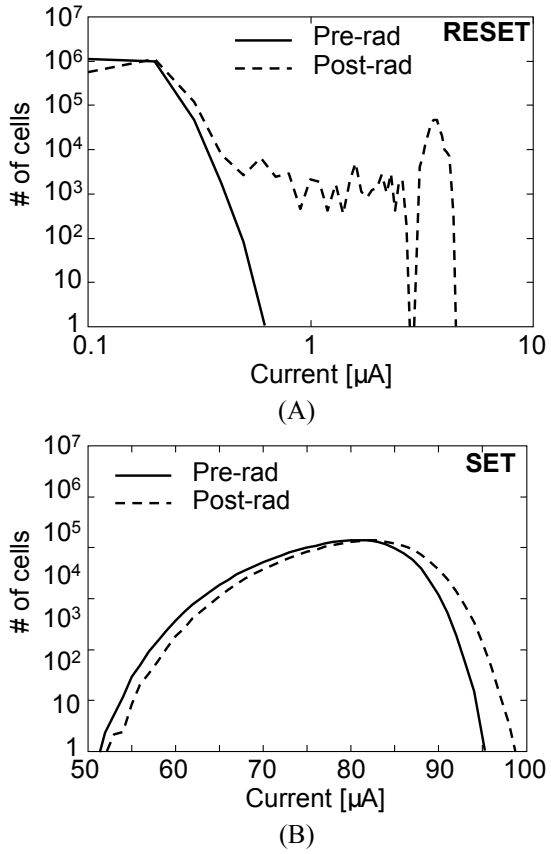


Fig. 17 RESET (A) and SET (B) distributions measured before and after 30 Mrad(SiO_2) proton irradiation in a chip with MOSFET selectors (irradiation performed on a part of the cell array).

already described before in this chapter. The shift of the RESET distribution is due to the same cause; however, it is smaller because GST features a higher resistance.

At higher doses, the SET distribution shows a turnover and starts decreasing. This fact is related to the enhancement of interface defects in M_1 that causes a $V_{Th}(M_1)$ enhancement. As a consequence, V_x reduces and we observe a reduction of the measured current.

Comparing Fig. 15 and Fig. 16, we observe that the distributions of MOS-chips feature larger shifts after irradiation. In particular, the average current of the RESET distribution increases from 0.2 to 7.9 μA (Fig. 16(a)).

The causes of this shift can be determined from the irradiation results of chip 9-MOS (Fig. 17-19). Only a fraction of the chip 9-MOS cell array was irradiated: hence the shift observed in Fig. 7, 8 is not due to positive charge trapping in the gate oxide of BL-selector MOSFETs that were not irradiated. Secondly, not only the irradiated cells feature a large shift (>1 μA) but all of the RESET or SET cells connected to the same BL of the irradiated cells (Fig. 19).

These results are in perfect agreement with the assumption that the MOS-chip distribution shift is due to leakage currents affecting all of the irradiated cells connected at the same BL caused by to radiation-induced positive charge trapping in the Shallow Trench Insulation (STI) of the MOSFETs.

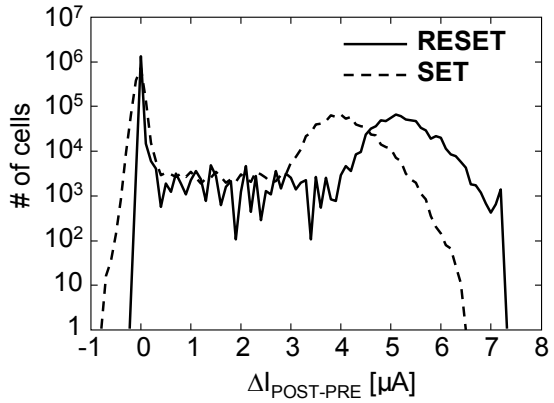


Fig. 18 RESET and SET $\Delta I_{POST-PRE}$ distributions measured before and after 30 Mrad proton irradiation in a chip with MOSFET selectors (irradiation performed on a part of the cell array).

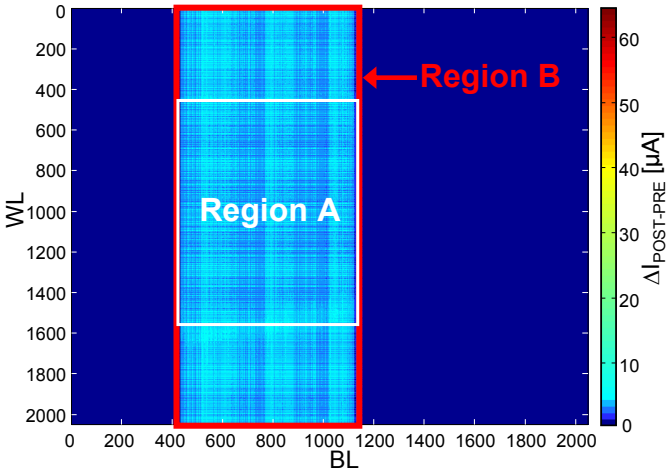


Fig. 19 Color map of the $\Delta I_{POST-PRE}$ value of the cells of a MOS-chip array irradiated with protons to 30 Mrad(SiO_2). Region A indicates the irradiated area and Region B indicates the region where cells feature $\Delta I_{POST-PRE}$ >1 μA.

The positive charge forms a parasitic transistor that drives the off-state leakage current [Fac05, Sha99] (Fig. 20). During the reading of a cell, the leakage currents of all of the irradiated cells connected to the same BL affect the measured current.

The shift of the second peak of Fig. 17 (+5.2 μA), is due to the leakage currents of 1100 cells and then the leakage current that affects a single BL-selector MOSFET is ~5 nA. This value agrees with data in the literature [Fac05].

It is important to note that the leakage currents and the distribution shifts are not due to a modification of the GST resistance. In fact, during the read operation, all of the WL-selector MOSFETs (except the one of the cell being read) are in the off state, and their "equivalent resistance" is higher than the GST resistance (equal to ~1 MΩ and ~10 kΩ in the amorphous and in the crystalline state, respectively). Hence the current that flows through a not-selected cell is controlled exclusively by the WL-selector MOSFET and a variation of the GST resistance would have no effect on the measured current.

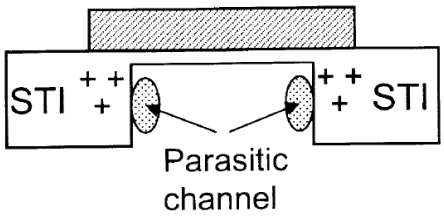


Fig. 20 Representation of the parasitic channel formed by the positive charge trapped into the STI [Fac05].

4.3 Retention tests

4.3.1 Experimental results

To determine if ionizing particles could compromise the retention characteristics of PCM cells, we performed retention tests both at room and high temperature. The room temperature retention tests were performed by measuring the devices several times after irradiation, storing the devices floating at room temperature between two different measurements.

Figs. 21 A and B show the RESET and the SET distributions of chip 9-MOS measured 5 minutes after the irradiation and then 1 hour, 1 day, 3 days and 23 days after the irradiation. In the RESET distribution, the second peak produced by irradiation drifts toward lower current values with time and the cells featuring a large shift after the irradiation drift toward the main distribution. The variations observed in the SET distribution are less noticeable due to the large span of the main SET distribution. For clarity, we report in Fig. 22 the RESET and SET $\Delta I_{POST-PRE}$ distributions measured 5 minutes and 23 days after the irradiation. After 23 days, the second peak of both the RESET and SET $\Delta I_{POST-PRE}$ distributions has drifted toward the main distributions and the variations produced by the irradiation are noticeably reduced.

The high temperature retention tests have been performed heating the irradiated devices at the increasing temperatures of 80, 100, 120, 140, 160, 180° C for 3 hours each temperature, and measuring the devices after each annealing step. All the measurements were performed at room temperature few minutes after the annealing step.

Figs. 23 A and B show the RESET and SET distributions of chip 9-MOS measured before the high temperature experiments and after each high temperature annealing step. In the RESET distribution measured before the annealing, we observe a main distribution, corresponding to cells that are not affected by irradiation, and a second peak corresponding to cells whose current values have noticeably increased after irradiation. The RESET distribution measured after the 80° C step almost overlaps the distribution measured before irradiation. Increasing the temperature to 160° C, the main RESET distribution shifts toward lower current values. The second peak of the distribution features a similar behavior but its variation is larger and after the 160°C step the RESET distribution second peak has completely disappeared. After the 180° C step, the RESET distribution is strongly modified and it extends between 0.1 μA and 52 μA.

The SET distribution (Fig. 23 B) shifts toward higher current values after each annealing step and it reduces its extension. After the 180° C step it extends between 72 μA and 100 μA.

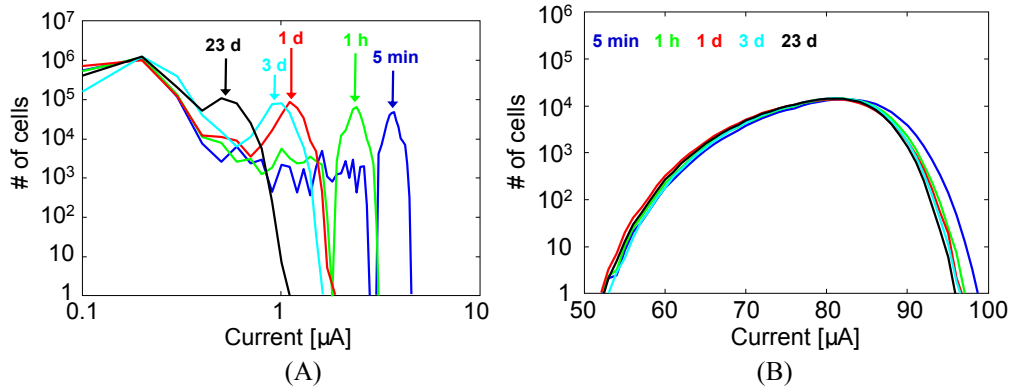


Fig. 21 RESET (A) and SET (B) distributions measured 5 minutes, 1 hour, 1 day, 3 days and 23 days after proton irradiation to 30Mrad(SiO_2) in a chip with MOSFET selectors (irradiation performed on a part of the cell array).

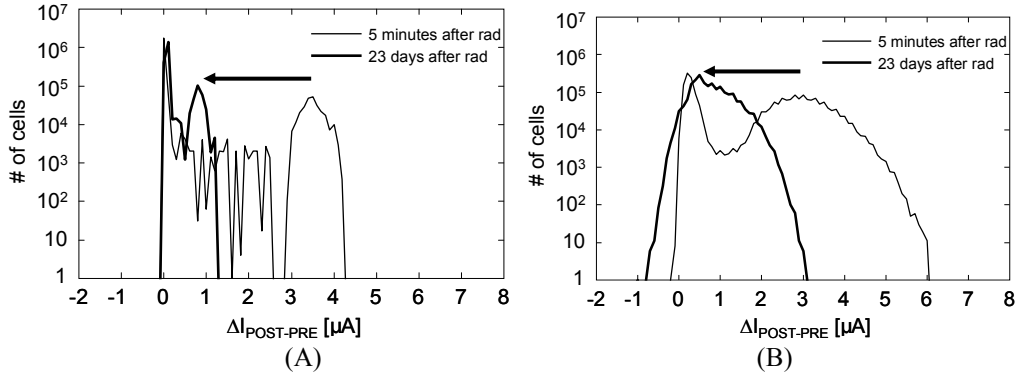


Fig. 22 RESET and SET $\Delta I_{POST-PRE}$ distributions measured 5 minutes and 23 days after 30 Mrad(SiO_2) proton irradiation in a chip with MOSFET selectors (irradiation performed on a part of the cell array).

All of the irradiated chips with MOSFET selectors featured a similar behaviour during the high temperature retention tests.

4.3.2 Discussion

The variation produced by irradiation reduces with time after irradiation both in the RESET and in the SET distributions (Fig. 21). This result is due to the progressive reduction of the leakage current affecting the WL-selector MOSFETs. In each MOSFET, electrons in the bulk are attracted toward the STI edges by the electric field produced by the STI positive trapped charge and they can tunnel into the STI traps recombining with the trapped holes. As the positive charge is neutralized, the electric field at the bulk/STI interfaces reduces as well as the electron density causing a reduction of the leakage and then a shift toward lower current values for both the RESET and the SET distribution second peak.

After the annealing steps at temperatures between 100 and 160° C, the main RESET distributions show a slight shift toward lower current values (Fig. 23 A). This effect is due to an acceleration of the typical drift of the amorphous GST [Pir04b] caused by the high temperatures.

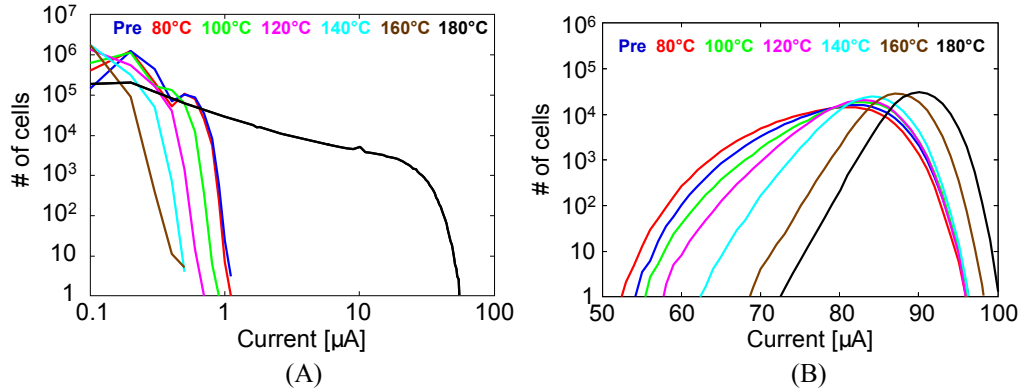


Fig. 23 RESET and SET distributions measured after 30 Mrad(SiO_2) proton irradiation in a chip with MOSFET selectors (irradiation performed on a part of the cell array). The distributions were measured before the annealing and after 80, 100, 120, 140, 140 and 160°C annealing steps.

The second peak of the RESET distribution shows a similar behavior but its shift is larger. The larger shift is due to two causes: the amorphous GST drift and the neutralization of the positive charge trapped into the WL-selector MOSFETs STI. The STI positive trapped charge neutralization is accelerated when the devices are heated [Sch02, Fac05]. After the 140° C annealing step, the second peak is no longer detectable indicating that most of the positive trapped charge has been neutralized.

After the 180° C annealing step, the RESET distribution is strongly modified and it extends to high current values. This is due to the partial crystallization of the amorphous GST of the RESET cells. Yet, any second peak appears in the RESET distribution after the 180° C step and the cells featuring a large shift are uniformly distributed into the array and there is not a correlation between irradiated cells and cells featuring a large shift after the 180° C step. This result confirms that the proton irradiation does not significantly produce a variation of the crystals nucleation dynamics and of the crystal growth process rate in GST [Pri04].

The SET distribution shifts toward higher current values after each annealing step and it reduces its extension. In fact, after a SET operation the GST is in the crystalline state, nevertheless small portions of amorphous GST can still be present in a SET cell, and the cell resistance is reduced due to these amorphous regions. After each annealing step, the amount of amorphous GST into the SET cells is reduced and this results in the observed SET distribution increase. Again, we do not detect any difference between irradiated and non irradiated cells, thus indicating that the irradiation does not affect the GST phase transition.

5. Heavy ion irradiation effects

The heavy-ion irradiation experiments were performed at the μ-beam facility of Sandia National Labs, Albuquerque, NM. We irradiated three MOS-chips with 50-MeV Cu ions. Considering the thicknesses of the passivation layers of the devices (~3 μm), we calculated that Cu ions have an LET=27 MeV×mg^{-1}×cm^2 in the active area of the devices (i.e., the GST and the MOSFETs). By using the μ-beam it has been possible to hit only part of the cell array without damaging the peripheral circuitry that have been proved to be the most sensitive part of our test-chips. In particular, we irradiated three regions with an area 0.127 mm^2 inside the cell array

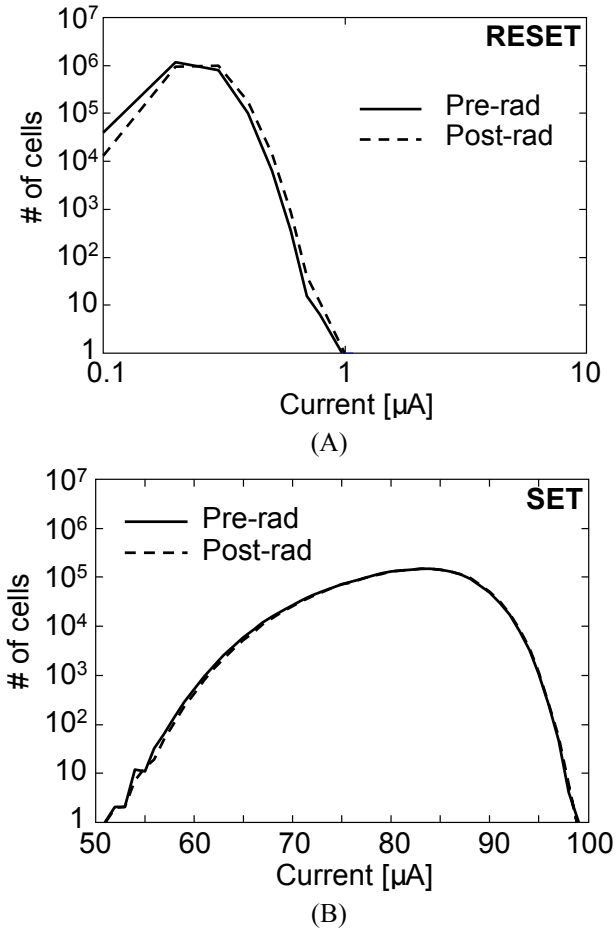


Fig. 24 RESET (A) and SET (B) distributions measured before and after heavy-ion irradiation in a chip with MOSFET selectors.

of each chip. The three regions were exposed to Cu ion fluences of 10^7, 10^8 and 10^9 cm^{-2}. Each region contains about 50.6 K cells. The GST films of 5 and 506 cells were struck by an ion in the regions irradiated at the lowest and at the highest fluences, respectively. During all irradiation experiments, the pins of all chips were grounded.

Fig. 24 shows the RESET and SET distributions of a MOS-chip measured before and after heavy-ion irradiation. Pre and post distributions perfectly overlap and $\Delta I_{POST-PRE}<1$ μA for all the SET cells, and $\Delta_{IPOST-PRE}<0.02$ μA for all the RESET cells.

These results indicate that PCMs with MOSFET selectors are robust against high-LET particle irradiation. In fact, heavy ions do not produce much charge trapping and for this reason we do no observe any modification of the cells distributions. Moreover, it has been proved the resilience of the GST material towards the ionization damage produced by high LET particles. Finally, the functionality of the SET/RESET operations is not compromised by the high-LET particle irradiation.

Chapter 5

Oxide-Nitride-Oxide Stack

1. Introduction

Radiation effects on thin oxide MOS capacitors have been thoroughly investigated in the past years, typically reporting a limited gate current increase after low LET particle irradiation (gamma, X-rays, electrons, low-LET ions) identified as Radiation Induced Leakage Current (RILC) [Pac06, Cec00, Ces98, Lar99, Sca97]. RILC has been attributed to electrons flowing through the oxide by a Single Trap Assisted Tunneling (S-TAT) conduction mechanism exploiting the oxide radiation induced defects uniformly produced over the capacitor area. RILC is usually observed in MOS capacitors with oxide thickness in the range of 4-6 nm, where the defects most effective for RILC are located in the central part of the thin oxide [Pac03]. High LET ions, instead, may leave several oxide defects along their track: the consequent gate current increase is attributed to electron Multi-Trap Assisted Tunneling (M-TAT) and is known as Radiation induced Soft Breakdown (RSB) in thin (<6 nm) oxides [Pac03, Cec00b, Can01, Cec00]. Thicker oxides are more robust against RILC owing to the low tunneling probability of the S-TAT mechanism, even though a DC leakage current has been observed after heavy ion irradiation of a 10-nm oxide [Can01]. In that case, however, the leakage current has been attributed to electron M-TAT through defect clusters generated along the ion tracks.

RILC is usually pretty small in comparison with the high gate leakage observed in contemporaneous CMOS technologies, and should not hamper the functionality of static CMOS digital circuits. Nevertheless, RILC could represent a major issue for Floating Gate Flash memories. In these devices, in fact, FG stores only thousands electrons and a RILC in the order of fA's could discharge the FG in few seconds [Cel04] with a consequent information loss. Heavy-ion irradiation effects on Flash memories have been investigated by several works [Cel04, Cel02, Cel05, Cel06, Cel06b, Cel06c]. The authors attributed the data-retention degradation measured after irradiation to very small RILC through the tunnel oxide. However, in these works it was never considered the possibility that RILC could flow through the control dielectric, constituted by an Oxide-Nitride-Oxide (ONO) stack. In fact, due to the higher thickness of ONO respect to tunnel oxide and its trapping efficiency, this probability was considered negligible [Cel04]. Still, there are no experimental results supporting this assumption.

Beyond being used in FG Flash memories, ONO has great importance because it is used also in SONOS [Des04] and NROM [Sha04] memories that exploit the nitride layer to store charge.

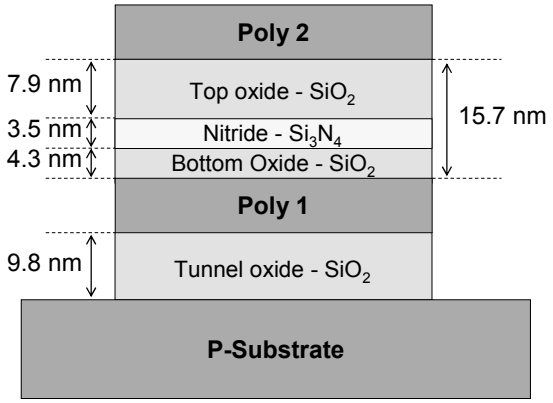


Fig. 1 Schematic of the devices used in this work.

TABLE I
DETAILS OF THE HEAVY ION IRRADIATION

Fluence (cm^{-2})	I ions (E=276 MeV, LET=61)	Ni ions (E=220 MeV, LET=24)
10^{10}	0° - 30°	0° - 30°
3×10^{10}	0° - 30°	0° - 30°
10^{11}	0° - 30°	0° - 30°

Few works have analyzed radiation effects on ONO stack [Lee00, Rap03, Tak99]. In [Lee00, Rap03] the authors focused their attention on charge trapping in MNOS capacitors after X-ray irradiation. The oxide thickness of devices used in [Lee00, Rap03] is in the order of 100 nm.

In this chapter we investigate the heavy ion irradiation effects on capacitors with an ONO stack as dielectric, focusing our attention on the RILC measured after irradiation.

2. Experimental and Devices

We have analyzed capacitors of area 1.14×10^{-3} cm^2 provided by Numonyx (Agrate Brianza, Italy). The structure of a capacitor is represented in Fig. 1. Each capacitor is composed by a p-type substrate, the Tunnel oxide, a high n-doped polysilicon layer (Poly1), an Oxide-Nitride-Oxide (ONO) stack and a high n-doped polysilicon gate (Poly2). The thickness of the Tunnel oxide is 9.8 nm and the bottom oxide, the nitride layer and the top oxide in the ONO stack are 4.3, 3.5, 7.9 nm thick, respectively. We can contact independently substrate, Poly1 and Poly2.

Actually, each device can be considered as a stack of two capacitors: the Tunnel capacitor (Substrate, Tunnel oxide, Poly1) and the ONO capacitor (Poly1, ONO, Poly2). We measure the Tunnel capacitors by applying voltage between Poly1 and Substrate ($V_{Poly1Sub}$) keeping at the same potential Poly1 and Poly2; during the ONO capacitors measurements we apply voltage between Poly2 and Poly1 ($V_{Poly2Poly1}$) keeping shorted Substrate and Poly1.

Heavy-ion irradiation experiments have been performed at the Sirad Irradiation Facility at the Tandem accelerator of the INFN-Laboratori Nazionali di Legnaro, Italy. We have irradiated samples with I ions (E=276 MeV, LET = 61 MeV×mg-1×cm^2) and Ni ions (E=220 MeV, LET

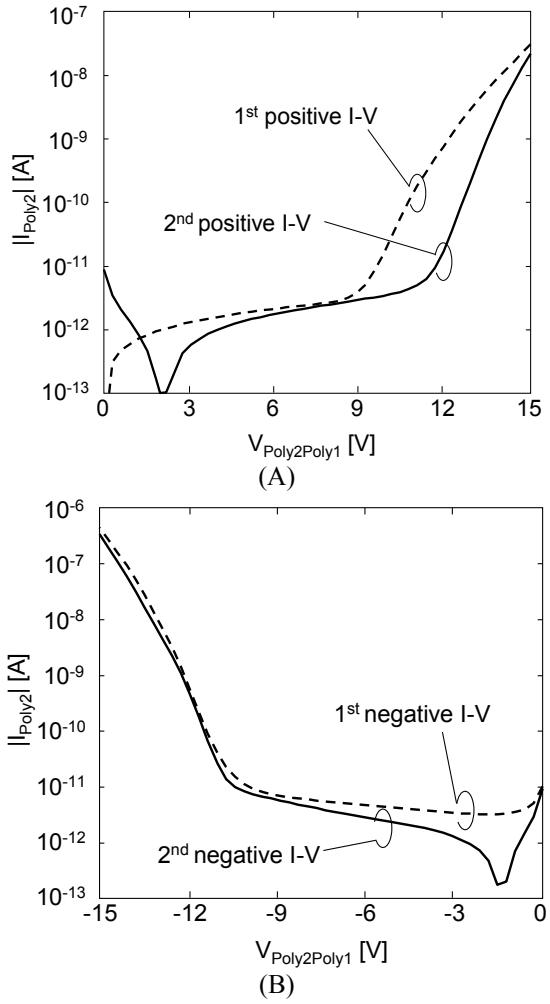


Fig. 2 Positive (A) and negative (B) I-V characteristics of a ONO capacitor measured before irradiation.

= 24 MeV×mg^{-1}×cm^2). We irradiated a total of 6 devices for each ion species: 3 devices were irradiated at 0 degrees incidence angle and 3 at 30 degrees incidence angle (Table I). For each incidence angle, we irradiated the three devices with three different fluences: 10^{10}, 3×10^{10} and 10^{11} cm^{-2}. All the capacitors contacts were grounded during the irradiation.

3. Measuring procedure and conduction mechanisms

Fig. 2 shows various I-V curves (current measured at Poly2) of an ONO capacitor before irradiation, performed by applying the $V_{P2P1} = V_{Poly2} - V_{Poly1}$ voltage to Poly2 and grounding Poly1. Two consecutive I-V sweeps from 0 V up to 15 V (1st and 2nd positive I-V, Fig. 2(a)) have been followed by two consecutive I-V sweeps from 0 V to -15 V (1st and 2nd negative I-V, Fig. 2(b)).

In each I-V sweep we may identify two regions, described now with reference to the 1st curve in Fig. 2(a): the first one featuring low leakage for $V_{P2P1} < 9$ V, and the second one featuring high current at higher V_{P2P1} voltages.

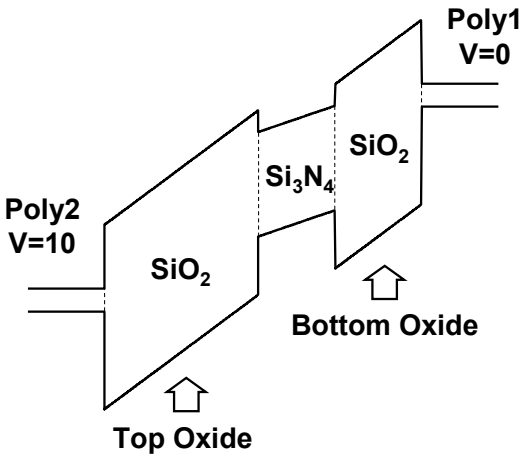


Fig. 3 Band diagram of an ONO capacitor with V_{P2P1} = 10 V.

The current at low electric fields (1st region) is mainly constituted by a transient component due to charge trapping/detrapping in dielectrics. If the I-V sweep is performed at slower ramp rates, we observe a noticeable reduction of the current measured below 9 V [Sco99]. In fact, when we increase V_{P2P1} during the I-V sweep, electrons (and possibly holes) are injected in the dielectric defects, producing the current observed for $V_{P2P1} < 9$ V. Still, as the charge is trapped, the injection electric field decreases and the number of defects that can trap electrons reduces, because most defects had already trapped charges. As a consequence, we observe a reduction of the charge injection and then of the current with time. Hence, it is clear that slowing down the ramp rate we observe a consequent current reduction.

Only in the second region we measure a truly DC current. To elucidate this conduction process, we show the ONO band diagram at V_{P2P1}=10 V in Fig. 3 [Lee00, Rap03]. In these conditions, electrons of the Poly1 conduction band can tunnel through the bottom oxide through a Fowler-Nordheim (FN) conduction mechanism. Some of the FN injected electrons are trapped in the nitride layer or at the nitride/oxide interfaces [Lee00, Rap03], enhancing the barrier seen by the Poly1 conduction band electrons and decreasing the slope of the FN I-V curve starting from 12 V. Such negative trapped charge is not completely and immediately re-emitted when V_{P2P1} returns to 0 V at the beginning of the 2nd I-V sweep (measured immediately after the 1st one). The residual trapped electrons produce a clear shift of the 2nd I-V curve toward higher V_{P2P1} values with respect to the 1st curve. In the 2nd curve, owing to the negative trapped charge, the FN conduction appears only for $V_{P2P1} > 11.5$ V.

To identify the trapped charge amount and position is not straightforward, being sensitive to the applied voltage and to the sample previous history. Further, C-V measurements may give few information due to the high Poly doping level. In fact, the voltages required to deplete or invert one of Poly contacts are so high that they would modify the amount and the position of ONO trapped charge.

The difference between the 3rd and 4th (negative) I-V sweeps in the FN regime (i.e., $|V_{P2P1}|>11$ V) is much smaller than for the first two sweeps, as much of the negative charge has already been trapped before the negative sweeps and only an additional negative charge trapping may take place.

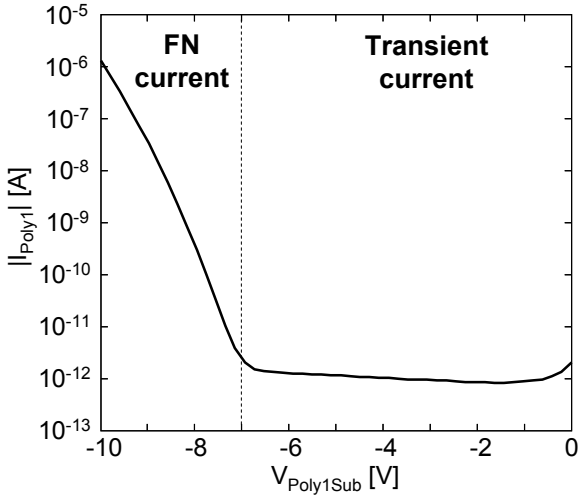


Fig. 4 Negative I-V characteristics of a Tunnel capacitor measured before irradiation.

Noticeably, differences between consecutive positive (or negative) sweeps disappear after the 2nd (4th) curve, indicating that charge trapping has reached a stationary state. Thus, in order to overcome the problems of the transient behavior of the first sweeps, in the following we will consider only the 2nd positive I-V and the 4th negative curves, where not specified.

The tunnel oxide is less sensitive than ONO to charge trapping. So, for Tunnel capacitors we used a measuring procedure simpler than for ONO capacitors. We performed only an I-V sweep by applying bias to Poly1 ($V_{P1Sub} = V_{Poly1} - V_{Substrate}$) from 0 V to 10 V and one from 0 to -10 V, keeping substrate and n-ring grounded (Fig. 4). The FN conduction starts for $|V_{P1Sub}| > 7$ V and for lower bias the measure is dominated by transient components. By repeating the voltage sweep the corresponding I-V curves overlap the first one, indicating that charge trapping is negligible.

4. Heavy Ion Irradiation Effects

4.1 Irradiation Effects on Tunnel Capacitors

Fig. 5 A shows the I-V characteristics of the Tunnel capacitor of the device irradiated with I ions, at 10^{11} cm^{-2}, 0° incidence angle, measured before and after the irradiation. As schematically represented in the figure, we can identify 3 regions in the I-V characteristics corresponding to 3 different effects produced by the irradiation. In the low electric field (E) region ($|V_{Poly1Sub}| < 3.5$ V), we observe a small current enhancement after irradiation. In the mid-E region (3.5 V < $|V_{Poly1Sub}| < 9$ V), a large current enhancement appears in the post-rad curve. Noticeably, in the high E region of Fig. 5 A ($|V_{Poly1Sub}| > 9$ V) we observe a current reduction after the irradiation and the current measured at $V_{Poly1Sub} = -10$ V is reduced by 13% after the irradiation. This difference is better observable in Fig. 5 B where we show the pre and post Tunnel capacitor characteristics limited to the high field region.

All the changes of the I-V characteristic can be explained considering Fig. 6 in which we represent the major modifications produced by a heavy ion in a thick oxide capacitor. (In the following, we do not consider charge trapping phenomena being interested in the permanent

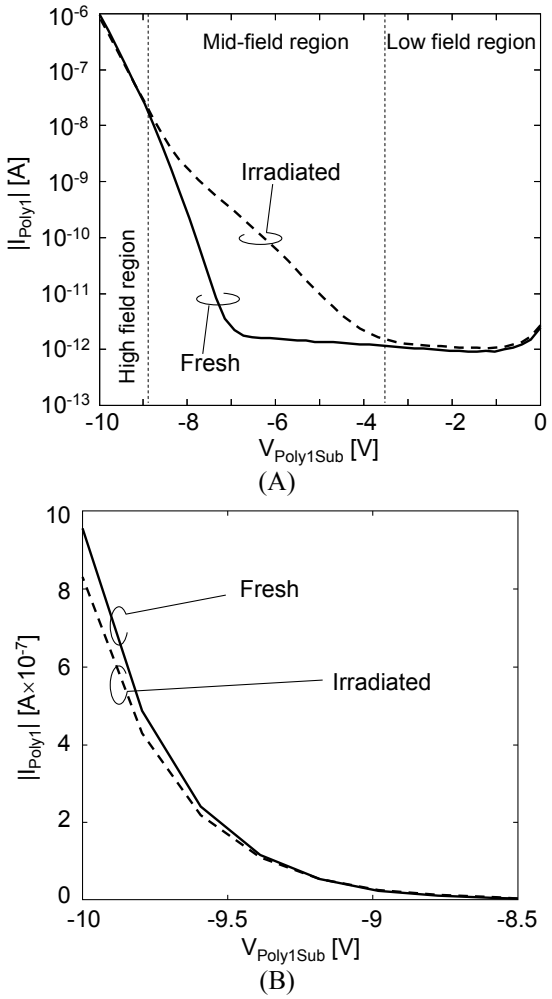


Fig. 5 (A) I-V characteristics of a Tunnel capacitor measured before (solid line) and after (dotted line) the irradiation (I ions, 10^{11} cm^{-2}, 0°). (B) Zoom of the high field region.

modifications produced by ions and we will focus our attention only on those effects that are still observable after the first I-V measurements.)

The ion produces defects in the oxide: some of them are aligned along the ion track while other defects are localized at the oxide interfaces. These two different categories of defects produce different effects.

Considering the defects localized along the ion track, when they exceed a threshold density, they can form a percolative conductive path responsible of RILC [Cel06b, Cel05, Can01]. The current enhancement observed in the mid-E region of Fig. 5 A is due to several conductive paths produced by the I ions into the capacitor. Electrons flow from Poly1 to substrate by Multi Trap-Assisted Tunneling (M-TAT), as represented in Fig. 7. Due to the thickness of the Tunnel oxide (9.8 nm) more than one trap is needed to form a conductive path [Cel02]. Moreover, it is worth to note that traps located at/near the oxide interface do not contribute to RILC. In fact, interface traps can easily capture electrons coming from the cathode but the potential barrier that the trapped electrons have to pass to be injected in the oxide conduction band or to reach the anode is two large. For this reason, interface defects do not noticeably contribute to RILC, except in the case when some of them constitute a conductive path with other traps located in

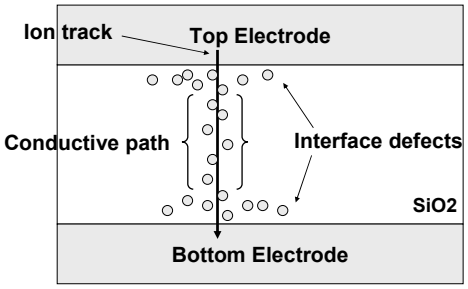


Fig. 6 Schematic representation of the modifications produced by a heavy ion in a capacitor with a thick oxide.

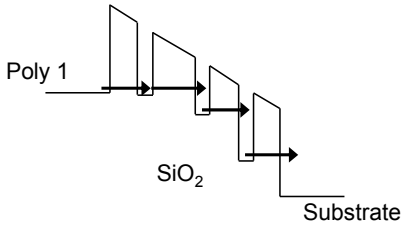


Fig. 7 Schematic representation of Multi-Trap Assisted Tunneling conduction in a Tunnel capacitor.

the oxide bulk or in the middle of the oxide, that are the most effective traps promoting RILC [Lar99].

Consider now the defects produced by ions at and within few nm from the interfaces of the oxide (simply defined as interface defects in the following) (Fig. 5). These interface defects are the responsible of the current increase in the low E region of Fig. 5 A. In this region the measured current is a transient current due to the charging/discharging of interface defects, and it strongly depends on the sweep rate of the measurement [Sco95, Sco96]. The ion-induced interface defects add up to those already present in the oxide, causing an enhancement of the charge trapped at the interfaces during the I-V measurements and then an enhancement of the current.

Interface defects produced by the ions account also for the high E current reduction. The defects at the cathode interface are negatively charged during the I-V measurement causing a reduction of the injection E. This situation is schematically represented in Fig. 8, where we show the band diagram of a Tunnel capacitor before and after the irradiation. At high E the current is mostly due to the FN tunneling of electrons from the cathode. The irradiation produces an enhancement of interface defects that trap negative charge during the I-V measurement. This trapped charge causes an enhancement of the potential barrier seen by electrons of Poly1 (Fig. 8 B) with a consequent reduction of the tunneling efficiency.

Fig. 9 shows the pre and post-rad I-V curves of a Tunnel capacitor irradiated with Ni ions, at 10^{11} cm^{-2}, at 30° incidence angle. In this case the post-rad curve shows two major differences respect to the pre-rad one: a current enhancement for $|V_{Poly1Sub}| < 7.5$ V, and a current reduction at higher voltages. Both these effects are due to the interface defects produced by irradiation, as explained before. Noticeably, no RILC similar to that observed in the mid-E region of Fig. 5 A appears in any of the devices irradiated with Ni ions. This result is due to the lower LET of Ni ions respect to the I ion (24 vs 61). Ni ions are unable to produce a high density of defects along their track and then the conductive path. This result is in agreement with previous data on FG

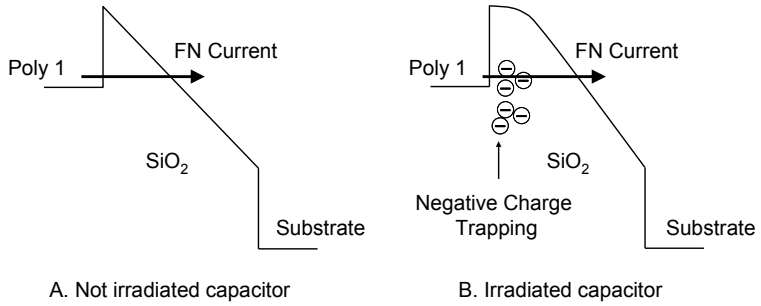


Fig. 8 Schematic band diagram of a Tunnel capacitor at high electric field before (A) and after (B) irradiation. The interface defects produced by the irradiation are negatively charged during the measurements with a consequent Fowler-Nordheim current reduction.

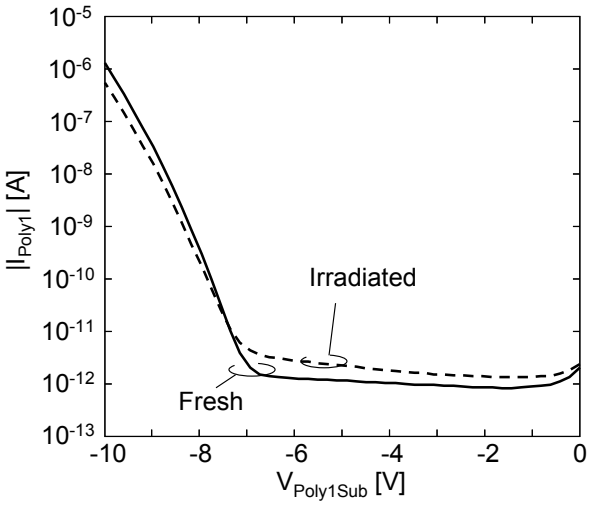


Fig. 9 I-V characteristics of a Tunnel capacitor measured before (solid line) and after (dotted line) the irradiation (Ni ions, 10^{11} cm^{-2}, 30°).

Flash Memories. In [Cel05], Cellere et al. reported that FG Flash cells irradiated with Ni ions with approximately the same energy and LET of those used in this work do not feature a noticeably threshold voltage variation after being reprogrammed after irradiation. On the contrary, FG cells irradiated with ions with higher LET (like I for instance) feature a large threshold voltage reduction if reprogrammed after the irradiation.

The radiation-induced interface defects responsible of the high-field current reduction observed in Fig. 5 B and Fig. 9 are not uniformly distributed at Poly1/Oxide interface but they are localized near the ion hit position. Hence, the FN tunneling is reduced only in these regions damaged by the ions. To estimate the radius of the damaged region is not straightforward because several factors should be took into consideration, such as: the actual defects distribution around the ion hit position and how much the tunneling efficiency is reduced by a certain number of defects, and many others.

However, we can obtain a lower bound of the radius of the interface defects region (IDR) produced by a single ion. Firstly, we assume that IDR has a circular shape. The capacitors irradiated with the fluence of 10^{11} ion/cm^2 were hit by about 10^6 ions. The capacitor high-field current reduced by 13% after irradiation (Fig. 5 B). Assuming that the FN injection is

completely neutralized in the IDR owning to the interface defects, this means that 10^6 IDR correspond to 13% of the total capacitor area and then a single IDR has a radius of 6.5 nm. This is the lower bound of the IDR size. Actually, the IDR extends on a larger area, because the FN tunnel of electrons is not completely naturalized by the charge trapped into the interface defects. Noticeably, if we consider that the FN efficiency is reduced by 50% in the IDR, we obtain a radius of 9.1 nm while assuming a FN efficiency reduction of 1% we obtain a radius of 65 nm.

In [Ces04] the authors investigate the effects of heavy ion irradiation on the drain current of MOSFETs. They assume that the drain current reduction observed after irradiation is due to the defects produced by the ions at the interface between the gate oxide and the channel causing a degradation of the channel conductance. They estimate that the radius of the region damaged by a heavy ion is between 100 and 500 nm. These values are considerably higher than those we obtained in our previous analysis. This discrepancy can be alleviated if we assume an average reduction of the FN injection efficiency in the IDR lower that 1%. For instance, assuming with a FN tunneling reduction of 0.1%, we obtain an IDR radius of 205 nm, in agreement with [Ces04]. Hence an average tunnel efficiency reduction in the order of 0.1% in the IDR seems more realistic.

4.2 Irradiation effects on ONO capacitors

Fig. 10 shows the I-V characteristics of the ONO capacitor measured before and after irradiation with I ions, 10^{11} cm^{-2}, at 0°. A clear enhancement of the current appears after irradiation.

To investigate the nature of this current increase, we biased the irradiated and a reference capacitor at a constant V_{P2P1}=11.5 V and we measured the current as a function of time, obtaining curve(I) and (R), respectively, in Fig. 11. This voltage was selected to get a measurable difference between the two capacitors (see Fig. 10) without inducing an electrical stress that could have cancelled the irradiation effects if a higher voltage were selected.

Current(R) decreases almost linearly in a log-log scale as a function of time, until after 10^4 s it reaches the level of the instrumental noise around 1 pA. This decreasing behavior is due to charge trapping, as reported by numerous works [Sco96, Reu97]. In fact, negative charge injected from Poly1 is trapped in the dielectric stack (particularly in the nitride layer) increasing the potential barrier and then reducing the injection electric field. As a consequence, the measured current decreases. Current(I) shows a completely different behavior. This current decreases slower than Current(R) and it tends to stabilize after a long time. This current must be considered as the sum of two contributes: the first one is the current due to charging/discharging of dielectric defects (that features values similar to Current(R)); the other contribution is a truly DC current effectively flowing through the ONO stack.

This DC leakage current is likely due to electron drift. In fact, hole drift is hampered by the larger nitride/oxide barrier seen by holes than by electrons (Fig. 3). The electrons pass through top and bottom oxide with an M-TAT conduction mechanisms.

However, silicon nitride is known to effectively trapping electrons, because of the large density and the large capture cross section of its electron traps [Lee00]. This fact opens an intriguing question about how electrons can pass across the N nitride layer in the ONO stack. Yet, some works [Kim04] evidence the drift of electrons in a nitride layer under an applied electric field with a Pool-Frenkel (PF) conduction mechanism, featuring an exponential

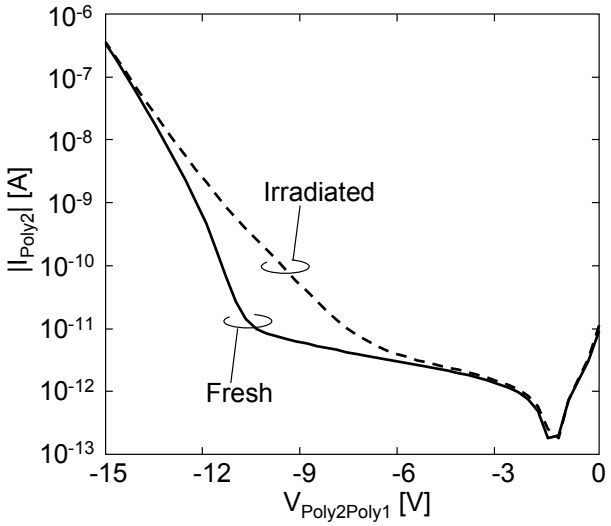


Fig. 10 I-V characteristics of an ONO capacitor measured before (solid line) and after (dotted line) the irradiation (I ions, 10^{11} cm^{-2}, 0°).

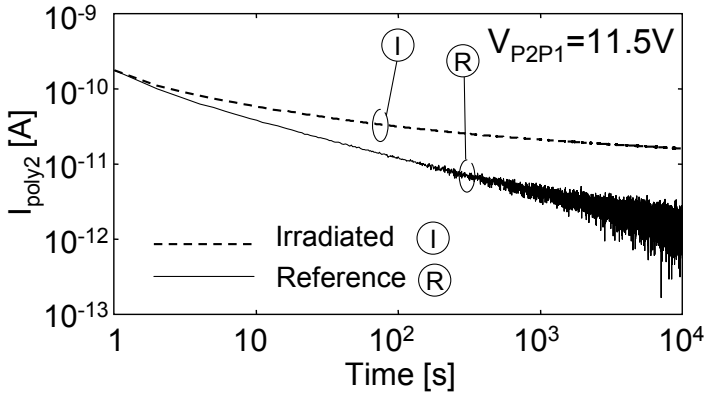


Fig. 11 Current measured in a irradiated (dotted line) and in a reference (solid line) ONO capacitor as a function of time with a constant applied bias of V_{P2P1} = 11.5V.

behavior as a function of the electric field. Hence, the measured leakage current could involve two different conduction mechanisms: M-TAT exploiting the radiation-induced defects in the top and bottom oxide and PF in nitride layer (Fig. 12), likely being the M-TAT the conduction limiting process.

Noticeably, Ni irradiation on ONO capacitors (Fig. 13) does not produce a measurable RILC. After irradiation we observed only a low-E current enhancement and a high-E current reduction due to the interface defects enhancement, as in the case of Tunnel capacitors (Fig. 9) and again in agreement with data on FG cells [Cel05].

Fig. 14 shows the ONO capacitors RILC (extrapolated from the I-V curve at $V_{Poly2Poly1}$=-10 V) as a function of I ion fluence, measured in devices irradiated at 0° and at 30°. For both the irradiation angles, RILC grows linearly with the fluence, as expected. In fact only few of the impinging ions produce the needed density of defects in the ONO stack to create a conductive path. If more ions hit the capacitor, more conductive paths can be generated and then RILC increases.

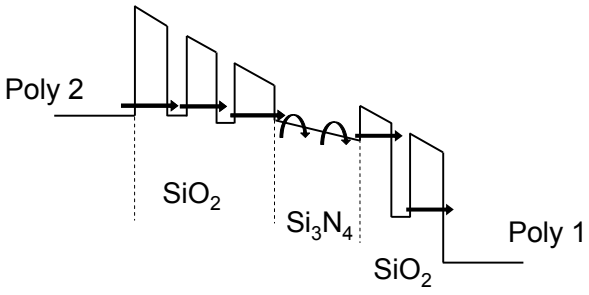


Fig. 12 Schematic representation of the leakage current through a ONO capacitor. The electrons pass the top and bottom SiO_2 layers by M-TAT while in the nitride layer there is a Poole-Frenkel conduction.

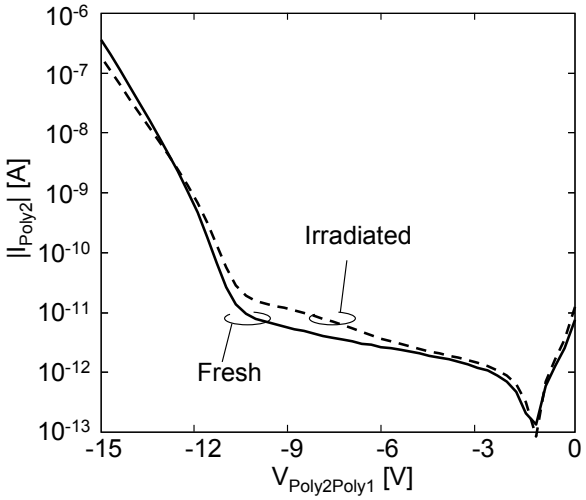


Fig. 13 I-V characteristics of an ONO capacitor measured before (solid line) and after (dotted line) the irradiation (Ni ions, 10^{11} cm^{-2}, 30°).

Moreover, there is a correlation between the RILC intensity and the irradiation angle. For each fluence, the devices irradiated at 30° feature a RILC that is about 60% lower than the RILC of the devices irradiated at 0°. This difference cannot be explained only considering that the devices irradiated at 30° are hit by a lower number of ions (~70%) with respect to the device irradiated at 0°. In fact, we have also to consider that when irradiation is performed at 30° the conductive path produced by the ions into the ONO stack is 40% longer than in the case of 0° incidence angle irradiation. Increasing the conductive path length, a higher number of tunneling processes are required for the electrons to pass through the oxide by M-TAT and this fact causes the observed RILC reduction.

Furthermore, the probability for an ion to form several defects uniformly distributed along its track (i.e., the conductive path) decreases as the ion track in the oxide increases. Hence, we believe that the percentage of impinging ions that form the conductive path is lower when the irradiation is performed at 30°.

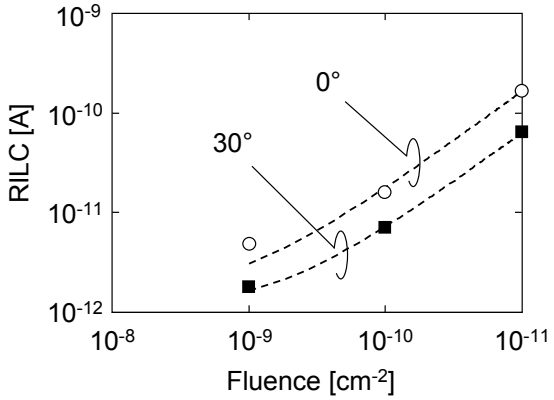


Fig. 14 RILC of ONO capacitors irradiated with I ions at 0° and 30° incidence angle as a function of the fluence. Dotted lines represent the linear fit of the experimental points.

4.3 Comparison between Tunnel and ONO capacitors RILC

Fig. 15 shows the difference between current measured after and before irradiation in the Tunnel capacitor (green line) and in the ONO capacitor (red line) of the device irradiated with I ions, at 10^{11} cm^{-2}, at 0°. The Tunnel and the ONO capacitor difference-currents were extrapolated from the I-V characteristics measured applying a negative bias to Poly1, so that in both cases the electron injection is from Poly1. The difference-currents of Fig. 15 are reported as a function of the E in the insulator. In the calculation of the Tunnel oxide E we considered a flat band voltage of 1 V. Conversely, the ONO E was obtained dividing $|V_{Poly2Poly1}|$ by the equivalent oxide thickness of the ONO stack; in this case no correction is needed being the flat band voltage of the ONO capacitor almost null. In the mid-E region the difference-current is mostly constituted by the RILC component in both the capacitors, while at low and high E it is dominated by other factors as already explained.

The RILC current of the Tunnel oxide is more than one order of magnitude higher than the ONO RILC current for all the E values for which the RILC component can be measured in both the capacitors.

A good fit of the RILC of both the capacitors can be obtained using a power law:

$$I = a \cdot E^b$$

already proposed in [Cec00b, Mir99] to fit Soft BD and Radiation induced Soft BD characteristics in thin oxides. The fitting curves are reported in Fig. 15 (dotted lines). We prolonged the fitting curves down to low E values, in order to investigate the RILC intensity at E values compatible with the operative conditions of a FG Flash cell. In fact, the E in ONO and in the Tunnel oxide is in the order of few MV/cm for most of the operative life of a FG cell. Even at low E, the Tunnel RILC is orders of magnitude higher than the ONO RILC. This result

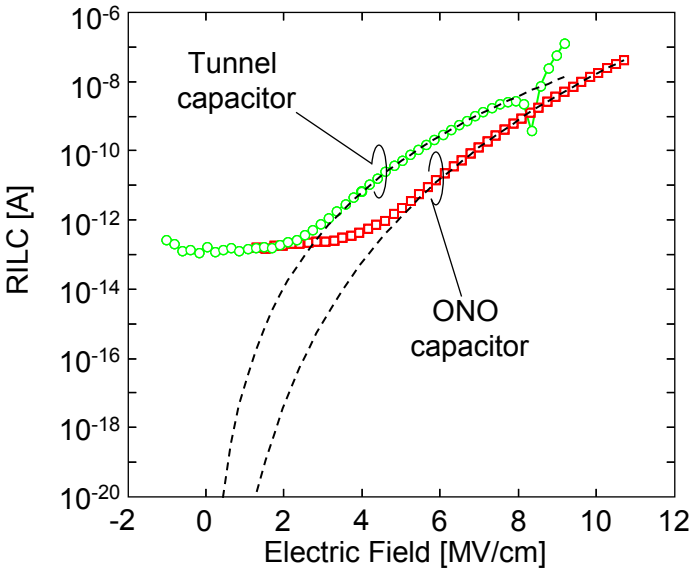


Fig. 15 Difference post-pre of the current measured in the Tunnel and in the ONO capacitor of the device irradiated with I ions, fluence 10^{11} cm^{-2} at 0° incidence, as a function of the electric field in the insulator. The dotted lines represent the extrapolation of the RILC at low electric fields.

is the experimental confirmation that the retention capability reductions of FG Flash memory cell is mostly due to RILC through the Tunnel oxide and that the ONO RILC has a low impact on the threshold voltage variation measured in a FG cell programmed after heavy ion irradiation.

Two major facts can explain why the ONO capacitor RILC is lower than that of the Tunnel capacitor. The first is the larger thickness of the ONO stack respect to the Tunnel oxide. Due to the larger thickness, more traps are needed to form the conductive path and the electrons are subjected to more tunneling processes to pass from cathode to anode. This results in a lower RILC.

The second is the presence of the nitride layer that can act as trapping layer. Electrons from the cathode can be trapped into the nitride layer. This negative charge causes a reduction of the electric field in the oxide between the cathode and the nitride layer with a consequent tunneling probability reduction.

It is also important to note that irradiation has similar effects on the Tunnel and ONO capacitors (for instance, the RILC observed after I ion irradiation can be fitted using the same law and the effects of Ni ion irradiation are similar in ONO and Tunnel capacitors). These similarities suggest that the variations observed in the ONO capacitors after irradiation are mostly related to defects produced in the Top and Bottom oxide, and not in the nitride layer.

4.4 ONO RILC annealing

The ONO and Tunnel capacitors were measured two days after the irradiation (I ions, 10^{11} cm^{-2}, 0°) and then 8, 21 and 37 days after the irradiation. The devices were stored floating at room temperature in the time between two measurements. The RILC current of Tunnel and ONO capacitors decreases with time. In Fig. 16 we report the current measured in Tunnel and in

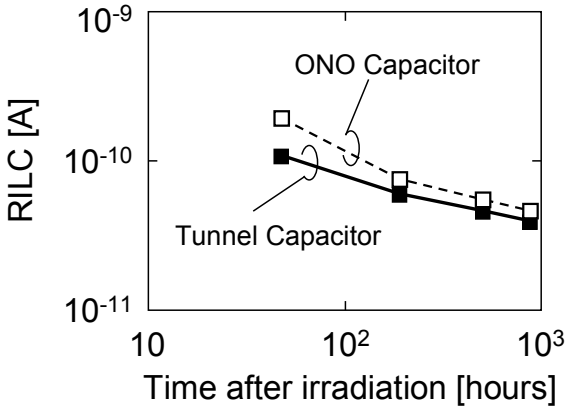


Fig. 16 RILC current of the ONO and of the Tunnel capacitor the device irradiated with I ions, fluence 10^{11} cm^{-2}, at 0°, as a function of the time after irradiation.

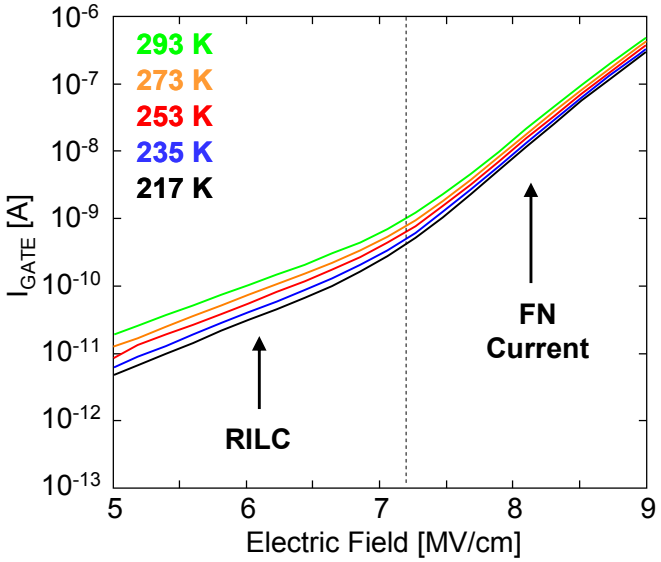
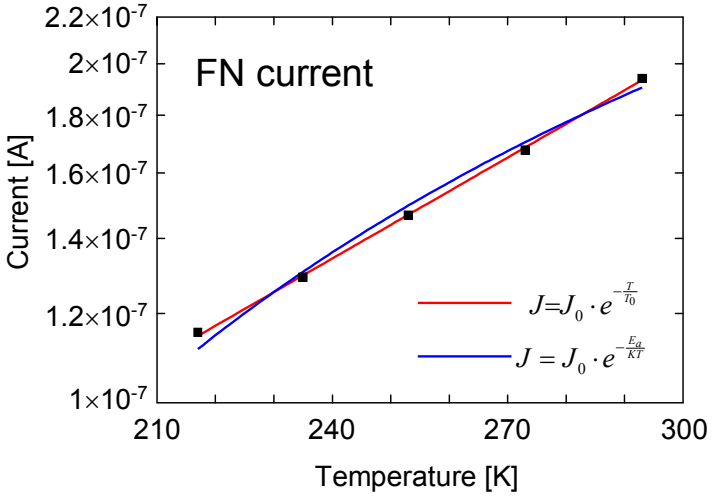


Fig. 17 Current of an irradiated capacitor as a function of the electric field, measured at the different temperatures of 293, 273, 253, 235 and 217 K.

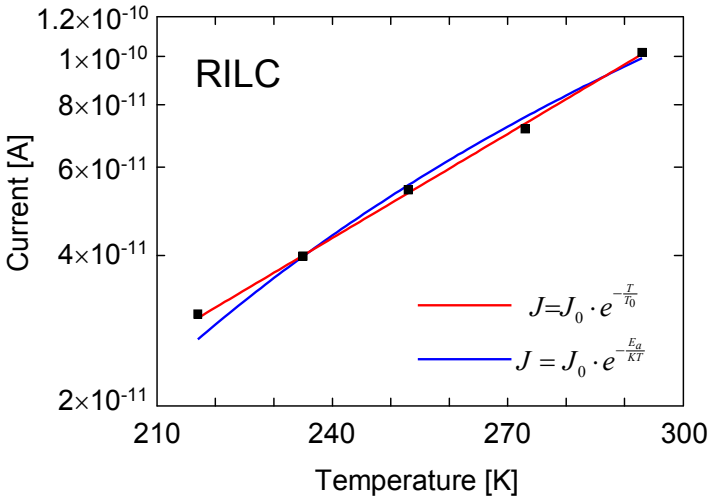
ONO capacitors at $V_{Poly1Sub}$ = -6.3 V and $V_{Poly2Poly1}$= -10 V, respectively. With reference to Figs. 5 A and 10, we see that at these voltage values the measured current is mostly constituted by the RILC current flowing through the insulator. The ONO and Tunnel RILC show the same decreasing behavior with time due to the recovery of the defects responsible for the conductive path. This fact indicates that the defects responsible of the RILC in Tunnel and in ONO capacitors could have the same physical nature, confirming again that the ONO RILC is determined by the defects located in the Top and Bottom oxide.

4.5 RILC vs Temperature

Fig. 17 shows the I-E curves measured at the different temperatures of 293, 273, 253, 235 and 217 K on a Tunnel capacitor after irradiation with I ions, at a fluence of 10^{11} cm^{-2}. We observe a reduction of both the FN current and the RILC in the log-plot as the temperature



(A)



(B)

Fig. 18 Fowler-Nordheim current (A) and RILC (B) as a function of the temperature. The blue and the red lines represent the fit of the experimental point obtained using eq. (1) and eq. (2), respectively.

decreases. Yet, RILC feature a larger variation than FN current. In Figs. 18 A and B we have plotted the FN current (@ E= 8.7 MV/cm) and the RILC (@ E= 5.6 MV/cm), respectively, as a function of the temperature. Both the FN current and the RILC behavior towards temperature is accurately fitted by the law proposed by De Salvo et al. [Des99b] to extrapolate the data-retention of nonvolatile memories:

$$J = J_0 \cdot e^{-\frac{T}{T_0}} \qquad (1)$$

For comparison, in Fig. 18 A and B we have reported also the best fit (dotted line) obtained using the Arrhenius equation:

$$J = J_0 \cdot e^{-\frac{E_a}{KT}} \qquad (2)$$

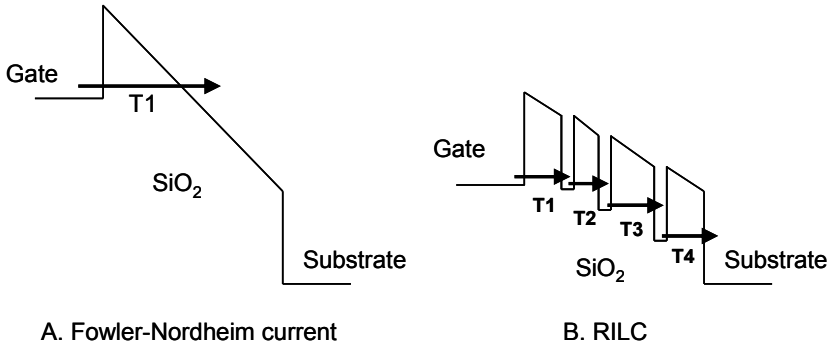


Fig. 19 Schematic representation of the Fowler-Nordheim current (A) and of RILC (B), assuming four traps in the oxide.

commonly used to extrapolate the activation energy of SILC in thin oxide. Noticeably, eq. (2) does not fit the experimental data.

T_0 in eq. (1) has a similar meaning of Ea in eq. (2), indicating the sensibility of the current to the temperature. The lower is T_0, the larger is the variation of the current with the temperature. The fact that both RILC and FN current can be fitted by equation (1) supports that the two currents are related to the same conduction mechanism, i.e., the electron tunneling.

The current reduction with the temperature observed in Fig. 17 is due to several causes, such as the variation of the electron number and distribution in the cathode conduction band. Yet, the most important cause is the reduction of the tunneling efficiency: the lower is the temperature the lower is the tunnel probability. Physically, this is due to the increase of the potential barrier height with the temperature [Des99b].

RILC features a larger decrease with temperature than FN current. This can be explained considering the two different conduction mechanisms (Fig. 19). FN current (Fig. 19 A) is due to electrons injected from cathode that pass the oxide by only one tunneling process (T_1 in the figure). Conversely, RILC (Fig. 19 B) is due to electrons pass thought the oxide by M-TAT and they are subjected to several Tunneling processes (T_1 – T_4). Hence, the reduction of the tunneling efficiency caused by the low temperature has a larger impact on RILC, being several the tunneling processes involved.

In Fig. 20 we report T_0 as a function of E. The current is dominated by RILC for E < 7 MV/cm and by FN current for higher E values. Hence, the T_0 values for E < 7 MV/cm are related to RILC and the T_0 values for E > 7 MV/cm are related to the FN current. As expected from the result of Fig. 17, the T_0 values of RILC are lower than those of the FN current. The RILC T_0 values show a linear behavior as a function of the E that can be well fitted using the following empirical law:

$$T_0 = 11.2 \cdot E$$

Incidentally, some works evidence that the E_a of SILC feature a linear relation with the electric field.

The FN current T_0 values show a different behavior: T_0 increases faster as a function of E and the T_0 values cannot be fitted using a linear fitting. These differences may be ascribed to the

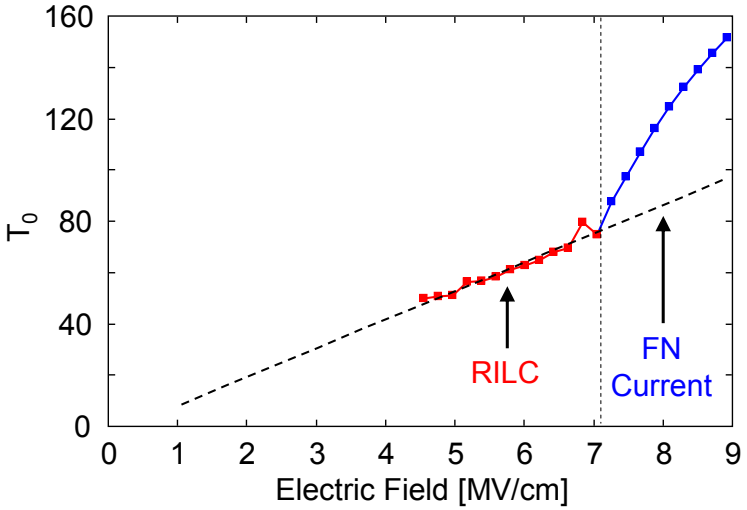


Fig. 20 T_0 values as a function of the electric field. The dotted line represents the linear interpolation of the T_0 values of RILC.

different tunneling process involved: at high electric field the electrons of the cathode conduction band see a triangular barrier and that they pass through FN tunnel. On the contrary, RILC is observed at lower E and the tunneling of electrons from one trap to another one is a direct tunneling.

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